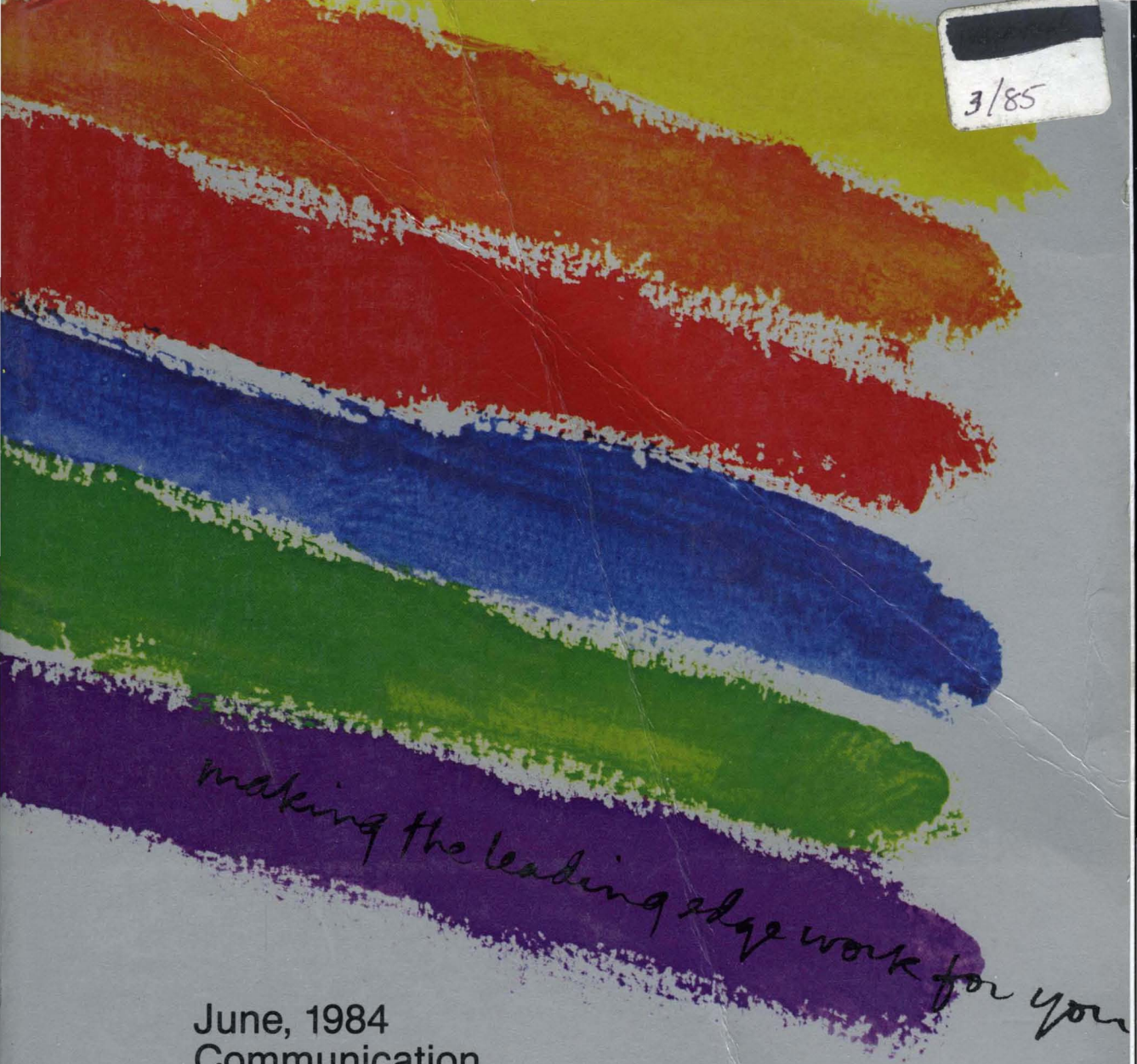

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June, 1984
Communication
Products Handbook

WESTERN DIGITAL
CORPORATION

June, 1984
Communications
Products Handbook

Making The Leading Edge Work For You.

This handbook is designed for you, the engineer. It's intended to be a useful tool, enabling you to make a preliminary evaluation of our products and later, with samples in hand, design our products into your own systems.

The data in these pages have been reviewed by our Marketing, Engineering, Manufacturing, and Quality groups. Now we would like you to review the information we've provided and tell us how we can improve it. Please feel free to suggest any changes, additions, or clarifications that occur to you. And don't hesitate to call to our attention any sins of omission or commission we may have made.

We're eager to help upgrade the quality of information our industry provides to its customers. So, please, help us. Direct your comments to:

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Table of Contents

Bulletin: New products soon to be announced.

Advance Information: This product has not been produced in volume and is subject to functional and timing revisions. Please contact Western Digital Corporation for current information.

Preliminary: This product is limited production and may be subject to change after device characterization has been completed. Please contact Western Digital Corporation for current information.

Final: This product is in full production and intended for normal commercial applications. For military, extended temperature, burn-in, or hi-rel applications, contact Western Digital Corporation for information regarding further processing.

Application Note: This is specific application information related to the designated product(s).

COMMUNICATION PRODUCTS — Functional Index

Part Number — **Page**

Numerical Index

WESTERN DIGITAL
CORPORATION

System Product Quality/Reliability

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown on the attached organization chart (Figure 2) reports directly to the President of Western Digital. It assures compliance to design control, quality and reliability specifications pursuant to corporate policy. Quality assurance provisions are derived in part from MIL-Q-9858, as applied to high grade commercial products.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution of the quality program rests with functional organizations to design, produce, and market high quality and high reliability products specified to our customers.

DESIGNING FOR RELIABILITY

The premise upon which board and system manufacturing operations are based is that quality is planned and designed-in, not screened-in or selected. A well-tested, high-quality design is far more reliable than a marginal design with any amount of burn-in or fixes. To assure top quality design, Western Digital maintains one of the most experienced board/system design staffs in the industry. A tightly controlled design review team comprising members from Quality Assurance, Marketing, Manufacturing and several experienced design engineers, provides review of each new design several times during its development to ensure widest possible performance margins. The production release procedure assures a checklist for:

- ☑ Test Method/Program Qualifications
- ☑ Characterization Report
- ☑ Field Test (Beta Test) Report
- ☑ Product Qualification Audit
- ☑ Documentation Package Release for Document Control
- ☑ Software/Diagnostics Qualification

MAINTAINING QUALITY/RELIABILITY IN PRODUCTION

The Quality Control Testing Flow Chart shown on Figure 1 defines the exact stages contained in the production process. Internally manufactured LSI components undergo 100% testing at maximum specified operating temperatures as well as strict quality controls defined to assure high quality and reliability. Components not designed and manufactured by Western Digital are also 100% screened as shown in photos during incoming inspection at 70°C. The tests performed include selective active component burn-in performed at 125°C for 160 hours to insure guaranteed levels of reliability. This 125°C accelerated testing eliminates defects that cannot effectively be accelerated by burning-in boards and systems which have temperature limitations. Key quality control procedures include:

- Incoming Inspection Procedure
- In-Process Travel Card Traceability
- Workmanship Standards
- Quality Corrective Action Notice/MRB Procedure
- Quality Audit Procedure

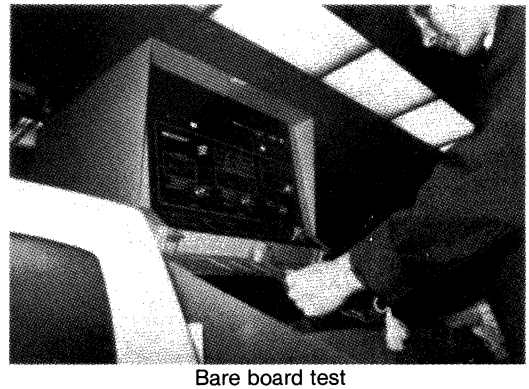
PRODUCT FINAL TEST/CORRECTIVE ACTION

All boards are 100% in-circuit tested and 100% functional tested for acceptable performance according to applicable test specifications on testers qualified by QA. Products are tested at maximum specified temperature and voltage margins using diagnostic software to ensure greater performance margins. Failures are logged on a travel card specifically designed to insure traceability to manufacturing steps and to maintain failure records for QA corrective action.

If the board is designed to perform in a host system, further diagnostics are performed in an environment configured to actual customer requirements.

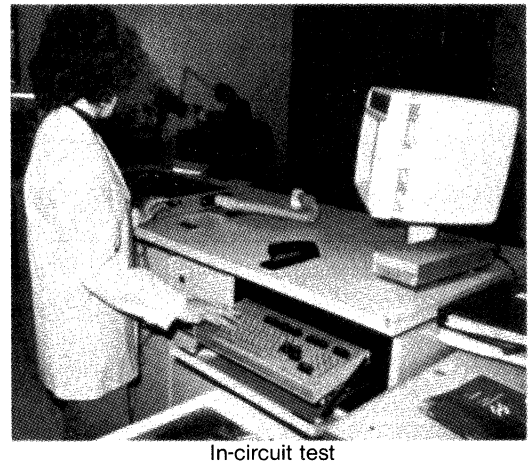
PRODUCT ACCEPTANCE

Upon completing the final test, the board/system undergoes QC final workmanship standards inspection and selective samples are audited to the functional product specification to guarantee quality at specified operating margins to the customer.



Bare board test

Incoming IC 100% screening



In-circuit test

Complete documentation available for you at our facility.

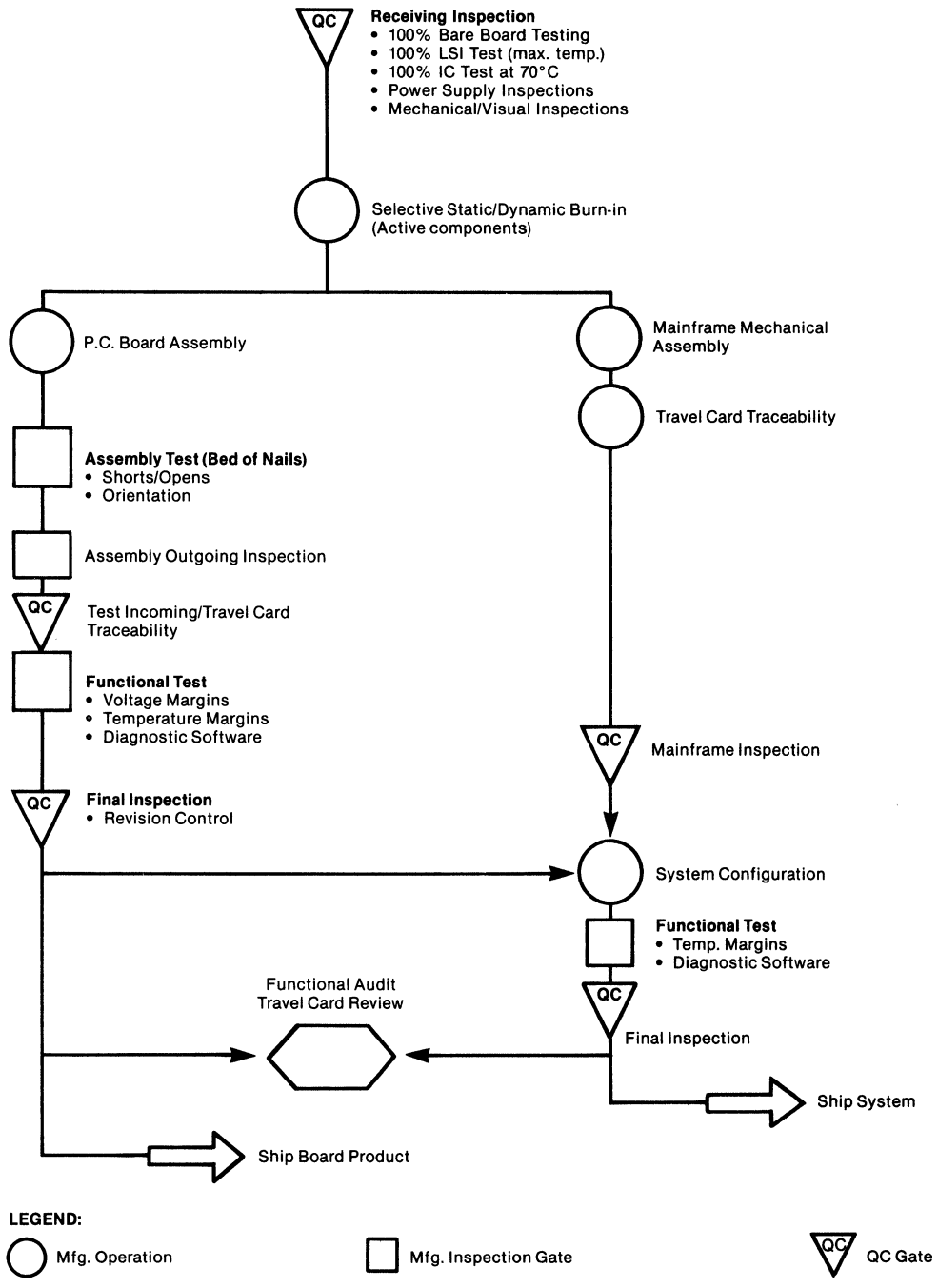


Figure 1. QUALITY CONTROL TESTING FLOW CHART

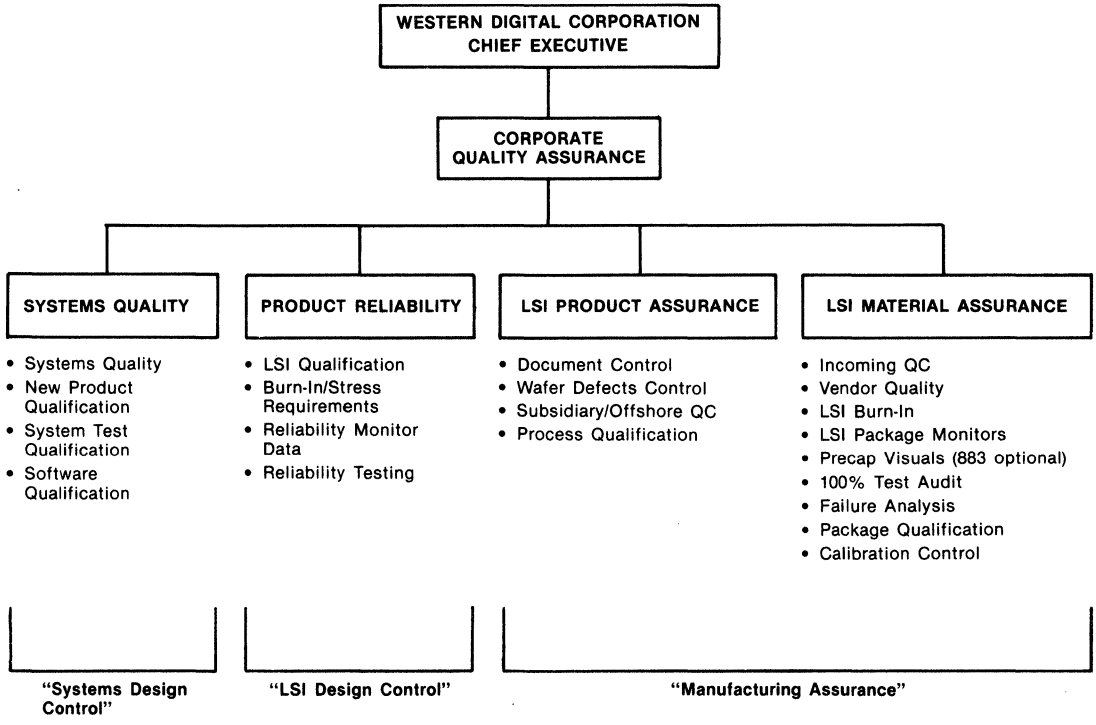


Figure 2. QUALITY ORGANIZATION

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Quality/Reliability To Leading Edge Technology

QUALITY PROGRAM DESCRIPTION

The Quality Organization shown in Figure 2 assures compliance to design control, quality and reliability specifications, pursuant to corporate policy.

CORPORATE QUALITY POLICY

It is the policy of Western Digital Corporation that every employee be committed to quality excellence in producing products/processes which conform to acceptable requirements. The total quality program is managed and monitored by the quality assurance organization. Quality assurance is chartered to review marketing product requirements, qualify hardware and software designs, certify manufacturing operations and monitor performance/control conformance to product specifications.

Primary responsibility for execution for the quality program rests with functional organizations to design, produce and market high quality and high reliability products specified to our customers.

LSI QUALITY ASSURANCE PROGRAM HIGHLIGHTS

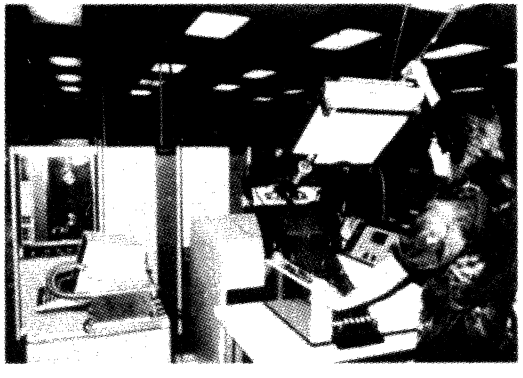
- LSI manufacturing assurance provisions are derived in part from MIL-M-38510 and MIL-STD-883B as applied to high grade commercial components.
- All process raw materials used in the Mask/Wafer fabrication and assembly operations are monitored by Material Assurance.
- Material Assurance maintains a thorough control of incoming material and has developed unique "use/stress tests" (look ahead sample build acceptance) which critical material must pass before acceptance.
- The Product Assurance Department continuously monitors the internal and external manufacturing flow (shown in Figure 1) and issues process control reports displaying detailed data and trends for the associated areas.
  - — Document control is an integral part of Product Assurance. All specifications are issued and controlled by this activity.
  - — The Western Digital Malaysian assembly operation uses specifications and quality control provisions controlled by Document Control. Indicators of Malaysia quality are reviewed weekly.
  - — Purchased FAB and assembly operations are individually qualified and are certified against standard specifications during vendor qualification and monitored against reliability criteria.
  - — Defect control within the process assures the highest levels of built-in reliability.
- Quality audits and gates are located throughout the manufacturing process in order to assure a stable process and thus, a quality product to our customers. Figure 1 illustrates the manufacturing/screening/inspection flow diagram and identifies the steps as they relate to the production of LSI devices.
- Testing assures quality margins through 100% testing by manufacturing and, in addition, all products must pass a specified AQL sample test performed by QA at maximum operating temperature as follows:

Outgoing Quality Levels

SUBGROUPS	INSPECTION LEVEL
Subgroup 1 — Final 100% Electrical Audit @ Max °C	0.5 AQL*
Subgroup 2 — Visual (Marking, Lead Integrity, Package, Verify customer shipper)	1.0 AQL
Subgroup 3 — Shipping Visual Audit	1.0 AQL

*The double sampling techniques used allow considerably better AQL's in most all cases.

- LSI devices are 100% tested on industry standard test systems like that shown below. Quality outgoing testing (auditing) is done on the Fairchild Sentry Series 20 where possible to allow better correlation with customers.



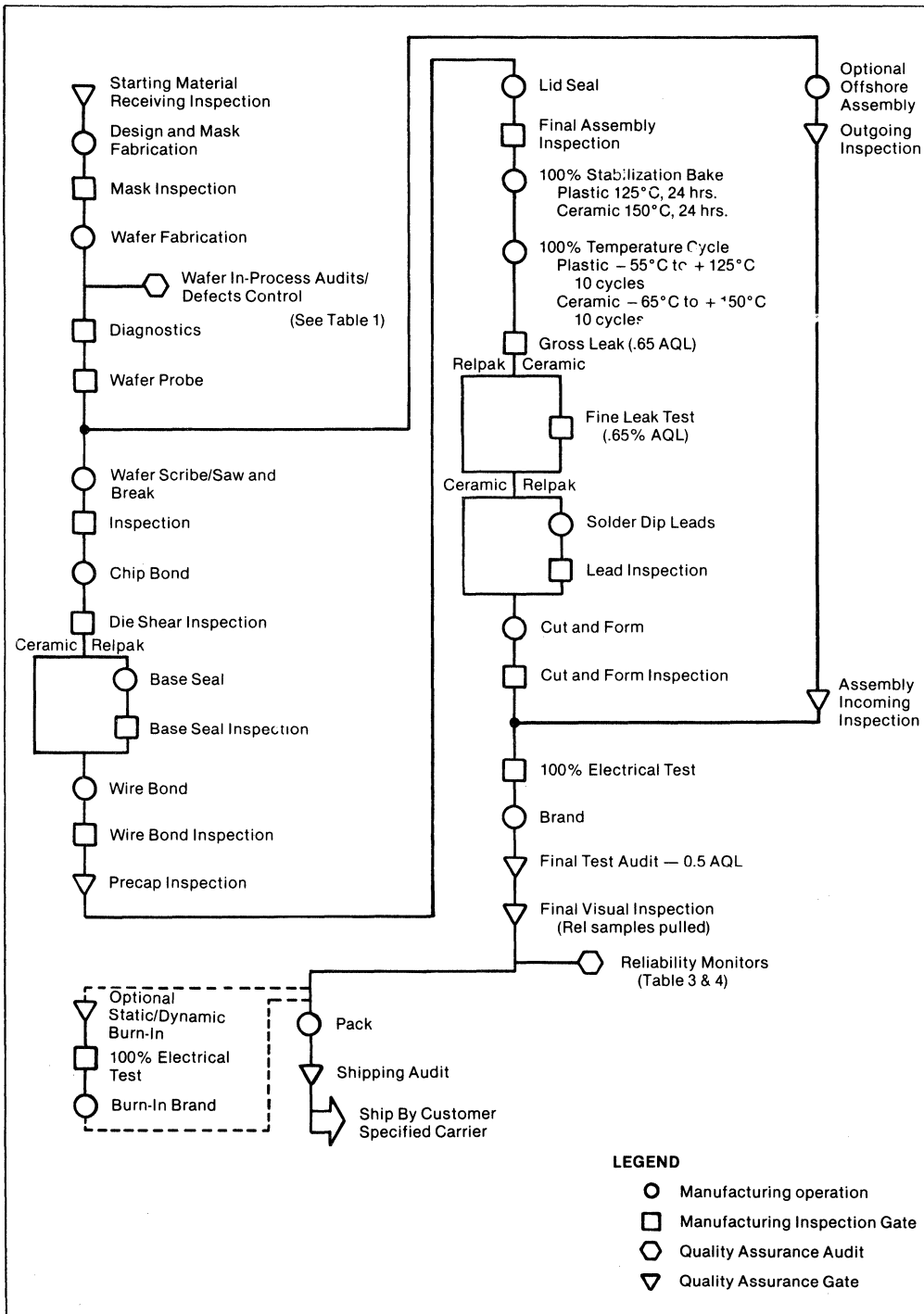


Figure 1 LSI PRODUCTION FLOW

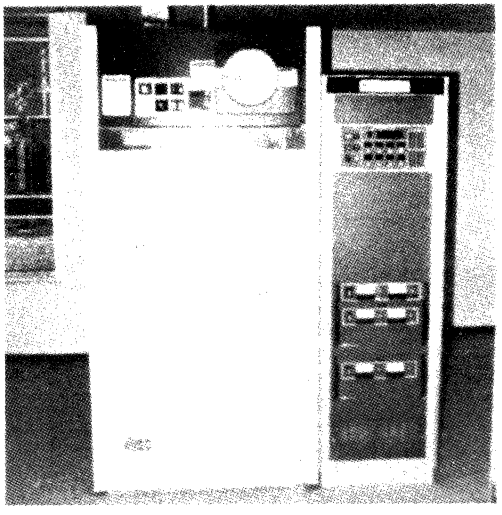
Reliability Means Lasting Value

• DESIGNING FOR RELIABILITY

The production release procedure for an LSI device is designed to assure maximum reliability with a Quality checklist for:

- Test program qualifications
- Characterization report
- Field test (Beta Test) report
- Reliability Lifetest Qualifications
- Infrared Thermal Analysis
- Static Protection

All new devices and major process changes must pass reliability qualification before incorporation into production using the criteria defined in Tables 2-4. The infrared microscope shown on the right assures optimum burn-in temperatures and margins of safety. The dynamic burn-in system shown on the right is one of two custom designed systems which assure protective device isolation during burn-in.



• MAINTAINING RELIABILITY IN PRODUCTION

Process defects control are defined to continually measure built-in reliability, as measured by the following criteria:

TABLE 1

PROCESS RELIABILITY CONTROL	METHOD	CONDITION	SAMPLE*
Subgroup 1 — Defects Control			
a. Oxide Integrity	Non-destructive bubble test	Pinhole defect density	5 wafers
b. Polysilicon Integrity	SEM Analysis	Visual	5 wafers
Subgroup 2 — Electro-Migration Control			
Metal Step Coverage	MIL-STD-883 Method 2018	SEM Analysis	5 wafers
Subgroup 3 — Defect Density	Critical layers Field Gate Contact Metal	Visual of Photo defects (Defects/in^2)	8 wafers each layer
Subgroup 4 — Passivation/Insulation Integrity	MIL-STD-883 Method 2021	Visual of Pinhole defect density	Final Silox 5 wafers Intermediate 5 wafers

*Inspection intervals are defined by the in-line process control data reviewed on a lot-by-lot basis.

• PROGRAMS TO ASSURE OPTIMUM RELIABILITY

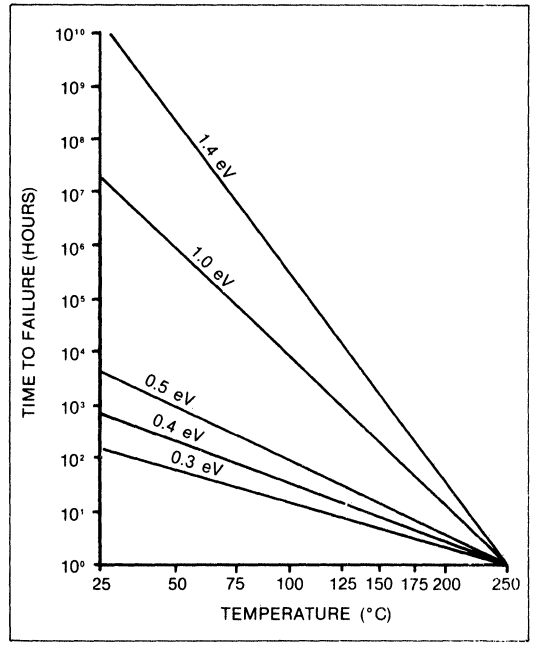
Improved levels of reliability are available under custom reliability programs using static and dynamic burn-in to further improve reliability. These programs focus on MOS failure mechanisms as follows:

FAILURE MECHANISMS IN MOS

FAILURE MECHANISM	EFFECT ON DEVICE	ESTIMATED ACTIVATION ENERGY	SCREENING METHOD
Slow Trapping	Wearout	1.0 eV	Static Burn-In
Contamination	Wearout/ Infant	1.4 eV	Static Burn-In
Surface Charge	Wearout	0.5-1.0 eV	Static Burn-In
Polarization	Wearout	1.0 eV	Static Burn-In
Electromigration	Wearout	1.0 eV	Dynamic Burn-In
Microcracks	Random	—	100% Temp. Cycling
Contacts	Wearout/ Infant	—	Dynamic Burn-In
Oxide Defects	Infant/ Random	0.3 eV	Dynamic Burn-In at max. voltage
Electron Injection	Wearout	—	Low Temp. Voltage Operating Life

Temperature Acceleration of Failure

The Arrhenius Plot defines a failure rate proportional to exp(– Ea/kt) where Ea is the activation energy for the failure mechanism. The figure on the right indicates that lower activation energy failures are **not** effectively accelerated by temperature alone; hense, maximum voltage operation is selectively applied to optimize the burn-in process.



Static Burn-In (125°C — 48 hours or 160 hours)

Provided on a sample basis for process monitor/control of 0.5 eV — 1.0 eV failure mechanisms. 100% static burn-in may be specified at an additional cost. However, static burn-in is considered only partially effective for internal LSI gates at logic "O" levels.

Dynamic Burn-In (Pattern test/125°C — 8 hours to 160 hours)

Accelerated functional dynamic operating life effectively controls internal MOS gate defects buried from external pin access. The input pattern is optionally pseudo-random or fixed pattern programmable to simulate 1000-3000 hours of field operation at maximum operating voltage(s).

High-Rel "K" Testing Program

General conformance to MIL-STD-883B method 5004.4, Class B with static Burn-In (Dynamic Burn-In may be specified as an option).

LSI RELIABILITY STANDARDS

TABLE 2 STANDARD RELIABILITY LEVELS

TEST	METHOD	CONDITION	FAILURE
Infant Mortality (see note)	Static Burn-In	125°C — 160 hrs.	<0.5%
Long Term Failure Rate	Dynamic Life Test	125°C — 1000 hrs.	<.05%/1000 hrs. @ 55°C 60% Confidence

*NOTE: Devices failing the infant mortality target remain on burn-in until acceptable failure rates are obtained.

TABLE 3 GROUP A DEVICE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Internal Visual			15
b. Thermal Shock	1011	Test Failure Used (cond. B or C)	
c. Bond Strength	2011	Test Failures (cond. B)	
d. Die Shear Strength	2019	Test Failures	
Subgroup 2			
a. Seal — Gross Leak		Fluorocarbon detection 10^{-3} atm/cc/sec	15
b. Seal — Fine Leak	1014	Test Condition A	
Subgroup 3			
a. Rotating Steady State Life Test	1005	Static 160 hr. Burn-In 125°C plus 125°C Lifetest — 1000 hrs.	5
b. Electrical Parameters	—	Final electrical @ 25°C (with data @ 70°C)	

TABLE 4 GROUP B PACKAGE RELIABILITY MONITORS

TEST	METHOD	CONDITIONS	LTPD
Subgroup 1			
a. Thermal Shock	1011	Test Condition B or C	15
b. Temperature Cycling	1010	Test Condition B or C	
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Electrical at max -C	
f. 85/85 Moisture Resistance (plastic only)	—	85% RH/85°C for 1000 hours PDA = 10%	
g. Electrical Parameters	—	Final electrical @ 25°C	
Subgroup 2			
a. High Temp. Storage	1008	Test Condition B or C	
b. Mechanical Shock	2002	Test Condition B	15
c. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
d. Seal — Fine Leak (ceramic)	1014	Test Condition A	
e. Electrical Parameters	—	Final electrical @ 25°C/max. C	
Subgroup 3			
a. Lead Integrity	2004	Test Condition B2 (Lead Fatigue)	15
b. Seal — Gross Leak	—	Fluorocarbon detection 10^{-3} atm/cc/sec	
c. Seal — Fine Leak (ceramic)	1014	Test Condition A	

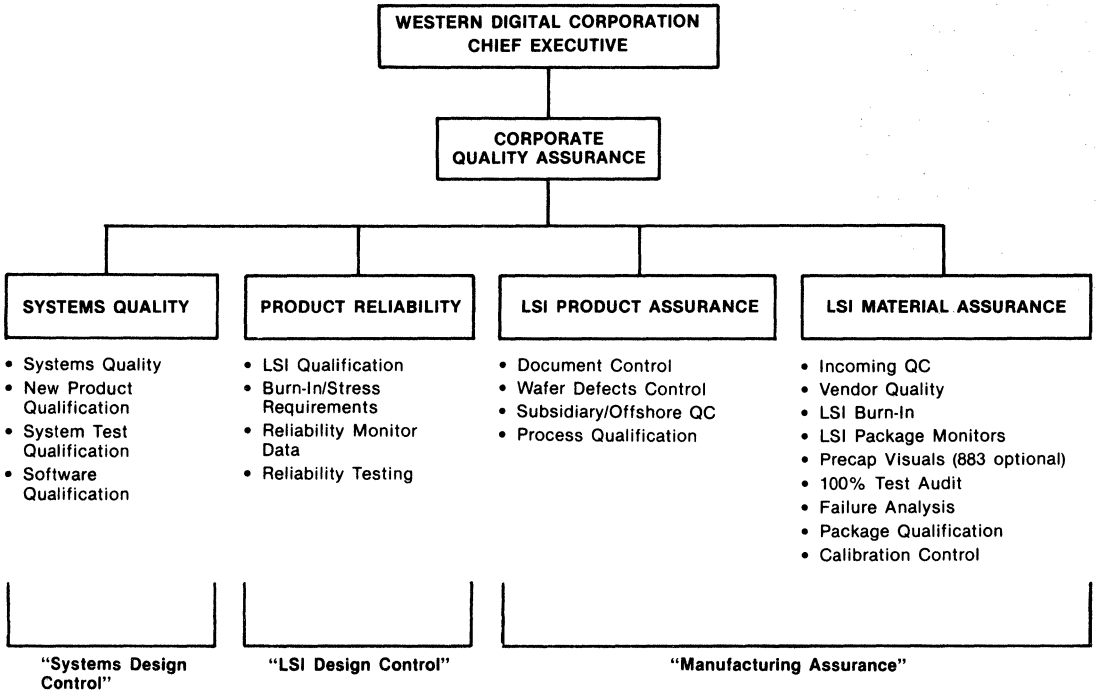


Figure 2 QUALITY ORGANIZATION

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Announcing Burn-In Program Availability/Warranties

Western Digital now supports customer burn-in requirements for both static and dynamic burn-in under the strict control of the QA-Reliability organization.

This burn-in provides high performance 125°C static and dynamic burn-in for 8-160 hours to eliminate infant mortality and improve reliability. This process is executed using custom modified 32Bit AEHR test commercial burn-in equipment which provide monitored fixed pattern or pseudorandom burn-in with power supply and resistor device pin isolation.

LSI dynamic burn-in is verified in all cases by the design engineer for proper functioning. LSI Chip sets are also individually burned-in with dynamic equivalency to assure high performance bundled reliability.

The warranty on the program will optionally provide certificate of compliance to standard or custom designed burn-in programs and guarantee <.05%/Khrs failure rate.

CAUTION

Using outside burn-in methods not certified as acceptable by Western Digital may result in voided warranty, due to mishandling, junction temperature stress, or electrical damage. Further, since most burn-in houses do not support testing, catastrophic system condition can result in substantial damage before a problem is identified.

One consistent problem experienced with outside LSI burn-in houses can cause reliability problems; namely, parallelling totem pole MOS outputs, where the output states are not predictable, can cause a single (or a few) device(s) to sink all the current from the other devices on the burn-in tray — electromigration or current zaps are both possible.

Western Digital burn-in diagrams, dated after 1/1/82, must be used exactly as shown and will be provided upon request.

SEE YOUR LOCAL REPRESENTATIVE FOR COSTS AND ORDERING INFORMATION ON THIS NEW PROGRAM.

Hi-Rel "K" Testing Program

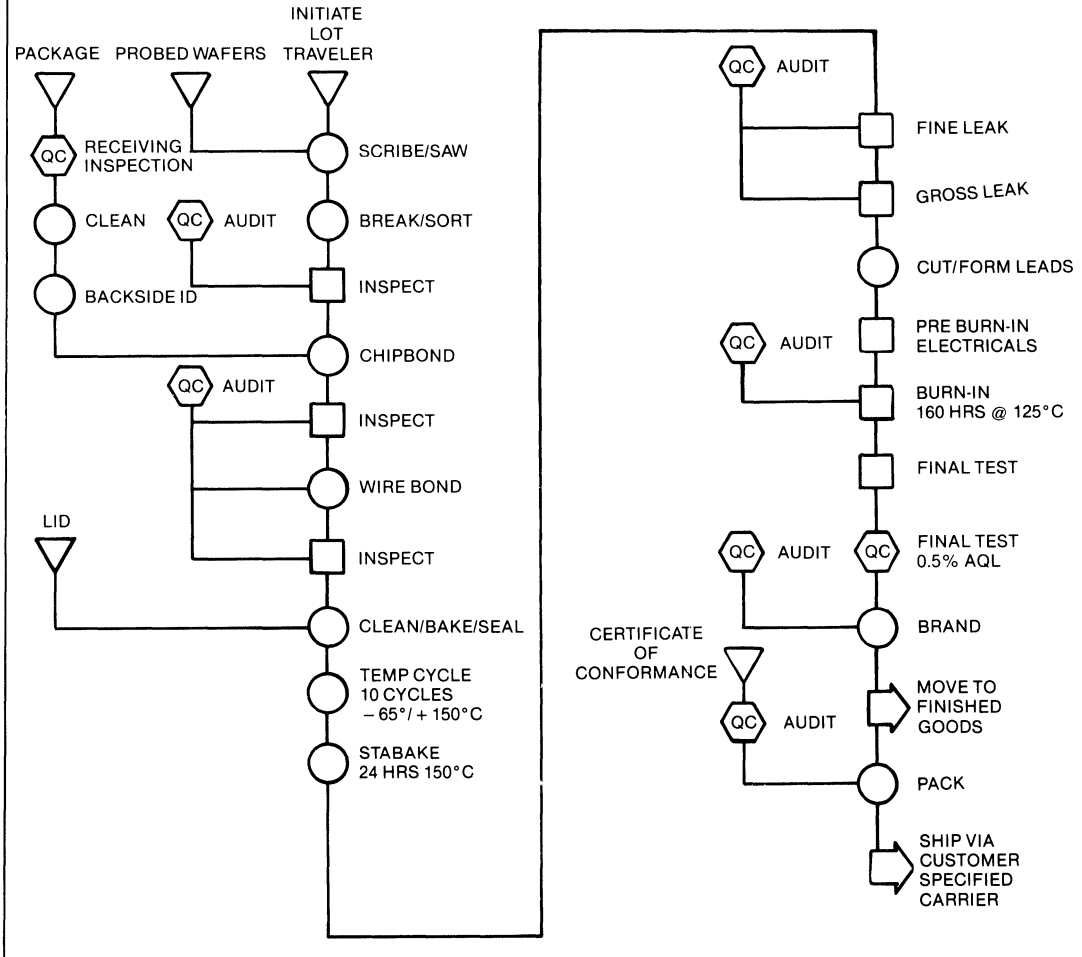
FEATURES

GENERAL CONFORMANCE TO MIL-STD-883B, METHOD 5004.4, CLASS B (SEE COMPARISON ON FOLLOWING PAGES)

- INCLUDES:
  - PRECAP VISUALS
  - SEAL INTEGRITY
  - POWER CONDITIONING
  - ENHANCEMENT OPTIONS

GENERAL DESCRIPTION

Western Digital's Hi-Rel "K" program is designed to provide high reliability devices for extended temperature environments. Individual enhancements may be specified to meet a customer's requirements.



HI-REL "K" PROGRAM FLOW DIAGRAM

COMPARISON OF MIL-STD-883 AND HI-REL "K" TEST PROGRAM

MIL-STD-883B, METHOD 5004.4, CLASS B	HI-REL "K" TEST
3.1.1 Internal Visual Method 2010.3 Test condition B	All Hi-Rel "K" devices receive 100% inspections prior to lid seal. These inspections together comprise criteria comparable to Mil-Std-883, method 2010.3, test condition B.
3.1.2 Stabilization Bake Method 1008.1 Test condition C 24 hours at 150°C	Same
3.1.3 Temperature Cycling Method 1010.2, Test condition C −65°C to 150°C for 10 cycles, with 10 minutes dwell and 5 minutes maximum transfer time	Same
3.1.4 Constant Acceleration Method 2001.2, Test condition E. 30,000 G stress level	Not Done Unless Specified
3.1.5 Visual Inspection Visual inspection for catastrophic failures after screens	Same
3.1.6 Seal Method 1014.2 (a) Helium fine leak — Test condition A_1. Bomb condition 2 hours at 60 psig. Reject limit 5×10^{-8} torr	Same
(b) Flourocarbon gross leak — Test condition C	Same
3.1.9 Interim (pre-burn-in) Electricals Per applicable device specification	Preburn-in test at 25°C. Must meet requirements of device data sheets.
3.1.10 Burn-in Test Method 1015.2 160 hours @ 125°C	Same
3.1.13 Interim (Post burn-in) electricals Per applicable device specification	Burn-in equipment isolate failures automatically to assure no harmful interaction.
3.1.15 Final Electrical Test (a) Static Tests (1) 25°C (2) Minimum and Maximum Operating Temperatures (b) Dynamic and Switching Tests at 25°C (c) Functional Tests at 25°C	Same
3.1.17 Qualification or Quality Conformance Inspection and Test Sample Selection	Not done unless defined using method 5005 as a guide.
3.1.18 External Visual Method 2009.2	Same

WESTERN DIGITAL RELIABILITY ENHANCEMENT OPTIONS

100% Temperature Testing

Level ..... −40° to +85°C
..... −55° to +125°C

Thermal, Shock (Liquid to Liquid)

Level..... 0° to +100°C, 15 cycles
..... −55° to +125°C
..... −65° to +150°C

Extended High Temperature Storage

+150°C for 24 hours standard, other time/temperature storage requirements available as required.

Dynamic Burn-In

Per note previously supplied.

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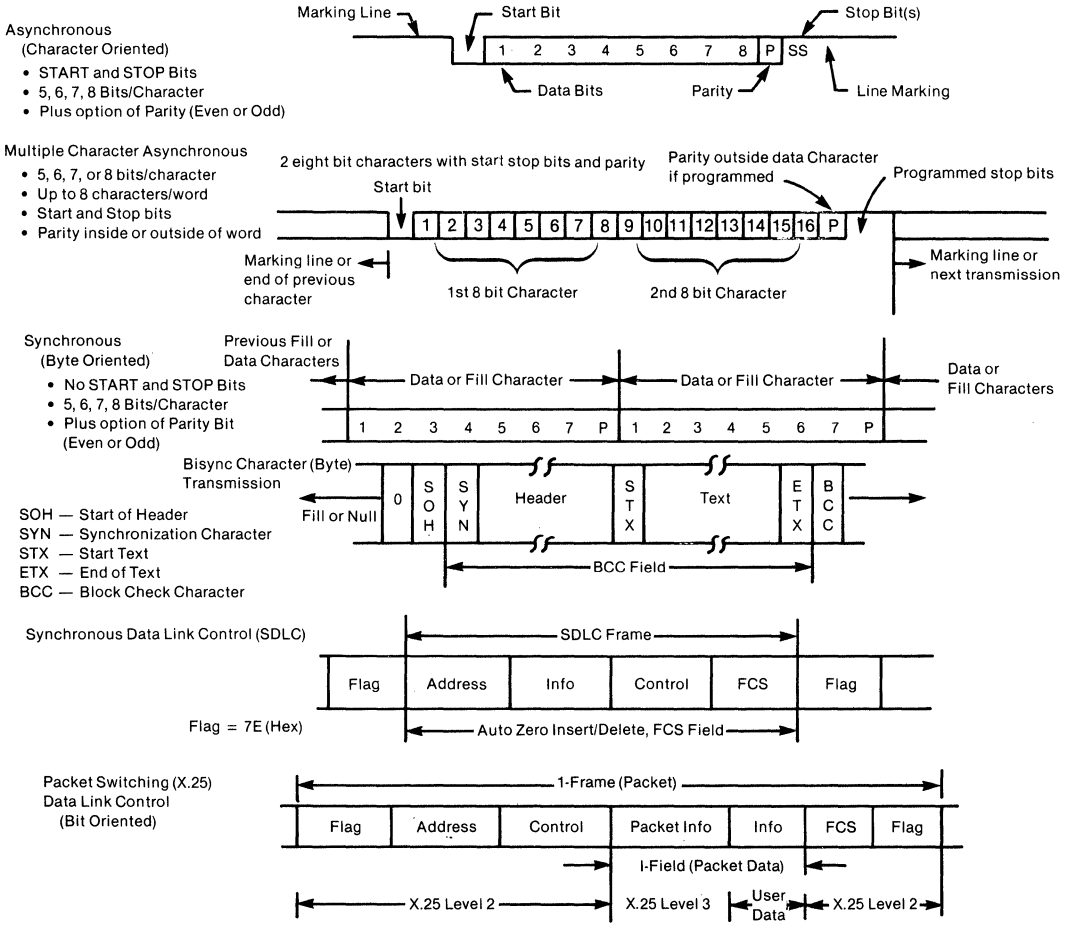
COMMUNICATION FAMILIES

UART — Universal Asynchronous Receiver-Transmitter
PSAT — Programmable Synchronous/Asynchronous Transmitter
PSAR — Programmable Synchronous/Asynchronous Receiver
USART — Universal Synchronous/Asynchronous Receiver-Transmitter
BOART — Bus Oriented Asynchronous Receiver-Transmitter
DLC — Data Link Controller

PROTOCOL DEFINITIONS

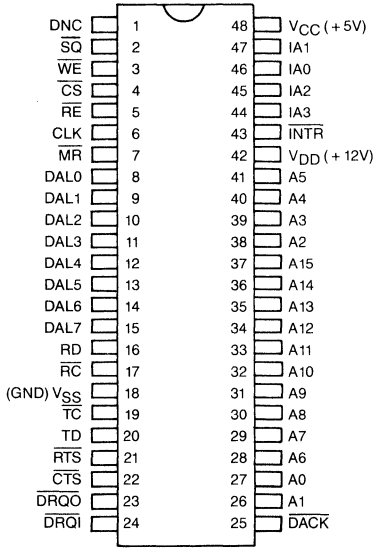


PRELIMINARY

WD2840 Local Network Token Access Controller

FEATURES

- Broadcast Medium Independent (Coax, RF, CATV, IR, etc.)
- Up to 254 nodes
- Dual DMA/Highly efficient Memory Block Chaining
- Token based protocol
- Acknowledge option on each datagram
- Adjustable fairness, stations may be prioritized
- Frame format similar to industry standard HDLC
- Supports Global Addressing
- Diagnostic Support: Self-Tests, System and Network
- TTL Compatible



PIN DESIGNATION

DESCRIPTION

The WD2840 is a MOS/LSI device intended for local network applications, where reliable data communications over a shared medium is required. The device uses a buffer chaining scheme to allow efficient memory utilization. This scheme minimizes the host CPU time requirements for handling packets of data. The WD2840 frees the host CPU from extensive overhead by performing network initialization, addressing, coordination, data transmission, acknowledgements and diagnostics.

APPLICATIONS

The WD2840 is a general purpose Local Network Token Controller applicable to virtually all types of multi-point communications applications. The token protocol allows the sharing of one bus by up to 254 nodes. WD2840's will be designed into process control equipment, micro-computers, mini-computers, personal computers, proprietary micro-processor based applications, intelligent terminals, front-end processors, and similar equipment.

The great advantage for the design engineer is the ease with which he can implement a local network function. The WD2840 handles autonomously all major communications tasks as they relate to the local network function.

1.1 PIN DEFINITIONS

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1	DNC	DO NOT CONNECT	Leave pin open.
2	$\overline{SQ}$	SIGNAL QUALITY	An active low input which signals the WD2840 that a frame may be received. The modem may negate this signal if its receive signal quality is below a reliability threshold, ensuring that the WD2840 will not accept the frame.
3	$\overline{WE}$	WRITE ENABLE	The data on the DAL are written into the selected register when $\overline{CS}$ and $\overline{WE}$ are low. $\overline{RE}$ and $\overline{WE}$ must not be low at the same time.
4	$\overline{CS}$	CHIP SELECT	Active low chip select for CPU control of I/O registers.
5	$\overline{RE}$	READ ENABLE	The content of the selected register is placed on DAL when $\overline{CS}$ and $\overline{RE}$ are low.
6	CLK	CLOCK	Clock input used for internal timing.
7	$\overline{MR}$	MASTER RESET	Initialize on active low. All registers reset to zero, except control bit ISOL is set to 1. DACK must be stable high before MR goes high. Status Register 0 is not defined at power-up (this register will be set-up upon entry into the Network mode).
8-15	DAL0-7	DATA ACCESS LINES	An 8-bit bi-directional three-state bus for CPU and DMA controlled data transfers.
16	RD	RECEIVE DATA	Receive serial data input.
17	$\overline{RC}$	RECEIVE CLOCK	This is a 1X clock input, and RD is sampled on the rising edge of $\overline{RC}$.
18	V_{SS}	GROUND	Ground.
19	$\overline{TC}$	TRANSMIT CLOCK	A 1X clock input. TD changes on the falling edge of $\overline{TC}$.
20	TD	TRANSMIT DATA	Transmitted serial data output.
21	$\overline{RTS}$	REQUEST-TO-SEND	An open collector output which goes low when the WD2840 is ready to transmit either data or flags.
22	$\overline{CTS}$	CLEAR-TO-SEND	An active low input which signals the WD2840 that transmission may begin.
23	$\overline{DRQO}$	DMA REQUEST OUT	An active low output signal to initiate CPU bus request so that the WD2840 can output onto the bus.
24	$\overline{DRQI}$	DMA REQUEST IN	An active low output signal to initiate CPU bus requests so that data may be input to the WD2840.
25	$\overline{DACK}$	DMA ACKNOWLEDGE	An active low input from the CPU in response to $\overline{DRQO}$ or $\overline{DRQI}$. $\overline{DACK}$ must not be low if $\overline{CS}$ and $\overline{RE}$ are low or if $\overline{CS}$ and $\overline{WE}$ are low.
26-41	A0-A15*	ADDRESS LINES OUT	Sixteen address outputs from the WD2840 for DMA operation.
42	V_{DD}	POWER SUPPLY	+ 12VDC power supply input.
43	$\overline{INTR}$	INTERRUPT REQUEST	An active low interrupt service request output. Returns high when Interrupt Register is read.
44-47	IA0-IA3*	ADDRESS LINES IN	Four address inputs to the WD2840 for CPU controlled read/write operations with registers in the WD2840. If ADRV = 0, these may be tied to A0-A3.
48	V_{CC}	POWER SUPPLY	+ 5VDC power supply input.

WD2840 LOCAL NETWORK TOKEN ACCESS CONTROLLER

INTRODUCTION

The WD2840 is a single LSI device which gives systems designers the ability to include networking capabilities into their unique products simply and economically.

A general and fundamental advantage to the use of complex LSI in a given system is the partitioning of required technical expertise. A successful user of the WD2840 need not be a data-communications expert, and further, he need not be at all concerned with low level network details (though these details are documented and available to him if he is interested). The potential user of the WD2840 must simply evaluate the communications facilities provided by the device to determine its suitability for the intended use.

The WD2840 is designed to logically interconnect 2 to 254 user devices over a shared communications medium. Examples of typical mediums include coax cable, twisted pair bus, RF, and CATV. All network control functions, such as data framing and error checking, destination filtering, fair and adjustable transmission scheduling, and network initialization and fault recovery (caused by noise for example) are handled completely by the WD2840.

The protocol implemented allows guaranteed station access intervals allowing applications in factory automation and other critical communications environments where "statistical delays" are not acceptable. The WD2840 token protocol also allows the addition and/or removal of stations to a network at anytime, including while operating.

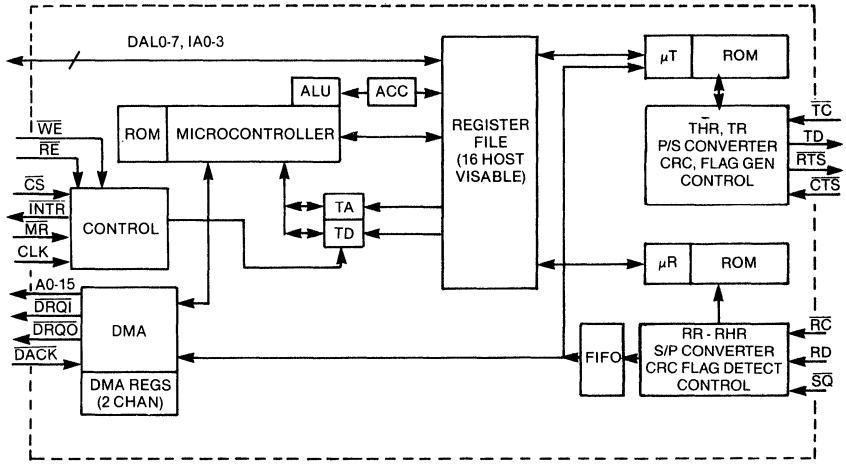


Figure 1.1 BLOCK DIAGRAM

Serious attention has also been given to the user's interface to the device. The interface is a combination of conventional I/O registers and an elaborate DMA buffer chaining interface. This chaining feature allows the user much more efficient use of his system memory, particularly in situations where the maximum message sent over the network is much longer than the average size. This feature also allows the automatic queueing of messages independently of the user's consumption rate, in effect, speed decoupling the user's CPU and processing requirements from the network.

The WD2840 has several parameters (registers) that allow tailoring to the user's requirements. In this way, network priority and access ordering, to name two, can be manually set if desired.

Using an integrated version of these network algorithms saves not only the development costs already mentioned, but further, the total processing power required for the user's application is not increased. In other words, a CPU upgrade can likely be avoided by "distributing" the network processing task into LSI devices such as the WD2840.

SCOPE

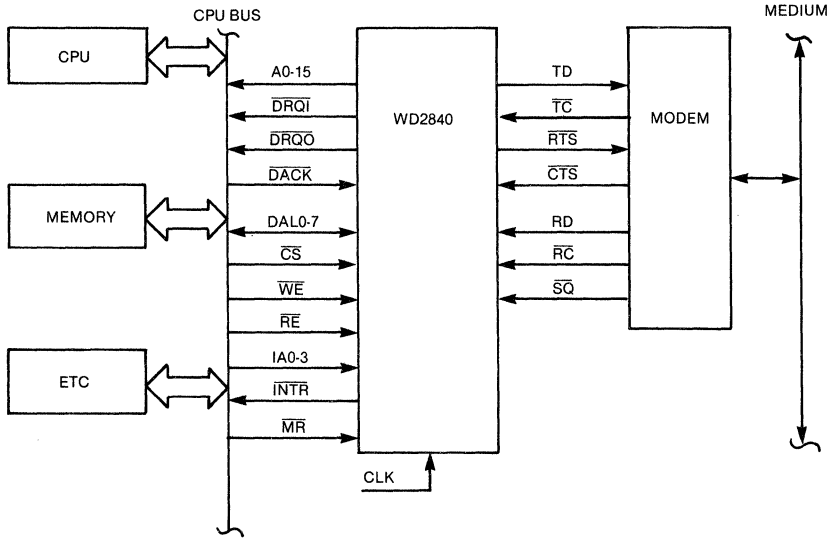
This document differs from traditional LSI data sheets in that it details not only the LSI implementation of a function, but also defines the overall function in detail. Specifically, this document includes details of the communications protocol implemented by the WD2840 Token Access Controller.

The document is organized into three main sections:

SECTION ONE is much like a traditional data sheet including register descriptions, pin definitions, and hardware architecture.

SECTION TWO describes the interfaces to the WD2840. The network side is conventional, the host side consists of an elaborate DMA interface with control blocks and WD2840/host handshaking.

SECTION THREE details the network protocol implemented by the device. Normal operation, initialization, and the handling of error conditions are described.



TYPICAL SYSTEM CONNECTION

1.2 DEVICE ARCHITECTURE

A detailed block diagram of the WD2840 is shown in Figure 1.1.

Mode control and monitor of status by the user's CPU is performed through the Read/Write Control circuit, which reads from or writes into registers addressed by IA0-IA3.

Transmit and receive data are accessed through DMA control. Serial data is generated and received by the bit-oriented controllers.

Internal control of the WD2840 is by means of three internal micro-controllers; one for transmit, one for receive, and one for overall control.

Parallel transmit data is entered into the Transmitter Holding Register (THR), and then presented to the Transmitter Register (TR) which converts the data to a serial bit stream. The Frame Check Sequence (FCS) is computed in the sixteen bit CRC register, and the results become the transmitted FCS.

Parallel receive data enters the Receiver Holding Register (RHR) from the 24 bit serial Receive Register (RR). The 24-bit length of RR prevents received FCS data from entering the RHR. The receiver CRC register is used to test the validity of the received FCS. A three level FIFO is included in the receiver.

The WD2840 sends all information, network control and user data, in blocks called frames. Each frame starts and ends with a single flag (binary pattern 01111110). In between flags, data transparency is provided by the insertion of a zero bit after all sequences of five contiguous one bits. The receiver will strip the inserted zero bits. (See section on frame format for location of address, control, and FCS fields.)

1.3 REGISTER DEFINITION

The WD2840 is controlled and monitored by sixteen 8 bit registers. This set of registers consists of two Control Registers, three Status Registers, an Interrupt Event Register, a Counter Register and a variety of Parameter Registers. In general the host is responsible for defining these registers (except certain host read-only registers: SR0-2, IR0, CTR0 and NA) to contain proper and meaningful values prior to entering Network Mode from Isolate State. Furthermore, while the WD2840 is in Network Mode, the CBP (H,L) and MA registers must not be changed by the host. Register NAR may be changed arbitrarily but will only be considered by the WD2840 in response to the NEWNA (CR10) control bit being set. The two Control Registers and the TA, TD, AHOLT, TXLT registers may change dynamically to control the behavior of the WD2840.

REG [1]	NAME	DESCRIPTION
0	CR0	Control Register 0
1	CR1	Control Register 1
2[2]	SR0	Status Register 0
3[2]	IR0	Interrupt Event Register
4[2]	SR1	Status Register 1
5[2]	SR2	Status Register 2
6[2]	CTR0	Counter Register 0
7[2]	NA	Next Address
8	TA	ACK Timer
9	TD	Net Dead Timer
A	CBPH	Control Block Pointer (MSB)
B	CBPL	Control Block Pointer (LSB)
C	NAR	Next Address, Request
D	AHOLT	Access Hold-off Limit
E	TXLT	Transmit Limit
F	MA	My Address

[1] = Hexadecimal representation of IA0-IA3.
[2] = CPU read only, write not possible.

Control, status, and interrupt bits will be referred to as CR, SR, or IR, respectively, along with two digits. For example, SR21 refers to status register #2 and bit 1, which is "STATE."

SUMMARY — CONTROL, STATUS, INTERRUPT REGISTERS

REGISTER	BIT # 7	6	5	4	3	2	1	0
CR0	TXDEN	TXEN	RXEN	ITOKON	ILOOP	COPY	NOINT	ISOL [1]
CR1[2] CR1[4]	DIAGC DIAGC	PIGT 0	INIT 0	ADRV ADRV	GIRING DMAT	0 LOOPT	TOFF RAMT	NEWNA NUDIAG
SR0	LASTF	SENDACK	L2	0	BSZ3	BSZ2	BSZ1	BSZ0
IR0 [3]	ITERR	IROR	INS	ITRAN	IREC	ITOK	ITA	ITD/M
SR1	TAOUT	$\overline{\text{IRTS}}$	RECIDL	1	1	1	1	1
SR2	NXTT0	NXTR0	TR	ACKRQ	RETRY	TSENT	STATE	INRING
NOTE: ZERO BITS (0) SHOWN ABOVE ARE RESERVED AND SHOULD NOT BE USED.								

NOTES:

[1] = Set to 1 on power-up or master reset.

[2] = Non diagnostic mode only (CR17-DIAGC cleared).

[3] = Any bit set causes host interrupt ($\overline{\text{INTR}}$ goes true) when Master Interrupt Suppress (CR01) is clear. All bits are cleared when register is read by the host.

[4] = Diagnostic State only (CR17-DIAGC set). See diagnostic section for register usage in diagnostic mode.

CR0 — CONTROL REGISTER 0 DEFINITION

REGISTER	CR07	CR06	CR05	CR04	CR03	CR02	CR01	CR00
CR0	TXDEN	TXEN	RXEN	ITOKON	ILOOP	COPY	NOINT	ISOL

BIT	NAME	DESCRIPTION
CR00	ISOL	Isolate. Set true on power up or master reset. Host clears this bit after the host memory based WD2840 control block and other WD2840 registers have been set up. May be set by the host at any time (will be ignored if WD2840 is in diagnostic state). There is some delay for the WD2840 to respond to any state change request. A state change to network mode is acknowledged by the state confirmation status bit (SR21-STATE) being cleared. Setting ISOL while the WD2840 is in Network State will cause a state change to Isolate State, confirmed by an interrupt event (IR00-ITM) and the STATE status bit (SR21) being set. This transaction will be delayed until the node does not possess the token. Any in-progress frame transmission will be completed normally (at the current frame, regardless of queue length), followed by a normal token pass sequence.
CR01	NOINT	Master Interrupt Suppress. When clear, the WD2840 will generate host interrupt requests ($\overline{\text{INTR}}$ low) if any bit in the WD2840 interrupt request register (IR0) is set. When set, only the interrupt request is suppressed, not the setting of bits in IR0. Note that any interrupt request will be dropped by the WD2840 when IR0 is read since this will clear IR0.
CR02	COPY	Enables COPY mode. When set causes all received data frames to be accepted and DMA'ed into memory regardless of destination address. (See description in Diagnostics Section.)
CR03	ILOOP	Instructs the WD2840 to loop data internally from transmitter to receiver. Used with the LOOP diagnostic. Must NOT be set while in network mode (CR00-ISOL clear).
CR04	ITOKON	Enable Token received interrupts. When clear no Token received interrupts are generated. When set the WD2840 generates an Itok interrupt when a token is received.

BIT	NAME	DESCRIPTION
CR05	RXEN	Receive Data Enable. When clear, the WD2840 still makes normal responses to supervisory frames (scan, token pass), but will not DMA any data frames into memory and ignores the receiver buffer chain. However any data frame which is addressed to this node and for which an ACK is requested, will be NAK'ed with a "receiver not enable" Nak code. When RXEN is set, it allows the receiver to DMA appropriate data frames into memory. RXEN may be arbitrarily set and reset while in Network State but changes will not affect any frames in progress. NOTE: Even when RXEN is clear, the WD2840 is "following" the receiver buffer chain with an internal register pointing either to the next available buffer (NXTR0 set) or, if the chain is exhausted, to a link field of zero (NXTR0 clear). The constraints on host manipulation of the receiver buffer chain are the same regardless of the state of RXEN. See the subsequent section on Receiver Memory Interface for more details.
CR06	TXEN	Master Transmit Enable. When clear no transmissions will occur and the transmit buffer chain will be ignored. When set, transmission activity is further dependent upon TXDEN (CR07). NOTE: Even when TXEN is clear, the WD2840 is "following" the transmitter buffer chain with an internal register pointing either to the next frame to transmit (NXTT0 set) or, if the chain is exhausted, to a link field of zero (NXTT0 clear). The constraints on host manipulation of the transmitter buffer chain are the same regardless of the state of TXEN. See the subsequent section on Transmitter Memory Interface for more details.
CR07	TXDEN	Data Transmit Enable. Has no meaning unless TXEN is set. When set in conjunction with TXEN, normal WD2840 transmission of data and supervisory frames will occur. When clear and with TXEN set, only data frame transmission will be suppressed. That is, token pass and Ack/Nak supervisory frames will still be transmitted when appropriate. NOTE: The note above for TXEN applies.

CR1 — CONTROL REGISTER 1 DEFINITION

REGISTER	CR17	CR16	CR15	CR14	CR13	CR12	CR11	CR10
CR1	DIAGC	PIGT	INIT	ADRV	GIRING	0	TOFF	NEWNA
CR1	DIAGC	0	0	ADRV	DMAT	LOOPT	RAMT	NUDIAG

BIT	NAME	DESCRIPTION (CR17 = 0, Network mode)
CR10	NEWNA	Update NA register. When set causes WD2840 to copy the contents of register NAR into register NA. The WD2840 clears this bit after the function is complete. This mechanism allows the host to define the WD2840's successor in the logical ring. The node's next token pass will be to the new NA node. NOTE: The normal token pass recovery applies. If the token pass to the new NA is not successful, a normal scan sequence will occur where the WD2840 attempts a single token pass to each node address in numerical sequence until a successful pass occurs or the node's address itself is reached.
CR11	TOFF	When set causes WD2840 to ignore timers. (This is NOT intended to be used in an operational network, but is provided to support network diagnosis.) CAUTION: This control bit disables all automatic network error recovery.
CR12	—	(Not used, Reserved.)
CR13	GIRING	Get in logical ring. Instructs the WD2840 to gain entry into the logical ring at the next opportunity (i.e. respond to a token pass). The INRING status bit (SR20) is confirmation; when INRING is set, it indicates that the WD2840 is participating in a logical ring of at least two nodes. If the host clears GIRING while INRING is set, the WD2840 will not accept the next token pass to it at which time INRING will be cleared as confirmation.

BIT	NAME	DESCRIPTION (CR17 = 0, Network mode)
CR14	ADRV	Address Driver Enable. Enables the sixteen output address (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{\text{DACK}}$ goes low. If ADRV = 1, the outputs are always TTL levels.
CR15	INIT	Network Initialization Enable. When clear, the WD2840 will not attempt to (re)initialize the network if the net dead timer (TD) expires. When set, TD timer expiration causes the WD2840 to enter Scan Mode. In this mode it transmits a token pass frame to each node numerically higher in address, one after another, until either network activity occurs (another node responds) or until the node's own address is reached. When Scan Mode begins, the first node address used is the then current NA (Next Address) node address. This value is derived from and is affected by the following actions: 1. At transition into Network State it defaults to MA + 1. 2. It may be set by the host using the NAR register and the NEWNA (CR10) control flag. 3. Upon receipt of a Scan Mode frame, NA is redefined to MA + 1. The successful initialization of the network by Scan Mode causes NA to be defined as the first responding node (hence, this node's successor). All node address computations are ascending and circular within the valid node address range of 1-254. NOTE: Since this network initialization activity comes about because of a timer expiration, TOFF (CR11) must be clear.
CR16	PIGT	If set, instructs WD2840 to piggy back token on last data frame transmitted. This request is honored if the last frame is determined as a result of limit TXLT or the LAST bit set in the TX-FCB, but not if transmission ends due to the reaching of the end of the chain.
CR17	DIAGC	Enables diagnostic mode. In network mode this bit must be zero.

CR1 — CONTROL REGISTER 1 DEFINITIONS

BIT	NAME	DESCRIPTION (CR17 = 1, Diagnostic mode)
CR10	NUDIAG	Perform a new diagnostic. When set causes WD2840 to perform the selected diagnostics. The host initializes the appropriate registers for the particular diagnostic and by setting this bit can initiate the test. The WD2840 clears this bit after completion of the diagnostic.
CR11	RAMT	Selects internal RAM test if in diagnostic mode.
CR12	LOOPT	Selects Loop Test if in diagnostic mode.
CR13	DMAT	Selects DMA Test if in diagnostic mode.
CR14	ADRV	Address Driver Enable. Enables the sixteen output address (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{\text{DACK}}$ goes low. If ADRV = 1, the outputs are always TTL levels.
CR15	—	(Not used, Reserved.)
CR16	—	(Not used, Reserved.)
CR17	DIAGC	Enables diagnostic mode. Confirmation of diagnostic mode is via status bit STATE (SR21). When DIAGC and STATE are both set, diagnostic functions of CR1 apply. When DIAGC is cleared, after the selected set of diagnostics in progress complete, the WD2840 will transition to the Isolate state. This transition will cause an interrupt event (ITM).

SR0 — STATUS REGISTER 0 DEFINITION

REGISTER	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
SR0	LASTF	SENDACK	L2	0	BSZ3	BSZ2	BSZ1	BSZ0

BIT	NAME	DESCRIPTION
SR00 .. .. SR03	BSIZ	BSIZ0 — BSIZ3 Buffer size, defines the buffer size in multiples of 64 bytes (the value ranges from 0 to 15_H. Corresponding to a buffer size of 64 to 1024 bytes in 64 byte increments). This value is used internally to define buffer boundaries to allow the chip to link buffers. A maximum of 16 buffers may be used for a single frame.
SR04	—	Not used.
SR05	L2	An internal flag set during frame transmission if the length value of the current frame is equal to eight. For normal data frame transmission this means the frame has no data field and for transparent frame transmission this means the frame is an access control frame. (SCAN FRAME)
SR06	SENDACK	An internal flag set during data frame reception to indicate that the incoming frame should be acknowledged (send ack/nak frame). This flag is cleared when the acknowledgement has been transmitted.
SR07	LASTF	An internal flag set during data frame transmission to indicate that the current frame will be the last to be transmitted with this token. Five situations can cause this to occur: 1) ISOL (CR00) becoming set, 2) TXDEN (CR07) becomes clear, 3) current frame flagged (via FCB) to be "last frame," 4) the current token frame count reaching the TXLT limit, 5) transmitter under-run detection. Note in particular that the last frame in the transmit queue will not cause LASTF to set since it's being last is not known until frame end. Also if a piggy-back token is permitted (CR16 set) and no acknowledge is requested (via FCXB), the token will be piggybacked on the current (last) data frame. LASTF is not cleared until the next data frame transmission begins.

IR0 — INTERRUPT REGISTER DEFINITION

REGISTER	IR07	IR06	IR05	IR04	IR03	IR02	IR01	IR00
IR0	ITERR	IROR	INS	ITRAN	IREC	ITOK	ITA	ITD/M

The setting of any bit in this register by the WD2840 causes an interrupt request ($\overline{INTR}$ = low) if NOINT (CR01) is clear. The reading of this register by the host clears all bits (and any interrupt request).

BIT	NAME	DESCRIPTION (1)
IR00	ITD/M	Network dead or mode change (dual use). When in Network mode, timer TD expiring (with TOFF clear) causes this bit to be set to indicate no network activity has occurred within the timeout period. Also INRING (SR20) is cleared and, if INIT (CR15) is set, the WD2840 will enter Scan Mode (see INIT - CR15 for details). Transition from Network or Diagnostic State to the Isolate State will be confirmed by this interrupt. The choice between the ITD and ITM interpretations is easily made based on the ISOL (CR00) bit.
IR01	ITA	Date Frame Transmission Unsuccessful. This interrupt indicates that a transmitted data frame with an acknowledge request was not successfully acknowledged. Either a NAK or no response after two transmissions will cause this. The exact cause can be determined by inspecting the appropriate FSB.
IR02	ITOK	The token has been received.

BIT	NAME	DESCRIPTION (1)
IR03	IREC	Data Frame Received. This interrupt signifies that a good data frame has been properly received and DMA'ed into the buffer chain. Frames that have been received can be identified by following the buffer chain noting the WD2840 frame status bytes (FSB). A non-zero FSB (host must clear when queuing free buffers) indicates a properly received frame. The host may freely remove all received frames from the chain up to but NOT necessarily including the last one posted. The last one posted may only be removed if the WD2840 NXTR0 (SR26) is set. For more details see the explanation for NXTR0.
IR04	ITRAN	Indicates that at least one data frame has been transmitted. The number of frames transmitted and the status of each (i.e. ACK/NAK, retry count) is determined by following the transmit chain and inspecting frame status bytes (FSB). All transmitted frames up to but NOT including the last posted may be freely removed. The last one posted may only be removed if the WD2840 NXTT0 (SR27) is set. For more details see the explanation for NXTT0.
IR05	INS	New successor. The WD2840 has identified a new successor in the logical ring. This happens when the prior successor either failed to respond to a token pass or as instigated by a network scan frame.
IR06	IROR	Receiver over-run. The WD2840 ran out of buffers or access to the DMA channel was delayed by the host so long as to cause loss of received data.
IR07	ITERR	Transmitter error. Three abnormal frame transmission cases can cause the ITERR interrupt. The causes are "transmitter underrun," "premature end of chain," and "exceeded 16 buffers." The frame transmission will repeat once per token until the host removes the WD2840 from the network, or the cause of the error is fixed.

(1) = Non diagnostic mode only. See diagnostic section for register usage for diagnostics.

SR1 — STATUS REGISTER 1 DEFINITION

REGISTER	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR00
SR1	TAOUT	$\overline{\text{IRTS}}$	RECIDL	1	1	1	1	1

BIT	NAME	DESCRIPTION
SR10 :: SR14	—	(Not used, reserved.)
SR15	RECIDL	Receiver Idle. Indicates the WD2840 has received at least 15 contiguous ones.
SR16	$\overline{\text{IRTS}}$	Internal Request To Send. Indicates the transmitter is attempting (successful or not) to send either data or flags. If the $\overline{\text{RTS}}$ pin is not tied to ground or WIRE-OR'ED with another signal, then $\overline{\text{IRTS}}$ = $\overline{\text{RTS}}$.
SR17	TAOUT	Timer TA expired.

SR2 — STATUS REGISTER 2 DEFINITION

REGISTER	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20
SR2	NXTTO	NXTRO	TR	ACKRQ	RETRY	TSENT	STATE	INRING

BIT	NAME	DESCRIPTION
SR20	INRING	In logical ring. Indicates the node has had the token and has successfully passed it at least once (therefore it is included in a logical ring of at least two nodes). See GIRING (CR13) for other comments.
SR21	STATE	Mode confirmation. Depending on DIAGC (CR17), the WD2840 is either in Isolate or Diagnostic state. When ISOL (CR00) is set, STATE set confirms the WD2840 is not in Network State. When ISOL is clear, STATE clear confirms Network State. Note any state transition into Isolate State causes an interrupt event to occur (ITM).
SR22	TSENT	An internal flag. TSENT is set when the WD2840 passes the token. It may have been either a piggyback or explicit token pass frame. TSENT is cleared when the next frame is received.
SR23	RETRY	An internal flag which is set when either a data frame or a token pass frame must be retransmitted. Data frames are only retransmitted if they have an acknowledge request and no response at all occurred. Token pass frames (except Scan) are retransmitted if no network activity was detected. Both of these situations are detected as a result of a TA timeout.
SR24	ACKRQ	An internal flag set during data frame transmission if an acknowledgement is requested for the specific frame. If this is the case, the WD2840 pauses to await the ACK/NAK response frame; if the TA timer expires before the response, a single retry will occur (see RETRY-SR23). ACKRQ is not cleared until the beginning of the next data frame transmission.
SR25	TR	An internal flag set when the WD2840 receives a token passed to it. It is cleared when the token is passed (or if it is ignored for any reason. For example, piggyback token on a bad data frame, TXEN clear, or detection of duplicate tokens in the logical ring).
SR26	NXTR0	Internal Receive Buffer Pointer State. Because of the linked list approach used in the buffer chains, the WD2840 internal register used to follow the list is either pointing to the next buffer in the chain or at the address of the next buffer in the chain (prior buffer's link field). The WD2840 will always advance along the chain so that it has the address of the next buffer to be used. However, when a zero link is encountered, the WD2840 retains the link field address expecting eventually that the chain will be extended by the host making the link some non-zero value. When the WD2840 actually needs the next buffer, it looks again at the contents of the link field expecting it to have been changed (chain extended) to the address of an available buffer. The NXTR0 bit differentiates between these two situations. When set it indicates the WD2840 has the address of the next buffer and that all prior frames (denoted by posted FSB's) can be removed from the chain for received frame processing by the host. When NXTR0 is clear it indicates that the WD2840 has advanced to a zero link (end of chain). NOTE: In this situation, the last posted frame CANNOT be removed from the chain for processing since it is the link field of his last buffer that must be set in order to extend the receiver buffer chain.
SR27	NXTT0	Internal Transmit Buffer Pointer State. The comments for NXTR0 (SR26) apply (in an analogous manner) to NXTT0 since the transmit buffer chain is handled by the WD2840 using an identical scheme. When NXTT0 is set it indicates that the WD2840 has the address of the next frame to transmit in its internal register. However when clear, it indicates that the transmit chain internal register points to the link field of the last buffer of the last transmitted frame. This link field contained zero when first read. For the transmit case, this is a normal situation corresponding to no data frames to transmit. NOTE: As in the receive case, when NXTT0 is set, all previously transmitted frames (denoted by posted FSB's) can be removed from the chain for reuse. However, when NXTT0 is clear it indicates that the transmit chain must be extended by the host before removing the very last frame that has been transmitted (posted).

OTHER REGISTER DEFINITIONS

NAME	DESCRIPTION
CTR0	Running Limit Counter. Used by the WD2840 for Access Hold-Off Limit (AHOLT) checking and Transmit Limit (TXLT) checking. When transmitting data frames CTR0 is used for TXLT counting; otherwise it is used for AHOLT counting. The counter runs from zero to the 8-bit limit value.
NA	Next Address. This register shows the current (instantaneous) successor node in the network logical ring. For validity, the WD2840 should be "in the ring" (see GIRING - CR13 and INRING - SR20 for more details). The successor node may be changed for a variety of reasons: 1. Any attempted token pass that fails twice will cause the WD2840 to attempt to locate a new successor by sequentially trying token passes to successively higher node addresses beginning with NA + 1. 2. A received Scan frame will cause NA to be set to MA$ 1. If the next token pass fails case 1 applies. 3. The host may arbitrarily redefine NA by using the NAR register and the NEWNA (CR10) control bit. At a convenient point the WD2840 recognizes NEWNA, copies NAR into NA, then clears NEWNA as confirmation. If the next token pass fails case 1 applies.
TA	Acknowledgement Timer. Value of maximum allowed time between frame transmission and ACK/NAK (if requested), or between token sent and network activity. The delay is in increments of 64 times the period of the clock CLK. Thus, if CLK = 2 MHz, then TA may be set in increments of 32 microseconds (range of 32 μs to 8.2 ms).
TD	Network Dead Timer. Value of maximum time interval between received valid frames on the network. 32X range of TA.
CBP (H,L)	Control Block Pointer. A sixteen bit pointer to the WD2840 control block in the user's memory. Must not be modified while the WD2840 is in network mode.
NAR	Next Address, Request. Used in conjunction with the NEWNA (CR10) control bit to cause the WD2840 to update the NA register. This redefines the node's successor in the network logical ring. It MUST be an address in the range 1-254. The acceptance of this update is confirmed when the NEWNA control bit is cleared. On the next token pass, if the redefined successor fails to accept the token, this WD2840 enters Scan mode where it sequentially attempts a token pass to successively higher nodes.
AHOLT	Access Hold-off Limit. This register is set at a value indicating the number of access cycles (tokens received) that must be skipped before the data frame may be transmitted. (A token pass frame will be sent even if a data frame may not be sent at a given access cycle.) Initialized to zero at power up.
TXLT	Transmit Limit. This register is set at the maximum number of consecutive data frames the WD2840 may transmit during one access cycle. A value of zero allows the WD2840 to transmit all frames queued up to 256. Initialized to zero at power up.
MA	My Address. The WD2840 receives only frames with this destination address (along with the broadcast address) and inserts this address into the SA field of any transmitted frame. Must be set by the host (range is 1 to 254).

1.4 DIAGNOSTIC AIDS

There are three levels of diagnostics supported by the WD2840; those that are associated with the network as a whole, those associated with the individual node, and those that are limited to the WD2840 as a device. These tests are Network Diagnostics, System Diagnostics and Self Diagnostics respectively. The Network Diagnostics can be performed while the WD2840 is in the logical ring, but the System Diagnostics and the Self Diagnostics may be used only while the WD2840 is in the diagnostic mode.

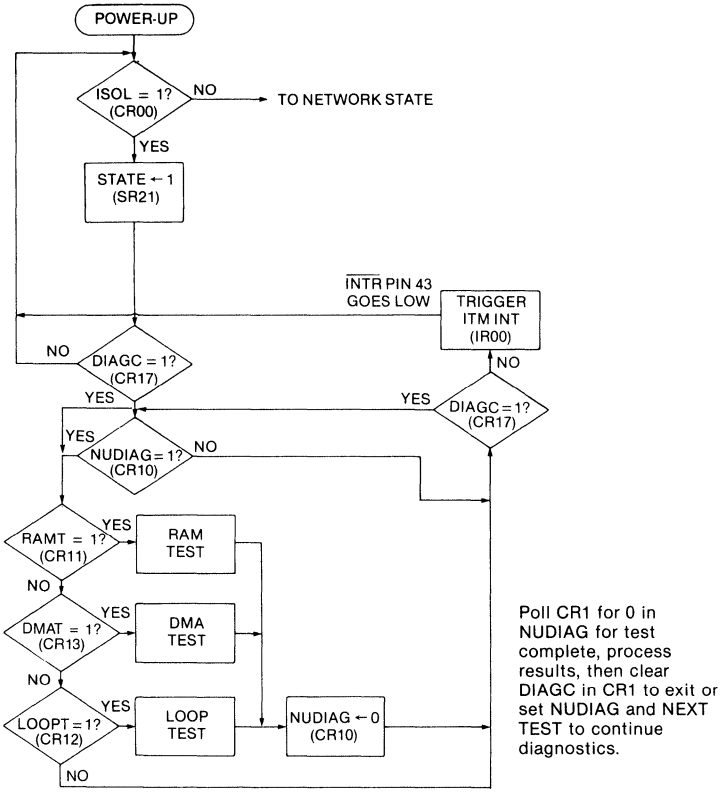
DIAGNOSTIC MODE CONTROL			
CR00 ISOL	CR17 DIAGC	SR21 STATE	DEFINITION
1	0	0	WD2840 "Isolated." Power-up condition or isolate request.
0	0	0	WD2840 active.
1	0	1	Isolate request function confirmed.
1	1	0	Host request to enter diagnostic mode.
1	1	1	Diagnostic mode confirmed. Diagnostic functions of CR1 apply.
0	0	1	Illegal.
0	1	0	Illegal.
0	1	1	Illegal.

Diagnostic mode may be entered after power-up or from the network mode by manipulation of the mode control bits. The mode transition is confirmed by the WD2840 via the STATE status bit.

Once in diagnostic mode, the desired test is selected via CR1. Because most of registers 8 through F are interpreted differently for each test, only one of the diagnostic test bits should be set at a time. In conjunction with setting the diagnostic bits, the NUDIAG (CR10) bit must be set to perform the diagnostic test requested.

At the completion of the selected test NUDIAG is cleared by the WD2840. Therefore the host can initiate a diagnostic by entering the diagnostic mode, initializing the proper registers, setting the desired diagnostic bit, and setting NUDIAG. The host then moniters CR1 for NUDIAG going to zero, indicating the completion of the requested diagnostic.

DIAGNOSTIC STATE FLOW CHART



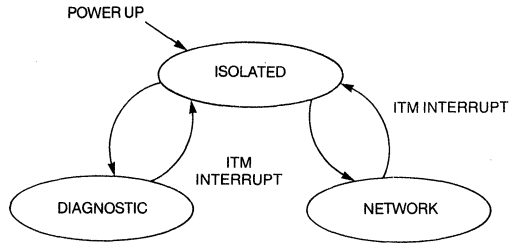


Figure 1.3 FUNCTIONAL STATES

1.4.1 SELF DIAGNOSTICS

Internal Ram and Interrupt Test

There are nine eight bit registers in the WD2840 which are not directly accessable by the users CPU. This test provides a means to check those registers and the interrupt register. The contents of register A are placed into the interrupt register and five even internal registers, and the contents of register B in four odd internal registers. The nine registers are then added together without carry and the result is placed in registers 2, 5, 6, 7.

Use the following procedure to initiate the RAM test:

1. Enter diagnostic mode.
2. Set up registers A and B
3. Set RAMT.
4. Set NUDIAG (can be set with RAMT bit together).
5. Wait for NUDIAG to be cleared.
6. Read registers 2, 5, 6, 7. Clear RAMT.

Note that the setting of any bit in the interrupt register while NOINT is clear will generate a hardware interrupt ($\overline{INTR}$, pin 43 goes true).

1.4.2 SYSTEM DIAGNOSTICS

DMA Test

This test verifies proper operation of the DMA subsystem by reading the value from a register and writing it into the user memory. The test continues by reading the value from the same location in memory and writing it into another register.

The value is read from register C. Using the transmitter DMA sub-system, it is written into memory location addressed by register A and B (location N; register A is the MSB). The receiver DMA sub-system is used and contents of the same address is read and it is stored into the register 7. Next the receiver dma is used and the contents from register D is written into location N + 1. The transmitter dma reads the value from location N + 1 and stores it into register 6.

It is the host's responsibility to check if the contents of registers C and register 7 and memory location N match. The same is true for registers D and 6 and memory location N + 1.

Loop-Back Test

The host can test the WD2840 transmitter and receiver logic by using the Loop Test.

There are two Loop Tests available for diagnostic purposes — internal and external.

(CR12) LOOPT	(CR03) 1LOOP	DEFINITION
0	0	Not in Loop Test
0	1	Do not use in network mode
1	0	External loop
1	1	Internal loop

When using the external loop the interface or modem must have the necessary logic to tie TD to RD and $\overline{TC}$ to $\overline{RC}$.

Use the following procedure to run the loop test.

1. Set up a 256 byte transmit buffer with the data pattern to be transmitted.
2. Initialize a 256 byte receive buffer with all "00s" or "FFs."
3. Load register A (MSB) and B (LSB) with the address of the transmit buffer.
4. Load register C (MSB) and D (LSB) with the address of the receive buffer.
5. Load register 0 for Internal or External Loop.
6. Load register 1 for diagnostic & loop. (85_H)
7. Refer to Diagnostic State Flow Chart.

NOTE:
If this test frame is allowed onto the network, transmission collisions may occur. Further, the first three bytes of the transmit buffers will be interpreted as TC, DA and SA, respectively, by the other stations. Therefore in case this test is initiated while this node is in the logical ring, care should be taken for choosing these three values for external loop-back test.

For proper operation of the internal loop-back test the $\overline{CTS}$ and $\overline{SQ}$ pins of the WD2840 should be either tied to ground or tied to $\overline{RTS}$ pin of the WD2840.

1.4.3 NETWORK DIAGNOSTICS

Duplicate Station Detection

Duplicate stations (more than one station with the same address) can result from the faulty programming of internal register MA (due to wrong address switch settings on the user's device, for example). This is expected to occur often enough to warrant the addition of a detection algorithm in the users WD2840 initialization procedure.

After initialization, the user should place the WD2840 in the network mode with TXEN off and ITOKON on. This will cause the WD2840 to generate an ITOK interrupt each time a token is passed to its address (MA). The host must provide the timeout algorithm which should be greater than the maximum time for the network to pass the token around the ring twice. Checking twice eliminates the possibility that the Network is in the scan mode and sending tokens to non-existing stations.

It is useful to note that this constraint requiring each node which is participating in the network logical ring to have a unique address does not extend to nodes which are "listening" but not "in the ring." It might be useful to a network designer to have groups of receive only nodes which have the same node address but do not participate in the network token passing (see GIRING - CR13). Data frames transmitted to such clusters must not request acknowledgement since all nodes in the cluster would simultaneously respond.

Copy Mode

The COPY Mode is selected by setting the COPY control bit (CR02). Normally the WD2840 receives (DMA's into the receive buffer chain) data frames only if they contain the general broadcast destination address or if they are specifically addressed to the WD2840. This occurs when the frame's destination address (DA) matches the WD2840 my address (MA, set by the host).

However, when COPY mode is selected data frames which are specifically addressed to other nodes will be treated as broadcast frames by this node. The COPY mode allows a specific node to "eavesdrop" on data frame traffic on the network.

Nak Response

The WD2840 sends negative acknowledgements (NAK's) on response to received frames under several circumstances. The NAK prevents the transmitting node from wasting bandwidth retrying indiscriminately, and further, lends visibility to individual network node problems. The NAK includes a reason code which is available to the transmitter's software (via the TFSB).

Each data frame to be transmitted can be specifically marked (via the FCB) by the host to require an ACK/NAK response from the receiving WD2840. In the absence of errors, an acknowledge (ACK) frame will be returned to the transmitter as confirmation. However, several circumstances cause a Negative Acknowledge (NAK) to be returned:

1. Insufficient buffer space
2. Receiver not enabled (RXEN - CR05 cleared)
3. Receiver overrun
4. Frame exceeded 16 buffers in length

This information is placed in the transmitted frames's FSB. See section 2.1.2 for more details on the Transmit Frame Status Byte (TFSB).

2.0 INTERFACES

There are two interfaces to the WD2840: the host computer side, and the network side. The network side is conventional from an electrical point of view, the WD2840 performs all logical functions required to ensure communications capability on broadcast media (such as coax or RF).

The host interface involves two separate functional interfaces: the status/control registers described in section one, and a DMA interface that is described in the following subsection.

2.1 HOST

The WD2840 uses a complex memory buffer architecture allowing it to respond in real time to its network obligations (e.g., to meet network data rate and processing delay requirements). These memory structures are managed cooperatively by the host and the WD2840.

Memory management functions requiring real time response (e.g., traversing chains) are completely handled by the WD2840. Other important, but not time critical operations are the responsibility of the host software (such as removing used buffers from the transmit chain).

All memory references by the WD2840 are pointed to by memory locations (and internal registers) initially defined and set up by the host software. Initial values and memory based registers are grouped together and called the WD2840 Control Block.

The location of this control block is written into the registers CBPH and CBPL anytime the WD2840 is in Isolate State. This control block has the following structure:

CBP→	+0	NXTR (H)	Receive Buffer Chain (MSByte)
	+1	NXTR (L)	Receive Buffer Chain (LSByte)
	+2	NXTT (H)	Transmit Buffer Chain (MSByte)
	+3	NXTT (L)	Transmit Buffer Chain (LSByte)
	+4	BSIZE	Buffer Size / 16 (0-F = 64-1024 bytes)
	+5	EVT0	
	+6	EVT1	Eleven separate Event Counters, see section 2.1.1 for details
	....		
	+F	EVT10	

As the WD2840 transitions to Network State, it reads and uses the first five bytes of the control block. The remaining eleven bytes of event counters are accessed by the WD2840 only when each specific event condition occurs.

Either the Receive (NXTR) or Transmit (NXTT) chain entries in the control block may initially be zero; in such a case the WD2840 expects the chain to be extended by the host's changing the zero link field in the control block. Thereafter any such zero link would be in a buffer.

The WD2840 uses constant size buffers; their length is set by the value in location BSIZE. The buffer size is indicated by a 4-bit count in the least significant 4 bits of the BSIZE byte in the WD2840 control block. The buffer sizes available are multiples of 64; (BSIZE + 1) 64 is the buffer size used by the WD2840. Thus a BSIZE range of 0-15 corresponds to actual buffer sizes of 64 through 1024 bytes. This buffer length is inclusive of control bytes and buffer link pointers.

The WD2840 includes a chained-block feature which allows the user more efficient use of memory, particularly in situations where the maximum packet size is much larger than the average packet size. One or up to 16 buffers may make up a frame but a buffer may not contain more than one frame.

Byte counters are associated with each frame (at the memory interface, not actually transmitted within the frame) so that frames on the network need not be integer multiples of buffers. The byte counters include all buffer management overhead. Therefore, a frame consisting of 100 transmitted data bytes, occupying two 64-byte buffers, would have a byte count of 110 (six bytes per frame + 2 bytes per buffer).

Since the WD2840 receive and transmit buffer chains are linked lists (see section 2.1.2 and 2.1.3) and are "followed" by the WD2840 but managed by the host; it is expected that the host will maintain both a FIRST and a LAST address for each chain. On transition into Network State, the chain origin information in the WD2840 control block is the same as FIRST. In fact, since the WD2840 does not change these control block entries, they can be maintained directly as FIRST by the host. An explicit LAST could be placed in an extended control block section.

The WD2840 "follows" the linked buffer chains by maintaining a NEXT address internally for each chain. This NEXT address can be in one of two states: 1) it can be the address of the next buffer in the chain, or 2) at the chain end (zero link), it can be the address of the buffer containing the zero link. The WD2840 uses a status bit for each chain, NXTR0 (receive) and NXTT0 (transmit), to differentiate the two states. When set they indicate the WD2840 chain NEXT address is in state 1 above; when clear they indicate state 2 above. This is an important distinction since it indicates whether the last buffer posted in a chain can be removed by the host (because the WD2840 has advanced to the buffer beyond) or must be left until the chain can be extended so the WD2840 can advance.

The host software monitors the progress of the NEXT pointer, and updates FIRST and LAST as it adds (and removes) buffers to (from) the chains as required. The WD2840 provides Interrupt Events (see IR0) and NXTR0, NXTT0 status bits to indicate when it advances along the two chains and exactly what state its NEXT address registers are in. The operation of these chains will be explained by example in later sections.

"Deadly Embrace" Prevention

A "Deadly Embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the WD2840. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the WD2840 and should also be obeyed by the user's CPU. This rule applies to the WD2840 memory registers and to the I/O registers. The Event Counters are an exception to this rule.

Rule:
If a bit is set by the CPU, it will not be set by the WD2840, and vice versa. If a bit is cleared by the WD2840, it will not be cleared by the CPU, and vice versa.

As an example, the NEWNA (CR10) control bit is only set by the host and is only cleared by the WD2840.

Dual DMA

The WD2840 may, for efficiency, interleave frame data fetch/store operations with fetches and stores of pointers and flags in memory. In all cases, operation sequencing is such as to prevent deadlocks and ambiguities between the WD2840 and software.

2.1.1 EVENT COUNTERS

Several non-fatal logical events are tabulated by the WD2840 and made visible to the host via memory based event counters (see WD2840 control block organization for specific locations). The WD2840 will increment each counter at the occurance of the specified event. Note that the WD2840 will not increment past 255. The host has the responsibility of initializing each counter.

COUNTER	DESCRIPTION
EVT0	"Set scan mode" frame received from the network. The NA register was redefined to MA + 1 at the time.
EVT1	Transmission error first attempt, second try successful. Can only occur for frames requiring an acknowledgement. It indicates no response was received for the first transmission; however, the second transmission was either ACK'ed or NAK'ed.
EVT2	Transmission error. Attempt aborted due to either transmitter underrun or frame length exceeding 16 buffers.
EVT3	Timer TD (network dead) expired.
EVT4	Access Control Frame Reception Error. A one or two byte supervisory frame (ACK/NAK, Token Pass, Scan Mode) has been received in error. This may be due to an FCS error, frame abort, or carrier loss detection.
EVT5	Data Frame Reception Error. An incoming data frame was incorrectly received due to an FCS error, frame abort, carrier loss detection, or receiving a data frame when expecting an ACK/NAK frame.
EVT6	NAK sent. Can occur for any of the following reasons: 1. Insufficient buffers in chain 2. Receiver not enabled (RXEN clear) 3. Receiver overrun 4. Frame length exceeded 16 buffers
EVT7	Invalid frame received. Caused by the detection of certain abnormal network conditions such as receiving an ACK/NAK frame when not expecting one, receiving a Scan mode frame when expecting an ACK/NAK frame, or receiving an invalid supervisory frame.
EVT8	Duplicate token detected. This counter will be incremented when the WD2840 determines that more than one token exists in the logical ring. This happens if a token pass is received when the WD2840 already has the token, or a data frame is received when the WD2840 is waiting for an acknowledgement frame.
EVT9	Not used.
EVT10	Duplicate node address. This counter will be incremented when a data frame being DMA'd into memory has a source address (SA) equal to the WD2840 node address (MA). This counter when used with COPY mode (CR02) is one way for detecting other nodes with the same node number (MA).

2.1.2 TRANSMIT MEMORY INTERFACE

When the token is received, data transmission is enabled (TXEN - CR06 and TXDEN - CR07 both set), and if the access hold-off counter has reached its limit, the WD2840 will determine whether any data frames are pending in the transmit chain. If so, it will transmit the first data frame in the chain. Otherwise the token will be passed. A given data frame will be the last frame transmitted for this token if any of several conditions occur:

1. ISOL (CR00) is set indicating the host has requested a transition to Isolate State.
2. TXDEN (CR07) is clear indicating the host has changed data frame transmission rights.
3. The frame FSB indicates this frame should be the last transmitted for this token.
4. The running frame counter has reached its limit (TXLT).
5. No further frames are pending in the transmit chain.

If any of the first four reasons above are true a token pass will occur. If the last frame does not require an acknowledgement, the WD2840 will piggyback the token pass if that is permitted (CR16). If the token cannot be piggybacked or if the last frame transmitted is the last frame pending (condition #5 above), an explicit token pass will occur. A piggyback token will not occur for the last pending frame because, for the general multiple buffer case, it is not known to be the last pending frame until after the transmission is complete.

The WD2840 will read and evaluate the address of the next frame at two specific points in time:

1. At the end of the prior frame, even if the prior frame is the last to be transmitted for this token.
2. When the token is received and data frame transmission is permitted.

If a non-zero frame address is found at time 1 above, it is kept and used without being re-read at time 2 above. However, if no pending frame is found at time 1, this is noted with the NXTT0 flag clear and the chain re-inspected on each occurrence of time 2 above.

As frame transmission commences, the WD2840 reads the address of the next buffer, the frame control byte, (FCB) and the frame length. It then starts reading bytes from the buffer and sending them until the frame length count or the end of the buffer is reached. The new buffer is read and data transmitted as before. (See Figure 2.1)

The frame length provided in the LENGTH field must be the sum of the overhead bytes and number of data bytes (see Fig. 2.1).

Simplified formula for LENGTH:

LENGTH = # of data bytes + 2 link bytes per buffer + 6 overhead constants per frame.

Example #1

LENGTH = 8 (0010_H in LENGTH field)

implies one buffer is used for this frame (64 bytes) two link + six overhead, no data.

Example #2

LENGTH = # of data bytes + 2 link bytes per buffer + 6 overhead constants per frame.

Programmed buffer size = 64 bytes per buffer. Two buffers are used in this frame for a total of four link bytes (2 per buffer), six overhead, and 57 data bytes.

The General Formula for LENGTH

WHERE

N_D = # of data bytes (max 4095)

6 = Overhead Constant per frame (FSB, FCB, LENGTH (H), LENGTH (L), DA, SA)

B_K = B SIZE in bytes (64, 128, etc.) a constant preprogrammed into the WD2840 on 64 byte boundaries to a max of 1024 bytes.

GIVEN N_D

$$L = N_D + 8 + 2^* \text{ TRUNC } \frac{N_D + 5}{B_K - 2}$$

GIVEN L

$$\#B's = 1 + \text{TRUNC } \frac{L - 1}{B_K}$$

$$N_D = L - 6 - 2(\#B's)$$

NOTE:
The expression for N_D fails for values of $L = B_K + 1$. This is okay since the 2840 doesn't generate such values.

Examples: Find L given N_D

	N_D	L	
	0	8	
	1	9	1 bufr
	56	64	
$B_K = 64$	57	67	2 bufrs
	118	128	
	119	131	3 bufrs
	120	128	1 bufr
$B_K = 128$	121	131	2 bufrs
	246	256	
	247	259	3 bufrs

Find #B's, N_D given L

	L	#B's	N_D
	8	1	0
	9	1	1
$B_K = 64$	64	1	56
	67	2	57
	128	2	118
	131	3	119

	L	#B's	N_D
	128	1	120
	131	2	121
$B_K = 128$	256	2	246
	258*	3	246
	259	3	247

***NOTE:**
Case corresponds to buffer end and frame end on same byte . . . extra buffer consumed.

When the frame length is finally reached, the WD2840 pauses if an acknowledgement has been requested. The frame status byte (FSB) is updated when the frame is completed; its posting indicates frame completion and gives information about the success or failure of the frame transmission. At frame completion, the WD2840 attempts to advance along the transmission chain to identify the next frame regardless of whether it will be transmitted with this token or later.

The host may add frames to the end of the transmit chain at any time by changing the zero link in the last buffer. Also buffers of all posted frames up to but NOT including the last buffer of the most recently posted, may be arbitrarily removed from the chain. The last posted frame (more specifically, the last buffer of the last frame) may only be removed and reused if NXTT0 is set. This indicates that the WD2840 has advanced its NEXT address to the next frame but that its transmission has not been completed (in fact, perhaps not even started).

NOTE:
The WD2840 checks only the most significant byte of the link field for zero link detection. This has the following implications:

1. When writing into a zero link field, the host must write the LSB of the new link field first, followed by the corresponding MSB.

2. All buffers must have a starting address greater than or equal to Hex '0100'.

TRANSMIT FRAME STATUS BYTE (WRITTEN BY WD2840)

BIT #	7	6	5	4	3	2	1	0
Name	DONE	WIRING	X	X	SELF	VAL2	VAL1	VAL0

BIT	NAME	DESCRIPTION
7	DONE	Set to guarantee a non-zero value for the posted FSB.
6	WIRING	Value of the corresponding bit in received ACK frame.
5-4	—	Reserved.
3	SELF	When set, indicates the ACK/NAK code appears in the value field (bit 2-0) of this FSB is assigned by the WD2840 transmitter routine. When clear, indicates value resulted from ACK/NAK code from receiving station.
2-0	VAL	An encoded field whose interpretation depends upon the SELF flag (bit 3) in this FSB. a. SELF clear 0 0 0 — No receive error (= ACK when DONE is set). 0 0 1 — Insufficent buffers for frame. 0 1 0 — Receiver not enabled at frame start. 0 1 1 — Receiver over-run. 1 0 0 — Frame exceeded 16 receive buffers. b. SELF set 0 0 0 — No transmit error. 0 0 1 — Transmission failed after retry. 0 1 0 — Transmission under-run. 0 1 1 — Premature end of chain. 1 0 0 — Transmission frame exceeded 16 buffers.

Transmit Frame Status and Control Bytes

Each frame has two bytes reserved, one for host control information needed by the WD2840, the other for status information posted by the WD2840 at frame transmission completion. The frame control byte (FCB) is only read by the WD2840, never changed; the frame status byte (FSB), is written (posted) by the WD2840 with no regard for its prior contents. On completion, the FSB value will always be non-zero; it is important that the host zero the FSB byte in order to be able to recognize a posted frame.

NOTE:
Specifically note in Figure 2.1 that the first buffer of each frame has a different structure than any overflow buffers for that frame. In particular, each frame has only one set of FSB, FCB, and LENGTH fields regardless of the number of buffers required by the frame.

TRANSMIT FRAME CONTROL BYTE (WRITTEN BY HOST)

BIT #	7	6	5	4	3	2	1	0
Name	WACK	FCBLF	TRANSP	X	X	X	X	X

BIT	NAME	DESCRIPTION
7	WACK	Wait for Acknowledgement. Instructs the WD2840 to wait for an ACK/NAK response from the receiver for this particular frame only. The token control (TC) byte in the frame is automatically set to cause the destination node to respond. This bit must NOT be set if the frame uses the broadcast destination address. Inadvertently doing so will cause the frame to be posted "Transmission failed, due to max retries."
6	FCBLF	Last Frame. This bit will cause the WD2840 to pass the token either piggybacked with this frame (if possible) or explicitly after the frame transmission completes.
5	TRANSP	Transparent Frame. This bit will cause the WD2840 to interpret the buffer contents to be the exact sequence of bytes to be transmitted. The normal token control (TC) byte and source address (SA) byte generation is suppressed. Note that for a non-transparent data frame the TC byte must NOT appear in the buffer.
4-0	—	Reserved.

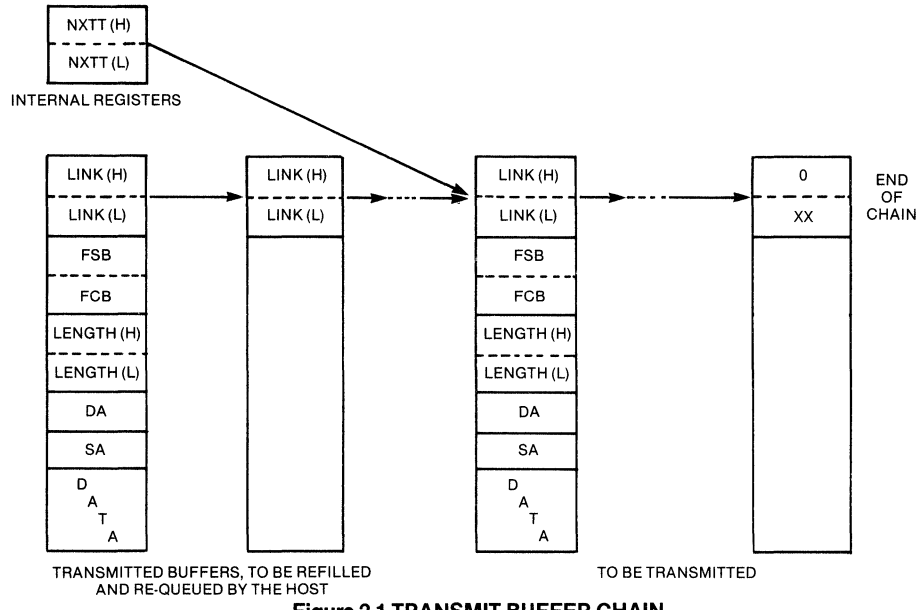


Figure 2.1 TRANSMIT BUFFER CHAIN

2.1.3 Receive Memory Interface

After the third byte of an incoming data frame is detected, the WD2840 will begin to place frame data into memory if several conditions are satisfied:

1. Receiver Enabled (RXEN-CR05 set).
2. There is an available buffer in the receive buffer chain.
3. The frame is addressed to this node specifically, it is a broadcast frame, or COPY mode has been selected by the host.

As the frame continues, it may completely fill its buffer. If this happens the WD2840 reads and inspects the link field of the current buffer. If this link is zero, an error occurs and the receive chain is reset to reuse from the first buffer used by the dropped frame. However, if another buffer is available, the incoming frame is continued beginning in the third byte of that buffer. This continues until one of several things happen:

1. Receiver overrun. The WD2840 has a four byte FIFO to buffer incoming frame data; however, if the host DMA responds too slowly a receiver overrun will occur. If this happens an event counter is incremented, the frame is dropped, and the receiver buffer chain is reset to reuse buffers of the dropped frame.
2. Current buffer capacity exhausted. If 16 buffers have been used for the current frame, an event occurs with the frame being dropped and the chain reset. Otherwise the WD2840 attempts to advance to the next buffer in the receiver buffer chain. The frame data will be continued in this subsequent buffer. If the end of the receiver buffer chain is reached an event counter is incremented, the frame is dropped, and the chain reset.
3. Frame ends. If the FCS is not correct an event counter is incremented, the frame is dropped, and the chain is reset. If correct however, the frame length is placed in the LENGTH field and the Frame Status Byte (FSB) is posted "done, no error."

If the frame is addressed to this node and indicates an acknowledgement is required (TC = 255), whether or not an error occurs, the WD2840 responds with an ACK/NAK supervisory frame indicating either success or failure. In case of receiver over-run, bad FCS, and SA = MA acknowledgement request will be ignored. (See section 1.4.3 for details)

It is the host's responsibility to ensure that buffers are available, initialized (FSB zero'ed), and attached to the end of the receive buffer chain.

RECEIVE FRAME STATUS BYTE (WRITTEN BY WD2840)

BIT #	7	6	5	4	3	2	1	0
Name	DONE	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
7	DONE	Set to indicate the frame reception is complete.
6-0	—	Reserved.

RECEIVE FRAME CONTROL BYTE (WRITTEN BY HOST)

BIT #	7	6	5	4	3	2	1	0
Name	X	X	X	X	X	X	X	X

BIT	NAME	DESCRIPTION
7-0	—	Reserved.

2.2 MODEM INTERFACE

The modem interface is the conventional half duplex NRZ type with separate data and clock (Figure 2.3). When the WD2840 desires to transmit, it asserts $\overline{RTS}$ and awaits $\overline{CTS}$. $\overline{RTS}$ is generally used to enable the modem transmitter. After a system dependent preamble is generated, the modem asserts $\overline{CTS}$ which allows the WD2840 to begin the actual transmission of the frame. (Note: $\overline{CTS}$ may be asserted permanently if the transmission system does not need to generate a preamble).

The $\overline{SQ}$ input is used on receive to indicate a valid carrier. If this term is negated anytime during a receive message, the WD2840 will presume the message is in error and treat it as an abort. This signal is used to augment message integrity beyond that of the CRC by allowing a modem to detect and report low level faults (such as out-of-frequency carrier or missing clock).

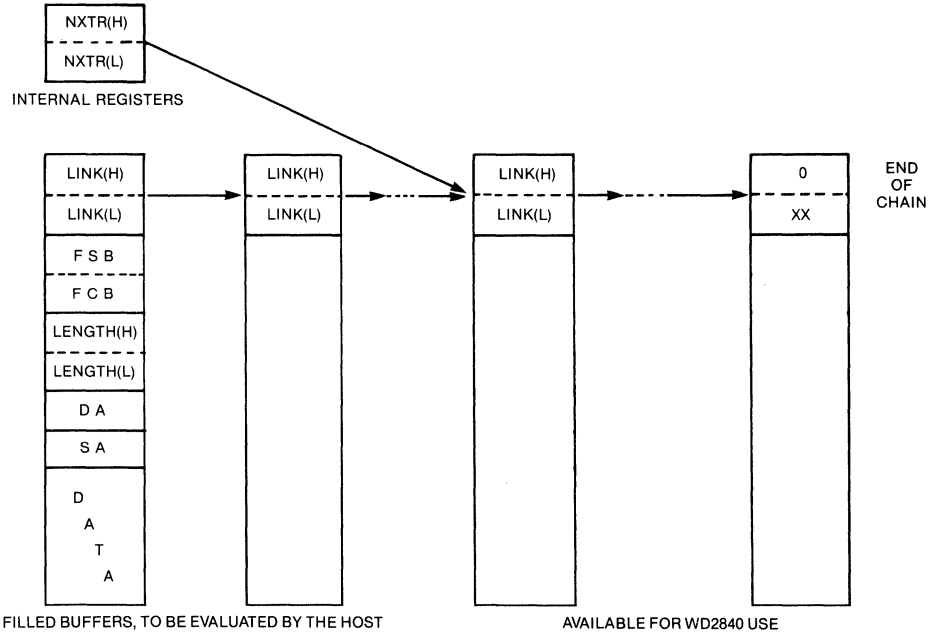


Figure 2.2 RECEIVE BUFFER CHAIN

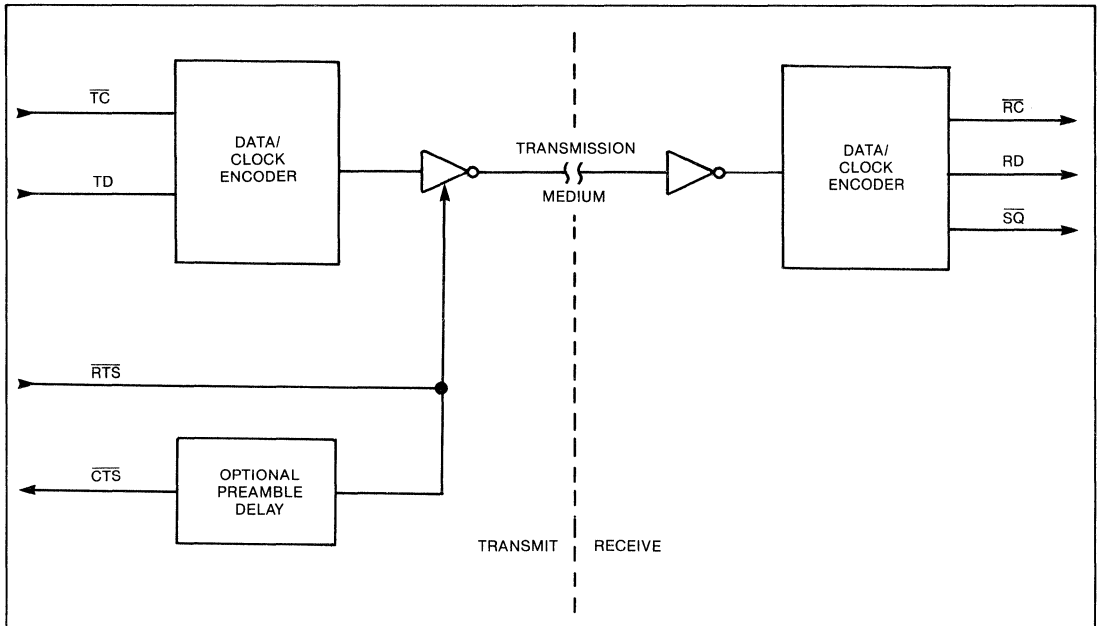


Figure 2.3 CONCEPTUAL MODEM

3.0 NETWORK PROTOCOL

To enable operation on a broadcast medium without the need for a central controller performing device polling, the WD2840 implements a media access protocol. The particular access protocol designed into the WD2840 prevents self-induced transmission collisions and ensures a fair and guaranteed distribution of transmission time among attached controllers. (See Appendix A for Protocol flowcharts.)

This design-out of collisions allows the WD2840 a greatly expanded selection of transmission media, since no physical characteristics of a particular medium are relied upon for proper network operation. Another benefit of this lack of collisions is the visibility of network faults. If a collision is detected, it is treated consistently in a error recovery mode by the WD2840 and is also unambiguously visible to service personnel as a fault.

Secondly, the WD2840 can ensure that a transmitted message was correctly received and buffered by requiring acknowledgement of its receipt. This is sometimes called "acknowledging datagrams" where the sender awaits a predefined period after a frame is sent for a reply from its destination. With this method, no sequence counters nor multi-frame retransmission buffering is required. The scheme is efficient since local network applications such as the WD2840 address do not encounter extremely long transmission delays (such as satellite links) as in conventional data networks (such as X.25).

Both functions are parameterized, allowing tuning and optimization by the user to his unique application. These parameters may be adjusted in real time by the user's software, allowing a dynamic network, responsive to constantly changing requirements.

The two functions, access control and data transmission, function simultaneously though independently. Thus they are described separately as subprotocols for clarity.

3.1 Data Transmission

The data transmission cycle is entered after the token has been received and data transmission rights validated (see section 3.2 "access method"). The WD2840 determines if there is a frame to be sent and, if not, simply sends the token to the next station.

If something is queued for transmit, the WD2840 DMA's it from memory and sends it. After the complete frame has been sent, the WACK (Wait for ACK) bit is tested in the TFSB (Transmit Frame Status Byte). If set, the WD2840 waits for, and expects, an acknowledgement from the frames recipient. A timer (TA) is started. In the normal case, the ACK is received before TA expires which causes the WD2840 to send the next frame queued, repeating this procedure. Thus, the WD2840 sends multiple frames to various destinations until the transmit queue is emptied or a programmed limit (register TXLT) is exceeded.

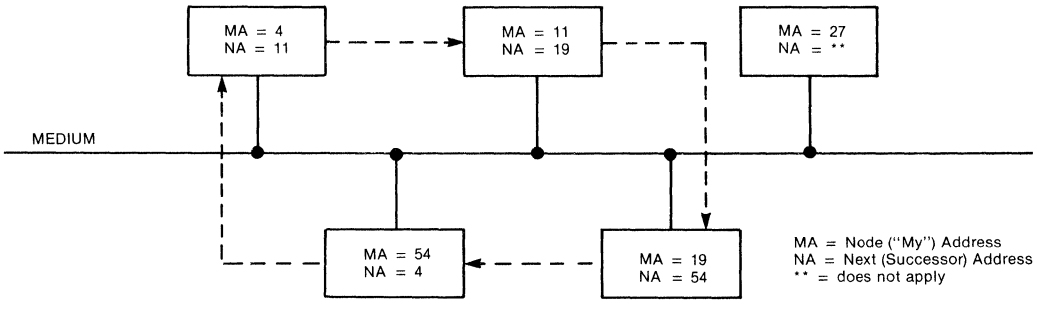


Figure 3.1 TOKEN PASSING ON A LOGICAL RING

In the event TA expires, the frame is re-transmitted once. (Note: it is the responsibility of higher level protocol operating in the host to protect against the possibility of duplicate frame reception.) If TA expires again, usually indicating the destination node is off-line, the FSB is updated to reflect the unsuccessful transmission, interrupt bit ITA is set, and the frame is skipped.

A frame is also skipped and tagged if the destination station sends a NAK, indicating it cannot presently process the frame.

TRANSMISSION OF ABORT

An ABORT is transmitted by the WD2840 to terminate a frame in such a manner that the receiving station will ignore the frame. An ABORT is sent when there is a Transmitter Under-Run. The abort sequence is a zero, followed by seven ones, after which RTS is set false.

3.2 ACCESS METHOD

The WD2840 network access method is based on the use of tokens, the specific granting of transmission rights passed from station to station. At any given time, exactly one station has the right to transmit (this right is called the token) and is obligated to pass it on when finished with it.

This can be clarified by referring to Figure 3.1. We assume in this figure that the network has already been initialized (meaning that the linkages in the access ring have already been established) and the token is held at this instant by station 4 (the station whose MA register = 4).

When station 4 is ready to pass his access right on, he sends a message to the station number called out in his internal register NA, in this case 11. The message, and thus the token, are received by station 11 who can now transmit its message(s). When station 11 is ready to pass the token, it sends a message to station 19, as directed by its internal register NA and the cycle continues, in a circular fashion, from station 4 to 11 to 19 to 54 to 4 . . .

Notice that the station numbers need not be contiguous. This relatively arbitrary station numbering (in the example) poses no inefficiency to the access method. The value of this is the ability to add and remove stations (re-configure) on the network without re-arranging everyone elses addresses. (See section 3.2.2 for an example).

In this way, the token is passed from one station to the next in a logical ring.

3.2.1 ACCESS INITIALIZATION/ERROR RECOVERY

When the WD2840 is commanded into Network State, the Next Address Request (NAR) register and the NEWNA (CR10) flag must be used to define the Next Address (NA) register. When it is necessary to pass the token, it is passed to the current node number in register NA. If station NA is not on-line, determined by its lack of response, station NA + 1 is tried. This process continues until a station is found

which does respond. The responding station number is written into register NA so that this scanning procedure need not be repeated on subsequent access cycles.

NOTE: 1. Node numbers 0 and 255 are reserved and cannot be used. Consequently scanning occurs circularly in the range 1-254.

2. During Scan mode token passing to each node is only tried once.

Anytime a station cannot successfully pass a token within two attempts, register NA is updated to NA + 1, and a new "next" station is searched for. The result is the removal of non-responding station(s) from the access ring. An interrupt (INS) is generated indicating a network exception caused a change to NA.

The above description covers network recovery from station failure and purposeful removal of stations during on-line network operation. Setting stations in the scan mode can also be accomplished by sending control frames (a Scan frame redefines NA = MA + 1) over the network. The control frame may be directed to a single station, or all stations simultaneously (using the broadcast address). It is this scanning for new stations that permits on line addition to the access ring.

NOTE:
The policy of the SCAN frame is redefined by the user software as required by the application. For example: in a process control environment where stations are not often added while the network is in use, this procedure would be initiated rarely if at all.

3.2.2 REMOVING A STATION

There are two ways a station can be removed from the access ring: non-response due to station failure and non-response due to host commanded transition to the Isolate State. Both are treated identically from a network point of view.

Referring to Figure 3.1, assume that station 19 is removed from the network (either physically or logically). In this example, station 11 would detect a network fault when trying to pass the token to 19 (time TA would expire since station 19 will not respond). Station 11 detects this and finds the next station in the access ring by using the "scan" function (similar to initialization). The next attempt at passing the token would be to station 20, register NA + 1.

By starting the token ring recovery procedure at the intended station plus one (station 20) rather than MA + 1 (station 12) as is done in initialization, recovery delays are minimized (since fewer stations are tested for presence, 8 less in this example).

The next station found would be number 54 in the example which station 11 writes into his register NA (now "patching out" dead station 19). The next time station 11 is finished with the token, it directly sends it to 54, making the sequence now 11 to 54 to 4 to 11 to 54...

3.2.3 ADDING STATIONS

There are three primary methods by which a station can be added to a network. The first is a distributed method, in which each station in the network can poll for new stations in the gap between its address and the next address (between MA and NA). Second is a centralized method, in which an individual station designated by the network architect can interrogate the entire address space seeking a new station desiring INRING. The third — central scan — is a simpler (from the host point of view), centralized method in which a station can send a global frame causing all the on-line TACs to reset their next address register. This causes each TAC to poll its address space at its next token-pass attempt. Each method has advantages and disadvantages.

Distributed Method

The distributed method does not rely on a specific station. Thus, there are no problems or efforts spent selecting the administrator, nor is there any concern about backup administrators. In the distributive method, each station has the same responsibility to allow new access members as other stations. This method is the most host intensive and requires each station to maintain a timer (that can be configuration set as to its value) as to how often it should poll its gap for new stations.

For example, assume the timer in each station is 5 sec. and that station 4's timer has expired (Fig. 3.2.3.1). The host attached to station 4 notes that the next address register (NA in the TAC) is set to 11, which indicates that a new station might be added to the network as station number 5, 6, 7, 8, 9, or 10.

The host queues a frame into the TAC transmit chain, polling station 5. This frame will be sent by 4 with an acknowledgement requested from 5. If 5 is present it responds; otherwise, the TAC aborts its attempt after time TA. The TAC marks the result on the frame in the host memory space and proceeds with other tasks.

After this exchange, the host, at its leisure, checks the transmit status of the frame. The host sees that the frame acknowledgement timed out, meaning that station 5 has not been added to the network, or that station 5 is on the network and whether the request INRING is set in the network code field. In either case, the host takes appropriate action. If the desired INRING bit is set, station 4 changes its NA register to 5, allowing its next token to be passed to 5. This action puts station 5 in the ring.

Depending on an application's sophistication, a control message can be sent to station 5. That message says, "Your successor is X." In this case, X = 11, so that 5 is not forced to poll for its successor. In any case, 4 updates its next address register to 5 and does not need to go through this distributive polling cycle again because there is no gap between 5's address and the next address; there is no possibility that a new station can be inserted between addresses 4 and 5. If 5 didn't respond to 4's poll, station 4 updates its poll counter so that the next time that the poll timer times out, station 6 will be tried.

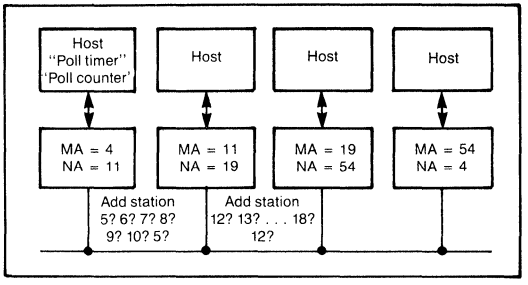


Fig. 3.2.3.1 Distributed polling. *Each host polls the gap in its address space for the possible addition of new stations. The host internal poll timer and poll counter set the polling rate and range as desired.*

If node 6 responds, its desired INRING bit is tested as above. If 6 does not respond, the host will queue a poll to station 7 the next time its poll timer expires. This continues until the host completes 10, when the cycle goes back to 5 and repeats. In this example, with a gap of 6 stations (between 4 and 11), and with a 5-sec. clock, a new node can be added within 30 sec.

In the centralized station-addition method, a single station can poll the entire address space, seeking a new station that desires INRING. One reason for centralizing this function might be the more careful control that can be placed in a network. There can also be optimizations. For example, the central polling station can keep track of the stations that already exist and, therefore, bypass some address ranges. A polling station may know the network will never have more than, say, 75 stations, In the example of Fig. 3.2.3.2, when station 4 starts polling, it polls only to address 75 before resetting to zero. This works like the distributed method except that a single station does all the work.

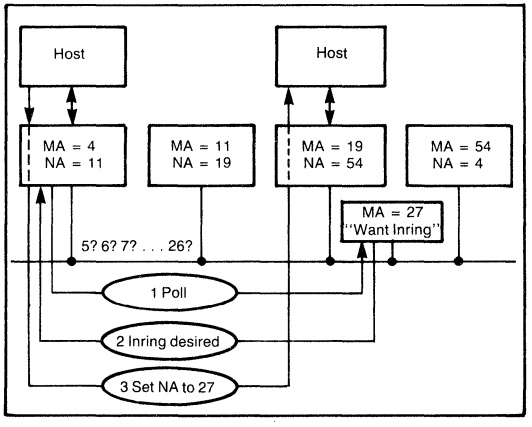


Fig. 3.2.3.2 Central polling. *A single station — in this case, station 4 — dubbed "the administrator," can be charged with all polling tasks. This simplifies the software in the other stations and centralizes network control.*

When the polling station determines that a station has been added, it must place the new station in the access ring. For example, station 4 is the centralized station doing all the polling (Fig. 3.2.3.2), and it discovers that station 27 has recently been added. Station 4 knows this because station 27 now responds to a first-time poll, and because its status bit is set, indicating that it wants to be added to the ring. (Some stations may be receive only, never desiring the right to initiate transmissions.) Station 4 sends a high-level message to the software in station 19, telling it to change its next address register to 27. This message can also prompt station 19 to tell 27 its next address register should be 54. This gets confusing, but it is all done with high-level software. These tasks are not real time and are quite efficient from the network point of view.

Station 4, the administrator, need not create and maintain a table of active stations on the network because the poll response returns three pieces of information. As node 4 polls the stations on the network, it finds out (a) that the polled station does not respond at all, as it would if it polled station 12 in Fig. 3.2.3.2 (b) that the station is already part of the network an is already in the ring or is receive only, as it would if station 4 happened to poll station 11 or 19; and (c) whether the station is attached to the network, is alive and wants to be in the ring, as is the case with a poll to 27. These indications are conveyed by a combination of status bits sent back by the acknowledge frame. This acknowledge frame and status information are transferred at a TAC device level, so a host is not concerned with whether its station wants to be in the ring. The host simply sets up the proper bits in the control registers; the bits are relayed automatically by the TAC. Thus, with a simple algorithm, an administrative station can poll the entire network address range and know the network's exact membership and status.

Central Scan

Central scan is the simplest method of adding stations to a network. It involves sending a global frame to all

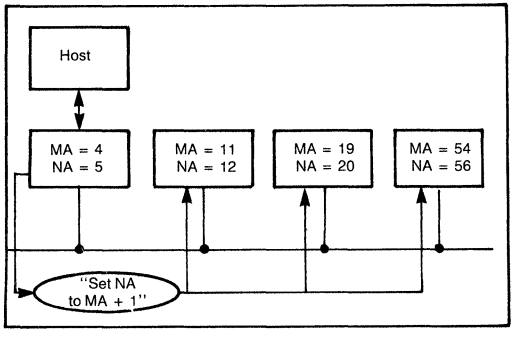


FIG. 3.2.3.3 Central scan request. *A special command can be sent by any station causing all attached TACs to set their NA register to the address of the next possible node. This causes each TAC to poll without the help of the host.*

stations on the network, which forces each to update its own next address register to its station address plus one (NA = MA + 1). Assume station 4 is the centralized station and sends the scan command frame (Fig. 3.2.3.3). Station 11, upon receiving it, automatically sets its next address register to 12 (the TAC does this; the host is not involved but is notified of the situation). Also, station 19 sets its next address register to 20, and station 54 sets its NA register to 55.

The result of this is a round of polling at the TAC level. Station 11, on completing its use of the token, tries to send it to 12. The token to station 12 times out because 12 is not present. Station 11 reclaims the token trying to send it to 13 and so on, causing 11 to poll for station addition. The drawback of this is the huge time disruption incurred by the simultaneous polling.

It is not required that station 4 send this scan control frame to all stations at the same time. If it is known that station 11 exists in the network and that a station may be trying to add into the network after station 11 in the address space, a command can be sent to 11 telling it to set its next address register to 11 + 1. Now 11 will go through scanning station 12, 13, 14 . . . again without intervention from station 11's host software. This directed scanning has the effect of smoothing the polling disturbance over a greater time.

The trade-off of all these methods is the software complexity distribution. If a TAC user assumes more responsibility, providing more intelligence distributed in the software, the system can be more sophisticated in handling new stations. If a user wants the TAC to handle this task itself, saving host software development, he pays only slightly in inefficiency. TAC gives the user an option.

3.2.4 INTERACTION OF THE SUB-PROTOCOLS

After a station is given the token, it will send an information frame, a token frame, or a combination of both. It is this combination frame, referred to as a "piggy back" token, that causes the sub-protocols to interact slightly.

In the normal case (no time-out), the SOURCE may transmit a combination frame to the DATASINK when his access period is over. All stations on the network observe this; after the reception of the current frame is complete, the one whose MA register matches the token address in the frame (TC) knows it has the token.

In the case of a combination frame, the SENDer resets his timer TA on transmission complete and waits for the NA station to transmit something valid,

FIELD DESCRIPTIONS AND ENCODING

TC — The token control byte has the dual purpose of transferring access control between stations and conveying a request for immediate acknowledgement of the frame by its intended receiver.

There is no interaction between the TC field and the DA or SA fields. Thus the token may be transferred to one station and data sent to the same or a different station, with one single frame. The value entered into the TC field is determined by the WD2840 and does not appear in the buffer (except for transparent frames).

TC Value	Meaning
0	Token not affected at this time.
1-254	After current frame, the token belongs to station TC. (The sending station has recovery responsibility).
255	Immediate ACK requested. Token not affected.

NOTE:
The sharing of this field prevents the passing of the token with data (piggy-back) and acknowledgement requests on the same frame. This combination is specifically disallowed because of its undesirable characteristics in network error situations.

DA — Destination address. Value of zero is reserved, 1 to 254 indicates the destination address of the frame. The value 255 is the global (or broadcast) address.

SA — Source address. The values of 0 and 255 are reserved. A value of 1 thru 254 is the address of the sender of the frame.

I — Information Field. User defines format and content.

FCS — Frame Check Sequence. The FCS calculation includes all data between the opening flag and the first bit of the FCS, except for 0's inserted for transparency. The sixteen bit FCS is compatible with the standard HDLC FCS.

AC — Access Control. Conveys supervisory information. May be sent as a command using transparent mode or received in response to an ACK/NAK request. Its format is shown below:

ACCESS CONTROL FIELD

BIT #	7	6	5	4	3	2 1 0
Name	SCANF	WIRING	0	0	0	NVAL2 — NVAL1 — NVAL0

BIT	NAME	DESCRIPTION
7	SCANF	Scan Mode (Command). Indicates that the addressed node(s) must redefine NA = MA + 1 for use on its next token pass.
6	WIRING	Wants in ring (Response). This bit when set informs the node requesting the ACK frame that this node is not in the logical ring, but is requesting entry. It is the logical function of the transmitting node's GIRING .AND. INRING. (see CR13 and SR20) The WD2840 does not act on this information but merely passes it to the host via the ACK'ed frame's FSB.
5-3	—	Reserved.
2-0	NVAL	An encoded NAK/ACK value (Response). The receiving node will set one of the following codes depending upon the state of the last received frame: 0 0 0 — No error 0 0 1 — Insufficient buffers for frame 0 1 0 — Receiver not enabled at frame start 0 1 1 — Receiver overrun 1 0 0 — Frame exceeded 16 receive buffers

to verify his reception of the piggy back token. If the timer expires, the sender sends an explicit token (the data from the combination frame is assumed to have been accepted) and enters the normal token sub-protocol.

The user is prevented from sending a combination frame and requesting an acknowledgement at the same time to prevent possible network state conflict under time-out conditions.

3.3 FRAME FORMAT

The frame format the WD2840 uses to transmit all data and control frames is similar to the industry standard HDLC. A 16 bit CRC is implemented and standard zero insertion (CRC16-CCITT) is used for framing. This framing method allows the use of standard network monitoring and diagnostic equipment such as data scopes and logic analyzers.

Additional address fields and control points are defined as required to support the protocol.

Normal Frame Format:

F - TC - DA - SA - I - FCS - F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
DA = Destination Address (8 bit)
SA = Source Address (8 bit)
I = Information Field (0 to 4095 bytes or 16 buffers, whichever is less).
FCS = Frame Check Sequence (16 bit)

Access Control Format:

F - DA - AC - FCS - F

F = Flag, binary pattern 01111110
DA = Destination Address (8 bit)
AC = Access Control Field (8 bit)
FCS = Frame Check Sequence (16 bit)

Token Pass Format:

F - TC - FCS - F

F = Flag, binary pattern 01111110
TC = Token Control (8 bit)
FCS = Frame Check Sequence (16 bit)

3.4 SENDING A TRANSPARENT OR ACCESS FRAME

Two types of frames are transmitted under the transparent mode under user control. A scan access frame or a transparent frame. The format of the frames are described under 3.3 Frame Format with the transparent format the same as Normal Frame Format.

ACCESS FRAME COMMANDS

There is only one Access Frame type permitted under user control — Scan Frame. The node that is addressed must redefine NA = MA + 1 for use on its next token pass. The format for sending this frame is:

LINK (H)	Pointer to next frame.
LINK (L)	
00 (FSB)	
20h (FCB)	Transparent frame, no acknowledge allowed.
00 LENGTH (H)	Access Control frame size (H, L).
08 LENGTH (L)	
DA	Destination Address or 255 broadcast.
80h	Set Scan Mode.

The FCB can be set for last frame, the acknowledge bit has no effect and no acknowledgements will be given to access frames nor will they be expected by the transmitting WD2840.

The node receiving the access frame will only recognize a scan access frame as a command. Event count #0 will increment and the receiving node will set its NA to MA + 1. Any other access code will increment Event Counter #7.

TRANSPARENT FRAME

Link (H)	
Link (L)	
FSB	
20H FCB	
XX Length (H)	
>08H Length (L)	
TC	pass token, broadcast, ackreq.
DA	
SA	
DATA	

The Transparent Data Frame allows a user to control the token pass, or TC field of a frame by using the first byte after length rather than the FCB. The frame transmitted will look like the User Info part of the buffer without the WD2840 firmware generating anything else but the flags and FCS.

4.0 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

Voltages referenced to V_{SS}

High Supply Voltage (V_{DD}) . . . . . −0.3 to 15V
Voltage at any Pin . . . . . −.03 to 15V
Storage Temperature Range . . . . −55°C to +125°C
Electro-static voltage at any pin . . . . . 400V (Note 6)

NOTE:
Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

OPERATING CHARACTERISTICS (DC):

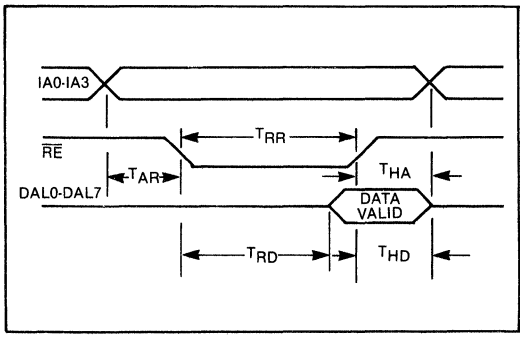
Operating Temperature Range . . . . . 0°C to +70°C

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
I_{DD}	V_{DD} Supply Current		18	30	mA	
I_{CC}	V_{CC} Supply Current		160	220	mA	
V_{DD}	High Voltage Supply	11.4	12	12.6	V	
V_{CC}	Low Voltage Supply	4.75	5	5.25	V	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −0.1mA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{OZH}	Three-State Leakage			50	μA	V_{IN} = V_{CC}
I_{OZL}	Three-State Leakage			50	μA	V_{IN} = 0.4V
I_{IH}	Input Current			10	μA	V_{IN} = V_{CC}
I_{IL}	Input Current			10	μA	V_{IN} = 0.4V

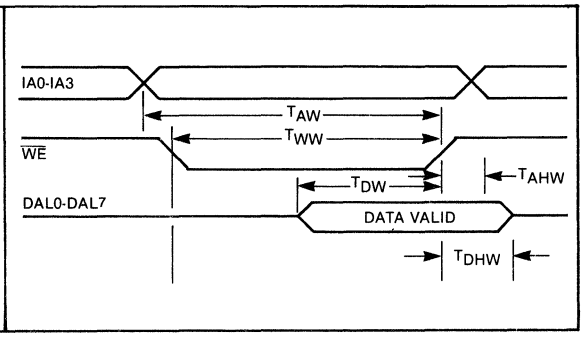
5.0 TIMING CHARACTERISTICS (AC):

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	CONDITIONS
CLK	Clock Frequency	0.5		2.05	MHz	Note 1, 7
RC	Receive Clock Range	0			MHz	Note 4, 7
TC	Transmit Clock Range	0			MHz	Note 4, 7
MR	Master Reset Pulse Width	10			mS	
T_{AR}	Input Address Valid to $\overline{RE}$	0			nS	
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid	2		375	nS	Note 5, 2
T_{HD}	Data Hold Time From Read to Strobe	20		100	nS	
T_{HA}	Address Hold Time From Read Strobe	0			nS	
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	100			nS	
T_{WW}	Minimum $\overline{WE}$ Pulse Width	200			nS	
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100			nS	Note 2, 3
T_{WRR}	CS High Between Writes	300			nS	
T_{RDR}	CS High Between RE	300			nS	
T_{RR}	RE Pulse Width	375			nS	
T_{DAK}	DACK Pulse Width	375				
T_{AHW}	Address Hold Time After $\overline{WE}$	80			nS	
T_{DHW}	Data Hold Time After $\overline{WE}$ or After $\overline{DACK}$ for DMA Write	100				
T_{DA1}	Time From $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1			80	nS	
T_{DA0}	Time From $\overline{DACK}$ to Output Address Valid if ADRV = 0			375	nS	Note 5
T_{DD}	Time From Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)			375	nS	Note 5
T_{DAH}	Output Address Hold Time From $\overline{DACK}$	20		100	nS	
T_{DMW}	Data Hold Time From $\overline{DACK}$ For DMA Read	20		100	nS	Note 2
T_{TDV}	TD Valid	100			nS	
T_{SRD}	RD Setup	0			nS	
T_{HRD}	RD Hold	320			nS	

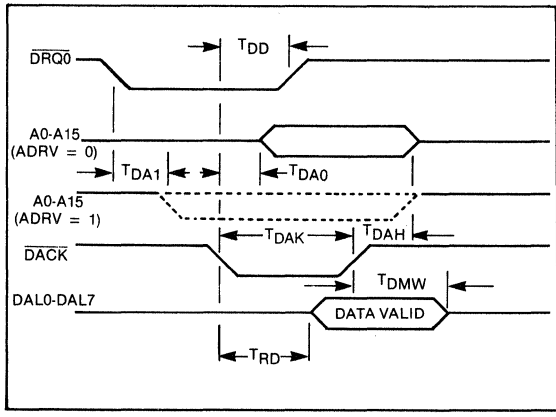
NOTES:
1. Clock must have 50% duty cycle.
2. There must not be a CPU read or write ($\overline{CS}$-$\overline{RE}$ or $\overline{CS}$-$\overline{WE}$) within 500 nanoseconds after the trailing (rising) edge of $\overline{DACK}$.
3. There must not be the leading (falling) edge of $\overline{DACK}$ allowed within 500 nanoseconds after the completion of a CPU write ($\overline{CS}$-$\overline{WE}$).
4. See "Ordering Information" for maximum serial rates.
5. C(load) = 100pf
6. Measured by discharging a 100pf capacitor to each pin through a 1K ohm resistor.
7. TC/RC must be <43% of CLK when transmitting multiple buffers.



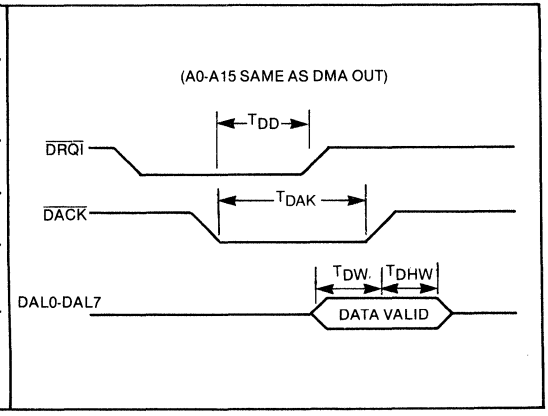
CPU READ ($\overline{CS}$ IS LOW)



CPU WRITE ($\overline{CS}$ IS LOW)



DMA OUT

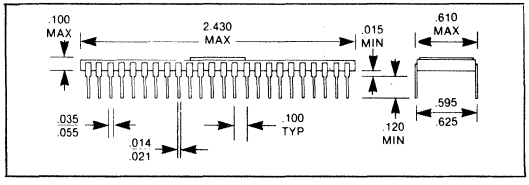


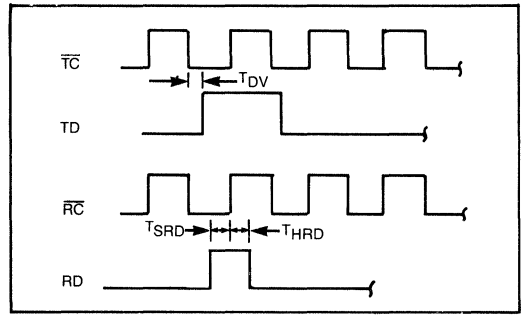
DMA IN

6.0 ORDERING INFORMATION

DEVICE NUMBER	MAXIMUM RATE
WD2840-01	100 Kbps
WD2840-05	500 Kbps
WD2840-11	1.0 Mbps

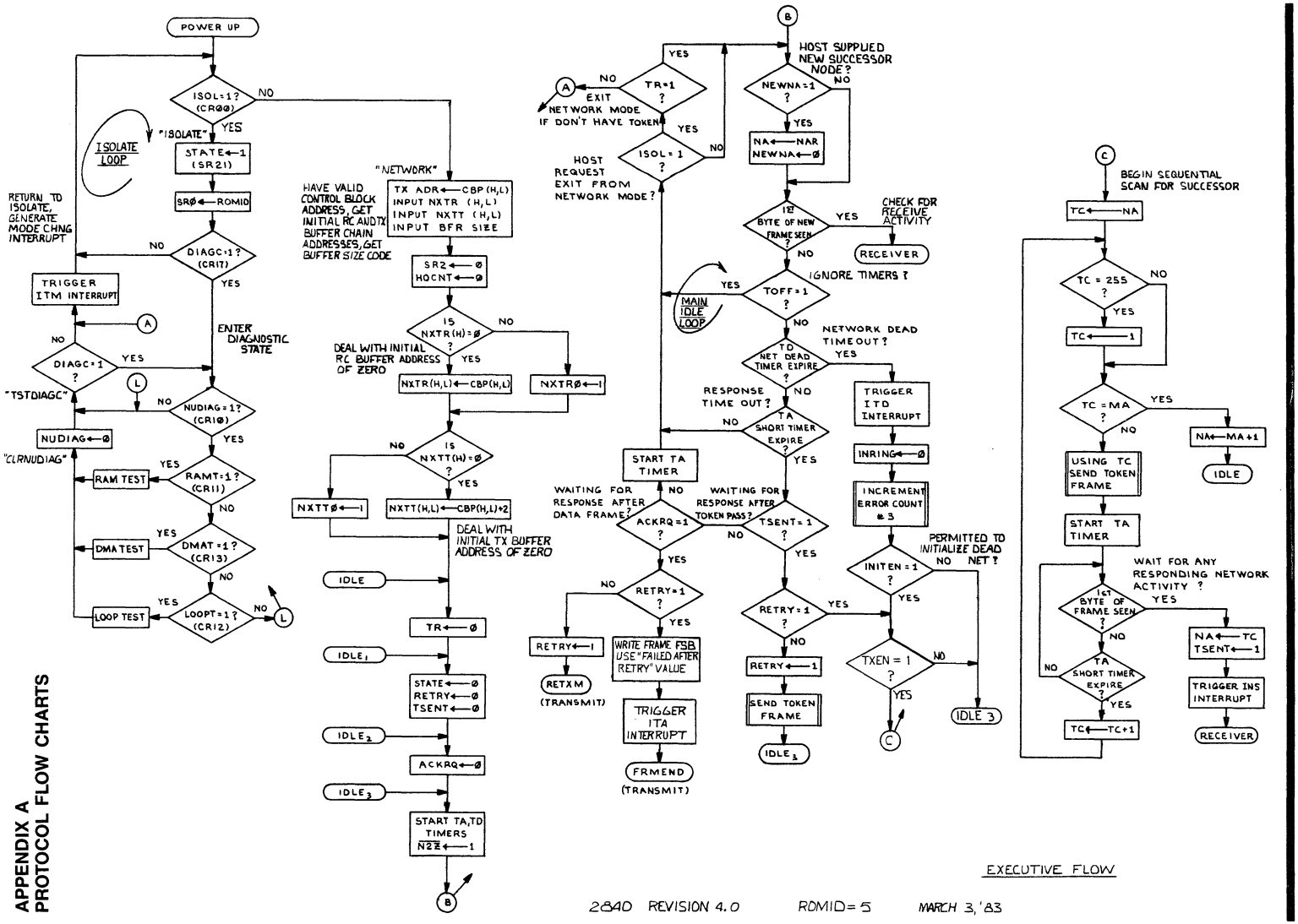
Package Diagram





TD-RD TIMING

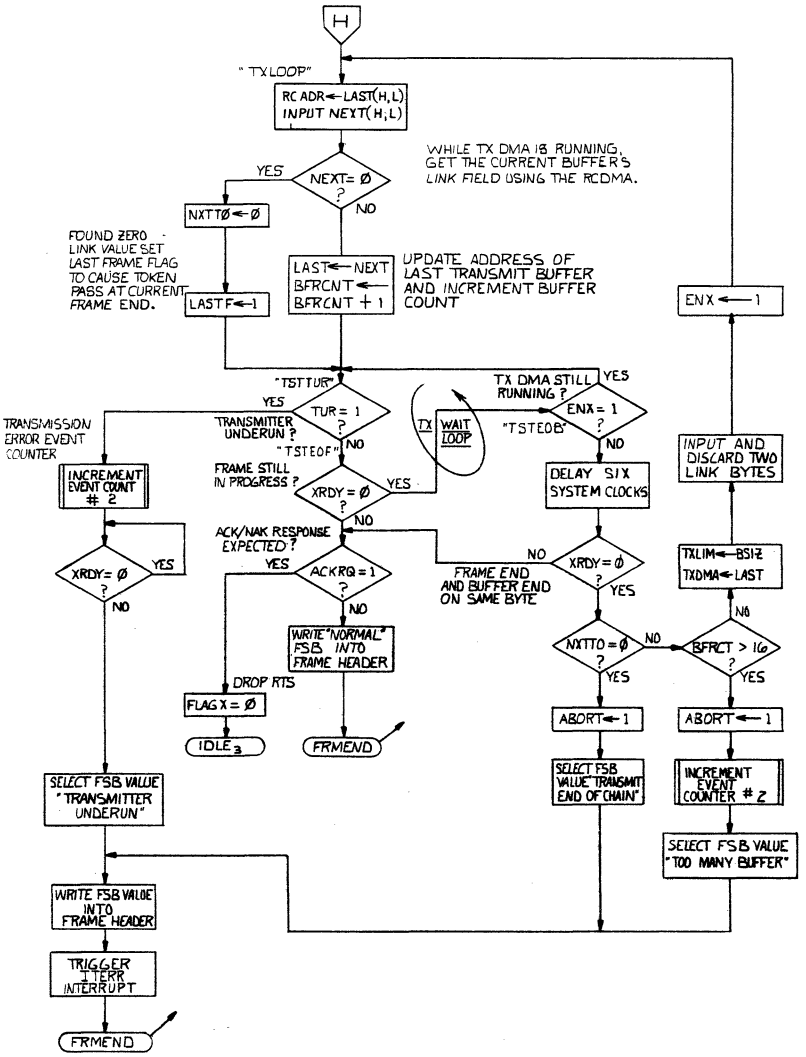
Printed in U.S.A.

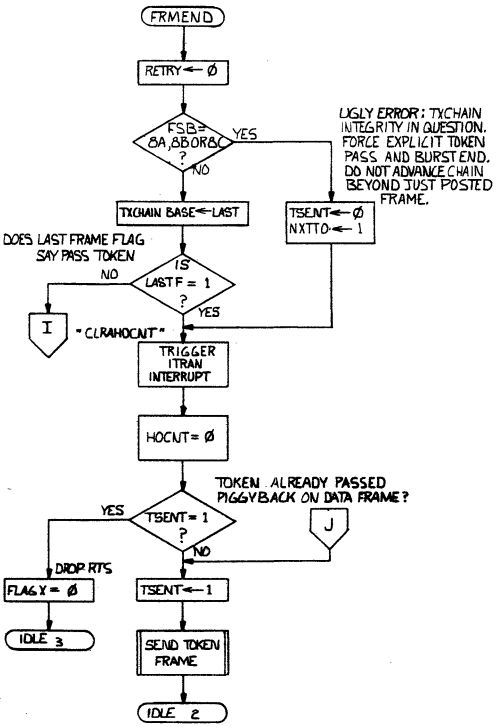


EXECUTIVE FLOW

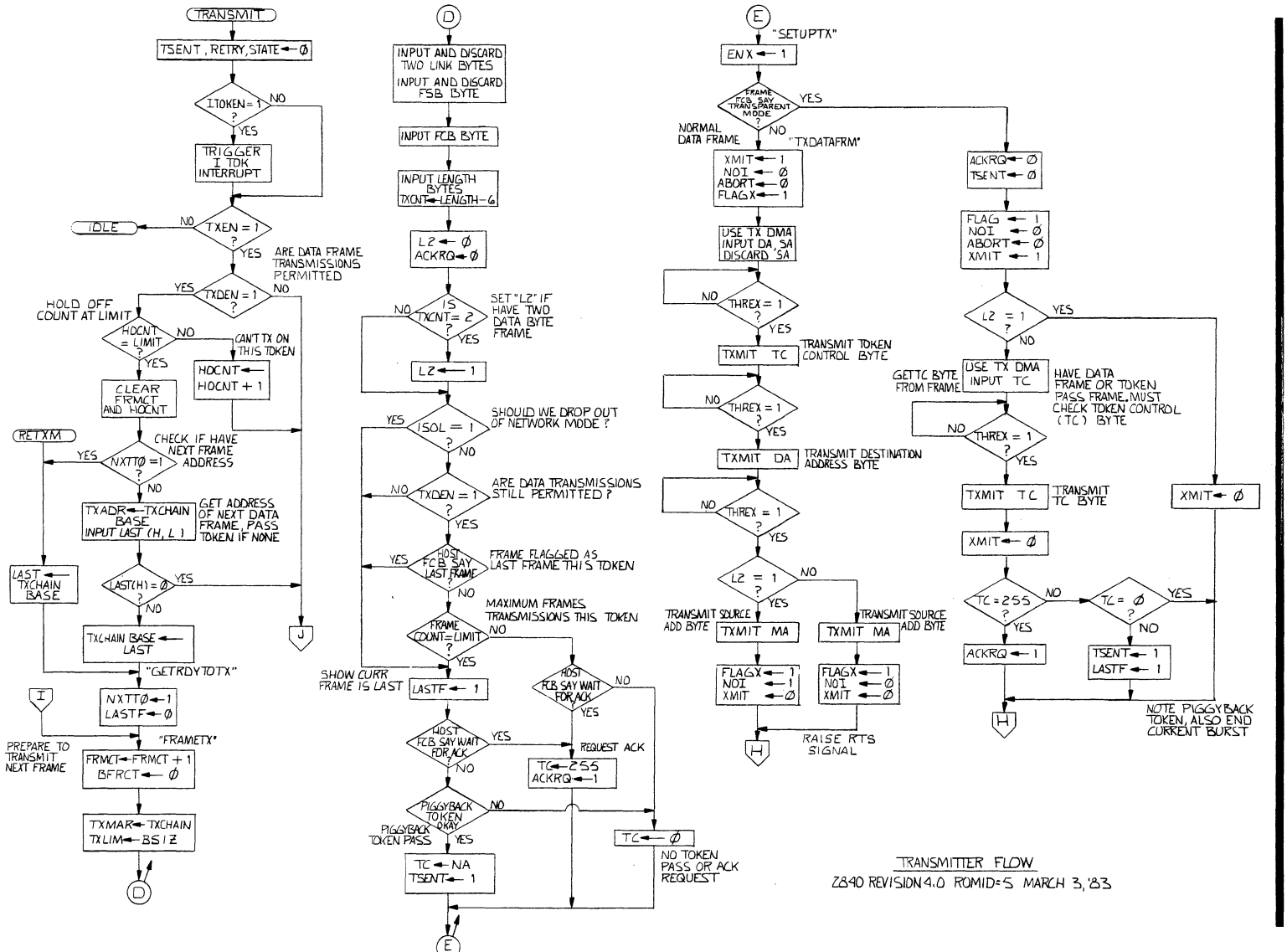
2840 REVISION 4.0 ROMID=5 MARCH 3, '83

APPENDIX A
PROTOCOL FLOW CHARTS



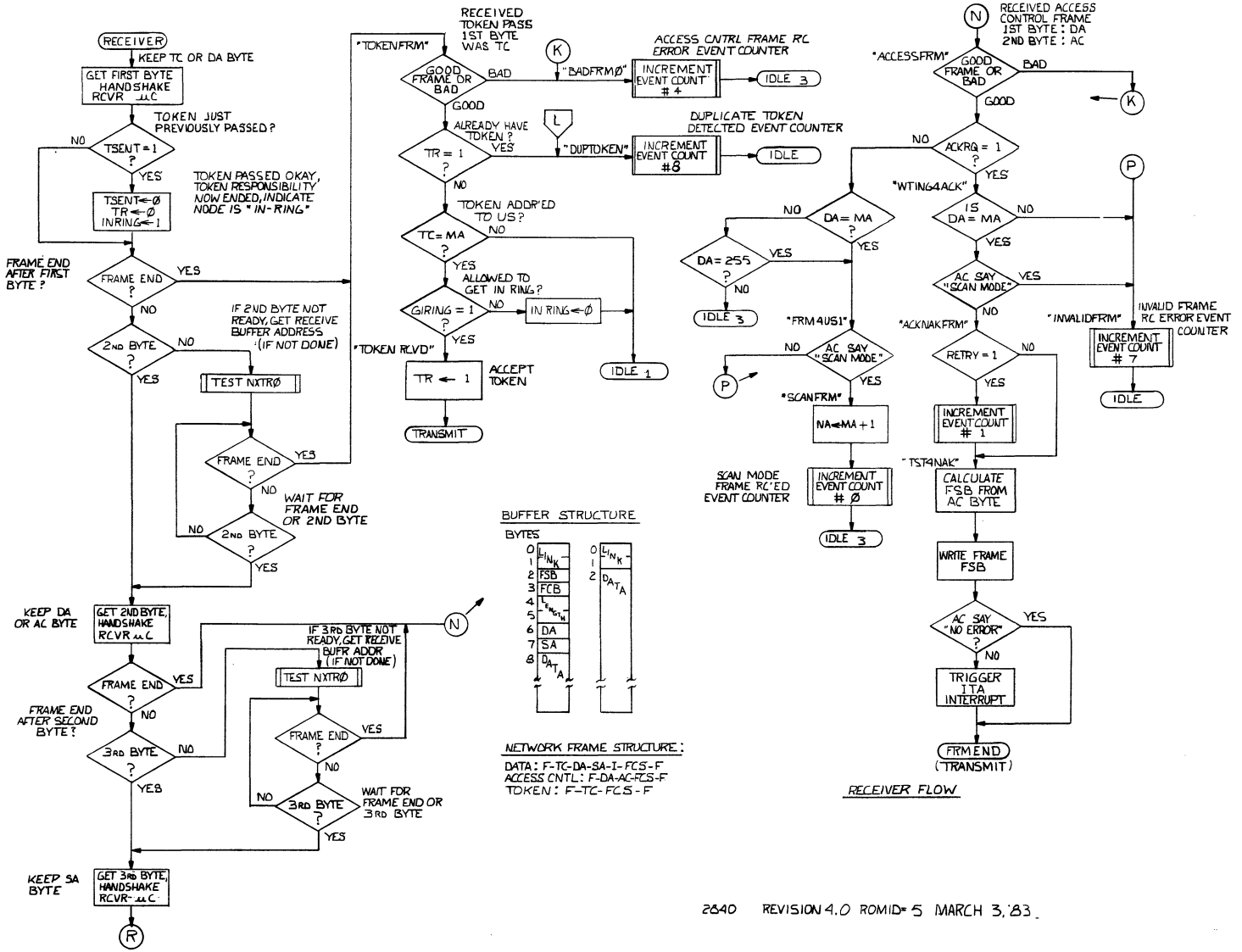


TRANSMITTER FLOW

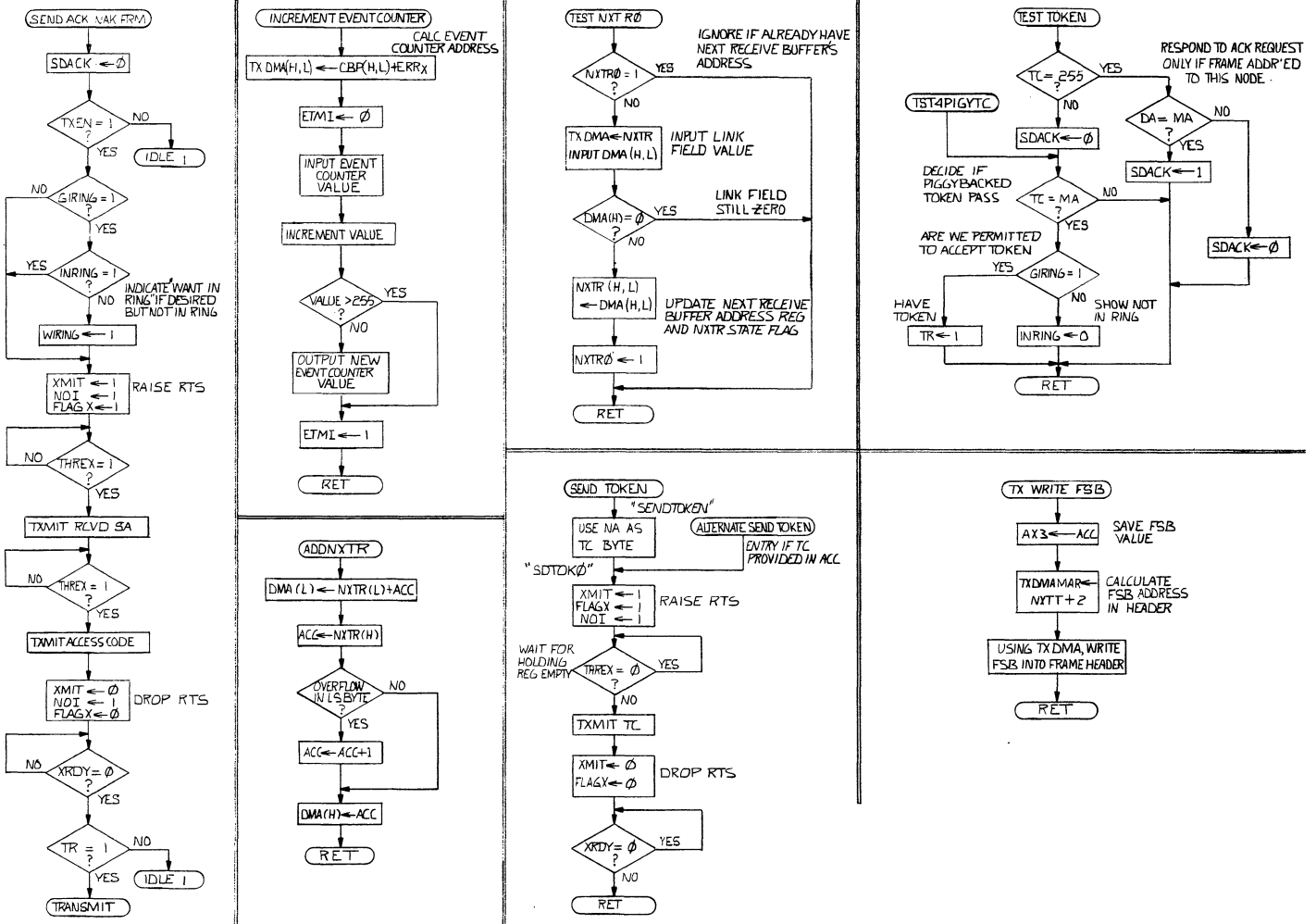


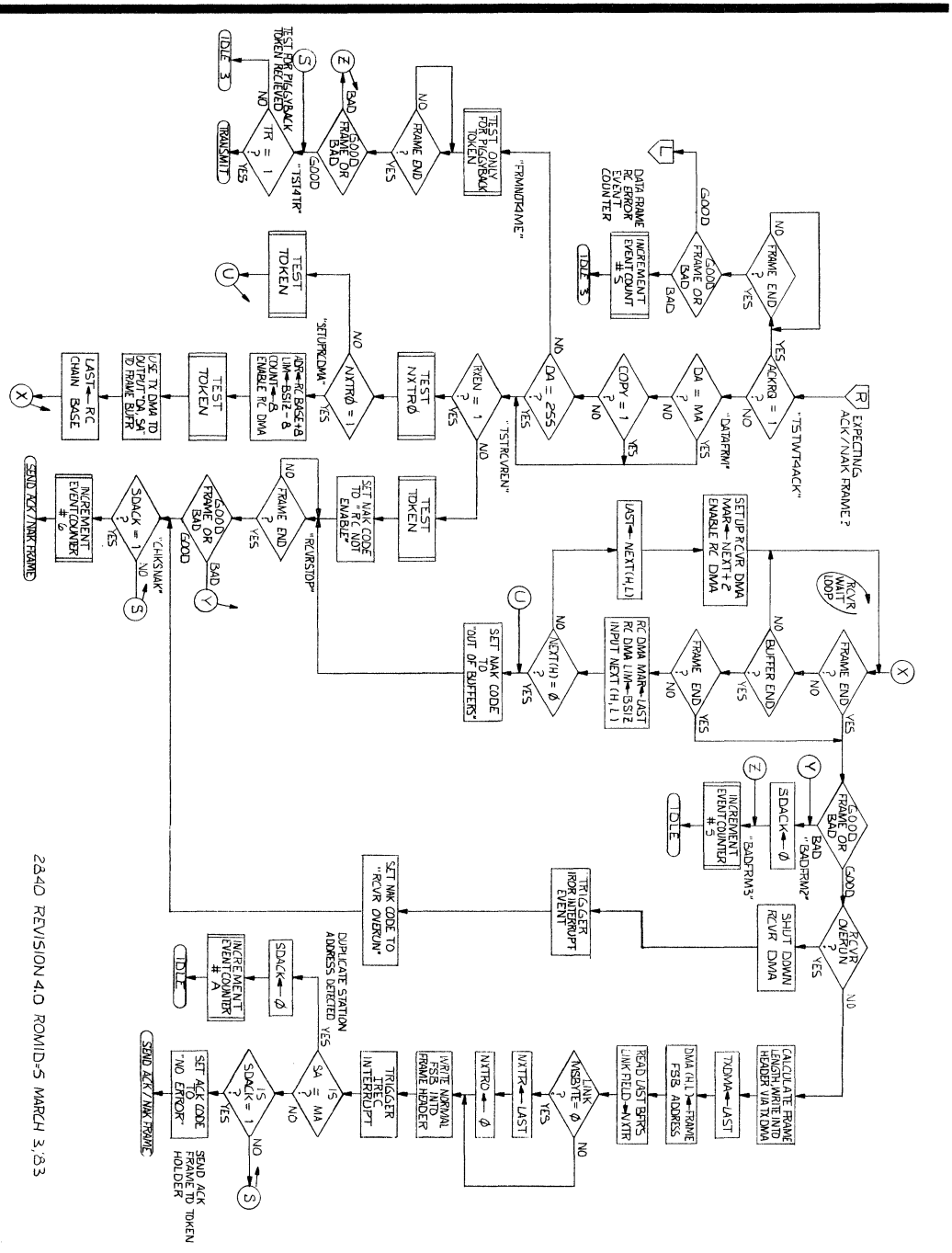
TRANSMITTER FLOW

Z840 REVISION 4.0 ROMID=5 MARCH 3, '83



2840 REVISION 4.0 ROMID= 5 MARCH 3, '83


SEND ACK, NAK FRM
SDACK ← Ø
TXEN = 1 ?
NO
IDLE 1
YES
GIRING = 1 ?
NO
YES
INRING = 1 ?
YES
NO
INDICATE WAIT IN RING IF DESIRED BUT NOT IN RING
WIRING ← 1
XMIT ← 1
NOI ← 1
FLAGX ← 1
RAISE RTS
THREX = 1 ?
NO
YES
TXMIT RCVD SA
THREX = 1 ?
NO
YES
TXMIT ACCESS CODE
XMIT ← Ø
NOI ← 1
FLAGX ← Ø
DROP RTS
XRDY = Ø ?
NO
YES
TR = 1 ?
NO
YES
IDLE 1
TRANSMIT
INCREMENT EVENT COUNTER
CALC EVENT COUNTER ADDRESS
TX DMA(H,L) ← CBF(H,L)+ERRX
ETMI ← Ø
INPUT EVENT COUNTER VALUE
INCREMENT VALUE
VALUE > 255 ?
YES
NO
OUTPUT NEW EVENT COUNTER VALUE
ETMI ← 1
RET
ADDNXTR
DMA(L) ← NXTR(L)+ACC
ACC ← NXTR(H)
OVERFLOW IN LS BYTE ?
NO
YES
ACC ← ACC+1
DMA(H) ← ACC
RET
TEST NXT RØ
IGNORE IF ALREADY HAVE NEXT RECEIVE BUFFER'S ADDRESS
NXTRØ = 1 ?
YES
NO
TX DMA ← NXTR
INPUT DMA(H,L)
INPUT LINK FIELD VALUE
DMA(H) = Ø ?
YES
LINK FIELD STILL ZERO
NO
NXTR(H,L) ← DMA(H,L)
UPDATE NEXT RECEIVE BUFFER ADDRESS REG AND NXTR STATE FLAG
NXTRØ ← 1
RET
SEND TOKEN
"SENDTOKEN"
USE NA AS TC BYTE
ALTERNATE SEND TOKEN
ENTRY IF TC PROVIDED IN ACC
"SDTOKØ"
XMIT ← 1
FLAGX ← 1
NOI ← 1
RAISE RTS
WAIT FOR HOLDING REG EMPTY
THREX = Ø ?
YES
NO
TXMIT TC
XMIT ← Ø
FLAGX ← Ø
DROP RTS
XRDY = Ø ?
YES
NO
RET
TEST TOKEN
RESPOND TO ACK REQUEST ONLY IF FRAME ADDR'ED TO THIS NODE
TC = 255 ?
YES
NO
TST4PIGYTC
SDACK ← Ø
DA = MA ?
NO
YES
SDACK ← 1
DECIDE IF PIGGYBACKED TOKEN PASS
TC = MA ?
NO
YES
SDACK ← Ø
ARE WE PERMITTED TO ACCEPT TOKEN
GIRING = 1 ?
YES
NO
HAVE TOKEN
SHOW NOT IN RING
TR ← 1
INRING ← Ø
RET
TX WRITE FSB
AX3 ← ACC
SAVE FSB VALUE
TXDMAMAR ← NXTT+2
CALCULATE FSB ADDRESS IN HEADER
USING TX DMA, WRITE FSB INTO FRAME HEADER
RET



See page 383 for ordering information.

WD2840 Application Note

INTERFACING THE WD2840 TO A VERSABUS SYSTEM USING A DUAL PORT MEMORY

This application note describes one possible method of interfacing the WD2840 Token Access Controller with a general purpose microprocessor based system. This is intended to be an example design only, no effort has been made to minimize the logic required to perform these functions as would be done in a production design. Rather, the design has been kept "clean" to promote readability.

This implementation is designed with a dual-port memory concept allowing its use in systems that either do not support DMA at all, as well as systems that are unable to guarantee reasonable DMA response to a request (Figure 1). Examples of these systems are low end personal computers that allow their disk controllers to "hog" the DMA channel for an entire sector transfer. Very high end systems are also candidates for the dual-port memory technique. Here, the system bus may be shared by multiple hosts and be of such extreme bandwidth that the internal WD2840 DMA controller may be inefficient.

In most applications, the WD2840, can simply self-DMA its data directly to/from the host system's working memory. In the applications described above, the WD2840 must DMA its messages to/from the network into a local RAM allowing the host to access it at its leisure.

REFERENCES

- WD2840 Token Access Controller Specification, Western Digital Corporation, 1983.
- "Token Passing Cashes in with Controller Chip" Electronic Design, October 14, 1982.
- Versabus Technical Reference Manual Motorola,
- RS-422 Technical Specification

This design is described in six sections:

- Host dependent logic, here designed for the Motorola Versabus system, including all required bus interface drivers and timing.
- Local two-port buffer memory which is shared by the host and the WD2840.
- Arbitration logic to fairly share the buffer memory, especially when both the host and WD2840 demand access at the same time.
- WD2840 Token Access Controller and associated timing
- Media interface consisting of a manchester encoder/decoder and liner drivers
- Generalized initialization flowchart

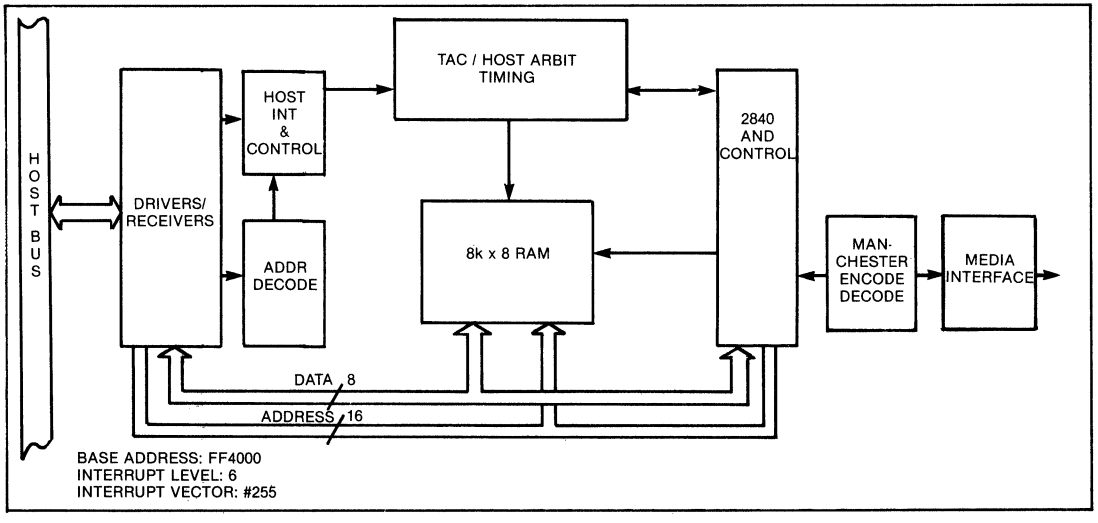


Figure 1. Versabus Application of WD2840 Using Dual Port Memory

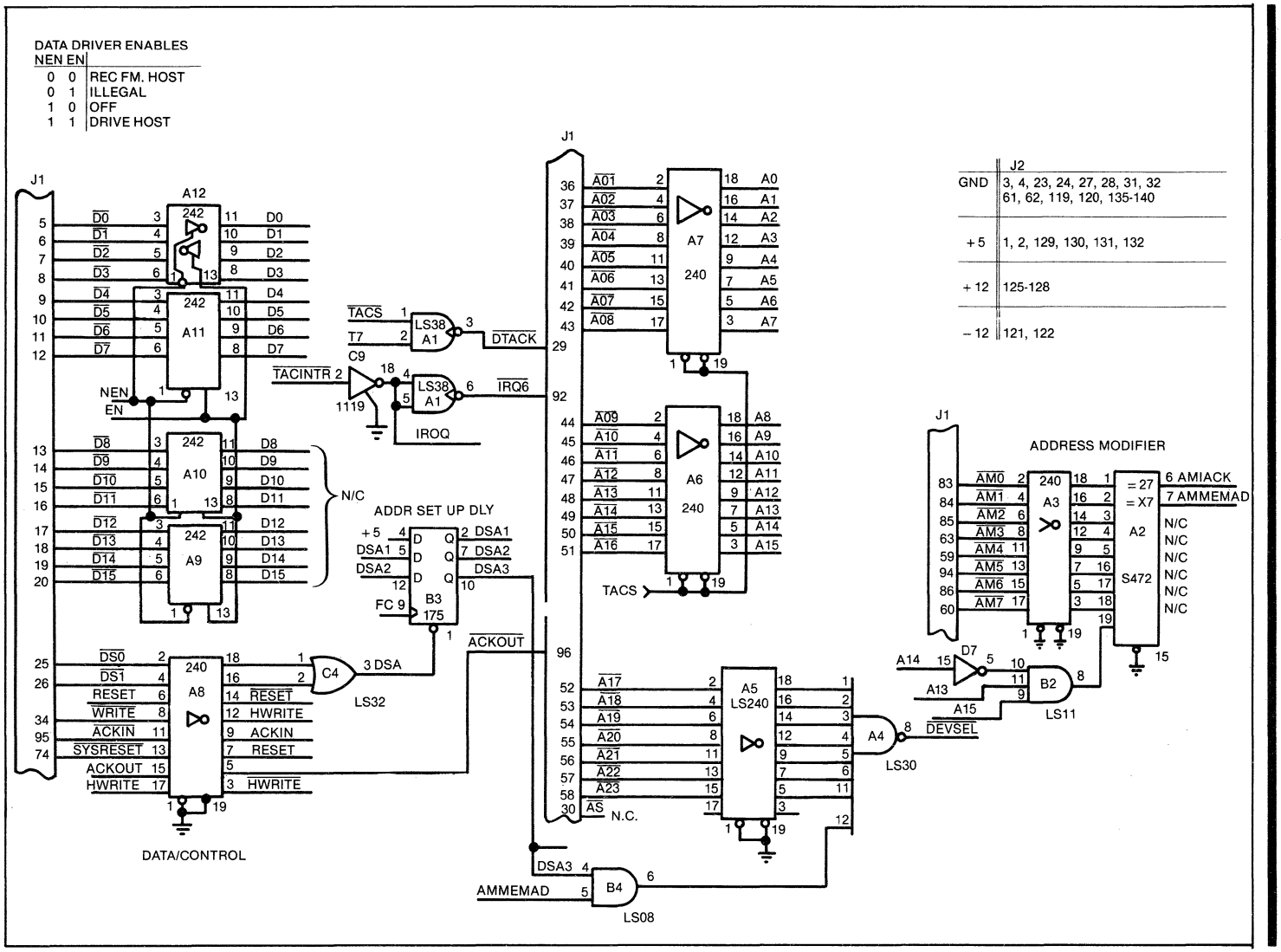


Figure 2. Host Interface

HOST INTERFACE

The host interface (Figure 2) utilizes common three-state bus drivers buffering the Versabus from the internal data bus. They are enabled low-Z onto the host bus whenever the host "reads" from the local memory (or WD2840 registers) and are enabled to drive the internal bus whenever the host writes to the internal memory (or registers). All other times these are hi-Z allowing other modules on the Versabus side to use that bus, as well as allowing the WD2840 to use the internal bus. Only an eight bit internal data bus is used mapping all host memory accesses into the lower byte. (Bus drivers A10 and A11 are not used)

Sixteen address bits are buffered and driven onto the internal address bus when the host has access to the RAMs (otherwise the WD2840 drives the internal address bus). The additional address lines of the Versabus are "anded" with the I/O Data Strobe signals DS0 and DS1 and address modifier bits creating a device select signal (DEVSEL) when all are active simultaneously indicating the host actually wants to access this module.

The Host Interrupt and Driver control logic (Figure 3) supplies the host interrupt vector (0FFH) when acknowledged (C10). Acknowledgement occurs when the Versabus ACKIN is received in conjunction with the proper priority level (set at 4 in this design), the proper address modifier (AMIACK), a short deskew delay (DSA3), and a signal indicating an interrupt was indeed generated by this module (IROQ).

The logic on this sheet also controls the direction of the data buffers previously described (with signals EN and NEN), presuming the host has active control of the local bus (HOST = 1). The host requests control of the bus for access to the on-board RAM and during interrupt acknowledgement.

CLOCK/ARBITRATION

This logic (Figure 4) generates the synchronous timing used in the rest of the sections. A 16MHz signal derived from a crystal oscillator (part of the manchester logic, described later) is buffered (by C9 and then called FC). This high speed clock is also divided down for the WD2840 system clock CLK at 2 MHz (other slower rates are not used in this design).

This high speed clock clocks a simple latch (B7) until either the host or the WD2840 request local bus access. If the host desires access to this module, HOST is made true, the on-board WD2840 DMA request generated TACDRQ. When either (or both) of these signals occur, IDLE goes false (B5 pin4) freezing the state of latch B7.

IDLE going false starts the timing chain (B1, C1) that generates general timing pulses used later.

When the local memory sequence is complete, at time T10 for the TAC (B8 pin 6) or at time T7 for the

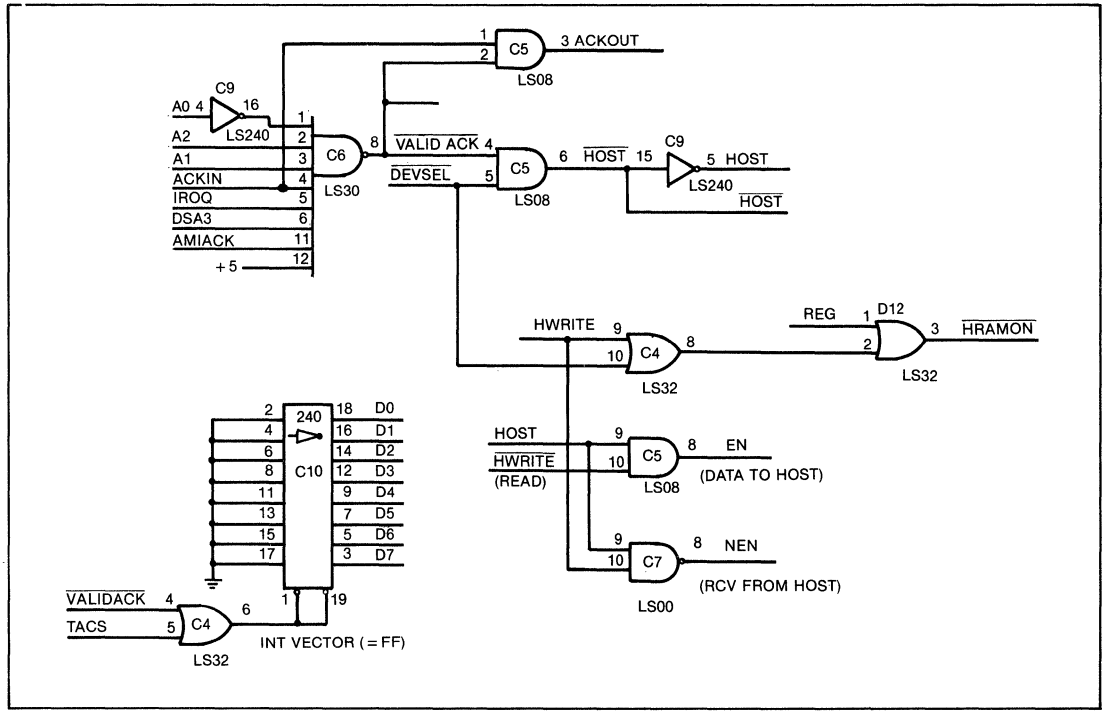


Figure 3. Host Interrupt and Driver Control

host (B2 pin 6) a special end of cycle delay is initiated (via shift register E7). This delay ensures that at least 500ns is maintained between WD2840 DMAs and possible host I/O accesses. At the end of this delay, flip-flop B6 generates a one clock "DONE" pulse resetting the arbitration logic.

MEMORY ARRAY

The memory (Figure 5) uses simple static memories configured as 8K by 8 bits. The RAM data lines are buffered onto the local data bus due to loading considerations. The RAM array is enabled during all I/O operations except those to the first sixteen locations, which are used for accessing the sixteen internal WD2840 registers (REG).

WD2840 SUPPORT

The WD2840 interface logic is given in Figure 6. The system clock (CLK) is derived from the timing generator (Figure 4). (This clock may be asynchronous with the transmit and receive data clocks if desired.) Address latches are used in this design to provide additional signal drive and to improve memory access timing (the WD2840 does have internal address latches that are useful in less stringent applications).

Host Write (HWRITE) is used to control the direction of I/O operations with the WD2840. When true, the WD2840 expects its internal registers to be written into. This occurs when both WE (pin 3) and CS (pin 4) are both low. Gate C7 1,2,3 ensures that the WE* signal goes false prior to the data changing (ensures hold time). Chip select logic (D10, 1,2,13,12) enables reads or writes only when the host has access to the internal bus, the internal address bus holds a value in the range of 0-15 (REG true), and a short set-up timer has expired (T1).

Gate F10 (11,12,13) "ands" the WD2840s DMA input and output requests and presents them to the arbitration logic described earlier (via TACDRQ). The sense of the WD2840 DMA request (input or output) is latched (with E10). The DMA output signal is delayed for RAM setup (T2) and turned off before the data is removed to meet RAM hold timing (T7) and presented to the RAM control logic to generate the write pulse.

MANCHESTER ENCODER/DECODER

The manchester encoder/decoder used here is a Harris HD-6409 (Figure 7). This device is ideal for use with the WD2840 in that its "invalid manchester output," that detects missing clocks, etc., can be directly connected to the WD2840's SQ input. A 16 Mhz crystal controls the internal digital phase locked loop used for clock recovery and generated the 16 Mhz master clock (FC) used for general timing in this design.

The "modem" consists of a simple RS-422 balanced driver and receiver. More elaborate media interfaces are possible, including FSK and broadband, depending on speed / distance / number of taps / cost requirements.

INITIALIZATION

Figure 10 "flow chart" gives a generalized method of initializing a WD2840 based communications subsystem. First the WD2840 internal diagnostic are preferred, followed by loading of station parameters. Next the network is tested for activity and potential duplicate addresses. Finally the WD2840 TXEN is set allowing normal network generation. The Host now simply monitors TX and RX chains to sent/receive network data.

SUMMARY

This application note details a simple WD2840 subsystem designed around the VERSAbus form factor. The on-board RAM makes removes any DMA/host bus access questions from the system design. A very simple line driver allows a number of these modules to communicate at speeds of 1 Mbps.

Note that this application note is intended for illustration only; simpler and more elaborate interfaces are possible.

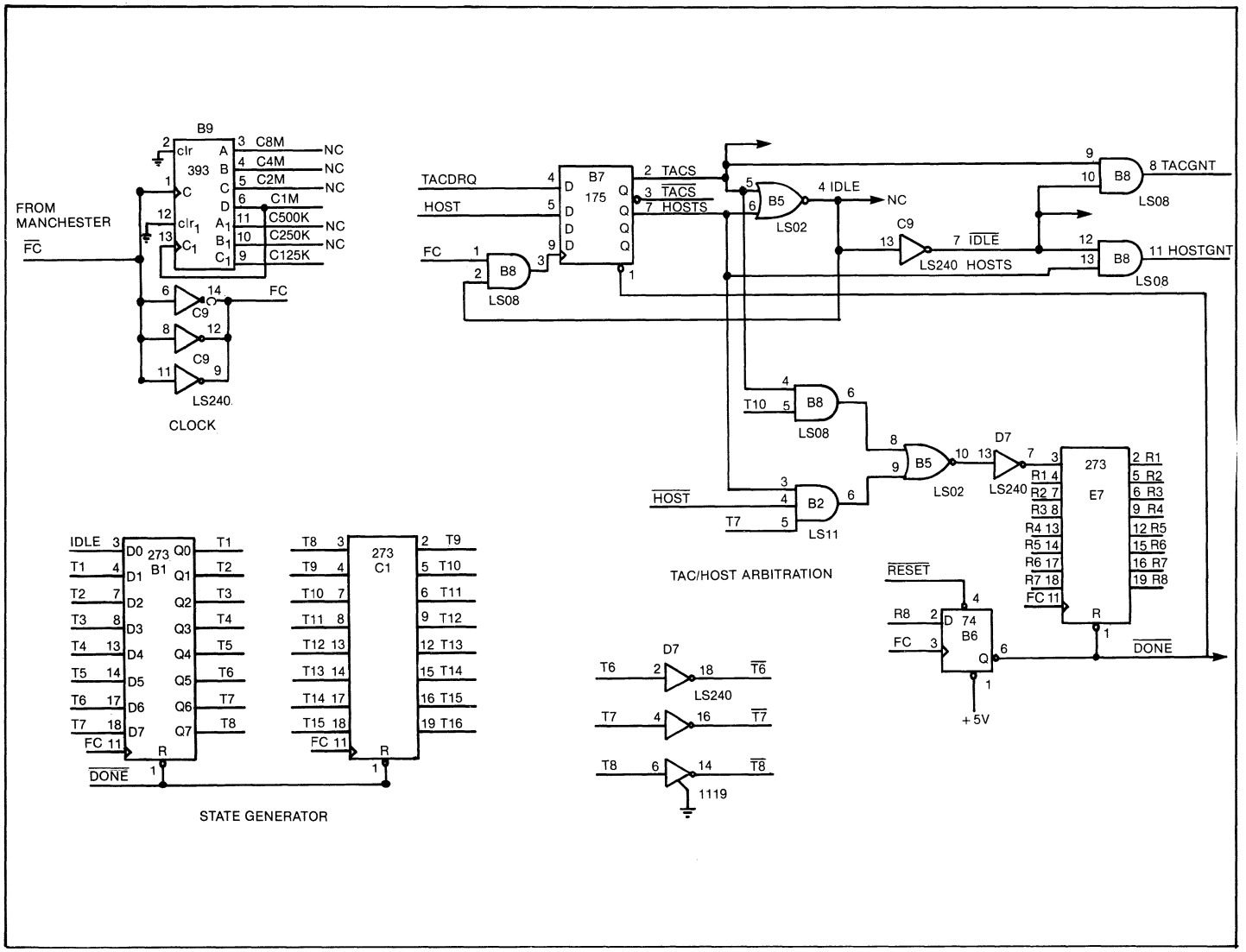


Figure 4. Clock and Arbitration

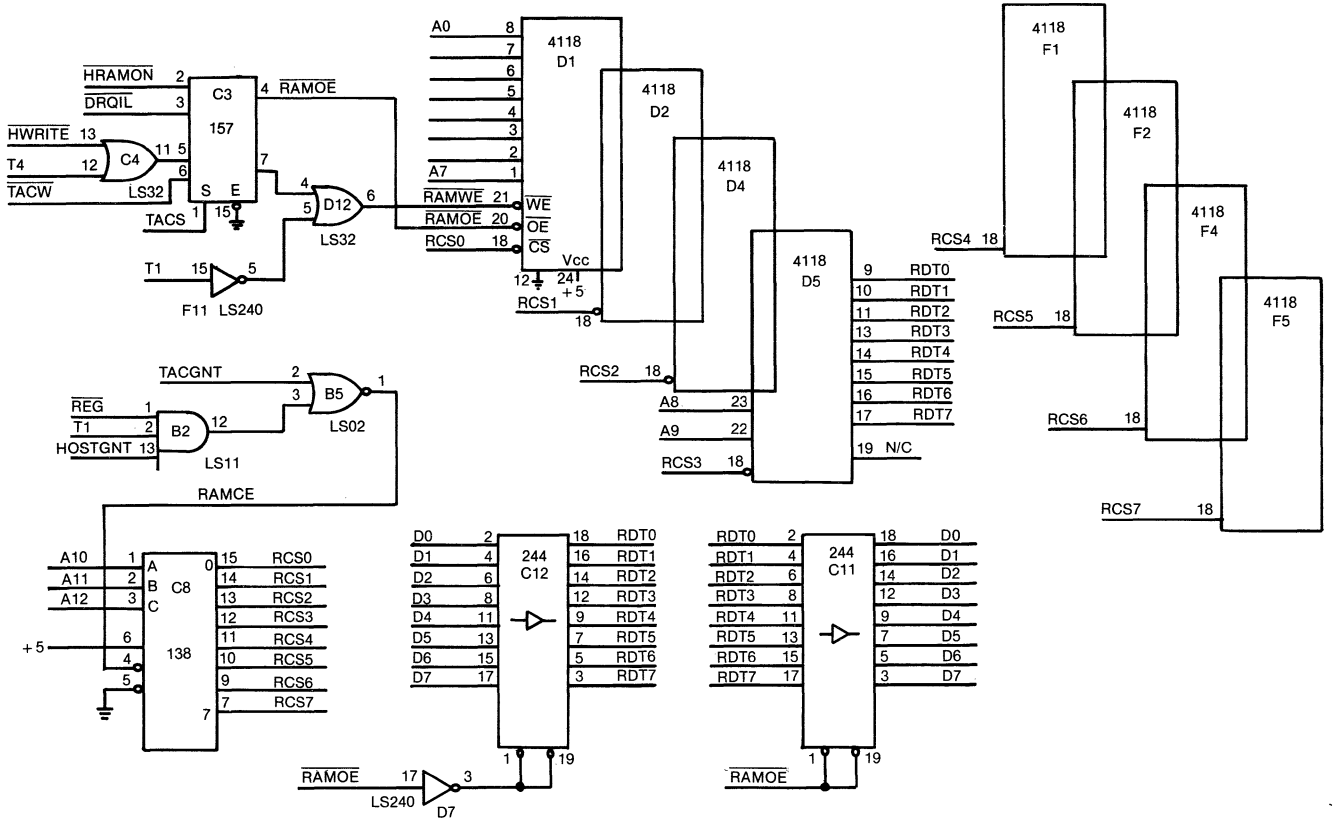


Figure 5. Memory Array

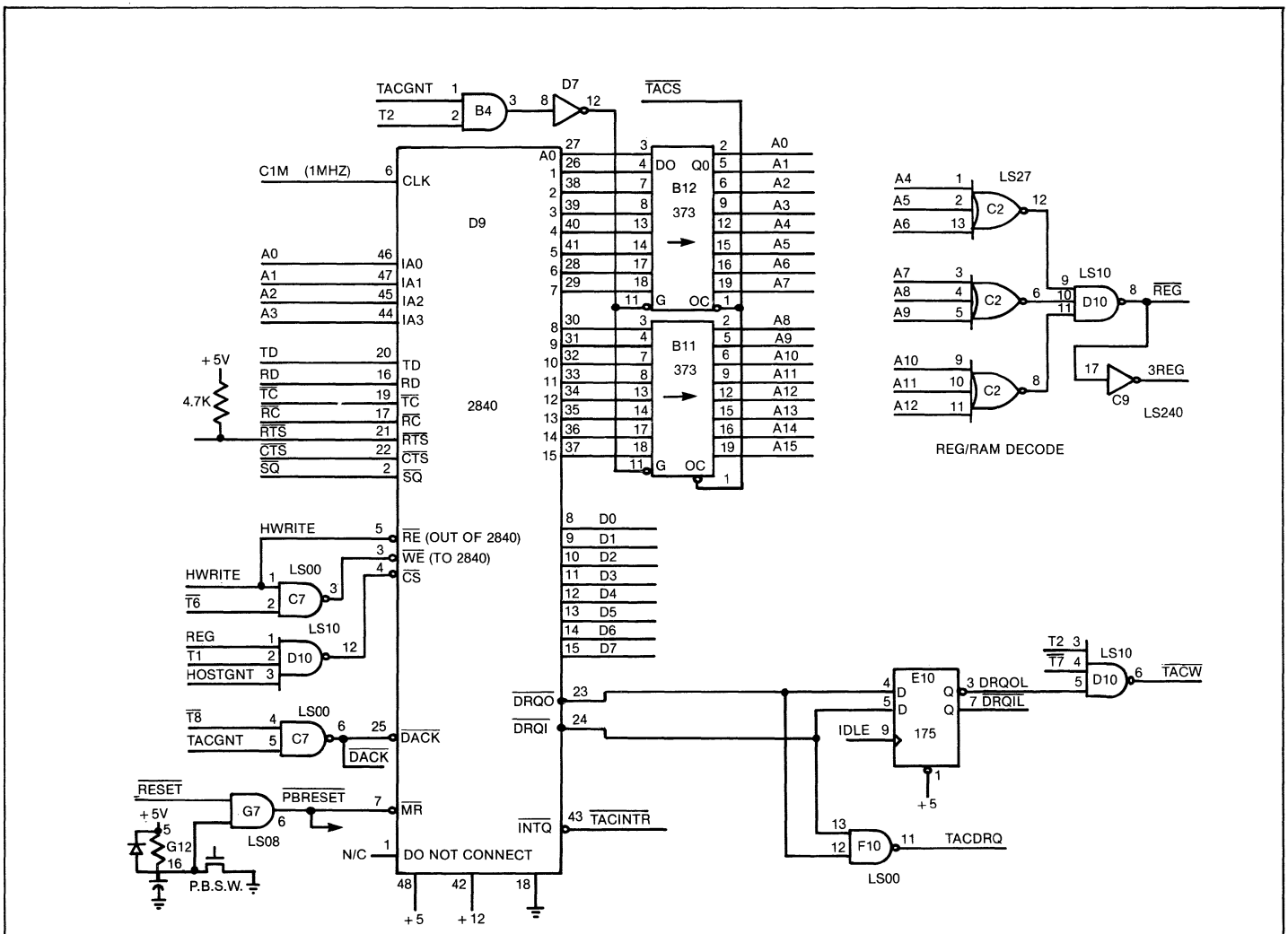


Figure 6. WD2840 Support

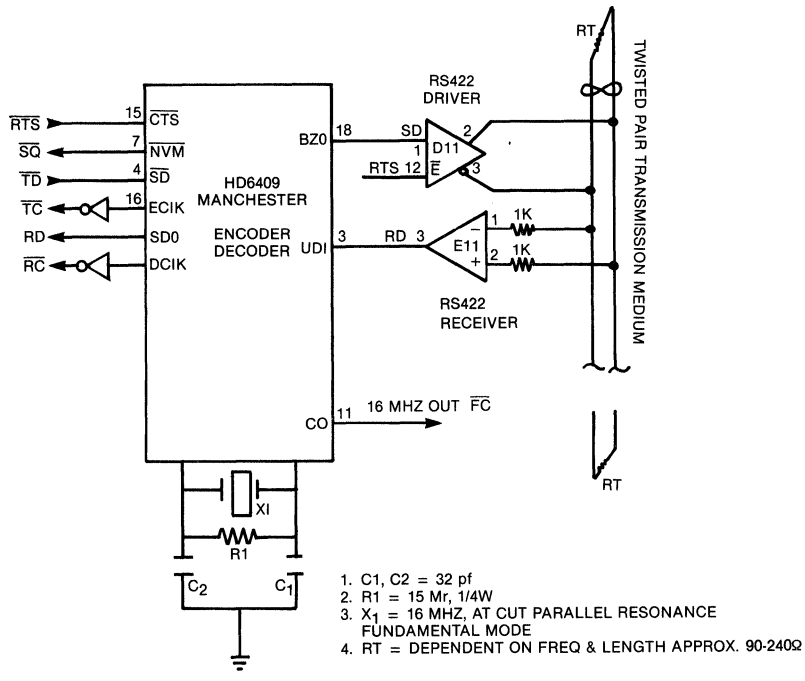


Figure 7. Manchester Encoder/Driver

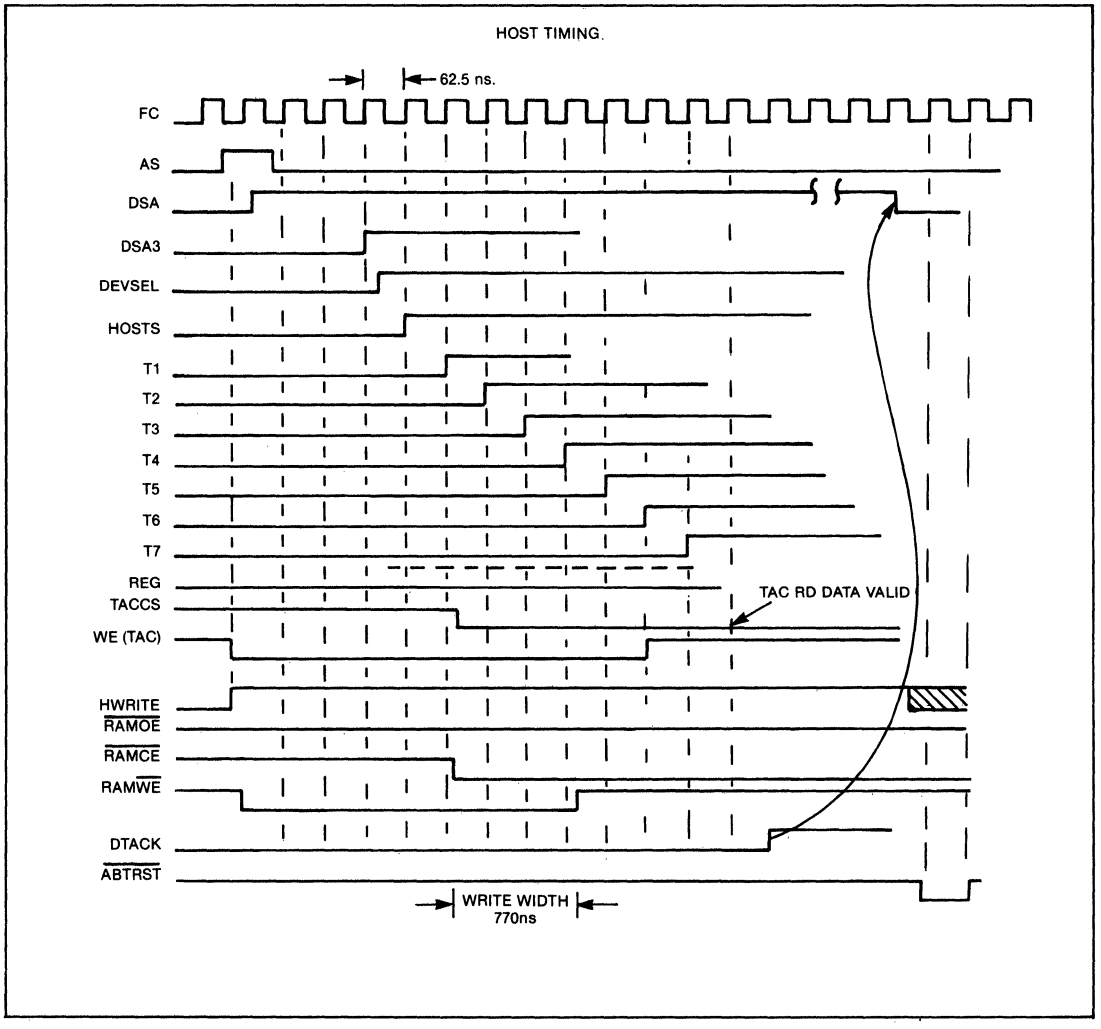


Figure 8. Host Timing

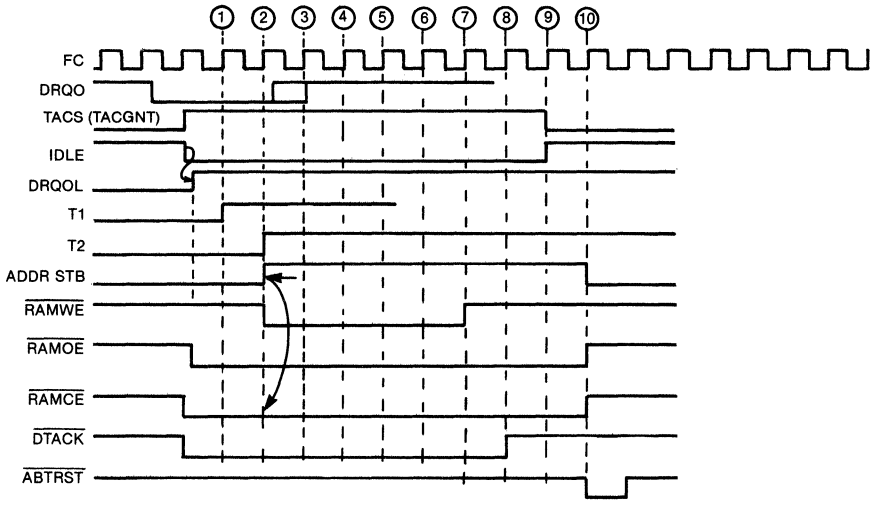


Figure 9. TAC Timing

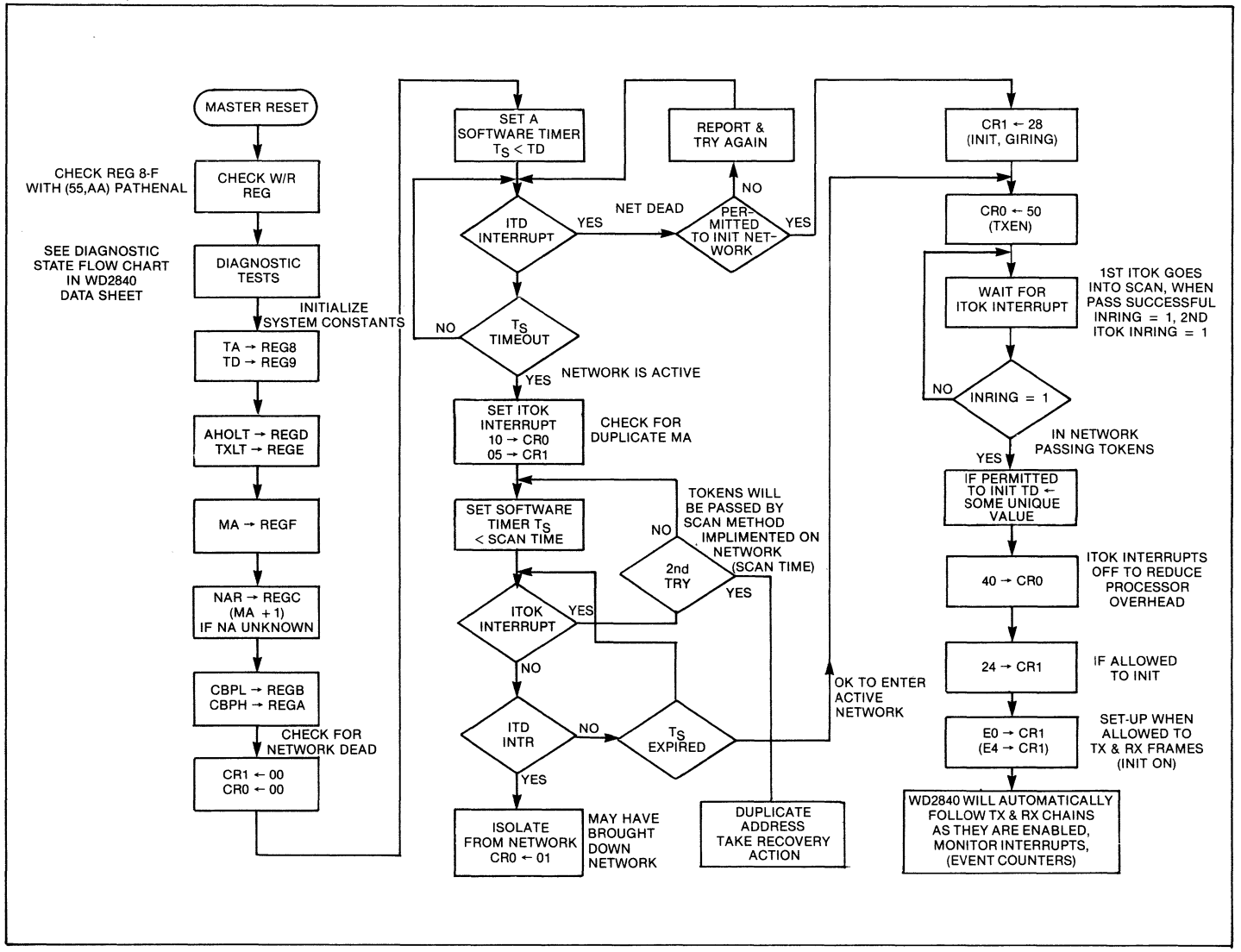


Figure 10. Typical Set-Up Sequence For WD2840

LOCAL NETWORK ACCESS TRADEOFFS

Cost/complexity tradeoffs are examined in CSMA/CD and token passing techniques for accessing local area networks

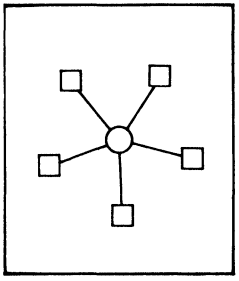
by Mark Stieglitz

Local networks are characterized by problems that are very similar to those encountered in conventional data communications networks.[1] Local networks, however, generate new problems and opportunities that require reconsideration of tradeoffs in system cost/complexity. A fundamental point of decision in local network design is the choice of access method. Chief contenders among access techniques are carrier sense multiple access and token passing.

What is a local network?

The current controversial nature of local area networks (LANs) is highlighted by their many definitions. A common theme in these is that the LAN be privately owned and/or administered by the user. An LAN need not be considered only as a high speed data transfer mechanism; current private branch exchanges also meet the definition of a private system. The opportunity to optimize the network for a particular user's application, therefore, becomes a key feature of the network. In this discussion we assume the following: that a local network is a privately owned communication system; it usually runs at data rates of 100k bits/s and above; and it is usually restricted geographically (100 to 25,000 m).

It is often asked if the X.25 protocol can be used in LAN applications, especially now that X.25 large scale integration (LSI) controllers are available. This question can be more readily answered by comparing LAN and X.25 protocol functions using the International Standards Organization Open Systems Interconnection (ISO/OSI) reference model.[2,3] The model was developed to help conceptualize the relationships of various elements in a communications protocol. The access function resides between physical and link level functions, often referred to as a link layer sub-layer (Fig 1). The primary difference is that the concept of a shared medium is foreign to X.25. Addresses at the link level are actually command/response indicators, since it is assumed that pairs of stations have point to point links between them.



The local network access layer implements both the device arbitration and addressing necessary for shared medium operation. Once this layer is chosen and implemented, it is expected that the remaining layers may be used in this new application with little change.

Network topologies

In simple terms, topology is the way in which networks are tied together (Fig 2). Many networks are wired in ring or star configurations in order to eliminate the contention problems that occur when more than one connected device tries to send data at the same time. The primary advantage of the bus topology is easy reconfigurability, more important, perhaps, than its reliability advantage. Costs of improving reliability in a star or ring network, eg, adding redundant subsystems, can be much less than reconfiguration costs of the same network over its lifetime. Reconfiguration is labor intensive, and the cost of labor is increasing at a faster rate than that of reliable electronics.

The security of a broadcast bus system is often questioned by users who are apprehensive of the party line

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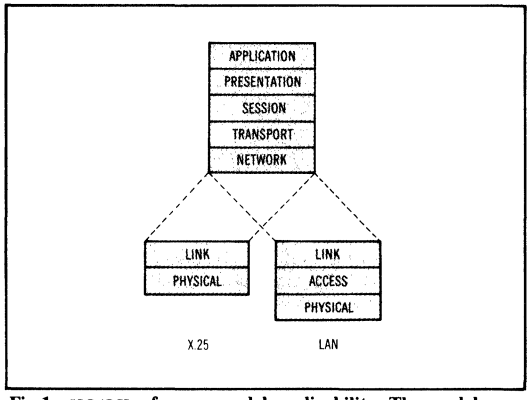

Fig 1 ISO/OSI reference model applicability. The model directly applies to local networks with addition of access layer

concept, where they share a network with diverse user groups. This problem is readily overcome by encrypting the appropriate data on the network. This alternative was at one time unfeasible because of high costs. Now several solutions are made possible by extensive LSI implementation of the National Bureau of Standards data encryption standard, which resolves this obvious problem in bus topology.

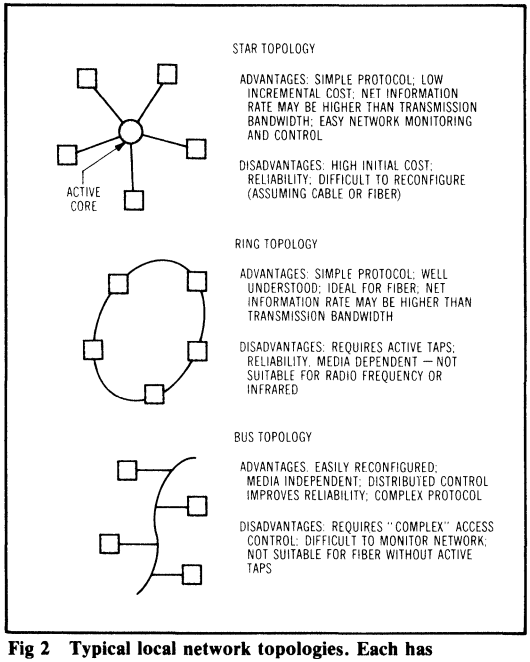

Fig 2 Typical local network topologies. Each has fundamental strengths and weaknesses. Bus topology's efficiency, maintainability, and cost are heavily dependent on access method used

Access methods

Currently the most controversial open question in the local network area is the choice of access methods in LAN buses. An access method is that part of a protocol that coordinates bandwidth use among all network subscribers. It ensures that only one station transmits at a given time, or, if more than one, that proper recovery action is taken to provide correct data transmission. Two common methods for allowing multiple transmission sources on a broadcast medium are frequency division and time division multiplexing (FDM and TDM). Both are fixed assignment schemes and require some centralized network intelligence to assign channels (FDM) or time slots (TDM). There are cost and reliability drawbacks to this centralized scheme. Also, it is difficult to effectively use the communications bandwidth where there are many sporadic data sources, such as word processing terminals. The solution to this lies in a demand access scheme, two of which are currently being promoted.

Carrier Sense Multiple Access (CSMA). In this method a station wishing to transmit listens first for channel clear, and transmits if such is the case. When two stations hear that the channel is clear and transmit simultaneously, a collision occurs. This must be detected and recovered by the CSMA protocol. The simplest type of collision detection requires a higher, usually link level, intelligence to note that a frame has been lost on the network. All frames would be buffered until acknowledged and retransmitted if no timely ACK is received.

Carrier sense multiple access with collision detection (CSMA/CD) is a CSMA implementation that can detect transmission collisions while the data are being transmitted. This enhancement greatly minimizes bandwidth wastage during collisions, but imposes a minimum size restriction on every frame to ensure that collisions are detected (Fig 3). A more serious drawback in collision detection is in its actual implementation. It must detect two simultaneous transmissions (a station's receiver must "listen" for others while its own transmitter is "talking"). Transceiver design is critical. Special cable and cable taps are often needed to minimize noise and impedance problems. Special installation and grounding practices that have been developed may necessitate additional training of cable installers and modifications to building codes. All these constraints have recurring cost implications. So, while many solutions have been implemented, some are costly, and each is media/speed dependent. Several different systems using CSMA/CD are commercially available. The most notable is Ethernet, a joint offering of DEC, Intel, and Xerox.[3,4]

The CSMA scheme is comparatively simple and has enjoyed much academic research, but it has some shortcomings. In the pursuit of simplicity, visibility of network errors and the potential for future upgrade have been sacrificed. Since CSMA allows and expects collisions on the transmission medium, it is difficult for diagnostic equipment to distinguish expected errors from those that are induced by noise or faults. Determinism, or the ability to guarantee the successful (no

collision) access of a station within a fixed time interval, cannot be accommodated in a CSMA environment.

Office automation, which is not real time and therefore CSMA compatible, is a major local network market. Process control, the other major application category, requires absolute delay limits and reliability guarantees. Both markets can be addressed with the same "standard" protocol and access method only if the needs of both are met. The token access method is a way to accomplish this.

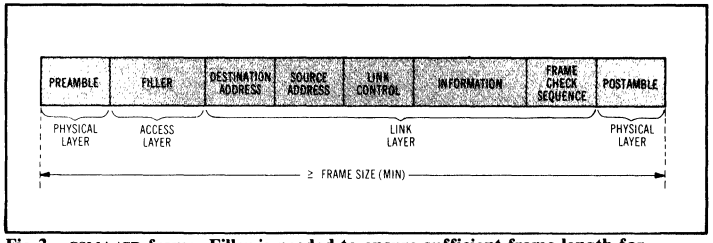

Fig 3 CSMA/CD frame. Filler is needed to ensure sufficient frame length for collision detection. Minimum frame length is function of propagation delay through maximum length of medium

Token passing. A token is an exclusive right, held by exactly one station at any given instant, to initiate transactions on the medium. Distributed network intelligence passes this access right around the network in a logical ring, resulting in an ordered and controlled access method. In the token passing scheme, sometimes referred to as "baton passing," each station sends a message to its access successor when it has finished its transactions (Fig 4).

Control messages are sent in the same format as is information, in frames. At first glance the token access scheme's frames look much like those of CSMA systems as shown in Fig 3. The similarities are purposely at the physical and link layers (Fig 5). The similarity ends with the access field; the required filler in CSMA/CD systems is replaced in the token passing frame with a token control field, usually of one octet.

The required control information could have been coded into the link level control field, but instead is placed directly ahead of the link field. There are three reasons for this. First, it provides adherence to the ISO/OSI model's sense of encapsulation. This says that a given layer must not modify or require the use of any data in a higher layer for its own proper operation. Observing this requirement saves software development and redevelopment as users switch between X.25 and LANs. Second, the ability to send "piggyback" tokens requires separate access and link control fields; link information can go to one station while control is (optionally) passed to another. This is an efficiency enhancement that allows a reduction in the bandwidth used for network management. Third, special format access frames can be sent. Since the access control field may be thought of as defining the rest of the frame (for example, an opcode), very short access frames can be transferred and evaluated without modifying link control programs.

While both access methods are conceptually simple, there are several implementation challenges in the token scheme. These include network initialization, building and maintaining the logical ring (online addition/removal of stations), and the resolution of fault recovery conditions. Centralized and fully distributed are two categories of solutions for these tasks.

The centralized scheme uses an administrative station to watch for and resolve unusual network conditions. Removing this chore from the bulk of the stations simplifies their processing requirements and thus their cost. This administrative method is also generally more expeditious than distributed schemes, since the latter require delays in their distributed algorithms and require all stations to rediscover their part of the network configuration each time.

In the distributed scheme, reliability and ease of configuration are achieved; the network configures itself each time it is initialized. The best of both worlds, speed and reliability, are achieved in the hybrid system. Here the distributed algorithms are retained as backup in case of an administrative failure.

The token protocol makes no assumptions about, or "improper" use of, the transmission medium or transmission rate. Any collisions are treated simply as manifestations of noise and are consistently handled as exceptions. No expected collisions mean no confusion as to cause, resulting in improved maintainability and serviceability. The use of strictly "inband" signaling allows true media independence. Radio frequency, infrared, CATV, baseband coaxial, fiber, and other broadcast media are usable with no change in the access algorithm or any sacrifice of efficiency. This flexibility will be useful as data rates and distances grow and as new transmission technologies are developed.

Inband signaling also means that existing components and technology can be used. This gives network

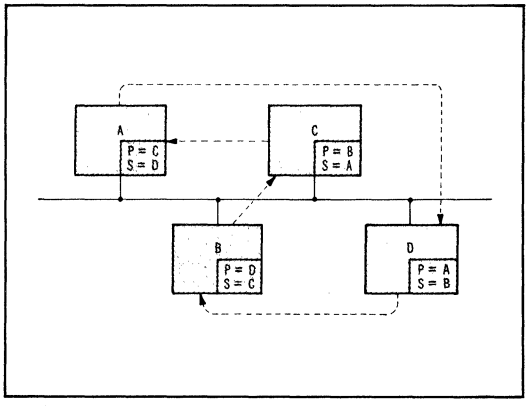

Fig 4 Model of logical ring. Each station has sufficient intelligence to receive and validate tokens from its predecessor (P) and send tokens to its successor (S). Physical ordering of stations is not relevant. Dashed lines indicate control flow

implementors the option to capitalize on established production efficiencies and low costs such as are represented by CATV components. From the use of existing broadcast technologies follows the applicability of existing regulations and trained cable installers.

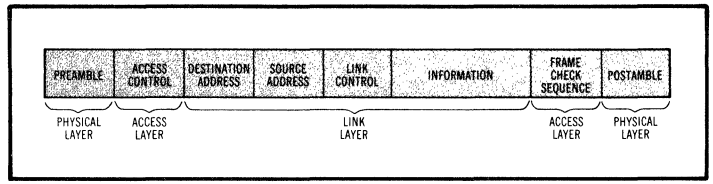

Fig 5 Token frame. Separate access control field allows option of passing control to one station while sending link level information to another

Token protocol's insensitivity to transmission speed is another important factor. It is unreasonable to assume that all network users need the same arbitrary data rate, such as 10M bits/s. Users with lesser requirements should be able to scale systems to their needs and budgets. Some CSMA implementations have minimum frame size restrictions that are directly based on the data rate and the physical length of the medium, to say nothing of the cost of multi-megabit hardware. There is no reason that a few cathode ray tube terminals cannot be linked together with inexpensive twisted pair cable, using the same token protocol and controllers as those used in applications with higher speed requirements.
tions with higher speed requirements.

Depending on the application, networks must either be fair (where all stations have equal access to the medium), or include some priority mechanism. The token access method supports both conditions by being generically fair, but also allows tuning of network and station parameters if desired. Features such as sending "n" frames while holding the token are easily supported. This allows prioritization of stations where some may be allowed to transmit more than others before giving up the token. The network may be set to guarantee access to all nodes within strict time boundaries, as required in control applications.

If tokens solve all LAN problems, why is there any controversy? The answer to this lies in the real and perceived complexities of the token access scheme.

Is token complexity worth it?

Complexity considerations must be evaluated on two fronts: technical (Can it be implemented reliably?) and economic (Is any additional incurred cost justified?). Intensive efforts by individual companies and standards groups have yielded some commercial offerings and several technical proposals. The token access method has been reviewed and evaluated by academicians, network implementors, and users. With the systems, models, and documents available today, it can safely be said that the token scheme is implementable.

The LSI developer is challenged to deliver this complex protocol at low cost. With such an LSI controller, a day can be envisioned when users need be as little concerned about low level network protocols as they are today with bit locations and formats on floppy discs. Efforts in protocol design are nonrecurring, but the benefit of a sophisticated, forward-looking design course will manifest itself more and more as network requirements grow.

Algorithm details and standardization

In the general token scheme just described, detailed algorithms vary depending on the system and design requirements. Choice of an initialization algorithm, for example, depends heavily on the address range allowed in the network: a 48-bit address range uses a different station sort scheme than does an 8-bit range. Work on the distillation of these tradeoffs is underway by standards committees and commercial organizations.

Standardization is key to volume manufacture of token controllers and to the interconnectivity of multivendor equipment. Standardization also advances the development of network diagnostic equipment and tools.

Summary and conclusions

A new science requires fresh consideration of engineering challenges. The needs of users and the progress of implementation technology, especially LSI, can be projected. There is no reason to accept any scheme simply because it exists, as proposed in References 5 and 6. Professional skill and judgment must be used in selecting all elements of any system, especially one as new and with such potential impact as the local area network.

The general token access scheme enjoys current commercial use, generality, and expandability that make it a truly useful standard. Investment costs in up-front complexity will be continually reduced with further LSI developments and as network uses proliferate.

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LOCAL NETWORKS

Token passing cashes in with controller chip

Token-passing protocols can upgrade a data-communication system, especially if a dedicated controller relieves the host from token-processing tasks.

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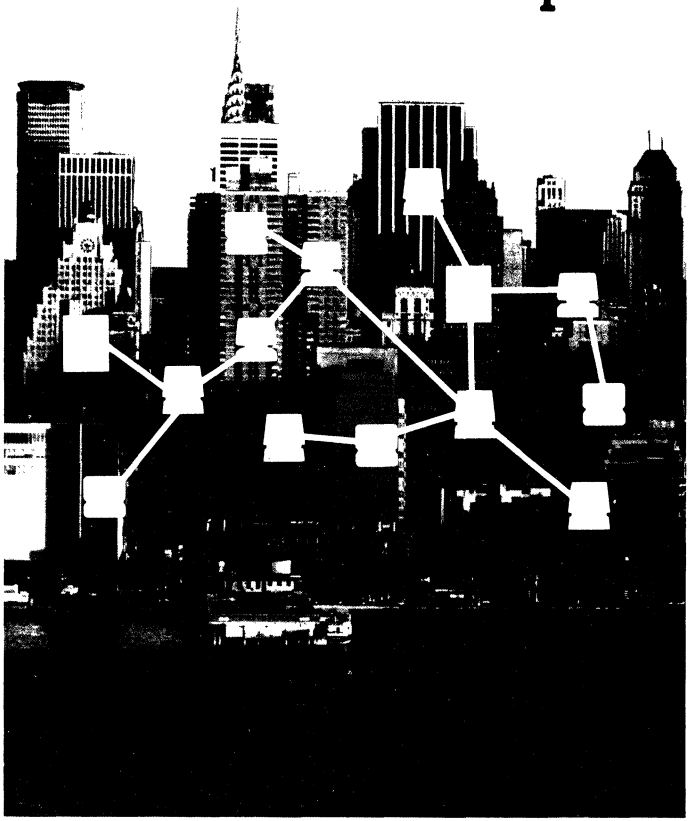

Designers can now implement a distributed-access token-passing systems without worrying about the complex details involved in the communications protocol. Those are taken care of by one LSI chip, called the token-access controller.

Token passing is one method of sharing a communications path. It enjoys the benefits of distributed-access systems while eliminating the drawbacks of schemes employing carrier-sense multiple access with collision detection (CSMA/CD). Until recently, however, token-passing techniques had little currency because of their need for complex controllers. This need relegated tokens primarily to proprietary uses. (For a complete review of local networks, including token-passing techniques, see "Broad Standards, Many Implementations Are on the Way," ELECTRONIC DESIGN, Sept. 30, p. 87.)

The introduction of Ethernet in 1980 marked the beginning of commercial local networks using distributed-access techniques. A distributed system does not rely on a single device for polling. Early versions of Ethernet were designed to use simple controllers because most of the development work began in the 1970s, before the LSI era. Although CSMA/CD offered a simplified access protocol, users incurred cost, performance, and flexibility penalties. Progress in LSI technology has now given designers the benefits of complexity—increased efficiency and enhanced flexibility—but without high cost.

The availability of the WD2840 token-passing controller chip brings token-access communications capability to a range of critical-process applications that were previously unsuited to the token method.

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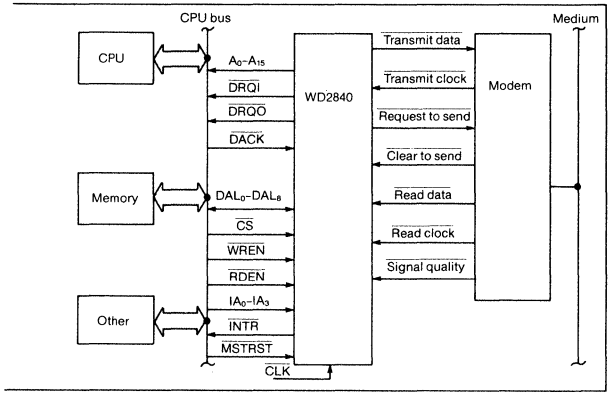
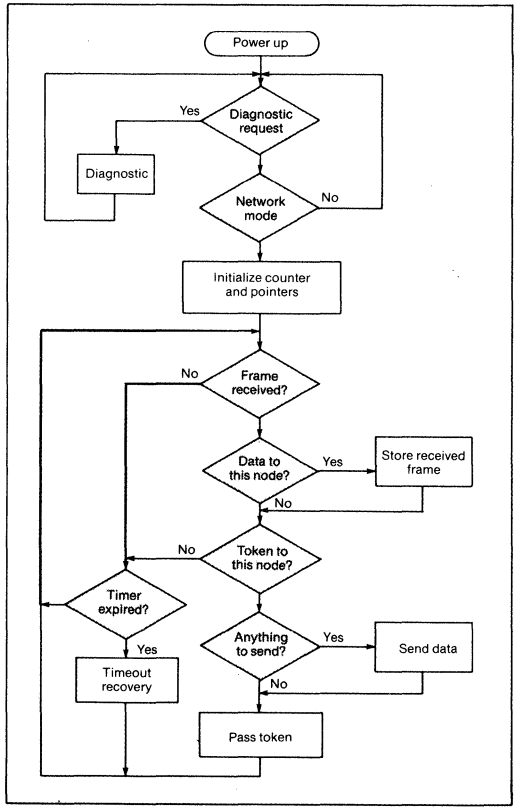


1. Two interfaces connect the WD2840 token-access controller chip to a local-area network. The network side (medium) is electrically conventional, whereas the host side (CPU) combines both a control and status register and a direct-memory-access interface.



2. After initialization, the token-access controller idles in its "watching" loop (bold lines), waiting for a data frame or token addressed to it. The upper portion of the flow chart shows the steps in the initialization procedure.

What's more, the controller sufficiently reduces system communication costs, encouraging its use with very inexpensive end products.

The controller is designed to connect distributed intelligent devices over a shared broadcast medium —usually coaxial cable, free-air radio, or twisted-pair party line. Shared by all stations through the use of a token-passing protocol, the broadcast medium enables each attached device to hear everything on the network. A station is a microprocessor-based device that incorporates the controller. Complementing the token protocol's efficiency is a high-level, software-friendly DMA (direct memory access) interface contained within the controller. In conjunction with conventional hardware and serial communications interfaces, the DMA interface and token protocol make the WD2840 simple to use.

The primary purpose of a token-access controller is to free the designer from data communications concerns. Once the chip is initialized, for example, the host microprocessor need never bother with the protocol; it merely processes frames addressed to it —the controller filters out all others—and generates messages to send later. In fact, it is the controller that sends messages when a token is received. This decoupling of the functions between the network and any user processing simplifies programming and system timing considerations.

Tasks that affect network performance—such as processing tokens and generating acknowledgments —are performed inside the controller. Thus designers can use any type of host processor in a station (Fig. 1). The circuit interfaces with systems in which a processor is busy with a specific application.

Illustrating that point is the microprocessor found in a CRT terminal. Its duties are to scan the keyboard and perform a limited amount of editing. That leaves enough processing power remaining to drive the controller, which handles data flow only for one specific terminal. If the processor falls behind momentarily, just one terminal is affected; all others in the network continue to operate at full speed. Thus a network of controller chips is not slowed by its weakest link.

Token passing in a system environment

When a token-access controller receives a data frame addressed either to itself or to all broadcast stations—there are 254 stations in a system—it transfers the frame to the host's memory via a DMA operation. If the frame is invalid, the close coupling of protocol handling and DMA operations allows the chip to manage its own housekeeping. For example, if errors are detected through a CRC (cyclic redundancy code) or signal-quality check, the memory space is automatically reclaimed.

On the successful reception of a data frame, the controller sets an interrupt and checks to determine whether an acknowledgment was requested by the sending station. If so, it sends the acknowledgment, adding the receiver status, as well. A typical message might be "Received successfully" or "Encountered DMA problem on this end. Please retry." While the controller evaluates each frame as it looks for its own data message, it simultaneously checks for tokens passed to it. This combined token-and-data frame—in which each part can be directed to a different station—is referred to as piggybacking, a feature that increases system efficiency, since most of the overhead associated with conventional token-passing is eliminated (Fig. 2).

Receipt of a token allows the WD2840 to transmit

A three-controller architecture

A single NMOS LSI chip, the WD2840 token-access controller, comprises three major elements: a fast serial communications subsystem, a two-channel DMA controller, and a microprocessor with internal ROM and RAM.

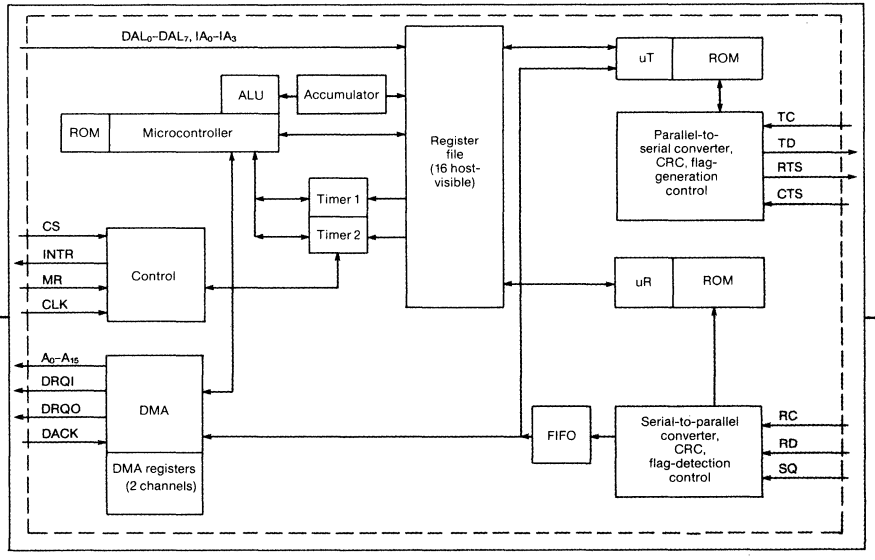
The device's three preprogrammed microcontrollers handle media access and host memory-management functions. This type of architecture facilitates internal parallel processing: for example, prefetching a new buffer address while transmitting or receiving data. Although the token-passing protocol is essentially a half-duplex scheme, separate receiving and transmitting subsystems permit loopback testing.

The primary microcontroller has the capabilities and instruction set of a conventional 8-bit microprocessor, including subroutines, bit manipulation, conditional branching, and arithmetic operations. This part, whose chief task is to implement the token algorithms and maintain the host memory chain, has its firmware located in the internal 1-kbyte ROM. Repetitive and simple operations such as DMA fetching and storing are controlled by the receiving and transmitting microcontrollers.

Two internal timers keep the network independent of the host microprocessor's timing. The first timer is set for a relatively short duration to limit the time it must wait for the required response from a transmission. The second timer has a longer and less critical duration that restricts the period that a network can normally be "idle." Limits on idle time are useful for initialization and some error-recovery operations.

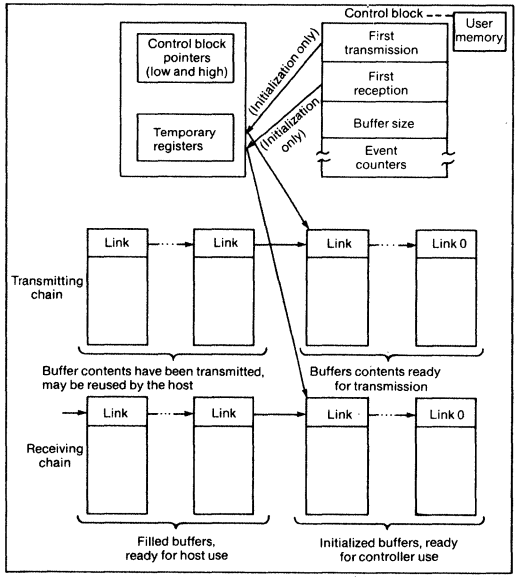
The serial-to-parallel and parallel-to-serial converter block includes standard 16-bit cyclic redundancy code (CRC) checking and generation, along with the framing logic specified by the HDLC (High-level Data Link Control) protocol. Also, the receiver contains an input FIFO buffer to speed internal processing and relieve DMA latency constraints.

Hardware interfacing is designed for flexibility. The DMA interface, for example, uses the familiar DMA request signals as outputs—one for input requested, one for output. Together with a grant signal that both notifies the token-access controller that the bus is available and optionally enables the address drivers, it permits synchronization with slower external memories.

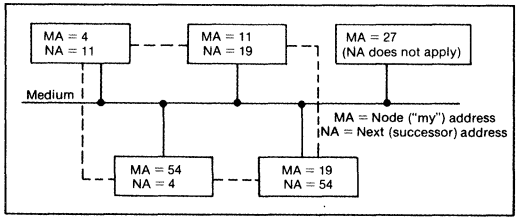


messages that its host has queued. Before transmitting, however, the device checks its internal holdoff register, AHOLT, to determine whether it should defer use of the token on the current cycle. With this optional deference capability, the system designer can bias the intrinsically fair token protocol in favor of selected stations. Those that have more access opportunities have effectively higher priorities.

Key to a token system is the visibility that each station has to network loading conditions. The less often a token is received in a given time, the greater the load on the network. This indication of load data is available to the host as an optional interrupt/token received, and the host can scale down its data over time. Since the host knows the importance of data it sends, it can defer (or set higher delay values in the priority registers) data transmissions of lesser importance to a later time.



3. The chaining technique allows either the host processor or the controller chip to vary the number of buffers in a system. In chaining, buffers are linked so that data frames may span multiple buffers, making memory operations more efficient and simplifies the host's memory allocation tasks.



4. In a logical ring, a token can pass from station 4 (MA-4) to 11, to 19, to 54, and back to 4. The physical order of the ring is irrelevant, since token passing is based only on station addresses.

If transmission proceeds, messages are sent automatically to their appropriate destination addresses, with acknowledgment requests optionally encoded into each frame's header. Such transmissions continue for each frame queued until either a preprogrammed limit or the end of a transmission chain is reached (preprogramming is an optional priority feature). When transmission is complete, the controller passes the token to the next station. After frames having an acknowledge option are transmitted, the transmitting controller awaits a response from the intended receiver. Responses can be positive (indicating that the frame was received correctly), negative, or nonexistent. In the last situation, the receiving station either received the frame incorrectly or was out of service. The waiting period is controlled by an interval timer. If a time out occurs from a no-response condition, the WD2840 automatically retries the transmission.

Automatic retransmissions overcome most network noise glitches quickly and automatically. In this case, the host makes no decisions. If the retry is unsuccessful, the frame is tagged and an interrupt is generated that allows the host to decide the disposition of the frame. To avoid holding up the network, the tagged frame is passed over in the transmission chain and the next frame's transmission is attempted.

A universal device

The WD2840 interfaces with any conventional, general-purpose microprocessor or minicomputer bus. Equally as important as that capability are the chip's contributions to host-speed independence (decoupling) and system efficiency. To achieve these goals, the device combines I/O register programming, interrupts, and dual DMA interfaces for data, exception reporting, and extended control (see "A Three-Controller Architecture").

The memory interface is a self-contained subsystem that consists of two sets of 16-bit registers, byte counters, and DMA control logic. Backing this up is internal intelligence that interprets and manipulates the high-level buffer control structures.

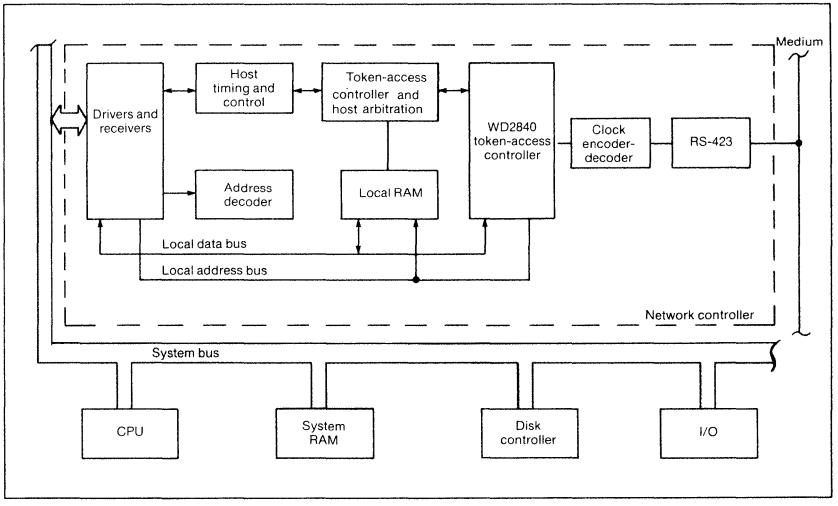
Fetching and storing user data destined for or received from the network are the most important functions of the DMA system. However, these are not simple tasks because of the speed decoupling

needed between the real-time controller and the non-real-time host processes. The WD2840 solves the problem using an open-ended FIFO (first-in, first-out) method of buffer chaining (Fig. 3). In chaining, either the controller or host adds or removes buffers as they consume or generate data, but neither need be concerned about the state of the other.

Though residents of the host's buffer memory, chains are visible to the token-access chip. They are constructed by the host from linked buffers prior to the controller's initialization. Linking the buffers maximizes use of the memory by permitting frames to span multiple buffers, an advantage when most frames are short but long frames must occasionally be accommodated. When receiving a frame, the chip fills the receiving buffer pointed to by an internal register until the frame is complete. If the buffer is filled and the frame is not complete, the device automatically reads the link field of the filled buffer to find the next one available and continues receiving. Of particular importance when interfacing with an existing operating system, this automatic link handling of variable-sized buffers simplifies the host's task of allocating memory.

The transmitting and receiving chains' linked buffers are maintained cooperatively through the use of control fields located in the first buffer of each frame. This header information includes frame status, destination address, and actual frame length in bytes. The length, which determines how many buffers the associated frame spans, is written by the host in the transmitting chain. Each device has its own status bytes and can only read the status of the other device, thus preventing deadlocks.

The control field written by the host is called the frame-control byte and determines what options to put into a frame. An example of a per-frame option is the wait-for-acknowledgment command bit. This bit is tested while the frame is transmitted; if set, it causes the controller to await a response after a frame transmission is complete. The control byte written by the controller is called the frame-status byte. It indicates receiving or transmitting status, including the received "negative acknowledgment,"



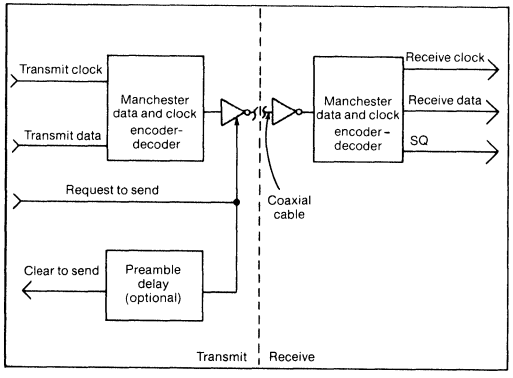
5. A high-performance word-processing application needs a two-ported memory interface between the token-access controller and the local network. This minimizes memory access latency time when the disk controller "hogs" the DMA bus for several consecutive cycles.

if any has been received.

Also contained in the logical memory interface is a series of 8-bit event counters. Located in the host's visible memory in the last section of the WD2840's control block (Fig. 3), they tabulate all noncritical but important network conditions. One such condition is the detection of a transmission error; by the time the host learns of the error, the controller has retransmitted. However, the chip increments the appropriate counter, since the event is valuable to the host for diagnostic purposes.

There are 16 control registers visible to the host (see table). The register file stores initial timer values and such fixed station parameters as station addresses and transmission limits. Included is a pointer to the initial DMA control block, which is used both when initializing the controller and when network exceptions are encountered. The register file also contains locations not visible to the host that are used by the internal controller for scratchpad functions, including the 16-bit pointers to the active receiving and transmitting buffers.

The controller's network (serial) interface accommodates standard modems and clock encoders. The device accepts non-return-to-zero (NRZ) data and permits the transmitting and receiving clocks to be stopped immediately upon completion of a frame if desired. Ordinarily this type of operation is not allowed, as most conventional devices use the clocks to clear the internal shift registers and perform other functions. A pair of request-to-send and clear-to-send signals is available for externally generating preambles for any type of medium.



6. One of the simplest network interfaces is the Manchester encoder-decoder, which operates through an RS-442 bus transceiver. A nonvalid Manchester output signal connects to the controller's signal-quality pin.

Locating errors

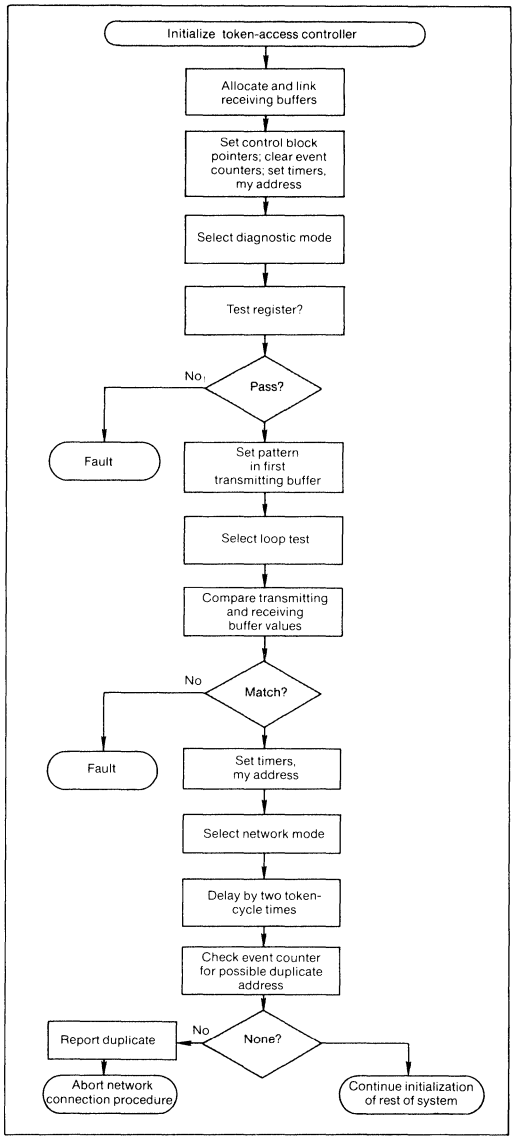
Furnishing the network interface with novel features, the signal-quality input warns the controller that the frame in progress contains an error due to a media, modem, or clock-recovery fault. An example of such a error is the detection of a missed clock transition by a Manchester decoder (see "Manchester II Transfers Data with Integrity, Speed," ELECTRONIC DESIGN, March 19, 1981, p. 233). Coupled with appropriate external logic (optional), this input enhances data integrity beyond that offered by the frame-check sequence included with each transmission.

A common problem in token systems involves the actions necessary if a station is removed or fails; that is, what if the logical ring is broken? Prompt correction of such a condition affects the entire network and is therefore handled autonomously by the controller chip (Fig. 4).

The primary responsibility for assuring that a token arrives at its intended destination rests with the controller chip that sent it. Similarly, if the token does not arrive, the sending device also must retrieve it. To accomplish this, the sending controller sets its short internal timer to indicate the longest time that it must wait for a receiving station to use the token. If the token pass is unsuccessful—time expires on the internal timer without a successful pass—the chip begins error-recovery procedures.

Since the chief cause of these dropped tokens is a station improperly leaving the network, the WD2840 initiates a station scan. First it polls the address space for an active station to which it can pass the token. When one is found, the chip then updates its successor register so that the poll need not be repeated on the next cycle. After the logical ring is restored, the host is informed by means of a new-successor interrupt.

The WD2840 incorporates several types of diagnostics that are necessary in conventional intelligent subsystems and LSI systems. Network-level tests provide confidence and maintainability for the distributed token-access system and its associated medium and modems. System tests validate local interfaces, such as external RAM and the interrupt



7. Initializing the token-access controller is necessary before a host processor can access a local network. The procedure includes buffer allocation, building a linked receiving chain, and performing diagnostic testing.

subsystem, and internal tests validate the chip itself, including the internal controllers and register file. All three diagnostics are used cooperatively.

As a new station powers up—or attaches itself to the network for any reason—it tests itself before transmitting on the network, thus ensuring that any faults do not disrupt the operating network. Self-testing is initiated by the host, which interprets the results. The host must be involved because an LSI device cannot always find and report its own failure.

Network testing occurs continuously. For example, a token-access controller watches for frames transmitted on the network by another station having the chip's own address as its destination. Source stations having the same address are prohibited from a token network. If that occurs, there is usually a hardware failure in the station or a misconfiguration (setting DIP switches incorrectly).

Local networks in word processing

A common application of a distributed network is multiple-user word processing. A typical system consists of a combined file server and print station connected to several remote CRT terminals. Each node contains its own processor and controller, and all communicate via the network. The CRTs are essentially "dumb" terminals having hardware modifications and internal firmware extensions that permit network use. The most critical station is the file server.

CRT terminals can be added or removed from the network while it operates. Either the control chip in each station or the host software configures the network. The choice depends on the speed with which new stations must be admitted and the tolerance of the network to access delays. This application tolerates delays of about 100 ms, so a simple token-access–control polling method is used.

The file server has a two-ported memory interface that minimizes memory access latency resulting from the disk interface's so-called hogging mode. Controllers that retain the DMA bus for several consecutive cycles are in the hogging mode. The two-ported memory is physically located on the network interface module and appears logically in the host processor's address space (Fig. 5).

The host interface matches the timing of the normal microcomputer bus to that of the controller and its local memory. This includes the memory-mapping logic of the host's operating system. Arbitration logic controls access to the local RAM and ensures that simultaneous memory requests by the host and controller do not end in improper memory operations or timing deadlocks. The logic is designed for FIFO-type command priority, with ties awarded to the controller.

The media interface here is implemented in its simplest form: a Manchester encoder-decoder chip and an RS-449 (three-state) bus transceiver (Fig. 6). That device handles its own preamble generation and detection at the start of each frame, so that the clear-to-send pin of the controller is tied directly to its request-to-send pin. Even more, the Manchester part provides a nonvalid Manchester output that is tied to the controller's signal-quality input.

Simple modems of this type are suitable for operation over moderate distances—about 1 km at a 1-Mbit/s transmission rate using twisted-pair cable. Other commercially available modems use more elaborate techniques to increase message reliability and distance or for other types of media.

The software interface with the host's file manager has three phases: initialization, file transmission, and command reception. The controller's initialization and network maintenance routines are included in the operating system. The software receives incoming frames from the WD2840, checks for proper frame sequencing, and builds messages that are compatible with normal operating-system file requests.

Before the operating system can access the network, the controller must be initialized. That process consists of allocating buffers, building an initial linked receive chain, and performing self-diagnostics. The flow chart shown in Fig. 7 gives the sequence of events. After diagnostics are complete, the host's initialization routine clears the event counters and writes the address of the chip's control block into the latter's internal registers. It then stores the proper values in the controller's registers (station addresses, priority values, timer settings) and puts the chip into the network mode.

A driver removes the incoming frames from the receiving chain and then ties them into the operating system in response to a controller interrupt. These messages are then separated into network management and information request groups. Network management frames serve primarily for the orderly addition and removal of stations. The file server periodically polls the network address space to allow new members in, but all stations process station-removal requests as they occur. There are many ways to maintain a network, each having a tradeoff between simplicity and timeliness. For this application, new stations need not be added very rapidly, allowing for greater simplicity.

Information requests always include a sequence number added by the controller's driver. These numbers are used in conjunction with the chip's automatic acknowledgment and thus ensure data integrity: the controller makes certain that no requests are lost, and the driver filters possible duplicates. The resultant messages are then removed from the controller's receiving chain and reformatted (including blocking if needed) before being passed to the filer. As a background task, the receiver driver initializes and attaches any free buffers returned by the file manager to the head of the chain for future use. Moreover, the operating system can add new buffers to the pool as the load increases.

Transmission is initiated after the filer obtains previously requested data. The information is passed to the network data, which then formats it into controller-compatible buffers, adds the correct sequence number and destination address, and finally attaches it to the transmitting chain. As its background task, the transmitting driver periodically checks the chain for buffers that can be returned to the transmission pool. This is an option that can be performed whenever a frame-transmission interrupt occurs. □

A summary of register files

Register	Name	Function
0	CR0	Control register 0
1	CR1	Control register 1
2	SR0	Status register 0
3	IR0	Interrupt register
4	SR1	Status register 1
5	SR2	Status register 2
6	CTR0	Temp counter
7	NA	Next address
8	TA	Acknowledge timer
9	TD	Network dead timer
A	CPBH	Control block pointer (most significant byte)
B	CPBL	Control block pointer (least significant byte)
C	NAR	Next address, request
D	AHOLT	Access hold-off limit
E	TXLT	Transmit limit
F	MA	My address

Token-access controller minimizes network complexity

MARK STIEGLITZ, Western Digital Corp.

Users can benefit from the increased speed this transmission method provides

In a data-communications network, contention among stations trying to get through to the central computer is inevitable. One of the more effective procedures to eliminate this contention is a form of distributed polling known as token passing. Despite its effectiveness, however, token passing has not been very popular with system integrators. Most network architects have been intimidated by the complexity of the algorithms required to set up the station linkages and to recover from network exception conditions, and have settled for less complex control methods. A new LSI token-access controller (TAC) residing in each station of the network minimizes this complexity for network designers.

A token is a message granting a polled station the temporary but exclusive right to transmit on the medium, a right the station must then relinquish to the next designated station. This method has been historically used on sequential media on which access sequence is implied by the physical interconnection, but tokens can also be used on broadcast media such as baseband coaxial or CATV systems by assigning unique addresses to each station or node (MA: "my address") and passing transmission rights between them (Fig. 1).

The simplicity and non-reliance on quirks of a medium make token methods superior for use on a wide array of applications. Relatively simple (from the data-movement viewpoint) applications such as file transfer to the complex time-critical applications of factory automation are supported with the same access

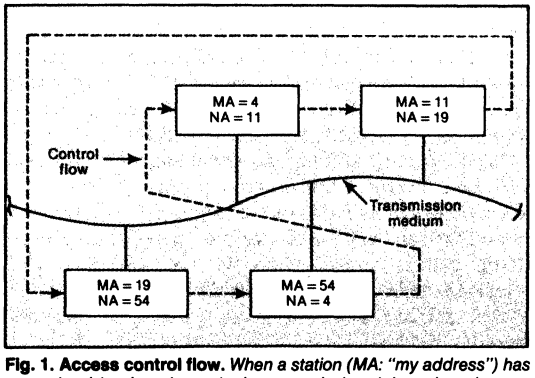


Fig. 1. Access control flow. *When a station (MA: "my address") has transmitted its data, it sends the transmission rights—the token—to the station identified in the next address (NA) register. Station numbers are in ascending order but need not be sequential for network efficiency.*

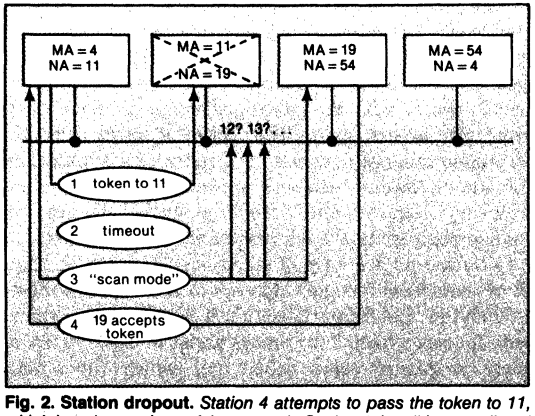


Fig. 2. Station dropout. *Station 4 attempts to pass the token to 11, which has dropped out of the network. Station 4 then "times out" and scans for another station to which it can pass the token, finding 19.*

TAC must handle three main exception conditions: network initialization and recovery from failed nodes, addition of stations to the access ring while the network is in use and recovery from an error situation in which two or more tokens have been generated on the network.

protocol. Also, data rates optimized for the application, not mandated by the network implementation, are possible with the same LSI network controllers.

TAC's tasks

TAC must handle three main exception conditions: network initialization and recovery from failed nodes, addition of stations to the access ring while the network is in use and recovery from an error situation in which two or more tokens have been generated on the network.

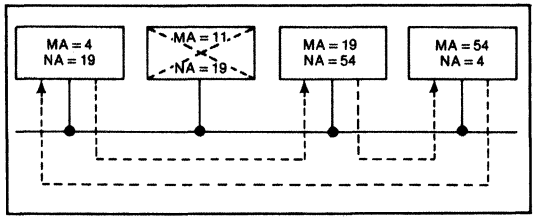


Fig. 3. Station patched out. *Station 11 is logically removed from the network when station 4 changes its next address (NA) register to 19. Thus, station 11 no longer consumes network time.*

Initialization and recovery

Initialization is setting up the network's token linkages and determining the correct values for registers in all TACs wanting to be part of the access ring (desiring INRING status). Failed-node recovery refers to the network restart when a token is lost or damaged.

Token loss results from exception or expected conditions. Error cases may be a product of noise hits on the transmission medium corrupting the token message, or simply a controller failure. A token loss usually occurs with the intentional removal of a station from the access ring. The ratio of noise hits to controller failures depends on a network's application and administration, but both are recovered identically. Recovery requires the detecting station to set its linkage register to the address of an active station.

Initialization is a form of failed-node recovery in that all of the access linkage registers of the network must be updated. Before initialization it is not known which node follows which. Two timers assist in these cases: a fairly long-time value called TD, which times out network inactivity and a shorter timer called TA, which is the maximum turnaround time required for a response (token or data) to be sent by the receiving station of a previous message. These timers are user settable and depend greatly on a network-transmission rate, and to a lesser extent, on an application. The timers work together and are the key to solving the initialization and failed-node challenges.

Two manifestations of a failed node can occur. One happens when a token holder tries to pass the token to the next station in the ring. If the next station does not respond to the token, the token-passing station soon knows because it knows how long it should take for a node to pass the token or to send a data message (time TA). In this case, the node that tries to pass the token has primary responsibility to recover. It does so by entering a scan mode from an access level, and polling the network for another successor.

Assume that station 11 (Fig. 2) is removed from the network and station 4 is attempting to pass the token to it. Station 4 will time out because 11 does not respond to the token within time TA and will attempt recovery by passing the token to station 12. Station 12 will not respond because it also is not present, which will cause

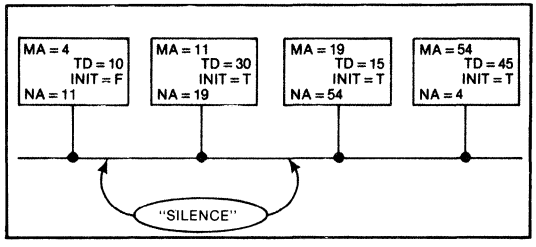


Fig. 4. With no token, there is no transmission. *All stations detect this and start internal timers. When one expires and has the proper control bit enabled, it restarts the network. TD is the station-inactivity timer. INIT is a switch that, when false (F), tells TAC not to attempt recovery regardless of TD. When INIT is true (T), TAC attempts to initialize the network after there has been no activity for duration of TD.*

station 4 to try 13. This "polling" continues by station 4 until it finally gets to 19. Station 19 will respond, causing station 4 to update its next address register (NA) to 19, bypassing station 11. The next time station 4 gets the token, it immediately passes it to 19 (after sending any messages).

At this stage, station 11 is logically removed from the network, or "patched out" (Fig. 3). If station 11 wants to get back into the network later, the standard station-adding procedures must be followed.

This station-by-station access polling consumes network time (each poll takes TA time), and may appear to be an inefficient use of network bandwidth. But this is a rare error-recovery case. Further, it is handled completely and autonomously by the TAC, which at least bounds the delay. The host μp is not burdened with this critical task and, as a result, does not slow the recovery procedure.

The second failed-node manifestation occurs when a station holding the token itself fails before it has a chance to pass the token to another. If station 4 has the token (Fig. 4) and dies before passing it, no activity

Additional stations can be added to an operating token network at any time. The distributed method does not rely on a specific station. Thus, there are no problems or efforts spent selecting the administrator.

occurs on the network and no station has the short timer (TA) running. All stations, however, have the timer TD, or network dead timer, running. The station whose TD timer expires first takes recovery responsibility.

To simplify network administration, not all stations must be able to reinitialize the network. The first station whose network timer TD times out tests the control bit "INIT," saying, in effect, "when timer TD expires, should I claim the token?" If INIT is false, the station waits, as does every other station, for a station's TD to expire that has INIT true.

One station on the network's timer TD that has the ability to initialize will eventually expire. That station will claim the token and send its messages, or send the token to its successor station as directed by its NA register. Thus, if station 19 happens to have the shorter timer TD and has its initialize enable bit set (Fig. 3), station 19 assumes the token, sends whatever messages it had queued and sends the token to station 54.

On receiving the token, station 54 (Fig. 4) sends its messages and tries to pass the token to station 4. If station 4 has recovered from its problem (its failure caused this recovery condition), it receives the token and transmits with it.

If station 4 still does not transmit, station 54 has primary recovery responsibility (54 has started its timer TA) and will enter the scan method. The scan starts at station 5 and searches until it finds the next available on-line station (11 in this example).

The power-up initialization case behaves in the same manner. As stations come up, they wait for a message or for their timer TD to expire.

Host software is responsible for setting up the next address register before enabling the transmitter in the TAC. This is set to the station address plus one (which will in effect cause a polling by that station) or, if it has some prior knowledge of what the network configuration looks like, it sets NA to reflect the correct address of the successor. Host software is also responsible for setting the time-out values in the recovery timers (TA and TD). The value for TA should be consistent among all stations of a network, but TD is not critical, and thus may vary greatly because it is used only in exception situations.

For example, there can be half a dozen stations on the network that are intended to recover from catastrophic conditions such as loss of token. These stations can all have substantially different time values TD so that if a couple of them are not on-line at a time, one will come up and reinitialize the network.

Additional stations can be added to an operating token network at any time. If a supervisory communication path can be assumed, a candidate station requests of the administrator that it be admitted to the access ring. This approach is not unlike the method pay-TV companies use to enable new subscribers' decoder boxes. When installed, a service representative of the cable-TV company telephones (the supervisory communications method) the central site, which then sends the properly addressed enabling signal over the network. While this method is efficient from the network viewpoint (the infrequent control messages are handled "out of band"), such duplicate communications schemes do not usually exist.

A more acceptable solution is to allow the control communications to share the data bandwidth. To avoid data collisions and retain the prized asset of a token system—determinism—new stations are added on a controlled-polling basis. To accomplish this, the TAC requires the host to initiate the test for a new station. Although, in this case, host interaction is required to expand the network, that interaction doesn't set back the goal of autonomous TAC network control in that adding stations is not a real-time requirement. The time to add a new station is not critical to the performance of the rest of the network.

There are three primary methods by which a station can be added to a network. The first is a distributed method, in which each station in the network can poll for new stations in the gap between its address and the next address (between MA and NA). Second is a centralized method, in which an individual station designated by the network architect can interrogate the entire address space seeking a new station desiring INRING. The third—central seam—is a simpler (from the host point of view), centralized method in which a station can send a global frame causing all the on-line TACs to reset their next address register. This causes each TAC to poll its address space at its next token-pass attempt. Each method has advantages and disadvantages.

The distributed method does not rely on a specific station. Thus, there are no problems or efforts spent selecting the administrator, nor is there any concern about backup administrators. In the distributive method, each station has the same responsibility to allow new access members as other stations. This method is the most host intensive and requires each station to maintain a timer (that can be configuration set as to its value) as to how often it should poll its gap for new stations.

For example, assume the timer in each station is 5 sec. and that station 4's timer has expired (Fig. 5). The host attached to station 4 notes that the next address register (NA in the TAC) is set to 11, which indicates that a new station might be added to the network as station number 5, 6, 7, 8, 9 or 10.

A token is a message granting a polled station the temporary but exclusive right to transmit on the medium, a right the station must then relinquish to the next designated station.

The host queues a frame into the TAC transmit chain, polling station 5. This frame will be sent by 4 with an acknowledgement requested from 5. If 5 is present it responds; otherwise, the TAC aborts its attempt after time TA. The TAC marks the result on the frame in the host memory space and proceeds with other tasks.

After this exchange, the host, at its leisure, checks

IMPLEMENTING TAC

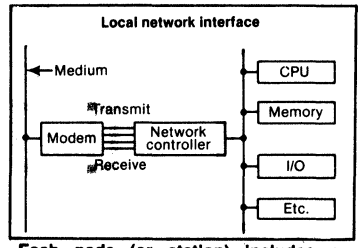
The TAC is a single-chip NMOS LSI device that performs all real-time communication tasks in a μp-based system. The assumed existence of a μp allows some less critical, non-network performance-affecting tasks to be performed outside the TAC, such as flow control and adding new stations.

Removing these functions from the device results in:

- Less processing power, which, in turn, makes the chip smaller and less expensive;
- No processing burdens, enabling the TAC to respond faster to network conditions, thus improving efficiency;
- Saved firmware space and processing power, which can be used for internal diagnostics and a more sophisticated host interface—a chained frame buffer scheme, which is a trade-off in favor of system efficiency.

To meet the network requirements and to include the other features expected in LSI, such as internal validation, a three-processor design was used consisting of a primary microcontroller, a receiver and a transmitter.

The primary microcontroller performs all token-algorithm support such as network initialization and error recovery, manages host interrupts and coordinates internal and system diagnostics. It also evaluates the host commands and arms and supervises the receiver and transmitter microcontrollers.



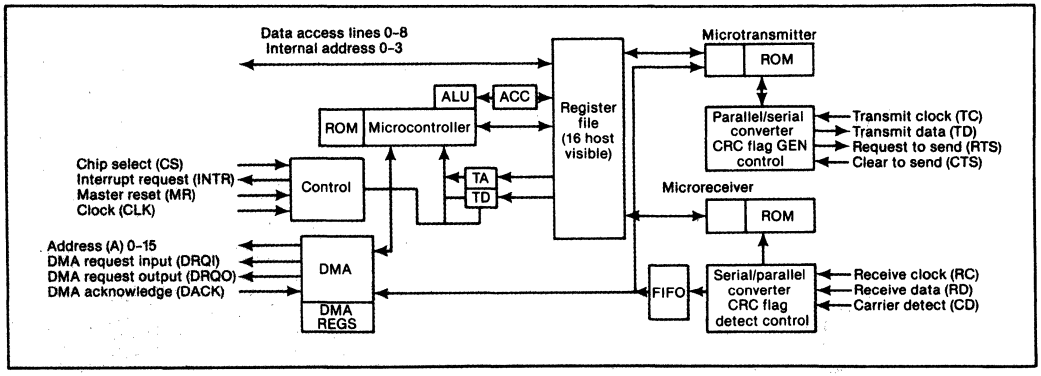
Each node (or station) includes a modem, *a network controller (TAC: token access controller) and appropriate hardware as required by the application ("host").*

The receiver does minor frame (group of bytes) filtering and frame validation and, independently of and simultaneously with the primary controller, performs DMA operations storing incoming data. The transmitter sends data via its DMA interface when allowed by the main controller, that is, when a token is received.

The register file is used by the host to set memory pointers, network address registers, long-term parameters such as frame transmit limits (allowing users to select exhaustive or non-exhaustive transmission) and the conventional command, status and interrupt indications. The TAC's primary interface to the host is its DMA system. Data to and from the network and options selectable on a frame-by-frame basis are read in this manner.

The half-duplex network interface has standard RTS/CTS handshakes. Another feature of the receiver is a signal-quality input that allows errors that are easily detected by the modem (such as a missing clock detected in a Manchester decoder or low carrier in a broadband system) to be signaled to the TAC. The use of these low-level checks further enhances the basic frame integrity beyond that of the CRC.

Messages are sent between stations on the network in frames. The frame structures are similar to the industry standard HDLC; delimiters are unique flag patterns with zero insertion used for data transparency. In addition to adding the required control fields to support the token protocol, the TAC recognizes three basic frame types: a short token pass frame, a short frame conveying only acknowledgement and control information and variable-length frames holding user information and optional network control information.



TAC includes three processors implemented in a single LSI device *that interfaces with the host through a register file and a DMA subsystem.*

In the centralized station addition method, a single station can poll the entire address space, seeking a new station that desires INRING.

the transmit status of the frame. The host sees that the frame acknowledgement timed out, meaning that station 5 has not been added to the network, or that station 5 is on the network and whether the request INRING is set in the network code field. In either case, the host takes appropriate action. If the desired INRING bit is set, station 4 changes its NA register to 5, allowing its next token to be passed to 5. This action puts station 5 in the ring.

Depending on an application's sophistication, a control message can be sent to station 5. That message says, "Your successor is X." In this case, X = 11, so that 5 is not forced to poll for its successor. In any case, 4 updates its next address register to 5 and does not need to go through this distributive polling cycle again

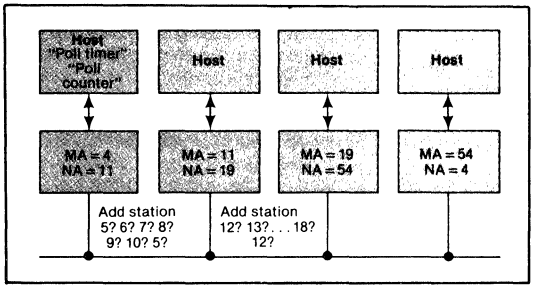


Fig. 5. Distributed polling. *Each host polls the gap in its address space for the possible addition of new stations. The host internal poll timer and poll counter set the polling rate and range as desired.*

because there is no gap between 5's address and the next address; there is no possibility that a new station can be inserted between addresses and 5. If 5 didn't respond to 4's poll, station 4 updates its poll counter so that the next time that the poll timer times out, station 6 will be tried.

If node 6 responds, its desired INRING bit is tested as above. If 6 does not respond, the host will queue a poll to station 7 the next time its poll timer expires. This continues until the host completes 10, when the cycle goes back to 5 and repeats. In this example, with a gap of 6 stations (between 4 and 11), and with a 5-sec. clock, a new node can be added within 30 sec.

In the centralized station-addition method, a single station can poll the entire address space, seeking a new station that desires INRING. One reason for centralizing this function might be the more careful control that can be placed in a network. There can also be optimizations. For example, the central polling station can keep track of the stations that already exist and, therefore, bypass some address ranges. A polling station may know the network will never have more than, say, 75 stations. In the example of Fig. 6, when station 4 starts polling, it polls only to address 75 before resetting to zero. This works like the distributed method except that a single station does all the work.

When the polling station determines that a station has been added, it must place the new station in the access ring. For example, station 4 is the centralized station doing all the polling (Fig. 6), and it discovers that station 27 has recently been added. Station 4 knows this because station 27 now responds to a first-time poll, and because its status bit is set, indicating that it wants to be added to the ring. (Some stations may be receive only, never desiring the right to initiate transmissions.) Station 4 sends a high-level message to the software in station 19, telling it to change its next address register to 27. This message

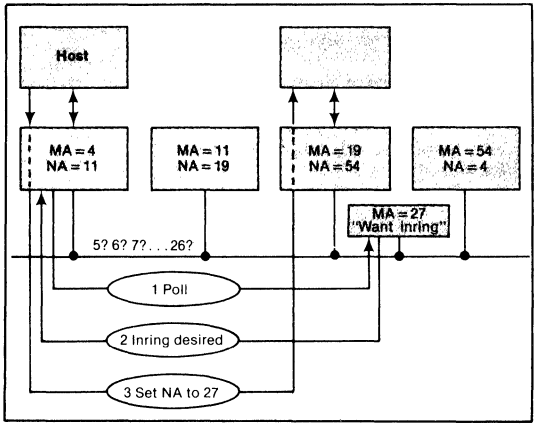


Fig. 6. Central polling. *A single station—in this case, station 4—dubbed "the administrator," can be charged with all polling tasks. This simplifies the software in the other stations and centralizes network control.*

can also prompt station 19 to tell 27 its next address register should be 54. This gets confusing, but it is all done with high-level software. These tasks are not real time and are quite efficient from the network point of view.

Station 4, the administrator, need not create and maintain a table of active stations on the network because the poll response returns three pieces of information. As node 4 polls the stations on the network, it finds out (a) that the polled station does not respond at all, as it would if it polled station 12 in Fig. 6; (b) that the station is already part of the network and is already in the ring or is receive only, as it would if station 4 happened to poll station 11 or 19; and (c) whether the station is attached to the network, is alive and wants to be in the ring, as is the case with a poll to 27. These indications are conveyed by a combination of status bits sent back by the acknowledge frame. This acknowledge frame and status information are transferred at a TAC device level, so a host is not concerned with whether its station wants to be in the ring. The host simply sets up the proper bits in the control

To simplify network administration, not all stations must be able to reinitialize the network.

registers; the bits are relayed automatically by the TAC. Thus, with a simple algorithm, an administrative station can poll the entire network address range and know the network's exact membership and status.

Central scan

Central scan is the simplest method of adding stations to a network. It involves sending a global frame to all stations on the network, which forces each to update its own next address register to its station address plus one (NA = MA + 1). Assume station 4 is the centralized station and sends the scan command frame (Fig. 7). Station 11, upon receiving it, automatically sets its next address register to 12 (the TAC does this; the host is not involved but is notified of the situation). Also, station 19 sets its next address register to 20, and station 54 sets its NA register to 55.

The result of this is a round of polling at the TAC level. Station 11, on completing its use of the token, tries to send it to 12. The token to station 12 times out because 12 is not present. Station 11 reclaims the token trying to send it to 13 and so on, causing 11 to poll for station addition. The drawback of this is the huge time disruption incurred by the simultaneous polling.

It is not required that station 4 send this scan control frame to all stations at the same time. If it is known that station 11 exists in the network and that a station may be trying to add into the network after station 11 in the address space, a command can be sent to 11 telling it to set its next address register to 11 + 1. Now 11 will go through scanning station 12, 13, 14 ... again without intervention from station 11's host software. This directed scanning has the effect of smoothing the polling disturbance over a greater time.

The trade-off of all these methods is the software complexity distribution. If a TAC user assumes more responsibility, providing more intelligence distributed in the software, the system can be more sophisticated in handling new stations. If a user wants the TAC to handle this task itself, saving host software development, he pays only slightly in inefficiency. TAC gives the user an option.

Recovery from multiple tokens

Multiple tokens are not allowed on a token bus because their presence causes a breakdown of the orderly nature of the protocol. Their presence can only be the result of a combination of exception and hardware failure conditions but, once present, must be handled immediately.

The primary defense against multiple tokens is prevention. The control algorithms and the frame formats have been designed to minimize multiple tokens. For example, the TAC can refuse to allow a

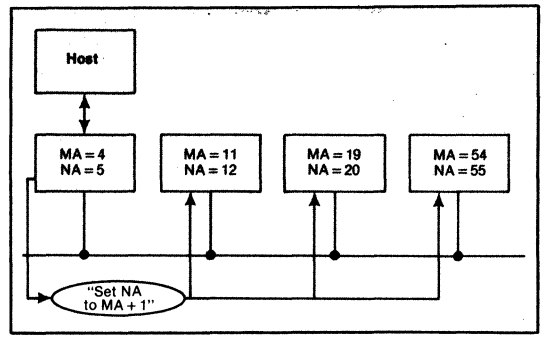


Fig. 7. Central scan request. *A special command can be sent by any station causing all attached TACs to set their NA register to the address of the next possible node. This causes each TAC to poll without the help of the host.*

piggyback token (a single frame containing both the token and a user-information field) with the data-acknowledge option. If this were allowed, conditions could result in which the data was negative acknowledged by its receiver and retransmitted, but the token arrived successfully at its destination—in this case, twice—creating two tokens.

Duplicate tokens, or at least network confusion, can result from more than one station having the same network address. Unless the stations are receive only, their simultaneous responses to data frames and tokens will probably result in their response not being accepted. While conceptually simple to prevent, address duplication can be the result of hardware failure (a bad DIP switch), operator error or configuration error (if a device is moved from one network to another).

Because the access controller must monitor the network for messages addressed to itself anyway, it is simple to check for messages sent by a station with its address (most frames contain both a source and a destination address). Part of a host's attachment algorithm would normally check this counter in the TAC before allowing it to transmit anything, thereby catching most of these duplicate station faults before they have a chance to affect the network.

A token access controller can also detect duplicate tokens by knowing that, when it has the token, no other station can transmit. This ability is supported in the TAC by incorporating separate receive, transmit and control sub-controllers. This allows the receiver to monitor the medium while the primary controller is, for example, searching the host's memory for a frame to be sent. If another token exists or is suspected, the TAC drops its token, allowing the other to circulate. If there is no other token, the network is left in a no token state and is easily restarted with the aid of recovery timer TD. ■

Mark Stieglitz is manager, local networks, Western Digital Corp., Newport Beach, Calif., and chairman of the IEEE committee working to set a token-passing protocol standard.

ADVANCE INFORMATION

WD4028 NetSource/PC-LAN™ Local Area Network Controller

FEATURES

- IBM PC™ COMPATIBLE
- TOKEN PASSING PROTOCOL FOR PREDICTABLE PERFORMANCE
- RING TOPOLOGY
- AVAILABLE WITH MS-DOS™ COMPATIBLE SOFTWARE
- RELIABLE OPERATION OVER 10,000 FEET AT 1.0 MBITS/SEC (1000′ MAX BETWEEN ADJACENT STATIONS)
- UP TO 254 NODES PER NETWORK
- LOW COST TWISTED PAIR CABLE
- INCLUDES 64 KBYTE PACKET BUFFER
- NBS ENCRYPTION AVAILABLE ON-BOARD
- EASILY INSTALLED

DESCRIPTION

The WD4028 PC-LAN is the Western Digital interface board for the IBM-PC™ Personal Computer. It is the first of a family of Local Area Network board level products from Western Digital. The NetSource/PC-LAN board provides a fast, reliable, yet inexpensive means for interconnecting a variety of different microcomputer systems. The basic design of the network combines a unique cable interface method with a new Western Digital LSI network control processor, the WD2840 Token Access Controller.

The network processor (WD2840) used in all PC-LAN boards is designed by Western Digital Corporation to handle the major communications tasks as they relate to the local ring network token passing protocol. These tasks include network initialization, addressing, data transmission, acknowledgments, and diagnostics. In addition, global addressing and dynamically alterable station priority is supported.

Communication with the Host is accomplished through a dual port memory included on the PC-LAN board. This 64 Kbyte memory is used as a FIFO for all data sent and received via the ring network, with the WD2840 Control Processor managing the data pointers.

ARCHITECTURE

The following is a brief description of the hardware functions included on the PN-IBM interface card:

Network Control Processor — The WD2840 is the heart of the PC-LAN Interface board. This device consists of three individual processors plus the micro-code containing the token passing algorithm (see WD2840 data sheet).

Data Buffer — This part of the circuitry includes the 64Kx9 RAM and the associated control logic for storing both the incoming and outgoing data packets.

Peripheral Logic — The three main peripheral devices shown here are the PPI parallel interface, the Programmable Timer, and the optional Data Encryption device. The PPI reads the user programmed node address straps on the board and provides additional control outputs used by the Cable Interface. The timer is available for use by higher level software interface routines for such functions as a security. Finally, a population option is available on the board for the addition of a high speed data encryption device (WD2001) for use with networks requiring data security.

Cable Interface — Since this portion of the circuit determines the reliability of the network, the cable interface for the PC-LAN was designed very carefully. In particular, circuitry is included to permit uninterrupted operation even in the presence of high ambient electromagnetic noise (typical of industrial environments). Circuitry is also included to automatically bypass any network node from which power is removed. For encoding the data on the network, a Manchester type Modem is used. This restricts the information content of the signal to a single octave of bandwidth. This increases the signal-to-noise ratio, minimizing distortion due to non-linearities within the cable, and permitting complete DC isolation between nodes.

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IBM-PC is a trademark of International Business Machines Inc.

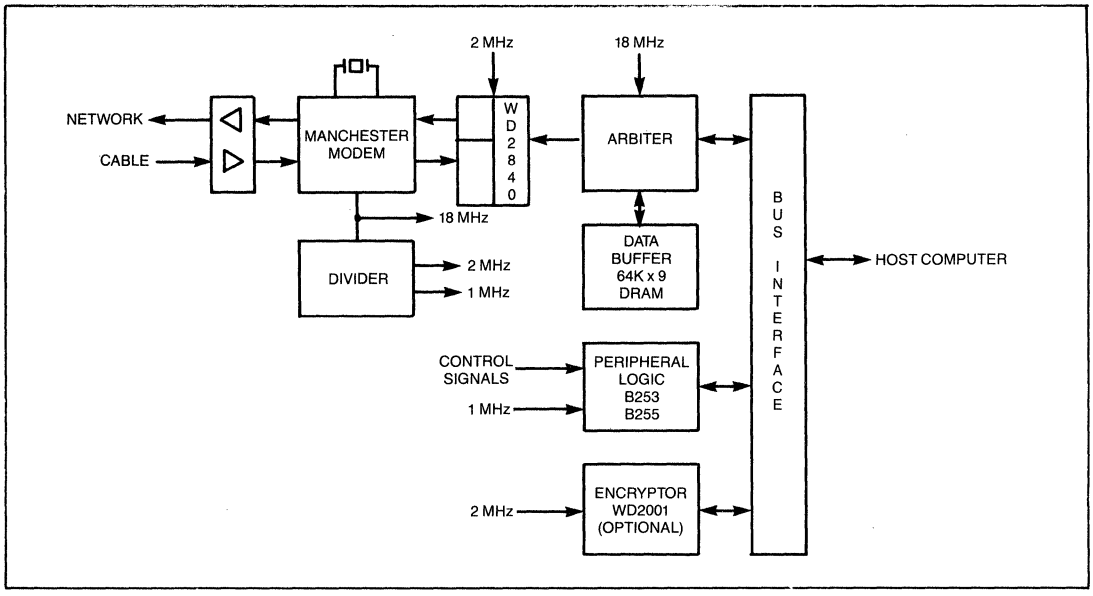

FIGURE 1. WD4028 PC-LAN SIMPLIFIED BLOCK DIAGRAM

BUS INTERFACE

The Bus Interface consists of Address Buffers, Data Buffers, and Control Buffers. These buffers isolate the PC-LAN from the Host bus and prevent the bus from overloading.

ARBITER

The PC-LAN uses custom logic devices to create a dual-port memory, allowing access to the Data Buffer by both the Host and the Network. Because of the real-time nature of the Network, the WD2840 has priority over the Host for access to the buffer. If the Host requests access while the WD2840 is accessing the memory, the Host is given WAIT states until the WD2840 releases the buffer. The WD2840 interleaves its accesses in such a manner that the Host is never denied access for more than about 1 microsecond at a time. WAIT states are generated only when the Host is accessing the PC-LAN Buffer Memory or Control Ports.

DATA BUFFER

The Data Buffer consists of nine 64Kx1 dynamic RAMs. A standard delay line timing control circuit is used to assure maximum reliability.

The Data Buffer appears to the Host as a contiguous 64K byte block of read/write random access memory that is addressable in the 90000H-9FFFFH range.

WD2840 NETWORK BOARD CONTROL PROCESSOR

The WD2840 Token-Access Controller is comprised of three major elements: a fast serial communications subsystem, a two-channel DMA controller, and a microprocessor with an internal ROM and RAM.

The device's three pre-programmed microcontrollers handle network access and Host memory-management functions. This type of architecture facilitates internal parallel processing, for example, prefetching a new Buffer Address while transmitting or receiving data. Although the token-passing protocol is a half-duplex scheme, separate receiving and transmitting subsystems permit loopback testing.

The primary microcontroller has the capabilities and instruction set of a conventional 8-bit microprocessor, including subroutines, bit manipulation, conditional branching, and arithmetic operations. The primary microcontroller, whose chief task is to run the token algorithms and maintain the Host memory chain, has its firmware located in the internal 1-kbyte ROM. Repetitive and simple operations (i.e. DMA fetching and storing), are controlled by the receiving and transmitting microcontrollers.

The control ports of the WD2840 are addressed at 280H-28FH.

MODEM

A CMOS HD6409 Manchester Modem device is used to encode data on the cable. The use of Manchester code restricts the information content of the signal to a single octave of bandwidth (f to 2f); thereby increasing the signal-to-noise ratio, minimizing distortion

(because of the nonlinear frequency response of the cable), minimizing group delay distortion, and permitting complete DC isolation between the nodes (if desired).

LINE DRIVERS AND RECEIVERS

The PC-LAN uses a unique line driver/receiver arrangement to permit uninterrupted operation in the presence of high ambient electromagnetic noise (typical of industrial environments).

A differential current mode line driver switches a constant low current (approximately 10 mA) between a pair of conductors and uses the shield for return. The resultant current in the shield is constant and does not radiate. Although the current in the pair is constant, the locus of the current moves slightly as the current is switched from conductor to conductor; however, the change in the locus is small, causing minimal radiation which is trapped by the shield. The overall result is a cable that radiates far less than traditional coax or twisted pair. Radiation is so low that two pairs of conductors operate within the same shield with no cross-coupling.

A differential line receiver is used to detect the received signal. This receiver provides 3 to 5 volts of common mode noise rejection and detects differential signals of 30 to 40 millivolts.

CABLE CONNECTION

The transmission line is terminated at the receiver with its characteristic impedance (100 ohms) to minimize reflection noise.

D-type 9-pin connectors are used to interconnect the PC-LAN nodes. Live pins connect to the cable (two pair plus one to the shield) to improve ground conductivity and minimize common mode noise problems. Two of the remaining pins are used to detect unplugged cables.

Having one male and one female connector at each node prevents improper cable installation and allows cables to connect to cables as well as to nodes for use as extensions.

BYPASS

High reliability relays are included to automatically bypass any network node which has power removed. These relays can also be de-energized under program control should self-diagnostics determine that the node has developed a fault.

PARALLEL PORT INTERFACE (PPI)

The Parallel Port Interface device provides three 8-bit ports that are used as follows:

Port A — Controls outputs to the cable interface and interrupt circuits.

Port B — Node address input (8 bit binary value).

Port C — Status inputs: interrupts and cable interface.

The PPI is addressed as ports 290H-293H.

PROGRAMMABLE INTERVAL TIMER (PIT)

Two channels of the PIT Programmable Interval Timer device are available for use by high level software interface routines for functions such as a Watchdog Timer. These two channels are cascaded to provide for a 32-bit time interval generation or measurement. The timer is clocked at 1 MHz.

The pit is addressed as ports 294H-297H.

ENCRYPTION

The optional WD2001 Data Encryption device can be used to provide high speed data security services. The WD2001 is addressed as ports 298H-299H.

CLOCK GENERATION

The modem device is also used as the master oscillator for the PC-LAN. The Modem device uses a 16 MHz crystal, and provides a high frequency clock for the Modem and the Arbiter. A portion of the custom logic circuit is used to divide the 16 MHz to 2 MHz for the WD2840 (Network Controller) and WD2001 (Encryptor), and to 1 MHz for the PIT.

RING TOPOLOGY

The unique topology chosen for the PC-LAN combines the best features of the commonly used Ring (IBM) and Bus (Ethernet) topologies. The result is a system with the low cost and high reliability of the Ring, but with the flexible topology of the Bus.

Physically, the network nodes are interconnected using pre-assembled lengths of cable having a 9-pin male connector at one end, and a 9-pin female connector at the other. Each node also has two 9-pin connectors; one male and one female. The user installs the system by simply interconnecting the nodes together in a daisy chain fashion as shown in Figure 2.

Electrically, the network resembles a Ring configuration with each node regenerating the signal. This eliminates cumulative noise and signal attenuation problems which can severely limit the size and reliability of bus oriented networks.

The network cable itself consists of two twisted pairs with an overall shield. This permits the separation of the Send and Receive signals, so that data flows in only one direction in each signal pair.

Each network node located at the physical end of the cable (or Cable Branch) has a termination plug connected to the unused 9-pin connector(s). These plugs are wired such that the two cable pairs are tied together, thus completing the ring.

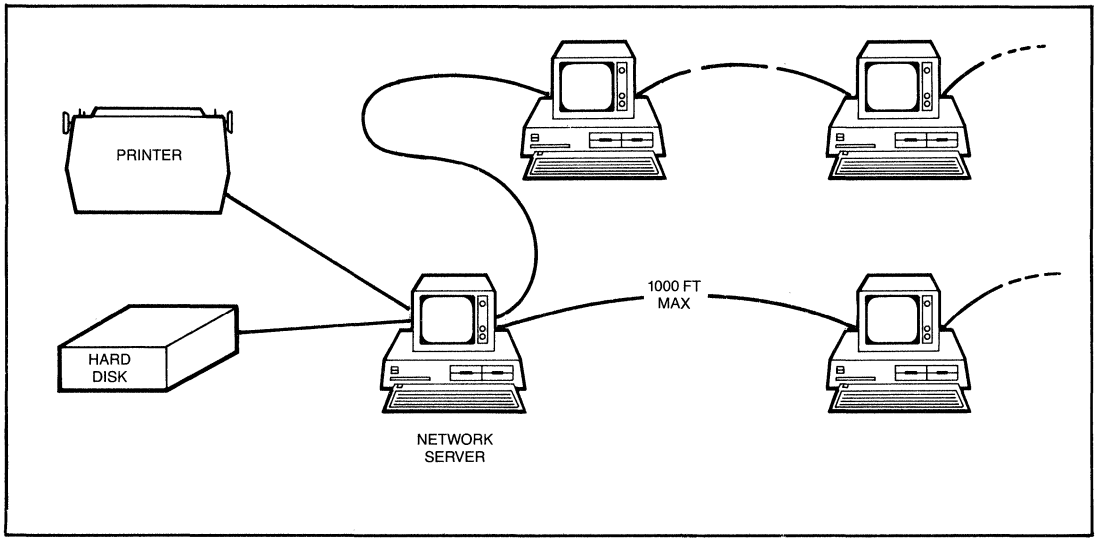

FIGURE 2. PC-LAN SYSTEM RING CONFIGURATION

SPECIFICATIONS

Physical:

width: 4.25″ (10.8 cm.)
Length: 13.32″ (33.8 cm.)
Thickness: .60″ (1.5 cm.)
Weight: 11 oz. (312 g.)

Network Cable Type:

Belden 9855/UL 2582 (standard)
Belden 89855 (Plenum)

Cable Connectors:

9-pin male D-type
9-pin female D-type

Cable Interface:

Impedance: 100 ohm balanced
Min. signal level: 25 mv differential
EMI susceptibility:
2 volts/meter from 10 kHz through 30 MHz
5 volts/meter from 30 MHz through 1 GHz
RFI emission:
Complies with Part 15, Subpart J of FCC 47 CFR

Computer Interface:

Power:
+5VDC (±5%)
+12VDC (±5%)
−5VDC (±5%)
Bus compatibility: IBM PC, Compaq, etc.

Environmental:

Operating Temperature 0 to +55°C
Relative Humidity to 90% (without condensation)

Network Specifications:

Data Rate: 1.0 Mbit/sec
Packet size: 1 to 4095 bytes
Access Protocol: Token Passing
Maximum number of nodes: 254
Buffer size: 65536 bytes + parity
Buffer access: dual port RAM
Maximum length: greater than 10,000 ft.
Maximum dist. between nodes/repeaters: 500 ft.
Frame format: similar to HDLC
Error detection: CRC16-CCITT (16 bit CRC)

Address Space Required:

Memory: 65536 bytes contiguous; selectable on any 64Kbyte boundary
Ports: 280h through 29Fh inclusive
Interrupts: optional; one required if used
DMA: Provided by 2840; IBM channels not used

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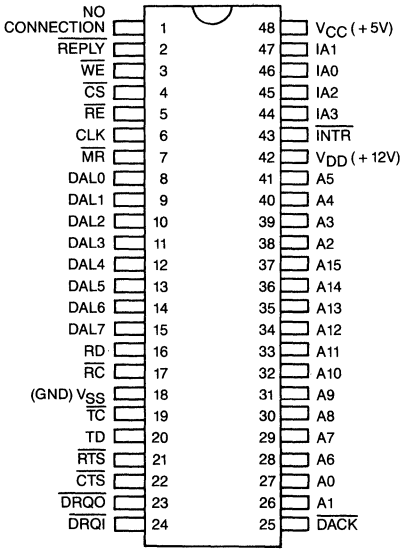
PRELIMINARY

WD2511 X.25 Packet Network Interface (LAPB)

FEATURES

- Packet switching controller, complies with CCITT Recommendation X.25, level 2, LAPB.
- Programmable primary timer (T1) and retransmission counter (N2).
- Programmable A-field which provides a wider range of applications than defined by X.25. These include: DTE-to-DTE connection, multipoint and loop-back testing.
- Direct memory access (DMA) transfer: two channels; one for transmit and one for receive. Send/receive data accessed by indirect addressing method. Sixteen output address lines.
- Zero bit insertion and deletion.
- Automatic appending and testing of FCS field.
- Computer bus interface structure: 8 bit bi-directional data bus. CS, WE, RE and four input address lines.
- DC to 1.1 MBPS data rate.
- TTL compatible.
- 48 pin dual in-line packages.



PIN DESIGNATION

DESCRIPTION

The WD2511 is a MOS/LSI device which handles bit-oriented, full-duplex serial data communications with DMA, which conforms to CCITT X.25's LAPB with programmable enhancements.

The device is fabricated in N-Channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.

APPLICATIONS

X.25 PACKET SWITCHING CONTROLLER
PART OF DTE OR DCE
PRIVATE PACKET NETWORKS
LINK LEVEL CONTROLLER
STORE AND FORWARD SYSTEM
HIGH REL POINT TO POINT COMMUNICATIONS
BIT ORIENTED PROTOCALS WITH BUILT IN DMA

INTERFACE SIGNALS DESCRIPTION (All signals are TTL compatible.)

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
1		No Connection	Leave pin open.
2	$\overline{\text{REPLY}}$	Reply	An active low output indicates the WD2511 has either a $\overline{\text{CS}}$•$\overline{\text{RE}}$ or a $\overline{\text{CS}}$•$\overline{\text{WE}}$ input condition.
3	$\overline{\text{WE}}$	Write Enable	The data on the DAL are written into the selected register when $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are low.
4	$\overline{\text{CS}}$	Chip Select	Active low chip select for CPU control of I/O registers.
5	$\overline{\text{RE}}$	Read Enable	The contents of the selected register is placed on DAL when $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low.
6	CLK	Clock	Clock input used for internal timing. Must be square wave and should be greater than 500 KHz.
7	$\overline{\text{MR}}$	Master Reset	Active low initializes the chip. All registers reset to zero, except control bits MDISC and $\overline{\text{LINK}}$ which are set to 1. $\overline{\text{DACK}}$ must be stable high before $\overline{\text{MR}}$ goes high.
8-15	DAL0-DAL7	Data Access Lines	An 8-bit bi-directional three-state data bus for CPU and DMA controlled transfers.
16	RD	Receive Data	Receive serial data input.
17	$\overline{\text{RC}}$	Receive Clock	This is a 1x clock input. RD is sampled on the rising edge of $\overline{\text{RC}}$.
18	V_{SS}	Ground	Ground.
19	$\overline{\text{TC}}$	Transmit Clock	A 1x clock input. TD changes on the falling edge of $\overline{\text{TC}}$.
20	TD	Transmit Data	Transmit serial data output.
21	$\overline{\text{RTS}}$	Request-To-Send	An open collector (drain) output which goes low when the WD2511 is ready to transmit either flags or data.
22	$\overline{\text{CTS}}$	Clear-To-Send	An active low input which signals the WD2511 that transmission may begin. If high, the TD output is forced high. May be hard-wired to ground.
23	$\overline{\text{DRQO}}$	DMA Request Out	An active low output signal which initiates CPU bus request so the WD2511 can output data onto the bus.
24	$\overline{\text{DRQI}}$	DMA Request In	An active low output signal which intitiates CPU bus request so that data may be input to the WD2511.
25	$\overline{\text{DACK}}$	DMA Acknowledge	An active low input from the CPU in response to $\overline{\text{DRQI}}$ or $\overline{\text{DRQO}}$. $\overline{\text{DACK}}$ must not be low if $\overline{\text{CS}}$ and $\overline{\text{RE}}$ are low or if $\overline{\text{CS}}$ and $\overline{\text{WE}}$ are low.
27, 26, 38-41, 28-37	A0-A15	Address Lines Out	Sixteen address outputs from the WD2511 for DMA operation. If the control bit ADRV is 1; the outputs are TTL drives at all times. If ADRV is 0, the outputs are three-state, and are HI-Z whenever $\overline{\text{DACK}}$ is high. (ADRV is in Control Register #1.)
42	V_{DD}	Power Supply	+ 12VDC power supply input.

INTERFACE SIGNALS DESCRIPTION CONTINUED (All signals are TTL compatible.)

PIN NUMBER	SYMBOL	PIN NAME	FUNCTION
43	$\overline{INTR}$	Interrupt Request	An active low interrupt service request output. Returns to high when Status Register #1 is read.
46, 47, 45, 44	IA0-IA3	Address Lines In	Four address inputs for CPU controlled read/ write operation of the I/O registers in the WD2511. If ADRV = 0, these may be tied to A0-A3. (ADRV is in Control Register = 1.)
48	V_{CC}	Power Supply	+5VDC power supply input.

ORGANIZATION

Note: See appendix D for a glossary of terms used throughout this document.

A detailed block diagram of the WD2511 is shown in Figure 1.

Mode control and monitor of status by the user's CPU is performed through the Read/Write Control circuit which reads from or writes into I/O registers addressed by IA0-IA3.

Transmit and receive data are accessed through the DMA control. Serial data is generated and received by the bit-oriented controllers.

Internal Control of the WD2511 is by means of three internal microcontrollers; one for transmit, one for receive, and one for overall control.

Parallel transmit data are entered into the Transmitter Holding Register (THR), and then presented to the Transmitter Register (TR) which converts the data to a serial bit stream. The Cyclic Redundancy Check (CRC) is computed in the 16-bit CRC register, and the result becomes the transmitted Frame Check Sequence (FCS).

Parallel receive data enters the Receiver Holding Register (RHR) from the 24-bit serial Receiver Register (RR). The 24-bit length of RR permits stripping of the FCS prior to transfer in to the RHR. The receiver CRC register is used to test the validity of the received FCS. A 3-stack FIFO is included in the receiver.

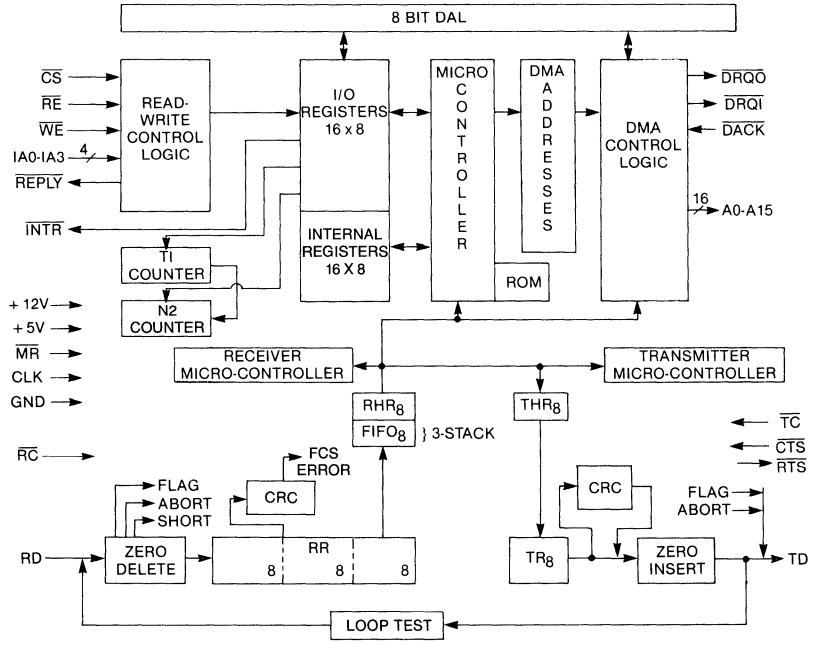


Figure 1 WD2511 BLOCK DIAGRAM — DETAILED

FRAME FORMAT

The WD2511 performs "bit-oriented" data communications control. According to the general format for bit-oriented procedures (HDLC, SDLC, ADCCP), each serial block of data is called a frame.

Each frame starts and ends with a Flag (01111110). A single flag may be used both as the closing flag of one frame and the opening flag of the next frame. In between flags, data transparency is provided by the insertion of a 0 bit after all sequences of 5 contiguous 1 bits. The receiver will strip the inserted 0 bits. The last 16-bits before the closing flag is in the Frame Check Sequence (FCS). Each frame also includes address and control fields (A and C fields).

The FCS calculation includes all data between the opening flag and the first bit of the FCS, except for 0's inserted for transparency. The 16-bit FCS has the following characteristics:

Polynomial = $X^{16} + X^{12} + X^5 + 1$
Transmitted Polarity —Inverted
Transmitted Order —High Order Bit First
Preset Value —All I's

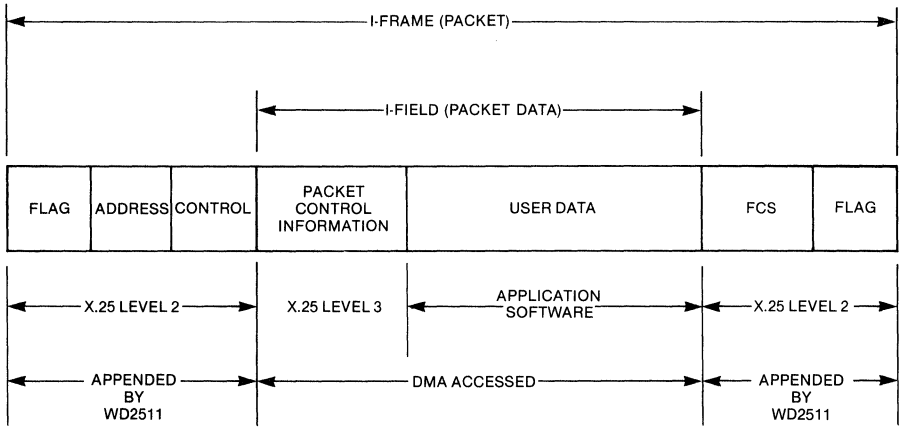
After the frame is received, if there were no errors then the remainder in the CRC register (internal in the WD2511) will be:

1111000010111000 F0B8

The WD2511 generates and tests the Flag, FCS, A-Field, C-Field, and performs zero bit insertion and deletion.

According to the X.25 protocol, there are three types of frames: supervisory (S-frame), un-numbered (U-frame), and information (I-frame). The WD2511 performs frame level (level 2) link access control. All S- and U-frames are automatically generated and tested by the WD2511. The user need only be concerned with the I-frames, which are packets.

The WD2511 will transmit contiguous flags for interframe time fill (full duplex mode).



X.25 MODE

NOTE: X.25 Level 1, is the Physical Interface

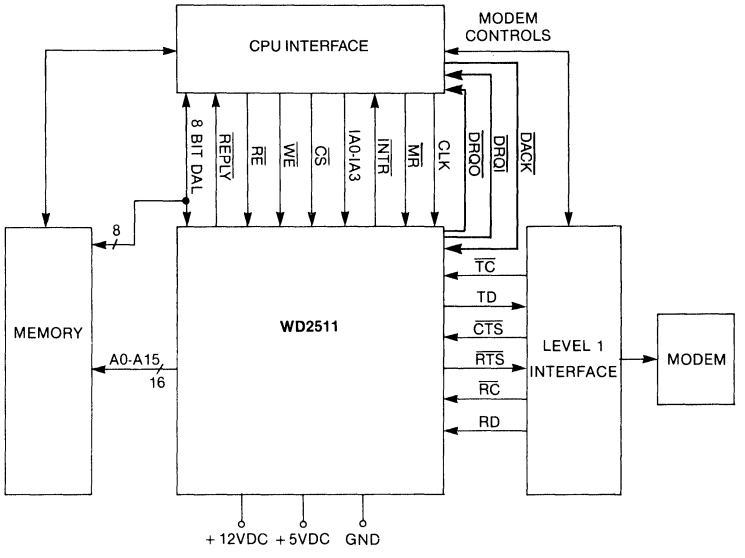


Figure 2. SYSTEM CONNECTION

II. PROGRAMMING THROUGH REGISTERS

The WD2511 is controlled and monitored by sixteen I/O registers.

Control, status, and error bits will be referred to as CR, SR, or ER, respectively, along with two digits. For example, SR16 refers to status register #1 and bit 6, which is "XBA."

REGISTER DEFINITION

REG #	IA3	IA2	IA1	IA0	REGISTER	REGISTER GROUPING
0	0	0	0	0	CR0	OVERALL CONTROL AND MONITOR
1	0	0	0	1	CR1	
2	0	0	1	0	*SR0	
3	0	0	1	1	*SR1	
4	0	1	0	0	*SR2	
5	0	1	0	1	*ER0	
6	0	1	1	0	*CHAIN MONITOR	RECEIVER MONITOR
7	0	1	1	1	*RECEIVED C-FIELD	
8	1	0	0	0	T1	TIMER
9	1	0	0	1	N2/T1	
A	1	0	1	0	TLOOK HI	DMA SET-UP
B	1	0	1	1	TLOOK LO	
C	1	1	0	0	CHAIN/BUFFER SIZE	
D	1	1	0	1	NOT USED	
E	1	1	1	0	XMT COMMAND "E"	"A" FIELD
F	1	1	1	1	XMT RESPONSE "F" (Note 1)	

*CPU READ ONLY. (Write Not Possible)

NOTE:
1. Registers E and F should be set-up while MDISC = 1.

CONTROL, STATUS, ERROR REGISTERS

REGISTER	BIT # 7	6	5	4	3	2	1	0
CR0	$\overline{\text{ADISC}}$	0	H/$\overline{\text{F}}$	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	RAMT	RECR	MDISC
CR1	TXMT	TRCV	$\overline{\text{XI}}$	ADRV	0	0	0	SEND
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX
SR1	1PKR	1XBA	1ERROR	0	NE2	NE1	NE0	0
SR2	T1OUT	IRTS	REC IDLE	0	0	0	0	$\overline{\text{LINK}}$
ER0	ER07	ER06	ER05	ER04	ER03	ER02	ER01	ER00

1 Causes Interrupt ($\overline{\text{INTR}}$ Goes Low).

CONTROL REGISTER 0

REGISTER	CR07	CR06	CR05	CR04	CR03	CR02	CR01	CR00
CR0	$\overline{\text{ADISC}}$	0	H/$\overline{\text{F}}$	ACTIVE/ $\overline{\text{PASSIVE}}$	LOOP TEST	RAMT	RECR	MDISC

BIT	DESCRIPTION
CR00	MDISC (mandatory disconnect command) MDISC will cause a logical disconnect in the link. No DMA accessed data will be transferred as long as MDISC = 1. After Master Reset, MDISC will be set. The WD2511 will neither transmit nor accept received data until MDISC = 0.
CR01	RECR (Receiver Ready) indicates the CPU's is receiver buffer is Ready (CR01 = 1). If RECR = 1, the WD2511 may begin receiving I-frames. (See SR00)
CR02	RAMT — Internal Register Test when set. (See Self Tests)
CR03	The LOOP TEST bit will connect the transmit data output to the receive data input. The receiver input pins RD and $\overline{\text{RC}}$ are then logically disconnected from the internal circuitry. The "E" and "F" data registers of the A-field must be equal.
CR04	The Active/Passive bit when set, in conjunction with MDISC = 0, will cause the WD2511 to initiate link set-up. When this bit is reset, the WD2511 will wait for a link setup from the remote station.
CR05	H/F selects full duplex if CR05 = 0, and half duplex if CR05 = 1. (See Appendix A).
CR06	Unused control bits should remain at 0.
CR07	$\overline{\text{ADISC}}$ (disconnect) is used when CR04 = 1 (ACTIVE). When the WD2511 actively initiates link set-up, a DISC will be transmitted and acknowledged prior to transmission of the SABM if CR07 = 0. If CR07 = 1, the WD2511 will send only the SABM.

CONTROL REGISTER 1

REGISTER	CR17	CR16	CR15	CR14	CR13	CR12	CR11	CR10
CR1	TXMT	TRCV	$\overline{XI}$	ADRV	0	0	0	SEND

BIT	DESCRIPTION
CR10	The SEND bit is used to command the WD2511 to send the next packet or packets. If SEND = 1, the WD2511 will read from TLOOK the BRDY bit of the next segment for transmission. If BRDY = 0, the WD2511 will clear SEND and no action occurs. If BRDY = 1, the WD2511 will then read TSADR and TCNT, followed by the transmission of that buffer. After transmission, the WD2511 clears BRDY of the segment just transmitted, and reads BRDY of the next segment. If 1, the next segment is transmitted. If 0, the SEND bit is cleared, and transmission of packets is stopped. As a matter of good practice, the CPU should set SEND each time a BRDY bit is set.
CR11-13	Unused bits, write in 0's.
CR14	The ADRV (ADDRESS VALID) bit is the control for the 16 bit output addresses (A0-A15). If ADRV = 0, the outputs are tri-state and are in HI-Z, except when $\overline{DACK}$ is low. If ADRV = 1, the outputs are always low impedance (TTL), and are forced high-level (logical 1) when $\overline{DRQO}$, $\overline{DRQI}$ and $\overline{DACK}$ are all high.
CR15	$\overline{XI}$ — (Transparent I-field) Used when TXMT = 1 $\overline{XI}$ = 0.Frame ⩾ 3 bytes excluding FCS and Flag. $\overline{XI}$ = 1.Frame < 3 bytes excluding FCS and Flag.
CR16	TRCV — Transparent Receive. Receive all frames including unknown frames. See Appendix A.
CR17	TXMT — Transparent transmit. See Appendix A.

STATUS REGISTER 0

REGISTER	SR07	SR06	SR05	SR04	SR03	SR02	SR01	SR00
SR0	NA2	NA1	NA0	RNRR	NB2	NB1	NB0	RNRX

BIT	DESCRIPTION
SR00	RNRX. An RNR has been transmitted or will be at next opportunity. The CPU should set RECR when receive buffers are available.
SR03-SR01	NB2-NB0. Next block to be transmitted.
SR04	RNRR. This bit is set when an RNR frame is received. Once set, it is cleared when an RR, REJ, SABM, or UA is received.
SR07-SR05	NA2-NA0. Next block of transmitted data to be Acknowledged.

STATUS REGISTER 1

REGISTER	SR17	SR16	SR15	SR14	SR13	SR12	SR11	SR10
SR1	$_1$PKR	$_1$XBA	$_1$ERROR	0	NE2	NE1	NE0	0

BIT	DESCRIPTION
SR10	0 (not used)
SR13-SR11	NE2-NE0. Next Expected packet number and next RLOOK segment number.
SR14	0 (not used)
SR15$_1$	The ERROR bit indicates: 1) An error has occurred which is not recoverable by the WD2511 or 2) A significant event has occured. For the specific reason for the ERROR bit being set, see error register (ER0) on next page.
SR16$_1$	The XBA (transmitted block acknowledgement) bit set, indicates that a previously transmitted Block, or Blocks, have been acknowledged by the remote device. Upon acknowledgement, the ACK'ED bit is set to "1" for each segment in TLOOK which was acknowledged.
SR17$_1$	The PKR bit stands for Packet Received. PKR = 1 indicates a packet has been received error-free and in correct sequence according to the received N (S) count. The I-field data has been placed in the host's RAM memory. NE is advanced.

NOTE 1:
The three interrupt-causing bits are SR17, SR16, and SR15. Any of the three will cause an interrupt request ($\overline{INTR}$ goes low). After SR1 is read, all three bits are reset to 0, and $\overline{INTR}$ returns to high.

STATUS REGISTER 2

REGISTER	SR27	SR26	SR25	SR24	SR23	SR22	SR21	SR20
SR2	T1OUT	$\overline{IRTS}$	REC IDLE	0	0	0	0	$\overline{LINK}$

BIT	DESCRIPTION
SR20	If the link is established, $\overline{LINK}$ = 0. If the link is logically disconnected, $\overline{LINK}$ = 1.
ST24-21	Unused Bits — 0.
SR25	REC IDLE (Receiver Idle) indicates that the WD2511 has received at least 15 contiguous 1's.
SR26	$\overline{IRTS}$ stands for the Internal Request-To-Send bit, and indicates that the transmitter is attempting (successful or not) to send either data or flags.
SR27	T1OUT bit means that timer T1 has timed-out. This bit returns to 0 when T1 is re-started. When T1OUT = 1, T1 is not running. NOTE: This bit could be a 1 for a few microseconds in between intervals when T1 stops and is restarted.

ERROR REGISTER (ER0)

HEX VALUE	ERROR/EVENT
02	Receiver overrun. The Receiver Register (RR) had a character to load into the FIFO but the FIFO was full. See note 2.
04	Transmitter underrun. The Transmitter (TR) needed a character from the Transmitter Holding Register (THR) but the THR was not ready. The frame being transmitted is aborted. See note 2.
10	RLOOK not ready. REC RDY bit of next segment is 0 but RECR = 1. This interrupt will not occur if RECR = 0.
21	Link is up. Was down.
22	DISC sent. REC IDLE for time T1xN2.
24	DISC sent. SABM sent N2 times without receiving UA.
30	Received DISC or DM while link was up.
41	Going to next chain segment.
42	Next chain segment of the Receiver was not ready.
80	Link reset (SABM) received.
88	S-command sent N2 times without acknowledgement.
C0	Frame Reject (FRMR) received. See note 1.
C1	Frame Reject (FRMR) transmitted. See note 3. The received C-field (returned in the first I-field byte of the FRMR frame) was invalid.
C3	Frame Reject (FRMR) transmitted. See note 3. The received and rejected frame contained an I-field which is not permitted with this frame type.
C4	Frame Reject (FRMR) transmitted. See note 3. Received I-field exceeded the total amount of I-field data bytes established in Register C.
C8	Frame Reject (FRMR) transmitted. See note 3. The received frame contained an invalid N(R).

NOTES:

1. Whenever a Frame Reject (FRMR) is received, the I-field will have been placed in the appropriate memory location by the DMA. A link reset (SABM) will be transmitted. The NB is not advanced.
2. Receiver overrun and Transmitter underrun are indication that the $\overline{TC}/\overline{RC}$ clocks are either too fast for the WD2511, or the $\overline{DACK}$ response is too slow, or both.
3. As a result of FRMR transmitted, a SABM is received, causing link reset. In this case, only the Frame Reject interrupt is indicated.

W, X, Y, Z OF FRMR

A frame reject (FRMR) contains a three byte I-field. The first byte is the rejected frame control field. The second byte contains the current N(S) and N(R) counts of the station reporting the reject condition. The third byte contains W-X-Y-Z-0-0-0-0 where W is the LSB.

W set to 1 indicates that the control field received and returned in the first I-field byte was invalid.

X set to 1 indicates the rejected frame contained an I-field which is not permitted with this command.

W is also set to 1 in this case.

Y set to 1 indicates the received I-field exceeded the maximum I-field data byte count established (CHAIN/BUFFER SIZE). Y is mutually exclusive with W.

Z set to 1 indicates the received control field contained an invalid N(R). Z is mutually exclusive with W.

Upon receiving a FRMR, the WD2511 will place the 3 byte I-field in memory by DMA, just as if the FRMR were a packet.

When the WD2511 transmits a FRMR, the frame reject condition is entered. Only a received SABM or DISC will clear this condition. If any other command is received, the WD2511 will re-transmit the FRMR. Also, the WD2511 will **not** transmit packets while in the frame reject condition.

In the FRMR I-field, bit #4 of the second byte is a "1" if the rejected frame was a response and a "0" if the frame was a command.

MEMORY ACCESS METHOD

The WD2511 memory access is accomplished by the use of DMA and two look-up tables. These tables are set-up to allow up to 7 I-frames to be outstanding in each direction of the communications link. The look-up tables are divided into a transmit and a receive area (TLOOK and RLOOK) and are located in memory external to the WD2511.

TLOOK
RLOOK

These tables contain address and control information for individual Transmit/Receiver packets.

To provide the WD2511 access to TLOOK and RLOOK load only the starting address of TLOOK into the WD2511 registers A and B.

REG A	A15	A14	A13	A12	A11	A10	A9	A8
REG B	A7	A6	A5	A4	A3	A2	A1	A0

A0-A15 16 bit TLOOK starting address

The TLOOK and RLOOK tables are each divided into 8 segments and each segment contains 8 bytes. Figure 3 illustrates the segmentation of TLOOK and RLOOK. Figure 5 and 6 illustrate the contents of a single TLOOK and RLOOK segment.

TRANSMIT

To transmit, the WD2511 will have read from TLOOK the starting address and length of the first packet to be transmitted. The WD2511 will automatically transmit the flag, address, and control fields. Next, the information field data will be transmitted using DMA from the "SEND #0 PACKET" memory buffer. At the end of the information field, the WD2511 will automatically send the FCS and closing Flag. The WD2511 will then move on to the next packet.

If retransmission of one or more (up to seven) packets becomes necessary, the WD2511 will automatically retrace the previous transmissions through the TLOOK table. The user's CPU software does not become involved in the retransmission. However, an ERROR COUNTER is incremented. (See Error Counter Section.)

RECEIVE

When received, each frame is checked for correct address and FCS fields and for type of control field. If the frame is a packet, the information field is placed in the assigned memory location in a method similar to that used in transmit mode. If the packet is received error-free and in proper N(S) sequence count, an interrupt is generated and the WD2511 is ready for the next packet which will be placed in the next location.

Figure 4 shows a "store-and-forward" example that is useful in a network node.

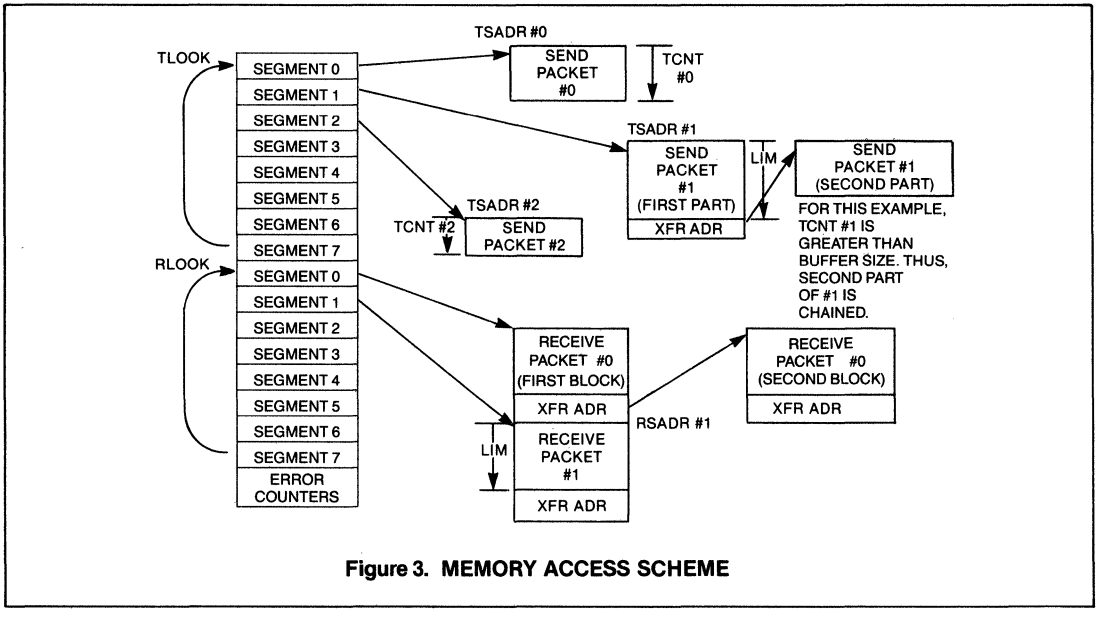


Figure 3. MEMORY ACCESS SCHEME

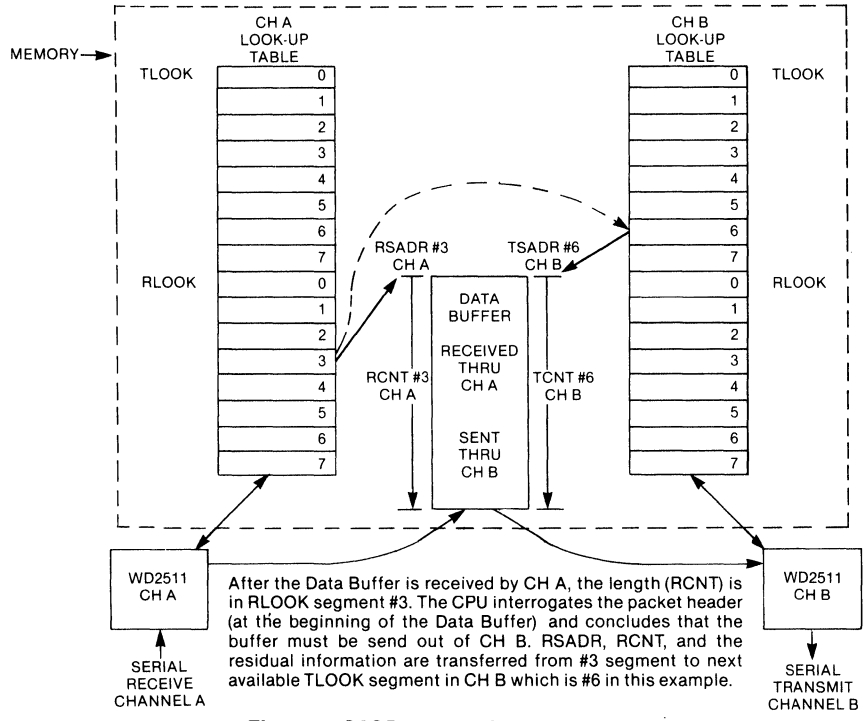


Figure 4. STORE-AND-FORWARD EXAMPLE

TLOOK AND RLOOK

Figures 5 and 6 detail the individual segments for TLOOK and RLOOK.

BRDY means that the transmit buffer is ready. The WD2511 will send the block only after the CPU sets BRDY = 1. (BRDY is used in conjunction with the SEND bit.) At the completion of the transmission, the WD2511 will set BRDY = 0 and then read the BRDY of the next segment.

After transmitting a packet, an acknowledgement must be received from the remote device. The acknowledgement is contained in the received N(R) count of an I-frame or S-frame. Upon acknowledgement, the WD2511 will set ACK'ED = 1, and generate a block-acknowledged interrupt. Before assigning a new block to a segment in TLOOK, the CPU must make sure that the previous block which used that segment number has been acknowledged.

REC RDY informs the WD2511 that the receive buffer is ready. The WD2511 will not receive a packet into a buffer referenced by a particular segment until REC RDY = 1. If the WD2511 progresses to a segment which has REC RDY = 0, an error interrupt will be generated.

After receiving an error-free packet with correct N(S), the WD2511 will, in order: 1) Set FRCML (Frame Complete), clear REC RDY and store received residual count. 2) Store the received length, in characters, of the I-field in RCNT HI and RCNT LO. 3) Advance the NE count and generate a packet received interrupt. 4) Acknowledge the received packet at the first opportunity.

The addresses (TSADR and RSADR) are 16-bit binary addresses. HI represents the upper 8-bits and LO represents the lower 8-bits. The counts (TCNT and RCNT) are 12-bit binary numbers for the number of characters in the I-field.

TSADR is the starting address of the buffer to transmit and TCNT is the binary count of the number of bytes to transmit.

RSADR is the starting address of the receive buffer. After successfully receiving the packets, the WD2511 will write the value of RCNT which is the binary length of the received packet.

Whether the WD2511 accesses a look-up table or a memory block, a DMA Cycle is required for each access.

BYTE # IN SEGMENT	BIT # 7	6	5	4	3	2	1	0
1	ACK'ED	NU	NU	NU	NU	NU	NU	BRDY
2	TSADR HI							
3	TSADR LO							
4	SPARE				TCNT HI			
5	TCNT LO							
6	SPARE FOR USER DEFINITION							
7	SPARE							
8	SPARE							

NU = Not Used

FIGURE 5. TLOOK SEGMENT

The control bits in TLOOK (BRDY and ACK'ED) and in RLOOK (FRCML and REC RDY) define various states for each segment. These states are shown below:

TLOOK STATES

ACK'ED	BRDY	STATE
0	1	Ready To Transmit (CPU set BRDY, cleared ACK'ED)
0	0	*Transmitted and Awaiting Acknowledge (WD2511 cleared BRDY)
1	0	Received Acknowledge (WD2511 set ACK'ED)
1	1	This state not allowed

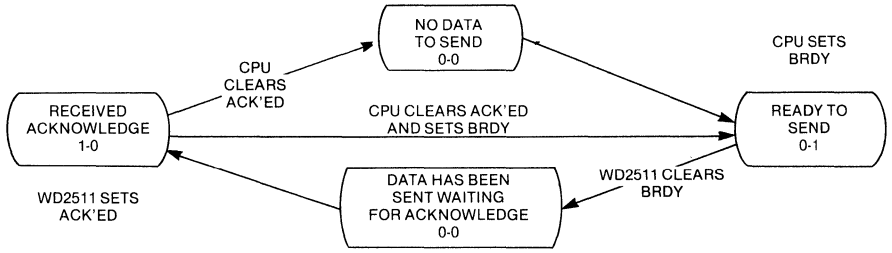
*State 0-0 could also occur whenever there is no data ready to send.

BYTE # IN SEGMENT	BIT # 7	6	5	4	3	2	1	0
1	FRCML*	NU	NU	NU	RES2	RES1	RES0	REC RDY
2	RSADR HI							
3	RSADR LO							
4	NOT USED				RCNT HI			
5	RCNT LO							
6	SPARE FOR USER DEFINITION							
7	SPARE							
8	SPARE							

NU = Not Used (NOTE: The "not used" bits may be either 1 or 0).

*FRCML = Frame Complete

FIGURE 6. RLOOK SEGMENT



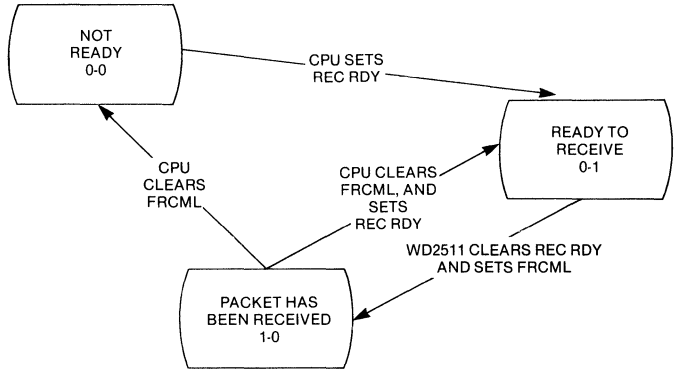
TLOOK SEGMENT STATE FLOW

Notice that in a TLOOK segment, the 0-0 state could have two meanings. Due to control internal to the WD2511, this will not pose an ambiguity to the WD2511. However, if it is a difficulty to the CPU, the CPU could at start-up, set all ACK'ED bits. Since this would only be a start-up procedure, this would not violate the "deadly embrace" rule.

In the "WAITING FOR ACKNOWLEDGE" state, one or more re-transmissions could occur.

RLOOK STATES

FRCML	REC RDY	STATE
0	1	Ready To Receive (CPU set REC RDY, cleared FRCML)
1	0	Received Packet (WD2511 set FRCML, cleared REC RDY)
0	0	Not Ready (CPU cleared FRCML)
1	1	This state not allowed



RLOOK SEGMENT STATE FLOW

REGISTER	CHAIN				BUFFER SIZE			
C	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

CHAINING/BUFFER SIZE

The WD2511 includes a chained-block feature which allows the user more efficient use of memory particularly in situations where the maximum packet size is much larger than the average packet size.

Register C is used to program the chaining feature. The upper 4 bits define CHAIN which is the number of chain segments allowed in addition to the first segment. (If this feature is not used, make CHAIN all 0's.)

The lower 4 bits of Register C define the buffer size, which is the size of the buffer in multiples of 64 bytes including the transfer address (XFR ADR). If buffer size is 0000, the size is 64. For 0001, the size is 128, and so on.

The maximum amount of I-field data bytes that can be contained in this buffer is the buffer size minus 2 bytes (XFR ADR) for all transmitter and receiver chaining blocks, except for the last receiver chaining block. For this block, the maximum amount of I-field data bytes is the buffer size minus 3.

For example, suppose that the buffer size defines a segment size of 128 and that CHAIN defines 8 additional segments in addition to the first. (Register C would be hex 81 in this example.) When 126 bytes of I-field data have been received, the WD2511 will read the next two buffer bytes as a transfer address (XFR ADR) pointing to another segment. At the end of that segment is another XFR ADR, and so on, up to a maximum of 9 total segments, (in this example).

For the receiver, a XFR ADR of all 0's will mean that the next segment is not ready. If the WD2511 reaches a XFR ADR on the receiver with all 0s, there will be an Error Interrupt code 42. Otherwise, there will be an Interrupt code 41 which is a status indication that the WD2511 is going to the next segment. I/O Register 6 upper 4 bits gives a status of which chain segment is currently being used.

The transmitter chaining works like the receiver with the following exceptions:

1. XFR ADR = all 0's will not indicate next segment not ready.
2. There is no interrupt when going from one segment to another.
3. There is no status of the current segment being used.
4. Last chaining block is allowed to contain one more I-field data byte.

Total amount of I-field data bytes in receiver = (64 x (1 + BUFFER SIZE) − 2) x (1 + CHAIN) − 1.

The total amount of I-field data bytes in transmitter = (64 x (1 + BUFFER SIZE) − 2) x (1 + CHAIN).

Also, note that the transmitter and receiver counts are modified by 2 for each time a chain boundary is crossed. For example, if BUFFER SIZE = 0001 (segment size = 128 bytes including XFR ADR), and if an I-field of 270 bytes is to be transmitted, then there will be two times that a chain boundary is crossed. The TCNT must be made 274 to send 270 bytes. The same is true for RCNT. Note that the largest block of data that can be sent without chaining is 1021 bytes.

"DEADLY EMBRACE" PREVENTION

A "deadly embrace" can occur when two processors reach a state where each is waiting for the other. In this case, the two processors are the user's CPU and the micro-controller inside the WD2511. Therefore, to prevent the "deadly embrace," the following rule is obeyed by the WD2511 and should also be obeyed by the user's CPU. This rule applies to TLOOK, RLOOK and to the I/O registers. The Error Counters do not apply to this rule.

> RULE: If a bit is set by the CPU, it will not be set by the WD2511, and vice versa. If a bit is cleared by the WD2511, it will not be cleared by the CPU, and vice versa.

As an example, the BRDY bit in the TLOOK segments is only set by the CPU and only cleared by the WD2511.

SEND BIT CONTENTION

The WD2511 may be clearing the Send bit when the host is setting it. To insure that the bit is set the host should read the status of the Send bit after it is set. If the Send bit is cleared the host should set it again.

TLOOK AND RLOOK POINTERS

There are three 3-bit counters for the status of the segments in TLOOK and RLOOK. Status Register #0 (SR0) contains counters NA and NB which are used in conjunction with TLOOK. NB is the segment number of the next block to be transmitted and is advanced at the end of each block transmission. NA is the value of the segment of the next block to be acknowledged. If all transmitted blocks have been acknowledged, then NA = NB.

In SR1 is a 3-bit counter, NE, used in conjunction with RLOOK. NE is the value of the segment number where the next received packet will be placed.

NA = Next to be Acknowledged

NB = Next Block to be Transmitted

NE = Next Expected to be Received

VARIABLE BIT LENGTH AND RESIDUAL BITS

The WD2511 will only send 8 bits per character and all transmitted frames will have an integral number of bytes.

The WD2511 may receive a packet with, or without, an integral number of bytes. The "RES" bits in the RLOOK tables indicate the number of received residual bits. The residual bits occupy the lower portion of the last received character.

RES 2	RES 1	RES 0	Received Residual Bits
0	0	0	0
0	0	1	7
0	1	0	6
0	1	1	5
1	0	0	4
1	0	1	3
1	1	0	2
1	1	1	1

ERROR COUNTERS

Following contiguously after RLOOK are six 8-bit error counters. The WD2511 will increment each counter at the occurrence of the defined event. However, the WD2511 will not increment past 255 (all 1's). The CPU has the responsibility of clearing each counter. The first counter past RLOOK is #1, etc.

ERROR COUNTER	TYPE OF ERROR
1	*Received Frames with FCS Error (includes frames ABORTed in the I-field).
2	Received Short Frames (less than 32-bits)
3	**Number of times T1 ran-out (completed)
4	Not used
5	*REJ Frames Received
6	REJ Frames Transmitted

*These counters are incremented only if the received A-field is equal to either Register E or F.

**Incremented only when attempting to transmit a command.

The Error Counters are accessed by the WD2511 transmitter DMA channel. Therefore, if multiple errors are received while the WD2511 is transmitting a long frame, only the last error will be counted. The only Counters which could miss counts because of this are Counters #1, #2, and #5. The error Counters are incremented only when the link is up ($\overline{LINK}$ = 0).

OTHER I/O REGISTERS

RECEIVED C-FIELD

Register 7 is the C-field of the last received frame, provided the A-field of the frame was equal to either register E or F, the FCS was good, the frame contained 32 or more bits, and the WD2511 is not waiting for a SABM or DISC in response to a transmitted FRMR.

TIMER

Registers 8 and 9 define a 10-bit timer (T1), and a 6-bit Maximum Number of Transmissions and Retransmissions counter (N2).

	BIT #							
REGISTER	7	6	5	4	3	2	1	0
8	T1							LSB
9	N2							
	MSB					LSB	MSB	

MSB = Most Significant Bit
LSB = Least Significant Bit

T1 provides the value of a delay in waiting for a response and/or acknowledgement. The delay is the binary count multiplied by time CT where:

$$CT = \frac{16384}{CLK} \text{ sec}$$

Thus, if CLK = 1 MHz, then T1 may be set in increments 16.384 milliseconds, to a maximum delay of 16.78 seconds. All ones in T1 is maximum delay.

Once the CPU establishes T1 and N2, there is no need to write into T1 and N2 again unless a master reset ($\overline{MR}$) has occurred, there is a power loss, or the CPU needs to change T1 or N2. If a time-out occurs, the WD2511 will still retain T1 and N2.

The conditions for starting, stopping, or restarting T1 are shown below: ("Re-start" means starting T1 before it ran-out).

START T1	RE-START T1	STOP T1
1. *I-frame sent and T1 not already in progress due to previous I-frame.	*Acknowledgement received to some, but not all, I-frames.	Acknowledgement received for all I-frames.
2. —	*RNR received while link up.	
3. *SABM or DISC sent. (N2 restarted at first occurrence)	—	UA or DM Received
4. Receiver Idle (REC IDLE = 1)	*Frame sent, while REC IDLE = 1	Detected REC IDLE = 0
5. S — command sent		—

*N2 is restarted.

"A" FIELD REGISTERS

Registers E and F provide a programmable A-field. This allows the WD2511 to be a super-set of the X.25 document. That is, the WD2511 can handle a wider range of application than the DTE-DCE links defined in X.25. These wider ranges include: DTE-to-DTE connection, multipoint, and loop-back testing.

If the WD2511 is strictly in an X.25 DTE-DCE link, use the values shown below:

DTE	Register E = 01 Register F = 03
DCE	Register E = 03 Register F = 01

If performing a loop-back test, either internal (CR03 = 1) or external (CR03 = 0), registers E and F should be the same.

V. LAPB PROCEDURE

The Link Access Procedure Balanced (LAPB) is described in CCITT Recommendation X.25 as the Level 2 protocol for the Asynchronous Balanced Mode (ABM).

Zero bit insertion/deletion, use of flags, and FCS are part of Level 2, and have been discussed in this document.

The DTE is the Data Terminal Equipment and the DCE is the Data Circuit Termination Equipment (the network side of the DTE-DCE connection).

The DTE and DCE are each "combined" stations in that each can transmit and receive commands and responses. Whether a particular frame is to be taken as a command or a Response is determined by the contents of the address field. Commands from the DCE and the associated responses from the DTE use address A (hex 03).

Commands from the DTE and the associated responses from the DCE use address B (hex 01).

The individual commands and responses are shown in Figure 7.

USE OF POLL BIT

One use of the Poll bit (P) is in conjunction with Time-Out Recovery. Timer T1 is started at the beginning of a transmitted command provided it has not been previously started. If T1 runs out, the command will be retransmitted with P = 1. If T1 runs out again, the command will again be retransmitted, with P = 1 up to N2 times. At N2 + 1, an error interrupt will occur. If the command was an S-frame (originally an I-frame), the WD2511 will reset the link by transmitting a SABM. If the command was a SABM, the WD2511 will send a DISC. If a DISC, the WD2511 will continue to send a DISC indefinitely.

LAPB Commands and Responses (Bit 0 is transmitted first).
Only the FRMR and I-frame contain I-fields.

FRAME TYPE	COMMAND	RESPONSE	BIT #							
			7	6	5	4	3	2	1	0
INFORMATION (I)	I-FRAME (PACKET)		N(R)			P	N(S)			0
UNNUMBERED (U)	SABM		0	0	1	P	1	1	1	1
	DISC		0	1	0	P	0	0	1	1
		UA	0	1	1	F	0	0	1	1
		FRMR	1	0	0	F	0	1	1	1
		DM	0	0	0	F	1	1	1	1
SUPERVISORY (S)	RR	RR	N(R)			P/F	0	0	0	1
	RNR	RNR	N(R)			P/F	0	1	0	1
	*REJ	REJ	N(R)			P/F	1	0	0	1

*The WD2511 will not send a REJ command (will send REJ response, only), but may receive either a REJ command or REJ response.

FIGURE 7.

TRANSMISSION OF ABORT

An ABORT (seven contiguous 1's) is transmitted to terminate a frame in such a manner that the receiving station will ignore the frame. There are two conditions which will cause the WD2511 to transmit an ABORT:

1. Transmitter Under-Run
2. While transmitting a packet, a REJ is received.

LOOP-BACK TEST

The loop-back may be internal (CR03 = 1) or external (CR03 = 0). Of course, if external, RD and TD must be tied together either directly or remotely.

If CR03 = 1, TD is internally tied to RD, and the RD signal (pin 16) is internally disconnected. Also, $\overline{TC}$ is internally tied to $\overline{RC}$ and the pin at $\overline{RC}$ (pin 17) is internally disconnected. $\overline{CTS}$ must be connected externally to GND or $\overline{RTS}$.

WD2511 ELECTRICAL SPECIFICATIONS:

ABSOLUTE MAXIMUM RATINGS:

Voltages referenced to V_{SS}

High Supply Voltage (V_{DD}) . . . . . −0.3 to +15V
Voltage at any Pin . . . . . −0.3 to +15V
Operating Temperature Range . . . . . 0°C to +70°C
Storage Temperature Range . . . . −55°C to +125°C

NOTE:
Maximum limits indicate where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC Electrical characteristics.

Operating DC Characteristics: V_{SS} = 0V, V_{CC} = +5.0V ±0.25, V_{SS} = +12.0V ±0.6V T_A = 0° to +70°C

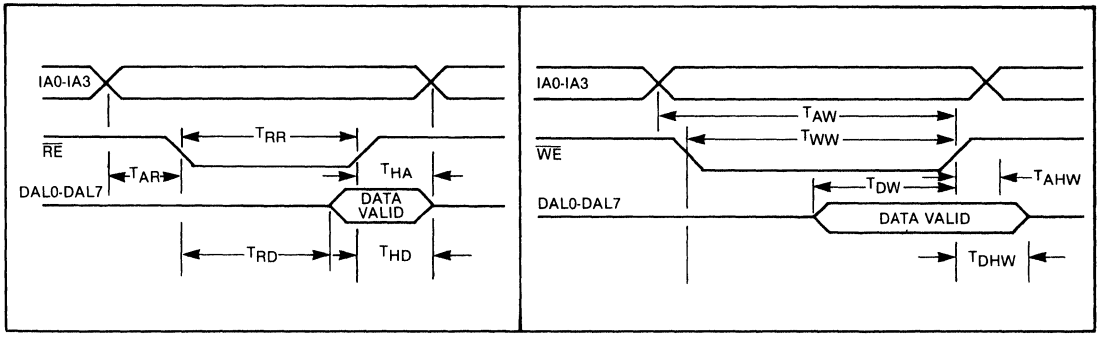
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
I_{DD}	V_{DD} Supply Current		20	70	mA	
I_{CC}	V_{CC} Supply Current		200	280	mA	
V_{DD}	High Voltage Supply	11.4	12	12.6	V	
V_{CC}	Low Voltage Supply	4.75	5	5.25	V	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = −0.1mA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{LH}	Input Source Current			10	μA	Vin = V_{CC}
I_{LL}	Input Sink Current			10	μA	Vin = +0.4V
I_{OZH}	Output Leakage (High Impedance)			50	μA	Vin = V_{CC}
I_{OZL}	Output Leakage (High Impedance)			50	μA	Vin = +0.4V

AC Timing Characteristics (AC):

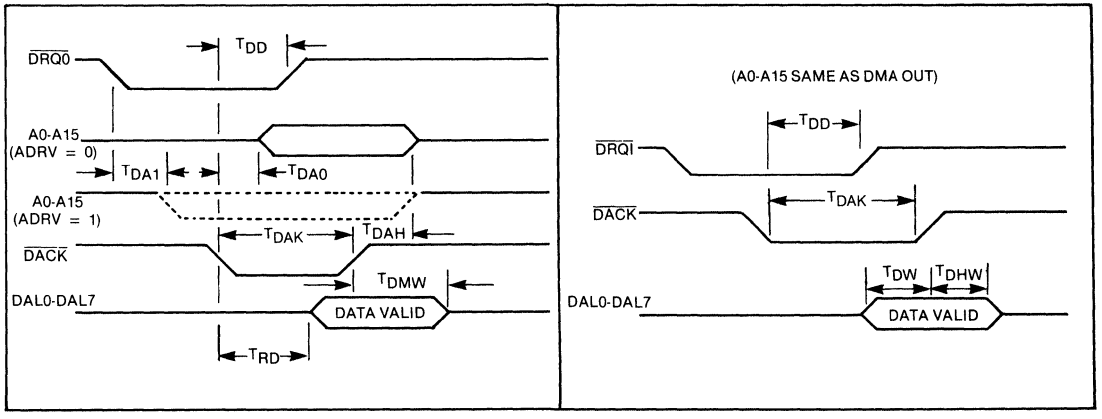
SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	CONDITIONS
CLK	Clock Frequency	0.5		2.05	MHz	Note 1
RC	Receive Clock Range	0			MHz	Note 4
TC	Transmit Clock Range	0			MHz	Note 4
MR	Master Reset Pulse Width	10			mS	
T_{AR}	Input Address Valid to $\overline{RE}$	0			nS	
T_{RD}	Read Strobe (or $\overline{DACK}$ Read) to Data Valid	2		375	nS	Note 5, 2
T_{HD}	Data Hold Time from Read to Strobe	20		100	nS	
T_{HA}	Address Hold Time from Read Strobe	0			nS	
T_{AW}	Input Address Valid to Trailing Edge of $\overline{WE}$	100			nS	
T_{WW}	Minimum $\overline{WE}$ Pulse Width	200			nS	
T_{DW}	Data Valid to Trailing Edge of $\overline{WE}$ or Trailing Edge of $\overline{DACK}$ for DMA Write	100			nS	Note 2, 3
T_{WRR}	CS High between Writes	300			nS	
T_{RDR}	CS High between RE	300			nS	
T_{RR}	RE Pulse Width	375			nS	
T_{DAK}	DACK Pulse Width	375				
T_{AHW}	Address Hold Time after $\overline{WE}$	80			nS	
T_{DHW}	Data Hold Time after $\overline{WE}$ or after $\overline{DACK}$ for DMA Write	100				
T_{DA1}	Time from $\overline{DRQO}$ (or $\overline{DRQI}$) to Output Address Valid if ADRV = 1			80	nS	Note 3
T_{DA0}	Time from $\overline{DACK}$ to Output Address Valid if ADRV = 0			375	nS	Note 5
T_{DD}	Time from Leading Edge of $\overline{DACK}$ to Trailing Edge of $\overline{DRQO}$ (or $\overline{DRQI}$)			375	nS	Note 5
T_{DAH}	Output Address Hold Time from $\overline{DACK}$	20		100	nS	
T_{DMW}	Data Hold Time from $\overline{DACK}$ for DMA Out	20		100	nS	Note 2
T_{TDV}	TD Valid	100			nS	
T_{SRD}	RD Setup	0			nS	
T_{HRD}	RD Hold	320			nS	

NOTES:

1. Clock must have 50% duty cycle.
2. There must not be a CPU read or write ($\overline{CS}$-$\overline{RE}$ or $\overline{CS}$-$\overline{WE}$) within 500 nanoseconds after the trailing (rising) edge of $\overline{DACK}$.
3. There must not be the leading (falling) edge of $\overline{DACK}$ allowed within 500 nanoseconds after the completion of a CPU write ($\overline{CS}$-$\overline{WE}$).
4. See "Ordering Information" for maximum serial rates.
5. C(load) = 100pf
6. Measured by discharging a 100pf capacitor to each pin through a 1K ohm resistor.



CPU READ ($\overline{CS}$ IS LOW) **CPU WRITE ($\overline{CS}$ IS LOW)**

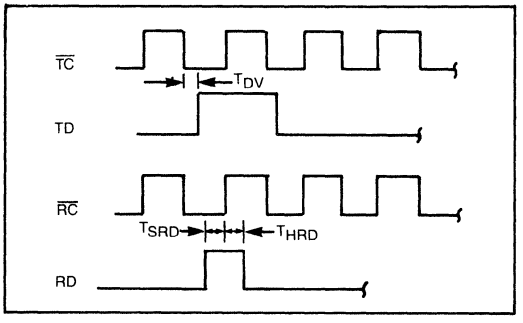


DMA OUT **DMA IN**

ORDERING INFORMATION

Order Number	Maximum Data Rate
WD2511AN-01	100 Kbps
WD2511AN-05	500 Kbps
WD2511AN-11	1.1 Mbps*

*Higher speeds available on special order.



TD-RD TIMING

APPENDIX A

TRANSPARENT MODES

The WD2511 was originally intended to be a link level controller meeting the requirements of X.25 LAPB and this has been accomplished. However, there has been an increasing demand from potential WD2511 users for additional frame types not included in the LAPB frame type repertoire.

For example, the Bell System standard, BX.25, calls for the use of XID (exchange identification) in LAPB connections of DTE-to-DTE and in Dial access. (Of course, DTE-to-DTE and Dial access are not X.25 in the strictest sense.) Also, Western Digital has received several requests for the use of a SIM (set initialization mode). Also, there has been one request to allow "unknown" frames to pass thru the chip for the purpose of teleloading.

Therefore, we have added two selectable modes to the WD2511: transparent transmit and transparent receive. Basically, these two modes allow the user the option to pass certain non-LAPB frames thru the chip without controlling these frames according to the LAPB protocol.

FEATURES OF THE TRANSPARENT MODES

- May transmit any A and C field under transparent control.
- May receive any U-frame not part of the LAPB repertoire if transparent-receive enabled.
- Transparent modes are link state independent.

1.0 HOW THE TRANSPARENT MODES WORK

Two control bits have been added. TXMT (CR17) is the bit to enable the Transparent Transmit and TRCV (CR16) will enable the Transparent Receive.

1.1 TRANSPARENT TRANSMIT

When TXMT = 1, the WD2511 will transmit the frame in the next TLOOK segment provided SEND (CR10) = 1 and BRDY of that TLOOK segment is 1. The link may be either UP or DOWN. The WD2511 will not add the A and C fields to the Transparent Transmitted frame. The user's CPU must add these fields as the first two bytes in the transmit buffer. Thus, the significance of the transmit count (TCNT) is different from normal packet transmission. In packet transmission, TCNT is the count of the I-field. In transparent transmission, TCNT is the I-field plus the A and C fields (I-field plus two bytes).

The timer, T1, will be disabled in transparent transmission. Therefore, if using this feature while the link is UP, it is advised that TXMT be set only when there are no outstanding (unacknowledged) packets which is indicated whenever NA = NB.

At the end of the transparent transmission, there will be an interrupt with XBA = 1. The SEND bit will be cleared, but the BRDY bit will not be cleared. The NB pointer will not be incremented. To send another transparent frame, set SEND. To resume packet transmission, clear TXMT and set SEND. (Of course, the TLOOK segment must be set-up prior to setting SEND.)

If SEND is set while the link is down, a transmission will occur even if TXMT = 0. Under this condition, a packet will be transmitted from current TLOOK segment, NB and V(S) will be incremented, and the chip will go on to the next TLOOK segment just as if the link were UP. However, the WD2511 will expect no acknowledgment to the packet(s). If the link is brought UP later, NB and V(S) are cleared to 0 at the time the link comes UP.

The bit $\overline{XI}$ (CR15) is used only when TXMT = 1. $\overline{XI}$ stands for Transmit I-field. If the frame contains three, or more bytes, not counting FCS, set $\overline{XI}$ = 0. If the frame contains two bytes not counting FCS, set $\overline{XI}$ = 1. When $\overline{XI}$ = 1, only two frame bytes will be transmitted regardless of TCNT. DO NOT attempt to transmit a frame with TXMT = 1 and $\overline{XI}$ = 0 if TCNT is 2, 1, or 0.

1.2 TRANSPARENT RECEIVE

For the purposes of this discussion, it is necessary to define an "unknown frame." That is, a frame which is "unknown" to the WD2511.

Unknown Frame: A U-frame (unnumbered) frame which is not part of the LAPB repertoire. The U-frame repertoire in LAPB is SABM, DISC, DM, UA, and FRMR. For the purposes of this discussion, "UF" will refer to an unknown frame without an I-field, and "UFI" will refer to an unknown frame with a I-field.

A received SREJ (Selective REJect), which is an S-frame, is not considered an unknown frame by the WD2511. If the link is DOWN and an SREJ command is received, a DM response will be sent. If the link is DOWN and a SREJ response is received, the SREJ is disregarded. If the link is UP and a SREJ command or response is received, a FRMR will be sent with W = 1. The WD2511 will treat a received SREJ the same whether TRCV is 0 or 1.

A received packet (I-frame) response is not considered an unknown frame by the WD2511. If the link is DOWN, the frame is disregarded. If the link is UP, a FRMR will be sent with W = 1 and X = 1. The received packet response is treated the same whether TRCV is 0 or 1.

Whether TRCV is 0 or 1, the WD2511 will check all received frames to insure that the A-field equals either Register E or F, that the FCS is correct, and that the frame contains 32 bits or more. If TRCV = 0, and if a UF or UFI is received, and if the link is UP, the WD2511 will send a FRMR with W = 1 (W and X are 1 in the case of a UFI). See "States of the WD2511."

When TRCV = 1, the WD2511 will be enabled to receive all frames. If the frame is "known" by the WD2511, it will be treated according to the protocol just as if TRCV = 0. However, if the frame is a UF or UFI, it will be passed on to the user's CPU.

When an unknown frame is received while TRCV = 1, there will be an interrupt with ERROR = 1 and the Error Register (ER0) will contain one of the following hexidecimal values:

ER0	FRAME RECEIVED
60	UFI Response
61	UFI Command
62	UF Response
63	UF Command

The C-field of the received frame is contained in Register #7. If the frame had an I-field, the frame will be placed in the next RLOOK segment and the value of RCNT will represent the count of bytes in the I-field (not including the A and C fields). The RLOOK pointer, NE, will be incremented. Therefore, the relationship between NE and V(R) will not be guaranteed if transparent receive is used while the link is UP. However, this will not cause a sequence problem in the protocol since the actual V(R) is maintained in an internal register in the WD2511. Note that NE is cleared when the link is brought UP. Thus, if transparent receive is used only when the link is DOWN, then NE will be equal to V(R).

A word of caution. If the next RLOOK segment is not ready when a UFI is received, the Error Register (60 or 61) will be overwritten almost immediately with an error code 10 (RLNR) and the user will not know if the received UFI was a command or response.

If RECR is set while the link is DOWN, the WD2511 will prepare to receive I-fields, whether TRCV is 0 or 1. If a packet command is received, there will be a PKR interrupt, and the NE and V(R) will be incremented. Of course, NE and V(R) are cleared once the link is brought up.

The following tables show what action the WD2511 will take when various frames are received.

TABLE 1. PACKET RECEIVED (command, not response)

LINK	RLOOK READY	TRCV	ACTION BY WD2511
DOWN	NO	0 or 1	DISREGARD
DOWN	YES	0 or 1	If N(S) = V(R), PKR interrupt, V(R) and NE incremented. No ack transmitted. If N(S) not = V(R), DISREGARD.
UP	NO	0 or 1	If N(S) = V(RT), RNR sent, Else, REJ condition entered.
UP	YES	0 or 1	If N(S) = V(R), PKR interrupt, V(R) and NE incremented. Acknowledgement sent at next opportunity. If N(S) not = V(R), enter REJ condition.

TABLE II. UFI RECEIVED

LINK	RLOOK READY	TRCV	ACTION BY WD2511
DOWN	NO	0 or 1	DISREGARD
DOWN	YES	0	DISREGARD
DOWN	YES	1	Error interrupt 60 or 61. NE incremented.
UP	NO	0	FRMR sent. W = 1 X = 1
UP	NO	1	DISREGARD
UP	YES	0	FRMR sent. W = 1 X = 1
UP	YES	1	Error interrupt 60 or 61. NE incremented.

If TRCV = 1 and UF (no I-field) is received, there will be an Error interrupt 62 or 63, independent of the link state or the readiness of RLOOK.

Of course, the received C-field of any frame will be in Register #7 provided the A-field matched either Register E or F, the FCS was good, and the frame contained 32, or more, bits.

APPENDIX B

HALF DUPLEX OPTION

The WD2511 is basically a full duplex device. The receiver is maintained in an "always ready" condition even if the receive buffer is not ready. Thus, whether the received frame came from a full or half duplex system is of no consequence to the WD2511.

Therefore, the half duplex option affects only the WD2511 transmitter. Half duplex is enabled when H/$\overline{F}$ (CR05) = 1.

The WD2511 will transmit one frame at a time according to the following procedure:

A. Enable $\overline{RTS}$ ($\overline{RTS}$ goes low).

B. Wait for $\overline{CTS}$ ($\overline{CTS}$ input goes low).

C. Transmit frame (when $\overline{CTS}$ is active).

D. Remove $\overline{RTS}$ ($\overline{RTS}$ goes high $2^1/_2$ bits of time after the last 0 of the trailing flag.)

NOTES:

The leading flag will be transmitted somewhere between 5 and 13 bits after $\overline{CTS}$ goes low.

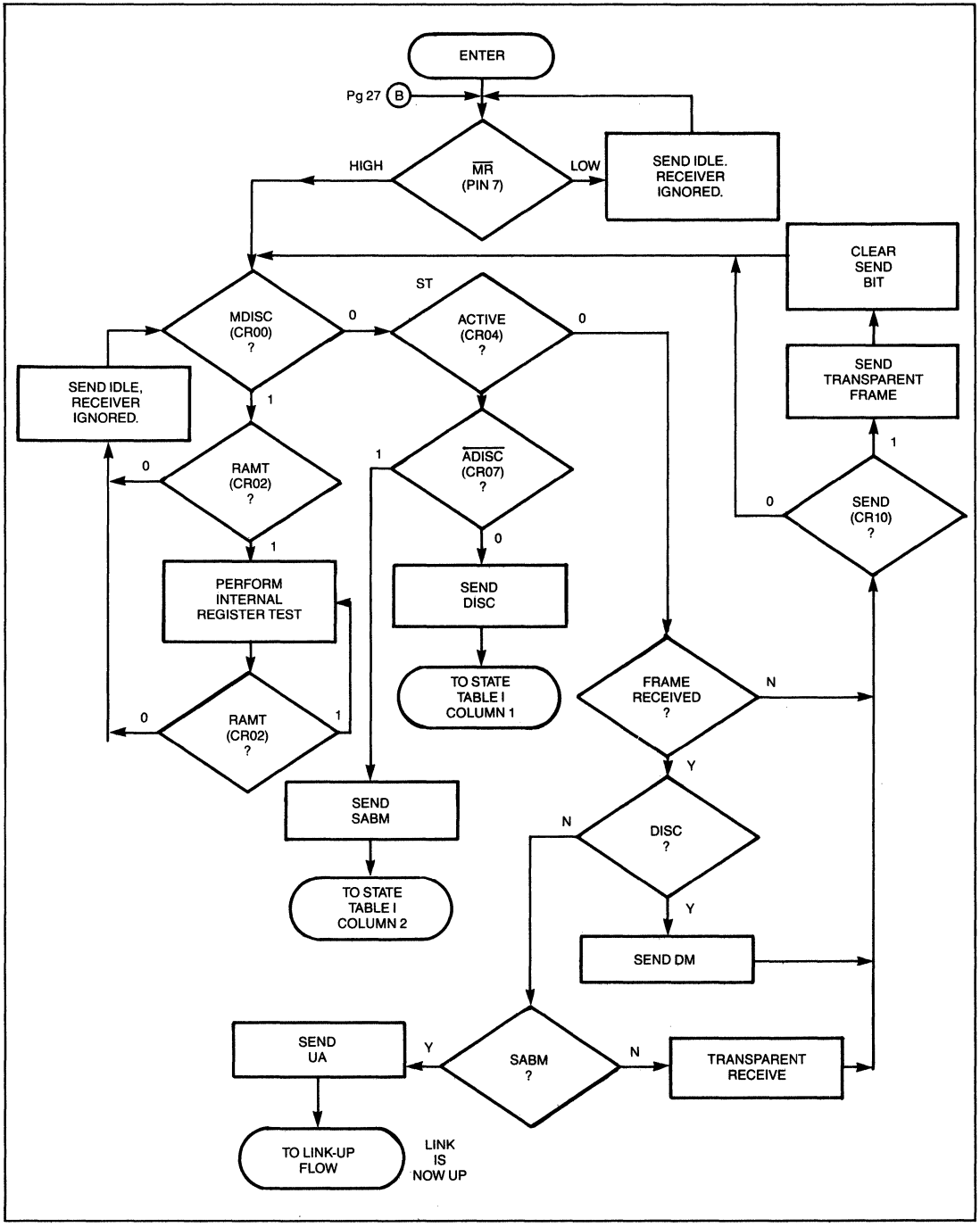
Interframe fill will be all 1's (IDLE).

If T1 is internally activated it is started when $\overline{RTS}$ goes low.

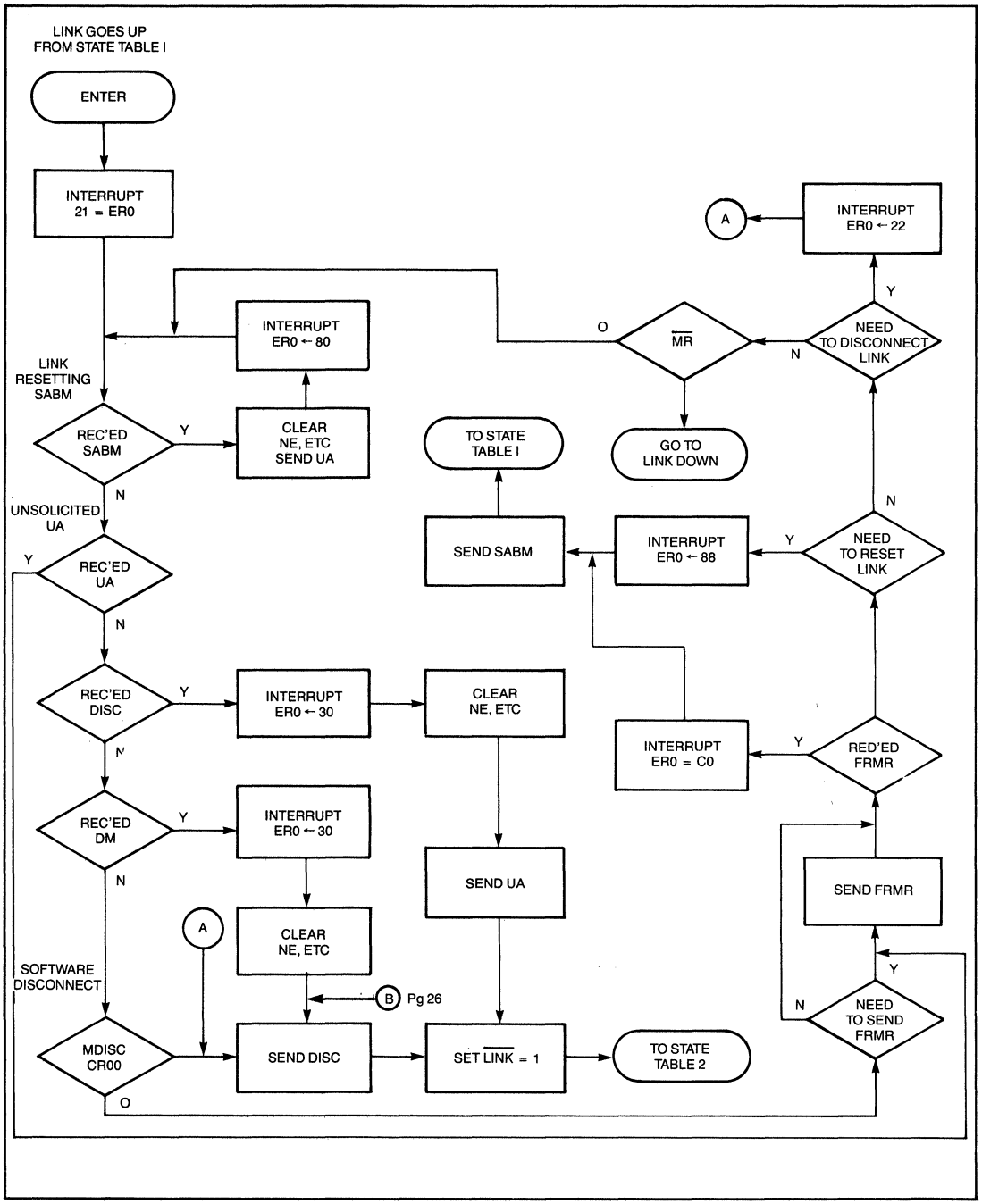
After $\overline{RTS}$ goes low, the frame will not begin transmission until $\overline{CTS}$ goes low. After the frame has started, the transmission of that frame is completed even if $\overline{CTS}$ returns high during the frame.

APPENDIX C STATE DESCRIPTIONS

LINK DOWN



CONDITION FOR RESET OR DISCONNECT
LINK IS UP



STATE TABLE I
LINK DOWN, BUT GOING UP

(Column 2 also applies to link reset)

ACTION BY WD2511

STIMULUS:	COLUMN 1: DISC sent. Waiting for UA or DM.	COLUMN 2: SABM sent. Waiting for UA.
T1 runs out	Re-send DISC. P = 1.	Re-send SABM. P = 1.
T1 and N2 run out	Re-send DISC. P = 1.	Send DISC. Interrupt ER0 = 24. Go to column 1
Received UA	Send SABM. Go to column 2	Clear NA, NB, NE, V(R), V(S). Go to link up flow.
Received DISC	Send DM.	Send DM.
Received SABM	Disregards	Send UA. Clear NA, NB, NE, V(R), V(S). Keep waitiing for UA.
Received DM	Send SABM. Go to column 2.	Send DISC. Go to column 1.
Received something other than UA, DM, DISC, or SABM	Disregard.	Disregard.

STATE TABLE II
LINK GOING DOWN (WAS UP)

User sets MDISC, Chip sends DISC.

ACTION BY WD2511

STIMULUS	DISC sent. Waiting for UA.
T1 runs out	Re-send DISC. P = 1.
Received UA or DM	Go to Link Down Flow
Received SABM	Disregard
Received DISC	Send DM. Go to Link Down Flow
Received something other than DISC, SABM, UA, or DM	Disregard.

USE OF FLAGS BY THE WD2511

Once MDISC has been reset the WD2511 will send interframe flags (hex 7E) if full duplex is selected (CR05 = 0) (point ST of the Link Down Flow point has been entered). If half duplex is selected, (CR05 = 1), interframe fill will be all 1's (IDLE).

The WD2511 does not require the interframe time fill flags. Either idle or flags will be accepted. However, if the receiver detects idle for time T1 X N2, the WD2511 will send a DISC.

When sending continuous flags, the WD2511 will send:

0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 0 1 1 1 1 1 1 0 0 1 1 . . .

The WD2511 will accept either the above sequence as continuous flags, or the "shared zero" pattern:

0 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 . . .

DEFINITIONS OF COMMAND AND RESPONSE

A transmitted or received command or response is a frame with the A-field defined below:

FRAME	A-FIELD =
Transmitted Command	Register E
Received Command	Register F
Transmitted Response	Register F
Received Response	Register E

For non-transparent transmitted frames, only commands or responses are transmitted. A transparent transmitted frame (TXMT = 1) may have any A-field the user chooses.

All received frames must be either commands or responses or the frame is disregarded ("thrown away"), even if transparent receive is enabled (TRCV = 1).

STATE TABLE III
SENDING I-FRAMES (PACKETS) AND S-COMMANDS

NOTES:
In all subsequent pages, the link is considered Up (LINK = 0) unless otherwise stated. X = don't care. TXMT = 0 for Table III.

SEND	BRDY	NA AND NB	RNRR	T1 EXPIRES	RCVD REJ	ACTION BY WD2511
1	0	X	0	No	No	Clear SEND (CR10)
1	1	X	0	No	No	Send next packet with N(S) = NB. After transmission complete. Increment NB. Exception: If NB + 1 = NA, do not send next packet. There are 7 outstanding.
X	X	X	1	Yes	No	Send S-command, P = 1.
X	X	not =	X	Yes	No	Send S-command, P = 1.
X	X	not =	X	No	Yes	Make NA = received N(R). Start sequential retransmission of packets beginning with N(S) = NA. See Note 3.

NOTES ON STATE TABLE III

1. Received S-frames in Table III are assumed to have valid N(R)'s.
2. When an acknowledgement of one or more previously transmitted packets is received, NA is set equal to the received N(R). All TLOOK segments from the old value of NA up to N(R) — 1 are acknowledged and the appropriate ACKED bits in the TLOOK segments will be set. After setting the ACKED bits, an XBA interrupt is generated.
3. Assuming appropriate TLOOK segments are ready, packets are transmitted sequentially without waiting for an acknowledgement, with three exceptions:
   a. There are already seven outstanding (unacknowledged) packets (NB + 1 = NA).
   b. The remote station has indicated a busy condition by sending an RNR frame (RNRR). T1 is started and an S-command will be transmitted with P = 1 when T1 expires.
   c. T1 expired and there are one or more outstanding packets. An S-command will be transmitted with P = 1.
4. If an S-frame command is received, the WD2511 will transmit an S-frame response at the next opportunity.
5. If SEND = and TXMT = 1, a frame will be transmitted from the next TLOOK segment if BRDY = 1. After transmission, SEND is cleared by the WD2511.

RECEIVING AND TRANSMITTING A NULL PACKET

If an error-free (FCS good) packet is received with a correct N(S), but has no I-field, that packet will be treated the same as a packet with an I-field. The fact that there was no I-field is shown by RCNT equal to all 0's. The WD2511 will not transmit a null packet. TCNT must not be allowed to be all 0's.

SENDING A REJ (RESPONSE)

1. The REJ condition is entered any time an error-free packet is received with an out-of-sequence N(S). Exception: If the received N(S) + 1 = V(R), then the received N(S) has been acknowledged, and either an RR or RNR is transmitted.
2. When the REJ condition is entered, the REJ frame with N(R) = V(R) is transmitted immediately if a packet is not being transmitted, or, at the completion of the current packet. There are two exceptions, as noted in 3 and 4 below.
3. If a link resetting SABM needs to be transmitted, the SABM is sent. When the UA is received for the SABM, the REJ condition is cleared.
4. If the receiver is not ready (RNRX = 1), the REJ is not sent.
5. Once the REJ condition is entered, only one REJ will be transmitted. Another REJ is not transmitted unless the REJ condition is cleared and re-entered. The REJ condition is cleared if a packet is with correct N(S) if a SABM is received, or if a SABM is transmitted and a UA received.
6. When the REJ is transmitted, error counter #6 is incremented.

RECEIVING A REJ (RESPONSE OR COMMAND)

Suppose a REJ has been received error-free with no I-field, then:

1. If the N(R) is not valid, an interrupt is generated with ER0 = C8, and a FRMR is transmitted.

2. If the N(R) is valid, and greater than NA, at least one transmitted packet is acknowledged. The appropriate ACKED bits in TLOOK are set and an XBA interrupt is generated.
3. If the N(R) is valid and less than NB, the WD2511 will begin sequential retransmission starting with V(S) = received N(R). If a packet is being transmitted when the REJ was received, that packet is aborted. If the N(R) is valid and equal to NB and a packet is being transmitted, that packet (which will be #NB) is aborted and retransmission will begin.
4. If the N(R) is valid and equal to NB and there is no packet being transmitted, there is no retransmission initiated. In this case the REJ has the same effect as an RR.
5. If in 2, 3, or 4 above, the received REJ is a command, the WD2511 will transmit a RR or RNR response at the next respond opportunity.

DEFINITION OF VALID RECEIVED N(R)

Reference

CCITT Recommendation X.25 paragraphs 2.4.10 and 2.3.4.10.

Definition

A valid received N(R) is greater than or equal to NA, and less than or equal to NB.

1. The "greater than" and "less than" relationships must be understood in a circular sense. 0 could be greater than 7 depending on the values of NA and NB.
2. If NA = NB, there is only one possible valid received N(R), N(R) = NA.
3. If NB + 1 = NA, there are seven outstanding packets and any received N(R) will be valid: N(R) = NB ACK's all of the outstanding frames, N(R) = NA ACK's none of them, and an N(R) in between ACK's some of the packets.
4. Basically, a received N(R) which is not valid is one which acknowledges a packet, or packets, never transmitted.

STATE TABLE IV
LOCAL STATION BUSY (SENT RNR: RNRX = 1)

$\overline{\text{LINK}}$	RECR	REC RDY	ACTION
1	X	X	No S-frame transmitted when link down.
1 → 0	1	1	RLOOK ready. No RNR frame sent.
1 → 0	1	0	RNR response sent immediately after link Up. RNRX set. RLNR Interrupt
1 → 0	0	X	RNR response sent immediately after link Up. RNRX set. No RLNR interrupt
0	1	1	Receiver ready to accept packets.
0	1 → 0	1	Receiver ready to accept packets.
0	1	0	RNR response sent. RNRX set. RLNR Interrupt.
0	0 → 1	1	If RNRX was set, then RNRX will be cleared after the next received packet or S-command. After that, an RR or REJ response is sent.
0	0	0	RNR response sent. RNRX set. There is no RLNR interrupt.

NOTES ON STATE TABLE IV

1. The arrows (→) indicate a change in state from the value on the left to the value on the right.
2. The RNRX status bit is set at the time the receiver-not-ready condition was established. The RNR frame will be sent immediately if no packet is being sent or after the end of the current packet.
3. When a received packet is brought into memory with RNRX = 0, the packet will be accepted provided the FCS and N(S) are correct and the I-field is not too long. The N(R) may or may not be correct but is checked separately. If N(R) is not valid, a FRMR is transmitted.
4. Whenever RNRX = 1, the I-field of a received frame is not brought into memory. For received packets, the N(S) and N(R) are checked as usual. If the N(S) is out-of-sequence, the REJ will not be transmitted.
5. If a link resetting SABM is transmitted when RNRX = 1, RNRX will be cleared when the UA is received. If the condition which caused receiver-not-ready still exists, an RNR is sent and RNRX is set. However, if the receiver instead is ready, I-field data may be brought into memory.

   The same also applies when a link resetting SABM is received.

STATE TABLE V
REMOTE STATION BUSY (RECEIVED RNR: RNRR = 1)

SEND	NA AND NB	RECVD ACK?	RECVD RNR	RECVD RR, REJ OR UA	T1 EXPIRES	ACTION
X	not =	Yes	Yes	No	No	Set RNRR. Restart T1 and N2. Update NA.
0	Equal	No	Yes	No	No	Set RNRR. Start T1.
X	not =	No	No	No	Yes	Send S-command (P = 1). If RNR subsequently received restart T1 and N2.
X	not =	Yes	No	Yes, but not UA	No	Clear RNRR. Restart T1 and N2. Update NA.
X	X	X	No	Yes	No	Clear RNRR.
0 → 1	Equal	No	No	No	No	Send next packet. Increment NB after transmission. (Then, NB does not = NA). Start T1 and N2.

2. NOTES OF TABLE V

1. If SEND = 1, it is assumed for this table that BRDY of the next TLOOK segment is set.
2. If RNRR = 1, an RR or RNR command is transmitted at T1 intervals.

SENDING S-FRAME COMMANDS

When an S-frame command is to be transmitted, an RR command is transmitted if RNRX = 0 or an RNR command is transmitted if RNRX = 1. If RNRX = 0, and a REJ is waiting to be transmitted, a REJ command is transmitted.

For all transmitted S-commands, the P bit is set to 1.

An S-command will be transmitted at T1 intervals if an RNR is received (RNRR = 1) or if T1 has expired due to waiting for an acknowledgement to previouusly transmitted packets.

CONDITIONS FOR SENDING SABM (LINK RESET)

1. FRMR received.
2. Have sent an S-command N2 times with P = 1 (at T1 intervals) without receiving an S-response with F = 1.

UNSOLICITED UA OR UNSOLICITED F BIT

If an unsolicited UA or an unsolicited F bit is received with the link up, a FRMR will be transmitted with W = 1.

SENDING AN FRMR

An FRMR may be transmitted for any of the reasons indicated in X.25 (W, X, Y, Z). An FRMR is transmitted only if the link is up.

Upon sending a FRMR, the WD2511 will not send a packet until the FRMR condition is cleared. The WD2511 will also discard any received I-fields. The FRMR condition is cleared when either a SABM or DISC is received.

If an S or I-frame is received which acknowledges a previously transmitted packet(s), the acknowledgement(s) is accepted, the appropriate ACKED bits in TLOOK are set, and there is an XBA interrupt.

While in the FRMR condition, the WD2511 will act as shown below:

FRAME RECEIVED	ACTION BY WD2511
SABM	Send UA. Clear FRMR condition. Enter information transfer phase.
DISC	Send UA. Clear FRMR condition. Enter logical disconnect state.
Packet with good N(R)	Retransmit FRMR
S-frame with good N(R) (command or response)	Retransmit FRMR
Packet or S-frame with bad N(R)	Transmit new FRMR (Z = 1)
Any frame with violation W, X, Y	Transmit new FRMR

RECEIVING AN FRMR

After a FRMR has been received:

1. The FRMR I-field will bee in the memory referenced by the current NE segment, provided the receiver was ready.
2. The SEND bit is cleared.
3. No more I-field data is allowed to come into memory until the user makes the receiver memory ready.
4. A link resetting SABM is transmitted and an error interrupt, ER0 = C0 is generated.
5. After the UA is received for the SABM, the NA, NB, NE, V(R), and V(S) are cleared to 0.

PROTOCOL SIGNIFICANCE OF TLOOK/RLOOK POINTERS

The NE, NA, and NB pointers have a relationship with the sequence counters used in the LAPB protocol.

The RLOOK pointer NE is equal to V(R) at all times if TRCV = 0. However TRCV = 1 and the link is UP, there is no guaranteed relationship between NE and V(R).

TLOOK pointer NB is the Next Block to be transmitted. If the chip is not in packet retransmission, NB is equal to the V(S) of the next new packet to be transmitted.

TLOOK pointer NA is the Next packet to be Acknowledged. It represents the V(S) number for the oldest packet in the retransmission buffer.

USE OF THE RECR BIT

The RECR (CR01) bit should be understood as an instruction to the WD2511 to enable the receiver function. The WD2511 will test RECR as soon as MDISC is cleared, and will retest RECR after each link set-up and each link reset. Once the receiver is ready, the WD2511 will not test RECR again unless there is a link set-up or a link reset.

The receiver-not-ready condition is indicated by RNRX = 1. This condition is cleared after the user makes RECR = 1 with RECRDY = 1 (in RLOOK #0) and after either a packet or an S-frame is received from the remote station.

If RECRDY of the next RLOOK is 0 but RECR = 0, there will not be an RLNR interrupt, but RNRX will be set. If RECR = 1 but the RECRDY bit of the next RLOOK segment is 0, there will be an RLNR interrupt (error code 10) and RNRX will be set.

HOST PROCEDURE FOR LINK RESET

The host should keep its own set of variables to determine the index of the Next Packet to be Received and the Next Packet to be Acknowledged because if a Link Reset occurs, the chip resets its NA, NB, and NE counters. After a Link Reset the host should look for unprocessed received packets (FRCML = 1) in the RLOOK table beginning at its Next Packet to be Received segment and proceeding in order until it finds FRCML = 0. Furthermore, if RLOOK0 has RECRDY = 1 and RECR is set to 1, a packet can be stored into RLOOK0 immediately after a Link Reset. Therefore, the host should also look for received packets beginning at RLOOK0 after a Link Reset.

The chip resets the SEND bit after a Link Reset so no new TLOOK buffers will be sent until the host sets SEND again. After a Link Reset the host should look for any unprocessed acknowledged packets (ACKED = 1) in the TLOOK table beginning at its Next Packet to be Acknowledged segment and proceeding in order until it finds a segment with ACKED = 0. Then the host must set up the TLOOK segments again so that the oldest unacknowledged packet is in TLOOK0, the next in TLOOK1, and so on, setting the BRDY = 1 in each occupied segment. (New packets may be added to the TLOOK at the next available segment.) When the host has finished setting up the TLOOK segments, it should set the SEND bit to 1. At this point packet transmission will resume if the remote station is up and is not in a receiver not ready (RNRR = 1) condition.

When presenting packets to the chip for transmission, the host should implement a timer. The value of the timer is system dependent and varies with packet size and line speed but should be in the order of seconds. If a packet has not been acknowledged by the time the timer expires, the host should check the SEND bit. If it is reset, set it to 1 again and restart the timer. If it was still set, the link must be reset. Do this by setting the MDISC bit (CR00 = 1), waiting for the link to go down (LINK = 1), then resetting MDISC (CR00 = 0), and waiting for the link to come back up (ER0 = 21 or, if RLOOK0 was not ready, 11 and LINK = 0).

For more software information refer to the WD2511 Application Note.

APPENDIX D
GLOSSARY OF DATA COMMUNICATIONS TERMS

The following is a list of industry-accepted data communications terms that are applicable to this specification.

ABM	Asynchronous Balanced Mode
ADCCP	Advanced Data Communications Control Procedure (ANSI BSR X3.66)
ANSI	American National Standards Institute
ARM	Asynchronous Response Mode
CCITT	International Consultative Committee for Telegraphy and Telephony
CMDR	Command Reject. A U-Frame
DCE	Data Circuit Termination Equipment (the network side of the DTE/DCE link)
DISC	Disconnect. A U-Frame
DTE	Data Terminal Equipment
DM	Disconnect Mode. A U-Frame (LAPB, only)
ECMA	European Computer Manufacturers Association
FCS	Frame Check Sequence
FDX	Full Duplex (also called "two way simultaneous")
FRAME	Basic serial block of bit-oriented data. Includes leading and trailing flags, address field, control field, FCS field, and an optional information field.
FRMR	Frame Reject. A U-Frame (LAPB, only)
HDLC	High-Level Data Link Control (ISO 3309)
HDX	Half Duplex (also called "two way alternate")
HOST	Another name for a DTE
I-Frame	Information Frame. Control field bit 0 is 0. In X.25 an I-frame is a packet.
ISO	International Standards Organization
LINK	The logical and physical connection between two data terminals
LAP	Link Access Procedure
LAPB	Link Access Procedure Balanced
N2	Maximum number of retransmissions of a frame. (Also called retransmission count variable.)
NODE	Another name for a DCE or DTE.
N(R)	Sequence number of next frame expected to be received.
N(S)	Sequence number of current frame being transmitted.
OCTET	An 8-bit byte
PACKET	An I-Frame in X.25
PAD	Packet Assembly/Disassembly facility
REJ*	Reject. An S-Frame
RNR*	Receiver Not Ready. An S-Frame
RR*	Receiver Ready. An S-Frame
S-Frame	Supervisory Frame. Control field bit 0 = 1 and bit 1 = 0
SARM	Set Asynchronous Response Mode. (LAP, only)
SABM	Set Asynchronous Balanced Mode. (LAPB, only)
SDLC	Synchronous Data Link Control (IBM document GA27-3093)
T1	A Primary Timer for a delay in waiting for a response to a frame
U-Frame	Unnumbered Frame. Control Field bit 0 = 1 and bit 1 = 1
UA	Unnumbered Acknowledge. A U-Frame
X.25	Recommendation by CCITT on Interfacing to Public Packet Switching Networks
X.3, X.28, X.29	Recommendations by CCITT involving PAD facilities

*There are also RR, RNR, and REJ packets which are not the same as the S-frame RR, RNR and REJ discussed in this document.

See page 383 for ordering information.

WD2511 Application Note

This application note provides an introduction to the X.25 communication protocol and introduces the ISO reference model. The link layer of X.25 is highlighted as it can today be implemented with a single LSI device, the WD2511.

The bulk of this document provides details of the hardware and software interfaces that a user typically encounters when using the WD2511. Schematic and timing diagrams for a typical Z80 interface along with high level flowcharts for initialization and operation are given. This circuitry is applicable for applications where the TC/RC speed is 64 Kbps and below.

CONTENTS

1.0 THE WD2511 GENERAL DESCRIPTION

The WD2511 is an LSI device that fully handles the link level (level 2) of the CCITT X.25 communications protocol.

In addition to the traditional parallel/serial converters and FCS logic, the WD2511 incorporates a highly efficient micro-programmed processor that fully handles the required link set-up and frame sequencing operations conventionally delegated to a "user defined" processor. The WD2511 also contains an intelligent two-channel DMA controller to further simplify its integration into a user's system.

2.0 THE WD2511 AND THE ISO MODEL

The CCITT X.25 recommendation comprises three levels of protocols (Level 1 to 3). See Figure 1.

Level 1 is the physical level, which concerns the actual means of bit transmission across a physical medium.

Level 2 is the link level which includes frame formatting, error control and link control.

Level 3 is the packet (network) level which controls the traffic of the different virtual calls and multiplexes these for passage over the physical line.

These three levels are completely independent of each other, which allows changes to be made to one level without disrupting the operation of any other level. An adjacent level is affected only if the changes affect the interface to that level.

Each level performs one well defined set of functions, using only a well defined set of services provided by the level below. These functions implement a set of services that can be accessed only from the level above. Each level is strictly controlled by the systems engineer according to formal functional and interface specifications.

The WD2511 implements level 2. Without additional logic, it generates the frame, performs error checking, performs link management (set up/disconnect) and ensures reliable data transmission by evaluating the sequence number associated with each I-frame. The device automatically acknowledges received I-frames and fully supports up to 7 outstanding (unacknowledged) frames, including retransmission if required.

3.0 HARDWARE

The WD2511 must be connected to the Physical Level (Level 1). This generally amounts to simple line drivers/receivers.

A typical X.25 DTE/DCE station block diagram is shown in Figure 2. Figure 3 shows a circuit diagram of the actual X.25 hardware interface of this same station. Table 1 is a description of signal functions for this circuit diagram. This is to be connected directly to a Z80 microprocessor on one side and an EIA RS-422 interface on the other side.

Figures 4 and 5 are DMA cycle timing diagrams for this particular station.

General notes to this interface:

- A modem would be needed for long-distance communication lines.
- The hardware interface in Figure 3 includes all hardware options. Simpler interfacing is possible.
- The function of the CPU Bus Driver Control Circuit (CBDCC) is to control the direction and/or timing of the data-line transceivers and the two address latches.
- If the CPU clock frequency is not higher than the WD2511 CLK maximum frequency, the High Speed Control Circuit (HSCC) is not needed. The function of the HSCC circuit is to divide a high speed CPU

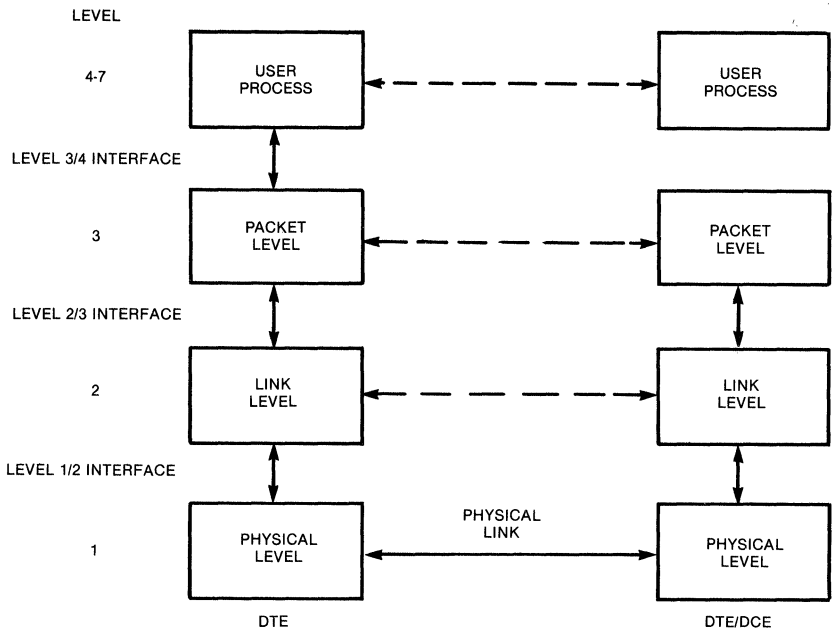


Figure 1. LAYERED ARCHITECTURE FOR COMPUTER NETWORKS

The only real physical connection between the two stations (DTE and DTE/DCE) is the Physical Link between the two physical layers. The other connections shown between two of the same layers (peer to peer interface) is not a physical but rather a logical connection made up by the respective protocols for that particular level.

Each level n "interfaces" to the corresponding level n on the other side of the Data Communication Link through the level n-1, then n-2 etc., via the physical link and up through the levels to n-2, n-1 and to level n.

clock signal (0) down to half the frequency (01A). It also delays the reset of $\overline{BUSRQ}$ with one additional 01 clock cycle when a high speed CPU clock is used. These functions are needed to establish a time window of at least 500ns between $\overline{DACK}$ being active and a CPU Write/Read function.

- When a high speed CPU clock is used, connect 01A signal to 01 signal and $\overline{BUSRQA}$ signal to $\overline{BUSRQ}$ signal. When a low speed CPU clock is used, connect CPU clock (0) direct to 01 signal and $\overline{BUSRQ2}$ signal to $\overline{BUSRQ}$ signal.
- The DMA I/O circuit matches the timing between the Z80 and the WD2511.
- The $\overline{RTS}$ open collector output needs a pull-up resistor.
- In this particular example, line drivers/receivers are of type EIA RS-422. However, RS-232C or RS-423 can also easily be used.
- Port A of a PIO in this example is programmed to be an output. In this case, the CPU controls the DTR output to the modem. Port B of the PIO is programmed to be interrupt controlled inputs; the CPU can be interrupted by $\overline{DSR}$ and/or $\overline{INTR}$ as programmed.
- $\overline{MRW}$ (Memory Read/Write) signal enables the output of the memory address decoder for the computer system memory chips. As an example, if a PROM type 28S42 is used as the memory address decoder, $\overline{MRW}$ is connected direct to $\overline{E}$ (Pin 15) input.
- The WD2511 $\overline{CS}$ input is to be connected to a port address decoder (or memory address decoder). $\overline{MWE}$ is connected to all $\overline{WE}$ inputs, and $\overline{MOE}$ is connected to all $\overline{OE}$ inputs of the system memory chips.
- $\overline{REPLY}$ output is not used in this application.

3.1 READ/WRITE CONTROL OF I/O REGISTERS

The sixteen I/O registers are directly accessible from the CPU data bus (DAL0-DAL7) by a read and/or write operation by the CPU. The CPU must activate the WD2511 register address (IA0-IA3). Chip Select (CS). Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation. The read/write operation is

completed when $\overline{CS}$ or $\overline{RE}/\overline{WE}$ is brought high. During a write operation, the falling edge of $\overline{WE}$ will initiate a WD2511 write cycle. The addressed register will then be loaded with the content of the Data Bus. The rising edge of $\overline{WE}$ will latch that data into the addressed register.

During a read operation, the falling edge of $\overline{RE}$ will initiate a WD2511 read cycle. The addressed register will then place its content onto the Data Bus.

The CPU must set-up all transmit data, TSADR HI and LO, TCNT HI and LO, and residual bits before setting BRDY in the applicable TLOOK segment.

The CPU must set aside receiver memory (at least one chain segment with transfer address), and set-up RSADR HI and LO before setting REC RDY in the applicable RLOOK segment.

3.2 DMA IN/OUT OPERATION

The Direct Memory Access (DMA) operation is completely controlled by the WD2511. During a DMA cycle, the CPU sets its address bus, data bus and three-state control signals to their high impedance states.

(See DMA In/Out timing diagrams, Figures 4 and 5.)

In this application example, the data bus transceivers are permanently enabled (low impedance state). When the CPU has control, the direction of these transceivers is pointing from the CPU bus towards the WD2511. During a DMA In cycle, this is not changed. During a DMA Out cycle however, the direction is reversed (WD2511 towards the CPU bus).

The address bus latches are in high impedance state while the CPU has control of the bus. When the WD2511 has control of the CPU bus, the address latches are in the low impedance state. During the DMA Out cycle, these latches function as regular bus drivers. During the DMA In cycle however, the address gets latched to assure enough data hold time for the WD2511.

3.2.1 DMA IN

During a DMA In cycle, the task of transferring one byte of I-field data from memory into the WD2511 is performed. The CPU time (in the example described in this paragraph to execute this task) is five T-states for a low speed CPU clock system and ten T-states for a high speed CPU clock system.

The DMA In function starts when the WD2511 is ready to receive a byte from memory to be transmitted out to the remote station. This condition causes the $\overline{DRQI}$ signal to go LO, which in turn activates the $\overline{BUSRQ}$ (Bus Request) signal. Also at this time (ADRV bit = 1), the WD2511 presents the address (on A0-A15) of the data byte to be retrieved from memory.

The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last CPU clock (0) period of any machine cycle. In this case, because the $\overline{BUSRQ}$ signal is active, the CPU goes into high impedance state with the rising edge of the next CPU clock pulse. At this time, the CPU also switches the control over to the WD2511 by activating the $\overline{BUSAK}$ signal. This causes $\overline{DACK}$ to go LO at the following rising edge of 01 clock. This is the actual indication for the WD2511 to start the DMA In cycle. $\overline{DACK}$ also causes $\overline{DRQI}$ to return to the HI state.

At the next rising edge of the 01 clock, $\overline{MOE}$ (Memory Output Enable) is activated. This causes the memory to output the addressed data byte onto the Data Bus. Also, the address is now latched into the address bus latches (74LS373) at this time.

At the next falling edge of the 01 clock, $\overline{DACK}$ gets deactivated, causing the WD2511 to latch the data byte (DAL0-DAL7) and to set its address lines (A0-A15) to logical HI state (ADRV bit = 1). The address bus latches hold the address active until $\overline{DMOE}$ signal is deactivated.

At the next rising edge of the 01 clock (low speed CPU clock), $\overline{BUSRQ}$ gets deactivated. When high speed CPU clock is used, $\overline{BUSRQ}$ is deactivated after an additional 01 clock cycle.

At the next following rising edge of 01 clock, $\overline{BUSRQ}$ is sampled by the CPU. This causes $\overline{BUSAK}$ and $\overline{MOE}$ to become deactivated, but not until the next falling edge of the CPU (0) clock. This is the end of the DMA In cycle. At the next rising edge of the CPU clock, the CPU again controls the CPU bus.

3.2.2 DMA OUT

This operation is very similar to the DMA In function. During this cycle, one byte of I-field data is transferred from the WD2511 to the memory. The CPU-time in this example described to perform this task is the same as for the DMA In cycle.

The DMA Out function starts when the WD2511 is holding a received I-field byte and is ready to transfer this to the memory. This condition activates the $\overline{DRQO}$ signal, which in turn sets the $\overline{BUSRQ}$ to LO. Also at this time (ADRV bit = 1), the WD2511 presents the address to the memory location to where the respective data byte is to be loaded.

The $\overline{BUSRQ}$ signal is sampled by the CPU with the rising edge of the last CPU clock period of any machine cycle. Since the $\overline{BUSRQ}$ signal is active, the CPU goes into high impedance state with the rising edge of the following CPU clock pulse. Now the CPU also switches the control over to the WD2511 by activating the $\overline{BUSAK}$ signal. This causes $\overline{DACK}$ to go LO at the next rising edge of 01 clock, which indicates to the WD2511 to start the DMA Out cycle. This causes $\overline{DRQO}$ to reset back to HI state and to load the data byte to be transferred onto the data-bus.

At the next rising edge of the 01 clock, $\overline{MWE}$ (Memory Write Enable) is activated. This causes the memory to input the addressed data byte.

At the following rising edge of the 01 clock, $\overline{MWE}$ goes HI, latching the data into the memory. Also at this time

TABLE 1. SIGNAL NAMES FOR THE HARDWARE INTERFACE (See Note)

NAME	SYMBOL	FUNCTION
RECEIVE	RCV	When activated (LO), sets the direction of the data bus transceivers from WD2511 towards the CPU bus. This is done only during CPU Read or DMA Out cycle.
DRM TRANSFER	$\overline{\text{DTFR}}$	When activated (LO), enables the output of the address bus latches. This is done during a DMA In/Out cycle.
DMA MEMORY OUTPUT ENABLE	$\overline{\text{DMOE}}$	Is activated during a DMA In cycle. Generates the $\overline{\text{MOE}}$ signal and latches the DMA In addresses.
MEMORY OUTPUT ENABLE	$\overline{\text{MOE}}$	Is activated during a DMA In or a CPU Read cycle. Enables the memory outputs. Is to be connected to the $\overline{\text{OE}}$ pin of the memory circuits.
MEMORY WRITE ENABLE	$\overline{\text{MWE}}$	Is activated during a DMA Out or a CPU Write Cycle. Enables the memory write function. Is to be connected to the $\overline{\text{WE}}$ input of the memory circuits.
MEMORY READ/WRITE	$\overline{\text{MRW}}$	Is activated during a DMA In/Out function or a Memory Read/Write cycle by the CPU. Enables the output of the Memory Address decoder.
DMA OUT	DMA OUT	Is activated during a DMA Out function.
DMA IN	DMA IN	Is activated during a DMA In function.
INTERNAL LOOP	ILOOP	Is activated during an internal loop-back test. Keeps the $\overline{\text{RTS}}$ signal to the modem in off condition and logically connects $\overline{\text{RTS}}$ to $\overline{\text{CTS}}$.
BUS ACKNOWLEDGE 1	$\overline{\text{BUSAK1}}$	When active, indicates that the CPU has switched bus control over to the WD2511. Compared to $\overline{\text{BUSAK}}$ signal, this is delayed one 01 clock cycle when going LO to allow a time window of at least 500 ns before $\overline{\text{DACK}}$ becomes activated.
BUS REQUEST 1	$\overline{\text{BUSRQ1}}$	When active, requests the CPU via $\overline{\text{BUSRQ2}}$ and $\overline{\text{BUSRQ}}$ (low speed CPU clock) to switch control over to the WD2511.
BUS REQUEST 2	$\overline{\text{BUSRQ2}}$	Same function as $\overline{\text{BUSRQ1}}$, except that $\overline{\text{BUSRQ2}}$ is delayed one 01 cycle when going HI. The delay allows a time window of at least 500 ns between $\overline{\text{DACK}}$ being active and a CPU Read/Write function.
BUS REQUEST A	$\overline{\text{BUSRQA}}$	Same function as $\overline{\text{BUSRQ2}}$, except is delayed an additional 01 cycle when going HI. This delay allows the necessary 500 ns time window between $\overline{\text{DACK}}$ being active and a CPU Read/Write function when an high speed CPU clock is used. This is then directly driving the $\overline{\text{BUSRQ}}$ signal.

(low speed CPU clock), $\overline{\text{BUSRQ}}$ signal gets deactivated. When high speed CPU clock is used, $\overline{\text{BUSRQ}}$ is deactivated after an additional 01 clock cycle.

At the next rising edge of 01 clock, the $\overline{\text{BUSRQ}}$ signal is sampled by the CPU.

$\overline{\text{DACK}}$ goes HI half a 01 clock cycle after $\overline{\text{MWE}}$ goes HI. This ends the DMA Out cycle by the WD2511 setting its data-lines in high impedance state and the address-lines (A0-A15) to logical HI state (ADRV bit = 1).

After CPU has sampled and detected $\overline{\text{BUSRQ}}$ being deactivated, it resets $\overline{\text{BUSAK}}$ to HI at the next falling edge of the CPU clock.

At the next rising edge of the CPU clock, the CPU again controls the bus.

TABLE 1. (Continued) SIGNAL NAMES FOR THE HARDWARE INTERFACE (See Note)

NAME	SYMBOL	FUNCTION
01	01	Clock used for timing of this hardware interface. The 01 frequency is not allowed to be higher than the CLK maximum frequency of the WD2511. When a low speed CPU clock is used, 01 signal is connected directly to the CPU clock (0). When a high speed CPU clock is used, this is connected to the 01A signal.
01A	01A	Clock signal with half the CPU clock frequency. This is driving the 01 clock when a high speed CPU clock is used.
+ 5 RESISTIVE	+ 5R	+ 5V through a resistor.

NOTE: Signals described in this paragraph are signals generated by this circuitry only. Other signals are described in either the WD2511 device specification or in the Z80 CPU data sheets.

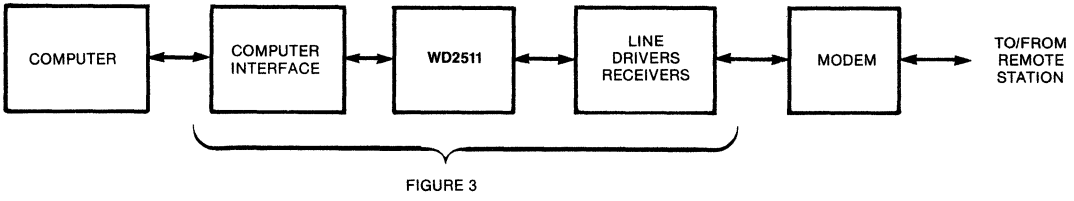


FIGURE 2. DTE/DCE STATION BLOCK DIAGRAM

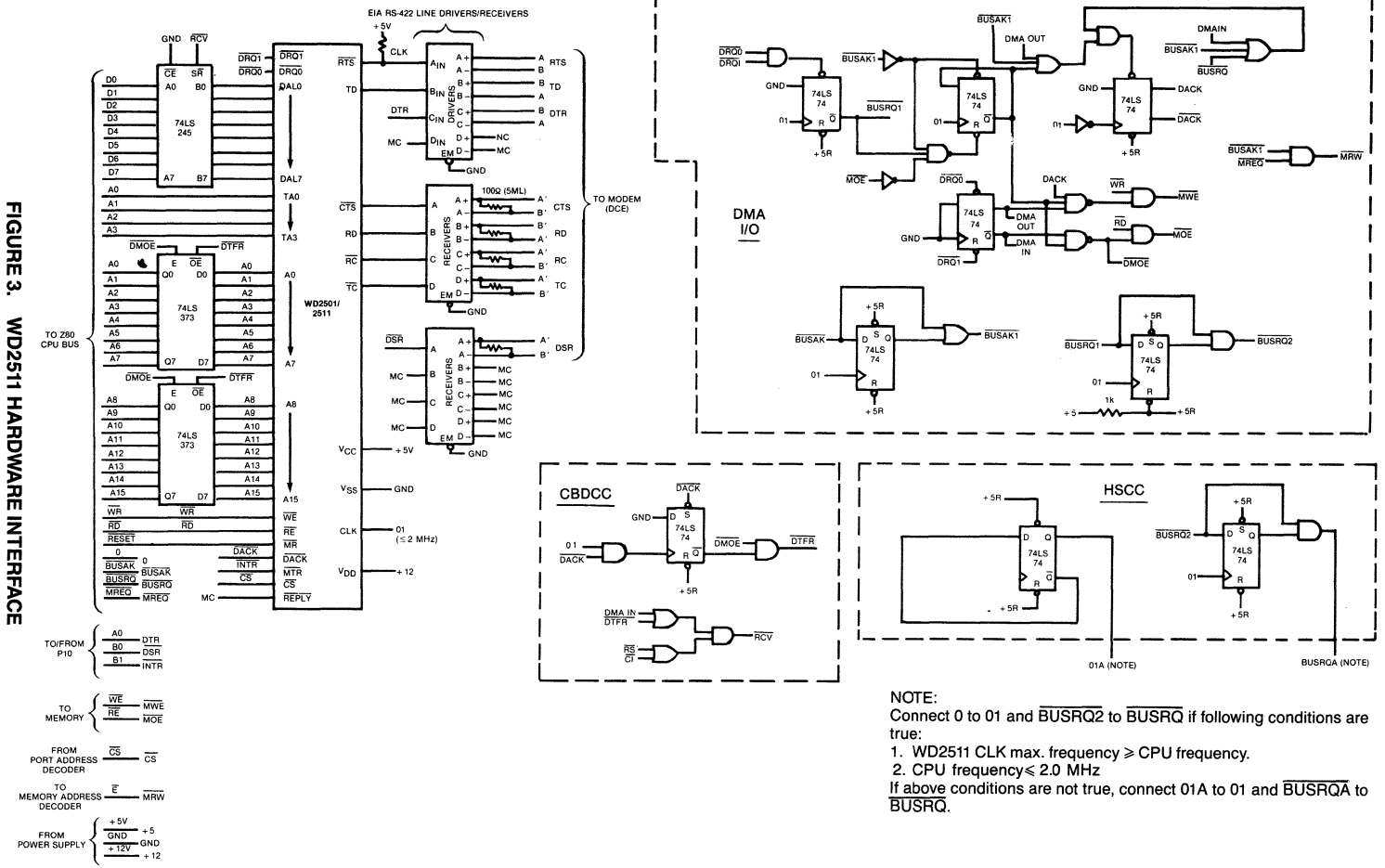
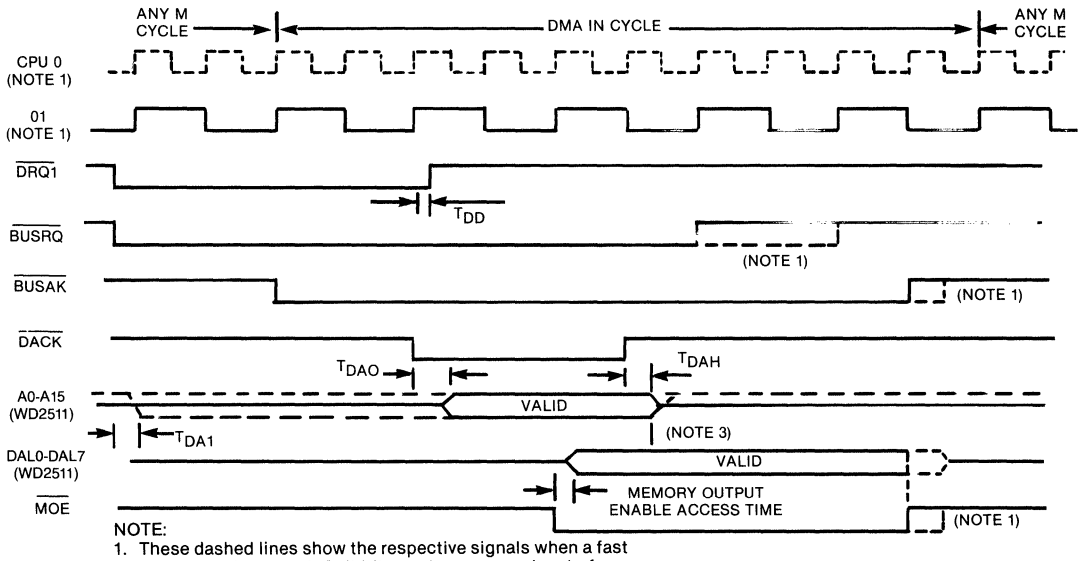


FIGURE 3. WD2511 HARDWARE INTERFACE

NOTE:
Connect 0 to 01 and $\overline{\text{BUSRQ2}}$ to $\overline{\text{BUSRQ}}$ if following conditions are true:

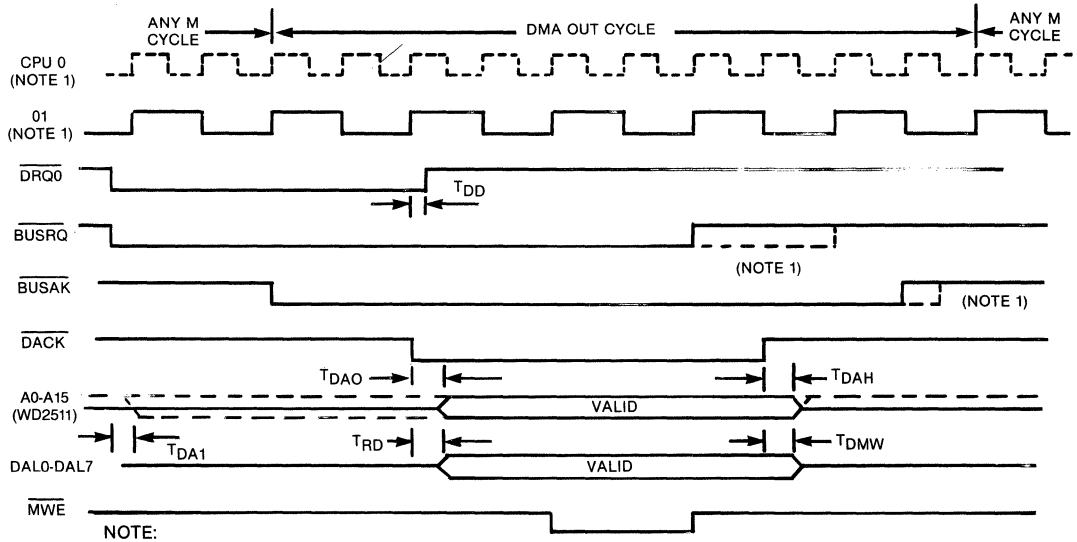
1. WD2511 CLK max. frequency ⩾ CPU frequency.
2. CPU frequency⩽ 2.0 MHz

If above conditions are not true, connect 01A to 01 and $\overline{\text{BUSRQA}}$ to $\overline{\text{BUSRQ}}$.



NOTE:
1. These dashed lines show the respective signals when a fast CPU 0 clock is used. Solid lines show same signals for a slow CPU 0 clock (CPU 0 = 01).
2. Propagation delay is omitted in this diagram unless timing symbol is shown.
3. Data would become non-valid after the address becomes non-valid if address latches were not used.

Figure 4. DMA IN TIMING



NOTE:
1. These dashed lines show the respective signals when a fast CPU 0 clock is used. Solid lines show same signals for a slow CPU 0 clock (CPU 0 = 01).
2. Propagation delay is omitted in this diagram unless timing symbol is shown.

Figure 5. DMA OUT TIMING

3.3 SERIAL INTERFACE

The receiver and transmitter sub-systems are completely independent of each other, the CPU Read/Write functions and the DMA In/Out functions.

The serial data is synchronized by the externally supplied $\overline{TC}$ clock and $\overline{RC}$ clock. The falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data.

After initilization and before the first frame is sent, the TD output sends Idles (continuous 1s).

After the first frame is sent or the ACTIVE/$\overline{PASSIVE}$ bit is set, continuous flags are sent in between frames.

For detailed information on what type of frames are sent for certain conditions, see the WD2511 specifications.

4.0 SOFTWARE

Initialization of the WD2511 and I-field data processing (level 3) is accomplished by user written software. This software need not be realtime, since the WD2511 responds to link exceptions and overhead functions on its own.

Configuring the WD2511 for certain test functions, modes, timer values, location of initial memory pointers, chain buffer lengths and link level addresses is performed via the sixteen I/O registers.

All buffer management support, buffer chaining and free/busy flags occur in user memory. Here two look-up tables (TLOOK/RLOOK), located in the user memory, contain pointers/counters for up to eight outstanding transmit/receive packets. The WD2511 contains only one address pointer which is the starting address of Segment #0 in the TLOOK table. Segment #0 in the RLOOK table always begins 40(Hex) bytes after TLOOK, Segment #0, byte #0. See section "Memory Access Scheme" in the WD2511 specifications.

Link monitoring is done by use of the I/O registers and the memory buffers. The WD2511 indicates to the system CPU that a certain event has occurred by setting a bit in status register 1 and setting the interrupt flag. This indicates whether a packet has been received, a transmitted packet has been acknowledged, a non-recoverable error condition or some other condition needs the attention of the CPU.

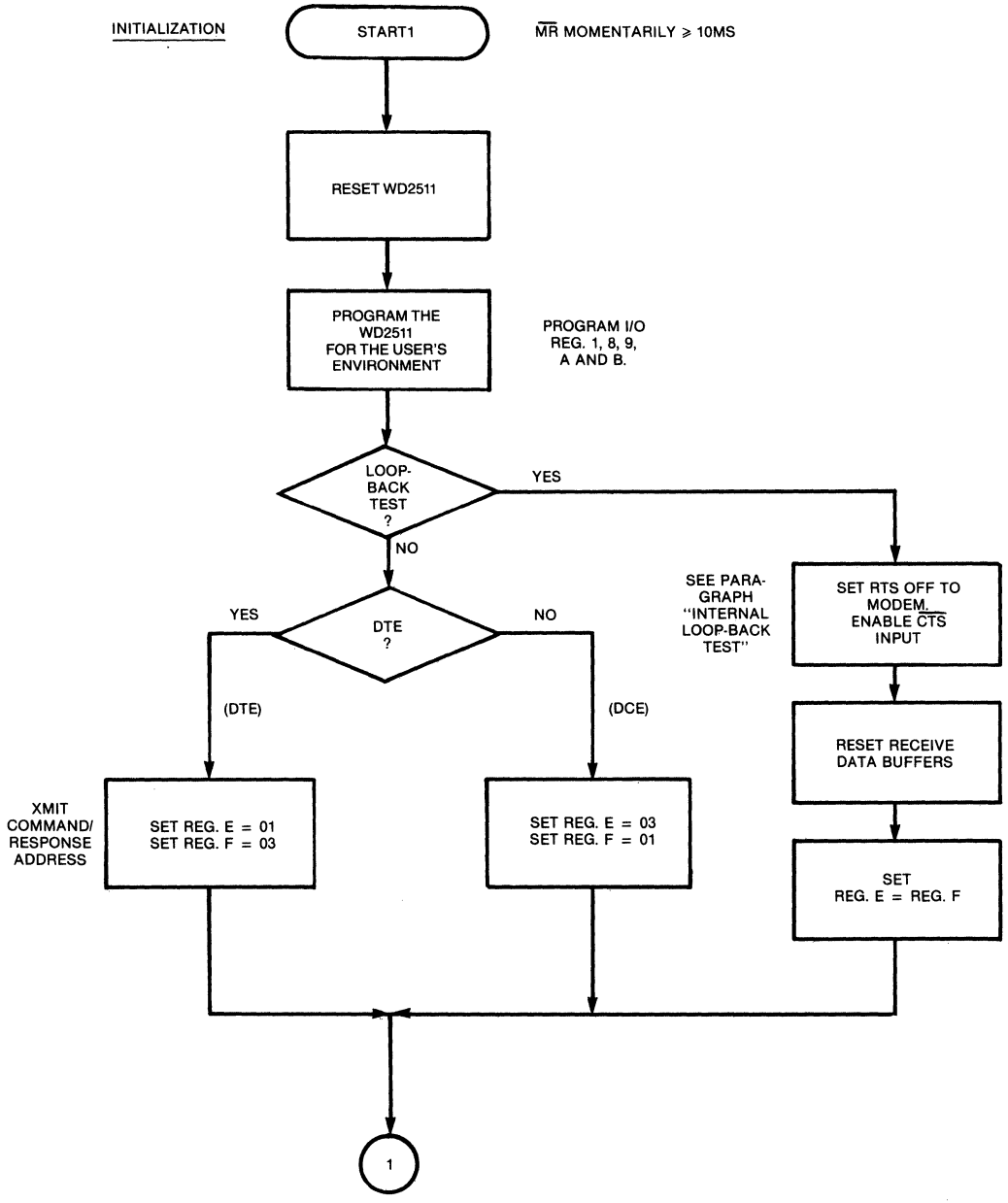
In this section a flow-chart is given to show the user how to program the WD2511. For more details refer to the data sheets.

The flow for programming/monitoring the WD2511 for transmitting or receiving a packet(s) or for a loop-back test is shown in the flowchart below. The flow starts at START1 if a power-up was just done and/or if no data communication environment programming (initialization) has been done.

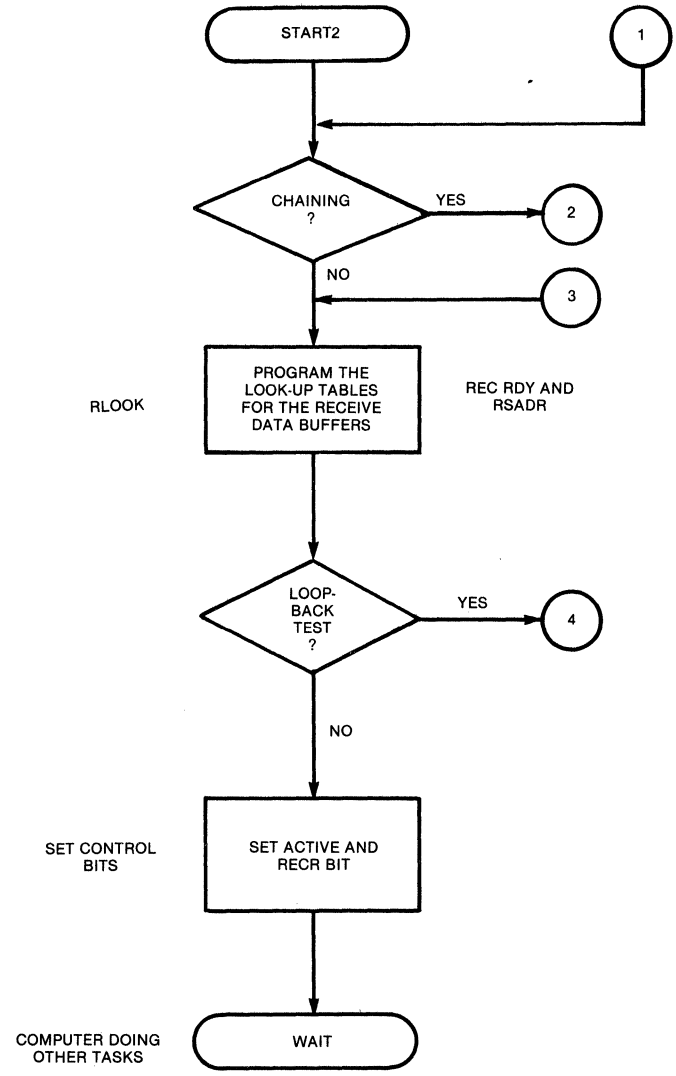
If initialization is complete, the flow starts at START2 when the WD2511 is to be enabled to receive a packet(s).

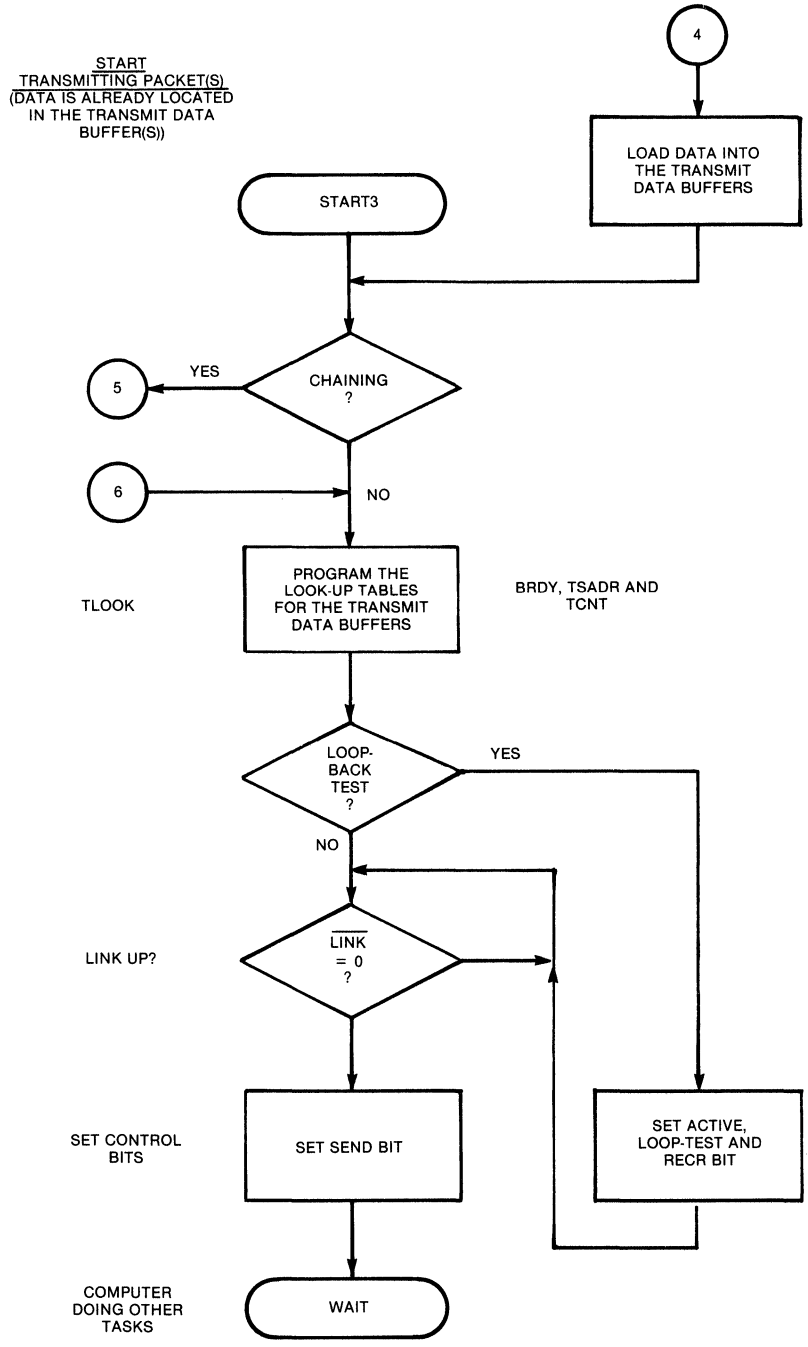
If a packet is to be transmitted and initialization is complete, the flow starts at START3.

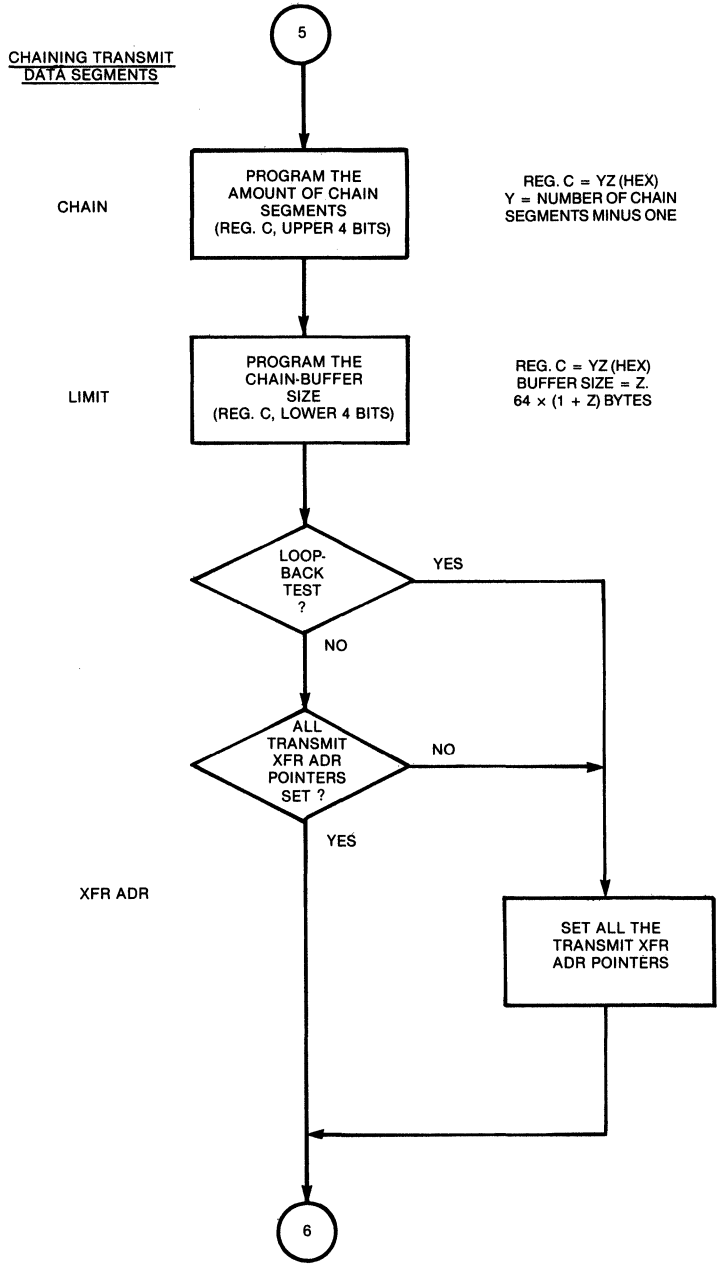
WD2511 PROGRAMMING FLOWCHART

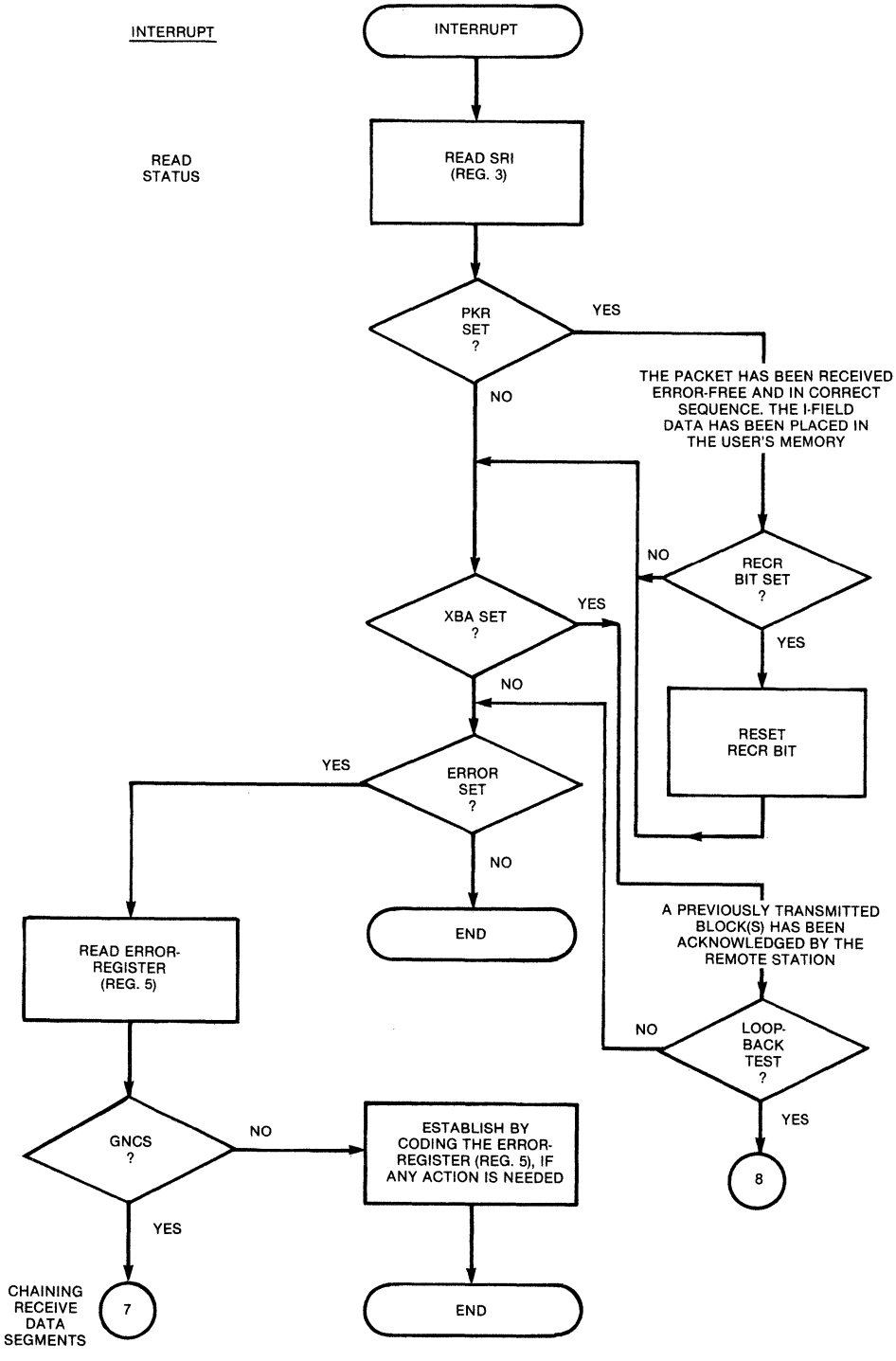


ENABLE RECEPTION
OF PACKET(S)

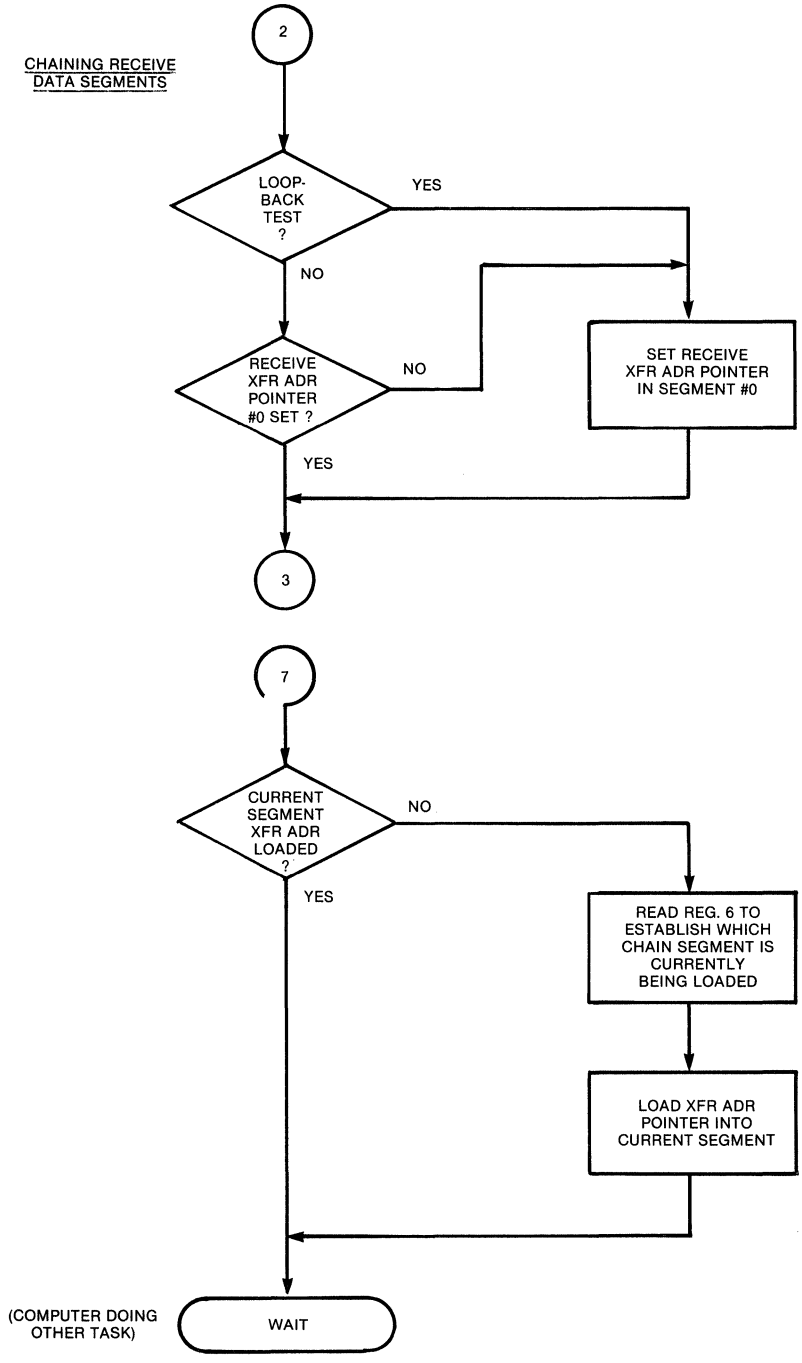


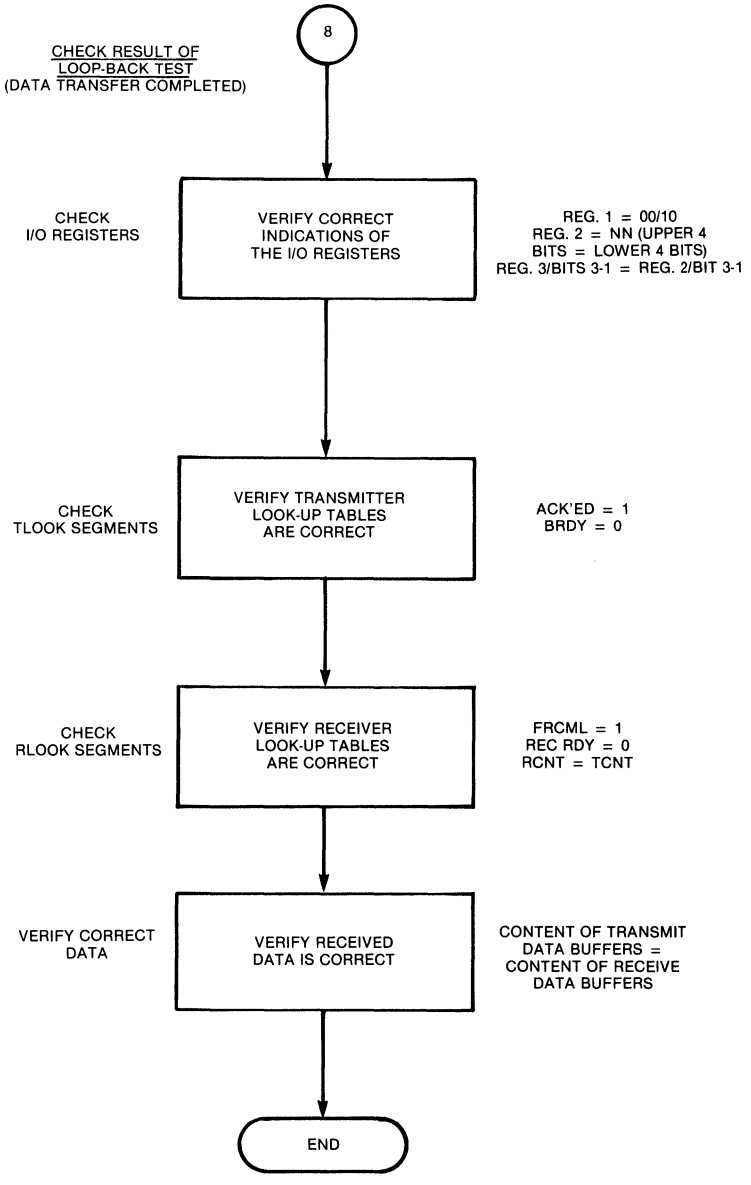

START
TRANSMITTING PACKET(S)
(DATA IS ALREADY LOCATED
IN THE TRANSMIT DATA
BUFFER(S))
START3
4
LOAD DATA INTO
THE TRANSMIT
DATA BUFFERS
CHAINING
?
YES
5
6
NO
TLOOK
PROGRAM THE
LOOK-UP TABLES
FOR THE TRANSMIT
DATA BUFFERS
BRDY, TSADR AND
TCNT
LOOP-
BACK
TEST
?
YES
NO
LINK UP?
LINK
= 0
?
SET CONTROL
BITS
SET SEND BIT
SET ACTIVE,
LOOP-TEST AND
RECR BIT
COMPUTER
DOING OTHER
TASKS
WAIT


CHAINING TRANSMIT DATA SEGMENTS
5
CHAIN
PROGRAM THE AMOUNT OF CHAIN SEGMENTS (REG. C, UPPER 4 BITS)
REG. C = YZ (HEX)
Y = NUMBER OF CHAIN SEGMENTS MINUS ONE
LIMIT
PROGRAM THE CHAIN-BUFFER SIZE (REG. C, LOWER 4 BITS)
REG. C = YZ (HEX)
BUFFER SIZE = Z.
64 × (1 + Z) BYTES
LOOP-BACK TEST ?
YES
NO
ALL TRANSMIT XFR ADR POINTERS SET ?
NO
YES
XFR ADR
SET ALL THE TRANSMIT XFR ADR POINTERS
6


INTERRUPT
INTERRUPT
READ STATUS
READ SRI (REG. 3)
PKR SET ?
YES
NO
THE PACKET HAS BEEN RECEIVED ERROR-FREE AND IN CORRECT SEQUENCE. THE I-FIELD DATA HAS BEEN PLACED IN THE USER'S MEMORY
RECR BIT SET ?
NO
YES
XBA SET ?
YES
NO
RESET RECR BIT
ERROR SET ?
YES
NO
END
A PREVIOUSLY TRANSMITTED BLOCK(S) HAS BEEN ACKNOWLEDGED BY THE REMOTE STATION
READ ERROR-REGISTER (REG. 5)
LOOP-BACK TEST ?
NO
YES
GNCS ?
NO
ESTABLISH BY CODING THE ERROR-REGISTER (REG. 5), IF ANY ACTION IS NEEDED
8
YES
CHAINING RECEIVE DATA SEGMENTS
7
END

CHAINING RECEIVE DATA SEGMENTS




8
CHECK RESULT OF LOOP-BACK TEST (DATA TRANSFER COMPLETED)
CHECK I/O REGISTERS
VERIFY CORRECT INDICATIONS OF THE I/O REGISTERS
REG. 1 = 00/10
REG. 2 = NN (UPPER 4 BITS = LOWER 4 BITS)
REG. 3/BITS 3-1 = REG. 2/BIT 3-1
CHECK TLOOK SEGMENTS
VERIFY TRANSMITTER LOOK-UP TABLES ARE CORRECT
ACK'ED = 1
BRDY = 0
CHECK RLOOK SEGMENTS
VERIFY RECEIVER LOOK-UP TABLES ARE CORRECT
FRCML = 1
REC RDY = 0
RCNT = TCNT
VERIFY CORRECT DATA
VERIFY RECEIVED DATA IS CORRECT
CONTENT OF TRANSMIT DATA BUFFERS = CONTENT OF RECEIVE DATA BUFFERS
END

4.1 INTERNAL LOOP-BACK TEST (Example 1)

The loop-back test feature is an internal programmable loop-back of data, enabling the user to make an almost complete test of the WD2511. It allows diagnostic testing of the WD2511 and the interfacing circuitry. In this mode, transmitted data to the TD pin is internally routed to the received data input circuitry, thus allowing this WD2511 to set-up a link, send a number of packets to itself and then reset the link.

The $\overline{RC}$ clock is internally connected to $\overline{TC}$ clock. $\overline{CTS}$ input however, must be connected externally to GND or the $\overline{RTS}$ output.

The loop-back test allows the verifying of proper operation of practically all the various functions of the WD2511. The features tested here, the addresses and values of the variables chosen are only used as examples and are as follows:

TLOOK segments starting address = 0800H
Transmit Data buffer #0 starting address = 1000H
Received Data buffer #0 starting address = 1800H
Number of packets transferred = 1
Number of I-field bytes per packet = 1024
Number of residual bits = 0
T1 = 101H
N2 = 20H

Chaining is used in this example. The 1024 bytes are divided into 256 byte chain segments. Five segments are needed for this operation with 256 bytes of I-field data and two XFR ADR bytes per segment in the first four chain-segments. The rest of the I-field data (8 bytes) are located in the fifth chain-segment.

Programming:

CHAIN = 4 = number of CHAIN segments – 1
LIMIT = 3 = (number of bytes per segment divided by 64) – 1

For buffer management programming, see memory access scheme in Figure 7.

XMIT Command Address and XMIT Response Address (REG. E and F) must be the same value.

In some applications it is necessary to keep the $\overline{RTS}$ signal to the modem in the Off condition during internal loop-back test. Also, to accomplish the most complete test, $\overline{RTS}$ output should be connected to $\overline{CTS}$ input externally (not done internally). Figure 6 shows one example of how to implement these two functions. The ILOOP signal is connected directly to a PIO output.

In the loop-back test example shown in this section, the logic in Figure 6 is used and contains the Z80 CPU, programmable I/O (PIO) etc., as shown in Figure 3.

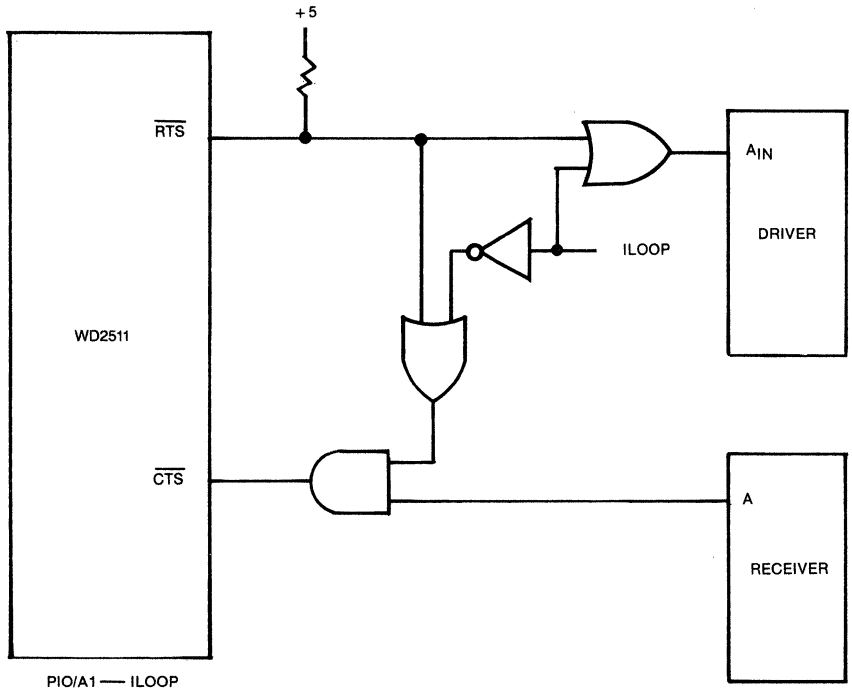


Figure 6. LOGIC FOR INTERNAL LOOP-BACK TEST

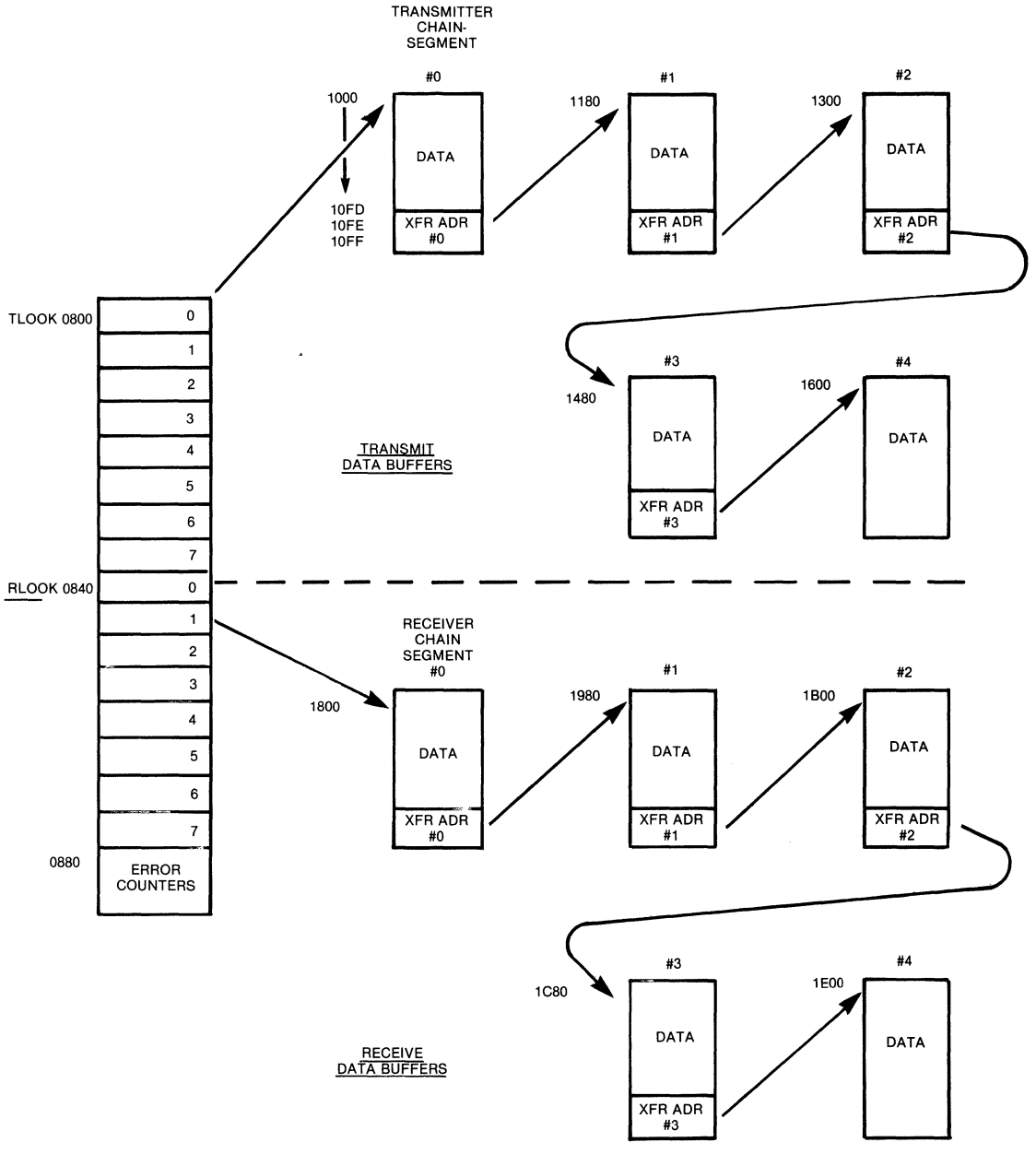


Figure 7. MEMORY ACCESS SCHEME FOR LOOP-BACK TEST (Example 1)

APPENDIX A
GLOSSARY OF DATA COMMUNICATIONS TERMS

The following is a list of industry-accepted data communications terms that are applicable to this specification.

ABM	Asynchronous Balanced Mode
ADCCP	Advanced Data Communications Control Procedure (ANSI BSR X3.66)
ANSI	American National Standards Institute
ARM	Asynchronous Response Mode
CCITT	International Consultative Committee for Telegraphy and Telephony
CMDR	Command Reject. A U-Frame
DCE	Data Circuit Termination Equipment (the network side of the DTE/DCE link)
DISC	Disconnect. A U-Frame
DTE	Data Terminal Equipment
DM	Disconnect Mode. A U-Frame (LAPB, only)
ECMA	European Computer Manufacturers Association
FCS	Frame Check Sequence
FDX	Full Duplex (also called "two way simultaneous")
FRAME	Basic serial block of bit-oriented data. Includes leading and trailing flags, address field, control field, FCS field, and an optional information field.
FRMR	Frame Reject. A U-Frame (LAPB, only)
HDLC	High-Level Data Link Control (ISO 3309)
HDX	Half Duplex (also called "two way alternate")
HOST	Another name for a DTE
I-Frame	Information Frame. Control field bit 0 is 0. In X.25 an I-frame is a packet.
ISO	International Standards Organization
LINK	The logical and physical connection between two data terminals
LAP	Link Access Procedure
LAPB	Link Access Procedure Balanced
N2	Maximum number of retransmissions of a frame. (Also called retransmission count variable.)
NODE	Another name for a DCE or DTE.
N(R)	Sequence number of next frame expected to be received.
N(S)	Sequence number of current frame being transmitted.
OCTET	An 8-bit byte
PACKET	An I-Frame in X.25
PAD	Packet Assembly/Disassembly facility
REJ*	Reject. An S-Frame
RNR*	Receiver Not Ready. An S-Frame
RR*	Receiver Ready. An S-Frame
S-Frame	Supervisory Frame. Control field bit 0 = 1 and bit 1 = 0
SARM	Set Asynchronous Response Mode. (LAP, only)
SABM	Set Asynchronous Balanced Mode. (LAPB, only)
SDLC	Synchronous Data Link Control (IBM document GA27-3093)
T1	A Primary Timer for a delay in waiting for a response to a frame
U-Frame	Unnumbered Frame. Control Field bit 0 = 1 and bit 1 = 1
UA	Unnumbered Acknowledge. A U-Frame
X.25	Recommendation by CCITT on Interfacing to Public Packet Switching Networks
X.3, X.28, X.29	Recommendations by CCITT involving PAD facilities

*There are also RR, RNR, and REJ packets which are not the same as the S-frame RR, RNR and REJ discussed in this document.

APPENDIX B

THE DIFFERENCE BETWEEN LAP AND LAPB

In March 1976, the CCITT adopted Recommendation X.25 as an interface standard for public packet-switching networks. The link level procedure adopted was called Link Access Procedure (LAP) and used the HDLC Asynchronous Response Mode (ARM). However, ARM was not designed for peer-to-peer communications so LAP had some subtle problems. Therefore, in 1977, when Provisional Recommendation X.25 was adopted, a procedure called LAPB was added. LAPB is Link Access Procedure-Balanced and operates under the HDLC Asynchronous Balanced Mode (ABM). Unfortunately, the 1977 LAPB lacked good symmetry between the DTE and DCE, and was unworkable.

In the April 1979 CCITT meeting, the LAPB was greatly enhanced, especially in the DTE/DCE symmetry. This enhanced version was approved in the February 1980 Plenary meeting of the CCITT. We now have a good, workable LAPB standard. LAPB is a superior procedure and the usage of LAP is being replaced with LAPB.

LAPB COMMANDS AND RESPONSES

			CONTROL FIELD				
FRAME TYPE	**COMMAND**	**RESPONSE**	**BIT #**				
			7 6 5	**4**	**3 2 1**	**0**	
I-FRAME	I-FRAME		N(R)	P	N(S)	0	
S-FRAME	RR	RR	N(R)	P/F	0 0 0	1	RECEIVER READY
	RNR	RNR	N(R)	P/F	0 1 0	1	RECEIVER NOT READY
	REJ	REJ	N(R)	P/F	1 0 0	1	REJECT
U-FRAME	SABM		0 0 1	P	1 1 1	1	SET ASYNCHRONOUS BALANCED MODE
	DISC		0 1 0	P	0 0 1	1	DISCONNECT
		DM	0 0 0	F	1 1 1	1	DISCONNECT MODE
		UA	0 1 1	F	0 0 1	1	UNNUMBERED ACKNOWLEDGE
		FRMR	1 0 0	F	0 1 1	1	FRAME REJECT

Only the FRMR and I-frame contain I-fields
P = Pole Bit F = Final Bit

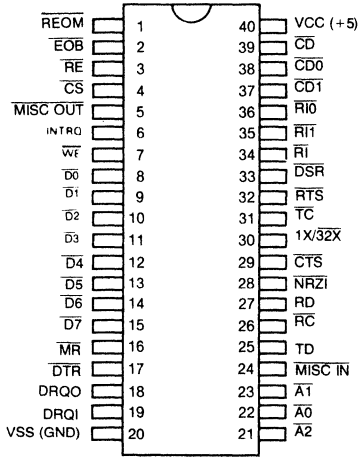
Printed in U.S.A.

FINAL

WD1935
Synchronous Data Line Controller

FEATURES

- HDLC, SDLC, ADCCP AND CCITT X.25 COMPATIBLE
- SDLC LOOP DATA LINK CAPABILITY
- FULL OR HALF DUPLEX OPERATION
- DC TO 2.0 MBITS/SEC DATA RATE
- PROGRAMMABLE/AUTOMATIC FCS (CRC) GENERATION AND CHECKING
- PROGRAMMABLE NRZI ENCODE/DECODE
- FULL SET OF MODEM CONTROL SIGNALS
- DIGITAL PHASE LOCKED LOOP
- FULLY COMPATIBLE WITH MOST CPU'S
- MINIMUM CPU OVERHEAD
- FULLY TTL COMPATIBLE
- SINGLE +5V SUPPLY
- ERROR DETECTION: CRC, UNDERRUN, OVERRUN, ABORTED OR INVALID FRAME ERRORS
- STRAIGHT FORWARD CPU INTERRUPTS
- PROGRAMMABLE MODEM CONTROL INTERRUPTS
- DOUBLE BUFFERING OF DATA
- DMA COMPATABILITY
- END OF BLOCK OPTION
- VARIABLE CHARACTER LENGTH (5, 6, 7 OR 8 BITS)
- RESIDUAL CHARACTER CAPABILITY
- ADDRESS COMPARE
- GLOBAL ADDRESS RECOGNITION
- EXTENDABLE ADDRESS FIELD
- EXTENDABLE CONTROL FIELD
- AUTOMATIC ZERO INSERTION AND DELETION
- MAINTENANCE MODE FOR SELF-TESTING



WD1935
PIN DESIGNATION

APPLICATIONS

COMPUTER COMMUNICATIONS
TERMINAL COMMUNICATIONS
COMPUTER TO MODEM INTERFACING
LINE CONTROLLERS
FRONT END COMMUNICATIONS
NETWORK PROCESSORS
TELECOMMUNICATION SWITCHING NETWORKS
MESSAGE SWITCHING
PACKET SWITCHING
MULTIPLEXING SYSTEMS
DATA CONCENTRATOR SYSTEMS
SDLC LOOP DATA LINK SYSTEMS
DMA APPLICATIONS
COMMUNICATION TEST EQUIPMENT
LOCAL NETWORKS
MULTIDROP LINE SYSTEMS

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	$\overline{REOM}$	Received End of Message	Received End of Message with no Errors.
2	$\overline{EOB}$	End of Block	This input, when low, function as an FCS command. Is independent of $\overline{CS}$.
3	$\overline{RE}$	Read Enable	This input, when low (and $\overline{CS}$ is active), gates the content of addressed register onto the Data bus.
4	$\overline{CS}$	Chip Select	This input, when low, selects the WD1935 for a read or write operation to/from the Data bus.
5	$\overline{MISC\ OUT}$	Misc Output	This output is an extra programmable output signal for the convenience of the user. Is controlled by the CR10 bit.
6	INTRQ	Interrupt Request	This output is high whenever any of the interrupt register bits IR7-IR3 are set. $\overline{TC}$ must be asserted to assert INTRQ.
7	$\overline{WE}$	Write Enable	This input when low (and $\overline{CS}$ is active), gates the content of the Data bus into the addressed register.
8 thru 15	$\overline{D0}$–$\overline{D7}$	Data Bus	Bidirectional three-state Data Bus. Bit 7 is MSB.
16	$\overline{MR}$	Master Reset	This input, when low, initializes all the registers, and forces the WD1935 into an idle state. The WD1935 will remain idle until a command is issued by the CPU.
17	$\overline{DTR}$	Data Terminal Ready	Modem Control Signal. This output, when low, indicates to the Data Communication Equipment (DCE) that the WD1935 is ready to transmit or receive data.
18	DRQO	Data Request Output	This output, when high, indicates that the Transmitter Holding Register (THR) is empty and ready to receive a data character from the Data bus for a transmit operation.
19	DRQI	Data Request Input	This output, when high, indicates that Receiver Holding Register (RHR) contains a newly received data character, available to be read onto the Data bus.
20	V_{SS}	V_{SS}	Ground
21 thru 23	$\overline{A2}$, $\overline{A0}$, $\overline{A1}$	ADDRESS	These inputs are used to address the CPU interface registers for read/write operations.
24	$\overline{MISC\ IN}$	Misc Input	This input is an extra input signal for the convenience of the user. The state is shown by the SR4 bit.
25	TD	Transmitted Data	This output transmits the serial data to the Data Communications Equipment/Channel.
26	$\overline{RC}$	Receive Clock	This input is used to synchronize the received data.
27	RD	Received Data	This input receives the serial data from the Data Communication Equipment/Channel.
28	$\overline{NRZI}$	NRZI	This input, when low, sets the WD1935 in NRZI mode.
29	$\overline{CTS}$	Clear to Send	Modem Control Signal. This input when low, indicates that the DCE is ready to accept data from the WD1935.
30	1X/$\overline{32X}$	DPLL Select	This input controls the internal clock. When high (1X clock), the external clock has the same frequency as the internal clock. When low (32X clock), the external clock is 32 times faster than the internal clock and the DPLL Logic is enabled.
31	$\overline{TC}$	Transmit Clock	This input is used to synchronize the transmitted data, as well as generating either Receive or Transmit INTRQ's.

PIN DESCRIPTION (continued)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
32	$\overline{RTS}$	Request to Send	Modem Control Signal. This output, when low, indicates to the DCE that the WD1935 is ready to transmit data.
33	$\overline{DSR}$	Data Set Ready	Modem Control Signal. This input, when low, indicates that the DCE is ready to receive or transmit data.
34	$\overline{RI}$	Ring Indicator	Modem Control Signal. This input, when low, indicates a ringing signal being received on the communication channel.
35	$\overline{RI1}$, $\overline{RI0}$	Ring Indicator Interrupt Control	These inputs are used to program Ring Indicator interrupts.
36			
37	$\overline{CD1}$, $\overline{CD0}$	Carrier Detect Interrupt Control	These inputs are used to program Carrier Detect Interrupts.
38			
39	$\overline{CD}$	Carrier Detect	Modem Control Signal. This input, when low, indicates there is a carrier signal received by the local DCE from a distant DCE.
40	V_{CC}	V_{CC}	+5VDC

TABLE 1. WD1935 GLOSSARY

TERM	DEFINITION/DESCRIPTION
BOP	Bit-oriented protocols: SDLC, HDLC, and ADCCP
ABORT	11111111 (seven or more contiguous 1's)
GA	Go-ahead pattern. 01111111 (0(LSB) followed by seven 1's)
LSB	First transmitted bit and first received bit. (Least significant bit)
MSB	Last transmitted bit and last received bit. (Most significant bit)
IDLE	11111111 11111111 (15 or more contiguous 1's)
FLAG	01111110. Starts and ends a Frame.
A-FIELD	Address-field in the Frame. Consists of one or more 8-bit characters. Defines the address of a particular station.
C-FIELD	Control field in the Frame. Consists of one or two 8-bit characters.
I-FIELD	Information field in the Frame. Consists of any number of bits.
FCS	Frame Check Sequence. A 16-bit error checking field sequence.
FRAME	A communication element, consisting of a minimum of 32 bits, and delimited by FLAGS.
GLOBAL ADDRESS	An A-field character of eight 1's. When this is compared and matched in the Address comparator, the DRQI will be set, indicating a valid address
RESIDUAL CHARACTER	The last I-field character, consisting of a lesser amount of bits than the other I-field characters in the Frame.
DATA SET	Data Communication Equipment (DCE). May be a modem.
BIT TIME	Length in time of a serial data bit.

The WD1935 is a MOS/LSI microcomputer peripheral device which performs the functioning of interfacing a parallel digital system to a synchronous serial data communication channel employing ISO's HDLC, IBM's SDLC or ANSI's ADCCP line protocol. These protocols are referred to as Bit-Oriented Protocols (BOP).

The chip is fabricated in N-channel depletion load MOS technology and is TTL compatible on all inputs and outputs. This controller requires a minimum of CPU software by supporting a comprehensive frame-level instruction set and by hardware implementation of the low level tasks associated with frame assembly/disassembly and data integrity. It can be programmed to encode/decode NRZI data. The internal clock is then derived from the NRZI data using a digital phase locked loop.

The receiver and transmitter logic operates as two total independent sections with a minimum of common logic. The frames are automatically checked for errors during reception by verifying correct Frame Check Sequence (FCS). In transmit mode, the FCS is automatically generated by this controller and sent before the final Flag. It also continuously checks for other errors. In case of an error, the CPU is interrupted.

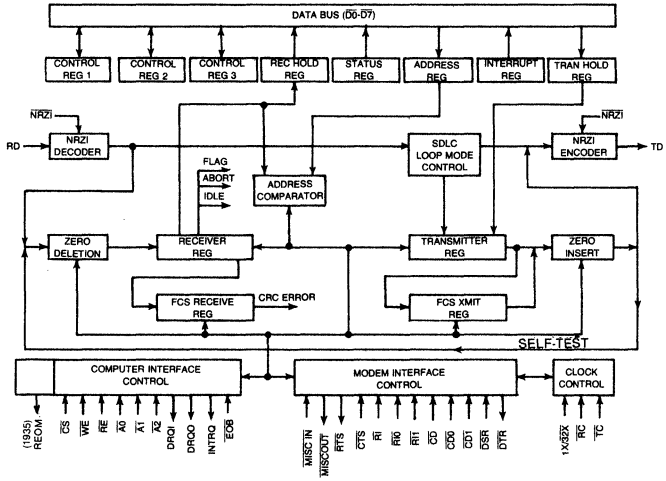


FIGURE 1. WD1935 BLOCK DIAGRAM

The controller recognizes and can generate Flag, Abort, Idle and GA characters. WD1935 can be used in an SDLC Loop configuration. An End of Block option is supplied to minimize CPU time. A full set of modem control signals are supplied to minimize external hardware.

A BRIEF DESCRIPTION OF HDLC, SDLC AND ADCCP PROTOCOLS

The WD1935 is compatible with HDLC, SDLC and ADCCP standard communication Link Protocols. These are bit-oriented, code independent, and ideal for full duplex communication. A single communication element is called a FRAME, which can be used for both link control and data transfer purposes.

The elements of a frame are the beginning eight bit FLAG (F) consisting of one logical "0," six 1's and a 0, an eight bit ADDRESS-FIELD(A), an eight bit CONTROL-FIELD (C), a variable (N bits) INFORMATION-FIELD, a sixteen bit FRAME-CHECK-SEQUENCE (FCS), and an eight bit end FLAG (F), having the same bit-pattern as the beginning flag.

In HDLC, the address (A) and control (C) characters are extendable (more than one character). An important characteristic of a frame is that its contents are made code transparent by use of a zero bit insertion and deletion technique. Thus, the user can adapt any format or code suitable for his system. The frame is bit-oriented, meaning that, bits not characters in each field have specific meanings. The Frame Check Sequence (FCS) is an error detection scheme similar to the Cyclic Redundancy Checkword (CRC) widely used in magnetic disk storage devices. The frame format is shown in Figure 3.

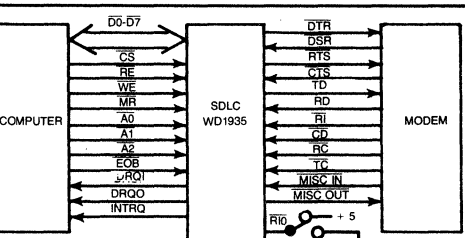


Figure 2. WD193X TYPICAL SYSTEM INTERFACE

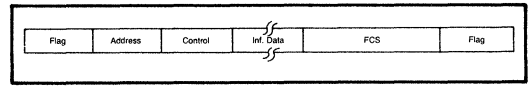


FIGURE 3. WD1935 SDLC/HDLC/ADCCP FRAME FORMAT

Where:

FLAG = 01111110

Address field—One or more 8-bit characters defining the particular station

Control field—One or two 8-bit characters

Information field—Any number of bits (may be zero bits)

Frame Check Sequence—16-bit error checking field

The following features are also part of these protocols.

ZERO INSERTION/ZERO DELETION—Zero insertion/deletion is performed within the 2 Flags of a frame. If there are more than five 1's in a row, a 0 is automatically inserted after the fifth 1 and it is deleted upon reception by the receiver.

FRAME CHECK SEQUENCE (FCS)—A 16 bit cyclic redundancy check (CRC) calculation is performed during transmission of the data in between the 2 flags of the frame. The CRC is then transmitted after the I-field and before the final FLAG. Upon reception the receiver also performs a CRC calculation on the incoming data. If there were no transmission error, the Receiver CRC equals F0B8 (hex).

HARDWARE ORGANIZATION

The WD1935 block diagram is illustrated in Figure 1 and described below.

CPU Interface Registers

All of these registers are addressable and to be read from and/or written into by the CPU via the Data bus. These are 8-bit registers and have to be enabled via Chip Select ($\overline{CS}$) before any data transfer can be done.

CONTROL REGISTER 1, 2, 3 (CR1, 2, 3) Operations are initiated by writing the appropriate commands into these registers. CR1 should be programmed last.

RECEIVER HOLDING REGISTER (RHR) When Data Request Input is set (DRQI=1), contains received assembled character.

ADDRESS REGISTER (AR) Contains the address of the accessed WD1935, which is to be compared to the received address character (A-field).

INTERRUPT REGISTER (IR) Contains the cause of the current interrupt request.

TRANSMITTER HOLDING REGISTER (THR) Is to be loaded with the next in line character to be transmitted, when Data Request Output is set (DRQO=1).

STATUS REGISTER (SR) Contains the overall status of the WD1935 plus some information of the last received frame.

Non-Addressable, Internal Registers

These registers are transparent to the user, but is mentioned in these data sheets to help the understanding of the WD1935.

TRANSMITTER REGISTER (TR) This 8-bit register functions as a buffer between the THR and the TD output. It is loaded from the THR (if Data Command) with the next character to be transmitted. A FLAG character may also be loaded into this register under program control. This character is automatically shifted out to the Transmit Data output. When the last bit of the current transmitted character has left the TR register, a new character will be loaded into this register, setting DRQO (Data command) or INTRQ (Abort, Flag or FSC command). If at the time when only one bit remains left in the TR register, and the THR is not loaded or a new command is not programmed (Data command), an underrun error will occur.

RECEIVER REGISTER (RR) The received data is, via the Zero-Deletion logic shifted into this 8-bit register. The data is here assembled to a 5, 6, 7 or 8-bit character length and then, under the right conditions, parallel transferred to the RHR register.

FCS RECEIVE REGISTER AND FCS XMIT REGISTER The WD1935 contains a 16-bit CRC check register (FCS REC. REG.) and a 16-bit CRC generation register (FCS XMIT REG.). The generating polynomial is:

$$G(X) = X^{16} + X^{12} + X^5 + 1$$

The transmitter and receiver initialize the remainder value to all ones before CRC accumulation starts. The data is multiplied by X^{16} and is divided by G(X). Inserted 0's are not included in the accumulation. Under program control, the complement called the frame check sequence (FCS) is sent with high order bit first.

Various Internal Circuits

ADDRESS COMPARATOR This 8-bit comparator is used to compare the contents of the Address Register with the first address character of the incoming frame. This feature is enabled by a bit in the Command Register. If enabled and there is a match, the received frame is valid and DRQIs are generated for every character received (including the A-field). If enabled and there is not a match or there is no Global Address, the received frame is discarded. If not enabled, all received frames are valid and DRQIs are generated.

ZERO INSERTION The transmitted data stream is continuously monitored by this logic. A zero is automatically inserted following five contiguous 1 bits anywhere between the beginning FLAG and the ending FLAG of a frame. The insertion of the zero bit thus applies to the contents of the Address, Control, Information Data, and the FCS field.

ZERO DELETION The received data stream is continuously monitored by this logic. Upon receiving five contiguous 1 bits, the sixth bit is inspected. If the sixth bit is a 0, it is automatically deleted from the data stream. If the sixth bit is a 1, the seventh bit inspected; if it is a 0, a FLAG is recognized; if it is a 1 an ABORT or GO AHEAD is recognized.

DATA BUS ($\overline{D7}$-$\overline{D0}$) This is an inverted 8-bit bidirectional data bus.

SDLC LOOP-MODE CONTROL This logic supervises the WD1935 running in SDLC Loop mode. It monitors the received data for a GO-AHEAD pattern in the case when SDLC LOOP MODE bit (CR22) and ACT TRAN bit (CR16) are set. When GO-AHEAD pattern is received, this logic suspends the repeater function and initiates the transmitter function. For more details, see functional description of SDLC Loop Mode.

NRZI ENCODER/DECODER When this mode is selected, the NRZI Encoder encodes the "normal" transmitted data to NRZI formatted data and the NRZI Decoder decodes the received NRZI data to "normal" data.

A binary 1 for "normal data" is TD = high.

A binary 1 for NRZI data is TD = no change.

A binary 0 for "normal data" is TD = low.

A binary 0 for NRZI data is TD = change of state.

COMPUTER INTERFACE CONTROL This logic interfaces the CPU, to the WD1935. It supervises the read and write functions to the addressable registers, generates data requests and interrupts, decodes and initiates commands, monitors the status of WD1935, etc.

MODEM INTERFACE CONTROL This logic interfaces and supervises the modem control signals to/from the WD1935. It provides both dedicated (EIA Standard) and user defined control functions.

CLOCK CONTROL This logic interfaces the transmit and receive clocks to the WD1935. It converts the external clocks to the necessary internal clocks.

FUNCTIONAL DESCRIPTION

SDLC Loop Mode

The diagram below shows an SDLC Loop Data Link System. WD1935 can be used in any of these stations.

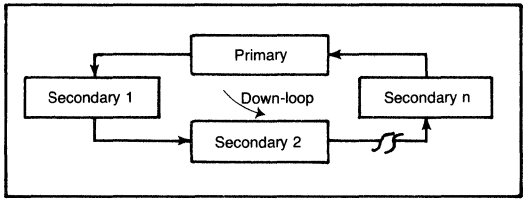


FIGURE 4. WD1935 SDLC LOOP DATA LINK

Each secondary station is normally a repeater in Receive mode (ACT REC bit on). The primary station is the loop controller. Signals sent out on the loop by the primary station are relayed from station to station, then back to the Primary. Any secondary station finding its address in the A-field captures the frame for action at that station. All received frames are relayed to the next station on the loop.

If a secondary station wants to transmit a message, it sets the ACT TRAN bit ($\overline{CTS}$ must be low) and waits for a GO AHEAD (GA) pattern. The ACT REC bit must be asserted for detection of the GA and other existing patterns. Until the GA pattern is received, this secondary station continues operating as a repeater. The primary station has the responsibility to generate the first GA pattern which can be accomplished by a flag followed by continuous 1's. The primary station must continue to send 1's until the GA has circulated through the entire loop. The first secondary station with its ACT TRAN bit set detects the GA and changes the last 1 bit of the GA pattern to a 0, thus generating the start flag of the frame it wants to transmit and preventing the GA pattern from propagating down the loop. The repeater function is then suspended by this secondary station and it goes into the transmit mode. When this secondary station completes its transmission frames, it resets the ACT TRAN bit and reverts back to the repeater mode. It repeats the 1's generated by the primary station to form another GA pattern from the final 0 of its ending flag. The GA pattern propagates through the loop until a secondary station down the loop, that wants to transmit (ACT TRAN bit is set), intercepts the GA pattern and starts to transmit as described, or until the primary station receives the idles (continuous 1's), indicating that the GA pattern has circulated through the entire loop. The primary station then generates another GA pattern or terminates its final data frame with continuous 1's.

Repeaters (Secondary stations) delay the received data by 4 bits (NRZ1 = 5 bits) before transmission.

The $\overline{RC}$ and $\overline{TC}$ clocks must be tied together. The internal DPLL will not function in the loop mode.

1X/32X Clock Option

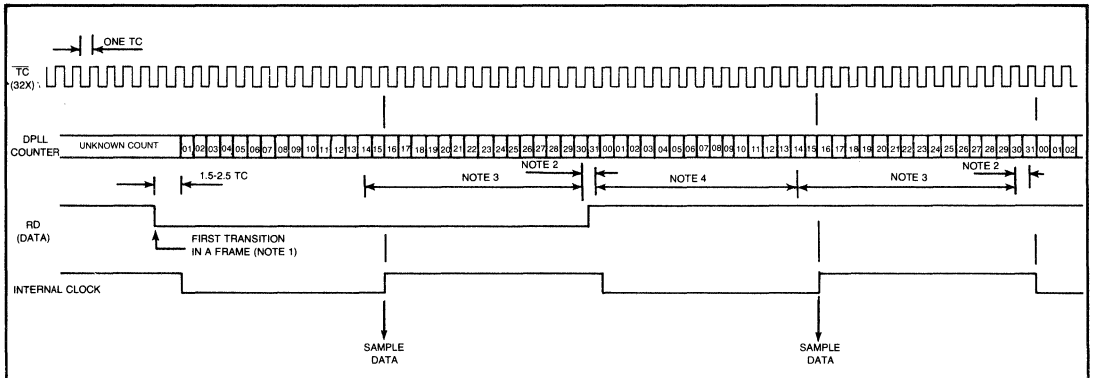
When 1X clock is selected, the data rate equals the external clock (receiver and transmitter).

When 32X clock is selected, the external clock rate is 32 times faster than the data rate.

Digital Phase Locked Loop (DPLL)

This feature is particularly useful in NRZI mode and/or when asynchronous modem is used. The purpose of the DPLL is to synchronize the internal 1X clock to the received data, thus insuring that this data is sampled in the middle of the incoming serial data bit. DPLL is automatically in operation when 32X clock is selected.

The DPLL Logic is initiated at the first received data transition in a frame. Corrections, if needed, are then made for each received data transition. A 32-counter is used for this operation. At the beginning of each frame and at the first received data transition, this 32 counter is reset. From this time on, the counter increments with one count for each external clock pulse. At count 16 the internal 1X clock is forced to change state to high (this transition = sampling time). At count 32, the counter resets itself. This forces the internal 1X clock again to change state back to low.



NOTE 1. FIRST DATA TRANSITION (FIRST FLAG) SETS THE DPLL COUNTER TO 01.

NOTE 2. DATA TRANSITION IN BETWEEN HERE, OR NO DATA TRANSITION AT ALL, CAUSES NO CORRECTION OF THE DPLL COUNTER.

NOTE 3. DATA TRANSITION IN BETWEEN HERE, WILL INCREMENT ONE COUNT TO THE DPLL COUNTER (ADD 01 TO WHAT IS SHOWN).

NOTE 4. DATA TRANSITION IN BETWEEN HERE, WILL DECREMENT ONE COUNT TO THE DPLL COUNTER (SUBTRACT 01 TO WHAT IS SHOWN).

FIGURE 5. WD1935 DPLL TIMING DIAGRAM

At each received data transition, if the internal clock and the received data is out of synchronization, a correction is automatically made by ± 1 external clock period. See DPLL Timing Diagram in Figure 5.

End Of Block (EOB)

This is an FCS command. The main purpose of EOB is to allow the user to initiate FCS and FLAG without the need of using extra computer time. This is particularly practical in DMA applications. At the end of a frame, when the last information data character has already been loaded into the THR and once again DRQO is set, either a regular FCS command is written into CR1 Register, or $\overline{EOB}$ is to be activated. At the end of FCS, when INTRQ is set (XMIT OPCOM), the $\overline{EOB}$ if activated is to be reset again.

Serial Data Synchronization

The serial data is synchronized by the externally supplied Transmit Clock ($\overline{TC}$) and Receive Clock ($\overline{RC}$). When 1X clock is selected, the falling edge of $\overline{TC}$ generates new transmitted data and the rising edge of $\overline{RC}$ is used to sample the received data. When 32X clock is selected, a 32-counter (in the DPLL Logic) is used to synchronize the internal clock. At time 0, when the counter is reset to 0, the new transmitted data is generated. At time 16 (counter = 16) the received data is sampled, insuring that sampling is done in the middle of the received serial data bit. At count 32, the counter is reset to 0 again.

Self Test (Diagnostic) Mode

This feature is a programmable Loop back of data, enabling the user to make a complete test of the WD1935 with a minimum of external circuitry. In this mode, transmitted data to the TD pin, is internally routed to the received data input circuitry, thus allowing a CPU to send a message to itself to verify proper operation of the WD1935. The modem control signals $\overline{DTR}$ and $\overline{RTS}$ are deactivated (off) to insure no interference to/from the Data Communication Equipment (DCE). $\overline{DSR}$ and $\overline{CTS}$ are internally activated for proper input conditions. $\overline{TC}$ and $\overline{RC}$ should be supplied by the same source if 1X clock is selected.

Auto Flag

If this is selected and Data Command is executed, continuous Flags will be sent between frames. This eliminates the need to execute the Flag Command. In DMA applications in particular, this is very practical.

Extended Addressing

This type of addressing means, that there is more than one address character in the A-field. In receive mode, the first address character is compared in the Address Comparator of the WD1935. The other address character/s is to be compared by the CPU. The last address character is recognized by the fact that the LSB (bit 2^0) is a 1.

PROGRAMMING

Controlling Operation

Prior to initiating data transmission or reception, CONTROL REGISTER 1-3 (CR1-3) must be loaded with control information from the CPU. The contents of these registers will configure the WD1935 for the user's specific data communication environment. These registers should be loaded during power-on initialization and after a reset operation. They can be changed at any time that the respective transmitter or receiver is deactivated. The CR1-3 dictate what the transmitter will send: the type of character (DATA, ABORT, FLAG or FCS), the number of bits per character, and the number of bits in the residual character. Similarly, they tell the receiver the types of frames to look for: the number of bits per I-field character, whether to perform an address compare, and whether to watch for an extended address. The Control Register also control Data Terminal Ready ($\overline{DTR}$), $\overline{Misc\ Out}$ and the activation of both the transmitter and the receiver. For more detailed information, see Register Formats.

Monitoring Operation

Monitoring is done by use of the Interrupt Register (IR) and Status Register (SR). The IR register indicates when a frame is completed (transmitted or received), if there was an error and if there is a Data Set Change. It also monitors the states of INTRQ, DRQO and DRQI.

The SR register indicates if an error is recognized by IR, what type of error. It also monitors the modem control signals; Ring Indicator ($\overline{RI}$), Carrier Detect ($\overline{CD}$), Data Set Ready ($\overline{DSR}$) and $\overline{Misc\ In}$.

Furthermore, the SR register monitors if the Receiver is idle, and also if in receive mode if the user has programmed the Receiver Character Length to be 8 bits per character, this register indicates the number of residual bits received. For more detailed information, see Register Formats.

Read/Write Control Of CPU Interface Registers

These registers are directly accessible from the CPU bus ($\overline{D7}$-$\overline{D0}$) by a read and/or write operation by the CPU.

The CPU must set up the WD1935 register address ($\overline{A2}$-$\overline{A0}$), Chip Select ($\overline{CS}$), Write Enable ($\overline{WE}$) or Read Enable ($\overline{RE}$) before each data bus transfer operation.

During a write operation, the falling edge of $\overline{WE}$ will initiate a WD1935 write cycle. The addressed register will then be loaded with the content of the Data Bus ($\overline{D7}$-$\overline{D0}$). During a read operation, the falling edge of $\overline{RE}$ will initiate a WD1935 read cycle. The addressed register will then place its content onto the Data Bus ($\overline{D7}$-$\overline{D0}$). The read/write operation is completed, when $\overline{CS}$ or $\overline{RE}$/$\overline{WE}$ is brought high.

See Read/Write Timing diagram for more detailed information.

For read and write operation, the CR1-3 registers normally need no external clock. After reset of CR1-3, $\overline{TC}$ clock is required. The AR and THR registers need no external clock, and can only be written into. The RHR, IR and SR registers need Transmit Clock ($\overline{TC}$) or Receive Clock ($\overline{RC}$) to set various bits, and are read-only.

All these registers will get initialized by a Master Reset. A read operation of RHR resets the DRQI. A write operation to THR, resets the DRQO. A read operation of IR, resets IR bits 0 and 3-7. A read operation of SR, resets SR bits 0-2. For addressing and external clocks needed, see TABLE 2.

A more detailed description is shown in Figure 6 of each bit location. It should be known, that because the Data Bus Lines ($\overline{D7}$-$\overline{D0}$) have inverted logic, a logic 1, asserted means low state. Also, a modem control signal which is inverted (example $\overline{DTR}$), is in on-state (asserted) when low.

TABLE 2. DEVICE ADDRESS CODES

$\overline{CS}$	$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	Read	Write	External Clock
L	H	H	H	CR1	CR1	None*
L	H	H	L	CR2	CR2	None*
L	H	L	H	CR3	CR3	None*
L	H	L	L	RHR	AR	RHR=$\overline{RC}$. AR=None
L	L	H	H	IR	THR	IR=$\overline{TC}$. THR=None
L	L	H	L	SR	—	SR0-3=$\overline{RC}$. SR4-7=None.
H	X	X	X	X	X	

L = V_{IL} at pins
H = V_{IH} at pins
X = Don't care

*2.5 $\overline{TC}$ clock cycles are required after a Master Reset to be able to read and write.

REGISTER FORMATS

Below shows a short form register format.

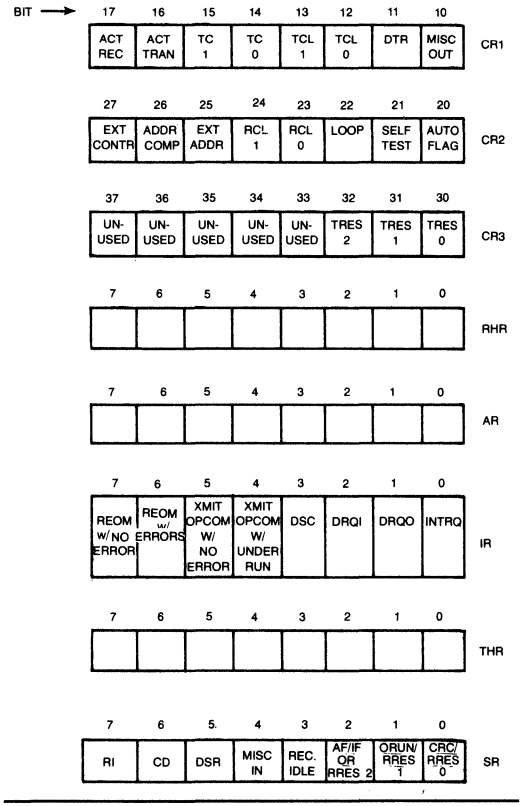


FIGURE 6. WD1935 BIT ASSIGNMENTS

Control Register 1 (CR1)

When initiating a transmit/receive operation, this should be the last register programmed.

Miscellaneous Output (CR10) This bit controls the Miscellaneous Output signal to the data set. When CR10 is a logical 0, $\overline{\text{Misc Out}}$ is off, when it is a logical 1, $\overline{\text{Misc Out}}$ is on.

DTR Command (CR11) This bit controls the data Terminal Ready ($\overline{DTR}$) signal to the data set. When CR11 is a logical 0, $\overline{DTR}$ is off. When CR11 is a logical 1, $\overline{DTR}$ is on. When the Self-Test mode is selected, $\overline{DTR}$ signal is forced to an off state.

Transmitter Character Length (CR13, 12) These bits control the transmitted I-field data character length. The data character may be 5, 6, 7 or 8 bits long.

TABLE 3. TRANSMITTER CHARACTER LENGTH

CR13 (TCL1)	CR12 (TCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Transmitter Commands (CR15, 14) These bits control the transmission of DATA (A-field, C-field and I-field), ABORT, FLAG, and FCS (FCS plus FLAG). When these commands are programmed, the previous command currently still in progress, will complete the transmission of its character. When this is done, a new character generated by this new command, will be transmitted.

CR 14, 15 can be programmed as follows:

A. If DATA is programmed, the new character to be transmitted will be the character loaded (or still to be loaded) in the THR REGISTER.
B. If ABORT is programmed, the new character will be eight logical 1's.
C. If FLAG is programmed, the new character will be 01111110.
D. If FCS is programmed, the new character which will be transmitted consists of the residual byte (which was automatically transferred to the XMIT REGISTER, provided that CR30-32 and are set correctly), followed by the 16-bit content of the FCS XMIT REGISTER and the FLAG.

One serial bit ahead of this new character (for FCS command the FLAG character), the CPU is signalled by DRQO or INTRQ that the WD1935 is again ready to receive a new command. DRQO is asserted by a DATA command and INTRQ (XMIT OPCOM) is asserted by an ABORT, FLAG or FCS command.

TABLE 4. TRANSMITTER COMMANDS

CR15 (TC1)	CR14 (TC0)	Command	Character/s Transmitted	Signal to CPU
0	0	DATA	Content of THR	DRQO
0	1	ABORT	1111 1111	INTRQ
1	0	FLAG	0111 1110	INTRQ
1	1	FCS	FCS + 01111110	INTRQ

In the case of the DATA command the user has two choices; 1. Change the command. 2. Keep the DATA command and load a new character into the THR register. For more information, please see the Transmission Timing diagram, Figure 7. See Table 4 for programming information.

Activate Transmitter (CR 16) This bit when set, enables the transmitter and sets $\overline{RTS}$ signal. If in SDLC Loop Mode (CR22 = set), the transmitter waits for a Go-Ahead pattern before the transmitter is enabled.

Activate Receiver (CR 17) This bit when set activates the receiver, which begins shifting in frames one character at a time into RR register for inspection.

CONTROL REGISTER 2 (CR2)

Auto Flag (CR20) When set, Flags (without INTRQs) will be continuously transmitted in between frames, when otherwise the transmitter would be in idle state.

Self-Test Mode (CR21) When set, the Transmitter Data Output is internally connected to the Receiver Data input circuitry. The modem control output signals are deactivated (off state). The modem control input signals are internally activated. This mode allows off-line diagnostic.

SDLC Loop Mode (CR22) When set, the WD1935 is conditioned to operate in an SDLC Loop Data Link system (see SDLC Loop Mode).

Receiver Character Length (CR24, 23) These bits indicate to the receiver how many bits per character there are to assemble for the I-field. The I-field characters may be 5, 6, 7 or 8 bits long. The unused bits read from RHR will be logical 0.

TABLE 5. RECEIVER CHARACTER LENGTH

CR24 (RCL1)	CR23 (RCL0)	Bits Per Character
0	0	8
0	1	7
1	0	6
1	1	5

Extended Address (CR25) When set, this bit indicates to the receiver that there is more than one address character in the A-field. The receiver will expect another address character if the LSB in the current address character is a logical 0. The purpose of this bit: If a non-8-bit field character length is expected, the DRQIs will get out of synchronization if the WD1935 does not know exactly when the I-field will start. Not used in transmit mode.

Address Compare (CR26) When set, the first address character will be inspected in the Address Comparator. If there is a match with the AR register, or if the address compared is a Global Address (eight 1's) the frame is considered valid, causing DRQIs to be generated. Otherwise, the receiver does not react, and will continue comparing for a new valid address. If not set, all frames are considered valid.

Extended Control (CR27) When set, indicates that there are two control characters per name. If not set, there is only one control character per frame. The purpose of this bit: If a non-8-bit I-field character length is to be received, the DRQIs will get out of synchronization if the WD1935 does not know when the I-field will start. Not used in transmit mode.

CONTROL REGISTER (CR3)

Transmit Residual Character Length (CR32, 31, 30) (Table 6) These bits inform the transmitter what bit-length the residual character will be. If no residual character is to be sent, these bits must be set to logical 0. (See Transmitter Commands).

Unused (CR33-37) These bits are not used, and are always a logical 0.

INTERRUPT REGISTER (IR)

This register contains the information why an interrupt INTRQ was generated. An IR register read operation, will reset bits 0, and 3-7. The Transmitter clock must be active to generate an interrupt.

Loading the THR register, will reset DRQO (bit 1). Reading the RHR register, will reset DRQI (bit 2). A new interrupt will occur if one is pending.

TABLE 6. TRANSMITTER RESIDUAL COMMANDS

CR32 (TRES 2)	CR31 (TRES 1)	CR30 (TRES 0)	Residual Char. Length
0	0	0	No residual char. sent
0	0	1	1 bit
0	1	0	2 bits
0	1	1	3 bits
1	0	0	4 bits
1	0	1	5 bits
1	1	0	6 bits
1	1	1	7 bits

TABLE 7. DATA SET CHANGE PROGRAMMING

$\overline{CD1}$	$\overline{CD0}$	Interrupting edge of $\overline{CD}$	$\overline{RI1}$	$\overline{RI0}$	Interrupting edge of $\overline{RI}$
LO	LO	Rising and falling	LO	LO	Rising and falling
LO	HI	Falling	LO	HI	Falling
HI	LO	Rising	HI	LO	Rising
HI	HI	None	HI	HI	None

If a new interrupt is generated while the CPU is reading the IR register, this new interrupt will set the respective bit in the IR register one bit time later (this to avoid losing any interrupt). The status of bits 3–7 will accumulate until the IR register is read by CPU.

INTRQ (IR0) When set, indicates an interrupt and that there are one or more bits set in positions 3 through 7 of this register. This bit is a mirror image of INTRQ signal (pin 6).

When pin 6 (INTRQ) is not used for pending interrupts information and only the IR register is read to obtain the status of the interrupt bits (polling method), a minimum of two (2) bits times must be allowed between IR registers "read's" to insure an orderly flow of pending interrupts.

DRQO (IR1) When set, indicates a Data request output. This bit is a mirror image of DRQO signal (pin 18).

DRQI (IR2) When set, indicates a Data Request input. This bit is a mirror image of DRQI signal (pin 19).

Data Set Change (IR3) When set, indicates a change of state of the Data Set (Data Communication Equipment). This is a change of state of $\overline{DSR}$, $\overline{CD}$ or $\overline{RI}$. The type of change of $\overline{CD}$ and $\overline{RI}$ that this bit will react to, is programmed by use of input signals $\overline{CD1}/\overline{CD0}$ and $\overline{RI1}/\overline{RI0}$ (Table 7).

XMIT Operation Complete with Underrun Error (IR4) When set, indicates that the transmitter command has been completed and there was an Underrun error. An Underrun error occurs when the Data Request Output (DRQO) is set, but THR register is not loaded in time.

XMIT Operation with No Error (IR5) When set, indicates that the transmitter command has been completed and there was no error.

Received End of Message With Errors (IR6) When set, indicates that a Received End of Message is detected, and there was an error. Errors include CRC, Overrun, Invalid Frame and Aborted Frame.

The SR Register bits 0–2 will indicate the exact type of error.

Received End Of Message With No Error (IR7) When set, indicates that a Received End of Message is detected, and there was no error.

STATUS REGISTER (SR)

This register contains the status of the receiver and some modem control signals. It also indicates (if REOM w/Errors) exactly what type of errors. If the Receiver Character Length is 8 bits, this register indicates the amount of Residual bits that was received. A read operation will reset bits 0–2.

Received Error/Received Residual Character Length (SR 2-0) If REOM w/NO ERROR (IR7) is set, these bits (SR 2-0), indicate the number of residual bits received (Table 8).

If REOM WITH ERROR (IR 6) is set, these bits indicate the type of error that occurred (Table 9).

TABLE 8.

CHAR. LENGTH	RES. BITS	SR 0	SR 1	SR 2
8 Bits/Char.	0	0	0	0
	1	0	0	1
	2	0	1	0
	3	0	1	1
	4	1	0	0
	5	1	0	1
	6	1	1	0
	7	1	1	1
7 Bits/Char.	0	0	1	0
	1	0	1	1
	2	1	0	0
	3	1	0	1
	4	1	1	0
	5	1	1	1
	6	0	0	1
6 Bits/Char.	0	1	0	0
	1	1	0	1
	2	1	1	0
	3	0	0	1
	4	0	1	0
	5	0	1	1
5 Bits/Char.	0	0	0	1
	1	0	1	0
	2	0	1	1
	3	1	0	0
	4	1	0	1

TABLE 9.

Bit Set	Error
SR0	CRC
SR1	Overrun
SR2	Aborted or Invalid frame

Receiver Idle (SR 3) When set, indicates that the receiver is currently IDLE.

Miscellaneous Input (SR4) This is a mirror image of $\overline{MISC}$ IN signal. When this signal is set, SR4 bit is set.

Data Set Ready (SR5) This is mirror image of $\overline{DSR}$ signal. When this signal is set, SR5 bit is set.

Carrier Detect (SR6) This is a mirror image of $\overline{CD}$ signal. When this signal is set, SR6 bit is set.

Ring Indicator (SR7) This is a mirror image of $\overline{RI}$ signal. When this signal is set, SR7 bit is set.

TRANSMITTER OPERATION

Prior to this operation, the programmable inputs and the transmit mode related register bits need to be programmed according to the user's specific data communications environment. The last bit to be set is always the ACT TRAN (CR16) bit.

Before this, the INTRQ has to be cleared, which can be done by reading the IR register. For more detailed information how to program the WD1935 see Programming.

As an example of how to program the WD1935 let's assume a 24-bit information is to be transmitted. The I-field would then consist of three 8-bit characters with no residual bits. CR3 should then be 00 (Hex).

Bits CR23-CR27 are for reception only (see Receiver Operation). The last register to be programmed is CR1. If MISC OUT is not used, this may be ignored. If a modem is used, DTR (CR11) is to be set. CR13 and CR12 should be logical 0's (8-bit char. length). CR15 and CR14 should be logical 0's (Data Command). ACT TRAN (CR16) bit is to be set. The ACT REC (CR17) is for reception only.

The DTR bit, when set, activates the $\overline{DTR}$ signal, indicating to the modem to prepare for communication. When the modem is ready, it sends back a Data Set Ready ($\overline{DSR}$) to the WD1935. This causes the DSC (IR3) bit to set, which in turn activates INTRQ. The IR register is now read. Simultaneously, when the ACT TRAN (CR16) bit is set, this activates the Request to Send ($\overline{RTS}$) signal, instructing the modem to enter into transmit mode. When the modem is ready to transmit data, it responds by activating the Clear to Send (CTS) signal.

The WD1935 is now conditioned to transmit. Now DRQO gets, set, indicating to the CPU (or DMA) to load the first character (Address) into the THR. When this is done, DRQO will reset. As soon as the WD1935 is ready to be loaded with the next character to be transmitted, DRQO is again set. When the THR register is again loaded with a character, DRQO will again reset.

This same sequence continues until the last I-field character to be transmitted is loaded into the THR. If CRC checking is to be used, the next time when DRQO is set, an FCS command has to be programmed. This is accomplished by either setting CR15, 14 to both logical 1's or by activating the $\overline{EOB}$ signal.

At the end of the FCS being transmitted, INTRQ will set indicating XMIT Operation Complete. The IR register is to be read to find out whether the frame was sent with or without error. Also the FCS Command which was used as described above has to be changed. If CR15, 14 were set, these have to be reset (to Data Command), or if $\overline{EOB}$ was activated, this signal has to be deactivated. At this same time, the ACT TRAN bit is allowed to be reset, causing the TD output to go idle after the end Flag is sent. If the ACT TRAN bit is kept set, continuous Flags will be sent following the FCS.

If a new frame is to be sent right after this first frame, only one Flag is needed in between frames, meaning the frames have one common Flag character. In this case, the second frame Address character may be loaded at the same time the FCS command is programmed during the first frame. Also, the ACT TRAN bit should be kept set in between frames. Every time DRQO gets set, the user must load the THR register before the last loaded character only has 1.5 bits left to be transmitted. In other words, when DRQO gets set, the user may wait (if 8-bit characters) up to 7.5 serial data bits before loading the THR. If THR is not loaded within this time, an Underrun error will occur.

If Auto Flag is not selected (CR20 = logical 0) the sequence will be a little different than described below. When the first DRQO is set, and after the Address character is loaded into THR, a Flag command is also programmed (CR15, 14 = 10).

This will set an interrupt (INTRQ), which indicates that the IR register must be read. Now, the Data Command is reprogrammed (CR15, 14 =00).

For more information, see Transmission Timing diagram.

ABORT CONDITIONS

The function of prematurely terminating a data link is called an "Abort." The transmitting station aborts by sending eight consecutive 1's. Unintentional Abort caused by 1's in the A-C- or I-field is prevented by zero insertion. Intentional Abort may be sent by programming an Abort command. Abort will also be sent in the case where THR is not loaded in time or FCS command is not programmed in time (= underrun). This means that after the DRQO is set, to avoid Abort; THR must be loaded, $\overline{EOB}$ activated or FCS command programmed before there is only 1.5 bits left of the last character to be transmitted.

If this is not done, INTRQ (XMIT OPCOM w/underrun) is set and Aborts are transmitted until, either the command is changed or the THR is loaded. If in this same case, Auto Flag was programmed, one Abort (with INTRQ) would be generated, and thereafter continuous Flags (with no INTRQs) will be sent.

RECEIVER OPERATION

Prior to this operation, the programmable inputs and the receive mode related register bits have to be programmed according to the user's specific data communication environment. Also, the INTRQ has to be cleared. The last bit to be set is always the ACT REC (CR17) bit.

For more detailed information how to program the WD1935 see Programming. As an example, let's assume a 26-bit information is to be received, and the I-field is made up by 8-bit characters. The CR3 register is only for transmit mode, and may be ignored here. CR20 and CR 12-16 bits are also for transmit mode only, and therefore may also be ignored. CR21 and CR22 are to be logical 0s (no Self-Test and no SDLC Loop Mode). CR24, 23 are to be logical 0's (8-bit character I-field). If only one A-field and one C-field character is expected, and this WD1935 has a specific address, CR25 should be a logical 0, CR26 should be a 1, and CR27 should be a 0. The address to which the A-field should compare should be loaded into the AR register.

The status of the modem is monitored by the SR register, and it may be useful to read it at this time. CR1 is loaded as the last register. CR10 (Misc In) bit is optionable to the user. CR11 (DTR) is to be set if modem is used. CR17 (ACT REC) is now set, starting the input of frame characters into the Receiver Register (RR). When a Flag is detected, the next

8-bit character (address-character), when received, is compared to the character in the AR register. If these match, or if the received character is a Global address, this frame is valid, and the DRQI gets set. If the Address Comparator (CR26) bit is not set, all frames would be considered valid and generate DRQIs. When the RHR register is read, DRQI will be reset. All characters in a valid frame which are input into the RR register will set DRQI, and every time RHR is read by the CPU, DRQI will be reset.

During reception, the receiver also performs a CRC calculation on the incoming data. When the end Flag is received, INTRQ will get set, indicating Received End of Message. If the reception is completed with no error, IR7 (REOM w/no Error) bit will be set. When 8-bit characters are received SR 0-2 bits indicate the number of residual bits, in this case two. If IR6 (REOM w/Error) was set, SR 0-2 bits indicate the type of errors (see Receiver Error Indication).

When all characters including the A-field and the FCS-field are read, and when the REOM interrupt is recognized, it is up to the user to disassemble these mentioned characters from the received data. If non-8-bit characters are received, the amount of residual bits have to be calculated by the CPU after masking out the part of the ending Flag showing up in the last read character.

After end of frame, the receiver begins searching for a new frame.

(For more information, see Figure 8.)

RECEIVER ERROR INDICATION

When a frame is received, and REOM w/Error (IR6) is set, the type of error is indicated by the SR bits 0-2.

CRC Error (SR0) If the CRC calculation performed on the incoming data does not equal to F0B8 (HEX), this bit will be set.

Overrun Error (SR1) After DRQI is set, if the RHR is not read within one character minus one bit time, this bit will be set.

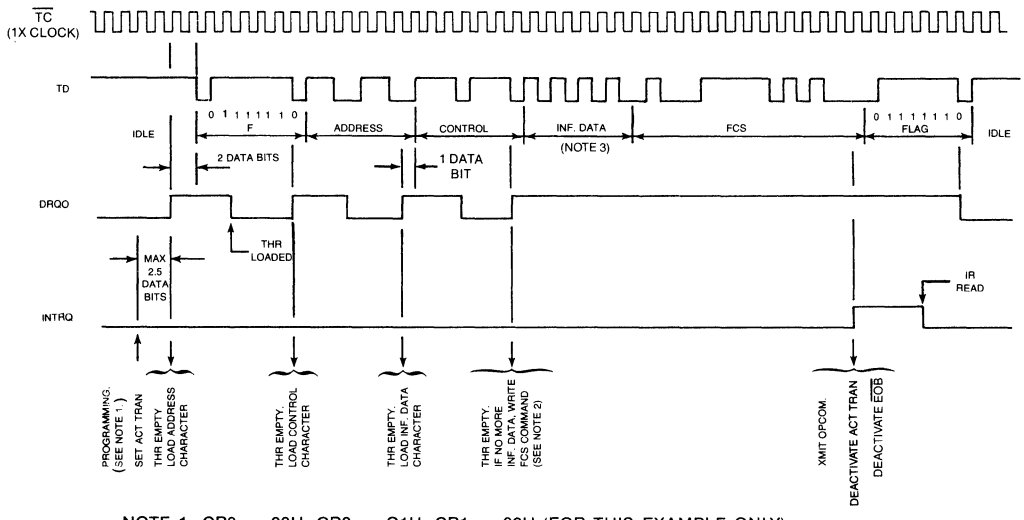
Aborted or Invalid Frame Error (SR2) If the frame is aborted or if in a frame the number of bits between flags are less than the required minimum (see Table 10), this bit will be set.

NOTES

1. TC-command—If two or more contiguous ABORTS or FLAGS are executed, the ACT TRAN (CR16) bit has to be reset before DATA-command can be executed.
2. Master Reset ($\overline{MR}$)—Needs no clock during activation of MR. However, 2.5 clock cycles are required to reset the WD1935 after the falling edge of $\overline{MR}$.
3. IR-register—Immediately when IR register is read, bit 0 will reset. Bits 3-7 are reset one bit time later.
4. SR-register—Bits 0-2 are reset one bit time after SR register is read.
5. SDLC Loop mode—Go-ahead pattern may be sent by either sending IDLE or ABORT after Flag.
6. $\overline{TC}$ and $\overline{RC}$ clocks are completely independent of each other.
7. It is recommended to verify that the INTRQ signal (pin 6) is set prior to reading the IR register.
8. End Of Block (EOB) — Minimum activated time must be one (1) character time. It can be activated indefinitely using IDDLE or AUTO FLAG (CR20).

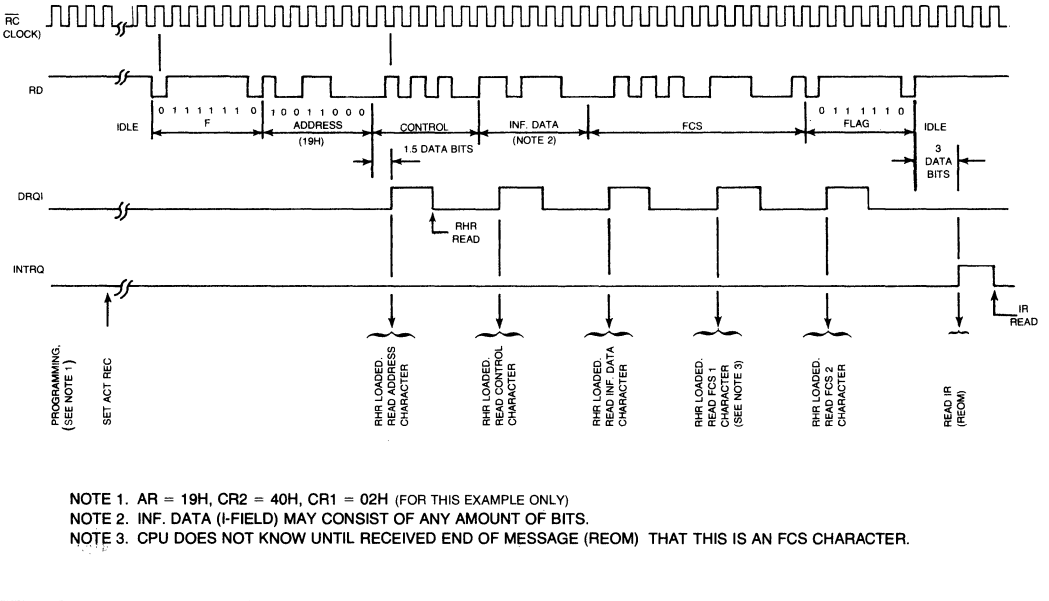
TABLE 10.

	Valid Frame For WD1935			
Receiver Programmed for	**8 bit char**	**7 bit char**	**6 bit char**	**5 bit char**
1 address, 1 control	≥25 bits	≥23 bits	≥21 bits	≥19 bits
2 addresses, 1 control 1 address, 2 controls	≥25 bits	≥24 bits	≥23 bits	≥22 bits
3 addresses, 1 control 2 addresses, 2 controls	≥25 bits	≥25 bits	≥25 bits	≥25 bits



NOTE 1. CR3 = 00H, CR2 = O1H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. WRITE FCS COMMAND, OR ACTIVATE EOB.
NOTE 3. INF. DATA MAY CONSIST OF ANY NUMBER OF BITS.

FIGURE 7. WD1935 TRANSMISSION TIMING DIAGRAM



NOTE 1. AR = 19H, CR2 = 40H, CR1 = 02H (FOR THIS EXAMPLE ONLY)
NOTE 2. INF. DATA (I-FIELD) MAY CONSIST OF ANY AMOUNT OF BITS.
NOTE 3. CPU DOES NOT KNOW UNTIL RECEIVED END OF MESSAGE (REOM) THAT THIS IS AN FCS CHARACTER.

FIGURE 8. WD1935 RECEPTION TIMING DIAGRAM

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Storage Temperature	−55°C to +125°C (plastic package)
Storage Temperature	−65°C to +150°C (ceramic package)
Voltage on any pin with respect to GND (V_{SS})	−0.3 to +7.0V
Power Dissipation	1W

DC Characteristics

T_A = 0°C to +70° V_{SS} = 0V, V_{CC} = +5 ± 0.25V

TABLE 11. WD1935 DC CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
I_{LI}	Input Leakage			10	μA	VIN = V_{CC}
I_{LO}	Output Leakage			10	μA	V_{OUT} = V_{CC} or V_{SS}
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage			0.8	V	All Inputs
V_{OH}	Output High Voltage	2.4			V	I_O = −100μA
V_{OL}	Output Low Voltage			0.4	V	I_O = 1.6mA
I_{CC}	Supply Current		70	210	ma	

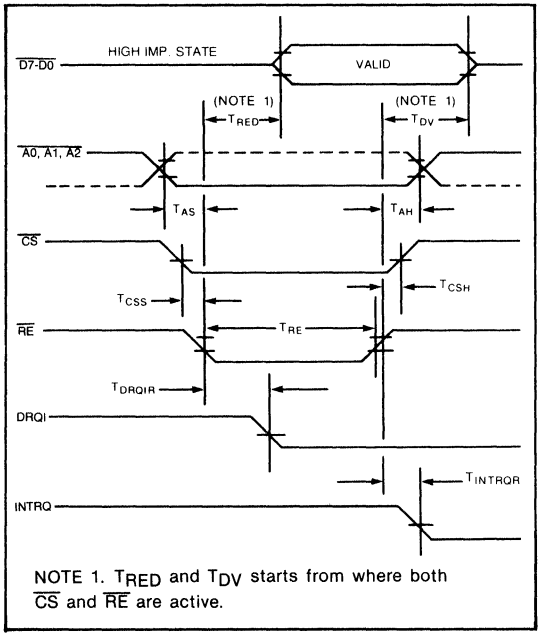
AC Characteristics

T_A = 0°C to +70° V_{SS} = 0V, V_{CC} = +5 ± 0.25V

TABLE 12. WD1935 AC CHARACTERISTICS

		−10		−11		−12		−13			
Symbol	Parameter	Min	Max	Min	Max	Min	Max	Min	Max	Units	Conditions
	READ & WRITE (Fig. 9, 10)										
T_{AS}	Address Set-Up	20		20		20		20		ns	
T_{AH}	Address Hold	20		20		20		20		ns	
T_{CSS}	Chip Select Set-up	20		20		20		20		ns	
T_{CSH}	Chip Select Hold	20		20		20		20		ns	
	READ (Fig. 9)										
T_{RED}	Data Delay from $\overline{RE}$ Asserted		315		290		265		240	ns	
T_{DV}	Date Valid from $\overline{RE}$ Deasserted	0	140	0	140	0	140	0	140	ns	
T_{DRQIR}	DRQI Reset Delay		280		280		280		280	ns	
T_{INTRQR}	INTRQ Reset Delay		280		280		280		280	ns	
T_{RE}	$\overline{RE}$ Pulse width	325		300		275		250		ns	
	WRITE (Fig. 10)										
T_{DS}	Data Set-up	200		180		160		140		ns	
T_{DH}	Data Hold	20		20		20		20		ns	
T_{DRQOR}	DRQO Reset Delay		330		330		330		330	ns	
T_{WE}	$\overline{WE}$ Pulse width	200		180		160		140			
	TRANSMIT& RECEIVE (Fig.11)										
T_{RDS}	Receive Data Set Up	150		150		150		150		ns	
T_{RDH}	Receive Data Hold	150		150		150		150		ns	
T_{TDO}	Transmit Data Out Delay		125		125		125		125	ns	
	CLOCK										
$1xF_C$	1X Clock		.5		1.0		1.5		2.0	MH_Z	at 50% duty cycle
$32xF_C$	32X Clock		1.0		1.5		2.0		2.5	MH_Z	at 50% duty cycle
	RISE & FALL (Fig. 12)										
T_R	Rise Time		20		20		20		20	ns	See figure 1
T_F	Fall Time		20		20		20		20	ns	

NOTE: All A.C. Timing Measurements made at 0.8V and 2.0V.



NOTE 1. T_{RED} and T_{DV} starts from where both $\overline{CS}$ and $\overline{RE}$ are active.

FIGURE 9. WD1935 READ TIMING DIAGRAM

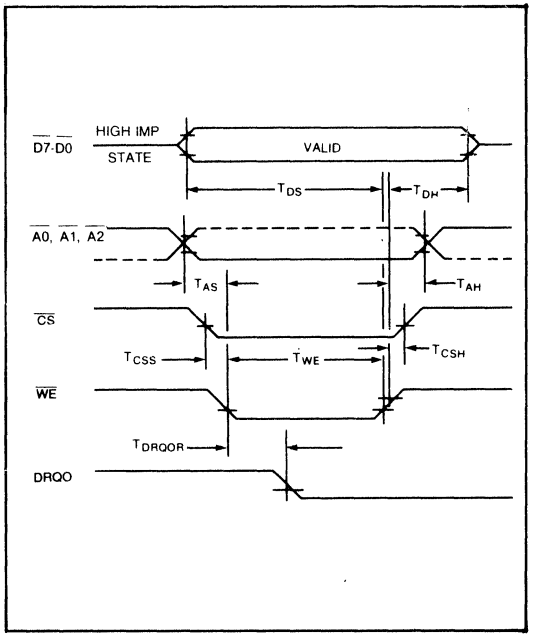


FIGURE 10. WD1935 WRITE TIMING DIAGRAM

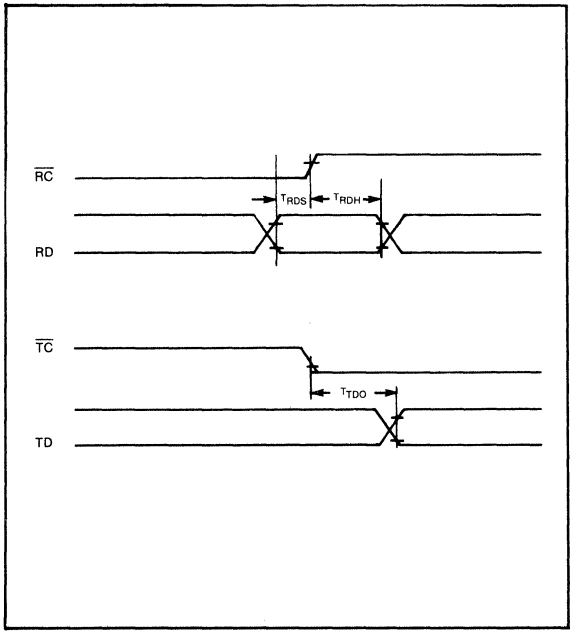


FIGURE 11. RECEIVER AND TRANSMITTER TIMING

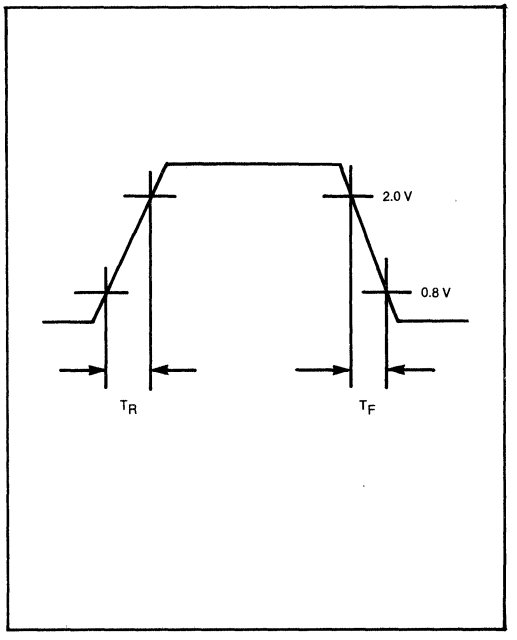


FIGURE 12. WD1935 RISE AND FALL TIMING DIAGRAM

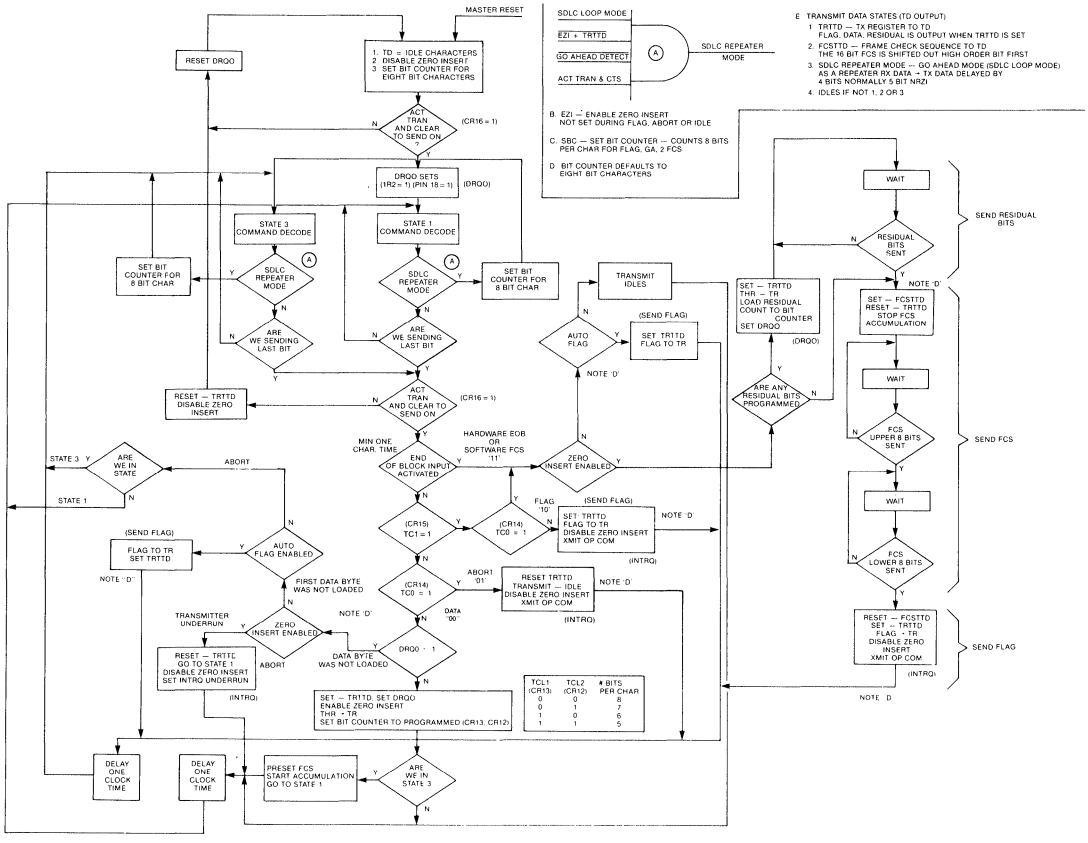


FIGURE 13. WD1935 TRANSMITTER FLOW CHART

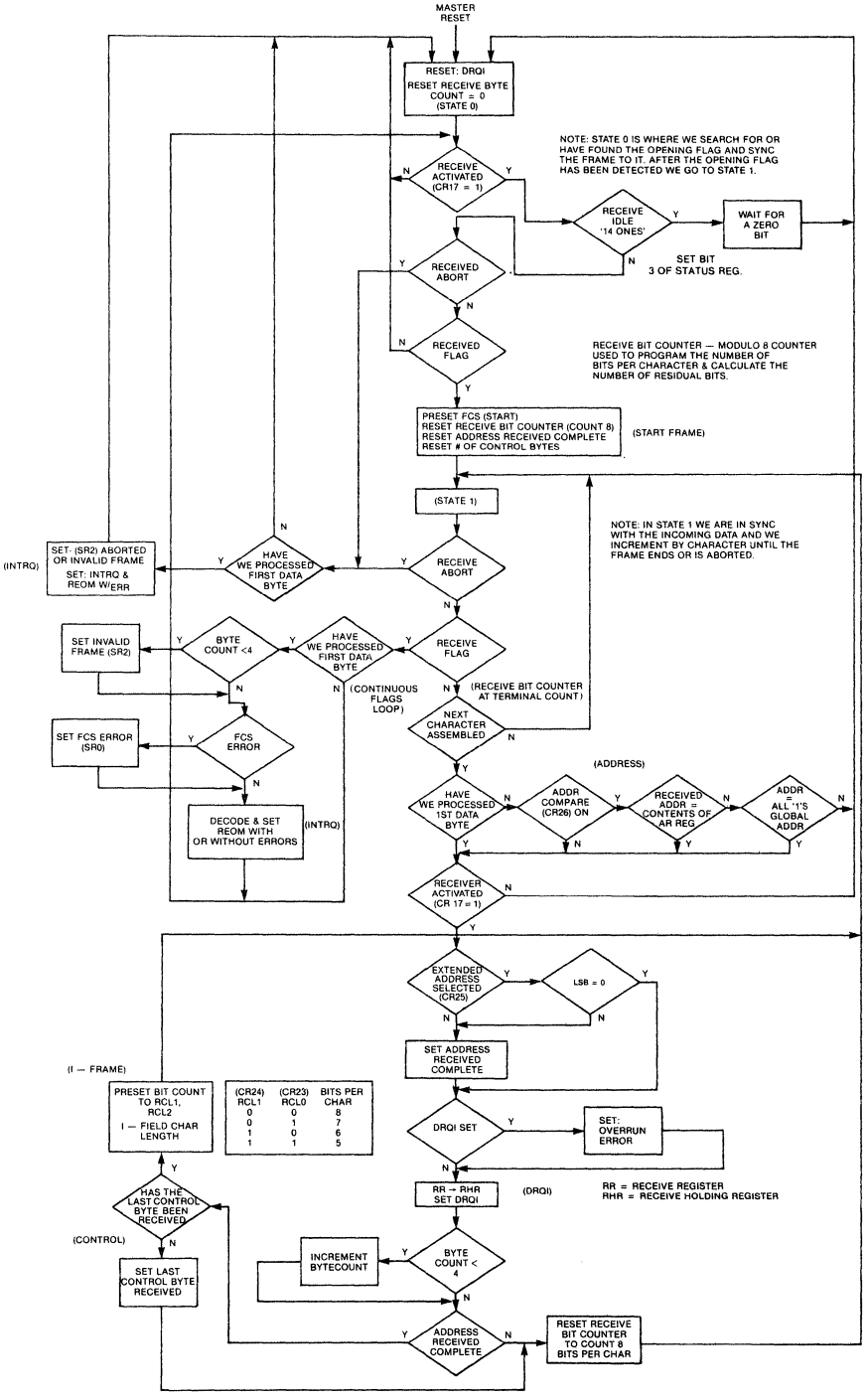


FIGURE 14. WD1935 RECEIVER FLOW CHART

TABLE 13. WD1935 ORDERING INFORMATION

Part Number	Maximum Data Rate	Temperature Range
WD1935*-10	500KBPS	0°C to +70°C
WD1935*-11	1.0MBPS	0°C to +70°C
WD1935*-12	1.5MBPS	0°C to +70°C
WD1935*-13	2.0MBPS	0°C to +70°C

*Please contact your local Western Digital Sales Representative for package availability and price information.

See page 383 for ordering information.

Printed in U.S.A

APPLICATION NOTE

WD1935 Application Note

INTRODUCTION

The purpose of this document is to provide the reader with information about the WD1935. Various applications examples are given showing flowcharts and timing diagrams. As the device is designed for use in a very large range of applications, many different features are described and illustrated for the benefit of the reader.

For detailed product information such as A.C. and D.C. parameters, please refer to the data sheet.

GENERAL DESCRIPTION

The WD1935 is an MOS/LSI device which interfaces a parallel digital system to a serial data communication channel (and vice versa). This circuit is capable of simplex, half duplex, and full duplex operation.

The WD1935 is designed for bit-oriented SDLC, HDLC and ADCCP protocols. The device is programmable and compatible with most 8-bit microcomputers on the market. The purpose of the device is to convert parallel data from a computer or terminal to a serial data stream at one end of a communication channel. At the other end of the channel. At the other end of the channel, the data is converted back to the original parallel data.

Serial data communications minimizes the number of physical channels required to transfer data and therefore reduces the cost to send data between two (or more) distant points. A microcomputer can perform the same serial/parallel conversion function as this device, but at a much slower speed. However, using the WD1935 to do this function is much more efficient. This makes the computer free to perform other tasks during transmission and reception. The only work that the computer is required to do is to initialize and write data characters to/from the WD1935. This device takes care of the serialization or deserialization of this data, plus control and timing.

Some control signals on the computer side of the device are needed for read, write, and control purposes. Additional signals can also be used for special purposes or modes for the convenience of the user. Typically, these other control signals are used to enable communication with a modem or DCE (Data Communications Equipment).

Interrupt outputs are provided to inform the microcomputer when to retrieve from, or to provide data to the holding registers. Interrupts can be generated to provide status information (i.e. changes in modem control lines, or events such as Transmission Complete or Received End of Message have occurred).

SYSTEM APPLICATIONS

Switched network
Multipoint network
Non-switched point to point network
Simplex, half-duplex, or full duplex
Synchronous Communication
Message switching
Multiplexing systems
Data concentrator systems
Loop data link systems
DMA applications
Parallel to serial data conversion (and vice versa)
Local Networks
Packet Switching
X.25
Multidrop line systems

A typical block diagram of a data link is shown in Figure 1.

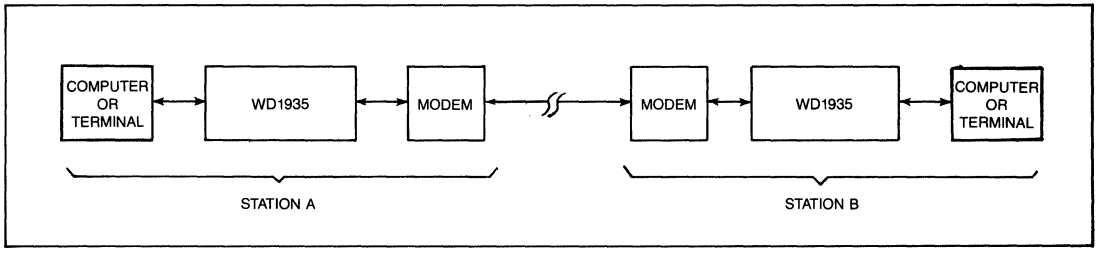


FIGURE 1. DATA LINK BLOCK DIAGRAM

The communication media used could be a direct communication channel (such as a leased telephone line), a switched telephone line, or one of many other possibilities. Typically these applications would require the use of a modem.

A modem is needed for long distance communication lines. For shorter distance, line drivers/receivers may be sufficient. In some very well controlled environments, such as a laboratory, two devices may be connected without line drivers and receivers.

The WD1935 may be connected directly to a microcomputer bus, but buffers are normally recommended. Figure 2 shows a typical schematic of an interface between a Z80 microcomputer and a modem.

Some example of various WD1935 systems are shown here by use of block diagrams. The station shown in Figure 3 consists of a computer or terminal, and a modem. A station may consist of only the computer or terminal, and one WD1935 device. Whether the modem, line drivers and receivers, or CPU buffers are needed depends on the details of the particular design situation.

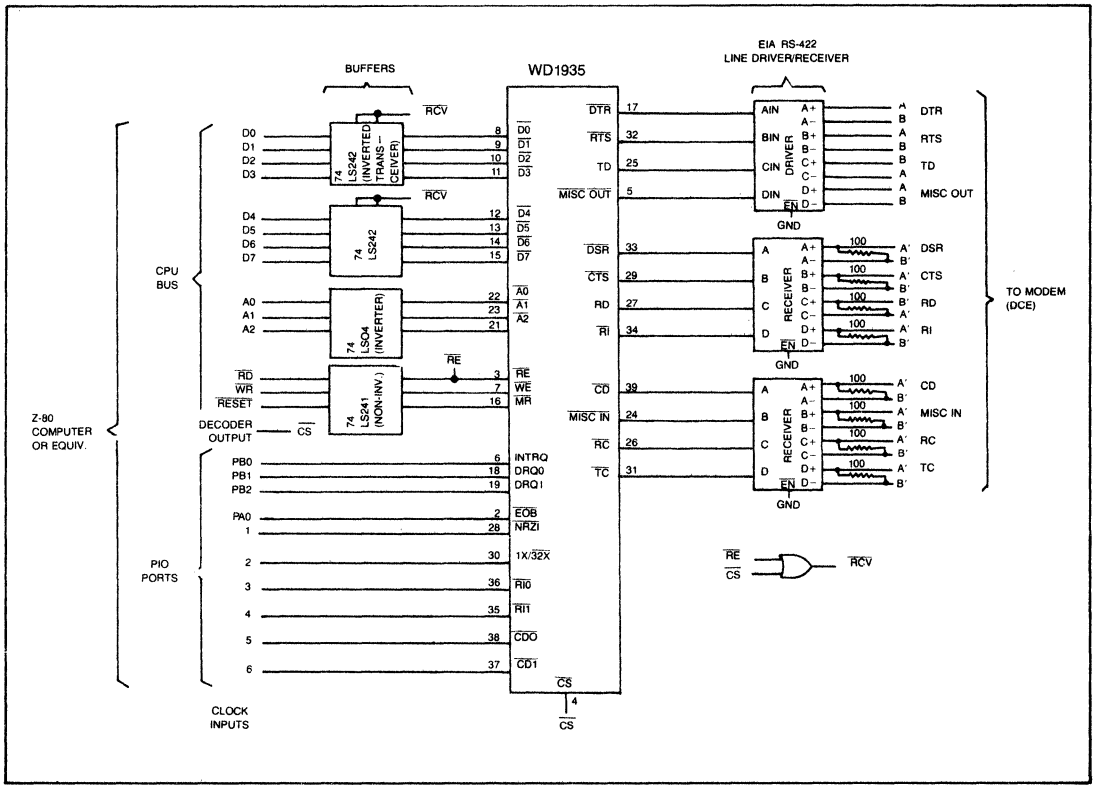
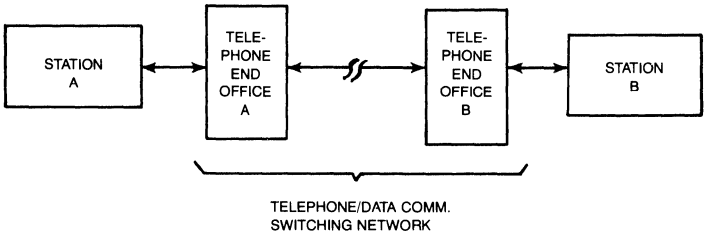
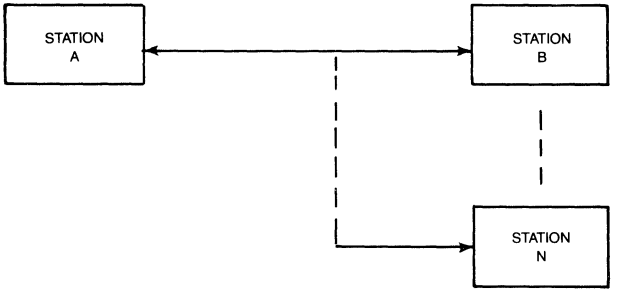


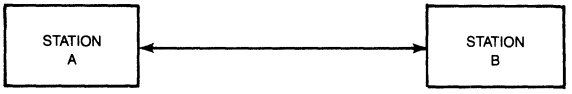
FIGURE 2. WD1935 MICROCOMPUTER



SWITCHED NETWORK



MULTIPOINT NETWORK



NONSWITCHED POINT TO POINT NETWORK

FIGURE 3. TYPICAL NETWORKS

LOOP DATA LINK SYSTEM

The Loop Mode is used in SDLC only. A loop data link system consists of one primary station (Loop Controller), and a number of secondary stations all functioning normally as repeaters. Figure 4 illustrates a typical Loop Data Link system.

Any secondary station finding its address in the address field captures the frame for action at that station. All received frames are relayed to the next station down the loop.

A secondary station is allowed to suspend the repeater function and initiate its transmission when a Go-Ahead pattern is received.

DATA COMMUNICATIONS EXAMPLE NO. 1

The diagrams below (Figures 5 and 6) illustrate a typical digital system employing several processing levels and digital communications protocols. It is flexible enough to satisfy several applications. For example, the host processor and remote terminals could be located in airline reservation offices and ticket counters, travel centers and travel agencies, central bank offices and branch banks, or department stores and individual cash registers.

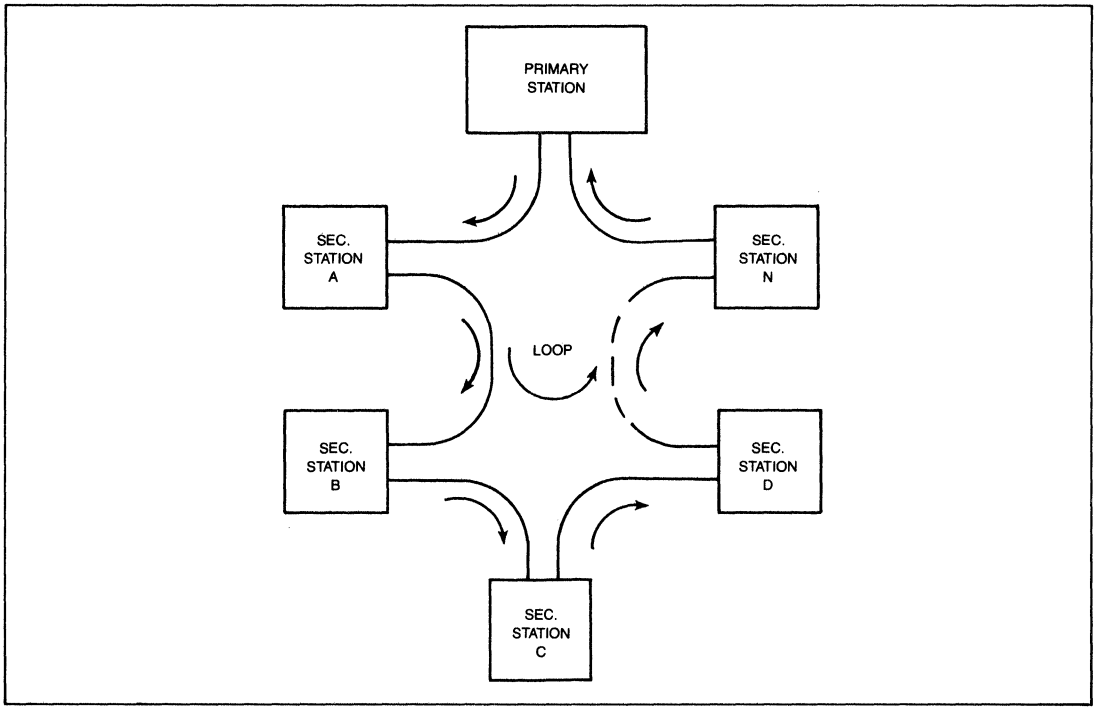


FIGURE 4. LOOP DATA LINK SYSTEM

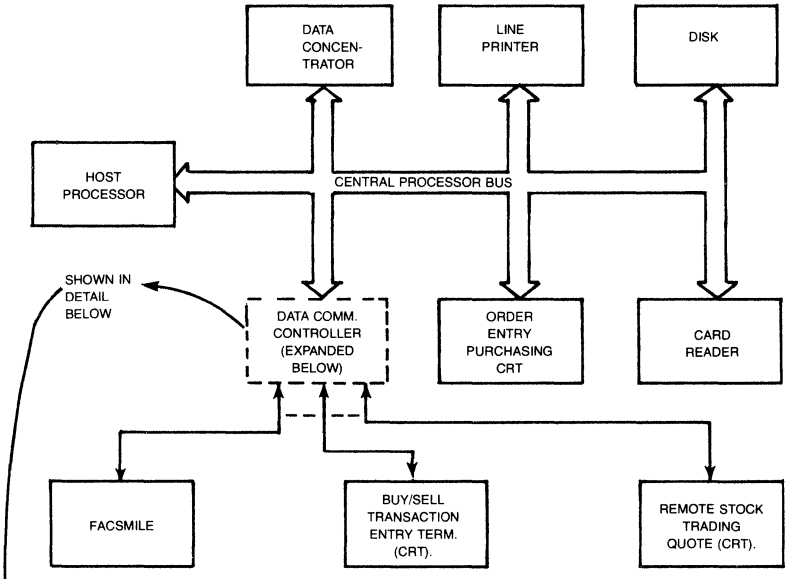


FIGURE 5. STOCK BROKERAGE SYSTEM

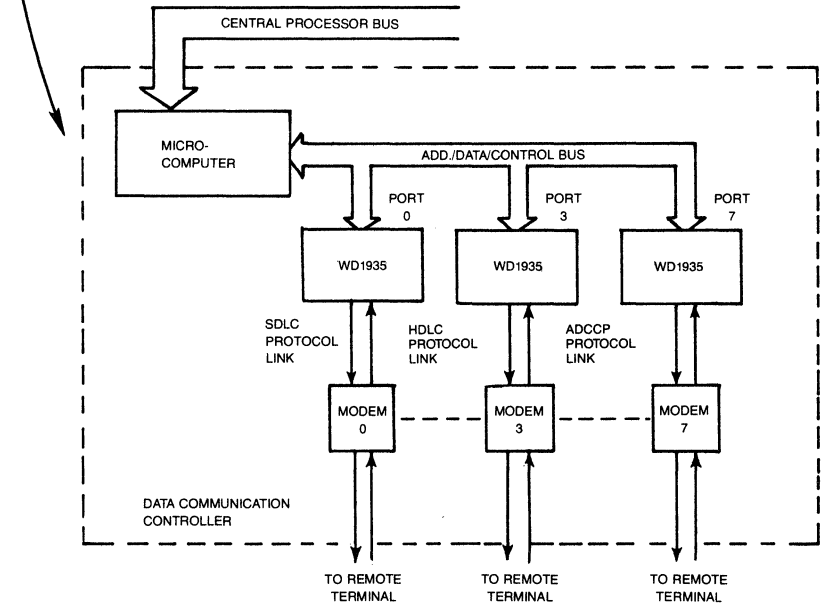


FIGURE 6. DATA COMMUNICATION CONTROLLER

DATA COMMUNICATIONS EXAMPLE NO. 2

Figure 7 illustrates a Host Computer that communicates through modems to a multiprotocol board. This in turn collects information from many remote stations through a Data Concentrator.

DATA COMMUNICATIONS EXAMPLE NO. 3

A simplified HDLC point to point connection is shown in Figure 8. In this example, no buffers or line drivers and receivers are used.

Figure 9 represents a more realistic application with the use of modems through a communications channel.

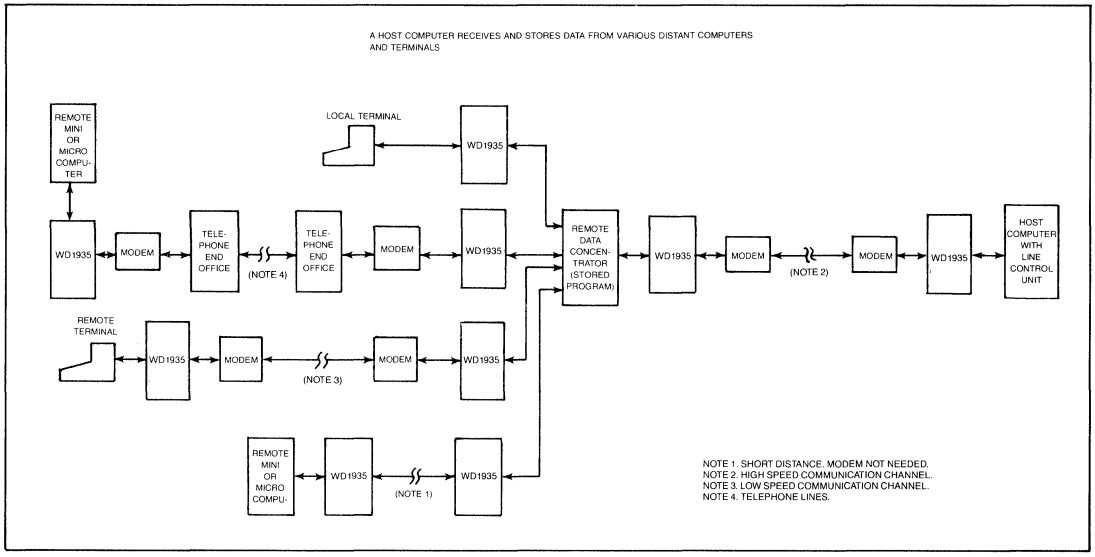


FIGURE 7. DATA CONCENTRATOR

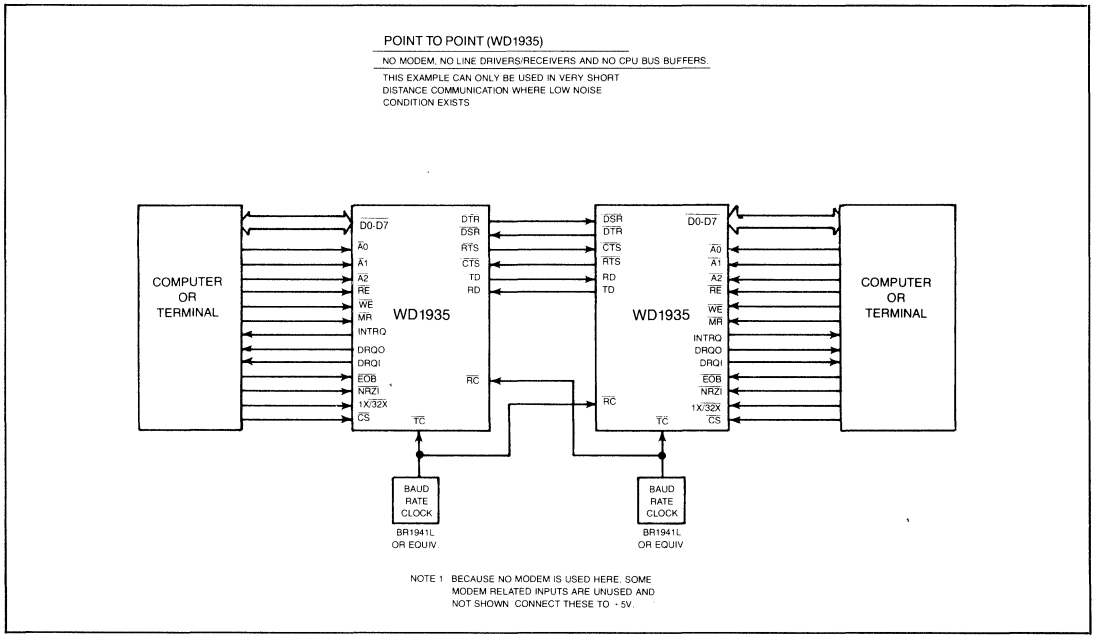


FIGURE 8. HDLC POINT TO POINT

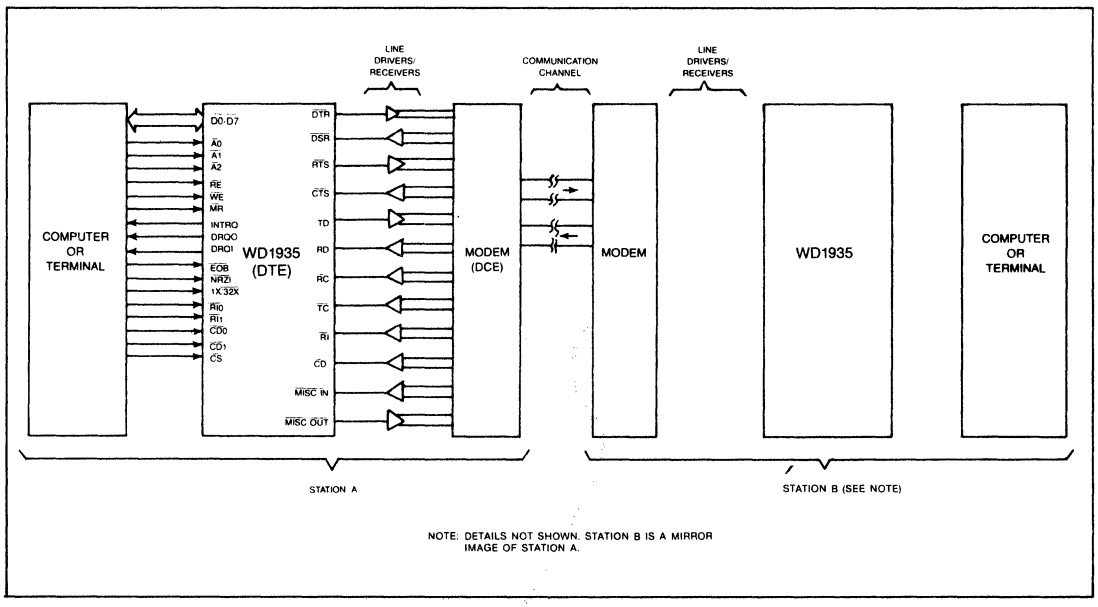


FIGURE 9. HDLC POINT TO POINT WITH MODEM

WD1935 PIN-OUTS AND BLOCK DIAGRAM

The WD1935 pin assignments and the block diagram are shown in Figure 10.

SHORT FORM REGISTER FORMAT AND ADDRESSING

Information concerning operating modes and status conditions are passed to and from the WD1935 through I/O addressable registers. Each register contains eight bits, where each bit represents a specific function and has its own mnemonics.

The state of each bit is represented by a "1" for TRUE and a "0" for FALSE. This may or may not correlate to a measurable voltage level at a pin, since some pins are TRUE when they are at 0 volts (this is indicated by a bar over the name, or a slash immediately preceeding the name).

The WD1935 registers are shown in Figure 11. Note that some bits are affected by the transmit clock ($\overline{TC}$) rate or the receive clock ($\overline{RC}$) rate.

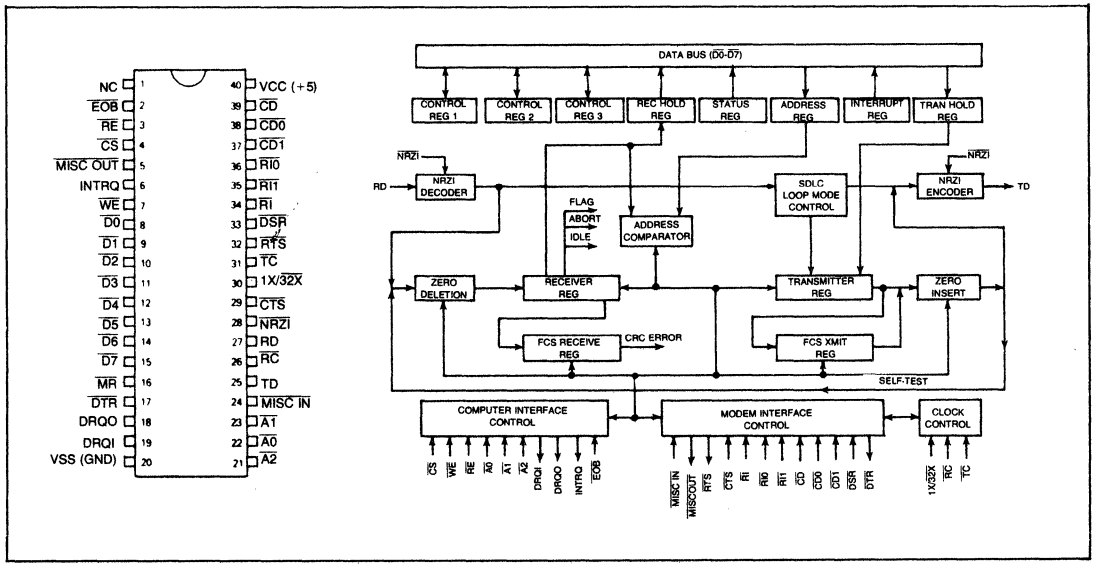
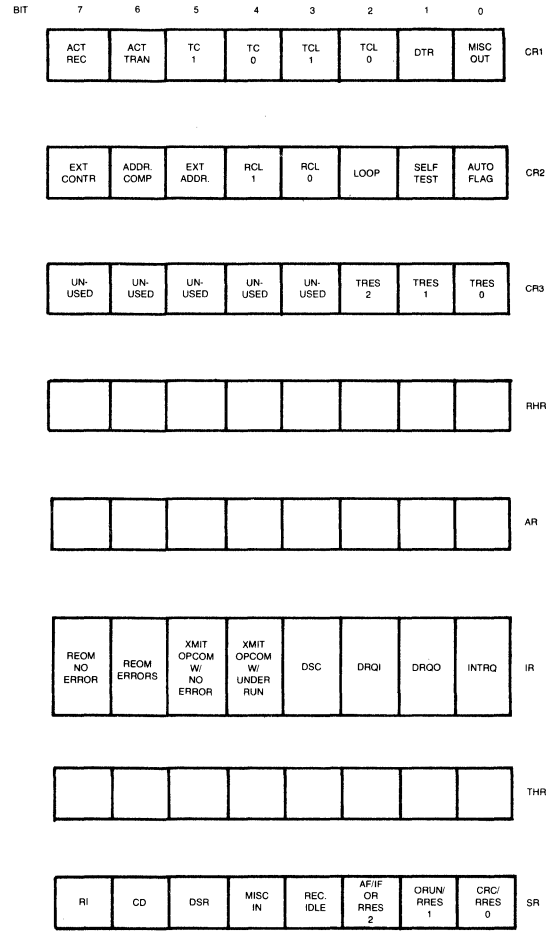


FIGURE 10. WD1935 PIN CONNECTIONS AND BLOCK DIAGRAM



WD1935 BIT ASSIGNMENTS

$\overline{A2}$	$\overline{A1}$	$\overline{A0}$	READ	WRITE	CLOCK
HI	HI	HI	CR1	CR1	NONE*
HI	HI	LO	CR2	CR2	NONE*
HI	LO	HI	CR3	CR3	NONE*
HI	LO	LO	RHR	AR	RHR = $\overline{RC}$. AR = NONE
LO	HI	HI	IR	THR	IR = $\overline{TC}$. THR = NONE
LO	HI	LO	SR	—	SR0-3 = $\overline{RC}$. SR4-7 = NONE

*After a master reset operation, 2.5 TC clock cycles are required.

WD1935 ADDRESSES AND CLOCKS

FIGURE 11. WD1935 REGISTERS

TRANSMISSION EXAMPLE 1 (ONE FRAME)

A typical sequence of events is shown here to transmit a message from computer A to another computer (or terminal) B through a switched network. The message to be sent is a synchronous SDLC protocol frame as shown below in Figure 12. For simplicity, the message sent in this example is very straightforward and short.

Line drivers and receivers are used, permitting transmission to a remote DCE or modem (see schematic in Figure 2).

Figure 13 illustrates the functional flow, and Figure 14 details the timing of the transmitted frame.

Note that the device can be programmed in several different ways to allow for various requirements.

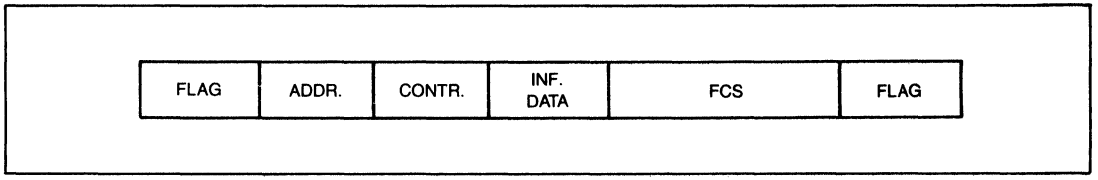


FIGURE 12. SDLC FRAME FORMAT

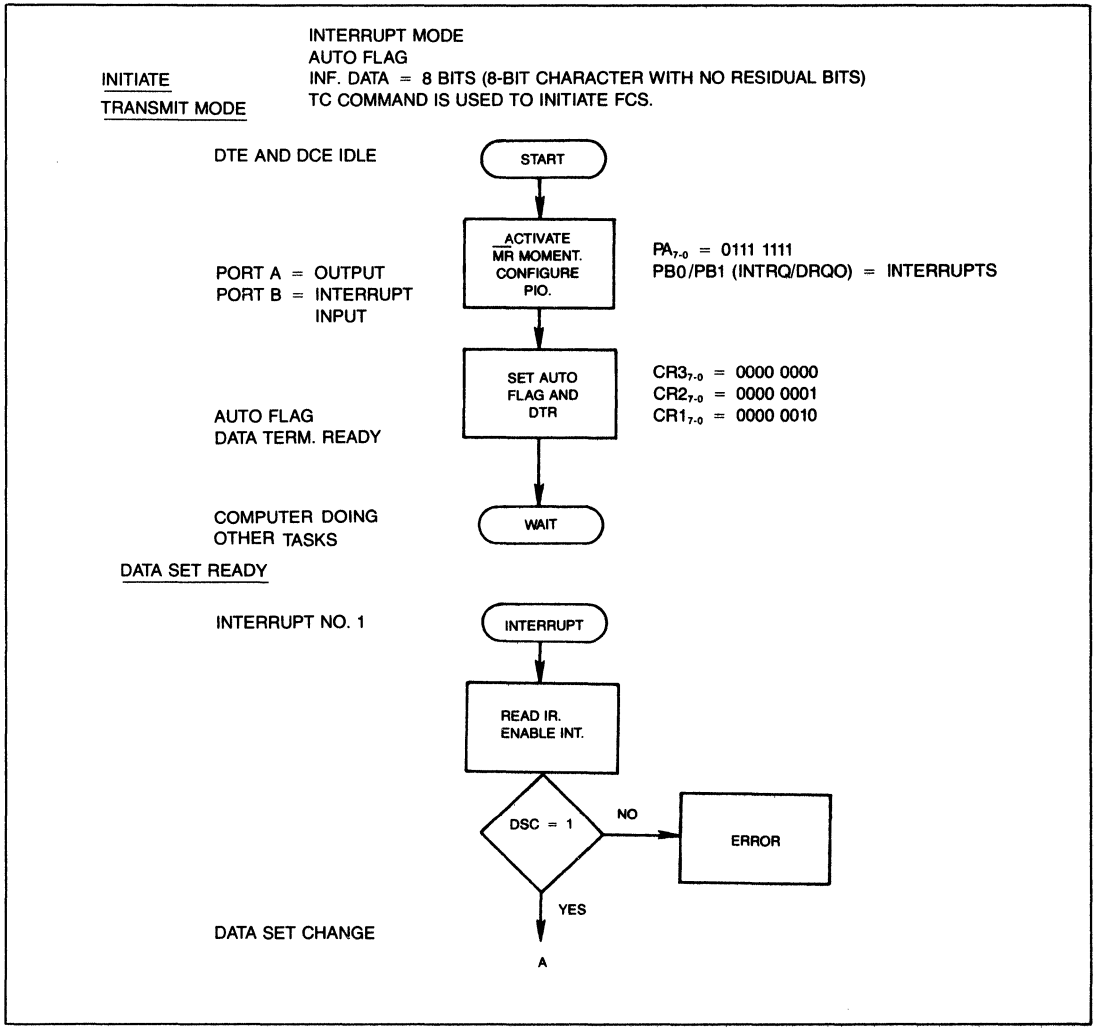


FIGURE 13. FLOW DIAGRAM OF FRAME TRANSMISSION

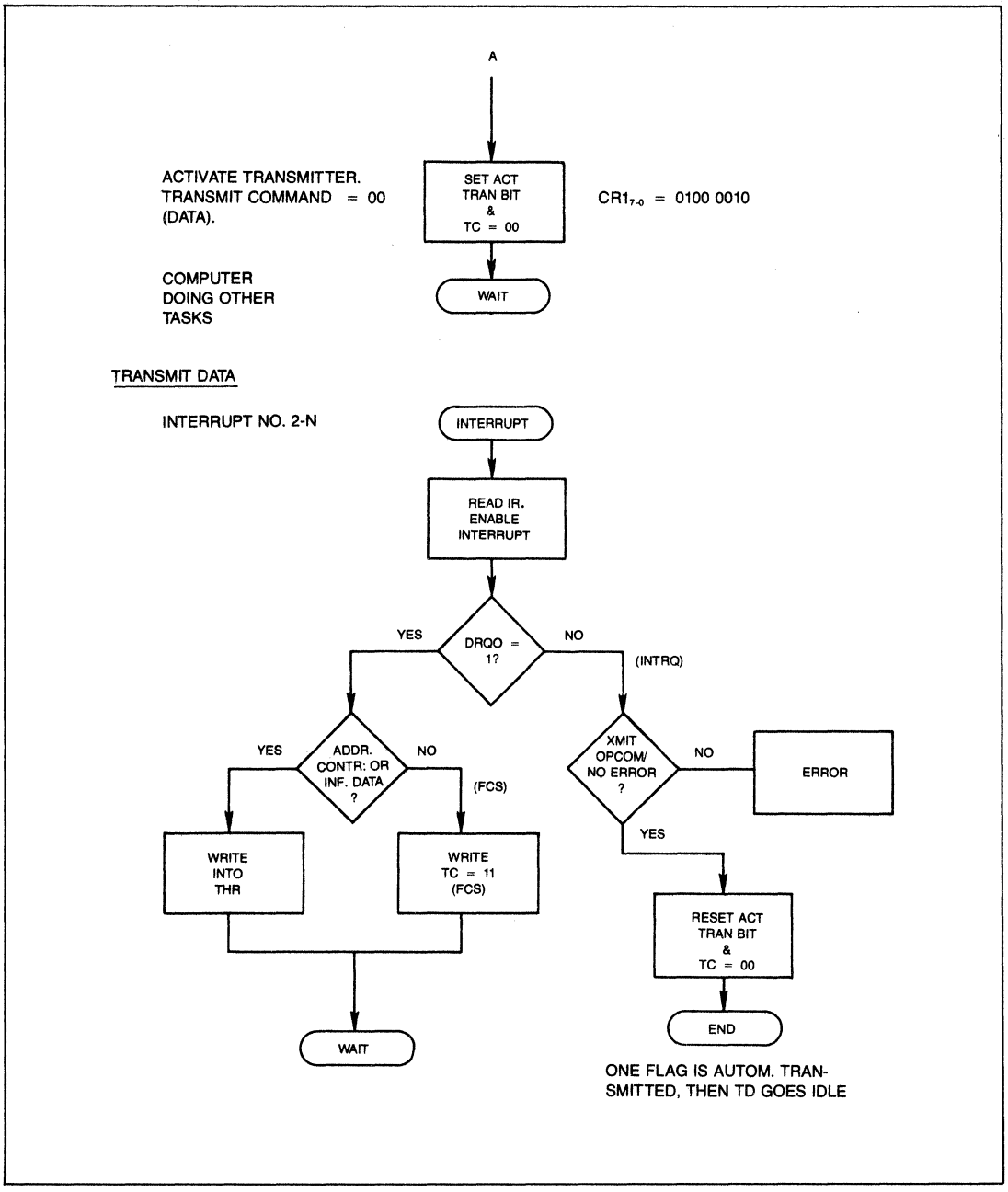


FIGURE 13. FLOW DIAGRAM OF FRAME TRANSMISSION (CONTINUED)

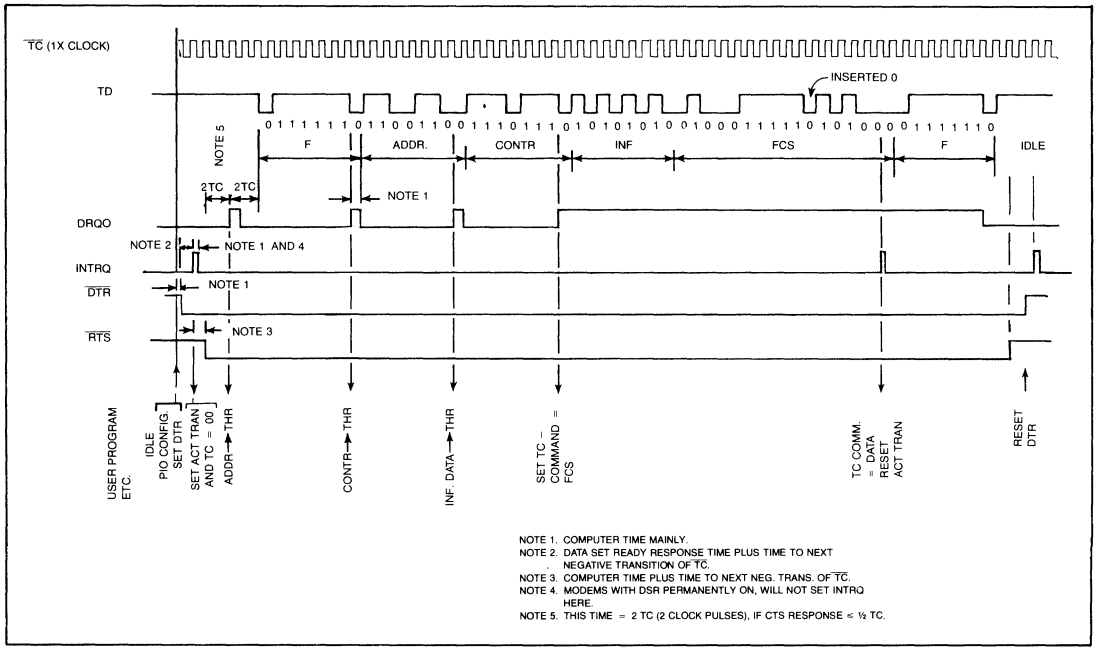


FIGURE 14. TIMING DIAGRAM OF FRAME TRANSMISSION

WD1935 TRANSMISSION EXAMPLE 2 (DMA APPLICATION)

The WD1935 is very efficient for DMA applications. The control registers are loaded to initiate the WD1935 for DMA mode in the same way as in Transmission Example 1. The Auto Flag bit is set, and the Transmitter Command is "DATA" (CR14 and CR15 bits = 00). The procedure to set up the link (initiate transmit mode and data set ready) is the same as in Transmission Example 1. When INTRQ is set and the Transmitter is activated, the DMA Controller Board takes over the control. From this time on, the DMA Controller Board responds on every DRQO (Data Request Out). When the last character is transmitted and the INTRQ is received, the control is switched back over to the CPU.

A very important feature of the WD1935 is the EOB (End of Block) input. Instead of using the normal (time-consuming) method of writing into a control register to start the FCS (Frame Check Sequence), the $\overline{EOB}$ input is activated at this time. At the next occurrence of INTRQ, the $\overline{EOB}$ signal is deactivated.

An example of a schematic/block diagram is shown in Figure 15, and a timing diagram is shown in Figures 16 through 18.

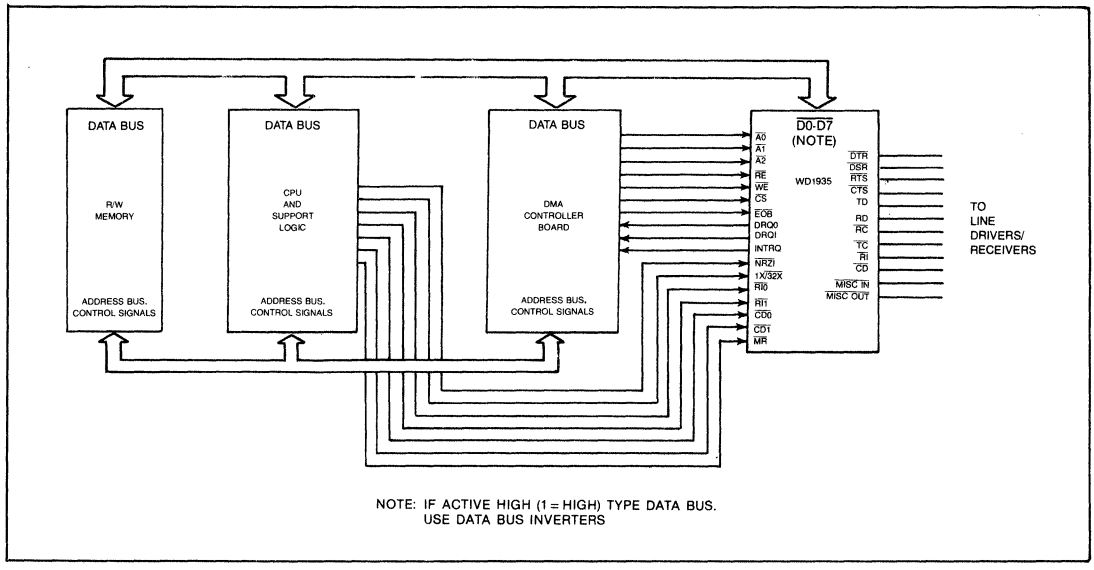


FIGURE 15. BLOCK DIAGRAM OF DMA APPLICATION

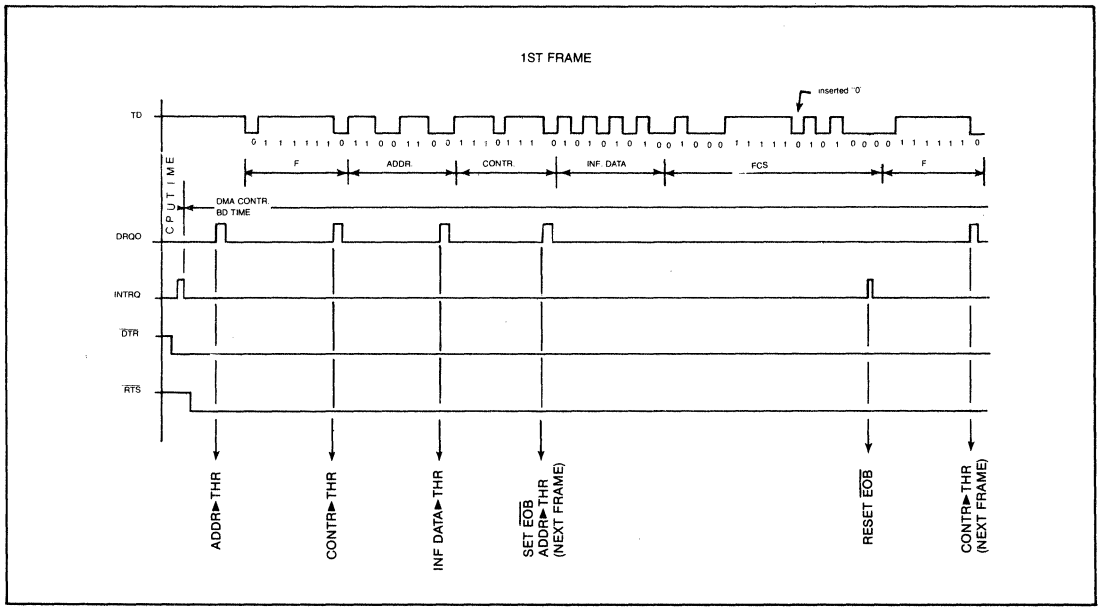


FIGURE 16. DMA TIMING OF FIRST FRAME

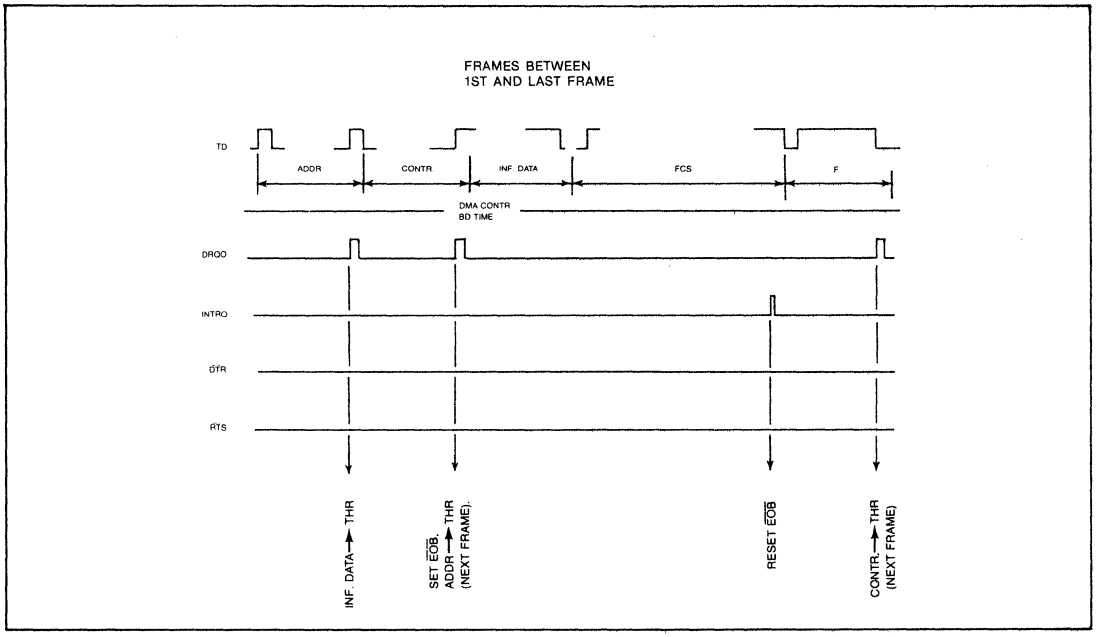


FIGURE 17. DMA TIMING OF MIDDLE FRAMES

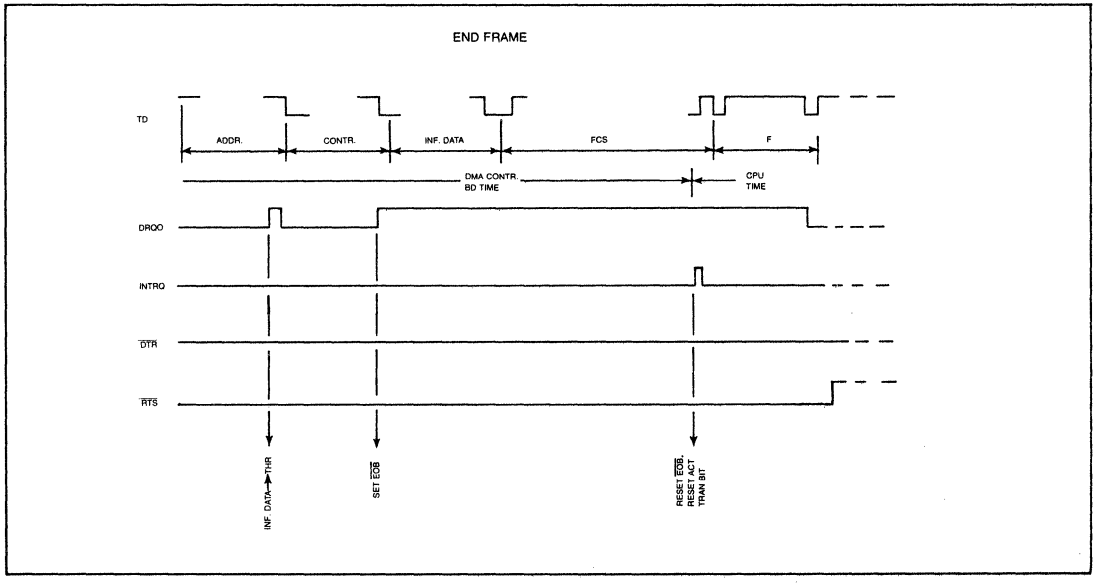


FIGURE 18. DMA TIMING OF LAST FRAME

WD1935 RECEPTION EXAMPLE 1

A sequence of events is shown in illustrating how to receive a message with the WD1935. For simplicity, the same SDLC frame structure is used as in Transmission Example 1. Also, please refer to the same interface circuitry shown in Figure 2.

Figure 19 illustrates the functional flow, and Figure 20 contains the timing information.

WD1935 RECEPTION EXAMPLE 2

This example shows a frame with two ADDRESS characters, two CONTROL characters, one 5-bit INFORMATION DATA character, and two residual bits. This example may not be a typical frame, but it shows how the WD1935 works in a wide range of frame structures.

The first FLAG and FCS are not shown in detail, and are not critical to this example.

Figure 21 illustrates the functional flow, and Figure 22 contains the timing information.

WD1935 LOOP DATA LINK EXAMPLE

this example shows how to program a secondary station to function in SDLC Loop mode. The functional flow is illustrated in Figure 24, and the interface circuit is show in Figure 2.

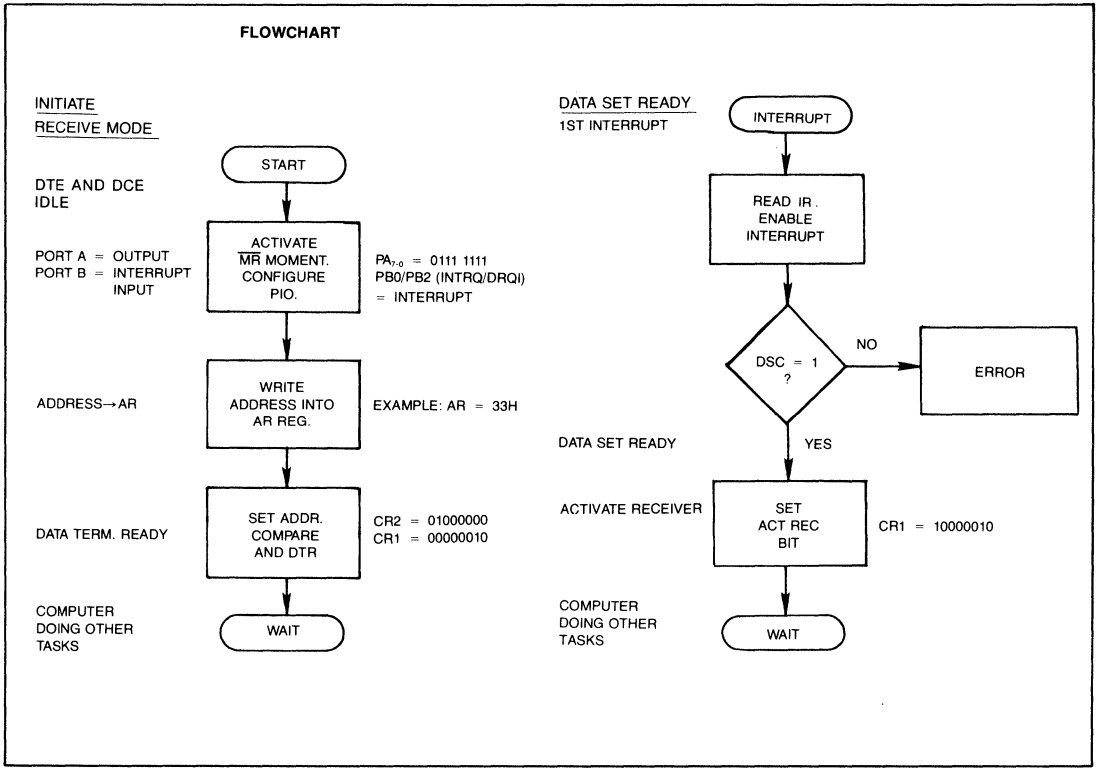


FIGURE 19. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

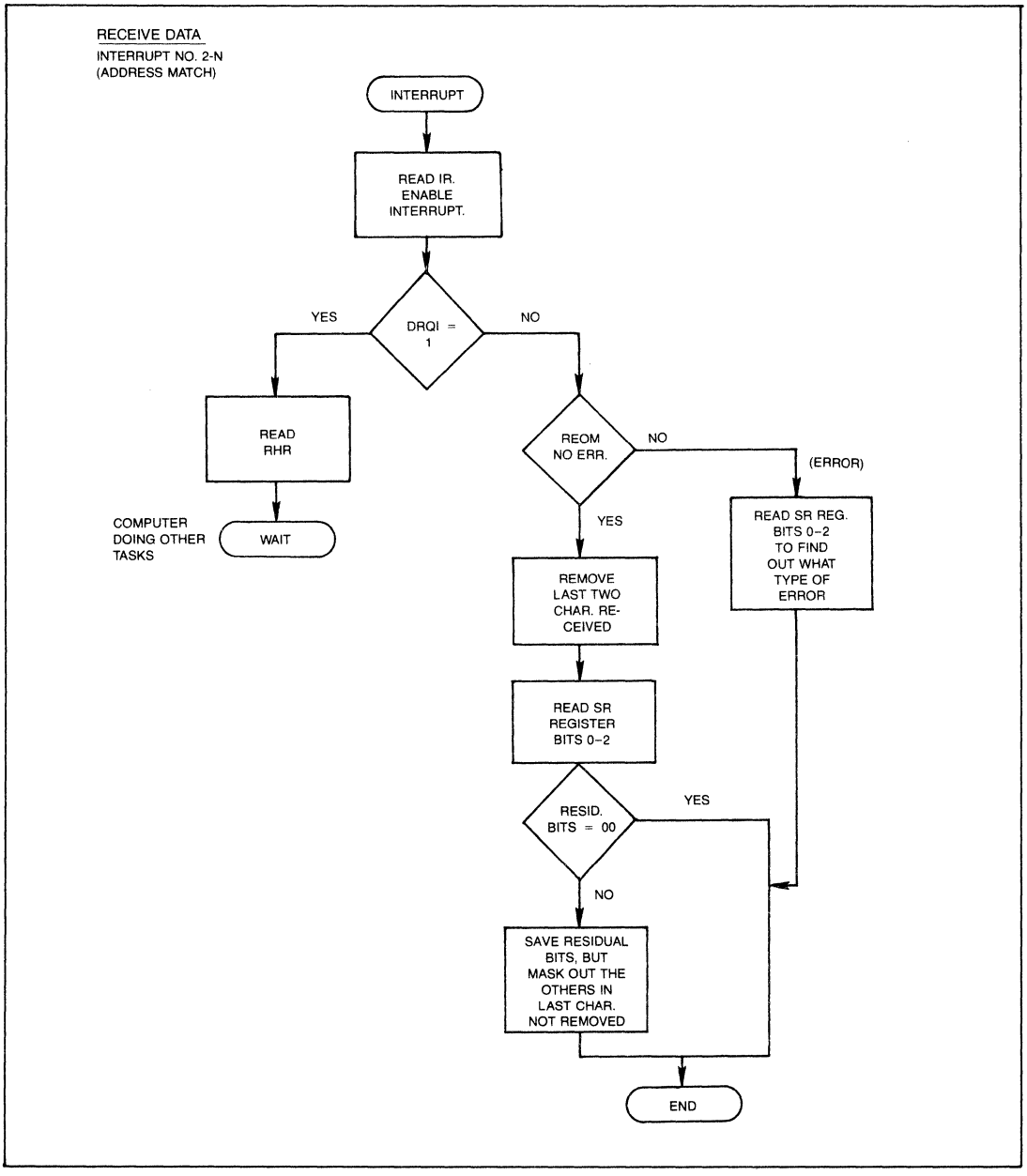
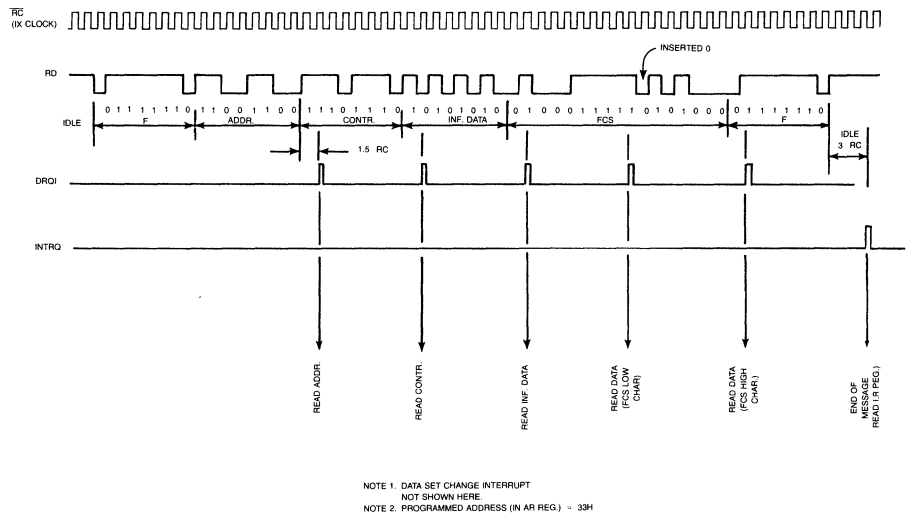


FIGURE 19. FLOW DIAGRAM OF FRAME RECEPTION (CONTINUED)



NOTE 1. DATA SET CHANGE INTERRUPT NOT SHOWN HERE.
NOTE 2. PROGRAMMED ADDRESS (IN AR REG.) = 33H

FIGURE 20. TIMING DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 1)

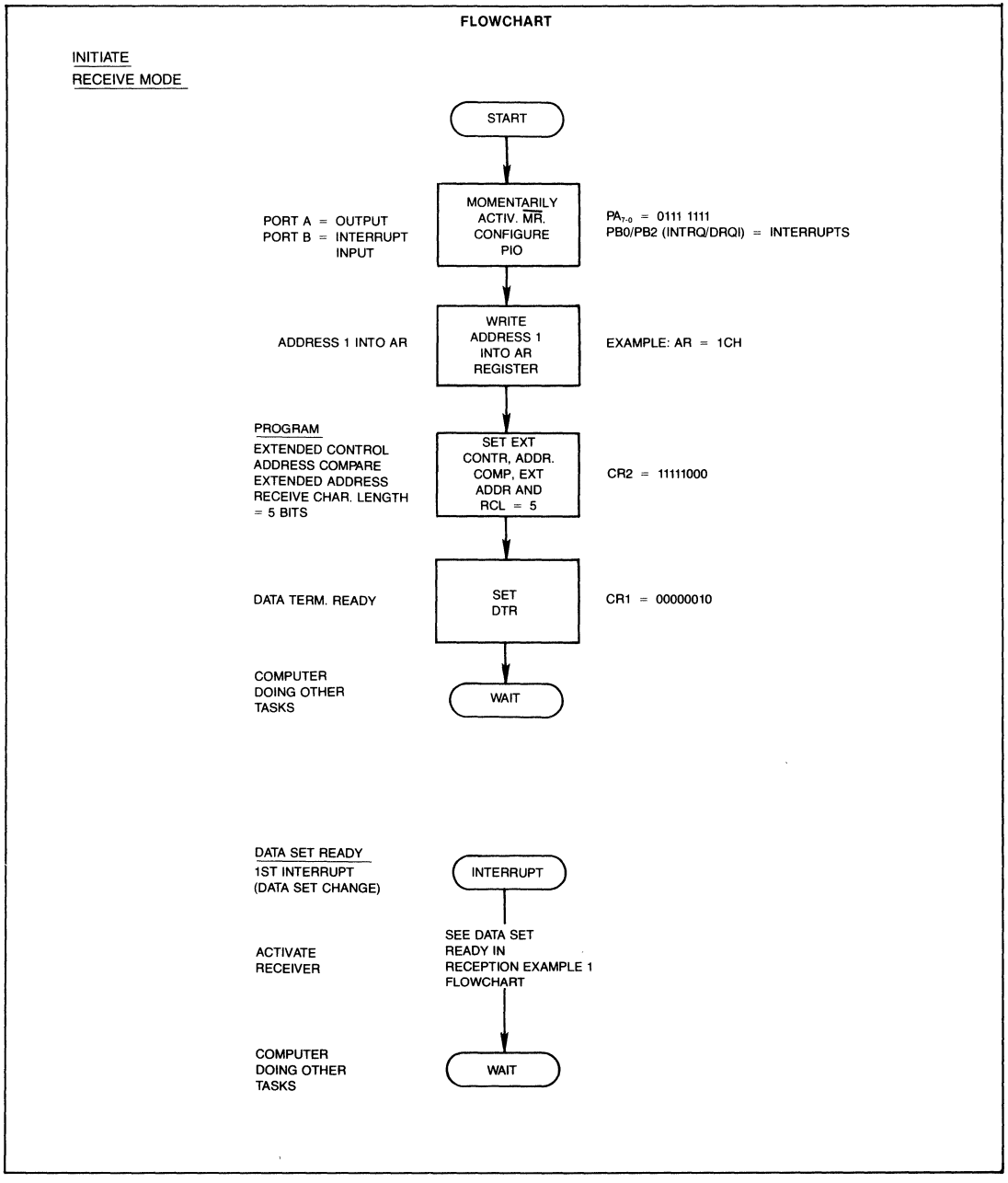


FIGURE 21. FLOW DIAGRAM OF FRAME RECEPTION (EXAMPLE NO. 2)

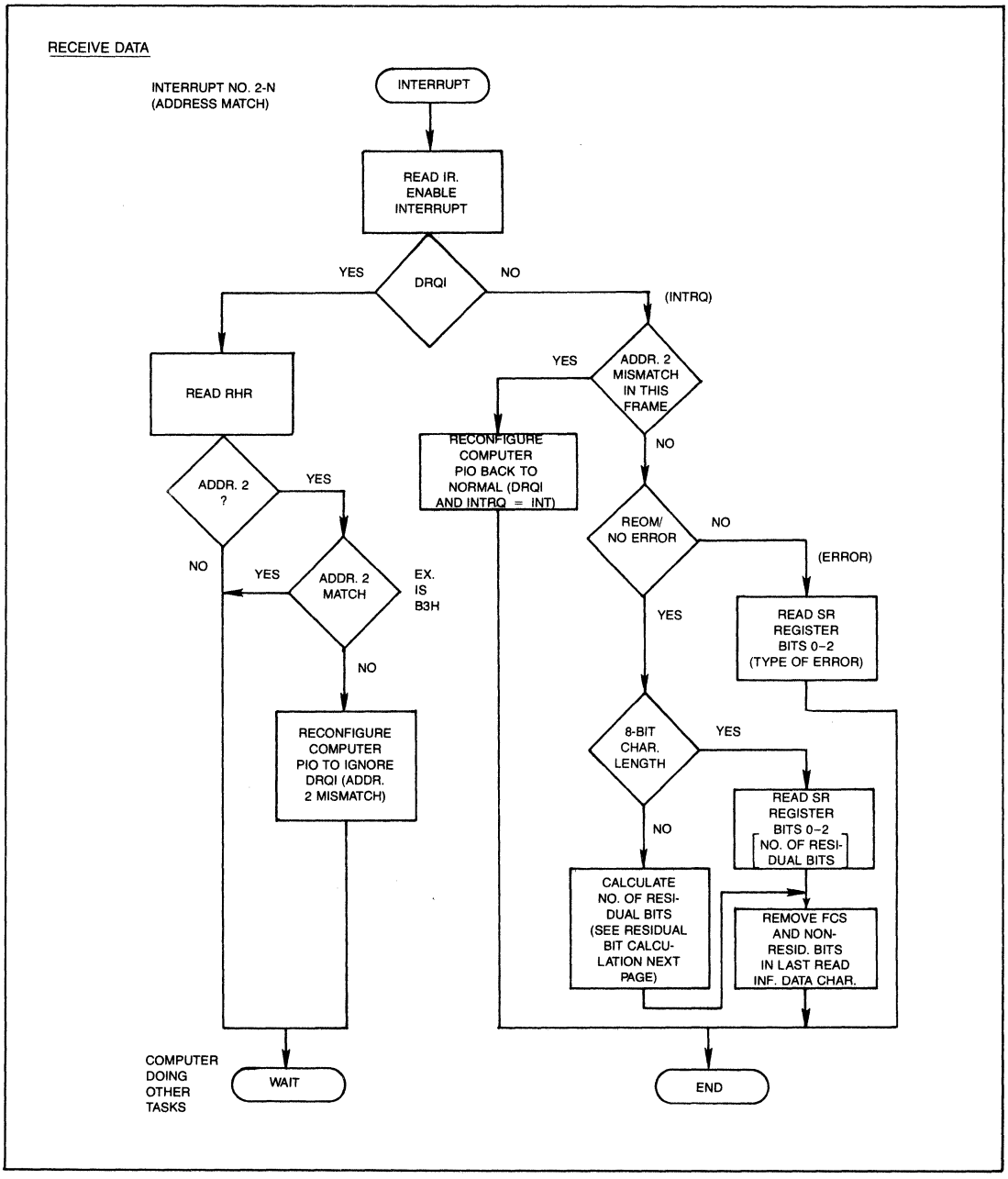


FIGURE 21. FLOW DIAGRAM OF FRAME RECEPTION (CONTINUED)

RESIDUAL BIT CALCULATION

THIS METHOD IS USED TO CALCULATE THE RESIDUAL BITS FROM THE COLLECTED DATA, RATHER THAN USING THE STATUS REGISTER BITS SR0-SR2.

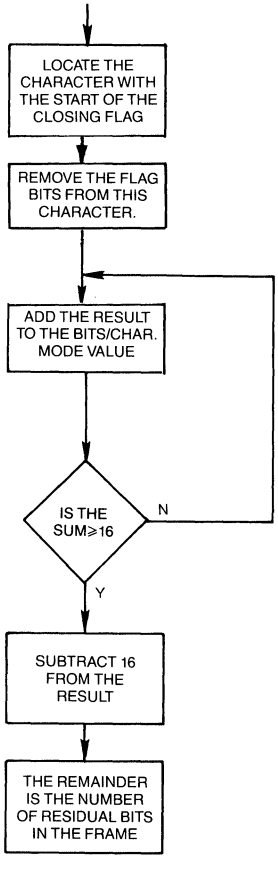


FIGURE 22. FLOW DIAGRAM OF RESIDUAL BIT CALCULATION

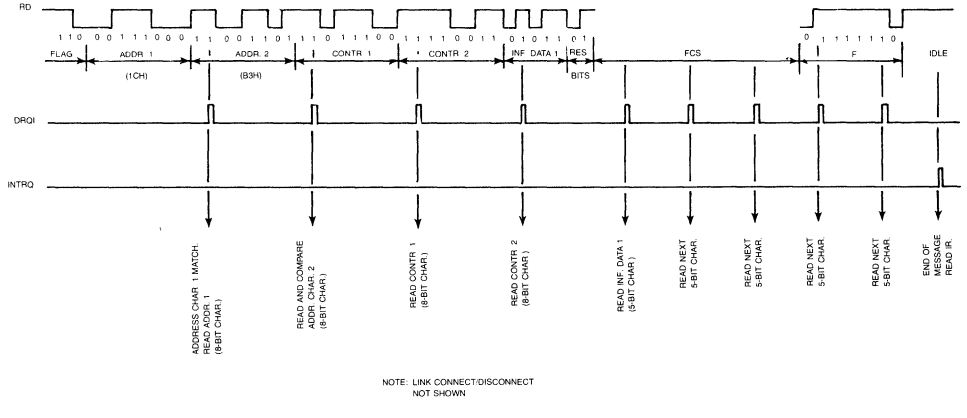


FIGURE 23. TIMING DIAGRAM OF FRAME RECEPTION

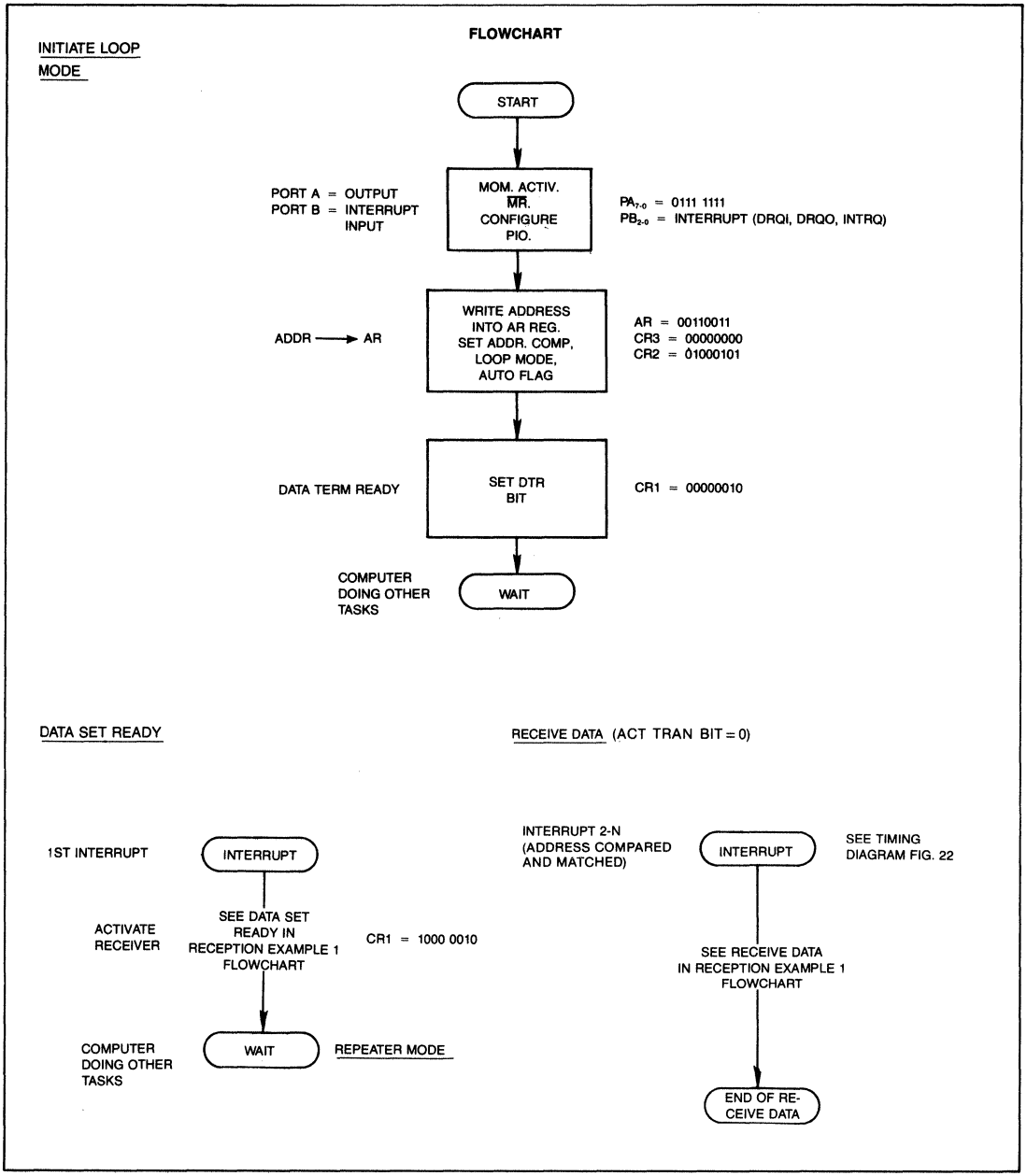


FIGURE 24. FLOW DIAGRAM OF SDLC LOOP MODE OPERATION

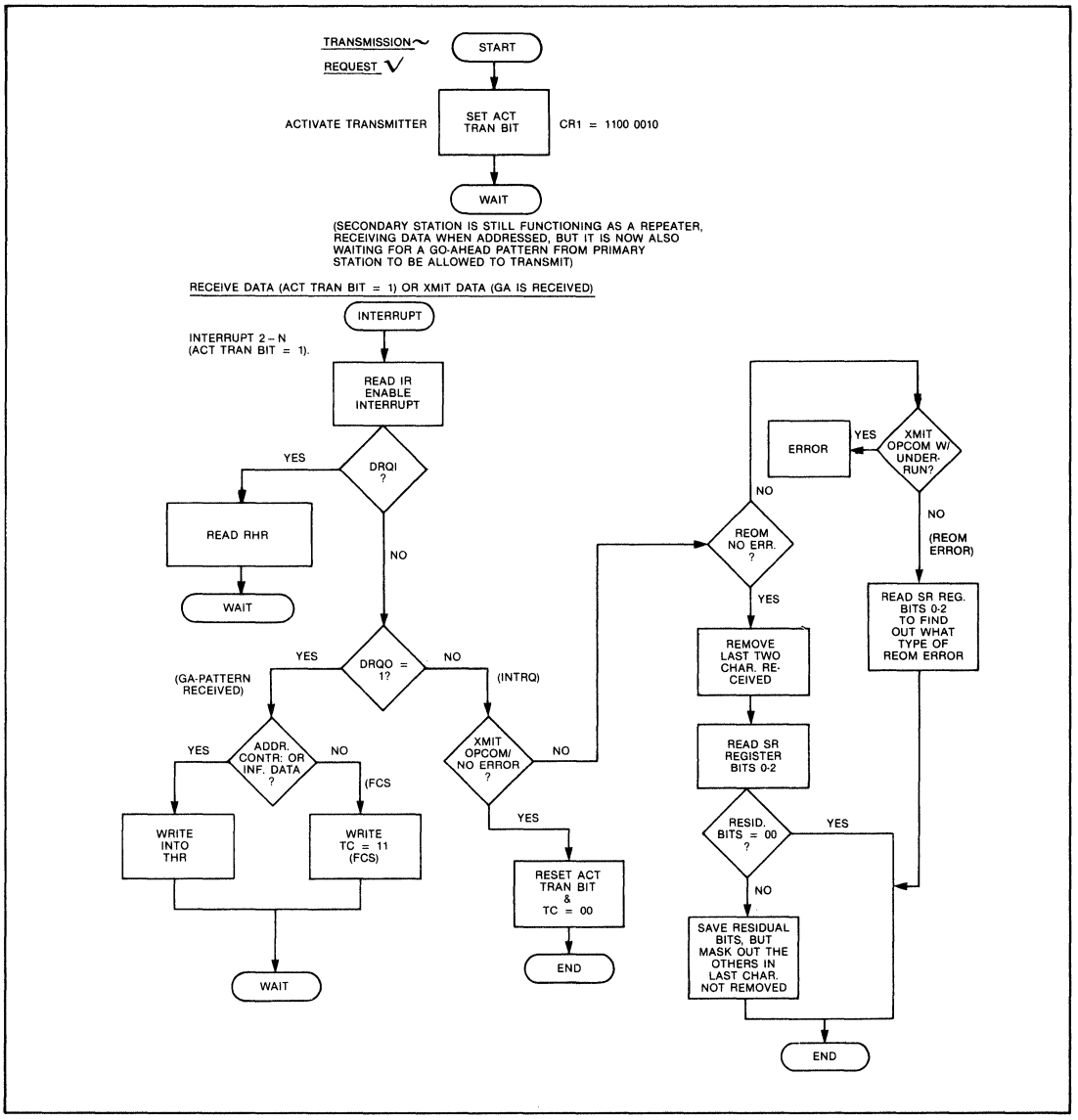


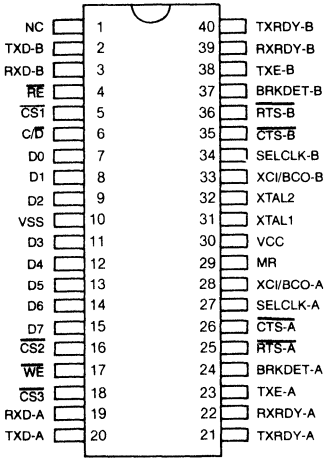
FIGURE 24. FLOW DIAGRAM OF SDLC LOOP MODE (CONTINUED)

FINAL

WD2123 DEUCE
Dual Enhanced Universal Communications Element

FEATURES

- TWO INDEPENDENT ASYNCHRONOUS FULL DUPLEX DATA COMMUNICATION CHANNELS (2 BOARTS)
- TWO INDEPENDENT BAUD RATE GENERATORS (ONE PER CHANNEL)
- EACH CHANNEL WITH FOLLOWING FEATURES:
- SELECTABLE 5 TO 8 BIT CHARACTERS
- 1X, 16X, 64X CLOCK RATES
- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES (INTERNAL)
- LINE BREAK DETECTION AND GENERATION
- 1, 1½, OR 2 STOP BIT SELECTION
- FALSE START BIT DETECTION
- ODD OR EVEN PARITY GENERATE AND DETECTION
- OVERRUN AND FRAMING DETECTION
- DOUBLE BUFFERING OF DATA
- TTL COMPATIBLE INPUTS AND OUTPUTS
- COMPATIBLE WITH 8251A (ASYNC ONLY) AND WD1983 DEVICES
- DIAGNOSTIC LOCAL LOOP-BACK MODE
- RXD INITIALIZATION UPON MASTER RESET
- ON-BOARD OSCILLATOR FOR EASE OF USE WITH A CRYSTAL
- VERSATILE CLOCK SELECT OPTIONS FOR INDEPENDENT TRANSMIT AND RECEIVE RATES



PIN DESIGNATION

DESCRIPTION

The Western Digital WD2123 Dual Enhanced Universal Communications Element (DEUCE) is a single chip MOS/LSI Data Communications Controller Circuit that contains two independent full-duplex asynchronous RECEIVER/TRANSMITTER CHANNELS and two independent BAUD RATE GENERATORS. The WD2123 is fabricated in N-Channel silicon gate technology and is packaged in a 40 pin plastic or ceramic package. All inputs and outputs are TTL compatible.

The WD2123 Block Diagram is shown in Figure 1. The WD2123 is a merger of two WD1983s and one WD1941 from WDC's line of communications devices on one piece of silicon. The 1983 is an asynchronous only version of the 8251A and the 1941 is a baud rate generator. In this manner, 8251A compatibility is maintained with the WD2123 with the added features of 2 channels and 2 baud rate generators on a single chip.

As depicted from the block diagram, the channels are referred to as CHANNELS A and B. CHANNEL A, which is an asynchronous 8251A, is addressed or controlled by the input signal $\overline{CS1}$. CHANNEL B is similarly controlled by $\overline{CS2}$. Finally, the BAUD RATE GENERATORS are controlled by $\overline{CS3}$.

Each channel of the WD2123 can be programmed to receive and transmit asynchronous serial data. The WD2123 performs serial-to-parallel conversion on data characters received from an input/output device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the status of either channel at any time. Status information on a per channel basis reported includes the type and the condition of the transfer operations being performed by the WD2123 as well as any transmission error conditions (parity, overrun, or framing). Programming the WD2123 is identical to the 8251A in the asynchronous mode, remembering that $\overline{CS1}$, when low, selects CHANNEL A and when $\overline{CS2}$ is low, selects CHANNEL B.

The WD2123 BAUD RATE GENERATORS may be selected either internally or externally. The clock select logic includes a clock select control bit CR1 (CS) in each COMMAND INSTRUCTION REGISTER. This control bit allows selection of the internal baud clock or an externally applied clock and works in conjunction with the select clock pin, "SELCLK" and the external clock input/baud clock output pin, "XCI/BCO". When CS is logic 1, the external clock select mode is selected. This means that the transmit and receive clocks (TXC and RXC) are internally tied together and the select clock pin, SELCLK, will determine whether those clocks are driven from the internal baud rate generator (SELCLK is high) or from the external clock input pin, "XCI/BCO", (SELCLK is low).

PIN DESCRIPTION

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
10	VSS	GROUND	Ground
30	VCC	POWER SUPPLY	+5VDC power supply input.
7 8 9 11 12 13 14 15	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the 8 bit Bidirectional Data Bus. It is the means of communication between the WD2123 and the CPU. Data, control, mode and status registers are accessed via this bus.
5	$\overline{CS1}$	CHIP SELECT ONE	V_{IL} on this input selects Channel A and enables computer communications with Channel A Data, control and status registers.
16	$\overline{CS2}$	CHIP SELECT TWO	V_{IL} on this input selects Channel B and enables computer communications with Channel B Data, control and status registers.
18	$\overline{CS3}$	CHIP SELECT THREE	V_{IL} on this input select the Baud Rate registers for programming.
6	C/$\overline{D}$	CONTROL or $\overline{DATA}$ SELECT	This input is used in conjunction with the appropriate Chip Select and an active read or write operation to determine register access via the Data Bus.
4	$\overline{RE}$	READ ENABLE	V_{IL} on this input allows the CPU to read data, or status information from the selected register.
17	$\overline{WE}$	WRITE ENABLE	V_{IL} on this input allows the CPU to write data or control information into the selected register.
29	MR	MASTER RESET	V_{IH} on this input resets both channels to the idle state and resets the status, command, mode and Data registers.
31	XTAL1	CRYSTAL OSCILLATOR INPUT	This is the input side of the on-chip oscillator. It can also be driven by an external clock source.
32	XTAL2	CRYSTAL OSCILLATOR OUTPUT	This is the output side of the on-chip oscillator.
27	SELCLK-A	SELECT CLOCK (Channel A)	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel A.
34	SELCLK-B	SELECT CLOCK (Channel B)	This input is used in conjunction with the Clock Select bit (CR1) in the command register to determine the baud clock source for Channel B.
28	XCI/BCO-A	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel A)	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel A)
33	XCI/BCO-B	EXTERNAL CLOCK INPUT/BAUD CLOCK OUTPUT-(Channel B)	This is a bidirectional port, which is used as the externally applied baud clock input or the internal baud rate generator output depending on the states of SELCLK and CR1 command bit. (Channel B)
26	$\overline{CTS-A}$	CLEAR-TO-SEND (Channel A)	V_{IL} on this input enables Channel A to transmit serial data if the Transmitter is enabled.

PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
35	$\overline{\text{CTS-B}}$	$\overline{\text{CLEAR-TO-SEND}}$ (Channel B)	V_{IL} on this input enables Channel B to transmit serial data if the Transmitter is enabled.
20	TXD-A	TRANSMIT DATA (Channel A)	This is the Serial Data Output from Channel A.
2	TXD-B	TRANSMIT DATA (Channel B)	This is the Serial Data Output from Channel B.
19	RXD-A	RECEIVE DATA (Channel A)	This is the Serial Data Input for Channel A.
3	RXD-B	RECEIVE DATA (Channel B)	This is the Serial Data Input for Channel B.
21	TXRDY-A	TRANSMITTER READY (Channel A)	This output, when high (V_{OH}), alerts the CPU that Channel A is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system. $\overline{\text{CTS}}$ must be asserted.
40	TXRDY-B	TRANSMITTER READY (Channel B)	This output, when high (V_{OH}), alerts the CPU that Channel B is ready to accept a new data character. The TXRDY output is automatically reset whenever a character is written into the Transmit Holding Register and can be used as an interrupt to the system. $\overline{\text{CTS}}$ must be asserted.
22	RXRDY-A	RECEIVER READY (Channel A)	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
39	RXRDY-B	RECEIVER READY (Channel B)	This output, when high (V_{OH}), alerts the CPU that Channel B contains a data character that is ready to be input. This output is automatically reset whenever the new character is read from the Receive Holding Register and can be used as an interrupt to the system.
23	TXE-A	TRANSMITTER EMPTY (Channel A)	This output, when high (V_{OH}), indicates that Channel A Transmitter has no new characters to send and is waiting in an idle state.
38	TXE-B	TRANSMITTER EMPTY (Channel B)	This output, when high (V_{OH}), indicates that Channel B Transmitter has no new characters to send and is waiting in an idle state.
24	BRKDET-A	BREAK DETECT (Channel A)	This output, when high (V_{OH}), indicates that the Receiver for Channel A has detected a break condition.
37	BRKDET-B	BREAK DETECT (Channel B)	This output, when high (V_{OH}), indicates that the Receiver for Channel B has detected a break condition.
25	$\overline{\text{RTS-A}}$	$\overline{\text{REQUEST-TO-SEND}}$ (Channel A)	A general purpose output that is controlled by the command register bit CR5 for Channel A.
36	$\overline{\text{RTS-B}}$	$\overline{\text{REQUEST-TO-SEND}}$ (Channel B)	A general purpose output that is controlled by the command register bit CR5 for Channel B.
1	NC		No Internal Connection.

If the internal BRG clock is selected, (SELCLK is high) then the external clock input pin becomes a BRG clock output. Hence, the mnemonic, "XCI/BCO".

When CR1 (CS) is logic 0, then internal clock select mode is selected. The transmit clock (TXC) is driven by the internal BRG clock and the receive clock is driven by the select clock pin, (SELCLK). The XCI/BCO pin becomes the baud clock output (the same signal that is being applied to TXC).

The WD2123 also provides a local loop-back test mode of operation for each channel. This diagnostic mode is independently controlled via the LB(CR7) bit of the COMMAND REGISTER. When LB is logic 1, the channel is programmed for Local Loop-Back. In this diagnostic mode, the TXD output is set to the marking (logic "1") state; the output of the TRANSMIT REGISTER is "looped-back" into the RECEIVER REGISTER input; $\overline{RTS}$ output is held high; the $\overline{CTS}$ and RXD inputs are ignored. An additional requirement is that the TEN(CR0) command bit and the REN(CR2) be logic 1. The status and output flags operate normally.

Each channel is also provided with break character generation and detection. (A break character is defined as all zero data bits, parity bit and stop bits after a valid start bit.) For break character generation, SBRK (CR3) command bit is set to a logic 1. This causes the TXD output to be forced low (spacing) for as long as SBRK is programmed high. The break detect output and status bit (SR6) is set to logic 1, indicating that the receiver has detected a break character. The framing error flag is also set to 1 for this condition.

ARCHITECTURE

The WD2123 is an eight bit bus-oriented device. Communication between the controlling CPU and the two RECEIVER/TRANSMITTER CHANNELS or the two BAUD RATE GENERATORS occurs via the 8-bit data bus through a common set of bus transceivers. Figure 1 is a Block Diagram of the WD2123.

A diagram of one of the two communication controllers is shown in Figure 2. There are two accessible data registers, which buffers transmit and receive data. They are the TRANSMIT HOLDING REGISTER and the RECEIVE HOLDING REGISTER. There is a parallel-to-serial shift register, the TRANSMIT REGISTER and a serial-to-parallel shift register, the RECEIVE REGISTER.

Operational Control and monitoring of the CHANNEL is performed by two CONTROL REGISTERS (the COMMAND INSTRUCTION REGISTER and the MODE INSTRUCTION REGISTER) and the STATUS REGISTER.

A read/write control circuit allows programming/monitoring or loading/reading of data in the CONTROL, STATUS and HOLDING REGISTERS by activating the appropriate control lines: Chip Select ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$), READ ENABLE ($\overline{RE}$), WRITE ENABLE ($\overline{WE}$) and CONTROL or DATA SELECT (C/$\overline{D}$).

Internal control of each channel is by means of two internal microcontrollers: one for transmit and one for receive. The control registers, various counters and external signals provide inputs to the microcontrollers, which generate the necessary control signals to send and receive serial data according to the programmed protocol.

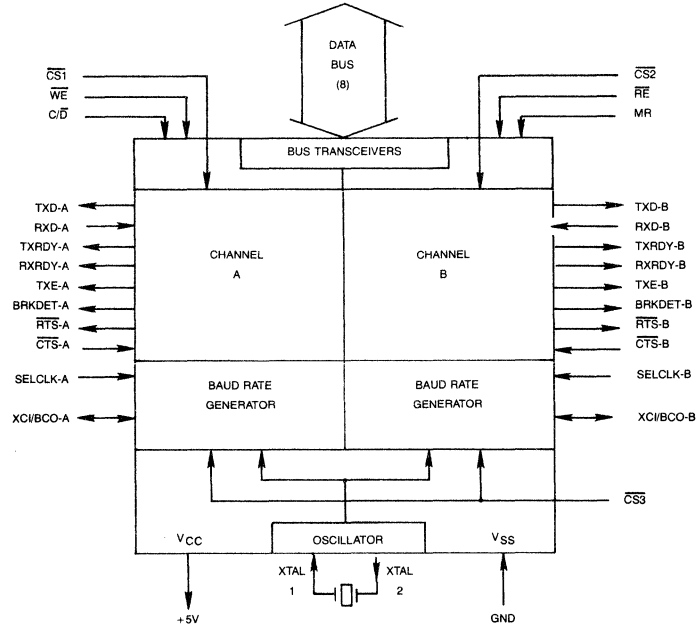


FIGURE 1. WD2123 BLOCK DIAGRAM

A diagram of one of the two BAUD RATE GENERATORS is shown in Figure 3. The 4 low order DATA BUS bits, D0-D3, are used to program the desired rate by loading the RATE REGISTER. Control signals CS3, We and C/D are used to select and load the appropriate register.

The contents of the RATE REGISTER is decoded and addresses a FREQUENCY SELECT ROM for the proper frequency, which is generated by the DIVIDER circuitry and the control logic.

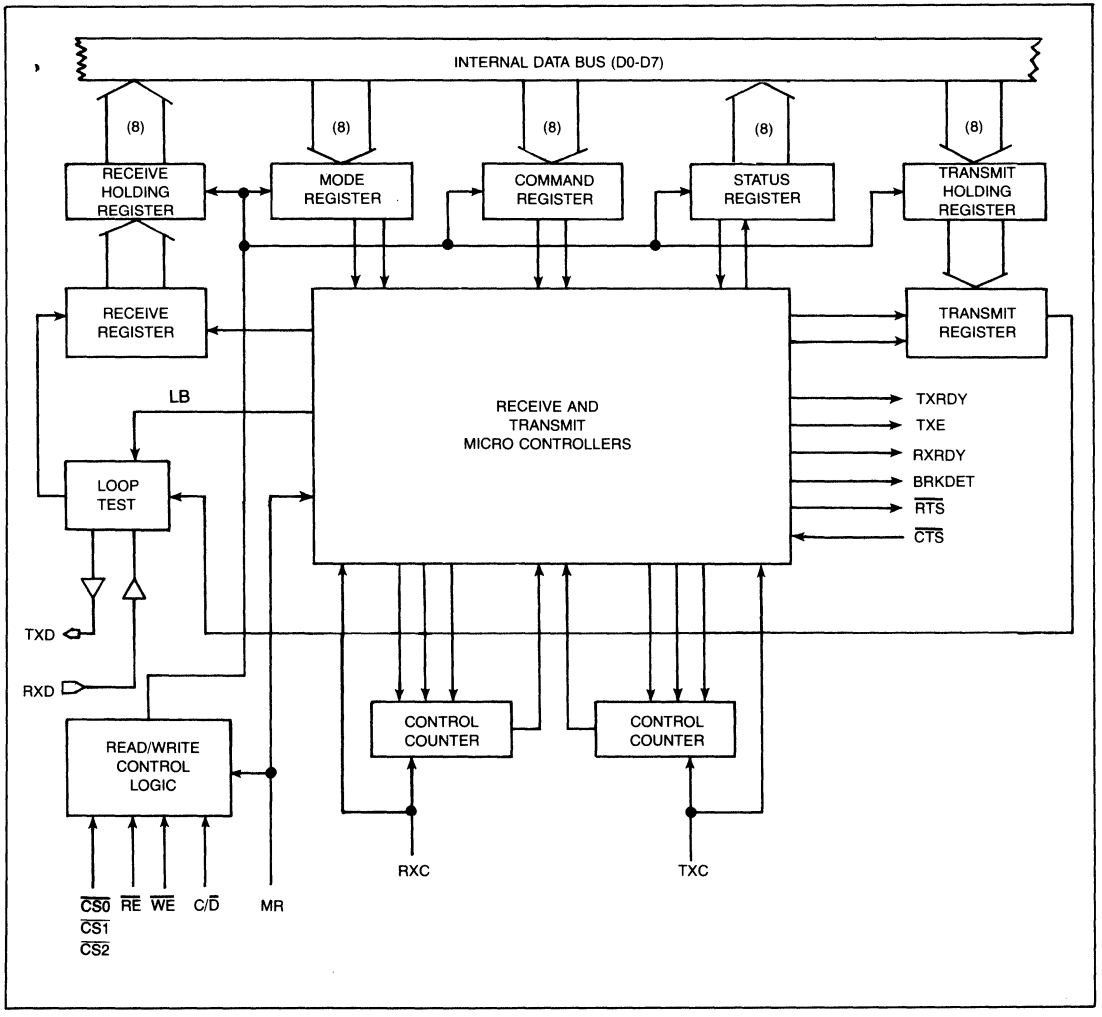


FIGURE 2. RECEIVE/TRANSMIT COMMUNICATIONS CONTROLLER DIAGRAM

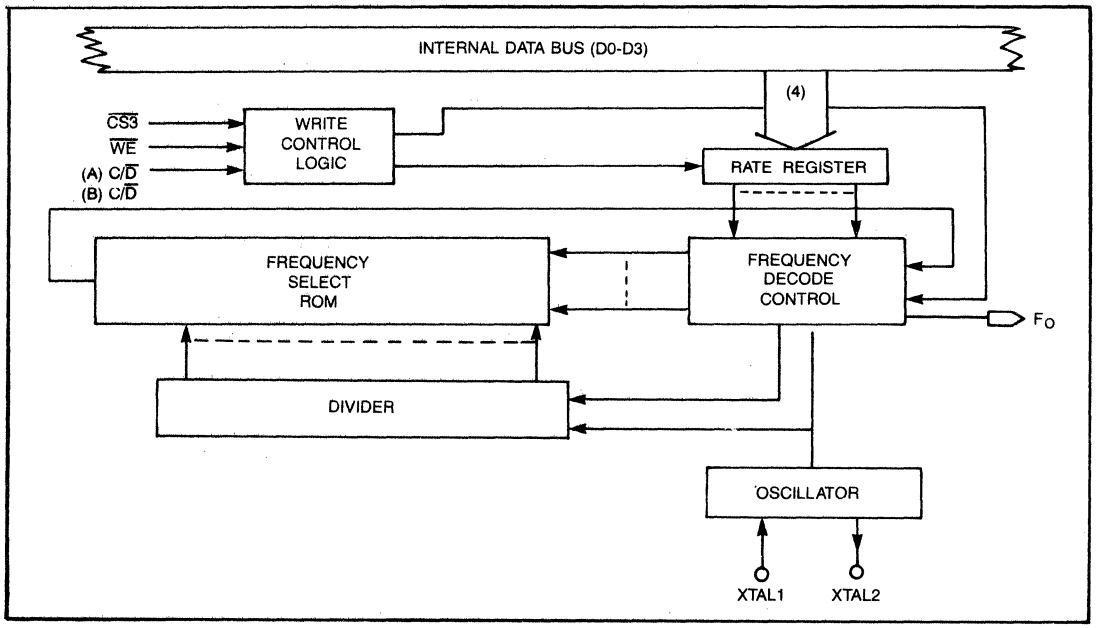


FIGURE 3. WD2123 BAUD RATE GENERATOR DIAGRAM

The WD2123 registers are addressed by the following table:

C/D	RE	WE	CS1	CS2	CS3	REGISTER SELECTED		
L	L	H	L	H	H	RECEIVE HOLDING REG.	—	CHA
L	H	L	L	H	H	TRANSMIT HOLDING REG.	—	CHA
H	L	H	L	H	H	STATUS REG.	—	CHA
H	H	L	L	H	H	MODE AND COMMAND REG.	—	CHA
L	L	H	H	L	H	RECEIVE HOLDING REG.	—	CHB
L	H	L	H	L	H	TRANSMIT HOLDING REG.	—	CHB
H	L	H	H	L	H	STATUS REG.	—	CHB
H	H	L	H	L	H	MODE and COMMAND REG.	—	CHB
L	H	L	H	H	L	RATE REG.	—	CHA
H	H	L	H	H	L	RATE REG.	—	CHB
X	X	X	H	H	H	DATA BUS IN HIGH IMPEDANCE MODE		

TABLE 1. WD2123 REGISTER ADDRESSING

Note:
"L" means V_{IL} at pins.
"H" means V_{IH} at pins.
"X" means don't care.

The WD2123 contains two MODE REGISTERS—one for each channel. The format and definition of the MODE REGISTERS are shown below:

MR7	MR6	MR5	MR4	MR3	MR2	MR1	MR0
S2	S1	EP	PEN	L2	L1	B2	B1

B2	B1	BAUD RATE FACTOR
0	0	Undefined
0	1	1X
1	0	16X
1	1	64X
L2	**L1**	**CHARACTER LENGTH**
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits
PEN		**PARITY ENABLE**
0		Disable Parity
1		Enable Parity
EP		**PARITY SELECT**
0		Odd Parity
1		Even Parity
S2	**S1**	**NUMBER OF STOP BITS**
0	0	Invalid
0	1	1 Bit
1	0	1½ Bits*
1	1	2 Bits

TABLE 2. WD2123 MODE REGISTERS

* 16X and 64X only. 1X will be 2 stop bits.

The WD2123 contains two COMMAND REGISTERS—one per channel. The format and definition of the COMMAND REGISTERS are shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
LB	IR	RTS	ER	SBK	REN	CS	TEN

TEN	TRANSMIT ENABLE
1	Enable
0	Disable
CS	**CLOCK SELECT**
1	XMIT and RCV Clock source common
0	XMIT and RCV Clock sources different
REN	**RECEIVE ENABLE**
1	Enable
0	Disable
SBK	**SEND BREAK CHARACTER**
1	Force TXD Low
0	Normal Operation
ER	**ERROR RESET**
1	Reset Error Flags
0	No Reset
RTS	**REQUEST TO SEND**
1	Force $\overline{RTS}$ pin = 0 (V_{OL})
0	Force $\overline{RTS}$ pin = 1 (V_{OH})
IR	**INTERNAL RESET**
1	Next Write to Mode Register
0	Next Write to Command Register
LB	**LOOP BACK ENABLE**
0	Normal Operation Mode
1	Local Loop-Back Mode

TABLE 3. WD2123 CONTROL REGISTERS

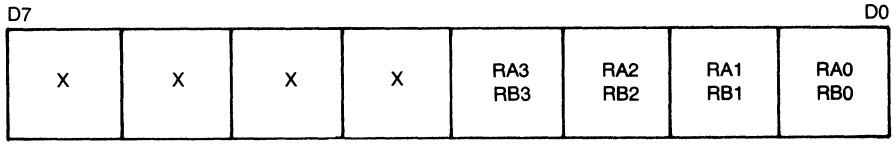
The WD2123 contains two STATUS REGISTERS—one per channel. The STATUS REGISTER is a read-only register. The format and definition of the STATUS REGISTERS are shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
CTS	BRK DET	FE	OE	PE	TXE	RX RDY	TX RDY

TXRDY	**TRANSMITTER READY**
1	Denotes THR is empty and ready for a new character
0	THR not empty. (Reset when THR is loaded by CPU)
RXRDY	**RECEIVER READY**
1	Denotes that the RHR contains a valid character
0	RHR does not contain a valid character. (Reset when the CPU reads the RHR)
TXE	**TRANSMITTER EMPTY**
1	Denotes that the TR is empty
0	Denotes that the TR is not empty
PE	**PARITY ERROR**
1	Denotes Parity Error
0	No Parity Error. (Reset by ER bit of command register)
OE	**OVERRUN ERROR**
1	Denotes Overrun Error
0	No Overrun Error. (Reset by ER bit of command register)
FE	**FRAMING ERROR**
1	Denotes Framing Error
0	No Framing Error. (Reset by ER bit of command register)
BRKDET	**BREAK DETECT**
1	Indicates that the receiver has detected a line break condition. (FE will also be set)
0	No Break Condition detected for at least one bit time
CTS	**CLEAR-TO-SEND**
1	Indicates that the $\overline{CTS}$ pin is active (V_{IL})
0	Indicates that the $\overline{CTS}$ pin is not active (V_{IH})

TABLE 4. WD2123 STATUS REGISTERS

The WD2123 contains two RATE REGISTERS that are used to select 16 BAUD rates when CR1 = 1 and SELCLK = 1. The Format of the RATE REGISTERS is shown below. Note that the Receiver and the Transmitter of any channel run off the same Baud clock except when CR1 = 0, then the Transmitter runs off the Baud Clock and the Receiver runs off an externally applied signal input on the SELCLK pin.



When C/D = 0, RA3 to RA0 are loaded.
When C/$\overline{D}$ = 1, RB3 to RB0 are loaded.

The C/$\overline{D}$ line is used in conjunction with $\overline{CS3}$ and $\overline{WE}$ to program the desired BAUD rate. When C/$\overline{D}$ is low, Channel A is selected, and when C/$\overline{D}$ is high, Channel B is selected. The low order 4 bits of the DATA BUS are loaded into the selected rate register, and the high order 4 bits are ignored.

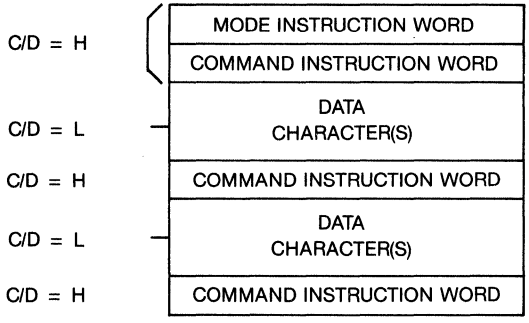
When the crystal frequency equals 1.8432 MH_Z the following baud rates may be programmed.

				BAUD RATE			FREQUENCY	
R3	R2	R1	R0	BRF 1X	BRF 16X	BRF 64X	(KHZ)	DIVISOR
0	0	0	0	800	50.0	12.50	0.80	2304
0	0	0	1	1,200	75.0	18.75	1.20	1536
0	0	1	0	1,760	110.0	27.50	1.76	1049
0	0	1	1	2,150	134.5	33.59	2.15	855
0	1	0	0	2,400	150.0	37.50	2.40	768
0	1	0	1	3,200	200.0	50.00	3.20	576
0	1	1	0	4,800	300.0	75.00	4.80	384
0	1	1	1	9,600	600.0	150.00	9.60	192
1	0	0	0	19,200	1,200.0	300.00	19.20	96
1	0	0	1	28,800	1,800.0	450.00	28.80	64
1	0	1	0	38,400	2,400.0	600.00	38.40	48
1	0	1	1	57,600	3,600.0	900.00	57.60	32
1	1	0	0	76,800	4,800.0	1,200.00	76.80	24
1	1	0	1	115,200	7,200.0	1,800.00	115.20	16
1	1	1	0	153,600	9,600.0	2,400.00	153.60	12
1	1	1	1	307,200	19,200.0	4,800.00	307.20	6

TABLE 5. WD2123 BAUD RATE SELECTION

READ/WRITE OPERATIONS

The WD2123 must be initialized after a MASTER RESET pulse by first writing the MODE INSTRUCTION word and then the COMMAND INSTRUCTION word. Thereafter, every control write to the device is interpreted as a COMMAND word. If it is desired to re-program the MODE REGISTER, a COMMAND REGISTER bit, INTERNAL RESET (CR6), allows the next control write data to be entered into the MODE REGISTER.



TYPICAL DATA BLOCK TRANSFER

OPERATING DESCRIPTION

The WD2123 is primarily designed to operate in an 8 bit microprocessor environment, although other control logic schemes are easily implemented. The DATA BUS and the interface control signals ($\overline{CS1}$, $\overline{CS2}$, $\overline{CS3}$, C/$\overline{D}$, $\overline{RE}$, $\overline{WE}$) should be connected to the microprocessor's data bus and system control bus. A 1.8432 MHz crystal should be connected to the WD2123 as shown in figure 5. The appropriate TXC (RXC) clock frequencies should be programmed via system software. Different Baud clock configurations are possible, such as separate transmit and receive frequencies, and are outlined in the general description.

For typical data communication applications, the RXD and TXD input/outputs can be connected to RS-232C interface circuits. Interface control signals, $\overline{CTS}$ and $\overline{RTS}$, are controlled and sensed by the CPU through the COMMAND and STATUS REGISTERS and can be configured in several ways. The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The TXRDY, RXRDY, TXE and BRKDET FLAGS may be connected to the microprocessor system as interrupt inputs or the STATUS REGISTER can be periodically read in a polled environment to support data communication control operations.

The SBRK bit of the COMMAND REGISTER (CR3) is used to send a Break Character. (A Break Character is defined as a start bit, and all zero data, parity and stop bits.) When the CR3 bit is set to a "1", it causes the transmitter output, TXD, to be forced low after the last bit of the last character is transmitted.

The Receiver is equipped with logic to look for a break character. When a break is received, the BREAK DETECT (BRKDET) FLAG and STATUS bit are set to "1". When the receiver input line goes high (V_{IH}) for at least one clock period, the receiver resets the BRKDET FLAG and resumes its search for a start bit.

PROGRAMMING PROCEDURE

The programming sequence of the two channels will be different, depending on whether it is an initialization sequence (that is, one performed right after a hardware master reset occurs) or a re-programming sequence (that is, one performed to change the protocol characteristics (Parity, rate, character length, etc.) after the device has been previously operating in the system). The programming sequence differs, in that, after a master reset, the chip is set to expect the first *control write* operation (C/$\overline{D}$=1) to contain a *mode instruction*. Any *subsequent control write* operations will be transferred to the *command instruction* register.

Now when it is desired to *change* the *mode instruction* register contents, the following re-programming sequence should be performed. A Command Control word of "40" Hex is written to the Chip. This turns off the Receiver and Transmitter and sets the IR (Internal Reset) bit. This bit causes the read/write control logic to expect the *next control write* operation to be a *new mode instruction*. After the new mode instruction is written to the chip, all subsequent control write operations will again be interpreted as *command instructions*. Therefore, after the *new mode instruction* is performed, the next command would turn the receiver and transmitter back on and resume normal Data operations.

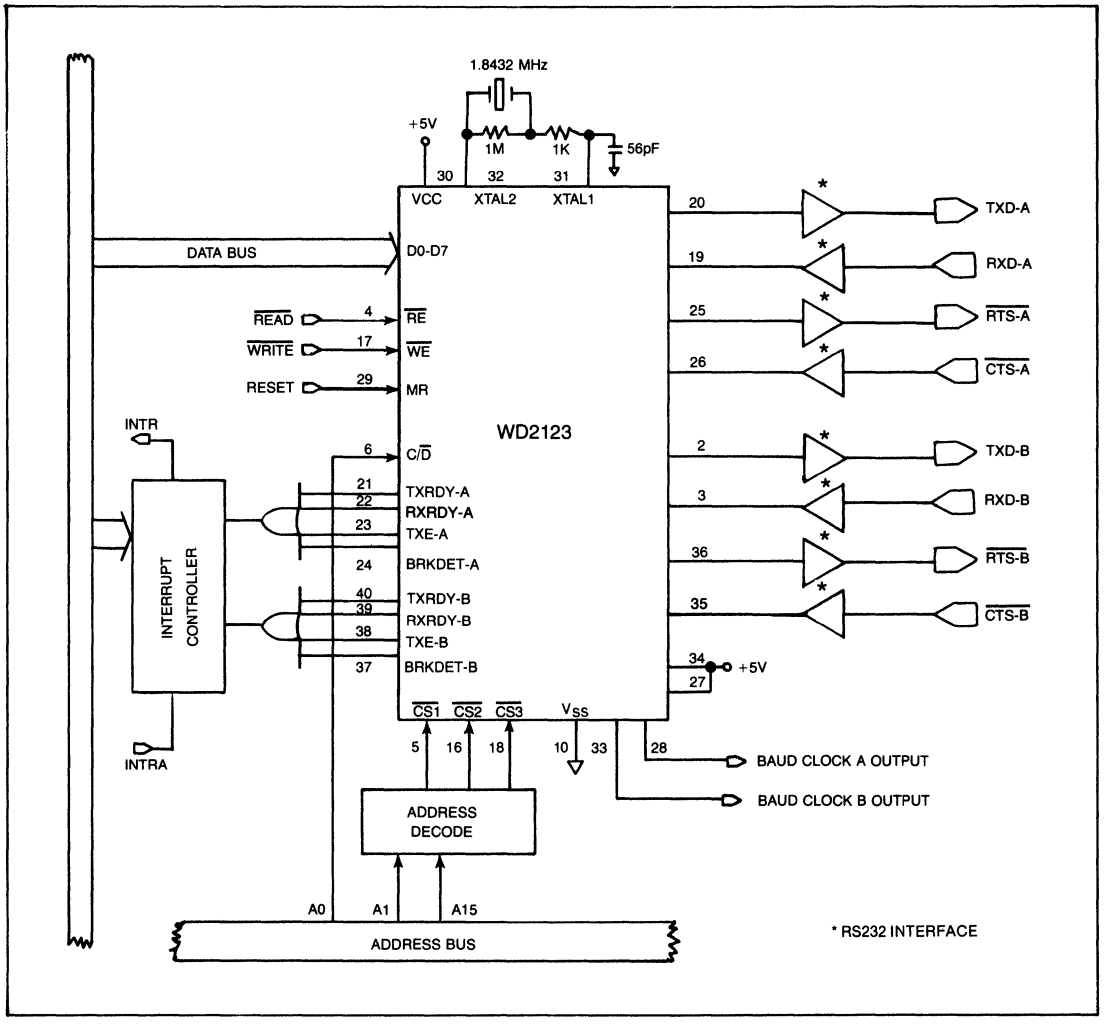


FIGURE 4. WD2123 MICROPROCESSOR APPLICATION

ABSOLUTE MAXIMUM RATINGS

V_{DD} with respect to V_{SS} ..... 0.5V to +12V
Voltage on Any Pin with Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 500 Mw.
Lead Temperature (Soldering 10 sec.) ..... 300°C

STORAGE TEMPERATURE:
Ceramic: —65°C to +150°C
Plastic: —55°C to +125°C

CRYSTAL SPECIFICATIONS:

Temperature range ..... 0°C to +70°C
Series resistance ..... 300Ω to 500Ω
Overall tolerance ..... ±0.01%

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

TABLE 6. DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	—0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6 mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = —100 uA
I_{DL}	Data Bus Leakage (High Impedance State)			—50 10	uA uA	V_{OUT} = 0.45V V_{OUT} = V_{CC}
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		100	125	mA	V_{CC} = 5.25V No Load

TABLE 7. CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND.

AC ELECTRICAL CHARACTERISTICS

TABLE 8. A.C. CHARACTERISTICS

T_A = 0°C to + 70C; V_{CC} = 5.0V ±5%; GND = 0V

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
BUS PARAMETERS Read Cycle					
t_{AR}	Address Stable Before READ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for READ ($\overline{CS}$,C/$\overline{D}$)	50		ns	
t_{RE}	READ Pulse Width	230		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 50 pF
t_{RDH}	READ to Data Floating	25	200	ns	C_L (Max) = 50 pF C_L (Min) = 15 pF
Write Cycle					
t_{AW}	Address Stable Before WRITE	50		ns	
t_{WA}	Address Hold Time for WRITE	50		ns	
t_{WE}	WRITE Pulse Width	230		ns	
t_{DS}	Data Set-Up Time for WRITE	TWE		ns	
t_{WDH}	Data Hold Time for WRITE	100		ns	
OTHER TIMINGS					
t_{TXC}	Transmit Clock Period	1.6		us	
t_{DTX}	TxD Delay from Falling Edge of TxC		1000	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-Up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	200		ns	C_L = 100 pF
f_{TX}	Transmitter Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	 Clock 50% Duty Cycle
t_{TPW}	Transmitter Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TPD}	Transmitter Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	

TABLE 9. A.C. CHARACTERISTICS (CONTINUED)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT	TEST CONDITION
f_{RX}	Receiver Input Clock Frequency 1x Baud Rate 16x and 64x Baud Rate	 DC DC	 500 600	 kHz kHz	Clock 50% Duty Cycle
t_{RPW}	Receiver Input Clock Pulse Width 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{RPD}	Receiver Input Clock Pulse Delay 1x Baud Rate 16x and 64x Baud Rate	 1.0 800		 us ns	
t_{TX}	TxRDY Delay from Center of Stop Bit		8	t_{RXC}	C_L = 50pF (16X)
t_{RX}	RxRDY Delay from Center of Stop Bit		½	t_{RXC}	
t_{IS}	Internal BRKDET Delay from Center of Data Bit		1	RXC	
t_{TRD}	TxRDY Delay from Falling Edge of WRITE		450	ns	
t_{TOD}	TXD Output from Falling Edge of WRITE		1½	t_{TXC}	
t_{WC}	Control Delay from Rising Edge of WRITE ($\overline{RTS}$)		200	ns	
t_{CR}	Control to READ Set-Up Time ($\overline{CTS}$)		1	t_{TXC}	
t_{MR}	Master Reset	500		ns	

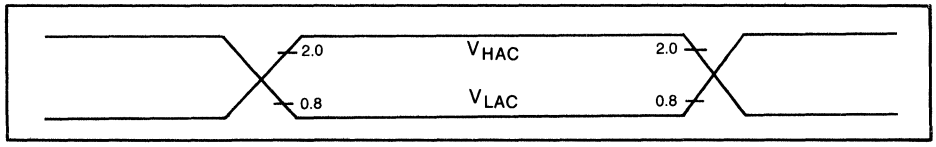


FIGURE 5. A.C. TEST POINTS

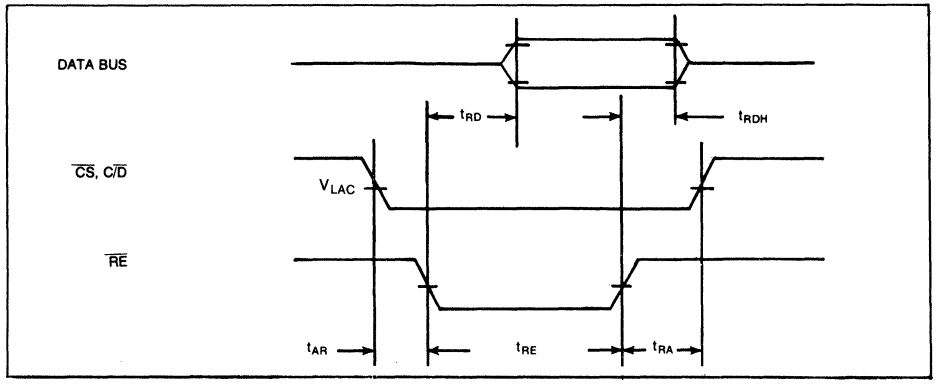


FIGURE 6. READ TIMING

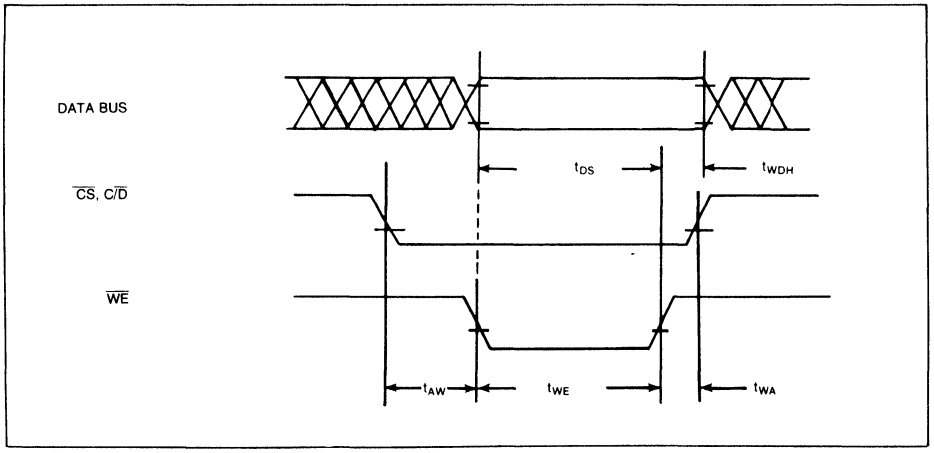


FIGURE 7. WRITE TIMING

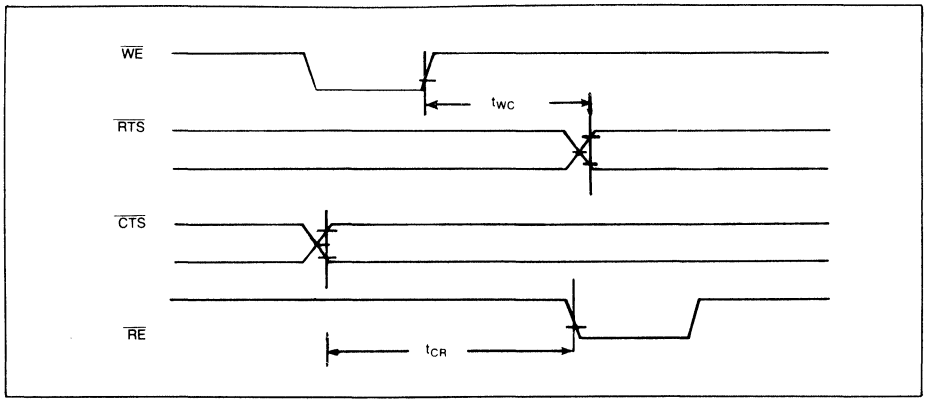


FIGURE 8. INTERFACE CONTROL TIMING

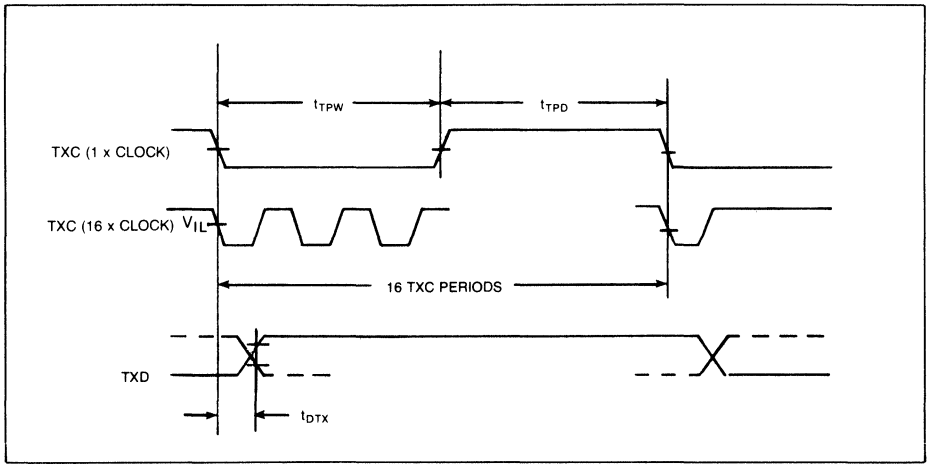


FIGURE 9. TRANSMITTER CLOCK AND DATA TIMING

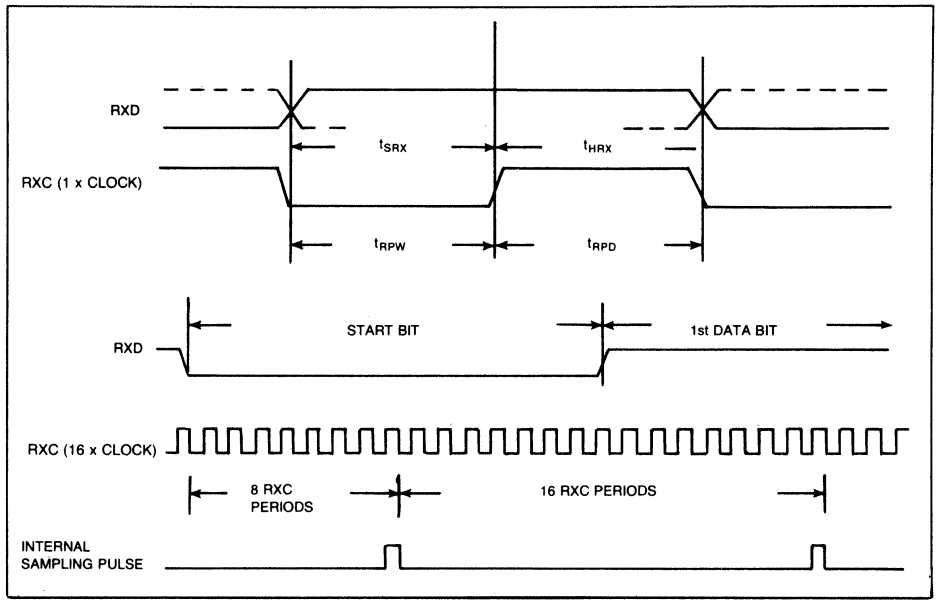


FIGURE 10. RECEIVER CLOCK AND DATA TIMINGS

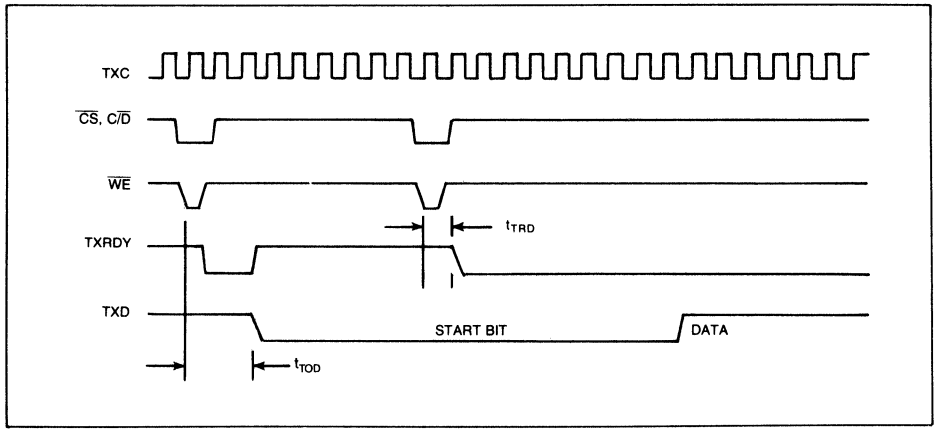


FIGURE 11. TRANSMITTER OUTPUT TIMINGS WITH RESPECT TO TRANSMIT CLOCK

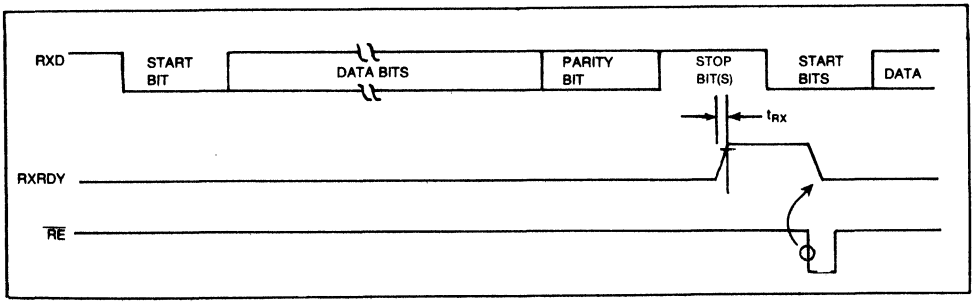


FIGURE 12. RXRDY TIMING

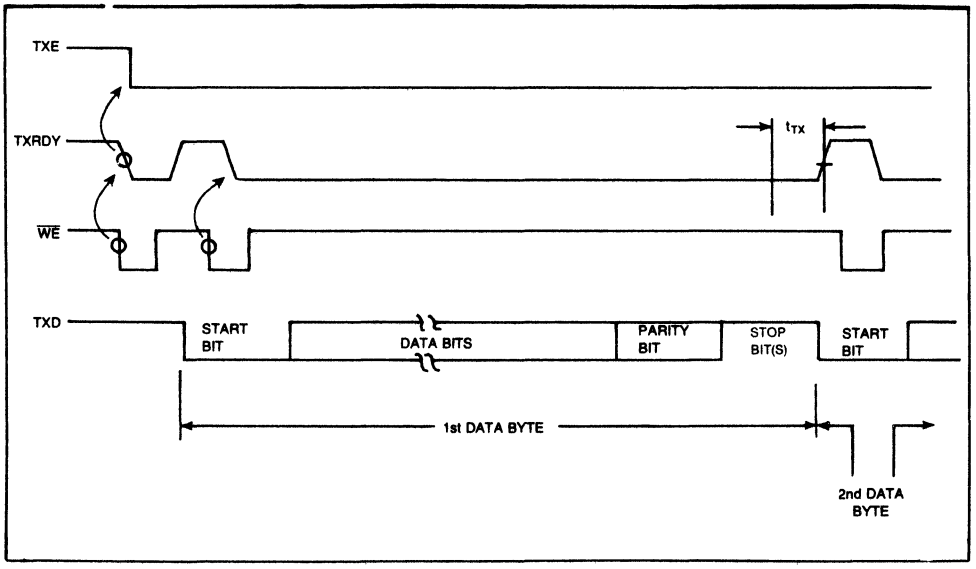


FIGURE 13. TXRDY TIMING

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See page 383 for ordering information.

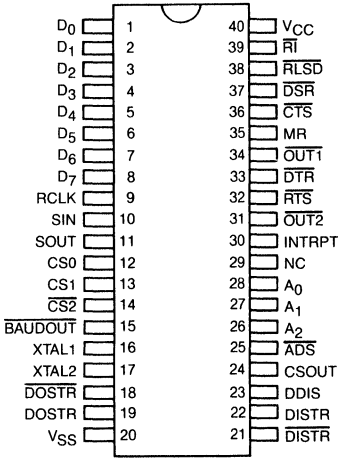
Printed in U.S.A.

FINAL

WD8250 Asynchronous Communications Element

FEATURES

- Designed to be Easily Interfaced to Most Popular Microprocessors (Z-80, 8080A, 6800, etc.)
- Full Double Buffering
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to (2^{16} - 1) and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- Fully Programmable Serial-Interface Characteristics
  - —5-, 6-, 7-, or 8-Bit Characters
  - —Even, Odd, or No-Parity Bit Generation and Detection
  - —1-, 1½-, or 2-Stop Bit Generation
  - —Baud Rate Generation (DC to 56K Baud)
- False Start Bit Detector
- Complete Status Reporting Capabilities
- THREE-STATE TTL Drive Capabilities for Bi-directional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - —Loopback Controls for Communications Link Fault Isolation
  - —Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply



PIN DESIGNATION

DESCRIPTION

The WD8250 is a programmable Asynchronous Communication Element (ACE) in a 40-pin package. The device is fabricated in N/MOS silicon gate technology.

The ACE is a software-oriented device using a three-state 8-bit bi-directional data bus.

The ACE is used to convert parallel data to a serial format on the transmit side, and convert serial data to parallel on the receiver side. The serial format, in order of transmission and reception, is a start bit, followed by five to eight data bits, a parity bit (if programmed) and one, one and one half (five bit format only) or two stop bits. The maximum recommended data rate is 56K baud.

Internal registers enable the user to program various types of interrupts, modem controls, and character formats. The user can read the status of the ACE at any time monitoring word conditions, interrupts and modem status.

An additional feature of the ACE is a programmable baud rate generator that is capable of dividing an internal XTAL or TTL signal clock by a division of 1 to $2^{16} - 1$.

The ACE is designed to work in either a polling or interrupt driven system, which is programmable by users software controlling an internal register.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1 thru 8	D0 thru D7	DATA BUS	3-state input/output lines. Bi-directional communication lines between WD8250 and Data Bus. All assembled data TX and RX, control words, and status information are transferred via the D0-D7 data bus.
9	RCLK	RECEIVE CLK.	This input is the 16X baud rate clock for the receiver section of the chip (may be tied to BAUDOUT pin 15).
10	SIN	SERIAL INPUT	Received Serial Data In from the communications link (Peripheral device, modem or data set).
11	SOUT	SERIAL OUTPUT	Transmitted Serial Data Out to the communication link. The SOUT signal is set to a (logic 1) marking condition upon a MASTER RESET.
12 13 14	CS0 CS1 $\overline{CS2}$	CHIP SELECT CHIP SELECT CHIP SELECT	When CS0 and CS1 are high, and $\overline{CS2}$ is low, chip is selected. Selection is complete when the address strobe $\overline{ADS}$ latches the chip select signals.
15	$\overline{BAUDOUT}$	$\overline{BAUDOUT}$	16X clock signal for the transmitter section of the WD8250. The clock rate is equal to the oscillator frequency divided by the divisor loaded into the divisor latches. The BAUDOUT signal may be used to clock the receiver by tying to (pin 9) RCLK.
16 17	XTAL 1 XTAL 2	EXTERNAL CLOCK IN EXTERNAL CLOCK OUT	These pins connect the crystal or signal clock to the WD8250 baud rate divisor circuit. See Fig. 3 and Fig. 4 for circuit connection diagrams.
18 19	$\overline{DOSTR}$ DOSTR	$\overline{DATA\ OUT\ STROBE}$ DATA OUT STROBE	When the chip has been selected, a low $\overline{DOSTR}$ or high DOSTR will latch data into the selected WD8250 register (a CPU write). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DOSTR}$ — high or DOSTR — low.
20	V_{SS}	GROUND	System signal ground.
21 22	$\overline{DISTR}$ DISTR	$\overline{DATA\ IN\ STROBE}$ DATA IN STROBE	When chip has been selected, a low $\overline{DISTR}$ or high DISTR will allow a read of the selected WD8250 register (a CPU read). Only one of these lines need be used. Tie unused line to its inactive state. $\overline{DISTR}$ — high or DISTR — low.
23	DDIS	DRIVER DISABLE	Output goes low whenever data is being read from the WD8250. Can be used to reverse data direction of external transceiver.
24	CSOUT	CHIP SELECT OUT	Output goes high when chip is selected. No data transfer can be initiated until CSOUT is high.
25	$\overline{ADS}$	$\overline{ADDRESS\ STROBE}$	When low, provides latching for Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) NOTE: The rising edge (↑) of the $\overline{ADS}$ signal is required when the Register Select (A0, A1, A2) and the Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If not required, the $\overline{ADS}$ input can be tied permanently low.

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
26 27 28	A2 A1 A0	REGISTER SELECT A2 REGISTER SELECT A1 REGISTER SELECT A0	These three inputs are used to select a WD8250 internal register during a data read or write. See Table below.
29	NC	NO CONNECT	No Connect
30	INTRPT	INTERRUPT	Output goes high whenever an enabled interrupt is pending.
31	$\overline{OUT2}$	$\overline{OUTPUT\ 2}$	User-designated output that can be programmed by Bit 3 of the modem control register = 1, causes $\overline{OUT2}$ to go low.
32	$\overline{RTS}$	$\overline{REQUEST\ TO\ SEND}$	Output when low informs the modem or data set that the WD8250 is ready to transmit data. See Modem Control Register.
33	$\overline{DTR}$	$\overline{DATA\ TERMINAL\ READY}$	Output when low informs the modem or data set that the WD8250 is ready to receive.
34	$\overline{OUT1}$	$\overline{OUTPUT\ 1}$	User designated output can be programmed by Bit 2 of Modem Control Register = 1 causes $\overline{OUT1}$ to go low.
35	MR	MASTER RESET	When high clears the registers to states as indicated in Table 1.
36	$\overline{CTS}$	$\overline{CLEAR\ TO\ SEND}$	Input from DCE indicating remote device is ready to transmit. See Modem Status Register.
37	$\overline{DSR}$	$\overline{DATA\ SET\ READY}$	Input from DCE used to indicate the status of the local data set. See Modem Status Register.
38	$\overline{RSLD}$	$\overline{RECEIVED\ LINE\ SIGNAL\ DETECT}$	Input from DCE indicating that it is receiving a signal which meets its signal quality conditions. See Modem Status Register.
39	$\overline{RI}$	$\overline{RING\ INDICATOR}$	Input, when low, indicates that a ringing signal is being received by the modem or data set. See Modem Status Register.
40	V_{CC}	+5V	+5 Volt Supply.

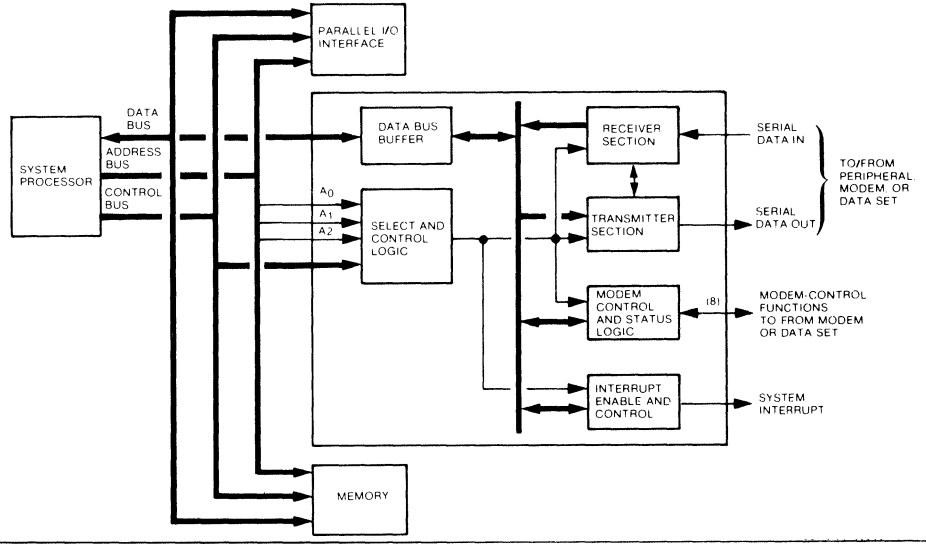


FIGURE 1. WD8250 GENERAL SYSTEM CONFIGURATION

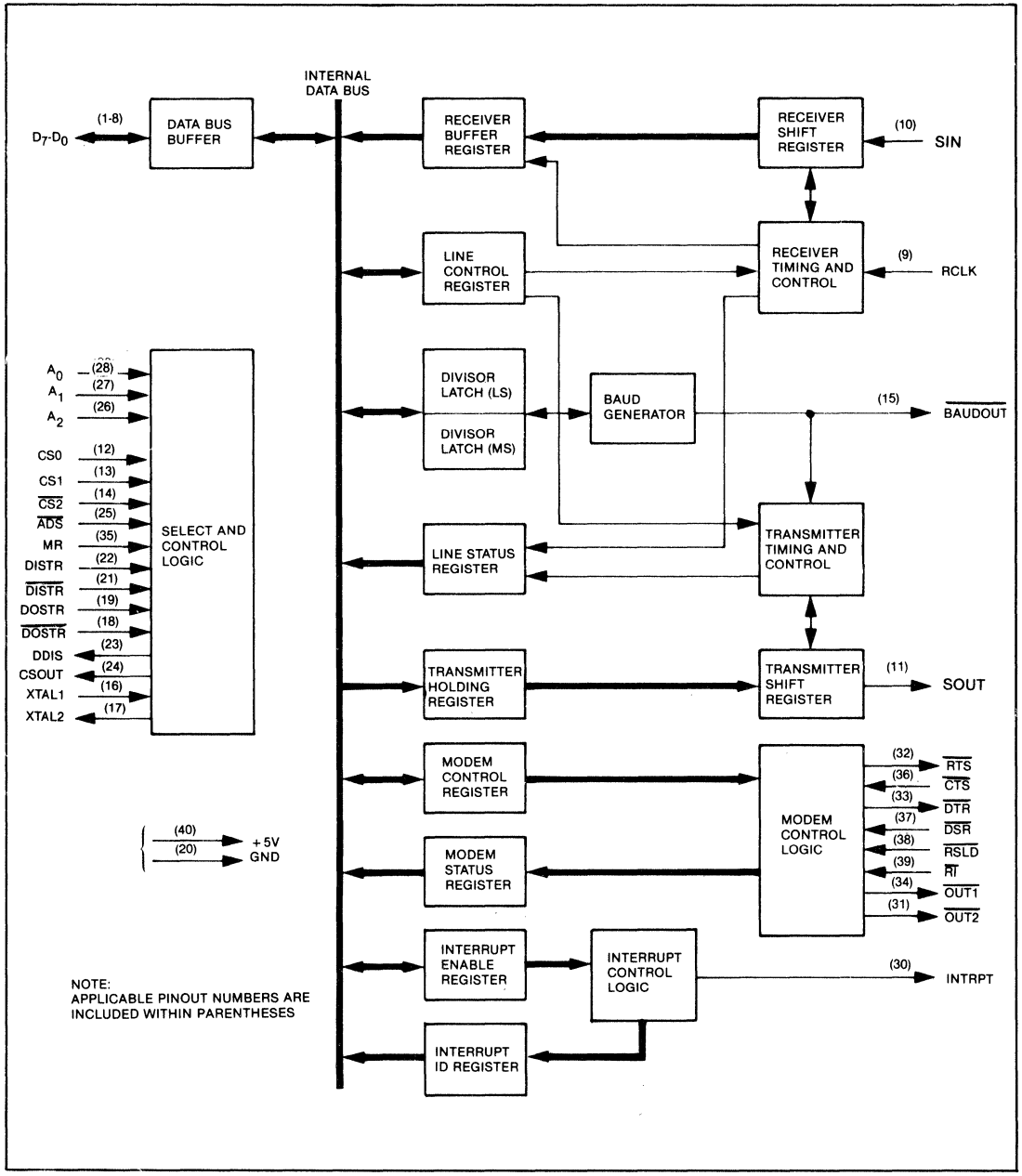


FIGURE 2. WD8250 BLOCK DIAGRAM

CHIP SELECTION AND REGISTER ADDRESSING

Address Strobe ($\overline{ADS}$ pin 25): When low provides latching for register select (A0, A1, A2) and chip select (CS0, CS1, $\overline{CS2}$).

NOTE: The rising edge (↑) of the $\overline{ADS}$ input is required when Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals are not stable for the duration of a read or write operation. If $\overline{ADS}$ is not required for latching, this input can be tied permanently low.

Chip Select (CS0, CS1, $\overline{CS2}$) pins 12-14: The definition of chip selected is CS0, CS1 both high and $\overline{CS2}$ is low. Chip selection is complete when latched by $\overline{ADS}$ or $\overline{ADS}$ is tied low.

Register Select (A0, A1, A2) pins 26-28: To select a register for read or write operation, see Register Table.

NOTE: (DLAB) Divisor Latch access bit is the MSB of the Line Control Register. DLAB must be programmed high logic 1 by the system software to access the Baud Rate Generator Divisor Latches.

DLAB	A2	A1	A0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

WD8250 OPERATIONAL DESCRIPTION

Master Reset

A high-level input on pin 35 causes the WD8250 to reset to the condition listed in Table 1.

WD8250 Accessible Registers

The system programmer has access to any of the registers summarized in Table 2. For individual register descriptions, refer to the following pages under register heading.

TABLE 1. RESET CONTROL OF REGISTERS AND PINOUT SIGNALS

Register/Signal	Reset Control	Reset State
Receiver Buffer Register	First Word Received	Data
Transmitter Holding Register	Writing into the Transmitter Holding Register	Data
Interrupt Enable Register	Master Reset	All Bits Low (0-3 forced and 4-7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High and Bits 1-7 Are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 and 6 Are High
Modem Status Register	Master Reset MODEM Signal Inputs	Bits 0-3 Low Bits 4-7 — Input Signal
Divisor Latch (low order bits)	Writing into the Latch	Data
Divisor Latch (high order bits)	Writing into the Latch	Data
SOUT	Master Reset	High
$\overline{BAUDOUT}$	Writing into either Divisor Latch	Low
CSOUT	$\overline{ADS}$ Strobe Signal and State of Chip Select Lines	High/Low
DDIS	DDIS = $\overline{CSOUT \cdot RCLK \cdot DISTR}$ (At Master Reset, the CPU sets RCLK and DISTR low.)	High
INTRPT	Master Reset	Low
$\overline{OUT\ 2}$	Master Reset	High
$\overline{RTS}$	Master Reset	High
$\overline{DTR}$	Master Reset	High
$\overline{OUT\ 1}$	Master Reset	High
D7-D0 Data Bus Lines	In THREE-STATE Mode, Unless CSOUT • DISTR = High or CSOUT • DOSTR = High	THREE-STATE Data (ACE to CPU) Data (CPU to ACE)

TABLE 2. SUMMARY OF WD8250 ACCESSIBLE REGISTERS

	Register Address									
	0 DLAB=0	0 DLAB=0	1DLAB=0	2	3	4	5	6	0DLAB 1	1DLAB=1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
0	Data Bit 0*	**Data Bit 0***	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DSLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Line Control Register

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver in the opposite state indicated by bit 4.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there (until reset by a low-level bit 6) regardless of other transmitter activity. The feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

WD8250 Programmable Baud Rate Generator

The WD8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to (2^{16} - 1). The output frequency of the Baud Generator is 16x the Baud rate. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Generator with two different driving frequencies. One is referenced to a 1.8432 MHz crystal. The other is a 3.072 MHz crystal.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 6 and below, the maximum frequency is equal to 1/2 the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1/2 MHz. In no case should the data rate be greater than 56K Baud.

Line Status Register

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of

TABLE 3. BAUD RATES USING 1.8432 MHz CRYSTAL.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.5	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

TABLE 4. BAUD RATES USING 3.072 MHz CRYSTAL.

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired and Actual
50	3840	—
75	2560	—
110	1745	0.026
134.5	1428	0.034
150	1280	—
300	640	—
600	320	—
1200	160	—
1800	107	—
2000	96	—
2400	80	—
3600	53	0.628
4800	40	—
7200	27	1.23
9600	20	—
19200	10	—
38400	5	—
56000	3	14.285

the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 will be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (Logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the WD8250 is ready to accept a new character for transmission. In addition, this bit causes the WD8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

Interrupt Identification Register

The WD8250 has an on chip interrupt capability that allows for complete flexibility in interfacing to all popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the WD8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and source of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register

This 8-bit register enables the four interrupt sources of the WD8250 to separately activate the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to a logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

TABLE 5. INTERRUPT CONTROL FUNCTIONS.

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Flag	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the WD8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the WD8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to a logic one (high) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control Inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the WD8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The WD8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register

and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal WD8250 operation. To return to this operation, the registers must be reprogrammed for normal operation and then bit 4 must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM Status Register

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input.

Typical Applications

Figures 3 and 4 show how to use the WD8250 chip in an 8080A system and in a microcomputer system with a high-capacity data bus.

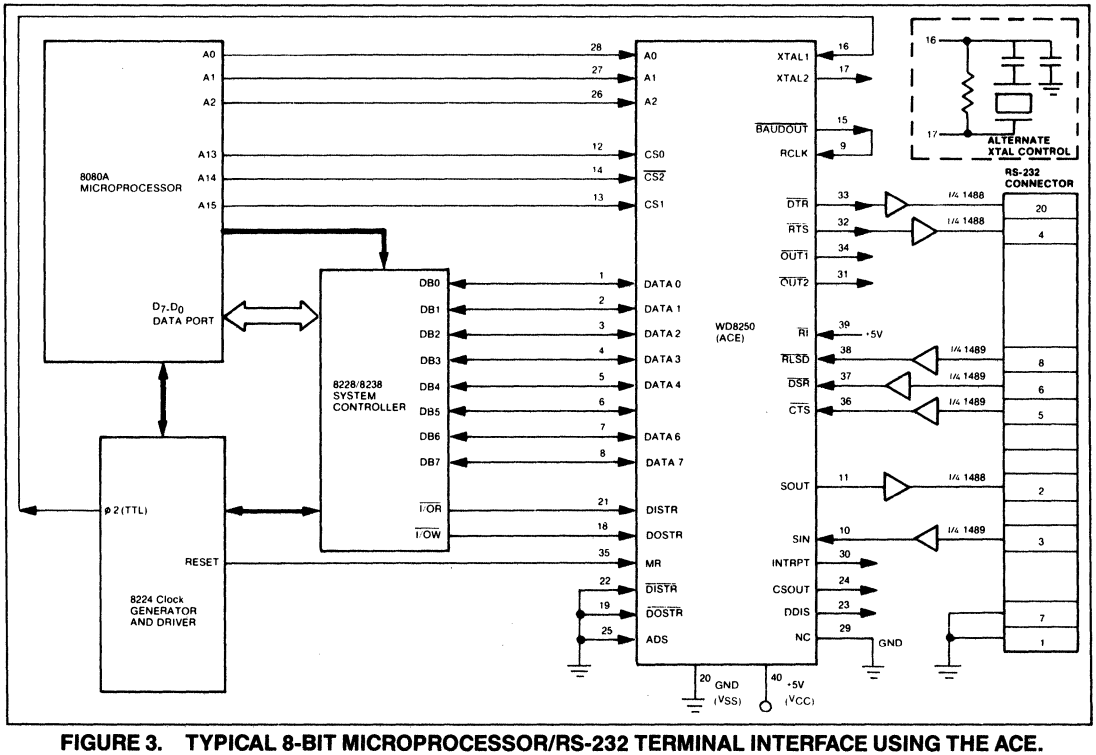


FIGURE 3. TYPICAL 8-BIT MICROPROCESSOR/RS-232 TERMINAL INTERFACE USING THE ACE.

Typical Applications (continued)

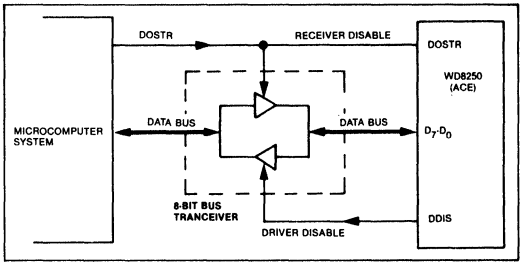


FIGURE 4. TYPICAL INTERFACE FOR A HIGH-CAPACITY DATA BUS.

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias ..... 0°C to +70°C
Storage Temperature -65°C to +150°C (Ceramic)
-50°C to +125°C (Plastic)
All Input or Output Voltages with
Respect to V_{SS} ..... -0.5 V to +7.0 V
Power Dissipation ..... 750 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

TABLE 6. DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = 0V, unless otherwise specified.

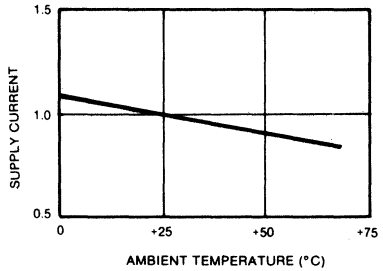
SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_{ILX}	Clock Input Low Voltage	-0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.4		V_{CC}	V	
V_{IL}	Input Low Voltage	-0.5		0.8	V	
V_{IH}	Input High Voltage	2.4		V_{CC}	V	
V_{OL}	Output Low Voltage			.45	V	I_{OL}=1.6mA on all outputs
V_{OH}	Output High Voltage	2.4			V	I_{OH}=-100 μA
$I_{CC(AV)}$	Avg Power Supply Current (V_{CC})			150	ma	
I_{IL}	Input Leakage			± 10	μA	
I_{CL}	Clock Leakage			± 10	μA	
I_{DL}	Data Bus Leakage			± 10	μA	V_{OUT} = 0.4V, V_{OUT} = 4.6V: Data Bus is at High-Impedance State

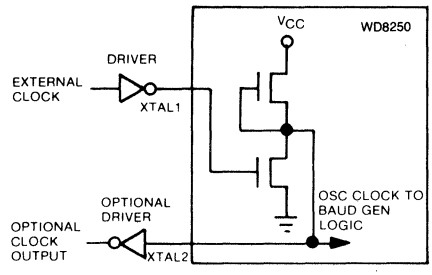
TABLE 7. CAPACITANCE

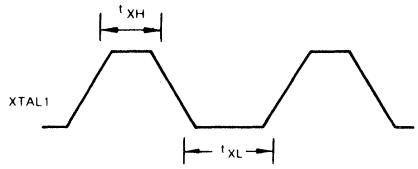
T_A = 25°C, V_{CC} = V_{SS} = 0V

SYMBOL	CHARACTERISTIC	TYP.	MAX.	UNITS	TEST CONDITIONS
C_{XIN}	Clock Capacitance	10	15	pF	fc=1 MHz, Unmeasured pins returned to V_{SS}
C_{IN}	Input Capacitance	6	10	pF	
C_{OUT}	Output Capacitance	10	20	pF	

Typical Supply Current vs. Temperature, Normalized

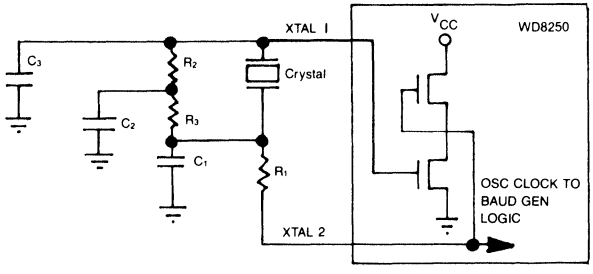






Timing	Min	Units
t_{XH}	100	ns
t_{XL}	115	ns

FIGURE 5. EXTERNAL CLOCK INPUT (3.1 MHz MAX.)



Crystal	R_1	R_2	R_3	C_1	C_2	C_3
3.1 MHz	2K	0.5M	0.5M	40-60pF	0.01μF	10-30pF
1.8 MHz	2K	0.5M	0.5M	65-100pF	0.01μF	10-15pF

FIGURE 6. TYPICAL CRYSTAL OSCILLATOR NETWORK

AC ELECTRICAL CHARACTERISTIC

TA = 0°C to +70°C, V_{CC} = +5V ± 5%

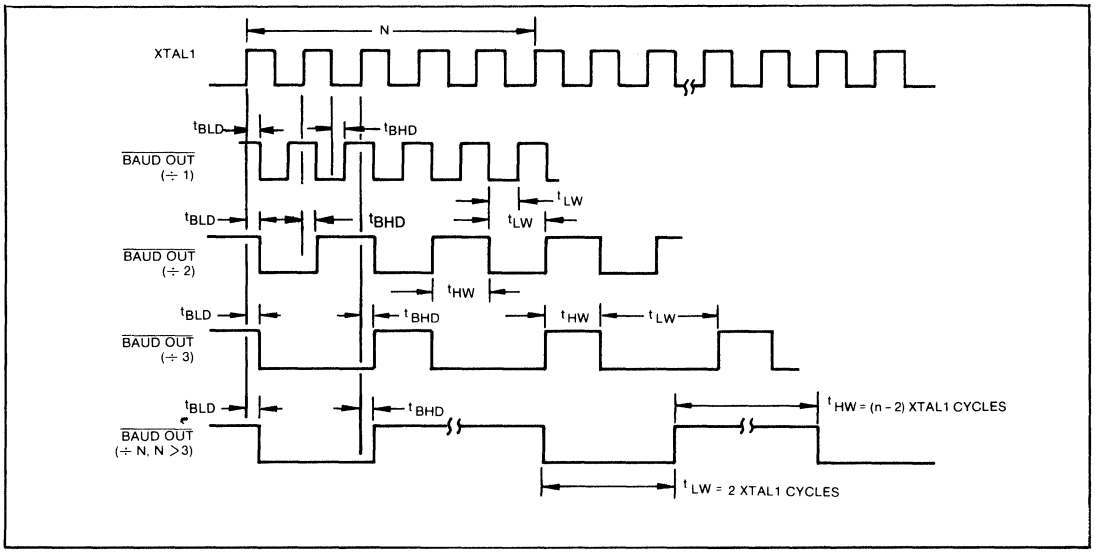
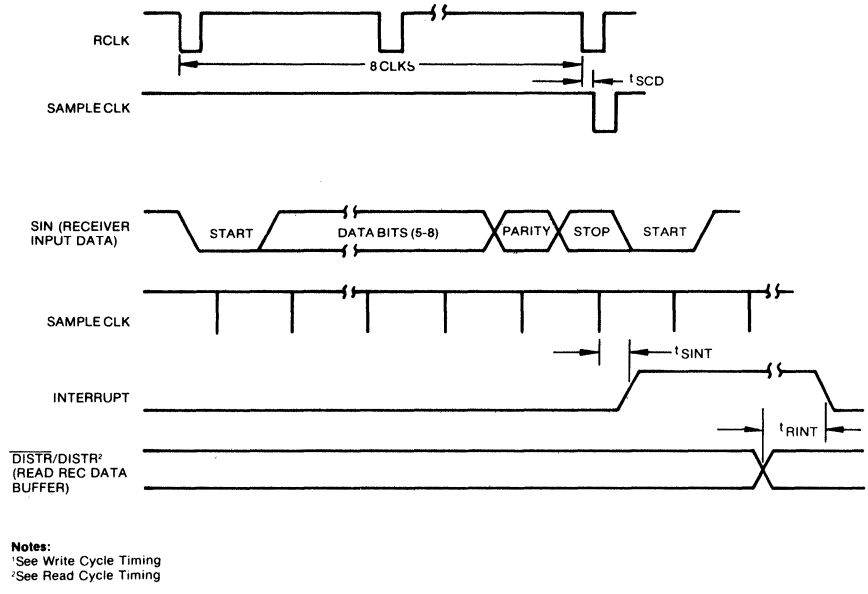


FIGURE 7. BAUDOUT TIMING

TABLE 8. BAUD GENERATOR

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	TEST CONDITIONS
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250	ns	100pF Load
t_{BHD}	Baud Output Positive Edge Delay		250	ns	100pF Load
t_{LW}	Baud Output Down Time	425		ns	100pF Load
t_{HW}	Baud Output Up Time	330		ns	100pF Load

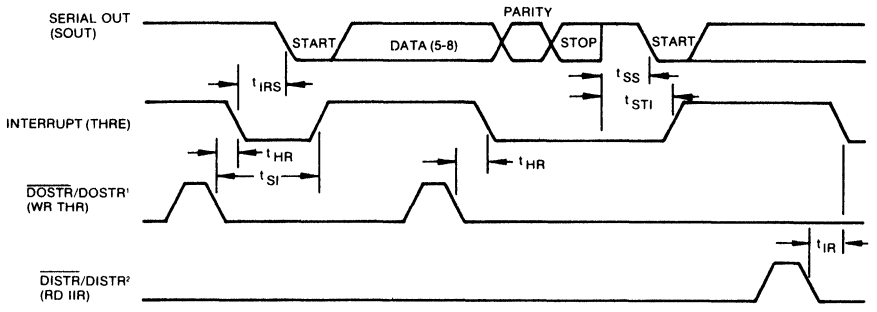


Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 8. RECEIVER TIMING

TABLE 9. RECEIVER TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{SCD}	Delay from RCLK to Sample Time		2	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2	μs	100pF Load
t_{RINT}	Delay from $\overline{DISTR}$/DISTR (RD RBR) to Reset Interrupt	.250	1	μs	100pF Load



Notes:
[1]See Write Cycle Timing
[2]See Read Cycle Timing

FIGURE 9. TRANSMITTER TIMING

TABLE 10. TRANSMITTER TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{HR}	Delay from $\overline{DOSTR}$/DOSTR (WR THR) to Reset Interrupt	.250	1	μs	100pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16	$\overline{BAUDOUT}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24	$\overline{BAUDOUT}$ Cycles	
t_{SS}	Delay from Stop to Next Start	.250	1	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8	$\overline{BAUDOUT}$ Cycles	
TIR	Delay from $\overline{DISTR}$/DISTR (RD IIR) to Reset Interrupt (THRE)	.250	1	μs	100pF Load

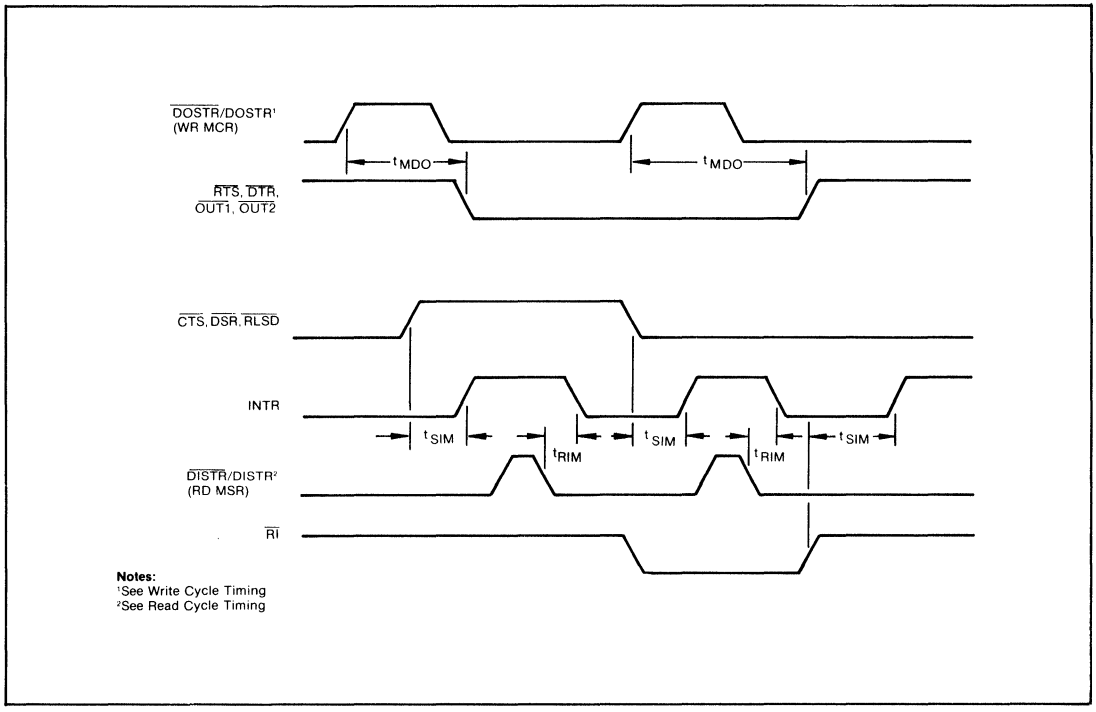


FIGURE 10. MODEM CONTROLS TIMING

TABLE 11. MODEM CONTROL TIMING

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNITS	TEST CONDITIONS
t_{MDO}	Delay from DOSTR/$\overline{\text{DOSTR}}$ (WR MCR) to Output	.250	1	μs	100pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input	.250	1	μs	100pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{\text{DISTR}}$/DISTR (RD MSR)	.250	1	μs	100pF Load

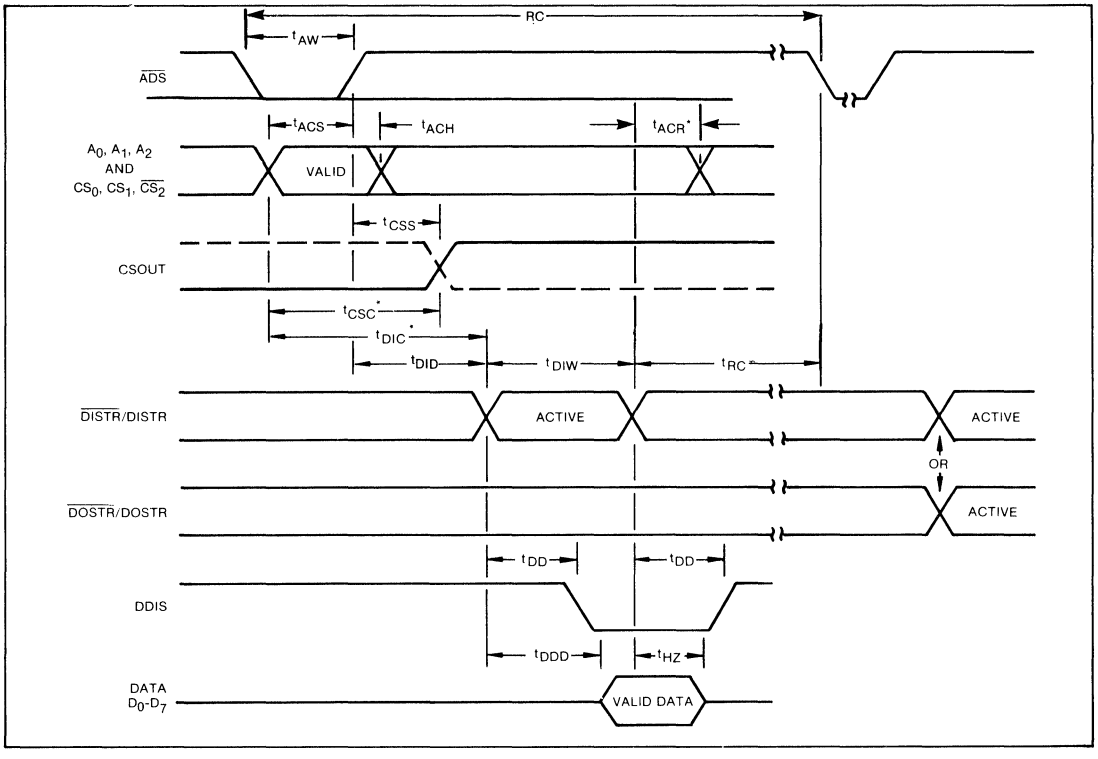


FIGURE 11. READ CYCLE TIMING

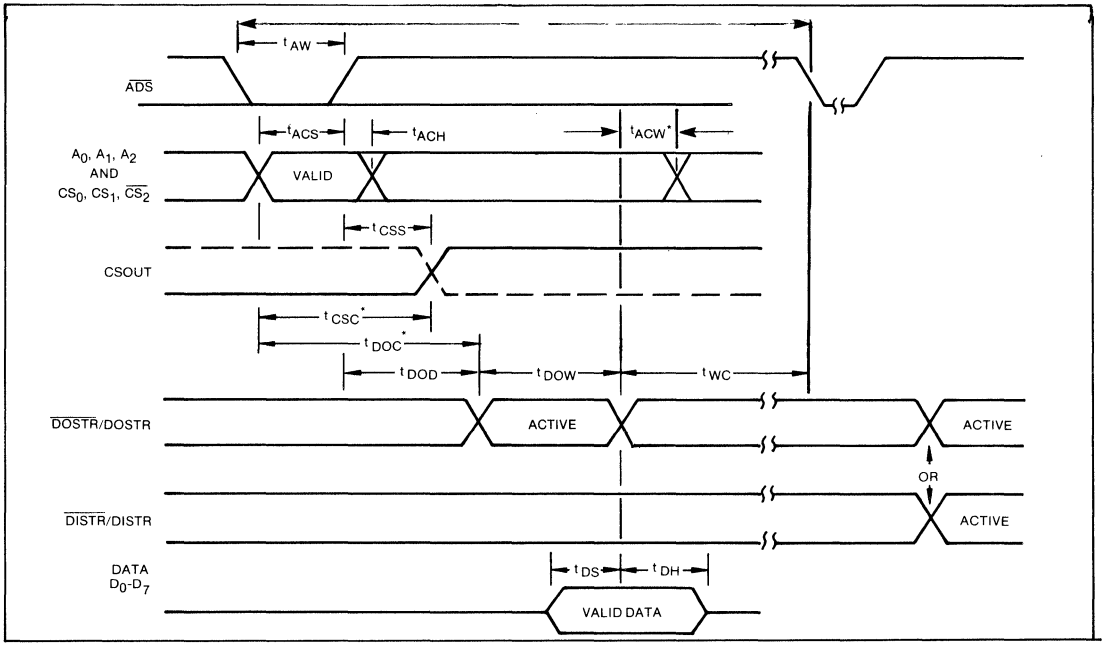


FIGURE 12. WRITE CYCLE TIMING

TABLE 12. READ/WRITE CYCLE TIMING

SYMBOL	PARAMETER	UNITS	MIN.	MAX.	TEST CONDITIONS
t_{AW}	Address Strobe Width	ns	120		1TTL Load
t_{ACS}	Address and Chip Select Setup Time	ns	100		1TTL Load
t_{ACH}	Address and Chip Select Hold Time	ns	10		1TTL Load
t_{CSS}	CSOUT Delay from Latch	ns		160	1TTL Load
t_{DID}	$\overline{DISTR}$/DISTR Delay from Latch	ns	50		1TTL Load
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	ns	300		1TTL Load
t_{RC}	Read Cycle Delay	ns	655		1TTL Load
RC	Read Cycle = $t_{ACS} + t_{DID} + t_{DIW} + t_{RC} + 20$ ns	ns	1125		1TTL Load
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	ns		200	1TTL Load
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	ns		300	1TTL Load
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	ns	60		1TTL Load
t_{DOD}	$\overline{DOSTR}$/DOSTR Delay From Latch	ns	20		1TTL Load
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	ns	175		1TTL Load
t_{WC}	Write Cycle Delay	ns	685		1TTL Load
WC	Write Cycle = $t_{ACS} + t_{DOD} + t_{DOW} + t_{WC} + 20$ ns	ns	1000		1TTL Load
t_{DS}	Data Setup Time	ns	175		1TTL Load
t_{DH}	Data Hold Time	ns	60		1TTL Load
t_{CSC}*	CSOUT Delay from Select	ns		260	1TTL Load
t_{DIC}*	$\overline{DISTR}$/DISTR Delay from Select	ns	150		1TTL Load
t_{DOC}*	$\overline{DOSTR}$/DOSTR Delay from Select	ns	150		1TTL Load
t_{ACR}*	Address and Chip Select Hold Time from $\overline{DISTR}$/DISTR	ns	10		1TTL Load
t_{ACW}*	Address and Chip Select Hold Time fom $\overline{DOSTR}$/DOSTR	ns	10		1TTL Load
t_{MR}	Master Reset Pulse Width	ns	500		1TTL Load

*Only applicable when ADS is permanently low.

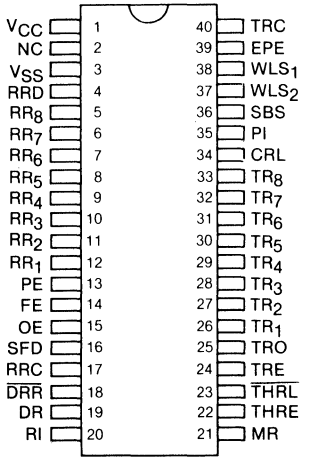
See page 383 for ordering information.

FINAL

TR1863/TR1865
Universal Asynchronous Receiver/Transmitter (UART)

FEATURES

- SINGLE POWER SUPPLY — +5VDC
- D.C. TO 1 MHZ (64 KB) (STANDARD PART) TR1863/5
- FULL DUPLEX OR HALF DUPLEX OPERATION
- AUTOMATIC INTERNAL SYNCHRONIZATION OF DATA AND CLOCK
- AUTOMATIC START BIT GENERATION
- EXTERNALLY SELECTABLE
  Word Length
  Baud Rate
  Even/Odd Parity (Receiver/Verification — Transmitter/Generation)
  Parity Inhibit
  One, One and One-Half, or Two Stop Bit Generation (1½ at 5 Bit Level)
- AUTOMATIC DATA RECEIVED/TRANSMITTED STATUS GENERATION
  Transmission Complete
  Buffer Register Transfer Complete
  Received Data Available
  Parity Error
  Framing Error
  Overrun Error
- BUFFERED RECEIVER AND TRANSMITTER REGISTERS
- THREE-STATE OUTPUTS
  Receiver Register Outputs
  Status Flags
- TTL COMPATIBLE
- TR1865 HAS PULL-UP RESISTORS ON ALL INPUTS



PIN DESIGNATION

APPLICATIONS

- PERIPHERALS
- TERMINALS
- MINI COMPUTERS
- FACSIMILE TRANSMISSION
- MODEMS
- CONCENTRATORS
- ASYNCHRONOUS DATA MULTIPLEXERS
- CARD AND TAPE READERS
- PRINTERS
- DATA SETS
- CONTROLLERS
- KEYBOARD ENCODERS
- REMOTE DATA ACQUISITION SYSTEMS
- ASYNCHRONOUS DATA CASSETTES

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UART) is a general purpose, programmable or hardwired MOS/LSI device. The UART is used to convert parallel data to a serial data format on the transmit side, and converts a serial data format to parallel data on the receive side.

The serial format in order of transmission and reception is a start bit, followed by five to eight data bits, a parity bit (if selected) and one, one and one-half, or two stop bits.

Three types of error conditions are available on each received character: parity error, framing error (no valid stop bit) and overrun error.

The transmitter and receiver operate on external 16X clocks, where 16 clock times are equal to one bit time. The receiver clock is also used to sample in the center of the serial data bits to allow for line distortion.

Both transmitter and receiver are double buffered allowing a one character time maximum between a data read or write. Independent handshake lines for receiver and transmitter are also included. All inputs and outputs are TTL compatible with three-state outputs available on the receiver, and error flags for bussing multiple devices.

PIN DESCRIPTION

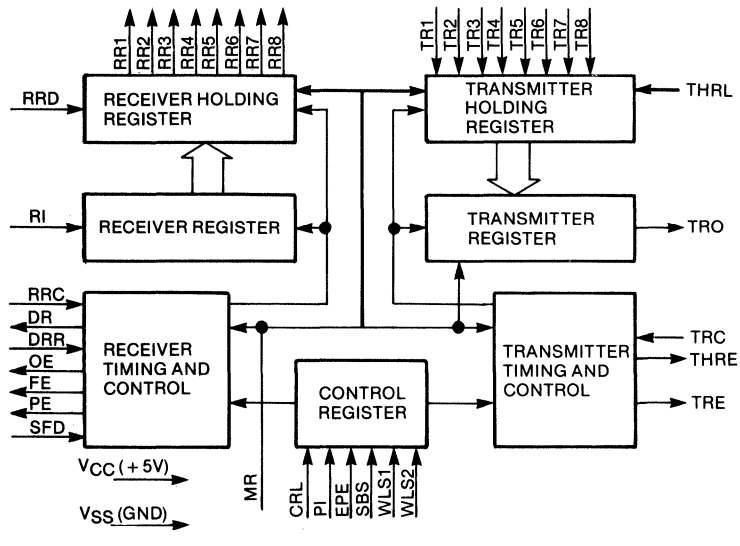
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
1	V_{CC}	POWER SUPPLY	+5 volts supply
2	NC	NC	No Internal Connection
3	V_{SS}	GROUND	Ground = 0V
4	RRD	RECEIVER REGISTER DISCONNECT	A high level input voltage, V_{IH}, applied to this line disconnects the RECEIVER HOLDING REGISTER outputs from the RR_{1-8} data outputs (pins 5-12).
5-12	RR_8-RR_1	RECEIVER HOLDING REGISTER DATA	The parallel contents of the RECEIVER HOLDING REGISTER appear on these lines if a low-level input voltage, V_{IL}, is applied to RRD. For character formats of fewer than eight bits received characters are right-justified with RR1 (pin 12) as the least significant bit and the truncated bits are forced to a low level output voltage, V_{OL}.
13	PE	PARITY ERROR	A high level output voltage, V_{OH}, on this line indicates that the received parity differ from that which is programmed by the EVEN PARITY ENABLE (pin 39) and the PARITY INHIBIT (pin 35) control lines. This output is updated each time a character is transferred to the RECEIVER HOLDING REGISTER. PE lines from a number of arrays can be bussed together since an output disconnect capability is provided by Status Flag Disconnect line (pin 16).
14	FE	FRAMING ERROR	A high-level output voltage, V_{OH}, on this line indicates that the received character has no valid stop bit, i.e., the bit (if programmed) is not a high level voltage. This output is updated each time a character is transferred to the Receiver Holding Register, FE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
15	OE	OVERRUN ERROR	A high-level output voltage, V_{OH}, on this line indicates that the Data Received Flag (pin 19) was not reset before the next character was transferred to the Receiver Holding Register. OE lines from a number of arrays can be bussed together since an output disconnect capability is provided by the Status Flag Disconnect line (pin 16).
16	SFD	STATUS FLAGS DISCONNECT	A high-level input voltage, V_{IH}, applied to this pin disconnects the PE, FE, OE, DR and THRE allowing them to be buss connected.
17	RRC	RECEIVER REGISTER CLOCK	The receiver clock frequency is sixteen (16) times the desired receiver shift rate.
18	$\overline{DRR}$	$\overline{DATA\ RECEIVED\ RESET}$	A low-level input voltage, V_{IL}, applied to this line resets the DR line.
19	DR	DATA RECEIVED	A high-level output voltage, V_{OH}, indicates that an entire character has been received and transferred to the RECEIVER HOLDING REGISTER.

PIN DESCRIPTION

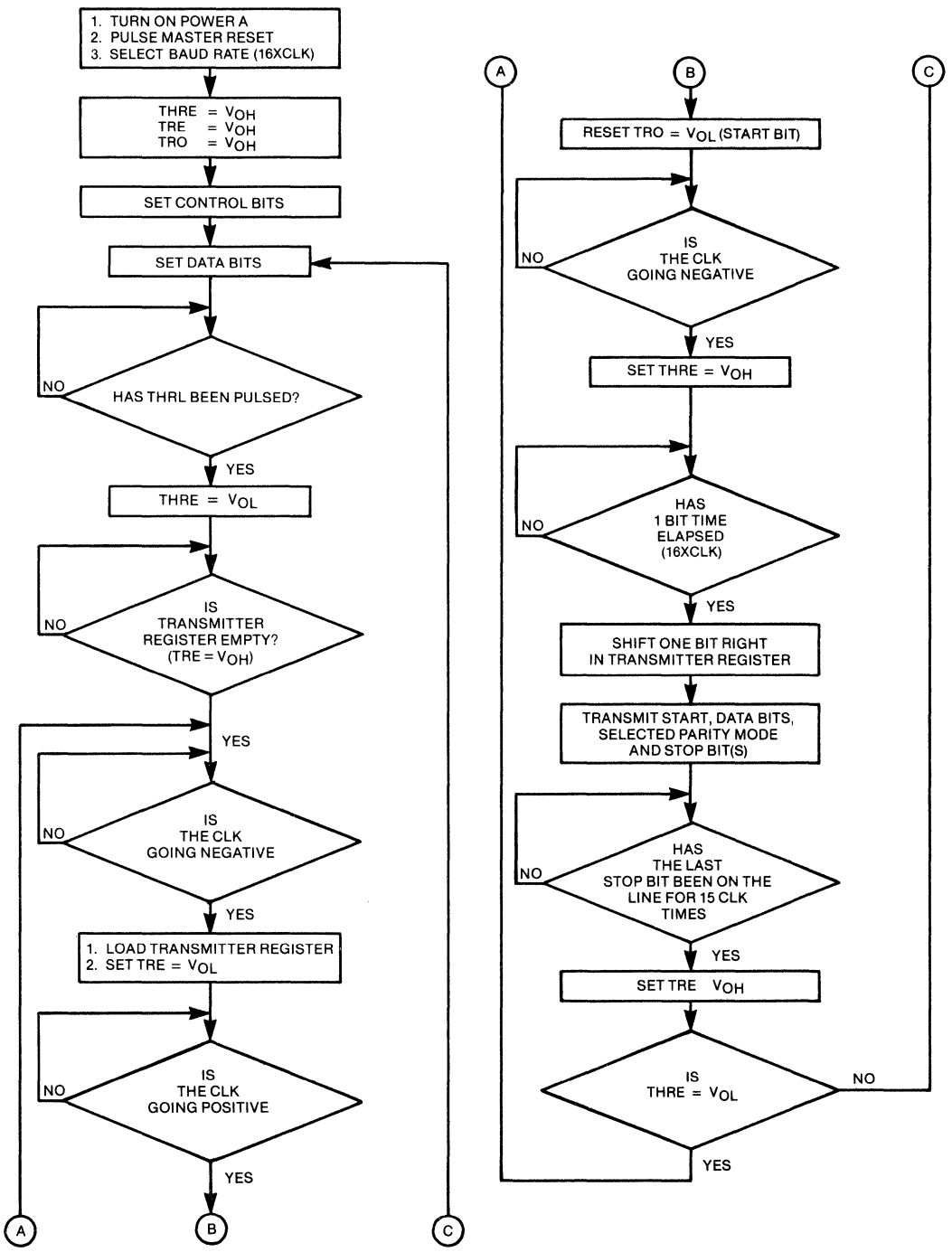
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
20	RI	RECEIVER INPUT	Serial input data. A high-level input voltage, V_{IH}, must be present when data is not being received.
21	MR	MASTER RESET	This line is strobed to a high-level input voltage, V_{IH}, to clear the logic. It resets the TRANSMITTER and RECEIVER HOLDING REGISTERS, the TRANSMITTER REGISTER, FE, OE, PE, DR and sets TRO, THRE, and TRE to a high-level output voltage, V_{OH}.
22	THRE	TRANSMITTER HOLDING REGISTER EMPTY	A high-level output voltage, V_{OH}, on this line indicates the TRANSMITTER HOLDING REGISTER has transferred its contents to the TRANSMITTER REGISTER and may be loaded with a new character.
23	$\overline{\text{THRL}}$	$\overline{\text{TRANSMITTER HOLDING REGISTER LOAD}}$	A low-level input voltage, V_{IL}, applied to this line enters a character into the TRANSMITTER HOLDING REGISTER. A transition from a low-level input voltage, V_{IL}, to a high-level input voltage, V_{IH}, transfers the character into the TRANSMITTER REGISTER if it is not in the process of transmitting a character. If a character is being transmitted, the transfer is delayed until its transmission is completed. Upon completion, the new character is automatically transferred simultaneously with the initiation of the serial transmission of the new character.
24	TRE	TRANSMITTER REGISTER EMPTY	A high-level output voltage, V_{OH}, on this line indicates that the TRANSMITTER REGISTER has completed serial transmission of a full character including STOP bit(s). It remains at this level until the start of transmission of the next character.
25	TRO	TRANSMITTER REGISTER OUTPUT	The contents of the TRANSMITTER REGISTER (START bit, DATA bits, PARITY bit, and STOP bits) are serially shifted out on this line. When no data is being transmitted, this line will remain at a high-level output voltage, V_{OH}. Start of transmission is defined as the transition of the START bit from a high-level output voltage V_{OH}, to a low-level output voltage V_{OL}.
26-33	TR_1-TR_8	TRANSMITTER REGISTER DATA INPUTS	The character to be transmitted is loaded into the TRANSMITTER HOLDING REGISTER on these lines with the THRL Strobe. If a character of less than 8 bits has been selected (by WLS_1 and WLS_2), the character is right justified to the least significant bit, TR_1, and the excess bits are disregarded. A high-level input voltage, V_{IH}, will cause a high-level output voltage, V_{OH}, to be transmitted.
34	CRL	CONTROL REGISTER LOAD	A high-level input voltage, V_{IH}, on this line loads the CONTROL REGISTER with the control bits (WLS_1, WLS_2, EPE, PI, SBS). This line may be strobed or hard wired to a high-level input voltage, V_{IH}.

PIN DESCRIPTION

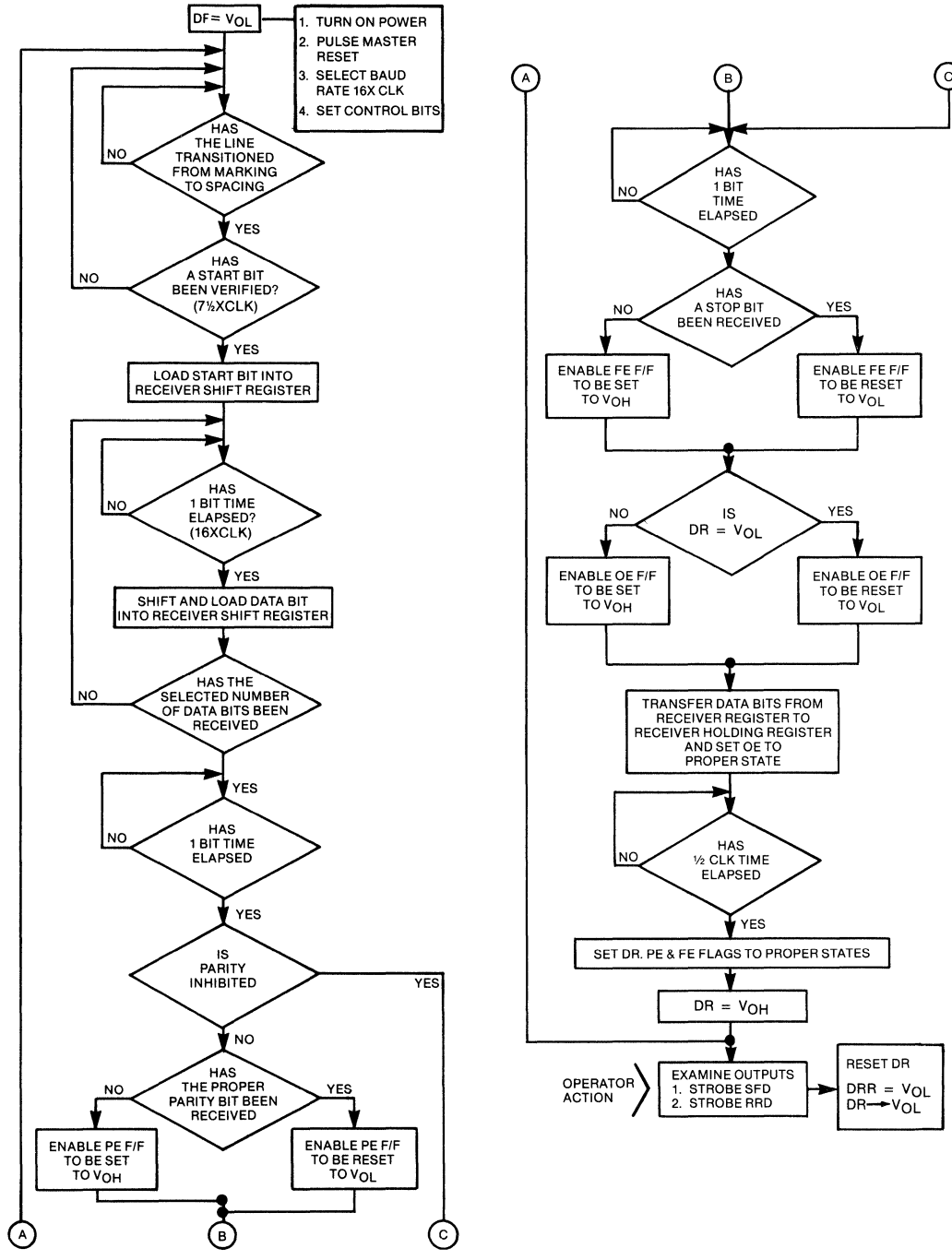
PIN NUMBER	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
35	PI	PARITY INHIBIT	A high-level input voltage, V_{IH}, on this line inhibits the parity generation and verification circuits and will clamp the PE output (pin 13) to V_{OL}. If parity is inhibited, the STOP bit(s) will immediately follow the last data bit of transmission.
36	SBS	STOP BIT(S) SELECT	This line selects the number of STOP bits to be transmitted after the parity bit. A high-level input voltage V_{IH}, on this line selects two STOP bits, and a low-level input voltage, V_{IL}, selects a single STOP bit. The TR1863 and TR1865 generate 1½ stop bits when word length is 5 bits and SBS is High V_{IH}.
37-38	WLS_2-WLS_1	WORD LENGTH SELECT	These two lines select the character length (exclusive of parity) as follows: WLS_2 / WLS_1 / Word Length V_{IL} / V_{IL} / 5 bits V_{IL} / V_{IH} / 6 bits V_{IH} / V_{IL} / 7 bits V_{IH} / V_{IH} / 8 bits
39	EPE	EVEN PARITY ENABLE	This line determines whether even or odd PARITY is to be generated by the transmitter and checked by the receiver. A high-level input voltage, V_{IH}, selects even PARITY and a low-level input voltage, V_{IL}, selects odd PARITY.
40	TRC	TRANSMITTER REGISTER	The transmitter clock frequency is sixteen (16) times the desired transmitter shift rate.



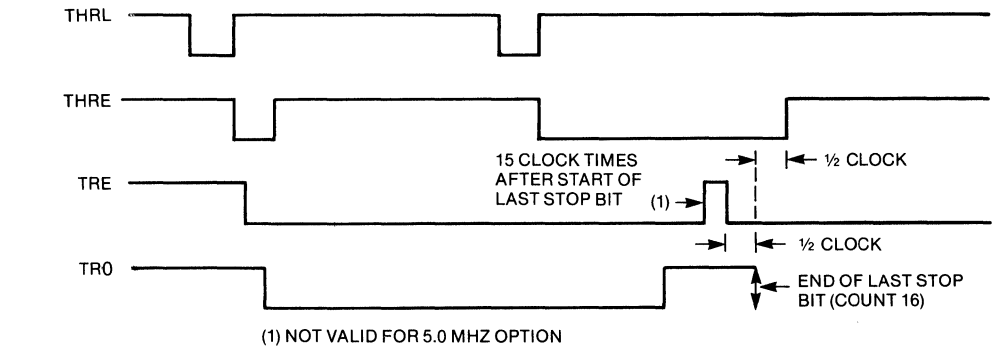
TR1863/TR1865 BLOCK DIAGRAM



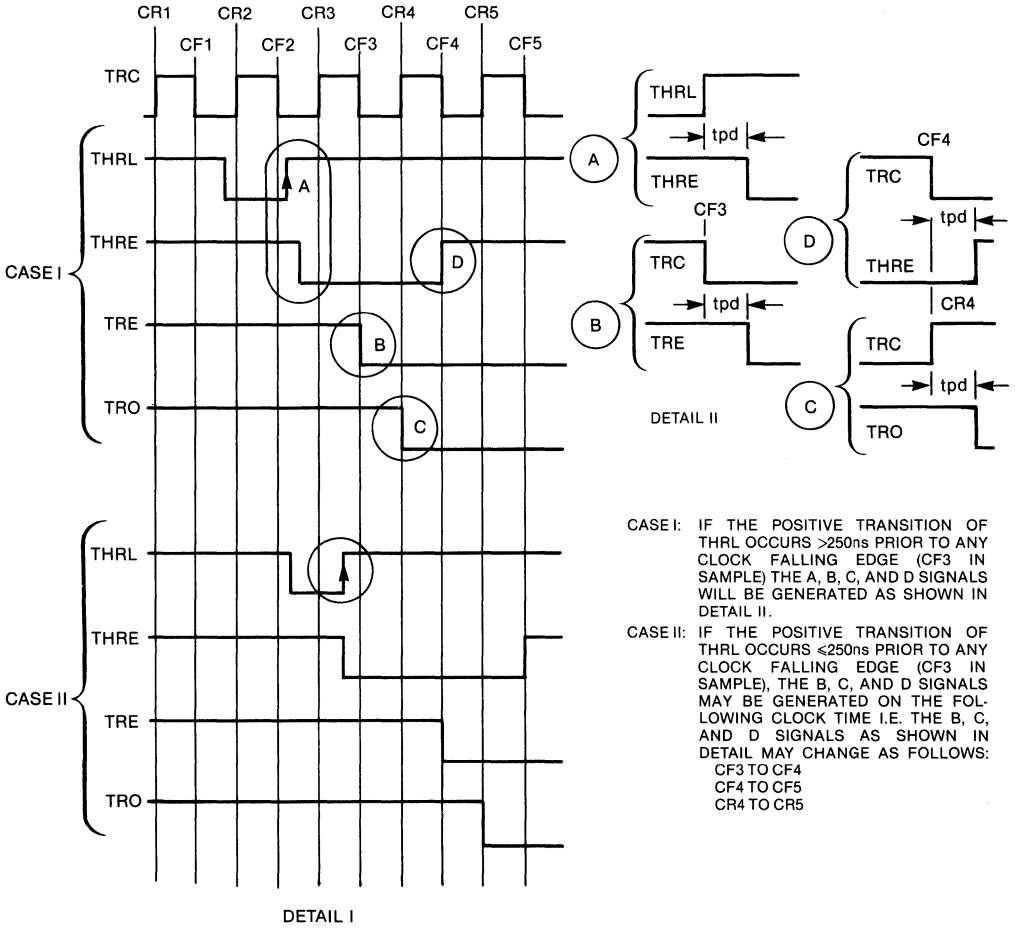
TRANSMITTER FLOW CHART



RECEIVER FLOW CHART



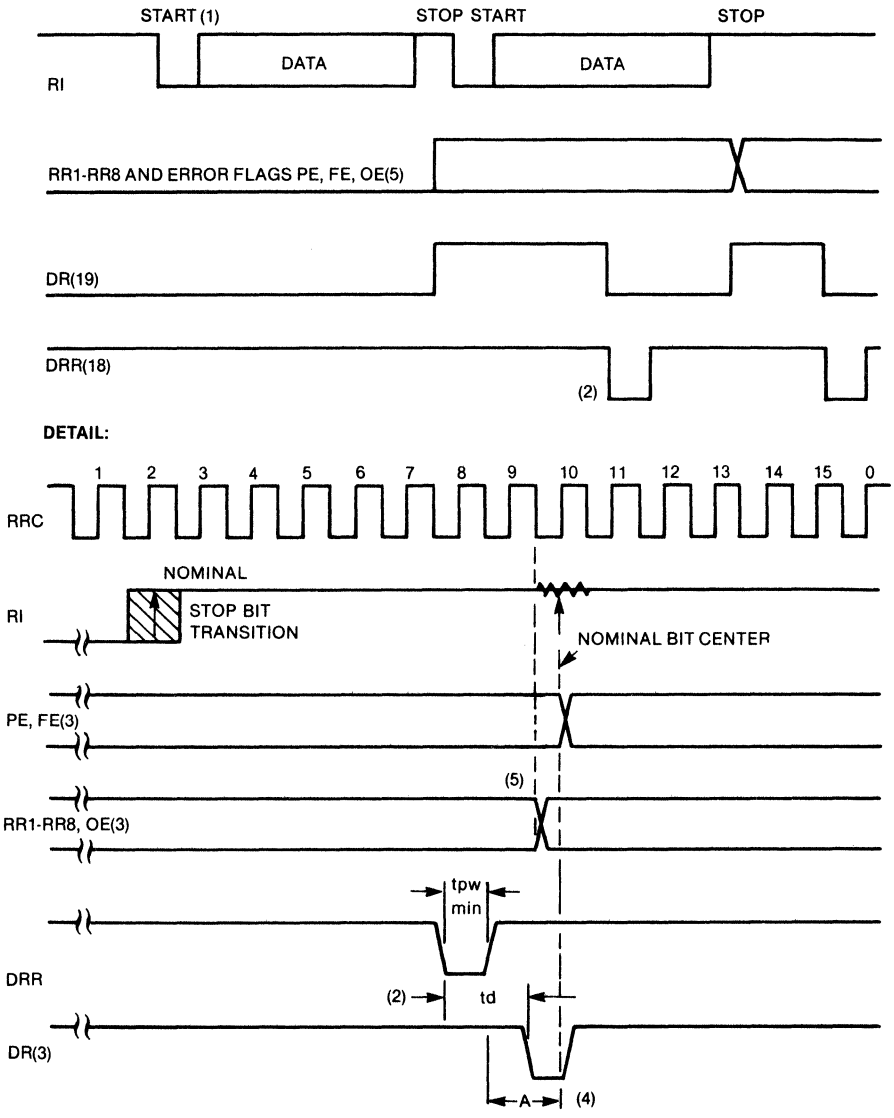
(1) NOT VALID FOR 5.0 MHZ OPTION



CASE I: IF THE POSITIVE TRANSITION OF THRL OCCURS >250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE) THE A, B, C, AND D SIGNALS WILL BE GENERATED AS SHOWN IN DETAIL II.

CASE II: IF THE POSITIVE TRANSITION OF THRL OCCURS ≤250ns PRIOR TO ANY CLOCK FALLING EDGE (CF3 IN SAMPLE), THE B, C, AND D SIGNALS MAY BE GENERATED ON THE FOLLOWING CLOCK TIME I.E. THE B, C, AND D SIGNALS AS SHOWN IN DETAIL MAY CHANGE AS FOLLOWS:
CF3 TO CF4
CF4 TO CF5
CR4 TO CR5

TRANSMITTER TIMING



(1) SEE APPLICATION FLAGS REPORT NO. 1 FOR DESCRIPTION OF START BIT DETECTION
(2) THE DELAY BETWEEN DRR AND DR = td = 500 NS
(3) DR. ERROR FLAGS, AND DATA ARE VALID AT THE NOMINAL CENTER OF THE FIRST STOP BIT
(4) DRR SHOULD BE HIGH A MINIMUM OF "A" NS (ONE-HALF CLOCK TIME PLUS tpd) PRIOR TO THE RISING EDGE OF DR
(5) DATA AND OE PRECEDES DR, PE, AND FE FLAGS BY ½ CLOCK
(6) DATA FLAGS WILL REMAIN SET UNTIL A GOOD CHARACTER IS RECEIVED OR MASTER RESET IS APPLIED.

FIGURE 1. RECEIVER TIMING

ABSOLUTE MAXIMUM RATINGS

NOTE: These voltages are measured with respect to GND

Storage Temperature
- Plastic ..... −55°C to +125°C
- Ceramic ..... −65°C to +150°C

V_{CC} Supply Voltage ..... −0.3V to +7.0V
Input Voltage at any pin ..... −0.3V to +7.0V
Operating Free-Air Temperature
- T_A Range ..... 0°C to 70°C

Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ± 5%, V_{SS} = 0V)

SYMBOL	PARAMETER	TR1863/5		
	OPERATING CURRENT	MIN	MAX	CONDITIONS
I_{CC}	Supply Current		35ma	V_{CC} = 5.25V
	LOGIC LEVELS			
V_{IH}	Logic High	2.4V		
V_{IL}	Logic Low		0.6V	V_{CC} = 4.75V
	OUTPUT LOGIC LEVELS			
V_{OH}	Logic High	2.4V		V_{CC} = 4.75V, I_{OH} = 100 μa
V_{OL}	Logic Low		0.4V	V_{CC} = 5.25V, I_{OL} = 1.6 ma
I_{OC}	Output Leakage (High Impedance State)		± 10μa	V_{OUT} = 0V, V_{OUT} = 5V SFD = RRD = V_1H
I_{IL}	Low Level Input Current	100μa	1.6ma	V_{IN} = 0.4V TR 1865 only
			10μa	V_{IN} = V_{IL}, TR 1863 only
I_{IH}	High Level Input Current		− 10μa	V_{IN} = V_{IH}, TR 1863 only

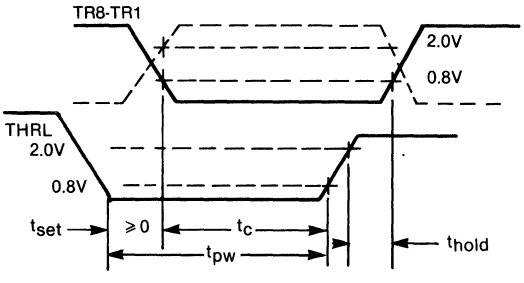


FIGURE 2. DATA INPUT LOAD CYCLE

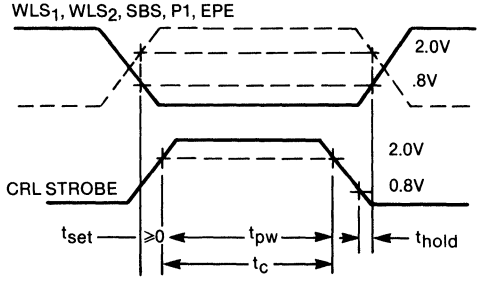
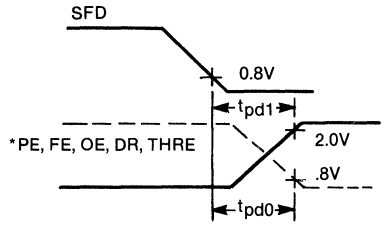
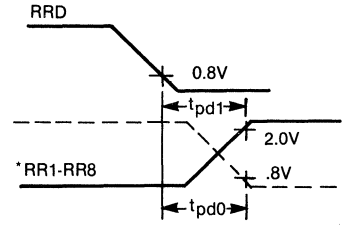


FIGURE 3. CONTROL REGISTER LOAD CYCLE



*OUTPUTS PE, FE, OE, DR, THRE ARE DISCONNECTED AT TRANSITION OF SFD FROM 0.8V TO 2.0V.

FIGURE 4. STATUS FLAG OUTPUT DELAYS



*RR_1-RR_3, ARE DISCONNECTED AT TRANSITION OF RRD FROM 0.8V TO 2.0V.

FIGURE 5. DATA OUTPUT DELAYS

SWITCHING CHARACTERISTICS

(See FIGURE 1-5)

SYMBOL	PARAMETER	MIN	MAX	CONDITIONS
f_{clk}	Clock Frequency			V_{CC} = 4.75V
	TR1863-00	DC	1.0 MHz	
	TR1863-02	DC	2.5 MHz	
	TR1863-04	DC	3.5 MHz	
	TR1865-00	DC	1.0 MHz	with internal pull-ups on all inputs
	TR1865-02	DC	2.5 MHz	with internal pull-ups on all inputs
	TR1865-04	DC	3.5 MHz	with internal pull-ups on all inputs
t_{pw}	Pulse Widths			
	CRL (Fig. 3)	200 ns		
	THRL (Fig. 2)	200 ns		
	DRR (Fig. 1)	200 ns		
	MR	500 ns		
t_c	Coincidence Time	200 ns		
t_{hold}	Hold Time (Fig. 2, 3)	20 ns		
t_{set}	Set Time (Fig. 2, 3)	0		
	OUTPUT PROPAGATION DELAYS			
t_{pd0}	To Low State (Fig. 4, 5)		250 ns	
t_{pd1}	To High State (Fig. 4, 5)		250 ns	C_L = 20 pf, plus one TTL load
	CAPACITANCE			
c_{in}	Inputs		20 pf	f = 1 MHz, V_{IN} = 5V
c_o	Outputs		20 pf	f = 1 MHz, V_{IN} = 5V

See page 383 for ordering information.

TR1863/65 MOS/LSI Application Notes
Asynchronous Receiver/Transmitter

INTRODUCTION

The transfer of digital data over relatively long distances is generally accomplished by sending the data in serial form thru a single communications channel using one of two general transmission techniques; asynchronous or synchronous. Synchronous data transmission requires that a clock signal be transmitted with the data in order to mark to location of the data bits for receiver. A specified clock transition (either rising or falling) marks the start of each data bit interval as shown in Figure 1. In addition, special synchronization data patterns are added to the start of the transmission in order for the receiver to locate the first bit of the message. with synchronous transmission, each data bit must follow contiguously after the sync word, since one data bit is assumed for every clock period or a fixed multiple of clock periods.

With asynchronous transmission, a clock signal is not transmitted with the data and the characters need not be contiguous, In order for the receiver to properly recover the message, the bits are grouped into data characters (generally from 5 to 8 bits in length) and synchronizing start and stop elements are added to each character as shown in Figure 2.

The start element is a single logic zero (space) data bit that is added to the front of each character. The stop element is a logic one (mark) that is added to the end of each character. The logic one (mark) level is maintained until the next data character is ready to be transmitted. (Asynchronous transmission is often referred to as start-stop transmission for obvious reasons). Although there is no upper limit to the length of the stop element, there is a lower limit that depends on the system characteristics. Typical lower limits are 1.0, 1.42 or 2.0 data bit intervals, although

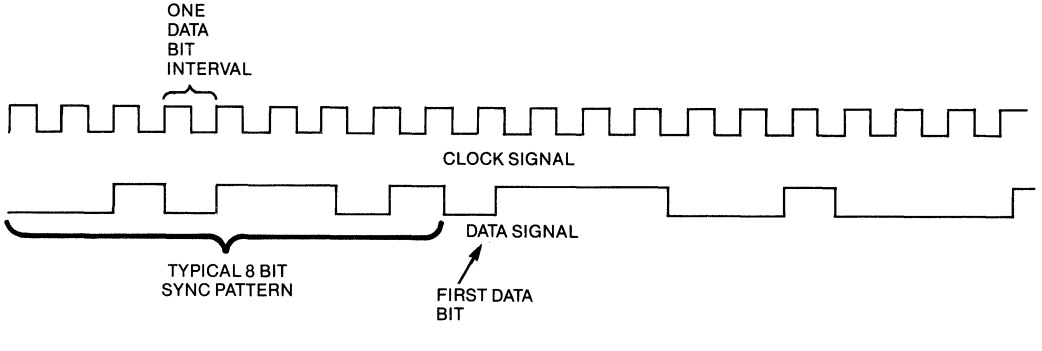


Figure 1. SYNCHRONOUS DATA

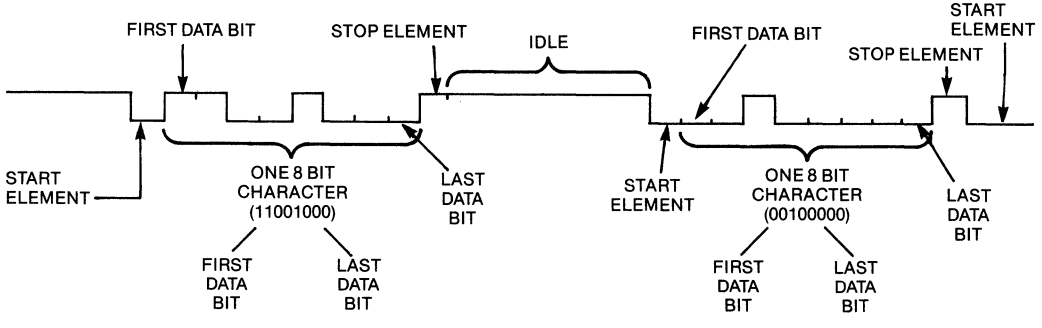


Figure 2. ASYNCHRONOUS DATA

most modern systems use 1.0 or 2.0. The negative going transition of the start element defines the location of the data bits in one character. A clock source at the receiver is reset by this transition and is used to locate the center of each data bit.

The rate at which asynchronous data is transmitted is usually measured in baud, where a baud is defined to be the reciprocal of the shortest signal element (usually one data bit interval). It is interesting to note that the variable stop bits is what makes the baud rate differ from the bit rate. For synchronous transmission, each data element is equal to the clock period therefore the baud rate equals the bit rate. The same is true for asynchronous transmission if the stop element is always one bit in duration (this is referred to as isochronous transmission). However, when the stop code is longer than one bit, as shown in Figure 3, the baud rate differs from the bit rate.

Each character in Figure 3 is 11 data bit intervals in length, and if 15 characters are transmitted per second, then the shortest signal element (one data bit interval) is 66.6 ms/11 = 6.06 ms; giving a rate of 1/6.06 ms = 165 baud. However, since only 10 bits of information (8 data bits, one start bit and 1 stop bit) are transmitted every 66.6 msec, the bit rate is 150 bit/sec. (Even though the stop element lasts for two data intervals, it still is only one bit of information.)

There are several reasons for using asynchronous transmission. The major reason is that since a clock signal need not be transmitted with the data, transmission equipment requirements are greatly simplified. (Note, however, that an independent clock source is still required at both the transmitter and receiver). Another advantage of asynchronous transmission is that characters need not be contiguous in time, but are transmitted as they become available. This is a very valuable feature when transmitting data from manual entry devices such as a keyboard. The major disadvantage of asynchronous transmission is that it requires a very large portion of the communication channel bandwidth for the synchronizing start and stop elements (a much smaller portion of the bandwidth is required for the sync words used in synchronous transmission).

Asynchronous transmission over a simple twisted wire pair can be accomplished at moderately high baud rates (10K baud or higher depending on the length of the wire, type of the line drivers, etc.) while it is generally limited to approximately 2K baud over the telephone network. Other types of asynchronous transmission can be as high as 218K baud. When operating over the telephone network, a modem is required to convert the data pulses to tones that can be transmitted through the network.

One of the major limiting factors in the speed of asynchronous transmission is the distortion of the signal elements. Distortion is defined as the time displacement between the actual signal level transmission and the nominal transition ($\Delta\dagger$), divided by the nominal data bit interval (See Figure 4).

The nominal data bit interval is equal to the reciprocal of the nominal transmission baud rate and all data transitions should ideally occur at an integer number of intervals from the negative transition of the start bit. Actual data transitions may not occur at these nominal points in time as shown in the lower waveform of Figure 4. The distortion of any bit transition is equal to $\Delta\dagger$ x NOMINAL BAUD RATE.

This distortion is generally caused by frequency jitter and frequency offset in the clock source, used to generate the actual waveform as well as transmission channel, noise, etc. Thus, the amount of distortion that can be expected on any asynchronous signal depends on the device used to generate the signal and the characteristics of the communication channel over which it was sent. Electronic signal generators can be held to less than 1% distortion while electromechanical devices (such as a teletype) typically generate up to 20% distortion. The transmission channel may typically add an additional 5% to 15% distortion.

The distortion previously described referred only to a single character as all measurements were referenced to the start element transition of that character. However, there may also be distortion between characters when operating at the maximum possible baud rate (i.e., stop elements are of minimum length).

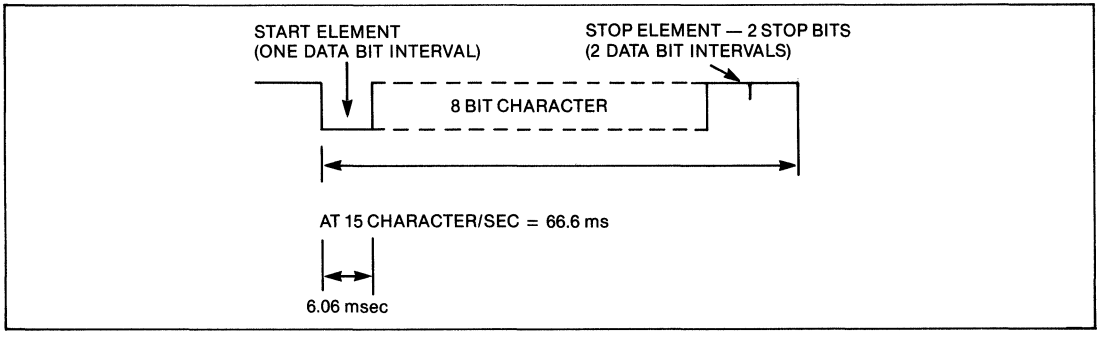


Figure 3.

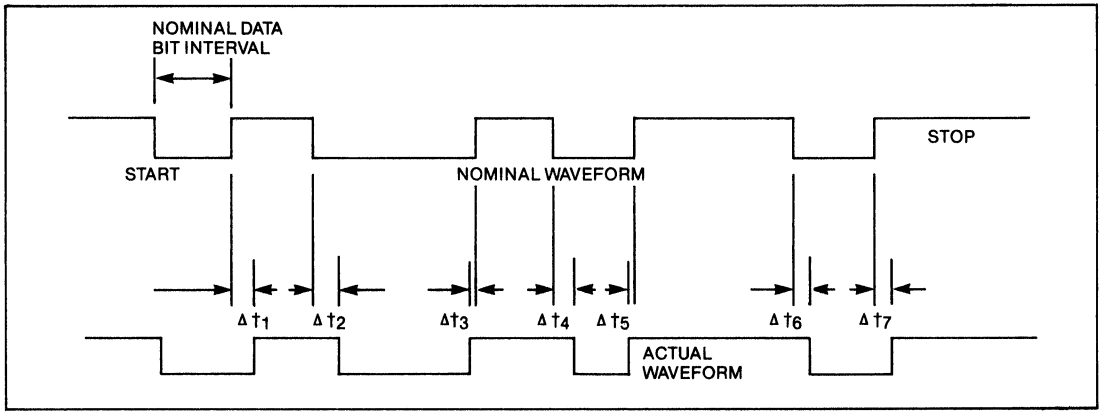


Figure 4A.

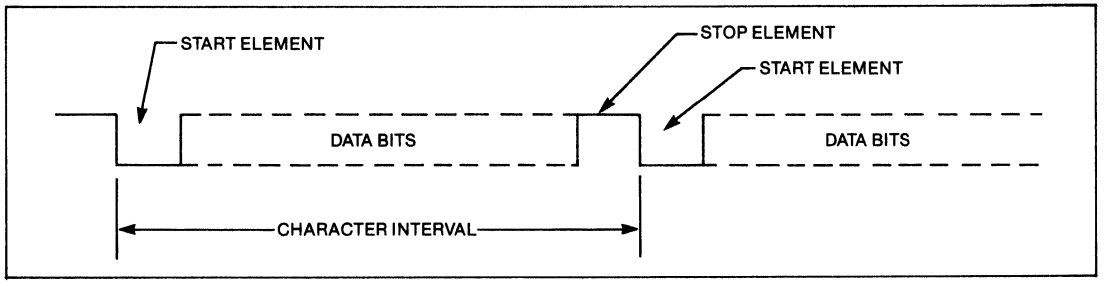


Figure 4B.

This type of distortion is usually measured by the minimum character interval as shown in Figure 4B.

The minimum character interval distortion is generally specified as the percentage of a nominal data bit interval that any character interval may be shortened from its nominal length. Since many of the same parameters that cause distortion of the data bits are also responsible for the character length distortion, the two distortions are often equal. However, some systems may exhibit character interval distortions of up to 50% of a data bit interval. This parameter is important when operating at the maximum baud rate since the receiver must be prepared to detect the next start bit transition after the minimum character interval.

Asynchronous receivers operate by locating the nominal center of the data bits as measured from the start bit negative going transition. However, due to receiver inaccuracies, the exact center may not be properly located. In electromechanical devices such as teletypes, the inaccuracy may be due to mechanical tolerances or variations in the power line frequency. With electronic receivers, the inaccuracies are due to frequency offset, jitter and resolution of the clock source used to find the bit centers. (The bit centers are located by counting clock pulses). For example, even if the receiver clock had no jitter or offset, and it was 16 times the baud rate, then the center of the bit could only be located within 1/16 of a bit interval (or 6.25%) due to clock resolution. However, by properly phasing the clock, this tolerance can be adjusted so that the sampling will always be within ±3.125% of the bit center. Thus, signals with up to 46.875% distortion could be received. This number (the allowable receiver input distortion) is often referred to as the receiver distortion margin. Electromechanical receivers have distortion margins of 25 to 30%. The receiver must also be prepared to accept a new character after the minimum character interval. Most receivers are specified to operate with a minimum character interval distortion of 50%.

TR1863/65 OPERATION

TR1863/65 is designed to transmit and receive asynchronous data as shown in Figure 5. Both the transmitter and the receiver are in one MOS CHIP, packaged in a 40 lead ceramic DIP. The array is capable of full duplex (simultaneous transmission and reception) or half duplex operation.

The transmitter basically disassembles parallel data characters into a serial asynchronous data system. Control lines are included so that the characters may be 5, 6, 7 or 8 bits in length, have an even or odd parity bit, and have either one or two * stop bits. Furthermore, the baud rate can be set anywhere between DC and 218K baud (3.5 MHz clock) by providing a transmit clock at 16 times the desired baud rate.

* 1-1/2 with 5 bit code

The receiver assembles the asynchronous characters into a parallel data character by searching for the start bit of every character, finding the center of every data bit, and outputting the characters in a parallel format with the start, parity and stop bits removed. Three error flags are also provided to indicate if the parity was in error, a valid stop bit was not decoded or the last character was not unloaded by the external device before the next character was received (and therefore the last character was lost). The receiver clock is set at 16 times the transmitter baud rate.

Both the transmitter and receiver have double character buffering so that at least one complete character interval is always available for exchange of the characters with the external devices. This double buffering is especially important if the external device is

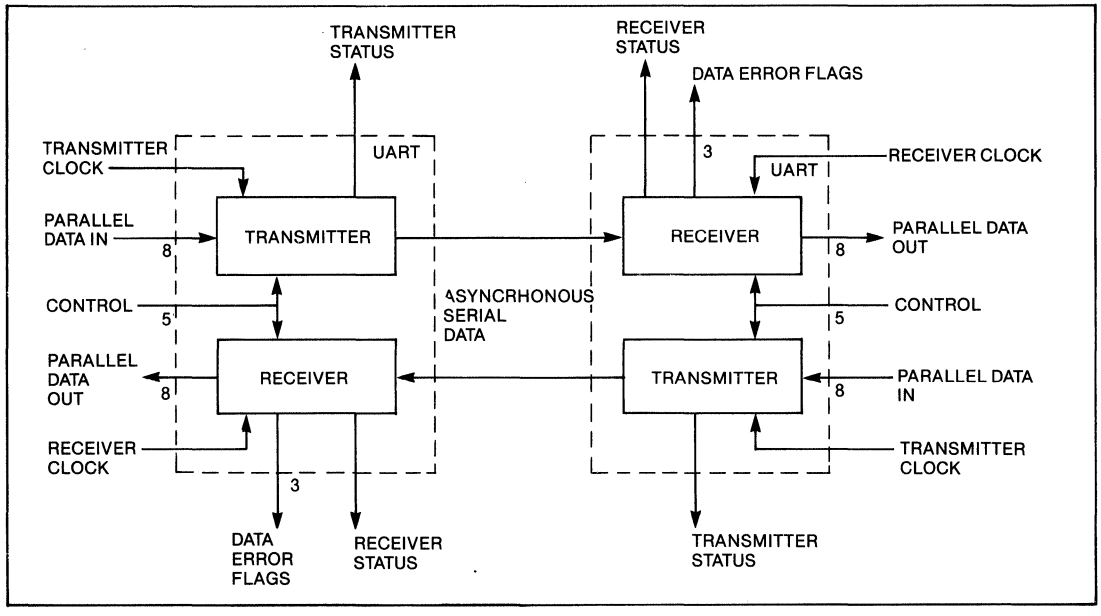


Figure 5.

a computer, since this provides a much longer permissible interrupt latency time (the time required for the computer to respond to the interrupt).

The status of the transmitter buffer and the receiver buffer (empty or full) is also provided as an output.

Another feature of the UART is that the control information can be strobed into the transmitter and receiver and stored internally. This allows a common bus from a computer to easily maintain the controls for a large number of transmitter/receivers.

The UART data and error flag outputs are designed for direct compatibility with bus organized systems. This feature is achieved by providing completely TTL compatible Three-state outputs (no external components are required). Three-state outputs may be set to a logic one or logic zero when enabled, or set to an open circuit (very high impedance) when disabled. A separate control line is provided to enable the data outputs and another one to enable the error flags so that the data outputs can be tied to a separate bus from the flag outputs.

The TR1865 has internal pullups connected to its inputs making it TTL compatible, while the TR1863 requires external pullups to be connected to its input pins.

UART DESCRIPTION

Figure 6 is a block diagram of the transmitter portion of the UART. Data can be loaded into the Transmitter Holding Register whenever the Transmitter Holding Register Empty (THRE) line is at a logic one, indicating the the Transmitter Holding Register is empty. The data is loaded in by strobing the Transmitter Holding Register Load (THRL) line to a logic zero. The data is automatically transferred to the Transmitter Register as soon as the Transmitter Register becomes empty. The desired start, stop and parity bits are then added to the data and serial transmission is started. The number of stop bits and the type of parity bit is under control of the Control Register. The state of the control lines is loaded into the Control Register when the Control Register Load (CRL) line is strobed to a logic one. The 5 control lines allow 24 different character formats as shown in Table 1. These 24 formats cover almost all of the transmission schemes presently in use.

A Master Reset (MR) input is provided which sets the transmitter to the idle state whenever this line is strobed to a logic one. In addition, a Status Flag Disconnect (SFD) line is provided. When this signal is at a logic one, the THRE output is disabled and goes to a high impedance. This allows the THRE outputs of a number of arrays to be tied to the same data bus.

Figure 7 illustrates the relative timing of the transmitter signals. After power turn-on, the master reset should be strobed to set the circuits to the idle state. The external device can then set the transmitter register data inputs to the desired value and after the data inputs are stable, the load pulse is applied. The data is then automatically transferred to the Transmitter Register where the start, stop and parity (if required) bits are added and transmission is started. This process is then repeated for each subsequent character as they become available. The only timing requirement for the external device is that the data inputs be stable during the load pulse (and 20 nsec after).

Table 1.
CONTROL DEFINITION

CONTROL WORD					CHARACTER FORMAT			
WLS2	WLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	x	0	1	5	NONE	1
0	0	1	x	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	x	0	1	6	NONE	1
0	1	1	x	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	x	0	1	7	NONE	1
1	0	1	x	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	x	0	1	8	NONE	1
1	1	1	x	1	1	8	NONE	2

The UART Transmitter output will have less than 1% Distortion at baud rates of up to 218K baud (assuming the Transmitter Register Clock is perfect) and is, therefore, compatible with virtually all other asynchronous receivers.

Figure 8 is a block diagram of the Receiver portion of the UART. Serial asynchronous data is provided to the Receiver Input (RI). A start bit detect circuit continually searches for a logic one to logic zero transition while in the idle (logic one) state. When this transition is located, a counter is reset and allowed to count until the center of the start bit is located. If the input is still a logic zero at the center, the signal is assumed to be a valid start bit and the counter continues to count to find the center of all subsequent data and stop bits. (Verification of the start bit prevents the receiver from assembling an erroneous data character when a logic zero noise

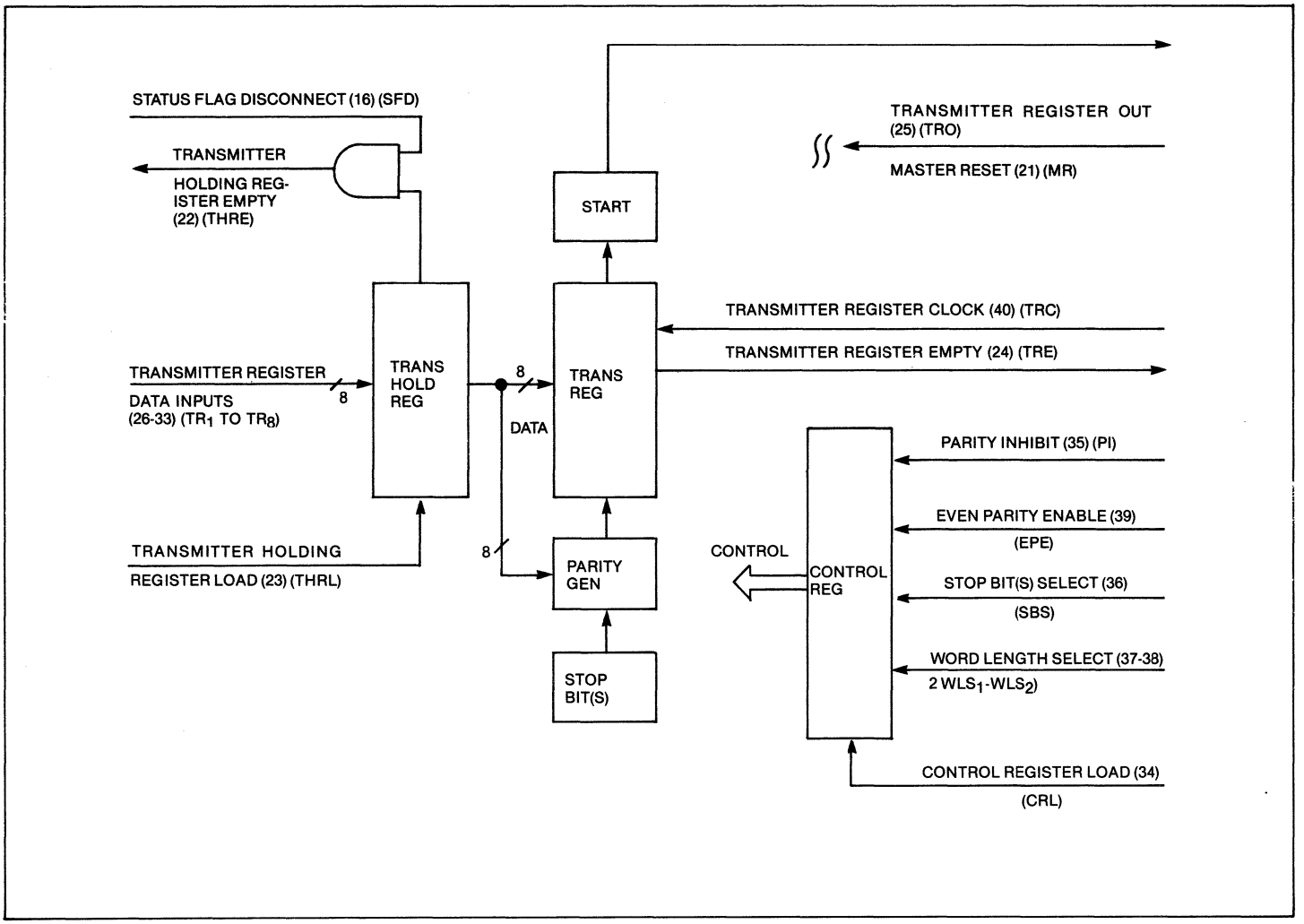


Figure 6. TRANSMITTER BLOCK DIAGRAM

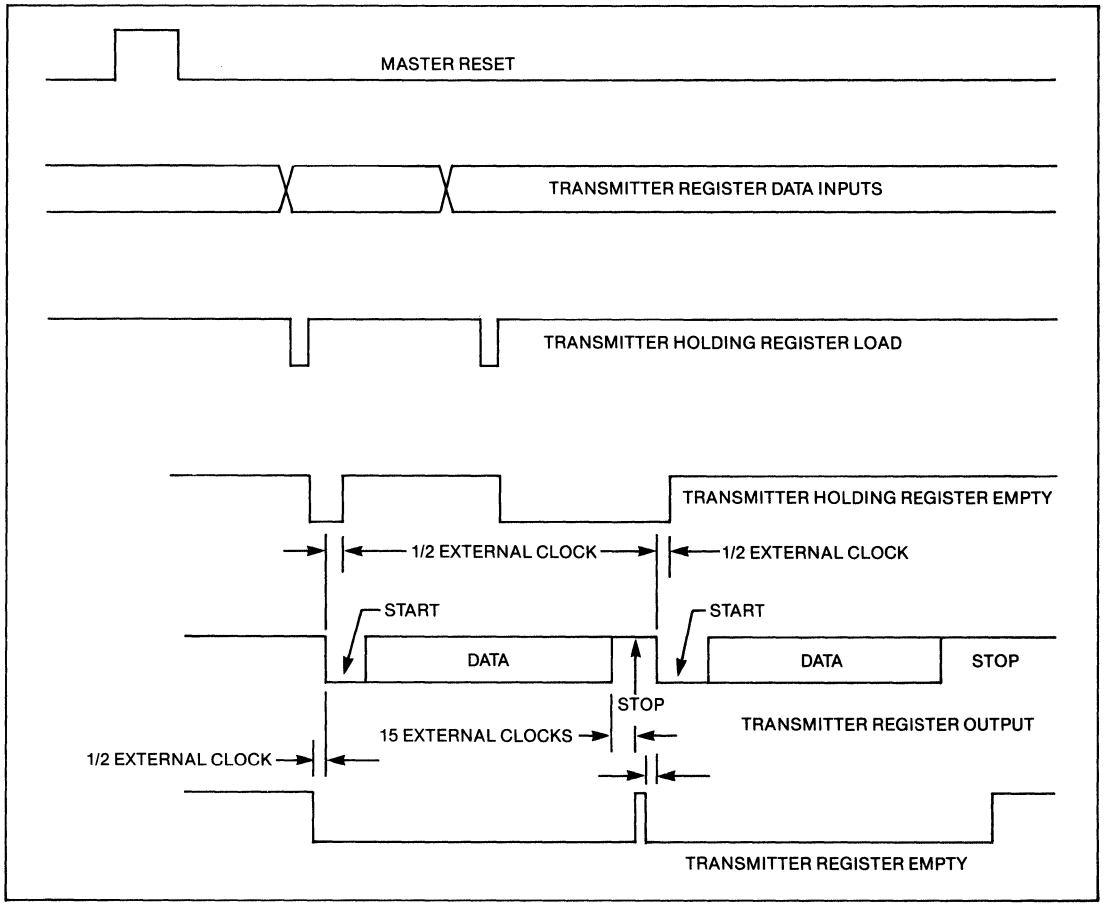


Figure 7. TRANSMITTER TIMING DIAGRAM

spike is presented to the Receiver Input). The Receiver is under control of the Control Register described in the previous paragraph. This register controls the number of data bits, number of stop bits, and the type of parity as described in Table 2. The word length gating circuit adjusts the length of the Receiver Register to match the length of the data characters. A parity check circuit checks for even or odd parity if parity was programmed. If parity does not check a Parity Error signal will be set to a logic one and this signal will be held until the next character is transferred to the Holding Register. A circuit is also provided that checks the first stop bit of each character. If the stop bit is not a logic one, the Framing Error line will be set to a logic one and held until the next character is transferred to the Holding Register. This feature permits easy detection of a break character (null character with no stop element). As each received character is transferred to the Holding Register, the Data Received (DR) line is set to a logic one indicating that the external device may sample the data output. When the external device samples the output, it should strobe the Data Received Reset (DRR) line to a logic zero to reset the DR line. If the DR line is not reset before a new character is transferred to the Holding Register (i.e., a character is lost) the Overrun Error line will be set to a logic one and held until the next character is loaded into the Holding Register. The timing for all of the Receiver functions is obtained from the external Receiver Register Clock which should be set at 16 times the baud rate of the transmitter.

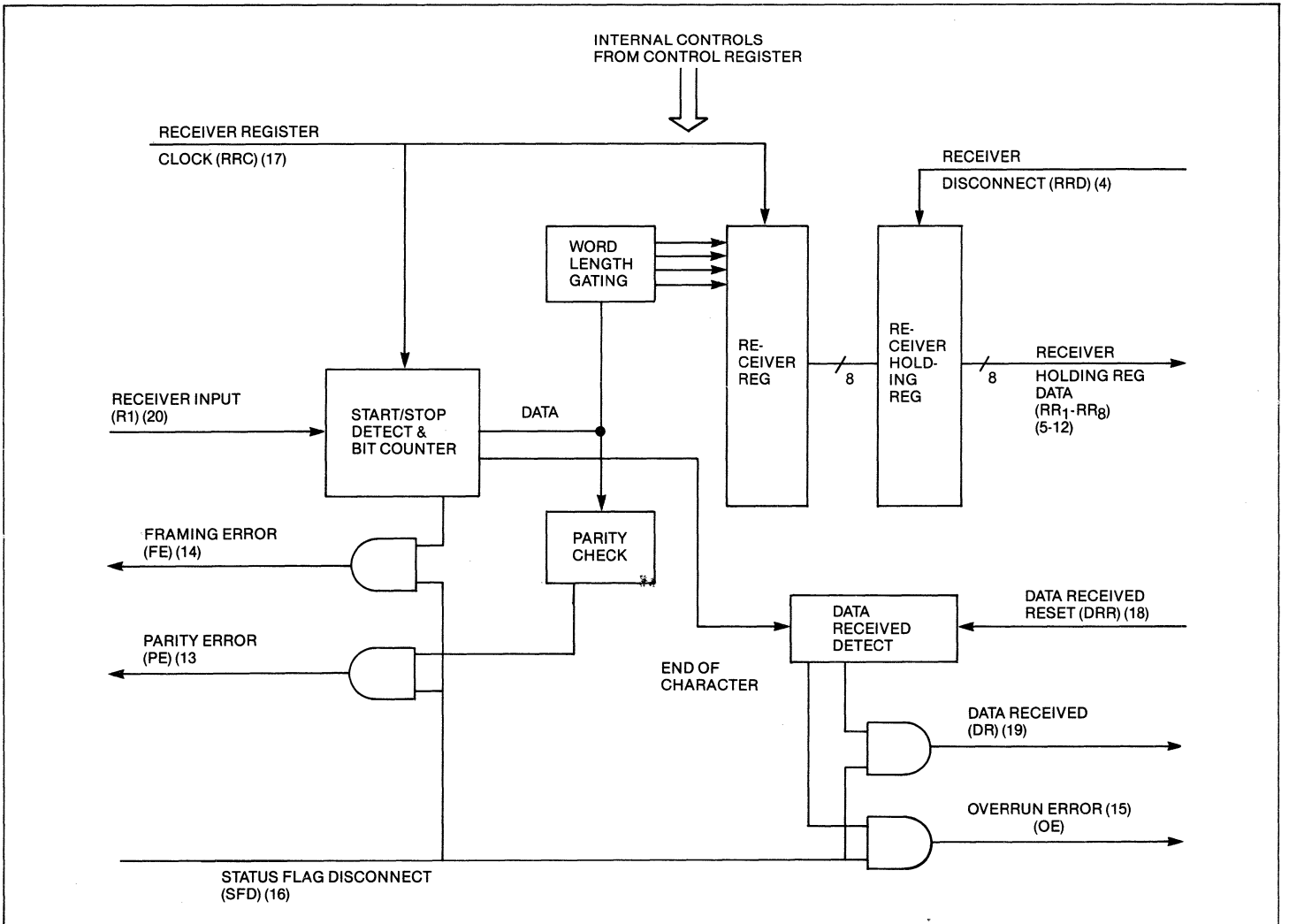


Figure 8. RECEIVER BLOCK DIAGRAM

Figure 9 illustrates the relative timing of the Receiver signals. A Master Reset strobe places the unit in the idle mode and the Receiver then begins searching for the first start bit. After a complete character has been decoded, the data output and error flags are set to the proper level and the Data Received (DR) line is set to a logic one. Although it is not apparent in Figure 9, the data outputs are set to the proper level one half clock period before the DR and error flags, which are set in the center of the first stop bit. The Data Received Reset pulse resets the DR line to a logic zero. Data can be strobed out at any time before the next character has been disassembled.

The UART Receiver uses a 16X clock for timing purposes. Furthermore, the center of the start bit is defined as clock count 7-1/2. Therefore, if the receiver clock is a symmetrical square wave as shown in Figure 10, the center of the bits will always be located within ±3.125% (assuming a perfect input clock) thus giving a receiver margin of 46.875%.

In Figure 10, the start bit could have started as much as one complete clock period before it was detected, as indicated by the shaded area of the negative going transition. Therefore, the exact center is also unknown by the shaded area around the sample point. This turns out to be ± 1/32 = ±3.125%.

If the receiver clock is not perfect, then the receiver distortion margin must be further reduced. For example, if the clock had 1.0% jitter, 0.1% offset and the positive clock pulse was only 40% of the clock cycle; then, for a 10 element character, the clock would add:

1.0% (Jitter)	+ (0.1% x 10) (Offset)	+ 0.1 (1/16) (Non-symmetrical Clock)	=	2.3% Distortion

(The frequency offset was multiplied by the number of elements per character since the offset is cumulative on each element.

Since a clock with these characteristics is very easy to obtain, it is apparent that a receiver operating margin of slightly over 45% is very easy to achieve when using the UART. Furthermore, this margin is sufficient for virtually all existing transmitters and modems presently in use.

The UART also begins searching for the next start bit exactly in the center of the first stop bit so that minimum character distortions of up to 50% can be accepted.

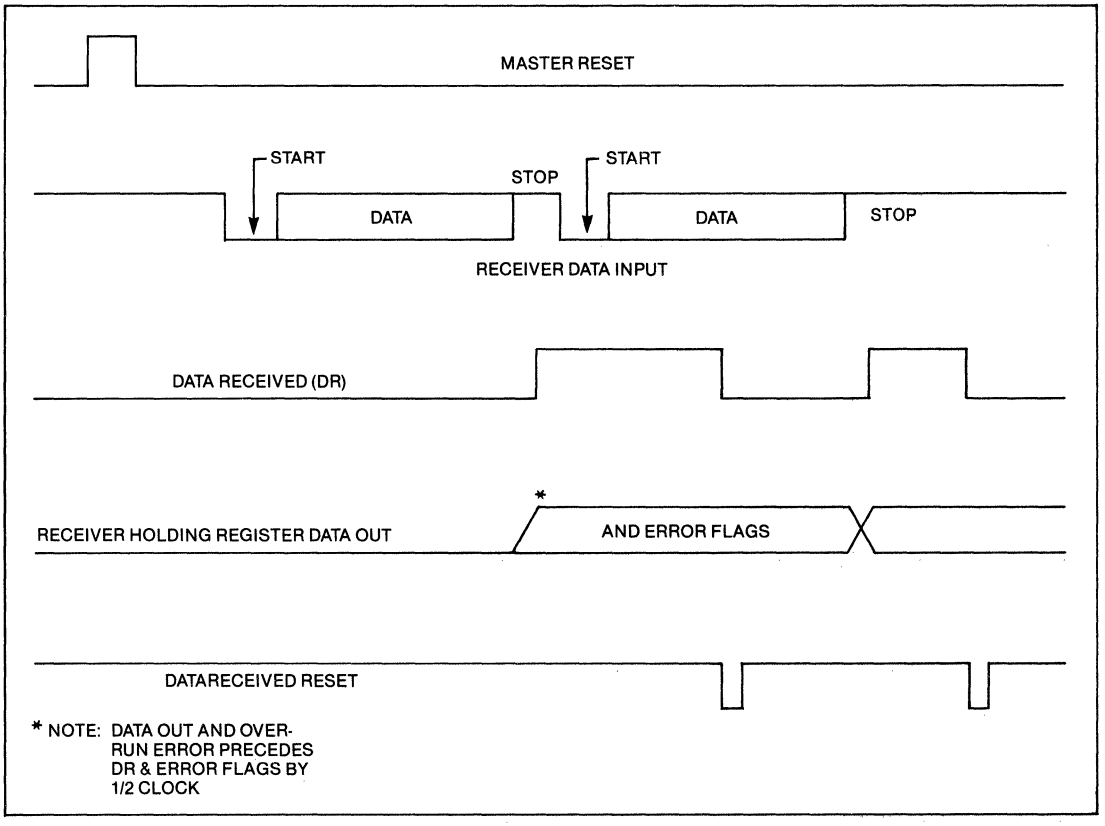


Figure 9. RECEIVER TIMING DIAGRAM

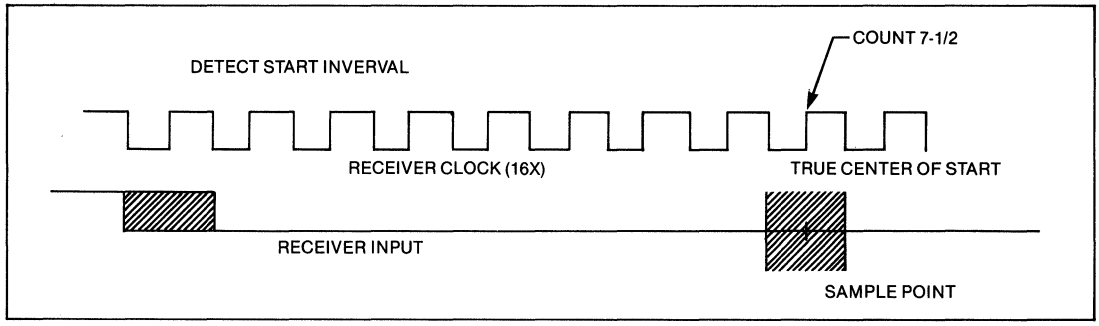


Figure 10.

A break character (null character without a stop bit) will lock the receiver up since it will not begin looking for the next start bit until a stop bit has been received.

TYPICAL UART APPLICATION

The UART is ideally suited for use in distributed computer networks such as is illustrated in Figure 11. One of the primary purposes of the communications controller is to assemble and disassemble the asynchronous characters (required for communication with the data terminals) to/from the parallel data format required by the host computer. Often the communications controller is a micro-computer and character assembly/disassembly is performed by the software. When this is the case, the micro-computer must be interrupted at a rate equal to 8 to 16 times the baud rate of all terminals being handled by the controller. (The actual interrupt rate depends on the amount of distortion that can be experienced on the received characters). When the number of terminals exceeds 8 to 16, even the most powerful micro-computers become overloaded due to the high interrupt rate and the complex algorithms required by the software.

The UART greatly reduces this problem by performing the character assembly/disassembly functions in external hardware as shown in a typical configuration in Figure 12. This solution not only reduces the interrupt rate by a factor of up to 176, but it also greatly reduces the micro-computer load, thus freeing it for other functions.

Since the UART inputs and outputs are TTL compatible, it interfaces directly with virtually all micro-computer I/O busses. In Figure 12, the micro-computer Data Output Bus is connected to the Transmitter Register (TR) inputs and the Control Register inputs. When the micro-computer has a character to transmit, the character is placed on the Data Output bus and the address of the appropriate UART is placed on the Device Address Bus. The Address Decode circuit will output a THRL load pulse under control of the Data Out Strobe from the micro-computer. When the control register should be changed, a new 5 bit control word is placed on the Data Output Bus and along with an appropriate device address which is converted to a CRL load pulse in the Address Decode circuits, again under control of the Data Out Strobe. A THRE Pulse to the Interrupt Request circuit will notify the micro-computer when a new character may be provided to the UART for transmission.

When a character has been received, a DR signal to the Interrupt Request circuit will request an interrupt from the micro-computer. The micro-computer will respond by setting the proper device address and provide a Data in Strobe pulse. The Address-Decode circuit then sets the RRD line and SFD line to the appropriate receiver to enable the Data Outputs onto the mini Data Input Bus. The Data in Strobe from the micro-computer then resets the DR signal with a DRR pulse from the Address Decode circuit.

The UART Transmitter Output (TRO) and Receiver Input (RI) must generally be converted to RS232 levels if they interface with a modem as shown in Figure 12. RS232 is a standard that has been established by the Electronic Industries Association for the interface between data terminals and data communications equipment. RS232-C defines a space as greater than 3 volts and a mark as less than negative 3 volts at the Receiver input. A transmitter output of between 5 and 15 volts is a space while a level between -5 and -15 is a mark. The input/output impedances and signal rise and fall times are also specified by RS232. Fairly simple discrete level translators can be used to convert from the TTL levels to the RS232 levels, or monolithic IC's are also available.

It should be noted that the typical application illustrated in Figure 12 is only one of many and it does not take advantage of many of the UART features. For example, the Status Flags could be tied to a separate interrupt request bus or the TRE output could be used to implement half-duplex operation.

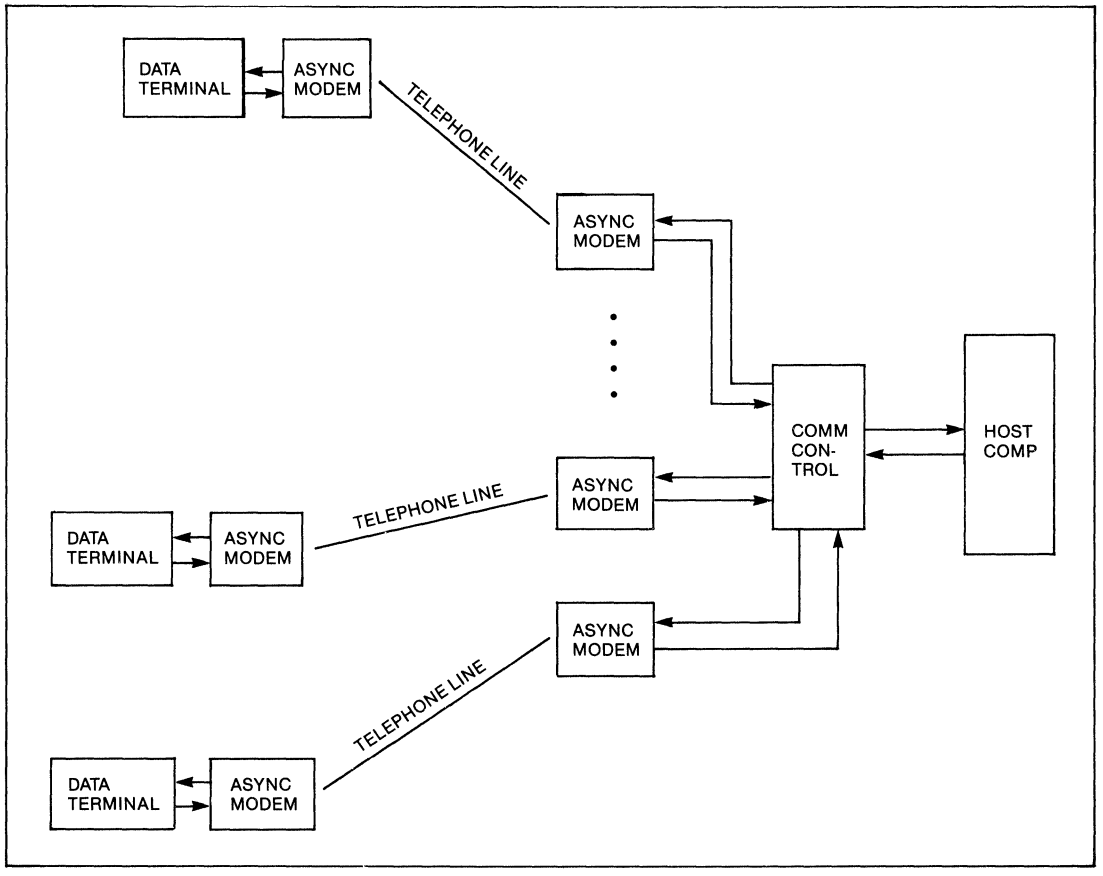

DATA TERMINAL
ASYNC MODEM
TELEPHONE LINE
ASYNC MODEM
COMM CON-TROL
HOST COMP
DATA TERMINAL
ASYNC MODEM
TELEPHONE LINE
ASYNC MODEM
DATA TERMINAL
ASYNC MODEM
TELEPHONE LINE
ASYNC MODEM

Figure 11.

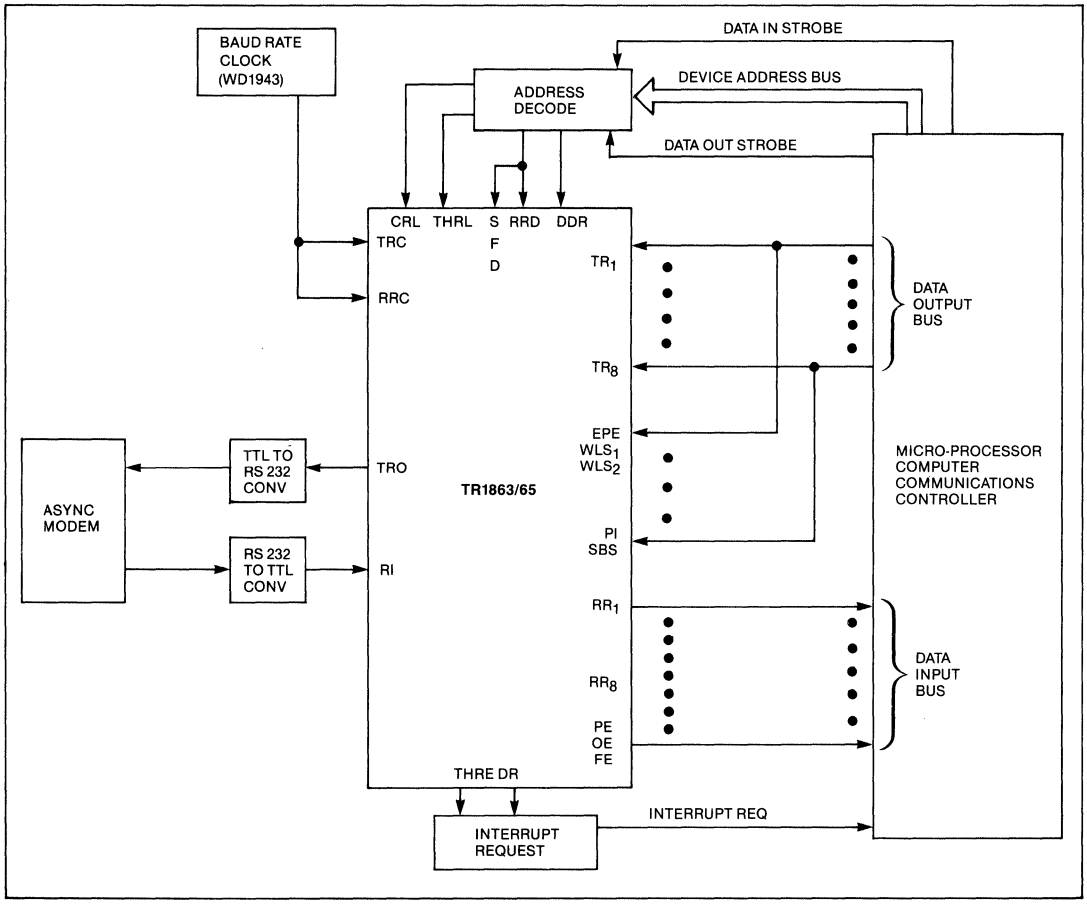


Figure 12. TYPICAL MICROCOMPUTER INTERFACE

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FINAL

UC1671 ASTRO

FEATURES

SYNCHRONOUS AND ASYNCHRONOUS
- Full Duplex Operations

SYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Two Successive SYN Characters Sets Synchronization
- Programmable SYN and DLE Character Stripping
- Programmable SYN and DLE-SYN Fill

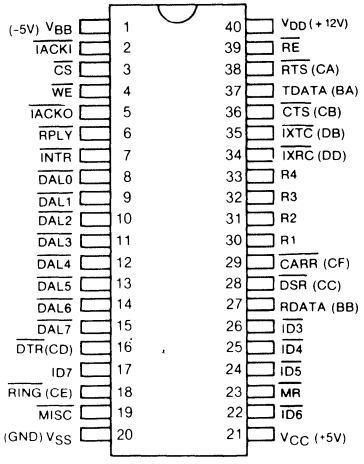
ASYNCHRONOUS MODE
- Selectable 5-8 Bit Characters
- Line Break Detection and Generation
- 1-, 1½-, or 2-Stop Bit Selection
- False Start Bit Detection Automatic Serial Echo Mode

SYSTEM COMPATIBILITY
- Double Buffering of Data
- 8-Bit Bi-Directional Bus For Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- Up to 32 ASTROS Can Be Addressed On Bus
- On-Line Diagnostic Capability

TRANSMISSION ERROR DETECTION-PARITY
- Overrun and Framing

BAUD RATE — DC TO 1M BIT/SEC

8 SELECTABLE CLOCK RATES
- Accepts 1X Clock and Up to 4 Different 32X Baud Rate Clock Inputs
- Up to 47% Distortion Allowance with 32X Clock



PIN DESIGNATION

APPLICATIONS

SYNCHRONOUS COMMUNICATIONS
ASYNCHRONOUS COMMUNICATIONS
SERIAL/PARALLEL COMMUNICATIONS

DESCRIPTION

The UC1671 (ASTRO) is a MOS/LSI device which performs the functions of interfacing a serial data communication channel to a parallel digital system. The device is capable of full duplex communications (receiving and transmitting) with synchronous or asynchronous systems. The ASTRO is designed to operate on a multiplexed bus with other bus-oriented devices. Its operation is programmed by a processor or controller via the bus and all parallel data transfers with these machines are accomplished over the bus lines.

The ASTRO is fabricated in n-channel silicon gate MOS technology and is TTL compatible on all inputs and outputs.

PIN DESCRIPTION

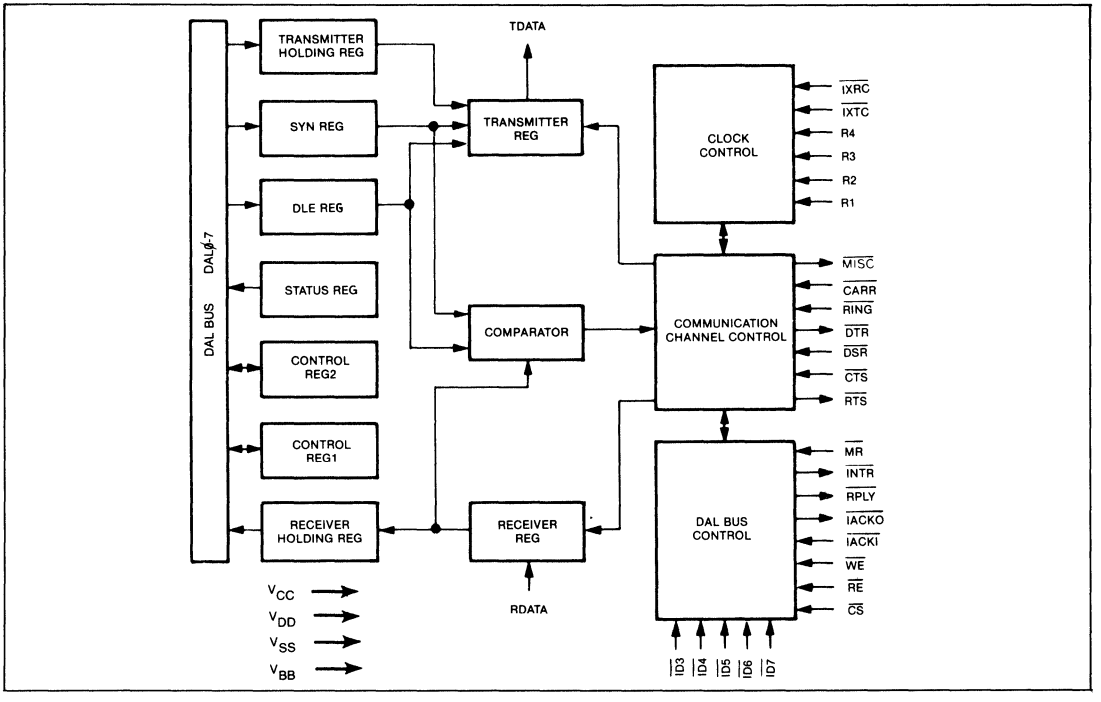
The device is packaged in a 40-pin plastic or ceramic cavity package. The interface signals are defined below with all input/output signals complemented to facilitate bussing and interfacing with TTL. The Data Set controls and Status signals are also complemented to allow for an inversion when converting to EIA RS232C levels. The names and symbols assigned to the Data Set interface signals follows EIA standard nomenclature.

A bar over a signal ($\overline{\text{SIGNAL}}$), means active low (set = low).

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	V_{BB}	POWER SUPPLIES	−5V
2	$\overline{\text{IACKI}}$	$\overline{\text{INTERRUPT ACKNOWLEDGE IN}}$	This input becomes low when polling takes place on the bus by the Controller to determine the interrupting source. When this signal is received, the ASTRO places its ID code on the DAL if it is requesting interrupt, otherwise it makes IACKO a low.
3	$\overline{\text{CS}}$	$\overline{\text{CHIP SELECT}}$	The low logic transition of CS identifies a valid address on the DAL bus during Read and Write operations.
4	$\overline{\text{WE}}$	$\overline{\text{WRITE ENABLE}}$	This signal, when low, gates the contents of the DAL bus into the addressed register of a selected ASTRO.
5	$\overline{\text{IACKO}}$	$\overline{\text{INTERRUPT ACKNOWLEDGE OUT}}$	This output is made a logic low in response to a low IACKI if the ASTRO receiving an IACKI input is not the interrupting device.
6	$\overline{\text{RPLY}}$	$\overline{\text{REPLY}}$	This open drain output is made low when the ASTRO is responding to being selected by an address on the DAL during read or write operations or in affirming that it is the interrupting source during interrupt polling.
7	$\overline{\text{INTR}}$	$\overline{\text{INTERRUPT}}$	This open drain output is made low when one of the communication interrupt conditions occur.
8-15	$\overline{\text{DAL0-DAL7}}$	$\overline{\text{DATA ACCESS LINES}}$	Eight-bit bi-directional bus used for transfer of data, control, status, and address information.
16	$\overline{\text{DTR}}$ ($\overline{\text{CD}}$)	$\overline{\text{DATA TERMINAL READY}}$	This output is generated by a bit in the Control Register and indicates Controller readiness.
17,22,24, 25,26	$\overline{\text{ID7-ID3}}$	$\overline{\text{SELECT CODE}}$	Five input pins which when hard-wired assign the device a unique identification code used to select the device when addressing and used as an identification when responding to interrupts.
18	$\overline{\text{RING}}$ ($\overline{\text{CE}}$)	$\overline{\text{RING INDICATOR}}$	This input from the Data Set generates an interrupt when made low with Data Terminal Ready in the "Off" condition.
19	$\overline{\text{MISC}}$	$\overline{\text{MISCELLANEOUS}}$	This output is controlled by a bit in the Control Register and is used as an extra programmable signal.
20	V_{SS}		Ground.
21	V_{CC}		+5V
23	$\overline{\text{MR}}$	$\overline{\text{MASTER RESET}}$	The Control and Status Registers and other controls are cleared when this input is low.
27	RDATA (BB)	RECEIVED DATA	This input receives serial data into the ASTRO.
28	$\overline{\text{DSR}}$ ($\overline{\text{CC}}$)	$\overline{\text{DATA SET READY}}$	This input generates an interrupt when going On or Off while the Data Terminal Ready signal is On. It appears as a bit in the Status Register.
29	$\overline{\text{CARR}}$ ($\overline{\text{CF}}$)	$\overline{\text{CARRIER DETECTOR}}$	This input from the Data Set generates an interrupt when going On or Off if Data Terminal Ready is On. It appears as a bit in the Status Register.

PIN DESCRIPTION (CONTINUED)

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
30-33	R1-R4	CLOCK RATES	These four inputs accept four different local 32X data rate Transmit and Receive clocks. The input on R4 may be divided down into a 32X clock from a 32X, 64X, 128X, or 256X clock input. The clock used in the ASTRO is selected by the control Register.
34	$\overline{IXRC}$ ($\overline{DD}$)	$\overline{RECEIVER\ TIMING}$	This input is the Receiver 1X Data Rate Clock. Its use is selected by the Control Register. The Received Data is sampled by the ASTRO on the positive transition of this signal.
35	$\overline{IXTC}$ ($\overline{DB}$)	$\overline{TRANSMITTER\ TIMING}$	This input is the Transmitter 1X Data Rate Clock. Its use is selected by the Control Register. The transmitted data changes on the negative transition of this signal.
36	$\overline{CTS}$ ($\overline{CB}$)	$\overline{CLEAR\ TO\ SEND}$	This input, when low, enables the transmitter section of the ASTRO.
37	TDATA (BA)	TRANSMITTED DATA	This output is the transmitted serial data from the ASTRO. This output is held in a Marking condition when the transmitter section is not enabled.
38	$\overline{RTS}$ ($\overline{CA}$)	$\overline{REQUEST\ TO\ SEND}$	This output is enabled by the Control Register and remains in a low state during transmitted data from the ASTRO.
39	$\overline{RE}$	$\overline{READ\ ENABLE}$	This signal, when low, gates the contents of an addressed register from a selected ASTRO onto the DAL bus.
40	V_{DD}		+ 12V



UC1671 BLOCK DIAGRAM

RECEIVER REGISTER — This 8-bit shift register inputs the received data at a clock rate determined by the Control Register. The incoming data is assembled to the selected character length and then transferred to the Receiver Holding Register with logic zeroes filling out any unused high-order bit positions.

RECEIVER HOLDING REGISTER — This 8-bit parallel buffer register presents assembled receiver characters to the DAL bus lines when requested through a Read operation.

COMPARATOR — The 8-bit comparator is used in the Synchronous mode to compare the assembled contents of the Receiver Register and the SYN register or DLE register. A match between the registers sets up stripping of the received character, when programmed, by preventing the data from being loaded into the Receiver Holding Register. A bit in the Status Register is set when stripping is performed. The comparator output also enables character synchronization of the Receiver on two successive matches with the SYN register.

SYN REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the synchronization code used to establish receiver character synchronization. It serves as a fill character when no new data is available in the Transmitter Holding Register during transmission. This register cannot be read onto the DAL lines. It must be loaded with logic zeroes in all unused high-order bits.

DLE REGISTER — This 8-bit register is loaded from the DAL lines by a Write operation and holds the "DLE" character used in the Transparent mode of operation in which an idle transmit period is filled with the combination DLE-SYN pair of characters rather than a single SYN character. In addition the ASTRO may be programmed to force a single DLE character prior to any data character transmission while in the transmitter transparent mode.

TRANSMITTER HOLDING REGISTER — This 8-bit parallel buffer register holds parallel transmitted data transferred from the DAL lines by a Write operation. This data is transferred to the Transmitter Register when the transmitter section is enabled and the Transmitter Register is ready to send new data.

TRANSMITTER REGISTER — This 8-bit shift register is loaded from the Transmitter Holding Register, SYN register, or DLE register. The purpose of this register is to serialize data and present it to the transmitted Data output.

CONTROL REGISTERS — There are two 8-bit Control Registers which hold device programming signals such as mode selection, clock selection, interface signal control, and data format. Each of the Control Registers can be loaded from the DAL lines by a Write operation or read onto the DAL lines by a Read operation. The registers are cleared by a Master Reset.

STATUS REGISTER — This 8-bit register holds information on communication errors, interface data register status, match character conditions, and communication equipment status. This register may be read onto the DAL lines by a Read operation.

DATA ACCESS LINES — The DAL is an 8-bit bidirectional bus port over which all address, data, control, and status transfers occur. In addition to transferring data and control words the DAL lines also transfer information related to addressing of the device, reading and writing requests, and interrupting information.

ASTRO OPERATION

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a Start bit (logic low) at the beginning of a character and a Stop bit (logic high) at the end of a character. Reception of a character is initiated on recognition of the first Start bit by a positive transition of the receiver clock, after a preceding Stop bit. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character or parity bit. If this bit is a logic high, the character is determined to have correct framing and the ASTRO is prepared to receive the next character. If the Stop bit is a logic low the Framing Error Status flag is set and the Receiver assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still a logic low when sampled at the theoretical center of the assumed

Start bit. As long as the Receive input is spacing, all zero characters are assembled and error flags and data received interrupts are generated so that line breaks can be determined. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received logic high is determined as a Stop bit and this resets the Receiver circuit to a Ready state for assembly of the next character.

In the Asynchronous mode the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the Insertion of a Start bit, followed by the serial output of the character least significant bit first with parity, if enabled, following the most significant bit; then the insertion of a 1-, 1.5-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Mark (logic high) condition is continually transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1.5-, or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization Character Code (SYN) transmitted at the beginning of a block of characters. The Receiver, when enabled, searches for two continuous characters matching the bit pattern contained in the SYN register. During the time the Receiver is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver assembles subsequent bits into characters whose length is determined by contents of the Control Register. If, after the first SYN character detection, a second SYN character is present, the Receiver enters the Synchronization mode until the Receiver Enable Bit is turned off. If a second successive SYN character is not found, the Receiver reverts back to the Search mode.

In the Synchronous mode a continuous stream of characters are transmitted once the Transmitter is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Nontransparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transparent mode of operation.

DETAILED OPERATION

Receiver — The Receiver Data input is clocked into the Receiver Register by a 1X Receiver Clock from a modem Data Set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Receiver Data is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receive Sampling Clock is phased to the Mark-To-Space transition of the Received Data Start bit and defines, through clock counts, the center of each received Data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode the Sampling Clock is phased to all Mark-To-Space transitions of the Received Data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the Sampling Clock by 1/32nd of a bit period. The Sampling Clock can be immediately phased to every Mark-To-Space Data transition by setting Bit 4 of Control Register 1 to a logic high, while the Receiver is disabled.

When the complete character has been shifted into the Receiver Register it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time the Receiver Status bits (Framing Error/Sync Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in the Control Register. Overrun Error is set if the Data Received status bit is not cleared through a

Read operation by an external device when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE register are not loaded into the Receiver Holding Register, and the DR interrupt is not generated, if Bit 3 of Control Register 2 (CR23 = SYN Strip) or Bit 4 of Control Register 1 (CR14 = DLE Strip) are set respectively, the SYN-DET and DLE-DET status bits are set with the next non SYN or DLE character. When both CR23 and CR14 are set (Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received only the first DLE character is stripped. No parity check is made while in this mode.

Transmitter — Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter is not enabled. Transmission of data is initiated only when the Request To Send bit is set to a logic one in the Control Register and the Clear To Send input is a logic low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (Bit 5 = Force DLE and 6 = TX Transparent Control Register 1 set to a logic one). The control bit CR15 must be set prior to loading of a new character in the transmitter holding register to insure forcing the DLE character prior to transmission of the data character. The Transmitter Register output passes through a flip-flop which delays the output by one clock period. When using the 1X clock generated by the Modem Data Set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock the transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register empty flag such that transmission of characters occurs within two data bit times of the loading of the Transmitter Holding Register when the Transmitter Register is empty.

When the Transmitter is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character the Transmitter enters an idle state. During this idle time a logic high will be presented to the Transmitted Data output in the Asynchronous mode or the contents of the SYN register will be presented in the Synchronous Non-transparent mode (CR16 = 0). In the Synchronous Transmit Transparent mode (enabled by Bit 6 of Control Register 1 = Logic 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transparent mode the DLE-SYN fill will not occur until the first forced DLE.

If the Transmitter section is disabled by a reset of the Request to Send, any partially transmitted character is completed before the transmitter section of the ASTRO is disabled. As soon as the CTS goes high the transmitted data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitted Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transparency mode.

DEVICE PROGRAMMING

The two 8-bit Control Registers of the ASTRO determine the operative conditions of the ASTRO chip. Control Register 1 is shown in the following table.

BIT 7 7	6	5	4	3	2	1	0
SYNC/ASYNC 0—LOOP MODE 1—NORMAL MODE	ASYNC 0—NON BREAK MODE 1—BREAK MODE SYNC 0—NON TRANSMITTER TRANSPARENT MODE 1—TRANSMIT TRANSPARENT MODE	ASYNC (TRANS. ENABLED) 0—1 1/2 or 2 STOP BIT SELECTION 1—SINGLE STOP BIT ASYNC (TRANS. DISABLED) 0—$\overline{\text{MISC OUT}}$ RESET 1—$\overline{\text{MISC OUT}}$ SET SYNC (CR16 = 0) 0—NO PARITY GENERATED 1—TRANSMIT PARITY ENABLED SYNC (CR16 = 1) 0—NO FORCE DLE 1—FORCE DLE	ASYNC 0—NON ECHO MODE 1—AUTO ECHO MODE SYNC (CR12 = 1) 0—DLE STRIPPING NOT ENABLED 1—DLE STRIPPING ENABLED SYNC (CR12 = 0) 0—$\overline{\text{MISC}}$ RESET 1—$\overline{\text{MISC}}$ SET	ASYNC 0—NO PARITY ENABLED 1—PARITY CHECK ENABLED ON RECEIVER PARITY GENERATION ENABLED ON TRANSMITTER SYNC 0—RECEIVER PARITY CHECK IS DISABLED 1—RECEIVER PARITY CHECK IS ENABLED	SYNC/ASYNC 0—RECEIVER DISABLED 1—RECEIVER ENABLED	SYNC/ASYNC 0—$\overline{\text{RTS}}$ RESET 1—$\overline{\text{RTS}}$ SET	SYNC/ASYNC 0—$\overline{\text{DTR}}$ RESET 1—$\overline{\text{DTR}}$ SET

CONTROL REGISTER 1

Control Register 1

Bit 7 — A logic 0 configures the ASTRO into an Internal Data and Control Loop mode and disables the Ring interrupt. In this diagnostic mode the following loops are connected internally:

a. The Transmit Data is connected to the Receive Data with the TD pin held in a Mark condition and the input to the RD pin disregarded.

b. With a 1X clock selected, the Transmitter Clock also becomes the Receive Clock.

c. The Data Terminal Ready ($\overline{\text{DTR}}$) is connected to the Data Set Ready ($\overline{\text{DSR}}$) input, with the $\overline{\text{DTR}}$ output in held in an Off condition (logic high), and the $\overline{\text{DSR}}$ input pin is disregarded.

d. The Request to Send Control bit is connected to the Clear To Send ($\overline{\text{CTS}}$) and Carrier Detector inputs, with the $\overline{\text{RTS}}$ output pin held in an Off condition (logic high), and the $\overline{\text{CTS}}$ and Carrier Detector input pins are disregarded.

3. The Miscellaneous pin is held in an Off (logic high) condition.

A logic 1 on Bit 7 enables the Ring interrupt and returns the ASTRO to the normal full duplex configuration.

Bit 6 — In the *Asynchronous* mode a logic 1 holds the Transmitted Data output in a Spacing (Logic 0) condition, starting at the end of any current transmitted character, when the Transmitter is enabled. Normal Transmitter timing continues so that this Break condition can be timed out after the loading of new characters into the Transmitter Holding Register.

In the *Synchronous* mode a logic 1 sets the Transmitter in a transparent transmission which implies that idle transmitter time will be filled by DLE-SYN character transmission and a DLE can be forced ahead of any character in the Transmitter Holding Register when CR15 is a logic one in the sync mode.

Bit 5 — In the *Asynchronous* mode a logic 1, with the Transmitter enabled, causes a single Stop bit to be transmitted. A logic 0 causes 2-Stop bit transmission for character lengths of 6, 7, or 8 bits and one-and-a-half Stop bits for a character length of 5 bits.

With the Transmitter disabled this bit controls the Miscellaneous output on Pin 19, which may be used for Make Busy on 103 Data Sets, Secondary Transmit on 202 Data Sets, or dialing on CBS Data Couplers.

In the *Synchronous* mode a logic 1 combined with a logic 0 on Bit 6 of control Register 1 enables Transmit parity; if CR15 = 0 or CR15 = 1 no parity is generated. When set to a logic 1 with Bit 6 also a logic 1, the contents of the DLE register are transmitted prior to the next character loaded in the Transmitter Holding Register as part of the Transmit Transparent mode.

Bit 4 — In the *Asynchronous* mode a logic 1 enables the Automatic Echo mode when the receiver section is enabled. In this mode the clocked regenerated data is presented to the Transmit Data output in place of normal transmission through the Transmitter Register. This serial method of echoing does not present any abnormal restrictions on the transmit speed of the terminal. Only the first character of a Break condition of all zeroes (null character) is echoed when a Line Break condition is detected. For all subsequent null characters, with logic zero Stop bits, a steady Marking condition is transmitted until normal character reception resumes. Echoing does not start until a character has been received and the Transmitter is idle. The Transmitter does not have to be enabled during the Echo mode.

In the *Synchronous* mode a logic 1, with the Receiver enabled, does not allow assembled Receiver data matching the DLE register contents to be transferred to the Receiver Holding Register; also, parity checking is disabled.

When the Receiver is not enabled this bit controls the Miscellaneous output on Pin 19, which may be used for New Sync on a 201 Data Set. When operating with a 32X clock and a disabled Receiver a logic 1 on this bit also causes the Receiver timing to synchronize on Mark-To-Space transitions.

Bit 3 — In the *Asynchronous* mode a logic 1 enables check of parity on received characters and generation of parity for transmitted characters.

In the *Synchronous* mode a logic 1 bit enables check of parity on received characters only. **Note:** Transmitter parity enable is controlled by CR15.

Bit 2 — A logic 1 enables the ASTRO to receive data into the Receiver Holding Register, update Receiver Status Bits 1, 2, 3, and 4, and to generate Data Received interrupts. A logic 0 disables the Receiver and clears the Receiver Status bits.

Bit 1 — Controls the $\overline{\text{Request To Send}}$ output on Pin 38 to control the CA circuit of the Data Set. The $\overline{\text{RTS}}$ output is inverted from the state of CR11. A logic 1 combined with a low logic $\overline{\text{Clear To Send}}$ input enables the Transmitter and allows THRE interrupts to be generated. A logic 0 disables the Transmitter and turns off the external $\overline{\text{Request To Send}}$ signal. Any character in the Transmitter Register will be completely transmitted before the Transmitter is turned off. The Request To Send output may be used for other functions such as "Make Busy" on 103 Data Sets.

Bit 0 — Controls the $\overline{\text{Data Terminal Ready}}$ output on Pin 16 to control the CD circuit of the Data Set. A logic 1 enables the Carrier and Data Set Ready interrupts. A logic 0 enables only the telephone line Ring interrupt. The $\overline{\text{DTR}}$ output is inverted from the state of CR10.

Control Register 2

Control Register 2, unlike Control Register 1, cannot be changed at any time. This register should be changed only while both the receiver and transmitter sections of the ASTRO are in the idle state.

Bits 7-6 — These bits select the character length as follows:

Bits 7-6	Character Length
00	8 bits
01	7 bits
10	6 bits
11	5 bits

When parity is enabled it must be considered as a bit when making character length selection, i.e. 5 character bits plus parity = 6 bits.

Bit 5 — A logic 1 selects the Synchronous Character mode. A logic 0 selects the Asynchronous Character mode.

Bit 4 — A logic 1 selects odd parity and a logic 0 selects even parity, when parity is enabled by CR13 and/or CR15.

Bit 3 — In the *Asynchronous* mode a logic 0 selects the rate 1(-32X) clock input (pin 30) as the Receiver Clock rate and a logic 1 selects the same clock rate for the Receiver as selected by Bits 2-0 for the Transmitter. This bit must be a logic 1 for the 1X clock selection by Bits 2-0.

In the *Synchronous* mode a logic 1 causes all DLE-SYN combination characters in the Transparent mode when DLE strip CR14 is a logic 1, or all SYN characters in the Non-transparent mode to be stripped and no Data Received interrupt to be generated. The SYN Detect status bit is set with reception of the next assembled character as it is transferred to the Receiver Holding Register.

Bits 2-0 — These bits select the Transmit and Receive clocks. The Input Clock to the Rate 4 pin may be divided down to form the 32X clock from a multiple clock as shown:

Bits 2-0	Clock
000	1X clock for Transmit and Receive (Pins 35 and 34 respectively)
001	32X clock — Rate 1 input (Pin 30)
010	32X clock — Rate 2 input (Pin 31)
011	32X clock — Rate 3 input (Pin 32)
100	32X clock — Rate 4 input ÷ 1 (Pin 33)
101	32X clock — Rate 4 input ÷ 2 (Pin 33)
110	32X clock — Rate 4 input ÷ 4 (Pin 33)
111	32X clock — Rate 4 input ÷ 8 (Pin 33)

BIT 7 6	5	4	3	2 1 0
SYNC/ASYNC CHARACTER LENGTH SELECT 00 = 8 BITS 01 = 7 BITS 10 = 6 BITS 11 = 5 BITS	MODE SELECT 0—ASYNCHRONOUS MODE 1—SYNCHRONOUS MODE	SYNC/ASYNC 1—ODD PARITY SELECT 0—EVEN PARITY SELECT	ASYNC 1—RECEIVER CLOCK DETERMINED BY BITS 2-0 0—RECEIVER CLK = RATE 1 SYNC (CR14 = 0) 0—NO SYN STRIP 1—SYN STRIP SYNC (CR14 = 1) 0—NO DLE-SYN STRIP 1—DLE-SYN STRIP	SYNC/ASYNC CLOCK SELECT 000 - IX CLOCK 001 - RATE 1 CLOCK 010 - RATE 2 CLOCK 011 - RATE 3 CLOCK 100 - RATE 4 CLOCK 101 - RATE 4 CLOCK ÷ 2 110 - RATE 4 CLOCK ÷ 4 111 - RATE 4 CLOCK ÷ 8

CONTROL REGISTER 2

Status Register

The data contained in the Status Register define Receiver and Transmitter data conditions and status of the Data Set. The Status word is shown and defined below.

Bit 7 — This bit is set to a logic 1 whenever there is a change in state of the Data Set Ready or Carrier Detector inputs while Data Terminal Ready (Bit 0 of Control Register 1) is a logic 1 or the Ring Indicator is turned on, with DTR a logic 0. This bit is cleared when the Status Register is read onto the Data Access Lines.

Bit 6 — This bit is the logic complement of the Data Set Ready input on Pin 28. With 202-type Data Sets it can be used for Secondary Receive.

Bit 5 — This bit is the logic complement of the Carrier Detector input on Pin 29.

Bit 4 — In the *Asynchronous* mode a logic 1 indicates that received data contained a log 0 bit after the last data bit of the character in the stop bit slot, while the Receiver was enabled. This indicates a Framing error. This bit is set to a logic 0 if the proper logic 1 condition for the Stop bit was detected.

In the *Synchronous* mode a logic 1 indicates that the contents of the Receiver Register matched the contents of the SYN Register. The condition of this bit remains for a full character assembly time. If SYN strip (CR23) is enabled this status bit is updated with the character received after the SYN character. In both modes the bit is cleared when the Receiver is disabled.

Bit 3 — When the DLE Strip is enabled (Bit 4 of Control Register 1) the Receiver parity check is disabled and this bit is set to a logic 1 if the *previous character* to the presently assembled character matched the contents of the DLE register; otherwise it is cleared. The DLE DET remains for one character time and is reset on the next character transfer or on a Status Register Read. If DLE Strip is not enabled, this bit is set to a logic 1 when the Receiver is enabled, Receiver parity (Bit 3 of Control Register 1) is also enabled, and the last received character has a Parity error. A logic 0 on this bit indicates correct parity. This bit is cleared in either of the above modes when the Receiver is disabled.

Bit 2 — A logic 1 indicates an Overrun error which occurs if the previous character in the Receiver Holding Register has not been read and Data Received is not reset, at the time a new character is to be transferred to the Receiver Holding Register. This bit is cleared when no Overrun condition is detected, i.e., the next character transfer time or when the Receiver is disabled.

Bit 1 — A logic 1 indicates that the Receiver Holding Register is loaded from the Receiver Register, if the Receiver is enabled. It is cleared to a logic 0 when the Receiver Holding Register is read onto the Data Access Lines, or the Receiver is disabled.

Bit 0 — A logic 1 indicates that the Transmitter Holding Register does not contain a character while the Transmitter is enabled. It is set to a logic 1 when the contents of the Transmitter Holding Register is transferred to the Transmitter Register. It is cleared to a 0 bit when the Transmitter Holding Register is loaded from the DAL, or when the Transmitter is disabled.

INPUT/OUTPUT OPERATIONS

All Data, Control, and Status words are transferred over the Data Access Lines (DAL 0-7). Additional input lines provide controls for addressing a particular unit, and regulating all input and output operations. Other lines provide interrupt capability to indicate to a Controller that an input operation is requested by the ASTRO. All input/output terminology below is referenced to the Controller so that a Read or Input takes data from the ASTRO and places it on the DAL lines, while a Write or Output places data from the DAL lines into the ASTRO. Bit 0 (DALO) must be a logic low in a Read or Write operation.

Read

A Read Operation is initiated by the placement of an *eight-bit address* on the DAL by the Controller. When the Chip Select signal goes to a logic low state, the ASTRO compares Bits 7-3 of the DAL with its hardwired ID code (Pins 17, 22, 24, 25, and 26) and becomes selected on a Match condition. The ASTRO then sets its REPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to read from as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	Status Register
110	Receiver Holding Register

BIT 7	6	5	4	3	2	1	0
• DATA SET CHANGE	• DATA SET READY	• CARRIER DETECTOR	• FRAMING ERROR • SYN DETECT	• DLE DETECT • PARITY ERROR	• OVERRUN ERROR	• DATA RECEIVED	• TRANSMITTER HOLDING REGISTER EMPTY

STATUS REGISTER

When the Read Enable (RE) line is set to a logic low condition by the Controller the ASTRO gates the contents of the addressed register onto the DAL. The Read operation terminates, and the devices becomes unselected, when both the Chip Select and Read Enable return to a logic high condition. Reading of the Receiver Holding Register clears the DR Status bit.

Write

A Write operation is initiated by the placement of an eight-bit address on the DAL by the Controller. The ASTRO compares Bits 7-3 of the DAL with its ID code when the Chip Select input goes to a logic low state. If a Match condition exists, the device is selected and makes it's RPLY line low to acknowledge its readiness to transfer data. Bits 2-0 of the address are used to select ASTRO registers to be written into as follows:

Bits 2-0	Selected Register
000	Control Register 1
010	Control Register 2
100	SYN and DLE Register
110	Transmitter Holding Register

When the Write Enable (WE) line is set to a logic low condition by the Controller the ASTRO gates the data from the DAL into the addressed register. If data is written into the Transmitter Holding Register, the THRE Status bit is cleared to a logic zero.

The 100 address loads both the SYN and DLE registers. After writing into the SYN register the device is conditioned to write into the DLE if followed by another Write pulse with the 100 address. Any intervening Read or Write operation with other addresses resets this condition such that the next 100 will address the SYN register.

Interrupts

The following conditions generate interrupts:

1. **Data Received (DR) —** Indicates transfer of a new character to the Receiver Holding Register while the Receiver is enabled.
2. **Transmitter Holding Register Empty (THRE) —** Indicates that the THR register is empty while the Transmitter is enabled. The first interrupt occurs when the Transmitter becomes enabled if there is an empty THR, or after the character is transferred to the Transmitter Register making the THR empty.
3. **Carrier On —** Indicates Carrier Detector input goes low when DTR is on.
4. **Carrier Off —** Indicates Carrier Detector input goes high when DTR is on.
5. **DSR On —** Indicates the Data Set Ready input goes low when DTR is on.
6. **DSR Off —** Indicates the Data Set Ready input goes high when DTR is on.
7. **Ring On —** Indicates the Ring Indicator input goes low when DTR is off.

Each time an Interrupt condition exists the INTR output from the ASTRO is made a logic low. The following interrupt procedure is then carried out even if the interrupt condition is removed.

The Controller acknowledges the Interrupt request by setting the Chip Select (CS) and the Interrupt Acknowledge Input (IACKI) to the ASTRO to a Low state. On this transition all non-interrupting devices receiving the IACKI set their Interrupt Acknowledge Output (IACKO) low, enabling lower priority daisy-chained devices to respond to the Interrupt request. The highest priority device that is interrupting will then set its RPLY low. This device places its ID code on Bit Positions 7-3 of the DAL when a low RE signal is received. In addition Bit 2 is set to a logic one if any of the interrupt numbers 1 and 3-7 above occurred, and remains a logic zero if the THRE has caused the interrupt.

To reset the Interrupt condition (INTR) Chip Select (CS) and (IACKI) must be received by the ASTRO. A setup time must exist between CS and the RE or WE signals to allow chip selection prior to read/write operations and deselection control through the latter signals. The data is removed from the DAL when the RE signal returns to the logic high state.

MAXIMUM RATINGS

V_{DD} With Respect to V_{SS} (Ground)		+20 to −0.3V
Max Voltage To Any Input With Respect to V_{SS}		+20 to −0.3V
Operating Temperature		0°C to 70°C
Storage Temperature	Plastic	−55°C to +125°C
	Ceramic	−65°C to +150°C
Power Dissipation		1000 mW

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

OPERATING CHARACTERISTICS

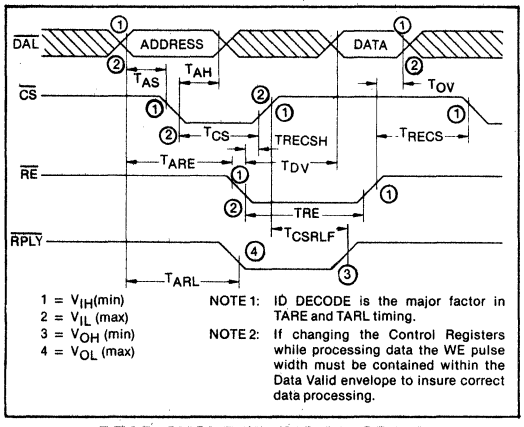
T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{SS} = 0V, V_{CC} = +5V ±5%

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current			1	mA	$V_{BB} = -5V$
I_{CCAVE}	V_{CC} Supply Current			80	mA	
I_{DDAVE}	V_{DD} Supply Current			10	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	$I_O = -100\,\mu A$
V_{OL}	Output Low Voltage			.45	V	I_O = 1.6 mA

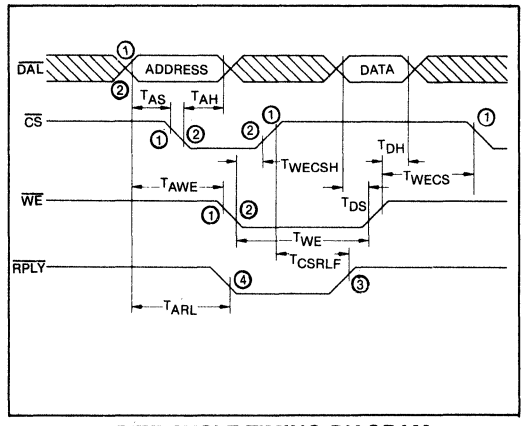
AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ±5%, V_{BB} = −5.0V ±5%, V_{CC} = +5.0 ±5%, V_{SS} = 0V
CL_{MAX} = 20 pf

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{AS}	Address Set-Up Time	0			ns	
t_{AH}	Address Hold Time	150			ns	
T_{ARL}	Address to $\overline{RPLY}$ Delay			400	ns	
T_{CS}	$\overline{CS}$ Width	250			ns	
T_{CSRLF}	$\overline{CS}$ to Reply OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{MR}	MR Width	1.0			μs	
READ						
T_{ARE}	Address and $\overline{RE}$ Spacing	250			ns	
T_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{DV}	$\overline{RE}$ to Data Out Delay			180	ns	C_L = 20 pf
T_{OV}	$\overline{RE}$ Off to DAL Open Delay	20		250	ns	
T_{RE}	$\overline{RE}$ Width	200		1000	ns	
WRITE						
T_{AWE}	Address to $\overline{WE}$ Spacing	250			ns	
T_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	20			ns	
T_{WE}	$\overline{WE}$ Width	200		1000	ns	
T_{DS}	Data Set-Up Time	150			ns	
T_{DH}	Data Hold Time	100			ns	
T_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	250			ns	



READ CYCLE TIMING DIAGRAM

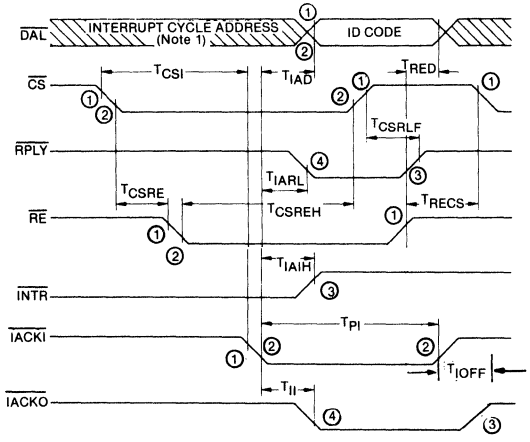


WRITE CYCLE TIMING DIAGRAM

INTERRUPT

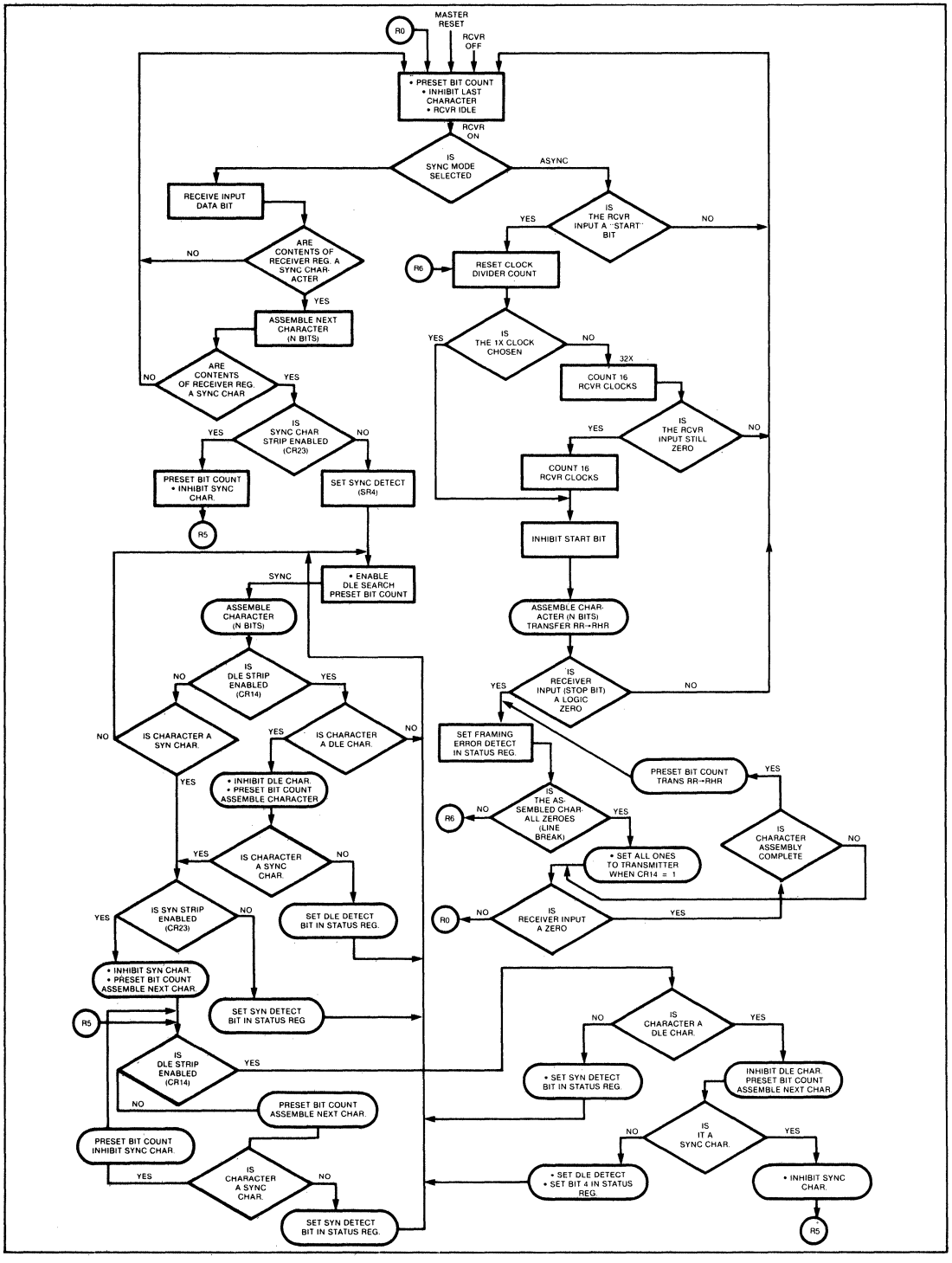
	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
T_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	0			ns	
T_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	250			ns	
T_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	20			ns	
T_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	250			ns	
T_{PI}	$\overline{IACKI}$ Pulse Width	200			ns	
T_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay			250	ns	See Note 1.
T_{OV}	$\overline{RE}$ OFF to $\overline{DAL}$ Open Delay	20		250	ns	
T_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay			250	ns	
T_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ OFF Delay	0		250	ns	R_L = 2.7 KΩ
T_{IAIH}	$\overline{IACKI}$ ON to $\overline{INTR}$ OFF Delay			300	ns	
T_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay			200	ns	
T_{IOFF}	$\overline{IACKO}$ OFF Delay From $\overline{CS}$ OFF, $\overline{RE}$ OFF, or $\overline{IACKI}$ HIGH.			250	ns	See Note 2.

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.
Note 2: $\overline{IACKO}$ goes false after the last one of the following three signals go false: $\overline{CS}$, $\overline{RE}$ and $\overline{IACKI}$. T_{IOFF} is measured from the last signal going false.

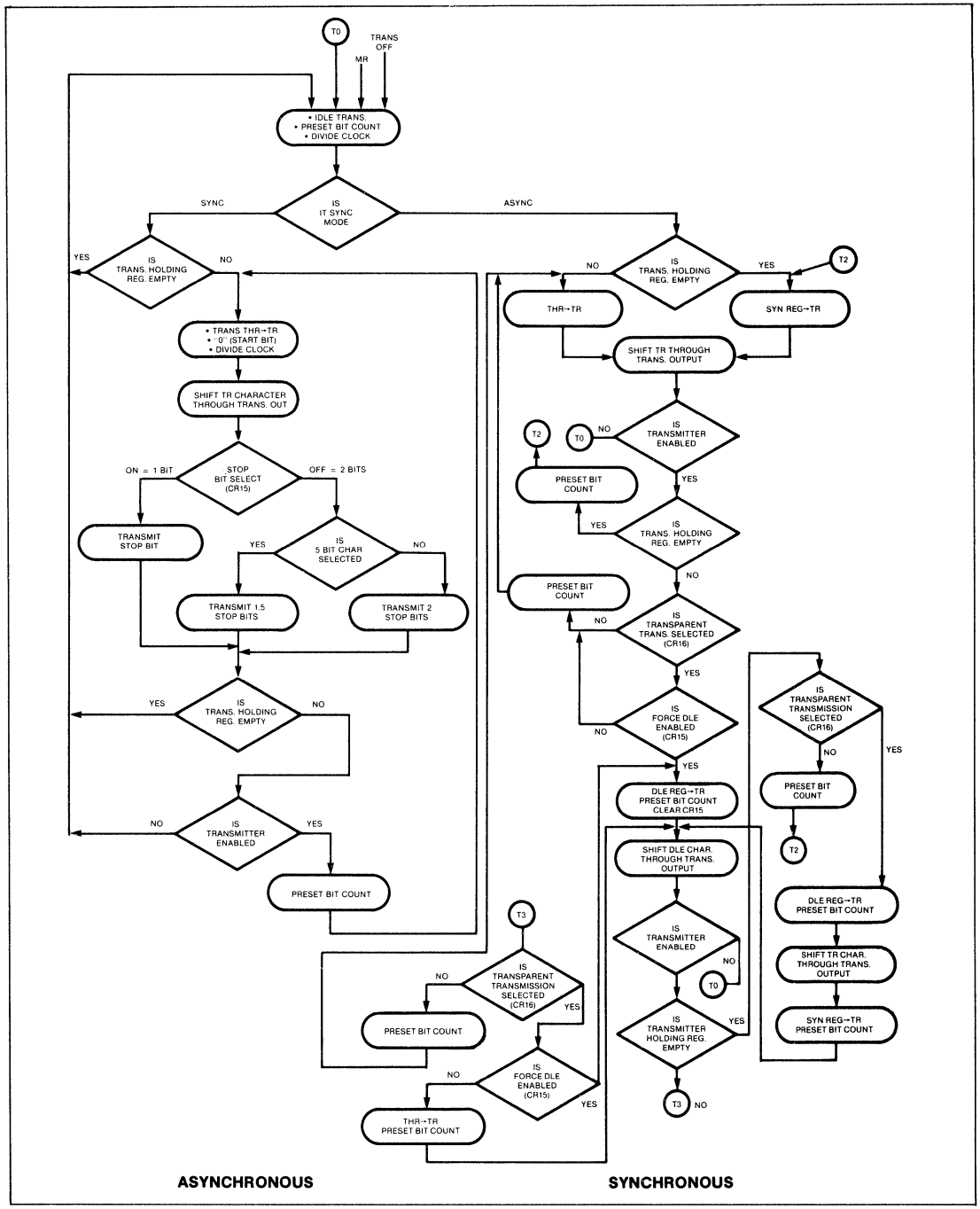


Note 1: $\overline{DAL0}$ must be a logic low during $\overline{CS}$ to form an Interrupt Cycle Address during Daisy Chain Interrupt Response.

INTERRUPT CYCLE TIMING DIAGRAM



RECEIVER SECTION



TRANSMITTER SECTION

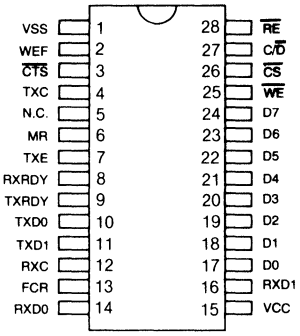
See page 383 for ordering information.

FINAL

WD1993 Arinc 429 Receiver/Transmitter and Multi-Character Receiver/Transmitter

FEATURES

- PRESENT UPON MASTER RESET FOR ARINC 429 PROTOCOL
- RETURN TO ZERO (RZ) OUTPUT
- AUTO SPACE GENERATION
- DOUBLE BUFFERED RECEIVER AND TRANSMITTER
- UNDERRUN ERROR DETECTION FOR TRANSMISSION
- OVERRUN, FRAMING AND PARITY ERROR DETECTION ON RECEIVER
- WORD ERROR FLAG FOR COMPREHENSIVE ERROR REPORTING
- FIRST CHARACTER OF WORD FLAG FOR SINGLE INTERRUPT APPLICATIONS
- DIAGNOSTIC LOCAL LOOP-BACK TEST MODE
- DC TO 200 KILOBITS PER SECOND OPERATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- SINGLE +5 VOLT SUPPLY
- TEMPERATURE RANGES 0°C to 70°C, — 1993-03, −40°C to +85°C — 1993-02, −55°C to +125°C — 1993-01



PIN DESIGNATION

DESCRIPTION

The Western Digital WD1993 Avionic Receiver/Transmitter is designed to handle digital data transmission, according to the Avionic Arinc 429 protocol.

Parallel data is converted into a serial data stream during transmission and serial to parallel during reception. The WD1993 is packaged in a 28 pin plastic or ceramic package and is available in three temperature ranges: Commercial, Industrial and Military.

The WD1993 is a bus-orientated MOS/LSI device designed to provide the Avionics Arinc 429 Data Communication Protocol.

Also, the WD1993 contains a local loop-back test mode of operation, which is controlled by the Loop Test Enable (LTE) bit in the command register. In this diagnostic mode, the transmitter output is "looped-back" into the receiver input. The REN and TEN control bits must also be active ("1") and the CTS input must be low. The status and output flags operate normally.

PIN DESCRIPTION

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
1	VSS	GROUND	Ground
2	WEF *	WORD ERROR FLAG	This pin is an output, which when active indicates an error in either the transmitter or receiver has been detected. It reflects an underrun, overrun, parity or framing (receive word) error and is intended as an error interrupt. The Status Register should be read to determine the specific error.
3	$\overline{CTS}$	CLEAR-TO-SEND	This input is activated (V_{IL}) to enable the transmitter logic.
4	TXC	TRANSMIT CLOCK	This input is the source clock for transmission. The data rate is a function of this clock frequency. ARINC MODE = 4 × bit rate
5	EGND	EXTERNAL GROUND	Requires external ground for proper operation.
6	MR	MASTER RESET	When active (V_{IH}), presets the WD1993 mode and command registers to the ARINC protocol. Master Reset also resets the data registers and places the WD1993 transmitter and receiver into idle states. After MR, the command register is set to 00100101 and the mode register is set to 00111100.
7	TXE	TRANSMITTER EMPTY	This output goes high to indicate the end of a transmit operation. TXE is automatically reset after the Transmit Holding Register is loaded.
8	RXRDY	RECEIVER READY	This output, when high, alerts the CPU that the Receiver Holding Register contains a data character that is ready to be input. This output is automatically reset whenever a character is read from the WD1993. RXRDY is enabled unless inhibited by setting command bit CR3 (RXRDYIN) to a logic "1." It is automatically enabled again after a receive sequence is completed.
9	TXRDY	TRANSMITTER READY	This output, when high, alerts the CPU that the Transmit Holding Register is ready to accept a data character. The TXRDY output is automatically reset whenever a character is written into the WD1993 and can be used as an interrupt to the system.
10	TXD0	TRANSMIT DATA ZERO	This output drives the V/Z circuit when á logic zero is to be transmitted and is active for one-half bit time.
11	TXD1	TRANSMIT DATA ONE	This output drives the V/Z circuit when a logic one is to be transmitted and is active for one-half bit time.

* The following operation must be performed to clear the error in the Status Register and de-assert the Word Error Flag
1. Perform a Master Reset (MR) or;
2. Transfer a new character to the Receiver Holding Register after a reload of the Receiver Register.

PIN DESCRIPTION (CONTINUED)

PIN NO.	SIGNAL MNEMONIC	SIGNAL NAME	FUNCTION
12	RXC	RECEIVE CLOCK	This input is the source clock for reception. The data rate characteristics are the same as the transmit clock.
13	FCR	FIRST CHARACTER READY	This output goes high after the receiver has completed reception of the first character in a multi-character sequence.
14	RXD0	RECEIVE DATA ZERO	RXD0 is driven by the line V/Z receiver circuit. When the V/Z circuit detects a logic zero, a TTL logic one (active for one-half bit time) is provided to the WD1993.
15	VCC	POWER SUPPLY	+5V DC
16	RXD1	RECEIVE DATA ONE	The RXD1 input is driven by the V/Z line receiver. Each time the V/Z circuit detects a logic one, a TTL level logic one (active for one-half bit time) is provided to this input.
17 18 19 20 21 22 23 24	D0 D1 D2 D3 D4 D5 D6 D7	DATA BUS	This is the bi-directional data bus. It is the means of communication between the WD1993 and the CPU. Control, Mode, Data and Status Registers are accessed via this bus.
25	$\overline{WE}$	$\overline{WRITE\ ENABLE}$	When active (V_{IL}), allows the CPU to write into the selected register.
26	$\overline{CS}$	$\overline{CHIP\ SELECT}$	When active (V_{IL}), the device is selected. This enables communication between the WD1993 and a microprocessor.
27	C/$\overline{D}$	CONTROL/$\overline{DATA}$	This input is used in conjunction with an active read or write operation to determine register access via the DATA BUS.
28	$\overline{RE}$	$\overline{READ\ ENABLE}$	When active (V_{IL}), allows the CPU to read data or status information from the WD1993.

ARCHITECTURE

A block diagram of the WD1993 is shown in Figure 1.

As mentioned, the WD1993 is an eight bit bus-oriented device. Communication between the WD1993 and the controlling CPU occurs via the 8 bit data bus through the bus transceivers. There are 2 accessible data registers, which buffer transmit and receive data. They are the Transmit Holding Register and the Receive Holding Register. There is a parallel-to-serial shift register (parallel in-serial out), the transmit register and a serial-to-parallel shift register (serial in-parallel out), the receive register.

Operational control and monitoring of the WD1993 is performed by two control registers (the command instruction register and the mode instruction register) and the status register.

A read/write control circuit allows programming/monitoring or loading/reading of data in the control, status or holding registers by activating the appropriate control lines: Chip Select ($\overline{CS}$), Read Enable ($\overline{RE}$), Write Enable ($\overline{WE}$), and Control or Data Select (C/$\overline{D}$).

Internal control of the WD1993 is by means of two internal microcontrollers; one for transmit and one for receive. The control registers, null detect logic and various counters, provide inputs to the microcontrollers which generate the necessary control signals to send and receive serial data according to the Arinc 429-1 protocol, along with the programmable multicharacter capabilities.

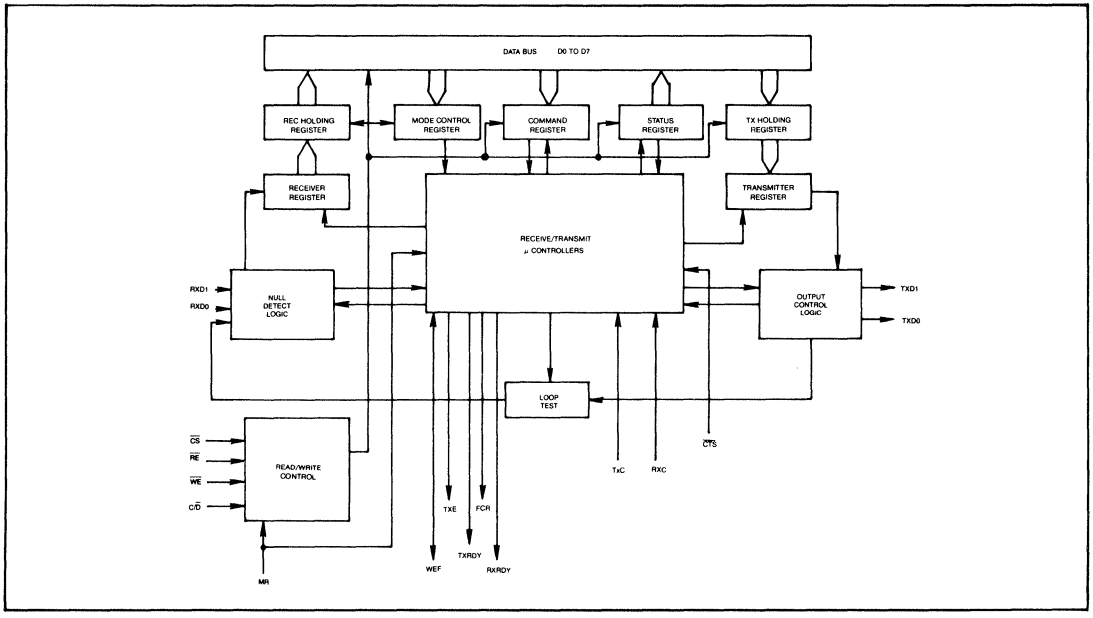


FIGURE 1. WD1993 BLOCK DIAGRAM

OPERATION

Upon master reset (MR), the device is programmed to transmit and receive four 8-bit contiguous characters with the 32nd bit inside odd parity. (ARINC protocol.)

A minimum four bit time space is automatically inserted after the character transmission. Two receiver inputs, RXD1/RXD0 and two transmitter outputs, TXD1/TXD0, are provided to interface with voltage—impedance (V/Z) circuits to translate ± 10 volt ARINC line levels to 5 volt TTL logic levels. The transmit clock (TXC) and receive clock (RXC), in ARINC mode, are four times (4X) the bit rate desired.

The receiver monitors the received data input to detect a four bit time null, which delimits the word. If the communications link is broken during a word reception, the receiver will generate a word error flag to (WEF) to notify the CPU to request retransmission. When a null is detected, the receiver logic is reset and returned to an idle state awaiting the next word.

The Command Register is used to select features such as parity options, loop test capability, RXRDY flag enabling, transmitter and receiver enabling, and may also cause the WD1993 to return to the Mode instruction.

The Status Register contains information such as Transmitter Ready, Transmitter Empty, Receiver Ready, error conditions, and First Character Ready.

OPERATING DESCRIPTION

The WD1993 is primarily designed to operate in an 8 bit micro-processor environment. The DATA BUS and the Interface Control Signals ($\overline{CS}$, $\overline{RE}$, $\overline{WE}$ and C/$\overline{D}$) should be connected to the microprocessor's data bus and system control bus.

The appropriate TXC and RXC clock frequencies should be selected for the particular application, using a programmable baud rate generator such as a WD1943. A master reset pulse initializes the WD1993 and presets the control registers to the ARINC protocol.

The RXD1/RXD0 inputs are interfaced to the DITS data line via external level translators that provide TTL (5V) logic levels to the WD1993. The TXD1/TXD0 outputs are connected to high voltage (± 10V) driver circuits. Figures 16 and 17 show some typical ± 10V translator and driver circuits.

The TXRDY, RXRDY, FCR and WEF Flags may be connected to the microprocessor system as interrupt inputs. The status register can be periodically read in a polled environment to support WD1993 operations.

The $\overline{CTS}$ input can be used to synchronize the transmitter to external events.

The WD1993 is designed such that a control register write operation accesses the command instruction register.

The RXRDYIN bit of the command register is used to inhibit the RXRDY output pin for ARINC operations.

Several "flags" are provided for interrupt purposes so that continuity is maintained and data integrity is preserved. These flags are First Character Ready (FCR), Receiver Ready (RXRDY), Transmitter Ready (TXRDY) and Transmitter Empty (TXE).

The Transmitter operates as follows:

a) With the mode and command registers programmed as desired, the transmitter is enabled, TEN (CR0) = "1".

b) The TXE and TXRDY flags are "1" (active).

c) The external $\overline{CTS}$ signal = "0".

d) The CPU loads data into the Transmitter Holding Register, TXE and TXRDY go Low.

e) When the Transmitter Holding Register has transferred its contents to the Transmitter Register for the character to be transmitted, it will activate the TXRDY (pin 9) output, to alert the CPU that the next 8-bit character can be accepted. When this new character is loaded into the Transmitter Holding Register (while the Transmitter Register is still transmitting its contents, thereby preventing the Transmitter Holding Register to transfer its character contiguously), TXRDY is not deactivated (reset low to a logic zero) when $\overline{WRITE\ ENABLE}$ ($\overline{WE}$) is deactivated (set high to a logic one), as shown by the dotted line in Figure 2. An underrun error will be generated if the next character is not loaded before the previous word is completely shifted out, unless the current character is the last character in a sequence.

However, the WD1993 will delay the deactivation of TXRDY until the end of the fourth clock or the end of a data bit being transmitted (see Figure 2).

f) If the last character is transmitted and no more new data is to be sent, the transmitter will indicate its status by raising the TXE flag. (No error is generated as a result of this condition.)

The Receiver operates similarly:

a) With the control registers suitably programmed, the receiver is enabled, REN (CR2) = "1".

b) The RXRDY and FCR flags are "0". (Inactive).

c) The incoming data word activates the receive logic and the data begins to be assembled in the Receiver Register.

d) When the first character is completely assembled in the Receiver Register, the data is loaded into the Receive Holding Register and the FCR (First Character Ready) and RXRDY (Receiver Ready) flags become active. The CPU should read the data in the Receiver Holding Register to reset the FCR and first RXRDY. If the Arinc 429 character is accepted, three more RXRDY's will be generated for the three remaining bytes of this character, i.e., every time a byte is transferred from the Receiver Register to the Receiver Holding Register (see Figure 3, Data Accepted). The CPU should read the data prior to the reception of the next character (next RXRDY) or an overrun error will be generated as the receiver will overwrite the old data with the new data character just received.

The first character in the Arinc protocol contains a label. The FCR and RXRDY Flags become active to indicate the reception of the first character of data. The CPU reads the first character and decides whether or not it wants to acquire the subsequent characters. If not, then the CPU performs a "control write" to the Command Register, setting the RXRDYIN (CR3) bit to a "1." This bit in Arinc mode should inhibit the RXRDY flag from interrupting the CPU during the reception of the 3 remaining characters. The RXRDYIN bit is then automatically reset upon completion of the receive sequence and RXRDY is enabled again (see Figure 3, Conforming Data Rejection).

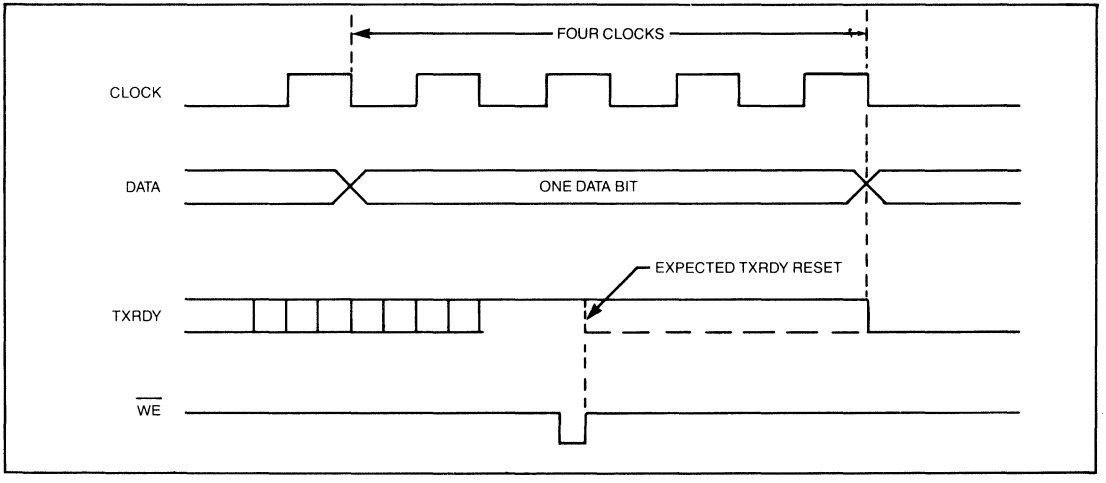


FIGURE 2

The WD1993 however generates a RXRDY after the null character (see Note), thereby conceivably misleading the CPU that a first 8 bit character (label) of the following 32 bit ARINC 429 character, has been assembled in the Receiver Register and transferred to the Receiver Holding Register, ready to be read (see Figure 3, "WD1993 Data Rejection").

A solution to overcome this misreading, is to gate (AND) the FCR and RXRDY outputs to interpret this combination as a valid RXRDY for the Label.

NOTE: A NULL character is the four bit (all zero's) character which is used in the ARINC 429 protocol to synchronize, differentiate and signify the start of the 32 bit ARINC 429 characters.

LOOP TEST MODE

As mentioned, the WD1993 is equipped with a diagnostic test mode, local loop-back. This mode is activated by setting the LTE command bit to a "1". The TEN and REN bits should be "1" and $\overline{CTS}$ should be "V_{IL}". The receiver inputs are ignored and the transmitter outputs are sending nulls. The transmitter is internally "looped-back" to the receiver and the error and status flags operate normally.

For basic testing, failing to reload the Transmit Holding Register in the middle of a data send sequence will cause an underrun error in the transmitter and a word error in the receiver. Failure to read the Receive Holding Register after a FCR or RXRDY flag will cause an overrun error to be generated.

For Loop-Back test operations, the user should be sure that the TXC and RXC clock frequencies are the same. This is normally implemented by placing the same clock signal on both pins (TXC and RXC).

ARINC BACKGROUND

Aeronautical Radio Inc. (ARINC) publishes the ARINC 429 specification. This document defines the air transport industries standards for the transfer of digital data between avionics systems elements. This specification was adopted by The Airlines Electronic Engineering Committee April 11, 1978. By the adoption of this specification the foundation is set for a standard protocol governing all intersystems equipment (Line Replaceable Units).

MARK 33 DIGITAL INFORMATION TRANSFER SYSTEM (DITS)

Basic Philosophy

Transmit from a designated output port over a single twisted and shielded pair of wires to designated receiver.

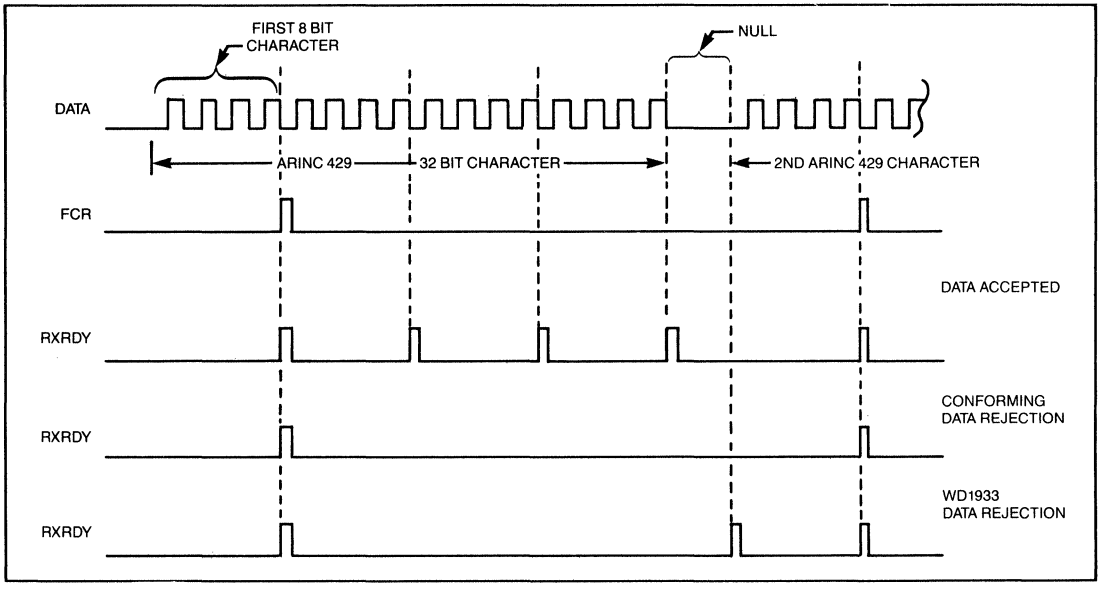


FIGURE 3

Bidirectional data flow not permitted on a given pair.

Data Transfer
Numeric
Iso Alphabet #5
Graphic

Data Format
32 bits or less (unused bit positions should be filled with binary zeros or valid data pad bits).

Bit #32 is assigned to parity.

Modulation
Return to Zero (RZ)

Transmit Voltage Levels

high	+10	±0.5V
null	0	±0.5V
low	−10	±0.5V

Receiver Voltage Levels:

	(in absence of noise)	(noisy environment)
high	+6.0V to +10V	+5.0V to +13V
low	−6.0V to +10V	−5.0V to −13V

No damage to receiver up to 20 vac rms between A & B; +28, A to Gnd; −28, B to Gnd.

Data Rate
100 kilo bit per second ± 1%
Low speed 12 to 14.5 kilo bit per second ± 1%

Word Synchronization
All zero gap of a minimum of 4 bit times

REGISTER DEFINITIONS

The format and definition of the Command Register is shown below:

CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0
NA	IR	NA	LTE	RXRDYIN	REN	NA	TEN

TEN	Transmit ENable
1	Enabled
0	Disabled

NA	Not Used

REN	Receive ENable
1	Enabled
0	Disabled

RXRDYIN	RXRDY Inhibit
1	Inhibit RXRDY output flag
0	Normal transmitter operation enable RXRDY output flag

LTE	Loop Test ENable
1	Local loop-back mode
0	Normal Operation

NA	Not Used

IR	Internal Reset
1	Returns WD1993 to mode instruction format
0	Stays in Command Register

NA	Not Used

The WD1993 registers are addressed according to the following table:

$\overline{CS}$	C/$\overline{D}$	$\overline{RE}$	$\overline{WE}$	Registers Selected
L	L	L	H	Read Receive Holding Register
L	L	H	L	Write Transmit Holding Register
L	H	L	H	Read Status Register
L	H	H	L	Write Command Register
H	X	X	X	Data Bus Tri-Stated

L = V_{IL} at pins
H = V_{IH} at pins
X = don't care

The format of the Status Register is shown below:

SR7	SR6	SR5	SR4	SR3	SR2	SR1	SR0
UE	FCR	WEF	OE	PE	TXE	RXRDY	TXRDY

TXRDY — Transmitter Ready
1 — Active (THR can be reloaded)
0 — Inactive (transmitter is busy)

RXRDY — Receiver Ready
1 — Active (RHR should be read)
0 — Inactive

TXE — Transmitter Empty
1 — Transmitter idle
0 — Transmitter active

PE — Parity Error
1 — Parity Error reported
0 — No error

OE — Overrun Error
1 — RHR has been written over with a new character before previous character was read.
0 — No error

FE — Framing Error
1 — Indicates improper receive sequence detected.
0 — No error

FCR — First Character Ready
1 — This bit indicates the receiver has just completed assembly of the 1st character in a multi-character sequence and that the data is contained in the RHR.
0 — First character not ready.

UE — Underrun Error
1 — Indicates that the THR has not been loaded with a new character in time for a contiguous data transmission sequence.
0 — No error

ABSOLUTE MAXIMUM RATINGS

Storage Temperature −55°C to +125°C (Plastic Package)
−65°C to +150°C (Ceramic Package)
Voltage on any Pin with Respect to Ground . −0.3V to +7V
Power Dissipation ..... 400 MW
Lead Temperature (soldering 10 sec) ..... 300°C

Note: Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under DC Electrical Characteristics.

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C; V_{CC} = 5.0V ± 5%; GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.45	V	I_{OL} = 1.6mA
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100μA
I_{DL}	Data Bus Leakage			50	uA	Data Bus is in High Impedence State
				10	uA	
I_{IL}	Input Leakage			10	uA	V_{IN} = V_{CC}
I_{CC}	Power Supply Current		45	80	mA	V_{CC} = 5.25V No Load

CAPACITANCE

T_A = 25°C; V_{CC} = GND = ØV

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance			10	pF	f_C = 1MHz
$C_{I/O}$	I/O Capacitance			20	pF	Unmeasured pins returned to GND

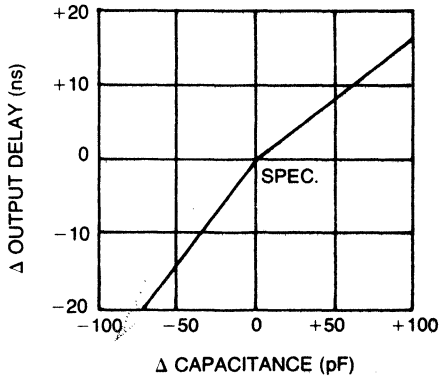


FIGURE 4. OUTPUT DELAY vs CAPACITANCE

A.C. TIMING PARAMETERS

SYMBOL	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS
	BUS PARAMETERS				
	Read Cycle (Reference Figure 6)				
t_{AR}	Address Stable before $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	50		ns	
t_{RA}	Address Hold Time for $\overline{RE}$, ($\overline{CS}$, C/$\overline{D}$)	5		ns	
t_{RE}	$\overline{RE}$ Pulse Width	350		ns	
t_{RD}	Data Delay from $\overline{RE}$		200	ns	C_L = 50 pF
t_{RDH}	$\overline{RE}$ to Data Floating		200	ns	C_L = 50 pF
		25		ns	C_L = 15 pF
	WRITE CYCLE (Reference Figure 7)				
t_{AW}	Address Stable before $\overline{WE}$	20		ns	
t_{WA}	Address Hold Time for $\overline{WE}$	20		ns	
t_{WE}	$\overline{WE}$ Pulse Width	350		ns	
t_{DS}	Data Set-Up Time for $\overline{WE}$	200		ns	
t_{WDH}	Data Hold Time for $\overline{WE}$	40		ns	
	OTHER TIMINGS (Reference Figures 8-12)				
t_{DTX}	TXD Delay from Falling Edge of TXC		500	ns	C_L = 100 pF
t_{SRX}	Rx Data Set-up Time to Sampling Pulse	200		ns	C_L = 100 pF
t_{HRX}	Rx Data Hold Time to Sampling Pulse	100		ns	C_L = 100 pF
t_{TX}	Transmitter Input Clock Frequency	DC	800	KHz	
t_{RX}	Receiver Input Clock Frequency	DC	800	KHz	
t_{DTY}	TXRDY Delay from $\overline{WE}$	200ns	2 Clock Periods		
t_{DRY}	RXRDY Delay from Center of Last Data Bit (FCR Delay from Center of Data Bit)		½ Clock Period		
t_{DTE}	TXE Delay from TXRDY		½ Clock Period		

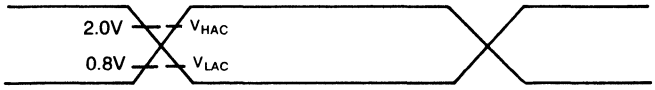


FIGURE 5. TEST POINTS FOR A.C. TIMING

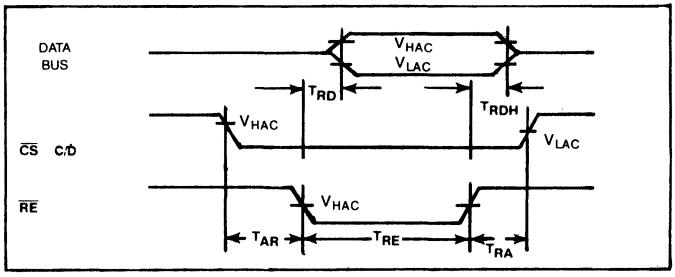


FIGURE 6. READ CYCLE TIMING

Note: AC timings measured at V_{OH} = 2.0V, V_{OL} = 0.8V and with test load circuit.

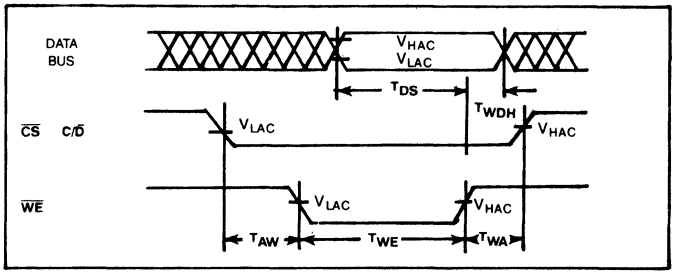


FIGURE 7. WRITE CYCLE TIMING

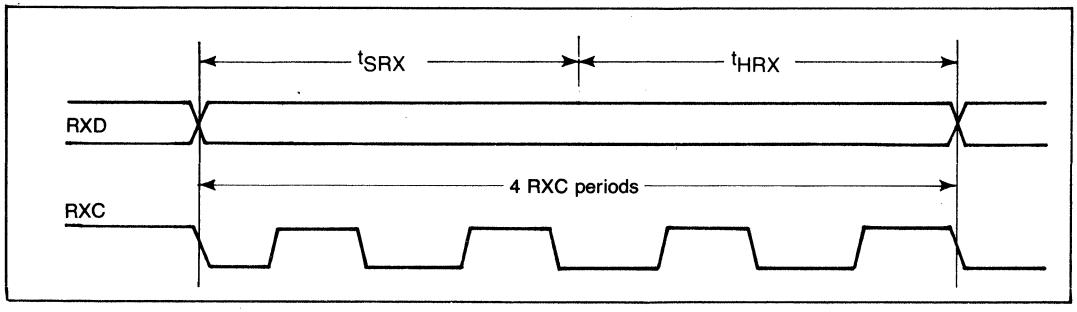


FIGURE 8. RECEIVER CLOCK AND DATA TIMINGS

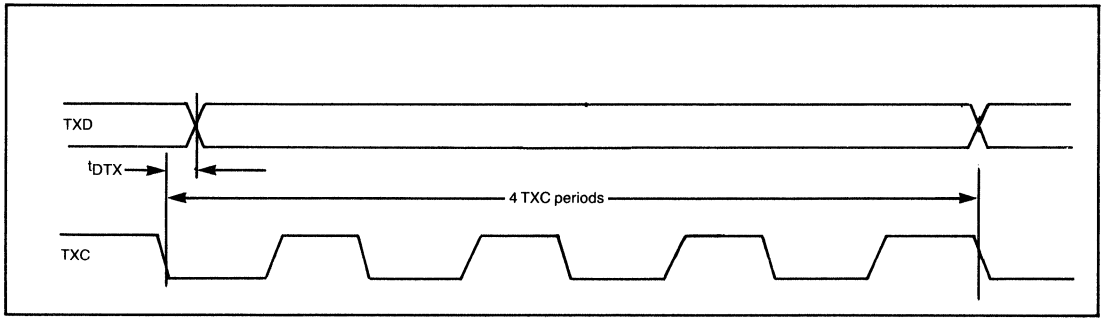


FIGURE 9. TRANSMITTER CLOCK AND DATA TIMINGS

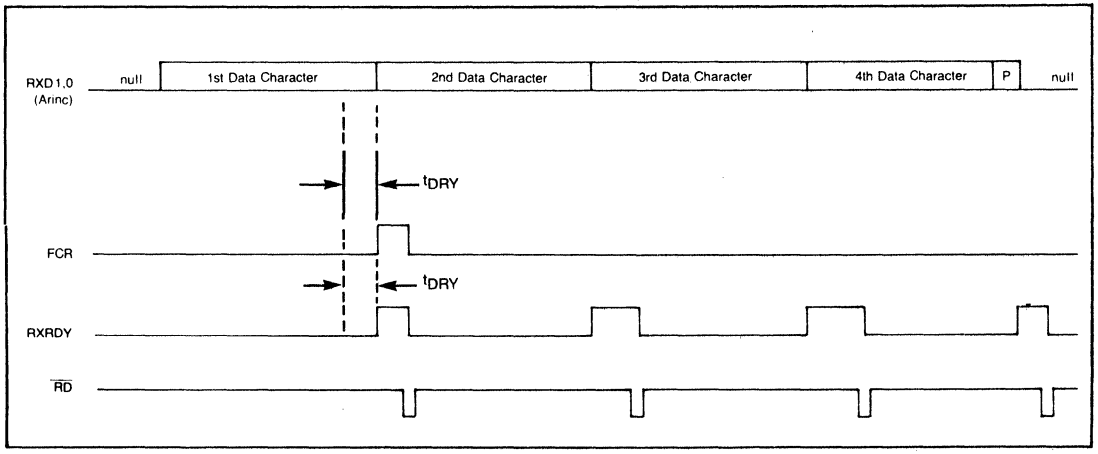


FIGURE 10. RXRDY AND FCR TIMING

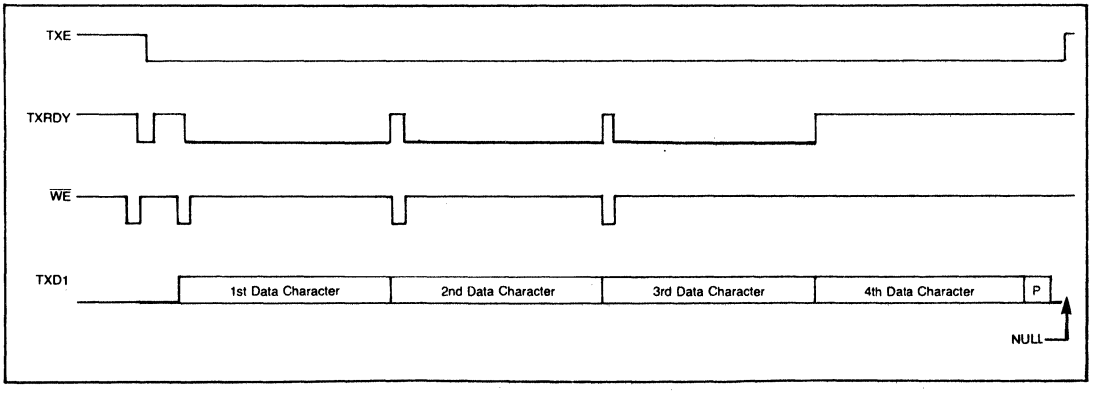


FIGURE 11. RXRDY AND TXE TIMINGS (4 Character Sequence)

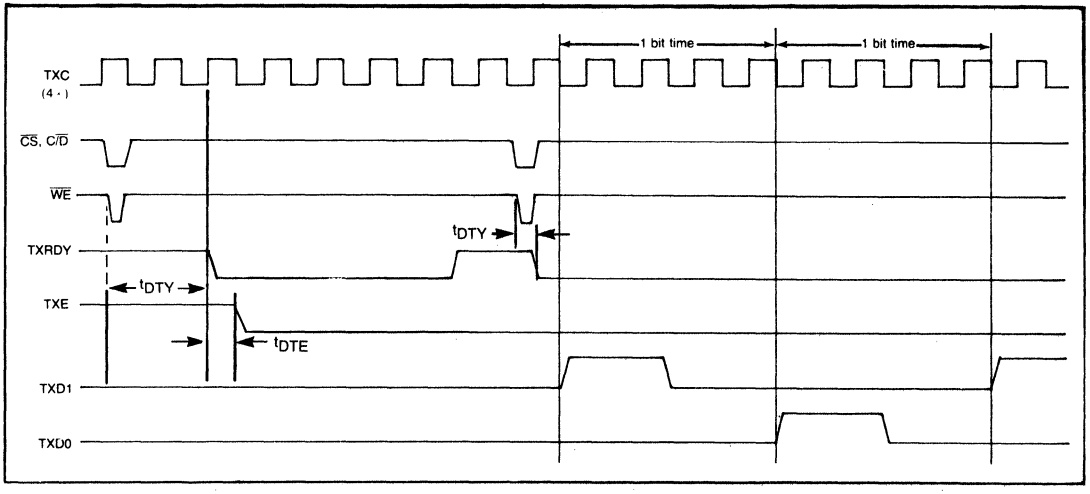


FIGURE 12. TRANSMITTER TIMINGS (ARINC MODE)

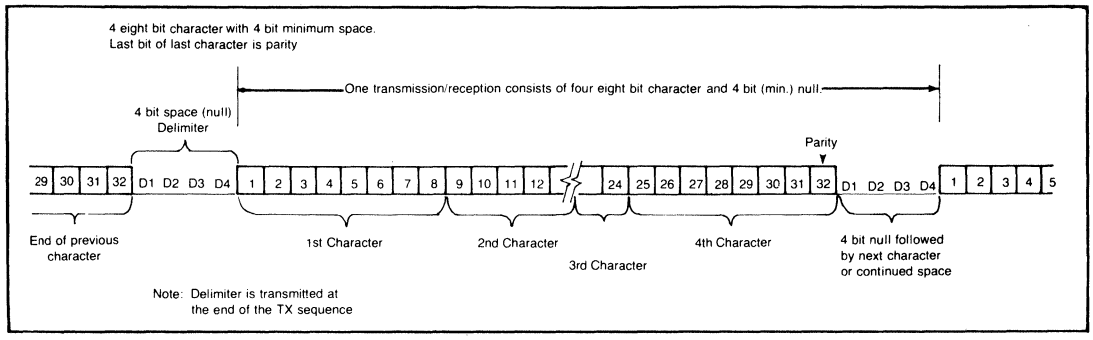


FIGURE 12. ARINC 429

The V/Z Receiver converts ±10 volt levels to TTL logic levels. It is composed of logic one and zero comparators. A logic one (RXD1) TTL output is derived when voltage rising to 1 (VR1) threshold is crossed and terminated at voltage falling to 1 (VF1). A logic zero (RXD0) TTL output is generated between voltage falling to zero (VFO) and voltage rising from zero (VRO). When input thresholds are not exceeded, neither output is active. The V/Z output can drive one TTL input.

The return to zero (RZ) format is shown below

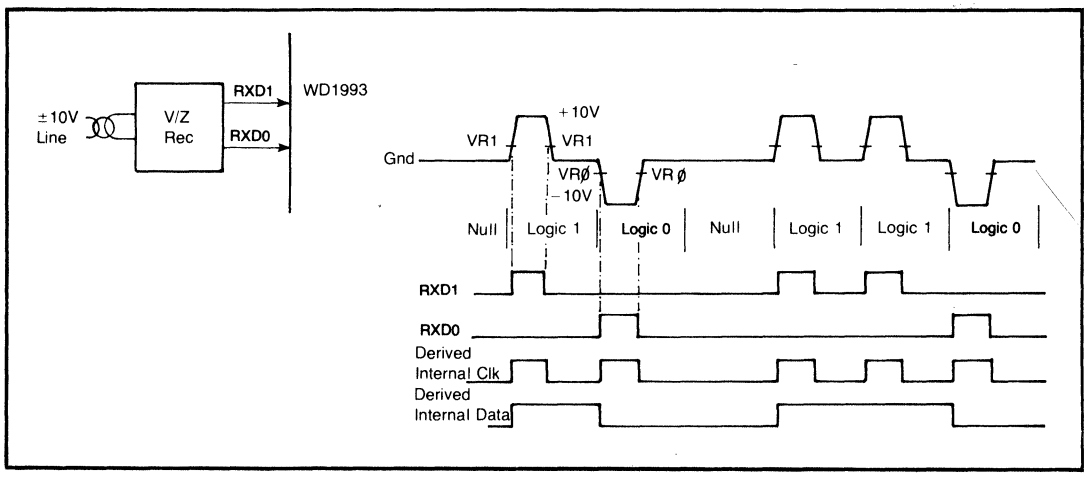


FIGURE 13. ARINC RECEIVER CIRCUIT

The V/Z Driver convert TTL logic levels into ± 10 volt levels. The TXD1 and TXD0 outputs of the WD1993 are used to drive the line drivers. Each output can drive one TTL load. When the outputs are not active, the line Driver should return to zero.

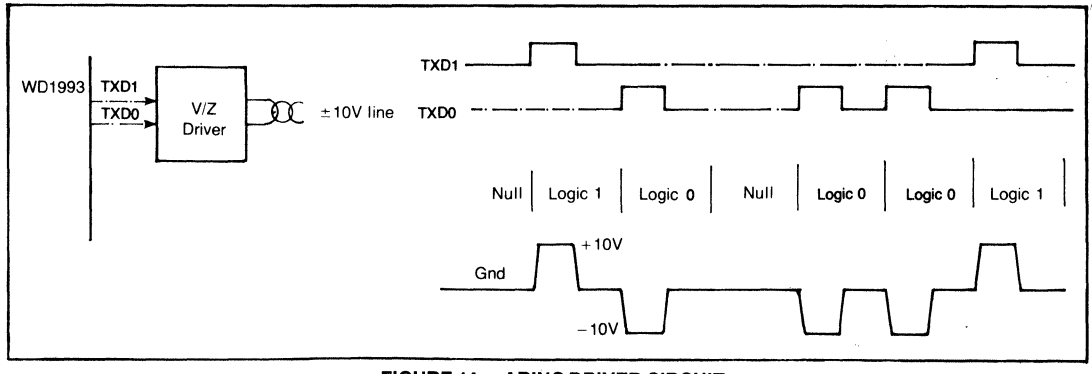


FIGURE 14. ARINC DRIVER CIRCUIT

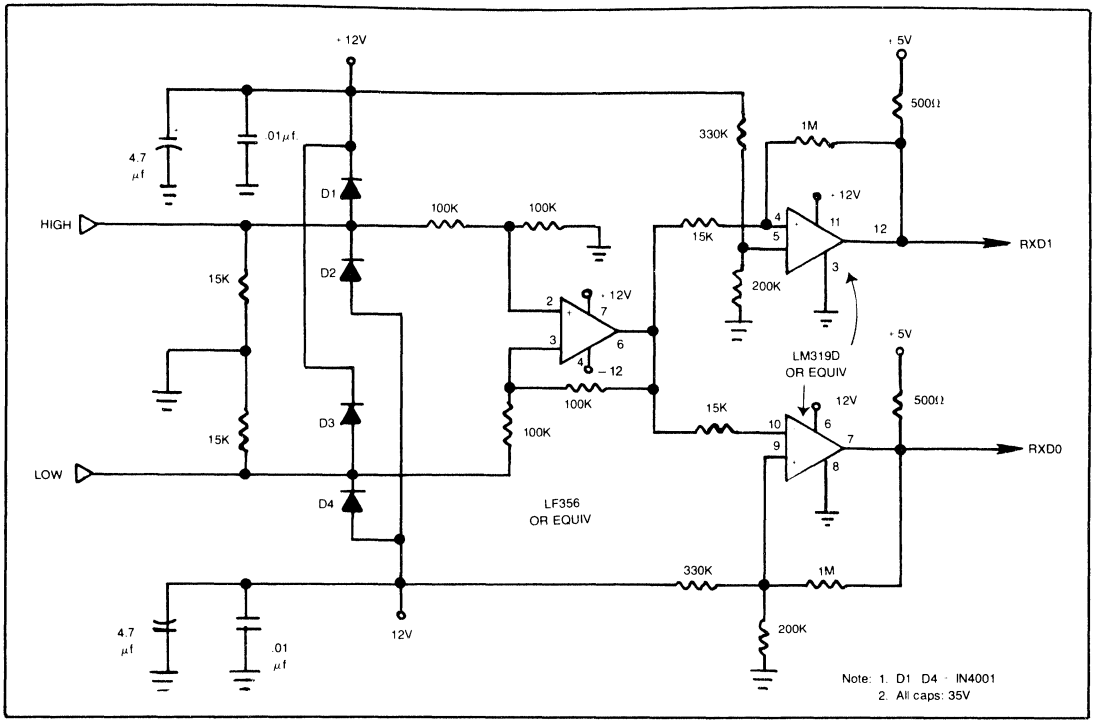


FIGURE 15. ARINC 429 LINE LEVEL TRANSLATOR (RECEIVER)

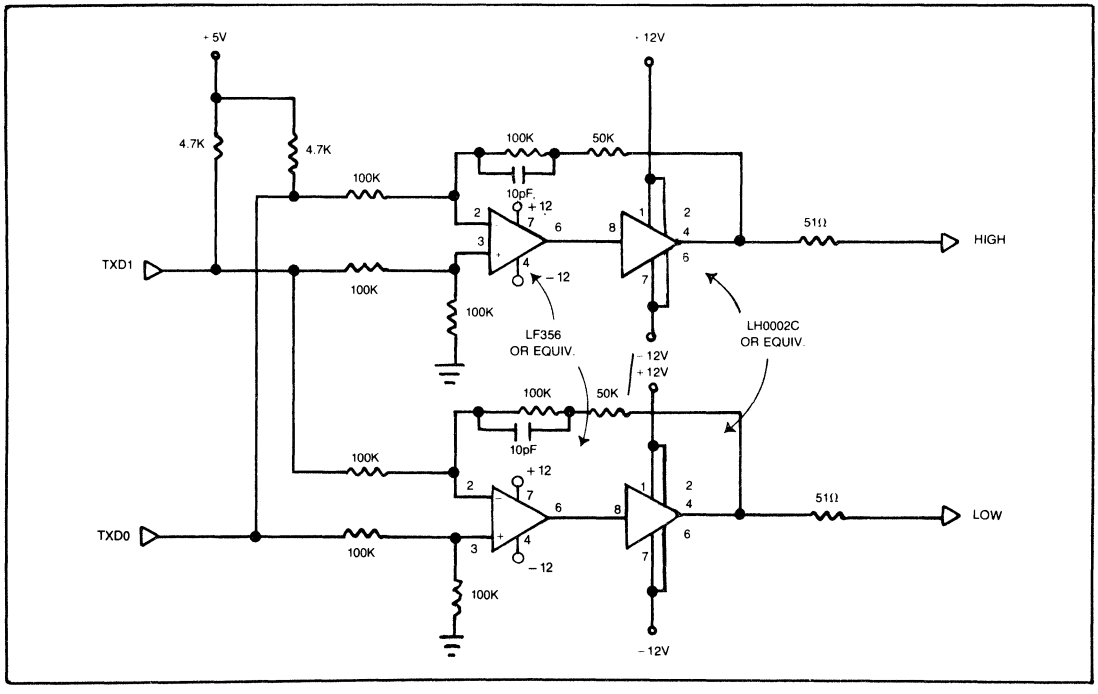


FIGURE 16. ARINC 429-1 LINE DRIVER

See page 383 for ordering information.

Printed in U.S.A.

FINAL

WD2001/02 Data Encryption Devices

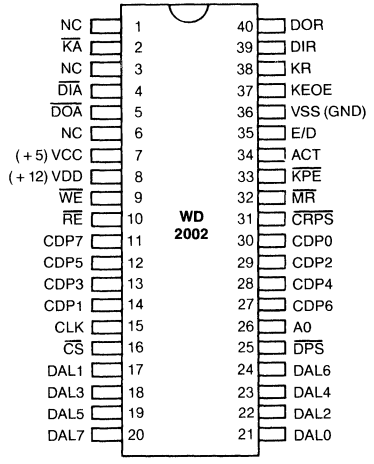
FEATURES

- CERTIFIED BY NATIONAL BUREAU OF STANDARDS.
- TRANSFER RATE:
  WD2001/2-05 300Kbs with 500KHz clock
  WD2001/2-20 1.3 Mbs with 2MHz clock
  WD2001/2-30 1.8 Mbs with 3MHz clock
- ENCRYPTS/DECRYPTS 64 BIT DATA WORDS USING 56 BIT KEY WORD
- SINGLE PORT 28 PIN PACKAGE WD2001 OR DUAL PORT 40 PIN PACKAGE WD2002
- COMMAND BIT PROGRAMMING VIA DAL BUS OR INPUT PINS
- PARITY CHECK ON KEY WORD LOADING
- STANDARD 8 BIT MICROPROCESSOR INTERFACE
- INPUTS AND OUTPUTS TTL COMPATIBLE
- KEY STORED ON CHIP IS NOT EXTERNALLY ACCESSIBLE

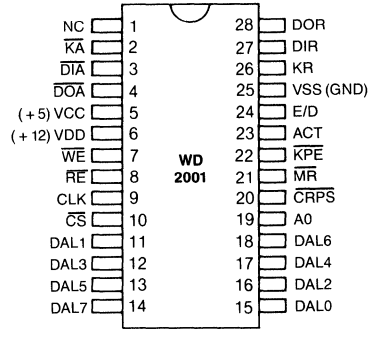
  SEPARATE CLEAR AND CIPHER BUS STRUCTURE ON WD2002

APPLICATIONS

- SECURE BROKERAGE TRANSACTIONS
- ELECTRONIC FUNDS TRANSFERS
- SECURE BANKING/BUSINESS ACCOUNTING
- MAINFRAME COMMUNICATIONS
- REMOTE AND HOST COMPUTER COMMUNICATIONS
- SECURE A/D
- SECURE DISK OR MAG TAPE DATA STORAGE
- SECURE PACKET SWITCHING TRANSMISSION



PIN DESIGNATION



PIN DESIGNATION

DESCRIPTION

The Western Digital WD2001 and WD2002 Data Encryption/Decryption devices are designed to encrypt and decrypt 64-bit blocks of data using the algorithm specified in the Federal Information Processing Data Encryption Standard (#46). These devices encrypt a 64-Bit clear text word using a 56-Bit user-specified key to produce a 64-Bit cipher text word. When reversed, the cipher text word is decrypted to produce the original clear text word.

The WD2001/02 are fabricated in N-channel silicon gate MOS technology and are TTL compatible on all inputs and outputs.

NOTE: This device can not be shipped outside of the United States of America without authorization from the State Department and Department of Defense.

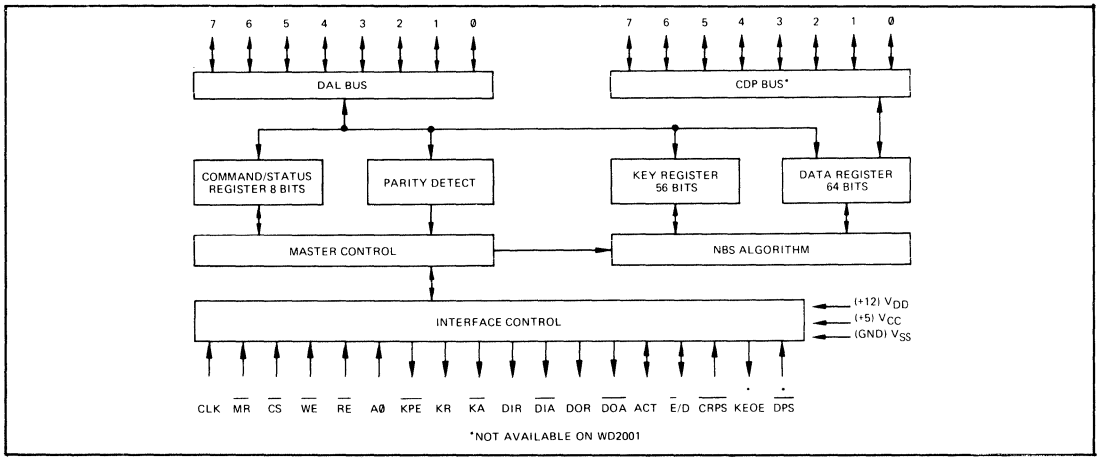
PIN DESCRIPTION

WD2001	WD 2002	SIGNAL NAME	MNEMONIC	FUNCTION
11-18	17-24	DATA LINES	DAL 0 → DAL 7	Eight active true three-state bi-directional I/O lines used for information transfer to and from the DES chip's registers. During single port operation, all COMMAND/STATUS, KEY WORD and DATA WORD transfers are via this bus. During dual port operation, all COMMAND/STATUS, KEY WORD and clear DATA WORD transfers are via this bus. (Cipher DATA WORD transfers are via the CIPHER DATA PORT (CDP) bus.)†
N/A*	11-14 27-30	CIPHER DATA PORT	CDP 0 → CDP 7	Eight active true three-state bi-directional I/O lines used only in dual port operation. Cipher DATA WORD transfers are via this bus. These pins are available on the WD2002 40 pin package version only.†
6	8	POWER SUPPLY	V_{DD}	+ 12v
5	7	POWER SUPPLY	V_{CC}	+ 5v
25	36	GROUND	V_{SS}	GROUND
9	15	CLOCK	CLK	System clock input.
21	32	MASTER RESET	$\overline{MR}$	$\overline{MR}$ active low resets the COMMAND/STATUS REGISTER and resets internal circuitry. (Requires active clock for reset operation.)
10	16	CHIP SELECT	$\overline{CS}$	$\overline{CS}$ is made low to access registers within the device.
8	10	READ ENABLE	$\overline{RE}$	The contents of the selected register are placed on the DAL (or CDP) bus lines when $\overline{CS}$ and $\overline{RE}$ are made low.
7	9	WRITE ENABLE	$\overline{WE}$	Information on the DAL (or CDP) bus lines is written into the selected DES register when $\overline{CS}$ and $\overline{WE}$ are made low.
19	26	A0	A0	When this input is active high (during $\overline{CS}$ active) the COMMAND/STATUS REGISTER is addressed. (A0 active high will override internally generated addressing of the KEY and DATA REGISTERS as described on page 6.) This input is ignored when $\overline{CRPS}$ is active.
26	38	KEY REQUEST	KR	This output is active high when the DES chip is requesting that a byte of the KEY WORD be written into the KEY REGISTER. (The KEY REGISTER is automatically addressed when KR is active, unless overriden by A0.)
2	2	KEY ACKNOWLEDGE	$\overline{KA}$	This output is active low when $\overline{WE}$ is made low while the KEY REGISTER is addressed. (Can be used for handshake.)
27	39	DATA-IN REQUEST	DIR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be written into the DATA REGISTER. (The DATA REGISTER is automatically addressed when DIR is active, unless overriden by A0.)
3	4	$\overline{\text{DATA-IN}}$ ACKNOWLEDGE	$\overline{DIA}$	This output is active low when $\overline{WE}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)
28	40	DATA-OUT REQUEST	DOR	This output is active high when the DES chip is requesting that a byte of the DATA WORD be read from the DATA REGISTER. (The DATA REGISTER is automatically addressed when the DOR is active, unless overridden by A0.)

PIN DESCRIPTION (Continued)

WD2001	WD2002	SIGNAL NAME	MNEMONIC	FUNCTION
4	5	DATA-OUT ACKNOWLEDGE	$\overline{DOA}$	This output is active low when $\overline{RE}$ is made low while the DATA REGISTER is addressed. (Can be used for handshake.)
22	33	KEY PARITY ERROR	$\overline{KPE}$	This output is active low when enabled via the COMMAND/STATUS REGISTER BIT 2 (KEOE) and a parity error has been detected during loading of the KEY REGISTER.
20**	31**	COMMAND REGISTER PIN SELECT	$\overline{CRPS}$	This input selects DAL bus or input pin programming of the COMMAND/STATUS REGISTER. $\overline{CRPS}$ high or open selects DAL bus programming. $\overline{CRPS}$ low selects input pin programming.
23	34	ACTIVATE	ACT	When $\overline{CRPS}$ is high or open, this pin is an output reflecting the status of the ACTIVATE bit (bit 1) of the COMMAND/STATUS REGISTER. When $\overline{CRPS}$ is low, this pin is an input that overrides the ACTIVATE bit of the COMMAND/STATUS REGISTER.
N/A*	37	KEY ERROR OUTPUT ENABLE	KEOE	This output indicates the status of the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER. This output is active when input pin programming is selected ($\overline{CRPS}$ low). This pin is available on the WD2002 40 pin package version only.
24	35	ENCRYPT/DECRYPT	E/D	When $\overline{CRPS}$ is high or open, this pin is an output reflecting the status of the ENCRYPT/DECRYPT bit (bit 3) of the COMMAND/STATUS REGISTER. When $\overline{CRPS}$ is low, this pin is an input pin that overrides the ENCRYPT/DECRYPT bit of the COMMAND/STATUS REGISTER.
N/A*	25**	DUAL PORT SELECT	$\overline{DPS}$	When this input is high or open, single port operation is selected and all DES chip transfers are via the DAL bus. When $\overline{DPS}$ is low, dual port operation is selected and both the DAL bus and the CDP bus are used [separate busses for clear data (DAL bus) and cipher data (CDP bus)]. This pin is available on the WD2002 40 pin package version only.

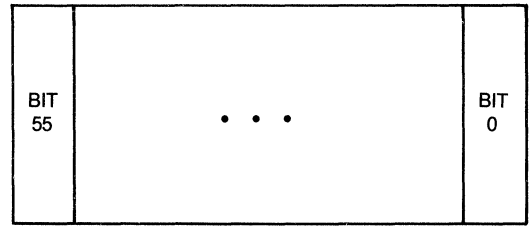
NOTE: * The WD2001 28 pin package version does not have the following pins: The 8 CDP pins, the KEOE pin, and the $\overline{DPS}$ pin.
** These inputs have internal pull-up resistors.
† L.S.B. (DATA BIT 0) at DAL7 and CDP7. M.S.B. (DATA BIT 7) at DAL0 and CDP0.



WD2001/WD2002 BLOCK DIAGRAM

ORGANIZATION

The Data Encryption Standard chip consists of a 56-bit KEY REGISTER, a 64-bit DATA REGISTER, an 8-bit COMMAND/STATUS REGISTER, plus the necessary logic to check KEY parity and implement the NBS algorithm. A typical system implementation is shown on page 10 and the block diagram is shown on page 1. Although the DES chip interfaces to a wide variety of processors including mini-computers, the interface is tailored to the 8080A class microprocessor.



KEY REGISTER
(LOAD ONLY)

GENERAL OPERATING DESCRIPTION

The user programs the DES chip for encryption or decryption, and single or dual port operation.* Data is encrypted/decrypted with a 64-bit user defined KEY WORD. Data encrypted with a given KEY WORD can be decrypted only using that KEY WORD. The KEY REGISTER is loaded by the computer with eight successive 8-bit bytes. Parity is checked on each byte of the KEY WORD as it is loaded into the KEY REGISTER (The 8th bit (DAL0) of each 8-bit byte is reserved for odd parity for that byte and is not used in the algorithm calculation.) Similarly the DATA REGISTER is loaded with eight successive 8-bit bytes. The DATA REGISTER is read by reading eight successive 8-bit bytes.

When the DES chip is programmed for encryption, the DATA REGISTER is loaded with eight bytes of plain or clear text. The DES chip encrypts the data, then the encrypted data may be read from the DATA REGISTER (64-bits of encrypted text). When the DES chip is programmed for decryption, the DATA REGISTER is loaded with eight bytes of encrypted or cipher text. The DES chip decrypts the data, then the plain text may be read from the DATA REGISTER (64-bits of plain text). Note that all transfers to and from the KEY REGISTER and/or DATA REGISTER must occur in eight successive 8-bit bytes.

***Note:** Dual port operation available with WD2002 40 pin package version only. (Single and dual port operation is described in detail under PART V. OPERATION.)

REGISTER DESCRIPTION

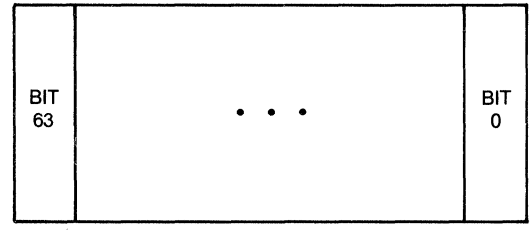
The following describes the KEY, DATA, and COMMAND/STATUS REGISTERS of the DES chip.

Key Register

This 56-bit register contains the KEY by which the Data Encryption Algorithm operates. Eight successive bytes are needed to load the KEY REGISTER. The KEY REGISTER can be loaded only when there is a KEY REQUEST (Status bit and output). THIS REGISTER IS LOAD ONLY AND CANNOT BE READ.

Data Register

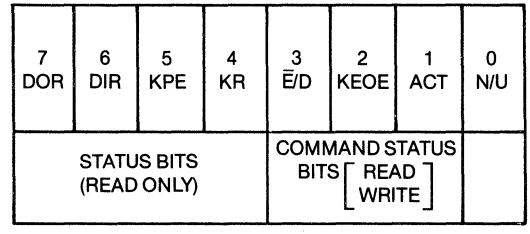
This 64-bit register contains plain or cipher text. When in the encrypt mode, the DATA REGISTER is loaded with plain text, and when read contains cipher text. When in the decrypt mode, the DATA REGISTER is loaded with cipher text, and when read contains plain text. The DATA REGISTER is always read or loaded with eight successive byte transfers. The DATA REGISTER can be loaded only when there is a DATA-IN REQUEST (status bit and output); similarly the DATA REGISTER can be read only when there is a DATA-OUT REQUEST (status bit and output).



DATA REGISTER

Command/Status Register (C/S R)

This 8-bit register controls the operation of the DES chip and monitors its status. Bits 7, 6, 5 and 4 are status-only bits (read only). Bits 3, 2 and 1 are COMMAND/STATUS bits (read/write). Bit 0 is not used. The COMMAND/STATUS bits (bits 3, 2, and 1) are normally loaded only once for an entire encrypt or decrypt process.



COMMAND/STATUS REGISTER

COMMAND/STATUS REGISTER (C/S R)

Bit	Name	Function
C/S R0	NOT USED	
C/S R1	ACTIVATE	This bit must be set from '0' to '1' to initiate loading the KEY REGISTER. This bit must be '1' for encrypt/decrypt operation. This is a read/write bit.
C/S R2	KEY ERROR OUTPUT ENABLE (KEOE)	When '0', the $\overline{\text{KEY PARITY ERROR}}$ output pin ($\overline{\text{KPE}}$) remains inactive regardless of the status of the $\overline{\text{KEY PARITY ERROR}}$ bit (bit 5). When '1', the $\overline{\text{KEY PARITY ERROR}}$ output pin is active when the KPE bit (bit 5) is '1'. This bit is set to '1' upon a MASTER RESET. This is a read/write bit.
C/S R3	$\overline{\text{ENCRYPT}}$/DECRYPT ($\overline{\text{E}}$/D)	When '0' data is to be encrypted. When '1' data is to be decrypted. This is a read/write bit.
C/S R4	KEY REQUEST (KR)	This bit is set one clock period after the ACTIVATE bit is set (from '0' to '1'). It is reset upon loading of the 8th and final byte of the KEY REGISTER. This is a read only bit.
C/S R5	KEY PARITY ERROR (KPE)	This bit is set internally upon detection of a parity error during loading of the KEY REGISTER. It is reset when the ACTIVATE bit is programmed from '1' to '0' (i.e., chip is deactivated). This is a read only bit.
C/S R6	DATA-IN REQUEST (DIR)	This bit is set upon either: a) Completion of KEY REGISTER loading - or - b) Completion of DATA REGISTER reading, (ie, the last DATA-OUT REQUEST has been serviced by an 8-byte read and the DATA REGISTER is now empty and ready to be loaded with the next DATA WORD). It is reset upon loading of the 8th and final byte of the DATA REGISTER. This is a read only bit.
C/S R7	DATA-OUT REQUEST (DOR)	This bit is set upon completion of the internal encrypt/decrypt calculation of a DATA WORD. It is reset upon reading of the 8th and final byte of the DATA REGISTER. This is a read only bit.

Note: All bits of the COMMAND/STATUS REGISTER are reset to '0' upon MASTER RESET, except bit 2 (KEOE) which is set to '1' and bit 0 (not used) which will read '1' by default during a COMMAND/STATUS REGISTER read.

DETAILED OPERATING DESCRIPTION

The DES chip is initiated by programming a '1' in the ACTIVATE bit of the COMMAND/STATUS REGISTER. The DES chip will respond by activating the KEY REQUEST (KR) bit (bit 4) of the STATUS REGISTER and the KEY REQUEST output.

The user must deactivate A0 (allowing the chip to internally address the KEY REGISTER), and load the KEY REGISTER with the 64-bit KEY WORD. The KEY REGISTER is loaded with 8 consecutive 8-bit bytes by activating $\overline{WE}$ 8 times (with $\overline{CS}$ active).

When $\overline{WE}$ is made active, the DES chip deactivates the KR output. When $\overline{WE}$ is deactivated, the KR output is again activated. The DES chip will activate 8 KEY REQUESTs in this fashion until the KEY REGISTER is full.

Also, when $\overline{WE}$ is made active, the DES chip responds by activating the $\overline{KEY\ ACKNOWLEDGE}$ ($\overline{KA}$) output. Thus, 8 $\overline{KA}$ activations will be made.

The KR and $\overline{KA}$ outputs can be used for asynchronous handshaking (as in DMA control) or further activations following the first KR can be ignored and the KEY REGISTER can be loaded in a synchronous (programmed I/O) manner via 8 successive activations of $\overline{WE}$.

Each byte of the KEY WORD is checked for odd parity as it is loaded. If a parity error is found, the chip will set the KEY PARITY ERROR (KPE) bit (bit 5) of the COMMAND/STATUS REGISTER. If the KEY ERROR OUTPUT ENABLE bit (bit 2) of the COMMAND/STATUS REGISTER has been set, the DES chip will also activiate the $\overline{KPE}$ output. The KPE bit will be reset when the ACTIVATE bit is re-programmed to a '0'.

After loading the last (8th) byte of the KEY WORD into the KEY REGISTER, the DES chip will set the DATA-IN REQUEST bit (bit 6) of the STATUS REGISTER and activate the DATA-IN REQUEST (DIR) output. The 64-bit DATA WORD must then be loaded into the DATA REGISTER. The DATA REGISTER is loaded in the same manner as the KEY REGISTER via 8 successive activations of DATA-IN REQUEST (DES output), $\overline{WE}$ (DES input, and DATA-IN ACKNOWLEDGE (DES output).

After the last (8th) byte of the DATA WORD has been loaded, the chip begins the internal calculation of the NBS algorithm. Upon completion of the calculation, the new data is internally loaded into the DATA REGISTER, and the DES chip sets the DATA-OUT REQUEST bit (bit 7) of the STATUS REGISTER and activates the DATA-OUT REQUEST (DOR) output. The DATA WORD must then be read from the DATA REGISTER. The DATA REGISTER is read in the same manner as it was loaded via 8 successive activations of DATA-OUT REQUEST (DES output), $\overline{RE}$ (DES input), and $\overline{DATA\text{-}OUT\ ACKNOWLEDGE}$ (DES output).

Again, for both data-in and data-out, further activations of the DIR, DOR and $\overline{DIA}$, $\overline{DOA}$ outputs, after the first request, can be ignored and the DATA REGISTER loaded (read) by 8 successive activations of $\overline{WE}$ ($\overline{RE}$).

After the last (8th) byte of the DATA REGISTER has been read, the DES chip will reactivate the DATA-IN REQUEST. This cycle of loading the DATA REGISTER, internal algorithm calculation, and reading the new data from the DATA REGISTER can continue indefinitely until all desired data has been encrypted or decrypted with the current KEY WORD.

After all desired data has been encrypted/decrypted with the current KEY WORD, the ACTIVATE bit of the COMMAND/STATUS REGISTER should be programmed to '0'. When the ACTIVATE bit has been reset to '0', an unauthorized user will not have access to the last KEY loaded into the DES chip since to resume operation, the ACTIVATE bit must be programmed to '1' which activates KEY REQUEST and a new KEY must be loaded before access to the DATA REGISTER is possible.

To encrypt plain data, plain data is loaded into the DATA REGISTER, and encrypted data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit (bit 3 of the COMMAND/STATUS REGISTER) must have been previously programmed to '0'.)

To decrypt encrypted data, encrypted data is loaded into the DATA REGISTER, and plain data is read from the DATA REGISTER. (The $\overline{ENCRYPT}$/DECRYPT bit must have been previously programmed to '1'.)

Note: If it is desired to switch from encrypt to decrypt (or vice versa) under the same KEY WORD, this can be accomplished before a DATA WORD transfer is initiated. By making A0 high, the DES chip will override the internal addressing of the DATA REGISTER, and address the COMMAND/STATUS REGISTER. The COMMAND/STATUS REGISTER can be re-programmed. When A0 is returned to a low state, the DES chip will internally address the DATA REGISTER awaiting loading of the next DATA WORD.

DUAL PORT OPTION

(Available on WD2002 40 Pin Version Only)

When the $\overline{DUAL\ PORT\ SELECT}$ ($\overline{DPS}$) input is high or left open (ie., single port operation is selected), all transfers to/from the DES chip are via the DAL bus. The CDP bus is not used and remains three-stated.

When $\overline{DPS}$ is made low (ie., dual port operation is selected), all transfers to/from the COMMAND/STATUS REGISTER, and transfers to the KEY REGISTER are still via the DAL bus. Clear DATA WORDS are also transferred via the DAL bus. However, cipher DATA WORDS are now transferred via the CDP bus. This provides separate busses for clear and ciphered text.

Encryption during dual port operation requires loading clear data via the DAL bus, and reading cipher data via the CDP bus.

Decryption during dual port operation requires loading cipher data via the CDP bus, and reading clear data via the DAL bus.

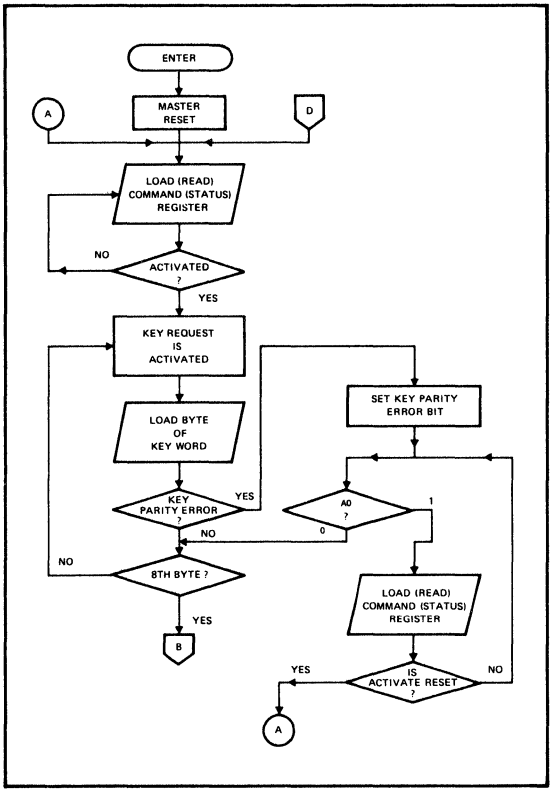
COMMAND SELECT OPTION

When the $\overline{\text{COMMAND REGISTER PIN SELECT}}$ ($\overline{\text{CRPS}}$) input is made low, the ACT and $\overline{\text{E}}$/D pins are enabled as inputs. These inputs override bits 1 and 3 (respectively) of the COMMAND/STATUS REGISTER. This allows input pin control of the DES chip. The KEOE bit (bit 2) of the COMMAND/STATUS REGISTER will be held to '1'.

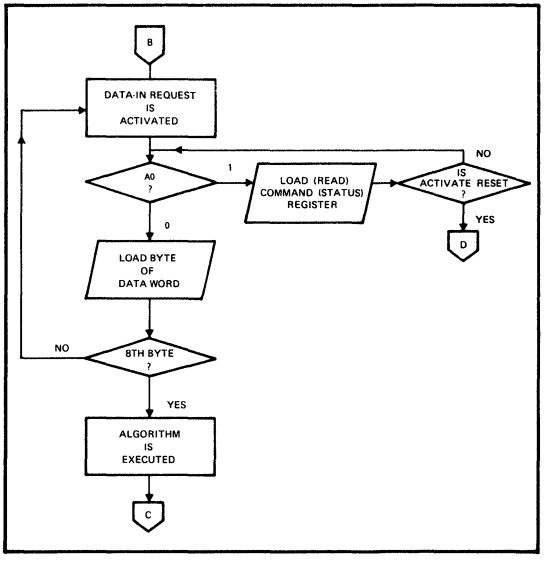
Input A0 will be disregarded in this mode of operation, and the COMMAND/STATUS REGISTER cannot be accessed via the DAL lines.

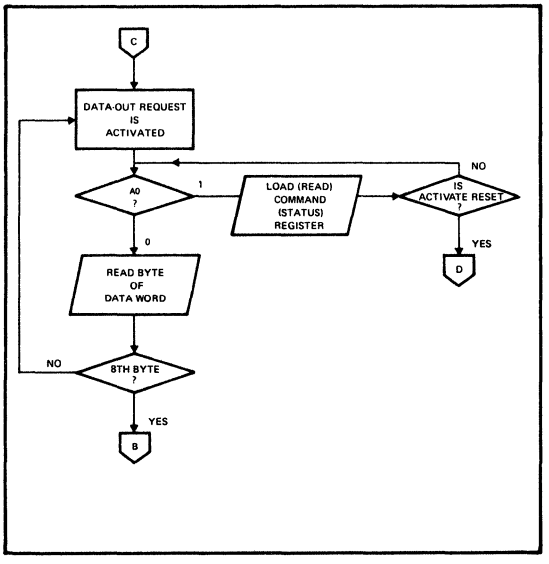
Note that the ACT pin must be toggled from '1' to a '0' to clear a parity error detection in this mode of operation.

All other operation remains as described previously.



WD2001/WD2002 FLOW CHARTS





MAXIMUM RATINGS

V_{DD} with Respect to V_{SS} (Ground) +15 to - 0.3V
Max. Voltage to any Input with Respect to V_{SS} +15 to - 0.3V
Operating Temperature 0°C to 70°C
Power Dissipation 1 W

Storage Temp. Ceramic -65°C to +150°C
Plastic -55°C to +125°C

OPERATING CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± .6V, V_{CC} = + 5.0V ± .25V, V_{SS} = OV

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
* I_{LI}	Input Leakage			10	uA	V_{IN} = V_{DD}
* * I_{IL}	Input Current Low			1.6	mA	V_{IN} = V_{SS}
I_{LO}	Output Leakage			10	uA	V_{OUT} = V_{CC}
I_{CCAVE}	V_{CC} Supply Current		68	100	mA	
I_{DDAVE}	V_{DD} Supply Current		17	25	mA	
V_{IH}	Input High Voltage	2.4			V	
V_{IL}	Input Low Voltage (All Inputs)			.8	V	
V_{OH}	Output High Voltage	2.8			V	I_O = -100uA
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA

* I_{LI} applies only to inputs without pull-up resistors.
* * I_{IL} applies only to inputs with pull-up resistors.

2001/2002-05 500KHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	100			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			500	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	500			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	50		250	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	100			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	300			ns	
T_{WR}	$\overline{WE}$ Pulse Width	300			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ (DIA)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ (DIA)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		450	700	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

2001/2002-20 2MHz CLOCK

AC CHARACTERISTICS

T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	80			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			330	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	330			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	30		200	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	80			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	200			ns	
T_{WR}	$\overline{WE}$ Pulse Width	200			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	90			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		300	450	ns	C_{LOAD} = 50PF

NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V

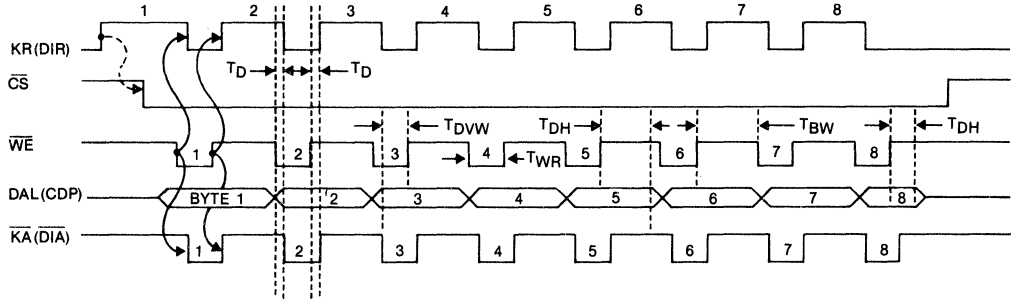
2001/2002-30 3MHz CLOCK

AC CHARACTERISTICS

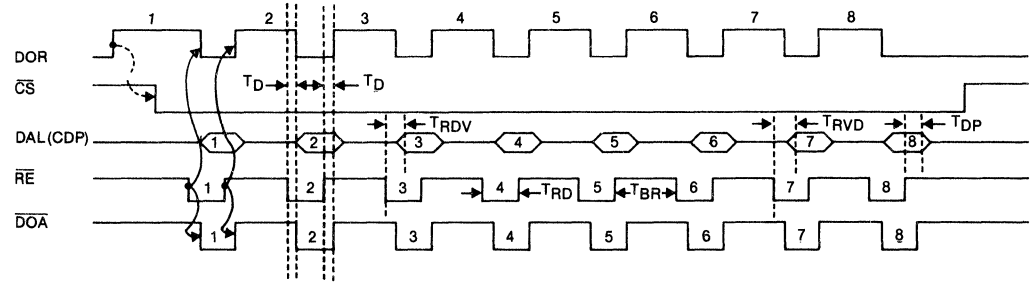
T_A = 0°C to 70°C, V_{DD} = +12.0V ± 0.6V, V_{SS} = OV, V_{CC} = +5.0 ± .25V

SYMBOL	CHARACTERISTIC	MIN.	TYP.	MAX.	UNITS	CONDITIONS
READ						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{RE}\downarrow$	50			ns	
T_{RDV}	$\overline{RE}\downarrow$ to DAL (CDP) Valid			220	ns	C_{LOAD} = 50PF
T_{RD}	$\overline{RE}$ Pulse Width	300			ns	
T_{DF}	$\overline{RE}\uparrow$ to DAL Float	20		130	ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{RE}\uparrow$	0			ns	
WRITE						
T_{ACS}	A0, $\overline{CS}$ Set up to $\overline{WE}\downarrow$	50			ns	
T_{DVW}	DAL (CDP) Set up to $\overline{WE}\uparrow$	130			ns	
T_{WR}	$\overline{WE}$ Pulse Width	175			ns	
T_{DH}	DAL (CDP) Hold From $\overline{WE}\uparrow$	60			ns	
T_{ACH}	A0, $\overline{CS}$ Hold From $\overline{WE}\uparrow$	0				
HAND-SHAKE						
T_D	KR (DIR)↓, $\overline{KA}$ ($\overline{DIA}$)↓ From $\overline{WE}\downarrow$ KR (DIR)↑, $\overline{KA}$ ($\overline{DIA}$)↑ From $\overline{WE}\uparrow$ DOR↓, $\overline{DOA}$↓ From $\overline{RE}\downarrow$ DOR↑, $\overline{DOA}$↑ From $\overline{RE}\uparrow$		150	300	ns	C_{LOAD} = 50PF

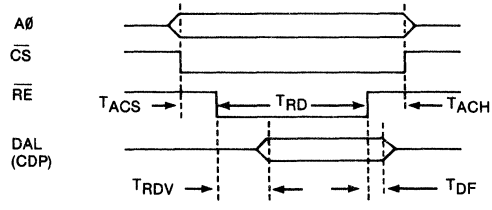
NOTE: All output timing specifications reflect the following: High Output 2.0V
Low Output 0.8V



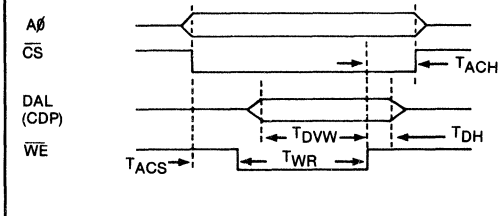
TYPICAL KEY OR DATA REGISTER LOAD



TYPICAL DATA REGISTER READ & TIMING



READ TIMING



WRITE TIMING

MISCELLANEOUS TIMING

1. CLOCK INPUT

FREQUENCY MAX.	FREQUENCY MIN.	PULSE WIDTH MIN
500KHz	100KHz	500nsec
2 MHz	100KHz	250nsec
3 MHz	100KHz	165nsec

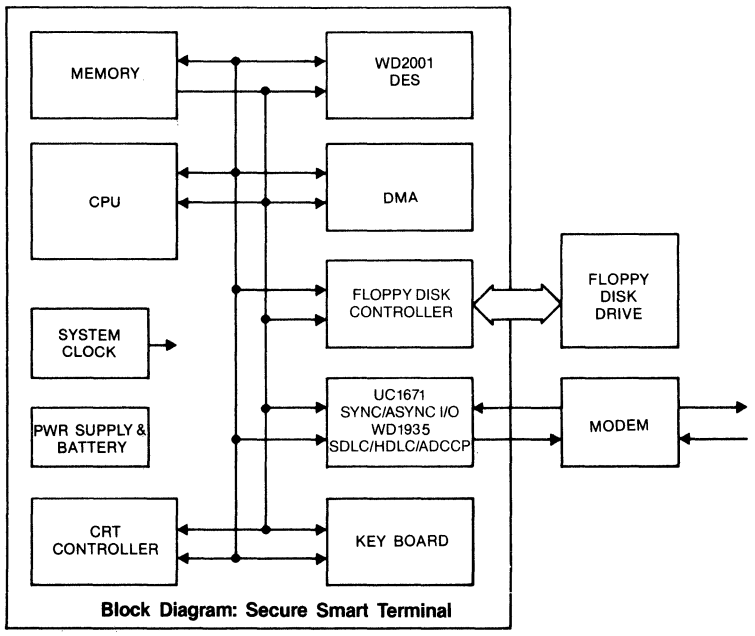
2. MASTER RESET PULSE WIDTH: 10 Clock Periods
3. Time between consecutive $\overline{RE}$ or $\overline{WE}$ pulses: $T_{BR} = T_{BW}$ = 2 CLOCK PERIODS MINIMUM
4. ACT, $\overline{E}$/D, KEOE OUTPUTS
   These pins will be valid within 2 CLK↓ + 450 nsec from $\overline{WE}$ ↑ of a COMMAND REGISTER write operation.
5. $\overline{KPE}$ OUTPUT
   This pin will be active within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write of a KEY WORD byte that results in a parity error.
6. $\overline{CRPS}$, $\overline{DPS}$, E/D INPUTS require a 300 ns set-up time.
7. The initial KR activation will be valid within 3 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of a write operation that programs a '1' into the COMMAND REGISTER ACTIVATE bit (or 2 CLK ↓ + 450 nsec from ACT input ↑, if $\overline{CRPS}$ = 0).
8. The initial DIR activation will be valid within 2 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the KEY REGISTER.
9. The initial DOR activation will be valid within 49 CLK ↓ + 450 nsec from $\overline{WE}$ ↑ of the 8th write into the DATA REGISTER.
10. When reading the DATA REGISTER (in response to DOR), subsequent data bytes are made available internally to the DAL (CDP) output buffers within 2 CLK ↓ + 450 nsec from $\overline{RE}$ ↑
11. After reading the DATA REGISTER in response to DORs, DIR will be activated and valid within 2 CLK↓ + 450 nsec. from RE ↑ of the 8th read from the DATA REGISTER.

NOTE: All output timings assume C_{LOAD} = 50 PF

TYPICAL APPLICATION

Shown below is a block diagram for a floppy disk based DES secure smart terminal. The Direct Memory Access (DMA) controller optimizes data transfer operations for not only the floppy but also for file encryption and decryption operations. Secure features for the terminal include: secure file storage on floppy disks, optical clear/secure transmission via the communications I/O and battery backup of the Terminal ID key.

Tampering with the Terminal by unauthorized persons either through the key board, power supply, interrupt interlock, or attempting to open the service panel results in memory scrambling and terminal ID key destruction. Finally, a hardware option was also included to allow the use of the UC1671 or the WD1935 for bit oriented SDLC, HDLC, or ADCCP protocols.



Block Diagram: Secure Smart Terminal

See page 383 for ordering information.

Printed in U.S.A.

APPLICATION NOTE

WD2001/2 Applications Note
"One Bit Cipher Feedback In A Synchronous System"

INTRODUCTION

The WD2001/2 Data Encryption device interfaces easily to both microcomputer and hard-wired logic circuits. This Applications Note provides suggestions for the implementation of a synchronous circuit to perform system timing in a one bit cipher feedback application.

SYSTEM TIMING CONSIDERATIONS

The synchronous operation of a digital circuit often leads to both minimal hardware count and simple, easy to understand timing relationships. In addition, the concern over individual device characteristics become non-critical through the use of a worst case design approach. Common problems such as race conditions and temperature sensitivity can be virtually eliminated by synchronizing all logical events to a well defined clock edge.

WD2001/2 TIMING REQUIREMENTS

The WD2001/2 may be operated from a 2 MHZ clock. This provides a fundamental time period of 500 nSec that easily fits into the timing requirements for the device. For example, the minimum pulse width for a read (RD) or write (WR) pulse is 450 nSec.

Generation of the RD or WR pulse can be directly obtained from a synchronous device that transitions at each edge of the synchronous clock (SYNCLK). Figure 1 illustrates the timing relationship between SYNCLK and RD or WR.

Once the timing relationship is understood, the implementation becomes quite straightforward. The circuit of Figure 2 suggests a possible method of RD or WR generation.

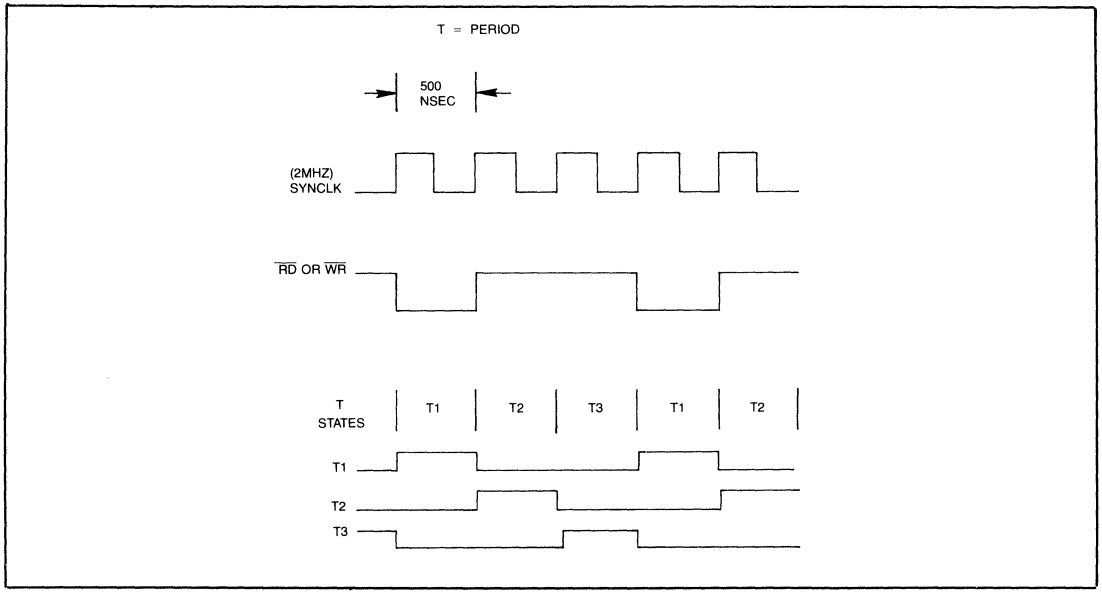
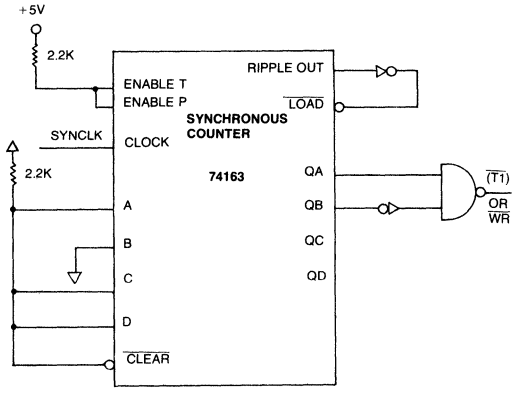


Figure 1 SYNCLK, RD, AND WR TIMING RELATIONSHIPS.



T STATE	COUNTER STATE	QB	QA	RD OR WR
T1	13	0	1	0
T2	14	1	0	1
T3	15	1	1	1

Figure 2 RD AND WR TIMING GENERATION

FUNDAMENTAL TIMING SEQUENCES

Any cryptographic implementation using the Data Encryption Standard (DES) can be broken down into four fundamental timing sequences. First, the key is loaded into the WD2001/2 (Load Key). Second, the data to be encrypted or decrypted is loaded into the device (Load Data). Next, the DES is executed. Finally, the result of the DES is unloaded from the WD2001/2 (Unload Data). Figure 3 lists the timing requirements for each timing sequence.

The Load Key, Load Data, and Unload Data sequences are highly similar. Figure 4 shows the logical flow associated with the Key Load or Data Load, or Data Unload. The Data Encryption Algorithm sequence can be derived from the timing associated with the other three sequences. For simplicity, the DES timing is accomplished by counting groups of three clock periods in a fashion similar to the method shown in Figure 4. The logical flow for the DES timing is shown in Figure 5.

SEQUENCE	NUMBER OF CLOCK PERIODS	TOTAL
Load Key	8 bytes × 3 clocks	24
Load Data	8 bytes × 3 clocks	24
DES	17 × 3 clocks	51
Unload Data	8 bytes × 3 clocks	24

Figure 3 FUNDAMENTAL TIMING SEQUENCES

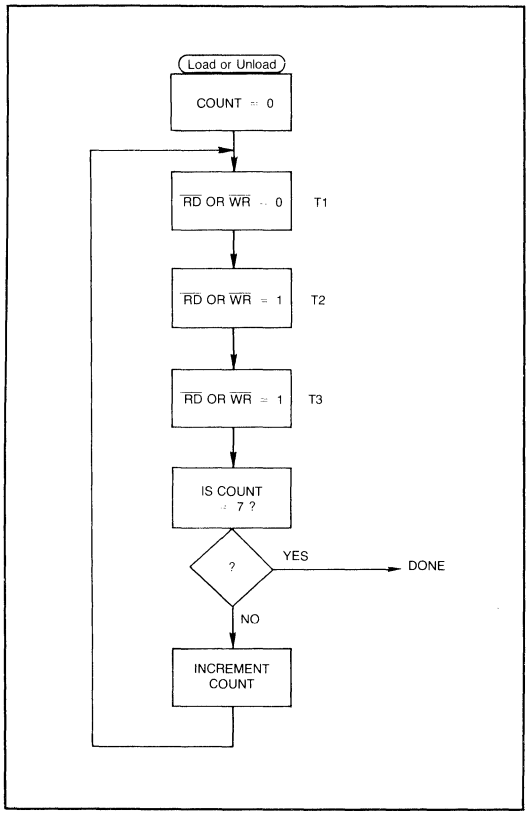


Figure 4 KEY LOAD, DATA LOAD, AND DATA UNLOAD FLOW

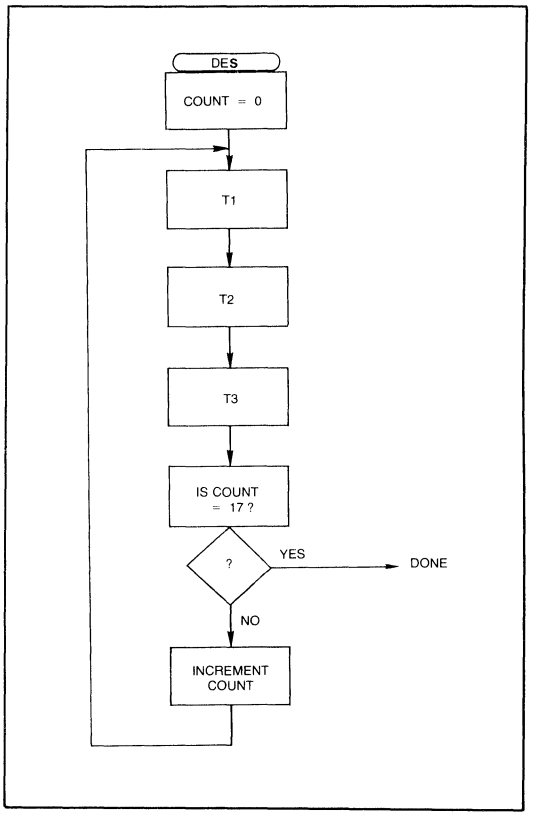


Figure 5 DES LOGICAL FLOW

SYSTEM TIMING OVERVIEW

The normal operation of a cryptographic system would require three classes of input/output (I/O) operations with the WD2001/2. First, the key is loaded (Key Load) through eight consecutive write cycles. Second, the data to be encrypted or decrypted is loaded (Load Data) in a similar fashion. After the Data Encryption standard is completed, the data is unloaded (Unload Data) through eight consecutive read cycles. Typically, the Key Load sequence would occur much less frequently than the Load Data or Unload Data sequences.

The flow diagram of Figure 6 shows the relationship between the four fundamental timing sequences defined previously, and also highlights the three I/O operations. Note that the Key Load sequence is outside of the tight loop.

Using the four fundamental timing sequences as logical building blocks, a functional block diagram of system timing can be designed. Figure 7 illustrates the overall system timing functions.

An implementation of the functions shown in Figure 7 is suggested in Figure 8. Note that all timing transitions are synchronous with the rising edge of SYNCLK.

Figure 9 details the timing of the Load Key sequence, and is similar to the Load Data, Unload Data, and DES sequences also.

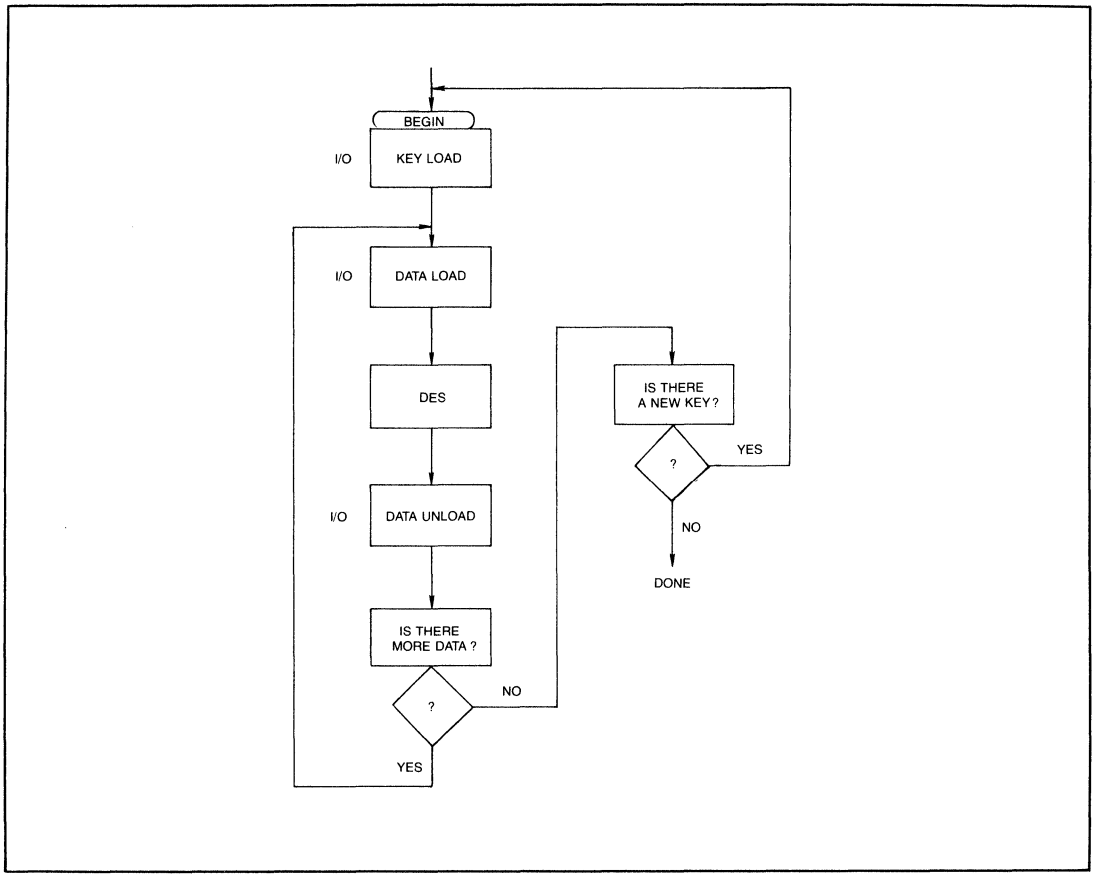


Figure 6 FUNDAMENTAL TIMING SEQUENCES INTERRELATIONS

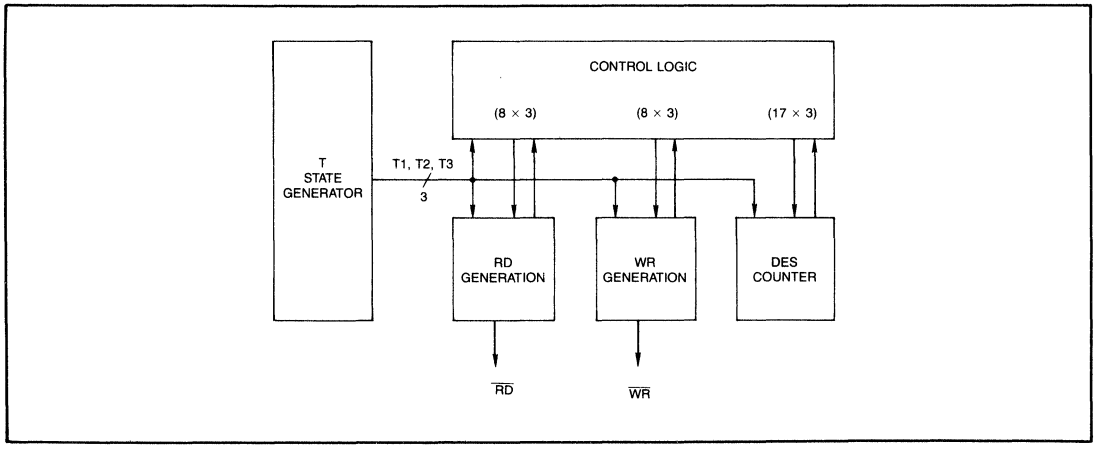
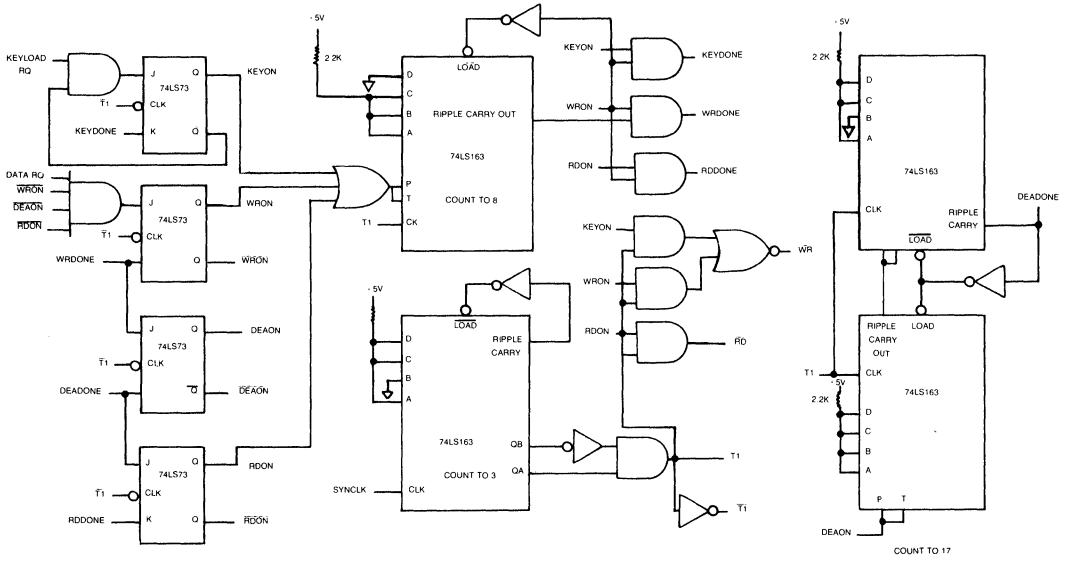


Figure 7 SYSTEM TIMING BLOCK DIAGRAM



1. KEYLOAD RQ AND DATA RQ DO NOT OCCUR SIMULTANEOUSLY.
2. ALL J-K PRESETS TO +5V.
3. ALL J-K CLEARS TO "RESET".
4. RESET SHOULD LOAD ALL 74LS163 COUNTERS.

Figure 8 SYSTEM TIMING IMPLEMENTATION

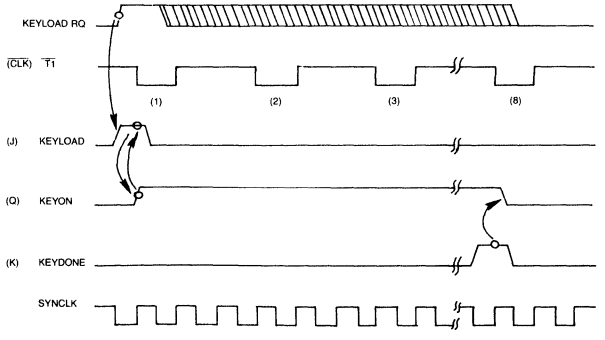


Figure 9 SINGLE KEYLOAD SEQUENCE

ONE BIT CIPHER FEEDBACK

The one bit cipher feedback (OBCFB) architecture is widely used in Data Communications. The WD2001/2 device, when operated with a 2 MHZ clock, will run at an effective bit rate of over 19,200 bits/second, which is the practical upper limit of many communications links.

FUNDAMENTAL LOGICAL COMPONENTS OF OBCFB

A one bit cipher feedback system can be broken down into nine logical components, as listed in Figure 10.

NAME	DESCRIPTION
KEY	56 bit number that maps INV to OV
IV	Initialization Vector
INV	Input Vector
DES	Data Encryption Standard
OV	Output Vector
SDI	Serial Data In
SDO	Serial Data Out
SR	Shift Register (used with INV)
MOD2	Modulo 2 Adder

Figure 10

NINE FUNDAMENTAL COMPONENTS OF OBCFB

FUNCTIONAL DESCRIPTION OF OBCFB

The OBCFB algorithm operates on a one bit wide data input, hence it is ideally suited to serial Data Communications applications. In encryption mode, the serial data in is added modulo 2 with the most significant bit (msb) of the 64 bit output vector. The result of this operation is then fed into the least significant bit (lsb) of a 64 bit shift register, and also is used as the serial data output. The shift register is then shifted from the lsb to the msb, and the result becomes the next input vector. After the Data Encryption Standard is completed, the process is repeated again for the next single bit of serial input data. Because each serial data bit requires an entire 64 bit INV and OV, the effective bit rate of this operation is 64 times less than that of a operation which uses all 64 bits of the OV, such as Code Book. Figure 11 shows a block diagram of a OBCFB circuit operating in encryption mode.

To decrypt, the operation is changed in one way. Instead of feeding the result of the modulo 2 adder to the shift register, the unmodified serial data is used. All other operations are identical. Figure 12 shows a circuit which supports both encryption and decryption.

Because the OBCFB algorithm uses a 64 bit shift register on the INV, each SDO bit is a function of its corresponding SDI bit and the 64 previous operations. This implies that the past history of the encryption operation is necessary to initialize a system. The IV is used to supply the history required to allow immediate use of the OV from the DEA. Typically, the IV is either a predefined value, or the last 64 SDO bits from the data stream being encrypted or decrypted. This allows the encryption process to be accomplished with discrete blocks of data, and hence the WD2001/2 can be used in a multichannel communications environment.

In OBCFB, the WD2001/2 is always set to encrypt mode. The selection of either the SDI as the feedback element to the shift register, or the SDO as the feedback element, determines whether the incoming data is encrypted or decrypted.

Another factor involved with OBCFB is the propagation of errors through a 64 bit block of data. Because of the 64 bit shift register that feeds the INV, a single bit error will cause the following 63 bits to be in error also. After the last bit of the 64 erred bits, the data will become resynchronized and the effect of the shift register will no longer cause bad data.

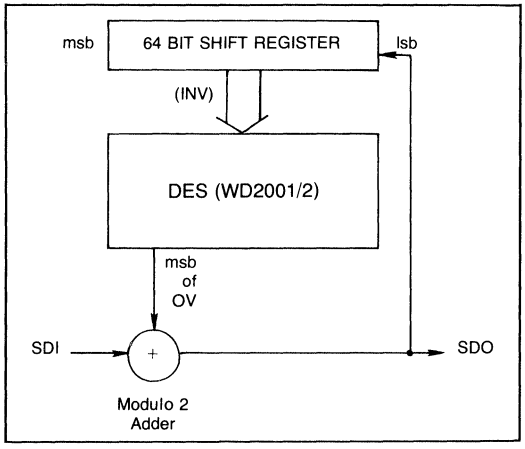


Figure 11 OBCFB ENCRYPTION BLOCK DIAGRAM

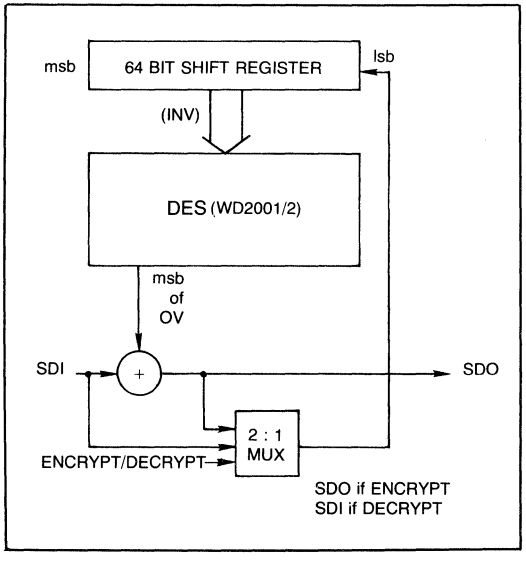


Figure 12

OBCFB ENCRYPTION/DECRYPTION BLOCK DIAGRAM

ONE BIT CIPHER FEEDBACK IMPLEMENTATION

Since the WD2001/2 is a byte input/output oriented device, the implementation of a OBCFB circuit can be accomplished without the 64 bit shift register shown in Figures 11 and 12. Through the use of a 9 bit wide FIFO, a "virtual" 64 bit shift register can be built. Figure 13 illustrates this with a Western Digital FIFO and some common TTL logic.

Once the modulo 2 adder, the encrypt/decrypt selector, and the shift register are defined, the overall circuit can be generated by combining these pieces along with the logic shown in Figure 8. The overall block diagram of the one bit cipher feedback system is given in Figure 14.

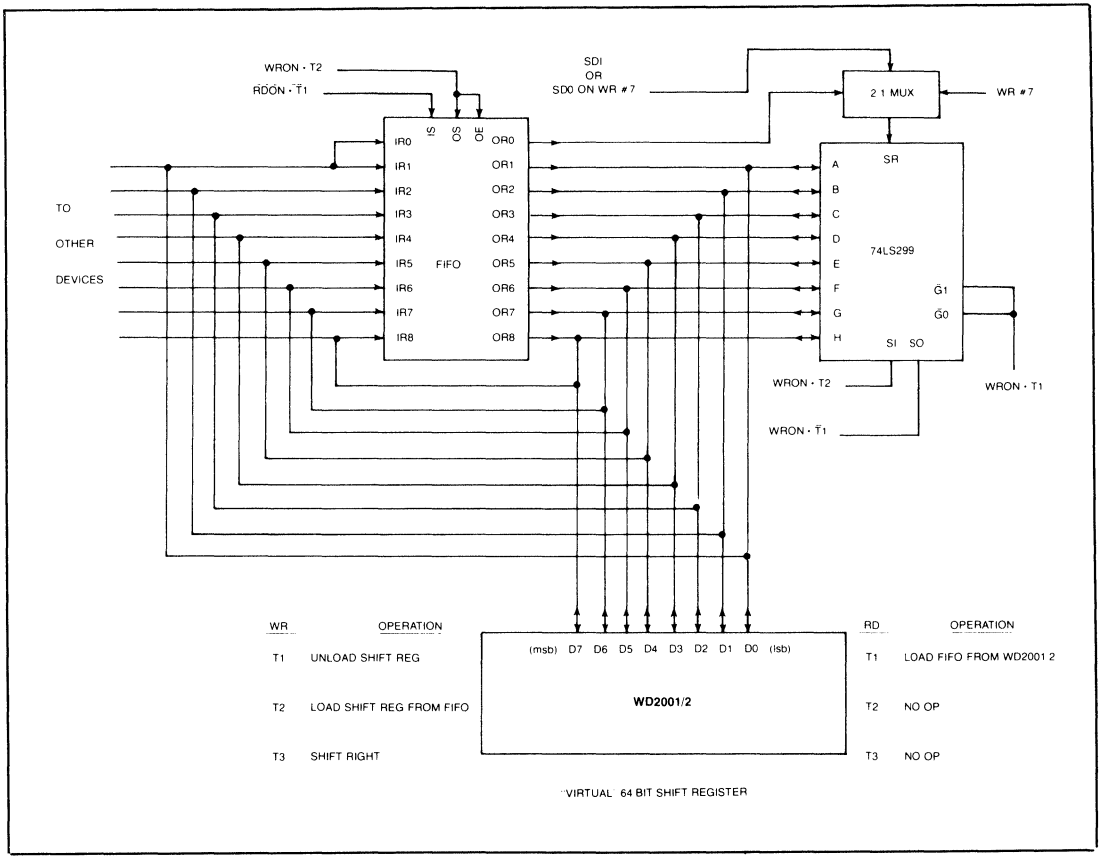


Figure 13 "VIRTUAL" 64 BIT SHIFT REGISTER

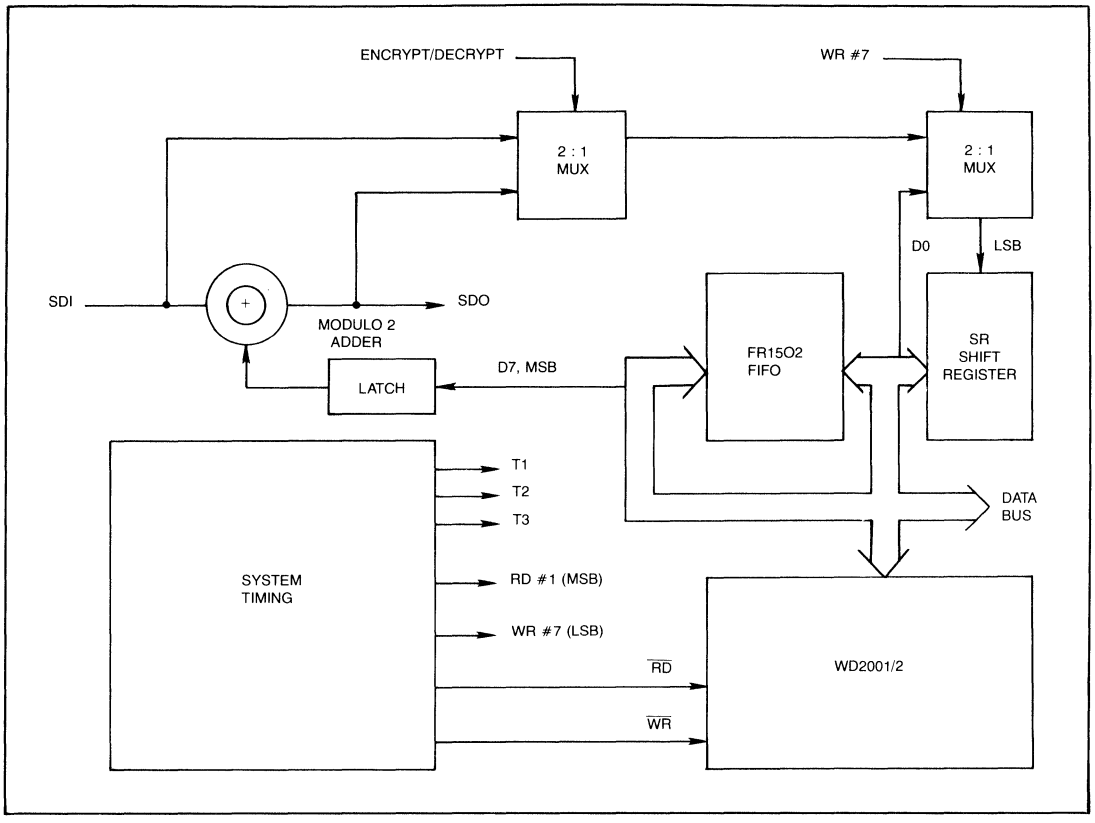


Figure 14 OBCFB SYSTEM BLOCK DIAGRAM

CONCLUSION

The WD2001/2 device lends itself readily to the most common of all Data Communications encryption techniques. The one bit cipher feedback algorithm can be implemented easily through the use of synchronous timing generation and circuit design techniques.

RELATED DOCUMENTS

WD2001/2 Data Sheet, Western Digital Corporation

FIPS 46
Federal Information Processing Standard
National Bureau Of Standard
Department of Commerce

Printed in U.S.A.

FINAL

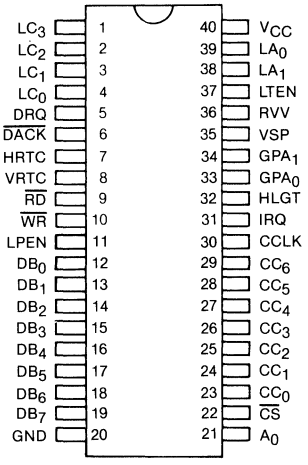
WD8275 Programmable CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- 11 VISUAL CHARACTER ATTRIBUTES (GRAPHIC CAPABILITY)
- CURSOR CONTROL (4 TYPES)
- LIGHT PEN DETECTION AND REGISTERS
- DUAL ROW BUFFERS
- PROGRAMMABLE DMA BURST MODE
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE
- 2 MHz VERSION (WD8275-00)
- 3 MHz VERSION (WD8275-02)

DESCRIPTION

The WD8275 Programmable CRT Controller is a single chip device to Interface CRT raster scan displays with microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.



Pin Designation

Table 1. Pin Descriptions

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	DMA REQUEST	DRQ	Output signal to the DMA controller requesting a DMA cycle.
6	I	DMA ACKNOWLEDGE	$\overline{DACK}$	Input signal from the DMA controller acknowledging that the requested DMA cycle has been granted.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers during a DMA cycle.
11	I	LIGHT PEN	LPEN	Input signal from the CRT system signifying that a light pen signal has been detected.
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL THREE-STATE DATA BUS LINES	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	A_0	A high input on A_0 selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	CS	The read and write are enabled by CS.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	From dot/timing logic.
31	O	INTERRUPT REQUEST	IRQ	Interrupt request.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the character attribute codes or field attribute codes.

Table 1. Pin Descriptions (Continued)

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
33 34	O	GENERAL PURPOSE ATTRIBUTE CODES	GPA_1 GPA_0	Outputs which are enabled by the general purpose field attribute codes.
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a DMA underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for character and field attributes) — to create blinking displays as specified by cursor, character attribute, or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to indicate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38 39	O	LINE ATTRIBUTE CODES	LA_0 LA_1	These attribute codes have to be decoded externally by the dot/timing logic to generate the horizontal and vertical line combinations for the graphic displays specified by the character attribute codes.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8275 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

$\overline{RD}$ (READ)

A "low" on this input informs the WD8275 that the CPU is reading data or status information from the WD8275.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8275 that the CPU is writing data or control words to the WD8275.

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8275. No reading or writing will occur unless the device is selected. When CS is high, the Data Bus in the float state and RD and WR will have no effect on the chip.

$\overline{DRQ}$ (DMA REQUEST)

A "high" on this output informs the DMA Controller that the WD8275 desires a DMA transfer.

$\overline{DACK}$ (DMA ACKNOWLEDGE)

A "low" on this input informs the WD8275 that a DMA cycle is in progress.

IRQ (INTERRUPT REQUEST)

A "high" on this output informs the CPU that the WD8275 desires interrupt service.

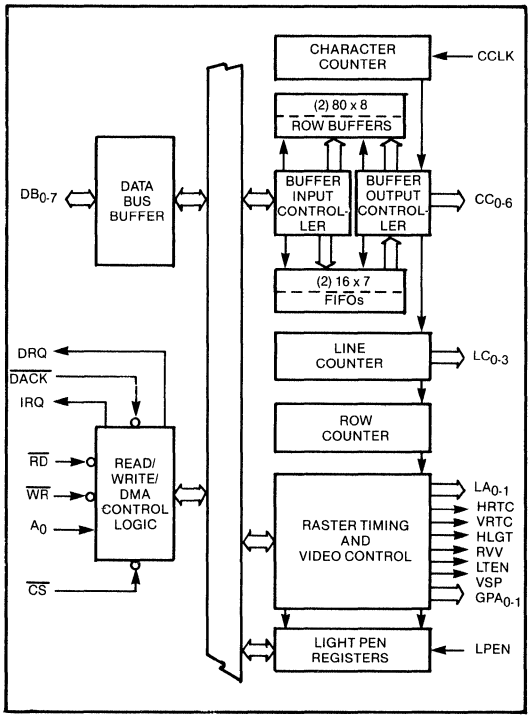


Figure 1.
WD8275 Functional Block Diagram

A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	Write WD8275 Parameter
0	1	0	0	Read WD8275 Parameter
1	0	1	0	Write WD8275 Command
1	1	0	0	Read WD8275 Status
X	1	1	0	Three-State
X	X	X	1	Three-State

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be a derivative of the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Sweeps) per character row. Its outputs are used to address the external character generator ROM.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Light Pen Registers

The Light Pen Registers are two registers that store the contents of the character counter and the row counter whenever there is a rising edge on the LPEN (Light Pen) input.

NOTE:
Software correction is required.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of LA_{0-1} (Line Attribute), HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters, the other is being filled with the next row of characters.

FIFOs

There are two 16 character FIFOs in the WD8275. They are used to provide extra row buffer length in the Transparent Attribute Mode (see Detailed Operation section).

Buffer Input/Output Controllers

The Buffer Input/output Controllers decode the characters being placed in the row buffers. If the character is a character attribute, field attribute or special code, these controllers control the appropriate action. (Examples: An "End of Screen-Stop DMA" special code will cause the Buffer Input Controller to stop further DMA requests. A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8275 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding, cursor timing, and light pen detection.

It is designed to interface with a DMA Controller and standard character generator ROMs for dot matrix decoding. Dot level timing must be provided by external circuitry.

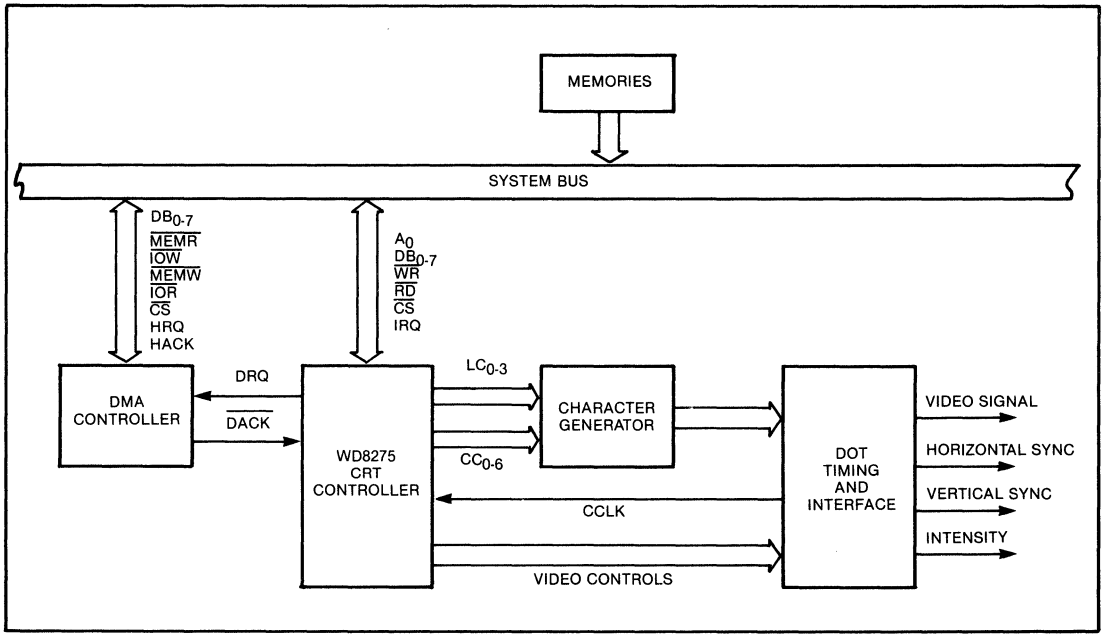


Figure 2. WD8275 Systems Block Diagram Showing Systems Operation

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

The WD8275 provides a "window" into the microcomputer system memory.

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8275 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8275 requests DMA to fill the row buffer that is not being used for display. DMA burst length and spacing is programmable. (See Programming Section.)

The WD8275 displays character rows one line at a time.

The number of lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8275 provides special Control Codes which can be used to minimize DMA or software overhead. It also provides Visual Attribute Codes to cause special action or symbols on the screen without the use of the character generator (see Visual Attributes Section).

The WD8275 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is programmable.

The WD8275 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

The WD8275 has a light pen input and registers. The light pen input is used to load the registers. Light pen registers can be read on command. (See Programming Section.)

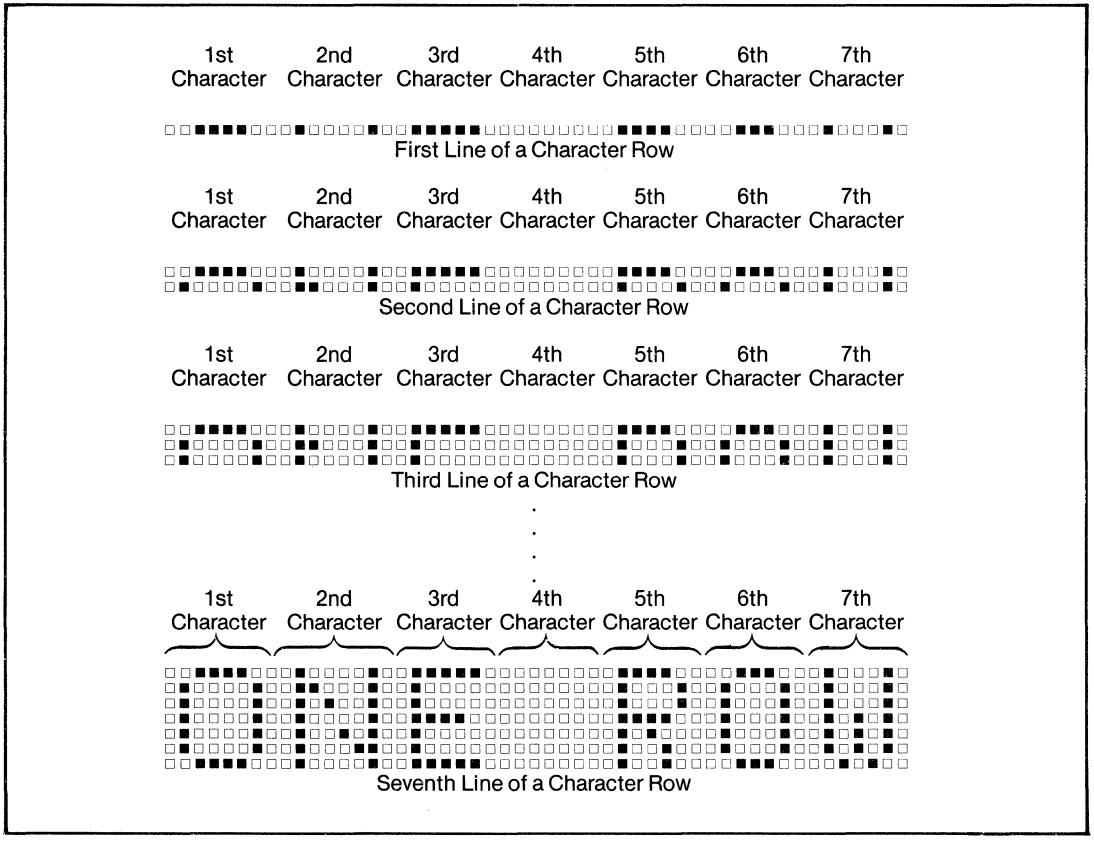


Figure 3. Display of a Character Row

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8275 requests DMA and one row buffer is filled with characters.

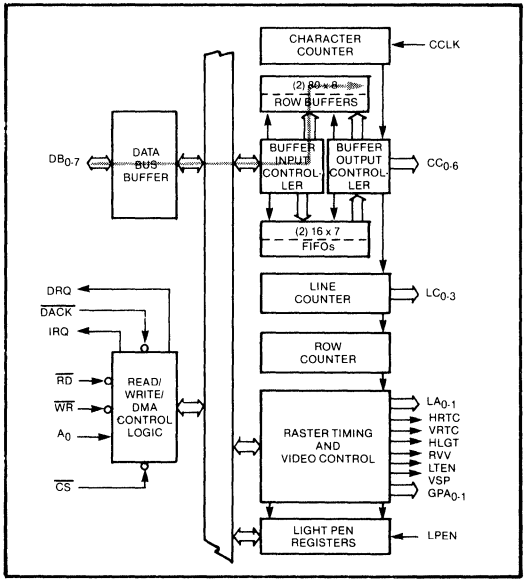


Figure 4.
First Row Buffer Filled

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, DMA begins filling the other row buffer with the next row of characters.

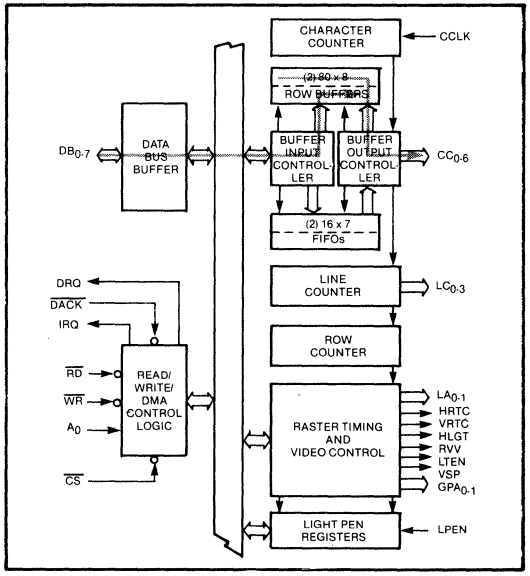


Figure 5.
Second Buffer Filled, First Row Displayed

After all the lines of the character row are scanned, the roles of the two row buffers are reversed and the same procedure is followed for the next row.

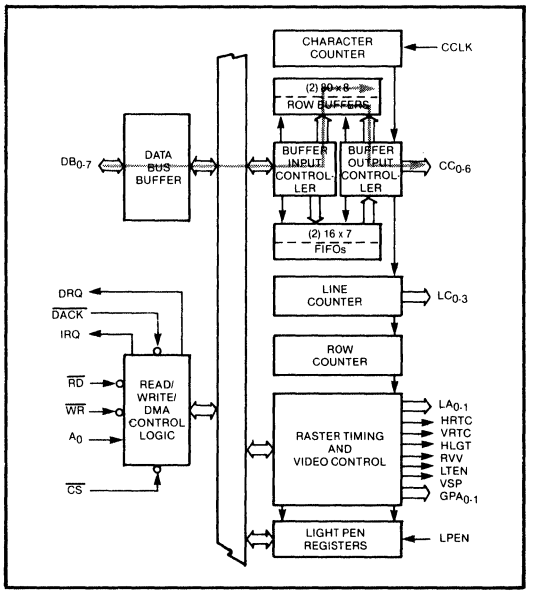


Figure 6.
First Buffer Filled with Third Row, Second Row Displayed

This is repeated until all of the character rows are displayed.

DISPLAY FORMAT

Screen Format

The WD8275 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

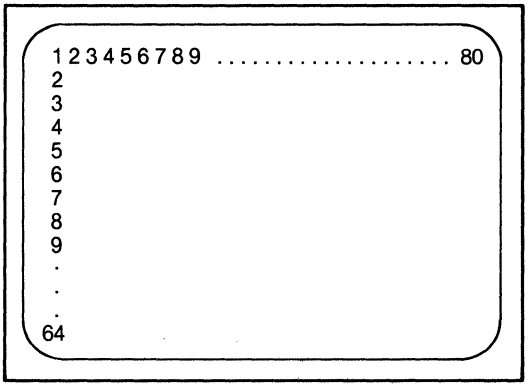


Figure 7.
Screen Format

The WD8275 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. DMA is not requested for the blanked rows.

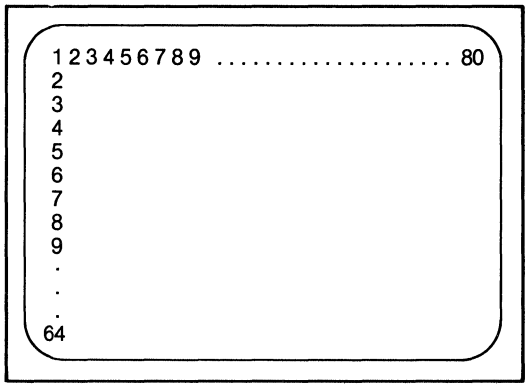


Figure 8.
Blank Alternative Rows Mode

Row Format

The WD8275 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number.*

In mode 1, the line *counter* is offset by one from the line *number.*

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0 0 0 0	1 1 1 1
1	□ □ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ □ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ □ □ □ □ □ ■ □	0 1 0 1	0 1 0 0
6	□ ■ ■ ■ ■ ■ ■ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ ■ □ □ □ □ □ ■ □	1 0 0 0	0 1 1 1
9	□ ■ □ □ □ □ □ ■ □	1 0 0 1	1 0 0 0
10	□ □ □ □ □ □ □ □ □	1 0 1 0	1 0 0 1
11	□ □ □ □ □ □ □ □ □	1 0 1 1	1 0 1 0
12	□ □ □ □ □ □ □ □ □	1 1 0 0	1 0 1 1
13	□ □ □ □ □ □ □ □ □	1 1 0 1	1 1 0 0
14	□ □ □ □ □ □ □ □ □	1 1 1 0	1 1 0 1
15	□ □ □ □ □ □ □ □ □	1 1 1 1	1 1 1 0

Figure 9.
Example of a 16-Line Format

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0 0 0 0	1 0 0 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ □ □ □ □ □ □	1 0 0 0	0 1 1 1
9	□ □ □ □ □ □ □	1 0 0 1	1 0 0 0

Figure 10.
Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □ □	0 0 0 0	1 0 1 1
1	□ □ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ □ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ □ □ □ □ □ ■ □	0 1 0 1	0 1 0 0
6	□ ■ ■ ■ ■ ■ ■ ■ □	0 1 1 0	0 1 0 1
7	□ ■ □ □ □ □ □ ■ □	0 1 1 1	0 1 1 0
8	□ ■ □ □ □ □ □ ■ □	1 0 0 0	0 1 1 1
9	□ ■ □ □ □ □ □ ■ □	1 0 0 1	1 0 0 0
10	■ ■ ■ ■ ■ ■ ■ ■ ■	1 0 1 0	1 0 0 1
11	□ □ □ □ □ □ □ □ □	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 11.
Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □ □	0 0 0 0	0 1 1 1
1	□ □ □ ■ □ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □ □	0 1 1 0	0 1 0 1
7	■ ■ ■ ■ ■ ■ ■ □	0 1 1 1	0 1 1 0

Top and Bottom Lines are not Blanked

Figure 12.
Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

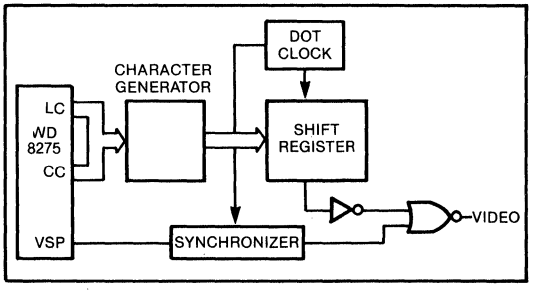


Figure 13.
Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This is constantly repeated.

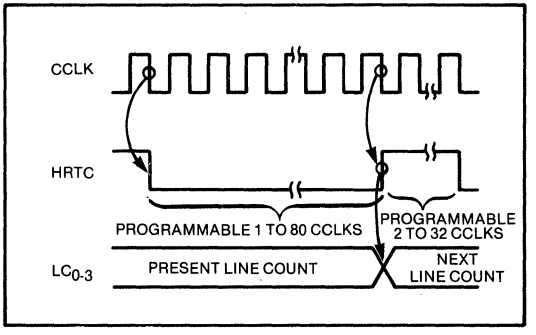


Figure 14.
Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

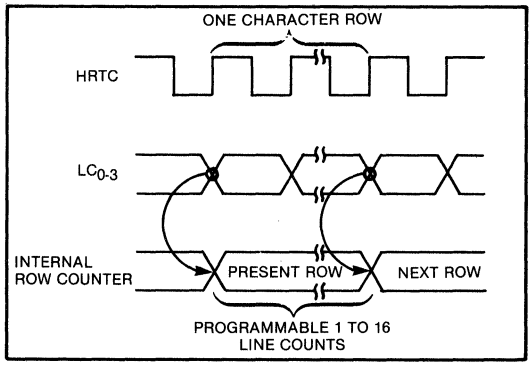


Figure 15. Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

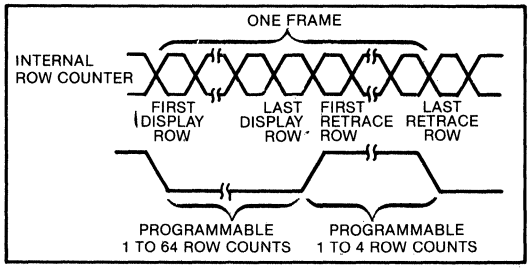


Figure 16. Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

DMA TIMING

The WD8275 can be programmed to request burst DMA transfers of 1 to 8 characters. The interval between bursts is also programmable (from 0 to 55 character clock periods ± 1). This allows the user to tailor his DMA overhead to fit his system needs.

The first DMA request of the frame occurs one *row time* before the end of vertical retrace. DMA requests continue as programmed, until the row buffer is filled. If the row buffer is filled in the middle of a burst, the WD8275 terminates the burst and resets the burst counter. No more DMA requests will occur until the *beginning* of the *next* row. At that time, DMA requests are activated as programmed until the other buffer is filled.

The first DMA request for a row will start at the first character clock of the preceding row. If the burst mode is used, the first DMA request may occur a number of character clocks later. This number is equal to the programmed burst space.

If, for any reason, there is a DMA underrun, a flag in the status word will be set.

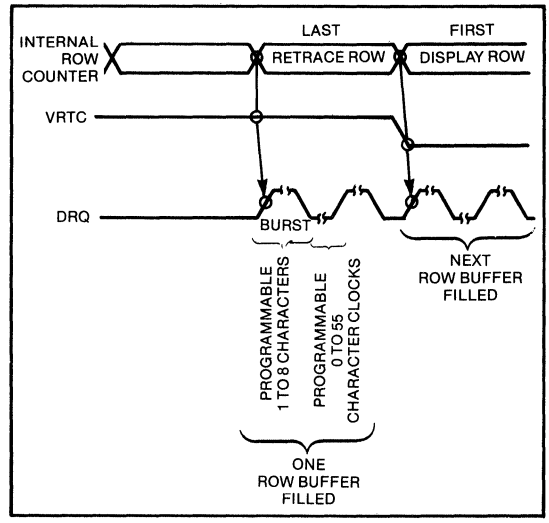


Figure 17. DMA Timing

The DMA controller is typically initialized for the next frame at the end of the current frame.

INTERRUPT TIMING

The WD8275 can be programmed to generate an interrupt request at the end of each frame. This can be used to reinitialize the DMA controller. If the WD8275 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

IRQ will go inactive after the status register is read.

A reset command will also cause IRQ to go inactive, but this is not recommended during normal service.

Another method of reinitializing the DMA controller is to have the DMA controller itself interrupt on terminal count. With this method, the WD8275 interrupt enable flag should not be set.

NOTE:
Upon power-up, the WD8275 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8275 before system interrupts are enabled.

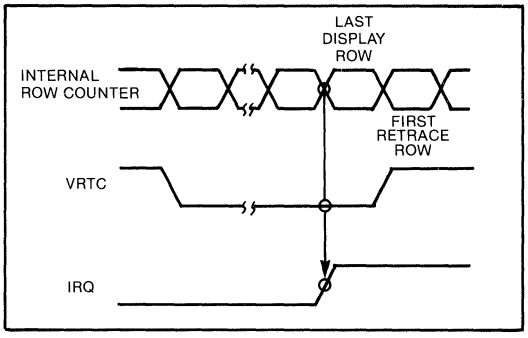


Figure 18.
Beginning of Interrupt Request

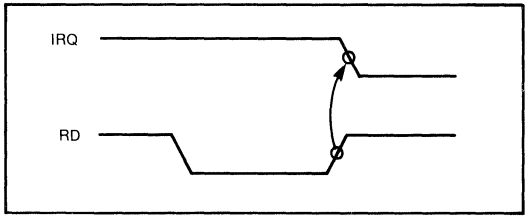


Figure 19.
End of Interrupt Request

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8275 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Visual Attribute or Special Code (MSB = 1).

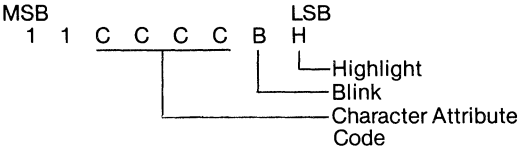
There are two types of Visual Attribute Codes. They are Character Attributes and Field Attributes.

Character Attribute Codes

Character attribute codes are codes that can be used to generate graphics symbols without the use of a character generator. This is accomplished by selectively activating the Line Attribute outputs (LA_{0-1}), the Video Suppression output (VSP), and the Light Enable output. The dot level timing circuitry can use these signals to generate the proper symbols.

Character attributes can be programmed to blink or be highlighted individually. Blinking is accomplished with the Video Suppression output (VSP). Blink frequency is equal to the screen refresh frequency divided by 32. Highlighting is accomplished by activating the Highlight output (HGLT).

Character Attributes



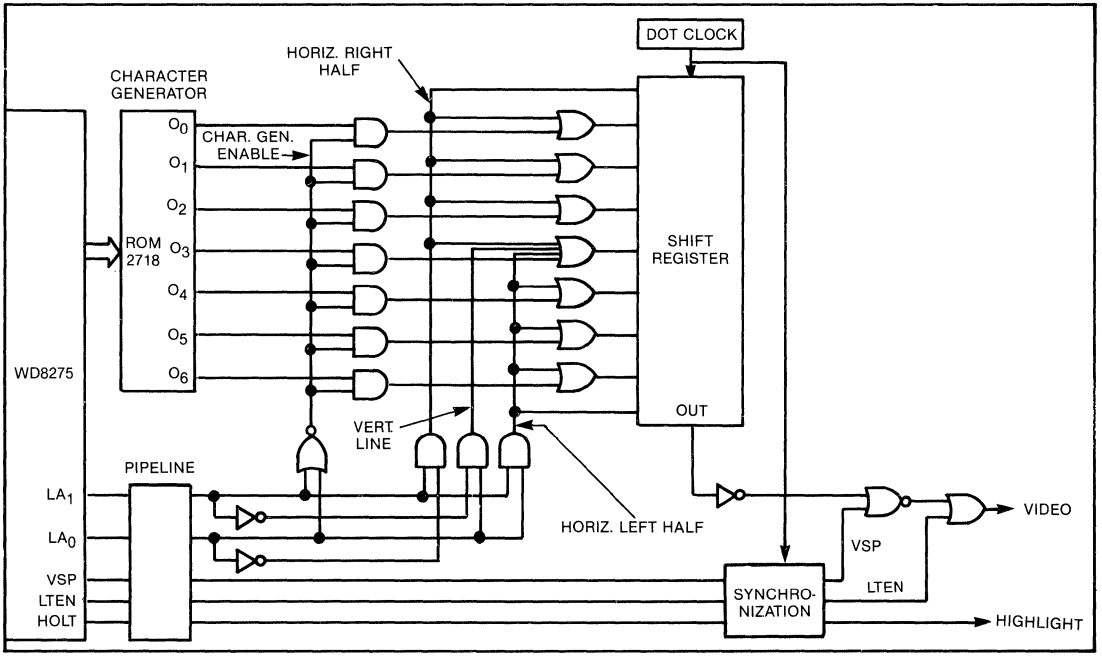
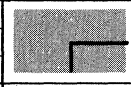
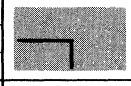
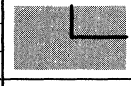
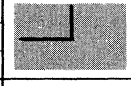
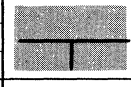
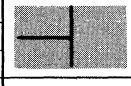
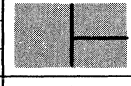
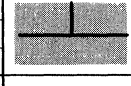
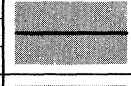
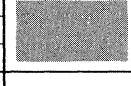


Figure 20. Typical Character Attribute Logic

Table 2. Character Attributes

Character attributes were designed to produce the following graphics:

CHARACTER ATTRIBUTE CODE "CCCC"		OUTPUTS LA_1	OUTPUTS LA_0	OUTPUTS VSP	OUTPUTS LTEN	SYMBOL	DESCRIPTION
0000	Above Underline	0	0	1	0		Top Left Corner
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0001	Above Underline	0	0	1	0		Top Right Corner
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0010	Above Underline	0	1	0	0		Bottom Left Corner
	Underline	1	0	0	0		
	Below Underline	0	0	1	0		
0011	Above Underline	0	1	0	0		Bottom Right Corner
	Underline	1	1	0	0		
	Below Underline	0	0	1	0		
0100	Above Underline	0	0	1	0		Top Intersect
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
0101	Above Underline	0	1	0	0		Right Intersect
	Underline	1	1	0	0		
	Below Underline	0	1	0	0		
0110	Above Underline	0	1	0	0		Left Intersect
	Underline	1	0	0	0		
	Below Underline	0	1	0	0		
0111	Above Underline	0	1	0	0		Bottom Intersect
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1000	Above Underline	0	0	1	0		Horizontal Line
	Underline	0	0	0	1		
	Below Underline	0	0	1	0		
1001	Above Underline	0	1	0	0		Vertical Line
	Underline	0	1	0	0		
	Below Underline	0	1	0	0		
1010	Above Underline	0	1	0	0		Crossed Lines
	Underline	0	0	0	1		
	Below Underline	0	1	0	0		
1011	Above Underline	0	0	0	0		Not Recommended*
	Underline	0	0	0	0		
	Below Underline	0	0	0	0		
1100	Above Underline	0	0	1	0		Special Codes
	Underline	0	0	1	0		
	Below Underline	0	0	1	0		
1101	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1110	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						
1111	Above Underline						Illegal
	Underline		Undefined				
	Below Underline						

*Character Attribute Code 1011 is not recommended for normal operation. Since none of the attribute outputs are active, the character Generator will not be disabled, and an indeterminate character will be generated.

Character Attribute Codes 1101, 1110, and 1111 are illegal.

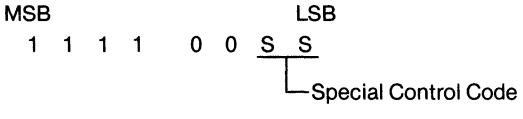
Blinking is active when B = 1.

Highlight is active when H = 1.

Special Codes

Four special codes are available to help reduce memory, software, or DMA overhead.

SPECIAL CONTROL CHARACTER



S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop DMA
1	0	End of Screen
1	1	End of Screen-Stop DMA

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop DMA Code (01) causes the DMA Control Logic to stop DMA for the rest of the row when it is written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop DMA Code (11) causes the DMA Control Logic to stop DMA for the rest of the frame when it is written into the Row Buffer. It affects the display in the same way as the End of Screen Code (10).

If the Stop DMA feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop DMA character is not the last character in a burst or row, DMA is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop DMA character.

Field Attributes

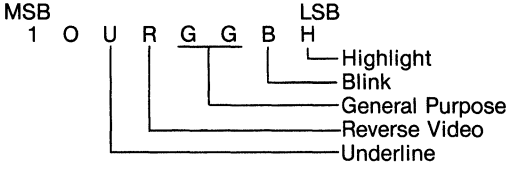
The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8275 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

The WD8275 can be programmed to provide visible or invisible field attribute characters.

If the WD8275 is programmed in the visible field attribute mode, all field attributes will occupy a position on the screen. They will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

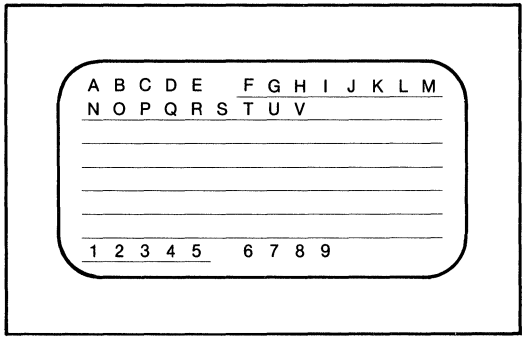


Figure 21.
Example of a Visible Field Attribute Mode (Underline Attribute)

If the WD8275 is programmed in the invisible field attribute mode, the WD8275 FIFO is activated.

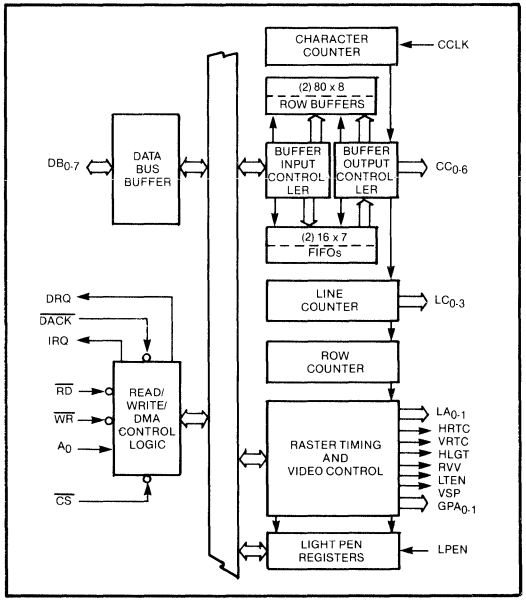


Figure 22.
Block Diagram Showing FIFO Activation

Each row buffer has a corresponding FIFO. These FIFOs are 16 characters by 7 bits in size.

When a field attribute is placed in the row buffer during DMA, the buffer input controller recognizes it and places the *next* character in the proper FIFO.

When a field attribute is placed in the Buffer Output Controller during display, it causes the controller to immediately put a character from the FIFO on the Character Code outputs (CC_{0-6}). The chosen Visual Attributes are also activated.

Since the FIFO is 16 characters long, no more than 16 field attribute characters may be used per line in this mode. If more are used, a bit in the status word is set and the first characters in the FIFO are written over and lost.

NOTE:
Since the FIFO is 7 bits wide, the MSB of any characters put in it are stripped off. Therefore, a Visual Attribute or Special Code must *not* immediately follow a field attribute code. If this situation does occur, the Visual Attribute or Special Code will be treated as a normal display character.

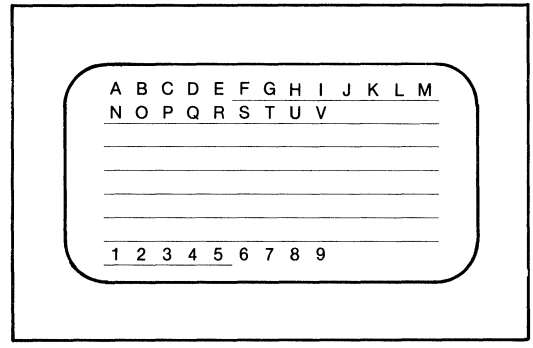


Figure 23.
Example of the Invisible Field Attribute Mode (Underline Attribute)

Field and Character Attribute Interaction

Character Attribute Symbols are affected by the Reverse Video (RVV) and General Purpose (GPA_{0-1}) field attributes. They are not affected by Underline, Blink or Highlight field attributes; however, these characteristics can be programmed *individually* for Character Attribute Symbols.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Light Pen Detection

A light pen consists of a micro switch and a tiny light sensor. When the light pen is pressed against the CRT screen, the micro switch enables the light sensor. When the raster sweep reaches the light sensor, it triggers the light pen output.

If the output of the light pen is presented to the WD8275 LPEN input, the row and character position coordinates are stored in a pair of registers. These registers can be read on command. A bit in the status word is set, indicating that the light pen signal was detected. The LPEN input must be a 0 to 1 transition for proper operation.

NOTE:
Due to internal and external delays, the character position coordinate will be off by at least three character positions. This has to be corrected in software.

Device Programming

The WD8275 has two programming registers, the Command Register (CREG) and the Parameter Register (PREG). It also has a Status Register (SREG). The Command Register can only be written into and the Status Registers can only be read from. They are addressed as follows:

A_0	OPERATION	REGISTER
0	Read	PREG
0	Write	PREG
1	Read	SREG
1	Write	CREG

The WD8275 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8275 instruction set consists of 8 commands.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Read Light Pen	2
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

In addition, the status of the WD8275 (SREG) can be read by the CPU at any time.

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M F C C Z Z Z Z

Action

After the reset command is written, DMA requests stop, WD8275 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V	V	NO. OF ROW COUNTS PER VRTC
0	0	1
0	1	2
1	0	3
1	1	4

Parameter—RRRRRR Vertical Rows/Frame

R	R	R	R	R	R	NO. OF ROWS/FRAME
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
			.			.
			.			.
			.			.
1	1	1	1	1	1	64

Parameter—UUUU Underline Placement

U	U	U	U	LINE NO. OF UNDERLINE
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—LLLL
Number of Lines per Character Row

L	L	L	L	NO. OF LINES/ROW
0	0	0	0	1
0	0	0	1	2
0	0	1	0	3
		.		.
		.		.
		.		.
1	1	1	1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—F Field Attribute Mode

F	FIELD ATTRIBUTE MODE
0	Transparent
1	Non-Transparent

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

2. Start Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 S S S B B
No parameters				

SSS Burst Space Code

S	S	S	NO. OF CHARACTER CLOCKS BETWEEN DMA REQUESTS
0	0	0	0
0	0	1	7
0	1	0	15
0	1	1	23
1	0	0	31
1	0	1	39
1	1	0	47
1	1	1	55

BB Burst Count Code

B	B	NO. OF DMA CYCLES PER BURST
0	0	1
0	1	2
1	0	4
1	1	8

Action
WD8275 interrupts are enabled, DMA requests begin, video is enabled, Interrupt Enable and Video Enable Status flags are set.

3. Stop Display Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Stop Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to re-enable the display.

4. Read Light Pen Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Read Light Pen	0 1 1 0 0 0 0 0
Parameters	Read Read	0 0	Char. Number Row Number	(Char. Position in Row) (Row Number)

Action

The WD8275 is conditioned to supply the contents of the light pen position registers in the next two read cycles of the parameter register. Status flags are not affected.

NOTE:
Software correction of light pen position is required.

5. Load Cursor Position

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write Write	0 0	Char. Number Row Number	(Char. Position in Row) (Row Number)

Action

The WD8275 is conditioned to place the next two parameter bytes into the cursor position registers. Status flags not affected.

6. Enable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

7. Disable Interrupt Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

8. Preset Counters Command

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	A_0	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR LP IC VE OU FO

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

LP —This flag is set when the light pen input (LPEN) is activated and the light pen registers have been loaded. This flag is automatically reset after a status read.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

DU —(DMA underrun) This flag is set whenever a data underrun occurs during DMA transfers. Upon detection of DU, the DMA operation is stopped and the screen is blanked until after the vertical retrace interval. This flag is reset after a status read.

FO —(FIFO Overrun) This flag is set whenever the FIFO is overrun. It is reset on a status read.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0.45V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}.

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating		100	ns	

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

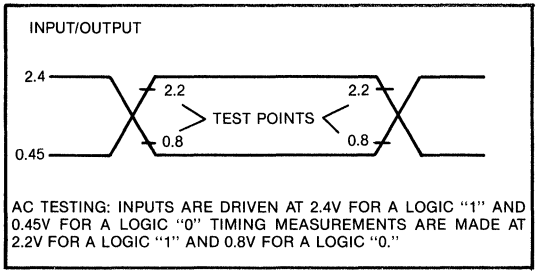
Clock Timing

		8275-00		8275-02			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		320		ns	
t_{KH}	Clock High	240		120		ns	
t_{KL}	Clock Low	160		120		ns	
t_{KR}	Clock Rise	5	30	5	30	ns	
t_{KF}	Clock Fall	5	30	5	30	ns	

Other Timing

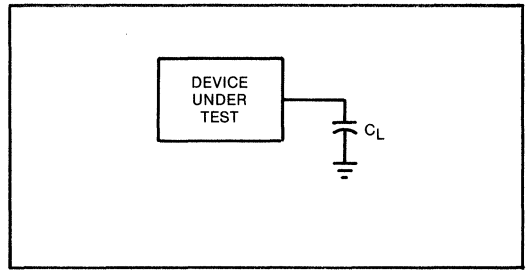
		8275-00		8275-02			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275		250	ns	C_L = 50 pF
t_{RI}	INT↓ from RD↑		250		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		200		200	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		0		ns	
t_{RL}	WR↑ to DACK↑	0		0		ns	
t_{PR}	LPEN Rise		50		50	ns	
t_{PH}	LPEN Hold	100		100		ns	

AC Testing Input, Output Wave Form



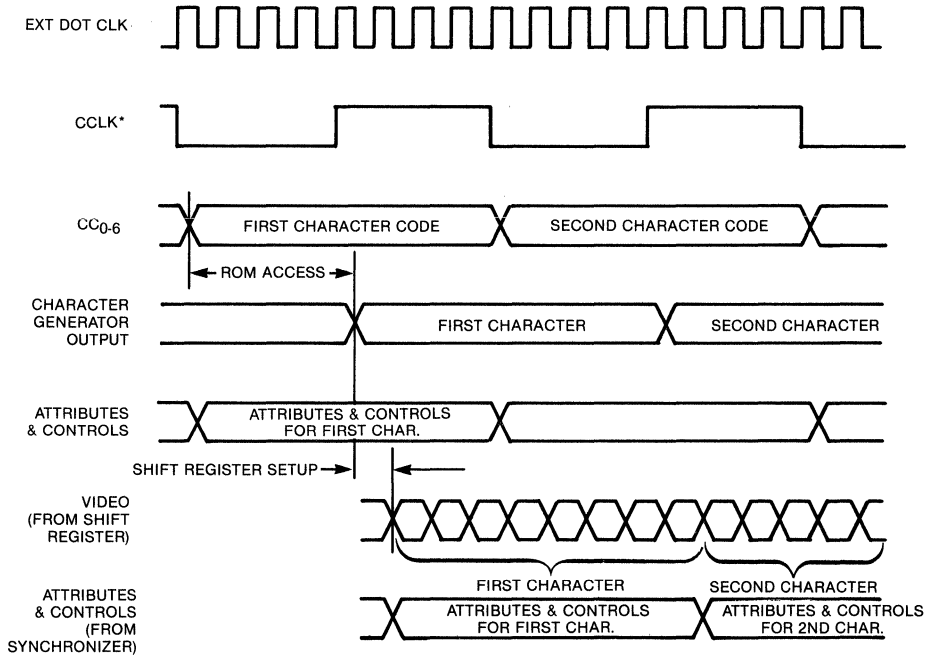
AC TESTING: INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0" TIMING MEASUREMENTS ARE MADE AT 2.2V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

AC Testing Load Circuit



WAVEFORMS

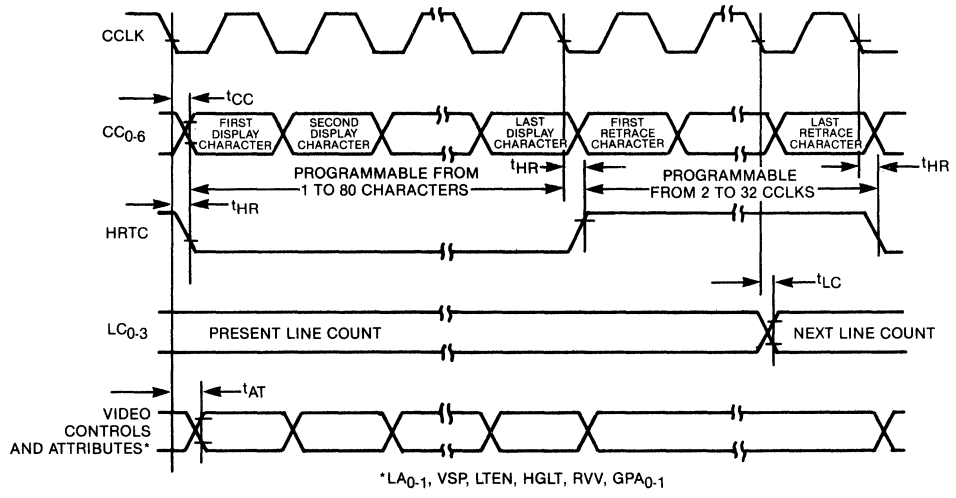
Typical Dot Level Timing



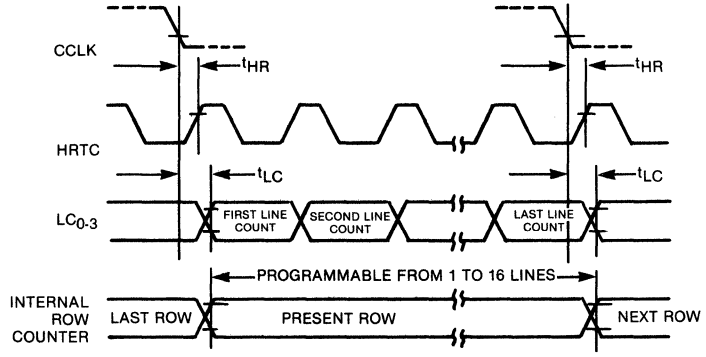
* CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8275.

WAVEFORMS (Continued)

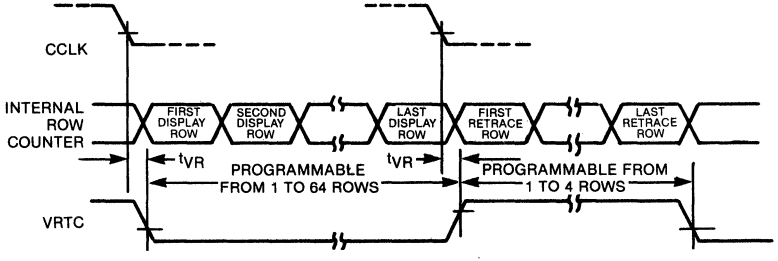
Line Timing



Row Timing

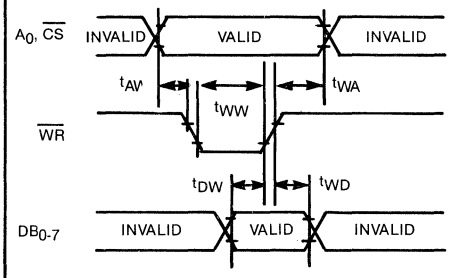


Frame Timing

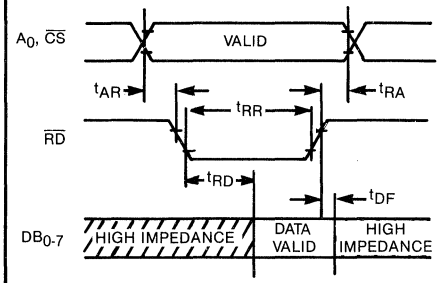


WAVEFORMS (Continued)

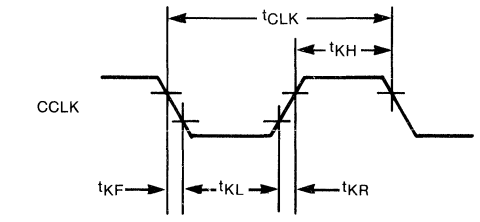
Write Timing



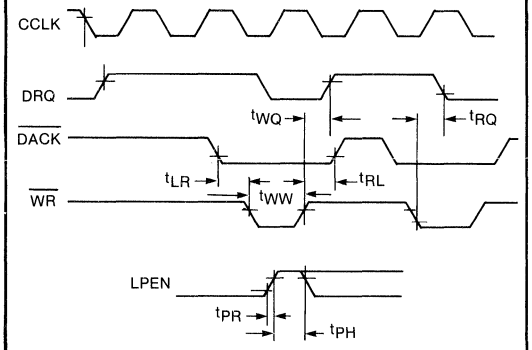
Read Timing



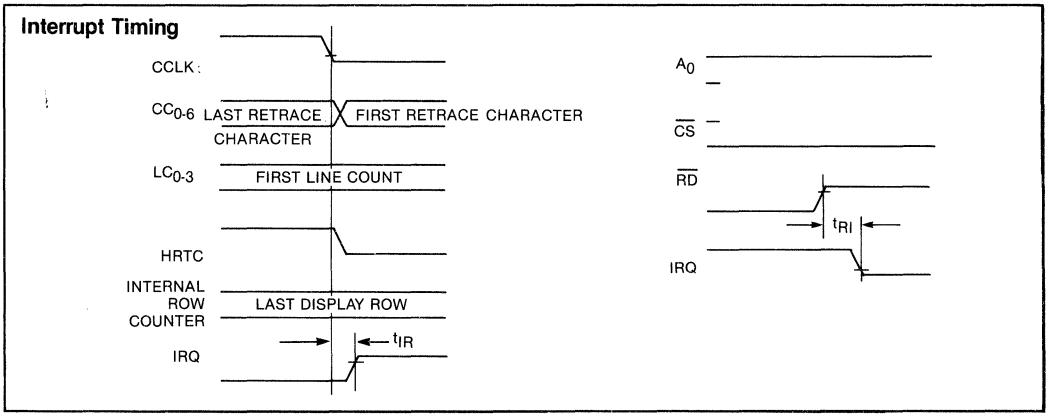
Clock Timing



DMA Timing



Interrupt Timing



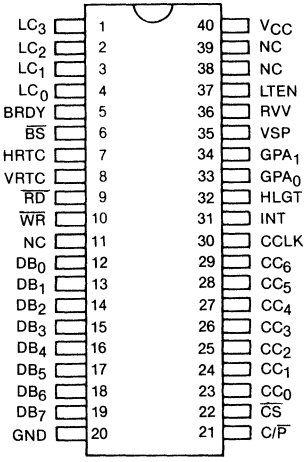
See page 383 for ordering information.

FINAL

WD8276 Small System CRT Controller

FEATURES

- PROGRAMMABLE SCREEN AND CHARACTER FORMAT
- 6 INDEPENDENT VISUAL FIELD ATTRIBUTES
- 11 VISUAL CHARACTER ATTRIBUTES (GRAPHIC CAPABILITY)
- CURSOR CONTROL (4 TYPES)
- LIGHT PEN DETECTION AND REGISTERS
- DUAL ROW BUFFERS
- PROGRAMMABLE DMA BURST MODE
- SINGLE +5V SUPPLY
- 40-PIN PACKAGE
- 2 MHz VERSION (WD8276-00)
- 3 MHz VERSION (WD8276-02)



Pin Designation

DESCRIPTION

The WD8276 Programmable CRT Controller is a single chip device to Interface CRT raster scan displays with microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the WD8276 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

Table 1. Pin Descriptions

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
1 2 3 4	O	LINE COUNT	LC_3 LC_2 LC_1 LC_0	Output from the line counter which is used to address the character generator for the line positions on the screen.
5	O	BUFFER READY	BRDY	Output signal indicating that a Row Buffer is ready for loading of character data.
6	I	BUFFER SELECT	$\overline{BS}$	Input signal enabling $\overline{WR}$ for character data into the Row Buffers.
7	O	HORIZONTAL RETRACE	HRTC	Output signal which is active during the programmed horizontal retrace interval. During this period the VSP output is high and the LTEN output is low.
8	O	VERTICAL RETRACE	VRTC	Output signal which is active during the programmed vertical retrace interval. During this period the VSP output is high and the LTEN output is low.
9	I	READ INPUT	$\overline{RD}$	A control signal to read registers.
10	I	WRITE INPUT	$\overline{WR}$	A control signal to write commands into the control registers or write data into the row buffers.
11		NO CONNECTION	NC	No connection
12 13 14 15 16 17 18 19	I/O	BIDIRECTIONAL DATA BUS	DB_0 DB_1 DB_2 DB_3 DB_4 DB_5 DB_6 DB_7	Three-state lines. The outputs are enabled during a read of the C or P ports.
20		GROUND	Ground	
21	I	PORT ADDRESS	$C/\overline{P}$	A high input on this pin selects the "C" port or command registers and a low input selects the "P" port or parameter registers.
22	I	CHIP SELECT	$\overline{CS}$	Enables $\overline{RD}$ of status or $\overline{WR}$ of command or parameters.
23 24 25 26 27 28 29	O	CHARACTER CODES	CC_0 CC_1 CC_2 CC_3 CC_4 CC_5 CC_6	Output from the row buffers used for character selection in the character generator.
30	I	CHARACTER CLOCK	CCLK	Character clock (from dot/timing logic).
31	O	INTERRUPT OUTPUT	INT	Interrupt output.
32	O	HIGHLIGHT	HLGT	Output signal used to intensify the display at particular positions on the screen as specified by the field attribute codes.
33 34	O	GENERAL PURPOSE ATTRIBUTE CODES	GPA_1 GPA_0	Outputs which are enabled by the general purpose field attribute codes.

Table 1. Pin Descriptions (Continued)

PIN NO.	TYPE	PIN NAME	SYMBOL	FUNCTION
35	O	VIDEO SUPPRESSION	VSP	Output signal used to blank the video signal to the CRT. This output is active: —during the horizontal and vertical retrace intervals. —at the top and bottom lines of rows if underline is programmed to be number 8 or greater. —when an end of row or end of screen code is detected. —when a Row Buffer underrun occurs. —at regular intervals (1/16 frame frequency for cursor, 1/32 frame frequency for attributes) — to create blinking displays as specified by cursor or field attribute programming.
36	O	REVERSE VIDEO	RVV	Output signal used to activate the CRT circuitry to reverse the video signal. This output is active at the cursor position if a reverse video block cursor is programmed or at the positions specified by the field attribute codes.
37	O	LIGHT ENABLE	LTEN	Output signal used to enable the video signal to the CRT. This output is active at the programmed underline cursor position, and at positions specified by attribute codes.
38		NO CONNECTION	NC	No connection.
39		NO CONNECTION	NC	No connection.
40		+5V POWER SUPPLY	V_{CC}	+5V power supply.

FUNCTIONAL DESCRIPTION

Data Bus Buffer

This 3-state, bidirectional, 8-bit buffer is used to interface the WD8276 to the system Data Bus.

This functional block accepts inputs from the System Control Bus and generates control signals for overall device operation. It contains the Command, Parameter, and Status Registers that store the various control formats for the device functional definition.

C/P	OPERATION	REGISTER
0	Read	RESERVED
0	Write	PARAMETER
1	Read	STATUS
1	Write	COMMAND

$\overline{RD}$ (READ)

A "low" on this input informs the WD8276 that the CPU is reading status information from the WD8276.

$\overline{WR}$ (WRITE)

A "low" on this input informs the WD8276 that the CPU is writing data or control words to the WD8276.

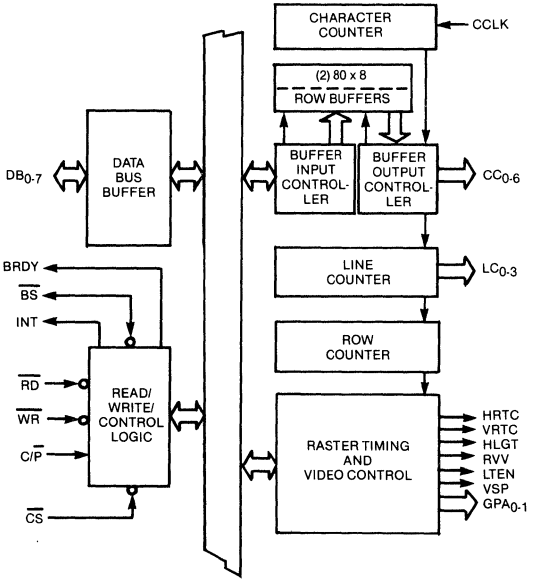


Figure 1.
WD8276 Functional Block Diagram

$\overline{CS}$ (CHIP SELECT)

A "low" on this input selects the WD8276 for $\overline{RD}$ or $\overline{WR}$ of Commands, Status, and Parameters.

BRDY (BUFFER READY)

A "high" on this output indicates that the WD8276 is ready to receive character data.

BS (BUFFER SELECT)

A "low" on this input enables $\overline{WR}$ of character data to the WD8276 row buffers.

INT (INTERRUPT)

A "high" on this output informs the CPU that the WD8276 needs interrupt service.

C/P	RD	WR	CS	BS	
0	0	1	0	1	Reserved
0	1	0	0	1	Write WD8276 Parameter
1	0	1	0	1	Read WD8276 Status
1	1	0	0	1	Write WD8276 Command
X	1	0	1	0	Write WD8276 Row Buffer
X	1	1	X	X	High Impedance
X	X	X	1	1	High Impedance

Character Counter

The Character Counter is a programmable counter that is used to determine the number of characters to be displayed per row and the length of the horizontal retrace interval. It is driven by the CCLK (Character Clock) input, which should be derived from the external dot clock.

Line Counter

The Line Counter is a programmable counter that is used to determine the number of horizontal lines (Raster Scans) per character row. Its outputs are used to address the external character generator.

Row Counter

The Row Counter is a programmable counter that is used to determine the number of character rows to be displayed per frame and length of the vertical retrace interval.

Raster Timing and Video Controls

The Raster Timing circuitry controls the timing of the HRTC (Horizontal Retrace) and VRTC (Vertical Retrace) outputs. The Video Control circuitry controls the generation of HGLT (Highlight), RVV (Reverse Video), LTEN (Light Enable), VSP (Video Suppress), and GPA_{0-1} (General Purpose Attribute) outputs.

Row Buffers

The Row Buffers are two 80-character buffers. They are filled from the microcomputer system memory with the character codes to be displayed. While one row buffer is displaying a row of characters,

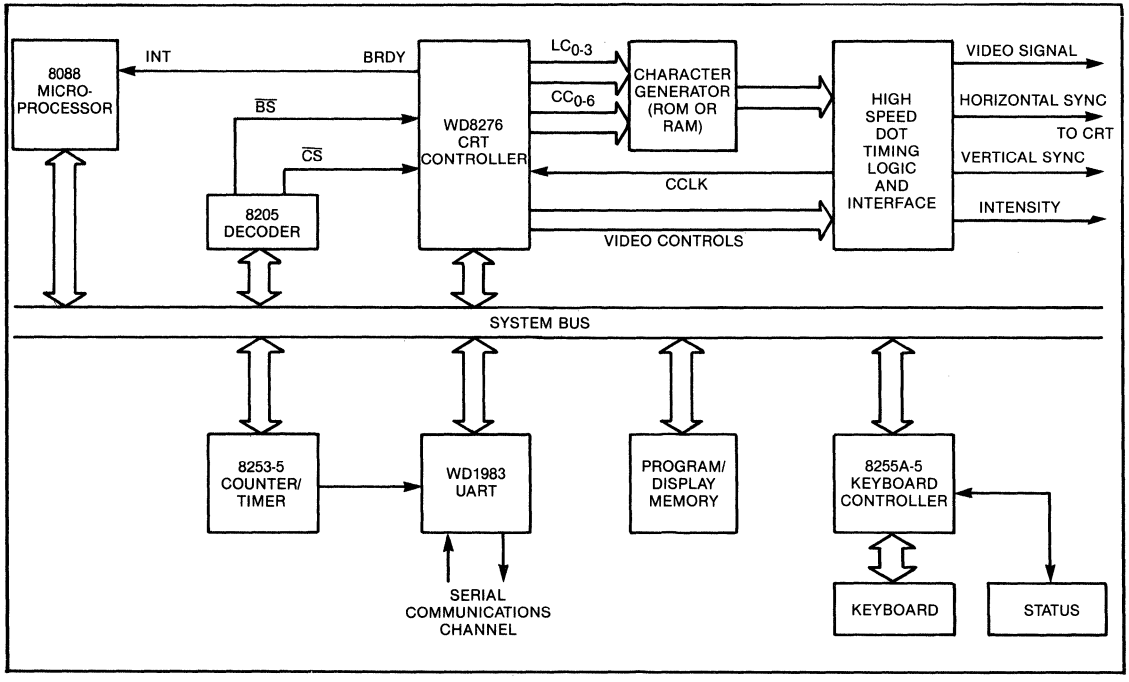


Figure 2. CRT System Block Diagram

the other is being filled with the next row of characters.

Buffer Input/Output Controllers

The Buffer Input/Output Controllers decode the characters being placed in the row buffers. If the character is a field attribute or special code, they control the appropriate action. (Example: A "Highlight" field attribute will cause the Buffer Output Controller to activate the HGLT output.)

SYSTEM OPERATION

The WD8276 is programmable to a large number of different display formats. It provides raster timing, display row buffering, visual attribute decoding and cursor timing.

It is designed to interface with standard character generators for dot matrix decoding. Dot level timing must be provided by external circuitry.

GENERAL SYSTEMS OPERATIONAL DESCRIPTION

Display characters are retrieved from memory and displayed on a row-by-row basis. The WD8276 has two row buffers. While one row buffer is being used for display, the other is being filled with the next row of characters to be displayed. The number of display characters per row and the number of character rows per frame are software programmable, providing easy interface to most CRT displays. (See Programming Section.)

The WD8276 uses BRDY to request character data to fill the row buffer that is not being used for display.

The WD8276 displays character rows one scan line at a time. The number of scan lines per character row, the underline position, and blanking of top and bottom lines are programmable. (See Programming Section.)

The WD8276 provides special Control Codes which can be used to minimize overhead. It also provides Visual Attribute Codes to cause special action on the screen without the use of the character generator. (See Visual Attributes Section.)

The WD8276 also controls raster timing. This is done by generating Horizontal Retrace (HRTC) and Vertical Retrace (VRTC) signals. The timing of these signals is also programmable.

The WD8276 can generate a cursor. Cursor location and format are programmable. (See Programming Section.)

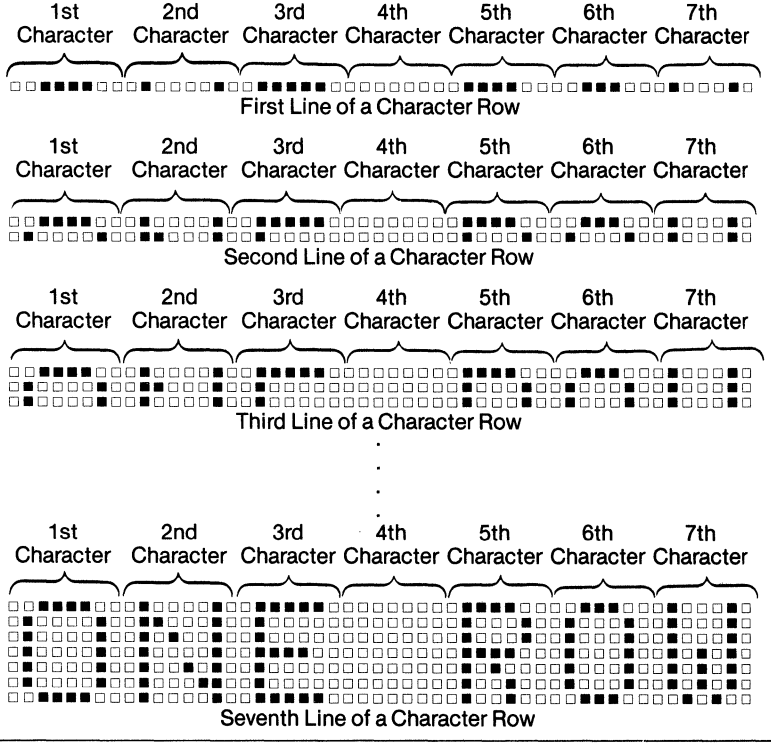


Figure 3. Display of a Character Row

DISPLAY ROW BUFFERING

Before the start of a frame, the WD8276 uses BRDY and $\overline{BS}$ to fill one row buffer with characters.

When the first horizontal sweep is started, character codes are output to the character generator from the row buffer just filled. Simultaneously, the other row buffer is filled with the next row of characters.

After all the lines of the character row are scanned, the buffers are swapped and the same procedure is followed for the next row.

This process is repeated until all of the character rows are displayed.

Row Buffering allows the CPU access to the display memory at all times except during Buffer Loading (about 25%). This compares favorably to alternative approaches which restrict CPU access to the display memory to occur only during horizontal and vertical retrace intervals (80% of the bus time is used to refresh the display.)

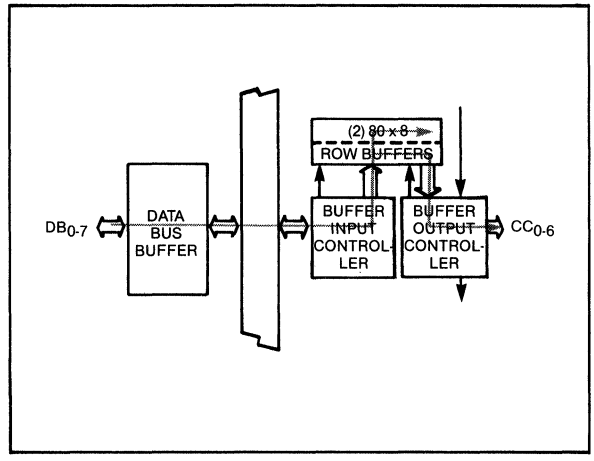


Figure 6.
First Buffer Filled with Third Row, Second Row Displayed

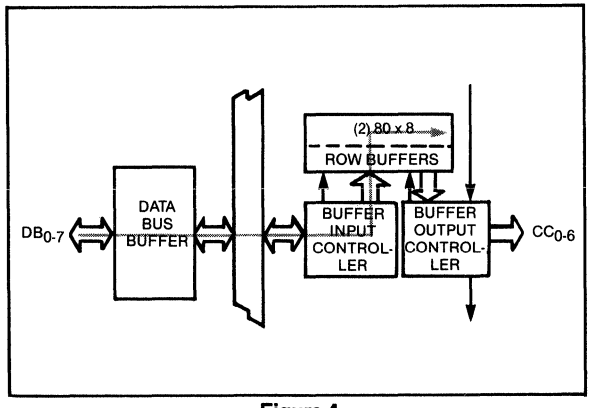


Figure 4.
First Row Buffer Filled

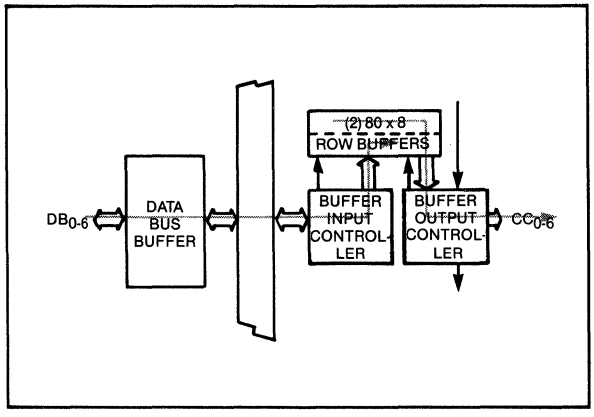


Figure 5.
Second Buffer Filled, First Row Displayed

DISPLAY FORMAT

Screen Format

The WD8276 can be programmed to generate from 1 to 80 characters per row, and from 1 to 64 rows per frame.

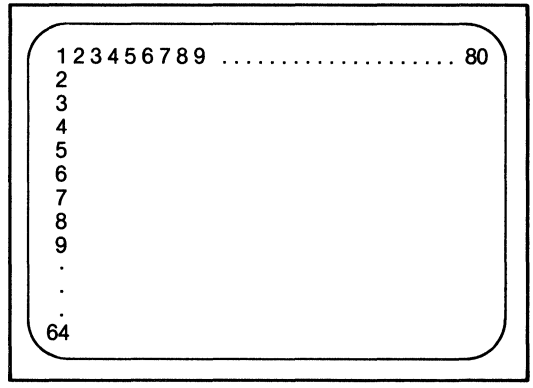


Figure 7.
Screen Format

The WD8276 can also be programmed to blank alternate rows. In this mode, the first row is displayed, the second blanked, the third displayed, etc. Display data is not requested for the blanked rows.

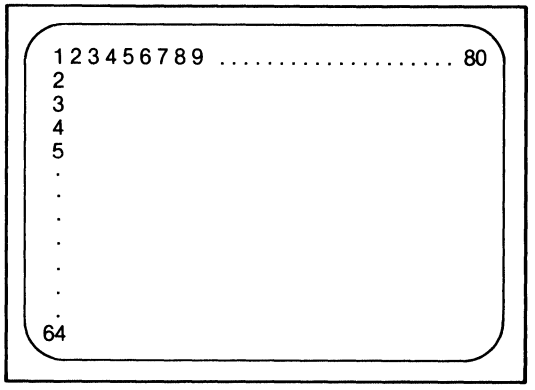


Figure 8.
Blank Alternative Rows Mode

Row Format

The WD8276 is designed to hold the line count stable while outputting the appropriate character codes during each horizontal sweep. The line count is incremented during horizontal retrace and the whole row of character codes are output again during the next sweep. This is continued until the entire character row is displayed.

The number of lines (horizontal sweeps) per character row is programmable from 1 to 16.

The output of the line counter can be programmed to be in one of two modes.

In mode 0, the output of the line *counter* is the same as the line *number*.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 1 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0
12	1 1 0 0	1 0 1 1
13	1 1 0 1	1 1 0 0
14	1 1 1 0	1 1 0 1
15	1 1 1 1	1 1 1 0

Figure 9.
Example of a 16-Line Format

In mode 1, the line *counter* is offset by one from the line *number*.

NOTE:
In mode 1, while the *first* line (line number 0) is being displayed, the *last* count is output by the line counter (see examples).

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 0 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0

Figure 10.
Example of a 10-Line Format

Mode 0 is useful for character generators that leave address zero blank and start at address 1. Mode 1 is useful for character generators which start at address zero.

Underline placement is also programmable (from line *number* 0 to 15). This is independent of the line *counter* mode.

If the line *number* of the underline is greater than 7 (line *number* MSB = 1), then the top and bottom lines will be blanked.

Line Number	Line Counter Mode 0	Line Counter Mode 1
0	0 0 0 0	1 0 1 1
1	0 0 0 1	0 0 0 0
2	0 0 1 0	0 0 0 1
3	0 0 1 1	0 0 1 0
4	0 1 0 0	0 0 1 1
5	0 1 0 1	0 1 0 0
6	0 1 1 0	0 1 0 1
7	0 1 1 1	0 1 1 0
8	1 0 0 0	0 1 1 1
9	1 0 0 1	1 0 0 0
10	1 0 1 0	1 0 0 1
11	1 0 1 1	1 0 1 0

Top and Bottom Lines are Blanked

Figure 11.
Underline in Line Number 10

If the line *number* of the underline is less than or equal to 7 (line *number* MSB = 0), then the top and bottom lines will *not* be blanked.

Line Number		Line Counter Mode 0	Line Counter Mode 1
0	□ □ □ □ □ □ □	0 0 0 0	0 1 1 1
1	□ □ □ ■ □ □ □	0 0 0 1	0 0 0 0
2	□ □ ■ □ ■ □ □	0 0 1 0	0 0 0 1
3	□ ■ □ □ □ ■ □	0 0 1 1	0 0 1 0
4	□ ■ □ □ □ ■ □	0 1 0 0	0 0 1 1
5	□ ■ ■ ■ ■ ■ □	0 1 0 1	0 1 0 0
6	□ ■ □ □ □ ■ □	0 1 1 0	0 1 0 1
7	■ ■ ■ ■ ■ ■ ■	0 1 1 1	0 1 1 0
	Top and Bottom Lines are not Blanked		

Figure 12.
Underline in Line Number 7

If the line *number* of the underline is greater than the maximum number of lines, the underline will not appear.

Blanking is accomplished by the VSP (Video Suppression) signal. Underline is accomplished by the LTEN (Light Enable) signal.

Dot Format

Dot width and character width are dependent upon the external timing and control circuitry.

Dot level timing circuitry should be designed to accept the parallel output of the character generator and shift it out serially at the rate required by the CRT display.

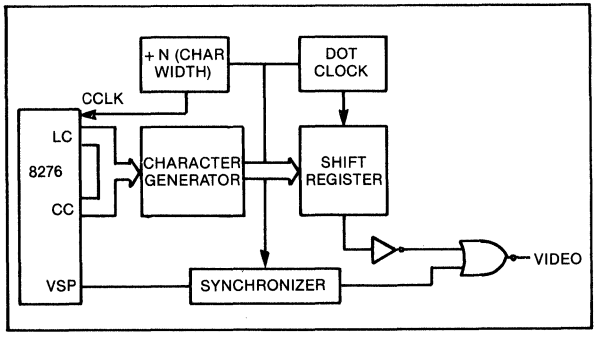


Figure 13.
Typical Dot Level Block Diagram

Dot width is a function of dot clock frequency.

Character width is a function of the character generator width.

Horizontal character spacing is a function of the shift register length.

NOTE:
Video control and timing signals must be synchronized with the video signal due to the character generator access delay.

RASTER TIMING

The character counter is driven by the character clock input (CCLK). It counts out the characters being displayed (programmable from 1 to 80). It then causes the line counter to increment, and it starts counting out the horizontal retrace interval (programmable from 2 to 32). This process is constantly repeated.

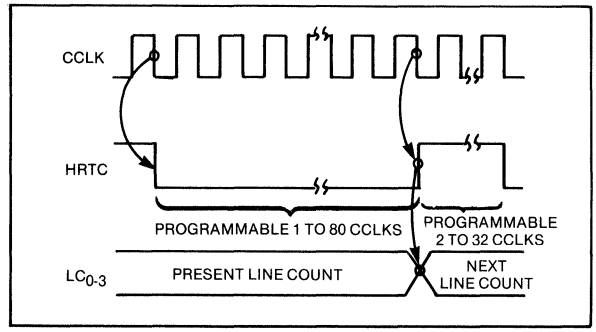


Figure 14.
Line Timing

The line counter is driven by the character counter. It is used to generate the line address outputs (LC_{0-3}) for the character generator. After it counts all of the lines in a character row (programmable from 1 to 16), it increments the row counter, and starts over again. (See Character Format Section for detailed description of Line Counter functions.)

The row counter is an internal counter driven by the line counter. It controls the functions of the row buffers and counts the number of character rows displayed.

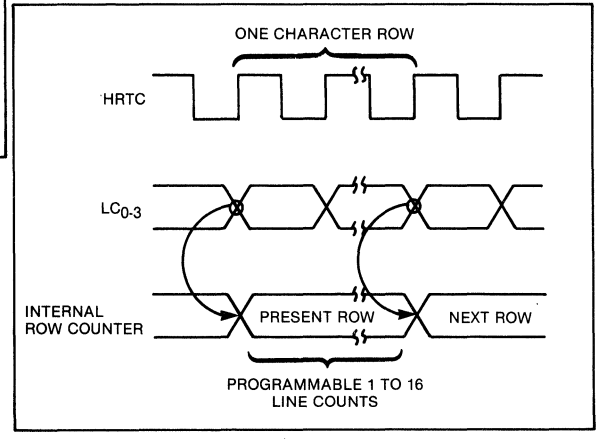


Figure 15.
Row Timing

After the row counter counts all of the rows in a frame (programmable from 1 to 64), it starts counting out the vertical retrace interval (programmable from 1 to 4).

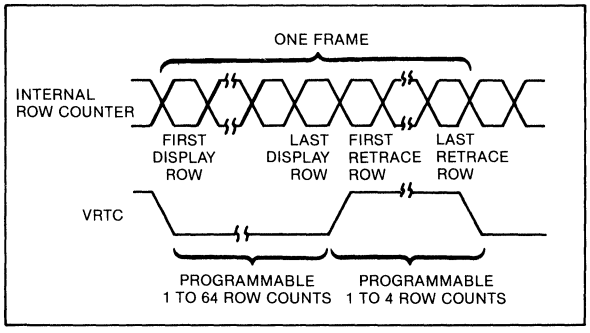


Figure 16.
Frame Timing

The Video Suppression Output (VSP) is active during horizontal and vertical retrace intervals.

Dot level timing circuitry must synchronize these outputs with the video signal to the CRT Display.

INTERRUPT TIMING

The WD8276 can be programmed to generate an interrupt request at the end of each frame. If the WD8276 interrupt enable flag is set, an interrupt request will occur at the *beginning* of the *last display row.*

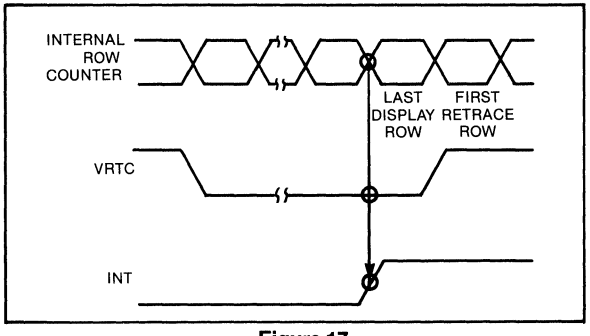


Figure 17.
Beginning of Interrupt

INT will go inactive after the status register is read.

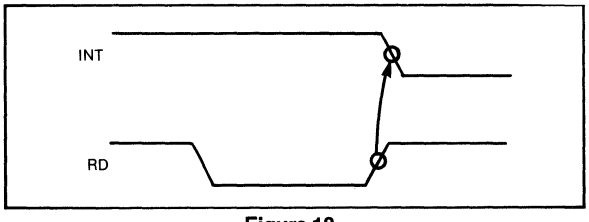


Figure 18.
End of Interrupt

A reset command will also cause INT to go inactive, but this is not recommended during normal service.

NOTE:
Upon power-up, the WD8276 Interrupt Enable Flag may be set. As a result, the user's cold start routine should write a reset command to the WD8276 before system interrupts are enabled.

VISUAL ATTRIBUTES AND SPECIAL CODES

The characters processed by the WD8276 are 8-bit quantities. The character code outputs provide the character generator with 7 bits of address. The Most Significant Bit is the extra bit and it is used to determine if it is a normal display character (MSB = 0), or if it is a Field Attribute or Special Code (MSB = 1).

Special Codes

Four special codes are available to help reduce bus usage.

SPECIAL CONTROL CHARACTER

MSB LSB

1 1 1 1 0 0 S S

Special Control Code

S	S	FUNCTION
0	0	End of Row
0	1	End of Row-Stop Buffer Loading
1	0	End of Screen
1	1	End of Screen-Stop Buffer Loading

The End of Row Code (00) activates VSP and holds it to the end of the line.

The End of Row-Stop Buffer Loading (BRDY) Code (01) causes the Buffer Loading Control Logic to stop buffer loading for the rest of the row upon being written into the Row Buffer. It affects the display in the same way as the End of Row Code (00).

The End of Screen Code (10) activates VSP and holds it to the end of the frame.

The End of Screen-Stop Buffer Loading (BRDY) Code (11) causes the Row Buffer Control Logic to stop buffer loading for the rest of the frame upon being written. It affects the display in the same way as the End of Screen Code (10).

If the Stop Buffer Loading feature is not used, all characters after an End of Row character are ignored, except for the End of Screen character, which operates normally. All characters after an End of Screen character are ignored.

NOTE:
If a Stop Buffer Loading is not the last character in a row, Buffer Loading is not stopped until after the next character is read. In this situation, a dummy character must be placed in memory after the Stop Buffer Loading character.

Field Attributes

The field attributes are control codes which affect the visual characteristics for a field of characters, starting at the character following the code up to, and including, the character which precedes the *next* field attribute code, or up to the end of the frame. The field attributes are reset during the vertical retrace interval.

The WD8276 can be programmed to provide visible field attribute characters; all field attribute codes will occupy a position on the screen. These codes will appear as blanks caused by activation of the Video Suppression output (VSP). The chosen visual attributes are activated after this blanked character.

There are six field attributes:

1. *Blink* — Characters following the code are caused to blink by activating the Video Suppression output (VSP). The blink frequency is equal to the screen refresh frequency divided by 32.
2. *Highlight* — Characters following the code are caused to be highlighted by activating the Highlight output (HGLT).
3. *Reverse Video* — Characters following the code are caused to appear with reverse video by activating the Reverse Video output (RVV).
4. *Underline* — Characters following the code are caused to be underlined by activating the Light Enable output (LTEN).

5,6. *General Purpose* — There are two additional WD8276 outputs which act as general purpose, independently programmable field attributes. GPA_{0-1} are active high outputs.

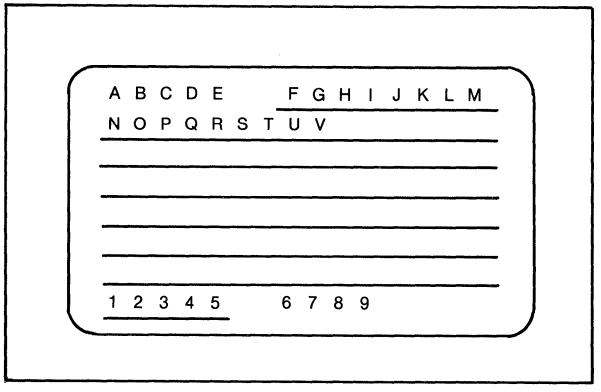
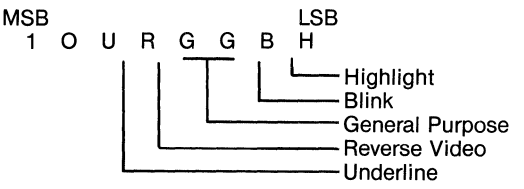


Figure 19.
End of a Visible Field Attribute (Underline Attribute)

FIELD ATTRIBUTE CODE



H = 1 for highlighting
B = 1 for blinking
R = 1 for reverse video
U = 1 for underline
GG = GPA_1, GPA_0

NOTE:
More than one attribute can be enabled at the same time. If the blinking and reverse video attributes are enabled simultaneously, only the reversed characters will blink.

Cursor Timing

The cursor location is determined by a cursor row register and a character position register which are loaded by command to the controller. The cursor can be programmed to appear on the display as:

1. a blinking underline
2. a blinking reverse video block
3. a non-blinking underline
4. a non-blinking reverse video block

The cursor blinking frequency is equal to the screen refresh frequency divided by 16.

If a non-blinking reverse video *cursor* appears in a non-blinking reverse video *field*, the cursor will appear as a normal video block.

If a non-blinking underline *cursor* appears in a non-blinking underline *field*, the cursor will not be visible.

Device Programming

The WD8276 has two programming registers, the Command Register and the Parameter Register. It also has a Status Register. The Command Register can only be written into and the Status Register can only be read from. They are addressed as follows:

C/$\overline{P}$	OPERATION	REGISTER
0	Read	Reserved
0	Write	Parameter
1	Read	Status
1	Write	Command

The WD8276 expects to receive a command and a sequence of 0 to 4 parameters, depending on the command. If the proper number of parameter bytes are not received before another command is given, a status flag is set, indicating an improper command.

INSTRUCTION SET

The WD8276 instruction set consists of 7 commands.

In addition, the status of the WD8276 can be read by the CPU at any time.

COMMAND	NO. OF PARAMETER BYTES
Reset	4
Start Display	0
Stop Display	0
Load Cursor	2
Enable Interrupt	0
Disable Interrupt	0
Preset Counters	0

1. Reset Command

	OPERATION	C/P	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Reset Command	0 0 0 0 0 0 0 0
Parameters	Write	0	Screen Comp Byte 1	S H H H H H H H
	Write	0	Screen Comp Byte 2	V V R R R R R R
	Write	0	Screen Comp Byte 3	U U U U L L L L
	Write	0	Screen Comp Byte 4	M 1 C C Z Z Z Z

Action

After the reset command is written, BRDY goes inactive, WD8276 interrupts are disabled, and the VSP output is used to blank the screen. HRTC and VRTC continue to run. HRTC and VRTC timing are random on power-up.

As parameters are written, the screen composition is defined.

Parameter—S Spaced Rows

S	FUNCTIONS
0	Normal Rows
1	Spaced Rows

Parameter—HHHHHHH Horizontal Characters/Row

H H H H H H H H	NO. OF CHARACTERS PER ROW
0 0 0 0 0 0 0	1
0 0 0 0 0 0 1	2
0 0 0 0 0 1 0	3
.	.
.	.
.	.
1 0 0 1 1 1 1	80
1 0 1 0 0 0 0	Undefined
.	.
.	.
.	.
1 1 1 1 1 1 1	Undefined

Parameter—VV Vertical Retrace Row Count

V V	NO. OF ROW COUNTS PER VRTC
0 0	1
0 1	2
1 0	3
1 1	4

Parameter—RRRRRR Vertical Rows/Frame

R R R R R R	NO. OF ROWS/FRAME
0 0 0 0 0 0	1
0 0 0 0 0 1	2
0 0 0 0 1 0	3
.	.
.	.
.	.
1 1 1 1 1 1	64

Parameter—UUUU Underline Placement

U U U U	LINE NO. OF UNDERLINE
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—LLLL
Number of Lines per Character Row

L L L L	NO. OF LINES/ROW
0 0 0 0	1
0 0 0 1	2
0 0 1 0	3
.	.
.	.
.	.
1 1 1 1	16

Parameter—M Line Counter Mode

M	LINE COUNTER MODE
0	Mode 0 (Non-Offset)
1	Mode 1 (Offset by 1 Count)

Parameter—CC Cursor Format

C	C	CURSOR FORMAT
0	0	Blinking reverse video block
0	1	Blinking underline
1	0	Non-blinking reverse video block
1	1	Non-blinking underline

NOTE:
uuuu MSB determines blanking of top and bottom lines (1 = blanked, 0 = not blanked).

Parameter—ZZZZ Horizontal Retrace Count

Z	Z	Z	Z	NO. OF CHARACTER COUNTS PER HRTC
0	0	0	0	2
0	0	0	1	4
0	0	1	0	6
		.		.
		.		.
		.		.
1	1	1	1	32

2. Start Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Start Display	0 0 1 0 0 0 0 0
No parameters				

Action

WD8276 interrupts are enabled, BRDY goes active, video is enabled, Interrupt Enable and Video Enable status flags are set.

3. Stop Display Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Stop Display	0 1 0 0 0 0 0 0
No parameters				

Action

Disables video, interrupts remain enabled, HRTC and VRTC continue to run, Video Enable status flag is reset, and the "Start Display" command must be given to reenable the display.

4. Load Cursor Position

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Load Cursor	1 0 0 0 0 0 0 0
Parameters	Write Write	0 0	Char. Number Row Number	(Char. Position in Row) (Row Number)

Action

The WD8276 is conditioned to place the next two parameter bytes into the cursor position registers. Status flag not affected.

5. Enable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Enable Interrupt	1 0 1 0 0 0 0 0
No parameters				

Action

The interrupt enable flag is set and interrupts are enabled.

6. Disable Interrupt Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Disable Interrupt	1 1 0 0 0 0 0 0
No parameters				

Action

Interrupts are disabled and the interrupt enable status flag is reset.

7. Preset Counters Command

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Write	1	Preset Counters	1 1 1 0 0 0 0 0
No parameters				

Action

The internal timing counters are preset, corresponding to a screen display position at the top left corner. Two character clocks are required for this operation. The counters will remain in this state until any other command is given.

This command is useful for system debug and synchronization of clustered CRT displays on a single CPU.

STATUS FLAGS

	OPERATION	C/$\overline{P}$	DESCRIPTION	DATA BUS MSB LSB
Command	Read	1	Status Word	0 IE IR X IC VE BU X

IE —(Interrupt Enable) Set or reset by command. It enables vertical retrace interrupt. It is automatically set by a "Start Display" command and reset with the "Reset" command.

IR —(Interrupt Request) This flag is set at the beginning of display of the last row of the frame if the interrupt enable flag is set. It is reset after a status read operation.

IC —(Improper Command) This flag is set when a command parameter string is too long or too short. The flag is automatically reset after a status read.

VE —(Video Enable) This flag indicates that video operation of the CRT is enabled. This flag is set on a "Start Display" command, and reset on a "Stop Display" or "Reset" command.

BU —(Buffer Underrun) This flag is set whenever a Row Buffer is not filled with character data in time for a buffer swap required by the display. Upon activation of this bit, buffer loading ceases, and the screen is blanked until after the vertical retrace interval.

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 1 Watt

*NOTICE:
Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

DC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5V ±5%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IL}	Input Low Voltage	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} +0.5V	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2.2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = −400 μA
I_{IL}	Input Load Current		±10	μA	V_{IN} = V_{CC} to 0V
I_{OFL}	Output Float Leakage		±10	μA	V_{OUT} = V_{CC} to 0.45V
I_{CC}	V_{CC} Supply Current		160	mA	

Capacitance (T_A = 25°C; V_{CC} = GND = 0V)

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
C_{IN}	Input Capacitance		10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		20	pF	Unmeasured pins returned to V_{SS}

AC Characteristics (T_A = 0°C to 70°C; V_{CC} = 5.0V ±5%; GND = 0V)

BUS PARAMETERS (Note 1)

Read Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AR}	Address Stable Before READ	0		ns	
t_{RA}	Address Hold Time for READ	0		ns	
t_{RR}	READ Pulse Width	250		ns	
t_{RD}	Data Delay from READ		200	ns	C_L = 150pF
t_{DF}	READ to Data Floating		100	ns	

Write Cycle

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
t_{AW}	Address Stable Before WRITE	0		ns	
t_{WA}	Address Hold Time for WRITE	0		ns	
t_{WW}	WRITE Pulse Width	250		ns	
t_{DW}	Data Setup Time for WRITE	150		ns	
t_{WD}	Data Hold Time for WRITE	0		ns	

Clock Timing

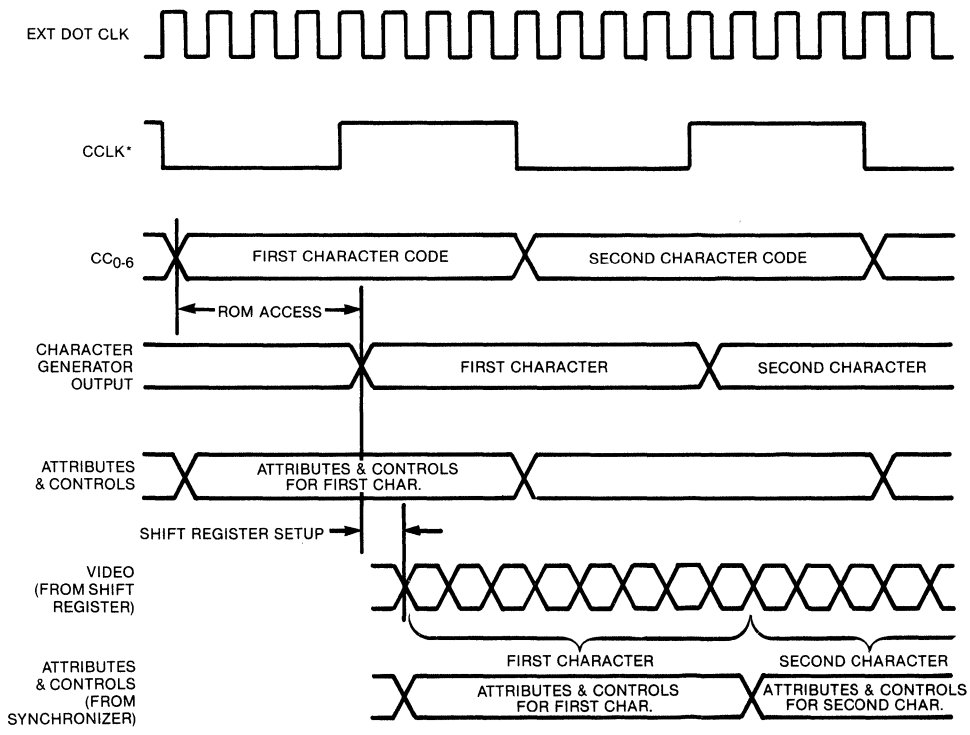
		8276-00		8276-02			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
t_{CLK}	Clock Period	480		320		ns	
t_{KH}	Clock High	240		120		ns	
t_{KL}	Clock Low	160		120		ns	
t_{KR}	Clock Rise	5	30	5	30	ns	
t_{KF}	Clock Fall	5	30	5	30	ns	

Other Timing

		8276-00		8276-02			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS
t_{CC}	Character Code Output Delay		150		150	ns	C_L = 50 pF
t_{HR}	Horizontal Retrace Output Delay		200		150	ns	C_L = 50 pF
t_{LC}	Line Count Output Delay		400		250	ns	C_L = 50 pF
t_{AT}	Control/Attribute Output Delay		275		250	ns	C_L = 50 pF
t_{VR}	Vertical Retrace Output Delay		275		250	ns	C_L = 50 pF
t_{RI}	INT↓ from RD↑		250		250	ns	C_L = 50 pF
t_{WQ}	DRQ↑ from WR↑		250		250	ns	C_L = 50 pF
t_{RQ}	DRQ↓ from WR↓		200		200	ns	C_L = 50 pF
t_{LR}	DACK↓ to WR↓	0		0		ns	
t_{RL}	WR↑ to DACK↑	0		0		ns	
t_{PR}	LPEN Rise		50		50	ns	
t_{PH}	LPEN Hold	100		100		ns	

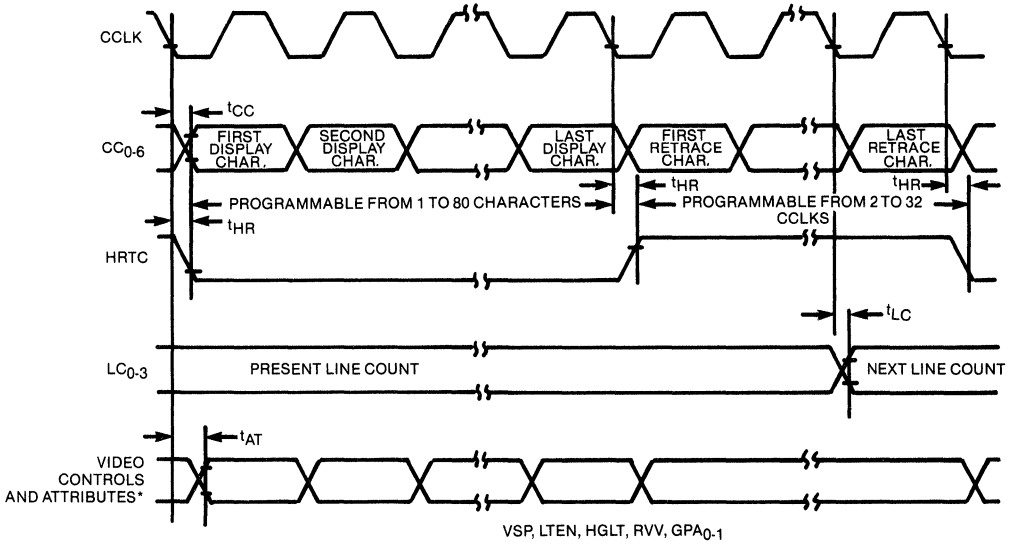
WAVEFORMS

Typical Dot Level Timing

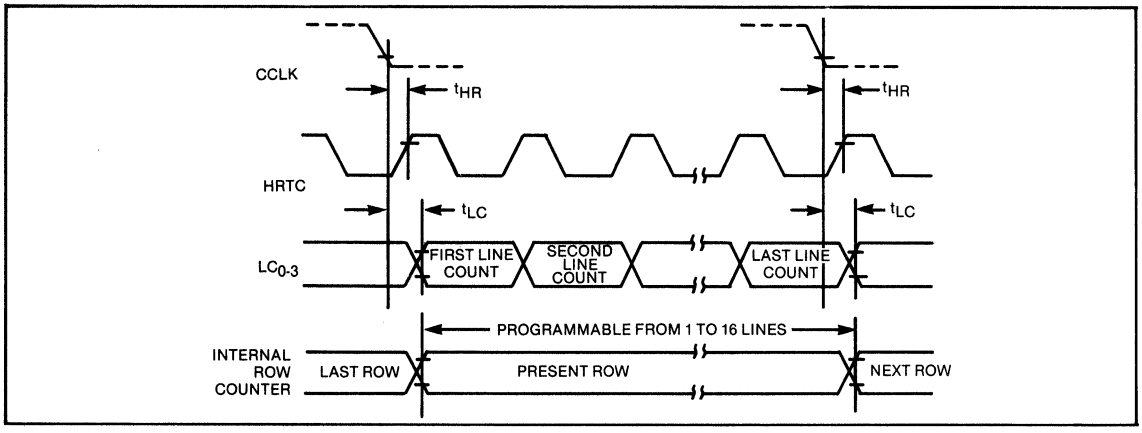


* CCLK IS A MULTIPLE OF THE DOT CLOCK AND AN INPUT TO THE 8276.

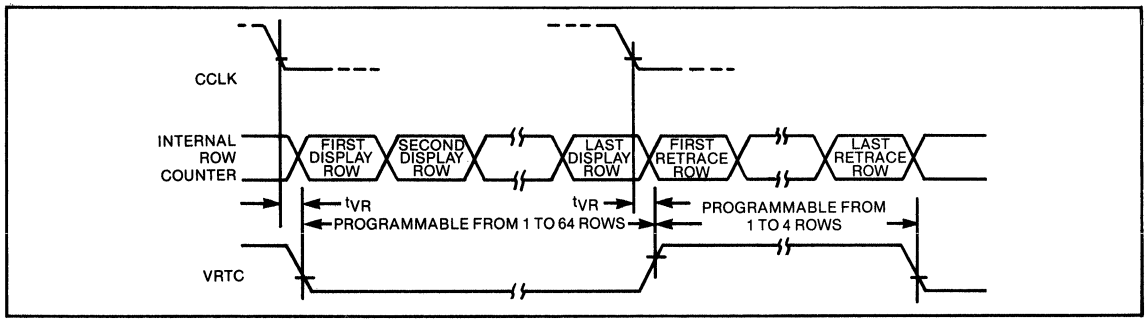
Line Timing



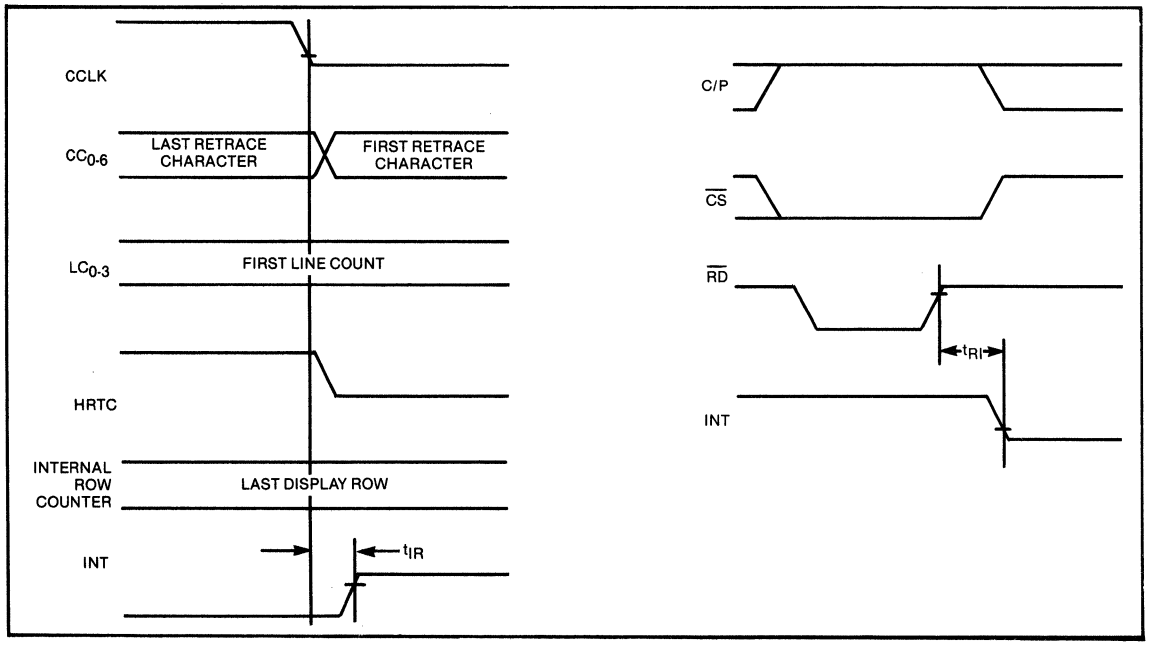
Row Timing



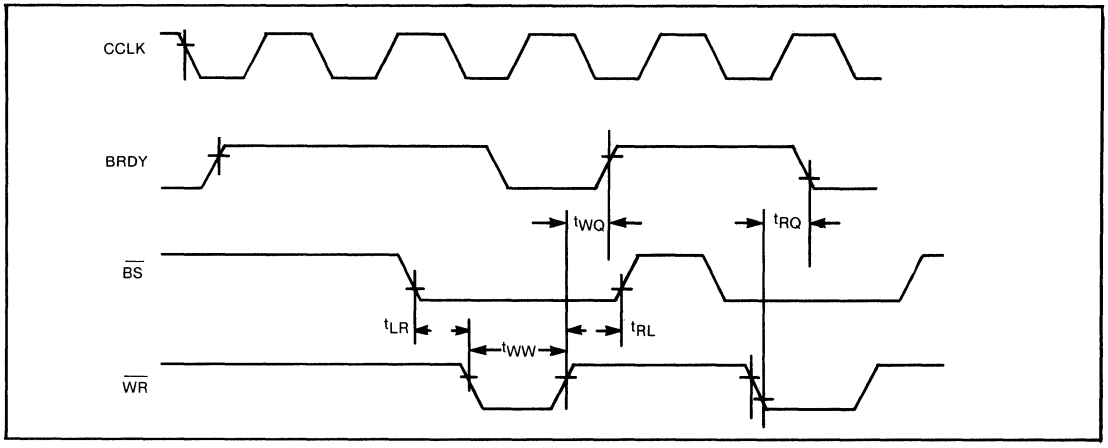
Frame Timing



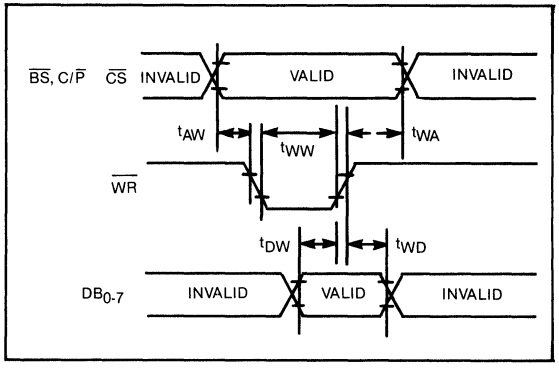
Interrupt Timing



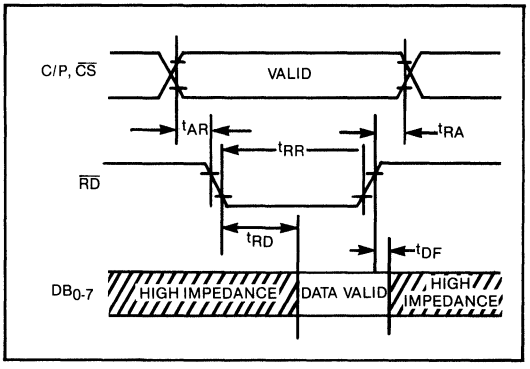
Timing for Buffer Loading



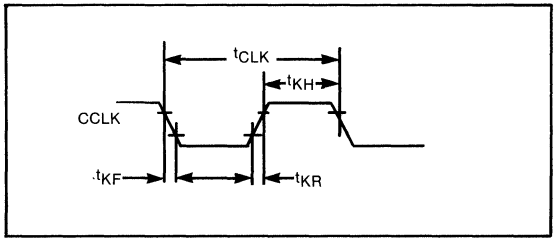
Write Timing



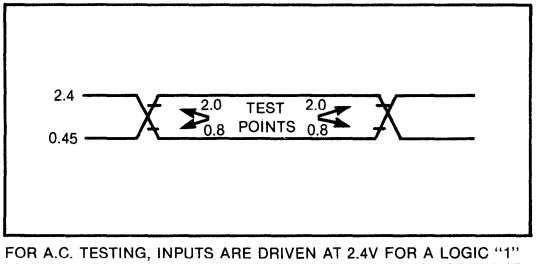
Read Timing



Clock Timing



Input and Output Waveforms for A.C. Tests



FOR A.C. TESTING, INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC "1" AND 0.45V FOR A LOGIC "0." TIMING MEASUREMENTS FOR INPUT AND OUTPUT SIGNALS ARE MADE AT 2.0V FOR A LOGIC "1" AND 0.8V FOR A LOGIC "0."

See page 383 for ordering information.

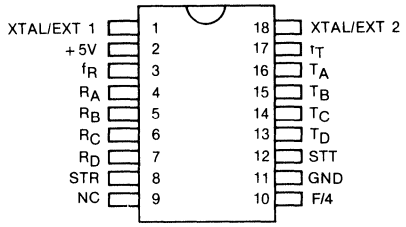
Printed in U.S.A.

FINAL

WD1943(8136) Dual Baud Rate Clock

FEATURES

- 16 SELECTABLE BAUD RATE CLOCK FREQUENCIES
- OPERATES WITH CRYSTAL OSCILLATOR OR EXTERNALLY GENERATED FREQUENCY INPUT
- ROM MASKABLE FOR NON-STANDARD FREQUENCY SELECTIONS
- INTERFACES EASILY WITH MICROCOMPUTERS
- OUTPUTS A 50% DUTY CYCLE CLOCK WITH 0.01% ACCURACY
- 6 DIFFERENT FREQUENCY/DIVISOR PAIRS AVAILABLE
- SINGLE +5V POWER SUPPLY
- COMPATIBLE WITH BR1941
- TTL, MOS COMPATIBILITY
- XTAL FREQ ÷ 4 OUTPUT INCLUDED
- WD1943 IS PIN COMPATIBLE TO THE COM8136 AND COM5036 (PIN 9 ON WD1943 IS A NO CONNECT)
- CAN REPLACE COM8116 AND COM5016 (Contact Western Digital Representative)



PIN DESIGNATION

DESCRIPTION

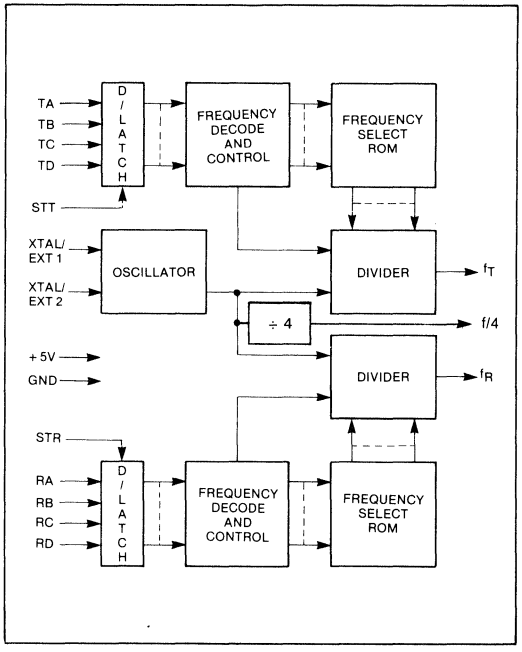
The WD1943 is a combination Baud Rate Clock Generator and Programmable Divider. It is manufactured in N-channel MOS using silicon gate technology. This device is capable of generating 16 externally selected clock rates whose frequency is determined by either a single crystal or an externally generated input clock. The WD1943 is a programmable counter capable of generating a division by any integer from 4 to $2^{15} - 1$, inclusive.

The WD1943 is available programmed with the most used frequencies in data communication. Each frequency is selectable by strobing or hard wiring each of the two sets of four Rate Select inputs. Other frequencies/division rates can be generated by reprogramming the internal ROM coding through a MOS mask change. Additionally, further clock division may be accomplished through cascading of devices. The frequency output is fed into the XTAL/EXT input on a subsequent device.

The WD1943 can be driven by an external crystal or by TTL logic.

PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	FUNCTION
1	XTAL/EXT 1	Crystal or External Input 1	This input receives one pin of the crystal package or one polarity of the external input.
2	V_{CC}	Power Supply	+5 volt Supply
3	f_R	Receiver Output Frequency	This output runs at a frequency selected by the Receiver Address inputs.
4-7	R_A, R_B, R_C, R_D	Receiver Address	The logic level on these inputs as shown in Table 1 thru 6, selects the receiver output frequency, f_R.
8	STR	Strobe-Receiver Address	A high-level input strobe loads the receiver address (R_A, R_B, R_C, R_D) into the receiver address register. This input may be strobed or hard wired to +5V.
9	NC	No Connection	No Internal Connection
10	F/4	XTAL freq ÷ 4 Output	XTAL1 input freq divided by four.
11	GND	Ground	Ground
12	STT	Strobe-Transmitter Address	A high-level input strobe loads the transmitter address (T_A, T_B, T_C, T_D) into the transmitter address register. This input may be strobed or hard wired to +5V.
13-16	T_D, T_C, T_B, T_A	Transmitter Address	The logic level on these inputs, as shown in Table 1 thru 6, selects the transmitter output frequency, f_T.
17	f_T	Transmitter Output Frequency	This output runs at a frequency selected by the Transmitter Address inputs.
18	XTAL/EXT 2	Crystal or External Input 2	This input receives the other pin of the crystal package or the other polarity of the external input.



BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS (T_A = 0°C to +70°C, V_{CC} = +5V ±5% standard.)

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
DC CHARACTERISTICS					
INPUT VOLTAGE LEVELS					
Low-level, V_{IL}			0.8	V	See Note 1
High-level, V_{IH}	2.0		V_{CC}	V	
OUTPUT VOLTAGE LEVELS					
Low-level, V_{OL}			0.4	V	I_{OL} = 3.2 mA
High-level, V_{OH}	V_{CC}-1.5	4.0		V	I_{OH} = 100μA
INPUT CURRENT					
High-level, I_{IH}			−10	μA	$V_{IN} = V_{CC}$ } STR (8) and STT (12) Only
Low-level, I_{IL}			10	μA	V_{IN} = GND }
Low-level, I_{IL}			300	μA	V_{IN} = GND (All inputs except XTAL, STR and STT)
INPUT CAPACITANCE					
All Inputs, C_{IN}		5	10	pf	V_{IN} = GND, excluding XTAL inputs
EXT. INPUT LOAD		4	5		Series 7400 unit loads
INPUT RESISTANCE					
Crystal Input, R_{XTAL}	1.1			KΩ	Resistance to ground for Pin 1 and Pin 18
POWER SUPPLY CURRENT I_{CC}		40	80	mA	
AC CHARACTERISTICS					T_A = +25°C
CLOCK FREQUENCY					See Note 2
PULSE WIDTH (T_{PW})					
Clock					50% Duty Cycle ± 10%. See Note 2
Receiver strobe	150		DC	ns	See Note 3
Transmitter strobe	150		DC	ns	See Note 3
INPUT SET-UP TIME (T_{SET-UP})					
Address	50			ns	See Note 3
OUTPUT HOLD TIME (T_{HOLD})					
Address	50			ns	
STROBE TO NEW FREQUENCY DELAY			6	CLK	

NOTE 1: XTAL/EXT inputs are either TTL compatible or crystal compatible. See crystal specification in Applications Information section.
All inputs except XTAL, STR and STT have internal pull-up resistors.

NOTE 2: Refer to frequency option tables for maximum input frequency on XTAL/EXT pins.
Typical clock pulse width is 1/2 x CL

NOTE 3: Input set-up time can be decreased to >0 ns by increasing the minimum strobe width (50 ns) to a total of 200 ns.
$T_{A\text{-}D}$ and $R_{A\text{-}D}$ have internal pull-up resistors.

OPERATION

Standard Frequencies

Choose a Transmitter and Receiver frequency from the table below. Program the corresponding address into TA-TD and RA-RD respectively using strobe pulses or by hard wiring the strobe and address inputs.

Non-Standard Frequencies

To accomplish non-standard frequencies do one of the following:

1. Choose a crystal that when divided by the WD1943 generates the desired frequency.
2. Cascade devices by using the frequency outputs as an input to the XTAL/EXT inputs of the subsequent WD1943.
3. Consult the factory for possible changes via ROM mask reprogramming.

FREQUENCY OPTIONS

TABLE 1. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6336
0	0	0	1	75	1.2	1.2	—	50/50	4224
0	0	1	0	110	1.76	1.76	—	50/50	2880
0	0	1	1	134.5	2.152	2.1523	0.016	50/50	2355
0	1	0	0	150	2.4	2.4	—	50/50	2112
0	1	0	1	300	4.8	4.8	—	50/50	1056
0	1	1	0	600	9.6	9.6	—	50/50	528
0	1	1	1	1200	19.2	19.2	—	50/50	264
1	0	0	0	1800	28.8	28.8	—	50/50	176
1	0	0	1	2000	32.0	32.081	0.253	50/50	158
1	0	1	0	2400	38.4	38.4	—	50/50	132
1	0	1	1	3600	57.6	57.6	—	50/50	88
1	1	0	0	4800	76.8	76.8	—	50/50	66
1	1	0	1	7200	115.2	115.2	—	50/50	44
1	1	1	0	9600	153.6	153.6	—	48/52	33
1	1	1	1	19,200	307.2	316.8	3.125	50/50	16

WD1943-00

TABLE 2. CRYSTAL FREQUENCY = 4.9152 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(16X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	0.8	0.8	—	50/50	6144
0	0	0	1	75	1.2	1.2	—	50/50	4096
0	0	1	0	110	1.76	1.7598	−0.01	*	2793
0	0	1	1	134.5	2.152	2.152	—	50/50	2284
0	1	0	0	150	2.4	2.4	—	50/50	2048
0	1	0	1	300	4.8	4.8	—	50/50	1024
0	1	1	0	600	9.6	9.6	—	50/50	512
0	1	1	1	1200	19.2	19.2	—	50/50	256
1	0	0	0	1800	28.8	28.7438	−0.19	*	171
1	0	0	1	2000	32.0	31.9168	−0.26	50/50	154
1	0	1	0	2400	38.4	38.4	—	50/50	128
1	0	1	1	3600	57.6	57.8258	0.39	*	85
1	1	0	0	4800	76.8	76.8	—	50/50	64
1	1	0	1	7200	115.2	114.306	−0.77	*	43
1	1	1	0	9600	153.6	153.6	—	50/50	32
1	1	1	1	19,200	307.2	307.2	—	50/50	16

WD1943-05

TABLE 3. CRYSTAL FREQUENCY = 5.0688 MHZ

Transmit/Receive Address				Baud Rate	Theoretical	Actual	Percent	Duty Cycle	
D	C	B	A	(32X Clock)	Freq. (kHz)	Freq. (kHz)	Error	%	Divisor
0	0	0	0	50	1.6	1.6	—	50/50	3168
0	0	0	1	75	2.4	2.4	—	50/50	2112
0	0	1	0	110	3.52	3.52	—	50/50	1440
0	0	1	1	134.5	4.304	4.303	.026	50/50	1178
0	1	0	0	150	4.8	4.8	—	50/50	1056
0	1	0	1	200	6.4	6.4	—	50/50	792
0	1	1	0	300	9.6	9.6	—	50/50	528
0	1	1	1	600	19.2	19.2	—	50/50	264
1	0	0	0	1200	38.4	38.4	—	50/50	132
1	0	0	1	1800	57.6	57.6	—	50/50	88
1	0	1	0	2400	76.8	76.8	—	50/50	66
1	0	1	1	3600	115.2	115.2	—	50/50	44
1	1	0	0	4800	153.6	153.6	—	*	33
1	1	0	1	7200	230.4	230.4	—	50/50	22
1	1	1	0	9600	307.2	298.16	2.941	*	17
1	1	1	1	19,200	614.4	633.6	3.125	50/50	8

*When the duty cycle is not exactly 50% it is 50% ± 10%

WD1943-06

APPLICATIONS INFORMATION

OPERATION WITH A CRYSTAL

The WD1943 Baud Rate Generator may be driven by either a crystal or TTL level clock. When using a crystal, the waveform that appears at pins 1 (STAL/EXT 1) and 18 (XTAL/EXT 2) does not conform to the normal TTL limits of $V_{IL} \leq 0.8V$ and $V_{IH} \geq 2.0V$. Figure 1 illustrates a typical crystal waveform when connected to a WD1943.

Since the D.C. level of the waveform causes the least positive point to typically be greater than 0.8V, the WD1943 is designed to look for an edge, as opposed to a TTL level. The XTAL/EXT logic triggers on a rising edge of typically 1V in magnitude. This allows the use of a crystal without any additional components.

OPERATIONS WITH TTL LEVEL CLOCK

With clock frequencies in the area of 5 MHz, significant overshoot and undershoot ("ringing") can appear at pins 1 and/or 18. The clock oscilator may, at times be triggered on a rising edge of an overshoot or undershoot waveform, causing the device to effectively "double-trigger." This phenomenon may result as a twice expected baud rate, or as an apparent device failure. Figure 2 shows a typical waveform that exhibits the "ringing" problem.

The design methods required to minimize ringing include the following:

1. Minimize the P.C. trace length. At 5 MHz, each inch of trace can add significantly to overshoot and undershoot.
2. Match impedances at both ends of the trace. For example, a series resistor near the device may be helpful.
3. A uniform impedance is important. This can be accomplished through the use of:
   a. parallel ground lines
   b. evenly spaced ground lines crossing the trace on the opposite side of PC board
   c. an inner plane of ground, e.g., as in a four layered PC board.

In the event that ringing exists on an already finished board, several techniques can be used to reduce it. These are:

1. Add a series resistor to match impedance as shown in Figure 3.
2. Add pull-up/pull-down resistor to match impedance, as shown in Figure 4.
3. Add a high speed diode to clamp undershoot, as shown in Figure 5.

The method that is easiest to implement in many systems is method 1, the series resistor. The series resistor will cause the D.C. level to shift up, but that does not cause a problem since the OSC is triggered by an edge, as opposed to a TTL level.

The 1943 Baud Rate Generator can save both board space and cost in a communications system. By choosing either a crystal or a TTL level clock, the user can minimize the logic required to provide baud rate clocks in a given design.

POWER LINE SPIKES

Voltage transients on the AC power line may appear on the DC power output. If this possibility exists, it is suggested that a by-pass capacitor is used between +5V and GND.

CRYSTAL SPECIFICATIONS

User must specify termination (pin, wire, other)
Frequency — See Tables 1-6.
Type: Microprocessor Crystal
Temperature range 0°C to +70°C
Series resistance 50Ω to 100Ω
Series resonant to 100Ω
Overall tolerance ±0.01%

CRYSTAL MANUFACTURERS (Partial List)

American Time Products Div.
Frequency Control Products, Inc.
Woodside, New York 11377

Bliley Electric Co.
Erie, Pennsylvania 16508

M-tron Ind. Inc.
Yankton, South Dakota 57078

Erie Frequency Control
Calisle, Pennsylvania 17013

Q-Matic Corporation
Costa Mesa, California 92626

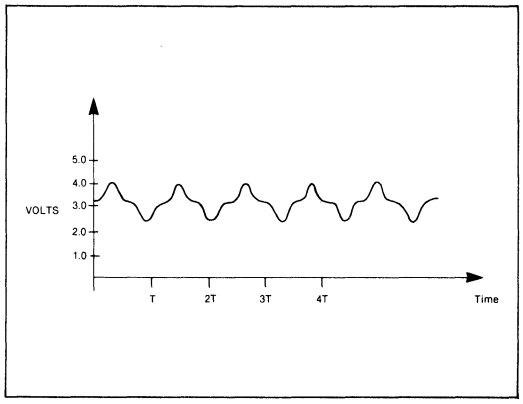


FIGURE 1. TYPICAL CRYSTAL WAVEFORM

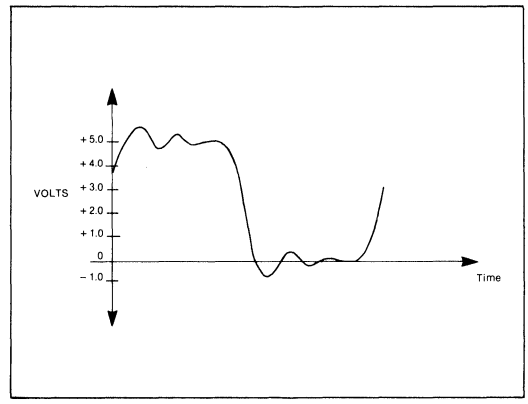


FIGURE 2. TYPICAL "RINGING" WAVEFORM from TTL INPUT

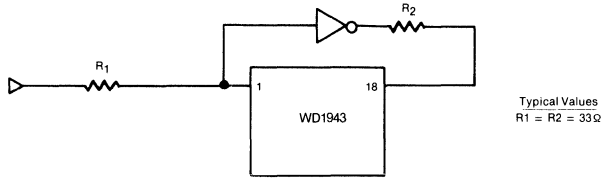


FIGURE 3. SERIES RESISTOR TO MATCH IMPEDANCE

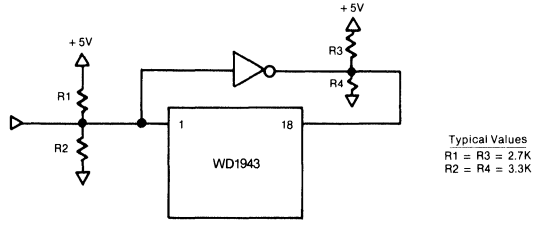


FIGURE 4. PULL-UP/PULL-DOWN RESISTORS TO MATCH IMPEDANCE

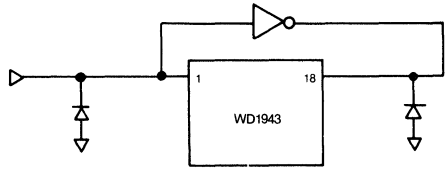
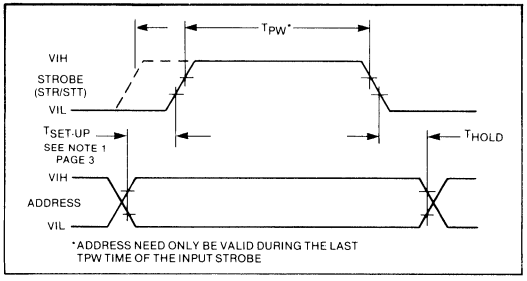
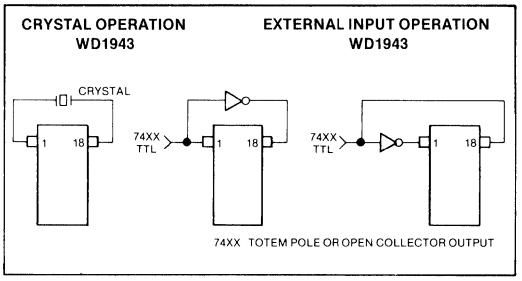


FIGURE 5. HIGH-SPEED DIODE TO CLAMP UNDERSHOOT



CONTROL TIMING



CRYSTAL/CLOCK OPTIONS

ABSOLUTE MAXIMUM RATINGS

Positive Voltage on any Pin, with respect to ground	+7.0V
Negative Voltage on any Pin, with respect to ground	−0.3V
Storage Temperature	(plastic package) −55°C to +125°C (Cerdip package and Ceramic package) −65°C to +150°C
Lead Temperature (Soldering, 10 sec.)	+325°C

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and Functional Operation of the device at these or at any other condition above those indicated in the operational sections of this specification are not implied.

See page 383 for ordering information.

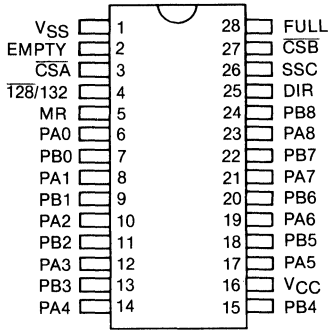
Printed in U.S.A.

FINAL

WD1510—00, -01, -02, -03 LIFO/FIFO Buffer Register

FEATURES

- WORD LENGTH SELECTABLE: 128 OR 132
- 9 BIT WORD WIDTH
- DC TO 650 KHZ (–00), 1 MHz (–01), 1.5 MHz (–02), 1.8 MHz (–03)
- EMPTY AND FULL FLAGS
- THREE-STATE DATA LINES
- 5-VOLT ONLY
- NO EXTERNAL CLOCKS REQUIRED
- TTL COMPATIBLE ON ALL INPUTS AND OUTPUTS
- 28 PIN PLASTIC OR CERAMIC DIP
- CASCADABLE WITH WD1511 SUPPORT CHIP
- FULLY ASYNCHRONOUS DUAL PORT OPERATION



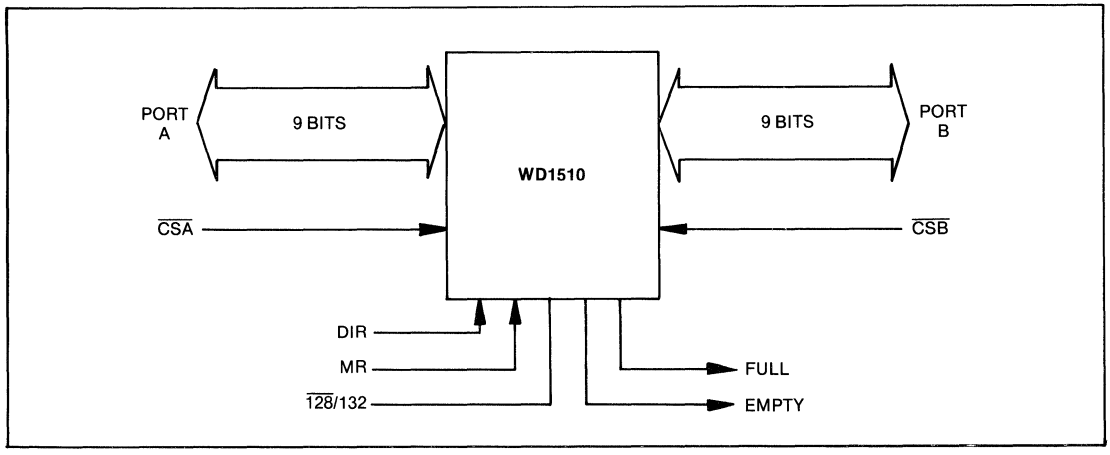
PIN DESIGNATION

DESCRIPTION

The WD1510 is an MOS/LSI Memory Buffer which is organized as a 9-bit by 128 or 132 word stack. The chip has 2 bidirectional data ports and may be read from or written into either port. Thus, the chip can function as a LIFO from either port or it can function as a FIFO, with data flow from either port A to port B or vice versa. The DIRECTION input pin is used to specify the data flow direction. The WD1510 is fabricated in 5-volt only N-channel technology.

PIN DESCRIPTION

PIN NUMBER	NAME	SYMBOL	FUNCTION
1	VSS	VSS	Ground
2	EMPTY	EMPTY	Indicates when there is no data in the buffer
3	CHIP SELECT PORT A	$\overline{CSA}$	Used to select Port A for either a Read or Write operation
4	128 OR 132	$\overline{128}$/132	Used to set word length. When low word length = 128, when high word length = 132
5	MASTER RESET	MR	When pulsed will clear the buffer and set the EMPTY pin
6,8,10,12,14, 17,19,21,23	PORT A DATA LINES	PA0-PA8	Bidirectional DATA Port for reading or writing
7,9,11,13,15 18,20,22,24	PORT B DATA LINES	PB0-PB8	Bidirectional DATA Port for reading or writing
16	V_{CC}	V_{CC}	+5 volts ± .25V
25	DIRECTION	DIR	When low DIR specifies that Port A may be read from and Port B may be written into. When high DIR specifies that Port A may be written into and Port B may be read from.
26	NO CONNECTION	NC	No connection (not for customer use).
27	CHIP SELECT PORT B	$\overline{CSB}$	Used to select Port B for either a Read or Write Operation
28	FULL	FULL	Indicates that all 132 or 128 words of memory are loaded with data



OPERATION

The WD1510 contains a 132 x 9 buffer which may be programmed for 128 x 9 operation. Setting the $\overline{128}$/132 pin to a Logic 0 enables the EMPTY and FULL lines to be activated when 128 bytes are read or written. When the $\overline{128}$/132 line is set to a Logic 1 or left open, the 132 byte operation is enabled. This line contains an internal pull-up resistor of approximately 5KΩ.

When the Master Reset Line (pin 5) is set to a Logic 1, all internal counters are reset and the EMPTY Flag is set. Prior to reading or writing data, the DIRECTION Line (pin 25) must be set to select the desired operation:

DIR	PORT A	PORT B
1	WRITE	READ
0	READ	WRITE

To operate the device in the FIFO mode, both Ports must be used. If the DIRECTION Line is set to a Logic 1, then data is written into Port A and read out of Port B. Reading/Writing to the two ports can be done asynchronously.

In the LIFO mode only one port is used. For example, if using Port A, the DIRECTION Line is set to a Logic 1 to enter data, and is reset to a Logic 0 to read data.

Reading or writing is performed by setting the appropriate $\overline{CS}$ (Chip Select) Line to a Logic 0. After the specified hold time has expired, data may be entered or read on the rising edge of $\overline{CSA}$ or $\overline{CSB}$. In a Read mode, data is valid as long as $\overline{CS}$ remains active. Both Ports return to the high impedance state when $\overline{CS}$ is returned to a Logic 1.

The EMPTY Line (Pin 2) and the FULL Line (Pin 28) are used as status or interrupt lines to determine the status of the buffer. When both EMPTY and FULL are at a Logic 0, the buffer contains 1 thru 127 bytes ($\overline{128}$/132 = 0) or 1 thru 131 bytes ($\overline{128}$/132 = 1).

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (Ground) ..... +7V
Max Voltage on any Pin with respect to V_{SS} ..... −0.5V to +7V
Operating Temperature ..... 0°C to 70°C
Storage Temperature
Plastic ..... −55°C to +125°C
Ceramic ..... −65°C to +150°C

OPERATING CHARACTERISTICS (DC)

TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V

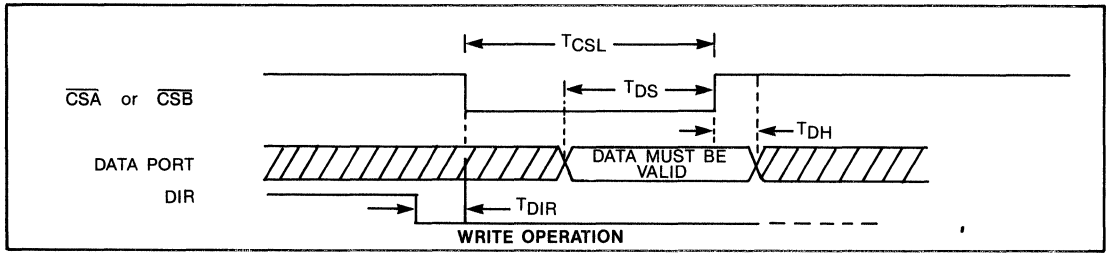
SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
I_{LI}	Input Leakage			10	μA	$V_{IN} = V_{CC}$
I_{LO}	Output Leakage			10	μA	$V_{OUT} = V_{CC}, V_{SS}$
V_{IH}	Input High Voltage	2.2			V	
V_{IL}	Input Low Voltage			0.8	V	
V_{OH}	Output High Voltage	2.4			V	$I_O = -100\mu A$
V_{OL}	Output Low Voltage			.4	V	I_O = 1.6 mA
I_{CC}	Power Supply Current		125	200	mA	All outputs open

A.C. TIMING CHARACTERISTICS

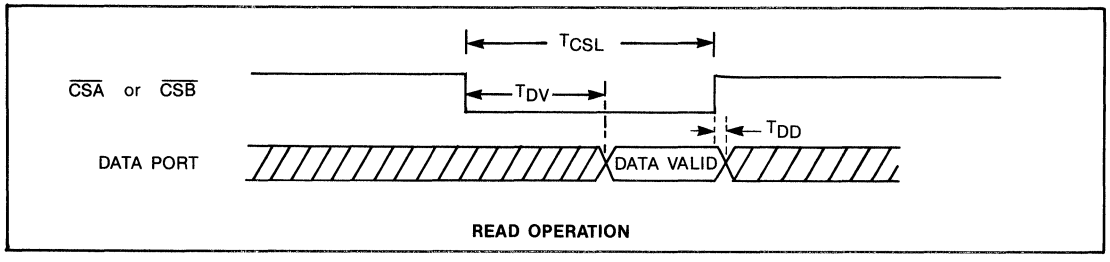
TA = 0°C to 70°C, V_{SS} = 0V, V_{CC} = +5V ± .25V, V_{OH} = 2.0V, V_{OL} = 0.8V

		WD1510-00*		WD1510-01*		WD1510-02*		WD1510-3*	
SYMBOL	CHARACTERISTICS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
T_{MR}	Master Reset Time	400		250		225		200	
T_{DV}	Data Valid from CS		550		350		233		200
T_{DD}	Data Delay from CS		110		85		70		60
T_{DH}	Data Hold from CS	150		100		80		80	
T_{DIR}	DIR Setup Time	1500		1000		667		556	
T_{EV}	EMPTY Valid from CS		550		350		234		200
T_{FV}	FULL Valid from CS		550		350		234		200
T_{CSL}	CS Pulse Width Low	600		500		334		278	
T_{CSH}	CS Pulse Width High	600		500		334		278	
T_{CY}	CS Cycle Time	1540		1000		667		556	
T_{DS}	Data Setup Time	80		50		50		33	
F_{MAX}	Data Transfer Rate		.65		1.0		1.5		1.8

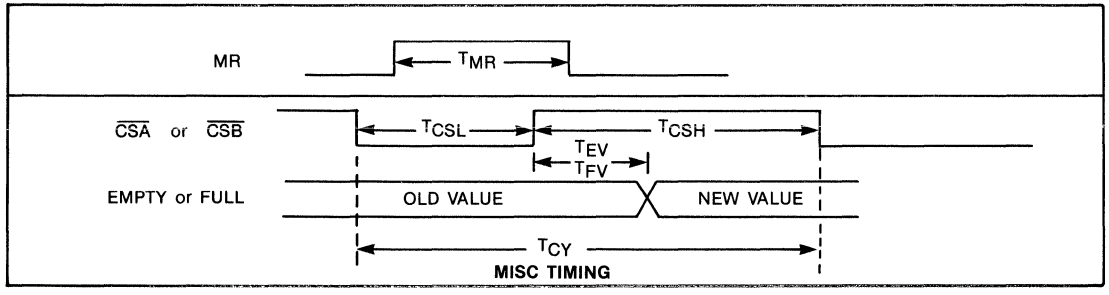
*All values are in nanoseconds with the exception of F_{MAX} = MHz.
**Not available.



WRITE OPERATION



READ OPERATION



MISC TIMING

CAPACITANCE

T_A = 25°C; V_{CC} = GND = 0V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT	TEST CONDITIONS
C_{IN}	Input Capacitance		6	10	pF	f_C = 1 MHz
$C_{I/O}$	I/O Capacitance		15	20	pF	Unmeasured pins returned to GND.
C_L	Load Capacitance		50		pF	V_{CC} = 5.0 V

WD1510 CAPACITANCE LEVELS

See page 383 for ordering information.

Printed in U.S.A.

WD9914 General Purpose Interface Bus (GPIB) Controller

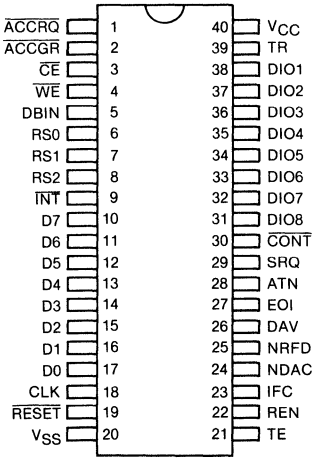
FINAL

FEATURES

- HANDLES ALL IEEE-488 1975/78 FUNCTIONS
- COMPATIBLE WITH IEEE-488A 1980 SUPPLEMENT
- TALKER AND LISTENER FUNCTION (T, TE, L, LE)
- AUTOMATIC SOURCE AND ACCEPTOR HANDSHAKES (SH, AH)
- CONTROLLER WITH PASS CONTROL
- SYSTEM CONTROLLER CAPABILITIES
- DEVICE TRIGGER AND DEVICE CLEAR CAPABILITIES (DT, DC)
- OPTIONAL AUTOMATICALLY CLEARED 'REQUEST SERVICE BIT'
- PARALLEL AND SERIAL POLL FACILITIES (PP)
- REMOTE/LOCAL FUNCTION WITH LOCAL LOCKOUT (RL)
- SINGLE OR DUAL PRIMARY ADDRESSING
- SECONDARY ADDRESS CAPABILITIES
- DIRECT INTERFACE TO SN75160/161/162 BUS TRANSCEIVERS WITH NO ADDITIONAL LOGIC
- COMPATIBLE WITH MOST MICROPROCESSORS
- DIRECT MEMORY ACCESS FACILITIES
- MEMORY-MAPPED MICROPROCESSOR INTERFACE
- SINGLE +5V SUPPLY
- COMPATIBLE WITH TMS9914A FEATURES

DESCRIPTION

The WD9914 provides an interface between a Microprocessor System and the General Purpose Interface Bus (GPIB) specified in the IEEE-488 1975/78 standards and the IEEE-488A 1980 supplement. The device is controlled and configured through 8-bit memory mapped registers and enables all aspects of the standards to be implemented, including talker, listener and controller.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	I/O (TYPE)	DESCRIPTION
1	$\overline{\text{ACCRQ}}$	O(p/p)	ACCESS REQUEST: this pin becomes active (low) to request a direct memory access.
2	$\overline{\text{ACCGR}}$	I	ACCESS GRANTED: when received from the direct memory access control logic this enables the byte onto the data bus. ACCGR must be high when not participating in DMA transfer.
3	$\overline{\text{CE}}$	I	CHIP ENABLE: $\overline{\text{CE}}$ low allows access of read and write registers. If $\overline{\text{CE}}$ is high, D0-D7 are in high impedance unless $\overline{\text{ACCGR}}$ is low.
4	$\overline{\text{WE}}$	I	WRITE ENABLE: when active (low), indicates to the WD9914 that data is being written to one of its registers.
5	DBIN	I	DATA BUS IN: an active (high) state indicates to the WD9914 that a read is about to be carried out by the MPU.
6 7 8	RS0 RS1 RS2	I I I	REGISTER SELECT LINES: determine which register is addressed by the MPU during a read or write operation.
9	$\overline{\text{INT}}$	O(o/d) (no pullup)	INTERRUPT: sent to the MPU to cause a branch to a service routine.
10-17	D7-D0	I/O(p/p)	Data transfer lines on the MPU side of the device.
18	CLK	I	CLOCK Input: 500 kHz to 5 MHz. Need not be synchronous to system clock.
19	$\overline{\text{RESET}}$*	I	INITIALIZES the WD9914 at power-on.
20	V_{SS}		Ground reference voltage.
21	TE	O(p/p)	TALK ENABLE: controls the direction of the transfer of the line transceivers. Logically, it is: (CACS + TACS + EIO.ATN.(CIDS + CADS). $\overline{\text{SWRST}}$).
22	REN	I/O(o/d)	REMOTE ENABLE: sent by system controller to select control either from the front panel or from the IEEE bus.
23	IFC	I/O(o/d)	INTERFACE CLEAR: sent by the system controller to set the interface system into a known quiescent state. The system controller becomes the controller in charge.
24	NDAC	I/O(p/p)	NOT DATA ACCEPTED: handshake line. Acceptor sets this false (high) when it has latched the data from the I/O lines.
25	NRFD	I/O(p/p)	NOT READY FOR DATA: handshake line. Sent by acceptor to indicate readiness for the next byte.
26	DAV	I/O(p/p)	DATA VALID: handshake line controlled by source to show acceptors when valid data is present to the bus.
27	EOI	I/O(p/p)	END OR IDENTIFY: if ATN is false (high), this indicates the end of a message block. If ATN is true (low), the controller is requesting a parallel poll.

PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	I/O (TYPE)	DESCRIPTION
28	ATN	I/O(p/p)	ATTENTION: sent by controller in charge. When true (low), interface commands are being sent over the DIO lines. When false (high), these lines carry data.
29	SRQ	I/O(p/p)	SERVICE REQUEST: set true (low) by a device to indicate a need for service.
30	$\overline{\text{CONT}}$	O(p/p)	Indicates if a device is controller in charge. It is used to control direction of SRQ and ATN in pass control systems. Logically, it is (CIDS + CADS).
31	DIO8	I/O(p/p)	DIO8 through DIO1 are the data input/output lines on the GPIB side. These pins connect to the IEEE-488 bus via non-inverting transceivers.
32	DIO7	I/O(p/p)	
33	DIO6	I/O(p/p)	
34	DIO5	I/O(p/p)	
35	DIO4	I/O(p/p)	
36	DIO3	I/O(p/p)	
37	DIO2	I/O(p/p)	
38	DIO1	I/O(p/p)	
39	TR	O(p/p)	TRIGGER: activated when the GET command is received over the interface or the fget command is given by the MPU.
40	V_{CC}		Supply voltage (+5 V nominal).

(p/p) = push/pull output.
(o/d) = open drain output with internal pull up.
*The hardware RESET pin has the following effect on the WD9914:
— Serial and Parallel Poll registers cleared
— All clear/set auxiliary commands cleared except 'swrst'
— 'swrst' auxiliary command set. This holds the WD9914 in known states.

ARCHITECTURE

The block diagram of the internal architecture of the WD9914 is given in Figure 1. As previously stated, there are 13 MPU accessible registers of which 6 are read and 7 are write. These registers handle all communication between the IEEE-488 1975/78 bus and microprocessor.

Each register is accessed by putting the relevant address on lines RS0, RS1 and RS2 and performing a memory read ($\overline{WE}$ = 1 DBIN = 1) or memory write ($\overline{WE}$ = 0 DBIN = 0) operation. The register addresses and use of each bit is shown in Table 1 for the read registers and Table 2 for the write registers. A full description of each register is given in the following paragraphs.

Implementation of the functions described by the state diagrams of the IEEE-488 standard is carried out in the IEEE-488 state diagram block. Information is received from the IEEE bus and from the internal registers and is combined with the current status of the device (for example, Talker Active State, TACS) to produce the control signals to load registers or handle the handshake or bus management lines.

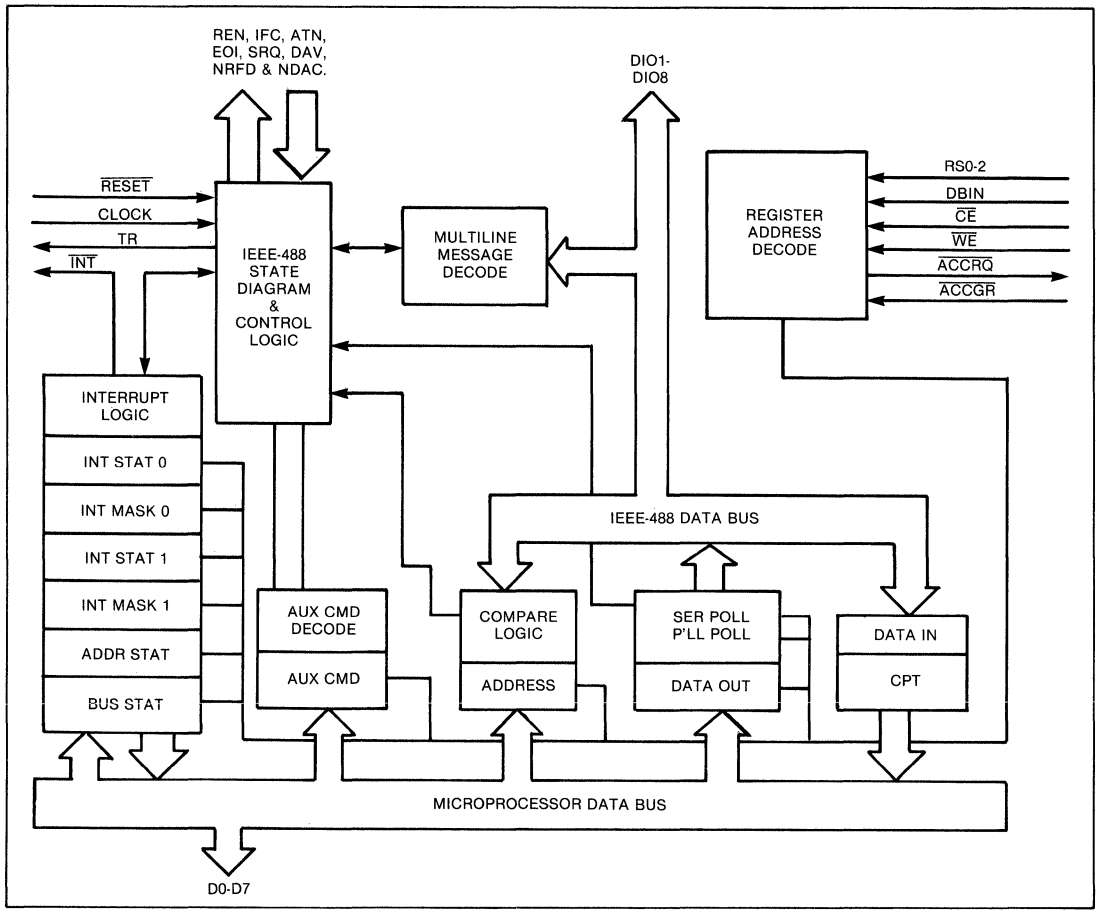


Figure 1. SIMPLIFIED BLOCK DIAGRAM

Table 1. WD9914 READ REGISTERS

ADDRESS RS2	RS1	RS0	REGISTER NAME	BIT ASSIGNMENT D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Status 0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC
0	0	1	Int Status 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	Address Status	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
0	1	1	Bus Status	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
1	0	0	*								
1	0	1	*								
1	1	0	Cmd Pass Thru	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
1	1	1	Data In	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

*The WD9914 host interface data lines will remain in the high impedance state when these register locations are addressed. An Address Switch Register may therefore be included in the address space of the device at these locations.

Table 2. WD9914 WRITE REGISTERS

ADDRESS RS2	RS1	RS0	REGISTER NAME	BIT ASSIGNMENT D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Int Mask 0			BI	BO	END	SPAS	RLC	MAC
0	0	1	Int Mask 1	GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC
0	1	0	*	xx	xx	xx	xx	xx	xx	xx	xx
0	1	1	Auxiliary Cmd	cs	xx	xx	f4	f3	f2	f1	f0
1	0	0	Address	edpa	dal	dat	A5	A4	A3	A2	A1
1	0	1	Serial Poll	S8	rsvl	S6	S5	S4	S3	S2	S1
1	1	0	Parallel Poll	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
1	1	1	Data Out	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

*This address is not decoded by the WD9914. A write to this location will have no effect on the device, as if a write had not occurred.

REGISTERS

Interrupt Mask and Status Registers 0

The Interrupt Mask and Interrupt Status registers operate independently of each other. The status bits will always be set when the appropriate events occur regardless of the state of the corresponding mask bit.

All interrupt bits, with the exception of INT0 and INT1 which are not storage bits, are edge triggered and are set when the appropriate condition becomes true. The storage bits are cleared immediately after the corresponding Interrupt Status Register is read by the host MPU. If an interrupt condition becomes true during this read operation, then the event is stored. The corresponding bit is set when the read operation ends, hence no interrupts are lost. In addition to being cleared by a read operation, the BO interrupt is also cleared by writing to the Data Out Register, and the BI interrupt is cleared by reading the Data In Register.

The interrupt status bits are cleared and held in the O condition while Software Reset (swrst) is set.

The corresponding bit of the Interrupt mask register must be set to a 1 if an interrupt status bit is to cause an external interrupt ($\overline{INT}$ Low) when it is set (i.e., $\overline{INT}$ = INT STATUS.INT MASK). The mask register is not cleared by 'swrst' or the Hardware Reset pin ($\overline{RESET}$) and will power on in a random state. It must, therefore, be written to by the host MPU before 'swrst' is cleared to avoid extraneous interrupts.

The INT0 and INT1 bits of the Interrupt Status Register are not true status bits. INT1 will be true if there are any unmasked interrupt status bits set to a 1 in Interrupt Status Register 1. INT0 will be true if any of bits 2-7 of Interrupt Status Register 0 are unmasked and set to a 1. If either INT1 or INT0 is true, then the external interrupt pin ($\overline{INT}$) will be pulled low provided that the Disable All Interrupts feature (dai) has not been set.

The individual bits of Interrupt Status and Interrupt mask Register 0 are described are in the following paragraphs. The conditions which set these bits, shown in parentheses, are given in terms of the state diagrams. Each bit is set on the rising edge of the condition shown.

INTERRUPT MASK/STATUS REGISTER 0

xx	xx	BI	BO	END	SPAS	RLC	MAC	INT	MASK 0
INT0	INT1	BI	BO	END	SPAS	RLC	MAC	INT	STATUS 0
D0	D1	D2	D3	D4	D5	D6	D7		MPU BUS

NOTE: A 0 masks and a 1 unmasks the bits in the interrupt mask registers.

INT1 — This will be a 1 when an unmasked status bit in Interrupt Status Register 1 is set to a 1.

INT0 — This will be a 1 when any of bits 2-7 of Interrupt Status Register 0 is unmasked and set to a 1.

BI — Byte In. A data byte has been received in the Data In register. If the mask bit is not set, then no interrupt is generated but a RFD holdoff will still occur before the next data byte is accepted. If the Shadow Handshake feature is used, then this status bit will not be set. This bit is cleared by reading the Data In Register as well as after Interrupt Status Register 0 has been read. (Set On: ACDS1.LACS)

BO Byte Out. This is set when the Data Out Register is available to send a byte over the GPIB. This byte may be either a command if the device is a controller or data if the device is a talker. It is set when the device becomes an active talker or controller but will not occur if the Data Out register has been loaded with a byte which has not been sent. Subsequently, it will occur after each byte has been sent and the WD9914 returns to SGNS. This bit is cleared by writing to the Data Out Register as well as by reading Interrupt Status Register 0. (Set On: SGNS.CACS + SGNS.TACS.SHFS)

NOTE:
When a controller addresses itself as a talker and then goes to standby, there will be a momentary transition of the source handshake into SIDS before TACS becomes true and it reenters SGNS. Under these circumstances, the WD9914 is guaranteed to give a BO interrupt on reentering 'SGNS'.

END This indicates that a byte just received by a listener was the last byte in a string, that is, it was received with the EOI line true. It is set at the same time as the BI interrupt. (Set On: (ACDS1.LACS.EOI)

SPAS This indicates that the WD9914 has requested service via rsv1 or rsv2 (in the Serial Poll Register or Auxiliary Command Register) and has been polled in a serial poll. It is set on the false transition of STRS when the serial poll status byte is sent. (Set On: STRS.SPAS.(APRS1 + APRS2)

RLC Remote/Local Change. This is set by any transition between local and remote states in the Remote/Local function. (Set On: (LOCS-REMS) + (REMS-LOCS) + (LWLS-RWLS) + (RWLS-LWLS)

MAC My Address Change. This indicates that a command has been received from the GPIB which has resulted in the addressed state of the WD9914 to change. It will not occur if secondary addressing is being used, nor indicate that the WD9914 has been readdressed on its other primary address. (Set On: ACDS1. (MTA.TADSUNT + OTA.$\overline{\text{TADS}}$ + MLA.LADS + UN.$\overline{\text{LADS}}$)

Interrupt Mask and Status Registers 1

The operation of Interrupt Mask and Status Register 1 is similar to that of Interrupt Mask and Status Register 0 except that all bits are true storage bits. The status bits are cleared only following the register being read and by 'swrst'.

There is one distinct group of interrupts in this register: GET, UNC, APT, DCAS, MA. These are all set in response to commands received over the bus and if unmasked, a Data Accepted (DAC) holdoff will occur when the interrupt in question is set, It may be released with a 'dacr' auxiliary command. This is further discussed in the Acceptor Handshake discussions.

The mask bit of the APT Interrupt is further used in the talker and listener functions. When the interrupt is unmasked, the talker and listener functions of the WD9914 implement the extended talker and extended listener functions of IEEE-488. Otherwise these functions implement the talker and listener functions of IEEE-488.

The individual bits of Interrupt Status and Interrupt Mask Register 1 are described below. The conditions which set these bits, shown in parentheses, are given in terms of the state diagrams.

INTERRUPT MASK/STATUS REGISTER 1

GET	ERR	UNC	APT	CDAS	MA	SRQ	IFC	INT	MASK 1
GET	ERR	UNC	APT	DCAS	MA	SRQ	IFC	INT	STATUS 1
D0	D1	D2	D3	D4	D5	D6	D7	MPU	BUS

GET This is set if a Group Execute Trigger command is received. A DAC holdoff occurs if the interrupt is unmasked. The TR pin becomes high when this command is received and persists high for the duration of a DAC holdoff if one occurs. If the interrupt is masked, the TR pin becomes high for approximately five clock cycles. (Set On: GET.LADS.ACDS1)

ERR Error. This is set if the source handshake becomes active and finds that the NDAC and NRFD lines are both high. This indicates that, for whatever reason, there are no acceptors on the bus. (Set On: SERS)

UNC Unrecognized Command. This is set if a command has been received which has no meaning to the WD9914. Unrecognized addressed commands will only cause this interrupt if the device is LADS except for TCT which will only interrupt in TADS. Secondary commands will only cause this interrupt if the 'pts' auxiliary command has been set previously. A DAC holdoff will occur if this interrupt is unmasked which effectively enables the command pass through feature. Unrecognized commands may be inspected in the Command Pass Through Register before this holdoff is released. (Set On: ACDS1. (UCG.$\overline{\text{LLO}}$. $\overline{\text{SPE}}$.

$\overline{SPD.DCL}$ + ACG.$\overline{GET.GTL.SCD.TCT.}$ LADS + TCT.TADS + SCG.pts)

APT — Address Pass Through. Unmasking this interrupt enables secondary addressing. It is set if a secondary command is received provided that the last primary command received was a primary talk or listen address of the WD9914. A DAC holdoff will occur and the secondary address may be read from the Command Pass Through Register. The holdoff may be released by a 'dacr' auxiliary command and the 'cs' bit of the Auxiliary Command Register is used to indicate that a valid (cs = 1) or an invalid (cs = 0) secondary has been identified by the host MPU. (Set On: ACDS1. SCG.(LPAS + TPAS)

DCAS — Device Clear Active State. This is set when a device clear command (DCL) is received or when a selected device clear (SDC) is received with the WD9914 in LADS. This will cause a DAC holdoff if unmasked. (Set On: ACDS1.(DCL + SDC.LADS)

SRQ — Service Request. This is provided for the benefit of the controller which should execute a serial poll in response to this interrupt. It is set when the SRQ line becomes true. (Set On: SRQ.($\overline{CIDS}$ + $\overline{CADS}$)

MA — My Address. This is set when the WD9914 recognizes its primary talk or listen address. A DAC holdoff will occur if this is unmasked. (Set On: (MLA + MTA).$\overline{SPMS.}$ $\overline{aptmk}$)

IFC — Interface Clear. This is provided for the benefit of devices which are not the System Controller. It is set when the IFC line becomes true and indicates that the WD9914 has been returned to an idle state. If the device is the System Controller, then the IFC interrupt is not set. (Set On: IFCIN)

Address Status Register

REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
D0	D1	D2	D3	D4	D5	D6	D7

MPU BUS

REM — The device is in the remote state
LLO — Local lockout is in operation
ATN — The attention line is low (true) on the bus
LPAS — WD9914 is in the listener primary addressed state
TPAS — WD9914 is the talker primary addressed state
LADS (or LACS) — The device is addressed to listen
TADS (or TACS) — The device is addressed to talk
ulpa — This bit shows the LSB of the last address recognized by the WD9914.

Address Register

edpa	dal	dat	A5	A4	A3	A2	A1
D0	D1	D2	D3	D4	D5	D6	D7

edpa — Enable dual primary addressing mode
dal — Disable listener function
dat — Disable talker function
A5-A1 — Primary address of the WD9914.

Bits A5-A1 of this register contain the primary address of the device (denoted AAAAA in Table 19). IEEE-488 1975/78 does not allow a device to be assigned the value 11111 for bits A5-A1. When 'swrst' is true at power-up or if set by the host MPU, the WD9914 is held in an idle state. During this time the host MPU may load the primary address of the device into these bits. Often this will be read from an Address Switch Register.

The 'edpa' bit is used to enable the dual addressing mode of the WD9914. It causes the LSB of the address to be ignored by the address comparator giving two consecutive primary addresses for the device. The address by which the WD9914 was selected is indicated by the 'ulpa' bit of the Address Status Register.

The Address Register is not cleared by 'swrst' or hardware reset.

Auxiliary Command Register

cs	xx	xx	F4	F3	F2	F1	F0
D0	D1	D2	D3	D4	D5	D6	D7

f4-f0 — Auxiliary command select (see Table 3)
cs — Clear or set the feature (where applicable)

Auxiliary commands are used to enable and disable most of the selectable features of the WD9914 and to initiate many of the actions of the device. The desired feature is selected by writing a byte to this register with the appropriate value in bits f4-f0. These values are given in Table 3.

The 'cs' bit is used in most cases when the feature selected by f4-f0 is of the clear/set type. The feature is enabled if 'cs' = '1' and disabled if 'cs' = '0'. The holdoff on all data (hdfa) feature is an example of such a feature. Other auxiliary commands initiate an action of the WD9914, such as release RFD holdoff (rhdf). In most cases, the 'cs' bit is unused and ignored by these commands.

All the clear/set auxiliary commands are cleared by the hardware RESET pin except 'swrst,' which is set true by RESET.

The force group execute trigger (fget) and return to local (rtl) auxiliary commands have a clear/set mode of operation and a pulsed mode of operation. They behave as normal clear/set features, but if they are written with 'cs' = '0' when they have not been previously set, then they will pulse true. Using the 'fget' command in this manner will produce a pulse of approximately 1 μs at the TR pin (with a 5 MHz clock). The 'rtl' command used in this way will cause a return to one of the local states (assuming local lockout is not in force) but the WD9914 may reenter the remote state next time the listen address occurs.

Table 3. AUXILIARY COMMANDS

c/s	f4	f3	f2	f1	f0	MNEMONIC	FEATURES
0/1	0	0	0	0	0	swrst	Software reset
0/1	0	0	0	0	1	dacr	Release DAC holdoff
na	0	0	0	1	0	rhdf	Release RFD holdoff
0/1	0	0	0	1	1	hdfa	Holdoff on all data
0/1	0	0	1	0	0	hdfe	Holdoff on EOI only
na	0	0	1	0	1	nbaf	New byte available false
0/1	0	0	1	1	0	fget	Force group execute trigger
0/1	0	0	1	1	1	rti	Return to local
na	0	1	0	0	0	feoi	Send EOI with next byte
0/1	0	1	0	0	1	lon	Listen only
0/1	0	1	0	1	0	ton	Talk only
na	0	1	0	1	1	gts	Go to standby
na	0	1	1	0	0	tca	Take control asynchronously
na	0	1	1	0	1	tcs	Take control synchronously
0/1	0	1	1	1	0	rpp	Request parallel poll
0/1	0	1	1	1	1	sic	Send interface clear
0/1	1	0	0	0	0	sre	Send remote enable
na	1	0	0	0	1	rqc	Request control
na	1	0	0	1	0	rlc	Release control
0/1	1	0	0	1	1	dai	Diable all interrupts
na	1	0	1	0	0	pts	Pass through next secondary
0/1	1	0	1	0	1	stdl	Short TI settling time
0/1	1	0	1	1	0	shdw	Shadow handshake
0/1	1	0	1	1	1	vstdl	Very short T1 delay
0/1	1	1	0	0	0	rsv2	Request Service Bit 2

DESCRIPTION OF AUXILIARY COMMANDS

Software Reset (swrst) 0/1xx00000

Setting this command causes the WD9914 to be returned to a known idle state during which it will not take part in any activity on the GPIB. This auxiliary command is set by the power-on RESET and the chip should be configured while 'swrst' is set. Configuration should include writing the address of the device into the Address Register, writing mask values into the Interrupt Mask Registers and selecting the desired features in the Auxiliary Command Register and Address Register. After this, 'swrst' may be cleared at which point the device becomes logicaly existent on the GPIB. The Serial Poll Register and Parallel Poll Registers may also be written in this period but this

is not necessary if there is no status to report as both of these are cleared by the power-on RESET pin. Table 4 lists the various states and other conditions forced by 'swrst'.

Table 4. SOFTWARE RESET CONDITIONS

MNEMONIC	DESCRIPTION
SIDS	Source idle state
AIDS	Acceptor idle state
TIDS	Talker idle state
TPAS	Talker primary idle state
LIDS	Listener idle state
LPAS	Listener primary state
NPRS	Negative poll response state
LOCS	Local state
CIDS	Controller idle state
SPIS	Serial poll idle state
PPSS	Parallel poll standby state
ADHS	DAC holdoff state
AEHS	RFD holdoff on end state
SHFS	Source holdoff state
ENIS	END idle state

NOTES: 1. See State Diagram Implementation for definition of above.
2. All interrupt status bits are held in a 0 state, but interrupt mask bits are not affected.

Release DAC Holdoff (dacr)0/1xx00001

The Data Accepted (DAC) holdoff allows time for the host microprocessor to respond to unrecognized commands, secondary addresses, and device trigger or device clear commands. The holdoff is released by the MPU when the required action has been taken. Normally the command is loaded with the clear/set bit at zero; however, when used with the address pass through feature CS is set to one if the secondary address was valid or to zero if invalid see APT interrupt.

Release RFD Holdoff (rhdf)naxx00010

Any Ready For Data (RFD) holdoff caused by a 'hdfa' or 'hdfe' is released.

Holdoff on All Data (hdfa)0/1xx00011

A Ready For Data (RFD) holdoff is caused on every data byte until the command is loaded with CS set to zero. The handshake must be completed after each byte has been received by the MPU using the 'rhdf' command.

Holdoff on End (hdfe)0/1xx00100

A RFD holdoff will occur when an end of data string message (EOI tru with ATN false) is received over the interface. This holdoff must be released using 'rhdf'.

Set New Byte Available False (nbaf)naxx00101

If a talker is interrupted before the byte just stored in the data out register is sent over the interface, this byte will normally be transmitted as soon as the ATN line returns to the false state. If, as a result of the interrupt, this byte is no longer required, its transmission may be suppressed using the 'nbaf' command.

Force Group Execute Trigger (fget)0/1xx00110

The state of the TR output from the WD9914 is affected when this command is executed. If the CS bit is zero, the line is pulsed high for approximately 5 clock cycles (1 μs at 5 MHz). If CS is one, the TR line goes high until 'fget' is sent with CS equal to zero. No interrupts or handshakes are initiated.

Return to Local (rtl)0/1xx00111

Provided the local lockout (LLO) has not been enabled, the remote/local status bit is reset, and an interrupt is generated (if enabled to inform the host microprocessor that it should respond to the front panel controls. If the CS bit is set to one the 'rtl' command must be cleared (CS = 0) before the device is able to return to remote control. If CS is set to zero, the device may return to remote without first clearing 'rtl'.

Force End or Identify (feoi)naxx01000

This command causes the EOI message to be sent with the next data byte. The EOI line is then reset.

Listen Only (lon)0/1xx01001

The listener state is activated until the command is sent with CS set to 0 or until deactivated by a bus command.

Talk Only (ton)0/1xx01010

The talker state is activated until the command is sent with CS set to 0 or until deactivated by a bus command.

NOTE:
'ton' and 'lon' are included for use in systems without a controller. However, where the WD9914 is being used as a controller, it utilizes the 'lon' and 'ton' functions to set itself up as a listener or talker, respectively. Care must therefore be taken to ensure these functions are reset if sending UNL or OTA.

Go to Standby (gts)naxx01011

Issued by the controller in charge to set the ATN line false.

Take Control Synchronously (tcs)naxx01101

Control is again taken by the controller in charge, and ATN is asserted. If the controller is not a true listener, the shadow handshake command must be used to monitor the handshake lines so that the WD9914 is synchronous with the talker/listeners and only sends ATN true at the end of byte transfer. This ensures that no data is lost or corrupted.

Request Parallel Poll (rpp)0/1xx01110

This is executed by the controller in charge to send the parallel poll command over the interface (the WD9914 must be in the Controller Active State so that the Attention line is asserted). The poll is completed by reading the Command Pass Through Register to obtain the status bits, then sending 'rpp' with the CS bit at zero.

Take Control Asynchronously (tca)naxx01100

This command is used by the controller in charge to set the attention line true and to gain control of the interface. The command is executed immediately and data corruption or loss may occur if a talker/listener is in the process of transferring a data byte.

Send Interface clear (sic)0/1xx01111

The IFC line is set true when this command is sent with CS set to one. This must only be sent by the system controller and should be reset (CS = 0) after the IEEE minimum time for IFC has elapsed (100 μs). The system controller is put into the controller active state.

Send Remote Enable (sre)0/1xx10000

Issued by the system controller to set the REN line true and send the remote enable message over the interface, REN is set false by sending 'sre' with CS at zero.

Request Control (rqc)naxx10001

When the TCT command has been recognized via the unidentified command pass through, this command is sent by the MPU. The WD9914 waits for the ATN line to go false and then enters the controller active state (CACS).

Release Control (ric)naxx10010

This command is used after TCT has been sent and handshake completed to release the ATN line and pass control to another device.

Disable All Interrupts (dai)0/1xx10011

The $\overline{\text{INT}}$ line is disabled, but the interrupt registers and any holdoffs selected are not affected.

Pass Through Next Secondary (pts)naxx10100

This feature may be used to carry out a remote configuration of a parallel poll. The parallel poll configure command (PPC) is passed through the WD9914 as an unrecognized addressed command and is identified by the MPU. The 'pts' command is loaded, and the next byte received by the WD9914 is passed through via the Command Pass Through Register. This would be the parallel poll enable (PPE), which is read by the microprocessor.

Set T1 Delay (std1)1xx10101

The T1 delay time can be set to 6 clock cycles (1.2 μs at 5 MHz) if this command is sent with the CS bit at one. The TI delay time is 11 clock cycles (2.2 μs at 5 MHz) following a power-on reset or if the command is sent with CS set to zero.

Shadow Handshake (shdw)0/1xx10110

This feature enables the controller in charge to carry out the listener handshake without participating in a data transfer. The Data Accepted line (DAC) is pulled true a maximum of 3 clock cycles after Data Valid (DAV) is received, and Not Ready For Data (NRFD) is allowed to go false as soon as DAV is removed.

The shadow handshake function allows the 'tcs' command to be synchronized with the Acceptor Not Ready State (ANRS) so that ATN can be re-asserted without causing the loss or corruption of data byte. The END interrupt can also be received and causes a RFD holdoff to be generated.

Very Short T1 Delay (vstd1)0/1xx10111

If this feature is enabled, the GPIB settling time (T1) will be reduced to 3 clock cycles (600 ns at 5 MHz) on the second and subsequent data bytes when ATN is false. Otherwise, the GPIB settling time is determined by the std1 feature.

Request Service Bit 2 (rsv2)0/1xx11000

The rsv2 bit performs the same function as the rsv1 bit but provides a means of requesting service which is independent of the Serial Poll Register.

This allows minor updates to be made to the Serial Poll Register without affecting the state of the request service.

In addition, rsv2 is cleared when the serial poll status byte is sent to the controller during a serial poll. It is therefore used in situations where a service request is simply a request from an instrument for the controller to poll its status. As soon as this happens, rsv2 is cleared since the reason for requesting service has been satisfied. This eliminates the burden of clearing the bit from the host MPU but also guarantees that rsv2 is cleared before another serial poll can occur. If this were not so, there would be a possibility of a second status byte being sent with the RQS message true, which could result in confusion for the controller. (rsv2 is cleared on: SPAS.(APRS1 + APRS2).STRS).

Bus Status Register

ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN	
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

The host MPU may examine the status of the GPIB management lines at the time of reading.

The IFC bit of this register does not indicate a true value if the device is a system controller using the 'sic' auxiliary command.

Serial Poll Register

S8	rsv1	S6	S5	S4	S3	S2	S1	
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

S8, S6-S0 Device status
rsv1 Request service bit 1

Bits S8, S6-S1 of this register are sent out over the GPIB when the device is addressed during a serial poll. They are cleared by a hardware reset but not by 'swrst' and may therefore be set up during configuration of the chip. These bits are fully double buffered and if the register is written to while the device is addressed during a serial poll (serial poll active state, SPAS), the value written is saved, and these bits are updated when SPAS is terminated.

The rsv1 bit provides an input to the service request function of the WD9914 and is used to instruct this to request that the controller service the device. When rsv1 is set true, the SRQ line is pulled true on the GPIB, and the controller typically responds by setting up a serial poll to obtain the status of all instruments on the bus that may require service. When the WD9914 is addressed to send its status byte, SRQ is set false, and the status byte is sent with the RQS message true on DIO7. The rsv1 bit must then be cleared and set true again if service is to be requested a second time. The SPAS interrupt is set immediately following the status byte being sent.

The rev1 bit is also cleared by the hardware reset pin but not by 'swrst'. It is not double-buffered but the service request function comprehends changes in the state of rsv1 while the device is in SPAS. The Serial Poll Register may therefore be written to any time.

Command Pass Through Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

This provides a means of directly inspecting the GPIB data lines (DIO(8-1)). It has no storage and should only be used when the data lines are known to be in a steady state such as will occur during a DAC holdoff or in CPWS during a parallel poll. It is used to read unrecognized commands and secondaries following a UNC interrupt or to read secondary addresses following an APT interrupt. In addition, an active controller uses this register to read the results of a parallel poll at least 2μs after setting the 'rpp' auxiliary command.

Parallel Poll Register

PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1	
DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

When a controller initiates a parallel poll, the contents of this register are presented to the GPIB data lines. If all bits of the register are cleared, then none of the lines DIO(8-1) will be pulled low during a parallel poll which corresponds to the Parallel Poll Idle State (PPIS) of IEEE-488. If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set to a 1.

The Parallel Poll Register is fully double buffered. If it is written to during a parallel poll, the new value is held until the parallel poll ends, at which point the register is updated. This permits the host MPU to update the parallel poll response completely asynchronously to the GPIB.

If this register is cleared by the hardware RESET pin but not by 'swrst,' it may be loaded while the chip is being configured with 'swrst' set.

Data In Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

This register is used to hold data received by the WD9914 when it is a listener. It is loaded during Accept Data State (ACDS1) and, following this, an RFD holdoff will occur. This will normally be released when the byte is read by the host MPU, but if the Holdoff On All Data (hdfa) feature is selected, this holdoff must be released by the 'rhdf' auxiliary command.

If the Holdoff On End (hdfe) feature is selected, the RFD holdoff will be released by reading the Data In Register. But if the EOI line is true when the byte is received, reading the data byte will not release the holdoff and rhdf must be used.

As the Data In Register is loaded, the BI interrupt is set. The END interrupt is set simultaneously if the byte is accompanied by a true EOI line.

Data Out Register

DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1	GPIB
D0	D1	D2	D3	D4	D5	D6	D7	MPU BUS

The Data Out register is used by a controller or talker for sending interface messages and device dependent messages. When the WD9914 enters the Talker Active State (TACS) or the Controller Active State (CACS), the contents of the Data Out Register are presented to the GPIB data lines (DIO(8-1)), and the byte is sent over the bus under the control of the Source Handshake. Each time a byte is written, the source handshake is enabled, and the byte is sent. If the handshake is interrupted before the byte can be sent, then it will be sent next time the Source Handshake becomes active unless a new byte available false (nbaf) auxiliary command is written. This has the effect of clearing an unsent byte from the Data Out Register, and although the register itself is not cleared the WD9914 behaves as if it had not been loaded.

Each time the source handshake becomes active and there is no unsent byte in the Data Out Register, a BO interrupt will occur informing the host MPU that the Data Out Register is available for use.

The Data In Register and Data Out Register operate independently. The Data Out Register is not double buffered, and its contents are output directly to the data lines of the GPIB.

DIRECT MEMORY ACCESS

The WD9914 can operate in DMA using the $\overline{\text{ACCRQ}}$ (DMA request) and $\overline{\text{ACCGR}}$ (DMA grant) DMA handshake lines. The operation is automatic within the WD9914 and needs no 'mpu' configuration.

The $\overline{\text{ACCRQ}}$ signal is set by (BO.$\overline{\text{CACS}}$ + BI) and can therefore not be used by a controller while ATN is asserted. It is reset by 'swrst' readin data in register, writing to the data out register and $\overline{\text{ACCGR}}$. It is not cleared by reading interrupt status register 0.

If using DMA, the internal CE and addressing is disabled by the $\overline{\text{ACCGR}}$ signal going low and $\overline{\text{ACCGR}}$ will automatically address either the data in register (DBIN = 0) or the data out register (DBIN = 1).

NOTE:
The sense of DBIN is inverted for DMA operation.

At the end of a DMA read from memory sequence, the $\overline{\text{ACCRQ}}$ will be left low (also BO bit set). It may be necessary for the 'mpu' to clear this in some circumstances, e.g., starting DMA write to memory sequence.

In DMA it is recommended that the MA interrupt be unmasked to prevent errors due to interrupted data streams.

If DMA is not being utilized, the $\overline{\text{ACCGR}}$ signal must be held high. In this case, the $\overline{\text{ACCRQ}}$ signal can be used as a separate interrupt line for BO and BI. This allows faster 'mpu' transfers to take place as it is not necessary to read the interrupt register to find the cause of the interrupt. Figure 2 shows a typical DMA configuration.

TERMINAL ASSIGNMENTS AND FUNCTIONS

The IEEE-488 standard uses the negative logic convention for the GPIB lines. The FALSE state (0) is represented by a high voltage (>2.0 V); the TRUE state (1) is represented by a low voltage (<0.8 V). The GPIB terminations of the WD9914 are in agreement with this convention. For example, if Data Valid is true (1), the DAV line is pulled low by the device. These terminations are connected to the bus via noninverting buffers to obtain the correct signal polarity.

Note that the terminations on the microprocessor side of the device are in positive logic (true state (1) = high voltage : false state (0) = low voltage). This is in agreement with the logic convention used by most microprocessors. Thus if:

DO(MSB) D7(LSB)

0	1	1	0	1	0	0	1

is written into the data out register, it will appear as:

DIO8(MSB) DIO1(LSB)

HIGH	LOW	LOW	HIGH	LOW	HIGH	HIGH	LOW

on the IEE-488 D10 lines.

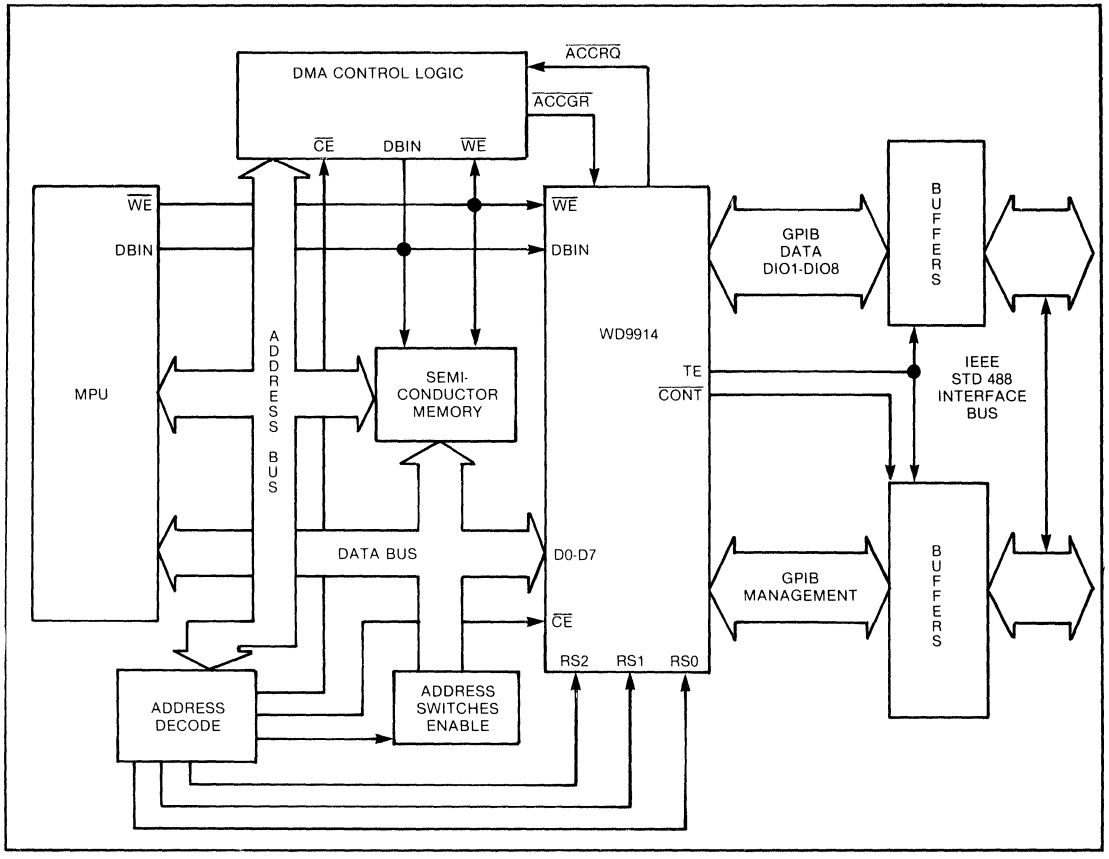


Figure 2. DMA CONFIGURATION

TRANSCEIVER CONNECTIONS

There are three linear transceivers designed to work with the WD9914: The SN75160, SN75161, and SN75162. Data sheets for these are included as Appendix C. Figure 3 shows the possible transceiver connections. Note that there is a corresponding pinout between the WD9914 and the transceivers. This allows the whole GPIB interface to be laid out in a very small area of printed circuit board.

The SN75160 is a 20 pin device used to buffer the IEEE-488 data lines (DIO(8-1)) in all applications. The direction of the buffers is controlled by the Talk Enable (TE) output of WD9914. This active high signal becomes true whenever there is an interface function of the WD9914 not sending the NUL message on DIO(8-1), that is, when the device is in TACS, CACS, SPAS, or PPAS. The Pull-Up Enable (PE) input of the SN75160 is an active high input which selects whether the 'DIO(8-1)' lines are driven by open collector or push/pull buffers. A push/pull buffer is required if faster data rates are required and the 'stdl' and/or the 'vstdl' features are used. Open collectors must be used if parallel polling is being used in a particular GPIB environment. If only one of these features is desired the PE input may be hardwired otherwise it must be derived from ATN and EIO, as shown in Figure 3.

The SN75161 is a 20-pin device used to buffer the IEEE-488 management lines. It may be used for a talker/listener device or for a controller which does not pass control. The direction of the handshake line buffers NRFD, NDAC, DAV are again controlled by the TE signal. However, the SRQ, ATN, REN, and IFC buffers are controlled by the DC input of the SN75161, which connects to the Controller Active ($\overline{CONT}$) output of the WD9914. $\overline{CONT}$ becomes low whenever the WD9914 is an active controller, that is, when it is not in CIDS or CADS. The SN75161 also includes the logic necessary to control the direction of the EOI buffer. This is dependent on the TE signal when ATN is false (high) and the DC signal when ATN is true (low).

The SN75162 is a 22-pin device which may be used to buffer the IEEE-488 management lines in all applications including devices which pass control. The SN75162 has a separate pin to control the direction

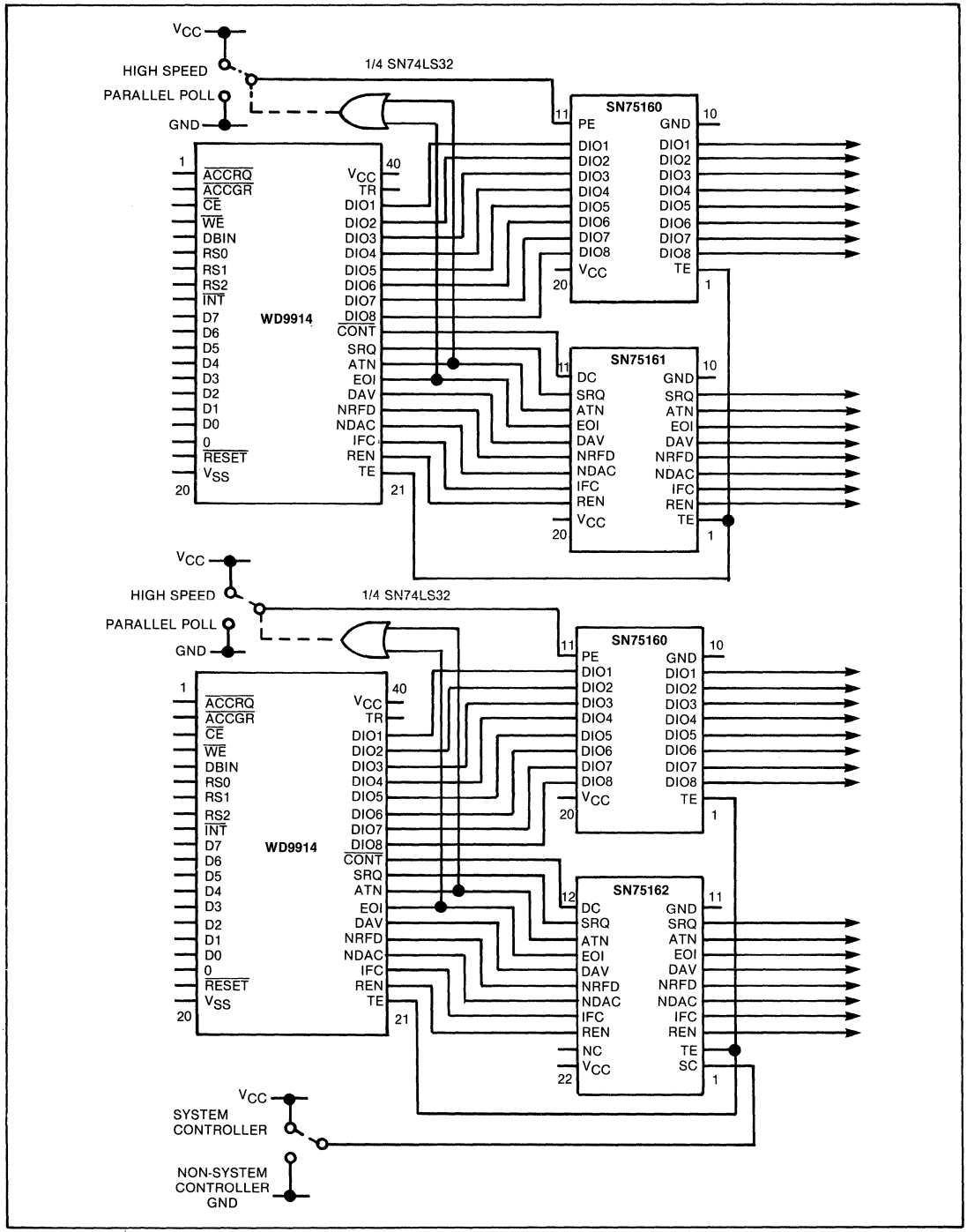


Figure 3. TRANSCEIVER CONNECTIONS

of the REN and IFC buffers, but is otherwise identical to the SN75161 in all other respects. This input is the System Controller input (SC) which may be hardwired or switchable to determine whether or not the instrument in question is a system controller or not. Note that a device which has its buffers configured as a non-system controller should never use the 'sic' and 'sre' auxiliary commands.

STATE DIAGRAM IMPLEMENTATION

This section presents the state diagrams for the WD9914.

Where equivalent, the names of WD9914 states are the same as those of IEEE-488. In some cases, IEEE-488 states have been divided, for example, ACDS of the IEEE-488 has been split into ACDS1 and ACDS2. The convention of lower case characters for local messages and upper case for remote messages and interface states is retained.

State diagrams with remote message outputs are supplemented with tables. T is used to represent a true output and F a false output. Parentheses denote a passive output; otherwise, it is active. The outputs shown are the values presented to the bus and assume the use of the SN75160 and SN75161 or SN75162 transceivers or their logical equivalents. The symbol (NUL) associated with DIO(1-8) indicates that each of these lines is sent passive false by the function in question.

NOTE:
An arrow into a state with no state as its origin represents a transition from every other state on the diagram. Note, however, that this does not imply that all exit conditions from the destination state are overridden. If such an entry condition is true and, simultaneously, an exit condition is true then this represents an illegal situation and should be avoided. Such situations will not occur in normal operation of the device.

No maximum timings are discussed. The WD9914 with its recommended transceivers meets all IEE-488 maximum timing requirements. If the WD9914 is used with other transceivers, then it must be ensured that these requirements are still met.

AUXILIARY COMMANDS

There are two basic types of commands implemented in the auxiliary command regiater: immediate execute and clear/set.

The clear/set commands are used to enable and disable the various features of the WD9914. The particular feature is selected by the code on f0-f4 and it is set or cleared according to the value on the cs bit. For the purposes of the state diagrams, the mnemonic of a clear/set command simply represents its current state.

The immediate execute auxiliary commands remain active for the duration of a strobe signal after the auxiliary command register has been written to. This is represented in the form of a state diagram in Figure 5. Note that writes to the auxiliary command register must be spaced by at least five clock cycles. For the purposes of the remaining state diagrams, the immediate execute commands are represented as the mnemonic gated by the auxiliary command strobe state (AXSS).

The clear/set bit of the auxiliary command register is used by several of the immediate execute commands, for example, 'dacr' uses it to differentiate between valid and not valid secondary addresses when releasing a DAC holdoff on a secondary address. The 'lon' and 'ton' auxiliary commands are also considered immediate execute.

The 'fget' and 'rtl' auxiliary commands are both immediate execute and clear/set. They may be cleared or set in the normal way, but if they are cleared when they are already in the false state, they will pulse true for the duration of AXSS. In the following state diagrams, however, these are simply included in their clear/set form.

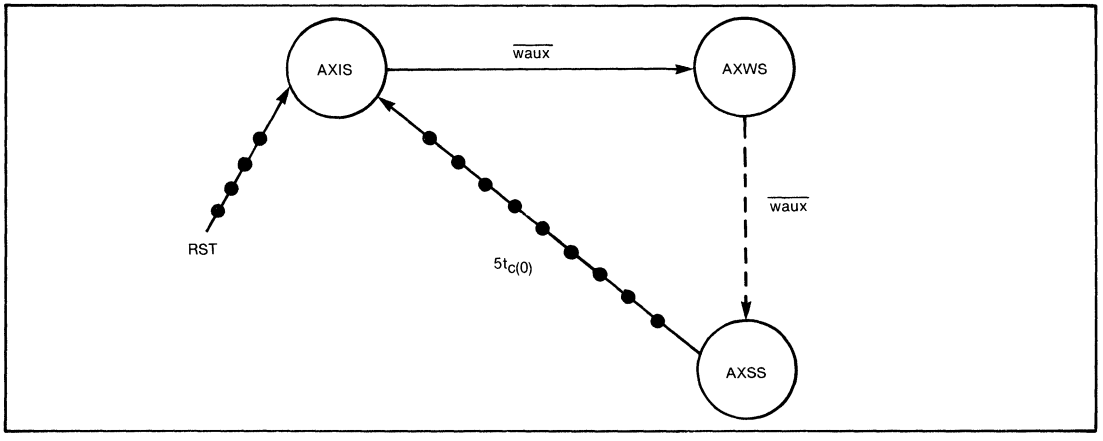


Figure 4. WD9914 AUXILIARY COMMAND STATE DIAGRAM

Table 5. AUXILIARY COMMAND STATE DIAGRAM MNEMONICS

MESSAGES			STATES		
waux	=	write to auxiliary command register	AXIS	=	auxiliary command register idle state
$t_{c(0)}$	=	clock cycle time	AXWS	=	auxiliary command write state
			AXSS	=	auxiliary command strobe state

ACCEPTOR HANDSHAKE

The WD9914 acceptor handshake is shown in Figure 5. The main variation from IEEE-488 to note is that the device remains in AIDS while the controller function is in CACS. The WD9914, therefore, does not monitor the commands which it sends over the bus and this places some restrictions on the user.

The accept data state of IEEE-488 (ACDS) is divided into two states. The first, (ACDS1) is used to strobe data into the Data In Register or to sequence the decoding of commands from the bus. All interrupts generated by the acceptor handshake (GET, MA, MAC, DCAS, APT, UCG, BI, and END) are generated by this state. The second (ACDS2) is used as a holding state where the device will remain in the event of a DAC holdoff.

Certain of the commands will cause interrupts in ACDS1 and, if the interrupts are unmasked, a DAC holdoff will occur. The interrupts concerned are GET, MA, DCAS, UCG, and APT. This is represented in the state diagram by the signal SAHF which becomes true when one of the above interrupts is set if it is unmasked. It persists for the duration of ACDS1. This event is stored by causing the ADHS to become active which inhibits the transition from ACDS2 to AWNS. ADHS is cleared by 'dacr.' Table 19 shows the response of the WD9914 to the various bus commands.

If a GET command is received in ACDS1, then the TR pin will be set high. This high condition persists throughout ACDS1 and ACDS2, which means that if a DAC holdoff occurs, the TR pin will remain high until the holdoff is released by a 'dacr' auxiliary command.

Two additional state diagrams are included to record

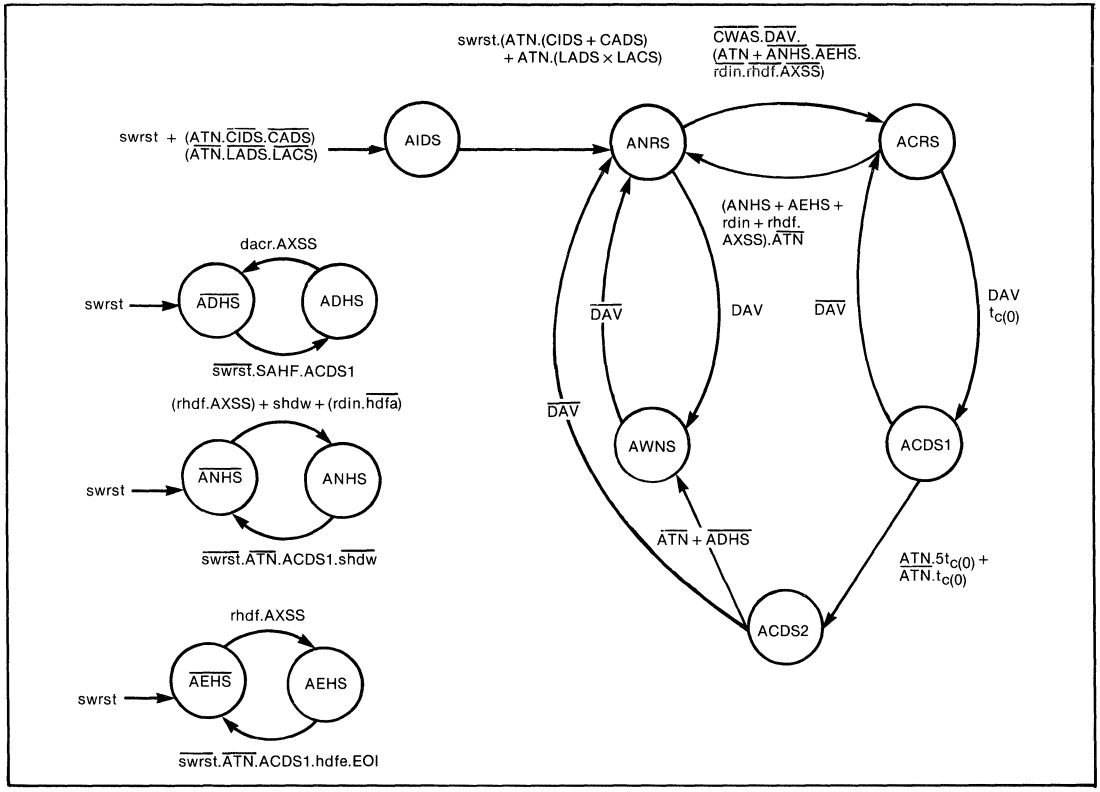


Figure 5. WD9914 ACCEPTOR HANDSHAKE STATE DIAGRAM

the type of data received in ACDS1 when ATN is false. ANHS indicates that a data byte has been received and that an RFD holdoff should be caused before the next data byte is accepted. The holdoff may be released by reading the Data In Register unless the 'hdfa' feature is enabled in which case 'rhdf' must be used. AEHS shows that the last data byte was accepted with the EOI message true and the 'hdfe' feature set. This will cause an RFD holdoff which can only be released by 'rhdf.'

Table 6. ACCEPTOR HANDSHAKE MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	AIDS	=	acceptor idle state
dacr	=	DAC release	ANRS	=	acceptor not ready state
rhdf	=	release RFD holdoff	ACRS	=	acceptor ready state
shdw	=	shadow handshake	ACDS1	=	accept data state 1
rdin	=	read data in register	ACDS2	=	accept data state 2
hdfe	=	enable RFD holdoff after END messages received	AWNS	=	acceptor wait for new cycle state
hdfa	=	enable RFD holdoff on all data	ADHS	=	accept data holdoff state
ATN	=	attention	ANHS	=	acceptor not ready holdoff state
DAV	=	data valid	AEHS	=	acceptor not ready holdoff after 'END'
EOI	=	end or identify state	CWAS	=	controller wait for ANRS state (controller function)
RFD	=	ready for data	AXSS	=	auxiliary command strobe state (auxiliary command register)
DAC	=	data accepted	LADS	=	listener addressed state (listener function)
SAHF	=	set accept data holdoff state	LACS	=	listener active state (listener function)
$t_{c(0)}$	=	clock cycle time	CIDS	=	controller idle state (controller function)
			CADS	=	controller addressed state (controller function)

Table 7. ACCEPTOR HANDSHAKE MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT		OTHER ACTIONS
	RFD	DAC	
AIDS	(T)	(T)	
ANRS	F	F	
ACRS	(T)	F	
ACDS1	F	F	ATN False: — data entered into Data In Register — BI interrupt generated — end interrupt generated if EOI is true. ATN true: — commands decoded — command related interrupts set — sahf set if command requires a DAC holdoff — TR pin set true if GET message is received — 'pts' feature cleared after UNC interrupt set
ACDS2	F	F	TR — pin set true if GET command was received in ACDS1
AWNS	F	(T)	

SOURCE HANDSHAKE

The WD9914 source handshake state diagram is shown in Figure 6. IEEE-488 states SIWS and SWNS have been removed. These record the false then true transition of 'nba' (new byte available) as the old data byte is removed and a new data byte is made ready. Instead the WD9914 uses a separate state (SHFS) to record the availability of a data byte in the Data Out Register. This state is exited when a byte is written to the Data Out Register which enables the transition from SGNS to SDYS and the subsequent transmission of the byte. The SHFS is reentered as the byte is sent in STRS, but if the handshake is interrupted before this, then the fact that the byte has not been sent is recorded until the source handshake again becomes active. If, however, the byte in the data out register is to be disregarded, then 'nbaf' may be used to return the device to SHFS.

The status byte in the Serial Poll Register is continually available. The transition from SGNS to SDYS is not dependent on SHFS during a serial poll, that is, while SPAS is active. By separately recording the availability of a byte in the Data Out Register, a talker sending data may be interrupted for a serial poll without risk of a byte being lost.

The additional state SERS is included to detect an error condition on the bus. This will be entered when the source handshake tries to send a byte but finds both the NRFD and NDAC lines false at the same time. This condition will normally indicate for a controller that there are no devices powered up on the bus, or for a talker that there are no devices addressed to listen on the bus.

The state VSTS will be entered after the first data byte of a talker has been sent if the 'vstdl' feature is enabled. This enables a very short bus settling time ($4t_{c(0)}$) for all subsequent bytes until ATN next becomes true. The WD9914 will not use the short bus settling time when it is an active controller.

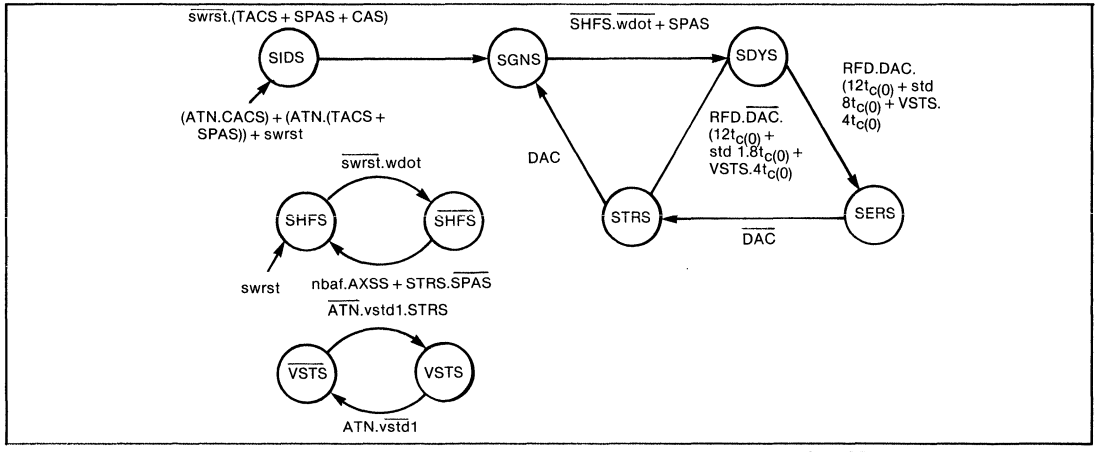


Figure 6. WD9914 SOURCE HANDSHAKE STATE DIAGRAM

Table 8. SOURCE HANDSHAKE MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	SIDS	=	source idle state
nbaf	=	new byte available false	SGNS	=	source generate state
wdot	=	write to the data out register	SDYS	=	source delay state
stdl	=	enable short bus settling time	SERS	=	source error state
vstdl	=	enable very short bus settling time	STRS	=	source transfer state
ATN	=	attention	SHFS	=	source holdoff state
RFD	=	ready for data	VSTS	=	very short bus settling time state
DAC	=	data accepted	TACS	=	talker active state (talker function)
$t_{c(0)}$	=	clock cycle time	CACS	=	controller active state (controller function)
			SPAS	=	serial poll active state (talker function)
			AXSS	=	auxiliary command strobe state (auxiliary command register)

Table 9. SOURCE HANDSHAKE MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT DAV	OTHER ACTIONS
SIDS	(F)	BO interrupt and ACCRQ set
SGNS	F	true if SHFS is false and SPAS is not true
SDYS	F	
SERS	F	ERR interrupt set true
STRS	T	

TALKER AND LISTENER FUNCTIONS

Figures 7 and 8 show the WD9914 listener and talker state diagrams, which serve the purpose of the listener and talker or extended listener and extended talker functions of IEEE-488, depending on the state of the APT interrupt mask bit.

The WD9914 does not recognize secondary addresses on-chip and these must be passed through to the host MPU for verification. Secondary addressing is enabled by unmasking the APT interrupt. A secondary address will cause this interrupt if the last primary command received was a primary address of the device, that is, it is in TPAS or LPAS. A DAC holdoff will also occur. The host MPU must respond to the interrupt by reading the secondary from the Command Pass Through Register and identifying it as being valid or not valid. The holdoff may then be released with a 'dacr' auxiliary command, the sense of the 'cs' bit being used to indicate a valid (cs = 1) or not valid (cs = 0) secondary. If a valid secondary address is indicated then the WD9914 will enter TADS or LADS depending on whether it is in TPAS or LPAS.

The 'lon' and 'ton' auxiliary commands together with the clear/set bit (cs) have a direct influence on the appropriate state diagrams. Therefore, although they appear as ordinary clear/set auxiliary commands, they can be effectively cleared by other bus events. For example, if a WD9914 addresses itself as a listener via the 'lon' command it may be returned to LIDS by an UNL command from the bus at a later time.

The 'lon' and 'ton' auxiliary commands are used to implement two features of IEEE-488. First, talk only and listen only are used in situations where there is no active controller on the bus. Note that the 'lon' and 'ton' commands are linked with these features to indicate to the user that these commands are not enabled by CAS as are 'ltn' and 'lun' of IEEE-488.

Second, the 'lon' and 'ton' auxiliary commands are used by an active controller to address itself. IEEE-488 provides for a controller to address itself to listen via the 'ltn' and 'lun' message but there is no corresponding message for the talker. Hence, when a controller addresses itself to talk via 'ton,' it must send its talk address over the bus and similarly, if it sends another talk address over the bus then it must unaddress itself by writing 'ton' false.

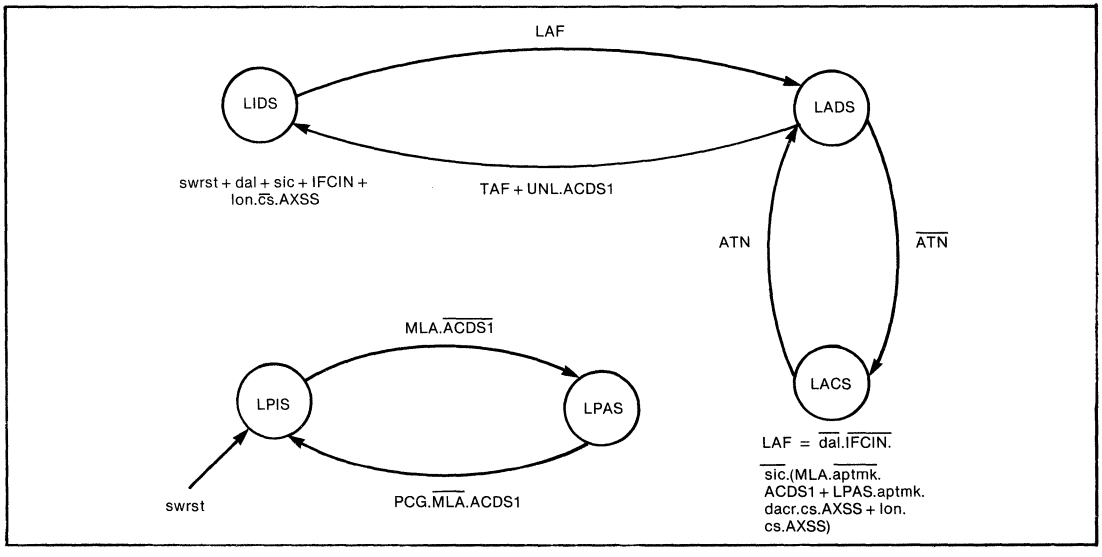


Figure 7. WD9914 LISTENER STATE DIAGRAM

When the WD9914 enters SPAS, the contents of the serial poll register are sampled and presented on DIO(8-1). These will remain unchanged until SPAS is exited. The source handshake will, however, send this status byte as many times as the controller will accept it.

The internal IFC signal of the WD9914 (IFCIN) is suppressed when the device itself is sending IFC in order to simplify implementation of the controller function. Therefore, the send interface clear (sic) auxiliary command is included with IFCIN to return the talker and listener functions to their idle states and allow a system controller to clear its own interface.

A separate state diagram is included to control the sending of the END message of IEEE-488. If the 'feoi' auxiliary command is written followed by loading a byte into the Data Out Register, the WD9914 will enter ERAS, and the EOI line will be asserted as 'DIO(8-1)' begin to change. The function will enter ENAS as soon as the source handshake begins to send this byte, and EOI will be released when the Data Out Register is next loaded. If it is desired to send EOI true with the next byte as well, then 'feoi' may be written before the Data Out Register returns the device to ERAS.

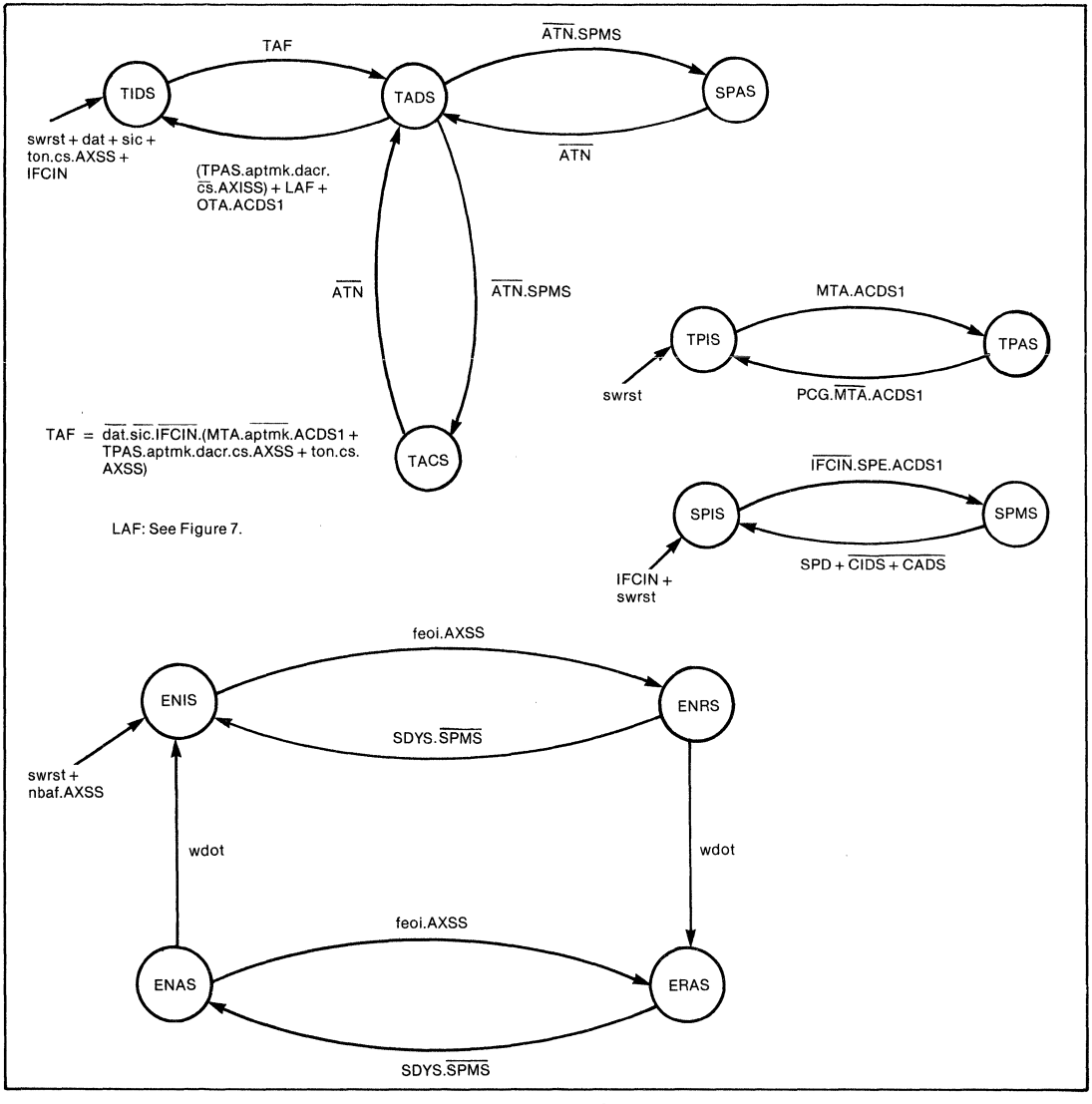


Figure 8. WD9914 TALKER STATE DIAGRAM

Table 10. TALKER AND LISTENER MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	LIDS	=	listener idle state
dal	=	disable listener	LADS	=	listener addressed state
dat	=	disable talker	LACS	=	listener active state
sic	=	send interface clear	LPIS	=	listener primary idle state
lon	=	listen only	LPAS	=	listener primary addressed state
ton	=	talk only	TIDS	=	talker idle state
cs	=	clear/set bit of the auxiliary command register	TADS	=	talker addressed state
dacr	=	release 'DAC' holdoff	TACS	=	talker active state
aptmk	=	address pass through interrupt mask	SPAS	=	serial poll active state
nbaf	=	new byte available false	SPIS	=	serial poll idle state
feoi	=	force 'EOI'	SPMS	=	serial poll mode state
wdot	=	write to the Data Out Register	TPIS	=	talker primary idle state
ATN	=	attention	TPAS	=	talker primary addressed state
IFCIN	=	internal interface clear message (a debounced signal, suppressed by 'sic')	ENIS	=	end idle state
EOI	=	end or identify	ENRS	=	end ready state
PCG	=	primary command group	ERAS	=	end ready and active state
MLA	=	my listen address	ENAS	=	end active state
MTA	=	my talk address	SDYS	=	source delay state (source handshake)
OTA	=	other talk address	CIDS	=	controller idle state (controller function)
SPE	=	serial poll enable	CADS	=	controller addressed state (controller function)
SPD	=	serial poll disable	ACDS1	=	accept data state 1 (acceptor handshake)
UNL	=	unlisten	AXSS	=	auxiliary command strobe state (auxiliary command register)
PCG	=	primary command group			

Table 11. TALKER FUNCTION MESSAGE OUTPUTS

STATE	QUALIFIER	REMOTE MESSAGES SENT		OTHER ACTIONS DIO(8-1)
		RQS	EOI	
TIDS		(F)	(F)	(NUL)
TADS		(F)	(F)	(NUL)
TACS	ENIS.ENRS	(F)	F	DATA OUT REG
TACS	ENAS.ERAS	(F)	T	DATA OUT REG
SPAS	NPRS.SRQS	F	F	SERIAL POLL REG
SPAS	APRS1.APRS2	T	F	SERIAL POLL REG

SERVICE REQUEST FUNCTION

Figure 9 shows the state diagram for the WD9914 service request function. The device has two means of implementing the request service (rsv) local message of IEEE-488: the first, 'rsv1,' is bit 7 of the Serial Poll Register; the second is the auxiliary command 'rsv2.' These are simply ORed together to provide an input to the service request function, and, in any particular application, only one would normally be used, the other being left in its hardware reset state.

The affirmative poll response state (APRS) of IEEE-488 is split into two states on the WD9914 for the following reason: Consider the case where a device has requested service, has been serial polled, and then wishes to request service again. The host MPU must clear the 'rsv' message and then set it true again. Now suppose this temporary false condition happens within one occurrence of SPAS. If the service request function has been implemented exactly as per IEEE-488, it will not be recognized, and SRQ will not be asserted a second time. Therefore, 'rsv' may only be cleared when the device is known not to be in SPAS, which can only happen if it is cleared as a consequence of some pre-arranged action of the controller. This action would normally be a part of the service routine executed by the controller as a response to the request for service. For example, if service was requested by an instrument which had some data to send for processing or to a printing device then 'rsv' could be cleared when it is addressed to talk and send its data over the bus.

For many applications, the fact that the device has been serial polled after requesting service is considered sufficient response from the controller. The 'rsv' local message therefore simply becomes a request for the controller to read its serial poll status byte. It is then desirable to be able to clear and reassert 'rsv' at any time after the serial poll status byte has been polled and the SPAS interrupt set. The WD9914 is able to record a false transition of 'rsv1' or 'rsv2' by moving from APRS1 to APRS2 even if the device is in SPAS. This makes the above approach to serial polling possible.

To further support this approach, the 'rsv2' auxiliary command is automatically cleared when the serial poll status byte is polled, ensuring that 'rsv2' is cleared before a second serial poll can occur. If this were not the case, then the same status byte might be polled twice by the controller with the RQS bit true, which may indicate that two reasons for requiring service have arisen.

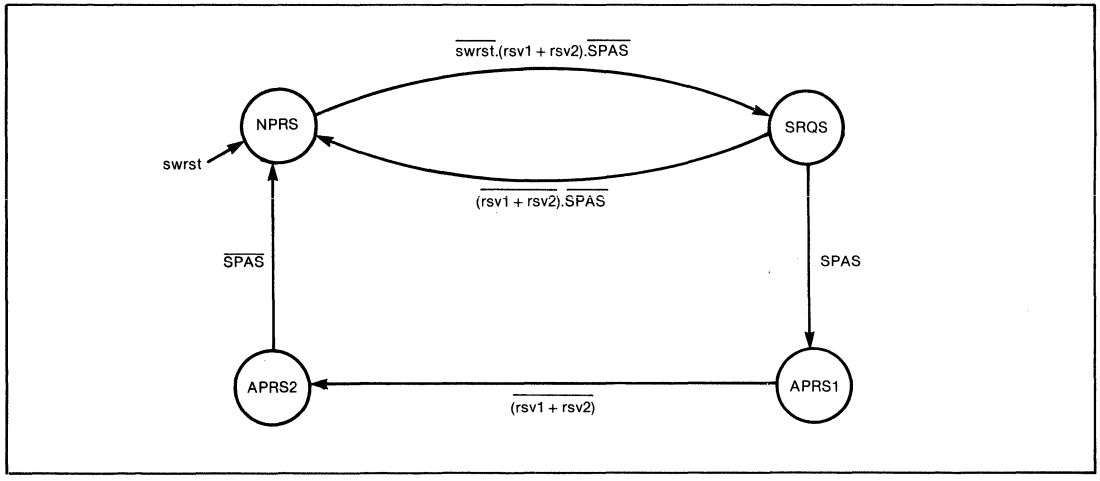


Figure 9. SERVICE REQUEST STATE DIAGRAM

The WD9914 will only send one serial poll status byte during each active period of SPAS. However, it will send this status byte as many times as the controller is prepared to accept it. Therefore, the controller should only read the status byte once per serial poll; otherwise, each time a status byte is sent with the RQS message true, the SPAS interrupt will be generated and 'rsv2' will be cleared.

Table 12. SERVICE REQUEST MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	NPRS	=	negative poll response state
srv1	=	request service 1 (bit 7 of serial poll register)	SRQS	=	service request state
rsv2	=	request service 2 (auxiliary command register)	APRS1	=	affirmative poll state 1
			APRS2	=	affirmative poll state 2
			SPAS	=	serial poll active state (talker function)

Table 13. SERVICE REQUEST MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT SRQ	OTHER ACTIONS
NPRS	(F)	
SRQS	T	
APRS1	(F)	— rsv2 cleared if in SPAS and STRS — SPAS interrupt set if in SPAS when STRS is exited
APRS2	(F)	— same as APRS1

REMOTE/LOCAL FUNCTION

The WD9914 remote local state diagram is shown in Figure 10. If differs little from that of IEEE-488.

The complete listener function (LAF) is used to effect the transition from LOCS to REMS or from LWLS to RWLS. This means that if the APT interrupt is masked, the device will enter one of the remote states in response to its listen address, but if secondary addressing is enabled, then this will not happen until 'dacr' is written with 'cs' true in response to a valid secondary address. In addition, the transition to one of the remote states will occur if 'lon' is used to address the device to listen.

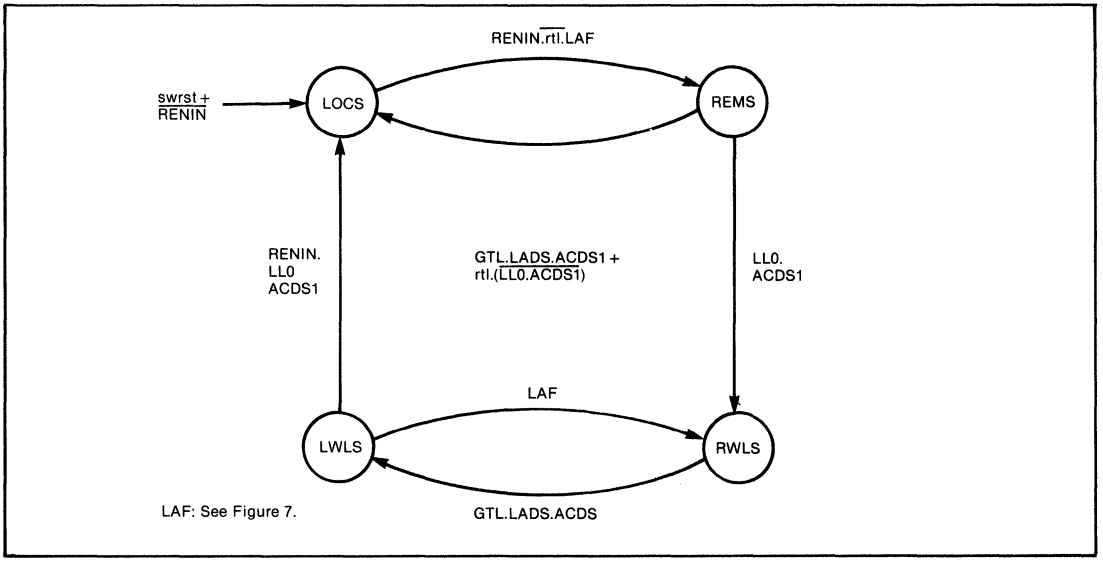


Figure 10. WD9914 REMOTE LOCAL STATE DIAGRAM

Table 14. REMOTE/LOCAL MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	LOCS	=	local state
rtl	=	return to local	REMS	=	remote state
RENIN	=	internal remote enable message (debounced)	RWLS	=	remote with lockout state
GTL	=	go to local	LWLS	=	local with lockout state
LLO	=	local lockout	LADS	=	listener addressed state (listener function)
			ACDS1	=	accept data state 1 (acceptor handshake)

PARALLEL POLL FUNCTION

The parallel poll function of the WD9914 only nominally supports logically-configured parallel poll. With a suitable software package, remotely-configured parallel poll may also be easily implemented. The state diagram is shown in Figure 11.

When the EOI and ATN lines become true simultaneously (the Identify message), the contents of the Parallel Poll Register are output to DIO(8-1). If parallel poll is to be used in a particular bus environment, then the Pull-Up Enable (PE) input of the SN75160 must be held low so that the DIO(8-1) are driven by open collector buffers. Parallel Poll, occurring when the Parallel Poll Register is in the hardware reset condition of all zeros, will result in none of DIO(8-1) being pulled low. This corresponds to the parallel poll idle state (PPIS). If it is desired to participate in a parallel poll, then the bit corresponding to the desired parallel poll response is set true. This implements the parallel poll standby state (PPSS), and, when the Identify message becomes true, the appropriate line of DIO(8-1) is pulled low. This is equivalent to the parallel poll active state (PPAS). Only one bit of the parallel Poll Register should be set true at once.

Remotely Configured Parallel Poll

The parallel poll configure command (PPC) is treated by the WD9914 as an unrecognized addressed command. It is passed through when the WD9914 is in LADS. If an instrument is to be remotely configured for parallel poll, then the pass through next secondary (pts) auxiliary command should be written before releasing the DAC holdoff. This will cause the next command received to also set a UNC interrupt if it is a secondary command. The secondary command will be either the parallel poll enable command (PPE) or the parallel poll disable command (PPD) and should be read from the Command Pass Through Register and identified. If it is the PPE command, then the attendant bits (S, P1, P2, P3) should be extracted and stored by the host MPU. The S bit should then be matched against the individual status of the instrument (represented by 'ist'), and if they are the same, the bit corresponding to the parallel poll response, specified by P1, P2, P3, should be set true in the Parallel Poll Register. If this is not the case, then the Parallel Poll Register should be cleared if it is not already clear. After this, each time the individual status of the device changes, the 'ist' should again be matched against the S bit and the Parallel Poll Register updated accordingly until PPD or PPU is received.

If a PPD command is passed through after the 'pts' feature has been written, the Parallel Poll Register should be cleared before the DAC holdoff is released. The PPC command that precedes PPD is an address command; it is a means of eliminating individual members of a parallel poll. The parallel unconfigure command is treated by the WD9914 as an unrecognized universal command. When it is passed through, the host MPU should clear its Parallel Poll Register before releasing the DAC holdoff. This command will clear all members of a parallel poll.

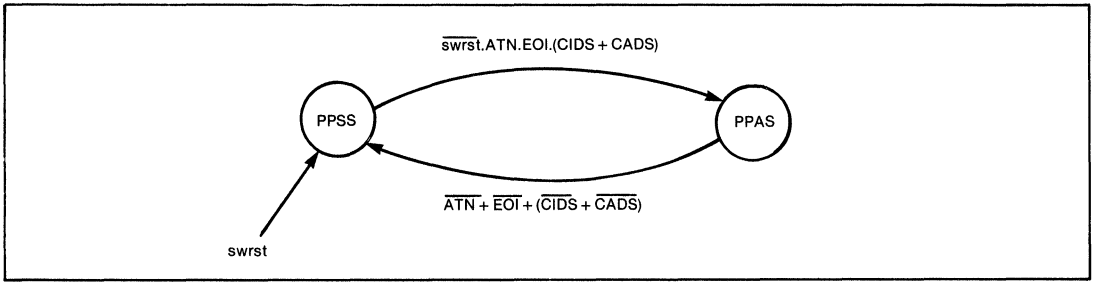


Figure 11. WD9914 PARALLEL POLL STATE DIAGRAM

Table 15. PARALLEL POLL MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	PPSS	=	parallel poll standby state
ATN	=	attention	PPAS	=	parallel poll active state
EOI	=	end or identify	CIDS	=	controller idle state (controller function)
			CADS	=	controller addressed state (controller function)

Table 16. PARALLEL POLL MESSAGE OUTPUTS

STATE	REMOTE MESSAGES SENT DIO(8-1)	OTHER ACTIONS
PPSS	(NUL)	
PPSS	PARALLEL POLL REG*	

*If there is a true bit in the Parallel Poll Register, it must be sent active; any false bit must be sent passive.

CONTROLLER FUNCTION

The controller function of the WD9914 is greatly simplified compared with that of IEEE-488. It relies heavily on software support but, with suitable software, it enables all subsets of the controller function to be implemented. With this approach the controller logic is reduced to a small proportion of the chip area which means that the device may be economically used in situations where a talker/listener only is required.

Figure 12 shows the controller function state diagram. With suitable software, it will perform the full controller function, as described in the IEEE-488A 1980 supplement to the IEEE-488 1978. It therefore includes the additional state CSHS, which allows time for DAV to be recognized false by all devices on the bus before ATN is asserted. The 'tcs' local message is implemented by an immediate execute auxiliary command. The state CWAS is therefore added to record the occurrence of this command until the acceptor handshake enters ANRS and the device can enter CSHS. The 'tca' auxiliary command also causes entry into CSHS although IEEE-488A 1980 allows it to move directly from CSBS to CSWS. This is done for convenience of implementation and results in the 'tca' auxiliary command taking an extra 1.6 microseconds to assert ATN.

The delay between CSWS and CAWS is slightly less than specified in IEEE-488A 1980 but the total time taken in moving from CSWS to CACS is still greater than the specified minimum.

The Controller Parallel Poll State (CPPS) is not included on the WD9914. To conduct a parallel poll, a WD9914 based controller must set the 'rpp' clear/set auxiliary command true when it is in CACS, moving it to CPWS which sends EOI true. The host MPU must then wait 2 microseconds before reading back the parallel poll responses via the Command Pass Through Register. The 'rpp' auxiliary command can then be cleared, EOI will go false, and the parallel poll is complete. The host MPU will receive a BO interrupt as soon as the WD9914 reenters CACS and the source handshake becomes active.

Controller Self Addressing

The acceptor handshake does not operate when the controller is active. This means commands being sent are not monitored, and special precautions are required as a consequence of this when addressing devices and when passing control.

When the controller is active, it uses 'ton' or 'lon' to address and unaddress itself. IEEE-488 provides for the controller to locally address itself to listen, but there is no corresponding local message for the talker. The WD9914 should always accompany a 'ton' auxiliary command with 'cs' true with its own talk address or an UNT command sent over the bus. Similarly, if the WD9914 sends the talk address of another device over the bus, it should ensure that it is in TIDS by writing the 'ton' auxiliary command false.

Passing Control

As Figure 12 shows, the controller transfer state (CTRS) of IEEE-488 is not present, and all transitions associated with the TCT command have been removed. Instead, two immediate execute auxiliary commands are included. Request control (rqc) will cause a transition from CIDS to CADS, and the release control command (rlc) will return the function to CIDS. The TCT command is treated similarly to an unrecognized addressed command but will cause a UNC interrupt if the device is in TADS.

Figure 13 is a representation of the sequence of events involved in passing control from one WD9914 based device to another. The device passing control must initially ensure that it is not in TADS; then it should send out the talk address of the device to receive control. The receiving device will enter TADS, and after any DAC holdoff has been released, the host MPU of the device passing control will set a BO interrupt indicating that it may then send the TCT command. The TCT command will cause a UNC interrupt to the host MPU of the receiving device, and also a DAC holdoff will occur. The host MPU of the receiving device must examine its Command Pass Through Register, and upon identifying TCT, should write the auxiliary command 'rqc' to put its WD9914 into CADS. The receiving device may then release DAC with a 'dacr' auxiliary command causing another BO interrupt at the device passing control. This indicates that the 'ric' auxiliary command may then be used by the host MPU of the device passing control to return its WD9914 to CIDS and allowing ATN to go false. The receiving device then enters CACS, asserts ATN, and its host MPU gets a BO interrupt as the source handshake becomes active. The passing of control is complete.

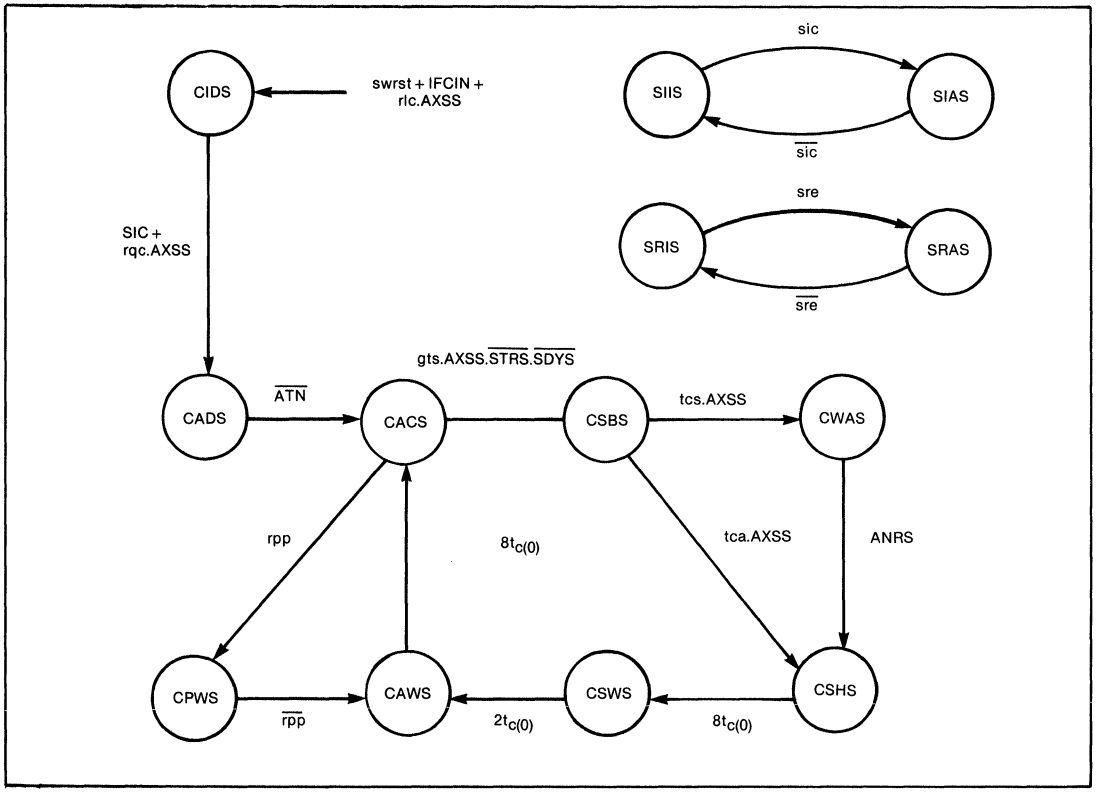


Figure 12. WD9914 CONTROLLER STATE DIAGRAMS

Table 17. CONTROLLER FUNCTION MNEMONICS

MESSAGES			STATES		
swrst	=	software reset	CIDS	=	controller idle state
sic	=	send interface clear	CADS	=	controller addressed state
sre	=	send remote enable	CACS	=	controller active state
rqc	=	request control	CSBS	=	controller standby state
rlc	=	release control	CSHS	=	controller standby hold state
gts	=	go to standby	CSWS	=	controller synchronous wait state
tcs	=	take control synchronously	CAWS	=	controller active wait state
tca	=	take control asynchronously	CPWS	=	controller parallel poll wait state
rpp	=	request parallel poll	ANRS	=	acceptor not ready state (acceptor handshake)
IFCIN	=	internal interface clear message (a debounced signal which is suppressed if 'sic' is true)	SDYS	=	source delay state (source handshake)
ATN	=	attention	STRS	=	source transfer state (source handshake)
$t_{c(0)}$	=	clock cycle time	AXSS	=	auxiliary command strobe state (auxiliary command register)
			LWAS	=	controller wait for ANRS state

Table 18. CONTROLLER FUNCTION MESSAGE OUTPUTS

STATE	REMOTE MESSAGE SENT			OTHER ACTIONS
	ATN	EOI	D10(8-1)	
CIDS	(F)	(F)	(NUL)	
CADS	(F)	(F)	(NUL)	
CACS	T	F	DATA OUT REG	Data Out Reg. may contain any of the commands in Table 19
CSBS	F	(F)	(NUL)	
CWAS	F	(F)	(NUL)	
CSHS	F	(F)	(NUL)	
CSWS	T	F	(NUL)	
CAWS	T	F	(NUL)	
CPWS	T	T	(NUL)	DIO(8-1) may be read via the Command Pass Through Register

STATE	REMOTE MESSAGES SENT	OTHER ACTIONS
	IFC	
SIIS*	(F)	Internal interface clear message IFCIN is held false
SIIS	F	
SIAS	T	

STATE	REMOTE MESSAGES SENT	OTHER ACTIONS
	REN	
SRIS*	(F)	
SRIS	F	
SRAS	T	

*Buffers not configured for a system controller; otherwise, buffers are configured for system controller.

The REN and IFC outputs of the WD9914 are controlled by the auxiliary commands 'sre' and 'sic.' These should never be used by the host MPU of a device unless it is the system controller. As may be seen from Figure 14, the REN and IFC outputs of the WD9914 are open drains with internal pull-ups. This means that the outputs are capable of driving the inputs of the buffers if the device is a system controller. If not, the buffers will drive into the REN and IFC pins and override the pull-ups. Hence, no direction control is required.

The false transition of REN and the true transition of IFC are both debounced to prevent noise on these lines from causing permanent state changes on the WD9914. In addition, the internal interface clear signal (IFCIN) is held false if the WD9914 is sending IFC. Figure 12 shows the reason for this. If the device is not a system controller, then the occurence of IFC will return the controller function to CIDS. If, however, the device is a system controller, when it asserts IFC and is in CIDS, the 'sic' auxiliary command will cause it to enter CADS. As IFCIN is suppressed, it will not be forced back into CIDS, and there will be no conflict.

System Controller

The WD9914 has no on-chip means of determining whether or not it is the system controller. Instead, this is determined by the software and by the configuration of the buffers to the IEEE-488 bus.

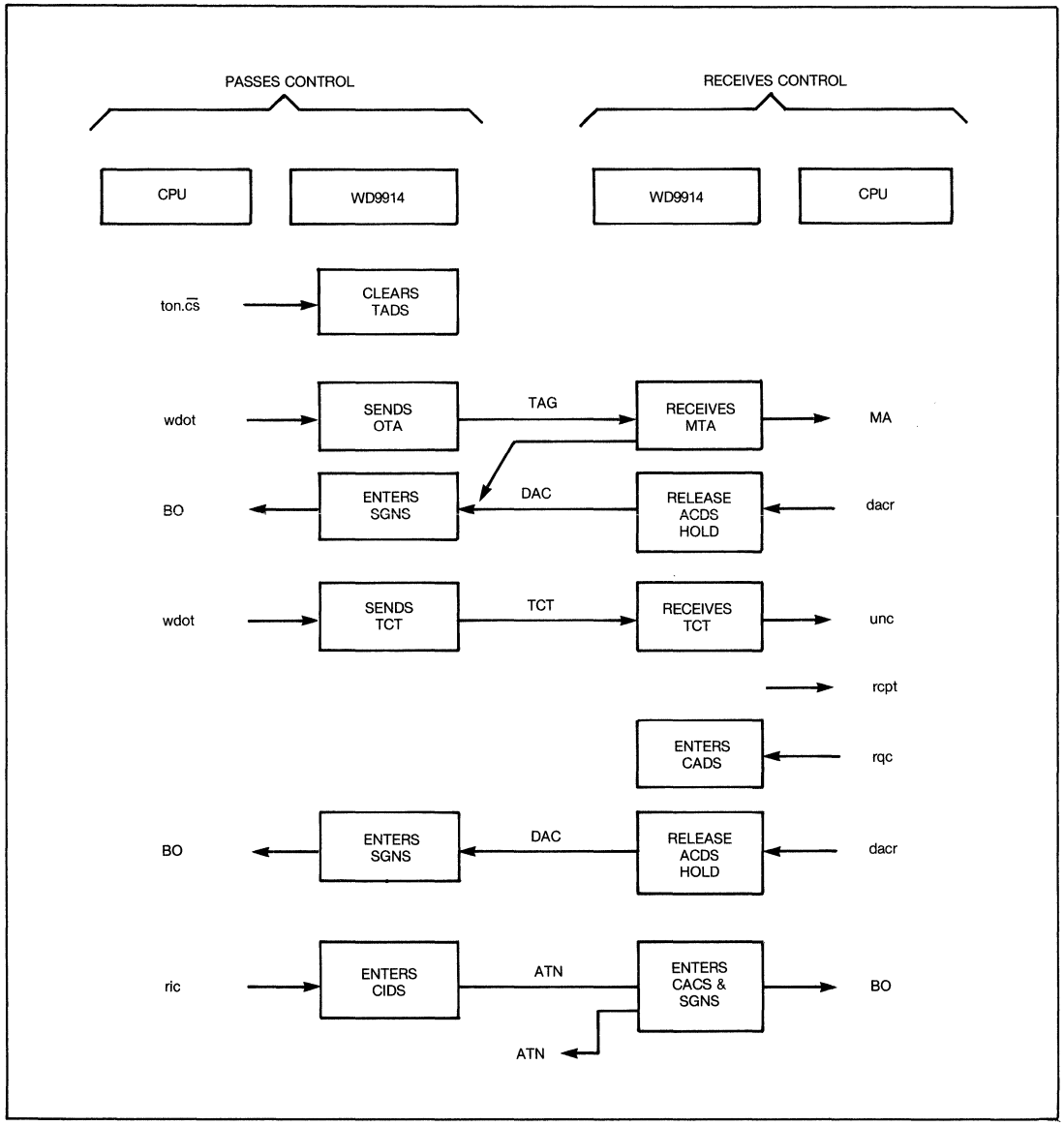
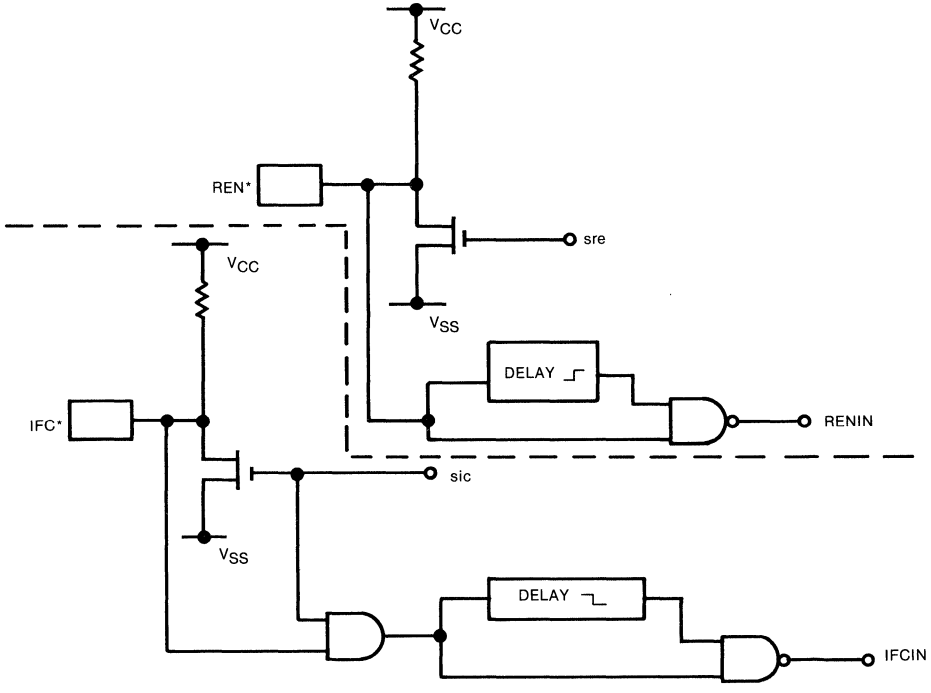


Figure 13. PASSING CONTROL BETWEEN WD9914



*The REN and IFC signals are at the pins of the WD9914 and are therefore negative logic signals. The remaining signals are conventional positive logic signals.

Figure 14. IFC AND REN PINS

Table 19. MULTILINE INTERFACE MESSAGES

COMMAND	SYMBOL	DIO 8-1	CLASS	INTERRUPT (1, 2)	DAC (3) HOLDOFF	NOTE
Addressed Command Group	ACG	000XXXX	AC	—	—	
Device Clear	DCL	X0010100	UC	DCAS	Yes	
Group Execute Trigger	GET	X0001000	AC	GET	Yes	
Go To Local	GTL	X0000001	AC	RLC	No	14
Listen Address Group	LAG	X01XXXXX	AD	—	—	
Local Lockout	LLO	X0010001	UC	None	No	
My Listen Address	MLA	X01AAAAA	AD	MA,MAC,RLC	MA Only	4,14
My Talk Address	MTA	X10AAAAA	AD	MA,MAC	MA Only	4
My Secondary Address	MSA	X11SSSSS	SE	APT	Yes	5,6
Other Secondary Address	OSA	SCG.MSA-	SE	APT	Yes	6,7
Other Talk Address	OTA	TAG.MTA-	AD	MAC	No	
Primary Command Group	PCG	ACG + UCG + LAG + TAG	—	—		
Parallel Poll Configure	PPC	X0000101	AC	UNC	Yes	8
Parallel Poll Enable	PPE	X110SPPP	SE	UNC	Yes	9,10
Parallel Poll Disable	PPD	X111DDDD	SE	UNC	Yes	9,11
Parallel Poll Unconfigure	PPU	X0010101	UC	UNC	Yes	12
Secondary Command Group	SCG	X11XXXXX	SE	—	—	
Selected Device Clear	SDC	X0000100	AC	DCAS	Yes	
Serial Poll Disable	SPD	X0011001	UC	None	No	
Serial Poll Enable	SPE	X0011000	UC	None	No	
Take Control	TCT	X0001001	AC	UNC	Yes	13
Talk Address Group	TAG	X10XXXXX	AD	—	—	
Unlisten	UNL	X0111111	AD	MAC	No	
Untalk	UNT	X1011111	AD	—	—	
Universal Command Group	UCG	X001XXXX	UC	None	No	

Classes: UC — universal command
AC — addressed command
AD — address
SE — secondary command

Symbols: 0 — logical zero (high level on GPIB)
1 — logical one (low level on GPIB)
x — don't care (received message)

NOTES:

1. Interrupts listed are as a direct consequence of the command received. They are set during ACDS1 and will cause the INT pin to be pulled low if unmasked.
2. The addressed commands will only cause their corresponding interrupt if the device is in LADS with the exception of TCT.
3. A DAC holdoff will only be caused if the corresponding interrupt is unmasked.
4. AAAAA represents the primary address of a device.
5. SSSSS represents the secondary address of a device.
6. Secondary addresses are handled via address pass through (APT interrupt). The host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.
7. If OSA is passed through via the APT interrupt,

the host MPU should respond by writing the 'dacr' auxiliary command with 'cs' false.

8. PPC is not recognized by the WD9914 and is therefore treated as an unrecognized addressed command.
9. PPE and PPD are secondary commands. These may be passed through to the host MPU using the 'pts' auxiliary command. When the PPC command is received the 'pts' auxiliary command should be written. PPE or PPD will then cause an APT interrupt.
10. SPPP specifies the sense bit, and the desired parallel poll response is a remotely configured parallel poll.
11. DDDD specifies don't care bits which must be sent as zeros but need not be decoded by the host MPU of the receiving devices.
12. PPU is not recognized by the WD9914 and will cause a UNC interrupt.
13. TCT is not recognized directly by the WD9914. It will cause a UNC interrupt when the device is in TADS.
14. RLC is set if MLA or GTL causes an appropriate transition in the Remote/Local function.

TYPICAL SEQUENCES OF EVENTS FOR THE CONTROLLER

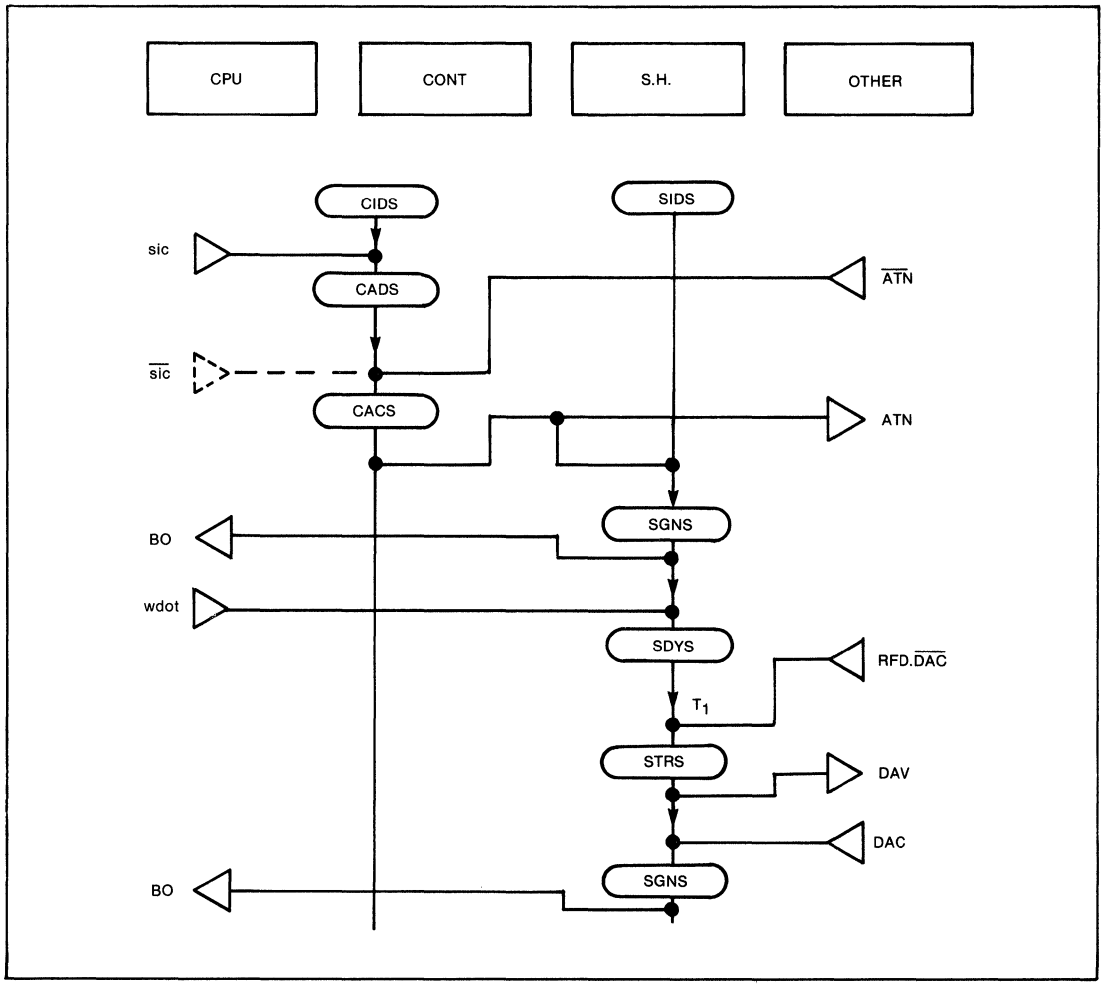


Figure 15. CONTROLLER TAKING CONTROL

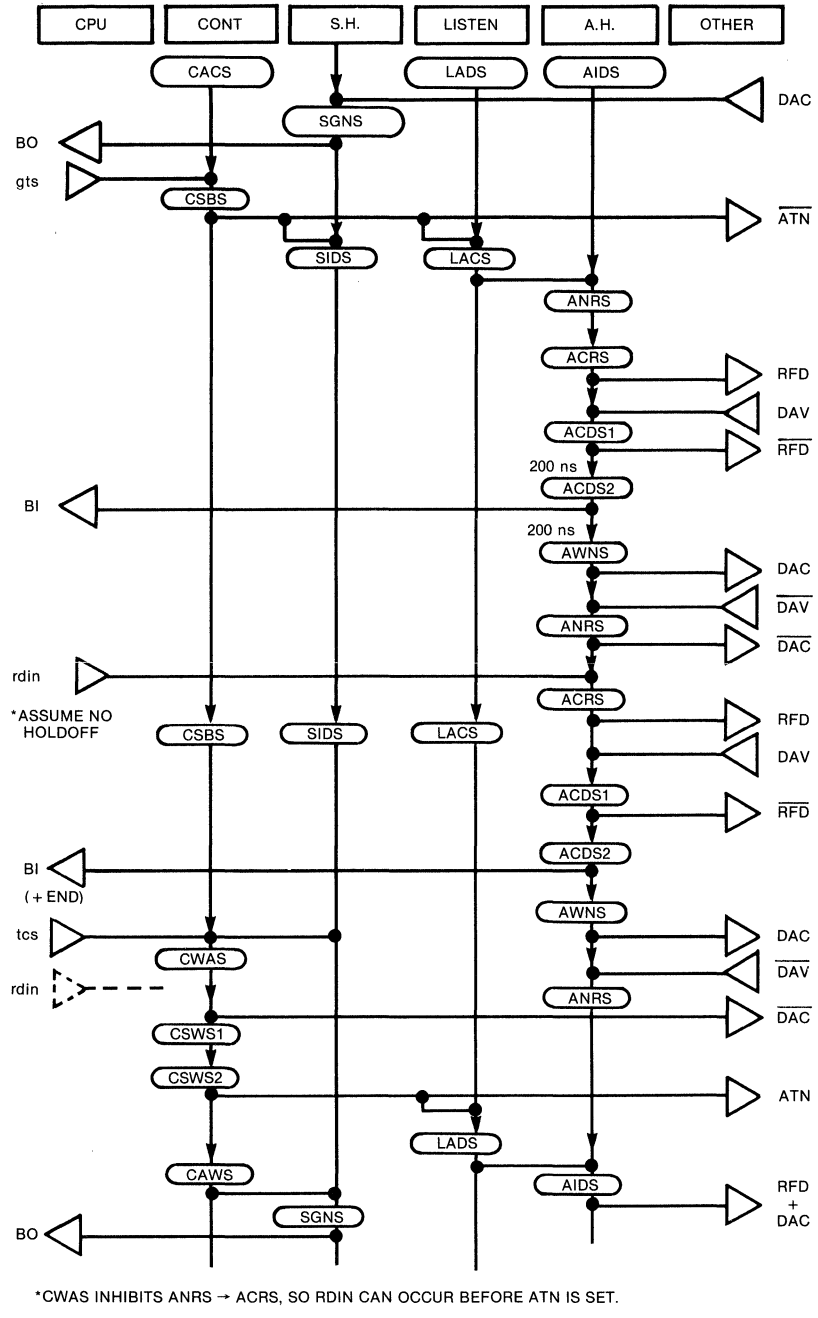
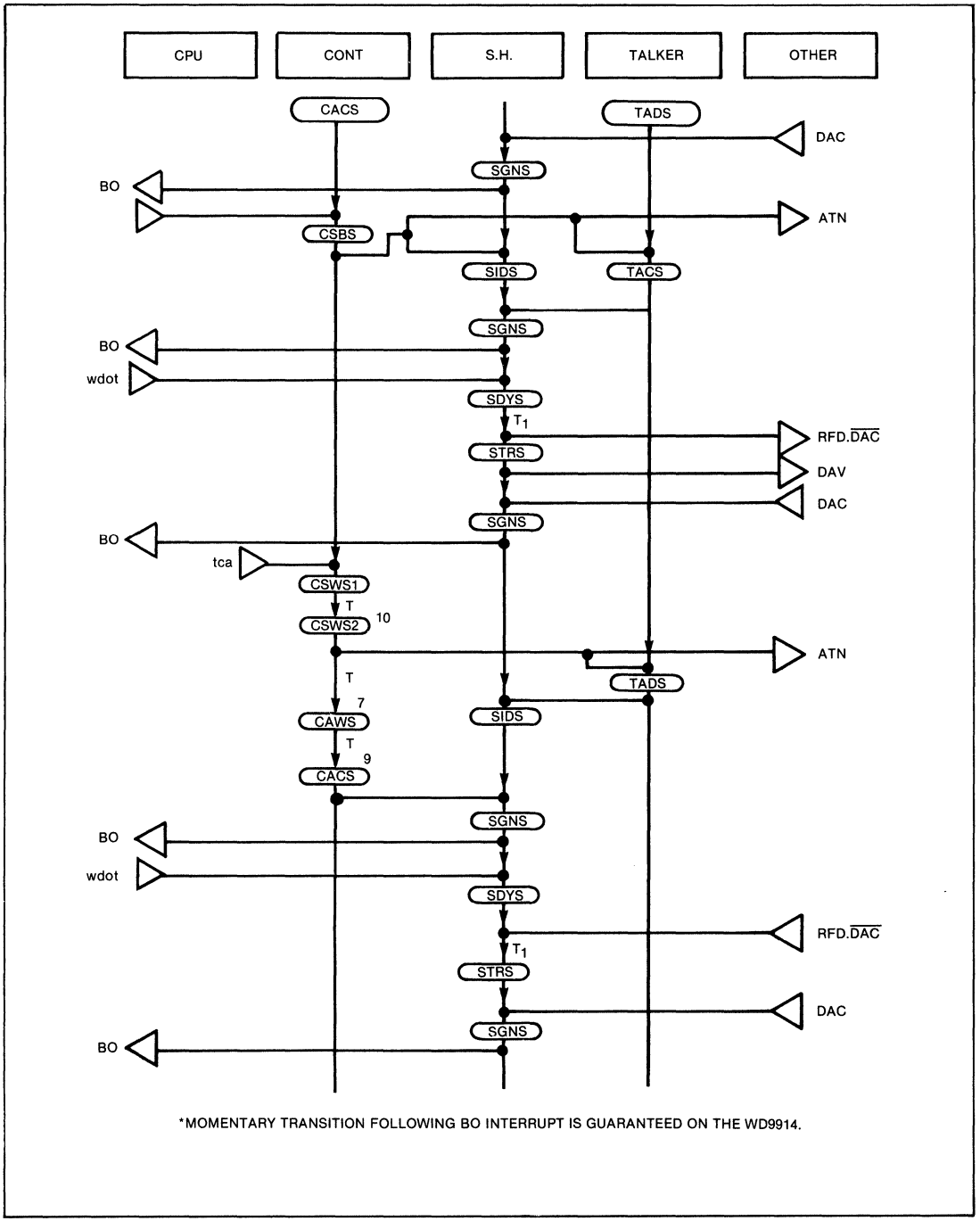


Figure 16. CONTROLLER AS A LISTENER (GOING TO STANDBY)



*MOMENTARY TRANSITION FOLLOWING BO INTERRUPT IS GUARANTEED ON THE WD9914.

Figure 17. CONTROLLER AS A TALKER (GOING TO A STANDBY)

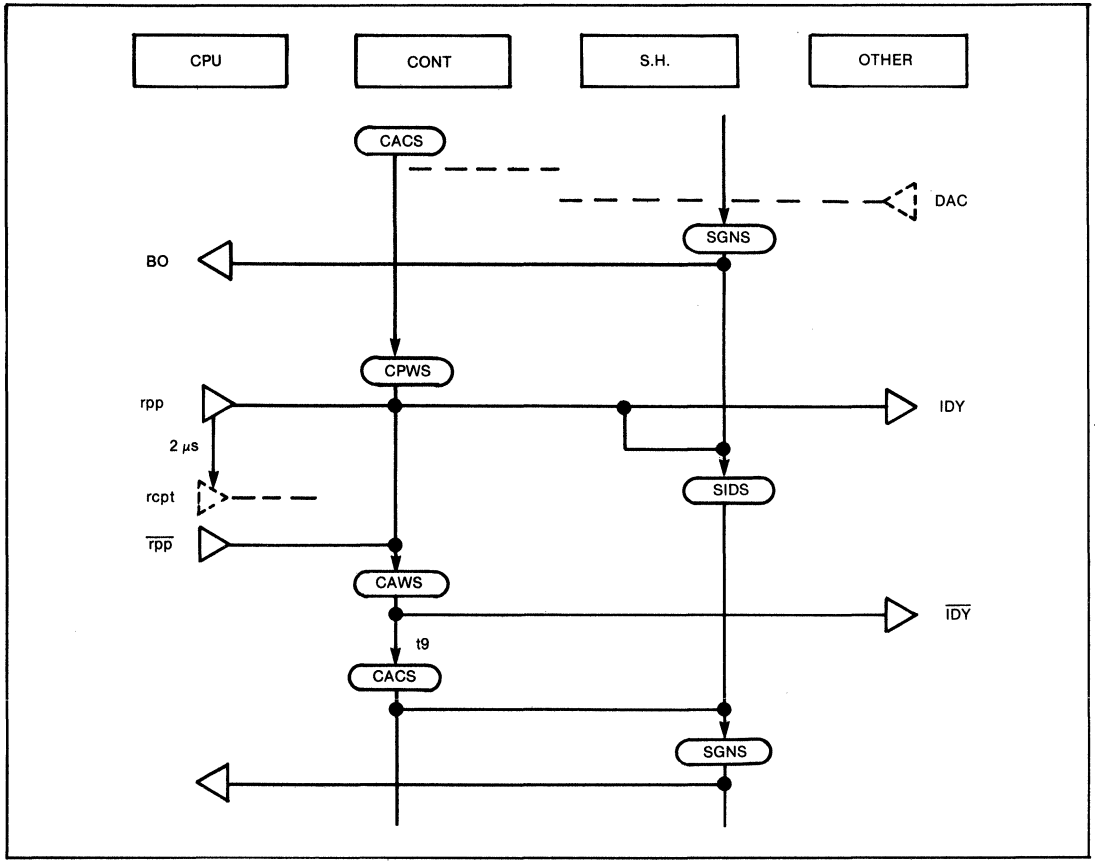


Figure 18. CONTROLLER PARALLEL POLLING

WD9914 ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (Unless otherwise noted)*

Supply Voltage, V_{CC} (see Note 1) .... −0.3V to 20V
All Input and Output Voltages ..... −0.3V to 20V
Continuous Power Dissipation ..... 0.8 W
Operating Free-Air Temperature Range . 0°C to 70°C
Storage Temperature Range ..... −55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:
Under absolute maximum ratings voltage values are with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
Supply voltage, V_{SS}		0		V
High-level input voltage, V_{IH}	2		$V_{CC}+1$	V
Low-level input voltage, V_{IL}	V_{SS}-0.3		0.8	V
Operating free-air temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER FULL RANGE OF RECOMMENDED OPERATING CONDITIONS

	PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage Except REN,IFC,INT	$I_{OH} = -400\,\mu A$	2.4		V_{CC}	V
	$\overline{REN}$,$\overline{IFC}$ only	$I_{OH} = -100\,\mu A$	2.2		V_{CC}	V
V_{OL}	Low-level output voltage	$I_{OL} = 2$ mA	V_{SS}		0.4	V
I_I	Input current (any input)	$V_I = 2$ V to V_{CC}			±10	μA
I_{CC}	V_{CC} supply current				150	mA
C_i	Input capacitance (any input)	f = 1 MHz, unmeasured pins at 0 V			15	pF

† All typical values are at $T_A = 25°C$ and nominal voltage.

TIMING CHARACTERISTICS AND REQUIREMENTS

Timing characteristics and requirements are given in the following and relevant timing diagrams are shown in Figure 10 through Figure 27.

Clock and Host Interface Timing Requirements Over Full Range of Operating Conditions

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{c(0)}$	Clock cycle time	200		2000	ns
$t_{w(0H)}$	Clock high pulse width	100		1955	ns
$t_{w(0L)}$	Clock low pulse width	45			ns
$t_{su(AD)}$	Address setup time	0			ns
$t_{su(DBIN)}$	DBIN setup time	0			ns
$t_{su(CE)}$	$\overline{CE}$ setup time	100			ns
$t_{su(WE)}$	$\overline{WE}$ setup time	0			ns
$t_{w(WE)}$	$\overline{WE}$ low pulse width	80			ns
$t_{su(DA)}$	Data setup time	60			ns
$t_{h(DA)}$	Data hold time	0			ns
$t_{h(AD)}$	Address hold time	0			ns
$t_{h(DBIN)}$	DBIN hold time	0			ns
$t_{h(CE)}$	$\overline{CE}$ hold time	80			ns
$t_{su(GR)}$	$\overline{ACCGR}$ setup time	100			ns
$t_{h(GR)}$	$\overline{ACCGR}$ hold time	80			ns

Host Interface Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	MIN	TYP	MAX	UNIT
$t_{a(CE)}$	Access time from $\overline{CE}$			150	ns
$t_{a(DBIN)}$	Access time from DBIN			150	ns
$t_{su(AD)}$	Address setup time to $\overline{CE}$	0			ns
$t_{z(DBIN)}$	Hi-Z time from DBIN		50	100	ns
$t_{z(CE)}$	Hi-Z time from $\overline{CE}$		50	100	ns
$t_{a(GR)}$	Access time from $\overline{ACCGR}$			150	ns
$t_{z(GR)}$	Hi-Z time from $\overline{ACCGR}$		50	100	ns
$t_{d(GR/RQ)}$	Delay of $\overline{ACCRQ}$ high from $\overline{ACCGR}$			100	ns

Source Handshake Timing Characteristics Over Full Range of Operating Conditions (see Note 1)

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay of DAV true from end of write operation to data out register	Normal T_1 (see Note 2)	12(0)↑	12(0)↑ + 310	ns
		Short T_1 (see Note 2)	8(0)↑	8(0)↑ + 310	ns
		Very short T_1 (see Note 2)	4(0)↑	4(0)↑ + 310	ns
t_{d2}	Delay of valid GPIB data lines from end of write cycle			140	ns
t_{d3}	Delay of BO interrupt from DAC true	BO interrupt unmasked		300	ns
t_{d4}	Delay of $\overline{\text{ACCRQ}}$ DAC true			300	ns
t_{d5}	Delay of DAV false from DAC true			160	ns

NOTES:

1. The timing of the source handshake is the same whether ATN is true or false, i.e., whether the device is in TACS, CACS, or SPAS.
2. A very short bus settling time (T_1) occurs on the second and subsequent data byte sent when ATN is false if the 'vstd1' feature is set. A slightly longer bus settling time takes place if 'std1' is set unless there is a very short bus settling time. In all other instances, a normal bus settling time occurs.

Acceptor Handshake Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d6}	Delay of BI interrupt from DAV true	BI interrupt unmarked ATN = false device is in LACS	2(0)↑	2(0)↑ + 415	ns
t_{d7}	Delay of $\overline{\text{ACCRQ}}$ from DAV true	ATN = false device is in LACS	2(0)↑	2(0)↑ + 290	ns
t_{d8}	Delay of DNAC false from DAV true	ATN = false device is in LACS	3(0)↑	3(0)↑ + 445	ns
t_{d9}	Delay of NRFD false from end of read operation of Data In register	ATN = false device is in LACS		220	ns
t_{d10}	Delay of interface message interrupt from DAV true	ATN = true device not in CACS all interface message interrupts (except UNO)	2(0)↑	2(0)↑ + 415	ns
		UNO interrupt only	5(0)↑	5(0)↑ + 415	ns
t_{d11}	Delay of NDAC false from DAV true	ATN = true device not in CACS no DAC holdoff	7(0)↑	7(0)↑ + 415	ns
t_{d12}	Delay of NDAC false from end of write operation			230	ns
t_{d13}	Delay of NRFD false from DAV false	ATN = true device not in CACS		180	ns

ATN, EOI, and IFC Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay of NDAC true from ATN true	Device is not in CACS		195	ns
t_{d15}	Delay of TE high from EOI true	Device is not in CACS		125	ns
t_{d16}	Delay of valid data from EOI true	Device is not in CACS		140	ns
t_{d17}	Delay of TE low from EOI false	Device is not in CACS		125	ns
t_{d18}	Delay of NRFD true from ATN false	Device is in LADS/LACS		140	ns
t_{d19}	Response time to IFC		$16t_{c(0)}$	$30t_{c(0)}$	ns

Controller Timing Characteristics Over Full Range of Operating Conditions

	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
t_{d20}	Delay of ATN true from end of t_{ca} aux command		$8t_{c(0)}$	$10(0)\dagger + 220$	ns
t_{d21}	Delay of BO interrupt from end of t_{ca} aux command		$18t_{c(0)}$	$22(0)\dagger + 415$	ns
t_{d22}	Delay of ATN true from end of t_{cs} aux command	BO unmasked device is in ANRS	$8t_{c(0)}$	$10(0)\dagger + 220$	ns
t_{d23}	Delay of BO interrupt from end of t_{cs} aux command	BO unmasked device is in ANRS	$18t_{c(0)}$	$22(0)\dagger + 415$	ns
t_{d24}	Delay of EOI true from r_{pp} aux command set			230	ns
t_{d25}	Delay of EOI false from r_{pp} aux command cleared			230	ns
t_{d26}	Delay of EOI from r_{pp} aux command cleared	BO unmasked	$8t_{c(0)}$	$10(0)\dagger + 415$	ns
t_{d27}	Delay of ATN false from sts aux command	Device is not in SDYS or STRS		210	ns

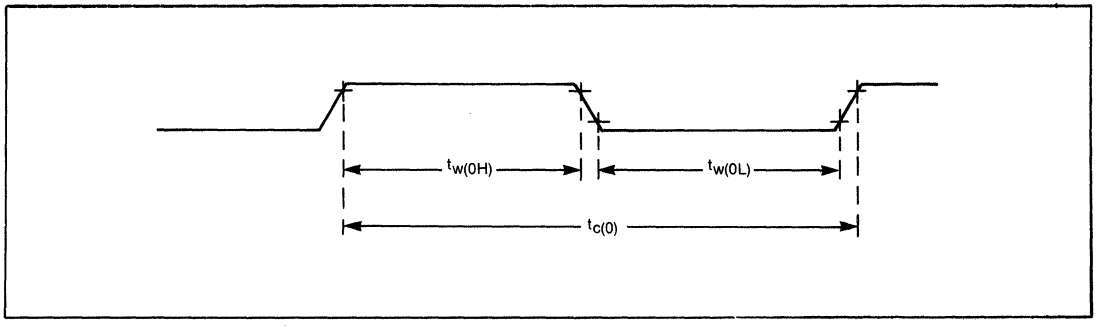


Figure 19. WD9914 CLOCK CYCLE TIMING

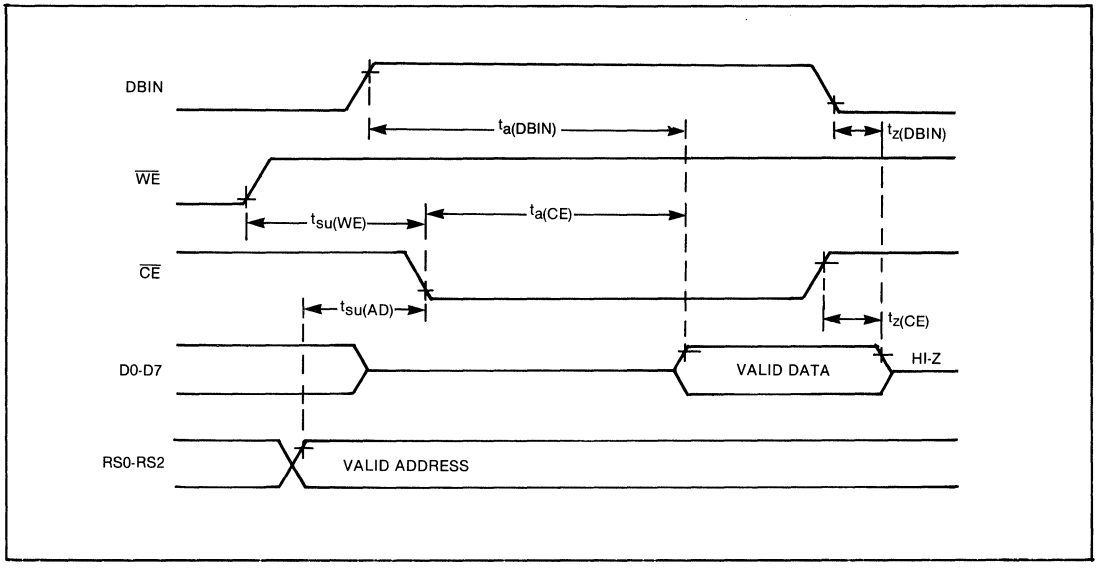
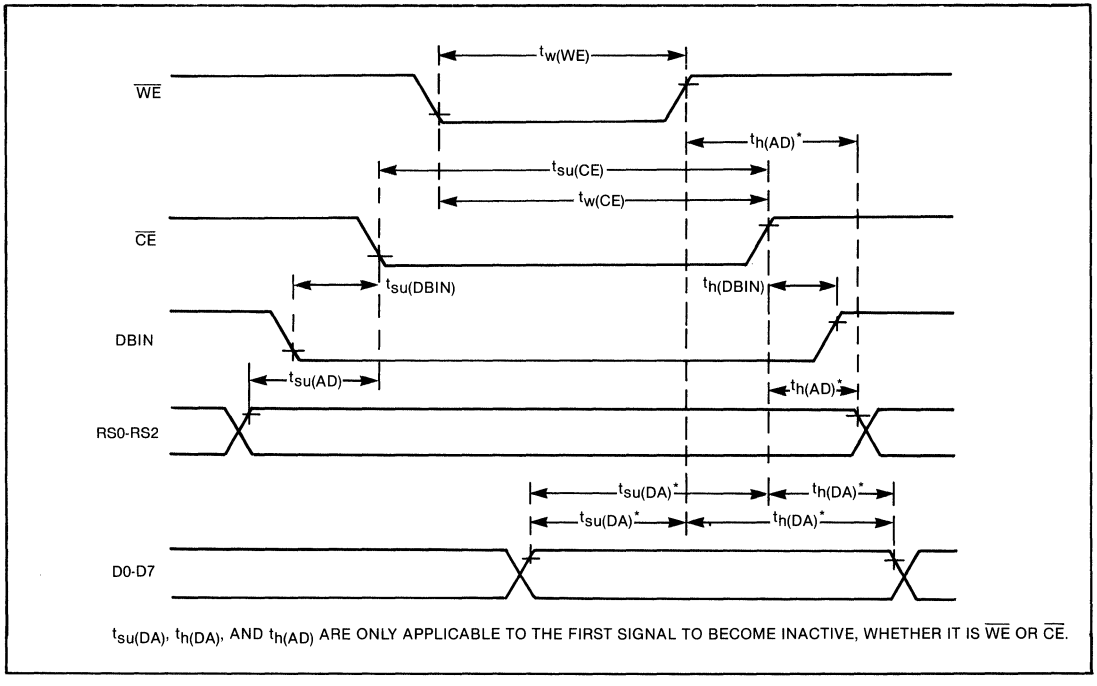
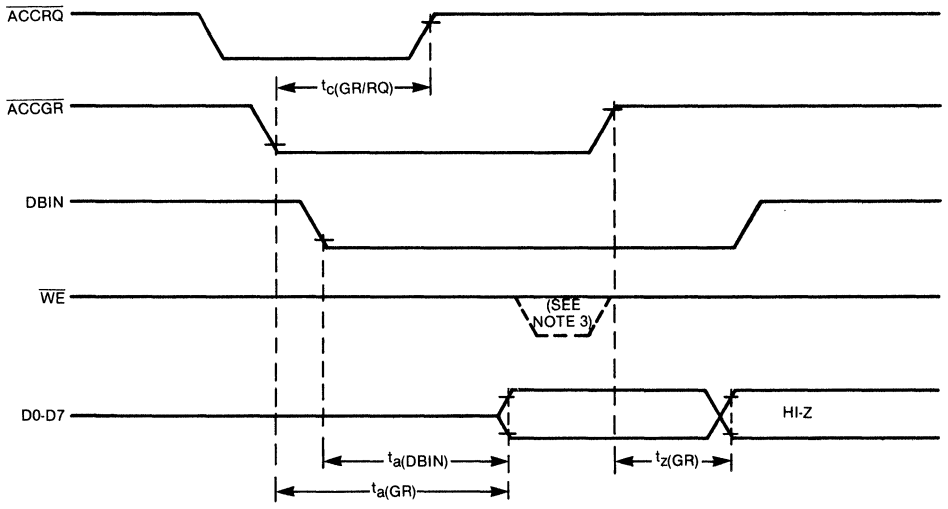


Figure 20. WD9914 READ CYCLE TIMING



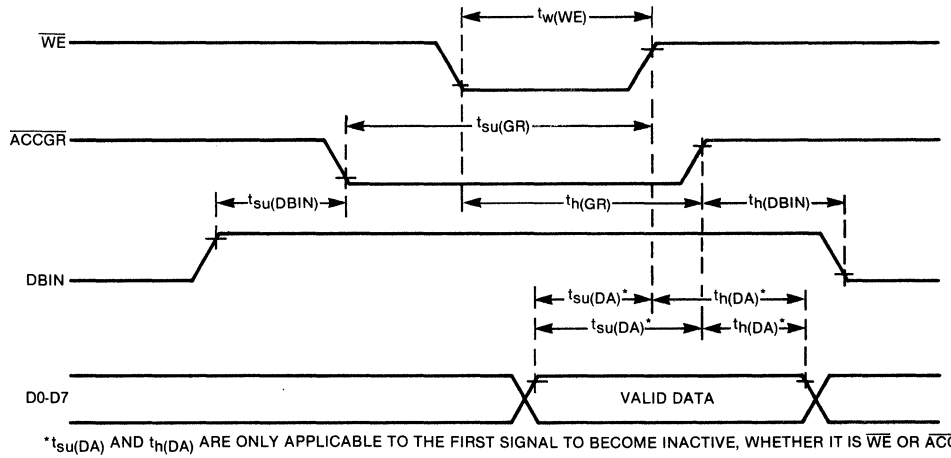
$t_{su(DA)}$, $t_{h(DA)}$, AND $t_{h(AD)}$ ARE ONLY APPLICABLE TO THE FIRST SIGNAL TO BECOME INACTIVE, WHETHER IT IS $\overline{WE}$ OR $\overline{CE}$.

Figure 21. WD9914 WRITE CYCLE TIMING



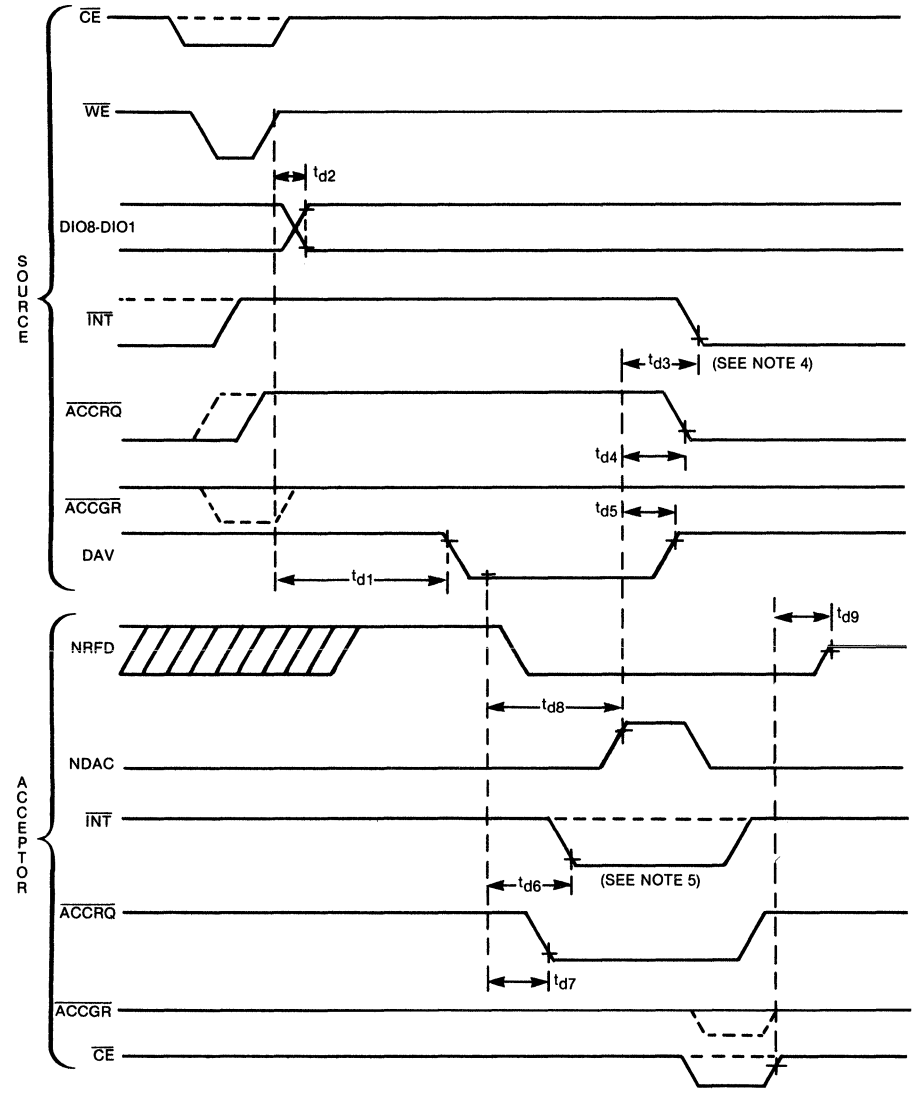
NOTE 3: A WRITE ENABLE PULSE MAY OCCUR IN A DMA READ OPERATION. A WRITE ENABLE PULSE MAY THEREFORE BE PROVIDED FOR SYSTEM MEMORY AND NEED NOT BE SUPPRESSED AT THE WD9914.

Figure 22. WD9914 DMA READ OPERATION



*$t_{su(DA)}$ AND $t_{h(DA)}$ ARE ONLY APPLICABLE TO THE FIRST SIGNAL TO BECOME INACTIVE, WHETHER IT IS $\overline{WE}$ OR $\overline{ACCGR}$.

Figure 23. WD9914 DMA WRITE OPERATION

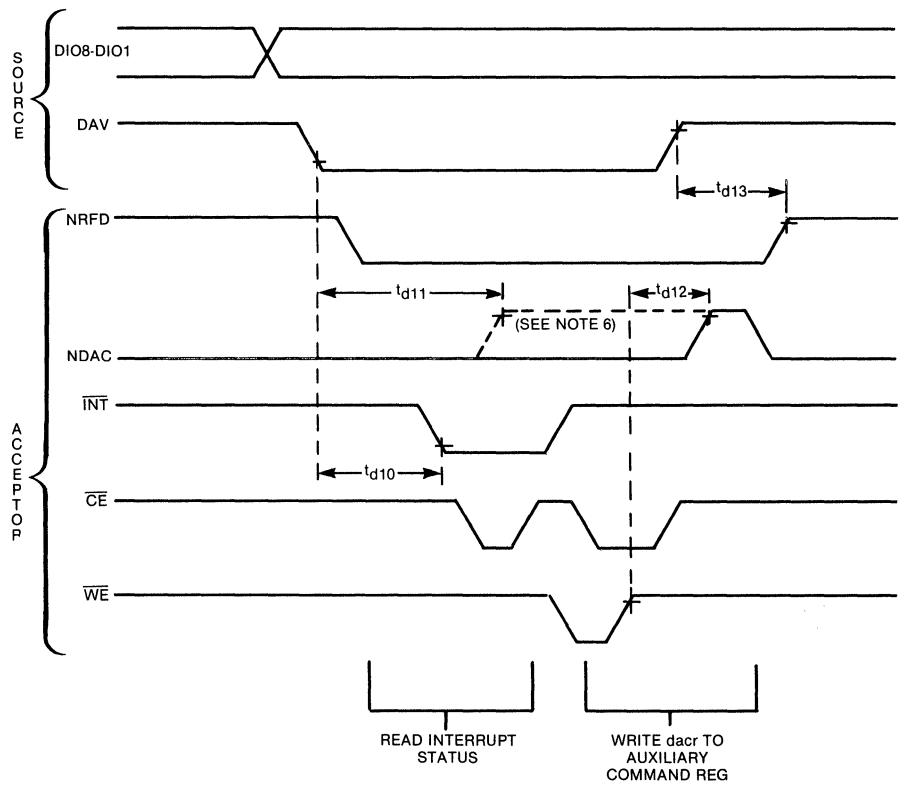


NOTES:

4: THE INTERRUPT LINE IS TAKEN LOW BY A BO INTERRUPT.

5: THE INTERRUPT LINE IS TAKEN LOW BY A BI INTERRUPT.

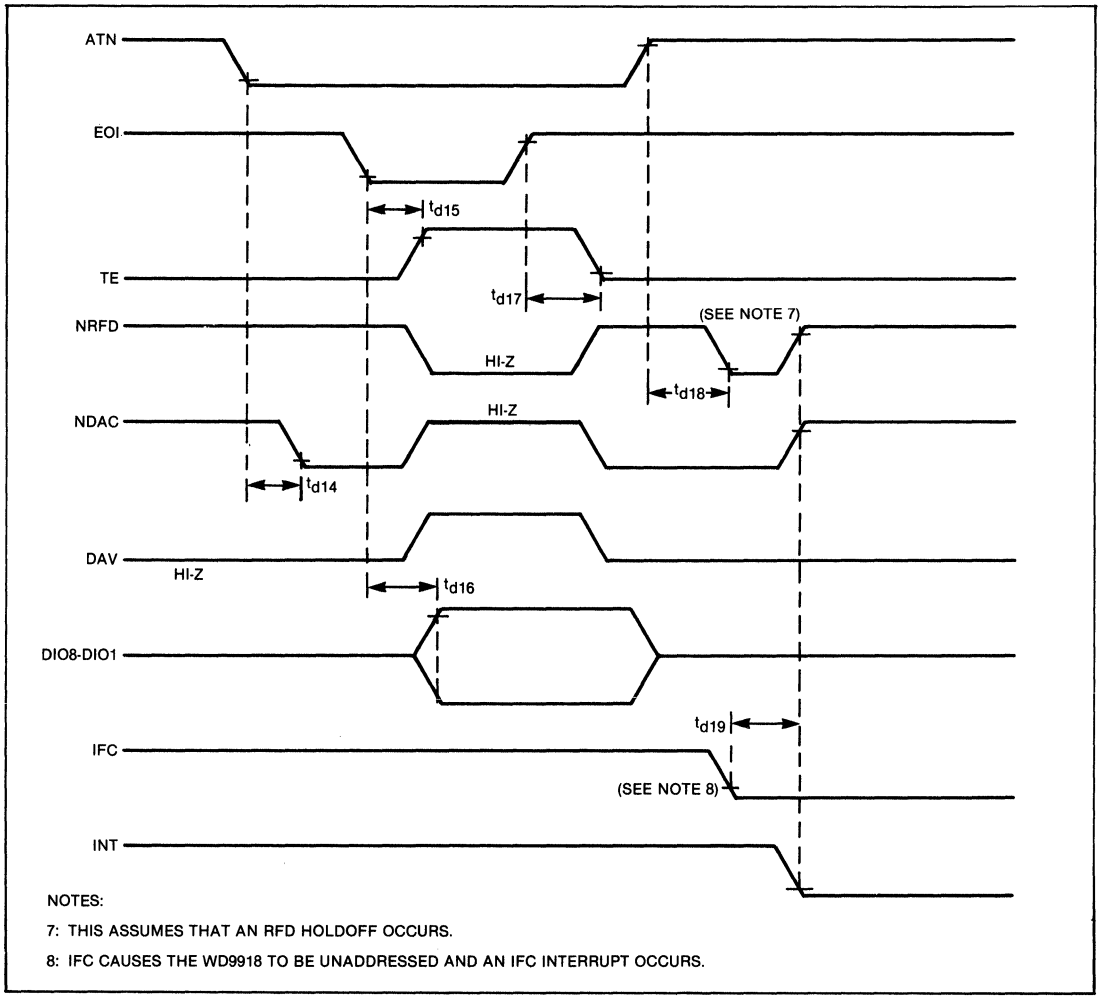
Figure 24. WD9914 SOURCE AND ACCEPTOR HANDSHAKE TIMING(S)



NOTES:

6: THE BROKEN LINE SHOWS THE WAVEFORM IF THERE IS NO DAC HOLDOFF. THE SOLID LINES ASSUME THERE IS A DAC HOLDOFF.

Figure 25. WD9914 ACCEPTOR HANDSHAKE TIMING "ATN" TRUE

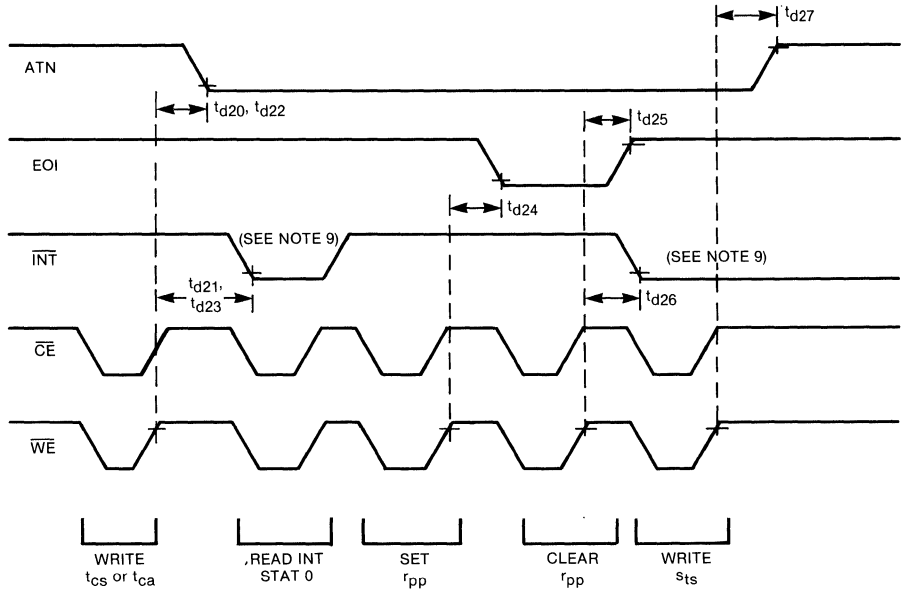


NOTES:

7: THIS ASSUMES THAT AN RFD HOLDOFF OCCURS.

8: IFC CAUSES THE WD9918 TO BE UNADDRESSED AND AN IFC INTERRUPT OCCURS.

Figure 26. WD9914 RESPONSE TO 'ATN' AND 'EOI'



NOTE: 9: A BD INTERRUPT OCCURS AS THE WD9914 ENTERS CACS.

Figure 27. WD9914 CONTROLLER TIMING

See page 383 for ordering information.

Printed in U.S.A.

ORDERING INFORMATION

OBSOLETE PACKAGE DESIGNATIONS

A 40 Lead DIP-Ceramic
B 40 Lead DIP-Relpak
C 24 Lead DIP-Ceramic
E 28 Lead DIP-Ceramic
F 28 Lead DIP-Relpak
L 18 Lead DIP-Ceramic
M 18 Lead DIP-Plastic (Totally Encapsulated)
P 40 Lead DIP-Plastic (Totally Encapsulated)
R 28 Lead DIP-Plastic (Totally Encapsulated)
T 48 Lead DIP-Ceramic
U 20 Lead DIP-Ceramic
V 20 Lead DIP-Plastic (Totally Encapsulated)
X Ceramic Kit
Y Plastic Kit

Example of obsolete method:
WD1943M00 Where M = Single Digit
Package Designator (M = 18 Lead Plastic)

CURRENT PACKAGE DESIGNATIONS

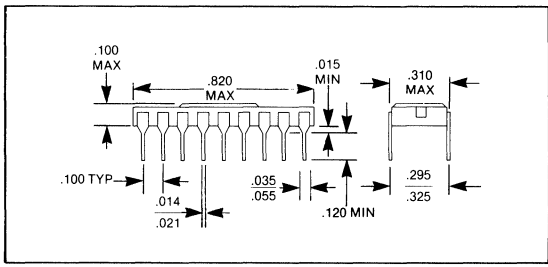
PACKAGE TYPE:		LEAD COUNT:	
A	Ceramic Side Braze	A	<14 Lead
C	Cerdip	B	14 Lead
P	Plastic (Encap)	C	16 Lead
D	Ceramic Chip Carrier-Leadless	D	18 Lead
		E	20 Lead
G	Ceramic Chip Carrier-Leaded	F	22 Lead
		G	24 Lead
H	Plastic Chip Carrier-Leadless	H	28 Lead
		L	40 Lead
J	Plastic Chip Carrier-Leaded	M	44 Lead
		N	48 Lead
		S	64 Lead
		T	68 Lead
		Z	Kit

Example of current method:
WD1943PD00 Where PD = Double Digit
Package Designator (P = Plastic and D = 18 Lead)

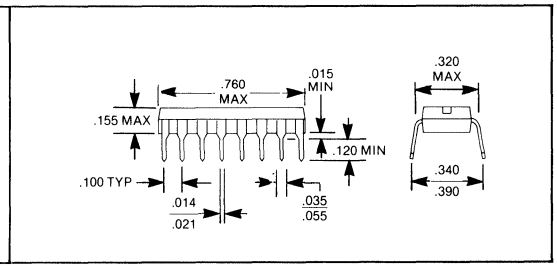
The following listing indicates the available packages for each product. The package diagrams are located on page 384.

Product	Plastic	Ceramic	CER-DIP
WD1510-00,01,02,03		AH	CH
UC1671-00	PL	AL	
TR1863-00,02,04	PL	AL	CL
TR1865-00,02,04	PL	AL	CL
WD1935-10,11,12,13	PL	AL	
WD1943-00	PD	AD	
WD1943-02	PD	AD	
WD1943-03	PD	AD	
WD1943-04	PD	AD	
WD1943-05	PD	AD	
WD1943-06	PD	AD	
WD1993-01,02,03	PH	AH	
WD2001-05,20,30	PH	AH	
WD2002-05,20,30	PL	AL	
WD2123-00	PL	AL	CL
WD2511-01,05,11		AN	
WD2840-01,05,11		AN	
WD8250-00	PL	AL	
WD8275-00,02	PL		CL
WD8276-00,02	PL		CL
WD9914-00	PL		CL

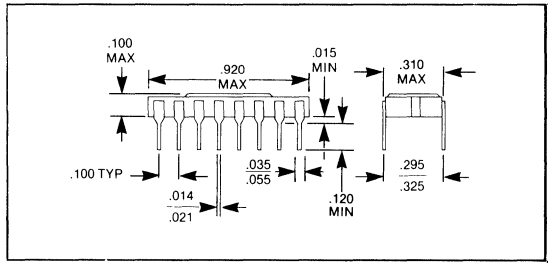
Package Diagrams



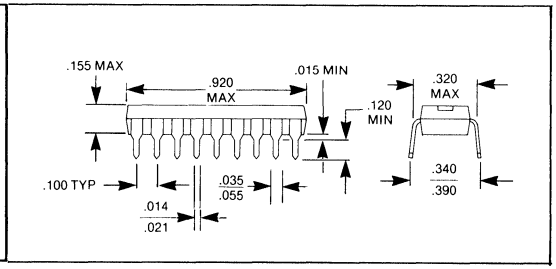
16 LEAD CERAMIC "AC"



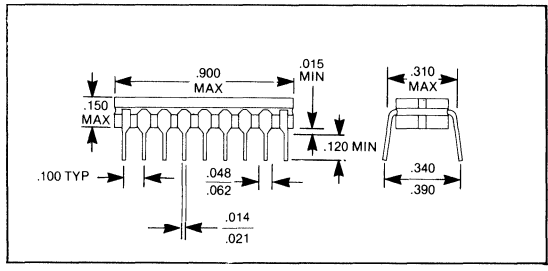
16 LEAD PLASTIC "PC"



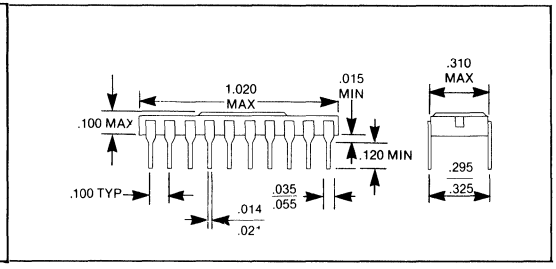
18 LEAD CERAMIC "AD"



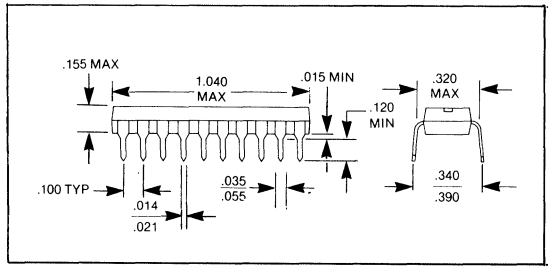
18 LEAD PLASTIC "PD"



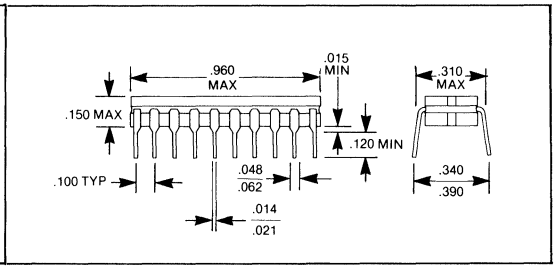
18 LEAD CERDIP "CD"



20 LEAD CERAMIC "AE"

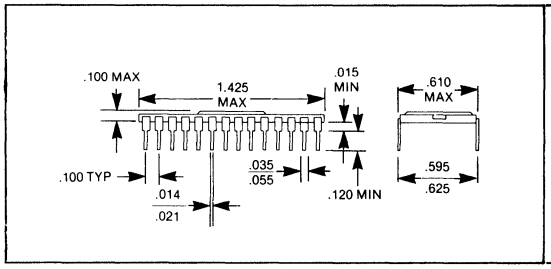


20 LEAD PLASTIC "PE"

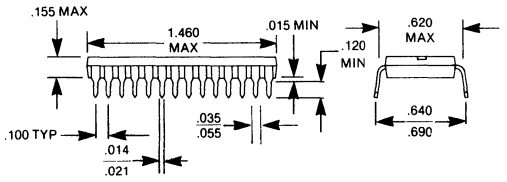


20 LEAD CERDIP "CE"

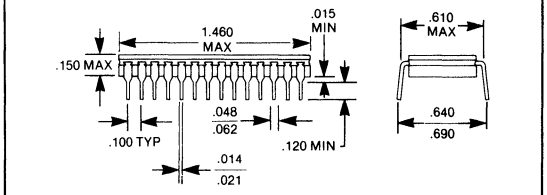
Package Diagrams



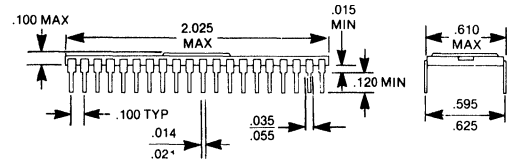
28 LEAD CERAMIC "AH"



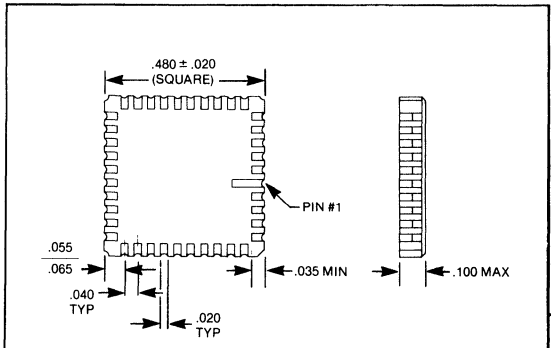
28 LEAD PLASTIC "PH"



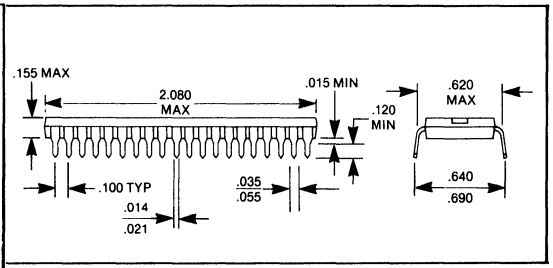
28 LEAD CERDIP "CH"



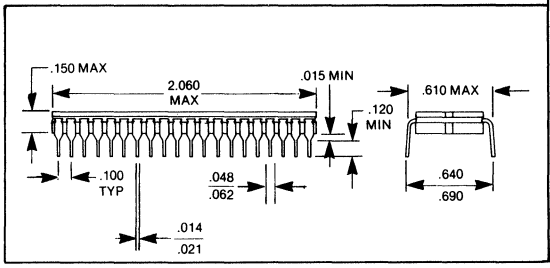
40 LEAD CERAMIC "AL"



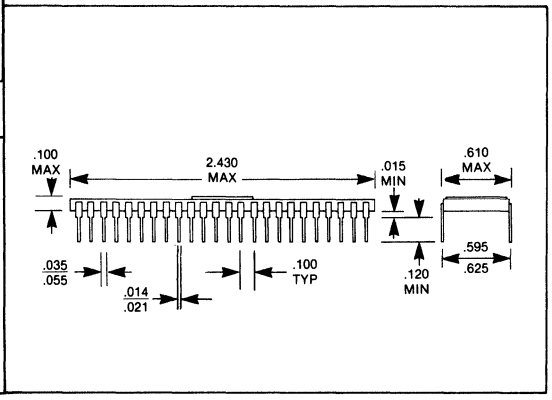
40 LEAD CERAMIC CHIP CARRIER "DL"



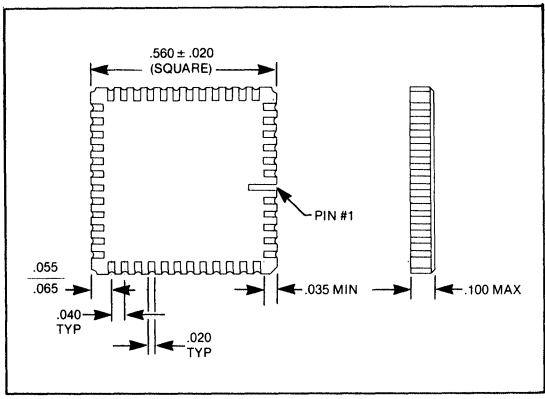
40 LEAD PLASTIC "PL"



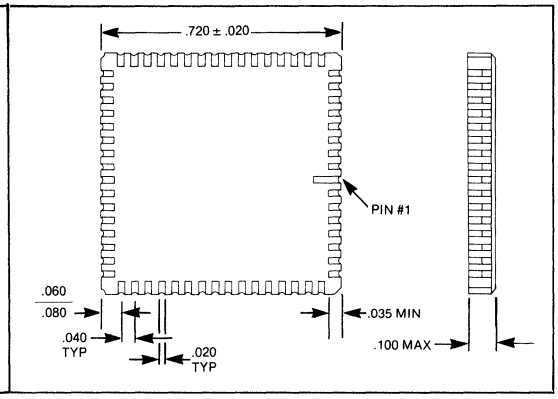
40 LEAD CERDIP "CL"



48 LEAD CERAMIC "AN"



48 LEAD CERAMIC CHIP CARRIER "DN"



64 LEAD CERAMIC CHIP CARRIER "DS"

COMMUNICATION PIN/FUNCTIONAL COMPATIBILITY GUIDE

WESTERN DIGITAL	AMI	SMC	INTEL	SSS	GI	HARRIS	INTERSIL	NTL	TI	FUJITSU
VIDEO DISPLAY PROCESSORS										
WD8275			8275							
WD8276			8276							
PROTOCOL CONTROLLERS										
TR1863	S1602	COM1863		SCR1854	AY-3-1014A	HD6402	IM64025			
TR1865	S6850	CM8018			AY-3-1015D					WB8868A
UC1671		COM1671						INS1671		
WD8250								INS8250		
WD9914									TMS9914A	
BAUD RATE GENERATOR										
WD1943		COM5016 COM8116								

STORAGE MANAGEMENT PRODUCTS

	Part Number	Technical Information	Power Requirements	Package Size	Product Description
Floppy Disk Controller Components	FD1771	Inverted data bus	+5V, −5V, +12V	40 pins	Single density, IBM compatible
	WD1770	Single chip	+5V	28 pins	FD179X functionality with built-in Digital Data Separator and Write Precompensation.
	WD1772	Single chip	+5V	28 pins	WD1770 with enhanced stepping rates of 2, 3, 5, and 6 msec.
	WD1773	Single chip	+5V	28 pins	WD1770 with software compatibility to FD179X.
	FD1791	Inverted data bus	+5V, +12V	40 pins	Single/double density, IBM compatible.
	FD1793	True data bus	+5V, +12V	40 pins	Single/double density, IBM compatible.
	FD1795	Inverted data bus	+5V, +12V	40 pins	Single/double density, double sided.
	FD1797	True data bus	+5V, +12V	40 pins	Single/double density, double sided.
	WD277X	Improved data separation	+5V	40 pins	WD279X with improved data separator.
	WD2791	Inverted data bus	+5V	40 pins	FD179X with built-in analog data separator and write precompensation, single/double density, and internal clock divide.
	WD2793	True data bus	+5V	40 pins	FD179X with built-in analog data separator and write precompensation, single/double density, and internal clock divide.
	WD2795	Inverted data bus	+5V	40 pins	FD179X with built-in analog data separator and write precompensation, single/double density, and side select out.
	WD2797	True data bus	+5V	40 pins	FD179X with built-in analog data separator and write precompensation, single/double density, and side select out.
Floppy Disk Support Devices	WD1691	8″ or 5.25″ drives	+5V	20 pins	Floppy disk data separation/write precompensation.
	WD2143	2.5 MHz	+5V	18 pins	Four phase clock generator.
	WD9216	Single chip	+5V	8 pins	Floppy disk data separator.
Winchester Disk Controller Devices	WD1010	5 MHz	+5V	40 pins	5.25″ and 8″ Winchester Controller chip.
	WD1050	Single chip	+5V	68 pins	SMD Controller.
	WD1100	Chip Series	+5V	20 pins	5.25″ and 8″ Winchester Controller chips.
	WD2010	5 MHz	+5V	40 pins	WD1010 with ECC.
Winchester Disk Support Devices	WD1011	CMOS	+5V	16 pins	Data separator device compatible with the WD1010.
	WD1012	CMOS	+5V	18 pins	Write precompensation device compatible with the WD1010.
	WD1014	Single chip	+5V	40 pins	Winchester error correction device.
	WD1015	Single chip	+5V	40 pins	Winchester Buffer Manager Control Processor.
	WD1100-13	Single chip	+5V	20 pins	ECC Support device compatible with the WD1010.
	WD1100-21	Single chip	+5V	14 pins	Winchester Buffer Manager Support Device.
Winchester Board Products	WD1000-05	Board	+5V	5.75X8	5.25″ Winchester Controller board with CRC.
	WD1002-05	Board	+5V	5.75X8	5.25″ Winchester/Floppy Controller board with ECC.
	WD1002-HDO	Board	+5V	5.75X8	5.25″ Winchester-only controller board with ECC.
	WD1002-SAS	Board	+5V	5.75X8	WD1002 with SASI interface.
	WD1002-SHD	Board	+5V	5.75X8	WD1002-SASI interface-Winchester only.
	WD1002-WX2	Board	+5V, −12V, +12V	3.85X13	WD1002 with IBM PC compatible interface.
	WD1002-MTB	Board	+5V	12X7	WD1002 w/Multibus interface.
Main Memory Devices	WD8206	Single chip	+5V	68 pins	Error detection and correction device for main memory units (static and dynamic).
	WD8207	Single chip	+5V	68 pins	Dynamic RAM controller.

Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller is prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes. Such taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products of any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against defective materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particlar purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorily required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and/or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

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