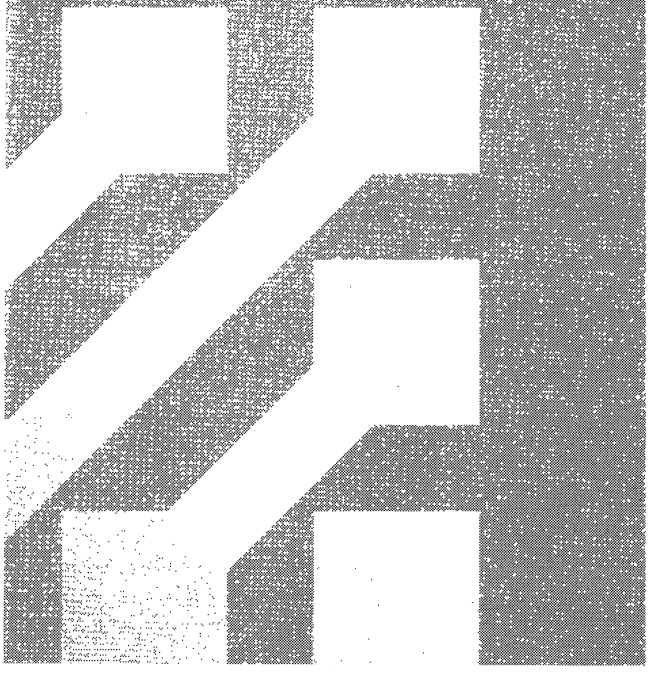
WD42C22C

Winchester Disk Subsystem

Controller Device



WESTERN DIGITAL

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1.0 INTRODUCTION

Western Digital's WD42C22C integrates a high performance, low cost Winchester formatter/controller, host interface, a buffer manager, and CRC/ECC generator/checker in a single 84-pin LSI device. Operating from a single +5V power supply, the WD42C22C is implemented in a low power CMOS design and is available in an 84-pin PLCC or PQFP (Figure 1). Figure 2 is a block diagram of the WD42C22C.

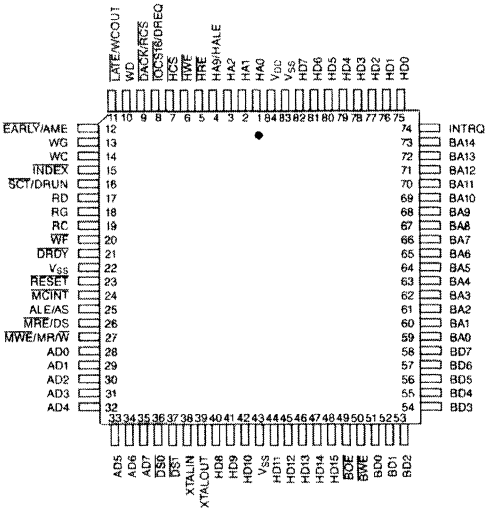

FIGURE 1. PIN DESIGNATION

1.1 FEATURES

- Enhanced host interface
  - IBM Personal Computer AT and XT port compatible
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 120 ns static RAM (SRAM)
  - Supports AT speeds up to 16 MHz, 1 wait state I/O and 0 wait state memory using 100 ns SRAM
  - Selectable DMA or programmed I/O data transfers in all host interface modes
  - Host port slave mode compatible with ALE based peripherals such as the WD33C93 SBIC
  - Host transfer rates up to 4 Mwords/sec for AT, 4 MB/sec for XT, 10 MB/sec for SCSI
  - Internal 12 mA high current drivers for direct connection to the XT or AT system bus
- Advanced buffer manager
  - Supports 1:1 interleave **without** resorting to wait states
  - Direct interface for up to 32 KB of static RAM
  - Sustained RAM bandwidth up to 10 MB/sec
  - Pipelined host and disk address counters
  - Operates as either ring or scatter-gather buffer
  - Allows full track buffering and facilitates look ahead cacheing algorithms
  - Adaptable disk controller
  - Software selectable MFM, RLL 2,7, or NRZ disk interface
  - Software selectable 56 bit ECC, 32 bit ECC, or 16 bit CRC
  - Software selectable 5, 11, or 22 bit error correction span
  - Software selectable default sector lengths of 128, 256, 512, and 1024 bytes
  - User programmable sector size up to 2048 bytes
  - Software selectable 3 bit or 4 bit head number field
  - Reads and writes at 1:1 Interleave regardless of the formatted interleave
  - 15 Mbs data transfer rate for MFM and RLL
  - 24 Mbs data transfer rate for NRZ
  - Supports hard or soft sectored formats
  - Supports "zero latency" read operations
  - Internal defect management of sector and track level alternates
  - Able to read ESDI defect list format
  - Supports sector servo schemes by disabling WRITE GATE over servo when formatting
  - Internal 48 mA drivers and Schmitt trigger input receivers for direct connection to the drive control cable
- Integrated support features
  - Programmable master/slave mode allows two Integrated Drive Electronics (IDE) disks on one connector
  - Supports both Intel-type(80xx) and Motorola-type(68xx) microcontrollers

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Internal power-qualified reset to detect low V_{DD}

- Low power sleep mode
- Available in 84-pin PLCC or 84-pin PQFP

1.2 DESCRIPTION

1.2.1 ENHANCED HOST INTERFACE

The WD42C22C host interface port directly connects to the host system bus via internal 12 mA drivers. When operating in either AT or XT mode, all host control, data, and task file address lines directly connect to the WD42C22C. Mapping the device to the desired host system I/O addresses requires external address decode logic. Integrated I/O port compatible AT and XT task file registers assure system compatibility.

To satisfy requirements for faster system bus rates and data transfers, the WD42C22C can operate in 12 MHz or 16 MHz, 1 wait state I/O channels (0 wait state memory) of 286 or 386 microprocessors. DMA or PIO data operations transfer at a rate of 4 Mwords/sec (AT mode) or 4 MB/sec (XT mode). In addition to traditional single mode DMA, burst mode DMA transfers are also available.

An alternative host mode, slave mode, allows communication between the microcontroller and a peripheral device through the host interface. The slave device transfers data to the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the WD33C93 SCSI bus interface controller (SBIC).

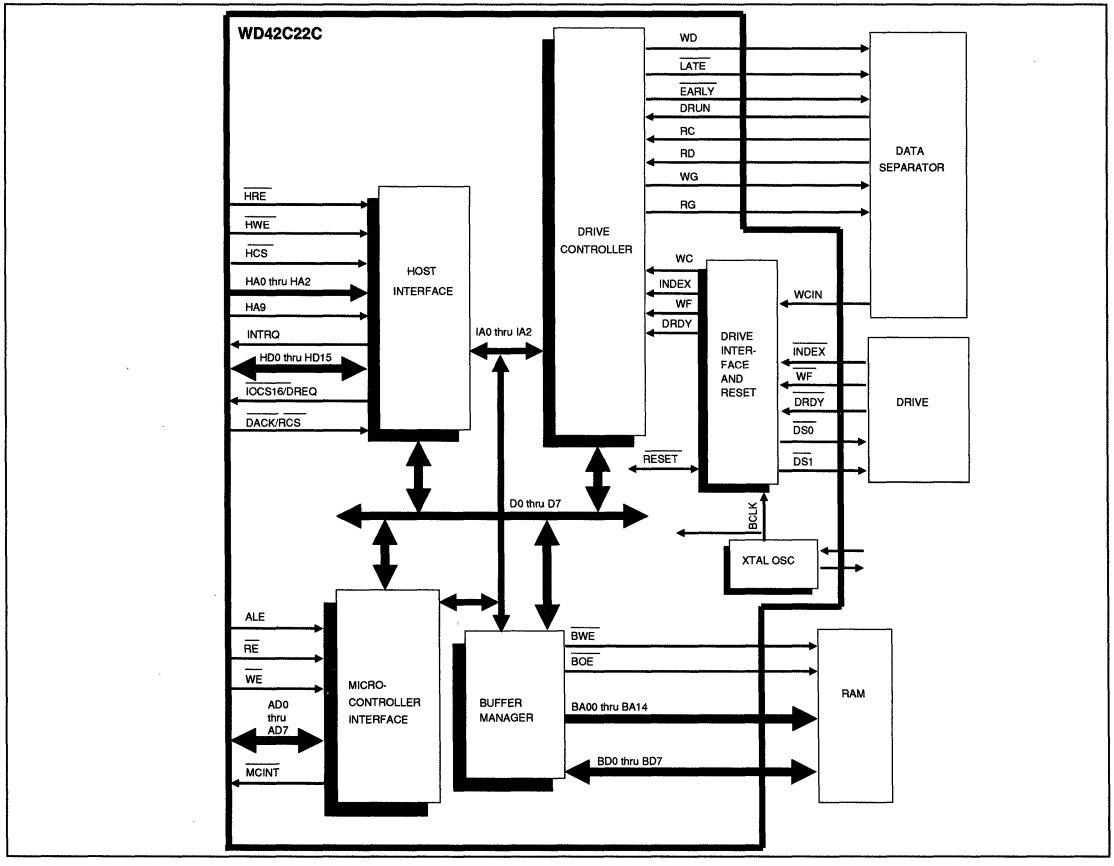

FIGURE 2. WD42C22C BLOCK DIAGRAM

1.2.2 ADVANCED BUFFER MANAGEMENT

The WD42C22C contains an advanced buffer manager satisfying the interface requirements between a byte or word wide host interface bus and a high speed serial disk interface. Optimized for the block oriented data structures of a disk controller, the WD42C22C can manage multiple sector buffers up to 32 KB. Each sector buffer can be any size to 2055 bytes. Pipelined host and disk address counters enable sustained, simultaneous transfers on each port. Sufficient RAM buffer bandwidth is available to support 1:1 interleaved 20 Mb/sec disk transfers while simultaneously performing 16-bit host transfers at a rate in excess of 3 Mwords/sec. Achieving maximum RAM bandwidth requires using 70 nsec static RAM.

The pipelined structure of the buffer manager controls the buffer RAM in either a simple ring structure or a more advanced scatter-gather structure.

1.2.3 ADAPTABLE DISK CONTROLLER

The WD42C22C's versatile design makes the device adaptable for a wide variety of disk interface operations. A designer can select from three data formats, MFM, RLL 2,7, or NRZ. Disk data rates range up to 15 Mbits/sec with MFM and RLL 2,7 encoding, while NRZ data rates range up to 24 Mbits/sec. To support varied data format requirements, the WD42C22C operates in hard or soft sectored mode with programmable sector sizes to 2048 bytes and programmable ID PLO, data PLO, and GAP lengths.

Software selectable retry algorithms and 32 or 56-bit ECC polynomials enhance data integrity. Data integrity can further be ensured through the use of the device's built-in advanced defect management. The WD42C22C can be programmed to automatically detect the presence of a previously assigned defective sector and identify the location of the alternate sector. This allows access to alternate sectors without the typical additional rotational latency associated with defect handling.

With the pipelined architecture of the buffer manager, the designer can program the disk controller to execute "zero-latency" multiple sector read operations. In this mode of operation, the WD42C22C immediately commences data transfer to the RAM buffer upon encountering the first sector on the desired track. All subsequent sectors transfer to the buffer within a single rotational period. Host transfers begin upon location of the first requested sector within the buffer. Simultaneous host and disk transfers continue until all sectors are read from the drive. Zero-latency operation makes available an entire track of data to the host within one rotational period from the time the host requested the data. This differs from traditional implementations which read the entire track within one rotational period **AFTER** the first requested sector has been located. Zero latency read operations eliminate the typical one-half rotational period average latency required to locate the first sector in full track data transfers

The WD42C22C includes an internal power qualified reset circuit for power up and power down conditions. This circuit eliminates the need for costly external circuitry that traditionally performed this function.

The WD42C22C features a multiplexed address/data bus on the microcontroller interface port and supports both Intel (80XX) and Motorola (68XX) type microcontrollers. An internal circuit automatically determines the connected microcontroller and configures the ports for direct interfacing.

Internal 48 mA drivers and Schmitt triggers input receivers provide direct connection to the drive control cable. Programmable input polarities assist in integrated drive electronics (IDE) designs.

1.2.4 FLEXIBILITY OF APPLICATION

As a result of its level of integration, a designer can create a wide variety of products. In addition to traditional stand alone Winchester controller boards, the WD42C22C is ideal for multi-function boards, direct system motherboards, and IDE applications. Special design considerations within the WD42C22C facilitate these applications.

1.2.5 TYPICAL APPLICATION

With an external microcontroller, buffer RAM, and a data separator such as the WD10C22B, the WD42C22C forms the basis of a Winchester disk controller product. For AT and XT applications, direct interfacing is available to the system bus. In

these applications, the WD42C22C requires external address decoding to select the primary and secondary I/O address range of the WD42C22C. Other bus interfaces are supported via auxiliary bus controllers such as the WD33C93A SCSI Bus Interface Controller.

For ST506 (MFM) and ST412HP (RLL) applications, the WD42C22C directly connects to the WD10C22 data separator. (Like the WD42C22C, the WD10C22B supports both MFM and RLL encoding methods.) An external microcontroller implements interface specific control lines, e.g. the ST506's $\overline{\text{STEP}}$ and $\overline{\text{DIRECTION}}$ signals. For ESDI applications, the WD42C22C operates in NRZ mode.

1.2.6 PIN DESCRIPTIONS

This section lists the pin number, signal name, and function for all the WD42C22C's pins. The pin descriptions are arranged by functions. Table 1 describes the pin designations for the host interface. Table 2 describes the pin designations for the local microcontroller interface. Table 3 describes the pin designations for the buffer interface. Table 4 describes the pin designations for the drive interface.

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
1	HA0	HOST ADDRESS 0	I	Schmitt-triggered input. These four inputs are used to address the internal registers. Internal decoding of these address signals is a function of the AT/XT and HSMB mode bits. Port compatibility is maintained for both the AT and XT. In slave host mode HALE is used by the peripheral device to latch the address from HD0 through HD7.
2	HA1	HOST ADDRESS 1	I	
3	HA2	HOST ADDRESS 2	I	
4	HA9/ HALE	HOST ADDRESS 9/ HOST ALE	I/O	
5	$\overline{\text{HRE}}$	HOST READ ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HRE}}$ is asserted by the AT or XT with HCS to read an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It can also be asserted by the slave peripheral in DMA mode.
6	$\overline{\text{HWE}}$	HOST WRITE ENABLE	I/O	Schmitt-triggered input. $\overline{\text{HWE}}$ is asserted by the AT or XT with HCS to write an internal register or the FIFO. In slave mode, $\overline{\text{HRE}}$ is asserted when $\overline{\text{MRE}}$ is asserted. It is also asserted by the slave peripheral in DMA mode.
7	$\overline{\text{HCS}}$	HOST CHIP SELECT	I/O	Schmitt-triggered input. $\overline{\text{HCS}}$ should be decoded from the AT or XT address bus and is used to qualify $\overline{\text{HRE}}$ and $\overline{\text{HWE}}$ for host accesses. In slave mode, $\overline{\text{HCS}}$ is asserted when the local microcontroller is accessing the slave device address space.
8	$\overline{\text{IOCS16}}$/ DREQ	I/O CHIP SELECT 16/ DMA REQUEST	O	This output is programmable to function as the AT bus signal $\overline{\text{IOCS16}}$ when the PIO mode is selected or as a DMA Request signal (DREQ) in the DMA mode. This output is tri-stated at power-up and remains tri-stated until the interface mode is set by the local microcontroller. $\overline{\text{IOCS16}}$ is an open-drain ouput. DREQ is a tri-state output.
9	$\overline{\text{DACK}}$/ RCS	DMA ACKNOWLEDGE/ RAM CHIP SELECT	I	Schmitt-triggered input. $\overline{\text{DACK}}$ is asserted by the host in response to the DREQ signal assertion in order to complete the DMA handshake. $\overline{\text{RCS}}$ is used in slave mode to qualify host data transfers to/from the FIFO.

TABLE 1. HOST INTERFACE PIN DESCRIPTION

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PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
23	$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	I/O	Open-drain output and Schmitt input, can be wire-ORed with an external reset. The WD42C22C resets all logic except the Task File when this input is asserted. On power-up, or when requested by the host, this output is asserted.
75 thru 82, 40, 41, 42, 44 thru 48	HD0 thru HD15	HOST DATA 0 thru HOST DATA 15	I/O	Schmitt-triggered inputs. These 16 pins are used during host 16-bit data transfers, and the lower eight bits (HD0-HD7) are used for byte-wide host data transfers as well as all command and status information transfers.
74	INTRQ	INTERRUPT REQUEST	I/O	INTRQ indicates to the AT or XT that a data blocktransfer is requested or a command has been completed. In slave host mode INTRQ is asserted by the slave peripheral device.
83	V_{SS}	GROUND		Ground.
84	V_{DD}	+5V		+5V

TABLE 1. HOST INTERFACE PIN DESCRIPTION (CONT'D)

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
22	V_{SS}	GROUND		Ground.
24	$\overline{MCINT}$	$\overline{\mu CONTROLER\ INTERRUPT}$	O	This output is used as an interrupt signal in order to alert the local microcontroller it is necessary to check command parameters or status. For the XT mode, $\overline{MCINT}$ is asserted when the controller is selected.
25	ALE/AS	ADDRESS LATCH ENABLE/ ADDRESS STROBE	I	Schmitt-triggered input. ALE is used to latch the lower eight address bits from the multiplexed address/data lines (AD7-AD0). AS is used for this function when tied to a Motorola type microcontroller.
26	$\overline{MRE}$/DS	$\overline{\mu CONTROLLER\ READ\ ENABLE}$ /DATA STROBE	I	Schmitt-triggered input. $\overline{MRE}$ is asserted by the local microcontroller to read an internal register or the buffer. DS is used in Motorola type microcontrollers to enable the data transfer.
27	$\overline{MWE}$/ MR/$\overline{W}$	$\overline{\mu CONTROLLER\ WRITE\ ENABLE}$/ uC READ/$\overline{WRITE}$	I	Schmitt-triggered input. $\overline{MWE}$ is asserted by the local microcontroller to write an internal register or the buffer. MR/$\overline{W}$ is used by Motorola type microcontrollers to set the direction of data transfers.
28 thru 35	AD0 thru AD7	ADDRESS/DATA 0 thru ADDRESS/DATA 7	I/O	Schmitt-triggered inputs. These multiplexed address/data lines are used to load the register/buffer address on the falling edge of ALE, and are used for data transfers to/from the local microcontroller.
43	V_{SS}	GROUND		Ground.

TABLE 2. LOCAL MICROCONTROLLER INTERFACE PIN DESCRIPTION

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PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
38	XTALIN	CRYSTAL INPUT	I	Crystal oscillator input. The crystal frequency is twice the buffer data rate.
39	XTALOUT	CRYSTAL OUTPUT	O	Crystal oscillator output.
49	$\overline{\text{BOE}}$	$\overline{\text{BUFFER}}$ OUTPUT ENABLE	O	$\overline{\text{BOE}}$ is asserted by the chip to read data from the external SRAM buffer.
50	$\overline{\text{BWE}}$	$\overline{\text{BUFFER}}$ WRITE ENABLE	O	$\overline{\text{BWE}}$ is asserted by the chip to write data into the external SRAM buffer.
51 thru 58	BD0 thru BD7	BUFFER DATA 0 thru BUFFER DATA 7	I/O	Schmitt-triggered. Buffer data bus, which connects directly to a static RAM.
59 thru 73	BA0 thru BA14	BUFFER ADDR 0 thru BUFFER ADDR 14	I/O	Buffer address bus, for direct connection to 32 KB of SRAM. In XT mode, also used to read jumper configuration data in Read Configuration Mode. In input mode, there is a low current internal pulldown.

TABLE 3. BUFFER INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
10	WD	WRITE DATA	O	WD is the MFM/NRZ write data written to the disk. It is shifted out at a rate determined by write clock. MFM write data should be synchronized by a D flip flop clocked at 10 MHz (for 5 Mbs operation).
11	LATE/ WCOUT	LATE/ WCOUT	O O	LATE is used along with EARLY in the Write Precompensation circuitry to control the delay of WD. In NRZ mode WCOUT is write clock out which can be used to qualify WD in an ESDI application.
12	AME/ EARLY	ADDRESS MARK ENABLE/EARLY	O	In NRZ mode, this output is the Address Mark Enable signal for an ESDI drive. In MFM or RLL mode, this output is EARLY. EARLY and LATE are used in the Write Precompensation circuitry to control the delay of WD.
13	WG	WRITE GATE	O	WG is asserted when valid data is to be written to the disk. It enables write current to the head and is immediately de-asserted if a WRITE FAULT (WF) is detected.
14	WC	WRITE CLOCK	I	A clock used internally to control WD. (Up to 10 MHz for ST412, up to 15 MHz for ESDI).
15	INDEX	INDEX	I	Schmitt-triggered INDEX input for direct connection to the drive control cable.
16	SCT/ DRUN	SECTOR/ DATA RUN	I	Schmitt-triggered input. In hard sector mode, SCT is used to indicate the start of a sector. In soft sector NRZ mode, SCT indicates Address Mark Found. In soft sector MFM or RLL mode, DRUN indicates a sequence of MFM or RLL '0's or a sequence of MFM '1's has been detected.
17	RD	READ DATA	I	RD is MFM or NRZ read data from the drive. Data and clocks are separated internally for MFM data.
18	RG	READ GATE	O	RG is asserted to initiate a search for an address mark. It remains asserted until the end of the ID or data field.

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION

PIN NUMBER	MNEMONIC	SIGNAL NAME	I/O	FUNCTION
19	RC	READ CLOCK	I	RC is typically generated from an oscillator phase-locked to the read data.
20	$\overline{WF}$	$\overline{WRITE\ FAULT}$	I	Schmitt-triggered. $\overline{WRITE\ FAULT}$ input for direct connection to the drive control cable.
21	$\overline{DRDY}$	$\overline{DRIVE\ READY}$	I	Schmitt-triggered. $\overline{DRIVE\ READY}$ input for direct connection to the drive control cable.
36	$\overline{DS0}$	$\overline{DRIVE\ SELECT\ 0}$	O	High-current open-drain $\overline{DRIVE\ SELECT}$ outputs for direct connection to the drive control cable.
37	$\overline{DS1}$	$\overline{DRIVE\ SELECT\ 1}$	O	

TABLE 4. DRIVE INTERFACE PIN DESCRIPTION (CONT'D)

2.0 ARCHITECTURE

2.1 POWER-QUALIFIED RESET

This integrated function is used to reliably initialize flip-flops to a predictable state during the application of V_{DD}. It causes the $\overline{RESET}$ output signal to be asserted until VDD reaches a given threshold. It also forces a reset if the V_{DD} falls below a specified threshold.

2.2 DRIVE INTERFACE LOGIC

The drive interface contains high-current 48 mA drivers for direct connection of the drive select outputs to the drive control cable. Schmitt trigger input receivers connect the drive interface logic directly to the control cable inputs.

2.3 DRIVE CONTROLLER ORGANIZATION

The controller is composed of the following major sections:

- PLA Control
- CRC/ECC Logic
- MFM/RLL Decoding
- Address Mark Detector
- Buffer and DMA Control
- Task Register File

The controller is designed to operate with 2 clock inputs, READ CLOCK (RC) and WRITE CLOCK (WC). The PLA controller, processor interface, and buffer control sections use the write clock input. The clock inputs are used for MFM, RLL, or NRZ decoding. The clock frequency is 10 MHz for a 10 Mbs data rate.

The controller reads or writes disk data to a 15 Mbs rate for MFM and RLL and 24 Mbs for NRZ. The RLL implementation is a (2,7,2,4,3) code based on the IBM 3370 code. The only difference lies in the assignments of the code words to the 7 different data streams possible. Error propagation for a single bit error is limited to 4 bits.

When programmed in the NRZ mode, the WD42C22C qualifies NRZ disk data using the Sector / Address Mark Detect signal, and also modifies the RG and WG signals to meet ESDI specifications.

In all modes, the length of the PLO sync and gap fields are software programmable. The ID PLO sync field length, the Gap1/Gap3 length, the Gap1/Gap3 data bytes and the ID CRC pad bytes are programmable during the format command. The data PLO sync field length and the data CRC/ECC pad bytes are programmable during the Write command.

Figure 3 is a block diagram of the drive controller section of the WD42C22C.

2.4 PROGRAMMABLE LOGIC ARRAY (PLA) CONTROLLER

The Programmabla Logic Array (PLA) controller interprets commands, e.g. write, read format, etc. This circuitry's operation is synchronized with the WC input. The PLA controller is started when a command is written into the command register. It generates control signals and operates in a hand-

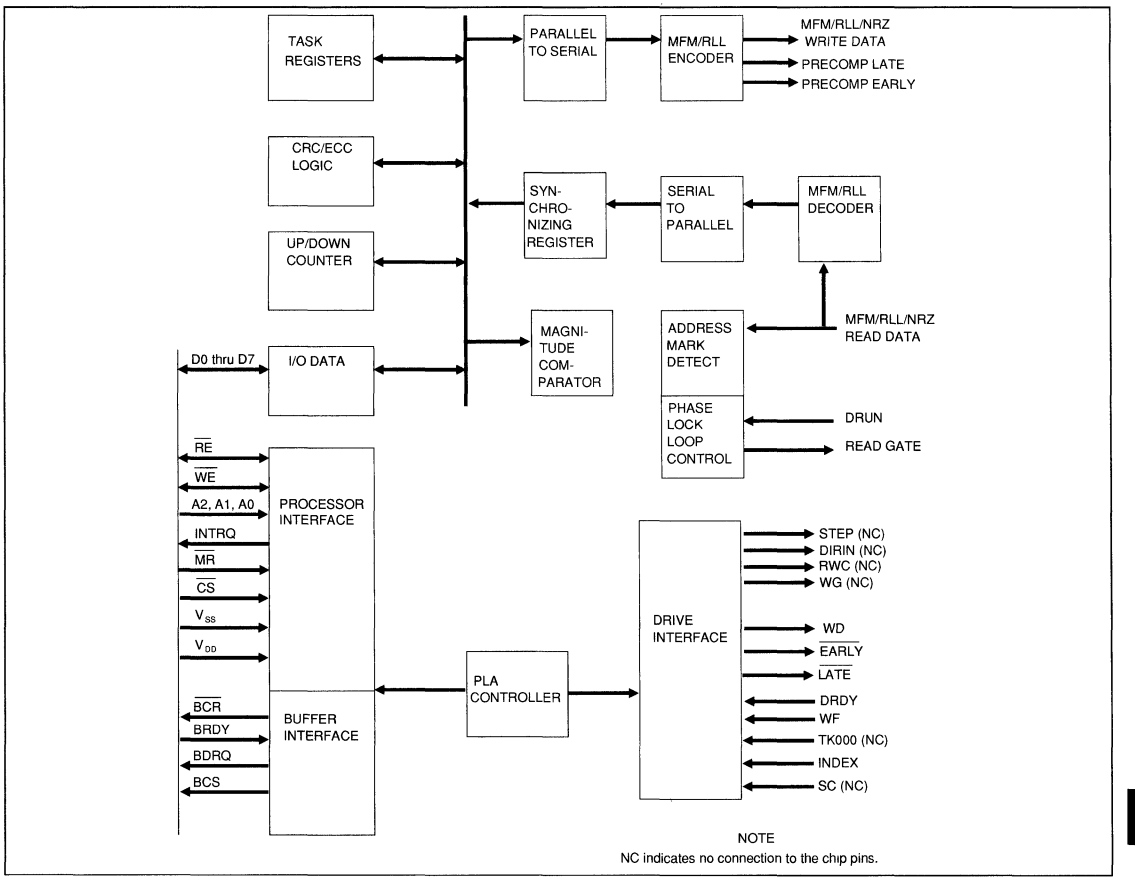

FIGURE 3. DRIVE CONTROLLER BLOCK DIAGRAM

shake mode when communicating with the MFM/RLL decoding block. The MFM/RLL decoding block uses the RC input which may be asynchronous to WC.

2.5 MAGNITUDE COMPARATOR

An 11-bit magnitude comparator calculated drive step direction and number of step pulses between present cylinder position and desired position in earlier Winchester controller versions. This comparator is **not** used in the WD42C22C. A separate high speed equivalence comparator is used to compare ID field bytes when searching for a sector ID field.

2.6 CRC/ECC GENERATOR AND CHECKER

The CRC/ECC generator computes and checks the cyclic redundancy check characters appended to the ID and data fields written on the disk. The CRC mode of operation, defined by the SDH register (bit 7 set to 0) provides a means of verifying the accuracy of the data read from the disk but does not attempt to correct it. (Bit 7 of the SDH register will not implement CRC mode for data fields when RLL mode is selected.) The CRC polynomial used is:

$$X^{16} + X^{12} + X^5 + 1$$

The CRC register is preset to all ones before computation starts.

If the CRC character being generated while reading the data does not equal the one previously written, an error exists. If there is a CRC failure in the ID field, an ID not found is indicated by setting bit 4 of the error register. If the failure is in the data field, bit 6 of the error register is set.

A 32 bit or 56 bit ECC polynomial may be selected instead of the CRC polynomial for the data field. The CRC/ECC selection is controller by bit 7 of the SDH register when the controller is in MFM or NRZ modes. CRC is selected when bit 7 of the SDH register is 0 in MFM or NRZ modes. ECC is selected when bit 7 of the SDH register is 1 in MFM or NRZ modes. Bit 2 in the set parameter command selects either the 32 bit or 56 bit polynomial. RLL mode defaults to the 56 bit polynomial. The CRC or 32 bit ECC options are **not** usable in RLL mode.

The ECC mode of operation (SDH bit 7 = 1) is only applicable to the data field. This feature built into the WD42C22C provides the user with the ability to detect and correct errors in the data field automatically.

The following is a summary of the parameters considered when ECC is used:

- 1. SDH register bit 7.
- 2. Read and write command bit 1 (L).
- 3. Compute correction command.
- 4. Set parameter command.
- 5. Error occurred, bit 0 of the status register.
- 6. On any ECC error the controller stops regardless of the T bit. (Refer to the read command description.)

The SDH register bit 7 must be equal to one to change from the CRC mode to the ECC mode, for MFM and NRZ only.

When an ECC error is detected, no attempt is made to correct it and bit 0 of the status register and bit 6 of the error register are set. The user now has two choices:

- 1. Ignore the error and make no attempt to correct it.
- 2. Use the compute correction command to determine the pattern and location of the error, and correct it within the user's program.

When implementing the compute correction command, use it before executing commands that alter the content of the ECC register. The read, write, scan, and format commands can alter the syndrome and make correction impossible. If the compution correction command determines that the error is uncorrectable, then the error bits in the status register and error register are set.

Although ECC generation starts with the first bit of the F8 byte in the data ID field, the actual ECC bytes produced for the sector are the same as if the A1 byte was included.

The 32-bit ECC polynomial is:

$$X^{32} + X^{28} + X^{26} + X^{19} + X^{17} + X^{10} + X^{6} + X^{2} + 1$$

and is the same one used in the WD1002, WD1003, and WD1006 controller boards. The 32-bit ECC polynomial has an 11 bit maximum single burst correction span. The reverse 32-bit ECC polynomial is:

$$X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + 1$$

The non-detection probability for the 32-bit ECC polynomial is:

$$2.3\ (E\text{-}10),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

and the miscorrection probability is:

$$1.57\ (E\text{-}5),\ r^{\dagger} = 516 \times 8,\ b^{\dagger} = 5$$

The 56-bit ECC polynomial is:

$$X^{56} + X^{52} + X^{50} + X^{43} + X^{41} + X^{34} + X^{30} + X^{26} + X^{24} + X^{8} + 1$$

The 56-bit ECC polynomial has a 22 bit maximum single burst correction span.

The reverse 56-bit ECC polynomial is:

$$X^{56} + X^{48} + X^{32} + X^{30} + X^{26} + X^{22} + X^{15} + X^{13} + X^{6} + X^{4} + 1$$

The non-detection probability for the 56-bit ECC polynomial is:

$$1.39\ (E\text{-}17),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

and the miscorrection probability is:

$$5.84\ (E\text{-}11),\ r^{\dagger} = 519 \times 8,\ b^{\dagger} = 11$$

The set parameter command selects the number of bits in the correction span, through the use of bit 0.

Read and write commands, with the L bit (bit 1) set to one, are referred to as read long and write long commands. With these commands, no ECC or CRC characters are generated or checked by the WD42C22C. In effect, the four or seven bytes are handled as an additional four or seven bytes of data which pass through the data buffer. With proper use of the write, read long, write long, and read commands, a diagnostic routine may be developed to test the accuracy of the error correction process.

For CRC/ECC calculations, the CRC/ECC register is initialized to all 1's. For CRC/ECC purposes only, the address mark byte has a value of "A1" and is included in the CRC/ECC calculations.

2.7 MFM/RLL ENCODING AND MFM/RLL DECODING

The MFM/RLL encoding section receives 8-bit parallel data and generates either MFM or RLL write data depending on the K option in the load parameter block command. This section operates with a write clock having a frequency of the desired bit rate. The write clock need not be synchronized to read clock (RC).

Data bytes are written to the drive most significant bit first. The MFM/RLL decoding section generates 8 bit binary data from MFM or RLL read data once an address mark has been detected. Table 5 lists the RLL coding rules followed by the controller.

NRZ Data				RLL Code Word Output	
First Bit		Last Bit		First Bit	Last Bit
1	1	X	X	1 0 0 0	X X X X
1	0	X	X	0 1 0 0	X X X X
0	1	1	X	0 0 1 0	0 0 X X
0	1	0	X	0 0 0 1	0 0 X X
0	0	0	X	1 0 0 1	0 0 X X
0	0	1	1	0 0 0 0	1 0 0 0
0	0	1	0	0 0 1 0	0 1 0 0

TABLE 5. RLL CODING RULES

When NRZ mode is selected, the MFM/RLL encode and decode logic is bypassed. NRZ read data is clocked in on the rising edge of Read Clock and NRZ write data is clocked out on the rising edge of WC.

2.8 ADDRESS MARK DETECTOR

An address mark is a unique 2 byte code placed at the beginning of each ID field or data field. A series of zero bytes always precedes each address mark. The address mark detector section begins searching for an address mark when synchronization has been lost after a series of zero bytes is detected. The detection of an address mark establishes resynchronization.

The address mark is composed of a 2 byte sequence. The first byte is used for resynchronization and the second byte specifies ID or data field. For the MFM mode, the first byte is an $A1_{16}$ byte with missing clock (data = A1, clock = 0A). The second byte is encoded with normal MFM rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In RLL mode, the first byte is a unique code which violates normal RLL coding rules but does not violate the 2,7 timing rule. The RLL address mark pattern is 1000 0000 1001 0000 (8090_{16}). The second byte is encoded with normal RLL rules. FF through FC and F7 through F4 specify the beginning of an ID field and F8 specifies the beginning of a data field.

In NRZ mode, an NRZ A1 byte establishes byte synchronization. When the WD42C22C is used to control an ESDI (NRZ) drive, the Sector Pulse (Address Mark Found) signal will qualify read data to prevent false address mark detection.

2.9 CONTROLLER TO DATA SEPARATOR INTERFACE

The read interface section generates READ GATE (RG) from signals sent by the PLA controller and by the DRUN input. In this system, raw read data from the drive is presented to the RD in put. RG is low when the controller is not inspecting read data. When a read command is started and a search begins for an address mark, DRUN from the data separator is examined. Since each

address mark should be preceded by approximately 12 bytes of zeroes, RG is activated when a sequence of zeroes is detected by DRUN and read data is examined until either an address mark is detected or a non-zero byte which is not an address mark is detected. If an address mark was detected, and it was preceded by at least 8 bytes of zeroes, read gate is held high and the ID or data field can be read.

If a non-zero non-address mark byte was detected, then RG is dropped for at least 2 byte times, allowing the phase lock loop to resynchronize with WC, before inspecting DRUN input again. If the desired ID field was read, then the sector transfer can be made. If a data field was detected or if the ID bytes did not match, or if an address mark was not preceded by eight bytes of zeroes with six coming after RG on, then RG is lowered and DRUN is inspected again for a sequence of zeroes.

Figures 4 illustrates the PLL control sequence for the ID field. Figure 5 illustrates the PLL control sequence for the data field.

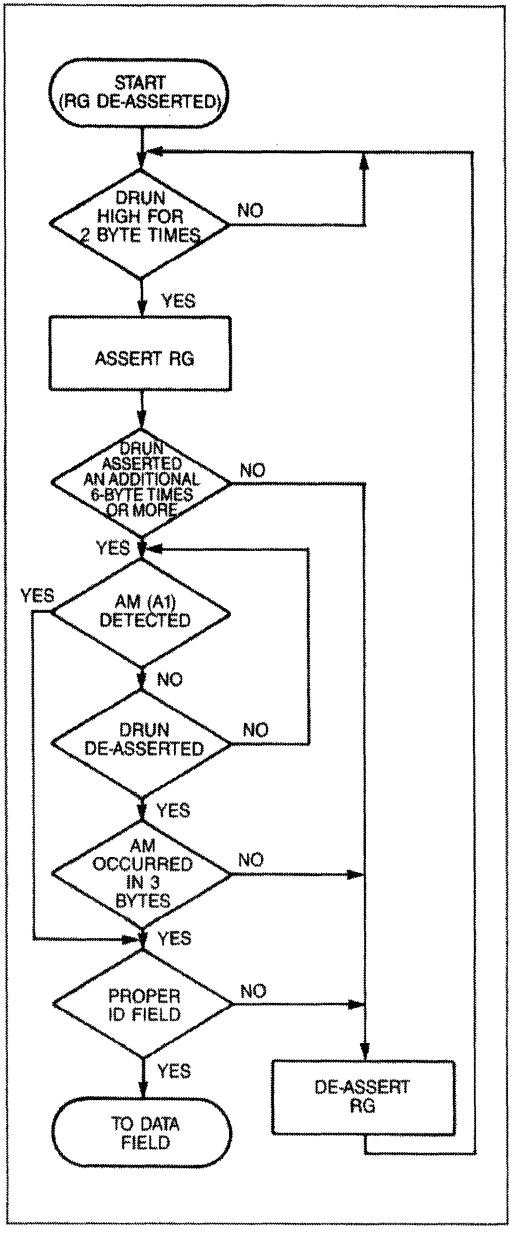

FIGURE 4. PLL CONTROL (ID FIELD)

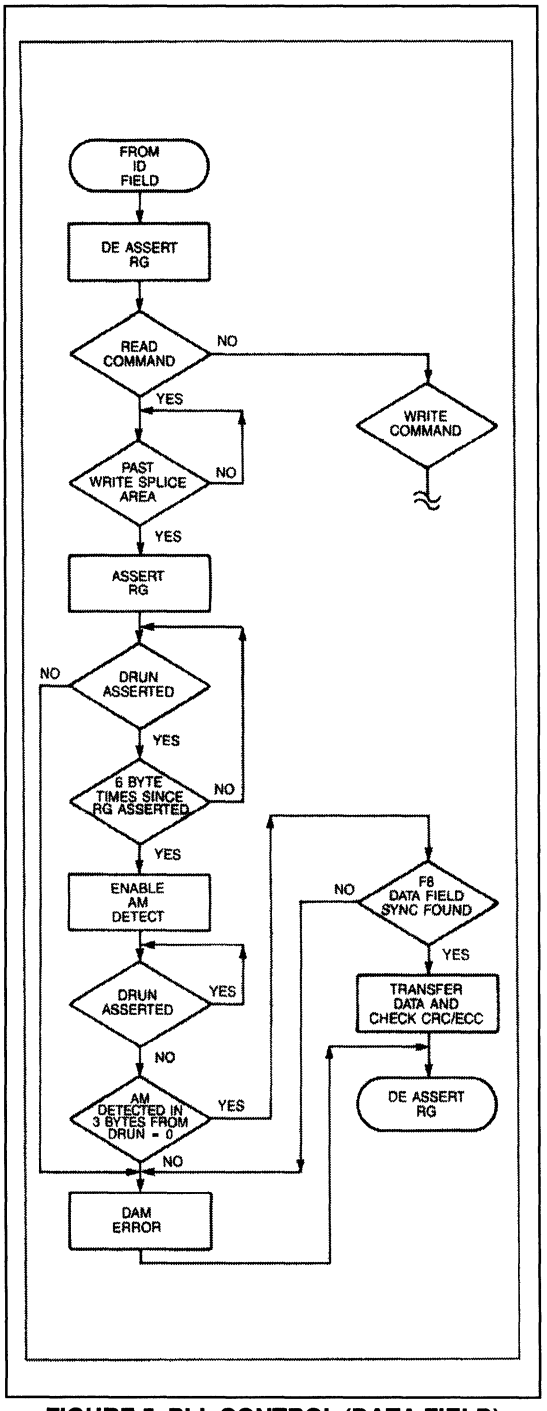

FIGURE 5. PLL CONTROL (DATA FIELD)

The write precompensation circuitry, in the controller to the drive interface, reduces the effects one bit has on another. There are two parts to write precompensation logic, reduced write current (RWC) and shifting of the bits as they are written. The RWC is **NOT** controlled by the drive controller. The local microcontroller should specify when the write current is reduced by asserting its own RWC output.

The shifting of the data bits is controlled by the $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs. These two outputs should be used to delay the output as follows in Table 6:

$\overline{\text{EARLY}}$	$\overline{\text{LATE}}$	DELAY
0	1	no delay
1	1	one unit delay
1	0	two units delay

TABLE 6. EARLY AND LATE DELAYS

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The $\overline{\text{EARLY}}$ and $\overline{\text{LATE}}$ outputs are generated according to the rules in Tables 7 (RLL) and 8 (MFM or NRZ).

RLL Coded Data Pattern			
Preceding Bits	Comp. Bit	Following Bits	Precomp
X 1 0 0	1	0 0 0 X	EARLY
X 0 0 0	1	0 0 0 X	None
X 0 0 0	1	0 0 1 X	LATE
0 1 0 0	1	0 0 1 0	None

TABLE 7. EARLY AND LATE GENERATION (RLL MODE)

MFM Coding - NRZ Data Pattern			
Preceding Bits	Comp. Bit	Following Bits	Precomp
X X X 1	1	0 X X X	EARLY
X X X 0	1	1 X X X	LATE
X X 0 0	0	1 X X X	EARLY
X X 1 0	0	0 X X X	LATE

TABLE 8. EARLY AND LATE GENERATION (MFM - NRZ)

3.0 INTERFACE PORTS AND TASK FILES

3.1 HOST INTERFACE ORGANIZATION

The WD42C22C's host interface directly connects to the IBM XT or IBM AT system bus as well as the system bus of any XT or AT compatible. The WD42C22C has high current drivers which allow it to be directly connected to the system bus.

The register configuration for the host interface is dependent on the state of the AT/$\overline{XT}$ control bit in the interface control register which is written by the local microcontroller.

There is an additional slave host mode. In this mode, the microcontroller communicates to a peripheral device with up to 32 registers through the host interface. The slave device can transfer data to/from the buffer RAM by using a slave DMA scheme such as the WD-BUS mode in the SBIC.

The sequence that the microcontroller follows to transfer data between the buffer RAM and the host is defined under the buffer manager description.

3.2 XT HOST INTERFACE

To put the WD42C22C in the XT compatible interface mode the local microcontroller resets the AT/$\overline{XT}$ control bit. In this mode, $\overline{HCS}$ should be active when I/O ports 320 (hex) through 323 (hex) are addressed. (XT I/O ports 320 through 323 are primary ports. XT I/O ports 324 through 327 are secondary ports. Unless otherwise noted, information regarding the primary ports is identical to information on secondary ports.) Table 9 lists the port descriptions for this mode.

HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
X	X	0	0	Read data	Write data
X	X	0	1	Hardware status	Hardware reset
X	X	1	0	Drive configuration	Drive select
X	X	1	1	NOT USED	DMA and interrupt control

TABLE 9. XT PORT DESCRIPTIONS

3.2.1 READ DATA PORT (HA1 THRU HA0 = 0, READ)

The read data port is used to send data and status to the host processor. The data read from this port comes from the buffer RAM under the control of the buffer manager.

3.2.2 WRITE DATA PORT (HA1 THRU HA0 = 0, WRITE)

The write data port is used to send commands and data from the host to the drive controller. The data is written to the buffer RAM under the control of the buffer manager.

3.2.3 HARDWARE STATUS (HA1 THRU HA0 = 1, READ)

This port contains the controller hardware status. It can be read by the host at any time. Bit 7, bit 6, bit 2, and bit 1 are written by the local microcontroller. Bit 5, bit 4, bit 3, and bit 0 are controlled by internal logic. The bits are defined as follows:

Bit							
7	6	5	4	3	2	1	0
X	X	IRQ	DRQ	XBSY	C/D	I/O	REQ

3.2.3.1 BIT 5 INTERRUPT REQUEST

This bit signifies that an interrupt is pending. IRQ reflects the state of the INTRQ output. The INTRQ pin is tri-stated and the IRQ status bit

and internal interrupt flip-flop are reset when the host disables the interrupt or when the WD42C22C is reset, either by the host or by asserting master reset.

3.2.3.2 BIT 4 DMA REQUEST

This bit signals that the WD42C22C is ready for a DMA transfer to take place. The direction of the transfer is determined by the I/O bit. This bit reflects the state of the DREQ output.

3.2.3.3 BIT 3 XT BUSY

This bit indicates that the WD42C22C is busy executing a command and is unable to accept another command. This bit is set by during a reset.

3.2.3.4 BIT 2 COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read and write data ports. C/$\overline{\text{D}}$ set to 1 indicates that a command or status transfer is expected. C/$\overline{\text{D}}$ set to 0 indicates that a data transfer is expected.

3.2.3.5 BIT 1 INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{\text{O}}$ set to 1 indicates an input (read) by the host and I/$\overline{\text{O}}$ set to 0 indicates an output (write) by the host.

3.2.3.6 BIT 0 REQUEST

This bit is one of the handshaking signals between the host and WD42C22C. When transferring data to/from, the WD42C22C's read data and write data ports by the host, assertion of this bit informs the host that the WD42C22C is ready for the transfer.

3.2.4 CONTROLLER RESET (HA1 THRU HA0 = 1, WRITE)

When this port is written, regardless of the data written, the RESET output is asserted if enabled. If the reset has been disabled by the local microcontroller, then writing to this port asserts $\overline{\text{MCINT}}$ and the local microcontroller is responsible for resetting the logic on the drive controller board.

3.2.5 DRIVE CONFIGURATION INFORMATION (HA1 THRU HA0 = 2, READ)

This register, when read, informs the host about the configuration of the drive(s) attached. This configuration information is written by the local microcontroller.

3.2.6 CONTROLLER SELECT (HA1 THRU HA0 = 2, WRITE)

When this port is written, regardless of the data written, the $\overline{\text{MCINT}}$ output is asserted to inform the local microcontroller that the controller board has been selected.

3.2.7 DMA AND INTERRUPT MASK (HA1 THRU HA0 = 3, WRITE)

This port enables or disables the DMA and interrupt to the host. When IRQEN is set to 1, then interrupts to the host are enabled. This bit is cleared when the WD42C22C is reset. The INTRQ line is tri-stated and the host interrupt is cleared when the interrupts are disabled. When DRQEN is set to 1, then DMA requests to the host are enabled. This bit is cleared when the WD42C22C is reset.

Bit							
7	6	5	4	3	2	1	0
X	X	X	X	X	X	IRQ EN	DRQ EN

3.3 AT HOST INTERFACE

To put the WD42C22C in the AT compatible interface mode, the AT/$\overline{\text{XT}}$ control bit is set by the local microcontroller. The $\overline{\text{HCS}}$ chip select should be active when I/O ports $1F0_{16}$ through $1F7_{16}$ and $3F6_{16}$ and $3F7_{16}$ are addressed for primary addressing and for I/O ports 170_{16} through 177_{16} and 376_{16} and 377_{16} for secondary addressing. Only address signals HA8 through $\overline{\text{HA3}}$ and AEN need to be decoded to generate $\overline{\text{HCS}}$. Table 10 describes the ports for AT mode as follows:

ABSY	HA9	HA2	HA1	HA0	READ PORT	WRITE PORT
					AT TASK FILE COPY	
0	0	0	0	0	Read Data (16 bits)	Write Data (16 bits)
0	0	0	0	1	Host Error Register	Write Precomp Cylinder
0	0	0	1	0	Sector Count	Sector Count
0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	1	0	SDH	SDH
0	0	1	1	1	Host Status Register	Host Command Register
1	0	X	X	X	Host Status Register	INVALID
					CONTROL PORTS	
X	1	1	1	0	Alternate Status Register	Fixed Disk Register
X	1	1	1	1	Digital Input Register*	NOT USED

*Bit 7 is tri-stated when the digital input register is read to accomodate the floppy disk change status.

TABLE 10. AT MODE PORT DESCRIPTIONS

When port 0 is accessed the $\overline{\text{IOCS16}}$ output is asserted when in AT programmed I/O mode. All buffer data transfers are 16 bits. The ECC byte transfers in a long mode (read or write) are 8 bit transfers. All other register transfers are 8 bits.

Registers 1 through 7 are an identical copy of the drive controller task registers 1 through 7. These registers can be read or written by the host only when the ABSY status bit is not active. Any attempt by the host to read the AT task file copy while ABSY is active results in the host status register being read. The AT task file copy registers cannot be written by the host while ABSY is active.

3.3.1 ERROR REGISTER (HA9, HA2 THRU HA0 = 01, READ)

The error register is read only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	0	IDNF	0	AC	TK0	DMNF

3.3.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field will not be read or written.

3.3.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

An uncorrectable ECC error or a CRC error was detected in the data field.

3.3.1.3 BIT 5 RESERVED

Not used, forced to zero.

3.3.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be

found. For read and write sector commands, with the retry disable bit reset, this bit indicates that after 10 index pulses, an auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set, then no matching ID field was found after 2 index pulses; no auto-scan or auto-seek is performed.

3.3.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.3.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.3.1.7 BIT 1 TRACK 0 ERROR

This bit, when set, indicates an error detecting Track 0 during a restore.

3.3.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.3.2 WRITE PRECOMP CYLINDER REGISTER (HA9, HA2 THRU HA0 = 01, WRITE)

This register is used to control the Reduce Write Current (RWC) signal going to the drive. RWC is turned on if the present position cylinder number is greater than or equal to the 4 times the write precomp cylinder number. If the write precomp cylinder number is FF_{16}, then the RWC is never asserted.

3.3.3 SECTOR COUNT (HA9, HA2 THRU HA0 = 02, READ/WRITE)

This register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count is decremented and the sector number is incremented after each sector transfer between the buffer and host or drive.

3.3.4 SECTOR NUMBER (HA9, HA2 THRU HA0 = 03, READ/WRITE)

The sector number register is used to hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.

3.3.5 CYLINDER NUMBER LOW AND HIGH REGISTERS (CYLINDER NUMBER LOW: HA9, HA2 THRU HA0 = 04, READ/WRITE. CYLINDER NUMBER HIGH: HA9, HA2 THRU HA0 = 05, READ/WRITE)

These registers specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047. Cylinder number low register holds the 8 least significant bits of the desired cylinder number. Cylinder number high register holds the three most significant bits of the desired cylinder number in bits 0 through 2. Bits 3 through 7 are not normally used in disk controller boards. These bits are latched when writing to this register. This means that all 8 bits can be used to transfer information between the host and the local microcontroller.

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3.3.6 SDH REGISTER (HA9, HA2 THRU HA0 = 06, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode.

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	0	SS	Drive Number	Head Number			

3.3.6.1 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode.

3.3.6.2 BIT 5 SECTOR SIZE

Bit 5 (SS0) is used to select sector size. If SS0 = 0, then the sector size is 256 bytes and if SS0 = 1, then the sector size is 512 bytes.

3.3.6.3 BIT 4 DRIVE SELECT

Bit 4 specifies the desired drive number. This bit also determines which of the two internal drive status registers are read when the host accesses the host status register or alternate status register. If DS = 0, the host receives drive zero status. If DS = 1, then the host receives drive one status.

3.3.6.4 BITS 3 THROUGH 0 HEAD NUMBER

Bits 3, 2, 1 and 0 specify the desired head number.

3.3.7 HOST STATUS REGISTER (HA9, HA2 THRU HA0 = 7, READ)

The status register reads only and reflects the status of the controller as well as the status of certain drive control lines. Some of the status bits are controlled by the local microcontroller. Drive status comes from two registers in the WD42C22C, one for each drive. Bit 4 of the SDH register in the AT task file copy controls which of the two registers is read when the host reads this port. Reading of the status register by the host resets INTRQ. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
ABSY	RDY	WF	SC	DRQ	DWC	IDX	ERR

3.3.7.1 BIT 7 AT BUSY

This bit is set to 1 when the controller is accessing the disk. ABSY is activated by the start of a command (writing into the host command register). It is deactivated at end of all commands by the local microcontroller. This bit is also set during a reset.

3.3.7.2 BIT 6 DRIVE READY

This bit reflects the state of the DRDY drive status pin. Any command aborts if DRDY is low. This bit is written by the local microcontroller.

3.3.7.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF drive status pin. Any command aborts if WF is high. This bit is written by the local microcontroller.

3.3.7.4 BIT 4 SEEK COMPLETE

This bit reflects the state of the SC signal coming from the drive. This bit is written by the local microcontroller.

3.3.7.5 BIT 3 DATA REQUEST

This bit is asserted when the host should be transferring data between the RAM buffer and host. This bit is controlled by the buffer manager.

3.3.7.6 BIT 2 DATA WAS CORRECTED

This bit indicates that an error in the data field was detected and corrected. The buffer contains corrected data. This bit is written by the local microcontroller.

3.3.7.7 BIT 1 INDEX

This bit reflects the state of the INDEX pin.

3.3.7.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is active. This bit is written by the local microcontroller.

3.3.8 HOST COMMAND REGISTER (HA9, HA2 THRU HA0 = 7, WRITE)

The command to be executed is written into this register. Writing this register sets ABSY in the status register and asserts the $\overline{\text{MCINT}}$ pin going to the local microcontroller. The command latches in a register which the local microcontroller reads. Writing this register resets INTRQ.

3.3.9 ALTERNATE STATUS REGISTER (HA9, HA2 THRU HA0 = E, READ)

This register is the same as the host status register (7) but mapped at a different address. Refer to page 23 for the bit description.

3.3.10 FIXED DISK REGISTER (HA9, HA2 THRU HA0 = E, WRITE)

The fixed disk register is used by the host to control some of the internal functions of the WD42C22C. Bit 0 and bits 4 through bit 7 are reserved for future definition. These bits are currently not used in the AT protocol but they are implemented in the WD42C22C, i.e. the fixed disk register passes 8 bits between the host and the

local microcontroller. The host should write zeroes to these bits in AT mode. The fixed disk register is coded as follows:

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.3.10.1 BIT 3 HEAD SELECT 3 ENABLE

When HS3EN = 1, then HEAD SELECT 3 is asserted by the local microcontroller. When HS3EN = 0, then RWC is asserted by the local microcontroller.

3.3.10.2 BIT 2 RESET

Writing a 1 to this bit resets the WD42C22C. The RESET output is asserted and remains asserted until this bit is written back to 0. This bit must be on for a minimum of 5.0 µsec. If reset has been disabled by the local microcontroller then writing a '1' to this bit only resets the WD42C22C. $\overline{RESET}$ is not asserted in this case. The WD42C22C asserts $\overline{MCINT}$ and the local microcontroller is responsible for resetting the drive controller board logic.

3.3.10.3 BIT 1 $\overline{INTERRUPT\ ENABLE}$

When $\overline{IEN}$ = 0, then the $\overline{INTRQ}$ output to the host is enabled. When $\overline{IEN}$ = 1, then the INTRQ output to the host is disabled. Disabling interrupts does NOT reset an existing interrupt but inhibits all further interrupts. Any interrupts pending when this bit is set causes the INTRQ output to be asserted. A system master reset does NOT affect the $\overline{IEN}$ bit but resets any existing interrupt. The internal power qualified reset sets $\overline{IEN}$ to 0. When interrupts are disabled, then the INTRQ pin is tri-stated.

3.3.11 DIGITAL INPUT REGISTER (HA9, HA2 THRU HA0 = F, READ)

The digital input register is used by the host to determine the state of WRITE GATE and the drive selects and head selects. Bit 5 is written by the local microcontroller when HS3EN (bit 3 of the fixed disk register) is set to zero. Bit 5 comes from bit 3 of the host SDH register with HS3EN set to one. Bits 0 through bit 4 also come from the host SDH register. When this register is read by the host, then HD7 (pin 82) is tri-stated. It is coded as follows:

Bit							
7	6	5	4	3	2	1	0
X	$\overline{WG}$	$\overline{HS3}$/ RWC	$\overline{HS2}$	$\overline{HS1}$	$\overline{HS0}$	$\overline{DS2}$	$\overline{DS1}$

3.3.11.1 BIT 6 WRITE GATE ON

This bit reflects the state of the $\overline{WG}$ output pin.

3.3.11.2 BIT 5 HEAD SELECT 3/ REDUCE WRITE CURRENT

This bit reflects the state of the $\overline{HS3}$/$\overline{RWC}$ drive control output. The $\overline{RWC}$ bit is written by the local microcontroller. $\overline{HS3}$ comes from the SDH register bit 3.

3.3.11.3 BIT 4, BIT 3, AND BIT 2 HEAD SELECTS

These bits reflect the states of the $\overline{HS2}$, $\overline{HS1}$, $\overline{HS0}$, and drive control outputs respectively. These bits are controlled by SDH register bits 2 through 0 respectively.

3.3.11.4 BIT 1 AND BIT 0 DRIVE SELECTS

These bits indicate which drive is currently being selected by the host. They are controlled by the SDH register bit 4.

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A D 7	A D 6	A D 5	A D 4	A D 3	A D 2	A D 1	A D 0	READ PORT	WRITE PORT
DISK CONTROLLER TASK FILE									
0	0	0	X	X	X	X	X	BUS TRISTATE	NOT USED
0	0	1	0	0	0	0	0	INVALID	INVALID
0	0	1	0	0	0	0	1	Error Register	PLO Length
0	0	1	0	0	0	1	0	Sector Count	Sector Count
0	0	1	0	0	0	1	1	Sector Number	Sector Number
0	0	1	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
0	0	1	0	0	1	0	1	Cylinder Number High	Cylinder Number High
0	0	1	0	0	1	1	0	SDH	SDH
0	0	1	0	0	1	1	1	Status Register	Command Register
XT									
0	0	1	0	1	1	0	1	Hardware Status	Hardware Status
0	0	1	0	1	1	1	0	NOT USED	Drive Configuration
BUFFER MANAGER									
0	0	1	1	0	0	0	0	Host Buffer Pointer Low	Host Buffer Pointer Low
0	0	1	1	0	0	0	1	Host Buffer Pointer High	Host Buffer Pointer High
0	0	1	1	0	0	1	0	Host Transfer Count Low	Host Transfer Count Low
0	0	1	1	0	0	1	1	Host Transfer Count High	Host Transfer Count High
0	0	1	1	0	1	0	0	Disk Buffer Pointer Low	Disk Buffer Pointer Low
0	0	1	1	0	1	0	1	Disk Buffer Pointer High	Disk Buffer Pointer High
0	0	1	1	0	1	1	0	Microcontroller RAM Access	Microcontroller RAM Access
0	0	1	1	0	1	1	1	Buffer Status	Buffer Control

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP

3.4 SLAVE HOST INTERFACE

In slave mode, the WD42C22C host interface can be hooked up to a peripheral device such as the WD33C93 (SBIC). The microcontroller reads and writes the peripheral device through the WD42C22C using the ports as follows:

A BSY	A D 7	A D 6	A D 5	A D 4	A D 3	A D 2	A D 1	A D 0	READ PORT	WRITE PORT
X	0	1	0	0	1	0	0	0	Bus tri-state	Slave address port for reads
X	0	1	0	0	1	0	1	0	Bus tri-state	Slave address port for writes
X	0	1	0	0	1	0	0	1	Slave read data	Slave write data

ABSY	A7	A6	A5	A4	A3	A2	A1	A0	READ PORT	WRITE PORT
MISC.										
X	0	0	1	1	1	0	0	0	Interface Status	Interface Control
X	0	0	1	1	1	0	0	1	Configuration Status Low	NOT USED
X	0	0	1	1	1	0	1	0	Configuration Status High	NOT USED
X	0	0	1	1	1	0	1	1	Drive Interface Status	Drive Interface Control
X	0	0	1	1	1	1	0	0	Alternate Sector Number	NOT USED
AT INTERFACE										
X	0	0	1	0	1	0	1	0	AT Control Register	AT Control Register
X	0	0	1	1	1	1	0	1	Drive 0 Status	Drive 0 Status
X	0	0	1	1	1	1	1	0	Drive 1 Status	Drive 1 Status
X	0	0	1	1	1	1	1	1	Fixed Disk Register	Digital Input Register
AT INTERFACE (TASK FILE COPY)										
1	0	1	0	0	0	0	0	1	Write Precomp Cylinder	Error Register
1	0	1	0	0	0	0	1	0	Sector Count	Sector Count
1	0	1	0	0	0	0	1	1	Sector Number	Sector Number
1	0	1	0	0	0	1	0	0	Cylinder Number Low	Cylinder Number Low
1	0	1	0	0	0	1	0	1	Cylinder Number High	Cylinder Number High
1	0	1	0	0	0	1	1	0	SDH	SDH
1	0	1	0	0	0	1	1	1	Command Register (from Host)	NOT USED
SLAVE HOST										
0	0	1	0	0	0	X	X	X	INVALID	INVALID
X	0	1	0	0	1	0	0	0	INVALID	Slave Address Port for reads
X	0	1	0	0	1	0	0	1	Slave Read Data	Slave Write Data
X	0	1	0	0	1	0	1	0	INVALID	Slave Address Port for writes
X	0	1	0	0	1	X	X	X	INVALID	NOT USED
X	0	1	0	1	X	X	X	X	INVALID	NOT USED
X	0	1	1	X	X	X	X	X	BUS TRISTATE	NOT USED
X	1	X	X	X	X	X	X	X	BUS TRISTATE	NOT USED

TABLE 11. LOCAL MICROCONTROLLER REGISTER MAP (CONT'D)

The slave peripheral connects to the WD42C22C using an ALE type interface. Register reads and writes are always 8-bit. The procedure to read or write a slave peripheral register is to first write the register number to the slave address port before the register contents are read or written. This address must always be written before each register access even when consecutively accessing the same register two or more times.

Data transfers between the peripheral device and the WD42C22C are WD-bus mode and can be either 8-bit or 16-bit and is controlled by the H16/8 bit (bit 1 of the auxilliary buffer control register). The slave mode is enabled by the HSMB bit (bit 6 of the auxilliary buffer control register).

3.5 LOCAL MICROCONTROLLER INTERFACE ORGANIZATION

The local microcontroller controls the host interface mode (AT or XT) and controls the buffer manager and the drive controller. The local microcontroller is usually in a sleep state until it is told to do something by the assertion of the MCINT output. In the XT mode, MCINT is asserted when the controller is selected. In the AT mode, MCINT is asserted when the host writes to the command register. In slave host mode, MCINT is asserted when the slave peripheral device asserts its INTRQ signal. MCINT is also asserted at the end of each host or disk transfer regardless of the interface mode.

The local microcontroller can have either the Intel-type (8051) or the Motorola-type (68HC11) interface. The WD42C22C has a built-in MOtorola-inTEL (MOTEL) circuit which can sense the processor interface type and can therefore be directly interfaced to either type processor.

Table 11 lists the register map for the local microcontroller.

3.6 DISK CONTROLLER TASK FILE (AD7 THRU AD0 = 20 THRU 27)

3.6.1 ERROR REGiSTER (AD7 THRU AD0 = 21, READ)

The error register reads only and contains the specific error status pertaining to a command. The meaning of the status register bits are as follows:

Bit							
7	6	5	4	3	2	1	0
BB	CRC/ ECC	RIDF	IDNF	0	AC	0	DMNF

3.6.1.1 BIT 7 BAD BLOCK

A bad block address mark has been detected when trying to read or write that sector. The data field is not be read or written.

3.6.1.2 BIT 6 CRC/ECC DATA FIELD ERROR

A CRC error in the data field has been detected when in CRC mode. In ECC mode, data errors were detected in the data.

3.6.1.3 BIT 5 RELOCATION ID FOUND

This bit is set if a relocation ID is found after detecting the bad block mark in the desired sector's ID field. This bit is only valid if the R option is used in the set parameter command.

3.6.1.4 BIT 4 ID NOT FOUND

Occurs when cylinder, head, sector, size parameters with a correct ID field CRC cannot be found. For a scan ID command, this bit is set after 10 index pulses if the retry disable bit is not set. Otherwise, IDNF is set after 2 index pulse if no ID was found. For read and write sector commands with the retry disable bit set, this bit indicates that after 10 index pulses, auto-scan ID and auto-seek, and 10 more index pulses, no matching ID field was found. If the retry disable bit is set and no matching ID field was found after 2 index pulses, then no auto-scan or auto-seek is performed.

3.6.1.5 BIT 3 RESERVED

Not used, forced to zero.

3.6.1.6 BIT 2 ABORTED COMMAND

Set if command was started and one of the following conditions occurred:

- 1. Drive not ready
- 2. Write fault
- 3. Illegal command code.

3.6.1.7 BIT 1 RESERVED

Not used in WD42C22C, forced to zero.

3.6.1.8 BIT 0 DATA ADDRESS MARK NOT FOUND

Set if the first two bytes of the data field following an ID match are not A1 F8. This condition is checked for read sector commands only.

3.6.2 PLO LENGTH REGISTER (AD7 THRU AD0 = 21, WRITE)

This register is used for two purposes:

- 1. To determine the length of the Data PLO sync field during write commands and to determine the length of the ID PLO sync field during format commands. The contents of this register regulates the PLO field size in all data coding modes.
- 2. To load a value in the internal GAP register. During the load parameter block command, the contents of the lower six bits of the PLO length register are transferred to the internal GAP register. In hard sector NRZ (ESDI) mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the leading edge of READ GATE. In hard sector MFM or RLL mode, this internal GAP register is used to control the delay between the INDEX or SECTOR pulse and the falling edge of the internally generated DRUN signal. In hard sector MFM or RLL mode, RG is asserted 2 byte times after INDEX or SECTOR. This GAP register is altered by loading the desired GAP register value into the PLO length register and then issuing a load parameter block command.

3.6.3 SECTOR COUNT (AD7 THRU AD0 = 22, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
NUMBER OF SECTORS/GAP VALUE SECTOR WITH BAD BLOCK							

This register is used for three purposes:

- 1. The sector count register is used in read sector, write sector, and format commands to implement multiple sector handling with one command. A value of 1 indicates a single sector transfer, a value of 2 indicates a 2 sector transfer, and so forth. A value of 0 indicates a 256 sector transfer. Sector count decrements and sector number increments after each sector transfer to or from the buffer.
- 2. To load a value into the internal gap value register. During the load parameter block command the contents of this register are transferred into an internal gap value register. This gap value register specifies the data byte written into the gaps during format commands.
- 3. To specify to the microcontroller the sector number where a bad block bit was detected if relocation ID searches are enabled. If the R option is set in a set parameter command, then during read and write commands if a bad block is detected, the WD42C22C searches for a special ID field containing relocation information. When the command terminates due to a bad block, then the sector number of the sector with the bad block is returned to the microcontroller in this register. This is true whether or not the relocation information is detected.

3.6.4 SECTOR NUMBER (AD7 THRU AD0 = 23, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
SECTOR NUMBER / GAP SIZE							

The sector number register has three uses:

- 1. To hold the number of the desired sector for read and write commands. The sector number can range from 0 to 255.
- 2. To control the Gap 1 and Gap 3 sizes during format commands. The sector number holds the number of gap bytes minus three for format (number of gap bytes minus six for NRZ mode).
- 3. To load a value into the internal pad value register. During the load parameter block command, the contents of this register are transferred into an internal pad value register. This pad value register specifies the data byte written into the ID and DATA pads during format and write commands.

3.6.5 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

This register has two functions:

- 1. To specify the cylinder number for read, write, and format commands. The cylinder number may range in value from 0 to 2047.
- 2. The cylinder number register is used during a load parameter block command to specify the desired sector size if a non-standard sec-

tor size is desired and to specify the offset for a write ID command. To load the internal sector size register, write in the desired sector size into the cylinder registers. Next, issue a load parameter block command. Set U=1 to enable the programmable sector size or programmable write ID offset.

3.6.6 CYLINDER NUMBER REGISTERS (CYLINDER NUMBER LOW: AD7 THRU AD0 = 24, READ/WRITE CYLINDER NUMBER HIGH: AD7 THRU AD0 = 25, READ/WRITE)

Cylinder number low register holds the 8 least significant bits of the desired cylinder number or the 8 least significant bits of the desired sector size.

Cylinder number high register holds the three most significant bits (bits 0 through 2) of the desired cylinder number or the three most significant bits of the desired sector size. Bits three through seven of the cylinder number high register are not used and must be set to zero.

3.6.7 SDH REGISTER (AD7 THRU AD0 = 26, READ/WRITE)

This register is used to specify the desired drive and head numbers and to specify CRC or ECC mode. There are two SDH modes available, three or four bit head number. Three bit head mode is the default after a master reset. Setting the H bit in the set parameter command engages the four bit head mode.

3.6.7.1 SDH REGISTER, THREE-BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	0	Head #		

3.6.7.2 SDH REGISTER, FOUR-BIT HEAD NUMBER

Bit							
7	6	5	4	3	2	1	0
CRC/ ECC	SS1	SS0	0	Head #			

3.6.7.3 BIT 7 ECC/CRC SELECT

This bit is set for data field ECC mode. It is reset for data field CRC mode. In RLL mode, this bit is ignored. RLL mode always uses 7-byte ECC. The CRC/ECC flag bit is not written on the disk at format time. The bad block flag is written on the disk in its place.

3.6.7.4 BIT 6 AND BIT 5 SECTOR SIZE

Bits 6 and 5 contain sector size bits. These bits are written on the disk at format time. These bits should be 0 if programmable sector size is used. These bits are reserved for special flags in programmable sector size mode. The possible sector sizes and their selection codes are as follows:

SS1	SS0	Sector Size
0	0	256 byte data field
0	1	512 byte data field
1	0	1024 byte data field
1	1	128 byte data field

The sector sizes can be optionally specified to be any value between 100 and 2048 bytes by using the load parameter block command. The user is responsible for validating the effectiveness of the ECC for sector sizes over 1056 bytes.

3.6.7.5 BIT 4 AND BIT 3 RESERVED BIT 4 DRIVE NUMBER RESERVED

Reserved. Set to 0.

3.6.7.6 BIT 2, BIT 1, AND BIT 0 THREE BIT HEAD NUMBER BIT 3, BIT 2, BIT 1, AND BIT 0 FOUR BIT HEAD NUMBER

Bits 2, 1, and 0 specify the desired head number in the three bit mode. Bits 3, 2, 1, and 0 specify the desired head number in four bit mode. The local microcontroller is responsible for outputting these bits to the drive.

NOTE

These bits are written on the disk at format time. The SDH byte written in the ID field during a format command is NOT the same as the SDH register. The SDH format byte is shown below:

3.6.7.7 SDH ID FIELD FORMAT BYTE (THREE BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	0	Head #		

3.6.7.8 SDH ID FIELD FORMAT BYTE (FOUR BIT HEAD MODE)

Bit							
7	6	5	4	3	2	1	0
Bad Block	SS1	SS0	0	Head #			

3.6.8 STATUS REGISTER (AD7 THRU AD0 = 27, READ)

The status register is read only and reflects the status of the controller as well as the status of certain drive control lines. If command in progress (bit 1) is set then no other register reads are valid and none of the other register bits are valid. The status register contents are returned for any read and all writes are disabled. The description of the status register bits follows:

Bit							
7	6	5	4	3	2	1	0
0	RDY	WF	1	0	0	0	ERR

3.6.8.1 BIT 7 ALWAYS 0

This bit is always zero when the microcontroller has access to this status register.

3.6.8.2 BIT 6 DRIVE READY

This bit reflects the status of the DRDY. Any command aborts if DRDY is low.

3.6.8.3 BIT 5 WRITE FAULT

This bit reflects the state of the WF pin. Any command aborts if WF is high.

3.6.8.4 BIT 4 ALWAYS 1

This bit reflects the state of the SC input to the drive controller. This signal is internally tied to V_{DD}.

3.6.8.5 BIT 3 ALWAYS 0

This bit reflects the state of the BDRQ signal that goes between the drive controller and the buffer manager. It is always zero when the microcontroller has access to this status register.

3.6.8.6 BIT 2 NOT USED

Forced to 0

3.6.8.7 BIT 1 ALWAYS 0

This bit reflects the state of the command in progress signal in the drive controller. It is always zero when the microcontroller has access to this status register.

3.6.8.8 BIT 0 ERROR

This bit indicates that a non-recoverable error has occurred. The error register describes the error condition when this bit is asserted.

Drive ready and write fault bits reflect the state of their associated input pins. The states of these status register bits are latched at the end of the command and are unlatched after the first status register read. Reading the status register results in the disk controller interrupt being reset.

3.6.9 COMMAND REGISTER (AD7 THRU AD0 = 27, WRITE)

The command to be executed is written into this register. Writing this register sets the internal BUSY and CIP signals and causes the controller to start executing the desired command. Writing this register resets the disk controller interrupt (DCI bit in the interface status register).

3.7 XT INTERFACE PORTS

3.7.1 XT HOST HARDWARE STATUS (AD7 THRU AD0 = 2D, READ/WRITE)

Bits 7, 6, 2, and 1 of this register are written by the local microcontroller and read by the host. The other bits reflect the state of certain hardware signals. This register is readable and valid in all host modes.

Bit							
7	6	5	4	3	2	1	0
1	1	IRQ	DRQ	XBSY	C/$\overline{D}$	I/$\overline{O}$	REQ

3.7.1.1 BITS 6 AND 7 UNDEFINED

These bits are currently undefined in the XT protocol and read as 1.

3.7.1.2 BIT 5 INTERRUPT REQUEST

This bit reflects the state of the INTRQ output. This bit can NOT be written by the microcontroller.

3.7.1.3 BIT 4 DMA REQUEST

This bit reflects the state of the DREQ output. This bit can NOT be written by the microcontroller.

3.7.1.4 BIT 3 XT BUSY

This bit reflects the state of the internal XT BUSY flipflop. This bit is set by during a reset and is set when the WD42C22C is selected in XT mode. This bit can NOT be written by the microcontroller.

3.7.1.5 BIT 2 COMMAND / $\overline{\text{DATA}}$

This bit tells the host which type of transfer is expected at the read data and write data ports. C/$\overline{D}$ = 1 indicates that a command or status transfer is expected and C/$\overline{D}$ = 0 indicates that a data transfer is expected. This bit is written by the microcontroller.

3.7.1.6 BIT 1 INPUT / $\overline{\text{OUTPUT}}$

This bit tells the host the direction of transfer for the two data ports. I/$\overline{O}$ = 1 indicates an input (read) by the host and I/$\overline{O}$ = 0 indicates an output (write) by the host. This bit is written by the microcontroller.

3.7.1.7 BIT 0 REQUEST

This bit indicates the state of the internal host transfer enable. This bit is active when the buffer manager is transferring data between the RAM and the host. This bit can NOT be written by the microcontroller. This bit is identical to the DRQ in the drive zero status and drive one status registers used in AT mode.

3.7.2 HOST DRIVE CONFIGURATION (AD7 THRU AD0 = 2E, WRITE)

This register is used to write the drive configuration information that is read by the host.

3.7.3 BUFFER MANAGER REGISTERS (AD7 THRU AD0 = 30 THRU 37) HOST BUFFER POINTER LOW (AD7 THRU AD0 = 30, READ/WRITE) HOST BUFFER POINTER HIGH (AD7 THRU AD0 = 31, READ/WRITE)

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BITS OF HOST BUFFER POINTER						

The host buffer pointer low register contains the least significant byte of the host buffer pointer. The host buffer pointer high register contains the seven most significant bits of the host buffer pointer. The host buffer pointer is used as the base address for the internal host buffer counter. The contents of the host buffer pointer registers are transferred to the host buffer pointer counter under the control of the buffer control register.

When the AHBP bit is set in the control register, then the pointer register is transferred to the pointer counter when the transfer counter reaches zero. If the transfer count is already zero, then the transfer occurs immediately. This allows a pending transfer to be queued behind the current transfer. When the pointer is transferred to the counter, the AHBP buffer status bit resets.

3.7.4 HOST TRANSFER COUNT LOW (AD7 THRU AD0 = 32, READ/WRITE HOST TRANSFER COUNT HIGH (AD7 THRU AD0 = 33, READ/WRITE)

The host transfer count low register contains the least significant byte of the host transfer count. The host transfer count high register contains the most significant bits of the host transfer count. The transfer count controls the number of bytes that are to be transferred on the host interface. The transfer count register is transferred to the internal transfer counter at the same time that the host buffer pointer register is transferred to the

host buffer pointer counter. The transfer counter is 12 bits long which gives a maximum transfer count of 4095 bytes.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF HOST TRANSFER COUNT							

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	MS BITS OF HOST TRANSFER COUNT			

3.7.5 DISK BUFFER POINTER LOW (AD7 THRU AD0 = 34, READ/WRITE) DISK BUFFER POINTER HIGH (AD7 THRU AD0 = 35, READ/WRITE)

The disk pointer low register contains the least significant byte of the disk buffer pointer. The disk pointer high register contains the seven most significant bits of the disk buffer pointer. The disk buffer pointer is used as the base address for the internal disk buffer counter. The contents of the disk buffer pointer registers are transferred to the disk buffer pointer counter under the control of the buffer control register. When the ADBP bit is set in the control register, then the pointer is transferred to the counter when the drive controller sets DRQI to 1 (bit 1) in the interface status register (38_{16}). This allows a pending transfer to be queued behind the current transfer. When the pointer register is transferred to the counter, the ADBP bit in the buffer status resets. If ADBP=0 when the drive controller sets DRQI to 1, then the drive controller stops transferring data to the buffer and discontinues the command until ADBP sets.

Bit							
7	6	5	4	3	2	1	0
LEAST SIGNIFICANT BYTE OF DISK BUFFER POINTER							

Bit							
7	6	5	4	3	2	1	0
0	MOST SIGNIFICANT BYTE OF DISK BUFFER POINTER						

3.7.6 MICROCONTROLLER RAM ACCESS PORT (AD7 THRU AD0 = 36, READ/WRITE)

This port is used by the local microcontroller to access the buffer RAM. Accesses to this port go through the drive controller's FIFO. These accesses are enabled by the MAC bit in the drive interface control register. The DRWB bit in the buffer manager control register controls the direction of the accesses.

3.7.7 BUFFER CONTROL REGISTER (AD7 THRU AD0 = 37, WRITE)

This register is used to control the buffer manager.

Bit			
7	6	5	4
AT/$\overline{XT}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.7.1 BIT 7 AT / $\overline{XT}$ INTERFACE CONTROL

This bit, along with HSMB, in the auxilliary buffer control register, controls the host interface type. If AT/$\overline{XT}$ = 0, then the interface is XT type if HSMB = 0. If AT/$\overline{XT}$ = 1, then the interface is AT type if HSMB = 0. This bit has no meaning if HSMB = 1. The RESET input and the host soft reset does not affect this bit.

3.7.7.2 BIT 6 READ CONFIGURATION

When this bit is set, all buffer address outputs are placed in a medium impedence state with each buffer address pin having a 180 µA current source pulldown. The buffer manager should be idle when this mode is enabled. This mode is used to read configuration switch information. The microcontroller should wait 100 µsec after setting this bit before reading the configuration registers. This bit resets when $\overline{RESET}$ is asserted.

3.7.7.3 BIT 5 RESET TRANSFER COUNTER

When this bit is set, the internal transfer counter and the host FIFO pointers reset. This bit resets after the transfer counter and FIFO reset.

3.7.7.4 BIT 4 ARM HOST BUFFER POINTER

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then when the internal transfer counter reaches zero the host buffer pointer is transferred to the internal host buffer counter and the host transfer count is transferred to the internal transfer counter. This bit is reset by the WD42C22C after the host pointer and count registers are transferred. This bit resets when $\overline{\text{RESET}}$ is asserted.

3.7.7.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit controls the direction of the host data transfers. It is used internally to control the direction of the FIFO. When HRWB = 0, then the host writes to the WD42C22C. When HRWB = 1, then the host reads from the WD42C22C.

3.7.7.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit controls the direction of the disk or local microcontroller data transfers. It is used internally to control the direction of the disk FIFO. When DRWB = 0, then the disk controller or local microcontroller writes to the buffer RAM. When DRWB = 1, then the disk controller or local microcontroller reads from the buffer RAM. When the microcontroller accesses the buffer RAM, then this bit should be written before the ADBP bit is set.

3.7.7.7 BIT 1 BURST DMA ENABLE

When BDEN = 1 and HDMA = 1 in the auxilliary buffer control register, then burst DMA transfers are enabled on the host interface.

3.7.7.8 BIT 0 ARM DISK BUFFER POINTER

Writing a 1 to this bit, sets an internal latch. Writing a 0 to this bit has no effect. When this bit is set, then the disk buffer pointer is transferred to the internal disk buffer counter when the drive controller sets the BDRQ interrupt. This bit also enables the disk controller to continue to the next sector. This bit is reset by the WD42C22C after the pointer registers have been transferred. When the disk controller port is used by the local microcontroller to access the buffer RAM, then setting this bit resets the disk FIFO pointers and the next byte read or written by the microcontroller will be at the new address loaded into the disk buffer pointer.

3.7.8 BUFFER STATUS REGISTER (AD7 THRU AD0 = 37, READ)

This register reflects the status of the buffer manager logic.

Bit			
7	6	5	4
AT/$\overline{\text{XT}}$	RDCFG	RXC	AHBP
3	2	1	0
HRWB	DRWB	BDEN	ADBP

3.7.8.1 BIT 7 AT / $\overline{\text{XT}}$ INTERFACE MODE

This status bit reflects the state of the AT/$\overline{\text{XT}}$ control bit defined above.

3.7.8.2 BIT 6 READ CONFIGURATION

This bit reflects the state of the read configuration control bit defined in the buffer manager control register.

3.7.8.3 BIT 5 RESET TRANSFER COUNTER

This bit reflects the state of the RXC control bit defined in the buffer control register.

3.7.8.4 BIT 4 HOST BUFFER POINTER ARMED

This bit reflects the state of the AHBP control bit defined in the buffer control register.

3.7.8.5 BIT 3 HOST READ / $\overline{\text{WRITE}}$

This bit reflects the state of the HRWB control bit defined in the buffer control register.

3.7.8.6 BIT 2 DISK READ / $\overline{\text{WRITE}}$

This bit reflects the state of the DRWB control bit defined in the buffer control register.

3.7.8.7 BIT 1 BURST DMA ENABLE

This bit reflects the state of the BDEN control bit defined in the buffer control register.

3.7.8.8 BIT 0 DISK BUFFER POINTER ARMED

This bit reflects the state of the ADBP control bit defined in the buffer control register.

3.7.9 AUXILLIARY BUFFER CONTROL REGISTER (AD7 THRU AD0 = 2F, WRITE)

This register is used for additional control of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	X	H16/$\overline{8}$	SCKS

3.7.9.1 BIT 7 HOST DMA

This bit controls the host data transfers to/from the buffer RAM. If HDMA = 1, then the data is transferred to the host via DMA regardless of the host interface selected. If HDMA = 0, the default, then data is transferred via programmed I/O.

3.7.9.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

When HSMB = 0, the default, then the host is a master which drives the WD42C22C in either XT or AT type interface. When HSMB = 1, then the host is a slave device which is controlled by the local microcontroller. The slave device can be addressed in either ALE or indirect mode. The SBIC is an example of a device which can be connected to the WD42C22C. The ALE mode supports up to 32 registers in the slave device. Data transfers occur via WD-BUS mode if HDMA = 1 and is an 8-bit transfer if H16/$\overline{8}$ = 0 and a 16-bit transfer if H16/$\overline{8}$ = 1. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.3 BIT 5 BURST CONTINUOUS

This bit, along with the HDMA bit, and the BDEN bit in the buffer control register control the bursting of data during DMA transfers. If BCNT = 1, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data continuously as long as the FIFOs can keep up. If BCNT = 0, HDMA = 1, and BDEN = 1, then the WD42C22C DMAs data in 8-byte or 16-byte maximum length bursts, for 8 and 16 bit host data bus width, respectively.

3.7.9.4 BIT 4 INTELLIGENT DRIVE DECODE

When IDD = 1, then the controller is assumed to be on an intelligent drive. The HD0-15, INTRQ, and DREQ/IOCS16 outputs are always tri-stated if the drive is not selected. If IDD = 0, the default, then the outputs are controlled normally. This bit resets upon power up but not affected by $\overline{\text{RESET}}$.

3.7.9.5 BIT 3 DRIVE SELECT

This bit is used when IDD = 1 to control drive selection. If AT/$\overline{\text{XT}}$ =1, then the drive is considered selected when SDH register bit 4 equals DSEL. If AT/$\overline{\text{XT}}$ = 0, then the drive is considered selected if DSEL = 1 and not selected if DSEL = 0. This bit resets upon power-up but not affected by $\overline{\text{RESET}}$.

3.7.9.6 BIT 1 HOST 16 / $\overline{8}$ BIT

This bit controls the width of the data transfers on the host side. If H16/$\overline{8}$ = 0, then the host data transfers are 8-bit. If H16/$\overline{8}$ = 1, the host data transfers are 16-bit. This bit resets upon power up but not affected by $\overline{\text{RESET}}$.

3.7.9.7 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit is used to control the clocking of the drive controller so that ESDI drives can be changed or data rates can be changed without the need for external clock deglitching. When SCKS =1, the default, then the WD42C22C synchronously switches the drive controller to the internal buffer clock (BCLK). When SCKS = 0, the WD42C22C switches the drive controller back to WCLK. The switch occurs only if both clocks are present. The CKSRC status bit defined below indicates whether or not the switch occured. When $\overline{\text{RESET}}$ is asserted, the buffer clock clocks the drive controller during the reset and SCKS is set. The microcontroller must switch the clock source to the WCLK input prior to issuing any commands to the drive controller.

3.7.10 AUXILLIARY BUFFER STATUS REGISTER (AD7 THRU AD0 = 2F, READ)

This register gives additional status of the buffer manager and host interface.

Bit			
7	6	5	4
HDMA	HSMB	BCNT	IDD
3	2	1	0
DSEL	CKSC	H16/$\overline{8}$	SCKS

3.7.10.1 BIT 7 HOST DMA

This bit reflects the state of the HDMA control bit defined in the auxilliary buffer control register.

3.7.10.2 BIT 6 HOST SLAVE / $\overline{\text{MASTER}}$

This bit reflects the state of the HSMB control bit defined in the auxilliary buffer control register.

3.7.10.3 BIT 5 BURST CONTINUOUS

This bit reflects the state of the BCNT control bit defined in the auxilliary buffer control register.

3.7.10.4 BIT 4 INTELLIGENT DRIVE DECODE

This bit reflects the state of the IDD control bit defined in the auxilliary buffer control register.

3.7.10.5 BIT 3 DRIVE SELECT

This bit reflects the state of the DSEL control bit defined in the auxilliary buffer control register.

3.7.10.6 BIT 2 CLOCK SOURCE

This bit indicates the source of the drive controller clock. If CKSRC = 1 and SCKS = 1, then the drive controller is being clocked by the buffer clock (BCLK). If CKSRC = 0 and SCKS = 0, then the drive controller is clocked by WCLK. If CKSRC = 1 and SCKS = 0 or CKSRC = 0 and SCKS = 1, then the clock source is undefined. CKSRC should not be checked until at least 10 clock periods after the SCKS has been written. The slower of BCLK and WCLK should be used in determining this delay.

3.7.10.7 BIT 1 HOST 16 / $\overline{8}$

This bit reflects the state of the H16/$\overline{8}$ control bit defined in the auxilliary buffer control register.

3.7.10.8 BIT 0 SYNCHRONOUS CLOCK SWITCH

This bit reflects the state of the SCKS control bit defined in the auxilliary buffer control register.

3.7.11 INTERFACE STATUS REGISTER (AD7 THRU AD0 = 38, READ)

This register is used to indicate the status of the WD42C22C. The bits are defined as follows:

Bit			
7	6	5	4
MINT	DCGI	RSTI	FEI
3	2	1	0
DCI	HPRI	DRQI	CWSI

3.7.11.1 BIT 7 MICROCONTROLLER INTERRUPT

This bit is high if the $\overline{\text{MCINT}}$ output pin is asserted. $\overline{\text{MCINT}}$ is the logical OR of seven sources:

- 1. A host SDH register write
- 2. A host soft reset
- 3. A FIFO error
- 4. The disk controller interrupt signal
- 5. The host transfer count interrupt flip-flop
- 6. The disk controller BDRQ signal
- 7. The command write/select interrupt flip-flop.

If any of the bits 6 through 0 are set, then the MCINT bit is high.

3.7.11.2 BIT 6 DRIVE CHANGE INTERRUPT

This bit sets when the host writes a new value to the SDH register bit 4 when AT mode is selected.

3.7.11.3 BIT 5 SOFT RESET INTERRUPT

This bit sets if the host initiates a soft reset. This bit resets by writing the proper bit in the interface control register.

3.7.11.4 BIT 4 FIFO ERROR INTERRUPT

This bit sets if a FIFO overrun or underrun condition occurs during host or disk transfers. It resets by writing the proper bit in the interface control register.

3.7.11.5 BIT 3 DISK CONTROLLER INTERRUPT

This bit reflects the state of the disk controller interrupt signal. This interrupt occurs at the end of a command. This bit resets either when the disk controller status (port 27_{16}) is read or when the disk controller command (port 27_{16}) register is written.

3.7.11.6 BIT 2 HOST POINTER READY INTERRUPT

This bit reflects the state of the host transfer count interrupt flip-flop. This interrupt sets when the host

transfer counter reaches zero and the FIFO is empty if the host pointer is not armed. It is also set when the host pointer pipeline register is loaded into the host pointer counter. It resets by writing the proper bit in the interface control register.

3.7.11.7 BIT 1 DISK BDRQ INTERRUPT

This bit reflects the state of the disk controller BDRQ signal. It sets when the disk controller starts a transfer between the disk controller and the sector buffer. It resets by writing the proper bit in the interface control register. If ADBP = 0 (bit 0 in the buffer control register, 37_{16}) when this bit first goes from 0 to 1, then DRQI and MCINT is not reset until after the microcontroller writes ADBP = 1.

3.7.11.8 BIT 0 COMMAND WRITE / SELECT / SLAVE INTERRUPT

This bit informs the local microcontroller that a command has been written if the WD42C22C is in AT mode, that the WD42C22C has been

selected if it is in XT mode, or that the slave host device has issued an interrupt if in slave host mode. (Asserts INTRQ. A slave interrupt only triggers on rising edge of INTRQ.) This bit resets by writing the proper bit in the interface control register.

3.7.12 INTERFACE CONTROL REGISTER (AD7 THRU AD0 = 38, WRITE)

This register is used to control various parts of the WD42C22C. The bits are defined as follows:

Bit			
7	**6**	**5**	**4**
SIRQ	RDCI	RSRI	RFEI
3	**2**	**1**	**0**
RBSY	RHRI	RDQI	RCWS

3.7.12.1 BIT 7 SET INTERRUPT

Writing a 1 to this bit generates a host interrupt if interrupts are enabled.

3.7.12.2 BIT 6 RESET DRIVE CHANGE INTERRUPT

Writing a 1 to this bit resets the host SDH write interrupt flip-flop.

3.7.12.3 BIT 5 RESET SOFT RESET INTERRUPT

Writing a 1 to this bit resets the soft reset interrupt flip-flop. In AT mode, the microcontroller must wait for the RST bit (2) in the FDR register ($3F_{16}$) to be reset by the host before this interrupt can be reset.

3.7.12.4 BIT 4 RESET FIFO ERROR INTERRUPT

Writing a 1 to this bit resets the FIFO error interrupt flip-flop.

3.7.12.5 BIT 3 RESET BUSY

Writing a 1 to this bit resets the BSY status bit in the hardware status register if XT mode is selected or it resets the ABSY status bit in the host status register if AT mode is selected. In AT mode, this bit should only be set at the very end of a command after the last DRQ is asserted to the host. Internal logic handles ABSY during buffer transfers to the host.

3.7.12.6 BIT 2 RESET HOST POINTER READY INTERRUPT

Writing a 1 to this bit resets the host pointer ready interrupt flip-flop.

3.7.12.7 BIT 1 RESET DISK BDRQ INTERRUPT

Writing a 1 to this bit resets the disk BDRQ interrupt flip-flop.

3.7.12.8 BIT 0 RESET COMMAND WRITE / SELECT / SLAVE INTERRUPT

Writing a 1 to this bit resets the command write/select/slave interrupt flip-flop.

3.7.13 CONFIGURATION STATUS REGISTERS (LOW: AD7 THRU AD0 = 39, READ HIGH: AD7 THRU AD0 = 3A, READ)

The configuration status registers are used to read the configuration jumpers on buffer address pins. When in read configuration mode, the buffer address lines have 300 µA current source pulldowns enabled. If there is no external pullup

resistor on the buffer address line, then the state of the line is read as a 0. If a 13K external pullup resistor is connected to a buffer address line, then the state of the line is read as a 1. The configuration registers should not be read until 100 µsec after enabling read configuration mode, to allow the buffer address line voltages to reach their proper value. Register contents are undefined if not in read configuration mode.

Configuration status low							
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BA7 THRU BA0							
Configuration status high							
Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
0	BA14 THRU BA8						

3.7.14 DRIVE INTERFACE STATUS (AD7 THRU AD0 = 3B, READ)

This register gives status information for the drive controller. It is coded as follows:

Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDC	DRDY	WF	HDS	MAC	DRQ	IPOL	DSN

3.7.14.1 BIT 7 RESET DRIVE CONTROLLER

This bit reflects the state of the reset drive controller control bit defined in the drive interface control register.

3.7.14.2 BIT 6 DRIVE READY

This bit is set if the $\overline{\text{DRDY}}$ input is asserted by the drive. It can always be read by the local microcontroller regardless of the state of disk controller busy.

3.7.14.3 BIT 5 WRITE FAULT

This bit is set if the $\overline{\text{WF}}$ input is asserted by the drive. It is always valid.

3.7.14.4 BIT 4 HOST DRIVE SELECT

This bit reflects the state of bit 4 of register 46_{16}, the host copy of the SDH register. It is used by the host in AT mode as a drive select. If HDS = 0, then drive 1 is selected. If HDS = 1, then drive 2 is selected. This bit is always accessable to the microcontroller regardless of the state of ABSY.

3.7.14.5 BIT 3 MICROCONTROLLER ACCESS CONTROL

This bit reflects the state of the microcontroller access control bit defined in the drive interface control register.

3.7.14.6 BIT 2 DISABLE RESET OUTPUT

This bit reflects the state of the disable reset output control bit defined in the drive interface control register.

3.7.14.7 BIT 1 INPUT POLARITY

This bit reflects the state of the input polarity control bit defined in the drive interface control register.

3.7.14.8 BIT 0 DISABLE SECTOR NUMBER

This bit reflects the state of the disable sector number control bit defined in the drive interface control register.

3.7.15 DRIVE INTERFACE CONTROL (AD7 THRU AD0 = 3B, WRITE)

This register is used to control the drive controller. It is coded as follows:

Bit							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RDC	X	X	X	MAC	DRQ	IPOL	DSN

3.7.15.1 BIT 7 RESET DRIVE CONTROLLER

When this bit is asserted, then the drive controller subsection of the WD42C22C resets. It is held reset as long as the bit is asserted. This bit is reset when $\overline{\text{RESET}}$ is asserted.

3.7.15.2 BIT 3 MICROCONTROLLER ACCESS CONTROL

When this bit is set, the microcontroller is tied to the buffer RAM through the disk controller's port. The microcontroller can then read or write the buffer by reading from or writing to the RAM access port (36_{16}). The DRWB bit in the buffer manager control port should be set to the proper

state before this bit is set. When MAC = 1, then the disk controller task file (registers 21_{16} through 27_{16}) cannot be accessed by the microcontroller. If the microcontroller writes to these registers when MAC = 1, then the disk controller may not act properly. This bit resets when RESET is asserted. The proper sequence for the microcontroller to read/write the RAM is defined under the buffer manager description.

3.7.15.3 BIT 2 DISABLE RESET OUTPUT

When this bit is set, all host initiated soft resets are disabled. Instead of the RESET line being asserted on soft reset, only the MCINT line is asserted. It is the responsibility of the local microcontroller to properly reset the board hardware when this bit is set. This bit resets only during power-up.

3.7.15.4 BIT 1 INPUT POLARITY

This bit is used to control the polarity of the INDEX, SCT, WF, and DRDY inputs. If IPOL= 0, the default, then the inputs are active low. If IPOL = 1, then the inputs are active high. In soft sector MFM and RLL modes, DRUN is always active high regardless of the state of IPOL.

3.7.15.5 BIT 0 DISABLE SECTOR NUMBER

When this bit is set, then the drive controller does not compare the sector number coming from the drive with the desired sector number when reads or writes are performed. The drive controller instead writes the sector number coming from the drive into the sector number register in the drive controller task file. At the end of each sector, just prior to issuing DRQI or DCI, the drive controller always writes the sector number to the alternate sector number register. This bit resets when RESET is asserted.

3.7.16 ALTERNATE SECTOR NUMBER (AD7 THRU AD0 = 3C, READ)

When the disk controller interrupts the microcontroller, this register holds the sector number of the sector just read or written. It is always updated just prior to the disk BDRQ interrupt (DRQI) or the disk controller interrupt (DCI). It is initialized to FF_{16} at the start of every command. It is written regardless of the state of the DSN bit described above.

Bit							
7	6	5	4	3	2	1	0
NUMBER OF LAST SECTOR READ OR WRITTEN							

3.8 AT INTERFACE PORTS

3.8.1 AT CONTROL REGISTER (AD7 THRU AD0 = 2A, READ/WRITE)

This register controls the new auto-DRQ option for write, write long, and format commands.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	0	0	ADQ7	ADRQ

3.8.1.1 BITS 7 THROUGH 2 RESERVED

Set to 0.

3.8.1.2 BIT 1 AUTO-DRQ 7 BYTE ECC

When ADRQ = 1 and ADQ = 1, then 7 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 1 and ADQ7 = 0, then 4 ECC bytes are transferred to/from the host on a read long or write long command. When ADRQ = 0, then the ECC7 bit in the fixed disk register ($3F_{16}$) controls the number of ECC bytes transferred on read long and write long commands.

3.8.1.3 BIT 0 AUTO-DRQ ENABLE

When ADRQ = 1 in AT mode, then the WD42C22C automatically sets up the first data transfer from the host for write, write long, and format commands. When ADRQ = 0, the local microcontroller must set up all data transfers to/from the host for all commands.

3.8.2 DRIVE ZERO STATUS (AD7 THRU AD0 = 3D, READ/WRITE)

In PC/AT mode, bits 6, 5, 4, 2, and 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register are set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 0. The other bits of the host status are not affected by this register.

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3.8.3 DRIVE ONE STATUS (AD7 THRU AD0 = 3E, READ/WRITE)

In AT mode, bits 6, 5, 4, 2, and bit 0 of the host status register are controlled by the local microcontroller. Bits 6, 5, 4, 2, and 0 of the host status register is set to the values of bits 6, 5, 4, 2, and 0, respectively, of this register if bit 4 of the AT task file copy SDH register (port 46 for microcontroller, port 6 for host) is 1. The other bits of the host status are not affected by this register.

3.8.4 FIXED DISK REGISTER (AD7 THRU AD0 = 3F, READ)

This register contains the fixed disk register data written by the host.

Bit							
7	6	5	4	3	2	1	0
0	0	0	0	HS3EN	RST	$\overline{IEN}$	0

3.8.5 DIGITAL INPUT REGISTER (AD7 THRU AD0 = 3F, WRITE)

Bit 5 of this register is written by the local microcontroller and read by the host if the fixed disk register bit 3 is zero. This bit is inverted when this register is read by the host. If HS3EN is one, then bit 5 of this register comes from SDH register bit 3.

Bit							
7	6	5	4	3	2	1	0
ECCM	ECC7/ DDRQ	RWC	X	X	X	DS1	DS0

3.8.5.1 BIT 7 ECC MODE

In PC/AT mode, ECCMOD = 1 indicates that the data transferred to the host includes ECC. The ECC is transferred in bytes rather than in words. This bit is reset when $\overline{RESET}$ is asserted. This bit should not be set in XT or slave host modes.

3.8.5.2 BIT 6 ECC 7 BYTES/ DISABLE BDRQ

When ECCM = 1, then this bit determines the number of ECC bytes transferred to the host. If ECC7 = 1, then 7 bytes are transferred. Otherwise, 4 bytes are transferred. If ECCM = 0, then this bit controls whether or not the drive controller issues BDRQ interrupts. If DDRQ = 0, then the drive controller issues BDRQ interrupts. If DDRQ = 1, then the drive controller does not issue BDRQ interrupts. It should be noted that when BDRQ occurs, the buffer manager loads the disk pointer from its pipeline register and when no BDRQ occurs then the disk pointer keeps incrementing from one sector to the next. This bit resets when $\overline{RESET}$ is asserted.

3.8.5.3 BIT 5 REDUCE WRITE CURRENT

This bit is set by the microcontroller and indicates the state of the $\overline{RWC}$ signal going to the drive.

3.8.5.4 BIT 1 DRIVE SELECT 1

This bit controls the state of the $\overline{DS1}$ output pin. When DS1 = 0, then the $\overline{DS1}$ output is tri-stated and when DS1 = 1 the $\overline{DS1}$ output is low. This bit is reset when $\overline{RESET}$ is asserted.

3.8.5.5 BIT 0 DRIVE SELECT 0

This bit controls the state of the $\overline{DS0}$ output pin. When DS0 = 0, then the $\overline{DS0}$ output is tri-stated and when DS0 = 1 the the $\overline{DS0}$ output is low. This bit is reset when $\overline{RESET}$ is asserted.

3.8.6 AT TASK FILE COPY (AD7 THRU AD0 = 40 THRU 47, READ/WRITE)

These registers are a copy of the disk controller task file. They are loaded by the host prior to the start of a command. The local microcontroller must read the command and interpret it and then copy the appropriate parameters from this task file copy to the actual drive controller task file (20_{16}-27_{16}). At the end of the command, the local microcontroller must update this task file copy before asserting INTRQ and resetting ABSY. The local microcontroller can only access these registers when ABSY=1.

4.0 BUFFER MANAGER ORGANIZATION

The buffer manager can control multiple sector buffers totalling up to 32 Kbytes. The buffer interface requires static RAMs. The sector buffers can be any size up to 2055 bytes, including ECC, and can be located at any byte boundary. The buffer manager has two address counters, one for the host interface and one for the disk data buffer. Both counters can access the SRAM simultaneously. The buffer manager handles the arbitration between the host interface and the drive controller. There is a FIFO in the host data interface that allows a sustained bandwidth of 4 Mwords/sec (8 Mbytes/sec) for 16-bit wide transfers and 8 Mbytes/sec for 8-bit wide transfers. The buffer manager can sustain a RAM bandwidth of 10 Mbytes/sec.

When the local microcontroller wants to access the buffer RAM, it has to use the disk buffer manager logic. It first loads the desired starting address into the disk buffer pointer. The proper buffer manager control bits are then set to enable the local microcontroller access to the buffer. When the local microcontroller accesses the special RAM access port (register 36_{16}), the data is read/written through the disk controller's FIFO port to the buffer. The RAM can only be accessed sequentially from the starting address and only in one direction as set by the DRWB control bit in the buffer control register.

Both address counters are pipelined. There are registers that can be loaded with the starting address of the next sector buffer while the current buffer is transferring. This allows noncontiguous buffers to be chained without any loss of RAM bandwidth between sectors.

4.1 ACCESSING BUFFER RAM FROM THE MICRO-CONTROLLER

The microcontroller can read and write the buffer RAM. To read the buffer RAM the procedure is:

1. Set DRWB = 1 (bit 2) in the buffer manager control Register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

The buffer manager begins reading data out of the RAM starting at the address specified in the disk pointer register and placing it into the FIFO. As the microcontroller reads from the RAM access port (36_{16}), sequential bytes from the buffer are transferred from the FIFO to the microcontroller.

The procedure to write to the buffer RAM is:

1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
2. Set MAC = 1 (bit 3) in the disk controller control register ($3B_{16}$).
3. Load the starting address of the data being accessed into the disk buffer pointer registers (34 & 35_{16}).
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).

As the microcontroller writes data to the RAM access port (36_{16}), the buffer manager transfers the bytes to sequential locations in the buffer RAM starting at the address specified in the disk pointer register.

NOTE

DRWB should not be changed while MAC = 1.

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4.2 STARTING HOST TRANSFERS TO/FROM BUFFER RAM

Host transfers can be performed in several modes. The modes available and the setup required to establish each mode are as follows:

HDMA	BDEN	BCNT	H16/8-
1	0	X	0
8-bit wide single byte DMA			
1	0	X	1
16-bit wide single word DMA			
1	1	0	0
8-bit wide, 8-byte burst DMA			
1	1	0	1
16-bit wide, 16-byte burst DMA			
1	1	1	0
8-bit wide, continuous burst DMA			
1	1	1	1
16-bit wide, continuous burst DMA			
0	X	X	0
8-bit wide PIO			
0	X	X	1
16-bit wide PIO			

Bits HDMA (bit 7), BCNT(bit 5), and H16/$\overline{8}$ (bit 1) are in the auxilliary buffer manager control register ($2F_{16}$) and bit BDEN (bit 1) is in the buffer manager control register (37_{16}). All of these modes are available in both the XT and AT host configurations. All of the DMA modes are available in the slave host configuration.

To perform a Host read data transfer the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 1 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16}).
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and sets REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.
6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.
7. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is be asserted.
8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors, then go to 3.
9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

To perform a host write data transfer, the following sequence should be followed.

1. Set up the appropriate transfer mode as described above.
2. Set HRWB = 0 (bit 3) in the buffer control register (37_{16}).
3. Load the starting address of the desired sector into the host pointer registers (30_{16} & 31_{16}). Load the number of bytes into the host transfer count registers (32_{16} & 33_{16})
4. Set AHBP = 1 (bit 4) in the buffer manager control register (37_{16}). Hardware automatically sets DRQ (bit 3) and resets ABSY (bit 7) in the host status register if AT mode and set REQ (bit 0) in the hardware status register if XT mode. If DMA transfers are enabled, then the hardware automatically starts the DMA handshake when AHBP is set by the micro-controller.
5. Wait for HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.

6. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If chaining and still more sectors then go to 3.

7. Wait for second HPRI = 1 (bit 2) in the interface status register (38_{16}). $\overline{\text{MCINT}}$ is asserted.

8. Set RHRI = 1 (bit 2) in the interface control register (38_{16}) to reset the interrupt. If still more sectors then go to 3.

9. Set RBSY = 1 (bit 3) in the interface control register when the entire command sequence is complete. This resets the ABSY and XBSY host status bits. They stay reset until the next command is issued by the host.

4.3 CONTROLLER COMMANDS

The WD42C22C Winchester command set contains twelve commands. Four commands (read sector, write sector, format, and set parameter) are directly executed through the command register. The remaining commands are not directly available to the host. These commands may be executed by the local microcontroller transparently to the host. Table 12 lists the commands and command codes.

COMMAND	7	6	5	4	3	2	1	0
Read Sector	0	0	1	0	0	M	L	T
Read Next Data	0	1	1	0	0	0	L	1
Write Sector	0	0	1	1	X	M	L	T
Write ID	1	0	1	1	F	0	A	T
Scan ID	0	1	0	0	0	0	0	T
Format Track	0	1	0	1	0	0	W	1
Format Single Sector	1	1	0	1	0	0	W	1
Compute Correction	0	0	0	0	1	P	0	0
Set Parameter	Z	0	0	R	0	E	H	S
Load Parameter Block	1	0	0	0	1	D	K	U
Sleep	1	0	0	1	1	0	0	0
Dump	1	0	1	0	I	B	L	1

TABLE 12. COMMAND AND COMMAND CODES

Mnemonic definitions for Table 12:

- M=0 Single sector read or write. Sector count is ignored.
  M=1 Multiple sector read or write. Used for 1:1 interleave.
- L=0 Normal mode, selected ECC or CRC functions performed.
  L=1 Sector extended by 4 or 7 bytes (depends on set parameter command. No ECC generated or checked.
- T=0 Enable retries.
  T=1 Disable retries.
- X=0 Write sector specified in sector number register.
  X=1 Write sector specified in first byte of the sector buffer.
- F=0 Write new ID immediately after current ID.
  F=1 Write new ID offset from current ID.
- A=0 Do not pulse AME when writing new ID.
  A=1 Pulse AME when writing new ID.
- W=0 Write gate stays asserted for entire track or sector.
  W=1 Write gate deasserted over all gaps during format.
- P=0 Transfer syndrome bytes to buffer and calculate error pattern bytes and transfer them to the buffer.
  P=1 Transfer syndrome bytes to the buffer but do not calculate error pattern bytes.
- Z=0 MFM or RLL mode.
  Z=1 NRZ mode. Mode used for ESDI drive interface.
- R=0 Disable relocation ID searches.
  R=1 Enable relocation ID searches.
- E=0 Sector extension for read long/write long 4 bytes. ECC generator/checker is 4 bytes.
  E=1 Sector extension for read long/write long 7 bytes. ECC generator/checker is 7 bytes.
- H=0 SDH register programmed for 3 head select bits.
  H=1 SDH register programmed for 4 head select bits.
- S=0 Error correction span 5 bits with 4 byte ECC or 11 bits with 7 byte ECC.
  S=1 Error correction span 11 bits with 4 byte ECC or 22 bits with 7 byte ECC.
- D=0 Select soft sector drive interface. Default after master reset.
  D=1 Select hard sector drive interface. In

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MODE	MODE CONTROL			OPTIONS														
	Z	D	K	M	T	L	X	A	F	R	S	E	H	P	U	W	I	B
RLL soft sector	?	0	0	x	x	x	x	x	x	x	x	*	x	x	x			
RLL hard sector	?	1	0	x	x	x	x	x	x	x	x	*	x	x	x	x	x	x
MFM soft sector	0	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
MFM hard sector	0	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
NRZ soft sector	1	0	1	x	x	x	x	x	x	x	x	x	x	x	x			
NRZ hard sector	1	1	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

? Don't care, could be 0 or 1.
x These options are supported.
* These options have no effect.

TABLE 13. OPTION SUMMARY TABLE

this mode, DRUN becomes a sector pulse input.

- K=0 RLL data interface. Selection of this option disables the NRZ option. Defaults to this setting after master reset.

  K=1 Data interface is either MFM or NRZ.

- U=0 Use the standard sector sizes defined under the SDH register description.

  U=1 Select user defined sector size. The desired sector size is put into the cylinder registers prior to issuing a load parameter block command. The auxilliary set parameter command transfers the desired sector size from the cylinder registers to an internal sector size register.

- I=0 Dump two fields per sector. Dump 5 ID bytes and the number of data bytes set by the sector size.

  i=1 Dump only one field per sector. The sizeof the field is set by the sector size and type of field (ID versus data) is controlled by where RG is asserted.

- B=0 FE sync byte and zero preset CRC.

  B=1 A1 sync byte and ones preset CRC.

Table 13 summarizes the data formats and options supported by these formats.

4.4 COMMAND DESCRIPTIONS

4.4.1 READ SECTOR

If M = 0, then the sector specified in sector number register is read. If M = 1, then multiple records are read. If the sector count register = 0, then 256 sectors are read at the desired track.

If T=0, then ID searches are retried for 10 index pulses. DAM not found errors are not retried. There are no retries for CRC/ECC errors. If T=1, ID searches are retried for two index pulses.

If L=0, then normal CRC or ECC read commands are performed. If L=1, then the CRC or ECC check bytes are not computed but instead the CRC or ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 4 or 7 bytes. If ECC and retry modes have been selected and a data field error occurs there are no attempts to correct the data.

A bad block mark in the ID field sets the error bit and the data field is not read. If the R option in the set parameter command is set then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately

even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector umber where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of Cylinder where sector has been relocated
26	Head number of relocated sector

If DSN = 1 (bit 0) in the drive interface control register ($3B_{16}$) than the sector number is not compared when ID searches are performed. The WD42C22A reads the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be read into the buffer in one revolution.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue read command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number, and sector size code.
  10. When the proper sector ID is found, read sector data and place in buffer.
  11. Write sector number to alternate sector number register. If M = 0, then go to 10.
  12. Decrement sector count, increment sector number. If M = 1, and sector count = 0 then go to 13 else go to step 8.
  13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if ID field not found or if ID field matches, but CRC check fails, and after retry procedure.
- Bad block set if attempt was made to read a sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.
- Data CRC/ECC set if data field CRC or ECC check fails. No attempt is made to correct ECC errors.
- Data AM not found in set if data address mark not found.

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4.4.2 READ NEXT DATA

The read next data command finds the next data field and places it in a buffer. If the WD42C22C detects that the drive number changed since the last read command, then an auto-scan ID is performed and step pulses are issued to update the present cylinder position.

All searches for a data field are retried for two index pulses, but if a data ECC error is detected there are no retries. If after reading the correct ID field, the data address mark is not found a DAM error is set.

The L flag controls the ECC check bytes. If L=0, then the data field is read and ECC is checked. If L=1, then the ECC check bytes are not computed. Instead, the ECC check bytes are loaded into the buffer immediately after the data field. The external sector buffer must be long enough to hold the additional 7 bytes.

NOTE

This command supports only soft sector MFM and RLL mode and is implemented for backward compatibility with the WD5011 and WD5011A.

Command Flow :

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  4. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  5. Set MAC=0 in the drive interface control register.
  6. Issue read next data command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Set DRQ status bit, activate BDRQ signal to buffer manager. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Find next data field, read sector data and place in buffer. If data mark error, try data field search again until 2 index pulses occur.
  10. Copy sector number register to alternate sector number register ($3C_{16}$). Set DCI (bit 3) in the interface status register (38_{16}). MCINT is asserted.
- MICRO:
  11. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- Data CRC/ECC set if data field CRC or ECC check fails. No correction is attempted.
- Data AM not found is set if data address mark not found after 2 index pulses of looking for any data field.

4.4.3 WRITE SECTOR

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write total number of sectors specified by sector count register if M = 1. Sectors are written in numerical order. If M = 0, then sector count is ignored and only one sector is written. The data field PLO sync field is nominally 12 bytes long but is extended by the PLO register.

If T = 0, then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If L = 0, then normal CRC or ECC write sector commands are performed. If L = 1, then the CRC or ECC check bytes are not computed and written

to the disk but instead, 4 or 7 additional bytes are read from the buffer and written to the disk immediately after the data field.

If X = 0, then the controller searches for the sector number in the sector number register and increments the sector number register and the end of each sector if M = 1. If X = 1, then the controller searches for the sector specified in the first byte of the sector buffer. The controller reloads the sector number register from the first byte of each subsequent sector buffer if M = 1. This allows a track formatted with interleave to be written in one revolution.

A bad block mark in the ID field sets the error bit and the data field is not be written. If the R option in the set parameter command is set, then the controller searches immediately after the normal ID field for a special ID field containing mapping information and a special "Relocation ID" flag bit. The RIDF bit in the error register sets if this special ID field is found. If a bad block mark is found in an ID field then the command terminates immediately even if more sectors remain to be read. The task file contents when a bad block bit is detected and the R option is used is as follows:

REGISTER	MEANING
22	Sector number of sector with bad block bit set
23	Sector number where sector has been relocated
24	LSB of cylinder number where sector has been relocated
25	MS bits of cylinder where sector has been relocated
26	Head number where sector has been relocated

If DSN = 1(bit 0) in the drive interface control register ($3B_{16}$) then the sector number is not compared when ID searches are performed. The WD42C22C writes the sector as long as the cylinder and head numbers match the desired values. This allows an interleaved track to be written into the buffer in one revolution. This option is only useful when doing the initial write-after-format to place 00 in the data fields.

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the first sector into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue write command to WD42C22C.
- WD42C22C:
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQ is enabled.) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Load starting address of next sector buffer into disk buffer pointer register. Set ADBP=1 in buffer manager control register if more sectors remaining. Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Search for head, cylinder, sector number and sector size code.
  10. When the proper sector ID is found, write buffer data to sector.
  11. Write sector number to alternate sector number register ($3C_{16}$). If M = 0 then go to 13.
  12. Decrement sector count, increment sector number. If M = 1 and sector count = 0

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then go to 13 else go to step 8.

13. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

- MICRO:

14. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if write sector attempted on any sector with bad block mark.
- Relocation ID found if R option enabled and relocation ID detected.

4.4.4 WRITE ID

Write from buffer to disk when BRDY signal is activated by the buffer manager. Write 4 bytes to create an ID field. The PLO sync field prior to this new ID field is nominally 12 bytes long but is extended by the PLO register. A value of 0 results in a 2048 byte PLO field and should not be used.

If T = 0 then ID searches are retried for 10 index pulses. If T = 1, then ID searches are retried for 2 index pulses only.

If F = 0, then the new ID is written immediately after the ID field of the desired sector. If F = 1, then the new ID field is written offset from the desired sector ID with the offset determined by the internal sector size register. A load parameter block command will have to be issued to set the offset value and another load parameter block will be needed to set the sector size back to the correct value if the programmable sector size option is being used. An offset of up to 2048 is allowed. This option can be used to reformat a single sector in soft sector mode.

If A = 0, then the AME output is held low during the write ID command. If A = 1, then the AME output is pulsed at the start of the PLO field before the new ID being written. This option, together with the F option, can be used to reformat a single sector in soft sector NRZ mode.

The four bytes in the buffer (F = 0) should be as follows:

BYTE 0: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 1: Low byte of cylinder number

BYTE 2: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 3: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

The five bytes in the buffer (F = 1) should be as follows:

BYTE 0: Sector Number

BYTE 1: 1 1 1 1 $\overline{\text{cyl 10}}$ 1 $\overline{\text{cyl 9}}$ cyl 8

BYTE 2: Low byte of cylinder number

BYTE 3: BB 0 RF 0 HS3 HS2 HS1 HS0

BYTE 4: Sector Number

BB = bad block flag

RF = Relocation ID flag

$\overline{\text{cyl 10}}$ thru cyl 8 = upper three cylinder number bits

HS3 thru HS0 = head select bits

RF should be set to 1 if the new ID being written is to be a special relocation ID for mapping a defective sector to a new position.

Command Flow:

- MICRO:

1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
2. Load the starting address of the ID buffer data into the disk buffer pointer registers (34_{16} & 35_{16}).
3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive

interface control register ($3B_{16}$) to disable DRQI, if desired.

4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC = 0 in the drive interface control register.
6. Issue Write ID command to WD42C22C.

• WD42C22C: 7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.

8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.

• MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).

• WD42C22C: 9. Search for head, cylinder, sector number and sector size code.

10. When the proper sector ID is found, write buffer data to sector.

• WD42C22C:11. Write sector number to alternate sector number register. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO: 12. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write Fault and aborted command set if WF pin activated.
- ID not Found set if exact ID field not found or if ID field matches but CRC check fails, after retry procedure.
- Bad Block set if bad block bit detected in ID of desired sector.

4.4.5 SCAN ID

When the next ID field of the present track is encountered, cylinder number, sector size, head number and sector number are loaded into the respective registers.

Command Flow:

• MICRO: 1. Issue Scan ID command to WD42C22C.

• WD42C22C 2. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.

3. Search for next ID field and read 4 ID bytes into respective registers. Search for ID field for up to 10 index pulses if T=0, up to 2 index pulses if T=1.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO: 5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin active.
- Bad Block set if bad block mark detected.
- ID not found if no ID fields are found.
- Relocation ID found if R option enabled and relocation ID detected.

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4.4.6 FORMAT TRACK

This command formats one track using parameters loaded in the task registers file and in buffer memory.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector numbers are taken from buffer memory. The total number of sectors formatted is specified by the sector count register. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register if B = 1. The data PLO field length is 12 bytes during format.

The data placed in the gaps comes from an internal register loaded during the load parameter

block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector addresses have been loaded into the buffer then the command register is loaded with the format command. When the BRDY signal is activated by the buffer manager, the specified number of sectors are written. The block marks and sector numbers are read from the buffer as needed. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

Write Gate is turned on and off within 4 bit times after index if NRZ or hard sector mode is selected or within 6 bit times otherwise. In RLL mode, Gap1/Gap3 data should be programmed to be 33_{16} with the load parameter command. The W option controls the state of WRITE GATE over the gaps. If W=1, WRITE GATE turns off over the gaps.

The sum of the number of bytes in both the Gap1/Gap3 and ID PLO field must be greater than or equal to 25 bytes to achieve 1:1 interleave.

The interleave table contains the bad block marks and sector numbers for the track. If there is a bad sector and it is desired for the controller to just skip over it, then the bad block mark for that sector position should be set to 80_{16} and the sector number for that sector should be set to FF_{16}. If it is desired to map the bad sector then the bad block mark for that sector should be set to 80_{16} and the sector number for that sector should be set to the correct value for that position in the interleave table. The R and U options should be set in the set parameter and load parameter block commands. A write ID command then places the relocation information for that sector onto the drive.

The interleave table format is:

- BYTE 0: 1st sector's block mark (00_{16} or 80_{16})
- BYTE 1: 1st sector's sector number
- BYTE 2: 2nd sector's block mark (00_{16} or 80_{16})
- BYTE 3: 2nd sector's sector number

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- BYTE 2n: nth sector's block mark (00_{16} or 80_{16})
- BYTE 2n+1: nth sector's sector number

Command Flow:

- MICRO:
  1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16})
  2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the buffer control register.
  6. Issue format command to WD42C22C.
- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Write gap.
  10. Write sector ID using parameters in task register file

and buffer memory. Data bytes are FF.

11. Decrement sector count register. If sector count = 0, then go to step 12, else go to step 9.
12. Write Gap until leading edge of index pulse.
13. De-assert Write Gate.
14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.

• MICRO: 15. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

Note

Gap length written on disk is 3 bytes longer than gap value specified in sector number register.

4.4.7 FORMAT SINGLE SECTOR

This command formats one sector using parameters loaded in the task register file and in buffer memory. This command only applicable to hard sector mode.

WRITE GATE is turned on and off within 4 bit times after index or sector if NRZ mode is selected or within 6 bit times otherwise. The W option controls the state of WRITE GATE over the gaps. Setting W to 1 turns off WRITE GATE over the gaps.

Cylinder, head, and sector size numbers are taken from the task register file. Good block/bad block marks and sector number are taken from buffer memory. The physical sector position to be formatted is specified by the sector count register. If sector count = 1, then the first sector after index is formatted. For sector count = 2, the second sector after index is formatted, and so on. The lengths of GAP 1 and GAP 3 are loaded into the sector number register. The length of the ID PLO sync field is loaded into the PLO length register.

The data placed in the gaps comes from an internal register loaded during the load parameter block command. The data placed into the pads comes from another internal register loaded during the load parameter block command.

After the task register file has been loaded with the desired format parameters and the block marks and sector number loaded into the buffer, then the command register is loaded with the format single sector command. When the BRDY pin is activated by the buffer manager, the controller then looks for the start of the desired sector. The bad block mark and sector number are read from the buffer. The data field is written with FF. CRC is automatically computed and written if in CRC mode. If in ECC mode, ECC check bytes are automatically computed and written after the data field. The number of ECC check bytes is determined by the E bit in the set parameter command.

The data for the buffer is:

- BYTE 0: bad block mark (00_{16} or 80_{16})
- BYTE 1: sector number of formatted sector.

Command Flow:

• MICRO:

1. Set DRWB = 1 (bit 2) in the buffer manager control register (37_{16}).
2. Load the starting address of the interleave table into the disk buffer pointer registers (34_{16} & 35_{16}).
3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
5. Set MAC=0 in the drive interface control register.
6. Issue format single sector command to WD42C22C.

• WD42C22C:

7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
8. (If DRQI is enabled) Activate BDRQ signal to buff-

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er manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer. Wait for leading edge of index.

- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C: 9. Decrement sector count. If sector count = 0 go to 11, else go to 10.
  10. Wait for SECTOR pulse, then go to 9.
  11. Assert WRITE GATE. Write gap.
- WD42C22C:12. Write sector ID using parameters in task register file and buffer memory. Data bytes are FF.
  13. Write gap until leading edge of SECTOR pulse.
  14. De-assert Write Gate.
  15. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 16. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.

4.4.8 COMPUTE CORRECTION

This command is used to compute the pattern and location of a single burst error. It is used after a read sector command has detected a data field ECC error. The compute correction command first writes the four or seven syndrome bytes into the buffer. It then processes the syndrome bytes to compute the error pattern and error location. The error location and error pattern bytes are written into the buffer. Either four or seven error pattern bytes are written to the buffer depending on the ECC length selected. The error pattern bytes are automatically byte aligned.

The P option is used to control whether or not the error pattern bytes are calculated. If P = 0, then the error pattern bytes are calculated and sent to the buffer. If P = 1, then the error pattern bytes are not calculated. Only the syndrome byte is transferred to the buffer. This option facilitates firmware algorithms that require a matching syndrome before a correction is made. In this case, the firmware calculates the error pattern, corrects the error, and saves the syndrome after initially detecting the error. Then, the firmware dumps and compares the syndrome on the second read of the same sector. An ECC error can now be corrected in one revolution of the disk compared to three revolutions required by earlier WD1010 and WD2010 based controllers.

The error pattern and error location bytes are not valid if the error is found to be uncorrectable. An uncorrectable error is indicated by the appropriate bits in the status and error register.

The buffer contents contains the following information:

- SYNDROME BYTE (MSB)
- SYNDROME BYTE
- SYNDROME BYTE
- SYNDROME BYTE (LSB if 4 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (if 7 byte ECC)
- SYNDROME BYTE (LSB if 7 byte ECC)
- BYTE OFFSET (MSB)
- BYTE OFFSET (LSB)
- ERROR PATTERN (MSB)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 4 byte ECC)
- ERROR PATTERN
- ERROR PATTERN
- ERROR PATTERN (LSB if 7 byte ECC)

If the byte offset is 0, then the first data byte of the sector should be exclusive OR'ed with the first error pattern byte (MSB). Each succeeding data byte exclusive OR'ed with the succeeding error pattern byte until the fourth data byte is exclusive OR'ed with the fourth error pattern byte (LSB). Exclusive OR the first two error pattern bytes for 5 bit spans. Exclusive OR the first three error pat-

tern bytes for 11 bit spans. Exclusive OR the first four error pattern bytes for the 22 bit span.

Command Flow:

- MICRO:
  1. Set DRWB=0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the error correction data buffer into the disk buffer pointer registers (34_{16} & 35_{16}).
  3. Set ECCM=0 (bit 7) and DDRQ =1 (bit 6) in the DIR write register ($3F_{16}$) and MAC=1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP=1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC=0 in the drive interface control register.
  6. Issue compute correction command to WD42C22C.
- WD42C22C:
  7. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY signal indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Transfer contents of the four (or seven) byte ECC register to buffer, most significant byte first.
  10. Clock the ECC register. Stop if correctable pattern found or if number of clocks exceeds sector size. If number of clocks exceeds sector size, set error bit of status register and ECC error of error register.
  11. Transfer byte count to buffer (2 bytes). Transfer 4 bytes of error pattern to buffer if 4 byte ECC. Transfer 7 bytes of error pattern 7 byte ECC.
  12. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  13. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- CRC/ECC flag set if data field error length exceeds correction span.

NOTE

Default 11 bit correction span after master reset if 7-byte ECC or 5 bit correction span if 4-byte ECC.

4.4.9 SET PARAMETER

The E bit is used to select either 4 byte or 7 byte sector extension for read long and write long commands. It also selects either a 4 or 7 byte internally generated ECC. A 7 byte sector extension and 7 byte ECC are the default after a master reset (due to RLL default). If E is 0, then a 4 byte sector extension and 4 byte ECC are selected if MFM or NRZ mode. If E is 1, then a 7 byte sector extension and 7 byte ECC are selected.

The H bit selects either 3 or 4 head select bits in the SDH register. If H=0, then 3 head select bits are written or compared in the ID fields on the drive. If H=1, then 4 head select bits are written or compared in the ID fields on the drive. The default after master reset is 3 head select bits.

The S bit is used to select either a 5 bit or 11 bit correction span if 4 byte ECC and an 11 bit or 22 bit correction span if 7 byte ECC. An 11 bit correction span for 7 byte ECC is the default parameter following master reset. If S is 0, then a 5 bit correction span is selected if 4 byte ECC, 11 bit correction span if 7 byte ECC. If S is 1, then an 11 bit correction span is selected if 4 byte ECC, 22 bit correction span if 7 byte ECC.

The Z bit is used to select MFM, RLL, or NRZ mode. If K=0 in the load parameter block command, then RLL coding is selected regardless of the state of Z. If Z is 0 and K is 1, then MFM coding is selected. If Z is 1 and K = 1, then NRZ coding is selected.

The R option is used to enable relocation ID searches. If R=1 for read and write sector com-

mands and a bad block mark is detected in the desired sector's ID, then the WD42C22C searches for a special ID field containing relocation information immediately after the desired sector's ID. This special ID field is placed using the write ID command. When the R option is used, then the U option must be set to 1 in the load parameter block command.

Command Flow:

- MICRO: 1. Issue set parameter command to WD42C22C.
- WD42C22A: 2. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
3. Set or reset internal parameter flip-flop.
4. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 5. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.10 LOAD PARAMETER BLOCK

The D bit is used to indicate the sectoring mode. If D = 0, the default after a master reset, then soft sector mode is selected. If D = 1, then hard sector mode is selected. In hard sector mode, the PLO length register is transferred to the internal GAP length register during the load parameter block command. This GAP register is used to control the delay from INDEX/SECTOR to READ GATE on.

The K bit selects the data interface mode. If K=0, the default after a reset, then RLL mode is selected. If K=1, then the interface is either MFM or NRZ as selected by the set parameter command.

The U bit selects the sector size options. If U=0, then the sector sizes are 128, 256, 512, and 1024 depending on the contents of the SDH register. If U=1, then the sector size is defined by the user. The cylinder registers are loaded with the desired sector size prior to issuing the load parameter block command.

In addition, the load parameter block command is used to load several internal parameters for format, read, and write commands. The task file is loaded with these parameters prior to the start of the command. The registers loaded and the corresponding parameters are:

REGISTER	PARAMETER
21	Delay from INDEX/SECTOR to RG
22	Data written in GAPS
23	Data written in PADS
24	LS byte of sector size, LS byte of offset for write ID command
25	3 MS bits of sector size, 3 MS bits of offset for write ID command

Command Flow:

- MICRO: 1. Load parameters into task file.
2. Issue load parameter block command to WD42C22C.
- WD42C22C: 3. Write FF to the alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
4. Set or reset internal parameter flip-flop.
5. Copy cylinder registers to internal sector size register. Copy PLO register to internal GAP register. Copy sector count register to internal GAP data register. Copy sector number register to internal PAD data register.
6. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO: 7. Read disk controller status register (27_{16}) and error register (21_{16}).

Error Flags:

- None.

4.4.11 SLEEP

The sleep command places the WD42C22C in a low power standby mode. When the sleep command is issued, the disk controller section clocks are disabled and only the buffer manager and host interface logic is enabled. The disk controller can be brought out of the sleep mode by setting RDC = 1 (bit 7) in the disk controller control register ($3B_{16}$) or by resetting the entire WD42C22C. The microcontroller should **NEVER** attempt to read or write the drive controller task file (registers 21_{16} through 27_{16}) while the drive controller is in the sleep mode.

Command Flow:

- MICRO: 1. Issue sleep command to WD42C22C.
- WD42C22C: 2. Write FF to the alternate sector number register ($3C_{16}$).
  3. Disable drive controller clocks.
- MICRO: 4. Wake up disk controller by setting RDC=1 or by resetting the WD42C22C.

Error Flags:

- None.
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4.4.12 DUMP

The dump command sends data off the media regardless of matching ID fields and regardless of the format. The command can dump an ID field, a data field, or both. Dump retrieves all the ID fields from index to index to determine the interleave. Dump can also read the ESDI standard defect list. The command dumps data starting at the first byte after the A1 sync byte for WD format or the first byte after the FE sync byte for ESDI format. This command can only do multisector dumps in hard sector mode.

The command is assumed to be a multisector command. To read just one sector as in an ESDI defect list read, then the sector count must be set to one. There are three options.

The I option controls the number of fields that are dumped for each sector. If I = 0, then two fields (ID and data) are dumped for each sector. If I = 1, then only one field is dumped for each sector. The type of field is determined by the read gate delay and the sector size. The sector size should be programmed to 1 less than the number of bytes to be dumped for the sector.

The B option controls the sync byte and CRC preset. If B = 0, then the sync byte is assumed to FE and the CRC is preset to all zeroes. If B = 1, then the sync byte is assumed to be A1 and the CRC is preset to all ones.

The L option selects either CRC or no CRC checking. If L = 0, then CRC is checked. If L = 1, then either four or seven check bytes are transferred to the buffer depending on the extension selected by the set parameter command. If L = 1, then I should also be set to 1. B does not affect the L option.

The PLO register controls the read gate delay for the first sector. READ GATE turns on x + 5 + CL bytes after the index pulse. Read gate for subsequent sectors is controlled as in normal read and write commands.

Use the dump command to read an ESDI defect list as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 255 for 256 byte sector.
3. Issue A1 command.

Use the dump command to dump the track interleave for WD format as follows:

1. Set PLO register = read gate delay - 5.
2. Set sector size = 4.
3. Set sector count = number of sectors per track.
4. Issue AD command.

Use the dump command to dump all the data fields on a track for WD format as follows:

1. Set PLO register = read gate delay to start of data PLO - 5.
2. Set sector size = actual number of bytes per sector.

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3. Set sector count = number of sectors per track.

4. Issue AF command or AB command.

In this case, the F8 second data sync byte is transferred to the buffer. The buffer requires one extra byte per sector.

One BRDQ interrupt occurs at the very beginning of the command. Therefore, the buffer must be contiguous and large enough to handle all the dumped sectors.

Command Flow:

- MICRO:
  1. Set DRWB = 0 (bit 2) in the buffer manager control register (37_{16}).
  2. Load the starting address of the buffer into the disk buffer pointer register (34_{16} & 35_{16}).
  3. Set ECCM = 0 (bit 7) and DDRQ = 1 (bit 6) in the DIR write register ($3F_{16}$) and MAC = 1 (bit 3) in the drive interface control register ($3B_{16}$) to disable DRQI, if desired.
  4. Set ADBP = 1 (bit 0) in the buffer manager control register (37_{16}).
  5. Set MAC = 0 in the drive interface control register.
  6. Issue dump command to WD42C22C.
- WD42C22C
  7. Write FF to alternate sector number register ($3C_{16}$). Abort if drive not ready or write fault.
  8. (If DRQI is enabled) Activate BDRQ signal to buffer manager and DRQI to microcontroller. Wait for BRDY indicating transfer of buffer pointer.
- MICRO: Set RDQI (bit 1) in the interface control register (38_{16}).
- WD42C22C:
  9. Wait for index.
  10. If I=1, then go to 12 else go to 11.
  11. Search for sync byte. When found, dump 5 data bytes into buffer.
  12. Search for sync byte. When found, dump programmed number of bytes into the buffer.
  13. Decrement sector count. If sector count = 0, then go to 14 else go to step 10.
  14. Set DCI (bit 3) in the interface status register (38_{16}). MCINT asserted.
- MICRO:
  15. Read disk controller status register (27_{16}) and errror register (21_{16}).

Error Flags:

- Drive not ready and aborted command set if drive not ready.
- Write fault and aborted command set if WF pin activated.
- ID not found set if I = 0 and index detected while searching for an ID field or if CRC of ID field doesn't zero.
- Data AM not found is set and index is detected while searching for a data field. If I=0 or when searching for either an ID or data field when I = 1.
- Data CRC if the data field CRC doesn't zero when I = 0 or if either an ID or data field CRC doesn't zero when I = 1.

5.0 ELECTRICAL AND TIMING SPECIFICATIONS

5.1 MAXIMUM RATINGS

V_{CC} with respect to V_{SS} (ground) ..... +5 V ± 5%

Max voltage on any pin with respect to V_{SS} ..... -0.5V to 5.5

Operating temperature (T_A) ..... 0°C (32°F) to 70°C (158°F)

Storage temperature ..... -55°C (-67°F) to 125°C (257°F)

NOTE

Maximum limits where permanent device damage occurs. Continuous operation at these limits is not intended and should be limited to those conditions specified in the DC operating characteristics.

5.2 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage		±10	µA	V_{IN} = 0.4 to V_{CC}
I_{OZ}	Tri-state and open drain output leakage		±10	µA	V_{OUT} = 0.4 TO V_{CC}
V_{IH}	Input High Voltage	2.0		V	
V_{IL}	Input Low Voltage		0.8	V	
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=2.0mA
I_{CC}	Supply Current		100	mA	All outputs open.
I_{CCS}	Supply Current (Standby Mode)		25	mA	All inputs at V_{DD} or V_{SS}, disk controller sleep mode, 15 MHz crystal.

TABLE 14. DC OPERATING CHARACTERISTICS

For pins 75 thru 82, 40 thru 42, 44 thru 48, 74, 8 (HD0 thru HD15, INTRQ, DREQ):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4		V	I_{OUT}=-5mA
V_{OL}	Output Low Voltage		0.4	V	I_{OUT}=12mA

For pin 8 ($\overline{IOCS16}$, AT PIO mode only):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=20.0mA

For pins 10, 11, and 12 (WD, EARLY, LATE):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OH}	Output High Voltage	2.4			I_O=-800µA
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0mA

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For pin 22 ($\overline{RESET}$)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=6.0 mA and VDD at spec. IO=2.0 mA and VDD at VRST2 max VRST3 max.

For pins 36, 37 ($\overline{DS0}$, $\overline{DS1}$):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{OL}	Output Low Voltage		0.4	V	I_O=48.0 mA

For pins 59-73 (BA0-B14)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PD}	Pulldown Current in read config. mode	40	160	µA	V_{OUT}=2.4V

For pins 5, 6, 9 ($\overline{HRE}$, $\overline{HWE}$, and $\overline{DACK}$ in slave host mode) and pins 40-42, 44-48 (HD8 through HD15 in 8-bit host mode):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{PU}	Pullup Current	100	2000	µA	V_{OUT}=0.4 V, V_{DD}=5.25 V

For pin 38 (XTALIN when driven by external osc.):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{IH}	Input High Voltage	3.5		V	
VIL	Input Low Voltage		1.0	V	

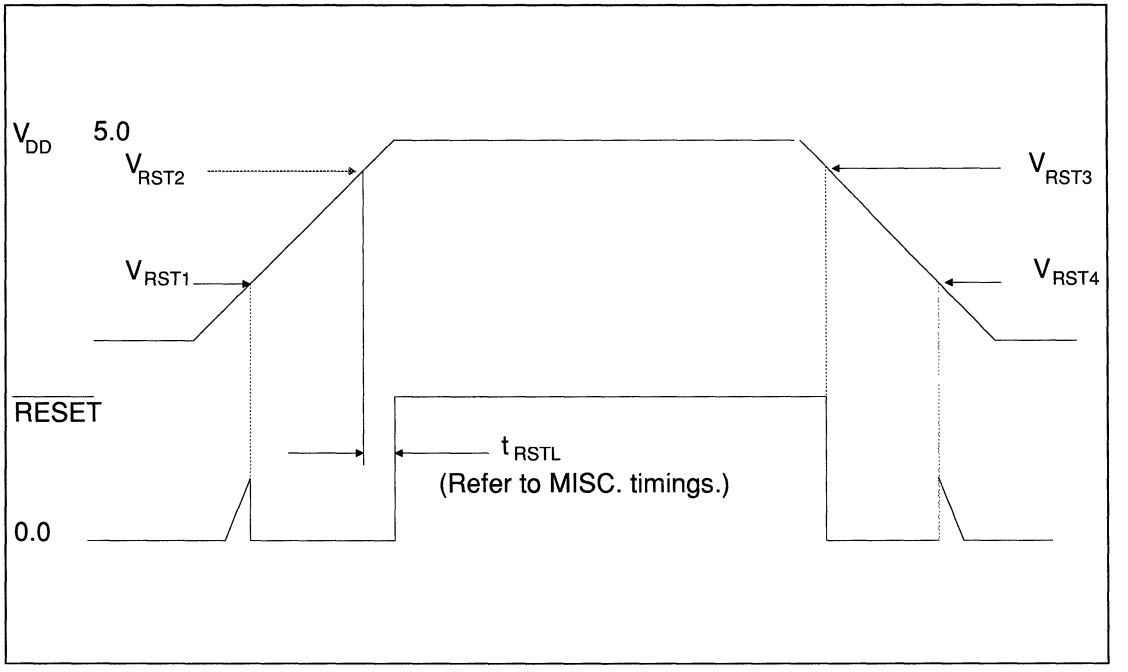

FIGURE 6. POWER QUALIFIED RESET VOLTAGE THRESHOLD

For pins 1-7, 9, 15, 16, 20, 21, 23, 25-35, 40-42, 44-48, 51-58, 59-73, 74, 75-82 (HA0-HA2, HA9, $\overline{HRE}$, HWE, HCS, DACK, INDEX, SCT, WF, DRDY, RESET, ALE, MRE, MWE, AD0-AD7, HD8-HD15, BD0-BD7, BA0-BA15, INTRQ, HD0-HD7)

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SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
VIH / VIL	Input Voltage Hysteresis	400		mV	

For pin 84 (V_{DD})

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
V_{RST1}	Power Qualified Reset Voltage Threshold	0.0	2.0	V	See Figure 7.
V_{RST2}		2.5	4.6	V	
V_{RST3}		2.5	4.6	V	
V_{RST4}		0.0	2.0	V	

5.3 AC TIMING CHARACTERISTICS

NOTE

Load capacitance=50 pF each for all other outputs. Timings must be derated for larger load capacitances.

For pins 14, 16, 17, 19 (WC, DRUN, RD, RC):

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{RS}	Rise Time		10	nsec	10% to 90%

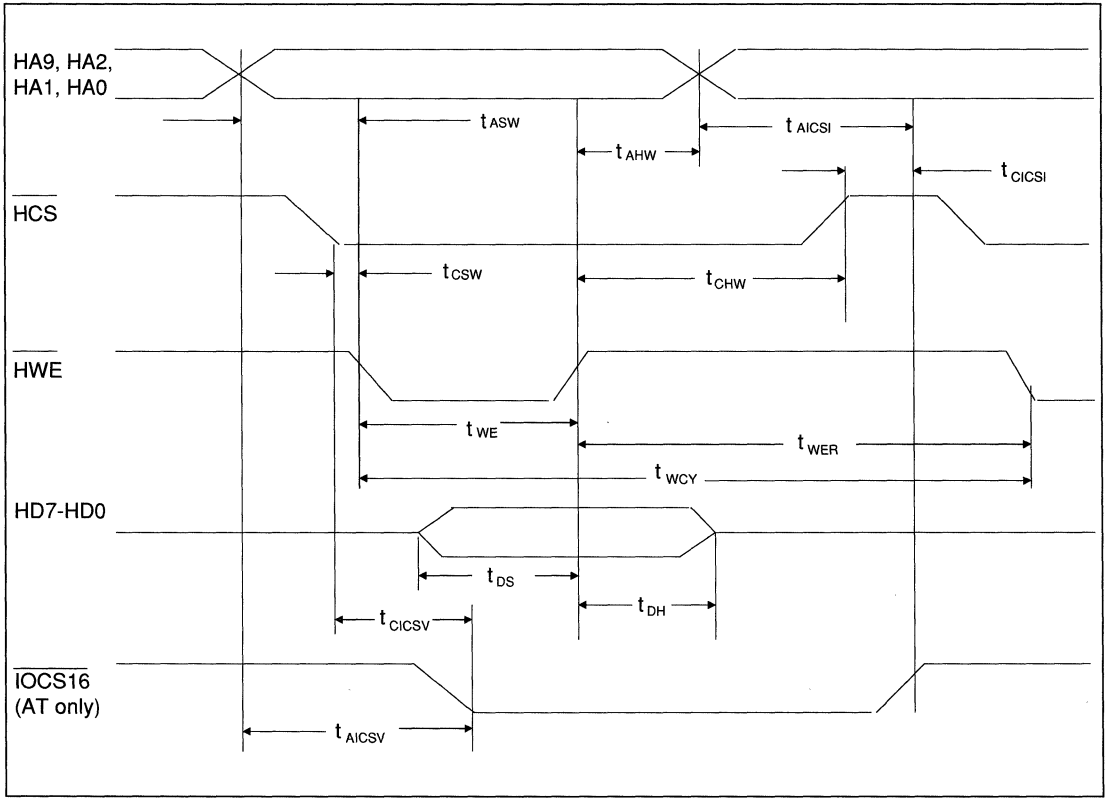

FIGURE 7. AT/XT HOST PROGRAMMED I/O WRITE TIMING

NOTE

A write occurs during the overlap of $\overline{HCS}$ and $\overline{HWE}$.

5.3.1 AT/XT HOST PROGRAMMED I/O WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASW}	Address Setup to $\overline{HWE}$ Low	30		ns	
t_{CSW}	$\overline{HCS}$ Setup to $\overline{HWE}$ Low	10		ns	
t_{DS}	Data Setup to $\overline{HWE}$ High	30		ns	Port 0 only.
t_{WE}	$\overline{HWE}$ Pulse Width	75		ns	Port 0 only.
t_{DS}	Data Setup to $\overline{HWE}$ High	50		ns	All other ports.
t_{WE}	$\overline{HWE}$ Pulse Width	100		ns	All other ports
t_{DH}	Data Hold from $\overline{HWE}$ High	15		ns	
t_{AHW}	ADDR Hold from $\overline{HWE}$ High	20		ns	
t_{CHW}	$\overline{HCS}$ Hold from $\overline{HWE}$ High	10		ns	
t_{WER}	$\overline{HCS}$ and $\overline{HWE}$ Inactive	20		ns	
t_{WCY}	Write Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16MHz (X=t_{XTAL})
t_{WCY}	Write Cycle Time	150		ns	All other ports
t_{CICSV}	$\overline{IOCS16}$ valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ valid from address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ inactive from $\overline{HCS}$		35	ns	Test circuit 1.
t_{AICSI}	$\overline{IOCS16}$ inactive from address		45	ns	Test circuit 1.

TABLE 15. AT/XT HOST PROGRAMMED I/O WRITE TIMING

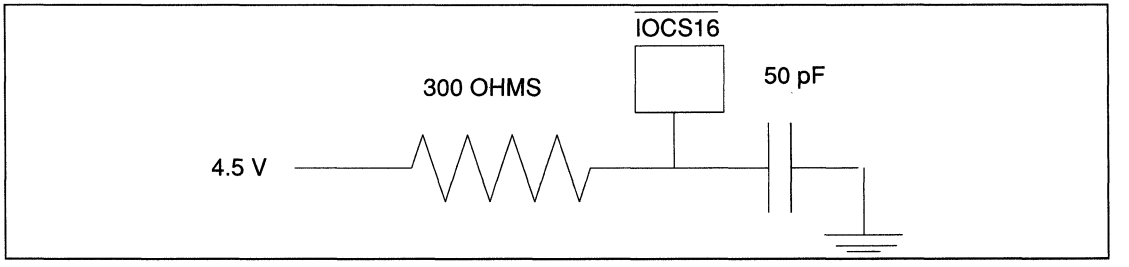

FIGURE 8. TEST CIRCUIT 1

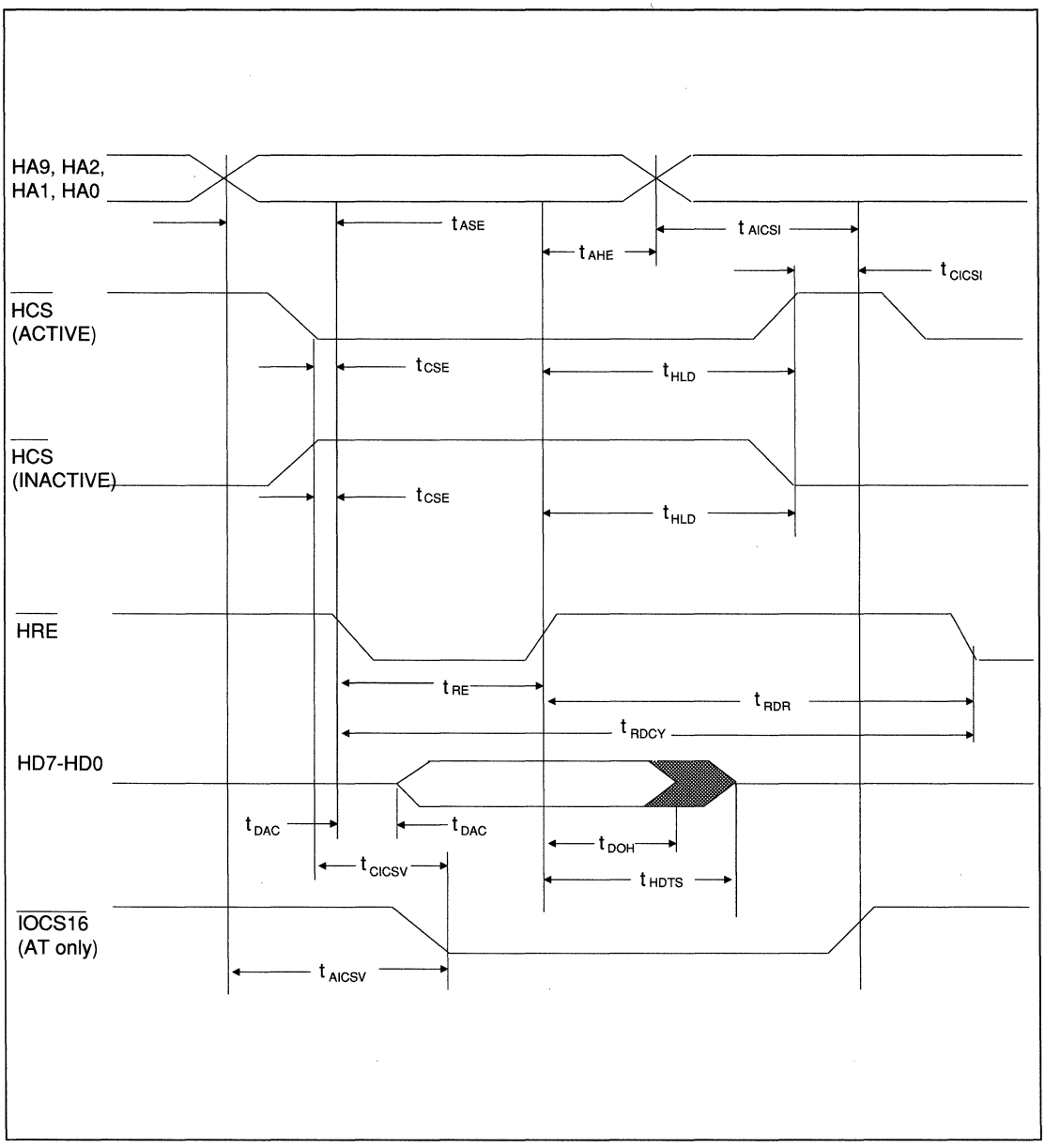

FIGURE 9. AT/XT HOST PROGRAMMED I/O READ TIMING

5.3.2 AT/XT HOST PROGRAMMED I/O READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{ASE}	Address Setup to $\overline{HRE}$ Low	30		ns	
t_{CSE}	$\overline{HCS}$ Setup to $\overline{HRE}$ Low	10		ns	
t_{DAC}	Data Valid from $\overline{HRE}$ Low		60 70 100	ns	Port 0, 8-bit. Port 0, 16-bit. All other ports.
t_{RE}	$\overline{HRE}$ Pulse Width	75 100		ns	Port 0 All other ports
t_{DOH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{HDTS}	Data Tri-state from $\overline{HRE}$		50	ns	
t_{HLD}	Address, $\overline{HCS}$ Hold from $\overline{HRE}$ High	10		ns	
t_{RDR}	$\overline{HCS}$ and $\overline{HRE}$ Inactive	20		ns	
t_{RDCY}	Read Cycle Time	125 2*X		ns	Port 0, XTAL>16 MHz Port 0, XTAL<16 MHz (X=t_{XTAL})
t_{RDCY}	Read Cycle Time	150		ns	All other ports.
t_{CICSV}	$\overline{IOCS16}$ Valid from $\overline{HCS}$		30	ns	
t_{AICSV}	$\overline{IOCS16}$ Valid from Address		40	ns	
t_{CICSI}	$\overline{IOCS16}$ Inactive from $\overline{HCS}$		35	ns	Test circuit 1
t_{AICSI}	$\overline{IOCS16}$ Inactive from Address		45	ns	Test circuit 1

TABLE 16. AT/XT HOST PROGRAMMED I/O READ TIMING

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5.3.3 AT/XT HOST DMA WRITE TIMING

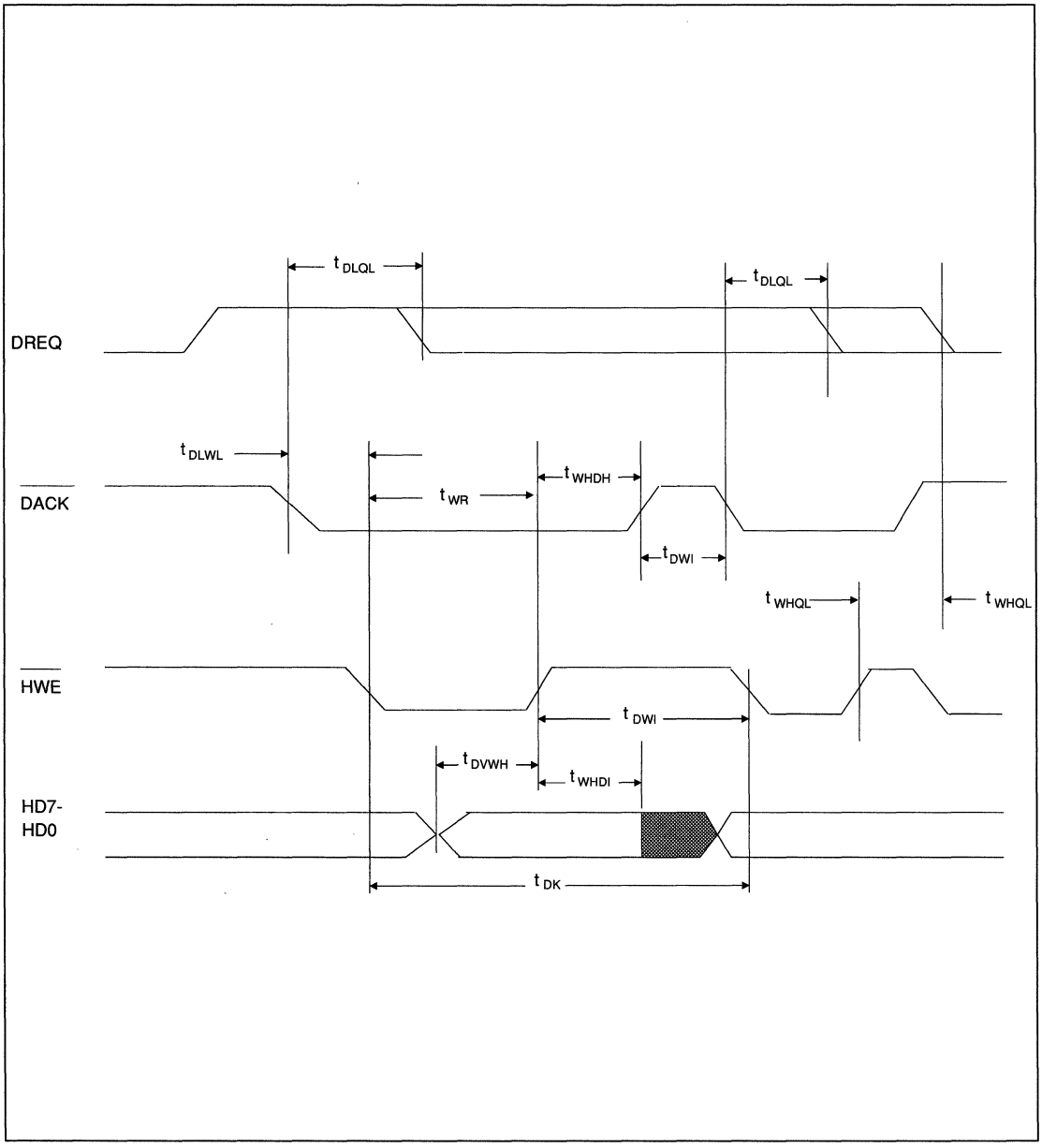

FIGURE 10. AT/XT HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{WHQL}	$\overline{HWE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First transfer count throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLWL}	$\overline{DACK}$ Low to $\overline{HWE}$ Low	0		ns	
t_{WR}	$\overline{HWE}$ Pulse Width	80		ns	
t_{DVWH}	Data Valid to $\overline{HWE}$ High	30		ns	
t_{WHDH}	$\overline{HWE}$ High to $\overline{DACK}$ High	0		ns	
t_{WHDI}	$\overline{HWE}$ High to Data Invalid	15		ns	
t_{DWI}	$\overline{DACK}$ and $\overline{HWE}$ Inactive	20		ns	

TABLE 17. AT/XT DMA WRITE TIMING

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5.3.4 AT/XT HOST DMA READ TIMING

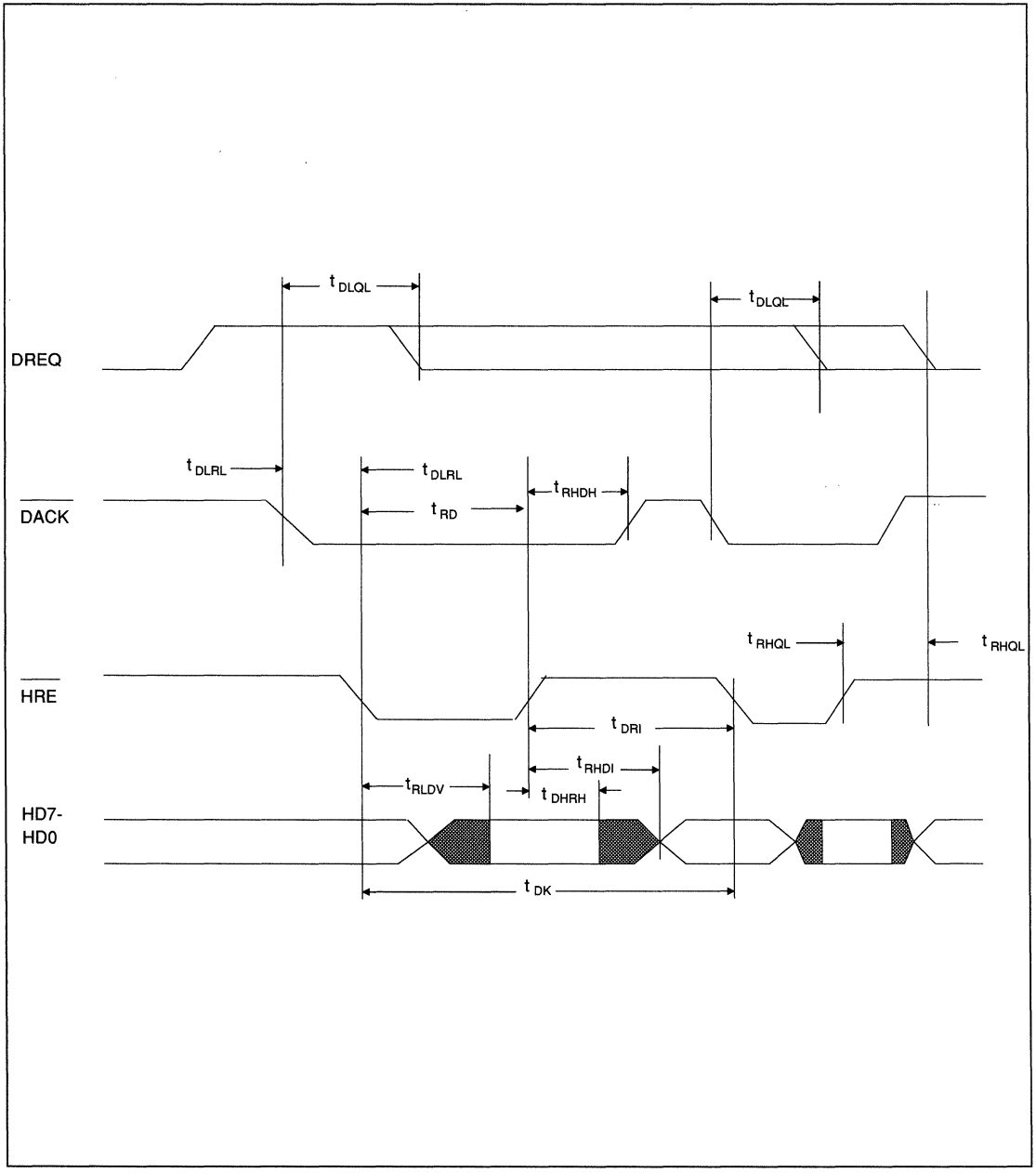

FIGURE 11. AT/XT HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{DLQL}	$\overline{DACK}$ Low to DRQ Low		100	ns	BDEN=0
t_{RHQL}	$\overline{HRE}$ High to DRQ Low		4*X +100	ns	BDEN=1. First TC throttle. (X=t_{XTAL})
t_{DK}	DMA Cycle	100 2*X		ns	XTAL=20MHz Any XTAL (X=t_{XTAL})
t_{DLRL}	$\overline{DACK}$ Low to $\overline{HRE}$ Low	0		ns	
t_{RD}	$\overline{HRE}$ Pulse Width	80		ns	
t_{RLDV}	$\overline{HRE}$ Low to Data Valid		60 70	ns	8-bit mode 16-bit mode
t_{RHDH}	$\overline{HRE}$ High to $\overline{DACK}$ High	0		ns	
t_{DHRH}	Data Hold from $\overline{HRE}$ High	5		ns	
t_{RHDI}	$\overline{HRE}$ High to Data tri-state		50	ns	
t_{DRI}	$\overline{DACK}$ and $\overline{HRE}$ Inactive.	20		ns	

TABLE 18. AT/XT DMA READ TIMING

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5.3.5 SLAVE HOST WRITE TIMINGS

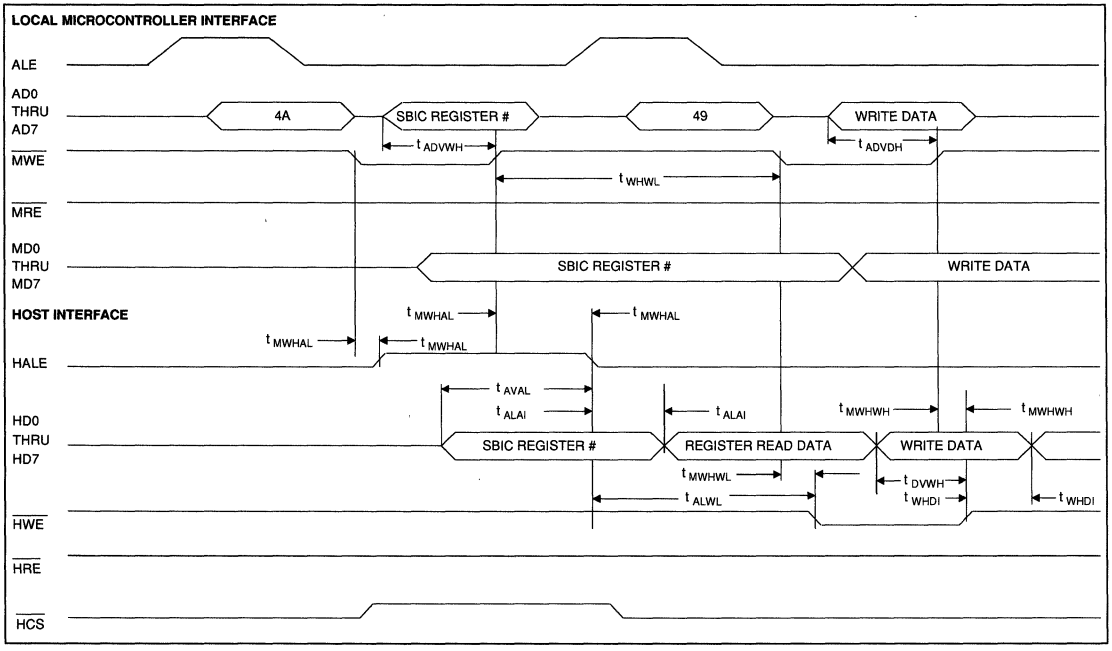

FIGURE 12. SLAVE HOST WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHWL}	Address Port Write to Data Write Recovery Time	120	10000	ns	
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{ALAI}	HD Address Hold From HALE low	0		ns	
t_{ALWL}	HALE Low To $\overline{HWE}$ Low	90		ns	
t_{DVWH}	HD Valid to $\overline{HWE}$ High	70		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns
t_{WHDI}	HD Inactive from $\overline{HWE}$	0		ns	
t_{MWHWL}	$\overline{MWE}$ Low to HWE Low		150	ns	
t_{MHWH}	MWE High to HWE High		150	ns	

TABLE 19. SLAVE HOST WRITE TIMING

5.3.6 SLAVE HOST READ TIMINGS

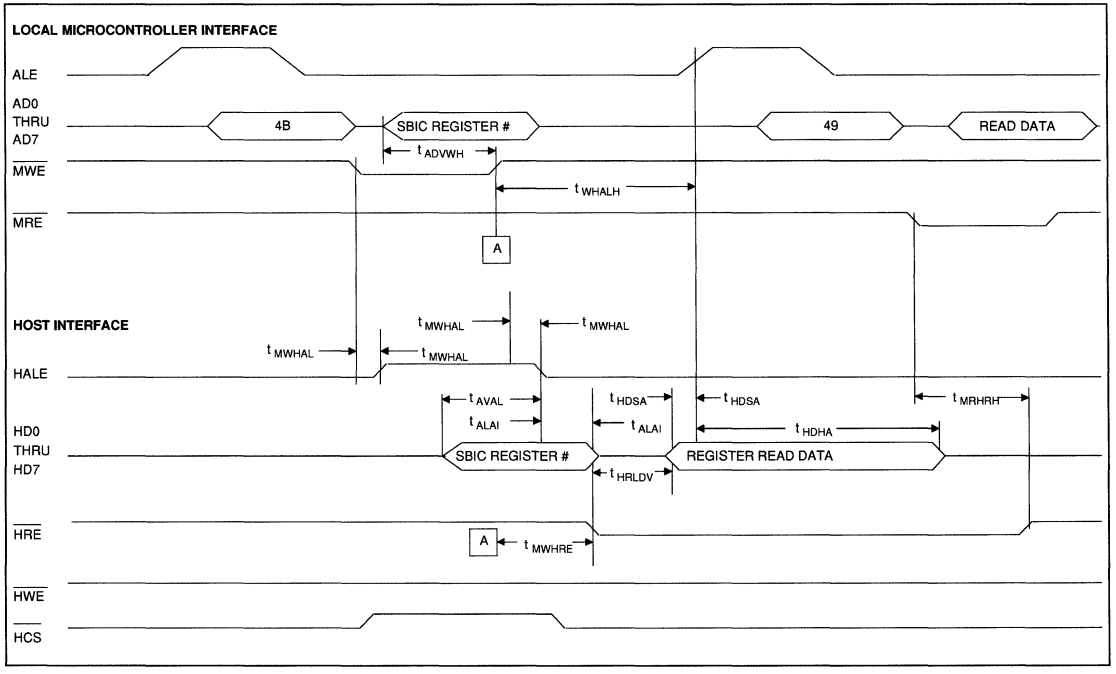

FIGURE 13. SLAVE HOST READ TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{WHALH}	Address Port Write to ALE High Read Recovery Time	400	10000	ns	t_{HRLDV}=210 ns
t_{MWHAL}	$\overline{MWE}$ to HALE Delay		150	ns	
t_{MWHRE}	$\overline{MWE}$ to $\overline{HRE}$ Delay		150	ns	
t_{AVAL}	HD Address Setup to HALE Low	40		ns	AD setup to $\overline{MWE}$ (t_{ADVWH})=130 ns.
t_{ALAI}	HD Address Hold from HALE Low	0		ns	
t_{HDSA}	HD Data **Setup to** ALE High	40		ns	
t_{HDHA}	HD Data **Hold from** ALE High	40		ns	
t_{MRHRH}	$\overline{MRE}$ Low to $\overline{HRE}$ High Delay	0		ns	
t_{HRLDV}	HRE Low to HD Data Valid Delay				t_{HRLDV} is a function of the slave peripheral device and only affects t_{WHALH}. t_{WALH} = t_{MWHRE} + t_{HRLDV} + t_{HDSA}

TABLE 20. SLAVE HOST READ TIMING

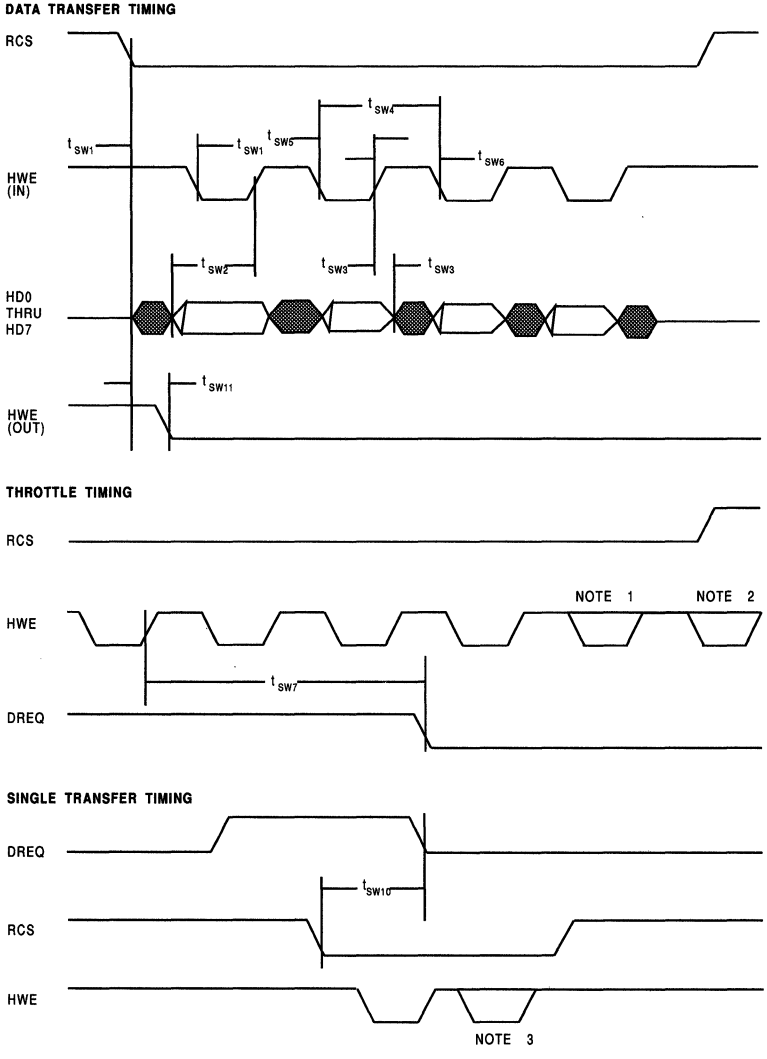

FIGURE 14. SLAVE HOST DMA WRITE TIMING

5.3.7 SLAVE HOST DMA WRITE TIMING

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to $\overline{HWE}$ First Transfer of Burst	0 0 0		ns	
t_{SW2}	HD Valid to $\overline{HWE}$ Rising	30 30 30		ns	
t_{SW3}	$\overline{HWE}$ Rising to HD Invalid	15 15 15		ns	
t_{SW4}	$\overline{HWE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HWE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HWE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HWE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HWE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 21. SLAVE HOST DMA WRITE TIMING

The following notes apply to Figure 15.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although 4 transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

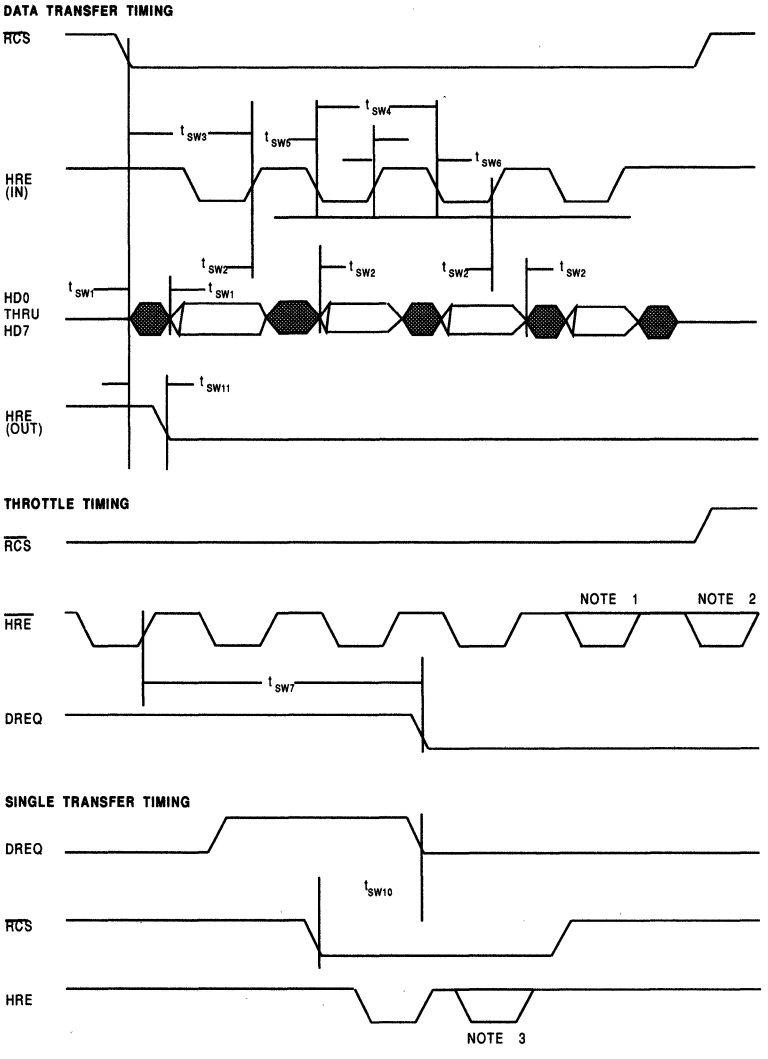

FIGURE 15. SLAVE HOST DMA READ TIMING

5.3.8 SLAVE HOST DMA READ TIMING

SYMBOL	CHARACTERISTIC	MIN BIN 02 BIN 03 BIN 05	MAX BIN 02 BIN 03 BIN 05	UNITS	CONDITIONS
t_{SW1}	$\overline{RCS}$ Low to HD Valid First Transfer of Burst	0 0 0		ns	
t_{SW2}	$\overline{HRE}$ Rising to HD Valid	5 5 5	180 180 180	ns	
t_{SW3}	$\overline{RCS}$ Low to First $\overline{HRE}$ Rising Edge	140 140 100		ns	
t_{SW4}	$\overline{HRE}$ Cycle Time	200 200 100		ns	$t_{XTAL} < t_{SW4} / 2$
t_{SW5}	$\overline{HRE}$ Low Pulse Width	80 80 30		ns	
t_{SW6}	$\overline{HRE}$ High Pulse	30 30 30		ns	
t_{SW7}	$\overline{HRE}$ Rising to DRQ Low		4*X + 100 4*X + 100 4*X + 50	ns	Intermediate throttle. X = t_{XTAL}
t_{SW10}	$\overline{RCS}$ Low to DREQ Low		100 100 50		Throttle when transfer count < 16 or single transfer mode
t_{SW11}	$\overline{DACK}$ Low to $\overline{HRE}$ Out Tri-state		60 60 60	ns	HSMB = 1

TABLE 22. SLAVE HOST DMA READ TIMING

The following notes apply to Figure 16.

NOTE 1

SBIC guarantees no transfer here at 5 MB/s transfer rate.

NOTE 2

SBIC guarantees no transfer here at 10 MB/s transfer rate.

NOTE 3

SBIC guarantees no transfer here.

Although 4 transfers may occur after the FIFO goes almost full at 10 MB/s and only 3 bytes remain at that time, the buffer manage guarantees that at least 1 additional transfer occurs out of the FIFO prior to the fourth host transfer after the almost full condition. This guarantees that no overrun condition occurs.

5.3.9 BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR; XTAL = 8 - 25 MHZ)

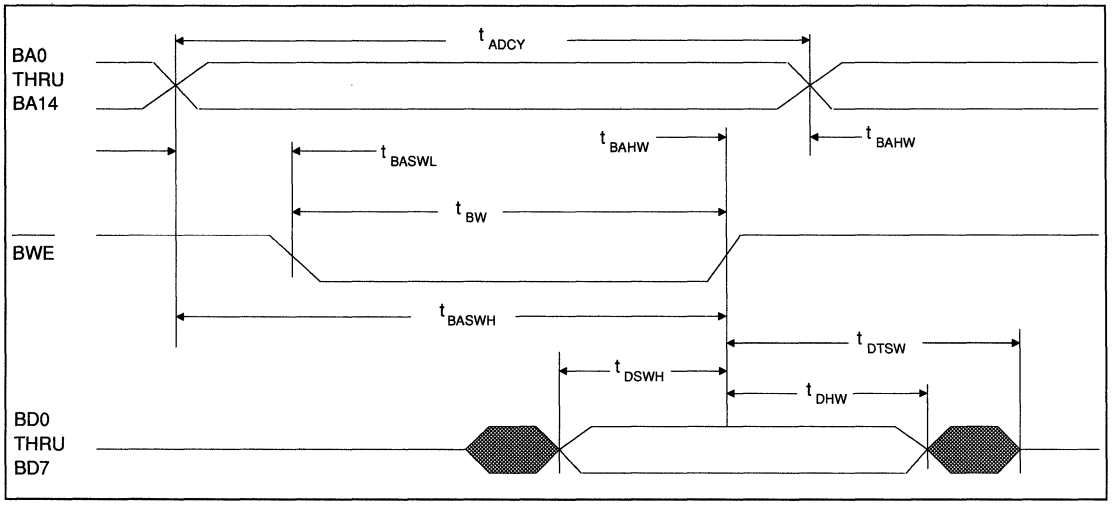

FIGURE 16. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN Bin 02 Bin 03 Bin 05	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}-28$ $2*t_{XTAL}-35$ $2*t_{XTAL}-25$		ns	Any XTAL
t_{BASWH}	Addres Setup to $\overline{BWE}$ High	$2*t_{XTAL}-40$ $2*t_{XTAL}-55$ $2*t_{XTAL}-35$		ns	Any XTAL
t_{BASWL}	Addres Setup to $\overline{BWE}$ Low	$0.5*t_{XTAL}-20$ $0.5*t_{XTAL}-35$ $0.5*t_{XTAL}-20$		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$1.5*t_{XTAL}-30$ $1.5*t_{XTAL}-35$ $1.5*t_{XTAL}-25$		ns	Any XTAL
t_{BAHW}	Address Hold From $\overline{BWE}$ High	5 5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$1.5*t_{XTAL}-40$ $1.5*t_{XTAL}-60$ $1.5*t_{XTAL}-35$		ns	Any XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10 10		ns	Any XTAL
t_{DTSW}	Data Tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

TABLE 23. BUFFER RAM WRITE TIMING (INTERNAL OSCILLATOR)

5.3.10 BUFFER RAM READ TIMING (INTERNAL OSCILLATOR; XTAL = 8 - 20 MHZ)

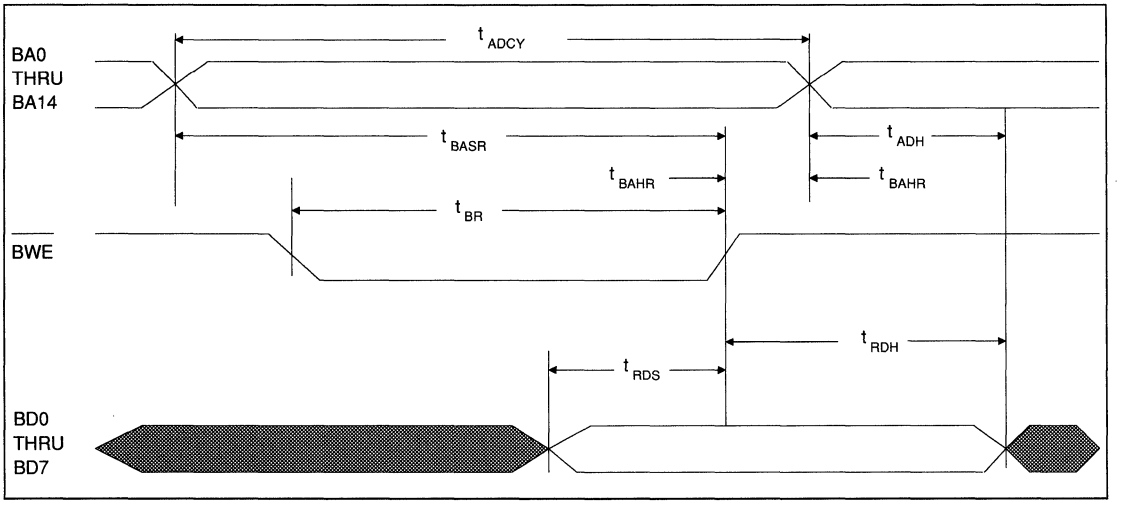

FIGURE 17. BUFFER READ TIMING (INTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$1.5*t_{XTAL}$-30 $1.5*t_{XTAL}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

• All timings in this table **only** are referenced to 1.5V levels.

TABLE 24. BUFFER READ TIMING (INTERNAL OSCILLATOR)

33

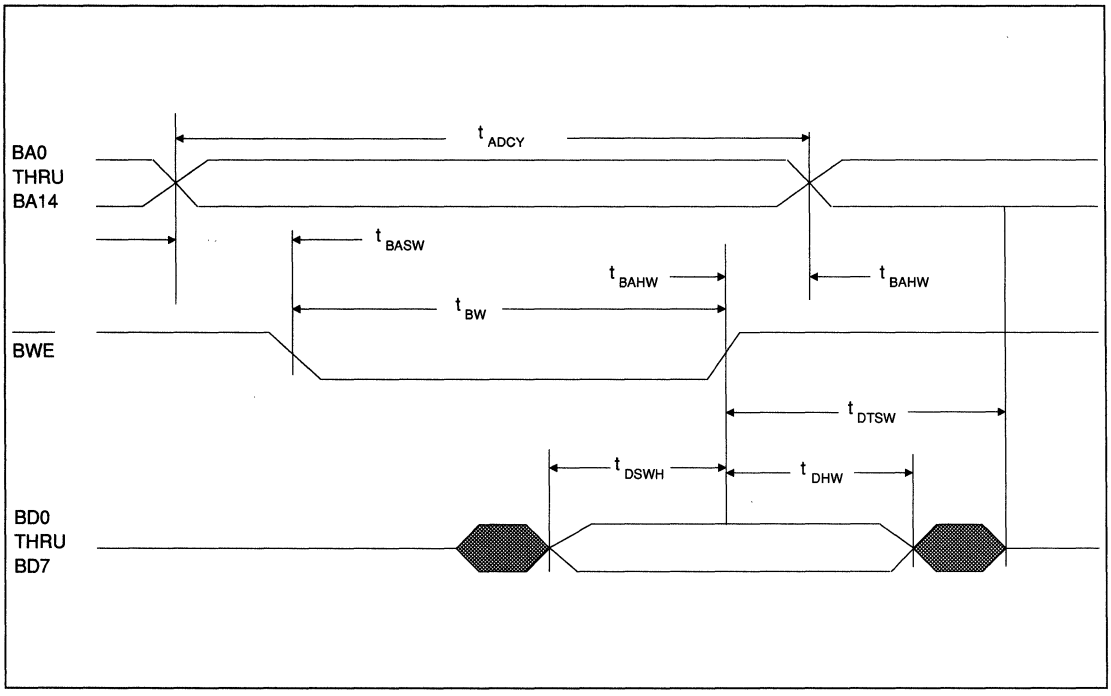

FIGURE 18. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

5.3.11 BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR; XTAL = 8 to 20 MHz)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125		ns	Max XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35		ns	Any XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	5 5		ns	Max XTAL/ 50% XTAL
t_{BASWL}	Address Setup to $\overline{BWE}$ Low	t_{XCH}-20 t_{XCH}-35		ns	Any XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	60 105		ns	Max XTAL
t_{BASWH}	Address Setup to $\overline{BWE}$ High	$2*t_{XTAL}$-40 $2*t_{XTAL}$-55		ns	Any XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	55 85		ns	Max XTAL/ 50% XTAL
t_{BW}	$\overline{BWE}$ Pulse Width	$t_{XTAL}+t_{XCL}$-30 $t_{XTAL}+t_{XCL}$-35		ns	Any XTAL
t_{BAHW}	Address Hold from $\overline{BWE}$ High	5 5		ns	Any XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	35 60		ns	Max XTAL
t_{DSWH}	Data Valid to $\overline{BWE}$ High	$t_{XTAL}+t_{XCH}$-40 $t_{XTAL}+t_{XCH}$-60		ns	Any XTAL/ %50 XTAL
t_{DHW}	Data Hold from $\overline{BWE}$ High	10 10		ns	Any XTAL
t_{DTSW}	Data tri-state from $\overline{BWE}$ High		50	ns	Any XTAL

• All timings in this table only are referenced to 1.5 V levels except t_{DHW}.

TABLE 25. BUFFER RAM WRITE TIMING (EXTERNAL OSCILLATOR)

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5.3.12 BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR; XTAL=8 to 20 MHz)

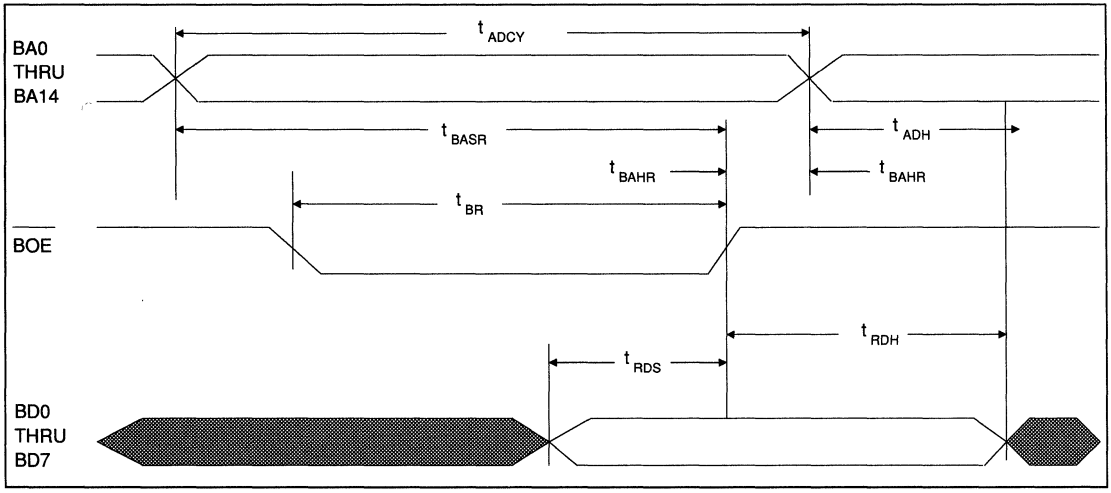

FIGURE 19. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	UNITS	CONDITIONS
t_{ADCY}	Address Cycle Time	72 125	ns	Max XTAL/50% XTAL
t_{ADCY}	Address Cycle Time	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	Any XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	72 125	ns	Max XTAL/50% XTAL
t_{BASR}	Address Setup to $\overline{BOE}$ High	$2*t_{XTAL}$-28 $2*t_{XTAL}$-35	ns	
t_{BR}	$\overline{BOE}$ Pulse Width	45 75	ns	Max XTAL/50% XTAL
t_{BR}	$\overline{BOE}$ Pulse Width	$t_{XTAL}+t_{XCH}$-30 $t_{XTAL}+t_{XCH}$-45	ns	Any XTAL
t_{BAHR}	Address Hold from $\overline{BOE}$ High	0 0	ns	Any XTAL
t_{RDS}	Data Setup to $\overline{BOE}$ High	5 5	ns	Any XTAL
t_{RDH}	Data Hold from $\overline{BOE}$ High	10 10	ns	Any XTAL
t_{DHW}	Data Hold from Address	10 10	ns	

• All timings in this table referenced to 1.5 V levels.

TABLE 26. BUFFER RAM READ TIMING (EXTERNAL OSCILLATOR)

5.3.13 MICROPROCESSOR WRITE TIMING (INTEL BUS)

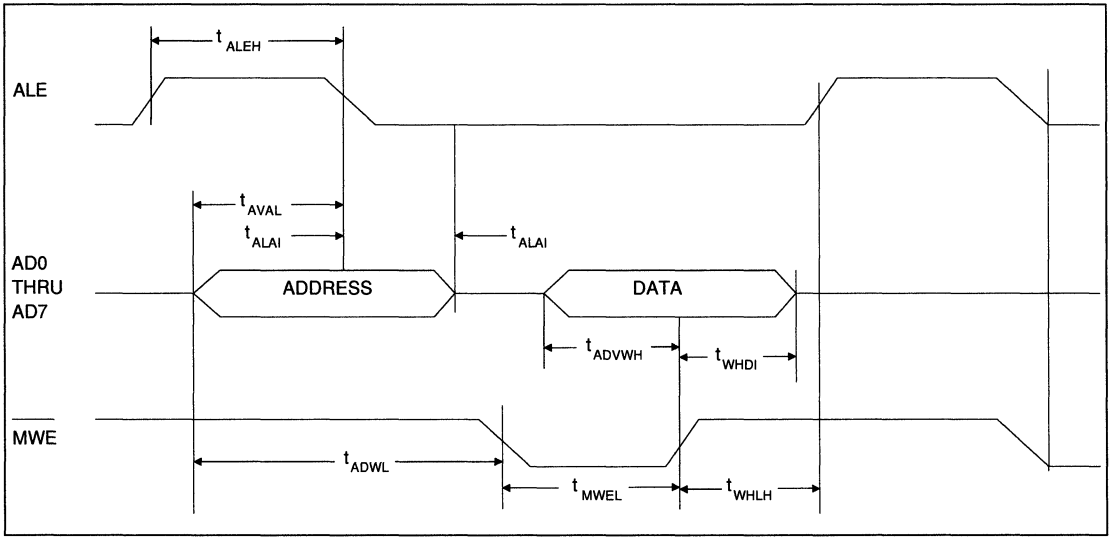

FIGURE 20. MICROPROCESSOR WRITE TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to ALE Low	15	ns	
t_{ALAI}	Address Hold from ALE Low	5	ns	
t_{ALEH}	ALE High Pulse Width	30	ns	
t_{ADVWH}	Data Setup to $\overline{MWE}$ High	50 130	ns	HSMB=0 HSMB=1
t_{WHDI}	Data Hold from $\overline{MWE}$ High	5	ns	
t_{MWEL}	$\overline{MWE}$ Low Pulse Width	75	ns	
t_{ADWL}	Address Valid to $\overline{MWE}$ Low	55	ns	
t_{WHLH}	$\overline{MWE}$ High to ALE High	10	ns	

TABLE 27. MICROPROCESSOR WRITE TIMING (INTEL BUS)

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5.3.14 MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

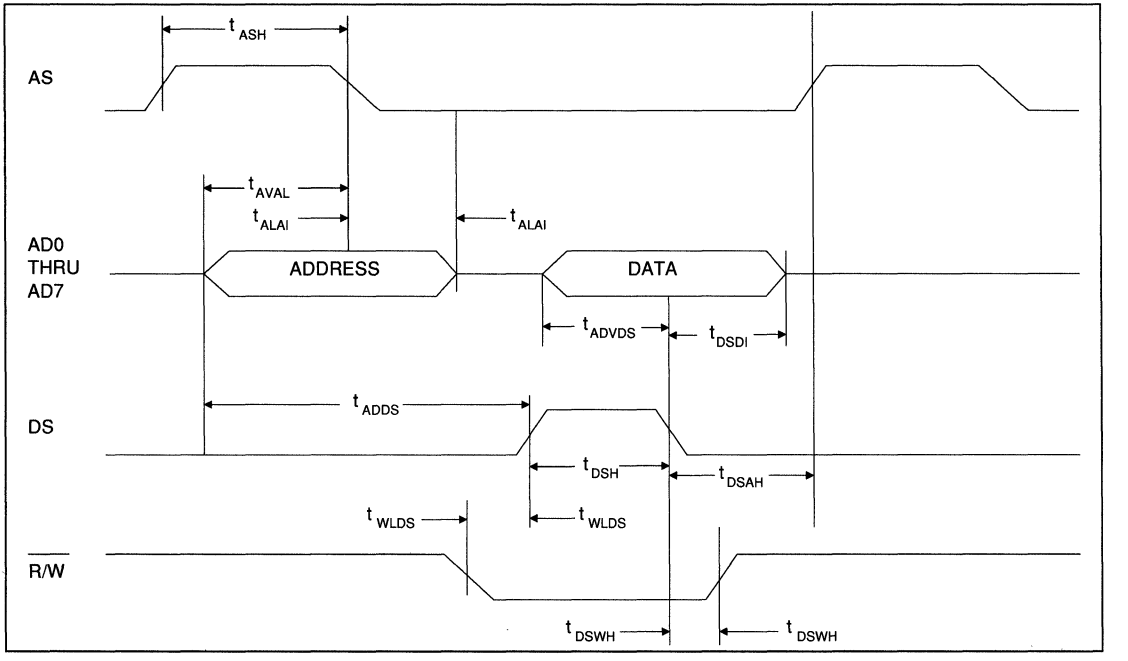

FIGURE 21. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	UNITS	CONDITIONS
t_{AVAL}	Address Setup to AS Low	15	ns	
t_{ALAI}	Address Hold from AS	5	ns	
t_{ASH}	AS High Pulse Width	30	ns	
t_{ADVDS}	Data Setup to DS Low	50 130	ns	HSMB=0 HSMB=1
t_{DSDI}	Data Hold from DS Low	5	ns	
t_{DSH}	DS High Pulse Width during Write	75	ns	
t_{WLDS}	R/$\overline{W}$ Low to DS High	5	ns	
t_{DSWH}	DS Low to R/$\overline{W}$ High	20	ns	
t_{ADDS}	Address High to DS High	55	ns	
t_{DSAH}	DS Low to AS High	10	ns	

TABLE 28. MICROPROCESSOR WRITE TIMING (MOTOROLA BUS)

5.3.15 MICROPROCESSOR READ TIMING (INTEL BUS)

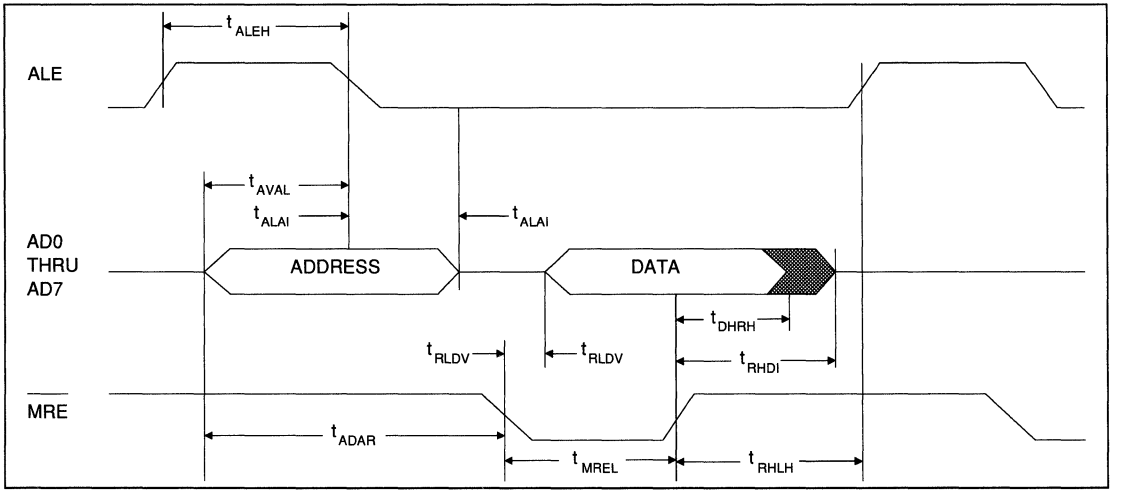

FIGURE 22. MICROPROCESSOR READ TIMING (INTEL BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to ALE Low	15		ns
t_{ALAI}	Address Hold from ALE Low	5		ns
t_{ALEH}	ALE High Pulse Width	30		ns
t_{RLDV}	Data Valid from $\overline{MRE}$ Low		100	ns
t_{DHRH}	Data Hold from $\overline{MRE}$ High	10		ns
t_{RHDI}	Data Tri-state from $\overline{MRE}$ High		50	ns
t_{MREL}	$\overline{MRE}$ Low Pulse Width	100		ns
t_{ADAR}	Address Valid to $\overline{MRE}$ Low	55		ns
t_{RHLH}	$\overline{MRE}$ High to ALE High	10		ns

TABLE 29. MICROPROCESSOR READ TIMING (INTEL BUS)

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5.3.16 MICROPROCESSOR READ TIMING (MOTOROLA BUS)

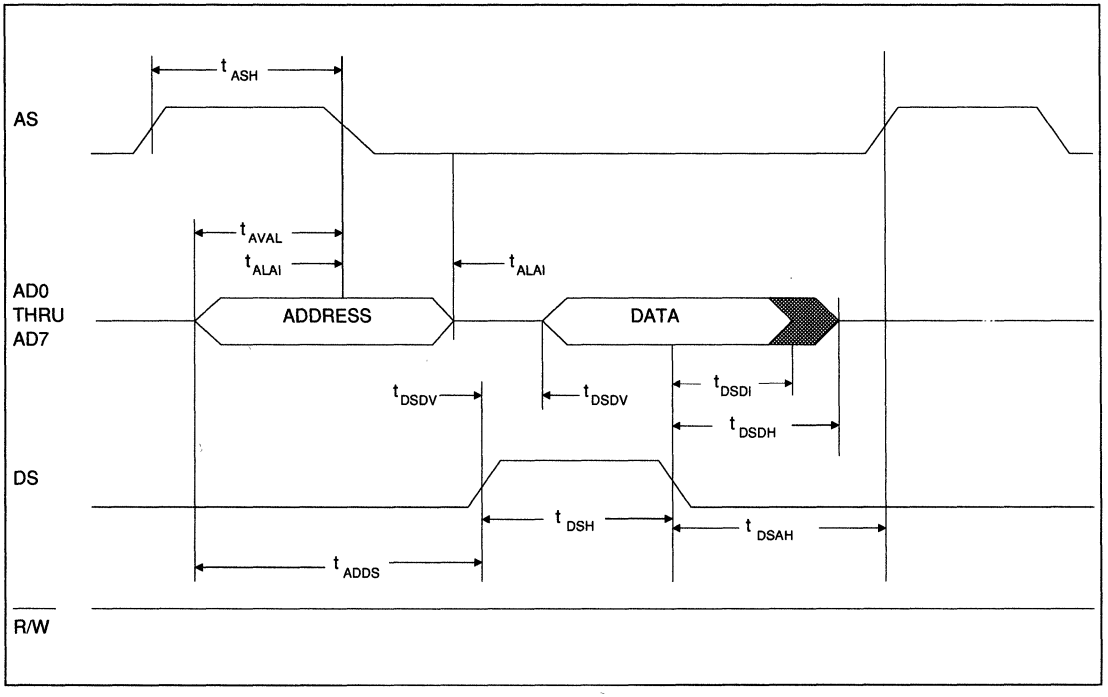

FIGURE 23. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
t_{AVAL}	Address Setup to AS Low	15		ns
t_{ALAI}	Address Hold from AS Low	5		ns
t_{ASH}	AS High Pulse Width	30		ns
t_{DSDV}	Data Valid from DS High		100	ns
t_{DSDI}	Data Tri-state from DS Low		50	ns
t_{DSH}	DS High pulse Width during Read	100		ns
t_{ADDS}	Address Valid to DS High	55		ns
t_{DSAH}	DS Low to AS High	10		ns

TABLE 30. MICROPROCESSOR READ TIMING (MOTOROLA BUS)

5.3.17 WRITE DATA TIMING (MFM/RLL MODE; WC 5 to 15 MHz)

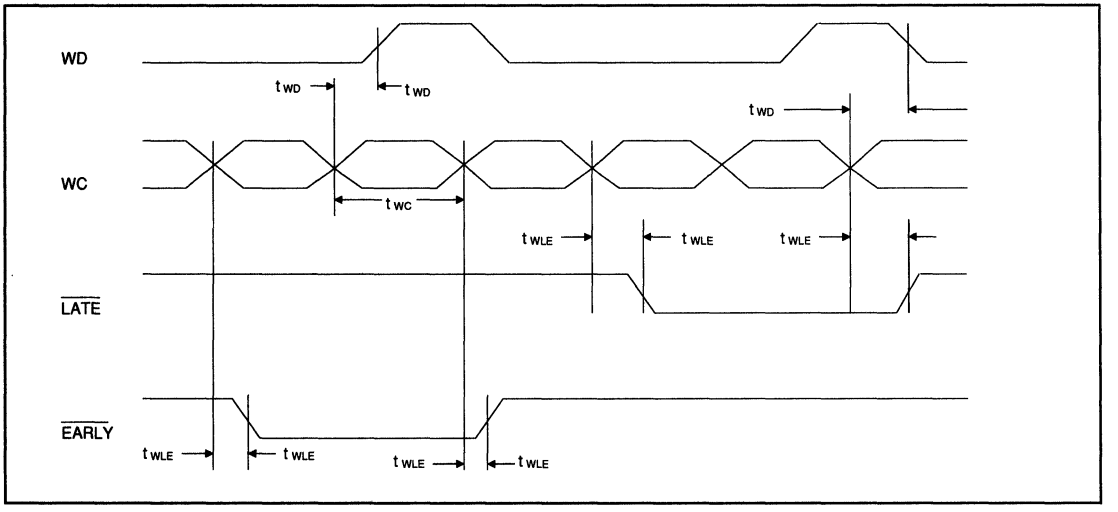

FIGURE 24. WRITE DATA TIMING (MFM/RLL MODE)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
		20 MHz		
		12 MHz		
t_{WC}	WC Pulse Width	28	500	ns
		45	500	
t_{WLE}	Early/Late Propagation	3	15	ns
		3	25	
t_{WD}	WD Propagation Delay	3	15	ns
		3	25	
t_{WCF}	WC Frequency	1	15	MHz
		1	10	

TABLE 31. WRITE DATA TIMING (MFM/RLL MODE)

33

5.3.18 WRITE DATA TIMING (NRZ MODE; WC 5 to 15 MHz)

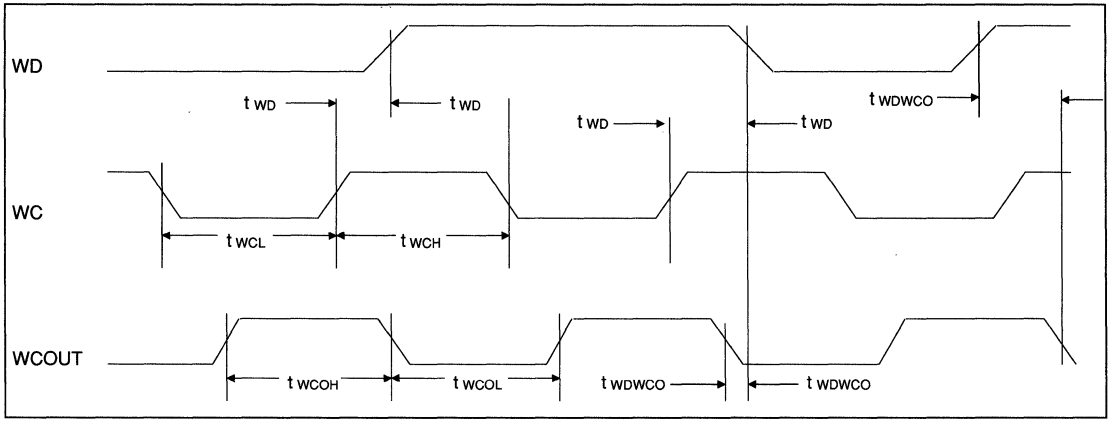

FIGURE 25. WRITE DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{WCL}	WC Pulse Width Low	20 27	500 500	ns
t_{WCH}	WC Pulse Width High	20 27	500 500	ns
t_{WLE}	Early/Late Propagation	3 3	15 25	ns
t_{WD}	WD Propagation Delay	3 3	15 25	ns
t_{WCF}	WC Frequency	1 1	22 16.5	MHz
t_{WCOL}	WCOUT Pulse Width Low	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOL}	WCOUT Pulse Width Low		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WCOH}	WCOUT Pulse Width High	t_{WCH} - 5 t_{WCH} - 9		ns
t_{WCOH}	WCOUT Pulse Width High		t_{WCH} + 5 t_{WCH} + 9	ns
t_{WDWCO}	WD Prop Delay from WCOUT	-5 -8	+5 +8	ns

TABLE 32. WRITE DATA TIMING (MFM/RLL MODE)

5.3.19 READ DATA TIMING (MFM/RLL MODE; RC/WC 5 to 15 MHz)

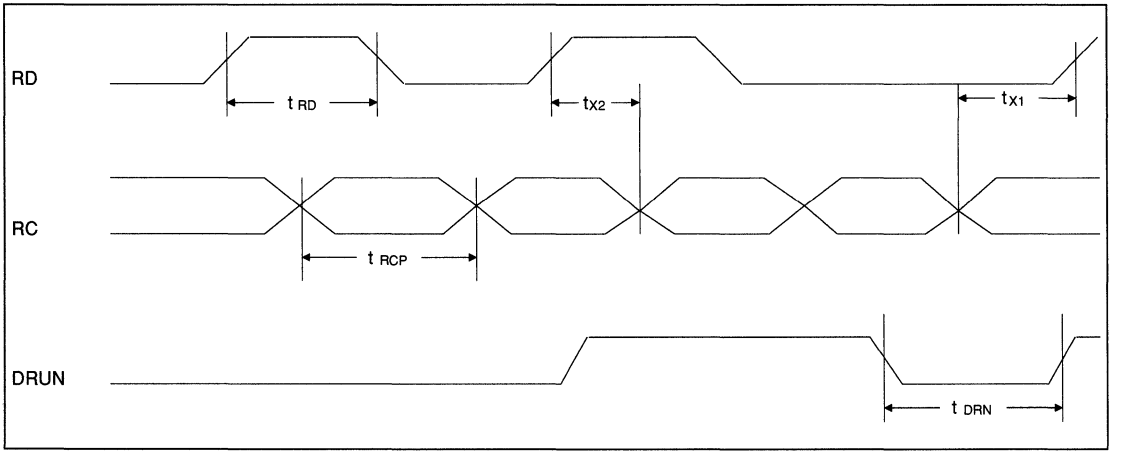

FIGURE 26. READ DATA TIMING (MFM/RLL)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	27 45	500 500	ns
t_{X1}	RC Transition to Next Leading RD	5 10		ns
t_{X2}	Leading RD to Next RC Transition	10 20		ns
t_{RD}	Read Data Pulse Width	20 30	t_{RCP} t_{RCP}	ns
t_{DRN}	DRUN Low Pulse Width	25 25		ns
t_{RCF}	RC Frequency	1 1	15 10	MHz

TABLE 33. READ DATA TIMING (MFM/RLL)

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5.3.20 READ DATA TIMING (NRZ MODE; WC 5 to 20 MHz)

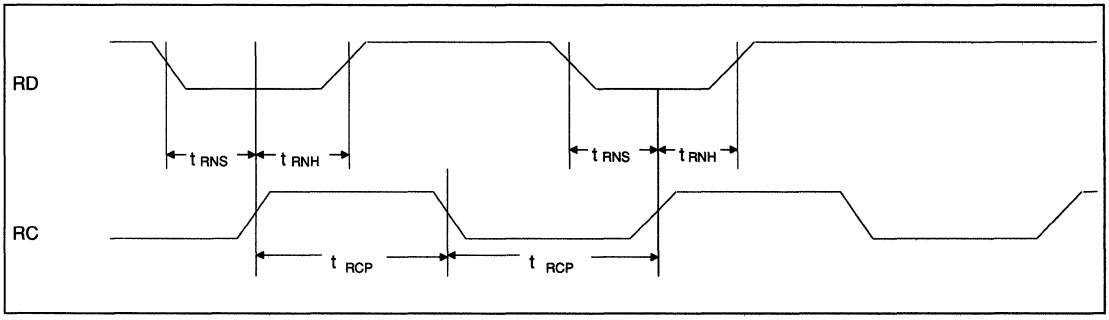


FIGURE 27. READ DATA TIMING (NRZ MODE)

SYMBOL	CHARACTERISTIC	MIN 20 MHz 12 MHz	MAX	UNITS
t_{RCP}	RC Pulse Width	20 27	500 500	ns
t_{RNS}	RD Setup to RC High	7 10		ns
t_{RNH}	RD Hold from RC High	7 10		ns
t_{RCF}	RC Frequency	1 1	22 16.5	MHz

TABLE 34. READ DATA TIMING (NRZ MODE)

5.3.21 MISCELLANEOUS TIMING

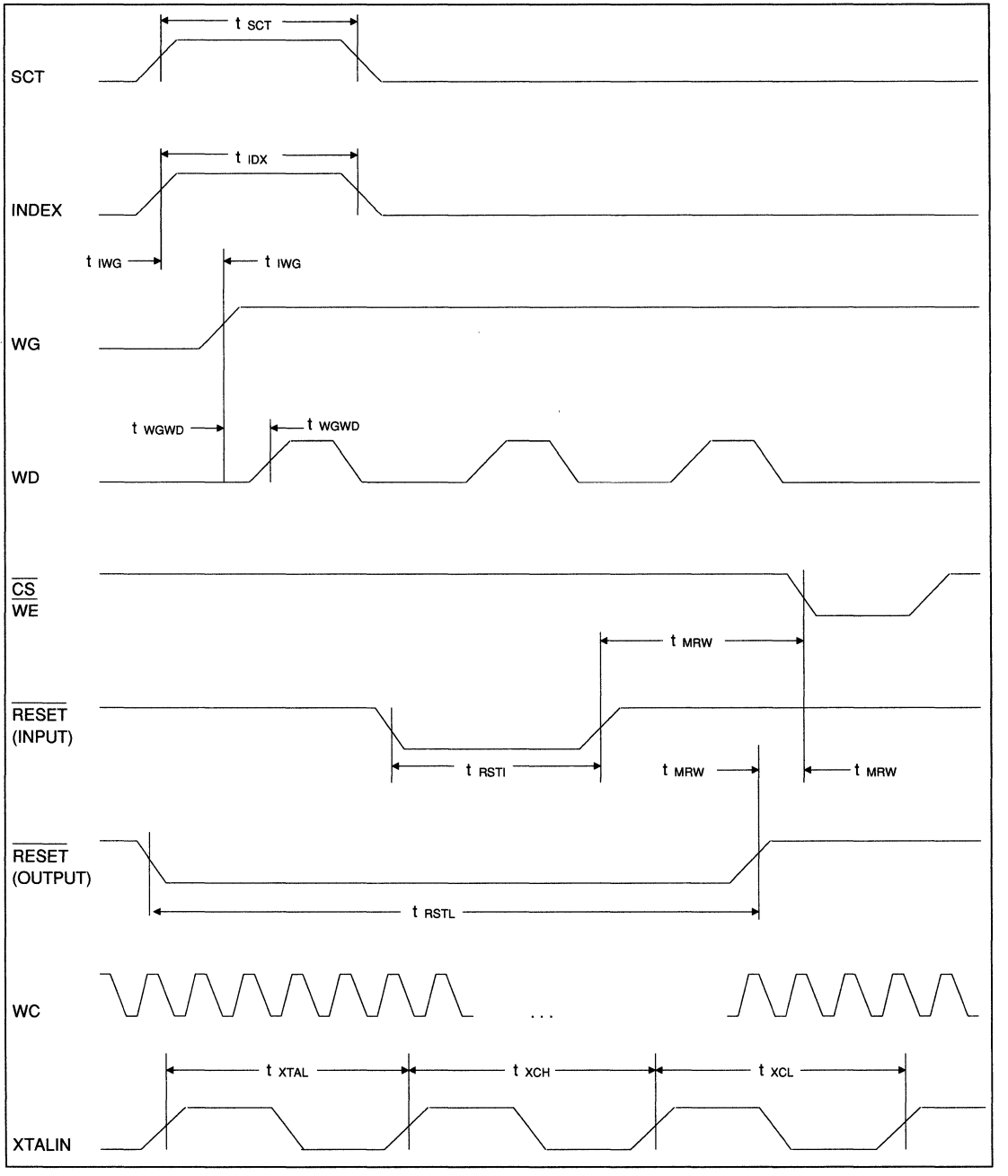


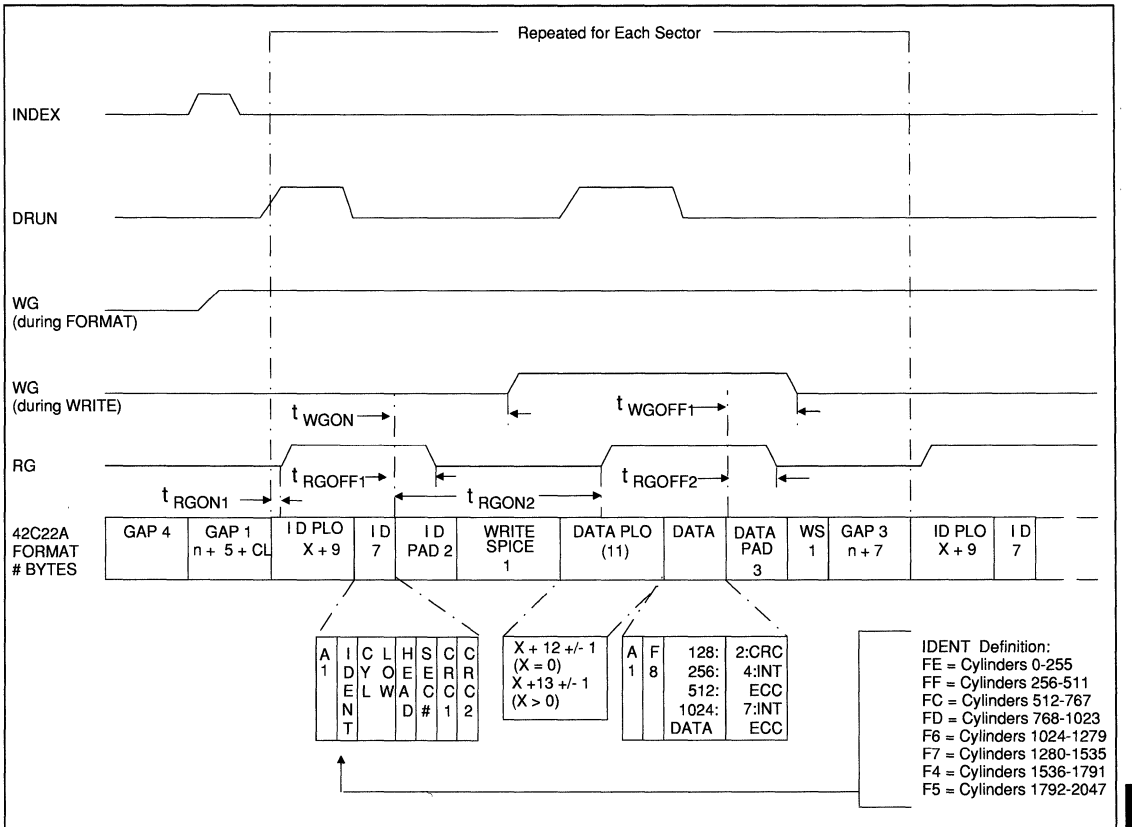
FIGURE 28. MISCELLANEOUS TIMING

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
t_{IDX}	Index Pulse Width	100		ns	
t_{SCT}	SCT Pulse Width	100		ns	
t_{IWG}	Index to write gate	0	4	WC periods	Gap data=33 in RLL mode. Any gap data in MFM and NRZ.
t_{WGWD}	Write gate to write data	0	4	WC periods	
t_{RSTI}	$\overline{\text{RESET}}$ in pulse width low	24		WC periods	
t_{MRW}	$\overline{\text{MR}}$ Trailing to Host Register Write	2.4		µs	
F_{RCWC}	Difference of RC Frequency from WC Frequency	-15%	+15%		
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	51.2		ms	XTAL=10 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	41.3		ms	XTAL=12.5 MHz
t_{RSTL}	$\overline{\text{RESET}}$ Out Low Pulse Width during Power-up	25.6		ms	XTAL=20 MHz
t_{XTAL}	Clock Period	50 70	125	ns	
t_{XCH}	Clock High Time	25 30		ns	
t_{XCL}	Clock Low Time	25 30		ns	

NOTE

t_{XTAL}, t_{XCH}, and t_{XCL} timings at 2.5 V levels.

TABLE 35. MISCELLANEOUS TIMING

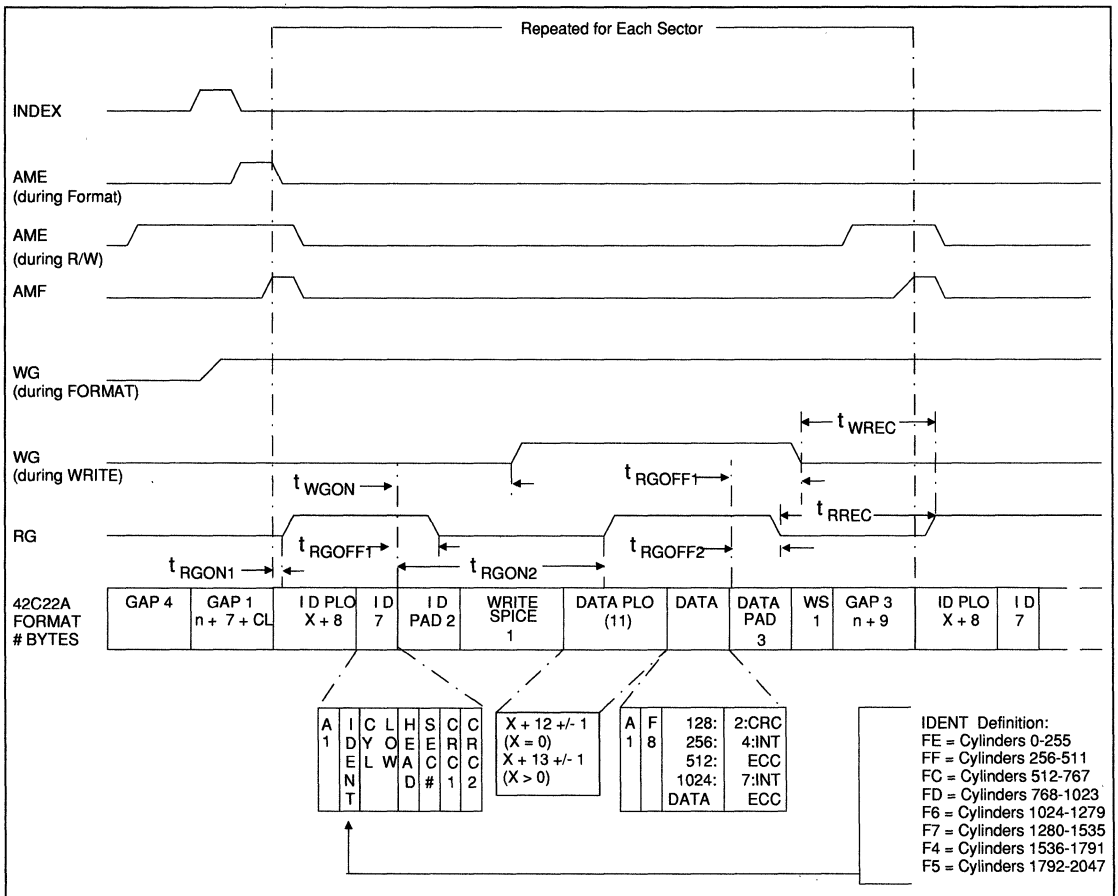


33

NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.

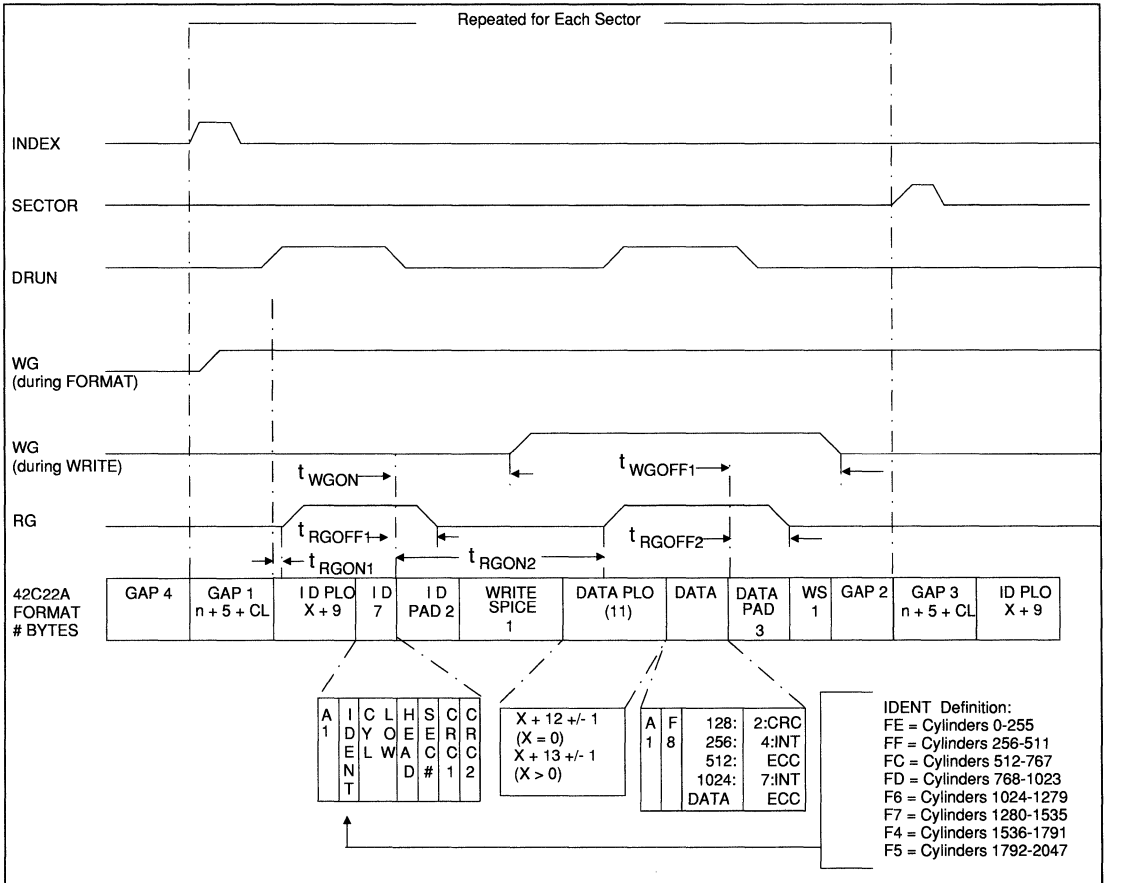
FIGURE 29. SOFT SECTOR MFM/RLL TRACK FORMAT



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = 3 ± 1 bit times with respect to AMF.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WREC} = 21 to 35 bytes minimum. t_{RREC} = 23 bytes minimum.

FIGURE 30. SOFT SECTOR NRZ TRACK FORMAT

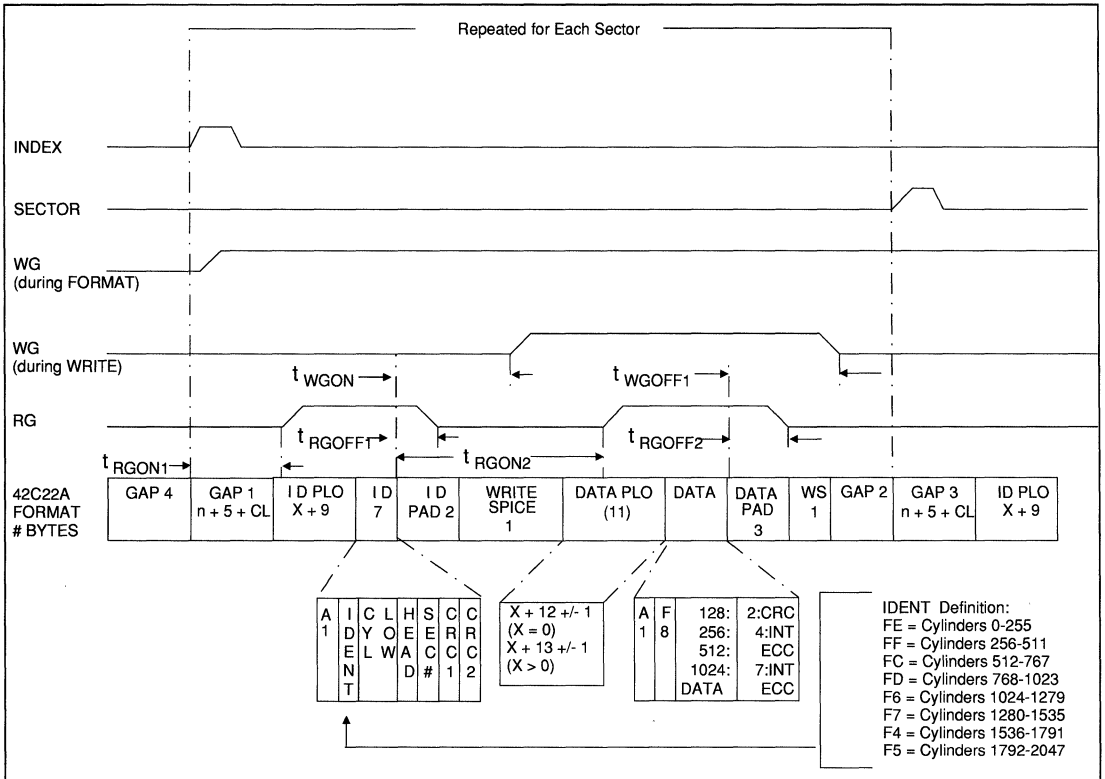


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = 19 ± 1 bit times with respect to DRUN. SECTOR is tied to DRUNSCT during format. DRUN is tied to DRUNSCT during read and write.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 31. HARD SECTOR RLL/MFM TRACK FORMAT (WITH SOFT SECTOR READ/WRITE)

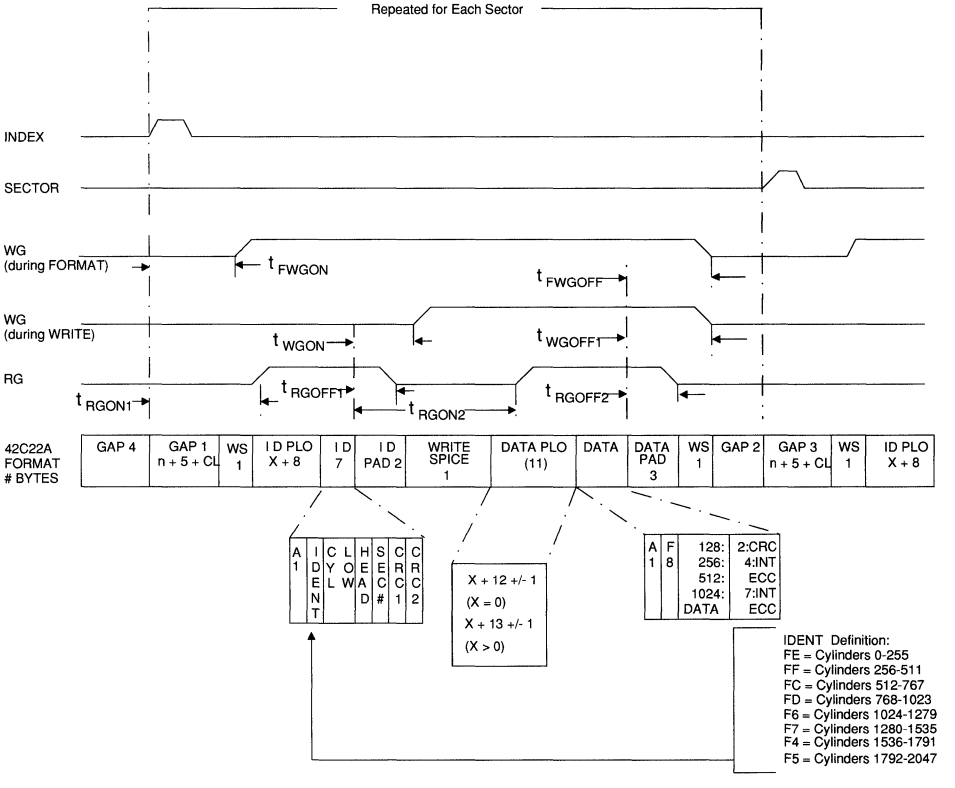


NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.

GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 32. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND CONTINUOUS WG OPTION)

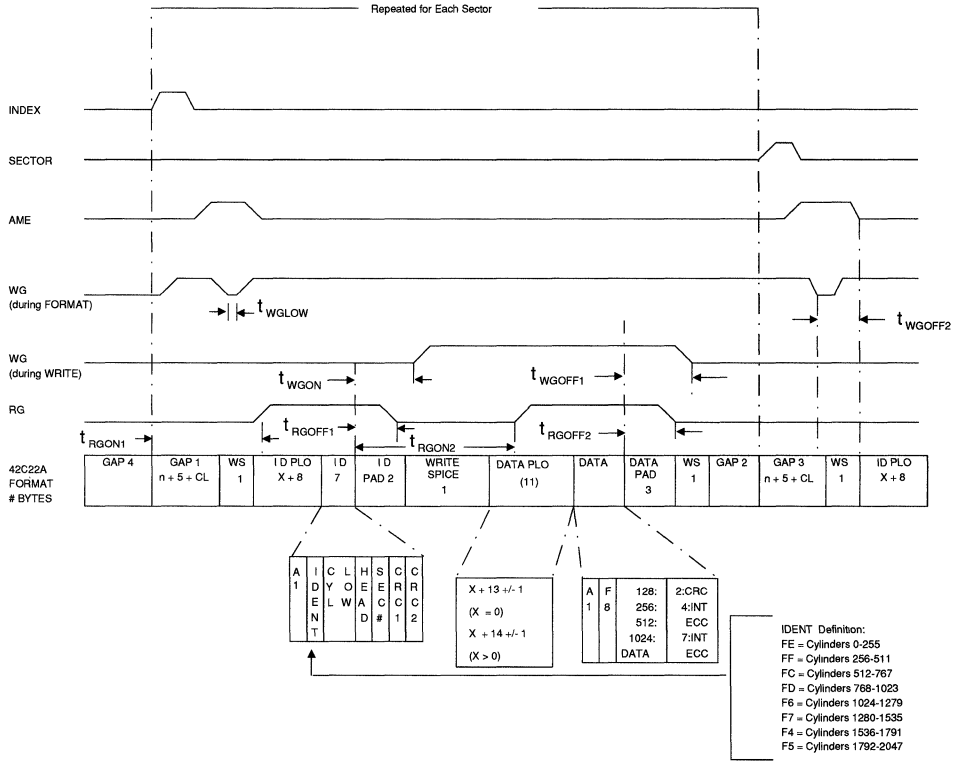


33

NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0 (x > 0).
4. t_{WGON} = 17 ± 1 bit times with respect to RD in.
5. t_{WGOFF1} = 28 bit times with respect to WD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to RD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to RD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). SECTOR is tied to DRUNSCT always. z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to RD in.
10. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)
11. t_{FWGON} = n + 5 + CL byte times with respect to INDEX/SECTOR. t_{WGOFF} = 20 bit times with respect to WD out.

FIGURE 33. HARD SECTOR RLL/MFM TRACK FORMAT (WITH HARD SECTOR READ/WRITE AND WG PULSE)



NOTES

1. n = contents of sector number register during format command.
2. CL = controller latency. 1/2 ≤ CL ≤ 1-1/2 byte times.
3. x = contents of PLO register. ID PLO length is programmable during format command. Data PLO length is programmable during write command. Data PLO length is 11 during format. Data PLO length is 12 ± 1 (or x + 13 ± 1) during write if x = 0.
4. t_{WGON} = 17 ± 1 bit times with respect to NRZRD in.
5. t_{WGOFF1} = 28 bit times with respect to NRZWD out.
6. t_{RGOFF1} = 9 ± 1 bit times with respect to NRZRD in.
7. t_{RGOFF2} = 9 ± 1 bit times with respect to NRZRD in.
8. t_{RGON1} = z + CL byte times with respect to INDEX/SECTOR (SCT). z = contents of internal GAP register.
9. t_{RGON2} = 35 + 1 bit times with respect to NRZRD in.
10. t_{WGLOW} = 2 bit times. t_{WGOFF2} = 8 bit times. Both timings with respect to NRZWD out.
11. GAP2 = Speed tolerance + combined ENDEC delays + other gap requirements, e.g. servo.
GAP2 length = (time between sector pulses) - (time from start of GAP1/GAP3 to end of data pad.)

FIGURE 34. HARD SECTOR NRZ TRACK FORMAT

5.4 PACKAGE DIAGRAMS

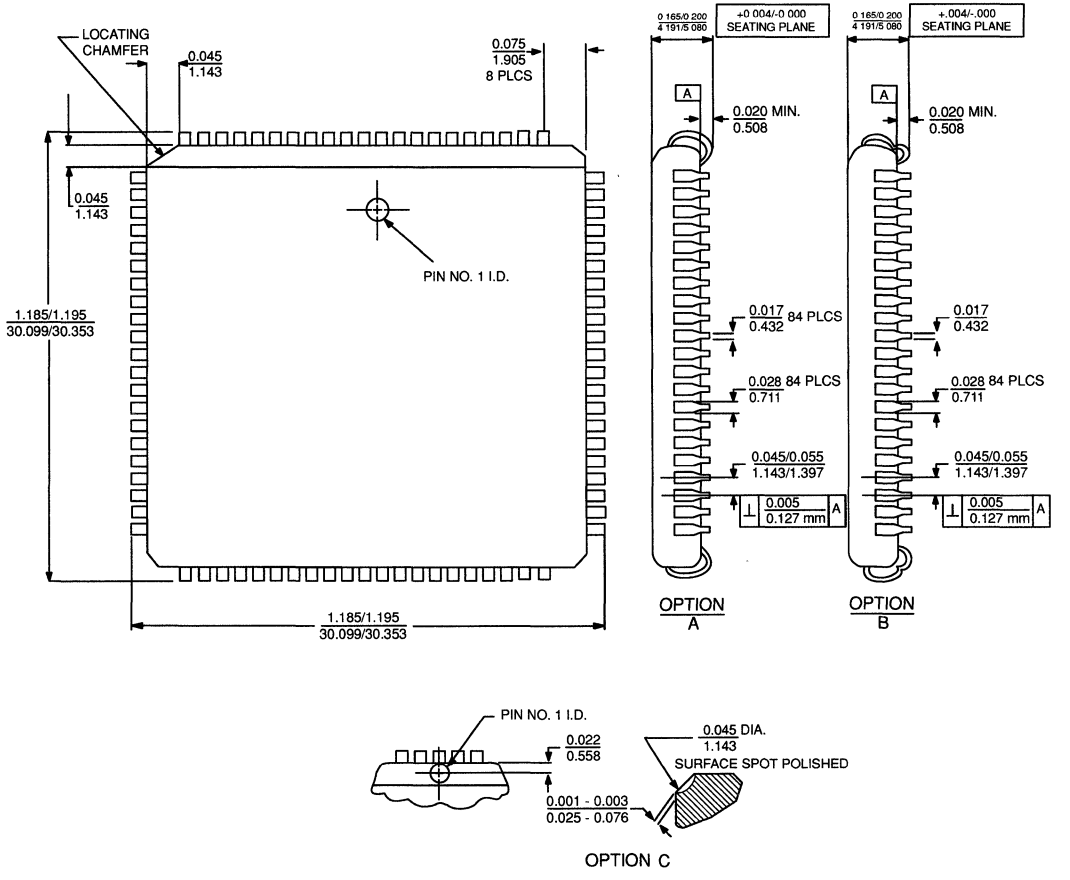


FIGURE 35. 84-LEAD PLCC

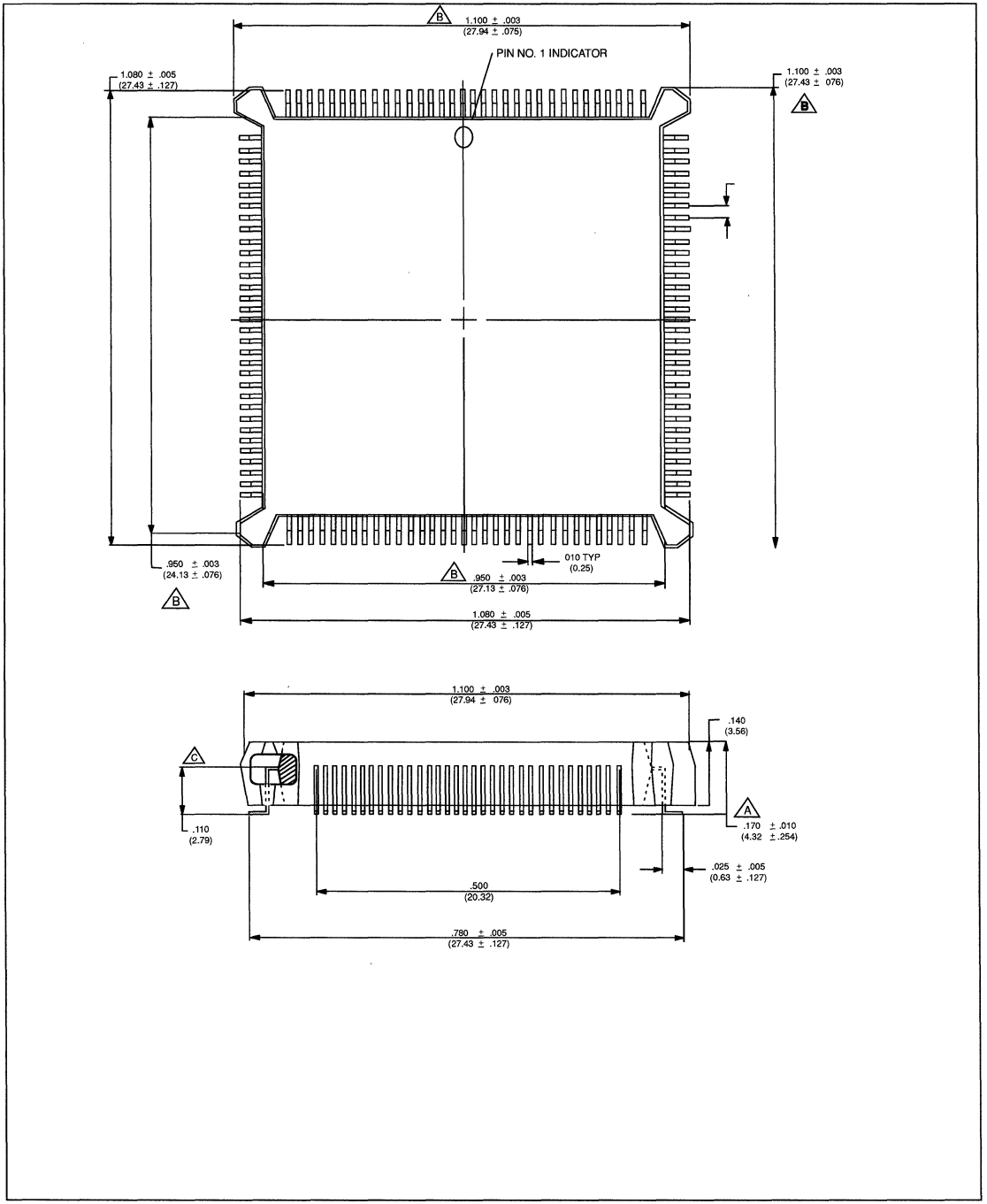


FIGURE 36. 84-LEAD PQFP