WD33C92A

Enhanced SCSI Bus

Interface Controller

WESTERN DIGITAL

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1.0 INTRODUCTION

The 33C92A is a MOS/VLSI device which is implemented in Western Digital's CMOS process. It operates from a single 5 volt supply and is available in either a 44-pin chip carrier or a 48-pin dual-in-line package. All inputs and outputs are TTL-compatible.

1.1 FEATURES

- Implements full SCSI bus features: arbitration, disconnect, reconnect, parity generation/checking on both data ports, soft reset, and synchronous data transfers.
- Synchronous offset selectable from 1 to 12 bytes, with selectable transfer period up to 5 Mbytes/s. ANSI spec compatibility guaranteed to 4 Mbytes/s.
- Compatible with most microprocessors through an 8-bit data bus; supports both multiplexed and non-multiplexed address/data bus systems. Host bus data parity checking and generation is an optional feature.
- Can be used as host adapter (SCSI Initiator) or peripheral adapter (SCSI Target).
- Data transfer options include programmed I/O, single-byte DMA, burst (multibyte) DMA, or direct bus access (WD bus) transfers.
- Burst data transfers up to 4096 bytes.
- Programmable timeout for selection and reselection.
- "Combination" commands greatly reduce interrupt-handling responsibilities.
- Special "Translate Address" command performs the Logical-to-Physical address translation.
- Single +5V supply.
- Available in 44-pin chip carrier or 48-pin DIP.
- Low-power CMOS design.
- Compatible with single-ended or differential external drivers.

2.0 DESCRIPTION

The 33C92A is intended for use in systems which interface to the SCSI (Small Computer System Interface) Bus. The 33C92A can operate in both the initiator (typically, a host computer system) and the target (typically, a peripheral device) SCSI bus roles.

When used in the host system, the 33C92A interfaces to both the host bus and the SCSI bus. To perform a SCSI operation, the host processor must issue a command to the 33C92A to select the desired Target. The 33C92A then arbitrates for the SCSI bus and selects the peripheral unit. If it fails to get the bus because of a device with higher priority, it continues trying, notifying the host when it has succeeded by generating an interrupt. At this point, the 33C92A is operating in the initiator role. When the peripheral requests a SCSI command from the host, the 33C92A receives the request and generates another interrupt to the host. The host responds to this interrupt by issuing a "Transfer Info" command and supplying SCSI command bytes to the 33C92A. The 33C92A transfers the SCSI command to the peripheral, and then waits for the next bus phase request. This process continues until all SCSI information including data, status, and messages have been transferred.

The 33C92A also offers high-level Select-and-Transfer commands, eliminating the interrupt handling otherwise required between each SCSI bus phase.

When the 33C92A is used in a peripheral system, it interfaces with a local processor and the SCSI bus just as it does when used as a host adapter. In this environment, the 33C92A will operate primarily in a Target role. The Target-role command set enables the 33C92A to request each SCSI bus phase individually or to sequence the SCSI bus phases automatically through the use of combination commands.

The 33C92A has an internal microcontroller, a register task file, and SCSI interface logic. This architecture supports both tight control of the protocol for non-standard SCSI implementations, as well as a hands-free mode for standard SCSI applications.

3.0 33C92A PINOUT

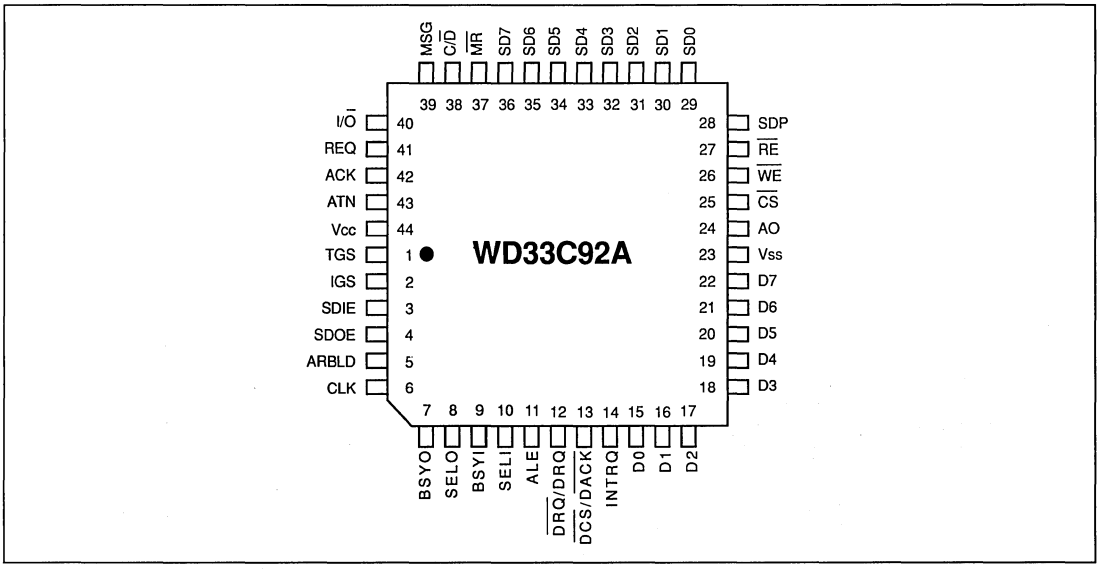

FIGURE 3-1. 44-PIN QUAD PIN DIAGRAM

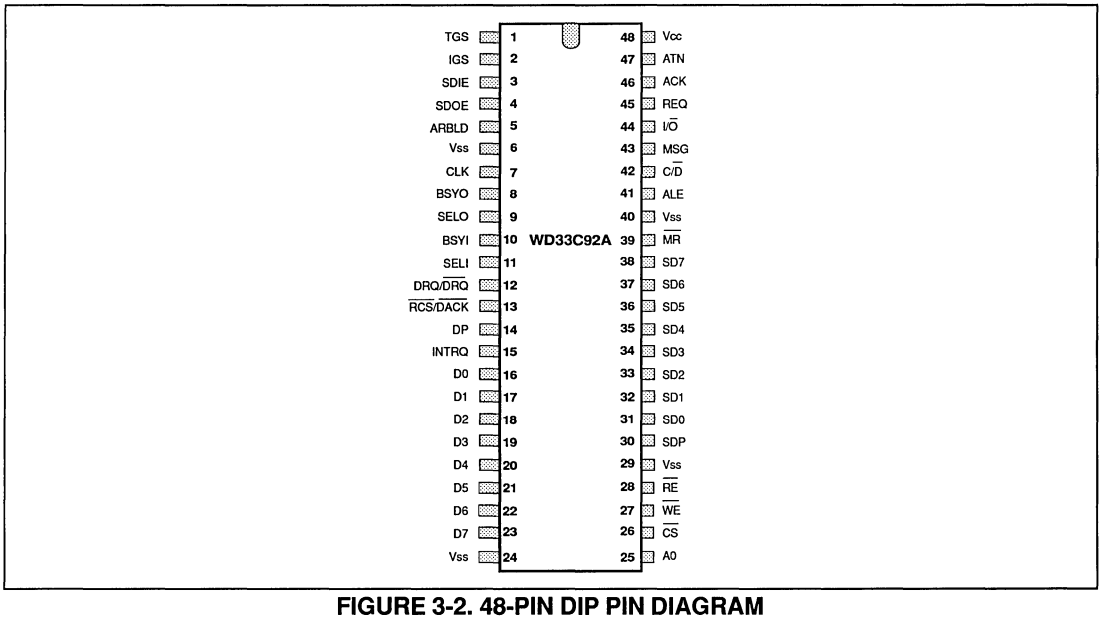

FIGURE 3-2. 48-PIN DIP PIN DIAGRAM

4.0 SIGNAL DESCRIPTIONS

PIN	MNEMONIC	I/O	DESCRIPTION
6	CLK	I	8-20 MHz square wave clock.
37	MR-	I	Reset is an active-low input which forces the 33C92A into an idle state. All SCSI outputs are tristated.
14	INTRQ	O	Interrupt Request to external microprocessor. Indicates command completion/termination or a need to service the SCSI interface. This bit is reset when the SCSI STATUS register is read.
27	RE-	I/O	Read enable is an active-low input which is used with CS- to read a register. In WD Bus mode, it is used as an output to read data from a sector buffer. Also used for DMA transfers. (TRI-STATE)
26	WE-	I/O	Write enable is an active-low input which is used with CS- to write a register. In WD Bus mode, it is used as an output to write data to a sector buffer. Also used for DMA transfers. (TRI-STATE)
25	CS-	I	Chip Select is an active-low input which qualifies RE- and WE- when accessing a register. This signal must be inactive during a DMA cycle (DACK- active in DMA/burst mode or DRQ active in WD Bus mode).
24	A0	I	Address pin used to access the internal registers for non-multiplexed address/data busses (i.e. the ALE pin is grounded). The address of the desired register is loaded into the ADDRESS register during a write cycle with A0=0. The selected register is then accessed when A0=1.
11	ALE	I	Address Latch Enable is used for multiplexed address/data busses to load the address of the desired 33C92A register from the data bus. If indirect addressing is to be used, the ALE pin should be grounded. See the description of the ADDRESS register for a complete discussion of direct and indirect addressing.
13	DACK- (RCS-)	I/O	DMA acknowledge input used for interfacing to an external DMA controller (e.g. 8237). When DACK- is low, all bus transfers are to/from the DATA register regardless of the contents of the ADDRESS register. In WD Bus mode, this pin functions as a RAM chip select output to allow the 33C92A to access a sector buffer. RE- and WE- are outputs when RCS- is active. Since this pin can be an open drain output, a pullup resistor may be required when operating in WD Bus mode.

TABLE 4-1. PROCESSOR/DMA INTERFACE

NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

PIN	MNEMONIC	I/O	DESCRIPTION
12	DRQ-	I/O	Data request is an output when interfacing to (DRQ) an external DMA controller and an input when in WD Bus mode. When used with an external DMA controller, DRQ- and DACK- form the handshake for the data-byte transfers. In Burst mode, DRQ- remains low as long as there is data to transfer. In WD Bus mode, the 33C92A performs burst transfers while DRQ is high, and when DRQ is low, data transfers are inhibited, RCS- is false, and the RE- and WE- outputs are disabled. Since this pin can be an open drain output, a pullup resistor may be required when operating in DMA or Burst mode.
15-22	D7-D0	I/O	Processor data bus.
28	DP	I/O	Data Parity, used only for checking/generating parity during data transfers.

TABLE 4-1. PROCESSOR/DMA INTERFACE (CONTINUED)

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NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

PIN	MNEMONIC	I/O	DESCRIPTION
43	ATN	I/O	ATN is an output in the initiator role and an input in the target role. It is used to indicate the ATTENTION condition.
41	REQ	I/O	REQ is an input in the initiator role and an output in the target role. It indicates a request for a REQ/ACK data transfer.
42	ACK	I//O	ACK is an output in the initiator role and an input in the target role. It indicates an acknowledgement for a REQ/ACK data transfer handshake.
39	MSG	I/O	MSG is an input in the initiator role and an output in the target role. It is asserted during a MESSAGE phase.
38	C/D-	I/O	C/D- is an input in the initiator role and an output in the target role. It is used to indicate whether CONTROL or DATA information is on the SCSI data bus.
40	I/O-	I/O	I/O- is an input in the initiator role and an output in the target role. It controls the direction of data movement on the SCSI data bus with respect to an Initiator.
29-36	SD7 | SD0	I/O	SCSI data bus.
28	SDP	I/O	SCSI data bus parity signal.
9	BSYI	I	BSYI signals the 33C92A that SCSI BSY- is asserted.
7	BSYO	O	The 33C92A asserts BSYO to assert the SCSI BSY- signal.
10	SELI	I	SELI signals the 33C92A that SCSI SEL- is asserted.
8	SELO	O	The 33C92A asserts SELO to assert the SCSI SEL-signal.
3	SDIE	O	Enables SCSI data bus receivers.
4	SDOE	O	Enables SCSI data bus drivers.
5	ARBLD	O	Latches the decoded port number into an external register just prior to the SCSI bus arbitration process.
2	IGS	O	The 33C92A asserts IGS when operating as an Initiator. IGS enables the SCSI drivers for ATN and ACK.
1	TGS	O	The 33C92A asserts TGS when operating as a Target.TGS enables the SCSI drivers for REQ, MSG, C/D- and I/O-.

TABLE 4-2. SCSI INTERFACE

NOTE:

Pin numbers are for the 44-pin quad package.
See Figure 3-2 for the 48-pin positions.

5.0 33C92A BLOCK DIAGRAM

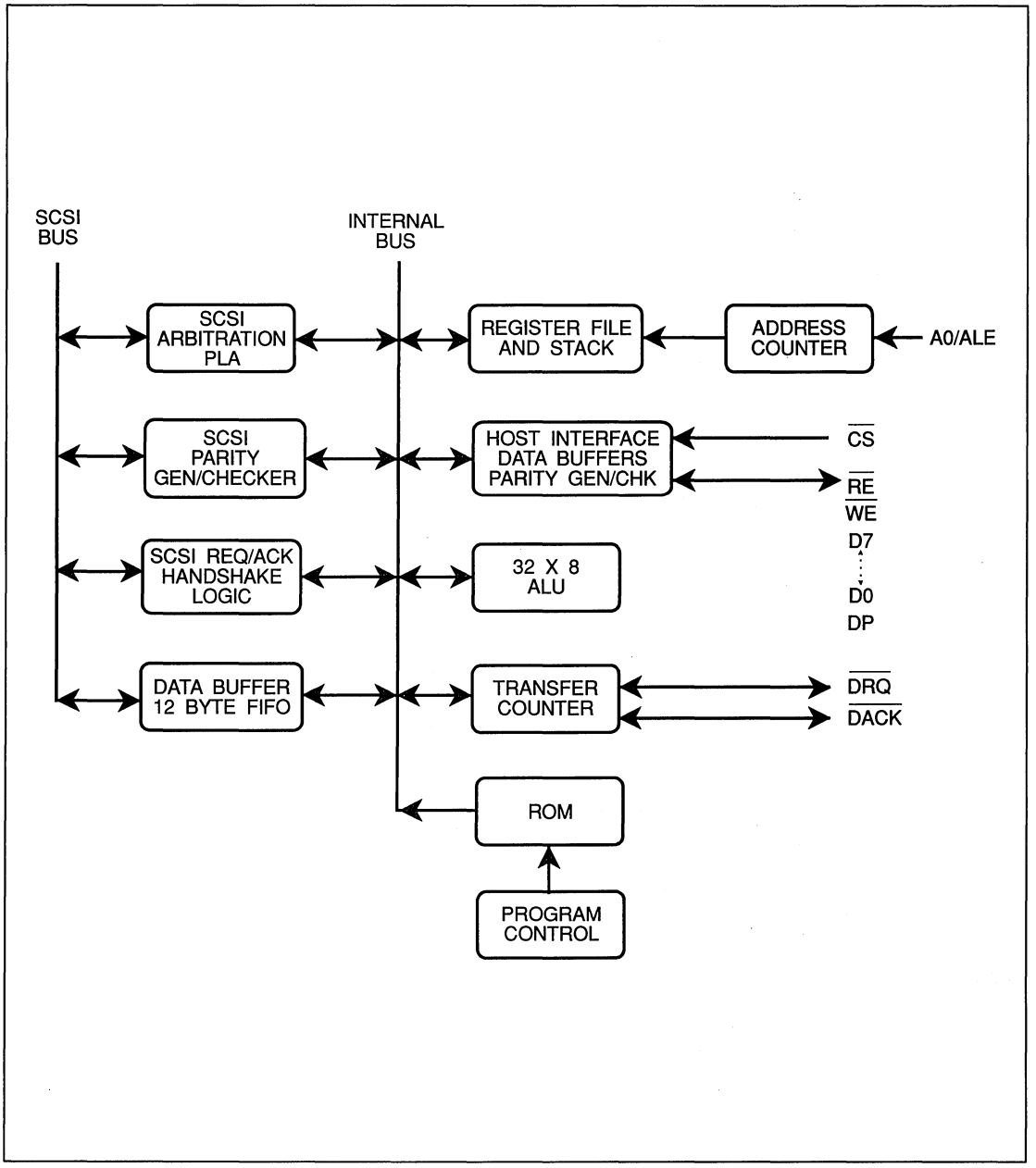

FIGURE 5-1. 33C92A BLOCK DIAGRAM

6.0 33C92A REGISTERS

6.1 REGISTER MAP

A0	R/W	REGISTER ACCESSED	ADDRESS (HEX)
0	R	AUXILIARY STATUS REGISTER	XX
0	W	ADDRESS REGISTER	XX
1	R/W	OWN ID REGISTER /CDB SIZE 00	00
1	R/W	CONTROL REGISTER	01
1	R/W	TIMEOUT PERIOD REGISTER	02
1	R/W	TOTAL SECTORS REGISTER /CDB 1ST	03
1	R/W	TOTAL HEADS REGISTER /CDB 2ND	04
1	R/W	TOTAL CYLINDERS REGISTER(MSB)/CDB 3RD	05
1	R/W	TOTAL CYLINDERS REGISTER(LSB)/CDB 4TH	06
1	R/W	LOGICAL ADDRESS(MSB) /CDB 5TH	07
1	R/W	LOGICAL ADDRESS(2ND) /CDB 6TH	08
1	R/W	LOGICAL ADDRESS(3RD) /CDB 7TH	09
1	R/W	LOGICAL ADDRESS(LSB) /CDB 8TH	0A
1	R/W	SECTOR NUMBER REGISTER /CDB 9TH	0B
1	R/W	HEAD NUMBER REGISTER /CDB 10TH	0C
1	R/W	CYLINDER NUMBER(MSB) REGISTER/CDB 11TH	0D
1	R/W	CYLINDER NUMBER(LSB) REGISTER/CDB 12TH	0E
1	R/W	TARGET LUN REGISTER	0F
1	R/W	COMMAND PHASE REGISTER	10
1	R/W	SYNCHRONOUS TRANSFER REGISTER	11
1	R/W	TRANSFER COUNT REGISTER (MSB)	12
1	R/W	TRANSFER COUNT REGISTER (2ND BYTE)	13
1	R/W	TRANSFER COUNT REGISTER (LSB)	14
1	R/W	DESTINATION ID REGISTER	15
1	R/W	SOURCE ID REGISTER	16
1	R	SCSI STATUS REGISTER	17
1	R/W	COMMAND REGISTER	18
1	R/W	DATA REGISTER	19

NOTES:

1. All unused bits of a defined register are reserved and must be zero.

2. Reading an undefined or unavailable register results in an all-ones data bus output.

3. Register addresses are determined by the ADDRESS register bits AR7 through AR0.

4. When using a multiplexed address/data bus with ALE, the A0 pin is ignored and the ADDRESS register is loaded with ALE. In this mode, the AUXILIARY STATUS register is mapped at hex 1F.

5. See section 6.3 for a description of how reset affects the internal registers.

6.2 REGISTER DESCRIPTIONS

6.2.1 Auxiliary Status Register

The AUXILIARY STATUS register is a read-only register which contains general status information not directly associated with the interrupt condition. The AUXILIARY STATUS register may be accessed at any time, except during DMA accesses (DACK- asserted in DMA/Burst mode or DRQ asserted in WD bus mode).

7	6	5	4	3	2	1	0
INT	LCI	BSY	CIP	0	0	PE	DBR

Bit 0 DBR-DATA BUFFER READY

DATA BUFFER READY is used during programmed I/O to indicate to the processor whether or not the DATA register is available for reading or writing. During Send or Transfer commands which transmit data over the SCSI bus, the DBR bit is set when the 33C92A is ready to take a byte from the host; the bit is reset when the processor writes the byte to the DATA register. During Receive or Transfer commands which receive data over the SCSI bus, the DBR is set when a byte is received; it is reset when the processor reads the byte from the DATA register.

Bit 1 PE-PARITY ERROR

PARITY ERROR status indicates that even parity was detected on a data byte received during an information transfer. Parity is checked on data received from the host bus during transfers out to the SCSI bus and is checked on data received from the SCSI bus during transfers out to the host bus.

Detection of a parity error will set the PE status bit regardless of the state of the HHP or HSP bits in the CONTROL register. The PE bit is cleared when a new command is issued.

Bit 2,3 Not Used

Not used bits are zero.

Bit 4 CIP-COMMAND IN PROGRESS

COMMAND IN PROGRESS, when set, indicates that the 33C92A is interpreting the last command entered into the COMMAND register and therefore this register is unavailable. When this bit is reset, a command may be written to the COMMAND register.

Bit 5 BSY-BUSY

BUSY indicates that a Level II command is currently executing and therefore only the COMMAND register (when CIP = 0), the DATA register, and the AUXILIARY STATUS register are accessible by the host. A Level II command may not be written to the COMMAND register when this bit is one.

Bit 6 LCI-LAST COMMAND IGNORED

LAST COMMAND IGNORED indicates that a command was issued by the host just prior to or concurrent with a pending interrupt, and therefore the command will be ignored.

Bit 7 INT-INTERRUPT PENDING

INTERRUPT PENDING indicates that the INTRQ pin is asserted. The host should read the SCSI STATUS register to clear INTRQ prior to issuing any commands.

6.2.2 Address Register

The ADDRESS register is a write-only register which contains the address of the register to be accessed. Registers in the 33C92A may be accessed in one of two ways:

- Direct addressing (multiplexed address/data busses). In direct addressing, the falling edge of the ALE signal is used to latch the address into the ADDRESS register. The A0 pin should be connected to ground when using this method. The ALE is typically then followed by the CS- and WE- or RE- signals that access the selected register. Also, in direct addressing, the AUXILIARY STATUS register is located at address 1F hex.

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- Indirect addressing (separate address/data busses). In indirect addressing, the register access is performed in two separate cycles. This method is enabled by attaching ALE to ground. First, the ADDRESS register is loaded by performing a write of the desired address to the 33C92A (WE- and CS- asserted) with A0=0. Then the register is accessed by asserting CS- and WE- or RE-, with A0=1. Also, following every access with A0=1, the ADDRESS register will automatically increment to point at the next register, with the exception of the following locations: AUXILIARY STATUS register, DATA register, and the COMMAND register. In indirect addressing, the AUXILIARY STATUS register is accessed by performing a read (CS- and RE- asserted) with A0=0.

6.2.3 Own ID/CDB Size Register

The OWN ID/CDB SIZE register, in its first mode, contains both the encoded ID of the 33C92A on the SCSI bus and several control bits that are used to initially configure the device during the "Reset" command. These bits control 'advanced feature' selection, host bus parity enable, and selection of the divisor for the input clock. In its second mode (when advanced features are enabled, see 7.3), this register is used during the combination commands to specify the SCSI CDB size if the command group is unknown to the 33C92A.

In the first mode, this register (as defined below) is sampled and becomes effective only after a "Reset" command is issued to the device. This register must be initialized, and a "Reset" command must then be issued, following a hardware reset to set the SCSI bus ID, the clock divisor, and the operating modes before any other commands are issued.

In the second mode, bits 3-0 of this register are used during the Select-and-Transfer and Wait-for-Select commands to specify the SCSI Command Descriptor Block size if it is not a group 0, group 1, or group 5 command. This mode is enabled only when advanced features are enabled (see 7.3).

7	6	5	4	3	2	1	0
FS1	FS0	0	EHP	EAF	ID2	ID1	ID0

Bit 0-2 IDn-SCSI ID Bits 0-2

SCSI ID Bits 0-2 set the SCSI bus ID number that the 33C92A will use during arbitration and selection.

Bit 3 EAF-ENABLE ADVANCED FEATURES

ENABLE ADVANCED FEATURES, when set to one, causes the 33C92A to enable certain advanced features (see section 7.3). When this bit is zero, those features are disabled.

Bit 4 EHP-ENABLE HOST PARITY

ENABLE HOST PARITY, when set to one, enables odd parity checking on the host bus; the PE bit in the AUXILIARY STATUS register will indicate parity errors detected on the host bus, and the HHP bit in the CONTROL register will be used. When this bit is zero, no checking is performed on the host bus; the PE bit is not set when a parity error is detected on the host bus, and the HHP bit must be set to zero. NOTE: Parity is always generated on the host data parity bit (DP), regardless of the state of this bit.

Bit 5 Not Used

Not used bits are zero.

Bit 6-7 FSn-FREQUENCY SELECT 0-1

FREQUENCY SELECT 0-1 select the divisor that is applied to the input clock. The resulting clock is used for data transfer timing and for SCSI bus arbitration timing. The table below shows input clock frequency ranges and the corresponding divisors. The correct divisor for the input clock must be used, or SCSI bus timing specifications may not be met.

INPUT CLOCK FREQUENCY (MHZ)	FS1	FS0	RESULTING DIVISOR
8-10	0	0	2
12-15	0	1	3
16-20	1	0	4
xx	1	1	undefined

Note that an 11 MHZ clock rate should not be used, as the resulting SCSI bus clear delay may violate SCSI specifications. The formula for computing the maximum SCSI data transfer rate is:

MAXIMUM SCSI TRANSFER RATE =
INPUT CLOCK FREQUENCY/CLOCK DIVISOR[MByte/sec]

6.2.4 Control Register

The CONTROL register is used to enable/disable certain functions, such as response to parity errors and the SCSI attention condition, interrupt handling, and data transfer modes.

7	6	5	4	3	2	1	0
DM2	DM1	DM0	HHP	EDI	IDI	HA	HSP

Bit 0 HSP-HALT on SCSI PARITY ERROR

The HALT on SCSI PARITY ERROR bit enables the 33C92A to immediately terminate a Receive or Transfer command if a parity error is detected on an incoming SCSI data byte. In the Initiator role, termination due to a SCSI parity error causes the ACK pin to be left in the active state in order to inhibit any additional data transfers (REQs) by the Target; this facilitates error handling with the Target. Synchronous data transfers check parity every 4096 bytes, or at the end of the remaining transfer count, whichever is less. Asynchronous transfers check parity on every byte.

Bit 1 HA-HALT on ATTENTION

The HALT on ATTENTION bit (in Target mode only) enables the 33C92A to terminate a Send or Receive command if the ATN input is asserted. This normally indicates that the Initiator detected a parity error while receiving data from the 33C92A. The ATN input is tested before the start of a data transfer, every 4096 bytes if the transfer count is greater than 4096, and after the end of the transfer. These rules apply to bothsynchronous and asynchronous transfers.

Bit 2 IDI-INTERMEDIATE DISCONNECT INTERRUPT

The INTERMEDIATE DISCONNECT INTERRUPT bit, when set, enables the 33C92A to generate an 85H interrupt and complete a Select-and-Transfer command if the Target disconnects according to the defined SCSI protocol. When this bit is reset, no interrupt is generated by a valid disconnect. This feature, when used with the Resume SAT command, provides support for overlapped SCSI operations. IDI is also used to select execution options in Target mode Combination commands that serve to reduce host system overhead. Refer to Section 7 for more details.

Bit 3 EDI-ENDING DISCONNECT INTERRUPT

When the ENDING DISCONNECT INTERRUPT bit is set, the 16H interrupt which normally follows the COMMAND COMPLETE message during the execution of a Select-and-Transfer command will be suppressed until the Target disconnects from the SCSI bus. EDI is also used in the Target mode Combination commands to enable chaining between those commands, resulting in reduced host system overhead. Refer to Section 7 for more details.

Bit 4 HHP-HALT on HOST PARITY ERROR

The HALT on HOST PARITY ERROR bit enables the 33C92A to immediately terminate a Send or Transfer command if a parity error is detected on an incoming host data byte. Host parity errors are checked according to the rules for checking SCSI parity errors. However, a halt on a host parity error will not hold the ACK signal asserted when an error occurs. Host parity checking is performed at the same intervals as SCSI parity checking.

Bit 5-7 DMx-DMA MODE SELECT

DMA MODE SELECT bits 2-0 are used to select the DMA mode of operation, which describes the host bus transfer mode used during Data In or Data Out phases. The following table describes the different DMA modes, and the state of these bits to select them:

DM2	DM1	DM0	DMA MODE SELECTED
0	0	0	POLLED MODE, or no DMA enabled. All data phase transfers are performed by polling for DBR in the AUXILIARY STATUS register, and then writing (reading) the data to (from) the DATA register.
0	0	1	BURST MODE selects a demand-mode DMA interface. In this mode, the DRQ- signal will be active as long as there is data/space in the internal FIFO to allow the transfer to continue. The DMA controller responds by asserting DACK- and RE-/WE- as long as DRQ- is active.
0	1	0	WD-BUS MODE is selected when the 33C92A is connected to a WD Bus. This mode also can be called Direct Buffer Access (DBA) mode. In this mode, the 33C92A acts as a bus master, and all data access signals reverse their direction: The DRQ- output signal becomes the DRQ input, which enables the 33C92A to drive the buffer bus control signals. The DACK- output signal becomes the RCS- input, which is asserted as a chip select for the buffer. The RE- and WE- inputs become outputs which drive the read and write functions of the RAM buffer. As long as the DRQ signal is asserted, transfers will continue in a burst manner, until the transfer is complete or the decides to pause the transfer by negating the DRQ signal; one more transfer may occur after this transition, and then the DACK-, RE-, and WE- signals are negated.
1	0	0	DMA MODE is selected when the 33C92A is to be used with a DMA controller in single-byte transfer mode. In this mode, DRQ- is asserted and then negated, and the DMA controller responds by asserting DACK- and WE- or RE-, for each data byte transferred to/from the 33C92A.

TABLE 6-1. DMA MODE SELECTED

6.2.5 Timeout Period Register

The TIMEOUT PERIOD register is an 8-bit register containinga preset value which determines the timeout period for Select and Reselect commands. This value may be calculated as a function of the input clock frequency and the desired timeout period, as shown in the following equation:

register value = Tper * Ficlk/80

Where:

Tper = the desired timeout period in milliseconds

Ficlk = the input clock frequency at the MCK pin in Megahertz (with no divisor applied).

The constant '80' scales the units of the equation, as is based on the internal timeout cycle time. The user should round the resulting 'register value' up to the next integral value to ensure that the user's minimum timeout requirement is met.

The timeout period specifies how long the 33C92A will wait for a response (indicated by assertion of the BSY- signal) after it has begun the selection phase (assert SEL- and negate BSY-) before terminating the command. The timeout function can be disabled by loading the TIMEOUT PERIOD register with zero.

The following twelve registers are used exclusively by the Translate Address and/or "combination" commands. The function of each register is determined by the type of command issued.

6.2.6 Total Sectors Register/CDB 1st Byte

Translate Address:
The TOTAL SECTORS register should be set to the total number of sectors per track prior to issuing a Translate Address command.

Select-and-Transfer:
This register should be loaded with the first byte of the COMMAND DESCRIPTOR BLOCK before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the first byte of the received CDB in this register.

6.2.7 Total Heads Register/CDB 2nd Byte

Translate Address:
This register holds the total number of heads during a Translate Address command.

Select-and-Transfer:
This register should be loaded with the second byte of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the second byte of the received CDB in this register.

6.2.8 Total Cylinders Register/CDB 3rd and 4th Bytes

Translate Address:
This is a 16-bit register which holds the total number of cylinders.

Select-and-Transfer:
This register should be loaded with the third and fourth bytes of the CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the third and fourth bytes of the received CDB in this register.

6.2.9 Logical Address Register/CDB 5th-8th Bytes

Translate Address:
The LOGICAL ADDRESS register is a 32-bit register which should be loaded with the logical address to be translated prior to issuing the Translate Address command.

Select-and-Transfer:
For six byte CDBs, only the first two bytes of this register are loaded with the fifth and sixth bytes of the CDB. For ten and twelve byte CDBs, this register is loaded with the fifth, sixth, seventh, and eighth bytes of the CDB.

Wait-for-Select-and-Receive:
The 33C92A will store the fifth, sixth, seventh (if any), and eighth (if any) bytes of the received CDB in this register.

6.2.10 Sector Number Register/CDB 9th Byte

Translate Address:
This register will contain the resulting sector number following a Translate Address command.

Select-and-Transfer:
This register should be loaded with the ninth byte of a ten or twelve byte CDB before issuing a Select-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the ninth byte of a ten or twelve byte received CDB in this register.

6.2.11 Head Number Register/CDB 10th Byte

Translate Address:
The HEAD NUMBER register contains the resulting head number following a Translate Address command. If automatic compensation for spare sectors on a disk is to be performed

by the WD33C92A, then the number of spare sectors per cylinder must be written into this register before issuing the Translate Address command. It should be noted that when compensation is used, the maximum number of cylinders allowed is 4096, and the maximum number of heads is 15. An initial value of zero in this register indicates that no compensation is to be performed.

Select-and-Transfer:
This register should be loaded with the tenth byte of a ten or twelve byte CDB before issuing a Select- and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the tenth byte of a ten or twelve byte received CDB in this register.

6.2.12 Cylinder Number Register/CDB 11th and 12th Bytes

Translate Address:
The CYLINDER NUMBER register is a 16-bit register which contains the resulting cylinder number following execution of the Translate Address command. When a Translate Address command involving automatic compensation for spare sectors is issued (i.e. the HEAD NUMBER register initially contains a nonzero value), then this register must be loaded with total number of sectors per cylinder (total sectors/track * total heads - total spare sectors/cyl) before issuing the command.

Select-and-Transfer:
This register should be loaded with the eleventh and twelfth bytes of a twelve byte CDB before issuing aSelect-and-Transfer command.

Wait-for-Select-and-Receive:
The 33C92A will store the eleventh and twelfth bytes of a twelve byte received CDB in this register.

Send-Status-and-Command-Complete:
The CDB11 register is used to specify the returned status byte to be sent during a Send-Status-and-Command-Complete command. The CDB12 register is used to determine the type of Command-Complete message sent by the 33C92A. If bit 0 of the CDB12 register is set to one, then a linked Command Complete message will be sent during command execution. In this case, bit 1 of the CDB12 register is used as a FLAG bit to determine whether a 0A hex (FLAG=0) or a 0B hex (FLAG=1) Linked Command Complete message is sent. If bit 0 is zero, then a simple Command Complete message (00 hex) is sent.

6.2.13 Target Lun Register

The TARGET LUN register is used to hold both the Logical Unit Number (LUN) and Target status information during various 33C92A commands and sequences. During a Select-and-Transfer or Reselect-and-Transfer command, the contents of this register (along with the SOURCE ID register) are used to generate and check the IDENTIFY messages which are transferred across the SCSI bus. In addition, the TARGET LUN register is used to hold the Target Status byte received during a Select-and-Transfer command.

During Wait-for-Select-and-Receive commands, this register may hold the image of the Identify message received from the Initiator. If the TLV bit is zero, there was no Identify message received. If the TLV bit is one, then a valid Identify message was received. The DOK bit will then indicate whether of not the Initiator has enabled disconnects.

During Reselect-and-Transfer commands, this register is used to set the LUN to be used in the Identify message sent to the Initiator after Selection phase. The TLV and DOK bits are not used.

In advanced mode, during Select-and-Transfer commands, this register is used to handle reselection by an unexpected Target. In this mode, this register will hold the logical unit number of the reselecting target. The TLV and DOK bits will be set to zero.

7	6	5	4	3	2	1	0
TLV	DOK	0	0	0	TL2	TL1	TL0

Bit 0-2 TLx-Target LUN

The Target Logical Unit Numbers bits 0-2.

Bit 3-5 Not Used

Not used bits are zero.

Bit 6 DOK-Disconnects OK

Disconnects permitted.

Bit 7 TLV-TARGET LUN Valid

TARGET LUN Valid.

6.2.14 Command Phase Register

The COMMAND PHASE register is used during combination commands to indicate which phases of these multi-phase commands have been completed. Thus, if the command has terminated abnormally, the processor can read this register to determine the cause of the termination and how to respond to it. This register is also used to resume combination commands by loading this register with a value that indicates the next desired or expected bus phase, and reissuing the command. Refer to the description of the specific commands for details regarding the various command phases and resume values.

7	6	5	4	3	2	1	0
0	CP6	CP5	CP4	CP3	CP2	CP1	CP0

Bit 0-6 CPx-COMMAND PHASE bits0-6

Bit 7 Not Used.
Not used bits are zero.

6.2.15 Synchronous Transfer Register

The SYNCHRONOUS TRANSFER register is used to select between synchronous and asynchronous transfers, and is also used to define the maximum transfer rate. For information phases other than a "data" transfer phase, or when the selected offset is zero (OF3=OF2=OF1=OF0=0), asynchronous transfers will occur. Values greater than zero define a synchronous transfer mode and the offset is determined as shown below. This offset determines the effective FIFO depth for synchronous data transfers, and is typically determined by negotiation with the other SCSI device (as defined in the SCSI standard). The Transfer Period control bits select the minimum transfer period for both synchronous and asynchronous SCSI transfers and, if WD-Bus mode is used, the transfer period and the width of the RE-/WE- strobes for host transfers. The period is defined in terms of the internal clock cycle time; the frequency of this clock is determined by the divisor selected in the OWN ID register.

7	6	5	4	3	2	1	0
0	TP2	TP1	TP0	OF3	OF2	OF1	OF0

Bit 0-3 OFx-OFFSET bit 0-3

OFFSET bits 0-3 are used to select the desired offset according to the following:

3	2	1	0	SELECTED OFFSET
0	0	0	0	0(= Asynchronous data
0	0	0	1	1 phase transfers)
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	Undefined
1	1	1	x	Undefined

Bit 4-6 TPx-TRANSFER PERIOD bits 0-3

The TRANSFER PERIOD bits are used to select the desired transfer period according to the following table:

6	5	4	SCSI/Bus Transfer Period	(SCSI REQ/ACK* & Bus RE-/WE-
0	0	x	8 cycles	4 cycles
0	1	0	2 cycles	1 cycles
0	1	1	3 cycles	1 cycles
1	0	0	4 cycles	2 cycles
1	0	1	5 cycles	3 cycles
1	1	0	6 cycles	4 cycles
1	1	1	7 cycles	4 cycles

*synchronous pulse width & pulse width

The 'cycle' referred to above is the period of the internal data transfer clock after the divisor chosen in the OWN ID register is applied. This period is calculated by the following formula:

cycle = divisor (from OWN ID)(nsec) / 2 * input clock frequency (MHz)

Bit 7 Not Used.

Not used bits are zero.

6.2.16 Transfer Count Register

The TRANSFER COUNT register is a 24-bit register containing a preset value for the internal transfer counter. This preset value is loaded into the internal transfer counter when a Send, Receive, or Transfer command is issued. This counter is used to define command completion by decrementing as each data byte is transferred over the SCSI bus and causing a "successful completion" interrupt when the counter reaches zero. In Combination commands, this register specifies the number of bytes to be transferred during a Data phase.

The counter function can be disabled by loading the TRANSFER COUNT register with zeros prior to issuing a command or by setting the SINGLE-BYTE TRANSFER bit in the COMMAND register concurrent with issuing the command. If the counter is disabled, the Send, Receive, or Transfer command will be completed when a single byte has been transferred.

After the completion of any successful transfer, the TRANSFER COUNT register will be zero. This includes commands issued in Single Byte Transfer mode.

When a transfer is interrupted by a halt on error condition, a SCSI bus phase change, or an abort, the TRANSFER COUNT register will contain the number of bytes NOT successfully transferred to/from the SCSI bus, including clearing the internal FIFO of any bytes left in the FIFO (see DATA register). This FIFO clearing process may cause the TRANSFER COUNT register to differ with the user's DMA controller count, because some bytes may have been transferred into the FIFO, but not to the SCSI bus; therefore, the TRANSFER COUNT should be used to determine the actual number of bytes transferred to/from the SCSI bus.

6.2.17 Destination ID Register

The DESTINATION ID register contains the encoded SCSI bus ID of the device which is to be selected or reselected when a Reselect or Select command is issued. This register also contains control bits that affect the operation of certain combination commands.

7	6	5	4	3	2	1	0
SCC	DPD	0	0	0	DI2	DI1	DI0

Bit 0-2 DIx-DESTINATION ID bits 0-2

DESTINATION ID bits 0-2.

Bit 3-5 Not Used.

Not used bits are zero.

Bit 6 DPD-DATA PHASE DIRECTION,

DATA PHASE DIRECTION, when advanced features are enabled (see 7.3), is used to specify the expected direction of the SCSI data phase, when it occurs. This allows the 33C92A to verify the direction during Select-and-Transfer commands before beginning the transfer. When this bit is zero, the expected direction is out (to the Target). When this bit is one, the expected direction is in (from the Target). An unexpected information phase error will occur if the direction does not match the setting of this bit.

Bit 7 SCC-SELECT COMMAND CHAIN

SELECT COMMAND CHAIN is used only when the Reselect-and-Transfer command is issued with EDI=1. This bit selects which command is chained to when the data transfer is completed. When this bit is zero, a Send-Status-and-Command-Complete command begins executing. When this bit is one, a Send-Disconnect-Message command begins executing.

6.2.18 Source ID Register

The SOURCE ID register is used to report the SCSI bus ID of the device that has selected or reselected the 33C92A. It also contains bits that

enable and control response to selection and reselection.

7	6	5	4	3	2	1	0
ER	ES	DSP	0	SIV	SIV	SIV	SIV

Bit 7 ER-ENABLE RESELECTION

ENABLE RESELECTION, when set to one, enables the 33C92A to respond to a reselection by another device on the SCSI bus. When this bit is zero, any reselection is ignored.

Bit 6 ES-ENABLE SELECTION

ENABLE SELECTION, when set to one, enables the 33C92A to respond to a selection by another device on the SCSI bus. When this bit is zero, any selection is ignored.

Bit 5 DSP-DISABLE SELECT PARITY

DISABLE SELECT PARITY, when set to one, causes the 33C92A to ignore the bus parity when responding to selection or reselection. When this bit is zero, any selection or reselection with a parity error is ignored.

Bit 4 Not Used.

Not used bits are zero.

Bit 3 SIV-SOURCE ID VALID

SOURCE ID VALID is set to one after the 33C92A is selected or reselected if the other SCSI bus device asserted its own bus ID bit (in addition to the bus ID bit of the 33C92A) during the select/reselect phase. This bit is zero if only the bus ID bit of the 33C92A was asserted.

Bit 2-0 SIx-SOURCE ID Bits 2-0

SOURCE ID Bits 2-0 are valid only if the SIV bit is set to one. These bits indicate the SCSI bus ID of the device that selected or reselected the 33C92A.

6.2.19 SCSI Status Register

The SCSI STATUS register is a read-only register which indicates the cause of the most recent INTRQ assertion. INTRQ is asserted whenever a condition occurs within the 33C92A that requires intervention by the host; for example:

- the 33C92A has been reset;
- the command completed successfully;
- the bus phase changed;
- an error occurred.

Once INTRQ has been asserted, the contents of this register will not change until after the SCSI STATUS register has been read or until the 33C92A has been reset.

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7	6	5	4	3	2	1	0
SS7	SS6	SS5	SS4	SS3	SS2	SS1	SS0

Bit 0-3 SSx-SCSI STATUS bits 0-3

SCSI STATUS bits 0-3 are status qualifiers whose meaning depends upon which upper (4-7) status bit is set.

Bit 4-7 SSx-SCSI STATUS bits 4-7

SCSI STATUS bits 4-7 define the type of interrupt that occurred. The possible codes are defined in the following table:

STATUS CODE	GROUP MEANING
0000 xxxx	The 33C92A is in a reset state.
0001 xxxx	A 33C92A command has completed successfully.
0010 xxxx	A 33C92A command has paused or was aborted by an Abort command.
0100 xxxx	A 33C92A command has been terminated prematurely due to an error or other unexpected condition.
1000 xxxx	An event on the SCSI bus requires service.

All other Status Code groups are currently not used and are reserved for future use.

In the following tables, the 'STATE' column indicates the current state in which the Status Code can occur. Also, the MCI field refers to the signals that define a SCSI bus information transfer phase:

MSG, C/D, and I/O. A bit set to one indicates that the signal is asserted on the SCSI bus. A zero indicates negation. Whenever one of these Status Codes occurs, the REQ signal is asserted on the SCSI bus. The following table summarizes the meaning of the MCI field:

MCI CODE	MEANING
000	Data Out phase
001	Data In phase
010	Command phase
011	Status phase
100	Unspecified Info Out phase
101	Unspecified Info In phase
110	Message Out phase
111	Message In phase

STATUS CODE	STATE	SPECIFIC MEANING
0000 0000	DTI	33C92 Reset. The device has been reset, or a Reset command has executed successfully with no advanced features enabled. The new state of the 33C92A is disconnected.
0000 0001	DTI	33C92A Reset. The device has successfully completed a Reset command with advance features enabled. The new state of the 33C92A is disconnected.

TABLE 6-2. RESET STATE INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0001 0000	D	A Reselect command completed successfully. The new state of the 33C92A is connected as a Target.
0001 0001	D	A Select command completed successfully. The new state of the 33C92A is connected as an Initiator.
0001 0010	-	Reserved for future use.
0001 0011	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is not asserted).
0001 0100	DT	A Receive, Send, Reselect-and-Transfer, Wait-for-Select-and-Receive, Send-Status-and-Command-Complete, or a Send-Disconnect-Message command completed successfully (ATN is asserted).
0001 0101	DT	A Translate Address command completed successfully.
0001 0110	D I	A Select-and-Transfer command completed successfully.
0001 0111	-	Reserved for future use.
0001 1MCI	I	A Transfer (non-MESSAGE IN phase) command completed successfully. MCI defines the new information type (SCSI bus phase) being requested.

TABLE 6-3. SUCCESSFUL COMPLETION INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0010 0000	I	A Transfer Info (MESSAGE-IN phase) command has paused with ACK asserted. This allows the host to examine the message before accepting it.
0010 0001	I	A Save-Data-Pointer message was received during a Select-and-Transfer command. The host should save its current data buffer pointer.
0010 0010	D	A Select or Reselect command was aborted.
0010 0011	T	A Receive or Send command was halted by an error or was aborted (ATN is not asserted).
0010 0100	T	A Receive or Send command was halted by an error, assertion of ATN, or was aborted (ATN is asserted).
0010 0101	D	Reserved for future use.
0010 0110	-	Reserved for future use.
0010 0111	D	The 33C92A has been reselected during a Select-and-Transfer (with IDI=0) by a Target that does not match the SCSI bus ID loaded into the DESTINATION ID register, or the following Identify message did not match the LUN loaded into the TARGET LUN register. ACK has been left asserted following the Identify message, and the bus ID and LUN of the reselecting Target are available in the SOURCE ID and TARGET LUN registers. (Advanced Mode only)
0010 1MCI	I	A Transfer command was aborted. MCI define the new information type (SCSI bus phase) being requested.

TABLE 6-4. PAUSED OR ABORTED INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
0100 0000	DTI	An invalid command was issued.
0100 0001	I	An unexpected disconnect (SCSI bus free) by the Target caused a command to terminate. The new state of the 33C92A is disconnected.
0100 0010	D	A timeout occurred during a Select or Reselect command. The state of the 33C92A is disconnected.
0100 0011	TI	A parity error caused a command to terminate ATN is not asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0100	TI	A parity error caused a command to terminate (ATN is asserted). The transfer direction determines whether it is a SCSI or host parity error.
0100 0101	DT	The Logical Address exceeded the disk boundaries.
0100 0110	D	A Target whose SCSI bus device ID does not match the bus ID set in the DESTINATION ID register has reselected the 33C92A during a Select-and-Transfer command (with IDI=0). This interrupt occurs when the 33C92A is not in Advanced Mode. The new state of the 33C92A is connected as an Initiator.
0100 0111	I	A status byte with bad parity was received during a Select-and-Transfer command. ACK is asserted.
0100 1MCI	I	An unexpected information phase was requested. MCI define the SCSI bus phase which is requested.This is typically caused by a phase change before the Transfer Counthas reached zero, or an unexpected phase sequence occurred during a Select-and-Transfer command.

TABLE 6-5. TERMINATED INTERRUPTS

STATUS CODE	STATE	SPECIFIC MEANING
1000 0000	D	The 33C92A has been reselected. The new state of the 33C92A is connected as an Initiator. No Identify message transfer has yet occurred.
1000 0001	D	The 33C92A has been reselected in Advanced Mode. The SCSI bus ID of the Target may be read from the SOURCE ID register. The Identify message from the Target may be read from the DATA register. The ACK signal is left asserted. The new state of the 33C92A is connected as an Initiator.
1000 0010	D	The 33C92A has been selected (no ATN assertion). The new state of the 33C92A is connected as a Target.
1000 0011	D	The 33C92A has been selected (ATN was asserted). The new state of the 33C92A is connected as a Target.
1000 0100	T	The ATN signal has been asserted.
1000 0101	I	A disconnect has occurred. The new state of the 33C92A is disconnected.
1000 0110	-	Reserved for future use.
1000 0111	T	The Wait-for-Select-and-Receive command has paused because the first byte of the incoming CDB is not a known command group. The OWN ID register must be loaded with the CDB length,and the command resumed. The CDB1 register may be examined to determine the SCSI command group from the opcode. The new state of the 33C92A is connected as a Target. (Advanced Mode only)
1000 1MCI	I	The REQ signal has been asserted following connection or when the 33C92A is in the Initiator state and no command is executing. The information phase type should be examined. MCI define the information phase (SCSI bus phase) which is being requested.

TABLE 6-6. SERVICE REQUIRED INTERRUPTS

6.2.20 Command Register

The COMMAND register is used to issue the 33C92A commands. This register should never be loaded when the CIP or INT bits (in AUXILIARY STATUS) are set to one, and a Level II command should never be loaded when the BSY bit is set to one.

The SINGLE-BYTE TRANSFER (SBT) bit in the COMMAND register is only used during information transfer type commands. When this bit is set in conjunction with one of these commands, the transfer counter is disabled and exactly one byte is to be transferred, regardless of the value in the TRANSFER COUNT register. The previous contents of the TRANSFER COUNT register are not preserved.

Refer to the COMMANDS section for a description of the commands and their corresponding command codes.

7	6	5	4	3	2	1	0
SBT	CC6	CC5	CC4	CC3	CC2	CC1	CC0

Bit 0-6 CCx-COMMAND CODE bits 0-6

COMMAND CODE bits 0-6.

Bit 7 SBT-SINGLE-BYTE TRANSFER

SINGLE-BYTE TRANSFER bit.

6.2.21 Data Register

The DATA register is used to transfer data bytes between the host and the SCSI bus during the SCSI information transfer phases (command, data, status, or message phase). It may be accessed by the processor during any type of information phase (simple Level II commands) or via the DMA/WD interface during a SCSI Data In phase or Data Out phase (simple and combination Level II commands).

The DATA register is actually a port for the host interface into the internal twelve byte FIFO of the 33C92A. The FIFO is used for all transfers (synchronous and asynchronous) between the SCSI bus and the host bus, for both DMA and processor access transfers. If the 33C92A is to be halted for any reason (through ABORT, for example), then data transfers with this FIFO must continue until an interrupt occurs. This must be done so that the FIFO is returned to a ready state for subsequent transfers, and to flush incoming data to the host bus.

The DATA register is accessed by the processor during a data phase when the CONTROL register DMA mode select bits are all reset (=0), and when the DBR bit in the AUXILIARY STATUS register is true. The processor writes (reads) the DATA register by loading the ADDRESS register with a hex value of 19 and asserting the WE- (RE-) and CS- pins. This access also occurs during non-data phases.

When the CONTROL register DMA mode select bits are set for DMA mode or BURST mode, the DMA interface is enabled. In this case, the DATA register is written (read) when the DACK- and WE-(RE-) pins are asserted in response to the assertion by the 33C92A of the DRQ- pin.

When the WD BUS is selected by the DMA mode select bits, the RCS- pin functions as an external buffer chip select and the WE- and RE- pins become outputs, allowing the 33C92A to automatically transfer data between its DATA register and the external buffer. In this mode, bus control can be returned to the external processor or any other device by negating the DRQ pin.

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6.3 RESET CONDITIONS

6.3.1 Hardware Reset

The following results occur when the 33C92A is reset by the assertion of the MR- signal:

- The AUXILIARY STATUS register is reset to zero. The INT bit (and the INTRQ pin) is set to one when the hardware reset completes.
- The OWN ID register is reset to zero.
- Advanced mode is disabled.
- The ES, ER, and DSP bits in the SOURCE ID register are reset to zero.
- The SCSI STATUS register is reset to zero.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The internal clock divider circuit is set to divide by two.
- The following host accessible registers are NOT affected by the MR- signal:
  - Registers 01 hex through 15 hex;
  - SOURCE ID (16 hex) register bits 0-3;
  - COMMAND register (18 hex);

The SCSI Soft Reset may be implemented by using the SCSI bus reset signal to cause a reset of the 33C92A (for example, OR the host power on reset signal with the received SCSI bus reset (RST) signal). The host may examine the registers that are not affected by the MR- signal to recover from the SCSI reset condition.

6.3.2 Software Reset

The following results occur when the 33C92A executes the Reset command:

- The DBR bit in the AUXILIARY STATUS register is reset to zero. The INT bit (and INTRQ pin) is set to one when the Reset command is complete.
- All SCSI bus signals are reset to the negated state.
- The internal FIFO, internal transfer counter (not the host accessible register), offsets, and state machines are cleared.
- The OWN ID register is interpreted and the clock divisor, host parity, and advanced mode are configured.
- Registers 01 hex through 16 hex are reset to zero. The COMMAND register (18 hex) is also reset to zero.
- The SCSI STATUS register is set as commanded by the EAF bit in the OWN ID register.

7.0 COMMANDS

7.1 COMMAND LIST

COMMAND CODE (HEX)	COMMAND	VALID STATES	LEVEL
00	Reset	D,T,I	I
01	Abort	D,T	I
02	Assert ATN	I	I
03	Negate ACK	I	I
04	Disconnect	T,I	I
05	Reselect	D	II
06	Select-with-ATN	D	II
07	Select-without-ATN	D	II
08	Select-with-ATN-and-Transfer	D,I	II
09	Select-without-ATN-and-Transfer	D,I	II
0A	Reselect-and-Receive-Data	D,T	II
0B	Reselect-and-Send-Data	D,T	II
0C	Wait-for-Select-and-Receive	D,T	II
0D	Send-Status-and-Command-Complete	T	II
0E	Send-Disconnect-Message	T	II
0F	Set IDI	D,T,I	I
10	Receive Command	T	II
11	Receive Data	T	II
12	Receive Message Out	T	II
13	Receive Unspecified Info Out	T	II
14	Send Status	T	II
15	Send Data	T	II
16	Send Message In	T	II
17	Send Unspecified Info In	T	II
18	Translate Address	D,T	II
20	Transfer Info	I	II

33C92A States:
D = Disconnected
T = Connected as a Target
I = Connected as an Initiator

Command Levels:
I = Level I command
II = Level II command

7.2 33C92A COMMAND TYPES

There are two basic types of 33C92A commands: Level I and Level II. Level I commands may be issued while a Level II command is in progress (indicated by an AUXILIARY STATUS of BSY=1,CIP=0) and, except for the "Abort" and "Reset" commands, do not generate an interrupt upon their completion. Level II command execution will always result in an interrupt. If a Level II command is issued while another Level II command is executing, unpredictable results may occur.

There are two types of Level II commands. 'Simple' Level II commands are associated with a single operation or phase (for example, selection or information transfer). 'Combination' Level II commands combine multiple phases into a single 33C92A command to minimize interrupt overhead. The Initiator combination commands 'expect' certain SCSI bus phases at certain times during a sequence. These expected phases are based on common sequences performed by a Target on the SCSI bus; any deviation causes an interrupt. Target combination commands can be chained together to further minimize interrupt overhead by creating longer phase sequences.

NOTE: When using command chaining, care must be taken to ensure that all commands in the chain are initialized prior to issuing the command.

The 33C92A will be in one of three "states" during operation: Disconnected, Connected as a Target, or Connected as an Initiator. Certain commands are valid only in particular states as indicated in the COMMAND LIST. An attempt to issue a Level II command which is invalid for the present 33C92A state will cause an "invalid command" interrupt. Level I commands issued in invalid states will be ignored.

7.3 ADVANCED MODE FEATURES

The 33C92A has several new features included which add new functions to the original 33C92 design. Some of these features cause the 33C92A to be incompatible with the 33C92. These features have been grouped together under the heading of 'Advanced Mode' features. These features are disabled when the 33C92A is reset by the MR- signal (hardware reset). They must be enabled by the host by issuing the 'Reset' command with the 'Enable Advanced Features' (EAF) bit set in the OWN ID register. The host can determine if advanced features have been enabled (thereby implying that a 33C92A is installed) by examining the SCSI STATUS register after issuing the 'Reset' command.

The features enabled by this bit are described in the subsections below.

7.3.1 Unexpected Reselection

When in normal (33C92) mode, a reselection when idle (ER=1) or when disconnected during a Select-and-Transfer command (and the Target bus ID does not match the DESTINATION ID register) causes an immediate interrupt after the reselection handshake is complete. In Advanced Mode, the 33C92A will continue to the Message In phase to fetch the Identify message. If the 33C92A was idle, the SCSI STATUS register will be set to 81 hex, and the Identify message will be in the DATA register. If the 33C92A was executing a Select-and-Transfer command, the SCSI STATUS register will be set to 27 hex, and the Identify message will be in the TARGET LUN register. In either case, the SOURCE ID register will contain the SCSI bus ID of the reselecting Target, and the ACK signal remains asserted so that the Identify message may be rEjected.

7.3.2 Unknown SCSI Command Groups

When a SCSI Command Descriptor Block is transferred on the SCSI bus, the command length in bytes is determined by the group code, which is found in bits 7-5 of the first command byte, or opcode. Group 0 (opcodes 00 to 1F hex), group 1 (opcodes 20 to 3F hex), and group 5 (opcodes A0 to BF hex) commands are defined by the SCSI standard (X3.131-1986) as six, ten, and twelve byte commands, respectively. All other command groups are undefined by that standard. In normal mode, the 33C92A will assume that these undefined groups are six byte commands when executing Select-and-Transfer or Wait-for-Select-and-Receive commands. In Advanced Mode, the following events will occur:

Select-and-Transfer:

When loading the CDB into the CDB registers prior to issuing the command, the host also loads the expected command length into the OWN ID register. The 33C92A uses

this value to make sure the correct number of bytes are then transferred in the command phase.

Wait-for-Select-and-Receive

When receiving the CDB from the Initiator, the 33C92A will check the first CDB byte as soon as it is received. If the group is undefined, an interrupt will occur so that the host can examine the first command byte in the CDB 1ST register, and then load the TOTAL command length into the OWN ID register. The SCSI STATUS register is set to 87 hex, and the COMMAND PHASE register is set to 31 hex, when this interrupt occurs. After the interrupt, the 33C92A will only accept a Resume Wait-for-Select-and-Receive command, Abort, Disconnect, or Reset command. All other commands are invalid; during the interrupt processing, the 33C92A will continue to transfer the first six bytes of the command into its internal FIFO.

7.3.3 Data Phase Direction

During a Select-and-Transfer command in normal mode, the Data phase direction is determined solely by the Target; if this direction does not match the direction expected by the host, the 33C92A will not detect this error but expects that the transfer will continue. In Advanced Mode, the DPD bit in the DESTINATION ID register is compared with the state of the I/O signal on the SCSI bus. If the expected and actual directions do not match, an interrupt will occur with 'unexpected phase' status in the SCSI STATUS register.

7.4 LEVEL I COMMANDS

7.4.1 Reset (00 hex)

The Reset command performs a similar function to the hardware reset caused by asserting the MR- pin except that the OWN ID register is sampled for information concerning the operating configuration of the 33C92A. The 33C92A is also initialized as described in the RESET CONDITIONS section. The Reset command may be executed in any 33C92A state and will force the 33C92A into the Disconnected state, aborting any previously issued command in progress. Upon completion of the Reset command, an interrupt is generated the SCSI STATUS will be 00 hex or 01 hex, depending on the contents of the OWN ID register.

7.4.2 Abort (01 Hex)

The Abort command is valid in the Disconnected and Connected-as-Target states. The Abort command has different effects depending on the state and the command that is currently executing, as described below:

Disconnected State

In the Disconnected state, the Abort command may be used to halt an attempted Select, Select-and-Transfer, Reselect, or Reselect-and-Transfer command. If the Abort command is issued following a Select or Reselect command and the WD33C92A has won arbitration, the WD33C92A releases the SCSI bus by removing the Bus ID bits while SEL- is asserted and checking for a negated BSY- signal. If, after at least 200 us, there is no BSY- response, the WD33C92A goes to a Bus Free condition, and a "paused/aborted" interrupt is generated. If there is a response within this time period, then a "successful completion" interrupt will result instead. If the WD33C92A has not yet won arbitration, it will immediately abort the Select or Reselect command. The abort command will also terminate a Wait-for-Select-and-Receive command, if selection has not already begun. Once selected, the WD33C92A will ignore any abort attempts, and the command will finish normally.

Target State

When the WD33C92A is in a Connected-as-a-Target state, the Abort command may be used to abort Receive, Send, or the data phase portion of a Target combination command.
When issuing an Abort in the Connected-as-a-Target state, the following rules apply:

1. When a Abort command is issued to abort a Send or Reselect-and-Send command, the local processor must not service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the SCSI bus. The WD33C92A removes the data request at

an arbitrary time during the Abort command processing and the data request is not valid once the Abort command is written to the COMMAND register.

2. When a Abort command is issued to abort a Receive or Reselect-and-Receive command, the local processor must CONTINUE to service any data request (DBR, DRQ, etc.) from the WD33C92A until an interrupt from the WD33C92A occurs. This is required to allow the FIFO to clear; the Abort processing will not complete until the FIFO contents are flushed to the local processor.

After the Abort command is processed and the local processorhas received the interrupt indicating this, the TRANSFER COUNT register contains the number of bytes that were not successfully transferred with the SCSI bus. The WD33C92A remains in the Connected-as-a-Target state. The WD33C92A is now ready to receive any appropriate Target mode command, including a resume of the command that was aborted.

7.4.3 Disconnect (04 hex)

The Disconnect command may be used in either the Target or the Initiator connected states. In the Target role, the Disconnect command is the normal procedure for disconnecting from the SCSI bus following the information transfer phase. In the Initiator role, Disconnect can be used to release the bus following a timeout condition. The Disconnect command causes the immediate release of all bus signals and, in Target mode, returns the SCSI bus to the Bus Free phase. If the Disconnect command is issued during an active Level II command, the Level II command is immediately terminated and the 33C92A transitions to the Disconnected state.

7.4.4 Assert ATN (02 hex)

The Assert ATN command is only valid when Connected as an Initiator. It is normally used to allow the Initiator to inform a Target that it has a message pending (The Target is expected to respond by performing a Message Out Phase). ATN is automatically negated:

- before the last byte of a Transfer Info command issued in response to the Message Out phase;
- when the Identify message out is transferred to the Target during a Select-and-Transfer command;
- when a SCSI Bus Free phase occurs.

The Select-with-ATN and Select-with-ATN-and-Transfer commands will cause the 33C92A to automatically assert ATN prior to the release of SEL- providing the bus arbitration is won.

7.4.5 Negate ACK (03 hex)

The Negate ACK command causes ACK to be negated. It may be used:

- When Connected as an Initiator following Message-In Transfer Info commands.
- After the 33C92A has detected a parity error on any received information and the HALT on SCSI PARITY ERROR (HSP) bit is set.
- After unexpected reselection in advanced mode.
- After a Save-Data-Pointer message is received during a Select-and-Transfer command.
- Host parity errors do not affect the ACK signal. For all other Initiator transfers, ACK negation is automatic.

In the case of a Message-In transfer, incoming messages may be rejected and the Initiator may indicate its intent to send either a "MESSAGE REJECT" or a "MESSAGE PARITY ERROR" Message by issuing the Assert ATN command prior to issuing the Negate ACK command. If the incoming message is to be accepted, only the Negate ACK command should be issued.

During non-Message-In transfers, if the Transfer command is terminated by a parity error, the Assert ATN command can again be issued prior to

Negate ACK, this time indicating the Initiator's intent to send an "INITIATOR DETECTED ERROR" Message.

7.4.6 Set IDI (0F hex)

The Set IDI command is used in the Initiator role to support overlapped SCSI operations. If a SCSI command is executing via a Select-and-Transfer command, then the Set IDI command may be used to set the IDI bit in the CONTROL register, which then causes an interrupt to occur upon a Target disconnection. This ability allows the IDI bit to be left reset when the first SCSI operation is started, which may reduce the number of 33C92A interrupts, yet also allows a second operation to be started when needed without waiting for the first operation to be completed.

7.5 SIMPLE LEVEL II COMMANDS

7.5.1 Select-with-ATN (06 hex)

Select-with-ATN is valid only in the Disconnected state and when issued will cause the 33C92A to select a Target. Before issuing this command, the SCSI Bus ID of the Target device should be written into the DESTINATION ID register. When the Select-with-ATN command is issued, the 33C92A begins bus arbitration. If the 33C92A is selected or reselected by another device during the arbitration, the Select-with-ATN command is aborted and a "service required" interrupt (8x hex) is generated.

Should the 33C92A win the arbitration, SEL- and ATN are asserted, the Target and Initiator Bus IDs are placed on the SCSI data bus, and then BSY- is deasserted. At this time, a timeout sequence whose length is determined by the value in the TIMEOUT PERIOD register begins. If BSY- is not asserted by the Target before a timeout occurs, the 33C92A begins its selection abort sequence (as described in the Abort command description), and if there is no Target response the Select-with-ATN command is terminated and a "terminated" interrupt is generated. If the Target responds before the timeout period has elapsed or before the selection abort sequence is complete, the 33C92A negates the SEL-signal, putting the 33C92A in a Connected-as-an-Initiator state. A "successful completion" interrupt indicates that the Select-with-ATN command has been completed successfully.

If the 33C92A does not win the arbitration or there is no response from the Target and the timeout feature is disabled, the Select-with-ATN command can be aborted with an Abort command. When the Abort command is successfully executed under these circumstances, the 33C92A is disconnected from the bus and a "paused/aborted" interrupt is generated.

7.5.2 Select-without-ATN (07 hex)

The Select-without-ATN command is identical to the Select-with-ATN command except that ATN is not set during the Selection Phase.

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7.5.3 Reselect (05 hex)

The Reselect command is identical to the Select-without-ATN command except that the I/O signal is asserted upon completion of the Arbitration Phase. Successful completion of the Reselect command results in the 33C92A being Connected as a Target.

7.5.4 Receive (10-13 hex)

There are four Receive commands which are distinguished from each other only by the state of three SCSI interface signals and the type of data that is transferred. These commands, consisting of the Receive Command, Receive Data, Receive Message Out, and Receive Unspecified Info Out commands are valid only in the Connected-as-a-Target state. The type of the Receive command selected determines the state of the I/O-, C/D-, and MSG outputs during the command according to the following chart (1=asserted):

Receive Command Type	OP Code	MSG	C/D	I/O
Receive Command	10	0	1	0
Receive Data	11	0	0	0
Receive Message Out	12	1	1	0
Receive Unspecified Info Out	13	1	0	0

The Receive commands are information transferring commands and are therefore dependent on the SBT bit in the COMMAND register for deter-

mination of a successful completion. In addition to a termination caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Receive command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred.
3. A parity error has been detected on one of the received data bytes (and HSP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.
6. A Disconnect command is issued.

When the Receive command is completed as a result of receiving the correct number of bytes, a "successful completion" interrupt will be generated. If a parity error has caused termination, a "terminated" interrupt will instead be generated. In this case, the TRANSFER COUNT register will contain the number of bytes yet to be transferred. After any completion or termination of the Receive commands except those due to a subsequent Disconnect command or reset, the 33C92A is in the Connected-as-a-Target state.

As data transfer commands, the Receive commands are dependent on the DMA mode select bits in the CONTROL register for the DATA register accessing mode. These bits determine whether the DATA register accesses will be handled by the processor or through a DMA/WD interface. When the processor is required to read the DATA register (i.e. DMA mode select bits=0), it must monitor the DBR status bit (in AUXILIARY STATUS) to determine when a byte is available for reading. During Receive commands, this status bit will be reset when a byte is read from the DATA register and set when a byte is loaded into the DATA register via the SCSI interface. DBR is also reset when a Receive command is issued.

All information transfers involving other than data information are asynchronous. However, if the information phase involves data transfers, the SYNCHRONOUS TRANSFER register will be evaluated. In this case, any selected offset other than zero results in synchronous transfers. The minimum Transfer Period for both types of transfers is determined by the transfer period bits in this same register.

7.5.5 Send (14-17 hex)

As in the case of the Receive commands, there are four Send commands which are distinguished only by the state of the I/O-,C/D-, and MSG pins and the type of data that is transferred. The four Send commands, also valid in the Connected-as-a-Target state only, are the Send Status, Send Data, Send Message In, and Send Unspecified Info In commands. The SCSI pin states during the Send commands are determined by the particular command as follows (asserted=1):

Send Command Type	OP Code	MSG	C/D	I/O
Send Status	14	0	1	1
Send Data	15	0	0	1
Send Message In	16	1	1	1
Send Unspecified Info In	17	1	0	1

The Send commands are also information transferring commands and as such are also dependent upon the SBT bit in the COMMAND register for command completion. In addition to that caused by reset (via either a Reset command being issued or assertion of the MR- pin), a Send command completion or termination will occur under any of these conditions:

1. The internal transfer counter is disabled (SBT=1 or the TRANSFER COUNT register is loaded with zero) and a single byte has been read from the DATA register.
2. The counter has decremented to zero (with SBT=0) indicating that the specified number of bytes have been transferred
3. A parity error has been detected on one of the data bytes from the host (and HHP=1).
4. The ATN pin is asserted (and HA=1).
5. The Abort command is issued.

6. A Disconnect command is issued. The 33C92A remains Connected-as-a-Target following the Send command completion/termination unless the Disconnect command or reset was used to force a termination.

During a Send command, DATA register accessing is controlled by the DMA mode select bits in the CONTROL register. When these bits are set to the appropriate mode, loading of the DATA register is accomplished by a DMA controller or through the WD-Bus interface. If the DMA mode select bits are zero, the processor must poll the AUXILIARY STATUS register and can write to the DATA register only when the DATA BUFFER READY bit is set (DBR=1). Send commands cause the DBR bit to be reset every time the processor loads a byte into the DATA register and set when a byte is transferred from the DATA register onto the SCSI data bus. The DBR bit will also be set upon issuing a Send command.

As in the case of Receive commands, synchronous transfers will occur only when data transfers are involved and an offset other than zero is selected.

7.5.6 Transfer Info (20 hex)

The Transfer Info command is valid only when Connected as an Initiator and is used to send and receive data, command, status, and message information.

The first REQ assertion following connection as an Initiator results in a "service required" interrupt. The processor should examine the SCSI STATUS register to determine the type and direction of information transfer requested by the Target, and then issue a Transfer Info command in response. While an Initiator, the 33C92A will also generate an interrupt each time the Target device requests a new type of information transfer phase.

As in the case of the Send and Receive commands, when completion of the Transfer Info command depends upon the internal transfer counter, the processor should load the TRANSFER COUNT register prior to issuing this command. The DMA mode select bits in the CONTROL register, the offset and transfer period bits in the SYNCHRONOUS TRANSFER register, and the SBT bit in the COMMAND register are used during Transfer Info commands just as they are during the Send and Receive commands. However, for processor access of the DATA register during Transfer Info commands (when the DMA mode select bits are zero or the bus phase is other than Data phase), behavior of the DATA BUFFER READY (DBR) status bit is determined by the direction of information transfer as defined by the I/O- pin. When the transfer is from Initiator to Target, the DBR bit is reset by writing to the DATA register and is set when the byte is transferred from the DATA register onto the SCSI data bus. When the transfer is from Target to Initiator, DBR is set when a byte is received over the SCSI data bus and transferred into the DATA register and is reset by reading the DATA register. DBR is also reset whenever a Transfer Info command is issued.

There are several causes of a Transfer Info command completion/termination in addition to a reset. Just as for a Send or Receive command, the Transfer Info command can be terminated by issuing a subsequent Disconnect command, causing an immediate disconnect but no interrupt.

A Transfer Info command will either complete or pause when the specified number of bytes (either a single byte or multiple bytes as defined by the SINGLE-BYTE TRANSFER bit in the COMMAND register) has been sent or received. The 33C92A generates a "successful completion" interrupt only after receiving another REQ from the Target during non-Message-In information phases but generates a "paused/aborted" interrupt for Message-In phases without waiting for an additional REQ (Note that when the completed Transfer Info command was a Message-In transfer phase, the ACK pin will be left asserted by the 33C92A in the last REQ/ACK cycle of the command, and the processor is required to issue a Negate ACK or an Assert ATN followed by a Negate ACK command to accept or reject the message).

If a parity error is detected on a data byte received from the SCSI bus (and HSP=1) or on a data byte byte received from the host (and HHP=1), then the 33C92A will terminate the command and, for SCSI parity errors, will leave ACK asserted (to also halt the Target). In this case a "terminated" interrupt is generated. Finally, a negation of the BSY- signal (i.e. the Target suddenly disconnects) or a transition in the I/O-, C/D-, and/or MSG pins during a Transfer command will also terminate the command and generate a "terminated" interrupt.

If a parity error is detected on a received byte but parity error command termination is disabled (HSP=0 or HHP=0, as appropriate), the 33C92A will still set the PARITY ERROR status bit in the AUXILIARY STATUS register but will not terminate the command as a result of this error.

7.5.7 Translate Address (18 hex)

The Translate Address command performs a logical-address to physical-address translation. Certain SCSI commands involve a logical address which may be up to 32 bits in length. When a command is detected which requires address translation, the processor can load the logical address into the 33C92A LOGICAL ADDRESS register and then issue the Translate Address command to have the 33C92A do the conversion. Upon receiving a "successful completion" interrupt, the processor can read the CYLINDER NUMBER, HEAD NUMBER, and SECTOR NUMBER registers to extract the logical address. The disk parameters contained in the TOTAL SECTORS, TOTAL HEADS, and TOTAL CYLINDERS registers must also be valid before issuing a Translate Address command.

If automatic compensation for spare sectors is to be performed by the WD33C92A, then the number of spare sectors per cylinder and total number of sectors per cylinder must also be loaded, respectively, into the HEAD NUMBER and CYLINDER NUMBER registers. A "terminated" interrupt will occur if any division operation performed during this command results in an overflow.

7.6 COMBINATION LEVEL II COMMANDS

7.6.1 Select-and-Transfer (08 and 09 hex)

The Select-and-Transfer commands greatly reduce the host or local processor interrupt-handling burden by enabling the 33C92A's internal microprocessor to manage the low-level SCSI protocol, resulting in as few as one interrupt per SCSI operation. Select-and-Transfer commands are used when in an Initiator role, and typically consist of at least the following SCSI phases:

1. Selection of a Target device.
2. Sending of a command.
3. Reception of status information.
4. Reception of a COMMAND COMPLETE Message.

These commands optionally consist of a Data Transfer phase and additional Message Transfer phases.

The 33C92A will update the COMMAND PHASE register as the Select-and-Transfer command executes. Upon completion or termination of the command, the local processor can read this register to determine where the SCSI operation stopped.

The two Select-and-Transfer commands differ from each other only by whether or not the ATN pin is asserted during the Selection phase. The ability to assert ATN during Selection supports the SCSI Message Protocol which calls for an IDENTIFY Message Out phase following the Selection. When executing a Select W/ATN-and-Transfer commands, the 33C92A expects the Target to request a Message Out phase immediately following selection, whereas for a Select W/O ATN-and-Transfer command, it expects the Target to directly enter Command phase. The Select-and-Transfer commands, moreover, support Group 0 (6-byte CDB), Group 1 (10-byte CDB), and Group 5 (12-byte CDB) SCSI commands.

When a Select-and-Transfer command is issued, the 33C92A arbitrates for the bus and selects a Target just as during a Select command. If the Target does not respond before a timeout occurs, the Select-and-Transfer command halts and a "terminated" interrupt is generated. Failure to complete the Selection phase is also indicated by the fact that the COMMAND PHASE register contains all zeros. If the Selection is successful, no interrupt is generated, but the COMMAND PHASE register will be set to a hex 10.

After completing the Selection phase, the 33C92A begins an information transfer phase. If ATN has been asserted (i.e. a Select W/ATN-and-Transfer command was issued), the 33C92A expects the Target to respond with a Message Out phase. If the first information phase request is other than a Message Out request, the 33C92A will terminate the command and generate a "terminated" interrupt. However, when the Target does request a Message Out phase, the 33C92A will respond by automatically sending an IDENTIFY Message. This single byte message is of the binary

form: 1r000ttt, where r=1 if the ENABLE RESELECTION bit in the SOURCE ID register is equal to 1, and ttt is the encoded Target LOGICAL UNIT NUMBER contained in the TARGET LUN register. Once the IDENTIFY Message has been sent, the 33C92A will set the COMMAND PHASE register to hex 20.

Following the Message Out phase (or Selection phase when ATN was not asserted during Selection), a Command phase is expected by the 33C92A. Again, and throughout the entire Select-and-Transfer command execution, if the Target requests an unexpected information phase type, the 33C92A terminates the command and generates a "terminated" interrupt. If the Command phase is requested in this situation, the 33C92A will extract the SCSI command from the internal COMMAND DESCRIPTOR BLOCK registers and send the 6-, 10-, or 12-bytes of command information as determined by its evaluation of the SCSI command code in the CDB1 register. The COMMAND PHASE register is set to hex 30 before the first Command byte is sent and then increments with each byte transferred, so that for a 12-byte CDB command the COMMAND PHASE register will contain hex 3C when all bytes of the CDB have been transferred.

After the Command phase, the 33C92A expects either a Data In phase, Data Out phase, Status phase, or Message In phase. If the Target is requesting a Message In phase, a pending disconnection is assumed. The 33C92A therefore expects to receive either a Save-Data-Pointer message (hex 02) or a Disconnect message (hex 04). If either message is incorrect, or if a different message is received, a "terminated" interrupt will be generated to alert the processor of that fact and to allow the message to be read from the DATA register. A "terminated" interrupt will also be generated if the Target disconnects before sending the Disconnect message. When a correct Save-Data-Pointer message is received, a "paused/aborted" interrupt is generated and the Select-and-Transfer command terminated to allow the processor to save the SCSI data pointer. However, if a Disconnect message is received, the COMMAND PHASE register will be updated to hex 42 and command execution continues.

When the actual Target-disconnection does occur, the COMMAND PHASE register is updated to hex 43 and if the IDI bit is set, the WD33C92A terminates the Select-and-Transfer command by generating an 85H interrupt. However, if the IDI bit is reset, then instead the WD33C92A sits in an idle state, waiting for the Target to reconnect. If a different Target device Reselects the 33C92A, a "terminated" interrupt is generated. However, if the original Target Reselects the 33C92A, no interrupt is generated and the COMMAND PHASE register is set to hex 44.

Following the original Target Reselection, the 33C92A expects a Message In phase which should consist of the Target sending an IDENTIFY Message. This single-byte message should be of the binary form: 10000ttt, where ttt is the Target LUN. If the data received by the 33C92A is different or the Target LUN specified in this byte does not match the contents of the TARGET LUN register, a "terminated" interrupt is generated and the Message byte may be examined by the processor. A correct IDENTIFY Message In phase results in the COMMAND PHASE register being updated to hex 45.

After the IDENTIFY Message is received from the Target or immediately after the Command Out phase (when there is no disconnection), a Data In phase, Data Out phase, or Status phase should occur. If the TRANSFER COUNT register contains any non-zero value, then the 33C92A will expect a Data Transfer phase. If Advanced Features are enabled, then the DPD bit will be examined to verify the correct data direction. If the data direction is incorrect, then a "terminated" interrupt is generated. In this phase, the 33C92A will use the TRANSFER COUNT register to determine the number of bytes to be transferred, and all host-side DATA register accesses will be accomplished via the method selected by the DMA mode select bits in the CONTROL register. When the internal counter reaches zero, the Data Transfer phase is complete and the COMMAND PHASE register is set to hex 46.

Any number of disconnection/reconnection cycles may occur during the Data Transfer phase so long as they are accomplished according to the defined message protocol. The COMMAND PHASE register will cycle through the disconnect phases (41-45) with each disconnection and subsequent reconnection until all of the data has been transferred and the Data Transfer phase is complete.

A Status phase is expected by the 33C92A following the Data Transfer phase (or instead of the Data Transfer phase when the TRANSFER

COUNT register contains a value of zero). At the start of the Status phase, the COMMAND PHASE register is loaded with hex 47. Upon completion of the Status phase, the COMMAND PHASE register will be updated to hex 50, and the received status byte is stored in the TARGET LUN register where it can be read upon completion of the command.

Following completion of the status-byte transfer, a Message In phase is expected. The 33C92A expects the Target to send a COMMAND COMPLETE Message (hex 00) to indicate that the SCSI command operation has been completed. After the 33C92A receives this COMMAND COMPLETE Message, the COMMAND PHASE register advances to hex 60, and if the EDI bit is reset, a "successful completion" interrupt is generated. The processor should then read the TARGET LUN register to examine the Target status. An additional interrupt will then occur when the SCSI bus goes to the Bus Free state, or when another REQ is asserted to begin an information transfer phase (as in SCSI linked commands). If the EDI bit is set, the "successful completion" interrupt will be suppressed until the Target disconnects from the SCSI bus.

At any time during execution of the Select-and-Transfer commands, an abnormal or unexpected condition will cause the 33C92A to terminate the command, set the appropriate status qualifiers, and generate a "terminated" interrupt. If the termination occurred during an information transfer phase, the 33C92A will be left in a Connected-as-an-Initiator state (unless termination was due to a sudden Target disconnection). Command termination during any other phase will result in the 33C92A being in a Disconnected state. Transfer commands may be used to handle the exception by transferring messages with the Target.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Select-and-Transfer commands, and their meanings relative to command termination:

COMMAND PHASE	MEANING
00	No SCSI bus device has been selected. The 33C92A is in the disconnected state.
10	The Target has been selected. The 33C92A is now in the connected as an Initiator state.
20	An Identify message has been sent to the Target.
30	Command phase has started, no bytes transferred.
3x	Command phase, x bytes have been transferred.
41	Save-Data-Pointer message received.
42	Disconnect message received, bus not free.
43	Target has disconnected (SCSI bus free) following a successful transfer of a Disconnect message. The 33C92A is now in the disconnected state.
44	The 33C92A has been reselected by the Target whose SCSI bus ID matches the value in the DESTINATION ID register. The 33C92A is now in the connected as an Initiator state.
45	The 33C92A has received an Identify message from the Target whose Logical Unit Number matches the value in the TARGET LUN register.
46	The number of bytes specified in the TRANSFER COUNT register have been transferred to/from the Target during a Data Out/In phase.
47	The Target has begun a Receive Status phase.
50	The 33C92A has successfully received a Status byte from the Target and stored it in the TARGET LUN register.
60	The 33C92A has successfully received a Command Complete message from the Target.

A "Resume Select-and-Transfer" command is assumed whenever a normal "Select-and-Transfer" command is issued while the 33C92A is in the Connected-As-An-Initiator state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Select-and-Transfer command execution. This feature, in conjunction with the INTERMEDIATE DISCONNECT INTERRUPT enabled, allows support of multi-threaded or overlapped I/O on the SCSI bus.

The following table briefly describes the valid settings of the COMMAND PHASE register when resuming a Select-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Target selection is complete.
20	Resume after Identify message out. Command phase is expected; an implied Negate ACK occurs.
30	Resume when Command phase has begun (REQ asserted).
41	Resume after Command phase or after Save-Data-Pointer message. Data, Status, or Message In phases are expected. An implied Negate ACK occurs.
42	Resume to complete Disconnect Message In; an implied Negate ACK occurs.
44	Resume after reselection by a Target.
45	Resume to transfer more data in a data transfer phase. May expect Status or Message In as well. An implied Negate ACK occurs.
46	Resume after the data has has been completed, expecting Status phase or a Save-Data-Pointer/Disconnect Message In phase. An implied Negate ACK does NOT occur.
50	Resume to complete a Status phase; an implied Negate ACK occurs.
60	Resume to complete a Command Complete message from the Target; an implied Negate ACK occurs.

7.6.2 Reselect-and-Transfer (0A and 0B hex)

The Reselect-and-Transfer commands include the Reselect-and-Receive-Data and the Reselect-and-Send-Data commands. These commands cause the 33C92A to execute certain common SCSI bus phase sequences as a Target following a Reselection phase. These phases are determined by which command is sent, and the setting of two bits: the EDI bit in the CONTROL register; and the SCC bit in the DESTINATION ID register. The SCSI bus phase sequences are summarized below.

Refer to the command descriptions of the Send-Status-and-Command-Complete and Send-Disconnect-Message commands for details on those sequences.

1. Reselect-and-Receive command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Completion interrupt.

2. Reselect-and-Send command, EDI=0, and SCC=don't care:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Completion interrupt.

3. Reselect-and-Receive command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Status-and-Command Complete;

4. Reselect-and-Send command, EDI=1, and SCC=0:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Status-and-Command-Complete;

5. Reselect-and-Receive command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Receive Data Out phase;
   - Chain to Send-Disconnect-Message;

6. Reselect-and-Send command, EDI=1, and SCC=1:

   - Reselection phase;
   - Send Identify Message In;
   - Send Data In phase;
   - Chain to Send-Disconnect-Message;

If the reselection attempt times out during a Reselect-and-Transfer command, ATN is asserted and HA=1, or if a parity error is detected on a incoming data byte (and HSP=1 or HHP=1, depending on data direction), the command will be terminated and the appropriate status will be set. In this case, the COMMAND

PHASE register should be evaluated to determine the last successfully completed phase. If none of these conditions occurs, all phases complete normally, and if EDI=0, then a "successful completion" interrupt would be generated at this point. However, if EDI=1, no interrupt is generated and command chain occurs (as described above).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Reselect-and-Transfer commands, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No SCSI bus device has been reselected. The 33C92A is in the disconnected state.
10	The 33C92A has successfully reselected the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully sent to the Initiator.
46	The requested data transfer has been completed.

A "Resume Reselect-and-Transfer" command is assumed whenever a normal "Reselect-and-Transfer" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Reselect-and-Transfer command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Reselect-and-Transfer command:

COMMAND PHASE	MEANING
10	Resume after Initiator reselection is complete; start with Identify Message Out.
20	Resume after Identify message out; start with data transfer phase. If TRANSFER COUNT is zero, no data transfer phase occurs. In either case, a chain to another combination command can occur if enabled.

7.6.3 Wait-for-Select-and-Receive (0C hex)

The Wait-for-Select-and-Receive causes the 33C92A to idle until it is selected by an Initiator, at which time the 33C92A will enter the Target mode and message and command information will automatically be requested. As an option, the 33C92A may be programmed to disconnect when a SCSI read command is received while executing a Wait-for-Select-and-Receive command. Use of this command therefore eliminates the interrupts which normally occur after selection and after each subsequent SCSI bus phase, and results in very short bus-connect time during SCSI read commands.

If ATN was asserted by the Initiator during the selection phase, the 33C92A will first execute an implied "Receive Message Out" command to get the Identify message from the Initiator, before continuing on with the implied "Receive Command" to receive the SCSI command information. The SCSI command information (CDB) will be stored in the CDB registers (hex addresses 03 to 0E), and if a valid IDENTIFY message is received, it will be saved in the TARGET LUN register (hex address 0F). The number of command bytes requested by the 33C92A is determined by the SCSI group code in the first byte of the CDB.

After the 33C92A is selected and receives all valid command and message information, a "successful completion" interrupt will normally be generated to allow the local processor to read out and interpret the SCSI CDB. However, by setting the EDI bit prior to issuing a Wait-for-Select-and-Receive command, the 33C92A is enabled to perform an automatic disconnect when a SCSI read command is received. Therefore, when EDI=1 and the 1st CDB byte received contains a 6-, 10-, or 12-byte read command code, then the 33C92A will temporarily suppress the interrupt and chain to begin execution of a Send-Disconnect-Message command. An interrupt will then be generated after completion of this command, which normally would indicate a transition to the bus free condition. Refer to the Send-Disconnect-Message command description for more details.

If during execution the message or command information received from the Initiator is invalid, the implied receive command will be terminated and the appropriate status reported. In this case, the COMMAND PHASE register should be read to determine which phase of the Wait-for-Select-and-Receive command was last completed before the error condition occurred. A COMMAND PHASE hex value of hex 10 indicates that the 33C92A was successfully selected. A hex value of 20 indicates that a message was received from the Initiator, and when the 33C92A begins receiving command bytes, the COMMAND PHASE is set to hex 30 and increments with each byte received (to a maximum of 3C for a 12-byte CDB command).

The following table summarizes the possible values that the COMMAND PHASE register can take during the Wait-for-Select-and-Receive command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	The 33C92A has not been selected. The 33C92A is in the disconnected state.
10	The 33C92A has been successfully selected by the Initiator. The 33C92A is now in the connected as a Target state.
20	The Identify message has been successfully received from the Initiator.
30	The 33C92A has begun command phase by setting the SCSI bus phase signals and asserting REQ.
31	The 33C92A has transferred 1 command byte from the Initiator. The SCSI STATUS may indicate the need for the host to load the command size into the OWN ID register.
3x	The 33C92A has transferred x command bytes from the Initiator.

A "Resume Wait-for-Select-and-Receive" command is assumed whenever a normal "Wait-for-Select-and-Receive" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Wait-for-Select-and-Receive command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Wait-for-Select-and-Receive command:

COMMAND PHASE	MEANING
10	Resume after selection by the Initiator is complete; start with Identify Message Out if ATN is asserted, otherwise, start with command phase.
20	Resume after a message out; check the received message in the TARGET LUN register for a valid Identify message.
30	Resume after Identify message out. Start with command phase.
31	Resume after the 33C92A has transferred 1 command byte from the Initiator. This resume point is used only when an unknown group code has been detected in Advanced Mode, and the command size has been loaded into the OWN ID register.

7.6.4 Send-Status-and-Command-Complete (0D hex)

The Send-Status-and-Command-Complete command is valid in the Target role, and is used to complete a SCSI operation by transferring the appropriate status information to the Initiator prior to disconnection from the SCSI bus. This command also supports linked SCSI operations by optionally allowing a linked command-complete message to be sent after the status is transferred. Linked command complete messages are controlled by the CDB12 register with bits that correspond to the standard linked command control bits in the CDB.

Before a Send-Status-and-Command-Complete command is issued, the CDB11 register must be loaded with a status byte which will then be transferred across the SCSI bus. Also, the link control bits from the current CDB must be loaded into the CDB12 register to ensure that the correct sequence occurs.

The bits used by the 33C92A are identical in meaning to the SCSI standard link control bits. The host processor may simply load the control byte from the current SCSI command into CDB12 to get the correct function. As the command execution progresses, the COMMAND PHASE register will be updated to indicate the last phase completed.

The possible sequences caused by this command are as follows:

1. CDB12 bit0=0, bit1=don't care: The status byte in CDB11 is sent, followed by a Command Complete message (00 hex). A "successful completion" interrupt now occurs.

2. CDB12 bit0=1, bit1=0: The status byte in CDB11 is sent, followed by a Linked Command Complete message (0A hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

3. CDB12 bit0=1, bit1=1: The status byte in CDB11 is sent, followed by a Linked Command Complete with Flag message (0B hex). A chain to the command fetch portion of Wait-for-Select-and-Receive then occurs to fetch the next CDB from the Initiator. 33C92A command execution proceeds as described for that command.

A Send-Status-and-Command-Complete command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Status-and-Command-Complete command, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
50	Status phase transfer completed.
60	Command Complete message transfer completed.
61	Linked Command Complete message transfer completed.

A "Resume Send-Status-and-Command-Complete" command is assumed whenever a normal "Send-Status-and-Command-Complete" command is issued while the 33C92A is in the Connected-as-a-Target state. When the "Resume" is issued, the 33C92A examines the COMMAND PHASE register to determine where to restart the Send-Status-and-Command-Complete command execution. This feature, in conjunction with the capability to chain to other combination commands, allows longer SCSI bus sequences to be executed by a single command.

The following table briefly describes the meaning of the COMMAND PHASE register when resuming a Send-Status-and-Command-Complete command:

COMMAND PHASE	MEANING
50	Resume after status phase. Start with command complete message. May chain to command fetch if commanded to do so.

7.6.5 Send-Disconnect-Message (0E hex)

The Send-Disconnect-Message command is a Target-role command which may be used to disconnect from the SCSI bus at any time during a SCSI command sequence. This command consists of sending a Disconnect message byte, followed by physical disconnection from the bus (SCSI bus free). An interrupt is generated only after transition to bus free occurs. As an option, a Save-Data-Pointer message will automatically be sent before the Disconnect message whenever the IDI bit is set prior to issuing this command.

The COMMAND PHASE register is updated during execution of the Send-Disconnect-Message command to indicate bus phase status. After a Save-Data-Pointer message is sent, the COMMAND PHASE will be set to 41H. After the Disconnect message transfer, this register will be updated to 42H, and after disconnection the COMMAND PHASE register will contain a 43H.

A Send-Disconnect-Message command may be terminated by ATN asserted when HA=1, or when a Disconnect or Reset command is issued.

The following table summarizes the possible values that the COMMAND PHASE register can take during the Send-Disconnect-Message, and their meanings relative to command termination. See other command descriptions for additional values that can occur when command chaining is used.

COMMAND PHASE	MEANING
00	No operation occurred; typically, ATN was found to be asserted.
41	The Save-Data-Pointer message was transferred.
42	The Disconnect message was transferred.
43	The bus free state occurred after the Disconnect message was transferred. The 33C92A is now in the disconnected state.

8.0 DC ELECTRICAL SPECIFICATIONS

8.1 MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-55° C to 125° C
Voltage on any pin with respect to GND	-0.5 to 7 Volts
Power dissipation	190 mW
Input Static Discharge Protection	2000 V pin to pin

NOTE

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

8.2 STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to V_{SS} (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70° C
V_{CC}	+5 Volts ± 0.25 V
V_{SS}	0 Volts

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8.3 DC OPERATING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS	CONDITIONS
I_{IL}	Input Leakage	---	10	µA	V_{IN} = .4 to VCC
I_{OL}	Output Leakage (inactive)	---	50	µA	V_{OUT} = .4 to VCC
V_{IH}	Input High Voltage	2.0	---	V	
V_{IL}	Input Low Voltage	---	0.8	V	
V_{OH}	Output High Voltage	2.4	---	V	I_O = -400 µA
V_{OL1}	Output Low Voltage (TGS, IGS)	---	0.4	V	I_O = 7.0 mA
V_{OL2}	Output Low Voltage (all others)	---	0.4	V	I_O = 4.0 mA
I_{CC}	Supply Current	---	36	mA	T_A = +25°C

9.0 AC OPERATING CHARACTERISTICS

Timing characteristics are valid over the entire operating temperature (0 to 70 deg. C) and voltage (4.75 to 5.25 Volts) ranges. All pins are referenced to and from a low voltage of 0.8 volts and a high voltage of 2.0 volts, except for SCSI bus pins, which are referenced to 1.5 volts. All outputs are assumed to have a load capacitance of 50 picofarads.

Many of the timing parameters that follow are defined in terms of an internal clock cycle time that is determined by the input clock and the clock divisor selected in the OWN ID register. This cycle time is calculated as follows:

Tcyc =Tcp * DIVISOR/ 2

where:

Tcyc is the internal clock cycle time;
Tcp is the period of the clock at the CLK input;
DIVISOR is the clock divisor selected in the OWN ID register.

For example, with a 16MHz clock input to the 33C92A, the clock divisor selected would be 4. Therefore, the value of Tcyc would be:

Tcyc = 62.5 nsec * 4/ 2 = 125 nsec

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9.1 PROCESSOR/DMA INTERFACE

9.1.1 CLK

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tcp	CLOCK PERIOD	50	125	ns
tch	CLOCK HIGH	20		ns
tcl	CLOCK LOW	20		ns

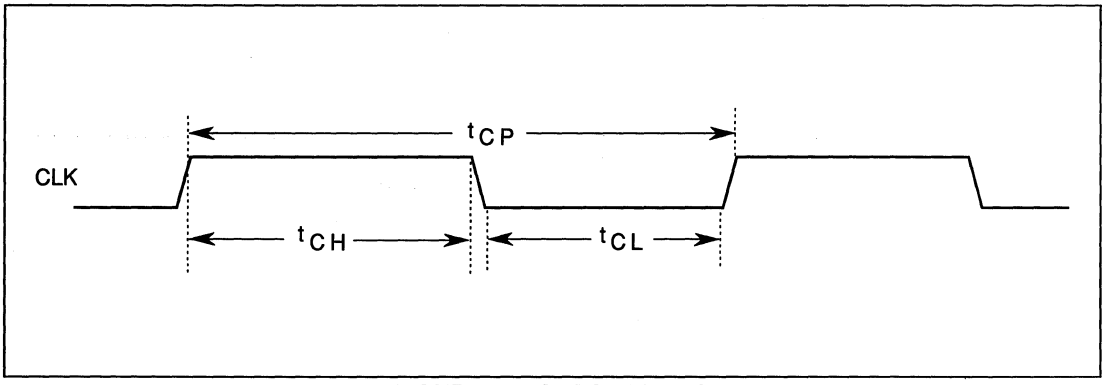

FIGURE 9-1. CLOCK TIMING

9.1.2 MR-

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tmr	MR- PULSE WIDTH	1		µs

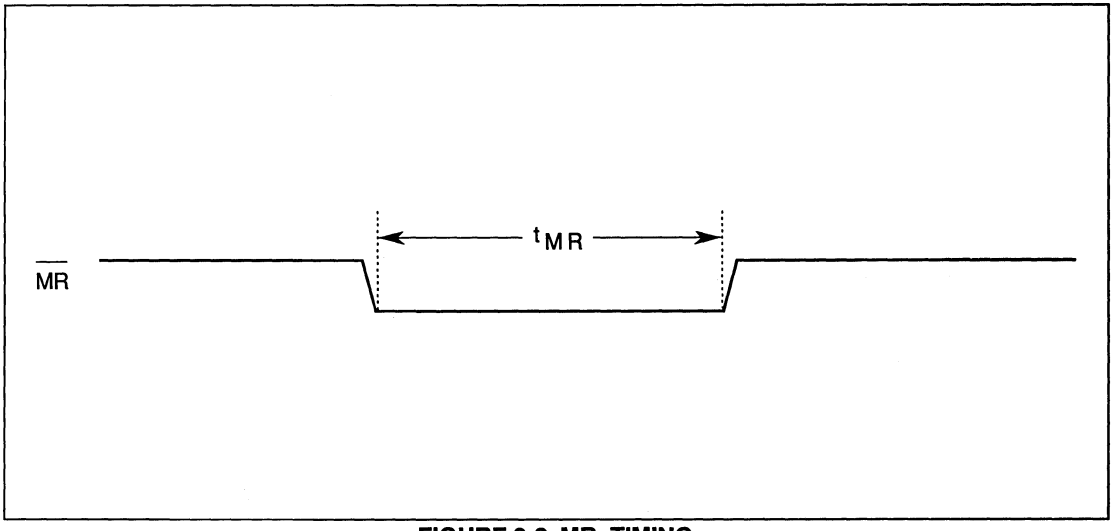

FIGURE 9-2. MR- TIMING

9.1.3 Processor Write (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavwl	A0 VALID TO WE- LOW	0		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhai	WE- HIGH TO A0 INVALID	0		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns

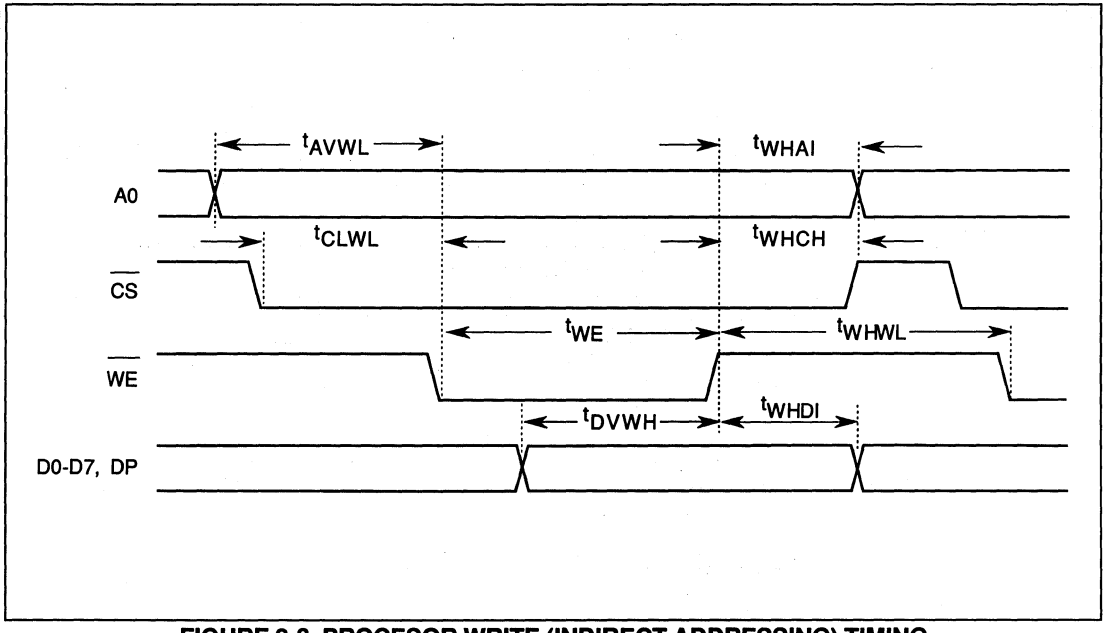

FIGURE 9-3. PROCESOR WRITE (INDIRECT ADDRESSING) TIMING

9.1.4 Processor Read (Indirect Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tavrl	A0 VALID TO RE- LOW	0		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID	---	180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
trhai	RE- HIGH TO A0 INVALID	0		ns

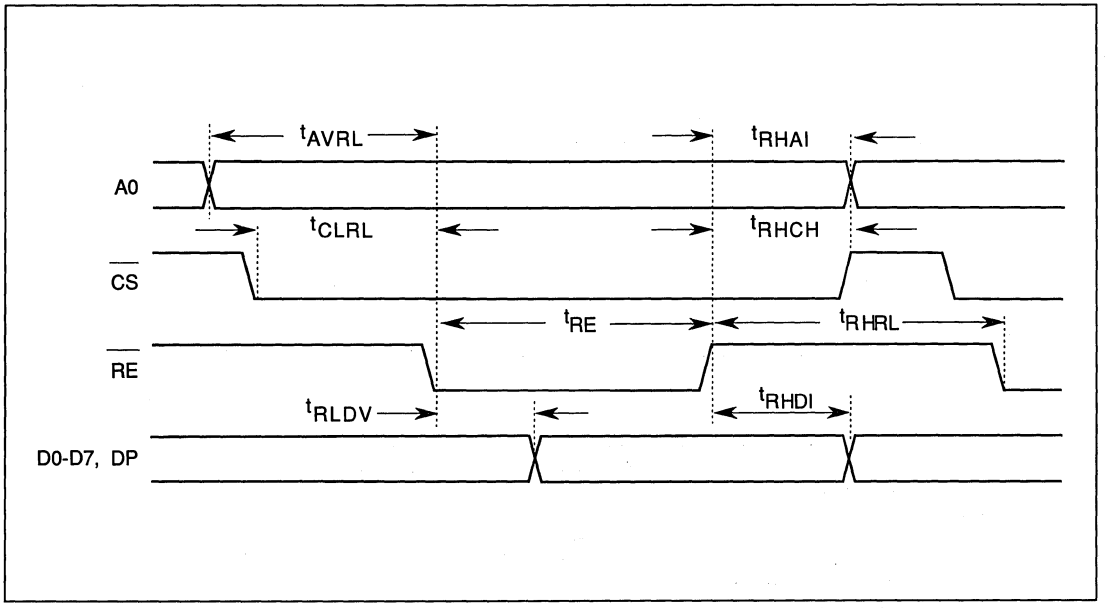

FIGURE 9-4. PROCESSOR READ (INDIRECT ADDRESSING) TIMING

9.1.5 Processor Write (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talwl	ALE LOW TO WE- LOW	90		ns
tclwl	CS- LOW TO WE- LOW	0		ns
twe	WE- PULSE WIDTH	120		ns
tdvwh	DATA VALID TO WE- HIGH	70		ns
twhch	WE- HIGH TO CS- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
twhwl	WE- HIGH TO WE- OR RE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW	---	1	µs

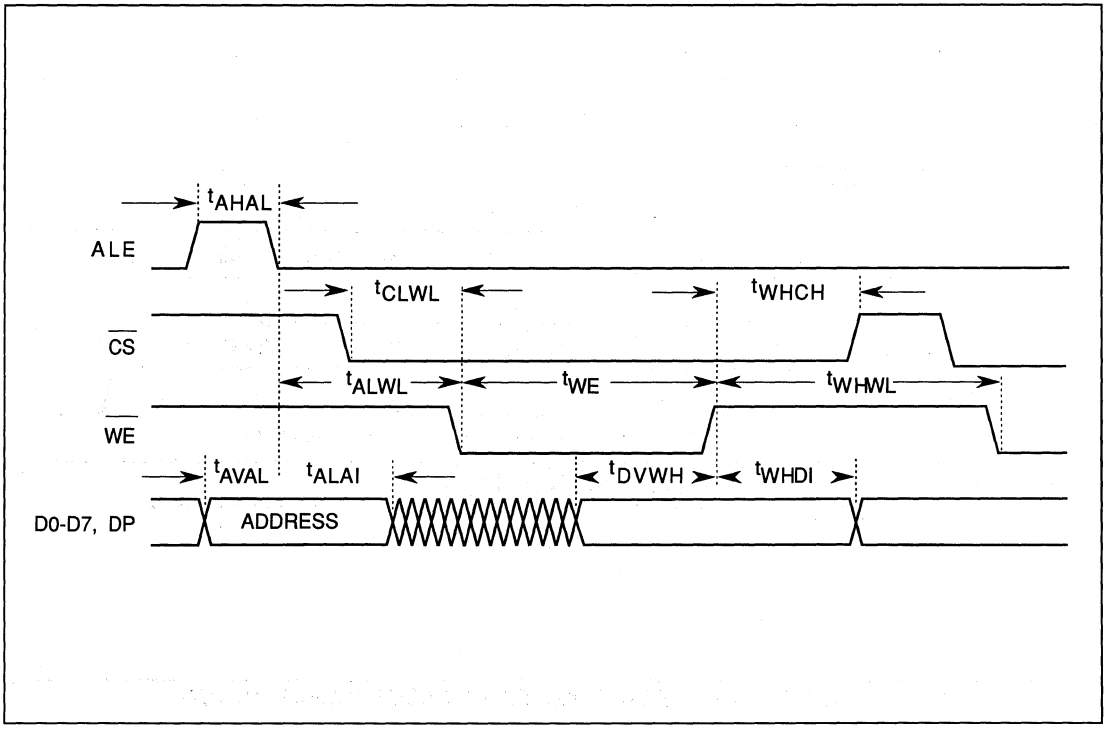

FIGURE 9-5. PROCESSOR WRITE (DIRECT ADDRESSING) TIMING

9.1.6 Processor Read (Direct Addressing)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
taval	ADDR VALID TO ALE LOW	40		ns
talai	ALE LOW TO ADDR INVALID	0		ns
talrl	ALE LOW TO RE- LOW	30		ns
tclrl	CS- LOW TO RE- LOW	0		ns
tre	RE- PULSE WIDTH	180	10000	ns
trldv	RE- LOW TO DATA VALID		180	ns
trhch	RE- HIGH TO CS- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
trhrl	RE- HIGH TO RE- OR WE- LOW	100		ns
tahal	ALE HIGH TO ALE LOW		1	µs

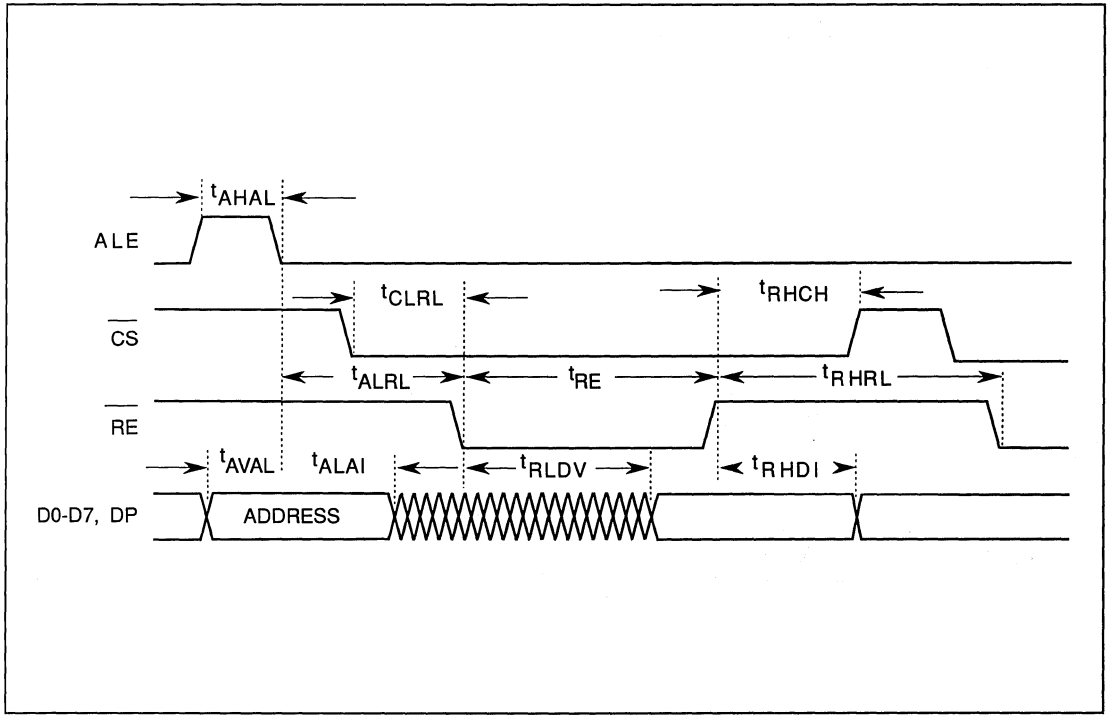

FIGURE 9-6. PROCESSOR READ (DIRECT ADDRESSING) TIMING

9.1.7 DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	100		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

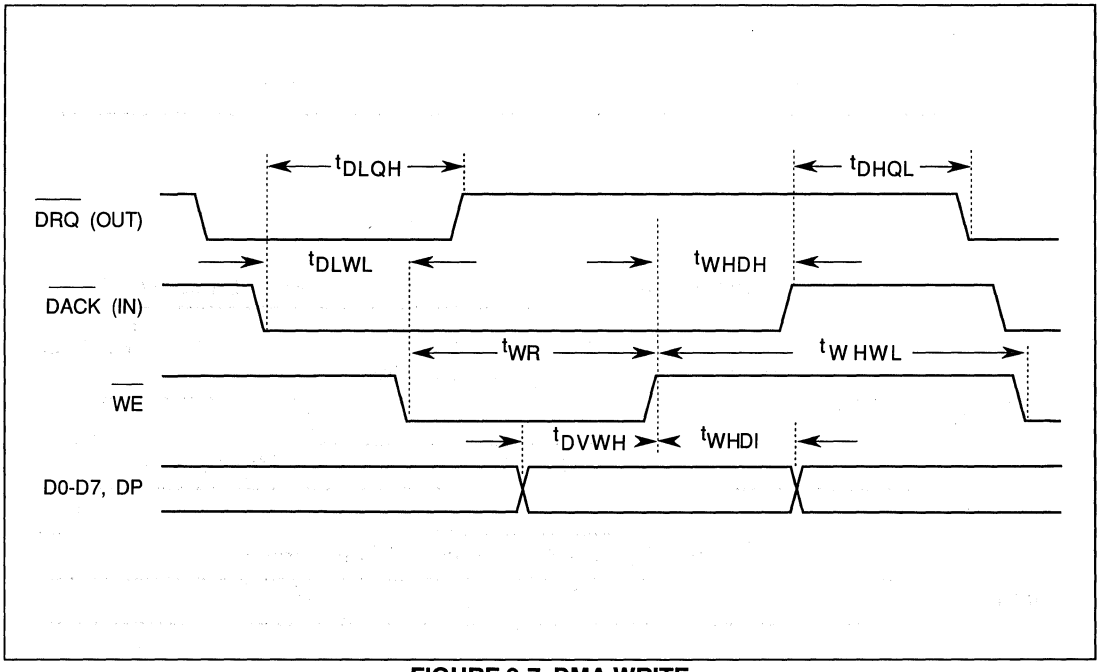

FIGURE 9-7. DMA WRITE

9.1.8 DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
tdlqh	DACK- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	100		ns
trldv	RE- LOW TO DATA VALID		70	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tdhql	DACK- HIGH TO DRQ- LOW	0		ns

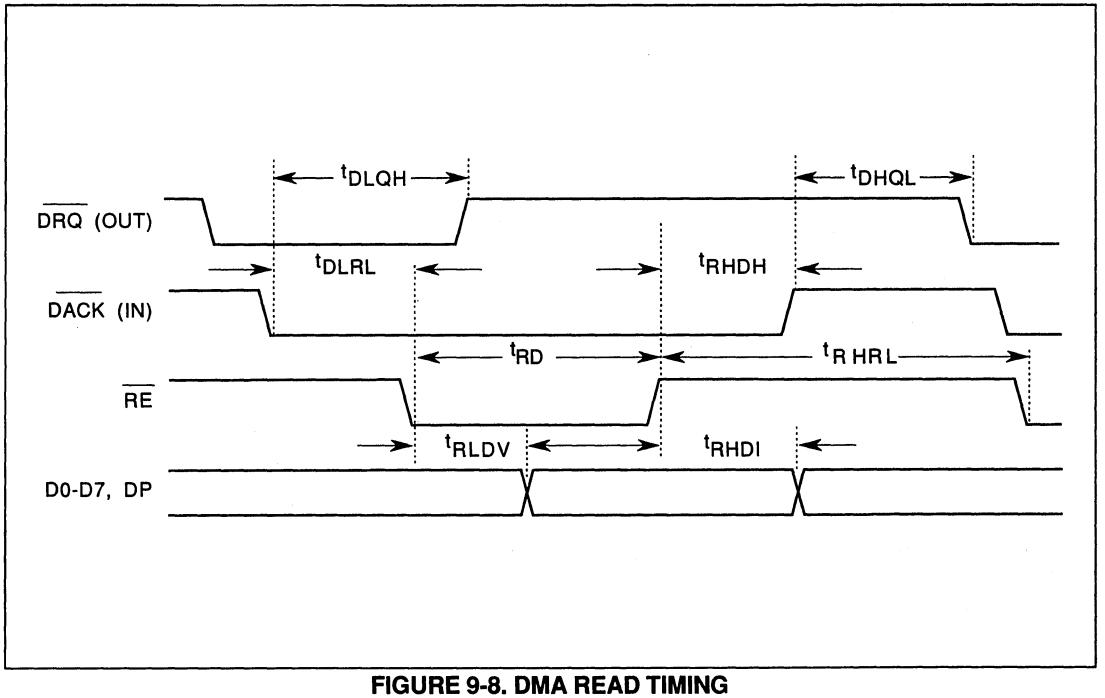

FIGURE 9-8. DMA READ TIMING

9.1.9 Bus Buffer Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslwv	RCS- LOW TO WE- VALID	-5	20	ns
two	WE- PULSE WIDTH	1-20ns		Tcyc
twldv	WE- LOW TO DATA VALID		50	ns
twhdi	WE- HIGH TO DATA INVALID	10		ns
twhwl	WE- HIGH TO WE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshwi	RCS- HIGH TO WE- INVALID		100	ns
twhsh	WE- HIGH TO RCS- HIGH	0		ns
tslwl	RCS- LOW TO WE- LOW	60		ns
tqlwl	DRQ LOW TO WE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

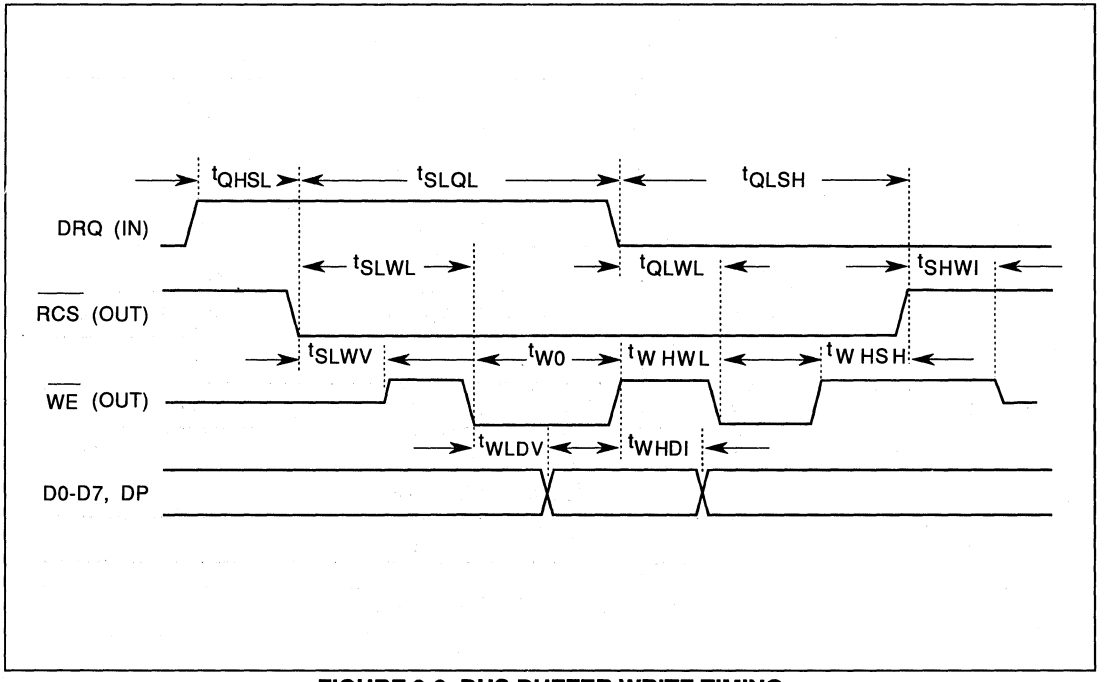

FIGURE 9-9. BUS BUFFER WRITE TIMING

9.1.10 Bus Buffer Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tqhsl	DRQ HIGH TO RCS- LOW	0	40	ns
tslrv	RCS- LOW TO RE- VALID	-5	20	ns
tro	RE- PULSE WIDTH	1-20ns		Tcyc
tdvrh	DATA VALID TO RE- HIGH	20		ns
trhdi	RE- HIGH TO DATA INVALID	0		ns
trhrl	RE- HIGH TO RE- LOW	1-20ns		Tcyc
tqlsh	DRQ LOW TO RCS- HIGH	8	10	Tcyc
tshri	RCS- HIGH TO RE- INVALID		100	ns
trhsh	RE- HIGH TO RCS- HIGH	0		ns
tslrl	RCS- LOW TO RE- LOW	60		ns
tqlrl	DRQ LOW TO RE- LOW (1)	0		ns
tslql	RCS- LOW TO DRQ LOW (2)		100	ns

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(1) Guarantees that only one more byte will be transferred.

(2) Guarantees that only one byte will be transferred.

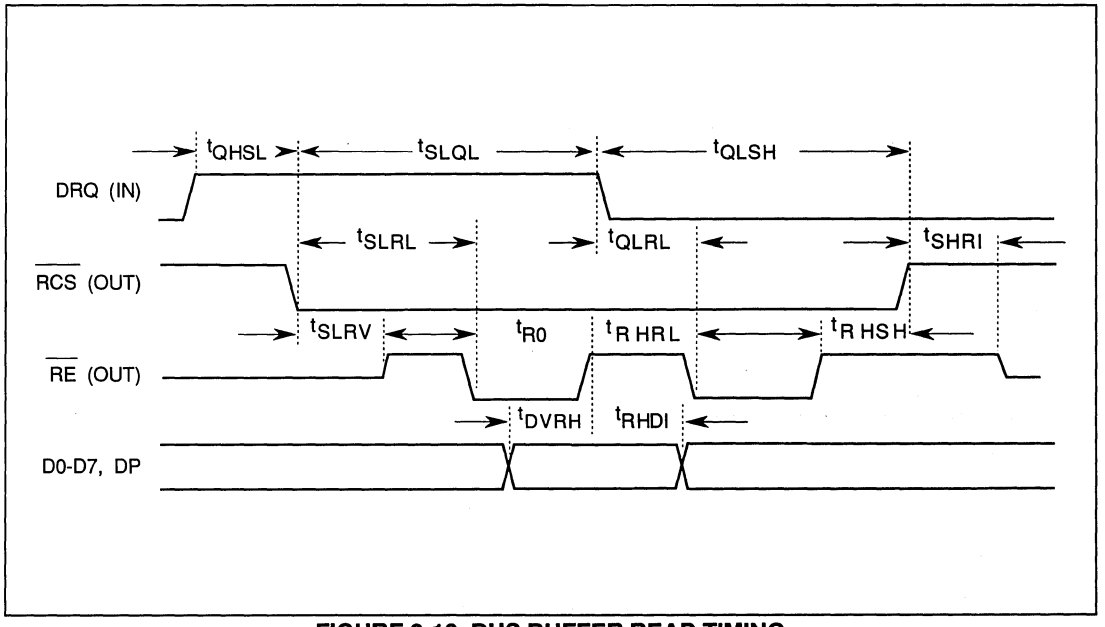

FIGURE 9-10. BUS BUFFER READ TIMING

9.1.11 Burst DMA Write

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlwl	DACK- LOW TO WE- LOW	0		ns
twlqh	WE- LOW TO DRQ- HIGH		75	ns
twr	WE- PULSE WIDTH	50		ns
twhwl	WE- HIGH TO WE- LOW	80		ns
tdvwh	DATA VALID TO WE- HIGH	25		ns
twhdh	WE- HIGH TO DACK- HIGH	0		ns
twhdi	WE- HIGH TO DATA INVALID	0		ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

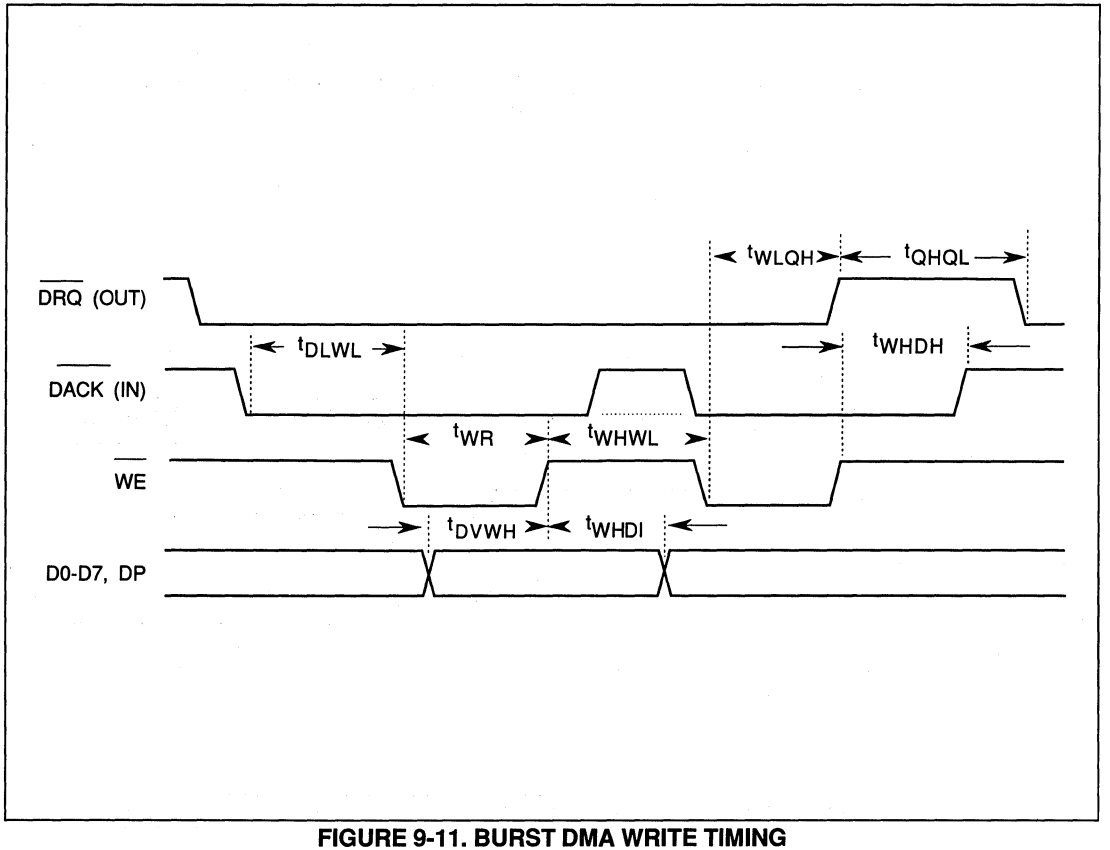

FIGURE 9-11. BURST DMA WRITE TIMING

9.1.12 Burst DMA Read

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdlrl	DACK- LOW TO RE- LOW	0		ns
trlqh	RE- LOW TO DRQ- HIGH		75	ns
trd	RE- PULSE WIDTH	80		ns
trhrl	RE- HIGH TO RE- LOW	80		ns
trldv	RE- LOW TO DATA VALID		50	ns
trhdh	RE- HIGH TO DACK- HIGH	0		ns
trhdi	RE- HIGH TO DATA INVALID	5	40	ns
tqhql	DRQ- HIGH TO DRQ- LOW	0.5		Tcyc

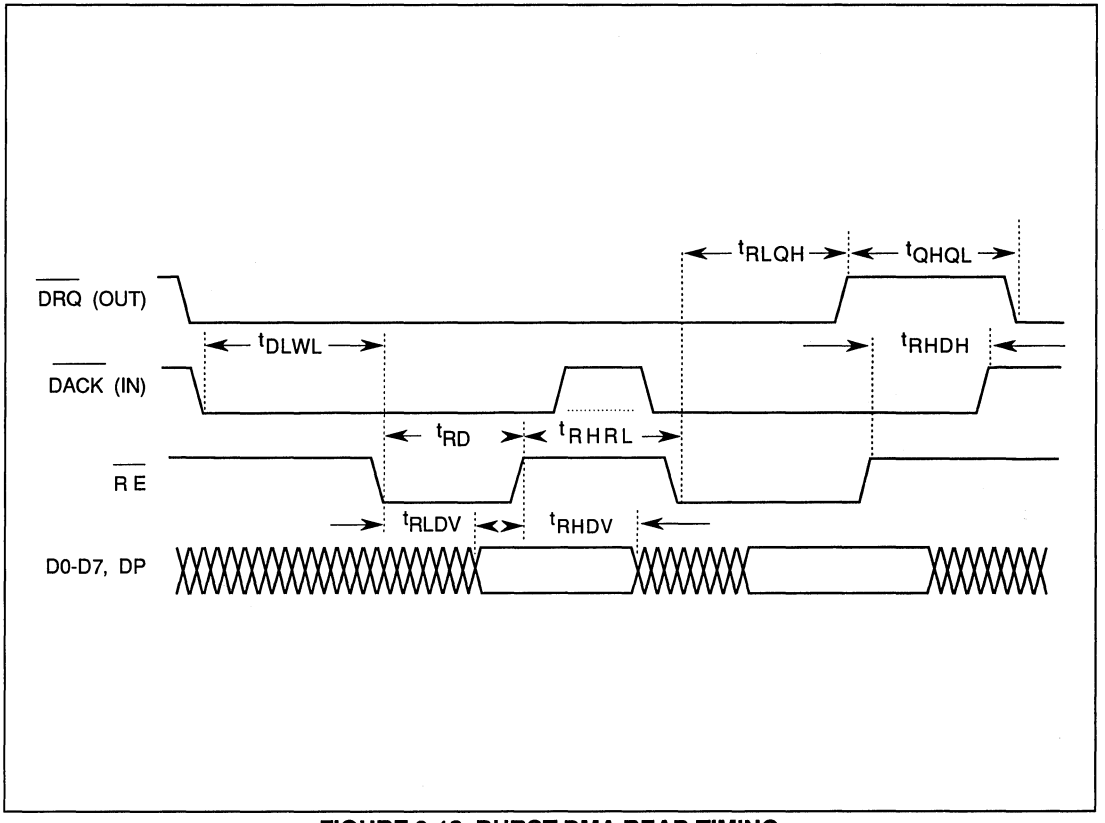

FIGURE 9-12. BURST DMA READ TIMING

9.1.13 INTRQ

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tihrl	INTRQ HIGH TO RE- LOW	0		ns
tri	RE- PULSE WIDTH	180		ns
trhil	RE- HIGH TO INTRQ LOW	0	100	ns
tilih	INTRQ LOW TO INTRQ HIGH	100		ns

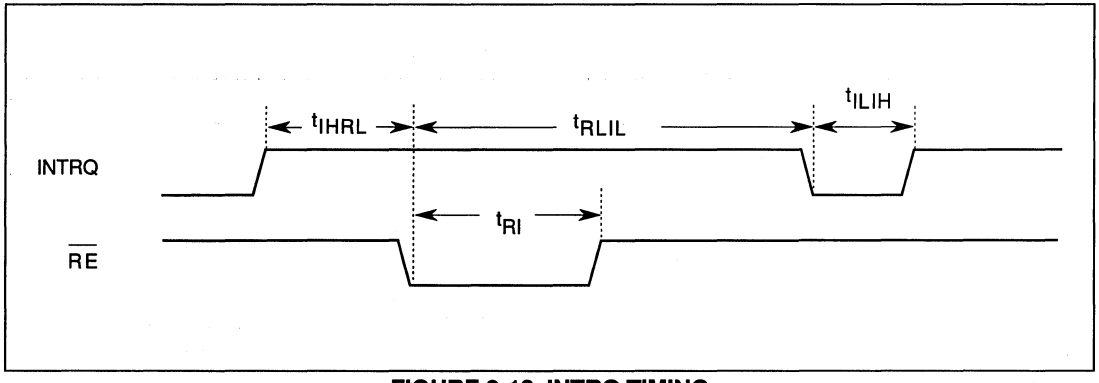

FIGURE 9-13. INTRQ TIMING

9.2 SCSI INTERFACE

9.2.1 Arbitration

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblel	BSYI, SELI LOW TO SDIE LOW	4		Tcyc
telio	SDIE LOW TO BUS ID OUT	1		Tcyc
tioah	BUS ID OUT TO ARBLD HIGH	1		Tcyc
tahdf	ARBLD HIGH TO DATA FLOAT	1		Tcyc
tdfeh	DATA FLOAT TO SDIE, SDOE HIGH	1		Tcyc
tblbh	BSYI, SELI LOW TO BSYO HIGH	12	17	Tcyc
tbheh	BSYO HIGH TO SDIE, SDOE HIGH	0	200	ns
tbhsh	BSYO HIGH TO SELO HIGH	2.2		µs

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NOTE:
I/O* = I/O, C/D, MSG, REQ; ATN* = ATN, ACK

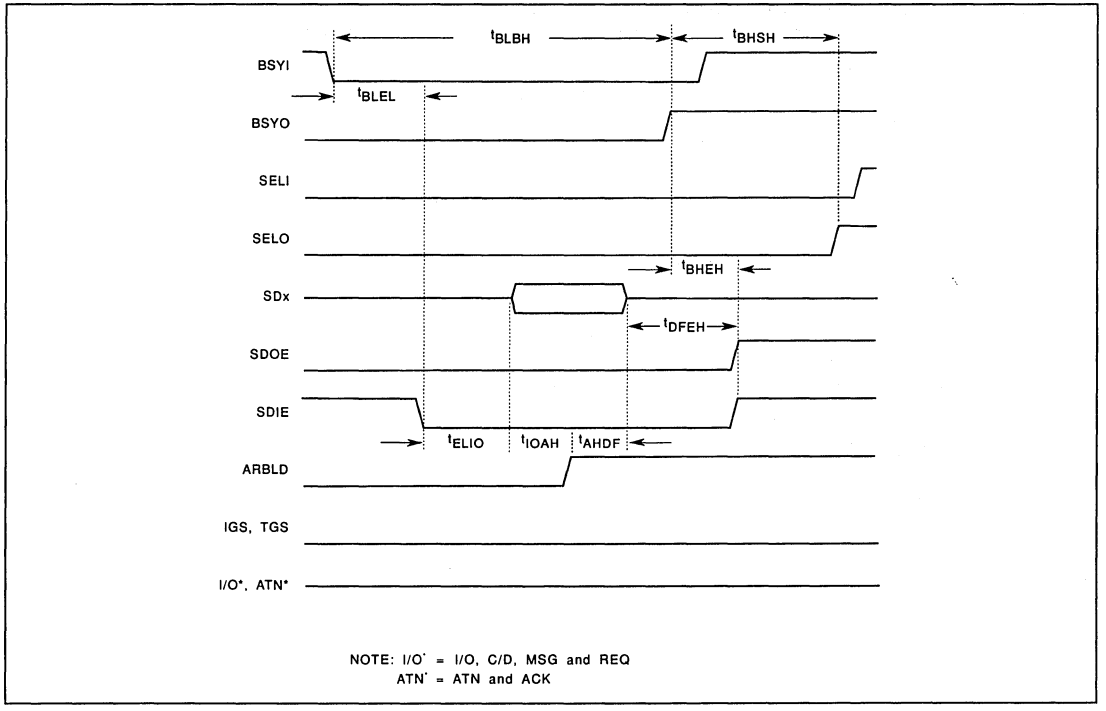

FIGURE 9-14. ARBITRATION TIMING

9.2.2 Selection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO IGS HIGH	100		ns
taogh	ATN, ACK OUT TO IGS HIGH	100		ns
tghav	IGS HIGH TO ATN VALID	400		ns
tavbl	ATN, ACK VALID OUT TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSY HIGH VALID	400		ns
tbhsl	BSYI HIGH TO SELO LOW	100		ns

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDIE* = SDIE, ARBLD

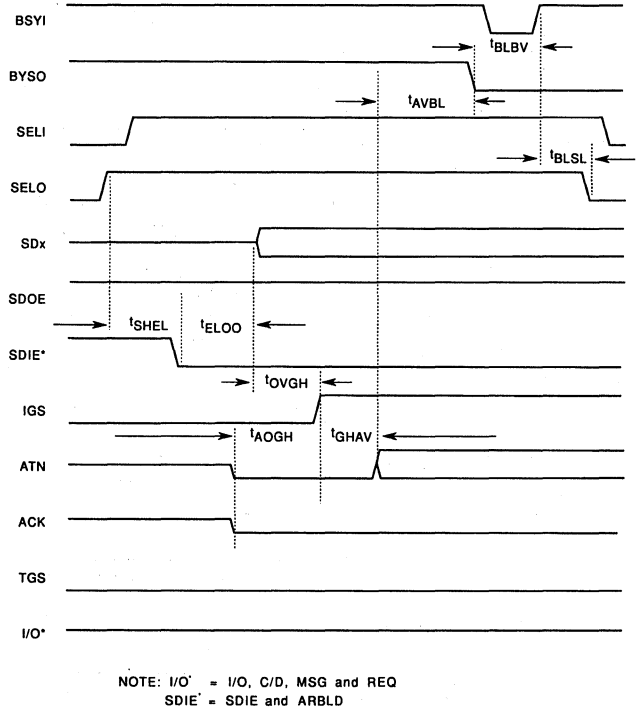

FIGURE 9-15. SELECTION (INITIATOR) TIMING

9.2.3 Selection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tblbh	SELI HIGH, ID VALID, BSYI LOW TO BSYO HIGH	0.4	200	µs
tbhoi	BSYO HIGH TO "OR-ED" ID INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tavsl	ATN VALID IN TO SELI LOW	0		ns
tslio	SELI LOW TO I/O OUT	100		ns
tivgh	I/O OUT VALID TO TGS HIGH	100		ns

22

NOTE:
I/O* = I/O, C/D, MSG, REQ; SDOE* = SDOE, ARBLD

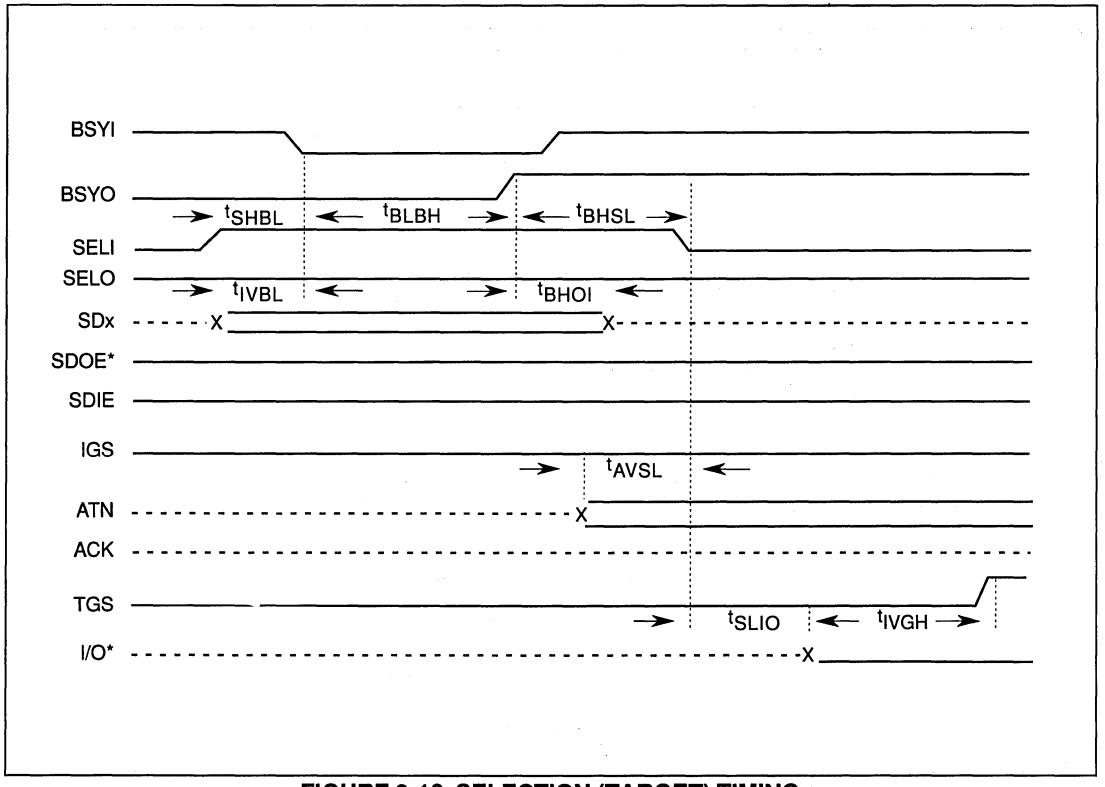

FIGURE 9-16. SELECTION (TARGET) TIMING

9.2.4 Reselection (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshel	SELO HIGH TO SDIE LOW	1.2		µs
teloo	SDIE LOW TO "OR-ED" ID OUT	100		ns
tovgh	"OR-ED" ID OUT VALID TO IGS HIGH	100		ns
taogh	ATN, ACK OUT TO IGS HIGH	100		ns
tghav	IGS HIGH TO ATN VALID	400		ns
tavbl	ATN, ACK VALID OUT TO BSYO LOW	100		ns
tblbv	BSYO LOW TO BSY HIGH VALID	400		ns
tbhsl	BSYI HIGH TO SELO LOW	100		ns

NOTE:
C/D* = C/D, MSG, REQ; ATN* = ATN, ACK; SDIE* = SDIE, ARBLD

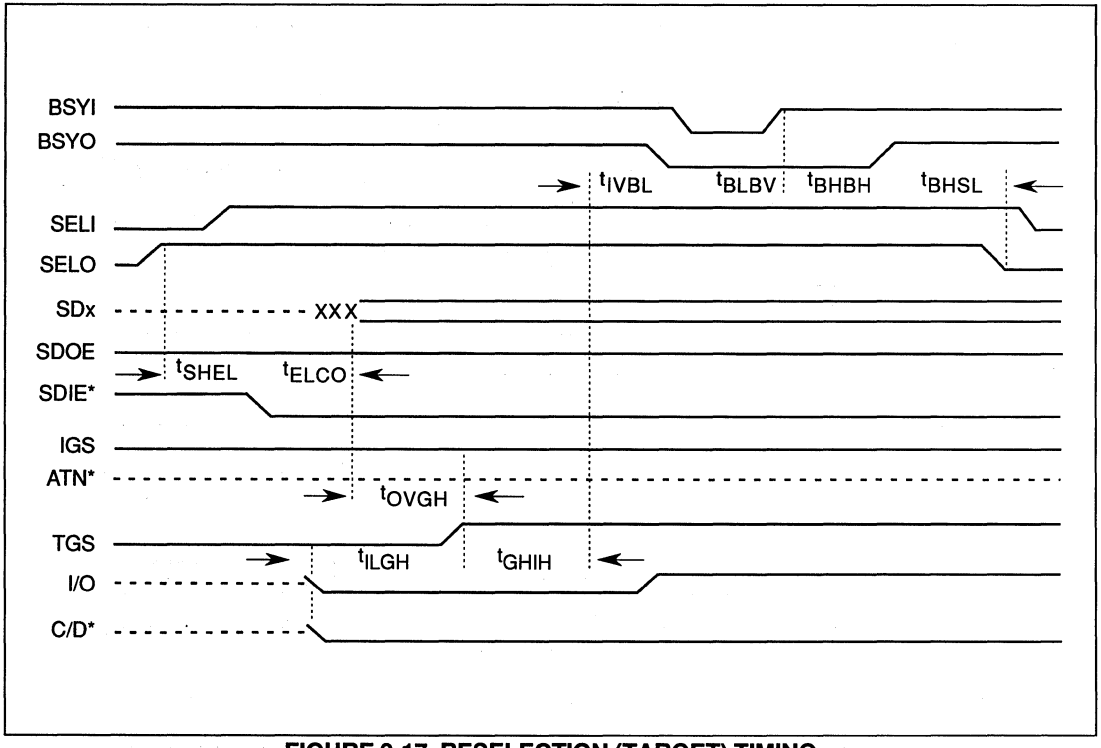

FIGURE 9-17. RESELECTION (TARGET) TIMING

9.2.5 Reselection (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYI LOW	0		ns
tivbl	"OR-ED" ID VALID IN TO BSYI LOW	0		ns
tihbl	I/O IN HIGH TO BSYI LOW	0		ns
tblal	SELI HIGH, ID VALID, BSYI LOW TO ATN LOW	0		ns
tghao	IGS HIGH TO ATN OUT	100		ns
talgh	ATN LOW TO IGS HIGH	400		ns
tihbh	IGS HIGH TO BSYO HIGH	100		ns
tblbh	BSYI LOW TO BSYO HIGH	0.4	200	ns
tbhoi	BSYO HIGH TO "OR-ED" INVALID IN	0		ns
tbhsl	BSYO HIGH TO SELI LOW	0		ns
tslbl	SELI LOW TO BSYO LOW	0		ns

22

NOTE:
ATN* = ATN, ACK; SDOE* = SDOE, ARBLD, SELO; C/D* = C/D, MSG, REQ

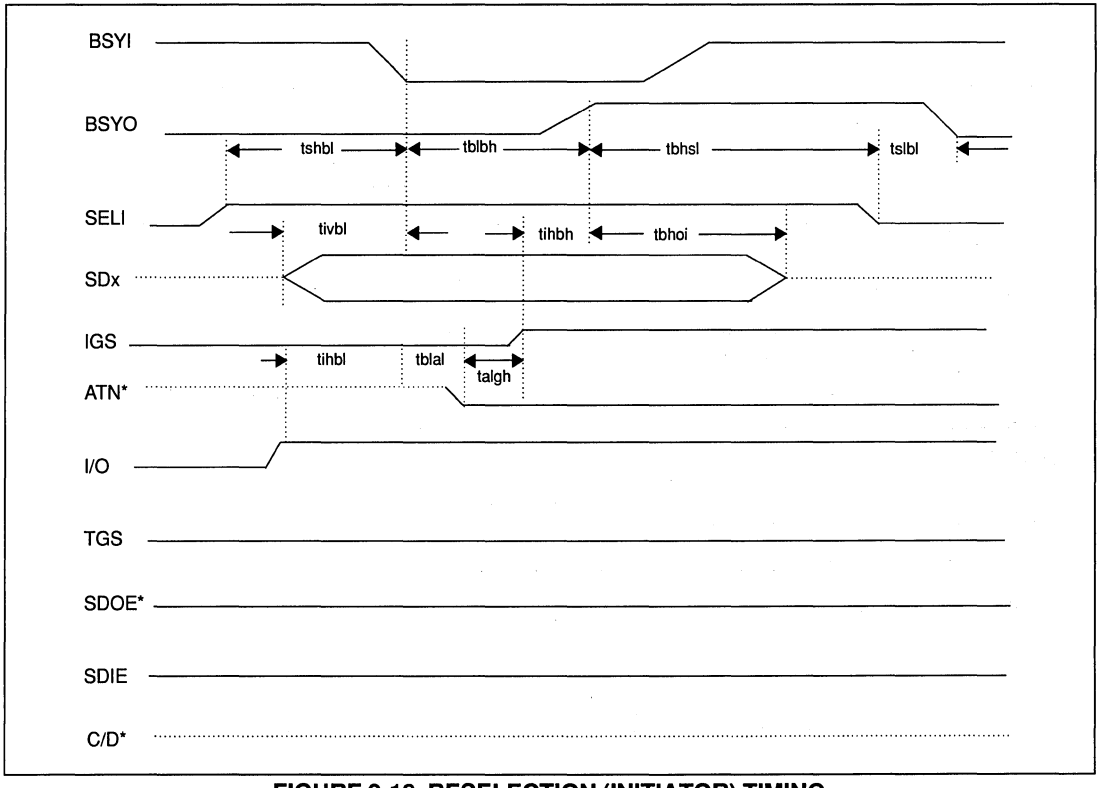

FIGURE 9-18. RESELECTION (INITIATOR) TIMING

9.2.6 Asynchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tihol	I/O IN HIGH TO SDOE LOW, DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
tahdi	ACK OUT HIGH TO DATA INVALID IN	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

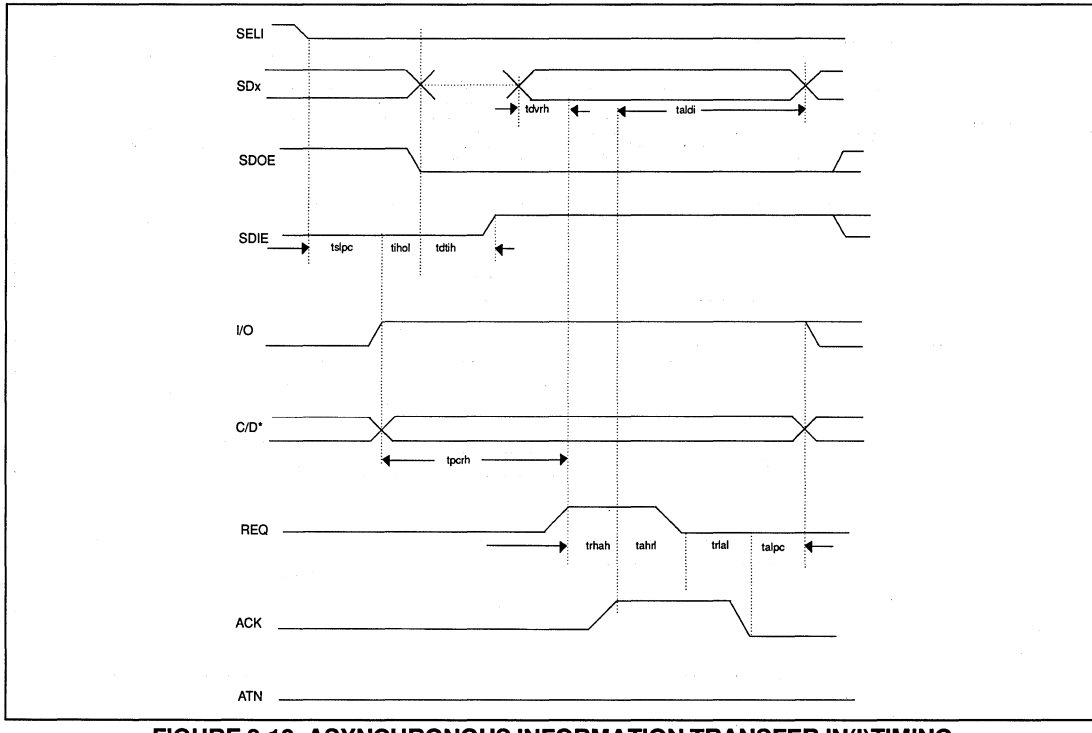

FIGURE 9-19. ASYNCHRONOUS INFORMATION TRANSFER IN(I)TIMING

9.2.7 Asynchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tihil	I/O OUT HIGH TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tdvrh	DATA OUT VALID TO REQ OUT HIGH	80		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
tahdi	ACK IN HIGH TO DATA OUT INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	100		ns

22

NOTE: C/D* = C/D, MSG

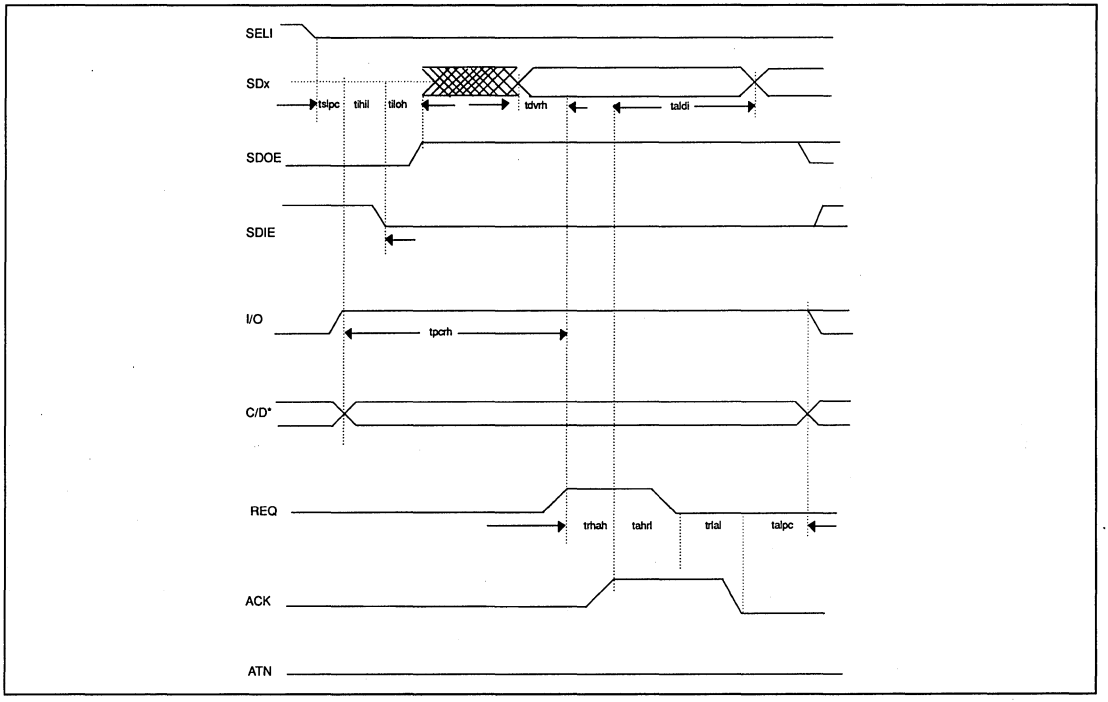

FIGURE 9-20. ASYNCHRONOUS INFORMATION TRANSFER IN(T)TIMING

9.2.8 Asynchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE IN	0		ns
tilil	I/O IN LOW TO SDIE LOW	0		ns
tiloh	SDIE LOW TO SDOE HIGH, DATA OUT	30		ns
tpcrh	PHASE CHANGE IN TO REQ IN HIGH	350		ns
trhah	REQ IN HIGH TO ACK OUT HIGH	0	175	ns
tdvah	DATA OUT VALID TO ACK OUT HIGH	80		ns
tahrl	ACK OUT HIGH TO REQ IN LOW	0		ns
trlal	REQ IN LOW TO ACK OUT LOW	0	175	ns
trldi	REQ IN LOW TO DATA OUT INVALID	0		ns
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

NOTE:
C/D* = C/D, MSG

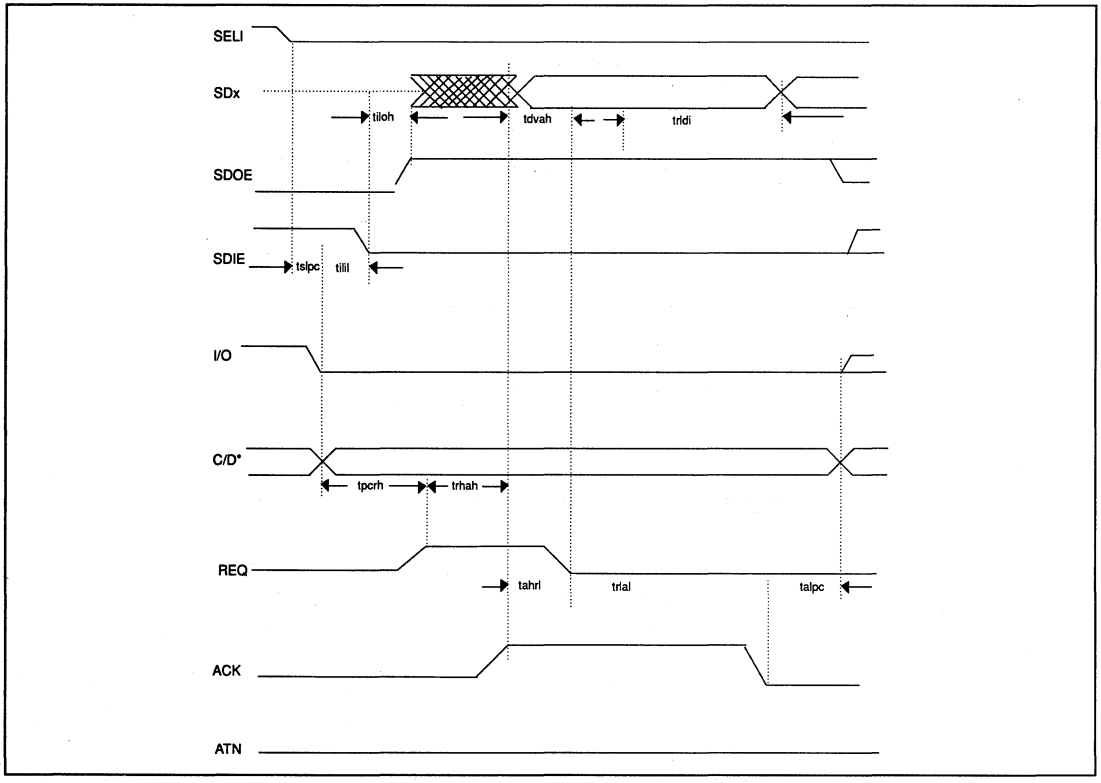

FIGURE 9-21.ASYNCHRONOUS INFORMATION TRANSFER OUT(I)TIMING

9.2.9 Asynchonous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tslpc	SELI LOW TO PHASE CHANGE OUT	100		ns
tilol	I/O OUT LOW TO SDOE LOW DATA BUS TRISTATE	0	125	ns
tdtih	DATA BUS TRISTATE TO SDIE HIGH	-10		ns
tpcrh	PHASE CHANGE OUT TO REQ OUT HIGH	500		ns
trhah	REQ OUT HIGH TO ACK IN HIGH	0		ns
tdvah	DATA IN VALID TO ACK IN HIGH	0		ns
tahrl	ACK IN HIGH TO REQ OUT LOW	0	175	ns
trldi	REQ OUT LOW TO DATA IN INVALID	0		ns
trlal	REQ OUT LOW TO ACK IN LOW	0		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

22

NOTE:
C/D* = C/D, MSG

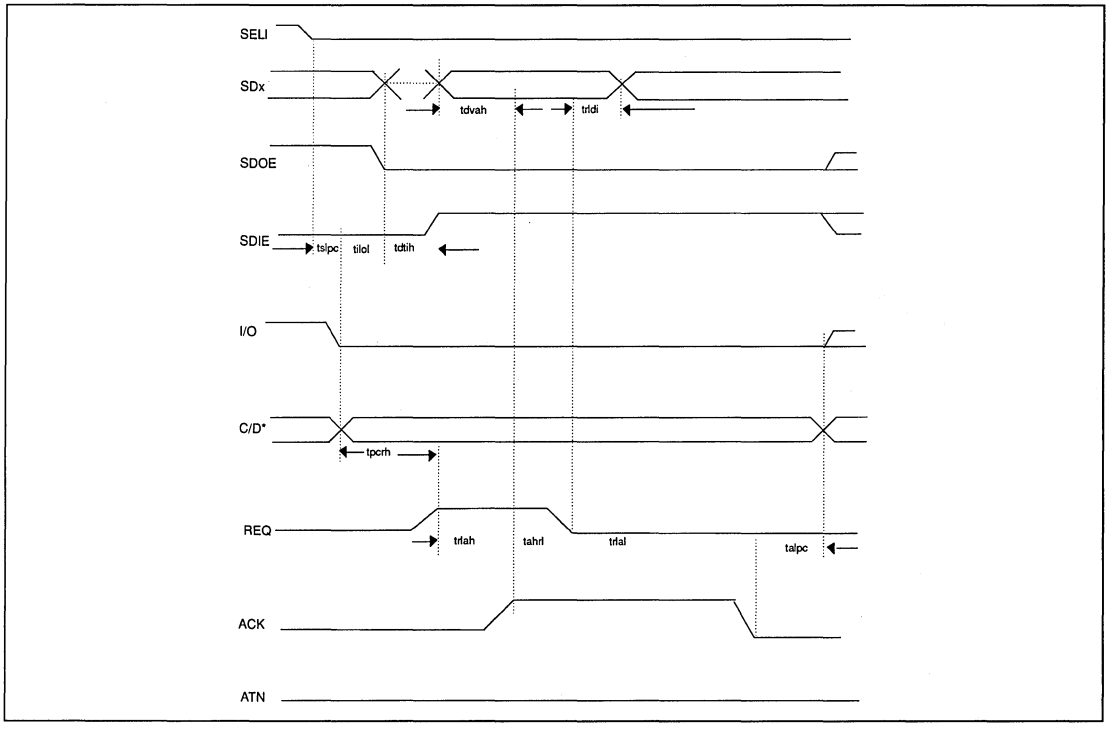

FIGURE 9-22. ASYNCHRONOUS INFORMATION TRANSFER OUT (T)

9.2.10 Synchronous Information Transfer In (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID IN TO REQ IN HIGH	0		ns
trhdi	REQ IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tihol, tdtih, and tpcrh ALSO APPLY (see 9.2.6).

NOTE:
C/D* = C/D, MSG

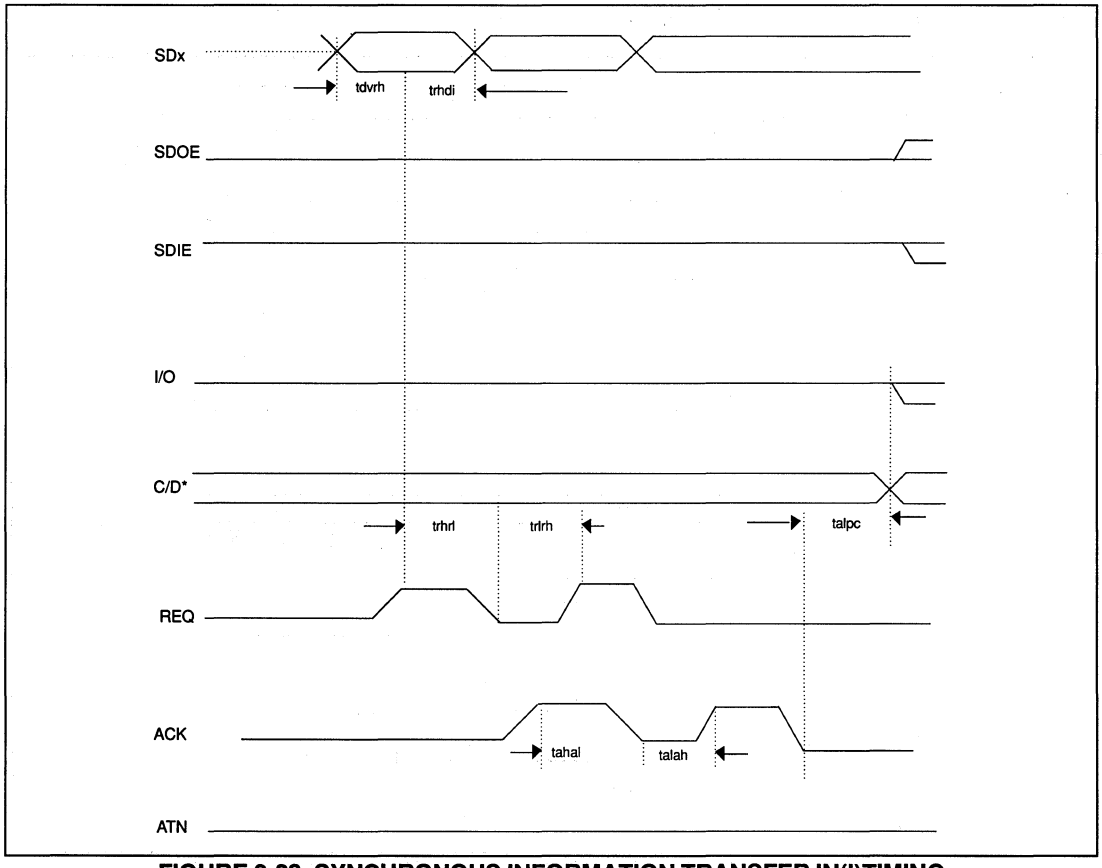

FIGURE 9-23. SYNCHRONOUS INFORMATION TRANSFER IN(I)TIMING

9.2.11 Synchronous Information Transfer In (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvrh	DATA VALID OUT TO REQ OUT HIGH	75		ns
trhdi	REQ OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tihil, tiloh, and tpcrh ALSO APPLY (see 9.2.7).

NOTE:
C/D* = C/D, MSG

22

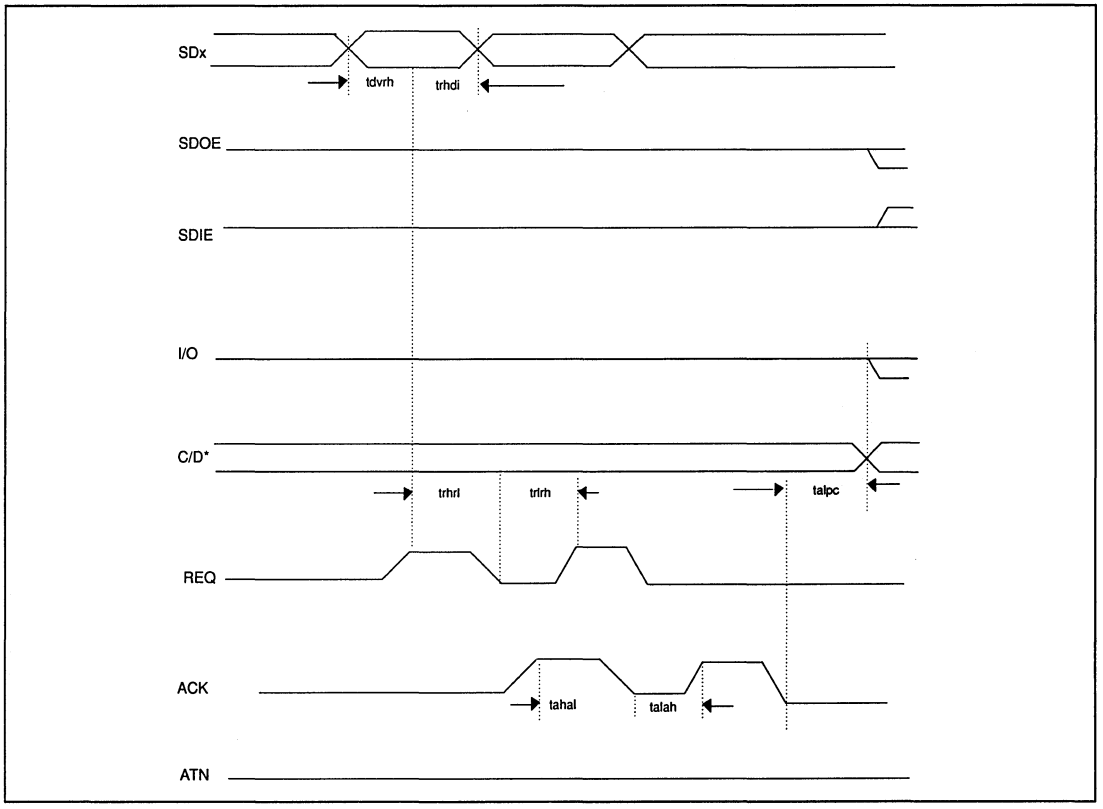

FIGURE 9-24. SYNCHRONOUS INFORMATION TRANSFER IN(T)TIMING

9.2.12 Synchronous Information Transfer Out (Initiator)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID OUT TO ACK OUT HIGH	75		ns
tahdi	ACK OUT HIGH TO DATA INVALID OUT	115		ns
trhrl	REQ IN HIGH TO REQ IN LOW	50		ns
trlrh	REQ IN LOW TO REQ IN HIGH	50		ns
tahal	ACK OUT HIGH TO ACK OUT LOW	1-15ns		Tcyc
talah	ACK OUT LOW TO ACK OUT HIGH	1-15ns		Tcyc
talpc	ACK OUT LOW TO PHASE CHANGE IN	0		ns

PARAMETERS tslpc, tiloh, tilil, and tpcrh ALSO APPLY (see 9.2.8).

NOTE:
C/D* = C/D, MSG

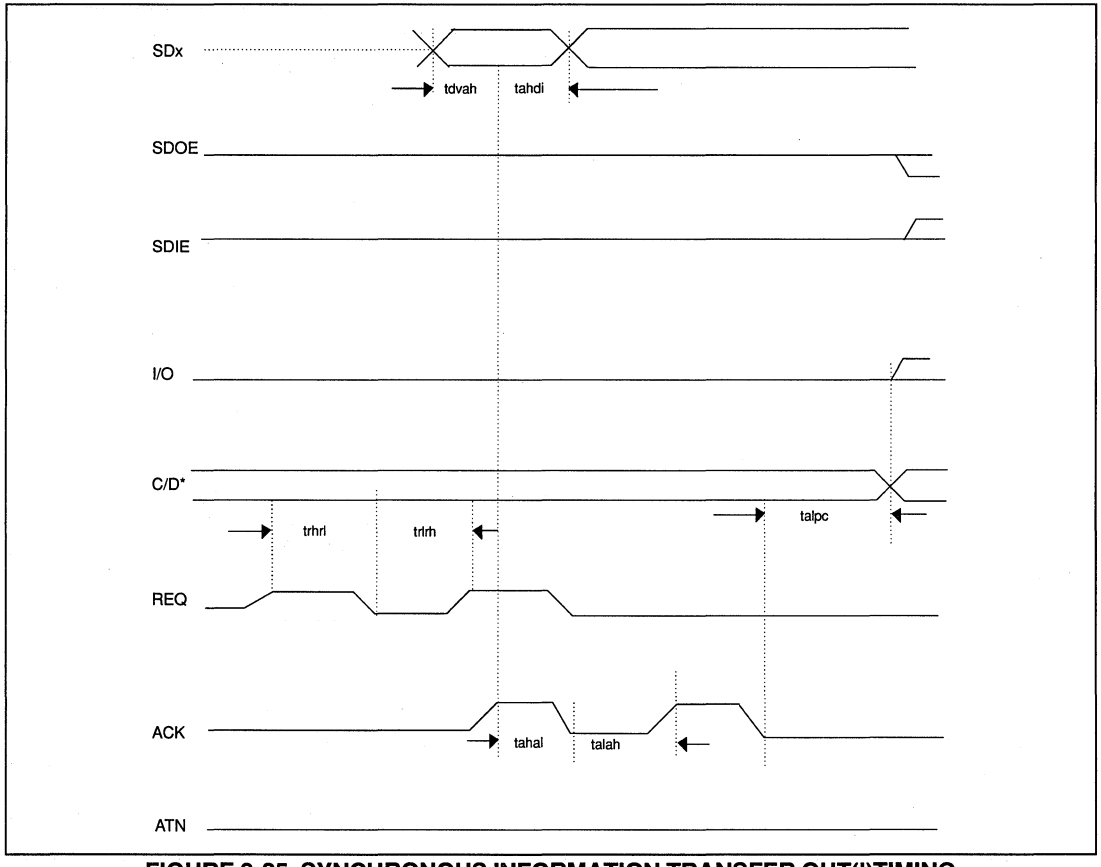

FIGURE 9-25. SYNCHRONOUS INFORMATION TRANSFER OUT(I)TIMING

9.2.13 Synchronous Information Transfer Out (Target)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tdvah	DATA VALID IN TO ACK IN HIGH	0		ns
tahdi	ACK IN HIGH TO DATA INVALID IN	45		ns
trhrl	REQ OUT HIGH TO REQ OUT LOW	1-15ns		Tcyc
trlrh	REQ OUT LOW TO REQ OUT HIGH	1-15ns		Tcyc
tahal	ACK IN HIGH TO ACK IN LOW	50		ns
talah	ACK IN LOW TO ACK IN HIGH	50		ns
talpc	ACK IN LOW TO PHASE CHANGE OUT	0		ns

PARAMETERS tslpc, tilol, tdtih, and tpcrh ALSO APPLY (see 9.2.9).

NOTE:
C/D* = C/D, MSG

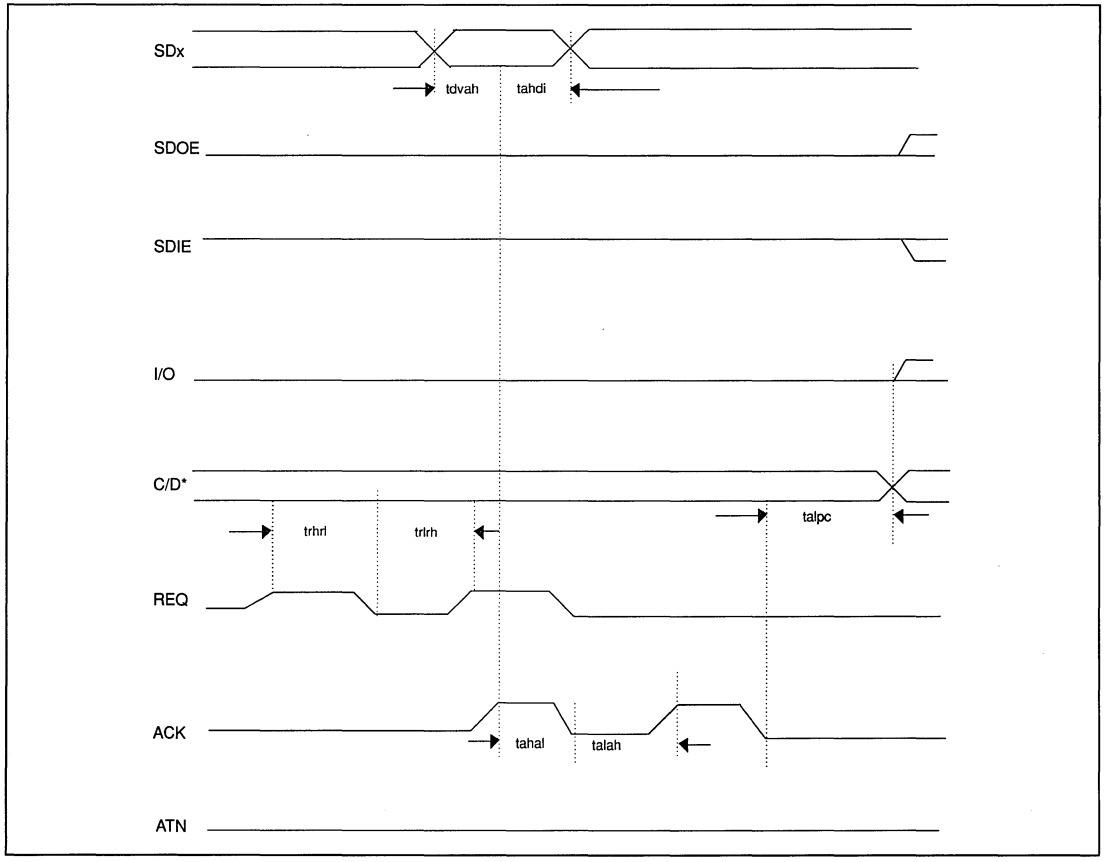

FIGURE 9-26. SYNCHRONOUS INFORMATION TRANSFER OUT(T)TIMING

9.2.14 Arbitration To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tshbl	SELI HIGH TO BSYO, SDOE, ARBLD LOW		8+120ns|	Tcyc

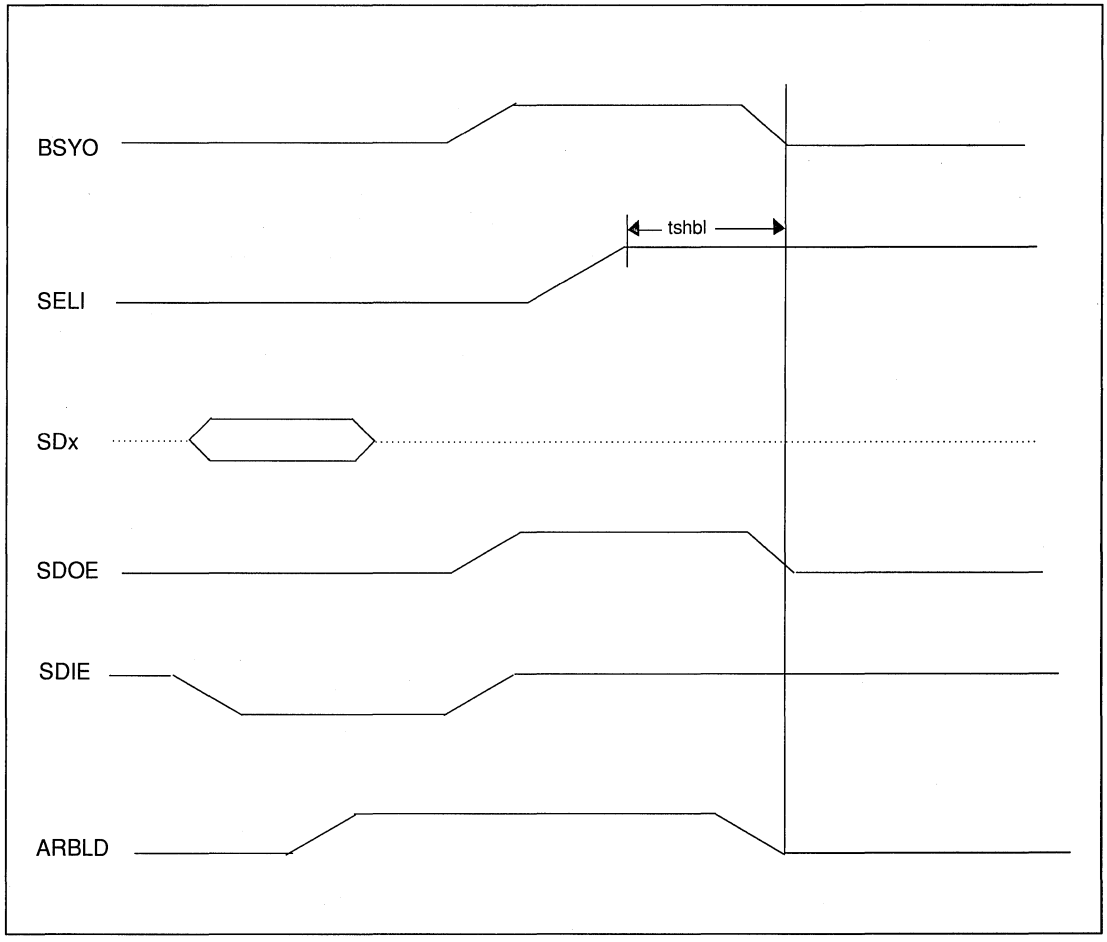

FIGURE 9-27. ARBITRATION TO BUS FREE TIMING

9.2.15 Selection (Initiator) Or Reselection (Target) To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
ttadc	TIMEOUT OR ABORT TO DATA BUS CLEARED*	0		ns
tdcsl	DATA BUS CLEARED* TO SELO LOW	200		µs
tslih	SELO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tsldt	SELO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tslgl	SELO LOW TO gs LOW, cntl TRISTATE		8+120ns	Tcyc

* SDx logic low, causing logic low on SCSI data bus.

NOTE:
gs = IGS (INITIATOR) or TGS (TARGET)
cntl = ATN, ACK (INIT) or I/O, C/D, MSG, and REQ (TARGET)

22

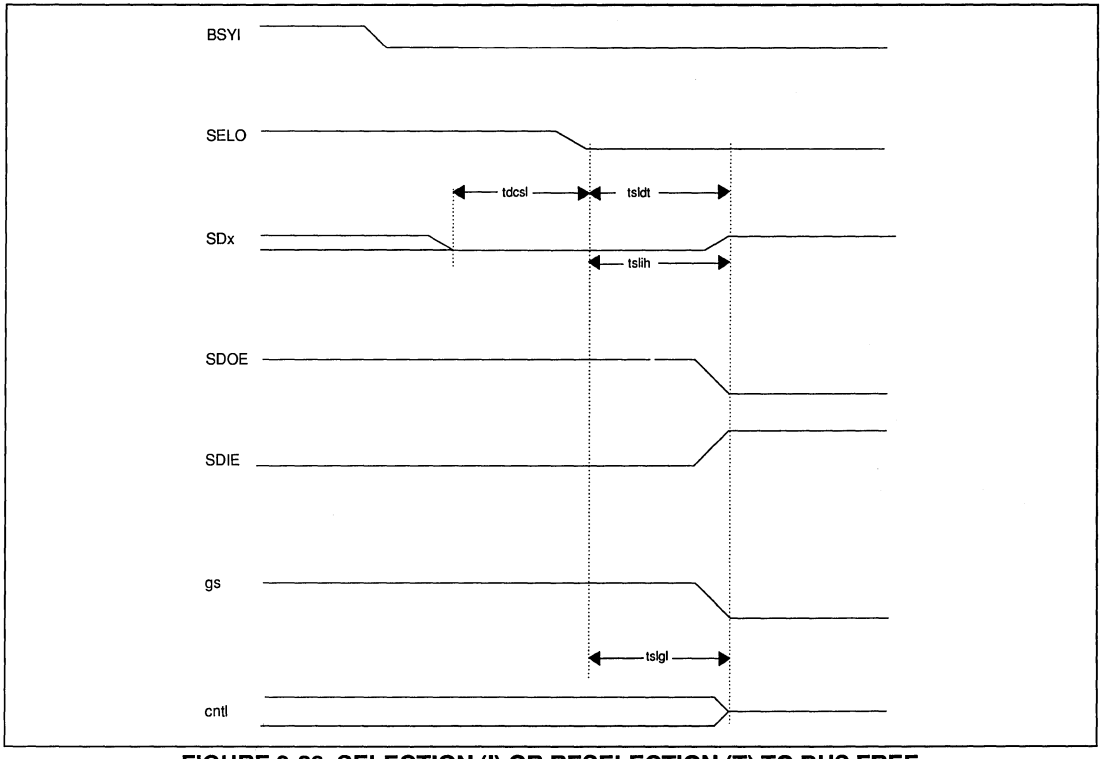

FIGURE 9-28. SELECTION (I) OR RESELECTION (T) TO BUS FREE

9.2.16 Connected-as-an-Initiator To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYI LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYI LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYI LOW TO IGS LOW, ATN TRISTATE		8+120ns	Tcyc

NOTE:
ATN* = ATN, ACK

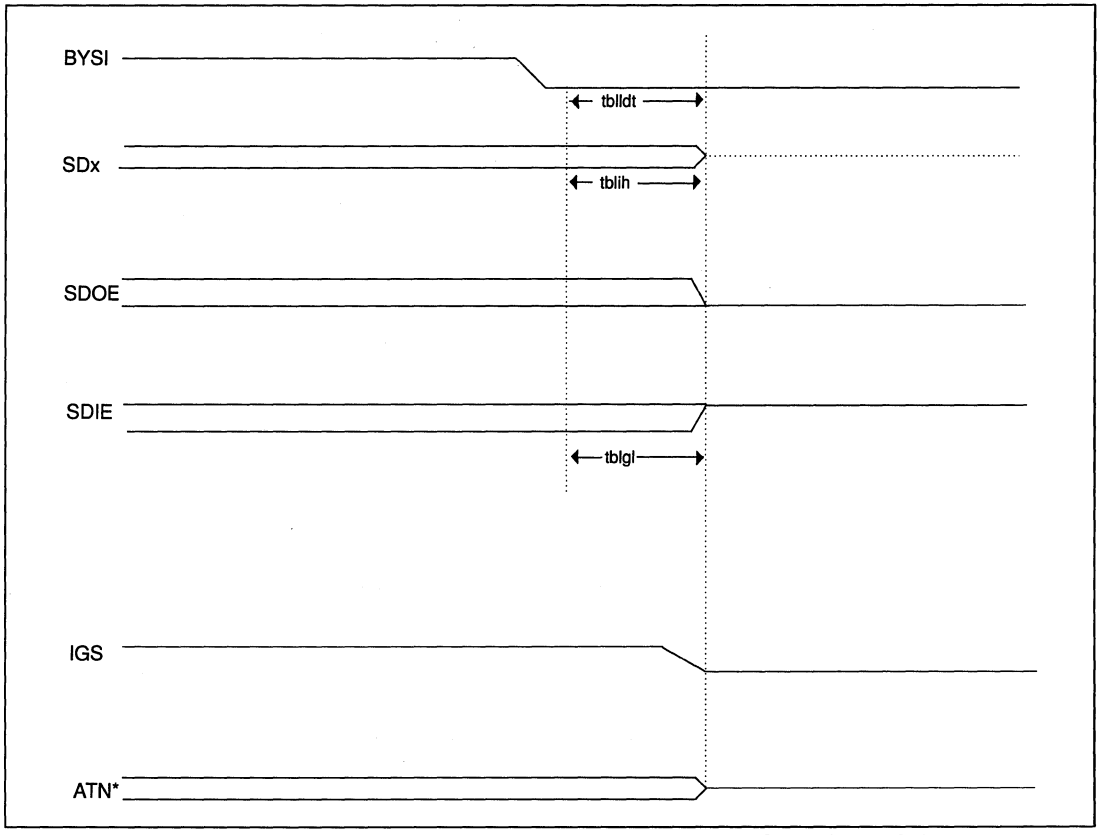

FIGURE 9-29. CONNECTED-AS AN-INITIATOR TO BUS FREE TIMING

9.2.17 Connected-as-a-Target To Bus Free

SYMBOL	CHARACTERISTIC	MIN	MAX	UNITS
tblih	BSYO LOW TO SDIE HIGH, SDOE LOW		8+120ns	Tcyc
tbldt	BSYO LOW TO DATA BUS TRISTATE		8+120ns	Tcyc
tblgl	BSYO LOW TO TGS LOW, I/O TRISTATE		8+120ns	Tcyc

NOTE:
I/O* = I/O, C/D, MSG, REQ

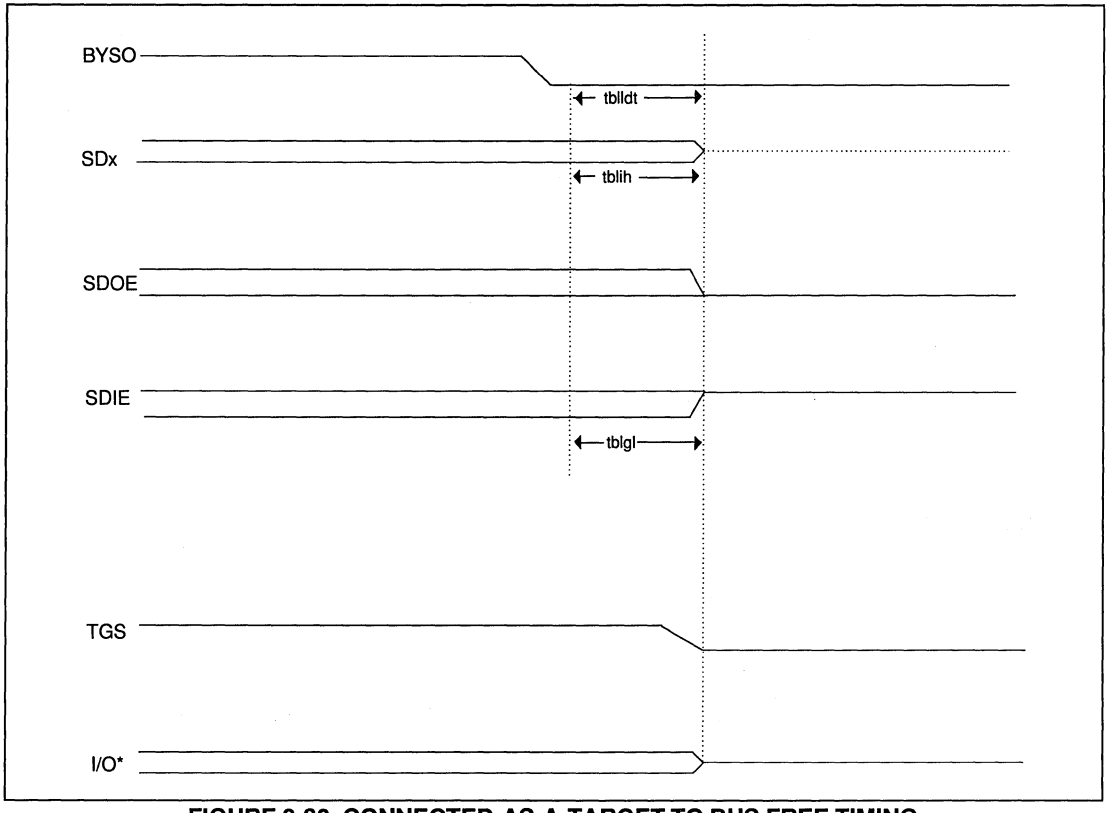

FIGURE 9-30. CONNECTED-AS-A-TARGET TO BUS FREE TIMING