WD1001 Winchester Disk Controller

FEATURES

- SINGLE +5V SUPPLY
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROL FOR UP TO 4 DRIVES
- CONTROL FOR UP TO 8 R/W HEADS
- 1024 CYLINDER ADDRESSING RANGE
- 256 SECTOR ADDRESSING RANGE
- 32 BIT ECC FOR BURST ERROR CORRECTION
- ERROR CORRECTION ON DATA FIELD ERRORS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD BLOCK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 128, 256, OR 512 BYTES PER SECTOR (SOFTWARE SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY
- MULTIPLE SECTOR READS AND WRITES
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS
- AUTOMATIC RETRIES ON ALL ERRORS
- AUTOMATIC RESTORE AND RE-SEEK ON SEEK ERROR
- WD1001-55, -85 SAME FORM FACTOR AS WD1000
- WD1001-05 CAN BE MOUNTED ON 5¼" DRIVE

GENERAL DESCRIPTION

The WD1001 is a stand-alone, general purpose Winchester controller board designed to interface up to four Winchester disk drives to a host processor. The drive signals are based upon the floppy look-alike interface available on the Shugart Associates' SA 1000, the Seagate Technology ST506, the Quantum Q2000, and other compatible drives. All necessary buffers and receivers/drivers are included on the board to allow direct connection to the drive.

Communications to and from the host computer are made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on board sector buffer allows data transfers to the host computer independent of the actual data transfer rate of the drive. The WD1001 is based upon a proprietary chip series, the WD1100, specifically designed for Winchester Control.

ORGANIZATION

The WD1001 has seven on-board connectors. These connectors consist of a power connector, host interface connector, drive control connector, and four high speed data cable connectors.

The drive control cable is daisy-chained to each of the four drives. Although there is space for two drive control connectors, only one would normally be used for any particular configuration.

The drive data connectors carry differential signals and are radially connected. Up to four drives can be accommodated by the WD1001.

The host interface connector provides interface signals that are compatible with most microprocessors and mini-computers.

The WD1001 provides dual burst detection and single 5-bit burst correction ECC circuitry. The ECC polynomial has been computer generated for optimum error correction on Winchester Disks.

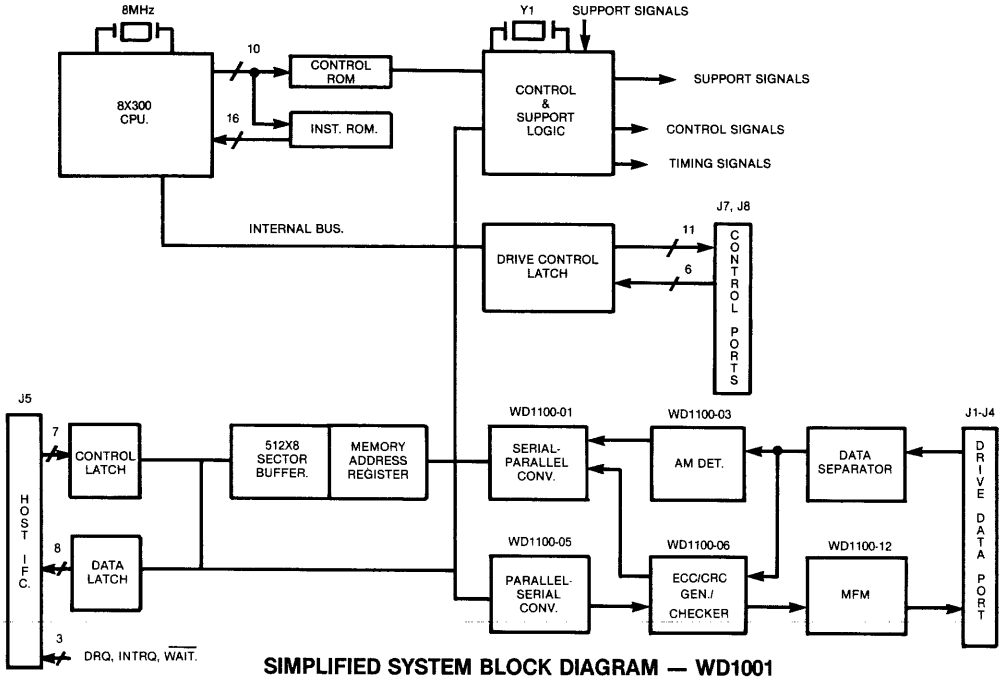
SPECIFICATIONS

Encoding method:	MFM
Cylinders per Head:	Up to 1024
Sectors per Track:	Up to 256 (512 byte sec)
Heads:	8
Drive Selects:	4
Step rate:	10 μS to 7.5 mS (0.5 mS increments)
Data Transfer Rate:	4.34 Mbits/sec (WD1001-85) 5.000 Mbits/sec (WD1001-05, -55)
Write Precomp Time:	12 nanoseconds
Sectoring:	Soft
Host Interface:	8 Bit bi-directional bus
Drive Capability:	10 "LS" Loads
Drive Cable Length:	10 ft. (3M) max.
Host Cable Length:	3 ft. (1M) max.
Power Requirements:	+5V ±5%, 3.0A Max. (2.5A typ.)
Ambient Temperature Operating:	0°C to 50°C (32 F to 122 F)
Relative Humidity:	20% to 80%
MTBF:	10,000 POH
MTTR:	30 minutes

DIMENSIONS	WD1001-55, -85	WD1001-05
Length:	9.9 in. (24.9 cm)	8.5 in. (21.6 cm)
Width:	6.8 in. (17.1 cm)	5.75 in. (14.6 cm)
Height:	0.75 in. (1.9 cm)	0.75 in. (1.9 cm)
Mounting Centers:	6.375 x 9.375 in. (16 x 23.6 cm)	3.12 in. (7.9 cm)

HOST INTERFACING

The WD1001 is designed to easily interface to most micro computers and mini-computers. All interfacing



SIMPLIFIED SYSTEM BLOCK DIAGRAM — WD1001

is done through the Host Interface Connector (J5). The interface is very similar to Western Digital's family of Floppy Disk Controllers. The only exception is the inclusion of the WAIT line.

WAITS

The $\overline{\text{WAIT}}$ control line goes true whenever either of the following are true:

- The WD1001 is accessing data internally to send to the host during a read operation.
- The WD1001 has not accepted the data from the host during a write operation.

The definition of the $\overline{\text{WAIT}}$ line is very similar to the $\overline{\text{WAIT}}$ signal found on many popular processors. $\overline{\text{WAIT}}$ is also similar to the REPLY signal on Western Digital and other processors.

$\overline{\text{WAIT}}$ will not necessarily make a transition for each access to the WD1001. When the WD1001 can return the requested data within 100 nS, there will be no transition of the $\overline{\text{WAIT}}$ line. This should be interpreted as an instant REPLY on Western Digital Processors.

If the WD1001 cannot return the requested data within 100 nS, it will assert its $\overline{\text{WAIT}}$ line. The period of the $\overline{\text{WAIT}}$ signal will vary from 750 nS to 6 μS with 1.25 μS being about average. The period of the $\overline{\text{WAIT}}$ only approaches 6 μS during a read or write which happens immediately after a command is written to the command register. This means that longer waits may be encountered during the first read or write to any WD1001 register if that first read or write happens within approximately 6 μS of a command being issued.

During the time that $\overline{\text{WAIT}}$ is asserted, the host system **must** hold all of its strobe and address lines stable. On write operations, the DAL lines must also be held stable.

The Host Interface connector (J5) consists of an eight bit bi-directional bus, three bit address bus, and seven control lines. All commands, status, and data are transferred over this bus. See Table 1:

HOST INTERFACE CONNECTOR **TABLE 1**

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{Card\ Select}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written via the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may write data to a selected register of the WD1000.
28	27	$\overline{RE}$	When $\overline{Read\ Enable}$ is active along with $\overline{CS}$, the host may read data from a selected register of the WD1001.
30	29	$\overline{WAIT}$	Upon receipt of a $\overline{CS}$, the $\overline{WAIT}$ line may go active. It returns to the inactive state when the DAL lines are valid on a read, or data has been accepted on a write.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The Data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the Data Register is read from or written to. The DRQ line will continue to toggle until the buffer is exhausted or until a write or read is performed on the Cylinder Low register.
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1001. Sector Number, Cylinder Number and SDH are cleared, stepping rate is set to 7.5 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
	41	Not Connected	Not on WD1001-05
	42	Not Connected	
	43-50	+5V	8 power pins for regulated +5 volts. This power input is also available on J6, pin 3. Not on WD1001-05.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONTROL CONNECTORS

The drive control connector is a (relatively) low speed bus that is daisy chain connected to each of the drives (up to four) in the system. To properly terminate each TTL level output signal from the WD1001, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. All other drives should have no termination. See Tables 2 and 3:

34 PIN DRIVE CONTROL CONNECTOR (WD1001-05, -55) **TABLE 2**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TR000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In

DRIVE CONTROL SIGNAL DESCRIPTIONS

RWC

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

Write Gate

This output signal allows data to be written on the disk.

Seek Complete

Informs the WD1001 that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

Track 000

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

50 PIN DRIVE CONTROL CONNECTOR FOR SA1000 TYPE INTERFACE (WD1001-85) **TABLE 3**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6		NC
7	8	I	Seek Complete
9	10		NC
11	12		NC
13	14	O	Head Select 0
15	16	I	Sector
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24		NC
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32	O	Drive Select 4
33	34	O	Direction In
35	36	O	Step
37	38		NC
39	40	O	Write Gate
41	42	I	TR000
43	44	I	Write Fault
45	46		NC
47	48		NC
49	50		NC

Write Fault

Informs the WD1001 that some fault has occurred on the selected drive. The WD1001 will not execute commands when this signal is true.

HS0 HS2

Head Select lines are used by the WD1001 to select a specific R/W head on the selected drive.

Index

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1001 that the desired drive is selected and that its motor is up to speed. The WD1001 will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

$\overline{\text{Direction In}}$

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

$\overline{\text{DS1}}$ $\overline{\text{DS4}}$

These four Drive Select lines are used to select one of four possible drives.

DRIVE DATA CONNECTOR

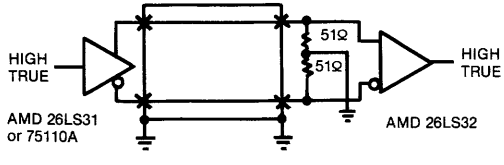
Four data connectors (J1-4) are provided for clock signals and data between the WD1001 and each drive. All lines associated with the transfer of data between the drive and the WD1001 system are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers that mate with Burndy #FRS20BS. The cable used should be flat ribbon cable or twisted pair with a length of less than 10 feet. The cable pin-outs are per Table 4:

DATA CONNECTIONS AND DESCRIPTIONS **TABLE 4**

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1	I	– Drive Selected
4	3		NC
6	5		NC
8	7		NC
	9	O	+ Timing Clock*
	10	O	– Timing Clock*
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

*WD1001-55, -85 only.

DIFFERENTIAL DATA DRIVER/RECEIVER



NOTE: ANY RS 422 DRIVER/RECEIVER PAIR WILL INTERFACE

Z_X = 105Ω
FLAT RIBBON OR TWISTED PAIR
MAX 10 FT.

POWER CONNECTOR

A three pin Molex connector (J6) is provided for power input to the WD1001-55 and -85. A four pin Amp connector is used on the WD1001-05. See Table 5:

TABLE 5

PIN	WD1001-55, -85	WD1001-05
1	Ground	Not Connected
2	NC	Ground
3	+5V Regulated	Ground
4	—	+5V Regulated
Housing	Molex 03-07-1032	Amp 1-4840429-0

COMMANDS

The WD1001 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1001 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mispositions, the WD1001 will automatically perform a restore and a re-seek. If the error is completely unrecoverable, the WD1001 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. No command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1001 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types which are summarized in Table 6:

TABLE 6

TYPE	COMMAND	BITS 7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r_3	r_2	r_1	r_0
I	Seek	0	1	1	1	r_3	r_2	r_1	r_0
II	Read Sector	0	0	1	0	D	M	L	0
III	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

r_3-r_0 — STEPPING RATE

0000 = 35μS	1000 = 4.0mS
0001 = 0.5mS	1001 = 4.5mS
0010 = 1.0mS	1010 = 5.0mS
0011 = 1.5mS	1011 = 5.5mS
0100 = 2.0mS	1100 = 6.0mS
0101 = 2.5mS	1101 = 6.5mS
0110 = 3.0mS	1110 = 7.0mS
0111 = 3.5mS	1111 = 7.5mS

D = DMA Read Mode
0 = Programmed I/O Mode
1 = DMA Mode

L = Long Read/Write
0 = Normal Read/Write
1 = Long Read/Write

M = 1 = Multiple Sector Read/Write
0 = Single Sector Read/Write

NOTE:
The DMA bit is used to position INTRQ in relation to DRQs during the read sector command. If the DMA bit is reset (D = 0), the interrupt will occur before the first DRQ. This allows the programmed I/O host to intervene and transfer the data from the sector buffer. If the DMA bit is set (D = 1), then the interrupt will occur only after the system DMA controller has transferred the entire buffer of data.

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

RESTORE

The Restore command is used to calibrate the position of the R/W head on each drive by stepping the head outward until the TR000 line goes true. Upon receipt of the Restore command, the Busy bit in the Status Register is set. Cylinder High and Cylinder Low Registers are cleared. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is rest.

If no errors are encountered thus far, the internal head position register for the selected drive is cleared. The TR000 line is sampled. If TR000 is true, an interrupt is generated and the Busy bit is reset. If TR000 is not true, stepping pulses at a rate determined by the stepping rate field are issued until the TR000 line is activated. When TR000 is activated, the Busy bit is reset and an interrupt is issued. If the TR000 line is not activated within 1023 stepping pulses, the TR000 Error bit in the Error Register and the Error bit in the Status Register are set, the Busy bit is reset and an interrupt is issued.

SEEK

The Seek command positions the R/W head to a certain cylinder. It is primarily used to start two or more concurrent seeks on drives that support buffered stepping. Upon receipt of the Seek command, the Busy bit in the Status Register is set. The lower four bits of the command byte are stored in the stepping rate register for subsequent implied seeks. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered thus far, the internal head position register for the selected drive is updated, the direction line is set to the proper direction and a step pulse is issued for each cylnder to be read and an interrupt is issued. Note that the Seek Complete line is not sampled after the Seek command, allowing multiple seek operations to be started using drives with buffered seek capability.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1001 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

READ SECTOR

The Read Sector command is used to read a sector of data from the disk to the host computer. Upon receipt of the Read command, the Busy bit in the Status register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted Command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line does not go true within 128 Index pulses, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, and a normal completion is simulated.

Once the head has settled over the desired cylinder, the WD1001 will attempt to read the sector. The WD1001 performs all retries necessary to recover the data during the read command. The controller attempts to read the desired sector up to 16 times. It will attempt a retry if it does not find an ID, if the ID of that sector has a bad CRC or if the Data Address Mark (DAM) couldn't be found or even if the data was actually read from the disk but incurred an uncorrectable error.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to read the sector once again. An auto-restore will be performed only once per read or write sector command.

If the WD1001 encounters an ECC error, it will attempt to correct the data in its sector buffer. If it can correct the data, the Corrected bit in the Status

register will be set, if not, the Uncorrectable Error bit is set.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. If the Uncorrectable bit is set, the data that last produced that error will be available in the sector buffer. The Error bit in the Status Register is set and a normal completion is simulated.

READ LONG

This variation of the Read command allows the user to read the ECC check bits directly. The check bits are placed in the data buffer immediately behind the data. This increases the effective buffer length by four bytes.

TYPE III COMMANDS

This type of command is characterized by a transfer of a block of data from the host to the WD1001 buffer. These commands have implicit stepping rates as set by the last Restore or Seek command.

WRITE SECTOR

The Write Sector command is used to write a sector of data from the host computer to the disk. Upn receipt of the Write command, the controller generates DRQs for each byte to be written to the buffer. (Note: It is recommended that programmed I/O transfers should take place as a block move without consulting the DRQ bit in the Status Register.)

After all data has been sent to the sector buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault are sampled, and if an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. The Seek Complete line is sampled. If the Seek Complete line doesn't go true within 128 Index pulses, then the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, it will attempt to read the ID of the sector. The WD1001 performs all retries necessary to recover the ID during the write command. The controller attempts to read the ID of the desired sector up to 16 times. It will attempt a retry if it doesn't find an ID or if the ID of that sector has a bad CRC.

Every time the controller encounters an error, it records the occurrence of that error in an internal register. If, after 16 retries, the controller was not able to get a match on the ID field, it assumes that the head was possibly mis-positioned and executes an auto-restore. During the auto-restore, the stepping rate is implied to be equal to the Seek Complete period. After the auto-restore has been successfully completed, the controller re-seeks and attempts to write the sector once again.

If the controller encounters a non-recoverable error, the controller examines its internal error history register. It then sets the bit in the Error Register of the highest severity error incurred. The Error bit in the Status Register is set, an Interrupt is generated and the Busy bit is reset.

If the proper sector is located, the sector buffer is written to the disk, an interrupt is generated and the Busy bit is reset.

WRITE LONG

This variation of the write command allows the user to introduce various error patterns to check correction capability. The check bits follow the data in the sector buffer. This increases the effective buffer length by four bytes.

FORMAT TRACK

The Format command is used for initializing the ID and data fields on a particular disk. Upon receipt of the Format command, the controller generates DRQs for each byte of the interleave table to be written to the buffer. In all cases, the number of bytes transferred to the buffer must correspond to the current sector size.

After all data has been sent to the buffer, the Busy bit in the Status Register is set. The state of Seek Complete, Ready and Write Fault lines are sampled. If an error condition exists, the Aborted command bit in the Error Register is set, the Error bit in the Status Register is set, an interrupt is generated and the Busy bit is reset.

If no errors are encountered so far, a Seek command is executed. No verification of track positioning accuracy is performed because the track may not have any ID fields present. After the Seek operation has been performed, the Seek Complete line is sampled. If the Seek Complete line is not asserted within 128 Index pulses, the Aborted command bit in the Error Register is set, an Interrupt is generated and the Busy bit is reset.

Once the head has settled over the desired cylinder, the controller starts writing a pattern of 4E's until the index is encountered. Once the index is found, a number of ID fields and nulled data fields are written to the disk. The number of sectors written is equal to the contents of the Sector Count Register. As each sector is written, the Sector Count Register is decremented, and consequently, must be updated before each format operation.

NOTE:

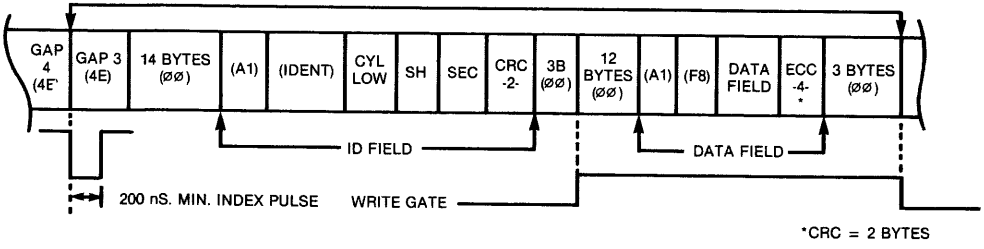
1) When MSB of head byte = 1, bad block is detected.
2) Write Gate turn-on is 3 bytes after the ID field's CRC bytes.
3) Write Gate turn-off is 3 bytes after the Data Field's ECC or CRC bytes.
4) 12 bytes of zeroes are re-written on a Data Field update.
5) The 2 LSB's of the IDENT byte are used for Cylinder high

These values are:

FE = 0 to 255 cylinders
FF = 256 to 511 cylinders
FC = 512 to 767 cylinders
FD = 768 to 1023 cylinders

6) GAP 3 values are:

SECTOR LENGTH	GAP 3
128	15
256	15
512	30



After the last sector is written, the controller backfills the track with 4E's. When the next index pulse after the last sector is written is encountered, the format operation is terminated, an Interrupt is generated and the Busy bit is reset.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1001 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1001 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1001 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High	Cylinder High
0	1	1	0	Size/Drive/head	Size/Drive/head
0	1	1	1	Status Register	Command Register

SDH REGISTER

BIT	7	6 5	4 3	2 1 0
FUNCTION	Sec Ext	Sec Size	Drive Select	Head Select

BIT 7	SECTOR EXTENSION
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Drive Sel 1
0	1	Drive Sel 2
1	0	Drive Sel 3
1	1	Drive Sel 4

BIT 2	BIT 1	BIT 0	HEAD SELECTED
0	0	0	Head 0
0	0	1	Head 1
0	1	0	Head 2
0	1	1	Head 3
1	0	0	Head 4
1	0	1	Head 5
1	1	0	Head 6
1	1	1	Head 7

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	Uncorrectable
5	Write Fault	CRC Error — ID Field
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected	Aborted Command
1	—	TR000 Error
0	Error	DAM not found

PROGRAMMING

Users familiar with floppy disk systems will find programming the WD1001 a pleasant surprise. A substantial amount of intelligence that was required by the host computer has been incorporated into the WD1001. The WD1001 performs all needed retries, even on data ECC and head positioning errors. Most commands feature automatic 'implied' seek which means that seek commands need not be issued to perform basic read/write functions. The WD1001 keeps track of the position of up to four read/write head assemblies, so the host system does not have to maintain track tables. All transfers to and from the disk are through an on-board full sector buffer. This means that data transfers are fully interruptable and can take place at any speed that is convenient to the system designer. In the event of an unrecoverable error, the WD1001 simulates a normal completion so that special error recovery software is not needed.

ERROR CORRECTION

General Description

The WD1001 with ECC is specifically designed to add error correction capabilities to 8" or 5.25" Winchester disk drives. The Polynomial selected is a computer generated code, optimized for sector sizes of 128, 256 and 512 byte data fields. The forur ECC bytes appended by this device enable correction of a single burst of 8 bits. Simultaneously it can detect a double burst of two bits in error.

During a write operation, the input stream is divided by the polynomial, X32 + X28 + X26 + X19 + X17 + X10 + X6 + X2 + 1 and the resulting 32 bit remainder is used as the four check bytes. In a Read operation the check bit are recomputed and compared to the recorded check bits to generate the four syndrome bytes. If the syndrome is zero, no errors were detected. Otherwise, the non-zero syndrome is used by the ECC processor to compute the displacement and the error vector within the sector. This information is then used to correct the data if a single burst of no more than 5 bits in error occurred.

Data Accuracy

ERP (Error Recovery Procedure) strategies have a significant influence on data accuracy. An ERP strategy requires data to be reread before applying correction and results in much better data accuracy. The WD1001 employs such a strategy. This strategy reduces the possibility of passing undetected, erroneous data by rereading until the error goes away.

Correction is applied only after the syndrome has been received and has the following parameters:

1. Single burst detection span with correction = 20 bits with max. correction span = 5 bits
2. Double burst detection span with correction = 4 bits with max. correction span = 5 bits
3. Non detection probability = 2.3 E-10
4. Miscorrection probability = 8.00 E-6 for max. correction span = 5 bits (256 byte Sector)

*All parameters given with respect to a 256 byte record length.

Correction Time Performance

All real time operations are performed with error correction hardware. The software algorithims used on the WD1001 get involved only after an error has been detected.

The following correction times are for a serial algorithim such as that used on the WD1001:

a) 30mS max.
b) 15mS min.
c) 20mS ave.

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PRELIMINARY

WD1002-05 Winchester/Floppy Controller

FEATURES

- SINGLE +5V POWER SUPPLY.
- CONTROL FOR UP TO 3 WINCHESTER AND 4 FLOPPY DRIVES.
- ON BOARD DATA SEPARATOR AND WRITE PRECOMPENSATION.
- 128, 256, 512, AND 1024 BYTE SECTOR SIZES.
- PROGRAMMABLE SECTOR SIZES TO 1K.
- AUTOMATIC TRACK FORMATTING ON HARD AND FLOPPY DISKS.
- MULTIPLE SECTOR OPERATIONS.
- 5 BIT SINGLE BURST ERROR CORRECTION ON WINCHESTER.
- CRC GENERATION/VERIFICATION ON ID FIELDS.
- 5 MBIT DATA TRANSFER RATE.
- ECC DIAGNOSTIC COMMANDS (READ LONG & WRITE LONG).

DESCRIPTION

The WD1002-05 Winchester-Floppy Controller (WFC) is a stand-alone general purpose board designed to interface up to three 5¼" Winchester hard disks and up to four 5¼" floppy disk drives. The WFC implements all the logic required for a variable length sector (to 1K bytes), ECC correction, data separation and host interface circuitry. The Winchester interface is based on the Seagate ST506 and the floppy interface on the Shugart SA450. All necessary buffers and drivers/receivers are on board.

Communication to and from the host is made via a separate computer access port. This port consists mainly of an 8 bit bi-directional bus and appropriate control signals. All data to be written to or read from the disk, status information, and macro commands are transferred via this 8 bit bus. An on-board sector buffer allows data transfers to the host computer at a rate independent of the drive transfer rate.

The WD1002-05 Controller board is based on the WD1014 EDS device and 1015 Buffer Controller device, as well as the WD2797 Floppy Disc Controller and WD1010 Winchester Disk Controller chips. It is form factor compatible with most 5¼" Winchesters and may be directly mounted on the drive.

ARCHITECTURE

The Block Diagram of the WD1002-05 is shown in Figure 1. The heart of the system is the WD1015 Buffer/Controller, which generates and processes all data and control lines, along with the WD1014 EDS that generates all control signals that cannot be handled in real time by the WD1015.

Commands, parameters, and data are entered via the Host Interface Logic. The WD1015 accepts both floppy and Winchester commands in identical format, converting these parameters to the WD2797/WD1010 protocol. Data is read from the selected drive and transferred to the sector buffer. If an error in the data field has been encountered, the WD1015 will instruct one of the controllers to perform retries automatically. In the case of an access on a Winchester drive, the WD1014 ECC device will be enabled and error correction procedures will be invoked. Error Correction may be disabled via software from the Host to allow "CRC-only" formatted Winchester drives to be used in the system. Data Separation and Write Precompensation Logic is on-board for Winchester transfers, while the WD2797 Floppy Controller provides an integrated separator and ajustable precomp. After the sector buffer is full, the WD1015 informs the Host Interface Logic that data may be read by the Host. The use of an on-board sector buffer provides both transparent error correction and data transfers to the Host that are independent of drive transfer rates.

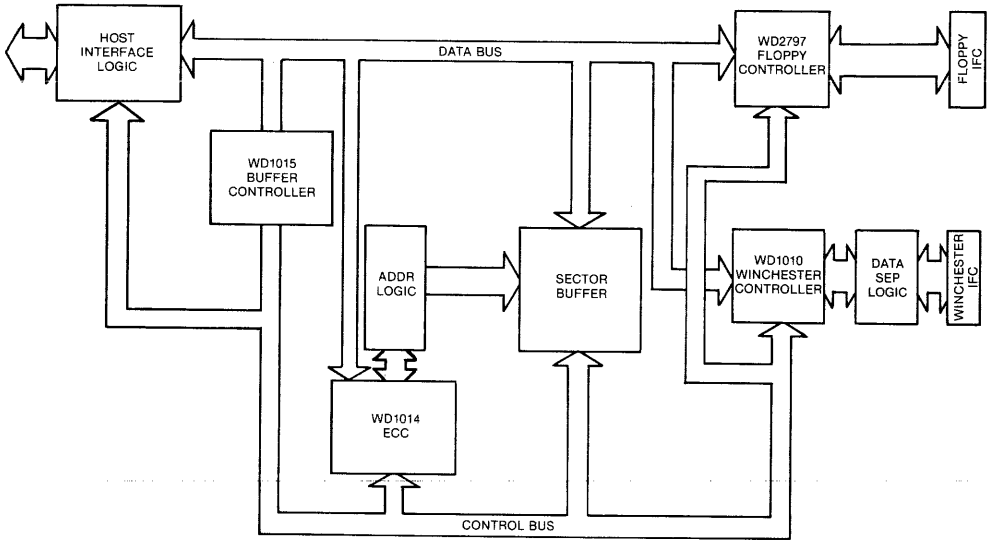

Figure 1. WD1002-05 BLOCK DIAGRAM

HOST INTERFACE

The WD1002-05 has been designed to interface to a Host processor via a parallel port or CPU bus configurations. The specific signals are compatible with the Western Digital WD1000/WD1001 series of Winchester-only controller boards. With the inclusion of the WD1015, the previous WAIT signal is no longer necessary but has been provided for compatibility; status information is always available to the Host for monitoring command progress. When the Busy bit is set, no other status bits are valid.

The Host Interface connector (J5) consists of an 8 bit bi-directional bus, three address lines, and read and write strobes. All functions within the WD1002-05 are initiated by the Host Interface.

HOST INTERFACE CONNECTOR

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
2 4 6 8 10 12 14 16	1 3 5 7 9 11 13 15	DAL0 DAL1 DAL2 DAL3 DAL4 DAL5 DAL6 DAL7	8 bit bi-directional Data Access Lines. These lines remain in a high-impedance state whenever the $\overline{CS}$ line is inactive.
18 20 22	17 19 21	A0 A1 A2	These three Address Lines are used to select one of eight registers in the Task File. They must remain stable during all read and write operations.
24	23	$\overline{CS}$	When $\overline{\text{Card Select}}$ is active along with $\overline{RE}$ or $\overline{WE}$, Data is read or written vis the DAL bus. $\overline{CS}$ must make a transition for each byte read from or written to the task file.
26	25	$\overline{WE}$	When Write Enable is active along with $\overline{CS}$, the host may read data to a selected register of the WD1002-05.
28	27	$\overline{RE}$	When Read Enable is active along with $\overline{CS}$, the host may read data from a selected register of the WD1002-05.
30	29	Pull-Up (PUP)	Used only when replacing WD1000 or WD1001 with WD1002-05. Tied to a pull-up resistor.
32	31	Not Connected	
34	33	Not Connected	
36	35	INTRQ	The INTerrupt ReQuest Line is activated whenever a command has been completed. It is reset to the inactive state when the Status Register is read, or a new command is loaded via the DAL lines.
38	37	DRQ	The data ReQuest line is activated whenever the sector buffer contains data to be read by the host, or is awaiting data to be loaded by the host. This line is reset whenever the buffer has been exhausted or filled by the host.
40	39	MR	The Master Reset line initializes all internal logic on the logic on the WD1002-05. Sector Number, Cylinder Number and SDH are cleared, stepping rate for Winchester devices are set to 7.5 mS, stepping rate for floppies is set to 40 mS, Write Precomp is set to cylinder 128 and Sector Count is set to 1. The DRQ and INTRQ lines are reset.
Note: Grounds			All even numbered pins (2 through 40) are to be used as signal grounds. Power ground is available on J6, pin 1.

DRIVE CONNECTORS

Six connectors are provided for connection of up to 3 Winchester and 4 Floppy drives. All applicable drivers and receivers have been included on the board to allow direct connections to the drives. All signals to the Floppies are daisy-chained and require the last (or only) drive to contain termination resistors.

The Winchester control cable is also daisy-chained and requires similar termination. Most Floppy/Winchester drives can be configured to provide this. The data cables on the Winchester are radially connected to each drive. Three data cable connectors are included on the board.

FLOPPY DRIVE CONTROL/DATA CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2		NC
3	4		NC
5	6	O	Drive Select 1
7	8	I	Index/Sector
9	10	O	Drive Select 2
11	12	O	Drive Select 3
13	14	O	Drive Select 4
15	16	O	Motor On
17	18	O	Direction In
19	20	O	Step
21	22	O	Write Data
23	24	O	Write Gate
25	26	I	Track 00
27	28	I	Write Protect
29	30	I	Read Data
31	32	O	Side Select
33	34		NC

34 PIN WINCHESTER DRIVE CONTROL CONNECTOR

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
1	2	O	RWC
3	4	O	Head Select 2
5	6	O	Write Gate
7	8	I	Seek Complete
9	10	I	TR000
11	12	I	Write Fault
13	14	O	Head Select 0
15	16		NC
17	18	O	Head Select 1
19	20	I	Index
21	22	I	Ready
23	24	O	Step
25	26	O	Drive Select 1
27	28	O	Drive Select 2
29	30	O	Drive Select 3
31	32		NC
33	34	O	Direction In

WINCHESTER DRIVE DATA CONNECTIONS AND DESCRIPTIONS

SIGNAL GROUND	SIGNAL PIN	I/O	SIGNAL NAME
2	1		NC
4	3		NC
6	5		NC
8	7		NC
10	9		NC
11			GND
12			GND
	13	O	+ MFM Write Data
	14	O	– MFM Write Data
15			GND
16			GND
	17	I	+ MFM Read Data
	18	I	– MFM Read Data
19			GND
20			GND

POWER CONNECTOR

A four pin AMP connector is used for power input to the WD1002-05. The pin-outs are as shown:

POWER CONNECTOR

PIN	SIGNAL NAME
1	NC
2	GROUND
3	GROUND
4	+5V REGULATED

COMMANDS

The WD1002-05 executes five easy to use macro commands. Most commands feature automatic 'implied' seek, which means the host system need not tell the WD1002-05 where the R/W heads of each drive are or when to move them. The controller automatically performs all needed retries on all errors encountered including data ECC errors. If the R/W head mis- positions, the WD1002 will automatically perform a restore and a re-seek. If the error is completely uncoverable, the WD1002-05 will simulate a normal completion to simplify the host system's software.

Commands are executed by loading the command byte into the Command Register while the controller is not busy. (Controller will not be busy if it has completed the previous command.) The task file must be loaded prior to issuing a command. On Write/Format operations, the Sector buffer must be filled with the required data before the command can be executed by the WD1002-05. On Winchester drives no command will execute if the Seek Complete or Ready lines are false or if the Write Fault line is true. Normally it is not necessary to poll these signals before issuing a command. If the WD1002-05 receives a command that is not defined in the following table, undefined results will occur.

For ease of discussion, commands are divided into three types:

TYPE	COMMAND	7	6	5	4	3	2	1	0
I	Restore	0	0	0	1	r3	r2	r1	r0
I	Seek	0	1	1	1	r3	r2	r1	r0
II	Read Sector	0	0	1	0	D	M	L	0
II	Write Sector	0	0	1	1	0	M	L	0
III	Format Track	0	1	0	1	0	0	0	0

R_3-R_0 = STEPPING RATES

$R_3R_2R_1R_0$	Winchester	Floppy
0 0 0 0	20 μsec	≈15 μsec
0 0 0 1	0.5 msec	1 mS
0 0 1 0	1.0 msec	2
0 0 1 1	1.5 msec	3
0 1 0 0	2.0 msec	4
0 1 0 1	2.5 msec	5
⋮	⋮	6
1 1 1 1	7.5 msec	6
		8
		8
		10
		12
		14
		16
		18
		20
		25
		40

D = DMA Read Mode

D = 0, Programmed I/O Mode
D = 1, DMA Mode

L = Read/Write Long

L = 0, Normal R/W Transfer
L = 1, R/W ECC Bytes from Host

M = Multiple Sector

M = 0, Single Sector R/W
M = 1, Multiple Sector R/W

TYPE I COMMANDS

These commands simply position the R/W heads of the selected drive. Both commands have explicit stepping rate fields. The lower four bits of these commands form the stepping rate.

Restore

The Restore command is used to move the R/W heads to the Track 0 position. It is usually performed after a power-up operation. When Restoring a Winchester drive, the specified stepping rate is not used; the actual Restore rate is handshaked with Seek Complete Time. When Restoring on a floppy drive, the R_3-R_0 rate is used when the rate is equal to or slower than 8 mS. On rates faster than 8 mS, the restore stepping rate defaults to 8 mS. On both floppy and Winchester, the rate is stored for subsequent implied Seeks for Read/Write commands.

Seek

The Seek command is used to position the Read/Write heads to a specified location. Since the Read and Write commands feature implied Seek, this command is normally used to perform simultaneous (overlap Seek) operations on multiple drives. The specified stepping rate is used for Track to Track access time.

The desired location is loaded into the cylinder registers prior to issuing the command. On Winchester drive, the Write Fault, Seek Complete, and Ready lines must be true for the command to execute. The Seek Complete line is not checked after all stepping pulses have been issued. A Seek operation on a floppy drive will be performed regardless of the state of Write Protect on the Drive Interface.

TYPE II COMMANDS

This type of command is characterized by a transfer of a block of data from the WD1002-05 buffer to the host. This command has an implicit stepping rate as set by the last Restore or Seek command.

Read Sector

The Read Sector command is used to transfer a specified sector from any drive to the Host buffer. The stepping rate, specified in an earlier Restore or Seek command, is used to automatically perform a Seek prior to execution of the Read. After the task file has been loaded with the desired parameter, the on-board sector buffer is filled with the data from the disk. The Host may then read this data by accessing the data register repeatedly.

The 'D' Flag allows the Interrupt line (INTRQ) to be activated when the data is available. The Data Request signal is always activated when the WD1002-05 either needs data (in the case of the Write commands) or has data available for the Host. If the 'D' Flag is not set, then the INTRQ will be activated before start of data transfer. If set, then INTRQ will be set after the last byte of the last sector has been transferred to the host.

The 'L' Flag allows the Host to both Read and Write and ECC polynomial to a Winchester drive. This function may be used for diagnostic and performance purposes by allowing the Host to compute and check ECC operation. Since the floppy disk format does not allow ECC, the 'L' Flag is a "don't care" bit in this case.

The 'M' Flag allows multiple sectors to be transferred via one command. The Sector Count register in the task file is used to specify the number of sectors to be transferred from a track. Retries and ECC correction (if applicable) will be performed on each sector.

Write Sector

The Write Sector command is used to transfer a block of data from the on-board buffer to a specified sector. After the command is issued, the WD1002-05 generates a DRQ and the Host proceeds to fill the buffer. Once filled, the desired sector is searched for. This may include an implied Seek. After the ID field is found the Write Gate signal is activated and the data is MFM encoded and written serially to the selected drive. The Write Precompensation Register in the task file specifies the starting cylinder on a Win-

chester drive where precomp is to be enabled. The WFC is configured with no precompensation when writing to the floppies. The user may cut the etch on WD2797 pin 1 so that precomp is always enabled or jumper it to pin 29 so that precomp is enabled for tracks greater than 43.

The option Flags 'L' and 'M' are also available and work exactly as described in the Read Sector command.

TYPE III COMMANDS

Format Track

This command is used to format a drive prior to reading or writing. It causes ID fields, gaps, and all information to be written to a selected Track for initialization. The on-board sector buffer serves a different purpose for this command; it contains the Bad Block Flag and the physical numbers of the sectors to be recorded. Since the actual sector numbers are now taken from the buffer, unlimited Interleaving is allowed. The Sector Count register in the task file, normally used during a multiple sector R/W, now specifies the number of sectors to be formatted. The Format Track command also features the implied Seek option, so that the entire drive can be formatted by incrementing the cylinder number after each execution.

SETTING UP TASK FILES

Before any of the five commands may be executed, a set of parameter registers called the Task File must be set up. For most commands, this informs the WD1002-05 of the exact location on the disk that the transfer should take place. For a normal read or write sector operation, the Sector Number, the Size/Drive/Head, Cylinder Number, and Command registers (usually in that order) will be written.

Note that most of these registers are readable as well as writable. These registers normally are not read from, but this feature is provided so that error reporting routines can determine physically where an error occurred without recalculating the sector, head and cylinder parameters.

Since the WD1002-05 can recall all the Task File parameters sent to it, it is recommended that Task File parameters be stored in the WD1002-05 as they are calculated. This will save the programmer a few instructions by not maintaining two copies of the same information.

Since most hard disk drives contain more than one head per positioner, it is more efficient to step the R/W head assemblies of most disk drives by cylinders, not tracks. In other words, the disk driver software should be designed to read or write all data that is directly accessible by all the heads on a positioner before stepping to a new cylinder.

REGISTER SELECTION ARRAY

CS	A2	A1	A0	RE	WE
1	X	X	X	Deselected	Deselected
0	0	0	0	Data Register	Data Register
0	0	0	1	Error Register	Write Precomp*
0	0	1	0	Sector Count	Sector Count
0	0	1	1	Sector Number	Sector Number
0	1	0	0	Cylinder Low	Cylinder Low
0	1	0	1	Cylinder High**	Cylinder High**
0	1	1	0	Size/Drive/Head	Size/Drive/Head
0	1	1	1	Status Register	Command Register

*Not used on Floppy

**When LSB = 1, permits 48 t.p.i. Floppy disk to be read on 96 t.p.i. Floppy disk system.

SDH REGISTER								
BIT	7	6	5	4	3	2	1	0
Function	Sec Ext	Sec Size		Drive Select		Head/ Drive Select		

BIT 7	SECTION EXTENSION (WINCHESTER ONLY)
0	Selects CRC for data field
1	Selects ECC for data field

BIT 6	BIT 5	SECTOR SIZE
0	0	256 Bytes
0	1	512 Bytes
1	0	1024 Bytes
1	1	128 Bytes

BIT 4	BIT 3	DRIVE SELECTED
0	0	Winchester Drive Sel 1
0	1	Winchester Drive Sel 2
1	0	Winchester Drive Sel 3
1	1	Floppy Drive Sel

BIT 2	BIT 1	BIT 0	WIN-CHESTER HEAD NR	FLOPPY DRIVE & HEAD NRS
0	0	0	0	DR1 HD0
0	0	1	1	DR1 HD1
0	1	0	2	DR2 HD0
0	1	1	3	DR2 HD1
1	0	0	4	DR3 HD0
1	0	1	5	DR3 HD1
1	1	0	6	DR4 HD0
1	1	1	7	DR4 HD1

STATUS & ERROR REGISTERS

The Status Register is used to monitor command flow and to supply the Host with specific information about the drive. A bit called "Busy" (Bit 7) indicates that the WD1002-05 is executing a current command and register access is prohibited. This bit can be read at any time by the host but all other bits are invalid when this status bit is set.

The Error Register is used to report different types of errors caused by execution of the last command. To ease programming, the LSB of the STATUS register will be set if any of the bits in the error register are also set.

STATUS AND ERROR REGISTER BITS

BIT	STATUS REGISTER	ERROR REGISTER
7	Busy	Bad Block Detect
6	Ready	ECC/CRC Error Data Field
5	Write Fault	—
4	Seek Complete	ID Not Found
3	Data Request	—
2	Corrected Data	Aborted Command
1	—	TR000 Error
0	Error	DAM Not Found

SPECIFICATIONS:

	HARD DISK	FLOPPY DISK
Encoding method:	MFM	MFM
Cylinders per Head:	Up to 1024	Up to 245
Sectors per Track:	Up to 64	Up to 64
Heads:	8	2
Drive Selects:	3 (ST506)	4 (SA450)
Step Rate:	35 μS to 7.5 mS (0.5 mS increments)	0-40 mS (1 of 16 rates in this range)
Data Transfer Rate:	5.0 Mbits/sec	250 Kbits/sec
Write Precomp Time:	12 nsec	100-300 nsec adj.
Sectoring:	Soft	
Host Interface:	8 Bit bi-directional bus	
Drive Cable Length:	10 ft (3M) max.	
Host Cable Length:	3 ft (1M) max.	
Power Requirements:	+5V ± 5%, 3.0A Max.	
Ambient Temperature Operating:	0°C to 50°C (32°F to 122°F)	
Relative Humidity:	20% to 80%	
MTBF:	10,000 POH	
MTTR:	30 minutes	
Length:	8.00 in	
Width:	5.75 in	
Height:	0.75 in	
Mounting Centers:	7.50 X 5.250 in	

This is a preliminary specification with tentative device parameters and may be subject to change after final product characterization is completed.

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PRELIMINARY

WD1002-SHD Winchester Disk Controller

FEATURES

- SINGLE +5V SUPPLY
- SASI™ HOST INTERFACE
- CONTROL FOR UP TO 2 WINCHESTER DRIVES, UP TO 8 R/W HEADS EACH
- 32 BIT ECC FOR WINCHESTER DATA CORRECTION
- DIAGNOSTIC READS AND WRITES FOR CHECKING ERROR CORRECTION
- BAD TRACK MAPPING CAPABILITY
- AUTOMATIC FORMATTING
- 256 OR 512 BYTES PER SECTOR
- SELECTABLE INTERLEAVE
- MULTIPLE SECTOR READS AND WRITES
- BUILT-IN DATA SEPARATOR
- BUILT-IN WRITE PRECOMPENSATION
- OVERLAPPED SEEKS
- IMPLIED SEEKS
- 0°C to 55°C OPERATIONS

DESCRIPTION

The WD1002-SHD is a stand alone, general purpose Winchester Controller Board designed to interface up to two Winchester Disk Drives to a Host Processor. The Winchester Drive signals are based upon the Floppy look-alike interface available on the Seagate Technology ST506 and other compatible drives. All necessary receivers and drivers are included on the board to allow direct connection to the drive.

Communications to and from the Host Computer are made via a separate computer access port. This port conforms to the popular Shugart Associates System Interface (SASI). It consists of control signals and an 8-bit bi-directional bus. All data to be written to or read from the disk, status information, and command parameters are transferred via this bus. An on-board Data Buffer allows bus transfers to be executed independently of the actual Data Transfer of the drive.

The WD1002-SHD is based upon the WD1010, and WD1100-13, specifically designed for Winchester disk drive control.

SASI™ is a trademark of Shugart Assoc.

ARCHITECTURE

The WD1002-SHD has five on-board interface connectors. Other connectors are for test only and should not be used.

The five connectors consist of a Power Connector, Host Interface Connector, Winchester Drive Control Connector and Two Winchester Data Cable Connectors.

The Winchester Drive Control Cable is daisy-chained to the drive. The drive Data Connectors carry differential signals and are radially connected.

The Host Interface Connector provides a path to the Host thru a SASI bus. Other SASI-Compatible controllers may also be connected to the same bus.

SPECIFICATIONS:

DRIVE INTERFACES

Encoding Method	MFM
Cylinders per Drive	Programmable
Bytes per Sector	Selectable, 256 or 512
Sectors per Track	32 (256 bytes/sector) 17 (512 bytes/sector)
Head Selects	8
Drive Selects	2
Stepping Rates/Algorithms	Programmable
Data Transfer Rate	5Mbits/sec
Write Precomp Time	12 nsec
Sectoring	Soft
Max Cable Length	
Control (Total Daisy Chain)	6M (20ft.)
Data (Radial — each)	6M (20ft.)

HOST INTERFACE

Type	SASI
Max Cable Length (Total Daisy Chain)	4.5M (15ft.)
Termination	Socketed 220/330 pack
Addressing	Jumperable, 0 to 7

POWER

Voltage	5V + 5%
Current	2.0A Max, 1.5A TYP
Ripple	.1 volts max, .1 to 25MV

MECHANICAL

Length	8″
Width	5.75″
Height (Max incl leads, board, & components)	.75″

ENVIRONMENTAL — OPERATING

Ambient Temperature	0° to 55°C
Relative Humidity	10% to 90% condensing
Altitude	0 to 3000M (10,000 ft)

CONNECTORS

MECHANICAL INFORMATION

Table 1 defines the connectors and a source for the mating connectors on the associated cables. The connector locations may be found in figure XX.

Table 1. CONNECTORS

REFERENCE DESIGNATION	INTERFACE FUNCTION	EQUIVALENT MATING CONNECTOR
P1	Power	AMP1-480424-0 (Housing) AMP350078-4 (Pins) AMP88379-8
P2	SASI Bus	
J1	Winchester Control (Daisy-Chain)	AMP88373-3
J2, J3	Winchester Data (Radial)	AMP88377-4
J4	Test — do not use	

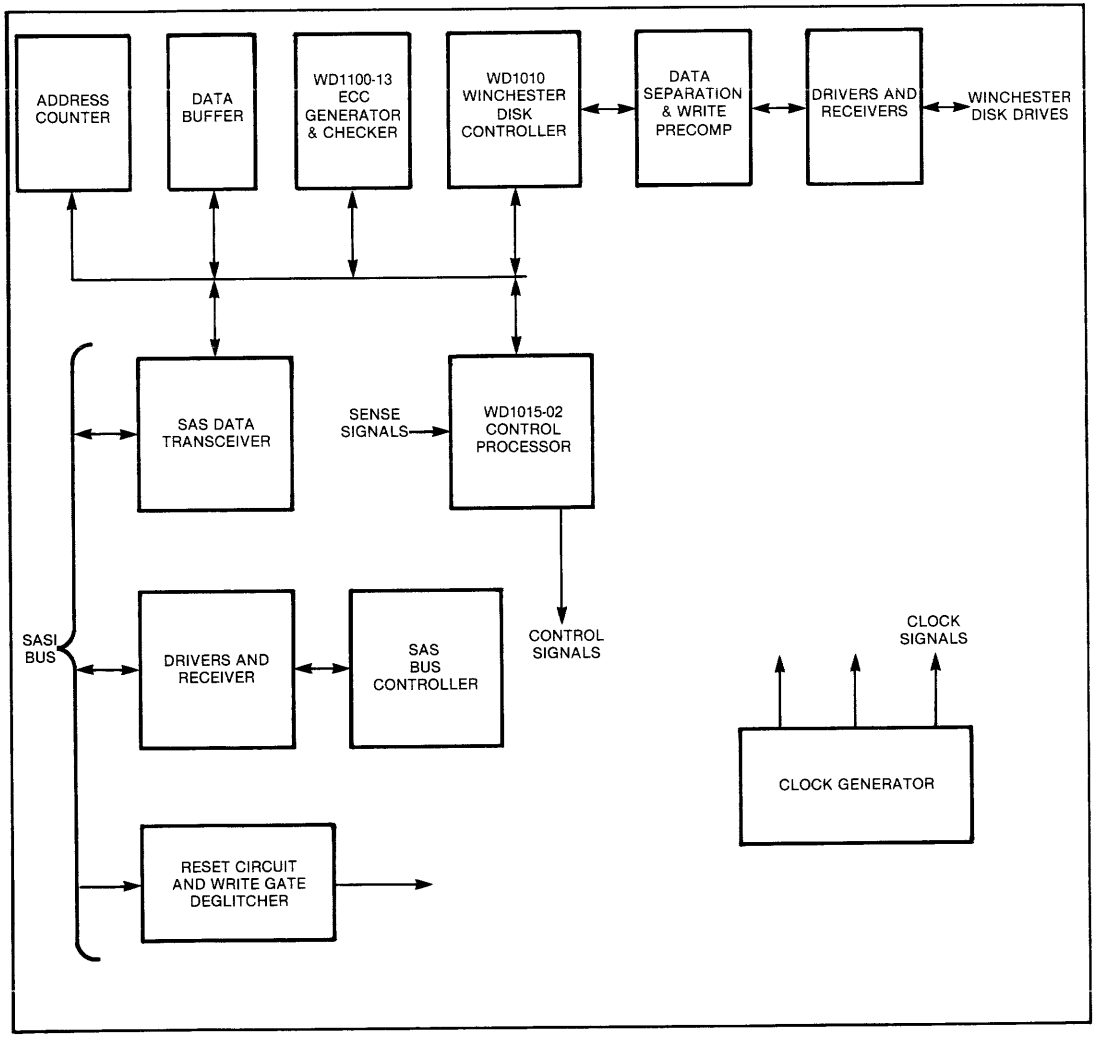


Figure 1. WD1002-SHD BLOCK DIAGRAM

HOST INTERFACING

The WD1002-SHD Controller has been designed to interface to the Shugart Associates System Interface (SASI) bus. All interfacing is done through the SASI connector (P2). Up to eight SASI compatible devices (including the Host) may be connected to this bus. The cable terminating resistor pack is socketed on the controller to aid flexibility in daisy-chaining bus devices. The controller is shipped from the factory configured to respond to SASI device address 0. This may be changed by the user to any SASI address (0 through 7).

HOST INTERFACE CONNECTOR

The host interface connector is a 50 pin vertical header. The connector pin-outs are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME	DESCRIPTION
1	2	$\overline{\text{DATA 0}}$ (LSB)	Bi-directional bytewide bus bits $\overline{\text{D0-D7}}$.
3	4	$\overline{\text{DATA 1}}$	
5	6	$\overline{\text{DATA 2}}$	
7	8	$\overline{\text{DATA 3}}$	
9	10	$\overline{\text{DATA 4}}$	
11	12	$\overline{\text{DATA 5}}$	
13	14	$\overline{\text{DATA 6}}$	
15	16	DATA 7 (MSB)	
17	18	SPARE	
19	20	SPARE	
21	22	SPARE	
23	24	SPARE	
25	26	SPARE	
27	28	SPARE	
29	30	SPARE	
31	32	SPARE	
33	34	SPARE	
35	36	$\overline{\text{BUSY}}$	Controller-to-host signal whose falling edge acknowledges receipt of $\overline{\text{SEL}}$ and own address. Rising edge indicates transaction complete.
37	38	$\overline{\text{ACK}}$	Host-to-controller handshake for byte transfers (both edges used).
39	40	$\overline{\text{RST}}$	100 nsec low level initiate (host-to-controller).
41	42	$\overline{\text{MSG}}$	Controller-to-host $\overline{\text{MESSAGE}}$ signal to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
43	44	$\overline{\text{SEL}}$	Host-to-controller low level signal gives control of bus to address target.
45	46	$\overline{\text{C/D}}$	Controller-to-host $\overline{\text{COMMAND}}$/DATA signal used to indicate type of bus transfer (see INFORMATION TRANSFER PHASE).
47	48	$\overline{\text{REQ}}$	Controller-to-host handshake for byte transfers (both edges used).
49	50	$\overline{\text{I/O}}$	0 = $\overline{\text{INPUT}}$ to host. 1 = $\overline{\text{OUTPUT}}$ from host. (see INFORMATION TRANSFER PHASE)

WINCHESTER DRIVE CONTROL CONNECTOR

The drive control connector is a 34 pin PC card edge connector that provides a low speed bus that is daisy chained to each of the Winchester drives in the system. To properly terminate the open collector outputs from the WD1002-SHD, the last drive in the daisy chain should have a 220/330 ohm line termination resistor pack installed. No other drives should have this termination. The drive control signals and pin-outs are as follows:

SIGNAL GROUND	SIGNAL PIN	SIGNAL NAME (I/O)	DESCRIPTION
1	2	$\overline{RWC}$ (O)	When the Reduce Write Current ($\overline{RWC}$) line is activated by Write Gate ($\overline{WG}$), a lower write current is used to compensate for a greater bit packing density on the inner cylinders. $\overline{RWC}$ is only valid when $\overline{WG}$ is low.
3 13 17	4 14 18	$\overline{HS2}$ (O) $\overline{HS0}$ (O) $\overline{HS1}$ (O)	Head Select lines are used by the WD1002-SHD to select a specific R/W head on the drive.
5	6	$\overline{WG}$ (O)	Write Gate ($\overline{WG}$) enables data to be written on the disk. Special circuitry has been included to ensure that this signal will not "glitch" at power-on. This enables the disk drive to remain powered on while the WD1002-SHD power is being cycled.
7	8	$\overline{SC}$ (I)	Seek Complete ($\overline{SC}$) informs the WD1002-SHD that the head of a selected drive has stabilized.
9	10	$\overline{TR000}$ (I)	Track 000 ($\overline{TR000}$) indicates that the R/W heads are positioned on the outermost cylinder.
11	12	$\overline{WF}$ (I)	Write Fault ($\overline{WF}$) informs the WD1002-SHD that some fault has been detected by the selected drive.
15	16		NC
19	20	$\overline{IND}$ (I)	Index ($\overline{IND}$) indicates the index point for synchronization during formatting. $\overline{IND}$ is also used as a time-out mechanism for retries. $\overline{IND}$ should pulse once for each disk rotation.
21	22	$\overline{RDY}$ (I)	Ready ($\overline{RDY}$) informs the WD1002-SHD that the desired drive is selected and its motor is up to speed.
23	24	$\overline{STEP}$ (O)	$\overline{STEP}$ is pulsed for each desired step. The direction of the step is determined by the $\overline{DIRIN}$ line.
25 27	26 28	$\overline{DS0}$ $\overline{DS1}$	The Drive Select bits ($\overline{DS0}$-$\overline{DS1}$) are used to select either drive 1 or drive 2.
29	30		NC
31	32		NC
33	34	$\overline{DIRIN}$	Direction In ($\overline{DIRIN}$) determines the direction of movement of the R/W heads when $\overline{STEP}$ is pulsed: $\overline{DIRIN}$ = 1 = direction out $\overline{DIRIN}$ = 0 = direction in

WINCHESTER DRIVE DATA CONNECTOR

Two data connectors are provided for data transfer between the controller and each drive. All lines associated with the transfer of data between the drive and the controller are differential in nature and may not be multiplexed. The data connectors are 20 pin vertical headers on tenth-inch centers. The cable pinouts are as follows:

SIGNAL GROUND	SIGNAL PIN	(I/O)	SIGNAL NAME
2	1	I	Drive Selected
4	3	—	NC
6	5	—	NC
8	7	—	NC
10	9	—	NC
12	11	—	GND
	13	O	+ MFM Write Data
	14	O	− MFM Write Data
16	15	—	GND
	17	I	+ MFM READ DATA
	18	I	− MFM READ DATA
20	19	—	GND

POWER CONNECTOR

A four pin AMP connector is provided for power input to the board. The pin-outs are as follows:

PIN	SIGNAL
1	NC
2	GROUND
3	GROUND
4	+ 5 V regulated

HOST INTERFACE DETAILED BUS OPERATION

With regard to bus operations, time can be partitioned into the following mutually exclusive phases:

1. Reset
2. Bus Free
3. Target Selection
4. Information Transfer
5. Bus Release

Bus Phase Sequencing

A Reset Phase may occur at any time. It is followed by the Bus Free Phase. In the absence of a Reset Phase, the bus alternates between the Bus Free Phase and one Transaction.

A Transaction always consists of the following sequence:

1. one Target Selection Phase
2. one or more Information Transfer Phases
3. one Bus Release Phase

The five bus phases are described below. The Information Transfer Phase is broken down into its mutually exclusive categories, which are also called phases.

1. RESET PHASE

Defined as the time $\overline{\text{RESET}}$ is low. It is used by a host to force the controller(s) on the bus to the same state as that following a power on condition.

2. BUS FREE PHASE

Defined as the time between completion (Bus Release Phase) of one Transaction and initiation (Target Selection Phase) of the next Transaction. It can also be thought of as the time during which no unit has control of the bus. All eight control lines are high. The Data Lines are in an undefined state.

3. TARGET SELECTION PHASE

This phase begins when the host places a target address on the bus. The host then brings $\overline{\text{SEL}}$ low. The phase ends when the target corresponding to that address responds by bringing $\overline{\text{BUSY}}$ low. Note: the host must bring $\overline{\text{SEL}}$ high before completion of the current Transaction (end of next Bus Release Phase).

The target address consists of one of $\overline{\text{D0}}$ through $\overline{\text{D7}}$ low and the other seven high. The controller's default address corresponds to $\overline{\text{D0}}$ low. It may be changed to any address by jumpering. Two controllers may not have the same address.

4. INFORMATION TRANSFER PHASE

This phase is used to transfer one or more bytes over the bus. It begins when the currently selected controller sets $\overline{\text{I/O}}$, $\overline{\text{C/D}}$, and $\overline{\text{MSG}}$ to one of the five legal combinations in the following table. This indicates to the host the type of byte transfer(s) which will follow.

$\overline{\text{I/O}}$	$\overline{\text{C/D}}$	$\overline{\text{MSG}}$	TYPE OF TRANSFER PHASE	NUMBER OF BYTES
1	0	1	Command Block (from host)	6
1	1	1	Data Block (from host)	3, 8, 256, 260, 512 or 516
0	1	1	Data Block (to host)	1, 4, 256, 260, 512 or 516
0	0	1	Status Byte (to host)	1
0	0	0	Message Byte (to host)	1

For each byte transferred, the following operations must occur in sequence to perform the asynchronous handshake.

1. The controller brings $\overline{REQ}$ low
2. The host brings $\overline{ACK}$ low
3. The controller brings $\overline{REQ}$ high
4. The host brings $\overline{ACK}$ high

For controller to host transfers, the eight bits are valid on the bus at least 125 nsec before $\overline{REQ}$ goes low. For host to controller transfers, they must be valid on the bus no later than 375 nsec after $\overline{ACK}$ goes low. Note: for debugging, it is useful to know that bytes are valid on the bus at the rising edge of $\overline{REQ}$ during any transfer.

The Command Block Transfer Phase is used to send a block of parameters to the controller. This block specifies the operation to be performed (e.g. Format Disk).

The Data Transfer Phase is primarily used to send one or more sectors of data (with or without ECC) in either direction. It is also used to send an extra block of parameters to the controller or to send byte(s) of controller operational information to the host. During the Status Transfer Phase, byte(s) are sent to the host. They are encoded to indicate the nature of errors that may have been detected.

During the Message Byte Transfer Phase, one byte of all zeroes is sent to the host. This is necessary to satisfy the protocol.

5. BUS RELEASE PHASE

This phase is simply the low-to-high transition of $\overline{BUSY}$. This event signifies to the host that the current Transaction has terminated and the associated target is no longer controlling the bus.

Now in more detail, a transaction always consists of the following sequence:

a. One Target Selection Phase
b. One Command Block Transfer Phase
c. Zero or more Data Block Transfer Phase(s) (type and number determined by the preceding Command Block parameters)
d. One Status Byte Transfer Phase
e. One Message Byte Transfer Phase
f. One Bus Release Phase

During a transaction, all Data Block Transfer Phases are in the same direction and of the same size.

COMMAND BLOCKS

A transaction is initiated by the host to instruct the controller to execute a command. During the Command Block Transfer Phase, six bytes of information specifying the command are transferred to the controller. There is a specific format for these bytes, shown in figure below.

	BITS							
BYTE	7	6	5	4	3	2	1	0
0	Command Class			OP Code				
1	Logical Unit Number			Logical Sector Address (high)				
2	Logical Sector Address (Middle)							
3	Logical Sector Address (Low)							
4	Interleave or Block Count							
5	Control Byte							

Byte 0 is transferred first. Byte 0 must be specified for all commands. Each command has exactly one Byte 0 value associated with it.

Depending on the value of Byte 0, each parameter in Bytes 1 through 5 may require specification. Table specifies the supported commands and their parameters. It also includes information in data transfers required during execution. All other commands are reserved.

LOGICAL UNIT NUMBER (LUN)

This is contained in the upper three bits of Byte 1. The allowed values are 0, 1. The designators in the Command Table are:

Drive 0 (LUN 0) or 1 (LUN 1)

LOGICAL SECTOR ADDRESS (L)

This is a 21 bit field contained in Bytes 1, 2, and 3. It is computed from the Cylinder (C), Head (H), and Sector (S) address, as well as the drive parameters, heads per drive (HD) and Sectors per track (ST):

$$L = (((C * Hd) + H) * ST) + S$$

C, H and S can be derived from L, HD, and ST as follows:

$$S = L \text{ Modulo } ST$$
$$H = ((L-S)/ST) \text{ Modulo } HD$$
$$C = (((L-S)/ST) - H)/HD$$

This field specifies a sector (or a beginning sector) for the Read and Write Drive commands. It specifies a track for the Format and Seek commands (marked with a * in the table). When only a track specification is required, the sector number implied by the Logical Sector Address is ignored.

INTERLEAVE OR BLOCK COUNT

This field makes up Byte 4. The Interleave Ratio (I) is specified in the Five Format commands. The maximum ratio is the sectors-per-track minus 1.

The Block Count (B) is specified in the Read, Write, Read Long, and Write Long commands. It specifies the number of Logical Sectors to be transferred.

Both Interleave Ratio and Block Count use all 8 bits to specify the parameters.

CONTROL BYTE

This Byte is broken into the following fields:

FIELD	BIT(s)	FUNCTION
S	0-3	Used in all commands which may cause an explicit seek. Contains a code corresponding to a seek stepping algorithm. See Device Control Block (Fast Step Options).
U	4	Reserved. Unused.
P	5	Used in the format commands. If 0, fill data fields with hex 6C. If 1, fill with the pattern in the sector buffer.
A	6	Used in the Read Drive command with LUN indicating Winchester. Normally 0. If 1, do not re-read before attempting error correction.
R	7	Used in all commands which will cause an ID field to be read. Normally 0. If 1, Disable retries.

NOTE:
If one or more of the above fields are required to be specified for a command, then all the other fields in that control byte must be set to zero. If none are required, all eight bits are interpreted as "don't cares."

WD1002-SHD DEVICE CONTROL BLOCK

FAST STEP OPTIONS

The fast step option field contains an unsigned 3-bit integer. These integers correspond to the following fast step algorithms:

OPTION	
0	Default: 3 milliseconds per step
1	Half-step for Seagate & Texas Instrument drives
2	3 Msec
3	3 Msec
4	200 microseconds per step. This is appropriate for buffered steps on drives made by Computer Memories, Inc. and Rotating Memories, Inc.
5	70 microseconds per step.
6	30 microseconds per step.
7	15 microseconds per step.
8	2 milliseconds per step.
9	3 Msec
B-F	Spare (3 Msec)

COMMAND STATUS BYTE

BITS	
0	0
1	Error flag: 0 → no error 1 → error
2	0
3	0
4	0
5-7	Logical unit number

At the completion of execution of each command a command status byte is sent by the WD1002/SHD to the host to indicate to the host whether or not the command was successful.

The logical unit number returned is simply the contents of the logical unit field in the drive control block. For those commands that do not take a logical unit number as an input parameter, the logical unit number returned in the command status byte is not meaningful.

COMMAND COMPLETION BYTE

The command completion byte is an all zero byte sent by the WD1002/SHD to the host immediately following each command status byte. It indicates to the host that the WD1002/SHD has freed the SASI bus.

COMMANDS

Each command is briefly described below.

1. TEST DRIVE READY (CLASS 0, OPCODE 1)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, invalid command, no seek complete, drive not ready, no index pulses, write fault.

Action

Select the drive and determine whether or not it is ready.

For a Winchester drive, read its status register and test the ready bit and busy bit. For Winchester drives supporting buffered seeks this command is useful for determining the first drive to reach its target track.

2. RECALIBRATE (CLASS 0, OPCODE 1)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5	Control field Bit 7 Bit 6 — Immediate ECC: 0 → no immediate correction Bit 4 — Reserved for future use. Must be zero. Bit 5 — Format data. Bits 0-3	don't care 0 0 0 don't care

Possible Error Codes

No error, invalid command. Track 0 not found, drive not ready, write fault.

Action

Position the heads to cylinder 0.

3. REQUEST STATUS (CLASS 0, OPCODE 3)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 3
1	Bits 5-7 = Logical unit number Bits 0-4	 don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, invalid command.

Action

Send the host the error byte and a 3-byte logical sector address for the specified drive.

The following non-drive error codes are treated as drive 0 errors: RAM failure (30.), ROM failure (31.), ECC failure (32.). Hence, if command RAM diagnostic or command controller diagnostic detects an error, then status for drive 0 should be requested.

Error Byte

BITS	
7	Logical sector address flag: 0 → sector address not valid 1 → sector address valid
6	Not used. Set to 0.
0-5	Error codes

Logical Sector Address

BYTE	
0	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21
1	Logical sector address bits 8-15
2	Logical sector address bits 16-23

If the most recent non-request-status command to the specified drive required a logical sector address, then the logical sector address flag is 1; else, it is 0. If the logical sector address flag is 0, then the logical sector address is not meaningful.

If there was an error on the immediately preceding command and the logical sector address flag is 1, then the logical sector address indicates the sector or track on which the error occured. If the command was a format type command, then the logical sector address indicates the track; else, it indicates the sector.

If there was no error on the immediately preceding command and the command was a format type command, then the logical sector address indicates the track one beyond the last track accessed.

If there was no error and the command was not a format type command, then the logical sector address indicates the last sector accessed.

3A. ERROR CODES

Disk Drive Error Codes

0 No error
1 No index pulses
2 No seek complete
3 Write fault
4 Drive not ready
6 Track 0 not found

Controller Error Codes

10/14 Not used because WD1010 bumps CRC with several other errors in an I.D. field as errors not found.
11 Uncorrectable data error
12 Address mark not found
15 Seek error
18 Error burst corrected
19 Bad track

1A Format error
1C Illegal (direct) access to an alternate track
1D Alternate track already used
1E Alternate track not marked as alternate
1F Alternate track equals bad track

Command Error Codes

20 Invalid command
21 Invalid sector address

Miscellaneous Error Codes

30 RAM failure
31 ROM failure
32 ECC hardware failure

3B. ERROR CODE DESCRIPTIONS

No Seek Complete (2)

This error code is only returned by the test drive ready command when the target drive is a Winchester that supports buffered seeks. It indicates that drive is busy doing a buffered seek.

Write Fault (3)

Indicates that there was write current to the head when write the write gate was off. This is a very serious problem and should be fixed immediately.

Track 0 Not Found (6)

This error code is only returned by the recalibrate command. It indicates that the track 0 status from the drive did not become active after the maximum necessary steps towards cylinder 0.

Uncorrectable Data Error (11)

For a Winchester drive this error code indicates one or more error bursts in the data field were beyond the error correction code's ability to correct. The sector data for the sector in error is not sent to the host.

Address Mark Not Found (12)

Indicates that the header for the target sector was found, but its address mark was not detected.

Error Burst Corrected (18)

Indicates that the error correction code (ECC) was used to successfully correct an error. The corrected sector data is sent to the host. This is the only error condition for which sector data is sent to the host.

Bad Track (19)

This usually indicates access of a track that was formatted as a bad track. However, there is a very small chance that it indicates that a track formatted as a bad track with alternate is so faulty that none of the multiple, duplicate pointers to the alternate track can be read.

Format Error (1A)

This error code is returned by the check track format command. It indicates that the track is not formatted, the track is not formatted with the specified interleave factor, or at least one sector header is unreadable.

This error code is returned by drive diagnostic to indicate that a bad-track-with-alternate does not contain a valid pointer to the alternate track.

Alternate Track Already Used (1D)

This error code is only returned by the format alternate track command. It indicates that the specified alternate track is already an alternate or bad track.

Alternate Track Not Marked As An Alternate (1E)

This error code indicates that access of a bad-track-with-alternate caused access to an alternate track which was not marked as an alternate track.

Alternate Track Equals Bad Track (1F)

This error code is only returned by the format alternate track command. It indicates that the same track was specified as the bad track and the alternate track.

Invalid Command (20)

This error code indicates that the command class, command code, logical unit number, interleave factor, or fast step number were invalid.

ROM Failure (30)

This error code indicates one of the following conditions: (1) The program memory ROM checksum does not match the calculated checksum. (2) The RAM in the microprocessor failed. (3) The microprocessor CPU failed.

4. FORMAT DRIVE (CLASS 0, OPCODE 4)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 4
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, write fault.

Action

Format from the specified track to the end of the disk. The previous contents of the formatted tracks are ignored.

5. CHECK TRACK FORMAT (CLASS 0, OPCODE 5)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 5
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0

5. CHECK TRACK FORMAT (Continued)

BYTE		CONTENTS
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, seek error, format error, drive not ready, write fault.

Action

Verify that the specified track is formatted with the specified interleave factor. Do not read the sector data fields.

6. FORMAT TRACK (CLASS 0, OPCODE 6)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 6
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, write fault.

Action

Format the specified track. The current contents of the specified track are ignored.

7. FORMAT BAD TRACK (CLASS 0, OPCODE 7)

The WD1002-SHD writes the data fields.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 7
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7	don't care
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, write fault.

Action

Format the specified track with a bad block mark in each sector header. The previous contents of the specified track are ignored. The contents of a bad track are not accessible.

8. READ (CLASS 0, OPCODE 8)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 8
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction 1 → immediate correction	
	Bit 5 — Format data	0

8. READ (CLASS 0, OPCODE 8) (Continued)

BYTE		CONTENTS
	Bit 4 — Reserved for future use. Must be zero. Bits 0-3 = Fast step option integer	0

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, error burst corrected, uncorrectable data error, write fault.

Action

Read the specified number of consecutive sectors beginning with the specified sector.

9. WRITE (CLASS 0, OPCODE 0A)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0A
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

Write the specified number of sectors beginning with the specified sector.

10. SEEK (CLASS 0, OPCODE 0B)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0B
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4		don't care
5	Control field	don't care
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, write fault.

Action

Move the read/write head to the specified cylinder. Do not read any sector header to verify start or end position.

11. SET PARAMETERS (CLASS 0, OPCODE 0C)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0C
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

If parameters out of range, "INVALID COMMAND."

Action

Set the following parameters for both of the Winchester drives (logical units 0 and 1): Number of cylinders, number of heads, starting reduced write current cylinder, starting write precompensation cylinder, and the maximum length of an error burst to be corrected. These parameters are sent by the host to the WD1002/SHD in a parameter block with the following format:

Parameter Block

BYTE	
0	Most significant byte of number of cylinders
1	Least significant byte of number of cylinders
2	Bits 4-7. Must be 0. Bits 0-3 = Number of heads
3	Most significant byte of starting reduced write current cylinder
4	Least significant byte of starting reduced write current cylinder
5	Most significant byte of starting write precompensation cylinder
6	Least significant byte of starting write precompensation cylinder
7	Bits 4-7. Must be 0. Bits 0-3 = Maximum length of an error burst to be corrected

Power up and reset set these parameters to the following defaults:

153. = Number of cylinders
4 = Number of heads
128. = Starting reduced write current cylinder
64. = Starting write precompensation cylinder
11. = Maximum length of an error burst to be corrected

The acceptable range of values for these parameters are as follows:

1 — 1024. Number of cylinders
1 — 8 Number of heads
0 — 1023. Starting reduced write current cylinder
0 — 1023. Starting write precompensation cylinder
1 — 11. Maximum length of error burst to be corrected.

If one of the parameters is out of range, then all parameters up to but not including the parameter in error are set for drive 0 and no parameter for drive 1 is set. The error code for this error is "invalid command."

Starting Reduced Write Current Cylinder

The specified starting reduced write current cylinder number is rounded down to the nearest integer multiple of four. That is, the actual starting reduced write current cylinder numbers are 0, 4, 8, 12, . . . 1020.

Maximum Length of Error Burst To Be Corrected

For almost all applications the maximum length of error burst to be corrected should be about 5. Correcting longer bursts greatly increases the chances of miscorrecting.

12. LAST CORRECTED BURST LENGTH (CLASS 0, OPCODE 0D)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0D
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Send the host one byte of data containing the length of the most recently corrected error burst. If no error burst has been corrected since the last power up or reset, then a length of zero is sent to the host.

Error Burst Length Block

BYTE	
0	Number of bits in most recently corrected error burst.

13. FORMAT ALTERNATE TRACK (CLASS 0, OPCODE 0E)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0E
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Interleave factor	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data: 0 → hex 6C 1 → contents of sector buffer	
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, alternate track already used, alternate track equals bad track, write fault.

Action

Format the specified track as a bad-track-with-alternate. Format the specified alternate track with the specified interleave factor. The alternate track is specified by the host by sending an alternate sector address block to the WD1002/SHD after the DCB.

Alternate Sector Address Block

BYTE	
0	Bits 5-7. Must be 0. Bits 0-4 = Logical sector address bits 16-21
1	Logical sector address bits 8-15
2	Logical sector address bits 0-7

14. WRITE SECTOR BUFFER (CLASS 0, OPCODE 0F)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 0F
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Write data from the host to the WD1002/SHD sector buffer. The host must send as many bytes as there are in a sector on logical unit 0. This data is not written to any disk. This command is used to initialize the format data optionally used by the format commands.

15. READ SECTOR BUFFER (CLASS 0, OPCODE 10)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	0 10
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error.

Action

Send the host the current contents of the WD1002's sector buffer. The host must accept as many bytes as there are in a sector on logical unit 0.

16. RAM DIAGNOSTIC (CLASS 7, OPCODE 0)

The WD1002-SHD does not preserve the sector buffer.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 0
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, RAM failure.

Action

Test the sector buffer by writing and reading various patterns into it.

17. DRIVE DIAGNOSTIC (CLASS 7, OPCODE 3)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 3
1	Bits 5-7 = Logical unit number Bits 0-4	don't care
2		don't care
3		don't care
4		don't care

17. DRIVE DIAGNOSTIC (Continued)

BYTE		CONTENTS
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, drive not ready, seek error, format error, write fault.

Action

Recalibrate the target drive then scan ID on each track. This command does not write to the disk. Nor does it send any sector data to the host.

The effect of drive diagnostic is to verify that at least one sector header can be read on each track. It does not report an error when it encounters a track that has been formatted as a "bad track," "bad-track-with-alternate," or "alternate track."

18. CONTROLLER DIAGNOSTIC (CLASS 7, OPCODE 4)

The WD1002-SHD does not preserve the sector buffer.

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 4
1		don't care
2		don't care
3		don't care
4		don't care
5		don't care

Possible Error Codes

No error, ROM failure, RAM failure, ECC hardware failure.

Action

Calculate a checksum for the program ROM, test the microprocessor, the sector buffer, and the ECC hardware. This command does not access any disk drive.

19. READ LONG (CLASS 7, OPCODE 5)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 5
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

Read the specified number of consecutive sectors and their ECC bytes beginning with the specified sector. There are four bytes of ECC per sector. This command is only useful for diagnostic purposes.

20. WRITE LONG (CLASS 7, OPCODE 6)

BYTE		CONTENTS
0	Bits 5-7 = Command class Bits 0-4 = Operation code	7 6
1	Bits 5-7 = Logical unit number Bits 0-4 = Logical sector address bits 16-21	
2	Logical sector address bits 8-15	
3	Logical sector address bits 0-7	
4	Sector count	
5	Control field	
	Bit 7 — Retry disable: 0 → no disable 1 → disable	
	Bit 6 — Immediate ECC: 0 → no immediate correction	0
	Bit 5 — Format data	0
	Bit 4 — Reserved for future use. Must be zero.	0
	Bits 0-3 = Fast step option integer	

Possible Error Codes

No error, invalid command, invalid sector address, drive not ready, seek error, bad track, illegal (direct) access to an alternate track, alternate track not marked as alternate, address mark not found, write fault.

Action

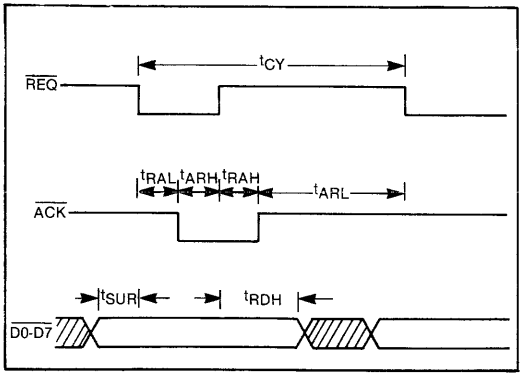
Write the specified number of consecutive sectors beginning with the specified sector. Following each sector the host sends four ECC bytes to the WD1002/SHD these are written to the disk as the ECC bytes for the sector.

This command is useful for diagnostic purposes. It allows the generation of a sector containing a correctable ECC error.

COMMAND NAME	CLASS + OP CODE	LUN	LOGICAL SECTOR ADDRESS	INTER-LEAVE OR BLOCK COUNT	CON-TROL BYTE OPTIONS	# OF SASI DATA BLOCK TRANSFERS	DATA BLOCK SIZE	DIRECTOR
Test Drive Ready	0,0	W	—	—	—	0	—	—
Restore To Track 0	0,1	W	—	—	R,S	0	—	—
Return Status	0,3	W	—	—	—	1	4	To Host
Format Drive	0,4	W	L*	I	R,P,S	0	—	—
Check Track Format	0,5	W	L*	I	R,S	0	—	—
Format Track	0,6	W	L*	I	R,P,S	0	—	—
Format Bad Track	0,7	W	L*	I	R,P,S	0	—	—
Read Drive	0,8	W	L	B	R,A,S	B	Sector	To Host
Write Drive	0,A	W	L	B	R,S	B	Sector	To CTLR
Seek	0,B	W	L*	—	R,S	0	—	—
Winchester Parameters	0,C	W	—	—	—	1	8	To CTLR
Return Burst Error Length	0,D	W	—	—	—	1	1	To Host
Format Alternate Track	0,E	W	L*	I	R,P,S	1	3	To CTLR
Write Sector Buffer	0,F	—	—	—	—	1	— Sector	To CTLR
Read Sector Buffer	0,10	—	—	—	—	1	— Sector	To Host
Perform RAM Diagnostics	7,0	—	—	—	—	0	—	—
Perform Drive Diagnostics	7,3	W	—	—	R,S	0	—	—
Perform Controller Diagnostics	7,4	—	—	—	—	0	—	—
Read Drive Long	7,5	W	L	B	R,S	B	— Sector +4	To Host
Write Drive Long	7,6	W	L	B	R,S	B	— Sector +4	To CTLR

LEGEND

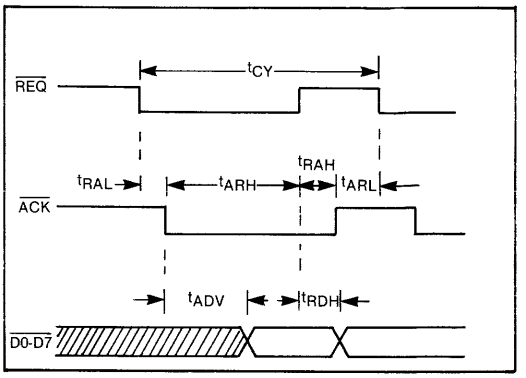
W Winchester
L* Logical sector address used only to specify track
I Interleave
B Block count
R Retry enable/disable
A Attempt immediate error correction enable/disable
S Stepping algorithm
P Used with format commands for determining data field pattern



CONTROLLER-TO-HOST TIMING

tXX	MIN*	MAX*
tCY**	1152	
tRAL†	0	
tARH	200	448
tRAH††	0	
tARL	200	848
tSUR	125	
tRDH	152	

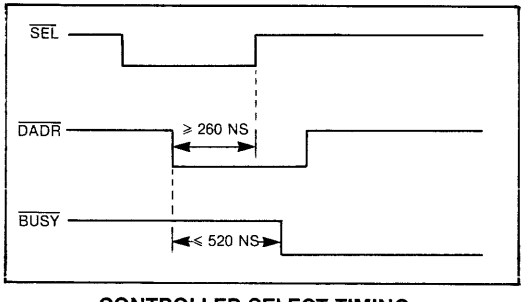
*nsec
**If conditions in † and †† are met, then tCYTYP = 1200 nsec and tCY max = 1248 nsec.
†If tRAL ⩽ 497 nsec, than no wait states are inserted.
††If tRAH⩽ 200 nsec, then no wait states are inserted.



HOST-TO-CONTROLLER TIMING

tXX	MIN*	MAX*
tCY**	1152	
tRAL†	0	
tARH	600	840
tRAH††	0	
tARL	200	448
tADV		375
tRDH	0	

*nsec
**If conditions in † and †† are met, then tCYTYP = 1200 nsec and tCY max = 1248 nsec.
†If tRAL ⩽ 89 nsec, than no wait states are inserted.
††If tRAH⩽ 97 nsec, then no wait states are inserted.



CONTROLLER SELECT TIMING

NOTE:
NO RESTRICTION ON SEQUENCE OF SEL AND DADR FALLING EDGES. BOTH MUST BE LOW TO ENSURE CONTROLLER SELECTION.

Printed in U.S.A.

PRELIMINARY

WD1002-MTB Multibus™ Winchester/Floppy Disk Controller

FEATURES

- ON-BOARD MICROPROCESSOR CONTROL
- MULTIBUS INTERFACE
- 16 BIT DATA BUS AND 24 BIT ADDRESSING
- DMA CONTROL
- SELF-TEST DIAGNOSTIC CAPABILITY
- INTERFACE COMPATIBLE WITH SEAGATE ST506/SHUGART SA450 TECHNOLOGY
- BUILT-IN DATA SEPARATOR/WRITE PRECOMP LOGIC
- DATA RATES UP TO 5 MBITS/SEC
- CONTROLS UP TO 2 WINCHESTER DRIVES AND 8 READ/WRITE HEADS PER DRIVE
- 1024 CYLINDER/256 SECTOR PER TRACK ADDRESSING RANGE
- CRC GENERATION/VERIFICATION ON ALL ID FIELDS
- DIAGNOSTIC READS AND WRITES FOR CHECKING ECC
- AUTOMATIC FORMATTING
- 128, 256, 512, AND 1024 BYTES PER SECTOR (USER SELECTABLE)
- UNLIMITED SECTOR INTERLEAVE CAPABILITY (INCLUDING INTERLEAVE FACTOR ONE)
- OVERLAP SEEK CAPABILITY
- IMPLIED SEEK ON ALL COMMANDS (ONLY IF DRIVE HAS BUFFERED SEEKS)
- PROGRAMMABLE STEP RATES FROM 7.5 mS TO 35 μS IN 500 μS INCREMENTS
- MULTIPLE SECTOR TRANSFERS (UP TO 65,535 SECTORS)
- AUTOMATIC TRACK/CYLINDER BOUNDARY CROSSING ON MULTI SECTOR TRANSFERS
- PROGRAMMABLE DISK PARAMETERS
- ECC 5 BIT CORRECTION ON ALL SECTORS, MULTIPLE BURST DETECTION TO 8 BITS
- PARALLEL ECC IMPLEMENTATION
- COMPUTER GENERATED ECC POLYNOMIAL
- ECC DISABLING CAPABILITY SUPPORTS READ/WRITE, SHORT/LONG FEATURES
- ERROR REPORTING SUPPORTS DISK AND CONTROLLER ERRORS
- SUPPORTS BAD BLOCK MAPPING
- CONTROLS UP TO FOUR 5.25" FLOPPY DISK DRIVES
- PROGRAMMABLE DISK PARAMETERS
- SINGLE SIDED, SINGLE DENSITY; DOUBLE SIDED, SINGLE OR DOUBLE DENSITY SUPPORTED
- INTEGRAL PLL DATA SEPARATOR
- SOFT SECTOR FORMAT COMPATIBILITY

DESCRIPTION

The WD1002-MTB is a custom single board disk controller, specifically designed to interface to Multibus. The WD1002-MTB conforms to all conditions set forth in the IEEE 796 Bus Standard. The purpose of the board is to provide disk control for up to two 5.25" Winchester disk drives and up to four 5.25" Floppy disk drives. All necessary buffers and driver/receivers are included on the board to allow direct connection to the various drives. Power is derived from a single +5VDC supply.

Communications between the host CPU and the WD1002-MTB, as well as all data transfers, are accomplished through DMA transfers. A uniquely defined system of I/O parameter blocks (IOPB) is utilized to establish command structures. One exception to DMA communication exists; e.g. the initial controller "Wake-Up" when the host CPU must pass the vector address of the IOPB to the WD1002-MTB via a specialized vector-stack port, located on the WD1002-MTB.

ARCHITECTURE

The WD1002-MTB architecture is illustrated in Figure 1. The WD1002-MTB board has seven on- board connectors including a test connector (J5) for initial test and alignment procedures. The remaining six connectors consist of two Multibus interface connectors (P1 and P2), one Winchester drive control connector (J1), two Winchester drive data connectors (J3 and J4), and a Floppy disk control connector (J2).

Additional capabilities include interleave factor one capability on hard disk media and extensive use of Western Digital proprietary logic devices. These include the WD1010 Winchester Controller, WD2797 Floppy Controller, WD1100-13 ECC Logic Support Device, WD1802 Octal Comparator, WD1100-10 Write Precomp/Data Separator Logic Support Device, and the DMA Controller.

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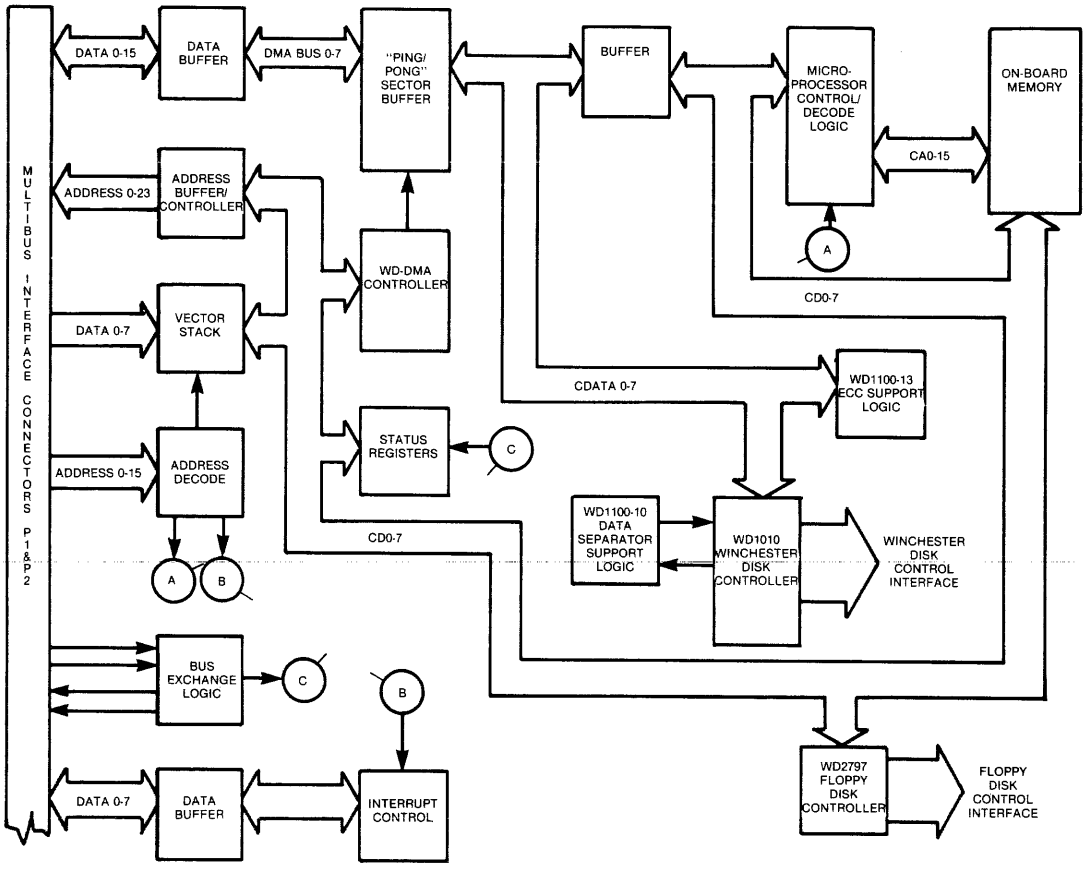

Figure 1. WD1002-MTB SIMPLIFIED BLOCK DIAGRAM

"PING PONG" SECTOR BUFFER ARCHITECTURE

The "ping/pong" buffer consists of dual RAM and counter combinations in two identical halves. All of the buffer controls are multiplexed through a single PAL (U23) for the purpose of properly switching buffers between DMA and microprocessor busses.

It is the unique architecture of these buffers which allows the controller to perform data transfers with 1:1 disk interleaving. It allows data to be written or read simultaneously to both host and controller simply by switching buffers back and forth as they become full and empty.

As can be seen in the preceding illustration, the controller bus and DMA are at opposite sides of the ping/pong. The buffers (tri-state devices) are switched in such a way that the entire ping/pong circuit looks like a single RAM buffer to either the controller or DMA.

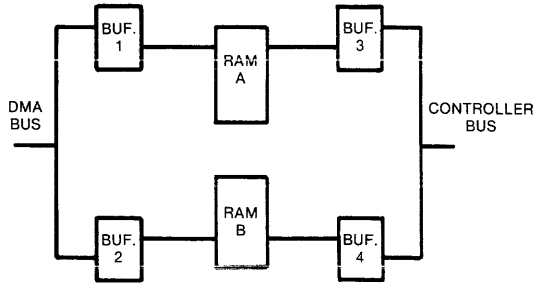

Figure 2. PING/PONG ARCHITECTURE

Example: Buffers 1 & 4 are switched simultaneously 'on' and 'off' and likewise 2 & 3 in opposition to 1 & 4. Neither bus is allowed access to the RAM at the same time. Data starts into one RAM, is switched via the buffers to the opposite bus, and taken in or out there, while more data is being transferred to the second buffer. As the two RAMs become empty and full respectively, they are switched back again for continued operation. All control of the "Ping/Pong" buffer is handled by the on-board Microprocessor while data is transferred by the respective disk controllers (WD1010, WD2797) and DMA. The "Ping/Pong" buffer control 'PAL' contains the following logical equations:

"PING PONG" SECTOR BUFFER OPERATIONAL EQUATIONS

SIGNAL	EQUATION
ARD	$\overline{WCS} * \overline{CCRD} * \overline{SELA} * ACTRO + \overline{DMASTB} * \overline{DMAWR} * SELA$
BRD	$\overline{WCS} * \overline{CCRD} * SELA * \overline{BCTRO} + \overline{DMASTB} * \overline{DMAWR} * \overline{SELA}$
AWR	$\overline{WCS} * \overline{CCWR} * \overline{SELA} * ACTRP\ \overline{DMASTB} * \overline{DMAWR} * SELA$
BWR	$\overline{WCS} * \overline{CCWR} * SELA * \overline{BCTRO} + \overline{DMASTB} * DMAWR * \overline{SELA}$
ADEC	$\overline{AWR} + \overline{WCS} * \overline{CCRD} * \overline{SELA} * ACTRO + \overline{DMASTB} * \overline{DMAWR} * SELA$
BDEC	$\overline{BWR} + \overline{WCS} * \overline{CCRD} * \overline{SELA} * BCTRO + \overline{DMASTB} * \overline{DMAWR} * \overline{SELA}$
IBUFRDY	$ACTRO * \overline{SELA} + BCTRO * SELA$
SMBRDY	$ABSY * SELA + BBSY * \overline{SELA}$

SPECIFICATIONS

TEMPERATURE:

Operating Range . . . . . 5 to 65°C*
Storage Range . . . . . −10 to +50°C
Transit . . −40 to +60 maximum gradient @ 20°C/hr.

*The 65°C includes a maximum 20°C rise in the internal unit.

RELATIVE HUMIDITY:

Operating Range . . . . . 5% to 90%*
Storage Range . . . . . 10% to 90%*

*The range of relative humidity is predicated on the basis of 0% condensation.

ALTITUDE:

Operating Range . . . . . up to 9850 ft. (3000 meters)

POWER:

+5VDC +/−5%, 3.5 amps typical (4.5 amps max)

DRIVE CONTROL SPECIFICATIONS

	WINCHESTER	FLOPPY
Encoding method	MFM	MFM
Cylinders/head	1024	—
Sectors/track	up to 256	17
Drive selects	2	4 (dual head)
Heads	8	—
Step rate	7.5ms to 35μs (500μs incr.)	programmable
Data transfer rate	5 Mbytes/sec	—
Write precomp time	12 ns	—
Drive capability	10 LS loads	—
Head load time	—	programmable
Intersector gap size	—	54 bytes
Motor-off delay time	—	programmable
Sectoring	soft	soft
Cable length (drive)	10 ft(3 m) max.	10 ft(3 m) max.

HOST INTERFACE

The WD1002-MTB is designed specifically as a Multibus compatible peripheral. Interfacing is accomplished in accordance with the IEEE P796 Bus Interface Standard and by the inclusion of an I/O parameter block scheme for command structure. The most direct approach to understanding the interface is to follow a simple interface scenario, which should serve as an overview only.

The host computer writes the address of an IOPB to the WD-1002-MTB. This address is written in 3 bytes, the first two of which are written to the base address of the board and the third, which is written to the base address +1. This third "WRITE" produces a 'wake-up' interrupt to the on-board processor which in turn reads the vector stack port where the address was stored (basically, a FIFO operation). This is the only instance in which communications will take place outside of DMA control.

The on-board processor now arbitrates for the bus, via Multibus convention and, once received, becomes the bus master. The controller now transfers, via DMA, the IOPB pointed to by the vector address and responds to the commands contained therein.

Once an operation has been completed by the controller a completion status is passed back to the host in the IOPB format, as well as any other pertinent information with respect to a given command. Also, upon completion of such commanded transfer, the controller will relinquish this bus for a period of about 500ns for the purpose of allowing other bus masters reasonable access. Burst length is programmable.

In addition, the controller contains an on-board interrupt controller which is entirely the host computer responsibility. That is, the controller has no communication lines with this chip at all, other than to issue it an interrupt. All initialization, set-up, and servicing of this chip must be handled by the host.

An interrupt will be issued by the controller at the completion of all commands or an aborted sequence, provided the interrupt controller is appropriately initialized.

This port is provided for the covenience of interrupt driven systems. If the host is a non-interrupt driven system, an alternative interface can be accomplished by polling the interrupt line or polling the completion code in the host memory.

MULTIBUS INTERFACE CONNECTORS

The Multibus interface connectors (P1 and P2) are card edge connectors compatible with IEEE Microcomputer Bus Standard (P796). Table 1 provides the pin descriptions for P1 and Table 2 provides the pin descriptions for P2.

Table 1. MULTIBUS INTERFACE CONNECTOR P1 PIN DESCRIPTIONS

	COMPONENT SIDE			CIRCUIT SIDE		
FUNCTION	**PIN**	**SIGNAL**	**DESCRIPTION**	**PIN**	**SIGNAL**	**DESCRIPTION**
Power Supplies	1	GND	Signal Ground	2	GND	Signal Ground
	3	+5V	+5VDC	4	+5V	+5VDC
	5	+5V	+5VDC	6	+5V	+5VDC
	7		Spare	8		Spare
	9		Spare	10		Spare
	11	GND	Signal Ground	12	GND	Signal Ground
Bus Controls	13	$\overline{\text{BCLK}}$	Bus Clock	14	$\overline{\text{INIT}}$	Initialization
	15	$\overline{\text{BPRN}}$	Bus Priority In	16	$\overline{\text{BPRO}}$	Bus Priority Out
	17	$\overline{\text{BUSY}}$	Bus Busy	18	$\overline{\text{BREQ}}$	Bus Request
	19	$\overline{\text{MRDC}}$	Mem Read Command	20	$\overline{\text{MWTC}}$	Mem Write Command
	21	$\overline{\text{TORC}}$	I/O Read Command	22	$\overline{\text{TOWC}}$	I/O Write Command
	23	$\overline{\text{XACK}}$	Transfer Acknowledge	24		Spare
	25		Spare	26		Spare
Bus Controls and Address	27	$\overline{\text{BHEN}}$	Byte Hi Enable	28	$\overline{\text{AD10}}$	Address Bus
	29	$\overline{\text{CBRQ}}$	Common Bus Request	30	$\overline{\text{AD11}}$	
	31	$\overline{\text{CCLK}}$	Constant Clock	32	$\overline{\text{AD12}}$	
	33	$\overline{\text{INTA}}$	Interrupt Acknowledge	34	$\overline{\text{AD13}}$	
Interrupts	35	$\overline{\text{INT6}}$	Parallel Interrupt Requests	36	$\overline{\text{INT7}}$	Parallel Interrupt Requests

Table 1. MULTIBUS INTERFACE CONNECTOR P1 PIN DESCRIPTIONS (Continued)

COMPONENT SIDE				CIRCUIT SIDE		
FUNCTION	PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
	37	$\overline{INT4}$		38	$\overline{INT5}$	
	39	$\overline{INT2}$		40	$\overline{INT3}$	
	41	$\overline{INT0}$		42	$\overline{INT1}$	
Address	43	$\overline{ADRE}$	Address Bus	44	$\overline{ADRF}$	Address Bus
	45	$\overline{ADRC}$		46	$\overline{ADRD}$	
	47	$\overline{ADRA}$		48	$\overline{ADRB}$	
	49	$\overline{ADR8}$		50	$\overline{ADR9}$	
	51	$\overline{ADR6}$		52	$\overline{ADR7}$	
	53	$\overline{ADR4}$		54	$\overline{ADR5}$	
	55	$\overline{ADR2}$		56	$\overline{ADR3}$	
	57	$\overline{ADR0}$		58	$\overline{ADR1}$	
Data	59	$\overline{DATE}$	Data Bus	60	$\overline{DATF}$	Data Bus
	61	$\overline{DATC}$		62	$\overline{DATD}$	
	63	$\overline{DATA}$		64	$\overline{DATB}$	
	65	$\overline{DAT8}$		66	$\overline{DAT9}$	
	67	$\overline{DAT6}$		68	$\overline{DAT7}$	
	69	$\overline{DAT4}$		70	$\overline{DAT5}$	
	71	$\overline{DAT2}$		72	$\overline{DAT3}$	
	73	$\overline{DAT0}$		74	$\overline{DAT1}$	
	75	GND	Signal Ground	76	GND	Signal Ground
	77		Spare	78		Spare
	79		Spare	80		Spare
	81		Spare	82		Spare
	83		Spare	84		Spare
	85	GND	Signal Ground	86	GND	Signal Ground

Table 2. MULTIBUS INTERFACE CONNECTOR P2 PIN DESCRIPTIONS

COMPONENT SIDE				CIRCUIT SIDE		
FUNCTION	PIN	SIGNAL	DESCRIPTION	PIN	SIGNAL	DESCRIPTION
	1-53 (odd)		Spare	2-54 (even)		Spare
Address	55	$\overline{ADR16}$	Address Bus	56	$\overline{ADR17}$	Address Bus
	57	$\overline{ADR14}$		58	$\overline{ADR15}$	
	59		Spare	60		Spare

WINCHESTER DRIVE CONNECTORS

Winchester Drive Control and Data Connectors

The Winchester drive control connector (J1) is daisy-chained to each of the two Winchester disk drives supported by the WD1002-MTB. The Winchester drive data connectors (J3 and J4) carry differential signals and are radially connected to the Winchester drives. The Winchester drive control requires the last drive to contain termination resisters. Table 3 provides the pin descriptions for Winchester Drive Control connector J1 and Table 4 provides the pin descriptions for Winchester Drive Data connectors J3 and J4.

Table 3. WD1002-MTB WINCHESTER DRIVE CONTROL CONNECTOR J1 PIN DESCRIPTIONS

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
1	2	O	$\overline{RWC}$	Reduce Write Current
3	4	O	$\overline{HS2}$	Head Select 2
5	6	O	$\overline{WG}$	Write Gate
7	8	I	$\overline{SEEK}$	Seek
9	10	I	$\overline{TR000}$	Track 000
11	12	I	$\overline{WF}$	Write Fault
13	14	O	$\overline{HS0}$	Head Select 0
15	16	—	$\overline{NC}$	No Connection
17	18	O	$\overline{HS1}$	Head Select 1
19	20	I	$\overline{IND}$	Index
21	22	I	$\overline{RDY}$	Ready
23	24	O	$\overline{STEP}$	Step
25	26	O	$\overline{DS1}$	Drive Select 1
27	28	O	$\overline{DS2}$	Drive Select 2
29	30	O	$\overline{DS3}$	Drive Select 3
31	32	O	$\overline{DS4}$	Drive Select 4
33	34	O	$\overline{DIRIN}$	Direction In

Table 4. WD1002-MTB WINCHESTER DRIVE DATA CONNECTORS J3 AND J4 PIN DESCRIPTIONS

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
2	1	I	$\overline{DS}$	Drive Select
4	3	—	NC	No Connection
6	5	—	NC	No Connection
8	7	—	NC	No Connection
—	9	—	NC	No Connection
—	10	—	NC	No Connection
11	—	—	GND	Ground
12	—	—	GND	Ground
—	13	O	+ MFMWD	+ MFM Write Data
—	14	O	– MFMWD	– MFM Write Data
15	—	—	GND	Ground
16	—	—	GND	Ground
—	17	I	+ MFMRD	+ MFM Read Data
—	18	I	– MFMRD	– MFM Read Data
19	—	—	GND	Ground
20	—	—	GND	Ground

WINCHESTER DRIVE CONTROL SIGNAL DESCRIPTIONS

Reduce Write Current

When the Reduce Write Current line is activated with Write Gate, a lower write current is used to compensate for greater bit packing density on the inner cylinders. The RWC line is activated when the cylinder number is greater than or equal to four times the contents of the Write Precomp Register. This output is valid only during Write and Format commands.

Write Gate

This output signal allows data to be written on the disk.

Seek Complete

Informs the WD1002-MTB that the head of the selected drive has reached the desired cylinder and has stabilized. Seek Complete is not checked after a SEEK command, thus allowing overlapped seeks.

Track 000

Indicates that the R/W heads are positioned on the outer-most cylinder. This line is sampled immediately before each step is issued.

Write Fault

Informs the WD1002-MTB that some fault has occurred on the selected drive. The WD1002-MTB will not execute commands when this signal is true.

HS0-HS2

Head Select lines are used by the WD1002-MTB to select a specific R/W head on the selected drive.

Index

Is used to indicate the index point for synchronization during formatting and as a time out mechanism for retries. This signal should pulse once each rotation of the disk.

Ready

Informs the WD1002-MTB that the desired drive is selected and that its motor is up to speed. The WD1002-MTB will not execute commands unless this line is true.

Step

This line is pulsed once for each cylinder to be stepped. The direction of the step will be determined by the DIRECTION IN line. The step pulse period is determined by the internal stepping rate register during implied seek operations or explicitly during Seek and Restore commands. During auto restore, the step pulse period is determined by the SEEK COMPLETE time from the drive.

Direction In

Determines the direction of motion of the R/W head when the step line is pulsed. A high on this line defines the direction as out and a low defines direction as in.

DS1-DS4

These four Drive Select lines are used to select the desired drive.

Floppy Drive Control Connector

All commands and data to the Floppy drives are transferred via the Floppy drive control connector (J2) which is daisy-chained to the Floppy drives supported by the WD1002-MTB (up to four). The last Floppy drive in the chain also requires termination resisters. Table 5 provides the pin descriptions for Floppy drive control connector J2.

Table 5. FLOPPY DRIVE CONTROL CONNECTOR J2 PIN DESCRIPTION

SIGNAL GND	SIGNAL PIN	I/O	SIGNAL	DESCRIPTION
1	2	—		Spare
3	4	O	$\overline{\text{READY}}$	In Use
5	6	O	$\overline{\text{DS4}}$	Drive Select 4
7	8	I	$\overline{\text{I/S}}$	Index/Sector
9	10	O	$\overline{\text{DS1}}$	Drive Select 1
11	12	O	$\overline{\text{DS2}}$	Drive Select 2
13	14	O	$\overline{\text{DS3}}$	Drive Select 3
15	16	O	$\overline{\text{MO}}$	Motor On
17	18	O	$\overline{\text{DIRC}}$	Direction
19	20	O	$\overline{\text{STEP}}$	Step
21	22	O	$\overline{\text{WD}}$	Write Data
23	24	O	$\overline{\text{WG}}$	Write Gate
25	26	I	$\overline{\text{TR00}}$	Track 00
27	28	I	$\overline{\text{WPRT}}$	Write Protect
29	30	I	$\overline{\text{RD}}$	Read Data
31	32	O	$\overline{\text{SS}}$	Side Select
33	34	—		Spare

HOST COMPUTER OPERATION

The WD1002-MTB provides the host computer a signal interface to both the floppy and Winchester disks. It does not buffer commands. The host gives the controller a single command and then waits until the controller interrupts the host to signal operation complete.

The WD1002-MTB deals only with physical drives. If the host wishes to treat one physical drive as several logical devices, then the host must keep track of these correspondences and must specify to the controller the appropriate physical drive and physical block(s) for each operation.

The host constructs an INPUT/OUTPUT Parameter Block (IOPB) to specify the desired operation and passes the address of that IOPB to the controller, via the vector address stack.

The host then waits for an interrupt from the controller. Until this interrupt occurs, the IOPB belongs to the controller and none of its contents are valid. When the interrupt occurs, the host checks the completion code returned in the IOPB to determine the success or failure of the operation.

IOPB OUTLINE

BYTES	DESCRIPTION
0	Command code (WD1002-MTB input parameter)
1	Completion code (WD1002-MTB output parameter)
2	Subdevice number (WD1002-MTB input parameter)
3	Not used
4,5,6,7	Block address (WD1002-MTB input parameter)
8,9,10,11	Memory address (WD1002-MTB input parameter)
12,13	Block count (WD1002-MTB input parameter)
14,15	Reserved for future use

As shown above, the Input/Output Parameter Block (IOPB) contains 16 bytes. For the convenience of the host computer each 2-byte field is aligned on a word boundary and each 4-byte field is aligned on a lone word boundary within the IOPB. The significance ordering of the bytes in each multi-byte field is selectable by two jumpers on the WD1002-MTB board (E44 to E43) and (E50 to E51). For 68000 operation [most significant byte (MSB) in least significant address (LSA)] E44,43 is left in tact and no jumper is required on E50,51. For Intel operation the E43,44 etch must be cut and a jumper placed on E50,51. All IOPB transfers are performed in the byte made only and therefore only the byte ordering as outlined is significant. The IOPB vector stack address must be received with the least significant byte first.

COMMANDS

0 = No action
1 = Sense Status
2 = Restore
3 = Seek
4 = Read Blocks
5 = Write Blocks
6 = Read Diagnostic
7 = Write Diagnostic
8 = Write Deleted Block
9 = Set Device Parameter
10 = Set Control Parameter
11 = Self-Test
12 = Format Blocks
13 = Reset
14 = Read bad block table
15 = Write bad block table
16 = Read device parameter
17 = Read control parameter

COMPLETION CODES

0 = No error
1 = Controller error
2 = Parameter error
3 = Aborted command
4 = Bad block
5 = Not used
6 = Block not found
7 = CRC error
8 = Write protect
9 = Write fault
A = Time-out
B = Host cancel
C = Multibus error
D = Data address mark not found
E = Track zero not found
F = Possible flex media change notification

The following commands return completion codes: no action, restore, seek, read blocks, write blocks, read diagnostic, write diagnostic, write deleted block, set device parameter, set control parameter, format blocks, reset, read bad block table, and write bad block table.

The following commands do not return completion codes: sense status and self-test.

A completion code is returned only if it is applicable and if no higher priority completion code is applicable. The completion codes in order from lowest to highest priority are: No error, Parameter error, Block not found, CRC error, Bad block, Aborted command, Write protect, Write fault, Time-out, Controller error, Multibus error and Host cancel.

NOTE:
Bit seven of the completion code is reserved as the controller busy bit for systems operating in a polled rather than an interrupt environment. An 80 hex should be written into the completion code byte prior to initiating an operation. The controller will then clear the bit at the end of command execution.

At the end of a command execution two bytes are transferred back to the host. The first byte is the command code and the second byte is the completion code.

Command Code

The command code specifies the operation to be performed by the WD1002-MTB. The command code is a WD1002-MTB input parameter.

Completion Code

The completion code indicates the success or reason for failure of a command. Completion code zero indicates successful completion of the command. A non-zero completion code indicates an error. The completion code is a WD1002-MTB output parameter.

All commands except sense status and self-test return a completion code. Sense status returns a status code and self-test returns a test result code. For both of these parameters the value zero indicates no error just as it does for the completion code. However, a non-zero status code or test result code does not mean what the same value completion code means.

Subdevice Number

The subdevice number specifies the operation's target disk drive. Subdevice numbers 0 and 1 specify Winchester drives 0 and 1, and the subdevice numbers 4 to 7 specify floppy drives 0 to 3. The subdevice number is a WD1002-MTB input parameter.

Block Address

For all operations except seek, the block address specifies the first block to be accessed. For a seek operation the block address specifies the target cylinder. The block address is a WD1002-MTB input parameter.

The block address is calculated from the block number, head number, and cylinder number using the formula:

BLOCK ADDRESS = Block number + (head number * blocks per track) + (cylinder number * number of heads * blocks per track).

Note that the blocks are numbered 0, 1, 2, 3, . . . up to the number of blocks per track minus one. The standard floppy formats all number blocks 1, 2, 3, . . . Consequently, the WD1002-MTB adds one to the block number to obtain the block number that is actually in the block header on the disk.

Memory Address

The memory address is a one-byte offset from the Multibus memory base address. That is, it is a "Multibus memory address." It is the Least Significant Address (LSA) in a buffer. A read operation transfers data from disk to Multibus memory beginning at this address. A write operation transfers data from Multibus memory beginning at this address to disk. Format uses the interleave table beginning at this address in Multibus memory. The memory address is a WD1002-MTB input parameter.

Block Count

The block count specifies the number of blocks to be transferred. It is a WD1002-MTB input parameter.

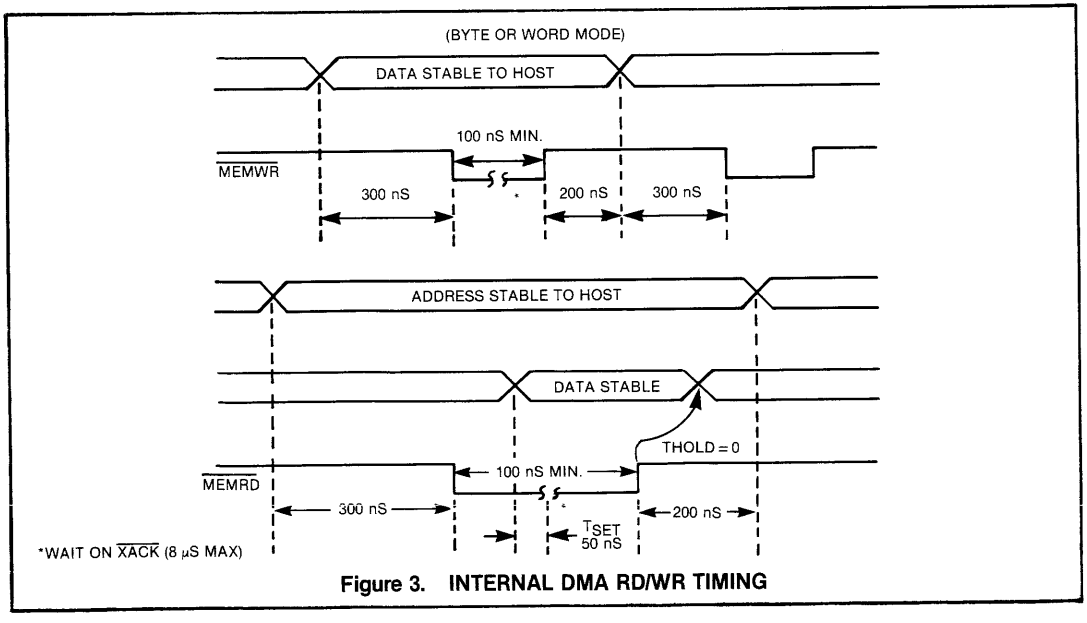

Figure 3. INTERNAL DMA RD/WR TIMING

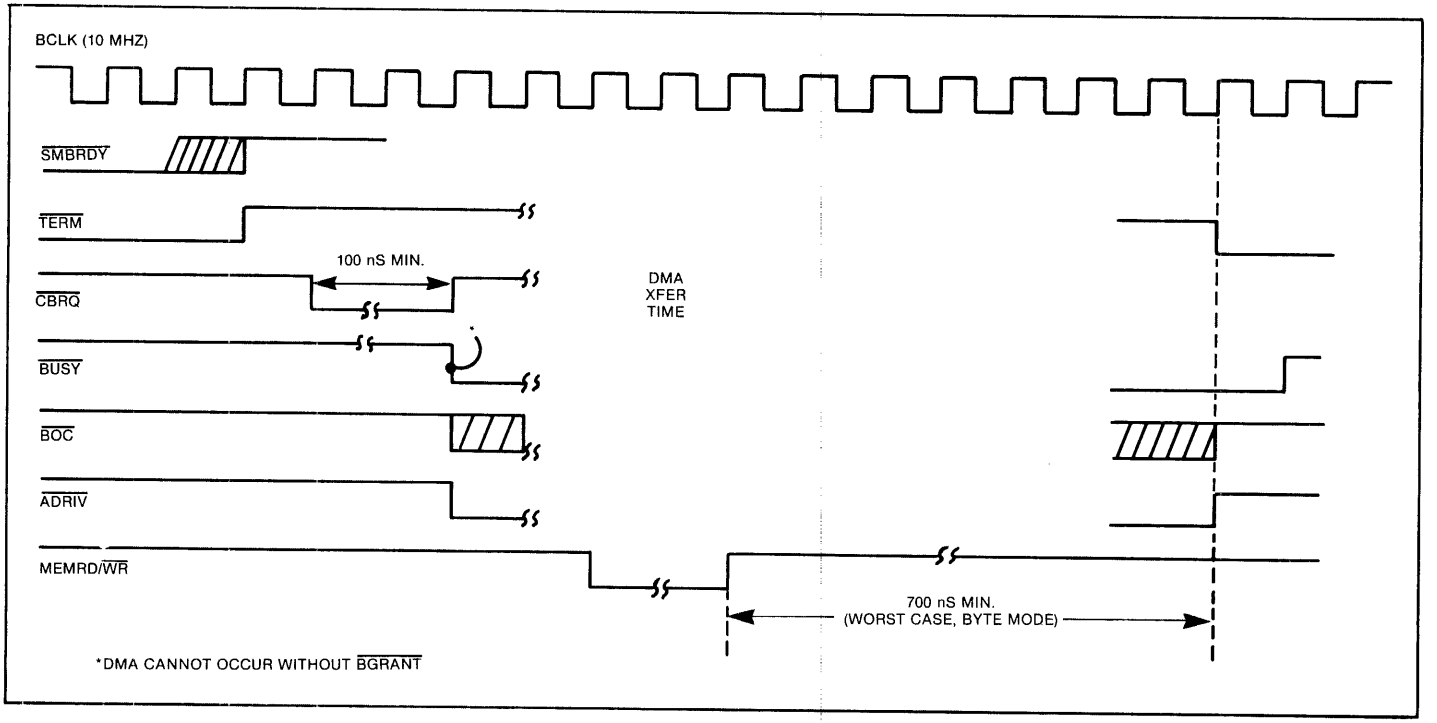

Figure 4. DMA/MULTIBUS TIMING

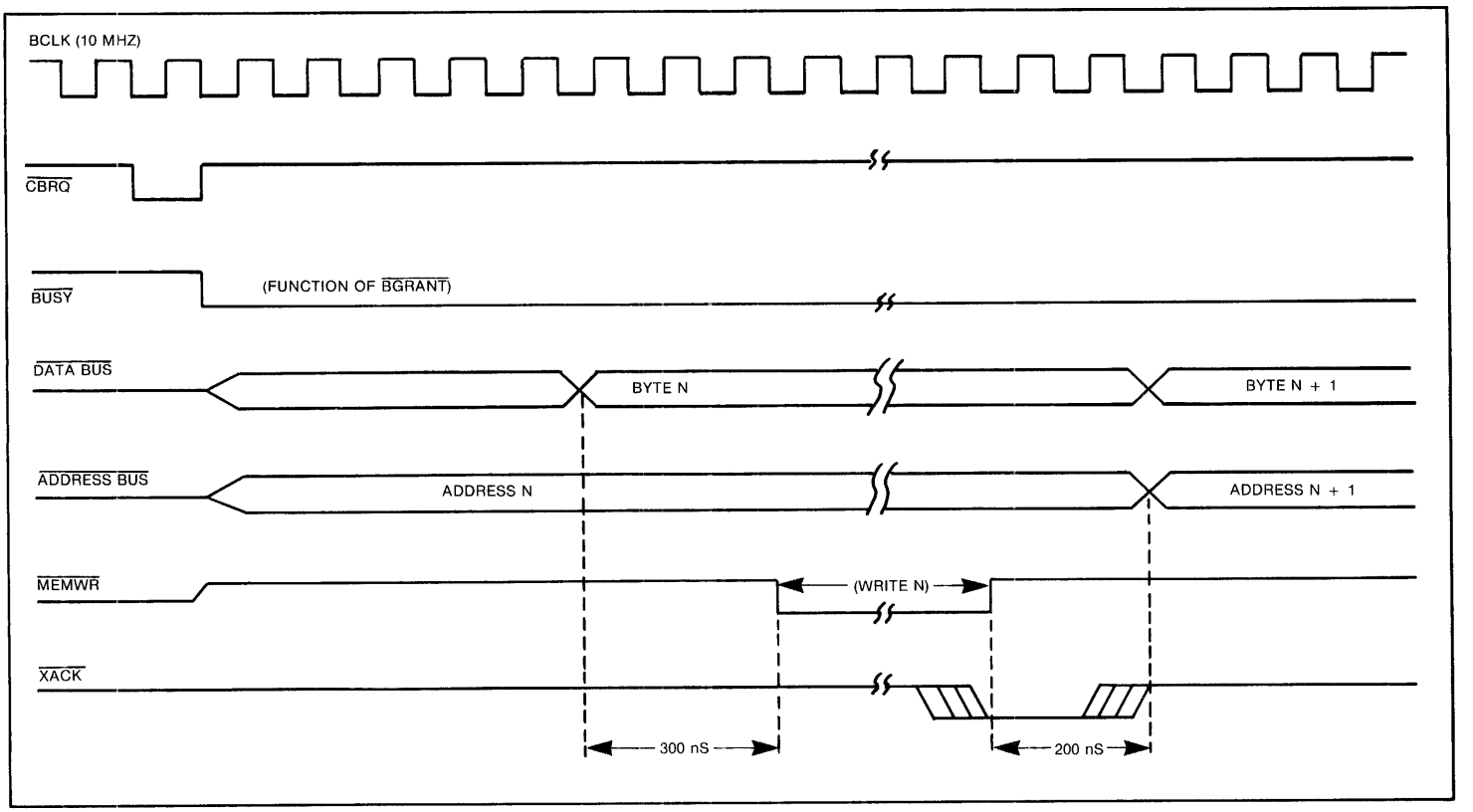

Figure 5. FIRST DMA WRITE TO HOST TIMING

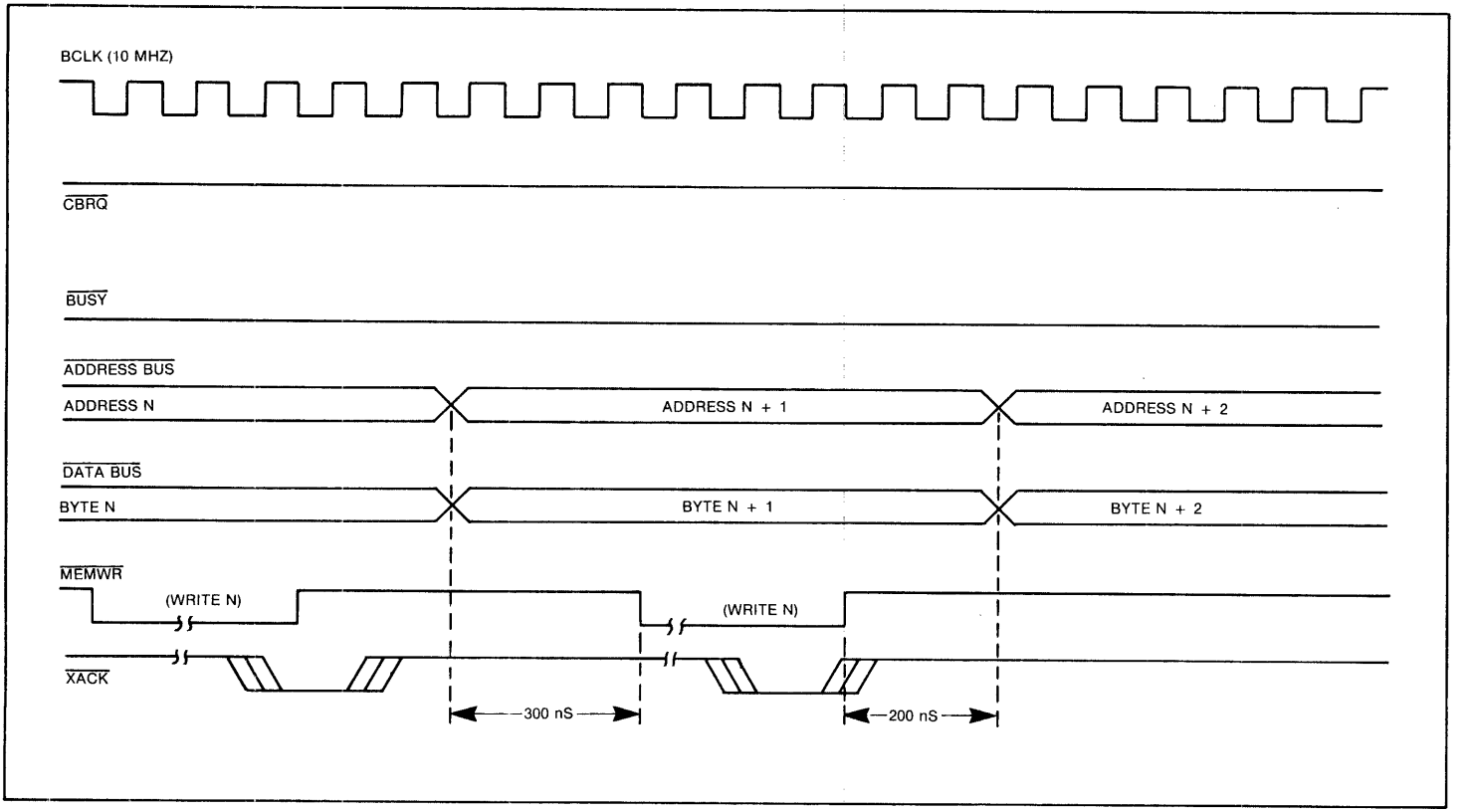

Figure 6. INTERIM WRITE DMA TO HOST TIMING

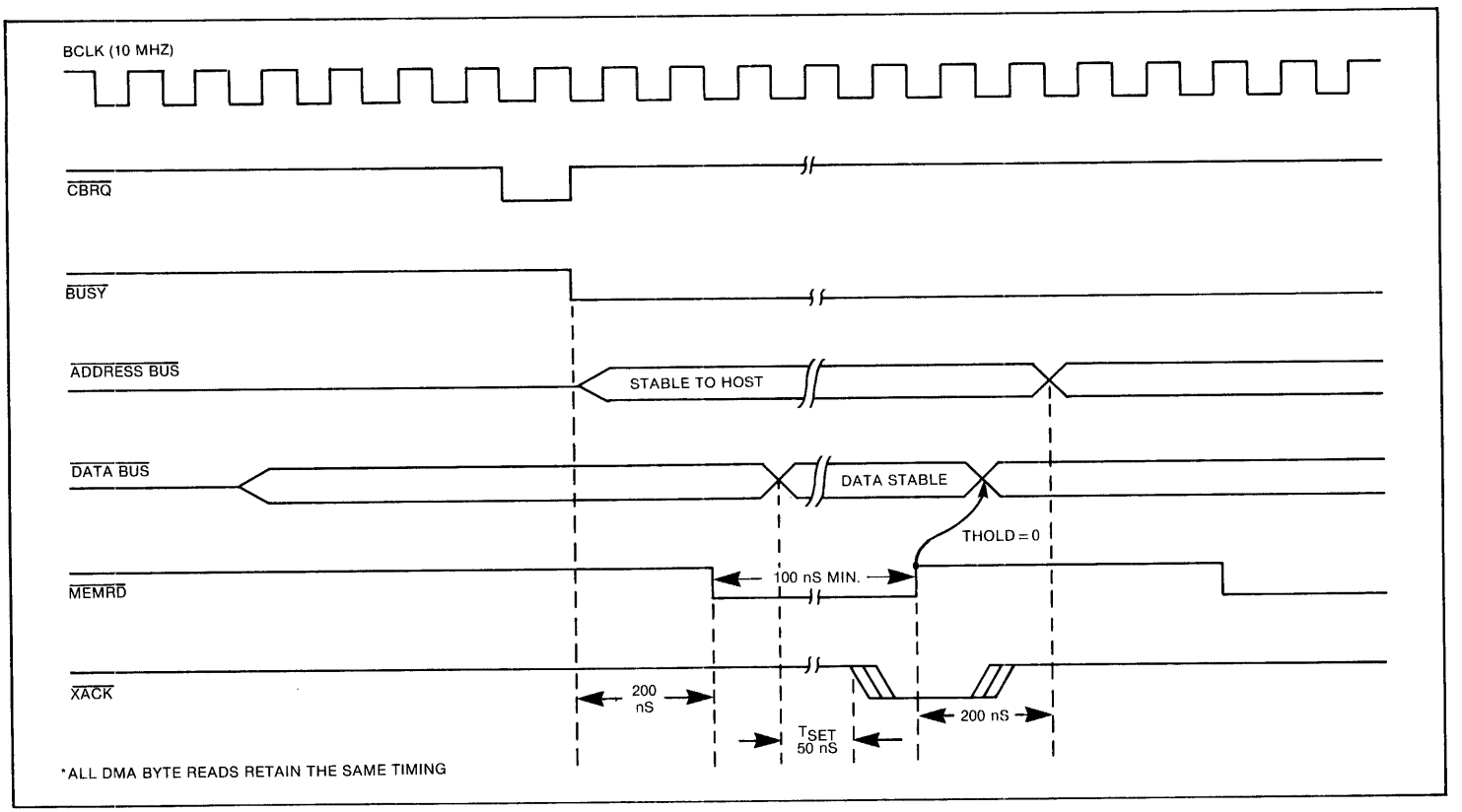

Figure 7. DMA BYTE READ (FROM HOST) TIMING

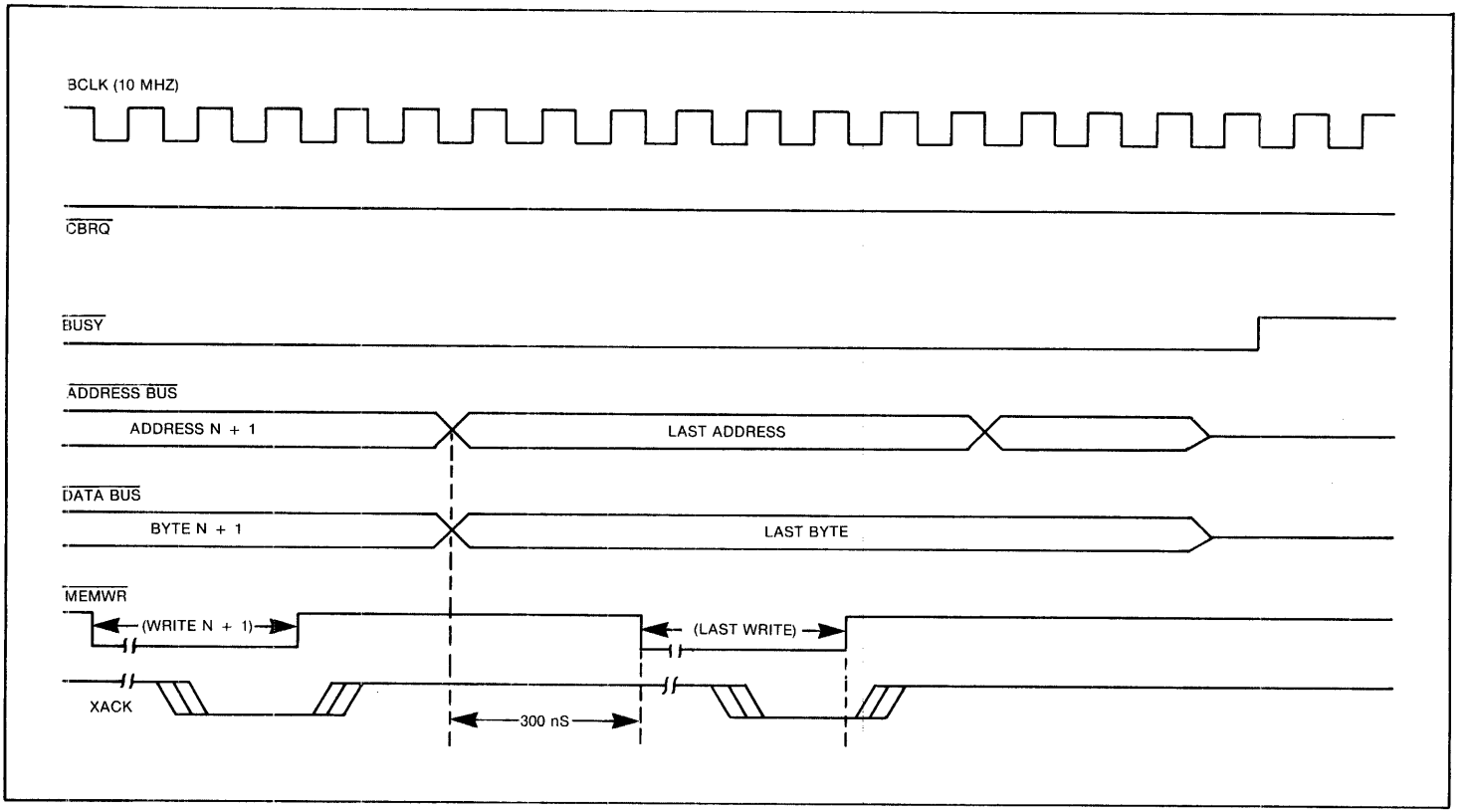

Figure 8. LAST DMA BYTE WRITE TO HOST

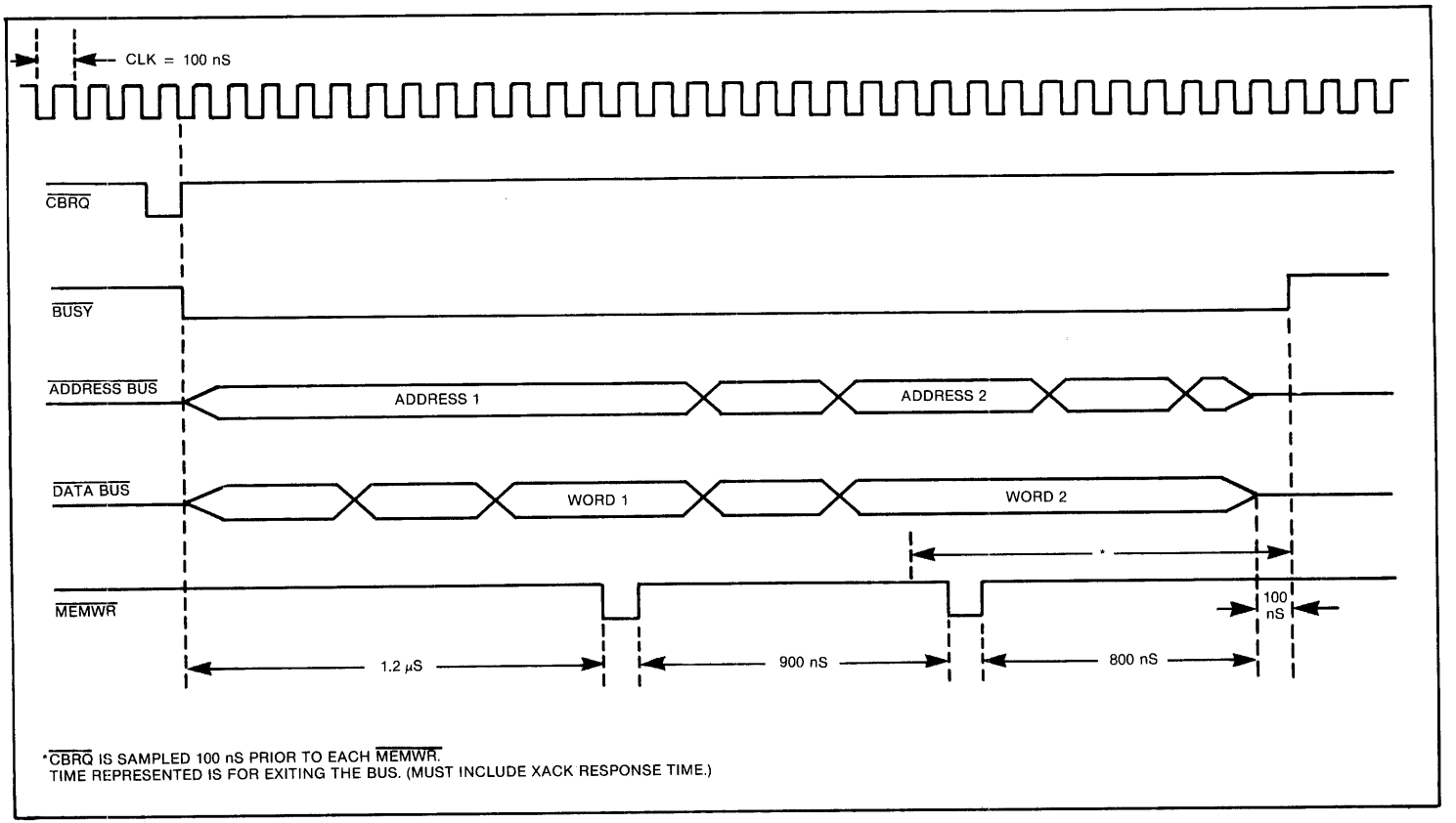

Figure 9. TYPICAL 2-WORD DATA TRANSFER TO HOST

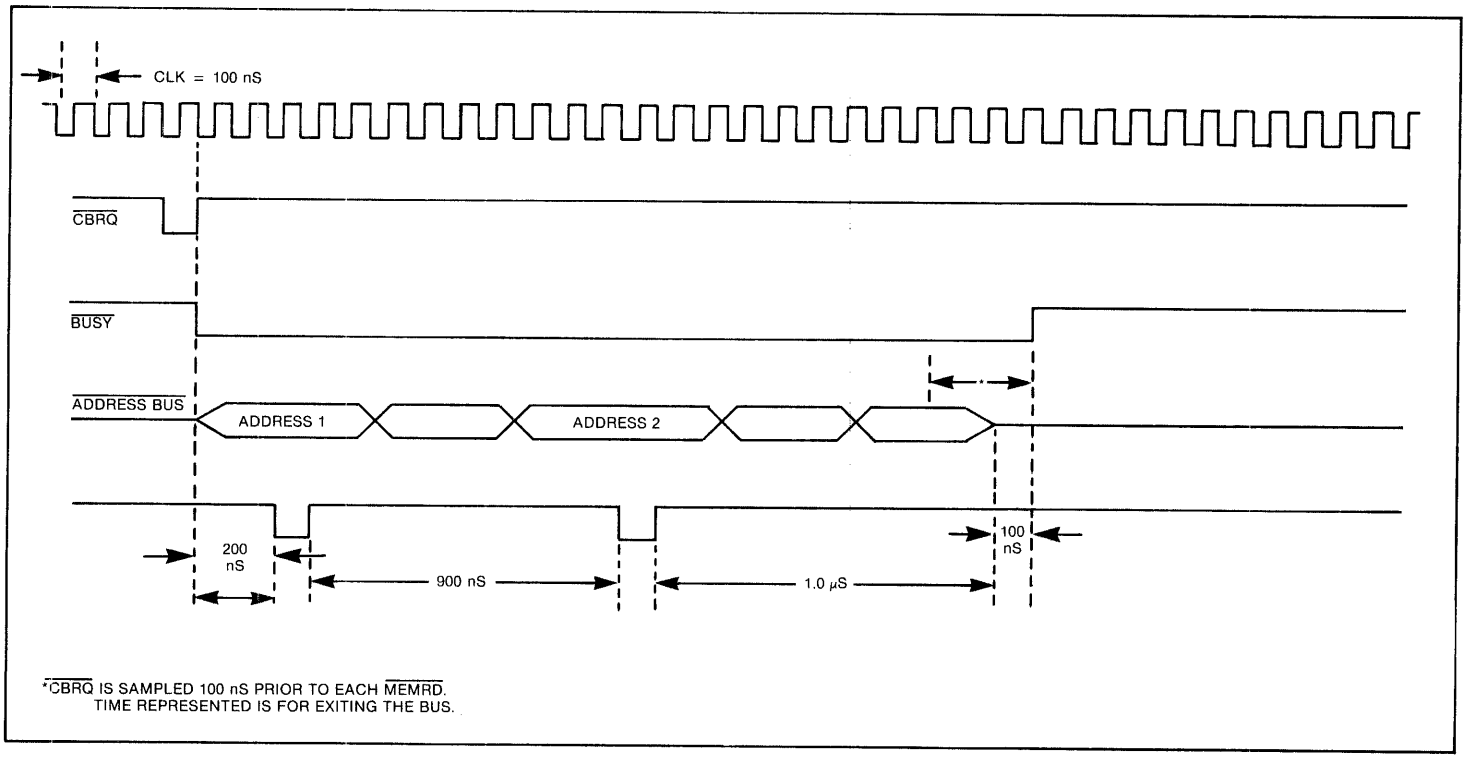

Figure 10. TYPICAL 2-WORD DATA TRANSFER FROM HOST

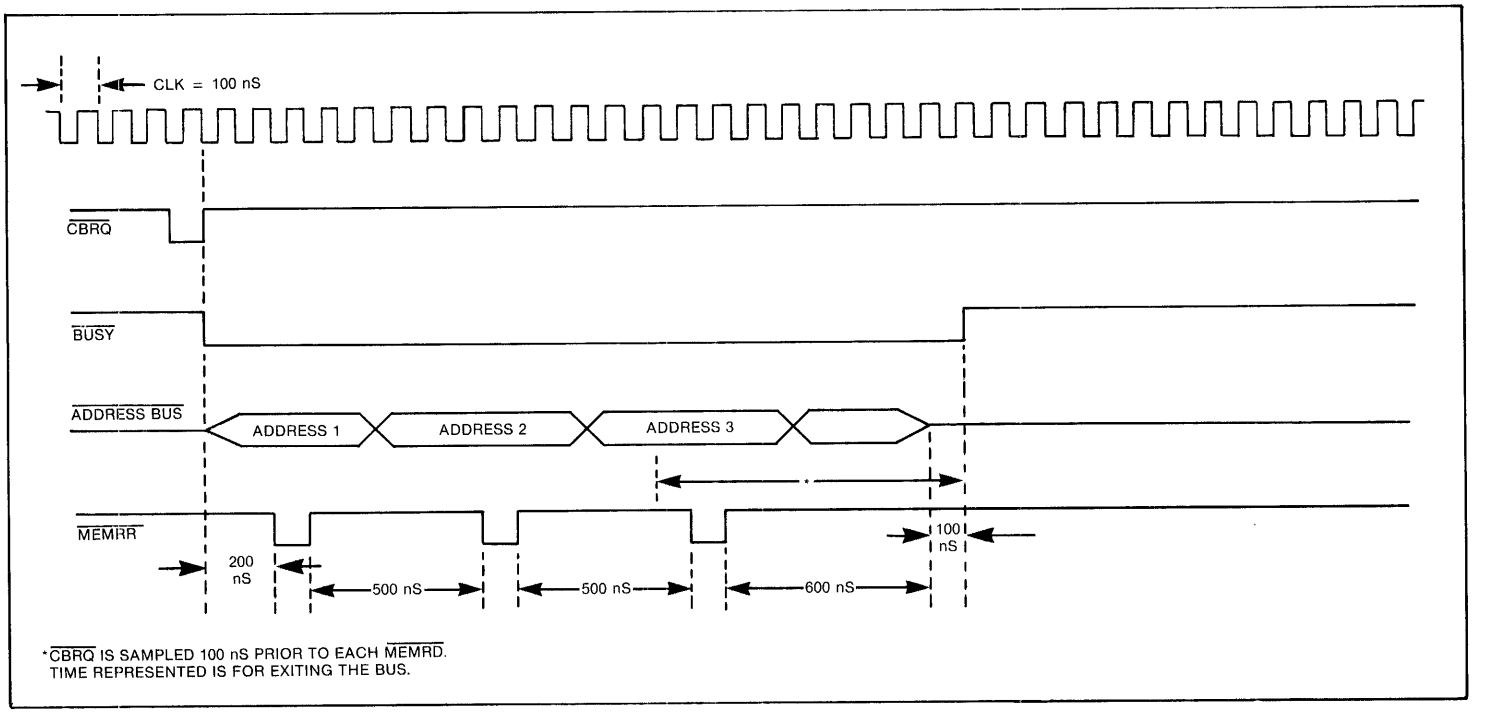

Figure 11. TYPICAL 3-WORD DATA TRANSFER TO HOST

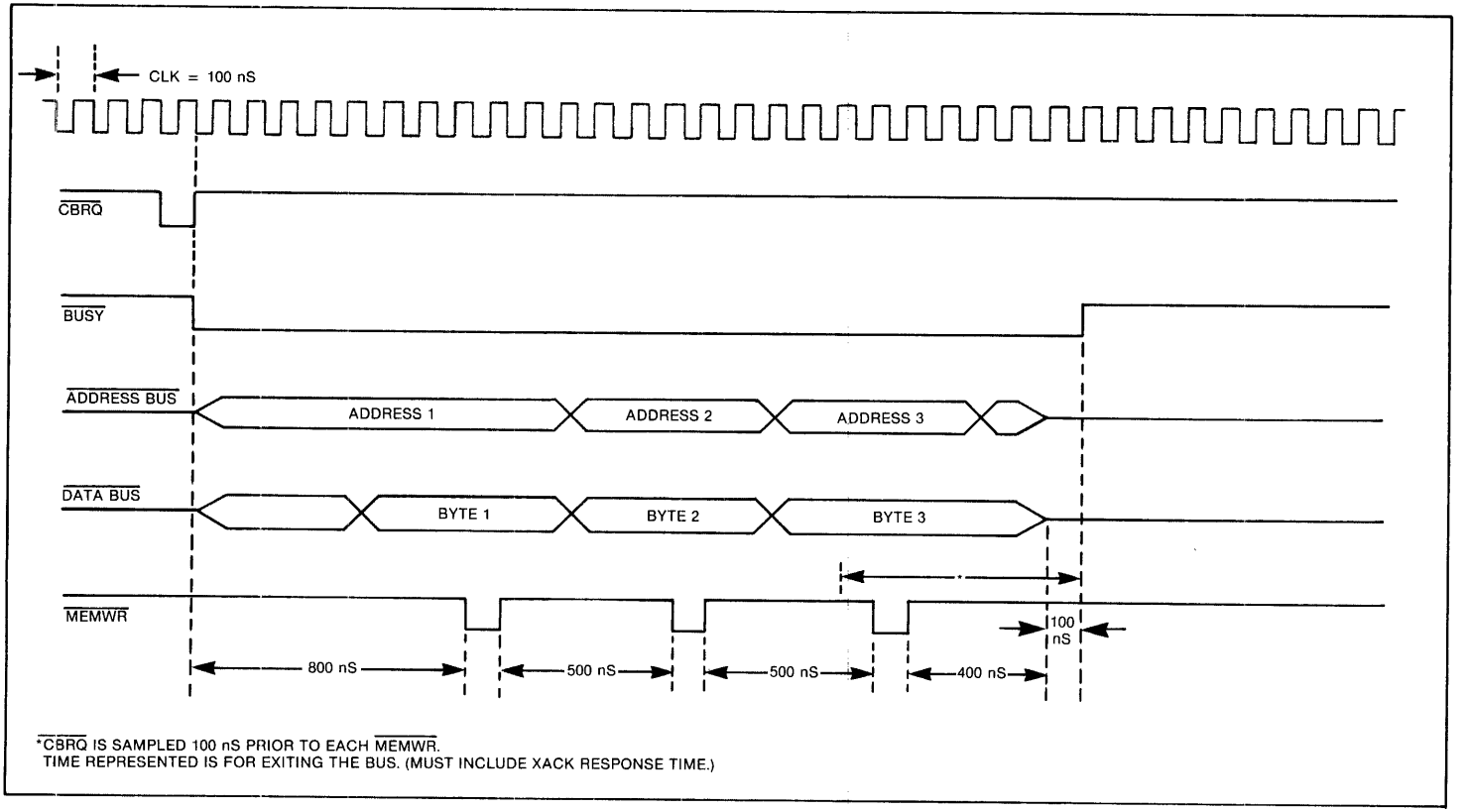

Figure 12. TYPICAL 3-BYTE TRANSFER TO HOST

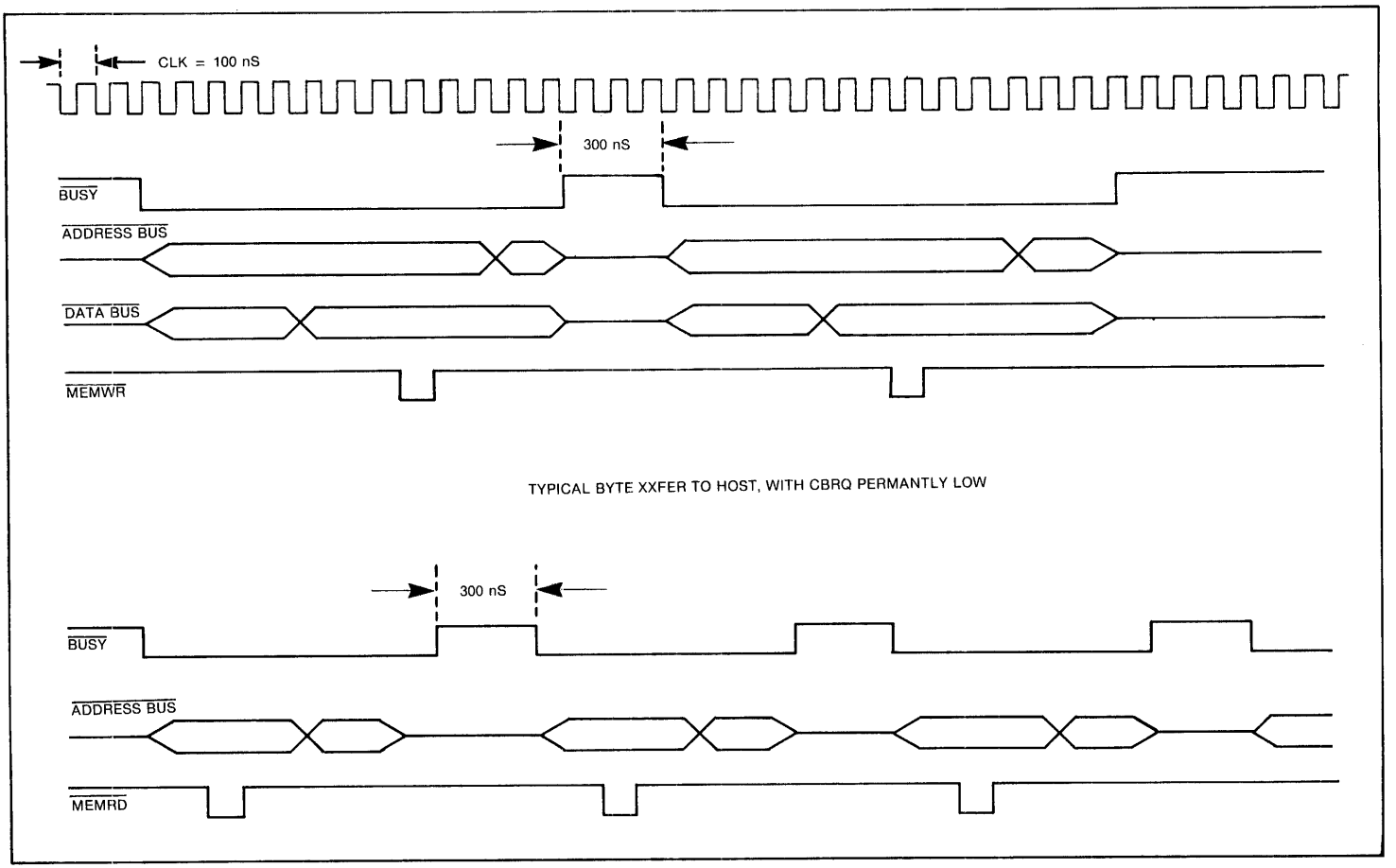

Figure 13. TYPICAL BYTE XFER FROM HOST WITH CBRQ PERMANTLY LOW

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WESTERN DIGITAL
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WD1055-SCS SMD Controller Board

FEATURES

- SMD DRIVE INTERFACE COMPATABILITY
- 56 BIT ECC
- 1K ON-BOARD BUFFER
- 10 MBIT DATA TRANSFER RATE
- SASI™ HOST INTERFACE COMPATIBILITY
- 8/16 BIT INTERFACE WITH HOST
- CAPABLE OF 1:1 INTERLEAVE
- PROGRAMMABLE POLYNOMIAL GENERATOR
- MARGINAL DATA RECOVERY CAPABILITY
- SINGLE/MULTIPLE RECORD OPERATION
- HARD SECTOR FORMAT
- SINGLE/MULTIPLE UNIT DRIVE SUPPORT

DESCRIPTION

The WD1055-SCS provides the necessary interface and control for Host systems to store and retrieve data from SMD disk drives. The WD1055-SCS is fully compatible with Host systems using the SASI bus interface. This includes the logic necessary for communicating with the Host via the SASI bus and all sequencing and control signals required for operation.

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WESTERN DIGITAL
CORPORATION

WD1055-MTB Multibus™ SMD Disk Drive Controller Board

FEATURES

- SMD DRIVE INTERFACE COMPATABILITY
- 56 BIT ECC
- 1K ON-BOARD BUFFER
- 10 MBITS/SEC DATA TRANSFER RATE (SMD INTERFACE)
- MULTIBUS (IEEE 796) COMPATABILITY
- 8/16 BIT DATA STRUCTURE ON HOST INTERFACE
- CAPABLE OF 1-1 INTERLEAVE
- MARGINAL DATA RECOVERY CAPABILITY
- SINGLE/MULTIPLE RECORD OPERATION
- HARD SECTOR FORMAT
- SINGLE/MULTIPLE UNIT DRIVE SUPPORT

DESCRIPTION

The WD1055-MTB provides facilities necessary for Host Systems to store and retrieve data from SMD disk drives. The WD1055-MTB is also compatible with host systems conforming to the Multibus electrical and mechanical discipline as described in the IEEE 796 specification. This includes the logic necessary to communicate with the host or hosts via the Multibus and all the sequencing and control signals required for the operation of one or more masters within the Multibus module.

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WESTERN DIGITAL
CORPORATION

WD8206 Error Detection and Correction Unit

FEATURES

- Detects and Corrects All Single Bit Errors.
- Detects All Double Bit and Most Multiple Bit Errors
- 52 ns Maximum for Detection; 67 ns Maximum for Correction (16 Bit System)
- Expandable to Handle 80 Bit Memories
- Syndrome Outputs for Error Logging
- Separate Input and Output Busses — No Timing Strobes Required
- Supports Reads With and Without Correction, Writes, Partial (Byte) Writes, and Read-Modify-Writes
- HMOS Technology for Low Power
- 68 Pin Leadless JEDEC Package
- Single +5V Supply

GENERAL DESCRIPTION

The HMOS 8206 Error Detection and Correction Unit is a high-speed device that provides error detection and correction for memory systems (static and dynamic) requiring high reliability and performance. Each 8206 handles 8 or 16 data bits and up to 8 check bits. 8206's can be cascaded to provide correction and detection for up to 80 bits of data. Other 8206 features include the ability to handle byte writes, memory initialization, and error logging.

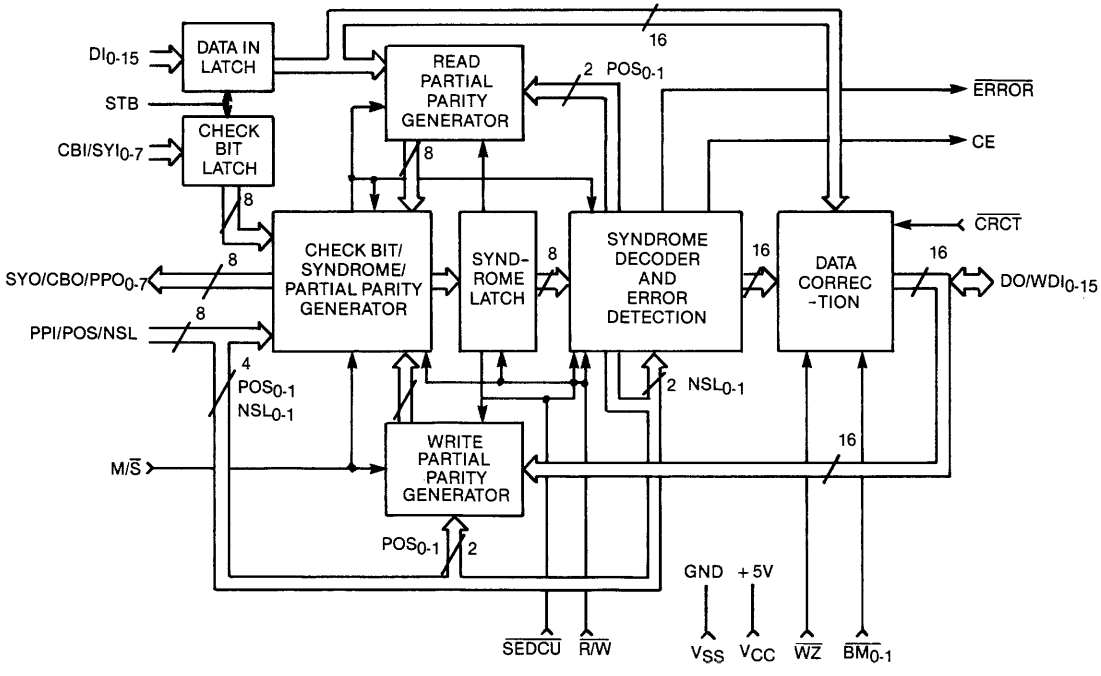


Figure 1. 8206 BLOCK DIAGRAM

Table 1. PIN DESCRIPTION

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
1, 68-61, 59-53	DI_{0-15}	I	**Data In:** These inputs accept a 16 bit data word from RAM for error detection and/or correction.
5	CBI/SYI_0	I	**Check Bits In/Syndrome In:** In a single 8206 system, or in the master in a multi-8206 system, these inputs accept the check bits (5 to 8) from the RAM. In a single 8206 16 bit system, CBI_{0-5} are used. In slave 8206's these inputs accept the syndrome from the master.
6	CBI/SYI_1	I	
7	CBI/SYI_2	I	
8	CBI/SYI_3	I	
9	CBI/SYI_4	I	
10	CBI/SYI_5	I	
11	CBI/SYI_6	I	
12	CBI/SYI_7	I	
51	DO/WDI_0	I/O	**Data Out/Write Data In:** In a read cycle, data accepted by DI_{0-15} appears at these outputs corrected if CRCT is low, or uncorrected if CRCT is high. The BM inputs must be high to enable the output buffers during the read cycle. In a write cycle, data to be written into the RAM is accepted by these inputs for computing the write check bits. In a partial-write cycle, the byte not to be modified appears at either DO_{0-7} if BM_0 is high, or DO_{8-15} if BM_1 is high, for writing to the RAM. When WZ is active, it causes the 8206 to output all zeroes at DO_{0-15}, with the proper write check bits on CBO.
50	DO/WDI_1	I/O	
49	DO/WDI_2	I/O	
48	DO/WDI_3	I/O	
47	DO/WDI_4	I/O	
46	DO/WDI_5	I/O	
45	DO/WDI_6	I/O	
44	DO/WDI_7	I/O	
42	DO/WDI_8	I/O	
41	DO/WDI_9	I/O	
40	DO/WDI_{10}	I/O	
39	DO/WDI_{11}	I/O	
38	DO/WDI_{12}	I/O	
37	DO/WDI_{13}	I/O	
36	DO/WDI_{14}	I/O	
35	DO/WDI_{15}	I/O	
23	$SYO/CBO/PPO_0$	O	**Syndrome Out/Check Bits Out/Partial Parity Out:** In a single 8206 system, or in the master in a multi-8206 system, the syndrome appears at these outputs during a read. During a write, the write check bits appear. In slave 8206's the partial parity bits used by the master appear at these outputs. The syndrome is latched (during read-modify-writes) by R/W going low.
24	$SYO/CBO/PPO_1$	O	
25	$SYO/CBO/PPO_2$	O	
27	$SYO/CBO/PPO_3$	O	
28	$SYO/CBO/PPO_4$	O	
29	$SYO/CBO/PPO_5$	O	
30	$SYO/CBO/PPO_6$	O	
31	$SYO/CBO/PPO_7$	O	
13	PPI_0/POS_0	I	**Partial Parity In/Position:** In the master in a multi-8206 system, these inputs accept partial parity bits O and 1 from the slaves. In a slave 8206 these inputs inform it of its position within the system (1 to 4). Not used in a single 8206 system.
14	PPI_1/POS_1	I	
15	PPI_2/NSL_0	I	**Partial Parity In/Number of Slaves:** In the master in a multi-8206 system, these inputs accept partial parity bits 2 and 3 from the slaves. In a multi-8206 system these inputs are used in slave number 1 to tell it the total number of slaves in the system (1 to 4). Not used in other slaves or in a single 8206 system.
16	PPI_3/NSL_1	I	
17	PPI_4/CE	I/O	**Partial Parity In/Correctable Error:** In the master in a multi-8206 system this pin accepts partial parity bit 4. In slave number 1 only, or in a single 8206 system, this pin outputs the correctable error flag. CE is latched by R/W going low. Not used in other slaves.
18	PPI_5	I	**Partial Parity In:** In the master in a multi-8206 system these pins accept partial parity bits 5 to 7. The number of partial parity bits equals the number of check bits. Not used in single 8206 systems or in slaves.
19	PPI_6	I	
20	PPI_7	I	

Table 1. PIN DESCRIPTION (CONTINUED)

PIN NUMBER	SYMBOL	TYPE	NAME AND FUNCTION
22	ERROR	O	**Error:** This pin outputs the error flag in a single 8206 system or in the master of a multi-8206 system. It is latched by R/W going low. Not used in slaves.
52	CRCT	I	**Correct:** When low this pin causes data correction during a read or read-modify-write cycle. When high, it causes error correction to be disabled, although error checking is still enabled.
2	STB	I	**Strobe:** STB is an input control used to strobe data at the DI inputs and check-bits at the CBI/SYI inputs. The signal is active high to admit the inputs. The signals are latched by the high-to-low transition of STB.
33 32	BM_0 BM_1	I I	**Byte Marks:** When high, the Data Out pins are enabled for a read cycle. When low, the Data Out buffers are tristated for a write cycle. BM_0 controls DO_{0-7}, while BM_1 controls DO_{8-15}. In partial (bytes) writes, the byte mark input is low for the new byte to be written.
21	R/W	I	**Read/Write:** When high this pin causes the 8206 to perform detection and correction (if CRCT is low). When low, it causes the 8206 to generate check bits. On the high-to-low transition the syndrome is latched internally for read-modify-write cycles.
34	WZ	I	**Write Zero:** When low this input overrides the BM_{0-1} and R/W inputs to cause the 8206 to output all zeros at DO_{0-15} with the corresponding check bits at CBO_{0-7}. Used for memory initialization.
4	M/S	I	**Master/Slave:** Input tells the 8206 whether it is a master (high) or a slave (low).
3	SEDCU	I	**Single EDC Unit:** Input tells the master whether it is operating as a single 8206 (low) or as the master in a multi-8206 system (high). Not used in slaves.
60	V_{CC}	I	**Power Supply:** +5V
26	V_{SS}	I	**Logic Ground**
43	V_{SS}	I	**Output Driver Ground**

FUNCTIONAL DESCRIPTION

The 8206 Error Detection and Correction Unit provides greater memory system reliability through its ability to detect and correct memory errors. It is a single chip device that can detect and correct all single bit errors and detect all double bit and some higher multiple bit errors. Some other odd multiple bit errors (e.g., 5 bits in error) are interpreted as single bit errors, and the CE flag is raised. While some even multiple bit errors (e.g., 4 bits in error) are interpreted as no error, most are detected as double bit errors. This error handling is a function of the number of check bits used by the 8206 (see Figure 2) and the specific Hamming code used. Errors in check bits are not distinguished from errors in a word.

A single 8206 handles 8 or 16 bits of data, and up to 5 8206's can be cascaded in order to handle data paths of 80 bits. For a single 8206 8 bit system, the DI_{8-15}, DO/WDI_{8-15} and BM_1 inputs are grounded. See the Multi-Chip systems section for information on 24-80 bit systems.

The 8206 has a "flow through" architecture. It supports two kinds of error correction architecture: 1) Flow-through, or correct-always; and 2) Parallel, or check-only. There are two separate 16-pin busses, one to accept data from the RAM (DI) and the other to deliver corrected data to the system bus (DO/WDI). The logic is entirely combinatorial during a read cycle. This is in contrast to an architecture with only one bus, with bidirectional bus drivers that must first read the data and then be turned around to output the corrected data. The latter architecture typically requires additional hardware (latches and/or transceivers) and may be slower in a system due to timing skews of control signals.

DATA WORD BITS	CHECK BITS
8	5
16	6
24	6
32	7
40	7
48	8
56	8
64	8
72	8
80	8

Figure 2: NUMBER OF CHECK BITS USED BY 8206

READ CYCLE

With the R/W pin high, data is received from the RAM outputs into the DI pins where it is optionally latched by the STB signal. Check bits are generated from the data bits and compared to the check bits read from the RAM into the CBI pins. If an error is detected the ERROR flag is activated and the correctable error flag (CE) is used to inform the system whether the error was correctable or not. With the BM inputs high, the word appears corrected at the DO pins if the error was correctable, or unmodified if the error was uncorrectable.

If more than one 8206 is being used, then the check bits are read by the master. The slaves generate a partial parity output (PPO) and pass it to the master. The master 8206 then generates and returns the syndrome to the slaves (SYO) for correction of the data.

The 8206 may alternatively be used in a "check-only" mode with the CRCT pin left high. With the correction facility turned off, the propagation delay from memory outputs to 8206 outputs is significantly shortened. In this mode the 8206 issues an ERROR flag to the CPU, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, etc.

A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is made available to the system at the SYO_{0-7} pins. Error logging may be accomplished by latching the syndrome and the memory address of the word in error.

WRITE CYCLE

For a full write, in which an entire word is written to memory, the data is written directly to the RAM, bypassing the 8206. The same data enters the 8206 through the WDI pins where check bits are generated. The Byte Mark inputs must be low to tristate the DO drivers. The check bits, 5 to 8 in number, are then written to the RAM through the CBO pins for storage along with the data word. In a multi-chip system, the master writes the check bits using partial parity information from the slaves.

In a partial write, part of the data word is overwritten, and part is retained in memory. This is accomplished by performing a read-modify-write cycle. The complete old word is read into the 8206 and corrected, with the syndrome internally latched by R/W going low. Only that part of the word not to be modified is output onto the DO pins, as controlled by the Byte Mark inputs. That portion of the word to be overwritten is supplied by the system bus. The 8206 then calculates check bits for the new word, using the byte from the previous read and the new byte from the system bus, and writes them to the memory.

READ-MODIFY-WRITE CYCLES

Upon detection of an error the 8206 may be used to correct the bit in error in memory. This reduces the probability of getting multiple-bit errors in subsequent read cycles. This correction is handled by executing read-modify-write cycles.

The read-modify-write cycle is controlled by the R/W input. After (during) the read cycle, the system dynamic RAM controller or CPU examines the 8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller or CPU forces R/W low, telling the 8206 to latch the generated syndrome and drive the corrected check bits onto the CBO outputs. The corrected data is available on the DO pins. The DRAM controller then writes the corrected data and corresponding check bits into memory.

The 8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the 8206 latches are used to hold the data and check bits from the read cycle to be used in the following write cycle. The WD8207 Advanced Dynamic RAM controller allows read-modify-write cycles in one memory cycle. See the System Environment section.

INITIALIZATION

A memory system operating with ECC requires some form of initialization at system power-up in order to set valid data and check bit information in memory. The 8206 supports memory initialization by the write zero function. By activating the WZ pin, the 8206 will write a data pattern of zeros and the associated check bits in the current write cycle. By thus writing to all memory at power-up, a controller can set memory to valid data and check bits. Massive memory failure, as signified by both data and check bits all ones or zeros, will be detected as an uncorrectable error.

MULTI-CHIP SYSTEMS

A single 8206 handles 8 or 16 bits of data and 5 or 6 check bits, respectively. Up to 5 8206's can be cascaded for 80 bit memories with 8 check bits.

When cascaded, one 8206 operates as a master, and all others as slaves. As an example, during a read cycle in a 32 bit system with one master and one

slave, the slave calculates parity on its portion of the word — "partial parity" — and presents it to the master through the PPO pins. The master combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate the syndrome. The syndrome is then returned by the master to the slave for error correction. In systems with more than one slave the above description continues to apply, except that the partial parity outputs of the slaves must be XOR'd externally. Figure 3 shows the necessary external logic for multi-chip systems. Write and read-modify-write cycles are carried out analogously. See the System Operation section for multi-chip wiring diagrams.

There are several pins used to define whether the 8206 will operate as a master or a slave. Tables 2 and 3 illustrate how these pins are tied.

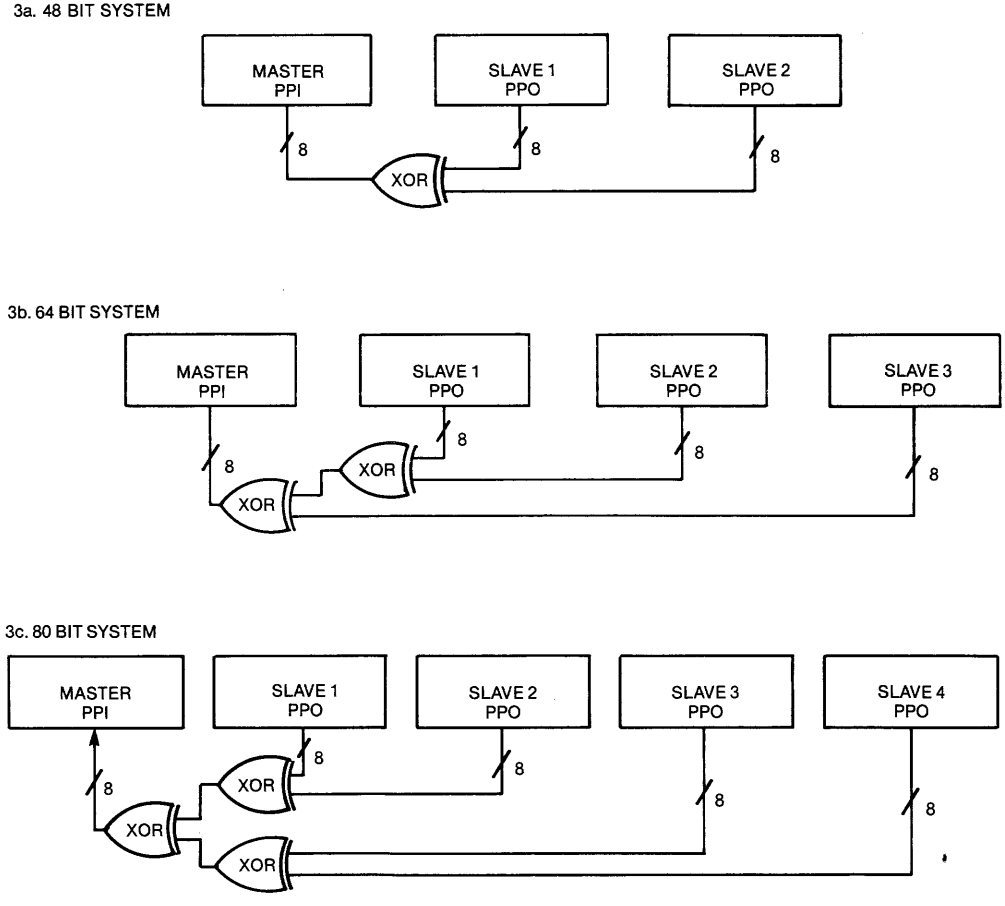


Figure 3. EXTERNAL LOGIC FOR MULTI-CHIP SYSTEMS

Table 2. MASTER/SLAVE PIN ASSIGNMENTS

PIN NO.	PIN NAME	MASTER	SLAVE 1	SLAVE 2	SLAVE 3	SLAVE 4
4	M/S	+5V	Gnd	Gnd	Gnd	Gnd
3	SEDCU	+5V	+5V	+5V	+5V	+5V
13	PPI_0/POS_0	PPI	Gnd	+5V	Gnd	+5V
14	PPI_1/POS_1	PPI	Gnd	Gnd	+5V	+5V
15	PPI_2/NSL_0	PPI	*	+5V	+5V	+5V
16	PPI_3/NSL_1	PPI	*	+5V	+5V	+5V

* See Table 3.

NOTE:
Pins 13, 14, 15, 16 have internal pull-up resistors and may be left as N.C. where specified as connecting to +5V.

Table 3. NSL PIN ASSIGNMENTS FOR SLAVE 1

	NUMBER OF SLAVES			
PIN	1	2	3	4
PPI_2/NSL_0	Gnd	+5V	Gnd	+5V
PPI_3/NSL_1	Gnd	Gnd	+5V	+5V

The timing specifications for multi-chip systems must be calculated to take account of the external XOR gating in 3, 4, and 5-chip systems. Let tXOR be the delay for a single external TTL XOR gate. Then the following equations show how to calculate the relevant timing parameters for 2-chip (n = 0), 3-chip (n = 1), 4-chip (n = 2), and 5-chip (n = 2) systems:

Data-in to corrected data-out (read cycle) =
TDVSV + TPVSV + TSVQV + ntXOR

Data-in to error flag (read cycle) =
TDVSV + TPVEV + ntXOR

Data-in to correctable error flag (read cycle) =
TDVSV + TPVSV + TSVCV + ntXOR

Write data to check-bits valid (full write cycle) =
TQVQV + TPVSV + ntXOR

Data-in to check-bits valid (read-mod-write cycle) =
TDVSV + TPVSV + TSVQV + TQVQV + TPVSV + 2ntXOR

Data-in to check-bits valid (non-correcting read-modify-write cycle) =
TDVQU + TQVQV + TPVSV + ntXOR

HAMMING CODE

The 8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all 8206's in parallel. No 8206 requires more time for propagation through logic levels than any other one, and hence no one device becomes a bottleneck in the parity operation. However, one or two levels of external TTL XOR gates are required in systems with three to five chips. The code appears in Table 4. The check bits are derived from the table by XORing or XNORing together the bits indicated by 'X's in each row corresponding to a check bit. For example, check bit 0 in the MASTER for data word 1000110101101011 will be "0." It should be noted that the 8206 will detect the gross-error condition of all lows or all highs.

Error correction is accomplished by identifying the bad bit and inverting it. Table 4 can also be used as an error syndrome table by replacing the 'X's with '1's. Each column then represents a different syndrome word, and by locating the column corresponding to a particular syndrome the bit to be corrected may be identified. If the syndrome cannot be located then the error cannot be corrected. For example, if the syndrome word is 00110111, the bit to be corrected is bit 5 in the slave one data word (bit 21).

The syndrome decoding is also summarized in Table 5, which can be used for error logging. By finding the appropriate syndrome word (starting with bit zero, the least significant bit), the result is either: 1) no error; 2) an identified (correctable) single bit error; 3) a double bit error; or 4) a multi-bit uncorrectable error.

Table 4. MODIFIED HAMMING CODE CHECK BIT GENERATION

Check bits are generated by XOR'ing (except for the CB0 and CB1 data bits, which are XNOR'ed in the Master) the data bits in the rows corresponding to the check bits. Note there are 6 check bits in a 16-bit system, 7 in a 32-bit system, and 8 in 48-or-more-bit systems.

BYTE NUMBER	0								1								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	XNOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	XNOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
CB5 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
CB6 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
DATA BITS	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	
	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	

16 BIT OR MASTER

2								3								OPERATION
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	XOR
X	X	X	—	—	X	—	X	X	X	—	—	—	—	—	X	XOR
—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	XOR
X	X	—	—	X	—	X	X	X	—	—	X	X	—	—	—	XOR
X	X	—	—	X	X	X	X	—	—	—	—	X	—	X	—	XOR
—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	XOR
—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	XOR
1	1	1	1	2	2	2	2	2	2	2	2	2	2	3	3	
6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	

SLAVE #1

BYTE NUMBER	4								5								6								7								8								9								OPERATION
BIT NUMBER	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	
CB0 =	X	X	—	X	—	X	X	—	X	—	—	X	—	X	—	—	X	—	X	X	—	—	X	—	—	X	X	X	—	X	X	—	—	X	X	—	—	X	—	—	—	X	X	—	—	X	—	—	XOR
CB1 =	X	—	X	—	—	X	—	X	—	X	—	X	X	—	X	—	—	X	X	—	—	—	X	—	—	X	X	X	—	X	X	X	—	—	X	X	—	—	—	—	—	—	X	X	—	—	—	—	XOR
CHECK CB2 =	—	X	X	—	X	—	X	X	—	—	X	—	X	—	—	X	—	X	X	X	—	X	X	—	X	—	—	X	—	X	—	—	—	X	—	X	—	—	X	—	—	X	—	X	—	—	X	—	XOR
CB3 =	X	X	X	X	X	—	—	—	X	X	X	—	—	—	—	—	X	—	—	—	X	X	—	—	X	X	—	—	—	X	X	—	—	X	X	X	—	—	—	—	X	X	—	—	X	—	—	—	XOR
BITS CB4 =	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	—	—	X	X	X	X	X	—	—	—	—	—	X	X	X	—	X	X	—	—	—	X	X	X	X	—	—	X	—	—	X	XOR
CB5 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	X	—	X	X	X	X	—	X	—	—	—	X	—	—	—	X	XOR
CB6 =	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	—	—	X	X	X	X	—	—	—	X	—	X	—	—	XOR
CB7 =	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	—	—	—	—	—	—	—	—	X	X	X	X	X	X	X	X	XOR
DATA BITS	3	3	3	3	3	3	3	3	4	4	4	4	4	4	4	4	4	4	5	5	5	5	5	5	5	5	5	5	6	6	6	6	6	6	6	6	7	7	7	7	7	7	7	7					
	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9	

SLAVE #2 | SLAVE #3 | SLAVE #4

Table 5. SYNDROME DECODING

Syndrome Bits 7	6	5	4	0 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 0 1 1 0 1 1 0 0 1 1 2 3 0	0 0 0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1 1
0	0	0	0	N	CB0 CB1 D CB2 D D 18 CB3 D D 0 D 1 2 D
0	0	0	1	CB4	D D 5 D 6 7 D D 3 16 D 4 D D 17
0	0	1	0	CB5	D D 11 D 19 12 D D 8 9 D 10 D D 67
0	0	1	1	D	13 14 D 15 D D 21 20 D D 66 D 22 23 D
0	1	0	0	CB6	D D 25 D 26 49 D D 48 24 D 27 D D 50
0	1	0	1	D	52 55 D 51 D D 70 28 D D 65 D 53 54 D
0	1	1	0	D	29 31 D 64 D D 69 68 D D 32 D 33 34 D
0	1	1	1	30	D D 37 D 38 39 D D 35 71 D 36 D D U
1	0	0	0	CB7	D D 43 D 77 44 D D 40 41 D 42 D D U
1	0	0	1	D	45 46 D 47 D D 74 72 D D U D 73 U D
1	0	1	0	D	59 75 D 79 D D 58 60 D D 56 D U 57 D
1	0	1	1	63	D D 62 D U U D D U U D 61 D D U
1	1	0	0	D	U U D U D D U 76 D D U D U U D
1	1	0	1	78	D D U D U U D D U U D U D D U
1	1	1	0	U	D D U D U U D D U U D U D D U
1	1	1	1	D	U U D U D D U U D D U D U U D

N = No Error
CBX = Error in Check Bit X
X = Error in Data Bit X
D = Double Bit Error
U = Uncorrectable Multi-Bit Error

SYSTEM ENVIRONMENT

The 8206 interface to a typical 32 bit memory system is illustrated in Figure 4. For larger systems, the partial parity bits from slaves two to four must be XOR'ed externally, which calls for one level of XOR gating for three 8206's and two levels for four or five 8206's.

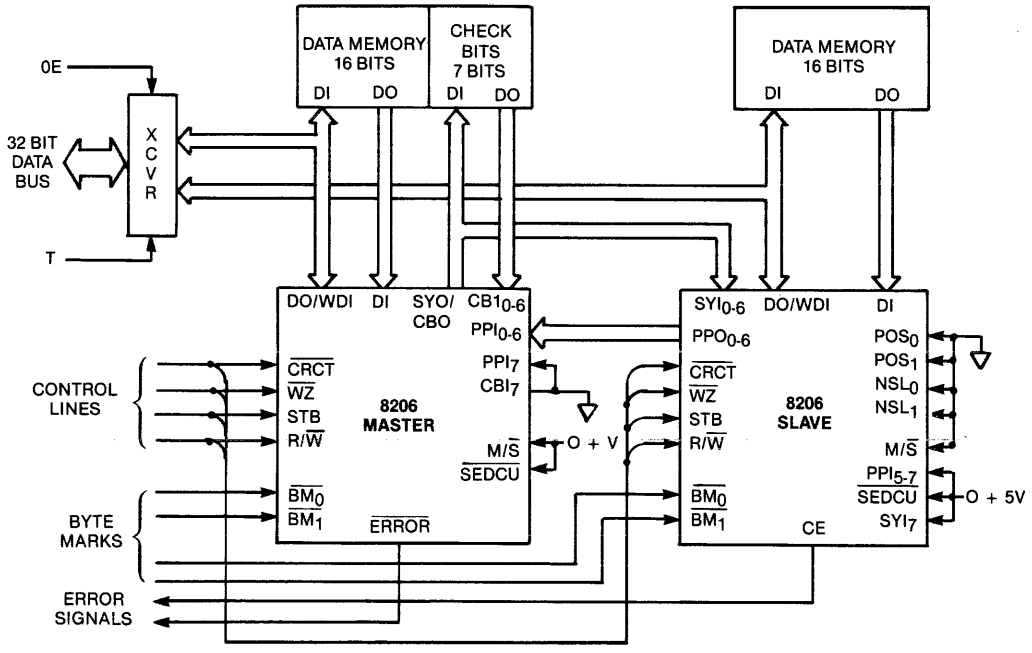


Figure 4. 32-BIT 8206 SYSTEM INTERFACE

The 8206 is designed for direct connection to the WD8207 Advanced Dynamic RAM Controller, due to be sampled in the first quarter of 1983. The 8207 has the ability to perform dual port memory control and Figure 5 illustrates a highly integrated dual port RAM implementation using the 8206 and 8207. The 8206/8207 combination permits such features as automatic scrubbing (correcting errors in memory during refresh), extending RAS and CAS timings for Read-Modify-Writes in single memory cycles, and automatic memory initialization upon reset. Together these two chips provide a complete dual-port, error-corrected dynamic RAM subsystem.

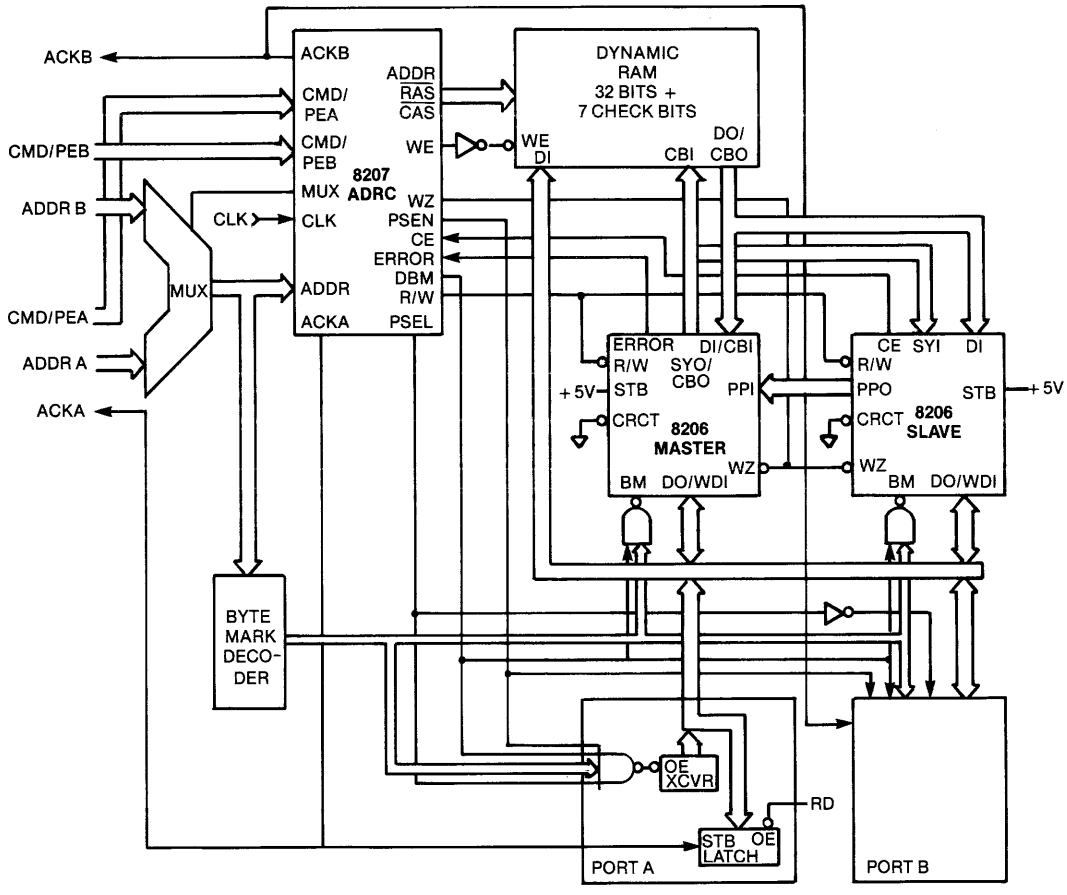


Figure 5. DUAL PORT RAM SUBSYSTEM WITH 8206/8207 (32-BIT BUS)

MEMORY BOARD TESTING

The 8206 lends itself to straightforward memory board testing with a minimum of hardware overhead. The following is a description of four common test modes and their implementation.

Mode 0 — Read and write with error correction.
Implementation: This mode is the normal 8206 operating mode.

Mode 1 — Read and write data with error correction disabled to allow test of data memory.
Implementation: This mode is performed with CRCT deactivated.

Mode 2 — Read and write check bits with error correction disabled to allow test of check bits memory.
Implementation: Any pattern may be written into the check bits memory by judiciously choosing the proper data word to generate the desired check bits, through the use of the 8206 Hamming code. To read out the check bits it is first necessary to fill the data memory with all zeros, which may be done by activating WZ and incrementing memory addresses with WE to the check bits memory held inactive, and then performing ordinary reads. The check bits will then appear directly at the SYO outputs, with bits CB0 and CB1 inverted.

Mode 3 — Write data, without altering or writing check bits, to allow the storage of bit combinations to cause error correction and detection.
Implementation: This mode is implemented by writing the desired word to memory with WE to the check bits array held inactive.

PACKAGE

The 8206 is packaged in a 68-pin, leadless JEDEC type A hermetic chip carrier. Figure 6 illustrates the package, and Figure 7 is the pinout.

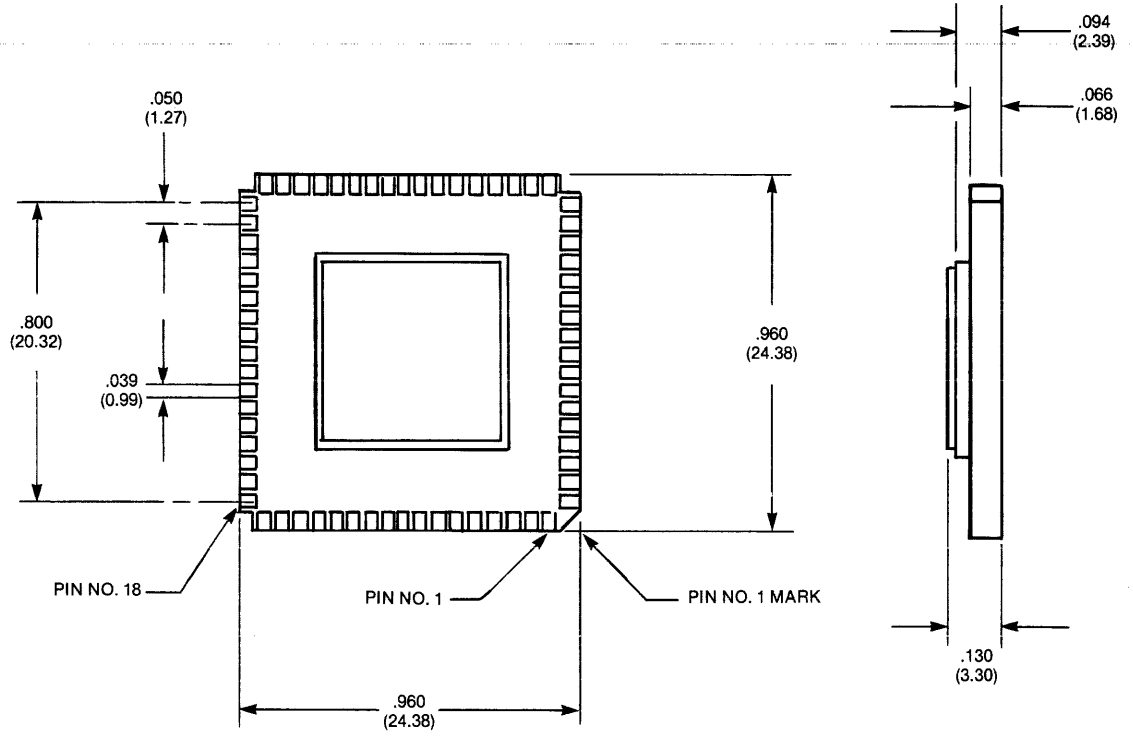


Figure 6. 8206 JEDEC TYPE A PACKAGE

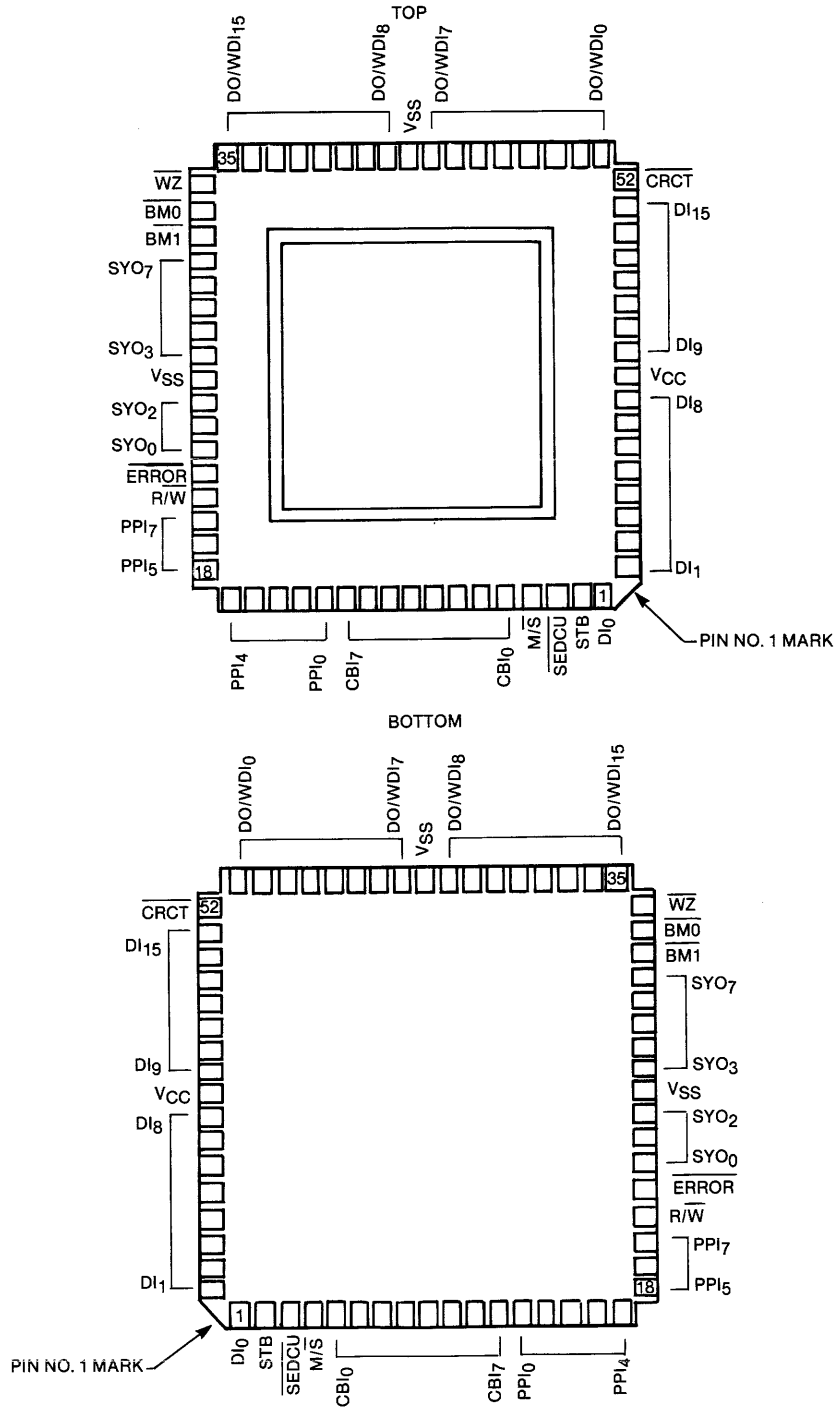


Figure 7. 8206 PINOUT DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Ambient Temperature Under Bias ..... 0°C to 70°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin
With Respect to Ground ..... −0.5V to +7V
Power Dissipation ..... 2.5 Watts

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

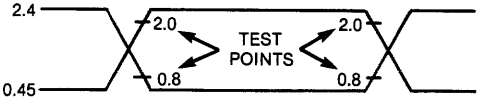
D.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = 5.0V ± 10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{CC}	Power Supply Current — Single 8206 or Slave #1 — Master in Multi-Chip or Slaves #2, 3, 4		 270 230	 mA mA	
V_{IL}[1]	Input Low Voltage	−0.5	0.8	V	
V_{IH}[1]	Input High Voltage	2.0	V_{CC} + 0.5V	V	
V_{OL}	Output Low Voltage — DO — All Others	 	 0.4 0.4	 V V	 I_{OL} = 8mA I_{OL} = 2.0mA
V_{OH}	Output High Voltage — DO, CBO — All Other Outputs	 2.6 2.4	 	 V V	 I_{OH} = −2mA I_{OH} = 0.4mA
I_{LO}	I/O Leakage Current — PPI_4/CE — DO/WDI_{0-15}	 	 ± 20 ± 10	 μA μA	 0.45V ≤ $V_{I/O}$ ≤ V_{CC}
I_{LI}	Input Leakage Current — $PPI_{0-3, 5-7}$, CBI_{6-7}, SEDCU[2] — All Other Input Only Pins	 	 ± 20 ± 10	 μA μA	 0V ≤ V_{IN} ≤ V_{CC}

NOTES:

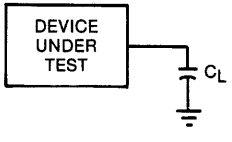
1. SEDCU (pin 3) and M/S (pin 4) are device strapping options and should be tied to V_{CC} or GND. V_{IH} min = V_{CC} − 0.5V and V_{IL} max = 0.5V.
2. PPI_{0-7} (pins 13-20) and CBI_{6-7} (pins 11, 12) have internal pull-up resistors and if left unconnected will be pulled to V_{CC}.

A.C. TESTING INPUT, OUTPUT WAVEFORM



A.C. TESTING INPUTS ARE DRIVEN AT 2.4V FOR A LOGIC 1 and 0.45V FOR A LOGIC 0. TIMING MEASUREMENTS ARE MADE AT 2.0V FOR A LOGIC 1 AND 0.8V FOR A LOGIC 0.

A.C. TESTING LOAD CIRCUIT



C_L INCLUDES JIG CAPACITANCE

A.C. CHARACTERISTICS (T_A = 0°C to 70°C, V_{CC} = +5V ± 10%, V_{SS} = 0V, C_L = 100pF; all times are in nsec.)

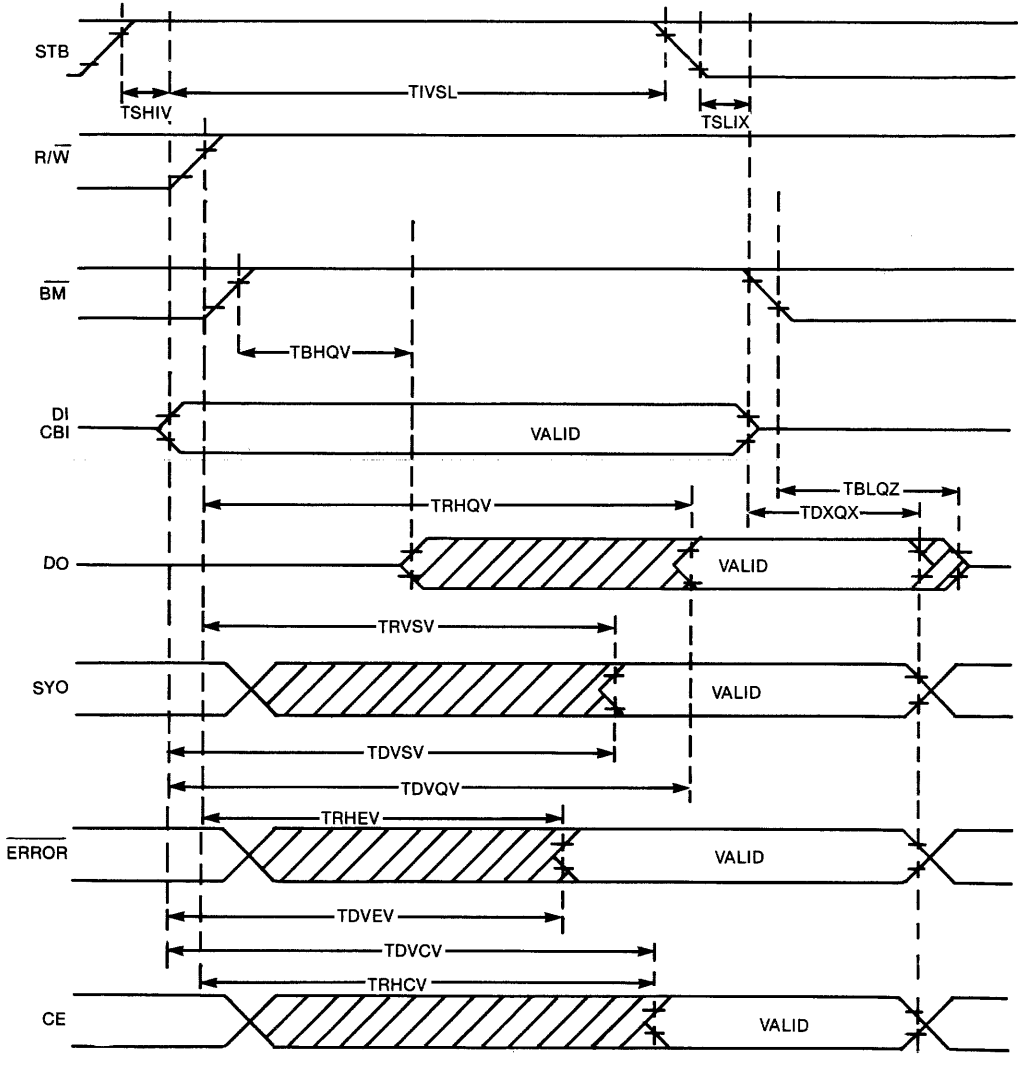
SYMBOL	PARAMETER	8206		8206-8		NOTES
		MIN.	MAX.	MIN.	MAX.	
TRHEV	ERROR Valid from R/W↑		25		34	
TRHCV	CE Valid from R/W↑ (Single 8206)		44		59	
TRHQV	Corrected Data Valid from R/W↑		54		66	1
TRVSV	SYO/CBO/PPO Valid from R/W		42		56	1
TDVEV	ERROR Valid from Data/Check Bits In		52		70	
TDVCV	CE Valid from Data/Check Bits In		70		94	
TDVQV	Corrected Data Valid from Data/Check Bits In		67		90	
TDVSV	SYO/PPO Valid from Data/Check Bits In		55		74	
TBHQV	Corrected Data Access Time		37		43	
TDXQX	Hold Time from Data/Check Bits In	0		0		1
TBLQZ	Corrected Data Float Delay	0	28	0	38	1
TSHIV	STB High to Data/Check Bits in Valid	30		40		2
TIVSL	Data/Check Bits In to STB↓ Set-up	5		5		
TSLIX	Data/Check Bits In from STB↓ Hold	25		30		
TPVEV	ERROR Valid from Partial Parity In		30		40	
TPVQV	Corrected Data (Master) from Partial Parity In		61		76	1
TPVSV	Syndrome/Check Bits Out from Partial Parity In		43		51	1
TSVQV	Corrected Data (Slave) Valid from Syndrome		51		69	
TSVCV	CE Valid from Syndrome (Slave number 1)		48		65	
TQVQV	Check Bits/Partial Parity Out from Write Data In		64		80	1
TRHSX	Check Bits/Partial Parity Out from R/W, WZ Hold	0		0		1
TRLSX	Syndrome Out from R/W Hold	0		0		
TQXQX	Hold Time from Write Data In	0		0		1
TSVRL	Syndrome Out to R/W↓ Set-up	17		22		
TDVRL	Data/Check Bits In to R/W Set-up	39		46		1
TDVQU	Uncorrected Data Out from Data In		32		43	
TTVQV	Corrected Data Out from CRCT↓		30		40	
TWLQL	WZ↓ to Zero Out		30		40	
TWHQX	Zero Out from WZ↑ Hold	0		0		

NOTES:

1. A.C. Test Levels for CBO and DO are 2.4V and 0.8V.
2. T_{SHIV} is required to guarantee output delay timings: T_{DVEV}, T_{DVCV}, T_{DVSV}. T_{SHIV} + T_{IVSL} guarantees a min STB pulse width of 35 ns (45 ns for the 8206-8).

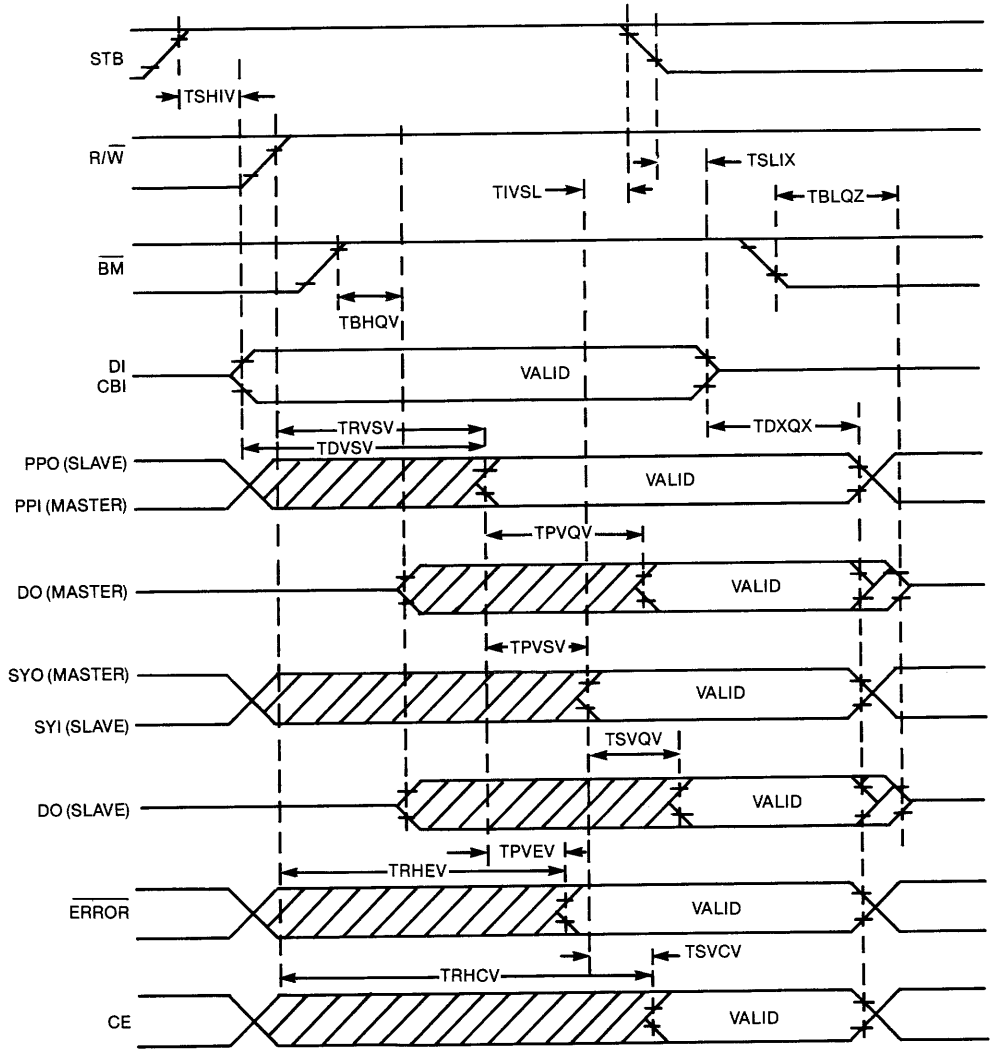
WAVEFORMS

READ — 16 BIT ONLY



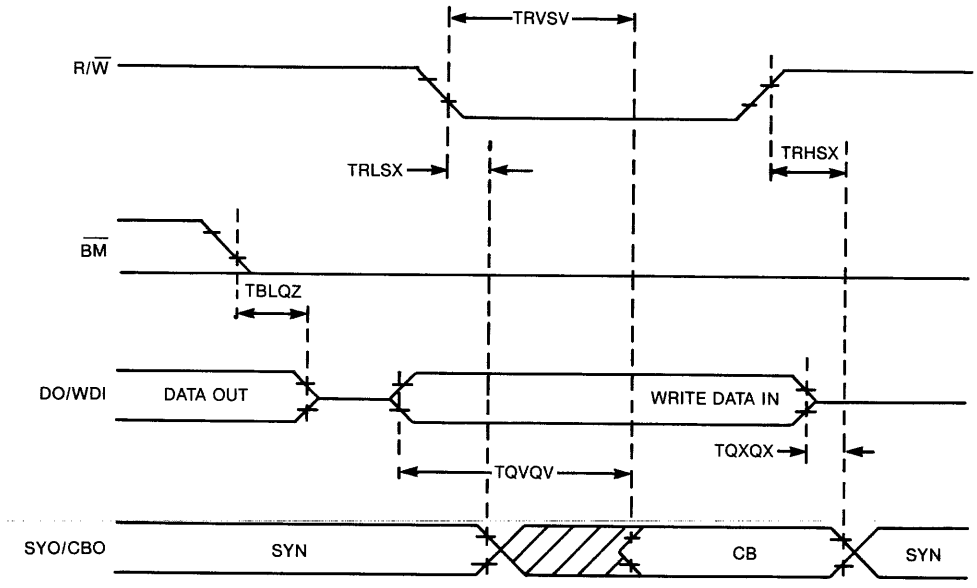
WAVEFORMS (Continued)

READ — MASTER/SLAVE

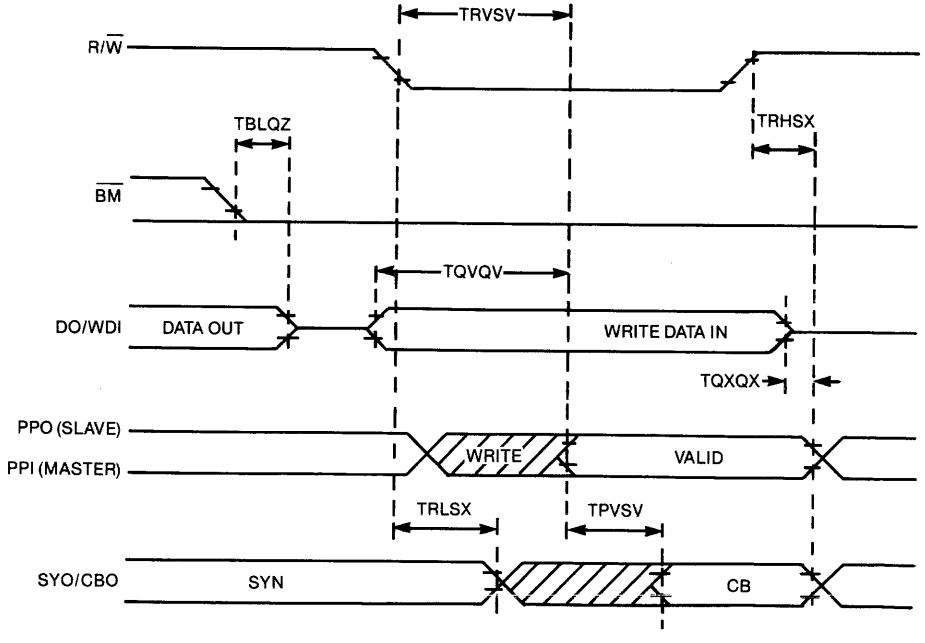


WAVEFORMS (Continued)

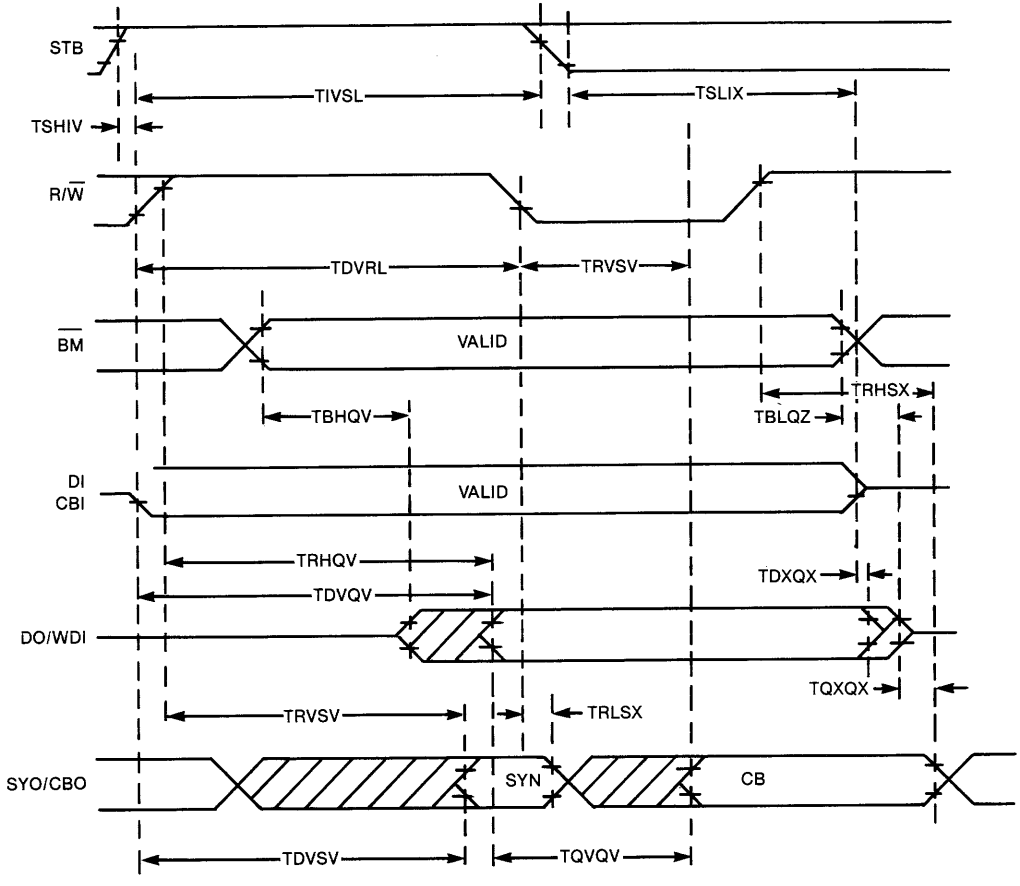
FULL WRITE — 16 BIT ONLY



FULL WRITE — MASTER/SLAVE

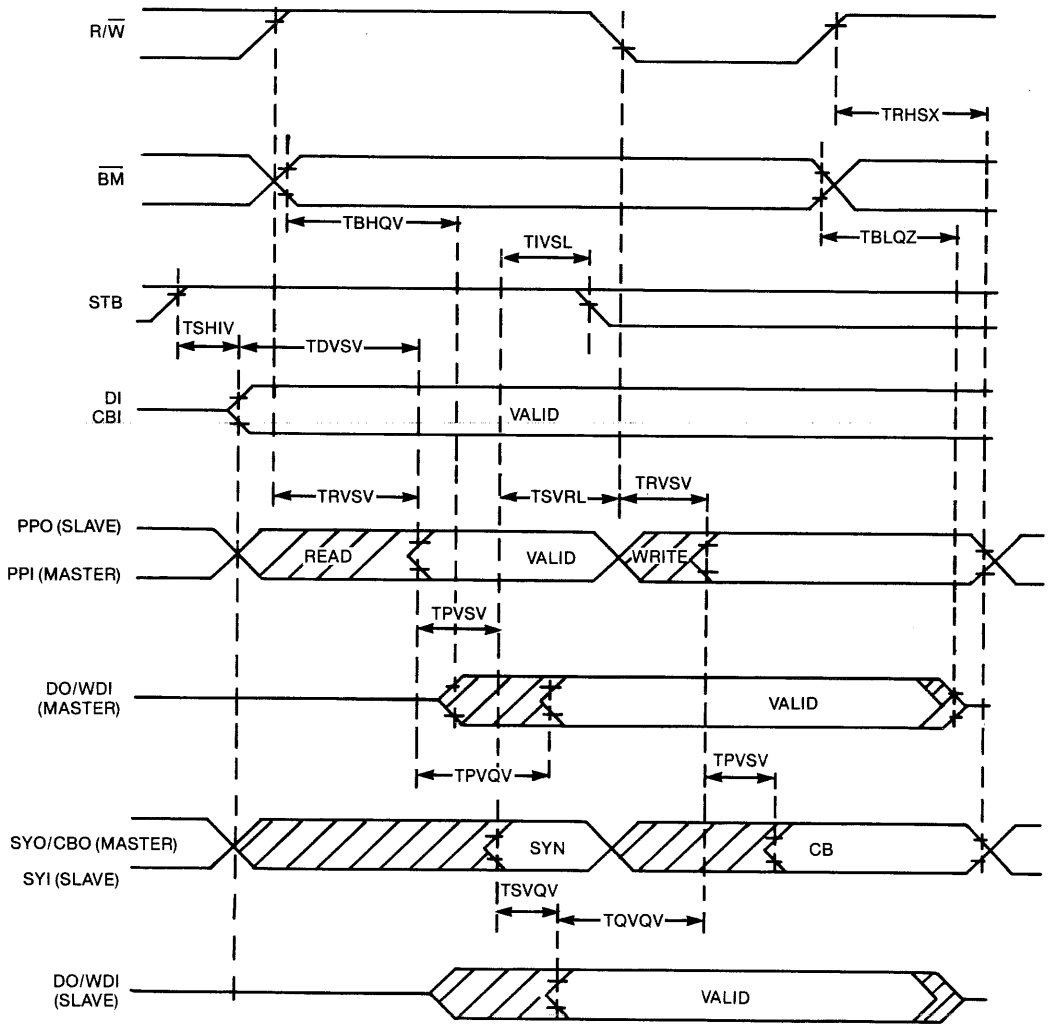


READ MODIFY WRITE — 16 BIT ONLY



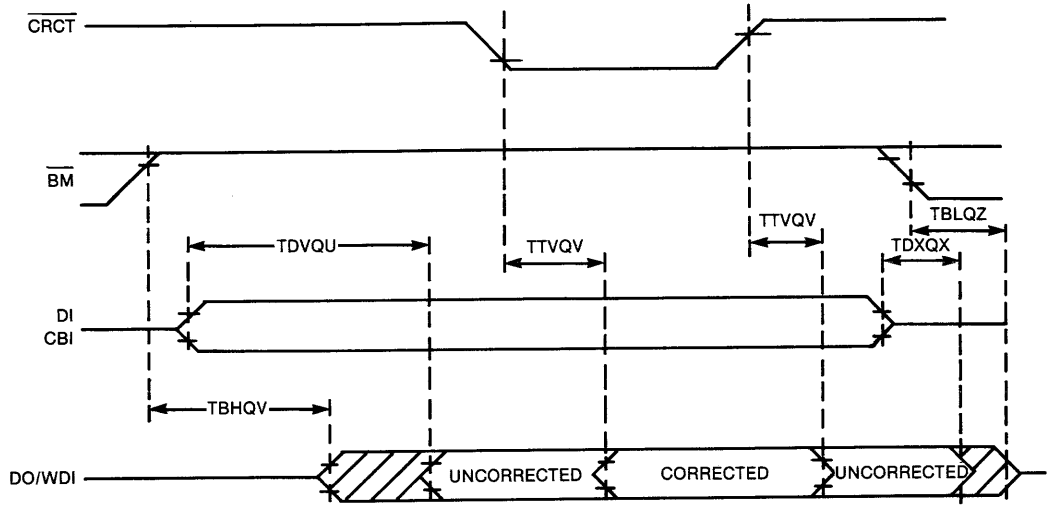
WAVEFORMS (Continued)

READ MODIFY WRITE — MASTER/SLAVE

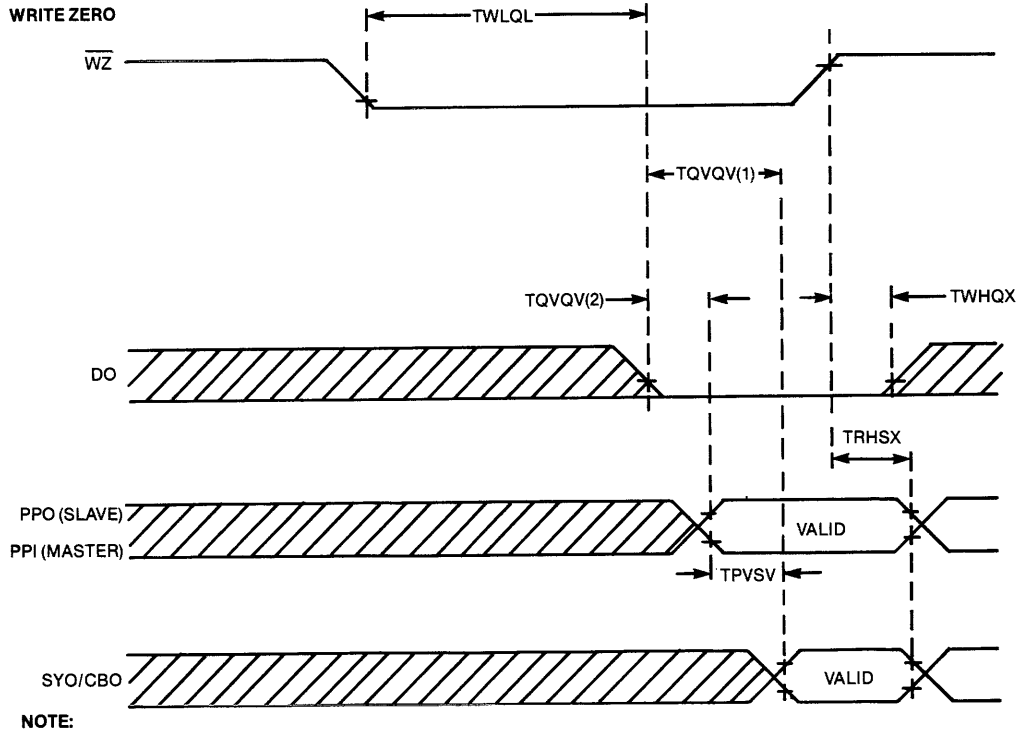


WAVEFORMS (Continued)

NON-CORRECTING READ



WRITE ZERO



NOTE:
(1): 16 BIT ONLY
(2): MASTER/SLAVE

See page 481 for ordering information.

Printed in U.S.A.

PRELIMINARY

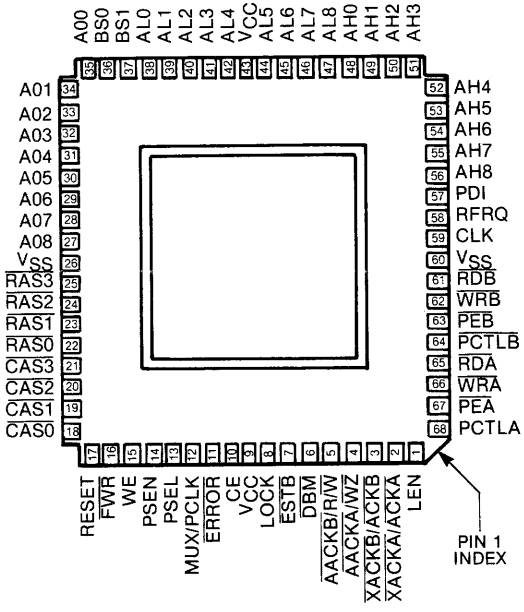
WD8207 Advance Dynamic RAM Controller

FEATURES

- PROVIDES ALL SIGNALS NECESSARY TO CONTROL 16K, 64K AND 256K DYNAMIC RAMS
- DIRECTLY ADDRESSES AND DRIVES UP TO 2 MEGABYTES WITHOUT EXTERNAL DRIVERS
- SUPPORTS SINGLE AND DUAL-PORT CONFIGURATIONS
- AUTOMATIC RAM INITIALIZATION IN ALL MODES
- FIVE PROGRAMMABLE REFRESH MODES
- TRANSPARENT MEMORY SCRUBBING IN ECC MODE
- DATA TRANSFER ACKNOWLEDGE SIGNALS FOR EACH PORT
- PROVIDES SIGNALS TO DIRECTLY CONTROL THE WD8206 ERROR DETECTION AND CORRECTION UNIT
- SUPPORTS SYNCHRONOUS OR ASYNCHRONOUS OPERATION ON EITHER PORT
- SINGLE +5V SUPPLY

DESCRIPTION

The WD8207 is a 68-pin leadless JEDEC type A hermetic chip carrier. The WD8207 Advanced Dynamic RAM Controller (ADRC) is a high-performance, systems-oriented, Dynamic RAM controller that is designed to easily interface 16K, 64K and 256K Dynamic RAMs microprocessor Systems. A dual-port interface allows two different busses to independently access memory. When configured with a WD8206 Error Detection and Correction Unit the WD8207 supplies the necessary logic for designing large error-corrected memory arrays. This combination provides automatic memory initialization and transparent memory error scrubbing.



PIN DESIGNATION

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
1	ADDRESS LATCH ENABLE	LEN	O	In two-port configurations, when port A is running with Status interface mode, this output replaces the ALE signal from the system bus controller and generates an address latch enable signal which provides optimum setup and hold timing for the WD8207.
2	TRANSFER ACKNOWLEDGE PORT A/ACKNOWLEDGE PORT A	$\overline{\text{XACK A}}$/ $\overline{\text{ACKA}}$	O	In non-ECC mode, this pin is $\overline{\text{XACKA}}$ and indicates that data on the bus is valid during a read cycle or that data may be removed from the bus during a write cycle for Port A. $\overline{\text{XACKA}}$ is a Multibus-compatible signal. In ECC mode, this pin is $\overline{\text{ACKA}}$ which can be configured, depending on the programming of the X program bit, as an XACK or AACK strobe. The SA programming bit determines whether AACK will be early or late.
3	TRANSFER ACKNOWLEDGE PORT B/ACKNOWLEDGE PORT B	$\overline{\text{XACKB}}$/ $\overline{\text{ACKB}}$	O	In non-ECC mode, this pin is $\overline{\text{XACKB}}$ and indicates that data on the bus is valid during a read cycle or that data may be removed from the bus during a write cycle for Port B. $\overline{\text{XACKB}}$ is a Multibus-compatible signal. In ECC mode, this pin is $\overline{\text{ACKB}}$ which can be configured, depending on the programming of the X program bit, as an XACK or AACK strobe. The SB programming bit determines whether AACK will be early or late.
4	ADVANCED ACKNOWLEDGE PORT A/WRITE ZERO	$\overline{\text{AACK A}}$/ $\overline{\text{WZ}}$	O	In non-ECC mode, this pin is $\overline{\text{AACKA}}$ and indicates that the processor may continue processing and that data will be available when required. This signal is optimized for the system by programming the SA program bit for synchronous or asynchronous operation. After a RESET, this signal will cause the WD8206 to force the data to all zeros and generate the appropriate check bits.
5	ADVANCED ACKNOWLEDGE PORT B/READ/WRITE	$\overline{\text{AACKB}}$/ R/$\overline{\text{W}}$	O	In non-ECC mode, this pin is $\overline{\text{AACKB}}$ and indicates that the processor may continue processing and that data will be available when required. This signal is optimized for the system by programming the SB program bit for synchronous or asynchronous operation. This signal causes the WD8206 EDCU to latch the syndrome and error flags and generate check bits.
6	DISABLE BYTE MARKS	$\overline{\text{DBM}}$	O	This is an ECC control output signal indicating that a read or refresh cycle is occurring. This output forces the byte address decoding logic to enable all WD8206 data output buffers. In ECC mode, this output is also asserted during memory initialization and the 8-cycle dynamic RAM wake-up exercise. In non-ECC mode synchronous local bus systems this signal may be used as an early WE output.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
7	ERROR STROBE	$\overline{ESTB}$	O	In ECC mode, this strobe is activated when an error is detected and allows a negative-edge triggered flip-flop to latch the status of the WD8206 EDCU CE for systems with error logging capabilities.
8	LOCK	LOCK	I	This input instructs the WD8207 to lock out the port not being serviced at the time LOCK was issued.
9	LOGIC POWER	V_{CC}	I	+5 Volts ± 10%. Supplies V_{CC} for the internal logic circuits.
43	DRIVER POWER		I	+5 Volts ± 10%. Supplies V_{CC} for the output drivers.
10	CORRECTABLE ERROR	CE	I	This is an ECC input from the WD8206 EDCU which instructs the WD8207 whether a detected error is correctable or not. A high input indicates a correctable error. A low input inhibits the WD8207 from activating WE to write the data back into RAM. This should be connected to the CE output of the WD8206.
11	ERROR	$\overline{ERROR}$	I	This is an ECC input from the WD8206 EDCU and instructs the WD8207 that an error was detected. This pin should be connected to the ERROR output of the WD8206.
12	MULTIPLEXER CONTROL/ PROGRAMMING CLOCK	MUX/ PCLK	O	Immediately after a RESET this pin is used to clock serial programming data into the PDI pin. In normal two-port operation, this pin is used to select memory addresses from the appropriate port. When this signal is high, port A is selected and when it is low, port B is selected. This signal may change state before the completion of a RAM cycle, but the RAM address hold time is satisfied.
13	PORT SELECT	PSEL	O	This signal is used to select the appropriate port for data transfer.
14	PORT SELECT ENABLE	PSEN	O	This signal used in conjunction with PSEL provides contention-free port exchange. When PSEN is low, PSEL is allowed to change state.
15	WRITE ENABLE	WE	O	This signal provides the dynamic RAM array the write enable input for a write operation.
16	FULL WRITE	$\overline{FWR}$	I	This is an ECC input signal that instructs the WD8207, in an ECC configuration, whether the present write cycle is normal RAM write (full write) or a RAM partial write (read-modify-write) cycle.
17	RESET	RESET	I	This signal causes all internal counters and state flip-flops to be reset and upon release of RESET, data appearing at the PDI pin is clocked in by the PCLK output. The states of the PDI, PCTLA, PCTLB and RFRQ pins are sampled by RESET going inactive and are used to program the WD8207.

PIN DESCRIPTION (CONT.)

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
18-21	COLUMN ADDRESS STROBE	$\overline{CAS0}$-$\overline{CAS3}$	O	These outputs are used by the dynamic RAM array to latch the column address, present on the AO0-8 pins. These outputs are selected by the BS0 and BS1 as programmed by program bits RB0 and RB1. These outputs drive the dynamic RAM array directly and need no external drivers.
22-25	ROW ADDRESS STROBE	$\overline{RAS0}$-$\overline{RAS3}$	O	These outputs are used by the dynamic RAM array to latch the row address, present on the AO0-8 pins. These outputs are selected by the BS0 and BS1 as programmed by program bits RB0 and RB1. These outputs drive the dynamic RAM array directly and need no external drivers.
26 60	DRIVER GROUND LOGIC GROUND	V_{SS}	I I	Provides a ground for the output drivers. Provides a ground for the remainder of the device.
35-27	ADDRESS OUTPUTS	AO0-AO8	O	These outputs are designed to provide the row and column addresses of the selected port to the dynamic RAM array. These outputs drive the dynamic RAM array directly and need no external drivers.
36, 37	BANK SELECT	BS0, BS1	I	These inputs are used to select one of four banks of the dynamic RAM array as defined by the program bits RB0 and RB1.
38-47	ADDRESS LOW	AL0-AL8	I	These lower-order address inputs are used to generate the row address for the internal address multiplexer.
48-56	ADDRESS HIGH	AH0-AH8	I	These higher-order address inputs are used to generate the column address for the internal address multiplexer.
57	PROGRAM DATA INPUT	PDI	I	This input programs the various user-selectable options in the WD8207. The PCLK pin shifts programming data into the PDI input from optional external shift registers. This pin may be strapped high or low to a default ECC (PCI = V_{CC}) or non-ECC (PDI = Ground) mode configuration.
58	REFRESH REQUEST	RFRQ	I	This input is sampled on the falling edge of RESET. If it is high at RESET, then the WD8207 is programmed for internal refresh request or external refresh request with failsafe protection. If it is low at RESET, then the WD8207 is programmed for external refresh without failsafe protection or burst refresh. Once programmed the RFRQ pin accepts signals to start an external refresh with failsafe protection or external refresh without failsafe protection or a burst refresh.
59	CLOCK	CLK	I	This input provides the basic timing for sequencing the internal logic.
61	READ FOR PORT B	$\overline{RDB}$	I	This pin is the read memory request command input for port B. This input also directly accepts the $\overline{S1}$ status line from processors.

PIN DESCRIPTION

PIN NUMBER	PIN NAME	SYMBOL	TYPE	FUNCTION
62	WRITE FOR PORT B	$\overline{WRB}$	I	This pin is the write memory request command input for port B. This input also directly accepts the $\overline{S0}$ status line from processors.
63	PORT ENABLE FOR PORT B	$\overline{PEB}$	I	This pin serves to enable a RAM cycle request for port B. It is generally decoded from the port address.
64	PORT CONTROL FOR PORT B	PCTLB	I	This pin is sampled on the falling edge of RESET. It configures port B to accept command inputs or processor status inputs. If low after RESET, the WD8207 is programmed to accept command, status inputs or Multibus commands. If high after RESET, the WD8207 is programmed to accept status inputs from compatible processors. The S2 status line should be connected to this input if programmed to accept specific status inputs. When programmed to accept commands it should be tied low or it may be used as a Multibus-compatible inhibit signal.
65	READ FOR PORT A	$\overline{RDA}$	I	This pin is the read memory request command input for port A. This input also directly accepts the $\overline{S1}$ status line from processors.
66	WRITE FOR PORT A	$\overline{WRA}$	I	This pin is the write memory request command input for port A. This input also directly accepts the $\overline{S0}$ status line from processors.
67	PORT ENABLE FOR PORT A	$\overline{PEA}$	I	This pin serves to enable a RAM cycle request for port A. It is generally decoded from the port address.
68	PORT CONTROL FOR PORT A	PCTLA	I	This pin is sampled on the falling edge of RESET. It configures port A to accept command inputs or processor status inputs. If low after RESET, the WD8207 is programmed to accept command inputs or Multibus commands. If high after RESET, the WD8207 is programmed to accept status inputs from processors. The $\overline{S2}$ status line should be connected to this input if programmed to accept status inputs. When programmed to accept commands or status, it should be tied low or it may be connected to INHIBIT when operating with Multibus.

GENERAL DESCRIPTION

The WD8207 Advanced Dynamic RAM Controller (ADRC) is a microcomputer peripheral device which provides the necessary signals to address, refresh and directly drive 16K, 64K and 256K dynamic RAMs. This controller also provides the necessary arbitration circuitry to support dual-port access of the dynamic RAM array.

The ADRC supports several microprocessor interface options including synchronous and asynchronous connection.

This device may be used with the WD8206 Error Detection and Correction Unit (EDCU). When used with the WD8206, the WD8207 is programmed in the Error Checking and Correction (ECC) mode. In this mode, the WD8207 provides all the necessary control signals for the WD8206 to perform memory initialization and transparent error scrubbing during refresh.

FUNCTIONAL DESCRIPTION

Processor Interface

The WD8207 has control circuitry for two ports each capable of supporting one of several possible bus structures. The ports are independently configurable allowing the dynamic RAM to serve as an interface between two different bus structures.

Each port of the WD8207 may be programmed to run synchronous or asynchronous to the processor clock. (See Synchronous/Asynchronous Mode) The WD8207 has been optimized to run synchronously with compatible microprocessors. When the WD8207 is programmed to run in asynchronous mode, the WD8207 inserts the necessary synchronization circuitry for the RD, WR, PE, and PCTL inputs.

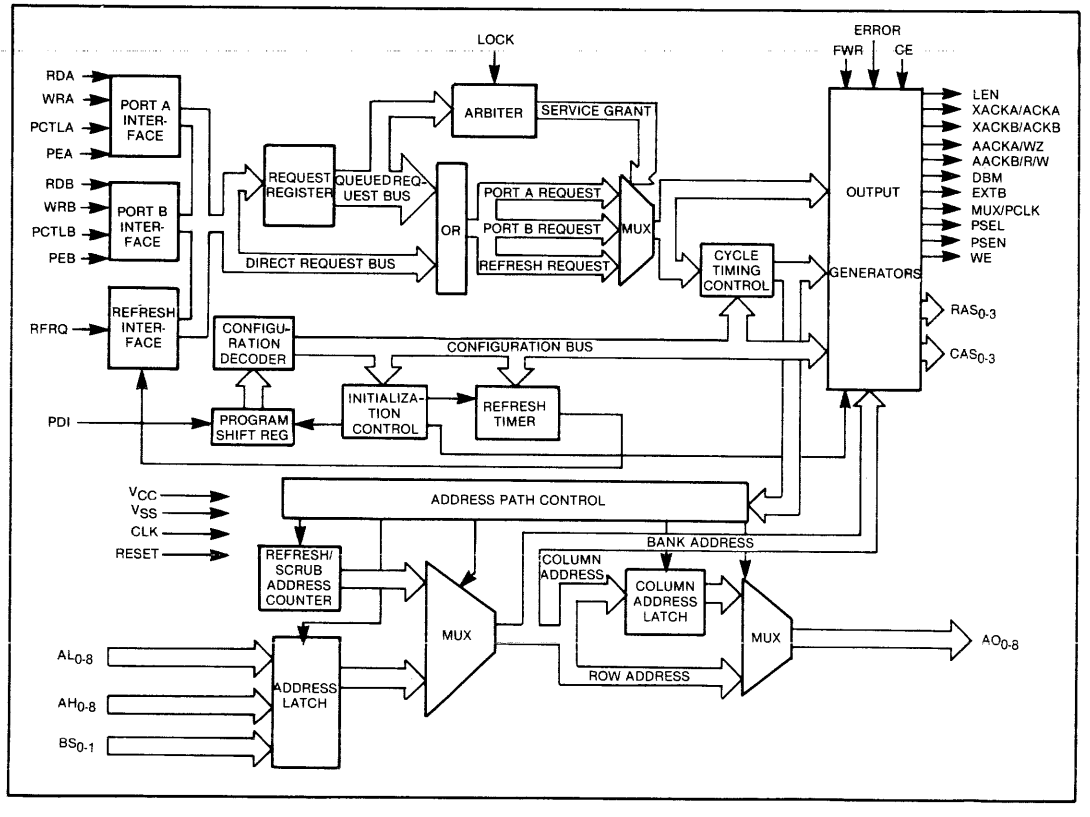
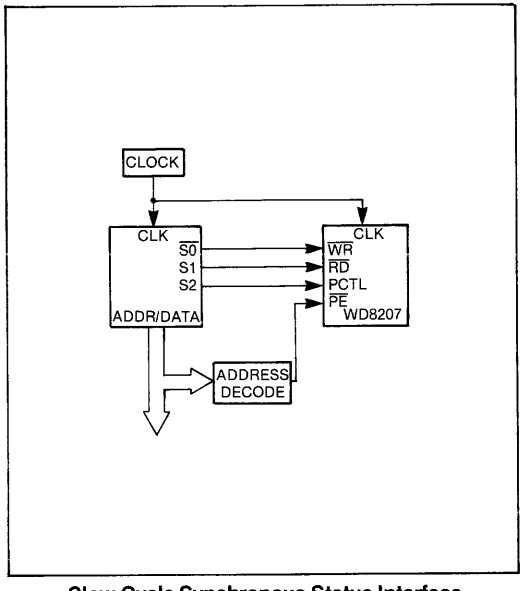


Figure 1. WD8207 BLOCK DIAGRAM

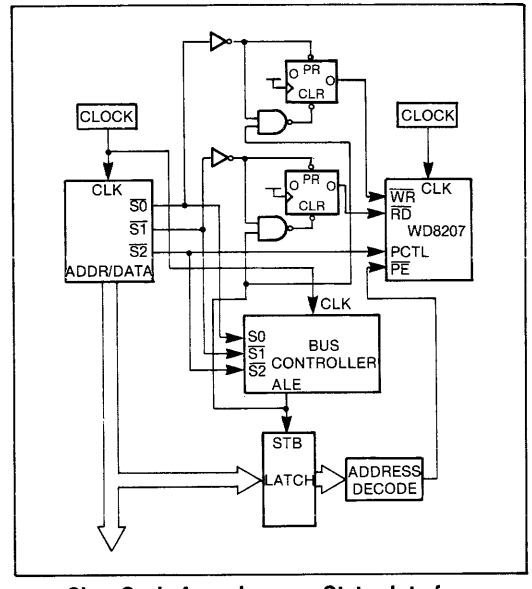
The WD8207 can also decode the status lines directly from various compatible microprocessors or can be programmed to receive read or write Multibus commands or commands from a bus controller. (See Status/Command Mode)

The WD8207 may be programmed to accept the clock of compatible microprocessors. The WD8207 adjusts its internal timing to allow for the different clock frequencies of these microprocessors. (See Microprocessor Clock Frequency Option)

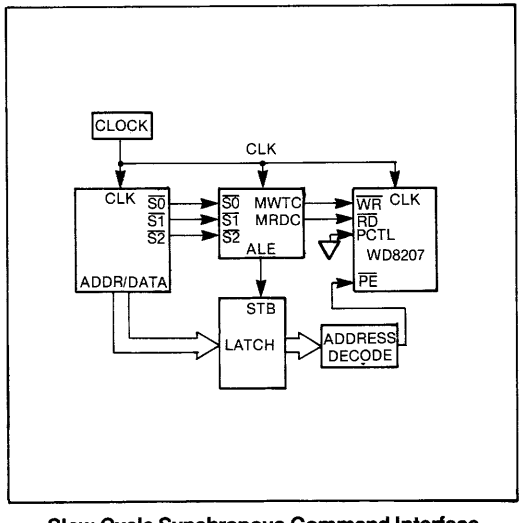
Figure 2 shows the different processor interfaces to the WD8207 using the synchronous or asynchronous mode and status or command interface.



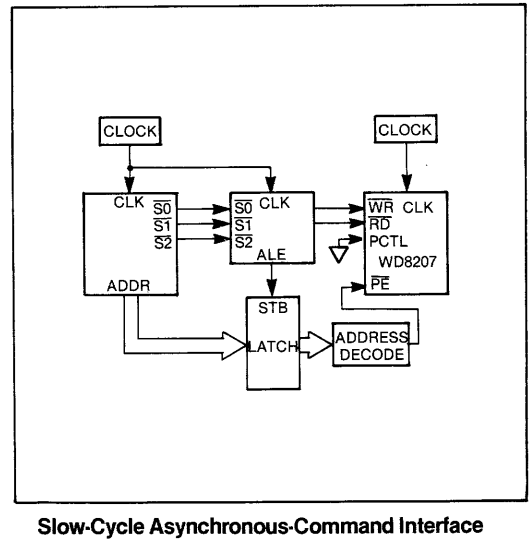
Slow-Cycle Synchronous-Status Interface



Slow-Cycle Asynchronous-Status Interface

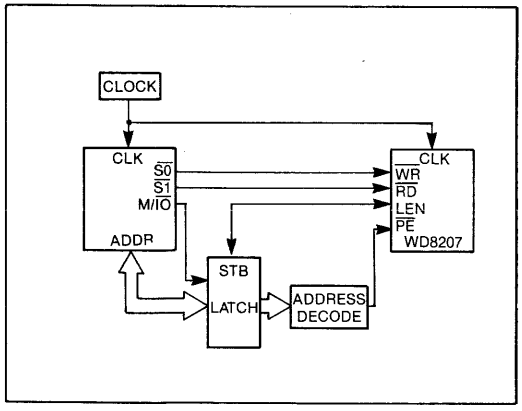


Slow-Cycle Synchronous-Command Interface

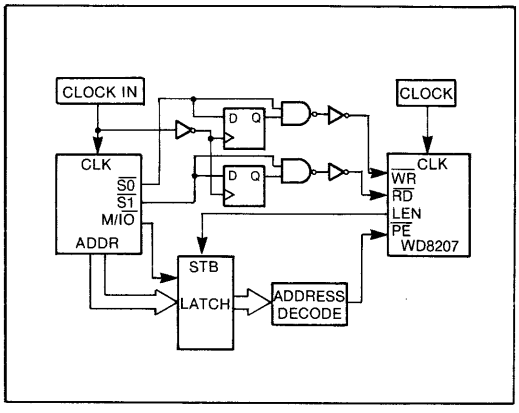


Slow-Cycle Asynchronous-Command Interface

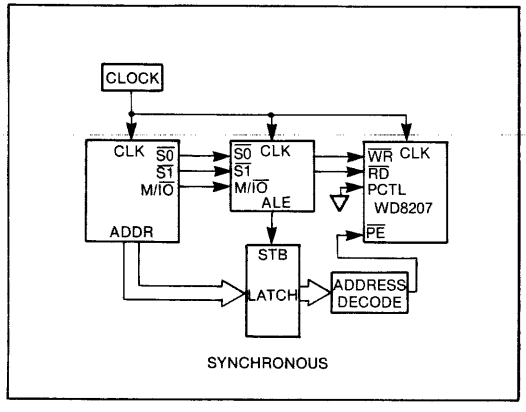
Figure 2A. SLOW-CYCLE PORT INTERFACES SUPPORTED BY THE WD8207



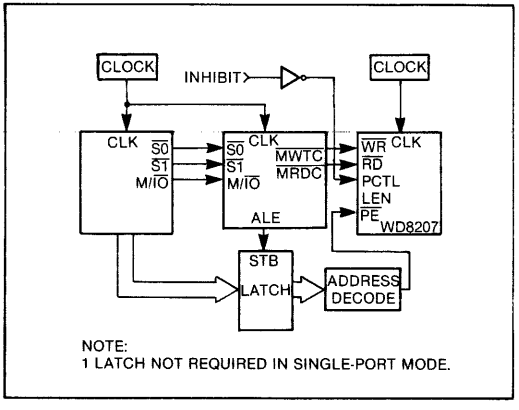
Fast-Cycle Synchronous-Status Interface



Fast-Cycle Asynchronous-Status Interface



Fast-Cycle Synchronous-Command Interface



Fast-Cycle Asynchronous-Command Interface

Figure 2B. FAST-CYCLE PORT INTERFACES SUPPORTED BY THE WD8207

Dual-Port Operation

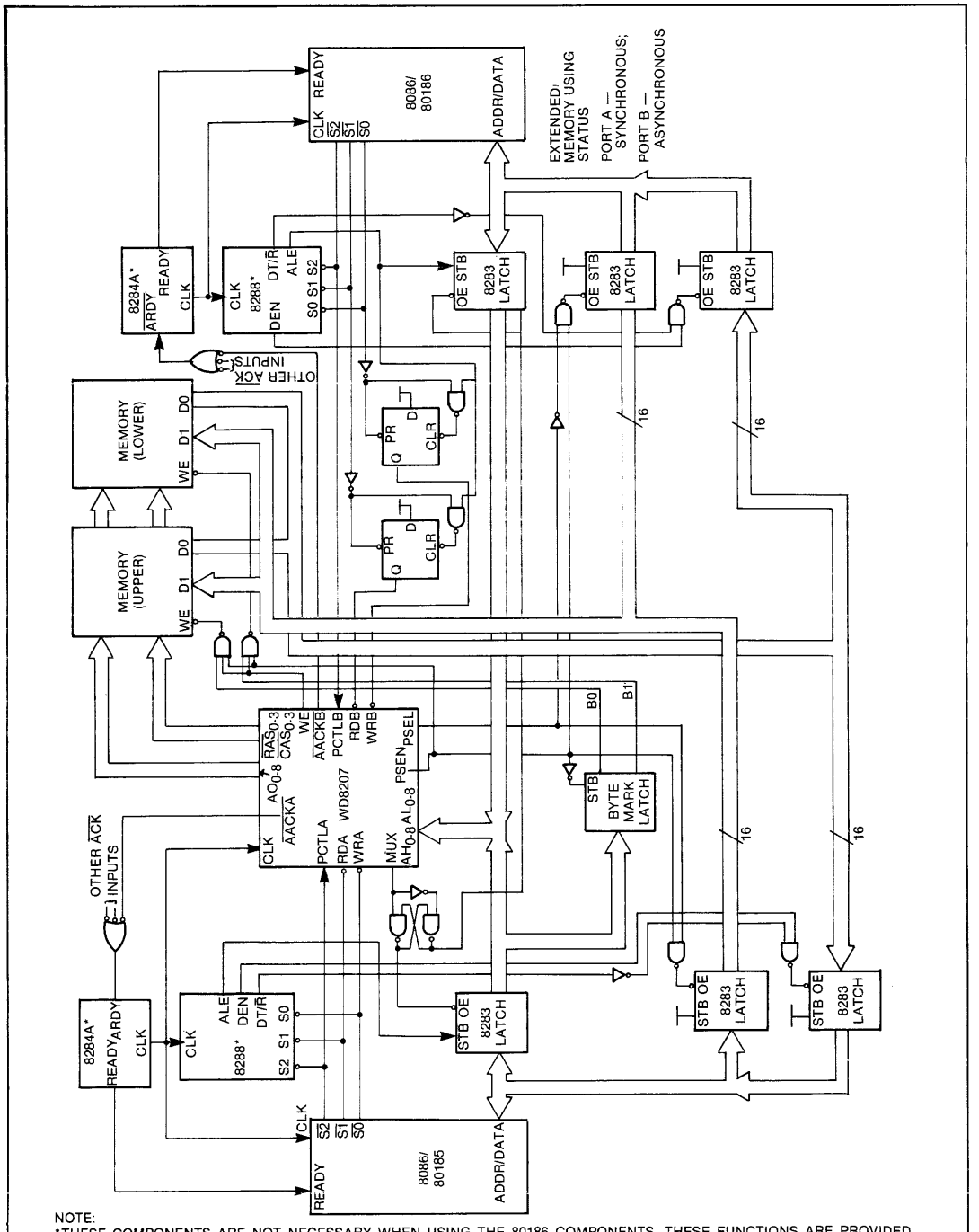
The WD8207 provides for two-port operation. Two independent processors may access memory controlled by the WD8207. The WD8207 arbitrates between each of the processor requests and directs data to or from the appropriate port. Selection is done on a priority concept that reassigns priorities based upon past history. Processor requests are internally queued.

Figure 3 shows a dual-port configuration with two systems interfacing to dynamic RAM. One of the processor systems is interfaced synchronously using the status interface and the other is interfaced asynchronously also using the status interface.

Dynamic RAM Interface

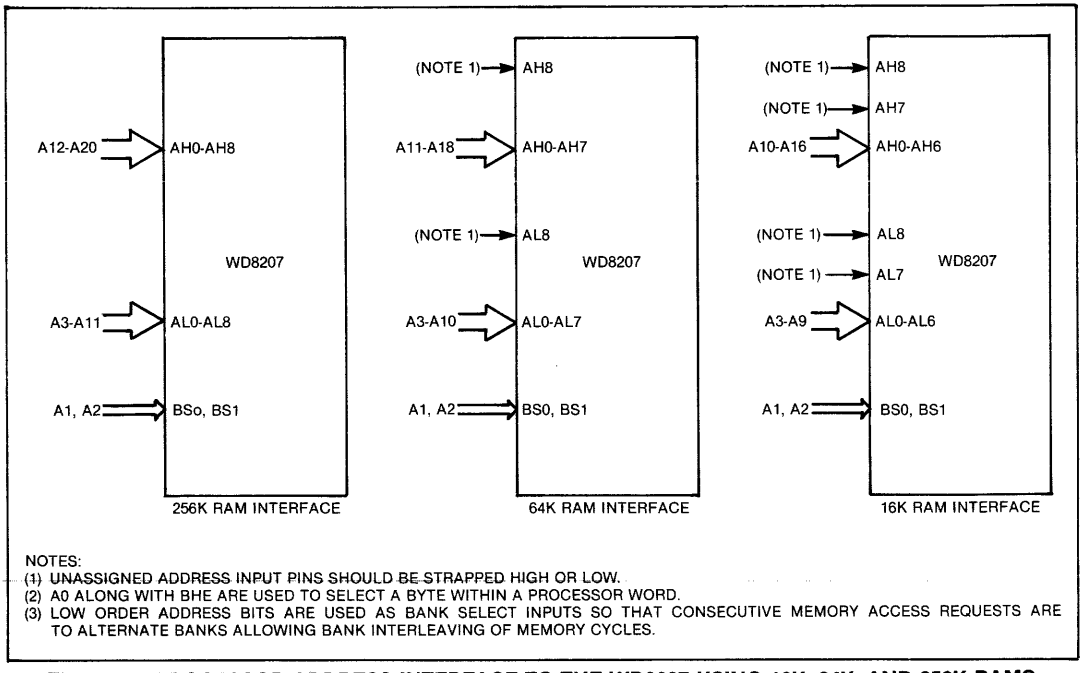
The WD8207 is capable of addressing 16K, 64K and 256K dynamic RAMs. Figure 4 shows the connection of the processor address bus to the WD8207 using the different RAMs. The WD8207 directly supports the 2118 RAM family or any RAM with similar timing requirements and responses including the 2164A RAM.

The WD8207 divides memory into four banks, each bank having its own Row ($\overline{RAS}$) and Column ($\overline{CAS}$) Address Strobe pair. This organization permits RAM cycle interleaving and permits error scrubbing during ECC refresh cycles. RAM cycle interleaving overlaps the start of the next RAM cycle with the RAM



NOTE:
*THESE COMPONENTS ARE NOT NECESSARY WHEN USING THE 80186 COMPONENTS. THESE FUNCTIONS ARE PROVIDED DIRECTLY BY THE 80186.

Figure 3. DUAL PORT SYSTEM



NOTES:
(1) UNASSIGNED ADDRESS INPUT PINS SHOULD BE STRAPPED HIGH OR LOW.
(2) A0 ALONG WITH BHE ARE USED TO SELECT A BYTE WITHIN A PROCESSOR WORD.
(3) LOW ORDER ADDRESS BITS ARE USED AS BANK SELECT INPUTS SO THAT CONSECUTIVE MEMORY ACCESS REQUESTS ARE TO ALTERNATE BANKS ALLOWING BANK INTERLEAVING OF MEMORY CYCLES.

Figure 4. PROCESSOR ADDRESS INTERFACE TO THE WD8207 USING 16K, 64K, AND 256K RAMS

Precharge period of the previous cycle. Hiding the precharge period of one RAM cycle behind the data access period of the next RAM cycle optimizes memory bandwidth and is effective as long as successive RAM cycles occur in alternate banks.

Successive data access to the same bank will cause the WD8207 to wait for the precharge time of the previous RAM cycle.

If not all RAM banks are occupied, the WD8207 reassigns the $\overline{RAS}$ and $\overline{CAS}$ strobes to allow using wider data words without increasing the loading on the $\overline{RAS}$ and $\overline{CAS}$ drivers. Table 2 shows the bank selection decoding and the word expansion, including $\overline{RAS}$ and $\overline{CAS}$ assignments. For example, if only two RAM banks are occupied, then two $\overline{RAS}$ and two $\overline{CAS}$ strobes are activated per bank.

The WD8207 can interface to fast or slow RAMs. The WD8207 adjusts and optimizes internal timings for either the fast or slow RAMs as programmed. (See RAM Speed Option)

Memory Initialization

After programming, the WD8207 performs eight RAM "warm-up" cycles to prepare the dynamic RAM for proper device operation and if configured for operation with error correction, the WD8207 and WD8206 EDCU will proceed to initialize all of memory (memory is written with zeros with corresponding check bits).

Table 2.
BANK SELECTION DECODING AND WORD EXPANSION

PROGRAM BITS		BANK INPUT		RAS/CAS
RB1	RB0	BS1	BS0	PAIR ALLOCATION
0	0	0	0	$RAS_{0\text{-}3}$, $CAS_{0\text{-}3}$ to Bank 0
0	0	0	1	Bank 1 unoccupied
0	0	1	0	Bank 2 unoccupied
0	0	1	1	Bank 3 unoccupied
0	1	0	0	$RAS_{0,1}$, $CAS_{0,1}$ to Bank 0
0	1	0	1	$RAS_{2,3}$, $CAS_{2,3}$ to Bank 1
0	1	1	0	Bank 2 unoccupied
0	1	1	1	Bank 3 unoccupied
1	0	0	0	RAS_0, CAS_0 to Bank 0
1	0	0	1	RAS_1, CAS_1 to Bank 1
1	0	1	0	RAS_2, CAS_2 to Bank 2
1	0	1	1	Bank 3 unoccupied
1	1	0	0	RAS_0, CAS_0 to Bank 0
1	1	0	1	RAS_1, CAS_1 to Bank 1
1	1	1	0	RAS_2, CAS_2 to Bank 2
1	1	1	1	RAS_3, CAS_3 to Bank 3

Because the time to initialize memory is fairly long, the WD8207 may be programmed to skip initialization in ECC mode. The time required to initialize all of memory is dependent on the clock cycle time to the WD8207 and can be calculated by the following equation:

Eq. 1 $T_{INIT} = (2^{23}) T_{CY}$

if T_{CY} = 125 ns then $T_{INIT} \approx 1$ sec.

WD8206 ECC Interface

For operation with Error Checking and Correction (ECC), the WD8207 adjusts its internal timing and changes some pin functions to optimize performance and provide a clean dual-port memory interface between the WD8206 EDCU and memory. The WD8207 directly supports a master-only (16-bit word plus 6 check bits) system. Under extended operation and reduced clock frequency, the WD8207 will support any ECC master-slave configuration up to 80 data bits, which is the maximum set by the WD8206 EDCU. (See Extend Option)

Correctable errors detected during memory read cycles are corrected immediately and then written back into memory.

In a synchronous bus environment, ECC system perfomance has been optimized to enhance processor throughput, while in an asynchronous bus environment (the Multibus), ECC performance has been optimized to get valid data onto the bus as quickly as possible. Performance optimization, processor throughput or quick data access may be selected via the Transfer Acknowledge Option.

The main difference between the two ECC implementations is that, when optimized for processor throughput, RAM data is always corrected and an advanced transfer acknowledge is issued at a point when, by knowing the processor characteristics, data is guaranteed to be valid by the time the processor needs it.

When optimized for quick data access, (valid for Multibus) the WD8206 is configured in the uncorrecting mode where the delay associated with error correction circuitry is transparent, and a transfer acknowledge is issued as soon as valid data is known to exist. If the $\overline{\text{ERROR}}$ flag is activated, then the transfer acknowledge is delayed until after the WD8207 has instructed the WD8206 to correct the data and the corrected data becomes available on the bus. Figure 5 illustrates a dual-port ECC system.

Figure 6 illustrates the interface required to drive the $\overline{\text{CRCT}}$ pin of the WD8206, in the case that one port (PORT A) receives an advanced acknowledge (not Multibus-compatible), while the other port (PORT B) receives $\overline{\text{XACK}}$ (which is Multibus-compatible).

Error Scrubbing

The WD8207/8206 performs error correction during refresh cycles (error scrubbing). Since the WD8207 must refresh RAM, performing error scrubbing during refresh allows it to be accomplished without additional performance penalties.

Upon detection of a correctable error during refresh, the RAM refresh cycle is lengthened slightly to permit the WD8206 to correct the error and for the corrected word to be rewritten into memory. Uncorrectable errors detected during scrubbing are ignored.

Refresh

The WD8207 provides an internal refresh interval counter and a refresh address counter to allow the WD8207 to refresh memory. The WD8207 will refresh 128 rows every 2 milliseconds or 256 rows every 4 milliseconds, which allows all RAM refresh options to be supported. In addition, there exists the ability to refresh 256 row address locations every 2 milliseconds via the Refresh Period programming option.

The WD8207 may be programmed for any of five different refresh options: Internal refresh only, External refresh with failsafe protection, External refresh without failsafe protection, Burst Refresh mode, or no refresh. (See Refresh Options)

It is possible to decrease the refresh time interval by 10%, 20% or 30%. This option allows the WD8207 to compensate for reduced clock frequencies. Note that an additional 5% interval shortening is built-in in all refresh interval options to compensate for clock variations and non-immediate response to the internally generated refresh request. (See Refresh Period Options)

External Refresh Requests after RESET

External refresh requests are not recognized by the WD8207 until after it is finished programming and preparing memory for access. Memory preparation includes 8 RAM cycles to prepare and ensure proper dynamic RAM operation, and memory initialization if error correction is used. Many dynamic RAMs require this warm-up period for proper operation. The time it takes for the WD8207 to recognize a request is shown below.

Eq. 2 Non-ECC Systems: $T_{RESP} = T_{PROG} + T_{PREP}$

Eq. 3 where: $T_{PROG} =$ (66) (T_{CY}) which is programming time

Eq. 4 $T_{PREP} =$ (8) (32) (T_{CY}) which is the RAM warm-up time

if T_{CY} = 125 ns then $T_{RESP} \approx 41$ us

Eq. 5 ECC Systems: $T_{RESP} = T_{PROG} + T_{PREP} + T_{INIT}$

if T_{CY} = 125 ns then $T_{RESP} \approx 1$ sec

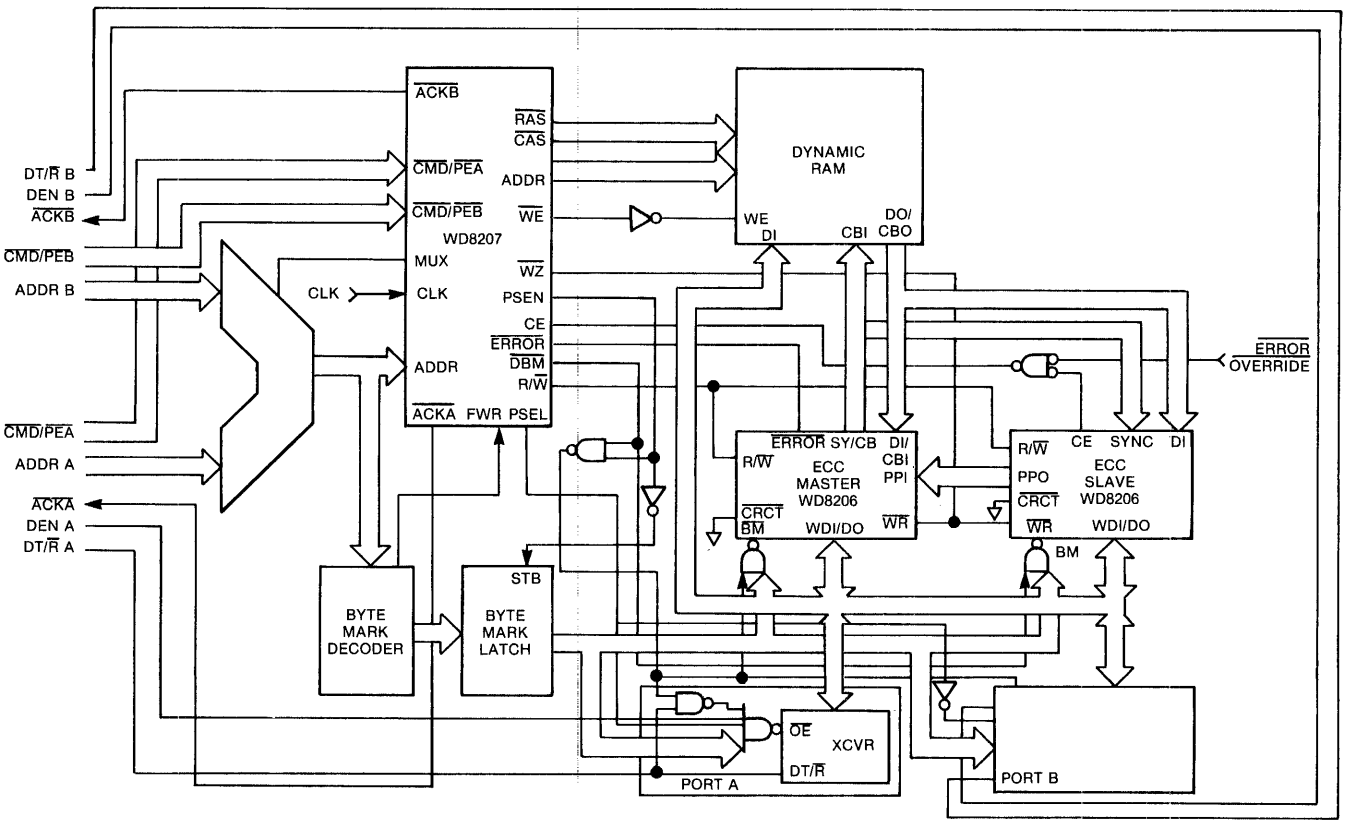


Figure 5. TWO-PORT ECC IMPLEMENTATION USING THE WD8207 AND THE WD8206

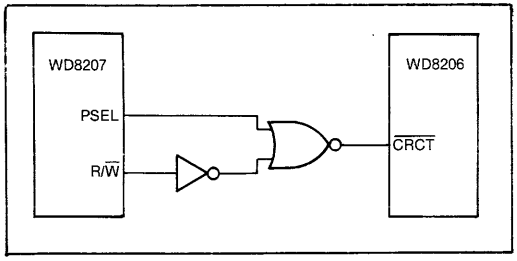


Figure 6.
INTERFACE TO WD8206 $\overline{\text{CRCT}}$ INPUT WHEN PORT A RECEIVES $\overline{\text{AACK}}$ AND PORT B RECEIVES $\overline{\text{XACK}}$

RESET

RESET is an asynchronous input, the falling edge of which is used by the 20 to directly sample the logic levels of the PCTLA, PCTLB, RFRQ, and PDI inputs. The internally synchronized falling edge of RESET is used to begin programming operations (shifting in the contents of the external shift register into the PDI input).

Until programming is complete the WD8207 registers but does not respond to command or status inputs. A simple means of preventing commands or status from occurring during this period is to differentiate the system reset pulse to obtain a smaller reset pulse for the WD8207. The total time of the reset pulse and the WD8207 programming time must be less than the time before the first command in systems that alter the default port synchronization programming bits (default is Port A synchronous, Port B asynchronous). Differentiated reset is unnecessary when the default port synchronization programming is used.

The differentiated reset pulse would be shorter than the system reset pulse by at least the programming period required by the WD8207. The differentiated reset pulse first resets the WD8207, and system reset would reset the rest of the system. While the rest of the system is still in reset, the WD8207 completes its programming. Figure 7 illustrates a circuit to accomplish this task.

Within four clocks after RESET goes active, all the WD8207 outputs will go high, except for PSEN, WE, and AO0-8, which will go low.

OPERATIONAL DESCRITION

Programming the WD8207

The WD8207 is programmed after reset. On the falling edge of RESET, the logic states of several input pins are latched internally. The falling edge of RESET actually performs the latching, which means that the logic levels on these inputs must be stable prior to that time. The inputs whose logic levels are latched at the end of reset are the PCTLA, PCTLB, REFRQ, and PDI pins. Figure 8 shows the necessary timing for programming the WD8207.

Refresh Options

Immediately after system reset, the state of the REFRQ input pin is examined. If REFRQ is high, the WD8207 provides the user with the choice between self-refresh or user-generated refresh with failsafe protection. Failsafe protection guarantees that if the user does not come back with another refresh request before the internal refresh interval counter times out, a refresh request will be automatically generated. If the REFRQ pin is low immediately after a reset, then the user has the choice of a single external refresh cycle without failsafe, burst refresh or no refresh.

Internal Refresh Only

For the WD8207 to generate internal refresh requests, it is necessary only to strap the REFRQ input pin high.

External Refresh with Failsafe

To allow user-generated refresh requests with failsafe protection, it is necessary to hold the REFRQ input high until after reset. Thereafter, a low-to-high transition on this input causes a refresh request to be generated and the internal refresh interval counter to be reset. A high-to-low transition has no effect on the WD8207. A refresh request is not reconized until a previous request has been serviced.

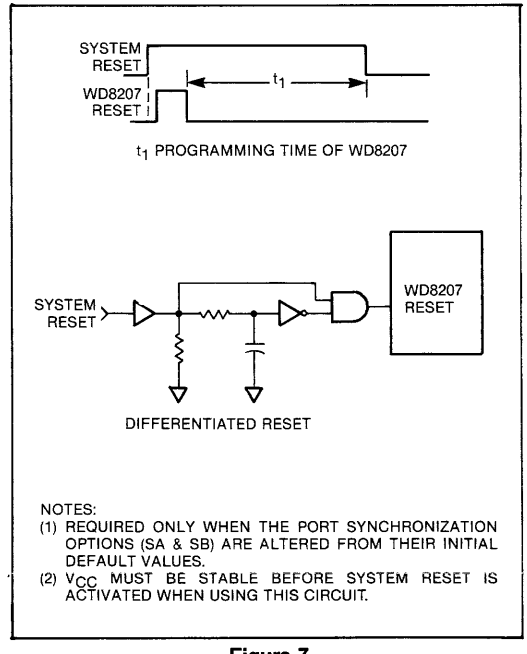


Figure 7.
WD8207 DIFFERENTIATED RESET CIRCUIT

External Refresh without Failsafe

To generate single external refresh requests without failsafe protection, it is necessary to hold REFRQ low until after reset. Thereafter, bringing REFRQ high for one clock period causes a refresh request to be generated. A refresh request is not recognized until a previous request has been serviced.

Burst Refresh

Burst refresh is implemented through the same procedure as a single external refresh without failsafe (i.e., REFRQ is kept low until after reset). Thereafter, bringing REFRQ high for at least two clock periods causes a burst of 128 row address locations to be refreshed.

In ECC-configured systems, 128 locations are scrubbed. A burst refresh request is not recognized until a previous request has been serviced.

No Refresh

It is necessary to hold REFRQ low until after reset. This is the same as programming External Refresh without Failsafe. No refresh is accomplished by keeping REFRQ low.

Option Program Data Word

The program data word consists of 16 program data bits, PD0-PD15. If the first program data bit PD0 is set to logic 1, the WD8207 is configured to support ECC. If it is logic 0, the WD8207 is configured to support a non-ECC system. The remaining bits, PD1-PD15, may then be programmed to optimize a selected configuration. Figures 8 and 9 show the Program word for non-ECC and ECC operation.

Using an External Shift Register

The WD8207 may be configured to use an external shift register with asynchronous load capability such as a 74LS165. The reset pulse serves to parallel load the shift register and the WD8207 supplies the clocking signal to shift the data in. Figure 10 shows a sample circuit diagram of an external shift register circuit. Serial data is shifted into the WD8207 via the PDI pin (57), and clock is provided by the MUX/PCLK pin (12), which generates a total of 16 clock pulses. After programming is complete, data appearing at the input of the PDI pin is ignored. MUX/PCLK is a dual-function pin. during programming, it serves to clock the external shift register, and after programming is completed, it reverts to a MUX control pin. As the pin changes state to select different port addresses, it continues to clock the shift register. This does not present a problem because data at the PDI pin is ignored after programming.

ECC Mode (ECC Program Bit)

The state of PDI (Program Data In) pin at reset determines whether the system is an ECC or non-ECC configuration. It is used internally by the WD8207 to begin configuring timing circuits, even before programming is completely finished. The WD8207 then begins programming the rest of the options.

Default Programming Options

After reset, the WD8207 serially shifts in a program data word via the PDI pin. This pin may be strapped either high or low, or connected to an external shift register. Strapping PDI high causes the WD8207 to default to a particular system configuration with error correction, and strapping it low causes the WD8207 to default to a particular system configuration without error correction. Table 4 shows the default configurations.

If further system flexibility is needed, one or two external shift registers can be used to tailor the WD8207 to its operating environment.

Synchronous/Asynchronous Mode (SA and SB Program Bits)

Each port of the WD8207 may be independently configured to accept synchronous or asynchronous port commands (RD, WR, PCTL) and Port Enable (PE) via the program bits SA and SB. The state of the SA and SB programming bits determine whether their associated ports are synchronous or asynchronous.

While a port may be configured with either the Status or Command interface in the synchronous mode, certain restrictions exist in the asynchronous mode. An asynchronous Command interface using the control lines of the Multibus is supported, and an asynchronous WD8086 interface using the control lines of the WD8086 is supported, with the use of TTL gates as illustrated in Figure 2. In the WD8086 case, the TTL gates are needed to guarantee that status does not appear at the WD8207 inputs too much before address, so that a cycle would start before address was valid.

Microprocessor Clock Frequency Option (CFS and FFS Program Bits)

The WD8207 can be programmed to interface with slow-cycle microprocessors or fast-cycle microprocessors. The CFS bit configures the microprocessor interface to accept slow or fast cycle signals from either microprocessor group.

This option is used to select the speed of the microprocessor clock. Table 5 shows the various microprocessor clock frequency options that can be programmed.

The external clock frequency must be programmed so that the failsafe refresh repetition circuitry can adjust its internal timing accordingly to produce a refresh request as programmed.

RAM Speed Option (RFS Program Bit)

The RAM Speed programming option determines whether RAM timing will be optimized for a fast or

PD15							PD8 PD7							PD0
0	0	TM 1	$\overline{PPR}$	$\overline{FFS}$	EXT	$\overline{PLS}$	CI0	CI2	$\overline{RB1}$	$\overline{RB0}$	$\overline{RFS}$	$\overline{CFS}$	SB	$\overline{SA}$	0

PROGRAM DATA BIT	NAME	POLARITY/FUNCTION	
PD0	ECC	ECC = 0	For non-ECC mode
PD1	$\overline{SA}$	$\overline{SA}$ = 0 $\overline{SA}$ = 1	Port A is synchronous Port A is asynchronous
PD2	SB	SB = 0 SB = 1	Port B is asynchronous Port B is synchronous
PD3	$\overline{CFS}$	$\overline{CFS}$ = 0 $\overline{CFS}$ = 1	Fast-cycle IAPX 286 mode Slow-cycle IAPX 86 mode
PD4	$\overline{RFS}$	$\overline{RFS}$ = 0 $\overline{RFS}$ = 1	Fast RAM Slow RAM
PD5 PD6	$\overline{RB0}$ $\overline{RB1}$	RAM bank occupancy See Table 2	
PD7	CI1	Count interval bit 1; see Table 6	
PD8	CI0	Count interval bit 0; see Table 6	
PD9	$\overline{PLS}$	$\overline{PLS}$ = 0 $\overline{PLS}$ = 1	Long refresh period Short refresh period
PD10	EMT EXT	EXT = 0 gext71	Not extended Extended
PD11	$\overline{FFS}$	$\overline{FFS}$ = 0 $\overline{FFS}$ = 1	Fast CPU frequency Slow CPU frequency
PD12	$\overline{PPR}$	$\overline{PPR}$ = 0 $\overline{PPR}$ = 1	Most recently used port priority Port A preferred priority
PD13	TM1	TM1 = 0 TM1 = 1	Test mode 1 off Test mode 1 enabled
PD14	0	Reserved must be zero	
PD15	0	Reserved must be zero	

Figure 8. NON-ECC MODE PROGRAM DATA WORD

slow RAM. Whether a RAM is fast or slow is measured relative to the 2118-10 (Fast) or the 2118-15 (Slow) RAM specifications.

Refresh Period Options (CI0, CI1, and PLS Program Bits)

The WD8207 refreshes with either 128 rows every 2 milliseconds or 256 rows every 4 milliseconds. This translates to one refresh cycle being executed approximately once every 15.6 microseconds. This rate can be changed to 256 rows every 2 milliseconds or a refresh approximately once every 7.8 microseconds via the Period Long/Short, program bit PLS, programming option. The 7.8 microsecond refresh request rate is intended for those RAMs, 64K and above, which may require a faster refresh rate.

In addition to PLS program option, two other programming bits for refresh exist: Count Interval 0 (CI0) and Count Interval 1 (CI1). These two programming bits allow the rate at which refresh requests are generated to be increased in order to permit refresh requests to be generated close to the same 15.6 or 7.8 microsecond period when the WD8207 is operating at reduced frequencies. The interval between refreshes is decreased by 0%, 10%, 20%, or 30% as a function of how the count interval bits are programmed. A 5% guardband is built-in to allow for any clock frequency variations. Table 6 shows the refresh period options available.

The numbers tabulated under Count Interval represent the number of clock periods between internal refresh requests. The percentages in parentheses represent the decrease in interval between refresh requests. Note that all intervals have a built-in 5% (approximately) safety factor to compensate for minor clock frequency deviations and non-immediate response to internal refresh requests.

PD15							PD8 PD7								PD0
$\overline{TM2}$	RB1	RB0	PPR	FFS	$\overline{EXT}$	PLS	$\overline{CI0}$	$\overline{CI1}$	XB	$\overline{XA}$	RFS	CFS	$\overline{SB}$	SA	1

PROGRAM DATA BIT	NAME	POLARITY/FUNCTION
PD0	ECC	ECC = 1 ECC mode
PD1	SA	SA = 0 Port A is asynchronous SA = 1 Port A is synchronous
PD2	$\overline{SB}$	$\overline{SB}$ = 0 Port B is synchronous $\overline{SB}$ = 1 Port B is asynchronous
PD3	CFS	CFS = 0 Slow-cycle IAPX 86 mode CFS = 1 Fast-cycle IAPX 286 mode
PD4	RFS	RFS = 0 Slow RAM RFS = 1 Fast RAM
PD5	$\overline{XA}$	$\overline{XA}$ = 0 Multibus-compatible ACKA $\overline{XA}$ = 1 Advanced ACKA not multibus-compatible
PD6	XB	XB = 0 Advanced ACKB not multibus compatible XB = 1 Multibus-compatible ACKB
PD7	$\overline{CI1}$	Count interval bit 1; see Table 6
PD8	$\overline{CI0}$	Count interval bit 0; see Table 6
PD9	PLS	PLS = 0 Short refresh period PLS = 1 Long refresh period
PD10	$\overline{EXT}$	$\overline{EXT}$ = 0 Master and slave EDCU $\overline{EXT}$ = 1 Master EDCU only
PD11	FFS	FFS = 0 Slow CPU frequency FFS = 1 Fast CPU frequency
PD12	PPR	PPR = 0 Port A preferred priority PPR = 1 Most recently used port priority
PD13	RB0	RAM bank occupancy
PD14	RB1	See Table 2
PD15	$\overline{TM2}$	$\overline{TM2}$ = 0 Test mode 2 enabled $\overline{TM2}$ = 1 Test mode 2 off

Figure 9. ECC MODE PROGRAM DATA WORD

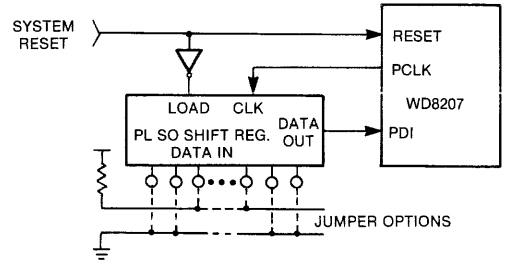


Figure 10.
EXTERNAL SHIFT REGISTER INTERFACE

Table 4A.
DEFAULT NON-ECC PROGRAMMING, PDI PIN (57) TIED TO GROUND

Port A is Synchronous
Port B is Asynchronous
Fast-cycle Processor Interface
Fast RAM
Refresh Interval uses 236 clocks
128 Row refresh in 2 ms; 256 Row refresh in 4 ms
Fast Processor Clock Frequency (16 MHz)
"Most Recently Used" Priority Scheme
4 RAM banks occupied

Table 4B.
DEFAULT NON-ECC PROGRAMMING, PDI PIN (57) TIED TO V_{CC}

Port A is Synchronous
Port B is Asynchronous
Fast-cycle Processor Interface
Fast RAM
Port A has Advanced ACKA strobe (non-multibus)
Port B has Non-advance ACKB strobe (multibus)
Refresh Interval uses 236 clocks
128 Row refresh in 2 ms; 256 Row refresh in 4 ms
Master EDCU only (16-bit system)
Fast Processor Clock Frequency (16 MHz)
"Most Recently Used" Priority Scheme
4 RAM banks occupied

Table 5.
MICROPROCESSOR CLOCK FREQUENCY OPTIONS

PROGRAM BITS		PROCESSOR	CLOCK FREQUENCY
CFS	FFS		
0	0	Slow Cycle	5 MHz
0	1	Slow Cycle	8 MHz
1	0	Fast Cycle	10 MHz
1	1	Fast Cycle	16 MHz

Extend Option (EXT Program Bit)

The Extend option lengthens the memory cycle to allow longer access time which may be required by the system. Extend alters the RAM timing to compensate for increased loading on the Row and Column Address Strobes, and in the multiplexed Address Out lines.

Port Priority Option and Arbitration (PPR Program Bit)

The WD8207 has to internally arbitrate among three ports: Port A, Port B and Port C — the refresh port. Port C is an internal port dedicated to servicing refresh requests, whether they are generated internally by the refresh interval counter, or externally by the user. Two arbitration approaches are available via the Port Priority programming option, program bit PPR. PPR determines whether the most recently used port will remain selected (PPR = 1) or whether Port A will be favored or preferred over Port B (PPR = 0).

A port is selected if the arbiter has given the selected port direct access to the timing generators. The front-end logic, which includes the arbiter, is designed to operate in parallel with the selected port. Thus a request on the selected port is serviced immediately. In contrast, an unselected port only has access to the timing generators through the front- end logic. Before a RAM cycle can start for an unselected port, that port must first become selected (i.e., the MUX output now gates that port's address into the WD8207 in the case of Port A or B). Also, in order to allow its address to stabilize, a newly selected port's first RAM cycle is started by the front- end logic. Therefore, the selected port has direct access to the timing generators. What all this means is that a request on a selected port is started immediately, while a request on an unselected port is started two to three clock periods after the request, assuming that the other two ports are idle. Under normal operating conditions, this arbitration time is hidden behind the RAM cycle of the selected port so that as soon as the present cycle is over a new cycle is started. Table 7 lists the arbitration rules for both options.

Port LOCK Function

The LOCK function provides each port with the ability to obtain uninterrupted access to a critical region of memory and, thereby, to guarantee that the opposite port cannot "sneak in" and read from or write to the critical region prematurely.

Only one LOCK pin is present and is multiplexed between the two ports as follows: when MUX is high, the WD8207 treats the LOCK input as originating at PORT A, while when MUX is low, the WD8207 treats LOCK as originating at PORT B. When the WD8207 recognizes a LOCK, the MUX output will remain pointed to the locking port until LOCK is deactivated. Refresh is not affected by LOCK and can occur during a locked memory cycle.

Table 6. REFRESH COUNT INTERVAL TABLE

FREQ. (MHz)	REF. PERIOD (μS)	CFS	PLS	FFS	COUNT INTERVAL CI1, CI0 (WD8207 CLOCK PERIODS)			
					00 (0%)	01 (10%)	10 (20%)	11 (30%)
16	15.6	1	1	1	236	212	188	164
	7.8	1	0	1	118	106	94	82
10	15.6	1	1	0	148	132	116	100
	7.8	1	0	0	74	66	58	50
8	15.6	0	1	1	118	106	94	82
	7.8	0	0	1	59	53	47	41
5	15.6	0	1	0	74	66	58	50
	7.8	0	0	0	37	33	29	25

Table 7.
THE ARBITRATION RULES FOR THE MOST RECENTLY USED PORT PRIORITY AND FOR PORT A PRIORITY OPTIONS

1. If only one port requests service, then that port — if not already selected — becomes selected.
2a. When no service requests are pending, the last selected processor port (Port A or B) will remain selected. (Most Recently Used Port Priority Option)
2b. When no service requests are pending, Port A is selected whether it requests service or not. (Port A Priority Option)
3. During reset initialization only Port C, the refresh port, is selected.
4. If no processor requests are pending after reset initialization, Port A will be selected.
5a. If Ports A and B simultaneously(*) request service while Port C is being serviced, then the next port to be selected is the one which was not selected prior to servicing Port C. (Most Recently Used Port Priority Option)
5b. If Ports A and B simultaneously(*) request service while Port C is selected, then the next port to be selected is Port A. (Port A Priority Option)
6. If a port simultaneously requests service with the currently selected port, service is granted to the selected port.
7. The MUX output remains in its last state whenever Port C is selected.
8. If Port C and either Port A or Port B (or both) simultaneously request service, then service is granted to the requester whose port is already selected. If the selected port is not requesting service, then service is granted to Port C.
9. If during the servicing of one port, the other port requests service before or simultaneously with the refresh port, the refresh port is selected. A new port is not selected before the presently selected port is deactivated.
10. Activating LOCK will mask off service requests from Port B if the MUX output is high, or from Port A if the MUX output is low.
*By "simultaneous" it is meant that two or more requests are valid at the clock edge at which the internal arbiter samples them.

Dual-Port Considerations

For both ports to be operated synchronously, several conditions must be met. The processors must be the same type (Fast or Slow Cycle) as defined by Table 8 and they must have synchronized clocks. Also when processor types are mixed, even though the clocks may be in phase, one frequency may be twice that of the other. So to run both ports synchronous using the status interface, the processors must have related timings (both phase and frequency). If these conditions cannot be met, then one port must run synchronous and the other asynchronous.

Figure 3 illustrates an example of dual-port operation using the processors in the slow cycle group. Note the use of cross-coupled NAND gates at the MUX output for minimizing contention between the two latches, and the use of flip flops on the status lines of the synchronous processor for delaying the status and thereby guaranteeing RAS will not be issued, even in the worst case, until address is valid. Figure 11 shows the timing associated with Port switching.

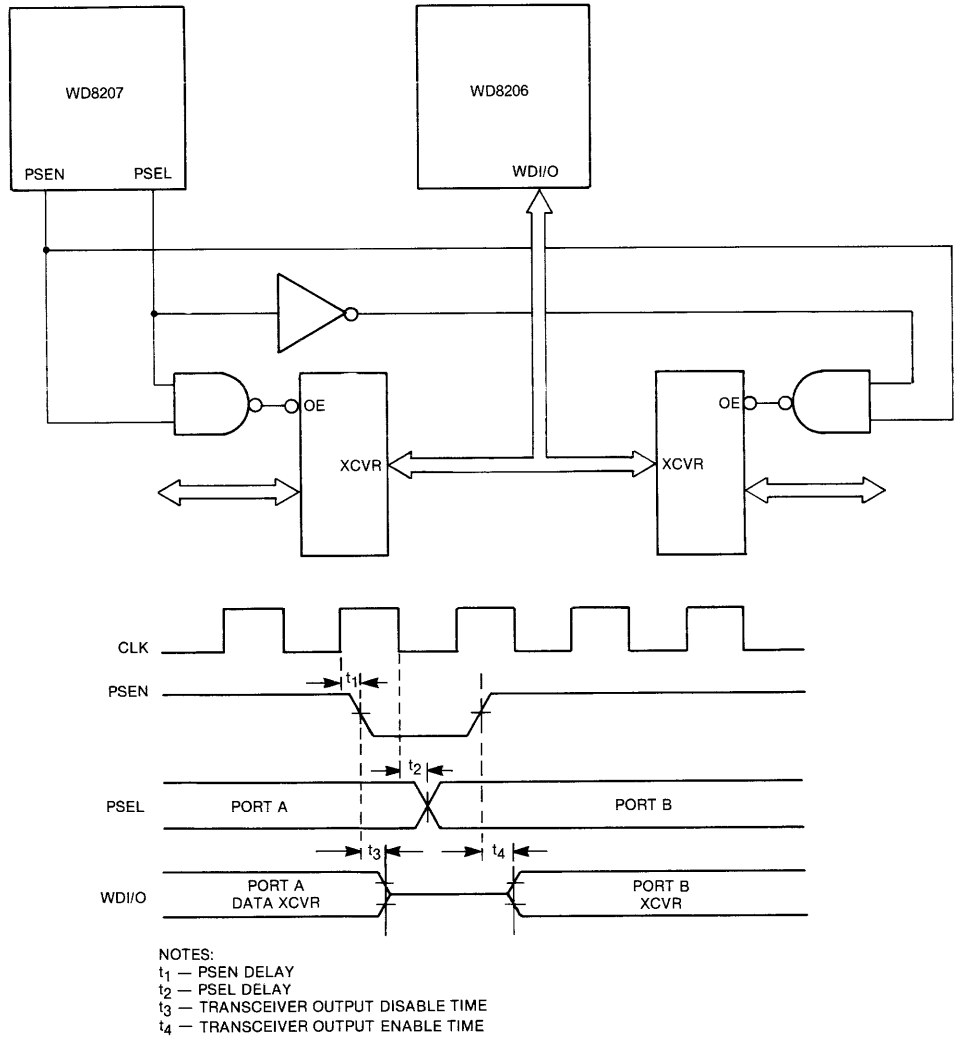


Figure 11.

Table 8. PROCESSOR INTERFACE/ACKNOWLEDGE SUMMARY

CYCLE	REQUEST TYPE	SYNC/ASYNC INTERFACE	ACKNOWLEDGE TYPE
Fast Cycle CFS = 1	Status	SYNC	$\overline{EAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	SYNC	$\overline{EAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{XACK}$
Slow Cycle CFS = 0	Status	SYNC	$\overline{EAACK}$
	Status	ASYNC	$\overline{LAACK}$
	Command	SYNC	$\overline{EAACK}$
	Command	ASYNC	$\overline{LAACK}$
	Command	ASYNC	$\overline{XACK}$

Table 9. MEMORY ACKNOWLEDGE OPTION SUMMARY

	SYNCHRONOUS	ASYNCHRONOUS	XACK
Fast Cycle	AACK Optimized	AACK Optimized	Multibus Compatible
Slow Cycle	AACK Optimized	AACK Optimized	Multibus Compatible

Test Modes

Two special test modes exist in the WD8207 to facilitate testing. Test Mode 1 (non-ECC mode) splits the refresh address counter into two separate counters and Test Mode 2 (ECC mode) presets the refresh address counter to a value slightly less than rollover.

Test Mode 1 splits the address counter into two, and increments both counters simultaneously with each refresh address update. By generating external refresh requests, the tester is able to check for proper operation of both counters. Once proper individual counter operation has been established, the WD8207 must be returned to normal mode and a second test performed to check that the carry from the first counter increments the second counter. The outputs of the counters are presented-on the address out bus with the same timing as the row and column addresses of a normal scrubbing operation. During Test Mode 1, memory initialization is inhibited, since the WD8207, by definition, is in non-ECC mode.

Test Mode 2 sets the internal refresh counter to a value slightly less than rollover. During functional testing other than that covered in Test Mode 1, the WD8207 will normally be set in Test Mode 2. Test Mode 2 eliminates memory initialization in ECC mode. This allows quick examination of the circuitry which brings the WD8207 out of memory initialization and into normal operation. Test Mode 2 is also useful for quick reset response in ECC systems.

General System Considerations

The RAS_{0-3}, CAS_{0-3}, AO_{0-8}, output buffers were designed to directly drive the heavy capacitive loads associated with dynamic RAM arrays. To keep the RAM driver outputs from ringing excessively in the system environment it is necessary to match the output impedance with the RAM array by using series resistors. Each application may have different impedance characteristics and may require different series resistance values. The series resistance values should be determined for each application.

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature
Under Bias ..... −10°C to +85°C
Storage Temperature ..... −65°C to +150°C
Voltage On Any Pin With
Respect to Ground ..... −3.5V to +7V
Power Dissipation ..... 2.5 Watts

NOTICE:
Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics (T_A = 0°C to +70°C, V_{CC} = 5.0V ± 10%, V_{SS} = GND)

SYMBOL	PARAMETER	MIN.	MAX.	UNITS	COMMENTS
V_{IL}	Input Low Voltage	−0.5	+0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage		0.45	V	Note 1
V_{OH}	Output High Voltage	2.4		V	Note 1
V_{ROL}	RAM Output Low Voltage		0.45	V	Note 1
V_{ROH}	RAM Output High Voltage	2.6		V	Note 1
I_{CC}	Supply Current		400	mA	T_A = 0°C
I_{LI}	Input Leakage Current		+10	μA	$0V \leqslant V_{IN} \leqslant V_{CC}$
V_{CL}	Clock Input Low Voltage	−0.5	+0.6	V	
V_{CH}	Clock Input High Voltage	3.9	V_{CC} + 1.0	V	
C_{IN}	Input Capacitance		20	pF	fc = 1 MHz

NOTES:
1. I_{OL} = 16 mA and I_{OH} = −0.4 mA for WE.
   I_{OL} = 8 mA and I_{OH} = −0.2 mA for all other outputs.

AC CHARACTERISTICS

Clock and Programming

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2 MIN.	WD8207 & WD8207-2 MAX.	WD8207-5 MIN.	WD8207-5 MAX.	UTS.	NOTES
1	TCLCL	Clock Period WD8207 WD8207 WD8207-2	62.5 125 125	500 500 500	 200	 500	ns ns ns	1 2 3
2	TCL	Clock Low Time	TCLCL/2-12		TCLCL/2-12		ns	
3	TCH	Clock High Time	TCLCL/3-3		TCLCL/3-3		ns	
4	TRTVCL	Reset to CLK↓ Setup	40		65		ns	4
5	TRTH	Reset Pulse Width	4TCLCL		4TCLCL		ns	
6	TPGVCL	PCTL, PDI, RFRQ to CLK↓ Setup	125		200		ns	5
7	TCLPGX	PCTL, PDI, RFRQ to CLK↓ Hold	0		0		ns	
8	TCLPC	PCLK from CLK↓ Delay		45		65	ns	
9	TPDVCL	PDIN to CLK↓ Setup	60		100		ns	
10	TCLPDX	PDIN to CLK↓ Hold	40		65		ns	6
RAM Warm-Up and Initialization								
64	TCLWZL	$\overline{WZ}$ from CLK↓ Delay		40		65	ns	7
μP Port Interface								
11	TPEVCL	$\overline{PE}$ to CLK↓ Setup	30		50			2
12	TKVCL	$\overline{RD}$, $\overline{WR}$, $\overline{PE}$, PCTL to CLK↓ Setup	20		30		ns	1,8
13	TCLKX	$\overline{RD}$, $\overline{WR}$, $\overline{PE}$, PCTL to CLK↓ Hold	0		0		ns	
14	TKVCH	$\overline{RD}$, $\overline{WR}$, PCTL to CLK↑ Setup	20		30		ns	2,8
15	TRWVCL	$\overline{RD}$, $\overline{WR}$ to CLK↓ Setup	20		30		ns	9
16	T R W L	$\overline{RD}$, $\overline{WR}$ Pulse Width	2TCLCL+20		2TCLCL+30		ns	
17	TRWLPEV	$\overline{PE}$ from $\overline{RD}$, $\overline{WR}$↓ Delay WD8207 WD8207 WD8207-2		TCLCL – 20 TCLCL – 30 TCLCL – 30		 TCLCL – 50	ns ns ns	1 2 3
18	TRWLPEX	$\overline{PE}$ to $\overline{RD}$, $\overline{WR}$↓ Hold	2TCLCL+20		2TCLCL+30		ns	6
19	TRWLPT	PCTL from $\overline{RD}$, $\overline{WR}$↓ Delay		TCLCL – 20		TCLCL – 30	ns	2
20	TRWLPTX	PCTL to $\overline{RD}$, $\overline{WR}$↓ Hold	2TCLCL+20		2TCLCL+30		ns	2
21	TRWLPT	PCTL from $\overline{RD}$, $\overline{WR}$↓ Delay		2tp – 20			ns	1
22	TRWLPTX	PCTL to $\overline{RD}$, $\overline{WR}$↓ Hold	2tp + 20				ns	1

AC CHARACTERISTICS (Continued)

RAM Interface

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2 MIN.	WD8207 & WD8207-2 MAX.	WD8207-5 MIN.	WD8207-5 MAX.	UTS.	NOTES
23	TAVCL	AL, AH, BS to CLK↓ Setup	35 + tASR		55 + tASR		ns	10
24	TCLAX	AL, AH, BS to CLK↓Hold	0		0		ns	
25	TCLLN	LEN from CLK↓ Delay		35		55	ns	
26	TCLRSL	$\overline{RAS}$↑ from CLK↓ Delay		35		55	ns	
28	TCLRSH	$\overline{RAS}$↑ from CLK↓ Delay		50		70	ns	
27	tRCD	$\overline{RAS}$ to $\overline{CAS}$ Delay	TCLCL/2 – 25 75 TCLCL – 25		 60 TCLCL – 40		ns ns ns	11 12 1
29	tRAH	Row AO to $\overline{RAS}$↓ Hold	TCLCL/4 – 10 40 TCLCL/2 – 10 90		 35		ns ns ns ns	11,13 12,13 13,14 13,15
30	tASR	Row AO to $\overline{RAS}$↓ Setup						10
31	tASC	Column AO to $\overline{CAS}$↓ Setup	TCLCL/4 – 25 25 TCLCL/2 – 25		 10		ns ns ns	11,16 12,16 1,16
32	tCAH	Column AO to $\overline{CAS}$Hold	(See RAM Timing Tables)					
33	TCLCSL	$\overline{CAS}$↓ from CLK↓ Delay		TCLCL/2 + 45		TCLCL/2 + 70	ns ns	11 12
34	TCLCSL	$\overline{CAS}$↓ from CLK↓ Delay		35			ns	1
35	TCLCSH	$\overline{CAS}$↑ from CLK↓ Delay		50		70	ns	
36	TCLW	WE from CLK↓ Delay		35		55	ns	
37	TCLTKL	$\overline{XACK}$↓ from CLK↓ Delay		35		55	ns	
38	TCLTKH	$\overline{XACK}$↑ from CLK↓ Delay		50		60	ns	
39	TCLAKL	$\overline{AACK}$↓ from CLK↓ Delay		35		55	ns	
40	TCLAKH	$\overline{AACK}$↑ from CLK↓ Delay		50		70	ns	
41	TCLDL	$\overline{DBM}$ from CLK↓ Delay		35		55	ns	

ECC Interface

42	TWRLFV	$\overline{FWR}$ from $\overline{WR}$↓ Delay WD8207 WD8207-2		2TCLCL – 40 TCLCL + TCL – 40		 TCLCL + TCL – 65	ns ns	1,17 2,17
43	TFVCL	$\overline{FWR}$ to CLK↓ Setup	40		65		ns	18
44	TCLFX	$\overline{FWR}$ to CLK↓ Hold	0		0		ns	19
45	TEVCL	$\overline{ERROR}$ to CLK↓ Setup	20		30		ns	20
46	TCLEX	$\overline{ERROR}$ to CLK↓ Hold	0		0		ns	
47	TCLRL	R/$\overline{W}$↓ from CLK↓ Delay		35		55	ns	
48	TCLRH	R/$\overline{W}$↑ from CLK↓ Delay		50		70	ns	
49	TCEVCL	CE to CLK↓ Setup	20		30		ns	20
50	TCLCEX	CE to CLK↓ Hold	0		0		ns	
51	TCLESV	ESTB from CLK↓ Delay		35		55	ns	

AC CHARACTERISTICS (Continued)

Port Switching and Lock

REF.	SYMBOL	PARAMETER	WD8207 & WD8207-2		WD8207-5		UTS.	NOTES
			MIN.	MAX.	MIN.	MAX.		
52	TCLMV	MUX from CLK↓ Delay		45		65	ns	
53	TCHPNV	PSEN from CLK↓ Delay		35		55	ns	
54	TCLPSV	PSEL from CLK↓ Delay		35		55	ns	
55	TLKVCL	LOCK to CLK↓ Setup	30		50		ns	21,22
56	TCLLKX	LOCK to CLK↓ Hold	0		0		ns	21,22
57	TRWLLKV	LOCK from $\overline{RD}$↓, $\overline{WR}$↓ Delay		2TCLCL − 30		2TCLCL − 50	ns	22,23
58	TRWHLKX	LOCK to $\overline{RD}$↑, $\overline{WR}$↑ Hold	3TCLCL+ 20		3TCLCL+ 20		ns	22,23

Refresh Request

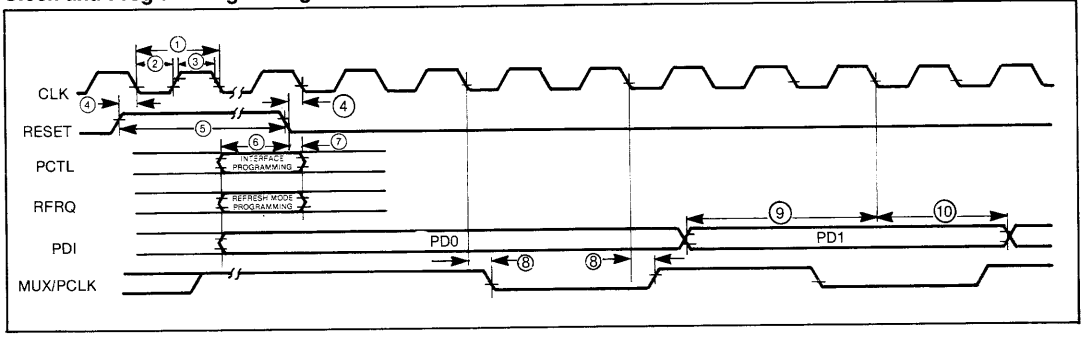
59	TRFVCL	RFRQ to CLK↓ Setup	20		30		ns	
60	TCLRFX	RFRQ to CLK↓ Hold	10		10		ns	
61	TFRFH	Failsafe RFRQ Pulse Width	TCLCL+ 20		TCLCL+ 30		ns	24
62	TRFXCL	Single RFRQ Inactive to CLK↓ Setup	20		30		ns	25
63	TBRFH	Burst RFRQ Pulse Width	2TCLCL+ 20		2TCLCL+ 30		ns	24

NOTES:

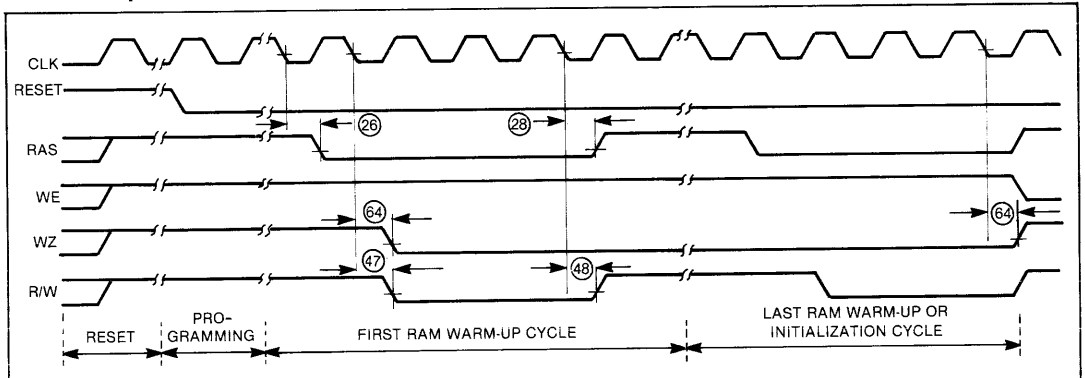
1. Specification when programmed in the Fast Cycle processor mode (iAPX 286 mode).
2. Specification when programmed in the Slow Cycle processor mode (iAPX 186 mode).
3. Must be programmed in Slow Cycle processor mode.
4. RESET is internally synchronized to CLK. Hence, a set-up time is required only to guarantee its recognition at a particular clock edge.
5. The first programming bit (PD0) is also sampled by RESET going low.
6. TCLPDX is guaranteed if programming data is shifted using PCLK.
7. WZ is issued only in ECC mode.
8. TKLCL and TKLCH are not required for an asynchronous command except to guarantee its recognition at a particular clock edge.
9. Valid when programmed in either Fast or Slow Cycle mode.
10. Minimum delay from address inputs to row address outputs is TAVCL − tASR, where tASR ≥ 0 ns; tASR should be specified by user.
11. When programmed in Slow Cycle mode and 125 ns ≤ TCLCL < 200 ns.
12. When programmed in Slow Cycle mode and 200 ns ≤ TCLCL.
13. $C_{AO}/C_{RAS} \geq 0.9$, where C_{AO} is the capacitive load on the address output ($AO_{0\text{-}8}$) pin and C_{RAS} is the capacitive loading of the $\overline{RAS}$ output ($\overline{RAS}_{0\text{-}3}$) pin.
14. When programmed in Fast Cycle mode (WD8207 only) and 62.5 ns ≤ TCLCL < 200 ns.
15. When programmed in Fast Cycle mode (WD8207 only) and 200 ns ≤ TCLCL.
16. $C_{AO}/C_{CAS} \leq 6.5$, where C_{AO} is the capacitive load on the address output ($AO_{0\text{-}8}$) pin and C_{CAS} is the capacitive load on the $\overline{CAS}$ output ($\overline{CAS}_{0\text{-}3}$) pin.
17. TWRLFV is defined for asynchronous $\overline{FWR}$.
18. TFVCL is defined for synchronous $\overline{FWR}$.
19. TCLFV is defined for both synchronous and asynchronous $\overline{FWR}$. In systems in which $\overline{FWR}$ is decoded directly from the address inputs to the WD8207. TCLFV is automatically guaranteed by TCLAV.
20. READ, REFRESH, or PARTIAL WRITE CYCLES: refer to Table 13, to rows marked 'RMW,' for exact clock edges R/$\overline{W}$, $\overline{XACK}$, $\overline{ESTB}$, and WE occur.
21. Synchronous operation only. Must arrive by the second clock falling edge after the clock edge which recognizes the command in order to be effective.
22. LOCK must be held active for the entire period the opposite port must be locked out. Upon release of LOCK the opposite port will be able to obtain access to memory.
23. Asynchronous mode only. In this mode a synchronizer stage is used internally in the WD8207 to synchronize up LOCK. TRWLLKV and TRWHLKX are only required for guaranteeing that LOCK will be recognized for the requesting port, but these parameters are not required for correct WD8207 operation.
24. TFRFH and TBRFH pertain to asynchronous operation only.
25. Single RFRQ cannot by supplied asynchronously.

WAVEFORMS

Clock and Programming Timings



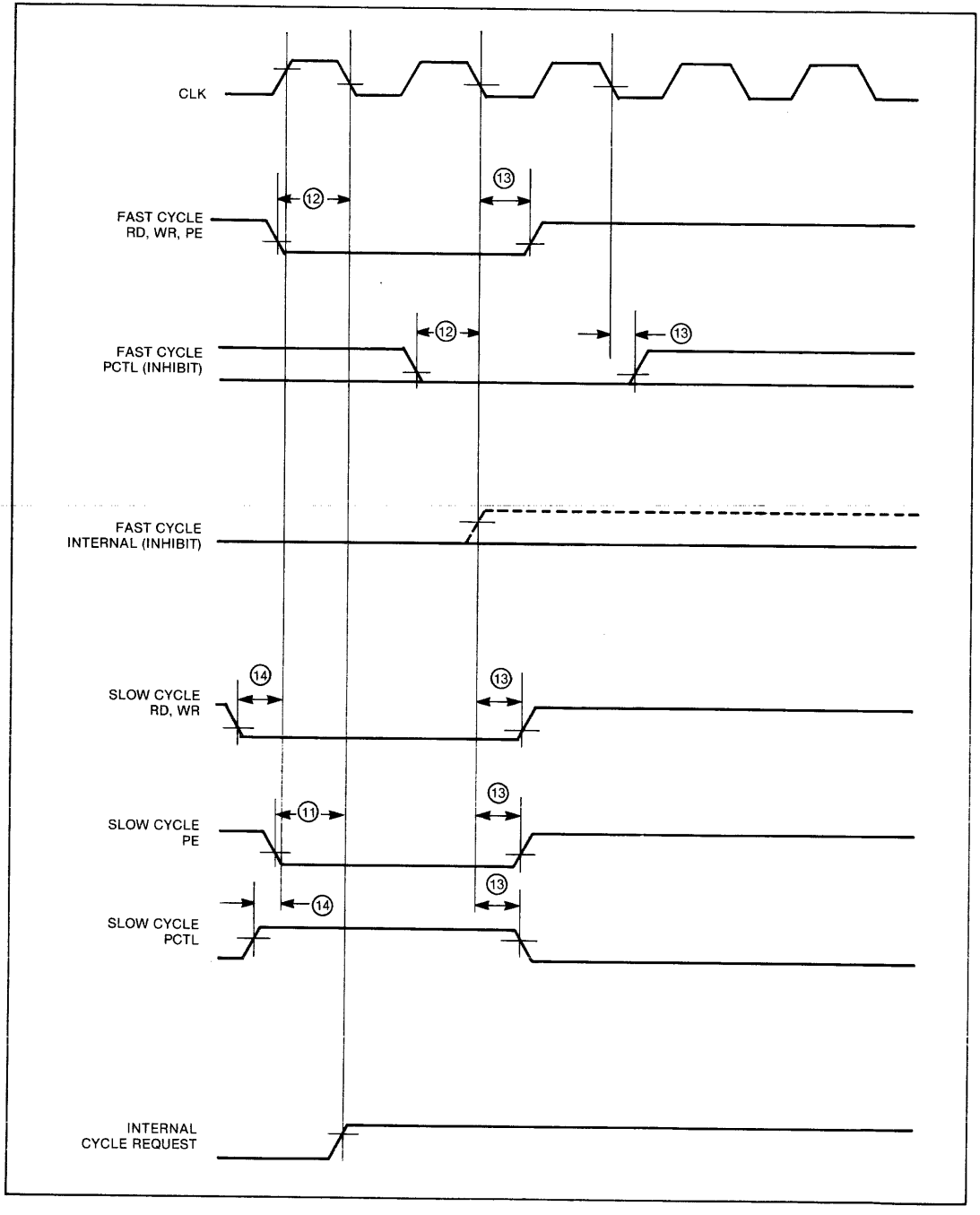
RAM Warm-up and Memory Initialization Cycles



NOTES:
(1) WHEN IN NON-ECC MODE, OR IN ECC MODE WITH THE TM2 PROGRAMMING BIT ON, THERE ARE NO INITIALIZATION CYCLES; WHEN IN ECC MODE WITH TM2 OFF, THE DUMMY CYCLES ARE FOLLOWED BY INITIALIZATION CYCLES.
(2) THE PRESENT EXAMPLE ASSUMES A RAS FOUR CLOCKS LONG.

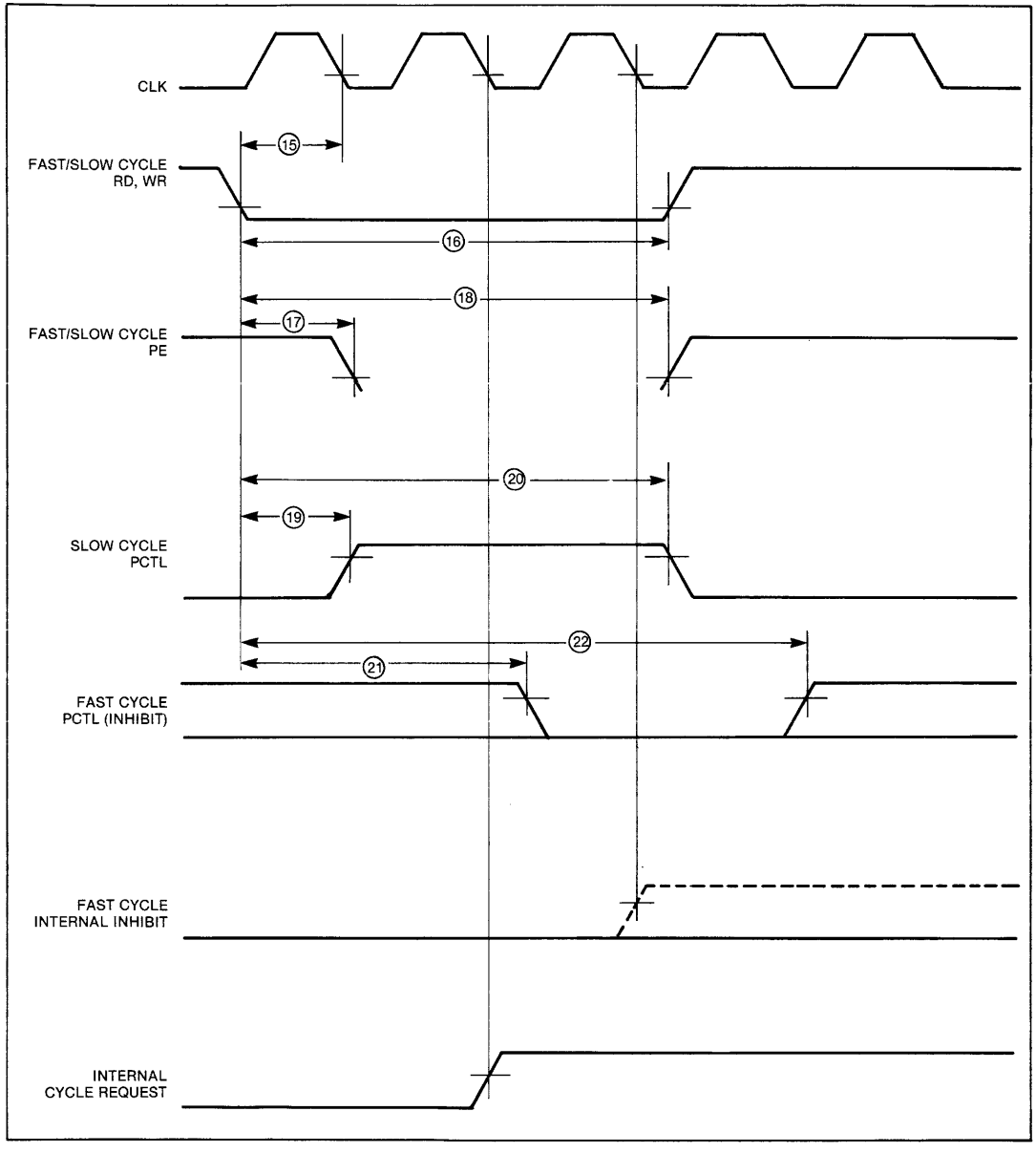
WAVEFORMS (Continued)

Synchronous Port Interface



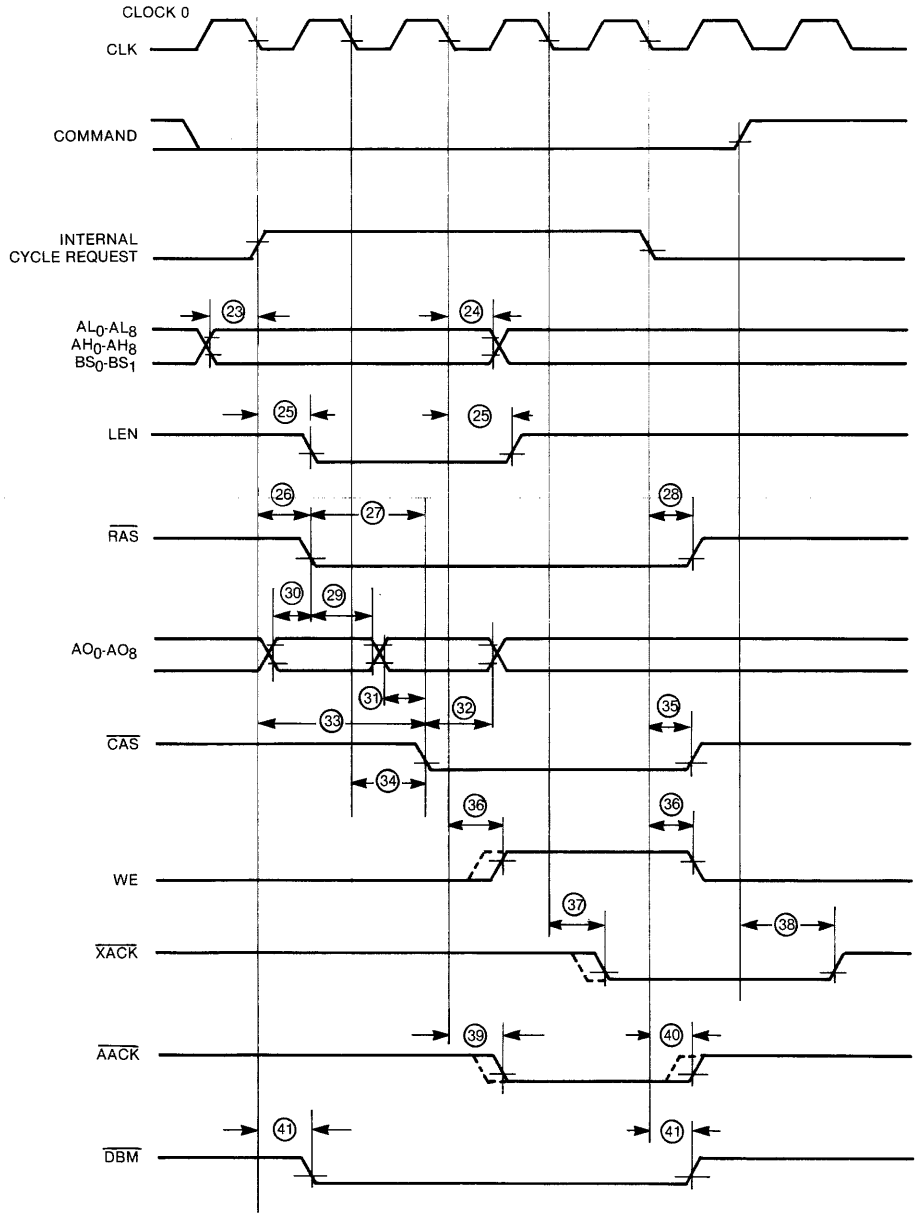
WAVEFORMS (Continued)

Asynchronous Port Interface



WAVEFORMS (Continued)

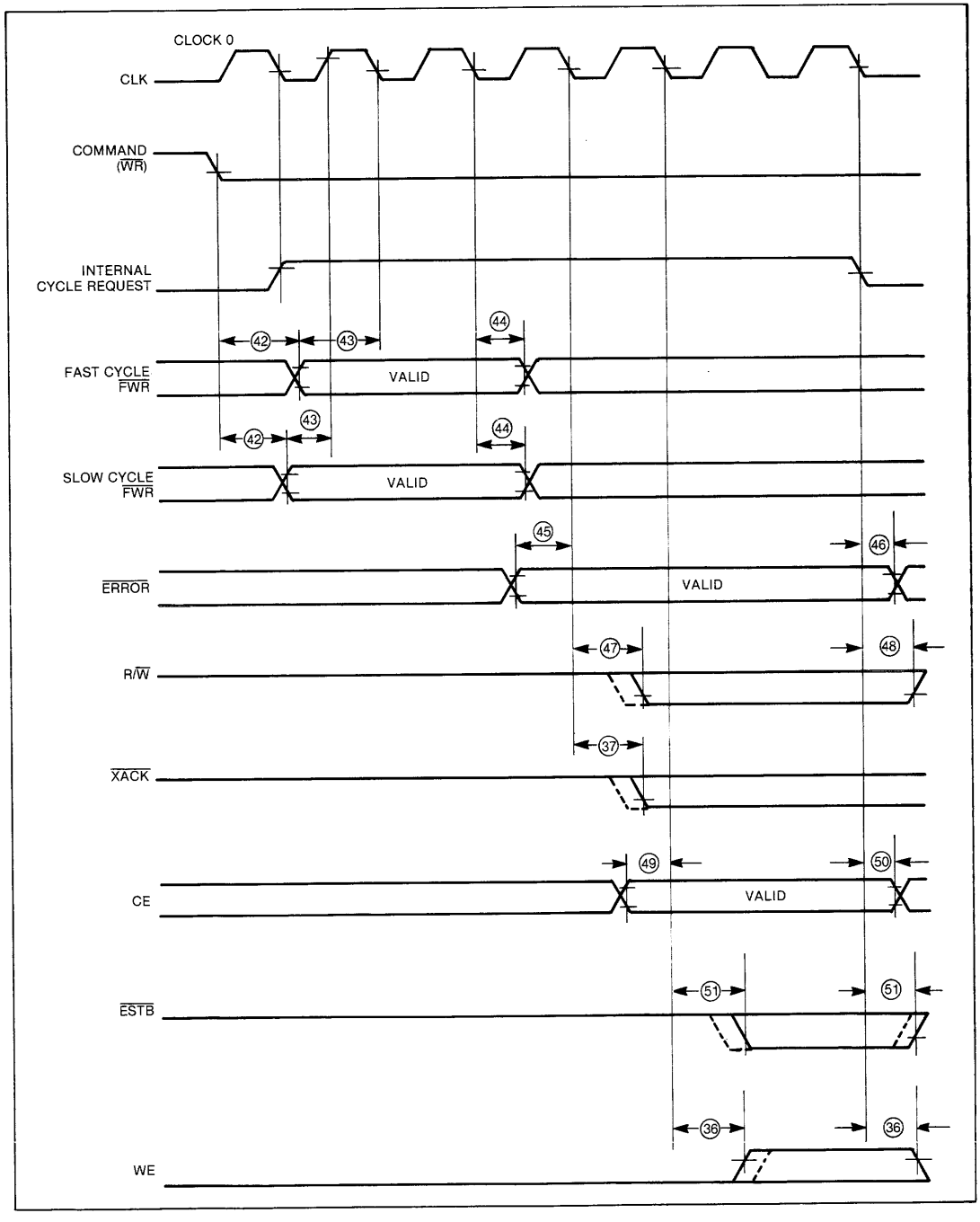
RAM Interface Timing
ECC and Non-ECC Mode



NOTE:
DASHED WAVEFORM INDICATES THAT EITHER CLOCK EDGE MAY CAUSE THE SIGNAL TRANSITION.

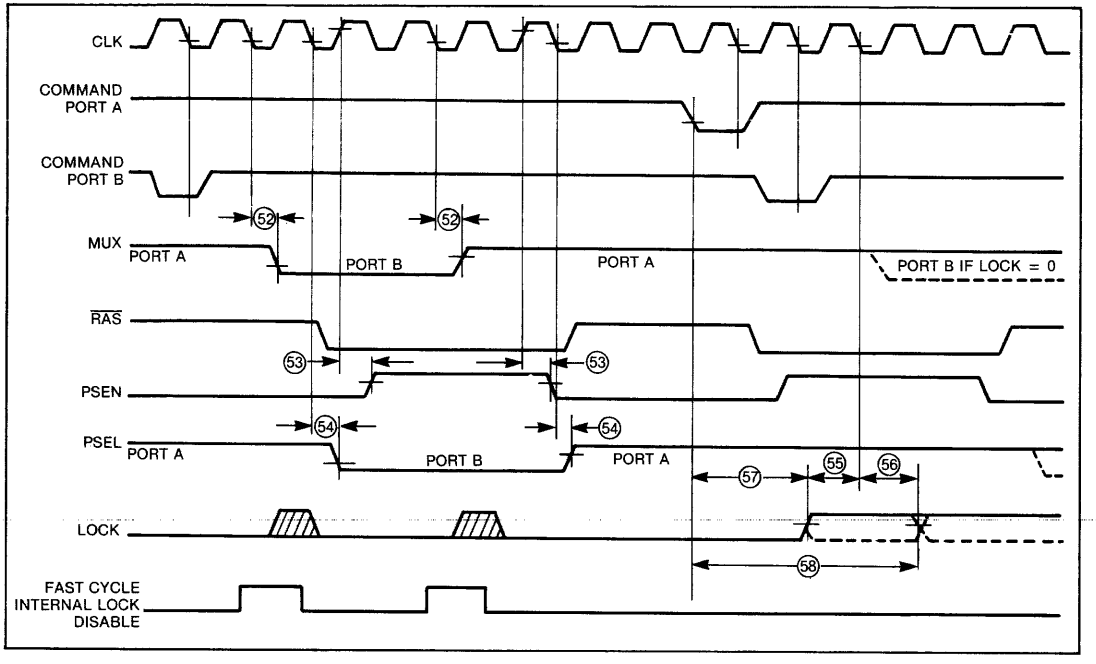
WAVEFORMS (Continued)

ECC Interface Timing

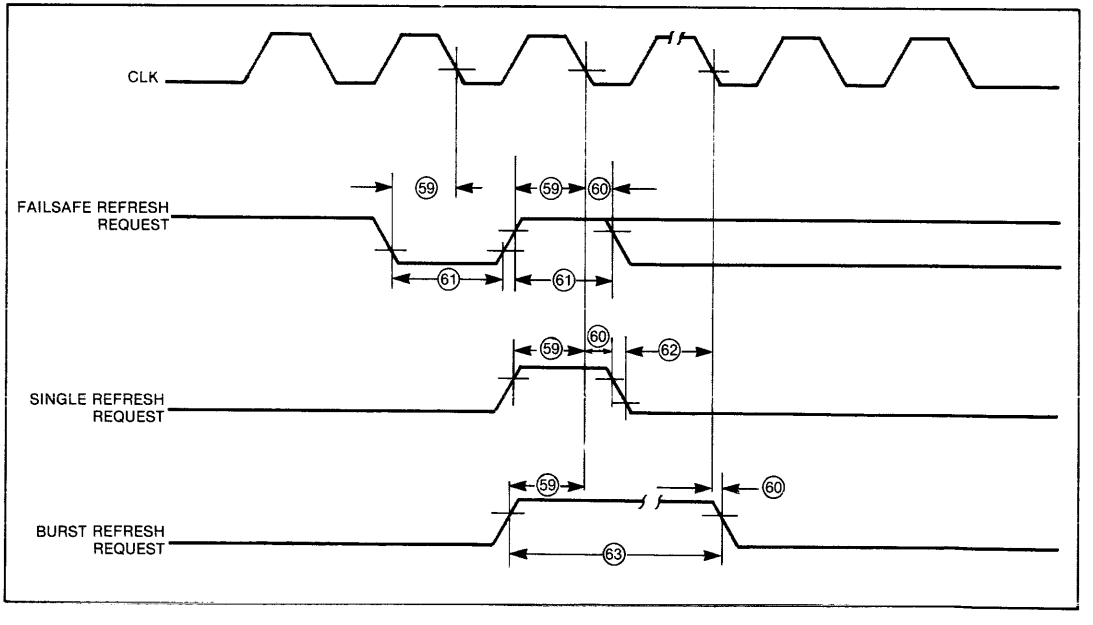


WAVEFORMS (Continued)

Port Switching and Lock Timing



Refresh Request Timing



CONFIGURATION TIMING CHARTS

The timing charts that follow are based on 8 basic system configurations where the WD8207 operates.

Tables 10 and 11 give a description of non-ECC and ECC system configurations based on the WD8207's PD0, PD3, PD4, PD10 and PD11 programming bits.

Table 10. NON-ECC SYSTEM CONFIGURATIONS

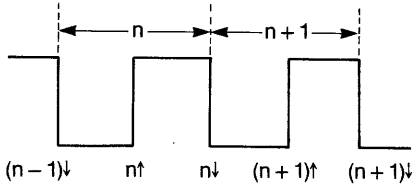
NON-ECC MODE: PD0 = 0				
TIMING CONF.	$\overline{CFS}$ (PD3)	$\overline{RFS}$ (PD4)	EXT (PD10)	$\overline{FFS}$ (PD11)
C_0	(0)	Fast RAM (0)	Not EXT (0)	10 MHz (1)
C_0	(0)	Fast RAM (0)	EXT (1)	10 MHz (1)
C_0	(0)	Slow RAM (1)	Not EXT (0)	10 MHz (1)
C_0	(0)	Slow RAM (1)	EXT (1)	10 MHz (1)
C_0	(0)	Fast RAM (0)	Not EXT (0)	16 MHz (0)
C_1	(0)	Slow RAM (1)	Not EXT (0)	16 MHz (0)
C_1	(0)	Fast RAM (0)	EXT (1)	16 MHz (0)
C_2	(0)	Slow RAM (1)	EXT (1)	16 MHz (0)
C_3	(1)	Fast RAM (0)	Not EXT (0)	8 MHz (0)
C_3	(1)	Slow RAM (1)	Not EXT (0)	8 MHz (0)
C_3	(1)	Fast RAM (0)	EXT (1)	8 MHz (0)
C_3	(1)	Fast RAM (0)	Not EXT (0)	5 MHz (1)
C_3	(1)	Fast RAM (0)	EXT (1)	5 MHz (1)
C_3	(1)	Slow RAM (1)	Not EXT (0)	5 MHz (1)
C_3	(1)	Slow RAM (1)	EXT (1)	5 MHz (1)
C_4	(1)	Slow RAM (1)	EXT (1)	8 MHz (0)

Table 11. ECC SYSTEM CONFIGURATIONS

ECC MODE: PD0 = 1				
TIMING CONF.	CFS (PD3)	RFS (PD4)	$\overline{EXT}$ (PD10)	FFS (PD11)
C_0	(1)	Slow RAM (0)	M/S EDCU (0)	10 MHz (0)
C_0	(1)	Slow RAM (0)	M EDCU (1)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M/S EDCU (0)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M EDCU (1)	10 MHz (0)
C_0	(1)	Fast RAM (1)	M EDCU (1)	16 MHz (1)
C_1	(1)	Slow RAM (0)	M EDCU (1)	16 MHz (1)
C_2	(1)	Fast RAM (1)	M/S EDCU (0)	16 MHz (1)
C_3	(1)	Slow RAM (0)	M/S EDCU (0)	16 MHz (1)
C_4	(0)	Slow RAM (0)	M/S EDCU (0)	5 MHz (0)
C_4	(0)	Fast RAM (1)	M/S EDCU (0)	5 MHz (0)
C_4	(0)	Slow RAM (0)	M EDCU (1)	8 MHz (1)
C_4	(0)	Fast RAM (1)	M EDCU (1)	8 MHz (1)
C_5	(0)	Slow RAM (0)	M/S EDCU (0)	8 MHz (1)
C_5	(0)	Fast RAM (1)	M/S EDCU (0)	8 MHz (1)
C_6	(0)	Slow RAM (0)	M EDCU (1)	5 MHz (0)
C_6	(0)	Fast RAM (1)	M EDCU (1)	5 MHz (0)

Using the Timing Charts

The notation used to indicate which clock edge triggers an output transition is "n↑" or "n↓", where "n" is the number of clock periods that have passed since clock 0, the reference clock, and "↑" refers to rising edge and "↓" to falling edge. A clock period is defined as the interval from a clock falling edge to the following falling edge. Clock edges are defined as shown below.



The clock edges which trigger transitions on each WD8207 output are tabulated in Table 12 for non-ECC mode, and Table 13 for ECC mode. "H" refers to the high-going transition, and "L" to low-going transition; "V" refers to valid, and "$\overline{V}$" to non-valid.

Clock 0 is defined as the clock in which the WD8207 begins a memory cycle, either as a result of a port request which has just arrived, or of a port request which was stored previously but could not be serviced at the time of its arrival because the WD8207 was performing another memory cycle. Clock 0 may be identified externally by the leading edge of RAS, which is always triggered on 0↓.

Notes for interpreting the timing charts.

1. **PSEL — valid** is given as the latest time it can occur. It is entirely possible for PSEL to become valid before the time given. In a refresh cycle, PSEL can switch as defined in the chart, but it has no bearing on the refresh cycle itself, but only on a subsequent cycle for one of the external ports.
2. **LEN — low** is given as the latest time it can occur. LEN is only activated by port A configured in Fast Cycle, and thus it is not activated by a refresh cycle, although it may be activated by port A during a refresh cycle.
3. In non-ECC mode the $\overline{CAS}$, $\overline{EAACK}$, $\overline{LAACK}$ and $\overline{XACK}$ outputs are not issued during refresh.
4. In ECC mode there are really seven types of cycles: Read without error, read with error, full write, partial write without error, partial write with error, refresh without error, and refresh with error. These cycles may be derived from the timing chart as follows:
   A. Read without error: Use row marked 'RD, RF.'
   B. Read with error: Use row marked 'RMW,' except for $\overline{EAACK}$ and $\overline{LAACK}$, which should be taken from 'RD, RF.' If the error is uncorrectable, WE will not be issued.
   C. Full write: Use row marked 'WR.'
   D. Partial write without error: Use row marked 'RMW,' except that $\overline{DBM}$ and $\overline{ESTB}$ will not be issued.
   E. Partial write with error: Use row marked 'RMW,' except that $\overline{DBM}$ will not be issued. If the error is uncorrectable, WE will not be issued.
   F. Refresh without error: Use row marked 'RD, RF.' except that $\overline{ESTB}$, $\overline{EAACK}$, $\overline{LAACK}$, and $\overline{XACK}$ will not be issued.
   G. Refresh with error: Use row marked 'RMW' except that $\overline{EAACK}$, $\overline{LAACK}$, $\overline{ESTB}$, and $\overline{XACK}$ will not be issued. If the error is uncorrectable WE will not be issued.
5. **XACK — high** is reset asynchronously by command going inactive and not by a clock edge.
6. **MUX — valid** is given as the latest time it can occur.

Table 12A. TIMING CHART — NON-ECC MODE

		PSEN		PSEL		$\overline{DBM}$		LEN		$\overline{RAS}$		CAS		WE	
C_n	CYCLE	H	L	V	$\overline{V}$	L	H	L	H	L	H	L	H	H	L
C_0	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	1↓	4↓		
C_0	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↓	5↓
C_1	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓		
C_1	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↑	5↓
C_2	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓		
C_2	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	1↓	5↓	2↓	5↓
C_3	RD, RF	1↑	2↑	0↓	3↓	0↓	3↓	0↓	2↓	0↓	3↓	0↓	3↓		
C_3	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	2↑	4↓
C_4	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	4↓	0↓	4↓		
C_4	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	2↑	4↓

Table 12B. TIMING CHART — NON-ECC MODE

		$\overline{EAACK}$		$\overline{LAACK}$		$\overline{XACK}$		MUX	
C_n	CYCLE	L	H	L	H	L	H	V	V
C_0	RD, RF	1↓	4↓	2↓	5↓	3↓	RD	−2↓	2↓
C_0	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_1	RD, RF	2↓	5↓	2↓	5↓	4↓	RD	−2↓	2↓
C_1	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_2	RD, RF	2↓	5↓	3↓	6↓	4↓	RD	−2↓	2↓
C_2	WR	1↓	4↓	1↓	4↓	3↓	WR	−2↓	2↓
C_3	RD, RF	0↓	3↓	1↓	3↓	2↓	RD	−1↓	2↓
C_3	WR	0↓	2↓	1↑	3↑	2↓	WR	−1↓	2↓
C_4	RD, RF	1↓	3↓	1↓	3↓	3↑	RD	−1↓	2↓
C_4	WR	0↓	2↓	1↑	3↑	2↓	WR	−1↓	2↓

Table 13A. TIMING CHART — ECC MODE

		PSEN		PSEL		DBM		LEN		RAS		CAS		R/W		WE	
C_n	CYCLE	H	L	V	V	L	H	L	H	L	H	L	H	L	H	H	L
C_0	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓				
C_0	WR	1↑	6↑	0↓	6↓			0↓	2↓	0↓	6↓	1↓	6↓	1↓	6↓	3↓	6↓
C_0	RMW	1↑	9↑	0↓	9↓	0↓	9↓	0↓	2↓	0↓	9↓	1↓	9↓	4↓	9↓	6↓	9↓
C_1	RD, RF	1↑	6↑	0↓	6↓	0↓	6↓	0↓	2↓	0↓	4↓	1↓	6↓				
C_1	WR	1↑	6↑	0↓	6↓			0↓	2↓	0↓	6↓	1↓	6↓	1↓	6↓	3↓	6↓
C_1	RMW	1↑	9↑	0↓	9↓	0↓	9↓	0↓	2↓	0↓	9↓	1↓	9↓	4↓	9↓	6↓	9↓
C_2	RD, RF	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	5↓	1↓	7↓				
C_2	WR	1↑	7↑	0↓	7↓			0↓	2↓	0↓	7↓	1↓	7↓	1↓	7↓	4↓	7↓
C_2	RMW	1↑	11↑	0↓	11↓	0↓	11↓	0↓	2↓	0↓	11↓	1↓	11↓	5↓	11↓	8↓	11↓
C_3	RD, RF	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	5↓	1↓	7↓				
C_3	WR	1↑	7↑	0↓	7↓			0↓	2↓	0↓	7↓	1↓	7↓	1↓	7↓	4↓	7↓
C_3	RMW	1↑	11↑	0↓	11↓	0↓	11↓	0↓	2↓	0↓	11↓	1↓	11↓	5↓	11↓	8↓	11↓
C_4	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_4	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	0↓	5↓	1↓	5↓	3↓	5↓
C_4	RMW	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	7↓	0↓	7↓	3↓	7↓	5↓	7↓
C_5	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_5	WR	1↑	5↑	0↓	5↓			0↓	2↓	0↓	5↓	0↓	5↓	1↓	5↓	3↓	5↓
C_5	RMW	1↑	7↑	0↓	7↓	0↓	7↓	0↓	2↓	0↓	7↓	0↓	7↓	3↓	7↓	5↓	7↓
C_6	RD, RF	1↑	4↑	0↓	4↓	0↓	4↓	0↓	2↓	0↓	3↓	0↓	4↓				
C_6	WR	1↑	4↑	0↓	4↓			0↓	2↓	0↓	4↓	0↓	4↓	1↓	4↓	2↓	4↓
C_6	RMW	1↑	5↑	0↓	5↓	0↓	5↓	0↓	2↓	0↓	5↓	0↓	5↓	2↑	5↓	3↑	5↓

WD8207 — DRAM Interface Parameter Equations

Several DRAM parameters, but not all, are a direct function of WD8207 timings, and the equations for these parameters are given in the following tables. The following is a list of those DRAM parameters which have NOT been included in the following tables, with an explanation for their exclusion.

READ, WRITE, READ-MODIFY-WRITE & REFRESH CYCLES

tRAC: response parameter.
tCAC: response parameter.
tREF: See "Refresh Period Options"
tCRP: must be met only if CAS-only cycles, which do not occur with WD8207, exist.
tRAH: See "AC Characteristics"
tRCD: See "AC Characteristics"
tASC: See "AC Characteristics"
tASR: See "AC Characteristics"
tOFF: response parameter.

READ & REFRESH CYCLES

tRCH: WE always goes active after $\overline{CAS}$ goes active, hence tRCH is guaranteed by tCPN.

WRITE CYCLE

tRC: guaranteed by tRWC.
tRAS: guaranteed by tRRW.
tCAS: guaranteed by tCRW.
tWCS: WE always activated after $\overline{CAS}$ is activated, except in memory initialization, hence tWCS is always negative (this is important for RMW only) except in memory initialization; in memory initialization tWCS is positive and has several clocks of margin.
tDS: system-dependent parameter.
tDH: system-dependent parameter.
tDHR: system-dependent parameter.

READ-MODIFY-WRITE CYCLE

tRWD: don't care in WD8207 write cycles, but tabulated for WD8207 RMW cycles.
tCWD: don't care in WD8207 write cycles, but tabulated for WD8207 RMW cycles.

Table 13B. TIMING CHART — ECC MODE

		$\overline{ESTB}$		$\overline{EAACK}$		$\overline{LAACK}$		$\overline{XACK}$		MUX	
C_n	CYCLE	L	H	L	H	L	H	L	H	V	$\overline{V}$
C_0	RD, RF			2↓	5↓	3↓	6↓	4↓	$\overline{RD}$	– 2↓	2↓
C_0	WR			2↓	5↓	2↓	5↓	4↓	$\overline{WR}$	– 2↓	2↓
C_0	RMW	6↓	8↓	5↓	8↓	5↓	8↓	7↓	$\overline{WR}$	– 2↓	2↓
C_1	RD, RF			3↓	6↓	3↓	6↓	4↓	$\overline{RD}$	– 2↓	2↓
C_1	WR			2↓	5↓	2↓	5↓	4↓	$\overline{WR}$	– 2↓	2↓
C_1	RMW	6↓	8↓	5↓	8↓	5↓	8↓	7↓	$\overline{WR}$	– 2↓	2↓
C_2	RD, RF			4↓	7↓	4↓	7↓	5↓	$\overline{RD}$	– 2↓	2↓
C_2	WR			3↓	6↓	3↓	6↓	5↓	$\overline{WR}$	– 2↓	2↓
C_2	RMW	8↓	10↓	7↓	10↓	7↓	10↓	9↓	$\overline{WR}$	– 2↓	2↓
C_3	RD, RF			4↓	7↓	5↓	8↓	5↓	$\overline{RD}$	– 2↓	2↓
C_3	WR			3↓	6↑	3↓	6↓	5↓	$\overline{WR}$	– 2↓	2↓
C_3	RMW	8↓	10↓	7↓	10↓	7↓	10↓	9↓	$\overline{WR}$	– 2↓	2↓
C_4	RD, RF			1↓	3↓	2↑	4↑	3↑	$\overline{RD}$	– 1↓	2↓
C_4	WR			1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	– 1↓	2↓
C_4	RMW	5↑	6↑	3↓	5↓	4↑	6↑	5↓	$\overline{WR}$	– 1↓	2↓
C_5	RD, RF			2↓	4↓	3↑	5↑	3↑	$\overline{RD}$	– 1↓	2↓
C_5	WR			1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	– 1↓	2↓
C_5	RMW	5↑	6↑	3↓	5↓	4↑	6↑	5↓	$\overline{WR}$	– 1↓	2↓
C_6	RD, RF			1↓	3↓	1↑	3↑	2↑	$\overline{RD}$	– 1↓	2↓
C_6	WR			1↓	3↓	1↑	3↑	2↓	$\overline{WR}$	– 1↓	2↓
C_6	RMW	3↑	4↑	1↓	3↓	2↑	4↑	3↓	$\overline{WR}$	– 1↓	2↓

Table 14. NON-ECC MODE — RD, RF CYCLES

	FAST CYCLE CONFIGURATIONS			SLOW CYCLE CONFIGURATIONS		
PARAMETER	C_0	C_1	C_2	C_3	C_4	NOTES
tRP	3TCLCL—T26	4TCLCL—T26	4TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	2TCLCL—T34	3TCLCL—T34	3TCLCL—T34	3TCLCL—T34	4TCLCL—T34	1
tCSH	4TCLCL—T26	6TCLCL—T26	6TCLCL—T26	3TCLCL—T26	4TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	3/30	2
tRC	6TCLCL	8TCLCL	8TCLCL	5TCLCL	6TCLCL	1
tRAS	3TCLCL—T26	4TCLCL—T26	4TCLCL—T26	3TCLCL—T26	4TCLCL—T26	1
tCAS	3TCLCL—T34	5TCLCL—T34	5TCLCL—T34	3TCLCL—T34	4TCLCL—T34	1
tRCS	2TCLCL—TCL —T36—TBUF	2TCLCL—TCL —T36—TBUF	2TCLCL—TCL —T36—TBUF	1.5TCLCL—TCL —T36—TBUF	1.5TCLCL—TCL —T36—TBUF	1

Table 15. NON-ECC MODE — WR CYCLE

PARAMETER	FAST CYCLE CONFIGURATIONS			SLOW CYCLE CONFIGURATIONS		NOTES
	C_0	C_1	C_2	C_3	C_4	
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tCSH	5TCLCL—T26	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	3/30	2
tRWC	8TCLCL	8TCLCL	8TCLCL	6TCLCL	6TCLCL	1
tRRW	5TCLCL—T26	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCRW	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tWCH	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	3TCLCL + TCL —T34	1,3
tWCR	4TCLCL + TCL —T26	4TCLCL + TCL —T26	4TCLCL + TCL —T26	3TCLCL + TCL —T26	3TCLCL + TCL —T26	1,3
tWP	2TCLCL + TCL —T36—TBUF	2TCLCL + TCL —T36—TBUF	2TCLCL + TCL —T36—TBUF	2TCLCL—TCL —TBUF	2TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—TCL —TBUF	3TCLCL—TCL —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

Table 16A. ECC MODE — RD, RF CYCLES

PARAMETER	FAST CYCLE MODE				NOTES
	C_0	C_1	C_2	C_3	
tRP	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCPN	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	3TCLCL—T35	1
tRSH	3TCLCL—T34	3TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tCSH	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRC	8TCLCL	8TCLCL	9TCLCL	9TCLCL	1
tRAS	4TCLCL—T26	4TCLCL—T26	5TCLCL—T26	5TCLCL—T26	1
tCAS	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tRCS	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	1

Table 16B. ECC MODE — RD, RF CYCLES

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	1.5TCLCL—T35	1.5TCLCL—T35	1.5TCLCL—T35	1
tRSH	3TCLCL—T34	3TCLCL—T34	3TCLCL—T34	1
tCSH	4TCLCL—T26	4TCLCL—T26	4TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRC	5TCLCL	5TCLCL	5TCLCL	1
tRAS	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCAS	4TCLCL—T34	4TCLCL—T34	4TCLCL—T34	1
tRCS	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	1

Table 17A. ECC MODE — WR CYCLE

PARAMETER	FAST CYCLE MODE				
	C_0	C_1	C_2	C_3	NOTES
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	1
tRSH	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tCSH	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRWC	9TCLCL	9TCLCL	10TCLCL	10TCLCL	1
tRRW	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1
tCRW	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1
tWCH	5TCLCL—T34	5TCLCL—T34	6TCLCL—T34	6TCLCL—T34	1,4
tWCR	6TCLCL—T26	6TCLCL—T26	7TCLCL—T26	7TCLCL—T26	1,4
tWP	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1

Table 17B. ECC MODE — WR CYCLE

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	2.5TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1
tCSH	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRWC	7TCLCL	7TCLCL	6TCLCL	1
tRRW	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1
tCRW	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1
tWCH	5TCLCL—T34	5TCLCL—T34	4TCLCL—T34	1,4
tWCR	5TCLCL—T26	5TCLCL—T26	4TCLCL—T26	1,4
tWP	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tRWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tCWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

Table 18A. ECC MODE — RMW

PARAMETER	FAST CYCLE MODE				
	C_0	C_1	C_2	C_3	NOTES
tRP	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tCPN	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	4TCLCL—T35	1
tRSH	8TCLCL—T34	8TCLCL—T34	10TCLCL—T34	10TCLCL—T34	1
tCSH	9TCLCL—T26	9TCLCL—T26	11TCLCL—T26	11TCLCL—T26	1
tCAH	TCLCL—T34	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	3TCLCL—T26	3TCLCL—T26	3TCLCL—T26	1
tT	3/30	3/30	3/30	3/30	2
tRWC	12TCLCL	12TCLCL	14TCLCL	14TCLCL	1
tRRW	9TCLCL—T26	9TCLCL—T26	11TCLCL—T26	11TCLCL—T26	1
tCRW	8TCLCL—T34	8TCLCL—T34	10TCLCL—T34	10TCLCL—T34	1
tRCS	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	TCLCL—T36 —TBUF	1
tRWD	6TCLCL—T26	6TCLCL—T26	8TCLCL—T26	8TCLCL—T26	1
tCWD	5TCLCL—T34	5TCLCL—T34	7TCLCL—T34	7TCLCL—T34	1
tWP	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tRWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1
tCWL	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	3TCLCL—T36 —TBUF	1

Table 18B. ECC MODE — RMW

PARAMETER	SLOW CYCLE MODE			
	C_4	C_5	C_6	NOTES
tRP	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tCPN	2.5TCLCL—T35	2.5TCLCL—T35	2.5TCLCL—T35	1
tRSH	7TCLCL—T34	7TCLCL—T34	5TCLCL—T34	1
tCSH	7TCLCL—T26	7TCLCL—T26	5TCLCL—T26	1
tCAH	2TCLCL—T34	2TCLCL—T34	2TCLCL—T34	1
tAR	2TCLCL—T26	2TCLCL—T26	2TCLCL—T26	1
tT	3/30	3/30	3/30	2
tRWC	9TCLCL	9TCLCL	7TCLCL	1
tRRW	7TCLCL—T26	7TCLCL—T26	5TCLCL—T26	1
tCRW	7TCLCL—T34	7TCLCL—T34	5TCLCL—T34	1
tRCS	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	0.5TCLCL—T36 —TBUF	1
tRWD	4TCLCL + TCL —T26	4TCLCL + TCL —T26	2TCLCL + TCL —T26	1
tCWD	4TCLCL + TCL —T34	4TCLCL + TCL —T34	2TCLCL + TCL —T34	1
tWP	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tRWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1
tCWL	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	3TCLCL—TCL —T36—TBUF	1

NOTES:
1. Minimum.
2. Value on right is maximum; value on left is minimum.
3. Applies to the eight warm-up cycles during initialization only.
4. Applies to the eight warm-up cycles and to the memory initialization cycles during initialization only.
5. TP = TCLCL
   T26 = TCLRSL
   T34 = TCLCSL
   T35 = TCLCSH
   T36 = TCLW
   TBUF = TTL Buffer delay

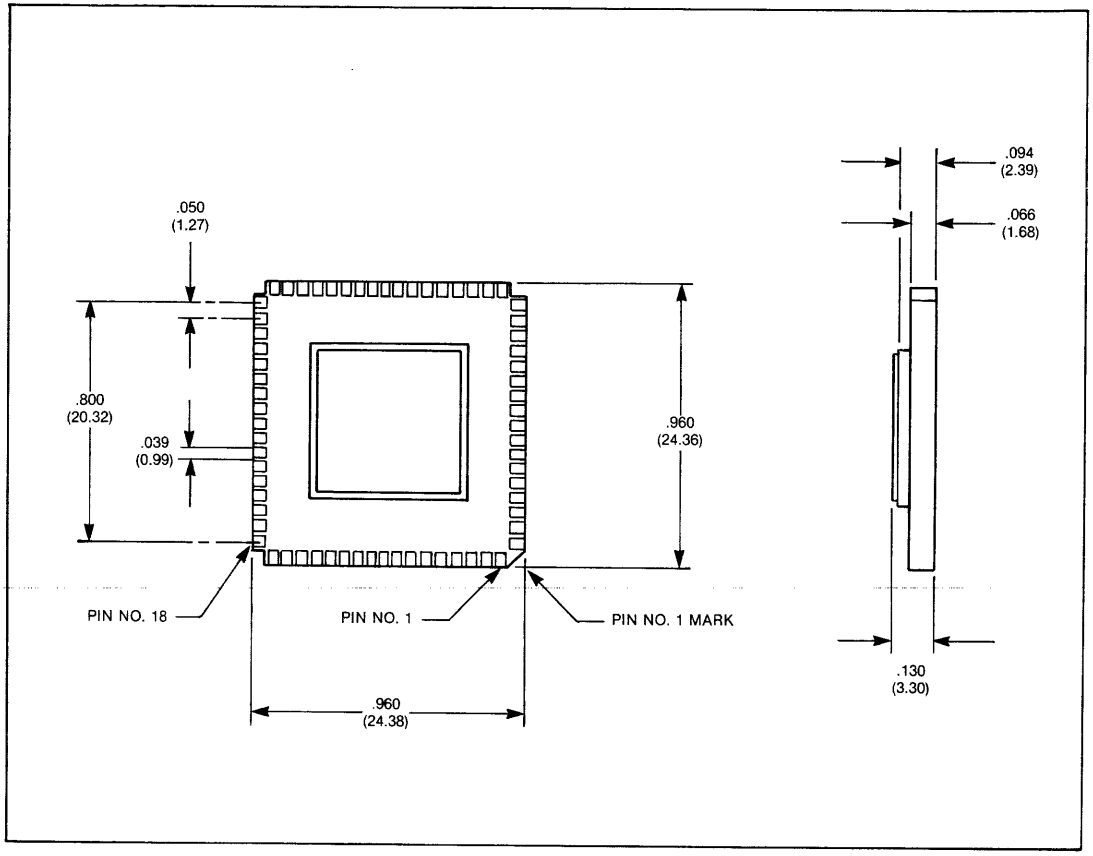


Figure 18. WD8207 JEDEC TYPE A PACKAGE

See page 481 for ordering information.

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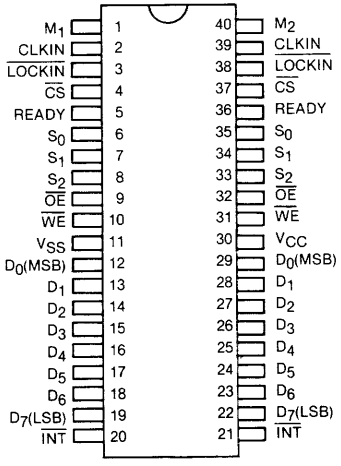
PRELIMINARY

WD99650 Multiprocessor Interface Device

FEATURES

- TWO FULLY INDEPENDENT, ASYNCHRONOUS PORTS
- EIGHT PROGRAMMABLE 8-BIT REGISTERS PER PORT
- STATUS AND CONTROL REGISTERS
- INTERRUPT REQUEST CONTROL AT EACH PORT
- POINTER REGISTERS INCREMENTABLE FOLLOWING RAM ACCESS
- MESSAGE REGISTERS TO PASS DATA BETWEEN PORTS INDEPENDENT OF RAM ARBITRATION LOGIC
- 256 BYTES OF RAM ADDRESSED INDIRECTLY USING POINTER REGISTERS
- HARDWARE SUPPORT FOR UTILIZATION OF RAM AS FIRST-IN FIRST-OUT (FIFO) BUFFER BETWEEN PORTS
- WIDTH OF DATA PATH EXPANDABLE IN 8-BIT INCREMENTS
- INTERNAL ARBITRATION OF ASYNCHRONOUS RAM-ACCESS CONFLICTS
- OPTIONAL READY SIGNAL FOR CONCURRENT USE OF THE MEMORY BY BOTH PORTS
- READY SYNCHRONIZED ON CHIP; CLKIN REQUIRED ONLY IF READY IS USED
- HARDWARE LOCKOUT CAPABILITY PROVIDED TO SUPPORT TEST-AND-SET, TEST-AND-CLEAR OPERATIONS
- SOFTWARE LOCKOUT FACILITY WITH INTERRUPT FOR CONFIRMATION
- SINGLE +5V SUPPLY
- 40-PIN DIP PACKAGE
- N-CHANNEL SILICON-GATE TECHNOLOGY



PIN DESIGNATION

DESCRIPTION

The WD99650 Multiprocessor Interface device (MPIF) provides a bit-parallel, asynchronous communications interface for passing messages and data between two processors or processor systems. It represents a standard peripheral interface consisting of eight programmable registers at each of its two ports and furnishes access to 256 bytes of random-access (RAM) used to buffer data transmitted between ports. The WD99650 supplies arbitration logic to resolve RAM-access conflicts between the two processor systems. The WD99650 can be used to connect virtually any 8-bit or 16-bit microprocessor to any other 8-bit or 16-bit microprocessor having the capability of interfacing to standard memory or peripheral devices.

PIN DESCRIPTION

SYMBOL	PIN NUMBER PORT A	PIN NUMBER PORT B	TYPE I/O	DESCRIPTION
M_1 M_2	1 40			MODE PINS: Reset the MPIF and establish whether it is to work in master, slave, or stand-alone mode.
CLKIN	2	39	I	CLOCK-IN: Allows READY to be presented synchronously to the host system.
$\overline{LOCKIN}$	3	38	I	LOCKOUT IN: Indicates to the MPIF that the opposite port should be denied access to the RAM.
$\overline{CS}$	4	37	I	CHIP SELECT: Indicates that the host system requires access to one of the MPIF internal registers.
READY	5	36	O	READY: Indicates to the host system that the memory operation in progress may be completed.
S_0	6	35	I	REGISTER SELECT LINES: Indicate to the MPIF which internal register is accessed by the host system.
S_1	7	34	I	
S_2	8	33	I	
$\overline{OE}$	9	32	I	OUTPUT ENABLE: Indicates that the host system is performing a read operation.
$\overline{WE}$	10	31	I	WRITE ENABLE: Indicates that the host is performing a write operation.
V_{CC}	30			POWER SUPPLY
V_{SS}	11			GROUND REFERENCE
D_0(MSB)	12	29	I/O	DATA BUS: Provides for bidirectional data transfer between the MPIF port and the host system.
D_1	13	28	I/O	
D_2	14	27	I/O	
D_3	15	26	I/O	
D_4	16	25	I/O	
D_5	17	24	I/O	
D_6	18	23	I/O	
D_7(LSB)	19	22	I/O	
$\overline{INT}$	20	21	O(o/d)*	INTERRUPT: Indicates to the host system that it should branch to a service routine.

*o/d = open drain output: all others are push/pull outputs.

ARCHITECTURE

The WD99650 Multiprocessor Interface, shown in Figure 1 as a block diagram, is built around a 256 x 8-bit static random-access memory and includes two complete microprocessor interfaces and two complete data paths. Each data path connects the microprocessor interface to the appropriate on-chip registers under the control of the external interface control signals, register select lines, and the arbitration latch.

Both interfaces have access to the RAM via data registers, which are simple bidirectional buffers between the RAM and the data paths and involve no storage.

Each data register has associated with it an address pointer register that supplies the address to the RAM when the corresponding data register is used. The address registers can be written to and read from both microprocessor interfaces.

Two message registers are provided, one assigned to each port. Each interface can read and write its own message register but only read that of the other interface.

The control register provides for the configuration and control of the WD99650. It includes the various Interrupt enable bits.

The status register shows the condition of the various interrupt sources.

The RAM can only be used by one host microprocessor, via its data register, at one time. The two outputs of the arbitration latch, ACTA and ACTB, control access to the RAM. These outputs select the RAM data and address buses from either the DATA A and ADDR A registers or the DATA B and ADDR B registers respectively. ACTA becomes true when the data register of port A is addressed, but only if ACTB is not already true and port B has not asserted a lockout. A corresponding definition applies for ACTB. Hence, the two signals are mutually exclusive, which ensures that both interfaces cannot use the RAM at once: The WD99650 provides its host microprocessors with continuous access to all the other registers.

If both interfaces try to gain access to the RAM concurrently, the first to address its data register will exclude the other. The RAM is assigned on a first-come, first-serve basis unless a lockout is in effect (see Lockout Capability).

Occasionally, both ports may address their data registers at exactly the same time. This can put the arbitration latch into an indeterminate state for some time. Due to the cross-coupled nature of ACTA and ACTB, the indeterminate state will be unstable. Eventually the conflict will resolve itself, the outcome being essentially random. ACTA and ACTB pass through threshold circuits to ensure that the unstable state is interpreted as an inactive state for both bits.

Each interface can request exclusive use of the RAM using the lockout feature. This is asserted by means of a software-accessible bit or with a dedicated input pin. In situations where both ports assert a lockout, the RAM is assigned on a first-come, first-serve basis.

A memory cycle cannot be allowed to proceed if the port concerned does not succeed in getting access to the RAM or there is uncertainty in the arbitration latch. The problem of sharing the RAM between two ports may be approached in three ways:

1. Ensure in software that both host ports do not try to use the RAM at the same time. Thus any attempt to gain access to the RAM is guaranteed to be successful. This involves the two systems passing messages between themselves regarding their status and intentions, for which the message registers may be used.
2. Use the READY signal provided by the WD99650 to put the system into a wait state if it is not successful in gaining access to the RAM or if uncertainty exists in the arbitration latch.
3. Use the software-accessible lockout bit to request exclusive use of the RAM. Wait until this is acknowledged before attempting access to the RAM.

It is possible to use method 2 on one port and 3 on the other port.

REGISTER DESCRIPTION

The WD99650 occupies eight locations in the memory map of each host system. It is so arranged that the registers accessible at the same location of each port serve the same function. The ports of the WD99650 are therefore completely identical and can be reversed without software or hardware changes. For the purpose of naming the locations in the memory map, the port under consideration is referred to as the local port and the other is referred to as the remote port. The location and function of each register is shown in Table 1.

DATA REGISTERS

Each port can read and write its own data register at the two memory locations designated as Data and Data/Increment. If a memory operation is performed to the RAM via the data/increment location, the corresponding address pointer register will be incremented on completion of the memory cycle. This will not happen if the Data location is used.

ADDRESS POINTER REGISTERS

Each port can read and write its own address pointer register at the location designated as the Local Address Pointer and can read and write the other port's pointer at the Remote Address Pointer location. This enables each port to determine where in the RAM it will operate by setting up its own address pointer register. Alternatively, the management of the RAM can be under the control of only one port, which sets up both address pointers. Each pointer register will cycle through the value FF_{16} increments to OO_{16}. The following limitations apply to the use of these locations:

1. If either address pointer is read while its value is being changed by a write operation from the other port, an erroneous value may be read.
2. A port should not write to its remote address pointer location while there is a possibility that the other port could perform a memory operation to the RAM. This can result in the address pointer being changed during a memory operation and data in the RAM being corrupted.

Figure 1.
WD99650
BLOCK DIAGRAM

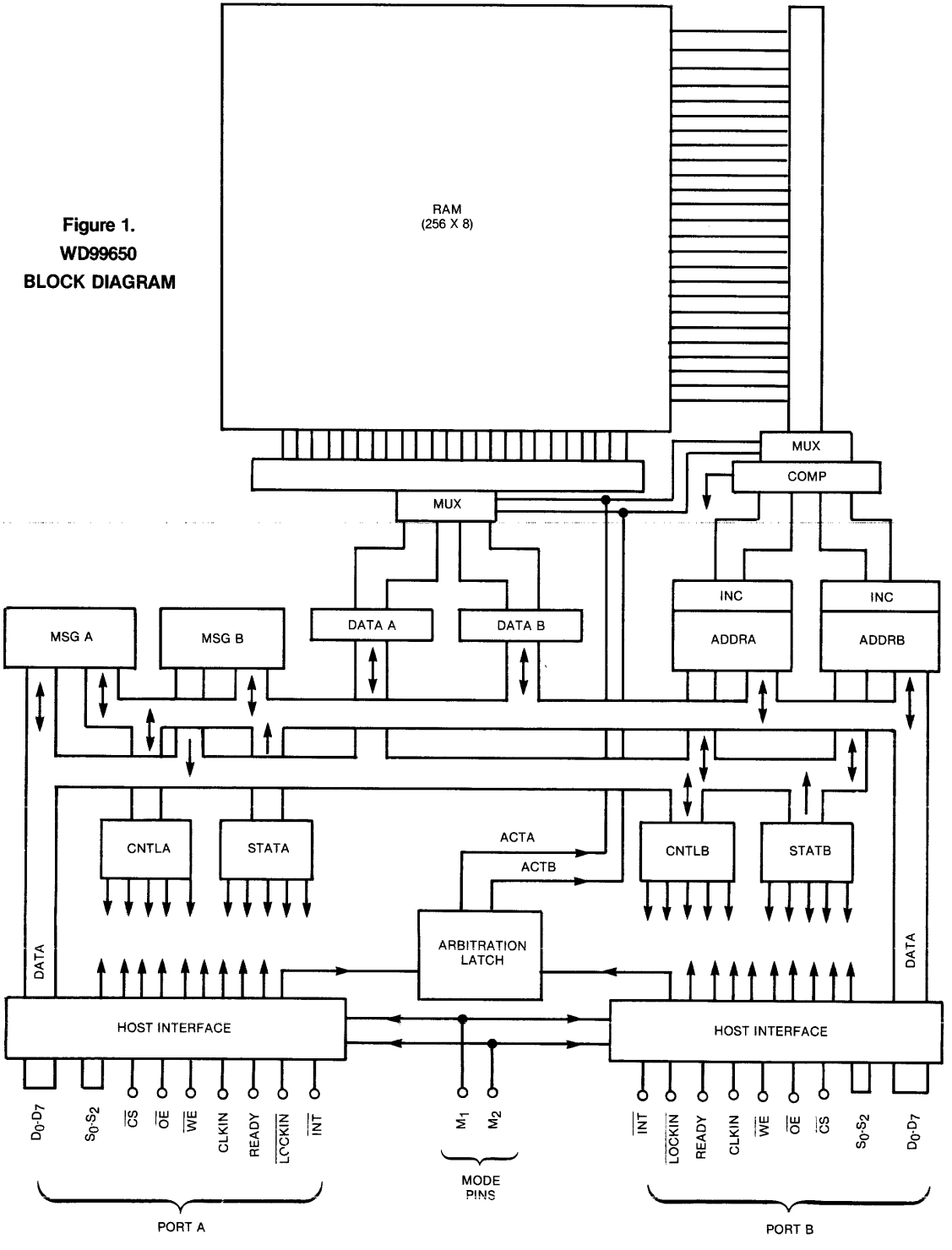


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Table 1. WD99650 REGISTER MAP

REGISTER SELECT LINES S_0, S_1, S_2	REGISTER FUNCTION	REGISTER SELECTED		READ/WRITE
		PORT A	PORT B	
000	DATA/INCREMENT	DATA A	DATA B	R/W
001	DATA	DATA A	DATA B	R/W
010	MESSAGE IN	MESSAGE B	MESSAGE A	R
011	MESSAGE OUT	MESSAGE A	MESSAGE B	R/W
100	CONTROL	CONTROL A	CONTROL B	R/W
101	LOCAL ADDRESS POINTER	ADDRESS A	ADDRESS B	R/W
110	STATUS	STATUS A	STATUS B	R
111	REMOTE ADDRESS POINTER	ADDRESS B	ADDRESS A	R/W

MESSAGE REGISTERS

Each port can read and write its own message register at the location designated as Message Out. In addition, it only reads that of the other port at the Message In Location. The message registers are implemented as two 8-bit registers, which can be written to at any time from their corresponding interface. During a write operation, the previous value of the register is held in a latch so that if a read operation occurs concurrently with the write, the previous value of the status register will be read. This means that the hosts may poll their remote status registers at any time without fear of reading an invalid code:

Interrupts are provided to support passing messages (see Status Registers).

CONTROL REGISTERS

Control registers can be written to and read by their respective hosts at any time. The bit assignment is shown in Figure 2.

IEN_1-IEN_5 Interrupt Enable Bits: When set to 1, these allow their respective interrupt status bits to set the INT status bit and pull low the INT line.

LEA Lockout On Equal Addresses Pointer: If this feature is set from either port, it is active for the entire device. When this feature is enabled and the address pointer registers become equal, the port corresponding to the last address pointer register to change will be locked out of the RAM. This will occur regardless of whether the change was due to incrementing or loading from either port. The lockout will persist as long as the above condition remains true.

SLOC Software Lockout Bit: This provides a software-accessible means of requesting that the remote port be locked out of the RAM.

All bits of the control register are cleared by the reset function of the mode pins, M_1 and M_2.

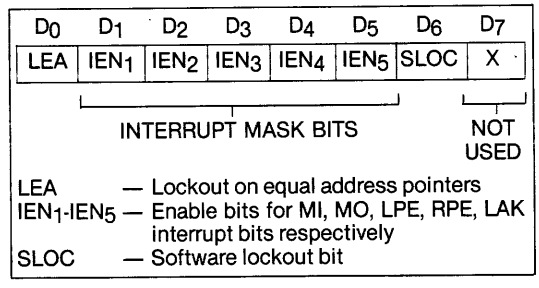


Figure 2.
WD99650 CONTROL REGISTER BIT ASSIGNMENT

STATUS REGISTERS

Each status register is read only and allows its corresponding host to inspect the status of various parameters on-chip. All may cause an interrupt if the appropriate interrupt enable bit is set to a 1. The bit assignment is shown in Figure 3.

INT Interrupt Asserted: An interrupt status bit has been set, and the INT line is pulled low.

MI Message In Interrupt: A byte should be read from the Message In register. It is set when the remote port loads its Message Out register and is cleared when the local port reads its Message In register. It is cleared by the reset function.

MO Message Out Interrupt: The local message register is available for use. It is cleared when a byte is written to the local Message Out register and set when the remote Message In register is read. It is set by the reset function.

LPE Local Pointer Equal to Remote Pointer: The address pointer registers are equal, and the local pointer was the last one to change, whether by incrementing or by loading from either port. It remains true as long as the condition persists.

RPE Remote Pointer Equal to Local Pointer: The address pointer registers are equal, and the remote address pointer was the last one to change, whether by incrementing or loading from either port. It remains true as long as the condition persists.

LAK Lockout Acknowledge: This is set following the assertion of SLOC by the local port when the lockout of the remote port from the RAM becomes effective. It is cleared when SLOC is cleared.

D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
INT	MI	MO	LPE	RPE	LAK	X	X
	INTERRUPT STATUS BITS					NOT USED	

INT — Interrupt occurred
MI — Message in
MO — Message out
LPE — Local address pointer equal to remote address pointer
RPE — Remote address pointer equal to local address pointer
LAK — Lockout acknowledge

Figure 3.
WD99650 STATUS REGISTER BIT ASSIGNMENT

HOST INTERFACES

The simplest read and write operations for the WD99650 are shown in Figure 4A & 4B. READY and CLKIN are not shown since the memory cycles here apply to all registers except the data register. They will apply to the data register only if READY is not used. As with the register map, the host interfaces are identical, both electrically and functionally.

The desired register is selected by putting the appropriate code (see Pin Description) on the register select lines (S_0-S_2) and by putting chip select ($\overline{CS}$) low. If a write operation is desired, a negative-going pulse is applied to the write enable pin ($\overline{WE}$), and valid data is set up on the data lines (D_0-D_7) sooner than the required setup time before the rising edge of the write enable. If a read operation is desired, the output enable ($\overline{OE}$) signal is set low, which brings the WD99650 data lines out of a high impedance state. The data that they display will only be valid after the appropriate access time has elapsed from the register being selected. The required setup times, access times, etc. are given in ARBITRATION AND SYNCHRONIZATION.

READY AND CLKIN

Although the WD99650 host interfaces can function without the READY and CLKIN signals, both signals are required if concurrent access to the RAM is desired by both host systems. Under these conditions, the selection of one interface or the other on to the RAM is done by the arbitration latch. The host interface logic is responsible for putting into a wait state the host which is unsuccessful in gaining access.

When a host system addresses the data register of the WD99650 (chip select low and the appropriate code on the register select lines), READY is immediately set low regardless of whether or not access is actually gained to the RAM. READY will then stay low, and the interface will remain in a wait state until any uncertainty in the arbitration latch has resolved itself and access has been clearly gained.

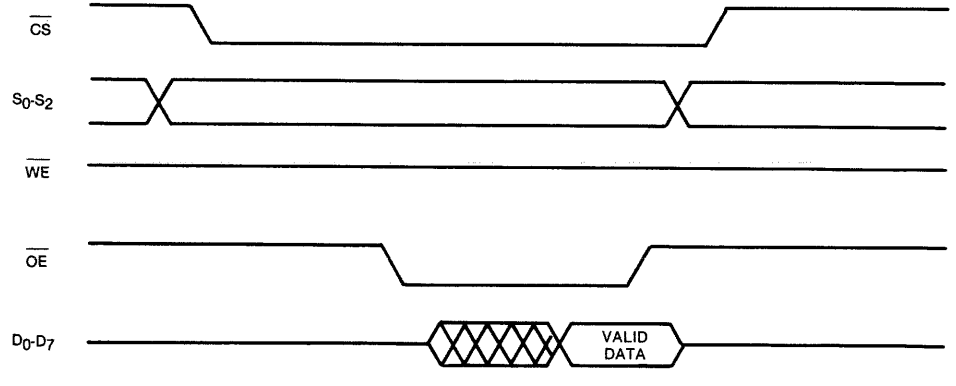


Figure 4A. READ OPERATIONS

Since the majority of systems will not accept an asynchronous READY signal, synchronization is provided on the WD99650. The falling edge of READY is generated by the CPU addressing its data register, so it is already synchronous. The rising edge, however, is not and must be synchronized to the system clock. CLKIN is provided for this purpose alone.

Each output of the arbitration latch is monitored by a threshold detector. which tests for a level in excess of the metastable level. ACTA or ACTB reaching this level indicates any conflict has resolved itself, and the corresponding port has gained access to the RAM. During the CLKIN high period, the output of the threshold detector is sampled as shown in Figure 5. When CLKIN is low, the feedback is applied to consolidate the sampled value so that any indeterminate sample will go to a valid 1 or 0 level. If a 1 is detected indicating that the memory cycle can proceed, then READY is set high on the next rising edge of CLKIN.

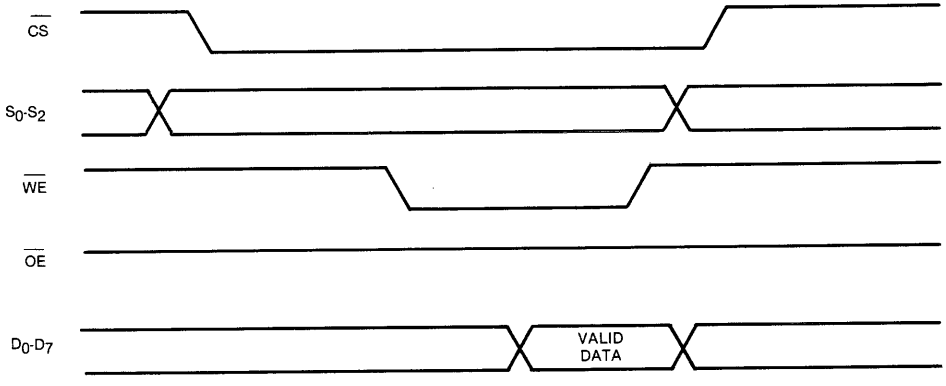


Figure 4B. WD99650 WRITE OPERATIONS

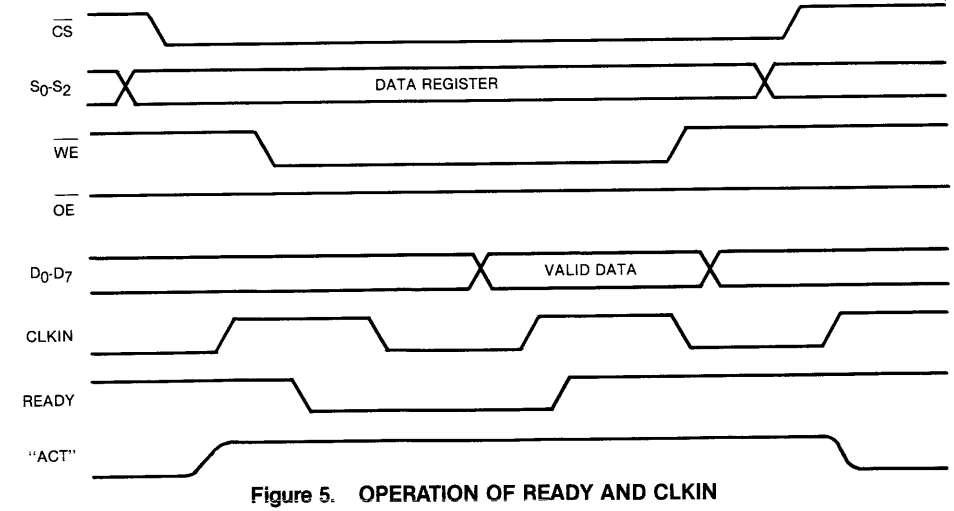
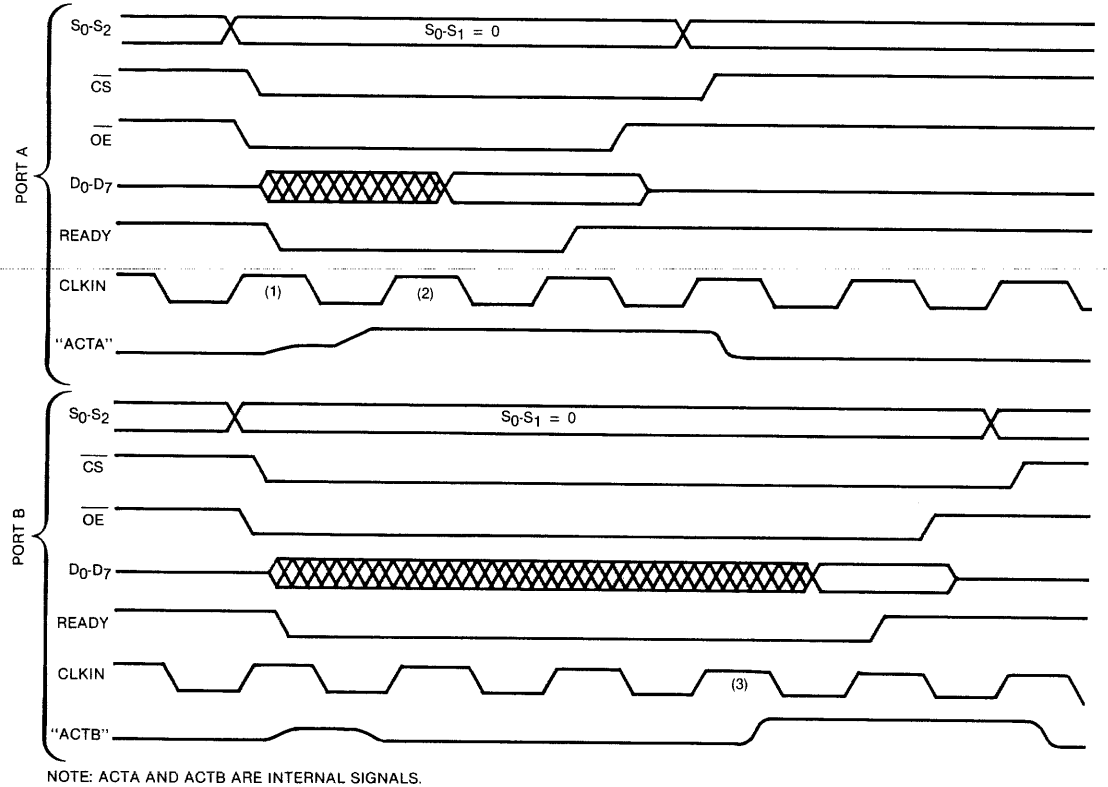


Figure 5. OPERATION OF READY AND CLKIN

Figure 6 shows the result of two read cycles beginning at the same time. When the data registers are addressed, the ACTA and ACTB bits both begin to rise. As they are both mutually exclusive, a metastable condition is reached. It is significantly later that a result is seen from this conflict when, in this case, port A gains access and port B does not. READY is taken low on both ports as soon as the data registers are addressed. At port A during the first subsequent CLKIN high period (1), ACTA is not seen as having a VALID high level. Therefore, it is the value sampled in the second CLKIN high period (2) that results in READY being set high on the next rising edge of CLKIN. Note that ACTA selects the data and local address pointer registers of port A on to the data and address lines of the RAM. It is not until after ACTA reaches a good 1 level that valid data is seen on the port A data lines. Port A then completes its memory cycle and ceases to address its data register. ACTA, therefore, goes low again, which allows ACTB to rise to a 1 level. This fact is detected in the CLKIN high period of port B (3), and READY goes high on the next rising edge. Up to this point, the data lines of port B have been displaying invalid data. This becomes valid after ACTB reaches a good 1 level. The memory cycle port B can then be completed.



NOTE: ACTA AND ACTB ARE INTERNAL SIGNALS.

Figure 6. SIMULTANEOUS READ CYCLES FROM BOTH PORTS

LOCKOUT CAPABILITY

Both ports have a lockout feature that can be asserted by either one of two means: (1) by putting a low level on the $\overline{LOCKIN}$ input of the host interface, or (2) by writing a 1 to the SLOC bit of the control register. If a lockout is asserted by the local port, then the ACT bit of the remote port is held low. Thus if the remote port addresses its data register, it will not get access to the RAM. If CLKIN and READY are used on the remote port, it will enter a wait state until the lockout is removed.

The assertion of a lockout will not guarantee immediate exclusive use of the RAM. A lockout asserted by the local port will only become effective after any memory operation to the RAM by the remote port has been completed. It will also not be effective until any lockout asserted by the remote port has been cleared. Lockouts, therefore, are mutually exclusive in a similar way to ACTA and ACTB, and concurrent lockout requests from both ports are assigned on a first-come, first-serve basis.

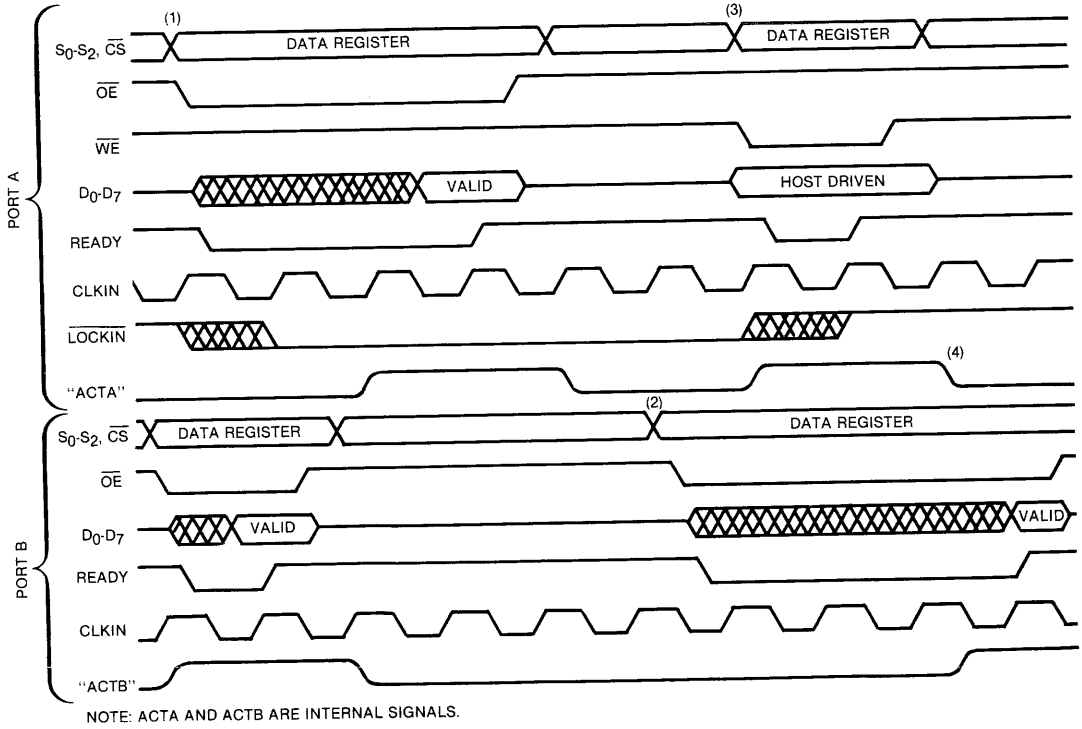
Figure 7 shows an example of the lockout facility being used to implement an indivisible read-modify-write operation. Port A performs the read and write operations with a lockout asserted between them by means of the LOCKIN input. At the time when port A tries to do a read from the RAM (1), there is already a read cycle in progress on port B. Port A, therefore, enters a wait state until this operation is complete even though the LOCKIN input is asserted. When the read cycle at port B is complete, the memory operation at port A can proceed and, in addition, the lockout of port B becomes effective. Consequently, when the next memory operation is initiated to port B (2), it enters a wait state even though there is no activity on port A. Port A then enters a write cycle (3), during which the LOCKIN is removed. When the write cycle ends and ACTA goes low (4), ACTB can rise in the absence of the lockout and the memory operation can also be completed here. Therefore, the read and write operations at port A cannot be interfered with from port B. LOCKIN would be derived from a multiprocessor interlock-type signal in host system B.

In a system where the user does not wish to use the READY and CLKIN signals on a particular port, the SLOC bit can be used to guarantee that access is gained to the RAM. The LAK interrupt status bit will be set in response to SLOC as soon as the lockout becomes effective. Thus LAK will not be set until any current memory cycle to the RAM from the remote port has been completed and any lockout that the remote port may have asserted has been cleared. After this, the local port has exclusive use of the RAM until it clears SLOC.

ADDRESS POINTER EQUAL INTERRUPTS AND LOCKOUT

If it is desired to move data blocks of greater than 256 bytes between systems, the WD99650 can be used to implement a circular buffer to absorb any data transfer rate mismatch between systems. Consider the case of system A (connected to port A) sending a block of data to system B. Both systems implement the MPIF READY signal.

To begin the transfer, the address pointer registers of both ports are set the same. This is done by either host system if the address pointer of port B is set up last. This generates an RPE interrupt to system A and an LPE interrupt to system B, these serving as buffer empty interrupts. Normally, system B should then avoid reading the RAM until the LPE interrupt has gone. However, if the LEA feature is enabled, system B can begin its first read. It will enter a wait state until the first byte is written into the buffer. When system A starts loading data via its data/increment register, the equality of pointers is removed, and the receiving



NOTE: ACTA AND ACTB ARE INTERNAL SIGNALS.

Figure 7. TYPICAL READ-MODIFY-WRITE OPERATION USING LOCKIN

system can sequentially read the data via its data/increment register. If the reading pointer succeeds in catching up with the writing pointer, then system A will again receive an RPE and system B an LPE and a lockout (assuming LEA is set) indicating that the buffer is empty.

If the sending system succeeds in getting 256 bytes ahead of the receiving system, then the address pointers again become equal. This time, system A gets the lockout and an LPE interrupt, and system B gets an RPE interrupt. This corresponds to a buffer full interrupt, and the sending system will be prevented from writing more data until there is room for it.

Another possible method of buffering large data streams is as follows: If the sending interface in the above example fills the buffer and receives an LPE interrupt, then it may subtract a certain number from that in its local address pointer and reload it with the result. It will be interrupted when there is this certain number of bytes left in the buffer and may return the original value to the address pointer and refill the buffer. However, the sending system should return the original value to its local address pointer if it enters a condition where it is unable to respond to an interrupt before the remaining bytes in the buffer are read.

An equivalent procedure can be undertaken by the receiving host system. This time, a certain number is added to the pointer register and an RPE interrupt received when there is that number of bytes in the buffer.

MODE PINS

The mode pins, M_1 and M_2, are used to reset the WD99650 and to enable several WD99650s to be used in parallel on memory buses of greater than 8 bits. There are four modes encoded on these pins: reset ($M_1 = M_2 = 0$), standalone ($M_1 = M_2 = 1$), master ($M_1 = 0$, $M_2 = 1$), and slave ($M_1 = 1$, $M_2 = 0$). Schmitt triggers are provided on both inputs to permit the use of a resistor and capacitor arrangement to implement reset.

Reset ($M_1 = M_2 = 0$)

The reset function establishes the following conditions on-chip:

1. All bits of the control register cleared
2. The MI interrupt status bit cleared
3. The MO interrupt status bit set
4. The data lines (D_0-D_7) of the host interfaces held in a high impedance state
5. The READY output of each port held in a high impedance state.

The other three combinations of the mode pins are operating modes.

Standalone Mode ($M_1 = M_2 = 1$)

The standalone mode is the operating mode of a single WD99650. To implement reset with this mode of operation, both M_1 and M_2 should be connected to an active-low system $\overline{\text{RESET}}$ signal.

Master ($M_1 = 0$, $M_2 = 1$) and Slave ($M_1 = 1$, $M_2 = 0$) Modes

The master and slave modes are included to avoid the possibility of problems occurring in multiple WD99650 arrangements. During simultaneous attempts at getting access to the RAM by both ports, it is possible for the arbitration latches of different devices in standalone mode to fall in opposite directions with consequent system malfunction. Master and slave modes allow the arbitration latch in only one WD99650 to decide which port should have access. This decision is then passed on to the remainder. Figure 8 shows an example of a multiple WD99650 system.

To implement the reset function on the master device, M_2 should be connected to the system $\overline{\text{RESET}}$ signal, and M_1 should be grounded. In normal operation, the timing of the READY line of each port is changed to provide an unclocked, active-high indication of when that port has gained access to the RAM. A CLKIN input is, therefore, not required by the master device.

On the slave devices, M_1 is connected to the system $\overline{\text{RESET}}$ line, and M_2 is grounded. In this mode, the $\overline{\text{LOCKIN}}$ signals of each port become enable inputs, which are connected directly to the modified READY outputs of the corresponding port of the master device. The slave has no arbitration and responds to a high level on the READY output of the master by granting access to the appropriate port immediately. At this time, it also begins the procedure of releasing its own READY line which is synchronized in the same way as on the standalone device. Hence, a CLKIN must be supplied to the slave devices. In dual WD99650 arrangements, the READY outputs of the slave may be taken directly to the READY input of the host systems. With more than one slave, the READY outputs of each port should be ANDed together to ensure that all WD99650s give access to the port before READY is released.

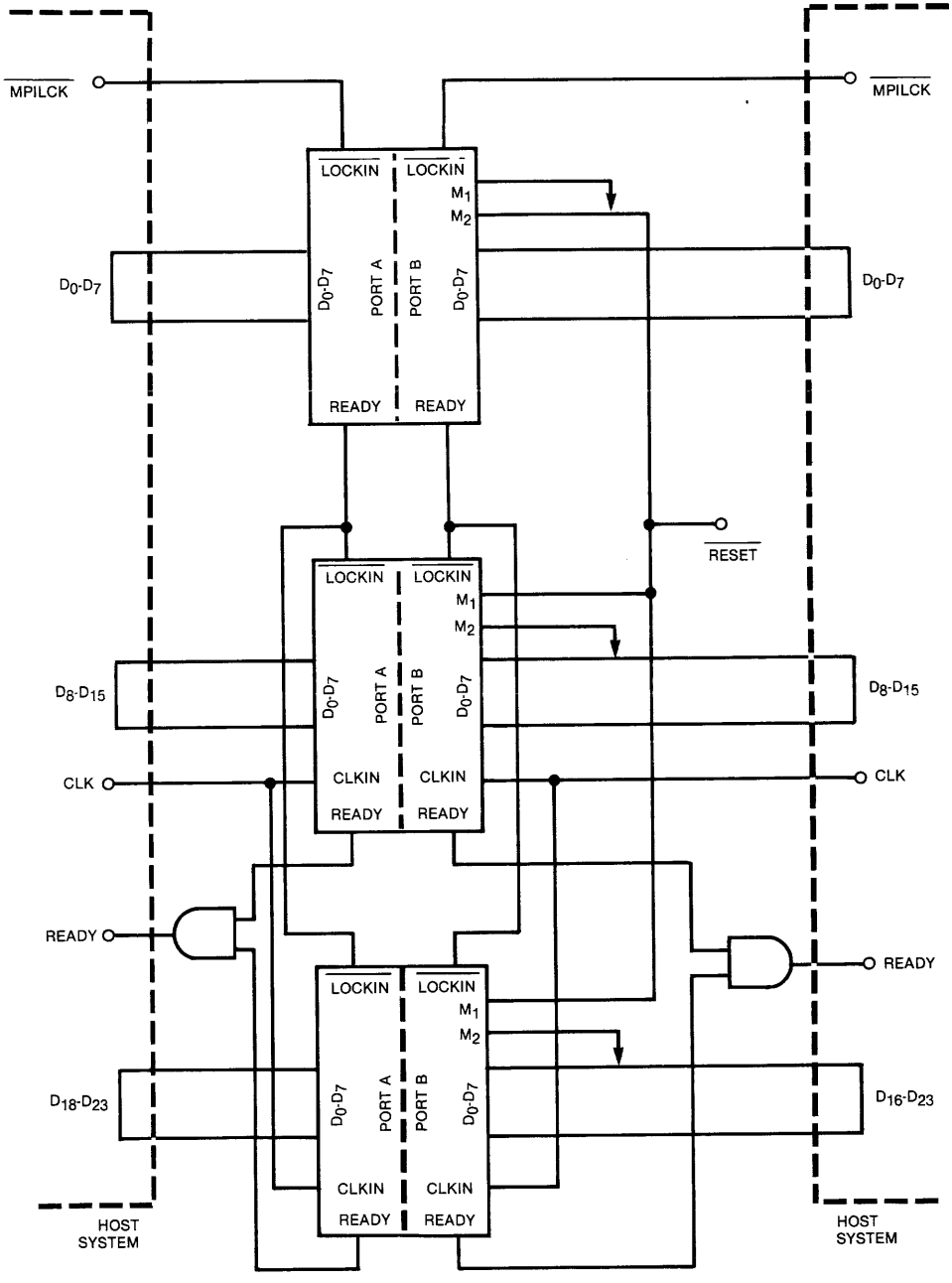


Figure 8. MULTIPLE WD99650 CONFIGURATION

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS OVER OPERATING FREE-AIR TEMPERATURE RANGE (UNLESS OTHERWISE NOTED)*

Supply voltage, V_{CC} (see Note 1) 7V
Input voltage . . . . . −0.3 to 20V
Off-state output voltage . . . . . −0.3 to 7V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:
Voltage values are with respect to network ground terminal, V_{SS}.

RECOMMENDED OPERATING CONDITIONS

	MIN.	NOM.	MAX.	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	V
Supply voltage, V_{SS}		0		V
High-level input voltage (All inputs), V_{IH}	2			V
Low-level input voltage (All inputs), V_{IL}			0.8	V
High-level output current, I_{OH} (All outputs except $\overline{INT}$)			100	μA
Low-level output current, I_{OL}				
All except $\overline{INT}$			2	mA
$\overline{INT}$ output only			2.5	mA
Operating free-air temperature, T_A	0		70	°C

ELECTRICAL CHARACTERISTICS OVER RECOMMENDED FREE-AIR TEMPERATURE RANGE

	PARAMETER	TEST CONDITIONS†	MIN.	TYP.‡	MAX.	UNIT
V_{OH}	High-level output voltage	V_{CC} = min, I_{OL} = max	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = min, I_{OL} = max			0.4	V
I_O	Off-state (high-impedance state) output current	V_{CC} = max, V_O = 2.4 V			20	μA
		V_{CC} = max, V_O = 0.4 V			−20	μA
I_I	Input current	V_I = V_{SS} to V_{CC}			±50	μA
I_{OS}	Short-circuit output current§	V_{CC} = max				μA
I_{OC}	Supply current	V_{CC} = max				
C_i	Input capacitance (except data bus)	f = 1 MHz, all other pins at 0 V		15		pF
C_{DB}	Data bus capacitance			25		pF
C_o	Output capacitance (except data bus)			10		pF

† For conditions shown as MIN. or MAX., use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

TIMING REQUIREMENTS AND CHARACTERISTICS

	PARAMETER	CONDITION	SEE NOTE	SEE FIGURE	MIN.	TYP.	MAX.	UNIT
t_{SU1}	Register select setup time for write	Data register		9	205			ns
		$S_0 = S_1 = 0$ Otherwise		9	150			ns
t_{SU2}	Chip select setup time for write	Data register		9	195			ns
		$S_0 = S_1 = 0$ Otherwise		9	140			ns
t_{SU3}	Data setup time for write	Data register		9	150			ns
		$S_0 = S_1 = 0$ Otherwise		9	50			ns
t_{WL2}	Write enable low pulse width	Data register		9	200			ns
		$S_0 = S_1 = 0$ Otherwise		9	70			ns
t_{H1}	Data hold time for write			9	0			ns
t_{H2}	Chip select hold time for write			9	0			ns
t_{H3}	Register select hold time for write			9	0			ns
t_{H4}	Hold time of write enable after CLKIN rising edge during concurrent RAM accesses	Data register	7	12	140			ns
t_{AC1}	Access time from register select for read	Data register	1, 2	10			185	ns
		$S_0 = S_1 = 0$ Otherwise	1	10		85		ns
t_{AC2}	Access time from chip enable for read	Data register	1, 2	10			175	ns
		Otherwise	1	10		75		ns
t_{AC3}	Access time from output enable for read	Data register	1, 2	10			100	ns
		$S_0 = S_1 = 0$ Otherwise	1	10		40		ns
t_{P1}	Chip select to data bus Hi-Z		1	10		40		ns
t_{P2}	Output enable to data bus Hi-Z		1	10			30	ns
t_{AC4}	Access time from CLKIN low during concurrent RAM accesses	Data register	1, 7	12			120	ns
		Data register $C_L = 25$ pF	1, 7	12			100	ns
t_{H5}	Chip select hold time after valid data	Data register	3	10			2	µs
t_{H6}	Output enable hold time after valid data	Data register	3	10			2	µs
t_{P3}	Chip select to ready low	Data register	1	11		40		ns
t_{P4}	Register select to ready low	Data register	1	11		50		ns
t_{P5}	CLKIN to ready high	Data register	1	11		40		ns
		Data register $C_L = 25$ pF	1	11			20	ns
t_{SU4}	Chip select setup time to CLKIN	Data register	4	11	55			ns

TIMING REQUIREMENTS AND CHARACTERISTICS (Concluded)

	PARAMETER	CONDITION	SEE NOTE	SEE FIGURE	MIN.	TYP.	MAX.	UNIT
t_{SU5}	Register select setup to CLKIN	Data register	4	11	60			ns
t_{SU6}	$\overline{\text{LOCKIN}}$ setup to end of access	Data register	5	11	100			ns
t_{WL1}	CLKIN low pulse width			11	60			ns
t_{WH1}	CLKIN high pulse width			11	45			ns
t_{P6}, t_{P7}	End of memory cycle to interrupt		1, 6	13			200	ns

NOTES:

1. Figure 14 shows the load circuit used to measure the timing characteristics of output and I/O pins. A value of C_L = 100 pF is used except where otherwise stated. R_1 is only included for open drain outputs.
2. These times only apply when the port in question gets immediate access to the RAM. Otherwise, the access time is determined by t_{AC4}.
3. Only one of the time t_{H5} or t_{H6} need be satisfied. These specify the maximum length of a RAM read operation after access has been gained.
4. These setup times need to be met if READY is to be set high on the next rising edge of CLKIN. If this is not the case, then READY will not be released until one CLKIN cycle later.
5. This setup time is required if $\overline{\text{LOCKIN}}$ is to be effective immediately after the termination of the memory access to the RAM. The memory access may be terminated either by $\overline{\text{CS}}$ going high or the address lines changing.
6. This is the delay of the interrupt line from the termination of the memory cycle that causes it. The cycle is terminated when $\overline{\text{CS}}$ goes high or when either $\overline{\text{OE}}$ or $\overline{\text{WE}}$ goes high.
7. These parameters describe the access time and required $\overline{\text{WE}}$ hold times when access to the RAM is not immediately achieved and the host system enters more than one wait state. The parameters are measured from the falling edge of CLKIN on which the corresponding ACT bit is first sampled as being high. This sampled value indicates that access to the RAM has started and results in READY are being released on the next rising edge of CLKIN.

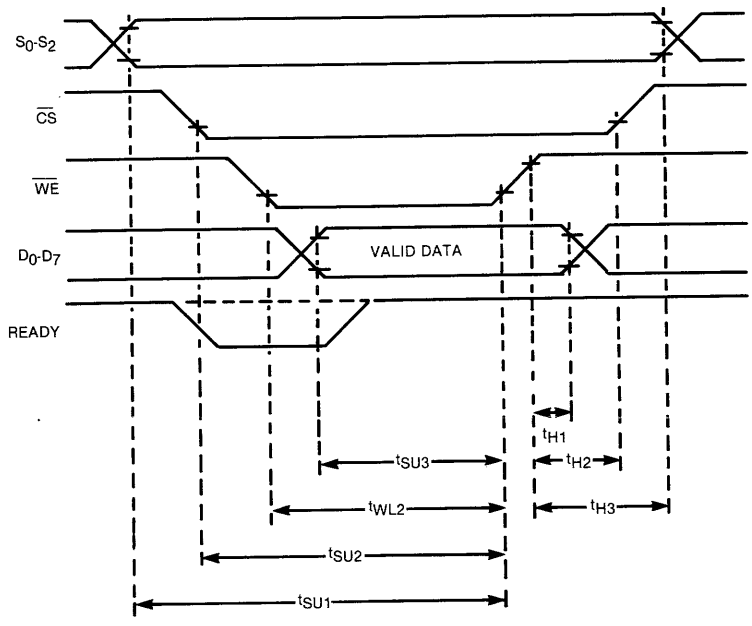


Figure 9. WRITE CYCLE TIMING CHARACTERISTICS

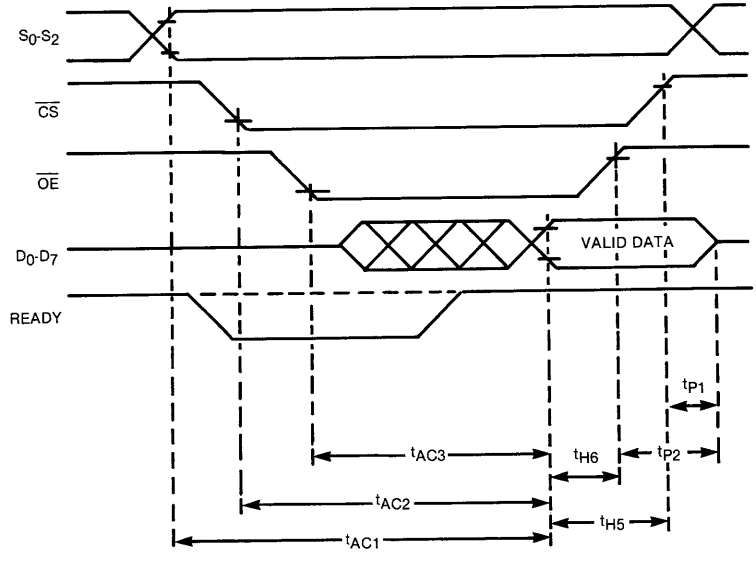


Figure 10. READ CYCLE TIMING CHARACTERISTICS

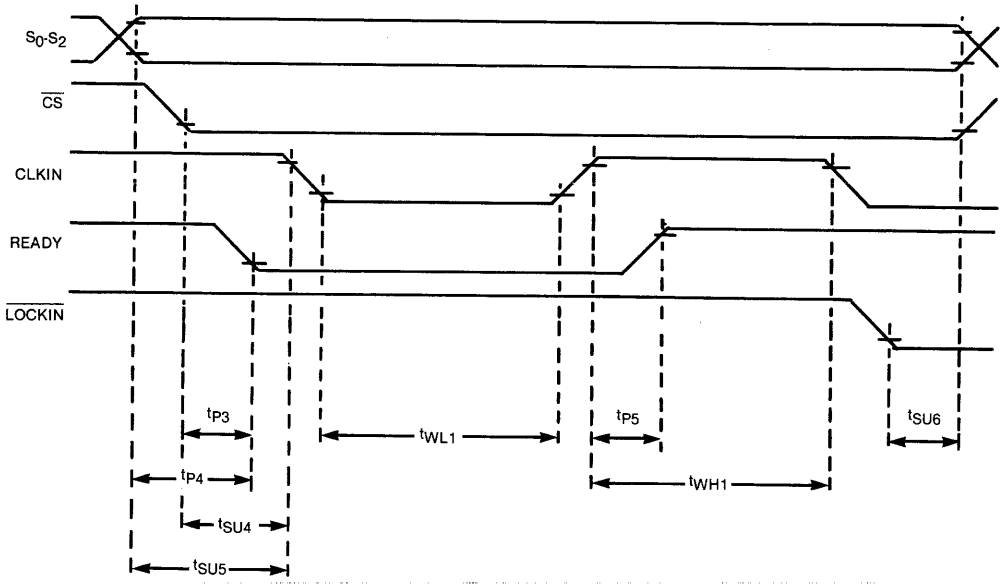


Figure 11. READY, CLKIN AND $\overline{\text{LOCKIN}}$ TIMING CHARACTERISTICS

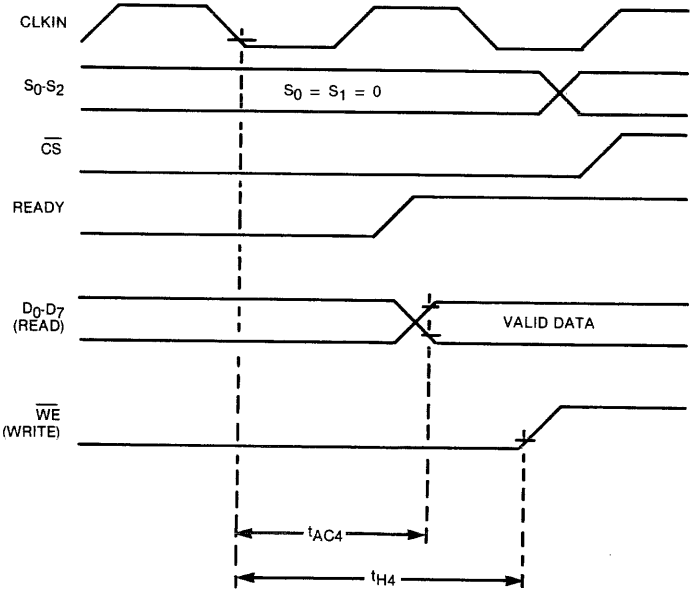


Figure 12. DATA WRITE CHARACTERISTICS

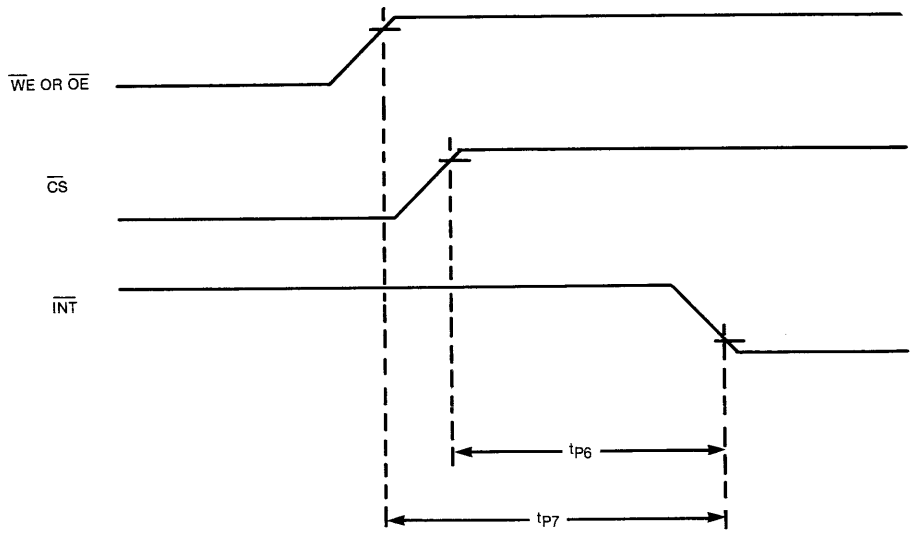


Figure 13. INTERRUPT TIMING CHARACTERISTICS

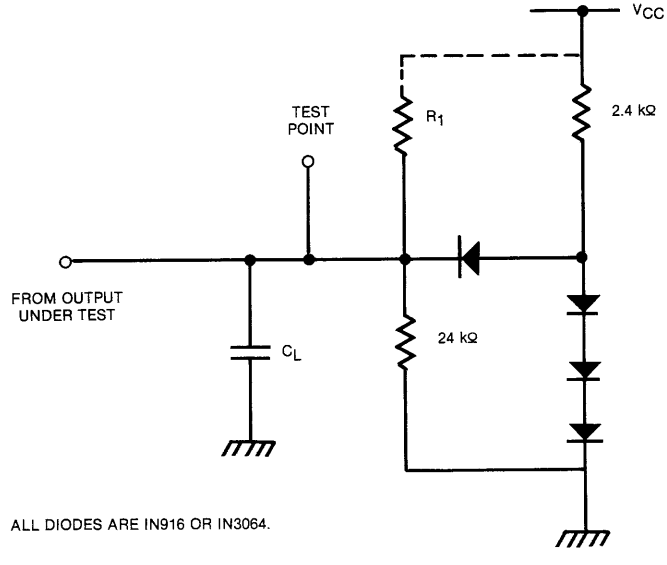


Figure 14. TEST LOAD CIRCUIT

See page 481 for ordering information.

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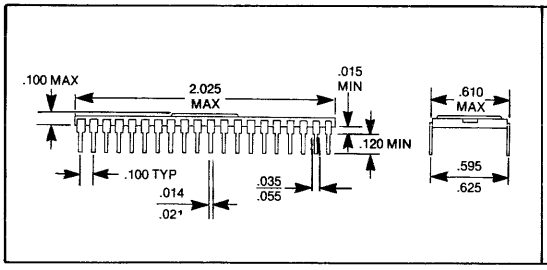
ORDERING INFORMATION

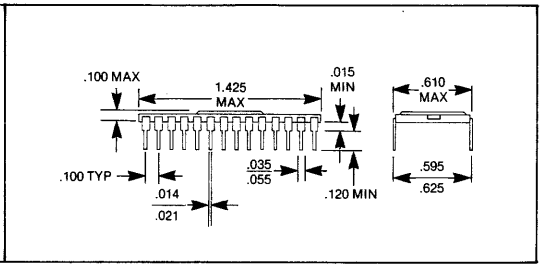
The following listing indicates the available packages for each product. The letter designation refers to the package diagrams, beginning on page 531.

Product	Plastic	Ceramic	CER-DIP
WD1010-00/01/05/08	PL	AL	CL
WD1011	P		C
WD1012	P		C
WD1014-00, 01	PL	AL	CL
WD1015-00, 01, 02			CL
WD1050			
WD1100-01	PE		CE
WD1100-02	PE		CE
WD1100-03	PE		CE
WD1100-04	PE		CE
WD1100-05	PE		CE
WD1100-06	PE		CE
WD1100-07	PE		CE
WD1100-09	PE		CE
WD1100-10	PE		CE
WD1100-11	PL		CL
WD1100-12	PE		CE
WD1100-13	PE		CE
WD1100-14	PE		CE
WD1691	V	U	CE
FD176X-02	PL	AL	CL
WD1770/72/73	PH	AH	CH
WD1771-01	PL	AL	CL
FD1781	PL	AL	
FD179X-02	PL	AL	CL
DM1883-A/B	PL	AL	CL
WD2010			
WD2143-03	M	L	CD
WD279X-02	PL	AL	CL
WD8206		DT	
WD8207		DT	
WD9216-00, 01	PA		
WD99650	PL	AL	CL

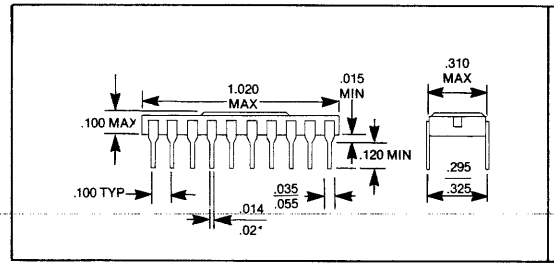
Package Diagrams



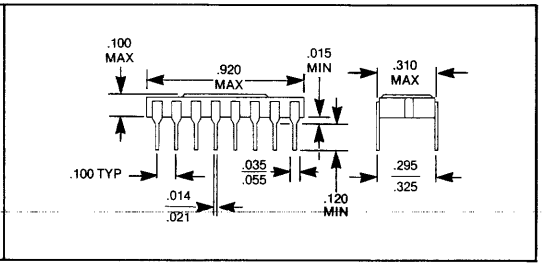
40 LEAD CERAMIC "A" or "AL"



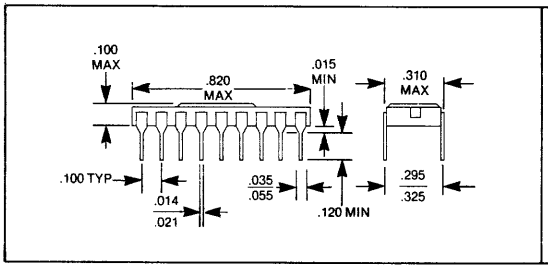
28 LEAD CERAMIC "E" or "AH"



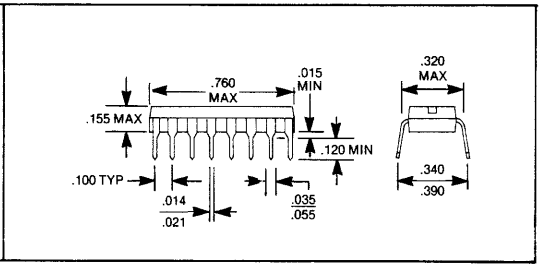
20 LEAD CERAMIC "U" or "AE"



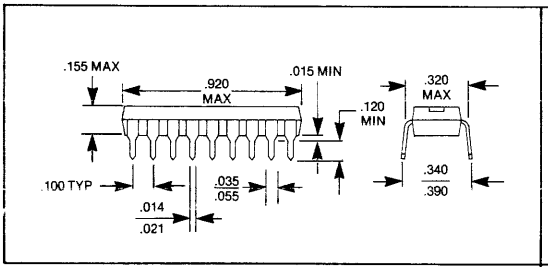
18 LEAD CERAMIC "L" or "AD"



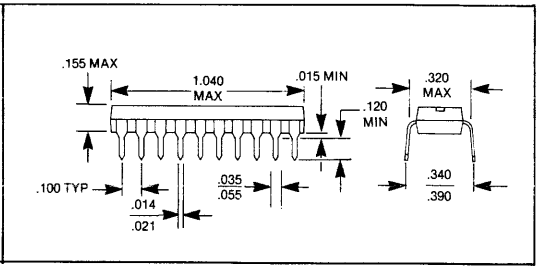
16 LEAD CERAMIC "J" or "AC"



16 LEAD PLASTIC "K" or "PC"

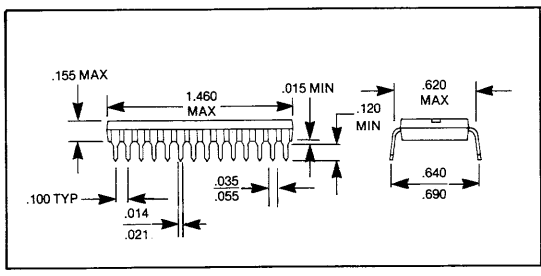


18 LEAD PLASTIC "M" or "PD"

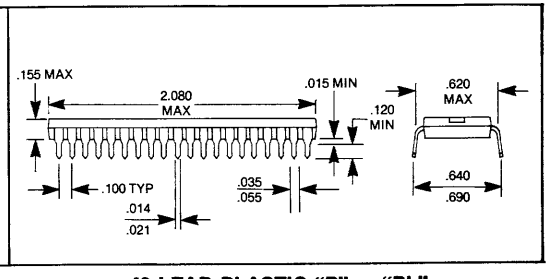


20 LEAD PLASTIC "V" or "PE"

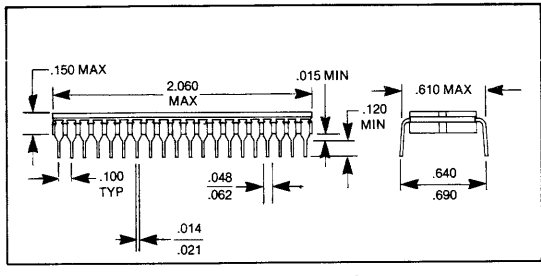
Package Diagrams



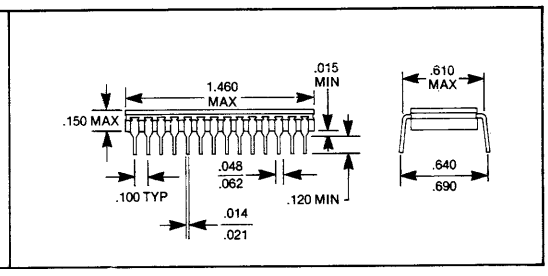
28 LEAD PLASTIC "R" or "PH"



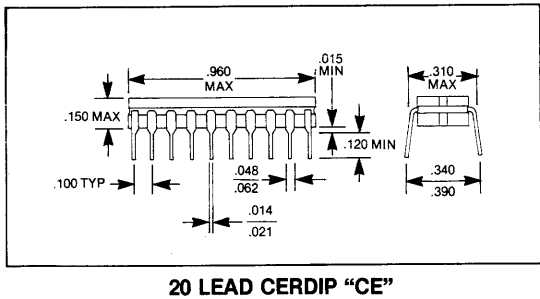
40 LEAD PLASTIC "P" or "PL"



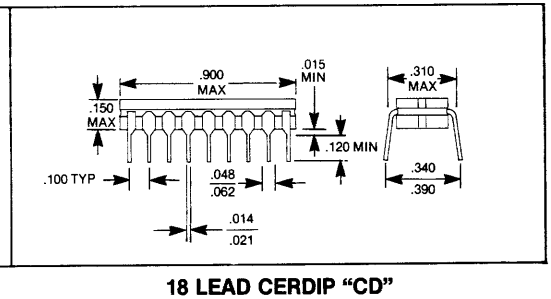
40 LEAD CERDIP "CL"



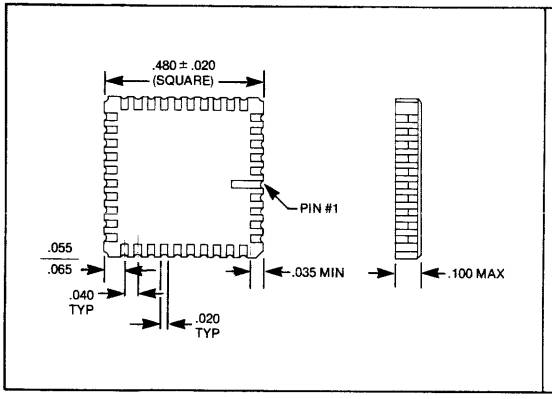
28 LEAD CERDIP "CH"



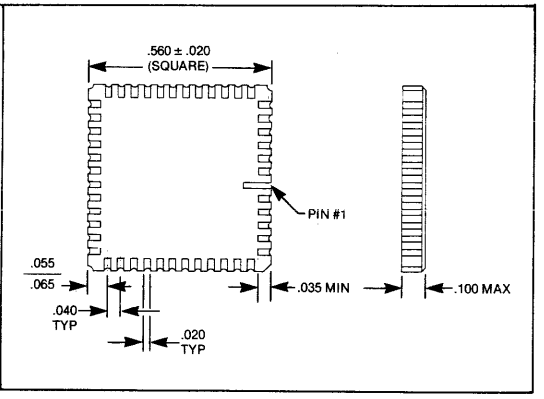
20 LEAD CERDIP "CE"



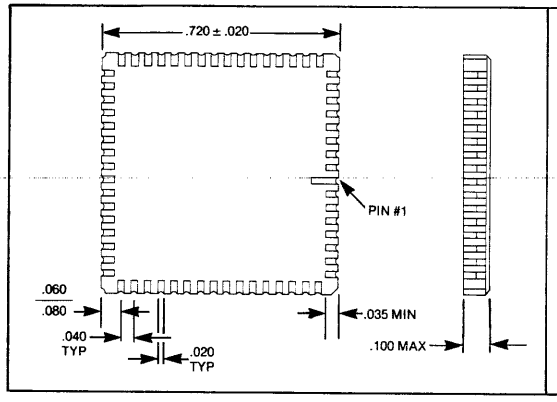
18 LEAD CERDIP "CD"



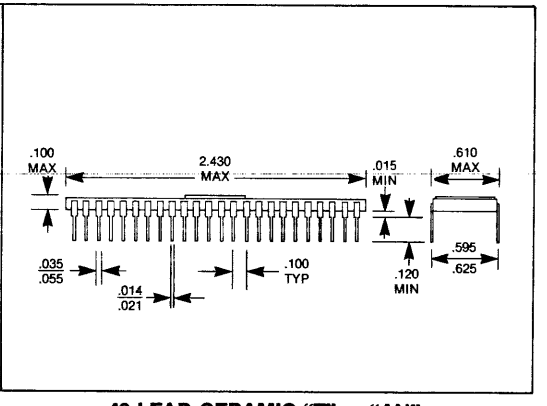
40 LEAD CERAMIC CHIP CARRIER "DL"



48 LEAD CERAMIC CHIP CARRIER "DN"



64 LEAD CERAMIC CHIP CARRIER "DS"



48 LEAD CERAMIC "T" or "AN"

Pin Compatibility Guide

	INTEL	NATIONAL	SIEMENS	TI
WD1010	82062			
FD1771-01		INS1771-1		
FD179X			SAB179X	
WD279X			SAB279X	
WD8206	8206			
WD8207	8207			
WD99650				TMS99650

Component Products
Terms and Conditions

1. **ACCEPTANCE:** Unless otherwise provided, it is agreed that sales are made on the terms, conditions and warranties contained herein and that to the extent of any conflict, the same take precedence over any terms or conditions which may appear on Buyer's order form. Seller shall not be bound by Buyer's terms and conditions unless expressly agreed to in writing. In the absence of written acceptance of these terms, acceptance of or payment for any of the articles covered hereby shall constitute an acceptance of these terms and conditions.

2. **F.O.B. POINT:** All sales are made F.O.B. point of shipment. Seller's title passes to Buyer and Seller's liability as to delivery ceases upon making delivery of articles purchased hereunder to carrier at shipping point in good condition; the carrier acting as Buyer's agent. All claims for damages must be filed with the carrier. Unless specific instructions from Buyer specify which method of shipment is to be used, the Seller will exercise his own discretion.

3. **DELIVERY:** Shipping dates are approximate only. Seller shall not be liable for any loss or expense (consequential or otherwise) incurred by Buyer if Seller fails to meet the specified delivery schedule because of unavoidable production or other delays. Seller may deliver the articles in installments, Seller shall not be liable for any delay in delivery or for non-delivery, in whole or in part, caused by the occurrence of any contingency beyond the control either of Seller or Seller's suppliers, including, by way of illustration but not limitation, war (whether an actual declaration thereof is made or not), sabotage, insurrection, riot or other act of civil disobedience, act of a public enemy, failure or delay in transportation, act of any government or any agency or subdivision thereof, judicial action, labor dispute, accident, fire, explosion, flood, storm or other act of God, shortage of labor, fuel, raw material or machinery or technical failure where Seller has exercised ordinary care in the prevention thereof. If any contingency occurs, Seller may allocate production and deliveries among Seller's customers.

4. **TERMS AND METHODS OF PAYMENT:** Where seller has extended credit to Buyer, terms of payment shall be net thirty (30) days from date of invoice. The amount of credit or terms of payment may be changed or credit withdrawn by Seller at any time. If the articles are delivered in installments, Buyer shall pay for each installment in accordance with the terms hereof. Payment shall be made for the articles without regard to whether Buyer has made or may make any inspection of the articles. If shipments are delayed by Buyer, payments are due from the date when Seller is prepared to make shipments. Articles held for Buyer are at Buyer's sole risk and expense.

5. **TAXES:** All prices are exclusive of all federal, state and local excise, sales, use, and similar taxes. Such taxes; when applicable to this sale or to the articles sold, will appear as separate additional items on the invoice unless Seller receives a properly executed exemption certificate from Buyer prior to shipment.

6. **PATENTS:** The Buyer shall hold the Seller harmless against any expense or loss resulting from infringement of patents or trademarks arising from compliance with Buyer's designs or specifications or instructions. The sale of products by the Seller does not convey any license, by implication, estoppel, or otherwise, under patent claims covering combinations of said products with other devices or elements. Except as otherwise provided in the preceding paragraph, the Seller shall defend any suit or proceeding brought against the Buyer so far as based on a claim that any product, or any part thereof, furnished under this contract constitutes an infringement of any patent of the United States, if notified promptly in writing and given authority, information and assistance (at the Seller's expense) for the defense of same, and the Seller shall pay all damages and costs awarded therein against the Buyer. In case said product, or any part thereof, is in such suit held to constitute infringement and the use of said product or part is enjoined, the Seller, shall at its own expense, either procure for the Buyer the right to continue using said product or part, or replace same with non-infringing product, or modify it so it becomes non-infringing, or remove said product and refund the purchase price and the transportation and installation costs thereof. The foregoing states the entire liability of the Seller for patent infringement by the said products of any part thereof.

7. **ASSIGNMENT:** The Buyer shall not assign his order or any interest therein or any rights thereunder without the prior written consent of Seller.

8. **WARRANTY:** Seller warrants articles of its manufacture against defective materials or workmanship for a period of one year from date on which Seller delivers said articles. The liability of Seller under this warranty is limited at Seller's option, solely to repair, replacement with equivalent articles, or an appropriate credit adjustment not to exceed the original sales price of articles returned to the Seller provided that (a) Seller is promptly notified in writing by Buyer upon discovery of defects, (b) the defective article is returned to Seller, transportation charges prepaid by Buyer, and (c) Seller's examination of such article disclosed to its satisfaction that defects were not caused by negligence, misuse, improper installation, accident, or unauthorized repair or alteration by the Buyer. In the case of equipment articles, this warranty does not include mechanical parts failing from normal usage nor does it cover limited life electrical components which deteriorate with age. In the case of accessories, not manufactured by Seller, but which are furnished with the Seller's equipment, Seller's liability is limited to whatever warranty is extended by the manufacturers thereof and transferable to the Buyer. This Warranty is expressed in lieu of all other Warranties, expressed or implied, including the implied Warranty of fitness for a particlar purpose, and of all other obligations or liabilities on the Seller's part, and it neither assumes nor authorizes any other person to assume for the Seller any other liabilities. This Warranty should not be confused with or construed to imply free preventative or remedial maintenance, calibration or other service required for normal operation of the equipment articles. These Warranty provisions do not extend the original Warranty period of any article which has either been repaired or replaced by Seller. In no event will Seller be liable for any incidental or consequential damages.

9. **TERMINATION:** Buyer may terminate this contract in whole or from time to time in part upon 60 days written notice to Seller. In such event Buyer shall be liable for termination charges which shall include a price adjustment based on the quantity of articles actually delivered, and all costs, direct and indirect, incurred and committed for this contract together with a reasonable allowance for pro-rated expenses and profits. Any termination or back off in scheduling will not be allowed on shipments scheduled for the month in which the request is made and for the month following.

10. **GOVERNMENT CONTRACTS:** If the articles to be furnished under this contract are to be used in the performance of a Government contract or subcontract and a Government contract number shall appear on Buyer's purchase order, those clauses of the applicable Government procurement regulation which are mandatorily required by Federal Statute to be included in Government subcontracts shall be incorporated herein by reference.

11. **ORIGIN OF ARTICLES:** Seller engages in off-shore production, assembly and/or processing and makes no warranty or representation, expressed or implied, that the articles delivered hereunder are United States articles or of U.S. origin for the purpose of any statute, law, rule, regulation or case thereunder. If Buyer ships the articles hereunder out of the U.S. for assembly, then at Buyer's request in writing, Seller shall provide information applicable to identification of any articles not of U.S. origin.

Corita Kent, the cover artist, is an American whose work presents an optimistic, yet philosophical view of the world we live in. A former Catholic nun and teacher, Corita now devotes her life and energies to her artwork and the "human needs she feels transcend national and religious barriers." A true "citizen of the world," Corita's philosophy positions her "on the positive side of hope." Her depiction of the Western Digital mission . . . "Making the leading edge work for you" . . . dramatizes the spectrum of solutions we provide our customers.

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