WD90C00

Enhanced VGA Controller

FEATURES:

- Provides single Chip Video Graphics Solution for IBM† PC† / XT / AT† and Personal System/2† compatible systems
- 100% hardware compatible with IBM's VGA card in all modes
- 100% IBM VGA and EGA hardware compatible
- 100% CGA, MDA, Hercules Graphics, AT&T Model 6300 compatible
- Integrated bus interface for PC / XT / AT, Micro Channel†
- 800 x 600 x 16 colors, 640 x 400 x 256 colors
- 640 x 480 x 256 colors (512K DRAM)
- 1024 X 768 X 16 colors interlaced graphics mode support - 8514/A monitor compatible
- High performance FIFO memory architecture
- 132 column text modes, with 25, 43, or 50 rows
- Includes 8 or 16 bit wide CPU data bus
- Support for external Color Lookup Table (Palette Chip) with 256K available colors
- Pin for pin compatible with PVGA1A (AT bus mode)
- Hidden registers support
- Enhanced virtual VGA support
- Up to 45MHz maximum video clock rate
- 1.25 Micron CMOS VLSI technology
- 100 pin Plastic Leadless Chip Carrier (PLCC) or Plastic Flat Pack (PFP) JEDEC package
- Minimizes circuit board space requirements and lowers system cost

DESCRIPTION:

The Paradise WD90C00 is a 1.25 micron, 15,000 gate CMOS LSI device designed to implement the IBM Personal System/2† standard video modes along with all of the popular modes used in the IBM PC† family. In comparision with Paradise Video Graphics Array (PVGA1A), the WD90C00 is designed to offer more improvements for wider range of applications. These enhancements include additional Paradise registers for EGA register level compatibility for PS/2 and TTL monitors, interlaced graphics support, cost reduced Micro Channel interface, and better video control for higher performance.

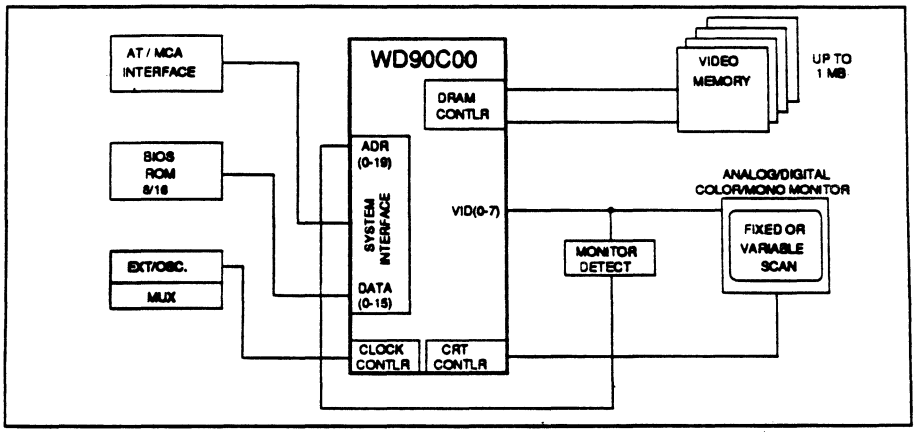


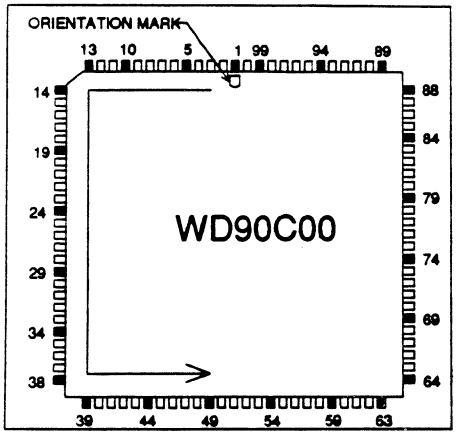
Figure 1. System Diagram

WD90C00

SALES ORDER INFORMATION :

PACKAGE TYPE	WESTERN DIGITAL PART NO.
100 PIN PLCC	WD90C00JK00
100 PIN PFP	WD90C00LK00

100 PIN PLCC (TOP VIEW)



100 PIN PFP (TOP VIEW)

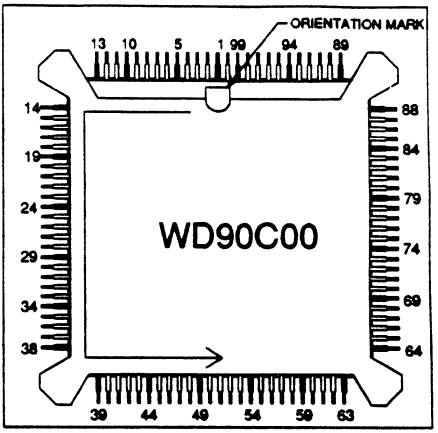


Figure 2. Pin Diagram

PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL	PIN	SYMBOL
36	RSET	40	DA1	2	MD4	48	VID7
76	MCLK	39	DA0	3	MD3	49	VID6
75	VCLK0	21	EMEM	4	MD2	50	VID5
74	VCLK1	33	EION	5	MD1	53	VID4
73	VCLK2	9	BHEN	6	MD0	54	VID3
28	A19	31	MRDN	80	CAS10N	55	VID2
27	A18	32	MWRN	83	CAS32N	56	VID1
24	A17	29	IORN	79	RAS10N	57	VID0
23	A16	30	IOWN	82	RAS32N	59	PCLK
22	A15	10	SFDBKN	81	OE10N	47	RPLTN
20	DA15	34	RDY	84	OE32N	58	WPLTN
19	DA14	35	IRQ	85	WE0	62	BLNKN
18	DA13	8	DS16N	86	WE1	60	HSYNC
17	DA12	89	MD15	87	WE2	61	VSYNC
16	DA11	90	MD14	88	WE3	7	EBROMN
14	DA10	91	MD13	63	MA8	11	EABUFN
13	DA9	92	MD12	65	MA7	38	EDBUFN
12	DA8	93	MD11	66	MA6	37	DIR
46	DA7	94	MD10	67	MA5	25, 52	+5VDC
45	DA6	95	MD9	68	MA4	78, 100	+5VDC
44	DA5	96	MD8	69	MA3	1, 15,	GND
43	DA4	97	MD7	70	MA2	26, 51,	GND
42	DA3	98	MD6	71	MA1	64, 77	GND
41	DA2	99	MD5	72	MA0		

WD90C00

Table of Contents

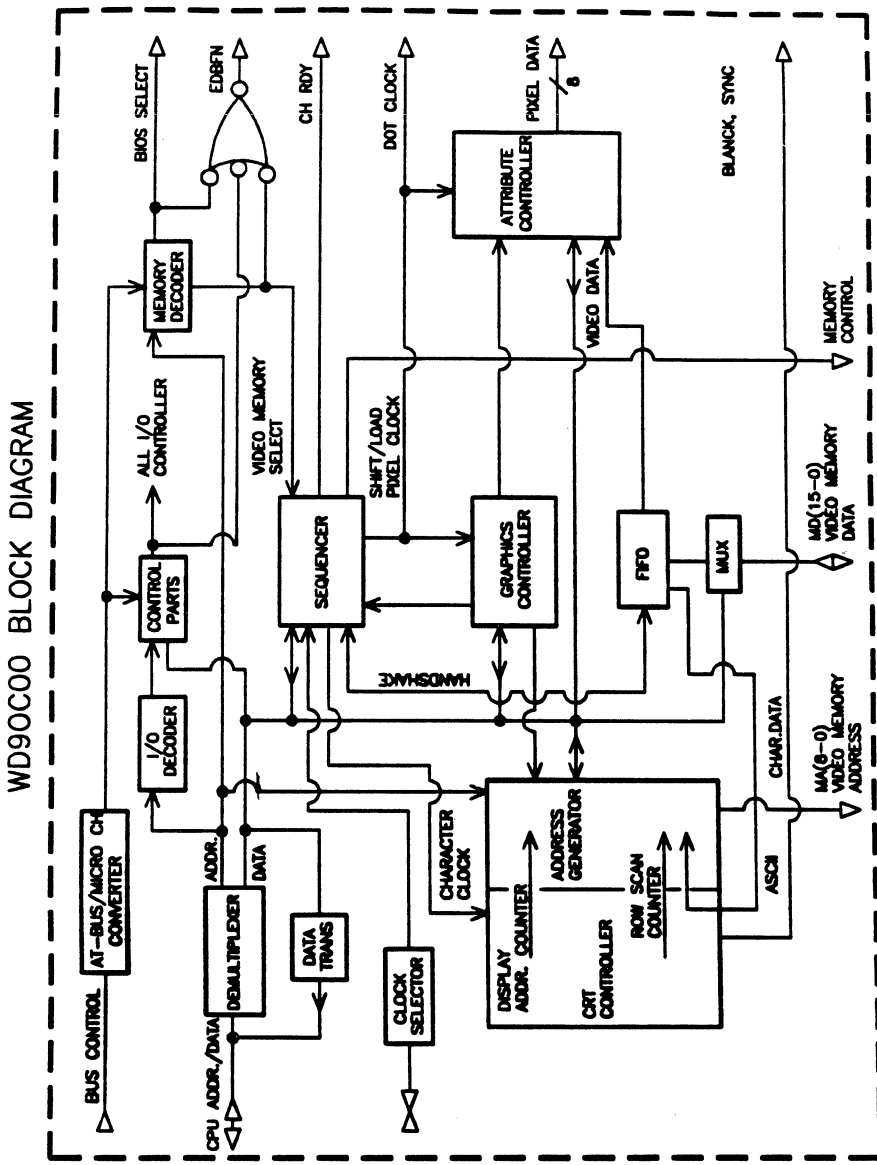

WD90C00 BLOCK DIAGRAM
BIOS SELECT
EDBFN
CH RDY
DOT CLOCK
PIXEL DATA
8
BLANCK, SYNC
MEMORY DECODER
ATTRIBUTE CONTROLLER
VIDEO DATA
MEMORY CONTROL
ALL I/O CONTROLLER
VIDEO MEMORY SELECT
SHIFT/LOAD PIXEL CLOCK
CONTROL PARTS
SEQUENCER
GRAPHICS CONTROLLER
FIFO
MUX
MD(15-0) VIDEO MEMORY DATA
I/O DECODER
HANDSHAKE
CHAR.DATA
MA(8-0) VIDEO MEMORY ADDRESS
AT-BUS/MICRO CH CONVERTER
ADDR.
DATA
CHARACTER CLOCK
ADDRESS GENERATOR
DISPLAY ADDR. COUNTER
ROW SCAN COUNTER
ASCII
CRT CONTROLLER
BUS CONTROL
DEMULTIPLEXER
DATA TRANS
CLOCK SELECTOR
CPU ADDR./DATA

FIGURE 3

WD90C00

SCOPE

Many applications require greater graphics capability than is available through the IBM Monochrome Display Adapter (MDA), Color Graphics Adapter (CGA), Enhanced Graphics Adapter (EGA), Multicolor Graphics Array (MCGA), and the Video Graphics Array (VGA). The Paradise WD90C00 is a 1.25 micron, 15,000 gate CMOS VLSI device that allows the design of a very high performance VGA graphics subsystem able to interface with the PC/XT/AT Bus, as well as the IBM Micro Channel Bus, while maintaining backwards compatibility with previous video standards. A major advantage of the WD90C00 is that designs implementing this graphics controller will be able to run applications requiring MDA, CGA, Hercules, AT&T 6300, and VGA hardware and BIOS compatibility, and also EGA register level compatibility on analog, TTL, or multifrequency monitors, in interlace or non-interlace mode.

This data sheet supplies sales order information, a functional overview, signal pin details, a block diagram, internal register descriptions, AC/DC characteristics, timing diagrams, VLSI package mechanical information, and a list of associated references.

WD90C00 DESCRIPTION

The WD90C00 internally contains four major modules. These are the CRT Controller, the Sequencer, the Graphics Controller and the Attribute Controller. The WD90C00 has 4 major interfaces: the CPU and BIOS ROM interface, the Clock interface, the DRAM Display Buffer interface, and the Video and RAM-DAC interface.

Since the WD90C00 arbitrates video memory accesses, between the system microprocessor and the CRT Controller contained within the WD90C00, all data passes through the WD90C00 when the system microprocessor writes to or reads from the video memory.

A FIFO is used internally to achieve the video display bandwidth necessary to interleave CPU accesses and display refresh cycles, using standard DRAMs.

WD90C00 MODULES

The CRT Controller section within the WD90C00 maintains screen refresh functions for the various display modes defined by the BIOS ROM resident firmware from a program of its registers. The WD90C00 CRT Controller also generates horizontal sync (HSYNC), vertical sync (VSYNC), and blanking for the display monitor and external RAMDAC.

The Sequencer functions as a timing generator for the AT bus or Micro Channel interface, in I/O or memory cycles. It also provides the character clock, and the dot clock for the CRT, Graphics, and Attribute Controllers.

The Graphics Controller manages data flow between video memory and the Attribute Controller during active display (non-blanked) periods. It also controls system microprocessor reads from and writes to the video memory, using the time slots defined by the Sequencer.

The Attribute Controller modifies the CRT display data stream in graphics and character modes. It controls display attributes such as blinking, underlining, cursor, pixel panning, reverse video, and background or foreground video.

WD90C00 INTERFACES

CPU AND BIOS ROM INTERFACE

The WD90C00 is designed to operate in two different bus architecture configurations. These are the PC/XT/AT Bus and the PS/2 Micro Channel Bus. The selection of the mode is dependant on the setting of a configuration register bit CNF(2), which is determined upon power-up/reset, and is described in the WD90C00 Paradise Register section of this data sheet.

When configured for AT or Micro Channel operation, the WD90C00 operates functionally in a manner that is conductive to PC/XT/AT or Micro Channel interfacing respectively. The signal pins, memory maps, and I/O ports all operate to optimize this interface with minimal external circuitry.

The WD90C00 provides all the signals, and decodes all the necessary memory and I/O addresses to interface with the AT bus or the Micro Channel bus, in 8 or 16 bit data path modes. WD90C00 also provides the necessary decoding of the adapter video BIOS ROM, and has additional signals and registers to help with BIOS ROM page mapping as done on the IBM PS/2 display adapter. Using the provided signals, the customer can implement designs which multiplex the address/data signals to the WD90C00 in 8 or 16 bit mode, control an 8 or 16 bit BIOS ROM, and generate the desired control/handshake signals (such as -CDDS16N in MCA mode).

The I/O data path is eight bit. The memory display buffer data path can be eight or sixteen bits wide. EGA Planar modes have an eight bit data path with the CPU. Text modes and 256 color extended modes (packed pixel modes) can have a sixteen bit data path if the video subsystem supports a 16 bit bus.

The WD90C00 will provide the necessary wait states for CPU accesses to the video memory. Wait states for I/O accesses, and BIOS ROM accesses are not generated.

Special I/O ports, such as 46E8H(AT) for setup, and 102H for VGA enable, have been implemented internally in the WD90C00.

DRAM INTERFACE

The WD90C00 optimizes its interface to the video memory display buffer. The video memory DRAMs are organized as 4 planes and the WD90C00 is designed for 3 configurations of DRAMs. Each plane can be configured as 64 KBytes (256 KByte total), 128 KBytes (512 KByte total), or 256 KBytes (1 MByte total).

The WD90C00 provides the necessary control signals and address/data lines to access the video memory as two 16 bit data interleaved banks. For display refresh cycles, the WD90C00 will perform page mode read operations on the video memory in graphics modes. In alpha modes, a choice of page video memory read operation is also provided. For video memory write operations during graphics or alpha modes, the WD90C00 will generate standard RAS/CAS cycles in non-page modes. WD90C00 will also refresh the DRAMs with 3 or 5 refresh cycles after every horizontal scan line.

The WD90C00 supports 256 KBytes of DRAM by using eight 64K X 4 page mode DRAM chips; 512 KBytes of DRAM by using sixteen 64K X 4 page mode DRAM chips; or 1 MByte of DRAM using eight 256K X 4 page mode DRAM chips. Usually a 36 MHz MCLK and 120ns DRAMs are used. A 640 X 400 X 256 color mode is supported when 100 ns DRAMs and a 44.9 MHz MCLK is used. 640 X 480 X 256 color mode is supported when the 512K DRAM configuration along with 100ns DRAMs and a 44.9 MHz MCLK are used. The WD90C00 Paradise registers provide support for accesses of up to 1 MByte of video memory.

VIDEO INTERFACE

The WD90C00 is optimized to connect to an analog CRT monitor through a RAMDAC, but it may also be used to drive other types of displays, such as TTL monitors along with the correct register programming using recommended crystal frequencies. In interfacing to an analog monitor through an external RAMDAC, the WD90C00 provides all the necessary signals to interface to the video RAMDAC.

The video interface for a CRT is very dependent on the CRT requirements and the resolution and depth (bits/pixels) of the image desired. New monitors, such as multifrequency monitors, are less stringent because of the many sync frequencies available. The WD90C00 can be programmed to directly generate all the CRT signals for up to 8 bits/pixel (256 color) displays. In addition, external hardware can be added to allow higher display resolutions by trading off the number of bits/pixel.

The Micro Channel Auxiliary Video Connector and the AT Feature Connector can be connected to WD90C00. The WD90C00 also provides an input for a monitor type detection interface as done on the IBM VGA using comparators.

CLOCK INTERFACE

The WD90C00 has four clock input signal pins. These are: the separate memory clock, MCLK, which drives the DRAM timing in graphics and alpha modes; and the three video clocks, VCLK0, VCLK1, and VCLK2, which drive the video timing. WD90C00 also provides the option to externally control a multiplexer that supplies the video clock. The MCLK can also be selected as the video dot clock.

WD90C00 POWER-UP CONFIGURATION

The WD90C00 uses the memory data pins to configure an internal configuration register upon power-up/reset. CNF(2) will determine whether the WD90C00 will operate in AT or Micro Channel Architecture (MCA) implementation. Other CNF bits configured by WD90C00 at power-up/reset are used as status bits, or for clock source control. For more information on WD90C00 power-up configuration, refer to the Paradise Register section of this data sheet.

PIN DESCRIPTION

The table below provides WD90C00 pin definitions for the 100 Pin Plastic Leadless Chip Carrier (PLCC) and Plastic Flat Pack (PFP) package. The WD90C00 mnemonics are used. For more design details in AT or Micro Channel modes refer to the application notes and reference section of this document.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			POWER ON
36	RSET	I	RESET: This signal input will reset the WD90C00. MCLK and VCLK0 should be connected to WD90C00 in order for the WD90C00 to initialize during Reset. Paradise registers PR1, PR11, and CNF are initialized at power-up reset based on the logic level on the MD(7-0), MD(15-11) bus as determined by pull-up/ pull-down resistors. Outputs EABUFN and EDBUFN are tri-stated during reset. The active high reset pulse width should be at least ten MCLK clock periods.
			CLOCK SELECTION
76	MCLK	I	MEMORY CLOCK: This clock signal determines the VGA graphics and alpha mode video DRAM read/write access timing as well as system microprocessor I/O and memory timing. MCLK should be equal or greater than VCLK. It is less than 36 MHz for 120 ns DRAMS, and less than 45 MHz for 100 ns DRAMS.
75	VCLK0	I	VIDEO CLOCK 0: This input is the video display clock for alphanumeric and graphics display modes. Typically, VCLK0 is 25.175 MHz to display 640 pixels per horizontal display line. The Miscellaneous Output Register bits 2 and 3, both set to 0, will select this clock.
74	VCLK1	I/O	VIDEO CLOCK 1: This pin can be a second video display clock input or an output to external clock selection module. Pin direction is determined on Reset by a pull-up/down resistor on pin MD3. A VCLK1 input frequency of 28.322 MHz is used to display 720 pixels per horizontal line. When it is an output, VCLK1 is an active low pulse during I/O writes to port 3C2H. Refer to the Configuration Register description.
73	VCLK2	I/O	VIDEO CLOCK 2: This pin can be a third video display clock input or an output to external clock selection module. Pin direction is programmed simultaneously with that of VCLK1. It acts as either a user defined external clock input, or as an output reflecting the content of bit PR2(1) if CNF (3) is set to 1. Refer to the Configuration Register description.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			CPU ADDRESS AND DATA BUS
28 27 24 23 22	A19 A18 A17 A16 A15	I I I I I	ADDRESS ONLY BUS (A15-A19): These active high inputs form the high-order five bits of video memory address. These addresses (19:16) are not decoded during I/O accesses in AT or MCA implementation. These inputs are directly connected to the system bus.
20 19 18 17 16 14 13 2 46 45 44 43 42 41 40 39	DA15(*) DA14 DA13 DA12 DA11 DA10 DA9 DA8 DA7 DA6 DA5 DA4 DA3 DA2 DA1 DA0	I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O I/O	DATA/ADDRESS BUS (DA0-DA15): These signals comprise an active high multiplexed data/address bus for I/O and memory accesses. Only the low eight bits are used for data during I/O read and write cycles. During every I/O read and write, the voltage level on DA15 is used to help determine the monitor type, and can be read at port 3C2H bit 4. A logic 0 or logic 1 on DA15 places a logic 0 or a logic 1 into bit 4 of the Input Status Register 0, respectively. Refer to the general register description for more information. NOTE : " * " DA15 signal is multiplexed with data bit 15 and CRT monitor sense input for auto monitor detection. Refer to technical brief on auto monitor detection circuit.
			CPU CONTROL BUS
21	EMEM	I	ENABLE DISPLAY MEMORY: This signal is active high in both Micro Channel and AT modes. In AT Mode, EMEM enables video memory accesses. BIOS ROM accesses are not controlled by EMEM. If the video memory is within the lowest 1MB of the processor address space, EMEM signal must be active during video memory access. Otherwise, EMEM should be generated by external logic when the WD90C00 video memory is accessed. During AT Bus refresh time, EMEM can be connected to REFRESH to disable the WD90C00. In Micro Channel mode this signal enables I/O and video memory access. External logic is required to implement the function EMEM.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
10	SFDBKN	O	16 BIT WIDE BIOS ROM: In AT mode this active low signal is the inverted value of register PR1(1), which determines BIOS ROM data path width selection. It may be used to control data buffers for a 16 bit data path BIOS ROM and to generate the BIOS ROM chip enable signal MEMCS16 in AT mode. In Micro Channel mode, its mnemonic is -CD SFDBK. -CD SFDBK is the unlatched decode (active low) when a memory, I/O, or BIOS ROM access is done from the system bus and may be considered as adapter or VGA feedback. For further details, refer to the reference literature.
34	RDY	O	READY: An active high output which signals to the system processor that a memory access is completed and is only used to add wait states to the MCA or CPU bus cycles during video memory accesses. It is pulled inactive by WD90C00 to allow additional time to complete a bus operation. This signal is not generated on I/O cycles and accesses to the BIOS ROM. For further details, refer to the reference literature. This is a tri-state signal.
35	IRQ	O	INTERRUPT REQUEST: Programmable processor interrupt request. It is enabled via bit 5 in the Vertical Retrace End register. It is active high in AT mode and active low in Micro Channel mode. When the end of Vertical Display occurs, this signal will transition active, causing the interrupt. It will stay latched until CRTC11 bit 4 clears it. In an AT system IRQ is not connected, but may be connected if desired. -IRQ9 is used to generate interrupt in the Micro Channel mode. For further details, refer to the reference literature and the CPU section in the introduction. This is a tri-state signal.
8	DS16N	O	DATA SIZE 16: Active low enable for 16 bit video memory word transfers. It is a mode dependent signal. In AT mode, the signal level is as programmed in bit PR1(2) and may be used to indicate 16 bit external data buffers. See the Paradise Register (PR1) description for further details. This signal is used to generate -MEMCS16 using external logic for AT mode designs. In Micro Channel mode, the signal is active only during BIOS ROM accesses (if enabled) by PR1(1)) and/or during memory 16 bit data path access (if enabled by PR1(2)). See the section on Paradise Registers or consult the reference literature for more information.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
33	EION	I	ENABLE I/O: In AT mode, this active low signal enables I/O accesses to the WD90C00. In Micro Channel mode, this signal is the set up input pin and is connected to the card set up or the VGA setup. The externally designed system I/O (96H for Adapter card or 94H bit 5 for system board design) is connected to the EION pin. When this signal is high, the WD90C00 is enabled or in the operating state. An active low signal on this pin puts the WD90C00 into set up mode. During the set up mode, write logic 1 to WD90C00 internal port 102H to awaken the WD90C00 after power on. Refer to application note for more information. When in set up mode, the WD90C00 will only respond to the internal I/O register located at 102H. Accesses to port 3C3H (external) and BIOS ROM addresses are not affected by setup mode, so they can be accessed.
9	BHEN	I	BUS HIGH ENABLE: In both AT and MCA mode, this active low signal enables and indicates transfer of data on the high byte of the data bus (DA8-D15) when WD90C00 is in 16 bit mode. With address A0, it distinguishes between high byte (DA15-8) and low byte (DA0-7) data transfers. It is not used for I/O transfers in either AT mode or Micro Channel mode. When BHEN is not used for 8 bit data transfer implementation, it must be pulled high.
31	MRDN	I	MEMORY READ: In AT mode, this signal is called -SMEMR and is an active low memory read strobe. It is asserted in 8/16 bit memory read cycles. In Micro Channel mode, the signal is called M/-IO. It distinguishes between memory and I/O cycles. When (M/-IO) is high, a memory cycle is in process. A low on (M/-IO) shows that an I/O cycle is in process. For further details, refer to the reference literature.
32	MWRN	I	MEMORY WRITE: The Active low memory write strobe in AT mode for 8/16 bit data transfers. In Micro Channel mode, it becomes -S0 and is the channel status signal which indicates the start and type of a channel cycle. Along with -S1, M/-IO, and -CMD signals, it is decoded to interpret I/O and memory commands. For further details, refer to the reference literature.
29	IORN	I	I/O READ: Active low I/O read strobe in AT mode. It is asserted in 8/16 bit I/O read bus cycles. -S1 is the alternate mnemonic used in Micro Channel mode to indicate the start and type of a channel cycle. For further details, refer to the reference literature.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
30	IOWN	I	I/O WRITE: Active low strobe. In AT mode, the strobe signals an I/O write for 8/16 bit I/O write cycles. In Micro Channel mode it is synonymous with -CMD; address bus validity is signaled by -CMD going low while the rising edge of -CMD indicates the end of a Micro Channel bus cycle. For further details, refer to the reference literature.
			VIDEO MEMORY DATA
89 90 91 92 93 94 95 96 97 98 99 2 3 4 5 6	MD15 MD14 MD13 MD12 MD11 MD10 MD9 MD8 MD7 MD6 MD5 MD4 MD3 MD2 MD1 MD0	I/O	DISPLAY MEMORY DATA (D0-D15): These lines are the data bus to the video display DRAMS. Data lines MD0-7 are pulled up or down with resistors to provide set up information on power-up (reset) as follows: MD / Power-Up Function / Register (Bit) 15 EGA SW4 PR11(7) + 14 EGA SW3 PR11(6) + 13 EGA SW2 PR11(5) + 12 EGA SW1 PR11(4) + 11 ANALOG/TTL Display CNF(8) * 7 General Purpose CNF(7) * 6 General Purpose CNF(6) * 5 General Purpose CNF(5) * 4 General Purpose CNF(4) * 3 VCLK1,2 Input/Output CNF(3) + 2 AT/Micro Channel Mode CNF(2) + 1 BIOS ROM Data Path PR1(1) * 0 BIOS ROM Mapping PR1(0) * NOTE: " * " Pulldown resistor sets these bits to logic 1. " + " Pullup resistor sets these bits to logic 1. For more details refer to Paradise Registers.
			VIDEO MEMORY ADDRESS
63 65 66 67 68 69 70 71 72	MA8 † MA7 † MA6 † MA5 † MA4 † MA3 † MA2 † MA1 † MA0 †	O	MEMORY ADDRESS (MA0-MA8): Display memory DRAM address.

NOTE:

1. "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4) = 1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			VIDEO MEMORY CONTROL SIGNALS
80	CAS10N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 1 & 0 CAS output signal.
83	CAS32N †	O	COLUMN ADDRESS STROBE: Active low Memory Maps 3 & 2 CAS output signal.
79	RAS10N †	O	ROW ADDRESS STROBE: Active low Memory Maps 1 & 0 RAS output signal.
82	RAS32N †	O	ROW ADDRESS STROBE: Active low Memory Maps 3 & 2 RAS output signal.
81	OE10N †	O	OUTPUT ENABLE: Active low Memory Maps 1 & 0 DRAM output enable.
84	OE32N †	O	OUTPUT ENABLE: Active low Memory Maps 3 & 2 DRAM output enable.
85	WE0N †	O	WRITE ENABLE: Active low Write Enable to DRAM bank 0, lower byte (Memory map 0).
86	WE1N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 0, upper byte (Memory map 1).
87	WE2N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, lower byte (Memory map 2).
88	WE3N †	O	WRITE ENABLE: Active low Write Enable for DRAM bank 1, upper byte (Memory map 3).

NOTE:

1. "†" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(4) = 1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			RAMDAC INTERFACE
48 49 50 53 54 55 56 57	VID7 § VID6 § VID5 § VID4 § VID3 § VID2 § VID1 § VID0 §	O	VIDEO (VD0-VD7): Pixel video data output to DAC.
47	RPLTN	O	READ PALETTE: Video DAC register and color palette read signal. Active low during I/O read to addresses at 3C6H, 3C8H, and 3C9H.
58	WPLTN	O	WRITE PALETTE: Video DAC register and color palette write signal. Active low during I/O write to addresses at 3C6H-3C9H.
59	PCLK	O	PIXEL CLOCK: Video pixel clock output used by the RAMDAC to latch video signals VID0-7. Its source is one of the video clock inputs: VCLK0, VCLK1, or VCLK2 as determined by the Miscellaneous Output register. Note that VCLK0, 1, or 2 is divided by two in 320/360 pixel display mode to derive PCLK.
62	BLNKN §	O	BLANK: Active low RAMDAC blank pulse.
			CRT CONTROL
60	HSYNC §	O	HORIZONTAL SYNC: Display monitor horizontal synchronization pulse. Active high or low depending on the Miscellaneous register programming.
61	VSYNC §	O	VERTICAL SYNC: Active high display monitor vertical synchronization pulse. It is active high or low, depending on the Miscellaneous Output Register.

NOTES:

1. "§" For testing purposes, these pins can be tri-stated by setting Paradise Register PR4(5) = 1.

PIN NO.	PIN SYMBOL	PIN TYPE	DESCRIPTION
			BIOS ROM CONTROL
7	EBROMN	O	ENABLE BIOS ROM ACCESS: In both AT and Micro Channel modes this signal is active (low) during memory reads in the address range (C0000H-C7FFFH) if enabled by bit PR1(0). It is not active for accesses to addresses in the range C6000H-C67FFH. However, the C6000H-C67FFH address range can be mapped in to increase BIOS space by setting PR17(0) = 0. In AT mode only, a write to the WD90C00 internal I/O port address 46E8H causes this signal to be used as a write strobe for an external register used in BIOS ROM page mapping.
			BUFFER CONTROL
11	EABUFN	O	ENABLE ADDRESS BUFFER: This active low signal permits control of an external address buffer for multiplexing address and data to WD90C00. It is tri-stated while Reset is active. When in MCA implementation, this output becomes the high byte data bus enable signal during the 16 bit data transfers and is referred as EDBHN in Figures 10, and 11.
38	EDBUFN	O	ENABLE DATA BUFFER: Allows control of an external data buffer for multiplexing address and data to WD90C00. It is tri-stated while Reset is active.
37	DIR	O	DIRECTION CONTROL: Active high Direction Control for reads of the MD0-15 data bus in AT and MCA implementation. The default state is low until a read cycle occurs, and the WD90C00 will drive DIR high to change the direction of the data buffers.
			POWER AND GROUND
25	VCC	-----	+5VDC
52	VCC	-----	+5VDC
78	VCC	-----	+5VDC
100	VCC	-----	+5VDC
1	GND	-----	Ground
15	GND	-----	Ground
26	GND	-----	Ground
51	GND	-----	Ground
64	GND	-----	Ground
77	GND	-----	Ground

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to 70°C
Storage temperature	-40°C to 125°C
Voltage on all inputs and outputs with respect to Vss	-0.3 to 7 Volts
Power dissipation	1.0 Watt

NOTE: Stressess above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

STANDARD TEST CONDITIONS

The characteristics below apply for the following standard test conditions, unless otherwise noted. All voltages are referenced to Vss (0V Ground). Positive current flows into the referenced pin.

Operating temperature range	0° to 70°C
Power supply voltage	4.75 to 5.25 Volts

D.C. CHARACTERISTICS

SYMBOL	PARAMETER	MIN.	MAX	UNITS	CONDITIONS	NOTE
V_{IL}	Input Low Voltage	-0.3	0.8	V	VCC = 5V +/-5%	
V_{IH}	Input High Voltage	2.0	VCC+0.3	V	VCC = 5V +/-5%	
I_{IL}	Input Low Current	-----	+/-10	uA	VIN = 0.0V	
I_{IH}	Input High Current	-----	+/-10	uA	VIN = VCC	
V_{OL}	Output Low Voltage	-----	0.4	V	IOL +4.0 mA	1
V_{OH}	Output High Voltage	2.4	-----	V	IOH = 4.0 mA	1
I_{OZ}	High Impedance Leakage Current	-10.0	10.0	uA	OV<VOUT<VCC	
I_{CC}	Stand By Current (All Inputs at TTL Levels)	-----	22	mA	VCC = 5.25 VDC TA = 0°C, Static	
I_{DD}	Operating current	-----	130	mA	VCC = 5.25V, MCLK= VCLK = 45MHz	
C_{IN}	Input Capacitance	-----	10	pF	FC = 1MHZ	
C_{OUT}	Output Capacitance	-----	10	pF	FC = 1MHZ	

NOTE :

1. WD90C00 outputs have 4.0 mA maximum source and sink capability except as follows:
   RDY = 24.0 mA sink and 4.0 mA source.
   IRQ = 24.0 mA sink and 4.0 mA source.

This page is intentionally left blank.

THE TIMING DIAGRAMS AND PARAMETERS IN THE AC CHARACTERISTICS MAY BE REVISED.

AC CHARACTERISTICS

I/O READ - AT MODE TIMING DIAGRAM (See Figure 4)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IORN	13	--	
2	Address Hold from IORN Active	4	--	
3	Read Data Valid from IORN Active	--	2Tp+40	1
4	IORN Pulse Width	2Tp+50	--	1
5	Read Data Hold from IORN Inactive	16	--	
6	EABUFN Inactive from IORN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IORN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	DIR Active to IORN Active	--	25	
11	DIR Inactive from IORN Inactive	--	26	
12	RPLTN Active from IORN Active	--	30	2
13	RPLTN Inactive from IORN Inactive	13	--	2
14	EION Hold from IORN Inactive	5	--	

NOTES:
* Units are in nanoseconds (ns)
\+ Tested with C_L = 70 pf unless specified otherwise.
1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 3C6H-3C9H, except 3C7H.

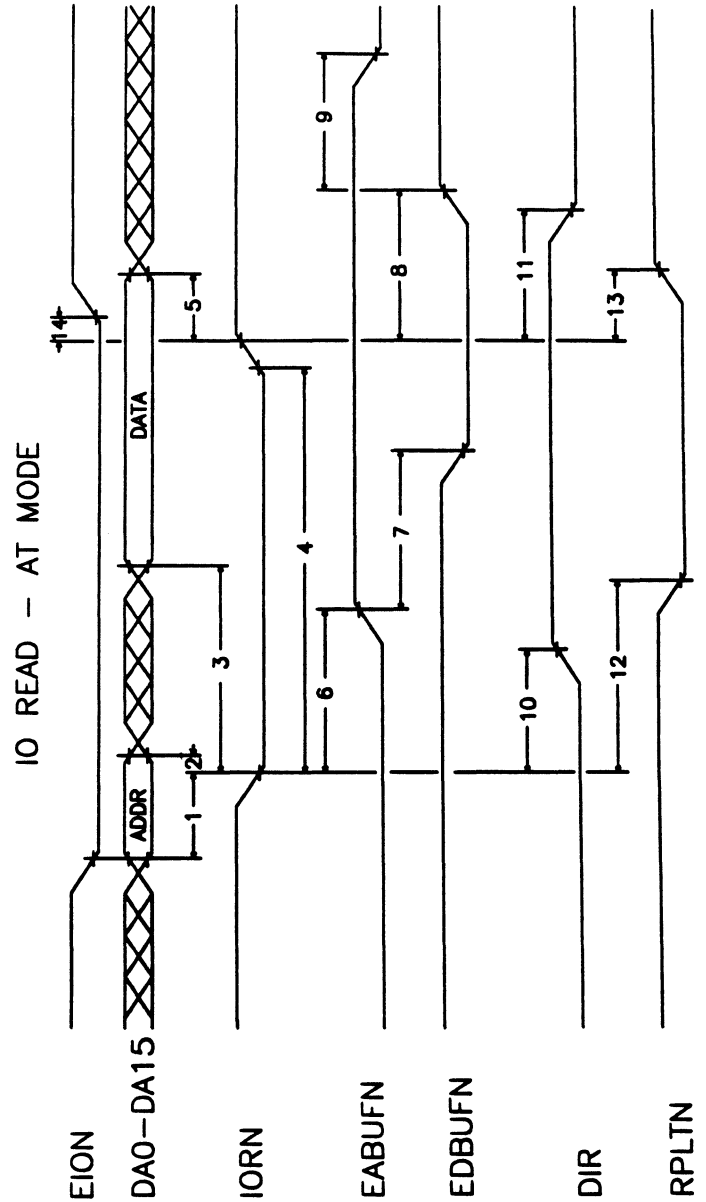

IO READ - AT MODE
EION
DA0-DA15
IORN
EABUFN
EDBUFN
DIR
RPLTN
ADDR
DATA
1
2
3
4
5
6
7
8
9
10
11
12
13
14

FIGURE 4

I/O WRITE - AT MODE TIMING DIAGRAM **(See Figure 5)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, EION Setup to IOWN	13	--	
2	Address Hold From IOWN Active	4	--	
3	Data Setup to IOWN Inactive	30	--	
4	IOWN Pulse Width	3Tp+50	--	1
5	Write Data Hold from IOWN Inactive	16	--	
6	EABUFN Inactive from IOWN Active	--	29	
7	EDBUFN Active from EABUFN Inactive	--	31	
8	EDBUFN Inactive from IOWN Inactive	--	30	
9	EABUFN Active from EDBUFN Inactive	--	31	
10	WPLTN Active from IOWN Active	--	2Tp+20	1,2
11	WPLTN Inactive from IOWN Inactive	16	--	2
12	EION Hold from IOWN Inactive	5	--	
13	EBROMN Active from IOWN Active	--	29	3
14	EBROMN Inactive from IOWN Inactive	--	27	3
15	IOWN Inactive Pulse Width	2Tp	--	1

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. WPLTN signal active only with I/O addresses 3C6H-3C9H.
3. EBROMN signal is also active during I/O port 46E8H write operation.

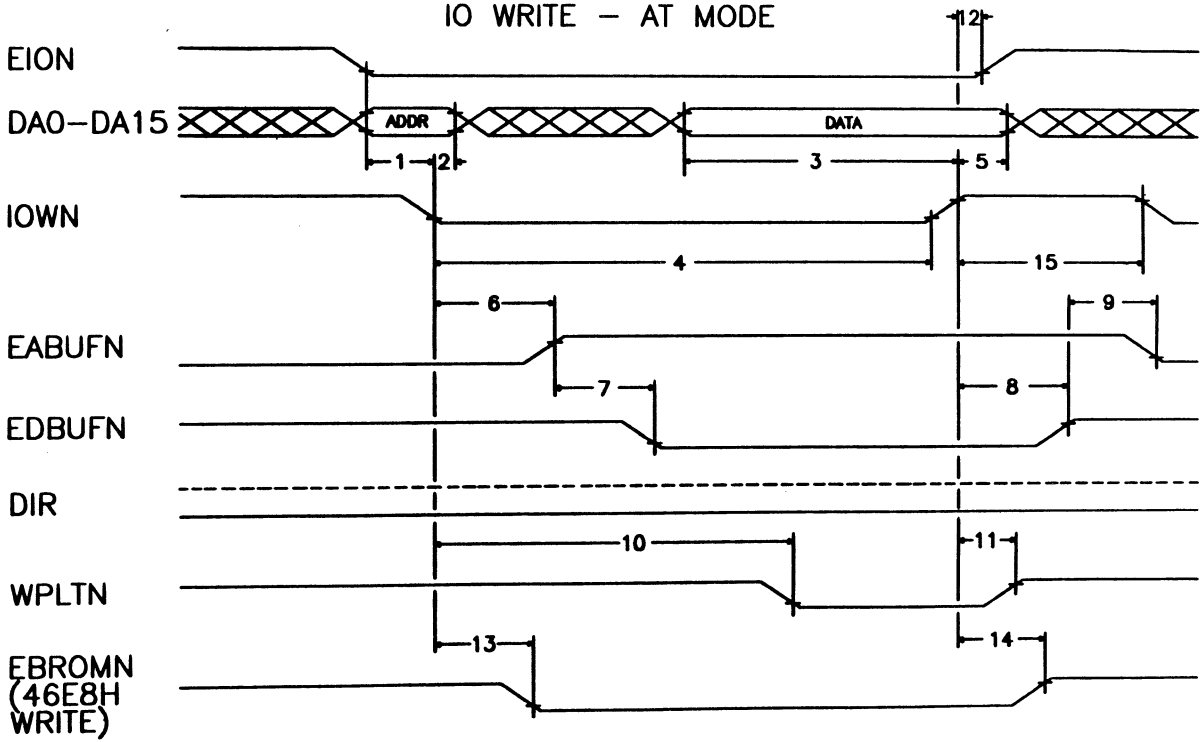

IO WRITE – AT MODE
EION
DA0–DA15
ADDR
DATA
IOWN
EABUFN
EDBUFN
DIR
WPLTN
EBROMN
(46E8H
WRITE)
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15

FIGURE 5

MEMORY READ - AT MODE TIMING DIAGRAM **(See Figure 6)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MRDN	13	--	5
2	Address, BHEN Hold from MRDN Active	4	--	5
3	Data Valid Setup to RDY	Tp+25	--	4
4	Data Hold from MRDN Inactive	10	--	
5	EABUFN Inactive from MRDN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MRDN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	DIR Active to MRDN Active	--	25	
10	DIR Inactive from MRDN Inactive	--	26	
11	RDY Inactive from MRDN Active	--	18	
12	RDY Active High from MRDN Active	--	2000	1
13	RDY Inactive (Tri-state) from MRDN Inactive	--	180	3
14	EBROMN Active from Address Active	--	30	2
15	EBROMN Inactive from MRDN Inactive	--	27	2
16	EMEM Hold from MRDN Inactive	4	--	
17	MRDN Active Low Time	90	--	
18	MRDN Inactive High Time	80	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. For standard VGA modes with MCLK greater than 36 MHz.
2. EBROMN signal is active for memory read addresses located at C0000-C7FFFH excluding addresses C6000-C67FFH which are optional and under program control.
3. This signal is tri-state and pulled up to +5V externally.
4. Tp = 1 / MCLK
5. BHEN will be sampled only if the 16 bit data transfers are enabled. For 8 bit implementation required in the PC / XT interface, BHEN must be pulled high.

MEMORY READ – AT MODE

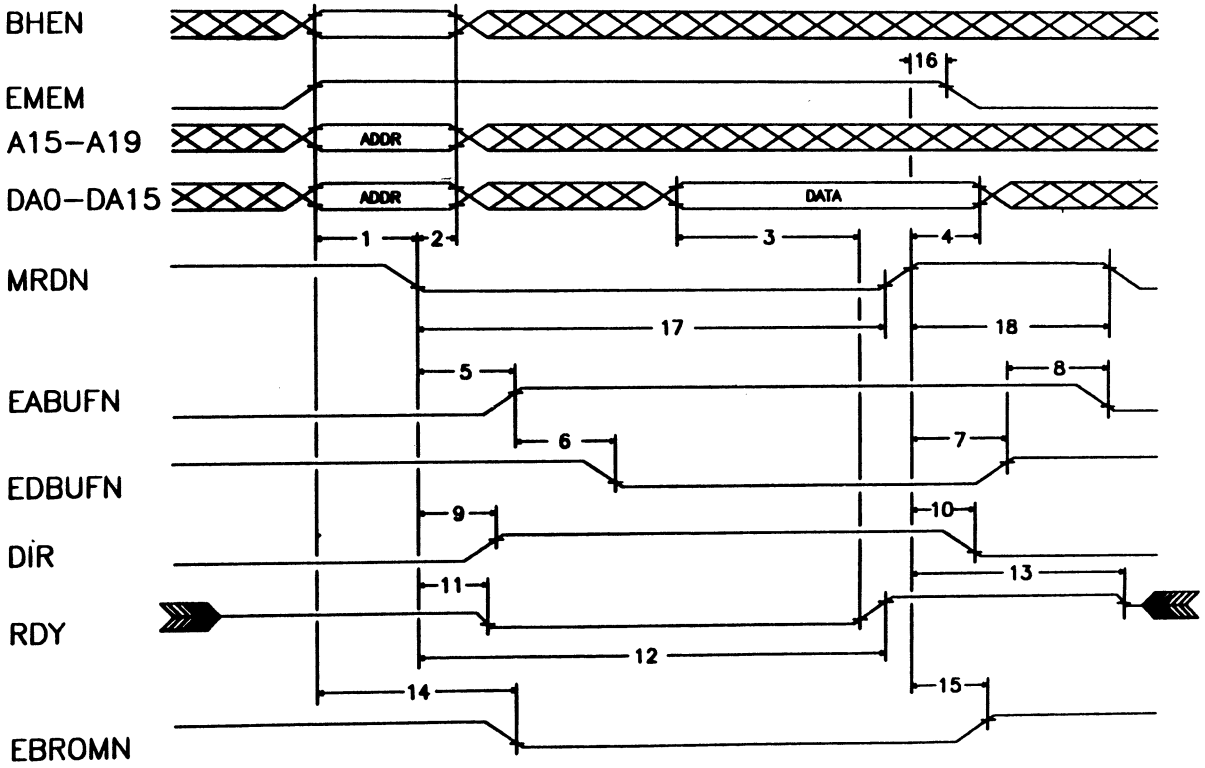


FIGURE 6

MEMORY WRITE- AT MODE TIMING DIAGRAM **(See Figure 7)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, BHEN, EMEM Setup to MWRN	13	--	4
2	Address, BHEN Hold from MWRN Active	4	--	4
3	Data Valid from MWRN Active	--	5Tp	1
4	Data Hold from MWRN Inactive	0	--	
5	EABUFN Inactive from MWRN Active	--	29	
6	EDBUFN Active from EABUFN Inactive	--	31	
7	EDBUFN Inactive from MWRN Inactive	--	30	
8	EABUFN Active from EDBUFN Inactive	--	31	
9	RDY Inactive from MWRN Active	--	18	
10	RDY Active High from MWRN Active	--	2000	2
11	RDY Inactive (Tri-state) from MWRN Inactive	--	180	3
12	EMEM Hold from MWRN Inactive	4	--	
13	MWRN Active Low Time	90	--	
14	MWRN Active High Time	80	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. For standard VGA modes with MCLK greater than 36 MHz.
3. This signal is tri-state and pulled up to +5V externally.
4. BHEN will be sampled only if the 16 bit data transfers are enabled. For 8 bit implementation required in the PC / XT interface, BHEN must be pulled high.

MEMORY WRITE–AT MODE

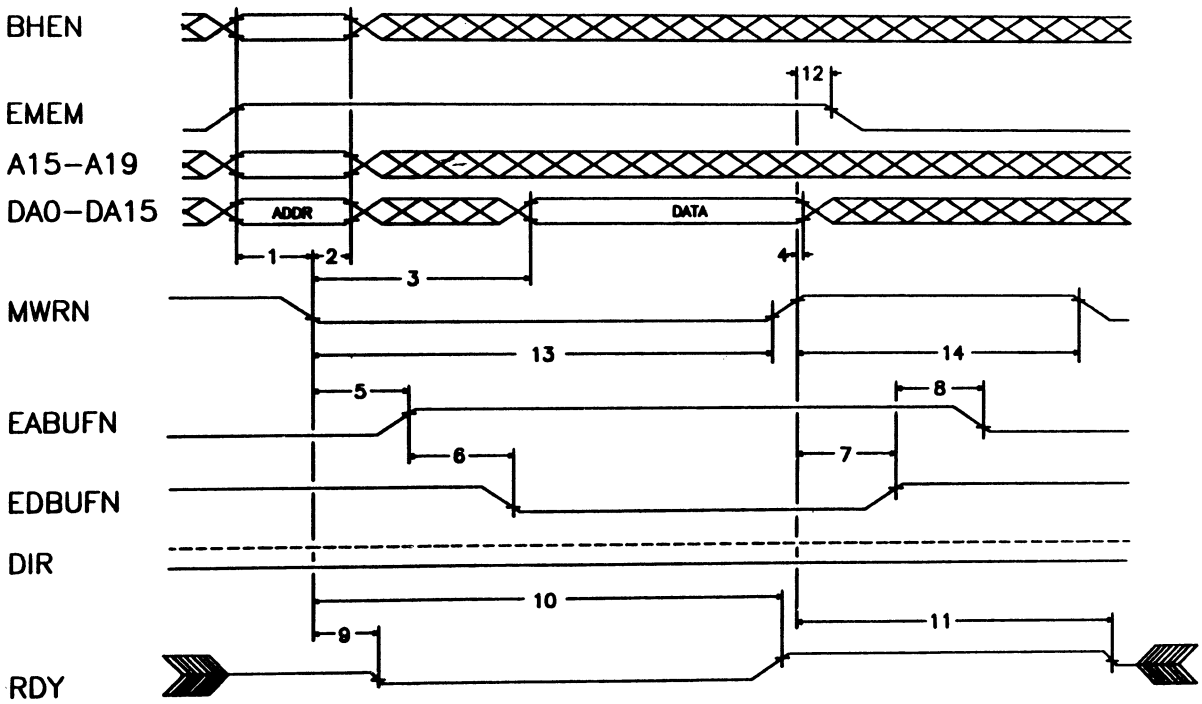


FIGURE 7

I/O READ - MICRO CHANNEL MODE TIMING DIAGRAM ** (See Figure 8)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Active	8	--	
5	-S0/-S1 Active to -CMD Active	3	--	
6	-S0/-S1 and M/IO Inactive from -CMD Active	5	--	
7	Read Data Valid from -CMD Active	--	40	
8	Read Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	50	--	
10	-CMD Inactive to next -CMD Active	2Tp	--	1
12	EDBUFN Active from -CMD Active	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RPLTN Active from -CMD Active	--	30	1,2
18	RPLTN Inactive from -CMD Inactive	13	--	2
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
20	SFDBKN Inactive from -CMD Inactive	--	32	4
21	-CD SETUP Active to -CMD Active	13	--	3
22	-CD SETUP Inactive from -CMD Inactive	4	--	3

NOTES:
* Units are in nanoseconds (ns)
\+ Tested with C_L = 70 pf unless specified otherwise.
1. Tp = 1/MCLK in all modes.
2. RPLTN signal active only with I/O addresses 3C6H-3C9H, except 3C7H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.
5 ** For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and WD90C00 pnemonics (Refer to the pin description section) are used in the MCA implementation timing diagrams.

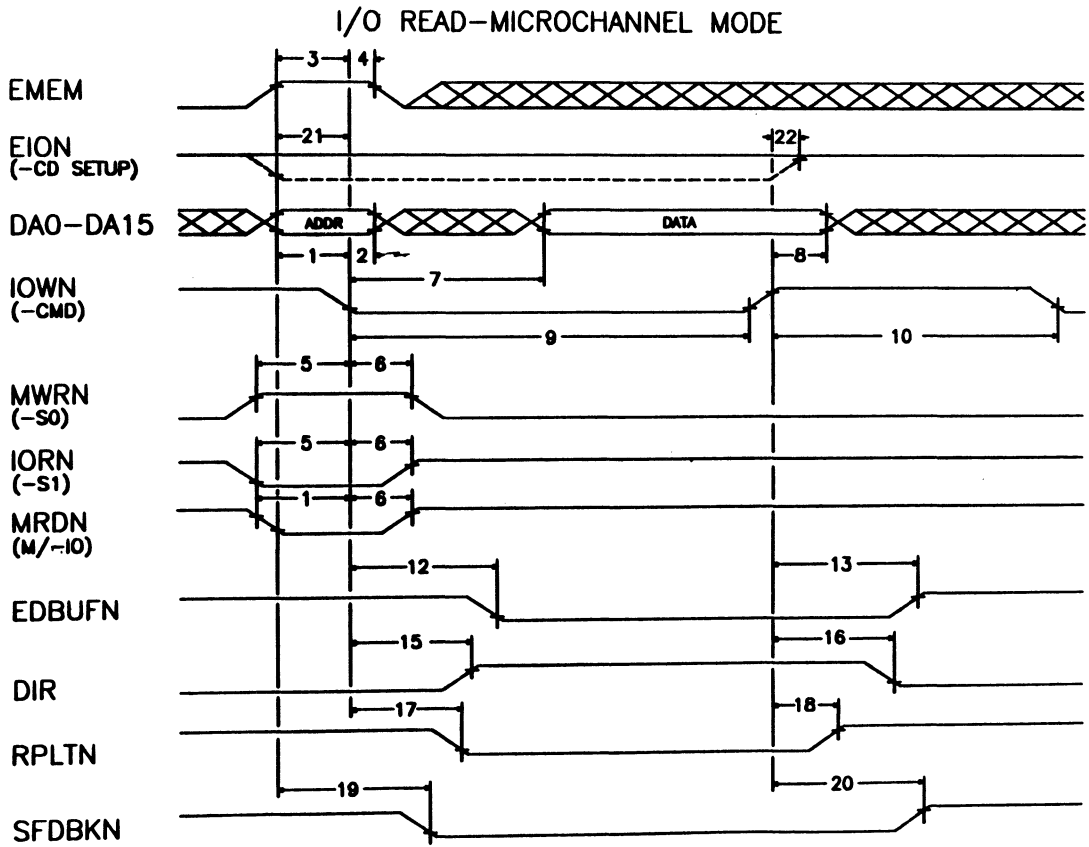

I/O READ–MICROCHANNEL MODE
EMEM
EION
(–CD SETUP)
DA0–DA15
IOWN
(–CMD)
MWRN
(–S0)
IORN
(–S1)
MRDN
(M/–IO)
EDBUFN
DIR
RPLTN
SFDBKN
ADDR
DATA
1
2
3
4
5
6
7
8
9
10
12
13
15
16
17
18
19
20
21
22

FIGURE 8

I/O WRITE - MICRO CHANNEL MODE TIMING DIAGRAM ** **(See Figure 9)**

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address, M/IO Setup to -CMD	13	--	
2	Address Hold from -CMD	4	--	
3	EMEM Active to -CMD Active	13	--	
4	EMEM Hold from -CMD Inactive	8	--	
5	-S0/-S1 Active to -CMD Active	3	--	
6	-S0/-S1 and M/IO Inactive from -CMD Active	5	--	
7	Write Data Setup to -CMD Inactive	--	30	
8	Write Data Hold from -CMD Inactive	18	--	
9	-CMD Pulsewidth	90	--	
10	-CMD Inactive to next -CMD Active	2Tp	--	1
12	EDBUFN Active from -CMD Active	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
15	WPLTN Active from -CMD Active	--	40	2
16	WPLTN Inactive from -CMD Inactive	18	--	2
17	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	4
18	SFDBKN Inactive from -CMD Inactive	--	32	4
19	-CD SETUP Active to -CMD Active	13	--	3
20	-CD SETUP Inactive from -CMD Inactive	4	--	3

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. WPLTN signal active only with I/O addresses 3C6H-3C9H.
3. EION signal active as -CD SETUP for I/O access to port 102H only, otherwise its level is high.
4. If -CD SETUP (EION) signal is low, this output stays inactive.

5 ** For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and WD90C00 pnemonics (Refer to the pin description section) are used in the MCA implementation timing diagrams.

I/O WRITE – MICROCHANNEL MODE

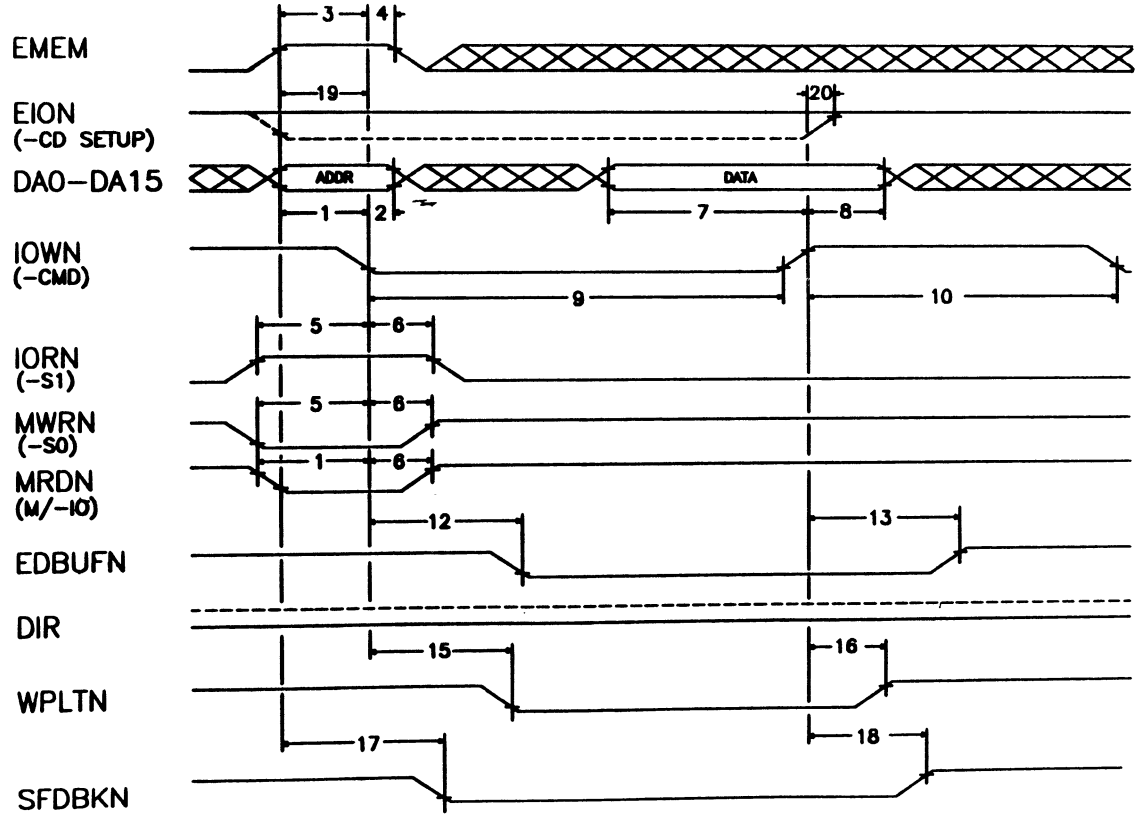


FIGURE 9

MEMORY READ - MICRO CHANNEL MODE TIMING DIAGRAM ** (See Figure 10)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	8	--	7
3	BHEN, EMEM, M/IO Setup to -CMD Active	13	--	7
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S0/-S1 Active to -CMD Active	3	--	
6	-S0/-S1 Hold from -CMD Active	5	--	
7	Read Data Valid Setup to RDY	Tp+25	--	4,5
8	Read Data Hold from -CMD Inactive	11	--	
9	-CMD Pulsewidth	90	--	5
10	-CMD Inactive to next -CMD Active	2Tp	--	4
11	EABUFN Active from -CMD Active	--	31	
12	EDBUFN Active from -CMD Active	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Inctive from -CMD Inactive	--	31	
15	DIR Active to -CMD Active	--	27	
16	DIR Inactive from -CMD Inactive	--	26	
17	RDY Inactive from Active Status	--	27	
18	RDY Active High from -CMD Active	--	2000	1
19	RDY Inactive (Tri-state) from -CMD Inactive	--	40	6
20	EBROMN Active from Address Valid	--	31	2
21	EBROMN Inactive from -CMD Inactive	--	29	2
22	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
23	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
24	SFDBKN Inactive from Address, M/IO, EMEM Invalid	--	32	
25	EMEM and M/IO Inactive from -CMD Active	8	--	
26	Address, Hold from -CMD Active	8	--	
27	-CDSETUP Active from -CMD Active	13	--	
28	-CDSETUP Inactive from -CMD Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1 For standard VGA modes with MCLK greater than 36 MHz.

2 EBROMN signal is only active for memory read addresses located at C0000-C7FFFH excluding addresses C6000-C67FFH which are optional and under program control.

3 DS16N signal active only for 16-bit access to memory and ROM addresses.

4 Tp = 1 / MCLK

5 ** For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and WD90C00 pnemonics (Refer to the pin description section) are used in the MCA implemenation timing diagrams.

6 This signal is tri-state. It is pulled up externally through a resistor to +5V.

7. BHEN will be sampled only if the 16 bit data transfers are enabled. For 8 bit implementation required in the PC / XT interface, BHEN must be pulled high.

MEMORY READ – MICROCHANNEL MODE

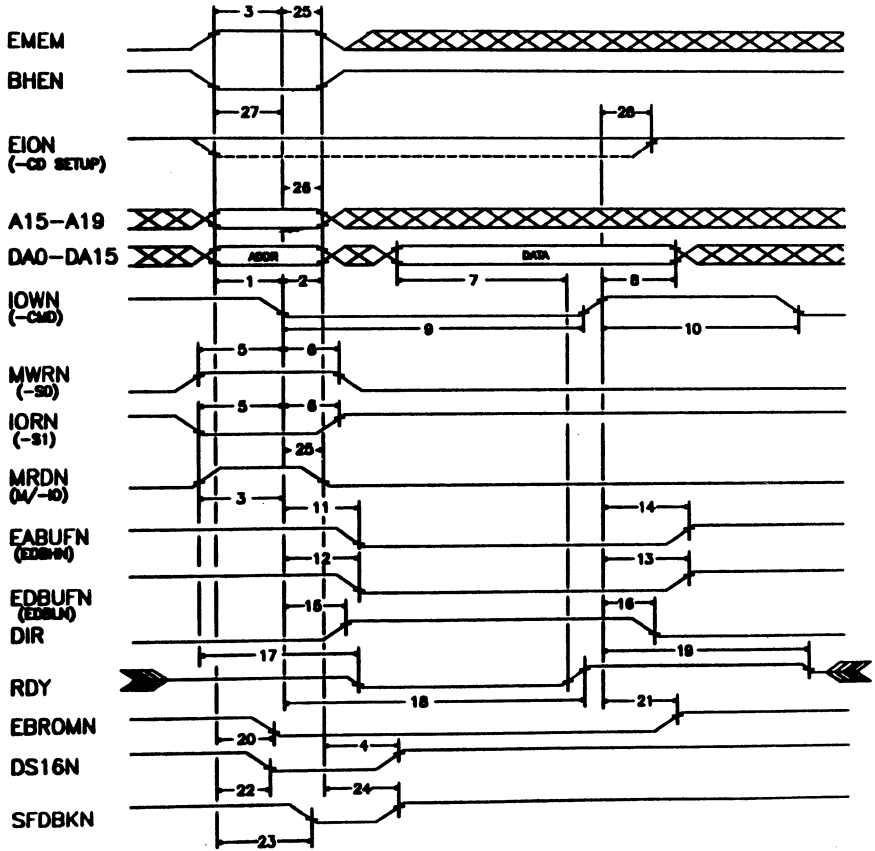


FIGURE 10

MEMORY WRITE - MICRO CHANNEL MODE TIMING DIAGRAM ** (See Figure 11)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Address Setup to -CMD	13	--	
2	Address, BHEN Hold from -CMD Active	8	--	7
3	BHEN,EMEM, M/IO Setup to -CMD Active	13	--	7
4	DS16N Inactive from EMEM, M/IO, Address Invalid	--	30	3
5	-S0/-S1 Active to -CMD Active	3	--	
6	-S0/-S1 Hold from -CMD Active	5	--	
7	Write Data Valid from -CMD Active	--	5Tp	1
8	Write Data Hold from -CMD Inactive	0	--	
9	-CMD Pulsewidth	90	--	
10	-CMD Inactive to next -CMD Active	2Tp	--	1
11	EABUFN Active from -CMD Active	--	31	
12	EDBUFN Active from -CMD Active	--	31	
13	EDBUFN Inactive from -CMD Inactive	--	31	
14	EABUFN Inactive from -CMD Inactive	--	31	
15	RDY Inactive from Active Status	--	27	
16	RDY Active High from -CMD Active	--	2000	2
17	RDY Inactive (Tri-state) from -CMD Inactive	--	180	5,6
18	DS16N Active from Address Valid, EMEM, and M/IO	--	32	3
19	SFDBKN Active from Address Valid, EMEM, and M/IO	--	34	
20	SFDBKN Inactive from, Address, M/IO, EMEM Invalid	--	32	
21	EMEM, and M/IO Inactive from -CMD Active	8	--	
22	Address, Hold from -CMD Active	8	--	
23.	-CDSETUP Active from -CMD Active	13	--	
24	-CDSETUP Inactive from -CMD Inactive	4	--	

NOTES:

* Units are in nanoseconds (ns)

\+ Tested with C_L = 70 pf unless specified otherwise.

1. Tp = 1/MCLK in all modes.
2. For standard VGA modes with MCLK greater than 36 MHz.
3. DS16N signal active only for 16-bit access to memory and ROM addresses.

4 ** For the signals that change between AT and Micro Channel modes, based upon CNF(2), the Micro Channel names and WD90C00 pnemonics (Refer to the pin description section) are used in the MCA implementation timing diagrams.

5 This signal is (tri-state) and is pulled up externally through a resistor to +5V.

6. RDY will always insert at least 1 wait state.
7. BHEN will be sampled only if the 16 bit data transfers are enabled. For 8 bit implementation required in the PC / XT interface, BHEN must be pulled high.

MEMORY WRITE – MICROCHANNEL MODE

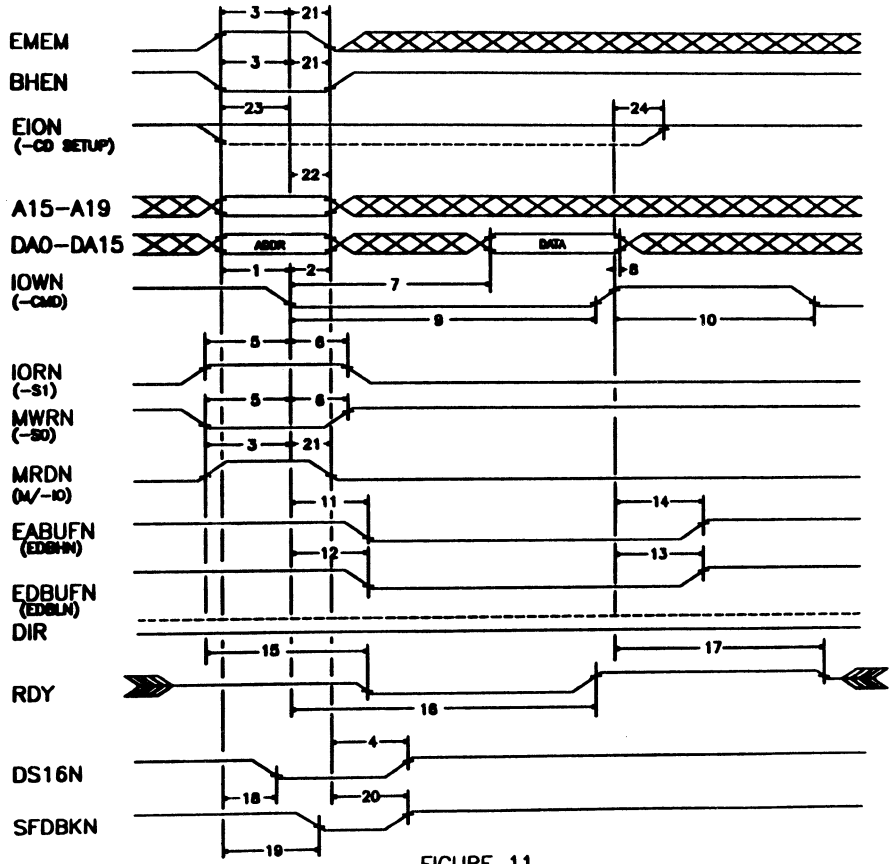


FIGURE 11

CRTC / CPU READ

NON-PAGE ALPHA MODE AND ALL MODE READ TIMING DIAGRAM

RAS ONLY REFRESH MODE (FIGURE 12)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock High	--	35	
2	Column Address Valid from Clock High	--	35	
3	RAS Active from Clock	--	40	
4	RAS Inactive from Clock	--	35	
5	CAS Active from Clock	--	35	2
6	CAS Inactive from Clock	--	35	2
7	Read Data Setup to CAS	25	--	
8	Read Data Hold from CAS	25	--	
9	Output Enable Active from Clock Low	--	35	
10	Output Enable Inactive from Clock Low	--	35	1
11	RAS Refresh Cycle Period	--	9Tp	1,3

NOTES:
* Units are in nanoseconds (ns)
\+ Tested with C_L = 70 pf unless specified otherwise.
1. In refresh cycle, RAS period is 5 clocks active and 4 clocks for precharge.
2. The CAS precharge time is 6 clocks and CAS active time is 3 clocks.
3. Tp = 1 /MCLK in all modes.

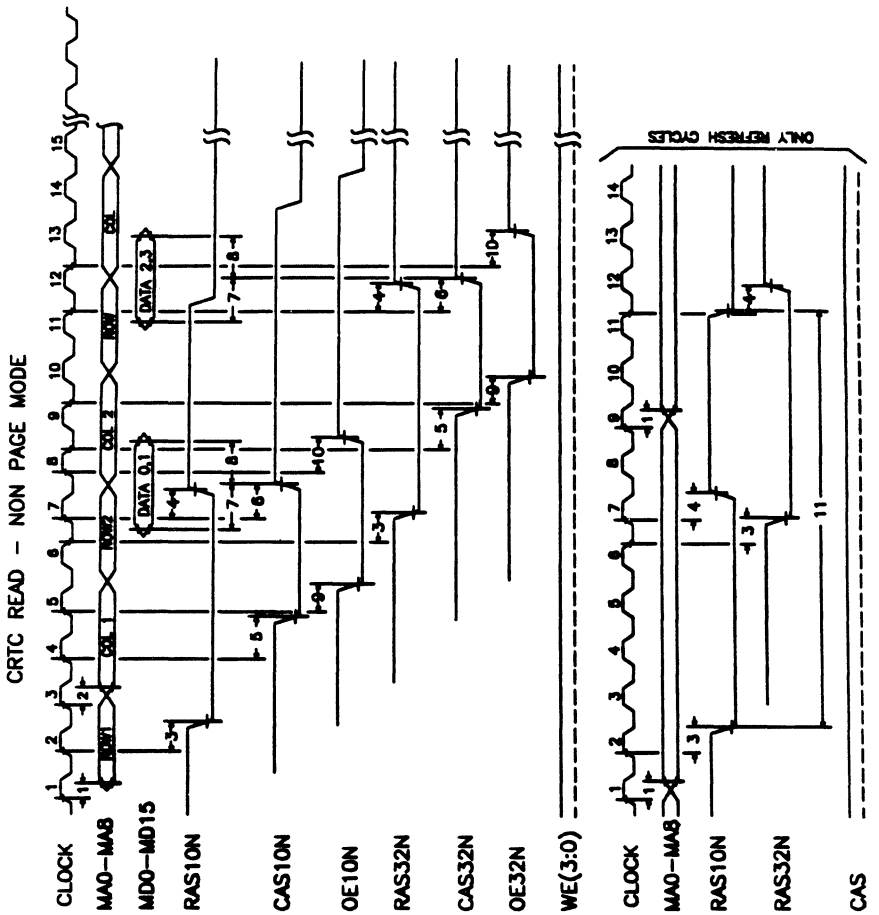

CRTC READ - NON PAGE MODE
CLOCK
MA0-MA8
MD0-MD15
RAS1ON
CAS1ON
OE1ON
RAS32N
CAS32N
OE32N
WE(3:0)
ROW1
COL 1
ROW2
COL 2
ROW
COL
DATA 0,1
DATA 2,3
ONLY REFRESH CYCLES
CLOCK
MA0-MA8
RAS1ON
RAS32N
CAS

FIGURE 12

CRTC READ

PAGE ALPHA AND GRAPHICS MODE TIMING DIAGRAM (See Figure 13)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock	--	35	1
2	Column Address Valid from Clock High	--	35	1
3	RAS Active from Clock	--	40	1
4	RAS Inactive from Clock	--	35	1
5	CAS Active from Clock	--	35	
6	CAS Inactive from Clock	--	35	
7	Output Enable Active from Clock	--	35	
8	Data Hold from CAS Inactive	25	--	
9	Data setup from CAS Inactive	25	--	
10	RAS Active Low time	--	10	us
11	CAS High Precharge time	2Tp	--	1
12	CAS Active Low time	3Tp	--	1

NOTES:
* Units are in nanoseconds (ns) unless otherwise specified.
\+ Tested with C_L = 70 pf unless specified otherwise.
1. Clock is MCLK in all modes.

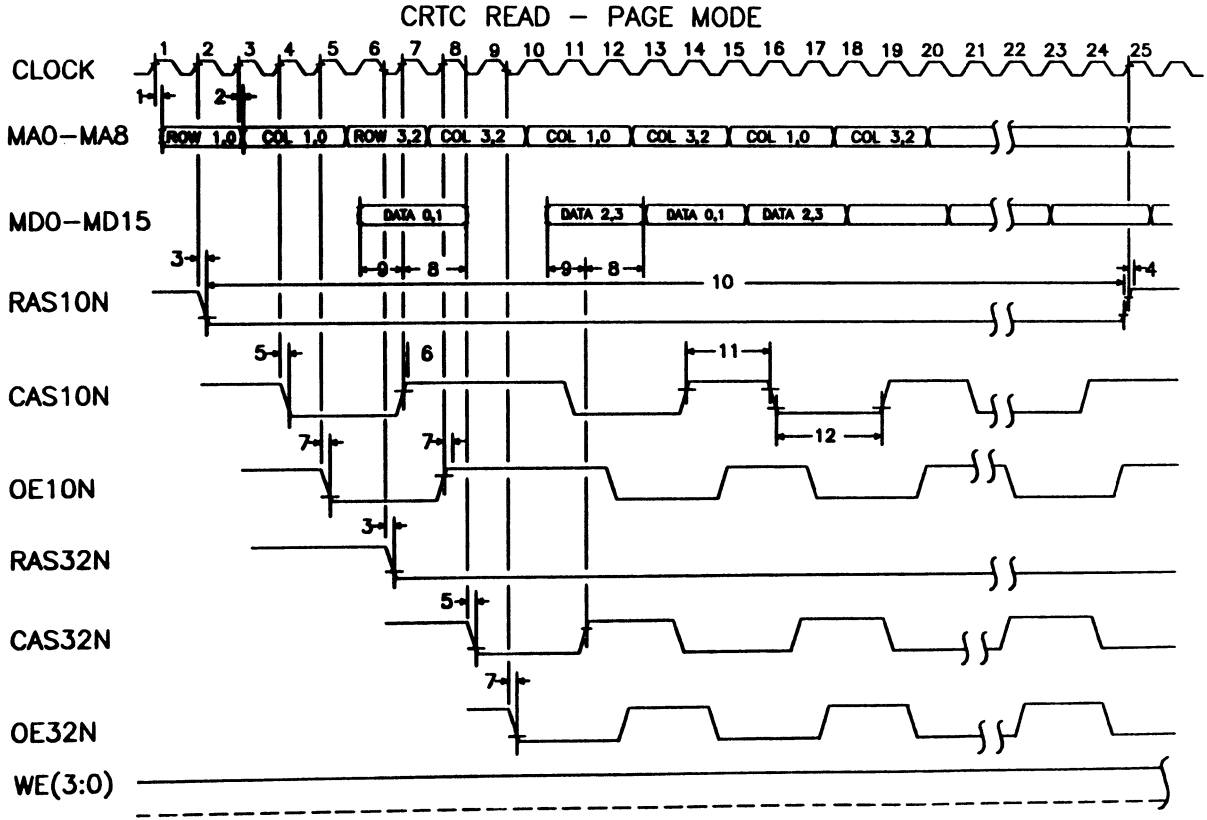

CRTC READ – PAGE MODE
CLOCK
MA0–MA8
ROW 1,0
COL 1,0
ROW 3,2
COL 3,2
COL 1,0
COL 3,2
COL 1,0
COL 3,2
MD0–MD15
DATA 0,1
DATA 2,3
DATA 0,1
DATA 2,3
RAS10N
CAS10N
OE10N
RAS32N
CAS32N
OE32N
WE(3:0)

FIGURE 13

CPU WRITE

ALPHA AND GRAPHICS MODE TIMING DIAGRAM (See Figure 14)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	Row Address Valid from Clock	--	35	
2	Column Address Valid from Clock	--	35	
3	RAS Active from Clock	--	40	
4	RAS Inactive from Clock	--	35	
5	CAS Active from Clock	--	35	2
6	CAS Inactive from Clock	--	35	2
7	Write Enable Active from Clock Low	--	35	
8	Write Enable Inactive from Clock Low	--	35	
9	Write Data(2:3) Setup to CAS32N Active	2Tp	--	1
10	Write Data(0:1) Hold from WE10 Active	2Tp	--	1
11	Write Data (2:3) Hold from CAS32N Active	1.5Tp	--	1

NOTES:
* Units are in nanoseconds (ns)
\+ Tested with C_L = 70 pf unless specified otherwise.
1. Tp = 1/MCLK in all modes.
2. CAS10N is referenced to Clock High and CAS32N to Clock Low.

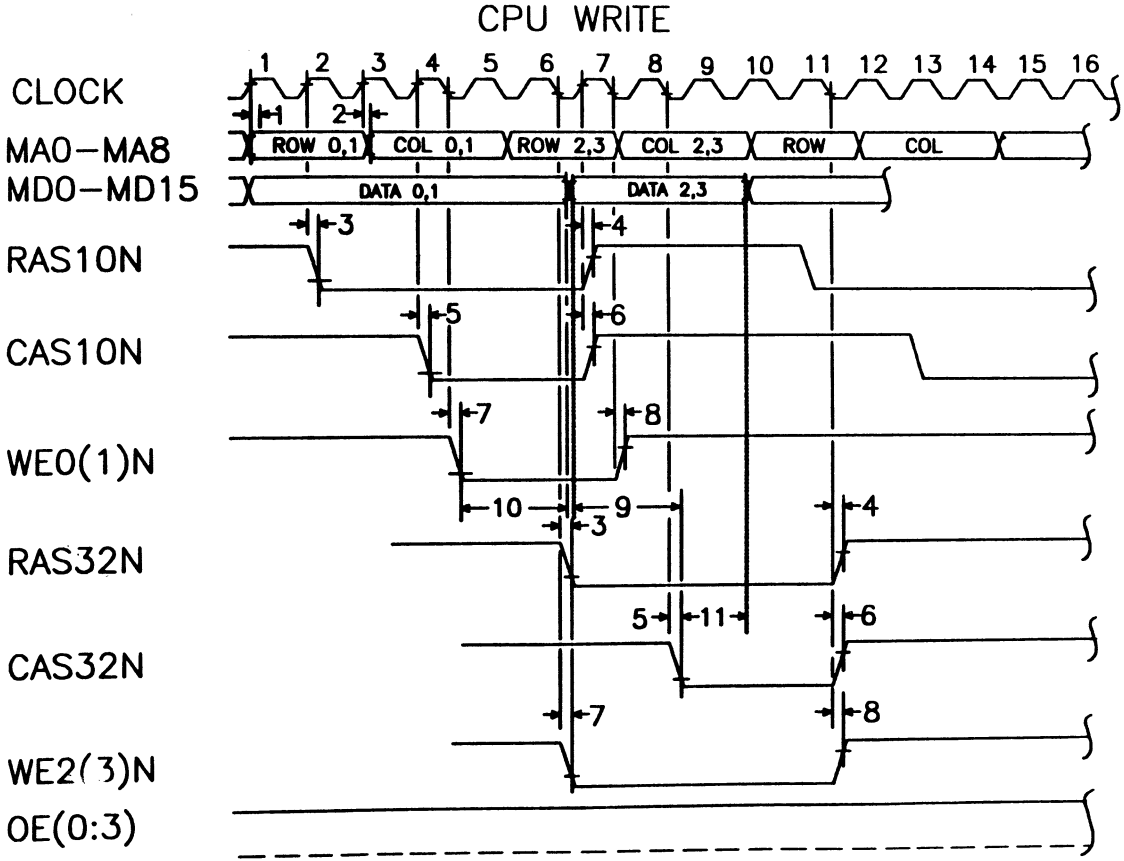

CPU WRITE
CLOCK
MA0–MA8
MD0–MD15
RAS1ON
CAS1ON
WE0(1)N
RAS32N
CAS32N
WE2(3)N
OE(0:3)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
ROW 0,1
COL 0,1
ROW 2,3
COL 2,3
ROW
COL
DATA 0,1
DATA 2,3

FIGURE 14

CLOCK AND VIDEO SIGNALS TIMING DIAGRAM (See Figure 15)

SYMBOL	PARAMETER	MIN	MAX	NOTES*+
1	MCLK Clock Period	23.8	--	1
2	MCLK Clock High Time	10.7	--	
3	MCLK Clock Low Time	10.7	--	
4	VCLK0, VLCK1, VCLK2 Clock Period	25	--	1
5	VCLK0, VLCK1, VCLK2 Clock Low Time	11.2	--	
6	VCLK0, VLCK1, VCLK2 Clock High Time	11.2	--	
7	PCLK Low from VCLK High	--	30	5
8	BLNKN Active Delay from VCLK	--	37	
9	BLNKN Inactive Delay from VCLK	--	38	
10	VSYNC Active Delay from VCLK	--	37	2
11	VSYNC Inactive Delay from VCLK	--	37	2
12	HSYNC Active Delay from VCLK	--	34	2
13	HSYNC Inactive Delay from VCLK	--	38	2
14	VID(7:0) Data from VCLK	--	30	5

NOTES:

* Units are in nanoseconds (ns)

1. Input clocks require a 50% duty cycle with a tolerance of 10 %.
2. VSYNC and HSYNC polarity is positive or negative depending on video mode.
3. PCLK / 2 is for 40 x 25 alpha modes or 320 x 200 x 256 color graphics modes.
4. C_L for VID(0:7) and PCLK is 30 pF.
5. There is a limit on the maximum skew between video clock and data outputs. With respect to the falling edge of PCLK, the delay of VID(0:7) output will not exeed + / - 5ns at 1.4V output level.
6. Duty cycle variations from VCLK to PCLK:
   Values are referenced to a input 50% waveform from 0.8V to 2.0V, 30pF load, and 1.3V threshold.
   High pulse width = Input width - 1.5ns Min
   Input width + 3.2ns Max
   Low pulse width = Input width - 3.2ns Min
   Input width + 1.5ns Max

CLOCK AND VIDEO SIGNALS

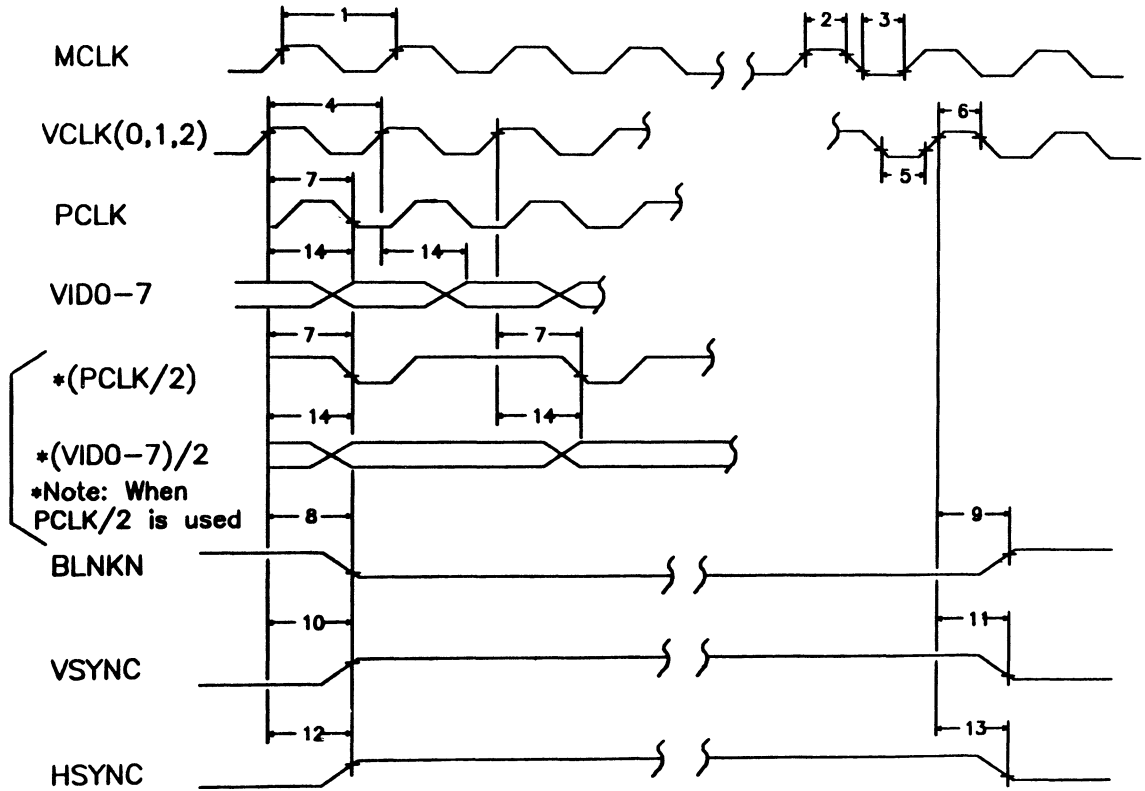


FIGURE 15

WD90C00 REGISTERS

All the standard IBM registers incorporated inside the WD90C00 are functionally equivalent to the VGA implementation while additional Paradise registers enhance the video subsystem. Compatibility registers provide functional equivalence for AT&T, Hercules, MDA, and CGA standards defined earlier using the 6845 CRT Controller. This section describes the VGA registers in greater detail followed by the, VGA / EGA difference section, and Paradise registers description. For more information, refer to the reference literature.

VGA REGISTERS SUMMARY

REGISTERS	RW	Monochrome	Color	Either
General Registers:				
Miscellaneous Output Reg	W			3C2
	R			3CC
Input Status Reg 0	RO			3C2
Input Status Reg 1	RO	3BA	3DA	
Feature Control Reg	W	3BA	3DA	
	R			3CA
‡Video Subsystem Enable	RW			3C3
Sequencer Registers:				
Sequencer Index Reg	RW			3C4
Sequencer Data Reg	RW			3C5
CRT Controller Registers:				
Index Reg	RW	3B4	3D4	
CRT Controller Data Reg	RW	3B5	3D5	
Graphics Controller Registers:				
Index Reg	RW			3CE
Other Graphics Reg	RW			3CF
Attribute Controller Registers:				
Index Reg	RW			3C0
Attribute Controller Data Reg	W			3C0
	R			3C1

NOTES:
1. **RO** = Read-Only, **RW** = Read/Write, **W** = Write, and **R** = Read.
2. All Register addresses are in hex.
3. ‡ = VGA Video Subsystem Enable Register 3C3 is to be implemented externally since it is not present inside the WD90C00 for Microchannel implementations.

PARADISE REGISTERS SUMMARY

REGISTERS	RW	Monochrome	Color
Paradise Register Index	RW	3CE	3CE
PR0(A) Address Offset A	RW	3CF.09	3CF.09
PR0(B) Alternate Address Offset B	RW	3CF.0A	3CF.0A
PR1 Memory Size	RW	3CF.0B	3CF.0B
PR2 Video Select	RW	3CF.0C	3CF.0C
PR3 CRT Control	RW	3CF.0D	3CF.0D
PR4 Video Control	RW	3CF.0E	3CF.0E
PR5 Unlock (PR0 - PR4) / Status	RW	3CF.0F	3CF.0F
PR10 Unlock (PR11 - PR17)	RW	3B5.29	3D5.29
PR11 EGA Switches	RW	3B5.2A	3D5.2A
PR12 Scratch Pad	RW	3B5.2B	3D5.2B
PR13 Interlace H/2 Start	RW	3B5.2C	3D5.2C
PR14 Interlace H/2 End	RW	3B5.2D	3D5.2D
PR15 Miscellaneous Control 1	RW	3B5.2E	3D5.2E
PR16 Miscellaneous Control 2	RW	3B5.2F	3D5.2F
PR17 Miscellaneous Control 3	RW	3B5.30	3D5.30
Reserved	RW	3B5.31 - 3B5.3F	3D5.31 - 3D5.3F
** CNF Configuration	HARD	-----	-----

NOTE: ALL THE PARADISE REGISTERS ARE WRITE PROTECTED. SEE THE PARADISE REGISTERS' DESCRIPTION FOR MORE DETAILS.

COMPATIBILITY REGISTERS SUMMARY

Functions	RW	MDA	CGA	AT&T	Hercules
Mode Control Reg	WO	3B8	3D8	3D8	3B8/3D8
Color Select Reg	WO	-----	3D9	3D9	-----
Status Reg	RO	3BA	3DA	3DA	3BA
Preset Light Pen Latch	WO	3B9	3DC	3DC	-----
Clear Light Pen Latch	WO	3BB	3DB	3DB	-----
AT&T / M24 Reg	WO	-----	-----	3DE	-----
Hercules Reg	WO	-----	-----	-----	3BF
+ CRTC	RW	3B0-3B7	3D0-3D7	3D0-3D7	3B0-3B7

NOTES:
1. **RO** = Read-Only, **WO** = Write-Only, **RW** = Read/Write, and **HARD** = Non-read / Non-write Hardware Port.
2. All Register addresses are in hex.
3. + = 6845 Mode Registers
4. ** = This register is loaded during power on.

VGA REGISTERS

Through out this section, all bit graphics and definitions apply to VGA mode followed by their brief description.

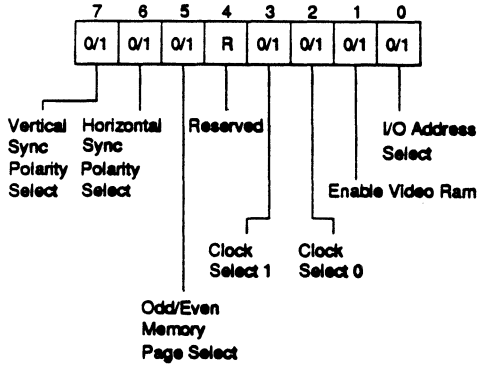
GENERAL REGISTERS

Name	Read Port	Write Port
Miscellaneous Output	3CC	3C2
Input Status Register 0	3C2	-----
Input Status Register 1	3?A	-----
Feature Control	3CA	3?A

NOTES:
1. Reserved bits should be set to zero.
2. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :

   0 = B in Monochrome Modes
   1 = D in Color Modes

MISCELLANEOUS OUTPUT REGISTER : READ PORT = 3CC WRITE PORT = 3C2



* Bit 7 Vertical Sync Polarity Selection.
  0 = Positive vertical sync polarity.
  1 = Negative vertical sync polarity.

* Bit 6 Horizontal Sync Polarity Selection.
  0 = Positive horizontal sync polarity.
  1 = Negative horizontal sync polarity.

NOTE: * These bits are determined by the monitor type. Their encoding is shown below:

Bit 7	Bit 6	Vertical Frame
0	0	Reserved
0	1	400 lines/scan
1	0	350 lines/scan
1	1	480 lines/scan

Miscellaneous Output Register contin'd

Bit 5 — Odd or Even Memory Page Select.
When in modes 0 - 5 the page size is 64KB. One memory page is selected from the two 64KB pages. This bit is used for diagnostic purposes and has no effect if PR1(7) = 1 or PR1(6) = 1.
0 = Lower page is selected.
1 = Upper page is selected.

Bit 4 — Reserved in VGA. In EGA mode, it disables the internal video drivers. Logic 0 activates internal video drivers while logic 1 deactivates video drivers in EGA designs.

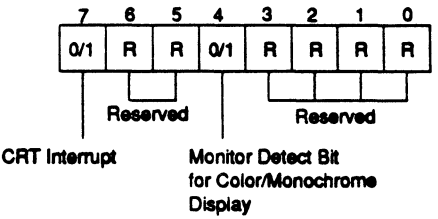
Bit 3, Bit 2 — Clock Select 1, 0.

Bit 3	Bit 2	Function
0	0	Selects VCLK0 for VGA applications. Can be connected to allow 640 dots/line (25.175MHZ).
0	1	Selects VCLK1 for VGA applications. Can be connected to allow 720 dots/line (28.322 MHZ) if Configuration Register bit 3 = 0.
1	0	Selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.
1	1	Reserved. Also selects VCLK2 (external user defined input) if Configuration Register bit 3 = 0.

Bit 1 — System Processor Video RAM Access Enable.
0 = CPU access disabled.
1 = CPU access enabled.

Bit 0 — CRT Controller I/O Address Range Selection.
Selection for Monochrome (3B4 and 3B5), or Color (3D4 and 3D5) mode. Bit 0 also maps Input Status Register 1 at MDA (3BA) or CGA (3DA).
0 = CRTC and status addresses for MDA mode.
1 = CRTC and status addresses for CGA mode.

INPUT STATUS REGISTER 0 : READ ONLY PORT = 3C2



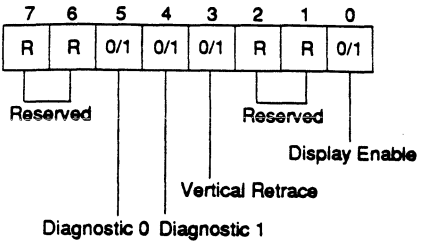
Bit 7 — CRT Vertical Retrace Interrupt Pending or Cleared.
0 = Vertical retrace interrupt cleared.
1 = Vertical retrace interrupt pending.

Bit 6, Bit 5 — Reserved in VGA.

Bit 4 — Monitor Detection in VGA mode. DA15 monitor status (pin 20) is sampled and can be read from this bit.

Bit 3-Bit 0 — Reserved.

INPUT STATUS REGISTER 1 : READ ONLY PORT = 3?A



Bit 7 Reserved.

Bit 6 Reserved.

Bit 5, Bit 4 Color Plane Diagnostics.
These bits allow the processor to set two out of eight colors by activating the Attribute Controller's Color Plane Enable Register bits 4 and 5. Their status is defined below:

Color Plane Enable Register		Input Status Register 1	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	P2	P0
0	1	P5	P4
1	0	P3	P1
1	1	P7	P6

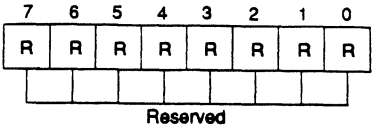
Bit 3 Vertical Retrace Status.
0 = Vertical frame is displayed.
1 = Vertical retrace is active.

Bit 2 Reserved.

Bit 1 Reserved.

Bit 0 Display Enable Status.
0 = CRT screen display in process.
1 = CRT screen display disabled for horizontal or vertical retrace interval.

FEATURE CONTROL REGISTER READ PORT = 3CA WRITE PORT = 3?A



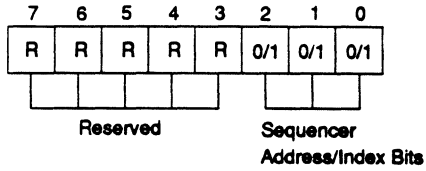
Bit 7 - Bit 0 Reserved.

SEQUENCER REGISTERS

Name	Port (hex)	Index (hex)
Sequencer Index	3C4	---
Reset	3C5	00
Clocking Mode	3C5	01
Map Mask	3C5	02
Character Map Select	3C5	03
Memory Mode	3C5	04

NOTE: 1. Reserved bits should be set to zero.

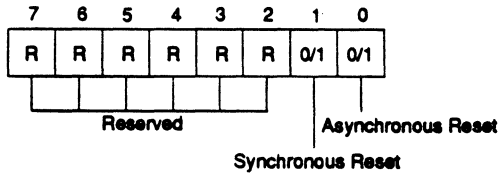
SEQUENCER INDEX REGISTER - READ/WRITE PORT = 3C4



Bit 7 - Bit 3 Reserved.

Bit 2 - Bit 0 Sequencer Address/Index.
The Sequencer Address Register is written with the index value (00H-04H) of the Seqencer register to be accessed.

RESET REGISTER - READ/WRITE PORT = 3C5 AND INDEX REGISTER = 00

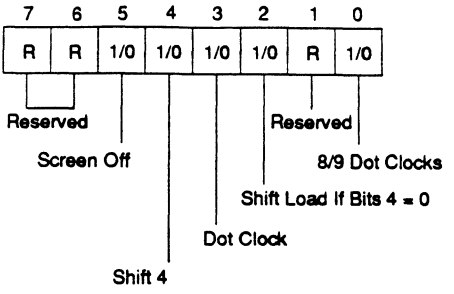


Bit 7 - Bit 2 Reserved.

Bit 1 Synchronous Reset.
0 = Sequencer is cleared and halted synchronously.
1= Operational mode (Bit 0 = 1).

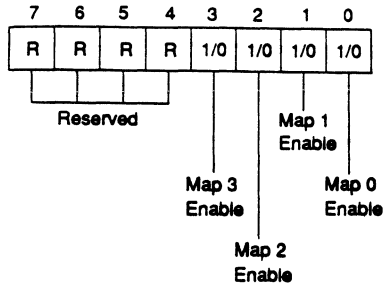
Bit 0 Asynchronous Reset.
0 = Sequencer is cleared and halted asynchronously.
1 = Operational mode (Bit 1 = 1).

CLOCKING MODE REGISTER - READ/WRITE PORT 3C5 AND INDEX REGISTER = 01



Bit 7, Bit 6	Reserved.
Bit 5	Screen Off. 0 = Normal screen operation. 1 = Screen turned off. SYNC signals are active and this bit may be used for quick full screen updates.
Bit 4	Video Serial Shift Register Loading. 0 = Serial shift registers loaded every character clock. 1 = Serial shift registers loaded every 4th character clock (32 bit fetches).
Bit 3	Dot Clock Selection 0 = Normal dot clock selected by VCLK0 input frequency (640 pixels). 1 = Dot Clock divided by 2 (320/360 pixels).
Bit 2	Shift Load. 0 = If bit 4 of this register also equals 0, then video serializers will be loaded every character clock. 1 = Video serializers are loaded every other character clock.
Bit 1	Reserved.
Bit 0	8/9 Dot Clock. Commands Sequencer to generate 8 or 9 dot wide character clock. 0 = 9 dot wide character clock. 1 = 8 dot wide character clock.

MAP MASK REGISTER - READ/WRITE PORT = 3C5 AND INDEX REGISTER = 02

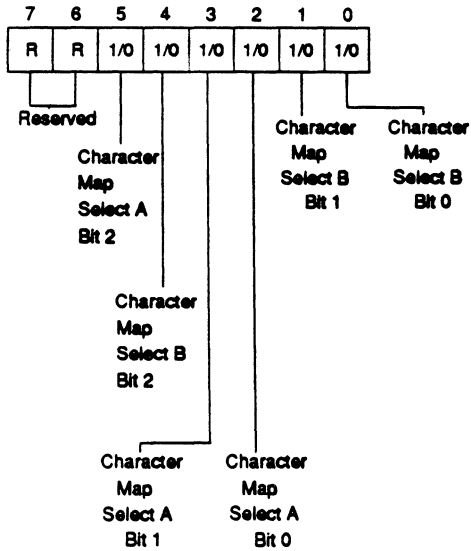


Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Controls Writing To Memory Maps (0 - 3).
0 = Writing to maps (0 - 3) disallowed.
1 = Maps (0 - 3) accessible.

CHARACTER MAP SELECT REGISTER

READ/WRITE PORT 3C5 AND INDEX REGISTER = 03



Character Map Select Register contin'd

Bit 7, Bit 6 Reserved.

Bit 5 Character Map A MSB Select.
The Most Significant Bit (MSB) of character map A is defined by bits 3 and 2, containing the character font table shown below:

Bits 5	3	2	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 4 Character Map B MSB Select.
MSB of character map B is defined by bits 1 and 0, containing the font table described below:

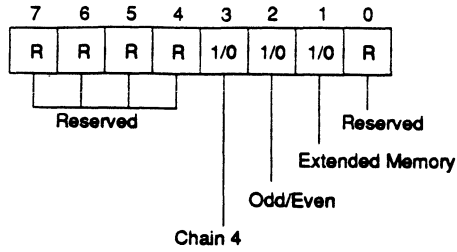
Bits 4	1	0	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	0	1st 8KB
0	0	1	1	3rd 8KB
0	1	0	2	5th 8KB
0	1	1	3	7th 8KB
1	0	0	4	2nd 8KB
1	0	1	5	4th 8KB
1	1	0	6	6th 8KB
1	1	1	7	8th 8KB

Bit 3, Bit 2 Characer Map Select A.
Refer to bit 5 table.

Bit 1, Bit 0 Character Map Select B.
Refer to bit 4 table.

NOTE: 1. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code.

MEMORY MODE REGISTER - READ/WRITE PORT = 3C5 AND INDEX REGISTER = 04



Bit 7 - Bit 4 Reserved.

Bit 3 Chains 4 Maps.
0 = Processor sequentially accesses data using map mask register.
1 = Directs the two lower order video memory address pins (MA0, MA1) to select the map to be addressed. The map selection table is shown below:

MA1	MA0	Map Enabled
0	0	0
0	1	1
1	0	2
1	1	3

Bit 2 Odd/Even Map Selection.
0 = Even processor addresses to access maps 0 and 2. Odd processor addresses to access maps 1 and 3.
1 = Sequential processor access as defined by map mask register.

Bit 1 Extended Video Memory.
0 = 64 KB of video memory.
1 = Greater than 64KB of memory for VGA/EGA modes.

Bit 0 Reserved.

CRT CONTROLLER REGISTERS

VGA Register Name	*6845 Register Name	Port (hex)	Index (hex)
CRT Controller Address Register	CRT Controller Address Register	3?4	---
Horizontal Total	†-----	3?5	00
Horizontal Display Enable End	†-----	3?5	01
Start Horizontal Blanking	†-----	3?5	02
End Horizontal Blanking	†-----	3?5	03
Start Horizontal Retrace Pulse	†-----	3?5	04
End Horizontal Retrace	†-----	3?5	05
Vertical Total	Vertical Displayed	3?5	06
Overflow	†-----	3?5	07
Preset Row Scan	†-----	3?5	08
Maximum Scan Line/Others	Maximum Scan Line Address	3?5	09
Cursor Start	Cursor Start	3?5	0A
Cursor End	Cursor End	3?5	0B
Start Address High	Start Address High	3?5	0C
Start Address Low	Start Address Low	3?5	0D
Cursor Location High	Cursor Location High	3?5	0E
Cursor Location Low	Cursor Location Low	3?5	0F
Vertical Retrace Start	Light Pen High	3?5	10
Vertical Retrace End	Light Pen Low	3?5	11
Vertical Display Enable End	†	3?5	12
Offset	†	3?5	13
Underline Location	†	3?5	14
Start Vertical Blank	†	3?5	15
End Vertical Blank	†	3?5	16
CRTC Mode Control	†	3?5	17
Line Compare	†	3?5	18

NOTES :

1. " ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :

   0 = B in Monochrome Modes and
   1 = D in Color Modes

2. "*" 6845 Mode Registers are defined and explained in greater detail in the reference literature.

3. "†" This register can be programmed in VGA mode only. It is not applicable in 6845 mode.

4. Reserved bits should be set to zero.

CRT CONTROLLER REGISTERS DESCRIPTION

CRT Address Register (Port = 3?4)

Bit 7 - Bit 5 Reserved.

Bit 4 - Bit 0 Index Register Bits.
CRT Controller index pointer bits to specify the register to be addressed. Its value is programmed hex.

†Horizontal Total Register (Port = 3?5, Index = 00H)

Bit 7 - Bit 0 Count Plus Retrace Less 5.
In VGA mode, the total character count is the total number of characters including retrace time less 5, per horizontal scan line.

†Horizontal Display Enable End Register (Port = 3?5, Index = 01H)

Bit 7 - Bit 0 Displayed Characters Less 1.
Program count of the displayed number of characters less 1 in VGA mode.

†Start Horizontal Blanking (Port = 3?5, Index = 02H)

Bit 7 - Bit 0 Character Clock Value.
Horizontal blanking begins when the horizontal character counter reaches this character clock value.

†End Horizontal Blanking (Port = 3?5, Index = 03H)

Bit 7 Reserved.

Bit 6, Bit 5 Display Enable Signal Skew Time.
They define the display enable signal skew time in relation to horizontal synchronization pulses. The skew table is shown below:

Bit 6	Bit 5	Skew in Character Clocks
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Blank Signal Width.
End horizontal blank signal width "W" is determined as the value of start blanking register plus "W" in character clocks. The least significant five bits are programmed in this register, while the sixth bit is the Retrace Register (index 05H) programmed as bit 7 of the End Horizontal Register.

NOTE: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

CRT Controller Registers Description Contin'd

†Start Horizontal Retrace Pulse Register (Port = 3?5, Index = 04H)

Bit 7 - Bit 0 Horizontal Retrace Character Count.
Hex value in character count at which horizontal retrace output pulse becomes active.

†End Horizontal Retrace Register (Port = 3?5, Index = 05H)

Bit 7 MSB (Sixth Bit) Of End Horizontal Blanking Register.

Bit 6, Bit 5 Horizontal Retrace Delay.
These bits define horizontal retrace signal delay. See the following table for details:

Bit 6	Bit 5	Character Clock Delay
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 End Horizontal Retrace Pulse Width "W".
Start retrace register value is added to the character count for width "W". The least significant five bits are programmed in this register. When the Start Horizontal Retrace Register value matches these five bits, the horizontal retrace signal is turned off.

‡Vertical Total Register (Port = 3?5, Index = 06H)

Bit 7 - Bit 0 Raster Scan Line Total Less 2.
The least significant eight bits of a ten bit count of raster scan lines for a display frame. The loaded value includes vertical total scan lines minus 2. Time for vertical retrace, and vertical sync is also included. The ninth and tenth bits of this count are loaded into the Vertical Overflow Register (index = 07H) bit 0 and bit 5 respectively. In 6845 modes, total vertical display time in rows is programmed into bit 6 - bit 0, while bit 7 is reserved. Scan count reduction is not necessary. (The number of scan lines in a row is determined by the Maximum Scan Line Register (index 09H) bits 0 thru 4).

Overflow Vertical Register (Port = 3?5, Index = 07H)

‡Bit 7 Vertical Retrace Start Bit 9 (index = 10H).

**Bit 6 Vertical Display Enable End Bit 9 (index = 12H).

‡Bit 5 Vertical Total Bit 9 (index = 06H).

Bit 4 Line Compare Bit 8 (index = 18H).

‡Bit 3 Start Vertical Blank Bit 8 (index = 15H).

‡Bit 2 Vertical Retrace Start Bit 8 (index = 10H).

**Bit 1 Vertical Display Enable End Bit 8 (index = 12H).

‡Bit 0 Vertical Total Bit 8 (index = 06H).

NOTES: † This register is locked if the Paradise Register PR3(5) = 1 OR the Vertical Retrace End Register bit 7 = 1.

** This register is locked if the Paradise Register PR3(1) = 0 AND the Vertical Retrace End Register bit 7 = 1.

‡ This register is locked if the Paradise Register PR3(0) = 1 OR the Vertical Retrace End Register bit 7 = 1.

CRT Controller Registers Description Contin'd

Preset Row Scan Register (Port = 3?5, Index = 08H)

Bit 7 Reserved.

Bit 6, Bit 5 Byte Panning Control.
These bits allow up to 3 bytes to be panned in modes programmed as multiple shift modes.

Bit 6	Bit 5	Operation
0	0	Normal
0	1	1 byte left shift
1	0	2 bytes left shift
1	1	3 bytes left shift

Bit 4 - Bit 0 Preset Row Scan Count.
These bits preset the vertical row scan counter once after each vertical retrace. This counter is incremented after each horizontal retrace period, until the maximum row scan count is reached. When maximum row scan count is reached, the counter is cleared. This register can be used for smooth vertical scroll of text.

Maximum Scan Line Register/ (Port = 3?5, Index = 09H)

Bit 7 200 To 400 Line Conversion.
0 = Normal operation.
1 = Activate line doubling. The row scan counter is clocked at half the horizontal scan rate to allow 200 line modes to display 400 scan lines (each line is double scanned).

Bit 6 Line Compare.
This is bit 9 of the Line Compare Register (index = 18H).

§ Bit 5 Start Vertical Blank.
This is bit 9 of the Start Vertical Blank Register (index = 15H).

Bit 4 - Bit 0 Maximum Scan Line.
Maximum number of scanned lines for each row of characters. The value programmed is the maximum number of scanned rows per character minus 1. In 6845 mode, bits 5-7 are reserved, and bits 4-0 are programmed with the maximum scan line count less 1 for non-interlace mode. Interlaced mode is not supported.

Cursor Start Register (Port = 3?5, Index = 0AH)

Bit 7, Bit 6 Reserved.

Bit 5 Cursor Control.
0 = Cursor on.
1 = Cursor off.

Bit 4 - Bit 0 These bits specify the row scan counter value within the character box where the cursor begins. These bits contain the value of the character row less 1. If this value is programmed with a value greater than the Cursor End Register (index = 0BH), no cursor is generated. For 6845 modes, bit 7 is reserved. Bit 5 controls the cursor operation and bits 4-0 contain the cursor start value. Bit 6 is not used.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT Controller Registers Description Contin'd

Cursor End Register (Port = 3?5, Index = 0BH)

Bit 7 Reserved.

Bit 6, Bit 5 Cursor Skew Bits.
Delays the displayed cursor to the right by the skew value in character clocks e.g., 1 character clock skew moves the cursor right by 1 position on the screen. Refer to the table below:

Bit 6	Bit 5	Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bit 4 - Bit 0 These bits specify the last row scan counter value within the character box during which the cursor is active. If this value is less than the cursor start value, no cursor is displayed. In 6845 mode, bits 7-5 are reserved and bits 4-0 contain row value of the cursor end.
NOTE: There are three types of cursors generated, depending upon the mode i.e., EGA, VGA, or 6845 (non-VGA). The above description refers to the VGA cursor only.

Start Address High Register (Port 3?5H, Index = 0CH)

Bit 7 - Bit 0 Display Screen Start Address Upper Byte Bits.
Eight high order bits of the 16 bit video memory address, used for screen refresh. The low order eight bit register is at index 0DH. The Paradise Register PR3 bits 3 and 4 extend this video memory start register to 18 bits. In 6845 modes bits 6 and 7 are forced to 0 regardless of this register's contents, while the lower order 8 bits are at index register 0DH.

Start Address Low Register (Port = 3?5H, Index = 0DH)

Bit 7 - Bit 0 Display Screen Start Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

Cursor Location High Register (Port = 3?5, Index = 0EH)

Bit 7 - Bit 0 Cursor Address Upper Byte Bits.
The eight higher order bits of 16 bit cursor location in VGA mode. For the lower order eight bits, see the Cursor Location Low Register at index 0F. In VGA mode, the Paradise Register PR3 bits 3 and 4 extend the Cursor Location High Register to 18 bits. For 6845 modes, bits 6 and 7 are reserved, while bits 5 - 0 are the high order bits of the cursor.

Cursor Location Low Register (Port = 3?5, Index = 0FH)

Bit 7 - Bit 0 Cursor Address Lower Byte Bits.
The lower order eight bits of the 16 bit video memory address in VGA or 6845 modes.

CRT Controller Registers Description Contin'd

§Vertical Retrace Start Register (Port = 3?5, Index = 10H)

Bit 7 - Bit 0 Vertical Retrace Start Pulse Lower Eight Bits.
The lower eight bits of the ten bit vertical retrace start register. Bits 8 and 9 are located in the Overflow Register (index = 07H). In 6845 compatible mode, this register shows the high order six bits in positions 5-0 as the **light pen** read back value, and bits 6 and 7 are reserved. The lower order eight bits of the **light pen** read back register are at index 11H. In EGA compatible mode this register shows the high order eight bits as the light pen value.

§Vertical Retrace End Register (Port = 3?5, Index = 11H)

Bit 7 CRTC Registers Write Protect.
0 = Enables writes to CRT index registers 00H-07H.
1 = Write protects CRT Controller index registers in the range of 00H-07H. The line compare bit 4 in the Overflow Register (07H) is not protected.

Bit 6 DRAM Refresh /Horizontal Scan Line.
Selects 5 DRAM refresh cycles per horizontal scan line.
0 = Generates 3 refresh cycles for each horizontal scan line for normal VGA operation.
1 = Generates 5 DRAM refresh cycles per horizontal scan lines for 15.75 KHZ display monitors.

Bit 5 Enable Vertical Retrace Interrupt.
0 = Enables vertical retrace interrupt.
1 = Disable vertical retrace interrupt.

Bit 4 Clear Vertical Retrace Interrupt.
0 = Clears vertical retrace interrupt by resetting (writing a 0 to) an internal flip-flop.
1 = Vertical retrace interrupt. Allows an interrupt to be generated after the last displayed scan line of the frame has occured (i.e., the start of the bottom border).

Bit 3 - Bit 0 Vertical Retrace End.
They specify scan count at which vertical sync becomes inactive. For retrace signal pulse width "W", add scan count for "W" to the value of the Vertical Retrace Start Register. The 4 bit result is written in the Vertical Retrace End Register. In 6845 or EGA compatible mode, this register allows the read back value of the lower eight bits of the **Light Pen Register**.

Vertical Display Enable End Register (Port = 3?5, Index = 12H)

Bit 7 - Bit 0 Vertical Display Enable End Lower Eight Bits. .
The eight lower bits of ten bit register that defines where the active display frame ends. The programmed count is in scan lines minus 1. Bits 8 and 9 are in the Overflow Register (index 07H) at positions 1 and 6, respectively.

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT Controller Registers Description Contin'd

Offset Register (Port = 3?5, Index = 13H)

Bit 7 - Bit 0 Logical Line Screen Width.
This register specifies the width of display memory in terms of an offset from the current row start address to the next character row. The offset value is a word address adjusted for word or double word display memory access. It is calculated as follows:

Next Row Scan Start Address = Current Row Scan Start Address + (K * value in Offset Register), where K = 2 in byte mode and K = 4 in word mode.

Underline Location Register (Port = 3?5, Index = 14H)

Bit 7 Reserved.

Bit 6 Doubleword Mode.
0 = Display memory addressed for byte or word access.
1 = Display memory addressed for double word access.

Bit 5 Count By 4 For Double word Access
0 = Memory address counter clocked for byte or word access.
1 = Memory address counter is clocked at the character clock rate divided by 4.

Bit 4 - Bit 0 Underline Location.
These bits specify the row scan counter value within a character matrix where underline is to be displayed. Load a value 1 less than the desired scan line number.

§Start Vertical Blank Register (Port = 3?5, Index = 15H).

Bit 7 - Bit 0 Start Vertical Blank Lower Eight Bits.
The lower eight bits of the ten bit Start Vertical Blank Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). The ten bit value is reduced by 1 from the desired scan line count where the vertical blanking signal starts.

§End Vertical Blank Register (Port = 3?5, Index = 16H)

Bit 7 - Bit 0 Vertical Blank Inactive Count.
End Vertical Blank is an 8 bit value calculated as follows:

8 Bit End Vertical Blank value =
(value of Start Vertical Blank minus 1) + (value of Vertical Blank signal in scan lines).

NOTE: § This register is locked if the Paradise Register PR3(0) = 1.

CRT Controller Registers Description Contin'd

CRT Mode Control Register (Port = 3?5, Index = 17H)
This register is locked if Paradise Register PR3(5) = 1.

Bit 7 Hardware Reset.
0 = Horizontal and vertical retrace outputs to be inactive.
1 = Horizontal and vertical retrace outputs enabled.

Bit 6 Word Or Byte Mode.
0 = Word address mode. All memory address counter bits shift down by 1 bit and the MSB of the address counter appears on the LSB. See the table below.
1 = Byte address mode.

Memory Address	Byte Address Mode	Word Address Mode	Doubleword Address Mode
MA0/RF0	MA0	* MA15 or MA13	MA12
MA1/RF1	1	0	MA13
MA2/RF2	2	1	0
MA3/RF3	3	2	1
MA4/RF4	4	3	2
MA5/RF5	5	4	3
MA6/RF6	6	5	4
MA7/RF7	7	6	5
MA8/RF8	8	7	6
MA9	9	8	7
MA10	10	9	8
MA11	11	10	9
MA12	12	11	10
MA13	13	12	11
MA14	14	13	12
MA15	15	14	13

NOTE: * See bit 5, defining address wrap. This table is only applicable when Paradise Register PR1 bits 7 and 6 equal zero, or PR16 bit 1 equals one.

The CRT Underline Location Register (index = 14H) bit 6 also controls addressing. However, when CRT14H(6) = 0, only the CRT Mode Control Register (index 17H) bit 6 controls addressing. See the table below:

CRT14H Bit 6	CRT17H Bit 6	Address Mode
0	0	Word
0	1	Byte
1	X	Doubleword

Bit 5 Address Wrap.
0 = In word address mode, this bit enables bit 13 or bit 15 to appear at MA0, otherwise bit 0 appears on MA0.
1 = Select MA15 for odd/even mode when 256KB of video memory is used on the system board. Bit MA13 is used in applications which do not use system board memory for CGA compatibility.

Bit 4 Reserved.

Bit 3 Count by 2
0 = Character clock increments memory address counter.
1= Character clock divided by 2 increments the address counter.

CRT Controller Registers Description Contin'd

CRT Mode Control Register Contin'd

Bit 2 — Horizontal Retrace Clock Rate Select For Vertical Timing Counter.
0 = Selects horizontal retrace clock rate.
1 = Selects horizontal retrace clock rate divided by 2.

Bit 1 — Select Row Scan Counter.
0 = Selects row scan counter bit 1 as output at MA14 address pin.
1 = Selects bit 14 of the CRTC address counter as output at MA14 pin.

Bit 0 — 6845 CRT Controller compatibility mode support for CGA operation.
0 = Row scan address bit 0 is substituted for memory address bit 13 at MA13 output pin during active display time.
1 = Enable memory address pin 13 to be output at MA13 address pin.

Line compare Register (Port = 3?5, Index = 18H)

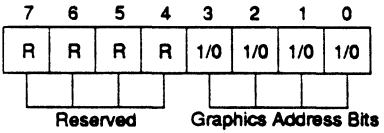
Bit 7 - Bit 0 — Line Compare Lower Eight Bits.
Lower eight bits of the ten bit Scan Line Compare Register. Bit 8 is in the Overflow Register (index = 07H) and bit 9 is in the Maximum Scan Line Register (index = 09H). When the vertical counter reaches this value, the internal start of the line counter is cleared.

GRAPHICS CONTROLLER REGISTERS

Name	Port (Hex)	Index (Hex)
Graphics Index Register	3CE	---
Set / Reset	3CF	00
Enable Set/ Reset	3CF	01
Color Compare	3CF	02
Data Rotate	3CF	03
Read Map Select	3CF	04
Graphics Mode Register	3CF	05
Miscellaneous Register	3CF	06
Color Don't Care	3CF	07
Bit Mask Register	3CF	08

NOTE: 1. Reserved bits should be set to zero.

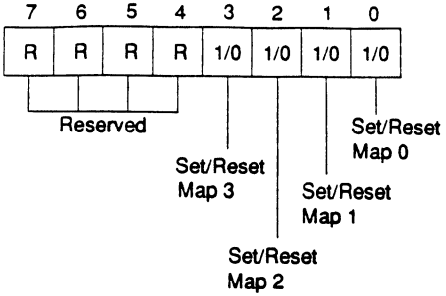
GRAPHICS INDEX REGISTER - READ/WRITE PORT = 3CE



Bit 7 - Bit 4 Reserved.

Bit 3 -Bit 0 Graphics Controller Register Index Pointer Bits.
Note that some of the Paradise registers reside with the index pointer extension beyond graphics Controller registers.

SET / RESET REGISTER - READ / WRITE PORT 3CF AND INDEX REGISTER = 00



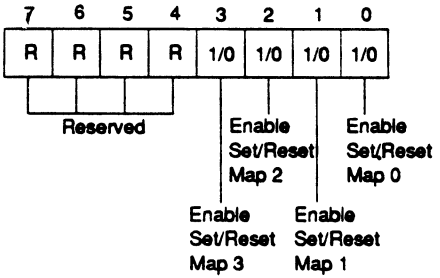
Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Set/Reset Map.
When the CPU executes display memory write with Write Mode 0* selected and the Enable Set/Reset Register (index = 01H) activated, the eight bits of the bit value in this register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. It is an eight bit fill operation. The map designations are defined below:
0 = Reset.
1 = Set.

Bit	Set/Reset
3	Map 3
2	Map 2
1	Map 1
0	Map 0

NOTE: *The selection of Write Mode 0 is determined by the Graphics Mode Register (index = 05H) bit 1 and bit 0.

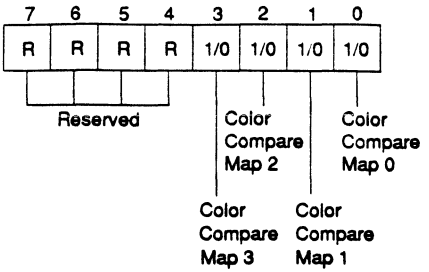
ENABLE SET / RESET REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER =01



Bit 7 - Bit 4 **Reserved.**

Bit 3 - Bit 0 Enable The Set/Reset Register (Index = 00H).
0 = When Write Mode 0 is selected, these bits, set to 0, disable the Set/Reset Register (index = 00H) memory map access and the map is written with the rotated 8-bit data value of the system microprocessor.
1 = When Write Mode 0 is selected, these bits enable memory map access defined by the Set/Reset Register (index = 00H), and the respective memory map is written with the Set/Reset Register value.

COLOR COMPARE REGISTER - READ/WRITE PORT 3CF AND INDEX REGISTER = 02

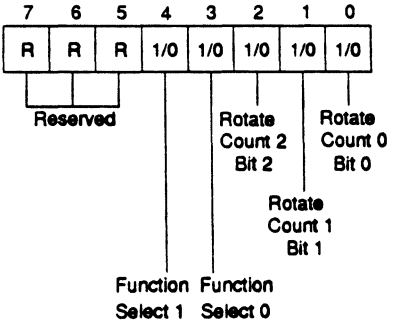


Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Color Compare.
The color compare bit contains the value to which all 8 bits of the corresponding memory map are compared. This comparison also occurs across all four maps, and a 1 is returned for the map positions where the bits of all four maps equal their corresponding color compare value.
When read mode bit 3 in the Graphics Mode Register (index = 05H) is set to 1 and the system does a memory read, a 1 will be returned for each bit where the four maps equal the Color Compare Register. If a system read is done with bit 3 = 0 for the Graphics Mode Register (index = 05H), data is returned without comparison. Color compare map coding is shown below:

Bit	Color Compare
3	Map 3
2	Map 2
1	Map 1
0	Map 0

DATA ROTATE REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER = 03



Bit 7 - Bit 5 Reserved.

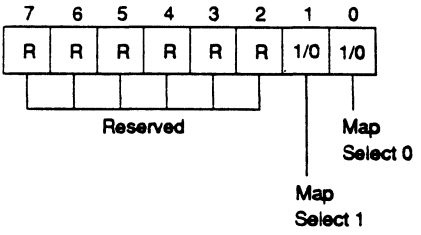
Bit 4, Bit 3 Function Select.
Function select for any of the write mode operations defined in the Graphics Mode Register (index = 05H) is defined as follows:

Data Rotate Register contin'd

Bit 4	Bit 3	Function
0	0	Video memory data unmodified
0	1	Video memory data ANDed with system data in the latches
1	0	Video memory data ORed with system data in the latches
1	1	Video memory data XORed with system data in the latches

Bit 2 - Bit 0 Rotate Count.
It specifies number of bit positions of rotation to the right. Data written by the CPU is rotated in write mode 0, defined by the Graphics Mode Register (index = 05H).

READ MAP SELECT REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER = 04

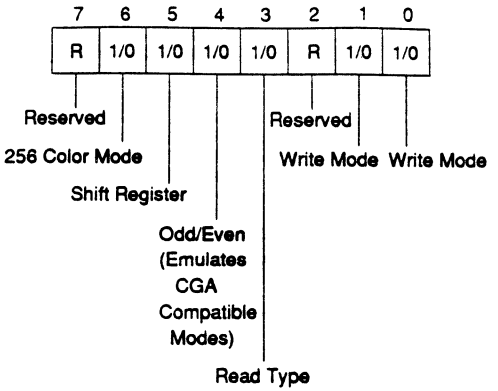


Bit 7 - Bit 2 Reserved.

Bit1, Bit 0 Map Select.
These bits select memory map in system read operations. It has no effect on color compare read mode. Map read is defined as shown under:

Bit 1	Bit 0	Read Map
0	0	0
0	1	1
1	0	2
1	1	3

GRAPHICS MODE REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER = 05



Bit 7 Reserved.

Bit 6 256 Color Mode.
0 = Enables bit 5 of this register to control loading of the shift registers. Four bit pixel is expanded to six bits through internal palette and is sent out on the lower six bits (VID5 - VID0) pins every dot clock. The remaining two video outputs (VID6, VID7) are determined by bits 2 and 3 of the Color Select Register located at index = 14H within the Attribute Controller.
1 = Load video shift registers to support 256 color mode.

Bit 5 Shift Register.
Shift register load controls the way in which memory data is formatted in the four video shift registers. MSB is shifted out in all cases.
0 = Map 0 - Map 3 data is placed into shift registers for normal operations.
1 = For CGA graphics mode compatibility, even numbered bits from all the maps are shifted out of the even numbered shift registers, and odd numbered bits from all the maps are shifted out of odd numbered shift registers.

Bit 4 Odd/Even Mode.
0 = normal
1 = CGA compatible odd/even system access mode. Sequential addressing as defined by bit 2 of the memory mode register (index = 04H) in the Sequencer Register. Even system addresses access maps 0 or 2 and odd system addresses access maps 1 or 3.

Bit 3 Read Mode.
0 = System reads data from memory maps selected by Read Map Select Register (index 04H). This setting will have no effect if bit 3 of the Sequencer Memory Mode Register = 1.
1 = System reads the comparison of the memory maps and the Color Compare Register.

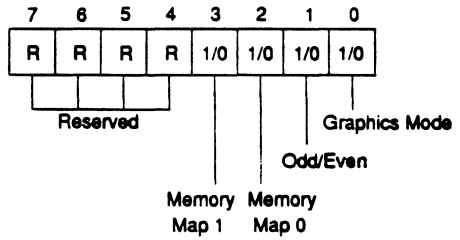
Bit 2 Reserved.

Graphics Mode Register Contin'd

Bit 1, Bit 0 Write Mode.
The following table defines the four write modes.

Bit 0	Bit 1	Write Mode
0	0	Write Mode 0. If the Set/Reset Register function is enabled for any of the maps, the eight bits of the bit value in the Set/Reset Register, which have been operated on by the Bit Mask Register, are then written to the corresponding display memory map. If the Set/Reset Register function is disabled, the map is written with the CPU data which is right rotated by the number of bits defined in the Data Rotate Register, with the old LSB now the new MSB.
0	1	Write Mode 1. This mode can be used to write the same value to many memory locations. The 32 bits of data in the system latches are written into each of the four memory maps. The system read operation loads the latches.
1	0	Write Mode 2. Memory maps (3 : 0) are filled with the 8-bit value of the corresponding CPU data bits (3 : 0). The 32 bit output of the four memory maps is operated on by the Bit Mask Register and the resulting data is written to the four memory maps.
1	1	Write Mode 3. Eight bits of the value contained in the Set/Reset Register (index = 00H) is written into the corresponding map, regardless of the Enable Set/Reset Register (index = 01H). The right rotated CPU data (see Write Mode 0) is ANDed with Bit Mask Register data to form an 8-bit mask value that performs the same function as the Bit Mask Register in Write Modes 0 and 2.

MISCELLANEOUS REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER = 06



Bit 7 - Bit 4 Reserved.

Miscellaneous Register Contin'd

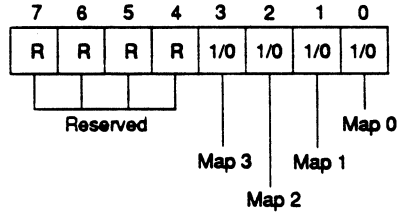
Bit3, Bit 2 Memory Map 1, 0
Display memory map control into the CPU address space is shown below:

Bit 3	Bit 2	CPU Address Range	Length
0	0	A0000 - BFFFFH	128KB
0	1	A0000 - AFFFFH	64KB
1	0	B0000 - B7FFFH	32KB
1	1	B8000 - BFFFFH	32KB

Bit 1 Odd/Even Mode.
0 = CPU address bit A0 is the memory address bit MA0.
1 = CPU address bit A0 is replaced by higher order address bit. A0 is then used to select odd or even maps. A0 = 0 selects map 0 or 2, while A0 = 1 selects map 1 or 3.

Bit 0 Graphics/Alphanumeric Mode
This bit is programmed the same way as bit 0 of the Attribute Mode Control Register.
0 = Alphanumeric mode selected.
1 = Graphics mode selected.

COLOR DON'T CARE REGISTER - READ/ WRITE PORT 3CF AND INDEX REGISTER = 07



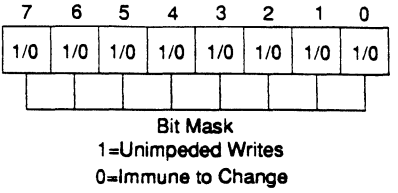
Bit 7 - Bit 4 Reserved.

Bit 3 - Bit 0 Memory Map Color Compare Operation.
Map coding is shown below:

Map #	Bit 3	Bit 2	Bit 1	Bit 0
	3	2	1	0

0 = Disable color compare operation.
1 = Enable color compare operation.

BIT MASK REGISTER - READ/WRITE PORT = 3CF AND INDEX REGISTER = 08



Bit 7 - Bit 0 Bit mask.
Bit mask operation applies simultaneously to all the four maps. In Write Modes 0 and 2, this register provides selective changes to any bit stored in the system latches during processor writes. Data must be first latched by reading the addressed byte. After setting the Bit Mask Register, new data is written to the same byte in a subsequent operation. Bit mask operation is applicable to any data written by the processor.
0 = Bit position value is masked or is not changeable.
1 = Bit position value is unmasked and can be changed in the corresponding map.

AT TRIBUTE CONTROLLER REGISTERS

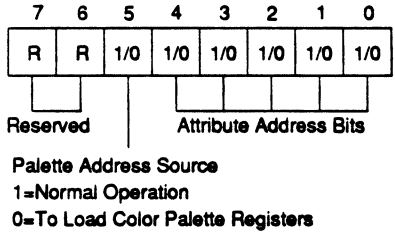
Name	Port (Hex)	Index (Hex)
Index Register	3C0	---
Palette Registers	3C0	00---0F
Attribute Mode Control Register	3C0	10
Overscan Control Register	3C0	11
Color Plane Enable Register	3C0	12
Horizontal PEL Panning Register	3C0	13
Color Select Register	3C0	14

NOTES:

1. Each attribute data register is written at 3C0 and register data is read from address 3C1.
2. Reserved bits should be set to zero.
3. ? " Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below :

   0 = B in Monochrome Modes and
   1 = D in Color Modes

ATTRIBUTE INDEX REGISTER - READ/WRITE PORT = 3C0



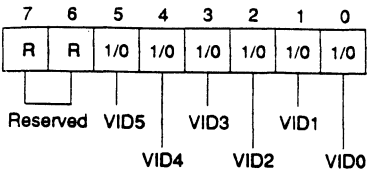
Bit 7 , Bit 6 Reserved.

Bit 5 Palette Address Source.
0 = Disable internal color palette outputs and video outputs to allow CPU access to color palette registers (index 00 - 0FH).
1 = Enable internal color palette and normal video translation.

Bit 4 - Bit 0 Attribute Controller Index Register Address Bits.

NOTE: The Attribute Index Register has an internal flip-flop, rather than an input bit, which controls the selection of the Address and Data Registers. Reading the Input Status Register 1 (port = 3?A) clears the flip-flop and selects the Address Register, which is read thru address 3C1 and written at address 3C0. Once the Address Register has been loaded with an index, the next write operation to 3C0 will load the Data Register. The flip-flop toggles between the Address and the Data Registers after every write to address hex 3C0, but does not toggle for reads to address 3C1.

PALETTE REGISTERS (00-0F Hex) - READ PORT 3C1/WRITE PORT 3C0



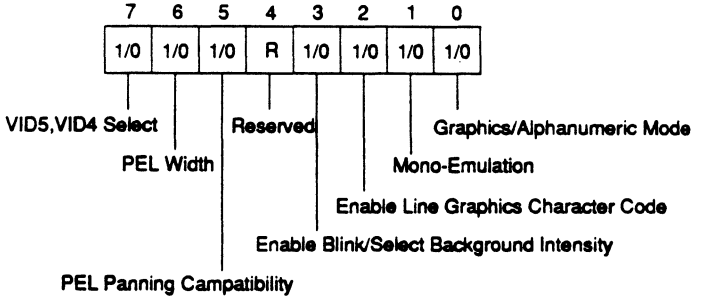
Bit 7, Bit 6 Reserved.

Bit 5 - Bit 0 Palette Pixel Colors.
They are defined as follows:
0 = Current pixel color deselected.
1 = Enable corresponding pixel color per the table below:

Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

ATTRIBUTE MODE CONTROL REGISTER

READ PORT 3C1/WRITE PORT 3C0 AND INDEX REGISTER = 10



Bit 7 VID5, VID4 Select.
0 = VID5 and VID4 palette register outputs are selected.
1 = Color Select Register (index 14H) bits 1 and 0 are selected for outputs at VID5 and VID4 pins.

Bit 6 Pixel Width.
0 = Disable 256 color mode pixel width. The PCLK output is the same as the internal dot clock rate.
1 = Enable pixel width for 256 color mode. The PCLK output is the internal dot clock divided by two.

Attribute Mode Control Register Contin'd

Bit 5 PEL Panning Compatibility.
Line Compare in the CRT Controller.
0 = A Line compare will have no effect on the PEL Panning Register.
1 = Allows a successful line compare to disable the PEL Panning Register and also bits 5 and 6 of the CRT Controller Register 08 until VSYNC occurs. Allows pixel panning of a selected portion of the screen.

Bit 4 Reserved.

Bit 3 Back Ground Intensity/Blink Selection.
0 = Selects background intensity from the MSB of the attribute byte.
1 = Selects blink attribute.

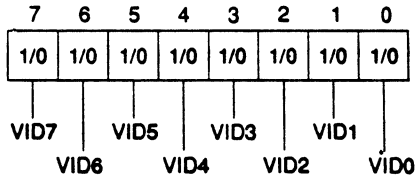
Bit 2 Enable Line Graphics Character Code.
Set this bit to zero for character fonts that do not utilize line graphics character codes.
0 = Forces ninth dot to be the same color as background in line graphics character codes.
1 = Used in MDA line graphics modes. The ninth dot character is forced to be identical to the eighth character dot.

Bit 1 Mono/Color Emulation.
0 = Color display attributes.
1 = MDA attributes.

Bit 0 Graphics/Alphanumeric Mode Enable.
0 = Alphanumeric mode.
1 = Graphics mode.

OVERSCAN COLOR REGISTER

READ PORT 3C1/WRITE PORT 3C0 AND INDEX REGISTER = 11

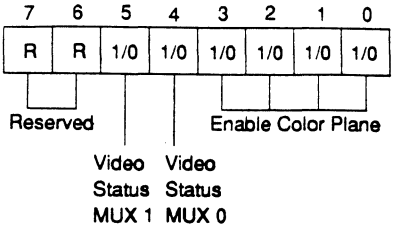


Bit 7 - Bit 0 **Overscan/Border Color.**
They determine the overscan or border color. For monochrome display, this register is set to 0. Border colors are set as shown below:

Bit 7	VID7
Bit 6	VID6
Bit 5	VID5
Bit 4	VID4
Bit 3	VID3
Bit 2	VID2
Bit 1	VID1
Bit 0	VID0

COLOR PLANE ENABLE REGISTER

READ PORT 3C1/WRITE PORT 3C0 AND INDEX REGISTER = 12



Bit7, Bit 6 Reserved.

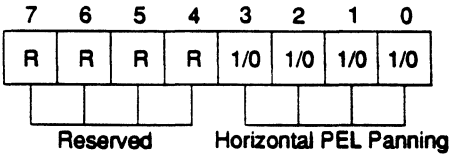
Bit 5, Bit 4 Video Status Control.
These bits select 2 out of 8 color outputs which can be read by the Input Status Register 1 (port = 03?A) bits 4 and 5.

Color Plane		Input Status Register	
Bit 5	Bit 4	Bit 5	Bit 4
0	0	VID2	VID0
0	1	VID5	VID4
1	0	VID3	VID1
1	1	VID7	VID6

Bit 3 - Bit 0 Color Plane Enable.
0 = Disables respective color planes.
1 = Enables the respective display memory color plane.

HORIZONTAL PEL PANNING REGISTER

READ PORT 3C1/WRITE PORT 3C0 AND INDEX REGISTER = 13



Bit 7 - Bit 4 Reserved.

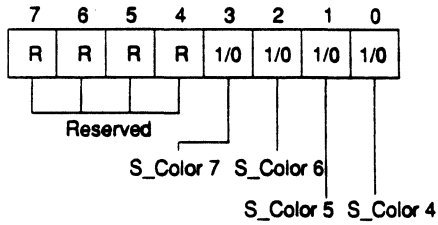
Bit 3 - Bit 0 Horizontal Pixel Panning.
It is available in text or graphics modes. These bits select pixel shift to the left horizontally. For 9 dots/character modes, up to 8 pixels can be shifted horizontally to the left. Likewise, for 8 dots/character up to 7 pixels can be shifted horizontally to the left. For 256 color, up to 3 position pixel shift can occur. The following table defines the shift in different modes:

Horizontal Pel Panning Register contin'd

	Left Shift Pixel Value		
Register Value	9 Dots/Character	8 Dots/Character	256 color Mode
0	1	0	0
1	2	1	-
2	3	2	1
3	4	3	-
4	5	4	2
5	6	5	-
6	7	6	3
7	8	7	-
8	0	-	-

COLOR SELECT REGISTER

READ PORT 3C1/WRITE PORT 3C0 AND INDEX REGISTER = 14



Bit 7 - Bit 4 Reserved.

Bit 3, Bit 2 Color Value MSB.
Two most significant bits of the eight digit color value for the video DAC. They are normally used in all modes except 256 color graphics.
Bit 3 = Set color bit VID7.
Bit 2 = Set color bit VID6.

Bit 1, Bit 0 Substituted Color Value Bits.
These bits can be substituted for VID5 and VID4 output by the Attribute Controller palette registers, to create eight bit color value. They are selected by the Attribute Controller Mode Control Register (index = 10H).

COMPATIBILITY REGISTERS

Name	Port (Hex)
Mode Control Register	3?8
Color Select Register	3D9
Status Register	3?A
AT&T/M24 Register	3DE
Hercules Register	3BF
Preset Light Pen Latch	3B9 (Mono) & 3DC (CGA)
Clear Light Pen Latch	3?B

NOTES:

1. The Compatibility Registers are available only in 6845 mode (non-VGA), which is enabled by setting Paradise Register PR2(6) = 1.

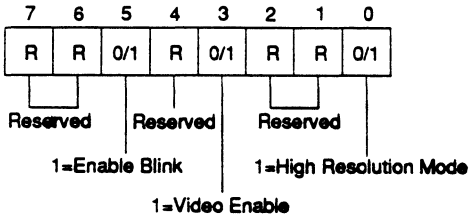
2. The AT&T/M24 Register also requires that M24 mode be enabled. This is done by setting Paradise Register PR2(7) = 1.

3. "?" Value is controlled by Bit 0 of the Miscellaneous Output Register and is programmed as shown below:

   0 = B in Monochrome Modes
   1 = D in Color Modes

MODE CONTROL REGISTER

MONOCHROME (HIGH RESOLUTION) MDA OPERATION - WRITE ONLY PORT = 3B8



Bit 7, Reserved.

Bit 6 Reserved.

Bit 5 Enable Blink.
0 = Disable blink.
1 = Enable blink.

Bit 4 Reserved.

Bit 3 Video Enable.
0 = Video disable.
1= Video activated.

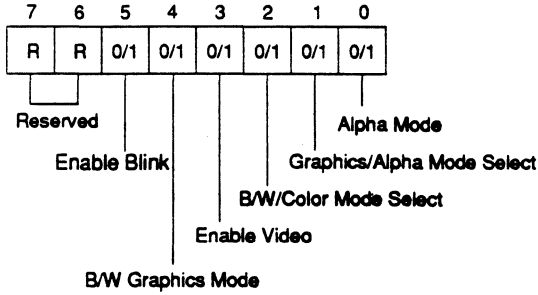
Mode Control Register contin'd

Bit 2, Reserved.

Bit 1 Reserved.

Bit 0 High Resolution Mode.
0 = High resolution disabled. This is not allowed in MDA designs.
1 = High resolution is enabled.

COLOR CGA OPERATION - WRITE ONLY PORT = 3D8



Bit 7, Bit 6 Reserved.

Bit 5 Enable Blink Function.
0 = Disables blinking function.
1 = For normal operation, set this bit to allow blinking.

Bit 4 B/W Graphics Mode Enable.
0 = Deselect 640 x 200 B/W graphics mode.
1 = Enable 640 x 200 B/W graphics mode.

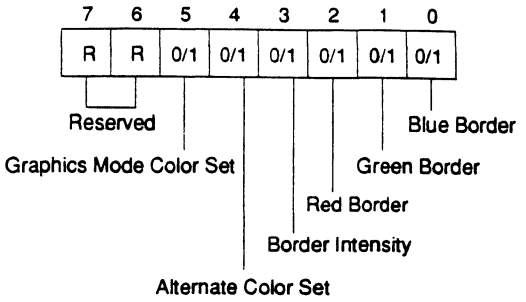
Bit 3 Activate Video Signal.
0 = Deactivates video signal. This is done during mode changes.
1 = Enable video signal.

Bit 2 B/W or Color Display Mode.
0 = Color mode selected.
1 = B/W mode enabled.

Bit 1 Text or Graphics Mode Selection.
0 = Alpha mode enabled.
1 = Graphics mode (320 x 200) activated.

Bit 0 (40 x 25) or (80 x 25) Text Mode Selection.
0 = (40 x 25) alpha mode enabled.
1 = (80 x 25) alpha mode activated.

CGA COLOR SELECT REGISTER - WRITE ONLY PORT = 3D9



Bit 7, Bit 6 Reserved.

Bit 5 320 x 200 Color Set Select.
0 = Disable 320 x 200 color mode.
1 = Color set selection for 320 x 200 color mode.

Bit 4 Alternate Color Set Enable.
0 = Background color in alpha mode.
1 = Enable alternate color set in graphics mode.

Bit 3 Border Intensity.
Border color select in text modes, and screen background color in (320 x 200) and (640 x 400) graphics mode.
Alphanumeric Mode.
1 = Selects intensified border color.
320 x 200 Graphics Mode.
1 = Selects intensified background and border color (C0-C1).
640 x 200 Graphics Mode.
1 = Selects intensified foreground color.

Bit 2 Red Border/Background.
Border color select in text modes, and screen background color in (320 x 200) and (640 x 400) graphics mode.
Alphanumeric Mode.
1 = Selects red border color.
320 x 200 Graphics Mode.
1 = Selects red background and border color (C0-C1).
640 x 200 Graphics Mode.
1 = Selects red foreground color.

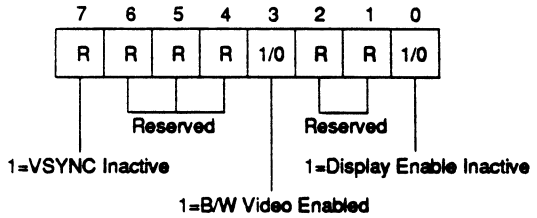
Bit 1 Green Border/Background.
Border color select in text modes, and screen background color in (320 x 200) and (640 x 400) graphics mode.
Alphanumeric Mode.
1 = Selects green border color.
320 x 200 Graphics Mode.
1 = Selects green background and border color (C0-C1).
640 x 200 Graphics Mode.
1 = Selects green foreground color.

CGA Color Select Register Contin'd

Bit 0 — Blue Border/Background.
Border color select in text modes, and screen background color in (320 x 200) and (640 x 400) graphics mode.
Alphanumeric Mode.
1 = Selects blue border color.
320 x 200 Graphics Mode.
1 = Selects blue background and border color (C0-C1).
640 x 200 Graphics Mode.
1 = Selects blue foreground color.

CRT STATUS REGISTER

MDA OPERATION - READ ONLY PORT = 3BA



Bit 7 — Vertical Retrace.
0 = Indicates the raster is in vertical retrace mode.
1 = Indicates vertical retrace is inactive (inverted VSYNC if I/O is mapped into 3BX).

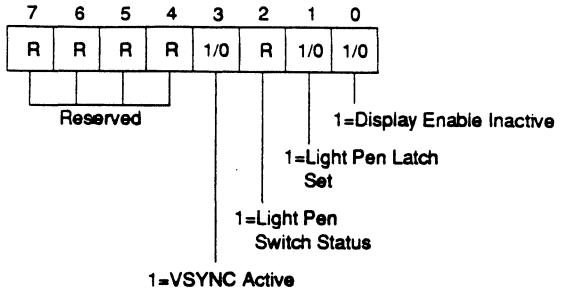
Bit 6 - Bit 4 — Reserved.

Bit 3 — B/W Video Status.
0 = B/W Video disabled.
1 = B/W video enabled.

Bit 2 - Bit 1 — Reserved.

Bit 0 — Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

CGA OPERATION - READ ONLY PORT = 3DA



Bit 7 - Bit 4 Reserved.

Bit 3 Vertical Retrace.
0 = Indicates vertical retrace is inactive.
1 = Indicates the raster is in vertical retrace mode.

Bit 2 Light Pen Switch Status

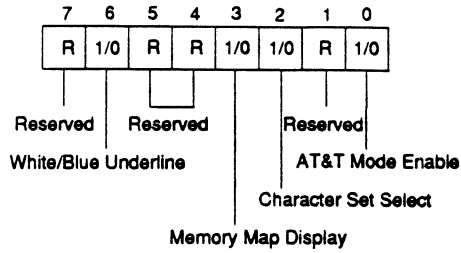
0 = Light pen switch closed
1 = Light pen switch open

Bit 1 Light Pen Latch.
0 = Light pen latch cleared.
1 = Light pen latch set.

Bit 0 Display Enable.
0 = Display Enable is active.
1 = Indicates the screen border or blanking is active; Display Enable is inactive.

AT&T / M24 REGISTER - WRITE ONLY PORT = 3DE

This is a write only, 8-bit register located at address 3DE. It is used to control the 640x400 AT&T graphics mode. All bits are set to zero by reset. This register is enabled by setting bit 7 in Paradise Register 2 (PR2).



Bit 7 Reserved.

Bit 6 White/Blue Underline.
Defines underline attribute according to the MDA display requirements.
0 = Underline attribute selects blue foreground in color text modes.
1 = Underline attribute selects white underlined foreground.

Bit 5, Bit 4 Reserved.

Bit 3 Page Select.
Selects between one or two 16KB RAM page for display in 200 line graphics mode.
0 = Display memory address starts at B8000H (16KB length).
1 = Display memory address starts at BC000H (16 KB length).

Bit 2 Character Set Select.
Selects between two character font planes.
0 = Standard character font from plane 2.
1 = Alternate character font from plane 3.

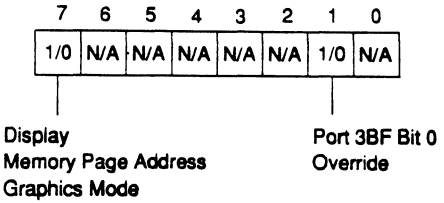
Bit 1 Reserved.

Bit 0 M24 or Non-IBM Graphics Mode.
A 400 line monitor is required for this mode.
0 = 200 line graphics mode active, using paired lines.
1 = AT&T mode enabled for 400 line graphics.

HERCULES REGISTERS

The Hercules Mode Register is a 2-bit write only register located at I/O port address 3BF. It affects the device operation only in the 6845 mode. The enable mode register located at the address 3?8 overrides the write port 3BF functions defined by its bits 0 and 1. The associated details are shown below:

ENABLE MODE REGISTER - 3?8



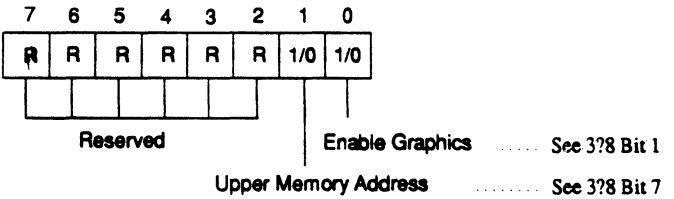
NOTE:
1.0 " ? " = " B " for Monochrome mode and "D " for Color mode.
2.0 " N/A " = Not Applicable.

Bit 7 — Display Memory Page Address In Graphics Mode.
0 = Display memory page address starts at B0000H.
1 = Display memory page address starts at B8000H.

Bit (6:2,0) — Not Applicable.

Bit 1 — Port 3BF Bit 0 Override.
0 = Prevents setting of Port 3BF bit 0, there by forcing the alpha mode operation.
1 = Allows the Port 3BF bit 0 to switch for the alpha or graphics mode selection.

HERCULES MODE REGISTER - WRITE ONLY PORT = 3BF



Bit 7 - Bit 2 — Reserved.

Bit 1 — Upper Memory Page Address.
Enable Mode Control Register (3?8) bit 7 selects the displayed memory page address in the graphics mode. When it is reset, bit 1 prevents access to the second memory page, located at B8000H for the 32KB memory space.
0 = Upper memory page is mapped out.
1 = Upper memory page is accessible.

Bit 0 — Enable Graphics.
Allows the Enable Mode Register (3?8) bit 1 to override.
0 = Alpha mode display.
1 = Text or graphics modes may be displayed.

EGA MODE

For the register defintions that **have not** changed from the VGA modes, refer to the VGA description. Only the **differences** between the VGA and EGA registers are briefly described in this section. Also, refer to the prior section for VGA mode details. Not Used bits should be set to 0, unless otherwise noted.

A general procedure to enter EGA mode of operation is described. The actual software implementation details are **not** covered in this procedure. These steps are briefly defined to outline the EGA mode entry:

* Load Configuration register bit 8. Logic 0 for VGA compatible PS2 display or Logic 1 for EGA compatible TTL monitor by appropriate pullup or pulldown resistor on MD(11). (Pullup resistor on MD11 causes CNF(8) to be latched with logic 0, for Analog PS2 compatible display).
* Unlock **all** the Paradise registers.
* Program PR2(6) to 0 for EGA mode.
* Set PR4 bit 1 to logic 1 for EGA compatibility.
* Load PR11(7:4) with EGA Configuration switches by using pullup or pulldown resistors on pins MD(15:12). (Pullup resistor causes logic 1 to be latched after power on reset.)
* The EGA switch setting may then be read from PR11(7:4) at I/O port 3C2 bit 4.
* If EGA is to be emulated on the IBM PS2 type analog display, follow the suggested steps listed below:

    - o Initialize all the registers.
    - o Lock CRT controller registers.
    - o Force Clock Control rate of the CRT controller.
    - o Set EGA emulation mode by programming:

```
PR11(3) = 1     ; Set EGA emulation on PS2 type display
PR14(6) = 1     ; Vertical double scan
PR11(2) = 1     ; Lock clock select
PR11(0) = 1     ; Lock 8/9 dot timing.
PR14(7) = 1     ; Enable IRQ (optional)
```

    - o Lock the Paradise registers PR0-PR5 and PR10-PR17.
    - o Read protect Paradise registers.

* When EGA is required on a TTL monitor, the suggested steps are:

    - o Initialize all the registers.
    - o Set EGA TTL mode by programming:

```
PR11(3) = 0     ; EGA TTL
PR14(7) = 1     ; Enable IRQ
PR15(6) = 1     ; Set Low Clock
PR14(7) = 1     ; Enable IRQ
```

    - o Lock Paradise registers PR0-PR5 and PR10-PR17
    - o Read protect Paradise registers.

For more details on the Paradise registers, refer to the Paradise registers section. The EGA register summary shown on the next page highlights all the EGA mode registers.

EGA REGISTERS SUMMARY

REGISTERS	EGA	I/O PORT
General Registers:		
Miscellaneous Output Reg	WO	3C2
Input Status Reg 0	RO	3C2
Input Status Reg 1	RO	3?A
Feature Control Reg	WO	3?A
Sequencer Registers:		
Sequencer Index Reg	WO	3C4
Sequencer Data Reg	WO	3C5
CRT Controller Registers:		
Index Reg	WO	3?4
CRT Controller Data Reg Except the following:	WO	3?5
Start Address High (Index=0C)	RW	3?5
Start Address Low (Index=0D)	RW	3?5
Cursor Location High (Index=0E)	RW	3?5
Cursor Location Low (Index=0F)	RW	3?5
Light Pen High, (Index=10)	R	3?5
Light Pen Low, (Index=11)	R	3?5
Graphics Controller Registers:		
Index Reg	WO	3CE
Other Graphics Reg	WO	3CF
Attribute Controller Registers:		
Index Reg	WO	3C0*
Attribute Controller Data Reg	WO	3C0*

NOTES:
1. **RO** = Read Only, **WO** = Write Only, and **RW** = Read/Write.
2. All Register addresses are in hex.
3. " ? " = " B " in Monochrome modes or " D " in Color modes.
4. " * " = Identical responses from I/O ports 3C0 and 3C1.

GENERAL REGISTERS

Only the General Registers and the bit definitions that **differ** between the VGA and EGA are addressed. Their EGA mode bit definitions are provided.

Miscellaneous Output Register (Write Port 3C2)

Bits (7:5) EGA: Same as Miscellaneous Output Register Bits (7:5) definition in the VGA section.

Bit 4 EGA: It disables the internal video drivers.

Logic 0 = Activates Video drivers
Logic 1 = De-activates video drivers.

Bits (3,2) EGA:

Bit 3	Bit 2	
0	0	14 MHz clock (VCLK0) is selected.
0	1	16 MHz clock (VCLK1) is selected if Configuration Register Bit 3 is 0.
1	0	External User Defined Clock (VCLK2) from the feature connector is selected if Configuration Register Bit 3 is 0.
1	1	Not Used. VCLK2 selected if Configuration Register Bit 3 is 0.

Bit (0) EGA: Identical to Miscellaneous Output Register Bit 0 definition in the VGA section.

Input Status Register 0 (Read Port 3C2)

Bit 7 EGA: Same as Input Status Register 0, Bit 7 definition in the VGA section.

Bits (6,5) EGA: Not used

Bit 4 EGA: The four configuration switches' information stored in PR11 can be read at this bit if PR4(1) has been set to 1.

Bits (3:0) EGA: Not used

Input Status Register 1 (READ PORT 3?A)

Bit (7) EGA: Not used

Bit 6 EGA: Set to 1.

Bits (5:3) EGA: Identical to Input Status Register 1 Bits (5:3) definition in the VGA section.

Bit 2 EGA: Not Used.

Bit 1 EGA: Not Used.

Bit (0) EGA: Same as Input Status Register 1 Bit 0 defintion in the VGA section.

Feature Control Register (WRITE PORT 3?A)

Bits (7:0) EGA: Not used

SEQUENCER REGISTERS (PORT 3C5)

Clocking Mode register (Index = 01)

Bits (7:4) EGA: Not Used

Bits (3,2) EGA: Same as Clocking Mode Register Bits (3,2) definition in the VGA section.

Bit 1 EGA: Set to zero

Bit (0) EGA: Identical to Clocking Mode Register Bit 0 definition in the VGA section.

Character Map Select Register (Index 03)

Bits (7:4) EGA: Not Used

Bits (3,2) EGA: Character Map Select A

Bits 3	2	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	1st 8K
0	1	1	2nd 8K
1	0	2	3rd 8K
1	1	3	4th 8K

Bits (1,0) EGA: Character Map Select B

Bits 1	0	Map Selected	Font Table/Plane 2 or 3 Location
0	0	0	1st 8K
0	1	1	2nd 8K
1	0	2	3rd 8K
1	1	3	4th 8K

NOTE: 1. Character Map selection from either Plane 2 or Plane 3 is determined by PR2(2), PR2(5) and bit 4 of the attribute code. It may be overridden by setting PR15(2) to 1 in alpha modes.

Memory Mode Register (Index = 04)

Bits (7:3) EGA: Not Used

Bits (2,1) EGA: Identical to Memory Mode Register Bits (2,1) definition in the VGA section.

Bit 0 EGA: Alpha mode bit.

A logic 1 shows that Alpha mode is active and character map selection is enabled. A logic 0 disables Alpha modes and enables non-Alpha modes.

CRT CONTROLLER REGISTERS (PORT 3?5)

The EGA registers that are different are listed. For similar registers and identical bits within registers refer to the VGA section. Also, " ? " implies that a register is mapped into either 3B5 or 3D5, for Monochrome or Color display modes, respectively.

Index Register (Port = 3?4)

Bits (7:5) EGA: Not Used.

Bits (4:0) EGA: Five bits point to the CRT Registers Address Index where the data is to be written.

Horizontal Total Register (Index = 00)

Bits (7:0) EGA: Eight bits of value for the " Total Character Count Less 2 " are loaded into this register. They define number of characters to be displayed per horizontal line.

End Horizontal Blanking Register (Index = 03)

Bits (7) EGA: Not Used.

Bits (6,5) EGA: They define display enable skew in character clocks.

Bit6	Bit5	Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0) EGA: Five bits of character count are loaded to determine when the horizontal blanking signal becomes inactive.

End Horizontal Retrace Register (Index = 05)

Bit 7 EGA: It defines the start of the odd or even CRT counter memory address following the horizontal retrace time. Logic "1" = Odd Address and logic "0" = Even Address.

Bits (6:0) EGA: Same as End Horizontal Retrace Register Bits (6:0) definition in the VGA section.

Vertical Total Register (Index = 06)

Bits (7:0) EGA: Lower eight bits of the CRT vertical frame time in scan lines including the vertical retrace.

CRT Controller Overflow Register (Index = 07)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Identical to CRT Controller Overflow Register Bits (4:0) definition in the VGA section.

Preset Row Scan Register (Index = 08)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Same as Preset Row Scan Register Bits (4:0) definition in the VGA section.

CRT CONTROLLER REGISTERS (PORT 3?5) CNTD.

Maximum Scan Line Register (Index = 09)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Same as Maximum Scan Line Register Bits (4:0) definition in the VGA section.

Cursor Start Register (Index = 0A)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Same as Cursor Start Register Bits (4:0) definition in the VGA section.

Cursor End Register (Index = 0B)

Bit (7) EGA: Not used.

Bits (6,5) EGA: They define cursor signal skew in character clocks.

Bit6	Bit5	Skew
0	0	0
0	1	1
1	0	2
1	1	3

Bits (4:0) EGA: These bits define Cursor End value of row scan address counter. The programmed value is equal to "N+1" where "N" is the last row of the Cursor to be displayed.

Vertical Retrace Start Register (Index = 10) - Write
(Light Pen High register, Index = 10 - Read)

Bits (7:0) EGA: Lower eight bits of the vertical retrace start position programmed in horizontal scan lines.

(Light Pen High : Bits 7:0 are the high order bits of memory address counter when light pen triggered. Not supported by WD90C00.)

Vertical Retrace End Register (Index = 11) - Write
(Light Pen Low register, Index = 11 - Read)

Bits (7,6) EGA: Not Used

Bit 5 EGA: It enables the IRQ output buffer control if Logic 0 is programmed. The IRQ latch within the CRT controller determines the logic state of the IRQ output signal. If programmed as logic 1, the IRQ buffer is switched to a high impedence state.

Bit 4 EGA: When programmed to logic 0, the IRQ latch is reset and cleared to 0 if bit 5 = 0. If it is logic 1, the IRQ latch gets set at the end of the vertical display.

Bits (3:0) EGA: Identical to Vertical Retrace End Register Bits (3:0) definition in the VGA section.

(Light Pen Low : Bits 7:0 are the low order bits of memory address counter when the light pen triggered. Not supported by WD90C00.)

CRT CONTROLLER RE TERS (PORT 3?5) CNTD.

Underline Location Register (Index = 14)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Horizontal scan row where the underline will be displayed.

End Vertical Blanking Register (Index = 16)

Bits (7:5) EGA: Not used.

Bits (4:0) EGA: Identical to End Vertical Blanking Register Bits (4:0) definition in the VGA section.

Mode Control Register (Index = 17)

Bits (7:5) EGA: Same as Mode Control Register Bits (7:5) definition in the VGA section.

Bit 4 EGA: Not Used.

Bits (3:0) EGA: Identical to Mode Control Register Bits (3:0) definition in the VGA section.

GRAPHICS CONTROLLER REGISTERS (PORT 3CF)

Read Map Select Register (Index = 04)

Bits (7:3) EGA: Not Used.

Bits (2:0) EGA: Map select bits (2:0) which represent encoded value of the memory plane in binary as shown below:

D2	D1	D0	Map selected
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3

Mode Register (Index = 05)

Bit (6,7) EGA: Not Used

Bits (5:2) EGA: Identical to Mode Register Bits (5:2) definition in the VGA section.

Bits (1,0) EGA: Binary coded write bits define the write modes per table below:

Bit 1	Bit 0	Function
0	0	Write mode 0 - Refer to earlier section
0	1	Write mode 1 - Refer to earlier section
1	0	Write mode 2 - Refer to earlier section
1	1	Write mode 3 - Not Legal. Selects write mode 1.

ATTRIBUTE CONTROLLER REGISTERS (PORTS = 3C0 / 3C1)

Palette Registers (Index = 00 through 0F)

Bits (7,6) EGA: Not Used.

Bits (5:0) EGA: Dynamic color selection. Logic 0 = Color de-selection, and Logic 1 = color selection per the table below:

Bits	Color	Pixel
5	Secondary Red	P5
4	Secondary Green	P4
3	Secondary Blue	P3
2	Red	P2
1	Green	P1
0	Blue	P0

Mode Control Register (Index = 10)

Bits (7:4) EGA: Not Used

Bits (3:0) EGA Identical to Mode Control Register Bits (3:0) definition in the VGA section.

Overscan Color Register (Index = 11)

Bits (7,6) EGA: Not Used

Bits (5:0) EGA: Overscan color for the border. For a monochrome display, set all the six bits to logic 0. The border color is defined by the color table for the Palette registers shown above.

Color Plane Enable Register (Index = 12)

Bits (7,6) EGA: Same as Color Plane Enable Register Bits(7,6) in the VGA section.

Bits (5,4) EGA: Determines two of six colors for the Video Status Mux. per the table listed:

Bit 5	Bit 4	Input Status Register 1 (Port 3?A) Bit 5	Bit 4
0	0	P2 (Red)	P0 (Blue)
0	1	P5 (SRed)	P4 (SGreen)
1	0	P3 (SBlue)	P1 (Green)
1	1	P5 (SRed)	P4 (SGreen)

Bits (3:0) EGA: Same as Color Plane Enable Register Bits (3:0) definition in the VGA section.

Horizontal PEL Panning Register (Index = 13)

Bits (7:4) EGA: Not Used

Bits (3:0) EGA: These four bits determine the horizontal left shift of the video data in number of pixels. In monochrome alpha numeric modes, (9 dots/character) image can be shifted by 9 pixels. For all other graphics or alpha numeric modes, a maximum left shift of 8 pixels is permitted. Refer to the left shift pixel table of the Horizontal PEL Panning Register Bits (3:0) described in the VGA section.

WD90C00 PARADISE REGISTERS

The Paradise WD90C00 has additional features that enhance the performance and functions of the PVGA1A, introduced earlier, and the basic VGA subsystem. To accomplish this, the WD90C00 architecture is optimized with additional I/O registers.

WD90C00 uses the MCLK to derive the DRAM timing in Alpha and Graphics modes. A 36 MHZ MCLK is provided for 120ns access time DRAMs. Similarly, 45 MHz MCLK is connected for the 100ns access time DRAMs. In Alpha modes, page read mode is also provided for faster video memory read operations. Due to the above changes in design, the WD90C00 performance will be significantly better than the PVGA1A. The registers are at the I/O locations unused by IBM. All registers are read/write, except where noted.

Name	Designation	I/O location
Address Offset A	PR0A(6:0)	3CF.09
Alternate Address Offset B	PR0B(6:0)	3CF.0A
Memory Size	PR1(7:0)	3CF.0B
Video Select	PR2(7:0)	3CF.0C
CRT Control	PR3(7:0)	3CF.0D
Video Control	PR4(7:0)	3CF.0E
Unlock PR0-PR4	PR5(7:0)	3CF.0F
Unlock PR11-PR17	PR10(7:0)	3?5.29
EGA Switches	PR11(7:0)	3?5.2A
Scratch Pad	PR12(7:0)	3?5.2B
Interlace H/2 Start	PR13(7:0)	3?5.2C
Interlace H/2 End	PR14(7:0)	3?5.2D
Miscellaneous Control 1	PR15(7:0)	3?5.2E
Miscellaneous Control 2	PR16(7:0)	3?5.2F
Miscellaneous Control 3	PR17(0)	3?5.30
Reserved		3?5.31 - 3?5.3F

Note: 1.0 The designation 3?5 means that the register is mapped into either 3B5 in monochrome mode or 3D5 in color modes.

2.0 Paradise register notation - XXX.YY where XXX is the data port address and YY is the register index e.g. 3CF.0F implies 0F-->3CEH (Select Index register) followed by (Data byte) --> 3CF (Data Port).

Registers PR0 through PR4 and PR11 through PR17 are normally locked. They are write protected at power-up by the hardware reset. In order to load those registers, the appropriate unlock register PR5 or PR10 must be loaded first with binary XXXXX101; a register remains unlocked until any other value is written to the unlocked register. Registers PR0 through PR5 are readable only if PR4 bit1 = 0. Registers PR10 through PR17 are read protected at power up by hardware reset. In order to read registers PR10 through PR17 load PR10 with 1XXX0XXX. The register remains readable until any other value is written to PR10. When registers PR10 through PR17 are read protected, reading them would show data to be FFH. Setting PR4 bit 1 to 1 does not read protect registers PR10 through PR17. All PR registers, are set to 0 at power-on-reset, except where noted.

PR0 A,B - [3CF.09, 3CF0A] Address Offset Registers PR0A & PR0B

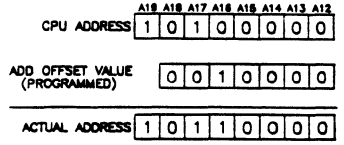
The WD90C00 can control up to one megabyte of video RAM. However, the memory map for IBM PC and compatible product assigns 128 Kbytes of the available 1MB total system space to the video controller. Therefore, the video memory space starts at A0000H and ends at BFFFFH. To allow a second video card to co-exist, this space is furthur limited to a 64KB video memory partition. Primary offset register (PR0A), is always enabled if PR(0:4) is unlocked. PR0A is normally used to control 64KB of the available video address space.

Alternatively, for 64KB VGA address space Paradise address offset register (PR0A) and address offset register (PR0B) may be used to access two 32KB video RAM windows. PR0A window is mapped from A8000H-AFFFF while PR0B is mapped from A0000H-7FFFFH if PR1 bit 3 is set to 1 (Alternate address register PR0B is enabled).

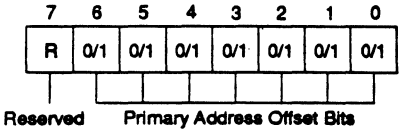
Similarly, for 128KB address space, PR0A is mapped from B0000-BFFFF while PR0B is mappped from A0000-AFFFF when the alternate address space register PR0B is enabled.

PR0 A,B - [3CF.09, 3CF0A] Address Offset Registers PR0A & PR0B (CNTD.)

These registers contain an offset which gets added to the system address when accessing more than 64K bytes of video memory. Address offset register A is the primary address offset register and is always enabled. On the other hand, alternate address offset register B is enabled only if PR1 bit3 is set to 1. PR0A,B register seven bit offset is added to address bits (12:18) of the system address bus SA(0:19) to form a 20 bit address. It can be thought of as being segment registers DS and ES of the 8088 / 80X86 architecture. PR0A,B will have 4KB segments. Bit 7 of both, PR0A and PR0B, are not used and always set to 0. This is shown in graphic below:

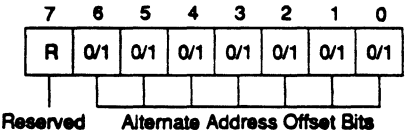


PR0 A - ADDRESS OFFSET REGISTER A - READ/WRITE PORT= 3CF & INDEX REGISTER=09



Address Offset Register A
Added to the System Address
Selected When Address Bit A15=1
It is the Default Address
Offset Register

PR0 B - ADDRESS OFFSET REGISTER B - READ/WRITE PORT=3CF & INDEX REGISTER=0A



Address Offset Register B
Selected by System Address
only if PR1(bit 3)=1

PR1 - [3CF.0B] Memory Size

This register is 8 bits wide. Bits PR1 (1:0) are latched internally at power on reset from the corresponding memory data bus pins MD (1:0), using either pullup or pulldown external resistors. Pullup resistors on MD(1:0) causes PR1(1:0) bits to be latched low. According to the VGA video memory organization, 256KB of the available memory space is divided into four 64KB maps (0-3) each defining bit planes (0-3). In mode 13, the four bit planes are chained to form one large bit plane.

The starting address of the 256KB video memory buffer can be configured to match other video adapters, and, or, application programs. For example, 256KB video display buffer with 128KB or 64KB segments can start at address A0000 (Hex) while 32KB segments start at address B0000 (Hex) or B8000 (Hex). WD90C00 enhances memory size capability when bits 6 and 7 are programmed to extend video buffer size to 512KB or 1024KB. The DRAM organizations supported by the WD90C00 and its associated video space table are shown below:

DRAMS	MA8 PIN	VIDEO SPACE	MEMORY PLANES
64Kx4	N/U	256KB	FOUR (64KB PER PLANE)
64Kx4	BANK SELECT	512KB	FOUR (128KB PER PLANE)
256Kx4	DRAM PIN A8	1024KB	FOUR (256KB PER PLANE)

When video memory size is 512KB, and 64Kx4 DRAMS are used, two banks of 64KB form 128KB per plane. MA8 provides the bank selection using an external multiplexer to access the appropriate bank in a plane. Four planes form the desired 512KB video memory space. For 1024KB video memory size, MA8 is directly connected to the A8 address pin of the 256Kx4 DRAMS, and two DRAMS form a 256KB per plane. Four planes make the desired 1024KB video memory space. For more details, refer to the programming section listed on the next page.

PR1 bits 7 and 6 must be set to reflect the amount of memory installed. These bits in conjunction with PR16 (1) also select the way memory is mapped into the system address space. If PR16 (1) is set to 1, the memory mapping is same as IBM VGA regardless of PR1 (6) and PR1 (7).

GRAPHICS MODE RAM ADDRESSING:

PR1(7) PR1(6)

0 0 256KTOTAL; 64K/PLANE; IBM VGA MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE CPU	BYTE CRT	WORD CPU	WORD CRT	DBL WORD CPU	DBL WORD CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
.....	.....	.....	.....	.....	....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(15)	CA(13)
MA(0)	A(0)	CA(0)	A(16) or XRN(5)	CA(15) or CA(13)	A(14)	CA(12)

PR1 - [3CF.0B] Memory Size (CNTD.)

PR1(7) PR1(6)

0 1 — 256K TOTAL; 64K/PLANE; WD90C00 MEMORY ORGANIZATION

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	0	0	0	0	0	0
MA(16)	0	0	0	0	0	0
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

PR1(7) PR1(6)

1 0 — 512KB TOTAL IN FOUR PLANES ; 128KB / PLANE IN WD90C00 MEMORY ORGANIZATION (EACH PLANE IS 2 BANKS OF 64K x 8)

VIDEO RAM ADDR BIT	BYTE		WORD		DBL WORD	
	CPU	CRT	CPU	CRT	CPU	CRT
MA(17)	-----	-----	-----	-----	-----	-----
MA(16)*	A(16)*	CA(16)*	A(17)*	CA(16)*	A(18)*	CA(16)*
MA(15)	A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)	A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....	.....	.....	.....	.....	.....	.....
MA(2)	A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)	A(1)	CA(1)	A(1)	CA(0)	A(17)	CA(15)
MA(0)	A(0)	CA(0)	A(16)	CA(15)	A(16)	CA(14)

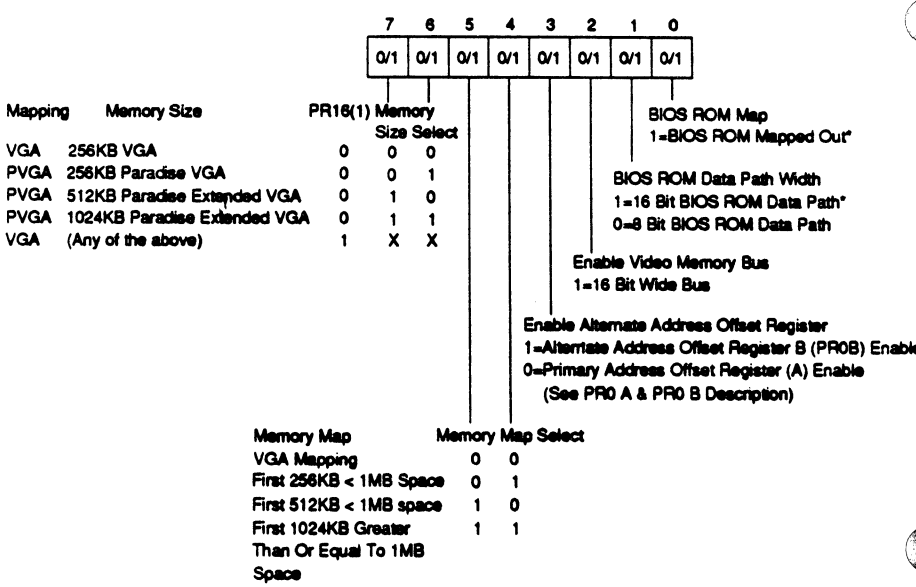
NOTE: "*" Controls CAS external to WD90C00

PR1 - [3CF.0B] Memory Size (CNTD.)

PR1(7)	PR1(6)						
1	1	1024KB TOTAL IN FOUR PLANES ; 256K/PLANE IN WD90C00 MEMORY ORGANIZATION					
VIDEO RAM ADDR BIT		BYTE		WORD		DBL WORD	
		CPU	CRT	CPU	CRT	CPU	CRT
MA(17)		A(17)	CA(17)	A(17)	CA(16)	A(17)	CA(15)
MA(16)		A(16)	CA(16)	A(16)	CA(15)	A(16)	CA(14)
MA(15)		A(15)	CA(15)	A(15)	CA(14)	A(15)	CA(13)
MA(14)		A(14)	CA(14)	A(14)	CA(13)	A(14)	CA(12)
.....		.....	.....	.....	.....	.....	.....
MA(2)		A(2)	CA(2)	A(2)	CA(1)	A(2)	CA(0)
MA(1)		A(1)	CA(1)	A(1)	CA(0)	A(19)	CA(17)
MA(0)		A(0)	CA(0)	A(18)	CA(17)	A(18)	CA(16)

NOTE :
1. A(19)-A(0) are modified System Addresses.
2. CA(17)-CA(0) are CRT Controller Character Address Counter bits.
3. XRN(5) is Miscellaneous Output Register 3C2, inverted bit 5. This bit selects the displayed page in chained modes. XRN(5)is selected as MA(0) if GR6(3) OR GR6(2) = 1.
4. CA(13) is selected as MA(0) if CRTC Mode Register R17(5) = 0.

PR1 - MEMORY SIZE REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0B



NOTE: * = A Pull Up Resister On MD(0) Or MD(1) Line Sets These Bits To 0 At Power On Reset

PR1 - [3CF.0B] Memory Size (CNTD.)

Bit7	Bit6	PR16(1)	MEMORY SIZE	MAPPING
0	0	0	256KB STANDARD VGA	VGA *
0	1	0	256KB PARADISE VGA	PVGA**
1	0	0	512KB PARADISE E XTENDED VGA	PVGA
1	1	0	1024KB PARADISE EXTENDED VGA	PVGA
X	X	1	Any of the above	VGA

Bit5	Bit4	MEMORY MAP
0	0	VGA Mapping in 64KB space - A0000 to BFFFF Address Range
0	1	1st 256KB in 1MB space - 00000 to 3FFFF Address Range
1	0	1st 512KB in 1MB space - 00000 to 7FFFF Address Range
1	1	1st 1024KB in greater or equal to 1MB space - 00000 to FFFFF Address Range

Bit3 — Enable Alternate Address Offset Register (Refer to PR0A and PR0B descriptions)

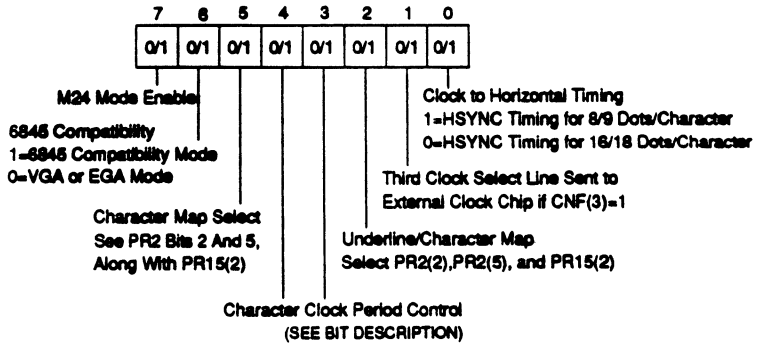
Bit2 — Enable 16 bit bus for Video Memory

Bit1 — When set to 1, the BIOS ROM has 16 bits data path. If set to 0, the BIOS ROM data path is 8 bits wide. A pullup on MD (1) sets this bit to 0 at power on reset.

Bit0 — If set to 1 the BIOS ROM is mapped out. Pullup reisistor latches 0 after power up. A pullup on MD (0) sets this bit to 0 at power on reset.

NOTE: " * " = Only 64KB are accessible for chained 4 packed pixel mode.
" ** " = Paradise extended modes can fully utilize up to 256 KB.

PR2 - VIDEO SELECT REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0C



PR2 - [3CF.0C] Video Select

Bit 7

Enable M24 mode.

Bit 6

0 : VGA or EGA mode
1 : Non-VGA (6845) mode

Bit 5

Character Map Select. The following functions are overriden by setting PR15(2). This bit in conjunction with PR2(2) and bit 4 of the attribute code, enables character maps from planes 2 or 3 to be selected per the table below:

PR2(5)	PR2(2)	ATT(4)	Plane Select
0	0	X	2
0	1	X	2
1	0	X	3
1	1	0	2
1	1	1	3

Note: Setting PR15(2) = 1 i.e. selecting page mode addressing overrides plane select table shown above.

Bit 4 3

Character clock period control

0	0
0	1
1	0
1	1

IBM VGA character clock (8 or 9 dots)
7 dots (used for 132 character mode)
9 dots
10 dots

Selecting 10 dots per character modifies the function of the horizontal PEL Panning register (3C0.13). Pixel panning in the 10 dot-character modes is obtained by storing the following values into the horizontal PEL Panning register:

PEL Panning Register value	PELS Shifted Left
09	0
08	1
00	2
01	3
02	4
03	5
04	6
05	7
06	8
07	9

NOTE: The character clock period control functions have no effect in graphics modes.

Bit 2

Underline and character map select. Setting this bit to 1 enables underline for all odd values of attribute codes, e.g. Programming 1 gives blue underline. It overrides the background color function of the attribute code bit 4 , which is forced to 0. Therefore, only eight choices of background colors are selectable. This function allows trading background colors for more character maps. In conjunction with PR2(5), this bit is also decoded to enable character maps from planes 2 or 3. See PR2(5) for details.

PR2 - [3CF.0C] Video Select (CNTD.)

Bit	1	This bit is the third clock select line which is sent to the external clock chip if CNF(3) is set to 1. When CNF(3) is set to 0, it locks the internal video clock select multiplexer.
Bit	0	Forces horizontal timing clock of the CRTC to the higher rate (8 or 9 VCLKs). 0 = Set horizontal sync timing for 16/18 dots per character. 1 = Set horizontal sync timing for 8/9 dots per character.

PR3 - [3CF.0D] CRT Control And Group Locking

The CRT control register description and software notation are summarized. For example, 3?5.11(7) refers to bit 7 of the CRTC data register 11 (Hex). To read this bit, first write 11 (Hex) to to 3?4, then read 3?5 and test bit 7's value.

WD90C00 CRT CONTROLLER - REGISTER LOCKING

Register locking is controlled by 4 bits. They are PR3 (5,1,0) and 3?5.11(7) (i.e. IBM Vertical Retrace End Register bit 7 controlled by index register 11). When bit 7 is 1, CRT contoller registers (R0-7) are write protected per VGA definition. For more information on the five groups, and their locking schemes, refer to the section below:

GROUP 0

These registers are locked if PR3(5)=1 OR 3?5.11(7)=1
CRT controller register 00 ------ Horizontal Total characters per scan
CRT controller register 01 ------- Horizontal Display Enable End
CRT controller register 02 ------ Start Horizontal Blanking
CRT controller register 03 ------ End Horizontal Blanking
CRT controller register 04 ------ Start Horizontal Retrace
CRT controller register 05 ------ End Horizontal Retrace

PR3- [3CF.0D] CRT Control And Group Locking(CNTD.)

GROUP 1

These registers are locked if PR3(1)=0 AND 3?5.11(7)=1
CRT controller register 07(Bit6) ------ Vertical Display Enable End bit 9
CRT controller register 07(Bit1) ------ Vertical Display Enable End bit 8

GROUP 2

These registers are locked if PR3(0)=1 OR 3?5.11(7)=1
CRT controller register 06 -------- Vertical Total
CRT controller register 07(Bit7) ------ Vertical Retrace Start bit 9
CRT controller register 07(Bit5) ------ Vertical Total bit 9
CRT controller register 07(Bit3) ------ Start Vertical Blank bit 8
CRT controller register 07(Bit2) ------ Vertical Retrace Start bit 8
CRT controller register 07(Bit0) ------ Vertical Total bit 8

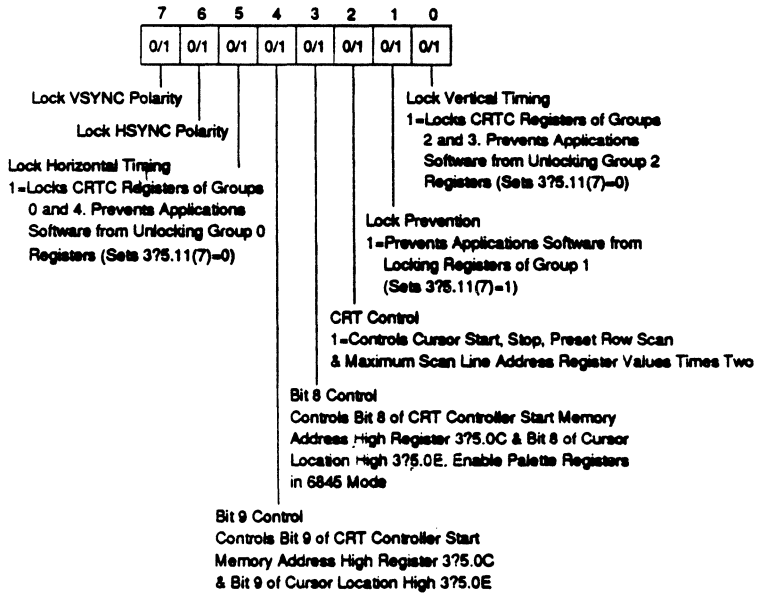
GROUP 3

These registers are locked if PR3(0)=1
CRT controller register 09(Bit5) ------ Start Vertical Blank bit 9
CRT controller register 10 ------ Vertical Retrace Start
CRT controller register 11(Bits 3-0) ------ Vertical Retrace End
CRT controller register 15 ------ Start Vertical Blanking
CRT controller register 16 ------- End Vertical Blanking

GROUP 4

This register is locked if PR3(5)=1
CRTC mode control register 17(Bit2) ----- Selects divide by two vertical timing

PR3 - CRT LOCK CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0D

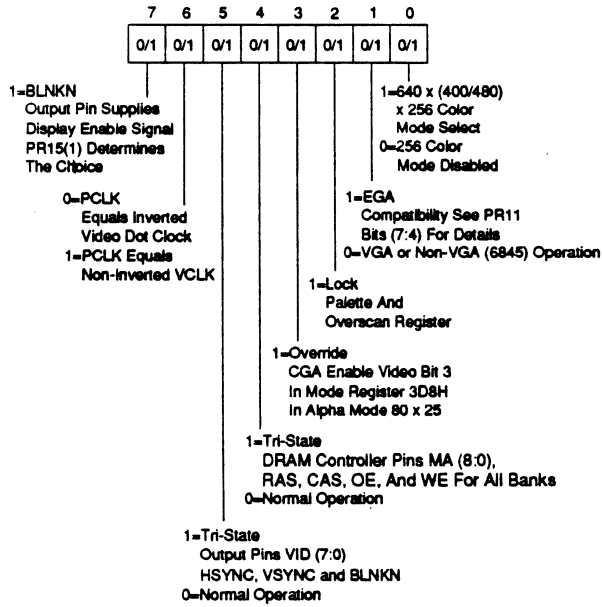


PR3 - [3CF.0D] CRT Control

Bit 7	Lock VSYNC polarity, as programmed in 3C2 bit 7
Bit 6	Lock HSYNC polarity, as programmed in 3C2 bit 6
Bit 5	Lock horizontal timing. Locks CRTC registers of Groups 0 and 4. Prevents attempt by applications software to unlock Group 0 registers by setting 3?5.11 bit 7=0.
Bit 4	Bit 9 of CRT Controller Start Memory Address High Register 3?5 .0C, and bit 9 of Cursor Location High 3?5 .0E. This bit corresponds to Character Address CA (17).
Bit 3	Bit 8 of CRT Controller Start Memory Address High Register 3?5.0C, and bit 8 of Cursor Location High 3?5.0E. This bit corresponds to Character Address CA (16).
Bit 2	Cursor start, stop, preset row scan, and maximum scan line address registers values multiplied by two.
Bit 1	1 = Prevents attempt by applications software to lock registers of Group 1 by its setting 3?5 .11 bit 7=1.
Bit 0	Lock vertical timing. 1 = Locks CRTC registers of Groups 2 and 3. Overrides attempt by applications software to unlock Group 2 registers by its setting 3?5 .11 bit 7=0.

PR4 - VIDEO CONTROL REGISTER - READ/WRITE PORT=3CF & INDEX REGISTER=0E

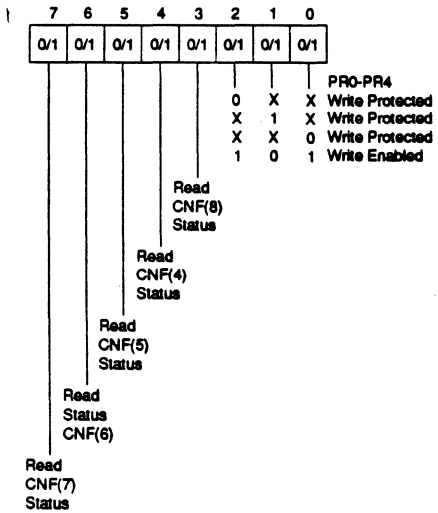
The video monitor output control register (PR4) can be programmed to tri-state the CRT display control outputs as well as video data for the RAMDAC, and memory control outputs.



PR4 - [3CF.0E] Video Control

Bit	7	This bit controls the output signal BLNKN. Normally in the VGA mode, BLNKN is used by the external video DAC to generate blanking. If this bit = 1, the BLNKN output supplies a display enable signal. A choice of two types of display enable timings can be selected, and is determined by PR15(1).
Bit	6	Select PCLK equal to VCLK. 0 = PCLK is the inverted internal video dot clock, or half the dot clock frquency, depending upon the video mode. 1 = PCLK is always the non-inverted VCLK input clock.
Bit	5	Tri-state the outputs VID(7:0), HSYNC,VSYNC, and BLNKN.
Bit	4	Tri-state the memory control outputs. The memory address bus MA(8:0), and all ten DRAM control signals are tri-stated when this bit is set to 1.
Bit	3	Overrides the CGA "enable video" bit 3 of mode register 3D8, only in 80 x 25 alpha CGA (Non-VGA) mode. Override effectively forces this bit to 1. Power-on-reset causes no override.
Bit	2	Lock palette and overscan registers.
Bit	1	EGA compatibility bit where 1 = EGA Compatible Mode. It disables reads to all registers which are write-only registers in the IBM EGA. Also, registers at 3C0/3C1 change to write-only mode if the EGA compatibility bit is set. In addition to selecting EGA compatibility, setting this bit to 1 disables reading PR0 - PR5. In VGA mode (PR(4) bit 1 is zero) 3C0 register is read/write while 3C1 register is read only, per the Attribute Controller registers definition.
Bit	0	Paradise shift register control. It configures the video shift registers for 256-color mode.

PR5 - GENERAL PURPOSE STATUS BITS - READ/WRITE PORT=3CF & INDEX REGISTER =0F



PR5 - [3CF.0F] Unlock PR0-PR4

Bits (2:0) are READ/WRITE bits and cleared to 0 by reset. They provide lock or unlock capability for Paradise for registers PR0 through PR4 like the PVGA1A. The PR0 - PR4 registers are unlocked when "X5" is written to PR5. They remain unlocked until any other value is written to PR5. This register also provides readable status for the configuration register bits 4 through 8. Setting PR(4) bit 1 to 1, read protects registers PR0 - PR5.

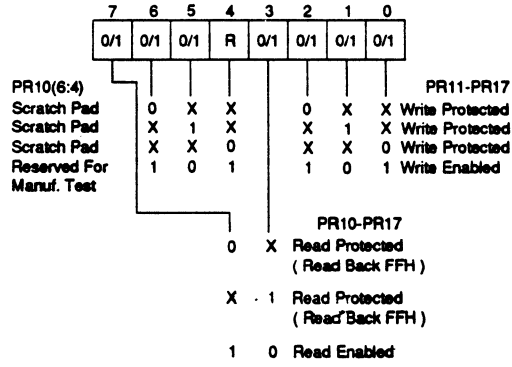
Bit	7	= CNF(7) [READ ONLY]
Bit	6	= CNF(6) [READ ONLY]
Bit	5	= CNF(5) [READ ONLY]
Bit	4	= CNF(4) [READ ONLY]
Bit	3	= CNF(8) [READ ONLY]
Bits	(2:0)	READ/WRITE bits and cleared to 0 by reset. They control writing to Paradise registers PR0-PR4 as follows:

2 1 0 PR0-PR4

0 X X Write protected
X 1 X Write protected
X X 0 Write protected

PR10 - [3?5.29] Unlock PR11-PR17

This register is READ/WRITE and cleared to 0 by reset. PR10 can be loaded if it contains XXXXX101, and can only be read if it has 1XXX0XXX. Bits (7,3), Bits(6:4), and Bits (2:0) control access to Paradise registers PR10-PR17. Bits 7 and 3 enable register read operation for PR10 - PR17. Bits (6:4) may be used as scratch pad. Bits (2:0) enable register write operation for PR11 - PR17.



PR10 - [3?5.29] Unlock PR11-PR17 (CNTD.)

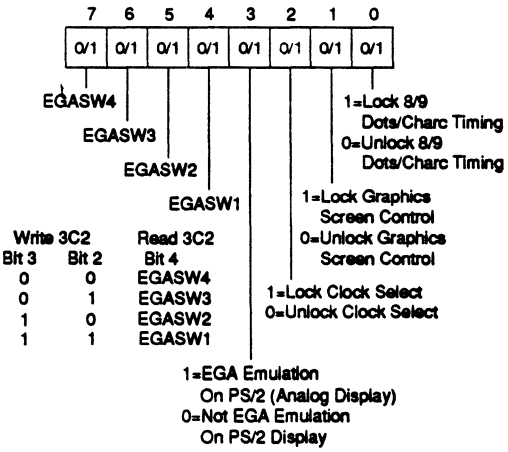
Bit7	Bit3	PR10-PR17
0	X	Read protected, read back data FFH
X	1	Read protected, read back data FFH
1	0	Read Enabled

Bit2	Bit1	Bit0	PR11-PR17
0	X	X	Write protected
X	1	X	Write protected
X	X	0	Write protected
1	0	1	Write Enabled

Bit6	Bit5	Bit4	PR10(6:4)
0	X	X	Scratch pad
X	1	X	Scratch pad
X	X	0	Scratch pad
1	0	1	Reserved for manufacturing test.

PR11 - [3?5.2A] EGA Switches

The EGA switch configuration details are stored in the PR11 register bits. This register can be **loaded** if PR10 contains XXXXX101, and can only be **read** if PR10 contains 1XXX0XXX.



PR11 - [3?5.2A] EGA Switches

Bits (7:4) = EGA CONFIGURATION SWITCHES SW4-SW1. These bits are READ/WRITE and latched internally at power-on-reset from corresponding memory data bus pins MD(15:12), provided with either pullup or pulldown external resistors. PULLING UP MD(15:12) causes PR11(7:4) to be latched HIGH. These bits can be read as bit 4 of port 3C2 if the EGA COMPATIBILITY BIT [PR4(1)] has been set to 1. Selection of the bit to be read is determined by bits 3 & 2 of the Miscellaneous Output Register 3C2, as follows:

WRITE		READ
3C2 bit 3	**3C2 bit 2**	**3C2 bit 4**
0	0	PR11(7) [= EGA SW4]
0	1	PR11(6) [= EGA SW3]
1	0	PR11(5) [= EGA SW2]
1	1	PR11(4) [= EGA SW1]

PR11 Bits 3 through 0 are READ/WRITE and cleared to 0 at power on reset.

Bit 3 Select EGA Emulation on a PS/2 (VGA-compatible, analog) display.

Bit 2 Lock Clock Select. This bit locks the internal video clock select multiplexer and disables loading of an external clock chip through VCLK1.

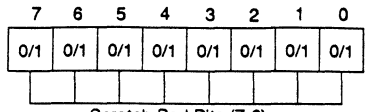
Bit 1 Lock Graphics Controller screen control. Setting PR11(1) to 1 prevents modification of the following bits in the Graphics controller as well as the Sequencer:

Graphics Controller	3CF.05 bits (6:5)
Sequencer	3C5.01 bits (5:2)
Sequencer	3C5.03 bits (5:0)

Although the internal functions selected by these graphics controller and sequencer bits are locked by setting PR11 bit 1 to 1, they appear unlocked to the system processor during read operation.

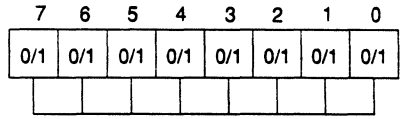
Bit 0 Lock 8/9 dots. Setting this bit to 1 prevents modification of clocking mode sequencer register 3C5.01 bit 0. Although 8 or 9 character timing is locked by setting PR11 bit 0 to 1, the 3C5.01 bit 0 appears unlocked to the system processor during read.

PR12 - [3?5.2B] Scratch Pad



This 8-bit register is READ/WRITE and is unlocked by loading XXXXX101 into PR10. To read this register load PR10 with 1XXX0XXX. The data in this register is unaffected by hardware reset and undefined at power up.

PR13 [3?5.2C] Interlace H/2 Start



PR13(7:0)=[Horizontal Retrace Start Register]-[Horizontal Total Count +5)/2]=HRD
Where HRD=Horizontal Retrace Delay

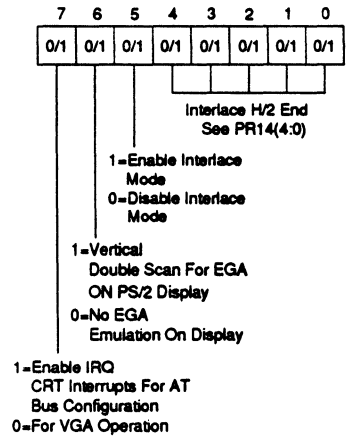
This 8-bit register is READ/WRITE and is unlocked by loading XXXXX101 into PR10. To read this register load PR10 with 1XXX0XXX. The data in this register is unaffected by hardware reset and undefined at power up. This register defines the starting horizontal character count at which vertical timing is clocked on alternate fields in interlaced operation. Interlaced operation is enabled by setting PR14(5) to 1. All other standard non-interlaced modes are unaffected by the contents of this register. This register must be programmed with a value derived from the values chosen to be programmed into the Horizontal Retrace Start Register (3?5.04) and Horizontal Total Register (3?5.00):

PR13(7:0) = [HORIZ RET START] - [(HORIZ TOT + 5) / 2] + HRD

Note: In the above expresssion, HRD = Horizontal Retrace Delay, determined by bits 6 and 5 of the Horizontal Retrace End Register (3?5.05).

PR14 - [3?5.2D] Interlace H/2 End

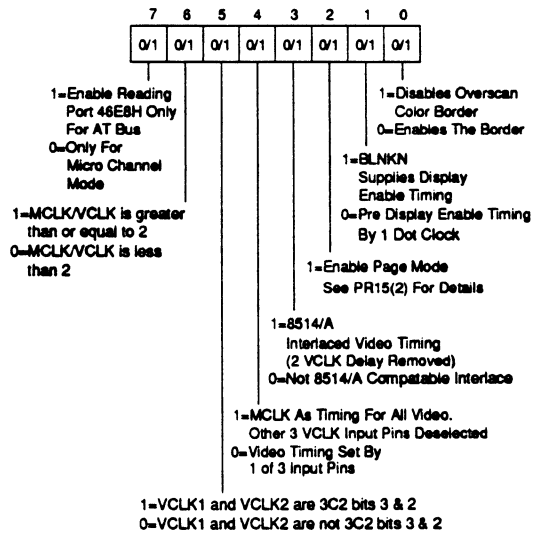
This 8-bit READ/WRITE register is unlocked by loadingXXXXX101 into PR10. To read this register load PR10 with 1XXX0XXX. Bits 4 through 0 are unaffected by hardware reset and undefined at power up. Bits 7 through 5 are cleared to 0 by reset.



PR14 - [3?5.2D] Interlace H/2 End (CNTD.)

Bit	7	Enable IRQ. This bit may be set to enable CRT interrupts to be generated when configured for AT BUS operation, allowing EGA compatibility support for interrupt-driven EGA applications. For VGA operation with an AT BUS, interrupts are not used, and this bit should be set to 0. This bit has no effect in MICROCHANNEL operation and is set to 0.
Bit	6	Vertical double scan. This bit should be set to 1 when emulating EGA on PS /2 display. Setting this bit to 1 causes the CRTC's Vertical Displayed line counter and row scan counter to be clocked by divide-by-two horizontal timing if vertical sync polarity (3C2 Bit 7=0) is programmed to be positive. Therefore, the relationship between the actual number of lines displayed [N] and the data [n] programmed into the Vertical Display Enable End register is: $N = 2(n+1)$ Likewise, the relationship between the actual number of scan lines per character row [N] and the data [n] programmed in the Maximum Scan Line register holds true.
Bit	5	Interlaced mode Setting this bit to 1 selects interlaced mode. The interlaced mode can be used in those video modes in which the data programmed into the Maximum Scan Line Address register {3?5.09} = 0XX00000. Line compare and double scan are not supported.
Bits	(4:0)	Interlace H/2 end bits (4:0). Add the contents of the Interlace H/2 Start Register PR(13) to the horizontal sync width (same as defined by 3X5.04,05). Program 5 LSB of the sum into these bit locations.

PR15 - [3?5.2E] Miscellaneous Control 1



PR15 - [3?5.2E] Miscellaneous Control 1 (CNTD.)

This Read/Write register is unlocked by writing XXXXX101 into PR10. To read this register load PR10 with 1XXX0XXX.

Bit	7	Enable reading port 46E8H. This bit is functional only if AT BUS architecture [CNF(2)=1] is selected. Setting this bit to 1 enables I/O port 46E8 to be read, regardless of the state of its own bits 3 and 4 and of port 102 bit 0 (sleep bit). Only bits (4:0) of port 46E8 are readable; bits (7:5) are 0.
Bit	6	Low VCLK. Setting this bit to 1 adjusts the memory timing to allow use of a video clock (VCLK) frequency which is much lower than the memory clock (MCLK) frequency. This bit should be set to 1 if the following expression is satisfied: (MCLK in MHZ) / (VCLK in MHZ) > 2
Bit	5	This bit is used only if CNF(3) = 1 which configures the VCLK1 and VCLK2 pins as outputs. Setting this bit to 1 causes outputs VCLK1 and VCLK2 to equal bits 2 and 3 of I/O write register (Miscellaneous output register) at 3C2H respectively.
* Bit	4	Select MCLK as video clock. Setting this bit to 1 causes the MCLK input to be selected for the source of all video timing. The other three VCLK inputs can not be selected when this bit is set.
Bit	3	Interlaced Compatibility. This bit should be used only if interlaced mode is selected (see PR14). This bit should be set to 1 if exact timing emulation of the IBM 8514/A's interlaced video timing is required. Setting this bit to 1 causes vertical sync to be generated from the trailing edge of non-skewed horizontal sync, instead of the leading edge, as generated for VGA timing. Setting this bit to 1 also removes two VCLK delays from the default VGA video dot path delay chain.
* Bit	2	Select Page Mode Addressing. Setting this bit to 1 forces screen refresh memory read cycles to use page mode addressing in alpha modes. Page mode addressing is automatically used in the graphics modes. Page mode addressing requires less time than RAS-CAS addressing; therefore, selecting page mode addressing increases the bandwidth for the CPU to access video memory by 30 - 40%. Set this bit to 1 if 132 character mode timing is selected (see description of PR2). Setting this bit to 1 in any alpha mode overrides the character map select functions of PR2(2) and PR2(5). When this bit is set to 1, it redefines the Character Map Select Register (3C5.03). One of eight, 8K memory segments containing a pair of maps in Plane 2 or Plane 3 is addressed by bits (2:0) of this register while the map selection is determined by the bits (4:3). A pair of adjacent 8K character maps in planes 2 and 3, (adjacent in the sense that they have the same addressing) may be selected by bit 3 of the attribute code.

PR15 - [3?5.2E] Miscellaneous Control 1 (CNTD.)

The Character attribute bit 3, in conjunction with bits 3 and 4 of the Character Map Select register (3C5.03), determine a character map from either Plane 2 or Plane 3 as shown by the table below:

3C5.03 Bit 4	3C5.03 Bit 3	ATT Bit 3	Plane Select
0	0	X	2
1	1	X	3
1	0	0	2
1	0	1	3
0	1	0	3
0	1	1	2

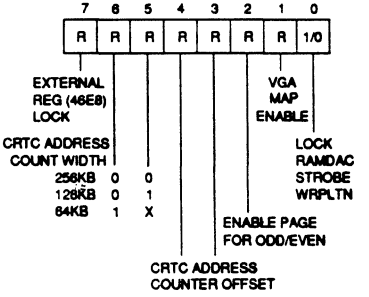
Note: The above Character Map Select functions override the functions of PR2(5) and PR2(2).

This bit must be set to 1 before loading the character maps into the video DRAM, because the addressing of the page mode character maps differs from the addressing of the default, non-page mode. However, setting this bit to 1 internally redirects all necessary addressing to make loading the character maps the same, whether in page mode or non-page mode.

Bit 1 — Display Enable Timing Select. This bit is used to select between two types of Display Enable timings available at output pin BLNKN if PR4(7)=1. If PR4(7)=0, this bit has no effect.
0 = BLNKN supplies Pre-Display Enable
Pre-Display Enable timing precedes active video by one dot clock.
1 = BLNKN supplies Display Enable. The display enable timing coincides with active video timing.

Bit 0 — Disable border. Setting this bit to 1 forces the video outputs to 0 during the interval when border (overscan) color would be active.

PR16 - [3?5.2F] Miscellaneous Control 2



PR16 - [3?5.2F] Miscellaneous Control 2 (CNTD.)

This 8 bit read/write register is unlocked by loading the value XXXXX101 into the PR10. To read this register load PR10 with 1XXX0XXX. All bits are cleared to 0 by reset.

Bit (7)

Lock External 46E8 register
Setting this bit to 1 causes EBROMN output to be forced high (Inactive) during I/O writes to port 46E8. This bit has no effect on loading the internal port 46E8.

Bit (6 : 5)

CRTC Address Counter Width
Power on reset clears these bits to 0. These two bits determine the modulus of the CRT controller's address counter, allowing its count width to be limited to 64K or 128K locations (Byte, Word, Double word). These bits may be used in virtual VGA applications containing 512K or 1024KB of video memory in which CRT controller is limited to only 64K or 128K locations. Bit PR16(6) should be set 1 to ensure VGA and EGA compatible operation of the address counter, limited to 64K locations. The following table shows details:

PR16(6)	PR16(5)	COUNT WIDTH
0	0	256K
0	1	128K
1	X	64K

Bit (4 : 3)

CRTC Address Counter Offset
Bits 4 and 3 are summed with the CRT Controller's Address Counter bits CA(17) and CA(16), respectively, and the 2-bit result defines the starting location of the displayed video buffer at one of the four 64K boundaries.

Bit 2

Enable Page Bit for Odd/Even
This bit affects addressing of memory by the system processor, if chain 2 (Odd/Even) has been selected by setting 3CF.06(1) to 1, setting 3C5.04(1) to 1, selecting extended memory, and setting 3C5.04(3) to 0 to de-select chain 4 addressing. It enables the " Page Bit for Odd/Even " [3C2(5)] to select between two pages of memory, by controlling video RAM address 0, regardless of the Memory Size bits PR1(7:6).

*** Bit** 1

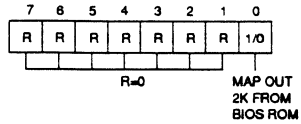
VGA Memory Mapping
Setting this bit to 1, selects 256K IBM VGA Mapping, regardless of the Memory Size bits PR1(7:6).

Bit 0

Lock RAMDAC write strobe (3C6H - 3C9H)
Programming this bit to 1 causes output WRPLTN to be forced to 1 disabling I/O writes to the video DAC registers. The DAC state register, located inside the WD90C00 is also protected from the modification but may still be read at the port 3C7. For normal operation program this bit is set to 0.

PR17 - [3?5.30] Miscellaneous Control 3

This 1-bit READ/WRITE register can be loaded only if PR10 contains XXXXX101, and can only be read if PR10 contains 1XXX0XXX.



Bit	(7:1)	Reserved.
Bit	(0)	Map out 2K of BIOS ROM Setting this bit to 1 disables access of the BIOS ROM in the system address range C6000H - C67FFH. Power on reset sets this bit to 1. Clearing this bit to 0, enables access of all 32K addresses of the BIOS ROM from C0000H - C7FFFH.

INTERNAL I/O PORTS

I / O PORT 46E8H (AT MODE - WRITE ONLY)

IBM has implemented a scheme for mapping the BIOS ROM on the PS/2 VGA display adapter card. This mapping is not done on Micro Channel based VGA implementations. The mapping is controlled through a five bit, write only register located at I/O address 46E8H. The card does not fully decode the address and it also appears at addresses 56E8H, 66E8H and 76E8H. The use of bits within the register are as follows:

D7:D5	Unused
D4	Setup
D3	Enable I/O and memory acceses
D2:D0	BIOS ROM page select (External Implementation)

The external mapping logic affects the three most significant bits of address applied to the BIOS ROM. The ROM can, therefore, be thought of as consisting of eight, 4K pages. External circuitry is required to implement the BIOS ROM page selection using bits D2:D0. The I/O port 46E8H bits (4 : 3) are provided inside the WD90C00. Bits (2 : 0) are implemented externally. WD90C00 provides EBROMN as the write strobe to external circuitry implementing BIOS ROM page mapping whenever 46E8H is accessed.

I / O PORT 102H - VIDEO ENABLE (AT AND MICRO CHANNEL MODES)

Power On Self Test (POST) sleep bit 0 is used to awaken the WD90C00 after power on in the MCA mode. Program the I/O port 102H Option Select Byte #1 to enter the set up mode. Port 102H is internal to the WD90C00. If the port 102H bit 0 is set to 1, the WD90C00 is functional. However, if the bit 0 is programmed as 0, the WD90C00 will only respond to setup read and write operations. It will disregard I/O or memory read / write operations and cause no interrupts in the set up mode. To enter the set up mode in AT bus applications, bit 4 of the partially decoded internal I/O port 46E8H is set to 1 before accessing the I/O port 102H. In MCA mode, when the CDSETUP (EION) signal pin is active low, the WD90C00 is in setup mode and port 102H can be accessed.

EXTERNAL I/O PORTS

I / O PORT 3C3H - VIDEO SUBSYSTEM ENABLE REGISTER

The Paradise WD90C00 does not internally support the 3C3H port in either the AT or Micro Channel mode. In the Micro Channel mode, bit D0 of this port is used to enable the video subsystem per IBM definition. If D0 is 1, the video I / O and memory address decoding is enabled. When D0 is 0, the video I/O and memory address is disabled. This port is set to enable (logic 1) after power on. It is not affected by the VGA sleep bit (I / O port 102H bit 0) of the Programmable Option Select (POS). When, WD90C00 is used in the Micro Channel bus designs, the read or write I/O port at 3C3H is implemented externally.

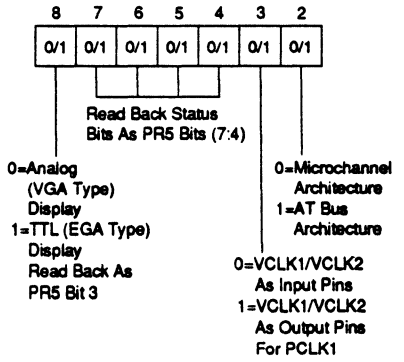
VIDEO RAMDAC PORTS

Video RAMDAC is implemented external to the WD90C00. However, the WPLTN and RPLTN signals required by the RAMDAC are provided by the WD90C00. Setting PR(16) bit 0 to a 1 forces WPLTN to a high level disabling I/O writes to the RAMDAC. Normally, the WPLTN and RPLTN signals to the RAMDAC are generated when the following I / O ports are written to or read from :

DAC ADDRESS	DAC OPERATION	DETAILS
3C8H	PEL address port (write)	Read/write port
3C7H	PEL address port (read)	Write only port
* **3C7H**	* **DAC state (read only)**	* If bits 0/1 =1, DAC in read operation When bits 0/1 =0, DAC in write operation. Bits 2-7 are reserved.
3C6H	PEL mask (read/write)	**Not to be written by application code or color look up table will be changed.**
3C9H	PEL data register (read/write)	Three successive read/write bytes.

*** NOTE : This port is internal to WD90C00.**

WD90C00 CONFIGURATION BITS CNF (8:2) - NON-READ / NON-WRITE HARDWARE PORT



Bits CNF (3:2) are latched internally at power on reset from the corresponding memory data bus pins MD (3:2) while CNF(8) is latched from MD (11). They are connected to the external pullup or pulldown resistors. Pullup resistor sets MD(3:2) to logic 1 while pull down resistor sets MD(11) to logic 1. Note, that the configuration bits (3:2) are not readable since they are latched after power up. However, the configuration register bits (8:4) are readable after power up as PR5 bits (7:3). They appear as general purpose read only status bits in the PR5 register.

CNF (8) — ANALOG/TTL DISPLAY STATUS BIT

Bit CNF(8) is latched internally at power-on-reset from memory data bus pin MD(11), provided with either a pullup or pulldown external resistor. PULLING UP MD(11) causes CNF(8) to be latched LOW. This bit controls no internal functions and READ ONLY as bit 3 of PR5 (3CF.0F). Also, CNF(8) is unaffected by writing to PR5 (3CF.0F)

0 = Analog (VGA-compatible) display is attached
1 = TTL (EGA-compatible) display is attached.

CNF (7:4) — GENERAL PURPOSE STATUS BITS

Bits CNF(7:4) are latched internally at power-on-reset from corresponding memory data bus pins MD(7:4), provided with either pullup or pulldown external resistors. These are READ ONLY bits at PR5 (3CF.0F) positions (7:4). These bits are unaffected by writing to PR5(3CF.0F). PULLING UP MD(7:4) causes CNF(7:4) to be latched LOW.

CNF (3) — VIDEO CLOCK SOURCE CONTROL

This bit cannot be written or read as I/O port. PULLING UP MD(3) causes CNF(3) to be latched HIGH. It configures WD90C00 pins VCLK1 and VCLK2 as inputs or outputs.

0 = For inputs
1 = For outputs.

When used as inputs, these pins supply alternate video dot clocks. Selection of dot clock is by an internal multiplexer. When used as outputs, VCLK1 supplies an active low load pulse for an external clock chip, during I/O writes to port 3C2. This load pulse may be inhibited by setting PR11(2)=1. VCLK2 becomes a third clock select input to the external clock chip, which supplies multiple dot clock frequencies to the VCLK0 input. If configured as outputs, setting PR15 bit 5 to 1 causes VCLK1 and VCLK2 outputs to equal bits 2 and 3 of the Miscellaneous output register at 3C2H respectively.

WD90C00 CONFIGURATION REGISTER BITS CNF(8:2) (CNTD.)

CNF (2) Bus Architecture Select
This bit cannot be written or read as I/O. PULLING UP MD(2) causes CNF(2) to be latched HIGH.

0 = Microchannel architecture
1 = AT BUS architecture

Selecting CNF(2)=0 changes the function of output pin EABUFN ,which becomes an active low bus transceiver enable signal. When low, EABUFN should externally enable data transfer across the upper 8 bits of the System Data Bus (D15:D8).

Micro Channel Interface Improvements

EABUFN is used to control high byte buffer and EDBUFN is designed to control the low byte buffer. WPLTN and RPLTN strobes to the RAMDAC for Micro Channel default cycle are also supported. No external latch is required for memory address (A19:A15) and M/-IO as in WD90C00 based designs.

Paradise Register Enhancements

PR1 PR2,PR4, PR5, and CNF registers have minimal changes to optimize VGA functions using WD90C00. They are briefly summarized below:

PR1 Bit (7,6)	Modified to allow IBM VGA mapping regardless of the memory size bits.
PR2 Bit (4,3)	Horizontal Pixel Panning in 10-dot character modes.
PR4 Bit(7)	When set to 0, it controls output signal BLNKN per VGA requirements. If programmed as 1 BLNKN output supplies display enable signal. PR15 bit 1 determines the selection of display enable timing from a choice of two settings.
PR4 Bit(6)	Select PCLK equal to VCLK. When it is set to 0, PCLK is the inverted video clock or half the dot clock frequency. If programmed as 1, PCLK is non-inverted VCLK input.
PR5 Bit(5)	If set to 1, in addition to VID(7:0), other outputs such as HSYNC, VSYNC, and BLNKN are also tri-stated.
PR5 Bit(3)	Read only CNF Bit(8) is provided as PR5 Bit 3.
CNF Bit(8)	Read only Analog (VGA compatible) display or Digital (EGA compatible) display bit.
PR15 Bit(2)	Video memory page mode read when displaying alpha numeric characters.

APPLICATION

The WD90C00 applications chapter is divided into various interfaces such as processor (AT or Micro Channel mode), video memory, RAMDAC (INMOS G171), monitor, and clock. The description and block diagrams are generic. **No attempt is made to present schematic level details.** Currently available application notes, technical briefs, and referenced literature at the end of the data sheet should supplement the information provided in this chapter. External video subsystem enable I/O port at 3C3H is briefly explained. The Figures 16 through 25 are shown along with their brief description on the subsequent pages.

The figure 16 shown below highlights the various WD90C00 Processor, memory, and I/O interfaces.

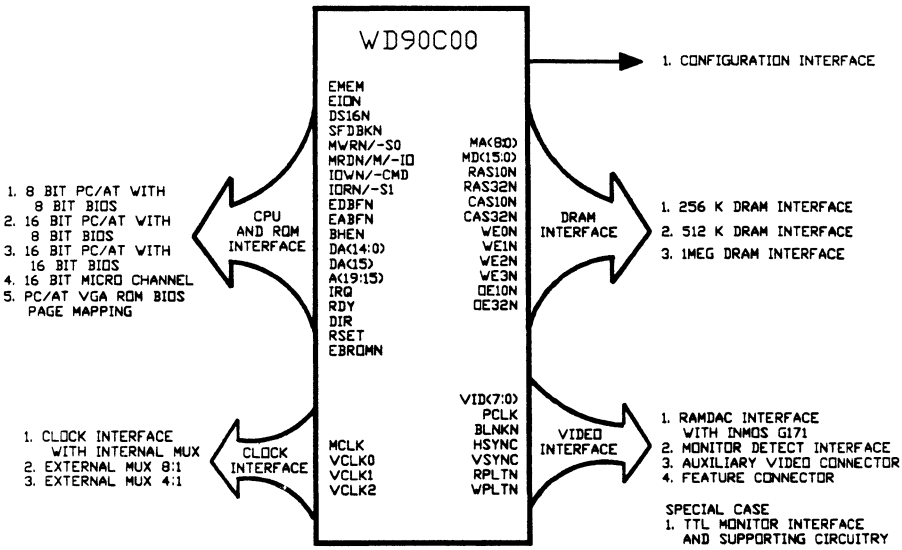
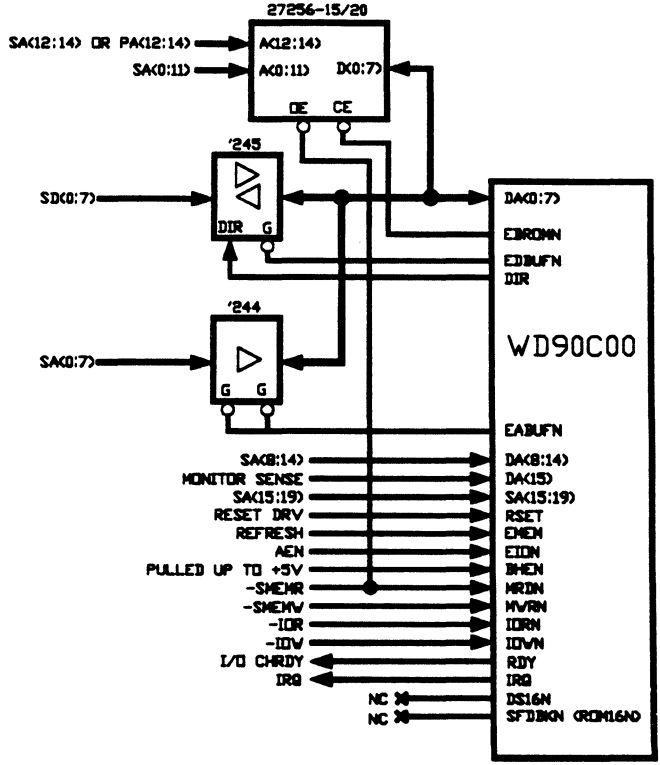


FIGURE 16

The Figure 17 shows a block diagram of the WD90C00 with 8 bit PC/AT interface using 8 bit BIOS. The system data bus SD(0:7) and address bus SA(0:19) are shown along with associated buffers and BIOS ROM. Auto monitor sense line is also included.

CONVENTION: " * " = Logic AND function, " / " = Inverted function, and " + " = Logic OR function

8 BIT PC / AT INTERFACE WITH 8 BIT BIOS



" * " NOTE: PA(12:14) CAN BE FROM PAGE MAPPING LOGIC.

FIGURE 17

The Figure 18 illustrates 16 bit PC/AT interface with 8 bit BIOS using WD90C00. The processor data bus SD(0:15), and the system address bus SA(0:19) are shown. Associated address and data bus buffers, BIOSROM, and auto monitor sense are also shown in it. Note, PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if implemented. Logic equations for upper data bus buffer gate EDBF1.

/EDBF1 = /EDBUFN * EBROMN * /SMEMW * /SBHE * /DS16N
+ /EDBUFN * EBROMN * /SMEMR * /SBHE * /DS16N

16 BIT PC / AT INTERFACE WITH 8 BIT BIOS

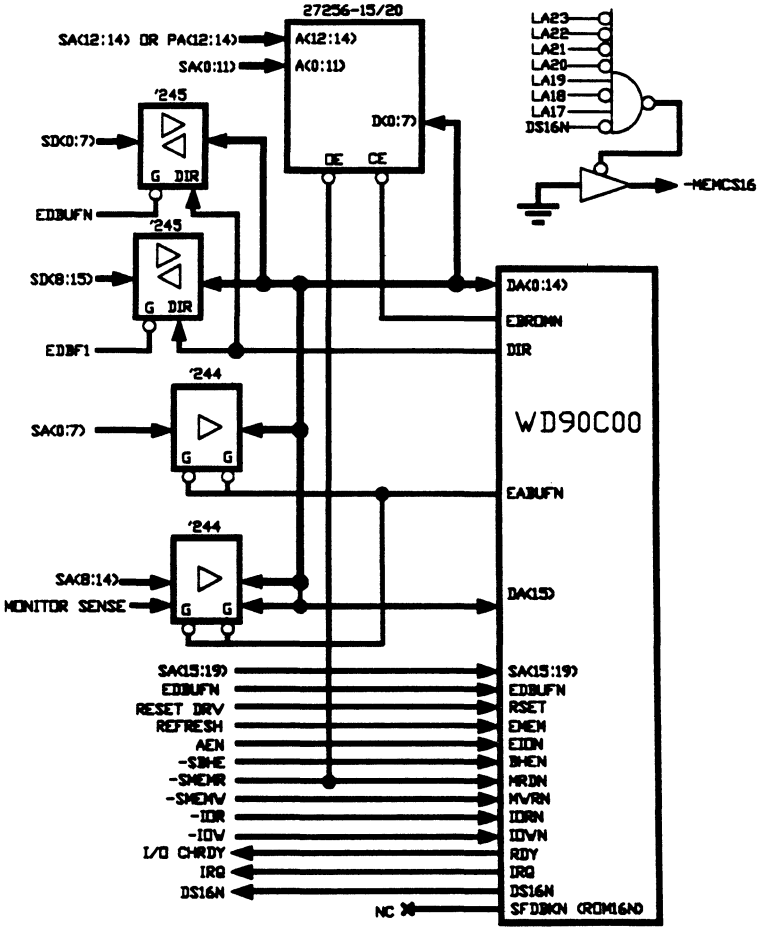


FIGURE 18

The Figure 19 describes 16 bit PC/AT interface with 16 bit BIOS ROM implementation using WD90C00. The system data bus SD(0:15), address bus SA(0:19), address and data bus buffers, and auto monitor sense input is presented. The (16KX8) upper and lower byte EPROMS, output enable lines (EROM0 / EROM1), and EPROM buffer (Gated by EDBFX) are shown. Note that PA(12:14) to BIOS ROM can be derived from the BIOS page mapping logic if it is implemented. Also, -MEMCS16 implementation limits addition of 8 bit cards with memory addresses at the locations of segment C000H for 128 KB memory space. Boolean equations for some of the important signals are listed:

/EROM0 = /EBROMN * /SMEMR * /SA0

/EROM1 = /EBROMN * /SBHE * /SMEMR * /ROM16N + /EBROMN * SA0 * /SMEMR * ROM16N

/EDBFX = /EBROMN * SA0 * /SMEMR * ROM16N

/EDBUF1 = /EDBUFN * /SMEMW * /SBHE * /DS16N + /EBROMN * /SMEMR * /SBHE * /ROM16N
+ /EDBUFN * /SMEMR * /SBHE * /DS16N * EBROMN

Figure 19 is illustrated on the subsequent page.

16 BIT PC / AT INTERFACE WITH 16 BIT BIOS

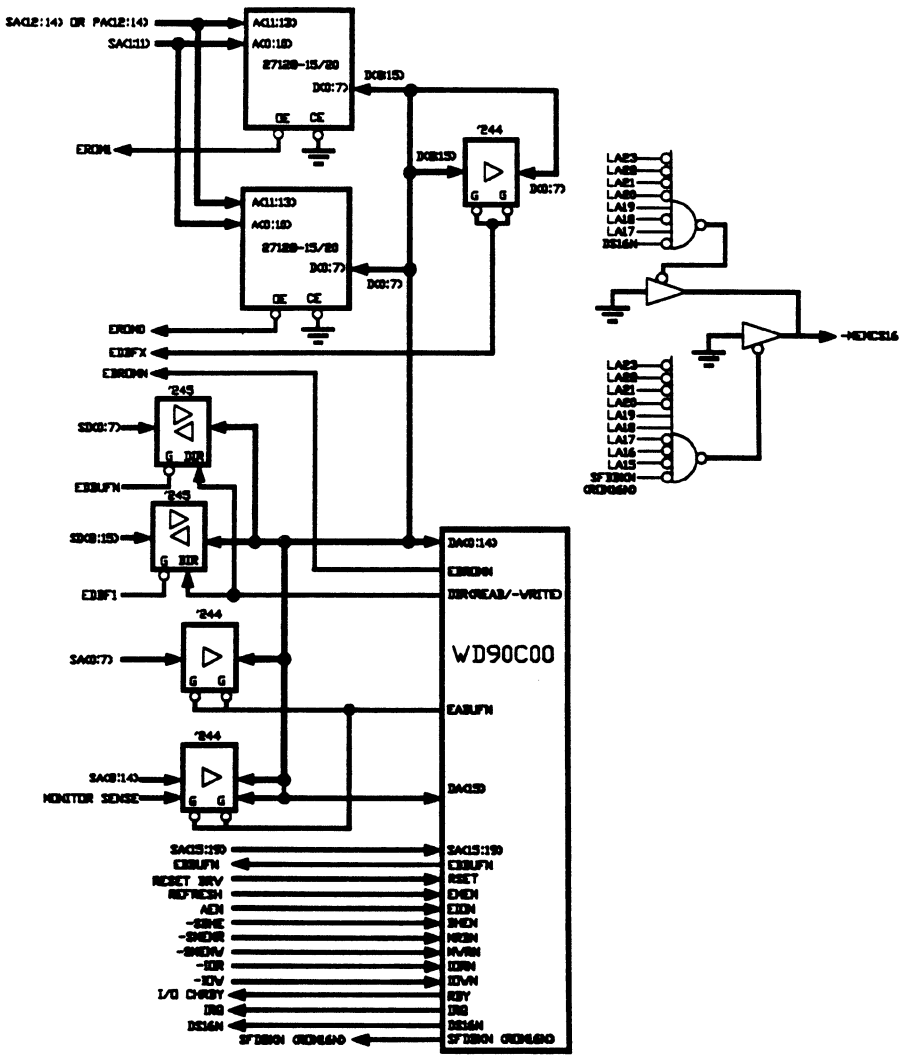


FIGURE 19

The Figure 20 indicates WD90C00 and 16 bit Micro Channel interface. The system data bus upper byte bits D(8:14) and lower data bus byte D(0:7) are sampled and buffered for the WD90C00 input pins DA(0:14). Likewise, system address byte upper bits A(8:14) and lower address byte A(0:7) are buffered and gated to the WD90C00 input pins DA(0:14). The most significant system address bits A(15:19) are latched and sent to the WD90C00. The monitor sense input buffer and D15 are gated into the DA15 input of the WD90C00. The Micro Channel bus control signals provide the timing and are gated by the appropriate logic blocks to the WD90C00. Associated Boolean equations are shown below:

EMEM = 3C3.D0 * /A23 * /A22 * /A21 * /A20 * (M/-IO) * (MADE24) +
3C3.D0 * /(M/-IO)

Figure 20 is drawn on the following page.

16 BIT MICRO CHANNEL INTERFACE

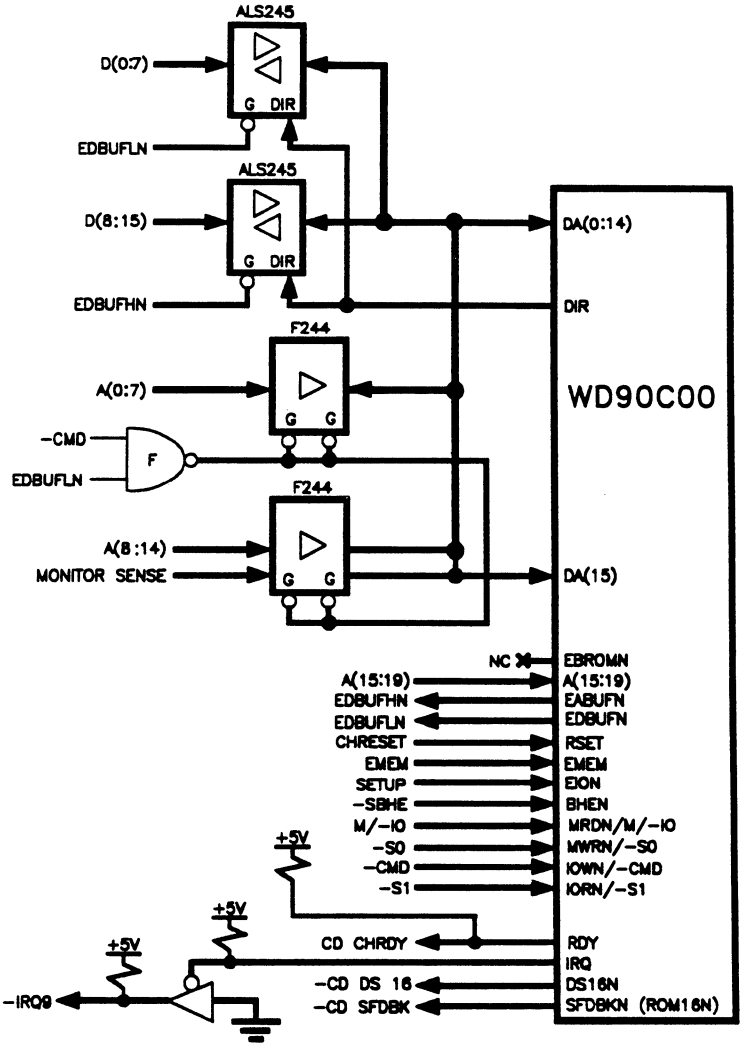


FIGURE 20

The Figure 21 presents WD90C00 with 1024 KB video memory organization using four 256KB maps. Each 256KB map is made from two (256KX4) DRAMs. The built in DRAM controller provides all the memory control signals and refresh cycles. The WD90C00 also supports 256KB, or 512KB video memory organization using (64KX4) DRAM modules.

1 MEGABYTE DRAM CONFIGURATION

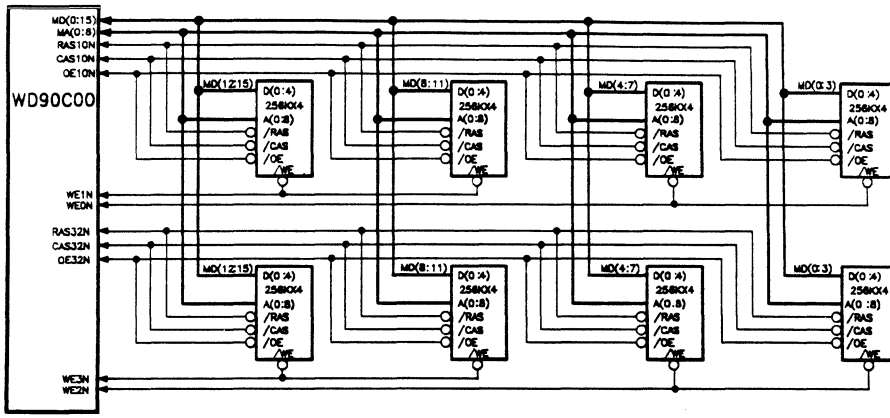
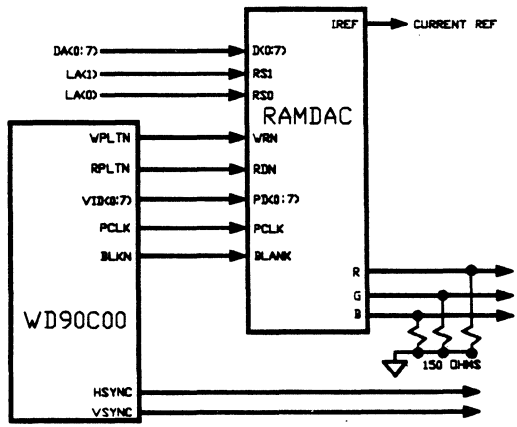


FIGURE 21

The Figure 22 illustrates the WD90C00 and RAMDAC (INMOS G171) interface block diagram for analog or TTL monitors.

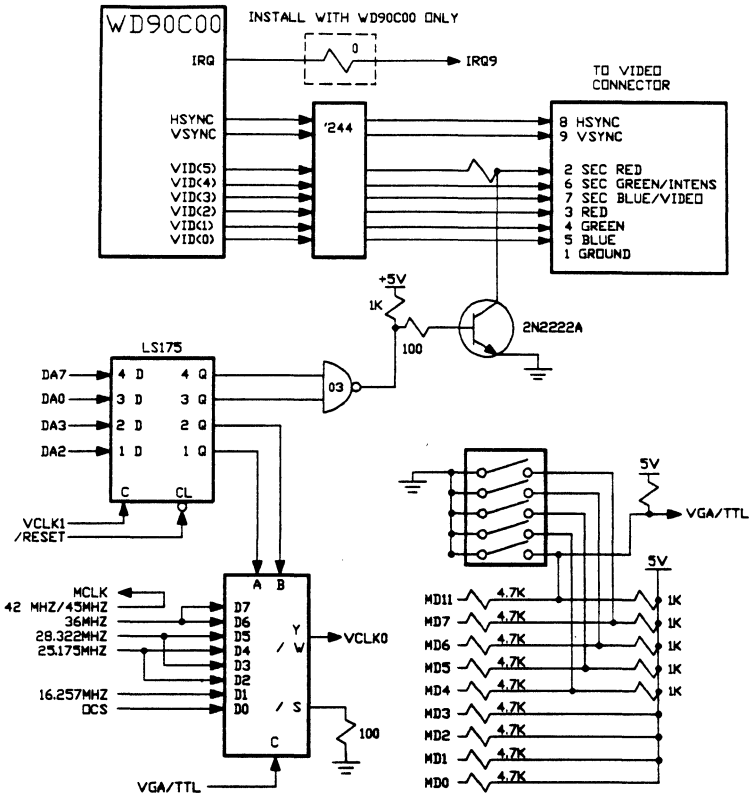
RAMDAC (INMOS G171) INTERFACE



NOTE: LA(1), LA(0) ARE LATCHED ADDRESSES.
DA(7:0) ARE MULTIPLEXED DATA BITS.

FIGURE 22

The Figure 23 shows the WD90C00 and TTL monitor connections.



NOTE :

1.0 VGA /TTL switch may be used to disable HSYNC and VSYNC for Analog or TTL Video connector.

2.0 MD(12:15) may also be connected as the EGA switches if desired. See Paradise register and Pin out sections for more details.

3.0 For AT applications using WD90C00, install the IRQ9 resistor.

FIGURE 23

The Figure 24 presents WD90C00 with external oscillators at the clock pins configured as inputs.. The clock selection is determined by register 3C2H bit 3 and bit 2. It is described by the table below:

3C2H Bit 3	3C2H Bit 2	CLOCK SELECTION
0	0	VCLK0
0	1	VCLK1
1	X	VCLK2

The Configuration register Bit 3 (MD3) should be tied low to make the WD90C00 signal pins (VCLK1, VCLK2) inputs.

CLOCK INTERFACE

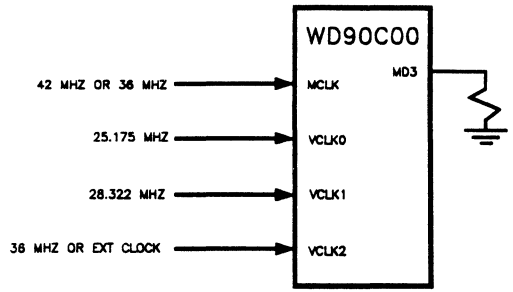


FIGURE 24

The Figure 25 illustrates WD90C00 pins VCLK1 and VCLK2 configured as outputs. This is done when the Configuration register Bit 3 (MD3) is tied high. The figure also shows how the VCLK1 and VCLK2 signals can be used to control external input clock multiplexor to select 1 of 8 possible clock frequencies.

EXTERNAL MULTIPLEXING OF THE VIDEO CLOCKS

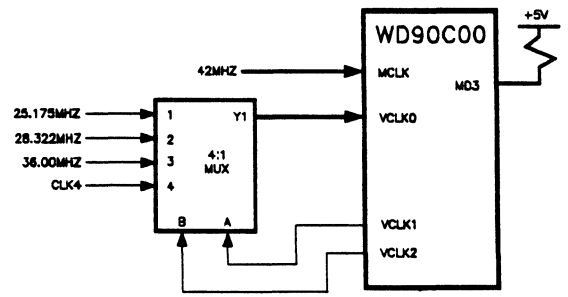


FIGURE 25

WD90C00 POWER UP CONFIGURATION

The WD90C00 uses the MD(0:7) and MD(11:15) input pins to configure itself at power up/reset. These lines will, upon power up/reset, latch logic values depending on whether there is a pull up or a pull down resister on them. PR1(1:0), PR11(4:7), and CNF(2:8) are the internal registers that are configured on power up. CNF(3:2) and PR11(4:7) will latch a noninverted value (pull up resister = 1) into it and the others will latch an inverted value. For more details see the Paradise register and Pin out sections.

PR1 bit 0 will latch the inverted value of MD(0). A value of 1 (pulled down) will map out the decoding of the BIOS ROM by the WD90C00. A value of 0 will map it in.

PR1 bit 1 will latch the inverted value of MD(1). A value of 1 (pulled down) will signify to the WD90C00 that the ROM BIOS data path is 16 bits. The WD90C00 will bring SFDBKN active low in AT mode (static signal) and SFDBKN can be used to externally generate -MEMCS16 (off the AT Bus) for 16 bit ROM accesses. In Micro Channel Mode, SFDBKN changes function to be the -CD SFDBK signal output and DS16N is driven active when PR1(1) is set and a valid ROM BIOS address is decoded.

PR11(4:7) bits will latch the EGA switch settings (SW4:SW1) after power up. A pull up resistor will set the appropriate PR11 register bit (4:7) to a logic 1.

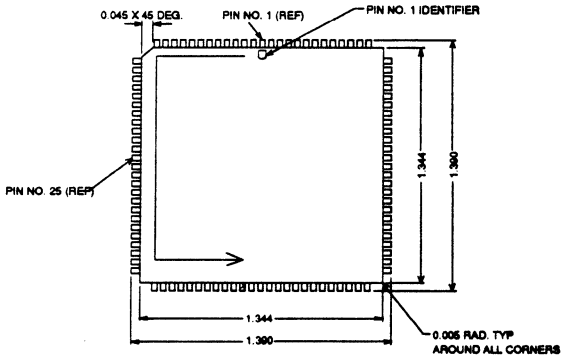
CNF(2) will latch the noninverted value of MD(2). A value of 1 (pulled up) will configure the WD90C00 for IBM PC/XT/AT architecture. A value of 0 will configure the WD90C00 for IBM PS/2 Micro Channel Architecture. WD90C00 Signal Pins and the interface will change functions depending on this value.

CNF(3) will latch the noninverted value of MD(3). This bit configures the WD90C00 pins VCLK1 and VCLK2 as inputs or as outputs. A value of 0 (pulled down) will configure these pins as inputs and a value of 1 sets them as outputs. When used as inputs, these pins when connected to clock crystals supply the video dot clock. The selection of these clocks, through an internal multiplexer and along with VCLK0, depends on the value of 3C2H bits 2 and 3. When used as outputs, VCLK1 becomes an active low load pulse when 3C2H is written to with data. VCLK2 becomes the static value determined by the state of PR2 bit 1. When these signal pins are selected as outputs, the internal multiplexer is locked to select the VCLK0 input pin as the video dot clock.

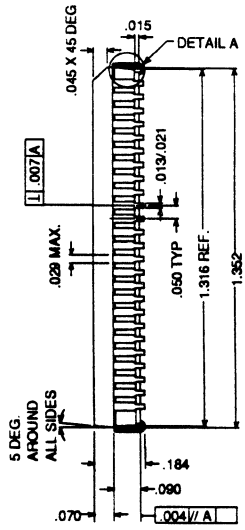
CNF(7:4) will latch the inverted value of MD(7:4). These bits can be read through Paradise Register PR5 bits 7 to 4. These are general purpose bits that may be used by the video BIOS. If reserved or unused by the BIOS, they are available to the application software.

CNF(8) will indicate that a TTL display or an analog monitor is present in the video subsystem. A Pull up resistor on MD(11) causes CNF(8) to be latched 0 indicating that VGA compatible analog display is in the video subsystem.

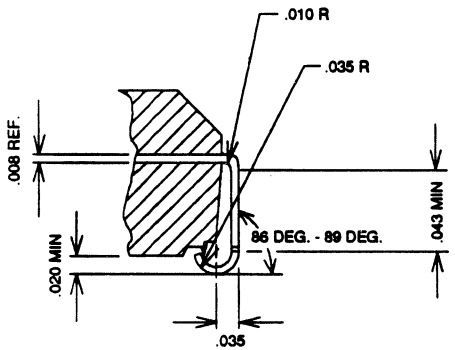
100 PIN PLCC PACKAGE



(TOP VIEW)



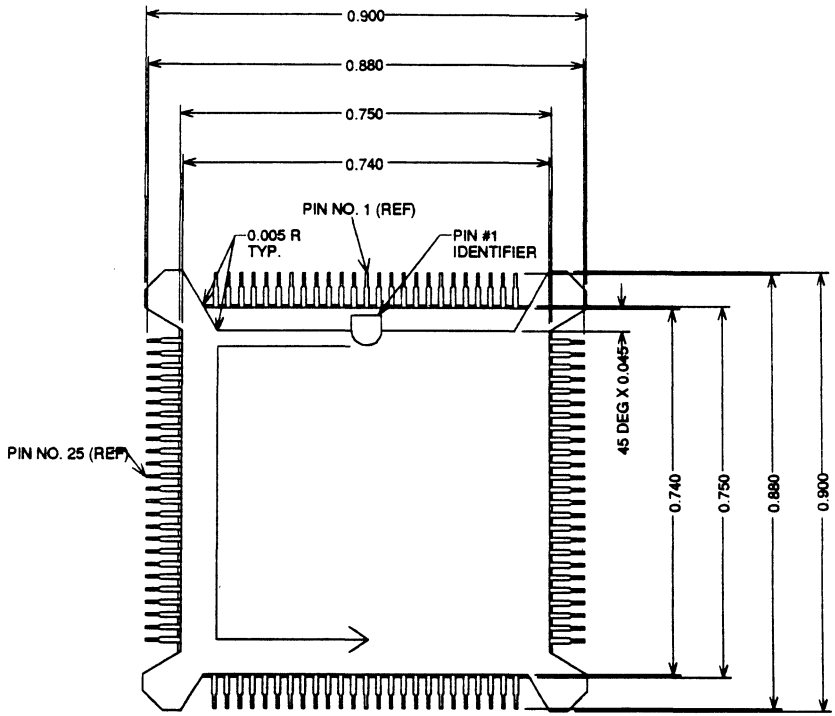
DETAIL A



NOTE : ALL DIMENSIONS ARE IN MILLIMETERS.

FIGURE 26

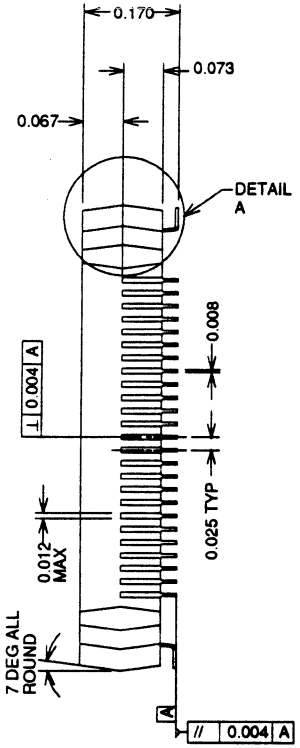
100 PIN JEDEC PLASTIC FLAT PACKAGE (PFP)



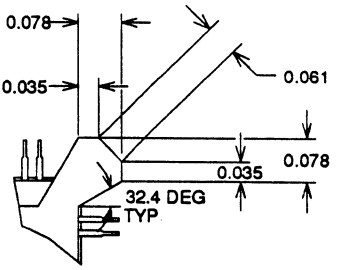
TOP VIEW

FIGURE 27

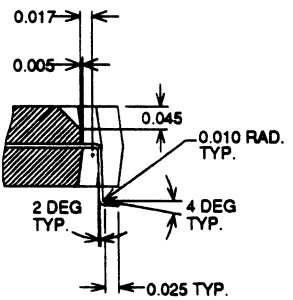
100 PIN JEDEC PLASTIC FLAT PACKAGE (PFP)



SIDE VIEW



BUMPER DETAIL



DETAIL A

FIGURE 28

REFERENCES

A list of references for generating the WD90C00 data sheet information is shown below:

IBM Personal Computer Hardware User Guide	(IBM # 6322510)
IBM Personal Computer XT Hardware User Guide	(IBM # 6322511)
IBM Personal Computer AT Hardware User Guide	(IBM # 6280066)
IBM Personal System 2 Model 30 Hardware User Guide	(IBM # 68x2230)
IBM Personal Computer AT Technical Reference Manual	(IBM # 6280070)
IBM Personal System 2 Model 30 Technical Reference Manual	(IBM # 68x2201)
IBM PC Options & Adapters Technical Reference Manual	(IBM # 6322509)
IBM Personal System 2 BIOS Reference Manual	(IBM # 68x2260)
Personal Computer Reference Manual	(IBM # 6025005)
AT &T Video Display Controller VDC 750 / VDC 600 Installation Guide	
Hercules Graphics Card Owner's Manual	
Paradise OEM Technical Publication Manual	

The customers are urged to refer to the manuals listed above and supplement their knowledge from **other** books and literature available in the market.

WD90C00

Western Digital Imaging/Paradise Systems
800 E. Middlefield Road
Mountain View, CA 94043
Tel: 415/960-3353 Fax: 415/968-1974

Important Notice

Paradise Systems, Inc., reserves the right to make changes to circuit or specifications in order to improve reliability, design, or function without prior written notice.

Paradise Systems, Inc., is not responsible and does not assume any liability for claims of patent infringement arising out of the use or application of any Paradise product in combination with other devices or computer programs.

Paradise Systems, Inc., does not assume any liability arising out of application or use of the product or circuit described herein and does not convey any license under its present patent rights or the rights of others.

Paradise Systems, Inc. provides no warranty for the use of its products and assumes no liability for any errors which may appear in this document.

Version: PRELIM.

July 31, 1989

PDS 100 800