X2443
X2443I

256 Bit Serial Nonvolatile Static RAM

16x16 Bit Serial NOVRAM*

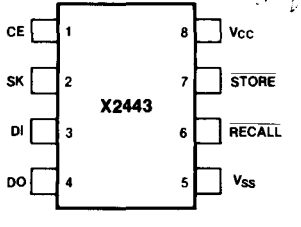
- **Ideal for use with Single Chip Microcomputers**
  - **Static Timing**
  - **Minimum I/O Interface**
  - **Minimum Support Circuits**
- **Software and Hardware Control of Nonvolatile Functions**
  - **Maximum Store Protection**
- **TTL Compatible**
- **16x16 Organization**
- **Reliable N-Channel Floating Gate Technology**
- **Single 5V Supply**
- **Low Power Dissipation**
  - **Active Current: 15mA Typ.**
  - **Store Current: 8mA Typ.**
  - **Standby Current: 6mA Typ.**
  - **Sleep Current: 5mA Typ.**
- **8-Pin Mini-Dip**
  - **Low Cost**
  - **Compact**

The X2443 is a 256-bit Xicor NOVRAM memory fabricated in Xicor's proven NMOS technology. The device is organized as 16 words of 16 bits each. Serial access allows the use of a cost-effective 8-pin package, making the X2443 ideal for cost sensitive and compact design applications. Each bit of the static RAM is overlayed with a bit of nonvolatile electrically erasable PROM (E^2PROM). Data can be transferred back and forth between the two memories either by instructions sent from the processor over the serial interface, or by toggling the external $\overline{\text{STORE}}$ and $\overline{\text{RECALL}}$ inputs. Nonvolatile data is retained in the E^2PROM, while independent data can be accessed and updated in the RAM.

High voltage pulses and supplies are not required. A single 5V supply is the only power source needed, and all signals are TTL compatible.

The X2443 offers many modes of operation in order to minimize the power consumption of the chip. The chip is placed in the STANDBY mode whenever it is deselected, and is placed in the SLEEP mode whenever the sleep instruction is executed. The chip will automatically return active from STANDBY when selected by CE, and will exit the SLEEP mode when the next RECALL operation is performed, either by the RCL instruction or by taking the $\overline{\text{RECALL}}$ input low.

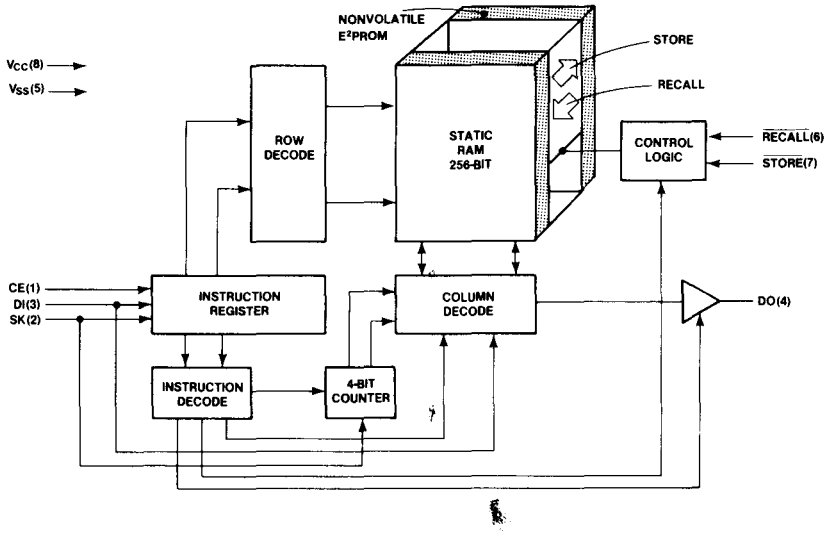
PIN CONFIGURATION
8-PIN DIP .300"



PIN NAMES

CE	CHIP ENABLE
SK	SERIAL CLOCK
DI	SERIAL DATA IN
DO	SERIAL DATA OUT
$\overline{\text{RECALL}}$	RECALL
$\overline{\text{STORE}}$	STORE
V_{CC}	+5V
V_{SS}	GROUND

FUNCTIONAL DIAGRAM X2443 (16x16)



*NOVRAM is Xicor's nonvolatile static random access memory device.

June 1983, Stock No. 200-023

XICOR, Inc., 851 Buckeye Court, Milpitas, California 95035 (408)946-6920 TWX910-379-0033

ABSOLUTE MAXIMUM RATINGS*

Temperature Under Bias X2443	−10°C to +85°C
X2443I	−65°C to +125°C
Storage Temperature	−65°C to +150°C
Voltage on any Pin with Respect to V_{SS}	−1.0V to +6V
D.C. Output Current	5mA

***COMMENT:**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC OPERATING CHARACTERISTICS

X2443 T_A = 0° C to +70° C, X2443I T_A = −40° C to +85° C.
V_{CC} = +5V ± 5% unless otherwise specified. All voltages with respect to V_{SS}.

Symbol	Parameter	Limits			Units	Conditions
		Min.	Typ.(1)	Max.		
V_{CC}	Operating Voltage	4.75	5	5.25	V	
I_{CC}	Power Supply Current		15		mA	Inputs = 5V, $I_{I/O}$ = 0mA
I_{SL}	Sleep Current		5		mA	
I_{SB}	Standby Current		6		mA	CE = 0.4V
I_{STO}	Store Current		8		mA	
I_{LI}	Input Load Current		.1	10	μA	V_{IN} = 0V to 5.5V
I_{LO}	Output Leakage Current		.1	10	μA	V_{OUT} = 0V to 5.5V
V_{IL}	Input Low Voltage	−1.0		.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC} + 0.5	V	
V_{OL}	Output Low Voltage			.4	V	I_{OL} = 2.4mA
V_{OH}	Output Low Voltage	2.4			V	I_{OH} = −.8mA

CAPACITANCE (2)

T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V

Symbol	Test	Max.	Unit	Conditions
C_O	Output Capacitance	8	pF	$V_{I/O}$ = 0 V
C_{IN}	Input Capacitance	6	pF	V_{IN} = 0 V

A.C. CONDITIONS OF TEST

Input Pulse Levels	0 Volt to 3.0 Volt
Input Rise and Fall Times	10 nsec
Input and Output Timing Levels	1.5 Volts
Output Load	1 TTL Gate and C_L = 100 pF

NONVOLATILE OPERATIONS(3)

Operation	$\overline{\text{STORE}}$	$\overline{\text{RECALL}}$	INST	WRITE ENABLE LATCH	Previous $\overline{\text{RECALL}}$
Hardware Recall	1	0	NOP	X	X
Software Recall	1	1	RCL	X	X
Hardware Store	0	1	NOP	SET	True
Software Store	1	1	STO	SET	True

Notes:
(1) Typical values for T_A = 25°C and nominal voltage
(2) This parameter is periodically sampled and not 100% tested.
(3) Positive logic is used, i.e., a low voltage represents a logic "0". A high voltage represents a logic "1". NOP designates when the X2443 is not currently executing an instruction.

AC CHARACTERISTICS

X2443 T_A = 0° C to +70° C, X2443I T_A = −40° C to +85° C.
V_{CC} = +5V ± 5% unless otherwise specified.

Symbol	Parameter	Limits			Units
		Min.	Typ.(1)	Max.	
F_{SK}	SK Frequency	0.0		1.0	MHz
t_{SKH}	SK Positive Pulse Width	0.4			μs
t_{SKL}	SK Negative Pulse Width	0.4			μs
t_{DS}	Data Setup Time	0.4			μs
t_{DH}	Data Hold Time	0.2			μs
t_{PD}	SK to Data Valid			0.75	μs
t_Z	Chip Enable to Output High Z			1.0	μs
t_{CES}	Chip Enable Setup	0.8			μs
t_{CEH}	Chip Enable Hold	0.4			μs
t_{CDS}	Chip De-select	0.8			μs

CONTROL/DATA TIMING

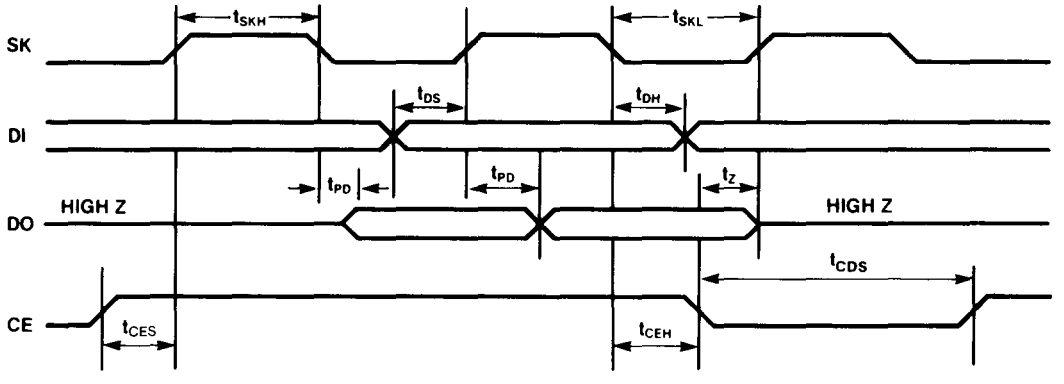


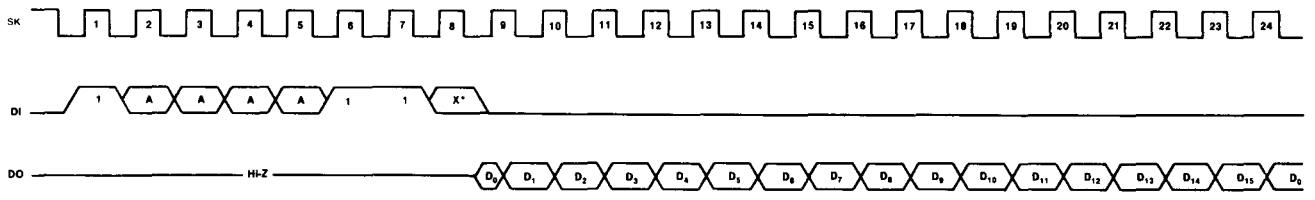
Diagram 1

—CE must be taken low between instructions.
—Once the chip has been selected with CE, the first logic "1" clocked by the rising edge of SK into the DI input marks the beginning of an instruction. All previous logic '0's are ignored.

INSTRUCTION SET		
Instruction	Format, I_2 I_1 I_0	Operation
WRDS (Diagram 5)	1XXXX000	Reset Write Enable Latch (Disables writes and stores)
STO (Diagram 5)	1XXXX001	Store RAM data in E^2PROM
SLEEP (Diagram 5)	1XXXX010	Enter SLEEP Mode
WRITE (Diagram 3)	1AAAA011	Write Data into RAM Address AAAA
WREN (Diagram 5)	1XXXX100	Set Write Enable Latch (Enables writes and stores)
RCL (Diagram 5)	1XXXX101	Recall E^2PROM Data into RAM
READ (Diagram 2)	1AAAA11X	Read Data from RAM Address AAAA

X = Don't Care
A = Address Bit

DATA OPERATIONS



*Bit 8 of Read Instructions is Don't Care

Diagram 2. RAM Read

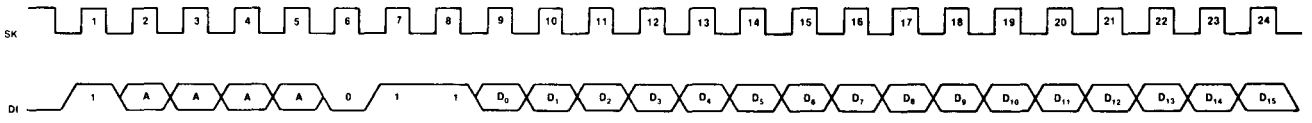


Diagram 3. RAM Write

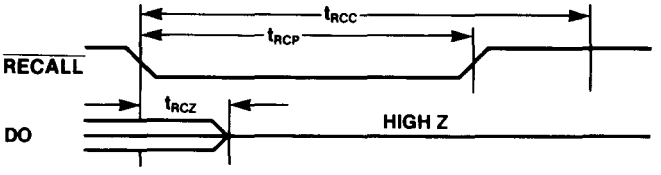


Diagram 4. Hardware Recall

ARRAY RECALL CYCLE

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
t_{RCC}	Recall Cycle Time	2.5			μs
t_{RCP}	Recall Pulse Width	1.0			μs
t_{RCZ}	Recall to Output High Z			0.5	μs

NUMBER OF RECALL CYCLES:
After data has been stored properly in the nonvolatile memory (E^2PROM), the NOVRAM is expected to recall this data an unlimited number of times during the lifetime of the device.

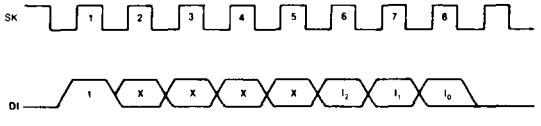


Diagram 5. Non-Data Operations

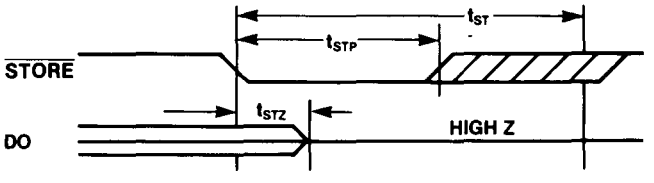


Diagram 6. Hardware Store

STORE CYCLE

Symbol	Parameter	Limits			Units
		Min.	Typ.	Max.	
t_{ST}	Store Time			10	ms
t_{STD}	Store Pulse Width	0.1			μs
t_{STZ}	Store to Output High Z			0.5	μs

NUMBER OF STORE CYCLES:
NOVRAMs are specified to perform a minimum of 10,000 store cycles. Each cell is specified to complete 1000 data changes per bit.

RECALL OPERATION

The RECALL operation transfers the data currently in the nonvolatile E^2PROM into the RAM section of the X2443. The RECALL operation can be initiated either from the $\overline{RECALL}$ input being driven low, or the execution of the RCL instruction. Once initiated, all other operations are inhibited, and the previous data in the RAM is overwritten. If the chip had been previously placed in SLEEP mode, the RECALL operation will leave the chip in Active mode. The first RECALL after power-on also sets an internal latch, which must be set in order to do subsequent STORE operations.

STORE OPERATION

The STORE operation transfers the data currently in the X2443 RAM into the E^2PROM. The data currently in the E^2PROM is overwritten. The STORE operation can be initiated from either the $\overline{STORE}$ input being driven low, or the execution of a STO instruction. In order to protect against inadvertent stores which might destroy important information in the E^2PROM, several conditions must be true in order to perform the STORE operation.

1. STO Command issued or $\overline{STORE}$ driven low
2. Write Enable Latch must be set
3. Previous Recall Latch must be set

The STORE operation inhibits all other operations, and any attempt to read the part during a STORE operation will result in the DO output remaining in the high impedance state. The STORE operation clears the Write Enable latch. If the X2443 is performing a WRITE operation, the $\overline{STORE}$ input is ignored until CE is taken low.

WRITE/STORE PROTECTION

WRITE and STORE protection is provided by the X2443 internal Write Enable Latch. This latch must be set in order to do either a WRITE or STORE operation. This latch can be set with the WREN instruction and reset with the WRDS instruction. The Write Enable latch is automatically reset after a STORE operation is performed.

READ/WRITE MEMORY

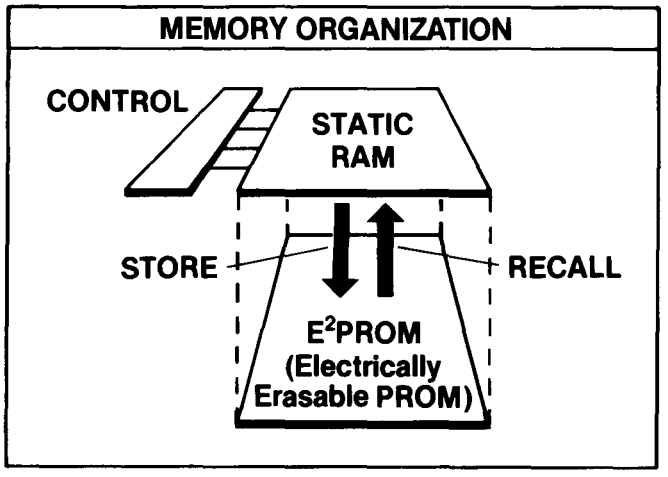
The RAM in the chip is accessed by the READ and WRITE instructions. These instructions include a 4-bit address, which selects which word is to be written or read. After the instruction and address have been sent, serial data (16-bits) will be either output on the DO pin in the case of a read, or input through the DI pin in the case of a write. The X2443 design allows the connection of the DI and DO lines together to form a bi-directional serial interface.

The least significant bit of the READ instruction is a don't care to enhance the use of the shared I/O capability of the DI and DO lines.

SLEEP MODE

The SLEEP mode places the X2443 into a low power quiescent mode. Internal RAM is turned off, and any data currently in RAM becomes invalid. Data is maintained in E^2PROM, as it was saved in the last STORE operation. The SLEEP mode can only be exited by a hardware or software initiated RECALL operation.

MEMORY ORGANIZATION



ORDERING INFORMATION

Part Number	Temperature Range	Memory Organization
X2443P	0°C to 70°C	16x16
X2443PI	– 40°C to 85°C	16x16

PACKAGING INFORMATION