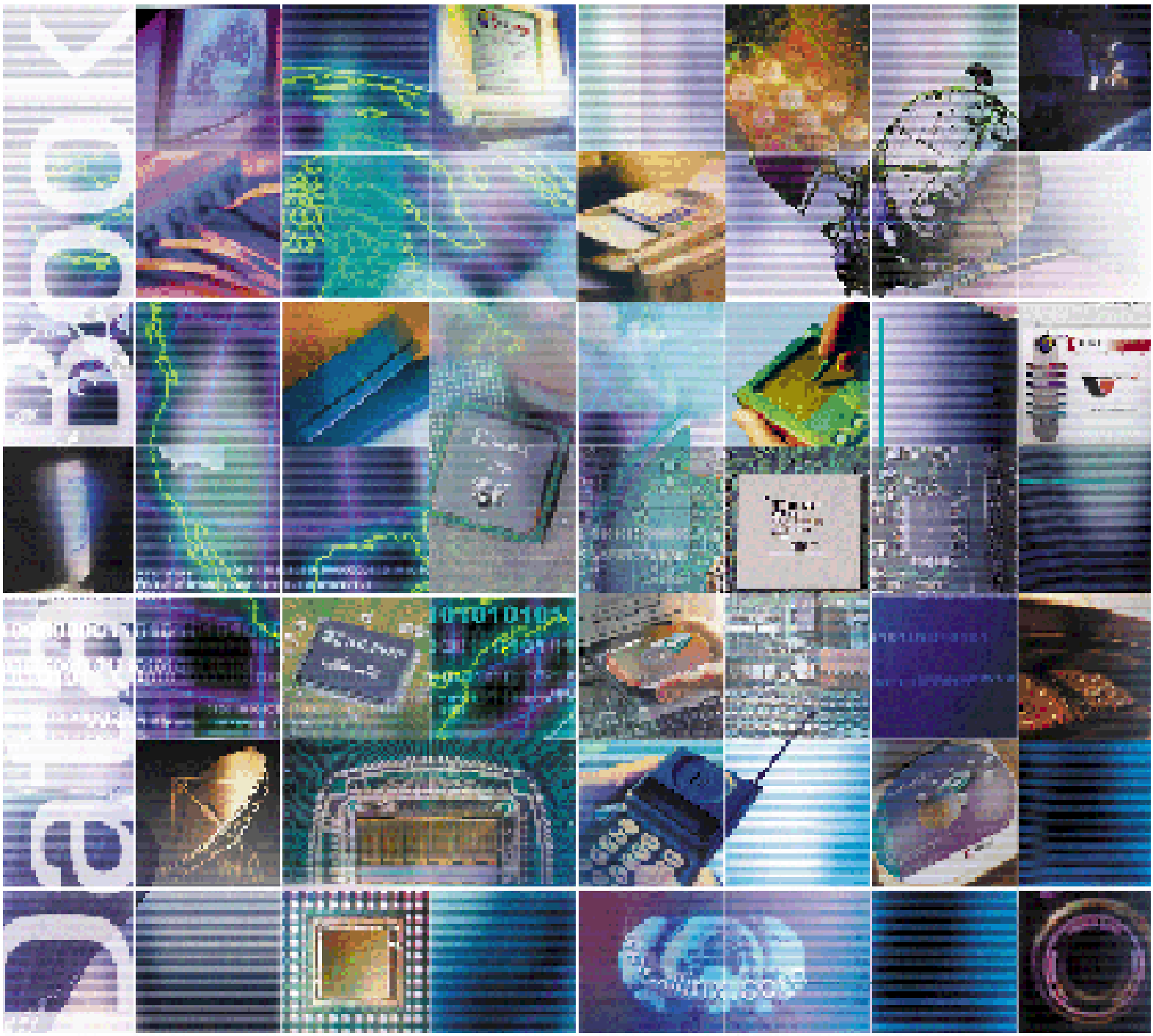
The Programmable Logic

Data Book 2000



XILINX®

Important Information You Need to Know About This Data Book

Veteran users of Xilinx programmable logic solutions will notice a number of significant changes in this latest edition of the Xilinx Data Book. As always, our goal is to provide you with the most accurate and timely information about Xilinx products.

However, as the world moves at "Internet speed" and the pace of product innovation accelerates, some of the information you see bound between these covers may well have become outdated as the pages were being printed.

The Web Site is Always Current

Whenever Xilinx updates technical data on its products, the first place that information goes is to the Xilinx web site. To find the absolutely latest technical product data from Xilinx, simply go to the following Web address:

www.xilinx.com/partinfo/databook.htm

DataSource CD-ROM

In addition to the challenge of providing you with timely information, there is the problem of sheer bulk associated with printing data books like this one. Over the last few years, Xilinx has introduced a record number of new products, and today Xilinx has the largest product portfolio in the programmable logic industry. As a result, the number of new Xilinx devices and software products continues to grow steadily—to the point that it is impossible to fit complete data sheets on all Xilinx products physically into a single usable volume.

Rather than attempting to publish multiple printed volumes, we have provided the **Xilinx DataSource CD-ROM,** located in the front sleeve of this data book. The CD-ROM contains complete data sheets on all Xilinx products currently in production, as well as all application notes.

Registration Advantage

Please take a moment to compete the registration section on the CD-ROM. This will ensure that you automatically begin to receive quarterly updates of the CD-ROM as they become available. For example, the CD-ROM in this edition of the Xilinx Data Book has an September 2000 expiration date. By registering, you will receive the next updated CD-ROM free of charge and without any other action required on your part.

Instructions for Using the CD-ROM

The CD-ROM contains a viewer called WebCD. WebCD operates as a plug-in to standard browsers, providing a floating window that allows for:

- Selecting bookmarks
- Searching files
- Opening the equivalent file on xilinx.com (if connected to the Internet) for real-time updates

New Content

- A video from Wim Roelandts, our CEO, about Xilinx focus
- Multimedia presentation on Virtex™-E, Spartan™-II, and XPLA3
- The new 2000 Data Book
- Service Pack (the latest version) for the PC
- Virtex-E, Spartan-II, and XPLA3 data sheets
- Many new application notes

NOTE: *Because of production and implementation time, data on the CD is at least five weeks old. For the very latest data, go to* ***www.xilinx.com.***

Installation Instructions for the CD-ROM

To enable search, multimedia, and custom bookmarks for the CD-ROM, install the WebCD™ Viewer, which works with Microsoft or Netscape browsers to provide a familiar graphical interface. The WebCD Viewer provides search capabilities and Smart Caching™, which automatically detects an internet connection and serves updated files from the xilinx.com web site.

Notes:

WebCD runs on Windows platforms by selecting the setup file, and on UNIX platforms when you open **file:/cdrom/datsource/docs/home.htm** from your web browser. Apple is not supported.

The WebCD setup program first looks for an installed browser and installs Microsoft Internet Explorer if no browser is found. The WebCD Viewer works automatically as a plug-in to Netscape Navigator. A DataSource CD icon gets added to the desktop, simplifying access to the CD.

Most material on the CD-ROM and on the Xilinx Web site is in **Adobe Acrobat (PDF)** format. If your browser is not already set up to view Acrobat files, you will need to download and install the Acrobat Reader from the Adobe Web site (**www.adobe.com**). Click the “Get Acrobat Reader” icon on the Adobe home page and follow the download / installation instructions.

To install WebCD Viewer under Windows NT or Windows 95/98/2000:

1. *Make sure you exit any browsers before beginning the installation.*
2. Exit all other open applications and insert the CD-ROM into your CD-ROM drive.
3. The WebCD Viewer’s setup program usually begins automatically on insertion of the CD-ROM in Windows 95/98/NT machines. If the setup program does not start by itself, proceed with steps 4 and 5. Otherwise, skip to step 6.
4. *If setup does not start by itself:* Click the **Start** button and select **Run**.
5. Type your CD-ROM drive letter, followed by **:\setup** (e.g., **D:\setup**). Then click **OK**.
6. Follow the on-screen prompts to complete the installation.

Other Operating Systems:

Point your own web browser at the file **index.htm** in the root directory of the CD-ROM.

For more installation details, see the **readme.txt** file in the root directory of the CD-ROM.

For the latest Xilinx information, go to **www.xilinx.com**.

The Programmable Logic Data Book

Xilinx Home Page (WWW):		http://www.xilinx.com/ (“Answers” Database, File Download)
XDOCS E-mail Document Server:		xdocs@xilinx.com send E-mail with help in the header
Application Service Centers		
North America	Hotline:	1-408-879-5199 (USA, Xilinx headquarters) 1-800-255-7778 (North America)
	Fax:	1-408-879-4442
	E-mail:	hotline@xilinx.com
United Kingdom	Hotline:	(44) 1932-820821
	Fax:	(44) 1932-828522
	E-mail:	ukhelp@xilinx.com
France	Hotline:	(33) 1-3463-0100
	Fax:	(33) 1-3463-0959
	E-mail:	frhelp@xilinx.com
Germany	Hotline:	(49) 89-93088-130
	Fax:	(49) 89-93088-188
	E-mail:	dlhelp@xilinx.com
Japan	Hotline:	(81) 3-3297-9163
	Fax:	(81) 3-3297-0067
	E-mail:	jhotline@xilinx.com
Korea	Hotline:	(82) 2-761-4277
	Fax:	(82) 2-761-4278
	E-mail:	korea@xilinx.com
Hong Kong	Hotline:	(85) 2-2424-5200
	Fax:	(85) 2-2424-7159
	E-mail:	hongkong@xilinx.com
Software Authorization and Licensing:		1-800-624-4782
On-Line Authorization:		www.xilinx.com

2100 Logic Drive
San Jose, California 95124
United States of America
Telephone: (408) 559-7778
Fax: (408) 559-7114

Section Titles

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Please note that the BOLD FACE represents what is printed in this data book. For items marked as CD-ROM, use the CD-ROM to access this information or products, or visit the Xilinx website at: www.xilinx.com and select the "Jump To: Data Book".

Section 9: Quality Assurance and Reliability

Section 10: Technical Support and Services

Section 11: Application Notes

Section 12: Sales Offices, Sales Representatives, and Distributors

XC4000 Products

XC3000 and XC5200 Products

1 Introduction

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An Introduction to Xilinx Products

February 15, 2000

About Xilinx

Xilinx® is the leading provider of complete programmable logic solutions. The company's products help minimize risks for manufacturers of electronic equipment by shortening the time required to develop products and take them to market.

Customers can design and verify their proprietary circuits in Xilinx programmable devices much faster than they could using traditional methods, such as mask-programmed gate arrays. Moreover, because Xilinx devices are standard parts needing only to be programmed, customers are not required to wait for prototypes or pay large non-recurring engineering costs. Customers incorporate Xilinx programmable logic into products for a wide range of markets, including data processing, telecommunications, networking, industrial control, instrumentation, consumer electronics, automotive, military and aerospace.

Founded in 1984, Xilinx pioneered the FPGA, and today fulfills more than half the worldwide demand for field-programmable devices. Xilinx, a publicly traded company (NASDAQ: XLNX) headquartered in San Jose, California, employs approximately 1,800 people worldwide. Market researcher Dataquest currently ranks Xilinx as the seventh-largest ASIC supplier in the world.

Operations

As a "fabless" supplier, Xilinx partners with leading semiconductor manufacturers—UMC Group in Taiwan and Seiko Epson in Japan—through close business relationships or equity positions in their factories. This strategy allows Xilinx to focus on designing new product architectures, software tools and cores while having access to the most advanced semiconductor process technologies. Today Xilinx is producing programmable logic devices using state-of-the-art 0.18- and 0.25-micron process technology, and is working on advanced copper interconnect.

Xilinx has manufacturing operations in San Jose and near Dublin, Ireland, where product design, software development, final testing and quality analysis take place. Xilinx also has facilities in Boulder, Colorado, where much of the company's software development takes place, and in Albuquerque, New Mexico, where development of the CoolRunner CPLDs takes place.

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Data Sheet Categories

In order to provide the most up-to-date information, some component products included in this book may not have been fully characterized at the time of publication. In these cases, the AC and DC characteristics included in the data sheets will be marked as *Advance* or *Preliminary* information. (Not withstanding the definitions of such terms, all specifications are subject to change without notice.) These designations have the following meaning:

- **Advance** — Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Use as estimates, but not for final production.
- **Preliminary** — Based on preliminary characterization. Changes are possible, but not expected.
- **Final (unmarked)** — Specifications not identified as either Advance or Preliminary are to be considered final.

About This Edition

This data book contains only a snapshot of mainstream Xilinx programmable logic products and brief descriptions and titles of applications note. The data sheets are abbreviated to provide you with basic information on each product line. You can see complete data sheets, pinout tables and application notes either on the current DataSource CD-ROM or by logging on to the data book section of the Xilinx web site. This edition of the data book contains abbreviated descriptions for the following Xilinx product lines:

Virtex™ series FPGAs expand the traditional capabilities of FPGAs to include a powerful set of features that address board level problems for high-performance system designs. The second generation of these devices, the Virtex-E series, is also the industry's first family of FPGAs to offer three million system gates. The Virtex series has numerous built-in features to solve designers' challenges throughout the system: broad capability for chip-to-chip communications through programmable support for the latest I/O standards, digital delay lock loops for clock signal synchronization on the FPGA and on the board, and a memory hierarchy to manage fast access to RAM on and off chip.

Spartan™ series FPGAs are targeted as gate array replacements for low-cost, high-volume designs under 150,000 system gates which require on-chip RAM and can benefit from pre-defined software cores. Spartan devices are optimized for low-cost and are available in 2.5V, 3.3V, and 5V versions. The latest Spartan-II family offers Virtex-like features such as digital delay locked loops, programmable I/O and on-chip block memory.

CoolRunner™ CPLDs are the first to combine very low power with high speed, high density, and high I/O counts in a single device. Xilinx CoolRunner CPLDs feature Fast Zero Power™ technology, allowing them to draw virtually no power in standby mode. CoolRunner CPLDs are ideal for battery operated portable electronic equipment such as laptop PCs, telephone handsets, personal digital assistants and electronic games. These CPLDs also use far less dynamic power during actual operation compared to conventional CPLDs, an important feature for high performance, heat sensitive equipment such as telecom switches, video conferencing systems, simulators, high end testers and emulators. The entire series is available in 3.3V and 5V versions with density ranges beginning at 32 macrocells.

XC9500™ CPLDs from Xilinx range in density from 36 to 288 macrocells and are available in 3.3V and 5V version. XC9500 devices support in-system programming, allowing manufacturers to perform unlimited design iterations during the prototyping phase, extensive system in-board debugging, program and test during manufacturing, and field upgrades. Based on advanced flash memory technology, the XC9500 family provides fast, guaranteed timing, superior pin locking, a full JTAG compliant interface, and 10,000 programming cycles.

QPRO™ Xilinx is the leading supplier of High-Reliability programmable logic devices to the aerospace and defense markets. These devices are used in a wide range of applications such as electronic warfare, missile guidance and targeting, RADAR, SONAR, communications, signal processing, avionics and satellites. The Xilinx QPRO family of ceramic and plastic QML products (Qualified Manufacturers Listing), certified to MIL-PRF-38585, provide system designers with advanced programmable logic solutions for next generation designs. The QPRO family also includes select products that are radiation hardened for use in satellite and other space applications.

The Xilinx QPRO family addresses the issues that are critical to the aerospace and defense market:

QML/Best commercial practices. Commercial manufacturing strengths result in more efficient process flows

Performance-based solutions, including cost-effective plastic packages.

Reliability of supply. Controlled mask sets and processes insure the same quality devices, every time, without variation, which remain in production for an extended time.

Off-the-shelf ASIC solutions. Standard devices readily available, no need for custom logic and gate arrays.

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Products published in this edition of the Xilinx Data Book are listed by page number in the table contents. Product information that is only on the DataSource CD-ROM, such as complete data sheets, application notes and pinout information, is listed as "CD-ROM" in the table of contents.

Xilinx Online

The Xilinx Online program is designed to enable, identify, and promote network upgradable systems. These are systems that can be upgraded, modified, or fixed after they have been deployed in the field. While many customers have been building upgradable devices based on Xilinx technology for years, the explosion of the networked connected devices has dramatically increased the demand for these user configurable and adaptable applications.

Xilinx provides IRL™ technology to make it easier to develop these systems based upon the most advanced programmable logic available. For more information on this program please visit:

www.xilinx.com/xilinxonline

Technical Support

Xilinx provides 24-hour access to a set of sophisticated tools for resolving technical issues via the Web. The Xilinx search utility scans thousands of Answers records to return solutions for the given issue. Several problem-solver tools are also available for assistance in specific areas, like Configuration or Install. A complete suite of one-hour modules is also available at the desktop via live or recorded e-Learning. Lastly, users with a valid service contract can access Xilinx engineers over the Web by opening a case against a specific issue. For technical support on the Web, log on to:

support.xilinx.com

Xilinx is committed to helping users succeed with programmable logic designs and provides a complete and uniquely accessible array of services and training for customers with service contracts. Xilinx experts provide responsive resolutions to problems and creative, timely solutions to design challenges. They also offer design evaluation of new projects and close consultation through the design process. Full training in design completion and methodology review is also available, along with special application consultation.

Internet-enabled Software Solutions

At Xilinx, software tools are a key part of the company's programmable logic solutions. Since its inception, Xilinx has shipped more than 60,000 development systems to customers worldwide. Today Xilinx offers two lines of design and implementation software that are Internet-enabled to allow designers instant and direct access from the tools to the technical support area of the Xilinx web site.

Through its Alliance Series™ software, Xilinx has chosen open systems approach that allows its customers to pick the highest quality and widest variety of design and programming tools available on the market today. To accomplish this, Xilinx has established engineering and marketing relationships with the leading third-party suppliers of electronic design automation (EDA) software. Those include Aldec, Cadence, Data I/O, Exemplar, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest and Viewlogic. This open systems strategy extends to front-end design creation, synthesis and verification. The result has been the creation of complementary technology and tightly integrated third-party links with the Xilinx Alliance Series backend place and route software for FPGAs and CPLDs.

Foundation Series™ is a family of a fully integrated, ready-to-use Windows NT and Windows 95 PC tools that support a broad range of FPGA and CPLD design requirements. Available at low price points and targeted at entry-level as well as high end users, the Foundation Series products leverage industry standard hardware description languages (HDLs), including Verilog/VHDL. The Windows-based Foundation Series software provides access to synthesis, schematic entry, gate level simulation and implementation tools. Since Foundation Series tools are integrated into a common design management environment, users have access to all technology from design entry and implementation to verification in a single software package.

WebFitter™ is a unique Internet-based software productivity tool that permits customers anywhere in the world to do on-line fitting of CPLD designs from their PC or workstation. Webfitter kicked off the Xilinx "Silicon Xpresso Initiative" that calls for stepped use of the Internet to help increase designer productivity.

Designers access WebFitter from the Xilinx Web site and work from a graphical user interface integrated with the Netscape browser. WebFitter produces complete on-line reports for design evaluation, and it eliminates the need for designers to load software or manage updates and licenses because the latest Xilinx tools always reside on the Xilinx Web site. WebFitter accepts design files for Xilinx XC9500 and CoolRunner series complex programmable logic devices (CPLDs) and supports VHDL, Verilog, ABEL, XNF or EDIF input formats. After completing a front-end

design, users simply enter their e-mail address, attach their design file and send it to the Xilinx server for compilation. Shortly after, a return e-mail provides a complete fitter report and bitstream to implement the design in the PLD. To get to the WebFitter tool, log on to:

www.xilinx.com/sxpresso/webfitter.htm

The Xilinx WebPACK contains FREE downloadable software solutions for Xilinx XC9500 and CoolRunner Series CPLDs. Each solution provides a simple and intuitive design environment for any Xilinx CPLD family. The WebPACK is a collection of three design suites: design entry, device fitting and programming. These tools can be downloaded and used individually or, when installed together become an integrated design environment for Xilinx CPLDs.

www.xilinx.com/sxpresso/webpack.htm

IP Center Solutions

Today, a large number of predefined cores are available to implement system-level functions directly in Xilinx programmable logic devices. These cores, available from Xilinx and third-party partners, allow designers to cut design time and significantly reduce risk while having access to the best performing and lowest cost components available. Full information about Xilinx cores is available on-line from the IP Center area of the Xilinx Web site. To get to the IP Center, log on to:

www.xilinx.com/ipcenter

LogiCORE™ products are sold and supported directly by Xilinx and include PCI interfaces, digital signal processing (DSP) functions and a number of other modules such as adders, multipliers and look-up tables.

AllianceCORE™ modules are sold and supported by a network of third-party developers and are optimized for Xilinx devices. Current AllianceCORE products range from processors and standard peripheral controllers to ATM functions.

The CORE Generator™ tool from Xilinx delivers highly optimized cores that are compatible with standard design methodologies for Xilinx FPGAs. This easy-to-use tool generates flexible, high performance cores with a high degree of predictability and allows customers to download future core offerings from the Xilinx web site. Both Xilinx and independent IP developers can design cores for the CORE Generator tool, which also serves as a cataloging and delivery system for related collateral for all designers using Xilinx.

Design Consultants

The Xilinx XPERTS Program qualifies, develops and supports design consultants, ensuring that they have superior design skills and the ability to work successfully with customers. XPERTS is a worldwide program that allows easy access to certified experts in Xilinx device architectures, software tools and cores. XPERTS partners also offer consulting in the areas of HDL synthesis and verification, customization and integration, system-level designs and team-based design techniques. A listing of partners in the Xilinx XPERTS program is located on the Web at:

www.xilinx.com/ipcenter

Feedback

We welcome any comments or suggestions you have about the Xilinx Data Book – whether it's the printed, CD-ROM, or web version. You can send your feedback by e-mail to:

Databook@xilinx.com

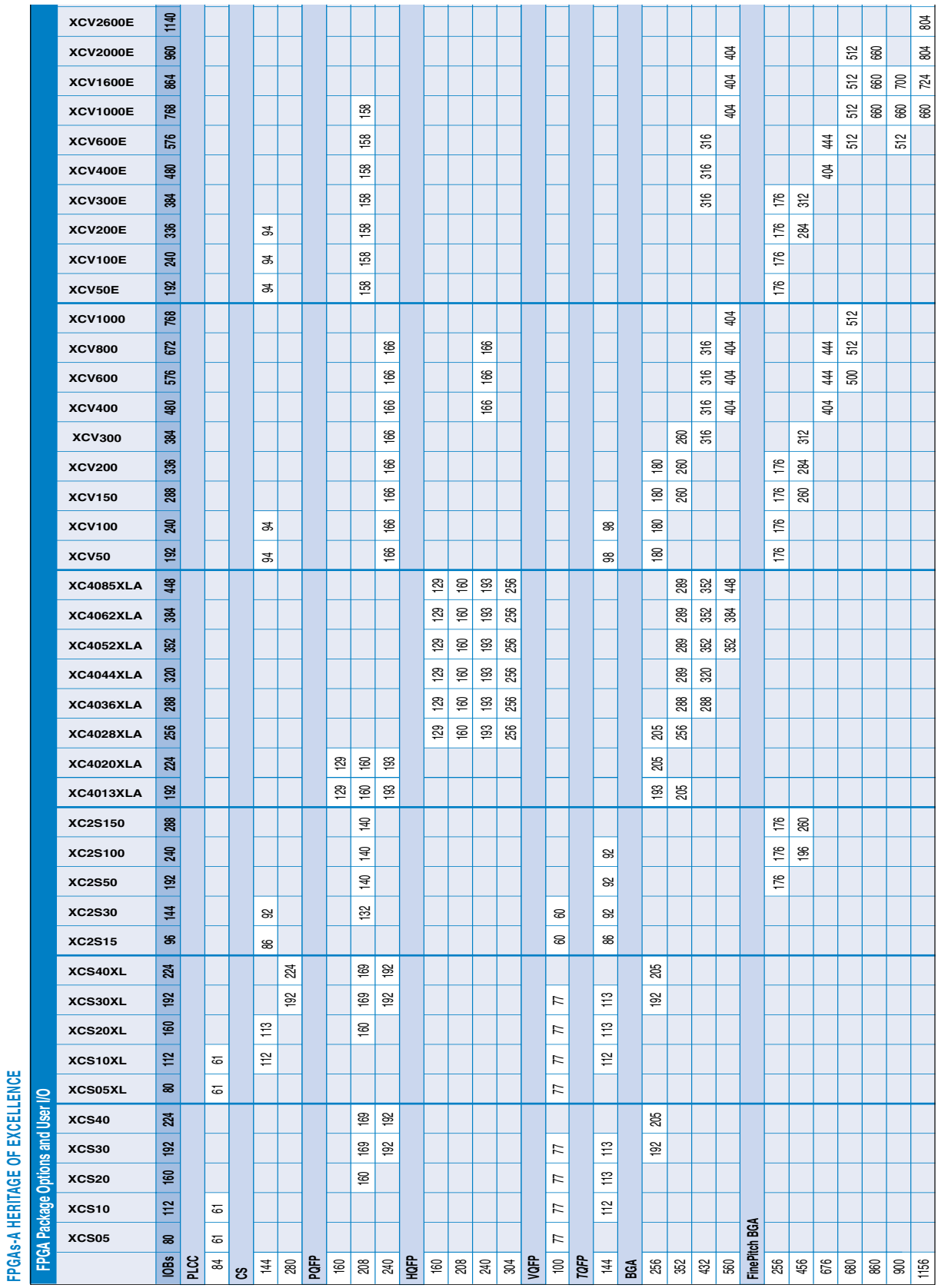

Figure 1: FPGA Package Options and User I/O Selection

FPGA Product Selection Matrix

		DENSITY							FEATURES						
Device	Key Features	Logic Cells	Maximum Logic Gates	Typical System Gate Range	Max. RAM Bits	CLB Matrix	CLBs	Flip-Flops	Max. I/O	Output Drive (mA)	PCI Compliant	1.8 Volt	2.5 Volt	3 Volt	5 Volt
XCS05	Spartan Series: High Volume ASIC Replacement/ High Performance/ SelectRAM Memory	238	3K	2K-5K	3K	10x10	100	360	77	12	Y	–	–	–	X
XCS10		466	5K	3K-10K	6K	14x14	196	616	112	12	Y	–	–	–	X
XCS20		950	10K	7K-20K	13K	20x20	400	1120	160	12	Y	–	–	–	X
XCS30		1368	13K	10K-30K	18K	24x24	576	1536	192	12	Y	–	–	–	X
XCS40		1862	20K	13K-40K	25K	28x28	784	2016	205	12	Y	–	–	–	X
XCS05XL		238	3K	2K-5K	3K	10x10	100	360	77	12/24	Y	–	–	X	*
XCS10XL		466	5K	3K-10K	6K	14x14	196	616	112	12/24	Y	–	–	X	*
XCS20XL		950	10K	7K-20K	13K	20x20	400	1120	160	12/24	Y	–	–	X	*
XCS30XL		1368	13K	10K-30K	18K	24x24	576	1536	192	12/24	Y	–	–	X	*
XCS40XL		1862	20K	13K-40K	25K	28x28	784	2016	224	12/24	Y	–	–	X	*
XC2S15		432	8K	6K-15K	22K	8x12	96	384	86	2/24	Y	–	X	I/O	*
XC2S30		972	17K	13K-30K	36K	12x18	216	863	132	2/24	Y	–	X	I/O	*
XC2S50		1728	30K	23K-50K	56K	16x24	384	1536	176	2/24	Y	–	X	I/O	*
XC2S100		2700	53K	37K-100K	78K	20x30	600	2400	196	2/24	Y	–	X	I/O	*
XC2S150		3888	77K	52K-150K	102K	24x36	864	3456	260	2/24	Y	–	X	I/O	*
XC4013XLA	XC4000 Series: Density Leadership/ High Performance/ SelectRAM Memory	1368	13K	10K-30K	18K	24x24	576	1536	192	12/24	Y	–	–	X	*
XC4020XLA		1862	20K	13K-40K	25K	28x28	784	2016	205	12/24	Y	–	–	X	*
XC4028XLA		2432	28K	18K-50K	33K	32x32	1024	2560	256	12/24	Y	–	–	X	*
XC4036XLA		3078	36K	22K-65K	42K	36x36	1296	3168	288	12/24	Y	–	–	X	*
XC4044XLA		3800	44K	27K-80K	51K	40x40	1600	3840	320	12/24	Y	–	–	X	*
XC4052XLA		4598	52K	33K-100K	62K	44x44	1936	4576	352	12/24	Y	–	–	X	*
XC4062XLA		5472	62K	40K-130K	74K	48x48	2304	5376	384	12/24	Y	–	–	X	*
XC4085XLA		7448	85K	55K-180K	100K	56x56	3136	7168	448	12/24	Y	–	–	X	*
XCV50	Virtex Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O 4 DLLs	1728	21K	34K-58K	56K	16x24	384	1536	180	2/24	Y	–	X	I/O	*
XCV100		2700	32K	72K-109K	78K	20x30	600	2400	180	2/24	Y	–	X	I/O	*
XCV150		3888	47K	93K-165K	102K	24x36	864	3456	260	2/24	Y	–	X	I/O	*
XCV200		5292	64K	146K-237K	130K	28x42	1176	4704	284	2/24	Y	–	X	I/O	*
XCV300		6912	83K	176K-323K	160K	32x48	1536	6144	316	2/24	Y	–	X	I/O	*
XCV400		10800	130K	282K-468K	230K	40x60	2400	9600	404	2/24	Y	–	X	I/O	*
XCV600		15552	187K	365K-661K	312K	48x72	3456	13824	512	2/24	Y	–	X	I/O	*
XCV800		21168	254K	511K-888K	406K	56x84	4704	18816	512	2/24	Y	–	X	I/O	*
XCV1000		27648	332K	622K-1,124K	512K	64x96	6144	24576	512	2/24	Y	–	X	I/O	*
XCV50E	Virtex-E Family: Density/ Performance Leadership BlockRAM Distributed RAM SelectI/O+ 8 DLLs LVDS, BLVDS, LVPECL	1728	21K	47K-72K	88K	16x24	384	2112	176	2/24	Y	X	I/O	I/O	*
XCV100E		2700	32K	105K-128K	117K	20x30	600	3120	176	2/24	Y	X	I/O	I/O	*
XCV200E		5292	64K	215K-306K	185K	28x42	1176	5712	284	2/24	Y	X	I/O	I/O	*
XCV300E		6912	83K	254K-412K	224K	32x48	1536	7296	316	2/24	Y	X	I/O	I/O	*
XCV400E		10800	130K	413K-570K	310K	40x60	2400	11040	404	2/24	Y	X	I/O	I/O	*
XCV600E		15552	187K	679K-986K	504K	48x72	3456	15552	512	2/24	Y	X	I/O	I/O	*
XCV1000E		27648	332K	1,146K-1,569K	768K	64x96	6144	26880	660	2/24	Y	X	I/O	I/O	*
XCV1600E		34992	420K	1,628K-2,189K	1062K	72x108	7776	33696	724	2/24	Y	X	I/O	I/O	*
XCV2000E		43200	518K	1,857K-2,542K	1240K	80x120	9600	41280	804	2/24	Y	X	I/O	I/O	*
XCV2600E		57132	686K	2,221K-3,264K	1529K	92x138	12696	54096	804	2/24	Y	X	I/O	I/O	*
XCV3200E		73008	876K	2,608K-4,047K	1846K	104x156	16224	68640	804	2/24	Y	X	I/O	I/O	*

* I/Os are 5 Volt compatible
X = Core and I/O voltage
I/Os = I/O voltage supported

Figure 2: FPGA Product Selection Matrix

High Density PROMs

Device	Density	PD8	SO20	PC20	VQ44	PC44	3 Volt	5 Volt	JTAG ISP
XC1701L	1Mb	X	X	X			X		
XC1701	1Mb	X	X	X				X	
XC1702L	2Mb				X		X		
XC1704L	4Mb				X		X		
XC17512L	512Kb	X	X	X			X		
XC18512	512Kb		X	X			X		X
XC1801	1Mb		X	X			X		X
XC1802	2Mb				X	X	X		X
XC1804	4Mb				X	X	X		X

3.3V Configuration PROMs for Spartan/Spartan-XL/Spartan-II

Device	Configuration Bits	PROM Solution	PD8	VO8	SO20	3 Volt	5 Volt
XCS05XL	54,544	XC17S05XL	X	X		X	
XCS10XL	95,752	XC17S10XL	X	X		X	
XC2S15	197,696	XC17S15XL	X	X		X	
XCS20XL	179,160	XC17S20XL	X	X		X	
XCS30XL	249,168	XC17S30XL	X	X		X	
XC2S30	336,768	XC17S30XL	X	X		X	
XCS40XL	330,696	XC17S40XL	X	X	X	X	
XC2S50	559,232	XC17S50XL	X		X	X	
XC2S100	781,248	XC17S100XL	X		X	X	
XC2S150	1,041,128	XC17S150XL	X		X	X	
XCS05	54,544	XC17S05	X	X			X
XCS10	95,752	XC17S10	X	X			X
XCS20	179,160	XC17S20	X	X			X
XCS30	249,168	XC17S30	X	X			X
XCS40	330,696	XC17S40	X		X		X

Configuration PROMs for Virtex

Device	Configuration Bits	XC17xx/18xx Solution	PD8	PC20	SO20	PC44	VQ44
XCV50	559,232	01	X*	X	X		
XCV100	781,248	01	X*	X	X		
XCV150	1,041,128	01	X*	X	X		
XCV200	1,335,872	02				X	X
XCV300	1,751,840	02				X	X
XCV400	2,546,080	04				X	X
XCV600	3,608,000	04				X	X
XCV800	4,715,648	04 + 512 or 8**				X	X
XCV1000	6,127,776	04 + 02 or 8**				X	X

* Available on XC17xx only
** In development

Configuration PROMs for Virtex-E

Device	Configuration Bits	XC17xx/18xx Solution	PD8	PC20	SO20	PC44	VQ44
XCV50E	630,048	01	X*	X	X		
XCV100E	863,840	01	X*	X	X		
XCV200E	1,442,106	01	X*	X	X		
XCV300E	1,875,648	02				X	X
XCV400E	2,693,440	02				X	X
XCV600E	3,961,632	04				X	X
XCV1000E	6,587,520	04 + 02 or 8***				X	X
XCV1600E	8,308,992	04 + 04 or 8***				X	X
XCV2000E	10,159,648	08 + 04 or 16***				X	X
XCV2600E	12,923,000**	16***				X	X
XCV3200E	16,284,000**	16***				X	X

* Available on XC17xx only
** Estimated
*** In development

Low Density PROMs

Device	Density	PD8	SO8	VO8	SO20	PC20	3 Volt	5 Volt	JTAG ISP
XC1736E	36Kb	X	X	X		X		X	
XC1765E	64Kb	X	X	X		X		X	
XC1765EL(X)	64Kb	X	X	X		X	X		
XC17128E	128Kb	X		X		X		X	
XC17128EL(X)	128Kb	X		X		X	X		
XC17256E	256Kb	X		X		X		X	
XC17256EL(X)	256Kb	X		X		X	X		
XC18128	128Kb				X	X	X		X
XC18256	256Kb				X	X	X		X

Note: XC1700EL parts are marked with an "X" instead of "EL"

Figure 3: PROM Package Options and Product Selection

CPLD Package Options and User I/O																										
		XC9536	XC9572	XC95108	XC95144	XC95216	XC95288	XC9536XL	XC9572XL	XC95144XL	XC95288XL	XCR22LV10	XCR22V10	XCR3032A	XCR3064A	XCR3128A	XCR3320C	XCR3960C	XCR5032C	XCR5064C	XCR5128C	XCR3032XL*	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL*
	I/O	34	72	108	133	166	192	36	72	117	192	10	10	32	64	96	192	384	32	64	96	32	64	104	160	216
PLCC																										
	28											10	10													
	44	34	34					34	34					32	32				32	32						
	84		69	69																						
VQFP																										
	44	34						34	34					32	32				32	32		32	32			
	64							36	52																	
	100														64	80				64	80		64	80		
CSP																										
	48	34						36	38													32				
	56														44								44			
	144									117														104		
	280										192														160	216
TQFP																										
	100		72	81	81				72	81																
	128															96					96					
	144									117	117													104	104	
	160																112									
PQFP																										
	100		72	81	81																					
	160			108	133	133																				
	208										168														160	
HQFP																										
	208					166	168																			
BGA																										
	256										192						192									
	352					166	192																			
	492																	384								
SOL																										
	24											10	10													
TSSOP																										
	24											10	10													
FBGA																										
	256										192															

* Contact sales offices for up-to-date product and package availability

Figure 4: CPLD Package Options and User I/O

				Density		Features				
Core Voltage	CPLD Family	Devices	Key Features	Macrocells	Max. I/O	Pin-to-Pin Delay (ns)	System Frequency	Individual OE Ctrl	JTAG	Ultra Low-Power
3.3 Volt ISP	XC9500XL	XC9536XL	Best Pin-Locking JTAG w/Clamp High Performance High Endurance	36	36	5	200	✓	✓	
		XC9572XL		72	72	5	178.6	✓	✓	
		XC95144XL		144	117	5	178.6	✓	✓	
		XC95288XL		288	192	7	151	✓	✓	
	XPLA3	XCR3032XL	Ultra Low Power JTAG Increased Logic Flexibility	32	32	5	200		✓	✓
		XCR3064XL		64	64	6	166		✓	✓
		XCR3128XL		128	104	6	166		✓	✓
		XCR3256XL		256	160	7.5	133		✓	✓
		XCR3384XL		384	216	7.5	133		✓	✓
	XPLA-Enhanced	XCR3032A (PZ3032A)*	Ultra Low Power JTAG	32	32	6	111		✓	✓
		XCR3064A (PZ3064A)*		64	64	7.5	95		✓	✓
		XCR3128A (PZ3128A)*		128	96	7.5	95		✓	✓
	XPLA2	XCR3320 (PZ3320C)*	Ultra Low Power High Density	320	192	7.5	100		✓	✓
		XCR3960 (PZ3960C)*		960	384	7.5	100		✓	✓
5 Volt ISP	XC9500	XC9536	Best Pin-Locking JTAG High Endurance	36	34	5	100	✓	✓	
		XC9572		72	72	7.5	83.3	✓	✓	
		XC95108		108	108	7.5	83.3	✓	✓	
		XC95144		144	133	7.5	83.3	✓	✓	
		XC95216		216	166	10	66.7	✓	✓	
		XC95288		288	192	10	66.7	✓	✓	
	XPLA-Enhanced	XCR5032C (PZ5032C)*	Ultra Low Power JTAG	32	32	6	111		✓	✓
		XCR5064C (PZ5064C)*		64	64	7.5	105		✓	✓
		XCR5128C (PZ5128C)*		128	96	7.5	100		✓	✓

* Philips part number

Figure 5: CPLD Product Selection Matrix

Development System Products and IP Solution Products Table of Contents

Development Systems: Products Overview

IP Solutions Overview

Development Systems: Products Overview

February 15, 2000 (v3.0) Product Overview

Introduction

Leading-edge silicon products, state-of-the art software solutions and world-class technical support make up the total solution delivered by Xilinx. The software component of this solution is critical to the success of every design project. Xilinx Software Solutions provide powerful tools which make designing with programmable logic simple. Push button design flows, integrated on-line help, multimedia tutorials, plus high performance automatic and auto-interactive tools, help designers achieve optimum results. And the industry's broadest array of programmable logic technology and EDA integration options deliver unparalleled design flexibility.

Product Overview

Xilinx Software Solutions are available in two different product series making it easy for designers to choose the right system for their needs. These two series support the industry's broadest array of programmable logic IC families. This allows users to standardize their design tools for all programmable logic applications and use these tools to realize the benefits of the industry's highest performance and density FPGAs and CPLDs. It also makes it easy to migrate designs to new technologies and re-use existing designs in new applications.

The **Xilinx Foundation Series** provides designers with a complete, ready-to-use solution for programmable logic design.

The **Xilinx Alliance Series** provides designers powerful integration of Xilinx design tools with their existing EDA environment.

Flexible Configurations

Xilinx Software Solutions are available in three device configurations giving designers a cost-effective way to match their tools to the design methodologies they require. These configurations are available for both the Foundation and Alliance Series.

Base configurations provide push button design flows and support a broad array of FPGA and CPLD devices targeted for low density and high volume applications.

Standard configurations combine push button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation. Standard configurations include support for all Xilinx programmable logic devices up to and including one million gates.

Elite configurations created to deliver the powerful design tools necessary for designers when creating designs for our greater than one million gate devices.

Foundation Series

The Xilinx Foundation Series provides everything required to design a programmable logic device in an easy-to-use environment. This fully integrated tool set allows users to access design entry, synthesis, implementation and simulation tools in a ready-to-use package. Every step in the design process is accomplished using graphical tool bars, icons and pop-up menus supported by interactive tutorials and comprehensive on-line help.

The Xilinx Foundation Series features support for standards based HDL design. All configurations support the popular ABEL language, with integrated compilers optimized for each target architecture. HDL configurations include integrated VHDL/Verilog synthesis from Synopsys with tutorials and graphical HDL design entry tools to turn new users into experts quickly and easily.

Configurations

Configurations of the Foundation Series contain integrated VHDL/Verilog synthesis and graphical interactive HDL entry tools with the following features:

On-line tutorial teaches the art of VHDL design.

Xilinx HDL Editor provides color coding, syntax checking and single click error navigation making it easy to create and debug VHDL, Verilog and ABEL designs.

Graphical State Machine editor makes the design of simple or complex state machines simple and intuitive.

HDL Language Assistant provides libraries of common functions with optimized VHDL, Verilog and ABEL code.

FPGA and CPLD specific synthesis and optimization from Synopsys tools produce high-utilization, high-performance results.

Foundation iSE v3.1I

http://www.xilinx.com/products/found.htm

The Foundation iSE software has been designed to enable both new and experienced Programmable logic designers to achieve results, through intuitive design flows. You are assured of success on each and every design because Foundation Series gives you the advanced tools and technology you need.

The Foundation iSE software represents Xilinx next evolution of our software. Xilinx has created a powerful HDL design environment by integrating and further developing acquired technology with our own FPGA design tools and powerful implementation tools. You will benefit from the same powerful tools and features of our Foundation and Alliance tools while working in a new environment designed to help you work faster and more efficiently.

The iSE software is packaged with two powerful synthesis tools: the FPGA Express from Synopsys and our own XST (Xilinx Synthesis Technology). We understand that synthesis tools work differently on different designs, with multiple synthesis tools you will have the option of using the tool that fits your design needs. The Foundation iSE Software comes in three configurations:

- Base X
- Express
- Elite

Alliance Series

The Alliance Series provides powerful and integrated design tools for users who require a quality solution for their chosen EDA design solution. With the Alliance Series, users can choose from a wide range of design techniques including schematic capture, module-based design and HDL design solutions. With standard based design interfaces including EDIF, VITAL, VHDL, Verilog and SDF, this series provides maximum flexibility, portability, mixed vendor support, and design reuse.

Quality integration with leading EDA vendors such as ALDEC, Exemplar, Cadence, Mentor Graphics, Model Technology, OrCAD, Synopsys, Synplicity, Veribest and VIEWlogic provide tightly-coupled environments that make it easy to move through the design process and through a mixed EDA vendor flow. The EDA vendors are supported through the Xilinx Alliance Program, insuring high quality tools and accuracy of results. Information on Xilinx Alliance Program vendors can be found on the Xilinx WEB page **www.xilinx.com.**

The Alliance design solutions continue Xilinx' trend of cutting place and route runtime in half, while maintaining or improving design performance. The accumulation of runtime improvements now enable the compilation of the 100,000 system gate Virtex devices in less time. Fast compile times translate to more turns per day and greater productivity.

Features include:

Timing Driven Place and Route. Allows you to specify your timing requirements for critical paths. This feature often gives 30-40% performance improvements when speed is critical; you no longer need to manually fine-tune your design.

Static Timing Analysis. Shortens your design process by providing an evaluation of your timing at various points in the implementation process, allowing you to make changes immediately.

Flow Engine. Automates and simplifies the implementation process. Using a simple graphical interface, you can monitor and control all aspects of your design implementation.

Simulation. Provides design verification before and after implementation, thus reducing the number of design iterations required to meet design specifications.

Incremental Design Capability. Reduces your overall design cycle by allowing you to re-use previous iterations of your design. This is very helpful for evaluating design alterations.

Hierarchical Timing Analysis. The Interactive Timing Analyzer has received a variety of dramatic improvements to its User interface, including hierarchical reporting of timing analysis results. This feature simplifies the process of navigation through the rich set of timing information Xilinx provides on your design. The Alliance Software comes in two configurations:

- Standard
- Elite

ModelSim Xilinx Edition

(http://www.xilinx.com/products/software/mxe.htm)

The ModelSim Xilinx Edition (XE) simulator is a complete HDL simulation environment, optimized for use in verifying Xilinx programmable logic designs. ModelSim XE enables designers to verify source code (VHDL and Verilog), functional, and timing models of their design using a common "self-checking" testbench. ModelSim XE provides a powerful first step into the world of HDL simulation with capacity and performance designed for the verification of the Xilinx XC9500 CPLD and Spartan FPGA series of programmable logic devices as well as lower-density XC4000 and Virtex series FPGAs.

ModelSim XE is most valuable for customers who understand the benefits of VHDL or Verilog simulation, and are looking for a cost-effective solution for low-density programmable logic design. It is available in both VHDL and Verilog versions. ModelSim XE may only be used with v2.1i Xilinx development systems and later. Xilinx sells the MOD-

ELSIM XE products as options to any of its development systems.

CPLD Web Powered Software Solutions:

The Xilinx CPLD Web Powered Software Solutions offer designers the flexibility to do CPLD design evaluation and fitting on-line or on their desktop. The WebFITTER is an on-line device fitting and evaluation tool which accepts VHDL, Verilog, ABEL or netlist files. The WebPACK downloadable desktop solutions offer FREE CPLD software modules from ABEL and HDL synthesis to device fitting and JTAG programming.

WebFITTER:

(http://www.xilinx.com/sxpresso/webfitter.htm)

The Xilinx WebFITTER is a FREE, web-based CPLD design evaluation and fitting software tool that allows system designers to target their designs using the industry's best CPLDs, the XC9500 Series and the CoolRunner Series, on the latest version of Xilinx software and get their results and pricing in minutes!

WebPACK:

(http://www.xilinx.com/sxpresso/webpack.htm)

The Xilinx WebPACK contains FREE downloadable software solutions for Xilinx XC9500 and CoolRunner Series CPLDs. Each solution provides a simple andintuitive design environment for any Xilinx CPLD family. The WebPACK is a collection of three design suites: design entry, device fitting and programming. These tools can be downloaded and used individually or, when installed together become an integrated design environment for Xilinx CPLDs.

Background

Designers everywhere are using Xilinx FPGAs to implement system-level functions in demanding applications including communications, high-speed networking, image processing, and computing. Xilinx offers the industry's largest selection of intellectual property (IP) cores, which serves as the foundation for accomplishing complex system-on-a-chip designs. Xilinx cores are pre-defined, tested, and verified to ensure correct functionality. In addition, Xilinx cores utilize Smart-IP technology to predetermine the implementation providing optimal and predictable performance and utilization.

The broadest selection of industry-standard solutions offered by Xilinx comprise two IP sources: LogiCORE™ and AllianceCORE™. The LogiCORE program being the most successful in the industry, offers cores exclusively for Xilinx FPGAs. These cores are sold and supported by Xilinx. The AllianceCORE program provides a broad selection of third-party cores customized for use with Xilinx FPGAs and CPLDs.

Smart-IP Core Design Methodology

Smart-IP technology is a combination of several features designed to deliver highest performance, predictability, and flexibility when implementing IP with Xilinx FPGAs.

Smart-IP technology ensures constant core performance regardless of its position in the FPGA device; maintained performance when multiple cores are integrated in the same FPGA device; and no performance degradation when migrating to larger devices.

Xilinx IP Center on the Web

The Xilinx IP Center offers a comprehensive list of LogiCORE and AllianceCORE products, reference designs, and application notes. It also provides access to AllianceCORE partners and to partners from the Xperts consultants program.

All cores, reference designs, and design reuse tools from Xilinx are delivered over the Internet; the latest versions of these products are available for download from the Xilinx IP Center at **www.xilinx.com/ipcenter**.

CORE Generator System™

The Xilinx CORE Generator system generates and delivers parameterizable cores optimized for Xilinx FPGAs. You use the Xilinx CORE Generator system to design high-density Xilinx FPGA devices and achieve high-performance results, while reducing your design time.

CORE Generator Features:

- Simple, intuitive operation – Select a core, enter parameters, and generate
- Compatible with VHDL, Verilog, and Schematic top-level design flows
- Cores are delivered with a logic design plus an optimal floorplan or layout
- Performance is independent of FPGA device size
- Performance stays constant as more cores are added
- Optimal results as measured against the best hand-packed design
- Data sheet and VHDL behavioral model with each core
- Ready access to intellectual property from Xilinx and Xilinx partners
- Predictable and repeatable results: core performance is specified in advance
- PC and Workstation platforms supported

CORE Generator Benefits:

- Faster time-to-market
- Fast core generation time with proprietary Xilinx software
- Reduced place and route time with preplaced Cores
- Less engineering required with predesigned cores
- Facilitates design reuse
- Build your design out of cores
- Simpler documentation with larger parameterizable building blocks
- Optimal core layout produces lower power dissipation

Xilinx Design Reuse

The need for design resuse has been apparent for many years; no company likes to put many man years of effort into a design that can be used only once. Today, thousands of designers are creating intellectual property (IP) on a huge scale, targeting the widely popular million-gate Virtex™ FPGA family which is ideally suited to support design resuse. For the latest most detailed information on Xilinx Design Reuse function, visit:

www.xilinx.com/ipcenter/designreuse/index.htm.

Xilinx PCI Solutions

PCI (Peripheral Component Interconnect) has become one of the most popular bus standards, not only for personal computers, but also for industrial computers, communication switches, routers, and instrumentation. It solves a wide range of compatibility problems and performance limitations that were encountered with the older ISA and VME standards.

However, PCI is also a significant design challenge; the stringent electrical, functional, and timing specifications are difficult to meet in any technology-and the standard keeps evolving to meet the dynamic needs of our industry. That's why you need a flexible PCI solution that will meet both your current and future requirements, while guaranteeing full PCI compliance with no limitations on performance or functionality.

Our first LogiCORE PCI product was released in January, 1996. Now, our PCI cores have been proven in over 1000 customer designs, clearly demonstrating that Real-PCI from Xilinx is the most flexible and cost-effective solution for your fully-compliant, high-performance PCI system.

Visit the Xilinx IP-Center for more details and datasheets on individual products, **www.xilnx.com/ipcenter.**

Features:

- **Real Compliance - all LogiCORE PCI products are:**
  - Fully verified using our industry-proven testbench that simulates over six million unique PCI cycles
  - Hardware verified
  - PCI cores and FPGAs characterized together for guaranteed maximum, minimum and hold timing
  - Smart-IP technology to maintain timing guarantees for every core implementation
- **Real Flexibility**
  - Supports Xilinx standard off-the-shelf PCI-compliant FPGAs
  - Range of device sizes and packages to choose from for most cost-effective solution
  - Integrates a fully-compliant target/initiator PCI interface, scalable dual-port FIFOs, customizable, DMA channels, and 7,000 to 2 million custom gates
  - Flexible source code Reference Designs available to exemplify back-end designs and accelerate time to market
  - Re-configurable FPGAs allows accommodation of future changes in the PCI standard or feature requirements
- **Real Performance**
  - Supports up to 66 MHz PCI systems
  - Operates at maximum throughput, with zero wait-state bursts
  - Full 32-bit and 64-bit data path
- **Real Availability**
  - All LogiCORE PCI products available from Xilinx IP-Center on the Internet (**www.xilinx.com/pci**) to give users instant access to latest versions
  - Easy and quick configuration via web-based configuration tool.
  - Generates unique netlists, implementation constraint files, simulation models and instantiation code for VHDL and Verilog
  - Design Kits available with 64-bit and 32-bit prototyping boards, driver development tools and Reference Designs
  - PCI training classes (3-4 days) available. See **support.xilinx.com** for details
  - Specially trained XPERTS partners available for design services such as retargeting to untested devices, integration, or core customization.

PCI Design Kits

Ballyinx 64/66 PCI Prototyping Board from Nallatech

The 64-bit Design Kit includes Ballyinx 64/66 PCI prototyping board with a XCV300-6 BG432 device that allows designers to quickly evaluate the performance of the Xilinx 64/66 PCI core in their system. In addition, the board demonstrates how to build a universal 3.3V and 5V PCI card. By incorporating Nallatech's DIME standard for modular expandability, the prototyping board can be used in a wide variety of system solutions including FPGA-based DSP.

HotPCI 32/33 PCI Prototyping Board from Virtual Computer Corporation

The 32-bit PCI Design Kit includes HotPCI 32/33 PCI prototyping board with an XCS40-4 PQ240 device that allows designers to quickly evaluate the performance of the Xilinx 32/33 PCI core in their system. The board includes 8x128K SRAM and is reconfigurable from the PCI bus.

SoftICE Driver Suite from Compuware

The Xilinx PCI Design Kits includes a standard license of Compuware's NuMega SoftICE Driver suite that accelerate the development and debugging of Windows device drivers. The SoftICE Drive Suite includes all versions of SoftICE, including SoftICE for Windows 2000/NT, SoftICE for Windows 95, SoftICE for Windows 3.1, and SoftICE for DOS along with DriveWorks, VtoolsD, and DriverAgent.

PCI Training

To further complete the Xilinx PCI solution, Xilinx offers a three-day PCI course for customers who are planning PCI systems. The course will give an introduction to the PCI standard, and will cover configuration and integration of core, system integration, verification and debug. More information can be found at **support.xilinx.com**.

Table 1: PCI Solutions Ordering Information

Product part number	Description	Accessible Design Files	Prototyping Board	Driver Development Tools	Miscellaneous
DO-DI-PCI32-S	32-bit PCI for Spartan family	PCI32 Spartan-II PCI32 Spartan-XL PCI32 Spartan	No	No	All design files and docs delivered over the Internet
DO-DI-PCI32-DK	32-bit PCI Design Kit	Same as DO-DI-PCI32-S *plus:* PCI32 Virtex-E PCI32 Virtex PCI32 4000XLA	VCC HotPCI board with XCS40 PQ208	Compuware NuMega SoftICE Driver Suite	PCI Systems Architecture Text Book Printed Design Guide
DO-DI-PCI64	64/32-bit 33/66 MHz PCI	Same as DO-DI-PCI32-DK *plus:* PCI64/66 Virtex-E PCI64/66 Virtex PCI64 Spartan-II	No	No	All design files and docs delivered over the Internet
DO-DI-PCI64-DK	64-bit 66 MHz Design Kit	Same as DO-DI-PCI64	Nallatech Ballyinx 64-bit 66 MHz PCI Prototyping Card with XCV300 BG432	Compuware NuMega SoftICE Driver Suite	PCI Systems Architecture Text Book Printed Design Guide
DX-DI-M2DK-DK	Upgrade from DO-DI-PCIM (obsolete) to DO-DI-PCI32-DK(1)				
DX-DI-S2DK-DK	Upgrade from DO-DI-PCIS (obsolete) to DO-DI-PCI32-DK(1)				
DX-DI-PCI32-DK	Upgrade from DO-DI-PCI32-S to DO-DI-PCI32-DK(1)				
DX-DI-PCI64	Upgrade from DO-DI-PCI32-DK to DO-DI-PCI64(1)				
DX-DI-PCI64-DK	Upgrade from DO-DI-PCI64 to DO-DI-PCI64-DK(1)				

Note 1: Requires a valid maintenance contract

Xilinx DSP Solutions

With Xilinx DSP, users can combine ASIC-like performance and integration with the flexibility of a DSP processor implementation. By utilizing parallel computing techniques in a Xilinx FPGA, users can achieve radical performance advantage over fixed processors. The Xilinx FGA implementation will at the same time maintain maximum flexibility and the shortest time-to-market, which is lost using an ASIC implementation. Until now, tools to automate the design process have been lacking and only experienced FPGA designers have completed most designs manually.

With the introduction of Xilinx' CORE Generator System for DSP, complex parameterized DSP building blocks can be implemented automatically with the performance and density of a hand-tuned implementation. LogiCORE DSP modules can be used with VHDL-, Verilog- or schematic-based design methodologies.

Higher-level DSP cores and DSP prototyping boards are available from our AllianceCORE partners.

DSP system level modeling tools are available to mathematically model LogiCORE based FPGA designs and aid in determining optimal core parameters.

The Xilinx DSP Solution consists of:

- Standard Xilinx FPGA components - Virtex-E, Virtex, Spartan-II, Spartan-XL, Spartan and XC4000
- DSP parameterizable LogiCORE and AllianceCORE FPGA products, e.g., FIR Filters, FFTs, Reed-Solomon FEC cores, and Multipliers, supporting high-performance applications such as wireless communication, digital networking, image processing, DVB, and HDTV.
- DSP system level tools integration
- DSP starter kit
- Regional dedicated DSP Field Applications Engineers
- DSP Ph.D. level support
- Acquiring LogiCORE Products

Features

- ASIC-like DSP performance through parallel processing, for example:
  - 128-tap FIR filter, 8-bit data, 12-bit coefficients, 120 MSPS
  - 1024 point complex FFT, 16-bit input, 35 µs transform time
- Re-configurable FPGAs allows accommodation of specification and feature changes late in the design process and in end users' products
- Cost-effective implementation saves cost over Application Specific Standard Products (ASSP)
- Integrates DSP functions with memory, control and glue logic into single-chip solutions

- Xilinx LogiCORE includes Smart-IP technology to maintain timing independently of surrounding logic and device size
- Wide range of device sizes and packages to choose from for most cost-effective solution
- All LogiCORE PCI products available from Xilinx IP-Center on the Internet (**www.xilinx.com/pci**) to give users instant access to latest versions
- Easy and quick configuration via CORE generator or web-based configuration tool
- Generates unique netlists, implementation constraint files, simulation models and instantiation code for VHDL and Verilog
- Specially trained XPERTS partners available for design services such as retargeting to untested devices, integration, or core customization

Table 2: DSP Solutions Ordering Information

Product part number	Description	Accessible Design Files	Prototyping Board	Miscellaneous
DO-DI-RSE	Reed-Solomon Encoder	Parameterizable encoder for: • Virtex-E • Virtex • Spartan-II • Spartan-XL • Spartan • XC4000XLA	No	All design files and docs delivered over the Internet
DO-DI-RSD	Reed-Solomon Decoder	Parameterizable decoder for: • Virtex-E • Virtex • Spartan-II • Spartan-XL • Spartan • XC4000XLA	No	All design files and docs delivered over the Internet

Note 1: Free LogiCORE DSP modules such as FIR filters, multipliers, and FFTs are available for download to all Xilinx SW customers from Xilinx IP-Center. These cores are installed and configured with the Xilinx CORE generator.

AllianceCORE Products

Through the AllianceCORE program, Xilinx is expanding the availability of high quality cores for programmable logic by sharing what has been learned with leading third-party core developers.

The AllianceCORE program is a cooperative effort between Xilinx and independent third-party core developers. It is designed to produce a broad selection of industry-standard solutions dedicated for use in Xilinx programmable logic.

Xilinx takes an active role with its partners in the process of productizing AllianceCORE products. This is unique to the AllianceCORE program. Because the process is so involved, we work closely with our partners to select the right cores first which helps raise the quality and usability of the cores that are offered. A core must meet a minimum set of criteria before it can receive the AllianceCORE label.

Table 3: Xilinx AllianceCORE Products

Standard Bus Products
Generic Bus Arbiter
CAN Bus Interface
XF-TWSI Two-Wire Serial Interface (IIC) Master Only
XF-TWSI-MS Two-Wire Serial Interface (IIC) Master & Slave
IEEE 1394 FireWire Link Layer Core
IEEE 1394 FireWire Evaluation Board
Communications and Networking
Asynchronous Transfer Mode
IMA 8-Channel Inverse Multiplexing for ATM
IMA 32-Channel Inverse Multiplexing for ATM
Distributed Sample Scrambler
Distributed Sample Descrambler
Cell Assembler (CC-201)
Cell Delineation (CC-200)
CRC10 Generator and Verifier (CC-130)
CRC32 Generator and Verifier (CC-131)
UTOPIA Level 2 Slave Transmitter
UTOPIA Level 2 Slave Receiver
UTOPIA Level 2 Master (CC-140f)
UTOPIA Level 2 Slave on-chip FIFO (CC-141f)
UTOPIA Level 2 Slave off-chip FIFO (CC-143s)
Ethernet
10/100 Mbps Fast Ethernet MAC
10/100 Mbps Fast Ethernet MAC Core Evaluation Board
HDLC
Single-Channel XF-HDLC Controller
Single-Channel PPP8 HDLC Controller
Single-Channel HDLC Controller Core
Forward Error Correction
Reed Solomon Decoder
Reed-Solomon Encoder
Reed Solomon Decoder
Reed-Solomon Encoder
Convolutional Encoder
Viterbi Decoder
Telecommunications
Noisy Transmission Channel Model
ADPCM Codec
XF-MOD-DVB Satellite Modulator
X-3DES Triple Data Encryption Standard Cryptoprocessor
X-DES Data Encryption Standard Cryptoprocessor

Table 3: Xilinx AllianceCORE Products (Continued)

XF-DES Data Encryption Standard
MT1FT1 Framer
DSP Functions
Video and Image Processing
X_DCT/IDCT Discrete/Inverse Discrete Cosine Transform
X_JPEG JPEG Codec
YCrCb2RGB Color Space Converter
RGB2YCrCb Color Space Converter
DSP Core Development Tool
GVA-270 Virtex-E DSP Hardware Accelerator Board
GVA-220 DSP Hardware Accelerator Board
GVA-250 Virtex DSP Hardware Accelerator Board
GVA-200 DSP Hardware Accelerator Board
GVA-100 DSP Prototyping Board
Processor Products
C2901 Microprocessor Slice
C2910a Microprogram Controller
Flip805x-PR 8051/2 Core
V8 uRISC 8-bit RISC Microprocessor
Intellicore™ Prototyping System
Processor Peripherals
M8237 DMA Controller
M8254 Programmable Timer
C8255A Peripheral Interface
M8255 Programmable Peripheral Interface
XF-8255 Programmable Peripheral Interface
XF-8256 Multifunction Microprocessor Support Controller
C8259A Programmable Interrupt Controller
M8259 Programmable Interrupt Controller
XF-8279 Programmable Keyboard Display Interface
SDRAM Controller
DRAM Controller
200 MHz SDRAM Controller
UARTs
C_UART Compact UART
XF-8250 Asynchronous Communications Element
C8251 Programmable Communications Interface
C16450 UART
M16450 UART
C16550 UART with FIFOs
M16550A UART with RAM
C6850 Asynchronous Communications Interface Adapter (ACIA)
Generic Core Development Tools
Microprocessor-Based Core Evaluation Card

XPERTS

Xilinx Program for Engineering Resources from Third Parties

Xilinx customers can take advantage of XPERTS, a world-wide program giving customers access to Xilinx-certified experts in Xilinx architecture, PCI designs, new design methodologies, customer or third-party IP customization and integration, and system level design. Partners (Table 4) have experience and expertise in delivering turn-key system designs for communications, networking, video and medical imaging and computer applications. Their experience with various standards and large systems design will complement your internal expertise to deliver the right product, at the right time and lowest cost.

Table 4: XPERTS Partners

XPERTS Partners	Telecom & Datacom	Networking	Imaging & Video
Advanced Digital Designs	X		X
Andraka Consulting			X
Applied Micro Technology Inc.	X		
Baranti			X
BARCO SILEX			X
Bottom Line Technologies Inc.			X
Comit Systems			X
DesignPRO Inc.	X		
Synchronous Design Solutions	X		
Dillon Engineering			X
ECLA Inc.		X	
Electronic Design Associates Inc.			X
Enator Elektroniksystem AB	X		X
EuroMIPS Systems	X		
GERPI	X		
Integrated Intellectual Property Inc. (I2P)		X	X
LP Technology Inc.	X		X
MultiVideo Designs			X
North Pole Engineering		X	X
Northwest Logic Design			X
Perigee			X
PLC 2	X		
Polybus		X	X
Rapid Prototypes Inc.			X
Roman-Jones Inc.			X
SECAD			X
Silicon & Software Systems	X		X
SO-LOGIC			X
SPEAR Technology CC			X
Synchronous Design Solutions	X		
Syntera Digital Solutions	X		
Thomas Design			X

Table 5: Xilinx LogiCORE Products

General-Purpose Cores
Asynchronous FIFOs (BlockRAM & Distributed RAM)
Memory Compilers (BlockRAM & Distributed RAM)
Multipliers (variable, parallel)
Multipliers (constant coefficient, loadable)
Divider
Counter
Accumulator
Adder-Subtractor
Comparator
Shift Register (Flip-Flop based)
Shift Register (RAM based)
Decoder (Binary)
Gate (bus output with control bit)
Gate (Single output)
Gate (bus output)
Multiplexer (Bit)
Multiplexer (Bus)
Multiplexer (BUFE based slice)
Multiplexer (BUFT based slice)
Register (Flip-Flop Based)
Latch (LD based)
Two's Complement

Table 5: Xilinx LogiCORE Products (Continued)

DSP and Communication Cores
FIR Filters, Distributed Arithmetic
FFT, Complex, High-performance, 1024 point
FFT, Complex, High-performance, 256-point
FFT, Complex, High-performance, 64-point
FFT, Complex, High-performance, 16-point
Reed Solomon Encoder, parameterizable
Reed Solomon Decoder, parameterizable
DDS (NCO)
Sine/Cosine Look Up Table
Interface Cores
PCI 64-bit, 33-66 MHz
PCI64 Design Kit (incl. Virtex prototyping board and driver development tools)
PCI 32-bit, 33 MHz
PCI32 Design Kit (incl. Spartan-II prototyping board and driver development tools)
Reference Designs
SDRAM Controller
ZBT RAM Controller
Double Data Rate RAM Controller
PCI64 Bridge Reference Designs
PCI32 Bridge Reference Designs
PCI Power Management Reference Design
PCI32 Asynchronous FIFO Reference Designs
PCI64 Asynchronous FIFO Reference Designs

Virtex Products
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Virtex-E 1.8V
Field Programmable Gate Arrays

For a complete data sheet, go to CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Virtex 2.5V
Field Programmable Gate Arrays

For a complete data sheet, go to CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Virtex-E 1.8V Field Programmable Gate Arrays

DS022 (v1.3) February 28, 2000

Advance Product Specification

Features

- Fast, High-density 1.8V FPGA Family
  - Densities from 58 k to 4 M system gates
  - 130 MHz internal performance (four LUT levels)
  - Designed for low-power operation
  - PCI compliant 3.3V, 32/64-bit, 33/ 66-MHz
- Highly Flexible SelectIO+™ Technology
  - Supports 20 high-performance interface standards
  - Up to 804 singled-ended I/Os or 344 differential I/O pairs for an aggregate bandwidth of > 100 Gb/s
- Differential Signalling Support
  - LVDS (622 Mb/s), BLVDS (Bus LVDS), LVPECL
  - Differential I/O signals can be input, output, or I/O
  - Compatible with standard differential devices
  - LVPECL and LVDS clock inputs for 300+ MHz clocks
- Proprietary High-performance SelectLink™ Technology
  - Double Data Rate (DDR) to Virtex-E link
  - Web-based HDL generation methodology
- Sophisticated SelectRAM+™ Memory Hierarchy
  - 1 Mb of internal configurable distributed RAM
  - Up to 832K of synchronous internal BlockRAM
  - True Dual-Port™ BlockRAM capability
  - Memory bandwidth up to 1.66 Tb/s (equivalent bandwidth of over 100 RAMBUS channels)
  - Designed for high-performance Interfaces to External Memories
  - 200 MHz ZBT* SRAMs
  - 200 Mb/s DDR SDRAMs
  - Supported by free Synthesizable reference design
- High-performance Built-in Clock Management Circuitry
  - Eight fully digital Delay-Locked Loops (DLLs)
  - Digitally-Synthesized 50% duty cycle for Double Data Rate (DDR) Applications
  - Clock Multiply and Divide
  - Zero-delay conversion of high-speed LVPECL/LVDS clocks to any I/O standard
- Flexible Architecture Balances Speed and Density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input function
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensor diode
- Supported by Xilinx Foundation™ and Alliance Series™ Development Systems
  - Further compile time reduction of 50%
  - Internet Team Design (ITD) tool ideal for million-plus gate density designs
  - Wide selection of PC and workstation platforms
- SRAM-based In-system Configuration
  - Unlimited re-programmability
- Advanced Packaging Options
  - 0.8 mm Chip-scale
  - 1.0 mm BGA
  - 1.27 mm BGA
  - HQ/PQ
- 0.18 µm 6-layer Metal Process
- 100% Factory Tested

Table 1: Virtex-E Field-Programmable Gate Array Family Members

Device	System Gates	Logic Gates	CLB Array	Logic Cells	Differential I/O Pairs	User I/O	BlockRAM Bits	Distributed RAM Bits
XCV50E	71,693	20,736	16 x 24	1,728	83	176	65,536	24,576
XCV100E	128,236	32,400	20 x 30	2,700	83	176	81,920	38,400
XCV200E	306,393	63,504	28 x 42	5,292	119	284	114,688	75,264
XCV300E	411,955	82,944	32 x 48	6,912	137	316	131,072	98,304
XCV400E	569,952	129,600	40 x 60	10,800	183	404	163,840	153,600
XCV600E	985,882	186,624	48 x 72	15,552	247	512	294,912	221,184
XCV1000E	1,569,178	331,776	64 x 96	27,648	281	660	393,216	393,216
XCV1600E	2,188,742	419,904	72 x 108	34,992	344	724	589,824	497,664
XCV2000E	2,541,952	518,400	80 x 120	43,200	344	804	655,360	614,400
XCV2600E	3,263,755	685,584	92 x 138	57,132	344	804	753,664	812,544
XCV3200E	4,074,387	876,096	104 x 156	73,008	344	804	851,968	1,038,336

* ZBT is a trademark of Integrated Device Technology, Inc.

Virtex-E Compared to Virtex Devices

The Virtex™-E family offers up to 43,200 logic cells in devices up to 30% faster than the Virtex family.

I/O performance is increased to 622 Mb/s using Source Synchronous data transmission architectures and synchronous system performance up to 240 MHz using singled-ended SelectIO technology. Additional I/O standards are supported, notably LVPECL, LVDS, and BLVDS, which use two pins per signal. Almost all signal pins can be used for these new standards.

Virtex-E devices have up to 640 Kb of faster (250 MHz) Block SelectRAM, but the individual RAMs are the same size and structure as in the Virtex family. They also have eight DLLs instead of the four in Virtex devices. Each individual DLL is slightly improved with easier clock mirroring and 4x frequency multiplication.

V_{CCINT}, the supply voltage for the internal logic and memory, is 1.8V, instead of 2.5V for Virtex devices. Advanced processing and 0.18 µm design rules have resulted in smaller dice, faster speed, and lower power consumption.

I/O pins are 3V tolerant, and can be 5V tolerant with an external 100Ω resistor. PCI 5V is not supported. With the addition of appropriate external resistors, any pin can tolerate any voltage desired.

Banking rules are different. With Virtex devices, all input buffers are powered by V_{CCINT}. With Virtex-E devices, the LVTTL, LVCMOS2, and PCI input buffers are powered by the I/O supply voltage V_{CCO}.

The Virtex-E family is not bitstream-compatible with the Virtex family, but Virtex designs can be compiled into equivalent Virtex-E devices.

The same device in the same package for the Virtex-E and Virtex families are pin-compatible with some minor exceptions. See the data sheet pinout section for details.

General Description

The Virtex-E FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 6-layer metal 0.18 µm CMOS process. These advances make Virtex-E FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex-E family includes the nine members in Table 1.

Building on experience gained from Virtex FPGAs, the Virtex-E family is an evolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex-E family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Virtex-E Architecture

Virtex-E devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex-E family to accommodate even the largest and most complex designs.

Virtex-E FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. Configuration data can be read from an external SPROM (master serial mode), or can be written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation Series™ and Alliance Series™ Development systems deliver complete design support for Virtex-E, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation and downloading of a configuration bit stream.

Higher Performance

Virtex-E devices provide better performance than previous generations of FPGAs. Designs can achieve synchronous system clock rates up to 240 MHz including I/O or 622 Mb/s using Source Synchronous data transmission architectures. Virtex-E I/Os comply fully with 3.3V PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz.

While performance is design-dependent, many designs operate internally at speeds in excess of 133 MHz and can achieve over 311 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: Performance for Common Circuit Functions

Function	Bits	Virtex-E -7
Register-to-Register		
Adder	16 64	4.3 ns 6.3 ns
Pipelined Multiplier	8 x 8 16 x 16	4.4 ns 5.1 ns
Address Decoder	16 64	3.8 ns 5.5 ns
16:1 Multiplexer		4.6 ns
Parity Tree	9 18 36	3.5 ns 4.3 ns 5.9 ns
Chip-to-Chip		
HSTL Class IV		
LVTTL,16mA, fast slew		
LVDS		
LVPECL		

Architectural Description

Virtex-E Array

The Virtex-E user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex-E architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

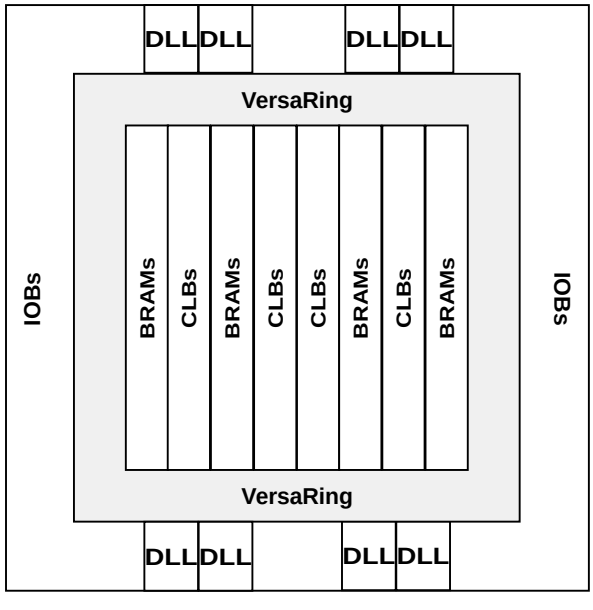


Figure 1: Virtex-E Architecture Overview

Input/Output Block

The Virtex-E IOB, Figure 2, features SelectIO+™ inputs and outputs that support a wide variety of I/O signalling standards, see Table 3.

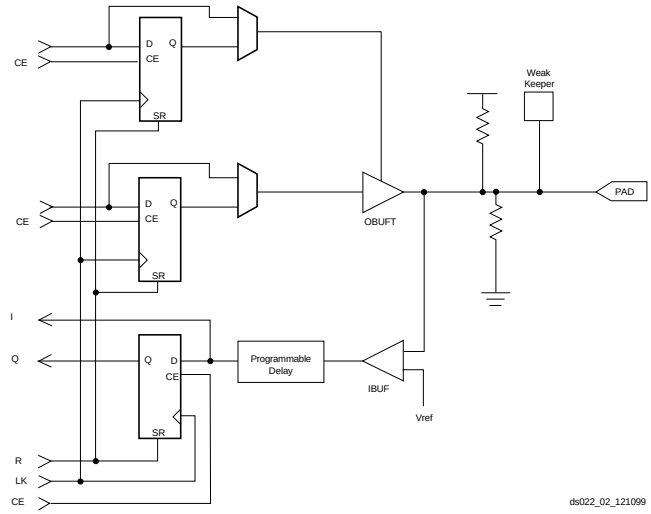


Figure 2: Virtex-E Input/Output Block (IOB)

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level-sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

Table 3: Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. When PCI 3.3 V compliance is required, a conventional clamp diode is connected to the output supply voltage, V_{CCO}.

Optional pull-up, pull-down and weak-keeper circuits are attached to each pad. Prior to configuration all outputs not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but IOs may optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins are in a high-impedance state. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex-E IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

The Virtex-E IOB input path routes the input signal directly to internal logic and/ or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 8.

There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 8.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Since the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages are externally supplied and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

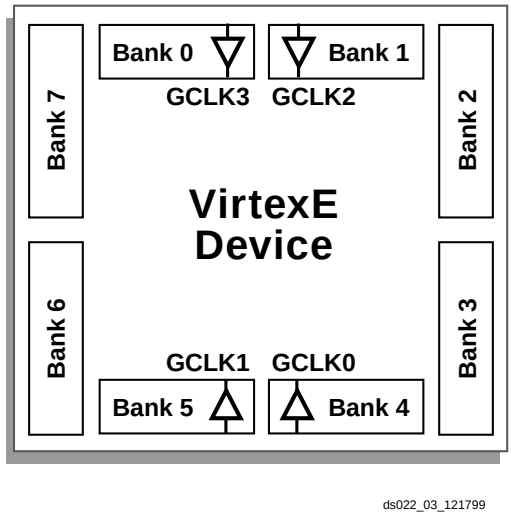


Figure 3: Virtex-E I/O Banks

Within a bank, output standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 4: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+, LVPECL
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+, BLVDS, LVDS
1.8 V	LVCMOS18, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage may be used within a bank.

In Virtex-E, input buffers with LVTTL, LVCMOS2, LVCMOS18, PCI33_3, PCI66_3 standards are supplied by V_{CCO} rather than V_{CCINT}. For these standards, only input and output buffers that have the same V_{CCO} can be mixed together.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a super set of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins may be left unconnected externally, or may be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

Configurable Logic Block

The basic building block of the Virtex-E CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex-E CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

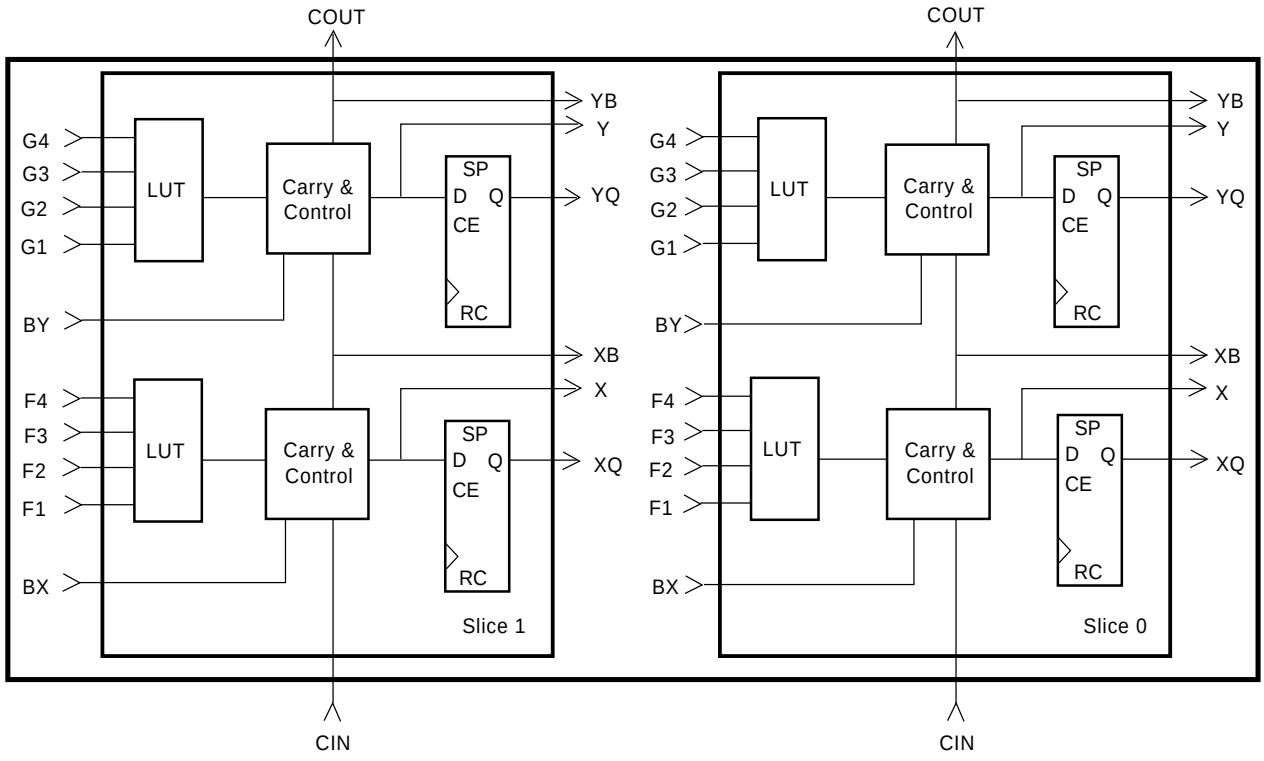


Figure 4: 2-Slice Virtex-E CLB

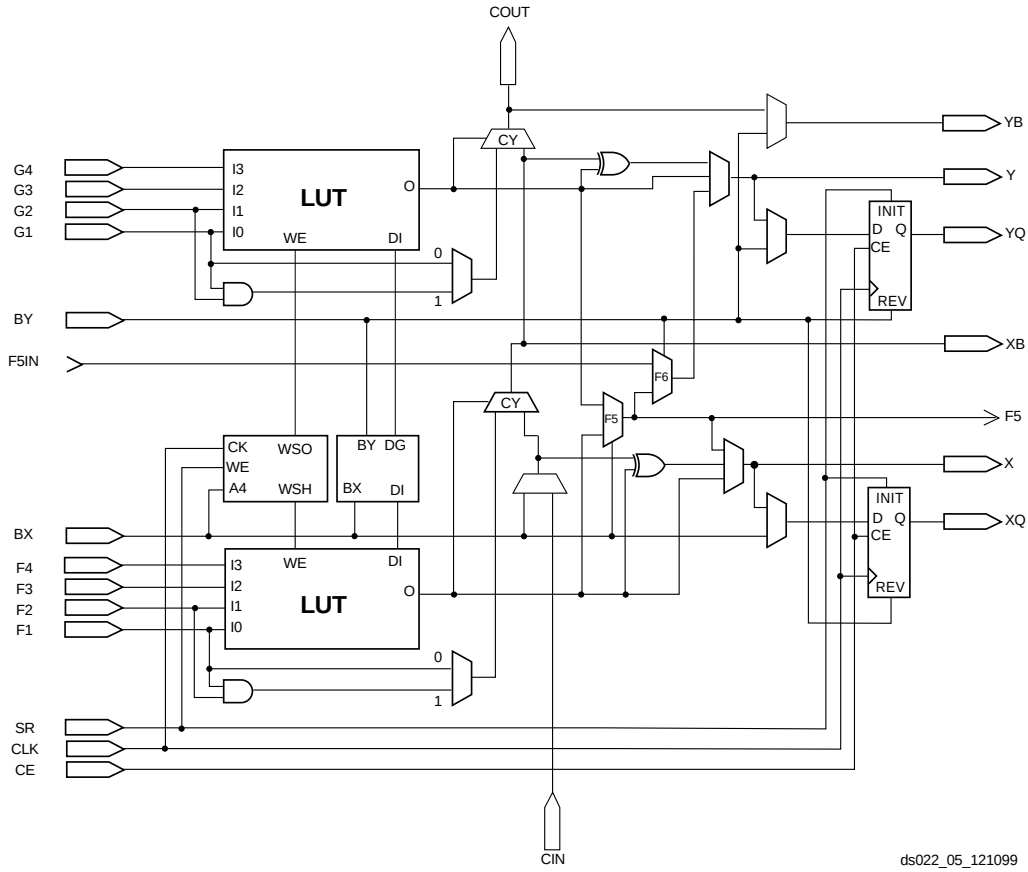


Figure 5: Detailed View of Virtex-E Slice

In addition to the four basic LCs, the Virtex-E CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex-E function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex-E LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex-E slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, two per slice. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex-E CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 2-bit full adder to be implemented within a slice. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex-E CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See "Dedicated Routing" on page 12. Each Virtex-E BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM

Virtex-E FPGAs incorporate large Block SelectRAM memories. These complement the Distributed SelectRAM memories that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns, starting at the left (column 0) and right outside edges and inserted every 12 CLB columns (see notes for smaller devices). Each memory block is four CLBs high, and each memory column extends the full height of the chip, immediately adjacent (to the right, except for column 0) of the CLB column locations indicated in Table 5.

Table 5: CLB/Block RAM Column Locations

Device/Col.	0	12	24	36	48	60	72	84	96	108	120
XCV50E	Columns 0, 6, 18, & 24										
XCV100E	Columns 0, 12, 18, & 30										
XCV200E	Columns 0, 12, 30, & 42										
XCV300E	√	√		√	√						
XCV400E	√	√			√	√					
XCV600E	√	√	√		√	√	√				
XCV1000E	√	√	√				√	√	√		
XCV1600E	√	√	√	√			√	√	√	√	
XCV2000E	√	√	√	√				√	√	√	√
XCV2600E	TBD										
XCV3200E	TBD										

Table 6 shows the amount of Block SelectRAM memory that is available in each Virtex-E device.

Table 6: Virtex-E Block SelectRAM Amounts

Virtex-E Device	# of Blocks	Block SelectRAM Bits
XCV50E	16	65,536
XCV100E	20	81,920
XCV200E	28	114,688
XCV300E	32	131,072
XCV400E	40	163,840
XCV600E	72	294,912
XCV1000E	96	393,216
XCV1600E	144	589,824

Table 6: Virtex-E Block SelectRAM Amounts

Virtex-E Device	# of Blocks	Block SelectRAM Bits
XCV2000E	160	655,360
XCV2600E	184	753,664
XCV3200E	208	851,968

Each Block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported (True Dual Port™) 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

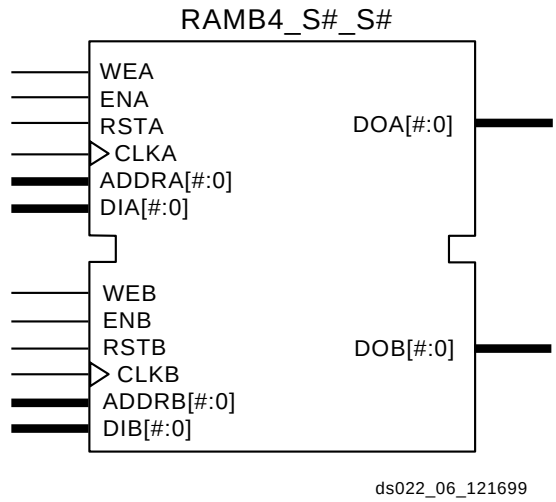


Figure 6: Dual-Port Block SelectRAM

Table 7 shows the depth and width aspect ratios for the Block SelectRAM. The Virtex-E Block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other Block SelectRAMs.

Table 7: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex-E routing architecture and its place-and-route software were defined in a joint optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

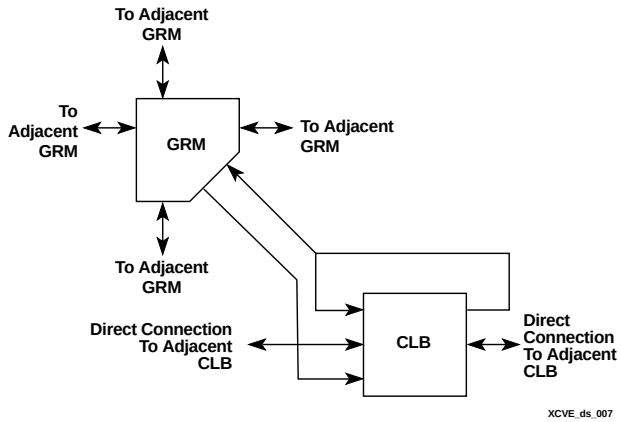


Figure 7: Virtex-E Local Routing

General Purpose Routing

Most Virtex-E signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the CLB rows and columns. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex-E devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex-E architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 8.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.Global Clock Distribution Network
- DLL Location

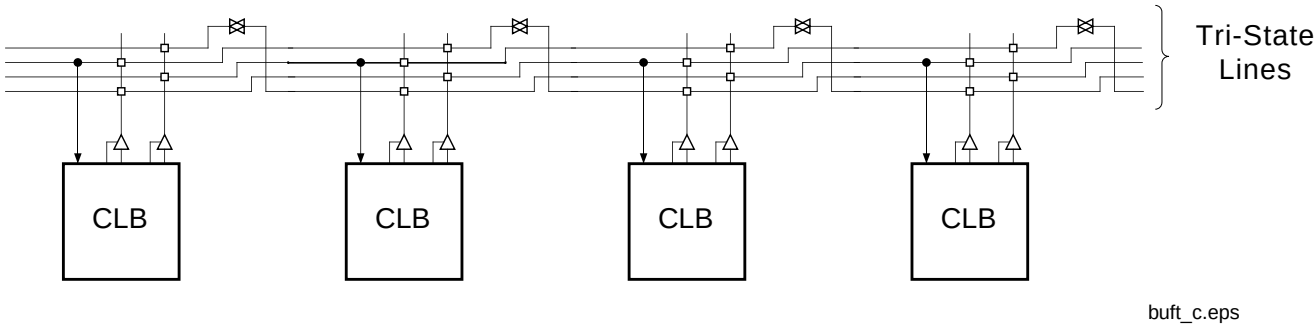


Figure 8: BUFT Connections to Dedicated Horizontal Bus LInes

Clock Routing

Clock Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex-E devices include two tiers of clock routing resources referred to as global and local clock routing resources.

- The global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These local resources are more flexible than the global resources since they are not restricted to routing only to clock pins.

Global Clock Distribution

Virtex-E provides high-speed, low-skew clock distribution through the global routing resources described above. A typical clock distribution net is shown in Figure 9.

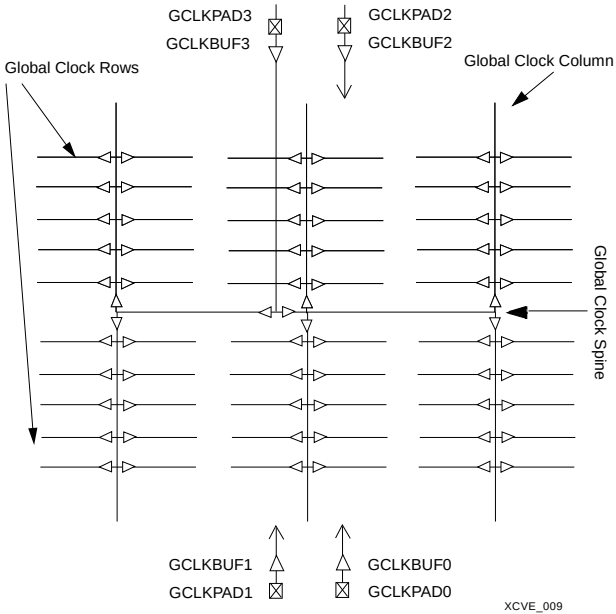


Figure 9: Global Clock Distribution Network

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Digital Delay-Locked Loop (DLL)

There are eight DLLs (Delay Lock Loops) per device, with four located at the top and four at the bottom, Figure 10. The DLLs can be used to eliminate skew between the clock input pad and the internal clock input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges arrive at internal flip-flops synchronized with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, and can double the clock or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

For more information about DLL functionality, see the Design Consideration section of the data sheet.

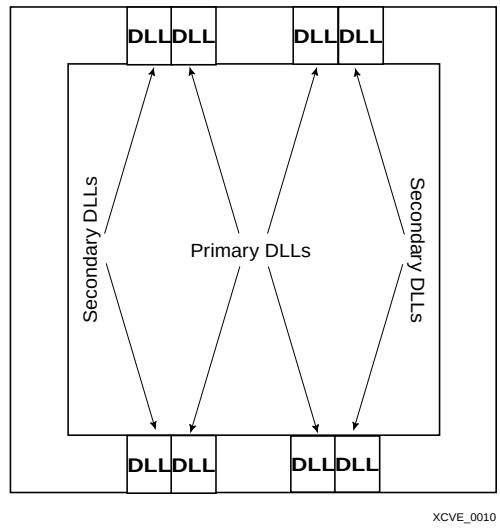


Figure 10: DLL Locations

Boundary Scan

Virtex-E devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The JTAG input pints (TDI, TMS, TCK) do not have a VCCO requirement and will operate with either 2.5 V or 3.3 V input signalling levels. The output pin (TDO) is sourced from the VCCO in bank 2, and for proper operation of LVTTL 3.3 V levels, the bank should be supplied with 3.3. V.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 8 lists the boundary-scan instructions supported in Virtex-E FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 11 is a diagram of the Virtex-E Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Table 8: Boundary Scan Instructions

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/PRE-LOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER1	00010	Access user-defined register 1
USER2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Tri-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

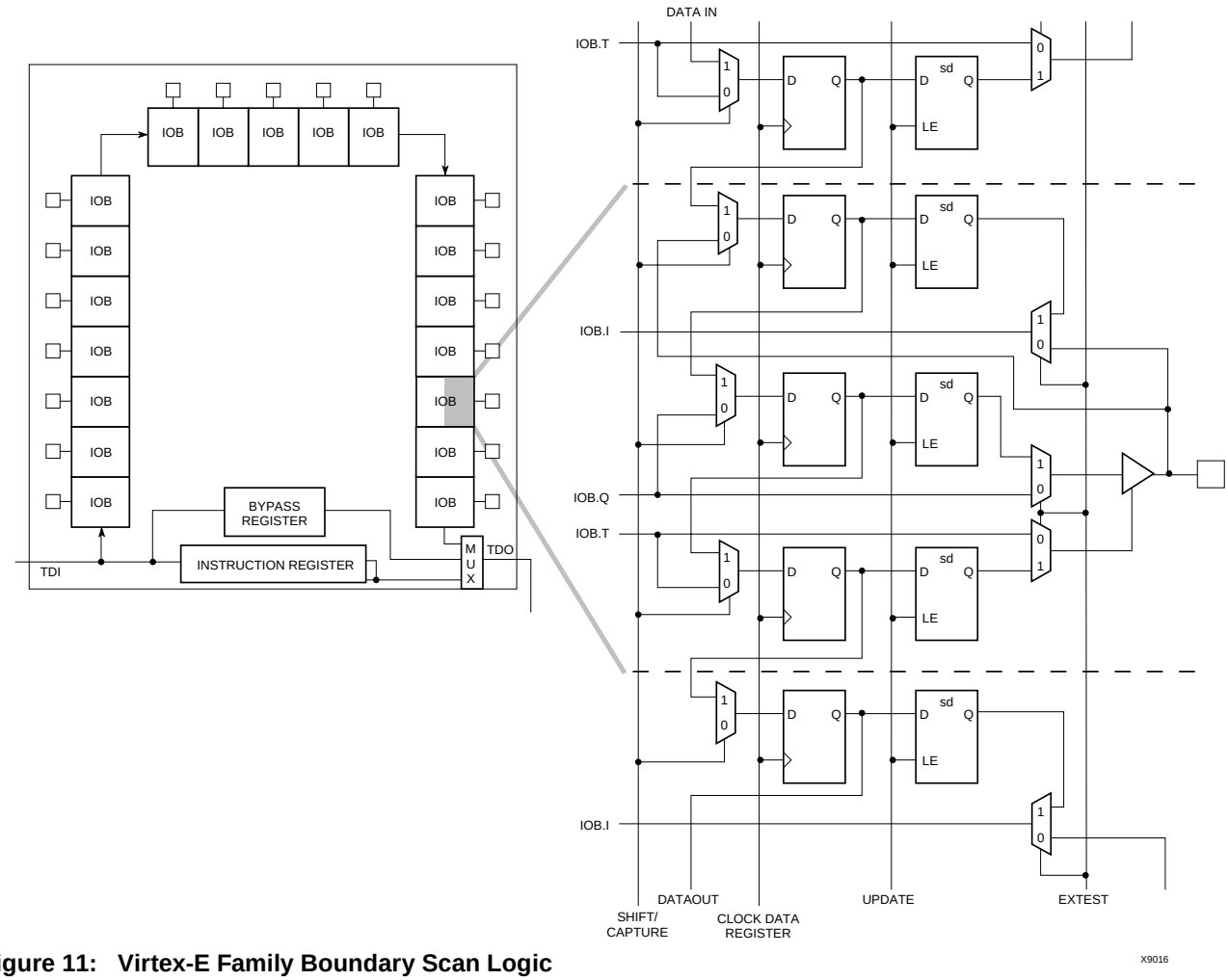


Figure 11: Virtex-E Family Boundary Scan Logic

Instruction Set

The Virtex-E Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 8.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (T DO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE).

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 12.

BSDL (Boundary Scan Description Language) files for Virtex-E Series devices are available on the Xilinx web site in the File Download area.

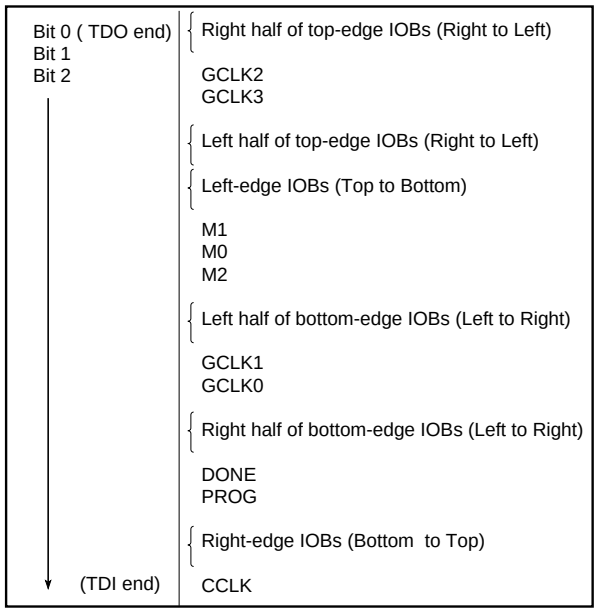


Figure 12: Boundary Scan Bit Sequence

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1,
where   v = the die version number
```

f = the family code (05 for Virtex-E family)

a = the number of CLB rows (ranges from 16 for XCV50E to 104 for XCV3200E)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 9: IDCODEs Assigned to Virtex-E FPGAs

FPGA	IDCODE
XCV50E	v0A10093h
XCV100E	v0A14093h
XCV200E	v0A1C093h
XCV300E	v0A20093h
XCV400E	v0A28093h
XCV600E	v0A30093h
XCV1000E	v0A40093h
XCV1600E	v0A48093h
XCV2000E	v0A50093h
XCV2600E	v0A5C093h
XCV3200E	v0A68093h

Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

Development System

Virtex-E FPGAs are supported by the Xilinx Foundation and Alliance Series CAE tools. The basic methodology for Virtex-E design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex-E design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and Alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex-E FPGAs are supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions,

latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRCE® static timing analyzer.

For in-circuit debugging, an optional download and readback cable is available. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex-E devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others may be re-used as general purpose inputs and outputs once configuration is complete.

The dedicated pins are the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{INIT}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the configuration mode chosen, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

For correct operation, these pins require a V_{CCO} of 3.3 V to permit LVTTL operation. All the pins affected fall in banks 2 or 3.

Configuration Modes

Virtex-E supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode (JTAG)

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 10.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 10: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Table 11 lists the total number of bits required to configure each device.

Table 11: Virtex-E Bit-stream Lengths

Device	# of Configuration Bits
XCV50E	630,048
XCV100E	863,840
XCV200E	1,442,106
XCV300E	1, 875,648
XCV400E	2,693,440
XCV600E	3,961,632
XCV1000E	6,587,520
XCV1600E	8,308,992
XCV2000E	10,159,648
XCV2600E	TBD
XCV3200E	TBD

Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but will not cause a problem for mixed configuration chains. This change was made to improve serial-configuration rates for Virtex and Virtex-E only chains.

Figure 13 shows a full master/slave system. A Virtex-E device in slave serial mode should be connected as shown in the third device from the left

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. Figure 14 shows slave-serial configuration timing.

Table 12 provides more detail about the characteristics shown in Figure 14. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Table 12: Master/Slave Serial Mode Programming Switching

	Description	Figure 14 References	Symbol	Values	Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0/0.0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{SCKD}	5.0/0.0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	

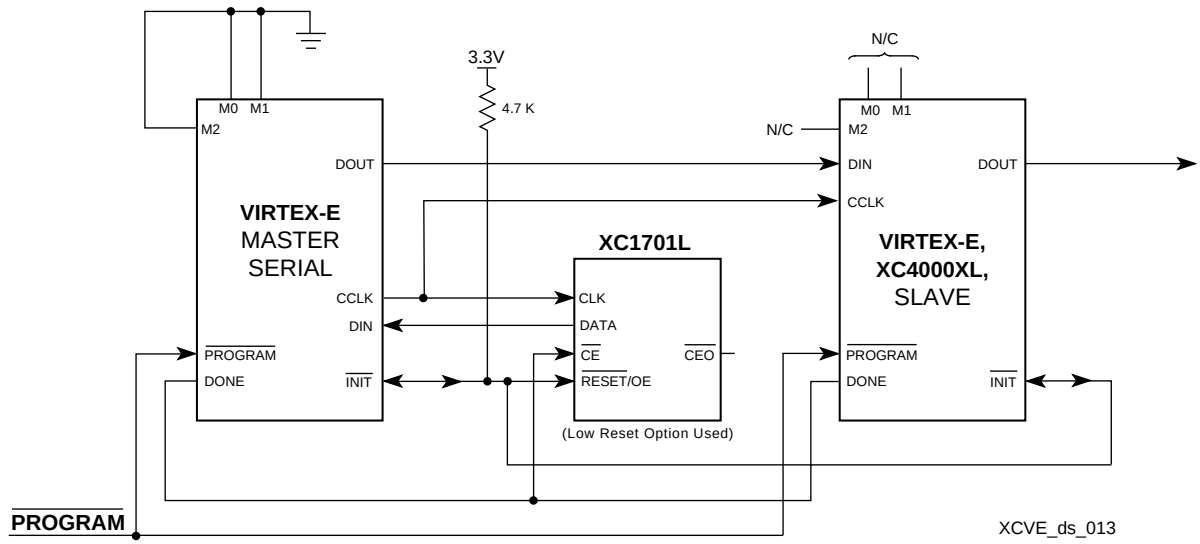


Figure 13: Master/Slave Serial Mode Circuit Diagram

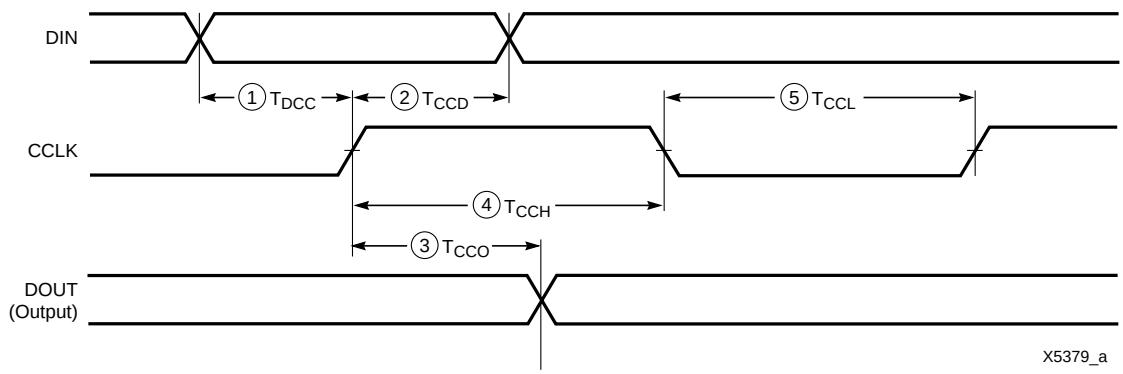


Figure 14: Slave Serial Mode Programming Switching Characteristics

Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is approximately 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 13 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex-E FPGA serially appears in Figure 15.

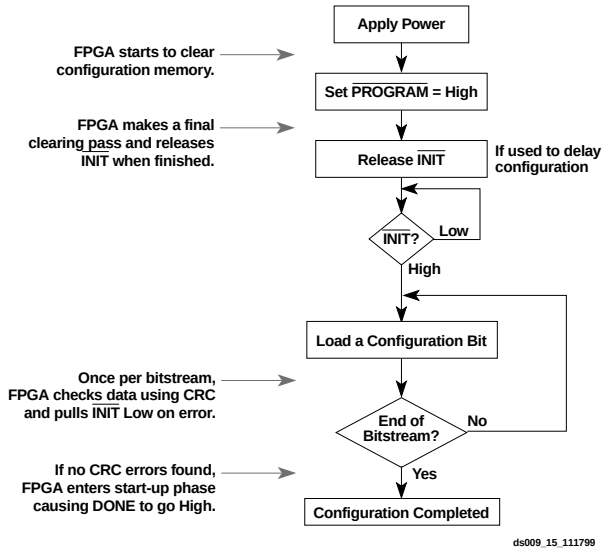


Figure 15: Serial Configuration Flowchart

Figure 16 shows the timing of master-serial configuration. Master serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 12 shows the timing information for Figure 16.

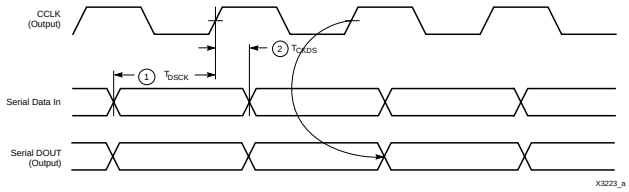


Figure 16: Master Serial Mode Programming Switching Characteristics

At power-up, Vcc must rise from 1.0 V to Vcc min in less than 50 ms, otherwise delay configuration by pulling PROGRAM Low until Vcc is valid.

SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select (CS) signal and a Write signal (WRITE). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If WRITE is not asserted, configuration data is read out of the FPGA as part of a readback operation.

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex-E FPGAs can be configured using the SelectMAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, WRITE, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the CS pin of each device in turn and writing the appropriate data. See Table 13 for SelectMAP Write Timing Characteristics.

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of CS, illustrated in Figure 17.

1. Assert WRITE and CS Low. Note that when CS is asserted on successive CCLKs, WRITE must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
2. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while CS is Low and WRITE is High. Similarly, while WRITE is High, no more that one CS should be asserted.
3. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
4. Repeat steps 2 and 3 until all the data has been sent.
5. De-assert CS and WRITE

Table 13: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0/0.0	ns, min
	$\overline{CS}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0/0.0	ns, min
	$\overline{WRITE}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0/0.0	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

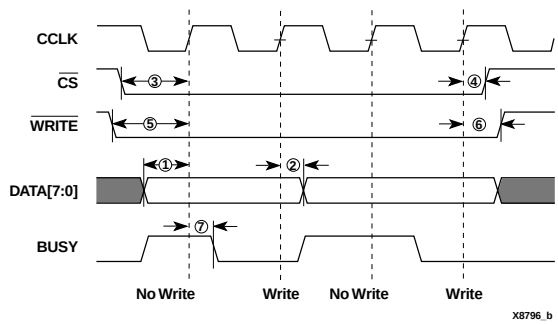


Figure 17: Write Operations

A flowchart for the write operation appears in Figure 18. Note that if CCLK is slower than f_{CCNH}, the FPGA will never assert BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

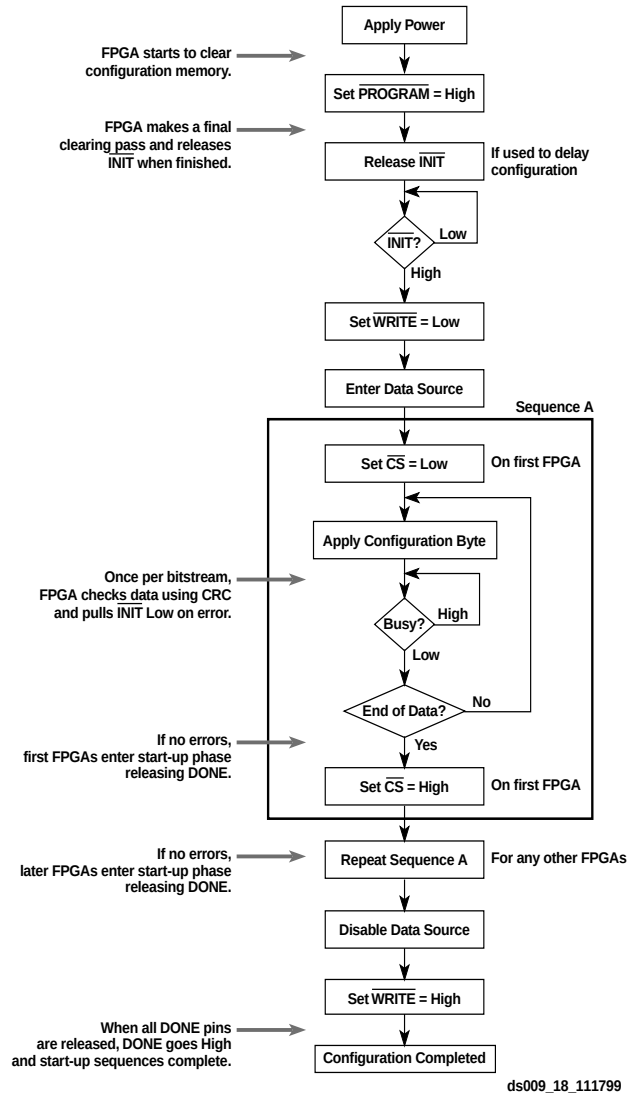


Figure 18: SelectMAP Flowchart for Write Operations

To initiate an abort during a write operation, de-assert $\overline{\text{WRITE}}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 19.

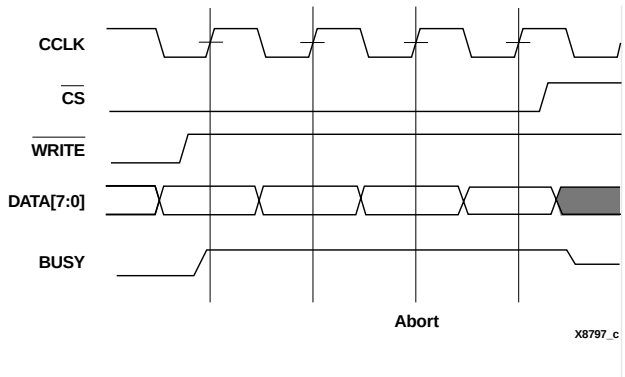


Figure 19: SelectMAP Write Abort Waveforms

Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or <001> on the mode pins (M2, M1, M0).

Configuration Sequence

The configuration of Virtex-E devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process may also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 20. The corresponding timing characteristics are listed in Table 14.

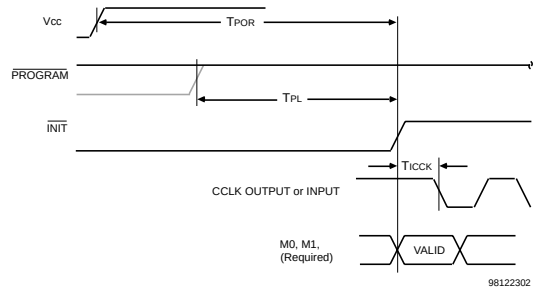


Figure 20: Power-up Timing Configuration Signals

Table 14: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global tri-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events may be changed. In addition, the GTS, GSR, and GWE events may be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start synchronously. The sequence may also be paused at any stage until lock has been achieved on any or all DLLs.

Readback

The configuration data stored in the Virtex-E configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUT RAMs, and block RAMs. This capability is used for real-time debugging. For more detailed information, see application note XAPP138 “Virtex FPGA Series Configuration and Readback”.

Virtex-E Electrical Characteristics

Definition of Terms

Data sheets may be designated as Advance or Preliminary. The status of specifications in these data sheets is as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

All specifications are subject to change without notice.

DC Characteristics

Absolute Maximum Ratings

Symbol	Description			Units
V_{CCINT}	Internal Supply voltage relative to GND		-0.5 to 2.0	V
V_{CCO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{REF}	Input Reference Voltage		-0.5 to 4.0	V
V_{IN}	Input voltage relative to GND		-0.5 to 4.0	V
V_{TS}	Voltage applied to 3-state output		-0.5 to 4.0	V
V_{CC}	Longest Supply Voltage Rise Time from 0 V - 1.71 V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temp. (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Power supplies may turn on in any order.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Internal Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.8 - 5%	1.8 + 5%	V
	Internal Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	1.8 - 5%	1.8 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.2	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	1.2	3.6	V
T_{IN}	Input signal transition time			250	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)		All	1.5		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)		All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)		XCV50E			
			XCV100E			
			XCV200E			
			XCV300E			
			XCV400E			
			XCV600E			
			XCV1000E			
			XCV1600E			
			XCV2000E			
			XCV2600E			
			XCV3200E			
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)		XCV50E			
			XCV100E			
			XCV200E			
			XCV300E			
			XCV400E			
			XCV600E			
			XCV1000E			
			XCV1600E			
			XCV2000E			
			XCV2600E			
			XCV3200E			
I_{REF}	V_{REF} current per V_{REF} pin		All			µA
I_L	Input or output leakage current		All			µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages	All			pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)		All	Note 2		mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)			Note 2		mA

Note 1: With no output current loads, no active input pull-up resistors, all I/O pins Tri-stated and floating.
Note 2: Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

DC Input and Output Levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	- 0.5	0.8	2.0	3.6	0.4	2.4	24	- 24
LVCMOS2	- 0.5	0.7	1.7	3.6	0.4	1.9	12	- 12
LVCMOS18	- 0.5	20% V_{CCO}	70% V_{CCO}	1.95	0.4	V_{CCO} - 0.4	8	- 8
PCI, 3.3 V	- 0.5	30% V_{CCO}	50% V_{CCO}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
GTL	- 0.5	V_{REF} - 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL III	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL IV	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
SSTL3 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	8	-8
SSTL3 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.8	V_{REF} + 0.8	16	-16
SSTL2 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.61	V_{REF} + 0.61	7.6	-7.6
SSTL2 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.80	V_{REF} + 0.80	15.2	-15.2
CTT	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
AGP	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Note 1: V_{OL} and V_{OH} for lower drive currents are sample tested.
Note 2: Tested according to the relevant specifications.

LVDS DC Specifications

DC Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage	V_{CCO}		2.375	2.5	2.625	V
Output High Voltage for Q and $\overline{Q}$	V_{OH}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.25	1.425	1.6	V
Output Low Voltage for Q and $\overline{Q}$	V_{OL}	R_T = 100 Ω across Q and $\overline{Q}$ signals	0.9	1.075	1.25	V
Differential Output Voltage (Q - $\overline{Q}$), Q = High (($\overline{Q}$ - Q), $\overline{Q}$ = High	V_{ODIFF}	R_T = 100 Ω across Q and $\overline{Q}$ signals	250	350	450	mV
Output Common-Mode Voltage	V_{OCM}	R_T = 100 Ω across Q and $\overline{Q}$ signals	1.125	1.25	1.375	V
Differential Input Voltage (Q - $\overline{Q}$), Q = High (($\overline{Q}$ - Q), $\overline{Q}$ = High	V_{IDIFF}	Common-mode input voltage = 1.25 V	100	350	NA	mV
Input Common-Mode Voltage	V_{ICM}	Differential input voltage = ±350 mV	0.2	1.25	2.2	V

Note: Refer to the Design Consideration section for termination schematics.

LVPECL DC Specifications

These values are valid when driving a 100 Ω differential load only, i.e., a 100 Ω resistor between the two receiver pins. The V_{OH} levels are 200 mV below standard LVPECL levels and are compatible with devices tolerant of lower common-mode ranges. The following table summarizes the DC output specifications of LVPECL.

DC Parameter	Min	Max	Min	Max	Min	Max	Units
V_{CCO}	3.0		3.3		3.6		V
V_{OH}	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{OL}	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{IH}	1.49	2.72	1.49	2.72	1.49	2.72	V
V_{IL}	0.86	2.125	0.86	2.125	0.86	2.125	V
Differential Input Voltage	0.3	-	0.3	-	0.3	-	V

Virtex-E Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex-E devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 28.

			Speed Grade			
Description	**Device**	**Symbol**	**-8**	**-7**	**-6**	**Units**
Propagation Delays						
Pad to I output, no delay	All	T_{IOPI}		0.8	0.8	ns, max
Pad to I output, with delay	XCV50E	T_{IOPID}		1.0	1.0	ns, max
	XCV100E			1.0	1.0	ns, max
	XCV200E			1.0	1.0	ns, max
	XCV300E			1.0	1.0	ns, max
	XCV400E			1.0	1.0	ns, max
	XCV600E			1.0	1.0	ns, max
	XCV1000E			1.1	1.1	ns, max
	XCV1600E			1.1	1.1	ns, max
	XCV2000E			1.1	1.1	ns, max

IOB Input Switching Characteristics (Continued)

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 28.

			Speed Grade			
Description	**Device**	**Symbol**	**-8**	**-7**	**-6**	**Units**
Propagation Delays						
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}		1.5	1.6	ns, max
Pad to output IQ via transparent latch, with delay	XCV50E	T_{IOPLID}		3.0	3.1	ns, max
	XCV100E			3.0	3.1	ns, max
	XCV200E			3.2	3.3	ns, max
	XCV300E			3.2	3.3	ns, max
	XCV400E			3.3	3.4	ns, max
	XCV600E			3.6	3.7	ns, max
	XCV1000E			3.6	3.7	ns, max
	XCV1600E			3.7	3.8	ns, max
	XCV2000E			3.7	3.8	ns, max
Sequential Delays						
Clock CLK to output IQ	All	T_{IOCKIQ}		0.7	0.7	ns, max
Setup and Hold Times with respect to Clock at IOB Input Register						
Pad, no delay	All	T_{IOPICK}/T_{IOICKP}		1.4 / 0	1.5 / 0	ns, min
Pad, with delay	XCV50E	$T_{IOPICKD}/T_{IOICKPD}$		2.9 / 0	2.9 / 0	ns, min
	XCV100E			2.9 / 0	2.9 / 0	ns, min
	XCV200E			3.1 / 0	3.1 / 0	ns, min
	XCV300E			3.1 / 0	3.1 / 0	ns, min
	XCV400E			3.2 / 0	3.2 / 0	ns, min
	XCV600E			3.5 / 0	3.5 / 0	ns, min
	XCV1000E			3.5 / 0	3.5 / 0	ns, min
	XCV1600E			3.6 / 0	3.6 / 0	ns, min
	XCV2000E			3.6 / 0	3.6 / 0	ns, min
ICE input	All	$T_{IOICECK}/T_{IOCKICE}$		0.7 / 0	0.7 / 0	ns, min
SR input (IFF, synchronous)	All	$T_{IOSRCKI}$		0.9	1.0	ns, min
Set/Reset Delays						
SR input to IQ (asynchronous)	All	T_{IOSRIQ}		1.2	1.4	ns, max
GSR to output IQ	All	T_{GSRQ}		8.5	9.7	ns, max

Note: A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Note: Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 16.

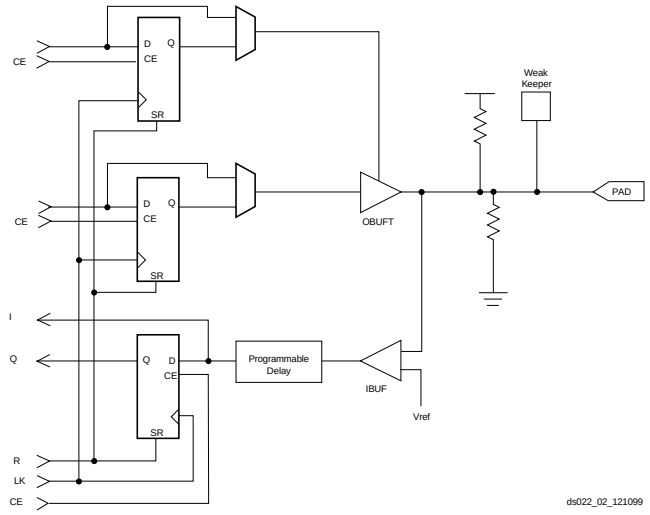


Figure 21: Virtex-E Input/Output Block (IOB)

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade			Units
			-8	-7	-6	
Data Input Delay Adjustments						
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL		0.0	0.0	ns
	$T_{ILVCMOS2}$	LVCMOS2		0.0	0.0	ns
	$T_{ILVCMOS18}$	LVCMOS18		+0.20	+0.20	ns
	T_{ILVDS}	LVDS		+0.15	+0.15	ns
	$T_{ILVPECL}$	LVPECL		+0.15	+0.15	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V		+0.08	+0.08	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V		-0.11	-0.11	ns
	T_{IGTL}	GTL		+0.14	+0.14	ns
	$T_{IGTLPLUS}$	GTL+		+0.14	+0.14	ns
	T_{IHSTL}	HSTL		+0.04	+0.04	ns
	T_{IHSTL2}	SSTL2		+0.04	+0.04	ns
	T_{IHSTL3}	SSTL3		+0.04	+0.04	ns
	T_{ICTTL}	CTT		+0.10	+0.10	ns
	T_{IAGP}	AGP		+0.04	+0.04	ns

Note: Input timing i for LVTTL is measured at 1.4 V. For other I/O standards, see Table 16.

IOB Output Switching Characteristics, Figure 21

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 30.

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Propagation Delays					
O input to Pad	T_{IOOP}		2.7	2.9	ns, max
O input to Pad via transparent latch	T_{IOOLP}		3.1	3.4	ns, max
3-State Delays					
T input to Pad high-impedance (Note 1)	T_{IOTHZ}		1.7	1.9	ns, max
T input to valid data on Pad	T_{IOTON}		2.9	3.1	ns, max
T input to Pad high-impedance via transparent latch (Note 1)	$T_{IOTLPHZ}$		2.0	2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		3.2	3.4	ns, max
GTS to Pad high impedance (Note 1)	T_{GTS}		4.6	4.9	ns, max
Sequential Delays					
Clock CLK to Pad	T_{IOCKP}		2.8	2.9	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 1)	T_{IOCKHZ}		2.0	2.2	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		3.2	3.4	ns, max
Setup and Hold Times before/after Clock CLK					
O input	T_{IOOCK}/T_{IOCKO}		1.0 / 0	1.1 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$		0.7 / 0	0.7 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOSRCKO}$		0.9 / 0	1.0 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}		0.6 / 0	0.7 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$		0.7 / 0	0.8 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$		0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays					
SR input to Pad (asynchronous)	T_{IOSRP}		3.3	3.5	ns, max
SR input to Pad high-impedance (asynchronous) (Note 1)	T_{IOSRHZ}		2.4	2.7	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		3.7	3.9	ns, max
GSR to Pad	T_{IOGSRQ}		8.5	9.7	ns, max

Note: A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

Note 1: Tri-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

			Speed Grade			
Description	**Symbol**	**Standard**	**-8**	**-7**	**-6**	**Units**
Output Delay Adjustments						
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow,2 mA		+14.7	+14.7	ns
	T_{OLVTTL_S4}	4 mA		+7.5	+7.5	ns
	T_{OLVTTL_S6}	6 mA		+4.8	+4.8	ns
	T_{OLVTTL_S8}	8 mA		+3.0	+3.0	ns
	T_{OLVTTL_S12}	12 mA		+1.9	+1.9	ns
	T_{OLVTTL_S16}	16 mA		+1.7	+1.7	ns
	T_{OLVTTL_S24}	24 mA		+1.3	+1.3	ns
	T_{OLVTTL_F2}	LVTTL, Fast,2 mA		+13.1	+13.1	ns
	T_{OLVTTL_F4}	4 mA		+5.3	+5.3	ns
	T_{OLVTTL_F6}	6 mA		+3.1	+3.1	ns
	T_{OLVTTL_F8}	8 mA		+1.0	+1.0	ns
	T_{OLVTTL_F12}	12 mA		0.0	0.0	ns
	T_{OLVTTL_F16}	16 mA		-0.05	-0.05	ns
	T_{OLVTTL_F24}	24 mA		-0.20	-0.20	ns
	$T_{OLVCMOS\_2}$	LVCMOS2		+0.09	+0.09	ns
	$T_{OLVCMOS\_18}$	LVCMOS18		+0.7	+0.7	ns
	T_{OLVDS}	LVDS		-1.2	-1.2	ns
	$T_{OLVPECL}$	LVPECL		-0.41	-0.41	ns
	$T_{OPCI\_33\_3}$	PCI, 33 MHz, 3.3 V		+2.3	+2.3	ns
	$T_{OPCI\_66\_3}$	PCI, 66 MHz, 3.3 V		-0.41	-0.41	ns
	T_{OGTL}	GTL		+0.49	+0.49	ns
	T_{OGTLP}	GTL+		+0.8	+0.8	ns
	T_{OHSTL_I}	HSTL I		-0.51	-0.51	ns
	T_{OHSTL_IIII}	HSTL III		-0.9	-0.9	ns
	T_{OHSTL_IV}	HSTL IV		-1.0	-1.0	ns
	T_{OSSTL2_I}	SSTL2 I		-0.51	-0.51	ns
	T_{OSSTL2_II}	SSTL2 II		-1.0	-1.0	ns
	T_{OSSTL3_I}	SSTL3 I		-0.51	-0.51	ns
	T_{OSSTL3_II}	SSTL3 II		-0.9	-0.9	ns
	T_{OCTT}	CTT		-0.6	-0.6	ns
	T_{OAGP}	AGP		-0.9	-0.9	ns

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} are based on the standard capacitive load (Csl) for each IO standard as listed in Table 15.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 15: Constants for Use in Calculation of T_{ioop}

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.10
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
LVCMOS18	35	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Note 1: IO parameter measurements are made with the capacitance values shown above. See the "Application Examples" on page 62 for appropriate terminations.
Note 2: IO standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Table 16: Delay Measurement Methodology

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	0.80
GTL+	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	1.0
HSTL Class I	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.75
HSTL Class III	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} -1.0	V_{REF} +1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} -0.75	V_{REF} +0.75	V_{REF}	1.25
CTT	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	1.5
AGP	V_{REF} - (0.2xV_{CCO})	V_{REF} + (0.2xV_{CCO})	V_{REF}	Per AGP Spec
LVDS	1.2 - 0.125	1.2 + 0.125	1.2	
LVPECL	1.6 - 0.3	1.6 + 0.3	1.6	

Note 1: Input waveform switches between V_L and V_H.
Note 2: Measurements are made at V_{REF} (Typ), Maximum, and Minimum. Worst-case values are reported.
Note 3: IO parameter measurements are made with the capacitance values shown in Table 14. See the "Application Examples" on page 62 for appropriate terminations.
Note 4: IO standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
GCLK IOB and Buffer					
Global Clock PAD to output.	T_{GPIO}		0.7	0.7	ns, max
Global Clock Buffer I input to O output	T_{GIO}		0.7	0.7	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used, see Figure 22. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Combinatorial Delays					
4-input function: F/G inputs to X/Y outputs	T_{ILO}		0.42	0.47	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}		0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}		0.8	0.9	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}		0.9	1.0	ns, max
6-input function: F5IN input to Y output	T_{F5INY}		0.16	0.17	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}		0.6	0.7	ns, max
BY input to YB output	T_{BYYB}		0.46	0.51	ns, max
Sequential Delays					
FF Clock CLK to XQ/YQ outputs	T_{CKO}		0.9	1.0	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}		0.9	1.0	ns, max
Setup and Hold Times before/after Clock CLK					
4-input function: F/G Inputs	T_{ICK}/T_{ICK}		0.9 / 0	1.0 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}		1.3 / 0	1.4 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}		0.7 / 0	0.8 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}		1.4 / 0	1.6 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}		0.6 / 0	0.7 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}		0.7 / 0	0.7 / 0	ns, min
SR/BY inputs (synchronous)	T_{RCK}/T_{CKR}		0.52 / 0	0.6 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{CH}		1.3	1.4	ns, min
Minimum Pulse Width, Low	T_{CL}		1.3	1.4	ns, min
Set/Reset					
Minimum Pulse Width, SR/BY inputs	T_{RPW}		2.1	2.4	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}		0.9	1.0	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG}		384	357	MHz

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

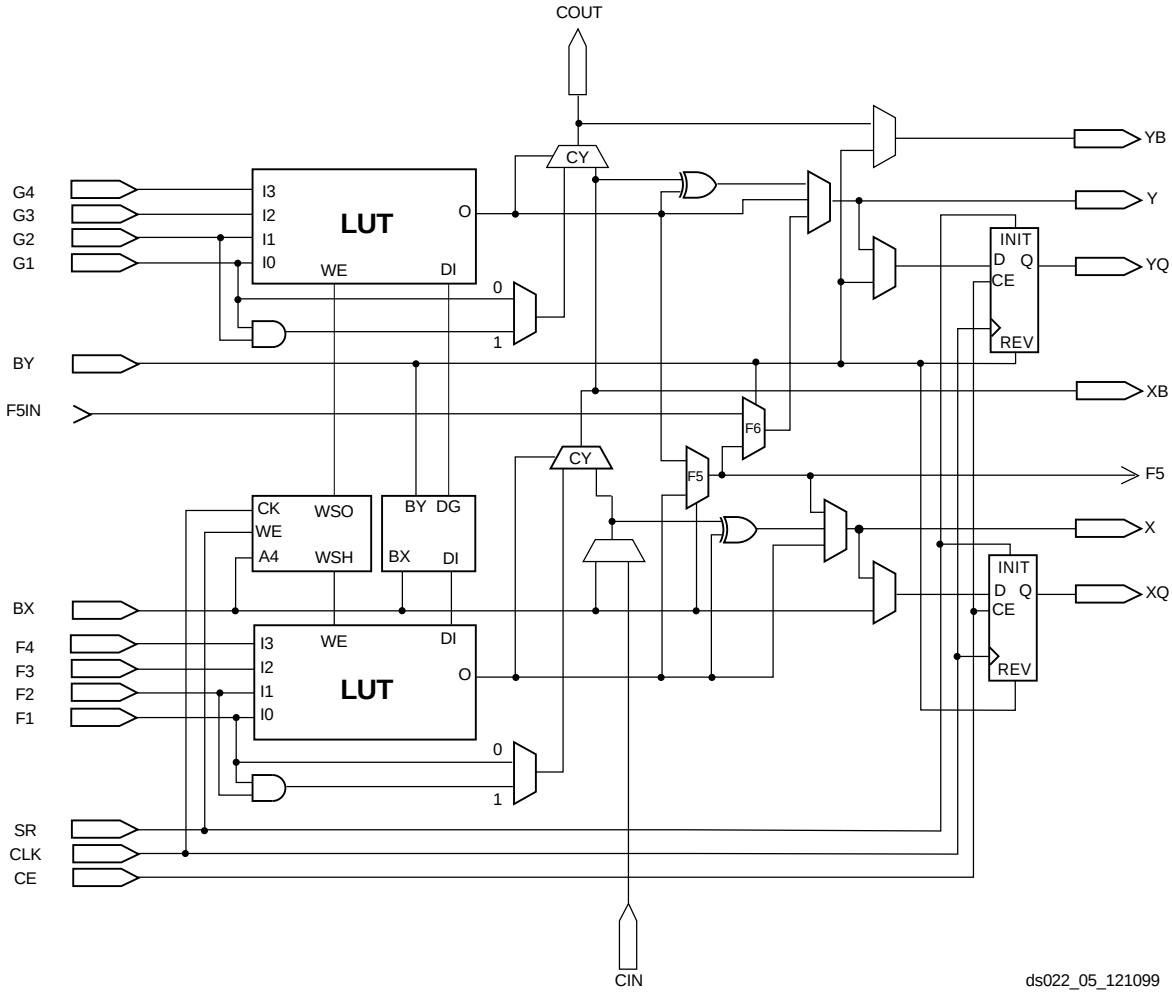


Figure 22: Detailed View of Virtex-E Slice

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade			
Description	**Symbol**	**-8**	**-7**	**-6**	**Units**
Combinatorial Delays					
F operand inputs to X via XOR	T_{OPX}		0.8	0.8	ns, max
F operand input to XB output	T_{OPXB}		0.8	0.9	ns, max
F operand input to Y via XOR	T_{OPY}		1.4	1.5	ns, max
F operand input to YB output	T_{OPYB}		1.3	1.4	ns, max
F operand input to COUT output	T_{OPCYF}		1.0	1.1	ns, max
G operand inputs to Y via XOR	T_{OPGY}		0.8	0.9	ns, max
G operand input to YB output	T_{OPGYB}		1.3	1.5	ns, max
G operand input to COUT output	T_{OPCYG}		1.0	1.1	ns, max
BX initialization input to COUT	T_{BXCY}		0.48	0.54	ns, max
CIN input to X output via XOR	T_{CINX}		0.6	0.7	ns, max
CIN input to XB	T_{CINXB}		0.07	0.08	ns, max
CIN input to Y via XOR	T_{CINY}		0.7	0.7	ns, max
CIN input to YB	T_{CINYB}		0.36	0.40	ns, max
CIN input to COUT output	T_{BYP}		0.10	0.11	ns, max
Multiplier Operation					
F1/2 operand inputs to XB output via AND	T_{FANDXB}		0.22	0.25	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}		0.8	0.9	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}		0.49	0.55	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}		0.45	0.50	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}		0.19	0.21	ns, max
Setup and Hold Times before/after Clock CLK					
CIN input to FFX	T_{CCKX}/T_{CKCX}		1.1 / 0	1.2 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}		1.2 / 0	1.3 / 0	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Distributed RAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Sequential Delays					
Clock CLK to X/Y outputs (WE active)	T_{SHCKO}		1.7	1.9	ns, max
Shift-Register Mode Clock CLK to X/Y outputs			1.7	1.9	ns, max
Setup and Hold Times before/after Clock CLK					
F/G address inputs	T_{AS}/T_{AH}		0.42 / 0	0.47 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		0.53 / 0	0.6 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}		0.7 / 0	0.8 / 0	ns, min
Shift-Register Mode					
BX/BY data inputs (DIN)	T_{SHDICK}		0.53 / 0	0.6 / 0	ns, min
CE input (WS)	T_{SHCECK}		0.7 / 0	0.8 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{WPH}		2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{WPL}		2.1	2.4	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		4.2	4.8	ns, min
Shift-Register Mode					
Minimum Pulse Width, High	T_{SRPH}		2.1	2.4	ns, min
Minimum Pulse Width, Low	T_{SRPL}		2.1	2.4	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

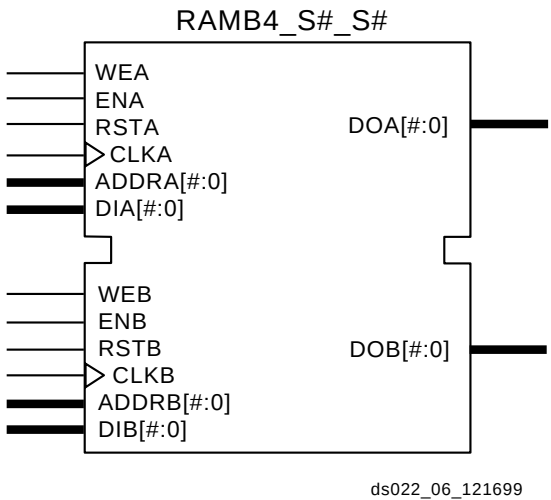


Figure 23: Dual-Port Block SelectRAM

Block RAM Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Sequential Delays					
Clock CLK to DOUT output	T_{BCKO}		2.6	2.9	ns, max
Setup and Hold Times before Clock CLK					
ADDR inputs	T_{BACK}/T_{BCKA}		1.0 / 0	1.1 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}		1.0 / 0	1.1 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}		2.2 / 0	2.5 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}		2.1 / 0	2.3 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}		2.0 / 0	2.2 / 0	ns, min
Clock CLK					
Minimum Pulse Width, High	T_{BPWH}		1.4	1.5	ns, min
Minimum Pulse Width, Low	T_{BPWL}		1.4	1.5	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
Combinatorial Delays					
IN input to OUT output	T_{IO}		0	0	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}		0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

Description	Symbol	Speed Grade			Units
		-8	-7	-6	
TMS and TDI Setup times before TCK	T_{TAPTK}			4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}			2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}			11.0	ns, max
Maximum TCK clock frequency	F_{TCK}			33	MHz, max

Virtex-E Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 30.	$T_{ICKOFDLL}$	XCV50E		3.1	3.1	ns
		XCV100E		3.1	3.1	ns
		XCV200E		3.1	3.1	ns
		XCV300E		3.1	3.1	ns
		XCV400E		3.1	3.1	ns
		XCV600E		3.1	3.1	ns
		XCV1000E		3.1	3.1	ns
		XCV1600E		3.1	3.1	ns
		XCV2000E		3.1	3.1	ns

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 15 and Table 16.
DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Max**	**Max**	**Max**	
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 30.	T_{ICKOF}	XCV50E		4.4	4.6	ns
		XCV100E		4.4	4.6	ns
		XCV200E		4.5	4.7	ns
		XCV300E		4.5	4.7	ns
		XCV400E		4.6	4.8	ns
		XCV600E		4.7	4.9	ns
		XCV1000E		4.8	5.0	ns
		XCV1600E		4.9	5.1	ns
		XCV2000E		5.0	5.2	ns

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 50% V_{CC} threshold with 35 pF external capacitive load. For other I/O standards and different loads, see Table 15 and Table 16.

Virtex-E Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 28.						
No Delay	T_{PSDLL}/T_{PHDLL}	XCV50E		1.5 / -0.4	1.5 / -0.4	ns
Global Clock and IFF, with DLL		XCV100E		1.5 / -0.4	1.5 / -0.4	ns
		XCV200E		1.5 / -0.4	1.5 / -0.4	ns
		XCV300E		1.5 / -0.4	1.5 / -0.4	ns
		XCV400E		1.5 / -0.4	1.5 / -0.4	ns
		XCV600E		1.5 / -0.4	1.5 / -0.4	ns
		XCV1000E		1.5 / -0.4	1.5 / -0.4	ns
		XCV1600E		1.5 / -0.4	1.5 / -0.4	ns
		XCV2000E		1.5 / -0.4	1.5 / -0.4	ns

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

DLL output jitter is already included in the timing calculation.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

		Speed Grade	-8	-7	-6	Units
Description	**Symbol**	**Device**	**Min**	**Min**	**Min**	
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 28.						
Full Delay	T_{PSFD}/T_{PHFD}	XCV50E		2.3 / 0	2.3 / 0	ns
Global Clock and IFF, without DLL		XCV100E		2.3 / 0	2.3 / 0	ns
		XCV200E		2.4 / 0	2.4 / 0	ns
		XCV300E		2.5 / 0	2.5 / 0	ns
		XCV400E		2.5 / 0	2.5 / 0	ns
		XCV600E		2.6 / 0	2.6 / 0	ns
		XCV1000E		2.8 / 0	2.8 / 0	ns
		XCV1600E		3.0 / 0	3.0 / 0	ns
		XCV2000E		3.2 / 0	3.2 / 0	ns

IFF = Input Flip-Flop or Latch

Note: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

		Speed Grade	-8		-7		-6		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Frequency (CLKDLLHF)	$F_{CLKINHF}$				60	320	60	260	MHz
Input Clock Frequency (CLKDLL)	$F_{CLKINLF}$				25	160	25	130	MHz
Input Clock Low/High Pulse Width	T_{DLLPW}	≥2 5 MHz			5.0		5.0		ns
		≥ 50 MHz			3.0		3.0		ns
		≥100 MHz			2.4		2.4		ns
		≥ 150 MHz			2.0		2.0		ns
		≥ 200 MHz			1.8		1.8		ns
		≥ 250 MHz			1.5		1.5		ns
		≥ 300 MHz			1.3		NA		ns

Note: All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

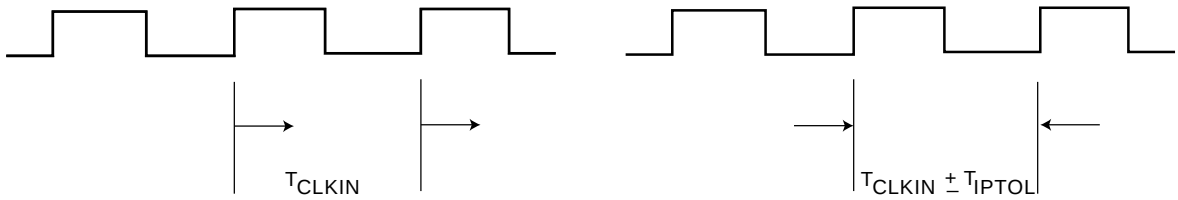
DLL Clock Tolerance, Jitter, and Phase Information

All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output[1]	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO[2]	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL[3]	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO[4]	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL[5]	T_{PHOOM}			± 200		± 200	ps

Note 1: **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
Note 2: **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
Note 3: **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
Note 4: **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
Note 5: **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
Note 6: All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Period Tolerance: the allowed input clock period change in nanoseconds.



Output Jitter: the difference between an ideal reference clock edge and the actual design.

Phase Offset and Maximum Phase Difference

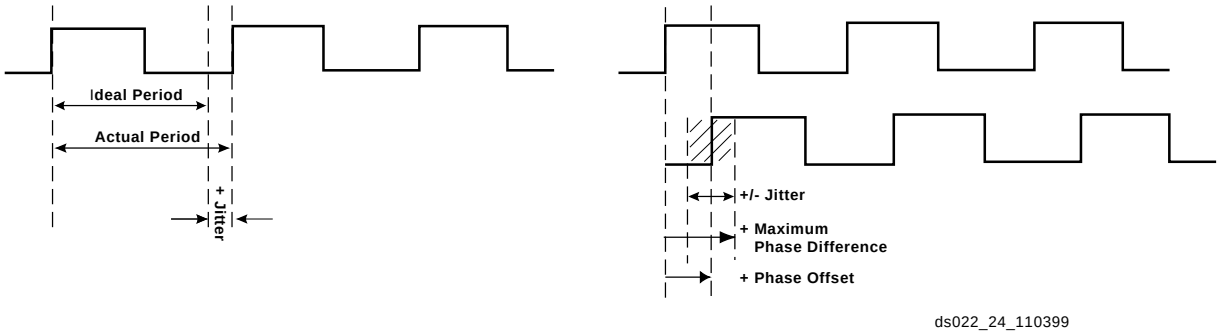


Figure 24: DLL Timing Waveforms

Design Considerations

This section contains more detailed design information on the following features.

Using Delay-Locked Loop

The Virtex-E FPGA series provides up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Virtex-E series of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device “waking up,” the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Symbols

Figure 25 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 26 and Figure 27 show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.

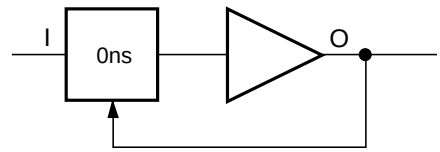


Figure 25: Simplified DLL Macro Symbol BUFGDLL

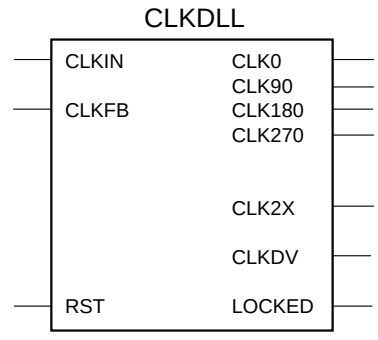
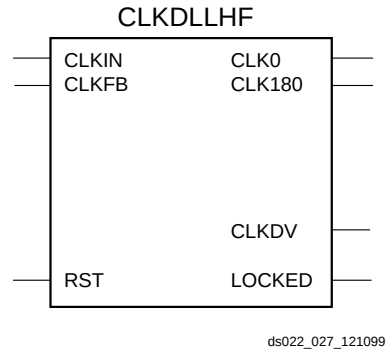


Figure 26: Standard DLL Symbol CLKDLL



igure 27: High Frequency DLL Symbol CLKDLLHF

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 28.

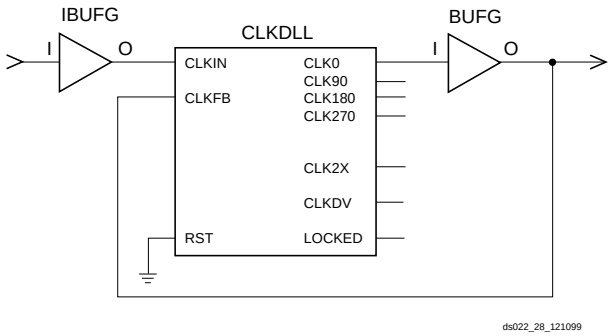


Figure 28: BUFGDLL Schematic

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL, one of the global clock input buffers (IBUFG), or an IO_LVDS_DLL pin on the same edge of the device (top or bottom) must source this clock signal. There are four IO_LVDS_DLL input pins that can be used as inputs to the DLLs. This makes a total of eight usable input pins for DLLs in the Virtex-E family.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pins.

IBUFG - Global Clock Input Pad
IO_LVDS_DLL - the pin adjacent to IBUF

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer de-skew with respect to one another. For these reasons, rarely use the reset pin unless re-configuring the device or changing the input frequency.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE

property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin always has a 50/50 duty cycle.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 17.

Table 17: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The timing diagrams in Figure 29 illustrate the DLL clock output characteristics.

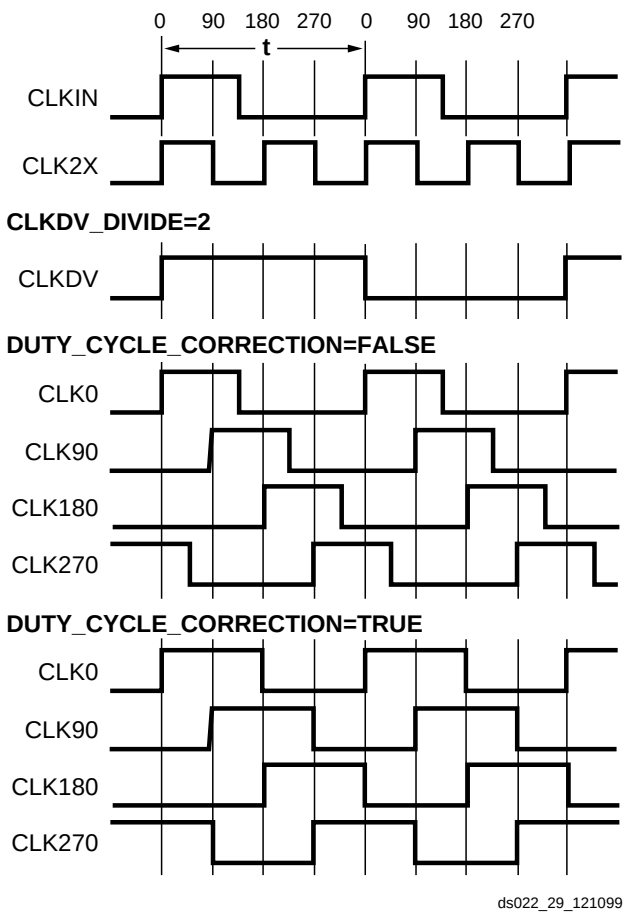


Figure 29: DLL Output Characteristics

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The DLL timing parameter section of the data sheet provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device “waking up,” the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Virtex-E series DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty-cycle correction deactivates, the output clock has the same duty cycle as the source clock.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

Virtex-E DLL Location Constraints

As shown in Figure 30, there are four additional DLLs in the Virtex-E devices, for a total of eight per Virtex-E device. These DLLs are located in silicon, at the top and bottom of the two innermost Block SelectRAM columns. The location constraint LOC, attached to the DLL symbol with the identifier DLL0S, DLL0P, DLL1S, DLL2S, DLL2P, DLL3S, or DLL3P, controls the DLL location.

The LOC property uses the following form:

LOC = DLL0P

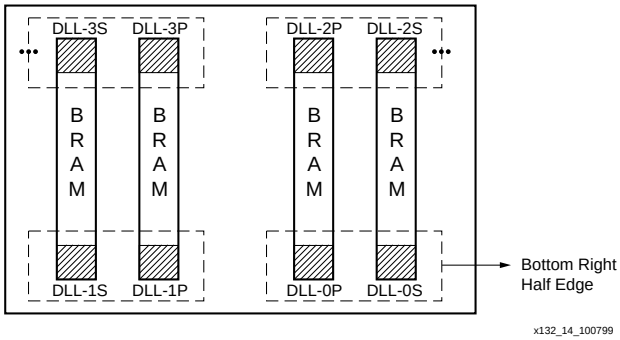


Figure 30: Virtex Series DLLs

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Virtex-E DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications. The Verilog and VHDL example files are available at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Standard Usage

The circuit shown in Figure 31 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

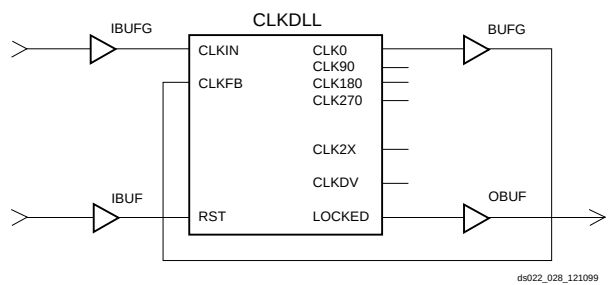


Figure 31: Standard DLL Implementation

Board Level De-skew of Multiple Non-Virtex-E Devices

The circuit shown in Figure 32 can be used to de-skew a system clock between a Virtex-E chip and other non-Virtex-E chips on the same board. This application is commonly used when the Virtex-E device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

Board-level de-skew is not required for low-fanout clock networks. It is recommended for systems that have fanout limitations on the clock network, or if the clock distribution chip cannot handle the load.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

The dll_mirror_1 files in the xapp132.zip file show the VHDL and Verilog implementation of this circuit.

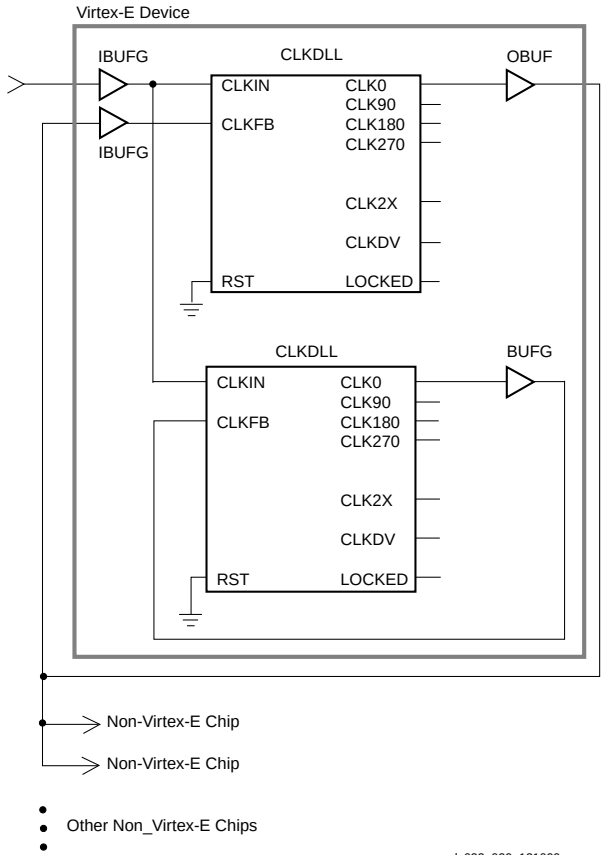


Figure 32: DLL De-skew of Board Level Clock

De-skew of Clock and Its 2x Multiple

The circuit shown in Figure 33 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.

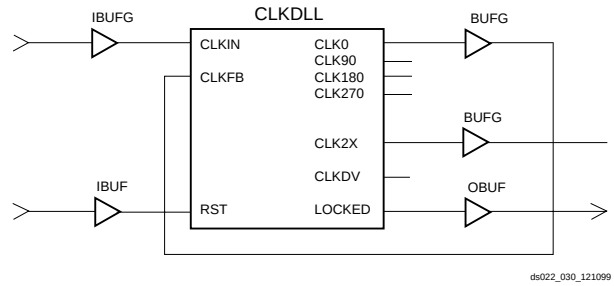


Figure 33: DLL De-skew of Clock and 2x Multiple

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

The dll_2x files in the xapp132.zip file show the VHDL and Verilog implementation of this circuit.

Virtex-E 4x Clock

Two DLLs located in the same half-edge (top-left, top-right, bottom-right, bottom-left) can be connected together, without using a BUFG between the CLKDLLs, to generate a 4x clock as shown in Figure 34. Virtex-E devices, like the Virtex devices, have four clock networks that are available for internal de-skewing of the clock. Each of the eight DLLs have access to two of the four clock networks. Although all the DLLs can be used for internal de-skewing, the presence of two GCLKBUFs on the top and two on the bottom indicate that only two of the four DLLs on the top (and two of the four DLLs on the bottom) can be used for this purpose.

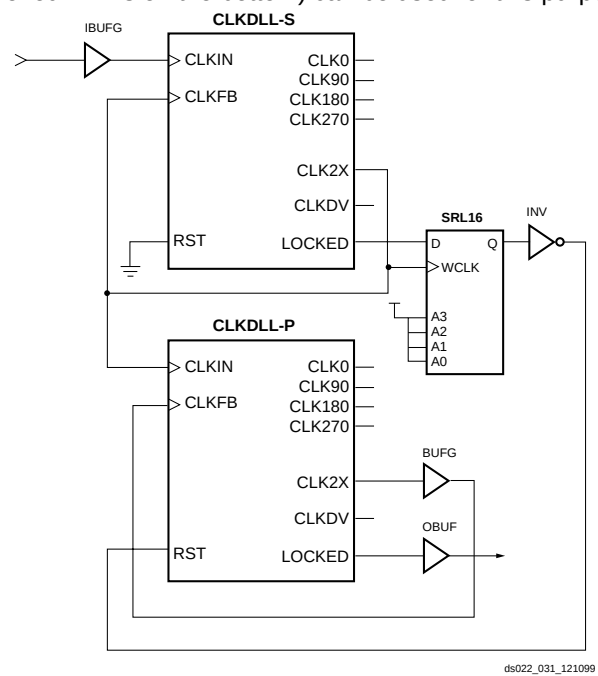


Figure 34: DLL Generation of 4x Clock in Virtex-E Devices

The dll_4xe files in the xapp 32.zip file show the DLL implementation in Verilog for Virtex-E devices. These files can be found at:

ftp://ftp.xilinx.com/pub/applications/xapp/xapp132.zip

Using Block SelectRAM+ Features

The Virtex FPGA Series provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the Block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The Block SelectRAM+ memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

VIrtex-E Block SelectRAM+ memory supports two operating modes.

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus set-up time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block SelectRAM+ Characteristics

1. All inputs are registered with the port clock and have a set-up to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The Block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 35 and Figure 36 show the two generic library Block SelectRAM+ primitives. Table 18 describes all of the available primitives for synthesis and simulation.

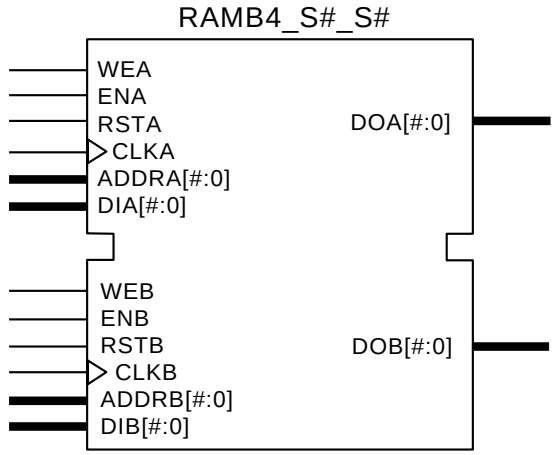


Figure 35: Dual-Port Block SelectRAM+ Memory

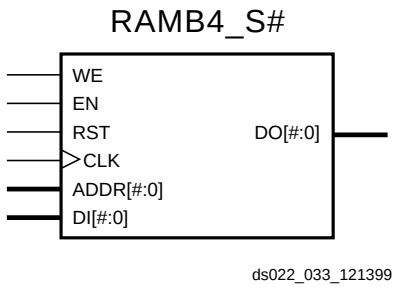


Figure 36: Single-Port Block SelectRAM+ Memory

Table 18: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16

Table 18: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each Block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 19 describes the depth and width aspect ratios for the Block SelectRAM+ memory.

Table 19: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 19.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 19.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 19.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$\text{Start} = ((\text{ADDR}_{port} + 1) * \text{Width}_{port}) - 1$$
$$\text{End} = \text{ADDR}_{port} * \text{Width}_{port}$$

Table 20 shows low order address mapping for each port width.

Table 20: Port Address Mapping

Port Width	Port Addresses															
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The Block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The Block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Conflict Resolution

The Block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 37 shows a timing diagram for a single port of a Block SelectRAM+ memory. The Block SelectRAM+ AC switching characteristics are specified in the data sheet. The Block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the Block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 38 shows a timing diagram for a true dual-port read/write Block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 37.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter

and the DOB reflects the new memory values written by Port A.

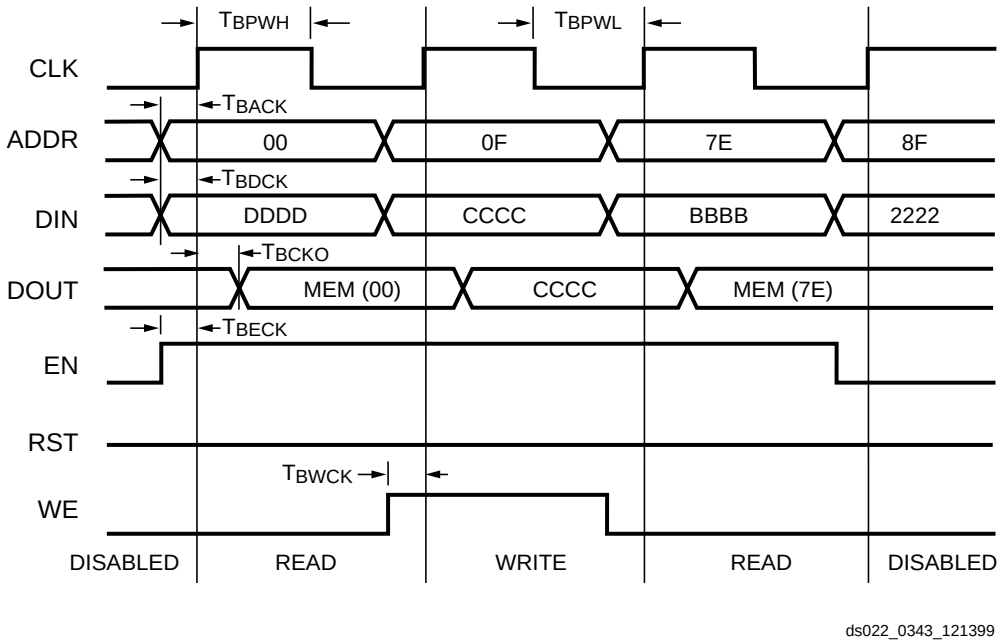


Figure 37: Timing Diagram for Single Port Block SelectRAM+ Memory

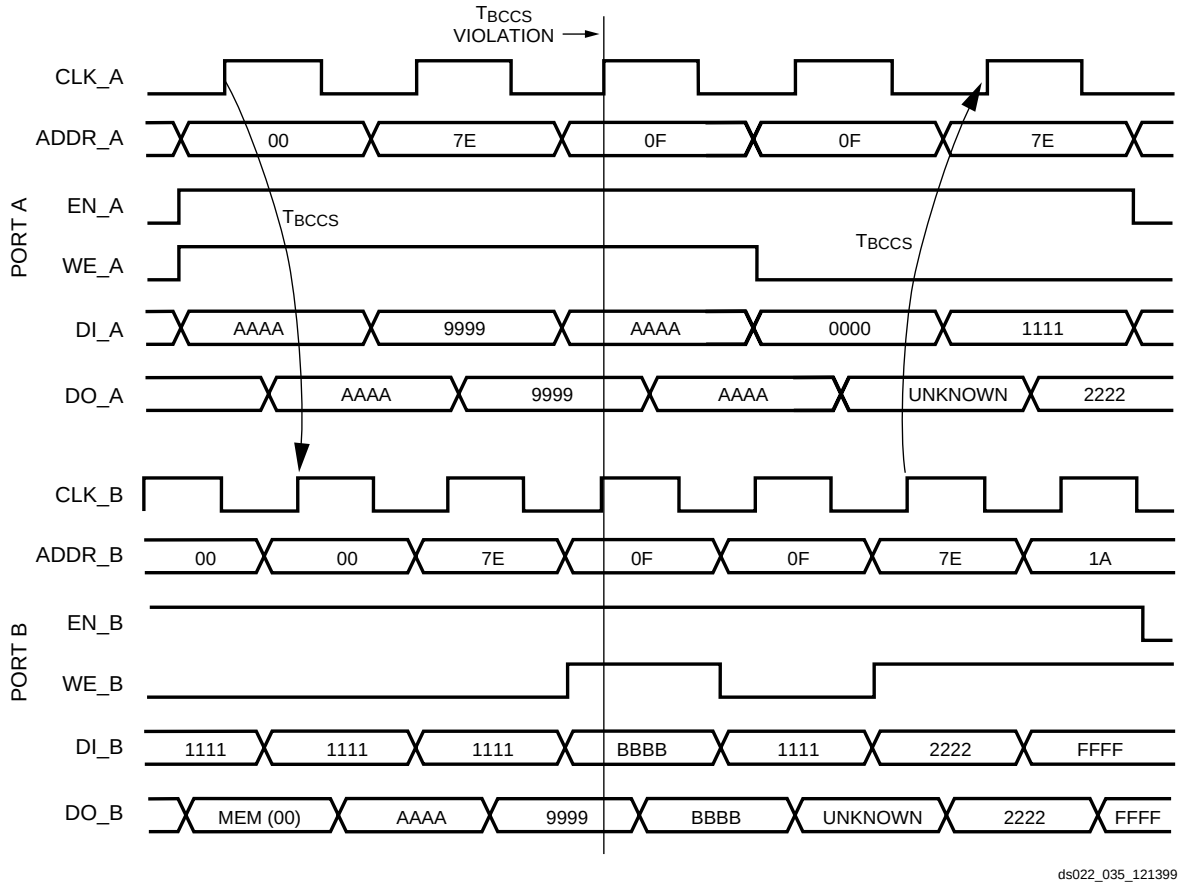


Figure 38: Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

Initialization

The Block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 21. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The Block SelectRAM+ structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 21: RAM Initialization Properties

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 2047
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

Initialization in Verilog and Synopsys

The Block SelectRAM+ structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the Block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single Block SelectRAM+ cell as shown inTable 39.

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

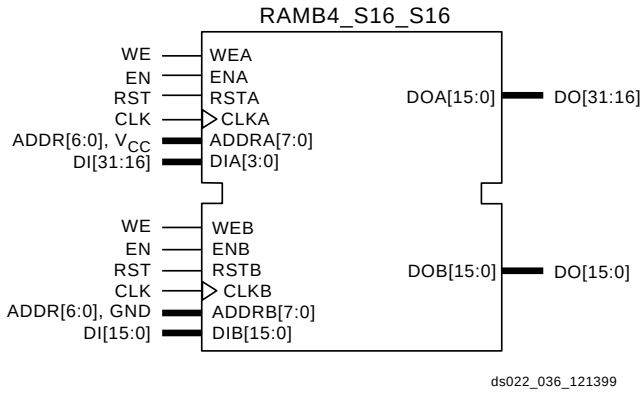


Figure 39: Single Port 128 x 32 RAM

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the Block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 40.

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single Block SelectRAM+. The address space for the RAM is split by fixing the

MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

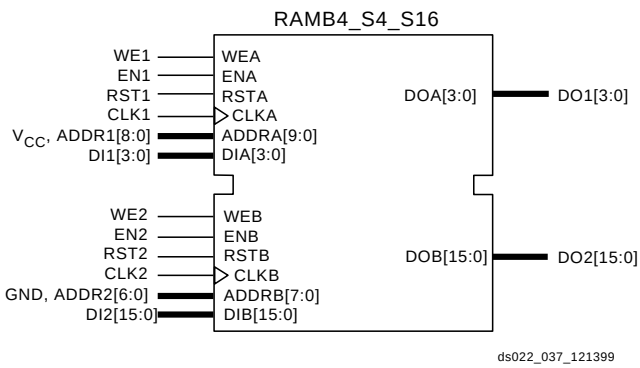


Figure 40: 512 x 4 RAM and 128 x 16 RAM

Block Memory Generation

The CoreGen program generates memory structures using the Block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

3

VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (
```

```
INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using Select I/O

The Virtex-E FPGA series includes a highly configurable, high-performance I/O resource, called SelectI/O™ to provide support for a wide variety of I/O standards. The SelectI/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and SelectI/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. SelectI/O, the revolutionary input/output resources of Virtex-E devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Virtex-E SelectI/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each SelectI/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

SelectI/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the

IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Virtex-E SelectI/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the SelectI/O features, system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The SelectI/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 22, each buffer type can support a variety of voltage requirements.

Table 22: Virtex-E Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
LVCMOS18	1.8	1.8	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A

Table 22: Virtex-E Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
BLVDS & LVDS	2.5	N/A	N/A	N/A
LVPECL	3.3	N/A	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Virtex-E devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance Jedec website at: http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5 Volts

The Low-Voltage CMOS for 2.5 Volts or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.-5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

LVCMOS18 — 1.8 V Low Voltage CMOS

This standard is an extension of the LVCMOS standard. It is used in general purpose 1.8 V applications. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required.

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}).

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. SelectI/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. SelectI/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

LVDS — Low Voltage Differential Signal

LVDS is a differential I/O standard. It requires that one data bit is carried through two signal lines. As with all differential signaling standards, LVDS has an inherent noise immunity over single-ended I/O standards. The voltage swing between two signal lines is approximately 350mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. LVDS requires the use of two pins per input or output. LVDS requires external resistor termination.

BLVDS — Bus LVDS

This standard allows for bidirectional LVDS communication between two or more devices. The external resistor termination is different than the one for standard LVDS.

LVPECL — Low Voltage Positive Emitter Coupled Logic

LVPECL is another differential I/O standard. It requires two signal lines for transmitting one data bit. This standard specifies two pins per input or output. The voltage swing between these two signal lines is approximately 850 mV. The use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}) is not required. The LVPECL standard requires external resistor termination.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of SelectI/O features. Most of these symbols represent variations of the five generic SelectI/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Virtex-E device must source an input buffer (IBUF) via an external input port. The generic Virtex-E IBUF symbol appears in Figure 41. The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

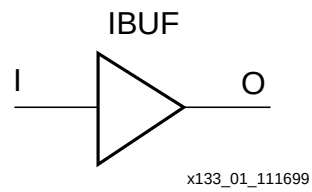


Figure 41: Input Buffer (IBUF) Symbols

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I

- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP
- IBUF_LVCMOS18
- IBUF_LVDS
- IBUF_LVPECL

When the IBUF symbol supports an I/O standard that requires a differential amplifier input, the IBUF automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 42 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 23 summarizes the Virtex-E input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

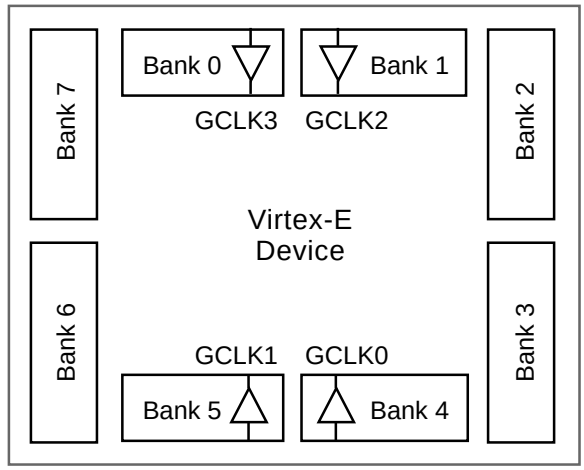


Figure 42: Virtex-E I/O Banks

Table 23: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Virtex-E device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic Virtex-E IBUFG symbol appears in Figure 43.

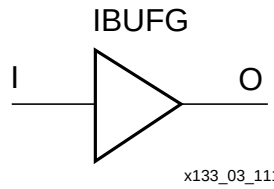


Figure 43: Virtex-E Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2

- IBUFG_PCI33_3
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP
- IBUFG_LVCMOS18
- IBUFG_LVDS
- IBUFG_LVPECL

When the IBUFG symbol supports an I/O standard that requires a differential amplifier input, the IBUFG automatically configures as a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 42 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

Unlike previous architectures, the Virtex-E BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 44.

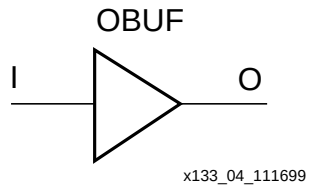


Figure 44: Virtex-E Output Buffer (OBUF) Symbol

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16
- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I

- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP
- OBUF_LVCMOS18
- OBUF_LVDS
- OBUF_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS packages support four V_{CCO} banks.

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 24 summarizes the Virtex-E output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 24: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 45, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

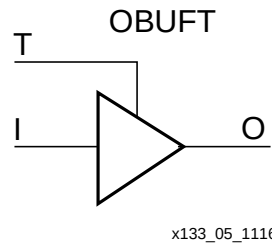


Figure 45: 3-State Output Buffer Symbol (OBUFT)

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP
- OBUFT_LVCMOS18
- OBUFT_LVDS
- OBUFT_LVPECL

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

The SelectI/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak “keeper” circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak “keeper” circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak “keeper” typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 46.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

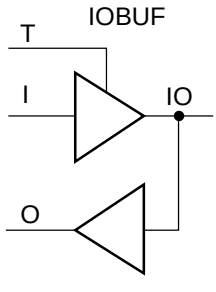


Figure 46: Input/Output Buffer Symbol (IOBUF)

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP
- IOBUF_LVCMOS18
- IOBUF_LVDS
- IOBUF_LVPECL

When the IOBUF symbol used supports an I/O standard that requires a differential amplifier input, the IOBUF automatically configures with a differential amplifier input buffer. The low-voltage I/O standards with a differential amplifier input require an external reference voltage input V_{REF}.

The voltage reference signal is “banked” within the Virtex-E device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 42 on page 55 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

IOBUF placement restrictions require any differential amplifier input signals within a bank be of the same standard.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Additional restrictions on the Virtex-E SelectI/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not

require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak “keeper” circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Select I/O Properties

Access to some of the SelectI/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The Virtex-E series IO Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each SelectI/O symbol with the location constraint LOC attached to the SelectI/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

LOC=A42

LOC=P37

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is “banked” within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 42 on page 55 for a representation of the Virtex-E I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input. After placing a differential amplifier input signal within a given V_{REF} bank, the same external source must drive all I/O pins configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by SelectI/O devices require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The Virtex-E series supports eight banks for the HQ and PQ packages. The CS package supports four V_{CCO} banks.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, LVCMOS18, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short distance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following.

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 47.

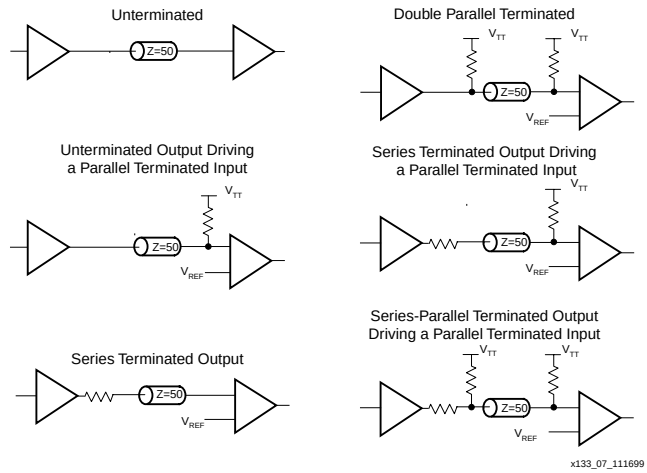


Figure 47: Overview of Standard Input and Output Termination Methods

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 25 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 26 for the number of effective output power/ground pairs for each Virtex-E device and package combination.

Table 25: Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair

	Package		
Standard	**BGA, CS, FGA**	**HQ**	**PQ, TQ**
LVTTL Slow Slew Rate, 2 mA drive	68	49	36
LVTTL Slow Slew Rate, 4 mA drive	41	31	20
LVTTL Slow Slew Rate, 6 mA drive	29	22	15

Table 25: Guidelines for Maximum Number of Simultaneously Switching Outputs per Power/Ground Pair

	Package		
Standard	**BGA, CS, FGA**	**HQ**	**PQ, TQ**
LVTTL Slow Slew Rate, 8 mA drive	22	17	12
LVTTL Slow Slew Rate, 12 mA drive	17	12	9
LVTTL Slow Slew Rate, 16 mA drive	14	10	7
LVTTL Slow Slew Rate, 24 mA drive	9	7	5
LVTTL Fast Slew Rate, 2 mA drive	40	29	21
LVTTL Fast Slew Rate, 4 mA drive	24	18	12
LVTTL Fast Slew Rate, 6 mA drive	17	13	9
LVTTL Fast Slew Rate, 8 mA drive	13	10	7
LVTTL Fast Slew Rate, 12 mA drive	10	7	5
LVTTL Fast Slew Rate, 16 mA drive	8	6	4
LVTTL Fast Slew Rate, 24 mA drive	5	4	3
LVCMOS2	10	7	5
PCI	8	6	4
GTL	4	4	4
GTL+	4	4	4
HSTL Class I	18	13	9
HSTL Class III	9	7	5
HSTL Class IV	5	4	3
SSTL2 Class I	15	11	8
SSTL2 Class II	10	7	5
SSTL3 Class I	11	8	6
SSTL3 Class II	7	5	4
CTT	14	10	7
AGP	9	7	5

Note: This analysis assumes a 35 pF load for each output.

Table 26: Virtex-E Equivalent Power/Ground Pairs

Pkg/Part	v100e	v200e	v300e	v400e	v600e	v1000e	v1600e	v2000e
CS144	12	12						
PQ240	20	20	20	20				
HQ240					20	20		
BG432			32	40	40			
BG560						56	58	60
FG256(1)	20	24	24					
FG456		40	40					
FG676				54	56			
FG680(2)					46	56	56	56
FG860						58	60	64
FG900								
FG1156						96	104	120

Notes:
1: Virtex-E devices in FG256 packages have more V_{CCO} than Virtex series devices.
2: FG680 numbers are preliminary.

Application Examples

Creating a design with the SelectI/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the SelectI/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the SelectI/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 48. Table 27 lists DC voltage specifications.

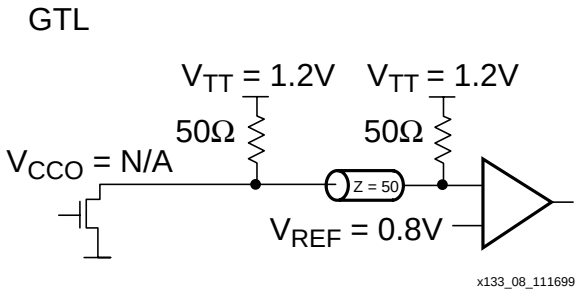


Figure 48: Terminated GTL

Table 27: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$ [1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} – 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL}at V_{OL}(mA) at 0.4V	32	-	-
I_{OL}at V_{OL}(mA) at 0.2V	-	-	40

Note 1: N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 49. DC voltage specifications appear in Table 28.

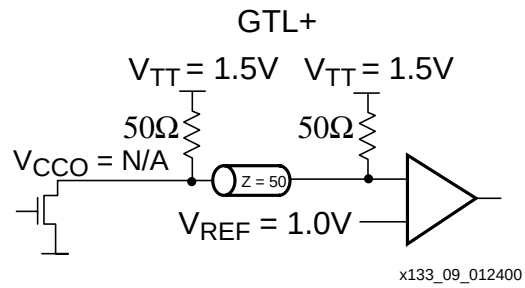


Figure 49: Terminated GTL+

Table 28: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$ [1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} – 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL}at V_{OL} (mA) at 0.6V	36	-	-
I_{OL}at V_{OL} (mA) at 0.3V	-	-	48

Note 1: N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 50. A sample circuit illustrating a

valid termination technique for HSTL_III appears in Figure 51.

HSTL Class I

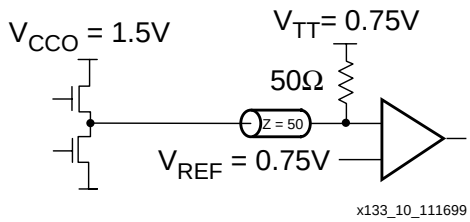


Figure 50: Terminated HSTL Class I

Table 29: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

HSTL Class III

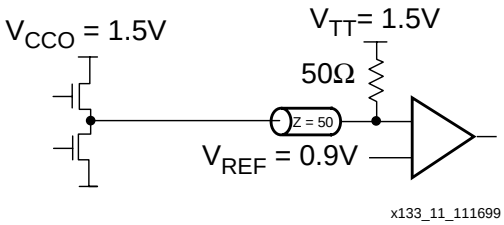


Figure 51: Terminated HSTL Class III

Table 30: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 52.

HSTL Class IV

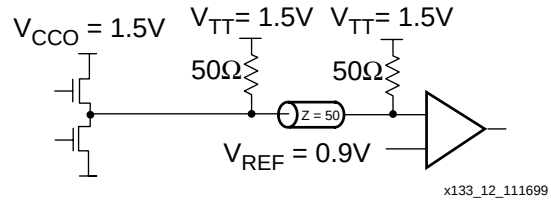


Figure 52: Terminated HSTL Class IV

Table 31: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	V_{REF} – 0.1
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 53. DC voltage specifications appear in Table 32.

SSTL3 Class I

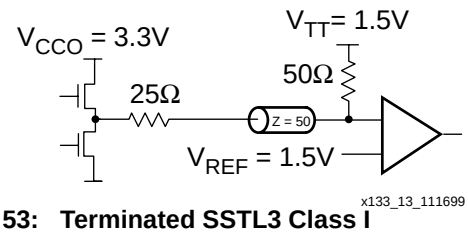


Figure 53: Terminated SSTL3 Class I

Table 32: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} – 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes
1: V_{IH} maximum is V_{CCO} + 0.3
2: V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 54. DC voltage specifications appear in Table 33.

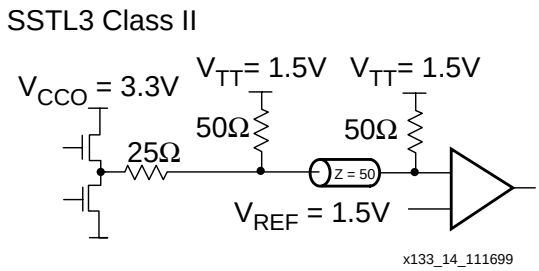


Figure 54: Terminated SSTL3 Class II

Table 33: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL} = V_{REF} – 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes
1: V_{IH} maximum is V_{CCO} + 0.3
2: V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 55. DC voltage specifications appear in Table 34.

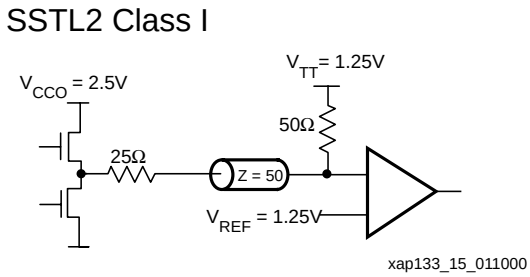


Figure 55: Terminated SSTL2 Class I

Table 34: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL} = V_{REF} – 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes
1: N must be greater than or equal to -0.04 and less than or equal to 0.04.
2: V_{IH} maximum is V_{CCO} + 0.3.
3: V_{IL} minimum does not conform to the formula.

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 56. DC voltage specifications appear in Table 35.

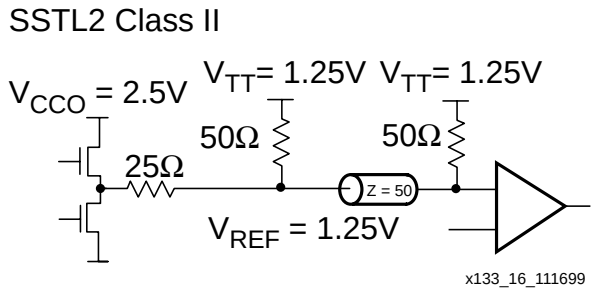


Figure 56: Terminated SSTL2 Class II

Table 35: SSTL2_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF}$ - 0.8	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL}at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2.V_{IH} maximum is V_{CCO} + 0.3.
3.V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 57. DC voltage specifications appear in Table 36.

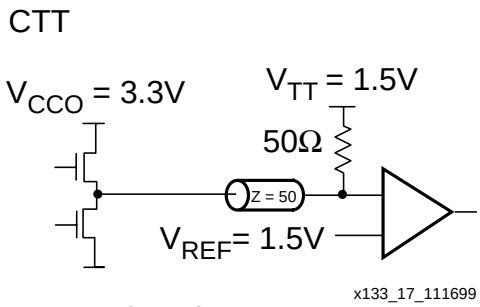


Figure 57: Terminated CTT

Table 36: CTT Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} – 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL} = V_{REF} – 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

Notes:
1: Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 & PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 37.

Table 37: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO}+ 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL} = 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL} at V_{OL} (mA)	Note 1	-	-

Note 1: Tested according to the relevant specification.

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 38.

Table 38: LVTTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	3.6
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL} at V_{OL} (mA)	24	-	-

Note: V_{OL} and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 39.

Table 39: LVCMOS2 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	3.6
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL} at V_{OL} (mA)	12	-	-

LVCMOS18

LVCMOS18 does not require termination. Table 40 lists DC voltage specifications.

Table 40: LVCMOS18 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	1.70	1.80	1.90
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	0.7 x V_{CCO}	-	1.95
V_{IL}	– 0.5	-	0.2 x V_{CCO}
V_{OH}	V_{CCO} – 0.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL} at V_{OL} (mA)	8	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 41.

Table 41: AGP-2X Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$ (1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} – 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL}at V_{OL} (mA)	Note 2	-	-

Notes:
1: N must be greater than or equal to 0.39 and less than or equal to 0.41.
2: Tested according to the relevant specification.

LVDS

Depending on whether the device is transmitting an LVDS signal or receiving an LVDS signal, there are two different circuits used for LVDS termination. A sample circuit illustrating a valid termination technique for transmitting LVDS signals appears in Figure 58. A sample circuit illustrating a valid termination for receiving LVDS signals appears in Figure 59. Table 42 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 44.

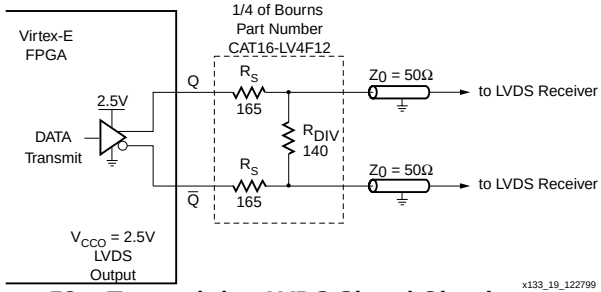


Figure 58: Transmitting LVDS Signal Circuit

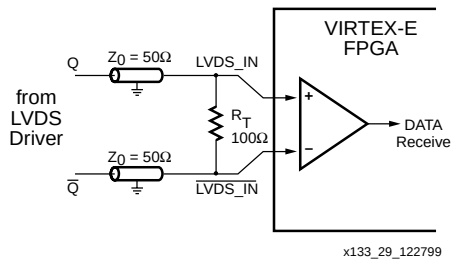


Figure 59: Receiving LVDS Signal Circuit

Table 42: LVDS Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.375	2.5	2.625
V_{ICM} (2)	0.2	1.25	2.2
V_{OCM} (1)	1.125	1.25	1.375
V_{IDIFF} (1)	0.1	0.35	-
V_{ODIFF} (1)	0.25	0.35	0.45
V_{OH} (1)	1.25	-	-
V_{OL} (1)	-	-	1.25

Notes:
1: Measured with a 100 Ω resistor across Q and $\overline{Q}$.
2: Measured with a differential input voltage = +/– 350 mV.

LVPECL

Depending on whether the device is transmitting or receiving an LVPECL signal, two different circuits are used for LVPECL termination. A sample circuit illustrating a valid termination technique for transmitting LVPECL signals appears in Figure 60. A sample circuit illustrating a valid termination for receiving LVPECL signals appears in Figure 61. Table 43 lists DC voltage specifications. Further information on the specific termination resistor packs shown can be found on Table 44.

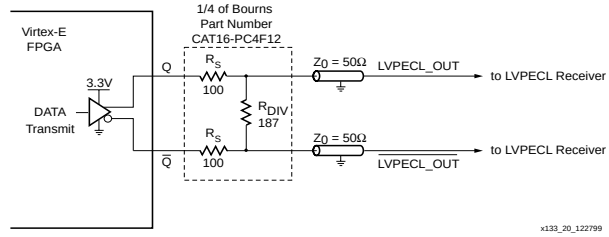


Figure 60: Transmitting LVPECL Signal Circuit

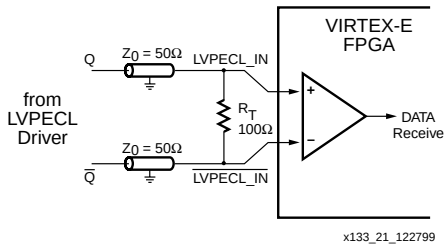


Figure 61: Receiving LVPECL Signal Circuit

Table 43: LVPECL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.49	-	2.72
V_{IL}	0.86	-	2.125
V_{OH}	1.8	-	-
V_{OL}	-	-	1.57

Note: For more detailed information, see page 25

Termination Resistor Packs

Resistor packs are available with the values and the configuration required for LVDS and LVPECL termination from Bourns, Inc., as listed in Table. For pricing and availability, please contact Bourns directly at www.bourns.com.

Table 44: Bourns LVDS/LVPECL Resistor Packs

Part Number	I/O Standard	Term. for:	Pairs/ Pack	Pins
CAT16–LV2F6	LVDS	Driver	2	8
CAT16–LV4F12	LVDS	Driver	4	16
CAT16–PC2F6	LVPECL	Driver	2	8
CAT16–PC4F12	LVPECL	Driver	4	16
CAT16–PT2F2	LVDS/LVPECL	Receiver	2	8
CAT16–PT4F4	LVDS/LVPECL	Receiver	4	16

LVDS Design Guide

The SelectI/O library elements have been expanded for Virtex-E devices to include new LVDS variants. At this time all of the cells may not be included in the Synthesis libraries. The 2.1i-Service Pack 2 update for Alliance and Foundation software includes these cells in the VHDL and Verilog libraries. It is necessary to combine these cells to create the P-side (positive) and N-side (negative) as described in the input, output, 3-state and bidirectional sections.

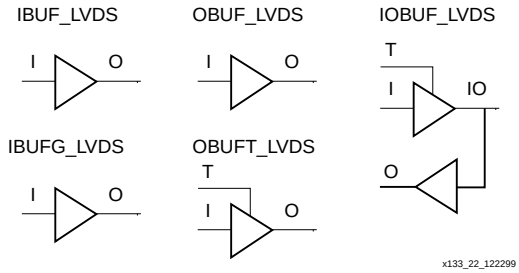


Figure 62: LVDS elements

Creating an LVDS Global Clock Input Buffer

The global clock input buffer may be combined with the adjacent IOB to form an LVDS clock input buffer. The P-side resides in the GCLKPAD location and the N-side resides in the adjacent IO_LVDS_DLL site.

Table 45: Global Clock Input Buffer Locations

Package	GCLK PAD3	GCLK PAD2	GCLK PAD1	GCLK PAD0
CS144	C6	B7	M6	N8
PQ240	P215	P209	P87	P93
BG432	C17	B16	AL17	AH15
BG560	C18	E17	AM18	AM17
FG256	A7	A8	T8	N9
FG456	B11	D11	AA11	U12
FG676	B13	F14	AF13	AC14
FG680	C22	A19	AT22	AT21
FG860	A22	D22	AW21	AW20
FG900	A15	E16	AH16	AF16
FG1156	C17	J18	AL17	AM18

HDL Instantiation

Only one global clock input buffer is required to be instantiated in the design and placed on the correct GCLKPAD location. The N-side of the buffer will be reserved and no other IOB will be allowed to be placed on this location.

In the physical device a configuration option is enabled that routes the pad wire to the differential input buffer located in the GCLKIOB. The output of this buffer then drives the output of the GCLKIOB cell. In EPIC it will appear that the second buffer is unused. Any attempt to use this location for another purpose will cause a DRC error from the software.

VHDL Instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_external, O=>clk_internal);
```

Verilog instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_external),
.O(clk_internal));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET clk_external LOC = GCLKPAD3;
```

GCLKPAD3 may also be replaced with the package pin name such as D17 for the BG432 package.

Optional N-side

Some designers may prefer to also instantiate the N-side buffer for the global clock buffer. This will allow the top-level net list to include both net connections for PCB layout and system level integration. In this case the output P-side IBUFG connection is the only one to have a net connected to it. Since the N-side IBUFG does not have a connection in the EDIF net list it will be trimmed from the design in MAP.

VHDL instantiation

```
gclk0_p : IBUFG_LVDS port map
(I=>clk_p_external, O=>clk_internal);

gclk0_n : IBUFG_LVDS port map
(I=>clk_n_external, O=>clk_internal);
```

Verilog instantiation

```
IBUFG_LVDS gclk0_p (.I(clk_p_external),
.O(clk_internal));

IBUFG_LVDS gclk0_n (.I(clk_n_external),
.O(clk_internal));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET clk_p_external LOC = GCLKPAD3;

NET clk_n_external LOC = C17;
```

GCLKPAD3 may also be replaced with the package pin name such as D17 for the BG432 package.

Creating an LVDS Input Buffer

An LVDS input buffer may be placed in a wide number of IOB locations. The exact location is dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Only one input buffer is required to be instantiated in the design and placed on the correct IO_L#P location. The N-side of the buffer will be reserved and no other IOB will be allowed to be placed on this location. In the physical device, a configuration option is enabled that routes the pad wire from the IO_L#N IOB to the differential input buffer located in the IO_L#P IOB. The output of this buffer then drives the output of the IO_L#P cell or the input register in the IO_L#P IOB. In EPIC it will appear that the second buffer is unused. Any attempt to use this location for another purpose will cause a DRC error from the software.

VHDL instantiation

```
data0_p : IBUF_LVDS port map
(I=>data(0), O=>data_int(0));
```

Verilog instantiation

```
IBUF_LVDS data0_p (.I(data[0]),
.O(data_int[0]));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data<0> LOC = D28; # IO_L0P
```

Optional N-side

Some designers may prefer to also instantiate the N-side buffer for the input buffer. This will allow the top-level net list to include both net connections for PCB layout and system level integration. In this case the output P-side IBUF connection is the only one to have a net connected to it. Since the N-side IBUF does not have a connection in the EDIF net list it will be trimmed from the design in MAP.

VHDL instantiation

```
data0_p : IBUF_LVDS port map
(I=>data_p(0), O=>data_int(0));

data0_n : IBUF_LVDS port map
(I=>data_n(0), O=>open);
```

Verilog instantiation

```
IBUF_LVDS data0_p (.I(data_p[0]),
.O(data_int[0]));

IBUF_LVDS data0_n (.I(data_n[0]),
.O());
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the global clock input buffers this may be done with the following constraint in the .ucf or .ncf file.

```
NET data_p<0> LOC = D28; # IO_L0P

NET data_n<0> LOC = B29; # IO_L0N
```

Adding an Input Register

All LVDS buffers may have an input register in the IOB. The input register will be in the P-side IOB only. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries available to explicitly create these structures. The input library macros are listed in Table 46. The I and IB inputs to the macros are the external net connections.

Table 46: Input Library Macros

Name	Inputs	Outputs
IBUFDS_FD_LVDS	I, IB, C	Q
IBUFDS_FDE_LVDS	I, IB, CE, C	Q
IBUFDS_FDC_LVDS	I, IB, C, CLR	Q
IBUFDS_FDCE_LVDS	I, IB, CE, C, CLR	Q
IBUFDS_FDP_LVDS	I, IB, C, PRE	Q
IBUFDS_FDPE_LVDS	I, IB, CE, C, PRE	Q
IBUFDS_FDR_LVDS	I, IB, C, R	Q
IBUFDS_FDRE_LVDS	I, IB, CE, C, R	Q
IBUFDS_FDS_LVDS	I, IB, C, S	Q
IBUFDS_FDSE_LVDS	I, IB, CE, C, S	Q

Table 46: Input Library Macros

Name	Inputs	Outputs
IBUFDS_LD_LVDS	I, IB, G	Q
IBUFDS_LDE_LVDS	I, IB, GE, G	Q
IBUFDS_LDC_LVDS	I, IB, G, CLR	Q
IBUFDS_LDCE_LVDS	I, IB, GE, G, CLR	Q
IBUFDS_LDP_LVDS	I, IB, G, PRE	Q
IBUFDS_LDPE_LVDS	I, IB, GE, G, PRE	Q

Creating a LVDS Output Buffer

LVDS output buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Both output buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one HIGH and one LOW). Failure to follow these rules will lead to DRC errors in software.

VHDL instantiation

```
    data0_p  : OBUF_LVDS port map
(I=>data_int(0),   O=>data_p(0));

    data0_inv: INV       port map
(I=>data_int(0),   O=>data_n_int(0));

    data0_n  : OBUF_LVDS port map
(I=>data_n_int(0), O=>data_n(0));
```

Verilog instantiation

```
    OBUF_LVDS data0_p   (.I(data_int[0]),
.O(data_p[0]));

    INV       data0_inv (.I(data_int[0],
.O(data_n_int[0]);

    OBUF_LVDS data0_n   (.I(data_n_int[0]),
.O(data_n[0]));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
    NET data_p<0> LOC = D28; # IO_L0P

    NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the output are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device.

The LVDS pairs that may be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

Adding an Output Register

All LVDS buffers may have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The clock pin (C), clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The output library macros are listed in Table 47. The O and OB inputs to the macros are the external net connections.

Table 47: Output Library Macros

Name	Inputs	Outputs
OBUFDS_FD_LVDS	D, C	O, OB
OBUFDS_FDE_LVDS	DD, CE, C	O, OB
OBUFDS_FDC_LVDS	D, C, CLR	O, OB
OBUFDS_FDCE_LVDS	D, CE, C, CLR	O, OB
OBUFDS_FDP_LVDS	D, C, PRE	O, OB
OBUFDS_FDPE_LVDS	D, CE, C, PRE	O, OB
OBUFDS_FDR_LVDS	D, C, R	O, OB
OBUFDS_FDRE_LVDS	D, CE, C, R	O, OB
OBUFDS_FDS_LVDS	D, C, S	O, OB
OBUFDS_FDSE_LVDS	D, CE, C, S	O, OB
OBUFDS_LD_LVDS	D, G	O, OB
OBUFDS_LDE_LVDS	D, GE, G	O, OB
OBUFDS_LDC_LVDS	D, G, CLR	O, OB
OBUFDS_LDCE_LVDS	D, GE, G, CLR	O, OB
OBUFDS_LDP_LVDS	D, G, PRE	O, OB
OBUFDS_LDPE_LVDS	D, GE, G, PRE	O, OB

Creating an LVDS Output 3-State Buffer

LVDS output 3-state buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Both output 3-state buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one High and one Low). If 3-state registers are used the must be initialized to the same state. Failure to follow these rules will lead to DRC errors in the software.

VHDL instantiation

```
    data0_p:   OBUFT_LVDS port map
(I=>data_int(0), T=>data_tri,
O=>data_p(0));

    data0_inv: INV port map
(I=>data_int(0), O=>data_n_int(0));

    data0_n:    OBUFT_LVDS port map
(I=>data_n_int(0), T=>data_tri,
O=>data_n(0));
```

Verilog instantiation

```
    OBUFT_LVDS data0_p  (.I(data_int[0]),
.T(data_tri), .O(data_p[0]));

    INV       data0_inv (.I(data_int[0],
.O(data_n_int[0]);

    OBUFT_LVDS data0_n  (.I(data_n_int[0]),
.T(data_tri), .O(data_n[0]));
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
    NET data_p<0> LOC = D28; # IO_L0P

    NET data_n<0> LOC = B29; # IO_L0N
```

Synchronous vs. Asynchronous 3-State Outputs

If the outputs are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the outputs are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that may be used as asynchronous outputs are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

Adding Output and 3-state Registers

All LVDS buffers may have an output register in the IOB. The output registers must be in both the P-side and N-side IOBs. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code.

Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs.

To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The input library macros are listed below. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output register. If this is not desirable then the library may be updated be the user for the desired functionality. The O and OB inputs to the macros are the external net connections.

Creating a LVDS Bidirectional Buffer

LVDS bidirectional buffer may be placed in wide number of IOB locations. The exact location are dependent on the package that is used. The Virtex-E package information lists the possible locations as IO_L#P for the P-side and IO_L#N for the N-side where # is the pair number.

HDL Instantiation

Both bidirectional buffer are required to be instantiated in the design and placed on the correct IO_L#P and IO_L#N locations. The IOB must have the same net source the following pins, clock (C), set/reset (SR), 3-state (T), 3-state clock enable (TCE), output (O), output clock enable (OCE). In addition, the output (O) pins must be inverted with respect to each other and if output registers are used the INIT states must be opposite values (one HIGH and one LOW). If 3-state registers are used the must be initialized to

the same state. Failure to follow these rules will lead to DRC errors in the software.

VHDL instantiation

```
    data0_p:   IOBUF_LVDS port map
(I=>data_out(0), T=>data_tri,
IO=>data_p(0), O=>data_int(0));

    data0_inv: INV        port map
(I=>data_out(0),   O=>data_n_out(0));

    data0_n  : IOBUF_LVDS port map
(I=>data_n_out(0), T=>data_tri,
IO=>data_n(0), O=>open);
```

Verilog instantiation

```
    IOBUF_LVDS data0_p(.I(data_out[0]),
.T(data_tri), .IO(data_p[0]),
.O(data_int[0]);

    INV       data0_inv (.I(data_out[0],
.O(data_n_out[0]);

    IOBUF_LVDS
data0_n(.I(data_n_out[0]),.T(data_tri),.IO(
data_n[0]).O());
```

Location constraints

All LVDS buffers must be explicitly placed on a device. For the output buffers this may be done with the following constraint in the .ucf or .ncf file.

```
   NET data_p<0> LOC = D28; #
IO_L0P

   NET data_n<0> LOC = B29; #
IO_L0N
```

Synchronous vs. Asynchronous Bidirectional Buffers

If the output side of the bidirectional buffers are synchronous (registered in the IOB) then any IO_L#P|N pair may be used. If the output side of the bidirectional buffers are asynchronous (no output register) then they must use one of pairs that part of the same IOB group at the end of a ROW or COLUMN in the device. This applies for either the 3-state pin or the data out pin.

The LVDS pairs that may be used as asynchronous bidirectional buffers are listed in the Virtex-E pinout tables. Some pairs are marked as asynchronous capable for all devices in that package and others are marked as only available for that device in the package. If the device size may be changed at some point in the product lifetime then only the common pairs for all packages should be used.

Adding Output and 3-state Registers

All LVDS buffers may have an output and input registers in the IOB. The output registers must be in both the P-side and N-side IOBs, the input register is only in the P-side. All the normal IOB register options are available (FD, FDE, FDC, FDCE, FDP, FDPE, FDR, FDRE, FDS, FDSE, LD, LDE, LDC, LDCE, LDP, LDPE). The register elements may be inferred or explicitly instantiated in the HDL code. Special care must be taken to insure that the D pins of the registers are inverted and that the INIT states of the registers are opposite. The 3-state (T), 3-state clock enable (CE), clock pin (C), output clock enable (CE) and set/reset (CLR/PRE or
S/R) pins must connect to the same source. Failure to do this will lead to a DRC error in the software.

The register elements may be packed in the IOB using the IOB property to TRUE on the register or by using the “map -pr [i|o|b]” where “i” is inputs only, “o” is outputs only and “b” is both inputs and outputs. To improve design coding times VHDL and Verilog synthesis macro libraries have been developed to explicitly create these structures. The bidirectional I/O library macros are listed in Table 48. The 3-state is configured to be 3-stated at GSR and when the PRE,CLR,S or R is asserted and shares it's clock enable with the output and input register. If this is not desirable then the library may be updated be the user for the desired functionality. The IO and IOB inputs to the macros are the external net connections.

Table 48: Bidirectional I/O Library Macros

Name	Inputs	Bidirectional	Outputs
IOBUFDS_FD_LVDS	D, T, C	IO, IOB	Q
IOBUFDS_FDE_LVDS	D, T, CE, C	IO, IOB	Q
IOBUFDS_FDC_LVDS	D, T, C, CLR	IO, IOB	Q
IOBUFDS_FDCE_LVDS	D, T, CE, C, CLR	IO, IOB	Q
IOBUFDS_FDP_LVDS	D, T, C, PRE	IO, IOB	Q
IOBUFDS_FDPE_LVDS	D, T, CE, C, PRE	IO, IOB	Q
IOBUFDS_FDR_LVDS	D, T, C, R	IO, IOB	Q
IOBUFDS_FDRE_LVDS	D, T, CE, C, R	IO, IOB	Q
IOBUFDS_FDS_LVDS	D, T, C, S	IO, IOB	Q
IOBUFDS_FDSE_LVDS	D, T, CE, C, S	IO, IOB	Q

Table 48: Bidirectional I/O Library Macros

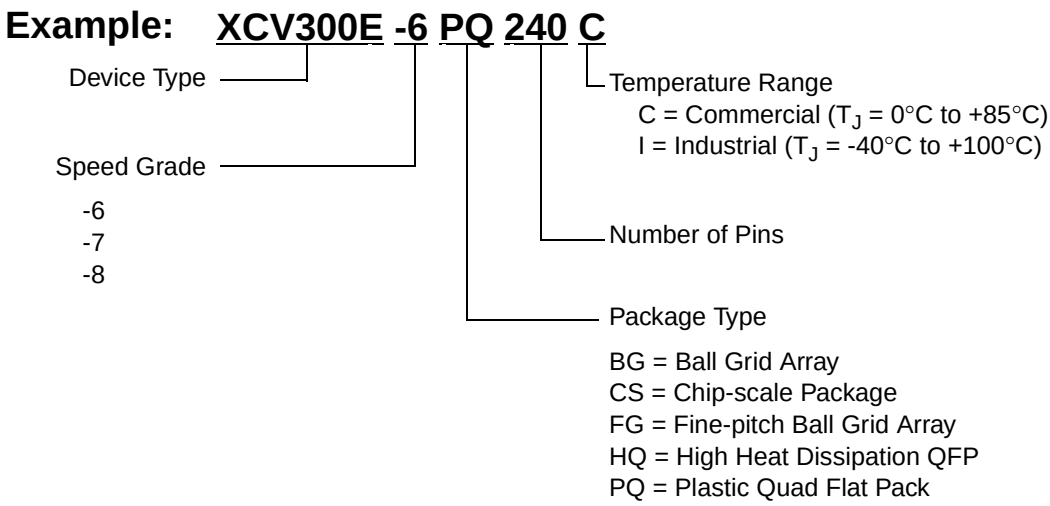
Name	Inputs	Bidirectional	Outputs
IOBUFDS_LD_LVDS	D, T, G	IO, IOB	Q
IOBUFDS_LDE_LVDS	D, T, GE, G	IO, IOB	Q
IOBUFDS_LDC_LVDS	D, T, G, CLR	IO, IOB	Q
IOBUFDS_LDCE_LVDS	D, T, GE, G, CLR	IO, IOB	Q
IOBUFDS_LDP_LVDS	D, T, G, PRE	IO, IOB	Q
IOBUFDS_LDPE_LVDS	D, T, GE, G, PRE	IO, IOB	Q

Virtex-E Pin Definitions

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode
PROGRAM	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
INIT	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides preamble and configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
WRITE	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
CS	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

For a complete Virtex-E data sheet including package pinouts, go to the CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Virtex-E Ordering Information



Revision History

Version	Description
1.0 (12/7/1999)	Initial Release of comprehensive data sheet with electrical specifications and packaging information.
1.1 (1/10/2000)	Re-rleased with spd.txt v. 1.18, FG860/900/1156 package information, and additional DLL, Select RAM and Select I/Oinformation.
1.2 (1/20/2000)	Updated Figures 54 & 55, text explaining Table 5, corrected Table 44 and buffered Hex Line info, p. 8.
1.3 (2/28/2000)	Updated Figure 20, Absolute Max Ratings: Vcc = 50 ms.

Virtex 2.5V Field Programmable Gate Arrays

DS003 (v1.9) January 28, 2000

Preliminary Product Specification

Features

- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 50k to 1M system gates
  - System performance up to 200 MHz
  - 66 MHz PCI Compliant
  - Hot-swappable for Compact PCI
- Multi-standard SelectIO™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary local clock nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensor diode
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited re-programmability
  - Four programming modes
- 0.22 µm 5-layer metal process
- 100% factory tested

Description

The Virtex™ FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22-µm CMOS process. These advances make Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the nine members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Table 1: Virtex Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Maximum SelectRAM+™ Bits
XCV50	57,906	16x24	1,728	180	32,768	24,576
XCV100	108,904	20x30	2,700	180	40,960	38,400
XCV150	164,674	24x36	3,888	260	49,152	55,296
XCV200	236,666	28x42	5,292	284	57,344	75,264
XCV300	322,970	32x48	6,912	316	65,536	98,304
XCV400	468,252	40x60	10,800	404	81,920	153,600
XCV600	661,111	48x72	15,552	512	98,304	221,184
XCV800	888,439	56x84	21,168	512	114,688	301,056
XCV1000	1,124,022	64x96	27,648	512	131,072	393,216

Virtex Architecture

Virtex devices feature a flexible, regular architecture that comprises an array of configurable logic blocks (CLBs) surrounded by programmable input/output blocks (IOBs), all interconnected by a rich hierarchy of fast, versatile routing resources. The abundance of routing resources permits the Virtex family to accommodate even the largest and most complex designs.

Virtex FPGAs are SRAM-based, and are customized by loading configuration data into internal memory cells. In some modes, the FPGA reads its own configuration data from an external PROM (master serial mode). Otherwise, the configuration data is written into the FPGA (SelectMAP™, slave serial, and JTAG modes).

The standard Xilinx Foundation™ and Alliance Series™ Development systems deliver complete design support for Virtex, covering every aspect from behavioral and schematic entry, through simulation, automatic design translation and implementation, to the creation, downloading, and readback of a configuration bit stream.

Higher Performance

Virtex devices provide better performance than previous generations of FPGA. Designs can achieve synchronous system clock rates up to 200 MHz including I/O. Virtex inputs and outputs comply fully with PCI specifications, and interfaces can be implemented that operate at 33 MHz or 66 MHz. Additionally, Virtex supports the hot-swapping requirements of Compact PCI.

Xilinx thoroughly benchmarked the Virtex family. While performance is design-dependent, many designs operated internally at speeds in excess of 100 MHz and can achieve 200 MHz. Table 2 shows performance data for representative circuits, using worst-case timing parameters.

Table 2: Performance for Common Circuit Functions

Function	Bits	Virtex -6
Register-to-Register		
Adder	16 64	5.0 ns 7.2 ns
Pipelined Multiplier	8 x 8 16 x 16	5.1 ns 6.0 ns
Address Decoder	16 64	4.4 ns 6.4 ns
16:1 Multiplexer		5.4 ns
Parity Tree	9 18 36	4.1 ns 5.0 ns 6.9 ns
Chip-to-Chip		
HSTL Class IV		200 MHz
LVTTL,16mA, fast slew		180 MHz

Architectural Description

Virtex Array

The Virtex user-programmable gate array, shown in Figure 1, comprises two major configurable elements: configurable logic blocks (CLBs) and input/output blocks (IOBs).

- CLBs provide the functional elements for constructing logic
- IOBs provide the interface between the package pins and the CLBs

CLBs interconnect through a general routing matrix (GRM). The GRM comprises an array of routing switches located at the intersections of horizontal and vertical routing channels. Each CLB nests into a VersaBlock™ that also provides local routing resources to connect the CLB to the GRM.

The VersaRing™ I/O interface provides additional routing resources around the periphery of the device. This routing improves I/O routability and facilitates pin locking.

The Virtex architecture also includes the following circuits that connect to the GRM.

- Dedicated block memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- 3-State buffers (BUFTs) associated with each CLB that drive dedicated segmentable horizontal routing resources

Values stored in static memory cells control the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

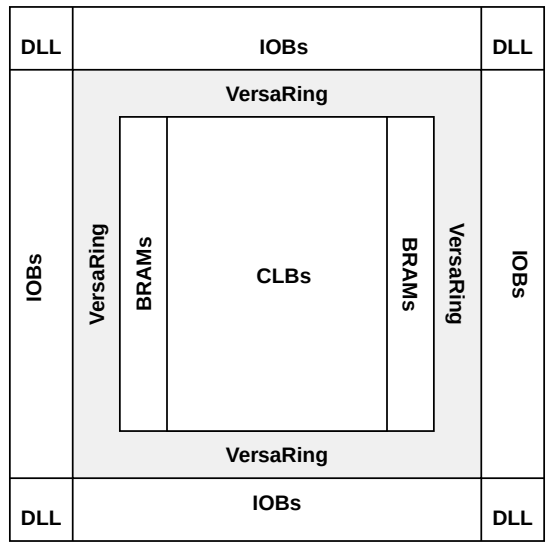


Figure 1: Virtex Architecture Overview

Input/Output Block

The Virtex IOB, Figure 2, features SelectIO™ inputs and outputs that support a wide variety of I/O signalling standards, see Table 3.

The three IOB storage elements function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three flip-flops and independent clock enable signals for each flip-flop.

In addition to the CLK and CE control signals, the three flip-flops share a Set/Reset (SR). For each flip-flop, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

The output buffer and all of the IOB control signals have independent polarity controls.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5 V compliance, and one that does not. For 5 V compliance, a Zener-like structure connected to ground turns on when the output rises to approximately 6.5 V. When PCI 3.3 V compliance is required, a conventional clamp diode is connected to the output supply voltage, V_{CCO}.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration, all pins not involved in configuration are forced into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up.

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All Virtex IOBs support IEEE 1149.1-compatible boundary scan testing.

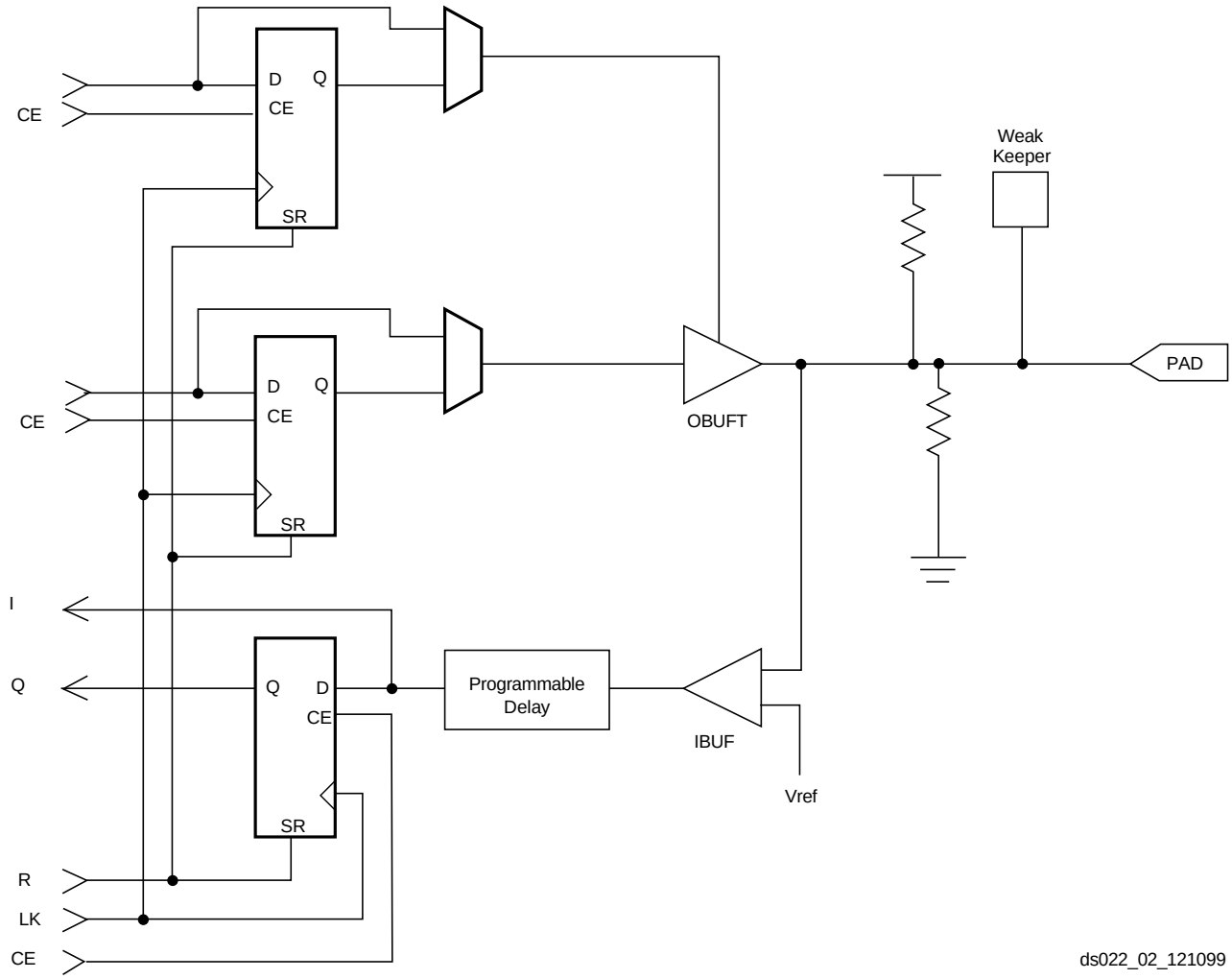


Figure 2: Virtex Input/Output Block (IOB)

Table 3: Supported Select I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})	5 V Tolerant
LVTTL 2 – 24 mA	N/A	3.3	N/A	Yes
LVCMOS2	N/A	2.5	N/A	Yes
PCI, 5 V	N/A	3.3	N/A	Yes
PCI, 3.3 V	N/A	3.3	N/A	No
GTL	0.8	N/A	1.2	No
GTL+	1.0	N/A	1.5	No
HSTL Class I	0.75	1.5	0.75	No
HSTL Class III	0.9	1.5	1.5	No
HSTL Class IV	0.9	1.5	1.5	No
SSTL3 Class I &II	1.5	3.3	1.5	No
SSTL2 Class I & II	1.25	2.5	1.25	No
CTT	1.5	3.3	1.5	No
AGP	1.32	3.3	N/A	No

Input Path

A buffer In the Virtex IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See “I/O Banking” on page 78.

There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 50 – 100 kΩ.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 78.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way eliminates bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Within a bank, output standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 4. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

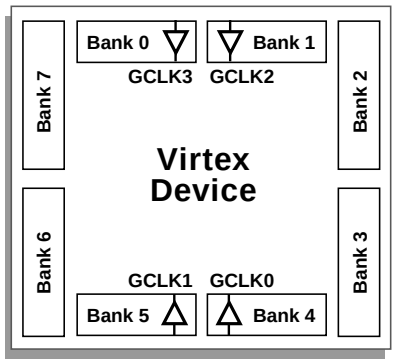


Figure 3: Virtex I/O Banks

Table 4: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3 V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5 V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5 V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5 V tolerant. LVTTL, LVCMOS2, and PCI 33 MHz 5 V, are 5 V tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins may be left unconnected externally, or may be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In TQ144 and PQ/HQ240 packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, permitting four choices for VCCO. In both cases, the V_{REF} pins remain internally connected as eight banks, and may be used as described previously.

Configurable Logic Block

The basic building block of the Virtex CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Virtex CLB contains four LCs, organized in two similar slices, as shown in Figure 4. Figure 5 shows a more detailed view of a single slice.

In addition to the four basic LCs, the Virtex CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Virtex function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16x1-bit dual-port synchronous RAM.

The Virtex LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Virtex slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously. All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

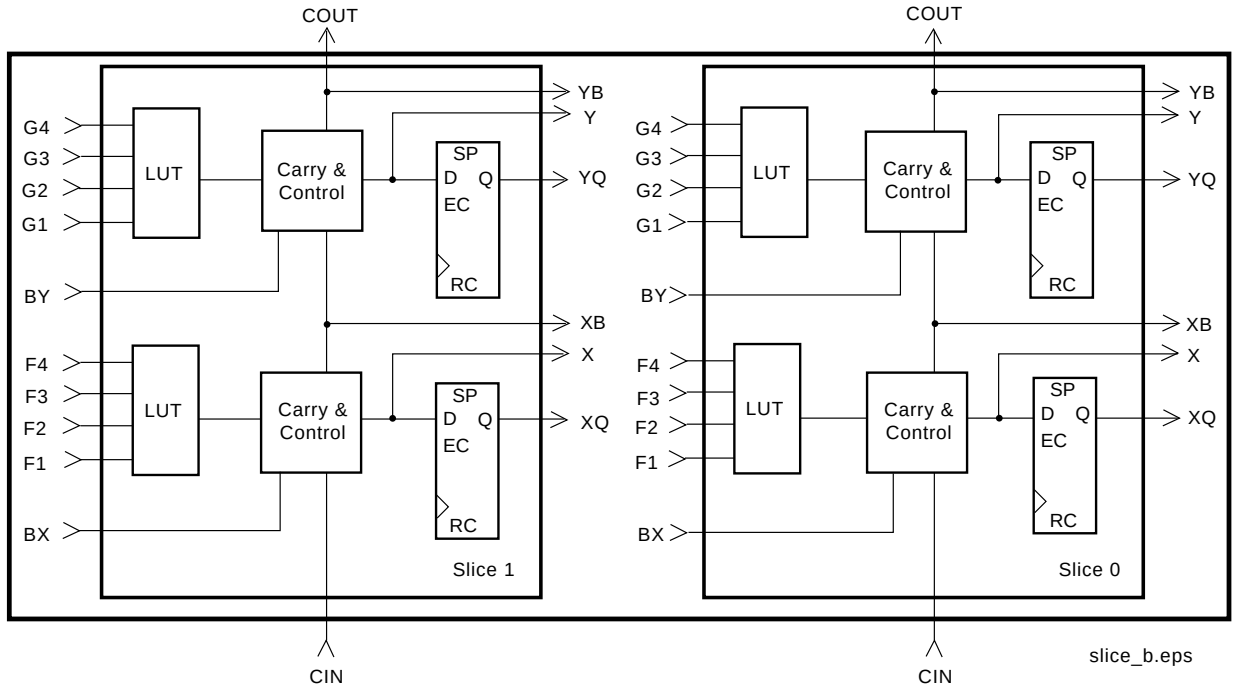


Figure 4: 2-Slice Virtex CLB

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Virtex CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Virtex CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See “Dedicated Routing” on page 83. Each Virtex BUFT has an independent 3-state control pin and an independent input pin.

Block SelectRAM

Virtex FPGAs incorporate several large Block SelectRAM memories. These complement the distributed LUT SelectRAMs that provide shallow RAM structures implemented in CLBs.

Block SelectRAM memory blocks are organized in columns. All Virtex devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Virtex device 64 CLBs high contains 16 memory blocks per column, and a total of 32 blocks.

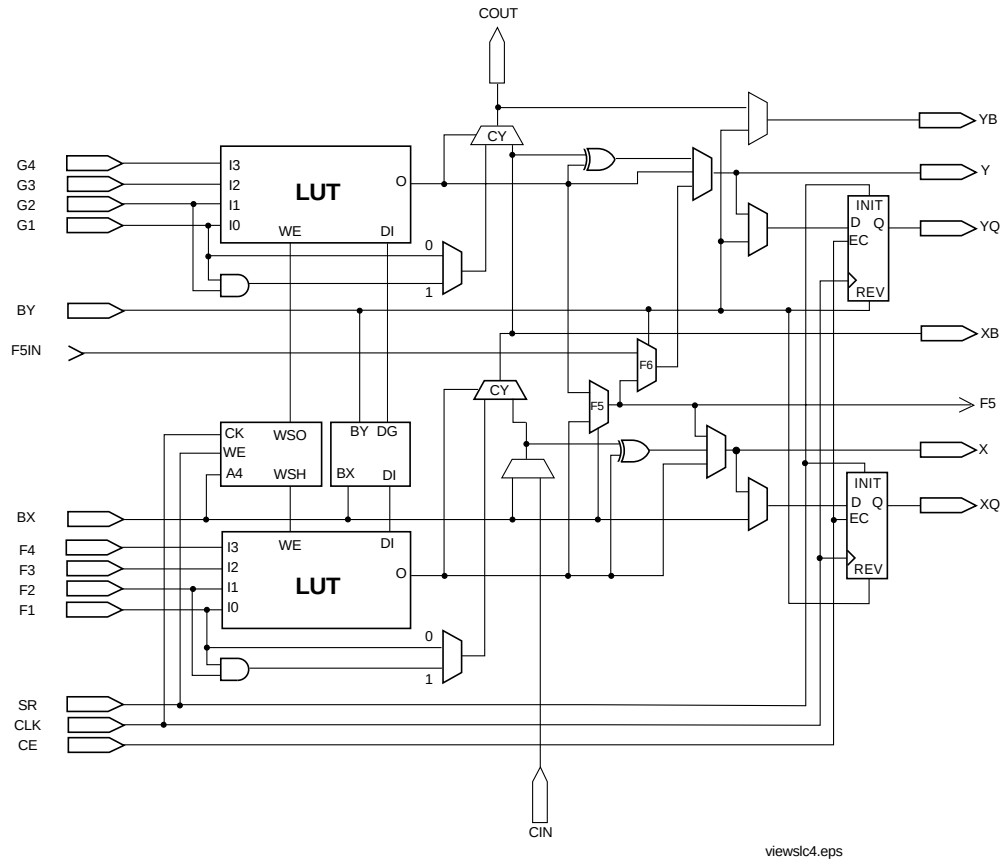


Figure 5: Detailed View of VIrtex Slice

Table 5 shows the amount of Block SelectRAM memory that is available in each Virtex device.

Table 5: Virtex Block SelectRAM Amounts

Virtex Device	# of Blocks	Total Block SelectRAM Bits
XCV50	8	32,768
XCV100	10	40,960
XCV150	12	49,152
XCV200	14	57,344
XCV300	16	65,536
XCV400	20	81,920
XCV600	24	98,304
XCV800	28	114,688
XCV1000	32	131,072

Each Block SelectRAM cell, as illustrated in Figure 6, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.‘

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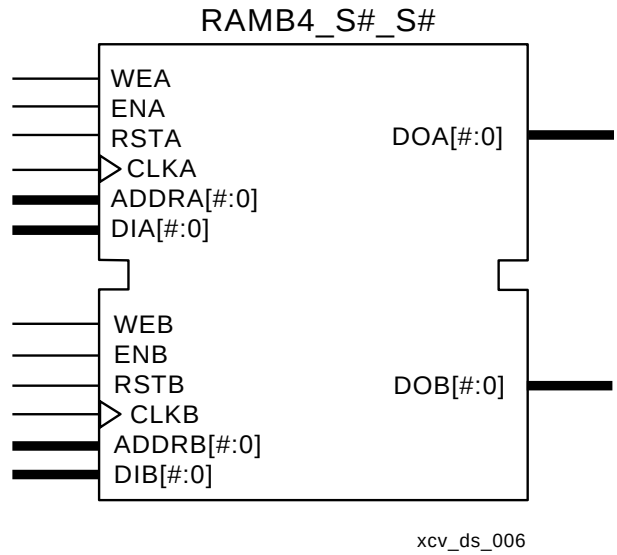


Figure 6: Dual-Port Block SelectRAM

Table 6 shows the depth and width aspect ratios for the Block SelectRAM

Table 6: Block SelectRAM Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Virtex Block SelectRAM also includes dedicated routing to provide an efficient interface with both CLBs and other Block SelectRAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Virtex routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 7, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

General Purpose Routing

Most Virtex signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 72 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Virtex devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

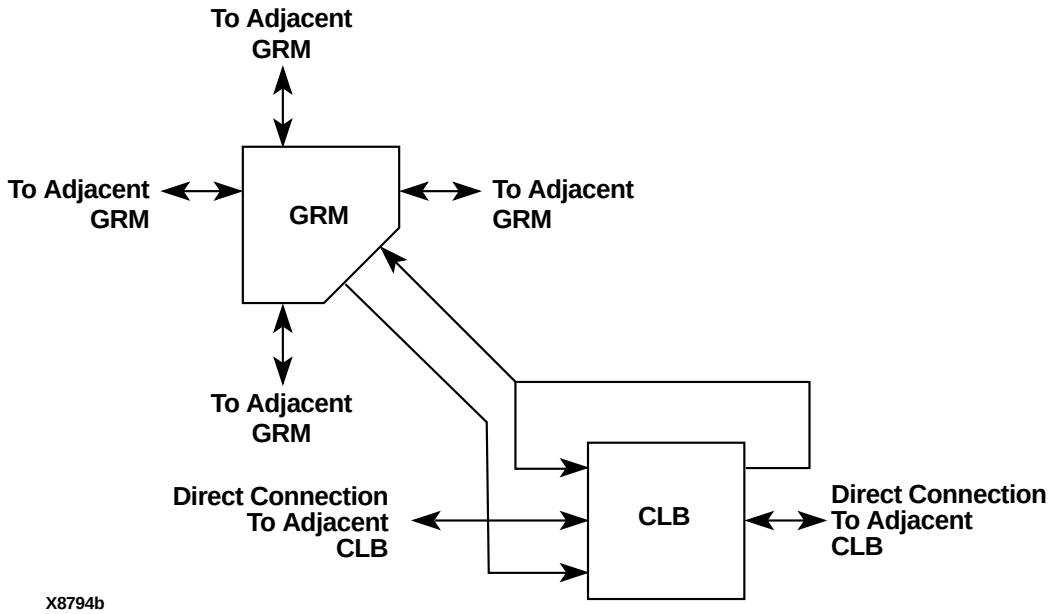


Figure 7: Virtex Local Routing

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Virtex architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure •.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Virtex devices include two tiers of global routing resources referred to as primary global and secondary local clock routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary local clock routing resources consist of 24 backbone lines, 12 across the top of the chip and 12 across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

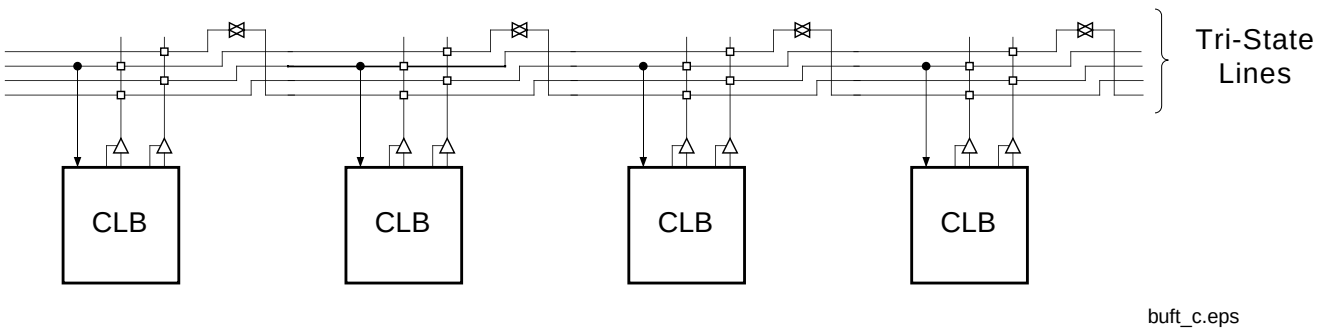


Figure 8: BUFT Connections to Dedicated Horizontal Bus Lines

Clock Distribution

Virtex provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure .

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Clock edges reach internal flip-flops one to four clock periods after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock, can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to de-skew a board level clock among multiple Virtex devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

See “DLL Timing Parameters” on page 113 for frequency range information.

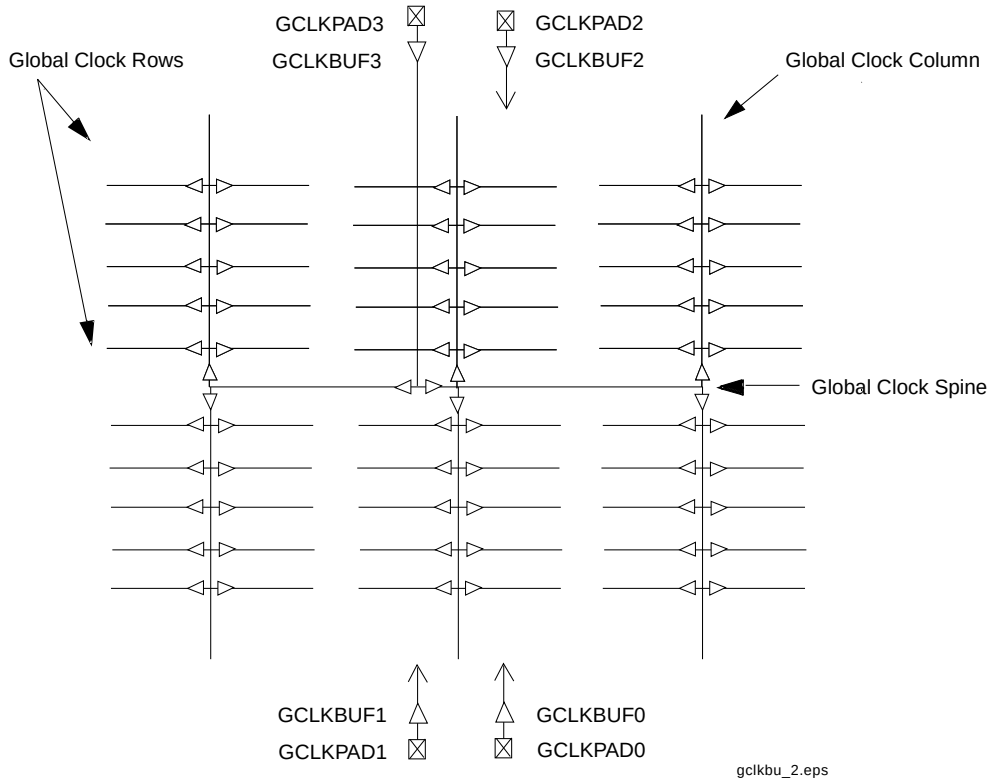


Figure 9: Global Clock Distribution Network

Boundary Scan

Virtex devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, INTEST, SAMPLE/PRELOAD, BYPASS, IDCODE, USERCODE, and HIGHZ instructions. The TAP also supports two internal scan chains and configuration/readback of the device.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 should be 3.3 V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including un-bonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 7 lists the boundary-scan instructions supported in Virtex FPGAs. Internal signals can be captured during EXTEST by connecting them to un-bonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins.

Before the device is configured, all instructions except USER1 and USER2 are available. After configuration, all instructions are available. During configuration, it is recommended that those operations using the boundary-scan register (SAMPLE/PRELOAD, INTEST, EXTEST) not be performed.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

Figure 10 is a diagram of the Virtex Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Instruction Set

The Virtex Series boundary scan instruction set also includes instructions to configure the device and read back configuration data (CFG_IN, CFG_OUT, and JSTART). The complete instruction set is coded as shown in Table 7.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out, and 3-State Control. Non-IOB pins have appropriate partial bit population if input-only or output-only. Each EXTEST CAPTURED-OR state captures all In, Out, and 3-state pins.

Table 7: Boundary Scan Instructions

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE/PRELOAD	00001	Enables boundary-scan SAMPLE/PRELOAD operation
USER 1	00010	Access user-defined register 1
USER 2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for read operations.
CFG_IN	00101	Access the configuration bus for write operations.
INTEST	00111	Enables boundary-scan INTEST operation
USERCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIGHZ	01010	Tri-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA supports up to two additional internal scan chains that can be specified using the BSCAN macro. The macro provides two user pins (SEL1 and SEL2) which are decodes of the USER1 and USER2 instructions respectively. For these instructions, two corresponding pins (TDO1 and TDO2) allow user scan data to be shifted out of TDO.

Likewise, there are individual clock pins (DRCK1 and DRCK2) for each user register. There is a common input pin (TDI) and shared output pins that represent the state of the TAP controller (RESET, SHIFT, and UPDATE)

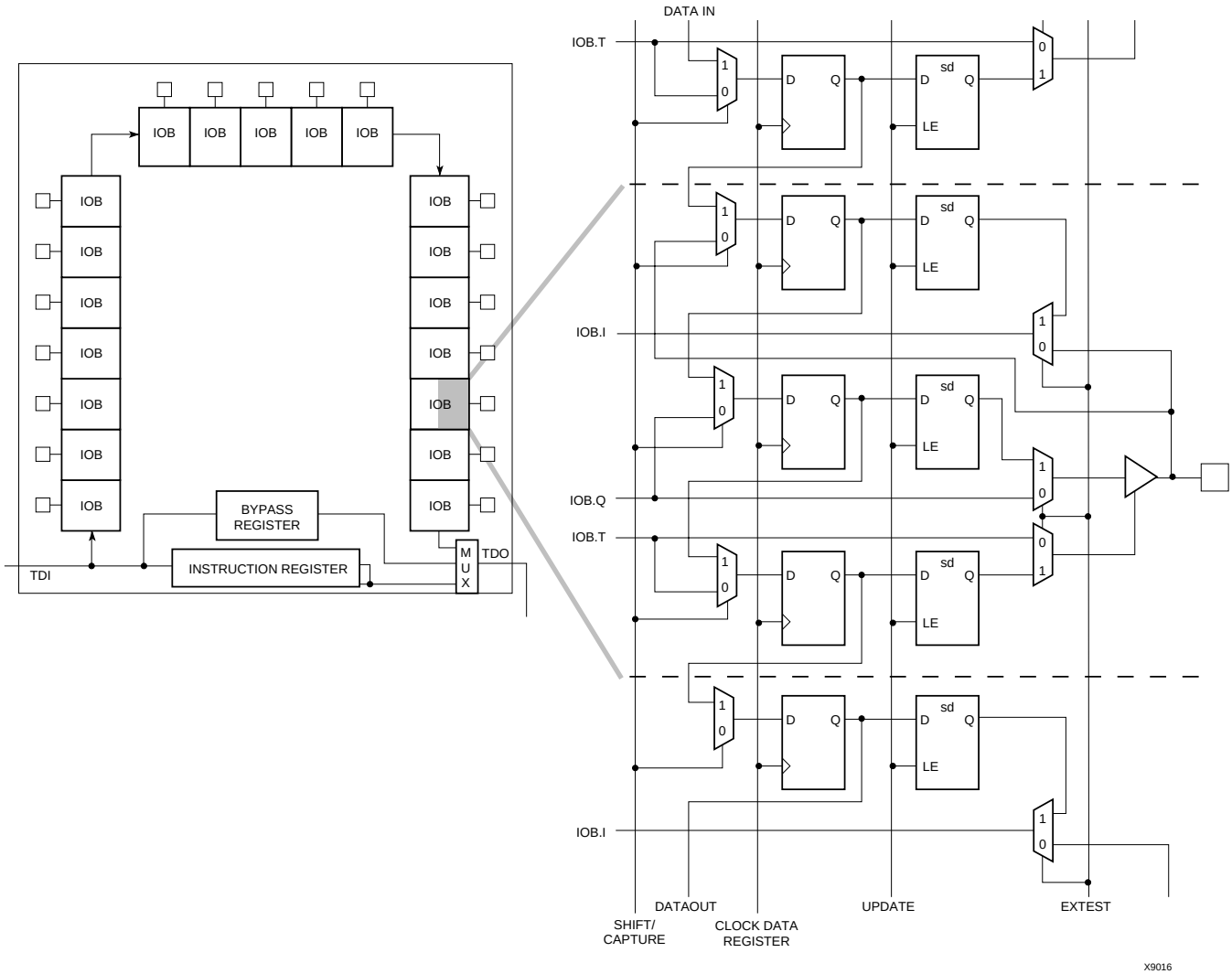


Figure 10: Virtex Series Boundary Scan Logic

Bit Sequence

The order within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 11.

BSDL (Boundary Scan Description Language) files for Virtex Series devices are available on the Xilinx web site in the File Download area.

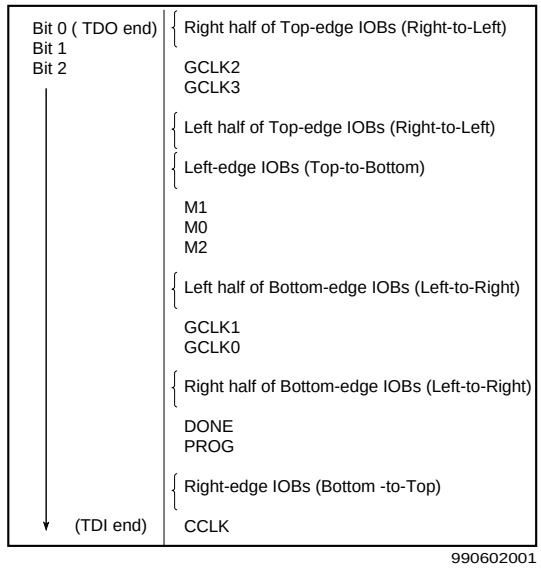


Figure 11: Boundary Scan Bit Sequence

Identification Registers

The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

v = the die version number

f = the family code (03h for Virtex family)

a = the number of CLB rows (ranges from 010h for XCV50 to 040h for XCV1000)

c = the company code (49h for Xilinx)

The USERCODE register is supported. By using the USERCODE, a user-programmable identification code can be loaded and shifted out for examination. The identification code is embedded in the bitstream during bitstream generation and is valid only after configuration.

Table 8: IDCODEs Assigned to Virtex FPGAs

FPGA	IDCODE
XCV50	v0610093h
XCV100	v0614093h
XCV150	v0618093h
XCV200	v061C093h
XCV300	v0620093h
XCV400	v0628093h
XCV600	v0630093h
XCV800	v0638093h
XCV1000	v0640093h

Including Boundary Scan in a Design

Since the boundary scan pins are dedicated, no special element needs to be added to the design unless an internal data register (USER1 or USER2) is desired.

If an internal data register is used, insert the boundary scan symbol and connect the necessary pins as appropriate.

Development System

Virtex FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Virtex design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Virtex design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Virtex FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The “soft macro” portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF net list for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floor planning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the net list for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Virtex devices are configured by loading configuration data into the internal configuration memory. Some of the pins used for this are dedicated configuration pins, while others may be re-used as general purpose inputs and outputs once configuration is complete.

The dedicated pins are the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the $\overline{\text{INIT}}$ pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the configuration mode chosen, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins may act as outputs. For correct operation, these pins may require a V_{CCO} of 3.3 V to permit LVTTL operation. All the pins affected fall in banks 2 or 3.

After Virtex devices are configured, unused IOBs function as tri-state OBUFTs with weak pull downs.

For a more detailed description than that given below, see the XAPP138, Virtex Configuration and Readback.

Configuration Modes

Virtex supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- SelectMAP mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 9.

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Table 9: Configuration Codes

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups
Master-serial mode	0	0	0	Out	1	Yes	No
Boundary-scan mode	1	0	1	N/A	1	No	No
SelectMAP mode	1	1	0	In	8	No	No
Slave-serial mode	1	1	1	In	1	Yes	No

Configuration Mode	M2	M1	M0	CCLK Direction	Data Width	Serial D_{out}	Configuration Pull-ups
Master-serial mode	1	0	0	Out	1	Yes	Yes
Boundary-scan mode	0	0	1	N/A	1	No	Yes
SelectMAP mode	0	1	0	In	8	No	Yes
Slave-serial mode	0	1	1	In	1	Yes	Yes

Slave Serial Mode

In slave serial mode, the FPGA receives configuration data in bit-serial form from a serial PROM or other source of serial configuration data. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.

Multiple FPGAs can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK.

The change of DOUT on the rising edge of CCLK differs from previous families, but will not cause a problem for mixed configuration chains. This change was made to improve serial-configuration rates for Virtex only chains.

Figure 12 shows a full master/slave system. A Virtex device in slave serial mode should be connected as shown in the third device from the left

Slave-serial mode is selected by applying <111> or <011> to the mode pins (M2, M1, M0). A weak pull-up on the mode pins makes slave serial the default mode if the pins are left unconnected. Figure 13 shows slave-serial configuration timing.

Table 10 provides more detail about the characteristics shown in Figure 13. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Table 10: Master/Slave Serial Mode Programming Switching

	Description	Symbol			Units
CCLK	DIN setup/hold, slave mode	1/2	T_{DCC}/T_{CCD}	5.0 / 0	ns, min
	DIN setup/hold, master mode	1/2	T_{DSCK}/T_{SCKD}	5.0 / 0	ns, min
	DOUT	3	T_{CCO}	12.0	ns, max
	High time	4	T_{CCH}	5.0	ns, min
	Low time	5	T_{CCL}	5.0	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max
	Frequency Tolerance, master mode with respect to nominal			+45% -30%	

.

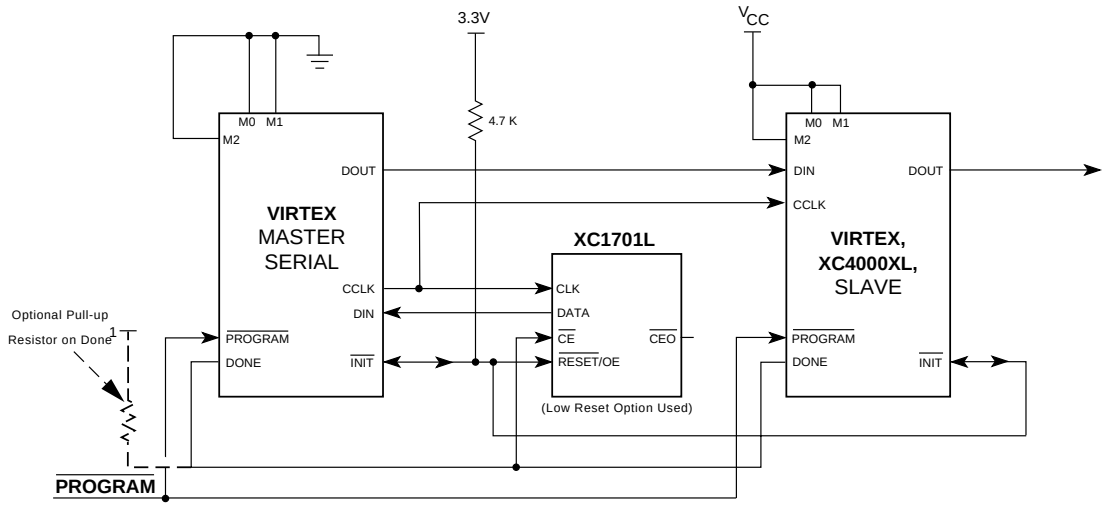


Figure 12: Master/Slave Serial Mode Circuit Diagram

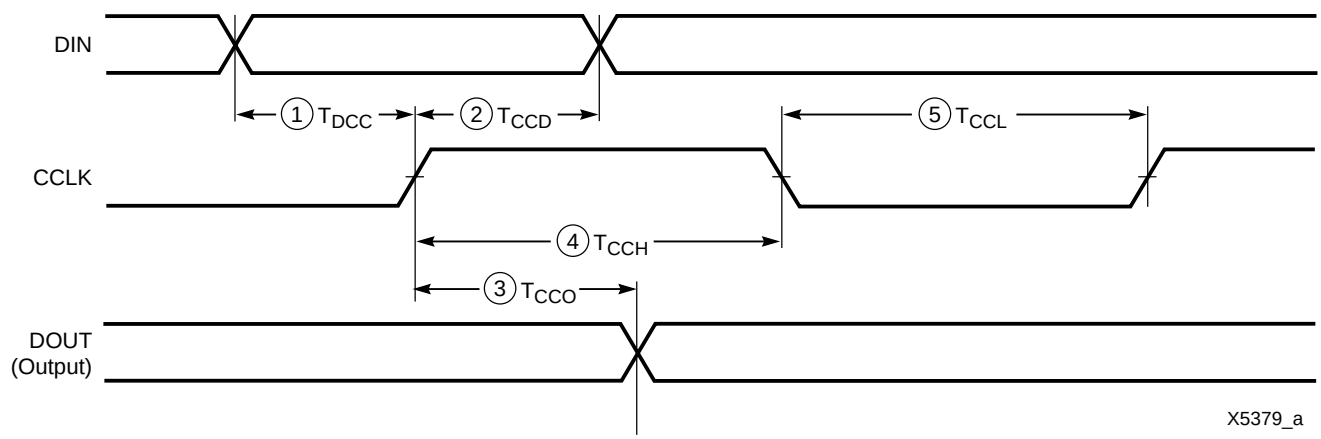


Figure 13: Slave Serial Mode Programming Switching Characteristics

Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM that feeds bit-serial data to the DIN input. The FPGA accepts this data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

The interface is identical to slave serial except that an internal oscillator is used to generate the configuration clock (CCLK). A wide range of frequencies can be selected for CCLK which always starts at a slow default frequency. Configuration bits then switch CCLK to a higher frequency for the remainder of the configuration. Switching to a lower frequency is prohibited.

The CCLK frequency is set using the ConfigRate option in the bitstream generation software. The maximum CCLK frequency that can be selected is 60 MHz. When selecting a CCLK frequency, ensure that the serial PROM and any daisy-chained FPGAs are fast enough to support the clock rate.

On power-up, the CCLK frequency is 2.5 MHz. This frequency is used until the ConfigRate bits have been loaded when the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz.

Figure 12 shows a full master/slave system. In this system, the left-most device operates in master-serial mode. The remaining devices operate in slave-serial mode. The SPROM $\overline{\text{RESET}}$ pin is driven by $\overline{\text{INIT}}$, and the $\overline{\text{CE}}$ input is driven by DONE. There is the potential for contention on the DONE pin, depending on the start-up sequence options chosen.

The sequence of operations necessary to configure a Virtex FPGA serially appears in Figure 14.

Figure 15 shows the timing of master-serial configuration. Master serial mode is selected by a <000> or <100> on the mode pins (M2, M1, M0). Table 10 shows the timing information for Figure 15.

At power-up, Vcc must rise from 1.0 V to Vcc min in less than 50 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until Vcc is valid.

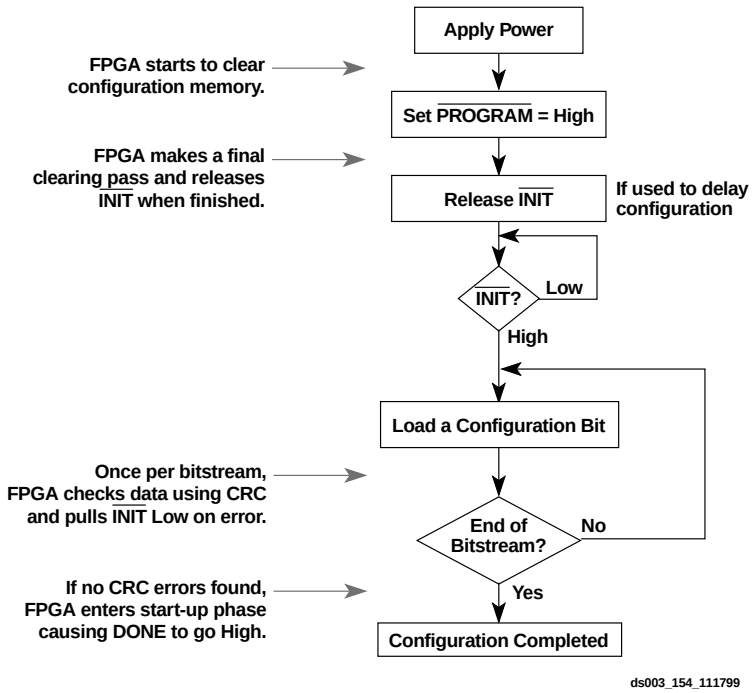
SelectMAP Mode

The SelectMAP mode is the fastest configuration option. Byte-wide data is written into the FPGA with a BUSY flag controlling the flow of data.

An external data source provides a byte stream, CCLK, a Chip Select ($\overline{\text{CS}}$) signal and a Write signal ($\overline{\text{WRITE}}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

Data can also be read using the SelectMAP mode. If $\overline{\text{WRITE}}$ is not asserted, configuration data is read out of the FPGA as part of a readback operation.

In the SelectMAP mode, multiple Virtex devices may be chained in parallel. DATA pins (D7:D0), CCLK, $\overline{\text{WRITE}}$, $\overline{\text{BUSY}}$, PROG, DONE, and $\overline{\text{INIT}}$ may be connected in parallel between all the FPGAs. Note that the data is organized with the MSB of each byte on pin DO and the LSB of each byte on D7. The $\overline{\text{CS}}$ pins are kept separate, insuring that each FPGA can be selected individually. $\overline{\text{WRITE}}$ should be Low before loading the first bitstream and returned High after the last device has been programmed. Use $\overline{\text{CS}}$ to select the appropriate FPGA for loading the bitstream and sending the configuration data. at the end of the bitstream, deselect the loaded device and select the next target FPGA by setting its $\overline{\text{CS}}$ pin High. A free-running oscillator or other externally generated signal can be used for CCLK. The $\overline{\text{BUSY}}$ signal may be ignored for frequencies below 50 MHz. For details about frequencies above 50 MHz, see XAPP138, Virtex Configuration and Readback. Once all the devices have been programmed, the DONE pin goes High.



igure 14: Serial Configuration Flowchart

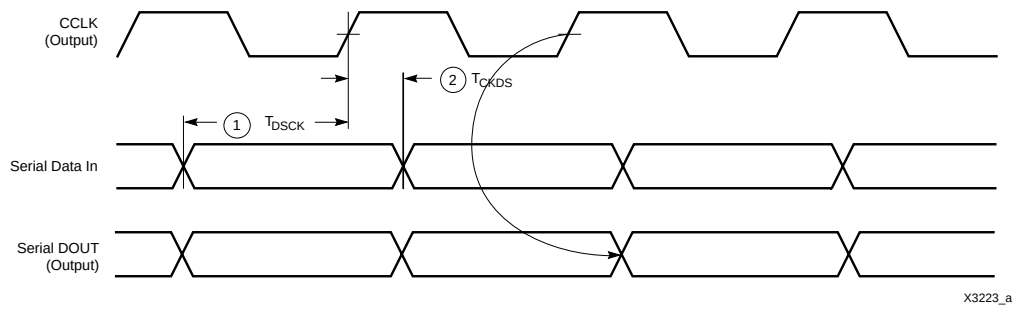


Figure 15: Master Serial Mode Programming Switching Characteristics

After configuration, the pins of the SelectMAP port can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback.

Retention of the SelectMAP port is selectable on a design-by-design basis when the bitstream is generated. If retention is selected, PROHIBIT constraints are required to prevent the SelectMAP-port pins from being used as user I/O.

Multiple Virtex FPGAs can be configured using the Select-MAP mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. See Table 11 for SelectMAP Write Timing Characteristics.

Table 11: SelectMAP Write Timing Characteristics

	Description		Symbol		Units
CCLK	D_{0-7} Setup/Hold	1/2	T_{SMDCC}/T_{SMCCD}	5.0 / 0	ns, min
	$\overline{\text{CS}}$ Setup/Hold	3/4	T_{SMCSCC}/T_{SMCCCS}	7.0 / 0	ns, min
	$\overline{\text{WRITE}}$ Setup/Hold	5/6	T_{SMCCW}/T_{SMWCC}	7.0 / 0	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12.0	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

3

Write

Write operations send packets of configuration data into the FPGA. The sequence of operations for a multi-cycle write operation is shown below. Note that a configuration packet can be split into many such sequences. The packet does not have to complete within one assertion of $\overline{\text{CS}}$, illustrated in Figure 16.

7. Assert $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as described below.
8. Drive data onto D[7:0]. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more that one $\overline{\text{CS}}$ should be asserted.
9. At the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this has happened.
10. Repeat steps 2 and 3 until all the data has been sent.
11. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

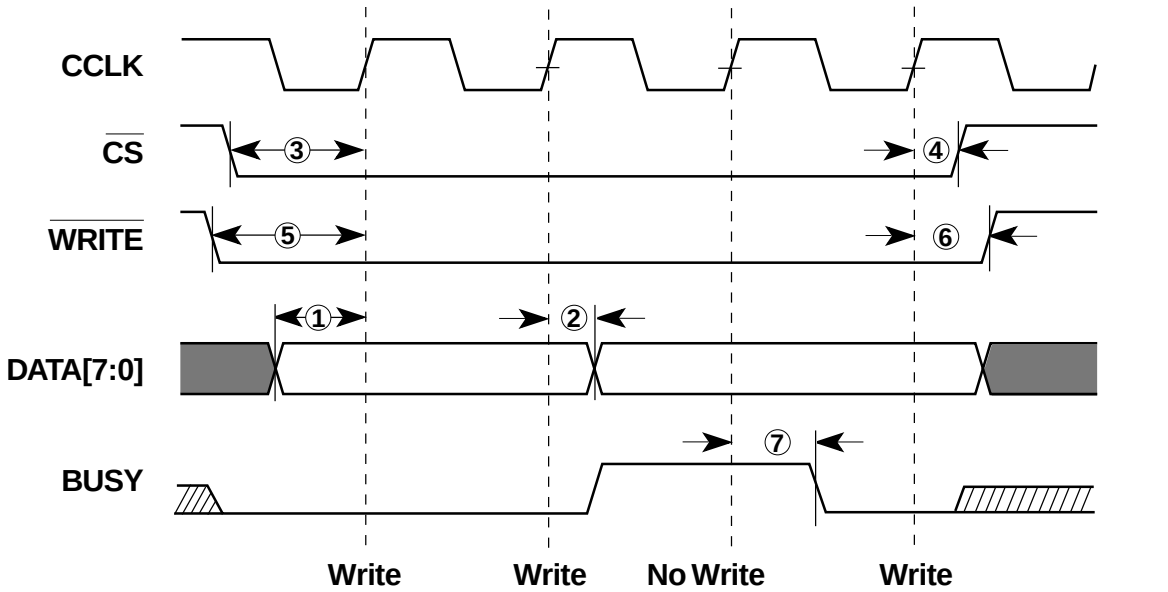


Figure 16: Write Operations

A flowchart for the write operation appears in Figure 17. Note that if CCLK is slower than f_{CCNH}, the FPGA will never assert BUSY, In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

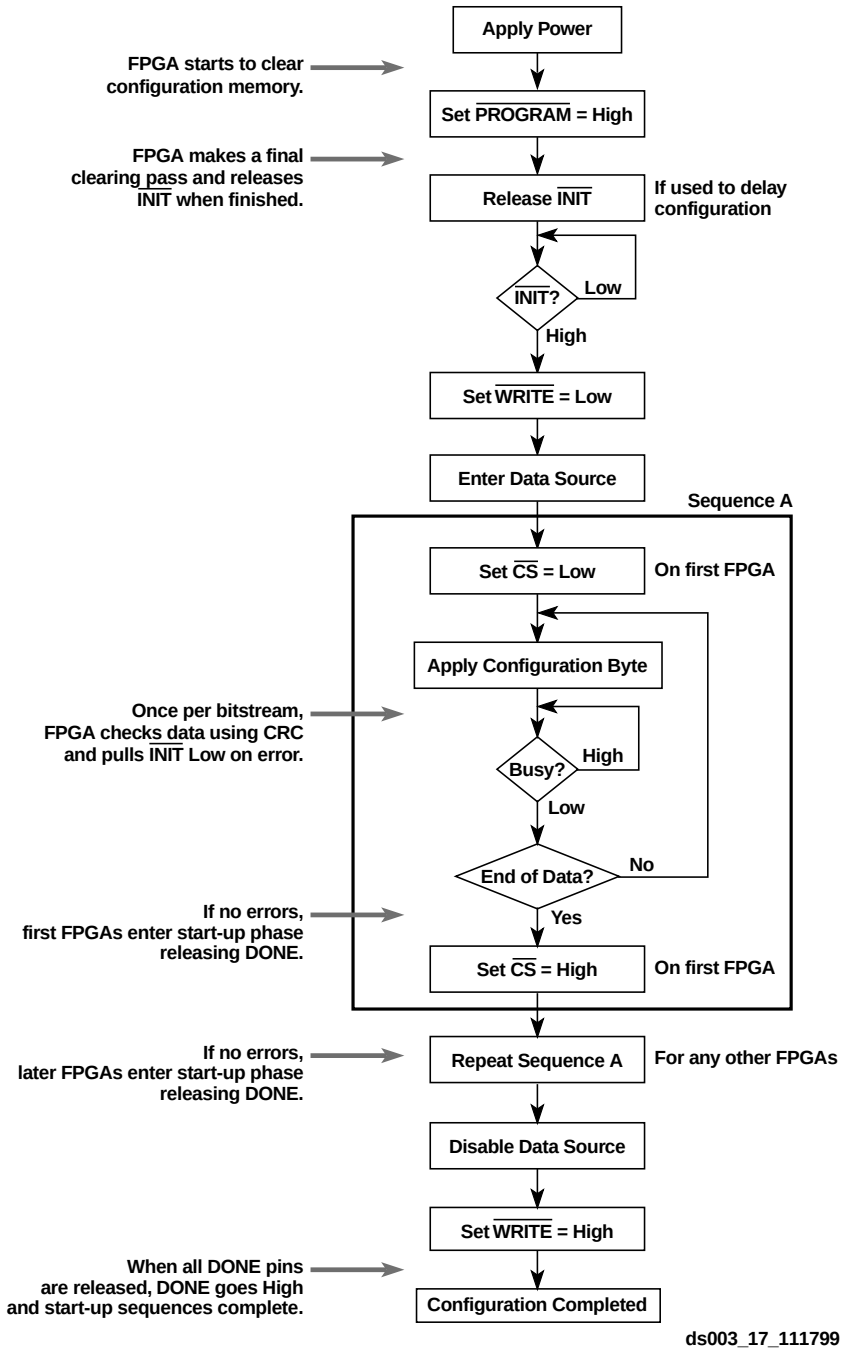


Figure 17: SelectMAP Flowchart for Write Operation

Abort

During a given assertion of $\overline{CS}$, the user cannot switch from a write to a read, or vice-versa. This action causes the current packet command to be aborted. The device will remain BUSY until the aborted operation has completed. Following an abort, data is assumed to be unaligned to word boundaries, and the FPGA requires a new synchronization word prior to accepting any new packets.

To initiate an abort during a write operation, de-assert $\overline{\text{WRITE}}$. At the rising edge of CCLK, an abort is initiated, as shown in Figure 18.

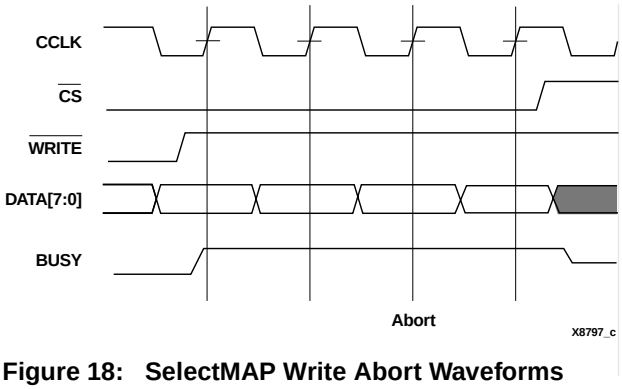


Figure 18: SelectMAP Write Abort Waveforms

Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port (when using TCK as a start-up clock).

1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the startup sequence
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode is selected by a <101> or 001> on the mode pins (M2, M1, M0).

Configuration Sequence

The configuration of Virtex devices is a three-phase process. First, the configuration memory is cleared. Next, configuration data is loaded into the memory, and finally, the logic is activated by a start-up process.

Configuration is automatically initiated on power-up unless it is delayed by the user, as described below. The configuration process may also be initiated by asserting $\overline{\text{PROGRAM}}$. The end of the memory-clearing phase is signalled by $\overline{\text{INIT}}$ going High, and the completion of the entire process is signalled by DONE going High.

The power-up timing of configuration signals is shown in Figure 19. The corresponding timing characteristics are listed in Table 12.

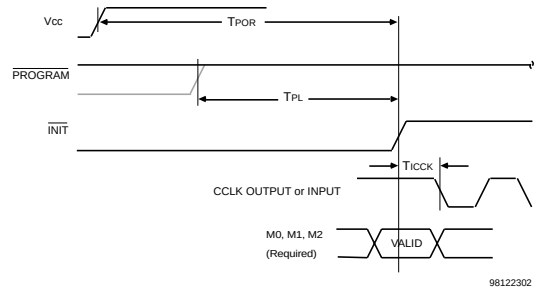


Figure 19: Power-up Timing Configuration Signals

Table 12: Power-up Timing Characteristics

Description	Symbol	Value	Units
Power-on Reset	T_{POR}	2.0	ms, max
Program Latency	T_{PL}	100.0	µs, max
CCLK (output) Delay	T_{ICCK}	0.5	µs, min
		4.0	µs, max
Program Pulse Width	$T_{PROGRAM}$	300	ns, min

Delaying Configuration

$\overline{\text{INIT}}$ can be held Low using an open-drain driver. An open-drain is required since $\overline{\text{INIT}}$ is a bidirectional open-drain pin that is held Low by the FPGA while the configuration memory is being cleared. Extending the time that the pin is Low causes the configuration sequencer to wait. Thus, configuration is delayed by preventing entry into the phase where data is loaded.

Start-Up Sequence

The default Start-up sequence is that one CCLK cycle after DONE goes High, the global tri-state signal (GTS) is released. This permits device outputs to turn on as necessary.

One CCLK cycle later, the Global Set/Reset (GSR) and Global Write Enable (GWE) signals are released. This permits the internal storage elements to begin changing state in response to the logic and the user clock.

The relative timing of these events may be changed. In addition, the GTS, GSR, and GWE events may be made dependent on the DONE pins of multiple devices all going High, forcing the devices to start in synchronism. The sequence may also be paused at any stage until lock has been achieved on any or all DLLs.

Data Stream Format

Virtex devices are configured by sequentially loading frames of data. Table 13 lists the total number of bits required to configure each device. For more detailed information, see application note XAPP151 “Virtex Configuration Architecture Advanced Users Guide”.

Table 13: Virtex Bit-stream Lengths

Device	# of Configuration Bits
XCV50	559,200
XCV100	781,216
XCV150	1,040,096
XCV200	1,335,840
XCV300	1,751,808
XCV400	2,546,048
XCV600	3,607,968
XCV800	4,715,616
XCV1000	6,127,744

Readback

The configuration data stored in the Virtex configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information, see application note XAPP138 “Virtex FPGA Series Configuration and Readback”.

Virtex Electrical Characteristics

Definition of Terms

Data sheets may be designated as Advance or Preliminary. The status of specifications in these data sheets is as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Data sheets not identified as either Advance or Preliminary are to be considered final.

All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications. Contact the factory for design considerations requiring more detailed information.

All specifications are subject to change without notice.

Virtex DC Characteristics

Absolute Maximum Ratings

Symbol	Description			Units
V_{CCINT}	Supply voltage relative to GND		-0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		-0.5 to 4.0	V
V_{REF}	Input Reference Voltage		-0.5 to 3.6	V
V_{IN}	Input voltage relative to GND	Using V_{REF}	-0.5 to 3.6	V
		Internal threshold	-0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		-0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1V-2.375V		50	ms
T_{STG}	Storage temperature (ambient)		-65 to +150	°C
T_{SOL}	Maximum soldering temp. (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic Packages	+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Power supplies may turn on in any order.

For protracted periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more than 3.6 V.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Input Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.5 - 5%	2.5 + 5%	V
	Input Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	2.5 - 5%	2.5 + 5%	V
V_{CCO} *	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	1.4	3.6	V
	Supply voltage relative to GND, T_J = -40°C to +100°C	Industrial	1.4	3.6	V
T_{IN}	Input signal transition time			250	ns

Notes: Correct operation is guaranteed with a minimum V_{CCINT} of 2.375 V (Nominal V_{CCINT} -5%). Below the minimum value, all delay parameters increase by 3% for each 50-mV reduction in V_{CCINT} below the specified range.

At junction temperatures above those listed as Operating Conditions, delay parameters do increase. Please refer to the TRCE report.

Input and output measurement threshold is ~50% of V_{CC}.

* Note that Min and Max values for V_{CCO} are I/O Standard dependant.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description	Device	Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)	All	2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)	All	1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Notes 1 and 3)	XCV50		50	mA
		XCV100		50	mA
		XCV150		50	mA
		XCV200		75	mA
		XCV300		75	mA
		XCV400		75	mA
		XCV600		100	mA
		XCV800		100	mA
		XCV1000		100	mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)	XCV50		2	mA
		XCV100		2	mA
		XCV150		2	mA
		XCV200		2	mA
		XCV300		2	mA
		XCV400		2	mA
		XCV600		2	mA
		XCV800		2	mA
		XCV1000		2	mA
I_{REF}	V_{REF} current per V_{REF} pin	All		20	µA
I_L	Input or output leakage current	All	-10	+10	µA
C_{IN}	Input capacitance (sample tested) BGA, PQ, HQ, packages	All		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{in} = 0 V, V_{CCO} = 3.3 V (sample tested)	All	Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{in} = 3.6 V (sample tested)		Note 2	0.15	mA

Notes: 1. With no output current loads, no active input pull-up resistors, all I/O pins Tri-stated and floating.
2. Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.
3. Multiply I_{CCINTQ} limit by two for industrial grade.

Power-On Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the nominal power supply voltage of the device[1] from 0 V. The current is highest at the fastest suggested ramp rate (0 V to nominal voltage in 2 ms) and is lowest at the slowest allowed ramp rate (0 V to nominal voltage in 50 ms).

Product	Description[2]	Current Requirement[3]
Virtex Family, Commercial Grade	Minimum required current supply	500 mA
Virtex Family, Industrial Grade	Minimum required current supply	2 A

Notes: 1. Ramp rate used for this specification is from 0 - 2.7 V dc. Peak current occurs on or near the internal power-on reset threshold and lasts for less than 3 ms.
2. Devices are guaranteed to initialize properly with the minimum current available from the power supply as noted above.
3. Larger currents may result if ramp rates are forced to be faster.

DC Input and Output levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for I_{OL} and I_{OH} are guaranteed output currents over the recommended operating conditions at the V_{OL} and V_{OH} test points. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} for each standard with the respective V_{OL} and V_{OH} voltage levels shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	- 0.5	0.8	2.0	5.5	0.4	2.4	24	- 24
LVCMOS2	- 0.5	.7	1.7	5.5	0.4	1.9	12	-12
PCI, 3.3 V	- 0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	- 0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	- 0.5	V_{REF} - 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	8	-8
HSTL III	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	24	-8
HSTL IV	- 0.5	V_{REF} - 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} - 0.4	48	-8
SSTL3 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.6	V_{REF} + 0.6	8	-8
SSTL3 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.8	V_{REF} + 0.8	16	-16
SSTL2 I	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.61	V_{REF} + 0.61	7.6	-7.6
SSTL2 II	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.80	V_{REF} + 0.80	15.2	-15.2
CTT	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	V_{REF} - 0.4	V_{REF} + 0.4	8	-8
AGP	- 0.5	V_{REF} - 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Note 1: V_{OL} and V_{OH} for lower drive currents are sample tested.
Note 2: Tested according to the relevant specifications.

Virtex Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation net list. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Virtex devices unless otherwise noted.

IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, adjust the delays with the values shown in "IOB Input Switching Characteristics Standard Adjustments" on page 101.

		Speed Grade	All	-6	-5	-4	Units
Description	**Device**	**Symbol**	**Min**				
Propagation Delays							
Pad to I output, no delay	All	T_{IOPI}	0.39	0.8	0.9	1.0	ns, max
Pad to I output, with delay	XCV50	T_{IOPID}	0.8	1.5	1.7	1.9	ns, max
	XCV100		0.8	1.5	1.7	1.9	ns, max
	XCV150		0.8	1.5	1.7	1.9	ns, max
	XCV200		0.8	1.5	1.7	1.9	ns, max
	XCV300		0.8	1.5	1.7	1.9	ns, max
	XCV400		0.9	1.8	2.0	2.3	ns, max
	XCV600		0.9	1.8	2.0	2.3	ns, max
	XCV800		1.1	2.1	2.4	2.7	ns, max
	XCV1000		1.1	2.1	2.4	2.7	ns, max
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}	0.8	1.6	1.8	2.0	ns, max
Pad to output IQ via transparent latch, with delay	XCV50	T_{IOPLID}	1.9	3.7	4.2	4.8	ns, max
	XCV100		1.9	3.7	4.2	4.8	ns, max
	XCV150		2.0	3.9	4.3	4.9	ns, max
	XCV200		2.0	4.0	4.4	5.1	ns, max
	XCV300		2.0	4.0	4.4	5.1	ns, max
	XCV400		2.1	4.1	4.6	5.3	ns, max
	XCV600		2.1	4.2	4.7	5.4	ns, max
	XCV800		2.2	4.4	4.9	5.6	ns, max
	XCV1000		2.3	4.5	5.1	5.8	ns, max

IOB Input Switching Characteristics (Continued)

Description	Device	Symbol	Speed Grade / All Min	-6	-5	-4	Units
Sequential Delays							
Clock CLK to output IQ	All	T_{IOCKIQ}	0.2	0.7	0.7	0.8	ns, max
Setup and Hold Times with respect to Clock CLK at IOB input register			Setup Time / Hold Time				
Pad, no delay	All	T_{IOPICK}/T_{IOICKP}	0.8 / 0	1.6 / 0	1.8 / 0	2.0 / 0	ns, min
Pad, with delay	XCV50	$T_{IOPICKD}/T_{IOICKPD}$	1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, max
	XCV100		1.9 / 0	3.7 / 0	4.1 / 0	4.7 / 0	ns, max
	XCV150		1.9 / 0	3.8 / 0	4.3 / 0	4.9 / 0	ns, max
	XCV200		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, max
	XCV300		2.0 / 0	3.9 / 0	4.4 / 0	5.0 / 0	ns, max
	XCV400		2.1 / 0	4.1 / 0	4.6 / 0	5.3 / 0	ns, max
	XCV600		2.1 / 0	4.2 / 0	4.7 / 0	5.4 / 0	ns, max
	XCV800		2.2 / 0	4.4 / 0	4.9 / 0	5.6 / 0	ns, max
	XCV1000		2.3 / 0	4.5 / 0	5.0 / 0	5.8 / 0	ns, max
ICE input	All	$T_{IOICECK}/T_{IOCKICE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Set/Reset Delays							
SR input (IFF, synchronous)	All	$T_{IOSRCKI}$	0.49	1.0	1.1	1.3	ns, min
SR input to IQ (asynchronous)	All	T_{IOSRIQ}	0.70	1.4	1.6	1.8	ns, max
GSR to output IQ	All	T_{GSRQ}	4.9	9.7	10.9	12.5	ns, max

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.
Note: Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 16.

IOB Input Switching Characteristics Standard Adjustments

Description	Symbol	Standard	Speed Grade / All Min	-6	-5	-4	Units
Data Input Delay Adjustments							
Standard-specific data input delay adjustments	T_{ILVTTL}	LVTTL	0	0	0	0	ns
	$T_{ILVCMOS2}$	LVCMOS2	-0.02	-0.04	-0.04	-0.05	ns
	T_{IPCI33_3}	PCI, 33 MHz, 3.3 V	-0.05	-0.11	-0.12	-0.14	ns
	T_{IPCI33_5}	PCI, 33 MHz, 5.0 V	0.13	0.25	0.28	0.33	ns
	T_{IPCI66_3}	PCI, 66 MHz, 3.3 V	-0.05	-0.11	-0.12	-0.14	ns
	T_{IGTL}	GTL	0.10	0.20	0.23	0.26	ns
	T_{IGTLP}	GTL+	0.06	0.11	0.12	0.14	ns
	T_{IHSTL}	HSTL	0.02	0.03	0.03	0.04	ns
	T_{ISSTL2}	SSTL2	-0.04	-0.08	-0.09	-0.10	ns
	T_{ISSTL3}	SSTL3	-0.02	-0.04	-0.05	-0.06	ns
	T_{ICTT}	CTT	0.01	0.02	0.02	0.02	ns
	T_{IAGP}	AGP	-0.03	-0.06	-0.07	-0.08	ns
Note: Input timing for LVTTL is measured at 1.4 V. For other I/O standards, see Table 16.							

IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays with the values shown in "IOB Output Switching Characteristics Standard Adjustments" on page 103.

	Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Min**				
Propagation Delays						
O input to Pad	T_{IOOP}	1.2	2.9	3.2	3.5	ns, max
O input to Pad via transparent latch	T_{IOOLP}	1.4	3.4	3.7	4.0	ns, max
3-State Delays						
T input to Pad high-impedance (Note 1)	T_{IOTHZ}	1.0	2.0	2.2	2.4	ns, max
T input to valid data on Pad	T_{IOTON}	1.4	3.1	3.3	3.7	ns, max
T input to Pad high-impedance via transparent latch (Note 1)	$T_{IOTLPHZ}$	1.2	2.4	2.6	3.0	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$	1.6	3.5	3.8	4.2	ns, max
GTS to Pad high impedance (Note 1)	T_{GTS}	2.5	4.9	5.5	6.3	ns, max
Sequential Delays						
Clock CLK to Pad	T_{IOCKP}	1.0	2.9	3.2	3.5	ns, max
Clock CLK to Pad high-impedance (synchronous) (Note 1)	T_{IOCKHZ}	1.1	2.3	2.5	2.9	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}	1.5	3.4	3.7	4.1	ns, max
Setup and Hold Times before/after Clock CLK		Setup Time / Hold Time				
O input	T_{IOOCK}/T_{IOCKO}	0.51 / 0	1.1 / 0	1.2 / 0	1.3 / 0	ns, min
OCE input	$T_{IOOCECK}/T_{IOCKOCE}$	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR input (OFF)	$T_{IOSRCKO}/T_{IOCKOSR}$	0.52 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min
3-State Setup Times, T input	T_{IOTCK}/T_{IOCKT}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
3-State Setup Times, TCE input	$T_{IOTCECK}/T_{IOCKTCE}$	0.41 / 0	0.9 / 0	0.9 / 0	1.1 / 0	ns, min
3-State Setup Times, SR input (TFF)	$T_{IOSRCKT}/T_{IOCKTSR}$	0.49 / 0	1.0 / 0	1.1 / 0	1.3 / 0	ns, min
Set/Reset Delays						
SR input to Pad (asynchronous)	T_{IOSRP}	1.6	3.8	4.1	4.6	ns, max
SR input to Pad high-impedance (asynchronous) (Note 1)	T_{IOSRHZ}	1.6	3.1	3.4	3.9	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}	2.0	4.2	4.6	5.1	ns, max
GSR to Pad	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max

Notes: A Zero "0" Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed "best-case", but if a "0" is listed, there is no positive hold time.
Tri-state turn-off delays should not be adjusted.

IOB Output Switching Characteristics Standard Adjustments

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and fast slew rate. For other standards, adjust the delays by the values shown.

		Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Standard**	**Min**	**Adjustments**			
Output Delay Adjustments							
Standard-specific adjustments for output delays terminating at pads (based on standard capacitive load, Csl)	T_{OLVTTL_S2}	LVTTL, Slow,2 mA	4.2	14.7	15.8	17.0	ns
	T_{OLVTTL_S4}	4 mA	2.5	7.5	8.0	8.6	ns
	T_{OLVTTL_S6}	6 mA	1.8	4.8	5.1	5.6	ns
	T_{OLVTTL_S8}	8 mA	1.2	3.0	3.3	3.5	ns
	T_{OLVTTL_S12}	12 mA	1.0	1.9	2.1	2.2	ns
	T_{OLVTTL_S16}	16 mA	0.9	1.7	1.9	2.0	ns
	T_{OLVTTL_S24}	24 mA	0.8	1.3	1.4	1.6	ns
	T_{OLVTTL_F2}	LVTTL, Fast,2 mA	1.9	13.1	14.0	15.1	ns
	T_{OLVTTL_F4}	4 mA	0.7	5.3	5.7	6.1	ns
	T_{OLVTTL_F6}	6 mA	0.2	3.1	3.3	3.6	ns
	T_{OLVTTL_F8}	8 mA	0.1	1.0	1.1	1.2	ns
	T_{OLVTTL_F12}	12 mA	0	0	0	0	ns
	T_{OLVTTL_F16}	16 mA	-0.10	-0.05	-0.05	-0.05	ns
	T_{OLVTTL_F24}	24 mA	-0.10	-0.20	-0.21	-0.23	ns
	$T_{OLVCMOS2}$	LVCMOS2	0.10	0.10	0.11	0.12	ns
	T_{OPCI33_3}	PCI, 33 MHz, 3.3 V	0.50	2.3	2.5	2.7	ns
	T_{OPCI33_5}	PCI, 33 MHz, 5.0 V	0.40	2.8	3.0	3.3	ns
	T_{OPCI66_3}	PCI, 66 MHz, 3.3 V	0.10	-0.40	-0.42	-0.46	ns
	T_{OGTL}	GTL	0.6	0.50	0.54	0.6	ns
	T_{OGTLP}	GTL+	0.7	0.8	0.9	1.0	ns
	T_{OHSTL_I}	HSTL I	0.10	-0.50	-0.53	-0.5	ns
	T_{OHSTL_III}	HSTL III	-0.10	-0.9	-0.9	-1.0	ns
	T_{OHSTL_IV}	HSTL IV	-0.20	-1.0	-1.0	-1.1	ns
	T_{OSSTL2_I}	SSTL2 I	-0.10	-0.50	-0.53	-0.5	ns
	T_{OSSLT2_II}	SSTL2 II	-0.20	-0.9	-0.9	-1.0	ns
	T_{OSSTL3_I}	SSTL3 I	-0.20	-0.50	-0.53	-0.5	ns
	T_{OSSTL3_II}	SSTL3 II	-0.30	-1.0	-1.0	-1.1	ns
	T_{OCTT}	CTT	0	-0.6	-0.6	-0.6	ns
	T_{OAGP}	AGP	0	-0.9	-0.9	-1.0	ns

Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 14 and Table 16.

Calculation of T_{ioop} as a Function of Capacitance

T_{ioop} is the propagation delay from the O Input of the IOB to the pad. The values for T_{ioop} were based on the standard capacitive load (Csl) for each IO standard as listed in Table 14.

For other capacitive loads, use the formulas below to calculate the corresponding T_{ioop}.

$$T_{ioop} = T_{ioop} + T_{opadjust} + (C_{load} - C_{sl}) * fl$$

Where:

$T_{opadjust}$ is reported above in the Output Delay Adjustment section.

C_{load} is the capacitive load for the design.

Table 14: Constants for Calculating T_{ioop}

Standard	Csl (pF)	fl (ns/pF)
LVTTL Fast Slew Rate, 2mA drive	35	0.41
LVTTL Fast Slew Rate, 4mA drive	35	0.20
LVTTL Fast Slew Rate, 6mA drive	35	0.13
LVTTL Fast Slew Rate, 8mA drive	35	0.079
LVTTL Fast Slew Rate, 12mA drive	35	0.044
LVTTL Fast Slew Rate, 16mA drive	35	0.043
LVTTL Fast Slew Rate, 24mA drive	35	0.033
LVTTL Slow Slew Rate, 2mA drive	35	0.41
LVTTL Slow Slew Rate, 4mA drive	35	0.20
LVTTL Slow Slew Rate, 6mA drive	35	0.100
LVTTL Slow Slew Rate, 8mA drive	35	0.086
LVTTL Slow Slew Rate, 12mA drive	35	0.058
LVTTL Slow Slew Rate, 16mA drive	35	0.050
LVTTL Slow Slew Rate, 24mA drive	35	0.048
LVCMOS2	35	0.041
PCI 33MHz 5V	50	0.050
PCI 33MHZ 3.3 V	10	0.050
PCI 66 MHz 3.3 V	10	0.033
GTL	0	0.014
GTL+	0	0.017
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037

Note 1: IO parameter measurements are made with the capacitance values shown above. See Xilinx application note XAPP133 for appropriate terminations.
Note 2: IO standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Table 15: Delay Measurement Methodology

Standard	V_L[1]	V_H[1]	Meas. Point	V_{REF} (Typ)[2]
LVTTL	0	3	1.4	-
LVCMOS2	0	2.5	1.125	-
PCI33_5	Per PCI Spec			-
PCI33_3	Per PCI Spec			-
PCI66_3	Per PCI Spec			-
GTL	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	0.80
GTL+	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	1.0
HSTL Class I	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.75
HSTL Class III	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.90
HSTL Class IV	V_{REF} -0.5	V_{REF} +0.5	V_{REF}	0.90
SSTL3 I & II	V_{REF} -1.0	V_{REF} +1.0	V_{REF}	1.5
SSTL2 I & II	V_{REF} -0.75	V_{REF} +0.75	V_{REF}	1.25
CTT	V_{REF} -0.2	V_{REF} +0.2	V_{REF}	1.5
AGP	V_{REF} - ($0.2xV_{CCO}$)	V_{REF} + ($0.2xV_{CCO}$)	V_{REF}	Per AGP Spec

Note 1: Input waveform switches between V_L and V_H.
Note 2: Measurements are made at VREF (Typ), Maximum, and Minimum. Worst-case values are reported.
Note 3: IO parameter measurements are made with the capacitance values shown in Table 14. See Xilinx application note XAPP133 for appropriate terminations.
Note 4: IO standard measurements are reflected in the IBIS model information except where the IBIS format precludes it.

Clock Distribution Guidelines

Description	Device	Symbol	Speed Grade -6	Speed Grade -5	Speed Grade -4	Units
Global Clock Skew						
Global Clock Skew between IOB Flip-flops	XCV50	$T_{GSKEWIOB}$	0.10	0.12	0.14	ns, max
	XCV100		0.12	0.13	0.15	ns, max
	XCV150		0.12	0.13	0.15	ns, max
	XCV200		0.13	0.14	0.16	ns, max
	XCV300		0.14	0.16	0.18	ns, max
	XCV400		0.13	0.13	0.14	ns, max
	XCV600		0.14	0.15	0.17	ns, max
	XCV800		0.16	0.17	0.20	ns, max
	XCV1000		0.20	0.23	0.25	ns, max

Note: These clock-skew delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.

Clock Distribution Switching Characteristics

Description	Speed Grade / Symbol	All Min	-6	-5	-4	Units
GCLK IOB and Buffer						
Global Clock PAD to output.	T_{GPIO}	0.33	0.7	0.8	0.9	ns, max
Global Clock Buffer I input to O output	T_{GIO}	0.34	0.7	0.8	0.9	ns, max

CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

	Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Min**				
Combinatorial Delays						
4-input function: F/G inputs to X/Y outputs	T_{ILO}	0.29	0.6	0.7	0.8	ns, max
5-input function: F/G inputs to F5 output	T_{IF5}	0.32	0.7	0.8	0.9	ns, max
5-input function: F/G inputs to X output	T_{IF5X}	0.36	0.8	0.8	1.0	ns, max
6-input function: F/G inputs to Y output via F6 MUX	T_{IF6Y}	0.44	0.9	1.0	1.2	ns, max
6-input function: F5IN input to Y output	T_{F5INY}	0.17	0.32	0.36	0.42	ns, max
Incremental delay routing through transparent latch to XQ/YQ outputs	T_{IFNCTL}	0.31	0.7	0.7	0.8	ns, max
BY input to YB output	T_{BYYB}	0.27	0.53	0.6	0.7	ns, max
Sequential Delays						
FF Clock CLK to XQ/YQ outputs	T_{CKO}	0.54	1.1	1.2	1.4	ns, max
Latch Clock CLK to XQ/YQ outputs	T_{CKLO}	0.6	1.2	1.4	1.6	ns, max
Setup and Hold Times before/after Clock CLK	Setup Time / Hold Time					
4-input function: F/G Inputs	T_{ICK}/T_{CKI}	0.6 / 0	1.2 / 0	1.4 / 0	1.5 / 0	ns, min
5-input function: F/G inputs	T_{IF5CK}/T_{CKIF5}	0.7 / 0	1.3 / 0	1.5 / 0	1.7 / 0	ns, min
6-input function: F5IN input	T_{F5INCK}/T_{CKF5IN}	0.46 / 0	1.0 / 0	1.1 / 0	1.2 / 0	ns, min
6-input function: F/G inputs via F6 MUX	T_{IF6CK}/T_{CKIF6}	0.8 / 0	1.5 / 0	1.7 / 0	1.9 / 0	ns, min
BX/BY inputs	T_{DICK}/T_{CKDI}	0.30 / 0	0.6 / 0	0.7 / 0	0.8 / 0	ns, min
CE input	T_{CECK}/T_{CKCE}	0.37 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
SR/BY inputs (synchronous)	$T_{RCK}T_{CKR}$	0.33 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{CH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{CL}	0.8	1.5	1.7	2.0	ns, min
Set/Reset						
Minimum Pulse Width, SR/BY inputs	T_{RPW}	1.3	2.5	2.8	3.3	ns, min
Delay from SR/BY inputs to XQ/YQ outputs (asynchronous)	T_{RQ}	0.54	1.1	1.3	1.4	ns, max
Delay from GSR to XQ/YQ outputs	T_{IOGSRQ}	4.9	9.7	10.9	12.5	ns, max
Toggle Frequency (MHz) (for export control)	F_{TOG} (MHz)	625	333	294	250	MHz

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

	Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Min**				
Combinatorial Delays						
F operand inputs to X via XOR	T_{OPX}	0.37	0.8	0.9	1.0	ns, max
F operand input to XB output	T_{OPXB}	0.54	1.1	1.3	1.4	ns, max
F operand input to Y via XOR	T_{OPY}	0.8	1.5	1.7	2.0	ns, max
F operand input to YB output	T_{OPYB}	0.8	1.5	1.7	2.0	ns, max
F operand input to COUT output	T_{OPCYF}	0.6	1.2	1.3	1.5	ns, max
G operand inputs to Y via XOR	T_{OPGY}	0.46	1.0	1.1	1.2	ns, max
G operand input to YB output	T_{OPGYB}	0.8	1.6	1.8	2.1	ns, max
G operand input to COUT output	T_{OPCYG}	0.7	1.3	1.4	1.6	ns, max
BX initialization input to COUT	T_{BXCY}	0.41	0.9	1.0	1.1	ns, max
CIN input to X output via XOR	T_{CINX}	0.21	0.41	0.46	0.53	ns, max
CIN input to XB	T_{CINXB}	0.02	0.04	0.05	0.06	ns, max
CIN input to Y via XOR	T_{CINY}	0.23	0.46	0.52	0.6	ns, max
CIN input to YB	T_{CINYB}	0.23	0.45	0.51	0.6	ns, max
CIN input to COUT output	T_{BYP}	0.05	0.09	0.10	0.11	ns, max
Multiplier Operation						
F1/2 operand inputs to XB output via AND	T_{FANDXB}	0.18	0.36	0.40	0.46	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}	0.40	0.8	0.9	1.1	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}	0.22	0.43	0.48	0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}	0.25	0.50	0.6	0.7	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}	0.07	0.13	0.15	0.17	ns, max
Setup and Hold Times before/after Clock CLK	Setup Time / Hold Time					
CIN input to FFX	T_{CCKX}/T_{CKCX}	0.50 / 0	1.0 / 0	1.2 / 0	1.3 / 0	ns, min
CIN input to FFY	T_{CCKY}/T_{CKCY}	0.53 / 0	1.1 / 0	1.2 / 0	1.4 / 0	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

CLB SelectRAM Switching Characteristics

Description	Symbol	All Min	-6	-5	-4	Units
Sequential Delays						
Clock CLK to X/Y outputs (WE active)	T_{SHCKO}	1.2	2.3	2.6	3.0	ns, max
Shift-Register Mode Clock CLK to X/Y outputs		1.2	2.3	2.6	3.0	ns, max
Setup and Hold Times before/after Clock CLK	Setup Time / Hold Time					
F/G address inputs	T_{AS}/T_{AH}	0.25 / 0	0.5 / 0	0.6 / 0	0.7 / 0	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}	0.34 / 0	0.7 / 0	0.8 / 0	0.9 / 0	ns, min
CE input (WE)	T_{WS}/T_{WH}	0.38 / 0	0.8 / 0	0.9 / 0	1.0 / 0	ns, min
Shift-Register Mode						
BX/BY data inputs (DIN)	T_{SHDICK}	0.34	0.7	0.8	0.9	ns, min
CE input (WS)	T_{SHCECK}	0.38	0.8	0.9	1.0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{WPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{WPL}	1.2	2.4	2.7	3.1	ns, min
Minimum clock period to meet address write cycle time	T_{WC}	2.4	4.8	5.4	6.2	ns, min
Shift-Register Mode						
Minimum Pulse Width, High	T_{SRPH}	1.2	2.4	2.7	3.1	ns, min
Minimum Pulse Width, Low	T_{SRPL}	1.2	2.4	2.7	3.1	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Block RAM Switching Characteristics

Description	Symbol	All Min	-6	-5	-4	Units
Sequential Delays						
Clock CLK to DOUT output	T_{BCKO}	1.7	3.4	3.8	4.3	ns, max
Setup and Hold Times before/after Clock CLK	Setup Time / Hold Time					
ADDR inputs	T_{BACK}/T_{BCKA}	0.6 / 0	1.2 / 0	1.3 / 0	1.5 / 0	ns, min
DIN inputs	T_{BDCK}/T_{BCKD}	0.6 / 0	1.2 / 0	1.3 / 0	1.5 / 0	ns, min
EN input	T_{BECK}/T_{BCKE}	1.3 / 0	2.6 / 0	3.0 / 0	3.4 / 0	ns, min
RST input	T_{BRCK}/T_{BCKR}	1.3 / 0	2.5 / 0	2.7 / 0	3.2 / 0	ns, min
WEN input	T_{BWCK}/T_{BCKW}	1.2 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
Clock CLK						
Minimum Pulse Width, High	T_{BPWH}	0.8	1.5	1.7	2.0	ns, min
Minimum Pulse Width, Low	T_{BPWL}	0.8	1.5	1.7	2.0	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}		3.0	3.5	4.0	ns, min

Note: A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

TBUF Switching Characteristics

	Speed Grade	All	-6	-5	-4	
Description	**Symbol**	**Min**				**Units**
Combinatorial Delays						
IN input to OUT output	T_{IO}	0	0	0	0	ns, max
TRI input to OUT output high-impedance	T_{OFF}	0.05	0.09	0.10	0.11	ns, max
TRI input to valid data on OUT output	T_{ON}	0.05	0.09	0.10	0.11	ns, max

JTAG Test Access Port Switching Characteristics

		Speed Grade			
Description	**Symbol**	**-6**	**-5**	**-4**	**Units**
TMS and TDI Setup times before TCK	T_{TAPTCK}	4.0	4.0	4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}	2.0	2.0	2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}	11.0	11.0	11.0	ns, max
Maximum TCK clock frequency	F_{TCK}	33	33	33	MHz, max

Virtex Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *with* DLL

		Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Device**	**Min**				
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *with* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments.	$T_{ICKOFDLL}$	XCV50	1.0	3.1	3.3	3.6	ns, max
		XCV100	1.0	3.1	3.3	3.6	ns, max
		XCV150	1.0	3.1	3.3	3.6	ns, max
		XCV200	1.0	3.1	3.3	3.6	ns, max
		XCV300	1.0	3.1	3.3	3.6	ns, max
		XCV400	1.0	3.1	3.3	3.6	ns, max
		XCV600	1.0	3.1	3.3	3.6	ns, max
		XCV800	1.0	3.1	3.3	3.6	ns, max
		XCV1000	1.0	3.1	3.3	3.6	ns, max

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 14 and Table 16.
DLL output jitter is already included in the timing calculation.

Global Clock Input to Output Delay for LVTTL, 12 mA, Fast Slew Rate, *without* DLL

		Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Device**	**Min**				
LVTTL Global Clock Input to Output Delay using Output Flip-flop, 12 mA, Fast Slew Rate, *without* DLL. For data *output* with different standards, adjust delays with the values shown in Output Delay Adjustments.	T_{ICKOF}	XCV50	1.5	4.6	5.1	5.7	ns, max
		XCV100	1.5	4.6	5.1	5.7	ns, max
		XCV150	1.5	4.7	5.2	5.8	ns, max
		XCV200	1.5	4.7	5.2	5.8	ns, max
		XCV300	1.5	4.7	5.2	5.9	ns, max
		XCV400	1.5	4.8	5.3	6.0	ns, max
		XCV600	1.6	4.9	5.4	6.0	ns, max
		XCV800	1.6	4.9	5.5	6.2	ns, max
		XCV1000	1.7	5.0	5.6	6.3	ns, max

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Output timing is measured at 1.4 V with 35 pF external capacitive load for LVTTL. For other I/O standards and different loads, see Table 14 and Table 16.

Minimum Clock to Out for Virtex Devices

I/O Standard	With DLL	Without DLL								
	All Devices	V50	V100	V150	V200	V300	V600	V800	V1000	Units
*LVTTL_S2	5.2	6.0	6.0	6.0	6.0	6.1	6.1	6.1	6.1	ns
*LVTTL_S4	3.5	4.3	4.3	4.3	4.3	4.4	4.4	4.4	4.4	ns
*LVTTL_S6	2.8	3.6	3.6	3.6	3.6	3.7	3.7	3.7	3.7	ns
*LVTTL_S8	2.2	3.1	3.1	3.1	3.1	3.1	3.2	3.2	3.2	ns
*LVTTL_S12	2.0	2.9	2.9	2.9	2.9	2.9	3.0	3.0	3.0	ns
*LVTTL_S16	1.9	2.8	2.8	2.8	2.8	2.8	2.9	2.9	2.9	ns
*LVTTL_S24	1.8	2.6	2.6	2.7	2.7	2.7	2.7	2.7	2.8	ns
*LVTTL_F2	2.9	3.8	3.8	3.8	3.8	3.8	3.9	3.9	3.9	ns
*LVTTL_F4	1.7	2.6	2.6	2.6	2.6	2.6	2.7	2.7	2.7	ns
*LVTTL_F6	1.2	2.0	2.0	2.0	2.1	2.1	2.1	2.1	2.2	ns
*LVTTL_F8	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	ns
*LVTTL_F12	1.0	1.8	1.8	1.8	1.8	1.9	1.9	1.9	1.9	ns
*LVTTL_F16	0.9	1.7	1.8	1.8	1.8	1.8	1.8	1.9	1.9	ns
*LVTTL_F24	0.9	1.7	1.7	1.7	1.8	1.8	1.8	1.8	1.9	ns
LVCMOS2	1.1	1.9	1.9	1.9	2.0	2.0	2.0	2.0	2.1	ns
PCI33_3	1.5	2.4	2.4	2.4	2.4	2.4	2.5	2.5	2.5	ns
PCI33_5	1.4	2.2	2.2	2.3	2.3	2.3	2.3	2.3	2.4	ns
PCI66_3	1.1	1.9	1.9	2.0	2.0	2.0	2.0	2.1	2.1	ns
GTL	1.6	2.5	2.5	2.5	2.5	2.5	2.6	2.6	2.6	ns
GTL+	1.7	2.5	2.5	2.6	2.6	2.6	2.6	2.6	2.7	ns
HSTL I	1.1	1.9	1.9	1.9	1.9	2.0	2.0	2.0	2.0	ns
HSTL III	0.9	1.7	1.7	1.8	1.8	1.8	1.8	1.8	1.9	ns
HSTL IV	0.8	1.6	1.6	1.6	1.7	1.7	1.7	1.7	1.8	ns
SSTL2 I	0.9	1.7	1.7	1.7	1.7	1.8	1.8	1.8	1.8	ns
SSTL2 II	0.8	1.6	1.6	1.6	1.6	1.7	1.7	1.7	1.7	ns
SSTL3 I	0.8	1.6	1.7	1.7	1.7	1.7	1.7	1.8	1.8	ns
SSTL3 II	0.7	1.5	1.5	1.6	1.6	1.6	1.6	1.6	1.7	ns
CTT	1.0	1.8	1.8	1.8	1.9	1.9	1.9	1.9	2.0	ns
AGP	1.0	1.8	1.8	1.9	1.9	1.9	1.9	1.9	2.0	ns

*S = Slow Slew Rate, F = Fast Slew Rate

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Input and output timing is measured at 1.4 V for LVTTL. For other I/O standards, see Table 16. In all cases, an 8 pF external capacitive load is used.

Virtex Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Listed below are representative values for typical pin locations and normal clock loading. Values are expressed in nanoseconds unless otherwise noted

Global Clock Set-Up and Hold for LVTTL Standard, *with* DLL

		Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Device**	**Min**				
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
No Delay Global Clock and IFF, with DLL	T_{PSDLL}/T_{PHDLL}	XCV50	0.40 / 0	1.7 / 0	1.8 / 0	2.1 / 0	ns, min
		XCV100	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV150	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV200	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV300	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV400	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV600	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV800	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min
		XCV1000	0.40 / 0	1.7 / 0	1.9 / 0	2.1 / 0	ns, min

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

DLL output jitter is already included in the timing calculation.

A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

Global Clock Set-Up and Hold for LVTTL Standard, *without* DLL

		Speed Grade	All	-6	-5	-4	Units
Description	**Symbol**	**Device**	**Min**				
Input Setup and Hold Time Relative to Global Clock Input Signal for LVTTL Standard. For data input with different standards, adjust the setup time delay by the values shown in Input Delay Adjustments.							
Full Delay Global Clock and IFF, without DLL	T_{PSFD}/T_{PHFD}	XCV50	0.6 / 0	2.3 / 0	2.6 / 0	2.9 / 0	ns, min
		XCV100	0.6 / 0	2.3 / 0	2.6 / 0	3.0 / 0	ns, min
		XCV150	0.6 / 0	2.4 / 0	2.7 / 0	3.1 / 0	ns, min
		XCV200	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV300	0.7 / 0	2.5 / 0	2.8 / 0	3.2 / 0	ns, min
		XCV400	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV600	0.7 / 0	2.6 / 0	2.9 / 0	3.3 / 0	ns, min
		XCV800	0.7 / 0	2.7 / 0	3.1 / 0	3.5 / 0	ns, min
		XCV1000	0.7 / 0	2.8 / 0	3.1 / 0	3.6 / 0	ns, min

IFF = Input Flip-Flop or Latch

Notes: Setup time is measured relative to the Global Clock input signal with the fastest route and the lightest load. Hold time is measured relative to the Global Clock input signal with the slowest route and heaviest load.

A Zero “0” Hold Time listing indicates no hold time or a negative hold time. Negative values can not be guaranteed “best-case”, but if a “0” is listed, there is no positive hold time.

DLL Timing Parameters

Switching parameters testing is modeled after testing methods specified by MIL-M-38510/605; all devices are 100 percent functionally tested. Because of the difficulty in directly measuring many internal timing parameters, those parameters are derived from benchmark timing patterns. The following guidelines reflect worst-case values across the recommended operating conditions.

	Speed Grade	-4		-5		-6		
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Frequency (CLKDLLHF)	$F_{CLKINHF}$	60	180	60	180	60	200	MHz
Input Clock Frequency (CLKDLL)	$F_{CLKINLF}$	25	90	25	90	25	100	MHz
Input Clock Pulse Width (CLKDLLHF)	$T_{DLLPWHF}$	2.4	-	2.4	-	2.0	-	ns
Input Clock Pulse Width (CLKDLL)	$T_{DLLPWLF}$	3.0	-	3.0		2.5	-	ns

Note: All specifications correspond to Commercial Operating Temperatures (0°C to + 85°C).

3

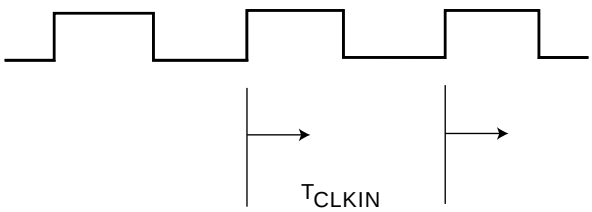
DLL Clock Tolerance, Jitter, and Phase Information

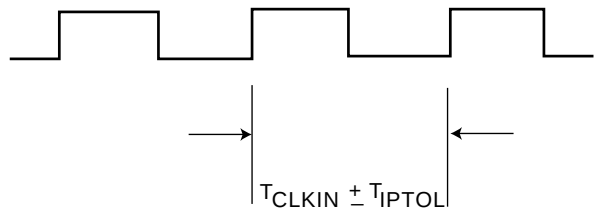
All DLL output jitter and phase specifications determined through statistical measurement at the package pins using a clock mirror configuration and matched drivers.

			CLKDLLHF		CLKDLL		
Description	**Symbol**	**F_{CLKIN}**	**Min**	**Max**	**Min**	**Max**	**Units**
Input Clock Period Tolerance	T_{IPTOL}		-	1.0	-	1.0	ns
Input Clock Jitter Tolerance (Cycle to Cycle)	T_{IJITCC}		-	± 150	-	± 300	ps
Time Required for DLL to Acquire Lock	T_{LOCK}	> 60 MHz	-	20	-	20	µs
		50 - 60 MHz	-	-	-	25	µs
		40 - 50 MHz	-	-	-	50	µs
		30 - 40 MHz	-	-	-	90	µs
		25 - 30 MHz	-	-	-	120	µs
Output Jitter (cycle-to-cycle) for any DLL Clock Output[1]	T_{OJITCC}			± 60		± 60	ps
Phase Offset between CLKIN and CLKO[2]	T_{PHIO}			± 100		± 100	ps
Phase Offset between Clock Outputs on the DLL[3]	T_{PHOO}			± 140		± 140	ps
Maximum Phase Difference between CLKIN and CLKO[4]	T_{PHIOM}			± 160		± 160	ps
Maximum Phase Difference between Clock Outputs on the DLL[5]	T_{PHOOM}			± 200		± 200	ps

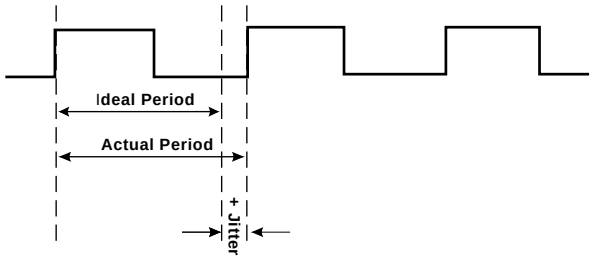
Note 1: **Output Jitter** is cycle-to-cycle jitter measured on the DLL output clock, *excluding* input clock jitter.
Note 2: **Phase Offset between CLKIN and CLKO** is the worst-case fixed time difference between rising edges of CLKIN and CLKO, *excluding* Output Jitter and input clock jitter.
Note 3: **Phase Offset between Clock Outputs on the DLL** is the worst-case fixed time difference between rising edges of any two DLL outputs, *excluding* Output Jitter and input clock jitter.
Note 4: **Maximum Phase Difference between CLKIN an CLKO** is the sum of Output Jitter and Phase Offset between CLKIN and CLKO, or the greatest difference between CLKIN and CLKO rising edges due to DLL alone (*excluding* input clock jitter).
Note 5: **Maximum Phase DIfference between Clock Outputs on the DLL** is the sum of Output JItter and Phase Offset between any DLL clock outputs, or the greatest difference between any two DLL output rising edges sue to DLL alone (*excluding* input clock jitter).
Note 6: All specifications correspond to Commercial Operating Temperatures (0°C to +85°C).

Period Tolerance: the allowed input clock period change in nanoseconds.





Output Jitter: the difference between an ideal reference clock edge and the actual design.



Phase Offset and Maximum Phase Difference

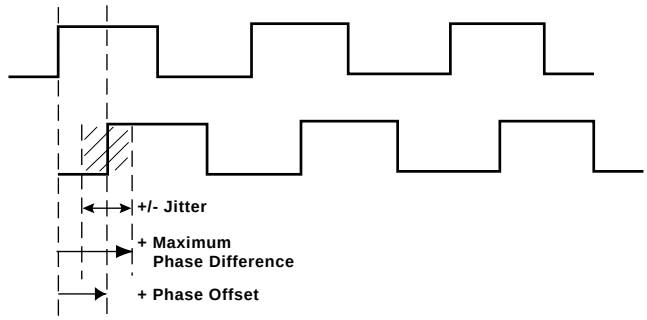


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Figure 20: Frequency Tolerance and Clock Jitter

Virtex Pin Definitions

Table 16: Special Purpose Pins

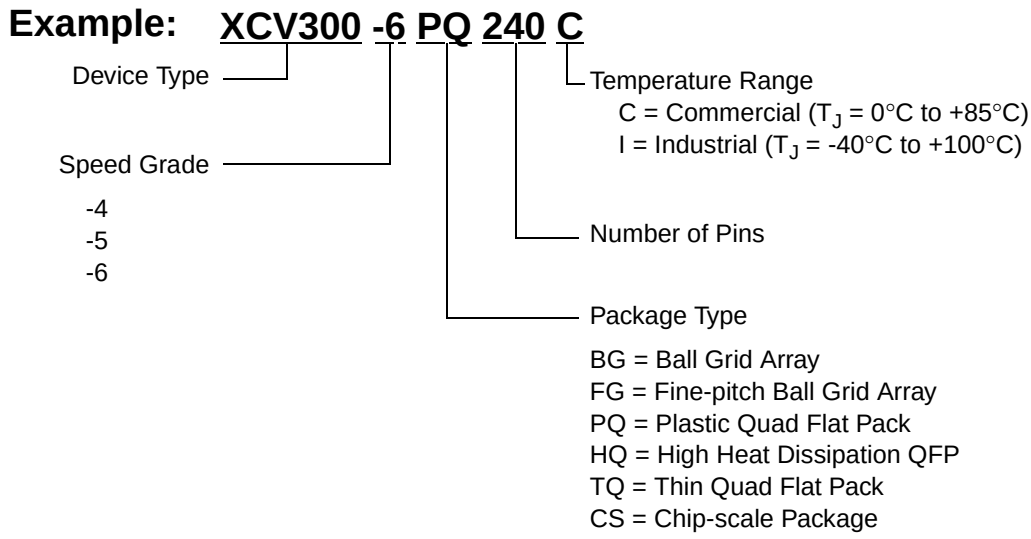
Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectMAP and slave-serial modes, and output in master-serial mode. After configuration, it is input only, logic level = "Don't Care".
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In SelectMAP mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the SelectMAP port is retained. In bit-serial modes, DOUT provides header information to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input or Output	In SelectMAP mode, D0-7 are configuration data pins. These pins become user I/Os after configuration unless the SelectMAP port is retained. In bit-serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In SelectMAP mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
$\overline{\text{CS}}$	No	Input	In SelectMAP mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the SelectMAP port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins, as defined in IEEE 1149.1.
DXN, DXP	Yes	N/A	Temperature-sensing diode pins. (Anode: DXP, cathode: DXN)
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for the output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground

For a complete Virtex data sheet including package pinouts, go to the CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Virtex Device/Package Combinations and Maximum I/O

Package	Maximum User I/O (excluding dedicated clock pins)								
	XCV50	XCV100	XCV150	XCV200	XCV300	XCV400	XCV600	XCV800	XCV1000
CS144	94	94							
TQ144	98	98							
PQ240	166	166	166	166	166				
HQ240						166	166	166	
BG256	180	180	180	180					
BG352			260	260	260				
BG432					316	316	316	316	
BG560						404	404	404	404
FG256	176	176	176	176					
FG456			260	284	312				
FG676						404	444	444	
FG680							512	512	512

Virtex Ordering Information



Revision History

Version	Description
1.0 (11/98)	Initial document release.
1.2 (1/99)	Updated package drawings and specs.
1.3 (2/99)	Update of package drawings, updated specifications.
1.4 (5/99)	Addition of package drawings and specifications.
1.5 (5/99)	Replaced FG 676 & FG680 package drawings.
1.6 (7/99)	Changed Boundary Scan Information and changed Figure 11, Boundary Scan Bit Sequence. Updated IOB Input & Output delays. Added Capacitance info for different IO Standards. Added 5 V tolerant information. Added DLL Parameters and waveforms and new Pin-to-pin Input and Output Parameter tables for Global Clock Input to Output and Setup and Hold. Changed Configuration Information including Figures 12, 14, 17 & 19. Added device-dependent listings for quiescent currents ICCINTQ and ICCOQ. Updated IOB Input and Output Delays based on default standard of LVTTL, 12 mA, Fast Slew Rate. Added IOB Input Switching Characteristics Standard Adjustments.
1.7 (9/99)	Speed grade update to preliminary status, Power-on specification and Clock-to-Out Minimums additions, “0” hold time listing explanation, quiescent current listing update, and Figure 6 ADDRA input label correction. Added T_{IJITCC} parameter, changed T_{OJIT} to T_{OPHASE}.
1.8 (1/2000)	Update to speed.txt file 1.96. Corrections for CRs 111036,111137, 112697, 115479, 117153, 117154, and 117612. Modified notes for Recommended Operating Conditions (voltage and temperature). Changed Bank information for V_{CCO} in CS144 package on page 43.
1.9 (1/2000)	Updated DLL Jitter Parameter table and waveforms, added Delay Measurement Methodology table for different I/O standards, changed buffered Hex line info and Input/Output Timing measurement notes.

Spartan Products Table of Contents

Spartan-II 2.5V Family Field Programmable Gate Arrays

For a complete data sheet, go to CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Spartan and Spartan-XL Families Field Programmable Gate Arrays

For a complete data sheet, go to CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Spartan-II 2.5V Family Field Programmable Gate Arrays

DS001 (v0.9) March 3, 2000 - **Advance Product Specification**

Introduction

The Spartan™-II family is the second generation high-volume production FPGA solution, based on the highly successful Virtex™ family architecture. The family delivers all the key requirements for ASIC replacement with up to 150,000 gates and 200 MHz system performance at 2.5V logic supply. These requirements include high performance, on-chip RAM, Core Solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan-II family is the result of more than fifteen years of FPGA design experience and feedback from thousands of customers. By streamlining the Virtex family feature set, leveraging advanced hybrid process technologies and focusing on total cost management, the Spartan-II family delivers the key features required by ASIC and other high volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs. The Spartan-II family currently has five members, as shown in Table 1.

Features

- Second generation ASIC replacement technology
  - On-chip RAM (block and distributed)
  - Power down mode (I_{CCO} = 100 µA)
  - Density up to 3,888 logic cells or 150,000 system gates
  - Hot-swappable for Compact PCI
  - Advanced 0.22/0.18 µm 6-layer metal process
  - Streamlined feature set based on Virtex architecture
  - Unlimited reprogrammability
  - Very Low cost
- System level features
  - Two types of On-chip SelectRAM™ memory, distributed and block
  - Fully PCI compliant
  - Low power segmented routing architecture
  - Full readback capability for program verification and internal node observability
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
  - IEEE 1149.1-compatible boundary scan logic
- Versatile I/O and packaging
  - Low cost packages available in all densities
  - Family footprint compatibility in common packages
  - 16 high-performance interface standards
  - Zero input register hold time simplifies system timing
- Fully supported by powerful Xilinx development system
  - Foundation series: Integrated, shrink-wrap software
  - Alliance series: Over 100 PC and workstation thrid party development systems supported
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization

.

Table 1: Spartan-II Field-Programmable Gate Array Family Members.

Device	Logic Cells	Typical System Gate Range (Logic and RAM)	CLB Array	Total CLBs	Maximum Available User I/O	Total BlockRam Blocks	Total BlockRAM Bits
XC2S15	432	6,000 - 15,000	8x12	96	86	4	16,384
XC2S30	972	13,000 - 30,000	12x18	216	132	6	24,576
XC2S50	1,728	23,000 - 50,000	16x24	384	176	8	32,768
XC2S100	2,700	37,000 - 100,000	20x30	600	196	10	40,960
XC2S150	3,888	52,000 - 150,000	24x36	864	260	12	49,152

General Overview

Spartan-II family of FPGAs is implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), surrounded by a perimeter of programmable Input/Output Blocks (IOBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels) also providing advanced functions such as Block RAM and DLL clock control blocks. (see Figure 1.)

The devices are customized by loading configuration data into internal static memory cells. Unlimited Re-programming cycles are possible with this approach. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can be programmed in one of three modes. The traditional Master Serial mode, Slave Serial mode, or Slave Parallel mode.

Spartan-II family FPGAs are typically used in high volume, applications where the versatilely of a fast programmable solution will add benefits. Spartan-II family FPGAs are ideal for shortening design and development cycles, and at the same time offer a cost-effective solution where product production volumes require 50,000 to well over 1,000,000 devices per year.

Spartan-II family devices achieve high-performance, low cost operation through the use of an advanced architecture and semiconductor technology. Spartan-II devices provide system clock rates exceeding 200 MHz and internal performance in excess of 350 MHz. In contrast to other FPGA devices, Spartan-II FPGAs offer the most cost effective solution while maintaining leading edge performance. In addition to the conventional benefit of high volume programmable logic solutions Spartan FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, block RAM, DLL clock drivers programmable set and reset on all flip-flops, fast carry logic, and many other features.

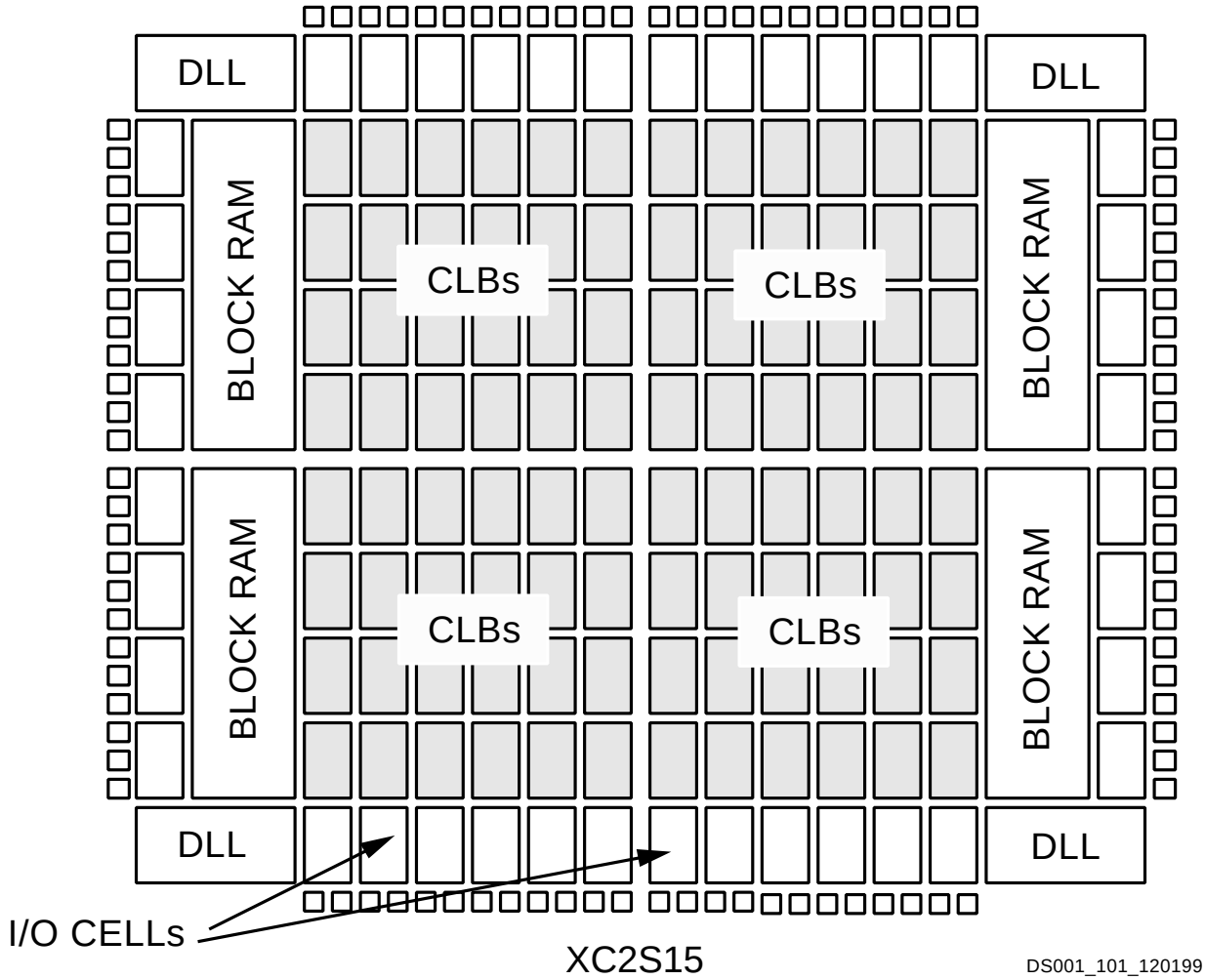


Figure 1: Basic Spartan-II Family FPGA Block

Architectural Description

Spartan-II Array

The Spartan-II user-programmable gate array, shown in Figure 1, is composed of five major configurable elements:

- IOBs provide the interface between the package pins and the internal logic
- CLBs provide the functional elements for constructing most logic
- Dedicated block RAM memories of 4096 bits each
- Clock DLLs for clock-distribution delay compensation and clock domain control
- Versital Multi-Level Interconnect structure

As you can see in the figure, the CLBs form the central logic structure with easy access to all support and routing strucures. The IOBs are located around all the logic and memory elements for easy and quick routing of signals on and off the chip.

Values stored in static memory cells control all the configurable logic elements and interconnect resources. These values load into the memory cells on power-up, and can reload if necessary to change the function of the device.

Each of these elements will be desicussed in detail in the following discussions.

Input/Output Block

The Spartan-II IOB, as seen in Figure 2, features inputs and outputs that support a wide variety of I/O signalling standards. These high-speed inputs and outputs are capable of supporting various state of the art memory and buss interfaces. Table 2 lists several of the standards which are supported along with the required refrence, output & termination voltages needed to meet the standard.

The three IOB registers function either as edge-triggered D-type flip-flops or as level sensitive latches. Each IOB has a clock signal (CLK) shared by the three registers and independent clock enable signals for each registers.

In addition to the CLK and CE control signals, the three registers share a Set/Reset (SR). For each registers, this signal can be independently configured as a synchronous Set, a synchronous Reset, an asynchronous Preset, or an asynchronous Clear.

A feature not shown in the block diagram, but controllable by the software is polarity control. The input and output buffers and all of the IOB control signals have independent polarity controls.

Optional pull-up and pull-down resistors and an optional weak-keeper circuit are attached to each pad. Prior to configuration all outputs not involved in configuration are forced

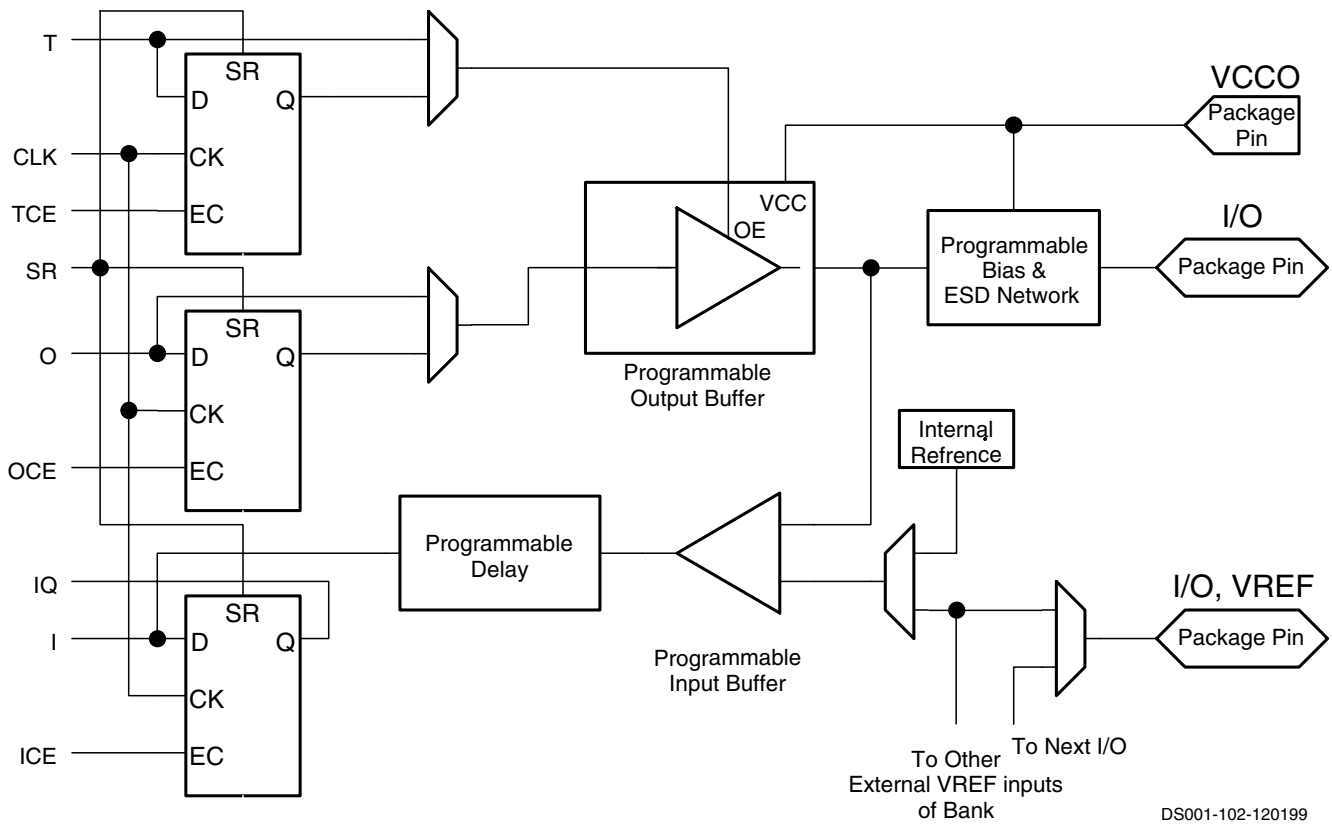


Figure 2: Spartan-II Input/Output Block (IOB)

into their high-impedance state. The pull-down resistors and the weak-keeper circuits are inactive, but inputs may optionally be pulled up.

Table 2: Supported I/O Standards

I/O Standard	Input Reference Voltage (V_{REF})	Output Source Voltage (V_{CCO})	Board Termination Voltage (V_{TT})
LVTTL 2 to 24 mA	N/A	3.3	N/A
LVCMOS2	N/A	2.5	N/A
PCI	N/A	3.3	N/A
GTL	0.8	N/A	1.2
GTL+	1.0	N/A	1.5
HSTL Class I	0.75	1.5	1.5
HSTL Class III	0.75	1.5	1.5
HSTL Class IV	0.75	1.5	1.5
SSTL3 Class I and II	1.5	3.3	1.5
SSTL2 Class I and II	1.25	2.5	1.25
CTT	1.5	3.3	1.5
AGP	1.32	3.3	N/A

The activation of pull-up resistors prior to configuration is controlled on a global basis by the configuration mode pins. If the pull-up resistors are not activated, all the pins will float. Consequently, external pull-up or pull-down resistors must be provided on pins required to be at a well-defined logic level prior to configuration.

All pads are protected against damage from electrostatic discharge (ESD) and from over-voltage transients. Two forms of over-voltage protection are provided, one that permits 5V compliance, and one that does not. For 5V compliance, a zener-like structure connected to ground turns on when the output rises to approximately 6.5V. When 5V compliance is not required, a conventional clamp diode may be connected to the output supply voltage, V_{CCO}. The type of over-voltage protection can be selected independently for each pad.

All Spartan-II IOBs support IEEE 1149.1-compatible boundary scan testing.

Input Path

A buffer In the Spartan-II IOB input path routes the input signal either directly to internal logic or through an optional input flip-flop.

An optional delay element at the D-input of this flip-flop eliminates pad-to-pad hold time. The delay is matched to the internal clock-distribution delay of the FPGA, and when used, assures that the pad-to-pad hold time is zero.

Each input buffer can be configured to conform to any of the low-voltage signalling standards supported. In some of these standards the input buffer utilizes a user-supplied threshold voltage, V_{REF}. The need to supply V_{REF} imposes constraints on which standards can used in close proximity to each other. See “I/O Banking” on page 9.

There are optional pull-up and pull-down resistors at each input for use after configuration. Their value is in the range 50 to 150 kohms.

Output Path

The output path includes a 3-state output buffer that drives the output signal onto the pad. The output signal can be routed to the buffer directly from the internal logic or through an optional IOB output flip-flop.

The 3-state control of the output can also be routed directly from the internal logic or through a flip-flip that provides synchronous enable and disable.

Each output driver can be individually programmed for a wide range of low-voltage signalling standards. Each output buffer can source up to 24 mA and sink up to 48 mA. Drive strength and slew rate controls minimize bus transients.

In most signalling standards, the output High voltage depends on an externally supplied V_{CCO} voltage. The need to supply V_{CCO} imposes constraints on which standards can be used in close proximity to each other. See “I/O Banking” on page 9.

An optional weak-keeper circuit is connected to each output. When selected, the circuit monitors the voltage on the pad and weakly drives the pin High or Low to match the input signal. If the pin is connected to a multiple-source signal, the weak keeper holds the signal in its last state if all drivers are disabled. Maintaining a valid logic level in this way helps eliminate bus chatter.

Because the weak-keeper circuit uses the IOB input buffer to monitor the input level, an appropriate V_{REF} voltage must be provided if the signalling standard requires one. The provision of this voltage must comply with the I/O banking rules.

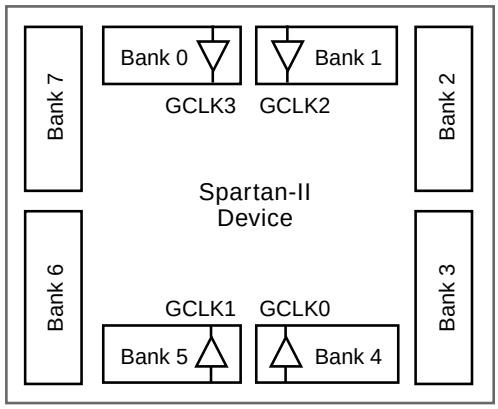


Figure 3: Spartan-II I/O Banks

I/O Banking

Some of the I/O standards described above require V_{CCO} and/or V_{REF} voltages. These voltages externally and connected to device pins that serve groups of IOBs, called banks. Consequently, restrictions exist about which I/O standards can be combined within a given bank.

Eight I/O banks result from separating each edge of the FPGA into two banks, as shown in Figure 3. Each bank has multiple V_{CCO} pins, all of which must be connected to the same voltage. This voltage is determined by the output standards in use.

Within a bank, output standards may be mixed only if they use the same V_{CCO}. Compatible standards are shown in Table 3. GTL and GTL+ appear under all voltages because their open-drain outputs do not depend on V_{CCO}.

Table 3: Compatible Output Standards

V_{CCO}	Compatible Standards
3.3V	PCI, LVTTL, SSTL3 I, SSTL3 II, CTT, AGP, GTL, GTL+
2.5V	SSTL2 I, SSTL2 II, LVCMOS2, GTL, GTL+
1.5V	HSTL I, HSTL III, HSTL IV, GTL, GTL+

Some input standards require a user-supplied threshold voltage, V_{REF}. In this case, certain user-I/O pins are automatically configured as inputs for the V_{REF} voltage. Approximately one in six of the I/O pins in the bank assume this role.

The V_{REF} pins within a bank are interconnected internally and consequently only one V_{REF} voltage can be used within each bank. All V_{REF} pins in the bank, however, must be connected to the external voltage source for correct operation.

Within a bank, inputs that require V_{REF} can be mixed with those that do not. However, only one V_{REF} voltage may be used within a bank. Input buffers that use V_{REF} are not 5V-tolerant. LVTTL, LVCMOS2, and PCI are 5V-tolerant.

The V_{CCO} and V_{REF} pins for each bank appear in the device pin-out tables and diagrams. The diagrams also show the bank affiliation of each I/O.

Within a given package, the number of V_{REF} and V_{CCO} pins can vary depending on the size of device. In larger devices, more I/O pins convert to V_{REF} pins. Since these are always a superset of the V_{REF} pins used for smaller devices, it is possible to design a PCB that permits migration to a larger device if necessary. All the V_{REF} pins for the largest device anticipated must be connected to the V_{REF} voltage, and not used for I/O.

In smaller devices, some V_{CCO} pins used in larger devices do not connect within the package. These unconnected pins may be left unconnected externally, or may be connected to the V_{CCO} voltage to permit migration to a larger device if necessary.

In TQ144 and PQ208 packages, all V_{CCO} pins are bonded together internally, and consequently the same V_{CCO} voltage must be connected to all of them. In the CS144 package, bank pairs that share a side are interconnected internally, pemitting four choices for VCCO. In both cases, the V_{REF} pins remain internally connected as eight banks, and may be used as described previously.

Configurable Logic Block

The basic building block of the Spartan-II CLB is the logic cell (LC). An LC includes a 4-input function generator, carry logic, and a storage element. The output from the function generator in each LC drives both the CLB output and the D input of the flip-flop. Each Spartan-II CLB contains four LCs, organized in two similar slices, a single slice is shown in Figure 4.

In addition to the four basic LCs, the Spartan-II CLB contains logic that combines function generators to provide functions of five or six inputs. Consequently, when estimating the number of system gates provided by a given device, each CLB counts as 4.5 LCs.

Look-Up Tables

Spartan-II function generators are implemented as 4-input look-up tables (LUTs). In addition to operating as a function generator, each LUT can provide a 16 x 1-bit synchronous RAM. Furthermore, the two LUTs within a slice can be combined to create a 16 x 2-bit or 32 x 1-bit synchronous RAM, or a 16 x 1-bit dual-port synchronous RAM.

The Spartan-II LUT can also provide a 16-bit shift register that is ideal for capturing high-speed or burst-mode data. This mode can also be used to store data in applications such as Digital Signal Processing.

Storage Elements

The storage elements in the Spartan-II slice can be configured either as edge-triggered D-type flip-flops or as level-sensitive latches. The D inputs can be driven either by

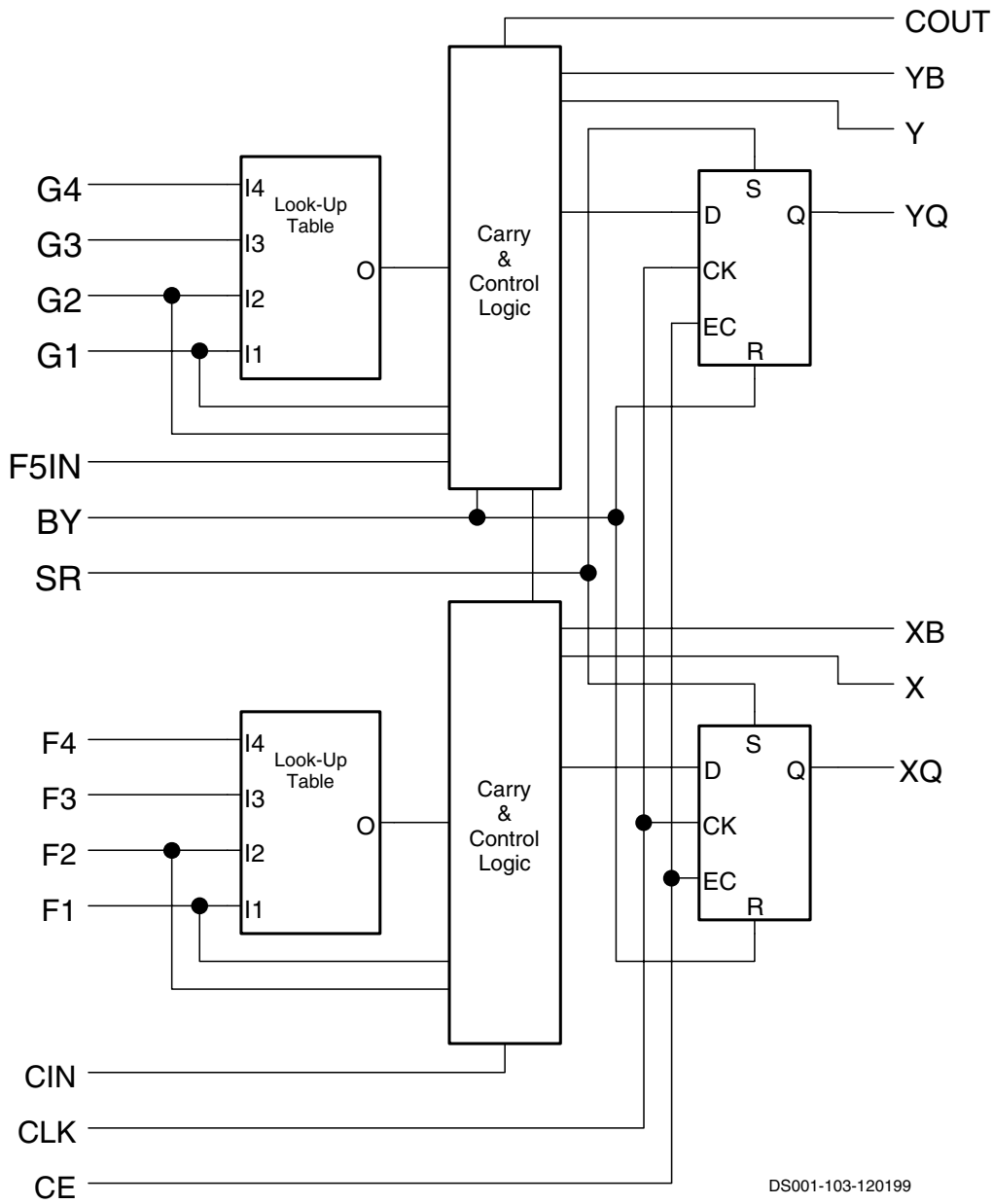


Figure 4: Spartan-II CLB Slice (two identical slices in each CLB)

the function generators within the slice or directly from slice inputs, bypassing the function generators.

In addition to Clock and Clock Enable signals, each Slice has synchronous set and reset signals (SR and BY). SR forces a storage element into the initialization state specified for it in the configuration. BY forces it into the opposite state. Alternatively, these signals may be configured to operate asynchronously.

All of the control signals are independently invertible, and are shared by the two flip-flops within the slice.

Additional Logic

The F5 multiplexer in each slice combines the function generator outputs. This combination provides either a function generator that can implement any 5-input function, a 4:1 multiplexer, or selected functions of up to nine inputs.

Similarly, the F6 multiplexer combines the outputs of all four function generators in the CLB by selecting one of the F5-multiplexer outputs. This permits the implementation of any 6-input function, an 8:1 multiplexer, or selected functions of up to 19 inputs.

Each CLB has four direct feedthrough paths, one per LC. These paths provide extra data input lines or additional local routing that does not consume logic resources.

Arithmetic Logic

Dedicated carry logic provides fast arithmetic carry capability for high-speed arithmetic functions. The Spartan-II CLB supports two separate carry chains, one per Slice. The height of the carry chains is two bits per CLB.

The arithmetic logic includes an XOR gate that allows a 1-bit full adder to be implemented within an LC. In addition, a dedicated AND gate improves the efficiency of multiplier implementation.

The dedicated carry path can also be used to cascade function generators for implementing wide logic functions.

BUFTs

Each Spartan-II CLB contains two 3-state drivers (BUFTs) that can drive on-chip busses. See “Dedicated Routing” on page 12. Each Spartan-II BUFT has an independent 3-state control pin and an independent input pin.

Block RAM

Spartan-II FPGAs incorporate several large BlockSelectRAM+ memories. These complement the distributed SelectRAM+ LUTRAMs that provide shallow RAM structures implemented in CLBs.

BlockSelectRAM+ memory blocks are organized in columns. All Spartan-II devices contain two such columns, one along each vertical edge. These columns extend the full height of the chip. Each memory block is four CLBs high, and consequently, a Spartan-II device eight CLBs high will contain two memory blocks per column, and a total of four blocks..

Table 4: Spartan-II Block SelectRAM+ Amounts

Spartan-II Device	# of Blocks	Total Block SelectRAM+ Bits
XC2S15	4	16,384
XC2S30	6	24,576
XC2S50	8	32,768
XC2S100	10	40,960
XC2S150	12	49,152

Each Block SelectRAM+ cell, as illustrated in Figure 5, is a fully synchronous dual-ported 4096-bit RAM with independent control signals for each port. The data widths of the two ports can be configured independently, providing built-in bus-width conversion.

.Table 5 shows the depth and width aspect ratios for the Block SelectRAM+

Table 5: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

The Spartan-II block RAM also includes dedicated routing to provide an efficient interface with both CLBs and other block RAMs.

Programmable Routing Matrix

It is the longest delay path that limits the speed of any worst-case design. Consequently, the Spartan-II routing architecture and its place-and-route software were defined in a single optimization process. This joint optimization minimizes long-path delays, and consequently, yields the best system performance.

The joint optimization also reduces design compilation times because the architecture is software-friendly. Design cycles are correspondingly reduced due to shorter design iteration times.

Local Routing

The VersaBlock provides local routing resources, as shown in Figure 6, providing the following three types of connections.

- Interconnections among the LUTs, flip-flops, and GRM
- Internal CLB feedback paths that provide high-speed connections to LUTs within the same CLB, chaining them together with minimal routing delay
- Direct paths that provide high-speed connections between horizontally adjacent CLBs, eliminating the delay of the GRM.

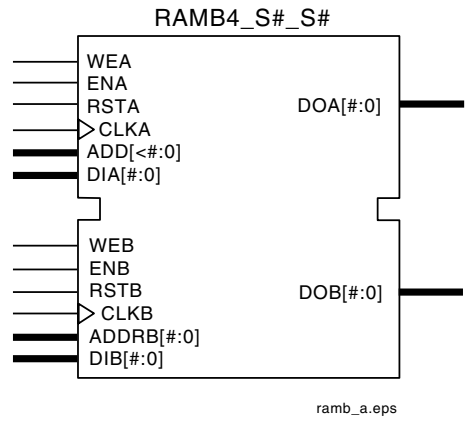


Figure 5: Dual-Port Block SelectRam+

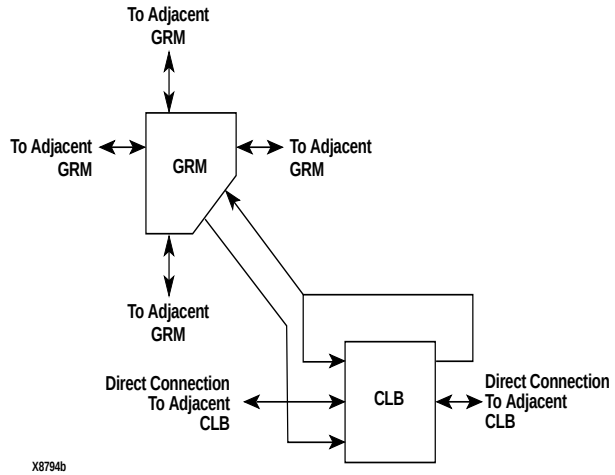


Figure 6: Spartan-II Local Routing

General Purpose Routing

Most Spartan-II signals are routed on the general purpose routing, and consequently, the majority of interconnect resources are associated with this level of the routing hierarchy. The general routing resources are located in horizontal and vertical routing channels associated with the rows and columns CLBs. The general-purpose routing resources are listed below.

- Adjacent to each CLB is a General Routing Matrix (GRM). The GRM is the switch matrix through which horizontal and vertical routing resources connect, and is also the means by which the CLB gains access to the general purpose routing.
- 24 single-length lines route GRM signals to adjacent GRMs in each of the four directions.
- 96 buffered Hex lines route GRM signals to another GRMs six-blocks away in each one of the four directions. Organized in a staggered pattern, Hex lines may be driven only at their endpoints. Hex-line signals can be accessed either at the endpoints or at the midpoint (three blocks from the source). One third of the Hex lines are bidirectional, while the remaining ones are uni-directional.
- 12 Longlines are buffered, bidirectional wires that distribute signals across the device quickly and efficiently. Vertical Longlines span the full height of the device, and horizontal ones span the full width of the device.

I/O Routing

Spartan-II devices have additional routing resources around their periphery that form an interface between the CLB array and the IOBs. This additional routing, called the VersaRing, facilitates pin-swapping and pin-locking, such that logic redesigns can adapt to existing PCB layouts. Time-to-market is reduced, since PCBs and other system components can be manufactured while the logic design is still in progress.

Dedicated Routing

Some classes of signal require dedicated routing resources to maximize performance. In the Spartan-II architecture, dedicated routing resources are provided for two classes of signal.

- Horizontal routing resources are provided for on-chip 3-state busses. Four partitionable bus lines are provided per CLB row, permitting multiple busses within a row, as shown in Figure 7.
- Two dedicated nets per CLB propagate carry signals vertically to the adjacent CLB.

Global Routing

Global Routing resources distribute clocks and other signals with very high fanout throughout the device. Spartan-II devices include two tiers of global routing resources referred to as primary and secondary global routing resources.

- The primary global routing resources are four dedicated global nets with dedicated input pins that are designed to distribute high-fanout clock signals with minimal skew. Each global clock net can drive all CLB, IOB, and block RAM clock pins. The primary global nets may only be driven by global buffers. There are four global buffers, one for each global net.
- The secondary global routing resources consist of 24 backbone lines, 12 across the top of the chip and 12

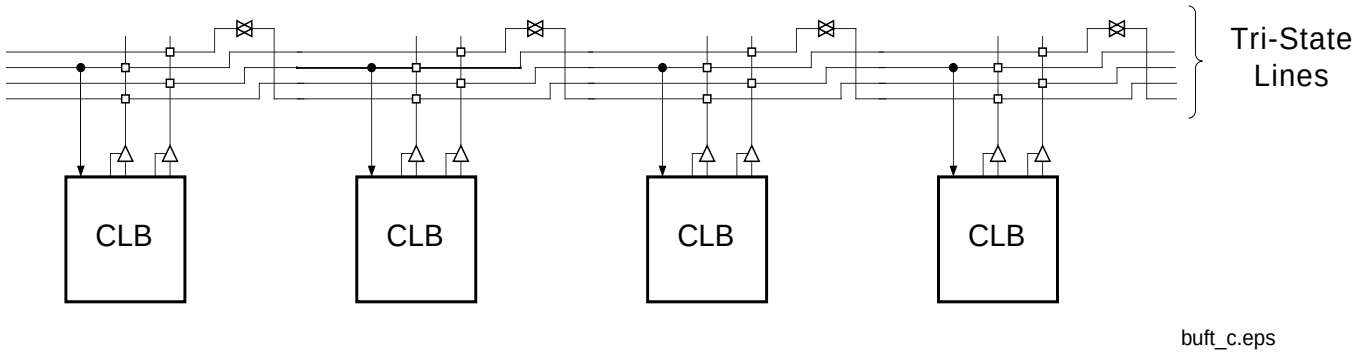


Figure 7: BUFT Connections to Dedicated Horizontal Bus Lines

across bottom. From these lines, up to 12 unique signals per column can be distributed via the 12 longlines in the column. These secondary resources are more flexible than the primary resources since they are not restricted to routing only to clock pins.

Clock Distribution

Spartan-II provides high-speed, low-skew clock distribution through the primary global routing resources described above. A typical clock distribution net is shown in Figure 8.

Four global buffers are provided, two at the top center of the device and two at the bottom center. These drive the four primary global nets that in turn drive any clock pin.

Four dedicated clock pads are provided, one adjacent to each of the global buffers. The input to the global buffer is selected either from these pads or from signals in the general purpose routing.

Delay-Locked Loop (DLL)

Associated with each global clock input buffer is a fully digital Delay-Locked Loop (DLL) that can eliminate skew between the clock input pad and internal clock-input pins throughout the device. Each DLL can drive two global clock networks.The DLL monitors the input clock and the distributed clock, and automatically adjusts a clock delay element. Additional delay is introduced such that clock edges reach internal flip-flops exactly one clock period after they arrive at the input. This closed-loop system effectively eliminates clock-distribution delay by ensuring that clock edges arrive at internal flip-flops in synchronism with clock edges arriving at the input.

In addition to eliminating clock-distribution delay, the DLL provides advanced control of multiple clock domains. The DLL provides four quadrature phases of the source clock,

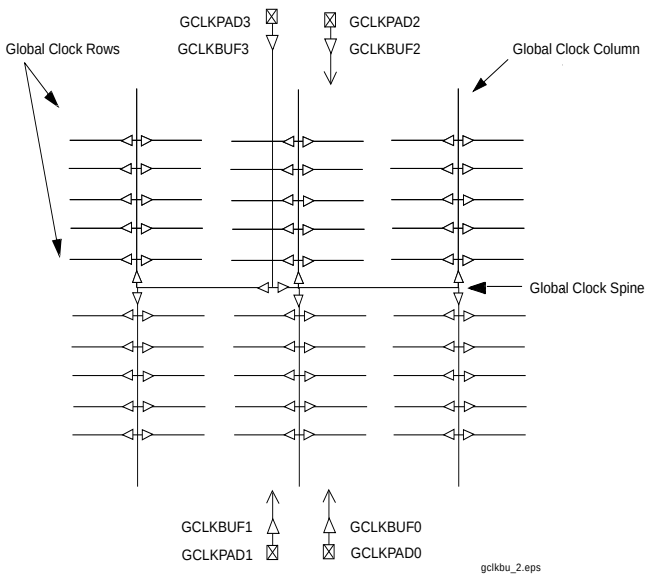


Figure 8: Global Clock Distribution Network

can double the clock, or divide the clock by 1.5, 2, 2.5, 3, 4, 5, 8, or 16. It has six outputs.

The DLL also operates as a clock mirror. By driving the output from a DLL off-chip and then back on again, the DLL can be used to deskew a board level clock among multiple Spartan-II devices.

In order to guarantee that the system clock is operating correctly prior to the FPGA starting up after configuration, the DLL can delay the completion of the configuration process until after it has achieved lock.

Boundary Scan

Spartan-II devices support all the mandatory boundary-scan instructions specified in the IEEE standard 1149.1. A Test Access Port (TAP) and registers are provided that implement the EXTEST, SAMPLE/PRELOAD, and BYPASS instructions. The TAP also supports two USERCODE instructions and internal scan chains.

The TAP uses dedicated package pins that always operate using LVTTL. For TDO to operate using LVTTL, the V_{CCO} for Bank 2 must be 3.3V. Otherwise, TDO switches rail-to-rail between ground and V_{CCO}.

Boundary-scan operation is independent of individual IOB configurations, and unaffected by package type. All IOBs, including unbonded ones, are treated as independent 3-state bidirectional pins in a single scan chain. Retention of the bidirectional test capability after configuration facilitates the testing of external interconnections.

Table 6 lists the boundary-scan instructions supported in Spartan-II FPGAs. Internal signals can be captured during EXTEST by connecting them to unbonded or unused IOBs. They may also be connected to the unused outputs of IOBs defined as unidirectional input pins. This technique partially compensates for the absence of INTEST support.

The public boundary-scan instructions are available prior to configuration. After configuration, the public instructions remain available together with any USERCODE instructions installed during the configuration. While the SAMPLE and BYPASS instructions are available during configuration, it is recommended that boundary-scan operations not be performed during this transitional period.

In addition to the test instructions outlined above, the boundary-scan circuitry can be used to configure the FPGA, and also to read back the configuration data.

To facilitate internal scan chains, the User Register provides three outputs (Reset, Update, and Shift) that represent the corresponding states in the boundary-scan internal state machine.

Figure 9 is a diagram of the Spartan-II Series boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

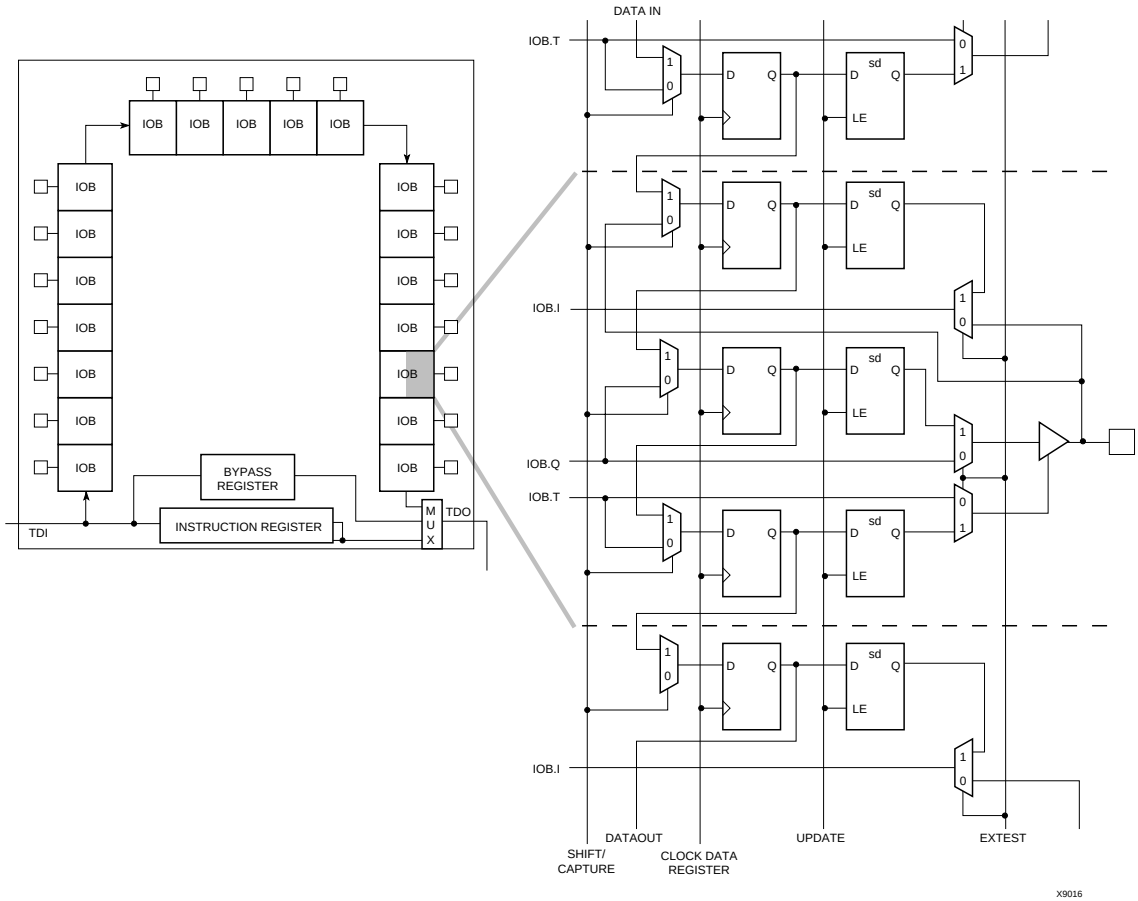


Figure 9: Spartan-II Series Boundary Scan Logic

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-State. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

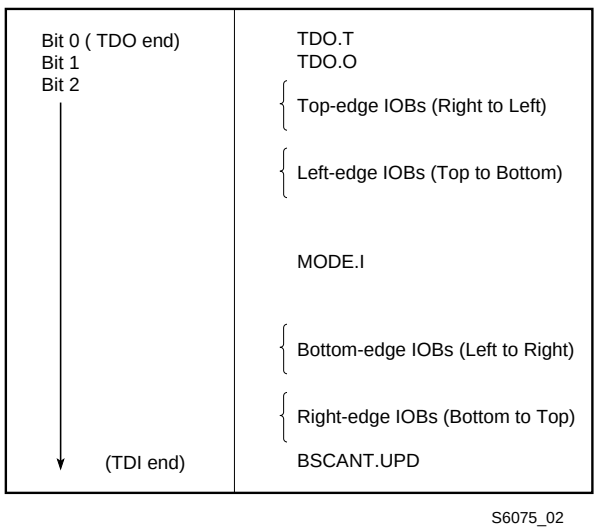


Figure 10: Boundary Scan Bit Sequence

From a cavity-up view of the chip (as shown in EPIC), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 10.

BSDL (Boundary Scan Description Language) files for Spartan-II Series devices are available on the Xilinx web site in the File Download area.

Development System

Spartan-II FPGAs are supported by the Xilinx Foundation and Alliance CAE tools. The basic methodology for Spartan-II design consists of three interrelated steps: design entry, implementation, and verification. Industry-standard tools are used for design entry and simulation (for example, Synopsys FPGA Express), while Xilinx provides proprietary architecture-specific tools for implementation.

The Xilinx development system is integrated under the Xilinx Design Manager (XDM™) software, providing designers with a common user interface regardless of their choice of entry and verification tools. The XDM software simplifies the selection of implementation options with pull-down menus and on-line help.

Table 6: Boundary-Scan Instructions

Boundary-Scan Command	Binary Code(4:0)	Description
EXTEST	00000	Enables boundary-scan EXTEST operation
SAMPLE	00001	Enables boundary-scan SAMPLE operation
USR1	00010	Access user-defined register 1
USR2	00011	Access user-defined register 2
CFG_OUT	00100	Access the configuration bus for Readback
CFG_IN	00101	Access the configuration bus for Configuration
INTEST	00111	Enables boundary-scan INTEST operation
USRCODE	01000	Enables shifting out USER code
IDCODE	01001	Enables shifting out of ID Code
HIZ	01010	Tri-states output pins while enabling the Bypass Register
JSTART	01100	Clock the start-up sequence when StartupClk is TCK
BYPASS	11111	Enables BYPASS
RESERVED	All other codes	Xilinx reserved instructions

Application programs ranging from schematic capture to Placement and Routing (PAR) can be accessed through the XDM software. The program command sequence is generated prior to execution, and stored for documentation.

Several advanced software features facilitate Spartan-II design. RPMs, for example, are schematic-based macros with relative location constraints to guide their placement. They help ensure optimal implementation of common functions.

For HDL design entry, the Xilinx FPGA Foundation development system provides interfaces to the following synthesis design environments.

- Synopsys (FPGA Compiler, FPGA Express)
- Exemplar (Spectrum)
- Synplicity (Synplify)

For schematic design entry, the Xilinx FPGA Foundation and alliance development system provides interfaces to the following schematic-capture design environments.

- Mentor Graphics V8 (Design Architect, QuickSim II)
- Viewlogic Systems (Viewdraw)

Third-party vendors support many other environments.

A standard interface-file specification, Electronic Design Interchange Format (EDIF), simplifies file transfers into and out of the development system.

Spartan-II FPGAs supported by a unified library of standard functions. This library contains over 400 primitives and macros, ranging from 2-input AND gates to 16-bit accumulators, and includes arithmetic functions, comparators, counters, data registers, decoders, encoders, I/O functions, latches, Boolean functions, multiplexers, shift registers, and barrel shifters.

The "soft macro" portion of the library contains detailed descriptions of common logic functions, but does not contain any partitioning or placement information. The performance of these macros depends, therefore, on the partitioning and placement obtained during implementation.

RPMs, on the other hand, do contain predetermined partitioning and placement information that permits optimal implementation of these functions. Users can create their own library of soft macros or RPMs based on the macros and primitives in the standard library.

The design environment supports hierarchical design entry, with high-level schematics that comprise major functional blocks, while lower-level schematics define the logic in these blocks. These hierarchical design elements are automatically combined by the implementation tools. Different design entry tools can be combined within a hierarchical design, thus allowing the most convenient entry method to be used for each portion of the design.

Design Implementation

The place-and-route tools (PAR) automatically provide the implementation flow described in this section. The partitioner takes the EDIF netlist for the design and maps the logic into the architectural resources of the FPGA (CLBs and IOBs, for example). The placer then determines the best locations for these blocks based on their interconnections and the desired performance. Finally, the router interconnects the blocks.

The PAR algorithms support fully automatic implementation of most designs. For demanding applications, however, the user can exercise various degrees of control over the process. User partitioning, placement, and routing information is optionally specified during the design-entry process. The implementation of highly structured designs can benefit greatly from basic floorplanning.

The implementation software incorporates Timing Wizard® timing-driven placement and routing. Designers specify timing requirements along entire paths during design entry. The timing path analysis routines in PAR then recognize these user-specified requirements and accommodate them.

Timing requirements are entered on a schematic in a form directly relating to the system requirements, such as the targeted clock frequency, or the maximum allowable delay between two registers. In this way, the overall performance of the system along entire signal paths is automatically tailored to user-generated specifications. Specific timing information for individual nets is unnecessary.

Design Verification

In addition to conventional software simulation, FPGA users can use in-circuit debugging techniques. Because Xilinx devices are infinitely reprogrammable, designs can be verified in real time without the need for extensive sets of software simulation vectors.

The development system supports both software simulation and in-circuit debugging techniques. For simulation, the system extracts the post-layout timing information from the design database, and back-annotates this information into the netlist for use by the simulator. Alternatively, the user can verify timing-critical portions of the design using the TRACE® static timing analyzer.

For in-circuit debugging, the development system includes a download and readback cable. This cable connects the FPGA in the target system to a PC or workstation. After downloading the design into the FPGA, the designer can single-step the logic, readback the contents of the flip-flops, and so observe the internal logic state. Simple modifications can be downloaded into the system in a matter of minutes.

Configuration

Configuration is the process by which the bit-stream of a design, as generated by the Xilinx development software, is loaded into the internal configuration memory of the FPGA. Spartan-II devices support both serial configuration, using the master/slave serial and JTAG modes, as well as byte-wide configuration employing the Slave Parallel mode.

Table 7: Spartan-II Configuration File Size

Device	Configuration File Size (Bits)
XC2S15	197,728
XC2S30	336,800
XC2S50	559,232
XC2S100	781,248
XC2S150	1,040,128

The Configuration File

Spartan-II devices are configured by sequentially loading frames of data that have been concatenated into a configuration file. Table 7 shows how much nonvolatile storage space is needed for Spartan-II devices.

It is important to note that, while a PROM is commonly used to store configuration data before loading them into the FPGA, it is by no means required. Any of a number of different kinds of under populated nonvolatile storage already available either on or off the board (i.e., hard drives, FLASH cards, etc.) can be used. For more information on configuration without a PROM, refer to XAPP098 ‘The Low-Cost, Efficient Serial Configuration of Spartan FPGAs.

Modes

Spartan-II supports the following four configuration modes.

- Slave-serial mode
- Master-serial mode
- Slave Parallel mode
- Boundary-scan mode

The Configuration mode pins (M2, M1, M0) select among these configuration modes with the option in each case of having the IOB pins either pulled up or left floating prior to configuration. The selection codes are listed in Table 8.

Table 8: Configuration Codes

Configuration Mode	Pre-configuration Pull-ups	M0	M1	M2	CCLK Direction	Data Width	Serial D_{out}
Master-serial mode	No	0	0	0	Out	1	Yes
	Yes	0	0	1			
Slave Parallel mode	Yes	0	1	0	In	8	No
	No	0	1	1			
Boundary-scan mode	Yes	1	0	0	N/A	1	No
	No	1	0	1			
Slave-serial mode	Yes	1	1	0	In	1	Yes
	No	1	1	1			

Configuration through the boundary-scan port is always available, independent of the mode selection. Selecting the boundary-scan mode simply turns off the other modes. The three mode pins have internal pull-up resistors, and default to a logic High if left unconnected.

Signals

There are two kinds of pins that are used to configure Spartan-II devices: Dedicated pins perform only specific configuration-related functions. The other pins can serve as general purpose I/Os once user operation has begun.

The dedicated pins comprise the mode pins (M2, M1, M0), the configuration clock pin (CCLK), the PROGRAM pin, the DONE pin and the boundary-scan pins (TDI, TDO, TMS, TCK). Depending on the selected configuration mode, CCLK may be an output generated by the FPGA, or may be generated externally, and provided to the FPGA as an input.

Note that some configuration pins can act as outputs. For correct operation, these pins require a V_{CCO} of 3.3V to drive an LVTTL signal. All the relevant pins fall in banks 2 or 3.

For a more detailed description than that given below, see Pin Definitions and XAPP176, "Spartan-II FPGA Series Configuration and Readback".

The Process

The sequence of steps necessary to configure Spartan-II devices are shown in Figure 11. The overall flow can be divided into three different phases.

- Initiating Configuration
- Configuration memory clear
- Loading data frames
- Start-up

The memory clearing and start-up phases are the same for all configuration modes; however, the steps for the loading of data frames are different. Thus, the details for data frame loading are described separately in the sections devoted to each mode.

Initiating Configuration

There are two different ways to initiate the configuration process: applying power to the device or asserting the PROGRAM input.

Configuration on power-up occurs automatically unless it is delayed by the user, as described in a separate section below. The waveform for configuration on power-up is shown Figure 12 on page 18 Before configuration can begin, V_{CCO} for bank 2 must be greater than 1.0V. Furthermore, all V_{CCINT} power pins must be connected to a 2.5V supply. At power-up, Vcc must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling

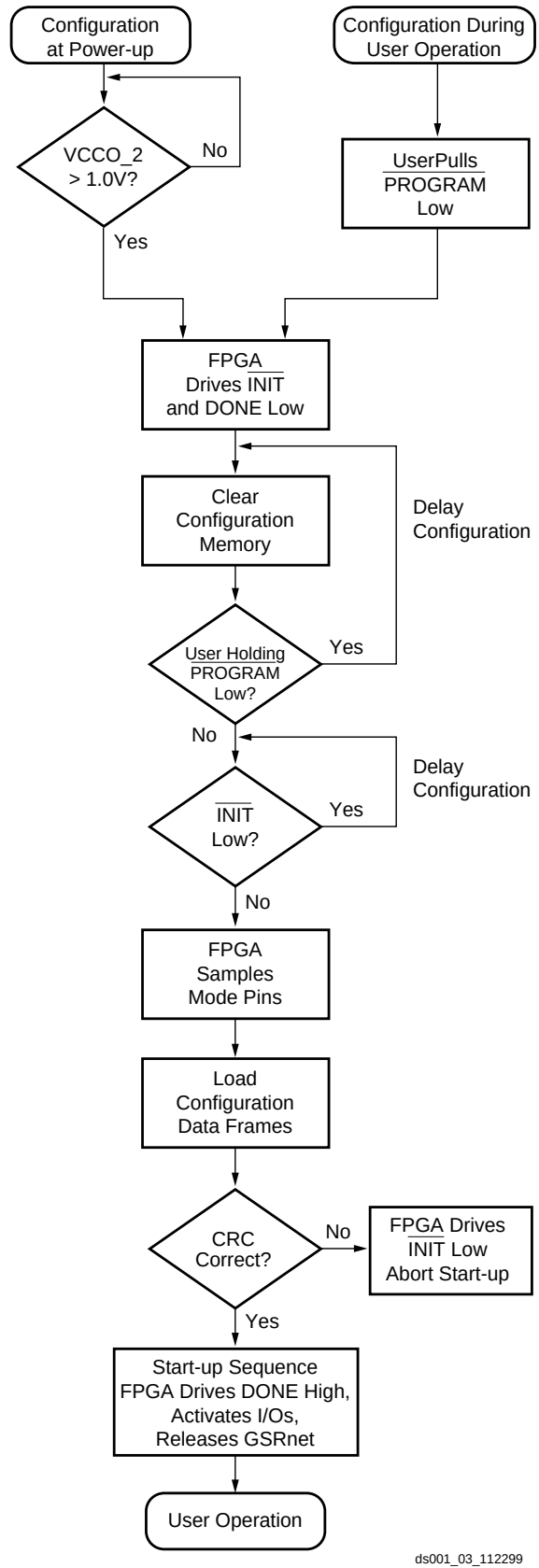
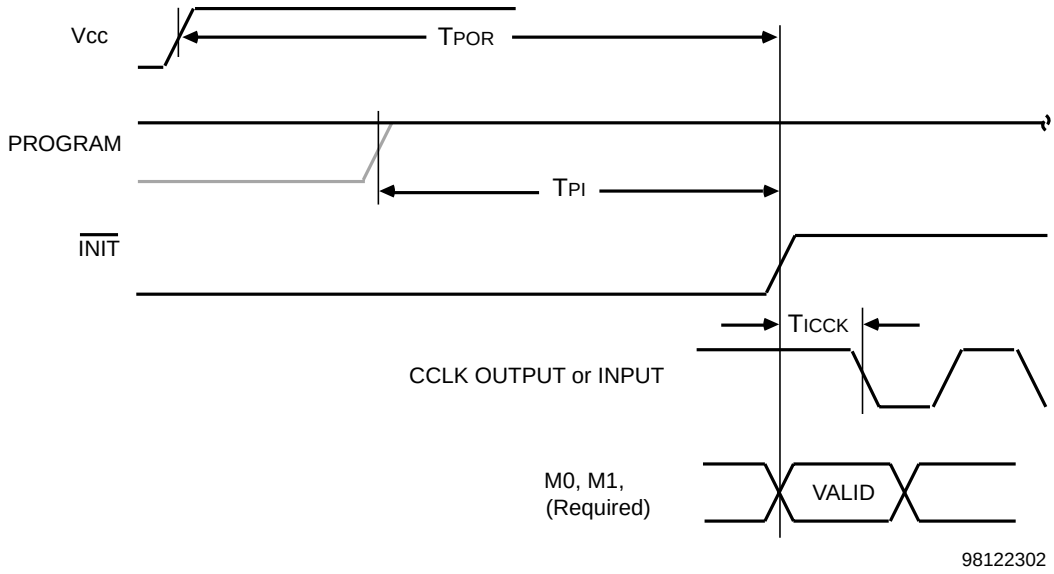


Figure 11: Configuration Flow Diagram



Description	Symbol		Units
Power-on Reset	T_{POR}	2	ms, max
Program Latency	T_{PL}	100	µs, max
CCLK (output) delay	T_{ICCK}	0.5	µs, min
		4	µs, max

Figure 12: Configuration Timing on Power-Up

PROGRAM Low until Vcc is valid. For more information on delaying configuration, see the next section.

Once in user operation, the device can be re-configured simply by pulling the PROGRAM pin Low. The device acknowledges the beginning of the configuration process by driving DONE Low, then enters the memory-clearing phase. .

Clearing Configuration Memory

The device indicates that clearing the configuration memory is in progress by driving INIT Low. At this time, the user can delay configuration by holding either PROGRAM or INIT Low, which causes the device to remain in the memory clearing phase. Note that the bidirectional INIT line is driving a Low logic level during memory clearing. Thus, to avoid contention, use an open-drain driver to keep INIT Low.

With no delay in force, the device indicates that the memory is completely clear by driving INIT High. The FPGA samples its mode pins on this Low-to-High transition.

Loading Configuration Data.

Once INIT is High, the user can begin loading configuration data frames into the device. The details of loading the configuration data are discussed in the sections treating the configuration modes individually. The sequence of operations necessary to load configuration data using the serial modes is shown in Figure 14 Loading data using the Slave Parallel mode is shown in Figure 19 on page 23.

CRC Error Checking

During the loading of configuration data, a CRC value embedded in the configuration file is checked against a CRC value calculated within the FPGA. If the CRC values do not match, the FPGA drives INIT Low to indicate that a frame error has occurred and configuration is aborted.

To reconfigure the device, the PROGRAM pin should be asserted to reset the configuration logic. Recycling power also resets the FPGA for configuration. See “Initiating Configuration” on page 17

Start-up

The start-up sequence oversees the transition of the FPGA from the configuration state to full user operation. A match of CRC values, indicating a successful loading of the configuration data, initiates the sequence.

During start-up, the device performs four operations:

1. The assertion of DONE. The failure of DONE to go High may indicate the unsuccessful loading of configuration data.

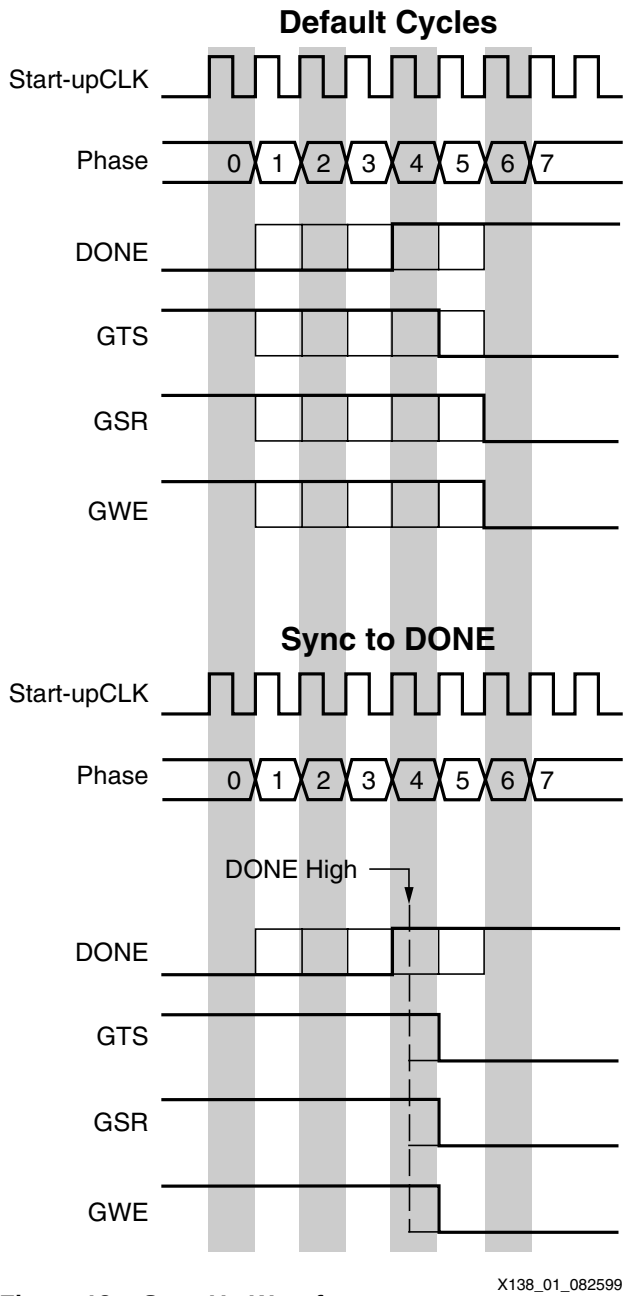


Figure 13: Start-Up Waveforms

2. The release of the Global Three State. This activates all the I/Os.

3. Negates Global Set Reset (GSR). This allows all flip-flops to change state.

4. The assertion of Global Write Enable (GWE). This allows all RAMs and flip-flops to change state.

By default, these operations are synchronized to CCLK. The entire start-up sequence lasts eight cycles, called C0-C7, after which the loaded design is fully functional. The default timing for start-up is shown in the top half of Figure 13 on page 19. The four operations can be selected to switch on any CCLK cycle C1-C6 through settings in BitGen, part of the Xilinx Development Software. The heavy lines show the defaults settings.

The bottom half of Figure 13 shows another commonly used version of the start-up timing known as Sync-to-DONE. This version makes the GTS, GSR, and GWE events conditional upon the DONE pin going High. This timing is important for a daisy chain of multiple FPGAs in serial mode, since it ensures that all FPGAs go through start-up together, after all their DONE pins have gone High.

Sync-to-DONE timing is selected by setting the GTS, GSR, and GWE cycles to a value of DONE in the BitGen configuration options. This causes these signals to transition one clock cycle after DONE externally transitions High.

The Serial Modes

There are two serial configuration modes: In Master Serial mode, the FPGA controls the configuration process by driving CCLK as an output. In Slave Serial mode, the FPGA passively receives CCLK as an input from an external agent (e.g., a microprocessor, CPLD, or second FPGA in the master mode) that is controlling the configuration process. In both modes, the FPGA is configured by loading one bit per CCLK cycle. The MSB of each configuration data byte is always written to the D_{IN} pin first.

The sequence of operations necessary to load data into the Spartan-II FPGA serially appears in Figure 14. This is an expansion of the "Load Configuration Data Frames" block in Figure 11 on page 17.

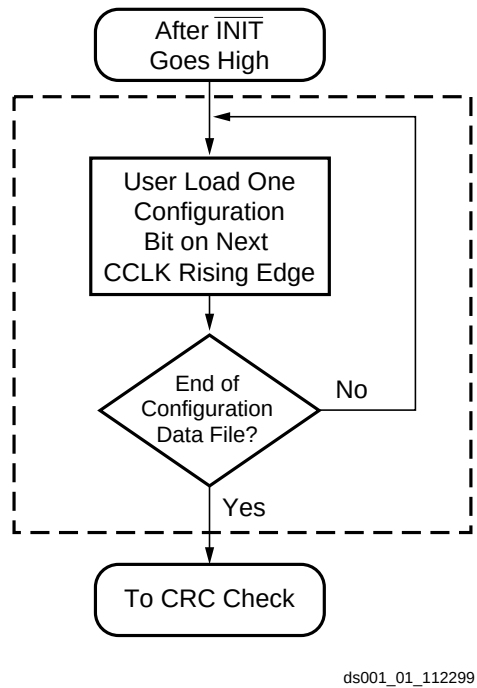


Figure 14: Loading Config. Data for the Serial Modes

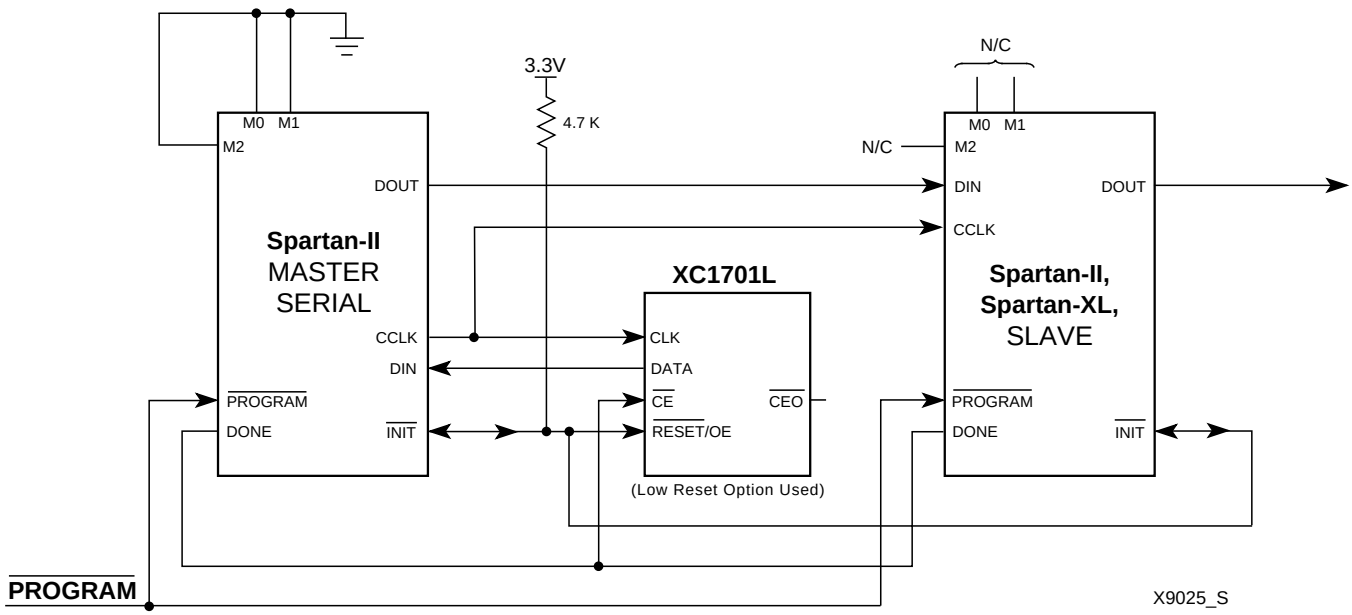
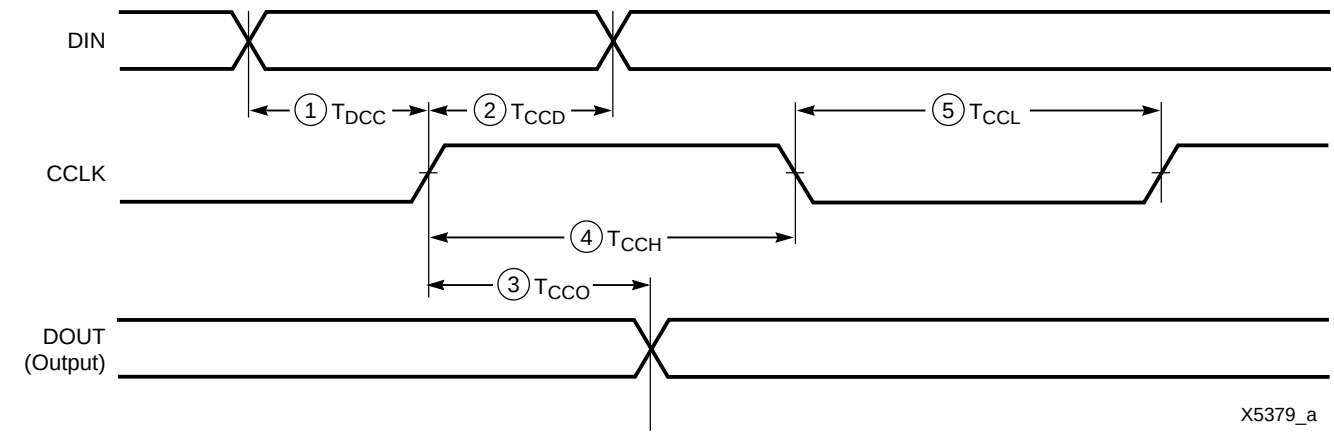


Figure 15: Master/Slave Serial Configuration Circuit Diagram

Slave Serial Mode

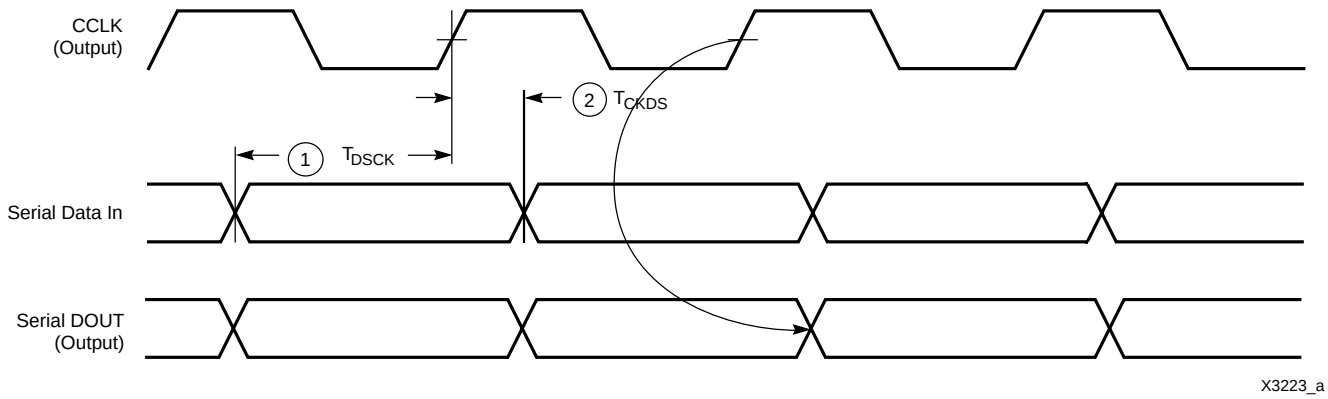
In Slave Serial mode, the FPGA's CCLK pin is driven by an external source. This mode allows for FPGAs to be configured from other logic devices, such as microprocessors, or in a daisy-chain configuration. Figure 15 on page 20 shows the connections for a Master Serial FPGA configuring a Slave Serial FPGA from an SPROM. A Spartan-II device in slave serial mode should be connected as shown for the third device from the left. Master serial mode is selected by a <111> on the mode pins (M0, M1, M2).

Figure 16 on page 20 shows the timing for Slave Serial configuration. The serial bitstream must be setup at the DIN input pin a short time before each rising edge of an externally generated CCLK.



	Description	Symbol			Units
CCLK	DIN setup	1	T_{DCC}	5	ns, min
	DIN hold	2	T_{CCD}	0	ns, min
	DOUT	3	T_{CCO}	12	ns, max
	High time	4	T_{CCH}	5	ns, min
	Low time	5	T_{CCL}	5	ns, min
	Maximum Frequency		F_{CC}	66	MHz, max

Figure 16: Slave Serial Mode Timing



	Description	Symbol			Units
CCLK	DIN setup	1	T_{DSCK}	5.0	ns, min
	DIN hold	2	T_{CKDS}	0.0	ns, min
	Frequency Tolerance with respect to nominal			+45% –30%	

Figure 17: Master Serial Mode Timing

Multiple FPGAs in slave serial mode can be daisy-chained for configuration from a single source. After a particular FPGA has been configured, the data for the next device is routed to the DOUT pin. The data on the DOUT pin changes on the rising edge of CCLK. Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High. For more information, see "Start-up" on page 18.

Master Serial Mode

In master serial mode, the CCLK output of the FPGA drives a Xilinx Serial PROM which feeds a serial stream of configuration data to the FPGAs DIN input. Figure 15 shows a Master Serial FPGA configuring a Slave Serial FPGA from an SPROM. A Spartan-II device in master serial mode should be connected as shown for the device on the left side. Master serial mode is selected by a <000> on the mode pins (M0, M1, M2). The SPROM RESET pin is driven by $\overline{INIT}$, and CE input is driven by DONE.The interface is identical to the slave serial mode except that an oscillator internal to the FPGA is used to generate the configuration clock (CCLK). Any of a number of different frequencies ranging from 4 to 60 MHz can be set using the ConfigRate option in BitGen, part of the Xilinx development software. On power-up, while the first 60 bytes of the configuration data are being loaded, the CCLK frequency is always 2.5 MHz. This frequency is used until the ConfigRate bits, part of the configuration file, have been loaded into the FPGA, at which point, the frequency changes to the selected ConfigRate. Unless a different frequency is specified in the design, the default ConfigRate is 4 MHz. The period of the CCLK signal created by the internal oscillator has a variance of +45%/-30% from the specified value.

Figure 17 shows the timing for Master Serial configuration. The FPGA accepts one bit of configuration data on each rising CCLK edge. After the FPGA has been loaded, the data for the next device in a daisy-chain is presented on the DOUT pin after the rising CCLK edge.

Slave Parallel Mode

The Slave Parallel mode is the fastest configuration option. Byte-wide data is written into the FPGA. A BUSY flag is provided for controlling the flow of data at clock frequencies above 50 MHz.

Figure 18 on page 22 shows the connections for two Spartan-II devices using the Slave Parallel mode. Slave Parallel mode is selected by a <011> on the mode pins (M0, M1, M2).

The agent controlling configuration is not shown. Typically, a processor, a microcontroller, or CPLD controls the Slave Parallel interface. The controlling agent provides byte-wide configuration data, CCLK, a Chip Select ($\overline{CS}$) signal and a Write signal ($\overline{WRITE}$). If BUSY is asserted (High) by the FPGA, the data must be held until BUSY goes Low.

After configuration, the pins of the Slave Parallel port (D0-D7) can be used as additional user I/O. Alternatively, the port may be retained to permit high-speed 8-bit readback. Then data can be read by de-asserting $\overline{WRITE}$. See "Readback" on page 23.

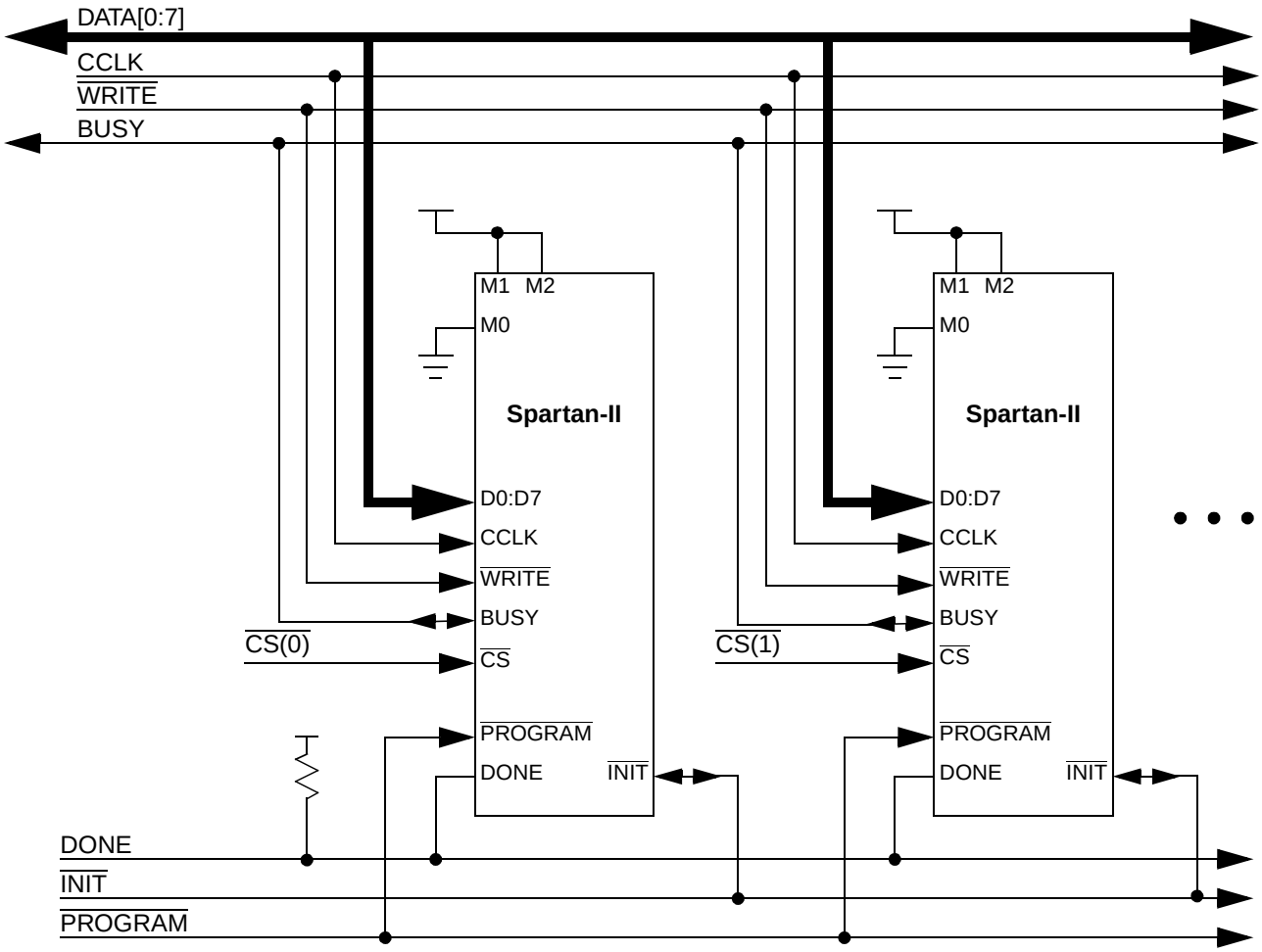


Figure 18: Slave Parallel Configuration Circuit Diagram

Multiple Spartan-II FPGAs can be configured using the Slave Parallel mode, and be made to start-up simultaneously. To configure multiple devices in this way, wire the individual CCLK, Data, $\overline{\text{WRITE}}$, and BUSY pins of all the devices in parallel. The individual devices are loaded separately by asserting the $\overline{\text{CS}}$ pin of each device in turn and writing the appropriate data. Sync-to-DONE start-up timing is used to ensure that the start-up sequence does not begin until all the FPGAs have been loaded. See "Start-up" on page 18.

Write

When using the Slave Parallel Mode, write operations send packets of byte-wide configuration data into the FPGA. Figure 19 on page 23 shows a flowchart of the write sequence used to load data into the Spartan-II FPGA. This is an expansion of the "Load Configuration Data Frames" block in Figure 11 on page 17. The timing for write operations is shown in Figure 20 on page 24.

For the present example, the user holds $\overline{\text{WRITE}}$ and $\overline{\text{CS}}$ Low throughout the sequence of write operations. Note that when $\overline{\text{CS}}$ is asserted on successive CCLKs, $\overline{\text{WRITE}}$ must remain either asserted or de-asserted. Otherwise an abort will be initiated, as in the next section.

9. Drive data onto D0-D7. Note that to avoid contention, the data source should not be enabled while $\overline{\text{CS}}$ is Low and $\overline{\text{WRITE}}$ is High. Similarly, while $\overline{\text{WRITE}}$ is High, no more than one device's $\overline{\text{CS}}$ should be asserted.
10. On the rising edge of CCLK: If BUSY is Low, the data is accepted on this clock. If BUSY is High (from a previous write), the data is not accepted. Acceptance will instead occur on the first clock after BUSY goes Low, and the data must be held until this happens.
11. Repeat steps 2 and 3 until all the data has been sent.
12. De-assert $\overline{\text{CS}}$ and $\overline{\text{WRITE}}$.

If CCLK is slower than f_{CCNH}, the FPGA will never assert BUSY. In this case, the above handshake is unnecessary, and data can simply be entered into the FPGA every CCLK cycle.

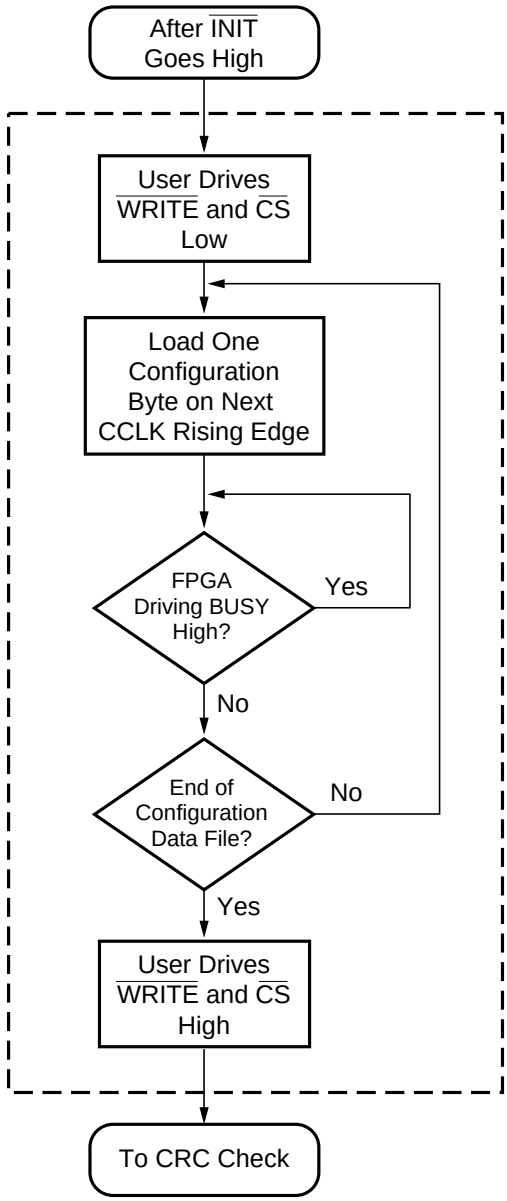


Figure 19: Loading Configuration Data for the Slave Parallel Mode

A configuration packet does not have to be written in one continuous stretch, rather it can be split into many write sequences. Each sequence would involve assertion of $\overline{CS}$.

In applications where multiple clock cycles may be required to access the configuration data before each byte can be loaded into the Slave Parallel interface, a new byte of data may not be ready for each consecutive CCLK edge. In such a case the $\overline{CS}$ signal may be de-asserted until the next byte is valid on D0-D7. While $\overline{CS}$ is High, the Slave Parallel interface does not expect any data and ignores all CCLK transitions. However, to avoid aborting configuration, $\overline{WRITE}$ must continue to be asserted while $\overline{CS}$ is asserted.

Abort

To abort configuration during a write sequence, de-assert $\overline{WRITE}$ while holding $\overline{CS}$ Low. The abort operation is initiated at the rising edge of CCLK, as shown in Figure 21 on page 24. The device will remain BUSY until the aborted operation is complete. After aborting configuration, data is assumed to be unaligned to word boundaries and the FPGA requires a new synchronization word prior to accepting any new packets.

Boundary-Scan Mode

In the boundary-scan mode, no non-dedicated pins are required, configuration being done entirely through the IEEE 1149.1 Test Access Port.

Configuration through the TAP uses the special CFG_IN instruction. This instruction allows data input on TDI to be converted into data packets for the internal configuration bus.

The following steps are required to configure the FPGA through the boundary-scan port.

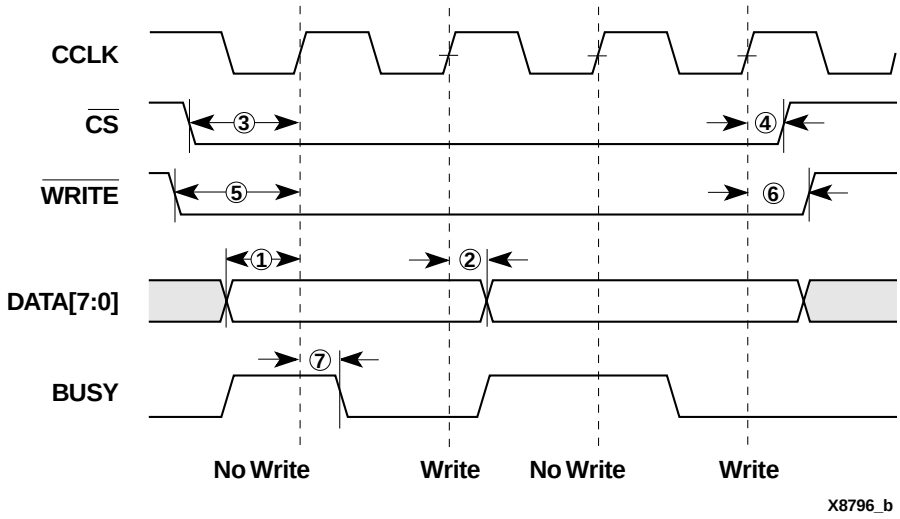
1. Load the CFG_IN instruction into the boundary-scan instruction register (IR)
2. Enter the Shift-DR (SDR) state
3. Shift a standard configuration bitstream into TDI
4. Return to Run-Test-Idle (RTI)
5. Load the JSTART instruction into IR
6. Enter the SDR state
7. Clock TCK through the sequence (the length is programmable)
8. Return to RTI

Configuration and readback via the TAP is always available. The boundary-scan mode simply locks out the other modes. The boundary-scan mode is selected by a <101> on the mode pins (M0, M1, M2).

Readback

The configuration data stored in the Spartan-II configuration memory can be readback for verification. Along with the configuration data it is possible to readback the contents of all flip-flops/latches, LUTRAMs, and block RAMs. This capability is used for real-time debugging.

For more detailed information see XAPP176 "*Spartan-II FPGA Series Configuration and Readback*"



	Description	Symbol			Units
CCLK	D_{0-7} Setup/Hold	1	T_{SMDCC}	5	ns, min
	D_{0-7} Hold	2	T_{SMCCD}	0	ns, min
	$\overline{CS}$ Setup	3	T_{SMCSCC}	7	ns, min
	$\overline{CS}$ Hold	4	T_{SMCCCS}	0	ns, min
	$\overline{WRITE}$ Setup	5	T_{SMCCW}	7	ns, min
	$\overline{WRITE}$ Hold	6	T_{SMWCC}	0	ns, min
	BUSY Propagation Delay	7	T_{SMCKBY}	12	ns, max
	Maximum Frequency		F_{CC}	66	MHz, max
	Maximum Frequency with no handshake		F_{CCNH}	50	MHz, max

Figure 20: Slave Parallel Write Timing

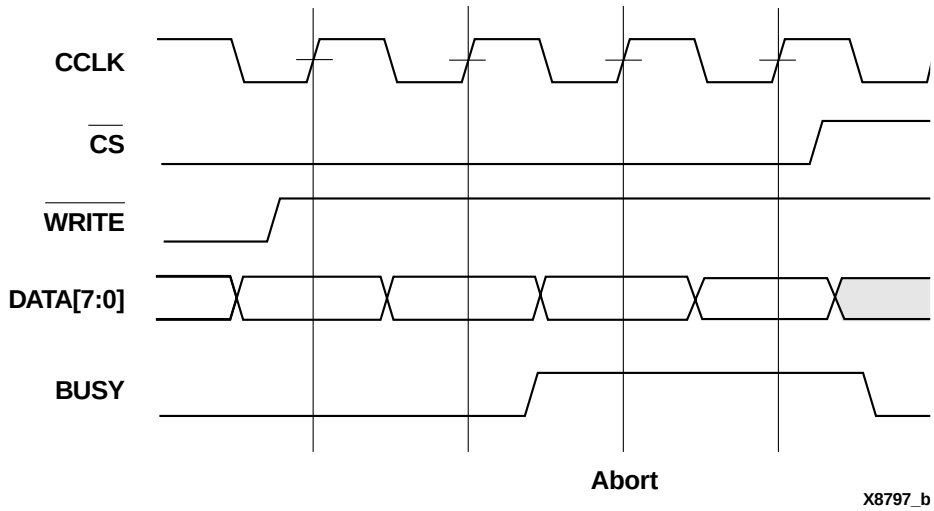


Figure 21: Slave Parallel Write Abort Waveforms

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Design Considerations

This section contains more detailed design information on the following features.

Using Delay-Locked Loop

The Spartan-II FPGA family provides up to four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits which improve and simplify system level design.

Introduction

As FPGAs grow in size, quality on-chip clock distribution becomes increasingly important. Clock skew and clock delay impact device performance and the task of managing clock skew and clock delay with conventional clock trees becomes more difficult in large devices. The Spartan-II family of devices resolve this potential problem by providing up to eight fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay and low clock skew between output clock signals distributed throughout the device.

Each DLL can drive up to two global clock routing networks within the device. The global clock distribution network minimizes clock skews due to loading differences. By monitoring a sample of the DLL output clock, the DLL can compensate for the delay on the routing network, effectively eliminating the delay from the external input port to the individual clock loads within the device.

In addition to providing zero delay with respect to a user source clock, the DLL can provide multiple phases of the source clock. The DLL can also act as a clock doubler or it can divide the user source clock by up to 16.

Clock multiplication gives the designer a number of design alternatives. For instance, a 50 MHz source clock doubled by the DLL can drive an FPGA design operating at 100 MHz. This technique can simplify board design because the clock path on the board no longer distributes such a high-speed signal. A multiplied clock also provides designers the option of time-domain-multiplexing, using one circuit twice per clock cycle, consuming less area than two copies of the same circuit. Two DLLs in can be connected in series to increase the effective clock multiplication factor to four.

The DLL can also act as a clock mirror. By driving the DLL output off-chip and then back in again, the DLL can be used to de-skew a board level clock between multiple devices.

In order to guarantee the system clock establishes prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL achieves lock.

By taking advantage of the DLL to remove on-chip clock delay, the designer can greatly simplify and improve system level design involving high-fanout, high-performance clocks.

Library DLL Symbols

Figure 22 shows the simplified Xilinx library DLL macro symbol, BUFGDLL. This macro delivers a quick and efficient way to provide a system clock with zero propagation delay throughout the device. Figure 23 and Figure 24 show the two library DLL primitives. These symbols provide access to the complete set of DLL features when implementing more complex applications.

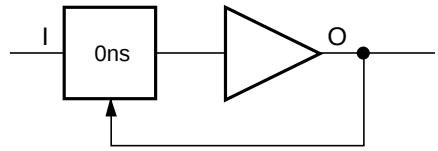


Figure 22: Simplified DLL Macro Symbol BUFGDLL

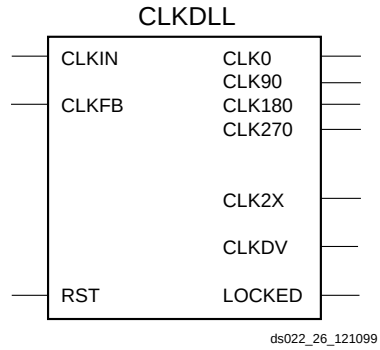


Figure 23: Standard DLL Symbol CLKDLL

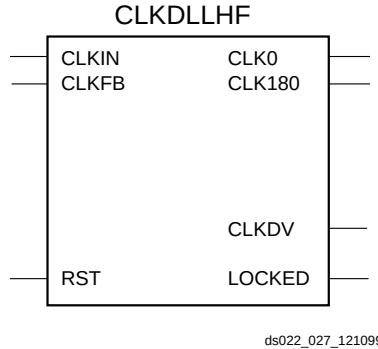


Figure 24: High Frequency DLL Symbol CLKDLLHF

BUFGDLL Pin Descriptions

Use the BUFGDLL macro as the simplest way to provide zero propagation delay for a high-fanout on-chip clock from an external input. This macro uses the IBUFG, CLKDLL and BUFG primitives to implement the most basic DLL application as shown in Figure 25.

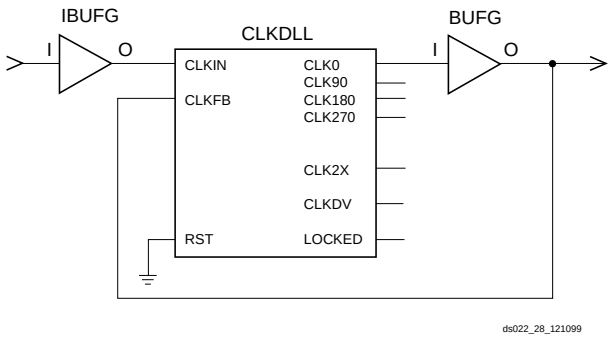


Figure 25: BUFGDLL Schematic

This symbol does not provide access to the advanced clock domain controls or to the clock multiplication or clock division features of the DLL. This symbol also does not provide access to the RST, or LOCKED pins of the DLL. For access to these features, a designer must use the library DLL primitives described in the following sections.

Source Clock Input — I

The I pin provides the user source clock, the clock signal on which the DLL operates, to the BUFGDLL. For the BUFGDLL macro the source clock frequency must fall in the low frequency range as specified in the data sheet. The BUFGDLL requires an external signal source clock. Therefore, only an external input port can source the signal that drives the BUFGDLL I pin.

Clock Output — O

The clock output pin O represents a delay-compensated version of the source clock (I) signal. This signal, sourced by a global clock buffer BUFG symbol, takes advantage of the dedicated global clock routing resources of the device.

The output clock has a 50-50 duty cycle unless you deactivate the duty cycle correction property.

CLKDLL Primitive Pin Descriptions

The library CLKDLL primitives provide access to the complete set of DLL features needed when implementing more complex applications with the DLL.

Source Clock Input — CLKIN

The CLKIN pin provides the user source clock (the clock signal on which the DLL operates) to the DLL. The CLKIN frequency must fall in the ranges specified in the data sheet. A global clock buffer (BUFG) driven from another CLKDLL or one of the global clock input buffers (IBUFG) must source this clock signal.

Feedback Clock Input — CLKFB

The DLL requires a reference or feedback signal to provide the delay-compensated output. Connect only the CLK0 or CLK2X DLL outputs to the feedback clock input (CLKFB) pin to provide the necessary feedback to the DLL. The feedback clock input can also be provided through one of the following pin.

IBUFG - Global Clock Input Pad

If an IBUFG sources the CLKFB pin, the following special rules apply.

1. An external input port must source the signal that drives the IBUFG I pin.
2. The CLK2X output must feedback to the device if both the CLK0 and CLK2X outputs are driving off chip devices.
3. That signal must directly drive only OBUFs and nothing else.

These rules enable the software determine which DLL clock output sources the CLKFB pin.

Reset Input — RST

When the reset pin RST activates the LOCKED signal deactivates within four source clock cycles. The RST pin, active High, must either connect to a dynamic signal or tied to ground. As the DLL delay taps reset to zero, glitches can occur on the DLL clock output pins. Activation of the RST pin can also severely affect the duty cycle of the clock output pins. Furthermore, the DLL output clocks no longer de-skew with respect to one another. For these reasons, rarely use the reset pin unless re-configuring the device or changing the input frequency.

2x Clock Output — CLK2X

The output pin CLK2X provides a frequency-doubled clock with an automatic 50/50 duty-cycle correction. Until the CLKDLL has achieved lock, the CLK2X output appears as a 1x version of the input clock with a 25/75 duty cycle. This behavior allows the DLL to lock on the correct edge with respect to source clock. This pin is not available on the CLKDLLHF primitive.

Clock Divide Output — CLKDV

The clock divide output pin CLKDV provides a lower frequency version of the source clock. The CLKDV_DIVIDE property controls CLKDV such that the source clock is divided by N where N is either 1.5, 2, 2.5, 3, 4, 5, 8, or 16.

This feature provides automatic duty cycle correction such that the CLKDV output pin always has a 50/50 duty cycle.

1x Clock Outputs — CLK[0|90|180|270]

The 1x clock output pin CLK0 represents a delay-compensated version of the source clock (CLKIN) signal. The CLKDLL primitive provides three phase-shifted versions of the CLK0 signal while CLKDLLHF provides only the 180 phase-shifted version. The relationship between phase shift and the corresponding period shift appears in Table 9.

Table 9: Relationship of Phase-Shifted Output Clock to Period Shift

Phase (degrees)	Period Shift (percent)
0	0%
90	25%
180	50%
270	75%

The timing diagrams in Figure 26 illustrate the DLL clock output characteristics.

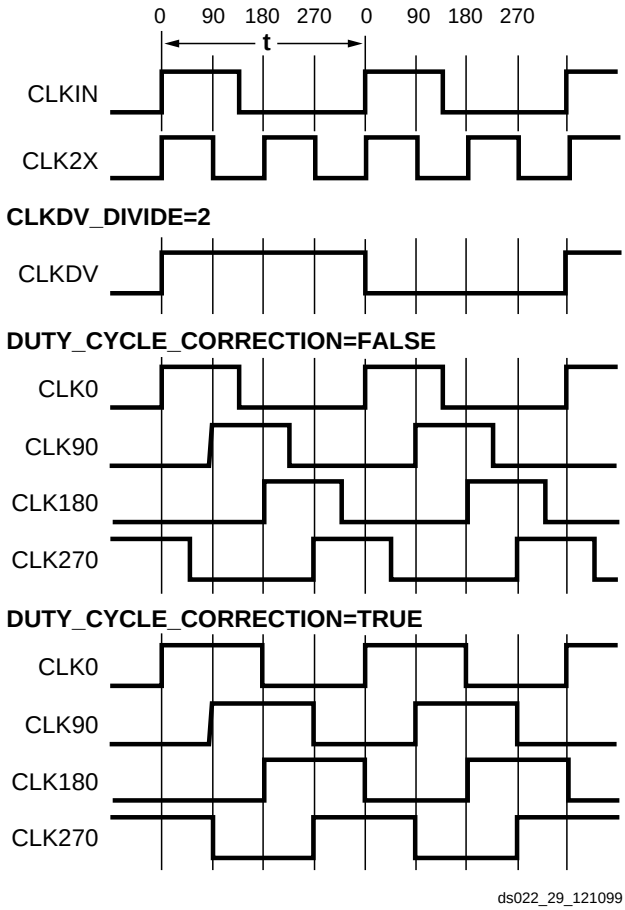


Figure 26: DLL Output Characteristics

The DLL provides duty cycle correction on all 1x clock outputs such that all 1x clock outputs by default have a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (TRUE by default), controls this feature. In order to deactivate the DLL duty cycle correction, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty cycle correction deactivates, the output clock has the same duty cycle as the source clock.

The DLL clock outputs can drive an OBUF, a BUFG, or they can route directly to destination clock pins. The DLL clock outputs can only drive the BUFGs that reside on the same edge (top or bottom).

Locked Output — LOCKED

In order to achieve lock, the DLL may need to sample several thousand clock cycles. After the DLL achieves lock the LOCKED signal activates. The DLL timing parameter section of the data sheet provides estimates for locking times.

In order to guarantee that the system clock is established prior to the device "waking up," the DLL can delay the completion of the device configuration process until after the DLL locks. The STARTUP_WAIT property activates this feature.

Until the LOCKED signal activates, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement. In particular the CLK2X output will appear as a 1x clock with a 25/75 duty cycle.

DLL Properties

Properties provide access to some of the Spartan-II family DLL features, (for example, clock division and duty cycle correction).

Duty Cycle Correction Property

The 1x clock outputs, CLK0, CLK90, CLK180, and CLK270, use the duty-cycle corrected default, exhibiting a 50/50 duty cycle. The DUTY_CYCLE_CORRECTION property (by default TRUE) controls this feature. To deactivate the DLL duty-cycle correction for the 1x clock outputs, attach the DUTY_CYCLE_CORRECTION=FALSE property to the DLL symbol. When duty-cycle correction deactivates, the output clock has the same duty cycle as the source clock.

Clock Divide Property

The CLKDV_DIVIDE property specifies how the signal on the CLKDV pin is frequency divided with respect to the CLK0 pin. The values allowed for this property are 1.5, 2, 2.5, 3, 4, 5, 8, or 16; the default value is 2.

Startup Delay Property

This property, STARTUP_WAIT, takes on a value of TRUE or FALSE (the default value). When TRUE the device configuration DONE signal waits until the DLL locks before going to High.

DLL Location Constraints

The DLLs are distributed such that there is one DLL in each corner of the device. The location constraint LOC, attached to the DLL symbol with the numeric identifier 0, 1, 2, or 3,

controls DLL location. The orientation of the four DLLs and their corresponding clock resources appears in Figure 27.

The LOC property uses the following form.

LOC = DLL2

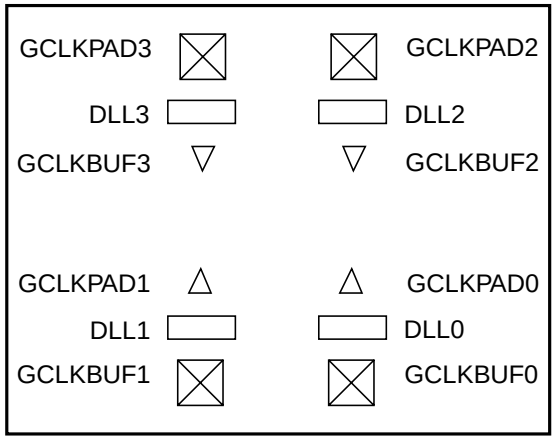


Figure 27: Orientation of DLLs

Design Factors

Use the following design considerations to avoid pitfalls and improve success designing with Xilinx devices.

Input Clock

The output clock signal of a DLL, essentially a delayed version of the input clock signal, reflects any instability on the input clock in the output waveform. For this reason the quality of the DLL input clock relates directly to the quality of the output clock waveforms generated by the DLL. The DLL input clock requirements are specified in the data sheet.

In most systems a crystal oscillator generates the system clock. The DLL can be used with any commercially available quartz crystal oscillator. For example, most crystal oscillators produce an output waveform with a frequency tolerance of 100 PPM, meaning 0.01 percent change in the clock period. The DLL operates reliably on an input waveform with a frequency drift of up to 1 ns — orders of magnitude in excess of that needed to support any crystal oscillator in the industry. However, the cycle-to-cycle jitter must be kept to less than 300 ps in the low frequencies and 150 ps for the high frequencies.

Input Clock Changes

Changing the period of the input clock beyond the maximum drift amount requires a manual reset of the CLKDLL. Failure to reset the DLL will produce an unreliable lock signal and output clock.

It is possible to stop the input clock with little impact to the DLL. Stopping the clock should be limited to less than 100 µs to keep device cooling to a minimum. The clock should be stopped during a Low phase, and when restored the full High period should be seen. During this time LOCKED will stay High and remain High when the clock is restored.

When the clock is stopped, one to four more clocks will still be observed as the delay line is flushed. When the clock is restarted, the output clocks will not be observed for one to four clocks as the delay line is filled. The most common case will be two or three clocks.

In a similar manner, a phase shift of the input clock is also possible. The phase shift will propagate to the output one to four clocks after the original shift, with no disruption to the CLKDLL control.

Output Clocks

As mentioned earlier in the DLL pin descriptions, some restrictions apply regarding the connectivity of the output pins. The DLL clock outputs can drive an OBUF, a global clock buffer BUFG, or they can route directly to destination clock pins. The only BUFGs that the DLL clock outputs can drive are the two on the same edge of the device (top or bottom). In addition, the CLK2X output of the secondary DLL can connect directly to the CLKIN of the primary DLL in the same quadrant.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

Useful Application Examples

The Spartan-II DLL can be used in a variety of creative and useful applications. The following examples show some of the more common applications.

Standard Usage

The circuit shown in Figure 28 resembles the BUFGDLL macro implemented to provide access to the RST and LOCKED pins of the CLKDLL.

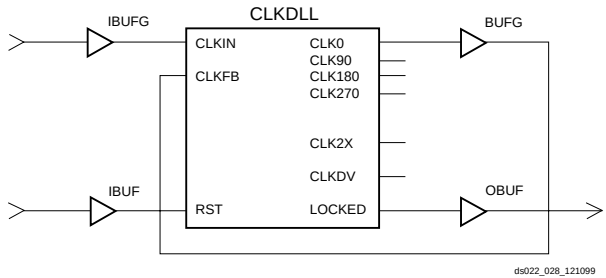


Figure 28: Standard DLL Implementation

Board Level De-skew of Multiple Non-Spartan-II Devices

The circuit shown in Figure 29 can be used to de-skew a system clock between a Spartan-II chip and other non-Spartan-II chips on the same board. This application is commonly used when the Spartan-II device is used in conjunction with other standard products such as SRAM or DRAM devices. While designing the board level route, ensure that the return net delay to the source equals the delay to the other chips involved.

Board-level de-skew is not required for low-fanout clock networks. It is recommended for systems that have fanout limitations on the clock network, or if the clock distribution chip cannot handle the load.

Do not use the DLL output clock signals until after activation of the LOCKED signal. Prior to the activation of the LOCKED signal, the DLL output clocks are not valid and can exhibit glitches, spikes, or other spurious movement.

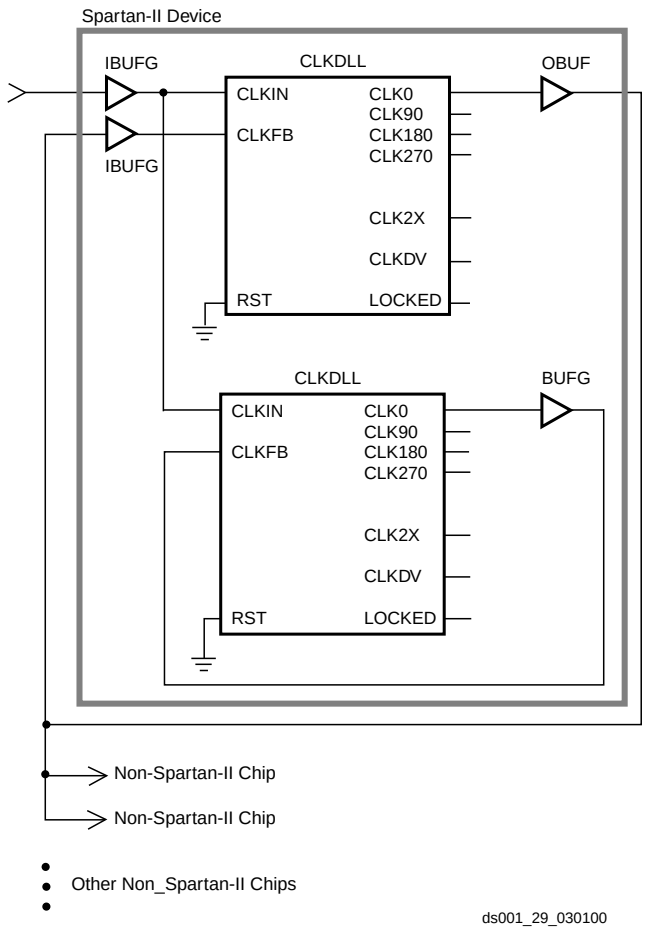


Figure 29: DLL De-skew of Board Level Clock

De-skew of Clock and Its 2x Multiple

The circuit shown in Figure 30 implements a 2x clock multiplier and also uses the CLK0 clock output with zero ns skew between registers on the same chip. A clock divider circuit could alternatively be implemented using similar connections.

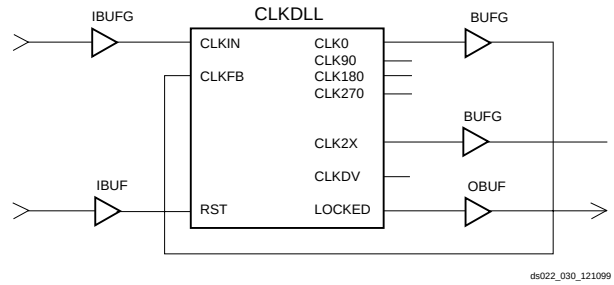


Figure 30: DLL De-skew of Clock and 2x Multiple

Because any single DLL can only access at most two BUFGs, any additional output clock signals must be routed from the DLL in this example on the high speed backbone routing.

Generating a 4x Clock

By connecting two DLL circuits each implementing a 2x clock multiplier in series as shown in Figure 31, a 4x clock multiply can be implemented with zero ns skew between registers in the same device.

If other clock output is needed, the clock could access a BUFG only if the DLLs are constrained to exist on opposite edges (Top or Bottom) of the device.

When using this circuit it is vital to use the SRL16 cell to reset the second DLL after the initial chip reset. If this is not done, the second DLL may not recognize the change of frequencies from when the input changes from a 1x (25/75) waveform to a 2x (50/50) waveform.

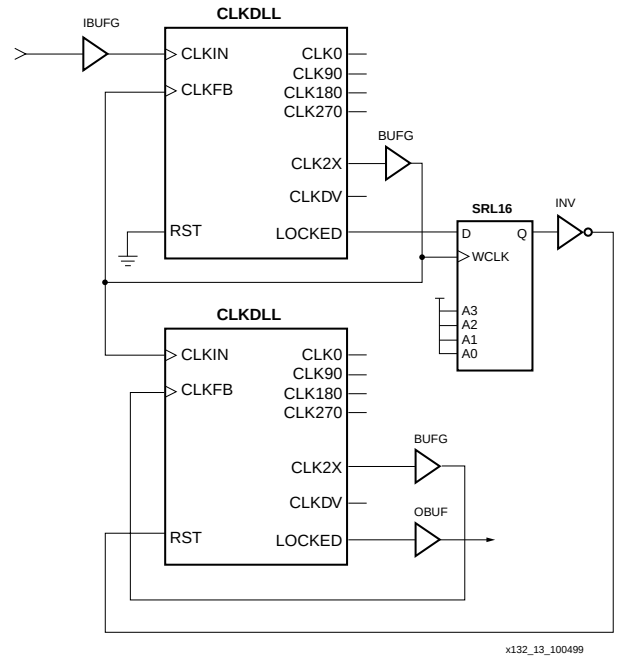


Figure 31: DLL Generation of 4x Clock

Using Block SelectRAM+ Features

The Spartan-II FPGA family provides dedicated blocks of on-chip, true dual-read/write port synchronous RAM, with 4096 memory cells. Each port of the Block SelectRAM+ memory can be independently configured as a read/write port, a read port, a write port, and can be configured to a specific data width. The Block SelectRAM+ memory offers new capabilities allowing the FPGA designer to simplify designs.

Operating Modes

Block SelectRAM+ memory supports two operating modes.

- Read Through
- Write Back

Read Through (one clock edge)

The read address is registered on the read port clock edge and data appears on the output after the RAM access time. Some memories may place the latch/register at the outputs depending on the desire to have a faster clock-to-out versus set-up time. This is generally considered to be an inferior solution since it changes the read operation to an asynchronous function with the possibility of missing an address/control line transition during the generation of the read pulse clock.

Write Back (one clock edge)

The write address is registered on the write port clock edge and the data input is written to the memory and mirrored on the write port input.

Block SelectRAM+ Characteristics

1. All inputs are registered with the port clock and have a set-up to clock timing specification.
2. All outputs have a read through or write back function depending on the state of the port WE pin. The outputs relative to the port clock are available after the clock-to-out timing specification.
3. The Block SelectRAMs are true SRAM memories and do not have a combinatorial path from the address to the output. The LUT SelectRAM+ cells in the CLBs are still available with this function.
4. The ports are completely independent from each other (*i.e.,* clocking, control, address, read/write function, and data width) without arbitration.
5. A write operation requires only one clock edge.
6. A read operation requires only one clock edge.

The output ports are latched with a self timed circuit to guarantee a glitch free read. The state of the output port will not change until the port executes another read or write operation.

Library Primitives

Figure 32 and Figure 33 show the two generic library Block SelectRAM+ primitives. Table 10 describes all of the available primitives for synthesis and simulation.

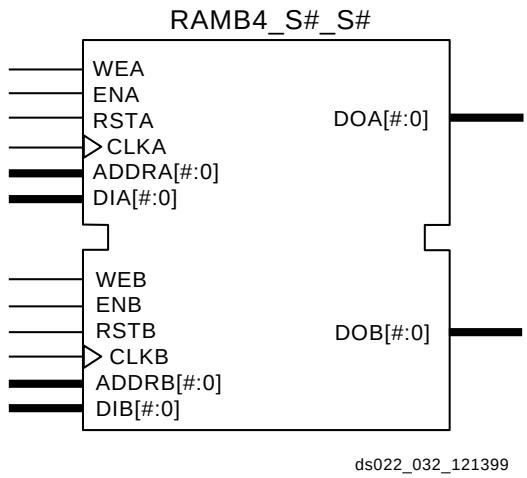


Figure 32: Dual-Port Block SelectRAM+ Memory

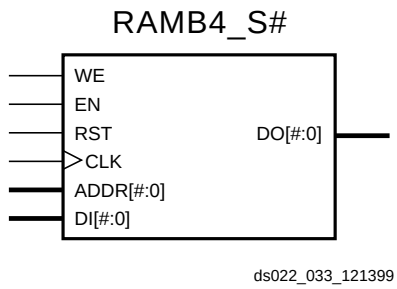


Figure 33: Single-Port Block SelectRAM+ Memory

Table 10: Available Library Primitives

Primitive	Port A Width	Port B Width
RAMB4_S1	1	N/A
RAMB4_S1_S1		1
RAMB4_S1_S2		2
RAMB4_S1_S4		4
RAMB4_S1_S8		8
RAMB4_S1_S16		16
RAMB4_S2	2	N/A
RAMB4_S2_S2		2
RAMB4_S2_S4		4
RAMB4_S2_S8		8
RAMB4_S2_S16		16
RAMB4_S4	4	N/A
RAMB4_S4_S4		4
RAMB4_S4_S8		8
RAMB4_S4_S16		16
RAMB4_S8	8	N/A
RAMB4_S8_S8		8
RAMB4_S8_S16		16
RAMB4_S16	16	N/A
RAMB4_S16_S16		16

Port Signals

Each Block SelectRAM+ port operates independently of the others while accessing the same set of 4096 memory cells.

Table 11 describes the depth and width aspect ratios for the Block SelectRAM+ memory.

Table 11: Block SelectRAM+ Port Aspect Ratios

Width	Depth	ADDR Bus	Data Bus
1	4096	ADDR<11:0>	DATA<0>
2	2048	ADDR<10:0>	DATA<1:0>
4	1024	ADDR<9:0>	DATA<3:0>
8	512	ADDR<8:0>	DATA<7:0>
16	256	ADDR<7:0>	DATA<15:0>

Clock—CLK[A|B]

Each port is fully synchronous with independent clock pins. All port input pins have setup time referenced to the port CLK pin. The data output bus has a clock-to-out time referenced to the CLK pin.

Enable—EN[A|B]

The enable pin affects the read, write and reset functionality of the port. Ports with an inactive enable pin keep the output pins in the previous state and do not write data to the memory cells.

Write Enable—WE[A|B]

Activating the write enable pin allows the port to write to the memory cells. When active, the contents of the data input bus are written to the RAM at the address pointed to by the address bus, and the new data also reflects on the data out bus. When inactive, a read operation occurs and the contents of the memory cells referenced by the address bus reflect on the data out bus.

Reset—RST[A|B]

The reset pin forces the data output bus latches to zero synchronously. This does not affect the memory cells of the RAM and does not disturb a write operation on the other port.

Address Bus—ADDR[A|B]<#:0>

The address bus selects the memory cells for read or write. The width of the port determines the required width of this bus as shown in Table 11.

Data In Bus—DI[A|B]<#:0>

The data in bus provides the new data value to be written into the RAM. This bus and the port have the same width, as shown in Table 11.

Data Output Bus—DO[A|B]<#:0>

The data out bus reflects the contents of the memory cells referenced by the address bus at the last active clock edge. During a write operation, the data out bus reflects the data in bus. The width of this bus equals the width of the port. The allowed widths appear in Table 11.

Inverting Control Pins

The four control pins (CLK, EN, WE and RST) for each port have independent inversion control as a configuration option.

Address Mapping

Each port accesses the same set of 4096 memory cells using an addressing scheme dependent on the width of the port. The physical RAM location addressed for a particular width are described in the following formula (of interest only when the two ports use different aspect ratios).

$$Start = ((ADDR_{port} + 1) * Width_{port}) - 1$$

$$End = ADDR_{port} * Width_{port}$$

Table 12 shows low order address mapping for each port width.

Table 12: Port Address Mapping

Port Width	Port Addresses															
1	4095...	15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
2	2047...	07		06		05		04		03		02		01		00	
4	1023...	03				02				01				00			
8	511...	01								00							
16	255...	00															

Creating Larger RAM Structures

The Block SelectRAM+ columns have specialized routing to allow cascading blocks together with minimal routing delays. This achieves wider or deeper RAM structures with a smaller timing penalty than when using normal routing channels.

Location Constraints

Block SelectRAM+ instances can have LOC properties attached to them to constrain the placement. The Block SelectRAM+ placement locations are separate from the CLB location naming convention, allowing the LOC properties to transfer easily from array to array.

The LOC properties use the following form.

LOC = RAMB4_R#C#

RAMB4_R0C0 is the upper left RAMB4 location on the device.

Conflict Resolution

The Block SelectRAM+ memory is a true dual-read/write port RAM that allows simultaneous access of the same memory cell from both ports. When one port writes to a given memory cell, the other port must not address that memory cell (for a write or a read) within the clock-to-clock setup window. The following lists specifics of port and memory cell write conflict resolution.

- If both ports write to the same memory cell simultaneously, violating the clock-to-clock setup requirement, consider the data stored as invalid.
- If one port attempts a read of the same memory cell the other simultaneously writes, violating the clock-to-clock setup requirement, the following occurs.
  - The write succeeds
  - The data out on the writing port accurately reflects the data written.
  - The data out on the reading port is invalid.

Conflicts do not cause any physical damage.

Single Port Timing

Figure 34 shows a timing diagram for a single port of a Block SelectRAM+ memory. The Block SelectRAM+ AC switching characteristics are specified in the data sheet. The Block SelectRAM+ memory is initially disabled.

At the first rising edge of the CLK pin, the ADDR, DI, EN, WE, and RST pins are sampled. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location, 0x00, as indicated by the ADDR bus.

At the second rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN and WE pins are High indicating a write operation. The DO bus mirrors the DI bus. The DI bus is written to the memory location 0x0F.

At the third rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is High and the WE pin is Low indicating a read operation. The DO bus contains the contents of the memory location 0x7E as indicated by the ADDR bus.

At the fourth rising edge of the CLK pin, the ADDR, DI, EN, WR, and RST pins are sampled again. The EN pin is Low indicating that the Block SelectRAM+ memory is now disabled. The DO bus retains the last value.

Dual Port Timing

Figure 35 shows a timing diagram for a true dual-port read/write Block SelectRAM+ memory. The clock on port A has a longer period than the clock on Port B. The timing parameter T_{BCCS}, (clock-to-clock set-up) is shown on this diagram. The parameter, T_{BCCS} is violated once in the diagram. All other timing parameters are identical to the single port version shown in Figure 34.

T_{BCCS} is only of importance when the address of both ports are the same and at least one port is performing a write operation. When the clock-to-clock set-up parameter is violated for a WRITE-WRITE condition, the contents of the memory at that location will be invalid. When the clock-to-clock set-up parameter is violated for a WRITE-READ condition, the contents of the memory will be correct, but the read port will have invalid data. At the first rising edge of the CLKA, memory location 0x00 is to be written with the value 0xAAAA and is mirrored on the DOA bus. The last operation of Port B was a read to the same memory location 0x00. The DOB bus of Port B does not change with the new value on Port A, and retains the last read value. A short time later, Port B executes another read to memory location 0x00, and the DOB bus now reflects the new memory value written by Port A.

At the second rising edge of CLKA, memory location 0x7E is written with the value 0x9999 and is mirrored on the DOA bus. Port B then executes a read operation to the same memory location without violating the T_{BCCS} parameter and the DOB reflects the new memory values written by Port A.

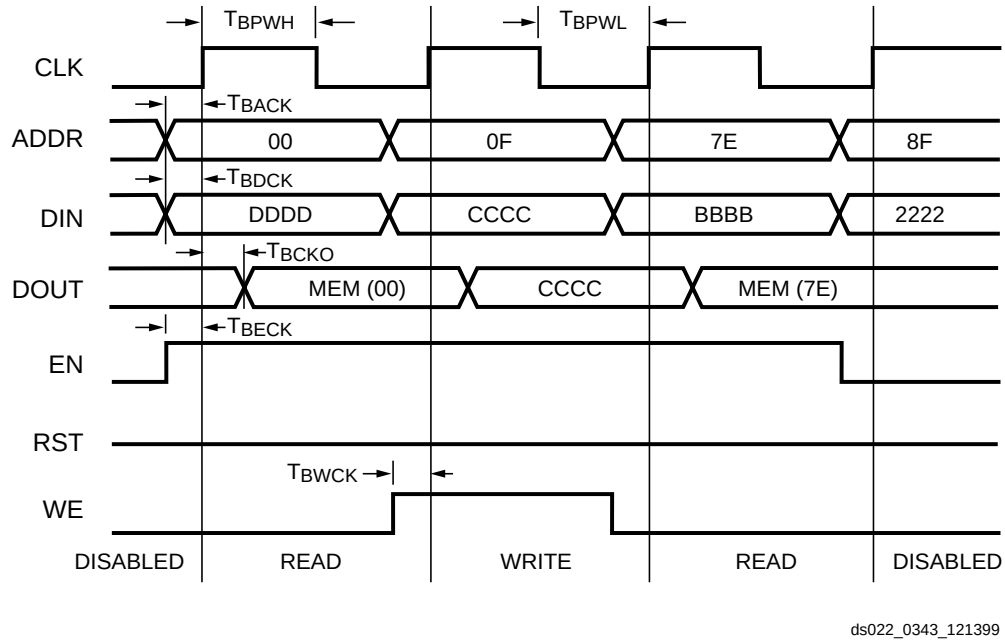


Figure 34: Timing Diagram for Single Port Block SelectRAM+ Memory

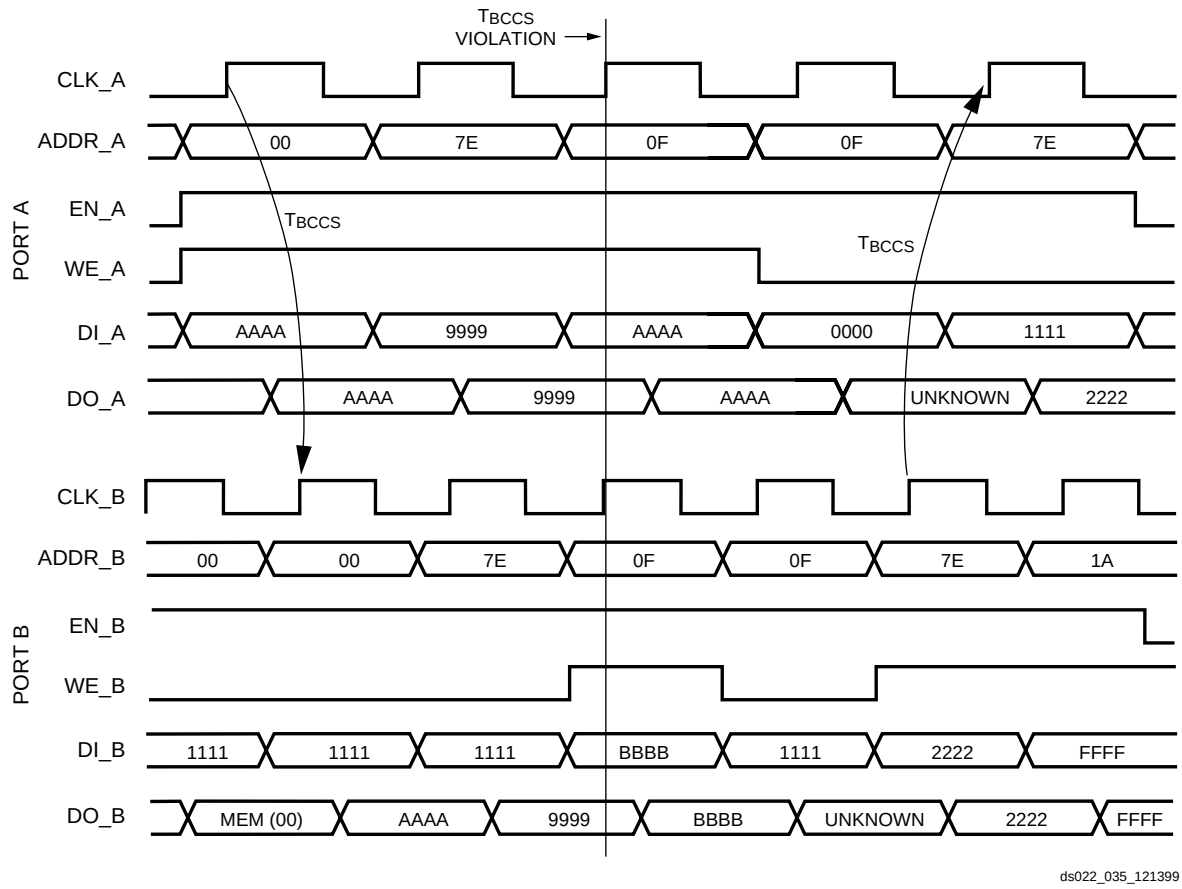


Figure 35: Timing Diagram for a True Dual-port Read/Write Block SelectRAM+ Memory

At the third rising edge of CLKA, the T_{BCCS} parameter is violated with two writes to memory location 0x0F. The DOA and DOB busses reflect the contents of the DIA and DIB busses, but the stored value at 0x7E is invalid.

At the fourth rising edge of CLKA, a read operation is performed at memory location 0x0F and invalid data is present on the DOA bus. Port B also executes a read operation to memory location 0x0F and also reads invalid data.

At the fifth rising edge of CLKA a read operation is performed that does not violate the T_{BCCS} parameter to the previous write of 0x7E by Port B. THe DOA bus reflects the recently written value by Port B.

Initialization

The Block SelectRAM+ memory can initialize during the device configuration sequence. The 16 initialization properties of 64 hex values each (a total of 4096 bits) set the initialization of each RAM. These properties appear in Table 13. Any initialization properties not explicitly set configure as zeros. Partial initialization strings pad with zeros. Initialization strings greater than 64 hex values generate an error. The RAMs can be simulated with the initialization values using generics in VHDL simulators and parameters in Verilog simulators.

Initialization in VHDL and Synopsys

The Block SelectRAM+ structures may be initialized in VHDL for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the VHDL code uses a generic to pass the initialization. Synopsys FPGA compiler does not presently support generics. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the generic statements. The following code illustrates a module that employs these techniques.

Table 13: RAM Initialization Properties

Property	Memory Cells
INIT_00	255 to 0
INIT_01	511 to 256
INIT_02	767 to 512
INIT_03	1023 to 768
INIT_04	1279 to 1024
INIT_05	1535 to 1280
INIT_06	1791 to 2047
INIT_07	2047 to 1792
INIT_08	2303 to 2048
INIT_09	2559 to 2304
INIT_0a	2815 to 2560
INIT_0b	3071 to 2816
INIT_0c	3327 to 3072
INIT_0d	3583 to 3328
INIT_0e	3839 to 3584
INIT_0f	4095 to 3840

Initialization in Verilog and Synopsys

The Block SelectRAM+ structures may be initialized in Verilog for both simulation and synthesis for inclusion in the EDIF output file. The simulation of the Verilog code uses a defparam to pass the initialization. The Synopsys FPGA compiler does not presently support defparam. The initialization values instead attach as attributes to the RAM by a built-in Synopsys dc_script. The translate_off statement stops synthesis translation of the defparam statements. The following code illustrates a module that employs these techniques.

Design Examples

Creating a 32-bit Single-Port RAM

The true dual-read/write port functionality of the Block SelectRAM+ memory allows a single port, 128 deep by 32-bit wide RAM to be created using a single Block SelectRAM+ cell as shown in Table 36.

Interleaving the memory space, setting the LSB of the address bus of Port A to 1 (V_{CC}), and the LSB of the address bus of Port B to 0 (GND), allows a 32-bit wide single port RAM to be created.

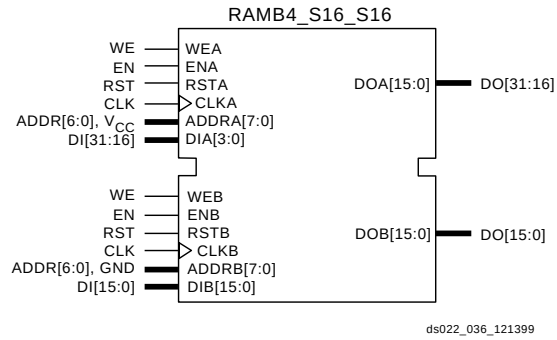


Figure 36: Single Port 128 x 32 RAM

Creating Two Single-Port RAMs

The true dual-read/write port functionality of the Block SelectRAM+ memory allows a single RAM to be split into two single port memories of 2K bits each as shown in Figure 37.

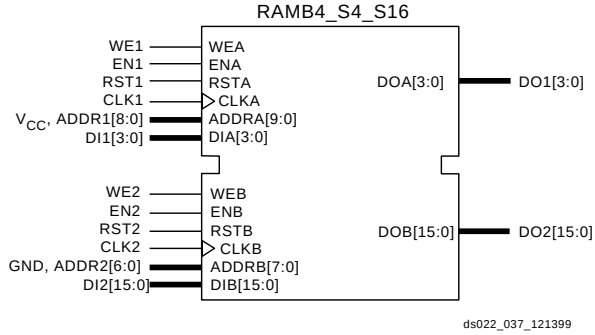


Figure 37: 512 x 4 RAM and 128 x 16 RAM

In this example, a 512K x 4 RAM (Port A) and a 128 x 16 RAM (Port B) are created out of a single Block SelectRAM+. The address space for the RAM is split by fixing the MSB of Port A to 1 (V_{CC}) for the upper 2K bits and the MSB of Port B to 0 (GND) for the lower 2K bits.

Block Memory Generation

The CoreGen program generates memory structures using the Block SelectRAM+ features. This program outputs VHDL or Verilog simulation code templates and an EDIF file for inclusion in a design.

VHDL Initialization Example

```
library IEEE;
use IEEE.std_logic_1164.all;

entity MYMEM is
port (CLK, WE:in std_logic;
ADDR: in std_logic_vector(8 downto 0);
DIN: in std_logic_vector(7 downto 0);
DOUT: out std_logic_vector(7 downto 0));
end MYMEM;

architecture BEHAVE of MYMEM is
signal logic0, logic1: std_logic;

component RAMB4_S8
--synopsys translate_off
generic( INIT_00,INIT_01, INIT_02, INIT_03, INIT_04, INIT_05, INIT_06, INIT_07,
INIT_08, INIT_09, INIT_0a, INIT_0b, INIT_0c, INIT_0d, INIT_0e, INIT_0f : BIT_VECTOR(255
downto 0)
:= X"0000000000000000000000000000000000000000000000000000000000000000");
--synopsys translate_on
port (WE, EN, RST, CLK: in STD_LOGIC;
ADDR: in STD_LOGIC_VECTOR(8 downto 0);
DI: in STD_LOGIC_VECTOR(7 downto 0);
DO: out STD_LOGIC_VECTOR(7 downto 0));
end component;

--synopsys dc_script_begin
--set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
--set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
--synopsys dc_script_end

begin
logic0 <='0';
logic1 <='1';

ram0: RAMB4_S8
--synopsys translate_off
generic map (

INIT_00 => X"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF",
INIT_01 => X"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210")
--synopsys translate_on
port map (WE=>WE, EN=>logic1, RST=>logic0, CLK=>CLK,ADDR=>ADDR, DI=>DIN, DO=>DOUT);

end BEHAVE;
```

Verilog Initialization Example

```
module MYMEM (CLK, WE, ADDR, DIN, DOUT);
input CLK, WE;
input [8:0] ADDR;
input [7:0] DIN;
output [7:0] DOUT;

wire logic0, logic1;

//synopsys dc_script_begin
//set_attribute ram0 INIT_00
"0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF" -type string
//set_attribute ram0 INIT_01
"FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210" -type string
//synopsys dc_script_end

assign logic0 = 1'b0;
assign logic1 = 1'b1;

RAMB4_S8 ram0 (.WE(WE), .EN(logic1), .RST(logic0), .CLK(CLK), .ADDR(ADDR), .DI(DIN),
.DO(DOUT));
//synopsys translate_off
defparam ram0.INIT_00 =
256h'0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF0123456789ABCDEF;
defparam ram0.INIT_01 =
256h'FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210FEDCBA9876543210;
//synopsys translate_on
endmodule
```

Using Versatile I/O

The Spartan-II FPGA family includes a highly configurable, high-performance I/O resource, called Versatile I/O to provide support for a wide variety of I/O standards. The Versatile I/O resource is a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and Versatile I/O features and the design considerations described in this document can improve and simplify system level design.

Introduction

As FPGAs continue to grow in size and capacity, the larger and more complex systems designed for them demand an increased variety of I/O standards. Furthermore, as system clock speeds continue to increase, the need for high performance I/O becomes more important. While chip-to-chip delays have an increasingly substantial impact on overall system speed, the task of achieving the desired system performance becomes more difficult with the proliferation of low-voltage I/O standards. Versatile I/O, the revolutionary input/output resources of Spartan-II devices, has resolved this potential problem by providing a highly configurable, high-performance alternative to the I/O resources of more conventional programmable devices. The Spartan-II Versatile I/O features combine the flexibility and time-to-market advantages of programmable logic with the high performance previously available only with ASICs and custom ICs.

Each Versatile I/O block can support up to 20 I/O standards. Supporting such a variety of I/O standards allows the support of a wide variety of applications, from general purpose standard applications to high-speed low-voltage memory busses.

Versatile I/O blocks also provide selectable output drive strengths and programmable slew rates for the LVTTL output buffers, as well as an optional, programmable weak pull-up, weak pull-down, or weak "keeper" circuit ideal for use in external bussing applications.

Each Input/Output Block (IOB) includes three registers, one each for the input, output, and 3-state signals within the IOB. These registers are optionally configurable as either a D-type flip-flop or as a level sensitive latch.

The input buffer has an optional delay element used to guarantee a zero hold time requirement for input signals registered within the IOB.

The Versatile I/O features also provide dedicated resources for input reference voltage (V_{REF}) and output source voltage (V_{CCO}), along with a convenient banking system that simplifies board design.

By taking advantage of the built-in features and wide variety of I/O standards supported by the Versatile I/O features,

system-level design and board design can be greatly simplified and improved.

Fundamentals

Modern bus applications, pioneered by the largest and most influential companies in the digital electronics industry, are commonly introduced with a new I/O standard tailored specifically to the needs of that application. The bus I/O standards provide specifications to other vendors who create products designed to interface with these applications. Each standard often has its own specifications for current, voltage, I/O buffering, and termination techniques.

The ability to provide the flexibility and time-to-market advantages of programmable logic is increasingly dependent on the capability of the programmable logic device to support an ever increasing variety of I/O standards

The Versatile I/O resources feature highly configurable input and output buffers which provide support for a wide variety of I/O standards. As shown in Table 14, each buffer type can support a variety of voltage requirements.

Table 14: Supported I/O Standards

I/O Standard	Output V_{CCO}	Input V_{CCO}	Input V_{REF}	Board Termination Voltage (V_{TT})
LVTTL	3.3	3.3	N/A	N/A
LVCMOS2	2.5	2.5	N/A	N/A
SSTL3 I & II	3.3	N/A	1.50	1.50
SSTL2 I & II	2.5	N/A	1.25	1.25
GTL	N/A	N/A	0.80	1.20
GTL+	N/A	N/A	1.0	1.50
HSTL I	1.5	N/A	0.75	0.75
HSTL III & IV	1.5	N/A	0.90	1.50
CTT	3.3	N/A	1.50	1.50
AGP-2X	3.3	N/A	1.32	N/A
PCI33_3	3.3	3.3	N/A	N/A
PCI33_5	3.3	3.3	N/A	N/A
PCI66_3	3.3	3.3	N/A	N/A

Overview of Supported I/O Standards

This section provides a brief overview of the I/O standards supported by all Spartan-II devices.

While most I/O standards specify a range of allowed voltages, this document records typical voltage values only. Detailed information on each specification may be found on the Electronic Industry Alliance Jedec website at: http://www.jedec.org

LVTTL — Low-Voltage TTL

The Low-Voltage TTL, or LVTTL standard is a general purpose EIA/JESDSA standard for 3.3V applications that uses an LVTTL input buffer and a Push-Pull output buffer. This standard requires a 3.3V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a termination voltage (V_{TT}).

LVCMOS2 — Low-Voltage CMOS for 2.5V

The Low-Voltage CMOS for 2.5V or lower, or LVCMOS2 standard is an extension of the LVCMOS standard (JESD 8.5) used for general purpose 2.5V applications. This standard requires a 2.5V output source voltage (V_{CCO}), but does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}).

PCI — Peripheral Component Interface

The Peripheral Component Interface, or PCI standard specifies support for both 33 MHz and 66 MHz PCI bus applications. It uses a LVTTL input buffer and a Push-Pull output buffer. This standard does not require the use of a reference voltage (V_{REF}) or a board termination voltage (V_{TT}), however, it does require a 3.3V output source voltage (V_{CCO}). I/Os configured for the PCI, 33 MHz, 5V standard are also 5V-tolerant.

GTL — Gunning Transceiver Logic Terminated

The Gunning Transceiver Logic, or GTL standard is a high-speed bus standard (JESD8.3) invented by Xerox. Xilinx has implemented the terminated variation for this standard. This standard requires a differential amplifier input buffer and a Open Drain output buffer.

GTL+ — Gunning Transceiver Logic Plus

The Gunning Transceiver Logic Plus, or GTL+ standard is a high-speed bus standard (JESD8.3) first used by the Pentium Pro processor.

HSTL — High-Speed Transceiver Logic

The High-Speed Transceiver Logic, or HSTL standard is a general purpose high-speed, 1.5V bus standard sponsored by IBM (EIA/JESD 8-6). This standard has four variations or classes. Versatile I/O devices support Class I, III, and IV. This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

SSTL3 — Stub Series Terminated Logic for 3.3V

The Stub Series Terminated Logic for 3.3V, or SSTL3 standard is a general purpose 3.3V memory bus standard also sponsored by Hitachi and IBM (JESD8-8). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL3 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

SSTL2 — Stub Series Terminated Logic for 2.5V

The Stub Series Terminated Logic for 2.5V, or SSTL2 standard is a general purpose 2.5V memory bus standard sponsored by Hitachi and IBM (JESD8-9). This standard has two classes, I and II. Versatile I/O devices support both classes for the SSTL2 standard. This standard requires a Differential Amplifier input buffer and an Push-Pull output buffer.

CTT — Center Tap Terminated

The Center Tap Terminated, or CTT standard is a 3.3V memory bus standard sponsored by Fujitsu (JESD8-4). This standard requires a Differential Amplifier input buffer and a Push-Pull output buffer.

AGP-2X — Advanced Graphics Port

The Intel AGP standard is a 3.3V Advanced Graphics Port-2X bus standard used with the Pentium II processor for graphics applications. This standard requires a Push-Pull output buffer and a Differential Amplifier input buffer.

Library Symbols

The Xilinx library includes an extensive list of symbols designed to provide support for the variety of Versatile I/O features. Most of these symbols represent variations of the five generic Versatile I/O symbols.

- IBUF (input buffer)
- IBUFG (global clock input buffer)
- OBUF (output buffer)
- OBUFT (3-state output buffer)
- IOBUF (input/output buffer)

IBUF

Signals used as inputs to the Spartan-II device must source an input buffer (IBUF) via an external input port. The generic IBUF symbol appears in Figure 38. The extension to the base name defines which I/O standard the IBUF uses. The assumed standard is LVTTL when the generic IBUF has no specified extension.

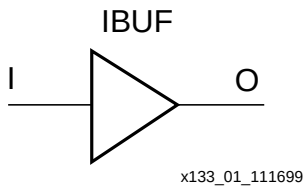


Figure 38: Input Buffer (IBUF) Symbols

The following list details the variations of the IBUF symbol:

- IBUF
- IBUF_LVCMOS2
- IBUF_PCI33_3
- IBUF_PCI33_5
- IBUF_PCI66_3
- IBUF_GTL
- IBUF_GTLP
- IBUF_HSTL_I
- IBUF_HSTL_III
- IBUF_HSTL_IV
- IBUF_SSTL3_I
- IBUF_SSTL3_II
- IBUF_SSTL2_I
- IBUF_SSTL2_II
- IBUF_CTT
- IBUF_AGP

When the IBUF symbol supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V-tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V-tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUF placement restrictions require that any differential amplifier input signals within a bank be of the same standard. How to specify a specific location for the IBUF via the LOC property is described below. Table 15 summarizes the input standards compatibility requirements.

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element by default activates to ensure a zero hold-time requirement. The NODELAY=TRUE property overrides this default.

When the IBUF does not drive a flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

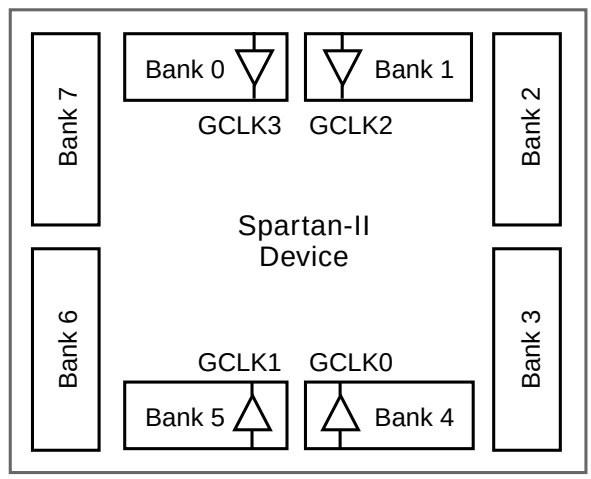


Figure 39: I/O Banks

Table 15: Xilinx Input Standards Compatibility Requirements

Rule 1	All differential amplifier input signals within a bank are required to be of the same standard.
Rule 2	There are no placement restrictions for inputs with standards that require a single-ended input buffer.

IBUFG

Signals used as high fanout clock inputs to the Spartan-II device should drive a global clock input buffer (IBUFG) via an external input port in order to take advantage of one of the four dedicated global clock distribution networks. The output of the IBUFG symbol can only drive a CLKDLL, CLKDLLHF, or a BUFG symbol. The generic IBUFG symbol appears in Figure 40.

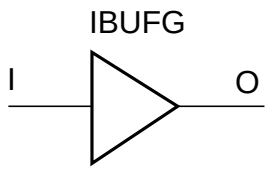


Figure 40: Global Clock Input Buffer (IBUFG) Symbol

The extension to the base name determines which I/O standard is used by the IBUFG. With no extension specified for the generic IBUFG symbol, the assumed standard is LVTTL.

The following list details variations of the IBUFG symbol.

- IBUFG
- IBUFG_LVCMOS2
- IBUFG_PCI33_3
- IBUFG_PCI33_5
- IBUFG_PCI66_3
- IBUFG_GTL
- IBUFG_GTLP
- IBUFG_HSTL_I
- IBUFG_HSTL_III
- IBUFG_HSTL_IV
- IBUFG_SSTL3_I
- IBUFG_SSTL3_II
- IBUFG_SSTL2_I
- IBUFG_SSTL2_II
- IBUFG_CTT
- IBUFG_AGP

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 39 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

IBUFG placement restrictions require any differential amplifier input signals within a bank be of the same standard. The LOC property can specify a location for the IBUFG.

As an added convenience, the BUFGP can be used to instantiate a high fanout clock input. The BUFGP symbol represents a combination of the LVTTL IBUFG and BUFG symbols, such that the output of the BUFGP can connect directly to the clock pins throughout the design.

The Spartan-II BUFGP symbol can only be placed in a global clock pad location. The LOC property can specify a location for the BUFGP.

OBUF

An OBUF must drive outputs through an external output port. The generic output buffer (OBUF) symbol appears in Figure 41.

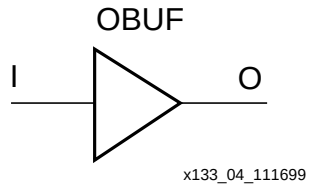


Figure 41: Output Buffer (OBUF) Symbol

The extension to the base name defines which I/O standard the OBUF uses. With no extension specified for the generic OBUF symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL output buffers have selectable drive strengths.

The format for LVTTL OBUF symbol names is as follows.

OBUF_<slew_rate>_<drive_strength>

<slew_rate> is either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

The following list details variations of the OBUF symbol.

- OBUF
- OBUF_S_2
- OBUF_S_4
- OBUF_S_6
- OBUF_S_8
- OBUF_S_12
- OBUF_S_16
- OBUF_S_24
- OBUF_F_2
- OBUF_F_4
- OBUF_F_6
- OBUF_F_8
- OBUF_F_12
- OBUF_F_16

- OBUF_F_24
- OBUF_LVCMOS2
- OBUF_PCI33_3
- OBUF_PCI33_5
- OBUF_PCI66_3
- OBUF_GTL
- OBUF_GTLP
- OBUF_HSTL_I
- OBUF_HSTL_III
- OBUF_HSTL_IV
- OBUF_SSTL3_I
- OBUF_SSTL3_II
- OBUF_SSTL2_I
- OBUF_SSTL2_II
- OBUF_CTT
- OBUF_AGP

OBUF placement restrictions require that within a given V_{CCO} bank each OBUF share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within any V_{CCO} bank. Table 16 summarizes the output compatibility requirements. The LOC property can specify a location for the OBUF.

Table 16: Output Standards Compatibility Requirements

Rule 1	Only outputs with standards which share compatible V_{CCO} may be used within the same bank.
Rule 2	There are no placement restrictions for outputs with standards that do not require a V_{CCO}.
V_{CCO}	Compatible Standards
3.3	LVTTL, SSTL3_I, SSTL3_II, CTT, AGP, GTL, GTL+, PCI33_3, PCI66_3
2.5	SSTL2_I, SSTL2_II, LVCMOS2, GTL, GTL+
1.5	HSTL_I, HSTL_III, HSTL_IV, GTL, GTL+

OBUFT

The generic 3-state output buffer OBUFT, shown in Figure 42, typically implements 3-state outputs or bidirectional I/O.

The extension to the base name defines which I/O standard OBUFT uses. With no extension specified for the generic OBUFT symbol, the assumed standard is slew rate limited LVTTL with 12 mA drive strength.

The LVTTL OBUFT additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL 3-state output buffers have selectable drive strengths.

The format for LVTTL OBUFT symbol names is as follows.

OBUFT_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

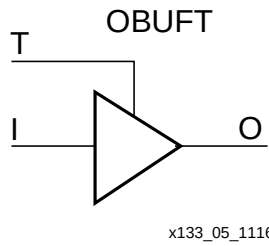


Figure 42: 3-State Output Buffer Symbol (OBUFT)

The following list details variations of the OBUFT symbol.

- OBUFT
- OBUFT_S_2
- OBUFT_S_4
- OBUFT_S_6
- OBUFT_S_8
- OBUFT_S_12
- OBUFT_S_16
- OBUFT_S_24
- OBUFT_F_2
- OBUFT_F_4
- OBUFT_F_6
- OBUFT_F_8
- OBUFT_F_12
- OBUFT_F_16
- OBUFT_F_24
- OBUFT_LVCMOS2
- OBUFT_PCI33_3
- OBUFT_PCI33_5
- OBUFT_PCI66_3
- OBUFT_GTL
- OBUFT_GTLP
- OBUFT_HSTL_I
- OBUFT_HSTL_III
- OBUFT_HSTL_IV
- OBUFT_SSTL3_I
- OBUFT_SSTL3_II
- OBUFT_SSTL2_I
- OBUFT_SSTL2_II
- OBUFT_CTT
- OBUFT_AGP

The Versatile I/O OBUFT placement restrictions require that within a given V_{CCO} bank each OBUFT share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank.

The LOC property can specify a location for the OBUFT.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the

appropriate symbol to the output net of the OBUFT (PULLUP, PULLDOWN, or KEEPER).

The weak "keeper" circuit requires the input buffer within the IOB to sample the I/O signal. So, OBUFTs programmed for an I/O standard that requires a V_{REF} have automatic placement of a V_{REF} in the bank with an OBUFT configured with a weak "keeper" circuit. This restriction does not affect most circuit design as applications using an OBUFT configured with a weak "keeper" typically implement a bidirectional I/O. In this case the IBUF (and the corresponding V_{REF}) are explicitly placed.

The LOC property can specify a location for the OBUFT.

IOBUF

Use the IOBUF symbol for bidirectional signals that require both an input buffer and a 3-state output buffer with an active high 3-state pin. The generic input/output buffer IOBUF appears in Figure 43.

The extension to the base name defines which I/O standard the IOBUF uses. With no extension specified for the generic IOBUF symbol, the assumed standard is LVTTL input buffer and slew rate limited LVTTL with 12 mA drive strength for the output buffer.

The LVTTL IOBUF additionally can support one of two slew rate modes to minimize bus transients. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals.

LVTTL bidirectional buffers have selectable output drive strengths.

The format for LVTTL IOBUF symbol names is as follows.

IOBUF_<slew_rate>_<drive_strength>

<slew_rate> can be either F (Fast), or S (Slow) and <drive_strength> is specified in milliamps (2, 4, 6, 8, 12, 16, or 24).

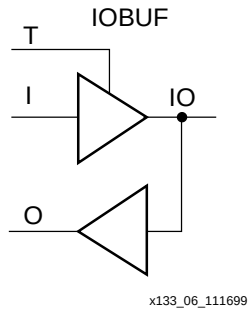


Figure 43: Input/Output Buffer Symbol (IOBUF)

The following list details variations of the IOBUF symbol.

- IOBUF
- IOBUF_S_2
- IOBUF_S_4
- IOBUF_S_6
- IOBUF_S_8
- IOBUF_S_12
- IOBUF_S_16
- IOBUF_S_24
- IOBUF_F_2
- IOBUF_F_4
- IOBUF_F_6
- IOBUF_F_8
- IOBUF_F_12
- IOBUF_F_16
- IOBUF_F_24
- IOBUF_LVCMOS2
- IOBUF_PCI33_3
- IOBUF_PCI33_5
- IOBUF_PCI66_3
- IOBUF_GTL
- IOBUF_GTLP
- IOBUF_HSTL_I
- IOBUF_HSTL_III
- IOBUF_HSTL_IV
- IOBUF_SSTL3_I
- IOBUF_SSTL3_II
- IOBUF_SSTL2_I
- IOBUF_SSTL2_II
- IOBUF_CTT
- IOBUF_AGP

When the IOBUF symbol supports an I/O standard such as LVTTL, LVCMOS, or PCI33_5, the IBUF automatically configures as a 5V-tolerant input buffer unless the V_{CCO} for the bank is less than 2V. If the single-ended IBUF is placed in a bank with an HSTL standard (V_{CCO} < 2V), the input buffer is not 5V-tolerant.

The voltage reference signal is "banked" within the Spartan-II device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 39 on page 38 for a representation of the Spartan-II I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Additional restrictions on the Versatile I/O IOBUF placement require that within a given V_{CCO} bank each IOBUF must share the same output source drive voltage. Input buffers of any type and output buffers that do not require V_{CCO} can be placed within the same V_{CCO} bank. The LOC property can specify a location for the IOBUF.

An optional delay element is associated with the input path in each IOBUF. When the IOBUF drives an input flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Override this default with the NODELAY=TRUE property.

In the case when the IOBUF does not drive an input flip-flop within the IOB, the delay element de-activates by default to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

3-state output buffers and bidirectional buffers can have either a weak pull-up resistor, a weak pull-down resistor, or a weak "keeper" circuit. Control this feature by adding the appropriate symbol to the output net of the IOBUF (PULLUP, PULLDOWN, or KEEPER).

Versatile I/O Properties

Access to some of the Versatile I/O features (for example, location constraints, input delay, output drive strength, and slew rate) is available through properties associated with these features.

Input Delay Properties

An optional delay element is associated with each IBUF. When the IBUF drives a flip-flop within the IOB, the delay element activates by default to ensure a zero hold-time requirement. Use the NODELAY=TRUE property to override this default.

In the case when the IBUF does not drive a flip-flop within the IOB, the delay element by default de-activates to provide higher performance. To delay the input signal, activate the delay element with the DELAY=TRUE property.

IOB Flip-Flop/Latch Property

The I/O Block (IOB) includes an optional register on the input path, an optional register on the output path, and an optional register on the 3-state control pin. The design implementation software automatically takes advantage of these registers when the following option for the Map program is specified.

map -pr b <filename>

Alternatively, the IOB = TRUE property can be placed on a register to force the mapper to place the register in an IOB.

Location Constraints

Specify the location of each Versatile I/O symbol with the location constraint LOC attached to the Versatile I/O symbol. The external port identifier indicates the value of the location constrain. The format of the port identifier depends on the package chosen for the specific design.

The LOC properties use the following form.

LOC=A42

LOC=P37

Output Slew Rate Property

As mentioned above, a variety of symbol names provide the option of choosing the desired slew rate for the output buffers. In the case of the LVTTL output buffers (OBUF, OBUFT, and IOBUF), slew rate control can be alternatively programed with the SLEW= property. By default, the slew rate for each output buffer is reduced to minimize power bus transients when switching non-critical signals. The SLEW= property has one of the two following values.

SLEW=SLOW

SLEW=FAST

Output Drive Strength Property

The desired output drive strength can be additionally specified by choosing the appropriate library symbol. The Xilinx library also provides an alternative method for specifying this feature. For the LVTTL output buffers (OBUF, OBUFT, and IOBUF, the desired drive strength can be specified with the DRIVE= property. This property could have one of the following seven values.

DRIVE=2

DRIVE=4

DRIVE=6

DRIVE=8

DRIVE=12 (Default)

DRIVE=16

DRIVE=24

Design Considerations

Reference Voltage (V_{REF}) Pins

Low-voltage I/O standards with a differential amplifier input buffer require an input reference voltage (V_{REF}). Provide the V_{REF} as an external signal to the device.

The voltage reference signal is "banked" within the device on a half-edge basis such that for all packages there are eight independent V_{REF} banks internally. See Figure 39 on page 38 for a representation of the I/O banks. Within each bank approximately one of every six I/O pins is automatically configured as a V_{REF} input.

Within each V_{REF} bank, any input buffers that require a V_{REF} signal must be of the same type. Output buffers of any type and input buffers can be placed without requiring a reference voltage within the same V_{REF} bank.

Output Drive Source Voltage (V_{CCO}) Pins

Many of the low voltage I/O standards supported by Versatile I/Os require a different output drive source voltage (V_{CCO}). As a result each device can often have to support multiple output drive source voltages.

The V_{CCO} supplies are internally tied together for some packages. The VQ100 and the PQ208 provide one combined V_{CCO} supply. The TQ144 and the CS144 packages provide four independent V_{CCO} supplies. The FG256 and the FG456 provide eight independent V_{CCO} supplies.

Output buffers within a given V_{CCO} bank must share the same output drive source voltage. Input buffers for LVTTL, LVCMOS2, PCI33_3, and PCI 66_3 use the V_{CCO} voltage for Input V_{CCO} voltage.

Transmission Line Effects

The delay of an electrical signal along a wire is dominated by the rise and fall times when the signal travels a short dis-

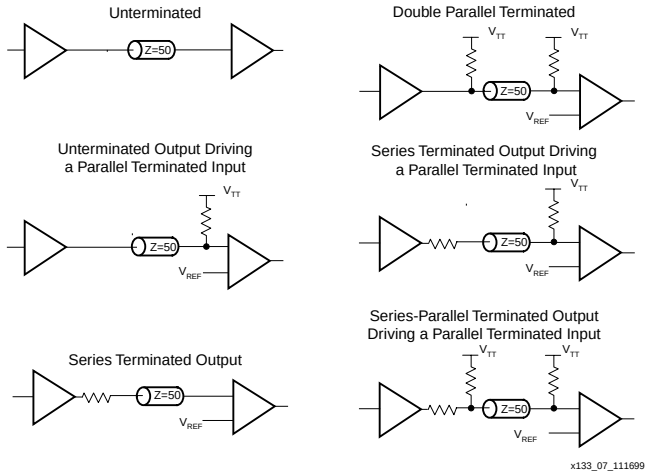


Figure 44: Overview of Standard Input and Output Termination Methods

tance. Transmission line delays vary with inductance and capacitance, but a well-designed board can experience delays of approximately 180 ps per inch.

Transmission line effects, or reflections, typically start at 1.5" for fast (1.5 ns) rise and fall times. Poor (or non-existent) termination or changes in the transmission line impedance cause these reflections and can cause additional delay in longer traces. As system speeds continue to increase, the effect of I/O delays can become a limiting factor and therefore transmission line termination becomes increasingly more important.

Termination Techniques

A variety of termination techniques reduce the impact of transmission line effects.

The following lists output termination techniques.

None
Series
Parallel (Shunt)
Series and Parallel (Series-Shunt)

Input termination techniques include the following.

None
Parallel (Shunt)

These termination techniques can be applied in any combination. A generic example of each combination of termination methods appears in Figure 44.

Simultaneous Switching Guidelines

Ground bounce can occur with high-speed digital ICs when multiple outputs change states simultaneously, causing undesired transient behavior on an output, or in the internal logic. This problem is also referred to as the Simultaneous Switching Output (SSO) problem.

Ground bounce is primarily due to current changes in the combined inductance of ground pins, bond wires, and ground metallization. The IC internal ground level deviates from the external system ground level for a short duration (a few nanoseconds) after multiple outputs change state simultaneously.

Ground bounce affects stable Low outputs and all inputs because they interpret the incoming signal by comparing it to the internal ground. If the ground bounce amplitude exceeds the actual instantaneous noise margin, then a non-changing input can be interpreted as a short pulse with a polarity opposite to the ground bounce.

Table 17 provides the guidelines for the maximum number of simultaneously switching outputs allowed per output power/ground pair to avoid the effects of ground bounce. Refer to Table 18 for the number of effective output power/ground pairs for each Spartan-II device and package combination..

Table 17: Guidelines for Max. Number of Simultaneously Switching Outputs per Power/Ground Pair

Standard	Package	
	CS, FG	PQ, TQ, VQ
LVTTL Slow Slew Rate, 2 mA drive	68	36
LVTTL Slow Slew Rate, 4 mA drive	41	20
LVTTL Slow Slew Rate, 6 mA drive	29	15
LVTTL Slow Slew Rate, 8 mA drive	22	12
LVTTL Slow Slew Rate, 12 mA drive	17	9
LVTTL Slow Slew Rate, 16 mA drive	14	7
LVTTL Slow Slew Rate, 24 mA drive	9	5
LVTTL Fast Slew Rate, 2 mA drive	40	21
LVTTL Fast Slew Rate, 4 mA drive	24	12
LVTTL Fast Slew Rate, 6 mA drive	17	9
LVTTL Fast Slew Rate, 8 mA drive	13	7
LVTTL Fast Slew Rate, 12 mA drive	10	5
LVTTL Fast Slew Rate, 16 mA drive	8	4
LVTTL Fast Slew Rate, 24 mA drive	5	3
LVCMOS2	10	5
PCI	8	4
GTL	4	4
GTL+	4	4
HSTL Class I	18	9
HSTL Class III	9	5
HSTL Class IV	5	3
SSTL2 Class I	15	8
SSTL2 Class II	10	5
SSTL3 Class I	11	6
SSTL3 Class II	7	4
CTT	14	7
AGP	9	5

Note: This analysis assumes a 35 pF load for each output.

Table 18: Effective Output Power/Ground Pairs for Spartan-II Devices

Package	Spartan-II Devices				
	XC2S15	XC2S30	XC2S50	XC2S100	XC2S150
VQ100	8	8	-	-	-
CS144	12	12	-	-	-
TQ144	12	12	12	12	-
PQ208	-	16	16	16	16
FG256	-	-	16	16	16
FG456	-	-	-	48	48

Application Examples

Creating a design with the Versatile I/O features requires the instantiation of the desired library symbol within the design code. At the board level, designers need to know the termination techniques required for each I/O standard.

This section describes some common application examples illustrating the termination techniques recommended by each of the standards supported by the Versatile I/O features.

Termination Examples

Circuit examples involving typical termination techniques for each of the Versatile I/O standards follow. For a full range of accepted values for the DC voltage specifications for each standard, refer to the table associated with each figure.

The resistors used in each termination technique example and the transmission lines depicted represent board level components and are not meant to represent components on the device.

GTL

A sample circuit illustrating a valid termination technique for GTL is shown in Figure 45. Table 19 lists DC voltage specifications.

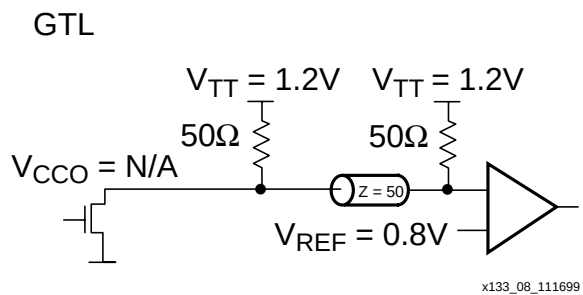


Figure 45: Terminated GTL

Table 19: GTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	N/A	-
$V_{REF} = N \times V_{TT}$[1]	0.74	0.8	0.86
V_{TT}	1.14	1.2	1.26
$V_{IH} = V_{REF} + 0.05$	0.79	0.85	-
$V_{IL} = V_{REF} - 0.05$	-	0.75	0.81
V_{OH}	-	-	-
V_{OL}	-	0.2	0.4
I_{OH} at V_{OH}(mA)	-	-	-
I_{OL}at V_{OL}(mA) at 0.4V	32	-	-
I_{OL}at V_{OL}(mA) at 0.2V	-	-	40

Note 1: N must be greater than or equal to 0.653 and less than or equal to 0.68.

GTL+

A sample circuit illustrating a valid termination technique for GTL+ appears in Figure 46. DC voltage specifications appear in Table 20.

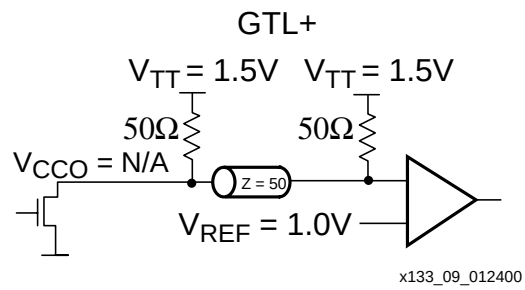


Figure 46: Terminated GTL+

Table 20: GTL+ Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	-	-	-
$V_{REF} = N \times V_{TT}$ [1]	0.88	1.0	1.12
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.1$	0.98	1.1	-
$V_{IL} = V_{REF} – 0.1$	-	0.9	1.02
V_{OH}	-	-	-
V_{OL}	0.3	0.45	0.6
I_{OH} at V_{OH} (mA)	-	-	-
I_{OL}at V_{OL} (mA) at 0.6V	36	-	-
I_{OL}at V_{OL} (mA) at 0.3V	-	-	48

Note 1: N must be greater than or equal to 0.653 and less than or equal to 0.68.

HSTL

A sample circuit illustrating a valid termination technique for HSTL_I appears in Figure 47. A sample circuit illustrating a valid termination technique for HSTL_III appears in Figure 48.

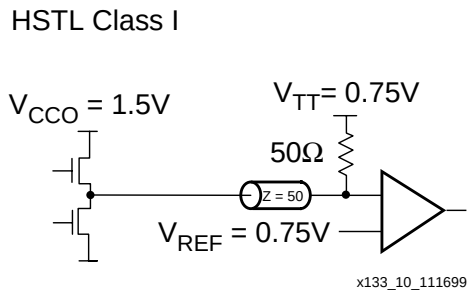


Figure 47: Terminated HSTL Class I

Table 21: HSTL Class I Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	0.68	0.75	0.90
V_{TT}	-	$V_{CCO} \times 0.5$	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	$V_{REF} – 0.1$
V_{OH}	$V_{CCO} – 0.4$	-	-
V_{OL}			0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

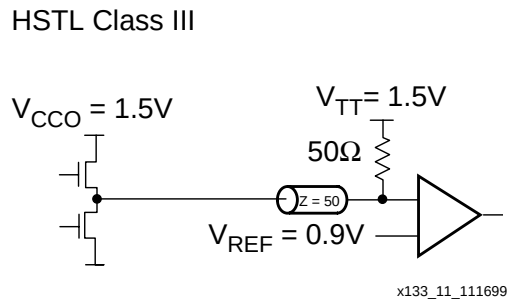


Figure 48: Terminated HSTL Class III

Table 22: HSTL Class III Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF} (1)	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	$V_{REF} – 0.1$
V_{OH}	$V_{CCO} – 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	24	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user."

A sample circuit illustrating a valid termination technique for HSTL_IV appears in Figure 49.

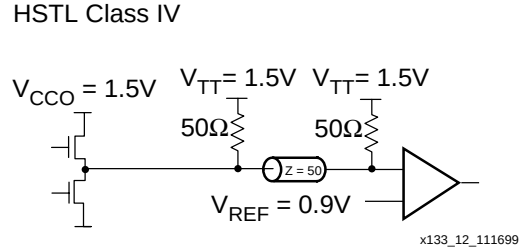


Figure 49: Terminated HSTL Class IV

Table 23: HSTL Class IV Voltage Specification

Parameter	Min	Typ	Max
V_{CCO}	1.40	1.50	1.60
V_{REF}	-	0.90	-
V_{TT}	-	V_{CCO}	-
V_{IH}	V_{REF} + 0.1	-	-
V_{IL}	-	-	$V_{REF} – 0.1$
V_{OH}	$V_{CCO} – 0.4$	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	48	-	-

Note: Per EIA/JESD8-6, "The value of V_{REF} is to be selected by the user to provide optimum noise margin in the use conditions specified by the user.

SSTL3_I

A sample circuit illustrating a valid termination technique for SSTL3_I appears in Figure 50. DC voltage specifications appear in Table 24.

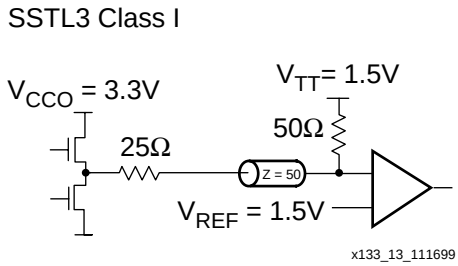


Figure 50: Terminated SSTL3 Class I

Table 24: SSTL3_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	**3.0**	**3.3**	**3.6**
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.6$	1.9	-	-
$V_{OL} = V_{REF} – 0.6$	-	-	1.1
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes
1: V_{IH} maximum is V_{CCO} + 0.3
2: V_{IL} minimum does not conform to the formula

SSTL3_II

A sample circuit illustrating a valid termination technique for SSTL3_II appears in Figure 51. DC voltage specifications appear in Table 25.

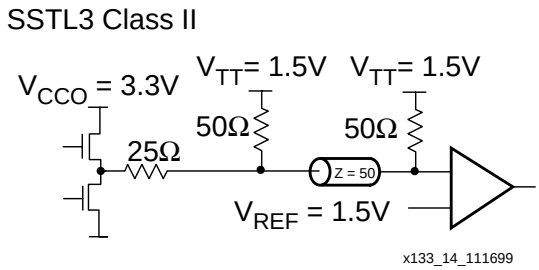


Figure 51: Terminated SSTL3 Class II

Table 25: SSTL3_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = 0.45 \times V_{CCO}$	1.3	1.5	1.7
$V_{TT} = V_{REF}$	1.3	1.5	1.7
$V_{IH} = V_{REF} + 0.2$	1.5	1.7	3.9(1)
$V_{IL} = V_{REF} – 0.2$	–0.3(2)	1.3	1.5
$V_{OH} = V_{REF} + 0.8$	2.1	-	-
$V_{OL} = V_{REF} – 0.8$	-	-	0.9
I_{OH} at V_{OH} (mA)	–16	-	-
I_{OL}at V_{OL} (mA)	16	-	-

Notes
1: V_{IH} maximum is V_{CCO} + 0.3
2: V_{IL} minimum does not conform to the formula

SSTL2_I

A sample circuit illustrating a valid termination technique for SSTL2_I appears in Figure 52. DC voltage specifications appear in Table 26.

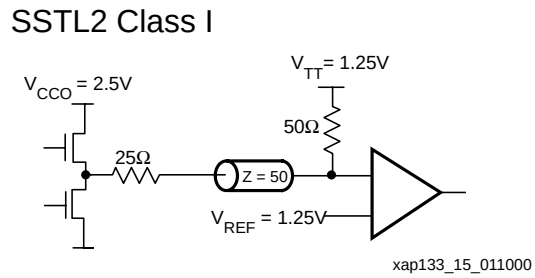


Figure 52: Terminated SSTL2 Class I

Table 26: SSTL2_I Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.61$	1.76	-	-
$V_{OL} = V_{REF} – 0.61$	-	-	0.74
I_{OH} at V_{OH} (mA)	–7.6	-	-
I_{OL}at V_{OL} (mA)	7.6	-	-

Notes
1: N must be greater than or equal to -0.04 and less than or equal to 0.04.
2: V_{IH} maximum is V_{CCO} + 0.3.
3: V_{IL} minimum does not conform to the formula.

SSTL2_II

A sample circuit illustrating a valid termination technique for SSTL2_II appears in Figure 53. DC voltage specifications appear in Table 27.

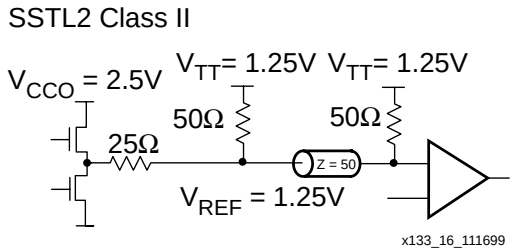


Figure 53: Terminated SSTL2 Class II

Table 27: SSTL2_II Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
$V_{REF} = 0.5 \times V_{CCO}$	1.15	1.25	1.35
$V_{TT} = V_{REF} + N$(1)	1.11	1.25	1.39
$V_{IH} = V_{REF} + 0.18$	1.33	1.43	3.0(2)
$V_{IL} = V_{REF} – 0.18$	–0.3(3)	1.07	1.17
$V_{OH} = V_{REF} + 0.8$	1.95	-	-
$V_{OL} = V_{REF}$ - 0.8	-	-	0.55
I_{OH} at V_{OH} (mA)	–15.2	-	-
I_{OL}at V_{OL} (mA)	15.2	-	-

Notes:
1. N must be greater than or equal to -0.04 and less than or equal to 0.04.
2. V_{IH} maximum is V_{CCO} + 0.3.
3. V_{IL} minimum does not conform to the formula.

CTT

A sample circuit illustrating a valid termination technique for CTT appear in Figure 54. DC voltage specifications appear in Table 28.

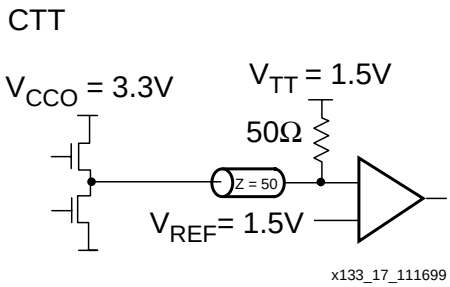


Figure 54: Terminated CTT

Table 28: CTT Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.05(1)	3.3	3.6
V_{REF}	1.35	1.5	1.65
V_{TT}	1.35	1.5	1.65
$V_{IH} = V_{REF} + 0.2$	1.55	1.7	-
$V_{IL} = V_{REF} – 0.2$	-	1.3	1.45
$V_{OH} = V_{REF} + 0.4$	1.75	1.9	-
$V_{OL}= V_{REF} – 0.4$	-	1.1	1.25
I_{OH} at V_{OH} (mA)	–8	-	-
I_{OL}at V_{OL} (mA)	8	-	-

Notes:
1: Timing delays are calculated based on V_{CCO} min of 3.0V.

PCI33_3 and PCI66_3

PCI33_3 or PCI66_3 require no termination. DC voltage specifications appear in Table 29.

Table 29: PCI33_3 and PCI66_3 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
$V_{IH} = 0.5 \times V_{CCO}$	1.5	1.65	V_{CCO}+ 0.5
$V_{IL} = 0.3 \times V_{CCO}$	–0.5	0.99	1.08
$V_{OH} = 0.9 \times V_{CCO}$	2.7	-	-
$V_{OL}= 0.1 \times V_{CCO}$	-	-	0.36
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL}at V_{OL} (mA)	Note 1	-	-

Note 1: Tested according to the relevant specification.

PCI33_5

PCI33_5 requires no termination. DC voltage specifications appear in Table 30.

Table 30: PCI33_5 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.425	1.5	5.5
V_{IL}	–0.5	1.0	1.05
V_{OH}	2.4	-	-
V_{OL}	-	-	0.55
I_{OH} at V_{OH} (mA)	Note 1	-	-
I_{OL}at V_{OL} (mA)	Note 1	-	-

Note 1: Tested according to the relevant specification.

LVTTL

LVTTL requires no termination. DC voltage specifications appears in Table 31.

Table 31: LVTTL Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	2.0	-	3.6
V_{IL}	–0.5	-	0.8
V_{OH}	2.4	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–24	-	-
I_{OL}at V_{OL} (mA)	24	-	-

Note: $V_{OL}$and V_{OH} for lower drive currents sample tested.

LVCMOS2

LVCMOS2 requires no termination. DC voltage specifications appear in Table 32.

Table 32: LVCMOS2 Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	2.3	2.5	2.7
V_{REF}	-	-	-
V_{TT}	-	-	-
V_{IH}	1.7	-	3.6
V_{IL}	–0.5	-	0.7
V_{OH}	1.9	-	-
V_{OL}	-	-	0.4
I_{OH} at V_{OH} (mA)	–12	-	-
I_{OL}at V_{OL} (mA)	12	-	-

AGP-2X

The specification for the AGP-2X standard does not document a recommended termination technique. DC voltage specifications appear in Table 33.

Table 33: AGP-2X Voltage Specifications

Parameter	Min	Typ	Max
V_{CCO}	3.0	3.3	3.6
$V_{REF} = N \times V_{CCO}$ (1)	1.17	1.32	1.48
V_{TT}	-	-	-
$V_{IH} = V_{REF} + 0.2$	1.37	1.52	-
$V_{IL} = V_{REF} – 0.2$	-	1.12	1.28
$V_{OH} = 0.9 \times V_{CCO}$	2.7	3.0	-
$V_{OL} = 0.1 \times V_{CCO}$	-	0.33	0.36
I_{OH} at V_{OH} (mA)	Note 2	-	-
I_{OL}at V_{OL} (mA)	Note 2	-	-

Notes:
1: N must be greater than or equal to 0.39 and less than or equal to 0.41.
2: Tested according to the relevant specification.

Spartan-II DC Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the a.c. parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-II Absolute Maximum Ratings

Symbol	Description		Value	Units
V_{CCINT}	Supply voltage relative to GND		–0.5 to 3.0	V
V_{CCO}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{REF}	Input Reference Voltage		–0.5 to 3.6	V
V_{IN}	Input voltage relative to GND	Using V_{REF}	–0.5 to 3.6	V
		Internal threshold	–0.5 to 5.5	V
V_{TS}	Voltage applied to 3-state output		–0.5 to 5.5	V
V_{CC}	Longest Supply Voltage Rise Time from 1V to 2.375V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temp. (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature		+125	°C

Notes: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
Power supplies may turn on in any order.
For extended periods (e.g., longer than a day), V_{IN} should not exceed V_{CCO} by more that 3.6V.

Spartan-II Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CCINT}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial	2.5 – 5%	2.5 + 5%	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	2.5 – 5%	2.5 + 5%	V
V_{CCO}	Supply voltage relative to GND, T_J = 0 °C to +85°C	Commercial		3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial		3.6	V
T_{IN}	Input signal transition time			250	ns

Notes: Correct operation is guaranteed with a minimum V_{CCINT} of 2.25V (Nominal V_{CCINT} –10%). Below the minimum value stated above, all delay parameters increase by 3% for each 50 mV reduction in V_{CCINT} below the specified range.
At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

Spartan-II DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{DRINT}	Data Retention V_{CCINT} Voltage (below which configuration data may be lost)		2.0		V
V_{DRIO}	Data Retention V_{CCO} Voltage (below which configuration data may be lost)		1.2		V
I_{CCINTQ}	Quiescent V_{CCINT} supply current (Note 1)				mA
I_{CCOQ}	Quiescent V_{CCO} supply current (Note 1)				mA
I_{REF}	V_{REF} current per V_{REF} pin			20	µA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)	BGA, PQ, HQ, packages		8	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V, V_{CCO} = 3.3V (sample tested)		Note 2	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.6V (sample tested)		Note 2	0.15	mA

Note 1: With no output current loads, no active input pull-up resistors, all I/O pins 3-stated and floating.
Note 2: Internal pull-up and pull-down resistors guarantee valid logic levels at unconnected input pins. These pull-up and pull-down resistors do not guarantee valid logic levels when input pins are connected to other circuits.

Spartan-II DC Input and Output levels

Values for V_{IL} and V_{IH} are recommended input voltages. Values for V_{OL} and V_{OH} are guaranteed output voltages over the recommended operating conditions. Only selected standards are tested. These are chosen to ensure that all standards meet their specifications. The selected standards are tested at minimum V_{CCO} with the respective I_{OL} and I_{OH} currents shown. Other standards are sample tested.

Input/Output Standard	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}
	V, min	V, max	V, min	V, max	V, Max	V, Min	mA	mA
LVTTL (Note 1)	–0.5	0.8	2.0	5.5	0.4	2.4	24	–24
LVCMOS2	–0.5	0.7	1.7	5.5	0.4	1.9	12	–12
PCI, 3.3 V	–0.5	44% V_{CCINT}	60% V_{CCINT}	V_{CCO} + 0.5	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2
PCI, 5.0 V	–0.5	0.8	2.0	5.5	0.55	2.4	Note 2	Note 2
GTL	–0.5	V_{REF} – 0.05	V_{REF} + 0.05	3.6	0.4	n/a	40	n/a
GTL+	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.6	n/a	36	n/a
HSTL I	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	8	–8
HSTL III	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	24	–8
HSTL IV	–0.5	V_{REF} – 0.1	V_{REF} + 0.1	3.6	0.4	V_{CCO} – 0.4	48	–8
SSTL3 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.6	V_{REF} + 0.6	8	–8
SSTL3 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.8	V_{REF} + 0.8	16	–16
SSTL2 I	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.50	V_{REF} + 0.50	7.6	–7.6
SSTL2 II	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.50	V_{REF} + 0.50	15.2	–15.2
CTT	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	V_{REF} – 0.4	V_{REF} + 0.4	8	–8
AGP	–0.5	V_{REF} – 0.2	V_{REF} + 0.2	3.6	10% V_{CCO}	90% V_{CCO}	Note 2	Note 2

Note 1: V_{OL} and V_{OH} for lower drive currents are sample tested.
Note 2: Tested according to the relevant specifications.

Spartan-II Switching Characteristics

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-II devices unless otherwise noted.

Spartan-II IOB Input Switching Characteristics

Input delays associated with the pad are specified for LVTTL levels. For other standards, these delays typically vary by less than 0.3 ns. Precise values are provided by the timing analyzer.

			Speed Grade		
Description		**Symbol**	**-6**	**-5**	**Units**
Propagation Delays					
Pad to I output, no delay	All	T_{IOPI}		1.0	ns, max
Pad to I output, with delay	XC2S15	T_{IOPID}		1.7	ns, max
	XC2S30			1.7	ns, max
	XC2S50			1.7	ns, max
	XC2S100			1.8	ns, max
	XC2S150			1.8	ns, max
Pad to output IQ via transparent latch, no delay	All	T_{IOPLI}		2.2	ns, max
Pad to output IQ via transparent latch, with delay	XC2S15	T_{IOPLID}		4.0	ns, max
	XC2S30			4.0	ns, max
	XC2S50			4.2	ns, max
	XC2S100			4.3	ns, max
	XC2S150			4.3	ns, max
Sequential Delays					
Clock CLK to output IQ		T_{IOCKIQ}		1.4	ns, max
Setup and Hold Times with respect to Clock CLK		Setup/Hold Time			
Pad, no delay		T_{IOPICK}/T_{IOICKP}		2.5/0.0	ns, min
Pad, with delay (Note 1)		$T_{IOPICKD}/T_{IOICKPD}$		4.7–0.5	ns, min
ICE input		$T_{IOICECK}/T_{IOCKICE}$		1.0/0.0	ns, min
SR input (IFF, synchronous)		$T_{IOSRCKI}/T_{IOCKISR}$		1.1/0.0	ns, min
Set/Reset Delays					
SR input to IQ (asynchronous)		T_{IOSRIQ}		1.6	ns, max
GSR to output IQ		T_{GSRQ}		13.0	ns, max

Note 1: With delay, the IOB hold time is negative. This reduces or eliminates pad-to-pad hold time.

Spartan-II IOB Output Switching Characteristics

Output delays terminating at a pad are specified for LVTTL with 12 mA drive and slow slew rate, the default output standard. For other standards, adjust the delays by adding the values shown. *Tri-state turn-off delays should not be adjusted*.

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Propagation Delays				
O input to Pad	T_{IOOP}		6.1	ns, max
O input to Pad via transparent latch	T_{IOOLP}		6.4	ns, max
3-State Delays				
T input to Pad high-impedance	T_{IOTHZ}		1.5	ns, max
T input to valid data on Pad	T_{IOTON}		6.6	ns, max
T input to Pad high-impedance via transparent latch	$T_{IOTLPHZ}$		2.2	ns, max
T input to valid data on Pad via transparent latch	$T_{IOTLPON}$		6.6	ns, max
GTS to Pad high impedance	T_{GTS}		6.7	ns, max
Sequential Delays				
Clock CLK to Pad	T_{IOCKP}		7.7	ns, max
Clock CLK to Pad high-impedance (synchronous)	T_{IOCKHZ}		2.8	ns, max
Clock CLK to valid data on Pad (synchronous)	T_{IOCKON}		7.7	ns, max
Setup Times before Clock CLK				
O input	T_{IOOCK}		0.6	ns, min
OCE input	$T_{IOOCECK}$		1.0	ns, min
SR input (OFF)	$T_{IOSRCKO}$		1.1	ns, min
3-State Setup Times				
TCE input	$T_{IOTCECK}$		1.0	ns, min
T input	T_{IOTCK}		0.3	ns, min
SR input (TFF)	$T_{IOSRCKT}$		1.1	ns, min
Hold Times after Clock CLK				
All Hold Times		0.0	0.0	ns, min
Set/Reset Delays				
SR input to Pad (asynchronous)	T_{IOSRP}		6.6	ns, max
SR input to Pad high-impedance (asynchronous)	T_{IOSRHZ}		3.0	ns, max
SR input to valid data on Pad (asynchronous)	T_{IOSRON}		7.9	ns, max
GSR to Pad	T_{GSRQ}		13.0	ns, max
Output Delay Adjustments				
Standard-specific increments for delays terminating at pads (based on standard capacitive load, Csl)	LVTTL, Slow,2 mA		17.5	ns
	4 mA		7.6	ns
	6 mA		4.0	ns
	8 mA		1.6	ns
	12 mA		0.0	ns
	16 mA		–0.3	ns
	24 mA		–0.8	ns
	LVTTL, Fast,2 mA		15.3	ns
	4 mA		4.7	ns
	6 mA		1.7	ns
	8 mA		–1.2	ns
	12 mA		–2.5	ns
	16 mA		–2.7	ns
	24 mA		–3.0	ns
	LVCMOS2		–2.7	ns
	PCI, 33 MHz, 3.3V		0.4	ns
	PCI, 33 MHz, 5.0V		–1.2	ns
	PCI, 66 MHz, 3.3V		–3.6	ns
	GTL		–3.5	ns
	GTL+		–2.5	ns
	HSTL I		–3.7	ns
	HSTL III		–3.7	ns
	HSTL IV		–3.9	ns
	SSTL3 I		–3.3	ns
	SSTL3 II		–3.9	ns
	SSTL2 I		–3.2	ns
	SSTL2 II		–3.7	ns
	CTT		–3.4	ns
	AGP		–3.8	ns

Calculation of T_{op} as a Function of Capacitance

The values for T_{opsl} were based on the standard capacitive load (Csl) for each IO standard as listed in Table 34.

For other capacitive loads, use the formulas below to calculate the corresponding T_{op}:

$T_{op} = T_{opsl} + (C_{load} – C_{sl}) * fl$

Where:

T_{opsl} is the T_{op} reported above in the Output Delay Adjustment section.
C_{load} is the capacitive load for the design.

Table 34: Constants for Use in Calculation of T_{op}

Standard	Csl (pF)	fl (ns/pF)
LVCMOS2	35	0.041
LVTTL Fast Slew Rate, 2 mA drive	35	0.41
LVTTL Fast Slew Rate, 4 mA drive	35	0.20
LVTTL Fast Slew Rate, 6 mA drive	35	0.13
LVTTL Fast Slew Rate, 8 mA drive	35	0.079
LVTTL Fast Slew Rate, 12 mA drive	35	0.048
LVTTL Fast Slew Rate, 16 mA drive	35	0.043
LVTTL Fast Slew Rate, 24 mA drive	35	0.033
LVTTL Slow Slew Rate, 2 mA drive	35	0.41
LVTTL Slow Slew Rate, 4 mA drive	35	0.20
LVTTL Slow Slew Rate, 6 mA drive	35	0.14
LVTTL Slow Slew Rate, 8 mA drive	35	0.086
LVTTL Slow Slew Rate, 12 mA drive	35	0.058
LVTTL Slow Slew Rate, 16 mA drive	35	0.053
LVTTL Slow Slew Rate, 24 mA drive	35	0.44
HSTL Class I	20	0.022
HSTL Class III	20	0.016
HSTL Class IV	20	0.014
SSTL2 Class I	30	0.028
SSTL2 Class II	30	0.016
SSTL3 Class I	30	0.029
SSTL3 Class II	30	0.016
CTT	20	0.035
AGP	10	0.037
GTL	0	0.014
GTL+	0	0.017
PCI 33MHz, 5V	50	0.050
PCI 33MHZ, 3V	10	0.050
PCI 66 MHz, 3V	10	0.033

Spartan-II Pad-to-Pad Switching Characteristics

Output delays terminating at the pad are specified for LVTTL levels with 12 mA drive and slow slew rate (the default output standard). For other standards, these delays must be adjusted by adding the values shown in the Spartan-II IOB Output Switching Characteristics table on page 52.

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Using a DLL				
Pad-to-pad input data setup time before the clock Pad-to-pad input data hold time after the clock Pad-to-pad delay from clock input to data output				ns, min ns, min ns, max
Without a DLL				
Pad-to-pad input data setup time before the clock Pad-to-pad input data hold time after the clock Pad-to-pad delay from clock input to data output		Note 1	Note 1	ns, min ns, min ns, max

Note 1: These dfelays may be calculated by adding the Clock-to-Pad delay from the Spartan-II IOB Input Switching Characteristics table on page 51 to the GCLK-pad-to-flip-flop delay shown in the Spartan-II Clock Distribution Guidelines table on page 54.

Spartan-II Clock Distribution Guidelines

Description		Symbol	Speed Grade -6	Speed Grade -5	Units
GCLK Distribution					
From GCLK pad to any flip-flop Note: These clock-distribution delays are provided for guidance only. They reflect the delays encountered in a typical design under worst-case conditions. Precise values for a particular design are provided by the timing analyzer.	XC2S15 XC2S30 XC2S50 XC2S100 XC2S150				ns, max ns, max ns, max ns, max ns, max ns, max ns, max ns, max ns, max

Spartan-II Clock Distribution Switching Characteristics

Description	Symbol	Speed Grade -6	Speed Grade -5	Units
GCLK IOB and Buffer				
Global Clock PAD to output. IN input to OUT output	T_{GPID} T_{GIO}		1.3 1.2	ns, max ns, max

Spartan-II CLB Switching Characteristics

Delays originating at F/G inputs vary slightly according to the input used. The values listed below are worst-case. Precise values are provided by the timing analyzer.

Description	Symbol	Speed Grade -6	Speed Grade -5	Units
Combinatorial Delays				
4-input function: F/G inputs to X/Y outputs 5-input function: F/G inputs to F5 output 5-input function: F/G inputs to X output 6-input function: F/G inputs to Y output via F6 MUX 6-input function: F5IN input to Y output Incremental delay routing through transparent latch to XQ/YQ outputs BY input to YB output	T_{ILO} T_{IF5} T_{IF5X} T_{IF6Y} T_{F5INY} T_{IFNCTL} T_{BYYB}		0.8 1.2 1.3 1.6 0.6 0.6 0.7	ns, max ns, max ns, max ns, max ns, max ns, max ns, max
Sequential Delays				
FF Clock CLK to XQ/YQ outputs Latch Clock CLK to XQ/YQ outputs	T_{CKO} T_{CKLO}		1.4 0.9	ns, max ns, max
Setup Times before Clock CLK				
4-input function: F/G Inputs 5-input function: F/G inputs 6-input function: F5IN input 6-input function: F/G inputs via F6 MUX BX/BY inputs CE input SR/BY inputs (synchronous)	T_{ICK} T_{IF5CK} T_{F5INCK} T_{IF6CK} T_{DICK} T_{CECK} T_{RCK}		1.2 1.8 1.0 2.0 2.0 1.0 1.7	ns, min ns, min ns, min ns, min ns, min ns, min ns, min
Hold Times after Clock CLK				
All Hold Times			0.0	ns, min
Clock CLK				
Minimum Pulse Width, High Minimum Pulse Width, Low	T_{CH} T_{CL}		2.0 2.0	ns, min ns, min
Set/Reset				
Minimum Pulse Width, SR/BY inputs Delay from SR/BY inputs to XQ/YQ outputs (asynchronous) Delay from GSR to XQ/YQ outputs	T_{RPW} T_{RQ} T_{GSRQ}		3.9 2.2 13.0	ns, min ns, max ns, max

Spartan-II CLB Arithmetic Switching Characteristics

Setup times not listed explicitly can be approximated by decreasing the combinatorial delays by the setup time adjustment listed. Precise values are provided by the timing analyzer.

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Combinatorial Delays				
F operand inputs to X via XOR	T_{OPX}		1.0	ns, max
F operand input to XB output	T_{OPXB}		1.6	ns, max
F operand input to Y via XOR	T_{OPY}		2.2	ns, max
F operand input to YB output	T_{OPYB}		1.7	ns, max
F operand input to COUT output	T_{OPCYF}		1.7	ns, max
G operand inputs to Y via XOR	T_{OPGY}		1.3	ns, max
G operand input to YB output	T_{OPGYB}		1.9	ns, max
G operand input to COUT output	T_{OPCYG}		1.8	ns, max
BX initialization input to COUT	T_{BXCY}		1.0	ns, max
CIN input to X output via XOR	T_{CINX}		0.6	ns, max
CIN input to XB	T_{CINXB}		0.1	ns, max
CIN input to Y via XOR	T_{CINY}		0.7	ns, max
CIN input to YB	T_{CINYB}		0.2	ns, max
CIN input to COUT output				
Multiplier Operation	T_{BYP}		0.2	ns, max
F1/2 operand inputs to XB output via AND	T_{FANDXB}		0.6	ns, max
F1/2 operand inputs to YB output via AND	T_{FANDYB}		0.6	ns, max
F1/2 operand inputs to COUT output via AND	T_{FANDCY}		0.6	ns, max
G1/2 operand inputs to YB output via AND	T_{GANDYB}		0.5	ns, max
G1/2 operand inputs to COUT output via AND	T_{GANDCY}		0.5	ns, max
Setup Times before Clock CLK				
CIN input to FFX	T_{CCKX}		1.1	ns, min
CIN input to FFY	T_{CCKY}		1.1	ns, min
Setup Time Adjustment				ns
Hold Times after Clock CLK				
All Hold Times			0.0	ns, min

Spartan-II CLB SelectRAM Switching Characteristics

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Sequential Delays				
Clock CLK to X/Y outputs (WE active)	T_{SHCKO}		3.0	ns, max
Shift-Register Mode				
Clock CLK to X/Y outputs			3.0	ns, max
Setup Times before Clock CLK				
F/G address inputs	T_{AS}/T_{AH}		0.8	ns, min
BX/BY data inputs (DIN)	T_{DS}/T_{DH}		1.3	ns, min
CE input (WE)	T_{WS}/T_{WH}		0.7	ns, min
Shift-Register Mode				
BX/BY data inputs (DIN)	T_{SHDICK}		0.9	ns, min
CE input (WS)	T_{SHCECK}		1.0	ns, min
Hold Times after Clock CLK				
All Hold Times			0.0	ns, min
Clock CLK				
Minimum Pulse Width, High	T_{WPH}		3.1	ns, min
Minimum Pulse Width, Low	T_{WPL}		3.1	ns, min
Minimum clock period to meet address write cycle time	T_{WC}		7.7	ns, min
Shift-Register Mode				
Minimum Pulse Width, High	T_{SRPH}		3.1	ns, min
Minimum Pulse Width, Low	T_{SRPL}		3.1	ns, min

Spartan-II BLOCKRAM Switching Characteristics

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Sequential Delays				
Clock CLK to DOUT output	T_{BCKO}		4.4	ns, max
Setup Times before Clock CLK				
ADDR inputs	T_{BACK}		1.6	ns, min
DIN inputs	T_{BDCK}		1.6	ns, min
EN input	T_{BECK}		3.6	ns, min
RST input	T_{BRCK}		3.3	ns, min
WEN input	T_{BWCK}		3.2	ns, min
Hold Times after Clock CLK				
All Hold Times			0.0	ns, min
Clock CLK				
Minimum Pulse Width, High	T_{BPWH}		2.0	ns, min
Minimum Pulse Width, Low	T_{BPWL}		2.0	ns, min
CLKA -> CLKB setup time for different ports	T_{BCCS}		4.0	ns, min

Spartan-II TBUF Switching Characteristics

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
Combinatorial Delays				
IN input to OUT output	T_{IO}		0.2	ns, max
TRI input to OUT output high-impedance	T_{OFF}		0.2	ns, max
Tri input to valid data on OUT output	T_{ON}		0.2	ns, max

Spartan-II Test Access Port Switching Characteristics

		Speed Grade		
Description	**Symbol**	**-6**	**-5**	**Units**
TMS and TDI Setup times before TCK	T_{TAPTCK}		4.0	ns, min
TMS and TDI Hold times after TCK	T_{TCKTAP}		2.0	ns, min
Output delay from clock TCK to output TDO	T_{TCKTDO}		11.0	ns, max
Maximum TCK clock frequency	F_{TCK}		33	MHz, max

For a complete Spartan and Spartan-XL data sheet including package pinouts, go to the CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

Pin Definitions

Table 35: Special Purpose Pins

Pin Name	Dedicated Pin	Direction	Description
GCK0, GCK1, GCK2, GCK3	Yes	Input	Clock input pins that connect to Global Clock Buffers. These pins become user inputs when not needed for clocks.
M0, M1, M2	Yes	Input	Mode pins are used to specify the configuration mode.
CCLK	Yes	Input or Output	The configuration Clock I/O pin: it is an input for SelectRAM and slave-serial modes, and output in master-serial mode
$\overline{\text{PROGRAM}}$	Yes	Input	Initiates a configuration sequence when asserted Low.
DONE	Yes	Bidirectional	Indicates that configuration loading is complete, and that the start-up sequence is in progress. The output may be open drain.
$\overline{\text{INIT}}$	No	Bidirectional (Open-drain)	When Low, indicates that the configuration memory is being cleared. The pin becomes a user I/O after configuration.
BUSY/ DOUT	No	Output	In Slave Parallel mode, BUSY controls the rate at which configuration data is loaded. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained. In serial modes, DOUT provides configuration data to downstream devices in a daisy-chain. The pin becomes a user I/O after configuration.
D0/DIN, D1, D2, D3, D4, D5, D6, D7	No	Input	In Slave Parallel mode, D0-7 are configuration data input pins. These pins become user I/Os after configuration unless the Slave Parallel port is retained. In serial modes, DIN is the single data input. This pin becomes a user I/O after configuration.
$\overline{\text{WRITE}}$	No	Input	In Slave Parallel mode, the active-low Write Enable signal. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
$\overline{\text{CS}}$	No	Input	In Slave Parallel mode, the active-low Chip Select signal. The pin becomes a user I/O after configuration unless the Slave Parallel port is retained.
TDI, TDO, TMS, TCK	Yes	Mixed	Boundary-scan Test-Access-Port pins (IEEE 1149.1).
V_{CCINT}	Yes	Input	Power-supply pins for the internal core logic.
V_{CCO}	Yes	Input	Power-supply pins for output drivers (subject to banking rules)
V_{REF}	No	Input	Input threshold voltage pins. Become user I/Os when an external threshold voltage is not needed (subject to banking rules).
GND	Yes	Input	Ground
$\overline{\text{PWDN}}$	Yes	Input	The pin is held High during normal operation and pulled Low for power down mode.
STATUS	Yes	Output	The pin goes Low when the part is in power down mode and is released High when part is ready to resume normal operation.

Spartan-II Product Availability

Table 36 shows the package and speed grades available for Spartan-II family devices. Table 37 shows the maximum user I/Os available on the device and the number of user I/Os available for each device/package combination.

Table 36: Spartan-II Package and Speed Grade Availability

Device	Pins	100	144	144	208	256	456
	Type	Plast. VQFP	Plast. TQFP	Chip Scale BGA	Plast. PQFP	Fine Pitch BGA	Fine Pitch BGA
	Code	VQ100	TQ144	CS144	PQ208	FG256	FG456
XC2S15	-5	C	C	(C)	-	-	-
	-6	(C)	(C)	(C)	-	-	-
XC2S30	-5	C	C	(C)	C	-	-
	-6	(C)	(C)	(C)	(C)	-	-
XC2S50	-5	-	C	-	C	C	-
	-6	-	(C)	-	(C)	(C)	-
XC2S100	-5	-	C	-	C	C	C
	-6	-	(C)	-	(C)	(C)	(C)
XC2S150	-5	-	-	-	C	C	C
	-6	-	-	-	(C)	(C)	(C)

9/28/99 RAM

C = Commercial T_J = 0° to +85°C

I = Industrial T_J = –40°C to +100°C

( ) Parentheses indicate future product plans

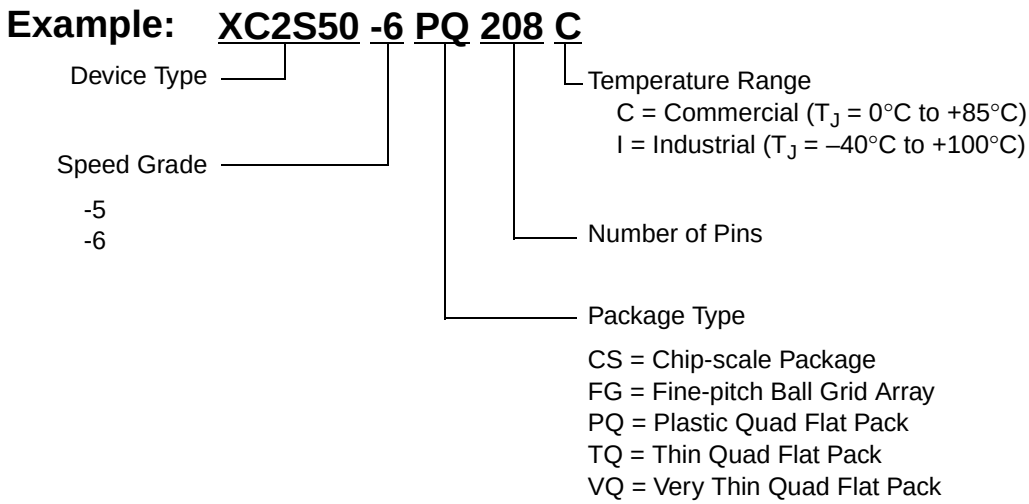
Table 37: Spartan-II Maximum User I/O Availability

Device	Max I/O		Package Type					
	SW*	Pkg.*	VQ100	TQ144	CS144	PQ208	FG256	FG456
XC2S15	96	86	60	86	86	-	-	-
XC2S30	144	132	60	92	92	132	-	-
XC2S50	192	176	-	92	-	140	176	-
XC2S100	240	196	-	92	-	140	176	196
XC2S150	288	260	-	-	-	140	176	260

11/18/99 RAM

*"SW" indicates the max number of IOs on Die including buried IOs, "PKG" indicates the max number of IOs available to the user in the largest packages.

Ordering Code Format



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Version No.	Date	Who	Description
0.1	6/29/99	RAM	Initial Review Version
0.2	7/2/99	RAM	Corrected I/O Count Errors, Misc. Errors
0.3	8/15/99	RAM	Corrected CLB count & BGA legend
0.4	9/28/99	RAM	Major Update - Speed, packages, architecture, etc.
0.5	10/15/99	RAM	Added Proposed TQ144 pinouts & minor corrections
0.6	11/8/99	RAM	Corrections to TQ144 and other tables
0.7	11/30/99	RAM	Update Arch Section, misc fixes
0.8	1/17/00	KEG	No. of RAM blocks/device, V_{CCO} bank assignments on XC2S50 and XC2S100, misc.
0.9	3/3/00	KEG	Added bank assoications to pinout tables, changed XC2S15 VQ100 pin 33 from I/O to V_{CCINT}. Added Delay-Locked Loop, BlockRAM, and Versatile I/O Design Considerations section.

Spartan and Spartan-XL Families Field Programmable Gate Arrays

DS060 (v1.5) February 16, 2000 - Product Specification

Introduction

The Spartan™ series is the first high-volume production FPGA solution to deliver all the key requirements for ASIC replacement up to 40,000 gates. These requirements include high performance, on-chip RAM, core solutions and prices that, in high volume, approach and in many cases are equivalent to mask programmed ASIC devices.

The Spartan series is the result of more than 14 years of FPGA design experience and feedback from thousands of customers. By streamlining the Spartan series feature set, leveraging advanced hybrid process technologies and focusing on total cost management, the Spartan series delivers the key features required by ASIC and other high-volume logic users while avoiding the initial cost, long development cycles and inherent risk of conventional ASICs. The Spartan and Spartan-XL families in the Spartan series have ten members, as shown in Table 38.

Spartan and Spartan-XL Features

Note: The Spartan series devices described in this data sheet include the 5V Spartan family and the 3.3V Spartan-XL family. See the separate data sheet for the 2.5V Spartan-II family.

- First ASIC replacement FPGA for high-volume production with on-chip RAM
- Advanced process technology
- Density up to 1862 logic cells or 40,000 system gates
- Streamlined feature set based on XC4000 architecture
- System performance beyond 80 MHz
- Broad set of AllianceCORE™ and LogiCORE™ predefined solutions available
- Unlimited reprogrammability
- Low cost
- System level features
  - Available in both 5V and 3.3V versions
  - On-chip SelectRAM™ memory
  - Fully PCI compliant
  - Low power segmented routing architecture
  - Full readback capability for program verification and internal node observability
  - Dedicated high-speed carry logic
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal networks
  - IEEE 1149.1-compatible Boundary Scan logic
- Versatile I/O and packaging
  - Low cost plastic packages available in all densities
  - Footprint compatibility in common packages
  - Individually programmable output slew-rate control maximizes performance and reduces noise
  - Zero input register hold time simplifies system timing
- Fully supported by powerful Xilinx development system
  - Foundation Series: Integrated, shrink-wrap software
  - Alliance Series: Dozens of PC and workstation third party development systems supported
  - Fully automatic mapping, placement and routing

Additional Spartan-XL Features

- 3.3V supply for low power with 5V tolerant I/Os
- Power down input
- Higher performance
- Faster carry logic
- More flexible high-speed clock network
- Latch capability in Configurable Logic Blocks
- Input fast capture latch
- Optional mux or 2-input function generator on outputs
- 12 mA or 24 mA output drive
- 5V and 3.3V PCI compatible
- Enhanced Boundary Scan
- Express Mode configuration
- Chip scale packaging

Table 38: Spartan and Spartan-XL Field Programmable Gate Arrays

Device	Logic Cells	Max System Gates	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-flops	Max. Available User I/O
XCS05 & XCS05XL	238	5,000	2,000 - 5,000	10 x 10	100	360	77
XCS10 & XCS10XL	466	10,000	3,000 - 10,000	14 x 14	196	616	112
XCS20 & XCS20XL	950	20,000	7,000 - 20,000	20 x 20	400	1,120	160
XCS30 & XCS30XL	1368	30,000	10,000 - 30,000	24 x 24	576	1,536	192
XCS40 & XCS40XL	1862	40,000	13,000 - 40,000	28 x 28	784	2,016	224

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

General Overview

Spartan series FPGAs are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a powerful hierarchy of versatile routing resources (routing channels), and surrounded by a perimeter of programmable Input/Output Blocks (IOBs), as seen in Figure 1. They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal static memory cells. Re-programming is possible an unlimited number of times. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA. The FPGA can either actively read its configuration data from an external serial PROM (Master Serial mode), or the configuration data can be written into the FPGA from an external device (Slave Serial mode).

Spartan series FPGAs can be used where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 50,000 systems per month.

Spartan series devices achieve high-performance, low-cost operation through the use of an advanced architecture and semiconductor technology. Spartan and Spartan-XL devices provide system clock rates exceeding 80 MHz and internal performance in excess of 150 MHz. In contrast to other FPGA devices, the Spartan series offers the most cost-effective solution while maintaining leading-edge performance. In addition to the conventional benefit of high volume programmable logic solutions, Spartan series FPGAs also offer on-chip edge-triggered single-port and dual-port RAM, clock enables on all flip-flops, fast carry logic, and many other features.

The Spartan/XL families leverage the highly successful XC4000 architecture with many of that family's features and benefits. Technology advancements have been derived from the XC4000XLA process developments.

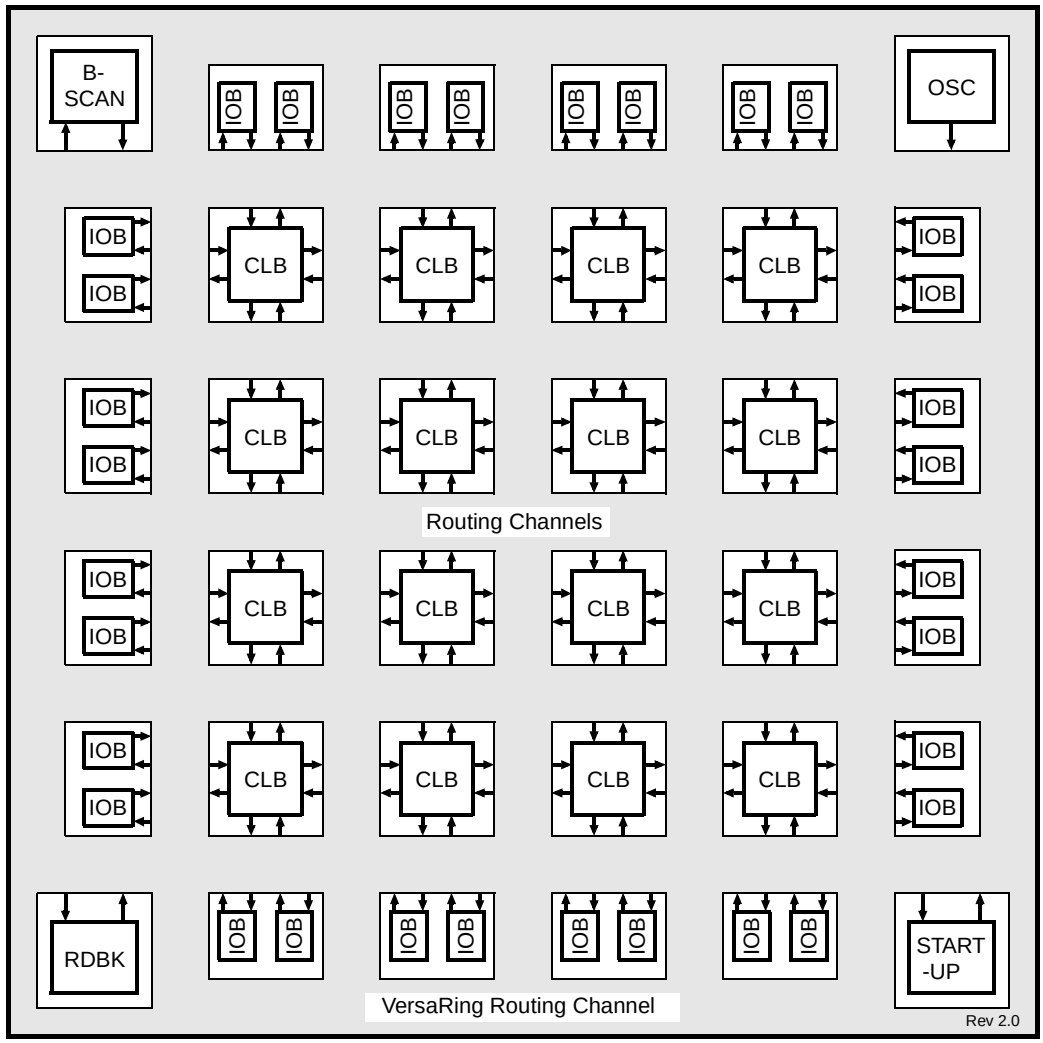


Figure 1: Basic FPGA Block Diagram

Logic Functional Description

The Spartan series uses a standard FPGA structure as shown in Figure 1 on page 62. The FPGA consists of an array of configurable logic blocks (CLBs) placed in a matrix of routing channels. The input and output of signals is achieved through a set of input/output blocks (IOBs) forming a ring around the CLBs and routing channels.

- CLBs provide the functional elements for implementing the user's logic.
- IOBs provide the interface between the package pins and internal signal lines.
- Routing channels provide paths to interconnect the inputs and outputs of the CLBs and IOBs.

The functionality of each circuit block is customized during configuration by programming internal static memory cells. The values stored in these memory cells determine the logic functions and interconnections implemented in the FPGA.

Configurable Logic Blocks (CLBs)

The CLBs are used to implement most of the logic in an FPGA. The principal CLB elements are shown in the simplified block diagram in Figure 2. There are three look-up tables (LUT) which are used as logic function generators, two flip-flops and two groups of signal steering multiplexers. There are also some more advanced features provided by the CLB which will be covered in the "Advanced Features Description" on page 72.

Function Generators

Two 16 x 1 memory look-up tables (F-LUT and G-LUT) are used to implement 4-input function generators, each offering unrestricted logic implementation of any Boolean function of up to four independent input signals (F1 to F4 or G1 to G4). Using memory look-up tables the propagation delay is independent of the function implemented.

A third 3-input function generator (H-LUT) can implement any Boolean function of its three inputs. Two of these inputs are controlled by programmable multiplexers (see box "A" of Figure 2). These inputs can come from the F-LUT or G-LUT outputs or from CLB inputs. The third input always comes from a CLB input. The CLB can, therefore, implement certain functions of up to nine inputs, like parity checking. The three LUTs in the CLB can also be combined to do any arbitrarily defined Boolean function of five inputs.

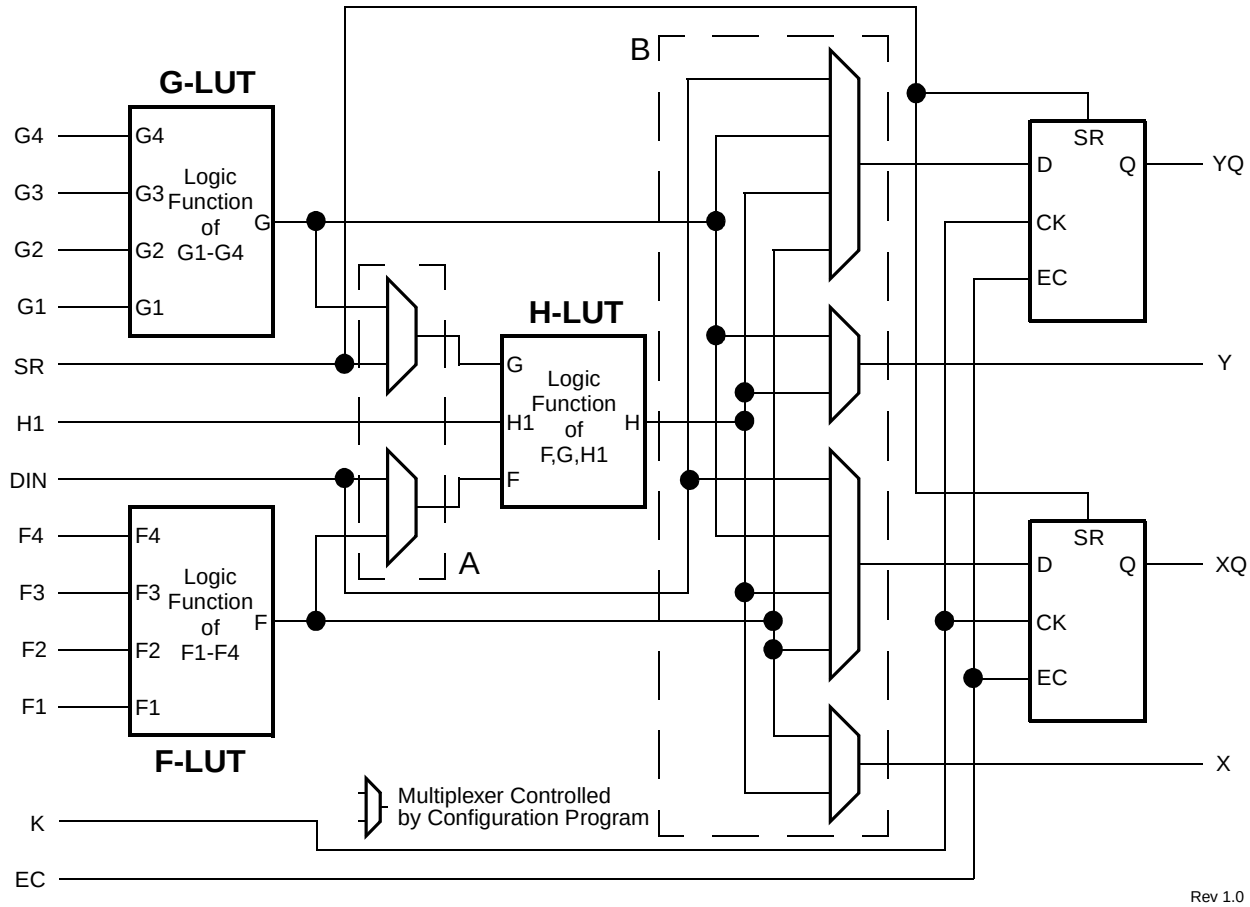


Figure 2: Spartan/XL Simplified CLB Logic Diagram (some features not shown)

A CLB can implement any of the following functions:

- Any function of up to four variables, plus any second function of up to four unrelated variables, plus any third function of up to three unrelated variables[1]
- Any single function of five variables
- Any function of four variables together with some functions of six variables
- Some functions of up to nine variables.

Implementing wide functions in a single block reduces both the number of blocks required and the delay in the signal path, achieving both increased capacity and speed.

The versatility of the CLB function generators significantly improves system speed. In addition, the design-software tools can deal with each function generator independently. This flexibility improves cell usage.

Flip-Flops

Each CLB contains two flip-flops that can be used to register (store) the function generator outputs. The flip-flops and function generators can also be used independently (see Figure 2 on page 63). The CLB input DIN can be used as a direct input to either of the two flip-flops. H1 can also drive either flip-flop via the H-LUT with a slight additional delay.

The two flip-flops have common clock (CK), clock enable (EC) and set/reset (SR) inputs. Internally both flip-flops are also controlled by a global initialization signal (GSR) which is described in detail in "Global Signals: GSR and GTS" on page 78.

Latches (Spartan-XL only)

The Spartan-XL CLB storage elements can also be configured as latches. The two latches have common clock (K) and clock enable (EC) inputs. Functionality of the storage element is described in Table 39.

Table 39: CLB Storage Element Functionality

Mode	CK	EC	SR	D	Q
Power-Up or GSR	X	X	X	X	SR
Flip-Flop Operation	X	X	1	X	SR
	⎍/‾	1*	0*	D	D
	0	X	0*	X	Q
Latch Operation (Spartan-XL)	1	1*	0*	X	Q
	0	1*	0*	D	D
Both	X	0	0*	X	Q

Legend:

X	Don't care
⎍/‾	Rising edge (clock not inverted)
$\overline{SR}$	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

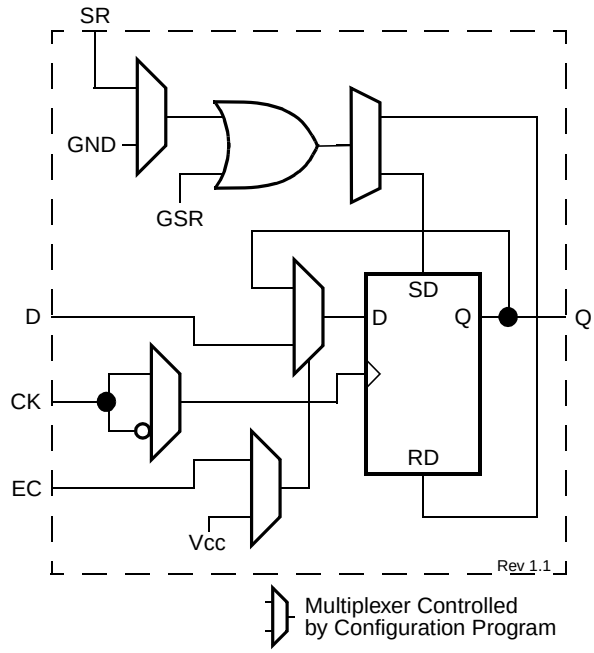


Figure 3: CLB Flip-Flop Functional Block Diagram

Clock Input

Each flip-flop can be triggered on either the rising or falling clock edge. The CLB clock line is shared by both flip-flops. However, the clock is individually invertible for each flip-flop (see CK path in Figure 3). Any inverter placed on the clock line in the design is automatically absorbed into the CLB.

Clock Enable

The clock enable line (EC) is active High. The EC line is shared by both flip-flops in a CLB. If either one is left disconnected, the clock enable for that flip-flop defaults to the active state. EC is not invertible within the CLB. The clock enable is synchronous to the clock and must satisfy the setup and hold timing specified for the device.

Set/Reset

The set/reset line (SR) is an asynchronous active High control of the flip-flop. SR can be configured as either set or reset at each flip-flop. This configuration option determines the state in which each flip-flop becomes operational after configuration. It also determines the effect of a GSR pulse during normal operation, and the effect of a pulse on the SR line of the CLB. The SR line is shared by both flip-flops. If SR is not specified for a flip-flop the set/reset for that flip-flop defaults to the inactive state. SR is not invertible within the CLB.

1. When three separate functions are generated, one of the function outputs must be captured in a flip-flop internal to the CLB. Only two unregistered function generator outputs are available from the CLB.

CLB Signal Flow Control

In addition to the H-LUT input control multiplexers (shown in box "A" of Figure 2 on page 63) there are signal flow control multiplexers (shown in box "B" of Figure 2) which select the signals which drive the flip-flop inputs and the combinatorial CLB outputs (X and Y).

Each flip-flop input is driven from a 4:1 multiplexer which selects among the three LUT outputs and DIN as the data source.

Each combinatorial output is driven from a 2:1 multiplexer which selects between two of the LUT outputs. The X output can be driven from the F-LUT or H-LUT, the Y output from G-LUT or H-LUT.

Control Signals

There are four signal control multiplexers on the input of the CLB. These multiplexers allow the internal CLB control signals (H1, DIN, SR, and EC in Figure 2 and Figure 4) to be driven from any of the four general control inputs (C1 - C4 in Figure 4) into the CLB. Any of these inputs can drive any of the four internal control signals.

The four internal control signals are:

- EC - Enable Clock
- SR - Asynchronous Set/Reset or H function generator Input 0
- DIN - Direct In or H function generator Input 2
- H1 - H function generator Input 1.

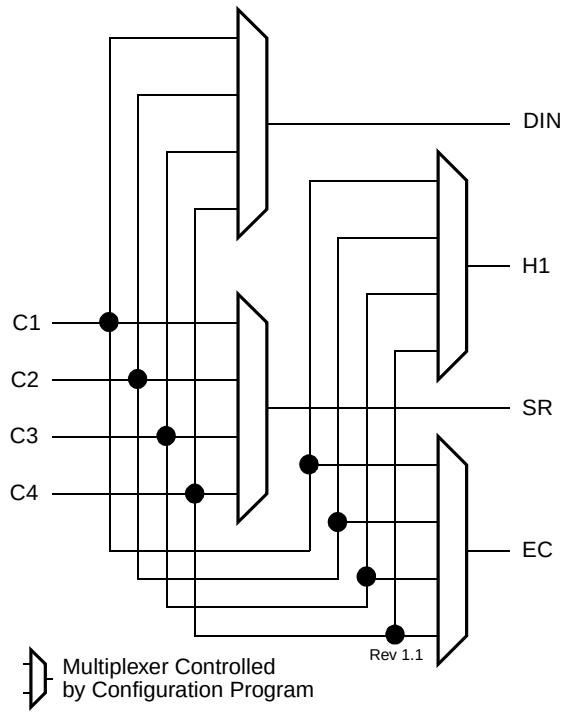


Figure 4: CLB Control Signal Interface

Input/Output Blocks (IOBs)

User-configurable input/output blocks (IOBs) provide the interface between external package pins and the internal logic. Each IOB controls one package pin and can be configured for input, output, or bidirectional signals. Figure 5 on page 66 shows a simplified functional block diagram of the Spartan/XL IOB.

IOB Input Signal Path

The input signal to the IOB can be configured to either go directly to the routing channels (via I1 and I2 in Figure 5) or to the input register. The input register can be programmed as either an edge-triggered flip-flop or a level-sensitive latch. The functionality of this register is shown in Table 40, and a simplified block diagram of the register can be seen in Figure 6.

Table 40: Input Register Functionality

Mode	CK	EC	D	Q
Power-Up or GSR	X	X	X	SR
Flip-Flop	__/‾	1*	D	D
	0	X	X	Q
Latch	1	1*	X	Q
	0	1*	D	D
Both	X	0	X	Q

Legend:

X	Don't care
__/	Rising edge (clock not inverted)
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)

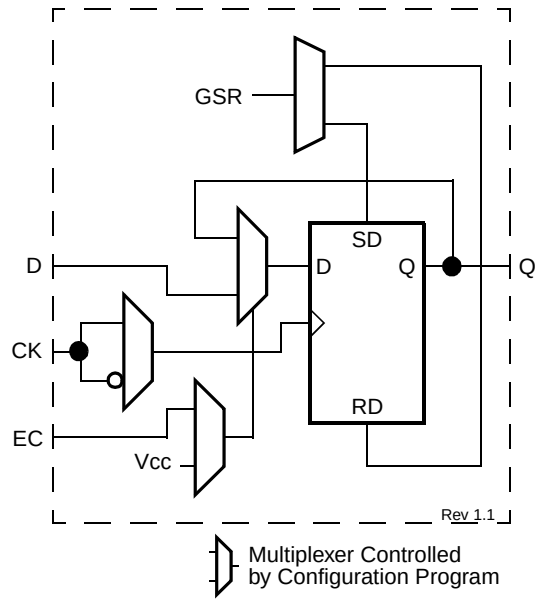


Figure 6: IOB Flip-Flop/Latch Functional Block Diagram

The register choice is made by placing the appropriate library symbol. For example, IFD is the basic input flip-flop (rising edge triggered), and ILD is the basic input latch (transparent-High). Variations with inverted clocks are also available. The clock signal inverter is also shown in Figure 6 on the CK line.

The Spartan IOB data input path has a one-tap delay element: either the delay is inserted (default), or it is not. The Spartan-XL IOB data input path has a two-tap delay element, with choices of a full delay, a partial delay, or no delay. The added delay guarantees a zero hold time with respect to clocks routed through the global clock buffers. (See "Global Nets and Buffers" on page 71 for a description of the global clock buffers in the Spartan/XL families.) For a shorter input register setup time, with positive hold-time, attach a NODELAY attribute or property to the flip-flop.

The output of the input register goes to the routing channels (via I1 and I2 in Figure 5). The I1 and I2 signals that exit the IOB can each carry either the direct or registered input signal.

The 5V Spartan input buffers can be globally configured for either TTL (1.2V) or CMOS (VCC/2) thresholds, using an option in the bitstream generation software. The Spartan output levels are also configurable; the two global adjustments of input threshold and output level are independent. The inputs of Spartan devices can be driven by the outputs of any 3.3V device, if the Spartan inputs are in TTL mode. Spartan-XL inputs are TTL compatible and 3.3V CMOS compatible.

Supported sources for Spartan/XL device inputs are shown in Table 41.

Spartan-XL I/Os are fully 5V tolerant even though the V_{CC} is 3.3V. This allows 5V signals to directly connect to the Spartan-XL inputs without damage, as shown in Table 41. In addition, the 3.3V V_{CC} can be applied before or after 5V signals are applied to the I/Os. This makes the Spartan-XL devices immune to power supply sequencing problems.

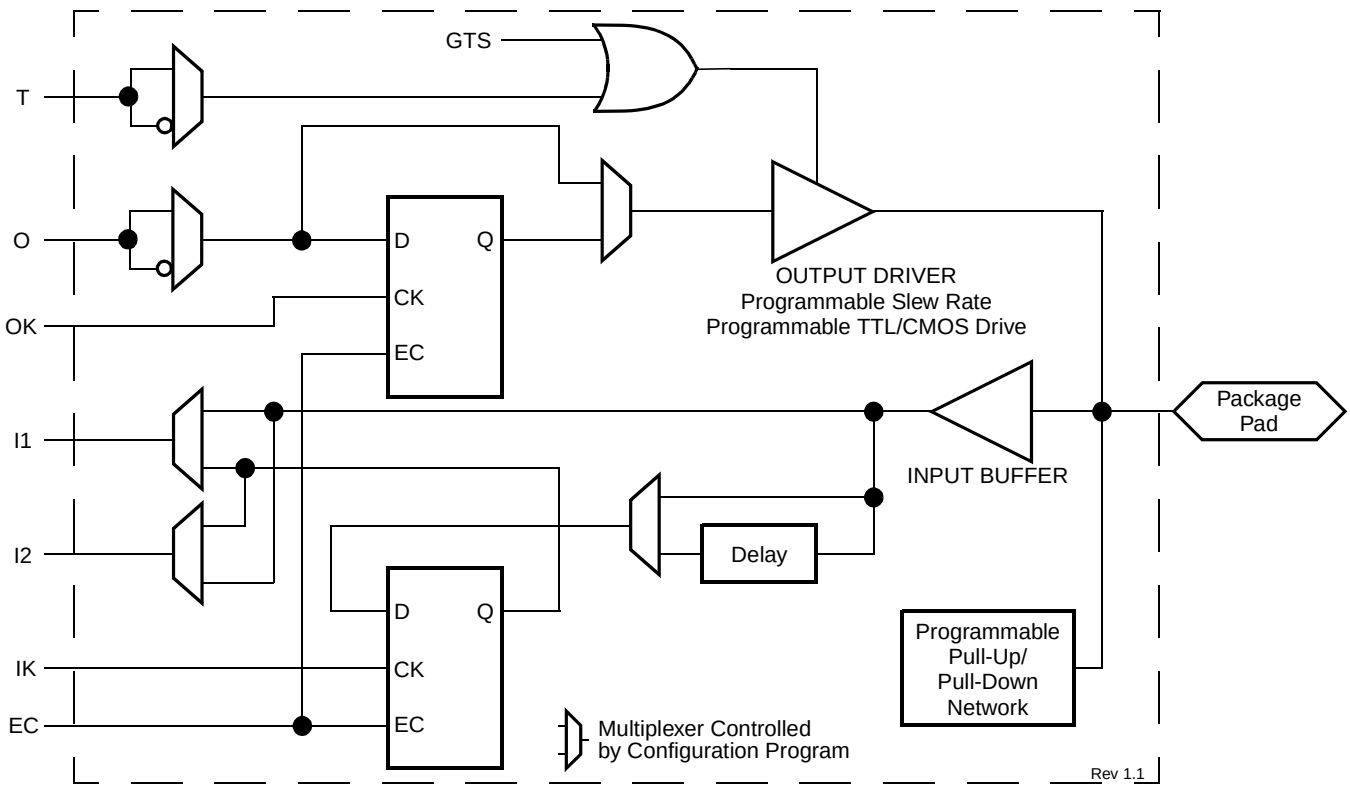


Figure 5: Simplified Spartan/XL IOB Block Diagram

Table 41: Supported Sources for Spartan/XL Inputs

Source	Spartan Inputs		Spartan-XL Inputs
	5V, TTL	5V, CMOS	3.3V CMOS
Any device, V_{CC} = 3.3V, CMOS outputs	√	Unreliable Data	√
Spartan family, V_{CC} = 5V, TTL outputs	√		√
Any device, V_{CC} = 5V, TTL outputs ($V_{OH} \leq 3.7V$)	√		√
Any device, V_{CC} = 5V, CMOS outputs	√	√	√ (default mode)

Spartan-XL V_{CC} Clamping

Spartan-XL FPGAs have an optional clamping diode connected from each I/O to V_{CC}. When enabled they clamp ringing transients back to the 3.3V supply rail. This clamping action is required in 3.3V PCI applications. V_{CC} clamping is a global option affecting all I/O pins.

Spartan-XL devices are fully 5V TTL I/O compatible if V_{CC} clamping is not enabled. With V_{CC} clamping enabled, the Spartan-XL devices will begin to clamp input voltages to one diode voltage drop above V_{CC}. If enabled, TTL I/O compatibility is maintained but full 5V I/O tolerance is sacrificed. The user may select either 5V tolerance (default) or 3.3V PCI compatibility. In both cases negative voltage is clamped to one diode voltage drop below ground.

Spartan-XL devices are compatible with TTL, LVTTL, PCI 3V, PCI 5V and LVCMOS signalling. The various standards are illustrated in Table 42.

4

Table 42: I/O Standards Supported by Spartan-XL FPGAs

Signaling Standard	VCC Clamping	Output Drive	$V_{IH\ MAX}$	$V_{IH\ MIN}$	$V_{IL\ MAX}$	$V_{OH\ MIN}$	$V_{OL\ MAX}$
TTL	Not allowed	12/24 mA	5.5	2.0	0.8	2.4	0.4
LVTTL	OK	12/24 mA	3.6	2.0	0.8	2.4	0.4
PCI5V	Not allowed	24 mA	5.5	2.0	0.8	2.4	0.4
PCI3V	Required	12 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}
LVCMOS 3V	OK	12/24 mA	3.6	50% of V_{CC}	30% of V_{CC}	90% of V_{CC}	10% of V_{CC}

Additional Fast Capture Input Latch (Spartan-XL only)

The Spartan-XL IOB has an additional optional latch on the input. This latch is clocked by the clock used for the output flip-flop rather than the input clock. Therefore, two different clocks can be used to clock the two input storage elements. This additional latch allows the fast capture of input data, which is then synchronized to the internal clock by the IOB flip-flop or latch.

To place the Fast Capture latch in a design, use one of the special library symbols, ILFFX or ILFLX. ILFFX is a transparent-Low Fast Capture latch followed by an active High input flip-flop. ILFLX is a transparent-Low Fast Capture latch followed by a transparent-High input latch. Any of the clock inputs can be inverted before driving the library element, and the inverter is absorbed into the IOB.

IOB Output Signal Path

Output signals can be optionally inverted within the IOB, and can pass directly to the output buffer or be stored in an edge-triggered flip-flop and then to the output buffer. The functionality of this flip-flop is shown in Table 43.

Table 43: Output Flip-Flop Functionality

Mode	Clock	Clock Enable	T	D	Q
Power-Up or GSR	X	X	0*	X	SR
Flip-Flop	X	0	0*	X	Q
	⎍/‾	1*	0*	D	D
	X	X	1	X	Z
	0	X	0*	X	Q

Legend:

X	Don't care
⎍/‾	Rising edge (clock not inverted)
SR	Set or Reset value. Reset is default.
0*	Input is Low or unconnected (default value)
1*	Input is High or unconnected (default value)
Z	3-state

Output Multiplexer/2-Input Function Generator (Spartan-XL only)

The output path in the Spartan-XL IOB contains an additional multiplexer not available in the Spartan IOB. The multiplexer can also be configured as a 2-input function generator, implementing a pass gate, AND gate, OR gate, or XOR gate, with 0, 1, or 2 inverted inputs.

When configured as a multiplexer, this feature allows two output signals to time-share the same output pad, effectively doubling the number of device outputs without requiring a larger, more expensive package. The select input is the pin used for the output flip-flop clock, OK.

When the multiplexer is configured as a 2-input function generator, logic can be implemented within the IOB itself. Combined with a Global buffer, this arrangement allows very high-speed gating of a single signal. For example, a wide decoder can be implemented in CLBs, and its output gated with a Read or Write Strobe driven by a global buffer.

The user can specify that the IOB function generator be used by placing special library symbols beginning with the letter "O." For example, a 2-input AND gate in the IOB function generator is called OAND2. Use the symbol input pin labeled "F" for the signal on the critical path. This signal is placed on the OK pin — the IOB input with the shortest delay to the function generator. Two examples are shown in Figure 7.

Figure 7: AND & MUX Symbols in Spartan-XL IOB

Output Buffer

An active High 3-state signal can be used to place the output buffer in a high-impedance state, implementing 3-state outputs or bidirectional I/O. Under configuration control, the output (O) and output 3-state (T) signals can be inverted. The polarity of these signals is independently configured for each IOB (see Figure 5 on page 66). An output can be configured as open-drain (open-collector) by tying the 3-state pin (T) to the output signal, and the input pin (I) to Ground.

By default, a 5V Spartan device output buffer pull-up structure is configured as a TTL-like totem-pole. The High driver is an n-channel pull-up transistor, pulling to a voltage one transistor threshold below V_{CC}. Alternatively, the outputs can be globally configured as CMOS drivers, with additional p-channel pull-up transistors pulling to V_{CC}. This option, applied using the bitstream generation software, applies to all outputs on the device. It is not individually programmable.

All Spartan-XL device outputs are configured as CMOS drivers, therefore driving rail-to-rail. The Spartan-XL outputs are individually programmable for 12 mA or 24 mA output drive.

Any 5V Spartan device with its outputs configured in TTL mode can drive the inputs of any typical 3.3V device. Supported destinations for Spartan/XL device outputs are shown in Table 44.

Three-State Register (Spartan-XL Only)

Spartan-XL devices incorporate an optional register controlling the three-state enable in the IOBs. The use of the three-state control register can significantly improve output enable and disable time.

Output Slew Rate

The slew rate of each output buffer is, by default, reduced, to minimize power bus transients when switching non-critical signals. For critical signals, attach a FAST attribute or property to the output buffer or flip-flop.

Spartan/XL devices have a feature called "Soft Start-up," designed to reduce ground bounce when all outputs are turned on simultaneously at the end of configuration. When the configuration process is finished and the device starts up, the first activation of the outputs is automatically slew-rate limited. Immediately following the initial activation of the I/O, the slew rate of the individual outputs is determined by the individual configuration option for each IOB.

Pull-up and Pull-down Network

Programmable pull-up and pull-down resistors are used for tying unused pins to V_{CC} or Ground to minimize power consumption and reduce noise sensitivity. The configurable pull-up resistor is a p-channel transistor that pulls to V_{CC}. The configurable pull-down resistor is an n-channel transistor that pulls to Ground. The value of these resistors is typically 20 kΩ – 100 kΩ (See “Spartan DC Characteristics Over Operating Conditions” on page 96.). This high value makes them unsuitable as wired-AND pull-up resistors.

Table 44: Supported Destinations for Spartan/XL Outputs

Destination	Spartan-XL Outputs	Spartan Outputs	
	3.3V, CMOS	5V, TTL	5V, CMOS
Any device, V_{CC} = 3.3V, CMOS-threshold inputs	√	√	Some[1]
Any device, V_{CC} = 5V, TTL-threshold inputs	√	√	√
Any device, V_{CC} = 5V, CMOS-threshold inputs	**Unreliable Data**		√

1. Only if destination device has 5V tolerant inputs

After configuration, voltage levels of unused pads, bonded or unbonded, must be valid logic levels, to reduce noise sensitivity and avoid excess current. Therefore, by default, unused pads are configured with the internal pull-up resistor active. Alternatively, they can be individually configured with the pull-down resistor, or as a driven output, or to be driven by an external source. To activate the internal pull-up, attach the PULLUP library component to the net attached to the pad. To activate the internal pull-down, attach the PULLDOWN library component to the net attached to the pad.

Set/Reset

As with the CLB registers, the GSR signal can be used to set or clear the input and output registers, depending on the value of the INIT attribute or property. The two flip-flops can be individually configured to set or clear on reset and after configuration. Other than the global GSR net, no user-controlled set/reset signal is available to the I/O flip-flops (Figure 6). The choice of set or reset applies to both the initial state of the flip-flop and the response to the GSR pulse.

Independent Clocks

Separate clock signals are provided for the input (IK) and output (OK) flip-flops. The clock can be independently inverted for each flip-flop within the IOB, generating either falling-edge or rising-edge triggered flip-flops. The clock inputs for each IOB are independent.

Common Clock Enables

The input and output flip-flops in each IOB have a common clock enable input (see EC signal in Figure 6), which through configuration, can be activated individually for the input or output flip-flop, or both. This clock enable operates exactly like the EC signal on the Spartan/XL CLB. It cannot be inverted within the IOB.

Routing Channel Description

All internal routing channels are composed of metal segments with programmable switching points and switching matrices to implement the desired routing. A structured, hierarchical matrix of routing channels is provided to achieve efficient automated routing.

This section describes the routing channels available in Spartan/XL devices. Figure 8 shows a general block diagram of the CLB routing channels. The implementation software automatically assigns the appropriate resources based on the density and timing requirements of the design. The following description of the routing channels is for information only and is simplified with some minor details omitted. For an exact interconnect description the designer should open a design in the FPGA Editor and review the actual connections in this tool.

The routing channels will be discussed as follows;

- CLB routing channels which run along each row and column of the CLB array.
- IOB routing channels which form a ring (called a VersaRing) around the outside of the CLB array. It connects the I/O with the CLB routing channels.
- Global routing consists of dedicated networks primarily designed to distribute clocks throughout the device with minimum delay and skew. Global routing can also be used for other high-fanout signals.

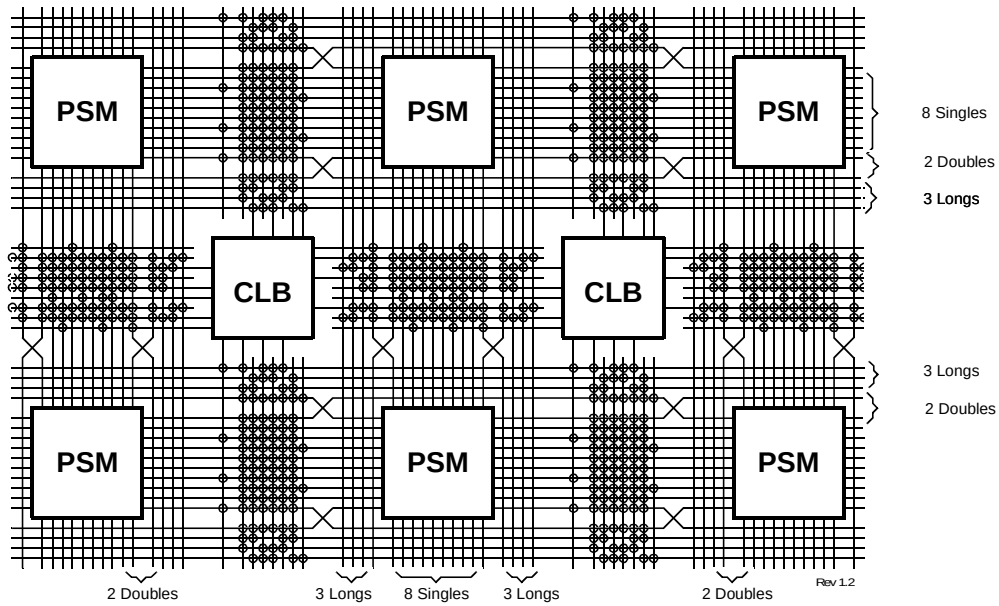


Figure 8: Spartan/XL CLB Routing Channels and Interface Block Diagram

CLB Routing Channels

The routing channels around the CLB are derived from three types of interconnects; single-length, double-length, and longlines. At the intersection of each vertical and horizontal routing channel is a signal steering matrix called a Programmable Switch Matrix (PSM). Figure 8 shows the basic routing channel configuration showing single-length lines, double-length lines and longlines as well as the CLBs and PSMs. The CLB to routing channel interface is shown as well as how the PSMs interface at the channel intersections.

CLB Interface

A block diagram of the CLB interface signals is shown in Figure 9. The input signals to the CLB are distributed evenly on all four sides providing maximum routing flexibility. In general, the entire architecture is symmetrical and regular. It is well suited to established placement and routing algorithms. Inputs, outputs, and function generators can freely swap positions within a CLB to avoid routing congestion during the placement and routing operation. The exceptions are the clock (K) input and CIN/COUT signals. The K input is routed to dedicated global vertical lines as well as four single-length lines and is on the left side of the CLB. The CIN/COUT signals are routed through dedicated interconnects which do not interfere with the general routing structure. The output signals from the CLB are available to drive both vertical and horizontal channels.

Programmable Switch Matrices

The horizontal and vertical single- and double-length lines intersect at a box called a programmable switch matrix (PSM). Each PSM consists of programmable pass transistors used to establish connections between the lines (see Figure 10).

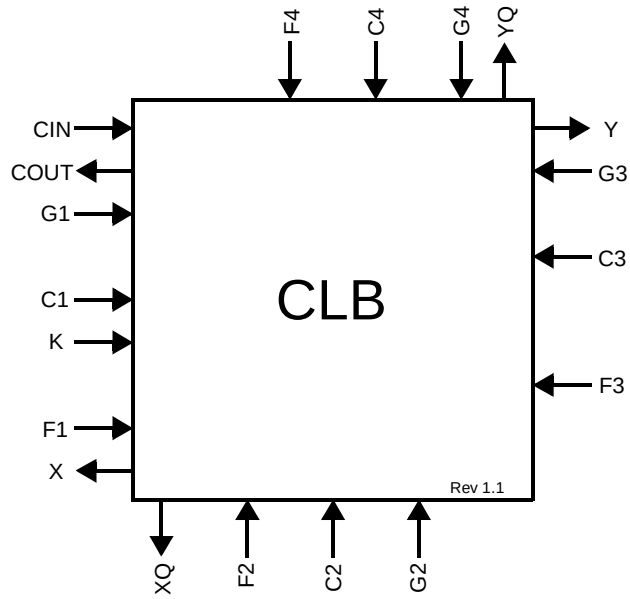


Figure 9: CLB Interconnect Signals

For example, a single-length signal entering on the right side of the switch matrix can be routed to a single-length line on the top, left, or bottom sides, or any combination thereof, if multiple branches are required. Similarly, a double-length signal can be routed to a double-length line on any or all of the other three edges of the programmable switch matrix.

Single-Length Lines

Single-length lines provide the greatest interconnect flexibility and offer fast routing between adjacent blocks. There are eight vertical and eight horizontal single-length lines associated with each CLB. These lines connect the switching matrices that are located in every row and column of CLBs.

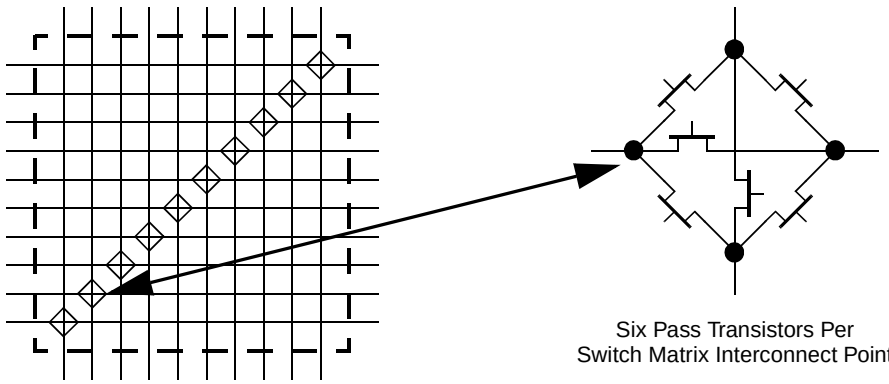


Figure 10: Programmable Switch Matrix

Single-length lines are connected by way of the programmable switch matrices, as shown in Figure 10. Routing connectivity is shown in Figure 8.

Single-length lines incur a delay whenever they go through a PSM. Therefore, they are not suitable for routing signals for long distances. They are normally used to conduct signals within a localized area and to provide the branching for nets with fanout greater than one.

Double-Length Lines

The double-length lines consist of a grid of metal segments, each twice as long as the single-length lines: they run past two CLBs before entering a PSM. Double-length lines are grouped in pairs with the PSMs staggered, so that each line goes through a PSM at every other row or column of CLBs (see Figure 8).

There are four vertical and four horizontal double-length lines associated with each CLB. These lines provide faster signal routing over intermediate distances, while retaining routing flexibility.

Longlines

Longlines form a grid of metal interconnect segments that run the entire length or width of the array. Longlines are intended for high fan-out, time-critical signal nets, or nets that are distributed over long distances.

Each Spartan/XL device longline has a programmable splitter switch at its center. This switch can separate the line into two independent routing channels, each running half the width or height of the array.

Routing connectivity of the longlines is shown in Figure 8. The longlines also interface to some 3-state buffers which is described later in “3-State Long Line Drivers” on page 77.

I/O Routing

Spartan/XL devices have additional routing around the IOB ring. This routing is called a VersaRing. The VersaRing facilitates pin-swapping and redesign without affecting board layout. Included are eight double-length lines, and four longlines.

Global Nets and Buffers

The Spartan/XL devices have dedicated global networks. These networks are designed to distribute clocks and other high fanout control signals throughout the devices with minimal skew.

Four vertical longlines in each CLB column are driven exclusively by special global buffers. These longlines are in addition to the vertical longlines used for standard interconnect. In the 5V Spartan devices, the four global lines can be driven by either of two types of global buffers; Primary Global buffers (BUFGP) or Secondary Global buffers (BUFGS). Each of these lines can be accessed by one particular Primary Global buffer, or by any of the Secondary Global buffers, as shown in Figure 11. In the 3V Spartan-XL devices, the four global lines can be driven by any of the eight Global Low-Skew Buffers (BUFGLS). The clock pins of every CLB and IOB can also be sourced from local interconnect.

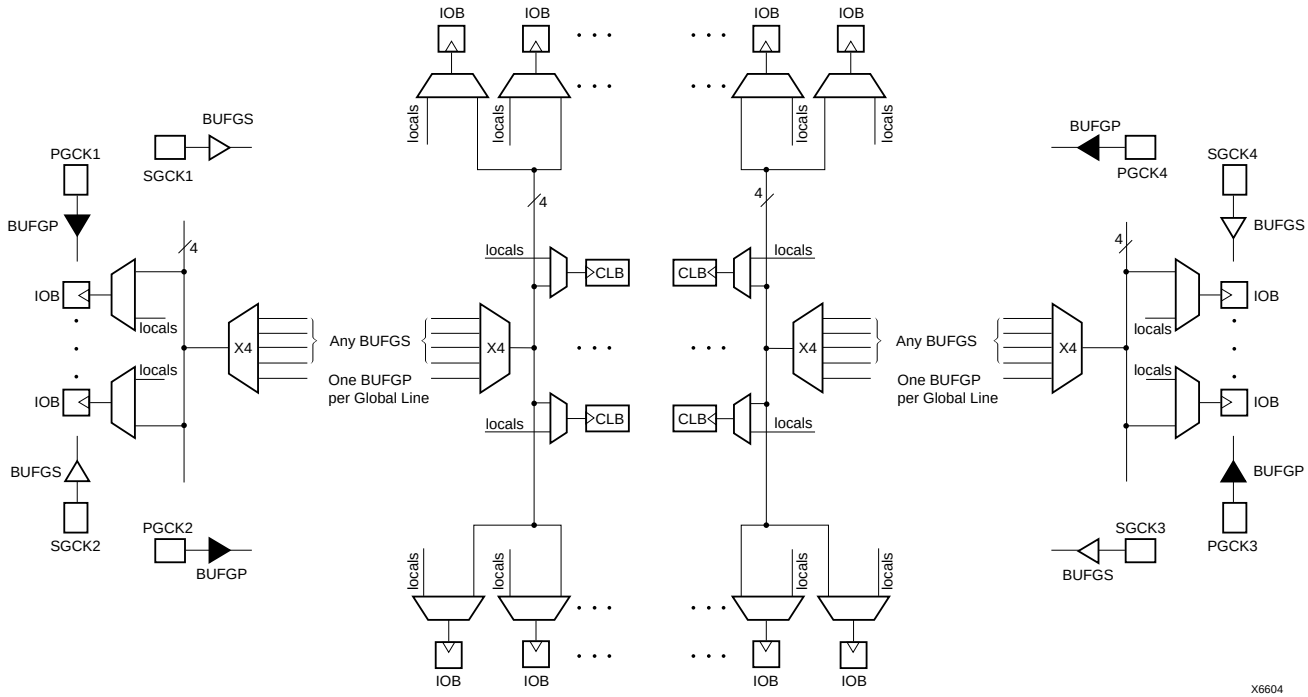


Figure 11: 5V Spartan Family Global Net Distribution

The four Primary Global buffers offer the shortest delay and negligible skew. Four Secondary Global buffers have slightly longer delay and slightly more skew due to potentially heavier loading, but offer greater flexibility when used to drive non-clock CLB inputs. The eight Global Low-Skew buffers in the Spartan-XL devices combine short delay, negligible skew, and flexibility.

The Primary Global buffers must be driven by the semi-dedicated pads (PGCK1-4). The Secondary Global buffers can be sourced by either semi-dedicated pads (SGCK1-4) or internal nets. Each corner of the device has one Primary buffer and one Secondary buffer. The Spartan-XL family has eight global low-skew buffers, two in each corner. All can be sourced by either semi-dedicated pads (GCK1-8) or internal nets.

Using the library symbol called BUFG results in the software choosing the appropriate clock buffer, based on the timing requirements of the design. A global buffer should be specified for all timing-sensitive global signal distribution. To use a global buffer, place a BUFGP (primary buffer), BUFGS (secondary buffer), BUFGLS (Spartan-XL global low-skew buffer), or BUFG (any buffer type) element in a schematic or in HDL code.

Advanced Features Description

Distributed RAM

Optional modes for each CLB allow the function generators (F-LUT and G-LUT) to be used as Random Access Memory (RAM).

Read and write operations are significantly faster for this on-chip RAM than for off-chip implementations. This speed advantage is due to the relatively short signal propagation delays within the FPGA.

Memory Configuration Overview

There are two available memory configuration modes: single-port RAM and dual-port RAM. For both these modes, write operations are synchronous (edge-triggered), while read operations are asynchronous. In the single-port mode, a single CLB can be configured as either a 16 x 1, (16 x 1) x 2, or 32 x 1 RAM array. In the dual-port mode, a single CLB can be configured only as one 16 x 1 RAM array. The different CLB memory configurations are summarized in Table 45. Any of these possibilities can be individually programmed into a Spartan/XL CLB.

- The 16 x 1 single-port configuration contains a RAM array with 16 locations, each one-bit wide. One 4-bit address decoder determines the RAM location for write and read operations. There is one input for writing data and one output for reading data, all at the selected address.
- The (16 x 1) x 2 single-port configuration combines two 16 x 1 single-port configurations (each according to the preceding description). There is one data input, one data output and one address decoder for each array. These arrays can be addressed independently.
- The 32 x 1 single-port configuration contains a RAM array with 32 locations, each one-bit wide. There is one data input, one data output, and one 5-bit address decoder.
- The dual-port mode 16 x 1 configuration contains a RAM array with 16 locations, each one-bit wide. There are two 4-bit address decoders, one for each port. One port consists of an input for writing and an output for reading, all at a selected address. The other port consists of one output for reading from an independently selected address.

Table 45: CLB Memory Configurations

Mode	16 x 1	(16 x 1) x 2	32 x 1
Single-Port	√	√	√
Dual-Port	√		

The appropriate choice of RAM configuration mode for a given design should be based on timing and resource requirements, desired functionality, and the simplicity of the design process. Selection criteria include the following: Whereas the 32 x 1 single-port, the (16 x 1) x 2 single-port, and the 16 x 1 dual-port configurations each use one entire CLB, the 16 x 1 single-port configuration uses only one half of a CLB. Due to its simultaneous read/write capability, the dual-port RAM can transfer twice as much data as the single-port RAM, which permits only one data operation at any given time.

CLB memory configuration options are selected by using the appropriate library symbol in the design entry.

Single-Port Mode

There are three CLB memory configurations for the single-port RAM: 16 x 1, (16 x 1) x 2, and 32 x 1, the functional organization of which is shown in Figure 12.

The single-port RAM signals and the CLB signals (Figure 2 on page 63) from which they are originally derived are shown in Table 46.

Table 46: Single-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN or H_1
A[3:0]	Address	F_1-F_4 or G_1-G_4
A_4 (32 x 1 only)	Address	H_1
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (Data Out)	F_{OUT} or G_{OUT}

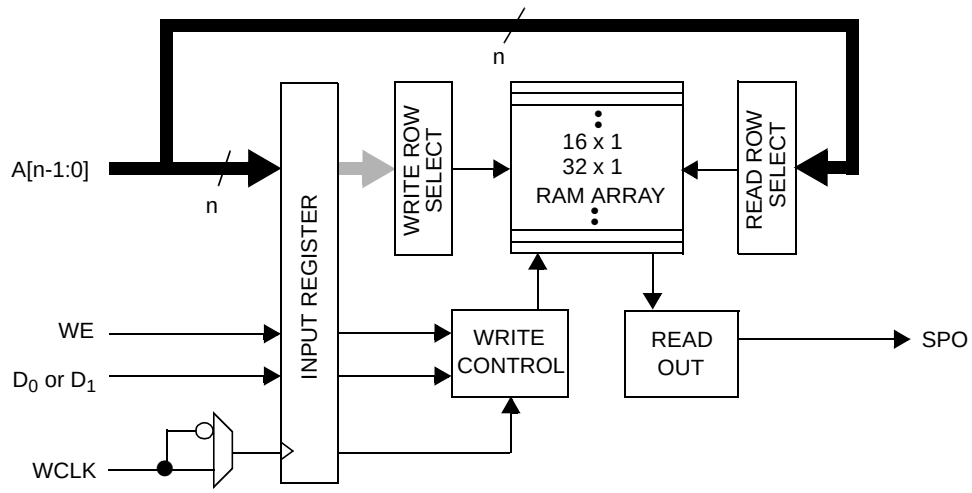


Figure 12: Logic Diagram for the Single-Port RAM

NOTE: 1. The (16 x 1) x 2 configuration combines two 16 x 1 single-port RAMs, each with its own independent address bus and data input. The same WE and WCLK signals are connected to both RAMs.
2. n = 4 for the 16 x 1 and (16 x 1) x 2 configurations. n = 5 for the 32 x 1 configuration.

Writing data to the single-port RAM is essentially the same as writing to a data register. It is an edge-triggered (synchronous) operation performed by applying an address to the A inputs and data to the D input during the active edge of WCLK while WE is High.

The timing relationships are shown in Figure 13. The High logic level on WE enables the input data register for writing. The active edge of WCLK latches the address, input data, and WE signals. Then, an internal write pulse is generated that loads the data into the memory cell.

WCLK can be configured as active on either the rising edge (default) or the falling edge. While the WCLK input to the RAM accepts the same signal as the clock input to the associated CLB's flip-flops, the sense of this WCLK input can be inverted with respect to the sense of the flip-flop clock inputs. Consequently, within the same CLB, data at the RAM's SPO line can be stored in a flip-flop with either the same or the inverse clock polarity used to write data to the RAM.

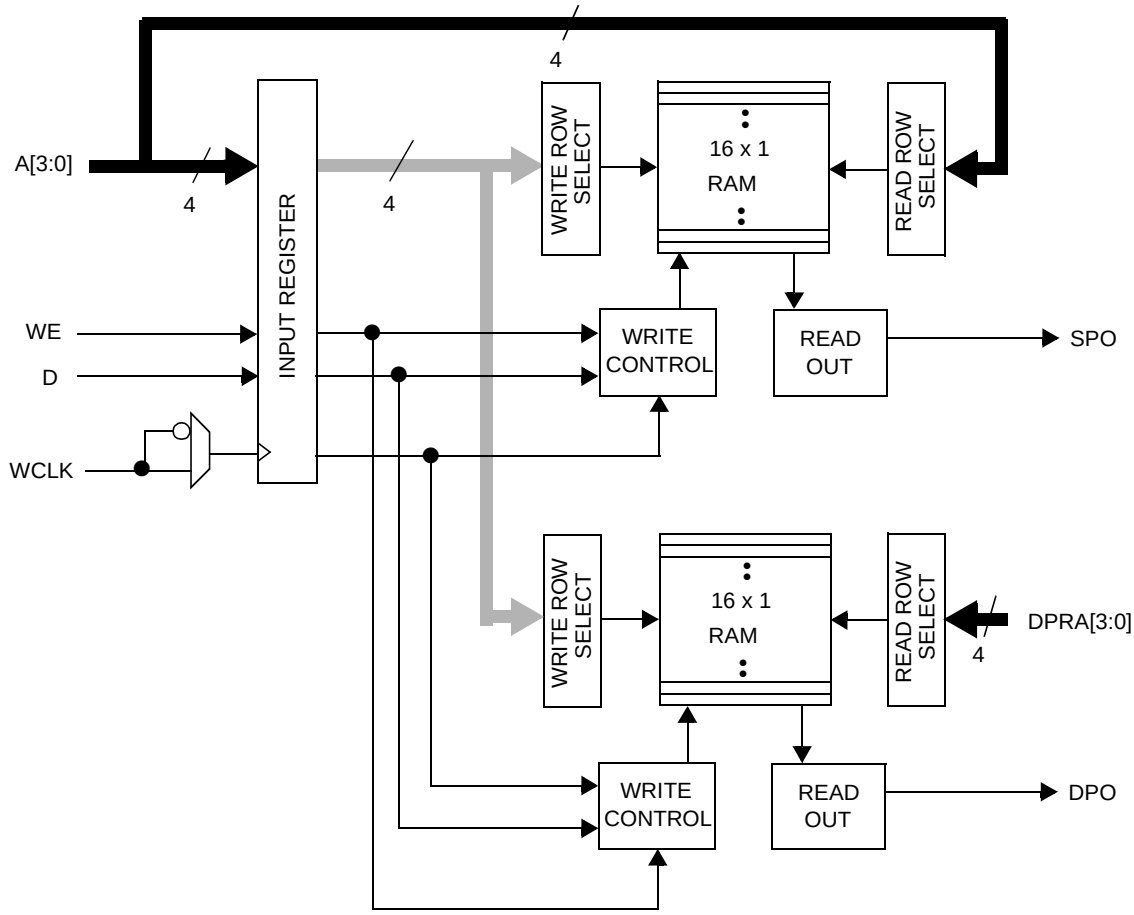
The WE input is active High and cannot be inverted within the CLB.

Allowing for settling time, the data on the SPO output reflects the contents of the RAM location currently addressed. When the address changes, following the asynchronous delay T_{ILO}, the data stored at the new address location will appear on SPO. If the data at a particular RAM address is overwritten, after the delay T_{WOS}, the new data will appear on SPO.

Dual-Port Mode

In dual-port mode, the function generators (F-LUT and G-LUT) are used to create a 16 x 1 dual-port memory. Of the two data ports available, one permits read and write operations at the address specified by A[3:0] while the second provides only for read operations at the address specified independently by DPRA[3:0]. As a result, simultaneous read/write operations at different addresses (or even at the same address) are supported.

The functional organization of the 16 x 1 dual-port RAM is shown in Figure 14.



igure 14: Logic Diagram for the Dual-Port RAM

The dual-port RAM signals and the CLB signals from which they are originally derived are shown in Table 47.

Table 47: Dual-Port RAM Signals

RAM Signal	Function	CLB Signal
D	Data In	DIN
A[3:0]	Read Address for Single-Port. Write Address for Single-Port and Dual-Port.	F_1-F_4
DPRA[3:0]	Read Address for Dual-Port	G_1-G_4
WE	Write Enable	SR
WCLK	Clock	K
SPO	Single Port Out (addressed by A[3:0])	F_{OUT}
DPO	Dual Port Out (addressed by DPRA[3:0])	G_{OUT}

The RAM16X1D primitive used to instantiate the dual-port RAM consists of an upper and a lower 16 x 1 memory array. The address port labeled A[3:0] supplies both the read and write addresses for the lower memory array, which behaves the same as the 16 x 1 single-port RAM array described previously. Single Port Out (SPO) serves as the data output for the lower memory. Therefore, SPO reflects the data at address A[3:0].

The other address port, labeled DPRA[3:0] for Dual Port Read Address, supplies the read address for the upper memory. The write address for this memory, however, comes from the address A[3:0]. Dual Port Out (DPO) serves as the data output for the upper memory. Therefore, DPO reflects the data at address DPRA[3:0].

By using A[3:0] for the write address and DPRA[3:0] for the read address, and reading only the DPO output, a FIFO that can read and write simultaneously is easily generated. The simultaneous read/write capability possible with the dual-port RAM can provide twice the effective data throughput of a single-port RAM alternating read and write operations.

The timing relationships for the dual-port RAM mode are shown in Figure 13.

Note that write operations to RAM are synchronous (edge-triggered); however, data access is asynchronous.

Initializing RAM at FPGA Configuration

Both RAM and ROM implementations in the Spartan/XL families are initialized during device configuration. The initial contents are defined via an INIT attribute or property attached to the RAM or ROM symbol, as described in the schematic library guide. If not defined, all RAM contents are initialized to zeros, by default.

RAM initialization occurs only during device configuration. The RAM content is not affected by GSR.

More Information on using RAM inside CLBs

Three application notes are available from Xilinx that discuss synchronous (edge-triggered) RAM: "*Xilinx Edge-Triggered and Dual-Port RAM Capability,*" "*Implementing FIFOs in Xilinx RAM,*" and "*Synchronous and Asynchronous FIFO Designs*." All three application notes apply to both the Spartan and the Spartan-XL families.

Fast Carry Logic

Each CLB F-LUT and G-LUT contains dedicated arithmetic logic for the fast generation of carry and borrow signals. This extra output is passed on to the function generator in the adjacent CLB. The carry chain is independent of normal routing resources. (See Figure 15.)

Dedicated fast carry logic greatly increases the efficiency and performance of adders, subtractors, accumulators, comparators and counters. It also opens the door to many new applications involving arithmetic operation, where the previous generations of FPGAs were not fast enough or too inefficient. High-speed address offset calculations in microprocessor or graphics systems, and high-speed addition in digital signal processing are two typical applications.

The two 4-input function generators can be configured as a 2-bit adder with built-in hidden carry that can be expanded to any length. This dedicated carry circuitry is so fast and efficient that conventional speed-up methods like carry generate/propagate are meaningless even at the 16-bit level, and of marginal benefit at the 32-bit level. This fast carry logic is one of the more significant features of the Spartan and Spartan-XL families, speeding up arithmetic and counting functions.

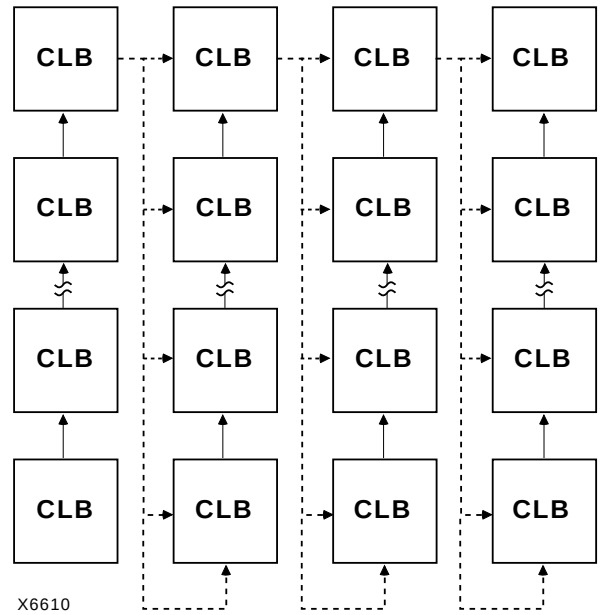


Figure 15: Available Spartan/XL Carry Propagation Paths

The carry chain in 5V Spartan devices can run either up or down. At the top and bottom of the columns where there are no CLBs above and below, the carry is propagated to the right. The default is always to propagate up the column, as shown in the figures. The carry chain in Spartan-XL devices can only run up the column, providing even higher speed.

Figure 16 on page 76 shows a Spartan/XL CLB with dedicated fast carry logic. The carry logic shares operand and control inputs with the function generators. The carry outputs connect to the function generators, where they are combined with the operands to form the sums.

Figure 17 on page 77 shows the details of the Spartan/XL carry logic. This diagram shows the contents of the box labeled "CARRY LOGIC" in Figure 16.

The fast carry logic can be accessed by placing special library symbols, or by using Xilinx Relationally Placed Macros (RPMs) that already include these symbols.

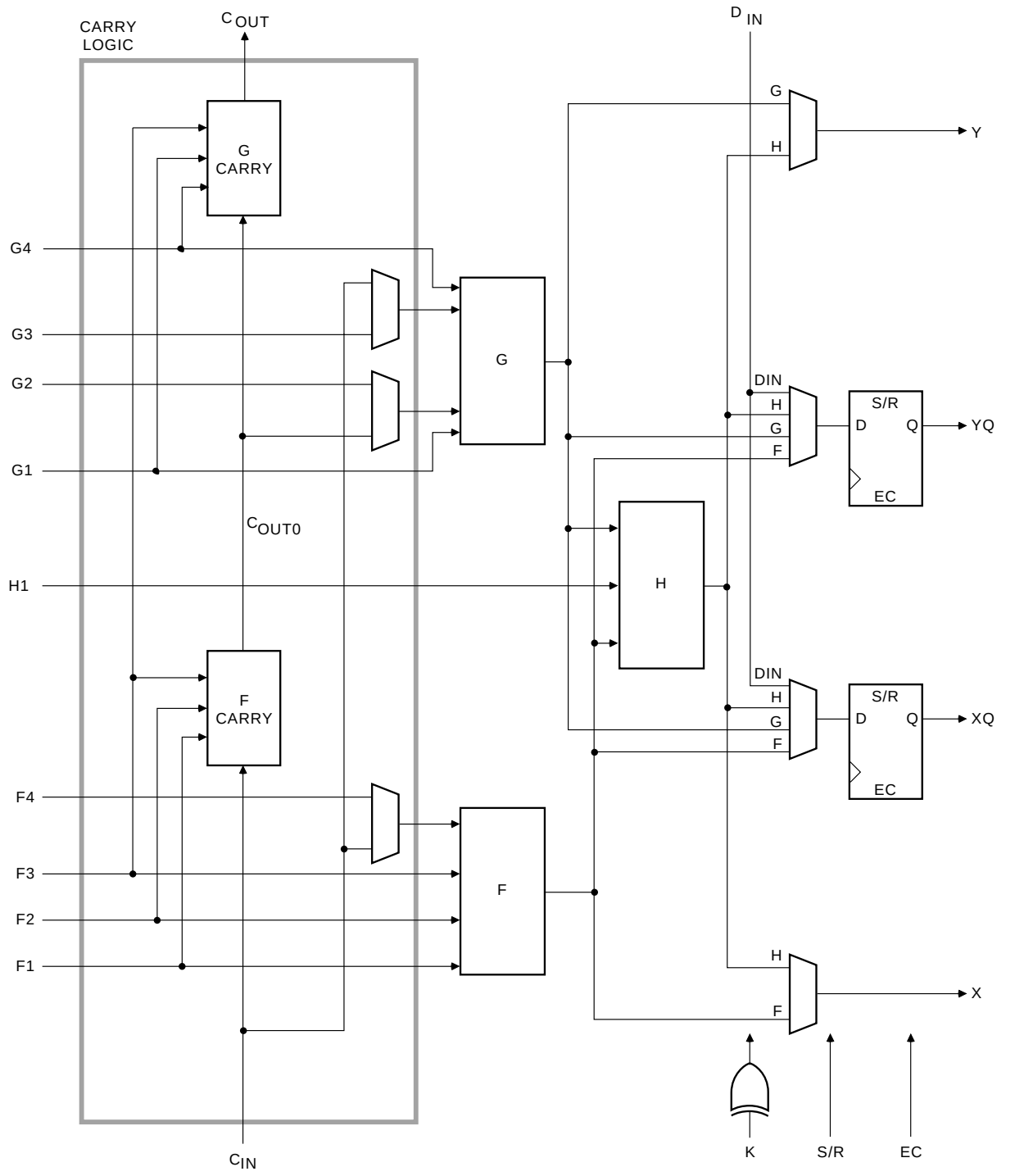


Figure 16: Fast Carry Logic in Spartan/XL CLB

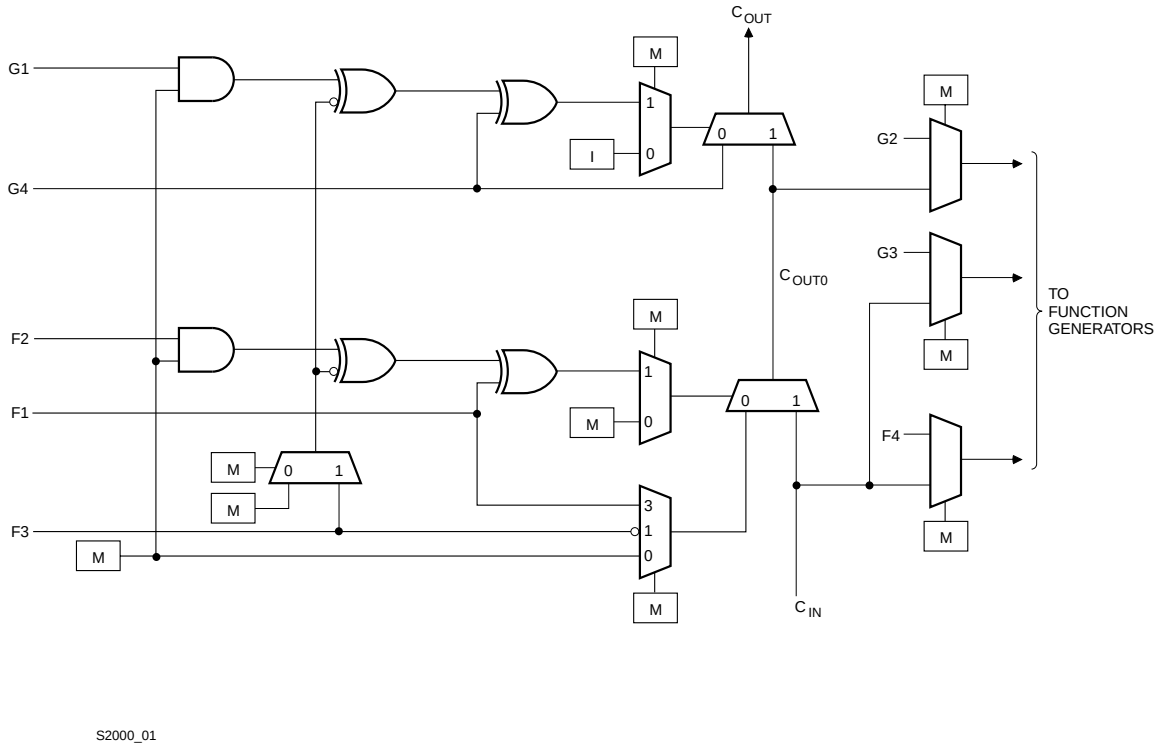


Figure 17: Detail of Spartan/XL Dedicated Carry Logic

3-State Long Line Drivers

A pair of 3-state buffers is associated with each CLB in the array. These 3-state buffers (BUFT) can be used to drive signals onto the nearest horizontal longlines above and below the CLB. They can therefore be used to implement multiplexed or bidirectional buses on the horizontal longlines, saving logic resources.

There is a weak keeper at each end of these two horizontal longlines. This circuit prevents undefined floating levels. However, it is overridden by any driver.

The buffer enable is an active High 3-state (i.e., an active Low enable), as shown in Table 48.

Three-State Buffer Example

Figure 18 shows how to use the 3-state buffers to implement a multiplexer. The selection is accomplished by the buffer 3-state signal.

Pay particular attention to the polarity of the T pin when using these buffers in a design. Active High 3-state (T) is identical to an active Low output enable, as shown in Table 48.

Table 48: Three-State Buffer Functionality

IN	T	OUT
X	1	Z
IN	0	IN

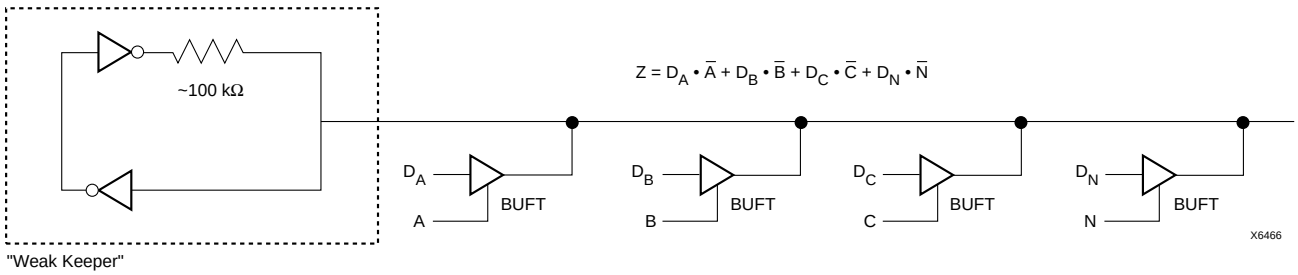


Figure 18: 3-state Buffers Implement a Multiplexer

On-Chip Oscillator

Spartan/XL devices include an internal oscillator. This oscillator is used to clock the power-on time-out, for configuration memory clearing, and as the source of CCLK in Master configuration mode. The oscillator runs at a nominal 8 MHz frequency that varies with process, V_{CC}, and temperature. The output frequency falls between 4 MHz and 10 MHz.

The oscillator output is optionally available after configuration. Any two of four resynchronized taps of a built-in divider are also available. These taps are at the fourth, ninth, fourteenth and nineteenth bits of the divider. Therefore, if the primary oscillator output is running at the nominal 8 MHz, the user has access to an 8-MHz clock, plus any two of 500 kHz, 16 kHz, 490 Hz and 15 Hz. These frequencies can vary by as much as -50% or +25%.

These signals can be accessed by placing the OSC4 library element in a schematic or in HDL code. The oscillator is automatically disabled after configuration if the OSC4 symbol is not used in the design.

Global Signals: GSR and GTS

Global Set/Reset

A separate Global Set/Reset line, as shown in Figure 3 on page 64 for the CLB and Figure 6 on page 65 for the IOB, sets or clears each flip-flop during power-up, reconfiguration, or when a dedicated Reset net is driven active. This global net (GSR) does not compete with other routing resources; it uses a dedicated distribution network.

Each flip-flop is configured as either globally set or reset in the same way that the local set/reset (SR) is specified. Therefore, if a flip-flop is set by SR, it is also set by GSR. Similarly, if in reset mode, it is reset by both SR and GSR.

GSR can be driven from any user-programmable pin as a global reset input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GSR pin of the STARTUP symbol. (See Figure 19.) A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the GSR signal. Alternatively, GSR can be driven from any internal node.

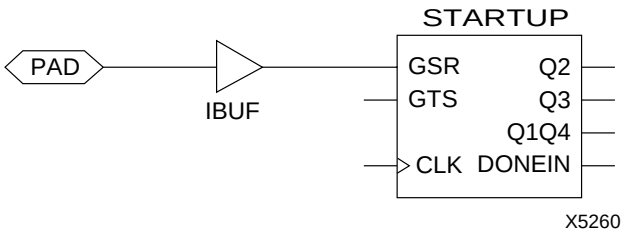


Figure 19: Schematic Symbols for Global Set/Reset

Global 3-State

A separate Global 3-state line (GTS) as shown in Figure 5 on page 66 forces all FPGA outputs to the high-impedance state, unless boundary scan is enabled and is executing an EXTEST instruction. GTS does not compete with other routing resources; it uses a dedicated distribution network.

GTS can be driven from any user-programmable pin as a global 3-state input. To use this global net, place an input pad and input buffer in the schematic or HDL code, driving the GTS pin of the STARTUP symbol. This is similar to what is shown in Figure 19 for GSR except the IBUF would be connected to GTS. A specific pin location can be assigned to this input using a LOC attribute or property, just as with any other user-programmable pad. An inverter can optionally be inserted after the input buffer to invert the sense of the Global 3-state signal. Alternatively, GTS can be driven from any internal node.

Boundary Scan

The "bed of nails" has been the traditional method of testing electronic assemblies. This approach has become less appropriate, due to closer pin spacing and more sophisticated assembly methods like surface-mount technology and multi-layer boards. The IEEE Boundary Scan Standard 1149.1 was developed to facilitate board-level testing of electronic assemblies. Design and test engineers can embed a standard test logic structure in their device to achieve high fault coverage for I/O and internal logic. This structure is easily implemented with a four-pin interface on any boundary scan compatible device. IEEE 1149.1-compatible devices may be serial daisy-chained together, connected in parallel, or a combination of the two.

The Spartan and Spartan-XL families implement IEEE 1149.1-compatible BYPASS, PRELOAD/SAMPLE and EXTEST boundary scan instructions. When the boundary scan configuration option is selected, three normal user I/O pins become dedicated inputs for these functions. Another user output pin becomes the dedicated boundary scan output. The details of how to enable this circuitry are covered later in this section.

By exercising these input signals, the user can serially load commands and data into these devices to control the driving of their outputs and to examine their inputs. This method is an improvement over bed-of-nails testing. It avoids the need to over-drive device outputs, and it reduces the user interface to four pins. An optional fifth pin, a reset for the control logic, is described in the standard but is not implemented in the Spartan/XL devices.

The dedicated on-chip logic implementing the IEEE 1149.1 functions includes a 16-state machine, an instruction register and a number of data registers. The functional details can be found in the IEEE 1149.1 specification and are also discussed in the Xilinx application note: "*Boundary Scan in FPGA Devices*."

Figure 20 is a diagram of the Spartan/XL boundary scan logic. It includes three bits of Data Register per IOB, the IEEE 1149.1 Test Access Port controller, and the Instruction Register with decodes.

Spartan/XL devices can also be configured through the boundary scan logic. See "Configuration Through the Boundary Scan Pins" on page 91.

Data Registers

The primary data register is the boundary scan register. For each IOB pin in the FPGA, bonded or not, it includes three bits for In, Out and 3-state Control. Non-IOB pins have appropriate partial bit population for In or Out only. PROGRAM, CCLK and DONE are not included in the boundary scan register. Each EXTEST CAPTURE-DR state captures all In, Out, and 3-state pins.

The data register also includes the following non-pin bits: TDO.T, and TDO.O, which are always bits 0 and 1 of the data register, respectively, and BSCANT.UPD, which is always the last bit of the data register. These three boundary scan bits are special-purpose Xilinx test signals.

The other standard data register is the single flip-flop BYPASS register. It synchronizes data being passed through the FPGA to the next downstream boundary scan device.

The FPGA provides two additional data registers that can be specified using the BSCAN macro. The FPGA provides two user pins (BSCAN.SEL1 and BSCAN.SEL2) which are the decodes of two user instructions. For these instructions, two corresponding pins (BSCAN.TDO1 and BSCAN.TDO2) allow user scan data to be shifted out on TDO. The data register clock (BSCAN.DRCK) is available for control of test logic which the user may wish to implement with CLBs. The NAND of TCK and RUN-TEST-IDLE is also provided (BSCAN.IDLE).

Instruction Set

The Spartan/XL boundary scan instruction set also includes instructions to configure the device and read back the configuration data. The instruction set is coded as shown in Table 49.

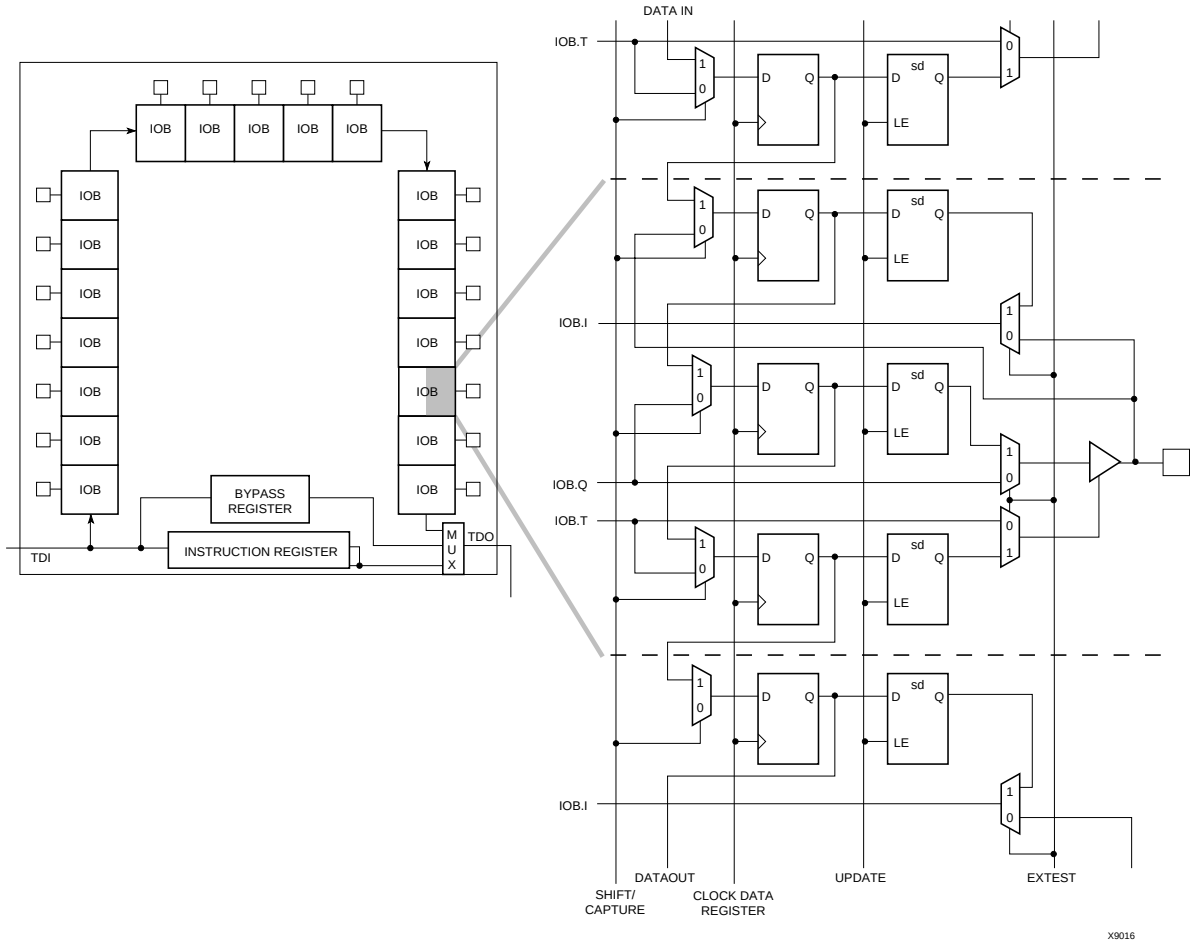


Figure 20: Spartan/XL Boundary Scan Logic

Table 49: Boundary Scan Instructions

Instruction			Test Selected	TDO Source	I/O Data Source
I2	I1	I0			
0	0	0	EXTEST	DR	DR
0	0	1	SAMPLE/ PRELOAD	DR	Pin/Logic
0	1	0	USER 1	BSCAN. TDO1	User Logic
0	1	1	USER 2	BSCAN. TDO2	User Logic
1	0	0	READBACK	Readback Data	Pin/Logic
1	0	1	CONFIGURE	DOUT	Disabled
1	1	0	IDCODE (Spartan-XL only)	IDCODE Register	—
1	1	1	BYPASS	Bypass Register	—

Bit Sequence

The bit sequence within each IOB is: In, Out, 3-state. The input-only pins contribute only the In bit to the boundary scan I/O data register, while the output-only pins contributes all three bits.

The first two bits in the I/O data register are TDO.T and TDO.O, which can be used for the capture of internal signals. The final bit is BSCANT.UPD, which can be used to drive an internal net. These locations are primarily used by Xilinx for internal testing.

From a cavity-up view of the chip (as shown in the FPGA Editor), starting in the upper right chip corner, the boundary scan data-register bits are ordered as shown in Figure 21. The device-specific pinout tables for the Spartan/XL devices include the boundary scan locations for each IOB pin.

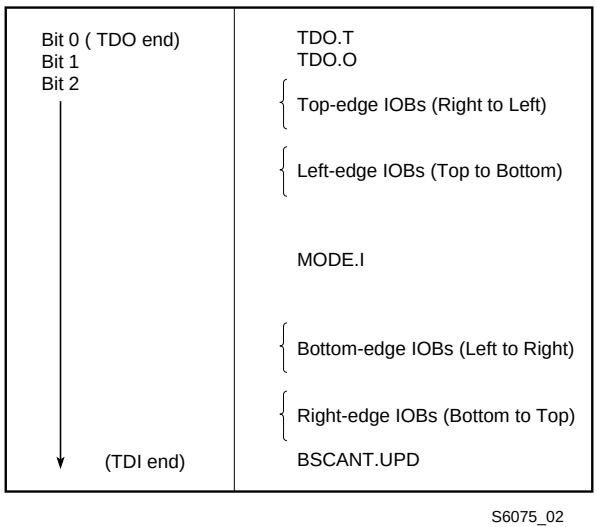


Figure 21: Boundary Scan Bit Sequence

BSDL (Boundary Scan Description Language) files for Spartan/XL devices are available on the Xilinx website in the File Download area. Note that the 5V Spartan devices and 3V Spartan-XL devices have different BSDL files.

Including Boundary Scan in a Design

If boundary scan is only to be used during configuration, no special schematic elements need be included in the schematic or HDL code. In this case, the special boundary scan pins TDI, TMS, TCK and TDO can be used for user functions after configuration.

To indicate that boundary scan remain enabled after configuration, place the BSCAN library symbol and connect the TDI, TMS, TCK and TDO pad symbols to the appropriate pins, as shown in Figure 22.

Even if the boundary scan symbol is used in a schematic, the input pins TMS, TCK, and TDI can still be used as inputs to be routed to internal logic. Care must be taken not to force the chip into an undesired boundary scan state by inadvertently applying boundary scan input patterns to these pins. The simplest way to prevent this is to keep TMS High, and then apply whatever signal is desired to TDI and TCK.

Avoiding Inadvertent Boundary Scan

If TMS or TCK is used as user I/O, care must be taken to ensure that at least one of these pins is held constant during configuration. In some applications, a situation may occur where TMS or TCK is driven during configuration. This may cause the device to go into boundary scan mode and disrupt the configuration process.

To prevent activation of boundary scan during configuration, do either of the following:

- TMS: Tie High to put the Test Access Port controller in a benign RESET state
- TCK: Tie High or Low—do not toggle this clock input.

For more information regarding boundary scan, refer to the Xilinx Application Note, "*Boundary Scan in FPGA Devices*."

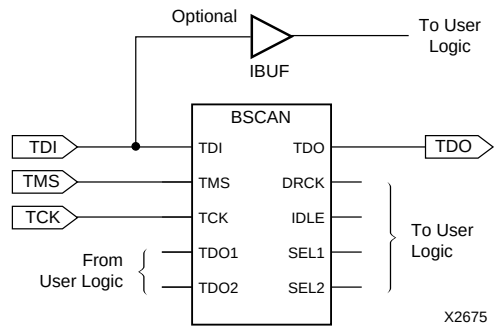


Figure 22: Boundary Scan Schematic Example

Boundary Scan Enhancements (Spartan-XL only)

Spartan-XL devices have improved boundary scan functionality and performance in the following areas:

IDCODE: The IDCODE register is supported. By using the IDCODE, the device connected to the JTAG port can be determined. The use of the IDCODE enables selective configuration dependent on the FPGA found.

The IDCODE register has the following binary format:

```
vvvv:ffff:fffa:aaaa:aaaa:cccc:cccc:ccc1
```

where

c = the company code (49h for Xilinx)

a = the array dimension in CLBs (ranges from 0Ah for XCS05XL to 1Ch for XCS40XL)

f = the family code (02h for Spartan-XL family)

v = the die version number (currently 0h)

Table 50: IDCODEs Assigned to Spartan-XL FPGAs

FPGA	IDCODE
XCS05XL	0040A093h
XCS10XL	0040E093h
XCS20XL	00414093h
XCS30XL	00418093h
XCS40XL	0041C093h

Configuration State: The configuration state is available to JTAG controllers.

Configuration Disable: The JTAG port can be prevented from configuring the FPGA.

TCK Startup: TCK can now be used to clock the start-up block in addition to other user clocks.

CCLK Holdoff: Changed the requirement for Boundary Scan Configure or EXTEST to be issued prior to the release of INIT pin and CCLK cycling.

Reissue Configure: The Boundary Scan Configure can be reissued to recover from an unfinished attempt to configure the device.

Bypass FF: Bypass FF and IOB is modified to provide DRCLOCK only during BYPASS for the bypass flip-flop, and during EXTEST or SAMPLE/PRELOAD for the IOB register.

Power Down (Spartan-XL Only)

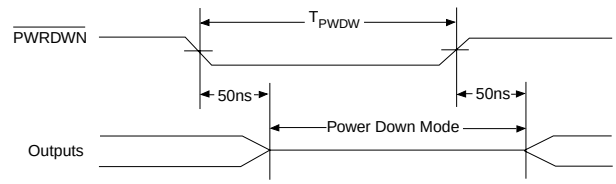
All Spartan/XL devices use a combination of efficient segmented routing and advanced process technology to provide low power consumption under all conditions. The 3.3V Spartan-XL family adds a dedicated active Low Power Down pin ($\overline{\text{PWRDWN}}$) to reduce supply current to 100 µA typical. The $\overline{\text{PWRDWN}}$ pin takes advantage of one of the unused No Connect locations on the 5V Spartan device. The user must de-select the "5V Tolerant I/Os" option in the Configuration Options to achieve the specified Power Down current. The $\overline{\text{PWRDWN}}$ pin has a default internal pull-up resistor, allowing it to be left unconnected if unused.

V_{CC} must continue to be supplied during Power-down, and configuration data is maintained. When the $\overline{\text{PWRDWN}}$ pin is pulled Low, the input and output buffers are disabled. The inputs are internally forced to a logic Low level, including the MODE pins, DONE, CCLK, and TDO, and all internal pull-up resistors are turned off. The $\overline{\text{PROGRAM}}$ pin is not affected by Power Down. The GSR net is asserted during Power Down, initializing all the flip-flops to their start-up state.

$\overline{\text{PWRDWN}}$ has a minimum pulse width of 50 ns (Figure 23). On entering the Power-down state, the inputs will be disabled and the flip-flops set/reset, and then the outputs are disabled about 10 ns later. The user may prefer to assert the GTS or GSR signals before $\overline{\text{PWRDWN}}$ to affect the order of events. When the $\overline{\text{PWRDWN}}$ signal is returned High, the inputs will be enabled first, followed immediately by the release of the GSR signal initializing the flip-flops. About 10 ns later, the outputs will be enabled. Allow 50 ns after the release of $\overline{\text{PWRDWN}}$ before using the device.

Power Down retains the configuration, but loses all data stored in the device flip-flops. All inputs are interpreted as Low, but the internal combinatorial logic is fully functional. Make sure that the combination of all inputs Low and all flip-flops set or reset in your design will not generate internal oscillations, or create permanent bus contention by activating internal bus drivers with conflicting data onto the same long line.

During configuration, the $\overline{\text{PWRDWN}}$ pin must be High. If the Power Down state is entered before or during configuration, the device will restart configuration once the $\overline{\text{PWRDWN}}$ signal is removed. Note that the configuration pins are affected by Power Down and may not reflect their normal function. If there is an external pull-up resistor on the DONE pin, it will be High during Power Down even if the device is not yet configured. Similarly, if $\overline{\text{PWRDWN}}$ is asserted before configuration is completed, the $\overline{\text{INIT}}$ pin will not indicate status information.



Description	Symbol	Min	Max
Power Down Time	T PWD	50ns	-
Power Down Pulse Width	T PWDW	50ns	-

Figure 23: $\overline{\text{PWRDWN}}$ Pulse Timing

Note that the $\overline{\text{PWRDWN}}$ pin is not part of the Boundary Scan chain. Therefore, the Spartan-XL family has a separate set of BSDL files than the 5V Spartan family. Boundary scan logic is not usable during Power Down.

Configuration and Test

Configuration is the process of loading design-specific programming data into one or more FPGAs to define the functional operation of the internal blocks and their interconnections. This is somewhat like loading the command registers of a programmable peripheral chip. Spartan/XL devices use several hundred bits of configuration data per CLB and its associated interconnects. Each configuration bit defines the state of a static memory cell that controls either a function look-up table bit, a multiplexer input, or an interconnect pass transistor. The Xilinx development system translates the design into a netlist file. It automatically partitions, places and routes the logic and generates the configuration data in PROM format.

Configuration Mode Control

5V Spartan devices have two configuration modes.

- MODE = 1 sets Slave Serial mode
- MODE = 0 sets Master Serial mode

3V Spartan-XL devices have three configuration modes.

- M1/M0 = 11 sets Slave Serial mode
- M1/M0 = 10 sets Master Serial mode
- M1/M0 = 0X sets Express mode

In addition to these modes, the device can be configured through the Boundary Scan logic (See “Configuration Through the Boundary Scan Pins” on page 91.).

The Mode pins are sampled prior to starting configuration to determine the configuration mode. After configuration, these pin are unused. The Mode pins have a weak pull-up resistor of 20 kΩ to 100 kΩ turned on during configuration. With the Mode pins High, Slave Serial mode is selected, which is the most popular configuration mode. Therefore, for the most common configuration mode, the Mode pins can be left unconnected. If the Master Serial mode is desired, the MODE/M0 pin should be connected directly to GND, or through a pull-down resistor of 1 KΩ or less.

During configuration, some of the I/O pins are used temporarily for the configuration process. All pins used during configuration are shown in Table 51 and Table 52.

Table 51: Pin Functions During Configuration (Spartan family only)

CONFIGURATION MODE <MODE Pin>		
SLAVE SERIAL <High>	MASTER SERIAL <Low>	USER OPERATION
MODE (I)	MODE (I)	MODE
HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)
DIN (I)	DIN (I)	I/O
DOUT	DOUT	SGCK4-I/O
TDI	TDI	TDI-I/O
TCK	TCK	TCK-I/O
TMS	TMS	TMS-I/O
TDO	TDO	TDO-(O)
		ALL OTHERS

Notes
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Table 52: Pin Functions During Configuration (Spartan-XL family only)

CONFIGURATION MODE <M1:M0>			
SLAVE SERIAL <1:1>	MASTER SERIAL <1:0>	EXPRESS <0:X>	USER OPERATION
M1(HIGH) (I)	M1(HIGH) (I)	M1(LOW) (I)	M1
M0(HIGH) (I)	M0(LOW) (I)	M0 (I)	M0
HDC (HIGH)	HDC (HIGH)	HDC (HIGH)	I/O
$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	$\overline{\text{LDC}}$ (LOW)	I/O
$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	$\overline{\text{INIT}}$	I/O
DONE	DONE	DONE	DONE
$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$ (I)	$\overline{\text{PROGRAM}}$
CCLK (I)	CCLK (O)	CCLK (I)	CCLK (I)
		DATA 7 (I)	I/O
		DATA 6 (I)	I/O
		DATA 5 (I)	I/O
		DATA 4 (I)	I/O
		DATA 3 (I)	I/O
		DATA 2 (I)	I/O
		DATA 1 (I)	I/O
DIN (I)	DIN (I)	DATA 0 (I)	I/O
DOUT	DOUT	DOUT	GCK6-I/O
TDI	TDI	TDI	TDI-I/O
TCK	TCK	TCK	TCK-I/O
TMS	TMS	TMS	TMS-I/O
TDO	TDO	TDO	TDO-(O)
		CS1	I/O
			ALL OTHERS

Notes
1. A shaded table cell represents the internal pull-up used before and during configuration.
2. (I) represents an input; (O) represents an output.
3. $\overline{\text{INIT}}$ is an open-drain output during configuration.

Master Serial Mode

The Master serial mode uses an internal oscillator to generate a Configuration Clock (CCLK) for driving potential slave devices and the Xilinx serial-configuration PROM (SPROM). The CCLK speed is selectable as either 1 MHz (default) or 8 MHz. Configuration always starts at the default slow frequency, then can switch to the higher frequency during the first frame. Frequency tolerance is -50% to +25%.

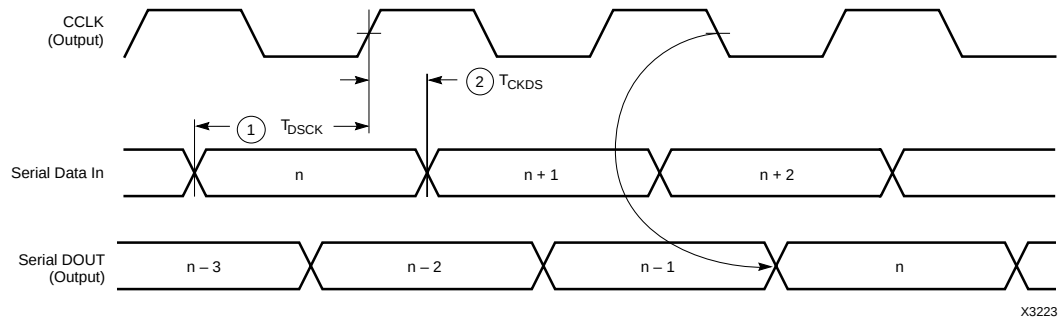
In Master Serial mode, the CCLK output of the device drives a Xilinx SPROM that feeds the FPGA DIN input. Each rising edge of the CCLK output increments the Serial PROM internal address counter. The next data bit is put on the SPROM data output, connected to the FPGA DIN pin. The FPGA accepts this data on the subsequent rising CCLK edge.

When used in a daisy-chain configuration the Master Serial FPGA is placed as the first device in the chain and is referred to as the lead FPGA. The lead FPGA presents the preamble data, and all data that overflows the lead device, on its DOUT pin. There is an internal pipeline delay of 1.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge. See the timing diagram in Figure 24.

In the bitstream generation software, the user can specify Fast Configuration Rate, which, starting several bits into the first frame, increases the CCLK frequency by a factor of eight. For actual timing values please refer to the specification section. Be sure that the serial PROM and slaves are fast enough to support this data rate. Devices such as XC3000A and XC3100A do not support the Fast Configuration Rate option.

The SPROM CE input can be driven from either $\overline{\text{LDC}}$ or DONE. Using $\overline{\text{LDC}}$ avoids potential contention on the DIN pin, if this pin is configured as user I/O, but $\overline{\text{LDC}}$ is then restricted to be a permanently High user output after configuration. Using DONE can also avoid contention on DIN, provided the Early DONE option is invoked.

Figure 25 shows a full master/slave system. The leftmost device is in Master Serial mode, all other devices in the chain are in Slave Serial mode.



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DSCK}	20		ns
	DIN hold	2	T_{CKDS}	0		ns

Notes: 1. At power-up, V_{CC} must rise from 2.0V to V_{CC} min in less than 25 ms, otherwise delay configuration by pulling $\overline{\text{PROGRAM}}$ Low until V_{CC} is valid.
2. Master Serial mode timing is based on testing in slave mode.

Figure 24: Master Serial Mode Programming Switching Characteristics

Slave Serial Mode

In Slave Serial mode, the FPGA receives serial configuration data on the rising edge of CCLK and, after loading its configuration, passes additional data out, resynchronized on the next falling edge of CCLK.

In this mode, an external signal drives the CCLK input of the FPGA (most often from a Master Serial device). The serial configuration bitstream must be available at the DIN input of the lead FPGA a short setup time before each rising CCLK edge.

The lead FPGA then presents the preamble data—and all data that overflows the lead device—on its DOUT pin. There is an internal delay of 0.5 CCLK periods, which means that DOUT changes on the falling CCLK edge, and the next FPGA in the daisy chain accepts data on the subsequent rising CCLK edge.

Figure 25 shows a full master/slave system. A Spartan/XL device in Slave Serial mode should be connected as shown in the third device from the left.

Slave Serial is the default mode if the Mode pins are left unconnected, as they have weak pull-up resistors during configuration.

Multiple slave devices with identical configurations can be wired with parallel DIN inputs. In this way, multiple devices can be configured simultaneously.

Serial Daisy Chain

Multiple devices with different configurations can be connected together in a "daisy chain," and a single combined bitstream used to configure the chain of slave devices.

To configure a daisy chain of devices, wire the CCLK pins of all devices in parallel, as shown in Figure 25. Connect the DOUT of each device to the DIN of the next. The lead or master FPGA and following slaves each passes resynchronized configuration data coming from a single source. The header data, including the length count, is passed through and is captured by each FPGA when it recognizes the 0010 preamble. Following the length-count data, each FPGA outputs a High on DOUT until it has received its required number of data frames.

After an FPGA has received its configuration data, it passes on any additional frame start bits and configuration data on DOUT. When the total number of configuration clocks applied after memory initialization equals the value of the 24-bit length count, the FPGAs begin the start-up sequence and become operational together. FPGA I/O are normally released two CCLK cycles after the last configuration bit is received.

The daisy-chained bitstream is not simply a concatenation of the individual bitstreams. The PROM File Formatter must be used to combine the bitstreams for a daisy-chained configuration.

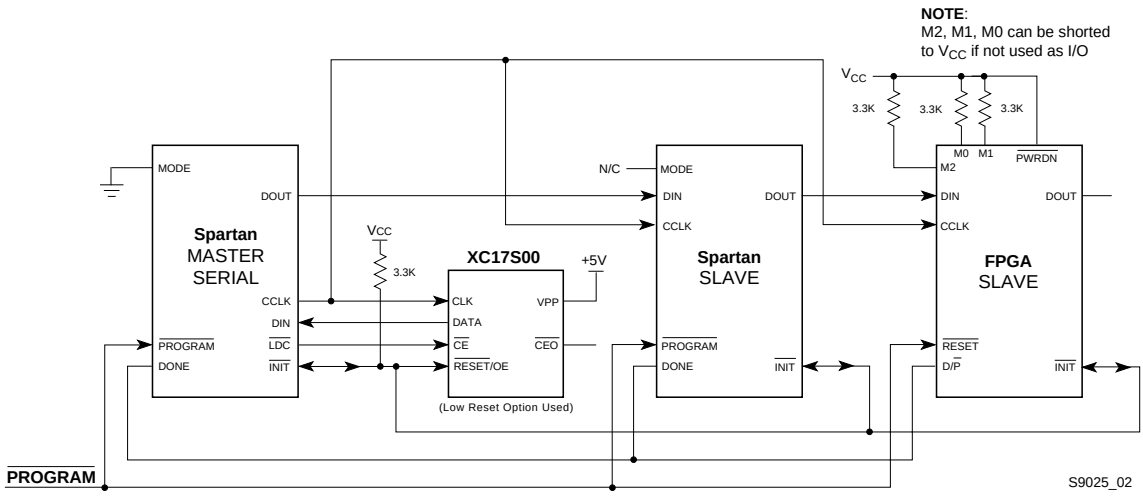
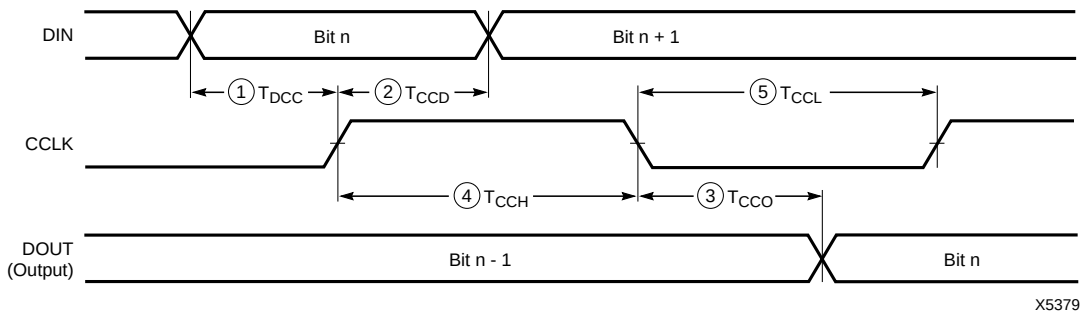


Figure 25: Master/Slave Serial Mode Circuit Diagram



	Description	Symbol		Min	Max	Units
CCLK	DIN setup	1	T_{DCC}	20		ns
	DIN hold	2	T_{CCD}	0		ns
	DIN to DOUT	3	T_{CCO}		30	ns
	High time	4	T_{CCH}	45		ns
	Low time	5	T_{CCL}	45		ns
	Frequency		F_{CC}		10	MHz

Note: Configuration must be delayed until the $\overline{INIT}$ pins of all daisy-chained FPGAs are High.

Figure 26: Slave Serial Mode Programming Switching Characteristics

Express Mode (Spartan-XL only)

Express mode is similar to Slave Serial mode, except that data is processed one byte per CCLK cycle instead of one bit per CCLK cycle. An external source is used to drive CCLK, while byte-wide data is loaded directly into the configuration data shift registers (Figure 27). A CCLK frequency of 1 MHz is equivalent to a 8 MHz serial rate, because eight bits of configuration data are loaded per CCLK cycle. Express mode does not support CRC error checking, but does support constant-field error checking. A length count is not used in Express mode.

Express mode must be specified as an option to the development system. The Express mode bitstream is not compatible with the other configuration modes (see Table 53 on page 88.) Express mode is selected by a <0X> on the Mode pins (M1, M0).

The first byte of parallel configuration data must be available at the D inputs of the FPGA a short setup time before the second rising CCLK edge. Subsequent data bytes are clocked in on each consecutive rising CCLK edge (Figure 28).

Pseudo Daisy Chain

Multiple devices with different configurations can be configured in a pseudo daisy chain provided that all of the devices are in Express mode. A single combined bitstream is used to configure the chain of Express mode devices. CCLK pins are tied together and D0-D7 pins are tied together for all devices along the chain. A status signal is passed from DOUT to CS1 of successive devices along the chain. Frame data is accepted only when CS1 is High and the device's configuration memory is not already full. The lead device in the chain has its CS1 input tied High (or floating, since there is an internal pull-up). The status pin DOUT is pulled Low after the header is received by all devices, and remains Low until the device's configuration memory is full. DOUT is then pulled High to signal the next device in the chain to accept the configuration data on the D0-D7 bus.

The DONE pins of all devices in the chain should be tied together, with one or more active internal pull-ups. If a large number of devices are included in the chain, deactivate some of the internal pull-ups, since the Low-driving DONE pin of the last device in the chain must sink the current from all pull-ups in the chain. The DONE pull-up is activated by default. It can be deactivated using a development system option.

The requirement that all DONE pins in a daisy chain be wired together applies only to Express mode, and only if all devices in the chain are to become active simultaneously. All Spartan-XL devices in Express mode are synchronized to the DONE pin. User I/Os for each device become active after the DONE pin for that device goes High. (The exact timing is determined by development system options.) Since the DONE pin is open-drain and does not drive a High value, tying the DONE pins of all devices together prevents all devices in the chain from going High until the last device in the chain has completed its configuration cycle. If the DONE pin of a device is left unconnected, the device becomes active as soon as that device has been configured. Because only Spartan-XL, XC4000XLA/XV, and XC5200 devices support Express mode, only these devices can be used to form an Express mode daisy chain.

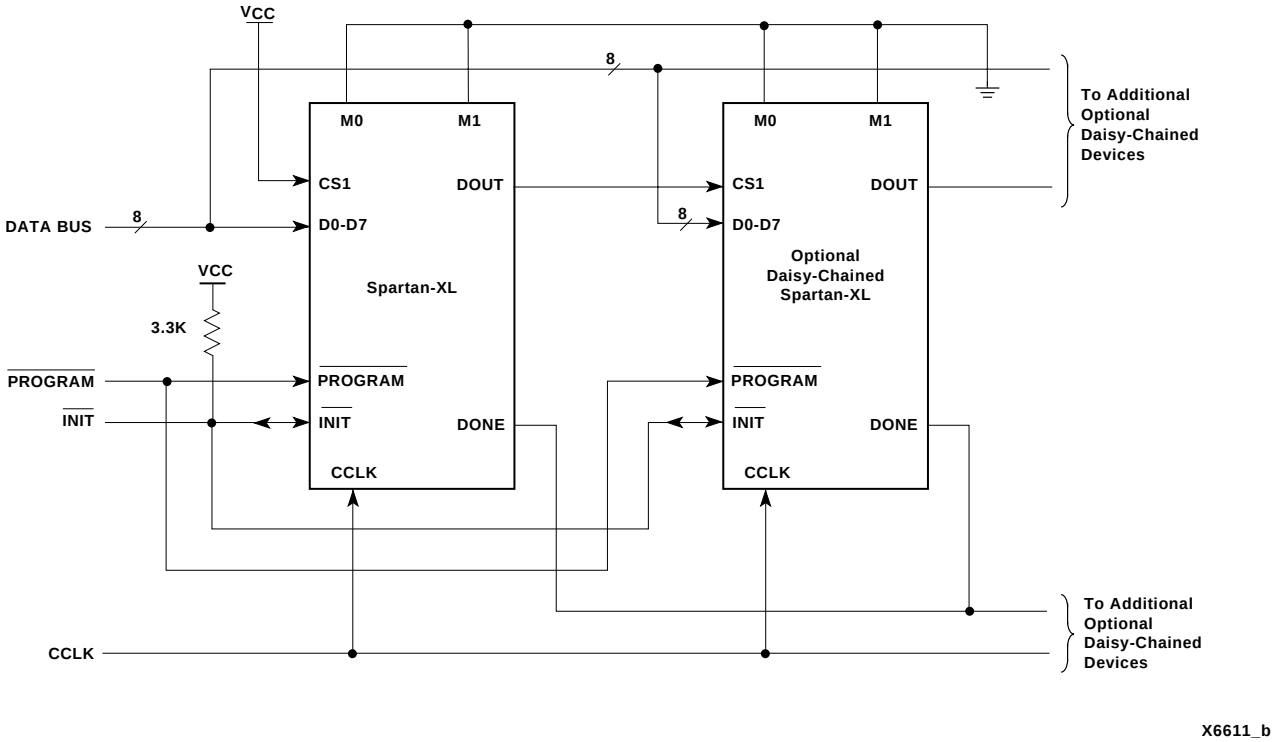
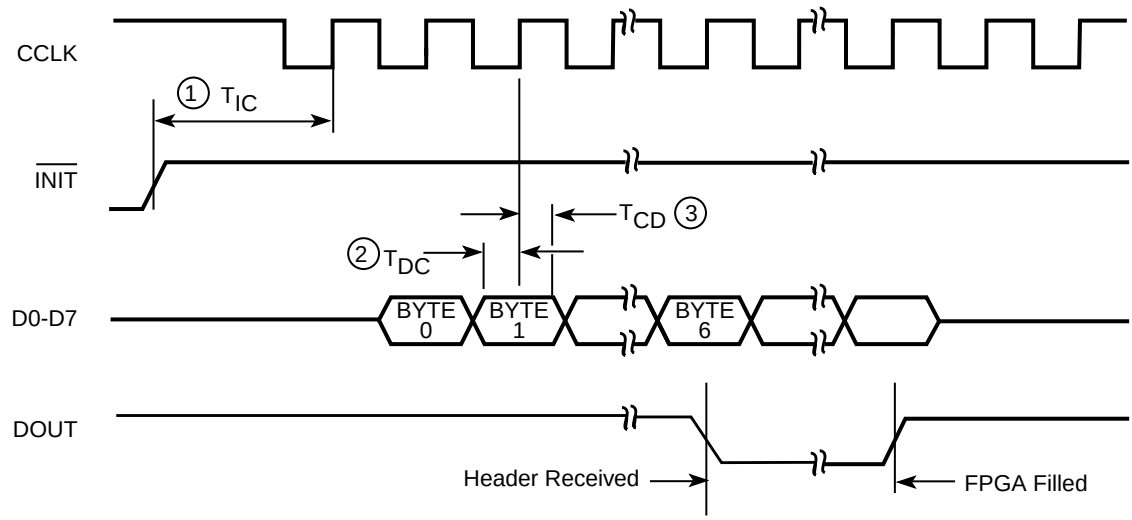


Figure 27: Express Mode Circuit Diagram

	Description		Symbol	Min	Max	Units
CCLK	$\overline{INIT}$ (High) setup time	1	T_{IC}	5		µs
	D0 - D7 setup time	2	T_{DC}	20		ns
	D0 - D7 hold time	3	T_{CD}	0		ns
	CCLK High time		T_{CCH}	45		ns
	CCLK Low time		T_{CCL}	45		ns
	CCLK Frequency		F_{CC}		10	MHz



Note: If not driven by the preceding DOUT, CS1 *must* remain High until the device is fully configured.

Figure 28: Express Mode Programming Switching Characteristics

Setting CCLK Frequency

In Master mode, CCLK can be generated in either of two frequencies. In the default slow mode, the frequency ranges from 0.5 MHz to 1.25 MHz for Spartan/XL devices. In fast CCLK mode, the frequency ranges from 4 MHz to 10 MHz for Spartan/XL devices. The frequency is changed to fast by an option when running the bitstream generation software.

Data Stream Format

The data stream ("bitstream") format is identical for both serial configuration modes, but different for the Spartan-XL Express mode. In Express mode, the device becomes active when DONE goes High, therefore no length count is required. Additionally, CRC error checking is not supported in Express mode. The data stream format is shown in Table 53. Bit-serial data is read from left to right. Express mode data is shown with D0 at the left and D7 at the right.

The configuration data stream begins with a string of eight ones, a preamble code, followed by a 24-bit length count and a separator field of ones (or 24 fill bits, in Spartan-XL Express mode). This header is followed by the actual configuration data in frames. The length and number of frames depends on the device type (see Table 54). Each frame begins with a start field and ends with an error check. In serial modes, a postamble code is required to signal the end of data for a single device. In all cases, additional start-up bytes of data are required to provide four clocks for the startup sequence at the end of configuration. Long daisy chains require additional startup bytes to shift the last data through the chain. All start-up bytes are "don't cares".

Table 53: Spartan/XL Data Stream Formats

Data Type	Serial Modes (D0...)	Express Mode (D0-D7) (Spartan-XL only)
Fill Byte	11111111b	FFFFh
Preamble Code	0010b	11110010b
Length Count	COUNT(23:0)	COUNT(23:0)[1]
Fill Bits	1111b	—
Field Check Code	—	11010010b
Start Field	0b	11111110b
Data Frame	DATA(n-1:0)	DATA(n-1:0)
CRC or Constant Field Check	xxxx (CRC) or 0110b	11010010b
Extend Write Cycle	—	FFFFFFFFFFh
Postamble	01111111b	—
Start-Up Bytes	FFh	FFFFFFFFFFFFFFh[2]

LEGEND:

Unshaded	Once per bitstream
Light	Once per data frame
Dark	Once per device

Note 1: Not used by configuration logic.
Note 2: Development system may add more start-up bytes.

A selection of CRC or non-CRC error checking is allowed by the bitstream generation software. The Spartan-XL Express mode only supports non-CRC error checking. The non-CRC error checking tests for a designated end-of-frame field for each frame. For CRC error checking, the software calculates a running CRC and inserts a unique four-bit partial check at the end of each frame. The 11-bit CRC check of the last frame of an FPGA includes the last seven data bits.

Detection of an error results in the suspension of data loading before DONE goes High, and the pulling down of the $\overline{\text{INIT}}$ pin. In Master serial mode, CCLK continues to operate externally. The user must detect $\overline{\text{INIT}}$ and initialize a new configuration by pulsing the $\overline{\text{PROGRAM}}$ pin Low or cycling V_{CC}.

Cyclic Redundancy Check (CRC) for Configuration and Readback

The Cyclic Redundancy Check is a method of error detection in data transmission applications. Generally, the transmitting system performs a calculation on the serial bitstream. The result of this calculation is tagged onto the data stream as additional check bits. The receiving system performs an identical calculation on the bitstream and compares the result with the received checksum.

Each data frame of the configuration bitstream has four error bits at the end, as shown in Table 53. If a frame data error is detected during the loading of the FPGA, the configuration process with a potentially corrupted bitstream is terminated. The FPGA pulls the $\overline{\text{INIT}}$ pin Low and goes into a Wait state.

Table 54: Spartan/XL Program Data

Device	XCS05		XCS10		XCS20		XCS30		XCS40	
Max System Gates	5,000		10,000		20,000		30,000		40,000	
CLBs (Row x Col.)	100 (10 x 10)		196 (14 x 14)		400 (20 x 20)		576 (24 x 24)		784 (28 x 28)	
IOBs	80		112		160		192		224	
Part Number	XCS05	XCS05XL	XCS10	XCS10XL	XCS20	XCS20XL	XCS30	XCS30XL	XCS40	XCS40XL
Supply Voltage	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V	5V	3.3V
Bits per Frame	126	127	166	167	226	227	266	267	306	307
Frames	428	429	572	573	788	789	932	933	1,076	1,077
Program Data	53,936	54,491	94,960	95,699	178,096	179,111	247,920	249,119	329,264	330,647
PROM Size (bits)	53,984	54,536	95,008	95,744	178,144	179,160	247,968	249,168	329,312	330,696
Serial PROM	17S05	17S05XL	17S10	17S10XL	17S20	17S20XL	17S30	17S30XL	17S40	17S40XL
Express Mode PROM Size (bits)		79,064		128,480		221,048		298,688		387,848

Notes: 1.Bits per Frame = (10 x number of rows) + 7 for the top + 13 for the bottom + 1 + 1 start bit + 4 error check bits (+ 1 for Spartan-XL device)
Number of Frames = (36 x number of columns) + 26 for the left edge + 41 for the right edge + 1 (+ 1 for Spartan-XL device)
Program Data = (Bits per Frame x Number of Frames) + 8 postamble bits
PROM Size = Program Data + 40 (header) + 8, rounded up to the nearest byte
2.The user can add more "1" bits as leading dummy bits in the header, or, if CRC = off, as trailing dummy bits at the end of any frame, following the four error check bits. However, the Length Count value **must** be adjusted for all such extra "one" bits, even for extra leading ones at the beginning of the header.
3. Express mode adds 57 (XCS05XL, XCS10XL), or 53 (XCS20XL, XCS30XL, XCS40XL) bits per frame, + 24 additional bits.

During Readback, 11 bits of the 16-bit checksum are added to the end of the Readback data stream. The checksum is computed using the CRC-16 CCITT polynomial, as shown in Figure 29. The checksum consists of the 11 most significant bits of the 16-bit code. A change in the checksum indicates a change in the Readback bitstream. A comparison to a previous checksum is meaningful only if the readback data is independent of the current device state. CLB outputs should not be included (Readback Capture option not used), and if RAM is present, the RAM content must be unchanged.

Statistically, one error out of 2048 might go undetected.

Configuration Sequence

There are four major steps in the Spartan/XL power-up configuration sequence.

- Configuration Memory Clear
- Initialization
- Configuration
- Start-up

The full process is illustrated in Figure 30.

Configuration Memory Clear

When power is first applied or is reapplied to an FPGA, an internal circuit forces initialization of the configuration logic.

When V_{CC} reaches an operational level, and the circuit passes the write and read test of a sample pair of configuration bits, a time delay is started. This time delay is nominally 16 ms. The delay is four times as long when in Master Serial Mode to allow ample time for all slaves to reach a stable V_{CC}. When all $\overline{INIT}$ pins are tied together, as recommended, the longest delay takes precedence. Therefore, devices with different time delays can easily be mixed and matched in a daisy chain.

This delay is applied only on power-up. It is not applied when reconfiguring an FPGA by pulsing the $\overline{PROGRAM}$ pin

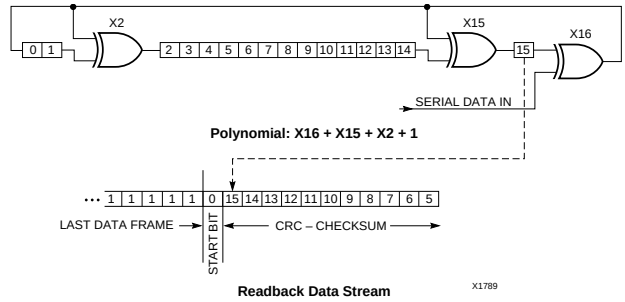


Figure 29: Circuit for Generating CRC-16

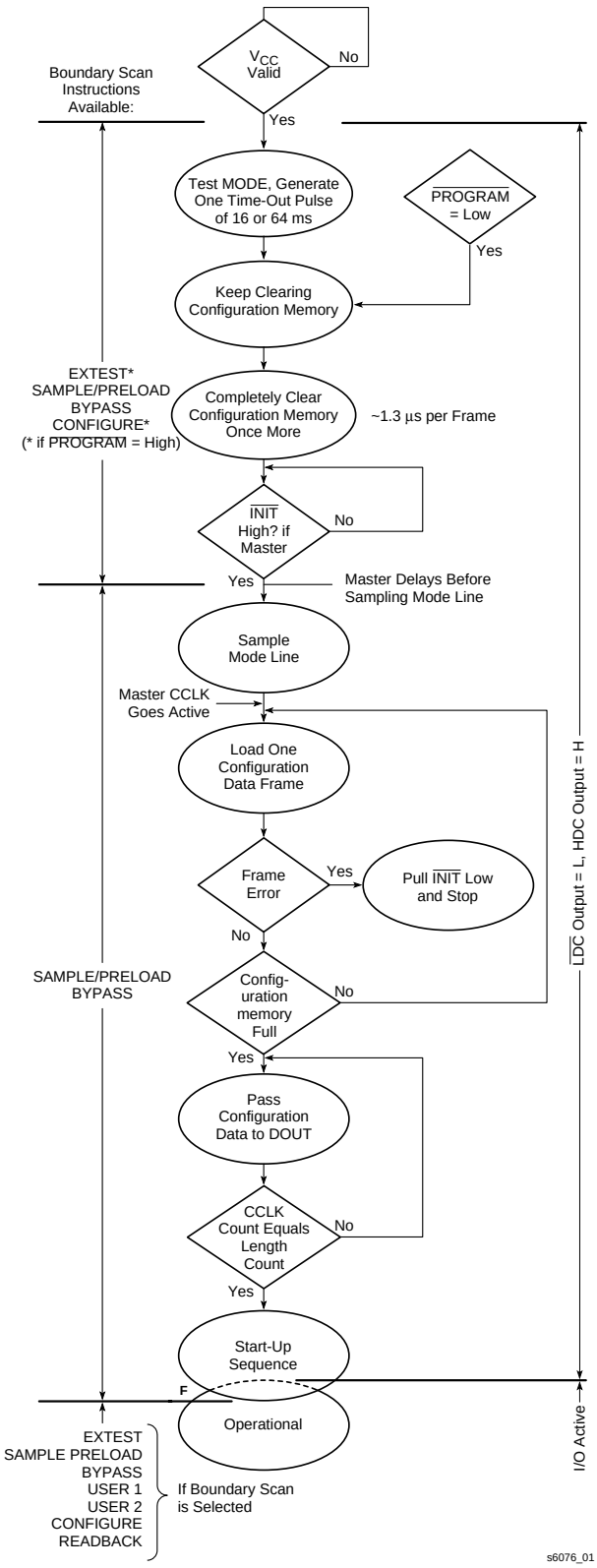


Figure 30: Power-up Configuration Sequence

Low. During this time delay, or as long as the PROGRAM input is asserted, the configuration logic is held in a Configuration Memory Clear state. The configuration-memory frames are consecutively initialized, using the internal oscillator.

At the end of each complete pass through the frame addressing, the power-on time-out delay circuitry and the level of the PROGRAM pin are tested. If neither is asserted, the logic initiates one additional clearing of the configuration frames and then tests the INIT input.

Initialization

During initialization and configuration, user pins HDC, LDC, INIT and DONE provide status outputs for the system interface. The outputs LDC, INIT and DONE are held Low and HDC is held High starting at the initial application of power.

The open drain INIT pin is released after the final initialization pass through the frame addresses. There is a deliberate delay before a Master-mode device recognizes an inactive INIT. Two internal clocks after the INIT pin is recognized as High, the device samples the MODE pin to determine the configuration mode. The appropriate interface lines become active and the configuration preamble and data can be loaded.

Configuration

The 0010 preamble code indicates that the following 24 bits represent the length count for serial modes. The length count is the total number of configuration clocks needed to load the complete configuration data. (Four additional configuration clocks are required to complete the configuration process, as discussed below.) After the preamble and the length count have been passed through to any device in the daisy chain, its DOUT is held High to prevent frame start bits from reaching any daisy-chained devices. In Spartan-XL Express mode, the length count bits are ignored, and DOUT is held Low, to disable the next device in the pseudo daisy chain.

A specific configuration bit, early in the first frame of a master device, controls the configuration-clock rate and can increase it by a factor of eight. Therefore, if a fast configuration clock is selected by the bitstream, the slower clock rate is used until this configuration bit is detected.

Each frame has a start field followed by the frame-configuration data bits and a frame error field. If a frame data error is detected, the FPGA halts loading, and signals the error by pulling the open-drain INIT pin Low. After all configuration frames have been loaded into an FPGA using a serial mode, DOUT again follows the input data so that the remaining data is passed on to the next device. In Spartan-XL Express mode, when the first device is fully programmed, DOUT goes High to enable the next device in the chain.

Delaying Configuration After Power-Up

There are two methods of delaying configuration after power-up: put a logic Low on the PROGRAM input, or pull the bidirectional INIT pin Low, using an open-collector (open-drain) driver. (See Figure 30 on page 90.)

A Low on the PROGRAM input is the more radical approach, and is recommended when the power-supply rise time is excessive or poorly defined. As long as PROGRAM is Low, the FPGA keeps clearing its configuration memory. When PROGRAM goes High, the configuration memory is cleared one more time, followed by the beginning of configuration, provided the INIT input is not externally held Low. Note that a Low on the PROGRAM input automatically forces a Low on the INIT output. The Spartan/XL PROGRAM pin has a permanent weak pull-up. Avoid holding PROGRAM Low for more than 500 µs.

Using an open-collector or open-drain driver to hold INIT Low before the beginning of configuration causes the FPGA to wait after completing the configuration memory clear operation. When INIT is no longer held Low externally, the device determines its configuration mode by capturing the state of the Mode pins, and is ready to start the configuration process. A master device waits up to an additional 300 µs to make sure that any slaves in the optional daisy chain have seen that INIT is High.

Configuration Through the Boundary Scan Pins

Spartan/XL devices can be configured through the boundary scan pins. The basic procedure is as follows:

- Power up the FPGA with INIT held Low (or drive the PROGRAM pin Low for more than 300 ns followed by a High while holding INIT Low). Holding INIT Low allows enough time to issue the CONFIG command to the FPGA. The pin can be used as I/O after configuration if a resistor is used to hold INIT Low.
- Issue the CONFIG command to the TMS input
- Wait for INIT to go High
- Sequence the boundary scan Test Access Port to the SHIFT-DR state
- Toggle TCK to clock data into TDI pin.

The user must account for all TCK clock cycles after INIT goes High, as all of these cycles affect the Length Count compare.

For more detailed information, refer to the Xilinx application note, "*Boundary Scan in FPGA Devices*." This application note applies to Spartan and Spartan-XL devices.

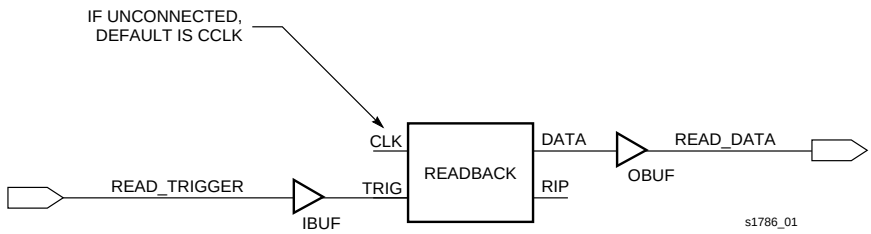


Figure 31: Readback Schematic Example

Readback

The user can read back the content of configuration memory and the level of certain internal nodes without interfering with the normal operation of the device.

Readback not only reports the downloaded configuration bits, but can also include the present state of the device, represented by the content of all flip-flops and latches in CLBs and IOBs, as well as the content of function generators used as RAMs.

Readback of Spartan-XL Express mode bitstreams results in data that does not resemble the original bitstream, because the bitstream format differs from other modes.

Spartan/XL Readback does not use any dedicated pins, but uses four internal nets (RDBK.TRIG, RDBK.DATA, RDBK.RIP and RDBK.CLK) that can be routed to any IOB. To access the internal Readback signals, instantiate the READBACK library symbol and attach the appropriate pad symbols, as shown in Figure 31.

After Readback has been initiated by a Low-to-High transition on RDBK.TRIG, the RDBK.RIP (Read In Progress) output goes High on the next rising edge of RDBK.CLK. Subsequent rising edges of this clock shift out Readback data on the RDBK.DATA net.

Readback data does not include the preamble, but starts with five dummy bits (all High) followed by the Start bit (Low) of the first frame. The first two data bits of the first frame are always High.

Each frame ends with four error check bits. They are read back as High. The last seven bits of the last frame are also read back as High. An additional Start bit (Low) and an 11-bit Cyclic Redundancy Check (CRC) signature follow, before RDBK.RIP returns Low.

Readback Options

Readback options are: Readback Capture, Readback Abort, and Clock Select. They are set with the bitstream generation software.

Readback Capture

When the Readback Capture option is selected, the \ data stream includes sampled values of CLB and IOB signals. The rising edge of RDBK.TRIG latches the inverted values of the four CLB outputs, the IOB output flip-flops and the input signals I1 and I2. Note that while the bits describing configuration (interconnect, function generators, and RAM content) are *not* inverted, the CLB and IOB output signals *are* inverted. RDBK.TRIG is located in the lower-left corner of the device.

When the Readback Capture option is not selected, the values of the capture bits reflect the configuration data originally written to those memory locations. If the RAM capability of the CLBs is used, RAM data are available in Readback, since they directly overwrite the F and G function-table configuration of the CLB.

Readback Abort

When the Readback Abort option is selected, a High-to-Low transition on RDBK.TRIG terminates the Readback operation and prepares the logic to accept another trigger.

After an aborted Readback, additional clocks (up to one Readback clock per configuration frame) may be required to re-initialize the control logic. The status of Readback is indicated by the output control net RDBK.RIP. RDBK.RIP is High whenever a readback is in progress.

Clock Select

CCLK is the default clock. However, the user can insert another clock on RDBK.CLK. Readback control and data are clocked on rising edges of RDBK.CLK. If Readback must be inhibited for security reasons, the Readback control nets are simply not connected. RDBK.CLK is located in the lower right chip corner.

Violating the Maximum High and Low Time Specification for the Readback Clock

The Readback clock has a maximum High and Low time specification. In some cases, this specification cannot be met. For example, if a processor is controlling Readback, an interrupt may force it to stop in the middle of a readback. This necessitates stopping the clock, and thus violating the specification.

The specification is mandatory only on clocking data at the end of a frame prior to the next start bit. The transfer mechanism will load the data to a shift register during the last six clock cycles of the frame, prior to the start bit of the following frame. This loading process is dynamic, and is the source of the maximum High and Low time requirements.

Therefore, the specification only applies to the six clock cycles prior to and including any start bit, including the clocks before the first start bit in the Readback data stream. At other times, the frame data is already in the register and the register is not dynamic. Thus, it can be shifted out just like a regular shift register.

The user must precisely calculate the location of the Readback data relative to the frame. The system must keep track of the position within a data frame, and disable interrupts before frame boundaries. Frame lengths and data formats are listed in Table 53 and Table 54.

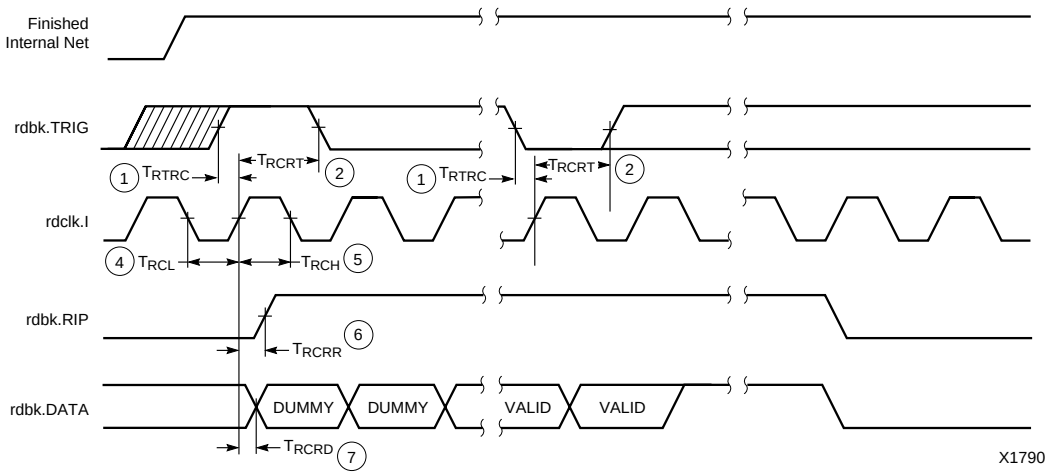
Readback with the XChecker Cable

The XChecker Universal Download/Readback Cable and Logic Probe uses the readback feature for bitstream verification. It can also display selected internal signals on the computer screen, acting as a low-cost in-circuit emulator.

Readback Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are not measured directly. They are derived from benchmark timing patterns that are taken at device introduction, prior to any process improvements.

The following guidelines reflect worst-case values over the recommended operating conditions.

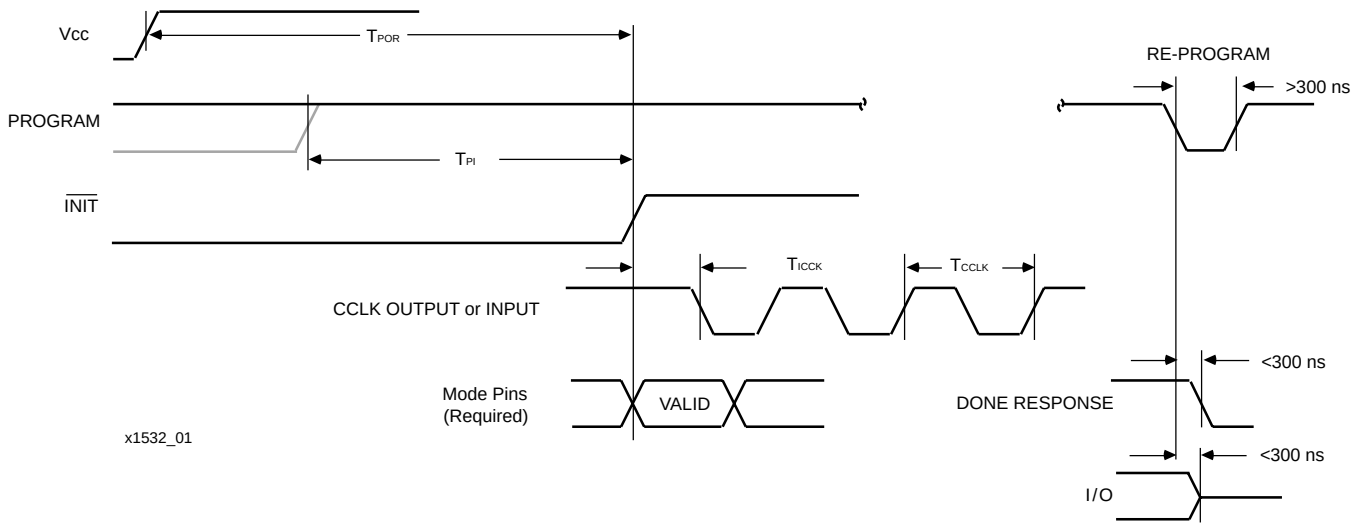


Spartan and Spartan-XL Readback

	Description	Symbol		Min	Max	Units
rdbk.TRIG	rdbk.TRIG setup to initiate and abort Readback	1	T_{RTRC}	200	-	ns
	rdbk.TRIG hold to initiate and abort Readback	2	T_{RCRT}	50	-	ns
rdclk.1	rdbk.DATA delay	7	T_{RCRD}	-	250	ns
	rdbk.RIP delay	6	T_{RCRR}	-	250	ns
	High time	5	T_{RCH}	250	500	ns
	Low time	4	T_{RCL}	250	500	ns

Note 1: Timing parameters apply to all speed grades.
Note 2: If rdbk.TRIG is High prior to Finished, Finished will trigger the first Readback.

Configuration Switching Characteristics



Master Mode

Description	Symbol	Min	Max	Units
Power-on Reset	T_{POR}	40	130	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (output) Delay	T_{ICCK}	40	250	µs
CCLK (output) Period, slow	T_{CCLK}	640	2000	ns
CCLK (output) Period, fast	T_{CCLK}	80	250	ns

Slave Mode

Description	Symbol	Min	Max	Units
Power-on Reset	T_{POR}	10	33	ms
Program Latency	T_{PI}	30	200	µs per CLB column
CCLK (input) Delay (required)	T_{ICCK}	4		µs
CCLK (input) Period (required)	T_{CCLK}	80		ns

Spartan Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan Absolute Maximum Ratings[1]

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 2, 3)		–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 2, 3)		–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2: Maximum DC overshoot (above V_{CC}) or undershoot (below GND) must be limited to either 0.5V or 10 mA, whichever is easier to achieve.
3: Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0V or overshoot to + 7.0V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

Spartan Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	4.75	5.25	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Note 1: At junction temperatures above those listed as Recommended Operating Conditions, all delay parameters increase by 0.35% per °C.
Note 2: Input and output measurement thresholds are: 1.5V for TTL and 2.5V for CMOS.

Spartan DC Characteristics Over Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ I_{OH} = –1.0 mA, V_{CC} min	CMOS outputs	V_{CC} – 0.5		V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
I_{CCO}	Quiescent FPGA supply current (Note 2)	Commercial		3.0	mA
		Industrial		6.0	mA
I_L	Input or output leakage current		–10	+10	µA
C_{IN}	Input capacitance (sample tested)			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 5V (sample tested)		0.02		mA

Note 1: With 50% of the outputs simultaneously sinking 12 mA, up to a maximum of 64 pins.
Note 2: With no output current loads, no active input pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a Tie option.

Spartan Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-4	-3	Units
Description	Symbol	Device	Max	Max	
From pad through Primary buffer, to any clock K	T_{PG}	XCS05	2.0	4.0	ns
		XCS10	2.4	4.3	ns
		XCS20	2.8	5.4	ns
		XCS30	3.2	5.8	ns
		XCS40	3.5	6.4	ns
From pad through Secondary buffer, to any clock K	T_{SG}	XCS05	2.5	4.4	ns
		XCS10	2.9	4.7	ns
		XCS20	3.3	5.8	ns
		XCS30	3.6	6.2	ns
		XCS40	3.9	6.7	ns

Spartan CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and expressed in nanoseconds unless otherwise noted.

Speed Grade		-4		-3		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Clocks						
Clock High time	T_{CH}	3.0		4.0		ns
Clock Low time	T_{CL}	3.0		4.0		ns
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		1.2		1.6	ns
F/G inputs via H to X/Y outputs	T_{IHO}		2.0		2.7	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.7		2.2	ns
CLB Fast Carry Logic						
Operand inputs (F1, F2, G1, G4) to C_{OUT}	T_{OPCY}		1.7		2.1	ns
Add/Subtract input (F3) to C_{OUT}	T_{ASCY}		2.8		3.7	ns
Initialization inputs (F1, F3) to C_{OUT}	T_{INCY}		1.2		1.4	ns
C_{IN} through function generators to X/Y outputs	T_{SUM}		2.0		2.6	ns
C_{IN} to C_{OUT}, bypass function generators	T_{BYP}		0.5		0.6	ns
Sequential Delays						
Clock K to Flip-Flop outputs Q	T_{CKO}		2.1		2.8	ns
Setup Time before Clock K						
F/G inputs	T_{ICK}	1.8		2.4		ns
F/G inputs via H	T_{IHCK}	2.9		3.9		ns
C inputs via H1 through H	T_{HH1CK}	2.3		3.3		ns
C inputs via DIN	T_{DICK}	1.3		2.0		ns
C inputs via EC	T_{ECCK}	2.0		2.6		ns
C inputs via S/R, going Low (inactive)	T_{RCK}	2.5		4.0		ns
Hold Time after Clock K						
All Hold times, all devices		0.0		0.0		ns
Set/Reset Direct						
Width (High)	T_{RPW}	3.0		4.0		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		3.0		4.0	ns
Global Set/Reset						
Minimum GSR pulse width	T_{MRW}	11.5		13.5		ns
Delay from GSR input to any Q	T_{MRQ}	See page 102 for T_{RRI} values per device.				
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		166		125	MHz

Spartan CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-4		-3		Units
	Size	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	8.0 8.0		11.6 11.6		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	4.0 4.0		5.8 5.8		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	1.5 1.5		2.0 2.0		ns ns
Address hold time after clock K	16x2 32x1	T_{AHS} T_{AHTS}	0.0 0.0		0.0 0.0		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	1.5 1.5		2.7 1.7		ns ns
DIN hold time after clock K	16x2 32x1	T_{DHS} T_{DHTS}	0.0 0.0		0.0 0.0		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	1.5 1.5		1.6 1.6		ns ns
WE hold time after clock K	16x2 32x1	T_{WHS} T_{WHTS}	0.0 0.0		0.0 0.0		ns ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		6.5 7.0		7.9 9.3	ns ns
Read Operation							
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	2.6 3.8		2.6 3.8		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.2 2.0		1.6 2.7	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	1.8 2.9		2.4 3.9		ns ns

Note: Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

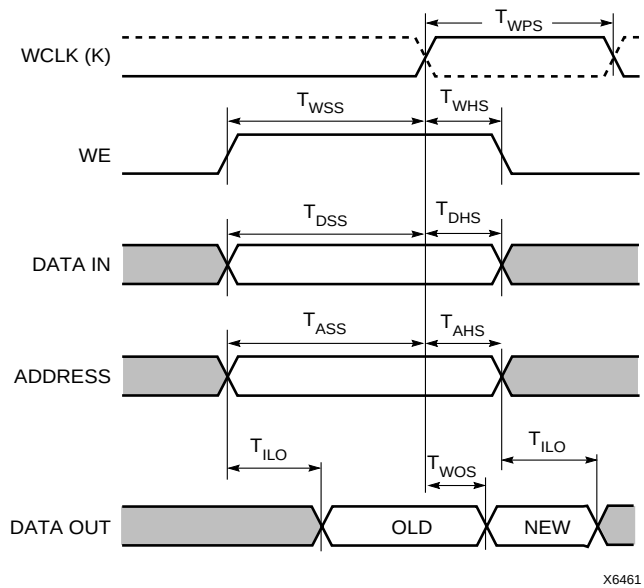
Spartan CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan devices and are expressed in nanoseconds unless otherwise noted.

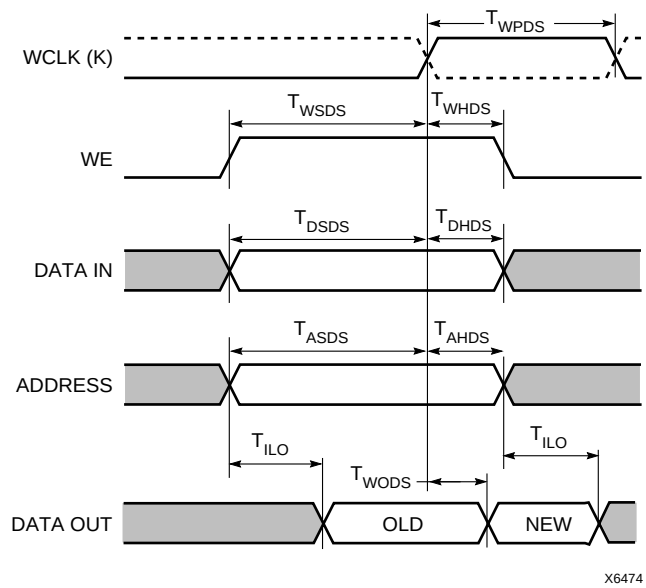
Dual Port RAM	Speed Grade		-4		-3		Units
	Size	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x1	T_{WCDS}	8.0		11.6		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.0		5.8		ns
Address setup time before clock K	16x1	T_{ASDS}	1.5		2.1		ns
Address hold time after clock K	16x1	T_{AHDS}	0.0		0.0		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.5		1.6		ns
DIN hold time after clock K	16x1	T_{DHDS}	0.0		0.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.5		1.6		ns
WE hold time after clock K	16x1	T_{WHDS}	0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		6.5		7.0	ns

Note 1: Read Operation timing for 16 x 1 dual-port RAM option is identical to 16 x 2 single-port RAM timing.

Spartan CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port



Dual Port

Spartan Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report.

Spartan Output Flip-Flop, Clock-to-Out

		Speed Grade	-4	-3	Units
Description	**Symbol**	**Device**	**Max**	**Max**	
Global Primary Clock to TTL Output using OFF					
Fast	T_{ICKOF}	XCS05	5.3	8.7	ns
		XCS10	5.7	9.1	ns
		XCS20	6.1	9.3	ns
		XCS30	6.5	9.4	ns
		XCS40	6.8	10.2	ns
Slew-rate limited	T_{ICKO}	XCS05	9.0	11.5	ns
		XCS10	9.4	12.0	ns
		XCS20	9.8	12.2	ns
		XCS30	10.2	12.8	ns
		XCS40	10.5	12.8	ns
Global Secondary Clock to TTL Output using OFF					
Fast	T_{ICKSOF}	XCS05	5.8	9.2	ns
		XCS10	6.2	9.6	ns
		XCS20	6.6	9.8	ns
		XCS30	7.0	9.9	ns
		XCS40	7.3	10.7	ns
Slew-rate limited	T_{ICKSO}	XCS05	9.5	12.0	ns
		XCS10	9.9	12.5	ns
		XCS20	10.3	12.7	ns
		XCS30	10.7	13.2	ns
		XCS40	11.0	14.3	ns
Delay Adder for CMOS Outputs Option					
Fast	T_{CMOSOF}	All devices	0.8	1.0	ns
Slew-rate Limited	T_{CMOSO}	All devices	1.5	2.0	ns

OFF = Output Flip-Flop

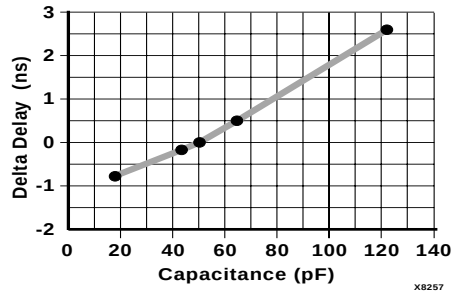
Note 1: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Note 2: Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load. For different loads, see Figure 32.

Capacitive Load Factor

Figure 32 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 32 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

Figure 32: Delay Factor at Various Capacitive Loads



Spartan Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan Primary and Secondary Setup and Hold

		Speed Grade	-4	-3	Units
Description	**Symbol**	**Device**	**Min**	**Min**	
Input Setup/Hold Times Using Primary Clock and IFF					
No Delay	T_{PSUF}/T_{PHF}	XCS05	1.2 / 1.7	1.8 / 2.5	ns
		XCS10	1.0 / 2.3	1.5 / 3.4	ns
		XCS20	0.8 / 2.7	1.2 / 4.0	ns
		XCS30	0.6 / 3.0	0.9 / 4.5	ns
		XCS40	0.4 / 3.5	0.6 / 5.2	ns
With Delay	T_{PSU}/T_{PH}	XCS05	4.3 / 0.0	6.0 / 0.0	ns
		XCS10	4.3 / 0.0	6.0 / 0.0	ns
		XCS20	4.3 / 0.0	6.0 / 0.0	ns
		XCS30	4.3 / 0.0	6.0 / 0.0	ns
		XCS40	5.3 / 0.0	6.8 / 0.0	ns
Input Setup/Hold Times Using Secondary Clock and IFF					
No Delay	T_{SSUF}/T_{SHF}	XCS05	0.9 / 2.2	1.5 / 3.0	ns
		XCS10	0.7 / 2.8	1.2 / 3.9	ns
		XCS20	0.5 / 3.2	0.9 / 4.5	ns
		XCS30	0.3 / 3.5	0.6 / 5.0	ns
		XCS40	0.1 / 4.0	0.3 / 5.7	ns
With Delay	T_{SSU}/T_{SH}	XCS05	4.0 / 0.0	5.7 / 0.0	ns
		XCS10	4.0 / 0.0	5.7 / 0.0	ns
		XCS20	4.0 / 0.5	5.7 / 0.5	ns
		XCS30	4.0 / 0.5	5.7 / 0.5	ns
		XCS40	5.0 / 0.0	6.5 / 0.0	ns

IFF = Input Flip-flop or Latch

Note 1: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Spartan IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-4		-3		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Setup Times - TTL Inputs (Note 1)							
Clock Enable (EC) to Clock (IK), no delay	T_{ECIK}	All devices	1.6		2.1		ns
Pad to Clock (IK), no delay	T_{PICK}	All devices	1.5		2.0		ns
Hold Times							
Clock Enable (EC) to Clock (IK), no delay	T_{IKEC}	All devices	0.0		0.9		ns
All Other Hold Times		All devices	0.0		0.0		ns
Propagation Delays - TTL Inputs (Note 1)							
Pad to I1, I2	T_{PID}	All devices		1.5		2.0	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.8		3.6	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		2.7		2.8	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		3.2		3.9	ns
Delay Adder for Input with Delay Option							
$T_{ECIKD} = T_{ECIK} + T_{Delay}$	T_{Delay}	XCS05	3.6		4.0		ns
$T_{PICKD} = T_{PICK} + T_{Delay}$		XCS10	3.7		4.1		ns
$T_{PDLI} = T_{PLI} + T_{Delay}$		XCS20	3.8		4.2		ns
		XCS30	4.5		5.0		ns
		XCS40	5.5		5.5		ns
Global Set/Reset							
Minimum GSR pulse width	T_{MRW}	All devices	11.5		13.5		ns
Delay from GSR input to any Q	T_{RRI}	XCS05		9.0		11.3	ns
		XCS10		9.5		11.9	ns
		XCS20		10.0		12.5	ns
		XCS30		10.5		13.1	ns
		XCS40		11.0		13.8	ns

Note 1: Delay adder for CMOS Inputs option: for -3 speed grade, add 0.4 ns; for -4 speed grade, add 0.2 ns.
Note 2: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.
Note 3: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-4		-3		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Clocks							
Clock High	T_{CH}	All devices	3.0		4.0		ns
Clock Low	T_{CL}	All devices	3.0		4.0		ns
Propagation Delays - TTL Outputs (Notes 1, 2)							
Clock (OK) to Pad, fast	T_{OKPOF}	All devices		3.3		4.5	ns
Clock (OK to Pad, slew-rate limited	T_{OKPOS}	All devices		6.9		7.0	ns
Output (O) to Pad, fast	T_{OPF}	All devices		3.6		4.8	ns
Output (O) to Pad, slew-rate limited	T_{OPS}	All devices		7.2		7.3	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}	All devices		3.0		3.8	ns
3-state to Pad active and valid, fast	T_{TSONF}	All devices		6.0		7.3	ns
3-state to Pad active and valid, slew-rate limited	T_{TSONS}	All devices		9.6		9.8	ns
Setup and Hold Times							
Output (O) to clock (OK) setup time	T_{OOK}	All devices	2.5		3.8		ns
Output (O) to clock (OK) hold time	T_{OKO}	All devices	0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	All devices	2.0		2.7		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	All devices	0.0		0.5		ns
Global Set/Reset							
Minimum GSR pulse width	T_{MRW}	All devices	11.5		13.5		ns
Delay from GSR input to any Pad	T_{RPO}	XCS05		12.0		15.0	ns
		XCS10		12.5		15.7	ns
		XCS20		13.0		16.2	ns
		XCS30		13.5		16.9	ns
		XCS40		14.0		17.5	ns

Note 1: Delay adder for CMOS Outputs option (with fast slew rate option): for -3 speed grade, add 1.0 ns; for -4 speed grade, add 0.8 ns.
Note 2: Delay adder for CMOS Outputs option (with slow slew rate option): for -3 speed grade, add 2.0 ns; for -4 speed grade, add 1.5 ns.
Note 3: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
Note 4: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL Detailed Specifications

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.
Preliminary: Based on preliminary characterization. Further changes are not expected.
Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

Notwithstanding the definition of the above terms, all specifications are subject to change without notice.

Except for pin-to-pin input and output parameters, the AC parameter delay specifications included in this document are derived from measuring internal test patterns. All specifications are representative of worst-case supply voltage and junction temperature conditions. The parameters included are common to popular designs and typical applications.

Spartan-XL Absolute Maximum Ratings[1]

Symbol	Description		Value	Units
V_{CC}	Supply voltage relative to GND		–0.5 to 4.0	V
V_{IN}	Input voltage relative to GND (Note 2, 3, 4, 5)	5V Tolerant I/O Checked[2, 3]	–0.5 to 5.5	V
		Not 5V Tolerant I/Os[4, 5]	–0.5 to V_{CC} + 0.5	V
V_{TS}	Voltage applied to 3-state output (Note 2, 3, 4, 5)	5V Tolerant I/O Checked[2, 3]	–0.5 to 5.5	V
		Not 5V Tolerant I/Os[4, 5]	–0.5 to V_{CC} + 0.5	V
V_{CCt}	Longest supply voltage rise time from 1V to 3V		50	ms
T_{STG}	Storage temperature (ambient)		–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260	°C
T_J	Junction temperature	Plastic packages	+125	°C

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.
2: With 5V Tolerant I/Os selected, the Maximum DC overshoot must be limited to either +5.5 V or 10 mA and undershoot (below GND) must be limited to either 0.5 V or 10 mA, whichever is easier to achieve.
3: With 5V Tolerant I/Os selected, the Maximum AC (during transitions) conditions are as follows; the device pins may undershoot to –2.0 V or overshoot to + 7.0 V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.
4: Without 5V Tolerant I/Os selected, the Maximum DC overshoot or undershoot must be limited to either 0.5 V or 10 mA, whichever is easier to achieve.
5: Without 5V Tolerant I/Os selected, the Maximum AC conditions are as follows; the device pins may undershoot to –2.0 V or overshoot to V_{CC} + 2.0 V, provided this overshoot or undershoot lasts no more than 11 ns with a forcing current no greater than 100 mA.

Spartan-XL Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, T_J = 0°C to +85°C	Commercial	3.0	3.6	V
	Supply voltage relative to GND, T_J = –40°C to +100°C	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30% of V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C.
Input and output measurement threshold is ~50% of V_{CC}.

Spartan-XL DC Characteristics Over Operating Conditions

Symbol	Description	Min	Typ.	Max	Units
V_{OH}	High-level output voltage @ I_{OH} = –4.0 mA, V_{CC} min (LVTTL)	2.4			V
	High-level output voltage @ I_{OH} = –500 µA, (LVCMOS)	90% V_{CC}			V
V_{OL}	Low-level output voltage @ I_{OL} = 12.0 mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ I_{OL} = 24.0 mA, V_{CC} min (LVTTL) (Note 2)			0.4	V
	Low-level output voltage @ I_{OL} = 1500 µA, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data retention supply voltage (below which configuration data may be lost)	2.5			V
I_{CCO}	Quiescent FPGA supply current (Notes 3,4)		100	5	mA
I_{CCPD}	Power Down FPGA supply current (Notes 3,5)		100	5	mA
I_L	Input or output leakage current	–10		+10	µA
C_{IN}	Input capacitance (sample tested)			10	pF
I_{RPU}	Pad pull-up (when selected) @ V_{IN} = 0V (sample tested)	0.02		0.25	mA
I_{RPD}	Pad pull-down (when selected) @ V_{IN} = 3.3V (sample tested)	0.02			mA

Note 1: With up to 64 pins simultaneously sinking 12 mA (default mode).
Note 2: With up to 64 pins simultaneously sinking 24 mA (with 24 mA option selected).
Note 3: With 5V tolerance not selected, no internal oscillators, and the FPGA configured with the Tie option.
Note 4: With no output current loads, no active input resistors, and all package pins at V_{CC} or GND.
Note 5: With $\overline{PWRDWN}$ active.

Power-on Power Supply Requirements

Xilinx FPGAs require a certain amount of supply current during power-on to insure proper device operation. The actual current consumed depends on the power-on ramp rate of the power supply. This is the time required to reach the required power supply voltage of the device from 0V. The current is highest at the fastest suggested ramp rate (2 ms) and is lowest at the slowest allowed ramp rate (50 ms).

Product	Description	Ramp-up Time	
		Fast (2 ms)	Slow (50 ms)
Spartan-XL Family	Minimum required current supply	100 mA	100 mA

Note 1: Devices are guaranteed to initialize properly with the minimum current listed above. A larger capacity power supply may result in larger initialization current.
Note 2: This specification applies to Commercial and Industrial grade products only. Advance information based on initial characterization.
Note 3: Ramp-up Time is measured at 0V to 3.0V. Peak current required lasts less than 3 ms and occurs near the internal power-on reset threshold voltage.

Spartan-XL Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-5	-4	Units
Description	**Symbol**	**Device**	**Max**	**Max**	
From pad through buffer, to any clock K	T_{GLS}	XCS05XL	1.4	1.5	ns
		XCS10XL	1.7	1.8	ns
		XCS20XL	2.0	2.1	ns
		XCS30XL	2.3	2.5	ns
		XCS40XL	2.6	2.8	ns

Spartan-XL CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and expressed in nanoseconds unless otherwise noted.

Speed Grade		-5		-4		Units
Description	**Symbol**	**Min**	**Max**	**Min**	**Max**	
Clocks						
Clock High time	T_{CH}	2.0		2.3		ns
Clock Low time	T_{CL}	2.0		2.3		ns
Combinatorial Delays						
F/G inputs to X/Y outputs	T_{ILO}		1.0		1.1	ns
F/G inputs via H to X/Y outputs	T_{IHO}		1.7		2.0	ns
F/G inputs via transparent latch to Q outputs	T_{ITO}		1.5		1.8	ns
C inputs via H1 via H to X/Y outputs	T_{HH1O}		1.5		1.8	ns
Sequential Delays						
Clock K to Flip-Flop or latch outputs Q	T_{CKO}		1.2		1.4	ns
Setup Time before Clock K						
F/G inputs	T_{ICK}	0.6		0.7		ns
F/G inputs via H	T_{IHCK}	1.3		1.6		ns
Hold Time after Clock K						
All Hold times, all devices		0.0		0.0		ns
Set/Reset Direct						
Width (High)	T_{RPW}	2.5		2.8		ns
Delay from C inputs via S/R, going High to Q	T_{RIO}		2.3		2.7	ns
Global Set/Reset						
Minimum GSR Pulse Width	T_{MRW}	10.5		11.5		ns
Delay from GSR input to any Q	T_{MRQ}	See page 111 for T_{RRI} values per device.				
Toggle Frequency (MHz) (for export control purposes)	F_{TOG}		250		217	MHz

Spartan-XL CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

Single Port RAM	Speed Grade		-5		-4		Units
	Size[1]	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x2 32x1	T_{WCS} T_{WCTS}	7.7 7.7		8.4 8.4		ns ns
Clock K pulse width (active edge)	16x2 32x1	T_{WPS} T_{WPTS}	3.1 3.1		3.6 3.6		ns ns
Address setup time before clock K	16x2 32x1	T_{ASS} T_{ASTS}	1.3 1.5		1.5 1.7		ns ns
DIN setup time before clock K	16x2 32x1	T_{DSS} T_{DSTS}	1.5 1.8		1.7 2.1		ns ns
WE setup time before clock K	16x2 32x1	T_{WSS} T_{WSTS}	1.4 1.3		1.6 1.5		ns ns
All hold times after clock K			0.0		0.0		ns
Data valid after clock K	16x2 32x1	T_{WOS} T_{WOTS}		4.5 5.4		5.3 6.3	ns ns
Read Operation							
Address read cycle time	16x2 32x1	T_{RC} T_{RCT}	2.6 3.8		3.1 5.5		ns ns
Data Valid after address change (no Write Enable)	16x2 32x1	T_{ILO} T_{IHO}		1.0 1.7		1.1 2.0	ns ns
Address setup time before clock K	16x2 32x1	T_{ICK} T_{IHCK}	0.6 1.3		0.7 1.6		ns ns

Note 1: Timing for 16 x 1 RAM option is identical to 16 x 2 RAM timing.

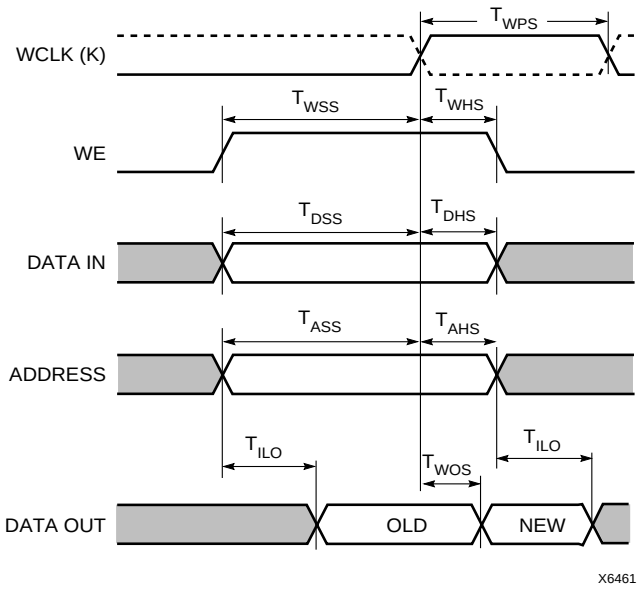
Spartan-XL CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines (cont.)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all Spartan-XL devices and are expressed in nanoseconds unless otherwise noted.

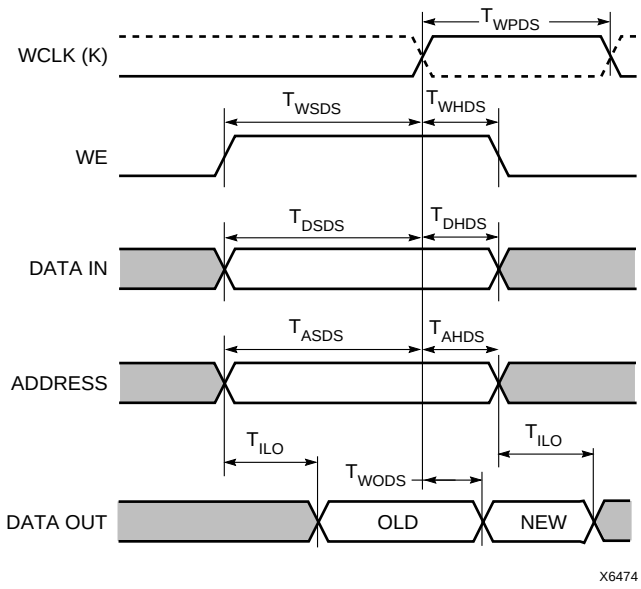
Dual Port RAM	Speed Grade		-5		-4		Units
	Size[1]	Symbol	Min	Max	Min	Max	
Write Operation							
Address write cycle time (clock K period)	16x1	T_{WCDS}	7.7		8.4		ns
Clock K pulse width (active edge)	16x1	T_{WPDS}	3.1		3.6		ns
Address setup time before clock K	16x1	T_{ASDS}	1.3		1.5		ns
DIN setup time before clock K	16x1	T_{DSDS}	1.7		2.0		ns
WE setup time before clock K	16x1	T_{WSDS}	1.4		1.6		ns
All hold times after clock K	16x1		0.0		0.0		ns
Data valid after clock K	16x1	T_{WODS}		5.2		6.1	ns

Note 1: Read Operation Timing for 16x1 dual-port RAM option is identical to 16x2 single-port RAM timing.

Spartan-XL CLB RAM Synchronous (Edge-Triggered) Write Timing



Single Port



Dual Port

Spartan-XL Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Output Flip-Flop, Clock-to-Out

		Speed Grade	-5	-4	Units
Description	**Symbol**	**Device**	**Max**	**Max**	
Global Clock to Output using OFF					
Fast	T_{ICKOF}	XCS05XL	4.6	5.2	ns
		XCS10XL	4.9	5.5	ns
		XCS20XL	5.2	5.8	ns
		XCS30XL	5.5	6.2	ns
		XCS40XL	5.8	6.5	ns
Slew Rate Adjustment					
For Output SLOW option add	T_{SLOW}	All Devices	1.5	1.7	ns

OFF = Output Flip Flop

Note 1: Output delays are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.
Note 2: Output timing is measured at ~50% V_{CC} threshold with 50 pF external capacitive load.

Spartan-XL Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading.

Spartan-XL Setup and Hold

		Speed Grade	-5	-4	Units
Description	**Symbol**	**Device**	**Min**	**Min**	
Input Setup/Hold Times Using Global Clock and IFF					
No Delay	T_{SUF}/T_{HF}	XCS05XL	1.1/2.0	1.6/2.6	ns
		XCS10XL	1.0/2.2	1.5/2.8	ns
		XCS20XL	0.9/2.4	1.4/3.0	ns
		XCS30XL	0.8/2.6	1.3/3.2	ns
		XCS40XL	0.7/2.8	1.2/3.4	ns
Full Delay	T_{SU}/T_{H}	XCS05XL	3.9/0.0	5.1/0.0	ns
		XCS10XL	4.1/0.0	5.3/0.0	ns
		XCS20XL	4.3/0.0	5.5/0.0	ns
		XCS30XL	4.5/0.0	5.7/0.0	ns
		XCS40XL	4.7/0.0	5.9/0.0	ns

IFF = Input Flip-Flop or Latch

Note 3: Setup time is measured with the fastest route and the lightest load. Hold time is measured using the furthest distance and a reference load of one clock pin per IOB/CLB.

Capacitive Load Factor

Figure 33 shows the relationship between I/O output delay and load capacitance. It allows a user to adjust the specified output delay if the load capacitance is different than 50 pF. For example, if the actual load capacitance is 120 pF, add 2.5 ns to the specified delay. If the load capacitance is 20 pF, subtract 0.8 ns from the specified output delay. Figure 33 is usable over the specified operating conditions of voltage and temperature and is independent of the output slew rate control.

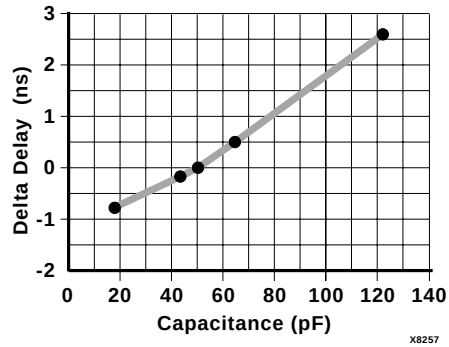


Figure 33: Delay Factor at Various Capacitive Loads

Spartan-XL IOB Input Switching Characteristic Guidelines

4

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

		Speed Grade	-5		-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Setup Times							
Clock Enable (EC) to Clock (IK)	T_{ECIK}	All devices	0.0		0.0		ns
Pad to Clock (IK), no delay	T_{PICK}	All devices	1.0		1.2		ns
Pad to Fast Capture Latch Enable (OK), no delay	T_{POCK}	All devices	0.7		0.8		ns
Hold Times							
All Hold Times		All devices	0.0		0.0		ns
Propagation Delays							
Pad to I1, I2	T_{PID}	All devices		0.9		1.1	ns
Pad to I1, I2 via transparent input latch, no delay	T_{PLI}	All devices		2.1		2.5	ns
Clock (IK) to I1, I2 (flip-flop)	T_{IKRI}	All devices		1.0		1.1	ns
Clock (IK) to I1, I2 (latch enable, active Low)	T_{IKLI}	All devices		1.1		1.2	ns
Delay Adder for Input with Full Delay Option							
$T_{PICKD} = T_{PICK} + T_{Delay}$ $T_{PDLI} = T_{PLI} + T_{Delay}$	T_{Delay}	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL	4.0 4.8 5.0 5.5 6.5		4.7 5.6 5.9 6.5 7.6		ns ns ns ns ns
Global Set/Reset							
Minimum GSR pulse width	T_{MRW}	All devices	10.5		11.5		ns
Delay from GSR input to any Q	T_{RRI}	XCS05XL XCS10XL XCS20XL XCS30XL XCS40XL		9.0 9.5 10.0 11.0 12.0		10.5 11.0 11.5 12.5 13.5	ns ns ns ns ns

Note 1: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input, see the pin-to-pin parameters in the Pin-to-Pin Input Parameters table.

Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Spartan-XL IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values are expressed in nanoseconds unless otherwise noted.

		Speed Grade	-5		-4		Units
Description	**Symbol**	**Device**	**Min**	**Max**	**Min**	**Max**	
Propagation Delays							
Clock (OK) to Pad, fast	T_{OKPOF}	All devices		3.2		3.7	ns
Output (O) to Pad, fast	T_{OPF}	All devices		2.5		2.9	ns
3-state to Pad hi-Z (slew-rate independent)	T_{TSHZ}	All devices		2.8		3.3	ns
3-state to Pad active and valid, fast	T_{TSONF}	All devices		2.6		3.0	ns
Output (O) to Pad via Output Mux, fast	T_{OFPF}	All devices		3.7		4.4	ns
Select (OK) to Pad via Output Mux, fast	T_{OKFPF}	All devices		3.3		3.9	ns
For Output SLOW option add	T_{SLOW}	All devices		1.5		1.7	ns
Setup and Hold Times							
Output (O) to clock (OK) setup time	T_{OOK}	All devices	0.5		0.5		ns
Output (O) to clock (OK) hold time	T_{OKO}	All devices	0.0		0.0		ns
Clock Enable (EC) to clock (OK) setup time	T_{ECOK}	All devices	0.0		0.0		ns
Clock Enable (EC) to clock (OK) hold time	T_{OKEC}	All devices	0.1		0.2		ns
Global Set/Reset							
Minimum GSR pulse width	T_{MRW}	All devices	10.5		11.5		ns
Delay from GSR input to any Pad	T_{RPO}	XCS05XL		11.9		14.0	ns
		XCS10XL		12.4		14.5	ns
		XCS20XL		12.9		15.0	ns
		XCS30XL		13.9		16.0	ns
		XCS40XL		14.9		17.0	ns

Note 1: Output timing is measured at ~50% V_{CC} threshold, with 50 pF external capacitive loads including test fixture. Slew-rate limited output rise/fall times are approximately two times longer than fast output rise/fall times.
Note 2: Voltage levels of unused pads, bonded or unbonded, must be valid logic levels. Each can be configured with the internal pull-up (default) or pull-down resistor, or configured as a driven output, or can be driven from an external source.

Pin Descriptions

There are three types of pins in the Spartan/XL devices:

- Permanently dedicated pins
- User I/O pins that can have special functions
- Unrestricted user-programmable I/O pins.

Before and during configuration, all outputs not used for the configuration process are 3-stated with the I/O pull-up resistor network activated. After configuration, if an IOB is unused it is configured as an input with the I/O pull-up resistor network remaining activated.

Any user I/O can be configured to drive the Global Set/Reset net GSR or the global three-state net GTS. See "Global Signals: GSR and GTS" on page 78 for more information.

Device pins for Spartan/XL devices are described in Table 55.

For a complete Spartan and Spartan-XL data sheet including package pinouts, go to the CD-ROM or Xilinx web site:
www.xilinx.com/partinfo/databook.htm

Table 55: Pin Descriptions

Pin Name	I/O During Config.	I/O After Config.	Pin Description
Permanently Dedicated Pins			
VCC	X	X	Eight or more (depending on package) connections to the nominal +5V supply voltage (+3.3V for Spartan-XL devices). All must be connected, and each must be decoupled with a 0.01 –0.1 µF capacitor to Ground.
GND	X	X	Eight or more (depending on package type) connections to Ground. All must be connected.
CCLK	I or O	I	During configuration, Configuration Clock (CCLK) is an output in Master mode and is an input in Slave mode. After configuration, CCLK has a weak pull-up resistor and can be selected as the Readback Clock. There is no CCLK High or Low time restriction on Spartan/XL devices, except during Readback. See "Violating the Maximum High and Low Time Specification for the Readback Clock" on page 92 for an explanation of this exception.
DONE	I/O	O	DONE is a bidirectional signal with an optional internal pull-up resistor. As an output, it indicates the completion of the configuration process. As an input, a Low level on DONE can be configured to delay the global logic initialization and the enabling of outputs. The optional pull-up resistor is selected as an option in the program that creates the configuration bitstream. The resistor is included by default.
$\overline{\text{PROGRAM}}$	I	I	$\overline{\text{PROGRAM}}$ is an active Low input that forces the FPGA to clear its configuration memory. It is used to initiate a configuration cycle. When $\overline{\text{PROGRAM}}$ goes High, the FPGA finishes the current clear cycle and executes another complete clear cycle, before it goes into a WAIT state and releases $\overline{\text{INIT}}$. The $\overline{\text{PROGRAM}}$ pin has a permanent weak pull-up, so it need not be externally pulled up to VCC.
MODE (Spartan) M0, M1 (Spartan-XL)	I	X	The Mode input(s) are sampled after $\overline{\text{INIT}}$ goes High to determine the configuration mode to be used. During configuration, these pins have a weak pull-up resistor. For the most popular configuration mode, Slave Serial, the mode pins can be left unconnected. For Master Serial mode, connect the Mode/M0 pin directly to system ground.
$\overline{\text{PWRDWN}}$	I	I	$\overline{\text{PWRDWN}}$ is an active Low input that forces the FPGA into the Power Down state and reduces power consumption. When $\overline{\text{PWRDWN}}$ is Low, the FPGA disables all I/O and initializes all flip-flops. All inputs are interpreted as Low independent of their actual level. VCC must be maintained, and the configuration data is maintained. $\overline{\text{PWRDWN}}$ halts configuration if asserted before or during configuration, and re-starts configuration when removed. When $\overline{\text{PWRDWN}}$ returns High, the FPGA becomes operational by first enabling the inputs and flip-flops and then enabling the outputs. $\overline{\text{PWRDWN}}$ has a default internal pull-up resistor.
User I/O Pins That Can Have Special Functions			
TDO	O	O	If boundary scan is used, this pin is the Test Data Output. If boundary scan is not used, this pin is a 3-state output without a register, after configuration is completed. To use this pin, place the library component TDO instead of the usual pad symbol. An output buffer must still be used.

Table 55: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
TDI, TCK, TMS	I	I/O or I (JTAG)	If boundary scan is used, these pins are Test Data In, Test Clock, and Test Mode Select inputs respectively. They come directly from the pads, bypassing the IOBs. These pins can also be used as inputs to the CLB logic after configuration is completed. If the BSCAN symbol is not placed in the design, all boundary scan functions are inhibited once configuration is completed, and these pins become user-programmable I/O. In this case, they must be called out by special library elements. To use these pins, place the library components TDI, TCK, and TMS instead of the usual pad symbols. Input or output buffers must still be used.
HDC	O	I/O	High During Configuration (HDC) is driven High until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, HDC is a user-programmable I/O pin.
$\overline{\text{LDC}}$	O	I/O	Low During Configuration ($\overline{\text{LDC}}$) is driven Low until the I/O go active. It is available as a control output indicating that configuration is not yet completed. After configuration, $\overline{\text{LDC}}$ is a user-programmable I/O pin.
$\overline{\text{INIT}}$	I/O	I/O	Before and during configuration, $\overline{\text{INIT}}$ is a bidirectional signal. A 1 kΩ - 10 kΩ external pull-up resistor is recommended. As an active Low open-drain output, $\overline{\text{INIT}}$ is held Low during the power stabilization and internal clearing of the configuration memory. As an active Low input, it can be used to hold the FPGA in the internal WAIT state before the start of configuration. Master mode devices stay in a WAIT state an additional 30 to 300 µs after $\overline{\text{INIT}}$ has gone High. During configuration, a Low on this output indicates that a configuration data error has occurred. After the I/O go active, $\overline{\text{INIT}}$ is a user-programmable I/O pin.
PGCK1 - PGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Primary Global inputs each drive a dedicated internal global net with short delay and minimal skew. If not used to drive a global buffer, any of these pins is a user-programmable I/O. The PGCK1-PGCK4 pins drive the four Primary Global Buffers. Any input pad symbol connected directly to the input of a BUFGP symbol is automatically placed on one of these pins.
SGCK1 - SGCK4 (Spartan)	Weak Pull-up	I or I/O	Four Secondary Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The SGCK1-SGCK4 pins provide the shortest path to the four Secondary Global Buffers. Any input pad symbol connected directly to the input of a BUFGS symbol is automatically placed on one of these pins.
GCK1 - GCK8 (Spartan-XL)	Weak Pull-up	I or I/O	Eight Global inputs each drive a dedicated internal global net with short delay and minimal skew. These internal global nets can also be driven from internal logic. If not used to drive a global net, any of these pins is a user-programmable I/O pin. The GCK1-GCK8 pins provide the shortest path to the eight Global Low-Skew Buffers. Any input pad symbol connected directly to the input of a BUFGLS symbol is automatically placed on one of these pins.
CS1 (Spartan-XL)	I	I/O	During Express configuration, CS1 is used as a serial-enable signal for daisy-chaining.
D0-D7 (Spartan-XL)	I	I/O	During Express configuration, these eight input pins receive configuration data. After configuration, they are user-programmable I/O pins.
DIN	I	I/O	During Slave Serial or Master Serial configuration, DIN is the serial configuration data input receiving data on the rising edge of CCLK. After configuration, DIN is a user-programmable I/O pin.

Table 55: Pin Descriptions (Continued)

Pin Name	I/O During Config.	I/O After Config.	Pin Description
DOUT	O	I/O	During Slave Serial or Master Serial configuration, DOUT is the serial configuration data output that can drive the DIN of daisy-chained slave FPGAs. DOUT data changes on the falling edge of CCLK, one-and-a-half CCLK periods after it was received at the DIN input. In Spartan-XL Express mode, DOUT is the status output that can drive the CS1 of daisy-chained FPGAs, to enable and disable downstream devices. After configuration, DOUT is a user-programmable I/O pin.
Unrestricted User-Programmable I/O Pins			
I/O	Weak Pull-up	I/O	These pins can be configured to be input and/or output after configuration is completed. Before configuration is completed, these pins have an internal high-value pull-up resistor network that defines the logic level as High.

Product Availability

Table 56 shows the packages and speed grades for Spartan/XL devices. Table 57 shows the number of user I/Os available for each device/package combination.

Table 56: Component Availability Chart for Spartan/XL FPGAs

Device	PINS	84	100	144	144	208	240	256	280
	TYPE	Plastic PLCC	Plastic VQFP	Chip Scale	Plastic TQFP	Plastic PQFP	Plastic PQFP	Plastic BGA	Chip Scale
	CODE	PC84	VQ100	CS144	TQ144	PQ208	PQ240	BG256	CS280
XCS05	-3	C	C, I						
	-4	C	C						
XCS10	-3	C	C, I		C				
	-4	C	C		C				
XCS20	-3		C		C, I	C, I			
	-4		C		C	C			
XCS30	-3		C		C, I	C, I	C	C	
	-4		C		C	C	C	C	
XCS40	-3					C, I	C	C	
	-4					C	C	C	
XCS05XL	-4	C	C, I						
	-5	C	C						
XCS10XL	-4	C	C, I	C	C				
	-5	C	C	C	C				
XCS20XL	-4		C	C	C, I	C, I			
	-5		C	C	C	C			
XCS30XL	-4		C		C, I	C, I	C	C	C
	-5		C		C	C	C	C	C
XCS40XL	-4					C, I	C	C	C
	-5					C	C	C	C

5/19/99

C = Commercial T_J = 0° to +85°C

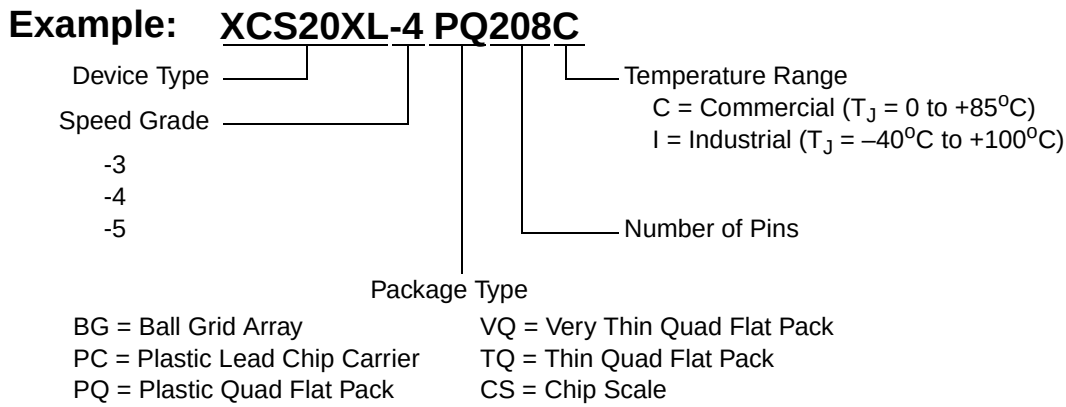
I = Industrial T_J = –40°C to +100°C

Table 57: User I/O Chart for Spartan/XL FPGAs

Device	Max I/O	Package Type							
		PC84	VQ100	CS144	TQ144	PQ208	PQ240	BG256	CS280
XCS05	80	61	77						
XCS10	112	61	77		112				
XCS20	160		77		113	160			
XCS30	192		77		113	169	192	192	
XCS40	224					169	192	205	
XCS05XL	80	61	77						
XCS10XL	112	61	77	112	112				
XCS20XL	160		77	113	113	160			
XCS30XL	192		77		113	169	192	192	192
XCS40XL	224					169	192	205	224

5/19/99

Ordering Information



4

Date	Version	Description
11/20/98	1.3	Added Spartan-XL specs and Power Down
1/6/99	1.4	All Spartan-XL -4 specs designated Preliminary with no changes
2/16/00	1.5	Added CS package, updated Spartan-XL specs to Final

PROM Products and Programming Support Table of Contents

XC18V00 Series of In-System Programmable Configuration PROMs

Spartan Family of PROMs

XC1700L and XC1700E

For a complete data sheet, go to CD-ROM or Xilinx web site: www.xilinx.com/partinfo/databook.htm

XC18V00 Series of In-System Programmable Configuration PROMs

DS026 (v2.2) March 3, 2000

Preliminary Product Specification

Features

- In-system programmable 3.3V PROMs for configuration of Xilinx FPGAs
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full commercial/industrial voltage and temperature range
- IEEE Std 1149.1 boundary-scan (JTAG) support
- Simple interface to the FPGA; could be configured to use only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Dual configuration modes
  - Serial Slow/Fast configuration (up to 15 MHz).
  - Parallel
- Low-power advanced CMOS FLASH process
- 5V tolerant I/O pins accept 5V, 3.3V and 2.5V signals.
- 3.3V or 2.5V output capability
- Available in PC20, SO20, PC44 and VQ44 packages.
- Design support using the Xilinx Alliance and Foundation series software packages.
- JTAG command initiation of standard FPGA configuration.

Description

Xilinx introduces the XC18V00 series of in-system programmable configuration PROMs. Initial devices in this 3.3V family are a 4-megabit, a 2-megabit, a 1-megabit, a 512-Kbit, a 256-Kbit, and a 128-Kbit PROM that provide an easy-to-use, cost-effective method for re-programming and storing large Xilinx FPGA or CPLD configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the PROM. A short access time after the rising CCLK, data is available on the PROM DATA (D0) pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. When the FPGA is in Slave Serial mode, the PROM and the FPGA are clocked by an external clock.

When the FPGA is in Express or SelectMAP Mode, an external oscillator will generate the configuration clock that drives the PROM and the FPGA. After the rising CCLK edge, data are available on the PROM's DATA (D0-D7) pins. The data will be clocked into the FPGA on the following rising edge of the CCLK. Neither Express nor SelectMAP utilize a Length Count, so a free-running oscillator may be used. See Figure 6.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all PROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family or with the XC1700L one-time programmable Serial PROM family.

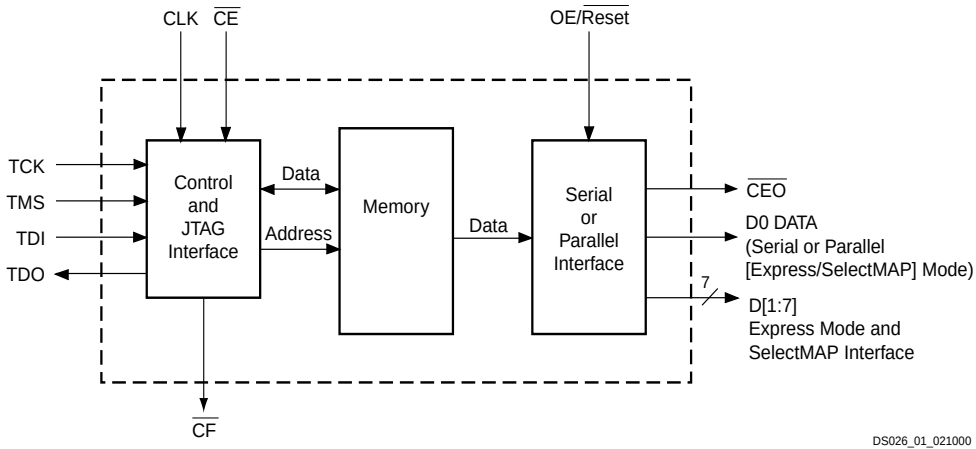


Figure 1: XC18V00 Series Block Diagram

Pinout and Pin Description

Table 1: Pin Names and Descriptions (pins not listed are "no connect")

Pin Name	Boundary Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
D0	4	DATA OUT	D0 is the DATA output pin to provide data for configuring an FPGA in serial mode.	40	2	1
	3	OUTPUT ENABLE				
D1	6	DATA OUT	D0-D7 are the output pins to provide parallel data for configuring a Xilinx FPGA in Express/ SelectMap mode.	29	35	16
	5	OUTPUT ENABLE				
D2	2	DATA OUT		42	4	2
	1	OUTPUT ENABLE				
D3	8	DATA OUT		27	33	15
	7	OUTPUT ENABLE				
D4	24	DATA OUT		9	15	7*
	23	OUTPUT ENABLE				
D5	10	DATA OUT		25	31	14
	9	OUTPUT ENABLE				
D6	17	DATA OUT		14	20	9
	16	OUTPUT ENABLE				
D7	14	DATA OUT		19	25	12
	13	OUTPUT ENABLE				
CLK	0	DATA IN	Each rising edge on the CLK input increments the internal address counter if both $\overline{CE}$ is Low and OE/$\overline{RESET}$ is High.	43	5	3
OE/ $\overline{RESET}$	20	DATA IN	When Low, this input holds the address counter reset and the DATA output is at High impedance. This is a bidirectional open-drain pin that is held Low while the PROM is reset. Polarity is NOT programmable.	13	19	8
	19	DATA OUT				
	18	OUTPUT ENABLE				
$\overline{CE}$	15	DATA IN	When $\overline{CE}$ is High, this pin puts the device into standby mode and resets the address counter. The DATA output pin is at High impedance, and the device is in low power standby mode.	15	21	10
$\overline{CF}$	22	DATA OUT	Allows JTAG CONFIG instruction to initiate FPGA configuration without powering down FPGA. This is an open-drain output that is pulsed Low by the JTAG CONFIG command.	10	16	7*
	21	OUTPUT ENABLE				

Pin Name	Boundary Scan Order	Function	Pin Description	44-pin VQFP	44-pin PLCC	20-pin SOIC & PLCC
$\overline{CEO}$	13	DATA OUT	Chip Enable Output ($\overline{CEO}$) is connected to the $\overline{CE}$ input of the next PROM in the chain. This output is Low when $\overline{CE}$ is Low and OE/$\overline{RESET}$ input is High, AND the internal address counter has been incremented beyond its Terminal Count (TC) value. When OE/$\overline{RESET}$ goes Low, $\overline{CEO}$ stays High until the PROM is brought out of reset by bringing OE/$\overline{RESET}$ High.	21	27	13
	14	OUTPUT ENABLE				
GND			GND is the ground connection.	6, 18, 28 & 41	3, 12, 24 & 34	11
TMS		MODE SELECT	The state of TMS on the rising edge of TCK determines the state transitions at the Test Access Port (TAP) controller. TMS has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the device if the pin is not driven.	5	11	5
TCK		CLOCK	This pin is the JTAG test clock. It sequences the TAP controller and all the JTAG test and programming electronics.	7	13	6
TDI		DATA IN	This pin is the serial input to all JTAG instruction and data registers. TDI has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.	3	9	4
TDO		DATA OUT	This pin is the serial output for all JTAG instruction and data registers. TDO has an internal 50K ohm resistive pull-up on it to provide a logic "1" to the system if the pin is not driven.	31	37	17
V_{CC}			Positive 3.3V supply voltage for internal logic and input buffers.	17, 35 & 38	23, 41 & 44	18 & 20
V_{CCO}			Positive 3.3V or 2.5V supply voltage connected to the output voltage drivers.	8, 16, 26 & 36	14, 22, 32 & 42	19

*Pin 7 is $\overline{CF}$ in Serial Mode, D4 in Express Mode for 20-pin packages.

Xilinx FPGAs and Compatible PROMs

Device	Configuration Bits	PROM
XC4003E	53,984	XC18V128
XC4005E	95,008	XC18V128
XC4006E	119,840	XC18V128
XC4008E	147,552	XC18V256
XC4010E	178,144	XC18V256
XC4013E	247,968	XC18V256
XC4020E	329,312	XC18V512
XC4025E	422,176	XC18V512
XC4002XL	61,104	XC18V128
XC4005XL	151,960	XC18V256
XC4010XL	283,424	XC18V512
XC4013XL/XLA	393,632	XC18V512
XC4020XL/XLA	521,880	XC18V512
XC4028XL/XLA/EX	668,184	XC18V01
XC4036XL/XLA/EX	832,528	XC18V01
XC4044XL/XLA	1,014,928	XC18V01
XC4052XL/XLA	1,215,368	XC18V02
XC4062XL/XLA	1,433,864	XC18V02
XC4085XL/XLA	1,924,992	XC18V02
XC40110XV	2,686,136	XC18V04
XC40150XV	3,373,448	XC18V04
XC40200XV	4,551,056	XC18V04 + XC18V512
XC40250XV	5,433,888	XC18V04 + XC18V02
XCV50	559,200	XC18V01
XCV100	781,216	XC18V01
XCV150	1,040,096	XC18V01
XCV200	1,335,840	XC18V02
XCV300	1,751,808	XC18V02
XCV400	2,546,048	XC18V04
XCV600	3,607,968	XC18V04
XCV800	4,715,616	XC18V04 + XC18V512
XCV1000	6,127,744	XC18V04 + XC18V02

Capacity

Devices	Configuration Bits
XC18V04	4,194,304
XC18V02	2,097,152
XC18V01	1,048,576
XC18V512	524,288
XC18V256	262,144
XC18V128	131,072

In-System Programming

One or more in-system programmable PROMs can be daisy chained together and programmed in-system via the standard 4-pin JTAG protocol as shown in Figure 2. In-system programming offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices. The Xilinx development system provides the programming data sequence using either Xilinx JTAG Programmer software and a download cable, a third-party JTAG development system, a JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence. The JTAG Programmer software also outputs serial vector format (SVF) files for use with any tools that accept SVF format and with automatic test euipment.

All outputs are 3-stated or held at clamp levels during in-system programming.

External Programming

Xilinx reprogrammable PROMs can also be programmed by the Xilinx HW-130 device programmer. This provides the added flexibility of using pre-programmed devices in board design and boundary-scan manufacturing tools, with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

Xilinx in-system programmable products provide a guaranteed endurance level of 10,000 in-system program/erase cycles and a minimum data retention of ten years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

Design Security

The Xilinx in-system programmable PROM devices incorporate advanced data security features to fully protect the programming data against unauthorized reading. Table 2 shows the security setting available.

The read security bit can be set by the user to prevent the internal programming pattern from being read or copied via JTAG. When set, it allows device erase. Erasing the entire device is the only way to reset the read security bit.

Table 2: Data Security Options

Default = Reset	Set
Read Allowed Program/Erase Allowed	Read Inhibited via JTAG Erase Allowed

5

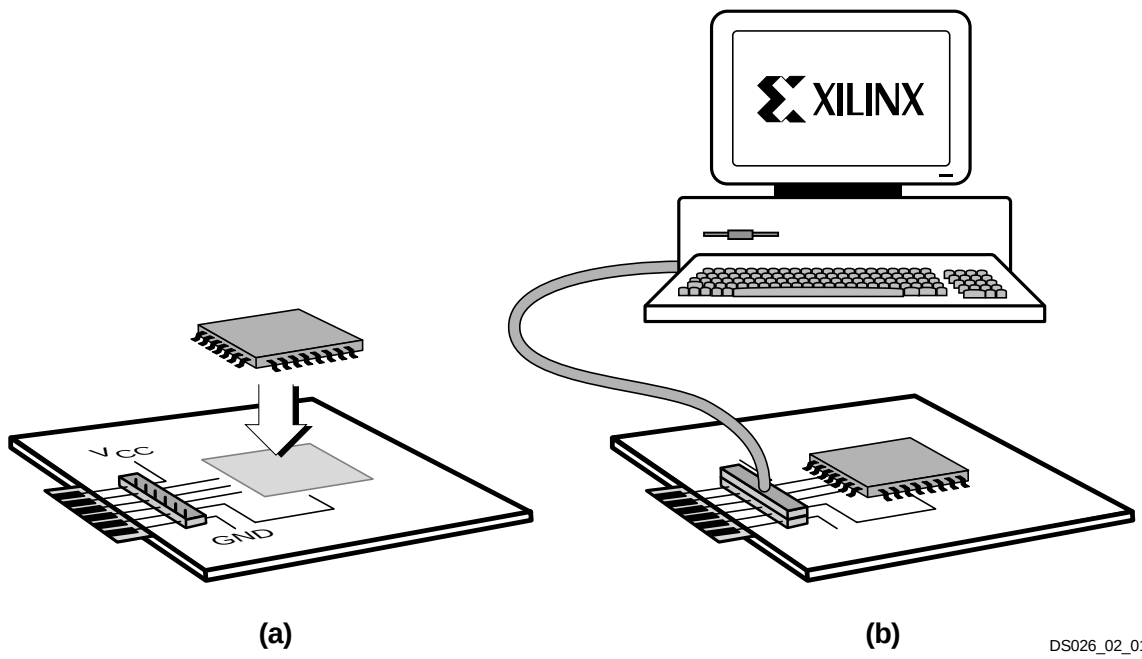


Figure 2: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

IEEE 1149.1 Boundary-Scan (JTAG)

The XC18V00 family is fully compliant with the IEEE Std. 1149.1 Boundary-Scan, also known as JTAG. A Test Access Port (TAP) and registers are provided to support all required boundary scan instructions, as well as many of the optional instructions specified by IEEE Std. 1149.1. In addition, the JTAG interface is used to implement in-system programming (ISP) to facilitate configuration, erasure, and verification operations on the XC18V00 device.

Table 3 lists the required and optional boundary-scan instructions supported in the XC18V00. Refer to the IEEE Std. 1149.1 specification for a complete description of boundary-scan architecture and the required and optional instructions.

Table 3: Boundary Scan Instructions

Boundary-Scan Command	Binary Code (7:0)	Description
Required Instructions		
BYPASS	11111111	Enables BYPASS
SAMPLE/ PRELOAD	00000001	Enables boundary-scan SAMPLE/PRELOAD operation
EXTEST	00000000	Enables boundary-scan EXTEST operation
Optional Instructions		
CLAMP	11111010	Enables boundary-scan CLAMP operation
HIGHZ	11111100	3-states all outputs simultaneously
IDCODE	11111110	Enables shifting out 32-bit IDCODE
USERCODE	11111101	Enables shifting out 32-bit USERCODE
XC18V00 Specific Instructions		
CONFIG	11101110	Initiates FPGA configuration by pulsing $\overline{CF}$ pin Low

Instruction Register

The Instruction Register (IR) for the XC18V00 is eight bits wide and is connected between TDI and TDO during an instruction scan sequence. In preparation for an instruction scan sequence, the instruction register is parallel loaded with a fixed instruction capture pattern. This pattern is shifted out onto TDO (LSB first), while an instruction is shifted into the instruction register from TDI. The detailed composition of the instruction capture pattern is illustrated in Figure 3.

The ISP Status field, IR(4), contains logic "1" if the device is currently in ISP mode; otherwise, it will contain "0". The Security field, IR(3), will contain logic "1" if the device has been programmed with the security option turned on; otherwise, it will contain "0".

	IR(7:5)	IR(4)	IR(3)	IR(2)	IR(1:0)	
TDI->	0 0 0	ISP Status	Security	0	0 1	->TDO

Note: IR(1:0) = 01 is specified by IEEE Std. 1149.1

Figure 3: Instruction Register Values Loaded into IR as Part of an Instruction Scan Sequence

Boundary Scan Register

The boundary-scan register is used to control and observe the state of the device pins during the EXTEST, SAMPLE/ PRELOAD, and CLAMP instructions. Each output pin on the XC18V00 has two register stages that contribute to the boundary-scan register, while each input pin only has one register stage.

For each output pin, the register stage nearest to TDI controls and observes the output state, and the second stage closest to TDO controls and observes the 3-state enable state of the pin.

For each input pin, the register stage controls and observes the input state of the pin.

Identification Registers

The IDCODE is a fixed, vendor-assigned value that is used to electrically identify the manufacturer and type of the device being addressed. The IDCODE register is 32-bits wide. The IDCODE register can be shifted out for examination by using the IDCODE instruction. The IDCODE is available to any other system component via JTAG.

The IDCODE register has the following binary format:

`vvvv:ffff:ffff:aaaa:aaaa:cccc:cccc:ccc1`

where

v = the die version number

f = the family code (50h for XC18V00 family)

a = the ISP PROM product ID (06h for the XC18V04)

c = the company code (49h for Xilinx)

Note: The LSB of the IDCODE register is always read as logic 1 as defined by IEEE Std. 1149.1

Table 4 lists the IDCODE register values for the XC18V00 devices.

Table 4: IDCODES Assigned to XC18V00 Devices

ISP-PROM	IDCODE
XC18V01	05004093h
XC18V04	05006093h

The USERCODE instruction gives access to a 32-bit user programmable scratch pad typically used to supply information about the device's programmed contents. By using the USERCODE instruction, a user-programmable identification code can be shifted out for examination. This code is loaded into the USERCODE register during programming of the XC18V00 device. If the device is blank or was not loaded during programming, the USERCODE register will contain FFFFFFFFh.

XC18V00 TAP Characteristics

The XC18V00 family performs both in-system programming and IEEE 1149.1 boundary-scan (JTAG) testing via a single 4-wire Test Access Port (TAP). This simplifies system designs and allows standard Automatic Test Equipment to perform both functions. The AC characteristics of the XC18V00 TAP are described as follows.

TAP Timing

Figure 4 shows the timing relationships of the TAP signals. These TAP timing characteristics are identical for both boundary-scan and ISP operations.

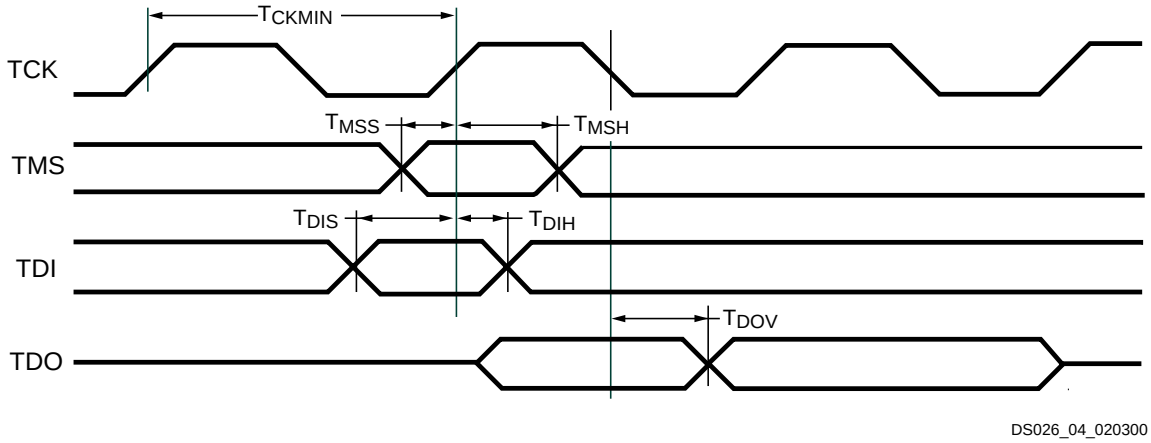


Figure 4: Test Access Port Timing

TAP AC Parameters

Table 5 shows the timing parameters for the TAP waveforms shown in Figure 4

Table 5: Test Access Port Timing Parameters

Symbol	Parameter	Min	Max	Units
T_{CKMIN1}	TCK Minimum Clock Period	100	-	ns
T_{CKMIN2}	TCK Minimum Clock Period, Bypass Mode	50	-	ns
T_{MSS}	TMS Setup Time	10	-	ns
T_{MSH}	TMS Hold Time	25	-	ns
T_{DIS}	TDI Setup Time	10	-	ns
T_{DIH}	TDI Hold Time	25	-	ns
T_{DOV}	TDO Valid Delay	-	25	ns

Connecting Configuration PROMs

Connecting the FPGA device with the configuration PROM (see Figure 6).

- The DATA output(s) of the of the PROM(s) drives the DIN input of the lead FPGA device.
- The Master FPGA CCLK output drives the CLK input(s) of the PROM(s).
- The $\overline{CEO}$ output of a PROM drives the $\overline{CE}$ input of the next PROM in a daisy chain (if any).
- The OE/$\overline{RESET}$ input of all PROMs is best driven by the $\overline{INIT}$ output of the lead FPGA device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch.
- The PROM $\overline{CE}$ input can be driven from the DONE pin. The $\overline{CE}$ input of the first (or only) PROM can be driven by the DONE output of the first FPGA device, provided that DONE is not permanently grounded. $\overline{CE}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.
- Express/SelectMap mode is similar to slave serial mode. The DATA is clocked out of the PROM one byte per CCLK instead of one bit per CCLK cycle. See FPGA data sheets for special configuration requirements.

Initiating FPGA Configuration

The XC18V00 devices incorporate a pin named $\overline{CF}$ that is controllable through the JTAG CONFIG instruction. Executing the CONFIG instruction through JTAG pulses the $\overline{CF}$ low for 300-500 ns, which resets the FPGA and initiates configuration.

The $\overline{CF}$ pin must be connected to the $\overline{PROGRAM}$ pin on the FPGA(s) to use this feature.

The JTAG Programmer software can also issue a JTAG CONFIG command to initiate FPGA configuration through the "Load FPGA" setting.

Selecting Configuration Modes

The XC18V00 accommodates serial and parallel methods of configuration. The configuration modes are selectable through a user control register in the XC18V00 device. This control register is accessible through JTAG, and is set using the "Parallel mode" setting on the Xilinx JTAG Programmer software. Master Serial is the default programming mode.

FPGA Configuration Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the three FPGA mode pins. In Master Serial mode, the FPGA automatically loads the configuration program from an external memory. Xilinx PROMs are designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, an FPGA enters the Master Serial mode whenever all three of the FPGA mode-select pins are Low (M0=0, M1=0, M2=0). Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial Mode provides a simple configuration interface. Only a serial data line, a clock line, and two control lines are required to configure an FPGA. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK. If the user-programmable, dual-function DIN pin on the FPGA is used only for configuration, it must still be held at a defined level during normal operation. The Xilinx FPGA families take care of this automatically with an on-chip pull-up resistor.

Cascading Configuration PROMs

For multiple FPGAs configured as a daisy-chain, or for FPGAs requiring larger configuration memories, cascaded PROMs provide additional memory (Figure 5). Multiple XC18V00 devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the data outputs of all XC18V00 devices in the chain are interconnected. After the last bit from the first PROM is read, the next clock signal to the PROM asserts its $\overline{CEO}$ output Low and 3-states its DATA line. The second PROM recognizes the Low level on its $\overline{CE}$ input and enables its DATA output. See Figure 6.

After configuration is complete, the address counters of all cascaded PROMs are reset if the PROM OE/$\overline{RESET}$ pin goes Low.

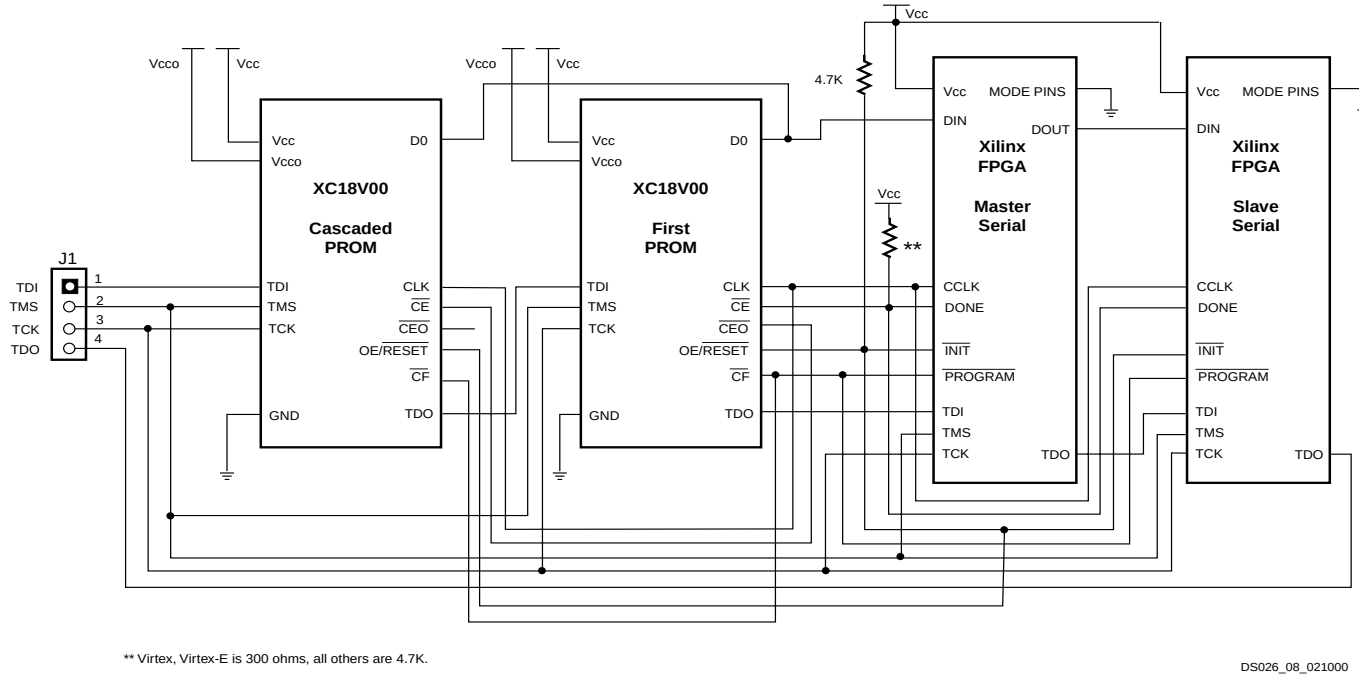
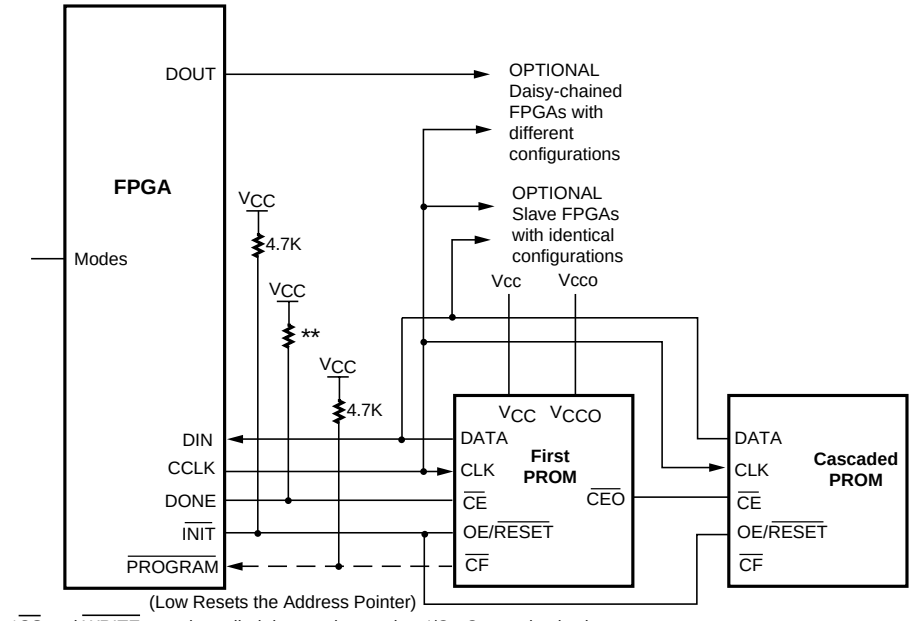
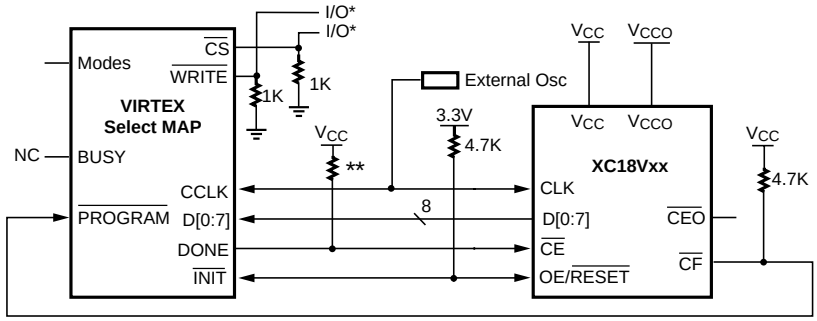


Figure 5: JTAG Chain for Configuring Devices in Master Serial Mode



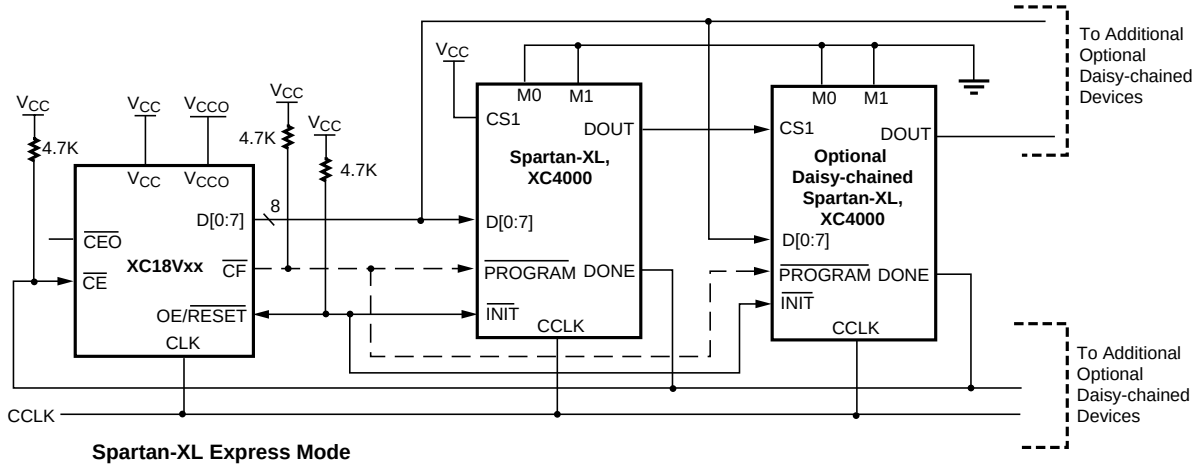
*$\overline{CS}$ and $\overline{WRITE}$ must be pulled down to be used as I/O. One option is shown.
**Virtex, Virtex-E is 300 ohms, all others are 4.7K.

Master Serial Mode



*$\overline{CS}$ and $\overline{WRITE}$ must be pulled down to be used as I/O. One option is shown.
**Virtex, Virtex-E is 300 ohms, all others are 4.7K.

Virtex Select MAP Mode



Spartan-XL Express Mode

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Figure 6: (a) Master Serial Mode (b) Virtex Select MAP Mode (c) Spartan-XL Express Mode (dotted lines indicates optional connection)

5V Tolerant I/Os

The I/Os on each re-programmable PROM are fully 5V tolerant even through the core power supply is 3.3V. This allows 5V CMOS signals to connect directly to the PROM inputs without damage. In addition, the 3.3V V_{CC} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CC}), and the output power supply (V_{CCO}) may have power applied in any order. This makes the PROM devices immune to power supply sequencing issues.

Reset Activation

On power up, OE/$\overline{\text{RESET}}$ is held low until the XC18V00 is active (1 ms) and able to supply data after receiving a CCLK pulse from the FPGA. OE/$\overline{\text{RESET}}$ is connected to an external resistor to pull OE/$\overline{\text{RESET}}$ HIGH releasing the FPGA $\overline{\text{INIT}}$ and allowing configuration to begin. OE/$\overline{\text{RESET}}$ is held low until the XC18V00 voltage reaches the operating voltage range. If the power drops below 2.0V, the PROM will reset. OE/$\overline{\text{RESET}}$ polarity is NOT programmable.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{\text{CE}}$ is asserted High. The output remains in a high impedance state regardless of the state of the OE input. JTAG pins TMS, TDI and TDO can be 3-state or High. The lower power standby modes available on some XC18V00 devices are set by the user in the programming software.

Customer Control Pins

The XC18V00 PROMs have various control bits accessible by the customer. These can be set after the array has been programmed using "Skip User Array" in Xilinx JTAG Programmer Software.

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Table 6: Truth Table for PROM Control Inputs

Control Inputs		Internal Address	Outputs		
OE/$\overline{\text{RESET}}$	**$\overline{\text{CE}}$**		**DATA**	**$\overline{\text{CEO}}$**	**I_{CC}**
High	Low	If address ≤ TC: increment If address > TC: don't change	Active 3-state	High Low	Active Reduced
Low	Low	Held reset	3-state	High	Active
High	High	Held reset	3-state	High	Standby
Low	High	Held reset	3-state	High	Standby

Note: TC = Terminal Count = highest address value. TC+1 = address 0.

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to +5.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to +5.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction Temperature	+150	°C

Notes

1: Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to +7.0V, provided this over- or undershoot lasts less then 10 ns and with the forcing current being limited to 200 mA.

2: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol		Parameter	Min	Max	Units
V_{CCINT}	Commercial	Internal Voltage supply (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Internal Voltage supply (T_A = –40°C to +85°C)	3.0	3.6	V
V_{CCO}	Supply voltage for output drivers for 3.3V operation		3.0	3.6	V
	Supply voltage for output drivers for 2.5V operation		2.3	2.7	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CCO}	V

Quality and Reliability Characteristics

Symbol	Description	Min	Max	Units
t_{DR}	Data Retention	10	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	10,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

DC Characteristics Over Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	High-level output voltage for 3.3V outputs	I_{OH} = –4 mA	2.4		V
	High-level output voltage for 2.5V outputs	I_{OH} = –500 µA	90% V_{CCO}		V
V_{OL}	Low-level output voltage for 3.3V outputs	I_{OL} = 8 mA		0.4	V
	Low-level output voltage for 2.5V outputs	I_{OL} = 500 µA		0.4	V
I_{CC}	Supply current, active mode	25 MHz		25	mA
I_{CCS1}	Supply current, standby mode 1 (default)			TBD	mA
I_{CCS2*}	Supply current, standby mode 2			TBD	µA
I_{CCS3**}	Supply current, standby mode 3			TBD	µA
I_{ILJ}	JTAG pins TMS, TDI, and TDO	V_{CC} = MAX V_{IN} = GND	–100		µA
I_{IL}	Input leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
I_{IH}	Input and Output High-Z leakage current	V_{CC} = Max V_{IN} = GND or V_{CC}	–10	10	µA
C_{IN} and C_{OUT}	Input and Output Capacitance	V_{IN} = GND f = 1.0 MHz		10	pF

***** 18V01/18V512/18V256/18V128 only, cascadable.
**18V01/18V512/18V256/18V128 only, non-cascadable, no brown-out protection.

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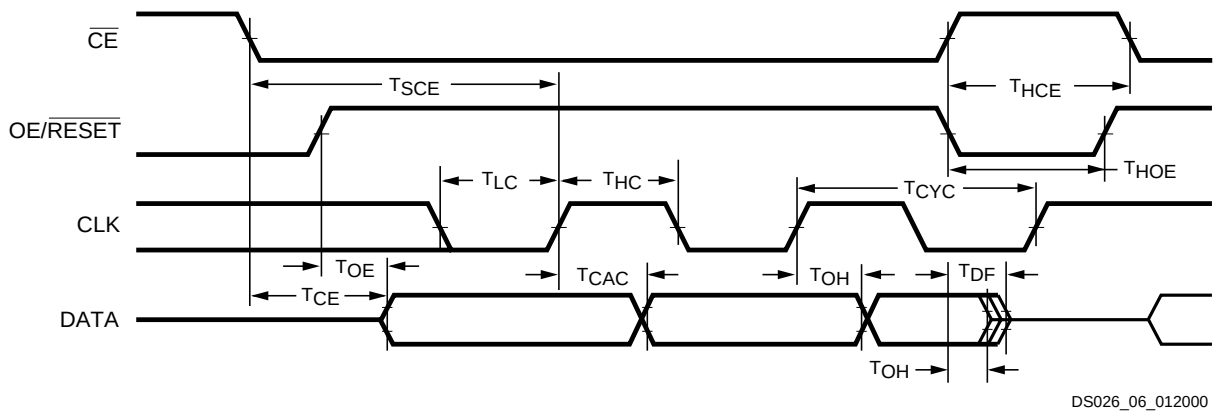
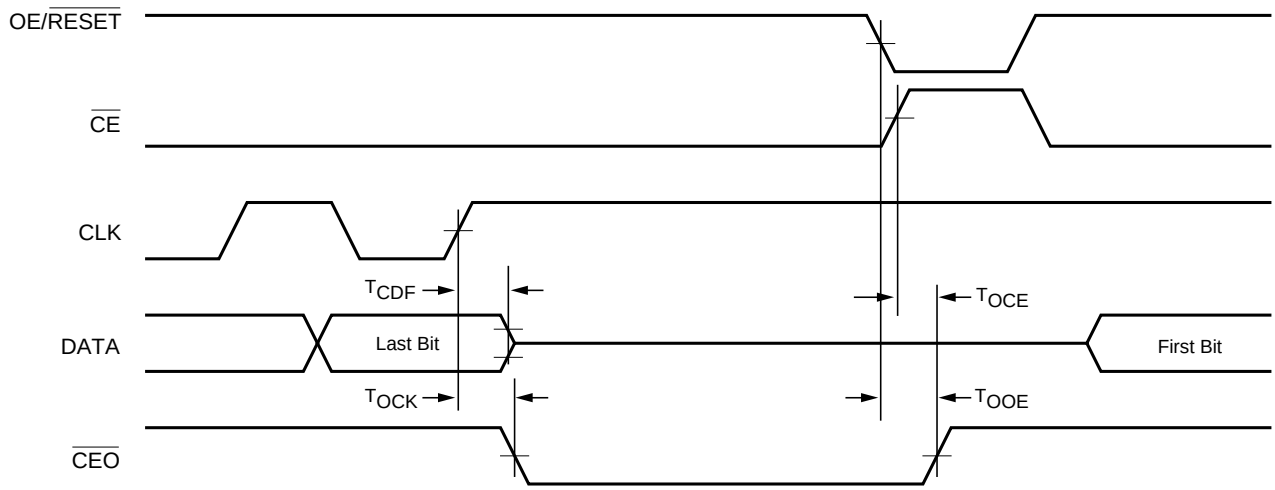
AC Characteristics Over Operating Conditions



Symbol	Description	Min	Max	Units
T_{OE}	OE/RESET to Data Delay		10	ns
T_{CE}	CE to Data Delay		20	ns
T_{CAC}	CLK to Data Delay		20	ns
T_{OH}	Data Hold From CE, OE/RESET, or CLK	0		ns
T_{DF}	CE or OE/RESET to Data Float Delay(2)		20	ns
T_{CYC}	Clock Periods	40		ns
T_{LC}	CLK Low Time(3)	10		ns
T_{HC}	CLK High Time(3)	10		ns
T_{HCE}	CE Hold Time to CLK (to guarantee proper counting)	2		µs
T_{HOE}	OE/RESET Hold Time (guarantees counters are reset)	25		ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Guaranteed by design, not tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.
5. If T_{HCE} High < 2 µs, T_{CE} = 2 µs.

AC Characteristics Over Operating Condition When Cascading



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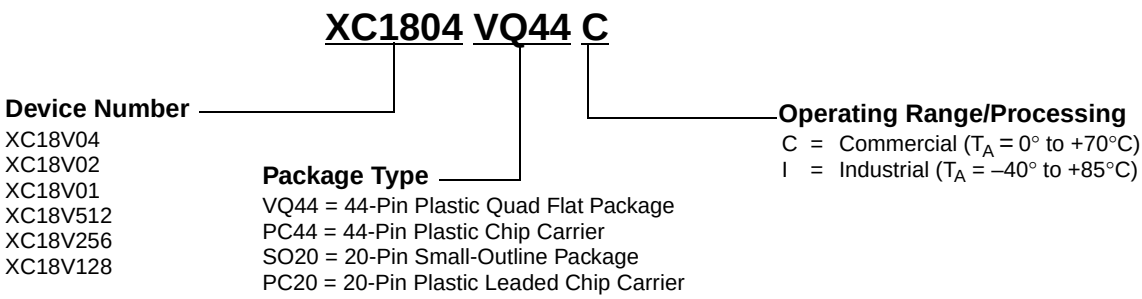
Symbol	Description	Min	Max	Units
T_{CDF}	CLK to Data Float Delay(2,3)		20	ns
T_{OCK}	CLK to $\overline{CEO}$ Delay(3)		20	ns
T_{OCE}	CE to $\overline{CEO}$ Delay(3)		20	ns
T_{OOE}	OE/$\overline{RESET}$ to $\overline{CEO}$ Delay(3)		20	ns

Notes: 1. AC test load = 50 pF
2. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
3. Characterized but not 100% tested.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

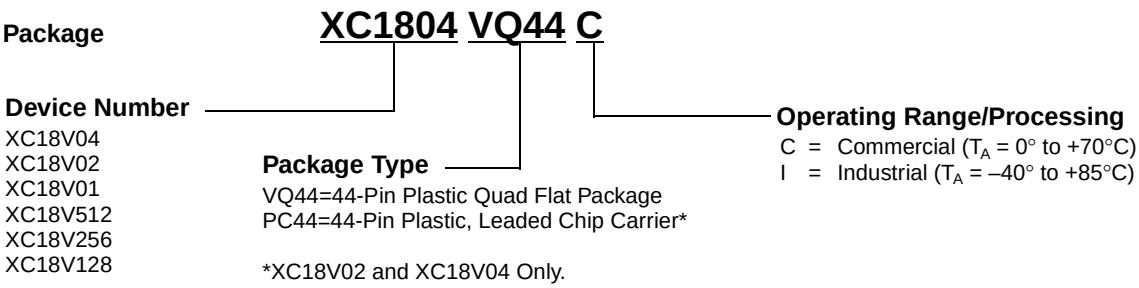


Valid Ordering Combinations

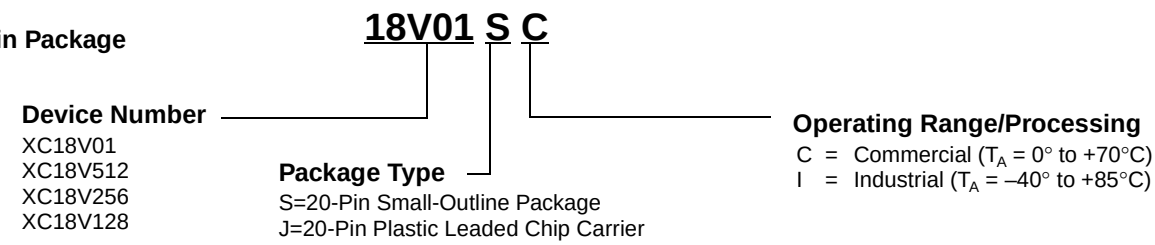
XC18V04VQ44C	XC18V02VQ44C	XC18V01VQ44C	XC18V512VQ44C	XC18V256VQ44C	XC18V128VQ44C
XC18V04PC44C	XC18V02PC44C	XC18V01PC20C	XC18V512PC20C	XC18V256PC20C	XC18V128PC20C
		XC18V01SO20C	XC18V512SO20C	XC18V256SO20C	XC18V128SO20C
XC18V04VQ44I	XC18V02VQ44I	XC18V01VQ44I	XC18V512VQ44I	XC18V256VQ44I	XC18V128VQ4I
XC18V04PC44I	XC18V02PC44I	XC18V01PC20I	XC18V512PC20I	XC18V256PC20I	XC18V128PC20I
		XC18V01SO20I	XC18V512SO20I	XC18V256SO20I	XC18V128SO20I

Marking Information

44-Pin Package



20-Pin Package



Revision Control

Date	Version	Revision
2/9/99	1.0	First publication of this early access specification
8/23/99	1.1	Edited text, changed marking, added $\overline{CF}$ and parallel load
9/1/99	1.2	Corrected JTAG order, Security and Endurance data.
9/16/99	1.3	Corrected SelectMAP diagram, control inputs, reset polarity. Added JTAG and $\overline{CF}$ description, 256 Kbit and 128 Kbit devices.
01/20/00	2.0	Added Q44 Package, changed XC18xx to XC18Vxx
02/18/00	2.1	Updated JTAG configuration, AC and DC characteristics
03/03/00	2.2	Removed stand alone resistor on INIT pin in Figure 5.

Introduction

The Spartan™ family of PROMs provide an easy-to-use, cost-effective method for storing Spartan device configuration bitstreams.

When the Spartan device is in Master Serial mode, it generates a configuration clock that drives the Spartan PROM. A short access time after the rising clock edge, data appears on the PROM DATA output pin that is connected to the Spartan device DIN pin. The Spartan device generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the PROM. When a Spartan device is in Slave Serial mode, the PROM and the Spartan device must both be clocked by an incoming signal.

For device programming, either the Xilinx Alliance or the Foundation series development systems compiles the Spartan device design file into a standard HEX format which is then transferred to most commercial PROM programmers.

Spartan PROM Features

- Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams for Spartan, Spartan-XL, and Spartan-II FPGA devices
- Simple interface to the Spartan device requires only one user I/O pin
- Programmable reset polarity (active High or active Low)
- Low-power CMOS floating gate process
- Available in 5V and 3.3V versions
- Available in compact plastic 8-pin DIP, 8-pin VOIC, or 20-pin SOIC (XC17S40 only) packages.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Spartan FPGA	Configuration Bits	Compatible Spartan PROM
XCS05	53,984	XC17S05
XCS05XL	54,544	XC17S05XL
XCS10	95,008	XC17S10
XCS10XL	95,752	XC17S10XL
XC2S15	197,728	XC17S15XL
XCS20	178,144	XC17S20
XCS20XL	179,160	XC17S20XL
XCS30	247,968	XC17S30
XCS30XL	249,168	XC17S30XL
XC2S30	336,768	XC17S30XL
XCS40	329,312	XC17S40
XCS40XL	330,696	XC17S40XL
XC2S50	559,232	XC17S50XL
XC2S100	781,248	XC17S100XL
XC2S150	1,040,128	XC17S150XL

Pin Description

Table 1: Spartan PROM Pinouts

Pin Name	8-pin PDIP & VOIC	20-pin SOIC	Pin Description
DATA	1	1	Data output, 3-stated when either $\overline{CE}$ or $\overline{OE}$ are inactive. During programming, the DATA pin is I/O. Note that $\overline{OE}$ can be programmed to be either active High or active Low.
CLK	2	3	Each rising edge on the CLK input increments the internal address counter, if both $\overline{CE}$ and $\overline{OE}$ are active.
RESET/$\overline{OE}$ (OE/$\overline{RESET}$)	3	8	When High, this input holds the address counter reset and 3-states the DATA output. The polarity of this input pin is programmable as either RESET/$\overline{OE}$ or OE/$\overline{RESET}$. To avoid confusion, this document describes the pin as RESET/$\overline{OE}$, although the opposite polarity is possible on all devices. When RESET is active, the address counter is held at zero, and the DATA output is 3-stated. The polarity of this input is programmable. The default is active High RESET, but the preferred option is active Low $\overline{RESET}$, because it can be driven by the FPGAs $\overline{INIT}$ pin. The polarity of this pin is controlled in the programmer interface. This input pin is easily inverted using the Xilinx HW-130 programmer software. Third-party programmers have different methods to invert this pin.
$\overline{CE}$	4	10	When High, this pin disables the internal address counter, 3-states the DATA output, and forces the device into low-I_{CC} standby mode.
GND	5	11	GND is the ground connection.
V_{CC}	7, 8	18, 20	The V_{CC} pins are to be connected to the positive voltage supply.

Controlling PROMs

Connecting the Spartan device with the PROM:

- The DATA output of the PROM drives the DIN input of the lead Spartan device.
- The Master Spartan device CCLK output drives the CLK input of the PROM.
- The $\overline{\text{RESET}}$/OE input of the PROM is driven by the $\overline{\text{INIT}}$ output of the Spartan device. This connection assures that the PROM address counter is reset before the start of any (re)configuration, even when a reconfiguration is initiated by a V_{CC} glitch. Other methods – such as driving $\overline{\text{RESET}}$/OE from $\overline{\text{LDC}}$ or system reset – assume that the PROM internal power-on-reset is always in step with the FPGA's internal power-on-reset, which may not be a safe assumption.
- The $\overline{\text{CE}}$ input of the PROM is driven by the DONE output of the Spartan device, provided that DONE is not permanently grounded. Otherwise, $\overline{\text{LDC}}$ can be used to drive $\overline{\text{CE}}$, but must then be unconditionally High during user operation. $\overline{\text{CE}}$ can also be permanently tied Low, but this keeps the DATA output active and causes an unnecessary supply current of 10 mA maximum.

FPGA Master Serial Mode Summary

The I/O and logic functions of the Configurable Logic Block (CLB) and their associated interconnections are established by a configuration program. The program is loaded either automatically upon power up, or on command, depending on the state of the Spartan device MODE pin. In Master Serial mode, the Spartan device automatically loads the configuration program from an external memory. The Spartan PROM has been designed for compatibility with the Master Serial mode.

Upon power-up or reconfiguration, the Spartan device enters the Master Serial mode when the MODE pin is Low. Data is read from the PROM sequentially on a single data line. Synchronization is provided by the rising edge of the temporary signal CCLK, which is generated during configuration.

Master Serial mode provides a simple configuration interface. Only a serial data line and two control lines are required to configure the Spartan device. Data from the PROM is read sequentially, accessed via the internal address and bit counters which are incremented on every valid rising edge of CCLK.

If the user-programmable, dual-function DIN pin on the Spartan device is used only for configuration, it must still be held at a defined level during normal operation. The Spartan family takes care of this automatically with an on-chip default pull-up resistor.

Programming the FPGA With Counters Unchanged Upon Completion

When multiple-configurations for a single Spartan device are stored in a PROM, the $\overline{\text{OE}}$ pin should be tied Low. Upon power-up, the internal address counters are reset and configuration begins with the first program stored in memory. Since the $\overline{\text{OE}}$ pin is held Low, the address counters are left unchanged after configuration is complete. Therefore, to reprogram the FPGA with another program, the DONE line is pulled Low and configuration begins at the last value of the address counters.

This method fails if a user applies $\overline{\text{RESET}}$ during the Spartan device configuration process. The Spartan device aborts the configuration and then restarts a new configuration, as intended, but the PROM does not reset its address counter, since it never saw a High level on its $\overline{\text{OE}}$ input. The new configuration, therefore, reads the remaining data in the PROM and interprets it as preamble, length count etc. Since the Spartan device is the Master, it issues the necessary number of CCLK pulses, up to 16 million (2^{24}) and DONE goes High. However, the Spartan device configuration will be completely wrong, with potential contentions inside the Spartan device and on its output pins. This method must, therefore, never be used when there is any chance of external reset during configuration.

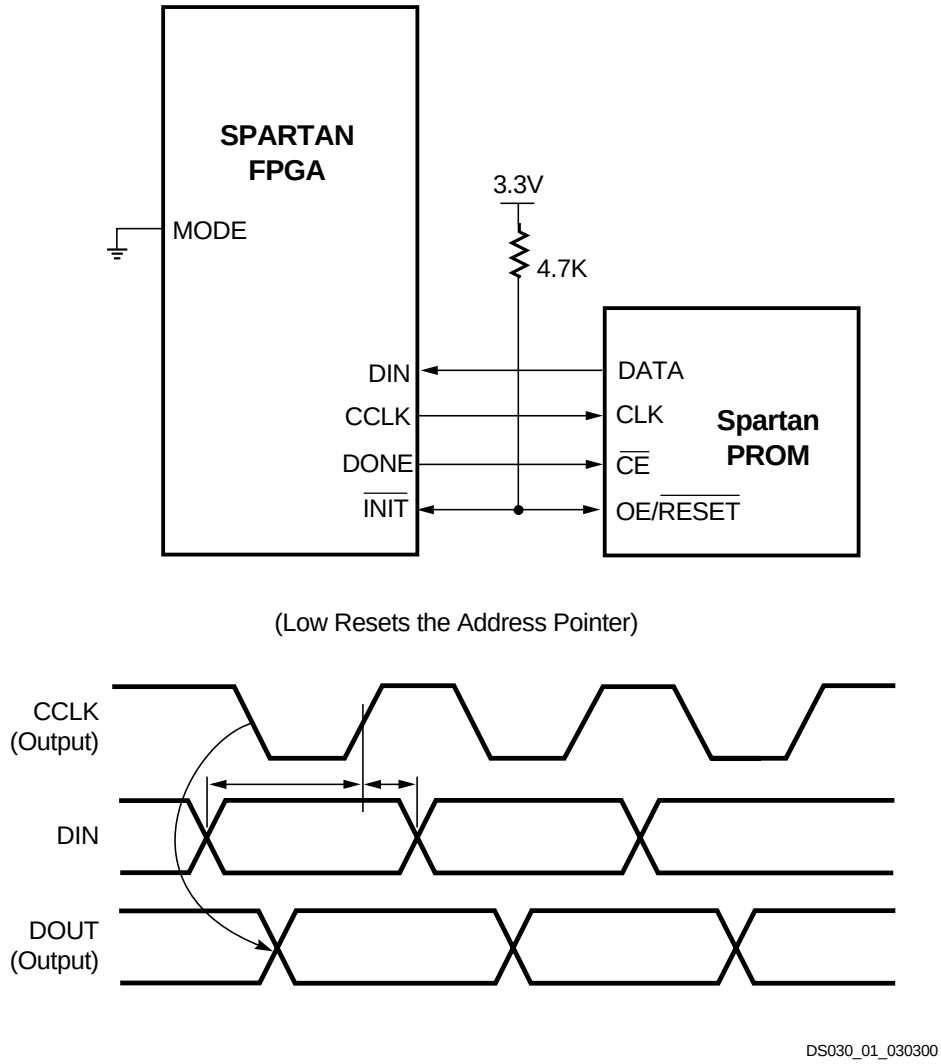


Figure 1: Master Serial Mode. The one-time-programmable Spartan PROM supports automatic loading of configuration programs. An early DONE inhibits the PROM data output one CCLK cycle before the Spartan FPGA I/Os become active.

Standby Mode

The PROM enters a low-power standby mode whenever $\overline{CE}$ is asserted High. The output remains in a high impedance state regardless of the state of the $\overline{OE}$ input.

Programming the Spartan Family PROMs

The devices can be programmed on programmers supplied by Xilinx or qualified third-party vendors. The user must ensure that the appropriate programming algorithm and the latest version of the programmer software are used. The wrong choice can permanently damage the device.

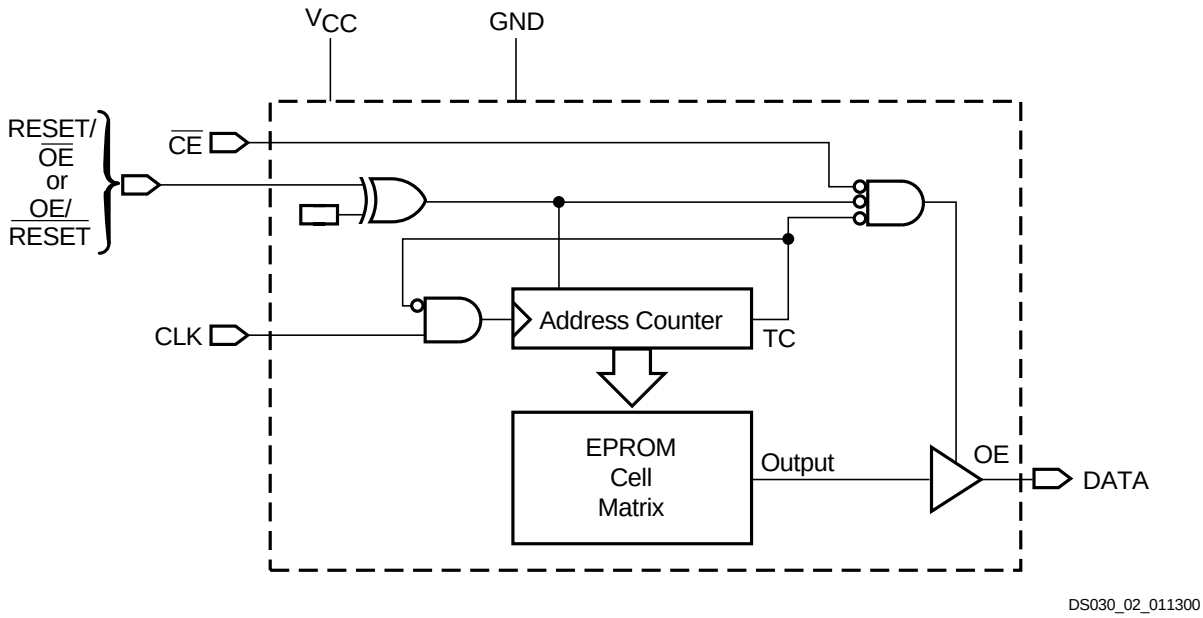


Figure 2: Simplified Block Diagram (does not show programming circuit)

Important: Always tie the two V_{CC} pins together in your application.

Table 2: Truth Table for XC17S00 Control Inputs

Control Inputs		Internal Address	Outputs	
RESET	**CE**		**DATA**	**I_{cc}**
Inactive	Low	If address ≤ TC: increment If address > TC: don't change	Active 3-state	Active Reduced
Active	Low	Held reset	3-state	Active
Inactive	High	Not changing	3-state	Standby
Active	High	Held reset	3-state	Standby

Notes: 1. The XC17S00 RESET input has programmable polarity
2. TC = Terminal Count = highest address value. TC+1 = address 0.

XC17S05, XC17S10, XC17S20, XC17S30, XC17S40

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage relative to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	4.75	5.25	V
	Industrial	Supply voltage relative to GND (T_A = –40°C to +85°C)	4.50	5.50	V

Note: During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description		Min	Max	Units
V_{IH}	High-level input voltage		2.0	V_{CC}	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Commercial	3.86		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.32	V
V_{OH}	High-level output voltage (I_{OH} = –4 mA)	Industrial	3.76		V
V_{OL}	Low-level output voltage (I_{OL} = +4 mA)			0.37	V
I_{CCA}	Supply current, active mode (at maximum frequency)			10.0	mA
I_{CCS}	Supply current, standby mode	XC17S05, XC17S10, XC17S20, XC17S30		50.0	µA
		XC17S40		100.0	µA
I_L	Input or output leakage current		–10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)			10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)			10.0	pF

XC17S05XL, XC17S10XL, XC17S15XL, XC17S20XL, XC17S30XL, XC17S40XL, XC17S50XL, XC17S100XL, XC17S150XL

Absolute Maximum Ratings

Symbol	Description	Value	Units
V_{CC}	Supply voltage relative to GND	–0.5 to +4.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output	–0.5 to V_{CC} +0.5	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

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Operating Conditions

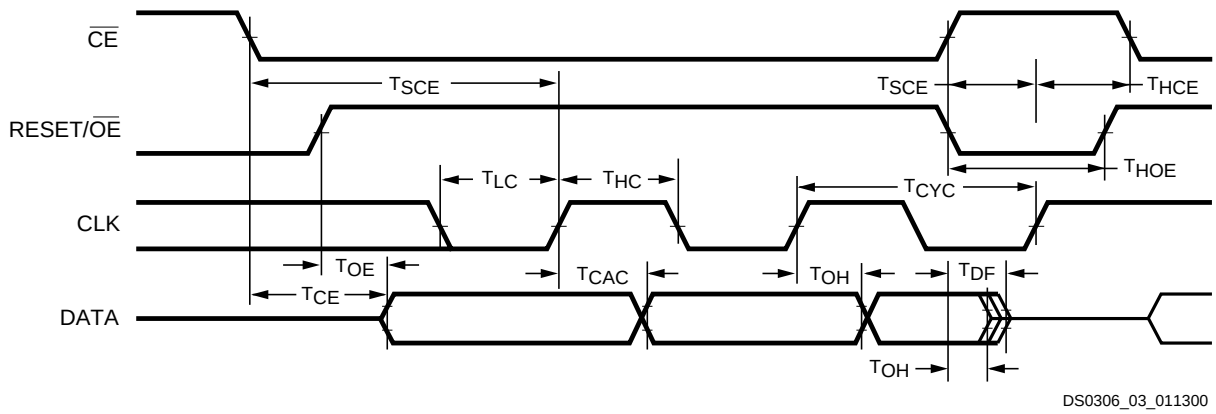
Symbol	Description		Min	Max	Units
V_{CC}	Commercial	Supply voltage relative to GND (T_A = 0°C to +70°C)	3.0	3.6	V
	Industrial	Supply voltage relative to GND (T_A = –40°C to +85°C)	3.0	3.6	V

Note: During normal read operation both V_{CC} pins must be connected together.

DC Characteristics Over Operating Condition

Symbol	Description	Min	Max	Units
V_{IH}	High-level input voltage	2.0	V_{CC}	V
V_{IL}	Low-level input voltage	0	0.8	V
V_{OH}	High-level output voltage (I_{OH} = –3 mA)	2.4		V
V_{OL}	Low-level output voltage (I_{OL} = +3 mA)		0.4	V
I_{CCA}	Supply current, active mode (at maximum frequency)		5.0	mA
I_{CCS}	Supply current, standby mode		50.0	µA
I_L	Input or output leakage current	–10.0	10.0	µA
C_{IN}	Input Capacitance (V_{IN} = GND, f = 1.0 MHz)		10.0	pF
C_{OUT}	Output Capacitance (V_{IN} = GND, f = 1.0 MHz)		10.0	pF

AC Characteristics Over Operating Condition



Symbol	Description	Min	Max	Units
T_{OE}	RESET/$\overline{OE}$ to Data Delay		45	ns
T_{CE}	$\overline{CE}$ to Data Delay		60	ns
T_{CAC}	CLK to Data Delay		80	ns
T_{OH}	Data Hold From $\overline{CE}$, RESET/$\overline{OE}$, or CLK(2)	0		ns
T_{DF}	$\overline{CE}$ or RESET/$\overline{OE}$ to Data Float Delay(2,3)		50	ns
T_{CYC}	Clock Periods	100		ns
T_{LC}	CLK Low Time(2)	50		ns
T_{HC}	CLK High Time(2)	50		ns
T_{SCE}	$\overline{CE}$ Setup Time to CLK (to guarantee proper counting)	25		ns
T_{HCE}	$\overline{CE}$ Hold Time to CLK (to guarantee proper counting)	0		ns
T_{HOE}	RESET/$\overline{OE}$ Hold Time (guarantees counters are reset)	25		ns

Notes: 1. AC test load = 50 pF
2. Guaranteed by design, not tested.
3. Float delays are measured with 5 pF AC loads. Transition is measured at ±200 mV from steady state active levels.
4. All AC parameters are measured with V_{IL} = 0.0V and V_{IH} = 3.0V.

Ordering Information

XC17S20XL VO8 C

Device Number
XC17S05
XC17S05XL
XC17S10
XC17S10XL
XC17S15XL
XC17S20
XC17S20XL
XC17S30
XC17S30XL
XC17S40
XC17S40XL
XC17S50XL
XC17S100XL
XC17S150XL

Package Type
PD8 = 8-pin Plastic DIP
VO8 = 8-pin Plastic Small-Outline Thin Package
SO20 = 20-pin Plastic Small-Outline Package

Operating Range/Processing
C = Commercial (T_A = 0°C to +70°C)
I = Industrial (T_A = –40°C to +85°C)

Valid Ordering Combinations

Spartan 5V	Spartan 5V	Spartan 3.3V	Spartan 3.3V	Spartan3.3V
XC17S05PD8C	XC17S20PD8C	XC17S05XLPD8C	XC17S20XLPD8C	XC17S50XLPD8C
XC17S05VO8C	XC17S20VO8C	XC17S05XLVO8C	XC17S20XLVO8C	XC17S50XLSO20C
XC17S05PD8I	XC17S20PD8I	XC17S05XLPD8I	XC17S20XLPD8I	XC17S50XLPD8I
XC17S05VO8I	XC17S20VO8I	XC17S05XLVO8I	XC17S20XLVO8I	XC17S50XLSO20I
XC17S10PD8C	XC17S30PD8C	XC17S10XLPD8C	XC17S30XLPD8C	XC17S100XLPD8C
XC17S10VO8C	XC17S30VO8C	XC17S10XLVO8C	XC17S30XLVO8C	XC17S100XLSO20C
XC17S10PD8I	XC17S30PD8I	XC17S10XLPD8I	XC17S30XLPD8I	XC17S100XLPD8I
XC17S10VO8I	XC17S30VO8I	XC17S10XLVO8I	XC17S30XLVO8I	XC17S100XLSO20I
	XC17S40PD8C	XC17S15XLPD8C	XC17S40XLPD8C	XC17S150XLPD8C
	XC17S40SO20C	XC17S15XLVO8C	XC17S40XLSO20C	XC17S150XLSO20C
	XC17S40PD8I	XC17S15XLPD8I	XC17S40XLVO8C	XC17S150XLPD8I
	XC17S40SO20I	XC17S15XLVO8I	XC17S40XLPD8I	XC17S150XLSO20I
			XC17S40XLSO20I	
			XC17S40XLVO8I	

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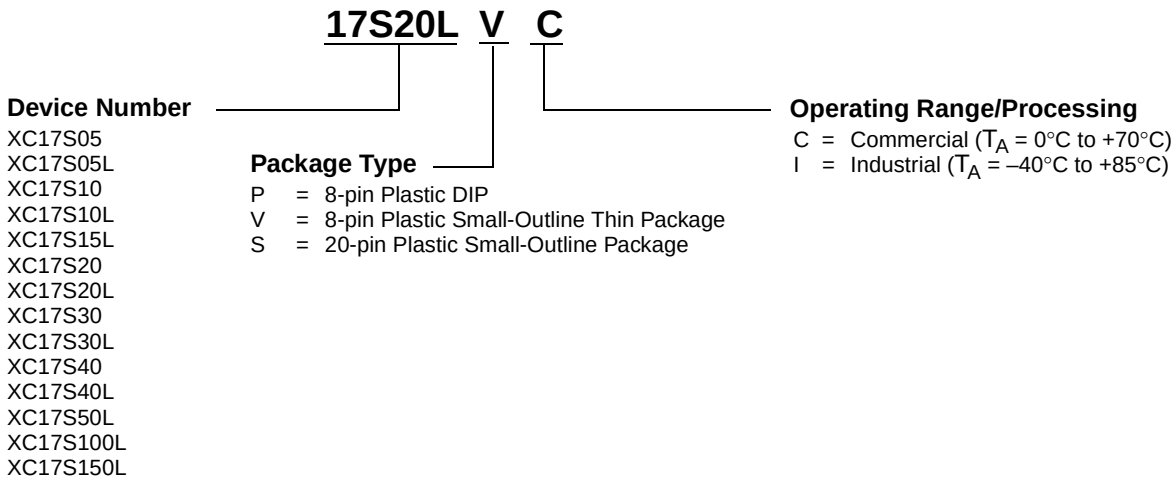
Marking Information

Due to the small size of the PROM package, the complete ordering part number cannot be marked on the package. The XC prefix is deleted and the package code is simplified. Device marking is as follows.



Note: When marking the device number on the XL parts, an L is used in place of an XL.

Revision Control

Date	Revision
7/14/98	Cosmetic edits for pages 19, 20, 21 & 22.
9/8/98	Clarified the SPARTAN FPGA and PROM interface by removing references to $\overline{CEO}$ pin. Removed the ESD notation in Absolute Maximum table since it is now included in Xilinx's Reliability Monitor Report.
01/20/00	Added additional Spartan-XL parts, changed SPROM to PROM.
02/18/00	Changed device ordering numbers.

CPLD: CoolRunner and XC9500 Table of Contents

CoolRunner™ XPLA3 CPLD Family

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CoolRunner™ XPLA3 CPLD

DS012 (v1.1) March 3, 2000 Advance Product Specification

Features

- Fast Zero Power (FZP™) design technique provides ultra-low power and very high speed
- Innovative XPLA3 architecture combines high speed with extreme flexibility
- Based on industry's first TotalCMOS™ PLD - both CMOS design and process technologies
- Advanced 0.35µ five metal layer E^2CMOS process
  - 1,000 erase/program cycles guaranteed
  - 20 years data retention guaranteed
- 3V, In-System Programmable (ISP) using JTAG IEEE 1149.1 interface
  - Full Boundary Scan Test (IEEE 1149.1)
- Ultra-low static power of less than 100 µA
- Simple deterministic timing model
- Support for complex asynchronous clocking
  - 16 product term clocks and four local control term clocks per logic block
  - Four global clocks and one universal control term clock per device
- Excellent pin retention during design changes
- 5V tolerant I/O pins
- Input register set up time of 1.7 ns
- Logic expandable to 48 product terms
- High-speed pin-to-pin delays of 5.0 ns
- Slew rate control per macrocell
- 100% routable
- Security bit prevents unauthorized access
- Supports hot-plugging capability
- Design entry/verification using Xilinx or industry standard CAE tools
- Innovative Control Term structure provides:
  - Asynchronous macrocell clocking
  - Asynchronous macrocell register preset/reset
  - Clock enable control per macrocell
- Four output enable controls per logic block
- Foldback NAND for synthesis optimization
- Global 3-state which facilitates "bed of nails" testing
- Available in Chip-scale BGA, and QFP packages
- Commercial and extended voltage industrial grades
- Pin compatible with existing CoolRunner low-power family devices

Family Overview

The CoolRunner XPLA3 (eXtended Programmable Logic Array) family of CPLDs is targeted for low power systems that include portable, handheld, and power sensitive applications. Each member of the XPLA3 family includes Fast Zero Power (FZP) design technology that combines low power and high speed. With this design technique, the XPLA3 family offers true pin-to-pin speeds of 5.0 ns, while simultaneously delivering power that is less than 100 µA at standby without the need for "turbo bits" or other power down schemes. By replacing conventional sense amplifier methods for implementing product terms (a technique that has been used in PLDs since the bipolar era) with a cascaded chain of pure CMOS gates, the dynamic power is also substantially lower than any competing CPLD. CoolRunner devices are the only TotalCMOS PLDs, as they use both a CMOS process technology and the patented full CMOS FZP design technique.

To the original XPLA architecture, XPLA3 adds a direct input register path, multiple clocks (both dedicated and product term generated), and both reset and preset for each macrocell, with a full PLA structure. These enhancements deliver high speed coupled with very flexible logic allocation which results in the ability to make design changes without changing pinout. The XPLA3 logic block includes a pool of 48 product terms that can be allocated to any macrocell in the logic block. Logic that is common to multiple macrocells can be placed on a single PLA product term and shared, effectively increasing design density.

XPLA3 CPLDs are supported by WebPACK from Xilinx and industry standard CAE tools (Cadence/OrCAD, Exemplar Logic, Mentor, Synopsys, Viewlogic, andd Synplicity), using text (ABEL, VHDL, Verilog) and schematic capture design entry. Design verification uses industry standard simulators for functional and timing simulation. Development is supported on personal computer, Sparc, and HP platforms. Device fitting uses Xilinx developed tools including WebFITTER.

The XPLA3 family features also include industry-standard, IEEE 1149.1, JTAG interface through which In-System Programming (ISP) and reprogramming of the device can

occur. The XPLA3 CPLD is electrically reprogrammable using industry standard device programmers from vendors such as Data I/O, BP Microsystems, and SMS.

XPLA3 Architecture

Figure 1 shows a high-level block diagram of a 128 macrocell device implementing the XPLA3 architecture. The XPLA3 architecture consists of logic blocks that are interconnected by a Zero-power Interconnect Array (ZIA). The ZIA is a virtual crosspoint switch. Each logic block has 36 inputs from the ZIA and 16 macrocells.

From this point of view, this architecture looks like many other CPLD architectures. What makes the XPLA3 family unique is logic allocation inside each logic block and the design technique used to implement these logic blocks.

Logic Block Architecture

Figure 2 illustrates the logic block architecture. Each logic block contains a PLA array that generates control terms, clock terms, and logic cells. There are 36 pairs of true and complement inputs from the ZIA that feed the 48 product terms in the array. Within the 48 P-terms there are eight local control terms (LCT[0:7]) available as control inputs to each macrocell for use as asynchronous clocks, resets, presets and output enables. The other P-terms serve as additional single inputs into each macrocell.

There are eight foldback NAND P-terms that are available for ease of fitting and pin locking. Sixteen product terms are coupled with the associated programmable OR gate into the VFM (Variable Function Multiplexer). The VFM increases logic optimization by implementing any two input logic funtion before entering the macrocell (see Figure 3).

Each macrocell can support combinatorial or registered inputs, preset and reset on a per macrocell basis and configurable D, T registers, or latch function. If a macrocell needs more product terms, it simply gets the additional product terms from the PLA array.

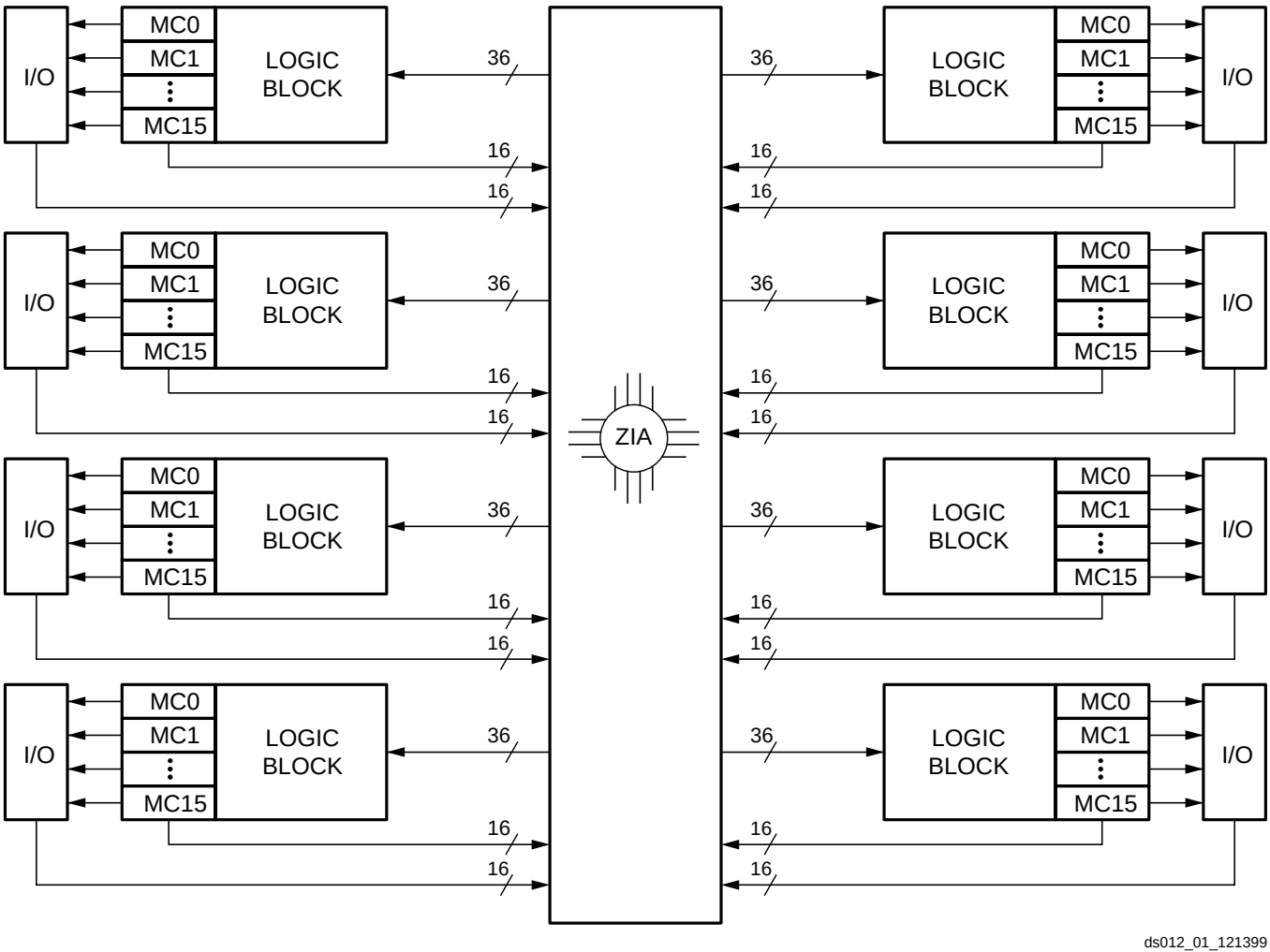


Figure 1: Xilinx XPLA3 CPLD Architecture

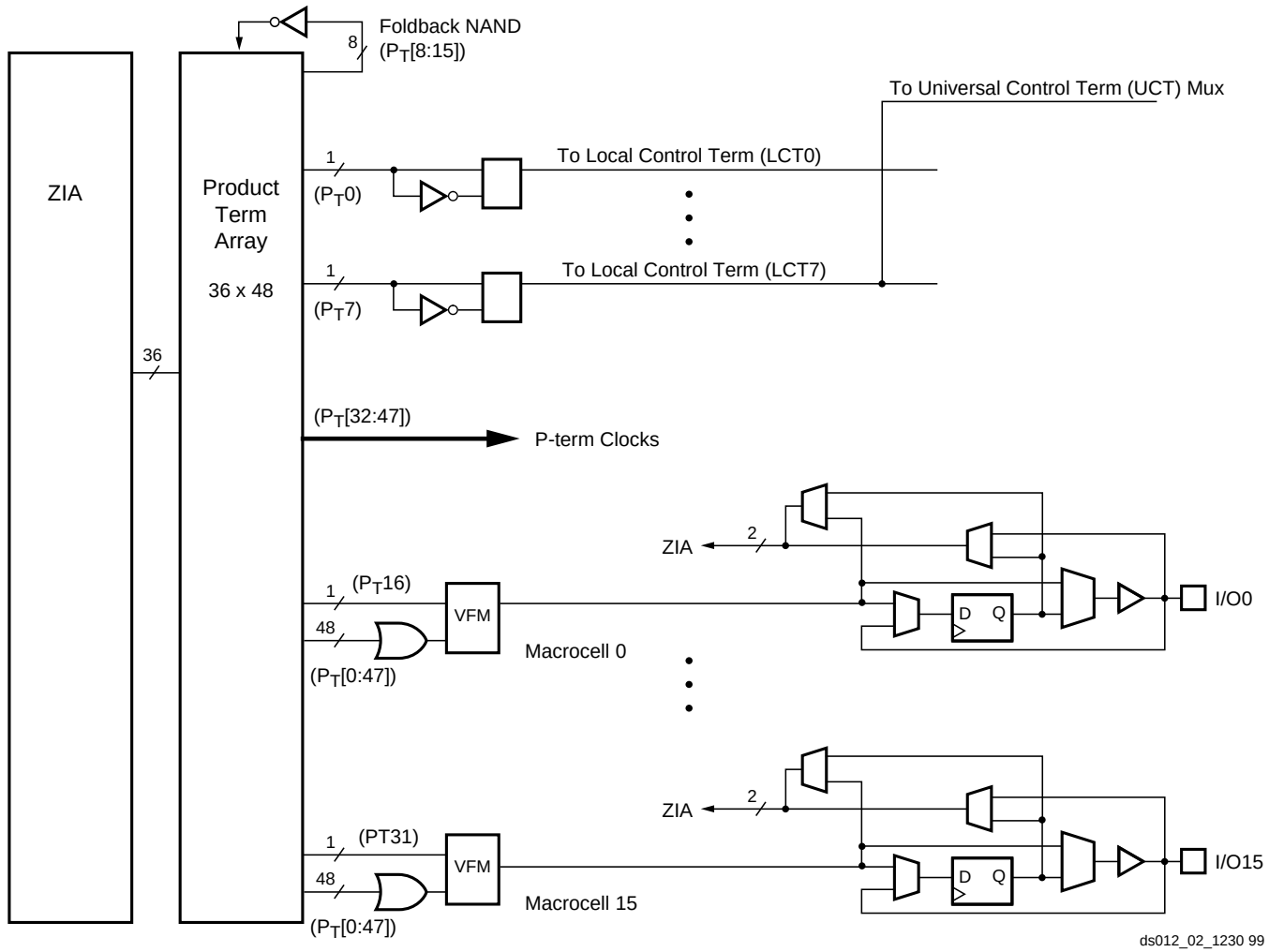


Figure 2: Xilinx XPLA3 Logic Block Architecture

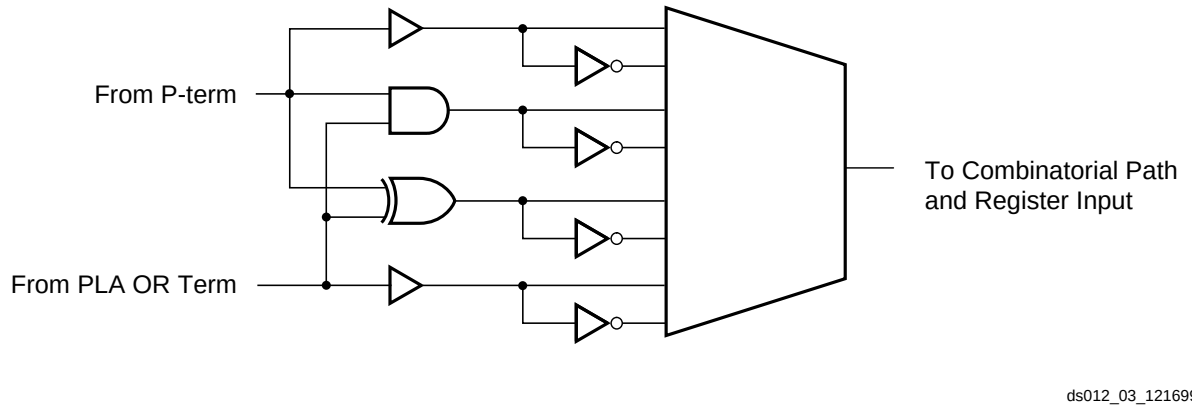


Figure 3: Variable Function Multiplexer

FoldBack NANDs

XPLA3 utilizes FoldBack NANDs to increase the effective product term width of a programmable logic device. These structures effectively provide an inverted product term to be used as a logic input by all of the local product terms. Refer to Figure 4 for an example of this technique. .

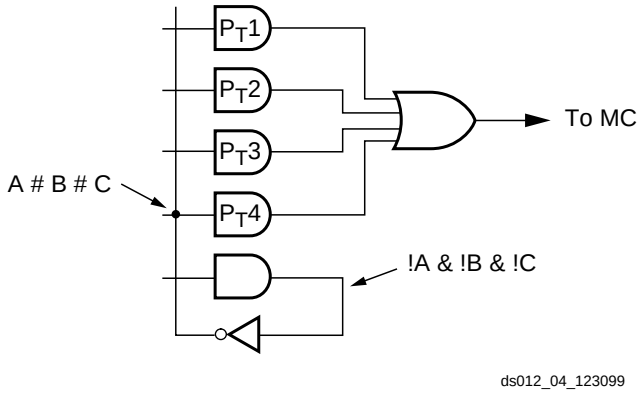


Figure 4: Basic FoldBack NAND Structure

As seen in Figure 4, the output signal is determined by the following equation:

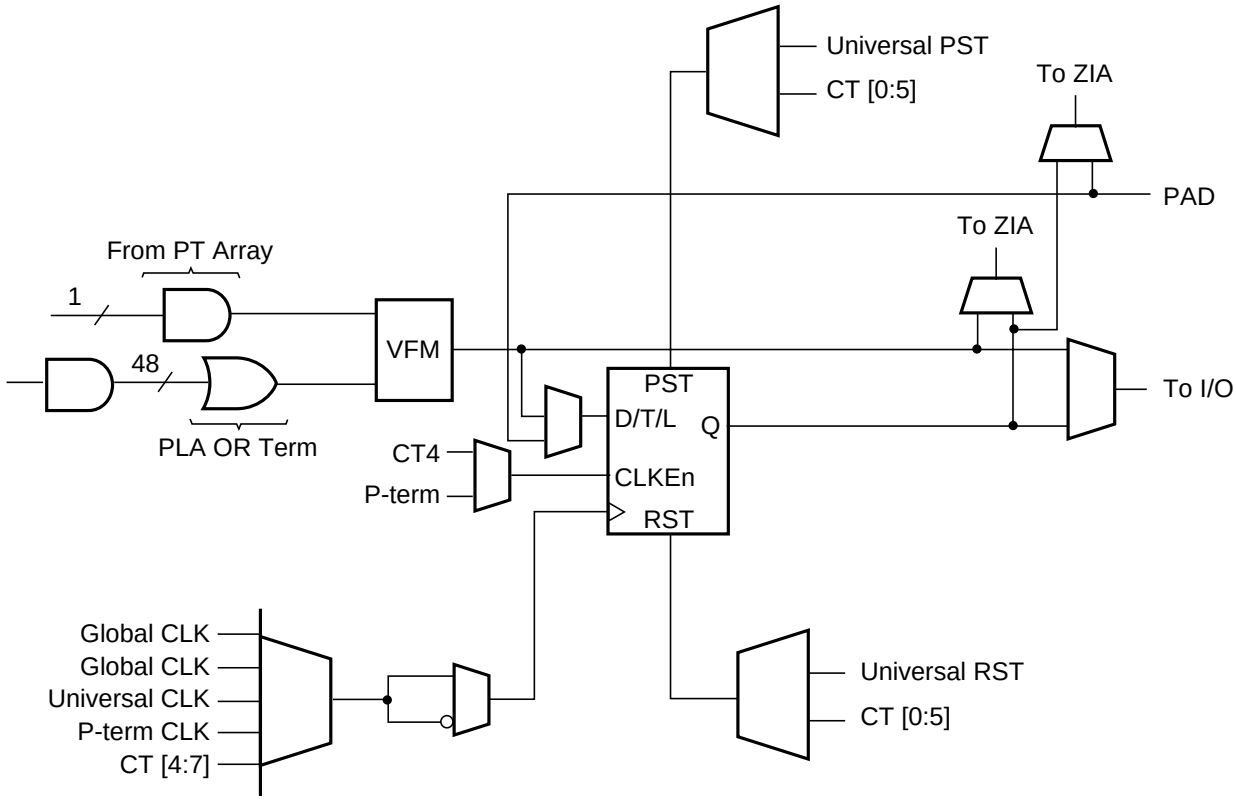
MC logic = PT1 # PT2 # PT3 # (PT4) &(A # B # C)

Macrocell Architecture

Figure 5 shows the architecture of the macrocell used in the CoolRunner XPLA3. Any macrocell can be reset or preset on power-up. Each macrocell register can be configured as a D-, T-, or Latch-type flip-flop, or combinatorial logic function. Each of these flip-flops can be clocked from any one of eight sources. There are two global synchronous clocks that are derived from the four external clock pins. There is one universal clock signal. The clock input signals CT[4:7] (Local Control Terms) can be individually configured as either a PRODUCT term or SUM term equation created from the 36 signals available inside the logic block..

There are two feedback paths to the ZIA: one from the macrocell, and one from the I/O pin. When the I/O pin is used as an output, the output buffer is enabled, and the macrocell feedback path can be used to feed back the logic implemented in the macrocell. When an I/O pin is used as an input, the output buffer will be 3-stated and the input signal will be fed into the ZIA via the I/O feedback path. The logic implemented in the buried macrocell can be fed back to the ZIA via the macrocell feedback path.

If the macrocell is configured as an input, there is a path to the register to provide a fast input setup time.



Note: Global CLK signals come from pins.

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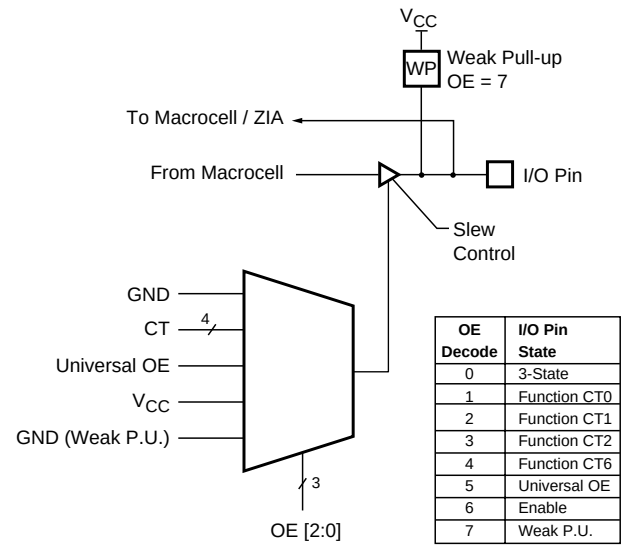
Figure 5: XPLA3 Macrocell Architecture

I/O Cell

The OE (Output Enable) multiplexer has eight possible modes (Figure 6), including a programmable weak pull-up (WPU) eliminating the need for external termination on unused I/Os.

The I/O Cell is 5V tolerant, and has a single-bit slew-rate control for reducing EMI generation.

Outputs are 3.3V PCI electrical specification compatible (no internal clamp diode).



OE Decode	I/O Pin State
0	3-State
1	Function CT0
2	Function CT1
3	Function CT2
4	Function CT6
5	Universal OE
6	Enable
7	Weak P.U.

ds012_06_121699

Figure 6: I/O Cell

Simple Timing Model

Figure 7 shows the XPLA3 timing model which has three main timing parameters, including T_{PD}, T_{SU}, and T_{CO}. In other architectures, the user may be able to fit the design into the CPLD, but may not be sure whether system timing requirements can be met until after the design has been fit into the device. This is because the timing models of other architectures are very complex and include such things as timing dependencies on the number of parallel expanders borrowed, sharable expanders, varying number of X and Y routing channels used, etc. In the XPLA3 architecture, the user knows up front whether the design will meet system timing requirements. This is due to the simplicity of the timing model.

Slew Rate Control

XPLA3 devices have slew rate control for each macrocell output pin. The user has the option to enable the slew rate control to reduce EMI. The nominal delay for using this option is 2.0 ns.

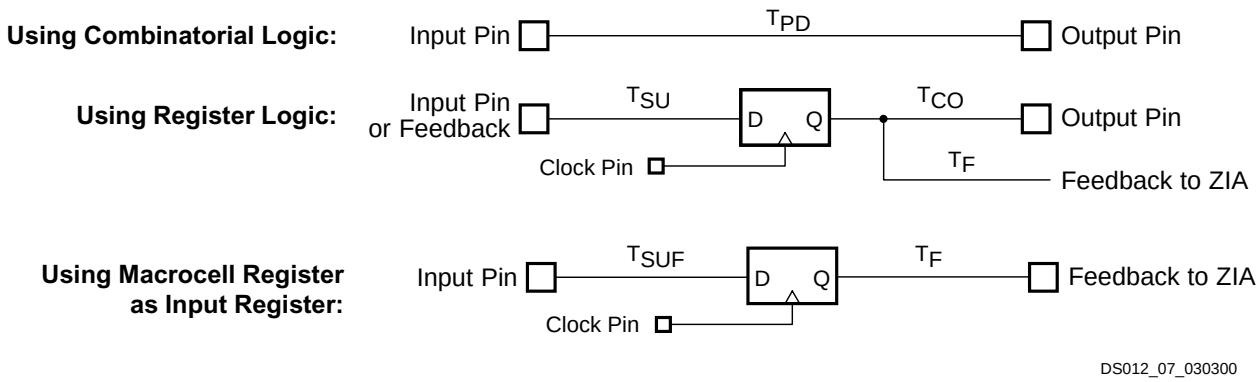


Figure 7: XPLA3 Timing Model

JTAG Testing Capability

JTAG is the commonly used acronym for the Boundary Scan Test (BST) feature defined for integrated circuits by IEEE Standard 1149.1. This standard defines input/output pins, logic control functions, and commands that facilitate both board and device level testing without the use of specialized test equipment. XPLA3 devices use the JTAG Interface for In-System Programming/Reprogramming. The full JTAG command set is implemented (see Table 1), including the use of a port enable signal.

As implemented in XPLA3, the JTAG Port includes four of the five pins (refer to Table 2) described in the JTAG specification: TCK, TMS, TDI, and TDO. The fifth signal defined by the JTAG specification is TRST (Test Reset). TRST is considered an optional signal, since it is not actually required to perform BST or ISP. The XPLA3 saves an I/O pin for general purpose use by not implementing the optional TRST signal in the JTAG interface. Instead, the XPLA3 supports the test reset functionality through the use of its power-up reset circuit, which is included in all CoolRunner CPLDs. It should be noted that the pins associated with the JTAG Port should connect to an external pull-up resistor (typical 10K) to keep the JTAG signals from floating when they are not being used.

The Port Enable pin is used to reclaim TMS, TDO, TDI, and TCK for JTAG ISP programming if the user has defined these pins as general purpose I/O during device programming. For ease of use, XPLA3 devices are shipped with the JTAG port pins enabled. Please note that the Port Enable pin must be low logic level during the power-up sequence for the device to operate properly.

During device programming, the JTAG ISP pins can be left as is or reconfigured as user specific I/O pins. If the JTAG ISP pins have been used for I/O pins, simply applying high logic level to the Port Enable pin converts the JTAG ISP pins back to their respective programming function and the device can be reprogrammed. After completing the desired JTAG ISP programming function, simply return Port Enable to Ground. This will re-establish the JTAG ISP pins to their respective I/O function. Note that reconfiguring the JTAG port pins as I/Os makes these pins non-JTAG ISP functional.

The XPLA3 family allows the macrocells associated with these pins to be used as buried logic when the JTAG/ISP function is enabled.

Table 1: XPLA3 Low-level JTAG Boundary-scan Commands

Instruction (Instruction Code) Register Used	Description
Sample/Preload (00010) Boundary-scan Register	The mandatory Sample/Preload instruction allows a snapshot of the normal operation of the component to be taken and examined. It also allows data values to be loaded into the latched parallel outputs of the Boundary-scan Shift Register prior to selection of the other boundary-scan test instructions.
Extest (00000) Boundary-scan Register	The mandatory Extest instruction allows testing of off-chip circuitry and board level interconnections. Data would typically be loaded onto the latched parallel outputs of Boundary-scan Shift Register using the Sample/Preload instruction prior to selection of the Extest instruction.
Bypass (11111) Bypass Register	Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through the selected device to adjacent devices during normal device operation. The Bypass instruction can be entered by holding TDI at a constant high value and completing an Instruction-scan cycle.
Idcode (00001) Boundary-scan Register	Selects the Idcode register and places it between TDI and TDO, allowing the Idcode to be serially shifted out of TDO. The Idcode instruction permits blind interrogation of the components assembled onto a printed circuit board. Thus, in circumstances where the component population may vary, it is possible to determine what components exist in a product.
High-Z (00101) Bypass Register	The High-Z instruction places the component in a state which all of its system logic outputs are placed in an inactive drive state (e.g., high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component. The High-Z instruction also forces the Bypass Register between TDI and TDO
Intest (00011) Boundary-scan Register	The Intest instruction selects the boundary scan register preparatory to applying tests to the logic core of the device. This permits testing of on-chip system logic while the component is already on the board

Table 2: JTAG Pin Description

Pin	Name	Description
TCK	Test Clock Input	Clock pin to shift the serial data and instructions in and out of the TDI and TDO pins, respectively.
TMS	Test Mode Select	Serial input pin selects the JTAG instruction mode. TMS should be driven high during user mode operation.
TDI	Test Data Input	Serial input pin for instructions and test data. Data is shifted in on the rising edge of TCK.
TDO	Test Data Output	Serial output pin for instructions and test data. Data is shifted out on the falling edge of TCK. The signal is 3-stated if data is not being shifted out of the device.

3V, In-System Programming (ISP)

ISP is the ability to reconfigure the logic and functionality of a device, printed circuit board, or complete electronic system before, during, and after its manufacture and shipment to the end customer. ISP provides substantial benefits in each of the following areas:

- Design
  - Faster time-to-market
  - Debug partitioning and simplified prototyping
  - Printed circuit board reconfiguration during debug
  - Better device and board level testing
- Manufacturing
  - Multi-functional hardware
  - Reconfigurability for Test
  - Eliminates handling of "fine lead-pitch" components for programming
- Field Support
  - Easy remote upgrades and repair
  - Support for field configuration, reconfiguration, and customization

XPLA3 allows for 3V, in-system programming/reprogramming of its EEPROM cells via a JTAG interface. An on-chip charge pump eliminates the need for externally provided super-voltages. This allows programming on the circuit board using only the 3V supply required by the device for normal operation. The ISP commands implemented in XPLA3 are specified in Table 3.

Table 3: Low -level ISP Commands

Instruction (Register Used)	Instruction Code	Description
Enable (ISP Shift Register)	01001	Enables the Erase, Program, and Verify commands. Using the Enable instruction before the Erase, Program, and Verify instructions allows the user to specify the outputs of the device using the JTAG Boundary-Scan Sample/Preload command.
Erase (ISP Shift Register)	01010	Erases the entire EEPROM array. User can define the outputs during this operation by using the JTAG Sample/Preload command.
Program (ISP Shift Register)	01011	Programs the data in the ISP Shift Register into the addressed EEPROM row. The outputs can be defined by using the JTAG Sample/Preload command.
Disable (ISP Shift Register)	10000	Disable instruction allows the user to leave ISP mode. It selects the ISP register to be directly connected between TDO and TDI.
Verify (ISP Shift Register)	01100	Transfers the data from the addressed row to the ISP Shift Register. The data can then be shifted out and compared with the JEDEC file. The user can define the outputs during this operation.

Terminations

The CoolRunner XPLA3 CPLDs are TotalCMOS devices. As with other CMOS devices, it is important to consider how to properly terminate unused inputs and I/O pins when fabricating a PC board. Allowing unused inputs and I/O pins to float can cause the voltage to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. The XPLA3 CPLDs have programmable on-chip weak pull-up resistors on each I/O pin. These resistors are automatically activated by fitter software for all unused I/O pins. Note that an I/O macrocell used as buried logic that does not have the I/O pin used for input is considered to be unused, and the weak pull-up resistors will be turned on. It is recommended that any unused I/O pins on the XPLA3 family of CPLDs be left unconnected. As with all CMOS devices, do not allow inputs to float.

JTAG and ISP Interfacing

A number of industry-established methods exist for JTAG/ISP interfacing with CPLDs and other integrated circuits. The XPLA3 family supports the following methods:

- Xilinx HW 130
- PC Parallel Port
- Workstation or PC Serial Port
- Embedded Processor
- Automated Test Equipment
- Third Party Programmers
- Xilinx ISP Programming Tools

For more details on JTAG and ISP, refer to the related application note: *JTAG and ISP in Xilinx CPLDs*. see also Table 4 below:

Table 4: Programming Specifications

Symbol	Parameter	Min.	Max.	Unit
DC Parameters				
V_{CCP}	V_{CC} supply program/verify	3.0 (com) 2.7 (ind)	3.6	V
I_{CCP}	I_{CC} limit program/verify		80	mA
V_{IH}	Input voltage (High)	2.0		V
V_{IL}	Input voltage (Low)		0.8	V
V_{OL}	Output voltage (Low)		0.4	V
V_{OH}	Output voltage (High)	2.4		V
AC Parameters				
F_{MAX}	TCK maximum frequency		10	MHz
P_{WE}	Pulse width erase	100		ms
P_{WP}	Pulse width program	10		ms
P_{WV}	Pulse width verify	10		µs
T_{INIT}	Initialization time	50		µs
T_{MS_SU}	TMS setup time before TCK ↑	10		ns
T_{DI_SU}	TDI setup time before TCK ↑	10		ns
T_{MS_H}	TMS hold time after TCK ↑	20		ns
T_{DI_H}	TDI hold time after TCK ↑	20		ns
T_{DO_CO}	TDO valid after TCK ↓		30	ns

Absolute Maximum Ratings(1)

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage(2) relative to GND	–0.5	3.6	V
V_I	Input voltage(3) relative to GND	–0.5	5.5	V
I_{OUT}	Output current	–100	100	mA
T_J	Maximum junction temperature	–40	150	°C
T_{STR}	Storage temperature	–65	150	°C

Notes:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.
2. The chip supply voltage must rise monotonically.
3. Maximum DC undershoot below GND must be limited to either 0.5V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to –2.0V or overshoot to 7.0V, provided this over- or undershoot lasts less than 10 ns and with the forcing current being limited to 200 mA.
4. External I/O voltage may not be applied for more than 100 milliseconds without the presence of V_{CC}.

Recommended Operation Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{CC}	Supply voltage f	Commercial T_A = 0°C to 70°C	3.0	3.6	V
		Industrial T_A = –40°C to +85°C	2.7	3.6	V
V_{IL}	Low-level input voltage		0	0.8	V
V_{IH}	High-level input voltage		2.0	5.5	V
V_O	Output voltage		0	V_{CC}	V
T_R	Input rise time			20	ns
T_F	Input fall time			20	ns

Quality and Reliability Characteristics

Symbol	Parameter	Min	Max	Units
T_{DR}	Data retention	20	-	Years
N_{PE}	Program/Erase Cycles (Endurance)	1,000	-	Cycles
V_{ESD}	Electrostatic Discharge (ESD)	2,000	-	Volts

Device Families

Parameter	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL
Macrocells	32	64	128	256	384
Usable gates	750	1,500	3,000	6,000	9,000
Registers	32	64	128	256	384
I/Os	32	64	104	160	216
T_{PD} (ns)	5.0	6.0	6.0	7.5	7.5
T_{SUF} (ns)	TBD	TBD	TBD	2.0	TBD
T_{CO} (ns)	4.0	4.0	4.5	4.5	5.0
F_{SYSTEM} (MHz)	200	167	167	140	TBD
	Preliminary Information				

Available Packages

Package Type	XCR3032XL	XCR3064XL	XCR3128XL	XCR3256XL	XCR3384XL
CS280				160 I/O	216 I/O
PQ208				160 I/O	
TQ144			104 I/O	116 I/O	
CS144			104 I/O		
VQ100		64 I/O	80 I/O		
CP56		44 I/O			
CS48	32 I/O	32 I/O(1)			
VQ44	32 I/O	32 I/O			
	Preliminary Information				

Note:
1. Future package.

Revision Table

Date	Version #	Revision
01/20/2000	1.0	Initial Xilinx release.
03/03/00	1.1	Minor update.

7

XCR3384XL: 384 Macrocell CPLD

DS014 (v1.0) February 7, 2000 Advance Product Specification

Features

- 7.5 ns pin-to-pin logic delays
- System frequencies up to 120 MHz
- 384 macrocells with 9,000 usable gates
- Available in small footprint packages
  - 280-pin CS BGA (216 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3384XL is a 3.3V, 384 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 9,000 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 120 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS™ CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance.

XCR3256XL: 256 Macrocell CPLD

DS013 (v1.0) February 7, 2000 Preliminary Product Specification

Features

- 7.5 ns pin-to-pin logic delays
- System frequencies up to 140 MHz
- 256 macrocells with 6,000 usable gates
- Available in small footprint packages
  - 144-pin TQFP (116 user I/O pins)
  - 208-pin PQFP (160 user I/O)
  - 280-pin CS BGA (160 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3256XL is a 3.3V, 256 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 6,000 usable gates. Pin-to-pin propagation delays are 7.5 ns with a maximum system frequency of 140 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS™ CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance.

XCR3128XL 128 Macrocell CPLD

DS016 (v1.0) January 21, 2000 Advance Product Specification

Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to 167 MHz
- 128 macrocells with 3,000 usable gates
- Available in small footprint packages
  - 144-pin TQFP (104 user I/O pins)
  - 144-pin CS BGA (104 user I/O)
  - 100-pin VQFP (80 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per macrocell
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3128XL is a 3.3V 128 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 3,000 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 167 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS™ CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance.

XCR3064XL: 64 Macrocell CPLD

DS017 (v1.0) February 7, 2000 Advance Product Specification

Features

- 6.0 ns pin-to-pin logic delays
- System frequencies up to167 MHz
- 64 macrocells with 1,500 usable gates
- Available in small footprint packages
  - 100-pin TQFP (64 user I/O pins)
  - 44-pin VQFP (32 user I/O)
  - 48-ball CS (32 user I/O)
  - 56-ball CS (44 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with supply with 3.3V core supply
  - Advanced 0.35 micron five metal layer EE process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 available clocks per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - 16 product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3064XL is a 3.3V, 64 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 1,500 usable gates. Pin-to-pin propagation delays are 6.0 ns with a maximum system frequency of 167 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMO™ CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance.

XCR3032XL: 32 Macrocell CPLD

DS015 (v1.0) February 7, 2000 Advance Product Specification

Features

- 5.0 ns pin-to-pin logic delays
- System frequencies up to 200 MHz
- 32 macrocells with 750 usable gates
- Available in small footprint packages
  - 44-pin VQFP (32 user I/O)
  - 48-ball CS BGA (32 user I/O)
- Optimized for 3.3V systems
  - Ultra low power operation
  - 5V tolerant I/O pins with 3.3V core supply
  - Advanced 0.35 micron five metal layer re-programmable process
  - FZP™ CMOS design technology
- Advanced system features
  - In-system programming
  - Input registers
  - Predictable timing model
  - Up to 23 clocks available per logic block
  - Excellent pin retention during design changes
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
  - Four global clocks
  - Eight product term control terms per logic block
- Fast ISP programming times
- Port Enable pin for additional I/O
- 2.7V to 3.6V industrial grade voltage range
- Programmable slew rate control per output
- Security bit prevents unauthorized access
- Refer to family data sheet for architecture description

Description

The XCR3032XL is a 3.3V, 32 macrocell CPLD targeted at power sensitive designs that require leading edge programmable logic solutions. A total of 16 logic blocks provide 750 usable gates. Pin-to-pin propagation delays are 5.0 ns with a maximum system frequency of 200 MHz.

TotalCMOS™ Design Technique for Fast Zero Power

Xilinx offers a TotalCMOS™ CPLD, both in process technology and design technique. Xilinx employs a cascade of CMOS gates to implement its Sum of Products instead of the traditional sense amp approach. This CMOS gate implementation allows Xilinx to offer CPLDs that are both high performance and low power, breaking the paradigm that to have low power, you must have low performance.

FastFLASH™ XC9500XV High-Performance, Low-Power CPLD Family

DS049 (v1.1) February 1, 2000

Advance Product Information

Features

- Optimized for high-performance 2.5V systems
  - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
  - Lower power operation
  - Multi-voltage operation
  - FastFLASH technology
- Advanced system features
  - In-system programmable
  - Output banking
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 10,000 program/erase cycles endurance rating
  - 20 year data retention
- Pin-compatible with 3.3V core XC9500XL family in common package footprints
- Hot Plugging capability

Family Overview

The FastFLASH XC9500XV family is a 2.5V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XV device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XV family is designed to work closely with the Xilinx Spartan-XL and Virtex FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in Table 1, logic density of the XC9500XV devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500XV family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XV architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 3.3V, 2.5V, 1.8V, and 1.5V inputs, and the outputs may be configured for 3.3V, 2.5V, or 1.8V operation. The XC9500XV device exhibits symmetric full 2.5V output voltage swing to allow balanced rise and fall times.

Architecture Description

Each XC9500XV device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54 inputs and 18 outputs. The FastCONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1.

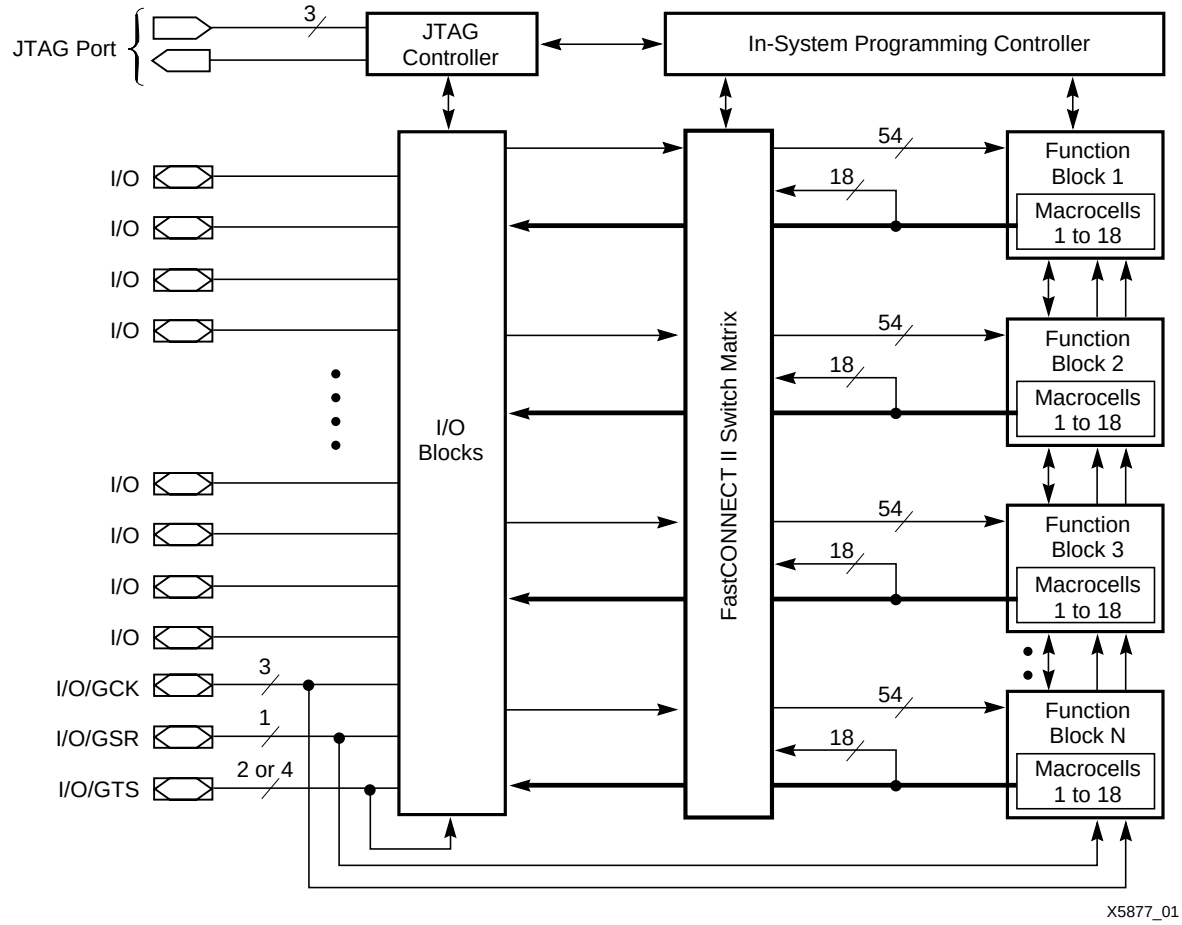


Figure 1: XC9500XV Architecture

Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

Table 1: XC9500XV Device Family

	XC9536XV	XC9572XV	XC95144XV	XC95288XV
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
t_{PD} (ns)	4	5	5	6
t_{SU} (ns)	3	3.7	3.7	4.1
t_{CO} (ns)	3	3.5	3.5	4.3
f_{SYSTEM} (MHz)	200	178	178	151

Table 2: XC9500XV Packages and User I/O Pins (not including four dedicated JTAG pins

	XC9536XV	XC9572XV	XC95144XV	XC95288XV
44-Pin PLCC	34	34		
64-Pin VQFP	36	52		
100-Pin TQFP		72	81	
144-Pin TQFP			117	117
208-Pin PQFP				168
48-Pin CSP	36	38		
144-Pin CSP			117	
256-Pin BGA				192
256-Pin FBGA				192

Function Block

Each Function Block, as shown in Figure 2 is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT II switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Fifty-four inputs provide 108 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

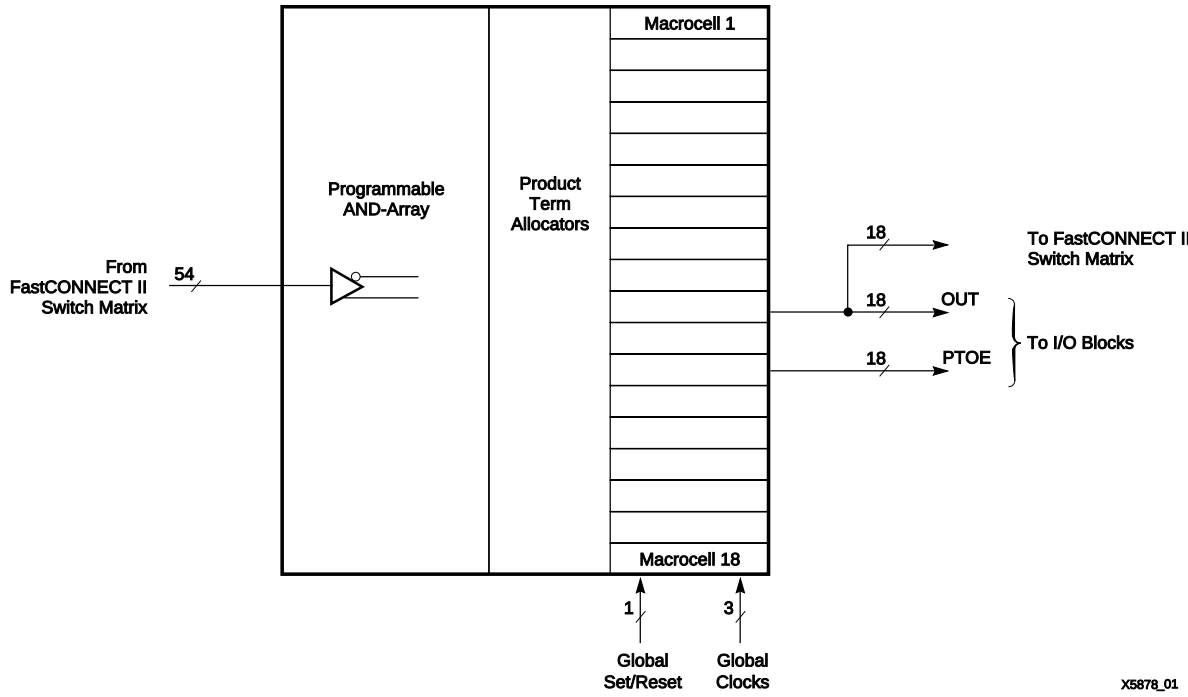


Figure 2: XC9500XV Function Block

Macrocell

Each XC9500XV macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, clock enable, set/reset, and output enable.

The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

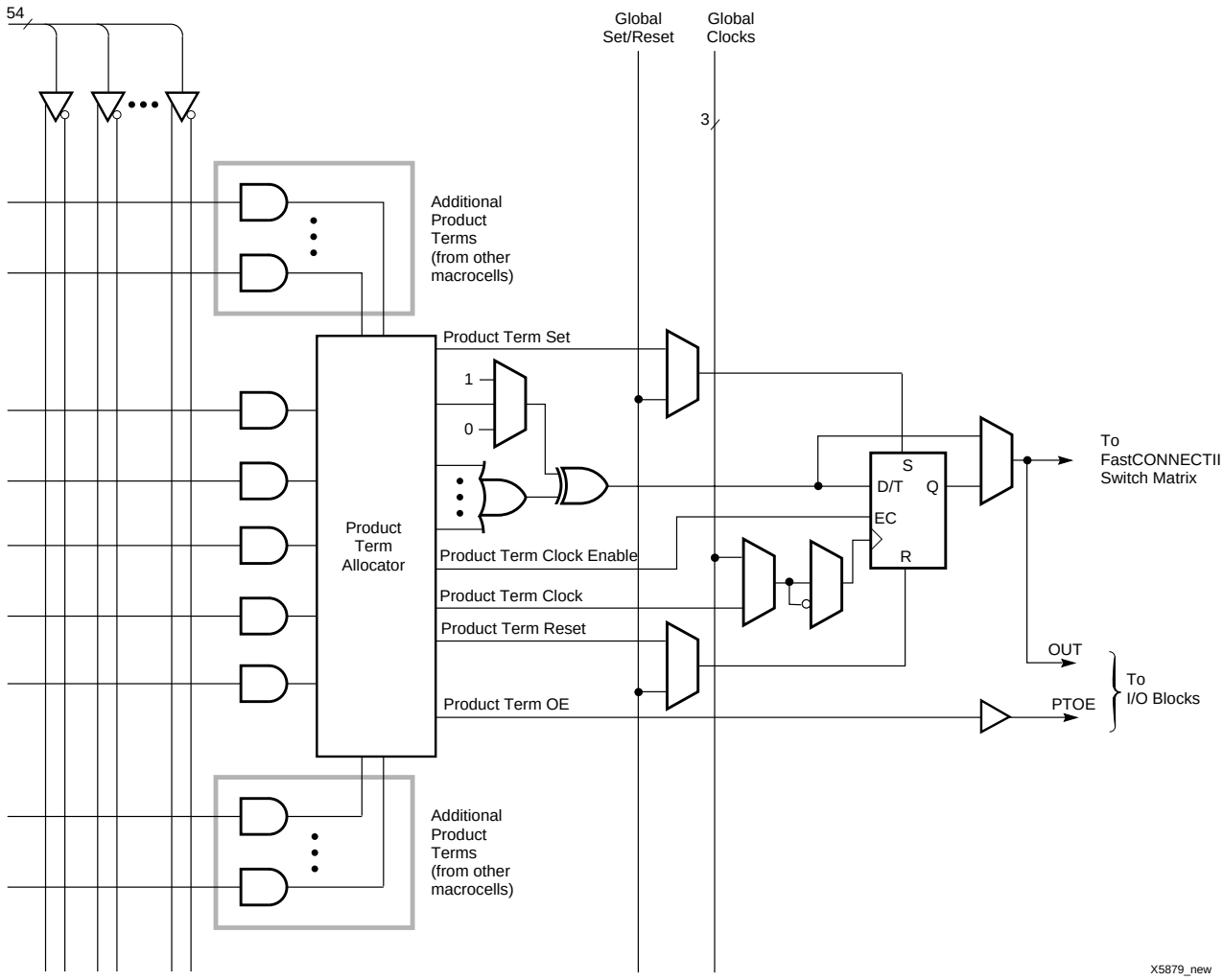


Figure 3: XC9500XV Macrocell Within Function Block

Note: See Figure 8 for additional clock enable details.

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of the selected clock source can be used within each macrocell. A GSR input is also provided to allow user registers to be set to a user-defined state.

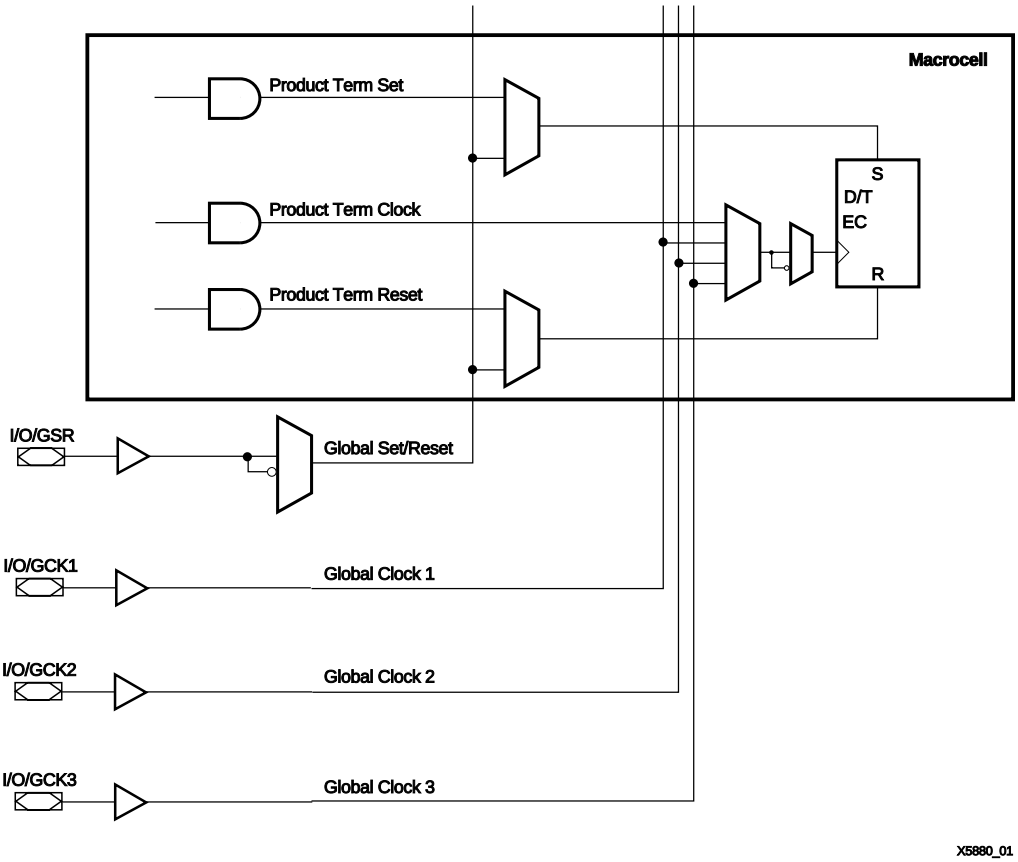


Figure 4: Macrocell Clock and Set/Reset Capability

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

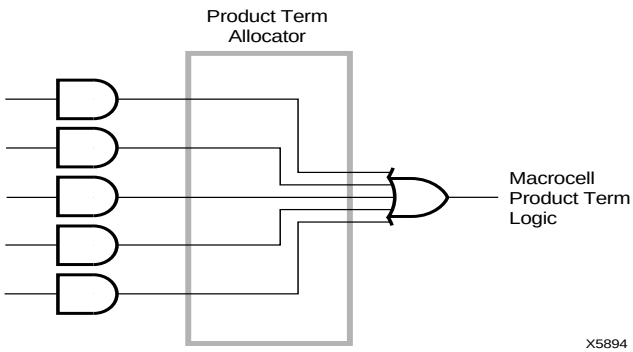


Figure 5: Macrocell Logic Using Direct Product Term

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of $t_{PTA,}$ as shown in Figure 6.

Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed.

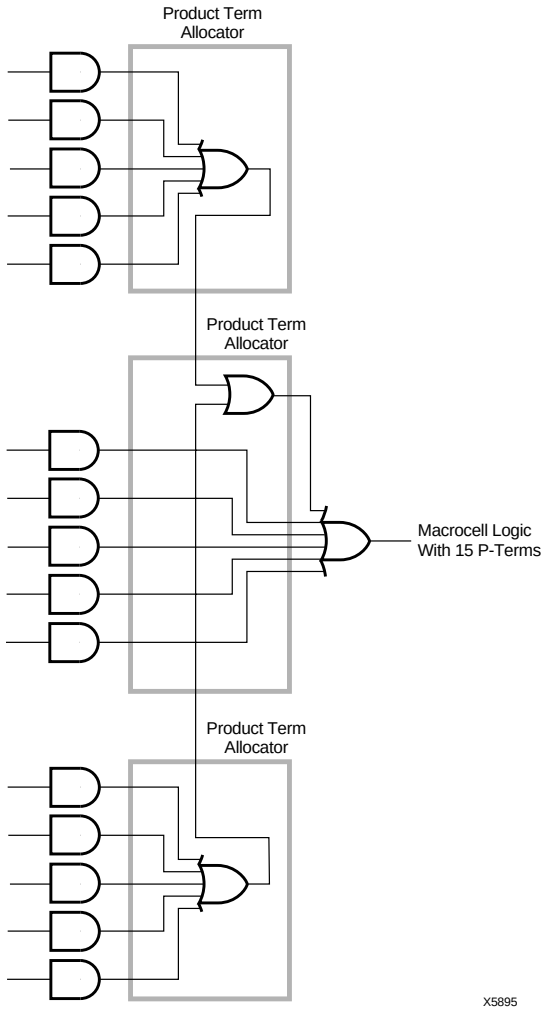


Figure 6: Product Term Allocation With 15 Product Terms

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7. In this example, the incremental delay is only $2*t_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8*t_{PTA}$.

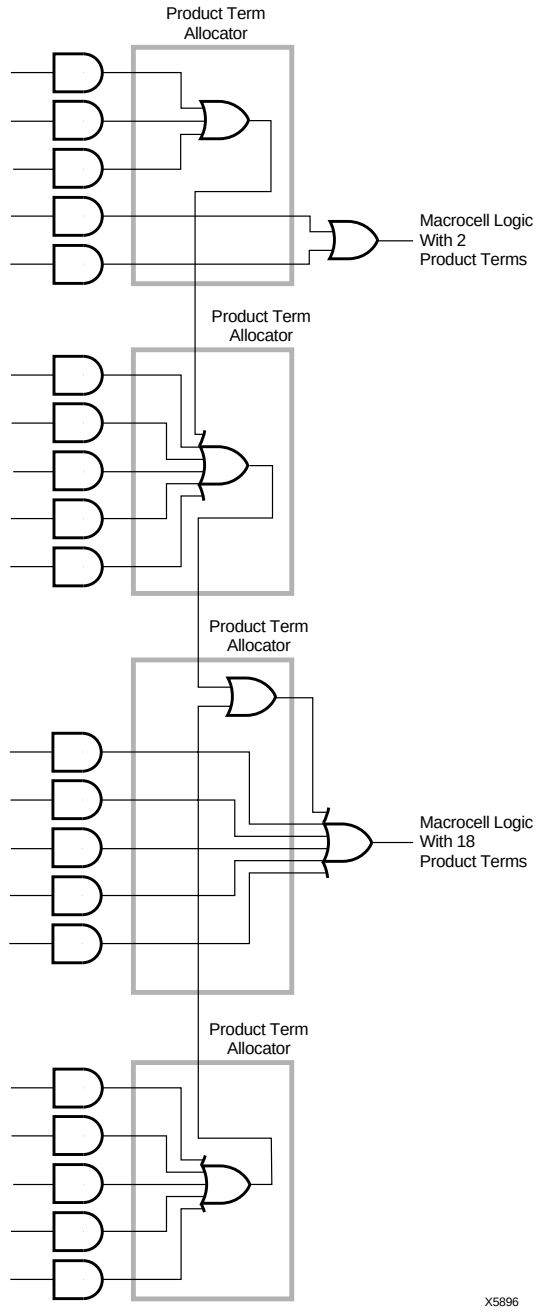


Figure 7: Product Term Allocation Over Several Macrocells

The internal logic of the product term allocator is shown in Figure 8.

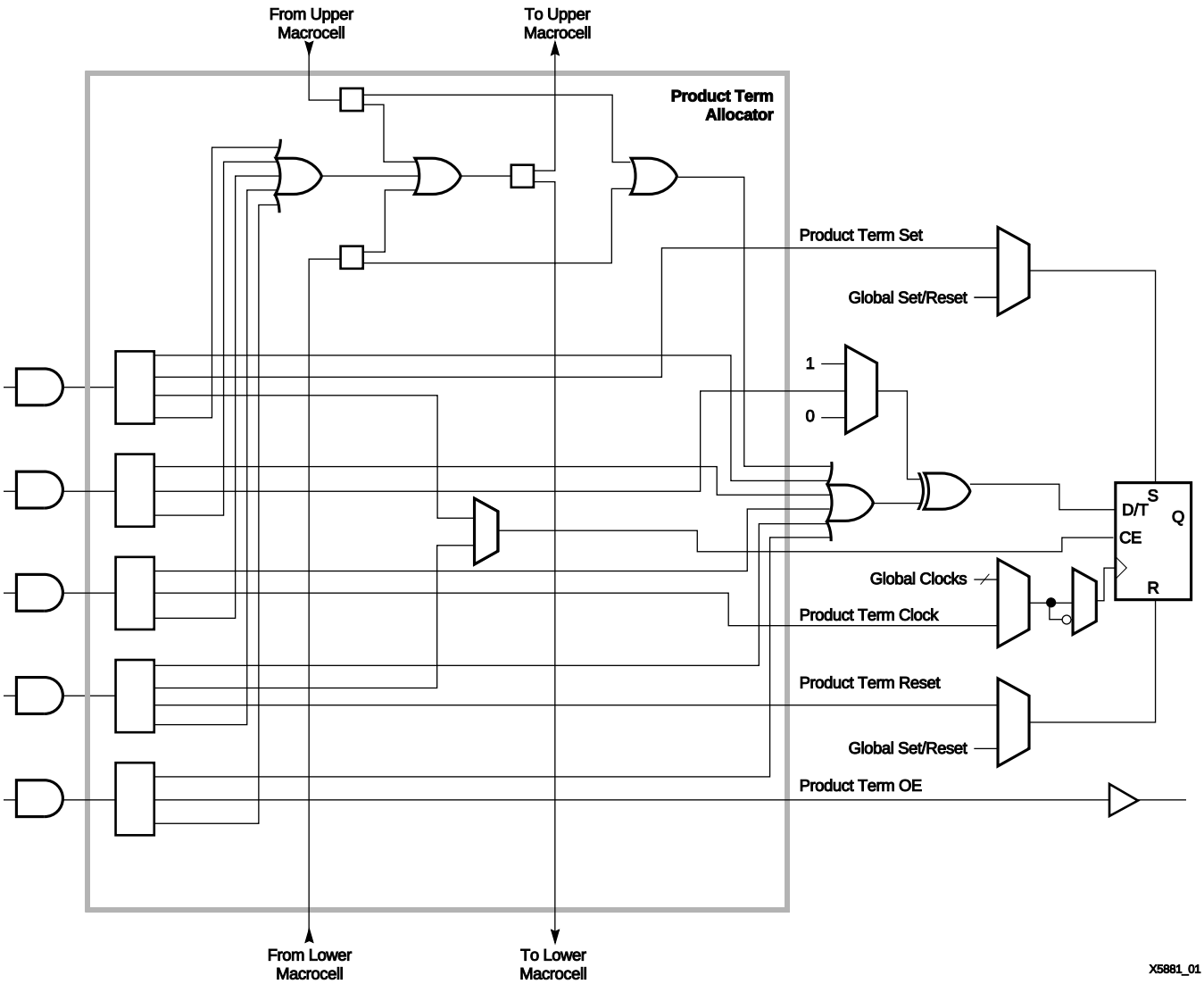


Figure 8: Product Term Allocator Logic

FastCONNECT II Switch Matrix

The FastCONNECT II Switch Matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT II matrix. Any of these (up to a fan-in limit of 54) may be selected to drive each FB with a uniform delay.

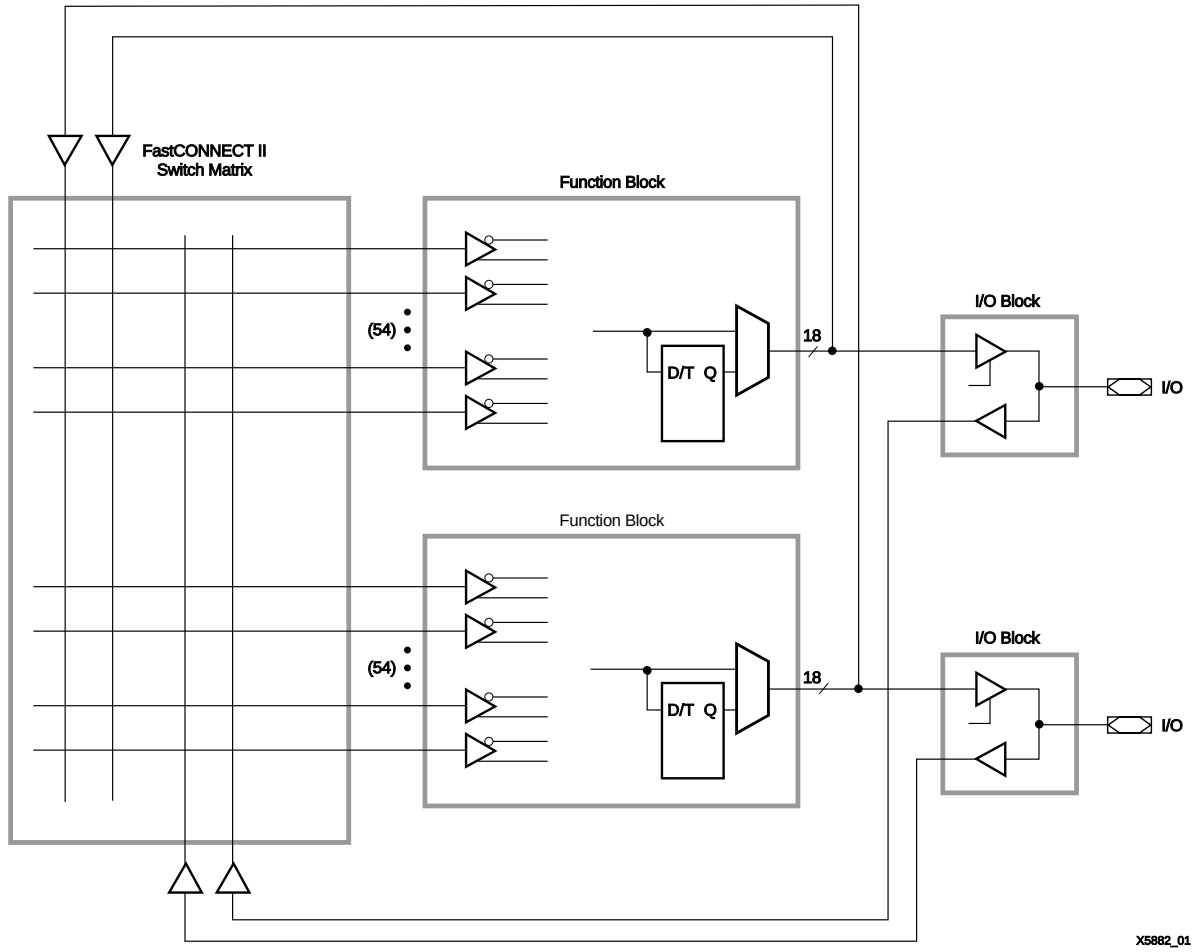


Figure 9: FastCONNECT II Switch Matrix

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

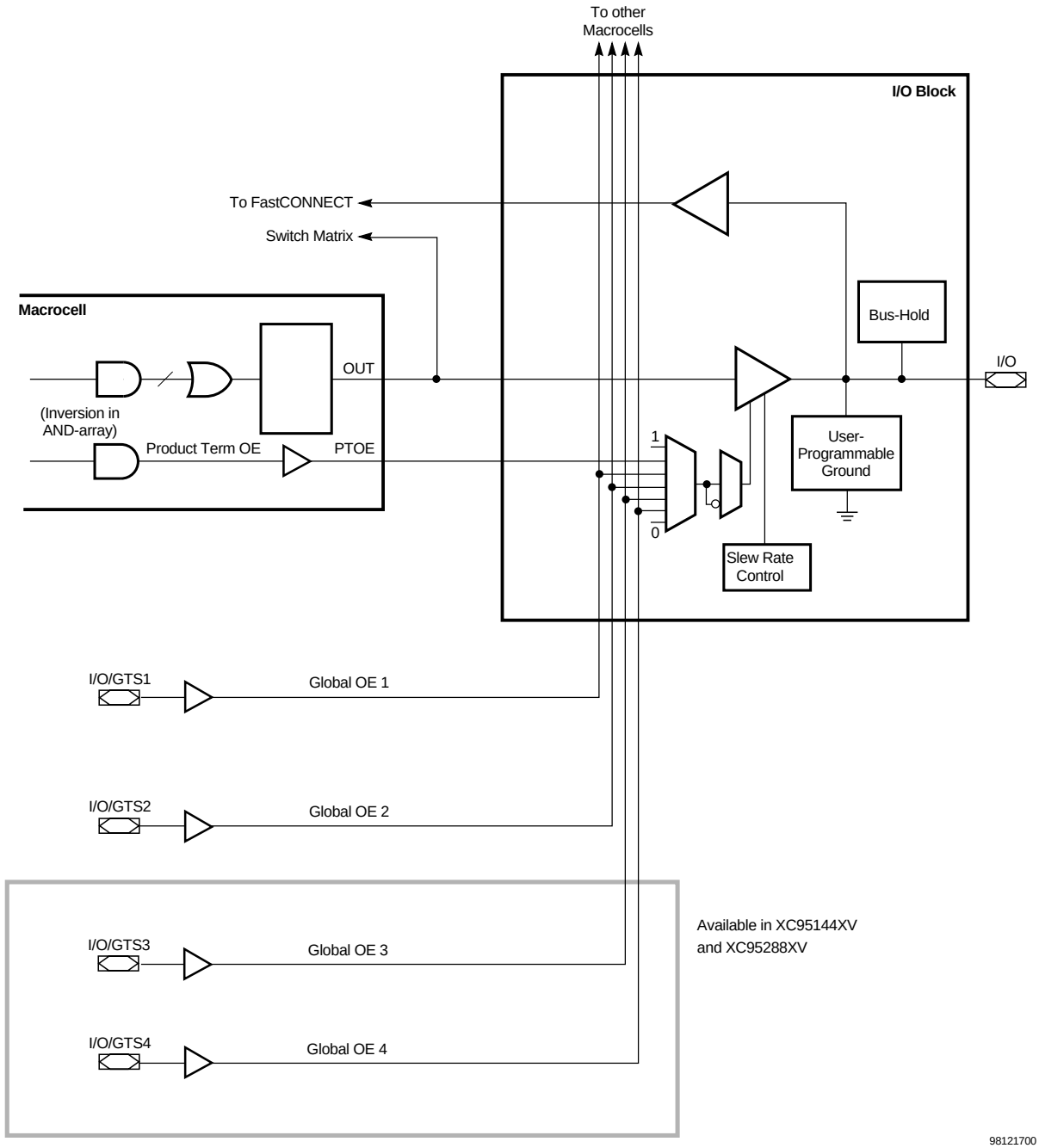


Figure 10: I/O Block and Output Enable Capability

The input buffer is compatible with 3.3V CMOS, 2.5V CMOS, and 1.8V CMOS signals. The input buffer uses the internal 2.5V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage. Each input buffer provides input hysteresis (50 mV typical) to help reduce system noise for input signals with slow rise or fall edges.

Each output driver is designed to provide fast switching with minimal power noise. All output drivers in the device may be configured for driving either 3.3V, 2.5V, or 1.8V CMOS

levels by connecting the device output voltage supply (V_{CCIO}) to a 3.3V, 2.5V, or 1.8V voltage supply. Figure 11 shows how the XC9500XV device can be used in 2.5V only.

Each output driver can also be configured for slew-rate limited operation. Output edge rates may be slowed down to reduce system noise (with an additional time delay of t_{SLEW}) under user control. See Figure 12.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global output enable signals (GTS), always “1,” or always “0.” There are two global output enables for devices with 72 or fewer macrocells, and four global output enables for devices with 144 or more macrocells. Any selected output enable signal may be inverted locally at each pin output to provide maximal design flexibility.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins in order to force otherwise unused pins to a low voltage state, as well as provide for additional device grounding capability. This grounding of the pin is achieved by internal logic that forces a logic low output regardless of the internal macrocell signal, so the internal macrocell logic is unaffected by the programmable ground pin capability.

Each IOB also provides for bus-hold circuitry that is active during valid user operation. The bus-hold feature eliminates the need to tie unused pins either high or low by holding the last known state of the input until the next input signal is present. The bus-hold circuit drives back the same state via a nominal resistance (R_{BH}) of 50k ohms. See Figure 13.

Note: the bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals when interfacing to 2.5V components.

When the device is not in valid user operation, the bus-hold circuit defaults to an equivalent 50k ohm pull-up resistor in order to provide a known repeatable device state. This occurs when the device is in the erased state, in programming mode, in JTAG INTEST mode, or during initial power-up. A pull-down resistor (1k ohm) may be externally added to any pin to override the default R_{BH} resistance to force a low state during power-up or any of these other modes.

Output Banking

XC9500XV parts are designed with a split-rail I/O structure. This permits the utilization of two separate output drive levels for systems able to operate best in that environment. The output partitioning is by function blocks (FB) where all even numbered FBs are attached to one VCCO rail and the odd ones attached to the other one. With this arrangement, designers can have one set of outputs driving to 2.5V and another set to 1.8V. Naturally, it is possible to tie both rails to a single output voltage and get all outputs driving to that level. Should designs be migrated from one density to another in the same package, care should be taken to remember the voltage assignments chosen at the outset to assure consistency.

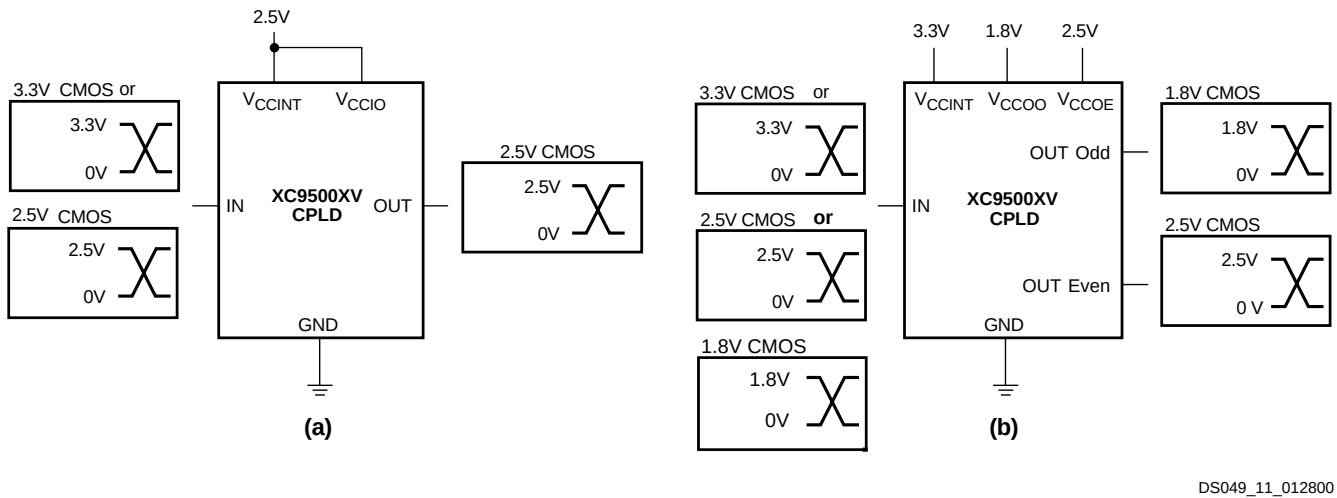


Figure 11: XC9500XV Devices in (a) 2.5V only and (b) Mixed 3.3V/2.5V/1.8V Systems

Mixed Voltage

The I/Os on each XC9500XV device are fully 3.3V tolerant even though the core power supply is 2.5 volts. This allows 3.3V CMOS signals to connect directly to the XC9500XV inputs without damage. In addition, the 2.5V V_{CCINT} power supply can be applied before or after 2.5V signals are applied to the I/Os. In mixed 3.3V/2.5V/1.8V systems, the user pins, the core power supply (V_{CCINT}), and the output power supply (V_{CCIO}) may have power applied in any order. This makes the XC9500XV devices immune to power supply sequencing problems.

Xilinx proprietary ESD circuitry and high impedance initial state permit hit plugging cards using XC9500XV CPLDs.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design iteration depends on the ability of the architecture to adapt to unexpected changes. The XC9500XV devices incorporate architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500XV architecture provides for superior pin-locking characteristics with a combination of large number of routing switches in the FastCONNECT II switch matrix, a 54-wide input Function Block, and flexible, bi-directional product term allocation within each macrocell. These features address design changes that require adding or changing internal routing, including additional signals into existing equations, or increasing equation complexity, respectively.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.

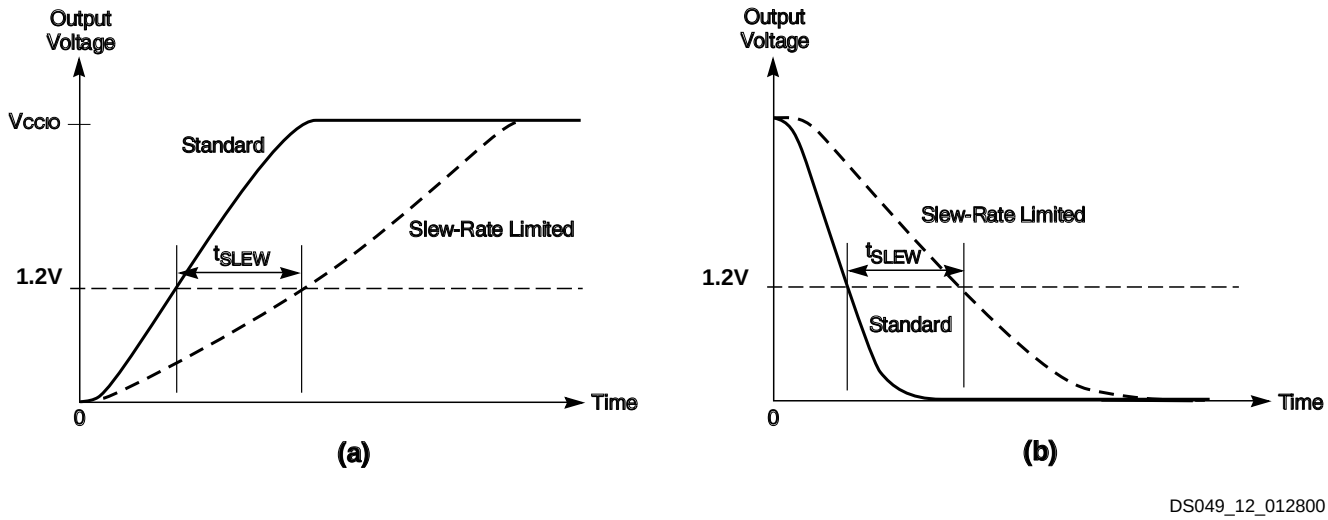


Figure 12: Output Slew-Rate Control For (a) Rising and (b) Falling Outputs

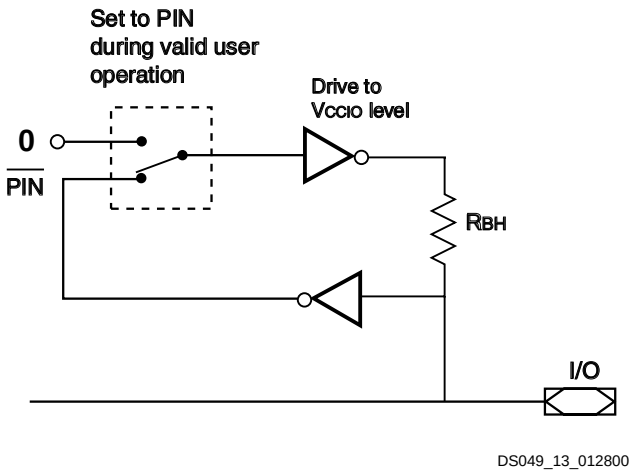


Figure 13: Bus-Hold Logic

In-System Programming

One or more XC9500XV devices can be daisy chained together and programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 14. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are 3-stated and pulled high by the bus-hold circuitry during in-system programming. If a particular signal must remain low during this time, then a pulldown resistor may be added to the pin.

Reliability and Endurance

All XC9500XV CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500XV devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, HIGHZ and CLAMP instructions are supported in each device. Additional instructions are included for in-system programming operations.

Design Security

XC9500XV devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. When set, they also inhibit further program operations but allow device erase. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern with a specific sequence of JTAG instructions.

Table 3: Data Security Options

		Read Security: Default	Read Security: Set
Write Security	Default	Read Allowed Program/Erase Allowed	Read Inhibited Program Inhibit Erase Allowed
	Set	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Inhibited

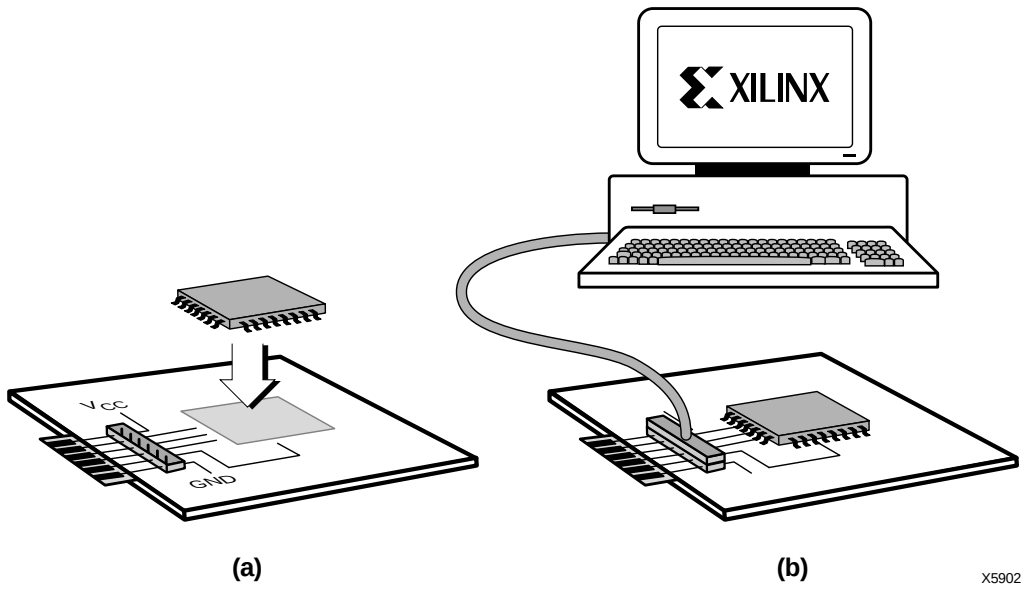


Figure 14: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

Low Power Mode

All XC9500XV devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (t_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500XV architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 15, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The example in Figure 6 shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

Detailed timing information may be derived from the full timing model shown in Figure 16. The values and explanations for each parameter are given in the individual device data sheets.

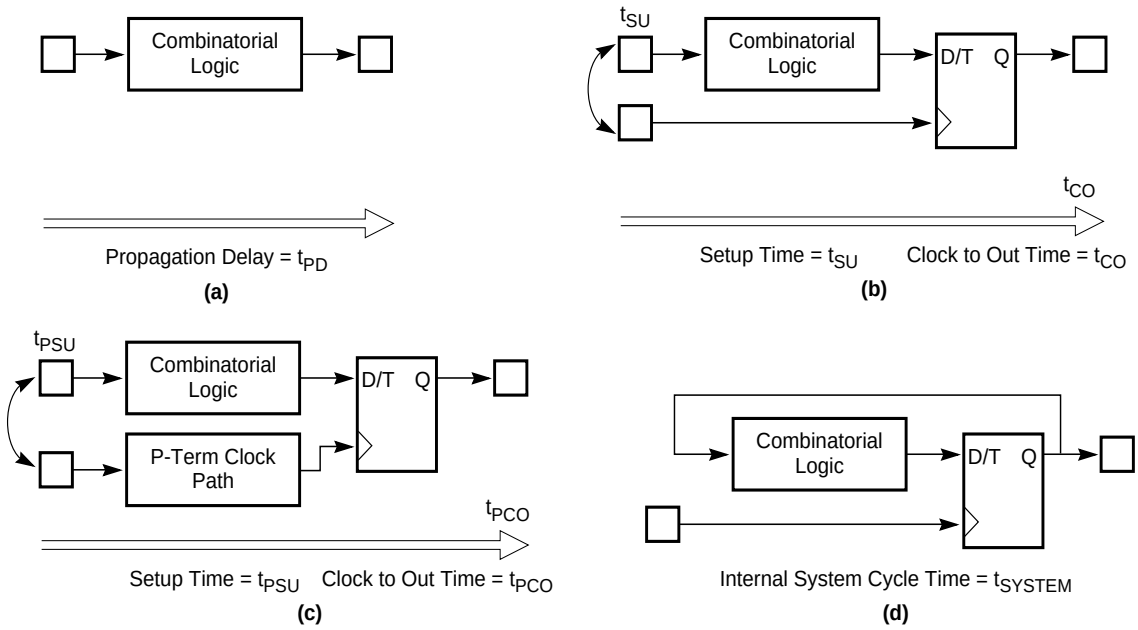


Figure 15: Basic Timing Model

Table 4: Timing Model Parameters

Description	Parameter	Product Term Allocator[1]	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	t_{PD}	+ t_{PTA} * S	+ t_{LP}	+ t_{SLEW}
Global Clock Setup Time	t_{SU}	+ t_{PTA} * S	+ t_{LP}	–
Global Clock-to-output	t_{CO}	–	–	+ t_{SLEW}
Product Term Clock Setup Time	t_{PSU}	+ t_{PTA} * S	+ t_{LP}	–
Product Term Clock-to-output	t_{PCO}	–	–	+ t_{SLEW}
Internal System Cycle Period	t_{SYSTEM}	+ t_{PTA} * S	+ t_{LP}	–

Note: 1. S = the logic span of the function, as defined in the text.

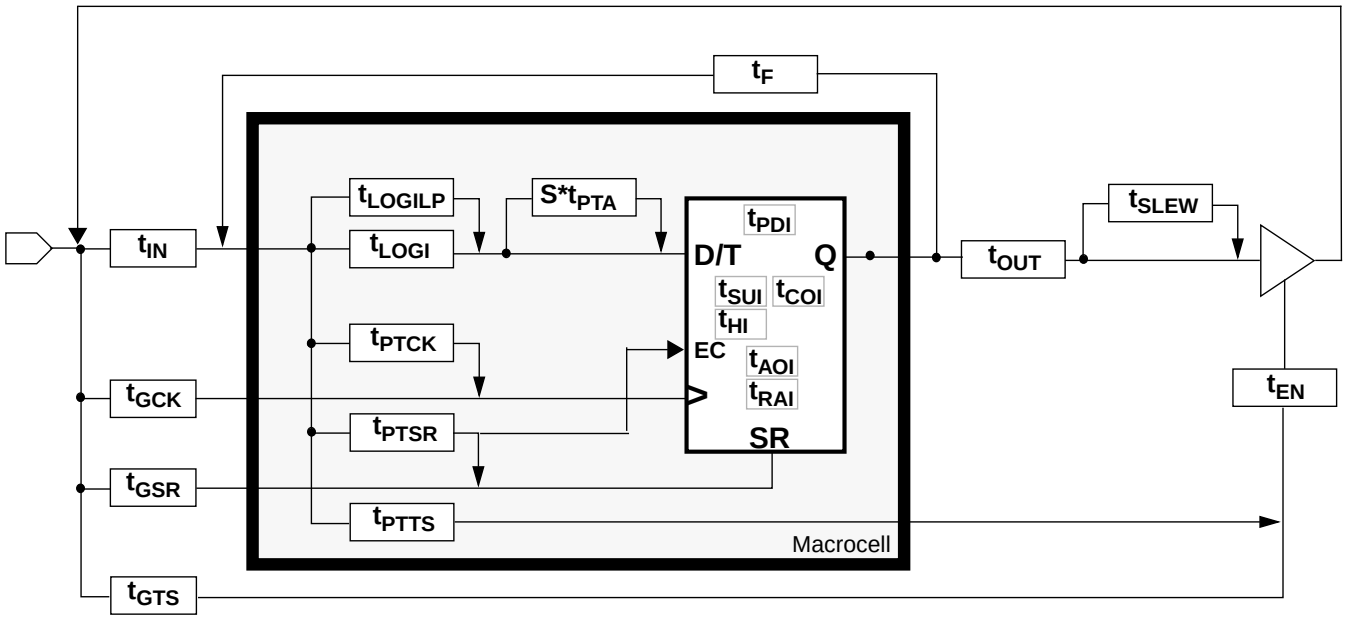


Figure 16: Detailed Timing Model

Power-Up Characteristics

The XC9500XV devices are well behaved under all operating conditions. During power-up each XC9500XV device employs internal circuitry which keeps the device in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 1.9V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the pins weakly pulled high, as shown in Table . When the supply voltage reaches a safe level, all user registers become initialized (typically within 300 µs), and the device is immediately available for operation, as shown in Figure 17.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

Development System Support

The XC9500XV family and associated in-system programming capabilities are fully supported in either software solutions available from Xilinx.

The Foundation Series is an all-in-one development system containing schematic entry, HDL (VHDL, Verilog, and ABEL), and simulation capabilities. It supports the XC9500XV family as well as other CPLD and FPGA families.

The Alliance Series includes CPLD and FPGA implementation technology as well as all necessary libraries and interfaces for Alliance partner EDA solutions.

FastFLASH Technology

An advanced CMOS Flash process is used to fabricate all XC9500XV devices. The FastFLASH process provides high performance logic capability, fast programming times, and superior reliability and endurance ratings.

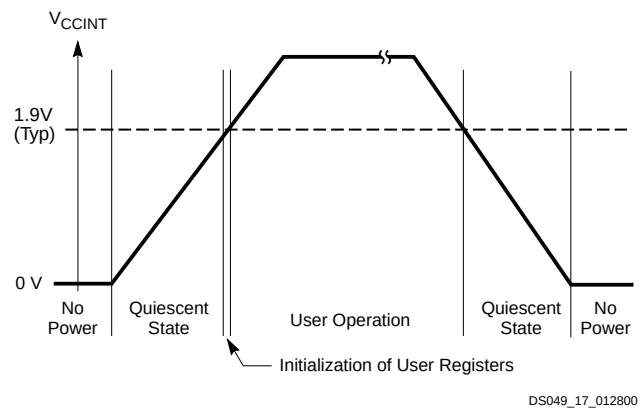


Figure 17: Device Behavior During Power-up

Table 5: XC9500XV Device Characteristics

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold	Pull-up	Pull-up	Bus-Hold
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

Revision History

Date	Revision No.	Description
1/19/99	1.0	Initial Xilinx release. Advance information specification.
2/1/00	1.1	Updated 3.3V information, added Output Banking, added DS049 number.

XC95288XV Low-power, High-performance CPLD

DS050 (v1.3) February 1, 2000

Advance Product Specification

Features

- 288 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (117 user I/O pins)
  - 208-pin PQFP (168 user I/O pins)
  - 256-pin BGA (192 user I/O pins)
  - 280-pin CSP (192 user I/O pins)
  - 256-pin FBGA (192 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Four separate output banks
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95288XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of 16 54V18 Function Blocks, providing 6,400 usable gates with propagation delays of 6 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

XC95144XV Low-power, High-performance CPLD

DS051 (v1.1) February 1, 2000

Advance Product Specification

Features

- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-pin CSP (117 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Two separate output banks
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95144XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

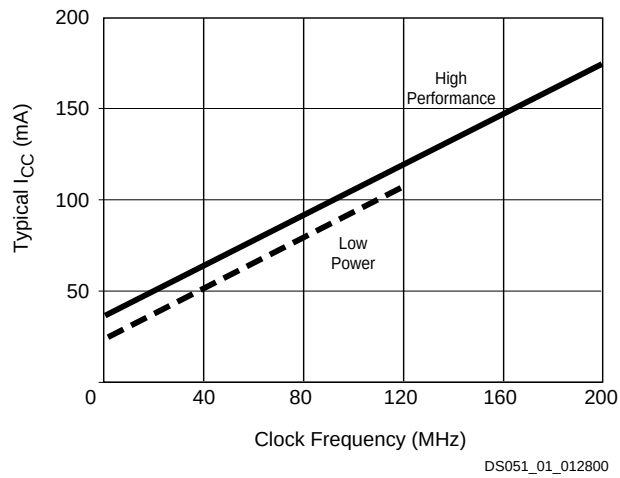


Figure 1: Typical I_{CC} vs. Frequency for XC95144XV

XC9572XV Low-power, High-performance CPLD

DS052 (v1.1) February 1, 2000

Advance Product Specification

Features

- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (38 user I/O pins)
  - 64-pin VQFP (52 user I/O pins)
  - 100-pin TQFP (72-user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Two separate output banks
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC95144XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

XC9536XV Low-power, High-performance CPLD

DS053 (v1.1) February 1, 2000

Advance Product Specification

Features

- 36 macrocells with 800 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (36 user I/O pins)
  - 64-pin VQFP (36 user I/O pins)
- Optimized for high-performance 2.5V systems
  - Low power operation
  - Multi-voltage operation
- Advanced system features
  - In-system programmable
  - Two separate output banks
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V

Description

The XC9536XV is a 2.5V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 4 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XV device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

FastFLASH™ XC9500XL High-performance CPLD Family

DS054 (v1.6) February 1, 2000

Product Specification

Features

- Optimized for high-performance 3.3V systems
  - 5 ns pin-to-pin logic delays, with internal system frequency up to 178 MHz
  - Small footprint packages including VQFPs, TQFPs and CSPs (Chip Scale Package)
  - Lower power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Supports hot-plugging capability
  - Full IEEE Standard 1149.1 boundary-scan (JTAG) support on all devices
- Four pin-compatible device densities
  - 36 to 288 macrocells, with 800 to 6400 usable gates
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - 10,000 program/erase cycles endurance rating
  - 20 year data retention
- Pin-compatible with 5V core XC9500 family in common package footprints

Table 1: XC9500XL Device Family

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
Macrocells	36	72	144	288
Usable Gates	800	1,600	3,200	6,400
Registers	36	72	144	288
t_{PD} (ns)	5	5	5	7
t_{SU} (ns)	3.7	3.7	3.7	4.8
t_{CO} (ns)	3.5	3.5	3.5	4.5
f_{SYSTEM} (MHz)	178	178	178	125

Table 2: XC9500XL Packages and User I/O Pins (not including 4 dedicated JTAG pins)

	XC9536XL	XC9572XL	XC95144XL	XC95288XL
44-pin PLCC	34	34		
44-pin VQFP	34	34		
64-pin VQFP	36	52		
100-pin TQFP		72	81	
144-pin TQFP			117	117
208-pin PQFP				168
48-pin CSP	36	38		
144-pin CSP			117	
280-pin CSP				192
256-pin BGA				192
256-pin FBGA				192

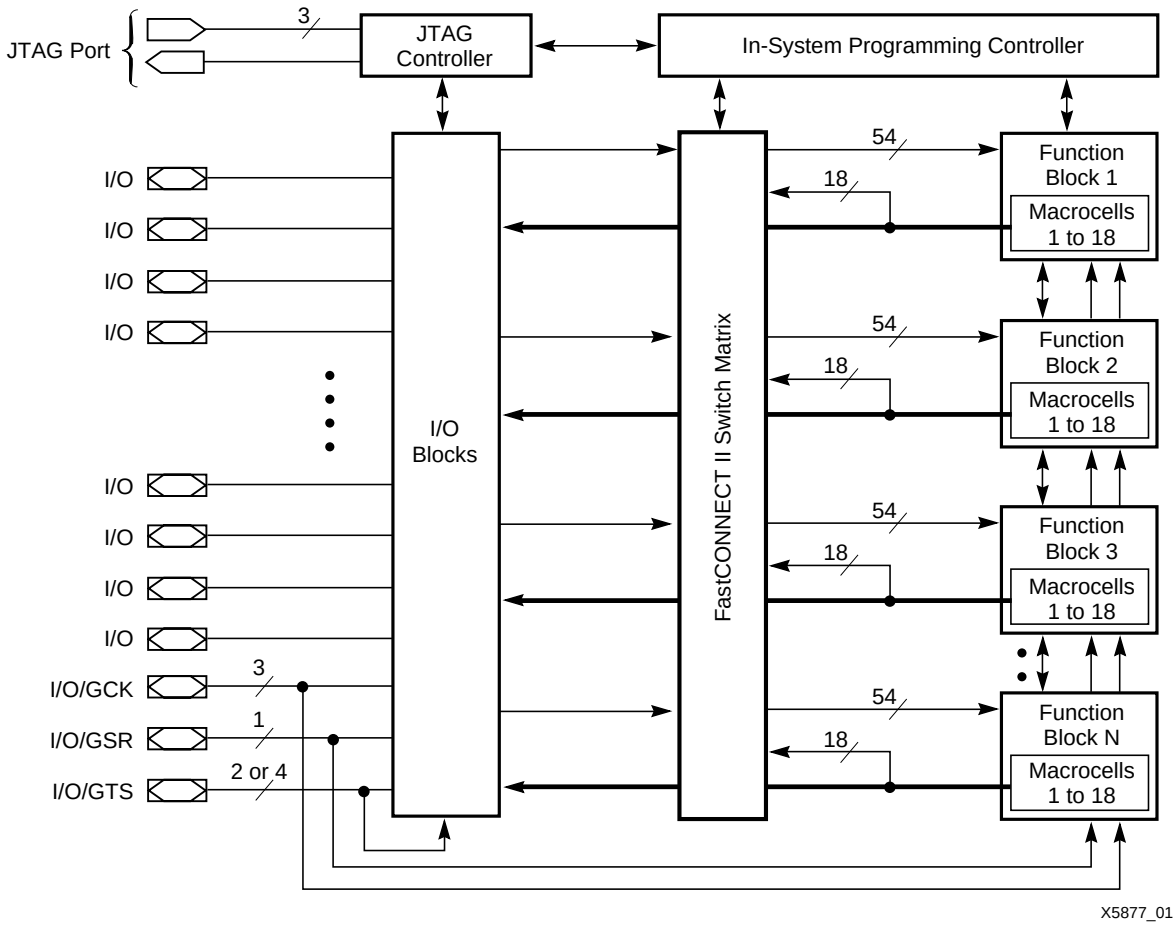


Figure 1: XC9500XL Architecture
Note: Function block outputs (indicated by the bold lines) drive the I/O blocks directly.

Family Overview

The FastFLASH XC9500XL family is a 3.3V CPLD family targeted for high-performance, low-voltage applications in leading-edge communications and computing systems, where high device reliability and low power dissipation is important. Each XC9500XL device supports in-system programming (ISP) and the full IEEE 1149.1 (JTAG) boundary-scan, allowing superior debug and design iteration capability for small form-factor packages. The XC9500XL family is designed to work closely with the Xilinx Virtex, Spartan-XL and XC4000XL FPGA families, allowing system designers to partition logic optimally between fast interface circuitry and high-density general purpose logic. As shown in Table 1, logic density of the XC9500XL devices ranges from 800 to 6400 usable gates with 36 to 288 registers, respectively. Multiple package options and associated I/O capacity are shown in Table 2. The XC9500XL family members are fully pin-compatible, allowing easy design migration across multiple density options in a given package footprint.

The XC9500XL architectural features address the requirements of in-system programmability. Enhanced pin-locking capability avoids costly board rework. In-system programming throughout the full commercial operating range and a high programming endurance rating provide worry-free reconfigurations of system field upgrades. Extended data retention supports longer and more reliable system operating life.

Advanced system features include output slew rate control and user-programmable ground pins to help reduce system noise. Each user pin is compatible with 5V, 3.3V, and 2.5V inputs, and the outputs may be configured for 3.3V or 2.5V operation. The XC9500XL device exhibits symmetric full 3.3V output voltage swing to allow balanced rise and fall times.

Architecture Description

Each XC9500XL device is a subsystem consisting of multiple Function Blocks (FBs) and I/O Blocks (IOBs) fully interconnected by the FastCONNECT II switch matrix. The IOB provides buffering for device inputs and outputs. Each FB provides programmable logic capability with extra wide 54inputs and 18 outputs. The FastCONNECT II switch matrix connects all FB outputs and input signals to the FB inputs. For each FB, up to 18 outputs (depending on package pin-count) and associated output enable signals drive directly to the IOBs. See Figure 1

Function Block

Each Function Block, as shown in Figure 2 is comprised of 18 independent macrocells, each capable of implementing a combinatorial or registered function. The FB also receives global clock, output enable, and set/reset signals. The FB generates 18 outputs that drive the FastCONNECT switch matrix. These 18 outputs and their corresponding output enable signals also drive the IOB.

Logic within the FB is implemented using a sum-of-products representation. Fifty-four inputs provide 108 true and complement signals into the programmable AND-array to form 90 product terms. Any number of these product terms, up to the 90 available, can be allocated to each macrocell by the product term allocator.

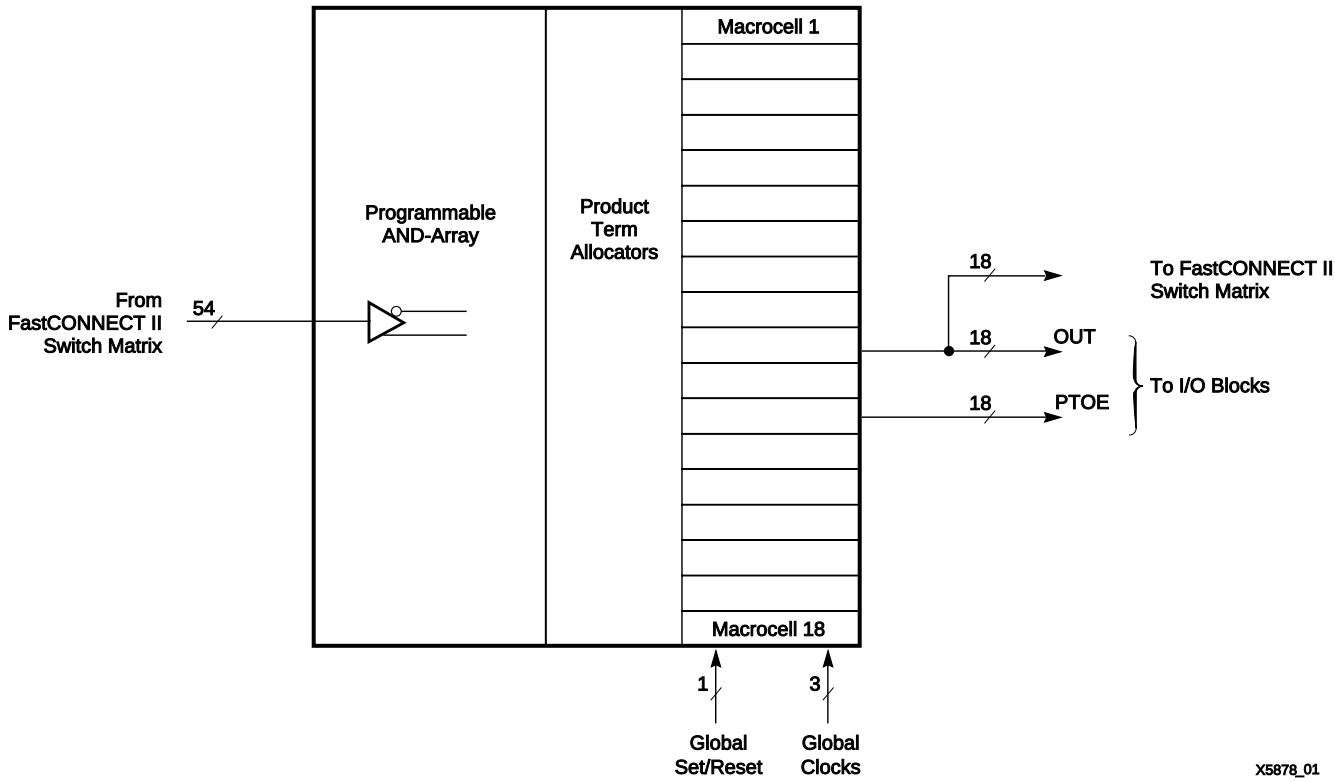


Figure 2: XC9500XL Function Block

Macrocell

Each XC9500XL macrocell may be individually configured for a combinatorial or registered function. The macrocell and associated FB logic is shown in Figure 3.

Five direct product terms from the AND-array are available for use as primary data inputs (to the OR and XOR gates) to implement combinatorial functions, or as control inputs including clock, clock enable, set/reset, and output enable.

The product term allocator associated with each macrocell selects how the five direct terms are used.

The macrocell register can be configured as a D-type or T-type flip-flop, or it may be bypassed for combinatorial operation. Each register supports both asynchronous set and reset operations. During power-up, all user registers are initialized to the user-defined preload state (default to 0 if unspecified).

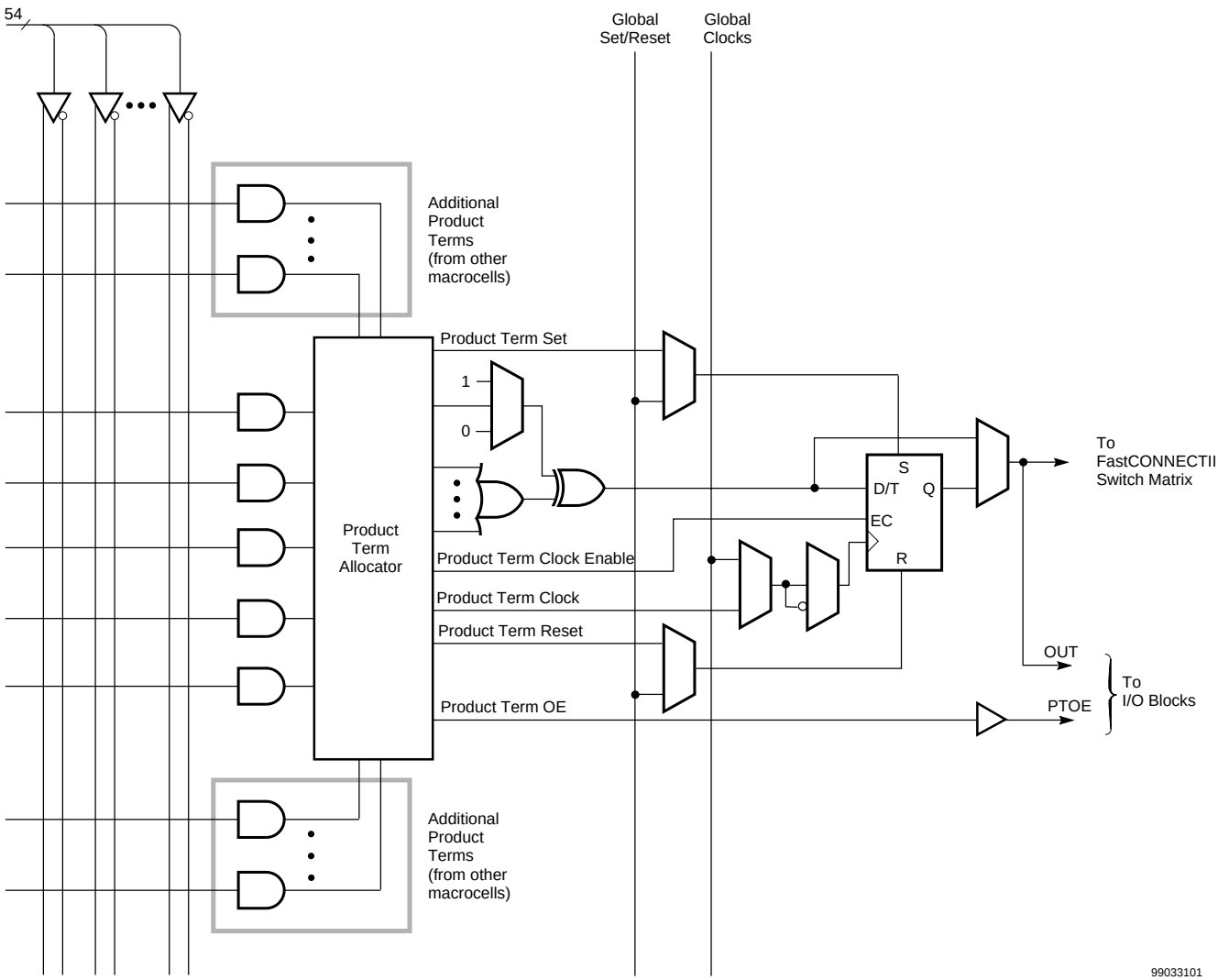


Figure 3: XC9500XL Macrocell Within Function Block

All global control signals are available to each individual macrocell, including clock, set/reset, and output enable signals. As shown in Figure 4, the macrocell register clock originates from either of three global clocks or a product term clock. Both true and complement polarities of the selected clock source can be used within each macrocell. A GSR input is also provided to allow user registers to be set to a user-defined state.

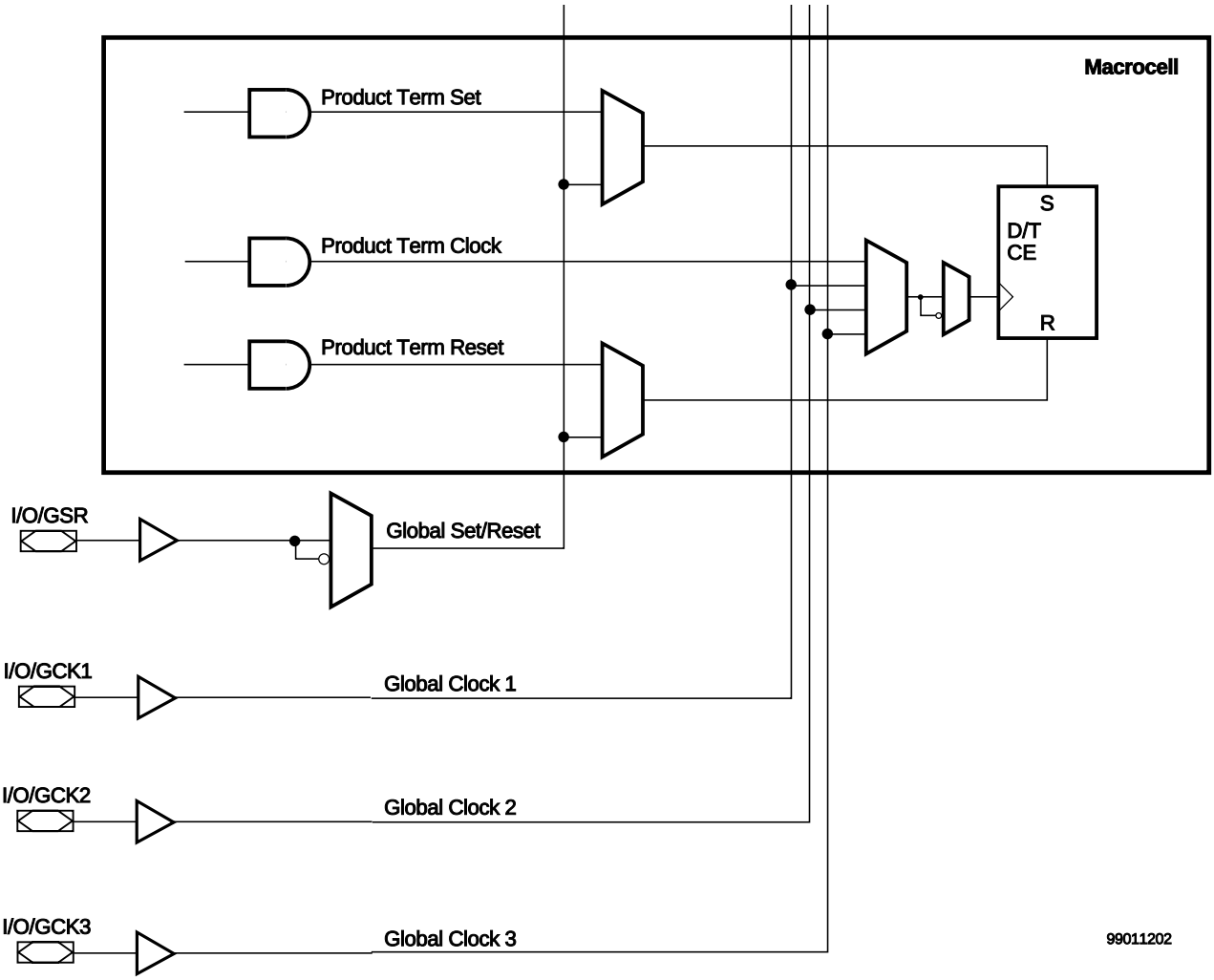


Figure 4: Macrocell Clock and Set/Reset Capability

Product Term Allocator

The product term allocator controls how the five direct product terms are assigned to each macrocell. For example, all five direct terms can drive the OR function as shown in Figure 5.

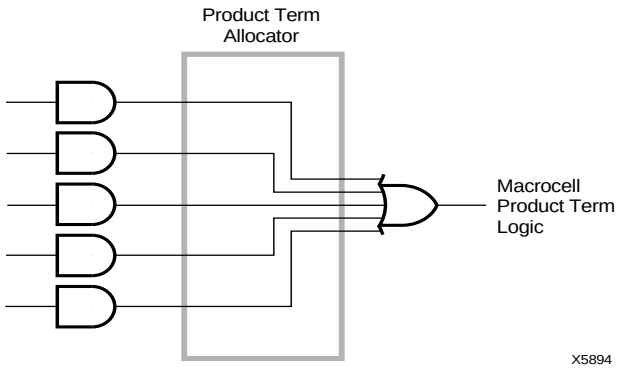


Figure 5: Macrocell Logic Using Direct

The product term allocator can re-assign other product terms within the FB to increase the logic capacity of a macrocell beyond five direct terms. Any macrocell requiring additional product terms can access uncommitted product terms in other macrocells within the FB. Up to 15 product terms can be available to a single macrocell with only a small incremental delay of $t_{PTA,}$ as shown in Figure 6.

Note that the incremental delay affects only the product terms in other macrocells. The timing of the direct product terms is not changed.

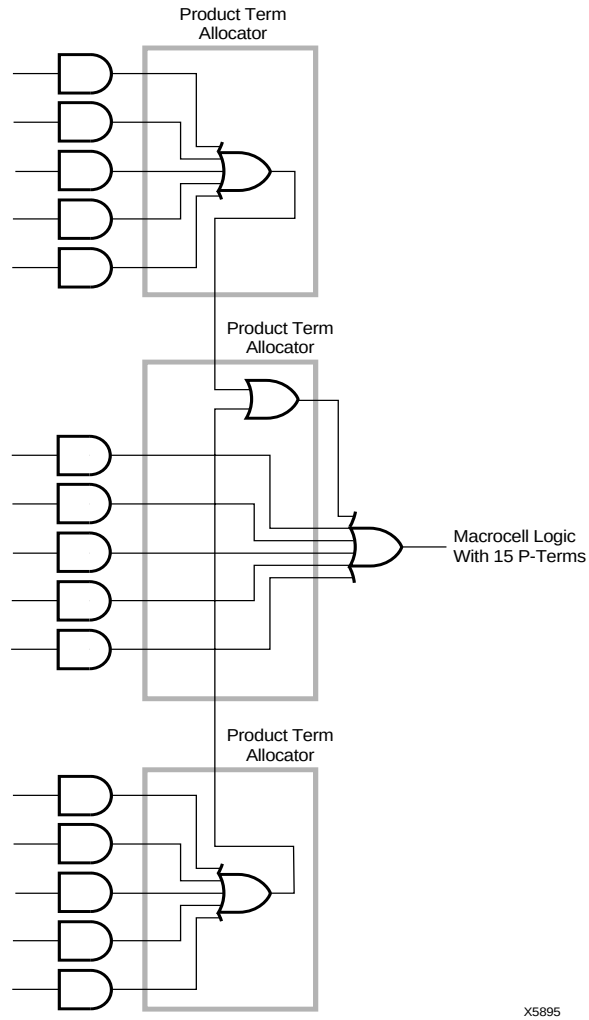


Figure 6: Product Term Allocation With 15 Product Terms

The product term allocator can re-assign product terms from any macrocell within the FB by combining partial sums of products over several macrocells, as shown in Figure 7.

In this example, the incremental delay is only $2*t_{PTA}$. All 90 product terms are available to any macrocell, with a maximum incremental delay of $8*t_{PTA}$.

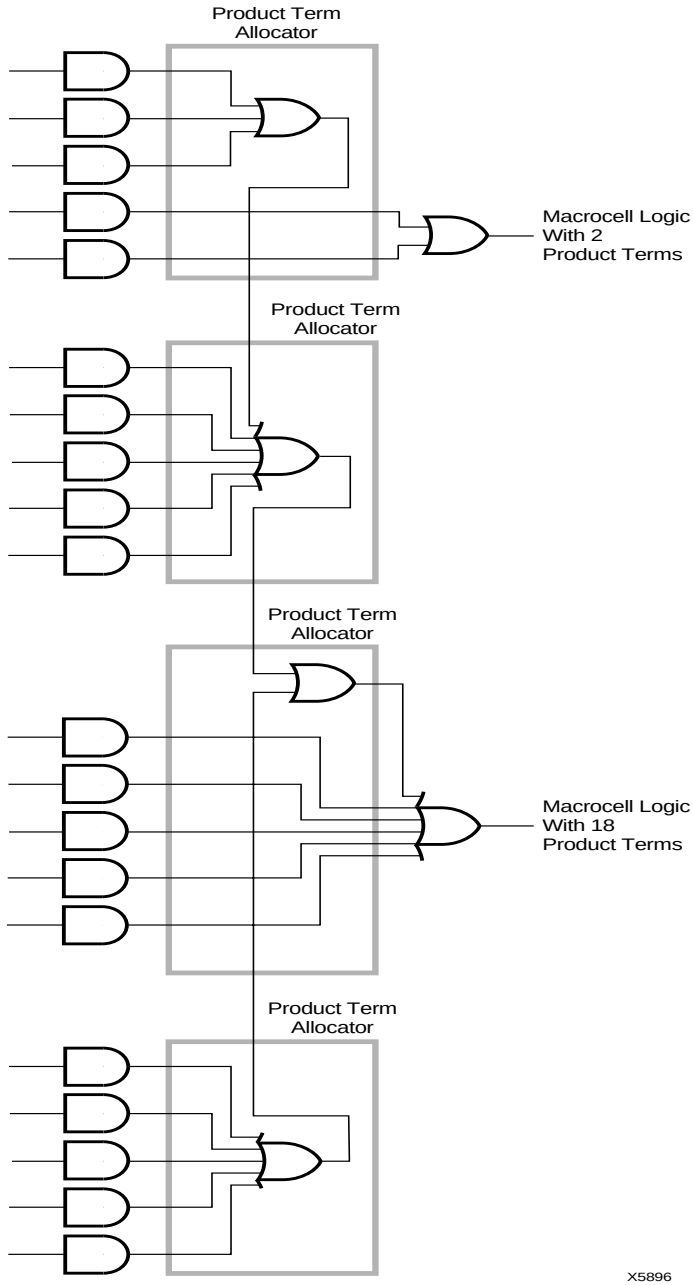


Figure 7: Product Term Allocation Over Several Macrocells

The internal logic of the product term allocator is shown in Figure 8.

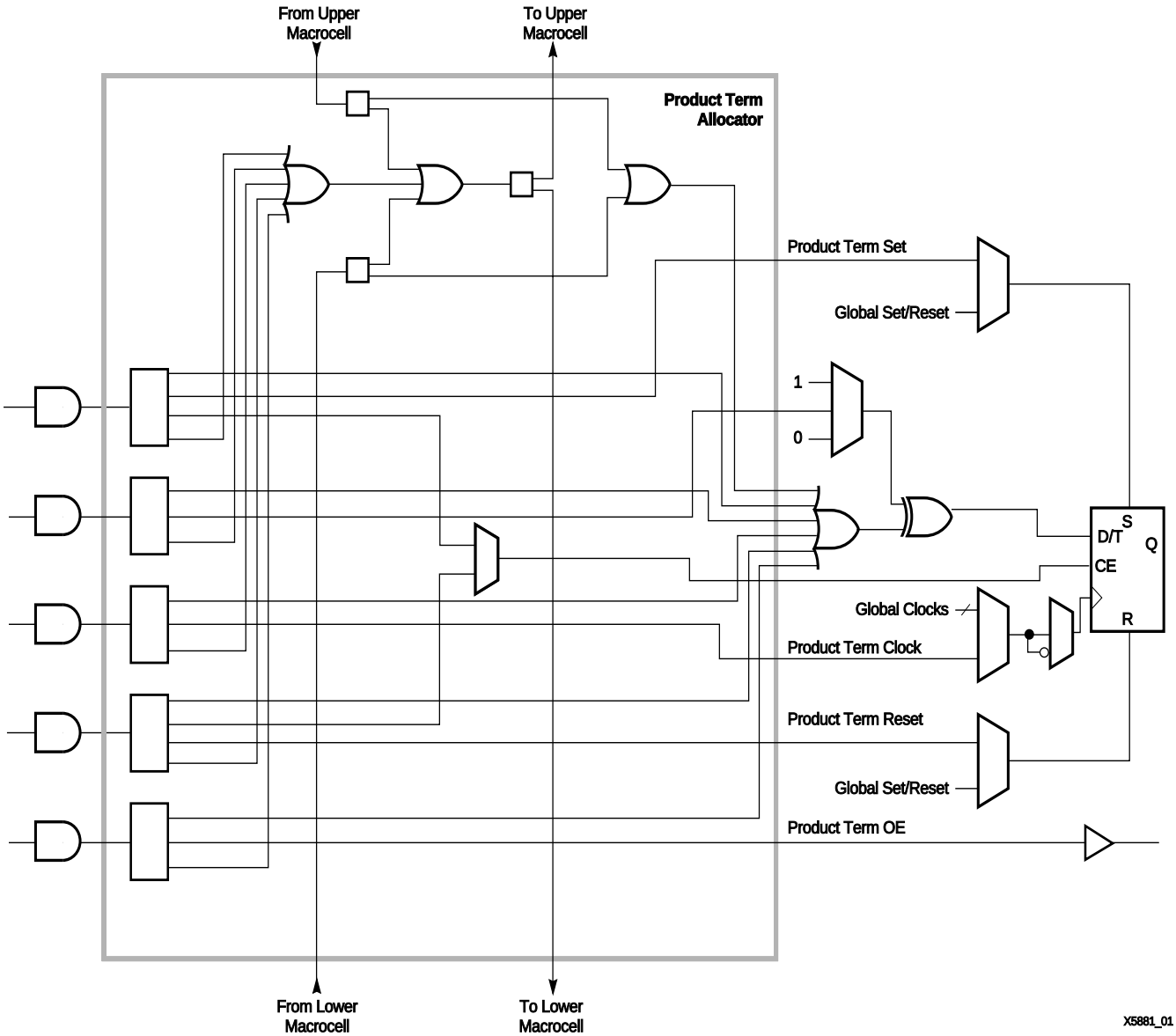


Figure 8: Product Term Allocator Logic

FastCONNECT II Switch Matrix

The FastCONNECT II Switch Matrix connects signals to the FB inputs, as shown in Figure 9. All IOB outputs (corresponding to user pin inputs) and all FB outputs drive the FastCONNECT II matrix. Any of these (up to a fan-in limit of 54) may be selected to drive each FB with a uniform delay.

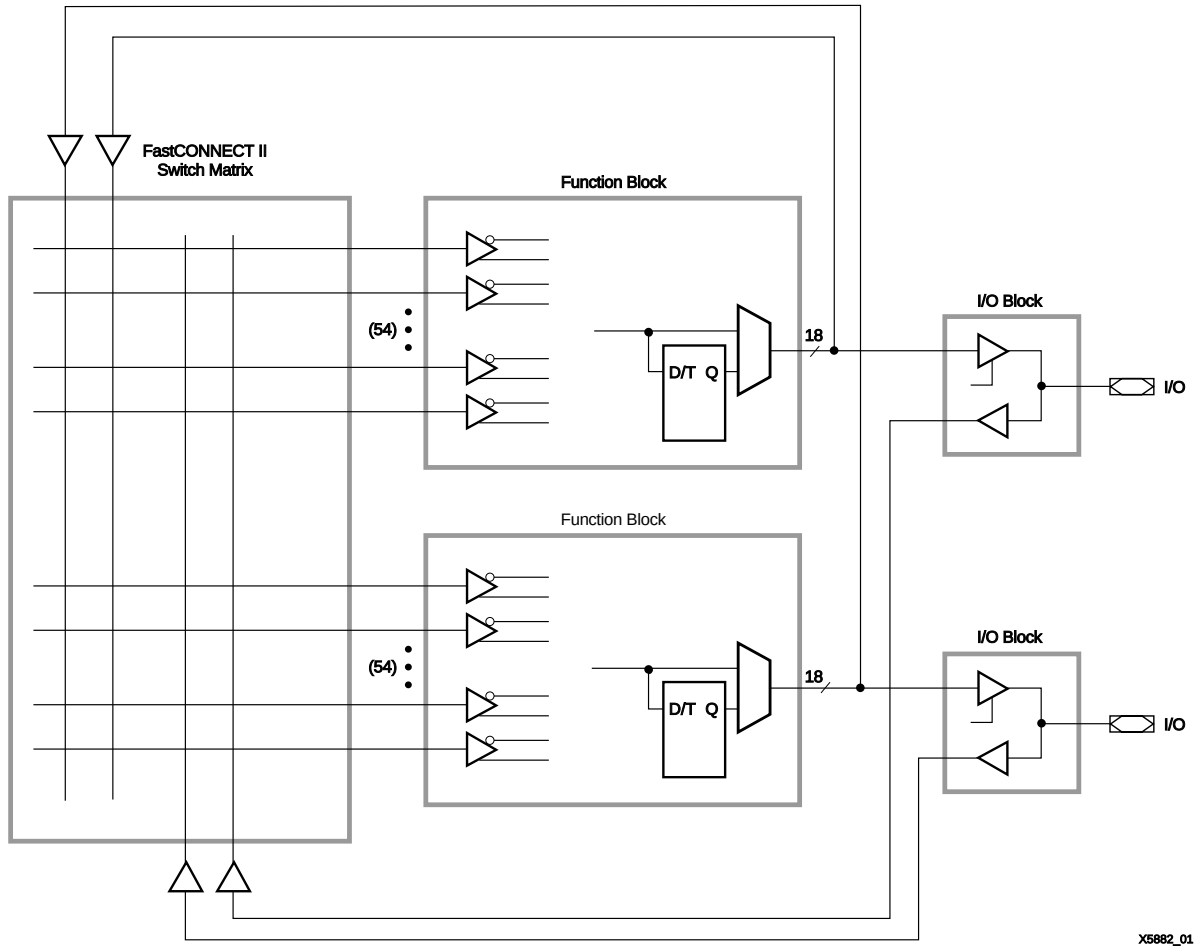


Figure 9: FastCONNECT II Switch Matrix

I/O Block

The I/O Block (IOB) interfaces between the internal logic and the device user I/O pins. Each IOB includes an input buffer, output driver, output enable selection multiplexer, and user programmable ground control. See Figure 10 for details.

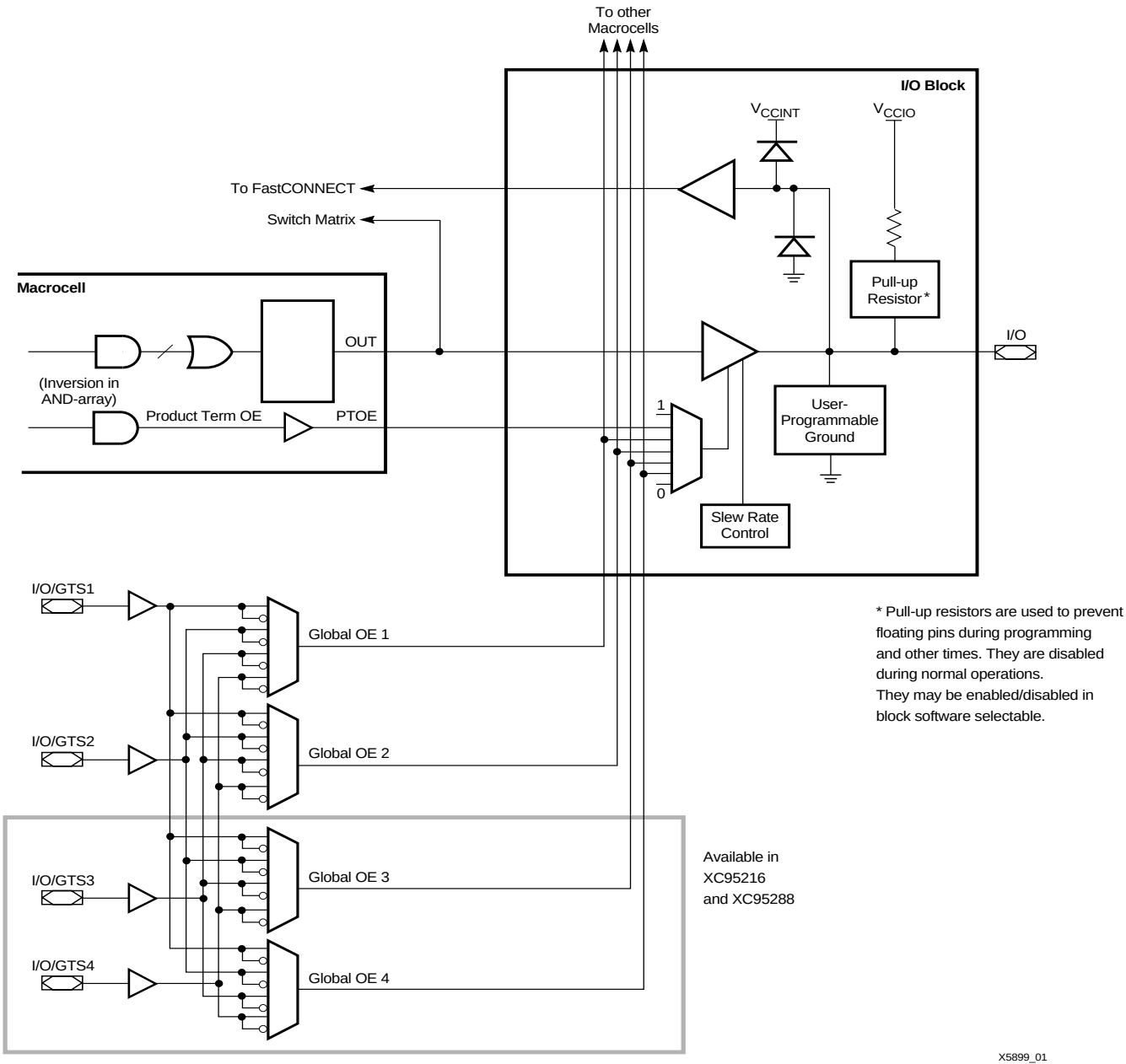


Figure 10: I/O Block and Output Enable Capability

The input buffer is compatible with 5V CMOS, 5V TTL, 3.3V CMOS, and 2.5V CMOS signals. The input buffer uses the internal 3.3V voltage supply (V_{CCINT}) to ensure that the input thresholds are constant and do not vary with the V_{CCIO} voltage. Each input buffer provides input hysteresis (50 mV typical) to help reduce system noise for input signals with slow rise or fall edges.

Each output driver is designed to provide fast switching with minimal power noise. All output drivers in the device may be configured for driving either 3.3V CMOS levels (which are compatible with 5V TTL levels as well) or 2.5V CMOS levels by connecting the device output voltage supply (V_{CCIO}) to a 3.3V or 2.5V voltage supply. Figure 11 shows how the XC9500XL device can be used in 3.3V only sys-

tems and mixed voltage systems with any combination of 5V, 3.3V and 2.5V power supplies.

Each output driver can also be configured for slew-rate limited operation. Output edge rates may be slowed down to reduce system noise (with an additional time delay of t_{SLEW}) under user control. See Figure 12.

The output enable may be generated from one of four options: a product term signal from the macrocell, any of the global output enable signals (GTS), always “1,” or always “0.” There are two global output enables for devices with 72 or fewer macrocells, and four global output enables for devices with 144 or more macrocells. Any selected output enable signal may be inverted locally at each pin output to provide maximal design flexibility.

Each IOB provides user programmable ground pin capability. This allows device I/O pins to be configured as additional ground pins in order to force otherwise unused pins to a low voltage state, as well as provide for additional device grounding capability. This grounding of the pin is achieved by internal logic that forces a logic low output regardless of the internal macrocell signal, so the internal macrocell logic is unaffected by the programmable ground pin capability.

Each IOB also provides for bus-hold circuitry (also called a “keeper”)that is active during valid user operation. The bus-hold feature eliminates the need to tie unused pins either high or low by holding the last known state of the input until the next input signal is present. The bus-hold circuit drives back the same state via a nominal resistance (R_{BH}) of 50k ohms. See Figure 13. Note the bus-hold output will drive no higher than V_{CCIO} to prevent overdriving signals when interfacing to 2.5V components.

When the device is not in valid user operation, the bus-hold circuit defaults to an equivalent 50k ohm pull-up resistor in order to provide a known repeatable device state. This occurs when the device is in the erased state, in programming mode, in JTAG INTEST mode, or during initial power-up. A pull-down resistor (1k ohm) may be externally added to any pin to override the default R_{BH} resistance to force a low state during power-up or any of these other modes.

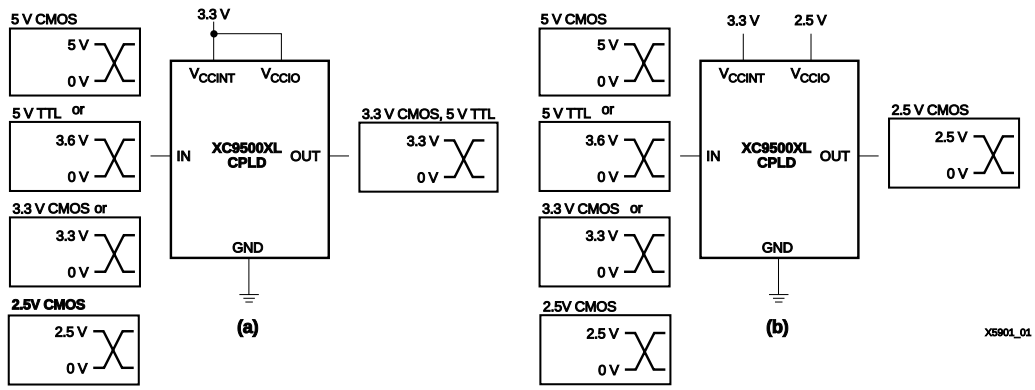


Figure 11: XC9500XL Devices in (a) 3.3V only and (b) Mixed 5V/3.3V/2.5V Systems

5V Tolerant I/Os

The I/Os on each XC9500XL device are fully 5V tolerant even though the core power supply is 3.3 volts. This allows 5V CMOS signals to connect directly to the XC9500XL inputs without damage. In addition, the 3.3V V_{CCINT} power supply can be applied before or after 5V signals are applied to the I/Os. In mixed 5V/3.3V/2.5V systems, the user pins, the core power supply (V_{CCINT}), and the output power supply (V_{CCIO}) may have power applied in any order. This makes the XC9500XL devices immune to power supply sequencing problems.

Xilinx proprietary ESD circuitry and high impedance initial state permit hot plugging cards using these devices.

Pin-Locking Capability

The capability to lock the user defined pin assignments during design iteration depends on the ability of the architecture to adapt to unexpected changes. The XC9500XL devices incorporate architectural features that enhance the ability to accept design changes while maintaining the same pinout.

The XC9500XL architecture provides for superior pin-locking characteristics with a combination of large number of routing switches in the FastCONNECT II switch matrix, a 54-wide input Function Block, and flexible, bi-directional product term allocation within each macrocell. These features address design changes that require adding or changing internal routing, including additional signals into

existing equations, or increasing equation complexity, respectively.

For extensive design changes requiring higher logic capacity than is available in the initially chosen device, the new design may be able to fit into a larger pin-compatible device using the same pin assignments. The same board may be used with a higher density device without the expense of board rework.

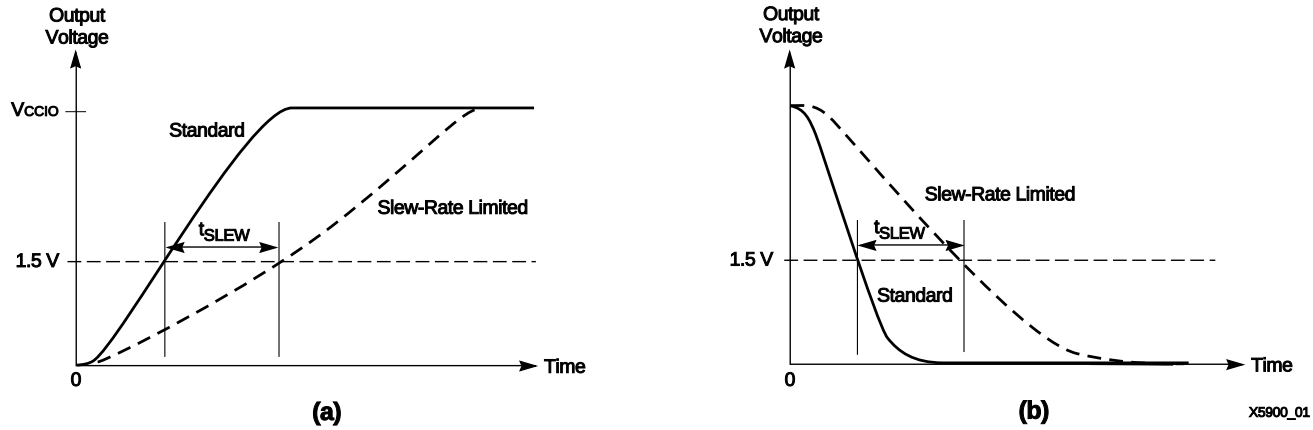


Figure 12: Output Slew-Rate Control For (a) Rising and (b) Falling Outputs

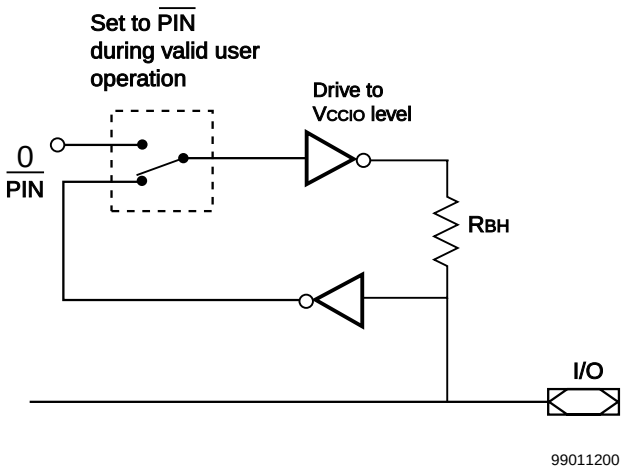


Figure 13: Bus-Hold Logic

In-System Programming

One or more XC9500XL devices can be daisy chained together and programmed in-system via a standard 4-pin JTAG protocol, as shown in Figure 14. In-system programming offers quick and efficient design iterations and eliminates package handling. The Xilinx development system provides the programming data sequence using a Xilinx download cable, a third-party JTAG development system, JTAG-compatible board tester, or a simple microprocessor interface that emulates the JTAG instruction sequence.

All I/Os are 3-stated and pulled high by the bus-hold circuitry during in-system programming. If a particular signal must remain low during this time, then a pulldown resistor may be added to the pin.

External Programming

XC9500XL devices can also be programmed by the Xilinx HW-130 device programmer as well as third-party programmers. This provides the added flexibility of using pre-programmed devices during manufacturing, with an in-system programmable option for future enhancements and design changes.

Reliability and Endurance

All XC9500XL CPLDs provide a minimum endurance level of 10,000 in-system program/erase cycles and a minimum data retention of 20 years. Each device meets all functional, performance, and data retention specifications within this endurance limit.

IEEE 1149.1 Boundary-Scan (JTAG)

XC9500XL devices fully support IEEE 1149.1 boundary-scan (JTAG). EXTEST, SAMPLE/PRELOAD, BYPASS, USERCODE, INTEST, IDCODE, HIGHZ and CLAMP instructions are supported in each device. Additional instructions are included for in-system programming operations.

Design Security

XC9500XL devices incorporate advanced data security features which fully protect the programming data against unauthorized reading or inadvertent device erasure/reprogramming. Table 3 shows the four different security settings available.

The read security bits can be set by the user to prevent the internal programming pattern from being read or copied. When set, they also inhibit further program operations but

allow device erase. Erasing the entire device is the only way to reset the read security bit.

The write security bits provide added protection against accidental device erasure or reprogramming when the JTAG pins are subject to noise, such as during system power-up. Once set, the write-protection may be deactivated when the device needs to be reprogrammed with a valid pattern with a specific sequence of JTAG instructions.

Table 3: Data Security Options

Write Security	Read Security: Default	Read Security: Set
Default	Read Allowed Program/Erase Allowed	Read Inhibited Program Inhibit Erase Allowed
Set	Read Allowed Program/Erase Allowed	Read Inhibited Program/Erase Inhibited

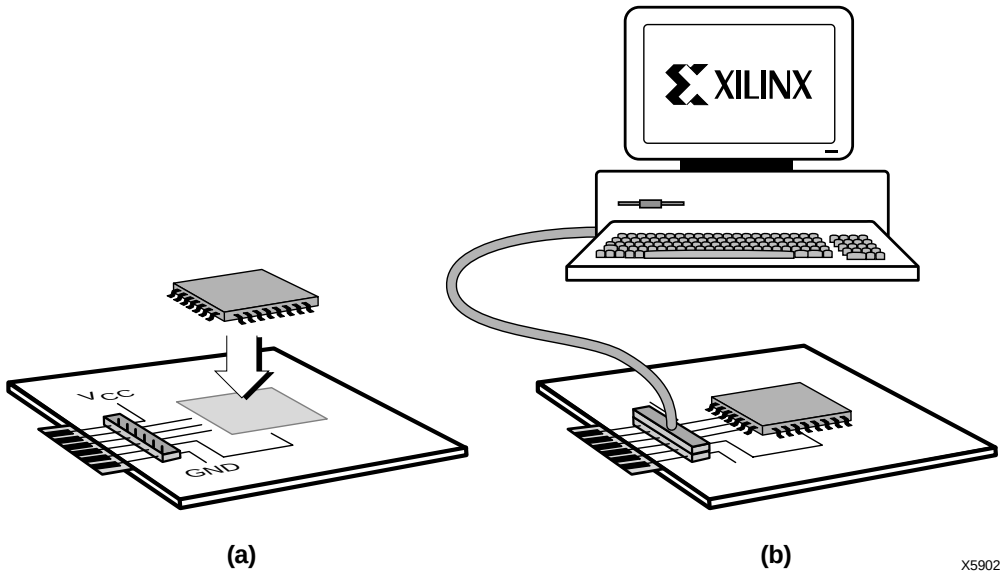


Figure 14: In-System Programming Operation (a) Solder Device to PCB and (b) Program Using Download Cable

Low Power Mode

All XC9500XL devices offer a low-power mode for individual macrocells or across all macrocells. This feature allows the device power to be significantly reduced.

Each individual macrocell may be programmed in low-power mode by the user. Performance-critical parts of the application can remain in standard power mode, while other parts of the application may be programmed for low-power operation to reduce the overall power dissipation. Macrocells programmed for low-power mode incur additional delay (t_{LP}) in pin-to-pin combinatorial delay as well as register setup time. Product term clock to output and product term output enable delays are unaffected by the macrocell power-setting.

Timing Model

The uniformity of the XC9500XL architecture allows a simplified timing model for the entire device. The basic timing model, shown in Figure 15, is valid for macrocell functions that use the direct product terms only, with standard power setting, and standard slew rate setting. Table 4 shows how each of the key timing parameters is affected by the product term allocator (if needed), low-power setting, and slew-limited setting.

The product term allocation time depends on the logic span of the macrocell function, which is defined as one less than the maximum number of allocators in the product term path. If only direct product terms are used, then the logic span is 0. The example in Figure 6 shows that up to 15 product terms are available with a span of 1. In the case of Figure 7, the 18 product term function has a span of 2.

Detailed timing information may be derived from the full timing model shown in Figure 16. The values and explanations for each parameter are given in the individual device data sheets.

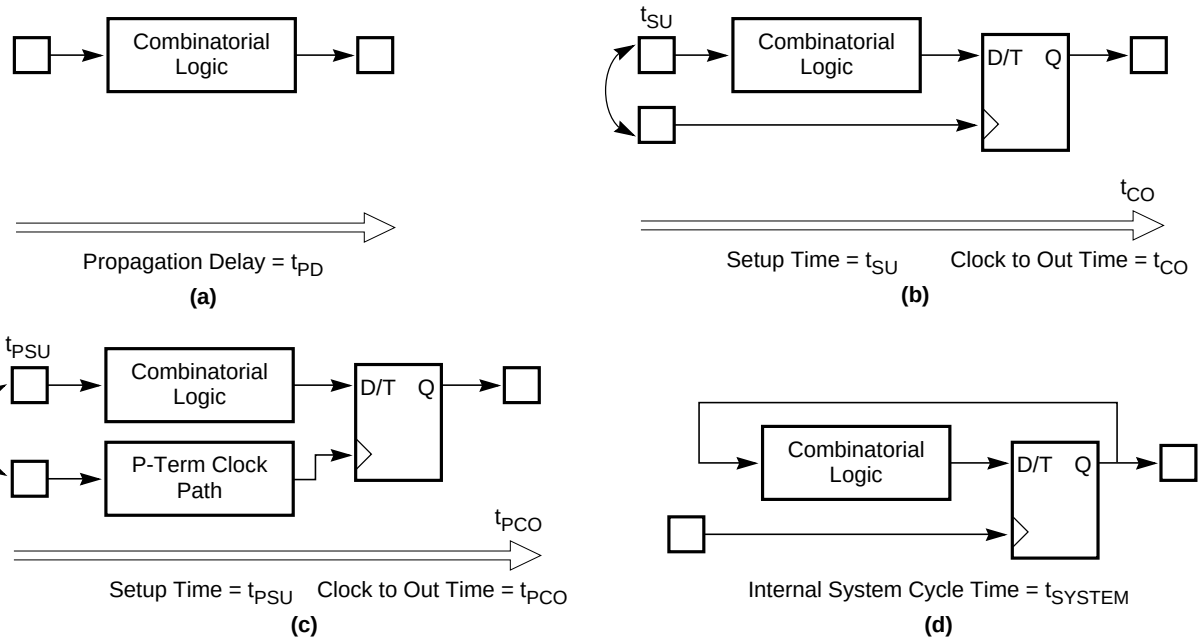


Figure 15: Basic Timing Model

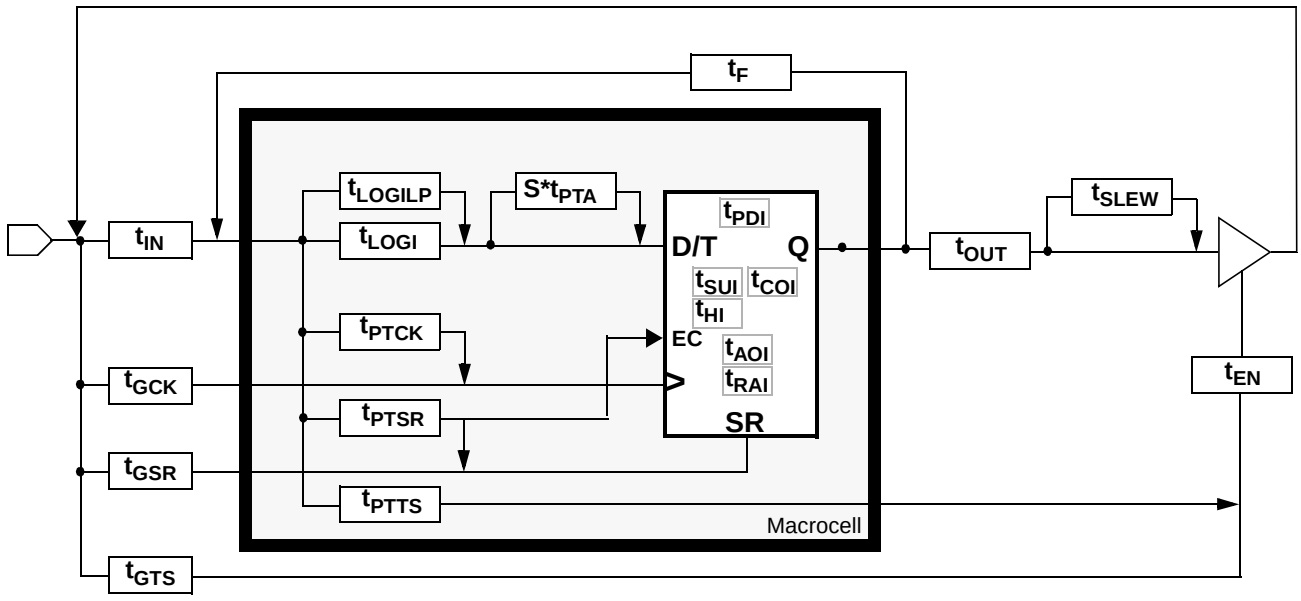


Figure 16: Detailed Timing Model

Power-Up Characteristics

The XC9500XL devices are well behaved under all operating conditions. During power-up each XC9500XL device employs internal circuitry which keeps the device in the quiescent state until the V_{CCINT} supply voltage is at a safe level (approximately 2.5 V). During this time, all device pins and JTAG pins are disabled and all device outputs are disabled with the pins weakly pulled high, as shown in Table . When the supply voltage reaches a safe level, all user registers become initialized (typically within 200 µs), and the device is immediately available for operation, as shown in Figure 17.

If the device is in the erased state (before any user pattern is programmed), the device outputs remain disabled with weak pull-up. The JTAG pins are enabled to allow the device to be programmed at any time. All devices are shipped in the erased state from the factory.

If the device is programmed, the device inputs and outputs take on their configured states for normal operation. The JTAG pins are enabled to allow device erasure or boundary-scan tests at any time.

Development System Support

The XC9500XL family and associated in-system programming capabilities are fully supported in either software solutions available from Xilinx.

The Foundation Series is an all-in-one development system containing schematic entry, HDL (VHDL, Verilog, and ABEL), and simulation capabilities. It supports the XC9500XL family as well as other CPLD and FPGA families.

The Alliance Series includes CPLD and FPGA implementation technology as well as all necessary libraries and interfaces for Alliance partner EDA solutions.

FastFLASH Technology

An advanced 0.35 micron feature size CMOS Flash process is used to fabricate all XC9500XL devices. The FastFLASH process provides high performance logic capability, fast programming times, and superior reliability and endurance ratings.

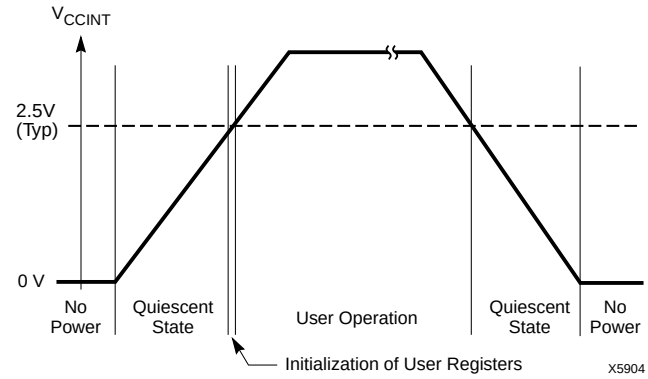


Figure 17: Device Behavior During Power-up

Table 4: Timing Model Parameters

Description	Parameter	Product Term Allocator[1]	Macrocell Low-Power Setting	Output Slew-Limited Setting
Propagation Delay	t_{PD}	+ t_{PTA} * S	+ t_{LP}	+ t_{SLEW}
Global Clock Setup Time	t_{SU}	+ t_{PTA} * S	+ t_{LP}	–
Global Clock-to-output	t_{CO}	–	–	+ t_{SLEW}
Product Term Clock Setup Time	t_{PSU}	+ t_{PTA} * S	+ t_{LP}	–
Product Term Clock-to-output	t_{PCO}	–	–	+ t_{SLEW}
Internal System Cycle Period	t_{SYSTEM}	+ t_{PTA} * S	+ t_{LP}	–

Note: 1. S = the logic span of the function, as defined in the text.

Table 5: XC9500XL Device Characteristics

Device Circuitry	Quiescent State	Erased Device Operation	Valid User Operation
IOB Bus-Hold	Pull-up	Pull-up	Bus-Hold
Device Outputs	Disabled	Disabled	As Configured
Device Inputs and Clocks	Disabled	Disabled	As Configured
Function Block	Disabled	Disabled	As Configured
JTAG Controller	Disabled	Enabled	Enabled

Date	Revision	Revision
9/28/98	1.0	Initial Xilinx release
10/2/98	1.1	Figure 1 correction
2/3/99	1.2	Included hot socket reference; revised layout; BGA package change for XC95288XL
4/2/99	1.3	Minor typesetting corrections.
6/7/99	1.4	Minor typesetting corrections.
6/7/99	1.5	Added CS280 package
2/1/00	1.6	Update Family Device Table 1, added DS054.

XC95288XL High-performance CPLD

DS055 (v1.3) February 1, 2000

Product Specification

Features

- 7 ns pin-to-pin logic delays
- System frequency up to 125 MHz
- 288 macrocells with 6,400 usable gates
- Available in small footprint packages
  - 144-pin TQFP (117 user I/O pins)
  - 208-pin PQFP (168 user I/O pins)
  - 256-pin BGA (192 user I/O pins)
  - 256-pin FA (192 user I/O pins)
  - 280-pin CSP (192 user I/O pins)
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC95288 device in the 208-pin HQFP package

Description

The XC95288XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of 16 54V18 Function Blocks, providing 6,400 usable gates with propagation delays of 7 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

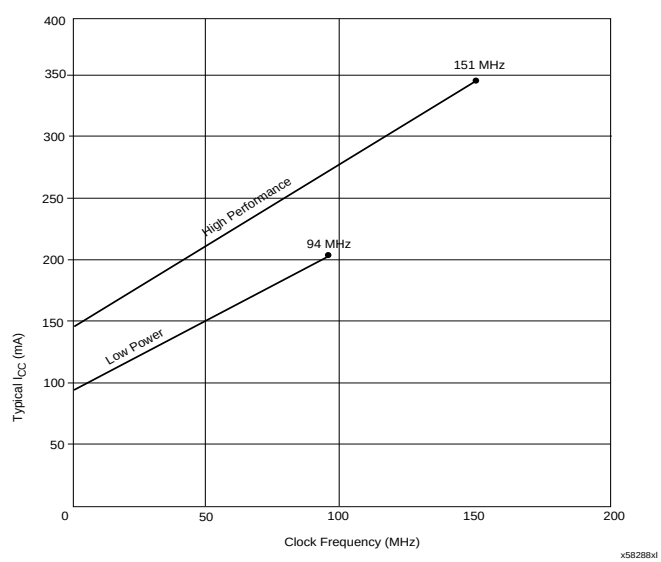


Figure 1: Typical I_{CC} vs. Frequency for XC95288XL

XC95144XL High Performance CPLD

DS056 (v1.3) February 1, 2000

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 144 macrocells with 3,200 usable gates
- Available in small footprint packages
  - 100-pin TQFP (81 user I/O pins)
  - 144-pin TQFP (117 user I/O pins)
  - 144-pin CSP (117 user I/O pins)
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin with local inversion
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold ciruitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC95144 device in the 100-pin TQFP package

Description

The XC95144XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of eight 54V18 Function Blocks, providing 3,200 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can very substantially depending on the system frequency, design application, and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in graphical form.

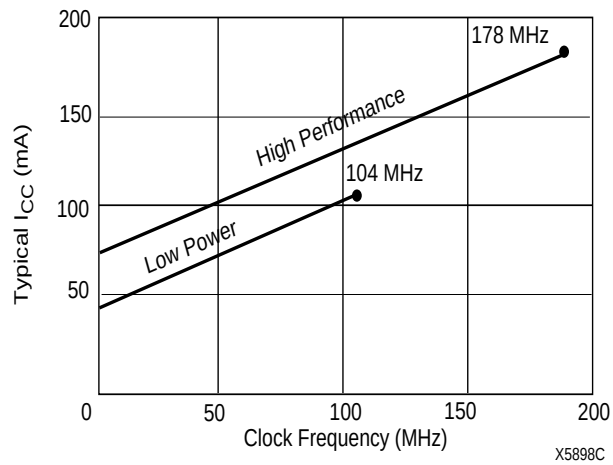


Figure 1: Typical I_{cc} vs. Frequency for XC95144XL

XC9572XL High-performance CPLD

DS057 (v1.1) February 1, 2000

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 72 macrocells with 1,600 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (38 user I/O pins)
  - 64-pin VQFP (52 user I/O pins)
  - 100-Pin TQFP (72 user I/O pins)
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC9572 device in the 44-pin PLCC package and the 100-pin TQFP package

Description

The XC9572XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of four 54V18 Function Blocks, providing 1,600 usable gates with propagation delays of 4 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

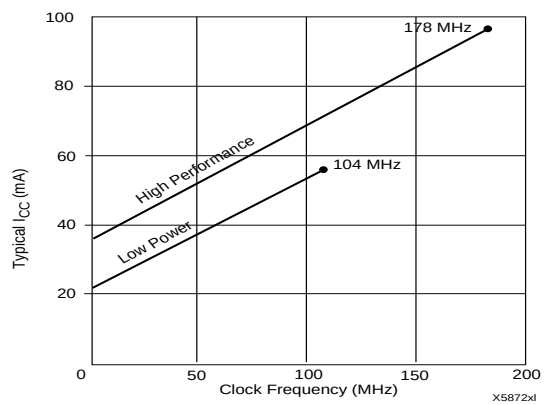


Figure 1: Typical I_{CC} vs. Frequency for XC9572XL

XC9536XL High-performance CPLD

DS058 (v1.1) February 1, 2000

Product Specification

Features

- 5 ns pin-to-pin logic delays
- System frequency up to 178 MHz
- 36 macrocells with 800 usable gates
- Available in small footprint packages
  - 44-pin PLCC (34 user I/O pins)
  - 44-pin VQFP (34 user I/O pins)
  - 48-pin CSP (36 user I/O pins)
  - 64-pin VQFP (36 user I/O pins)
- Optimized for high-performance 3.3V systems
  - Low power operation
  - 5V tolerant I/O pins accept 5V, 3.3V, and 2.5V signals
  - 3.3V or 2.5V output capability
  - Advanced 0.35 micron feature size CMOS FastFLASH™ technology
- Advanced system features
  - In-system programmable
  - Superior pin-locking and routability with FastCONNECT II™ switch matrix
  - Extra wide 54-input Function Blocks
  - Up to 90 product-terms per macrocell with individual product-term allocation
  - Local clock inversion with three global and one product-term clocks
  - Individual output enable per output pin
  - Input hysteresis on all user and boundary-scan pin inputs
  - Bus-hold circuitry on all user pin inputs
  - Full IEEE Standard 1149.1 boundary-scan (JTAG)
- Fast concurrent programming
- Slew rate control on individual outputs
- Enhanced data security features
- Excellent quality and reliability
  - Endurance exceeding 10,000 program/erase cycles
  - 20 year data retention
  - ESD protection exceeding 2,000V
- Pin-compatible with 5V-core XC9536 device in the 44-pin PLCC package and the 48-pin CSP package

Description

The XC9536XL is a 3.3V CPLD targeted for high-performance, low-voltage applications in leading-edge communications and computing systems. It is comprised of two 54V18 Function Blocks, providing 800 usable gates with propagation delays of 5 ns.

Power Estimation

Power dissipation in CPLDs can vary substantially depending on the system frequency, design application and output loading. To help reduce power dissipation, each macrocell in a XC9500XL device may be configured for low-power mode (from the default high-performance mode). In addition, unused product-terms and macrocells are automatically deactivated by the software to further conserve power.

For a general estimate of I_{CC}, the following equation may be used:

I_{CC} (mA) = $MC_{HP}(0.5) + MC_{LP}(0.3) + MC(0.0045\ mA/MHz)\ f$

Where:

MC_{HP} = Macrocells in high-performance (default) mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

This calculation is based on typical operating conditions using a pattern of 16-bit up/down counters in each Function Block with no output loading. The actual I_{CC} value varies with the design application and should be verified during normal system operation.

Figure 1 shows the above estimation in a graphical form.

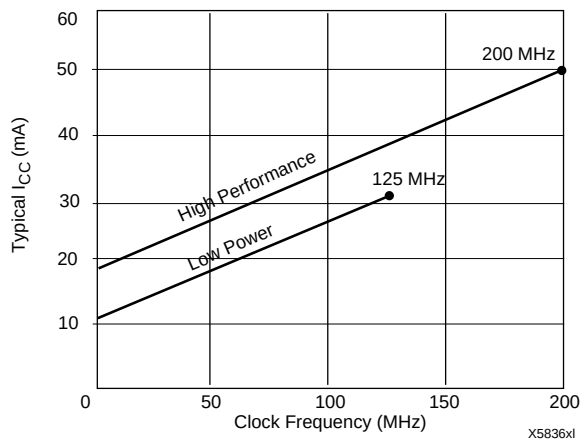


Figure 1: Typical I_{CC} vs. Frequency for XC9536XL

QPRO™ QML Certified and Radiation Hardened Products Table of Contents

QPRO™ High-Reliability QML Certified and Radiation Hardened Products for Aerospace and Defense Applications

January 21, 2000 (v2.0)

The High-Reliability Programmable Logic Leader

Xilinx is the leading supplier of High-Reliability programmable logic devices to the aerospace and defense markets. These devices are used in a wide range of applications such as electronic warfare, missile guidance and targeting, RADAR, SONAR, communications, signal processing, avionics and satellites. The Xilinx QPRO family of ceramic and plastic QML products (Qualified Manufacturers Listing), certified to MIL-PRF-38585, provide system designers with advanced programmable logic solutions for next generation designs. The QPRO family also includes select products that are radiation hardened for use in satellite and other space applications.

The Xilinx QPRO family addresses the issues that are critical to the aerospace and defense market:

QML/Best commercial practices. Commercial manufacturing strengths result in more efficient process flows

Performance-based solutions, including cost-effective plastic packages.

Reliability of supply. Controlled mask sets and processes insure the same quality devices, every time, without variation, which remain in production for an extended time.

Off-the-shelf ASIC solutions. Standard devices readily available, no need for custom logic and gate arrays.

Unmatched Product Offering

The QPRO family provides a wide variety of devices, delivering the industry's fastest and biggest devices. The Virtex members of the QPRO family offers FPGAs with densities greater than 1,000,000 system gates, and even larger devices planned for the future. This broad range of devices is available in a wide variety of speed and package options. Both military temperature and full QML/SMD versions are available as standard off-the-shelf products. Select software cores, such as complete PowerPC peripherals, is also available.

Products for Space Applications

Xilinx offers the industry's only radiation hardened reconfigurable FPGAs for satellite and space. These devices are manufactured using an epitaxial wafer process, and have guaranteed total dose, latch up immunity, and low soft upset rates. These products allow for the ultimate in design and mission flexibility in a cost-effective manner.

QML Certification Part of Overall Quality Platform

Being certified to MIL-PRF-38535 QML complemented by ISO-9000 certification results in an overall product quality platform that makes Xilinx a world-class supplier of programmable logic devices. Designers can confidently design with Xilinx for High-Reliability systems with the knowledge they are getting unsurpassed quality and reliability, and long-term commitment to the aerospace and defense market.

Commitment to the Aerospace and Defense Market

Xilinx understands that our customers need to be able to count on their suppliers to be around for the long-term. Xilinx is committed to the long-term support of the aerospace and defense market, and we are continually expanding our product portfolio. Because our focus is in the form of a vertical market concept, we are able to provide emphasis on all of our customer's product requirements.

Table 1: High Density High Performance and Radiation Hardened Products

Family	Devices	Features
XC/XQ4000/E/EX	XC4005/E XC4010/E XC4013/E XC4025E XQ4028EX	• 5,000-28,000+ gates • Up to 256 user-definable I/Os • Extensive system features include on-chip user RAM, built-in 1149.1 test support and fast carry logic
XQ4000XL	XQ4013XL XQ4036XL XQ4062XL	• Up to 130,000 system gates • 3.3 V, 5V-compatible I/O
XQR4000XL Radiation Hardened	XQR4013XL XQR4036XL XQR4062XL	• Up to 130,000 System Gates • 60K Rads total dose, latchup immune
Virtex	XQV100 XQV300 XQV600 XQV1000	• Up to 1,000,000 System Gates, 2.5V
Virtex Radiation Hardened	XQVR300 XQVR600 XQVR1000	• 100K Rads Total Dose, Latchup Immune

Revision Control

Date	Version	Description
1/98	1.1	Version 1.1 -- High-Reliability and QML Military Products, correct erroneous information page 2 “XC3000 Products”, delete last page, table - “Mil-PRF-3853 QML, Xilinx M Grade and Plastic Commercial Flows”
11/98	1.2	Version 1.2 - Added new products, corrected XC3000, XC4000 products.
02/02/00	2.0	Updated Introduction and product listing.

QPRO Virtex 2.5V QML High-Reliability FPGAs

DS002 (v1.0) October 4, 1999

Preliminary Product Specification

Features

- Certified to MIL-PRF-38535 (Qualified Manufacturer Listing)
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Ceramic and Plastic Packages
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22 µm 5-layer metal process
- 100% factory tested

Description

The QPRO™ Virtex™ FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex family comprises the four members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

Table 1: QPRO Virtex Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQV100	108,904	20x30	2,700	180	40,960	38,400
XQV300	322,970	32x48	6,912	316	65,536	98,304
XQV600	661,111	48x72	15,552	316	98,304	221,184
XQV1000	1,124,022	64x96	27,648	404	131,072	393,216

QPRO™ Virtex™ 2.5V Radiation Hardened FPGAs

DS028 (v1.0) February 9, 2000

Advance Product Specification

Features

- Radiation hardened FPGAs for space and satellite applications
- Guaranteed total ionizing dose to 100K Rad(si)
- Latch-up immune to LET = 125 MeV cm^2/mg
- SEU immunity achievable with recommended redundancy implementation
- Guaranteed over the full military temperature range (–55°C to +125°C)
- Fast, high-density Field-Programmable Gate Arrays
  - Densities from 100k to 1M system gates
  - System performance up to 200 MHz
  - Hot-swappable for Compact PCI
- Multi-standard SelectI/O™ interfaces
  - 16 high-performance interface standards
  - Connects directly to ZBTRAM devices
- Built-in clock-management circuitry
  - Four dedicated delay-locked loops (DLLs) for advanced clock control
  - Four primary low-skew global clock distribution nets, plus 24 secondary global nets
- Hierarchical memory system
  - LUTs configurable as 16-bit RAM, 32-bit RAM, 16-bit dual-ported RAM, or 16-bit Shift Register
  - Configurable synchronous dual-ported 4k-bit RAMs
  - Fast interfaces to external high-performance RAMs
- Flexible architecture that balances speed and density
  - Dedicated carry logic for high-speed arithmetic
  - Dedicated multiplier support
  - Cascade chain for wide-input functions
  - Abundant registers/latches with clock enable, and dual synchronous/asynchronous set and reset
  - Internal 3-state bussing
  - IEEE 1149.1 boundary-scan logic
  - Die-temperature sensing device
- Supported by FPGA Foundation™ and Alliance Development Systems
  - Complete support for Unified Libraries, Relationally Placed Macros, and Design Manager
  - Wide selection of PC and workstation platforms
- SRAM-based in-system configuration
  - Unlimited reprogrammability
  - Four programming modes
- 0.22 µm 5-layer epitaxial process

Description

The QPRO Virtex FPGA family delivers high-performance, high-capacity programmable logic solutions. Dramatic increases in silicon efficiency result from optimizing the new architecture for place-and-route efficiency and exploiting an aggressive 5-layer-metal 0.22 µm CMOS process. These advances make QPRO Virtex FPGAs powerful and flexible alternatives to mask-programmed gate arrays. The Virtex radiation hardened family comprises the three members shown in Table 1.

Building on experience gained from previous generations of FPGAs, the Virtex family represents a revolutionary step forward in programmable logic design. Combining a wide variety of programmable system features, a rich hierarchy of fast, flexible interconnect resources, and advanced process technology, the QPRO Virtex family delivers a high-speed and high-capacity programmable logic solution that enhances design flexibility while reducing time-to-market.

Refer to the "Virtex™ 2.5V Field Programmable Gate Arrays" commercial data sheet for more information on device architecture and timing specifications.

Table 1: QPRO Virtex Radiation Hardened Field-Programmable Gate Array Family Members.

Device	System Gates	CLB Array	Logic Cells	Maximum Available I/O	Block RAM Bits	Max Select RAM Bits
XQVR300	322,970	32x48	6,912	316	65,536	98,304
XQVR600	661,111	48x72	15,552	316	98,304	221,184
XQVR1000	1,124,022	64x96	27,648	404	131,072	393,216

QPRO™ XQ4000E/EX
QML High Reliability FPGAs

May 19, 1998 (Version 2.1)

Product Specification

XQ4000E/EX High-Reliability Features

- Certified to MIL-PRF-38535, appendix A QML (Qualified Manufacturers Listing)
- System featured Field-Programmable Gate Arrays
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - 8 global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12-mA sink current per XQ4000E/EX output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Backward Compatible with XC4000 Devices
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Available Speed Grades:
  - XQ4000E -3 for plastic packages only
  - -4 for ceramic packages only
  - XQ4028EX -4 for all packages

More Information

For more information refer to Xilinx XC4000E and XC4000X series Field Programmable Gate Arrays product specification. This datasheet contains pinout tables for XQ4010E only. Refer to Xilinx 1998 Databook for pinout tables for other devices. (Pinouts for XQ4000E/EX are identical to XC4000E/EX.)

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Table 1: XQ4000E/EX Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-Flops	Max. Decode Inputs per side	Max. User I/O	Packages
XQ4005E	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112	PG156, CB164
XQ4010E	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160	PG191, CB196, HQ208
XQ4013E	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	72	192	PG223, CB228, HQ240
XQ4025E	25,000	32,768	15,000 - 45,000	32 x 32	1,024	2,560	96	256	PG299, CB228
XQ4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1024	2560	96	256	PG299, CB228, HQ240, BG352

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

QPRO™ XQ4000XL Series QML High-Reliability FPGAs

DS029 (v1.2) February 9, 1999

XQ4000X Series Features

- Certified to MIL-PRF-38535 Appendix A QML (Qualified Manufacturer Listing)
- Ceramic and plastic packages
- Also available under the following standard microcircuit drawings (SMD)
  - XQ4013XL 5962-98513
  - XQ4036XL 5962-98510
  - XQ4062XL 5962-98511
  - XQ4085XL 5962-99575
- For more information contact the Defense Supply Center Columbus (DSCC)
  http://www.dscc.dla.mis/v/va/smd/smdsrch.html
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - SelectRAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System Performance beyond 50 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA Sink Current Per XQ4000XL Output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - - Interfaces to popular design environments
  - - Fully automatic mapping, placement and routing
  - - Interactive design editor for design optimization
- Highest Capacity — Over 130,000 Usable Gates
- Additional Routing Over XQ4000E
  - almost twice the routing capacity for high-density designs
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- 0.35 µm SRAM process

Introduction

XQ4000X Series high-performance, high-capacity Field Programmable Gate Arrays (FPGAs) provide the benefits of custom CMOS VLSI, while avoiding the initial cost, long development cycle, and inherent risk of a conventional masked gate array.

The result of thirteen years of FPGA design experience and feedback from thousands of customers, these FPGAs combine architectural versatility, on-chip Select-RAM memory with edge-triggered and dual-port modes, increased speed, abundant routing resources, and new, sophisticated soft-ware to achieve fully automated implementation of complex, high-density, high-performance designs.

Refer to the complete Commercial XC4000X Series Field Programmable Gate Arrays Data Sheet for more information on device architecture and timing, and the latest Xilinx databook for package pinouts other than the CB228 (included in this data sheet). (Pinouts for XQ4000XL device are identical to XC4000XL.)

QPRO™ XQR4000XL Radiation Hardened Field Programmable Gate Arrays

October 5, 1998 (Version 1.0)

Preliminary Product Specification

XQR4000XL Series Features

- Radiation Hardened FPGAs for space and satellite applications
- Guaranteed Total Ionizing Dose
- Latch-up Immune
- Low Soft Upset Rate
- Guaranteed to meet full electrical specifications over –55°C to +125°C
- Available in -3 speed
- System featured Field-Programmable Gate Arrays
  - Select-RAM™ memory: on-chip ultra-fast RAM with
    - synchronous write option
    - dual-port RAM option
  - Abundant flip-flops
  - Flexible function generators
  - Dedicated high-speed carry logic
  - Wide edge decoders on each edge
  - Hierarchy of interconnect lines
  - Internal 3-state bus capability
  - Eight global low-skew clock or signal distribution networks
- System Performance beyond 60 MHz
- Flexible Array Architecture
- Low Power Segmented Routing Architecture
- Systems-Oriented Features
  - IEEE 1149.1-compatible boundary scan logic support
  - Individually programmable output slew rate
  - Programmable input pull-up or pull-down resistors
  - 12 mA sink current per output
- Configured by Loading Binary File
  - Unlimited reprogrammability
- Readback Capability
  - Program verification
  - Internal node observability
- Development System runs on most common computer platforms
  - Interfaces to popular design environments
  - Fully automatic mapping, placement and routing
  - Interactive design editor for design optimization
- Highest capacity—over 130,000 usable gates
- Buffered Interconnect for Maximum Speed
- New Latch Capability in Configurable Logic Blocks
- Improved VersaRing™ I/O Interconnect for Better Fixed Pinout Flexibility
  - Virtually unlimited number of clock signals
- Optional Multiplexer or 2-input Function Generator on Device Outputs
- 5V tolerant I/Os
- Advanced 0.35µ process
- Processed on Xilinx's QML Line

Table 1: XQR4000X Series Radiation Hardened Field Programmable Gate Arrays

Device	Logic Cells	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total CLBs	Number of Flip-flops	Max. User I/O	Packages
XQR4013XL	1,368	13,000	18,432	10,000 - 30,000	24 x 24	576	1,536	192	CB228
XQR4036XL	3,078	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	288	CB228
XQR4062XL	5,472	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	384	CB228

Note: Max values of Typical Gate Range include 20-30% of CLBs used as RAM.

XC1700L Series High Density Serial Configuration PROMs Including XQ1701L QPRO™ Series

July 8, 1999 (Version 2.3)

Product Specification

Features

- Serial Configuration one-time programmable (OTP) read-only memory designed to store configuration bitstreams of Xilinx FPGA devices
- Simple interface to the FPGA; requires only one user I/O pin
- Cascadable for storing longer or multiple bitstreams
- Programmable reset polarity (active High or active Low) for compatibility with different FPGA solutions
- Supports XC4000EX/XL/XLA/XV fast configuration mode (15.0 MHz)
- Low-power CMOS Floating Gate process
- XC1704L, XC1702L, XC1701L, XQ1701L and the XC17512L are 3.3V devices
- XC1701 is a 5V device only
- Available in compact plastic packages: 8-pin PDIP, 20-pin SOIC, 20-pin PLCC, 44-pin PLCC or 44-pin VQFP.
- QPRO™ parts available in 44-pin ceramic LCC and 20-pin SOIC.
- Programming support by leading programmer manufacturers.
- Design support using the Xilinx Alliance and Foundation series software packages.

Description

The XC1704L, XC1702L, XC1701L, and the XC17512L are Xilinxs 3.3V series of high density serial configuration PROMs (SPROMs). Included within this family are the XC1701 (5V) and the XQ1701L (3.3V) SPROMs to provide an easy-to-use, cost-effective method for storing large Xilinx FPGA configuration bitstreams.

When the FPGA is in Master Serial mode, it generates a configuration clock that drives the SPROM. A short access time after the rising clock edge, data appears on the SPROM DATA output pin that is connected to the FPGA DIN pin. The FPGA generates the appropriate number of clock pulses to complete the configuration. Once configured, it disables the SPROM. When the FPGA is in Slave Serial mode, the SPROM and the FPGA must both be clocked by an incoming signal.

Multiple devices can be concatenated by using the $\overline{CEO}$ output to drive the $\overline{CE}$ input of the following device. The clock inputs and the DATA outputs of all SPROMs in this chain are interconnected. All devices are compatible and can be cascaded with other members of the family.

For device programming, either the Xilinx Alliance or Foundation series development system compiles the FPGA design file into a standard Hex format, which is then transferred to most commercial PROM programmer.

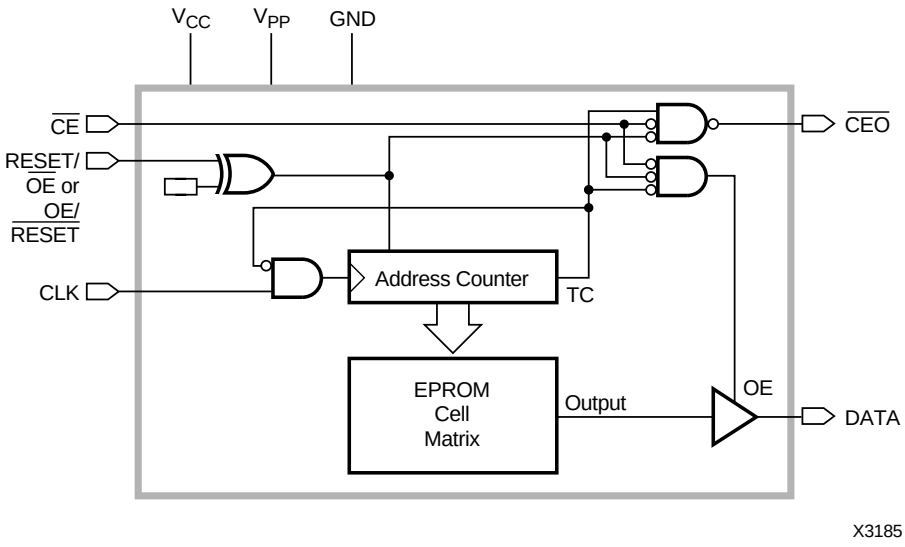


Figure 1: Simplified Block Diagram (does not show programming circuit)

Packages and Thermal Characteristics

Packages and Thermal Characteristics Table of Contents

Packages and Thermal Characteristics

Package Drawing

For complete Package Drawing information, refer to CD-ROM or Xilinx web site:
www.xilinx.com/partinfo/databook.htm

February 15, 2000 (Version 2.1)

Package Information

Inches vs. Millimeters

The JEDEC standards for PLCC, CQFP, and PGA packages define package dimensions in inches. The lead spacing is specified as 25, 50, or 100 mils (0.025", 0.050" or 0.100").

The JEDEC standards for PQFP, HQFP, TQFP, and VQFP packages define package dimensions in millimeters. These packages have a lead spacing of 0.5 mm, 0.65 mm, or 0.8 mm.

Because of the potential for measurement discrepancies, this Data Book provides measurements in the controlling standard only, either inches or millimeters. (See Table 1 for package dimensions.)

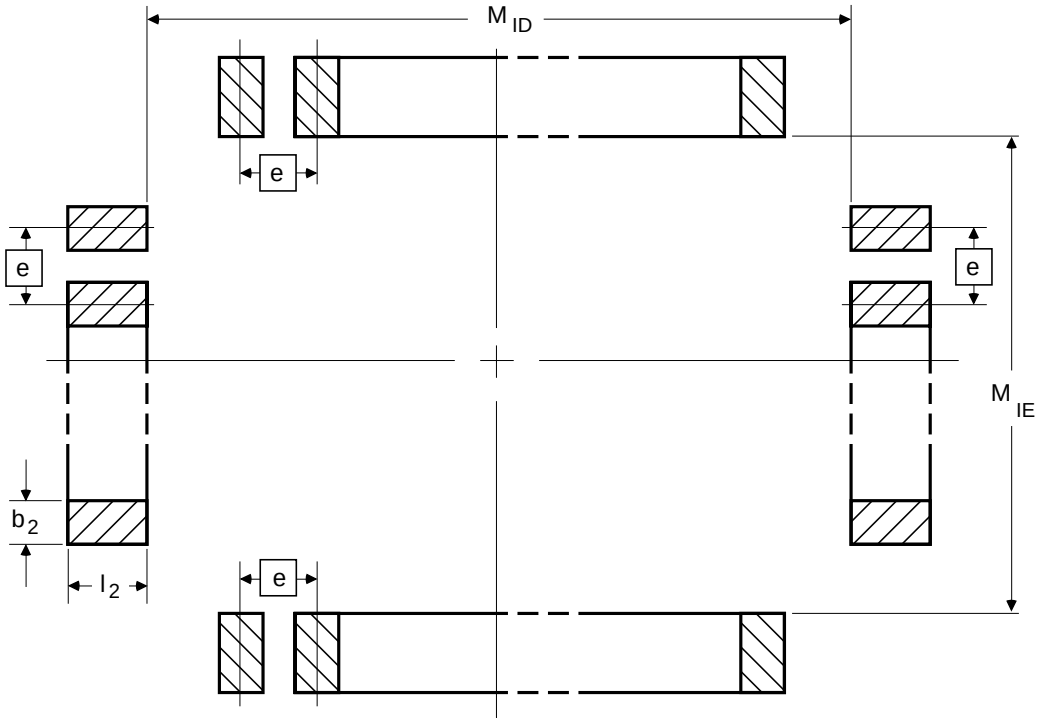


Figure 1: EIA Standard Board Layout of Soldered Pads for QFP Devices

Table 1: Dimensions for Xilinx Quad Flat Packs(1)

Dim.	VQ44	VQ64	PQ100	HQ160 PQ160	HQ208 PQ208	VQ100 TQ100	TQ144	TQ176	HQ240 PQ240	HQ304
M_{ID}	9.80	9.80	20.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
M_{IE}	9.80	9.80	14.40	28.40	28.20	13.80	19.80	23.80	32.20	40.20
e	0.80	0.50	0.65	0.65	0.50	0.50	0.50	0.50	0.50	0.50
b_2	0.4 - 0.6	0.3 - 0.4	0.3 - 0.5	0.3 - 0.5	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4	0.3 - 0.4
l_2	1.60	1.60	1.80[2]	1.80	1.60	1.60	1.60	1.60	1.60	1.60

Notes: 1. Dimensions in millimeters
2. For 3.2 mm footprint per MS022, JEDEC Publication 95.

Suggested Board Layout of Soldered Pads for BGA, CS and FG Packages

Suggested Board Layout of Soldered Pads for BGA, CS and FG Packages

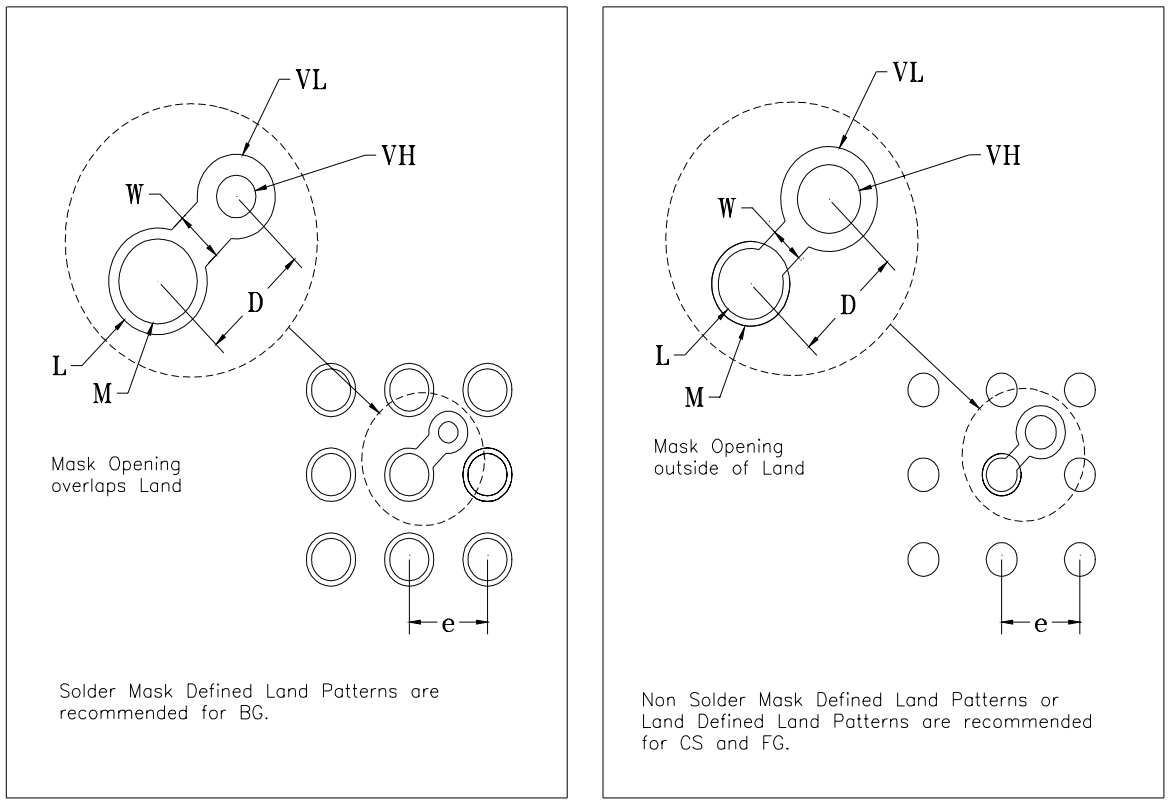


Figure 2: Suggested Board Layout of Soldered Pads for BGA, CS and FG Packages

Table 2: Soldering Dimensions for BG, CS, and FG Packages

	BG225	*BG256	BG352	BG432	BG560	CS48	CS144	CS280
Solder Land (**L**) diameter	0.89	0.79	0.79	0.79	0.79	0.33	0.33	0.33
Opening in Solder Mask (**M**) diameter	0.65	0.58	0.58	0.58	0.58	0.44	0.44	0.44
Solder (Ball) Land Pitch (**e**)	1.5	1.27	1.27	1.27	1.27	0.8	0.8	0.8
Line Width between Via and Land (w)	0.3	0.3	0.3	0.3	0.3	0.13	0.13	0.13
Distance between Via and Land (D)	1.06	0.9	0.9	0.9	0.9	0.56	0.56	0.56
Via Land (VL) diameter	0.65	0.65	0.65	0.65	0.65	0.51	0.51	0.51
Through Hole (VH) diameter	0.3	0.3	0.3	0.3	0.3	0.25	0.25	0.25
Pad Array	Full	-	-	-	-	-	-	-
Matrix or External Row	15 x 15	20 x 20	26 x 26	31 x 31	33 x 33	7 x 7	13 x 13	19 x 19
Periphery rows	-	4	4	4	5	3	4	5
	FG256	**FG456**	**FG556**	**FG676**	**FG680**	**FG860**	**FG900**	**FG1156**
Solder Land (**L**) diameter	0.4	0.4	0.4	0.4	0.4	0.4	0.4	0.4
Opening in Solder Mask (**M**) diameter	0.5	0.5	0.5	0.5	0.5	0.5	0.5	0.5
Solder (Ball) Land Pitch (**e**)	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0
Line Width between Via and Land (w)	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13
Distance between Via and Land (D)	0.7	0.7	0.7	0.7	0.7	0.7	0.7	0.7
Via Land (VL) diameter	0.61	0.61	0.61	0.61	0.61	0.56	0.61	0.61
Through Hole (VH), diameter	0.3	0.3	0.3	0.3	0.3	0.3	0.3	0.3
Pad Array	Full	Full	-	Full	-	-	Full	Full
Matrix or External Row	16 x 16	22 x 22	30 x 30	26 x 26	39 x 39	42 x 42	30 x 30	34 x 34

Table 2: Soldering Dimensions for BG, CS, and FG Packages

Periphery rows	-	-	7	-	5	6	-	-

Cavity Up or Cavity Down

Most Xilinx devices attach the die against the inside bottom of the package (the side that does not carry the Xilinx logo). This is called cavity-up, and has been the standard IC assembly method for over 25 years. This method does not provide the best thermal characteristics. Pin Grid Arrays (greater than 130 pins) and Ceramic Quad Flat Packs are assembled "Cavity Down", with the die attached to the inside top of the package, for optimal heat transfer to the ambient air.

For most packages this information does not affect how the package is used because the user has no choice in how the package is mounted on a board. For Ceramic Quad Flat Pack (CQFP) packages however, the leads can be formed to either side. Therefore, for best heat transfer to the surrounding air, CQFP packages should be mounted with the logo up, facing away from the PC board.

Clockwise or Counterclockwise

The orientation of the die in the package and the orientation of the package on the PC board affect the PC board layout. PLCC and PQFP packages specify pins in a counterclockwise direction, when viewed from the top of the package (the surface with the Xilinx logo). PLCCs have pin 1 in the center of the beveled edge while all other packages have pin 1 in one corner, with one exception: The 100- and 165-pin CQFPs (CB100 and CB164) for the XC3000 devices have pin 1 in the center of one edge.

CQFP packages specify pins in a clockwise direction, when viewed from the top of the package. The user can make the pins run counterclockwise by forming the leads such that the logo mounts against the PC board. However, heat flow to the surrounding air is impaired if the logo is mounted down.

Thermal Management

Modern high speed logic devices consume an appreciable amount of electrical energy. This energy invariably turns into heat. Higher device integration drives technologies to produce smaller device geometry and interconnections. With smaller chip sizes and higher circuit densities, heat generation on a fast switching CMOS circuit can be very significant. The heat removal needs for these modern devices must be addressed.

Managing heat generation in a modern CMOS logic device is an industry-wide pursuit. However, unlike the power needs of a typical Application Specific Integrated Circuit (ASIC) gate array, the power requirements for FPGAs are not determined as the device leaves the factory. Designs vary in power needs.

There is no way of anticipating the power needs of an FPGA device short of depending on compiled data from previous designs. For each device type, primary packages are chosen to handle "typica" designs and gate utilization requirements. For the most part the choice of a package as the primary heat removal casing works well.

Occasionally designers exercise an FPGA device, particularly the high gate count variety, beyond "typical" designs. The use of the primary package without enhancement may not adequately address the device's heat removal needs. Heat removal management through external means or an alternative enhanced package should be considered.

Removing heat ensures the functional and maximum design temperature limits are maintained. The device may go outside the temperature limits if heat build up becomes excessive. As a consequence, the device may fail to meet electrical performance specifications. It is also necessary to satisfy reliability objectives by operating at a lower temperature. Failure mechanisms and the failure rate of devices depend on device operating temperature. Control of the package and the device temperature ensures product reliability.

Package Thermal Characterization Methods & Conditions

Method and Calibration

Xilinx uses the indirect electrical method for package thermal resistance characterization. The forward-voltage drop of an isolated diode residing on a special test die is calibrated at constant forcing current of 0.520mA with respect to temperature over a correlation temperature range of 22°C to 125°C (degree Celsius). The calibrated device is then mounted in an appropriate environment (still air, forced convection, circulating FC-40, etc.) Depending on the package, between 0.5 to 4 watts of power (Pd) is applied. Power (Pd) is applied to the device through diffused resistors on the same thermal die. The resulting rise in junction temperature is monitored with the forward-voltage drop of the precalibrated diode. Typically, three identical samples are tested at each data point. The reproducibility error in the set-up is within 6%.

Definition of Terms

T_J Junction Temperature — the maximum temperature on the die, expressed in °C (degree Celsius)

T_A Ambient Temperature — expressed in °C.

T_C The temperature of the package body taken at a defined location on the body. This is taken at the pri-

mary heat flow path on the package and represents the hottest part on the package — expressed in °C.

T_I The isothermal fluid temperature when junction to case temperature is taken — expressed in °C.

P_d The total device power dissipation — expressed in watts.

Junction-to-Reference General Setup

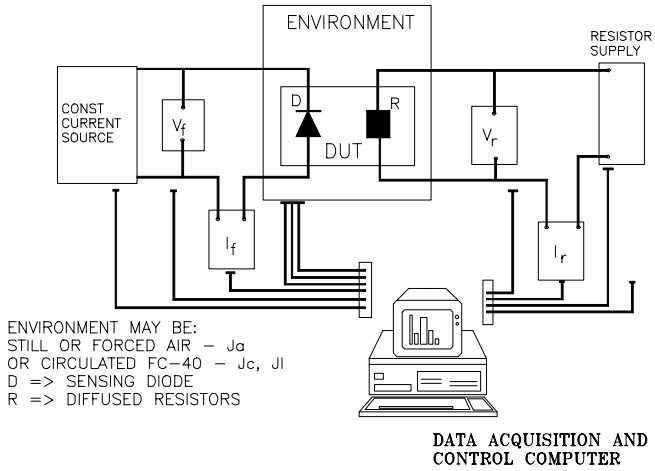


Figure 3: Thermal Measurement Set-Up (Schematic for Junction to Reference)

Junction-to-Case Measurement — Θ_{JC}

Θ_{JC} is measured in a 3M Flourinert (FC-40) isothermal circulating fluid stabilized at 25°C. The Device Under Test (DUT) is completely immersed in the fluid and initial stable conditions are recorded. **Pd** is then applied. Case temperature **(T_C)** is measured at the primary heat-flow path of the particular package. Junction temperature **(T_J)** is calculated from the diode forward-voltage drop from the initial stable condition before power was applied.

$$\Theta_{JC} = (T_J - T_C)/Pd$$

The junction-to-isothermal-fluid measurement **(Θ_{JI})** is also calculated from the same data.

$$\Theta_{JL} = (T_J - T_I)/Pd$$

The latter data is considered as the ideal Θ_{JA} data for the package that can be obtained with the most efficient heat removal scheme. Other schemes such as airflow, heatsinks, use of copper clad board, or some combination of all these will tend towards this ideal figure. Since this is not a widely used parameter in the industry, and it is not very realistic for normal application of Xilinx packages, the Θ_{JI} data is not published. The thermal lab keeps such data for package comparisons.

Junction-to-Ambient Measurement — Θ_{JA}

Θ_{JA} is measured on FR4 based PC boards measuring 4.5" x 6.0" x .0625" (114.3mm x 152.4mm x 1.6mm) with edge connectors. There are two main board types.

Type I, 2L/0P board, is single layer with 2 signal planes (one on each surface) and no internal Power/GND planes. The trace density on this board is less than 10% per side. Type II, the 4L/2P board, has 2 internal copper planes (one power, one ground) and 2 signal trace layers on both surfaces.

Data may be taken with the package mounted in a socket or with the package mounted directly on the board. Socket measurements typically use the 2L/0P boards. SMT devices may use either board. Published data always reflects the board and mount conditions used.

Data is taken at the prevailing temperature and pressure conditions (22°C to 25°C ambient). The board with the DUT is mounted in a cylindrical enclosure. The power application and signal monitoring are the same as Θ_{JC} measurements. The enclosure (ambient) thermocouple is substituted for the fluid thermocouple and two extra thermocouples brought in to monitor room and board temperatures. The junction to ambient thermal resistance is calculated as follows:

$$\Theta_{JA} = (T_J - T_A)/Pd$$

The setup described herein lends itself to the application of various airflow velocities from 0 - 800 Linear Feet per Minute (LFM), i.e., 0 - 4.06 m/s. Since the board selection (copper trace density, absence or presence of ground planes, etc.) affects the results of the thermal resistance, the data from these tests shall always be qualified with the board mounting information.

Data Acquisition and Package Thermal Database

Xilinx gathers data for a package type in die sizes, power levels and cooling modes (air flow and sometimes heatsink effects) with a Data Acquisition and Control system (DAS). The DAS controls the power supplies and other ancillary equipment for hands-free data taking. Different setups within the DAS software are used to run calibration, Θ_{JA}, Θ_{JC}, fan tests, as well as the power effect characteristics of a package.

A package is characterized with respect to the major variables that influence the thermal resistance. The results are stored in a database. Thermal resistance data is interpolated as typical values for the individual Xilinx devices that are assembled in the characterized package. Table 3 shows the typical values for different packages. Specific device data may not be the same as the typical data. However, the data will fall within the given minimum and maximum ranges. The more widely used packages will have a wider range. Customers may contact the Xilinx application group for specific device data.

Table 3: Summary of Thermal Resistance for Packages

PKG-CODE	Θ_{JA} still air (Max)	Θ_{JA} still air (Typ)	Θ_{JA} still air (Min)	Θ_{JA} 250 LFM (Typ)	Θ_{JA} 500 LFM (Typ)	Θ_{JA} 750 LFM (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
BG225	37	30	24	19	17	16	3.3	Various
BG256	32	29	24	19	17	16	3.2	4L/2P-SMT
BG352	14	12	10	8	7	6	0.8	4L/2P-SMT
BG432	13	11	9	8	6	6	0.8	4L/2P-SMT
BG560	10	9	8	7	6	5	0.8	Estimated
CB100	44	41	38	25	19	17	5.1	Socketed
CB164	29	26	25	17	12	11	3.6	Socketed
CB196	25	24	24	15	11	10	1.8	Socketed
CB228	19	18	17	11	8	7	1.3	Socketed
CS48		45						Estimated
CS144		65						Estimated
DD8	114	109	97	90	73	60	8.2	Socketed
HQ160	14	14	14	10	8	7	1.0	4L/2P-SMT
FG256	27	25	23	21	20	19	3.9	4L/2P-SMT
FG456	19	18	17	14	13	13	1.5	4L/2P-SMT
FG556	14	14	14	10	9	9	0.8	4L/2P-SMT
FG676	17	17	17	13	12	12	0.9	4L/2P-SMT
FG680	11	11	10	8	6	6	0.9	4L/2P-SMT
FG860	10	10	10	7	6	5	0.8	4L/2P-SMT
FG900	14	14	14	10	9	9	0.8	Estimated
FG1156	14	13	13	10	9	9	0.8	Estimated
HQ208	15	14	14	10	8	7	1.7	4L/2P-SMT
HQ240	13	12	12	9	7	6	1.5	4L/2P-SMT
HQ304	11	11	10	7	5	5	0.9	4L/2P-SMT
HT144	-	10.9	-	7.3	5.7	5.0	0.9	4L/2P-SMT
HT176	-	16.0	-	-	-	-	2.0	Estimated
PC20	86	84	76	63	56	53	25.8	2L/0P-SMT
PC44	51	46	42	35	31	29	13.7	2L/0P-SMT
PC68	46	42	38	31	28	26	9.3	2L/0P-SMT
PC84	41	33	28	25	21	17	5.3	2L/0P-SMT
PD8	82	79	73	60	54	50	22.2	Socketed
PG84	37	34	31	24	18	16	5.8	Socketed
PG120	32	27	25	19	15	13	3.6	Socketed
PG132	32	28	24	20	17	15	2.8	Socketed
PG156	25	23	21	15	11	10	2.6	Socketed
PG175	25	23	20	14	11	10	2.6	Socketed
PG191	24	21	18	15	12	11	1.5	Socketed
PG223	24	20	18	15	12	11	1.5	Socketed
PG299	18	17	16	10	9	8	1.9	Socketed
PG411	16	15	14	9	8	7	1.2	Socketed
PG475	14	13	12	9	8	7	1.2	Socketed
PG559	-	12.00	-	-	-	-	-	Estimated
PP132	35	34	33	23	18	17	6.0	Socketed

Table 3: Summary of Thermal Resistance for Packages (Continued)

PKG-CODE	Θ_{JA} still air (Max)	Θ_{JA} still air (Typ)	Θ_{JA} still air (Min)	Θ_{JA} 250 LFM (Typ)	Θ_{JA} 500 LFM (Typ)	Θ_{JA} 750 LFM (Typ)	Θ_{JC} (Typ)	Comments
	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	°C/Watt	
PP175	29	29	28	19	15	13	2.5	Socketed
PQ100	35	33	32	29	28	27	5.5	4L/2P-SMT
PQ160	37	32	22	24	21	20	4.6	2L/0P-SMT
PQ208	35	32	26	23	21	19	4.3	2L/0P-SMT
PQ240	28	23	19	17	15	14	2.8	2L/0P-SMT
SO8	147	147	147	112	105	98	48.3	IEEE-(Ref)
TQ100	37	31	31	26	24	23	7.5	4L/2P-SMT
TQ144	35	32	30	25	21	20	5.3	4L/2P-SMT
TQ176	29	28	27	21	18	17	5.3	4L/2P-SMT
VO8	162	162	162	123	116	108	48.3	Estimated
VQ44	44	44	44	36	34	33	8.2	4L/2P-SMT
VQ64	44	41	39	34	32	31	8.2	4L/2P-SMT
VQ100	47	38	32	32	30	29	9.0	4L/2P-SMT

Notes:
1. Maximum, typical and minimum numbers are based on numbers for all the devices in the specific package at the time of compilation. The numbers do not necessarily reflect the absolute limits of that packages. Specific device data should lie within the limits. Packages used for a broader spectrum of devices have a wider range in the table. Specific device data in a package may be obtained from the factory.
2. Package configurations and drawings are in the package section of the data book.
3. 2L/0P - SMT: the data is from a surface mount type I board -- no internal planes on the board.
4. 4L/2P - SMT: the data is from a 4 layer SMT board incorporating 2 internal planes. Socketed data is taken in socket.
5. Air flow is given Linear Feet per Minute (LFM). 500 LFM = 2.5 Meters per Second

Application of Thermal Resistance Data

Thermal resistance data gauges the IC package thermal performance. Θ_{JC} measures the internal package resistance to heat conduction from the die surface, through the die mount material to the package exterior. Θ_{JC} strongly depends on the package's heat conductivity, architecture and geometrical considerations.

Θ_{JA} measures the total package thermal resistance including Θ_{JC}. Θ_{JA} depends on the package material properties and such external conditions as convective efficiency and board mount conditions. For example, a package mounted on a socket may have a Θ_{JA} value 20% higher than the same package mounted on a 4 layer board with power and ground planes.

By specifying a few constraints, devices are ensured to operate within the intended temperature range. This also ensures device reliability and functionality. The system ambient temperature needs to be specified. A maximum T_J also needs to be established for the system. The following inequality will hold.

$$\mathbf{T_J(max) > \Theta_{JA} * Pd + T_A}$$

The following two examples illustrates the use of this inequality.

Example 1:

The manufacturer's goal is T_J (max) < 100°C

A module is designed for a T_A = 45°C max.

A XC3042 in a PLCC 84 has a Θ_{JA} = 32°C/watt.

Given a XC3042 with a logic design with a rated power Pd of 0.75watt.

With this information, the maximum die temperature can be calculated as:

T_J = 45 + (32 x .75) ==> 69°C.

The system manufacturer's goal of T_J < 100°C is met.

Example 2:

A module has a T_A = 55°C max.

The Xilinx XC4013E is in a PQ240 package (HQ240 is also considered).

A XC4013E, in an example logic design, has a rated power of 2.50 watts. The module manufacturers goal is T_J(max.) < 100°C.

Table 4 shows the package and thermal enhancement combinations required to meet the goal of T_J < 100°C.

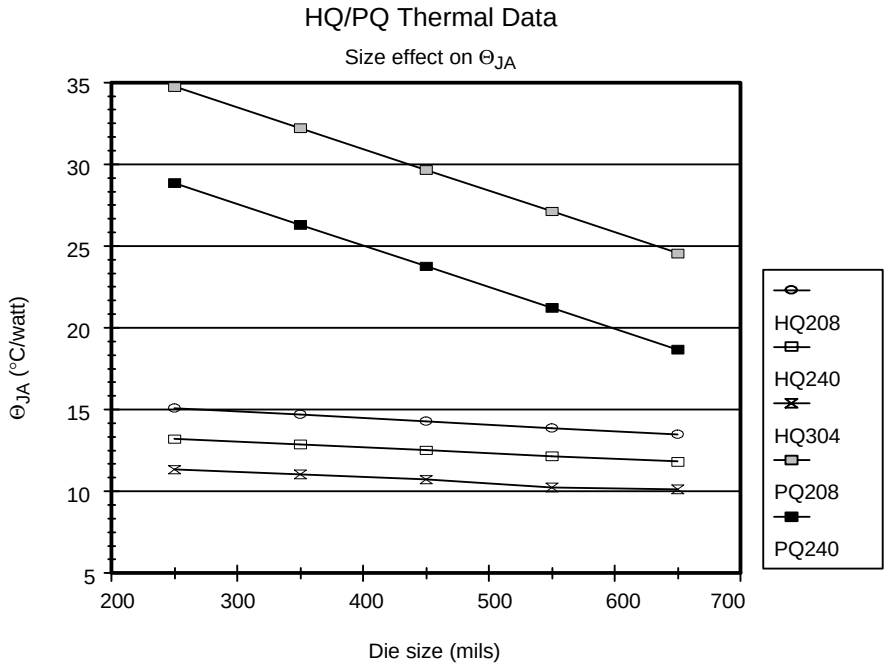
Table 4: Thermal Resistance for XC4013E in PQ240 and HQ240 Packages

Device Name	Package	Θ_{JA} still air	Θ_{JA} (250 LFM)	Θ_{JA} (500 LFM)	Θ_{JA} (750 LFM)	Θ_{JC}	Comments
XC4013E	PQ240	23.7	17.5	15.4	14.3	2.7	Cu, SMT 2L/0P
XC4013E	HQ240	12.5	8.6	6.9	6.2	1.5	4 Layer Board data

Notes: Possible Solutions to meet the module requirements of 100°C :
1a.Using the standard PQ240; T_J = 55 + (23.7 x 2.50) ==> 114.25 °C.
1b.Using standard PQ240 with 250LFM forced air; T_J = 55 + (17.5 x 2.50) ==> 98.75 °C
2a.Using standard HQ240T_J = 55 + (12.5 x 2.50) ==> 86.25 °C
2b.Using HQ240 with 250 LFM forced air; T_J = 55 + (8.6 x 2.50) ==> 76.5 °C

For all solutions, the junction temperature is calculated as: T_J = Power x Θ_{JA} + T_A. All solutions meet the module requirement of less than 100°C, with the exception of the PQ240 package in still air. In general, depending on ambient and board temperatures conditions, and most importantly the total power dissipation, thermal enhancements -- such as forced air cooling, heat sinking, etc. may be necessary to meet the T_J(max) conditions set.

PQ/HQ Thermal Data Comparison



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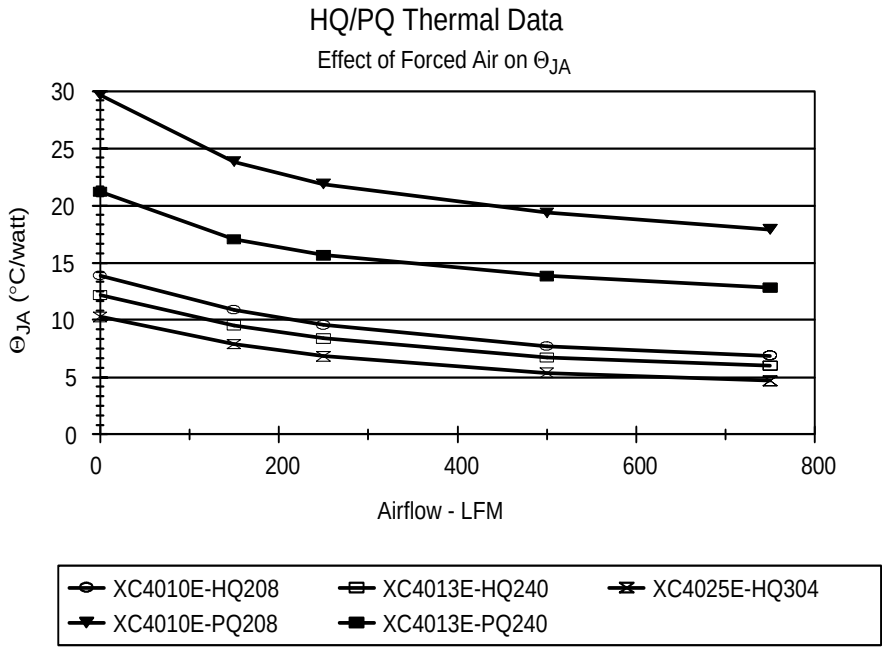
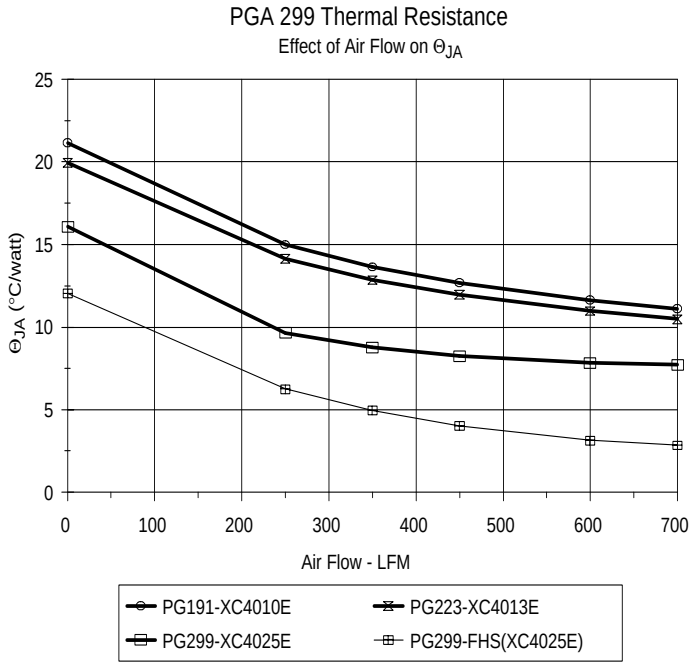
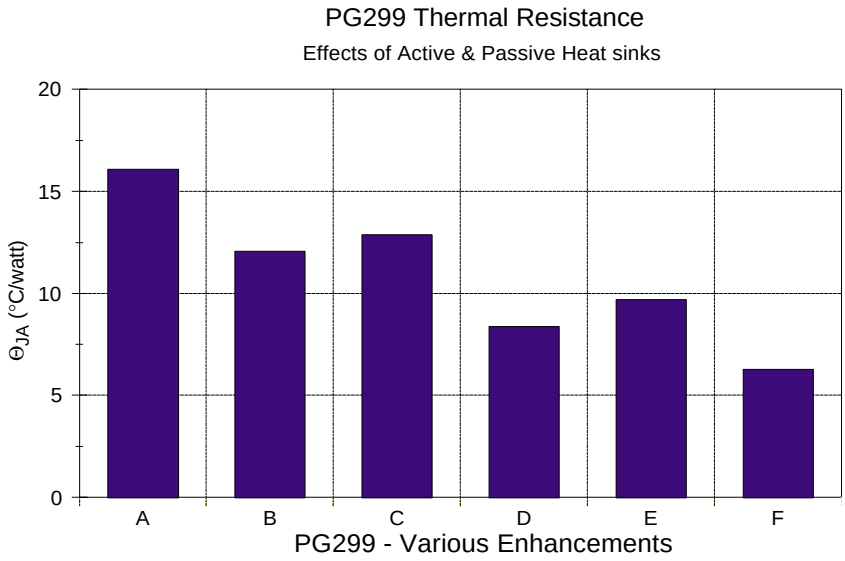
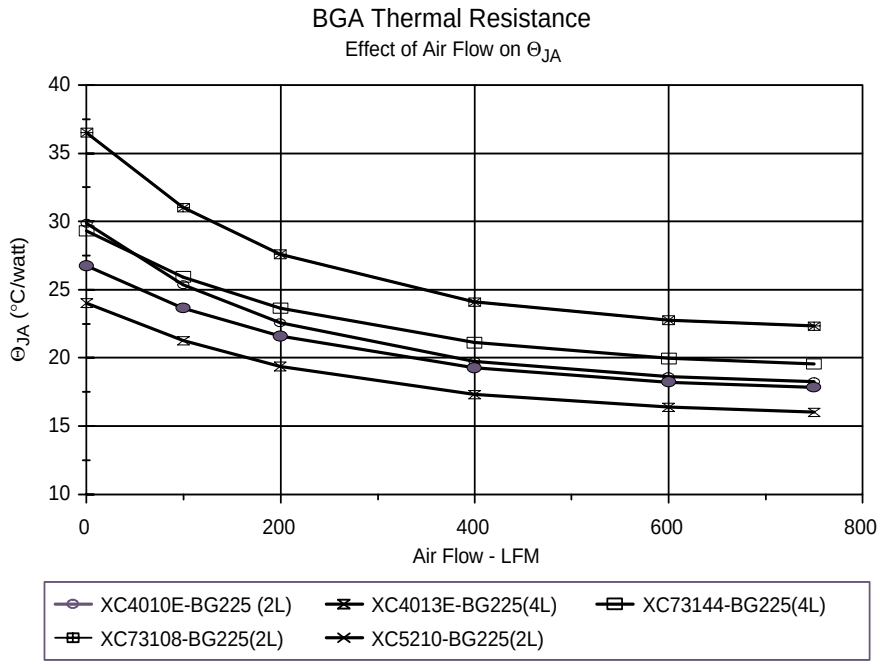

HQ/PQ Thermal Data
Effect of Forced Air on ΘJA
ΘJA (°C/watt)
30
25
20
15
10
5
0
0
200
400
600
800
Airflow - LFM
XC4010E-HQ208
XC4013E-HQ240
XC4025E-HQ304
XC4010E-PQ208
XC4013E-PQ240


PGA 299 Thermal Resistance
Effect of Air Flow on ΘJA
ΘJA (°C/watt)
25
20
15
10
5
0
0
100
200
300
400
500
600
700
Air Flow - LFM
PG191-XC4010E
PG223-XC4013E
PG299-XC4025E
PG299-FHS(XC4025E)



A Standard Pkg
B Pkg+Finned HS (Passive)
C Pkg+Active Fan (V=0)
D Pkg+Active Fan (V=12)
E Std Pkg +250LFM
F Pkg+Finned HS+ 250LFM



8

Some Power Management Options

FPGA devices are usually not the dominating power consumers in a system, and do not have a big impact on power supply designs. There are obvious exceptions. When the actual or estimated power dissipation appears to be more than the specification of the chosen package, some options can be considered. Details on the engineering designs and analysis of some of these suggested considerations may be obtained from the references listed at the end of the section. The options include:

- A Xilinx low power (L) version of the circuit in the same package. With the product and speed grade of choice, up to a 40% power reduction can be anticipated. For more information, contact the Xilinx Hotline group.
- Explore thermally enhanced package options available for the same device. As illustrated above, the HQ240 package has a thermal impedance of about 50% of the equivalent PQ240. Besides, the 240 lead, the 208 lead and the 304 lead Quad packages have equivalent heatsink enhanced versions. Typically 25% to 40% improvement in thermal performance can be expected from these heatsink enhanced packages. Most of the high gate count devices above the XC4013 level come either exclusively in heat enhanced packages or have these packages as options. If the use of a standard PQ appears to be a handicap in this respect, a move to the equivalent HQ package if available may resolve the issue. The heat enhanced packages are pin to pin compatible and they use the same board layout.
- The use of forced air is an effective way to improve thermal performance. As seen on the graphs and the calculations above, forced air (200 -- 300 LFM) can reduce junction to ambient thermal resistance by 30%.
- If space will allow, the use of finned external heatsinks can be effective. If implemented with forced air as well, the benefit can be a 40% to 50% reduction. The HQ304, all cavity down PGAs, and the BG352 with exposed heatsink lend themselves to the application of external heatsinks for further heat removal efficiency.
- Outside the package itself, the board on which the package sits can have a significant impact. Board designs may be implemented to take advantage of this. Heat flows to the outside of a board mounted package and is sunk into the board to radiate. The effect of the board will be dependent on the size and how it conducts heat. Board size, the level of copper traces on it, the number of buried copper planes all lower the junction-to-ambient thermal resistance for a package. Some of the heatsink packages with the exposed heatsink on the board side can be glued to the board with thermal compound to enhance heat removal.

References

Forced Air Cooling Application Engineering

COMAIR ROTRON
2675 Custom House Court
San Ysidro, CA 92173
1-619-661-6688

Heatsink Application Engineering

The following facilities provide heatsink solutions for industry standard packages.

AAVID Thermal Technologies
1 Kool Path
Box 400
Laconia, NH 03247-0400
1-603-528-3400

Thermalloy, Inc.
2021 W. Valley View Lane
Box 810839
Dallas, TX 75381-0839
1-214-243-4321

Wakefield Engineering, Inc.
60 Audubon Road
Wakefield MA 01880-1255
1-617-245-5900

Xilinx does not endorse these vendors nor their products. They are listed here for reference only. Any materials or services received from the vendors should be evaluated for compatibility with Xilinx components.

Package Electrical Characterization

In high-speed systems, the effects of electrical package parasitics become very critical when optimizing for system performance. Such problems as ground bounce and crosstalk can occur due to the inductance, capacitance, and resistance of package interconnects. In digital systems, such phenomena can cause logic error, delay, and reduced system speed. A solid understanding and proper usage of package characterization data during system design simulation can help prevent such problems.

Theoretical Background

There are three major electrical parameters which are used to describe the package performance: resistance, capacitance, and inductance. Also known as interconnect parasitics, they can cause many serious problems in digital systems. For example, a large resistance can cause RC & RL off-chip delays, power dissipation, and edge-rate degradation. Large capacitance can cause RC delays, crosstalk, edge-rate degradation, and signal distortion. The lead inductance, perhaps the most damaging parasitic in digital

circuitry, can cause such problems as ground bounce (also known as simultaneous switching noise or delta-I noise), RL delays, crosstalk, edge rate degradation, and signal distortion.

Ground bounce is the voltage difference between any two grounds (typically between an IC and circuit board ground) induced by simultaneously switching current through bondwire, lead, or other interconnect inductance.

When IC outputs change state, large current spikes result from charging or discharging the load capacitance. The larger the load capacitance and faster the rise/fall times, the larger the current spikes are: I = C * dv/dt. Current spikes through the IC pin and bondwire induces a voltage drop across the leads and bondwires: V = L * di/dt. The result is a momentary voltage difference between the internal IC ground and system ground, which show up as voltage spikes and unswitched outputs.

Factors that affect ground bounce:

- rise and fall times
- load capacitance
- package inductance
- number of output drivers sharing the same ground path
- device type

Analytical Formulas for Lead Inductance

1. Rectangular Leadframe/Trace (straight)

$$L_{self} = 5l\left[\ln\left(\frac{2l}{w+t}\right)+\frac{1}{2}\right] \text{ nH}$$
(no ground)

$$L_{self} = 5l\left[\ln\left(\frac{8h}{w+t}\right)+\left(\frac{w+t}{4h}\right)\right] \text{ nH}$$
(above ground)

l = lead/trace length
w = lead/trace width
t = lead/trace thickness
h = ground height
unit = inches

2. Bondwire (gold wire)

$$L_{wire} = 5l\left[\ln\left(\frac{2l}{r}\right)-\frac{3}{4}\right] \text{ nH}$$

L = wire length
r = wire radius
unit = inches

General Measurement Procedure

Xilinx uses the Time-Domain Reflectometry (TDR) method for parasitic inductance and capacitance measurements. The main components of a TDR setup includes: a digitizing sampling oscilloscope, a fast rise time step generator (<17 ps), a device-under-test (DUT) interface, and an impedance-profile analysis software to extract parasitic models from the TDR reflection waveforms. In this method, a voltage step is propagated down the package under test, and the incident and reflected voltage waves are monitored by the oscilloscope at a particular point on the line. The resulting characteristic impedance of the package interconnect shows the nature (resistive, inductive, and capacitive) of each discontinuity.

Package and Fixture Preparation

Before performing the measurements, the package and the DUT interface must be fixtured. Proper fixturing ensures accurate and repeatable measurements. The mechanical sample for all inductance (self & mutual) measurements are finished units with all leads shorted to the internal ground. For packages without an internal ground (i.e. QFP, PLCC, etc.) the die-paddle is used instead. The mechanical sample for all capacitance (self & mutual) measurements are finished units with all internal leads floating. The DUT interface provides a physical connection between the oscilloscope and the DUT with minimum crosstalk and probe/DUT reflection. It also provides small ground loop to minimize ground inductance of the fixture.

Inductance and Capacitance Measurement Procedure

For inductance measurements, a minimum of 25% and maximum of 50% of packages leads, including all leads that are adjacent to the lead(s) under test, are insulated from the DUT fixture ground. All other leads, except for the lead(s) under test, are grounded. This insulation forces the current to return through a low impedance path created on the opposite side of the package. It also eliminates mutual coupling from the neighboring leads. Self-inductance is measured by sending a fast risetime step waveform through the lead under test. The inductive reflection waveform through the lead and the bondwire is then obtained. This reflection waveform, which includes the inductance of the die-paddle (for QFP and PLCC-type packages) and parallel combination of leads in the return path, is the self-inductance. The parasitic effects of the return path are small enough to ignore in the context of this method. For mutual-inductance measurement, two adjacent leads are probed. A fast risetime step waveform is sent through one of the leads. The current travels through the lead/bondwire and returns by the path of the low-impedance ground. On the adjacent “quiet” lead, a waveform is induced due to mutual coupling. This waveform is measured as the mutual inductance.

For capacitance measurements, all external leads except for the lead(s) under test are grounded to the DUT fixture. For QFP, PLCC, and Power Quad-type of packages, the die-paddle and the heat slug are left floating. Self-capacitance is measured by sending a fast risetime step waveform through the lead under test. The reflection waveform from the lead, which includes the sum of all capacitive coupling with respect to the lead under test, is then measured. Appropriately, the self-capacitance can also be called the “bulk” capacitance since the measured value includes the capacitance between the lead under test and all surrounding metal, including the ground plane and the heat slug. For mutual-capacitance measurement, two adjacent leads are probed. An incident waveform is sent through one lead, and the induced waveform on the neighboring lead is measured as the mutual capacitance.

In order to de-embed the electrical parasitics of the DUT fixture and the measuring probes, the short and the open compensation waveforms are also measured after each package measurement. This procedure compensates the DUT fixture to the very tip of the probes.

Inductance & Capacitance Model Extraction

All measured reflection waveforms are downloaded to a PC running the analysis software for package parasitic model extraction. The software uses a method called the Z-profile algorithm, or the impedance-profile algorithm, for parasitic analysis. This method translates the downloaded reflection waveforms into true impedance waveforms, from which package models for inductance and capacitance are extracted.

Data Acquisition and Package Electrical Database

Xilinx acquires electrical parasitic data only on the longest and the shortest lead/traces of the package. This provides the best and the worst case for each package type (defined by package design, lead/ball count, pad size, and vendor). For convenience, the corner interconnects are usually selected as the longest interconnect, while the center interconnects are usually selected as the shortest.

For symmetrical quad packages, all four sides of the package are measured and averaged. Three to five samples are usually measured for accuracy and continuity purposes. The average of these samples is then kept as the official measured parasitic data of that package type in the database.

Component Mass (Weight) by Package Type

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
BG225	MOLDED BGA 27 mm FULL MATRIX	MO-151-CAL	OBG0001	2.2
BG256	MOLDED BGA 27 mm SQ	MO-151-CAL	OBG0011	2.2
BG352	SUPERBGA - 35 X 35 mm PERIPHERAL	MO-151-BAR	OBG0008	7.1
BG432	SUPERBGA - 40 X 40 mm PERIPHERAL	MO-151-BAU	OBG0009	9.1
BG560	SUPERBGA - 42.5 X 42.5 mm SQ	MO-192-BAV	OBG0010	11.5
CB100	NCTB TOP BRAZE 3K VER	MO-113-AD[3]	OCQ0008	10.8
CB100	NCTB TOP BRAZE 4K VER	MO-113-AD[3]	OCQ0006	10.8
CB164	NCTB TOP BRAZE 3K VER	MO-113-AA-AD[3]	OCQ0003	11.5
CB164	NCTB TOP BRAZE 4K VER	MO-113-AA-AD[3]	OCQ0007	11.5
CB196	NCTB TOP BRAZE 4K VER	MO-113-AB-AD[3]	OCQ0005	15.3
CB228	NCTB TOP BRAZE 4K VER	MO-113-AD[3]	OCQ0012	17.6
DD8	.300 CERDIP PACKAGE	MO-036-AA	OPD0005	1.1
HQ160	METRIC 28 28 -.65 mm 1.6H/S DIE UP	MO-108-DDI	OPQ0021	10.8
HQ208	METRIC 28 X 28 - H/S DIE UP	MO-143-FA1	OPQ0020	10.8
HQ240	METRIC QFP 32 32 - H/S DIE UP	MO-143-GA	OPQ0019	15.0
HQ304	METRIC QFP 40 40-H/S DIE DOWN	MO-143-JA	OPQ0014	26.2
PC20	PLCC JEDEC MO-047	MO-047-AA	OPC0006	0.8
PC44	PLCC JEDEC MO-047	MO-047-AC	OPC0005	1.2
PC68	PLCC JEDEC MO-047	MO-047-AE	OPC0001	4.8
PC84	PLCC JEDEC MO-047	MO-047-AF	OPC0001	6.8
PD8	DIP .300 STANDARD	MO-001-AA	OPD0002	0.5
PG84	CERAMIC PGA CAV UP 11X11	MO-067-AC	OPG0003	7.2
PG120	CERAMIC PGA 13 X 13 MATRIX	MO-067-AE	OPG0012	11.5
PG132	CERAMIC PGA 14 X 14 MATRIX	MO-067-AF	OPG0004	11.8

Component Mass (Weight) by Package Type (Continued)

Package	Description	JEDEC Outline #	Xilinx #	Mass (g)
PG156	CERAMIC PGA 16 X 16 MATRIX	MO-067-AH	OPG0007	17.1
PG175	CERAMIC PGA 16 X 16 STD VER.	MO-067-AH	OPG0009	17.7
PG191	CERAMIC PGA 18 X 18 STD - ALL	MO-067-AK	OPG0008	21.8
PG223	CERAMIC PGA 18 X 18 TYPE	MO-067-AK	OPG0016	26.0
PG299	CERAMIC PGA 20 X 20 HEATSINK	MO-067-AK	OPG0022	37.5
PG299	CERAMIC PGA 20 X 20 TYPE	MO-067-AK	OPG0015	29.8
PG411	CERAMIC PGA 39 X 39 STAGGER	MO-128-AM	OPG0019	36.7
PG475	CERAMIC PGA 41 X 41 STAGGER	MO-128-AM	OPG0023	39.5
PG559	CERAMIC PGA 43 x 43	MO-128	OPG0025	44.50
PP132	PLASTIC PGA 14 X 14 MATRIX	MO-83-AF	OPG0001	8.1
PP175	PLASTIC PGA 16 X 16 BURIED	MO-83-AH	OPG0006	11.1
PQ100	EIAJ 14 X 20 QFP - 1.60	MO-108-CC1	OPQ0013	1.6
PQ160	EIAJ 28 X 28 .65 mm 1.60	MO-108-DD1	OPQ0002	5.8
PQ208	EIAJ 28 X 28 .5 mm 1.30	MO-143-FAI	OPQ0003	5.3
PQ240	EIAJ 32 X 32 .5 mm	MO-143-GA	OPQ0010	7.1
SO8	VERSION 1 - .150/55MIL	MO-150	OPD0006	0.1
TQ100	THIN QFP 1.4 mm thick	MS-026-BDE	OPQ0004	0.7
TQ144	THIN QFP 1.4 mm thick	MS-026-BFB	OPQ0007	1.4
TQ176	THIN QFP 1.4 mm thick	MS-026-BGA	OPQ0008	1.9
CS48	Chip Scale 7 x 7 mm, 0.8 mm ball pitch	-	OBG0012	0.2
CS144	Chip Scale 12 x 12 mm, 0.8 mm ball pitch	MO-205-BE	OBG0015	0.3
FG256	Fine Pitch BGA 17 x 17 mm, 1.0 mm ball pitch	MO-151-AAF-1	OBG0021	0.8
FG456	Fine PItch BGA 23 x 23 mm, 1.0 mm ball pitch	MO-151-AAJ-1	OBG0019	2.1
FG556	Fine Pitch BGA 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0020	3.92
FG676	Fine PItch BGA, 27 x 27 mm, 1.0 mm ball pitch	MO-151-AAL-1	OBG0018	3.3
FG680	Fine PItch BGA 40 x 40 mm, 1.0 mm ball pitch	MO-151-AAU-1	OBG0022	10.3
FG900	Fine Pitch BGA, 31 x 31 mm, 1.0 mm ball pitch	MO-151-AAN-1	OBG0027	4.0
FG1156	Fine Pitch BGA, 35 x 35 mm, 1.0 mm ball pitch	MO-151-AAR-1	OBG0028	5.5
VO8	THIN SOIC-II	N/A	OPD0007	0.1
VQ44	THIN QFP 1.0 thick	MS-026-ACB	OPQ0017	0.4
VQ64	THIN QFP 1.0 thick	MS-026-ACD	OPQ0009	0.5
VQ100	THIN QFP 1.0 thick	MS-026-AED	OPQ0012	0.6

Notes:
1. Data represents average values for typical packages with typical devices. The accuracy is between 7% to 10%.
2. More precise numbers (below 5% accuracy) for specific devices may be obtained from Xilinx through a factory representative or by calling the Xilinx Hotline.
3. Tie-bar details are specific to Xilinx package. Lead width minimum is 0.056”.

Xilinx Thermally Enhanced Packaging

The Package Offering

Xilinx Code	Body (mm)	THK (mm)	Mass (gm)	Heatsink Location	JEDEC No.	Xilinx No.
HQ160	28x28	3.40	10.8	DOWN	MO-108-DD1	OPQ0021
HQ208	28x28	3.40	10.0	DOWN	MO-143-FA	OPQ0020
HQ240	32x32	3.40	15.0	DOWN	MO-143-GA	OPQ0019
HQ304	40x40	3.80	26.2	TOP	MO-143-JA	OPQ0014

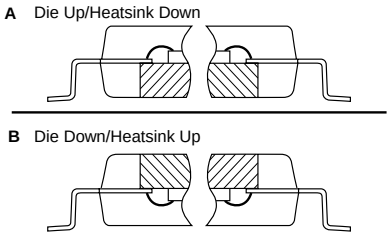
Overview

Xilinx offers thermally enhanced quad flat pack packages on certain devices. This section discusses the performance and usage of these packages (designated HQ). In summary:

- The HQ-series and the regular PQ packages conform to the same JEDEC drawings.
- The HQ and PQ packages use the same PCB land patterns.
- The HQ packages have more mass
- Thermal performance is better for the HQ packages

Where and When Offered

- HQ packages are offered as the thermally enhanced equivalents of PQ packages. They are used for high gate count or high I/O count devices in packages, where heat dissipation without the enhancement may be a handicap for device performance. Such devices include XC4013E, XC4020E, XC4025E, and XC5215.
- They are also being used in place of MQUAD (MQ) packages of the same lead count for new devices.
- The HQ series at the 240 pin count level or below are offered with the heatsink at the bottom of the package. This was done to ensure pin to pin compatibility with the existing PQ and MQ packages.
- At the 304 pin count level, the HQ is offered with the heatsink up. This arrangement offers a better potential for further thermal enhancement by the designer.



A – Heatsink down orientation
B – Heatsink up orientation X5962

Mass Comparison

Because of the copper heatsink, the HQ series of packages are about twice as heavy as the equivalent PQ. Here is a quick comparison.

	HQ (gm)	PQ (gm)
160 Pin	10.8	5.8
208 Pin	10.8	5.3
240 Pin	15.0	7.1
304 Pin	26.2	N/A

nants to the die surface and increasing the potential for early device failure.

Thermal Data for the HQ

The data for individual devices may be obtained from Xilinx.

Still Air Data Comparison		
	HQ Θ_{JA} (°C/Watt)	PQ Θ_{JA} (°C/watt)
160 Pin	13.5-14.5	20.5-38.5
208 Pin	14-15	26-35
240 Pin	12-13	19-28
304 Pin	10-11	N/A

Note: Θ_{JC} is typically between 1 and 2 °C/Watt for HQ and MQ Packages. For PQ's, it is between 2 and 7 °C/Watt.

Data Comparison at Airflow - 250 LFM		
	HQ Θ_{JA} (°C/watt)	PQ Θ_{JA} (°C/watt)
160 Pin	9-10	15-28.5
208 Pin	9-10	14-26
240 Pin	8-9	11-21
304 Pin	6.5-8	N/A

Other Information

- Leadframe: Copper EFTEC-64 or C7025
- Heat Slug: Copper - Nickel plated → Heatsink metal is Grounded
- Lead Finish 85/15 Sn/Pb 300 microinches minimum
- D/A material - Same as PQ; Epoxy 84-1LMISR4
- Mold Cpd. Same as PQ - EME7304LC
- Packed in the same JEDEC trays

Moisture Sensitivity of PSMCs

Moisture Induced Cracking During Solder Reflow

The surface mount reflow processing step subjects the Plastic Surface Mount Components (PSMC) to high thermal exposure and chemicals from solder fluxes and cleaning fluids during user's board mount assembly. The plastic mold compounds used for device encapsulation are, universally, hygroscopic and absorb moisture at a level determined by storage environment and other factors. Entrapped moisture can vaporize during rapid heating in the solder reflow process generating internal hydrostatic pressure. Additional stress is added due to thermal mismatch, and the Thermal Coefficient of Expansion (TCE) of plastic, metal lead frame, and silicon die. The resultant pressure may be sufficient to cause delamination within the package, or worse, an internal or external crack in the plastic package. Cracks in the plastic package can allow high moisture penetration, inducing transport of ionic contami-

How the effects of moisture in plastic packages and the critical moisture content result in package damage or failure is a complex function of several variables. Among them are package construction details -- materials, design, geometry, die size, encapsulant thickness, encapsulant properties, TCE, and the amount of moisture absorbed. The PSMC moisture sensitivity has, in addition to package cracking, been identified as a contributor to delamination-related package failure artifacts. These package failure artifacts include bond lifting and breaking, wire neckdown, bond cratering, die passivation, and metal breakage.

Because of the importance of the PSMC moisture sensitivity, both device suppliers and device users have ownership and responsibility. The background for present conditions, moisture sensitivity standardized test and handling procedures have been published by two national organizations. Users and suppliers are urged to obtain copies of both documents (listed below) and use them rigorously. Xilinx adheres to both.

- JEDEC STANDARD JESD22-A112. Test Method A112 "Moisture-Induced Stress Sensitivity for Plastic Surface Mounted Devices".
  Available through Global Engineering Documents
  Phone: USA and Canada 800-854-7179, International 1-303-792-2181
- IPC Standard IPC-SM-786A "Procedures for Characterizing and Handling of Moisture/Reflow Sensitive ICs".

  Available through IPC
  Phone: 1-708-677-2850

None of the previously stated or following recommendations apply to parts in a socketed application. For board mounted parts careful handling by the supplier and the user is vital. Each of the above publications has addressed the sensitivity issue and has established 6 levels of sensitivity (based on the variables identified). A replication of those listings, including the preconditioning and test requirements, and the factory floor life conditions for each level are outlined in Table 5. Xilinx devices are characterized to their proper level as listed. This information is conveyed to the user via special labeling on the Moisture Barrier Bag (MBB).

In Table 5, the level number is entered on the MBB prior to shipment. This establishes the user's factory floor life conditions as listed in the time column. The soak requirement is the test limit used by Xilinx to determine the level number. This time includes manufacturer's exposure time or the time it will take for Xilinx to bag the product after baking.

Table 5: Package Moisture Sensitivity Levels per J-STD-020

Level	Factory Floor Life		Soak Requirements (Preconditioning)			
	Conditions	Time	Time			Conditions
1	≤30°C / 90% RH	Unlimited	168 hours			85°C / 85% RH
2	≤30°C / 60% RH	1 year	168 hours			85°C / 60% RH
			Time (hours)			
			X +	Y =	Z	
3	≤30°C / 60% RH	168 hours	24	168	192	30°C / 60% RH
4	≤30°C / 60% RH	72 hours	24	72	96	30°C / 60% RH
5	≤30°C / 60% RH	24/28 hours	24	24/48	48/72	30°C / 60% RH
6	≤30°C / 60% RH	6 hours	0	6	6	30°C / 60% RH

Notes: X =Default value of semiconductor manufacturer's time between bake and bag. If the semiconductor manufacturer's actual time between bake and bag is different from the default value, use the actual time.
Y = Floor life of package after it is removed from dry pack bag.
Z = Total soak time for evaluation.

Factory Floor Life

Factory floor life conditions for Xilinx devices are clearly stated on MBB containing moisture sensitive PSMCs. These conditions have been ascertained by following Test Methods outlined in JEDEC JESD22-A112 and are replicated in Table 5. If factory floor conditions are outside the stated environmental conditions (30°C/90% RH for level 1, and 30°C/60% RH for Levels 2-6) or if time limits have been exceeded, then recovery can be achieved by baking the devices before the reflow step. Identified in the next section are two acceptable bake schedules. Either can be used for recovery to the required factory floor level.

Dry Bake Recommendation and Dry Bag Policy

Xilinx recommends, as do the mentioned publications and other industry studies, that all moisture sensitive PSMCs be baked prior to use in surface mount applications, or comply strictly with requirements as specified on the MBB. Tape and Reeled parts are universally dry packed. Level 1 parts are shipped without the need for, or use of, an MBB.

Two bake schedules have been identified as acceptable and equivalent. The first is 24 hours in air at 125°C., in shipping media capable of handling that temperature. The second bake schedule is for 192 hours in a controlled atmosphere of 40°C, equal to or less than 5% RH.

Dry Devices are sealed in special military specification Moisture Barrier Bags (MBB). Enough desiccant pouches are enclosed in the MBB to maintain contents at less than 20% RH for up to 12 months from the date of seal. A reversible Humidity Indicator Card (HIC) is enclosed to monitor the internal humidity level. The loaded bag is then sealed shut under a partial vacuum with an impulse heat sealer.

Artwork on the bags provides storage, handling and use information. There are areas to mark the seal date, quantity, and moisture sensitivity level and other information. The following paragraphs contain additional information on handling PSMCs.

Handling Parts in Sealed Bags

Inspection

Note the seal date and all other printed or hand entered notations. Review the content information against what was ordered. Thoroughly inspect for holes, tears, or punctures that may expose contents. Xilinx strongly recommends that the MBB remain closed until it reaches the actual work station where the parts will be removed from the factory shipping form.

Storage

The sealed MBB should be stored, unopened, in an environment of not more than 90% RH and 40°C. The enclosed HIC is the only verification to show if the parts have been exposed to moisture. Nothing in part appearance can verify moisture levels.

Expiration Date

The seal date is indicated on the MBB. The expiration date is 12 months from the seal date. If the expiration date has been exceeded or HIC shows exposure beyond 20% upon opening the bag bake the devices per the earlier stated bake schedules. The three following options apply after baking:

Use the devices within time limits stated on the MBB.

Reseal the parts completely under a partial vacuum with an impulse sealer (hot bar sealer) in an approved MBB within 12 hours, using fresh desiccant and HIC, and label accordingly. Partial closures using staples, plastic tape, or cloth tape are unacceptable.

Store the out-of-bag devices in a controlled atmosphere at less than 20% RH. A desiccator cabinet with controlled dry air or dry nitrogen is ideal.

Other Conditions

Open the MBB when parts are to be used. Open the bag by cutting across the top as close to the seal as possible. This provides room for possible resealing and adhering to the reseal conditions outlined above. After opening, strictly adhere to factory floor life conditions to ensure that devices are maintained below critical moisture levels.

Bags opened for less than one hour (strongly dependent on environment) may be resealed with the original desiccant. If the bag is not resealed immediately, new desiccant or the old one that has been dried out may be used to reseal, **if the factory floor life has not been exceeded**. Note that factory floor life is cumulative. Any period of time when MBB is opened must be added to all other opened periods.

Both the desiccant pouches and the HIC are reversible. Restoration to dry condition is accomplished by baking at 125°C for 10-16 hours, depending on oven loading conditions.

Tape and Reel

Xilinx offers a tape & reel packing for PLCC, BGA, QFP, and SO packages. The packing material is made of black conductive Polystyrene and protects the packages from mechanical and electrical damage. The reel material provides a suitable medium for pick and place equipment.

The tape & reel packaging consists of a pocketed carrier tape, sealed with a protective cover. The device sits on pedestals (for PLCC, QFP packages) to protect the leads from mechanical damage. All devices loaded into the tape carriers are baked, lead scanned before the cover tape is attached and sealed to the carrier. In-line mark inspection for mark quality and package orientation is used to ensure shipping quality.

Benefits

- Increased quantity of devices per reel versus tubes improves cycle time and reduces the amount of time to index spent tubes.
- Tape & reel packaging enables automated pick and place board assembly.
- Reels are uniform in size enabling equipment flexibility.
- Transparent cover tape allows device verification and orientation.
- Anti-static reel materials provides ESD protection.
- Carrier design include a pedestal to protect package leads during shipment.
- Bar code labels on each reel facilitate automated inventory control and component traceability.
- All tape & reel shipments include desiccant pouches and humidity indicators to insure products are safe from moisture.
- Compliant to Electronic Industries Association (EIA) 481.

Material and Construction

Carrier Tape

- The pocketed carrier Tape is made of conductive polystyrene material, or equivalent, with a surface resistivity level of less than 106 ohms per square inch.
- Devices are loaded ‘live bug’ or leads down, into a device pocket.
- Each carrier pocket has a hole in the center for automated sensing of whether a unit is in the pocket or not.
- Sprocket holes along the edge of the carrier tape enable direct feeding into an automated board assembly equipment.

Cover Tape

- An anti-static, transparent, polyester cover tape, with heat activated adhesive coating, sealed to the carrier edges to hold the devices in the carrier pockets.
- Surface resistivity on both sides is less than 1011 ohms per square inch.

Reel

- The reel is made of anti-static Polystyrene material. The loaded carrier tape is wound onto this conductive plastic reel.
- A protective strip made of conductive Polystyrene material is placed on the outer part of the reel to protect the devices from external pressure in shipment.
- Surface resistivity is less than 1011 ohms per square inch.
- Device loading orientation is in compliance with EIA Standard 481.

Bar Code Label

- The bar code label on each reel provides customer identification, device part number, date code of the product and quantity in the reel.
- Print quality are in accordance with ANSI X3.182-1990 Bar Code Print Quality Guidelines. Presentation of Data on labels are EIA-556-A compliant.
- The label is an alphanumeric, medium density Code 39 labels.
- This machine-readable label enhances inventory management and data input accuracy.

Shipping Box

- The shipping container for the reels are in a 13” x 13” x 3” C-flute, corrugated, # 3 white ‘pizza’ box, rated to 200 lb test.

Table 6: Tape & Reel Packaging

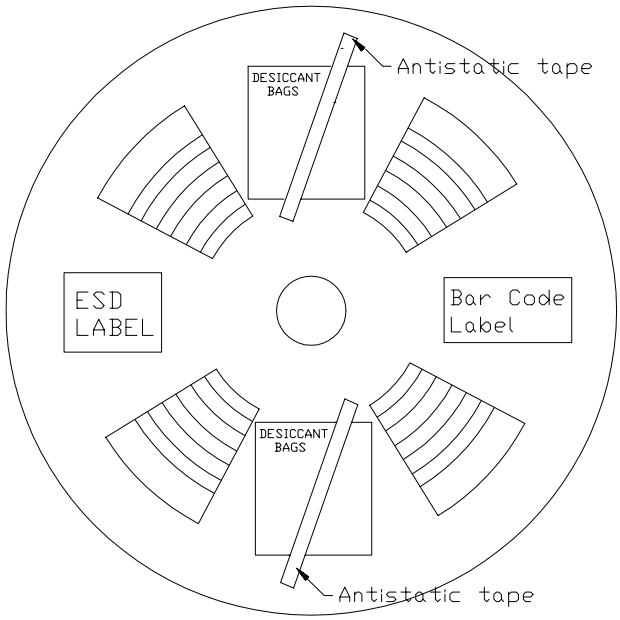
Package Type	Pin Count	Carrier Width	Cover Width	Pitch	Reel Size	Qty per Reel
PLCC (Plastic Leaded Chip Carrier)	20	16 mm	13.3 mm	12 mm	7 inch	250
	20	16 mm	13.3 mm	12 mm	13 inch	750
	44	32 mm	25.5 mm	24 mm	13 inch	500
	68	44 mm	37.5 mm	32 mm	13 inch	250
	84	44 mm	37.5 mm	36 mm	13 inch	250
SO (Plastic Small Outline)	8	12 mm	9.2 mm	8 mm	7 inch	750

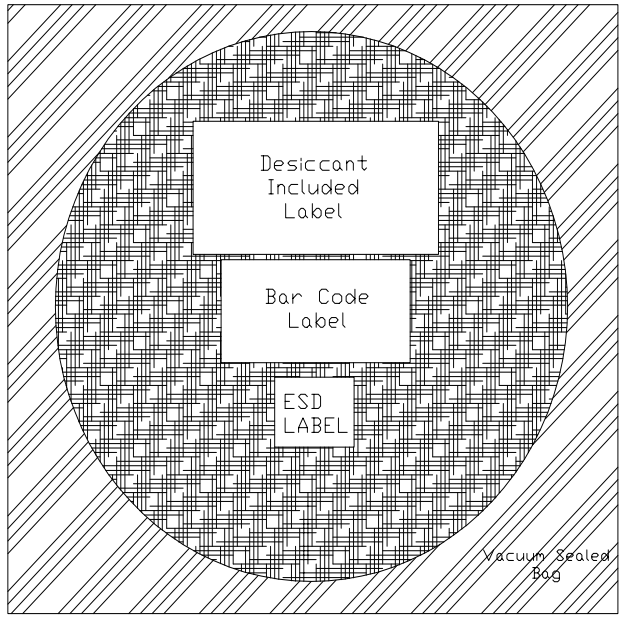
Table 6: Tape & Reel Packaging

Package Type	Pin Count	Carrier Width	Cover Width	Pitch	Reel Size	Qty per Reel
QFP (Plastic Quad Flat Pack) PQ, VQ, TQ, HQ	100	44 mm	37.5 mm	32 mm	13 inch	250
	160	44 mm	37.5 mm	40 mm	13 inch	200
BGA (Plastic Ball Grid Array)	225/256	44 mm	37.5 mm	32 mm	13 inch	500
SBGA	352/432/560	56 mm	49.5 mm	40,48,48 mm	13 inch	200

Notes:
1. A minimum of 230mm of empty pockets are provided at the beginning (leader) of each reel.
2. A minimum of 160mm of empty pockets are provided at the end (trailer) of each reel.
3. Tape Leader/Trailer requirements are in compliance to EIA Standards 481.
4. Peel Strength between 20 and 120 grams ensures consistency during de-reeling operations and is compliant to EIA Standard 481.
5. Each reel is subject to peel back strength tests.
6. For packages not listed above, please contact your Xilinx sales representative for updated information.

Standard Bar Code Label Locations





Reflow Soldering Process Guidelines

To implement and control the production of surface mount assemblies, the dynamics of the solder reflow process and how each element of the process is related to the end result must be thoroughly understood.

The primary phases of the reflow process are as follows:

1. Melting the particles in the solder paste
2. Wetting the surfaces to be joined
3. Solidifying the solder into a strong metallurgical bond

The sequence of five actions that occur during this process is shown in Figure 4.

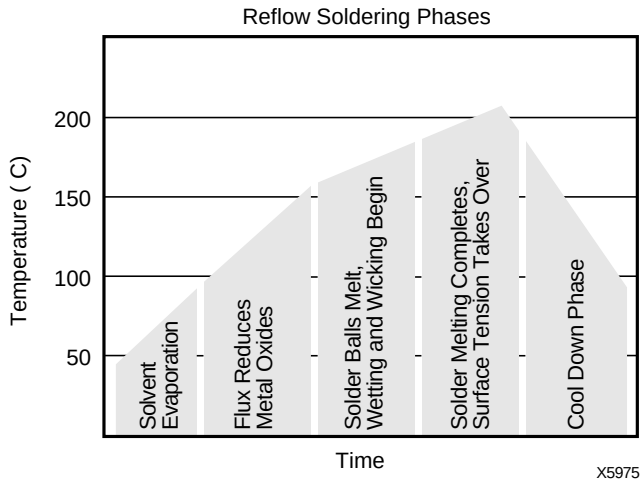
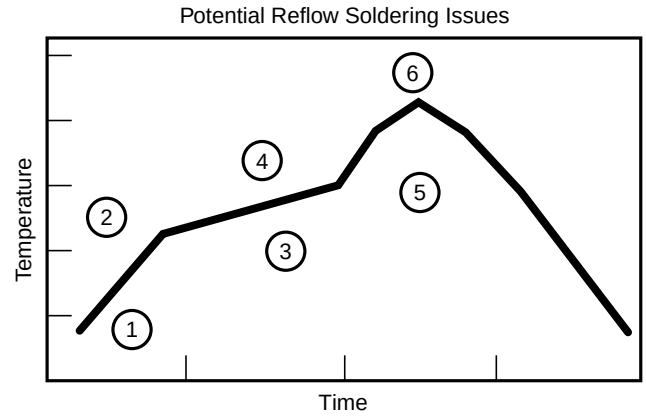


Figure 4: Soldering Sequence

Each phase of a surface mount reflow profile has min/max limits that should be viewed as a process window. The process requires a careful selection and control of the materials, geometries of the mating surfaces (package footprint vs. PCB land pattern geometries) and the time temperature of the profile. If all of the factors of the process are sufficiently optimized, there will be good solder wetting and fillet formation (between component leads and the land patterns on the substrate). If factors are not matched and optimized there can be potential problems as summarized in Figure 5.



1. Insufficient Temperature to Evaporate Solvent
2. Component Shock and Solder Splatter
3. Insufficient Flux Activation
4. Excessive Flux Activity and Oxidation
5. Trapping of Solvent and Flux, Void Formation
6. Component and/or Board Damage

Figure 5: Soldering Problems Summary

8

Figure 6 and Figure 7 show typical conditions for solder reflow processing using IR/Convection or Vapor Phase. Both IR and Convection furnaces are used for BGA assembly. The moisture sensitivity of Plastic Surface Mount Components (PSMCs) must be verified prior to surface mount flow. See the preceding sections for a more complete discussion on PSMC moisture sensitivity.

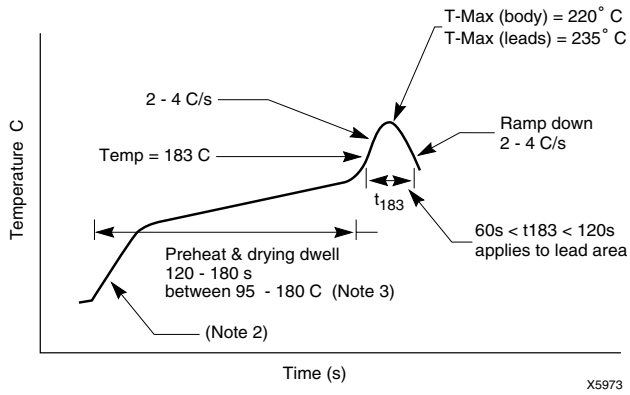


Figure 6: Typical Conditions for IR Reflow Soldering

Notes:
1. Max temperature range = 220°C-235°C (leads)
   Time at temp 30-60 seconds
2. Preheat drying transition rate 2-4°C/s
3. Preheat dwell 95-180°C for 120-180 seconds
4. IR reflow shall be performed on dry packages

The IR process is strongly dependent on equipment and loading differences. Components may overheat due to lack of thermal constraints. Unbalanced loading may lead to significant temperature variation on the board. This guideline is intended to assist users in avoiding damage to the components; the actual profile should be determined by the users using these guidelines.

The peak reflow temperature of the PSMC body should not be more than 220° C in order to avoid internal package delamination. For multiple BGAs in a single board, it is recommended to check all BGA sites for varying temperatures because of differences in surrounding components.

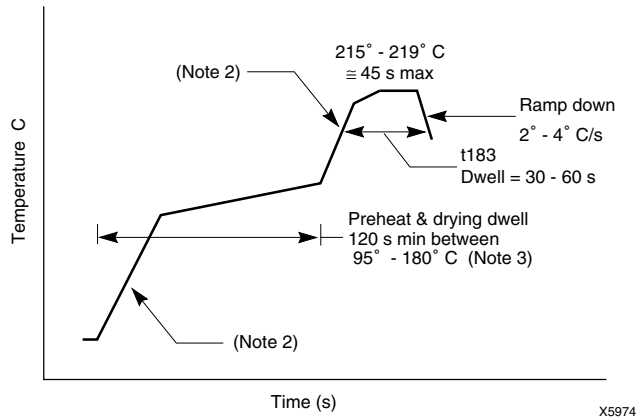


Figure 7: Typical Conditions for Vapor Phase Reflow Soldering

Notes:
1. Solvent - FC5312 or equivalent - ensures temperature range of leads @ 215-219°C
2. Transition rate 4-5°C/s
3. Dwell is intended for partial dryout and reduces the difference in temperature between leads and PCB land patterns.
4. These guidelines are for reference. They are based on laboratory runs using dry packages. It is recommended that actual packages with known loads be checked with the commercial equipment prior to mass production.

Sockets

Table 7 lists manufacturers known to offer sockets for Xilinx Package types. This summary does not imply an endorsement by Xilinx. Each user has the responsibility to evaluate and approve a particular socket manufacturer.

Table 7: Socket Manufacturers

Manufacturer	Packages					
	DIP SO VO	PC WC	PQ HQ TQ VQ	PG PP	CB	BG CG
AMP Inc. 470 Friendship Road Harrisburg, PA 17105-3608 (800) 522-6752	X	X		X		
Augat Inc. 452 John Dietsch Blvd. P.O. Box 2510 Attleboro Falls, MA 02763-2510 (508) 699-7646	X	X		X		
McKenzie Socket Division 910 Page Avenue Fremont, CA 94538 (510) 651-2700	X	X		X		
3M Textool 6801 River Place Blvd. Austin, TX 78726-9000 (800) 328-0411 (612) 736-7167				X	X	X
Wells Electronics 1701 South Main Street South Bend, IN 46613-2299 (219) 287-5941				X		
Yamaichi Electronics Inc. 2235 Zanker Road San Jose, CA 95131 (408) 456-0797		X	X	X	X	

Package Drawings

Testing, Quality Assurance, and Reliability Table of Contents

Testing, Quality Assurance, and Reliability

Quality Assurance and Reliability

February 1, 2000 (v3.0)

Quality Assurance Program

All aspects of the Quality Assurance Program at Xilinx have been designed to eliminate the root cause of defects by prevention, rather than to try to remove defects through inspection. A quality management system is in place which is fully compliant with the requirements of ISO9001. Xilinx was found to be in full compliance to ISO 9001:1994 by an independent ISO auditor and was registered in November 1997. At that time Xilinx was registered for "the design, manufacturing and testing of programmable logic devices". Also in November 1997, DSCC found Xilinx to be in full compliance with the requirements of MIL 38535 and granted Xilinx full status as a QML supplier.

Those aspects of ISO compliance which are in place at Xilinx include the following seventeen points:

- **Management Review**: a comprehensive system of management attention to and direction of all aspects of company performance which directly affect our customers. These include (among others) Xilinx performance in the areas of Quality, Reliability and On-Time Delivery. Management assures that this quality policy is understood, implemented and maintained at all levels in the organization.
- **Quality Systems**: are in place to ensure that all Xilinx products conform to customer specifications. These systems facilitate, measure and continuously improve Xilinx performance in those areas which affect customer satisfaction. Xilinx remains committed to achieving 100% customer satisfaction.
- **Contract Review**: is conducted to ensure that each contract adequately defines and documents customer requirements, that differences between customer and Xilinx standard specifications are mutually satisfactorily resolved, and that Xilinx has the capability to meet all contract requirements.
- **Document Control**: procedures are established and maintained to control all documents and data that relate to the performance of Xilinx business and processing requirements. All organizations who need access to such documentation during the performance of their functions are assured availability of the latest, controlled versions of that documentation.
- **Purchasing**: procedures are in place to ensure that all purchased products conform to the specified requirements. As Xilinx is a "fabless" manufacturing company, special attention is paid to our subcontract partners. They are required to demonstrate the type of control and capabilities that our customers require of us. All key Xilinx subcontract partners are ISO certified.
- **Product Identification and Traceability**: is maintained throughout the manufacturing process. Traceability back to the starting materials is available through unique product identification techniques and markings.
  Process Control: is assured by identifying and planning those processes which directly affect the quality of our products, whether those processes are performed directly by Xilinx, or buy our subcontract partners.
- **Inspection and Test**: is performed to ensure that incoming product is not used or processed until it has been verified as conforming to required specifications. This inspection is done jointly by Xilinx and by its subcontract partners.
- **Inspection, Measuring and Test Equipment**: is calibrated in conformance with the requirements of ANSI/NCSL Z540-I-1994 (and former Mil Ref 45662) and/or other international standards. Equipment is maintained in such a manner to ensure that measurement uncertainty is known and is consistent with specification accuracy requirements.
- **Inspection and Test Status**: of product is uniquely identified throughout the manufacturing process both at Xilinx and at our subcontract partners. Records are kept to identify the authority responsible for the release of conforming production.
- **Control of Non-Conforming Product**: is assured through disposition procedures which are defined in such a manner to prevent the shipping of non-conforming products. The responsibility and authority for the disposition of such products are well defined.
- **Corrective Action**: processes are documented and implemented to prevent the recurrence of nonconforming product. These processes are the key to implementing Xilinx strategy of eliminating the root causes of nonconformity, rather that to apply inspection to try to remove nonconformity.
- **Handling, Storage, Packing and Delivery**: procedures are defined and implemented to prevent damage or deterioration of product once the manufacturing process is complete.
- **Quality Records**: procedures are established and maintained for the identification, collection, indexing, filing, storage, maintenance and disposition of quality records.

- **Internal Quality Audits**: are carried out to verify whether quality activities comply with planned arrangements and to determine the effectiveness of the quality system. These audits are regularly supplemented by quality audits performed by our customers, and by our independent ISO auditors.
- **Training**: procedures have been established and are maintained to identify the training needs of all personnel affecting quality during the production of Xilinx products. Personnel performing such activities are qualified based upon appropriate education, training and/or experience.
- **Statistical Techniques**: are in place at Xilinx and at our subcontract partners for verifying the acceptability of process capability and product characteristics.

These key requirements are in place at Xilinx and at our subcontract partners to ensure our ability to achieve customer satisfaction through the **on-time delivery** of **quality products** that **meet customer requirements** and are **reliable**.

Device Reliability

Device reliability is often expressed in a measurement called Failures in Time (FITs). In this measure one FIT equals one failure per billion (10^9) device operating hours. A failure rate in FITS must include the operating temperature to be meaningful. Hence failure rates are often expressed in FITS at 55°C (or some other temperature in excess of the application). Since one billion hours is well in excess of 100,000 years, the FIT rate of modern ICs can only be measured by accelerating the failure rate by testing at a higher junction temperature (usually 125°C or 145°C). Extensive testing of Xilinx devices (performed on actual production devices taken directly from finished goods) has been done continuously since 1989 and reported quarterly. Quarterly reports on the reliability of Xilinx products are available through your Xilinx sales representative and at the WebLINX web site (http://www.xilinx.com/products/qa_data/relreprt.pdf). During the last two years, over 20,000 devices have accumulated a total of over 50,000,000 hours of both static and dynamic operation at 125°C (equivalent) to yield the FIT rates shown in Figure 1 and Figure 2.

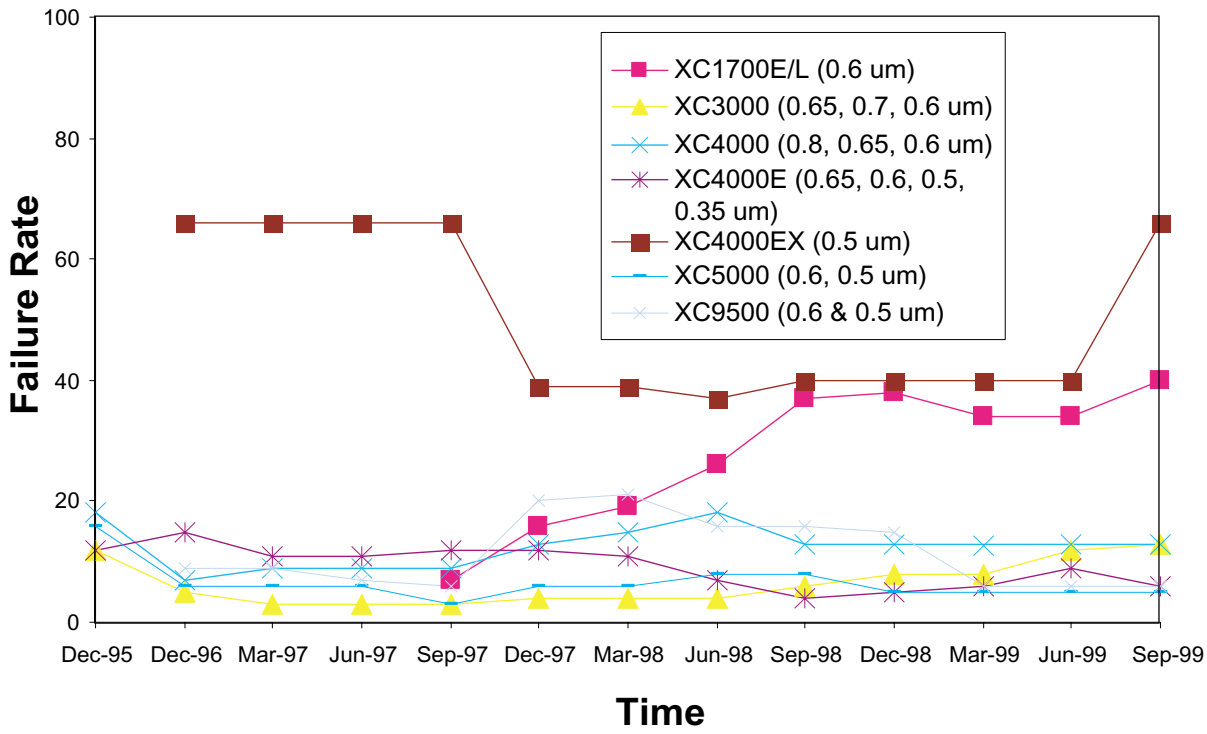


Figure 1: Failure Rate in FITS at Tj = 55°C for Mature Products-XSJ

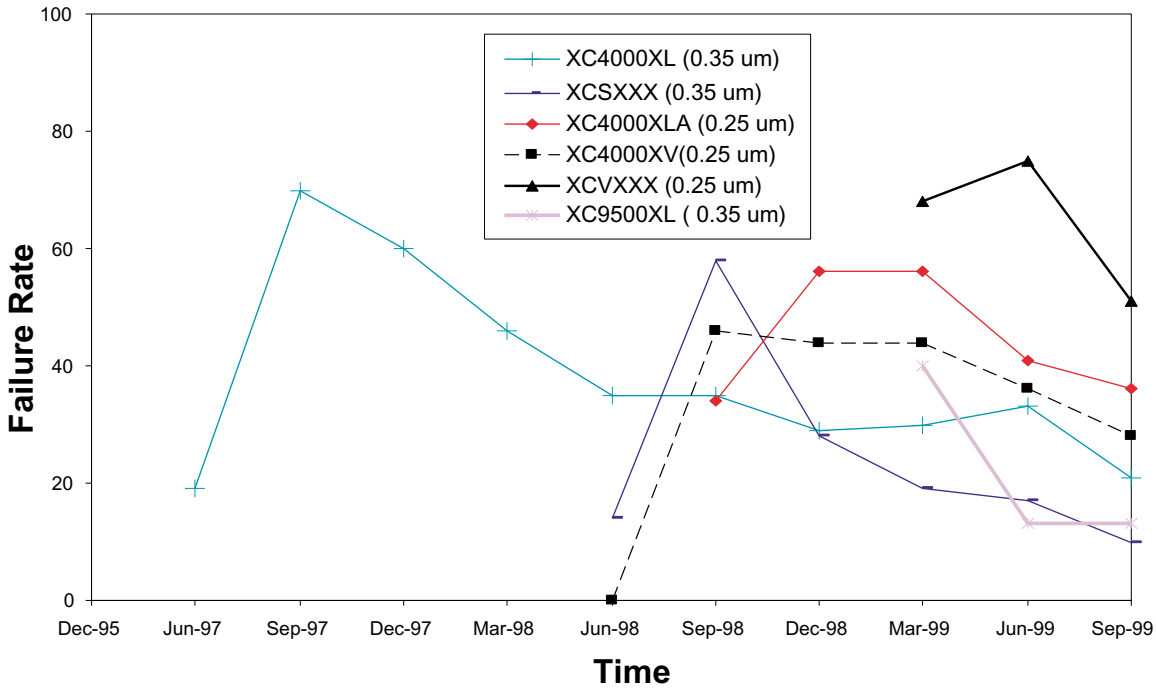


Figure 2: Failure Rate in FITS at Tj = 55°C for New Products-XSJ

Testing Facilities

Xilinx has facilitated a laboratory to perform High Temperature Life Testing, Thermal Shock, Temperature Cycling, Biased Moisture Life Test, Unbiased Pressure Pot, Solderability and Hermeticity on site, as well as having complete Failure Analysis capabilities in house. Table 1 and Table 2 show typical qualification requirements for new and/or changed process flows. Table 3 is a list of current failure analyses capabilities. These laboratories are dedicated exclusively to increasing customer satisfaction through continuous improvements in our processes and technologies.

Table 1: Plastic Package/Product Qualification Requirements

							New Assy Techniques (Mat'l/Process/Method								
Test Seq	**Test Description (note 1)**	**Acc# S.Size (note 2)**	**New Assy Plant**	**New Pkg Type I (note3)**	**New Pkg Type II (note4)**	**New Pkg Type III LF Design (note5)**	**Lead Frame**	**Die Attach**	**Die Coat**	**Wire Bond**	**Mold CLP**	**Lead Finish**	**New Device Mask (note6)**	**New Fab Proc**	**Full Qual**
B1	* Phy. Dimension	0/5	X	X	X							X			X
B2	* Resist. to Solvents	0/3	X								X	X			X
B3	* Solderability Test (note 7)	0/5	X				X					X			X
B4	Solder Heat Test (Optn'l)	0/15				X	X				X				X
B5	Auto Clave (SPP)(Optn'l) 0/76	0/76	X	X	X	X	X		X		X		X		X
B6	* Ball Shear/Bond Pull (note 7)	0/5	X	X					X	X	X		X	X	X
B7	** X-Ray (note 7)	0/5	X	X	X	X			X	X	X		X		X
B8	* S.A.T/Dye Pen Test (note 7)	0/10	X	X	X	X	X				X	X			X
B9	* Adhesion of L/Finish (Optn'l)	0/3	X				X					X			X
B10	* External Visual (note 7)	0/25	X	X	X	X	X				X				X
B11	Internal Visual (note 7)	0/5	X	X	X		X	X	X	X			X	X	X
B12	* Die Shear (note 7)	0/5	X					X					X	X	X
B13	Flammability Test (note 7)	Per lot									X				X
C1-A	High Temp Life Test	0/76							X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	C2-A:HAST (0/22) or C2-B: 85/85	0/76	X	X		X	X	X	X		X			X	X
C3	ESD (HBM)	0/3											X	X	X
C4	High Temp Storage (Optn'l)	0/77									X		X	X	X
D1	* Lead Integrity	0/3	X	X	X							X			X
D2	Thermal Shock (Optn'l)	0/76													X
D3	Temp Cycle	0/76	X	X	X	X	X	X	X	X	X			X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake EPLD & EPR	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
E9	Power Cycling (Optn'l)	0/22											X	X	X
Qty required per lot		E.Good	239	238	162	248	248	157	314	86	325	0	393	464	636
		E.Reject	63	48	43	35	43	5	5	5	43	29	10	10	64
		Total	302	286	205	283	291	162	319	91	368	29	403	474	700

Notes: 1) Test method and stress conditions available upon request.2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Any new package which has not been qualified in the qualified assembly facility.
4) Any new package where the same body size with different lead pitch has been qualified.
5) New leadframe design whereby the paddle size is larger than the existing leadframe paddle size used in the same qualified package.
6) For new mask from same device family, only high temp life test, ESD, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement.
*) Electrical rejects can be used as test sample.
**) This is a non-destructive test, sample can be re-used.

Table 2: Hermetic Package/Product Qualification Requirements (Commercial)

			New Assy Techniques (Mat'l/Process/Method												
Test Seq	**Test Description (note 1)**	**Acc# S.Size (note 2)**	**New Assy Plant**	**New Pkg Family (note3)**	**New Pkg Qual Family (note4)**	**Lead Frame**	**Die Attach**	**Die Coat**	**Wire Bond**	**Type of Seal**	**Lead Finish**	**New Cavity Size (note6)**	**New Device (note6)**	**New Fab Proc**	**Full Qual**
B1	Solder Heat Test (Optn'l)	0/15		X	X					X		X			X
B2	* Resist. to Solvents (note 7)	0/3	X	X							X				X
B3	* Solderability Test (note 7)	0/3	X	X		X					X				X
B4	* Die Shear/Stud Pull (note 7)	0/5	X	X	X		X						X	X	X
B5	* Bond Pull (note 7)	0/2	X	X	X	X		X	X				X	X	X
B6	* External Visual (note 7)	0/25	X	X	X	X			X		X				X
B7	Internal Visual (note 7)	0/5	X	X	X	X	X	X	X				X	X	X
C1-A	High Temp Life Test	0/76	X	X				X	X				X	X	X
C1-B	Low Temp Life Test (note 7)	0/22											X	X	X
C2	High Temp Storage (Optn'l)	0/77						X					X	X	X
C3	ESD (HBM)	0/3											X	X	X
D1	* Phy. Dimension	0/15	X	X	X						X	X		X	X
D2	* Lead Integrity	0/3	X	X	X	X					X			X	X
D3	Thermal Shock + Temp Cycl + Moisture Resistance	0/32	X	X	X	X	X	X	X	X	X	X	X	X	X
D4	Mech. Shock + Vibration + Constant Acceleration	0/32	X	X	X	X	X		X	X		X	X	X	X
D5	* Salt Atmosphere	0/15	X	X	X						X			X	X
D6	* Internal Vapor Content (note 7)	0/3	X	X	X		X	X		X		X		X	X
D7	* Adhesion of L/Finish (Optn'l)	0/2	X	X	X	X					X			X	X
D8	* Lid Torque	0/5	X	X	X					X		X		X	X
D9	Temp Cycle	0/45	X	X	X		X	X	X	X		X	X	X	X
E1	Electrical Test & Data Log	0/30											X	X	X
E2	Electrical Characterization	0/30											X	X	X
E3	T.D.D.B (note 7)	–											X	X	X
E4	Latch-up	0/9											X	X	X
E5	Electromigration (note 7)	–											X	X	X
E6	Photosensitivity (Optn'l)	0/11											X	X	X
E7	Data Retention Bake	0/22											X	X	X
E8	Input/Output Capacitance	0/5											X	X	X
Qty required per lot		E.Good	190	205	129	69	114	235	190	124	32	124	399	399	414
		E.Reject	81	81	75	50	8	5	2	33	41	48	7	50	81
		Total	271	286	204	119	122	240	192	157	73	172	406	449	495

Notes:
1) Test method and stress conditions available upon request.
2) For any QUAL which does not meet the standard requirements, approval from Product Engineering and Product QA is required.
3) Package Family - A set of package type with the same package, material, Package construction techniques, terminal pitch, lead shape, row spacing and with identical package assembly tech.
4) Package Type - A package with a unique case outline, configuration, material, piece parts and assembly process.
5) Application to new piece parts or leadframe where cavity size is larger than the largest cavity size for the same package.
6) For new mask from same device family, only high temp life test, ESP, Latch & Capacitance are required.
7) In-process monitor data may be used to satisfy this requirement, for Qual data, data from Assy. lot traveler maybe used.
*) Electrical rejects can be used as test samples

Table 3: Failure Analysis Equipment List

Item	Equipment	Vendor	Model Number	Item	Equipment	Vendor	Model Number
1	Scanning Electron Microscope	JEOL	JMS-6401F	17	Die-Shear Tester	KELLER	see #7
2	Gold Sputter (SEM Sample Prep)	ANATECH	Hummer VIII	18	Steam Aging System	Robotic Systems	ST2D
3	Energy Dispersive X-Ray	OXFORD INST.	LINK ISIS-L200C	19	Solder Wave/Pot	Robotic Systems	RPS-202
4	F.I.B. - Focused Ion Beam Workstation	F.E.I.	FIB-600	20	Lead Fatigue Tester	B & G	004-012-00
5	Real-Time X-Ray Imaging System	FEIN FOCUS	FXS-100.10	21	Conventional Oven (C.D.A.)	BID Services	
6	Scanning Acoustic Microscopy	Sonix	Micro-Scan 4HF-200	22	Drill-bit to open MQUADS + Decapping vise		
7	Ball Shear Strength Tester	KELLER	MBS-200	23	Color Printer	Tektronic	Tektronic Phaser IISD
8	XRF Lead Finish/Composition Measurement System	Twin City, Inc.	XRF-5500	24	Stud Pull Tester	B & G	003-010-00
9	Liquid Crystal Hot Spot Detection System/Kit, with 3 temp.	Technology Associates	P/N 4330	25	Work Benches		
10	Emission Microscope for Multilayer Inspection (EMMI)	Hypervision	Visionary 2000	26	Cabinets		
11	Curve Tracer	BID Services		27	Facilities (Lab Area and Equipment Installation Costs)		
12	Metallurgical High Power Microscope	Scientific Instrument Company	see quote (various)	28	Tool Maker Microscope		
13	Stereozoom Low Power Microscope - video camera + monitor	Scientific Instrument Company	see quote (various)	29	Flowhood & Rinse Station		
14	Micro-Etcher System	TM Associates		30	Precision X-Sectioning Equipment		
15	Viseco Camera Interface with High Power Microscope	Computer Modules		31	Plasma Etcher	March Instruments	CS-1701
16	Hermeticity Test System - Fine Leak - Gross Leak	BID Services	-Trio-tech 486 - Veeco MS-170	32	E-Beam IDS-3000		

Description of Tests

Die Qualification

1. **High Temperature Life:** This test is performed to evaluate the long-term reliability and life characteristics of the die. It is defined by the Military Standard from which it is derived as a "Die-Related Test" and is contained in the Group C Quality Conformance Tests. Because of the acceleration factor induced by higher temperatures, (typically 125°C and/or 145°C) data representing a large number of equivalent hours at a normal temperature of 25°C can be accumulated in a reasonable period of time.
2. **Biased Moisture Life:** This test is performed to evaluate the reliability of the die under conditions of long-term exposure to severe, high-moisture environments that could cause corrosion. Although it clearly stresses the package as well, this test is typically grouped under the die-related tests. The device is operated at maximum rated voltage (Vccmax) and is exposed to a temperature of 85°C and a relative humidity of 85% throughout the test.

Package Integrity and Assembly Qualification

1. **Unbiased Pressure Pot:** This test is performed at a temperature of 121°C and a pressure of 2 atm of saturated steam to evaluate the ability of the plastic encapsulating material to resist water vapor. Moisture penetrating the package could induce corrosion of the bonding wires and nonglassivated metal areas of the die (bonding pads only for FPGA devices). Under extreme conditions, moisture could cause drive-in and corrosion under the glassivation. Although it is difficult to correlate this test to actual field conditions, it provides a well-established method for relative comparison of plas-

tic packaging materials and assembly and molding techniques.

2. **Thermal Shock:** This test is performed to evaluate the resistance of the package to cracking and resistance of the bonding wires and lead frame to separation or damage. It involves nearly instantaneous change in temperature from –65°C to +150°C (known as condition "C").
3. **Temperature Cycling:** This test is performed to evaluate the long-term resistance of the package to damage from alternating exposure to temperature extremes. The range of temperatures is –65°C to +150°C (again condition "C"). The transition time is longer than that in the Thermal Shock test but the test is conducted for many more cycles.
4. **Salt Atmosphere:** This test was originally designed by the US Navy to evaluate resistance of military-grade ship-board electronics to corrosion from sea water. It is used more generally for non-hermetic industrial and commercial products as a test of corrosion resistance of the package marking and finish.
5. **Resistance to Solvents:** This test is performed to evaluate the integrity of the package marking during exposure to a variety of solvents. This is an especially important test, since an increasing number of board-level assemblies are subjected to severe conditions of automated cleaning before system assembly. This test is performed according to the methods specified by MIL-STD-883.
6. **Solderability:** This test is performed to evaluate the solderability of the leads under conditions of low soldering temperature following exposure to the aging effects of water vapor.
7. **Lead Fatigue:** This test is performed to evaluate the resistance of the completed assembly to vibrations during storage, shipping, and operation.

Data Integrity

Memory Cell Design in the FPGA Device:

An important aspect of SRAM-based FPGA device reliability is the robustness of the static memory cells used to store the configuration program. The basic cell is a single-ended 5-transistor memory element (Figure 3). By eliminating a sixth transistor, which would have been used as a pass transistor for the complementary bit line, a higher circuit density is achieved. During normal operation, the outputs of these cells are fixed, since they determine the user configuration. Write and readback times, which have no relation to the device performance during normal operation, will be slower without the extra transistor. In return, the user receives more functionality per unit area. This explains the basic cell, but how is the FPGA user assured of high data integrity in a noisy environment? Consider three different situations: normal operation, a Write operation and a Read operation

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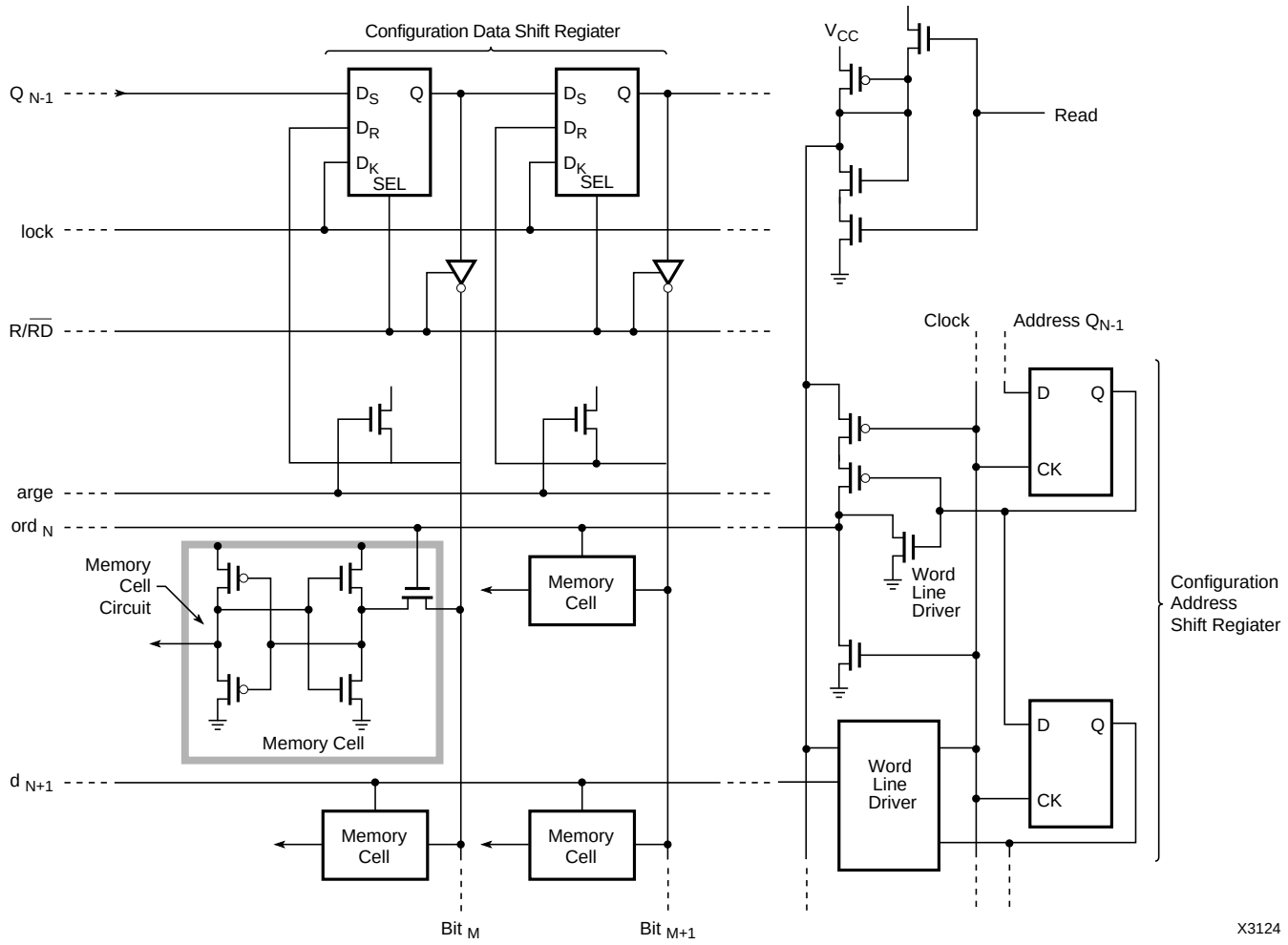

Figure 3: Configuration Memory Cell

In the normal operation, the data in the basic memory element is not changed. Since the two circularly linked inverters that hold the data are physically adjacent, supply transients result in only small relative differences in voltages. Each inverter is truly a complementary pair of transistors. Therefore, whether the output is High or Low, a low-impedance path exists to the supply rail, resulting in extremely high noise immunity. Power supply or ground transients of several volts have no effect on stored data. The transistor driving the bit line has been carefully designed so that whenever the data to be written is opposite the data stored, it can easily override the output of the feedback inverter. The reliability of the Write operation is guaranteed within the tolerances of the manufacturing process. In the Read mode, the bit line, which has a significant amount of parasitic capacitance, is precharged to a logic one. The pass transistor is then enabled by driving the word line High. If the stored value is a zero, the line is then discharged to ground. Reliable reading of the memory cell is achieved by reducing the word line High level during reading to a level that insures that the cell will not be disturbed.

Electrostatic Discharge:

Electrostatic-discharge (ESD) protection for each pad is provided by circuitry that uses distributed transistors, diodes and/or other structures, represented by the circles in Figure 4. In older devices, these protection circuits are conventional diffused structures. In newer designs, Xilinx utilizes proprietary device structures which exhibit substantially enhanced ESD protection.

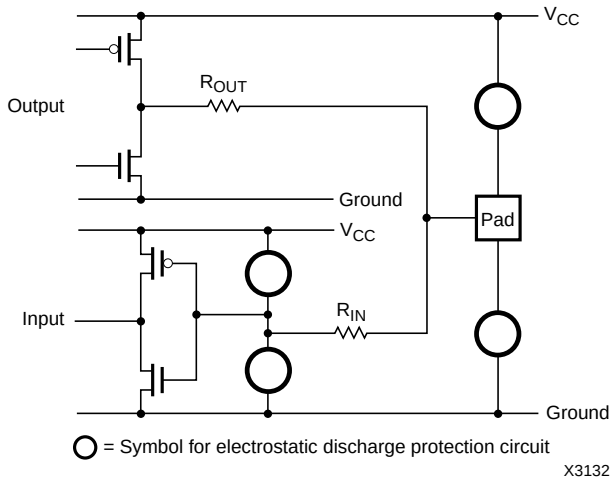

Figure 4: Input/Output Protection Circuitry

Table 4: ESD Performance of Xilinx Components

Device Family	HBM Model	EIAJ Model	CDM Model
XC17xxE	>3,000v	>325v	>1,000v
XCS17xx	>3,000v	>325v	>1,000v
XC31xx/A	>1,750v	>700v	>1,000v
XC3xxx/A	>4,000v	>325v	>2,000v
XC4xxx/A	>1,000v	>800v	>2,000v
XC4xxxE	>3,000v		>2,000v
XC4xxxEX	>3,000v		>2,000v
XC4xxxXL	>2,000v		>1,000v
XC4xxxXLA	>2,000v		>500v
XCxxxxXV	>1500v		
XCVxxx	>1400v		
XCSxx	>6,000v		>1,000v
XCSxxXL	>3,000v		
XC5xxx	>3,000v		>2,000v
XC95xxx	>2,000v		>2,000v
XC95xxXL	>2,000v		>1,000v

Whenever the voltage on a pad approaches a dangerous level, current flows through the protective structures to or from a power supply rail (VCC or ground). In addition, the capacitance in these structures integrate the pulse to provide sufficient time for the protection networks to clamp the input, avoiding damage to the circuit being protected. Geometries and doping levels are chosen to provide ESD protection on all pads for both positive and negative voltages.

Latchup

Latchup is a condition in which parasitic bipolar transistors form a positive feedback loop (Figure 5), which quickly reaches current levels that permanently damage the device. Xilinx uses techniques based on doping levels and circuit placement to avoid this phenomenon. The beta of each parasitic transistor is minimized by increasing the base width. This is achieved with large physical spacings. The butting contacts effectively short the n+ and p+ regions for both wells, which makes the VBE of each parasitic very close to zero. This also makes the parasitic transistors very hard to forward bias. Finally, each well is surrounded by a dummy collector, which forces the VCE of each parasitic almost to zero and creates a structure in which the base width of each parasitic is large, thus making latchup extremely difficult to induce.

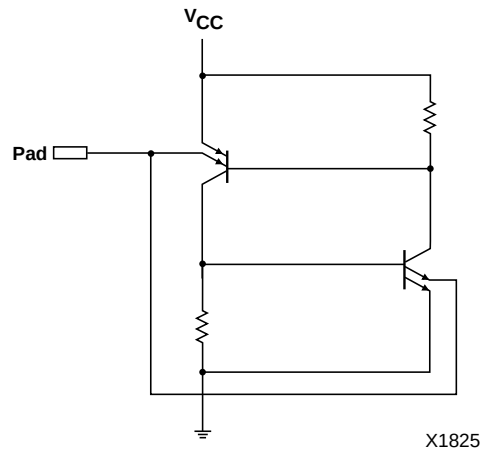

Figure 5: SCR Model

At elevated temperatures, 100 mA will not cause latchup. At room temperature, the FPGA can withstand more than 300 mA without latchup; the EPLD device can withstand more than 200 mA without latchup. However, to avoid metal-migration problems, continuous currents in excess of 10 mA are not recommended.

High Temperature Performance

Though Xilinx guarantees parts to perform only within the specifications of the data sheet, high temperature life testing has been done at 145°C with excellent results.

Revision Control

Version	Date	Revision
2.1	12/14/98	Revised certification dates, updated Figure 1.
3.0	02/01/00	Rewritten for year 2000 updates.

Technical Support, Customer Education, and Services Table of Contents

Technical Support And Services

February 15, 2000 (v3.0)

A complete and uniquely accessible offering of worldwide technical support services is available to Xilinx users.

Xilinx Field Application Engineers at sales offices and technical support centers worldwide provide local engineering support, including design evaluation of new projects, close consultation throughout the design process, special training assignments, and new product presentations. Because their role as advisors and troubleshooters keeps them constantly on the go, they are best used not for general questions, but for more targeted queries such as those related to architectural recommendations. The world-wide network of Xilinx sales representatives and distributors also provide local technical support for Xilinx users.

Technical and applications queries can be directed to support.xilinx.com, the Xilinx technical services web site, or the telephone "hotlines". Xilinx provides 24-hour access to the Answers database, product and applications information, and a variety of files and utilities via support.xilinx.com and the Software Updates area. Hotline telephone support provides access to permanent teams of expert Application Engineers located in the United States, United Kingdom, France, Germany, and Japan. These engineers can handle problems and answer questions right on the spot, and are contributors to, as well as, users of the Answers database, accessible at **support.xilinx.com** (Figure 1).

Many different publications assist users in completing designs quickly and efficiently, including technical manuals, data sheets, application notes, the Xilinx DataSource CD-ROM (a regularly-updated collection of the latest data sheets, application notes and design hints), and the quarterly XCell newsletter. Most of these publications are available on the **support.xilinx.com** web site.

For more in-depth support and instruction, a dedicated training organization conducts technical training classes worldwide. Courses geared for both novice and experienced users are available.

The following Technical Support Services are discussed in more detail in this chapter:

- **support.xilinx.com** (World Wide Web site)
- Software Updates
- Hotline (telephone support)
- Online Software Manuals
- Customer Education

Figure 1: http://support.xilinx.com — For the Designing Engineer

support.xilinx.com Web Site

support.xilinx.com, the Xilinx World Wide Web site, provides instant access to the latest information, ranging from the Configuration Problem Solver, Application Notes, and Data Sheets to online software manuals. It is designed to give users quick, easy, and intuitive access to the desired information.

support.xilinx.com holds a wealth of Xilinx information, readily available at your fingertips. What's more, SmartSearch, our industry-wide search engine, is the definitive resource for all Programmable Logic information on the web. SmartSearch searches over 50 different web sites rich in Programmable Logic content, providing central access to a vast amount of data. SmartSearch Agents will watch the Web for you and inform you via e-mail when new or updated information is added to any of the sites served by SmartSearch. SmartSearch Agents allow you to stay up-to-date in the rapidly changing world of Programmable Logic. You can also use support.xilinx.com to open a case via the web, giving you access to Xilinx Applications Engineers dedicated to providing resolutions to problems that may arise during the desing process.

New information is constantly being added to the Xilinx site. The following is a list of some of the technical information now available on **support.xilinx.com** (as of February, 2000):

- Over 100 Application Notes organized by system type (e.g., PCI, DSP, and PCMCIA), function (e.g., memory functions, arithmetic functions, and busses), component product family, and application.
- Complete and detailed data sheets on all Xilinx products.
- Over 3000 records in our Technical Answers database containing answers to frequently-asked technical questions.
- Xilinx Product Change Notices and Xilinx Customer Updates
- Access to XCell, our quarterly journal for programmable logic users.
- Software Updates
- Links to technical Xilinx presentations via Marshall Electronics' NetSeminarTM archives.
- Configuration Problem Solver
- Online Software Manuals
- Technical and Applications Information
- The Answers Search area of **support.xilinx.com** provides access to technical and applications information that assists design engineers in solving problems. The Answers Search area is accessible from the Xilinx home page under "Troubleshoot".
- The Answers Search area provides access to a variety of technical and applications resources including:
- Over 4000 technical solutions and frequently asked questions.
- The Software Update Area for access to patches, utilities, and updates.
- Expert Journals that provide flow-specific collections of information including FAQs, Tips, and Hot Topics.
- Application Notes
- Information about Worldwide Hotline access
- Learning Services including e-Learning
- Online Software Manuals

File Access and Transfer

Through the file download areas, users have on-line access to a variety of useful files, including user manuals, automated tutorials, design examples, and utilities. Data files can be exchanged with Application Engineers through a secure section of the file download area.

Hotline Telephone Support

A network of Technical Support Hotlines provides Xilinx users with a service contract telephone access to Xilinx Application Engineers dedicated to providing resolutions to problems that may arise during the design process. Xilinx Application Engineers use many of the same resources and databases that are now directly available to users via the support.xilinx.com web site. Technical questions also can be submitted via the web or e-mail. See Table 1 on page 3 for more information.

Technical Literature

Xilinx offers many different publications to assist users in completing designs quickly and efficiently. These include technical manuals, Data Books, data sheets, application notes, the Xilinx DataSource CD-ROM, the XCell newsletter, and the Answers Database. Most of these publications are available on-line at the support.xilinx.com web site.

As part of the development system products, Xilinx provides manuals and supporting documents for the development system tools, libraries, CAE tool interfaces, and related software tools. Many of these manuals are available on the CD-ROM that holds the software as well as in hard-copy format. On-line help facilities also are an integral part of the development system products.

The Xilinx DataSource CD-ROM

The Xilinx DataSource CD-ROM is a collection of current data sheets, application notes and other new technical documentation provided on a CD-ROM for easy reference by the design engineer. All the material on the CD-ROM is provided in Adobe Acrobat format for easy viewing and printing. The Xilinx DataSource CD-ROM is updated regularly as new material becomes available.

Table 1: Hotline Telephone Support

Country	Hours	Hotline	Fax	E-mail
All Regions of the World (support.xilinx.com): >		web site: **http://support.xilinx.com**		
North American Support:	**Mon.- Wed., Fri.** 7:00 AM - 5:00 PM **Thur.** 7:00 AM - 4:00 PM Pacific Time	**800-255-7778** or 408-879-5199		
United Kingdom Support:	**Mon.-Thur.** 9:00 AM - 12:00 PM, 1:00 PM - 5:30 PM **Fri.** 9:00 AM - 12:00 PM, 1:00 PM - 3:30 PM	**(44) 1932-820821**	(44) 1932-828522	ukhelp@xilinx.com
France Support:	**Mon.- Fri.** 9:30 AM - 12:30 PM, 2:00 PM - 5:30 PM	**(33) 1-3463-0100**	(33) 1-3463-0959	frhelp@xilinx.com
Germany Support:	**Mon.-Thur.** 8:00 AM - 12:00 PM, 1:00PM - 5:00 PM **Fri.** 8:00 AM - 12:00 PM, 1:00 PM - 3:00 PM	**(49) 89-93088-130**	(49) 89-93088-188	dlhelp@xilinx.com
Japan Support:	Mon., Tue., Thur., Fri. 9:00 AM - 5:00 PM **Wed.** 9:00 AM - 4:00 PM	**(81) 3-3297-9163**	(81) 3-3297-0067	jhotline@xilinx.com
Korea Support:		**(82) 2-761-4277**	(82) 2-761-4278	korea@xilinx.com
Hong Kong Support:		**(85) 2-2424-5200**	(85) 2-2424-7159	hongkong@xilinx.com

XCell Newsletter

XCell, the quarterly journal for Xilinx programmable logic users, is dedicated to supplying up-to-date information for system designers. A typical issue includes descriptions of new products, updates on component and software availability and revision levels, application ideas, design hints and techniques, and answers to frequently-asked questions.

To add your name to the XCell subscription list, please send your name, company affiliation, and mailing address to XCell editor, via **FAX** at **408-879-4676**.

Xilinx Customer Education

Who Should Recieve Training?

All users of Xilinx products should participate in at least one of our training courses. Participation in a Xilinx training course is one of the fastest and most efficient ways to learn how to design with Xilinx FPGA devices. Hands-on experience with the latest information and software will allow you to implement your own design in less time with more effective use of the devices. Not only design engineers, but also test engineers, component engineers, CAD engineers, technicians, and engineering managers may want to participate in training in order to understand the Xilinx products. Learning Services offers a number of courses in a variety of delivery methods.

Training Course Delivery Methods

1. **Day-Segment Courses**. Xilinx continues to develop and instruct traditional day length courses. Working with various Xilinx product development groups, new courses are created and made available to reflect the current product releases. This serves to make training available when you need it and on the products you need it for. These classes are held in centers around the world. Specific onsite instruction is also available at your facility. Check our Web site at http://support.xilinx.com and click on Courses under Education.
2. **e-Learning.** Xilinx offers both live and recorded one hour e-Learning courses available at the convenience of your own desktop. Check our Web site at http://support.xilinx.com and click on Courses under Education.
3. **Computer-Based Training (CBT)**. Xilinx introduced computer-based training with Verilog CBT. Verilog CBT will allow you to learn the Verilog language at your own pace without ever leaving your office. Verilog CBT is based on the traditional 3-day course, converted into a computerized self-study program.
4. **Modules**. A module is a group of topics, one hour or longer, that are specific to products, audiences, and solutions. They can be taken as stand-alone courses or grouped. Modular courses will be released on a weekly basis. As modules are made available, you can build your own modular library or product-focused reference base. Modules will provide just-in-time training, giving you the ability to access development information quickly. For up-to-date information on modules, check our Web site at http://support.xilinx.com and click on Courses under Education.

What You Will Learn

Not only will you learn about our products, but we will also recommend the best ways to use the software based on our years of experience with thousands of designs. You will learn how to efficiently enter, implement, and verify your design. You can use the Xilinx automatic mode or take a power-user approach and guide the automatic tools to the best implementation of your design.

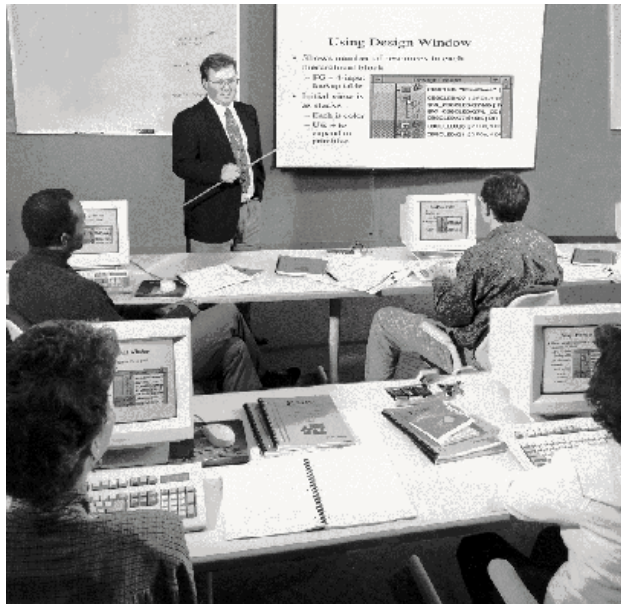

Figure 2: Customer Service Training

Prerequisites

Students need only have a background in digital logic design. Basic familiarity with the PC or workstation is helpful but not required. It will benefit you to learn your design entry tool of choice before attending the Xilinx course.

If you would like to prepare for the training course to maximize your learning, you should complete the tutorials available in the development system. There are tutorials available for the third-party tools for which Xilinx sells the interface.

Benefits

Make Fewer Design Iterations

By learning the proper approach, you will save time and expense in prototyping and debugging designs. However, if you do need to make changes to your design, you will learn how to do this quickly and efficiently.

Get to Market Faster

Getting your product to market faster is probably one of the key reasons you are using Xilinx products in the first place. Studies have shown that time-to-market often has a greater effect on profits than development costs. Training will allow you to get your product to market on schedule, allowing your company to reap the rewards that follow.

Control Your Training Time

With the variety of course delivery vehicles available from Xilinx Customer Education, you can decide how you want and when you want to learn. You set your training schedule

and determine the amount of information you need to complete your design. With the choices of e-Learning, self-study computer-based training, hour-long modules, and full day courses, learning Xilinx products is now flexible. Extensive Xilinx documentation is provided with all course delivery methods.

Lower Production Costs

By learning how to use the device effectively, you may be able to get more logic into a smaller device, and/or operate at a higher speed. As a result, you may be able to save on the cost of the device itself and the surrounding logic on your board.

Increase Quality

Effective verification techniques prove the quality of your Xilinx-based design. Higher quality leads to less maintenance and repair costs, improving customer satisfaction.

Time and Cost Savings

Learning Xilinx software tools is an investment that will pay for itself with the first Xilinx design that you begin. The instructor-led courses are fast-paced, each providing as much information as possible in the short time available. Computer-based training and hourly modules provide just-in-time solutions-based training. With computer-based training, you can set your training pace and hourly modules let you schedule your time efficiently. The hands-on learning experience provided throughout your training ensures that you retain information and are capable of applying it. Just as Xilinx products reduce your development time, the flexibility of the training can reduce your design time.

You can reduce your training costs by:

- Having training conducted at your facility
- Participating in self-education courses with e-Learning, modular or computer-based training

Hands-On Experience

Each course includes hands-on labs. There is at least one computer for every two people in the class.

Platforms

The courses use PC platforms with either WIN95 or NT operating systems.

Instructors

Xilinx training courses have been successfully held worldwide for over eight years. The instructors are Xilinx experts who are skilled at passing that knowledge on to fellow engineers. A dedicated Customer Education organization at Xilinx works closely with the Applications and Engineering groups to keep the courses up-to-date with the latest improvements to Xilinx and third-party tools.

Course Materials

All course materials are supplied by Xilinx. Every student gets an excellent reference tool in the form of course notes, which include all the material presented during the course. The course notes are bound for easy use and include additional reference material beyond what is covered in the course.

Course Descriptions

Instructor-Led Courses

Xilinx courses will cover the latest released versions of our devices and development systems. While all available products will be covered, emphasis will be placed on the more popular and/or recommended solutions. New courses are being produced frequently to ensure a high level of support for our tools. If you have any questions on coverage of a particular product, please go to our Web site at **http://support.xilinx.com** and click on Courses under Education.

Computer-Based Training (CBT)

This is a self-study training technique that allows users to learn at their own pace. Verilog CBT is the first of such training provided by Xilinx. It is based on the popular three-day Verilog class. You can learn a comprehensive Verilog language from the convenience of your desktop by using the Verilog CBT program. This professional learning tool delivers all the essentials for writing, simulating, and synthesizing Verilog HDL for Xilinx devices.

Key Features:

- High-Quality HDL instruction developed by Verilog experts
- Easy navigation through a complete set of Verilog training modules
- Full Indexing for easy reference
- Extensive design exercises and Verilog examples
- Coding guidelines, formatting conventions, and practical tips
- Glossary of key Verilog terms
- Instruction and advice to help you avoid common errors
- Serves as an excellent reference tool for the life of the project
- On-screen instruction with matching audio narration
- Powerful Macromedia CBT application

Modular Courses

A training module is a unit of instruction that can stand-alone or function as a part of a set of modules or a course. Modules will be one or two hours of training content on a specific topic. They will be developed and delivered according to the audience type. New modules and courses will be released weekly, so please check the Web site at http://support.xilinx.com and click on Courses under Education to see the latest and greatest Customer Education offerings. Here are examples of existing audiences and modules:

- **New FPGA Designers**
  - Basic Synchronous Design
  - HDL Editor
  - MAP, PAR
  - Constraints
  - Timing Analyzer
  - Coding Styles
  - Help
  - Intro to VHDL
  - VHDL Language
- **Advanced FPGA Designers**
  - Advanced Constraints
  - Advanced Timing Analyzer
- **Virtex Designers**
  - Virtex Architecture
  - System-level Design Using Virtex
  - Applications

Training Locations

Domestic and International Locations

Xilinx courses are held in North America and also throughout Europe, Asia, India, Israel, Australia, South Africa, and South America. Classes held in international locations vary in length and tuition but are based on the same material used in North America. The schedule lists the courses as well as the contact's name and phone number.

On-Site Courses

Xilinx can bring the training course to your own facility for the greatest convenience to your company.

On-Site Courses Provide Additional Benefits:

No Travel Costs

- On-site Xilinx training courses eliminate travel time and expenses:
  - No airfare
  - No hotel bills
  - No car rental

Courses Tailored To Your Needs

On-site courses can be tailored to meet the specific needs of your company:

- Convenient class time and location
- Projects of a proprietary nature can be discussed openly
- Students can use their own equipment and begin an actual design during the course

Scheduling an On-site Course

To schedule a training class at your facility and determine pricing, call 877-XLX-CLASS [(877) 959-2527]. On-site training courses are popular, so the more advanced notice we have, the better our ability to schedule your class exactly when you want it.

Money-back Guarantee

We are so confident you will be satisfied with the benefits of a Xilinx training course that we offer this guarantee:

- Full refund of the course cost if you are not completely satisfied.

Enrollment

Class size is limited, so early enrollment is recommended. In order to register for a class, please follow the steps listed below:

1. Enroll: Contact the registrar to enroll yourself in a class (877) 959-2527 (877-XLA-CLASS). You must have your tuition payment information available at the time of enrollment. We now accept credit cards (Visa, MasterCard, American Express, and Discover) as well as Purchase Orders and checks.
2. Confirmation: Following enrollment in a class, the registrar will send you a confirmation letter.

Please call **877-XLX-CLASS [(877) 959-2527]** if you have any questions or do not receive a confirmation letter.

If you are unsatisfied or have further questions, call **877-XLX-CLASS [(877) 959-2527] (toll-free)**.

Student Cancellations

Course tuition is fully refundable up to two weeks before the class starts. Cancellations within two weeks (7-13 days) of the class start date will incur a 50% cancellation fee. Those who cancel fewer than 7 days prior to the class will be billed for the full amount of the tuition.

Course Cancellations

Xilinx reserves the right to cancel any class with up to 14 days notice. Typically our process is to look at a class' enrollment numbeR 14 days before a its scheduled start date and determine if the number of students enrolled is sufficient for us to hold or cancel the class. Please be aware of this when booking your travel arrangements.

Application Notes Table of Contents

The Application Notes are in numerical order. To the right of the Application Note title is the Product Family for quick reference. To access the latest version of an Application Note, go to the Xilinx web site at www.xilinx.com/apps/xapp.htm.

For the latest version of an Application Note, go to the Xilinx web site:
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February 15, 2000 (v1.0)

The Application Notes are in numerical order. To the right of the Application Note title is the Product Family for quick reference. To access the latest version of an Application Note, go to the Xilinx web site at www.xilinx.com/apps/xapp.htm.

XAPP008 Complex Digital Waveform Generator **FPGAs**

Complex digital waveforms are generated without the need for complex decoding. Instead, fast loadable counters are used to time individual High and Low periods.

XAPP009 Harmonic Frequency Synthesizer and FSK Modulator **FPGAs**

Uses an accumulator technique to generate frequencies that are evenly spaced harmonics of some minimum frequency. Extensive pipelining is employed to permit high clock rates. A modification of the Harmonic Frequency Synthesizer that automatically switches between two frequencies in accordance with an NRZ input.

XAPP010 Bus Structured Serial Input/Output Device **XC4000**

Simple shift registers are used to illustrate how 3-state busses may be used within an FPGA device. Dedicated wide decoders are used to decode an I/O address range and enable the internal registers.

XAPP011 LCA Speed Estimation: Asking the Right Question **FPGAs**

A simple algorithm is described for determining the depth of logic, in CLBs, that can be supported at a given clock frequency. The algorithm is suitable for XC3000 Series or XC4000 Series FPGA devices.

XAPP013 Using the Dedicated Carry Logic in XC4000E **XC4000**

This Application Note describes the operation of the XC4000/Spartan dedicated carry logic, the standard configurations provided for its use, and how these are combined into arithmetic functions and counters.

XAPP014 Ultra-Fast Synchronous Counters **FPGAs**

This fully synchronous, non-loadable, binary counter uses a traditional prescaler technique to achieve high performance. Typically, the speed of a synchronous prescaler counter is limited by the delay incurred distributing the parallel Count Enable. This design minimizes that delay by replicating the LSB of the counter. In this way even the small longline delay is eliminated, resulting in the fastest possible synchronous counter.

XAPP015 Using the XC4000 Readback Capability **XC4000**

This Application Note describes the XC4000/Spartan Readback capability and its use. Topics include: initialization of the Readback feature, format of the configuration and Readback bitstreams, timing considerations, software support for reading back FPGA devices, and Cyclic Redundancy Check (CRC).

XAPP017 Boundary Scan in XC4000 and XC5200 Series Devices **v3.0 (11/99)** **XC4000**

XC4000/XC5200/Spartan FPGA devices contain boundary scan facilities that are compatible with IEEE Standard 1149.1. This Application Note describes those facilities in detail, and explains how boundary scan is incorporated into an FPGA design.

XAPP018 Estimating the Performance of XC4000E Adders and Counters **XC4000**

Using the XC4000/Spartan dedicated carry logic, the performance of adders and counters can easily be predicted. This Application Note provides formulae for estimating the performance of such adders and counters.

XAPP023 Accelerating Loadable Counters in XC4000 **XC4000**

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www.xilinx.com/apps/xapp.htm

The XC4000/Spartan dedicated carry logic provides for very compact, high-performance counters. This Application Note describes a technique for increasing the performance of these counters using minimum additional logic. Using this technique, the counters remain loadable.

XAPP027 Implementing State Machines in LCA Devices **FPGAs**

This Application Note discusses various approaches that are available for implementing state machines in FPGA devices. In particular, the one-hot-encoding scheme for medium-sized state machines is discussed.

XAPP028 Frequency/Phase Comparator for Phase Locked Loops **FPGAs**

The phase comparator described in this Application Note permits phase-locked loops to be constructed using FPGA devices that only require an external voltage-controlled oscillator and integrating amplifier.

XAPP043 Improving XC4000 Design Performance **XC4000**

This Application Note describes XC4000 architectural features that can be exploited in high-performance designs, and software techniques that improve placement, routing and timing. It also contains information necessary for advanced design techniques, such as floor planning, locking down I/Os, and critical path optimization.

XAPP045 XC4000 Series Technical Information **XC4000**

This Application Note contains additional information that may be of use when designing with XC4000 Series devices. This information supplements the product descriptions and specifications, and is provided for guidance only.

XAPP051 Synchronous and Asynchronous FIFO Designs **XC4000**

This application note describes RAM-based FIFO designs using the dual-port RAM in XC4000 Series devices. Synchronous designs with a common read/write clock are described, as well as asynchronous designs with independent read and write clocks. Emphasis is on the fast, efficient and reliable generation of the handshake signals FULL and EMPTY, which determine design performance.

XAPP052 Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators **XC4000**

Shift registers longer than eight bits can be implemented most efficiently in XC4000 or Spartan Series SelectRAM memory. Using Linear Feedback Shift Register (LFSR) counters to address the RAM makes the design even simpler. This application note describes 4- and 5-bit universal LFSR counters, very efficient RAM-based 32-bit and 100-bit shift registers, and pseudo-random sequence generators with repetition rates of thousands and even trillions of years, useful for testing and encryption purposes. The appropriate taps for maximum-length LFSR counters of up to 168 bits are listed.

XAPP053 Implementing FIFOs in XC4000 Series RAM **XC4000**

This Application Note demonstrates how to use the various RAM modes in XC4000 and Spartan Series logic blocks. A simple FIFO is implemented in several different ways, using combinations of level-sensitive (asynchronous) and edge-triggered (synchronous), single-port and dual-port RAM.

XAPP054 Constant Coefficient Multipliers for the XC4000E **XC4000**

This paper identifies two points at which constant coefficient multipliers become the optimum choice in DSP, and implements constant (k) coefficient multipliers (KCMs) in the XC4000E. It also reveals the solution to an interesting design problem which emerges.

XAPP055 Block Adaptive Filter **XC4000**

This application note describes a specific design for implementing a high-speed, full-precision, adaptive filter in the XC4000E/X family of FPGAs. The design may be easily modified, and demonstrates the suitability of using FPGAs in digital signal processing applications. This application note is based on a 12-bit data, 12-bit coefficient, full-precision, block adaptive filter design. This design can be modified to accommodate different data and coefficient sizes, as well as lesser precision. The application note covers how to modify the design including the trade-offs involved. The filter is engineered for use in the XC4000 Series.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP056 System Design with New XC4000X I/O Features **XC4000**

The XC4000X FPGA family (XC4000EX, XC4000XL, XC4000XLA, XC4000XV) provides several new I/O features, including an additional latch on each input and an output multiplexer on each output. The output multiplexer can also be configured as a two-input function generator. Two different types of clock buffers allow system timing flexibility. These features are discussed, and examples show how to use them.

XAPP057 Using SelectRAM Memory in XC4000 Series FPGAs **XC4000**

XC4000 and Spartan Series FPGAs include SelectRAM memory, which can be configured as ROM or as single- or dual-port RAM, with edge-triggered or level-sensitive timing. This application note describes how to implement SelectRAM memory in a design: in schematic entry, using LogiBLOX synthesis, and HDL synthesis environments. Specifying timing requirements, evaluating performance, and floorplanning are also described.

XAPP058 Xilinx In-System Programming Using an Embedded Microcontroller **All Products**

The Xilinx high performance CPLD and FPGA families provide in-system programmability, reliable pin locking, and JTAG boundary-scan test capability. This powerful combination of features allows designers to make significant changes and yet keep the original device pinouts, eliminating the need to re-tool PC boards. By using an embedded controller to program these CPLDs and FPGAs from an on-board RAM or EPROM, designers can easily upgrade, modify, and test designs, even in the field.

XAPP059 Gate Count Capacity Metrics for FPGAs **FPGAs**

Three metrics are defined to describe FPGA device capacity: Maximum Logic Gates, Maximum Memory Bits, and Typical Gate Range. The methodology used to determine these values is described.

XAPP060 Design Migration from XC4000 to XC5200 **XC4000**

This Application Note reviews the differences between the XC5200 and XC4000 families, recommends approaches for converting XC4000 designs to the XC5200 architecture, and provides a methodology to migrate designs easily in multiple CAE environments.

XAPP062 Design Migration from XC4000 to XC4000E **XC4000**

The XC4000E is an enhanced architecture based on the XC4000 family, but offers many new features, particularly SelectRAM memory. When converting XC4000, XC4000A, XC4000D, and XC4000H designs, the XC4000E is an excellent choice. The conversion process may be as simple as downloading the same bitstream into the XC4000E device (XC4000 and XC4000D bitstreams only), or it may involve changes to the schematic or HDL code. This Application Note describes techniques that should be employed to convert from any of the XC4000, XC4000A, XC4000D, or XC4000H families to the XC4000E family.

XAPP065 XC4000 Series Edge-Triggered and Dual-Port RAM Capability **XC4000**

The XC4000E/X and Spartan FPGA families provide distributed on-chip RAM. SelectRAM memory can be configured as level-sensitive or edge-triggered, single-port or dual-port RAM. The edge-triggered capability simplifies system timing and provides better performance for RAM-based designs. The dual-port mode offers new capabilities and simplifies FIFO designs.

XAPP067 Using Automatic Test Equipment to Program XC9500 Devices In-System **XC9500**

This application note describes how to program XC9500 devices in-system, using standard Serial Vector Format (SVF) stimulus files.

XAPP068 In-System Programming Times **XC9500**

This application note discusses the in-system programming speed of the XC9500 devices.

XAPP069 Using the XC9500 JTAG Boundary Scan Interface **XC9500**

This application note explains the XC9500 boundary scan interface and demonstrates the software available for programming and testing XC9500 CPLDs. An appendix summarizes the JTAG programmer operations and overviews the additional operations supported by XC9500 CPLDs for in-system programming.

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www.xilinx.com/apps/xapp.htm

XAPP070 Using In-System Programmability in Boundary Scan Systems **XC9500**

This application note discusses basic design considerations for in-system programming of multiple XC9500 devices in a boundary scan chain, and shows how to design systems that contain multiple XC9500 devices as well as other IEEE 1149.1-compatible devices.

XAPP071 Using the XC9500 Timing Model **XC9500**

This application note describes how to use the XC9500 timing model. All XC9500 CPLDs have a uniform architecture and an identical timing model, making them very easy to use and understand. To determine specific timing details, users need only compare their paths of interest to the architectural diagrams and, using the timing model presented here, perform a simple addition of incremental time delays.

XAPP073 Designing with XC9500 CPLDs **XC9500**

This application note will help designers understand the XC9500 architecture and how to get the best performance from these devices.

XAPP074 Pin Preassigning with XC9500 CPLDs **XC9500**

This application note describes the planning required for successful pin preassigning and gives a detailed example.

XAPP075 Using ABEL with Xilinx CPLDs **XC9500**

This application note provides a basic overview of the ABEL language and gives examples showing how to use ABEL to fully utilize the specific features of Xilinx CPLDs.

XAPP076 Embedded Instrumentation Using XC9500 CPLDs **XC9500**

This application note shows how to build embedded test instruments into XC9500 CPLDs.

XAPP077 Metastability Considerations **XC9500**

Metastability is unavoidable in asynchronous systems. However, using the formulas and test measurements supplied here for the XC9500 CPLDs, designers can calculate the probability of failure. Design techniques for minimizing metastability are also provided.

XAPP078 XC9536 ISP Demo Board **XC9500**

The demo board described in this application note is a tool for demonstrating the In-System Programming (ISP) capabilities of the XC9500 CPLD family.

XAPP080 Supply Voltage Migration, 5 V to 3.3 V **XC4000**

Mixed voltage environments could create a variety of design challenges. The new 3.3-V XC4000XL, XC4000XLA, and SpartanXL FPGA families are immune to all power sequencing problems and can be interfaced directly with older technology 5-V devices, making them an ideal solution for many mixed voltage systems.

XAPP088 I/O Characteristics of the 'XL FPGAs **XC4000/Spartan-XL**

Data sheets describe I/O parameters in digital terms, providing tested and guaranteed worst case values. This application note describes XC4000XL/XLA and SpartanXL I/O parameters in analog terms, giving the designer a better understanding of the circuit behavior. Such parameters are, however, not production tested and are, therefore, not guaranteed.

XAPP090 FPGA Configuration Guidelines **FPGAs**

These guidelines describe the configuration process for all members of the XC3000, XC4000, XC5200, and Spartan FPGA devices and their derivatives. The average user need not understand or remember all these details, but should refer to the debugging hints when problems occur.

XAPP091 Configuring Mixed FPGA Daisy Chains **FPGAs**

Xilinx FPGAs can be configured in a common daisy chain structure, where the lead device generates CCLK pulses and feeds serial configuration information into the next downstream device, which in turn feeds data into the next downstream device, etc. There is no limit to the number of devices in a daisy chain, and XC3000, XC4000, Spartan, and XC5200 series devices can be mixed freely with only one constraint: the lead device must be a member of the highest order family used in the chain.

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XAPP092 **Configuration Issues: Power-up, Volatility, Security, Battery Back-up** **FPGAs**

This application note covers several related subjects: How does a Xilinx FPGA power up, and how does it react to power supply glitches? Is there any danger of picking up erroneous data and configuration? What can be done to maintain configuration during loss of primary power? What can be done to secure a design against illegal reverse engineering?

XAPP093 **Dynamic Reconfiguration** **FPGAs**

All Xilinx SRAM-based FPGAs can be in-system configured and re-configured an unlimited number of times. This application note describes the procedures for reconfiguring the more traditional Xilinx FPGAs.

XAPP094 **Metastable Recovery** **FPGAs**

Whenever a clocked flip-flop synchronizes an asynchronous input, there is a small probability that the flip-flop output will exhibit an unpredictable delay. The flip-flop can enter a symmetrically balanced transitory state, called metastable (meta = between). Xilinx evaluated the XC4000 and XC3000 series flip-flops. The result of this evaluation shows the Xilinx flip-flop to be superior in metastable performance to many popular MSI and PLD devices.

XAPP095 **Setup and Hold Times** **FPGAs**

Beware of hold time problems, because they can lead to unreliable, temperature-sensitive designs that can fail even at low clock rates.

XAPP096 **Overshoot and Undershoot** **FPGAs**

When users put modern CMOS devices on PC boards, and interconnect them with unterminated lines, there are reflections, commonly called "ringing", that cause overshoots and undershoots of substantial amplitude.

XAPP097 **Xilinx FPGAs: A Technical Overview for the First Time User** **FPGAs**

In the Spartan, XC3000, XC4000, and XC5200 device families, Xilinx offers several evolutionary and compatible generations of Field Programmable Gate Arrays (FPGAs). Here is a short description of their common features. This overview describes two aspects of Xilinx FPGAs: What logic resources are available to the user . How the devices are programmed.

XAPP098 **The Low-Cost, Efficient Serial Configuration of Spartan FPGAs** **Spartan**

This application note shows how to achieve low-cost, efficient serial configuration for Spartan FPGA designs. The approach takes advantage of unused resources in a design, thereby reducing the cost, part count, memory size, and board space associated with the serial configuration circuitry. As a result, neither processor nor PROM needs to be fully dedicated to performing configuration. Information is provided on how the idle processing time of an onboard controller can be used to load configuration data from an off-board source. As a result, it is possible to upgrade a Spartan design in the field by sending the bitstream over a network. A brief summary of Spartan slave serial configuration, its protocol and signals, lays the groundwork for a discussion on ways to reduce bitstream storage and processing requirements. A detailed example illustrates how these techniques can be put into practice. Finally, different formats for configuration data are described along with instructions for their use.

XAPP100 **Choosing a Xilinx Product Family** **All Products**

This Application Note describes the various Xilinx product families. Differences between the families are highlighted. The focus of the discussion is how to choose the appropriate family for a particular application. Covers the Spartan, XC3000, XC4000, XC5200, and XC9500 families.

XAPP102 **XC9500 Remote Field Upgrade** **XC9500**

This application note describes the concept and design of a remote field upgrade subsystem for an in-system programmable XC9500 CPLD. The description of the subsystem is given along with guidelines that should help with variations on it. Additional VHDL files are available for direct use of this design. Specifically, the VHDL files include a complete IRDA receiver design fitting into an XC95108 CPLD.

XAPP103 **The Tagalyzer - A JTAG Boundary Scan Debug Tool** **XC9500**

The Tagalyzer is a diagnostic tool that helps debug long JTAG boundary scan chains. It can be modified to adapt to a wide variety of different testing situations, and is made from a single XC9536 CPLD. It can be used to debug JTAG chains made up of any manufacturer's parts. The Tagalyzer can be expanded to support arbitrarily long boundary scan chains and adapted to change its functionality, as needed.

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XAPP104 A Quick JTAG ISP Checklist **XC9500**

ISP circuitry is beneficial for fast prototype development. However, even the most robust circuitry needs minimal consideration to deliver the best in system programming results. This application brief describes a short list of considerations needed to get the best performance from your ISP designs.

XAPP105 A CPLD VHDL Introduction **XC9500**

This introduction covers the basics of VHDL as applied to CPLDs. Specifically included are those design practices that translate well to CPLDs, permitting designers to use the best features of this powerful language to extract the best performance from CPLD designs.

XAPP107 Synopsys/Xilinx High Density Design Methodology Using FPGA Compiler **XC4000**

This paper describes design practices to synthesize high density designs (i.e. over 100,000 gates), composed of large functional blocks, for today's larger Xilinx FPGA devices using the Synopsys FPGA Compiler. The Synopsys FPGA Compiler version 1998.02, Alliance Series 1.5, and the XC4000X family were used in preparing the material for this application note.

XAPP108 Chip-Level HDL Simulation Using the Xilinx Alliance Series **FPGAs**

This application note describes the basic flow and some of the issues to be aware of for HDL simulation with Alliance Series software. The goal of this document is to familiarize the user with some of the concepts but should not be considered a replacement for the Xilinx or HDL simulator's documentation.

XAPP109 Hints, Tips and Tricks for using XABEL with Xilinx M1.5 Design and Implementation Tools **All Products**

This application note summarizes the issues and design techniques specific to the Xilinx ABEL Interface, version M1.5.

XAPP110 XC9500 CPLD Power Sequencing **XC9500**

Mixed signal systems require logic parts that can operate with two power supplies. XC9500 CPLDs are designed to operate in either mixed 5V/3.3V systems or 5V only systems. To handle both conditions, care has been taken to ensure that designers need not introduce elaborate circuitry to guarantee that 5V and 3.3V power supplies rise or fall in any particular sequence. This application note describes the underlying XC9500 circuitry to give designers the understanding they need to best use these powerful CPLDs.

XAPP111 Using the XC9500XL Timing Model **XC9500XL**

This application note describes how to use the XC9500XL timing model.

XAPP112 Designing With XC9500XL CPLDs **XC9500XL**

This application note will help designers get the best results from XC9500XL CPLDs. Included are practical details on such topics as pin migration, timing, mixed voltage interfacing, power management, PCB layout, high speed considerations and JTAG best practices.

XAPP113 Faster Erase Times for XC95216 and XC95108 Devices on HP 3070 Series Testers **XC9500**

This application note describes an enhanced procedure for utilizing the new faster bulk erase capability of the XC95216 and XC95108 devices on the HP 3070 tester.

XAPP114 Understanding XC9500XL CPLD Power **XC9500XL**

The goal of this application note is to discuss XC9500XL CPLD power estimation and optimization and provide the reader with an understanding of sense-amplifier based CPLD power dissipation. A brief discussion of the process for estimation is given. With this information, you can accurately assess the power dissipation for a design. You will also be given guidelines permitting you to make key choices to manage the power dissipation of your design and understand the package thermal limits.

XAPP115 Planning for High Speed XC9500XL Designs **XC9500XL**

Discovering electrical problems at debug is too late. The printed circuit board has been built and may have to be significantly changed to debug. The best approach is to avoid the problem. By anticipating common problems, designs can be substantially "bullet-proofed" before debug. This means planning for options at the outset is the best solution. A thorough

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but practical checklist is one aspect of planning for success. This application note provides a framework for checklisting a design early to eliminate problems.

XAPP119 **Adapting ASIC Designs for Use with Spartan FPGAs** **Spartan**

Spartan FPGAs are an exciting, new alternative for implementing digital designs that, previously, would have employed ASIC technology. Pre-existing ASIC intellectual property can be adapted for use with Spartan devices by following a straightforward procedure. Each step of the procedure is explained in detail. Guidelines show how an ASIC design, in the form of an RTL-level HDL file, can be revised to take full advantage of the Spartan series' capabilities, thereby achieving efficient, high-performance implementations.

XAPP120 **How Spartan Series FPGAs Compete for Gate Array Production** **Spartan**

This application note discusses the enormous progress made by FPGAs in the areas of technology, low-price and performance. It discusses the major advantages of using FPGAs over traditional gate arrays, which makes FPGAs the best high-volume production solution available today.

XAPP122 **The Express Configuration of SpartanXL FPGAs** **Spartan-XL**

Express Mode uses an eight-bit-wide bus path for fast configuration of Xilinx FPGAs. This application note provides information on how to perform Express configuration specifically for the SpartanXL family. The Express mode signals and their associated timing are defined. The steps of Express configuration are described in detail, followed by detailed instructions that show how to implement the configuration circuit.

XAPP123 **Using Three-State Enable Registers in XLA, XV, and SpartanXL FPGAs** **XC4000XLA, XC4000XV, Spartan-XL**

The use of the internal IOB three-state control register can significantly improve output enable and disable time. This application note shows you how to use hard macros to implement this register in both HDL and schematic based designs.

XAPP124 **Using Manual Power Down Mode With SpartanXL FPGAs** **Spartan-XL**

SpartanXL FPGAs come equipped with a Power Down mode that permits an exceptionally low level of power consumption (ICCO = 100 µA typical), making the family ideal for portable battery-powered applications. This application note provides all the information the designer needs to use Power Down mode effectively, including descriptions of the mode's common applications, internal functioning and electrical characteristics.

XAPP125 **Conserving Power With Auto Power Down Mode in SpartanXL FPGAs** **Spartan-XL**

Power consumption plays an important role in battery-powered applications. SpartanXL FPGAs are designed with segmented routing, 3.3-V operation and advanced process technology to meet the needs for low power and high performance. This application note shows how to reduce power consumption by selectively disabling portions of the design that are not required all the time. Considerable amount of power is saved by disabling the non-critical user logic. This approach is particularly useful for the devices which must be operating all the time. This application note discusses different strategies for reducing the supply current incrementally for an operating device.

XAPP126 **Data Generation and Configuration for Spartan Series FPGAs** **Spartan**

This application note describes various methods to configure Spartan series FPGAs. Each configuration method is described in detail. Information on necessary software programs to run with input files required, output files produced, download cables used, and other hardware necessary to accomplish the task is discussed. This application note targets users who are new to Xilinx devices and Alliance/Foundation series software tools and is intended to make the configuration and debugging flows easy to understand.

XAPP130 **Using the Virtex Block SelectRAM+ v1.2 (01/00)** **Virtex**

The Virtex FPGA Series provides dedicated blocks of on-chip 4096 bit dual-port synchronous RAM. You can use each port of the block SelectRAM+ memory independently as a read/write, read or write port, and configure each port to a specific data width. The Block SelectRAM+ offers new capabilities for the FPGA designer, allowing you to simplify designs.

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XAPP131 **170 MHz FIFOs Using the Virtex Block SelectRAM+** **Virtex**

The Virtex FPGA Series provides dedicated on-chip blocks of 4096 bit dual-port synchronous RAM, which are ideal for use in FIFO applications. This application note describes a way to create a common clock (synchronous) version and an independent clock (asynchronous) version of a 512 x 8 FIFO, with the depth and width being adjustable within the Verilog code. A hand-placed version of the design runs at 170 MHz in the -6 speed grade.

XAPP132 **Using the Virtex Delay-Locked Loop** **Virtex**

The Virtex FPGA series provides four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits which provide zero propagation delay, zero clock skew between output clock signals distributed throughout the device, and advanced clock domain control. You can use these dedicated DLLs to implement several circuits which improve and simplify system level design.

XAPP133 **Using the Virtex SelectIO** **Virtex**

The Virtex FPGA series provides highly configurable, high-performance I/O resources called SelectIO which provide support for a wide variety of I/O standards. SelectIO includes a robust set of features including programmable control of output drive strength, slew rate, and input delay and hold time. Taking advantage of the flexibility and features of SelectIO and the design considerations described in this document can improve and simplify system level design.

XAPP134 **Virtex Synthesizable High Performance SDRAM Controller v2.0 (01/00)** **Virtex**

Synchronous DRAMs are becoming available in speed grades above 100 MHz using LVTTL IOs. The Virtex FPGA family has many features, such as the SelectIO and the Clock Delay Lock Loop, that make it easy to interface to high speed Synchronous DRAMs. This application note describes the design and implementation of a synthesizable, parameterizable, flexible, auto-placed-and-routed synchronous DRAM controller in the Virtex FPGA family. A 32-bit wide data interface version can run up to 125 MHz when automatically placed and routed in a Virtex -6 speed grade. Hand placed versions of the design can run even faster.

XAPP135 **Virtex I/V Curves for Various Output Options** **Virtex**

These typical curves describe the output sink and source current for average processing, nominal supply voltage and room temperature. For the other families see XAPP150. For additional data see the Xilinx IBIS files.

XAPP136 **Synthesizable 143 MHz ZBT SRAM Interface v2.0 (01/00)** **Virtex**

The Virtex Series FPGAs provide access to a variety of on-chip and off-chip RAM resources. In addition to the on-chip SelectRAM and Block SelectRAM+ memory, a Virtex design can interface to megabytes of external high-speed SRAM and DRAM. The combination of high speed SelectIO levels and on-chip Clock Delay-Locked Loop enables the interface to operate at maximum RAM speeds. A Virtex interface to ZBT (Zero Bus Turnaround) SRAM provides interleaved Read/Write without wasteful turnaround cycles.

XAPP137 **Configuring Virtex FPGAs from Parallel EPROMs with a CPLD** **Virtex, XC9500**

Previous generations of Xilinx FPGAs supported a Master Parallel Configuration Mode which allowed the FPGA to configure itself directly from a parallel (byte wide) PROM. The Virtex family of Xilinx FPGAs does not utilize a Master Parallel mode. This application note describes a simple interface design to configure a Virtex device from a parallel EPROM using the SelectMAP configuration mode.

XAPP138 **Virtex Configuration and Readback** **Virtex**

This application note is offered as complementary text to the Configuration section of the Virtex Data Sheet. It is strongly recommended that the Virtex Data Sheet be reviewed prior to reading this application note. This application note first provides a comparison of how Virtex configuration and readback is different from previous Xilinx FPGAs, followed by a complete description of the configuration process and flow. Each of the configuration modes are outlined and discussed in detail, concluding with a complete description of data stream formats, and readback functions and operations.

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XAPP139 Configuration and Readback of Virtex FPGAs Using (JTAG) Boundary-Scan v1.0 (11/99) **Virtex**

This application note demonstrates using a boundary-scan (JTAG) interface to configure and readback Virtex FPGA devices. Virtex devices have boundary-scan features that are compatible with the IEEE Standard 1149.1. This application note is a complement to the configuration section in the Virtex Data Sheet and application note XAPP138: "Virtex Configuration and Readback". Review of both the Virtex Data Sheet and XAPP138 is recommended prior to reading this document.

XAPP141 In-System Programming Times for XC9500XL **Virtex**

This application note discusses the in-system programming speed of the XC9500XL devices.

XAPP144 Designing CPLD Multi-voltage Systems v1.0 (02/00) **XC9500XL**

This application note discusses XC9500XL use in multi-voltage systems.

XAPP150 I/V Curves for Various Device Families **FPGAs**

These typical curves describe the output sink and source current for average processing, nominal supply voltage and room temperature. For the Virtex FPGAs see XAPP135. For additional data see the Xilinx IBIS files.

XAPP151 Virtex Configuration Architecture Advanced Users Guide **Virtex**

The Virtex architecture supports powerful new configuration modes, including partial reconfiguration. These mechanisms are designed to give advanced applications access to and manipulation of on-chip data through the configuration interfaces. This document is an overview of the Virtex architecture, emphasizing data bit locations in the configuration bitstream. Knowing bit locations is the basis for accessing and altering on-chip data. FPGA applications can be built that change or examine the functionality of the operating circuit without stopping the circuit loaded in the chip. A glossary is included to explain some of the terminology used in this application note.

XAPP152 Virtex Power Estimator User Guide **Virtex**

This application note is complementary to the Virtex power estimator worksheet. To use the worksheet, users should have completed a Virtex design with a successful functional simulation.

XAPP153 Status and Control Semaphore Registers Using Partial Reconfiguration **Virtex**

The Virtex FPGA Series supports partial reconfiguration of a cross-section of data while the rest of the circuit is still in operation. This enables a system to read and write specific bits within a LUT configured as RAM, through the configuration port. This application note demonstrates how to lock the LUT SelectRAM to specific locations, determine the corresponding frame of data in the .RBT (Rawbits) file, modify the LUT memory as desired, and re-write this frame into the chip. This provides a microprocessor/FPGA interface through the configuration port with a minimum of IOs.

XAPP154 Virtex Synthesizable Delta-Sigma DAC **Virtex**

Digital to analog converters (DACs) convert a binary number into a voltage directly proportional to the value of the binary number. A variety of applications use DACs including waveform generators and programmable voltage sources. This application note describes a Delta-Sigma DAC implemented in a Virtex FPGA. The only external circuitry required is a low pass filter comprised of just one resistor and one capacitor. Internal resource requirements are also minimal. For example, a 10-bit DAC uses only three Virtex CLBs. The speed and flexible output structure of the Virtex series FPGAs make them ideal for this application.

XAPP155 Virtex Analog to Digital Converter **Virtex**

When digital systems are used in real-world applications, it is often necessary to convert an analog voltage level to a binary number. The value of this number is directly or inversely proportional to the voltage. The analog to digital converter (ADC) described here uses a Virtex FPGA, an analog comparator, and a few resistors and capacitors. An 8-bit ADC can be implemented in about 16 Virtex CLBs, and a 10-bit ADC requires about 19 CLBs.

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XAPP158 Powering Virtex FPGAs **Virtex**

The power consumption of Xilinx FPGAs depends upon the number of internal logic transitions and is then proportional to the operating clock frequency. Unless adequate heat sinking is provided, the heat generated could easily exceed the maximum allowable junction temperature. Other power supply requirements including initial conditions, transient behavior, turn-on and turn-off are also important. Bypassing or decoupling the power supplies at the device requires careful consideration of the specific supply currents and the device clock frequencies.

XAPP161 XC1700 and XC1800 Design Migration Considerations **FPGAs**

Designing a board with Xilinx PROMs is advantageous because migration between XC1700 and XC1800 series devices is simple. This application note discusses two migration paths: XC1700 designs upgrading to XC1800, and XC1800 designs migrating to XC1700 for production-stable cost reductions. The topics discussed are pinout compatibility, power and ground connections, and boundary-scan chain integrity.

XAPP164 Using Xilinx and Synplify for Incremental Designing (ECO) **FPGAs**

Guided place and route (PAR) can help you reduce runtimes when incremental changes are made to a design, such as for an Engineering Change Order (ECO). By making only small changes to a design along with optimizing only the changed block(s), you allow guided PAR to perform at its best, preserving timing and reducing PAR runtimes. To localize the design changes without affecting the remainder of your design, either a top-down preserving hierarchy or a bottom-up methodology must be used.

XAPP165 Using Xilinx and Exemplar for Incremental Designing (ECO) **FPGAs**

Guided place and route (PAR) can help you reduce runtimes when incremental changes are made to a design, such as for an Engineering Change Order (ECO). By making only small changes to a design along with optimizing only the changed block or blocks, you allow guided PAR to perform at its best, preserving timing and reducing PAR runtimes. To localize the design changes without affecting the remainder of your design, either a top-down preserving hierarchy or a bottom-up methodology must be used.

XAPP166 TAU/BLAST Support in 2.1i **FPGAs**

The Xilinx 2.1i development system adds Stamp Model Generation. This feature supports the use of board level Static Timing Analysis tools, such as Mentor Graphics' Tau and Viewlogic's Blast. With these tools, users of Xilinx programmable logic products can accelerate board level design verification.

XAPP168 Getting Started With the MultiLINX Cable **FPGAs**

This application note provides a quick introduction to the MultiLINX cable hardware. Topics covered are a description of the cable, how to order a MultiLINX system, a list of features, what the cable may be used for, the current software support, and how to integrate cable access into a users' board. For more information on the MultiLINX cable and other hardware products from Xilinx, please refer to the Hardware User's Guide.

XAPP169 MP3 NG: A Next Generation Consumer Platform v1.0 (01/00) **Spartan-II**

This application note illustrates the use of a Xilinx Spartan-II FPGA and an IDT RC32364 RISC controller in a handheld, consumer electronics platform. Specifically the target application is an MP3 audio player with advanced user interface features. In this application the Spartan device is used to implement the complex system level glue logic required to interface and manage the memory and I/O devices.

XAPP170 Implementing an ISDN PCMCIA Modem Using Spartan Devices v1.0 (7/99) **Spartan**

This application note illustrates the use of Spartan devices in an ISDN modem. The design example shows how cost effective a Spartan device can be in these applications. While the design is targeted at solving a specific problem, it illustrates solutions to a number of general technical issues.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP171 **Implementing an ADSL to USB Interface Using Spartan Devices** **v1.0 (3/99)** **Spartan**

This application note illustrates the use of Spartan devices in an ADSL modem. The Spartan device is used to implement the complex system level glue logic required for the modem's USB interface and manages DMA transfers of ATM cells. The design example shows how cost effective a Spartan device can be in these applications. While the design is targeted at solving a specific problem, it illustrates solutions to a number of general technical issues. These include implementing Utopia interfaces for ATM devices and remote configuration of Spartan devices.

XAPP172 **The Design of a Video Capture Board Using the Spartan Series** **v1.0 (3/99)** **Spartan**

This application note describes a reference design for a video capture board that acts as an interface between a video source such as a camcorder, VCR, CCD camera, etc. and a PC. The board captures and digitizes frames from a video source, which it then transfers to a PC for viewing. The main electronic components consist of a video pixel decoder, DRAM and a Spartan FPGA, all chosen to achieve a low overall cost, making the board suitable for high-volume, consumer-oriented products. To this end, the ability to implement all the interface and memory control logic in a single programmable Spartan device provides crucial benefits including low cost, reduced part count, a small form factor, low power, and easy field upgrades.

XAPP173 **Using Block SelectRAM+ Memory in Spartan-II FPGAs** **v1.0 (01/00)** **Spartan-II**

The Spartan-II FPGAs provide dedicated blocks of true dual-port RAM, known as Block SelectRAM+ memory. This dedicated memory provides a cost-effective use of resources without sacrificing the existing distributed SelectRAM memory or logic resources. The Block SelectRAM+ memory is fully synchronous for easy timing analysis and is easily initialized at configuration. This additional integration capability makes the Spartan-II family ideal for cost-sensitive applications.

XAPP174 **Using Delay-Locked Loops in Spartan-II FPGAs** **v1.0 (01/00)** **Spartan-II**

The Spartan-II series provides four fully digital dedicated on-chip Delay-Locked Loop (DLL) circuits, which provide zero propagation delay, low clock skew between output clock signals distributed throughout the device, and advanced clock domain control. These dedicated DLLs can be used to implement several circuits that improve and simplify system level design.

XAPP175 **High Speed FIFOs In Spartan-II FPGAs** **v1.0 (01/00)** **Spartan-II**

This application note describes how to build high-speed FIFOs using the Block SelectRAM+ memory in the Spartan-II FPGAs. Verilog and VHDL code is available for the design. The design is for a 512x8 FIFO, but each port structure can be changed if the control logic is changed accordingly. Both a common-clock version and an independent-clock version are described.

XAPP176 **Spartan-II FPGA Family Configuration and Readback** **v1.0 (01/00)** **Spartan-II**

This application note is offered as complementary text to the configuration section of the Spartan-II data sheet. It is strongly recommended that the Spartan-II data sheet be reviewed prior to reading this note. Spartan-II FPGAs offer a broader range of configuration and readback capabilities than previous generations of Xilinx FPGAs. This note first provides a comparison of how Spartan-II configuration is different from previous Xilinx FPGAs, followed by a complete description of the configuration process and flow. Each of the configuration modes are outlined and discussed in detail, concluding with a complete description of data stream formats, and readback functions and operations.

XAPP177 **Spartan-II Family I/V Curves for Various Output Options** **v1.0 (01/00)** **Spartan-II**

These typical curves describe the output sink and source current for average processing, nominal supply voltage and room temperature for the Spartan-II family of FPGAs. These curves are graphical representations of IBIS models, which are traditionally used for system and board-level simulation.

XAPP178 **Configuring Spartan-II FPGAs from Parallel EPROMs** **v1.0 (01/00)** **Spartan-II**

This application note describes a simple CPLD-based interface design to configure a Spartan-II device from a parallel EPROM using the Slave Parallel configuration mode.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP179 Using SelectI/O Interfaces in Spartan-II FPGAs v1.0 (01/00) Spartan-II

The Spartan-II FPGA family simplifies high-performance design by offering SelectI/O inputs and outputs. The Spartan-II devices can support 16 different I/O standards with different specifications for current, voltage, I/O buffering, and termination techniques. As a result, the Spartan-II FPGA can be used to integrate discrete translators and directly drive the most advanced backplanes, busses, and memories. This application note describes how to take full advantage of the flexibility of the SelectI/O features and the design considerations to improve and simplify system level design.

XAPP200 Virtex Synthesizable 1.6 Gbytes/s DDR SDRAM Controller. v2.0 (01/00) Virtex

The DLLs and the SelectI/O features in the Virtex architecture make it the perfect choice for implementing a controller of a Double Data Rate (DDR) SDRAM. This application note describes the reference controller design for a 64-bit DDR SDRAM. At a clock rate of 100 MHz, and data changing at both clock edges, a peak bandwidth of 1.6 Gbytes/s is obtained. The reference design is synthesizable and achieves 100 MHz performance with auto place and route tools.

XAPP201 An Overview of Multiple CAM Designs in Virtex Devices Virtex

Flexible CAMs (Content Addressable Memory) are implemented in Virtex devices by taking advantage of the reprogrammability of the basic LUT as a Shift Register or a SelectRAM memory and the fast carry logic chain. Although Cams are also feasible in Spartan and XC4000X devices, this application note concentrates on Virtex devices. The flexibility of a Virtex device is a key advantage in designing a CAM. The application must decide the best implementation.

XAPP202 Content Addressable Memory (CAM) in ATM Applications Virtex

Content Addressable Memory (CAM) or associative memory, is a storage device which can be addressed by its own contents. Each bit of CAM storage includes comparison logic. A data value input to the CAM is simultaneously compared with all the stored data. The match result is the corresponding address. A CAM operates as a data parallel processor. CAMs can be used to design Asynchronous Transfer Mode (ATM) switches. Implementing CAM in ATM applications are specifically described in this application note. As a reference, the application note XAPP201 “An Overview of Multiple CAM Designs in Virtex Devices” presents diverse approaches to implement CAM in other designs.

XAPP203 Designing Flexible, Fast CAMs with Virtex Slices Virtex

Content Addressable Memories (CAM) allow a fast search for specific data in a memory. Each application has different CAM requirements. A CAM design implemented in Virtex slices offers a flexible approach to CAM depth and width based upon LUTs configured as Shift Registers. This application note describes a fast CAM design finding a match in a single clock cycle. The application note XAPP201 “An Overview of Multiple CAM Designs in Virtex devices” discusses the diverse solutions available when implementing CAM and introduces the specific solution described in this application note.

XAPP204 Using Block SelectRAM+ for High-Performance Read/Write CAMs Virtex

CAM (Content Addressable Memory) offers increased data search speed. In various applications based on CAM, there are differing requirements for data organinzatation and read/write performance. The innovative design described in this application note is suited for small embedded CAMs with high-speed match and write requirements. The reference design is built using the Dual Read/Write Port™, Block RAM feature of the Virtex family. An earlier application note, XAPP201 "An Overview of Multiple CAM Designs in Virtex Family Devices", discusses the diverse solutions available when implementing CAM while introducing the specific solution described in this application note.

XAPP205 Data-Width Conversion FIFOs using the Virtex Block SelectRAM Memory Virtex

The Virtex FPGA series provides dedicated on-chip blocks of 4096-bit dual-port synchronous RAM (Block SelectRAM+™). The Block SelectRAM feature is ideal for use in FIFO applications. This application note describes how to create a common-clock (synchronous) version and an independent-clock (asynchronous) version of a FIFO for data-width conversion with different width Read and Write data ports.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP208 **An Inverse Discrete Cosine Transform (IDCT) Implementation in Virtex Devices for MPEG Video Applications v1.1 (01/00)** **Virtex**

This application note describes an implementation of IDCT in the Virtex family. DCT/IDCT are used in the MPEG video standard to reduce the bandwidth requirements. IDCT is one of the most computation-intensive parts of the MPEG decoding process. A fast, hardware based IDCT implementation is crucial to speed the MPEG decoding process. In this implementation, the inherent parallelism is exploited to achieve throughput as high as 3.28 Gbits/s, making it suitable for real time video applications. The implementation is synthesizable Verilog code at the RTL level.

XAPP211 **PN Generators Using the SRL Macro v1.0 (2/00)** **Virtex/Spartan-II**

Pseudo-random Noise (PN) generators are at the heart of every spread spectrum system. Many PN generators are required within Code Division Multiple Access (CDMA) base stations. PN generators are used to implement synchronization and uniquely code individual user signals across the transmission interface. PN generators are based upon Linear Feedback Shift Registers (LFSRs). Every Look-Up-Table (LUT) in a Virtexä device can be configured as a 16-bit shift register (SRL16 macro). Hence, Virtex devices implement efficient LFSRs and deliver a significant reduction in resource utilization when compared with alternative flip-flop only PLD structures. For example, a 16-stage LFSR can be realized in just one LUT.

XAPP210 **Linear Feedback Shift Registers in Virtex Devices** **Virtex**

This application note describes the implementation of Linear Feedback Shift Registers (LFSR) using the Virtex SRL macro. One half of a CLB can be configured to implement a 15-bit LFSR, one CLB can implement a 52-bit LFSR, and with two CLBs a 118-bit LFSR is implemented.

XAPP230 **The LVDS I/O Standard** **Virtex-E**

This application note describes the LVDS I/O standard. LVDS provides higher noise immunity than single-ended techniques, allowing for higher transmission speeds, smaller signal swings, lower power consumption, and less electro-magnetic interference than single-ended signaling. Differential data can be transmitted at these rates using inexpensive connectors and cables. LVDS provides robust signaling for high-speed data transmission between chassis, boards, and peripherals using standard ribbon cables and IDC connectors with 100 mil header pins. Point-to-point LVDS signaling is possible at speeds of up to 622 Mb/s.

XAPP231 **Multi-Drop LVDS with Virtex-E FPGAs** **Virtex-E**

This application note describes how to use LVDS signaling for high-performance multi-drop applications with Virtex-E FPGAs. Multi-drop LVDS allows many receivers to be driven by one Virtex-E LVDS driver. Simulation results indicate that the reference design described here will operate from DC up to 311 Mbits/s. This application note includes DC specifications, microstrip and layout guidelines. With simple source and differential termination, Virtex-E FPGAs drive multi-drop LVDS directly, replacing costly TTL-LVDS drivers and receivers, reducing board area and skew for high-performance applications. The Virtex-E driver actually improves signal integrity over other LVDS drivers by absorbing any reflected energy at the source instead of passing it on down the line. This innovation enables 311 Mb/s signaling on multi-drop lines with as many as 20 LVDS receivers, spanning distances of over four feet in the reference design, with high signal integrity and noise immunity.

XAPP232 **Virtex-E LVDS Drivers & Receivers: Interface Guidelines v1.0 (11/99)** **Virtex-E**

This application note describes how to use the new Virtex-E LVDS (low-voltage differential signaling) drivers and receivers for high-performance LVDS interfaces to industry-standard LVDS devices. LVDS provides higher noise immunity than single-ended techniques, allowing for higher transmission speeds, smaller signal swings, lower power consumption, and less electro-magnetic interference than single-ended signaling. Differential data can be transmitted at these rates using inexpensive connectors and cables. Virtex-E LVDS drivers offer improved signal integrity over other LVDS drivers because they absorb reflected signals unlike other LVDS drivers.

XAPP233 **Multi-channel 622 MHz LVDS Data Transfer with Virtex-E Devices v1.0 (12/99)** **Virtex-E**

The Virtex-E FPGA Series provides dedicated on-chip differential receivers between adjacent user I/O pins, which are ideal for receiving LVDS signals at speeds of up to 622 Mbits/s in the -7 speed grade. This application note describes how to create a high-speed LVDS receiver and transmitter on a single Virtex-E FPGA suitable for point-to-point data transmission at a data rate of 622 MHz. The design utilizes a guide file for optimal routing.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP234 Virtex SelectLink Communications Channel v1.0 (12/99) **Virtex-E**

Systems that include two or more FPGAs often require high-bandwidth data paths between devices. As the clock period and switching times of digital circuits become shorter, straightforward methods of transferring data between devices are often inadequate. At high frequencies, signal propagation delay and reflections that occur in conductors just a few centimeters long must be taken into account. The SelectLink™ communications channel utilizes special features of the Virtex family, including Delay Locked Loops, Block SelectRAM+, and SelectI/O, to create a system that can move large amounts of data between FPGAs at very high speeds. A code generation tool available at www.xilinx.com allows logic designers everywhere to instantly create customized SelectLink Verilog source code. The modules are easily instantiated in the designers top level code for a complete system solution.

XAPP235 Virtex™-E Package Compatibility Guide **Virtex-E**

This package compatibility guide describes the advance Virtex-E pin-outs and established guidelines for package compatibility between Virtex and Virtex-E devices. The information in this guide is advance in nature and subject to change at any time. For the latest information regarding Virtex-E devices, see the Xilinx web sit at http://www.xilinx.com.

XAPP300 In-System Programming (ISP) **CoolRunner**

Describes JTAG and ISP background information, and specific features in the CoolRunner CPLDs.

XAPP302 Metastability Characteristics for CoolRunner CPLDs **CoolRunner**

If setup and hold times are violated, there is a finite chance that the flip-flop will not immediately latch a high or low but get caught half way in between. This is the metastable state and it is manifested in a bistable device by the outputs glitching, going into an undefined state, oscillating, or by the output transition being delayed for an indeterminable time. The probability that it will still be metastable some time later has been shown to be an exponentially decreasing function. A designer can simply wait for some added time after the specified propagation delay before sampling the flip-flop output so that he can be assured that the likelihood of metastable failure is remote enough to be tolerable. On the other hand, there is some probability (albeit vanishingly small) that the device will remain in a metastable state forever. The designer needs to know the characteristics of metastability so that he can determine how long he must wait to achieve his design goals. The following information on the CoolRunner CPLDs is provided to fill this basic need to know how the device operates in situations where metastability may be a problem.

XAPP307 Terminating Unused CoolRunner I/O Pins **CoolRunner**

The CoolRunner family of CPLDs are the first PLDs to employ a TotalCMOS design methodology. Because these devices are fabricated on CMOS process technology, it is important to consider the options available in terminating unused pins. Allowing unused inputs and I/O pins to float can cause the voltage on the pin to be in the linear region of the CMOS input structures, which can increase the power consumption of the device. All unused dedicated inputs and JTAG/ISP function pins (when JTAG/ISP is used) on CoolRunner devices must be terminated. For unused I/O pins, some CoolRunner devices have on-chip, programmable, weak pull-down resistors that can be used for termination, but other devices require termination by the user.

XAPP308 ISP Design Considerations for CoolRunner CPLDs **CoolRunner**

This application note addresses board design considerations, i.e., signal integrity, power supply decoupling, power supply filtering, and component placement that will allow you to utilize the advantages of CoolRunner ISP, in an actual design environment, without headaches.

XAPP310 Power Up Reset Characteristics of CoolRunner CPLDs **CoolRunner**

Depending upon where and how CoolRunner CPLDs are used, the power up characteristics may be of interest.

XAPP311 Five Volt Tolerance and PCI **CoolRunner**

The purpose of this application note is to investigate the PCI (Peripheral Component Interface) environment when using 5 volt tolerant, 3.3 volt supply integrated circuits. In particular, we will examine the meaning of the statement “PCI compliant” when used in CPLD or FPGA data sheets.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP312 **Differences In ABEL and PHDL** **v1.0 (11/99)** **CoolRunner**

This document highlights the few major differences between ABEL and PHDL. All other PHDL constructs and syntax not discussed in this document are supported in ABEL. Most PHDL designs will be accepted in Xilinx Project Navigator with just a modification to the file extension.

XAPP313 **Achieving High Performance in a CoolRunner XCR3960** **v1.0 (11/99)** **CoolRunner**

High-performance designs can be successfully implemented in the XCR3960 with a general understanding of its architecture and guiding the compilation and fitting processes with a control file. This document provides an overview of the XCR3960 architecture, compiler and fitter options along with an example to provide a resource for high-performance system designers.

XAPP315 **Implementing an I2C Bus Controller in a CoolRunner CPLD** **v1.0 (11/99)** **CoolRunner**

This document details the VHDL implementation of an I2C controller in a Xilinx CoolRunner 128 macrocell CPLD. CoolRunner CPLDs are the lowest power CPLDs available and thus are the perfect target device for an I2C controller. The VHDL code described in this document can be obtained by contacting Xilinx Technical Support.

XAPP316 **Xilinx Project Navigator XST - XPLA Professional Design Flow for CoolRunner CPLDs** **v1.0 (10/99)** **CoolRunner**

This document provides an overview of the design flow for WebPACK Verilog/VHDL users targeting the Xilinx CoolRunner CPLDs.

XAPP327 **Fitting Designs Efficiently Into CoolRunner CPLDs** **v1.0 (02/00)** **CoolRunner**

Design performance is directly related to how well a design is fit to a CoolRunner™ CPLD, therefore it is important to understand the architecture of the CoolRunner CPLDs as well as how the compiler/fitter behaves. This document briefly reviews the architecture of the CoolRunner CPLDs, but more specifically describes how to control the compiler and fitter options in XPLA Professional to obtain the desired fit.

XAPP328 **Design of an MP3 Portable Player Using a CoolRunner CPLD** **v1.1 (12/99)** **CoolRunner**

The CoolRunner family of CPLDs includes versatile clocking options that include both synchronous (external) and asynchronous (internal, equation-based) clocking and selectable clock polarity at every macrocell. This application brief describes in detail these clocking options, and shows how to access these features using Xilinx XPLA Designer. We also detail how to synthesize ‘soft’ flip-flops and latches for those instances where these devices can be useful.

XAPP332 **Pin Locking in CoolRunner XPLA3 CPLDs** **CoolRunner**

This document highlights the architectural features provided with CoolRunner CPLDs that enable pin assignments to be maintained through many design iterations.

XAPP333 **CoolRunner XPLA3 I2C Bus Controller Implementation** **CoolRunner**

This document details the VHDL implementation of an I2C controller in a Xilinx CoolRunner XPLA3 256 macrocell CPLD. CoolRunner CPLDs are the lowest power CPLDs available, making this the perfect target device for an I 2 C controller. The VHDL code described in this document can be obtained by contacting Xilinx Technical Support.

XAPP334 **Utilizing XPLA3 Universal Control Terms** **CoolRunner**

This document highlights the advantages of utilizing the universal control terms provided in the CoolRunner XPLA3 CPLD architecture. Design examples showing the efficiency of these universal control terms are discussed.

XAPP400 **Constraining Virtex Design in 2.1i** **Virtex**

Constraining a Virtex Design is different in 2.1i compared to older versions of the software. There are improvements in the Trace, Timing Analyzer, FloorPlanner, Constraints Editor, and other implementation tools to help make the designing procedure easier for Virtex. This paper is devoted to describing some of the simple steps necessary to constraining a Virtex design with the new 2.1i implementation tools. The major focus of this paper is to explain how to constrain with a CLKDLL in Virtex and the new look of the Timing Analyzer Reports.

For the latest version of an Application Note, go to the Xilinx web site:
www.xilinx.com/apps/xapp.htm

XAPP401 2.1i FPGA Editor (10/99) **FPGAs**

This application note presents the new, easier to use FPGA Editor and how it differs from the previous version of EPIC. For general FPGA Editor usage, refer to the FPGA Editor Guide. This application note will also cover how to return to EPIC type actions for zoom and pan actions.

XAPP402 2.1i Floorplanner Support for Virtex FPGAs (10/99) **Virtex**

With the release of M2.1i, the Floorplanner will support the Virtex family of FPGAs. This application note will show you how the major Virtex-specific architectural features such as BlockRAMs, global clock buffers, DLLs, and carry logic are represented within the Floorplanner GUI and how you can manipulate a design containing these elements. The general operation of the 2.1i Floorplanner is identical to that of the Floorplanner in the previous, 1.5i release.

XAPP403 Using the Version 2.1i Xilinx Design Manager and Flow Engine (DMFE) **FPGAs**

Welcome to the version 2.1i Xilinx Design Manager (DM) and Flow Engine (FE). The functionality of both DM and FE has been significantly enhanced in this release. In 2.1i, the focus for DM/FE has been to improve "ease of use". A number of new features are provided including "self contained revisions" and the "Smart" Flow Engine, to name a few. These and many other new features are explained in the sections that follow.

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