August 6, 1996 (Version 1.1)

XACT*step:* Accelerating Your Productivity

The newest version of the XACT development system, XACT*step*, started shipping in the fourth quarter of 1995.

XACT*step* software features a revolutionary combination of power and ease-of-use to provide accelerated learning curves, short implementation cycles, and faster design debug. This high-productivity environment contains six new productivity tools that are easily accessible through graphical tool bars, icons and pop-up menus. They support the complete spectrum of programmable logic design methodology from fully automatic to hand-crafted.

All the tools in XACT*step* feature a new graphical user interface (GUI). On the PC, the GUI is fully Microsoft Windows compliant.

With this new GUI, all programs are executed from tool bars and icons. Tool tips provide instant descriptions and on-line help is available for more in-depth information. Report browsers present message files with plain English titles and allow simultaneous viewing of multiple documents.

Six Powerful New Tools

- The new Design Manager provides a complete project management environment for a wide range of families. It provides version control, device re-targeting and design re-use.
- The configurable Flow Engine lets designers choose the amount of control they want over the implementation process. They can choose a fully automatic flow or set break points that allow analysis and optimization of results before proceeding to the next step.
- XACT*step* contains the industry's first graphically-based hierarchical Floorplanner. This tool provides techniques that have proven to be extremely valuable to gate array and custom silicon designers. Using floorplanning, it is easy to achieve hand-crafted levels of performance and density without resorting to low-level manual techniques. Floorplanning is valuable for any design that has a high degree of structure or a large number of gates. It also allows optimization of specialized structures like Xilinx unique high-speed distributed RAM and three-state internal bus features.
- The new interactive Timing Analyzer makes it easy to quickly determine a design's performance by generating custom timing reports. Using pop-up menus, it is quickly configured to show the delay along a specific path or group of paths. It also shows the delay along all paths of a certain type or those associated with a specific clock signal. In addition, the Timing Analyzer automatically compares the design's actual performance to XACT-Performance goals and shows the estimated maximum frequency for each clock in the design.
- The Hardware Debugger allows verification of configuration data and viewing of internal signal activity. It takes advantage of the reprogrammability of SRAM-based devices by configuring the FPGA in-circuit using a cable connected to a host PC or workstation. After configuring the device, bitstream data is read back through the cable for automatic verification.
  While the device is running, an unlimited number of internal nodes can be probed and displayed in a waveform window.
- The new PROM Formatter in XACT*step* assists the designer in creating PROM programming files. This tool chooses the best PROM size or automatically splits the data into multiple files if multiple PROMs are required. It supports serial and byte-wide PROMs in four different formats. If the target system uses the daisy chain capability of the Xilinx FPGA, the PROM formatter graphically creates the load order and verifies the load sequence.

The Xilinx Design Manager—Simplifies the Design Flow

- Source and revision control
- Permits running all Xilinx software from menus
- Automates design translation via XMake facility
- Provides on-line help for all menus, programs and options

Flow Engine

- Automatically invokes all implementation programs as required to compile a design into an FPGA or CPLD
- Supports hierarchically-structured designs

Extensive On-line Help

- The Design Manager contains on-line Help for
  Every menu
  Every program
  Every program option
  Design-flow suggestions

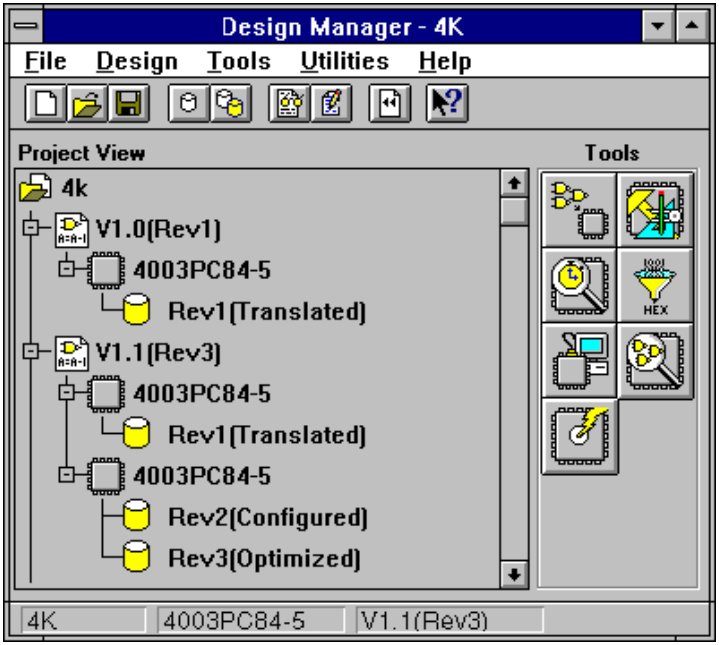

Figure 1: Design Manager Main Window

Design Flow Overview

This section describes the Xilinx Automated CAE Tools (XACT) design environment for Xilinx FPGA and CPLD devices.

High-density programmable logic has created unique requirements for CAE software; the tools must deliver the ease-of-design and fast time-to-market benefits that have popularized FPGA and CPLD technologies, must be capable of implementing high-density logic designs on an engineer's desktop system, and must be easy-to-use and compatible with the user's existing design environment.

In order to meet those needs, Xilinx offers a variety of development system products optimized to support the Xilinx FPGA and CPLD architectures. Available products include state-of-the-art design implementation software, libraries and interfaces to popular schematic editors, synthesis and timing simulators, and behavioral-based design entry tools. All Xilinx development system software is integrated under the Xilinx Design Manager, providing designers with a common user interface regardless of their choice of device architecture and tools.

As with other logic technologies, the basic methodology for FPGA design consists of three interrelated steps: entry, implementation, and verification. (Figure 2 - Figure 4). The design process is iterative, returning to the design entry phase for correction and optimization. Popular generic tools are used for entry and simulation (for example, Viewlogic System's PROcapture schematic editor and PROsim simulator), but architecture-specific tools are needed for implementation.

Design Entry

Schematic editors and synthesis are the most-popular methodologies for design entry. FPGA/CPLD symbol libraries and netlist interfaces are available for schematic editors from vendors such as Viewlogic, OrCAD, Mentor Graphics, and Cadence. These libraries reflect the wide variety of logic functions that can be implemented in FPGA/CPLD devices.

Behavioral-oriented design entry methods, including Boolean equations and state-machine descriptions, are supported by the Xilinx ABEL and LogiBloxs products, as well as a number of products from CAE vendors such as Data I/O, Logical Devices, MINC, and ISDATA.

As the density and complexity of FPGA and CPLD designs increase to 10,000 gates and beyond, gate-level entry tools often are cumbersome, and the use of logic synthesis and high-level description languages (HDLs), such as VHDL and Verilog, can raise designer productivity. The use of HDLs requires synthesis tools that effectively compile designs for the target architecture. Xilinx offers interfaces for synthesis tools from Synopsys. Other CAE vendors, such as Mentor Graphics, Cadence Design Systems, Viewlogic, and Exemplar Logic, also offer synthesis tools tailored for the Xilinx device architectures.

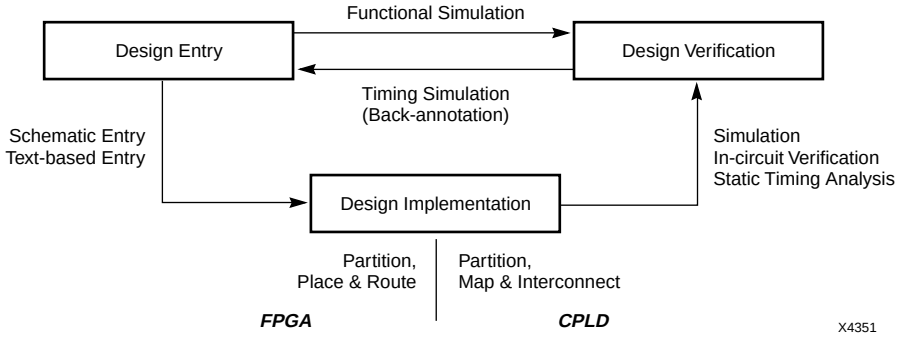

Figure 2: FPGA/CPLD Design Flow

Many engineers prefer visually oriented design-entry techniques over text-based HDLs. The benefits of HDLs are provided to these designers with tools that provide high-level design constructs in a symbolic format compatible with graphics-based schematic editors. X-BLOX is a graphics-based high-level language that allows designers to use a schematic editor to enter designs as a set of generic modules. The X-BLOX compiler optimizes the modules for the target device architecture, automatically choosing the appropriate architectural resources for each function.

The XACT*step* design environment supports hierarchical design entry, with top-level drawings defining the major functional blocks, and lower-level descriptions defining the logic in each block. The implementation tools automatically combine the hierarchical elements of a design. Different hierarchical elements can be specified with different design entry tools, allowing the use of the most convenient entry method for each portion of the design. In this type of 'mixed-mode' design entry, designers can intermix schematic, text, gate-level and behavioral-level design, permitting the re-use of previously designed modules and easing the transition to higher-level design methodologies.

Design Implementation

After the design is entered, implementation tools map the logic into the resources of the target device architecture, determine an optimal placement of the logic, and select the routing channels that connect the logic and I/O blocks. Xilinx design implementation tools apply a very high degree of automation to these tasks. A design compilation utility automatically retrieves the design's input files and performs all the necessary steps to create the CPLD or FPGA configuration program.

For demanding applications, the user can exercise various degrees of control over the automated implementation process using auto-interactive tools and techniques. Optionally, user-designated partitioning, placement, and routing information can be specified as part of the design entry process (typically, right on the schematic). The implementation of highly structured designs can greatly benefit from the basic floorplanning techniques familiar to designers of large gate arrays.

For Xilinx FPGAs, the automatic tools are complemented by an interactive, graphics-based editor that allows users to view and manipulate a model of the logic and routing resources inside the FPGA device, providing the user with visibility into the implementation of the design.

Design Verification

Verification of FPGA/CPLD designs typically involves a combination of in-circuit testing, simulation, and static timing analysis. The user-programmable nature of these devices allows designs to be tested immediately in the target application. For Xilinx FPGAs and in-system-programmable CPLDs, download cables are provided that allow for the direct downloading of a bitstream from a PC or workstation to an FPGA or CPLD device on a target board. Demonstration/prototyping boards are also available. The implementation tools include back-annotation to provide post-layout timing of implemented designs to support timing simulation. A static timing analyzer can be used to examine a design's logic and timing to calculate the performance along signal paths, identify possible race conditions, and detect set-up and hold-time violations. Timing analyzers do not require the user to generate input stimulus patterns or test vectors.

Xilinx software is available both in bundled packages containing front end implementation tools and with integrated kits to enable plug and play with 3rd party EDA environments. New enhancements are constantly being developed, and update services are available to ensure timely access to the latest versions.

Xilinx Software on CD-ROM

Xilinx software and updates are now delivered on CD-ROM for the PC and workstations (Sun, HP700 and RS6000 Series). Here are some of the benefits:

- Faster Installation: No more wasted time, feeding floppy after floppy into the PC. No more waiting for workstation tapes to spin, looking for the proper data. Installing or updating Xilinx software is as easy as popping in one CD-ROM disk.
- Software Compatibility: New install utilities monitor the software configuration, ensure executable version compatibility, and update only the necessary files to keep the software up-to-date. Archiving old versions of XACT software is as easy as storing one CD-ROM disk.
- On-line documentation, tutorials, application notes, and product demonstrations.

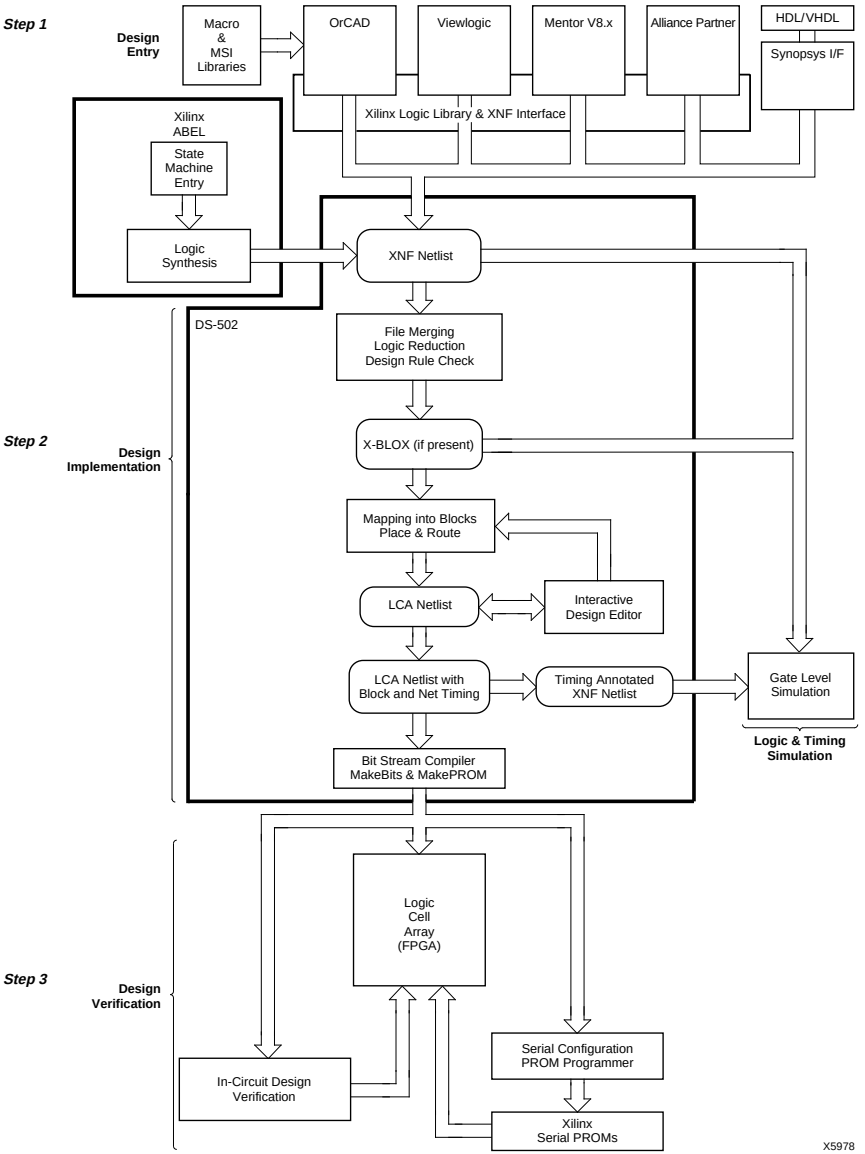

Figure 3: Detailed FPGA Design Flow

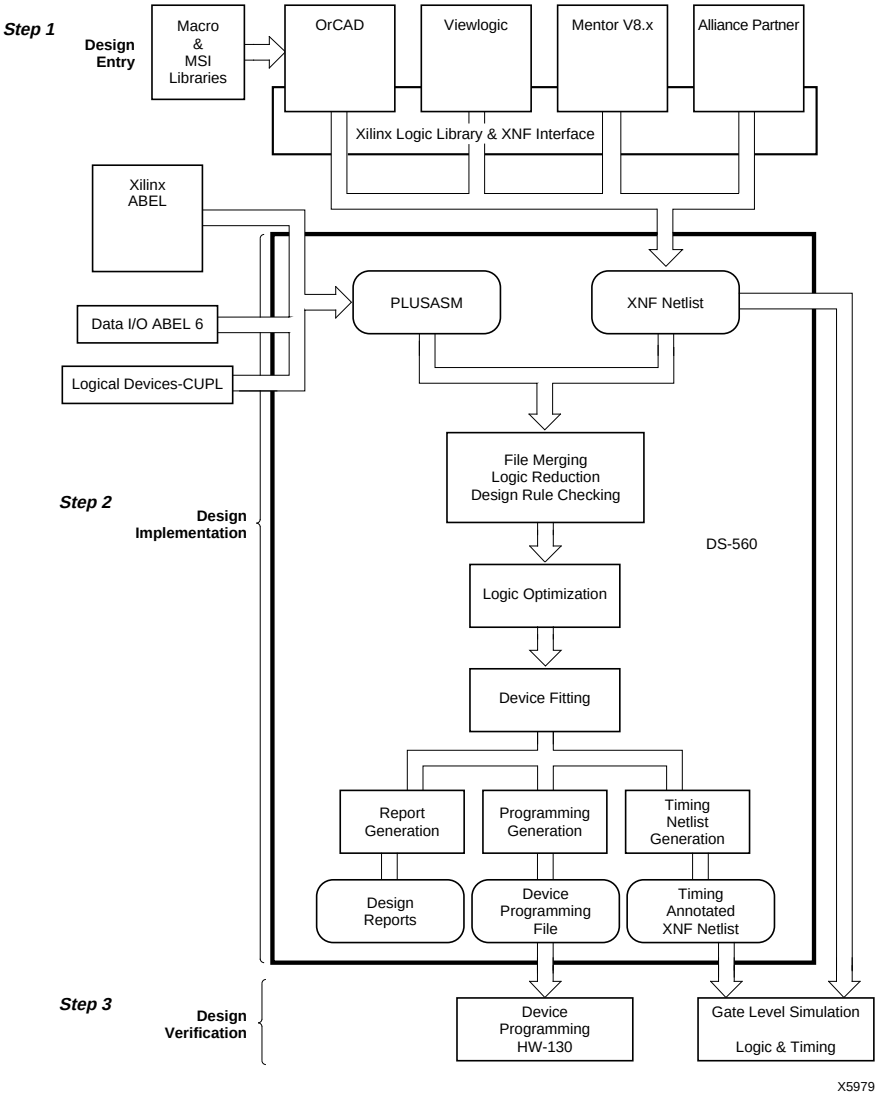

Figure 4: Detailed CPLD Design Flow

Support and Update Services

Software Updates

A major focus of Xilinx engineering is continual improvement of the Xact*step* Development System Software. This is accomplished by developing new features to improve your design productivity, and adding new technologies to give you access to the latest Xilinx products. If you are on maintenance, you will receive new revisions containing enhancements to the software products you have licensed from Xilinx.

Base Product Updates

The Xact*step* Base packages do not come with a standard one-year update contract. When Xilinx releases a new version of software, customers will be notified and may purchase the new version update at the listed price.

Online Documentation

Xilinx continually updates documentation to reflect changes to the Development System Software. As part of the update service, you receive new online documentation with each update.

Technical Support Hotline

The Technical Telephone Support Hotline provides you with toll-free telephone access to trained software technical support engineers. (See Chapter 13.) Expertise provided includes most major third-party interfaces including Viewlogic, OrCAD, Mentor Graphics, Xilinx ABEL, Synopsys, and Cadence. Additionally, Xilinx core expertise is available for both FPGA and CPLD product lines covering place and route, X-BLOX, XACT Performance, XDelay, configuration and component issues.

This support service for problem resolution assistance is available between 8:00 am and 5:00 pm Pacific Standard Time, Monday through Friday (except holidays).

For service outside USA, please contact your local representative.

Xilinx Technical Bulletin Board

The Xilinx Technical Bulletin Board allows electronic exchange of information with technical support engineers. With this service you can upload your design data making it available to support engineers during problem resolution.

You can use the Technical Bulletin Board download capability to obtain various software utilities, the latest released revisions of speed and package files, detailed solutions for commonly encountered problems, and marketing updates. The Technical Bulletin Board number is 1-408-559-9327 and it is available 24 hours a day, 7 days a week.

Customer Support FAX

The technical support engineers can be reached directly via facsimile by using the “Technical Support only” fax line. This service is available to supply information to the support engineers to resolve a specific inquiry. Additionally, this service may be used in lieu of, or together with, the Technical Support Hotline. The fax number is 1-408-879-4442.

Internet Electronic Mail Support

Another alternative for technical support is via the Internet E-Mail address, hotline@xilinx.com. As with the other previously described methods, electronic mail allows full access to Xilinx Technical Support engineers.

Software Series Overview

The Xilinx Xact*step* Software Series provides powerful, easy to use design tools for FPGA and CPLD devices. Three different series with several choices of configurations lets designers choose the exact system for their needs.

- Foundation Series — Complete shrink-wrapped design solutions
- Alliance Series — Powerful systems that integrate into existing EDA environments
- SLI Series — Value added options that enable system level integration.

The Foundation Series provides entry-level designers with a complete solution in a shrink-wrapped, easy-to-use environment. This fully integrated set of tools, which is perfect for users that are new to PLD design, includes design entry simulation, VHDL synthesis, and design implementation tools.

The Xilinx Alliance Series is for designers who want to integrate into their existing EDA tool environment. It supports the complete spectrum of design techniques with interfaces to over 45 EDA vendors and 80 different design tools.

Optional Viewlogic front-end products are part of the Alliance Series. This is ideal for users who want a complete system that is extensible to board and system level design.

The Foundation and Alliance Series support the industry's broadest array of PLD solutions including the XC2000, XC3000A, XC3100A, XC4000/E, XC5000, XC7300 and XC9500 families. This gives designers technology independence by letting them choose target devices late in the design cycle.

Both series include the powerful XACT*step* implementation system containing the popular Design Manager, Flow Engine, PROM File Formatter, Floorplanner and Hardware Debugger.

All products in the Xilinx XACT*step* Series use standards-based design techniques that maximize design portability and reuse. EDA design tools that support EDIF, ABEL, Verilog, VHDL and LPM formats interface easily into the Xilinx design environment.

PLD designs can use integrated ABEL design and synthesis or interfaces to any of the leading PLD design tools environments. Schematic designs can use the integrated capture tool in the Foundation Series or choose interfaces to any leading EDA environment. HDL designs enjoy standards-based design using integrated VHDL synthesis in the Foundation Series or interfaces to any leading VHDL or Verilog synthesis tool.

This flexibility protects the user's investment in design tools and training and makes it easy to re-use designs even when EDA systems change.

Foundation Series

The Foundation Series provides everything required to design a programmable logic device in an easy-to-use, fully-integrated environment. This fully integrated solution makes PLD design easy by providing push button design flows, on-line training and the XACT*step* windows-based graphical user interface.

This series features broad support for standards based HDL design. All configurations interface with the popular ABEL language and fitters optimized for each target architecture. VHDL configurations include integrated VHDL synthesis with tutorials and wizards to turn new users into experts quickly and easily.

Easy to Learn and Use

The Foundation Series is a fully integrated tool set allowing users to access design entry, implementation and verification tools from a single graphical user interface. Every step in the design process is accomplished using graphical tool bars, icons and pop-up menus supported by interactive tutorials and comprehensive on-line help.

VHDL Synthesis

VHDL configurations of the Foundation Series contain integrated VHDL synthesis and wizards with the following features.

- On-line tutorial teaches the art of VHDL design.
- Intelligent HDL editor with color coding, syntax checking and single click error navigation makes it easy to read and debug VHDL designs.
- HDL Language Assistant provides libraries of common functions with optimized VHDL code.
- FPGA specific synthesis tools produce high-density, high-performance results.

ABEL-HDL Synthesis

ABEL™ configurations of the Foundation Series contain integrated synthesis and wizards with the following features.

- Intelligent HDL editor with color coding, syntax checking and single click error navigation makes it easy to read and debug ABEL designs.
- HDL Language Assistant provides libraries of common functions with optimized ABEL code.
- FPGA/CPLD specific synthesis tools produce high-density, high-performance results.

Alliance Series

The Alliance Series is for users who want powerful design tools that integrate into their existing EDA environment. With this series, designers can choose from a wide range of design techniques including schematic capture, module-based design and HDL from over 45 EDA vendors. With standards based design interfaces including EDIF, ABEL, Verilog and VHDL, this series provides maximum flexibility, portability and design reuse.

Advanced integration with Cadence, Mentor, OrCAD, Synopsys and Viewlogic provide tightly-coupled environments that make it easy to move through the design process.

Other EDA vendors are supported through the Xilinx Alliance Program, insuring high quality tools and accurate results. Information on these vendors can be found on the Xilinx Alliance CD or through WebLINX on the world wide web at www.xilinx.com.

The Alliance Series includes the complete XACT*step* implementation tool set supporting the complete spectrum of design methodologies from fully-automatic to hand-crafted.

Viewlogic Standalone products are part of the Alliance Series and are for those users who want the integration of a complete solution with the power to access board and system level design tools. These products include Viewlogic Workview Office schematic capture, simulation and synthesis tools.

Configurations

The Xilinx Software Series are available in 3 configurations giving designers a cost effective way to match their tools to the gate densities they require.

CPLD configurations provide support for Xilinx's XC9500 and XC7300 CPLD families.

Base configurations provides push-button design flows and support designs up to 5,000 gates.

Standard configurations combine push-button flows with powerful auto-interactive tools. These tools give designers more influence and control over implementation while maintaining the benefits of design automation. Standard configurations support designs up to 20,000 gates.

Optional LogiCores give designers access to large fully verified functions that simplify design entry and provide dramatic savings in engineering resources. The initial LogiCore product set includes a complete PCI interface module.

Migration Paths

All tools in the Xilinx XACT*step* Series use standards-based design to protect the user's investment as design requirements change.

For example, designers can use Foundation products to learn ABEL or VHDL and produce code optimized for device resources. If future requirements force the use of different design tools, users can upgrade to the Xilinx Alliance Series and reuse their code while gaining access to powerful system-level tools.

The Foundation and Alliance Series use the same core implementation tools eliminating the need to re-learn the design process after an upgrade.

Unified libraries and standard design file formats allow schematic designers to enjoy the same migration capabilities.

Individual Products

Libraries and Interface – Contains schematic symbols or HDL libraries, simulation models with timing information, and translators to the XNF file format.

Core Implementation – Provides the software necessary to process an XNF file into a file which can be used to program a Xilinx FPGA or CPLD device. Includes tools for logic reduction, design rule checking, mapping, automatic placement and routing, bitstream generation and PROM file generation.

X-BLOX Module Generator & Optimizer – Allows design entry as block diagrams using a familiar schematic editor. Using built-in expert knowledge, X-BLOX software automatically optimizes your design to take full advantage of the unique features of the XC3000A, XC3100A, XC4000, and XC5000 FPGA families.

Xilinx ABEL – Supports CPLD and FPGA text-based design entry and netlist translation using ABEL high level description language. ABEL supports different design styles including Boolean equations, truth tables and encoded or symbolic state machines.

XChecker™ Cable – Supports downloading of bitstream and PROM files, and readback of configuration data and internal node values. This cable uses the serial port of IBM PCs & compatibles and supported workstations.

FPGA Demoboard – Provides demonstration or prototype capability for XC2000, XC3000, XC3000A, XC3100, XC3100A devices in 68-pin PLCC packages, and XC4000 family devices in 84-pin PLCC. This board is designed to offer flexibility for learning and prototyping.

Order Codes

Order codes for Development Systems products consist of a multiple-field part number. The first field indicates the product category. Additional fields indicate the third-party CAE vendor for interface tools, the package name or individual product number and the platform.

For example, the following order code indicates the category as Development System, the interface CAE vendor as Viewlogic, the package as Standard, the platform as IBM PC or compatible, and the media as CD-ROM.

DS-VL-STD-PC1-C

The following table shows valid product category, CAE vendor, package type, platform and media type codes.

Product Category	Code
Development System	DS
Support and Updates	SC
Base Update	BU
Re-instate Updates	SR
Product Upgrade	DX
Hardware	HW
Training Course	TC

Interface Vendor	Code
OrCAD	OR
Viewlogic	VL
Viewlogic *Stand-alone*	VLS
Mentor, version 8	MN8
Synopsys	SY
Cadence	CDN
Foundation	FND

Package Type	Code
Base System	BAS
Standard System	STD
Extended System	EXT
Advanced System	ADV

Platform	Code
IBM PC compatible	PC1
Sun-4	SN2
HP700	HP7
IBM RS6000	RS6

Media Type	Code
CD-ROM	C