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This section describes the following products:

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- CPLD Core Implementation – DS-560
- Schematic and Simulator Interfaces
- X-BLOX – DS-380
- Xilinx ABEL Design Entry – DS-371
- Xilinx ABEL Design Entry – DS-571
- Xilinx-Synopsys Interface (XSI) – DS401
- XChecker Cables
- Demonstration Boards

FPGA Core Implementation – DS-502

Core Implementation Includes:

- Software to process an XNF file for an XC2000, XC3000, XC3000A, XC3100, XC3100A, XC4000/E, XC5200 device into a BIT or PROM file that can be downloaded
- Automatic or interactive implementation
- XACT Performance™ system-level timing-driven mapping, placement, and routing
- Fast incremental design capability
- Advanced logic reduction algorithms
- Comprehensive design rule checker
- Powerful design editor
- Static timing analyzer
- Bitstream and PROM file generators
- Original hierarchical netlist-based back-annotation
- Software Support and Updates if on maintenance

Support and Updates Include:

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Hardware Requirements:

PC

- Fully compatible PC386/486
- MS-Windows 3.1 (minimum)
- MS-DOS version 5.0 (minimum)
- Minimum 50 Mbytes hard-disk space for Xilinx software
- One 3.5" High-Density floppy disk drive or ISO 9660 type CD-ROM drive
- VGA display
- One parallel and two serial ports
- 16 Mbytes of RAM for devices up to XC4008
- 32 Mbytes of RAM for XC3195, XC4010, and XC4013
- Mouse

Workstations

- 65 Mbytes hard-disk drive space for Xilinx software
- Other hardware requirements are same as for the Standard package

CPLD Core Implementation – DS-560

CPLD Core Implementation Includes:

- Fitter software to process XC7000 and XC9500 family designs
- Automatic optimization and mapping
- Automatic use of UIM resources
- Automatic arithmetic functions
- Complete optimization and collapsing
- High speed compilation

Support and Updates Include:

- Documentation Updates
- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX

XACT-CPLD provides a complete, user-friendly, multi-platform design environment for implementing behavioral or schematic designs. XACT-CPLD allows users to easily create, verify, and implement logic designs targeting the entire range of Xilinx XC7000 and XC9500 series devices.

Automatic Logic Mapping and Optimization

The automatic partitioning and mapping capabilities of XACT-CPLD allow the designer to concentrate on design functionality without concern for physical implementation; all device resources are automatically mapped and interconnected with no user intervention required. In addition, automatic logic optimization insures the highest performance and the most efficient usage of device resources. Because of these automatic features, the user does not need a detailed knowledge of the device architecture. However, XACT-CPLD also allows the designer to fully control the physical mapping of logic and I/O resources when necessary.

Required Hardware Environment

- Fully compatible PC 486/Pentium
- MS-Windows 3.1
- MS-DOS version 5.0 (minimum)
- Minimum 26 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel port for EZTag download cable
- One serial port for Windows compatible mouse
- 16 MB of RAM

Feature Summary

- Advanced XACT*step* v6.0 XC7000 implementation software with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing driven fitting.
- XC9500 implementation software with advanced pinlocking capability.
- EZTag download software supporting the programming of multiple Xilinx CPLDs anywhere in a JTAG chain.
- Includes XC9500 Synopsys, Viewlogic, and OrCAD interfaces.
- On-line tutorials and documentation
- Static timing report
- Schematic Design Entry — XACT-CPLD, coupled with the appropriate external interface, provides a schematic library that includes familiar TTL and PAL components for use with industry-standard schematic editors such as those available from OrCAD, ViewLogic, Mentor Graphics, and Cadence Design Systems.
- Simulation Support — XACT-CPLD supports various third-party simulators such as ViewLogic PROsim, OrCAD VST, Mentor QuickSim, Cadence Verilog, and Cadence RapidSim. Both functional and timing simulation are supported.
- Board-Level Simulation Support — XACT-CPLD device models are available from Logic Modeling Corporation for board-level simulation on a variety of platforms.
- High-Speed Compilation — Design iterations are easily performed and the results are quickly reported.
- Predictable Design Performance — The PAL-like architecture of the Xilinx CPLDs provides fixed predictable delays independent of physical placement, routing, or device utilization.
- Automatic Mapping and Logic Optimization — Device resources are automatically mapped for optimal efficiency and high performance. Users can focus on design functionality without concern for the physical implementation in the device.
- Complete Design Control — Users have the option to override the automatic features of XACT-CPLD and selectively control any or all device resources.
- Multiple Platform Support — XACT-CPLD runs on Sun, HP, and PC (DOS) platforms

Schematic and Simulator Interfaces

Interfaces and libraries for several popular schematic editors and timing simulators are available as individual products, for users that already own an editor and simulator. For designers looking for a design entry tool, Xilinx offers Xilinx-specific versions of Viewlogic's schematic editor, simulator, and ViewSynthesis VHDL synthesizer and VHDL simulator.

The following products are available for the platforms noted in parentheses:

DS-390 Viewlogic schematic editor with Xilinx libraries and interface (PC)

DS-290 Viewlogic simulator with Xilinx libraries and interface (PC)

DS-391 Libraries and interfaces that support Viewlogic's Workview Office Series, PRO Series, and Powerview design entry and simulation tools (PC, Sun, HP700)

DS-344 Libraries and interfaces for Mentor Graphics Design Architect schematic editor and QuickSim II simulator (HP700, Sun)

DS-35 Libraries and interfaces for OrCAD 386+ schematic editor and VST 386+ simulator (PC)

Features

- Complete set of primitive and macro libraries for all FPGA and CPLD products
- Full simulation models provides for accurate post-layout timing analysis
- Unified libraries allow easy migration between all Xilinx architectures, including CPLDs
- Converts schematic drawings to Xilinx Netlist Format (XNF) output
- Converts XNF files to format compatible with logic and timing simulators
- Supports unlimited levels of hierarchy
- Includes one year of support and updates
- All above products can be purchased with core implementation tools as a package, offering easier upgrading and reduced cost.

X-BLOX – DS-380

X-BLOX Includes:

- Parameter-based schematic and function-generation tool. Allows block-diagram design entry using generic function modules.
- Works with many Schematic Entry Interfaces (Viewlogic, Mentor, OrCAD, Cadence and other Alliance Partners)
- Expert system that automatically utilizes the advanced features of the XC5200 family, XC4000/E family and XC3000A and XC3100A families
- Schematic library with more than 30 frequently-used generic modules (adders, counters, decoders, registers, MUXes, etc.)
- Software Support and Updates for first year

Note:

- XC5200, XC4000/E and XC3000A, XC3100A families are supported. XC2000, XC3000, and XC3100 are not supported.
- Additional Requirements:
  Five Mbytes hard-disk space for program and design files

Xilinx ABEL Design Entry – DS-371

The Xilinx ABEL system gives designers the ability to enter Xilinx designs using the industry standard ABEL Hardware Description Language (ABEL-HDL). Designers can describe circuits with Boolean equations, state machines and truth tables. State machine and logic optimization software automatically generates efficient logic for Xilinx devices.

Many designs contain portions of logic that are best described in a text-based format; some designs can be completely described in this way. In the Xilinx ABEL system, Xilinx designs can be created with Boolean equations, state machines, and truth tables. The ABEL HDL makes designing quick and simple. Intelligent state machine and logic optimization software automatically creates efficient, fast state machines. The ABEL simulator allows functional simulation of ABEL-HDL designs.

CPLD designs may be entered entirely with ABEL-HDL. FPGA designs should be entered via a combination of XABEL and a schematic editor to take optimal advantage of the Xilinx architectures. The recommended design flow is to enter designs schematically with functional blocks that refer to logic described in ABEL-HDL. From inside the Xilinx ABEL environment, designers create and compile the logic in these functional blocks. The Xilinx XMake program then compiles the complete design to a bitstream that can be downloaded to a Xilinx device. XMake automatically calls the software that merges the various design files (schematics and ABEL-HDL), partitions, places and routes the design and creates the final bitstream. The design can then be verified with a simulator and a timing analyzer, as well as verified in-circuit.

One-Hot Encoding

For the flop-flop rich, fan-in limited Xilinx FPGA architecture, One-Hot Encoding (OHE) is the preferred technique for implementing high-performance state machines. OHE is also know as state-per-bit encoding, since it uses one flip-flop per state. OHE takes advantage of the abundance of flip-flops in Xilinx FPGAs to reduce the levels of logic required to implement a state machine. This implementation significantly increases performance over fully encoded state machines, the traditional technique used in PLDs. Xilinx ABEL automatically uses OHE on symbolic state machines created in ABEL-HDL for FPGAs.

Features

- State machine and Boolean equation entry via DATA I/O's ABEL language
- ABEL Functional Simulator
- Xilinx-specific ABEL environment, compiler, and optimizer for FPGAs
- Automatic symbolic One-Hot encoding or fully encoded state-machine implementation
- Ability to integrate ABEL designs with other schematic elements
- Software Support and Updates for the first year

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Software Updates if on maintenance
- Online Documentation
- World Wide Web Access
- Technical Newsletter
- Extensive Application Notes

Additional Requirements

- 10 Mbytes hard-disk space for program and design files

Xilinx ABEL Design Entry – DS-571

XABEL-CPLD is the new Xilinx development system designed for PAL and CPLD users. With this completely self contained system, customers can quickly and easily integrate their logic into Xilinx CPLDs using the industry-standard ABEL hardware description language.

XABEL-CPLD Includes

- Familiar Data I/O ABEL, Windows based environment for design entry, simulation and fitting
- Hierarchical design entry and JEDEC file conversion
- Functional simulation with graphical waveform viewer
- Static timing report
- Advanced XACT*step* v6.0 XC7000 and XC9500 fitters with fully automatic device selection, multiple pass optimization, partitioning and mapping, and timing driven fitting
- EZTag download software and cable
- Online tutorial and online help reduces learning curve

Support and Updates Include

- Hotline Telephone Support
- Access to Xilinx Technical Bulletin Board
- Apps FAX and E-Mail
- Online tutorial and help

Required Hardware Environment

- Fully compatible PC 486/Pentium
- MS-Windows 3.1
- MS-DOS version 5.0 (minimum)
- Minimum 45 MB hard disk space
- ISO 9660 type CD ROM drive
- VGA display
- One parallel port for EZTag download cable
- One serial port for Windows compatible mouse
- 16 MB of RAM

Feature Summary

- Familiar Data I/O ABEL, Windows based environment for design entry, simulation and fitting provides a simple, single push button design flow
- Industry-standard ABEL-HDL supports state machines, high level logic descriptions, truth tables and equation entry
- Hierarchical design entry and JEDEC file conversion enables reuse of existing PAL codes, simplifying PAL integration into Xilinx CPLDs
- Functional simulation with graphical waveform viewer and static timing reports facilitate rapid design verification
- Advanced XACT*step* v6.0 fitter's architecture specific knowledge let's the user focus on design functionality
- Online tutorial leads users through the entire design process in minutes
- Extensive online help system places all documentation just a mouse-click away

Xilinx-Synopsys Interface (XSI) – DS-401

This interface and library product supports VHDL and Verilog/HDL synthesis using either the Synopsys Design Compiler or FPGA Compiler products

Features

- Synthesis libraries for:
  XC3000/XC3100, XC4000/E and XC5000 family FPGAs
  XC7000 and XC9500 family CPLDs
- X-BLOX synthetic library
- Translator from Synopsys to Xilinx XNF
- Ability to integrate models with other design
- Available for Sun-4, and HP700, platforms

DS-401 (XSI) lets the Synopsys FPGA Compiler and Design Compiler target the XC3000, XC3100, XC4000/E, and XC5000 FPGA families and XC7500 and XC9500 CPLD families. XSI consists of synthesis libraries, a translator from Synopsys to XNF, and a library of X-BLOX functions implemented using Synopsys DesignWare.

Language Support

Either VHDL or Verilog/HDL entry is supported through the use of the appropriate Synopsys language compiler.

Compiler Support

FPGA Compiler is highly recommended for XC4000/E and XC5200 designs due to its specific XC4000/E algorithms. Design Compiler is sufficient for XC3000 and XC3100 designs.

Simulation Support

Behavioral simulation before compilation using Synopsys VHDL System Simulator (VSS) is supported. In the future, gate-level simulation of designs after layout will be supported as well.

Support and Updates

- Software updates for one year
- Documentation updates
- Hotline Telephone Support for the first six months
- Access to Xilinx bulletin board
- Apps FAX

Notes

- This product does not support the Synopsys Test Compiler
- A Synopsys Standard package is available which combines XSI (DS-401) and FPGA core implementation tools (DS-502) in one product. Packages offer reduced prices over modules purchased separately.
- The X-BLOX library allows Synopsys software to automatically insert certain X-BLOX functions (adders, subtracters, and comparators) where possible for maximum performance. In-warranty XSI customer receive X-BLOX as an automatic upgrade.

XChecker Cables

XChecker Cable Package Includes:

- XChecker cable
- Flying wire jumper
- Flat header jumper
- XChecker diagnostics fixture

XChecker Cable Features:

- Provides bitstream and PROM-file download capability to FPGAs
- Provides readback capability
- Works with serial ports on IBM 386/486/Pentium and compatibles
- Compatible with XACT XChecker diagnostics software and the XACT Probe utility
- Flying-wire and flat-header jumpers provide easy access during prototyping

Demonstration Board – FPGA

FPGA Demo Board Includes:

- Three 7-segment displays (one for XC3000, XC3000A and two for XC4000/E)
- Two, octal DIP switches for inputs to LCA devices (one for XC3000 and one for XC4000/E)
- Test pins for access to all LCA I/O
- XC4003A in 84-pin PLCC package
- XC3020A in 68-pin PLCC package
- Two 8-segment bar displays (one for XC3000A and one for XC4000/E)
- Program, Reset, and Spare momentary contact switches

FPGA Demo Board Features

- Operates from a 5-V power supply
- Compatible with XChecker and parallel download cables
- Supports Master-Serial configuration mode for interface to Xilinx serial PROMs
- Two sockets, one can be used for any XC2000, XC3000 or XC3100 device in a 68-pin PLCC package, the other can be used for any XC4000/E device in an 84 pin PLCC package
- Provides sockets for up to three daisy-chained serial PROMs
- Includes 3 inch by 3 inch prototyping area
- Daisy-chain configuration capability (XC4000/E must be first in the chain)