XCELL

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THE QUARTERLY JOURNAL FOR XILINX PROGRAMMABLE LOGIC USERS

XILINX®
The Programmable Logic Company℠

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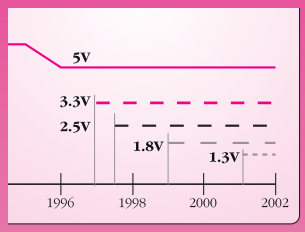

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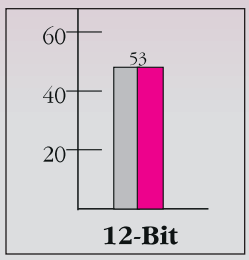

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Getting to the Core

By BRADLY FAWCETT ◆ Editor

Continuing improvements to both fabrication processes and device architectures have led to dramatic increases in FPGA capacity and performance, as evidenced by the new XC4000EX family devices. Taking advantage of these increasing capabilities can pose formidable challenges to the user — challenges that cannot always be met by traditional gate-level design techniques, or even HDLs and synthesis-based design. For many users, reusable intellectual property in the form of design "cores" are becoming a key tool in meeting the twin challenges of increasing design complexity and shorter development cycles.

Simply put, cores are complex, pre-designed and reusable functional blocks, typically hundreds to thousands of gates in size, that can be included as part of a larger FPGA design. Cores can be developed internally (for example, re-used portions of previous-generation designs) or purchased as intellectual property from the FPGA vendor or a third-party provider.

The main benefit of cores is the decreased development time and effort associated with using a pre-designed, proven function. Designers can focus their efforts on the proprietary portions of their designs, rather than "re-inventing" a standard function.

Xilinx is committed to the development of a broad selection of cores optimized for use in Xilinx devices. We are fulfilling that commitment in two ways — through the internal development of our own core products, called LogiCORE™ modules, and by partnering with leading third-party core developers through the Xilinx AllianceCORE™ program. The goal is to allow Xilinx FPGA users to act as system integrators, easily combining proven functional blocks with the proprietary logic of the particular application.

To date, the Xilinx LogiCORE PCI Interface has been the most-successful core-based product in the programmable logic industry. With its combination of logic complexity and strict performance requirements, the PCI interface also is one of the most-challenging designs ever to be placed in an FPGA core. We are now using the considerable experience that we gained in developing, selling, and servicing the PCI interface to improve future LogiCORE products and shape our relationships with third-party core developers.

Two of the most-important lessons that we learned are (1) cores should be fully-optimized for the target FPGA architecture, and (2) cores must be delivered to the user as part of a complete product solution.

Some third-party ASIC core vendors are seeking to expand their potential market by re-targeting their "generic" HDL code to various FPGAs. However, with such an HDL-based core, there is little guarantee that the physical implementation will be optimal for the target FPGA architecture. The utilization levels and performance will vary dependent on the efficiency of the synthesis tools and how the core is combined with adjacent logic. The time and effort spent in overcoming these problems can quickly eliminate the time-to-market advantage that initially motivated the use of a core.

In contrast, cores optimized for the target FPGA can use all the available features of the architecture, such as dedicated arithmetic carry logic, internal three-state buffers, and on-chip memory, to achieve optimal logic utilization. Placement and timing constraints, used in conjunction with re-entrant, timing-driven 'place and route' tools, result in predictable and optimized performance levels.

However, there is much more to delivering a core-based solution than just supplying the

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GUEST EDITORIAL

1997 *The Year That Defines the Future*

by SANDEEP VIJ ◆ Vice-President, Marketing

In 1985, Xilinx introduced the world's first FPGA device, creating an important new product category in the semiconductor industry. Since then, a steady stream of new, innovative component and development system products has allowed Xilinx to grow into the industry's leading supplier of programmable logic.

In 1997, the pace of innovation will increase. By aggressively applying architectural improvements and the latest process technologies, Xilinx will be setting new standards for FPGA capacity, performance, and cost-effectiveness. All 10 members of the new XC4000XL family will be available by mid-year. Based on 0.35 µ technology, this family provides usable logic gate densities ranging from 5,000 to 85,000 gates (about 500 to 7,500 "logic cells," where a logic cell consists of a 4-input look-up table and a register). These are true "logic gates," not the "combined logic and memory gates" metrics used by others to inflate their gate counts.

By mid-year, we expect to be sampling the first FPGA based on a 0.25 µ process, and we will be working with 0.18 µ technology by year-end. Our next-generation architecture also should be available by year-end, and is projected to reach densities of over 30,000 logic cells (about 400,000 logic gates) in 1998. Of course, correspondingly faster speed grades also will be introduced, reaching true 100 MHz chip-to-chip performance later this year. Our next-generation of place and route tools will support these new offerings.

> *"Xilinx will be setting new standards for FPGA capacity, performance, and cost-effectiveness."*

The XC5200 series FPGAs also will be migrated to a 0.35 µ process this year. Die sizes for these cost-optimized devices will shrink to the point where they are "pad limited"; that is, the die size is constrained by the number of I/O pads required, not the logic gate density. When this occurs, traditional gate arrays will have no die size advantage and, therefore, no cost advantage over FPGAs. Lower FPGA costs will open new markets to programmable logic devices in applications such as Internet applicances, PC add-in cards, consumer electronics, automotive electronics and large household appliances.

The Xilinx CPLD product lines will benefit equally from aggressive process migration this year. The industry has adopted FLASH memory technology as the mainstream floating-gate technology, facilitating the migration of the FLASH-based XC9500 family down the process curve. Xilinx CPLDs will continue to be the lowest-priced in the industry, while offering the best routability and pin-locking capabilities of any available CPLD.

Optimizing the Process

Advanced process technology is critical to providing leading-edge performance, density and cost-effectiveness. Xilinx is firmly committed to always having and using the most advanced IC fabrication processes available. One of the major advantages of being a "fabless" semiconductor company is the ability to form manufacturing partnerships with the process leaders at any point in time. An in-house staff of process engineers allows Xilinx to work with our fabrication partners to quickly bring new processes on-line.

Continued on the next page

XILINX®

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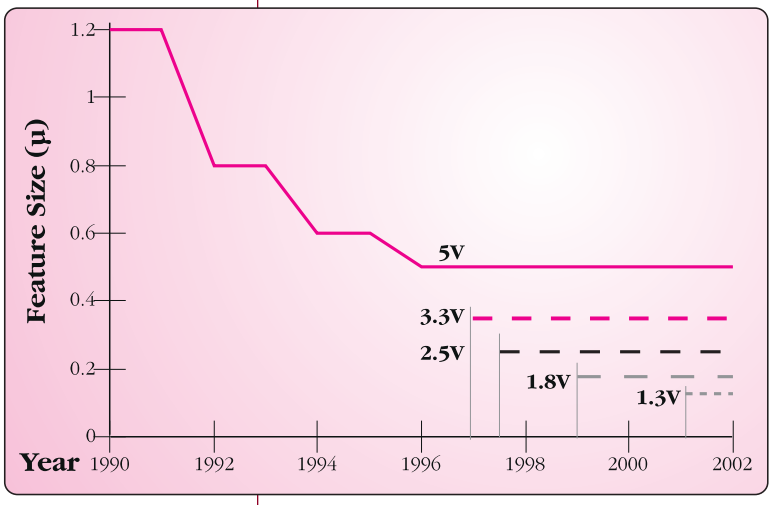
The leading semiconductor foundries are eager to use Xilinx FPGAs to drive their process development. The regularity and testability of our FPGA architectures facilitates defect analysis and fault testing. With their large transistor counts (the XC4062XL device has about twice as many transistors as the Intel Pentium Pro processor), FPGAs are a very good "test vehicle" for the most-advanced fabrication lines.

The Voltage Staircase

In order to reap the benefits of advancing process technology — increased performance, increased density, lower power consumption and lower price — users must be willing to migrate their designs down the "voltage staircase." The graph shows how CMOS process technology has improved from 1.2 µ design rules in 1990 to today's 0.5 µ processes, while maintaining 5 volt logic levels. As geometries shrink below 0.5 µ, the smallest transistors cannot withstand 5 volts without damage. This leads to the voltage levels shown in the graph, with each successive process generation using a smaller supply voltage.



Rapidly shrinking device geometries will require the use of smaller supply voltages.

Xilinx is taking an active lead in working with our users to plan an orderly migration from one voltage standard to the next. A major part of our migration strategy is to maintain I/O compatibility across multiple generations. For example, all of the 3.3 V products in the XC5200L and XC4000XL families have I/O structures that are fully 5 V compatible — accepting full 5 V signals on all I/Os and being able to drive TTL-like levels into any 5 V devices. Even our future 0.25 µ, 2.5 V components will employ split I/O and core power supplies to maintain I/O compatibility with either 5 V or 3.3 V devices.

This is not meant to imply that Xilinx will discontinue production of 5 V devices anytime soon. Although we encourage our users to migrate their designs to the lower voltage standards as these new products become available, we recognize that designs based on the 5 V standard will continue in production for many years to come, and we remain firmly committed to supporting those designs.

Complete Solutions

Users require complete solutions that meet their logic requirements, not just the biggest or fastest device. We realize that programmable logic solutions consist of a combination of many elements, including device architecture, device packaging, EDA interface software, synthesis software, place and route implementation software, pre-designed cores, sales support, and technical support. We intend to continue to lead the market in all these areas.

In summary, Xilinx will be releasing a formidable array of new products in the coming year. These will include:

- The industry's highest-density FPGAs
- The fastest FPGAs
- The first full family of FPGAs available for 3.3 V systems
- The first FPGAs using a 0.25 µ process
- The next major release of the Xilinx development software
- A broad offering of pre-designed cores
- The introduction of the next-generation FPGA architecture.

This will set the stage for the next five years, during which FPGA speeds are expected to increase five-fold, and FPGA densities will increase to 150,000 logic cells (2 million logic gates). ◆

Continued from page 2

core's design netlist. Potential users should also consider three other main factors that lead to a "complete" solution: silicon, software, and service.

Core-based designs are most appropriate for high-density FPGAs with a rich feature set. FPGA device features such as flexible clocking, numerous and flexible output enables, on-chip memory capability, and on-chip three-state bussing are critical to the implementation of system-level solutions. Broad product families, such as the Xilinx XC4000 series, allow the choice of the most-appropriate device for a given application.

The FPGA development environment must support the appropriate design entry, synthesis, implementation, and verification tools needed for the particular core design. The methodology and tools used to pre-define the implementation of critical paths, such as placement and timing constraint files or guide designs, should be well-understood. Where appropriate, simulation models and test benches should be part of the package supplied to the user, thereby facilitating the verification of the completed design. System software and prototyping equipment also may be required to ease the rapid integration of a core into a complete design.

To ensure the productivity gains that motivated the use of a core, extensive documentation and application support must be available. Of course, the degree of support required for core integration is often proportional to the complexity and flexibility of the core.

Recognizing these needs, the LogiCORE and AllianceCORE programs are emphasizing quality over quantity. For example, we are taking an active role in working with our AllianceCORE partners in the process of "productizing" their cores. A core must meet a minimum set of criteria before it can receive the AllianceCORE label, in terms of "sensibility," format, and completeness.

First, the core must "make sense" — it must provide value over an ASIC or standard product version of the same function, and be cost-effective when implemented in a Xilinx device.

We are not interested in promoting generic, synthesizable functions as AllianceCORE products. The core must be optimized for the target Xilinx FPGA architecture and be delivered as a parametizable "black box" that allows needed customization in critical areas. Timing-critical cores designed to adhere to an industry standard (such as PCI and USB bus interfaces) must be supplied with the appropriate constraints files in order to guarantee functionality and compliance.

The core must be packaged as part of a complete product, including adequate documentation, the availability of technical support, and, where appropriate, additional elements such as test benches, simulation models, and prototyping equipment.

Xilinx recently announced the availability of the first AllianceCORE products, USB modules from CAE/Inventra, and PCMCIA modules from Mobile Media Research *(see page 17)*. It is notable that their offerings include important system integration tools such as simulation models and prototyping boards. The chart on page 17 lists the partners that are currently developing products under the AllianceCORE program; expect future additions and deletions to this list as we discover which providers can meet our stringent quality criteria.

> *"The intention is to provide our users with complete solutions that preserve the value of using Xilinx programmable logic devices, as opposed to just filling pages in a catalog of products by promoting the use of generic cores developed for other technologies."*

Of course, this emphasis on complete, optimized solutions and our high level of involvement will limit the number of partners that we can work with at a given time and, subsequently, the number of available AllianceCORE products. Again, the intention is to provide our users with complete solutions that preserve the value of using Xilinx programmable logic devices, as opposed to just filling pages in a catalog of products by promoting the use of generic cores developed for other technologies. ◆

New Look, More Content for WebLINX

www.xilinx.com

Visitors to WebLINX,™ the Xilinx home page on the World Wide Web, will have noticed its new look and feel. Designed to provide users with quick, easy and intuitive access to the desired information, the home page features a "virtual desktop," complete with labeled icons for direct links to the site's various sections. Fewer steps are required to get to information.

WebLINX holds a wealth of Xilinx information, but *Smart*Search™, our industry-wide search engine, goes a step further. The definitive resource for all Programmable Logic information on the web, *Smart*Search indexes and connects you to more than 50 PLD-rich web sites. *Smart*Search Agents will watch the Web for you and inform you via e-mail when new or updated information is added to any of the sites served by *Smart*Search.

New information is constantly being added to WebLINX. Technical information on the site now includes:

- More than 60 application notes organized by system type (e.g., PCI, DSP, and PCMCIA), function (e.g., memory functions, arithmetic functions, and busses), component product family and application.
- Complete and detailed datasheets on all Xilinx products.
- Hundreds of records in our technical answers database
- Xilinx product change notices and customer updates
- Access to back issues of *XCell*
- Software updates and patches
- Links to technical Xilinx presentations via Marshall Electronics NetSeminar™ archives.

So visit WebLINX and stay abreast of the latest developments from Xilinx, the industry's leading supplier of programmable logic. ◆

Xilinx CPLDs Satisfy High-Speed Processing Needs

TRANSTECH

Transtech Parallel Systems Ltd. (High Wycombe, United Kingdom) designs and manufacturers a wide range of embedded multi-processing products for OEM, end-user and scientific research applications. Specializing in meeting the needs of demanding high-performance, high-bandwidth applications, Transtech's products include every state-of-the-art microprocessor available today.

For example, three new board-level products are based on the 200 MHz PowerPC 603eV and 604eV processors: two TSP family VMEbus boards, and the TTM610 board featuring the popular TRAM format. The TTM610 TRAM module combines the PowerPC processor with a T805 transputer and up to 32 Mbytes of high-speed Synchronous DRAM (SDRAM), and is tailored for scalable, high-performance multi-processor solutions. Shared SDRAM memory is used for inter-processor communication

To take full advantage of these high-performance processors and memories, equally high-performance interface logic was required. This need, coupled with fast time-to-market requirements, led Transtech engineers to the Xilinx XC7300 and XC9500 CPLD families.

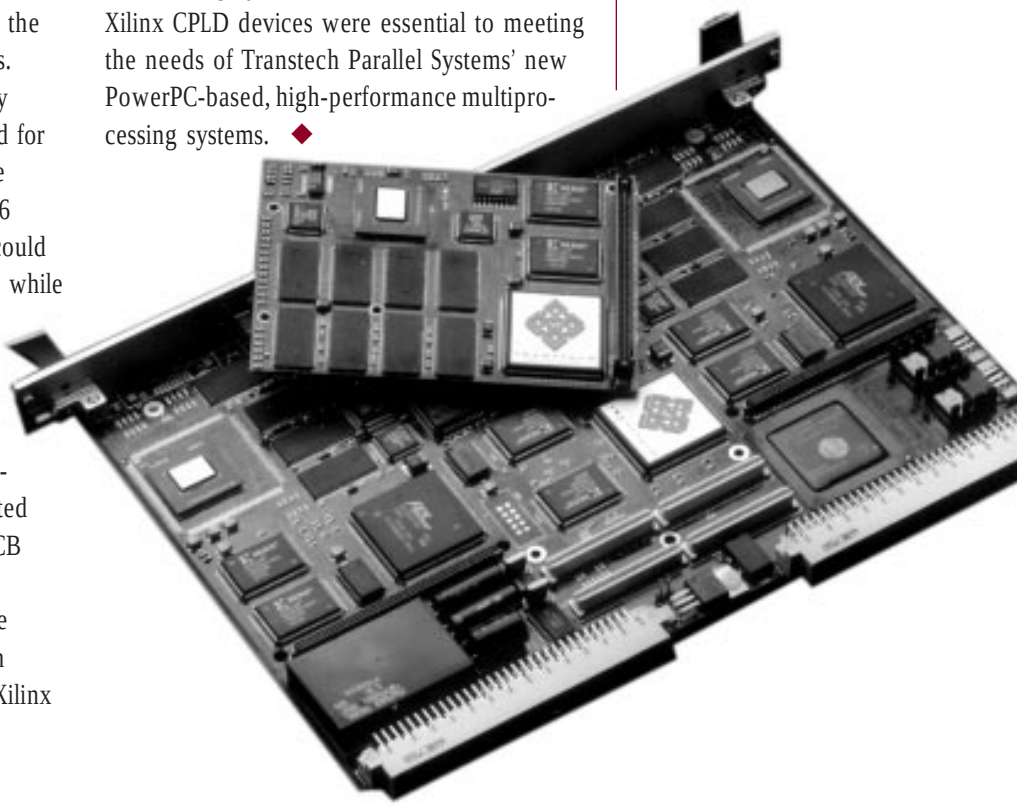
To support the fastest possible memory cycles, two XC7336-5 CPLDs were selected for implementing high-speed memory decode circuits on the TTM610 board. The XC7336 device was the only available CPLD that could perform the necessary decoding functions while maintaining a pin-to-pin delay of just 5 ns.

Two 108-macrocell XC95108-10 CPLD devices hold the more complex, high-speed state machine functions within the processor/memory interfaces. With an aggressive development schedule that dictated the parallel design of the logic and the PCB layout, the pin-locking capabilities of the XC9500 architecture proved crucial. In the words of Transtech design engineer Hugh Tarver, "The increased routability of the Xilinx XC95108 CPLD enabled a number of logic design iterations to be completed without the risk of the XC95108 changing its pinout assignment. This enabled us to complete our transputer board design quickly and without PCB modification."

A further attraction of the XC95108 CPLD was its in-system-programming capabilities. High-density packaging was required for the densely-populated TTM601 and TSP boards. In-system-programming eliminated the extra handling of the 100-pin PQFP packages that would have been required if an external programmer were used.

Multiple XC7336 and XC95108 CPLDs implement similar high-speed processor-to-memory and processor-to-processor interfaces on the TSP family VME boards, which feature up to four PowerPC processors per board. All the CPLD designs were developed using the Xilinx XABEL-CPLD™ software package on a PC platform.

High-speed systems need high-speed logic. The combination of the high performance and flexible, highly-routable architectures of the Xilinx CPLD devices were essential to meeting the needs of Transtech Parallel Systems' new PowerPC-based, high-performance multiprocessing systems. ◆



New Product Literature

Learn about the newest Xilinx products and services through our extensive library of product literature. The most recent pieces are listed below. To order or to obtain a complete list of all available literature, please contact your local Xilinx sales representative. ◆

TITLE	DESCRIPTION	NUMBER
Corporate		
AppLINX CD	Technical Data	#106425-03
Xilinx Educational Services & Course Brochure		#0010134-06
CPLD		
ISP Applications Guide	Technical Date	#0010290-02
HardWire		
HardWire Data Book	Technical Data	#0010164-03

UPCOMING EVENTS

Look for Xilinx technical papers and/or product exhibits at these upcoming industry forums. For further information about any of these conferences, please contact Kathleen Pizzo (Tel: 408-879-5377 FAX: 408-879-4676). ◆

11th International Parallel Processing Symposium (IPPS)
(Reconfigurable Architectures Workshop)
Apr. 1-5
Geneva, Switzerland

PCI Plus '97
April 13-18
Santa Clara, California

5th Annual IEEE Symposium on Custom Computing Machines (FCCM)
Apr. 16-18
Napa, California

DSP World
Mar. 25-26
Washington, DC

The Advanced PLD & FPGA Conference
May 13-14
London, UK

The Advanced PLD & FPGA Conference
May 20
Stockholm, Sweden

Design Automation Conference
June 9-13
Anaheim, California

FINANCIAL RESULTS

Quarterly Revenues Up 4%

Xilinx Inc. stock is traded on the NASDAQ exchange under symbol XLNX.

Xilinx sales revenues for the December-ending quarter increased 4% sequentially to $135.6 million, but were down 6% compared to the same quarter one year ago.

International revenues grew to comprise 38% of total sales. Both Japan and the Asia-Pacific region posted sales revenue increases of more than 15% compared to the previous quarter.

From a product viewpoint, revenues from the XC5200 FPGA family increased 45% to comprise 8% of total revenue. The new XC9500 in-system-programmable CPLD family contributed its first $1 million in revenues. Development system revenues increased 13% sequentially, and, for the second quarter in a row, the number of installed development system seats increased by nearly 1,400 units. ◆

XACT*step* M1 Course Available

A new training course using XACT*step*™ M1, the new release of the Xilinx development system, is now available at the regional level and at Xilinx headquarters in San Jose, Calif. M1 integrates the best of the Xilinx and Neocad tools into a new tool set *(see page 14)*. The currently released M1.1, a version that is workstation-based and emphasizes the XC4000EX FPGA family, makes the course most appropriate for designers using XC4000EX devices. General availability of the M1-based course will coincide with the upcoming M1 software release; check the next issue of *XCell* for updates on M1 training courses.

VHDL Courses

VHDL workshops and seminars continue to be in great demand. In North America, two-day workshops, sponsored by distributors Marshall, Hamilton-Hallmark, and Insight use Foundation™ tools and Xilinx devices for lab exercises. A Xilinx-sponsored one-day seminar for new VHDL users stresses the basics of the language. Contact your local Xilinx representative or distributor to ask about VHDL workshops and seminars in your area.

The entire training course schedule, including schematic- and synthesis-based courses and VHDL seminars, is available on WebLINX (www.xilinx.com). ◆

Xilinx 1997 Seminar Series

Coming Soon to a Location Near You

Xilinx technical seminars provide an easy way to learn about the latest programmable logic technologies to carry your designs through the '90s and beyond. Sessions are planned for May and June in more than 40 cities worldwide. Presented by members of the Xilinx technical support staff, the program covers solutions for all phases of the design cycle, including:

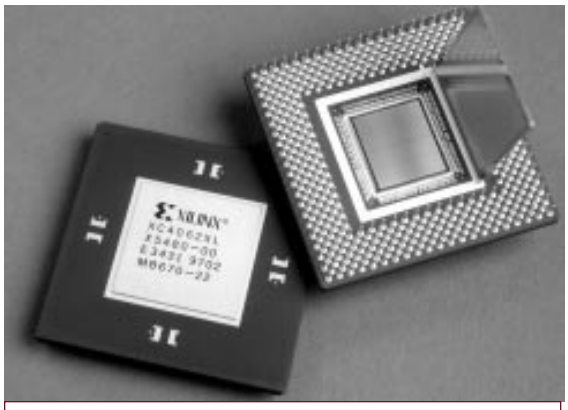
- An evaluation of logic alternatives
- Estimating design needs
- Design implementation and optimization techniques
- Getting the most out of Xilinx programmable logic devices

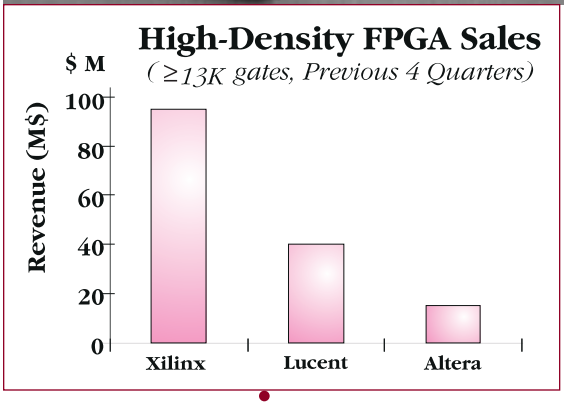
Several new Xilinx products will be highlighted, including the XC4000EX FPGA family, the XC9500 CPLD family and LogiCore™ drop-in modules. Each segment of the program will be supported by actual applications examples. In addition, hands-on demonstrations will enable you to operate the newest versions of our Foundation™ and Alliance™ series development tools.

Watch For Your Personal Invitation!

Invitiations for the 1997 Xilinx seminar series will be mailed directly to everyone on the *XCell* mailing list. You can respond by registering to attend a seminar via WebLINX (www.xilinx.com), phone, fax, e-mail or reply card. If your invitation does not arrive or you would like information, contact your sales representative or visit WebLINX. ◆

XC4062XL Debuts: *Xilinx Extends High-Density FPGA Leadership*





In January, Xilinx began sampling the XC4062XL FPGA device, currently the world's highest-capacity FPGA. Xilinx has shipped more than $90 million worth of high-density FPGAs over the past 12 months, more than all competitors combined.

The XC4062XL device, the largest available member of the XC4000XL family, is manufactured on an advanced 0.35 µ process and operates at 3.3 volts. It contains 2,304 CLBs (5,472 logic cells).

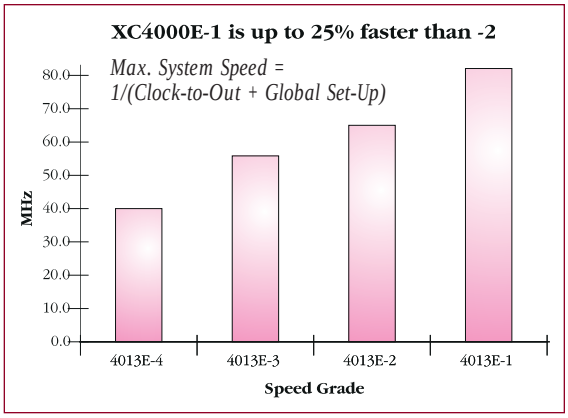
Logic cells are fast becoming the industry-standard metric for comparing densities of SRAM-based FPGAs. A logic cell is defined as the combination of a 4-input look-up table (LUT) and a dedicated register that reside in the same block, such that the output of the LUT can be the data input to the register.

The majority of FPGAs in use today are SRAM-based FPGAs whose logic blocks are based on a combination of memory look-up tables (LUTs) and dedicated registers. Thus, logic cells are a more direct and objective capacity metric than gate counts. Each XC4000 CLB, with two 4-input LUTs, one 3-input LUT, and two registers, is equivalent to 2.375 logic cells.

The XC4062XL is available in 560-pin ball grid array (BGA), 475-pin pin grid array (PGA) and 240-pin high performance quad flat pack (HQFP) packages. ◆

Faster XC4000E-1 FPGAs Support High-Performance Applications

Once again, continuing process improvements have led to the release of a new, faster speed grade for the XC4000E FPGA family. Devices with the new -1 speed grade are expected to start sampling in March and enter full production in June.



Based on an optimized 0.5 µ three-layer-metal process, the new -1 rated devices support typical system clock speeds in the 80 MHz range — about 20% higher performance than the XC4000E-2 FPGAs. The XC4000E-1 devices are applicable to a wide range of high-density, high-performance applications, such as PCI bus interfaces, fast ATM switches and video processing.

For pricing and availability information, please contact your local Xilinx sales representative. ◆

XILINX®

Product Discontinuance Policy Update

The Xilinx Product Discontinuance Policy provides for the early notification of future product changes and discontinuances, generous last-time buy periods, and relationships with end-of-life suppliers. Refer to page 14 in *XCell 23* for information about the development of the policy.

"End-of-Life" Supplier Selected

Xilinx has selected **Rochester Electronics, Inc. (REI)** as "end-of-life" supplier for Xilinx discontinued products. REI is the industry leader in after-market support for semicondutor suppliers. Our relationship with REI will provide for product availability beyond the Xilinx last-time-buy and last-time-ship periods. REI also provides capabilities such as assembly and test. Contact REI at its Newburyport, MA headquarters by phone at 508-462-9332, by e-mail at sales@rocelec.com, or on the internet at www.rocelec.com.

XC2000 Shipments to End in 1999

On December 20, 1996, Xilinx issued Product Discontinuance Notification PCN96010 for the XC2000 FPGA family. Included in the discontinuance are all commercial, industrial, military and hi-rel products. The last-time-buy period extends until January 1, 1999 *(see table)*.

The XC2000 devices, first introduced in 1985, can be replaced by more cost-effective FPGA and CPLD product families, such as the XC5200, XC7300 and XC9500 families, or by their HardWire™ equivalent, the XC2318.

XC3000 Series Product Line Streamlining

We plan to improve our leadtimes by removing device and package combinations with extremely low order volumes. A few XC3000 series components, mostly slower speed grades and unpopular pin grid array package combinations, will be discontinued within the next two years.

However, higher-performance XC3000 series devices are getting less expensive. The most recent price reductions for the XC3000-100 and XC3100A-4 devices have eliminated the need for the XC3000-70 and XC3100A-5 devices, so we are dicontinuing the C and I grades of those two devices. Users of these discontinued products can now move to the next-highest speed grade, maintaining pin and bitstream compatibility, and take advantage of decreased component costs.

For further information about these products, including a complete list of the ordering codes for the discontinued products, please contact your local sales office or visit the Xilinx WebLINX website. ◆

Product Discontinuance Schedule

MILESTONE	DATE	NOTES
XC2000 Product Line Discontinuance		
Notification	12/20/96	PCN96010
Last-time-buy	1/1/99	
Last-time-ship	6/30/99	
XC3000 -70 (C and I) Discontinuance		
Notification	1/31/97	PDN97003
Last-time-buy	1/31/98	
Last-time-ship	4/30/98	
XC3000 Low Volume Packages		
Notification	1/31/97	PDN97005
Last-time-buy	12/31/98	
Last-time-ship	3/31/99	
XC3100A -5 (C and I) Discontinuance		
Notification	1/31/97	PDN97004
Last-time-buy	1/31/98	
Last-time-ship	4/30/98	
XC3100A Low Volume Packages		
Notification	1/31/97	PDN97006
Last-time-buy	12/31/98	
Last-time-ship	3/31/99	

Xilinx Receives QML Certification

The Defense Supply Center Columbus (formerly DESC) has awarded Xilinx transitional certification to MIL-PRF-38535 Qualified Manufacturer Listing (QML). As with our ISO 9000 certification, QML demonstrates our status as a proven, world-class supplier of programmable logic.

About the QML Program

The QML program involves the certification of a quality and manufacturing system applicable to both military and commercial products — a "dual-use" system. Developed in 1988 at the direction of the Defense Science Board, QML calls for the use of "best commercial practices" for manufacturing and testing, allowing the supplier to optimize the manufacturing, assembly, screening and test flows. The QML certification is basically a validation that the company is well-managed and technically sound enough to be "world class" with minimal government interference. As a result, we have greater flexibility in controling the ways that we qualify, manufacture and test our military products.

Suppliers new to the QML program, such as Xilinx, are awarded "transitional" certification as they move from MIL-STD-883 to QML. It is our target to achieve full QML status before the end of 1997, but we will begin operating as a QML supplier immediately.

QML and MIL-STD-883

Xilinx has been qualified to MIL-STD-883 since 1988, and we have been a very active supporter of the Standard Microcircuit Drawing (SMD) Program. Under MIL-STD-883, we have been operating under a system that specifies the manufacturing requirements for our military products. For example, these requirements include temperature cycling and acceleration tests, and full electrical testing both before and after a "burn-in" period. These requirements apply to all products that we supply as SMD-qualified; ***each individual product*** is subject to the standard's screening and qualification requirements.

The QML program works to ensure the same high quality levels as MIL-STD-833 without all of its onerous testing requirements. The QML program focuses on the generic qualification of an envelope of processes and materials, rather than individual products. It allows for the use of pertinent existing military and commercial reliability data, statistical process controls (SPC), and in-process monitors. In short, the QML program encourages the use of the "best commercial practices" that are commensurate with military performance, quality and reliability.

Benefits of the QML Program.

The benefits of being a QML supplier are significant, both to Xilinx and our users.

- ***More Rapid Product Introductions —*** Historically, the MIL-STD-883 standards have caused a significant time lag between the release of new commercial products and their military/hi-rel versions. Under QML, this time lag will be greatly reduced, if not eliminated entirely.
- ***Improved Manufacturing Efficiency —*** Since we now have the ability to begin optimizing military screening previously mandated by MIL-STD-883, we will become a more efficient and cost-effective supplier to the military/hi-rel market.
- ***Access to Military Programs Requiring QML Product*** — There are some military programs that require the use of QML parts. Xilinx programmable logic solutions will now be available for those programs.
- ***Greater Access to New Markets*** — Since the QML program is based on the concept of "best commercial practices," the opportunity exists for Xilinx to explore the possibilities of using commercial pack-

aging technology (i.e., plastic packages) for use in high-reliability applications. More work is required in this area, but we now have the basis for evaluation.

How the program will be implemented

Our QML certification encompasses manufacturing and test processes at Xilinx, Seiko-Epson (wafer fabrication) and Anam Philippines (assembly). Consequently, all of our current Standard Microcircuit Drawing (SMD) products will be immediately transitioned to QML. We will begin marking our SMD parts with a "Q" to indicate QML. SMD documents will be updated to reflect our QML status. The SMD program will continue — as we introduce new products, they will be included in the SMD program as QML-certified, rather than MIL-STD-883 certified.

Because many of the new products that we intend to introduce for the military/hi-rel market will be produced at another foundry, United Microelectronics Corp. (UMC), it is our intention to seek QML certification for this facility by the end of 1997.

While other manufacturers are abandoning their military/hi-rel users, the participation of Xilinx in the QML program is one more demonstration of our strong commitment to support military and high-reliability applications, as well as a testament to the quality of Xilinx processes and products. ◆

XC5200 Family Breaks The $4 Price Barrier

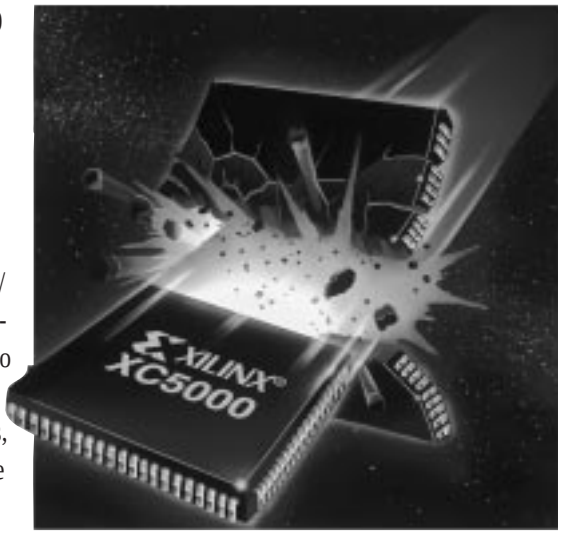
FPGA benefits now available to consumer and high-volume markets

Xilinx shipped the millionth unit of the XC5200 FPGA family in the fourth quarter of 1996. The XC5200 family reached this milestone faster than any previous FPGA product family.

As one result of the migration of this family to 0.5 µ three-layer-metal process technology, Xilinx has significantly reduced component die sizes, leading to dramatically reduced prices. In fact, Xilinx has introduced the world's first FPGA for less than $4. The direct price for the 256-logic-cell XC5202-6PC84C is now $3.95 (in 25,000 piece quantities).

The migration of the family to the 0.5 µ process has resulted in a "pad-limited" die size; that is, a die size limited by the number of I/O on the device, not the amount of logic. This, in turn, leads to production cost parity with low-end gate arrays. As a result, high-volume products can now achieve their cost and margin targets while obtaining all the traditional benefits of FPGA technology, including design flexibility and off-the-shelf availability. The XC5200 family is now the ideal logic solution for consumer and other high-volume products that require both low cost and fast time-to-market, such as set-top boxes, PC add-in cards, cable modems, and digital cameras.

With five XC5200 family devices ranging from 2,000 to 23,000 maximum logic gates in 15 different packages, there are now over 100 different device/package/speed combinations available to meet your exact design requirements, all at very affordable prices. ◆



New XACT*step* M1 Software for High-Density Design

Xilinx has begun shipments of the first version of its new XACT*step*™ M1 software, geared for high-density XC4000EX/XL applications. This software solution delivers unprecedented speed, utilization, and run-time performance for high-density FPGA designs.

XACT*step* M1.1 includes a new generation of core implementation applications, including mapping, optimization, timing-driven placement and routing, and timing analysis programs. This state-of-the-art software environment builds on technology from the Xilinx XACT™ and NeoCAD FPGA Foundry™ design systems to deliver high-performance with intuitive, easy-to-use design tools. Key features of this system include:

- Multi-level design support, with automatic netlist translation and integration
- A comprehensive timing-constraint language (Timespecs), with automatic links to synthesis tools
- Advanced, timing driven-placement and routing, with both push-button flows and auto-interactive capabilities
- Superior pin-locking and incremental design capabilities
- 100% back-annotation, with EDIF, VITAL and Verilog/SDF back-annotation interfaces

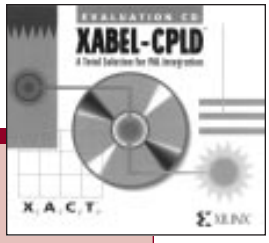
Designer feedback on this software has been very positive. One user who targeted a 90%-utilized XC4028EX device stated, "The M1 software is very easy to use with very little tweaking and no hand assist. The power of Timespecs made the timing constraints very simple to meet and verify."

XACT*step* M1.1, available for Solaris, SunOS, and HP UNIX platforms, includes libraries and interfaces for Synopsys, Mentor Graphics, and Viewlogic design environments. Future releases will provide EDA interface and Windows NT/95 support, as well as integrated solutions for the XC9500 and XC7300 CPLD families, the XC4000 and XC5200 FPGA series, and the XC3000A family.

XACT*step* M1.1 is being provided now to selected users known to have high-density FPGA designs in progress. All XACT*step* users with active maintenance contracts will be upgraded to this new version around mid-year. ***Please contact customer service to renew or check the status of your software maintenance agreement.*** ◆

XABEL-CPLD Available for Windows 95 and 3.x

XABEL-CPLD™ v6.1.2 now executes on both Windows 95 and Windows 3.x platforms. Existing XABEL-CPLD users can receive a free update upon request through normal Xilinx Customer Service channels. The update includes new EZTAG™ download software, but no cable. ◆



PRODUCT NAME	PART NUMBER	PRICE
XABEL-CPLD v6.1.2	DS-571-PC1	$495
XABEL-CPLD v6.1.2 Update	SC-571-PC1-CU	No charge

XILINX®

Update Your Foundation Software with the v6.0.2 Service Pack

Xilinx is pleased to offer all registered Foundation™ users an update to their current software. The new Foundation Service Pack updates your v6.0.1 software to v6.0.2. Shipments of this update to all registered Foundation owners began in February. To speed the distribution process, Foundation package owners are urged to register their software licenses if they have not already done so.

The v6.0.2 update includes numerous improvements to this integrated package of schematic entry, simulation, VHDL synthesis, and programmable logic implementation tools. A sampling of some of the enhancements are listed in the table. Foundation owners who have not yet received this update can download the files from the Xilinx FTP site or bulletin board, or call their Xilinx Customer Service representative to request the service pack CD.

Sampling of Foundation v6.0.2 improvements:

Schematic

- ✓ New design rule checker
- ✓ Improved bus connectivity and naming
- ✓ New schematic generation tool
- ✓ Wired schematic creation from XNF or ABL files
- ✓ Improved importing capability for Viewlogic schematics and symbols
- ✓ More user-friendly query/find feature
- ✓ More flexible symbol editor

Simulation

- ✓ Better Viewlogic simulation command language compatibility
- ✓ More intuitive graphical user interfaces
- ✓ Improved functionality in waveform viewer
- ✓ Context-sensitive help

Synthesis

- ✓ New graphical user interface status information
- ✓ Improved macrocell usage for comparators, adders, subtractors and up-down counters
- ✓ New documentation on compilation methodology
- ✓ Improved and more verbose information in error messages ◆

ProSeries Users Upgraded with Workview Office

Viewlogic started shipping versions 7.12 and 7.2 of Workview Office to in-warranty Xilinx ProSeries™ users in December (to be completed by the end of 1Q97). Workview Office 7.2 can be installed under Windows 95 or NT. However, Xilinx and Viewlogic have tested the integration of the Viewlogic toolset with the XACT*step*™ development system on Windows 95 only, not Windows NT.

Xilinx will be shipping the next version of Workview Office, version 7.3, with the next major XACT*step* release later this year. In version 7.3, the Viewsynthesis optimizer will be significantly enhanced, including 100% Synopsys language compatibility.

If you are currently an in-warranty ProSeries owner and have not received your free upgrade to Workview office, please contact Viewlogic via fax (508) 481 3961 or e-mail xilinxupdate@viewlogic.com. For any technical questions please contact Xilinx technical support. ◆

OrCAD to Provide Support for OrCAD-Xilinx Interface

For several years, Xilinx has developed, distributed and supported products that allowed OrCAD users to seamlessly interface their schematic designs with Xilinx devices. Due to OrCAD's growing reputation for offering quality programmable logic solutions, it has become evident that OrCAD is in the best position to offer support for designers wishing to use OrCAD products with Xilinx devices. As always, OrCAD and Xilinx will continue to work together so that designers can take advantage of the powerful features of OrCAD's solutions and the latest advancements in Xilinx devices.

"It has become evident that OrCAD is in the best position to offer support for designers wishing to use OrCAD products with Xilinx devices."

With our users' best interests in mind, Xilinx and OrCAD have jointly agreed to the following:

- The new recommended OrCAD/Xilinx solution consists of OrCAD FPGA Designer Pack (including OrCAD Capture and Simulate for Windows) for schematic entry, functional simulation, and timing simulation. All Xilinx schematic libraries, simulation models and the XNF interface are included in the FPGA Designer Pack. Only the "back-end" implementation (place and route) tools need to be acquired from Xilinx. The new design flow is very straightforward: from OrCAD Capture, generate an XNF file that is input into the XACT*step*™ tools for physical implementation; the post-routed XNF file is then input to OrCAD Simulate for post-route timing simulation.
- Starting with the next XACT*step* release, Xilinx will transfer development and support to OrCAD for the OrCAD/Xilinx Kit (DS-35), the Base System with OrCAD Interface package (DS-OR-BAS-PCI-C), and the Standard System with OrCAD Interface package (DS-OR-STD-PCI-C). (These packages include OrCAD's SDT386+ schematic capture tool and VST386+ simulation tool. SDT386+ and VST386+ have been replaced by Capture and Simulate for Windows, respectively.) Xilinx will no longer provide direct support for the OrCAD products.

We anticipate a very smooth transition. However, if you need any assistance, please contact your account manager or call OrCAD at 800-671-9505. ◆

COMING SOON: *DSP Module Generator*

The key to high-performance, FPGA-based digital signal processing is to craft the DSP algorithm for efficient implementation in the target FPGA architecture. Ironically, many DSP designers, while well-versed in the algorithmic approaches suitable for programming commercially-available digital signal processors, are not familiar with distributed arithmetic and similar techniques applicable to the hardware structures of FPGA devices.

To aid designers in implementing optimized DSP designs, Xilinx is developing a library of module generators for DSP functions, targeted for the XC4000 FPGA architecture. The production version of the Xilinx DSP Module Generator will be available in July. The first release includes modules to generate customized implementations of FIR filters, comb filters, integrators, multipliers, square root functions and various basic DSP building blocks. The tool outputs logic implementations compatible with the Xilinx implementation tools, behavioral models for simulation, instantiation code and schematic capture symbols. Additional modules will be available as plug-ins on an on-going basis.

For further information, see WebLINX (www.xilinx.com). ◆

USB and PCMCIA AllianceCOREs Now Available

The first products in the AllianceCORE™ program are now available:

- Cores for Universal Serial Bus (USB) applications from CAE/Inventra, Inc., and
- Cores for PCMCIA card design from Mobile Media Research, Inc.

The AllianceCORE program is a cooperative effort between Xilinx and independent third-party developers, with the goal of providing a broad selection of industry-standard cores that are optimized and verified for Xilinx programmable logic devices.

Universal Serial Bus

The USB AllianceCORE products from CAE/Inventra include a full-speed USB function controller, low-speed USB function controller, and three-port USB hub. These cores, targeted for the XC4000E and XC4000EX FPGA architectures and their HardWire™ equivalents, are delivered as XNF netlists (source code in Verilog RTL format also is available). They are fully-compliant to the USB v1.0 specification, and the FPGA-implementations were verified in hardware at a USB-IF sponsored interoperability workshop. To facilitate the integration of these cores, CAE/Inventra also offers a USB simulation model and FPGA-based prototyping board, for both hub and function controllers.

PCMCIA Fax/Modem

Mobile Media Research offers a PCMCIA fax/modem interface macro and a PCMCIA interface library. Fully PCMCIA v2.0 compliant, the fax/modem core is designed for implementation in XC3000 and XC5000 series FPGAs; when used with an external fax/modem chipset, it forms a complete PCMCIA fax/modem card. The PCMCIA library provides the basic building blocks for constructing a custom PC-card interface. Additional products include an FPGA-based prototyping board with 12 square inches of breadboarding area, a Windows-based CIS (Card Information Structure) generator, and system-level debug software.

These products are available now from their respective vendors. For vendor contact information, please see the AllianceCORE Partners chart below. Additional information about the AllianceCORE program can be found at WebLINX™ (www.xilinx.com). ◆

The chart below will join the other Alliance Program charts in the next issue of XCell.

AllianceCORE Partners - Feb. 1997

ARM Semiconductor (USA)
1095 E. Duane Ave., Suite 211
Sunnyvale, CA 94086 (USA)
Tel: 408-733-3344
Fax: 408-733-9922
armsemi@netcom.com
Microprocessors, microcontrollers, peripherals, communications

CAE/Inventra
1001 Ridder Park Drive
San Jose, CA 95131 (USA)
Tel: 408-451-5814
Fax: 408-451-5690
info@caetech.com
USB, PCI

Comit Systems
1250 Oakmead Pkwy, #210
Sunnyvale, CA 94088 (USA)
Tel: 408-988-2988
Fax: 408-988-2133
preeth@comit.com
www.comit.com
Base functions, communications

CoreEL Microsystems
46750 Fremont Blvd #208
Fremont, CA 94538 (USA)
Tel: 510-770-2277
Fax: 510-770-2288
chetan@coreel.com
ATM, communications

Eureka Technology
4962 El Camino Real, #108
Los Altos, CA 94022 (USA)
Tel: 415-960-3800
Fax: 415-960-3805
info@eurekatech.com
PCI, PowerPC peripherals

Integrated Silicon Systems, Ltd.
29 Chlorine Gardens
Belfast, BT9 5DL (No. Ire.)
Tel: +44 1232 664664
Fax: +44 1232 669664
info@iss-dsp.com; www.iss-dsp.com
DSP functions

Logic Innovations
6205 Lusk Boulevard
San Diego, CA 92121 (USA)
Tel: 619-455-7200
Fax: 619-455-7273
info@logici.com; www.logici.com
PCI, MPEG-2, ATM, commun.

Memec Design Services
1819 S. Dobson Rd., Suite 203
Mesa, AZ 85202 (USA)
Tel: 602-491-4311
Fax: 602-491-4907
info@mds.memec.com
www.mds.memec.com
Microprocessor peripherals, base functions, Xilinx design

Mobile Media Research, Inc.
1977 O'Toole Ave., Suite B207
San Jose, CA 95131 (USA)
Tel: 408-428-0310
Fax: 408-428-0379
sales@mobmedres.com
www.mobmedres.com
PCMCIA, CardBus

Phoenix Tech./Virtual Chips
2107 N. First Street, Suite 100
San Jose, CA 95131 (USA)
Tel: 408-452-1600
Fax: 408-452-0952
sales@vchips.com; www.vchips.com
PCI, USB, CardBus, ATM

Rice Electronics
PO Box 741
Florissant, MO 63032 (USA)
Tel: 314-838-2942
Fax: 314-838-2942
ricedsp@aol.com *DSP*

SAND Microelectronics
1630 Oakland Road, A103
San Jose, CA 95131 (USA)
Tel: 408-441-7138
Fax: 408-441-7538
sales@sandmicro.com
www.sandmicro.com *PCI, USB*

Sierra Research and Tech.
465 Fairchild Dr., Suite 130
Sunnyvale, CA 94088 (USA)
Tel: 415-988-4800
Fax: 415-988-0582
cores@srti.com
Communications, PCI, CPU

Toucan Technology
Technology Centre
Mervue Industrial Estate
Galway, Ireland
Tel: +353-91-757223
Fax: +353-91-755635
info@toucan.ie; www.toucan.ie
PCI, communications

VAutomation
20 Trafalgar Square
Suite 443 (4th Floor)
Nashua, NH 03063 (USA)
Tel: 603-882-2282
Fax: 603-882-1587
sales@vautomation.com
www.vautomation.com
Microprocessors, microcontrollers, communications

VisitWebLINX for more information: http://www.xilinx.com/products/logicore/tblpart.htm

New LogiCORE PCI Target Eases System Integration

MEMBER
PCI LOCAL BUS
SPECIAL INTEREST GROUP

The new LogiCORE™ PCI Slave (target-only) v1.1 has been shipped to all LogiCore PCI owners with current maintenance agreements. This updated release will further simplify integration of the core with the user's unique back-end logic. The design has been fine-tuned and constraints (e.g., new guide files) have been added. As a result, timing has improved, and the new version is more robust than its predecessor.

The improved User's Guide has been restructured to take the designer step-by-step through the design process. In addition, two new documents have been added to the product: a LogiCORE PCI Check List detailing the PCI commands that are supported by the core, and a PCI reference text book, *PCI Systems Architecture* (T. Shanley and D. Anderson, Mindshare Press). Furthermore, support for several new devices and package options has been added *(see table)*.

For complete data sheets and other information, please visit the LogiCORE site at WebLINX (www.xilinx.com/products/logicore/logicore.htm). ◆

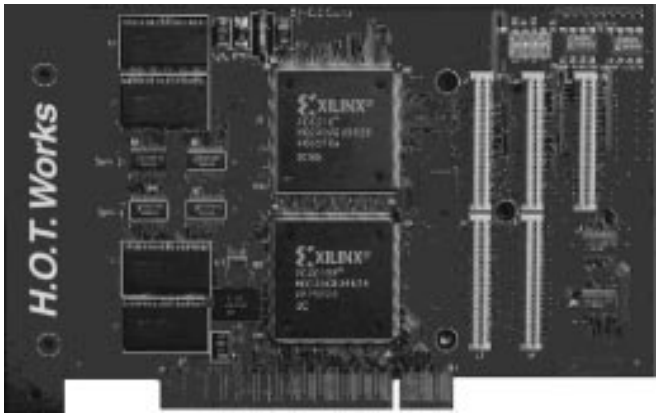
Device	Package	PCI Master	PCI Slave
XC4020E	HQ240	April 1997	✓*
	PQ208	April 1997	✓*
XC4013E	HQ240	April 1997	✓
	PQ208	✓	✓
	PQ160		✓

** Available on the web for registered LogiCORE customers*

Virtual Computing Debuts XC6200 Development Kit

Virtual Computing Corp. (Reseda, CA) has introduced the H.O.T. Works 6200 Development System, a complete programming and development system for the Xilinx XC6200 family of Reconfigurable Processing Units (RPUs). H.O.T. Works 6200 includes the PCI-XC6200 plug-in board and a number of software development tools:

- **The Lola Programming System** — a simple, object-oriented hardware description language for describing synchronous, digital circuits that was developed at ETH Zurich by Niklaus Wirth (the author of Pascal and Modula2)
- **XACT-6000™** — the Xilinx implementation tool set for the XC6200 family
- **XC6200 VHDL Elaborator** — a VHDL analyzer and EDIF netlist generator
- **Hardware Object Technology (H.O.T.) Interface** — tools that provide for the insertion of designs into executable C programs, enabling run-time reconfigurable computing
- **WebScope 6200** — a Java tool for real-time design emulation using the PCI-XC6200 board
- Design and application examples



The PCI-XC6200 board is a single PCI bus board featuring an XC6216 RPU, XC4013E FPGA (used for the PCI interface), 512Kb of SRAM, a programmable oscillator, and PCI mezzanine connectors for daughter boards.

List price for the entire kit is $995. For further information, contact Virtual Computer Corp. (tel: 818-342-8294; fax: 818-342-0240; e-mail: info@vcc.com) or visit its web page at www.vcc.com. ◆

Benchmarks Again Demonstrate XC9500 Pinlocking Capabilities

A new set of XC9500 pinlocking benchmarks focuses on two commonly-used comparator functions — magnitude and equality compares. Magnitude comparators are often used in digital peak detector circuits in audio and video applications. Equality comparators are a key part of page mode DRAM memory controllers.

As with previously-published CPLD benchmarks (*XCell 22*, page 18), the comparator benchmarks illustrate the CPLD device's capability to accommodate design changes with fixed pinouts while maintaining an acceptable level of design performance; in other words, not only must the iterated design route when the pinout is maintained, it must do so with minimal impact on design performance.

The following two sets of benchmark data show the relative pinlocking performance of the XC9500 CPLDs and a competitor's CPLD family. The designs are ABEL-HDL implementations of benchmarks suggested by the competitor, and are targeted at devices of the competitor's choosing. ABEL compiler and fitter options were chosen to maximize design performance, per each vendor's recommendations.

Magnitude Compare Benchmark

This benchmark contains a single 8-, 10-, or 12-bit magnitude comparator and is intended to measure the effect of routing resources and function block fan-in on the CPLD's pinlocking performance. A typical design change involves the correction of an error in which one of the input data paths was ordered incorrectly.

The benchmark results in **Figure 1** demonstrate that both the XC95108-15 and the ispLSI2096-80 were able to accommodate the design change without any impact on design performance. However, it should be noted that the XC95108-15 was faster overall than the other device.

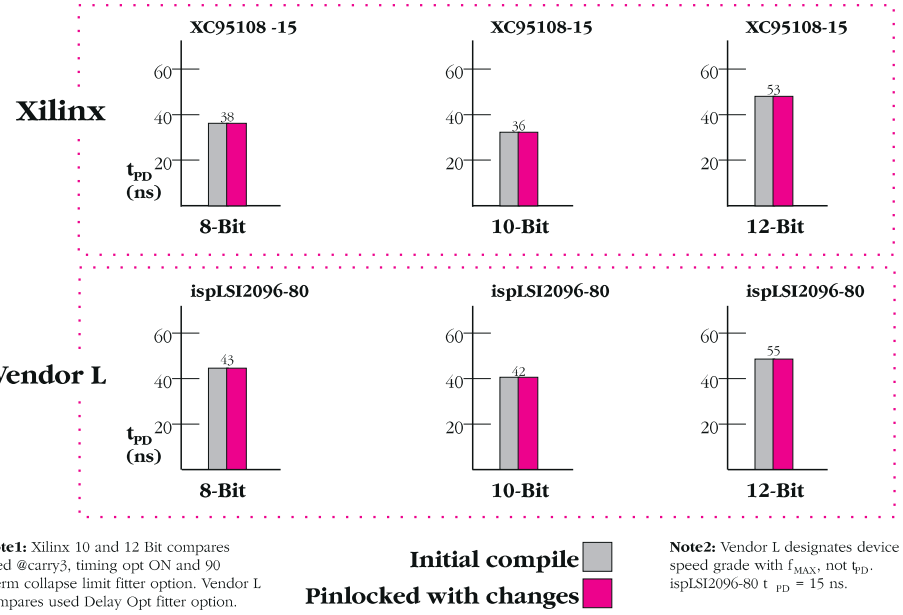
Equality Compare Benchmark

This benchmark contains a single 8-, 10-, or 12-bit equality comparator and is intended to measure the effect of routing resources and function block fan-in on the CPLD's pinlocking performance. A typical design change involves the correction of an error in which one of the input data paths was ordered incorrectly.

The benchmark results in **Figure 2** demonstrate the superiority of the XC9500 CPLD architecture. Not only was the XC95108 able to accommodate the design changes without any impact on design performance, that level of performance was significantly higher than the competitor's device. Vendor L's device

Continued on the next page

Figure 1: Magnitude Compare Performance



Note1: Xilinx 10 and 12 Bit compares used @carry3, timing opt ON and 90 pterm collapse limit fitter option. Vendor L compares used Delay Opt fitter option.

Note2: Vendor L designates device speed grade with f_{MAX}, not t_{PD}. ispLSI2096-80 t_{PD} = 15 ns.

XILINX®

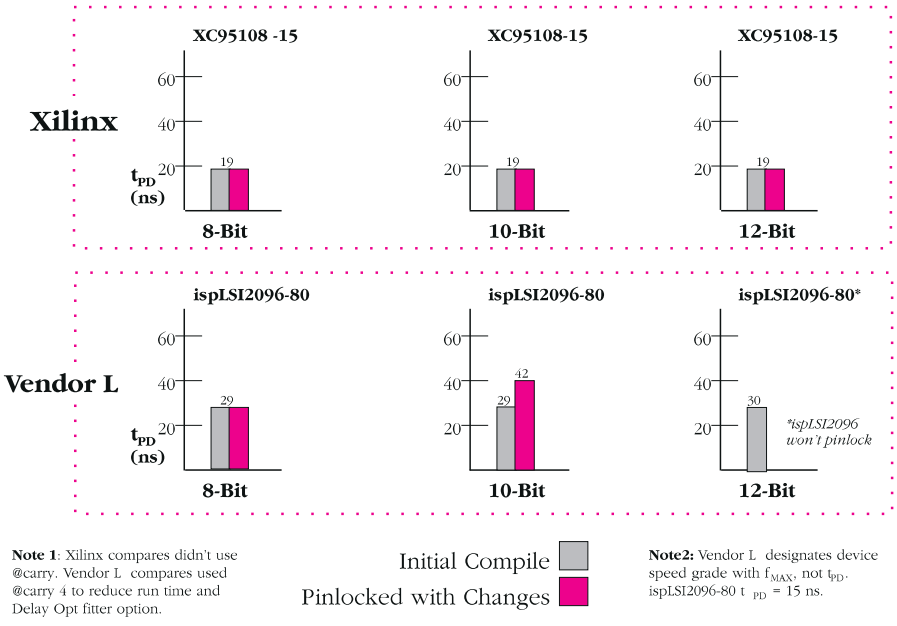
XC9500 Benchmarking

Continued from the previous page

used multi-level logic to implement the 8-bit equality compare; a 16-input, 16 product-term logic function that is implemented in a single pass in the XC9500 CPLD.

Vendor L's routing resources were stressed while attempting to pinlock the 10-bit equality compare; a 45% performance degradation was incurred after the design iteration. While attempting to pinlock the 12-bit equality compare, the performance didn't just degrade, the device completely failed to route.

Figure 2: Equality Compare Performance



Note 1: Xilinx compares didn't use @carry. Vendor L compares used @carry 4 to reduce run time and Delay Opt fitter option.

Note2: Vendor L designates device speed grade with f_{MAX}, not t_{PD}. ispLSI2096-80 t_{PD} = 15 ns.

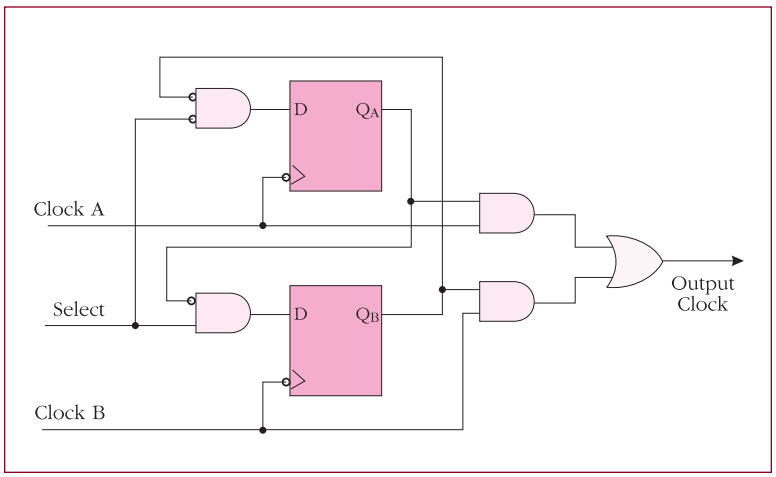
Conclusions

These benchmarks reconfirm the superior pin-locking performance of the XC9500 CPLD family. The wide function-block fan-in enables pinlocking of wide high-speed logic functions while at the same time delivering higher performance than competitive devices. Furthermore, because logic feedthroughs are not needed for routing, there is no performance degradation due to routing congestion. This timing consistency is as important as routing ability for maintaining pinlocked designs.

The XC9500 CPLD devices deliver high performance and feature the industry's best pin-locking capability, eliminating the need for PCB modifications due to design changes. This feature not only shortens design cycles and decreases design costs but also facilitates the use of in-system programmability to upgrade or modify systems in the field. ◆

Trouble-Free Switching Between Clocks

Asynchronously selecting between two clock sources can easily produce glitches that cause unreliable system behavior. The circuit diagrammed here avoids these problems.



While the SELECT input is stable (either High or Low), the two control flip-flops are in opposite states and one of the two clock inputs drives the clock output. When the SELECT input changes, there is no immediate impact until after the next falling edge of the originally-selected clock source, which also resets its control flip-flop. The Output Clock signal will then stay Low until the next falling edge of the newly-selected clock. This edge will set its control flip-flop, causing this clock to drive the Output Clock. Thus, with this circuit, any switching between clock sources is delayed by holding the output Low from the time the first clock goes Low until the time the second clock is Low. ◆

Demultiplexing 200 MHz Data Streams

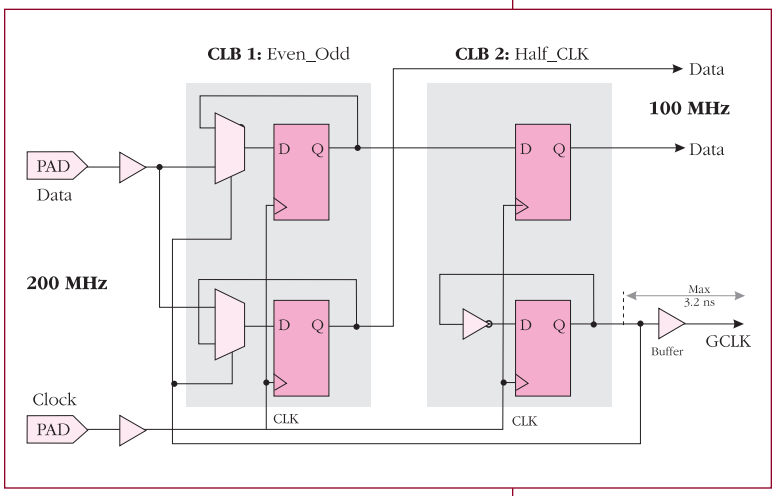
Modern serial data protocols (e.g., FireWire, SONET, ATM, T4) sometimes require clocks that are faster than maximum FPGA global clock speeds. To solve this problem, the incoming clock (200 MHz in the example below) can be used to demultiplex the incoming single data stream into two parallel data streams clocked at one-half the speed (100 MHz here).

The circuit diagrammed below avoids the set-up time of the XC3100A-09 FPGA's IOB input flip-flop and the delay of the global clock distribution network. Incoming data and clock are both routed to nearby CLBs. The delay on the data path from pad to CLB function generator is 2.1 ns (worst case), while the delay on the clock path from pad to CLB input is 2.3 ns. The CLB register's set-up time (function generator input to CLB clock input) is 1.5 ns. The longest possible input pad-to-CLB register set-up time is 2.1 + 1.5 - (0.7 x 2.3) = 2.0 ns. (This assumes 70% delay tracking; i.e., if one delay is at its worst-case value, the other delay cannot be shorter than 70% of its maximum value.)

The possibility of a pad-to-register hold time requirement is assessed by evaluating the opposite situation: (0.7 x 3.6) - 2.3 = 0.2 ns. Since the result is a positive value, the pad-to-register set-up time will always be positive, so there is no hold time requirement.

The circuit also can be cascaded to demultiplex the incoming data stream into four parallel streams (for example, for storage in the slightly slower XC4000E distributed RAM). Such a 1-to-4 demultiplexing structure uses just six CLBs.

The corresponding output multiplexing is more difficult, since the delay between clock input-to-output pad and clock-to-out in the XC3100A-09 is greater than 5 ns. An external ECL clocked multiplexer may be the most practical solution. ◆



FPGA Highs and Lows *Up in Space and Below the Surface*

The highest-flying Xilinx FPGAs are in instrumentation cards on-board the United States' space shuttle, as well as the Russian SOYUZ spacecraft and MIR space station. The instrumentation card contains two XC3042-70 PQ100C commercial-temperature devices in inexpensive plastic packages that have functioned properly in orbit for several years.

The FPGA depth record was set by a variety of XC3000 and XC4000 series devices used in oil exploration instruments that have dropped to a depth of more than 15,000 feet (5,000 meters). They help measure important parameters that may point to the existence of oil pockets. Used for days and weeks at a time, the devices have continued working at temperatures of up to 175° C (about 350° F). For future, deeper drillings, designers are now exploring the behavior of Xilinx devices at 200° C (the typical geothermal gradient is 30° C per 1,000 m). ◆

Using the HW-130 Programmer

If you have had difficulty installing your HW-130 Programmer, Xilinx Technical Support recommends this troubleshooting process.

First, before first connecting the HW-130 to the COM port of your PC (or after disconnecting it from the port), check to ensure that it powers up properly. The power-on LED indicator light located above the FAIL light should blink following power-on while the programmer performs a self-test, and then stop blinking and remain lit. If the power-on LED does not blink initially, or the FAIL light goes on and stays on, the programmer is probably defective; contact Xilinx Customer Service to obtain a replacement unit.

A typical installation and start-up of the programmer involves the following steps:

1. Insert the floppy disk and change to the "a:\>" (or "b:\>") prompt.
2. Type "install" and follow the instructions on the screen.
3. After installation of the software, "cd" to the target directory.
4. Hook up the programmer to the serial port of your PC and power it up. Make sure the FAIL LED is **not** flashing three or four seconds after power-on.
5. Type "hw130" to launch the application. The software will search all COM ports for the programmer and negotiate the highest baud rate after doing a reset of the programmer. The power LED of the programmer will flash for about four seconds during the reset.
6. Once communication has been established, you can select a device and use the programmer.

Assuming that this installation process has been followed completely, but the HW-130 is still not working properly, one of the following procedures may solve the problem:

- If you are using the DOS version, make sure you are **not** running out of a DOS window in Windows 3.1, 95 or NT. The hw130 program only works in a DOS-only environment.
- Make sure there is **not** a "hw130.ini" file in the working directory. Delete it if there is one.
- Check that you are using a standard serial cable and/or 9-25 or 25-9 pin cable adapters. Null modem cables will not work.
- Make sure the minimum 470K of conventional memory needed to launch the program is available. Type "mem" from the DOS prompt, look for the line, "Largest executable program size ...Kbyte." If it is less than 470K, unload some device drivers in the config.sys or autoexec.bat files and restart the PC (or run a memory optimization routine, such as "memmaker" provided with later DOS versions).
- Run "msd" (Microsoft diagnostics) from the DOS prompt, type in "C" for COM ports. Check that two COM ports are available (two 16550 UART chips). The additional port is required to support your mouse. The other settings of the COM ports (like the baud rate, data bits, and so on) do **not** matter because the HW130 software initializes these settings. Make sure the address used is correct for the COM ports. Type in "Q" from the main menu of msd for the IRQ settings on the PC. Make sure IRQ3 points to COM2 and 4, and IRQ4 to COM1 and 3. The software assumes the following default addresses and IRQ settings on the COM ports:

	COM1	COM2	COM3	COM4
Address	03F8	02F8	03E8	02E8
IRQ	4	3	4	3

- If all else fails, reboot the PC and enter the CMOS setup. Search around for the COM ports and try swapping the COM ports (i.e. use a different UART for the programmer). Point COM1 to COM2 and COM2 to COM1. If there is only one COM port, point it to COM1 instead of 2 (or vice versa). Exit and save the CMOS setup and try again. ◆

Q What should be done with unused I/O pins in an XC9500 CPLD design?

XC9500 devices have internal pull-up resistors on all I/O pins. However, these resistors are active only during power-up, device configuration, in-system programming, and Intest. During normal operation, the pull-up resistors are disabled.

Xilinx recommends that any unused I/O be tied to board ground.

The upcoming M1 software release supports "user-programmable grounds". This feature ties unused I/O cells to the internal lead frame ground of the CPLD device.

Need technical help right now? Here's where to start:

1. Find us on the Internet at www.xilinx.com

We update our **"Answers"** Web tool daily with the very latest application notes, data sheets, patches and solutions to your technical questions. Get immediate answers 24 hours per day!

If you don't have access to the Web or can't locate an answer via step #1, then...

2. Contact your nearest Customer Support Hotline

NORTH AMERICA SUPPORT

(Mon, Tues, Wed, Fri 6:30am-5pm Thur 6:30am - 4:00pm Pacific Time)
Hotline: 800 255 7778
or 408 879 5199
Fax: 408 879 4442
BBS: 408 559 9327
Email: hotline@xilinx.com

UNITED KINGDOM SUPPORT

(Mon, Tues, Wed, Thur 9:00am-12:00pm, 1:00-5:30pm, Fri 9:00am-12:00pm, 1:00-3:30pm)
Hotline: (44) 1932 820821
Fax: (44) 1932 828522
Email: ukhelp@xilinx.com

FRANCE SUPPORT

(Monday-Friday 9:30am-12:30pm, 2:00-5:30pm)
Hotline: (33) 1 3463 0100
Fax: (33) 1 3463 0959
Email: frhelp@xilinx.com

GERMANY SUPPORT

(Mon, Tues, Wed, Thur 8:00am-12:00pm, 1:00-5:00pm, Fri 8:00am-12:00pm, 1:00pm-3:00pm)
Hotline: (49) 89 991 54930
Fax: (49) 89 904 4748
Email: dlhelp@xilinx.com

JAPAN SUPPORT

(Mon, Tues, Thur, Fri 9:00am-5:00pm, Wed 9:00am-4:00pm)
Hotline: (81) 3 3297 9163
FAX: (81) 3 3297 0067
Email: jhotline@xilinx.com

Need a software update, authorization code, or documentation update?

Contact Xilinx Customer Service
in the U.S.: 800 624 4782
Europe: (44) 1932-349401
international: 408 559 7778, *(ask for Customer Service)* ◆

COMPONENT AVAILABILITY CHART

PINS	TYPE	CODE	XC3020A	XC3030A	XC3042A	XC3064A	XC3090A	XC3020L	XC3030L	XC3042L	XC3064L	XC3090L	XC3142L	XC3190L	XC3120A	XC3130A	XC3142A	XC3164A	XC3190A	XC3195A	XC4003E	XC4005E	XC4006E	XC4008E	XC4010E	XC4013E	XC4020E	XC4025E	XC4028EX	XC4036EX	XC4005XL	XC4010XL	XC4013XL	XC4020XL	XC4028XL	XC4036XL	XC4044XL	XC4052XL	XC4062XL
44	PLASTIC LCC	PC44		◆												◆																							
	PLASTIC QFP	PQ44																																					
	PLASTIC VQFP	VQ44																																					
	CERAMIC LCC	WC44																																					
64	PLASTIC VQFP	VQ64		◆					◆							◆																							
68	PLASTIC LCC	PC68	◆	◆											◆	◆																							
	CERAMIC LCC	WC68																																					
84	PLASTIC LCC	PC84	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆	◆						❖	❖							
	CERAMIC LCC	WC84																																					
	CERAMIC PGA	PG84	◆	◆	◆										◆	◆	◆																						
100	PLASTIC PQFP	PQ100	◆	◆	◆										◆	◆	◆				◆	◆									❖	❖							
	PLASTIC TQFP	TQ100														◆	◆																						
	PLASTIC VQFP	VQ100		◆	◆				◆	◆			◆			◆	◆				◆																		
	TOP BRZ. CQFP	CB100	◆		◆										◆	◆	❖																						
120	CERAMIC PGA	PG120																			◆																		
132	PLASTIC PGA	PP132			◆	◆											◆	◆																					
	CERAMIC PGA	PG132			◆	◆											◆	◆																					
144	PLASTIC TQFP	TQ144			◆	◆	◆			◆	◆	◆	◆	◆			◆	◆				◆	◆															
	CERAMIC PGA	PG144																																					
156	CERAMIC PGA	PG156																				◆	◆															
160	PLASTIC PQFP	PQ160				◆	◆											◆	◆	◆		◆	◆	◆	◆	◆					❖	❖	❖	❖					
164	TOP BRZ. CQFP	CB164					◆												◆	◆		❖																
175	PLASTIC PGA	PP175					◆												◆	◆																		
	CERAMIC PGA	PG175					◆												◆	◆																		
176	PLASTIC TQFP	TQ176					◆					◆		◆					◆																			
191	CERAMIC PGA	PG191																						◆	◆													
196	TOP BRZ. CQFP	CB196																							❖													
208	PLASTIC PQFP	PQ208					◆												◆	◆		◆	◆	◆	◆	◆					❖	❖	❖	❖				
	HI-PERF QFP	HQ208																							◆	◆	◆		◆						❖	❖		
223	CERAMIC PGA	PG223																		◆						◆	◆	◆					❖					
225	PLASTIC BGA	BG225																							◆	◆												
228	TOP BRZ. CQFP	CB228																								❖		❖										
240	PLASTIC PQFP	PQ240																								◆							❖	❖				
	HI-PERF QFP	HQ240																								◆	◆	◆	◆	❖					❖	❖	❖	❖	❖
256	PLASTIC BGA	BG256																														❖	❖	❖					
299	CERAMIC PGA	PG299																										◆	◆						❖				
304	HI-PERF. QFP	HQ304																										◆	◆	◆					❖	❖			
352	SUPER BGA	BG352																											◆	❖					❖	❖	❖		
411	CERAMIC PGA	PG411																												◆						❖	◆	◆	
432	SUPER BGA	BG432																												◆						❖	◆	◆	❖
475	CERAMIC PGA	PG475																																					◆
559	CERAMIC PGA	PG559																																					❖
560	SUPER BGA	BG560																																				◆	◆

FEBRUARY 1997

PINS	TYPE	CODE	XC4005L	XC4010L	XC4013L	XC5202	XC5204	XC5206	XC5210	XC5215	XC7236A	XC7272A	XC7318	XC7336	XC7336Q	XC7354	XC7372	XC73108	XC73144	XC9536	XC9572	XC95108	XC95216	XC95288
44	PLASTIC LCC	PC44									◆		◆	◆	◆	◆				◆	❖			
	PLASTIC QFP	PQ44											◆	◆	◆									
	PLASTIC VQFP	VQ44													◆					◆				
	CERAMIC LCC	WC44									◆			◆	◆	◆								
64	PLASTIC VQFP	VQ64																						
68	PLASTIC LCC	PC68										◆				◆	◆							
	CERAMIC LCC	WC68										◆				◆	◆							
84	PLASTIC LCC	PC84	◆	◆		◆	◆	◆	◆			◆					◆	◆			◆	◆		
	CERAMIC LCC	WC84										◆					◆	◆						
	CERAMIC PGA	PG84										◆												
100	PLASTIC PQFP	PQ100				◆	◆	◆									◆	◆			◆	◆		
	PLASTIC TQFP	TQ100																			◆	◆		
	PLASTIC VQFP	VQ100				◆	◆	◆																
	TOP BRZ. CQFP	CB100																						
120	CERAMIC PGA	PG120																						
132	PLASTIC PGA	PP132																						
	CERAMIC PGA	PG132																						
144	PLASTIC TQFP	TQ144				◆	◆	◆	◆															
	CERAMIC PGA	PG144																◆						
156	CERAMIC PGA	PG156				◆	◆																	
160	PLASTIC PQFP	PQ160					◆	◆	◆	◆								◆	◆			◆	◆	
164	TOP BRZ. CQFP	CB164																						
175	PLASTIC PGA	PP175																						
	CERAMIC PGA	PG175																						
176	PLASTIC TQFP	TQ176		◆				◆	◆															
191	CERAMIC PGA	PG191						◆																
196	TOP BRZ. CQFP	CB196																						
208	PLASTIC PQFP	PQ208	◆	◆	◆			◆	◆															
	HI-PERF QFP	HQ208								◆													◆	❖
223	CERAMIC PGA	PG223							◆															
225	PLASTIC BGA	BG225			◆				◆	◆								◆	◆					
228	TOP BRZ. CQFP	CB228																						
240	PLASTIC PQFP	PQ240			◆				◆															
	HI-PERF QFP	HQ240								◆														
256	PLASTIC BGA	BG256																						
299	CERAMIC PGA	PG299								◆														
304	HI-PERF. QFP	HQ304								◆														
352	PLASTIC BGA	BG352								◆													❖	❖
411	CERAMIC PGA	PG411																						
432	PLASTIC BGA	BG432																						
475	CERAMIC PGA	PG475																						
559	CERAMIC PGA	PG559																						
560	PLASTIC BGA	BG560																						

◆ = Product currently shipping or planned

❖ = New since last issue of *XCell*

Programmer Support For Xilinx XC7200/XC7300 CPLDs — February 1997

MANUFACTURER	MODEL	7236A	7272A	7318	7336	7336Q	7354	7372	73108	73144
ADVANTECH	PC-UPROG LABTOOL-48				DISQUALIFIED					
ADVIN SYSTEMS	PILOT-U40 PILOT-U84	10.84B 10.84B	10.84B	10.86B 10.86B	10.86B 10.86B	10.84B 10.84B	10.84B 10.84B	10.84B	10.84B	10.84B
AMERICAN RELIANCE, INC.	SPECTRUM-48									
B&C MICROSYSTEMS, INC.	Proteus	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97
BP MICROSYSTEMS	BP-1200 BP-2100	V3.15 V3.15	V3.15 V3.15	V3.15 V3.15	V3.18 V3.18	V3.15 V3.15	V3.15 V3.15	V3.15 V3.15	V3.15 V3.15	
BYTEK	CHIPBURNER-40		1.0a	1.0a	1.0a		1.0a	1.0a	1.0a	1.0a
DATAMAN	DATAMAN-48	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	V1.30	
DATA I/O	2900 3900/AutoSite UniSite			V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	V5.3 V5.3 V5.3	 V5.3 V5.3	 V5.3 V5.3	
DEUS EX MACHINA ENGINEERING	XPGM	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.40	V1.50
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ MEGAMAX	V2.4U V1.1E	V2.4U V1.1E	V2.5 V2.1x	V2.5 V2.1x	V2.4U V1.1E	V2.4U V1.1E	V2.4U V1.1E	V2.4U V1.1E	
ELAN	6000 APS				DISQUALIFIED					
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	V3.09 V3.09	
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV Speedmaster LV	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1	V3.1 V3.1 V3.1 V3.1	V1.1 V1.1 V1.1 V1.1	V1.1 V1.1 V1.1 V1.1
LEAP ELECTRONIC CO., LTD.	LEAPER-10 LP U4	V3.2 V2.1	V3.2 V2.1	V3.2 V3.0	V3.2 V3.0	V3.2 V2.1	V3.2 V2.1	V3.2 V2.1	V3.2 V2.1	
LOGICAL DEVICES	ALLPRO-88 ALLPRO-88XR ALLPRO-96 Chipmaster 2000 Chipmaster 6000 XPRO-1	6.4.26 V2.4U V1.31A	6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	V2.9Rev1 V2.9Rev1 6.4.26 V2.4U V1.31A	
MICROPROSS	ROM9000									
MQP ELECTRONICS	SYSTEM 2000 PIN-MASTER 48	Feb-97	Feb-97	Feb-97	Feb-97	Feb-97	Feb-97	Feb-97	Feb-97	Feb-97
NEEDHAM'S ELECTRONICS	EMP20	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	V3.10	
SMS	EXPERT OPTIMA				DISQUALIFIED DISQUALIFIED					
STAG	ECLIPSE	6.4.26	6.4.26	6.12.11	6.12.11	6.4.26	6.4.26	6.4.26	6.4.26	6.8.9
SUNRISE	T-10 UDP T-10 ULC				DISQUALIFIED DISQUALIFIED					
SUNSHINE	POWER-100 EXPRO-60/80	V8.40 V8.40	V8.40 V8.40	V8.40 V8.40	V8.40 V8.40		V8.40 V8.40	V8.40 V8.40	V8.40 V8.40	
SYSTEM GENERAL	TURPRO-1/FX MULTI-APRO	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02	V2.30 V3.02
TRIBAL MICROSYSTEMS	Flex-700 TUP-300 TUP-400	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09 V3.09 V3.09	V3.09	
XELTEK	SUPERPRO SUPERPRO II SUPERPRO II/P	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B	2.4B 2.4B
XILINX	HW-130	V2.04	V2.04	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00

Programmer Support For XC9500 CPLDs — February 1997

MANUFACTURER	MODEL	9536	9536F	9572	9572F	95108	95108F	95216
ADVANTECH	LABTOOL-48	1Q97	1Q97	1Q97	1Q97	1Q97	1Q97	
BP MICROSYSTEMS	BP-1200 BP-2100	V3.21 V3.21	V3.21 V3.21	Feb '97 Feb '97	Feb '97 Feb '97	V3.21 V3.21	V3.21 V3.21	
DATA I/O	2900 3900/AutoSite UniSite	BBS BBS BBS	BBS BBS BBS	 BBS BBS	 BBS BBS	 BBS BBS	 BBS BBS	
HI-LO SYSTEMS RESEARCH	All-07	Feb '97	Feb '97	1Q97	1Q97	Feb '97	Feb '97	
LOGICAL DEVICES	ALLPRO-88	Feb '97	Feb '97	1Q97	1Q97	Feb '97	Feb '97	
SMS	EXPERT OPTIMA	1Q97 1Q97	1Q97 1Q97	1Q97 1Q97	1Q97 1Q97	1Q97 1Q97	1Q97 1Q97	
STAG	ECLIPSE	Feb '97	Feb '97	1Q97	1Q97	Feb '97	Feb '97	
SYSTEM GENERAL	TURPRO-1/FX MULTI-APRO	Feb '97 Feb '97	Feb '97 Feb '97	1Q97 1Q97	1Q97 1Q97	Feb '97 Feb '97	Feb '97 Feb '97	
TRIBAL MICROSYSTEMS	Flex-700	Feb '97	Feb '97	1Q97	1Q97	Feb '97	Feb '97	
XILINX	HW-130*	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00	V4.00

Changes since last issue are noted in color.

**** NOTE**: Reflects the version of the Host Software.*

PROGRAMMER SUPPORT FOR XILINX XC1700 SERIAL PROMS - FEBRUARY 1997

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
ADVANTECH	PC-UPROG LABTOOL-48	DISQUALIFIED			
ADVIN	PILOT-U24 PILOT-U28 PILOT-U32 PILOT-U40 PILOT-U84 PILOT-142 PILOT-143 PILOT-144 PILOT-145	10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B		10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B 10.84B	
AMERICAN RELIANCE, iNC.	SPECTRUM-48				
B&C MICROSYSTEMS INC.	PROTEUS-UP40	3.7Q		3.7Q	
BP MICROSYSTEMS	CP-1128 EP-1140 BP-1200 BP-2100	 V3.15 V3.15	 V3.15 V3.15	 V3.15 V3.15	
BYTEK	135H-FT/U MTK-1000 MTK-2000 MTK-4000 FIREMAN-8M FIREMAN-8X CHIPBURNER-40	8E 8E 8E 8E 8E 8E 1.0a	8E 8E 8E 8E 8E 8E 1.0a	8E 8E 8E 8E 8E 8E 1.0a	8E 8E 8E 8E 8E 8E 1.0a
DATAMAN	DATAMAN-48	V1.30		V1.30	
DATA I/O	UniSite 2900 3900 AutoSite ChipLab 2700	New algorithms in progress			
DEUS EX MACHINA	XPGM	V1.60	V1.60	V1.60	V1.60
ELECTRONIC ENGINEERING TOOLS	ALLMAX/ALLMAX+ MEGAMAX	V2.4U V1.1E	V2.4U V1.1E	V2.4U V1.1E	
ELAN DIGITAL SYSTEMS	3000-145 5000-145 6000 APS	DISQUALIFIED			
HI-LO SYSTEMS RESEARCH	All-03A All-07	V3.19 V3.19	V3.19 V3.19	V3.19 V3.19	V3.19 V3.19
ICE TECHNOLOGY LTD	Micromaster 1000/E Speedmaster 1000/E Micromaster LV LV40 Portable Speedmaster LV	V3.17 V3.17 V3.17 V3.17 V3.17	V3.17 V3.17 V3.17 V3.17 V3.17	V3.17 V3.17 V3.17 V3.17 V3.17	V3.17 V3.17 V3.17 V3.17 V3.17
LEAP ELECTRONICS	LEAPER-10 LP U4	V2.0 V2.0		V2.0 V2.0	

MANUFACTURER	MODEL	XC1718D XC1736D XC1765D	XC1718L XC1765L	XC17128D XC17256D	XC17128L XC17256L
LINK COMPUTER GRAPHICS	CLK-3100	V5.61		V5.61	
LOGICAL DEVICES	ALLPRO-40 ALLPRO-88 ALLPRO-88XR ALLPRO-96 CHIPMASTER 2000 CHIPMASTER 6000 XPRO-1	 V2.7 V2.7 6.5.10 V2.4U V1.31A SPROM.310	 6.5.10 	 V2.7 V2.7 6.5.10 V2.4U V1.31A SPROM.310	 6.5.10
MICRO PROSS	ROM 5000 B ROM 3000 U ROM9000	V1.94 V3.84		V1.94 V3.84	
MQP ELECTRONICS	MODEL 200 SYSTEM 2000 PIN-MASTER 48	6.46 2.25	6.46 2.25	6.46 2.25	
NEEDHAM'S ELECTRONICS	EMP20	V3.10		V3.10	
RED SQUARE	IQ-180 IQ-280 Uniwriter 40 Chipmaster 5000	DISQUALIFIED DISQUALIFIED DISQUALIFIED DISQUALIFIED			
SMS	Expert Optima Multisyte Sprint Plus48	DISQUALIFIED DISQUALIFIED DISQUALIFIED DISQUALIFIED			
STAG	Eclipse Quasar	6.5.10	6.5.10	6.5.10	6.5.10
SUNRISE	T-10 UDP T-10 ULC	DISQUALIFIED DISQUALIFIED			
SUNSHINE	POWER-100 EXPRO-60/80	V8.40 V8.40		V8.40 V8.40	
SYSTEM GENERAL	TURPRO-1 TURPRO-1 F/X TURPRO-1 T/X APRO MULTI-APRO	V2.26H V2.26H V1.24 V1.16	V2.26H V2.26H V1.16	V2.26H V2.26H V1.16	V2.26H V2.26H V1.16
TRIBAL MICROSYSTEMS	TUP-300 TUP-400 FLEX-700	V3.19 V3.19 V3.19	V3.19 V3.19 V3.19	V3.19 V3.19 V3.19	V3.19 V3.19 V3.19
XELTEK	SuperPRO SuperPRO II SuperPRO II/P	 2.4B 2.4B		 2.4B 2.4B	
XILINX	HW-112* HW-130*	New algorithms in progress V2.03	V2.03	V2.03	V2.03

**NOTE: Reflects the version of the host software*

Changes since last issue printed in color

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS - FEBRUARY 1997 - 1 OF 2

	Company Name	Product Name	Version	Function	DesignKit	3K/ 4K	XC 5200	CPLD 7K9K	Uni Lib	PLATFORMS PC	Sun	RS6000	HP7
DIAMOND	Aldec	Active-CAD	2.2	Schematic Entry, State Machine & HDL Editor, FPGA Synthesis & Simulation	Included	✓	✓	✓	✓	✓			
	Cadence	Verilog	2.4	Simulation	Xilinx Front End	✓	✓	7k	✓		✓	✓	✓
		Concept	2.1	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
		FPGA Designer	9504	Topdown FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Synergy	2.3	FPGA Synthesis	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Composer	4.4	Schematic Entry	Xilinx Front End	✓		7k	✓		✓	✓	✓
	Mentor Graphics	Autologic	A.3-B.1	Synthesis	Xilinx Synthesis Lib.	✓	✓	7k	✓		✓	✓	✓
		Design Architect	B.x	Schematic Entry	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickSim II	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		QuickHDL	B.x	Simulation	Call Xilinx	✓	✓	7k	✓		✓	✓	✓
		Galileo	3.2.5	Synthesis	Call Mentor	✓	✓	✓	✓		✓	✓	✓
		Leonardo	4.0.1	Synthesis	Call Mentor	✓	✓	✓	✓		✓	✓	✓
	OrCAD	Capture (Win)	7.0	Schematic Entry	Call OrCAD	✓	✓	✓	✓	✓			
		Simulate (Win)	6.10	Simulation	Call OrCAD	✓	✓	✓	✓	✓			
		VST 386+ (DOS)	1.2	Simulation	Call OrCAD	✓			✓	✓			
		SDT 386+ (DOS)	1.2	Schematic Entry	Call OrCAD	✓			✓	✓			
		PLD 386+ (DOS)	2.0	Synthesis	Call OrCAD	✓			✓	✓			
	Synario Design Automation	ABEL	6.3	Synthesis, Simulation	ABEL-XCPLD			✓	✓	✓			
		Synario	2.3	Schematic Entry, Synthesis & Simulation	SYRO-LCA, SYRO-XCPLD	✓	✓	✓	✓	✓			
	Synopsys	FPGA Express	1.0	Synthesis	Call Synopsis	✓	✓	TBD		✓			
		FPGA Compiler	3.5	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		VSS	3.5	Simulation	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
		Design Compiler	3.5	Synthesis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
	Viewlogic	WorkView Office	7.1.2/7.2	Schem/Sim/Synth	Call Xilinx	✓	✓	✓	✓	✓	✓	✓	✓
		ProSynthesis	5.02	Synthesis	Call Xilinx	✓	✓	7k	✓	✓	✓	✓	✓
		ProSim	6.1	Simulation, Timing Analysis	Call Xilinx	✓	✓	7k	✓	✓	✓	✓	✓
		ProCapture	6.1	Schematic Entry	Call Xilinx	✓	✓	7k	✓	✓	✓	✓	✓
		PowerView	6.0	Schem/Sim/Synth/Timing Analysis	Call Xilinx	✓	✓	✓	✓		✓	✓	✓
RUBY	Capilano Computing	Design Works	3.1	Schematic Entry/Sim	XD-1	✓			✓	✓			
	Compass Design Automation	ASIC Navigator		Schematic Entry	Xilinx Design Kit	✓	✓	7k			✓		✓
		X-Syn		Synthesis		✓					✓		✓
		QSim		Simulation		✓	✓	7k			✓		✓
	Escalade	DesignBook	2.0	Design Entry		✓			✓	✓	✓		
	Exemplar Logic	Galileo	3.2	Synthesis/Timing Analysis Simulation	Included	✓	✓	✓	✓	✓	✓		✓
		Leonardo	4.0.1WS / 4.02PC	Synthesis	Included	✓	✓	✓	✓	✓	✓		✓
	IK Technology Co.	Ishizue Professionals	1.06	Schematic Entry/Simulation	Xilinx Design Kit	✓	4Q			✓	✓		✓
	IKOS Systems	Voyager	2.31	Simulation	Xilinx Tool Kit	✓	✓				✓		✓
		Gemini	1.21	Simulation	Xilinx Tool Kit	✓	✓				✓		✓
	INCASES Engineering GmbH	Theda	4.1	Design Entry	Xilinx Kit	✓							✓
	ISDATA	LOG/iC Classic	4.2	Synthesis	LCA-PP	✓		7k	✓	✓	✓		✓
		LOG/iC2	4.2	Synthesis Simulation	Xilinx Mapper	✓	✓	7k	✓	✓	✓		✓
	Logic Modeling Corp. (Synopsis Division)	Smart Model		Simulation Models	In Smart Model Lib.	✓	✓	7k,9k		✓	✓	✓	✓
		LM1200		Hardware Modeler	Xilinx Logic Module	✓		7k,9k		✓	✓	✓	
	Model Technology	V-System/VHDL	4.4j (PC) / 4.6a (WS)	Simulation		✓			✓	✓	✓	✓	✓
	Protel Technology	Advanced Schematic	3.2	Schematic Entry	Included	✓	✓	7k	✓	✓			
		Advanced PLD	3	PLD/FPGA Design & Simulation	Included	✓	✓	7k		✓			
	Quad Design Technology	Motive	4.3	Timing Analysis	XNF2MTV	✓				✓	✓	✓	✓
	SimuCad	Silos III	96.1	Schematic Entry & Simulation	Included	✓	✓		✓	✓			
	Sophia Sys & Tech	Vanguard	5.31	Schematic Entry	Xilinx I/F Kit	✓		✓		✓	✓		✓
	Summit Design Corp.	Visual HDL	3.0	Graphical Design Entry/Simulation/Debug	EDIF Interface	✓	✓	✓	✓	✓	✓	✓	✓
	Synplicity, Inc.	Synplify-Lite	2.6b	Synthesis	Xilinx Mapper	✓	✓	9k	✓	✓	✓		✓
		Synplify	2.6b	Synthesis	included	✓	✓	9k	✓	✓	✓		✓
	TopDown Design Solutions	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓	✓		✓	✓	✓	✓	

XILINX ALLIANCE-EDA COMPANIES & PRODUCTS - FEBRUARY 1997 - 2 OF 2

	Company Name	Product Name	Version	Function	DesignKit	2K/3K/4K	XC 5200	CPLD 7K9K	Uni Lib	Platforms PC	Sun	RS6000	HP7
RUBY	TopDown Design Solutions	V-BAK	1.1	XNF to VHDL translator	XNF interface	✓	✓		✓	✓	✓	✓	
RUBY	Veda Design Automation Inc	Vulcan	4.5	Simulation	XILINX Tool Kit	✓					✓		✓
RUBY	Veribest	Veribest VHDL	14.0	Schematic Entry	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
RUBY		Veribest Verilog	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
RUBY		VeriBest Simulator	14.0	Simulation	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
RUBY		DMM	14.x	Design Management	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
RUBY		VeriBest Synthesis	14.0	Synthesis	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
RUBY		Synovation	12.2	Synthesis	Xilinx FPGA Design Kit	3k,4k			✓	✓	✓		✓
RUBY		PLDSyn	12.0	Design Entry Synthesis		✓		7k		✓	✓		✓
RUBY		VerBest Design Capture	14.x	Design Capture	Xilinx FPGA Design Kit	3k,4k	✓		✓	✓	✓		✓
EMERALD	Accolade Design Automation	Peak VHDL	2.21	Simulation	Xilinx Plus	✓	✓			✓			
EMERALD		Peak FPGA	2.20	Synthesis	Included	✓	✓	✓		✓			
EMERALD	ACEO Technology, Inc.	Asyn	4.1	Synthesis	Included	✓	✓		✓	✓	✓	✓	✓
EMERALD		Softwire	3.3	Multi-FPGA Partitioning	Included	✓	✓		✓	✓	✓	✓	✓
EMERALD		Gatran	3.3	ASIC to FPGA Netlist Mapping	Included	✓	✓		✓	✓	✓	✓	✓
EMERALD	Acugen Software, Inc.	Sharpeye	2.60	Testability Analysis	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD		ATGEN	2.60	Automatic Test Generation	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD		AAF-SIM	2.60	Fault Simulation	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD		PROGBSDL	2.63	BSDL Customization	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD		TESTBSDL	2.63	Boundary Scan ATG	AALCA interface	✓	✓	7k		✓	✓		✓
EMERALD	ALPS LSI Technologies	Edway Design Systems		Synthesis/Simlulation		✓		✓		✓			
EMERALD	Aptix Corporation	System Explorer	3.1	System Emulation	Axess 3.1	✓	✓	✓			✓		✓
EMERALD		ASIC Explorer	2.3	ASIC Emulation	Axess 2.3	4K	✓		✓				
EMERALD	Aster Ingenierie S.A.	XILLAS	4.2	LASAR model generation	Worst Case Simulation	✓		7k		✓	✓		✓
EMERALD	Auspy Development Co.	APS	1.3.3	Multi-FPGA Partitioning	Included	✓	✓			✓	✓		
EMERALD	Chronology Corporation	TimingDesigner	3.0	Timing Specification and Analysis	Included	✓	✓	7k,9k	✓	✓	✓		✓
EMERALD		QuickBench	1.0	Visual Test Bench Generator	Included	✓	✓	7k,9k	✓	✓	✓		✓
EMERALD	CINA-Computer Integrated Network Analysis	SmartViewer	1.0e	Schematic Generation	XNF Interface	✓		7k		✓			
EMERALD	Epsilon Design Systems	Logic Compressor		Synthesis optimization		✓	✓			✓	✓	✓	✓
EMERALD	Flynn Systems	Probe	3.0	Testability Analysis	Xilinx Kit	✓	✓	7k		✓			
EMERALD		FS-ATG	3.0	Test Vector Generation	Xilinx Kit	✓	✓	7k		✓			
EMERALD		CKTSIM	3.0	Logic Analysis	Xilinx Kit	✓	✓	7k		✓			
EMERALD		FS-SIM	3.0	Simulation	Xilinx Kit	✓	✓	7k		✓			
EMERALD	Fujitsu LSI	PROVERD		Top-Down Design System	Included	3k,4k				✓			
EMERALD	Harmonix Corporation	PARTHENON	2.3	Synthesis		4k		7k		✓	✓		
EMERALD	Logical Devices	Total Designer	4.7	Simulation & Synthesis	Call Xilinx	✓	✓	✓	✓	✓			
EMERALD		Ulysa	1.0	VHDL Synthesis	Call Xilinx	✓	✓	✓	✓	✓			
EMERALD	MINC	PLDesigner-XL/PL-Synthesizer	3.3/3.2.2	Synthesis	Xilinx Design Module	✓				✓	✓		✓
EMERALD	Teradyne	Lasar	6	Simulation	Xilinx I/F Kit	✓					✓		✓
EMERALD	Tokyo Electron Limited	ViewCAD	1.2	FLDL to XNF translator	XNFGEN	✓							
EMERALD	Trans EDA Limited	TransPRO	1.2	Synthesis	Xilinx Library	✓					✓		✓
EMERALD	Visual Software Solutions	Statecad	3.0	Grph. Design Entry, Sim., Debug		✓	✓	✓	✓	✓	✓		✓
EMERALD	Zuken	Tsutsuji		Synthesis/Simulation	XNF Interface	3k,4k					✓	✓	✓
EMERALD	Zycad	Paradigm RP		Rapid Prototyping		✓					✓		✓
EMERALD		Paradigm XP		Gate-level Sim		✓					✓		✓

Items that have changed since the last issue (XCell 23) are in color.
The following entry was removed: MEMEC

Diamond: These partners have strong strategic relationships with Xilinx and have a direct impact on our releases. Typically, Xilinx is directly involved in the development and testing of the interface to XACT*step* software for these products.

Ruby: These partners have a high degree of compatibility and have repeatedly shown themselves to be significant contributors to our users' development solutions.

Emerald: Proven Xilinx compatibility

XILINX ALLIANCE-EDA CONTACTS - FEBRUARY 1997

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Changes since last issue (*XCell* 23) printed in color.

XILINX RELEASED SOFTWARE STATUS - FEBRUARY 1997

XILINX INDIVIDUAL PRODUCTS

Key	Product Category	Product Description	Product Function	Xilinx Part Reference Number	Current Version by Platform PC1 6.2	SN2 4.1.x	HP7 9.01	Last Updt Comp	Previous Version Release	Notes/ Features
	CORE XEPLD	XC7K Support	Core Implementation	DS-550-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	PC update by request only
U*	XABEL-CPLD	XC7K, XC9500 Support	Entry/Simulation/Core	DS-571-PC1	6.1.2			7/96	6.10	New version w/Win 95 to 3.11, update by request
*	XACT-CPLD	XC7K, XC9500 Support	Core + Interface	DS-560-xxx	6.0.1	6.0.1	6.0.1	7/96	6.0	
	Mentor	8.4=A.4	Interface and Libraries	DS-344-xxx		5.2.1	5.2.1	7/96	5.20	
	OrCAD		Interface and Libraries	DS-35-PC1	6.0.1			7/96	6.0	Support for SDT+, VST+ v1.2
	Synopsys		Interface and Libraries	DS-401-xxx		5.2.1	5.2.1	7/96	5.20	DA1 platform remains at v5.2
	Viewlogic	PROcapture	Interface and Libraries	DS-390-PC1	6.0.1			7/96	5.2/6.0	Includes PRO Series 6.1
	Viewlogic	PROsim	Interface and Libraries	DS-290-PC1	6.0.1			7/96	6.0	Includes PRO Series 6.1
	Viewlogic		Interface and Libraries	DS-391-xxx	6.0.1	5.2.1	5.2.1	7/96	6.0	
	XABEL		Entry,Simulation,Lib, Optimizer	DS-371-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	Now available on HP7
	XBLOX		Module Generator & Optimizer	DS-380-xxx	5.2.1	5.2.1	5.2.1	7/96	5.2/6.0	
E	Verilog	2K,3K,4K,4KE,5K Lib.	Models & XNF Translator	ES-VERILOG-xxx		1.00	1.00	na	na	Sun and HP
E	XC4000EX	XC4000EX Support	Core Implementation	PR-4EX-WS		pre-release	pre-release	na	na	Pre-release software available to pre-determined users

XILINX PACKAGES

Key	Product Category	Silicon Support 2K	3K	4K/E	5K	7K	9K	Xilinx Part Reference Number	PC1 6.2	SN2 4.1.x	HP7 9.01	Last Updt Comp	Previous Version Release	Notes/ Features
	Cadence	X	X	X	X	X	X	DS-CDN-STD-xxx		5.2.1	5.2.1	7/96	5.20	
	Mentor	X	X	X	X	X	X	DS-MN8-STD-xxx		5.2.1	5.2.1	7/96	5.20	No AP1 update
	Mentor	X	X	X	X	X	X	DS-MN8-ADV-xxx		7.00	7.00	na	na	
U	OrCAD	X	X	X	X	X	X	DS-OR-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	OrCAD	X	X	X	X	X	X	DS-OR-STD-PC1	6.0.1			7/96	6.0	
	Synopsys		X	X	X	X	X	DS-SY-STD-xxx		5.2.1	5.2.1	7/96	5.20	Includes DS-401 v5.2
	Synopsys		X	X	X	X	X	DS-SY-ADV-xxx		7.00	7.00	na	na	Includes DS-401 v5.2
U	Viewlogic	X	X	X	X	X	X	DS-VL-BAS-PC1	6.0.1			7/96	6.0	Customer w/v6.0 will receive v6.0.1 update
	Viewlogic	X	X	X	X	X	X	DS-VL-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.26.0	DA1 platform remains at v6.0
	Viewlogic	X	X	X	X	X	X	DS-VL-ADV-xxx	7.00	7.00	7.00	na	na	
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-BAS-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-STD-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewlogic/S	X	X	X	X	X	X	DS-VLS-EXT-PC1	6.0.1			7/96	6.0	Currently updating in-warranty cust. w/WVO
	Viewllogic/S	X	X	X	X	X	X	DS-VLS-ADV-PC1	7.00			na	na	
U	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-BAS-xxx	6.0.1			7/96	na	Customer w/v6.0 will receive v6.0.1 update
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-STD-xxx	6.0.1	5.2.1	5.2.1	7/96	5.2/6.0	Includes 502/550/380
	3rd Party Alliance	X	X	X	X	X	X	DS-3PA-ADV-xxx	7.00	7.00	7.00	na	na	Includes 502/550/380 & Foundry
	Foundation Series	X	X	X	X	X	X	DS-FND-BAS-PC1	6.0.2			2/97	7/96	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-BSV-PC1	6.0.2			2/97	7/96	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STD-PC1	6.0.2			2/97	7/96	Includes support for XC4000E and XC9500
	Foundation Series	X	X	X	X	X	X	DS-FND-STV-PC1	6.0.2			2/97	7/96	Includes support for XC4000E and XC9500
	LogiCore-PCI Slave			X				LC-DI-PCIS-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	LogiCore-PCI Master			X				LC-DI-PCIM-C	1.10	1.10	1.10	na	na	Requires signed license agreement
	Evaluation	X	X	X	X	X	X	DS-EVAL-XXX-C	2.00	2.00	2.00	4/96	01/04	PC, Sun, HP kits with v5.2.1 and v6.0.1

KEY: *N=New Product E= Engineering software for in-warranty users by request only U= Update by request only * = Check BBS or FTP site.*

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FAX in Your Comments and Suggestions

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