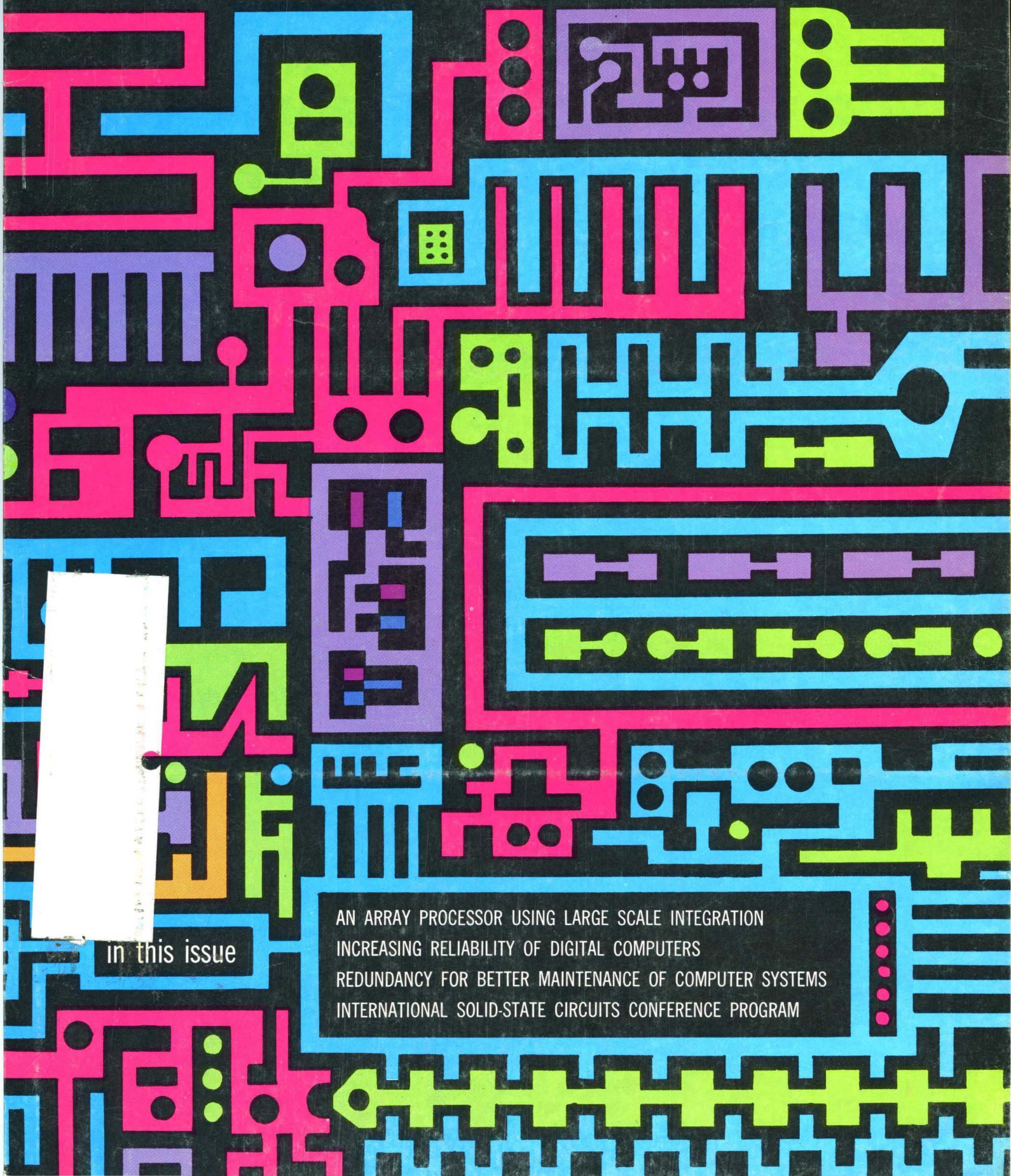
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS JANUARY 1969



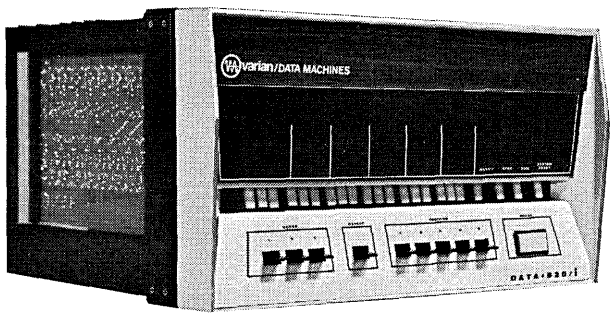
in this issue

The mystery of Stonehenge. Even the world's most famous special-purpose computer soon outlived its usefulness. There's a lesson in there somewhere.

The Varian Data 620/i. 18 months old. Over 450 delivered. And no mystery at all.

More than 3,000 years ago, Stonehenge did a crude but incredible job of computing a variety of things.

Today, the system-oriented Varian Data 620/i does an incredible job too. Because the general purpose 620/i has a bigger instruction set than any other computer in its class. 1.8 μsec. cycle time. 16/18 bit words. 4-32K memory. Easy interfacing capability. Multi-level priority interrupts. Field-proven software. 10½ inches of rack space.



The Varian Data 620/i is a very timely computer. And it costs $13,900 with 4K 16-bit memory and ASR 33 TT. Less than any other computer in its class. Write for your brochure today. You'll get more than the time of day.

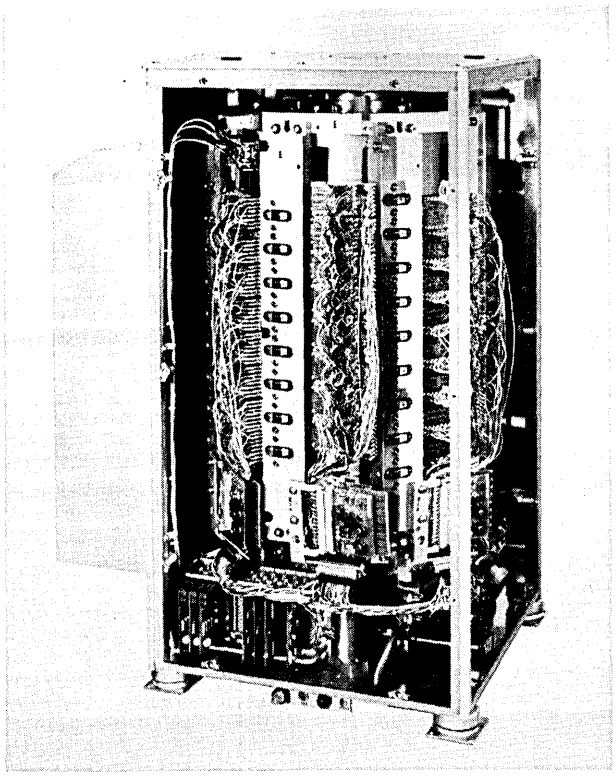
varian data machines

a varian subsidiary
2722 Michelson Drive/Irvine/California 92664
(714) 833-2400

SALES OFFICES: U.S., Santa Monica and San Francisco, California; Vernon and Westport, Connecticut; Chicago, Illinois; Houston, Texas; Fort Washington, Pennsylvania; Washington, D.C.; Waltham, Massachusetts; Fort Lauderdale, Florida. INTERNATIONAL: Australia, Belgium, Canada, France, Germany, India, Italy, South Africa, Sweden, Switzerland, United Kingdom and Ireland.

CIRCLE NO. 1 ON INQUIRY CARD

Fact:



Drum memories add power to power systems.

Many sophisticated computer systems are using Vermont Research drum memories to provide large capacity, fast operation and years of dependable, trouble-free service. For example, VRC's model 1032 is being used with a Sigma 2 computer in a new line of digital process controllers for power generation and industrial work. The computer has access to more than 4 million bytes of data, and can reach any portion of that within 8.7 milliseconds, on the average. The data moves between drum and computer at a speed of two million bits per second.

The result is a system of large and varied capabilities, able to operate for long periods with the dependability needed by large and vital industrial applications.

The 1032 drum may be used as easily by other computers, large or small. Complete with a self-enclosed interface package, it fits simple or complex systems. Applications range from simple stand-by memory for display systems, to multi-computer, time-shared memory and data exchange.

You'll find details about the 1032 and other Vermont Research Drum Memories in the Brochure DB-6809. Send for a copy today . . . it may help you add power to your next system.

Computers are known by their MEMORIES

. . . so is

Vermont Research
CORPORATION

DRUM MEMORIES • SYSTEMS • DISK PACKS

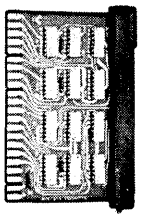
20a Precision Park • North Springfield, Vermont 05150 • Tel. 802/886-2256 • TWX 710 363-6533

When it comes to engineering opportunities (and the good life, North Country style), the place to come is Vermont Research Corporation. For specific information, contact: RICHARD A. STOVER, Vice President-Engineering.

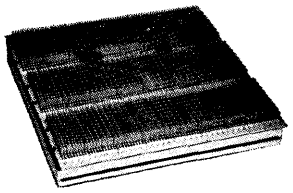
CIRCLE NO. 2 ON INQUIRY CARD

number one in complete products and capabilities for automatic wire-wrap* assembly

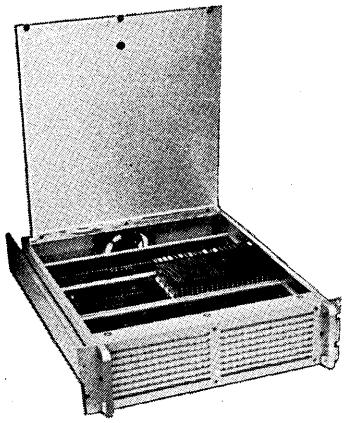
SERIES AW



DC to 30MC AW Medium CARDS



120 CARD AW BASE BOARD



120 CARD AW DRAWER CAGE

From Control Logic . . . to help you utilize the benefits of automatic wire-wrap assembly in the electronic systems you want! Benefits like reducing wiring errors by a factor of 100:1. Simplifying (even eliminating) expensive direct wire testing. Making reliable, fast, numerous (600 to 1200 per hour) gas-tight electrical connections with a failure rate that is less than 1 in 100,000 connections. Eliminating confusing, unfathomable wire build-up rat's nests with every wire in a known position . . . and a 50% reduction in wiring costs!

Control Logic help begins with a complete Series C family of automatic assembly products to satisfy all aspects of systems construction: a *complete* choice of DTL and TTL circuit cards with speeds of DC through 30 MC; *complete* packaging products from breadboarding to full system design, including connector baseplates and card cage housings designed for optimum utilization of automatic wire-wrap processes — 7 package assemblies for automated design for up to 120 card systems!

Control Logic offers complete services in design and specification of the system you want. Control Logic can generate a wiring list from your logic network diagrams. Can help you construct prototypes utilizing standard Series C components with any type of connection terminal. Can help you convert to automatic wire-wrap processes at any phase in a program.

Control Logic, to complete the picture, offers *production* of the wire-wrap systems you want . . . in part or *complete:* systems tested, checked-out and ready to serve your function. Yes, even if you have a small volume, low budget job . . . or you don't want to invest in automatic wire-wrap equipment, now . . . Control Logic can help you achieve automatic assembled systems! Call or write for BROCHURE 12 on SERIES AW products and services, today!

CONTROL LOGIC, INC.

3 Strathmore Road, Natick, Massachusetts 01760
Tel: (617) 235-1865 or (617) 235-1170

* "Wire-Wrap" is the registered trademark of the Gardner-Denver Company, Grand Haven, Michigan.

CIRCLE NO. 3 ON INQUIRY CARD

JANUARY 1969 • VOLUME 8 • NUMBER 1

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
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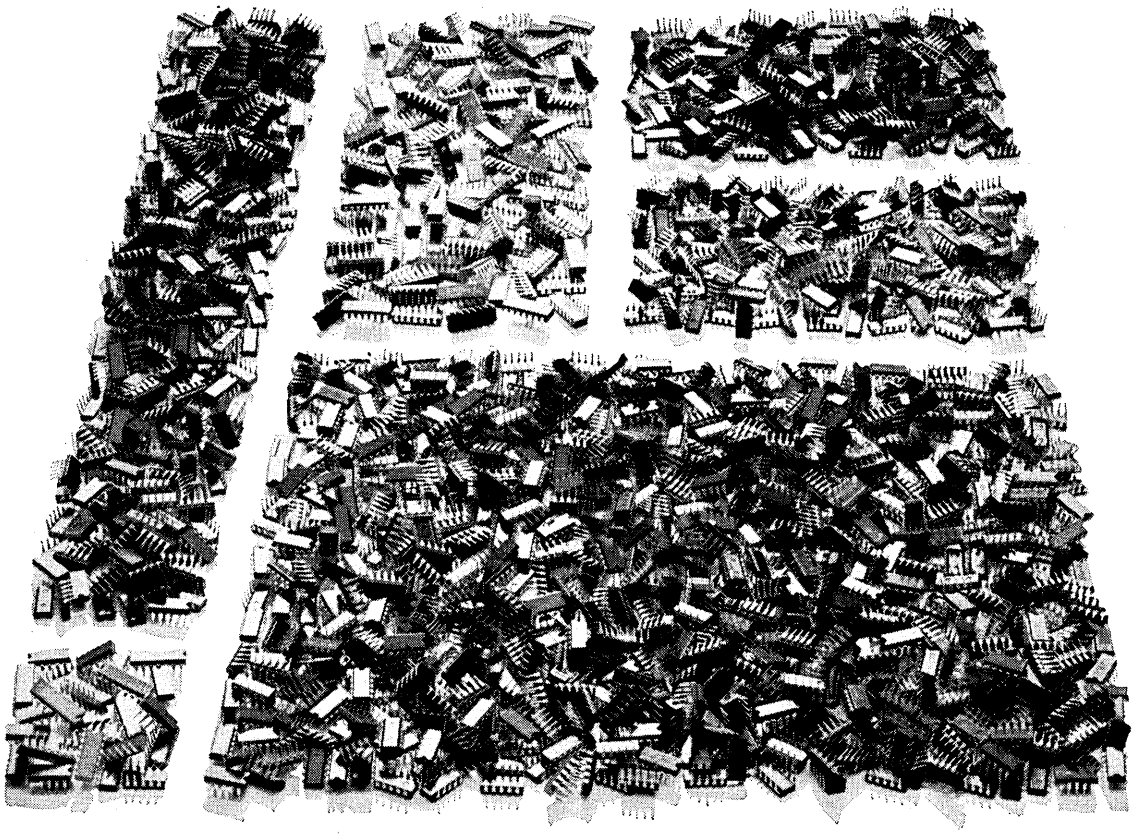
Tel. 369-6660

BPA Circulation over 42,000

FEATURES

DEPARTMENTS

Fairchild told everyone what MSI could do.

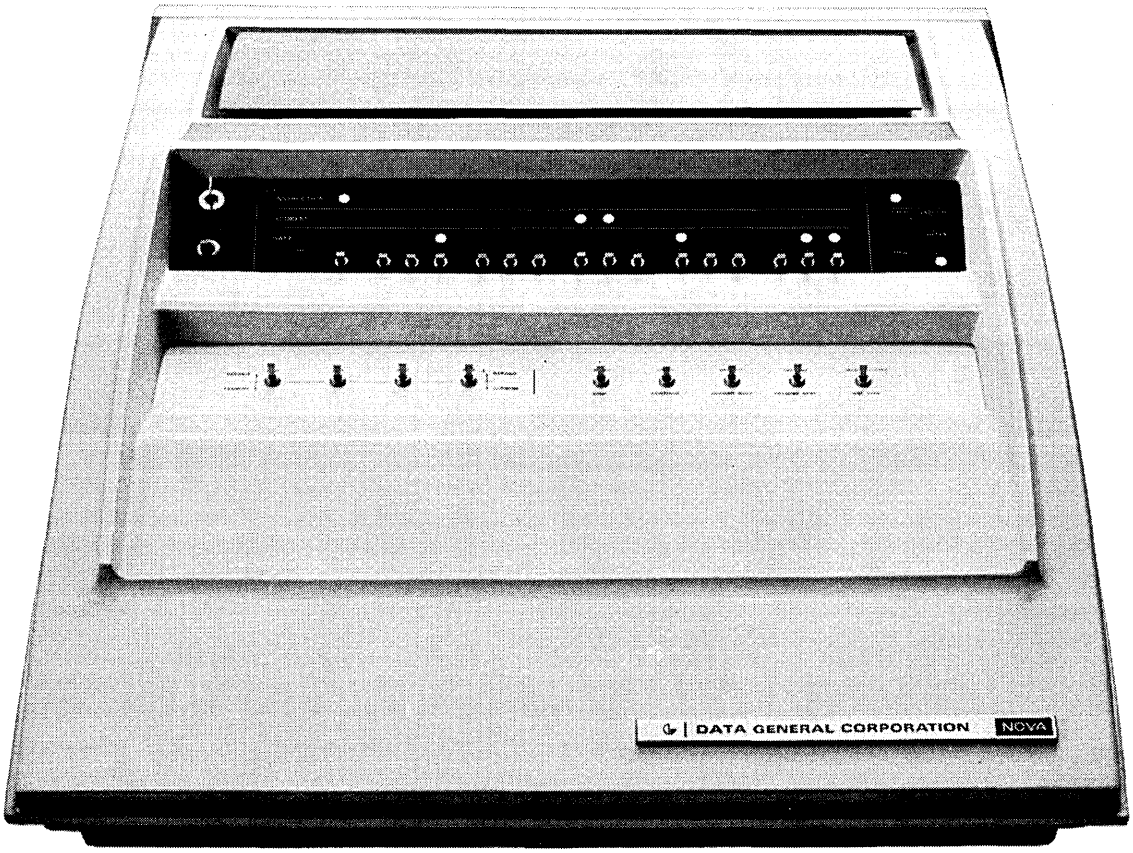


Ever since we introduced medium scale integration in 1967, we've been talking about the systems approach to computer design. Basic, compatible fundamental building blocks that do more jobs than a hundred Integrated Circuits.

Versatile circuits that function like shift registers, counters, decoders, latching circuits, storage elements, comparators, function generators, etc. We said we had enough MSI device types to build more than half of any digital system you could design. An imaginative company in Boston took us up on it.

CIRCLE NO. 4 ON INQUIRY CARD

We're glad someone was listening.



Data General Corporation built a revolutionary computer with Fairchild MSI circuits. The building block approach allowed them to design and build the whole system in six months. And put it in either a desk top console (shown above) or a 5¼-inch high standard 19-inch rack mount package. The central processor fits on two 15-inch by 15-inch plug-in circuit boards.

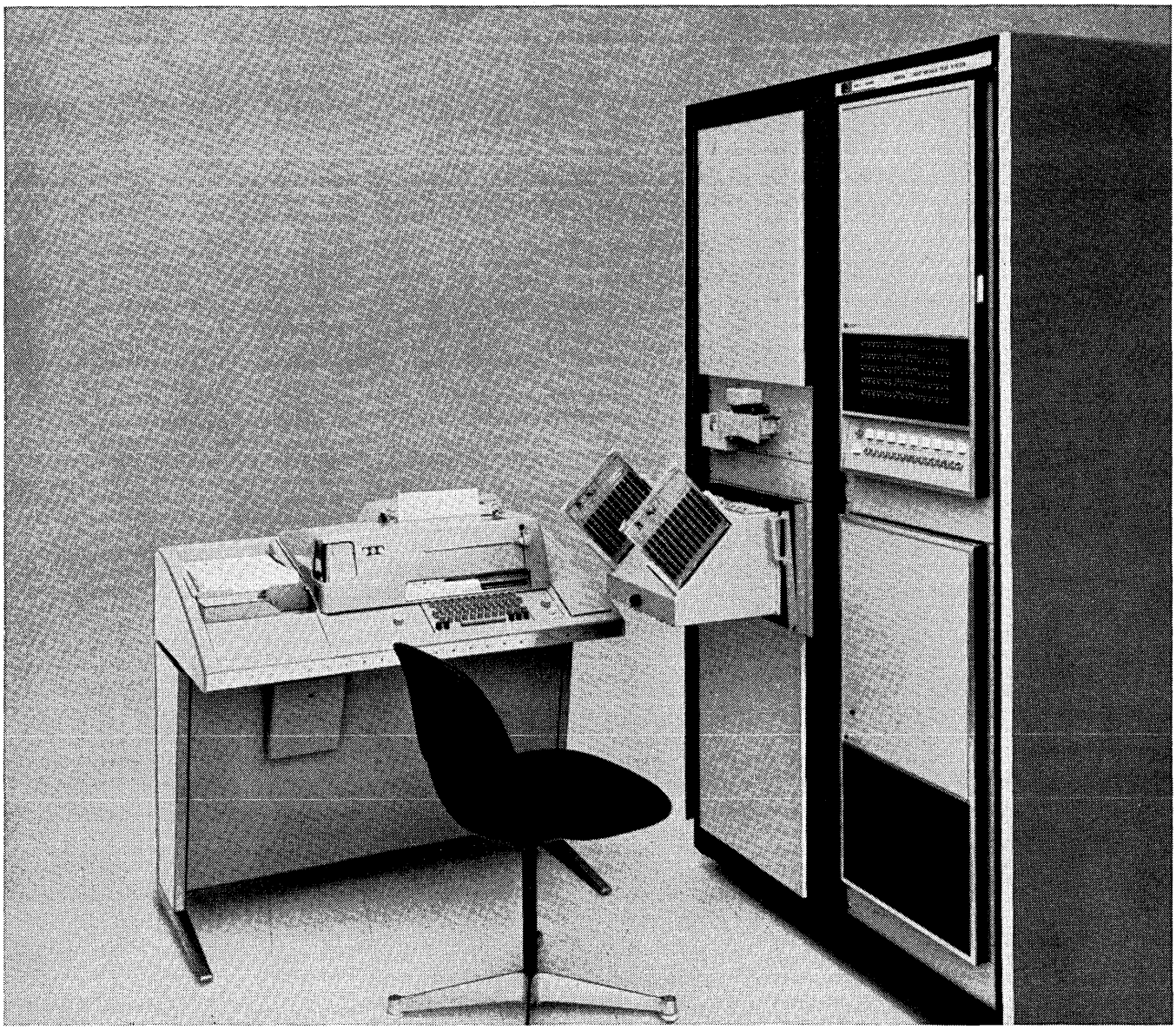
Another board houses a 4,096-word core memory. A fourth board provides enough space for eight I/O devices. And there's still enough room left for boards that expand the memory capability up to 16K. Any circuit board can be changed in seconds, so the computer has zero down time. The NOVA is the world's first computer built around medium scale integration. The first general-purpose computer with multi-accumulator/index register organization. The first with a read-only memory you can program like core. The first low-cost computer that allows you to expand memory or build interfaces within the basic configuration. And the first to prove the price/performance economy of MSI circuitry: The NOVA 16-bit, 4K word memory computer with Teletype interface costs less than $8,000.

If you'd like more information on MSI, use the reader service number on the opposite page. For specs on the NOVA, use the reader service number below.

FAIRCHILD
SEMICONDUCTOR

FAIRCHILD SEMICONDUCTOR / A Division of Fairchild Camera and Instrument Corporation ■ 313 Fairchild Drive, Mountain View, California 94040, (415) 962-5011 ■ TWX: 910-379-6435

CIRCLE NO. 5 ON INQUIRY CARD



Logical Tester

Got a bottleneck testing digital logic modules? Are delivery dates slipping and circuit tests costing more? Here's the logical solution.

Hewlett-Packard has developed the 2060A Logic Module Tester. It quickly and efficiently tests digital modules, simple or complex, in a matter of seconds instead of hours. From 16 to 256 pins per module can be handled — at 10,000 tests/second/pin. That's two and a half *million* tests per second, which figures out to less than a dollar per module. And it tests all logic types: DTL, TTL, CTL, RTL— even different types mixed in a single module.

The key to this system is simplicity. It compares modules against a reference module known to be good and gives you a printout of nonmatching areas, right down to the specific test and pin numbers that failed. Test technicians learn to program the 2060A quickly and easily with a new, test-oriented language. No special knowledge is needed to run the system, so production people are expert operators within minutes. At $80,000 this system makes economic sense. Fast, 100% testing is definitely better business than slow, partial checking by manual methods.

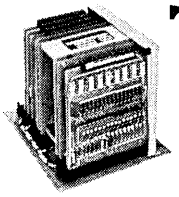
Call your local HP field engineer for details. Or write Hewlett-Packard, Palo Alto, California 94304; Europe: 1217 Meyrin-Geneva, Switzerland.

HEWLETT hp PACKARD

06830

CIRCLE NO. 6 ON INQUIRY CARD

The case for our micromemory.



There is none.

Most memories available today come in nice packages. Totally-enclosed, well-protected, and looking like they still belong to the original manufacturer.

We've got one that doesn't look like it belongs to anyone. Our newest system for industrial/commercial applications, the MICROMEMORY™ 1000, provides up to 32K bits of storage with a cycle time of 2.5 usec for less than 7 cents/bit. And it's just as economical with space (400 cubic inches) and power (35 watts maximum).

But it has no case. The system consists of a stack and five cards of electronics that plug into an unenclosed mother board, with a single connector providing the I/O interface for integration into your system. Maintainability is enhanced by this configuration even though you'll probably never have to take advantage of it. The same advanced 3D drive technique that gives you the lower price because of a lower component count also yields a correspondingly higher MTBF.

The MICROMEMORY 1000 will fit almost anyplace in your system. Its open construction leaves access unhampered, while its low power dissipation eliminates the need for additional cooling. Mount it upside down or sideways, show it off or hide it. It looks like it belongs in your system because it does.

Price and delivery, true random access and ease of electrical interface all strengthen the case for the MICROMEMORY 1000. Write us for the full story.

EM electronic memories

12621 Chadron Ave., Hawthorne, California 90250 • (213) 772-5201

CIRCLE NO. 7 ON INQUIRY CARD

SPC-12
the new automation computer

The SPC-12 is a new automation computer designed for economical use in dedicated automation and control functions.

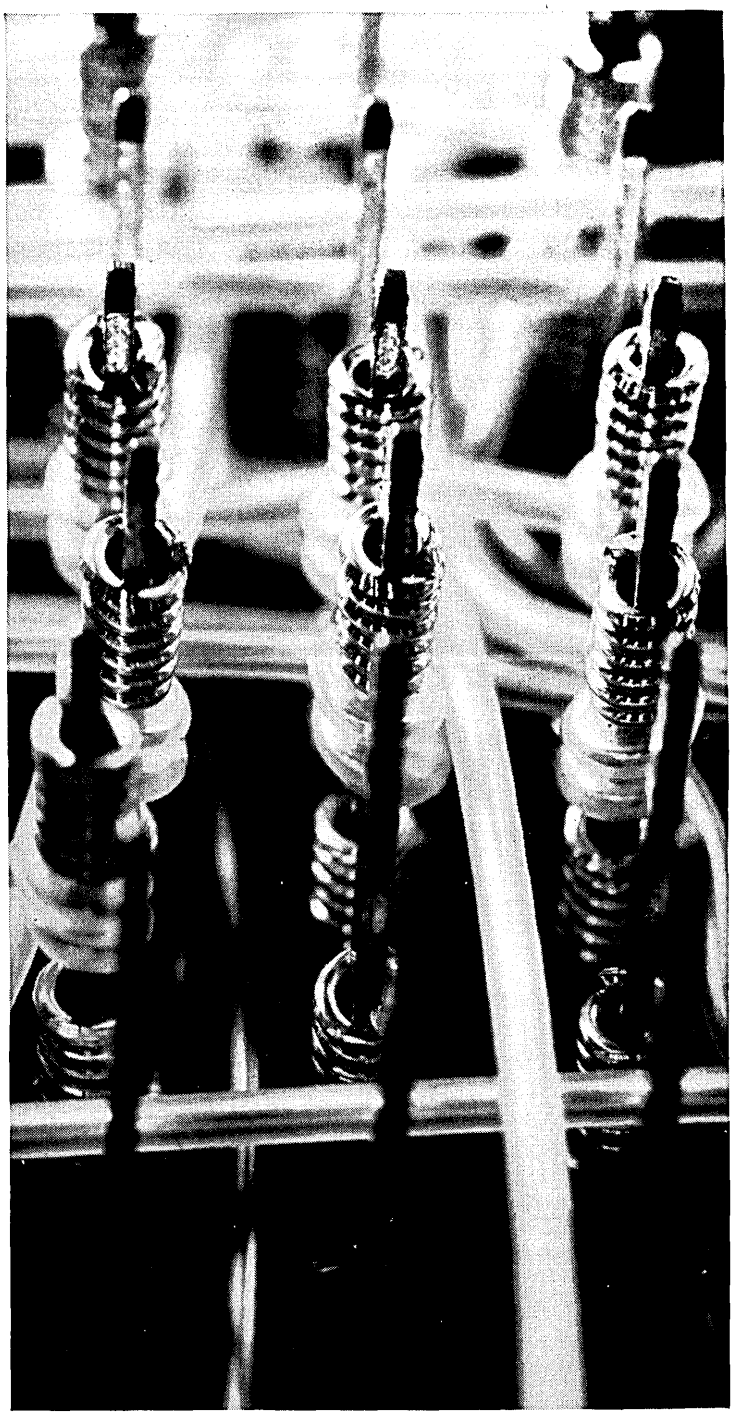
The SPC-12 is powerful—with six programmable 12-bit registers, a 2-microsecond (4K to 16K) memory of 8-bit bytes, and a unique memory saving "shared command" concept. Fully IC'd for reliable 'round-the-clock' operation. $6400, *including* a teletypewriter interface, control panel, and real time clock, console lock, optional power failure restart, and optional direct memory transfer.

That's just half the story. Most computers require expensive engineering and black boxes to work in a control system. Not the SPC-12. It comes with economical functional modules which adapt the SPC-12 easily to instrumentation, computer peripherals, keyboards and displays, sensors and communication networks. With these functional modules and its power, the SPC-12 achieves a new cost/performance ratio and makes computer control practical in your system today. Programming aids and application software of course. Call or write for more information about the SPC-12—the new automation computer.

GENERAL AUTOMATION, INC.
Automation Products Division
706 West Katella, Orange, Calif. (714) 633-1091

CIRCLE NO. 8 ON INQUIRY CARD

We know somebody with connections.



So we told them about wire insulation made of Kynar®

That was five years ago.

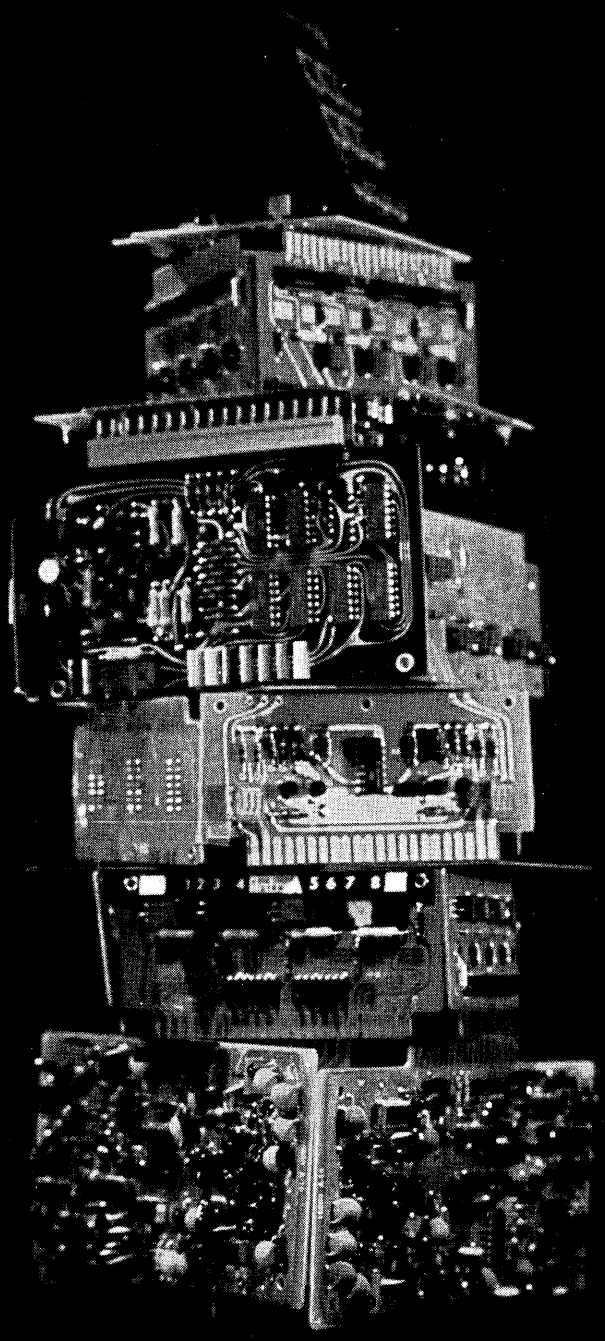
Burroughs Corporation's computer plant in Pasadena runs 200,000 feet of wire a week, makes 120 terminations per minute. With that many connections, at that speed, the right kind of insulation is important—insulation that's not only tough, but absolutely reliable. That's why Burroughs has used wire insulated with Kynar for back planes since 1963.

Why Kynar? A Burroughs engineer answers: "It works better than many others we've tried . . . so why argue with success?" Kynar works for some good solid reasons. It has twice the cut-through resistance of other common fluoroplastics and virtually eliminates cold-flow problems. Kynar runs economically in automatic wire-wrap equipment . . . it feeds, cuts, and strips smoothly. It's unaffected by cleaning solvents, and it won't degrade with age.

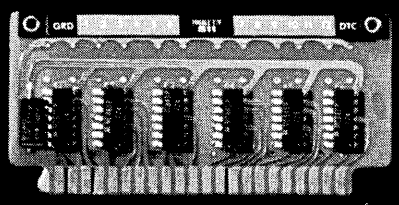
Tough arguments? You bet. Tough material . . . that's Kynar. So take a tip from experience. Switch to wire insulated with Kynar. It's available from leading wire manufacturers. For additional information contact: Plastics Department, Pennsalt Chemicals Corporation, 3 Penn Center, Philadelphia, Pa. 19102.

Kynar...the fluoroplastic that's tough! PENNSALT®

CIRCLE NO. 9 ON INQUIRY CARD



Now... in cost too we stand alone



And we can prove it. With our new, lower prices, you don't have to sacrifice quality for price any longer. Phone or write...

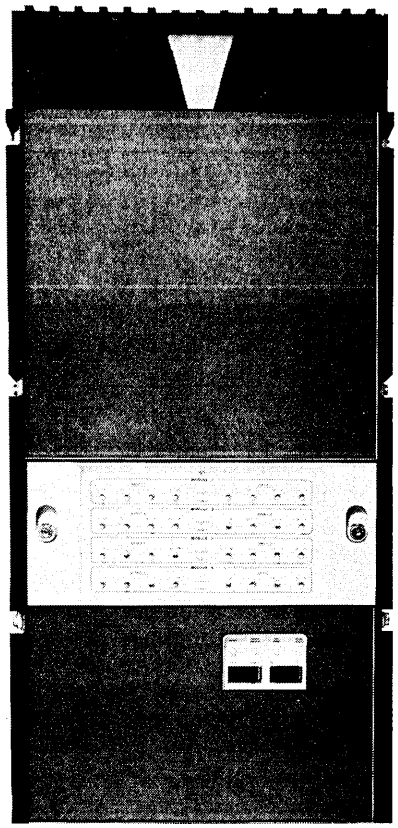
DATA TECHNOLOGY CORPORATION

1050 East Meadow Circle
Palo Alto, California 94303
Tel: (415) 321-0551

Peripheral quiz
for computer manufacturers

How many bits of head-per-track fast access disc memory in this sleek, compact matched companion for your computer?

☐ *25 Million* ☐ *50 Million*
☐ *75 Million* ☐ *100 Million*
☐ *125 Million* ☐ *150 Million*
☐ *175 Million* ☐ *200 Million*



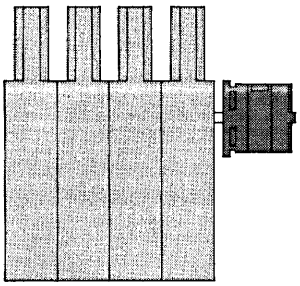
40" high, 24" deep to mount in your 19" rack. Decorator Colors to match your computer.

All 8 answers are correct:
Reason? The new CPC model DSU-8100 is a truly modular fast access disc memory system. It's designed for today's sophisticated computers. Ideal for real time response, program swapping, and message switching.

Four Sealed Disc Modules to Choose From

Fast access modules with individual heads for each track can locate data in 16.7 ms average. Available with 25 million or 50 million bits. In the two economy modules each head services 4 data tracks with positioning time of only 25 ms.

One Drive Serves Up to Four Modules



Because from one to four CPC memory modules are served by the single drive, 25 million to 200 million bits of ultra-reliable disc memory fit comfortably in the compact chassis designed for slide-mounting in your 19-inch console. Field expandable to billions of bits.

Fail Safe Protection
No head avalanche possible here. Modules are ultrasonically cleaned, clean-room inspected, then sealed. The flying heads never touch the recording surface and automatically retract if motor speed, internal voltages, or air pressure vary. Tamper-proof lockouts protect your data too.

Small Size... Low Cost
A unique recording system with higher packing densities plus T²L integrated circuit logic means small size, light weight, and low power. Standard "off the shelf" modules reduce inventory and make it possible for computer manufacturers to quickly supply the right amount of memory for every job.
A full system with logic level interface sells at less than 1/10th of a penny per bit. Contact Dick Baker, V.P. Marketing, for more information.

computer peripherals corp.
5037 Ruffner St., San Diego, Calif. 92111, (714) 279-7500

CIRCLE NO. 11 ON INQUIRY CARD

← CIRCLE NO. 10 ON INQUIRY CARD

Mag tape too expensive?
Punched tape too slow?
Your small computer deserves PEC data power!

High Speed—Low Price

Seems a shame to shackle that fast new computer of yours with slow, maintenance-prone punched tape. Yet digital magnetic tape recorders are so expensive.

Not now, they aren't.

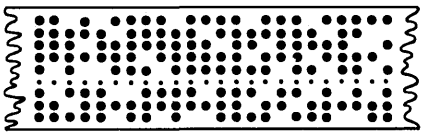
PEC can give your small computer real write/read data power. 10 KHz data transfer rates for under $3,000. 20 KHz transfer rates from $5,000. (Less than $4,000 in quantities).

Discriminating computer users are demanding higher input/output performance on even the smallest machines.

That's why more and more major computer manufacturers are offering PEC digital magnetic tape recorders as standard equipment.

Insist on low cost-high performance PEC data power for your computer.

Compare With Punched Tape



You can store ten characters on an inch of punched tape. You can store up to 800 characters on an inch of magnetic tape. That's 80 times more data per inch!

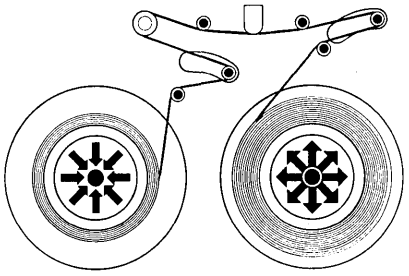
What about data transfer rates? A paper tape perforator plods along at 150 characters a second. Pretty slow for today's fast computers.

PEC digital magnetic tape recorders zip data in and out at speeds to 25 ips. Data transfer rates up to 20 KHz. That's 133 times faster than punched tape.

PEC data power costs just a little more than punched tape. Yet look at the tremendous increase in storage capacity and data transfer rates you get.

Compare With Other Mag Tape Models

PEC digital magnetic tape recorders use an elegantly simple single capstan velocity servo system. Pinch roller, a major source of skew and tape wear, is eliminated.



PEC recorders cost half as much as competitive makes, yet perform even better.

IBM compatible? You bet. Including the precise requirements for System/360, 9 channel, 800 bpi operation.

Choose the speed you want from 4 to 25 ips, at 800, 556, or 200 bpi. 7 track dual density available too. And up to 4 PEC recorders can operate from a single computer.

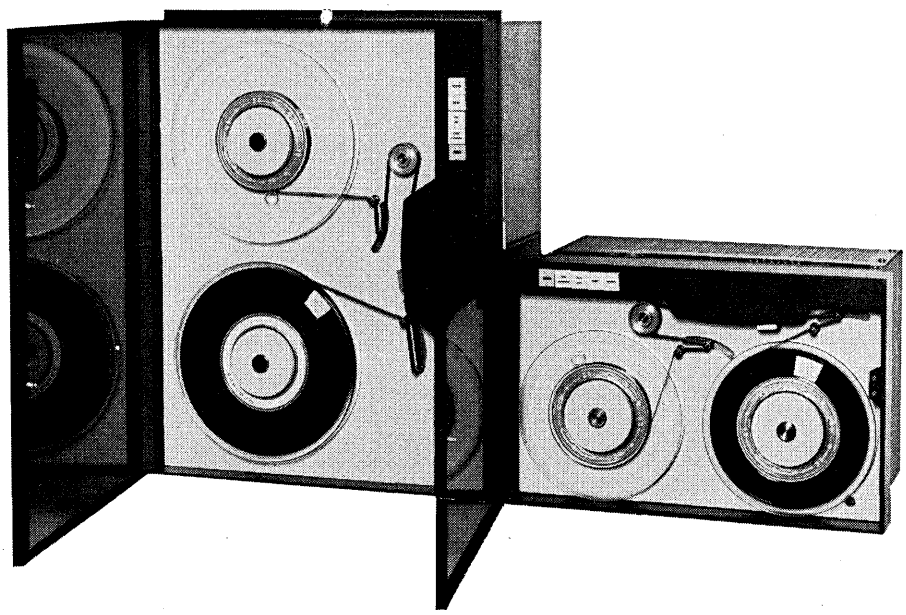
Select the data capacity, transfer rate, rack height and price from 3 distinct models.

Three Reel Sizes

Reel Size	Max. Transfer Rates	Tape capacity
7 inch	10 KHz	600 feet
8½ inch	20 KHz	1200 feet
10½ inch	20 KHz	2400 feet

PEC also makes synchronous write-only and read-only recorders. A complete line of incremental models too. Perfect for data acquisition systems, off-line plotters, line printers, and data terminals. Perfect for just about any input or output requirement, for that matter.

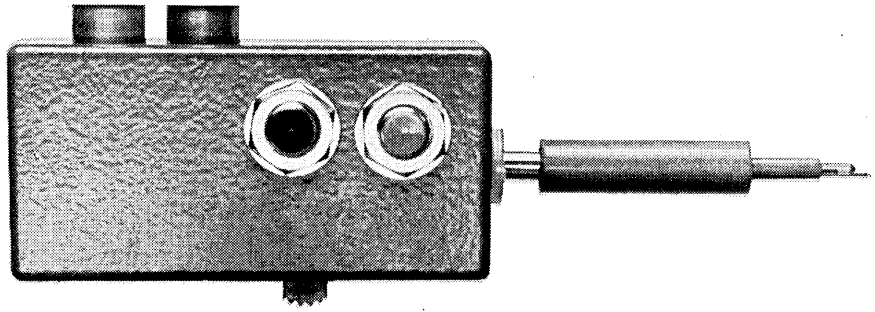
Write or phone today for our 8 page brochure.



PEC

PERIPHERAL EQUIPMENT CORPORATION
9551 Irondale Avenue ■ Chatsworth, California 91311 ■ (213) 882-0030 ■ TWX (910) 494-2093
CIRCLE NO. 12 ON INQUIRY CARD

SCOPE SAVER



DIGI-PROBE*

New Test Probe Replaces Expensive Oscilloscopes For Simple Production Tests on Digital Circuits

This little test probe is a real money saver on the production line. Performs most checks on digital circuits now being done with costly oscilloscopes. Simple-to-interpret red/green indicator lights determine presence and polarity of pulses as fast as 25 ns. Speeds testing and debugging. Reduces skill level of testers. Send for our brochure describing how the Digi-Probe works to save you time and money.

*Trademark, Pat. Pend.

Available from stock $89.

PULSE MONITORS, INC.
351 New Albany Road
Moorestown, N.J. 08057
(609) 234-0556
A SUBSIDIARY OF
TELEPRODUCTS, INC.

CIRCLE NO. 13 ON INQUIRY CARD

A new Ampex computer tape drive for $3500.* Wow!

The new Ampex TM-Z is a complete computer-class tape memory system (including read/write electronics) that best fulfills the need for a low-cost, high performance, low speed unit for your computer, data terminal or data acquisition system. Completely computer-compatible, it conforms to all requirements of IBM and ASCII 7- and 9-track formats.

Simplicity of design results in the utmost in reliability and easy maintenance. This completely new, ready-to-plug-in tape memory system features the same precision as the higher speed Ampex TM-7 and TM-16 tape memories.

PERFORMANCE CHARACTERISTICS

Tape Speeds:
Standard speed is 24 inches per second, Read/Write (19.2 kHz transfer rate at 800 cpi). Any single tape speed between 10 and 24 ips can be obtained by utilizing a continuously variable adjustment.

Tape Width and Thickness:
½-inch width, 1.5 mil by 2400 feet (732 meters)

Recording Density:
Standard: 556 and 800 cpi. Optional densities available.

Recording Formats:
Standard: 9-track ASCII 0.6 inch IRIG (IBM 360, 2400 Series compatible).
Optional: 7-track, NRZ 0.75 inch IRIG (IBM 7330, 729 Series compatible).

Start/Stop:
Tolerances permit bilateral interchange of tapes with equipment compatible with IBM and ASCII 9-track standards.

Input Voltage and Frequency:
Voltage: 100-250 volts RMS with transformer taps.
Frequency: 48 to 63 Hz.
Consumption: Average, 400 watts. Peak, 500 watts.

Interface Characteristics, Data and Control Lines:
True: Logic "1" = 0.2 (−0.2 + 0.2 volts)
False: Logic "0" = + 3.3 (− 0.9 + 1.7 volts)
Logic: TTL units employed

Dimensions:
Complete tape memory system, including self-contained data electronics, can be mounted in a standard 19" or 24" rack.
Height: 24"
Width: 19" or 24"
Depth: 17" overall (14½" rack depth)

Weight:
100 lbs. maximum

Functional Modes (selective):
1. Write Forward, Read Forward
2. Read Only Forward
3. Read Only Reverse

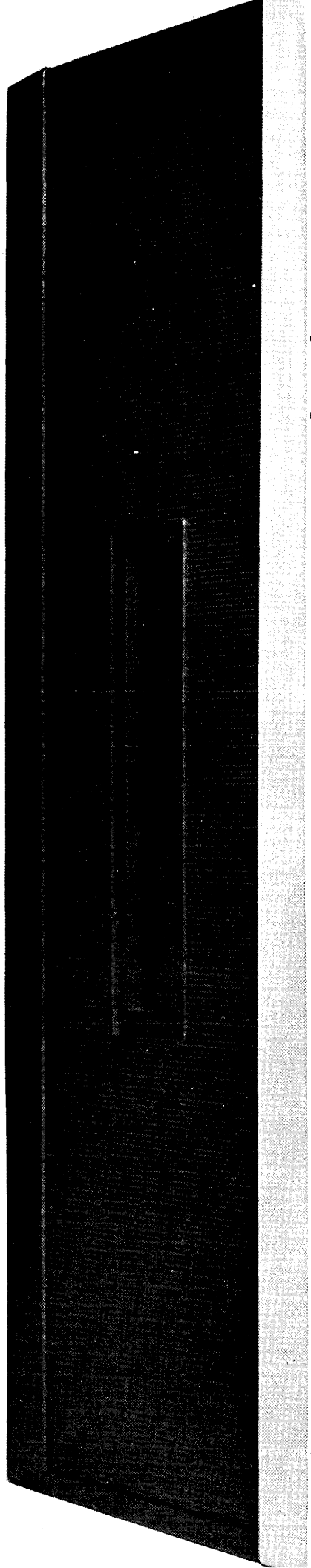
Options:
1. Vertical Parity Check
2. Vertical Parity Generate
3. Write Echo Check
4. Longitudinal Parity Check
5. Longitudinal Parity Generate

For complete technical information on the TM-Z, write: Ampex Corporation, 401 Broadway, Redwood City, California 94063.

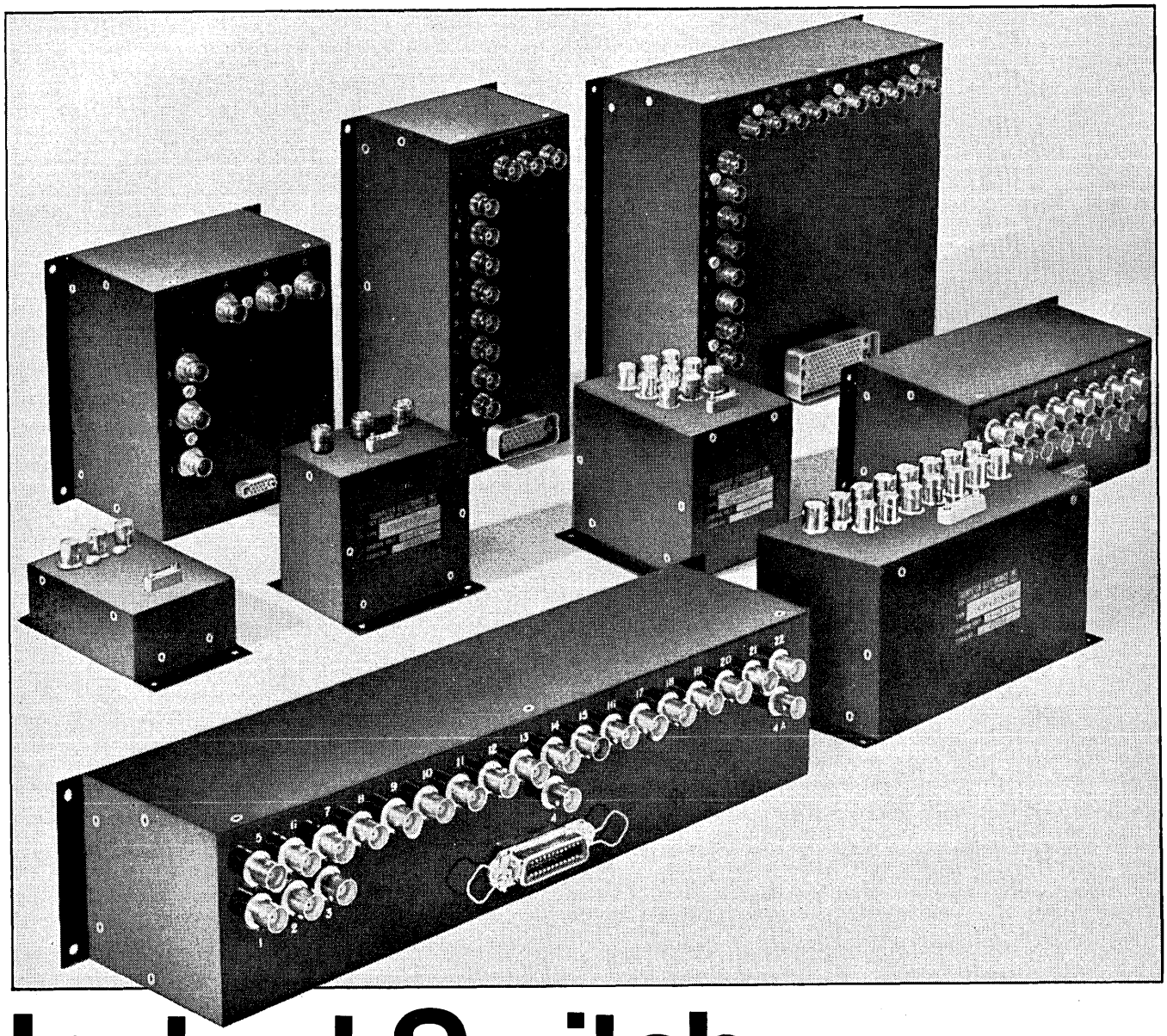
AMPEX

CIRCLE NO. 14 ON INQUIRY CARD

*Price including all read/write and control electronics, in lots of 100 per year.



REVERSE
FORWARD
FILE PROTECT
REMOTE



Instant Switch...Just plug in and start switching ...We don't give you a handful of parts to strap together! Trompeter Matrices and Switches come to you as a completely assembled system that has been carefully tested to meet your specifications. Available in twinax or coax configurations, they are pre-programmable, electrically activated systems configured as cross point matrices (crossbar), featuring low cross talk, high isolation, hermetically sealed contacts, fast activation time, excellent high frequency and pulse responses and excellent electro-magnetic shielding. As video data and switching matrices, systems are available in either X,Y plane, or X,Y,Z and multi-level formats with isolation up to 110db at 60MHz.

Switches are available in multi-pole, multi-throw formats up to 20 poles, 20 throws in both coax and twinax.

Now, if you still want to use the modular approach...Okay! We have a building block matrix system also available that helps to eliminate a lot of the usual fuss and high cost of assembling such a system. And incidentally, we'll even take on the system's responsibility!...Ask for our new catalogue M-5.

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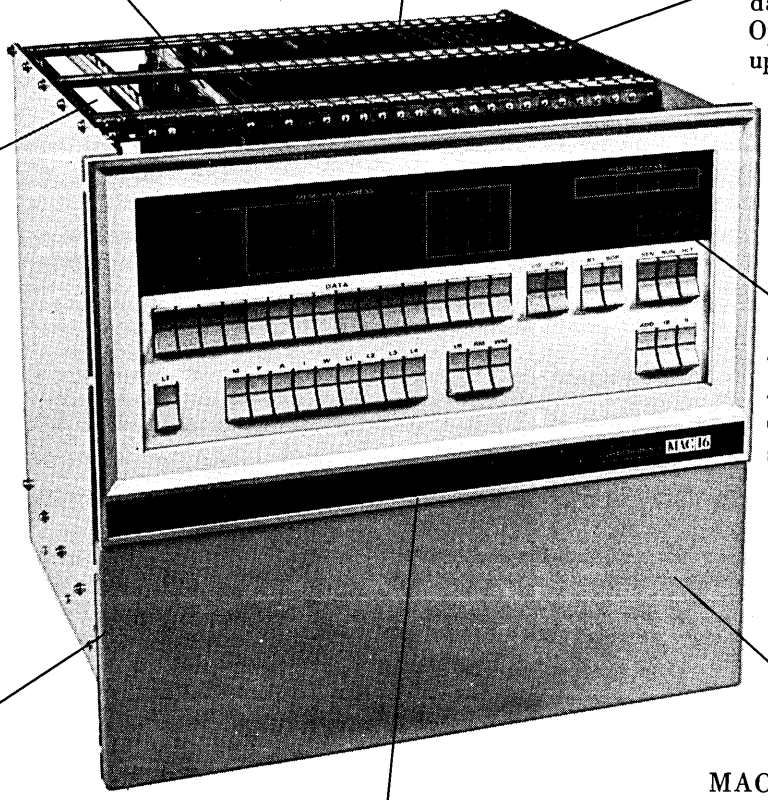
CIRCLE NO. 15 ON INQUIRY CARD

MAC is a good deal of computer.

1-μsec memory cycle time. 16-bit parellel word, 2-μsec add time. 4K words standard.

72 instructions including: byte handling, 3-way nondestruct compare, test and skip up to 15 instructions, fast shifts, and optional multiply/divide.

Three data channels: Programmed data channel, up to 90KHz. Optional multiplexed data channel up to 333KHz. Optional direct-memory-access up to 800 KHz.



Expansion to 8K words in mainframe. Up to 65K available.

True-nested priority interrupts: 4 levels standard. Expansion to 64 levels. Automatic register save-and-restore, 6-μsec response.

Third-generation software: LEAP, a two-pass, macro-handling assembler, linking relocatable loader with automatic depaging, debug and edit programs, utility routines, I/O drivers, and diagnostics. LEAP-FORT and MACSIM: Program assembly and simulation on big computers. USASA Standard FORTRAN IV with math library.

MAC 16, with 4K memory, ASR 33, 4 priority interrupts. Ready to operate.....$11,950.

Mainframe space for options. Swing-out front panel, relocatable to remote position. Control-panel programmer aids.

Let MAC do it.

For technical data, write: MAC, Lockheed Electronics Company, Data Products Division, 6201 East Randolph Street, Los Angeles, California 90022.

CIRCLE NO. 16 ON INQUIRY CARD

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If you're building any computer except a Computer, you need CTμL.

CTμL integrated circuits will give you more speed for less money than any other ICs. They're perfect for process control systems, test instrumentation, central processing units, computer peripheral equipment—just about anything short of an airborne computer.

Keep it in the family.

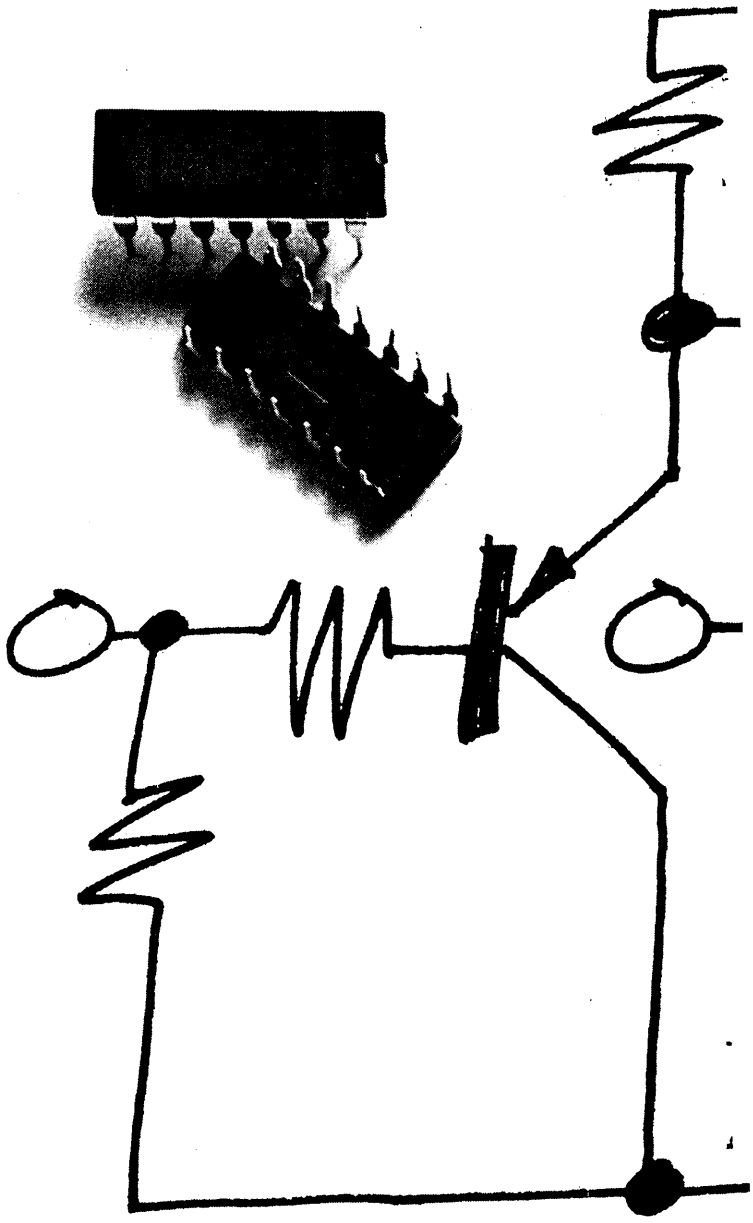
You can build a complete digital logic system with Fairchild's family of CTμL devices. We have gates, flip-flops, inverters and memory circuits. A dozen different devices that make a computer easy to package. And, you'll need only about 80 percent as many packages as required with TTL.

You get out of it what you put into it.

The key CTμL characteristic is non-saturating logic. That means you get fast gate propagation delay (typically 3nsec) with slow rise and fall times (typically 6nsec). So, there's no need for transmission lines or complex packaging. You can build an entire computer with normal two-sided circuit boards. Also, CTμL can handle signal swings as large as 3V. It also provides typical noise immunity of 500mV.

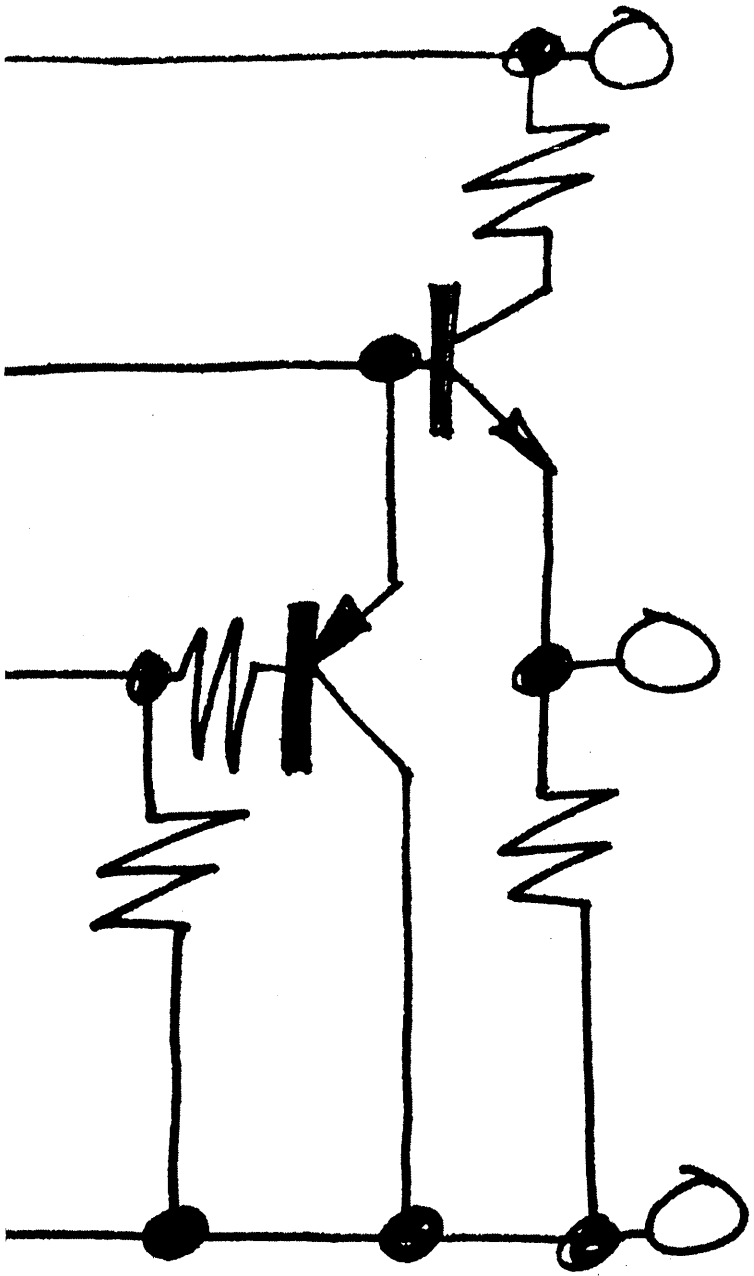
What we'll do for an encore:

MSI CTμL will be out before the year ends. CTμL-II will be out even sooner, offering improvements like gate propagation delay of 1.5nsec. (typical, loaded) and a buffer and



The world's largest manufacturer

inverter with propagation delays of 5nsec, compared with 12nsec in standard CTμL. And, the new MSI and CTμL-II circuitry will interface beautifully with all these standard CTμL devices:



Device	Price (100-999)
9952 Dual NOR Gate	$1.25
9953 Triple AND Gate	1.25
9954 Dual Four-input AND Gate	1.25
9955 Eight-input AND Gate	1.25
9956 Dual Buffer	1.25
9957 Dual-rank Flip-flop	2.00
9964 Dual Three-input and Single-input AND Gates	1.25
9965 Quad Single-input AND Gate	1.25
9966 Quad Two-input AND Gates, one pair with OR-tie	1.25
9967 JK Flip-flop	2.00
9968 Dual Latch	2.00
9971 Quad Two-input AND Gates with OR-tied pairs	1.25
9972 Quad Two-input AND Gates, one pair with OR-tie	1.25

If you want CTμL-II in sample quantities, call Fairchild. If you want standard CTμL in production quantities, call a Fairchild distributor. He has everything you need to build any computer.
Even a Computer.

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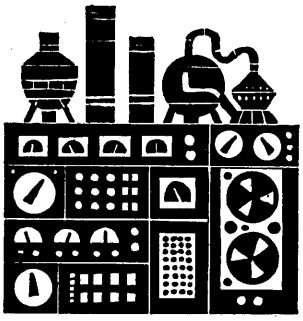
Fairchild Semiconductor/A Division of Fairchild Camera and Instrument Corporation/313 Fairchild Drive, Mountain View, Calif. 94040 (415) 962-5011/TWX: 910-379-6435

# of LSI admits there's another way:

CIRCLE NO. 17 ON INQUIRY CARD



INDUSTRY NEWS

IEEE ANNOUNCES TWO COMPUTER COURSES FOR EE'S—The IEEE has announced two new 2-day tutorial courses for the practicing electrical engineer who would like to use digital computer programs as an aid in solving day-to-day problems, or who would benefit from knowing how to use time shared computers to solve practical electrical engineering problems. The courses were developed for the Institute by Oyer Professional Computer Services, New York, N. Y. subsidiary of Computer Age Industries, Inc.

"Computer Programming For Electrical Engineers" is intended to equip attendees with the knowledge to begin to write some of their own programs and the ability to discuss programming problems knowledgeably with experienced programmers.

"Problem Solving For Electrical Engineers Using Time Shared Computers" will consist of lectures on how to use time shared computers to best advantage in solving practical electrical engineering problems. This course is intended to equip attendees with the knowledge to begin to solve some of their own problems through "conversation" with a time shared computer system.

Both courses are being offered in conjunction with several IEEE Conferences; January 23 & 24, following Reliability Symposium; February 14 & 15, following AES Wincon; March 27 & 28, following IEEE International Convention; April 24 & 25, following SWIEECO; and, Tentatively, April 17 & 18, following INTERMAG (Holland).

Full information about the courses and registration for members and nonmembers can be obtained by writing Education Registrar, IEEE, 345 East 47th Street, New York, N. Y. 10017.

AUTOMATIC COMMUNICATIONS SYSTEM CONTRACT AWARDED—Burroughs Corp., Detroit, Mich. has been awarded a contract by the Army Electronics Command, Fort Monmouth, N. J., to build a Tactical Automatic Digital Switching System (TADSS).

TADSS will provide the Army with an automatic communications system which will receive incoming tactical field data and redistribute it on a real-time, priority basis to various field commanders.

Included in the data will be the status of enemy troops and weapons and other intelligence, logistical, operational and administrative information.

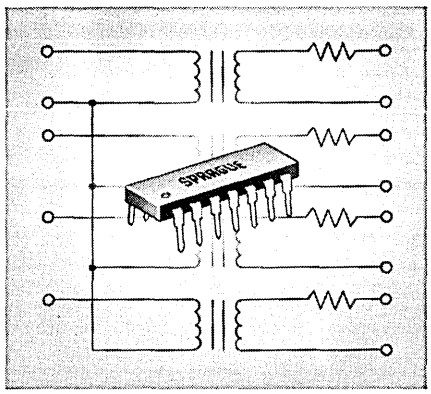
The initial contract calls for two mobile message switching centers, each comprised of six vans containing computers, communications, and technical support equipment. The heart of each center, two Burroughs B3500 computers, will be housed in two of the vans along with their associated disk file memory, magnetic tape and other peripheral equipment modified to meet the Army's rugged tactical requirements. The information flows to and from the system over 48 fully duplexed communications lines at the rate of over 300,000 characters per minute.

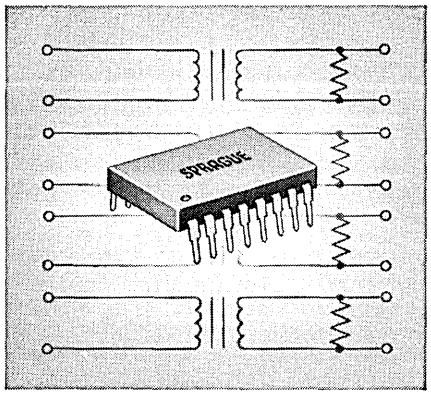
The contract contains an option for three additional switching centers, bringing the total potential under the present contract to $11-million. Overseas shipments of the first TADSS message switching center to the United States Seventh Army, West Germany, is scheduled for December 1969.

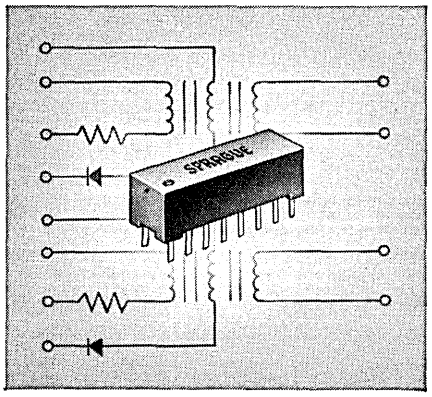
FCC CHIEF SEEKS USERS GROUP REACTION TO CARTERFONE RULING—At the Third Annual Meeting of the Digitronics Users Association in New Orleans last week, Kelley E. Griffith, Chief of the FCC Domestic Rates Bureau expressed the Commission's desire to hear all interested parties, especially users, with respect to recent AT&T tariff filings. The new filings were made subsequent to the FCC's ruling in the Carterfone case against AT&T restriction of equipment to be used on telephone lines. Griffith noted that in making its Carterfone decision on September 13, 1968, the Commission removed some long standing prohibitions (in effect since 1899) in the Bell Systems tariffs. These restrictions prohibiting customer-provided devices and systems from being connected into the telephone network, acted to eliminate harmless, as well as harmful devices. The FCC holds that AT&T must allow users to connect any device to their lines that will be beneficial to the user providing it does not interfere with the telephone network itself or another user's activity within the system.

Mr. Griffith told the users that the Commission was anxious to hear from anyone who has something to say on the subject and would accept informal as well as formal pleadings. One of the major tasks of the Commission now is to determine whether or not the new tariff filing, scheduled to go into effect Jan. 1,1969, complies with the recent Carterfone ruling.

MODULINE® Memory-drive Hybrid Circuit Modules combine miniaturized inductive elements with thick-film ceramic-based technology.







You get pulse transformers and resistors (diodes and capacitors can also be included) in a circuit tailored to your specifications.

A single module may contain up to four identical circuits. They're particularly useful in memory systems where a similar repetitive pattern exists.

Flexibility offered by modular concept simplifies specific designs.

3 package styles: standard dual in-line, jumbo dual in-line, molded case with pin leads. They're all compatible with conventional in-line circuit layout.

High component density permits substantial size and cost reduction.

For complete technical data, write for Engineering Bulletin 22210 to: Technical Literature Service, Sprague Electric Co., 555 Marshall St., North Adams, Mass. 01247.

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CIRCLE NO. 18 ON INQUIRY CARD

INDUSTRY NEWS

ANOTHER REACTION TO AT&T's TARIFF—In a joint petition filed with the FCC, Photo Magnetic Systems, Inc. and its wholly owned subsidiary, Computer Telephone Corporation, said that AT&T's proposed tariff schedule could result in "less service available to the public for more money to the telephone company."

The Maryland based manufacturer of the patented "Comput-A-Phone" Touch-Tone telephone time-sharing system, told the FCC that AT&T's action "seeks by artful, misleading and cleverly contrived language in its proposed revised tariff to retain the same or even stronger controls over so-called foreign attachments' (customer-provided equipment)"—in direct contradiction of the FCC's Carterfone decision prohibiting unreasonable AT&T imposed tariffs on harmless interconnecting equipment produced and sold by independent companies.

"Under the guise of protection of its telecommunications network," the petitioners said "AT&T has proposed elaborate regulations . . . to set standards for the use of customer-provided data transmitting and/or receiving terminal equipment," and that the data access arrangement which AT&T has proposed "is only a cleverly contrived method of requiring, in most instances, the leasing of a Data-Phone from the Telephone Company, at increased and unnecessary cost to the user."

In addition, the petitioners said that AT&T's new "protective connecting arrangement, proposed to be tariffed as equipment, with installation and monthly rental charges to be made by the Telephone Company" could be easily built into the independent manufacturers equipment "at little cost and with no installation charge or recurrent rental required."

The petitioners said that certain data equipment changes made by AT&T are "done in the name of progress and improved service, but the results of the changes involved are presently available through cheaper AT&T products and services."

LARGE SCALE INTEGRATION TEXT PUBLISHED—Availability of a 105-page text on LSI has been announced by Integrated Circuit Engineering Corporation, Phoenix, Ariz. The publication, written primarily for engineering and management personnel involved in state-of-the-art product development, summarizes the status of LSI. It evaluates the impact of this technology and presents its advantages and limitations in proper perspective.

In addition to analyzing the effect of LSI on the electronic industry, the report reviews LSI design and processing techniques, cost factors, reliability and future applications and techniques. Both MOS and bipolar approaches to LSI are investigated and their systems design and applications explored. Silicon wafer processing for each configuration is summarized and the problem of interconnections is reviewed.

Other topics covered include: special packaging problems and pin limitations, power considerations, cooling and canning requirements, multilevel metalization, discretionary wiring, system partitioning, complementary and four-phase MOS design, yield projections, cost comparisons, system reliability, maintenance and repair, silicon on sapphire techniques, projection printing, as well as novel application techniques.

The text is priced at $75 per copy and is available from Integrated Circuit Engineering Corporation, 4900 East Indian School Road, Phoenix, Ariz. 85018. Contact David B. Kret, Manager of Publications.

WESTERN UNION INAUGURATES 'INFO-COM'—INFO-COM, Western Union's new nationwide shared-use communication network for business firms, has gone into operation with inauguration of service for Montgomery Ward, giant merchandising company and the first INFO-COM customer. The service provides each subscriber with a private, computercontrolled, multi-station network at shared-system savings.

Ward started using INFO-COM (Information Communications) to link its Chicago corporate office with 17 Ward facilities coast-to-coast. The system, equipped with sophisticated computers and communication gear, transmits messages at 100 words a minute.

Western Union furnishes the computers, computer programming, communication circuits, teleprinters, outstation equipment, and operation and maintenance of the system.

Service is provided nationally through Western Union's computer center in Chicago. As INFO-COM expands, computer centers in New York and San Francisco will also be used. Each center is equipped with two UNIVAC 418 computer systems.

Sending points on the network prepare messages on a teleprinter which produces a punched paper tape and a typed version of the message. The tape is inserted in an automatic transmitter which flashes the message to Western Union's computer center.

The computer selects the terminal on which to deliver the message, checks to be certain it is the correct terminal and then transmits the message.

As a double check, the computer verifies, by means of an automatic answer-back, that the right terminal has been reached.

MICRO CIRCUITS FIRM IS FORMED—Hybrid Electronics, Inc. located in the Jonathan Industrial Center, Chaska, Minnesota, will manufacture thick film circuits as its main product and will also do custom electronic development and electronic assemblies.

Robert L. Geib, who was formerly President of Universal Circuits, Inc., a subsidiary of Dahlberg Electronics, Inc., will be President. Other officers will be Peter C. Spaulding, V. P. of Marketing; Gerald F. Jablinski, V. P. of Engineering, and Virgil H. Hill, Secretary.

NEW PRESIDENT of IEEE ELECTED—Dr. F. Karl Willenbrock, Provost of the Faculty of Engineering and Applied Sciences at the State University of New York, Buffalo, will be President of The Institute of Electrical and Electronics Engineers for 1969.

Dr. Willenbrock's election was recently announced by the IEEE Board of Directors. He will head the world's largest engineering society, with a membership totalling over 150,000 throughout the world.

He succeeds Dr. Seymour W. Herwald, Vice President of Engineering for the Westinghouse Electric Corporation. IEEE Directors also announced the election by the voting members of Dr. John V. N. Granger as Vice President, 1969. Dr. Granger is President of Granger Associates in Palo Alto, California. Two additional Vice Presidents for 1969 will be elected at the IEEE's Annual Assembly in January.

Care to extrapolate?

1957 Delivered the first Fabri-Tek 80-mil core memory stack.

1958 Initiated production of stacks.

1959 Major computer stack production (Control Data Corporation's model 1604).

1960 Production of 50-mil stacks. First heated stacks.

1961 Delivered first Fabri-Tek core memory system.
Initiated thin film research.

1962 Thin film memory system developed.

1963 Production of 2-microsecond core memory systems.
Delivered the first commercially available planar thin film memory systems.

1964 Development of 1-microsecond main memory systems.
Large production of 2-microsecond main memory systems.

1965 Delivery of 500-nanosecond, 3D core memory systems. Development of mass memory system prototype (2½D, 2-wire). Delivery of large capacity 1-microsecond memory systems (2 million bits/memory).

1966 Development of 18-mil cores. Delivery of memory systems with integrated circuit logic.

1967 10^7 bit, 2.75-microsecond mass core memory installation.

1968 Delivery of large-scale planar thin film memory system.
Delivery of 16K x 80, 650-nanosecond, 2½D core memory systems.

1969 Mass core memory system production. Expanded production of proprietary core memory systems. Mass production of 2½D core stacks.

1970 $YP = \int_{o}^{Max.} (i + c + r)^*$

Fabri-Tek is a leader in advanced memory research, development and production. Our experienced Applications Engineers are ready to help you find solutions to problems in the following areas: Main Memories • Buffer Memories • Scratch Pad Memories • CRT Refresher Memories • Peripheral Mass Memories • Mil-Spec Memories • Extension of Main Memory • Numerical Control

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CIRCLE NO. 19 ON INQUIRY CARD

SUBSTATION TRANSFORMER LOADING ANALYSIS PROGRAM DEVELOPED—The Advanced Systems Technology Group at Westinghouse recently developed a computer program which appraises the area growth plans for transformer substations by the application of probability techniques. The method determines the risk for exceeding maximum transformer temperatures and evaluates the expected loss of transformer insulation life, based on area load forecasts and local ambient temperature conditions.

Calculations include the effect of ambient temperature on area load, as well as on transformer hot-spot and top-oil temperatures. Load and temperature are represented by statistical models so that the joint probability of each load and temperature level can be evaluated.

The probabilities of each combination of load and temperature which result in transformer temperatures in excess of specified limits are accumulated, and the resultant is converted to risk of exceeding limits in days per period. Transformer loss of insulation life is also based upon probability mathematics. Percent loss of life is calculated as a function of transformer hot-spot temperature for each combination of load and temperature and considered by the joint probability of occurrence of that combination. The sum for all combinations is then the expected percent loss of life for that transformer.

These calculations are made each period of each year of a study for each existing transformer. The program keeps tract of the accumulated percent loss of life for each transformer. When a limit is exceeded (usually 100 percent), that transformer is replaced with another having similar capabilities.

COMPUTER SYSTEMS MANUFACTURER FORMED—Computer Operations, Inc., a computer services and computer systems manufacturer has been formed in Silver Spring, Md. The new company consolidates the previous systems operations of Digital Associates, Inc. Baltimore and Ron Davies Associates, Silver Spring, Md.

Computer Operations provides complete turn key computer systems for a wide range of applications in data acquisition, analysis and control. In addition, the Company manufactures numerous hardware interfaces for non-standard data sources and peripherals. These include mass magnetic tape memories of the LINC type. Systems are delivered in an operating state with all interfacing and programming necessary for the application.

President of the new company is Stephen E. Silverman, formally of the Biomedical Engineering Laboratory of Johns Hopkins University. Facilities are located at 11215 Oak Leaf Drive, Silver Spring and 702 N. Broadway, Baltimore, Md.

ORDERS ENTERED FOR OVER HALF-MILLION DOLLARS IN DATA SETS—International Communications Corp., a subsidiary of Milgo Electronic Corp., Miami Fla., announced today the receipt of two significant awards, one from Trans World Airlines, the other from Western Union for data communications equipment totaling over $500,000.

Under an agreement with Trans World Airlines, ICC began delivery in December of Modem 440/24 PB data sets to be used in connecting TWA's Passenger Reservation Computer Center in Zurich, Switzerland with the United States as well as with cities in seven European countries.

The Western Union contract is a reorder for an additional quantity of Modem 4400 data sets. These data sets, which transmit information at a rate of 2400 bits-per-second, are of the same type currently utilized in Western Union's nationwide communication network.

The 1969 Systems Science and Cybernetics Conference will be held October 22 - 24, 1969 in Philadelphia, Pa. The conference theme is understanding and controlling natural [non-engineered] systems through the application of the methods of systems science and cybernetics and the use of natural system models in the design of engineered systems.

Abstracts of approximately 1000 words in length are required to be submitted to the Program Chairman by April 15, 1969, and final manuscripts for publication in the Conference Record are required by August 15, 1969. Address correspondence to: Mr. Hugh A. Raymond, Valley Forge Space Technology Center, General Electric Co., P. O. Box 8555, Philadelphia, Pa. 19101

The Instrument Society of America (ISA) announces the call for papers for its 24th Annual ISA Conference & Exhibit, to be held October 27-30, 1969 in Houston, Texas. The four-day conference will focus on "Instrumentation + Systems + Automation = Greater Productivity."

ISA invites state-of-the-art papers relating to this theme in all major areas of instrumentation and automatic control. Interested authors must obtain an "Intent To Present An ISA Paper" form (B3-2), that states instructions on preparing an abstract. Direct requests for forms to: Program Co-ordinator Herbert Buntzel, Bonner & Moore Assoc., Suite 1124, 500 Jefferson Building, Houston, Texas 77002, or Director of Technology Services Vincent J. Giardina, Instrument Society of America, 530 William Penn Place, Pittsburgh, Pa. 15219.

The deadline for abstracts is February 15, 1969.

The 1969 ACM National Conference, scheduled for August 26-28, 1969, at the San Francisco Civic Center, has issued a call for papers.

Areas of interest include: Techniques for symbolic and algebraic manipulation; Computer graphics; Computer assisted instruction; Design automation; Data transmission for online terminals; General purpose languages; Development and operation of remote access utilities; Realtime systems, and applications; Testing and conversion of realtime systems; Systems acceptance criteria; Time sharing networks; Resource allocation and scheduling; Automata theory-computability; Biomedical data processing.

Those planning to submit a paper should send a post card giving a brief description; working title; name, affiliation, business address (with zip code) and telephone number immediately to Ward Sangren, ACM 69 Technical Program Chairman, P. O. Box 2867, San Francisco, Calif., 94126. Five copies of the entire paper must be submitted by February 17, 1969.

We've expanded our plant for the fourth time and doubled our multilayer production.

We will now be able to produce more boards of all types, including higher density multilayer boards. Our present experience is 36 layers. Our new 24 x 40 fully automatic press will increase versatility and capacity. Our new equipment includes a 28-foot camera — largest and most precise in the industry. Together with our 18 foot camera this gives us unique capability.

We're steadily expanding our engineering staff to meet our customer's needs.

If you know us by our record, that's all we need say. If not, we'll add that we are known as the leader in the PC board industry.

Our story is quality. We hire the best people, train them our own way. NASA, the "mil spec" people, the big computer and consumer producers — they all come to us. They demand skill, reliability. They get it.

We're busy, but we're always interested in additional challenges. There's room for another wing out back.

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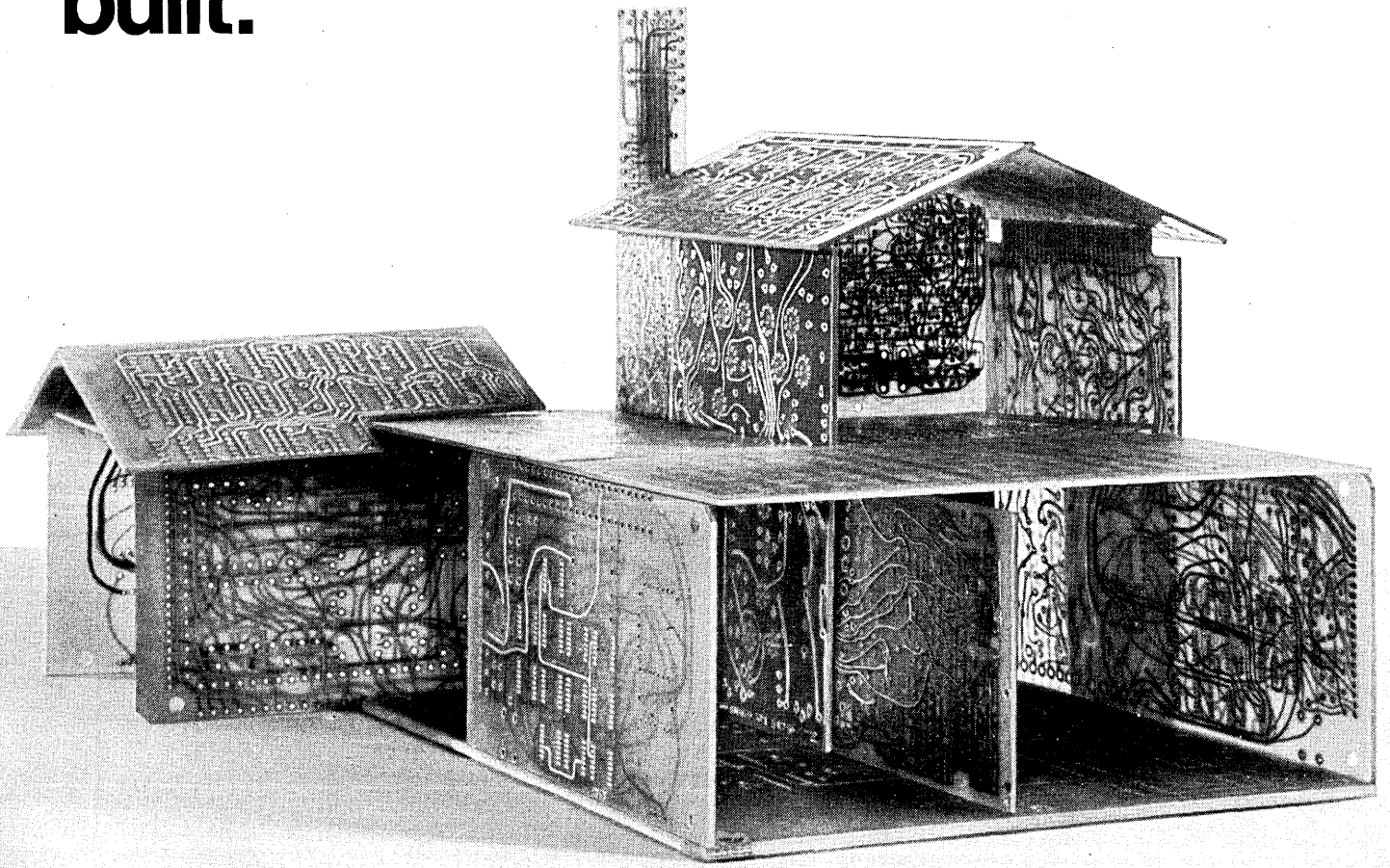

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DEVELOPMENTS

Superconductivity Temperature Pushed Higher in New Material

The highest known temperature at which a material becomes superconducting—that is, loses all resistance to the passage of current—has been reported by Bell Telephone Labs scientist B. T. Matthias and his associates, G. Hull and E. Corenzwit, together with scientists at the University of California and the University of Chicago.

Matthias and his co-workers have pushed the temperature for transition into the superconducting state of a multi-phase system of niobium, aluminum and germanium to above 20.7°K (Zero degrees K, or Kelvin, is equivalent to −460°F and represents total absence of heat.) This work represents a further increase in the highest attained transition temperature by 0.7 degrees over a record of 20°K reached last year in similar materials by Matthias and Professor T. H. Geballe of Stanford University and Bell Laboratories, and by L. D. Longinotti, E. Corenzwit, G. W. Hull, R. H. Willens and J. P. Maita, all of Bell Laboratories.

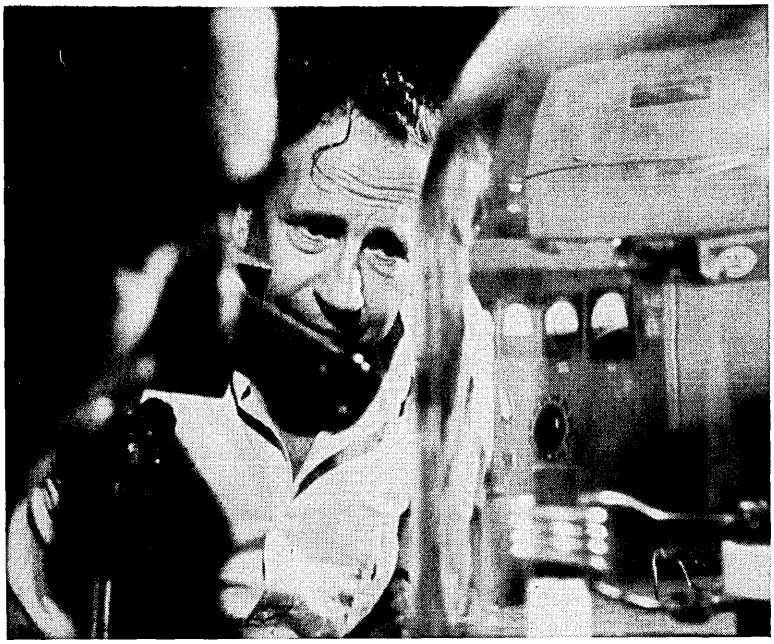
Since it is difficult to cool materials to the extremely low temperatures needed for superconductivity, physicists have searched for many years for ways to increase the temperature at which metals become superconducting. Until recently it was thought possible that a temperature near 18°K was an absolute upper limit for superconductivity, but the work reported last year by Matthias and Geballe showed that higher temperatures were possible and encouraged intensive work that has led to the new record of 20.7°K.

One very important feature of these newest superconducting materials is that the transition temperature is substantially higher than the boiling point of liquid hydrogen, about 20°K. This means that the new superconductors can be immersed in liquid hydrogen rather than the much more expensive liquid helium which boils at 4°K. Applications of superconductivity which have not been possible until now because of the high cost of liquid helium may now become feasible.

The niobium-tin superconductors discovered in 1954 were shown in 1961 by Kunzler and co-workers at Bell Laboratories to be capable of carrying very large currents and generating intense magnetic fields greater than 100 thousand gauss when wound into the form of a cylindrical coil or solenoid. Because of their higher transition temperature, the new materials recently discovered by Matthias and his associates may make possible solenoids that produce even more intense magnetic fields.

Only about 30 metals with superconducting properties were known when Matthias became interested in the field. Today more than 1000 superconducting metals are known —largely due to the discoveries of Matthias and his co-workers at Bell Telephone Laboratories and the University of California.

Matthias' findings have led him to formulate rules which have brought increased order to the study of superconductivity and have enabled him and others to predict the existence of new superconductors. The phenomenon of superconductivity has been a major factor leading to the understanding of the behavior of materials at low temperatures.



Bell Labs scientist B. T. Matthias and his co-workers have achieved the highest superconducting transition temperature (above 20.7°K) in a multi-phase system of niobium, aluminum and germanium. Superconductivity describes the state in which a material loses all resistance to electric current. Here, Matthias melts the material in a vacuum in preparation for studying its superconductivity properties.

With a memory like this, you can forget the logic

Use the logic easily programmed into our ROM (Read Only Memory) elements. With a minimum of time (typically four weeks versus the twelve required for new custom logic elements), we can set up the simple interconnection metalization pattern your needs dictate and start shipments. Costs about a thousand dollars versus the forty thousand new logic elements run to. And there's every probability that your production run elements will cost less too.

ROM elements are far simpler to make than a new, untried logic design. They're highly repeatable and proven reliable. No logic race conditions; no logic circuit debugging. And our new MOS ROM elements are fast, 500 nanoseconds, the fastest available. They operate from +12 and −12 volt supplies. Easily compatible with conventional DTL and TTL.

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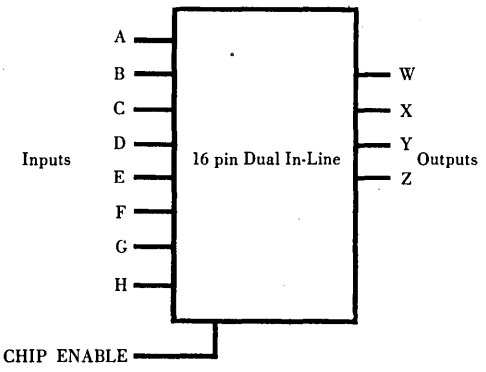
FROM YOUR TRUTH TABLE

Inputs								Outputs			
A	B	C	D	E	F	G	H	W	X	Y	Z
0	0	0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	0	0	1	0	0	1	1
0	0	0	0	0	0	1	0	0	1	1	0
0	0	0	0	0	0	1	1	1	1	0	0
0	0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	1	0	1	1	1
0	0	0	0	0	1	1	0	0	0	0	0
0	0	0	0	0	1	1	1	1	0	1	0
0	0	0	0	1	0	0	0	1	0	1	1
0	0	0	0	1	0	0	1	1	1	1	1
0	0	0	0	1	0	1	1	1	1	0	1

TO YOUR MM 521



National MOS

CIRCLE NO. 20 ON INQUIRY CARD

Image Display System Could Expand Television Monitor Market

A powerful computer-based image display system that could make the television monitor as important as the telephone in the office of tomorrow has been developed by the Rand Corp., Santa Monica, Calif. Thomas O. Ellis, a senior scientist, said that a new Rand information network makes use of standard television monitors that are linked to an experimental image distribution system (IDS) developed by IBM's Los Gatos Laboratory.

In operation at their headquarters in Santa Monica, the new system serves as a video-electronics hub that will eventually give many scientists access to data stored in several computers by using television terminals in their offices.

The image-generation portion of the network was built under contract to Rand and is linked to an IBM 1800 data acquisition and control system which receives data from an IBM System/360 Model 40 computer. This information is then converted into text or graphics for display on television monitors.

The image distribution system can display computer-generated video information on thirty-two remote high-resolution television monitors simultaneously, and then modify this information according to the user's instructions.

Information to be displayed, whether initiated from the computer or the viewer, is combined under program control, generated as digital data, converted and organized into a two-to-one interlaced television signal by scan conversion.

These video signals are then recorded on a thirty-two track magnetic disk buffer which stores the video information and transmits it to the appropriate television monitor.

"There are three television consoles in operation now, but we expect to add 29 more next year," Mr. Ellis said. "The system could handle several hundred consoles in the offices of individual staff members. To communicate with the system, a scientist may use several devices including a keyboard and an electronic tablet to write or sketch information directly into the computer.

He may modify sections of the image displayed on his screen with the help of the computer which processes the information entered on the tablet. Thus, the scientist can change sections of the image by correcting or adding to it. This new information may appear brighter on the screen so that there is a useful reference point.

The system can handle gray tones as well as black and white. This permits both live and still pictures to be routed to the TV terminals. Live broadcasts by-pass the computer system and are transmitted directly to the television monitors. However, still photographs taken with a TV camera can be recorded on the video disk.

By reading two tracks on the video disk simultaneously, computer-generated information, such as text, can be superimposed on pictures or graphs which appear on the television screen.

Capacity of Bulk Random Access Memories Increased

Ampex Corp. has developed an experimental system at its Redwood City, California, Laboratories which stores up to 50 billion bits of information on single 10½ inch reels of magnetic tape. This is approximately 1,000 times the capacity of typical tape reels presently used with computers. The information can be accessed and transferred, on the average, in less than ten seconds.

"During the experimental stage, now completed, the test system demonstrated the feasibility of applying videotape recording techniques to the bulk digital storage problems of a computer, with substantial advantages in storage capacity, access speed, at a reliability and economy," said Dr. William A. Gross, VP-GM of the Research and Advanced Technology Division.

A finished memory based on the development would enable a computer user to place all of his digital records on-line, ready for immediate random access by the computer. These dramatic gains in capacity are made possible by the recording densities inherent in the video recording technique plus efficiencies in the use of tape which it makes possible. Today's on-line bulk memories can store only a fraction of typical large data stores. The remainder is stored on magnetic tapes which are kept on shelves and manually loaded into the computer system as needed.

The Ampex system would eliminate shelf storage and delays now required when a needed tape reel or disc pack is located and manually placed in the system. All records would be at hand with any portion of the data accessible in seconds.

Gross said Ampex is continuing work on systems with configurations applicable to both existing and fourth generation computer systems. The videotape recorder increases recording density by using four recording and playback heads mounted on a small metal disc that rotates perpendicularly across the moving tape for recording or playback. Conventional digital tape drives have fixed heads that record and play back parallel to the motion of the tape. The rotary head increases relative tape-to-head speed by approximately six times that of the fastest fixed-head device. This makes possible the recording of high frequency television pictures or, when applied to coded data, greatly increased volumes of information.

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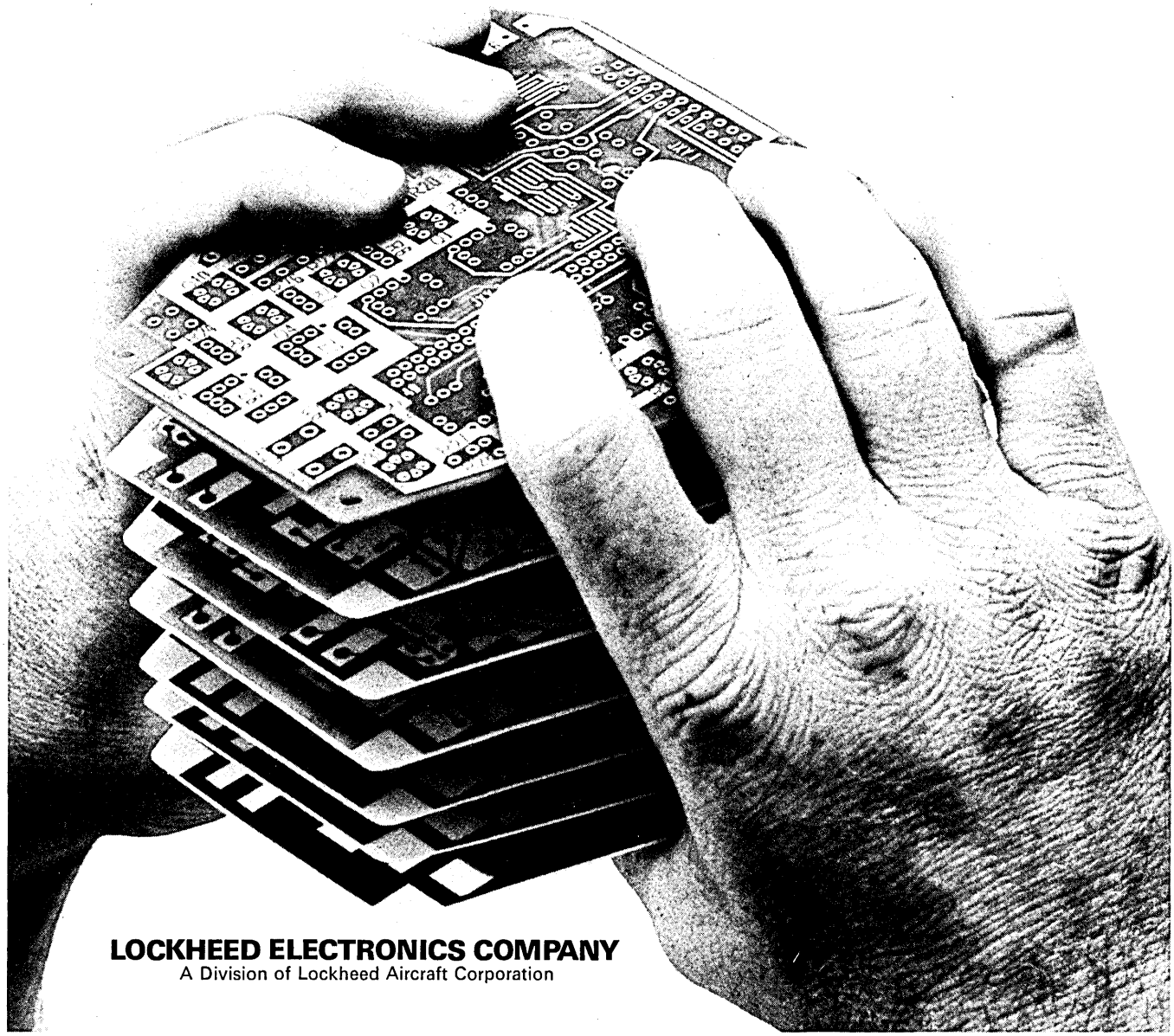


LOCKHEED ELECTRONICS COMPANY
A Division of Lockheed Aircraft Corporation

CIRCLE NO. 21 ON INQUIRY CARD

DEVELOPMENTS

Error Correction Developed For Trillion-Bit Storage System

The chance for error in a line of data read by the world's largest computer storage system is only 0.000075 percent.

This statistic is based on test data in "Error Detection and Correction in a Photo-Digital Memory System," an article in the November issue of the *IBM Journal of Research and Development.*

The journal article describes the trillion-bit systems' error-correcting techniques and shows how the system can correct errors rapidly enough for real-time operation.

The photo-digital storage system was built by IBM under a special contract for the U.S. Atomic Energy Commission. The AEC contract specified the allowable error rate as no more than one 300-bit line with uncorrected errors in 2,700,000 lines read. The system has demonstrated a much better average of one line with uncorrected errors in 13,500,000 lines read.

The system functions in a network of computers at the Lawrence Radiation Laboratory in Livermore, California. A second system, using the same error-correction techniques and having approximately one-third the storage capacity of the first, has been installed at the Lawrence Radiation Laboratory in Berkeley, California.

The error-correction methods blend with the special characteristics of the system, which uses an electron beam to record binary data on 1.3- by 2.7-inch film "chips." The system develops the chips in its own fully automated film laboratory, transports them in plastic cells through a system of pneumatic tubes, and files them for retrieval and reading by a high-speed flying spot scanner. A programmed control processor coordinates these events.

A hybrid combination of software in this control processor and hardware in a data controller helps provide the powerful error-handling facilities needed in the system. The system's high recording density necessitates the use of a sophisticated code, and the one employed —a Reed-Solomon type—is particularly suited for correcting errors that occur on photographic film. To implement the code, the data line is divided into 50 six-bit characters of data, a 2 character line number, and 11 characters of redundancy. The data controller encodes data and detects errors, while the control processor, acting in a time-sharing mode, directs error correction. Time sharing by the processor is accomplished through the use of multiple interrupt levels.

The journal article emphasizes that this unique hardware-software combination in the error-correcting process is adaptable to any of a growing number of systems with a programmed processor available on a time-shared basis.

A novel feature of the process that helps implement the code rapidly enough for real-time operation is the initial assumption that an erroneous line of data contains only one error. Using the full capabilities of the code for every correction would be time consuming. Consequently, the process always begins with single-error correction, which is comparatively simple and rapid. If single-error correction fails, the process continues with attempts to correct two, three, four and, finally, five errors. This procedure is relatively slow for lines with four or five errors, but the fact that most errors are single errors keeps the average correction time down. In a large test sampling, average decoding time for all lines with errors was only one-third higher than the time expended on lines with one error alone.

Other significant features include a symmetric code polynomial that allows an economic use of circuitry and two-error correction without the usual trial-and-error procedures.

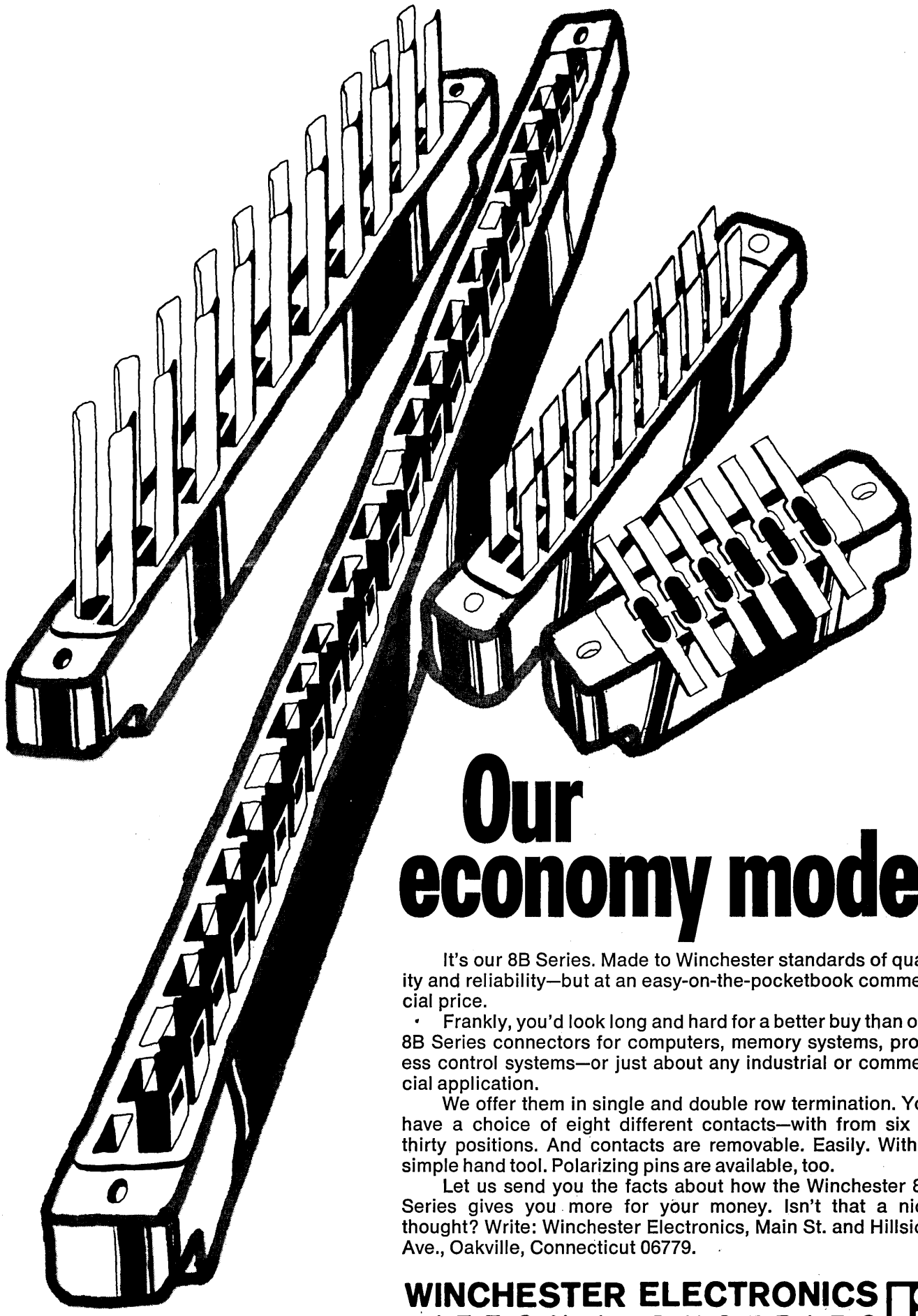
New Material Provides Longer Recording Head Life

Ferroxcube Corporation has announced the development of a monocrystalline ferrite material for use in magnetic recording heads. The new material, with its increased wear resistant characteristics, is expected to find wide use in video and high density tape-recording applications where recording head wear is a significant problem. Recording heads made of the new material are expected to increase the head life in these applications by a factor of 10 times or more thereby reducing the service costs of users.

The practical process for growing single-crystal manganese-zinc ferrite has been developed by using a technique similar to that used in producing synthetic gem stones. This material is not the conventionally designated "monocrystalline" ferrite, which, though composed of large-size crystals, is actually polycrystalline.

The single-crystal ferrite, as the name implies, is a single, completely homogeneous crystal, with no grain boundaries to permit crystal pullout which is frequently responsible for the familiar crumbling or wear of the contact face and gap edges. The superior mechanical properties of this new ferrite are further enhanced by proprietary glass-bonding, or metal-bonding processes. Heads fabricated from single-crystal ferrite and bonded by this means present a monolithic contact surface of extremely high density and very low porosity in which the magnetic gap can be controlled to within ± 5 microinches or less and original sharp edges and machined profiles preserved intact through thousands of hours of operation.

Characteristics include an initial permeability (u_0) of 2250± 250 at 100 kHz, 350± 50 at 5 MHz.



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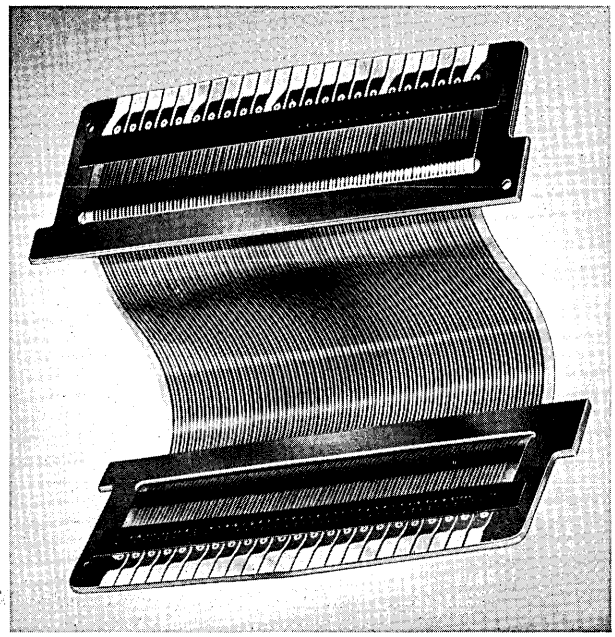
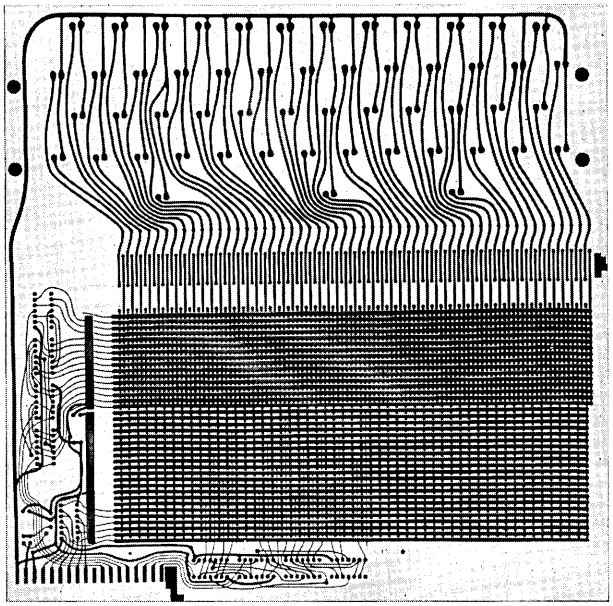
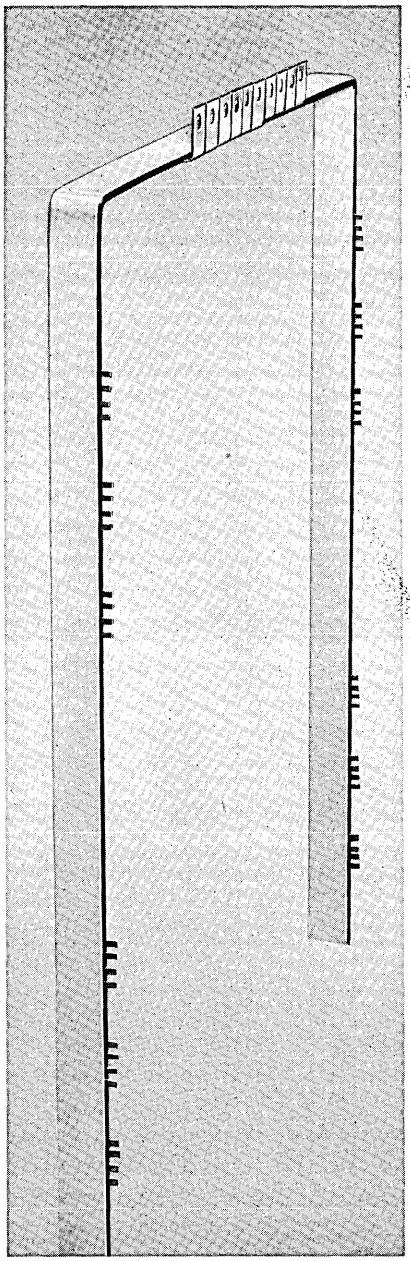
a.



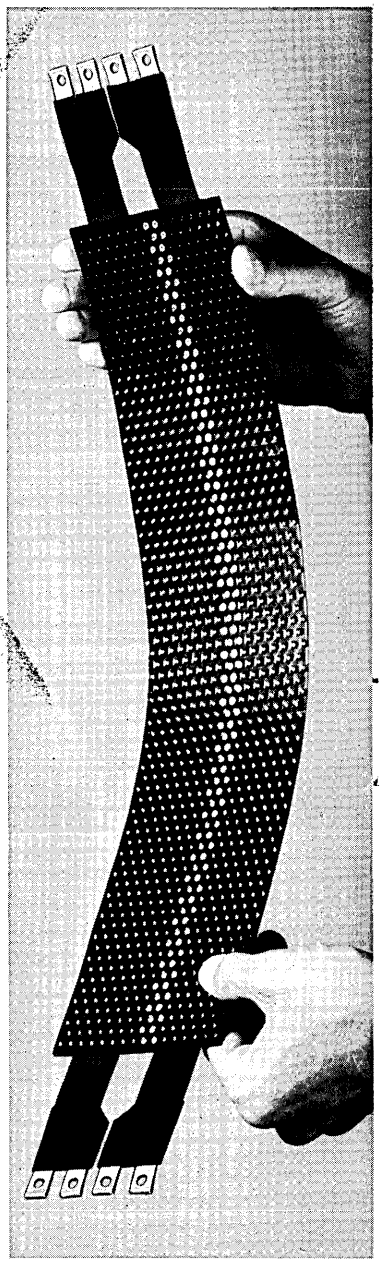
b.



c.



d.



An electronic solution is proposed to the process of solving linear partial differential equations utilizing highly-multiple processing elements.

AN ARRAY PROCESSOR USING LARGE SCALE INTEGRATION

David H. Andrews

Electronics Consultant
Boulder, Colo.

The solution of array-type boundary-value problems by machine leads to an interesting study. Calculations of this nature involve the simpler arithmetic operations of addition, subtraction, complementation and shifting; these operations are repeated as many times as there are elements in the array. The complete solution of a boundary-value problem requires many iterations of the processes involved in the computations for a single set of array values.

The methods presented later are applicable to the solution of linear partial differential equations of the following forms:[1]

Parabolic—Heat Conduction, Diffusion

$$V^2\Phi - \frac{1}{y^2}\frac{\partial\Phi}{\partial t} = f(r,t) \qquad (1)$$

Hyperbolic—Waves

$$V^2\Phi - \frac{1}{c^2}\frac{\partial^2\Phi}{\partial t^2} = f(r,t) \qquad (2)$$

Hyperbolic—Damped Waves

$$V^2\Phi - a_0\frac{\partial^2\Phi}{\partial t^2} - a_1\frac{\partial\Phi}{\partial t} - a_2\Phi = f(r,t) \qquad (3)$$

Elliptic—Static Case

$$V^2\Phi = f(r) \qquad (4)$$

David Andrews received the degree of EE from Rensselaer in 1934, and the MEE at the University of Colorado in 1968. Since then he has spent 31 years in the employ of the U.S. Government. Most recently he was chief of the standard frequency and time broadcasts section of the National Bureau of Standards. He is now a registered P.E. and an electronics consultant and is a senior member of IEEE.

The processor described here is intended to be used as an adjunct to a general purpose computer.

USUAL COMPUTER TECHNIQUES

In order to understand the advantages to be gained by using a special processor unit, it is first necessary to examine the steps required to perform a single element calculation using a general purpose computer.

The steps are:

1. Fetch from memory the value of the element and other nearby elements.
2. Perform the necessary arithmetic operations.
3. Restore the updated values.

This same process must then be repeated by the number of elements in the array and the total process a sufficient number of times to assure the desired accuracy in the final result.

It is then possible to define the processing time as follows:

$$T = t\ (m \times n \times c) \qquad (5)$$

where: T is the total processing time
t is the element processing time
m is the number of columns in the array
n is the number of rows in the array
c is the cycles of iteration required.

Since this is a serial processing method, all of the arithmetic operations must be done by the arithmetic unit in sequence, thus rendering the arithmetic unit incapable of other operations than the simple ones required for this problem. In addition, the fetch and restore functions are continually in operation, effectively harnessing an entire general purpose computer capable of very sophisticated computations to a lengthy and menial task.

Economic considerations dictate that expensive and complex equipment only be used for purposes compatible with its greatest capabilities, unless the equipment is otherwise idle, or for purposes of experimental study or development.

Thus, if a particular type of computation was

necessary only once, it would be economically justifiable on a general purpose computer at great expense; however, if the same computation were required repeatedly the possible cost savings would, at least, call for a study of hopefully less expensive computational methods.

With due deference to Dr. Amdahl, I.B.M.'s staunch exponent of uniprocessors[2], it is the author's firm conviction that parallel processors will find a real place in the future computer industry.

HISTORICAL APPROACHES

With firm confidence in the maxim "Never send a man to do a boy's job!" others have turned their talents to parallel processors as an answer to the problem of multitudinous routine or simple calculations.

A very fine article by John C. Murtha[3] gives a complete background of information on parallel processing. For the purposes of this article attention will be focused on a few of the computers that have been arranged for parallel processing.

The SOLOMON computer[4] is undoubtedly the most significant of parallel processing computers that have been designed and built. The SOLOMON system is built around a network of processing elements arranged in an array of 32 $\times$ 32 units, or a total of 1024 processing elements. Each processing element is a complete minimized serial-by-bit arithmetic and logical unit capable of performing a full complement of arithmetic and logical instructions on a pair of binary digits at a time. Each processing element has associated with it a data memory which serves as its working storage. In addition to the element data memory there are also the program memory and the bulk exterior memory. Arrangements are made whereby each processing element may have access to stored data in its own memory, the memory of any of its four neighbor processing elements, the program memory, or the bulk exterior memory. Each processing element is capable of several different modes of operation, and all of the processing elements are directly controlled by the network control unit. The basic difference between the SOLOMON computer and a multiplicity of general purpose computers is that only one control unit is used and it programs all of the processing elements identically. A block diagram showing the arrangement of the major components of the SOLOMON II system is given in Fig. 1.

The operation of the SOLOMON system is described with reference to Fig. 1. Data to be used in the computations is loaded into the memory through the input/output control unit. The program memory is loaded with the required instructions which direct the computer in its performance of the desired computation. As necessary the individual processing unit memories are loaded through the buffer from the main memory. Information is transmitted in parallel to the buffer and then serially-by-bit to 32 of the 1024 processing elements simultaneously. Addressing of the data to the processing elements is controlled by the program memory through the network control and sequencer; two of the data bits furnished the processing

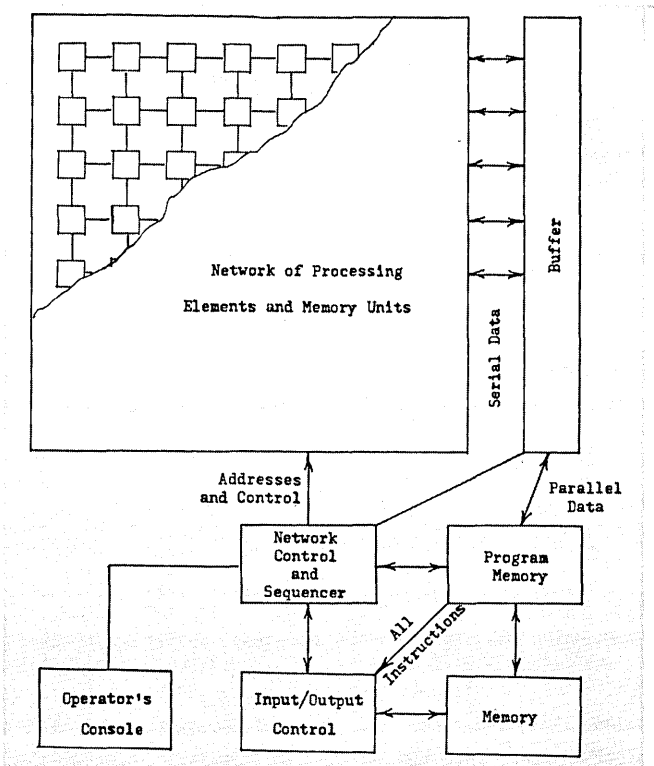


Fig. 1 The Solomon II System.

elements control the mode of operation of the processing element.

When the computation is complete the data from each processing element is read out through the buffer either into the main memory or through the input/output control unit to peripheral equipment.

Hard on the heels of the SOLOMON computer is the ILLIAC IV[5,6,7] computer being developed jointly by the University of Illinois and the Burroughs Corporation. Categorically this computer falls in between a general purpose "pipeline" computer and the SOLOMON computer. Instead of the design value of 1024 processing elements used with the SOLOMON computer, the ILLIAC IV uses only 256. The ILLIAC IV, however, has four control units, each controlling 64 of the processing elements. This arrangement leads to a more flexible programming capability. The processing element used in the ILLIAC IV is considerably more sophisticated than the serial-by-bit element used in the SOLOMON computer. This processing element is a three-register arithmetic unit capable of performing a full repertoire of instructions on 64-bit, 32-bit, or 8-bit operands. Full floating-point operations are included for the 64-bit and 32-bit words. A number of special purpose logic operations combine with the arithmetic capabilities to enable a floating-point multiply time of about 400 nanoseconds and a floating-point add time of about 200 nanoseconds. The general arrangement of the ILLIAC IV computer is shown in Fig. 2.

The operation of the ILLIAC IV system is somewhat similar to that of the SOLOMON system. A general purpose computer is required in conjunction with the

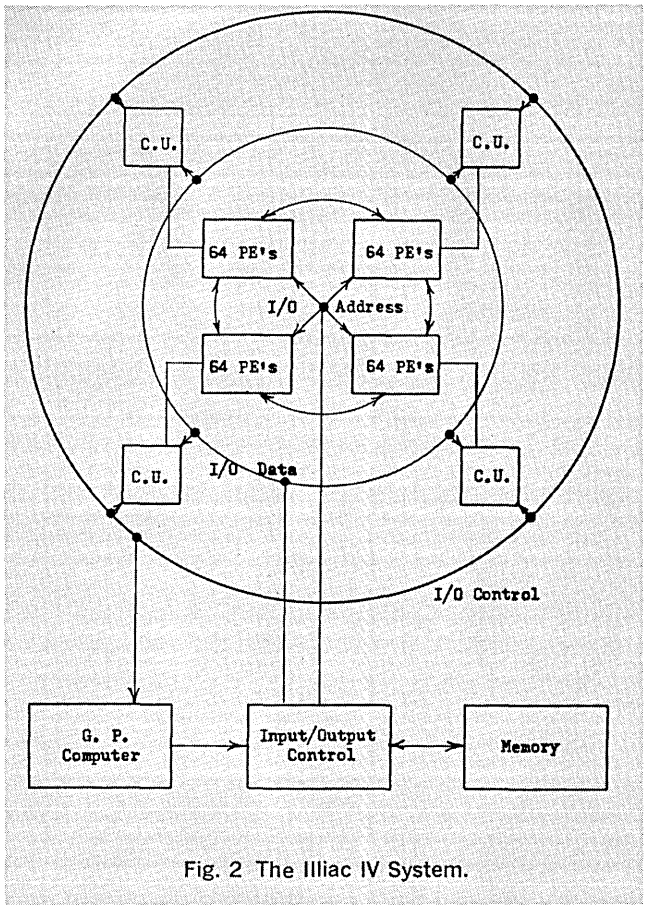


Fig. 2 The Illiac IV System.

ILLIAC IV system and serves as the control center for the computer system. Information to be processed is loaded into the main memory and upon demand is transferred to the processing elements. Addressing is done through the input/output control unit to any of the 64 elements in each of the four banks of processing elements. Each bank of 64 processing elements has its own control unit to enable different programs to proceed in each bank if desired. Computations proceed as directed by the program unit. Upon completion of the program, data is recovered through the input/output unit and is transmitted to the peripheral equipment.

Having reviewed the two most promising parallel computer systems, it will now be advantageous to limit further review to those systems which have been proposed particularly for the solution of numerical differential equations.

The concept of a machine designed especially for the solution of Laplace, Poisson, diffusion and wave equations probably originated with Leondes and Rubinoff in 1952[8]. As with many good ideas, the state-of-the-art had to catch up with the concept, hence the idea remained dormant until the early 1960's when work was done by Tanaka at Lockheed[9] and Rosin at the University of Michigan[10].

The Lockheed array processor consists essentially of a general purpose computer working in conjunction with a line of processing modules operating on data stored serially on a magnetic drum. The system as conceived would operate with 20 processing modules, each assigned to a single track on a 20 track magnetic drum. Each track would be equipped with one read head and one write head. With a magnetic drum rotating at 6000 rpm and with a 1 MHz/s clock rate, an add time for a 20-bit word of 20 microseconds would result. A plugboard sequencer was also designed for use with the processing modules to enable a variety of computational programs. The general purpose unit is used to set up the data in the modules, to supply initial conditions, and to receive output data.

The University of Michigan array processor, while very similar in fundamental concept to that of Lockheed, differs in several important points. This unit is restricted in its application to the solution of the Laplace equation with Dirichlet boundary conditions. The machine undoubtedly could be reorganized to enable the solution of other partial differential equations. The array for the University of Michigan machine is contemplated as much larger than that of Lockheed, 1000 tracks each containing 375 words of 40 bits each. The drum speed is 1500 rpm. While not specifically mentioned, it is logical that a general purpose computing capability would be required to enter the data on the drum and receive the data from the drum.

A simple calculation will give a comparison of the computing capabilities of the Lockheed and University of Michigan machines. The term bits-per-second will be used as the common term for comparison.

For the Lockheed machine:

$$\text{Bits/sec} = \text{No. of channels} \times \text{bits/channel} \times \text{rev/sec} \quad (6)$$
$$= 20 \times 20{,}000 \times 100 = 40 \text{ Megabits/sec}$$

For the University of Michigan machine:

$$\text{Bits/sec} = 1000 \times (375 \times 40) \times 25$$
$$= 375 \text{ Megabits/sec}$$

Thus, it is evident that the University of Michigan machine's computing capability is nearly an order of magnitude greater than that of the Lockheed machine.

Before leaving the subject of computing capabilities it would be well to note the capabilities of the IBM System/360 Model 91[11]. This system represents the state-of-the-art as far as uniprocessors are concerned. A very high speed of operation is attained. This speed results partly from higher speed components but mainly from a reorganization of machine operation. The storage access time has been reduced by interleaving and by providing CPU buffer registers, a technique to allow data and instruction queues. Applying the full capabilities of the machine to a problem of repetitive calculations results in one computation every 60 nanoseconds on a word of 72 bits length. Hence—

For the IBM/360 Model 91 machine:

$$\text{Bits/sec} = 72 + (60 \times 10^{-9})$$
$$= 1200 \text{ Megabits/sec}$$

Obviously, the data processing capabilities of the IBM machine exceed the capabilities of either the Lockheed or University of Michigan machines. Two things work at this point in favor of parallel processors. One is that the IBM speed for a uniprocessor represents just about the limit for processing element speeds and advantageous machine organization. The

second is that the calculated speeds of the parallel processors were derived without the advantage of the higher speeds that can now be attained in computer circuitry. That these two factors can work to a really advantageous position for parallel processors will be seen.

A SPECIFIC PROBLEM DEFINED

At present parallel processors have the advantage over uniprocessors for the solution of specialized problems involving a tremendous number of routine calculations. For the purpose of this article, it was decided to select one such problem commonly encountered in scientific calculations and plan a computational system to handle this problem effectively.

The solution of partial differential equations using finite difference methods involves a large number of identical iterations over a large array of data. Thus, by its very nature, this type of problem should lend itself admirably to solution by a parallel processor type of computing machine organization.

Equation (4) has been selected for this study. Indeed, the generality of this equation has been further restricted to the two dimensional case and also the right side of (4) has been set equal to zero. The following equation then becomes of direct concern:

$$\frac{\partial^2 U}{\partial x^2} + \frac{\partial^2 U}{\partial y^2} = 0 \qquad (7)$$

This equation is commonly known as Laplace's equation in two dimensions. The solution of this equation usually involves the determination of values of U at selected values of x and y lying between given values of U at specified x, y boundaries. Thus the accepted solution must be capable of using the given boundary values and producing the desired intermediate values to the required accuracy.

METHOD OF SOLUTION

The technique of obtaining a numerical solution to the above defined problem may be readily found in a good text[12] on numerical analysis. Satisfactory methods revolve around the fact that the true value at any point is equal to the arithmetic mean of the four values obtained at adjacent mesh points.

The method of iteration consists in a systematic progression through an array replacing each interior value with a new value which is the mean of the four neighbor values. This method lends itself readily to machine solution.

The method of relaxation consists in making corrections to each interior value amounting to ¼ of the algebraic sum of the differences between each neighbor value and the value at the mesh point being computed.

The method of over-relaxation is essentially the method of relaxation with the difference that the corrections made are multipled by some factor "w" where w lies between 0 and 2. The case where w = 1 is the regular relaxation method.

The relaxation methods are of optimum value where the residue values, the differences between the present values at points and their updated values, may be observed. Under these conditions it is possible to operate selectively on those residues having the largest magnitudes from the outset and thus arrive at a solution expeditiously. For manual solution this method has obvious advantages.

The objectives of this article will be attained by employing the method readily performed by machine, the iteration method. This method, however, may be applied satisfactorily in several different ways depending upon the machine organization. The three ways considered here are point, line, and array iteration.

Point iteration consists in taking the array one point at a time in an orderly fashion, calculating a new value for the point and immediately substituting the new value. This method is readily used with a general purpose computer.

Line iteration consists in taking the array one line (row or column) at a time in sequence, calculating new values for each point of the line and then substituing the new values for the line. This method is used in the Lockheed and University of Michigan machines.

Array iteration consists of taking the entire array at once, calculating new values for every point of the array at once, and then replacing all of the values with their updated values. This method will be employed in this article.

In order to give some feel for the effectiveness of these methods of calculation, an extremely simple array with an obvious answer has been computed by each of the three methods with sufficient iterations to come within 0.1 percent of the correct answer. The array selected is a 4 x 4 square array with all edge values equal to 1. The four central values are then computed by each of these iteration methods.

Figure 3 shows the problem as described.

1.000	1.000	1.000	1.000
1.000	a	b	1.000
1.000	c	d	1.000
1.000	1.000	1.000	1.000

Fig. 3 A simple array for studying computational effectiveness.

In addition to the values for a, b, c, and d the arithmetic mean is also computed. These computations are presented in Table I.

Using the arithmetic mean values from Table I, it is seen that 5 iterations are needed by the point method to attain a value of 0.999, 7 iterations by the line method, and 9 iterations by the array method. This shows that the point method is the most efficient and the array method the least efficient with the line method falling in between.

Figure 4 shows the percent deviation from true value plotted on semi-logarithmic paper as a function of the number of iterations. The three methods of iteration, point, line, and array are compared. The regular nature of the curves would indicate that it is likely that a mathematical expression can be found that would relate the required iterations to the size

of the array and iteration method employed. It is sufficient here to note that the point method is the most efficient and the array method the least efficient. Data for this graph were taken from Table I.

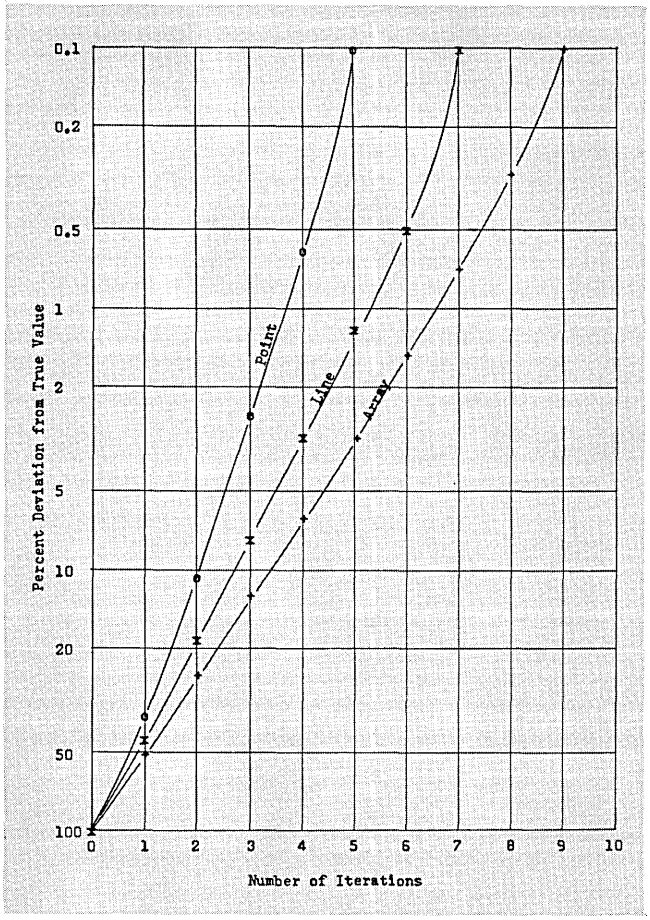


Fig. 4 Comparison of iteration method efficiencies.

GENERAL DESCRIPTION OF THE ARRAY PROCESSOR

The array processor to be described is oriented specifically to the rapid solution of Laplace's equation in two dimension (7) by the method of array iteration.

The array may be built in any desired size; however, to select a suitable size for discussion, the array has been selected to have a size of 100 x 100 elements.

The processing element for each array point must have the ability to sum the four neighbor values, divide by four, and replace the existing value of the point with the new value. For the array under consideration, then, there must be 10,000 similar processing elements.

The processing elements then must be arranged in some logical pattern for ease of construction, assembly, and addressing. Since the array of processing elements was chosen to be square, and since the processing elements are basically memory elements, it seemed logical to arrange them in a cubic form similar to usual core memory systems. Hence, it is proposed that each processor element be arranged in a linear fashion, and that a number of these elements be formed side-by-side to compose a plane of processing elements. These planes may then be stacked to the desired height to compose the array of processing elements.

Like any memory system it is necessary to have suitable auxiliary equipment to address particular elements and to write-in or read-out the data stored in each element. In addition to these items it is also necessary to have means to effect the computation cycle.

Figure 5 shows a skeleton view of the proposed array processor. The "Y" address register is used to select the particular plane of the array containing the desired element. The "X" address register then selects the processing element from the line of elements on the plane. Finally, the read-write unit inserts or re-

	Point Iteration Method					Line Iteration Method					Array Iteration Method				
	a	b	c	d	ave	a	b	c	d	ave	a	b	c	d	ave
Commencement	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000
1 Iteration	0.500	0.625	0.625	0.813	0.641	0.500	0.500	0.625	0.625	0.563	0.500	0.500	0.500	0.500	0.500
2 Iterations	0.813	0.907	0.907	0.954	0.895	0.783	0.783	0.852	0.852	0.818	0.750	0.750	0.750	0.750	0.750
3 Iterations	0.954	0.977	0.977	0.989	0.974	0.909	0.909	0.940	0.940	0.925	0.875	0.875	0.875	0.875	0.875
4 Iterations	0.989	0.995	0.995	0.998	0.994	0.962	0.962	0.976	0.976	0.969	0.938	0.938	0.938	0.938	0.938
5 Iterations	0.998	0.999	0.999	0.999	0.999	0.985	0.985	0.990	0.990	0.988	0.969	0.969	0.969	0.969	0.969
6 Iterations	-	-	-	-	-	0.994	0.994	0.996	0.996	0.995	0.985	0.985	0.985	0.985	0.985
7 Iterations	-	-	-	-	-	0.998	0.998	0.999	0.999	0.999	0.993	0.993	0.993	0.993	0.993
8 Iterations	-	-	-	-	-	-	-	-	-	-	0.997	0.997	0.997	0.997	0.997
9 Iterations	-	-	-	-	-	-	-	-	-	-	0.999	0.999	0.999	0.999	0.999

Table I Comparison of various iteration methods.

moves data from the processing element.

The processing element which will be described in detail later operates serially-by-bit as a shift register. Figure 5 shows a shift driver to be used to perform the computation cycle; a clear driver is also shown. This unit has the capability of clearing the entire array of memory elements simultaneously, thus preparing the processor for a new problem.

In its original conception this processing unit was planned for use as an auxiliary unit to a general purpose computer. Since then it appears that the processor could be operated with relatively simple control equipment and the inevitable input-output facilities. Thus, the processor would be suitable as a special purpose computer which, with integrated circuits, could be made relatively small with respect to the input-output equipment.

THE PROCESSING ELEMENT

The heart of the array processor is the processing element. Since there must be many of them in any useful array, the circuitry has been reduced to a minimum. The required components are a natural for integrated circuitry. It is to be expected that advances will be made in the art of large scale integration so that 100 processing elements could be formed on a single sheet of base material. In this case 100 such sheets would compose the entire array processor.

Referring to Fig. 6 it is seen that the processing element is composed of N+1 memory elements arranged as a shift register. N is the number of parallel data bits that the processing element is capable of handling. One isolated bit, the "0" bit, is used to set the mode of operation of the processing element. If a zero is written in "0" the element will compute, and if a one is written in "0" the data will recycle unchanged.

Data is entered into the processing element in parallel through the set (s) terminals of the memory elements. Read-out is accomplished by observing the "1" terminals.

Each iteration cycle consists of N + 1 pulses applied through the shift input terminal. Consider first the operation of the element when a one is in memory element "0". This one enables the Hold AND gate to pass information at the output of memory element "1". This information from "1" then becomes the input for N+1 and after N + 1 shift pulses reappears at "1". The OR gate between N-L and N passes this information without interference since the

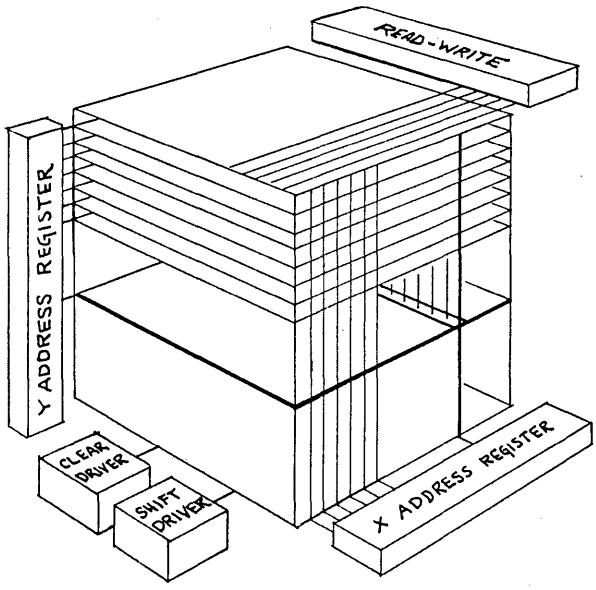


Fig. 5 Skeleton view of proposed "array" computer.

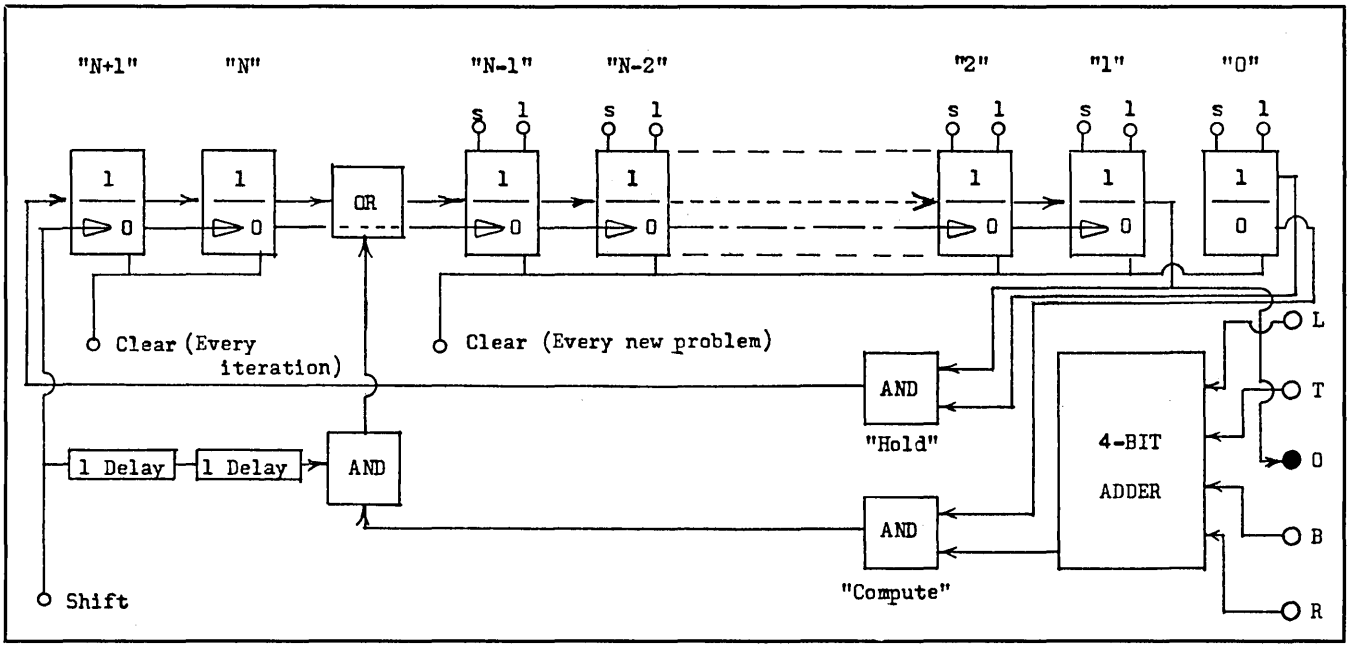


Fig. 6 Logic diagram for memory and compute circuitry for typical array point "word".

Compute AND gate is inactive. This condition of operation is used for all boundary points of the array to be computed. It also is the operating condition for all elements external to the boundary points of the array.

Reconsider the operation when "0" contains a zero. The Hold AND gate is now disabled and data output from "1" goes only to the output terminal of the processing element, indicated by the black dot of the output terminals. The Compute AND gate is now enabled allowing the output from the 4-bit adder to be entered into the memory elements. The subsequent AND gate, however, is not enabled until the third shift pulse occurs. Thus, the first two bits out of the 4-bit adder are lost and only N−1 bits are entered into the memory elements. This technique effects the division by 4 that is required to process the sum of the 4 adjacent bits to the processing element under consideration. Note that there are only N−1 active bits of data whereas there are N + 1 shift pulses used to perform the operation. This is necessitated by the divide-by-four factor in the calculation. Also note that the N and N+1 memory elements can only be set to one when they are used in the Hold mode and then only by the shifting ones. Since these two memory elements never contain ones at the completion of a compute cycle, they do not interfere with the accuracy of information transmitted through the OR gate in the Compute mode of operation.

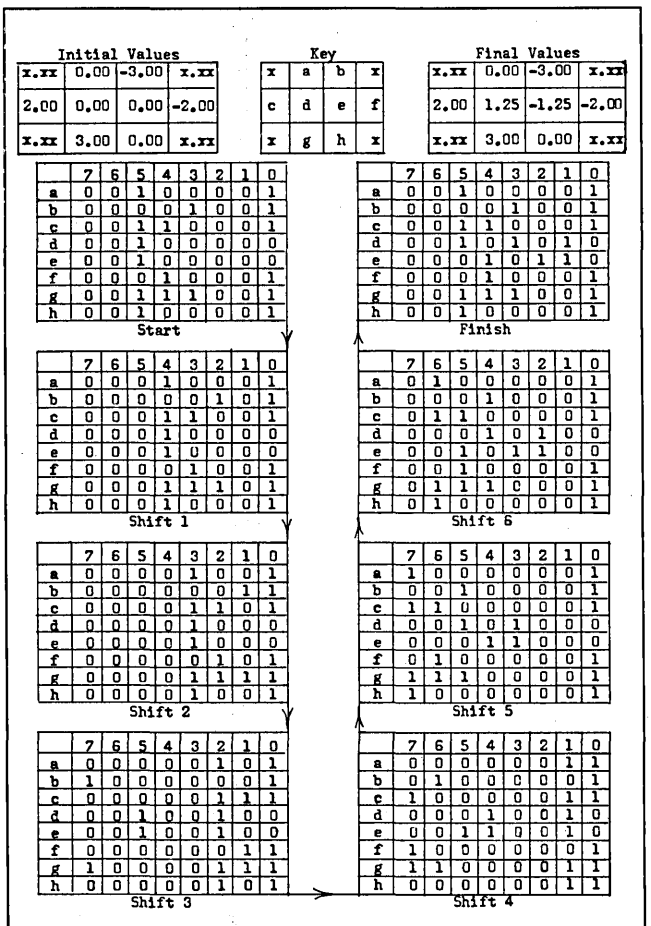


Table II Tabulation of shift register contents during one iteration.

It is interesting to consider the 4-bit adder for a moment. This device can produce two bits of carry pulses subsequent to the latest data entry. Because of this fact it is necessary to provide two zero pulses after the active bits of data have been shifted. The circuit shown enters these carry bits in N-1 and N-2 cells.

In order to give one a feel for the performance of the shift registers during an actual calculation, Table II shows the actual contents of the various memory cells during each step of the calculation. An extremely simple array of 3 x 4 elements having eight active processing elements was chosen for illustration.

The initial values of the contents of each processing element are shown in the upper left diagram. The values obtained after a single iteration are shown in the upper right diagram. The key to the tabulation is shown in the upper center diagram.

The processing elements are N = 6 type and have seven active bits for computational purposes with one extra bit for Hold or Compute control logic. The "O" bit is used for control purposes.

The bit in the "5" position is used for sign information and is a one for positive numbers and a zero for negative numbers. When the zero occurs the number is represented in complement form. The mathematical background for this unconventional notation is given in the next section.

The bits in the "6" and "7" positions are always zero at start and finish. To assure that this is so each iteration begins with a clear pulse to these memory elements. These elements will change to ones during the Hold cycle as required to propagate the binary number information. During the Compute cycle these bits provide the zeroes necessary to allow the two carries from the four-bit adder to enter the memory elements unaltered.

For ease in comparing the decimal values of the array at start and finish, the tabulation starts in the upper left and progresses downward to the bottom of the page, thence to the bottom right of the page and upward to the finish.

For this example bits in positions "3" and above represent whole numbers and in positions "1" and "2" represent fractions.

MATHEMATICAL ANALYSIS

As indicated previously this processor employs the fixed point binary system of notation. The sign bit occurs in the highest order position. A one is used to denote positive numbers and a zero represents negative numbers which are expressed in complement form.

In mathematical notation any number may be represented as:

$$a_0a_1a_2a_3 \ldots a_ja_k \ldots . a_n \qquad (8)$$

where a_0 is the sign bit and $a_1 \ldots . a_j$ are the binary representation of the whole part of the number and $a_k \ldots . a_n$ are the binary representation of the fractional part of the number.

Any positive number may then be described by the formula:

$$X = 2^j \left(1 + \sum_{i=1}^{n} 2^{-i}\, a_i\right) \qquad (9)$$

and any negative number by the same expression with the sign reversed, where the summation is the positive representation of the number. The effect of this notation is that every number used in the computation has added to it 2^j. A positive number thus is represented by a number 2^j greater than the desired number and a negative number is represented by a number equal to 2^j minus the desired negative number.

Now consider a set of numbers x_1,x_2,x_3,x_4 where $-1 \leqq xi \leqq 1$.

These numbers may then be described by the formula:

$$X_i = 1 + x_i \qquad (10)$$

which is the machine notation used in the processor.

Entering these four numbers in the processor results in

$$x_1 + x_2 + x_3 + x_4$$

being represented by

$$X_1 + X_2 + X_3 + X_4$$
$$= (1 + x_1) + (1 + x_2) + (1 + x_3) + (1 + x_4)$$
$$= 4 + (x_1 + x_2 + x_3 + x_4)$$

After the addition is performed a divide-by-four operation occurs so that

$$\frac{X_1 + X_2 + X_3 + X_4}{4} = 1 + \frac{x_1 + x_2 + x_3 + x_4}{4} \qquad (11)$$

which is the machine notation for the arithmetic mean of

$$x_1 , x_2 , x_3 , x_4$$

The following lemma with its proof is applicable to this operation:

Lemma: If $x_1, x_2, x_3, \ldots . x_n$ are real numbers with an average $A = (x_1 + x_2 + x_3 + \ldots . x_n)/n$, and if B is any real number, then A + B is the average of the numbers $x_1 + B, x_2 + B, x_3 + B, \ldots . . x_n + B$.

Proof:
$$\frac{(x_1 + B) + (x_2 + B) + \ldots . . + (x_n + B)}{n}$$
$$= \frac{(x_1 + x_2 + x_3 + \ldots . . + x_n) + nB}{n}$$
$$= A + nB/n = A + B \quad \text{Q. E. D.}$$

In the preceding discussion, a system is illustrated in which positive numbers are represented by a one in the most significant bit position and negative numbers by a zero in the most significant bit position, using, of course, the complement representation of negative numbers. This results, as has been shown, in the machine notation for the average of four numbers to be consistent with the machine notation for each of the numbers entered into the machine. Thus it is possible to perpetually reiterate the machine computation without giving any consideration to whether the numbers are negative or positive for they will always be in the correct notation whether negative or positive. Zero, in this system, will always be represented as a positive number.

Consider now the customary system in which a zero represents a positive number and a one represents a negative number. This results in the following condition:

If $x \geqq 0$, let x represent x
If $x < 0$, let $2 + x$ represent x

Further consider that there are four numbers which are to be averaged, x_1 and x_2 which are $\geqq 0$, and x_3 and x_4 which are < 0. The machine notation for these numbers then is:

$x_1 = x_1$; $x_2 = x_2$; $x_3 = 2 + x_3$; and $x_4 = 2 + x_4$

The machine average of these four numbers then is:

$$1 + (x_1 + x_2 + x_3 + x_4)/4 \qquad (12)$$

which is not interpretable as 2 + Sum/4 (negative) or Sum/4 (positive). Thus it is seen that the customary notation does not lend itself to the automatic reiteration process.

THE FOUR-BIT ADDER

A block is included in Fig. 6 labeled 4-bit adder. This device has as its function the binary addition of four bits of information simultaneously. Such a unit used in conjunction with the divide-by-four circuitry mentioned previously very effectively accomplishes the required computation. The four-bit adder is an extension of the work done by Watson on a three-bit adder.[13] The circuit is shown in Fig. 7. Inputs to the adder are obtained from the four terminals, "R", "B", "T" and "L". These data come from the outputs of the right, bottom, top and left adjacent processing elements respectively.

The four-bit adder is composed of three full-adders, a half-adder, and three units of delay. One output is provided.

In operation the adder unit requires that two sets of zero bits be introduced subsequent to the addition of the regular data bits. This allows the carry and sum outputs from the lower full-adder to appear in the output in their proper arithmetical positions.

It has not been mentioned previously but it should be noted that data is processed through the shift register and the adder unit with the least significant bit first.

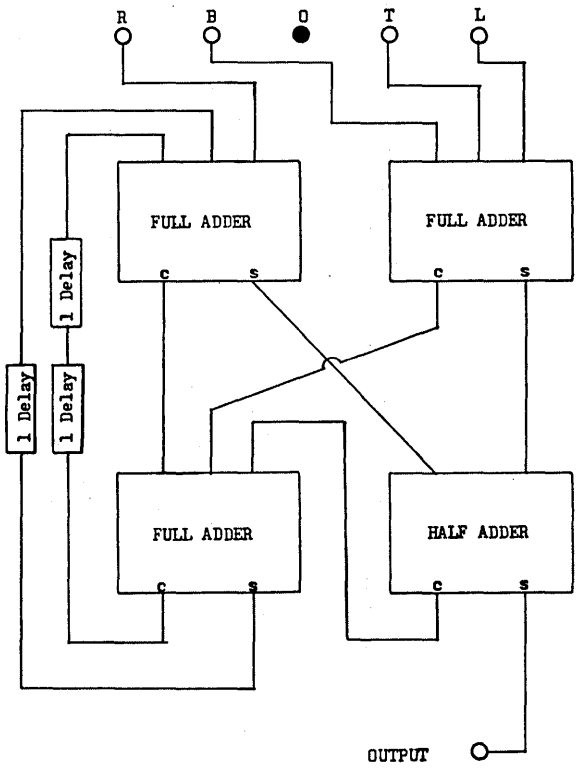


Fig. 7 Four-bit adder.

A study of the circuit of Fig. 7 will reveal that any single input will cause an "s" output from one or the other of the top full-adders and an "s" output from the half-adder. Two inputs will produce either a "c" output from the right top full-adder or two "s" outputs from the top full-adders, either case producing an "s" output from the left lower full-adder, with the effect of a carry to the next more significant bit. Three inputs will produce an "s" and a "c" from the top full-adders resulting in an "s" output from the half-adder and an "s" output from the left lower full-adder, having the effect of a one in both the immediate bit and the next most significant bit. The one remaining case of four bits results in an "s" in the top left adder and both an "s" and a "c" in the top right adder, ultimately producing two inputs to the lower left full-adder, a "c" output which effects a carry to the second more significant bit. Further perusal will show that the carries will add in correctly to produce the desired results.

INTERCONNECTIONS

It is beyond the scope of this work to detail all of the interconnections required to make the system operable. Of special interest, though, is the simplicity with which the connections may be made to interconnect each processing element to the four adjacent elements to provide the input that the adder requires to accomplish its computation.

Figure 8 shows how a printed circuit board might be laid out to accomplish this task. The outputs from each array point are shown by the black dots. Inputs to the 4-bit adder associated with each array point are located at the two terminals on each side of the output terminal. The sketch shows clearly how each array point distributes its data to the four adjacent array points and also how an array point receives its data from the adjacent array point outputs.

A layer of 100 processing elements in a row would then have its 500 connections completed by a circuit board as shown.

While not attempting to detail all of the interconnections it may be well to note several sets of connections that will be necessary in order to make the system operable.

With reference to Fig. 5, the following interconnections are required:

a. The Shift-Driver must be connected to provide the shift signals to every processing element. The driver must also be designed to provide exactly N + 1 pulses for every iteration. A space equal to at least two pulses is also required between iterations to clear the shift pulses through the delay units in the divide-by-four circuitry (Fig. 6).

b. The Clear-Driver must be connected to each and every memory element to enable complete zero-setting prior to the performance of any calculation.

c. The X Address Register and the Y Address Register need appropriate connections to the vertical and horizontal lines of computing elements respectively. This might be done by a printed circuit board with horizontal conductors on one side and vertical conductors on the other side. Each processing element would then be connected to the appropriate x and y conductors. Simultaneous signals on both conductors would activate an AND gate to ready the processing element for write-in or read-out of information.

d. The Read-Write unit requires connections to all of the "0" memory elements from its "0" read-write element. Likewise, each of the read-write elements must be connected to all of the corresponding memory elements. Appropriately connected AND gates all any processing element to be selected.

THE PROCESSOR IN OPERATION

The steps to be followed in solving a boundary-value problem using Laplace's equation in two dimensions are as follows:

a. Operate Clear Driver. This operation clears all of the memory elements in the processor. The processor is now ready to receive data for the problem to be solved.

b. Write-in boundary values. Using the X and Y address registers and the Read-Write unit write-in N−1 data bits for each boundary processing element. Write-in a one for the "0" memory element. This puts the data into the machine ready for computation and assures that the data will not be altered in the process of the computation.

c. Set exterior elements to Hold mode. Since processing elements exterior to the boundaries will not enter into the computations their "0" mode bits must be set to one so that they will hold their zero values throughout the computation period.

d. Compute. In this step the Shift-Driver is caused to operate, providing N + 1 pulses for each iteration separated by the space of at least two pulses. This cycle may be repeated as many times as is required to attain the desired accuracy of final result.

e. Check accuracy of results. This is accomplished by interrupting the compute cycle at appropriate intervals and reading-out a selected set of values at the points being computed. These values are then compared with previous values obtained for the same points. When the values no longer change a solution has been reached. In general, no-charge will be taken as a change less than stipulated minimum value.

f. Read-out computed data. Having operated in the Compute mode a sufficient number of times to attain the desired accuracy of results, all that remains is to

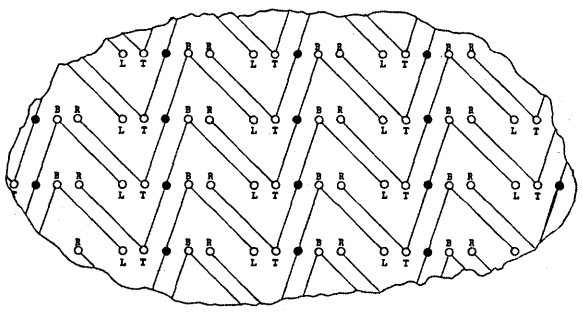


Fig. 8 Section of possible printed circuit interconnection board.

read-out the data. This is done by addressing the proper processing elements and operating the Read-Write unit in conjunction with the selected output device such as a printer, plotter or tape unit.

Several operational considerations should be noted in connection with the logic employed in the circuitry presented here. The system will handle negative as well as positive numbers with equal facility. If it is desired to use both types of numbers the simple expedient of using the highest order digit as a sign digit and expressing negative numbers in twos-complement form renders the system operational. It should be noted that the divide-by-four circuit makes it necessary to represent positive numbers with a one and negative numbers with a zero. Thus done, the circuit performs the required calculation without error, the binary ones automatically giving the sign and magnitude of the mean of the four points surrounding the array point being computed.

Another point of interest is that the system never can perform a computation resulting in an overflow. This is the natural consequence of the fact that the equation being solved can have no values greater than the maximum positive boundary value and no values less than the minimum negative boundary value. Thus, data capable of causing an overflow would be detected prior to being loaded in the array processor.

CONCLUSIONS

Certain types of problems such as the numerical solution of partial differential equations do not lend themselves to economical solution on general purpose uniprocessor computers. This has led to the expenditure of large sums of money for the development of parallel processing machines such as SOLOMON and ILLIAC IV. IBM has pushed the state of the art in their System 360/91 which can handle over a billion bits of data per second, thus placing them in an excellent position with respect to parallel processors in the computer field. This computational speed is, however, rapidly approaching a limit for uniprocessor techniques.

For comparison with a general purpose computer it is noted that the techniques required to load the memory of either computer, the general purpose computer or the computer described herein, are much the same. Both could be loaded by parallel data bits from magnetic tape. The loading time and the unloading time would both be much the same and alike for both machines. The difference in speed would show up in the array computation. This machine has the capability of handling 500 bits of data per second using components rated for 50 MHz operation which are readily available, assuming an 100 x 100 array. Thus, for the computing phase of the operation over two orders of magnitude improvement in computing speed have been realized over an optimized general purpose computer. The system as described could readily be extended to larger array sizes to attain still higher speeds.

In this study of array processing, limits were definitely set on the flexibility of the unit. This has resulted, for the moment, in a system which is strictly single-purpose. Doing this has made it possible to exploit a number of extremely efficient computing techniques: the four-bit adders for each array point, the divide-by-four operation performed by a dual shift, and the use of the memory actually as computing registers, thereby making possible the mass withdrawal of information from the memory and restoring it to memory.

The system as described would be bulky and undoubtedly quite expensive if it were to be constructed of the usual components or even customary integrated circuits. Since all of the basic processing elements are identical, production economics would be expected. Further, large scale integrated circuits are approaching reality, which would mean that many of the processing elements could be fabricated at one time, perhaps the 100 elements required for a single plane so that 100 such planes could be stacked to provide the total array. Thus, immediately forseeable improvements in the state-of-the-art will make the system as described quite feasible.

Undoubtedly, as is usually the case, others will desire greater flexibility. Further study will probably show that some additional flexibility may be attained by rather simple modifications.

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Digital computer reliability can be enhanced by circuit redundancy. Several techniques for accomplishing this are discussed in this article.

INCREASING RELIABILITY OF DIGITAL COMPUTERS

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This article surveys various techniques that have been developed to increase the reliability of digital computers by adding redundancy to their circuitry. A historical survey of the impact of evolving circuit technology on the use of redundancy is followed by a discussion of two important topics in redundancy application, concluding with a critical review of several techniques.

Early digital computers were constructed with relays which caused great emphasis to be placed on self-checking and self-correcting logic designs due to the very high intermittent failure rate of these devices. This emphasis continued when vacuum tubes replaced the relays in digital logic circuits.

The second generation of computers heralded the introduction of transistorized circuitry. The transistor has no inherent failure mechanism as does the vacuum tube; therefore, when the transistors with manufacturing defects have been removed from the computer, it should operate with a very low failure rate for an extended period. Experience has borne out this expectation. Because of this greater reliability, the second generation of digital computers brought with it diminished emphasis on redundancy techniques, although basic theoretical work continued.

The third generation of computers features the use of hybrid and integrated circuits for logic functions. These circuits greatly reduce the number of wired interconnections that must be made in a computer, further increasing reliability over discrete solid-state circuits. And along with these new, more reliable circuits has come increased emphasis on redundant design techniques. This has resulted primarily because of two applications that require reliability levels that cannot be achieved with nonredundant designs—on-line commercial processing and deep-space exploration. On-line commercial applications require processing of requests for service as they arrive; if failures occur, processing must continue while repairs are being made. In deep-space applications, the computer must maintain a specified level of computing capability with a high probability over an extended period without direct human intervention.

REDUNDANCY APPLICATION

Techniques for redundancy application can be classified into two broad groups, signal redundancy and hardware redundancy.[1] Signal redundancy is the practice of adding redundant information to signals that are manipulated or stored within the machine. Hardware redundancy is the addition of redundant circuits to process signals without changing the structure of signals themselves. Each of these categories can be further subdivided into "on-line" and "off-line". If the redundant circuitry functions during normal operation of the computer, the redundancy can be called on-line. If the redundant circuitry does not function during normal computer operation, the redundancy is said to be off-line. This use of these terms originates with this article.

Before reviewing particular redundancy-application techniques, two important topics in redundancy application must be considered—the level of application and stratification.

Level of Application

Redundancy can be applied at various levels; the level of application greatly influences multiple-failure vulnerability. Consider as an example the technique of duplication. As shown in Fig. 1a, let M be a non-

redundant computer composed of modules M1, M2, and M3. Because M is nonredundant, any single failure in M1, M2, or M3 will cause the computer to fail. Suppose now that M is duplicated at the system level, as illustrated in Fig. 1b, by the addition of a duplicate machine M′ which is constructed of the modules M1′, M2′, and M3′ (for simplicity, ignore the problem of selecting the correct output). No single failure in M or M′ can now disable the system. Further, no multiple failure in M alone or in M′ alone will cause system failure. Any single failure in M plus any single failure in M′, however, will cause system failure.

Now let M be duplicated at the module level, as shown in Fig. 1c. The same amount of additional hardware has been added; however, the selection of correct outputs now occurs at the module level. The system is now invulnerable to all single failures and all double failures except simultaneous failures in M1 and M1′, M2 and M2′, or M3 and M3′. Thus, changing the level of application of redundancy has vastly increased the computer's tolerance of multiple failures.

It might seem, therefore, by a straightforward extrapolation of these arguments, that component-level redundancy would be the ideal level of application; however, this is not the case. In the discussion above, the problem of selecting the correct output was ignored. In practice, however, performing this function requires additional circuitry. As the level of application lowers, the amount of circuitry performing this selection process becomes greater, relative to the size of the modules that comprise the machine itself. Therefore, after a certain point, the reliability of this selection circuitry begins to dominate the reliability of the computer. Thus, the optimum point for level of application lies somewhere between the component and system level. The techniques of redundancy application discussed later in this article will illustrate some choices of level of application that have been made.

Stratification

The second general topic in redundancy application discussed in this paper is stratification. A machine is said to be stratified if there exists at least one circuit whose operation is not checked by some other circuit. The circuits of a stratified machine, then, can be classified into strata—checked and unchecked. An unstratified machine contains only checked circuitry. Diagnostic programs often assume that some portion of the machine is failure free; this is usually called the hard core. The hard core assumption is sometimes justified by constructing that portion of the machine from ultra-reliable components, or by making that portion of the machine more redundant than the rest of the machine.

REDUNDANCY APPLICATION TECHNIQUES

Signal Redundancy

As mentioned earlier, signal redundancy is applied by adding redundant bits to information that is stored or transferred within the computer. The redundant information can be used to detect or correct errors.

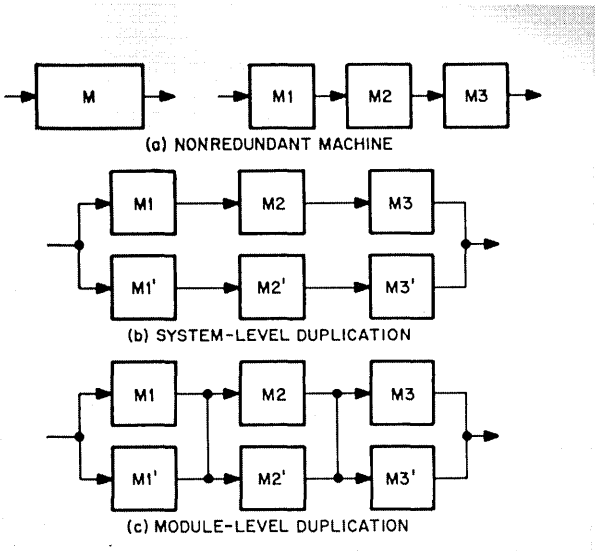

Fig. 1 Level of application.

These techniques were originally developed for use in noisy communication channels;[2] their use in computers has been confined mostly to those areas of the computer that are similar in error characteristics to models of the communication channel that have been used for the derivation of the various codes.

Hamming Distance

In discussing the characteristics of binary codes, the concept of Hamming distance is useful. The Hamming distance between two code words is defined to be the number of positions in which the two words differ.[2] For a code to detect up to d errors in one word, the Hamming distance between the two least distant words of the code (the "minimum distance") must be at least d+1. This is apparent from the definition of Hamming distance; if the minimum distance of a code is d+1, no error in d or fewer positions can make the two least distant code words identical, since by assumption these two words differ in at least d+1 positions.

If error correction is to be performed by a code, then correcting d errors requires a minimum distance of 2d+1; if a code word with d errors is received, it will be distance d from the correct word and at least distance d+1 from every other word of the code, enabling the selection of the correct code word.

Magnetic Storage Devices

Two applications in digital computers that resemble certain models of communication channels are magnetic storage devices and information transfer. The two main types of magnetic storage media, ferrite core and magnetic oxide, have different error characteristics. Core memories occasionally suffer errors in one or two bits of a word due to noise or marginal circuit performance; on the other hand, errors in oxide layer storage devices are often due to flaws physically great enough to cause several simultaneous errors. Thus, single parity checking is often used for core memories,

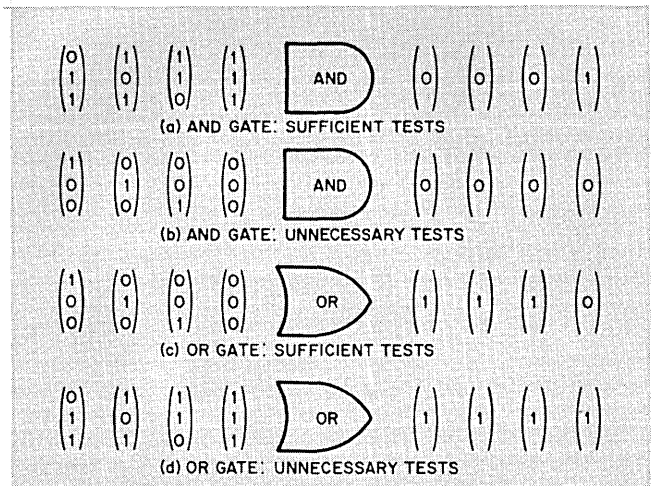

Fig. 2 Fault tests for combinational circuits.

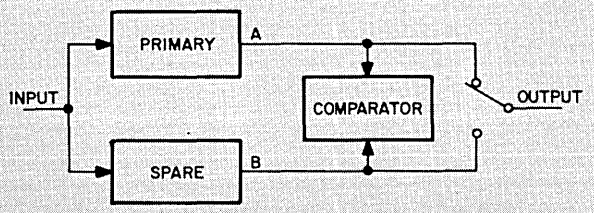

Fig. 3 Spare switching technique.

while double parity checking, a minimum distance three code, or various burst codes capable of detecting bursts of errors, are used for oxide-film storage devices. In more recent computers, the quality of magnetic recording media has reduced error rates so much that double parity checks are usually sufficient for error detection, eliminating the need for the use of the inefficient burst codes.

Information Transfer

The second major area of application of binary coding in digital computer design is in information transfer between the central processor and various input/output devices. These transfers are subject to random single-bit errors caused by noise, very nearly approximating the ideal binary erasure channel. For this application, single (or occasionally double) parity checking is usually used to give single- (or double-) error detecting capability.

There are several reasons why error-correcting codes have not found wider application in digital computers. Some of them are:[1]

1. The most probable types of error in a digital computer are not the same as for a communication channel. In particular, if an error in a digital computer was due to a circuit malfunction, it is very likely that another error will occur in the same bit of the word at another time.
2. Most binary codes are not compatible with arithmetic operations.
3. Coding and decoding schemes developed for communication codes do not allow for errors in the coding and decoding circuits; the computer application requires that this be taken into account.

Hardware Redundancy

In contrast to the signal redundancy techniques discussed above, hardware redundancy adds redundant circuitry to the computer without changing the characteristics of the information transfer and storage within the machine. Thus, the word length of the computer is not increased by the use of hardware redundancy; each word may be processed by more circuitry.

Applications of hardware redundancy generally fall into two categories: spare switching and masking. Masking uses the correctly-operating neighbors of a faulty element to continue correct operation; spare switching replaces the faulty element with an identical spare. Both masking and spare switching have been applied at various levels.

Spare Switching

Spare switching techniques consist of two separate operations; locating the inoperative module and switching in its spare. Adequate methods have been developed for testing combinational circuits; one example of these was described by Maling and Allen.[3] A combinational gate of n inputs can be tested in this way by the application of a sequence of n+1 inputs; Fig. 2 illustrates the method for gates of 3 inputs. For the AND gate, the sequence of inputs shows that any single input can turn off the output, and that the output is on if all inputs are on. Fig. 2a shows the sufficient tests for an AND gate; Fig. 2b, the unnecessary tests for this gate, along with the correct outputs for each test. It is interesting to note that, because of De Morgan's Law, the unnecessary tests for the OR gate are the necessary tests for the AND gate, and vice-versa. Maling and Allen also showed that combinational circuits of any number of gates can be tested by input sequences of this kind, provided the circuits contain no redundancy.

Unfortunately, no method as simple as the one described above has yet been developed for testing sequential circuits.[3] The methods that have been described in the literature usually lead to tests of impractical length, or require excessive amounts of additional hardware to perform the checking. If a satisfactory method for checking sequential circuits is devised, spare switching will become a much more attractive method of adding redundancy to computer design.

An example of spare switching at the circuit level is the technique developed by Cole and Zimmerman.[4] In this technique, the spare unit is also used for fault detection by comparison with the primary unit, as shown in Fig. 3. When the comparator signals an unequal compare between signals A and B, processing is halted, and execution of diagnostic programs is begun.

If the diagnostics indicate improper operation, then the primary unit has failed, and the switch on the output is thrown. If the diagnostics find no error, then the failure was either the spare circuit, the comparator circuit, or a transient error of the primary circuit; a message to the repairman is printed. This approach to spare switching is practical if maintenance is available. The diagnostic program does not have to perform fault location, since the comparator has located the fault. This approach to reliability enhancement provides substantial increase in reliability at minimal cost in additional circuitry.

An example of spare switching at various levels is the Variable Instruction Computer developed by RCA.[5] Within the processor, switching is at the module level; in the memory, switching takes place at the system level. The computer is called "variable-instruction" because these three characteristics of an instruction are varied in response to failures within the computer:

1. source of information for the operation;
2. sequence of operations performed on the information;
3. destination of the results.

The memory contains instructions that are actually macro-instructions; each one specifies a sequence of micro-operations. In case of some failure in the processor, the parallel arithmetic unit is arranged in partial-word modules so that operations can be performed by using the part of the circuitry that still operates, and shifting the operands and results appropriately. When a failure occurs, a degraded micro-instruction sequence can replace the original; in this way, the execution of an instruction can actually change in response to system changes.

The memory unit of the VIC is duplicated; the two modules are completely independent, including their power supplies. All memory accesses are normally performed from the primary memory module; however, storage operations are performed in duplicate on both modules. If a parity error is detected on a fetch from the primary module, then the fetch is transferred to the spare module. This spare switching technique is practically identical to the method of Cole and Zimmerman adescribed above, except that the redundancy has been applied at the system level instead of the module level. The basic elements of Fig. 3, namely the duplicate modules, comparator, and switch, are present in this scheme; each memory module corresponds to a logic module, the comparator function is performed by parity check, and the switch is implemented in the processor.

Masking

Masking techniques use the properly-operating (redundant) neighbors of a faulty device to mask its errors. The first use of masking techniques applied to computers is due to Moore and Shannon[6]; they suggested that networks of relays be used to perform with greater probability of correct operation than a single relay. Because each device of a semiconductor circuit

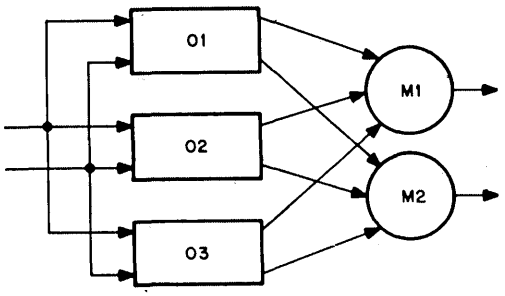

Fig. 4 Triplication.

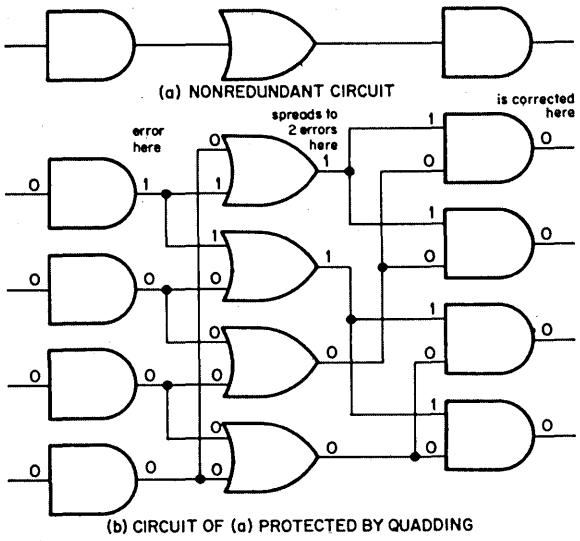

Fig. 5 Quadding.

does not have the same failure probability in a circuit with other semiconductor circuits that may also fail as it does alone and since individual semiconductor devices are not subject to the high dynamic failure rates of relays, these techniques of component-level masking have fallen into disuse, and are not discussed at any greater length in this article.

The form of masking generally in use today was described originally by von Neumann[7]. He described the use of multiple copies of a circuit, each receiving identical inputs; the resultant output of a majority of these is assumed to be correct. Von Neumann pointed out that there could be an arbitrary number of redundant circuits and voting circuits. Figure 4 illustrates triplication of machine O with duplication of voting circuits M.

Tryon further developed von Neumann's basic idea in his development of quadding[8]. These three principles form the basis for quadding:

1. All logic appears in quadruplicate
2. Every error is corrected just downstream of the fault that caused it
3. Correction is accomplished by good signals from neighbors of the faulty unit.

Figure 5, which shows the protection of a circuit by

quadding, illustrates how these ideas are implemented. Although the circuit is trivial, consisting of two single-input AND gate in series with one single-input OR gate, its complexity is sufficient to illustrate this technique. The example shows an error in the first AND gate; this propagates to two errors through the OR gates, and is then corrected by the correct signals in the final stage of AND gates.

Tryon points out that quadding can be derived from von Neumann's original scheme of replication and majority voting if the replication and voting circuits are all quadruplicated and then the logic of individual gates and the logic of the majority voters is merged wherever possible.

Another interesting masking technique is due to Russo[9]. This technique uses a minimum distance three state assignment to design a counter that is invulnerable to any single failure. If the states of the circuit are considered as code words, any word with an error in a single position can be associated with the correct word, as pointed out in the discussion of Hamming distance that appears earlier in this paper. Russo restricts the possible class of single failures by making a few assumptions that limit "single failures" to failures that produce an error in only one bit of the state-word; he then shows a design technique to perform the correction when an error occurs.

COMPARISON OF SPARE SWITCHING AND MASKING

The advocates of spare switching and masking both claim superiority for their methods. An attempt is made here to present and objectively evaluate their claims.

A redundant system using masking will continue operating without interruption unless there is some catastrophic failure of the system; spare-switching is a time-consuming process, because of the difficulty of fault diagnosis and location. The masked machine has no need for any kind of diagnosis during operation; the redundant protection is always operating, and will function to remove transient errors. Further, a system using masking is unstratified; every part of the machine is checked.

On the other hand, spare switching also has certain advantages. Power consumption of the redundant system can be reduced by supplying power to the standby units only after they have been switched into the circuit; this practice also reduces the failure rate of the standby circuits, because power-off failure rates are much lower than power-on failure rates for semiconductor circuits. Spare switching also avoids the reduction of circuit tolerances produced by the increased fan-in and fan-out required of circuits for use in a system protected by masking. Theoretically, a system using spare switching will operate properly if one copy of each circuit operates correctly; a masked system can fail and still have embedded within it enough properly operating components to form one whole machine.

Thus, both techniques have their advantages. One practical problem, debugging, is a handicap to the use of masking; it is very difficult to determine whether all the components of a system protected by masking are operating correctly. Usually the difficulty is relieved to some extent by placing the several copies of the system on separate power supplies, so each can be checked out individually. This still leaves substantial difficulties connected with the interaction of the various copies of the system.

The problem of pre-mission verification ascribed to masking has its counterpart in spare switching in the diagnosis problem, as discussed above. Therefore, neither method of redundancy application is clearly superior, and a choice must be made for each application, with consideration for the various constraints involved. In general, where manual maintenance is to be performed, spare switching is to be preferred; the system with spare switching can be repaired by replacing faulty components while they are switched out of the system. The masked system will not indicate a circuit failure until the whole system has failed. If no maintenance can be performed, the choice of a redundancy scheme would seem to depend on the details of the mission of the computer.

CONCLUSION

What, then, is the future of redundancy techniques? Today the cost of the logic circuitry of a computer represents less than 20% of the cost of the system. Doubling this cost to achieve a reliability increase of hundreds of per cent would not significantly affect the total cost of the computer system. In fact, it may be less expensive to build highly reliable computers from redundant, unreliable, inexpensive circuits than from nonredundant, highly reliable, expensive circuits.[10]

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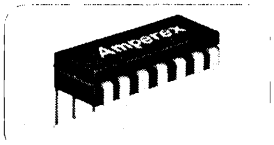

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This article discusses the use of redundancy, and in particular, triple modular redundancy for error detection and fault isolation.

REDUNDANCY FOR BETTER MAINTENANCE OF COMPUTER SYSTEMS

Michael Ball
Fred Hardie

IBM Corp.
Owego, N. Y.

A number of articles have been written about the use of redundancy in aerospace digital computing systems to improve reliability.[1] Less attention has been given to the use of redundancy for automatic error detection and fault isolation. In fact, many authors have referred obliquely to the increased maintenance problem resulting from the adoption of redundant configurations.[2]

Although error detection and diagnosis are complicated by some forms of redundancy that mask the effects of component failures, hardware redundancy can be configured which can simplify maintenance tasks rather than complicate them. Specifically, the organization of a digital system into two or more parallel data paths or channels provides the capability of error detection by data comparison at related points in each channel. Strategic location of these points can provide an automatic fault isolation capability as well.

ERROR DETECTION

The following paragraphs describe the instrumentation of specific schemes for automatic error detection and diagnostic functions in a triple modular redundant (TMR) digital computing machine organization. Figure 1 shows the operation of two-out-of three voting in a TMR network. The voter operates as a current summer feeding a threshold circuit. Two units of current from any two of the three channel inputs are required to operate the threshold circuit.

A failure is indicated in Module 2/Channel 3 by the dotted output lines from the circuit block. The input set of signals to each of the following voter circuits in all three channels consist of two good signals (solid lines) and one bad signal (dotted line). Since the output of each voter is determined by a majority vote of three input signals, the input signals to Module 3 on all three channels are correct. That is, the effects of a circuit failure in Module 2/Channel 3 logic block have been corrected.

Error detection is provided by placing disagreement detectors (DD's) at the channel inputs to the voters. The detectors compare the channel signals and generate an error signal if all three channel signals are not logically identical. A three-input exclusive-OR circuit will satisfy this function.

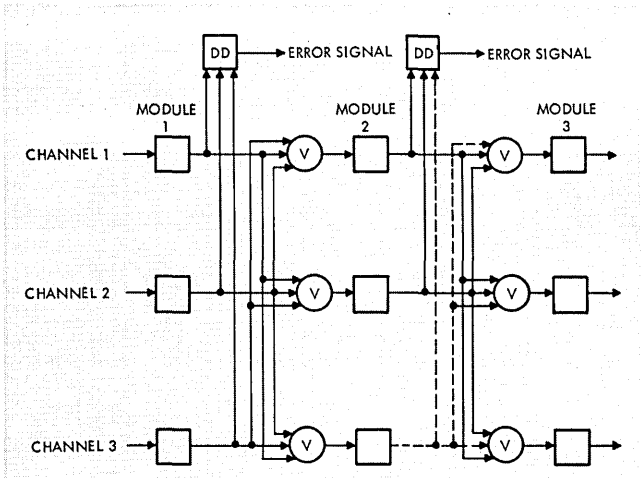

Fig. 1 Triple modular redundancy voting.

This signal comparison technique provides the following advantages over many other approaches to error detection:

1. Continuous monitoring of system performance, as opposed to periodic test problems, reasonableness checks, or system checkout programs.

2. Monitoring of the partially processed data as well as input/output data by means of detectors placed internally in the system. This capability is used for fault isolation to relatively low levels of equipment organization, as in the arithmetic unit of a computer. With early detection of the error, errors may be prevented from propagating into critical areas of the system and causing a system failure or perhaps generating a catastrophic command.

3. High confidence in the error detection and diagnosis functions. Since the effectiveness of these functions depends only on the proper operation of the detection network and not on prior knowledge of computer operation (preprogrammed operations), equipment performance tolerances (test problems or checkout programs), or computer performance tolerances (reasonableness or operational checks).

4. Provides an error detection and fault isolation capability that does not require any interruption of system operation.

5. Provides a potential capability to respond automatically to internal and external stimuli by dynamic reconfiguration to adapt more precisely to specialized functions or to provide graceful degradation.

DESIGN EXAMPLE

In one computer configuration (Saturn Launch Vehicle Digital Computer), disagreement detectors were used to monitor the three signal channels at approximately 170 points in the digital data flow of the computer. The signals were sampled when the input signals to the detectors had reached a steady-state condition to avoid false alarms due to slightly different channel response times. The detection circuit was essentially a logical exclusive-OR followed by an inverter driver circuit. The outputs of the disagreement detector drivers were selectively OR'ed into eleven bit positions of an error storage register. This stored error data was used to isolate failures.

Isolation is feasible since the selective OR'ing of disagreement detectors partitioned the computer into eleven diagnostic modules. At present, no clearly defined ground rules exist for partitioning electronic units into diagnostic modules. Logic simulation techniques have been used, to determine the characteristics of failed machines and the nature of error propagation in digital systems. With this information the detectors may be selectively OR'ed, once the disagreement detectors are optimumly positioned.[3]

SIMULATION

The logic of the computer was simulated to determine the effectiveness of the error-detection placement. The simulator was controlled by a specially written test program that exercised all computer components at least once during the program cycle. Of several hundred simulated component failures, less than one percent were undetected by the disagreement detectors during one cycle of the test program.

Although the detection network operates in parallel with the operational program, a periodic checkout of the system is desirable, using a special test program such as employed in the simulator to assure that infrequently used components are tested. A self-test error detection program for a redundant computer of moderate complexity would consist of less than a hundred instructions.

FAULT ISOLATION

The disagreement detectors are clocked every like-clock time, while most of the computer logic is used periodically under program control. As a result, detectors sense for disagreements between simplex modules of TMR trios even when those modules are not being used by the program. Extensive error propagation through the computer tends to be sensed by many detectors, even though these detectors are not directly associated with the logic containing the fault; thus, the source of the error is masked by over detection.

Despite the over-detection characteristic of the detector network, diagnostic resolution to a replaceable module level was achieved by storing the program instruction and computer time of the first detection of an error. An analysis of the simulation results showed that:

- 53 percent of the failures could be identified by knowing what disagreement detectors sensed the failed conditions.
- 41 percent of the failures could be identified by also knowing the program instruction and computer execution time.
- 6 percent of the failures could not be identified.

By redesigning and rearranging the disagreement detectors, a detector network was developed in which all but a very small class of failures could be identified by knowing only which disagreement detectors sensed the failed conditions. Fault isolation to the module and channel was thus obtained.

In the revised detection network, the three-input exclusive OR detector circuits were replaced with two-input types. The redesigned detectors were placed across each voter rather than across the TMR channels. The detector outputs were then OR'ed along each

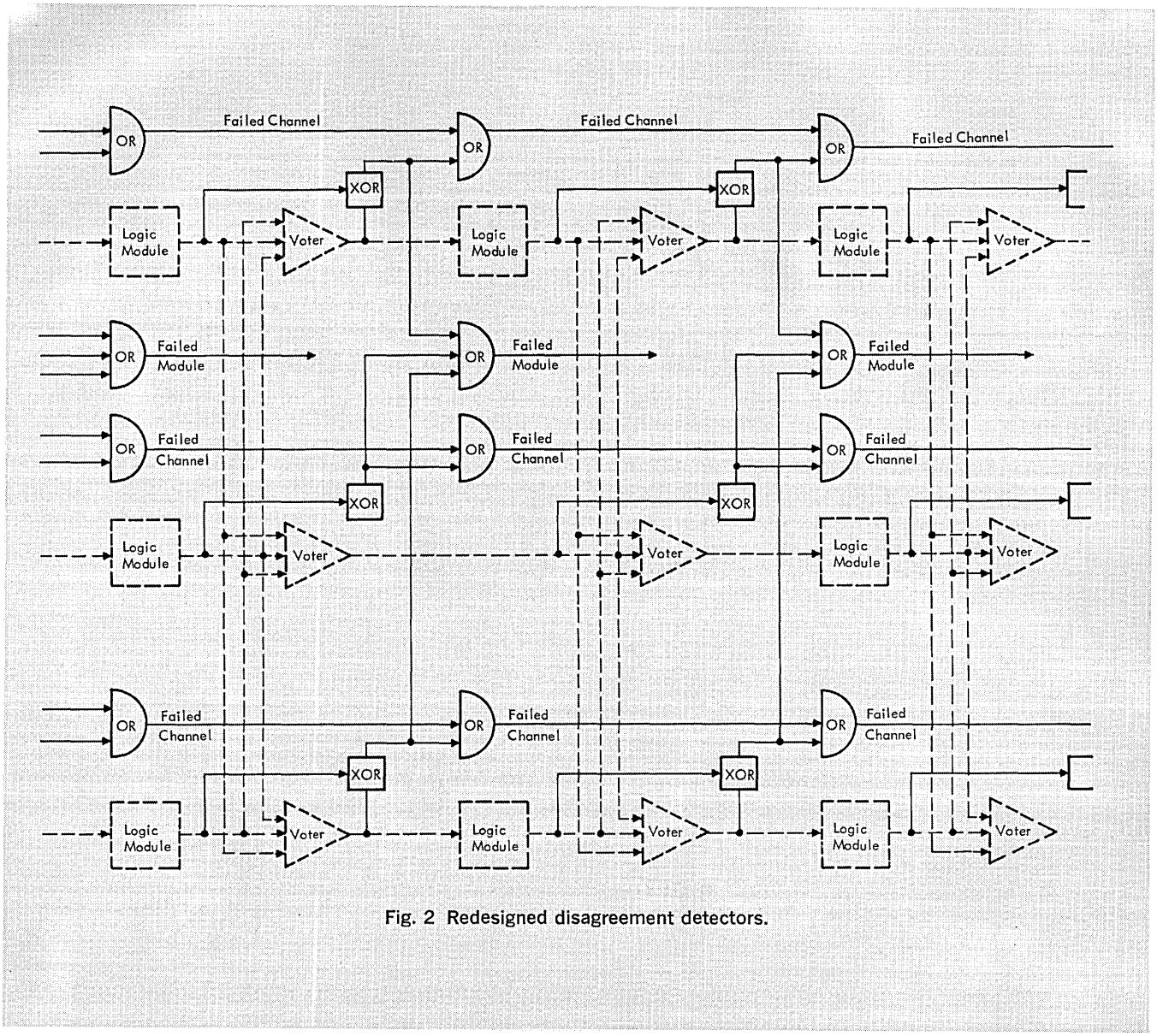

Fig. 2 Redesigned disagreement detectors.

channel (indicating the module containing the fault). See Fig. 2 for interconnection details.

CONCLUSIONS

IBM found that hardware redundancy as a means of error detection and fault isolation could simplify the required maintenance functions. The signals generated by the disagreement detector network indicating the channel and module locations can be used in several operational ways, including:

1. Panel indication of the specific module containing the fault and requiring replacement.

2. Initiation of automatic switching to replace the faulty module with a built-in spare.

3. Initiation of a change in mode or computer organization to by-pass the faulty circuit.

4. Ability to respond to input errors by dynamic reconfiguration or program change to continue operation in alternate and perhaps degraded modes.

5. Ability of the computer to supervise itself in real-time applications.

Consideration is now being given at IBM to the use of redundancy in coming generation computers primarily for easing maintenance operations rather than improving reliability.

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TECHNICAL NOTE

IMP—A TOOL FOR MEMORY SYSTEM EVALUATION*

Bernard Sklar

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In evaluating the performance of a memory system, many different parameters should be considered in order to select the optimum system for a given application. Usually one or two of the performance variables loom heavily in the decision making, outweighing the others, or causing them to be totally neglected. For example, the selection might be unduly influenced by the price, or perhaps the speed or the packing density. With many variables involved it is often difficult to evaluate different systems in the same manner.

A "standard" measure is desired by which any type memory for a certain application can be compared with other types for the same application. The purpose of this paper is to describe an Index for Memory Performance (IMP) which enables one to establish a figure-of-merit for different memory systems.

The formula was developed empirically on the basis that cost and speed are the most important variables. After them, come MTBF, element density and tolerance to environmental stresses. Finally we have power consumption and MTTR. The NDRO memory is considered for several reasons (some psychological) to have an inherent edge over DRO in many system applications. This edge has been heuristically fixed at 20 percent. For certain space applications, the improvement that NDRO has over DRO will be considerably greater than 20 percent.

The IMP presented here was formulated with an airborne computer in mind. However, the general technique can be considered as a flexible methodology when comparing memory systems for many other applications. It is not intended to be a hard-and-fast rule for all situations. For some applications, speed is not at all pertinent, and it would therefore be desirable to use a less sensitive weighting for that variable. Also, ground systems, for example, do not put the same premium on element-packing-density that airborne systems do, and so a modification in the weighting of this parameter would be in order for such an application.

The figure-of-merit is based on eight essential variables which help contribute to a system's effectiveness (or to its shortcomings). These variables are as follows:

1. "C" in cents/system bit (which in itself depends on several variables)
2. "S" in microseconds (cycle time)
3. "D" in system bits/cubic inch (packing density)
4. "M" in thousand hours (MTBF)
5. "R" in hours (MTTR)
6. "T" tolerance to environmental stress graded from best to worst
7. "P" power consumption in watts (under normal operating conditions)
8. "N" = 10.0 for DRO
   "N" = 12.0 for NDRO

The formula for the index can be stated as follows for a military airborne memory system:

$$\text{IMP} = N\left[\frac{M + \frac{D}{100} + T}{C + 10S + \frac{R}{10} + \frac{P}{30}}\right]$$

This work was performed while both authors were employed by Litton Industries.

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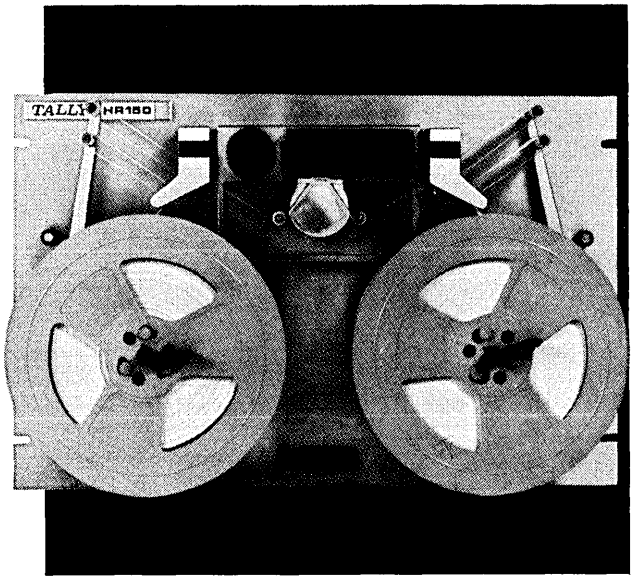

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CIRCLE NO. 26 ON INQUIRY CARD

A different technique for an evaluation formula would be one where each variable is pre-assigned a weighting factor and then the total figure-of-merit is a simple addition of eight terms corresponding to these variables. But the problem with such a series-string is that any major improvement of a single variable can inordinately reflect in the index much beyond its intended weight. It can give the illusion of a memory system superior to all others, based on only one parameter. The index proposed here cannot be "pulled out" so radically by only one parameter.

The cost variable can itself be broken down into several variables, such as:
1. Yield (either batch fabrication or automation)
2. Optimum utilization of yield (the ability to make use of less than perfect wafers)
3. Simplicity of fabrication
4. Memory organization (most batch processes do not lend themselves to coincident-current organization; hence, there may be more electronics for a given size memory, creating higher cost). New cost effective organizations will be created when LSI techniques can be applied to memory electronics.
5. The required memory system speed has, in many cases, a direct bearing on system cost; however, this consideration is included indirectly in the cost variable.

Rather than attempt to pin-point each of these "sub-variables" with a weighting factor, the computer designer can generally dismiss this level of detail and use the composite cost-per-system-bit simply as a number available to him.

Let us now show how the Index of Memory Performance is used for evaluating different present-day, random-access, military systems. It should be stressed that in this particular example today's technology is being considered. The application is a special-purpose airborne computer requiring a 4K x 32 bit memory. It is assumed that the memory can be ground loaded and that the alteration of data while in flight is not necessarily required. Our goal is to obtain a figure of merit for each of the memories under consideration.

The five different memory configurations evaluated are:
1. Core, DRO, (4K x 32 bits)
2. Thin Film, NDRO Read only, Electrically Alterable on ground (4K x 32 bits)
3. Thin Film, NDRO Electrically Alterable in flight (4K x 32 bits)
4. Plated Wire, NDRO Read Only, Electrically Alterable on ground (4K x 32 bits)
5. I.C., NDRO Electrically Alterable in flight (4K x 32 bits)

Core, DRO, (4K x 32 bits)

C = 20 cents per system bit
S = 2 microseconds (read-restore)
M = 16,000 hours MTBF
D = 916 bits per cu. in.
T = 9 (estimates for tolerance to stress)
P = 72 watts average power
R = 5 hours (estimate for MTTR)
N = 10 (assigned for DRO)

$$\text{IMP} = 10\left[\frac{16 + \frac{916}{100} + 9}{20 + 10\ (2) + \frac{5}{10} + \frac{72}{30}}\right]$$

$$\text{IMP} = 7.96$$

Thin Film, NDRO Read Only, Electrically Alterable on Ground (4K x 32 bits)

C = 55 cents per system bit
S = 500 nanoseconds (read only)
M = 17,000 hours MTBF (estimate)
D = 675 bits per cu. in.
T = 8 (estimate for tolerance to stress)
P = 30 watts average power (estimate)
R = 10 hours (estimate for MTTR)
N = 12 (assigned for NDRO)

$$\text{IMP} = 12\left[\frac{17 + \frac{675}{100} + 8}{55 + 10\ (0.5) + \frac{10}{10} + \frac{30}{30}}\right]$$

$$\text{IMP} = 6.15$$

Thin Film NDRO Electrically Alterable in Flight (4K x 32 bits)

C = 70 cents per system bit (estimate)
S = 1 microsecond (read-alter)
M = 15,000 hours MTBF
D = 810 bits per cu. in.
T = 7 (estimate for tolerance to stress)
P = 35 watts average power estimate)
R = 15 hours (estimate for MTTR)
N = 12 (assigned for NDRO)

$$\text{IMP} = 12\left[\frac{15 + \frac{810}{100} + 7}{70 + 10\ (1) + \frac{15}{10} + \frac{35}{30}}\right]$$

$$\text{IMP} = 4.36$$

Plated Wire, NDRO Read Only, Electrically Alterable on Ground (4K x 32 bits)

C = 50 cents per system bit
S = 500 nanoseconds (read only)
M = 17,000 hours MTBF
D = 890 bits per cu. in.
T = 8 (estimate for tolerance to stress)
P = 20 watts average power
R = 8 hours (estimate for MTTR)
N = 12 (assigned for NDRO)

$$\text{IMP} = 12\left[\frac{17 + \frac{890}{100} + 8}{50 + 10\ (0.5) + \frac{8}{10} + \frac{20}{30}}\right]$$

$$\text{IMP} = 7.16$$

I. C., NDRO Electrically Alterable in Flight (4K x 32 bits). (It is as-

sumed that a volatile storage medium is acceptable.)

C = 75 cents per system bit
S = 1 microsecond (read-alter)
M = 13,000 hours MTBF
D = 605 bits per cu. in.
T = 9 (estimate for tolerance to stress)
P = 15 watts average power
R = 5 hours (estimate for MTTR)
N = 12 (assigned for NDRO)

IMP =

$$12\left[\frac{13+\frac{605}{100}+9}{75+10\,(1)+\frac{5}{10}+\frac{15}{30}}\right]$$

IMP = 3.91

Table I

Memory Type	IMP
1. Core, DRO	7.96
2. Thin Film, Read Only	6.15
3. Thin Film, Read-Alter	4.36
4. Plate Wire, Read Only	7.16
5. I. C. Read-Alter	3.91

Table I is a summary of the indices for the five memory systems examined. The conclusions drawn from these quick calculations is that the Core DRO Type would be the most cost effective choice for our application. Second choice is the Plated Wire Read Only, and the least cost effective is the I.C. Read-Alter memory.

The Index for Memory Performance provides a rapid "standard" comparison for evaluating different memory types for a given application.

APPLICATION NOTE

Small Data Processor Fully Automates Bulk Loading Terminal

MOTOROLA INSTRUMENTATION
AND CONTROL INC.
Phoenix, Arizona

This application note describes the use of the MDP-1000 small data processor, Fig. 1, in a data acquisition system where the requirement for optimum functional capability is complicated by the requirement for rigorous system simplicity.

The self-contained system, which typifies the latest technology in bulk loading terminal automation, controls four loading docks, and uses the MDP-1000 as its central element. It is used for round-the-clock, unattended loading of bulk product trucks.

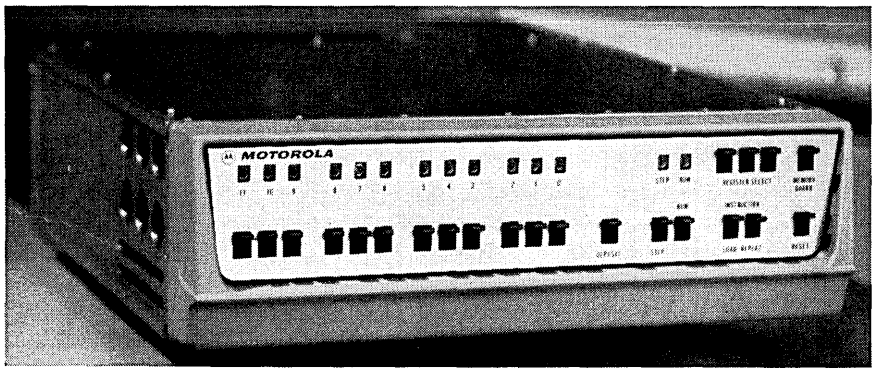

Fig. 1 The MDP-1000 data processor.

System Description

The system consists of two card readers; a driver's console where the driver receives authorization to withdraw product and receives the transfer manifest for product withdrawn; an RO35 output teletype and ASR35 input-output-communication teletype; sensors for tank temperature, tank level, pump control, additive control and riser control; and a central equipment cabinet containing the MDP-1000 data processor, control circuitry modules, emergency battery power supply, and a tape deck.

The block diagram, Fig. 2, shows how the units interconnect and

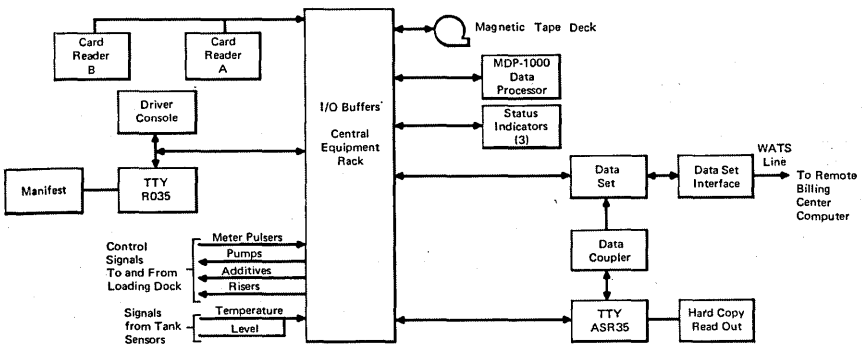

Fig. 2 Block diagram of data system for bulk loading automation.

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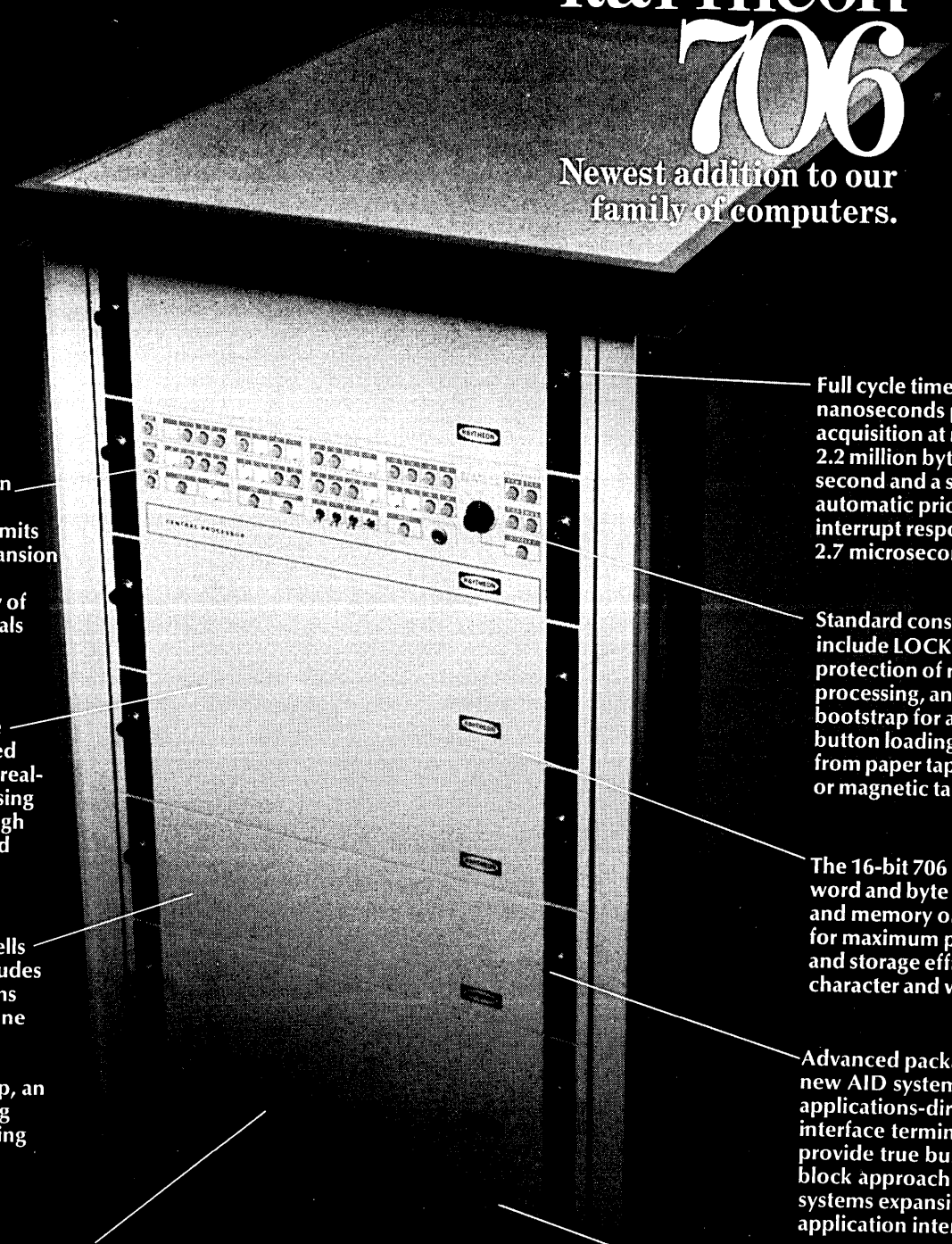

Full cycle time of 900 nanoseconds permits data acquisition at rates up to 2.2 million bytes per second and a standard automatic priority interrupt response time of 2.7 microseconds.

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how the system communicates with a remotely located billing center.

Data Processor Functions

The data processor in this application performs three functions.

- It functions as a stored logic controller for the bulk loading operation by releasing valves, registering withdrawal quantities, controlling additives and controlling pumps.
- It also functions as a data gathering terminal by gathering and storing transaction data, inventory control data, data pertinent to plant management and performance, and operational data from sensors.
- Its third function is that of a data communication and interchange terminal that interfaces between the bulk plant and a larger computer in the billing center.

Stored Logic Control Function

Its function as a stored logic controller is activated when the customer driver requests access to the terminal loading facilities. This access is controlled by wallet-sized, punched identity cards coded with specific identity digits and a unique terminal validity code. The driver inserts the card into the driver's console along with a customer card he selects from a file. The computer identifies the driver and customer from the coded cards. It also recognizes the products that the customer is authorized to withdraw, checks credit, product quota allowed, and inventory files to insure that the customer hasn't exceeded credit or product quota and that the product is available. If valid identity occurs, the computer indicates that the driver should select the product he wishes and then accepts the selections. The driver then withdraws the cards. If invalid identity occurs for any reason, the computer so indicates and withdrawal is automatically prohibited.

The driver proceeds to the loading dock, positions the truck, inserts his ID card into the reader controlling the dock, and repeats his product selection at the card reader. The MDP-1000 checks that safety regulations have been observed, then compares the selections with those made at the driver's console. If they match, it activates the pumps, permitting delivery to proceed. During delivery it mixes additives, monitors temperatures, and registers product throughput using the signals from the loading dock and from the tank sensors. When withdrawal is completed the processor computes net gallonage from gross gallonage, temperature, and gravity. It also updates plant inventory and customer product quota information. When withdrawal is completed, the driver requests a delivery manifest at the driver's console by signalling the computer. The data processor recalls the information from the tape, reproduces it, and the teletypwriter types out the manifest.

Data Gathering Terminal Function

The MDP-1000 performs its second function by harvesting transaction data as it is generated and storing it on tape and on paper tape at the ASR35 teletypewriter. This information includes up to 14 items summarizing and identifying the transaction and updating the plant inventory record. The information is serially coded and stored in USASCII code at 800 bits per inch and speeds to 120 characters per second for data set and teletypewriter compatibility. Each recorded character consists of 8 bits with odd parity (serially placed on tape). In the event of power failure the unit continues to accept transaction information while operating on 28VDC battery back-up power. It will not respond to read-out requests until ac power is restored. Also, after one hour on emergency power, or if the dc power falls below a preset level, the MDP-1000 shuts down and holds the stored information intact in its memory until power is restored. The status indicators give the operating state of the teletypes and power circuits and the tank inventory status.

Causes and Cures of Noise in Digital Systems

J. PAUL JONES
President
Navigation Computer Corp.
Norristown, Pa.

Based on a 3-part series of articles in the 1964 September, October, and November issues of COMPUTER DESIGN magazine, this handbook serves as a practical design guide for solving one of the major problems in designing digital systems. The author's emphasis is on practical tips for eliminating or minimizing noise — generalized rules are highlighted throughout the discussion. In Part 1, the forms of noise that are generated in wiring backplanes are considered and standard precautions that should be taken in systems design are given. Part 2 covers noise elimination in digital modules, and Part 3 discusses the control of external noise.

PART 1

Systems Design Considerations

PART 2

Noise Elimination in Digital Modules

PART 3

Control of External Noise

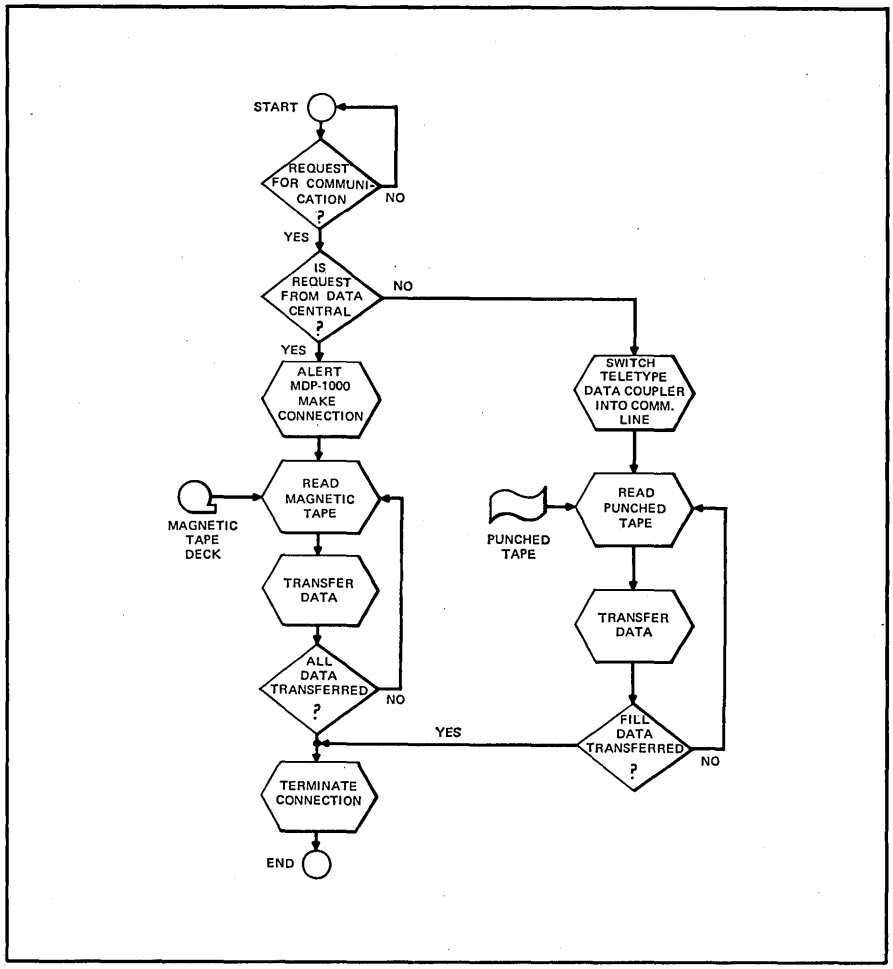


Fig. 3 Flow of communications to a remotely located central computer.

Data Communication and Interchange Terminal Function

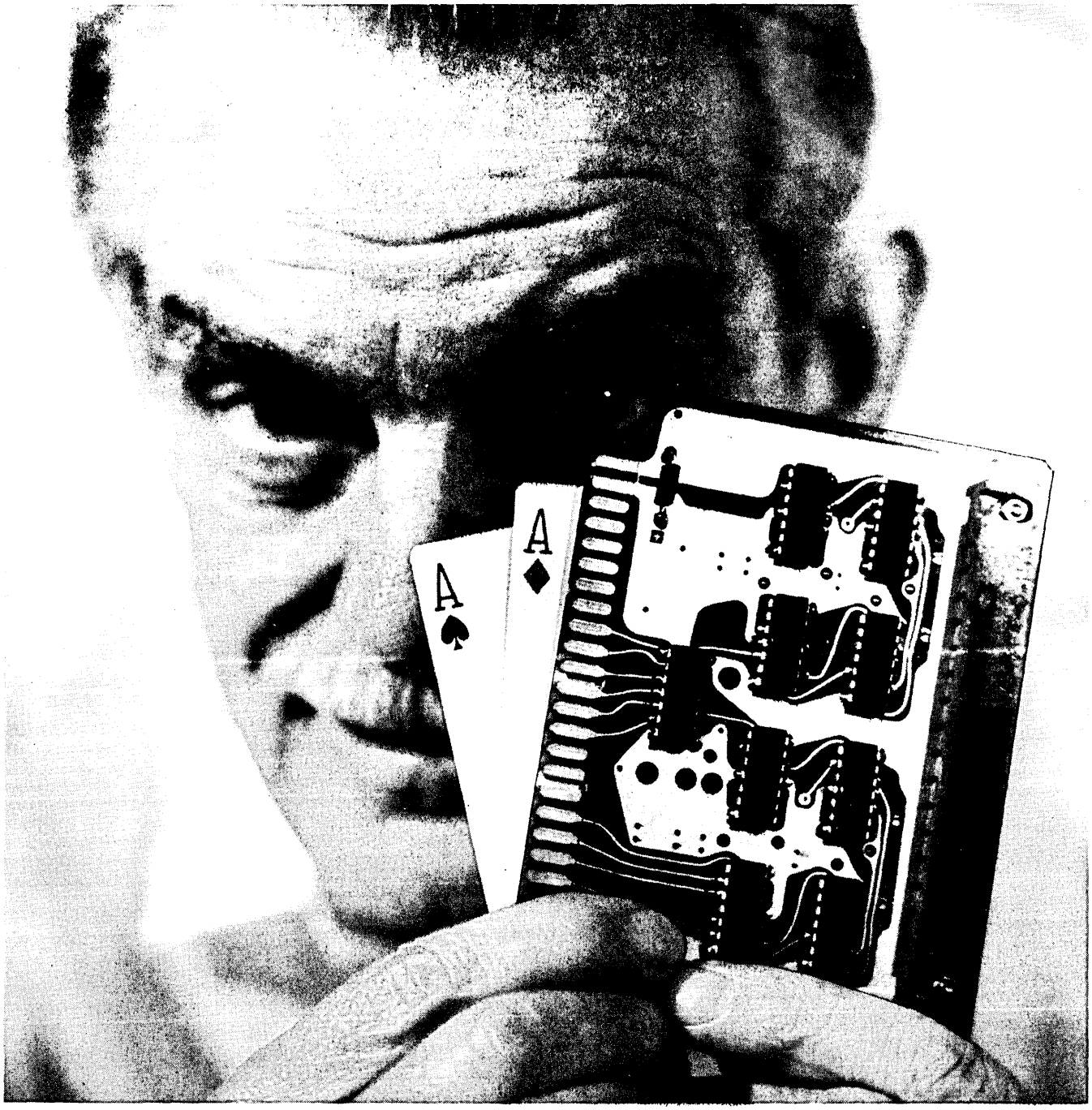
The remainder of the network shown in the block diagram assists the MDP-1000 in performing its third function as a data communication terminal interfacing with a larger computer. Communication is via WATS line to the remote billing center computer and although the data processor normally is interrogated at 36 hour intervals, it will release its data on demand. A flow diagram for communication with the remote billing center is shown in Fig. 3. Upon command from the central computer, the MDP-1000 issues the necessary commands to prepare the system for transferring the information it has stored to the general computer. The information is read serially bit-by-bit from the magnetic tape, routed through the I/O buffer, the Data Phone Data Set, and the Data Set interface to the WATS link. The information also can be transmitted by using the ASR35 teletypewriter to establish communication with the central computer. Again the flow is via the data coupler, Data Set, and Data Set interface. However, in this instance the ASR35 transmits the data from the punched paper tape record.

Other Applications

Other potential applications for the MDP-1000 data processor are:

- As the central element of automated process control systems and supervisory control systems.
- As the central element of management information systems.
- As a preprocessor for large-scale computers.
- In specialized real-time accounting systems.
- As a message concentrator in communications control networks.
- As a multiplexer for systems having several data inputs.
- As a relay center controller.

For additional information Circle No. 198 on Inquiry Card



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CIRCLE NO. 31 ON INQUIRY CARD

1969 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

University of Pennsylvania and
Sheraton Hotel, Philadelphia, Pa.
February 19, 20, 21, 1969

At this year's ISSCC, over 30 scientists and engineers from France, Germany, England, Holland, Australia and Japan will cover such timely subjects as current-input differential amplifiers, MOS-IC memories, IC monolithic displays, IC signal-processing circuits for TV receivers, pressure-sensitive diodes for switching, brushless dc motor-switching circuitry and computer-aided design practices.

The U.S. segment of the program will feature papers by over 120 specialists who will discuss operational amplifiers, semiconductor memories, optoelectronic technology and applications, digital circuits, solid-state power control, computer-aided design, analog circuits, and circuit and device modeling.

The conference will also be highlighted by seven invited papers, including a keynote address on strategy and tactics for integrated electronics by J. A. Morton of Bell Telephone Laboratories.

The traditional, and ever-popular, Wednesday-Thursday evening discussions, held at the Sheraton Hotel, will include twelve informal sessions with over 70 panelists participating. They will comment on analog IC's custom versus standard LSI, artwork design and implementation, impact of LSI on memory organization and design, and electroluminescent-diode alphanumeric displays. Appraisals will also cover IGFETs today, ultra high-speed digital techniques, and computer-aided circuit design.

All of the conference papers, invited and contributed, will be published in the ISSCC DIGEST of TECHNICAL PAPERS. All who register at the meeting will receive a copy. Additional copies will also be available at the conference and thereafter ($10.00 to IEEE members and $15.00 to nonmembers) from H. G. Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, Philadelphia, Pa. 19104, and the IEEE, 345 E. 47th Street, New York, N. Y. 10017.

The ISSCC 69 preregistration fee for IEEE members is $18.00; nonmembers, $20.00. Fees at the conference will be $20.00 for IEEE members, and $25.00 for nonmembers. Programs, with registration forms, can be obtained from H. G. Sparks, or Lewis Winner, 152 West 42nd St., New York, N. Y. 10036.

The general chairman of the 1969 conference is James D. Meindl, Stanford University, Stanford, California; program chairman is R. S. Engelbrecht, Bell Telephone Laboratories, Inc., Murray Hill, N. J.

J. D. MEINDL

R. S. ENGELBRECHT

TECHNICAL PROGRAM EXCERPTS

Wed./9:00-11:45/Irvine Aud.

SESSION I: Operational Amplifiers

Chairman: M. M. McWhorter, Stanford University, Stanford, Calif.

1.1:—INVITED: NEW APPROACHES FOR THE DESIGN OF MONOLITHIC OPERATIONAL AMPLIFIERS, R. J. Widlar, National Semiconductor Corp., Santa Clara, Calif.

A survey of recently-discovered integrated-circuit elements will be made, explaining their impact on the design of monolithic operational amplifiers with good DC characteristics, especially low-input current, and faster operating speeds.

1.2: A NEW HIGH-SPEED MONOLITHIC OPERATIONAL AMPLIFIER, E. S. Narayanamurthi, Fairchild Semiconductor, Mountain View, Calif.

The design and fabrication of a monolithic operational amplifier with high slew rate, large bandwidth, fast settling time and excellent DC characteristics will be discussed. At closed loop gains of 1, 10 and 100, typical slew rates are 20 V/μs, 40 V/μs and 60 V/μs, respectively.

1.3: A SELF-COMPENSATED MONOLITHIC OPERATIONAL AMPLIFIER WITH LOW INPUT CURRENT AND HIGH SLEW RATE, J. E. Solomon and W. R. Davis, Motorola Semiconductor Products Div., Phoenix, Ariz.

A monolithic operational amplifier which achieves a gain of 150,000, 5 nA input current and a 4 V/μs slew rate will be described. The amplifier incorporates high β input transistors, a novel PNP-NPN composite and an MOS compensation capacitor.

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1.4: AN INTEGRATED ELEMENTAL LOW-VOLTAGE OPERATIONAL AMPLIFIER, M. J. Hellstrom and W. R. Harden, Westinghouse Electric Corp., Linthicum Heights, Md.
A low-power operational amplifier that has medium open-loop gain will be described. Optimum circuit performance can be maintained, notwithstanding power drain and voltage gain changes due to amplifier's external components.

1.5: CURRENT INPUT DIFFERENTIAL AMPLIFIERS WITH HIGH COMMON MODE REJECTION, J. I. Brown, Monash University, Clayton, Victoria, Australia.
This paper will describe a new differential amplifier, the dual of conventional amplifiers, whose output is proportional to the differential mode input current, while common-mode currents are rejected. High common-mode rejection can be maintained over wide bandwidths.

Wed./1:45-2:45/Irvine Aud.

SESSION III—FORMAL OPENING OF CONFERENCE

INTRODUCTORY COMMENTS—J. D. Meindl, Stanford University Chairman of Conference

WELCOMING REMARKS—Gaylord P. Harnwell, President, University of Pennsylvania

1968 CONFERENCE AWARDS—J. S. Mayo, Bell Telephone Laboratories, Inc., Chairman, 1968 Conference

3.1:—KEYNOTE ADDRESS: STRATEGY AND TACTICS FOR INTEGRATED ELECTRONICS, J. A. Morton, Bell Telephone Laboratories, Inc., Murray Hill, N.J.
A critical evaluation citing how through an orderly evolution of compatible semiconductor and thin-film technologies, we can provide for continuing major advances in the performance, complexity and diversity of integrated electronics.

Wed./2:50-5:30/Irvine Aud.

SESSION IV: Semiconductor Memories

Chairman: L. Spandorfer, Univac Corp., Blue Bell, Pa.

4.1: A HIGH-PERFORMANCE MONOLITHIC STORE, J. K. Ayling, R. D. Moore, G. K. Tu, IBM Corp., Poughkeepsie/E. Fishkill, N.Y. and B. Agusta, IBM Corp., Essex Junct., Vt.
A 40-ns access bipolar monolithic memory of 2021 words x 144 bits capacity has been developed and incorporated in a computing system. The design and structure of a 64-bit silicon chip will be presented and some aspects of the organization and circuit design discussed.

4.2: A 40-NS, 144-BIT N-CHANNEL MOS-IC MEMORY, H. Yamamoto, M. Shiraishi and T. Kurosawa, Nippon Electric Co., Ltd., Tokyo, Japan
A monolithic MOS 144-bit random access memory has been fabricated, using N-channel MOS transistors. The memory operates with a 10-ns access time, 30-ns non-destructive read cycle time, and a 40-ns write cycle time.

4.3: AN INTEGRATED ASSOCIATIVE MEMORY ELEMENT, R. F. Herlein and A. V. Thompson, American Micro-Systems, Inc., Santa Clara, Calif.
The design of an integrated, parallel-organized, associative memory element containing the majority of repetitive logic required to implement a large, flexible associative memory system will be described.

4.4: ANOMALOUS BEHAVIOR IN STACKED-GATE MOS TETRODES, H. G. Dill, R. W. Bower and K. G. Aubuchon, Hughes Research Laboratories, Newport Beach, Calif.
This paper will describe a new type of trapping effect observed in stacked-gate MOS tetrodes. Control of and application of this effect to an electrically-alterable read-only memory will be discussed.

4.5: THE APPLICATION OF MNOS TRANSISTORS IN A PRESET COUNTER WITH NONVOLATILE MEMORY, F. W. Flad, Harry Diamond Laboratories, Washington, D.C. and C. J. Varker and H. C. Lin, Westinghouse Electric Corp., Elkridge, Md.
A DC binary circuit which utilizes P-channel MNOS transistors for all circuit functions and several novel characteristics such as nonvolatile storage, preset complementing and the elimination of a threshold voltage drop on the load devices will be discussed.

Wed./2:50-5:30/Univ. Museum

SESSION V: Optoelectronic Technology and Applications

Chairman: D. Sawyer, NASA Electronic Research Center, Cambridge, Mass.

5.1: INTEGRATED ELECTRONICS FOR A READING AID FOR THE BLIND, J. D. Meindl, J. D. Plummer, P. J. Salsbury and J. S. Brugler, Stanford University, Stanford, Calif.
A novel dictionary-size optical-tactile reading aid for the blind has been developed using integrated electronics. Salient features include efficient multiplex circuitry, a unique image sensor and automatic compensation of optical changes in reading material.

5.2: LIQUID CRYSTAL MATRIX DISPLAYS, B. J. Lechner, F. J. Marlowe, E. O. Nester and J. Tults, RCA Laboratories, Princeton, N.J.
The display related properties of liquid crystal cells and addressing techniques for liquid crystal matrix displays will be presented. A 36-element matrix producing moving half-tone images in real time will be described.

5.3: DESIGN OF AN ALL SOLID-STATE NUMERIC DISPLAY USING LSI READ-ONLY MEMORY, J. C. Barret, Hewlett-Packard Co., Palo Alto, Calif.
An all solid-state display has been developed by combining a matrix of 28 GaAs luminescent diodes with complex silicon integrated circuits. Design trade-offs will be discussed showing the total interaction. Some applications will be illustrated.

5.4: MONOLITHIC ARRAYS OF LIGHT-EMITTING DEVICES WITH INTERNAL MEMORY, A. M. Barnett, R. E. Glusick, H. A. Jensen, V. F. Meikleham and D. C. Osborn, General Electric Co., Syracuse, N.Y.
This paper will describe a semiconductor display with inherent memory whose central element is a monolithic integrated circuit that performs the logic function in addition to the optical output on the display surface. Matrix address is permitted.

5.5: A HIGH-SPEED, WORD ORGANIZED, PHOTODETECTING ARRAY, R. S. Mezrich, D. H. R. Vilkomerson and J. M. Assour, RCA Laboratories, Princeton, N.J.
A word-organized photodetecting array capable of submicrosecond response to low light-level signals will be described. The array uses PIN diodes for both detection and selection, and fabrication in monolithic form has been achieved.

Wed./8:00/Sheraton Hotel

Informal Discussion Sessions

2. ANALOG INTEGRATED CIRCUITS (East Ballroom)
Moderator: J. E. Solomon, Motorola Semiconductor Products Div., Phoenix, Ariz.
The latest advances in integrated operational amplifiers, multipliers and voltage regulators will be discussed. Discrete and IC approaches will be compared and trends toward more complex analog processes, circuits and hybrid systems will be covered.

Panel Members: *H. Koerner,* Burr-Brown Research Inc., Tucson, Ariz. *R. Stata,* Analog Devices, Inc., Cambridge, Mass. *R. J. Widlar,* National Semiconductor Corp., Santa Clara, Calif. *G. Wilson,* Fairchild Semiconductor, Palo, Alto, Calif. *B. Gilbert,* Textronix, Inc., Beaverton, Ore. *W. Howard,* Univ. of California, Berkeley, Calif.

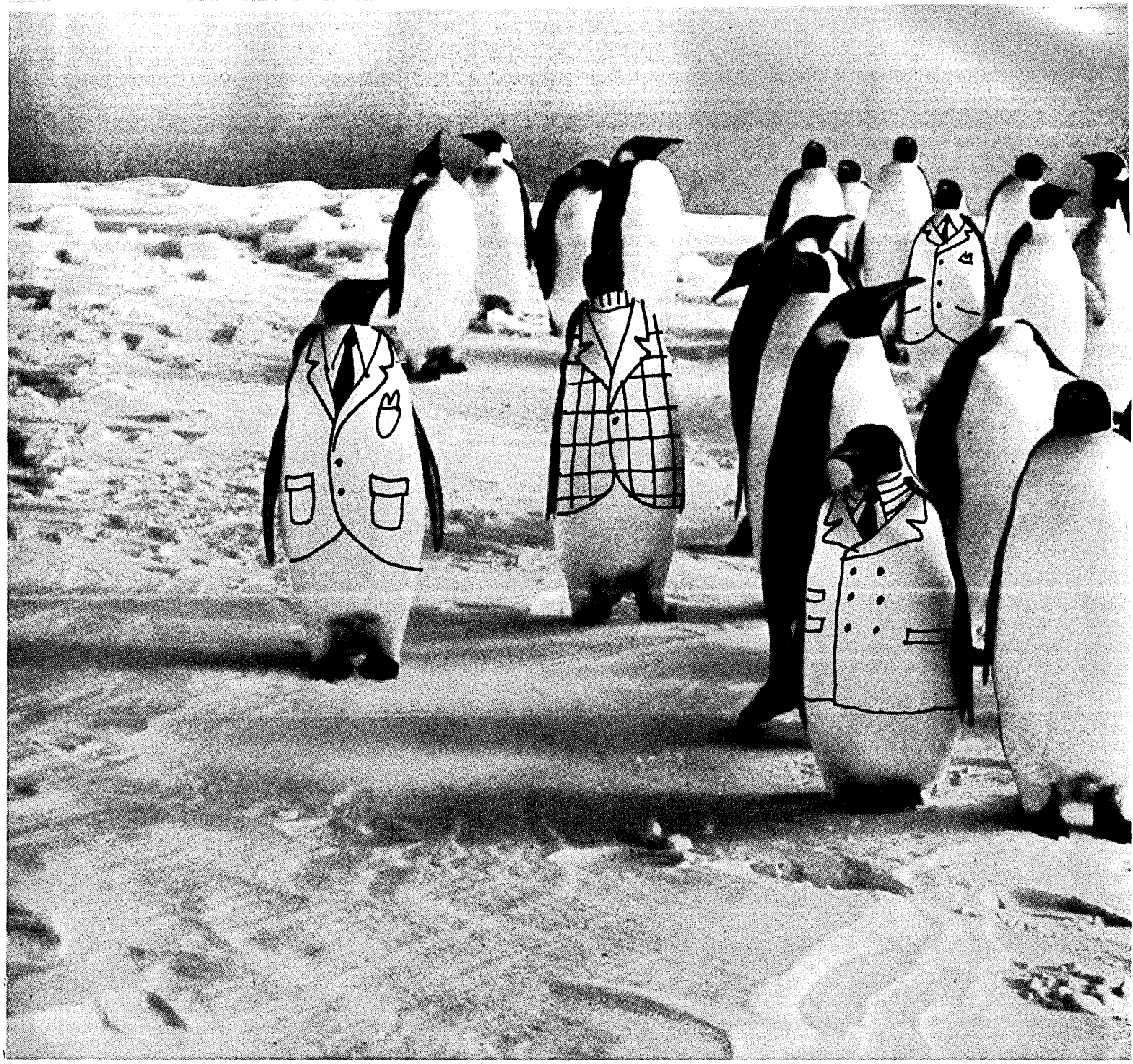
3: CUSTOM VERSUS STANDARD LSI (Pennsylvania West)
Moderator: R. Ulrickson, Fairchild Semiconductor, Mountain View, Calif.
As it becomes possible to make semiconductor logic devices having the functional complexity of digital subsystems, can we define standard products or is LSI inherently custom? Panelists from digital systems manufacturers will compare their needs against product plans of semiconductor houses.

Panel Members: *H. Miller,* RCA Laboratories, Princeton, N.J. *D. Winsted,* Signetics Corp., Sunnyvale, Calif. *C. Ghest,* Fairchild Semiconductor, Mountain View, Calif. *W. R. Raisanen,* Motorola Semiconductor, Products Div., Mesa, Ariz. *U. Faber,* Burroughs Corp., Paoli, Pa. *R. W. Ballard,* Litton Data System, Van Nuys, Calif.

5: IMPACT OF LSI ON MEMORY ORGANIZATION AND DESIGN (Independence-Constitution)
Moderator: J. I. Raffel, MIT Lincoln Laboratory, Lexington, Mass.
The probable impact of LSI on computer memory organization and design, with respect to storage, hierarchies switching, parallel access, logic and memory will be considered.

Panel Members: *G. Hornbuckle,* MIT Lincoln Laboratory, Lexington, Mass. *M. Pirtle,* University of California, Berkeley, Calif. *G. H. Barnes,* Burroughs Corp., Paoli, Pa. *C. Conti,* IBM Corp., Poughkeepsie, N.Y.

6: ELECTROLUMINESCENT-DIODE ALPHANUMERIC DISPLAYS (Hall of Flags)
Moderator: E. I. Gordon, Bell Telephone Laboratories, Inc., Murray Hill, N.J.
Device technology and characterization, circuits and electronic-optical interface topology for various approaches toward alphanumeric display using electroluminescent devices will be discussed.



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Panel Members: *R. E. Brown,* Monsanto Co., Cupertino, Calif. *M. M. Atalla,* Hewlett-Packard Laboratories, Palo Alto, Calif. *R. W. Keyes,* IBM Corp., Yorktown Heights, N.Y. *R. James,* RCA, Somerville, N.J. *W. Rosenzweig,* Bell Telephone Laboratories, Inc., Murray Hill, N.J.

Thurs./9:00-12:00/Irvine Aud.

SESSION VI: Digital Circuits

Chairman: V. I. Johannes, Bell Telephone Laboratories, Inc., Holmdel, N.J.

6.1: A LARGE-SCALE INTEGRATION HYBRID SUBSTRATE, M. Dumesnil and J. Schroeder, Fairchild Semiconductor, Palo Alto, Calif.
Two high-density multichip subsystems utilizing beam lead ICs and multilayer metal technology on large ceramic substrates will be described: a 26-IC dual four-bit arithmetic unit (1″ by 2″) and a 16 k/b random-access MOS memory (304 ICs) on a 4″ x 5″ alumina card.

6.2: HIGH-SPEED LSI CURRENT MODE LOGIC ARRAYS FOR LIMAC, A. Rashid, RCA. Somerville, N.J.
Design and fabrication of high-speed 72- and 144-gate arrays developed for the LIMAC computer will be described. Arrays employ a low-power current mode logic cell with 4 to 5-ns propagation delay at 10 mW to provide increased logic complexity at reduced power dissipation.

6.3: AN INTEGRATED LOGIC GATE WITH SUBNANOSECOND PROPAGATION DELAY AS A SYSTEM ELEMENT, H. S. Gold, Bell Telephone Laboratories, Inc., Holmdel, N.J., R. A. Pederson, Bell Telehpone Laboratories, Inc., Allentown, Pa.
Subnanosecond propagation delays in a system environment have been achieved using beam-lead silicon integrated-circuit chips assembled on ceramic substrates. The basic gate design and performance of a multi-chip logic circuit will be discussed.

6.4: A 30-CIRCUIT MONOLITHIC CHIP WITH 750-PS LOADED-CIRCUIT DELAY PER STAGE, V. A. Dhaka, J. Langdon, E. J. Vanderveen, C. Chen, A. Oberai, B. P. F. Wu and R. Sechler, IBM Corp., Hopewell Junction, N.Y.
A high-speed 30-circuit silicon chip using non-saturating emitter-coupled logic circuits with 750-ps loaded delay per stage using 3-level metalization will be described. The chip contains 210 transistors and 196 resistors.

6.5: AN APPLICATION OF A MONOLITHIC DISPLAY INTEGRATED CIRCUIT, K. Yoshimura, H. Tanaka, K. Okura, M. Sakai and T. Matsumura, Nippon Electric Co., Ltd., Tokyo, Japan
This paper will discuss an indicator tube driver circuit using MOS and bipolar transistors in a monolithic form, making it economically practical to use the driver in desk-top calculators.

6.6: A FULLY INTEGRATED TIMING GENERATOR FOR THE PICTUREPHONE VIDEO TELEPHONE CAMERA, P. C. Davis and K. R. Gardner, Bell Telephone Laboratories, Inc., Reading, Pa. A. M. Gordon, Bell Telephone Laboratories, Inc., Holmdel, N.J.
A complete timing generator has been realized using five beam-leaded silicon and two tantalum integrated circuits, including 217 transistors, 345 resistors, and capacitors totaling 400 pf, all mounted on one square inch of ceramic.

Thurs./1:30-5:00/Irvine Aud.

SESSION IX: Solid-State Power Control

Co-Chairman J. C. van Vessem, Philips Integrated Circuits Div., Nijmegen, Netherlands and J. D. Harnden, Jr., General Electric Co., Schenectady, N.Y.

9.1: A MONOLITHIC INTEGRATED CIRCUIT FOR PROPORTIONAL POWER CONTROL, J. Mullaly, General Electric Co., Syracuse, N.Y. and E. K. Howell, General Electric Co., Auburn, N.Y.
The design and performance of an AC line-operated phase-control circuit will be discussed and novel monolithic functional elements—full-wave bridge rectifier, silicon bilateral switch, and low impedance zener—described and related to performance.

9.2: SUBMINIATURE SILICON PRESSURE TRANSDUCER, A. C. M. Gieles, Philips Research Laboratories, Eindhoven, Netherlands
By combining spark erosion and electrochemical etching it has been found possible to fabricate solid-state microtransducers. Technology for a pressure transducer, with an epitaxial layer as the diaphragm, will be described.

9.3: A NEW PRESSURE-SENSITIVE DIODE AND ITS APPLICATION TO SWITCHING CIRCUITS, A. Yamashita, M. Tanaka and T. Suzuki, Matsushita Electric Industrial Co., Ltd., Osaka, Japan
A high-sensitivity pressure diode with a resistance variation of 1000-10,000 has been developed. Solid-state switching circuits and SCR controls using the pressure-sensitive diode will be described.

9.4: A SWITCHING CIRCUIT FOR A BRUSHLESS DC MOTOR CONTAINING A SI HALL ELEMENT, G. Bosch, Philips Research Laboratories, Eindhoven, Netherlands
A circuit containing a Si Hall element that can drive a brushless DC motor will be described. Requirements with respect to the accuracy of the components will be given and compared with possibilities of the current Si technology.

9.5: A NEW PHASE-SENSITIVE RECTIFIER CIRCUIT EMPLOYING A FLOATING POWER SUPPLY, R. C. Bowes and E. F. Good, Royal Radar Establishment, Great Malvern, Worcs., England
A phase-sensitive rectifier with a dynamic range of 10^4 from 3 Hz-100 kHz that features a floating power supply insensitive to component values and supply voltages will be described.

9.6: SURGE VOLTAGES IN RESIDENTIAL AND INDUSTRIAL POWER CIRCUITS, F. D. Martzloff and G. J. Hahn, General Electric Co., Schenectady, N.Y.
The effect of transient voltage on solid-state circuits is often detrimental. Data on surge severity and occurrence that devices must withstand to insure more reliable solid-state circuit design will be covered.

Thurs./1:30-5:00/Annenberg Aud.

SESSION XI: Computer-Aided Design

Chairman: R. E. McMahon, MIT Lincoln Laboratory, Lexington, Mass.

11.1: COMPUTER ANALYSIS AND SIMULATION OF MOS CIRCUITS, A. Feller, RCA, Camden, N.J.
The algorithm, model and results of computer programs with a built-in large signal MOS model that provides DC and transient analysis of P, N or complementary MOS circuits will be covered in this paper.

11.2: TOPOLOGICAL LAYOUT DESIGN OF MONOLITHIC IC IN COMPUTER-AIDED DESIGN, K. Yoshida and T. Nakagawa, Tokyo-Shibaura Electric Co., Kawasaki, Japan
This paper will discuss a topological layout project for IC components using a computer, based on given circuit diagrams and order of bonding pads.

11.3: TOPOLOGICAL SYNTHESIS PROCEDURE FOR CIRCUIT INTEGRATION, W. L. Engl and D. A. Mlynski, Technische Hochschule, Aachen, Germany
A computer-aided topological layout of components and wiring in integrated circuits will be presented based on a new kind of graph which accounts for all technological restrictions, as well as possibilities.

11.4: DIAGNOSIS OF SINGLE GATE FAILURES IN COMBINATIONAL CIRCUITS, G. D. Hornbuckle and R. N. Spann, MIT Lincoln Laboratory, Lexington, Mass.
A method for diagnosing arbitrary single-gate failures in combinational logic circuits will be presented. The procedure will locate the faulty gate and describe its failure which may be any detachable transformation of the correct gate function.

11.5: A MOST MEMORY USING DISCRETIONARY WIRING, A. F. Beer, K. H. Nicholas and I. H. Lewin, Mullard Research Laboratories, Redhill, Surrey, England
This paper will describe an integrated 1024-bit MOST memory, including selection matrices, using discretionary wiring. The technology, including the optomechanical mask generator and performance, will be discussed along with some indication of costs in production.

Thurs./8:00/Sheraton Hotel

Informal Discussion Sessions

7: IGFETS TODAY (West Ballroom)
Moderator: H. C. Lin, Westinghouse Electric Corp., Elkridge, Md.
The following problems will be probed by the panel. Comparison of IGFETs with bipolar transistors for LSI. The state-of-the-art for N-channel, complementary nitride and other gate insulators and substrates. Applications in memories, shift registers, and other digital and linear circuits.

Panel Members: *F. M. Wanlass,* General Instrument Corp., Salt Lake City, Utah. *A. C. Lowell,* Autonetics, Anaheim, Calif. *S. Katz,* RCA, Somerville, N.J. *A. K. Rapp,* Philco-Ford Corp., Blue Bell, Pa. *W. C. Kessler,* National Cash Register Co., Dayton, O. *D. A. Hodges,* Bell Telephone Laboratories, Inc., Murray Hill, N.J.

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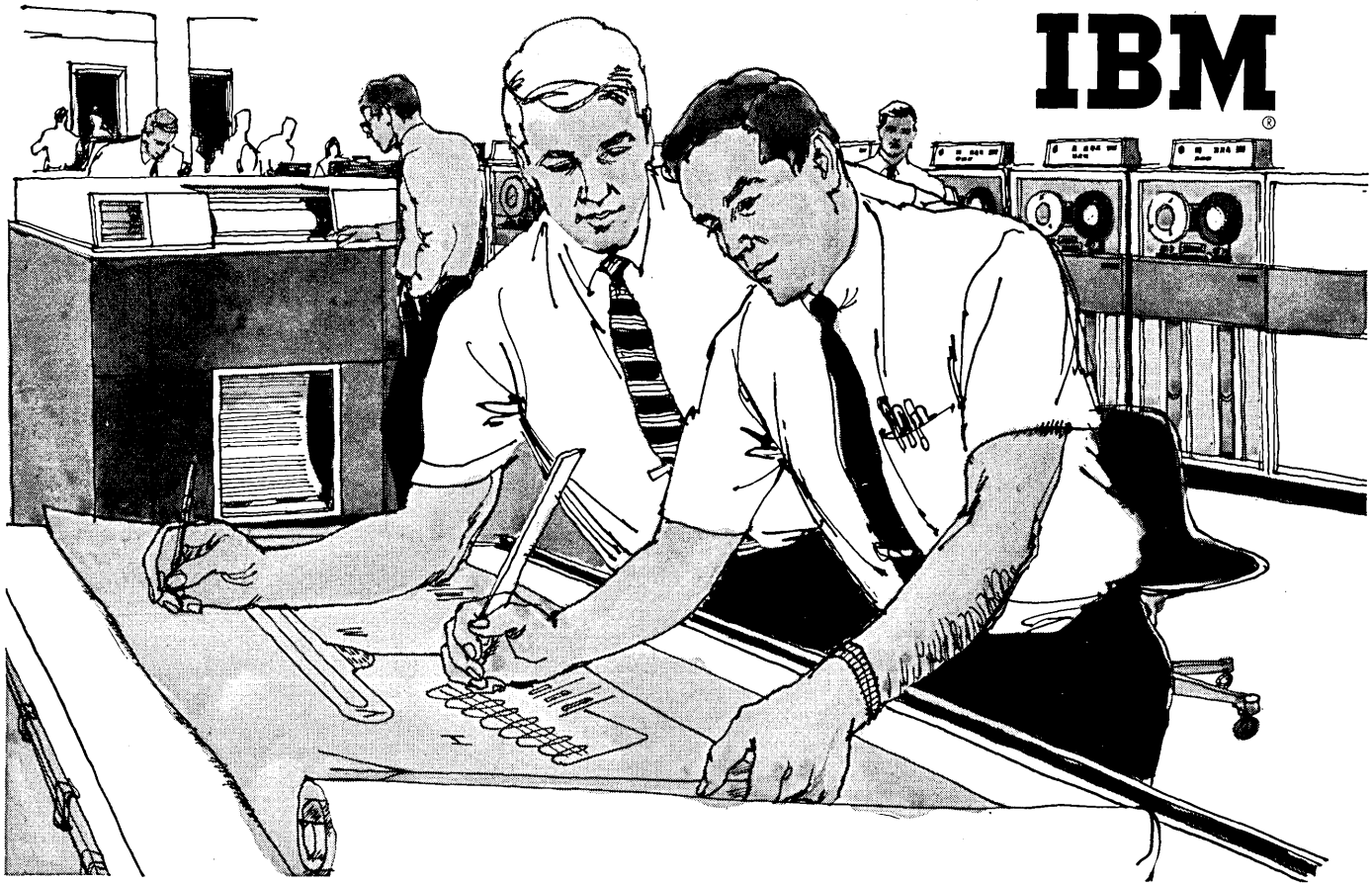


8: ULTRA HIGH-SPEED DIGITAL TECHNIQUES
(East Ballroom)

Moderator: D. DeWitt, IBM Corp., Hopewell Junction, N.Y.

The status and possible future directions of very fast computer logic, including system needs, device, circuit and packaging approaches and their potential, will be discussed.

Panel Members: *A. V. Brown,* IBM Corp., Yorktown Heights, N.Y. *H. Cardinas,* Texas Instruments, Inc., Dallas, Tex. *M. J. Flynn,* Evanston, Ill. *B. T. Murphy,* Bell Telephone Laboratories, Inc., Murray Hill, N.J. *J. A. Narud,* Motorola Semiconductor Div., Phoenix, Ariz. *H. Runkel,* Control Data Corp., Chippewa Falls, Wis. *R. B. Seeds,* Fairchild Semiconductor, Palo Alto, Calif.

11: COMPUTER-AIDED CIRCUIT DESIGN
(Independence-Constitution)

Moderator: D. Pederson, University of California, Berkeley, Calif.

The focus in this panel session will be on alternate approaches for circuit design, as well as the needs of the circuit designer. The requirements imposed on the computer will also be discussed, and additionally, the panelists will explore what has been accomplished to date and offer some predictions.

Panel Members: *M. L. Dertouzos,* MIT, Cambridge, Mass. *E. J. Baldwin,* Bell Telephone Laboratories, Inc., Murray Hill, N.J. *D. K. Lynn,* Motorola Semiconductor Products Div., Mesa, Ariz. *R. A. Rohrer,* Fairchild Semiconductor, Palo Alto, Calif. *M. O'Hagan,* Southern Methodist University, Dallas, Tex. *R. J. Schreiner,* Fairchild Semiconductor, Mountain View, Calif.

Fri./9:00-12:00/Irvine Aud.

SESSION XII—INVITED: Technology for Integrated Circuit Design

Chairman: C. Thornton, Philco-Ford Corp., Blue Bell, Pa.

12.1: NEW SIMPLIFIED BIPOLAR TECHNOLOGY AND ITS APPLICATION TO SYSTEMS, B. T. Murphy, Bell Telephone Laboratories, Inc., Murray Hill, N.J., S. M. Neville, Bell Telephone Laboratories, Inc., Indian Hill, Ill. and R. A. Pedersen, Bell Telephone Laboratories, Inc., Allentown, Pa.

New bipolar integrated circuit structures, which use no more processing steps than a conventional transistor, promise reduced processing costs and an increase in circuit packing density. This should lead to corresponding reductions in system cost with improved system performances; these improvements will be described.

12.2: TECHNOLOGY FOR DESIGN OF LOW POWER CIRCUITS, C. Bittman, G. Wilson, R. Whittier and R. Waits, Fairchild Semiconductor, Palo Alto, Calif.

A comprehensive discussion of circuit design and technology for the realization of micropower consumption in linear integrated circuits will be offered. Essential transistor and resistor, physics and process technology with tradeoffs in circuit design between speed, power dissipation, and scale of integration will be discussed.

12.3: THE INTERACTION OF TECHNOLOGY AND PERFORMANCE OF COMPLEMENTARY SYMMETRY MOS INTEGRATED CIRCUITS, P. D. Gardner and R. W. Ahrons, RCA, Somerville, N.J.

The technology of complementary MOS has already resulted in significant advantages in circuit simplicity, speed-power, and noise immunization. Future technological improvements to increase device gain, reduce capacity, and increase packing density will make complementary MOS even more attractive. The relationships among device physics, processing technology and performance will be presented.

12.4: THE IMPACT OF TECHNOLOGY ON RADIATION-HARDENED INTEGRATED CIRCUITS, J. P. Spratt, G. L. Schnable and J. Standeven, Philco-Ford Corp., Blue Bell, Pa.

The physics, process technology, and circuit design of radiation-hardened ICs will be discussed. Appropriate circuit design, plus optimum processing techniques (dielectric isolation, small geometry, controlled assembly methods, etc.) will be shown to improve low-power integrated circuits to the point where they no longer limit most systems exposed to nuclear weapons.

Fri./9:00-12:00/Univ. Museum

SESSION XIII: Analog Circuits

Chairman: R. W. Ahrons, RCA, Somerville, N.J.

13.1A: CONTACT RESISTANCE ON DIFFUSED RESISTORS, H. H. Berger, IBM Deutschland, Boeblingen, Germany

The electrical behavior of contacts on diffused resistors can be explained by an equivalent transmission line. What contributes to the contact resistance and how the contacts can be optimized will be discussed in this paper.

13.1B: CURRENT CROWDING ON METAL CONTACTS TO PLANAR DEVICES, H. Murrmann and D. Widmann, Siemens AG, Munich, Germany

The results of a theoretical and experimental investigation of contact resistance and current distribution in metal-to-silicon contacts of planar devices will be presented. Typical experimental values of the transition resistance between metal and diffusion layers will be offered.

13.2: INTEGRATED MOS ANALOG DELAY LINE, R. A. Mao, K. R. Keller and R. W. Ahrons, RCA, Somerville, N.J.

An analog fixed or variable delay line using P-channel MOS field-effect transistors has been monolithically fabricated on silicon. This paper will describe sample-and-hold operation, design considerations, properties, and applications of this integrated circuit.

13.3: PULSED FILTER NETWORKS—A MEANS OF AMPLIFYING AND VARYING TRANSFER FUNCTION PARAMETERS, J. A. Kachler, Martin Marietta Corp., Denver, Colo.

This paper will discuss a technique of pulsing filter networks that simultaneously achieves the realization of continuously variable filter parameters and capacitor multiplication. Active elements are shared to provide multiple transfer function channels whose parameters are pulse controlled.

13.4: A HIGHLY EFFICIENT, INDUCTORLESS VOLTAGE REGULATOR, C. Keeney and M. McWhorter, Vidar Corp., Mountain View, Calif.

A voltage regulator, using solid-state switching techniques, for applications where the conventional series regulator and inductor type of switching regulator are impractical, will be described. Good regulation with high peak current capability are provided.

13.5: WIDE BAND IMPEDANCE MEASUREMENT BY FOURIER TRANSFORMATION OF NETWORK PULSE RESPONSE, A. S. Farber and C. W. Ho, IBM Corp., Yorktown Heights, N.Y.

The measurement of driving point and transfer impedances over a wide spectrum rapidly and accurately will be discussed in this paper. A computer transforms the pulse response into the frequency response, and a sampling oscilloscope provides the time transformation needed for data acquisition.

Fri./9:00-12:00/Annenberg Aud.

SESSION XIV: Circuit and Device Modeling

Chairman: D. Marshall, Honeywell, Inc., Framingham, Mass.

14.1:THEORETICAL PROJECTION OF DELAY IN GERMANIUM AND SILICON HIGH-SPEED SWITCHING CIRCUITS, G. D. Hachtel, IBM Corp., Yorktown Heights, N.Y.

This paper will describe a 1-dimensional transistor analysis program featuring Fermi statistics, saturated velocity and transient effects that predicts switching delays (loaded, packaged CSEF circuits) of 50 ps(Ge) and 150 ps(SI) for near-ultimate impurity profiles, and at current densities of 10^5 A/cm^2.

14.2: COMPUTER MODELING OF A SUBNANOSECOND TRANSISTOR INCLUDING HIGH LEVEL INJECTION EFFECTS, P. C. Davis, Bell Telephone Laboratories, Inc., Reading, Pa.

A new base-widening theory that predicts nonlinear transistor transit times will be presented. These and special measurement techniques have been used in modeling a subnanosecond transistor to predict the switching performance of a 350-ps emitter coupled pair.

14.3: HIGH-SPEED PULSE CIRCUITS OBTAINED BY COMPUTER-AIDED NONLINEAR ANALYSIS OF STEP-RECOVERY DIODES, H. G. Jungmeister and D. Schmidt, Siemens AG, Munich, Germany

A computer-aided analysis method for the design of generators which can produce pulses shaped to specifications even in the GH range will be discussed. Pulse powers of more than 10 V p/p across 50 ohms can be obtained.

14.4: IGFET CIRCUIT PERFORMANCE: N-CHANNEL VS P-CHANNEL, D. L. Critchlow and L. M. Terman, IBM Corp., Yorktown Heights, N.Y. and G. Cheroff, IBM Corp., Hopewell Junction, N.Y.

Previous circuit performance comparisons between N-channel and P-channel IGFETs have not considered the control of device performance with substrate bias. These factors will be described and the resulting performance advantages of N-channel devices illustrated for a memory chip.

14.5: THE VARIABLE THRESHOLD FET: THEORY AND EXPERIMENT, F. A. Sewell, Jr., H. A. R. Wegener and E. T. Lewis, Sperry Rand Research Center, Sudbury, Mass.

The general theoretical model predicts the amount of threshold voltage change with time for both writing and storage modes of operation. Experimental data fit these theoretical expressions containing no adjustable parameter.

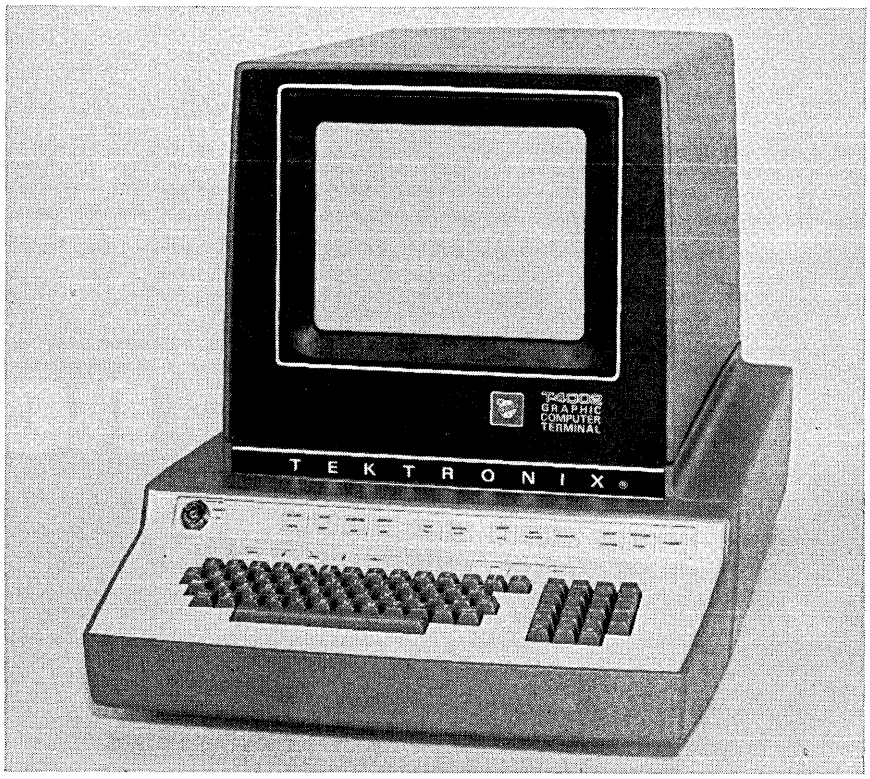
A LOW COST GRAPHIC COMPUTER TERMINAL

TEKTRONIX, INC.
Beaverton, Oregon

A completely self-contained, desk-top information display system, the Type T4002 Graphic Computer Terminal introduced by Tektronix Inc., provides complex graphics capability at a significantly low cost.

Complete communication interaction is achieved through the utilization of a solid-state data entry keyboard and a visual display of high-resolution alphanumerics and graphics. All of the elements required to effectively communicate with a computer are housed within the console, and space is provided within the console cabinet to accommodate an auxiliary module for expanding system capability. Two types of interfaces have been made available for direct coupling to computers or data communication systems.

System components include: a display unit, a terminal control, a character generator, a keyboard and an input/output interface.



Display Unit

An 11-inch, direct-view, bistable storage tube is used as the display media to produce high-density alphanumerics and complex graphics without flicker or drift. The 6½-inch by 8¼-inch screen will accommodate up to 35 lines of alphanumeric characters with 80 symbols per line permitting more than 2800 characters to be displayed with excellent clarity. Resolution achieved is equivalent to 400 x 300 line pairs. The luminance level of stored information is at least 3 fL and the contrast ratio is at least 3:1. Stored information may be erased in 0.5 seconds or less.

Terminal Control

The terminal control provides timing logic, data buffers and interconnection logic for the character generator, keyboard and auxiliary module. Linear interpolation is a function of the terminal control, D/A converters and plot logic. 1024 x 1024 points are addressable.

Character Generator

The character generator provides a set of 94 USASCII printable characters. Two sizes of characters are under program control, 70 x 90 mils and 140 x 180 mils. Up to 1000 characters per second (average) may be generated and stored on the display tube.

Continued on page 74

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CIRCLE NO. 901 ON INQUIRY CARD

Keyboard

Manual entry of data is through a solid-state keyboard with full USASCII capability (128 codes). Ninety-six upper and lower-case characters, numbers and special symbols are provided for alphanumeric data entry. Two sizes of characters are under program control with others available and 32 additional control characters are included for communications between the computer and the terminal.

Input/Output Interface

The terminal interface provides code conversion, logic levels and necessary connections to interface with a computer or data communication system. Initially, two types of interface are available: Type 4801 for DEC PDP-8 Series computers; and Type 4802 for interface with Bell System Type 201 and Type 202 data sets and other compatible acoustic modems or high-speed data systems.

Controls and Indicators

In addition to a standard alphanumeric keyboard, the following controls are provided to enhance ease of operation.

- Control Characters—The USASCII provides for 32 control characters to be utilized for communication between computers and remote I/O equipment.
- View—Switches the display from a hold mode to a view mode for approximately 1 minute.
- Erase—Erases the display.
- Format Controls — Provide a means of moving the cursor when fixed-format alphanumerics are used. The five format buttons (top left of keyboard) move the cursor up, down, right, left or home (fixed reference point).
- Power—Key switch for power on/off and control lock. Control lock position locks out all keyboard and control functions.
- On Line/Local—Controls on-line and off-line terminal operation and indicates status.
- Ready/Busy—Signals the status of the computer when an initial inquiry is made from the terminal.
- Input—Permits selection of keyboard or auxiliary as input to computer. Indicates status.
- Output—Permits selection of the display or auxiliary or both to receive output from computer. Indicates status.
- Page Full—Indicates full page and stops information from computer.
- Margin Shift—Allows a choice of four margin positions, starting on the left and moving to the right. Useful when writing columns of short statements.
- Error/Halt — Indicates echoplexed character is not identical character sent. Halt control allows a halt on data error detection.
- Data Received—Indicates computer entry to the display.
- Interrupt—Any time the computer is sending data, all controls on the terminal are inhibited except the interrupt switch (and the power switch). Pressing this switch stops the transmission and allows the operator to send data to the computer.

Auxiliary Module

Provision is made inside the terminal console for an auxiliary plug-in module to expand future capability with a blank plug-in available to satisfy unusual or special design requirements.

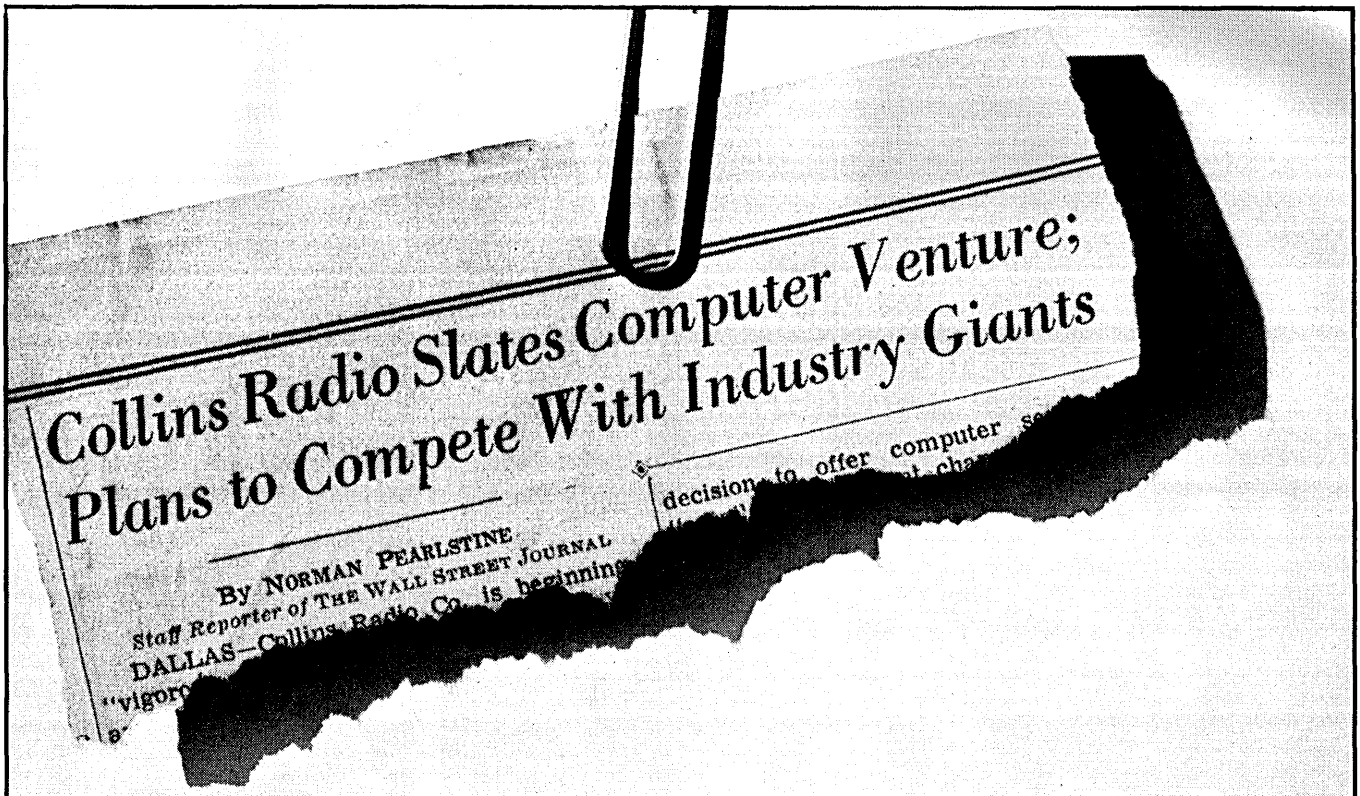
Other Characteristics

Quick-change line-voltage selector provides three ranges: 90 to 110V, 104 to 126V and 112 to 136V; 48 to 66Hz, 375 watts maximum at 117V and 60Hz. Normal operation is over the temperature range of 20°C to 50°C.

The terminal measures 19½-inches high x 35-inches long x 19-inches wide and has a net weight of 103 lbs.

Price of the Type T4002 terminal is $8000. Price of the Type 4801 DEC PDP-8 Series interface, with cable is $585; Type 4802 data communications interface, with cable is $515.

For additional information circle No. 199 on inquiry card.



Collins' New Data Program Creating New Opportunities

Collins' C-8500 C-System gives users the first completely integrated system with virtually unlimited expansion capability.

This new concept in computer applications is creating exceptional career opportunities for: Programmers, Hardware Diagnostic Programmers, Circuit Design Engineers, Memory Design Engineers, Digital System Engineers, Digital Systems Analysts, Logic Design Engineers, Mechanical Engineers, Data Systems Analysts and Applied-Systems Analysts/Programmers.

Engineers, Physicists, Mathematicians, and those with degrees in other physical sciences (1 to 5 years experience) will find an outstanding opportunity to learn and progress rapidly in the data field, even without previous data experience.

Please send resume in confidence to Manager of Professional Employment, Collins Radio Company, Dallas, Texas 75207; Cedar Rapids, Iowa 52406, or Newport Beach, California 92663.

an equal opportunity employer

COLLINS

CIRCLE NO. 902 ON INQUIRY CARD

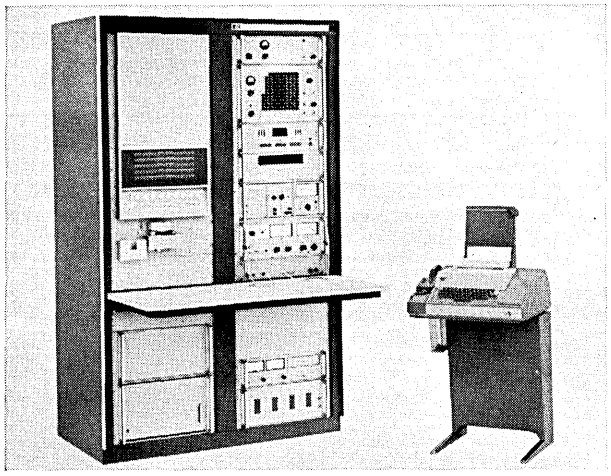
NEW PRODUCTS

STIMULUS-RESPONSE TEST SYSTEM

Model 9500A is a computer-controlled test system which offers means of testing electronic components, modules, or assemblies at the laboratory, production, incoming inspection, or field maintenance level. Standard test-signal sources, under computer command, stimulate the device under test. With standard options the frequency range may range from dc to 100 kHz, or as high as 500 MHz, controllable in level from 0 to 132 dB. Standard test instruments, similarly controlled, measure response. Measurement may be of voltage, phase, frequency, or ohms, as desired.

A basic system consists of the computer (Model 2116B), a teleprinter input/output unit on which instructions are typed in and output information recorded, a punched tape reader to take in programming data at 300 characters per second, a programmable dc power source (Model 6130B), an integrating digital voltmeter (Model 2402A) for precise dc measurements, and a distribution switch to connect the system to any of 16 test points.

Among the capabilities which can be added with options are ac voltage stimulus to 100 kHz, or up to 500 MHz, attenuation 0 to 132 dB, ac voltage measurement to 100 kHz or 10 MHz, ac voltage and phase measurement to 1000 MHz, 200-line measurement scanning, frequency measurement, and ohms measurement. Hewlett Packard Co., Palo Alto, Calif.



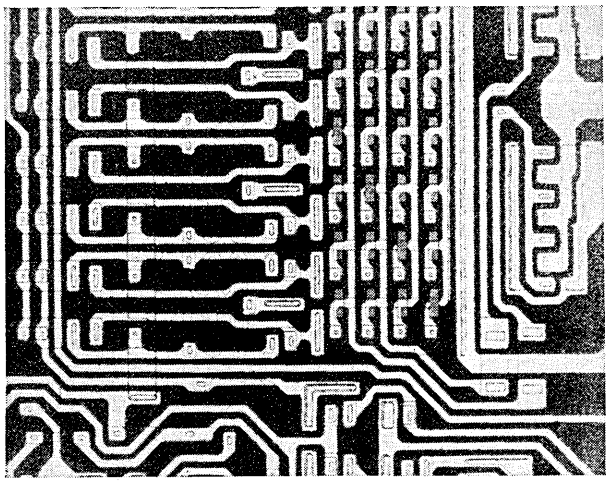
Circle No. 200 on Inquiry Card.

CUSTOMIZABLE READ ONLY MEMORY

The XC170, a bipolar 128-bit Read Only Memory (ROM), provides 16 custom eight bit words. The ROM is capable of performing logic which would require as many as 33 gates to implement and is specially suited for code translation applications. Examples of other ROM uses are: n of eight decoding, Hamming single error detection and parity generation, and 7 or 16 indicator lamp decoding.

A feature of the XC170 is a unique ordering system whereby the customer orders his ROM program (the array bit pattern of "1's" and "0's") by punching the necessary information on an ordinary EDP card. The order card then serves to control the automatic generation of the mask used to insert the customer program in the ROM. The same punched card also supplies the program for automatic testing of the finished product.

The ROM is composed of a 16x8 emitter-follower transistor array in which 8 TTL type amplifiers provide a buffered access from the four address inputs to the 16 word-select gates. The 16 gates perform the one-of-sixteen selection of the desired word in the ROM array and an additional AND gate enables or inhibits the entire array. Eight output buffer stages with open collectors allow each bit line to sink 20 mA and permit wired-OR construction of larger ROM for sequence generation and other applications.



The XC170 is supplied in the Unibloc™ 16 pin dual-in-line package for operation over a 0°C to 75°C temperature range. Motorola Semiconductor Products Inc., Phoenix, Ariz.

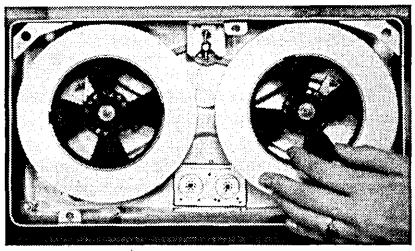
Circle No. 202 on Inquiry Card.

D/S CONVERTER

The ADverter Model DS12A1, a general purpose digital-to-synchro converter converts a 12-bit binary word into 3-wire synchro signals (or 4-wire resolver signals) with an accuracy of 2.7 arc min. It requires a 26 Vrms, 400 Hz reference for an output of 11.8 Vrms line-to-line, 100 mA max. and is able to directly drive most control transformers. Optional high power output stages enable the DS-12A1 to drive one or several torque receivers. Operating temperature is 0°C to 70°C.

Packaging features easily interchangeable encapsulated submodules, mounted directly on three PC boards, 8.3" x 5.6" x 1.1" max. height. Ditran Corp., Div. of Clifton/Litton Industries, Burlington, Mass.

Circle no. 237 on Inquiry Card



DIGITAL TAPE RECORDERS

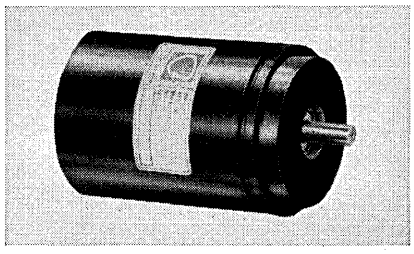
The DS-4130 incremental and the DS-4150 synchronous recorders are available in 7 or 9 track configurations with 6" reels. Model DS-4130 includes incremental recording capability for RZ or NRZ(1) inputs with a 200 bpi density and a character transfer rate to 200 steps/sec. Tape speed and tension are controlled by a dual differential capstan system. Rewind time is less than 1½ minutes.

Model DS-4150 synchronous recorders are controlled by command levels of Run-Write, Run-Read, Write Enable, Rewind Stop. Inputs can be either RZ or NRZ(1). Recording densities of 200, 556 or 800 bpi with read/write speeds to 37.5 ips are available. Outputs are reconstructed at the same levels as received and de-skewed to within 1 μs when played back on DS-4150 equipment.

Both models measure 6" x 7" x 13" and weigh 19 pounds. They are cartridge loaded, meet military specifications, and have a tape capacity of 1,000 feet. Sanders Associates, Inc., Nashua, N.H.

Circle no. 223 on Inquiry Card

NEW PRODUCTS



STEPPER MOTOR

Variable reluctance Tormax stepper, 020-021, couples load-driving capability with high response. In steady state, response is on the order of 3 milliseconds while driving a 1 oz-in load in a random bidirectional manner. Or, at the other end of the curve, driving a 10-oz-in load, response is approximately 100 milliseconds. The design limits overshoot and oscillation.

Performance figures are based on the use of a standard 28 Vdc Tormax controller-driver in one-phase-at-a-time excitation mode, incrementing the shaft 15 degrees per pulse. Other excitation modes permit different step angles and response rates. IMC Magnetics Corp., Westbury, N. Y.

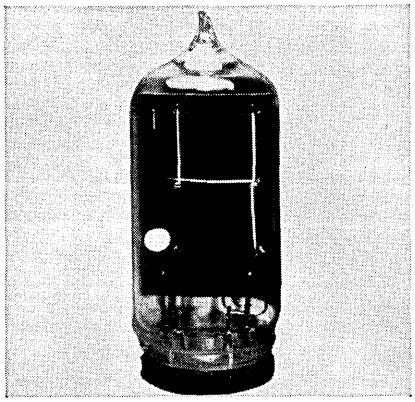
Circle no. 210 on Inquiry Card

CORE MEMORY

Model 25DM-500 features an access time of 280 ns and a cycle time of 500 ns and provides 8,192 words by 36 bits in a single module, 5¼" high, 19" wide and 23" deep. Modular expandability allows the capacity to be increased to 64,000 words by 72 bits. Integrated circuits are used extensively to achieve a compact modular design. A single module can fit into a standard 19-inch rack or be used unmounted. The standard memory features TTL positive true logic interface levels, and the system is designed to accommodate a wide range of input/output characteristics. The memory has a non-destructive power on/off control.

Significant optional equipment includes a power supply in a module the same size as the basic memory module, a memory tester of the same dimensions, data parity generation and check, address parity check, zone transfer, and a separate register indicator panel. Ampex Corp., Redwood City, Calif.

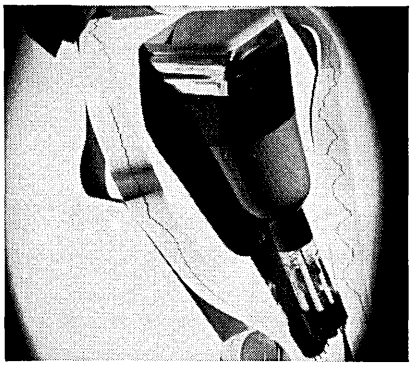
Circle no. 236 on Inquiry Card



NUMERICAL READOUT LAMPS

Numeralamps have a rating of 3 to 4V and 0.10 to .015 A and operate without buffer transistors. BCD input is decoded directly to drive the incandescent filaments. The filament is enclosed in a standard nine-pin vacuum tube. Numerals 0 through 9 are produced on a seven-bar frame with decimal point available as an option. Brightness can be varied from levels suitable for total darkness to a maximum of 4,000 foot lamberts. Useful life span is 200,000 hours or more; color temperature at rated voltage is approximately 1800° K. Circuit options include 10-line and/or BCD inputs with memory added where desired. Lamps, Inc., Gardena, Calif.

Circle no. 208 on Inquiry Card



FIBER OPTIC CRT

The WX-30738 records oscillographic information on direct-print photographic paper with a writing speed greater than one million inches per second.

The CRT has an 8-mil center spot size, and a trace linearity within 1%. In addition, it has a 3" x 5" faceplate and an over-all length of 16½". It weighs 3½ pounds and can be mounted with its axis facing in any direction. Westinghouse Electronic Tube Div., Elmira, N.Y.

Circle no. 218 on Inquiry Card

OPERATIONAL AMPLIFIER

The A101 is a general purpose operational amplifier capable of 10V common mode voltage, 5 mA output current and a bandwidth of 125 kHz, and features a .385" profile.

Operating parameters include: input offset drift, 20 μV/°C; input current 20nA/°C; common mode input impedance 50 megohms; and common mode rejection ratio, 90 dB. The unit is frequency compensated for a 6 dB/decade roll-off with a slew rate of 1.2 V/μs. Intronics, Inc., Newton, Mass.

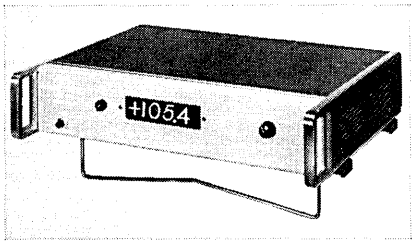
Circle no. 238 on Inquiry Card

ADHESIVES KIT

A multipurpose "Bond-All" adhesives kit is designed to fulfill the adhesive needs of research laboratories. It can be used to bond glass, plastics, iron, steel, copper, gold, silver, woods, glass-to-metal, wood-to-metal, different metals together, and just about any other combination of materials desired.

The kit contains more than twenty pieces of equipment including tweezers, clamps, mixing cups and mixing sticks, applicators, syringes and knives. Contains four different epoxy systems which provide a wide selection of bonding characteristics. Tescom Corp., Instrument Div., Minneapolis, Minn.

Circle no. 234 on Inquiry Card

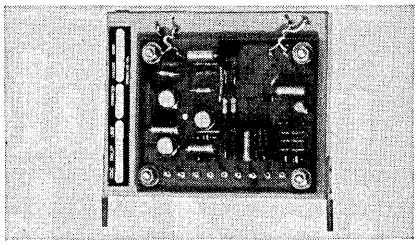


ALTITUDE REPORTING DISPLAY

The display accepts the standard ICAO, 11 bit altitude telemetry code and displays the absolute altitude in decimal form, including sign, through the use of code conversion modules and a fixed program computer. This system display altitude in 100 foot increments for a range of from −1200 to +126,700 feet. Units are available in laboratory and cockpit configurations. Northern Precision Laboratories, Inc., Fairfield, N. J.

Circle no. 207 on Inquiry Card

NEW PRODUCTS

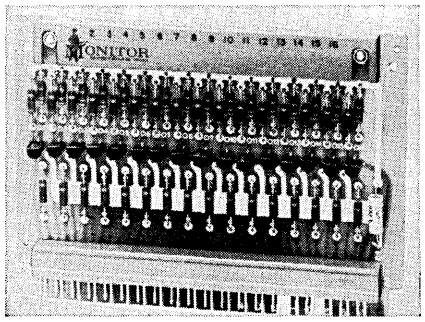


MAGNETOSTRICTIVE MEMORY

The MS 2219 miniature memory, for use in small electronic computers, calculators and digital interface devices, has a storage capacity of 1300 bits and a bit rate of 2.6 MHz. Its input is compatible with DTL logic and the output is from a Fairchild DTL 932. It is also compatible with T^2L logic.

Power requirements are +12 and +5 V, and −12 V. The operating temperature range is from 0° to 70°C. Dimensions are 4" x 3¼" x 1". Computer Devices Corp., Commack, N.Y.

Circle no. 226 on Inquiry Card

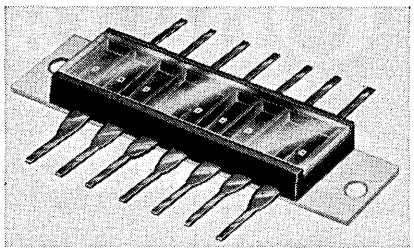


LINE DRIVER

Monilogic Card L74 contains 12 line drivers in the standard Monilogic card configuration complete with test point block and hermaphroditic connector.

The assembly is designed to drive terminated transmission lines such as 100 ohm coax or 91 ohm twisted pair. Logical "1" output levels will all be between +5 and +10 V as predetermined by the application of an equal voltage at a single pin of the connector. Each of the 12 outputs is connected to an individual test point. The L74 is a non-inverting device with propagation delays of less than 25 ns and 175 ns respectively for turn-off and turn-on. The inputs are compatible with DTL/TTL drives. Monitor Systems, Fort Washington, Pa.

Circle no. 203 on Inquiry Card

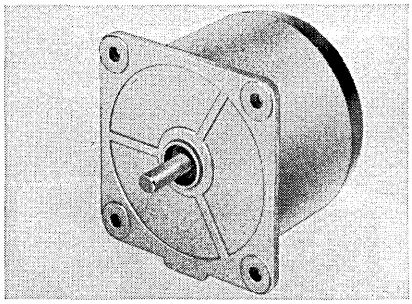


THICK FILM PHOTO ARRAY

The LA-800 Series standard light arrays for paper tape readers, provide each sensor with shielding from the next to eliminate cross-talk. The package and lead frame is similar to the standard 14 lead dual in-line plastic IC type. These units can be mounted directly to a fiber optic head, or PC board, or plugged into standard sockets.

The photo chips are mounted on .100" centers. For custom applications, chips can be mounted as close as .050" centers. Chips can be precisely aligned to within ±.002" in both the X and Y axis. Hybrid Electronics Inc., Chaska, Minn.

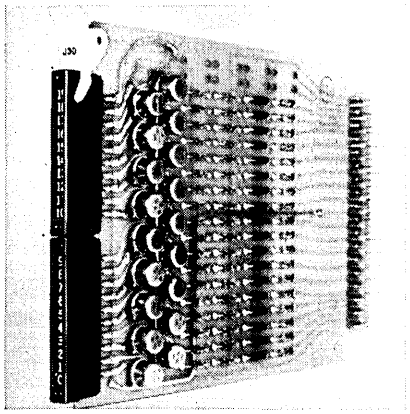
Circle no. 222 on Inquiry Card



STEPPER MOTORS

The K82105 stepper has a step angle of 7½° and a stepping rate of 0-240 pps. Available torque, is up to 8.2 oz-in. Stepper motor K82107 develops up to 4.8 oz-in of torque, with a 15° step angle and a step rate of 0-175 pps. These stepper motors are for use in incremental controls, line-spacing control in paperfeed devices, punched-paper tape drives, X-Y plotters, and chart drives. Dimensions are 2¾" dia. x 2¼" long x 2¾" square mounting flange. A. W. Haydon Co., Waterbury, Conn.

Circle no. 211 on Inquiry Card

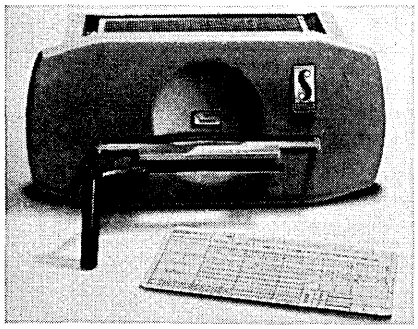


CIRCUIT INDICATOR

An illuminated status indicator for printed circuit boards, called Digistrip, is mounted directly to the board, singly or in required multiples. Lamp terminations are affixed to both sides of the board, and the status indicator itself can be utilized as a pull-handle for board removal.

Each unit uses ten T-1 size lamps. Total legend is 1.5", and overall size of the indicator is .25" wide x 1.873" long. Lamps can be replaced from the front of the indicator. The T-1 lamps are available in ratings from 1.5 to 28V. Display Devices, Inc., Santa Monica, Calif.

Circle no. 217 on Inquiry Card



STATIC CARD READER

The unit features contacts which sense punched holes mechanically. Normally-open contacts cannot close without the presence of a properly-oriented card due to a positive mechanical lockout. The reader reads all 960 (12 x 80) points on a standard IBM punched card simultaneously, is rated for a life of 1 x 10^6 operations, and can dissipate 60 watts maximum. Switches can carry 3.0 A static and 0.3 A during switching. Internal switch resistance is 30 milliohms maximum after 1 x 10^6 operations. Programming Devices Div. of Sealectro Corp. Mamaroneck, N. Y.

Circle no. 206 on Inquiry Card

NEW PRODUCTS

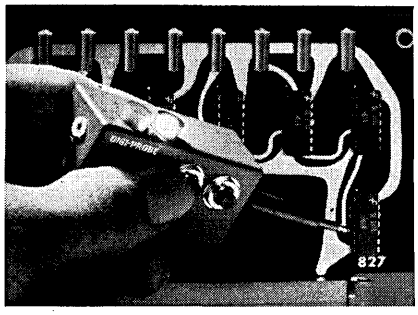
STORAGE UNITS

A program board organizer storage unit for use with Measurement/Data's Series 1100 family of low-cost automatic IC testers will hold up to 10 IC test program boards for either the 1100 or the 1110 testers. Two of the units will fit atop either tester making 20 test boards readily available to the operator.

The units have a drawer where connectors for all types of IC packages can be stored. The program boards are color-coded by connector-socket type.

A separate program board is used for each type of IC to be tested and each board is marked with the part number. Spare labels are included so that the part number can be changed if the program board is modified to test a different IC. Signetics Corp., Sunnyvale, Calif.

Circle No. 259 on Inquiry Card.



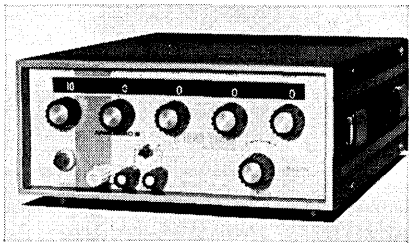
DIGITAL TEST PROBE

The Digi-Probe Model 1210 determines the presence and polarity of pulses in digital circuits and operates from a 5 V, 75 mA source.

A red and green indicator light in the hand-held probe allows non-technical personnel to perform most digital circuit production line checks.

The Model 1210 has an input impedance of greater than 75K ohms and can accommodate pulses to 24 volts. It can detect pulses as narrow as 25 ns and monitor a square wave pulse train to 15 MHz. Pulse Monitors, Inc., Moorestown, N.J.

Circle No. 204 on Inquiry Card.

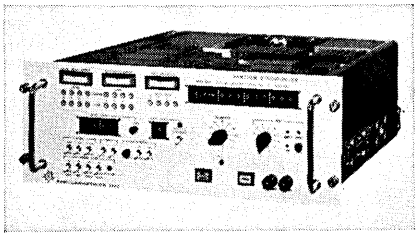


VARIABLE VOLTAGE STANDARD

AN3100 variable dc voltage standard provides 100 μV resolution of any voltage up to ±11.1110V. Five decades of control in constant increments are provided by front-panel rotary switches and a ±1 mV vernier. A built-in 100:1 divider permits an additional ±111.110 mV output range. Output current is 50 mA with short-circuit protection.

Warm-up time to rated accuracy (ISA) of 0.005% of reading ±50 μV is less than 10 minutes, and temperature coefficient over the 0°C to 70°C temperature range is 0.0002%/°C. DC output impedance is 10 milliohms, and external load capacitance has no effect on accuracy. Maximum common mode voltage is ±500 V. Analogic Co., Waltham, Mass.

Circle No. 213 on Inquiry Card.



PAM AND PDM DECOMMUTATORS

Designed for ultra-high-speed decommutation of PAM and PDM signals from 1 to 100,000 pps, Series APS-1000 decommutators provide selectable computer or manual control of all operating functions. Also provided is complete input signal conditioning and synchronization (frame and pulse) for PAM-RZ/NRZ and PDM normal or differentiated signals and parallel analog and digital (10-bit) output data for recording and processing equipment.

Other features include: automatic digital ranging (level and gain) of the input amplifier; data zero and full scale correction servos; selectable frame lengths up to 999 channels; parallel and serial 10-bit natural binary outputs for each input data pulse. Stellarmetrics, Inc., El Segundo, Calif.

Circle No. 209 on Inquiry Card.

NUMERIC KEYBOARDS

Low-profile, unitized Model NW modules are available in both 12-key and 16-key arrangements in Form A contact structure with vertical columns bussed. The NW modules may be fitted together in a variety of combinations and colors without affecting crucial key spacing. Both square and truncated button styles have molded-in legending.

Terminations may be made to printed circuit boards or with quick-connect terminals. A wired and encoded version is also being offered. The silent keys which will function from +35°F to +125°F. Micro Switch, a division of Honeywell, Inc., Freeport, Ill.

Circle no. 239 on Inquiry Card

ACTIVE BANDPASS FILTER

The DE500 series of active bandpass filters with integral detector cover the 1 Hz to 10 kHz frequency range. Fast detector response time makes these units ideal for all tone-burst control applications—voice coding, acoustical coupling, facsimile, and frequency shift keying.

Typical for the 2125 Hz model is an 80 Hz passband with greater than 60 dB attenuation at 170 Hz.

Common features of the DE500 models include: Input signal, 1 to 5 Vrms; Input impedance, 600 ohms; Operating voltage, 12 to 15 Vdc at 100 mA; Size, 1x2x3″; Weight, 10 ounces. Diversified Electronics Company, Inc., Sunnyvale, Calif.

Circle no. 235 on Inquiry Card

DATA COUPLER

Series 1500 solid state Iso-Switches can transmit data at bit rates up to 500 kHz over a distance of 1,000 feet and up to 100 kHz over 10,000 feet. It will operate with as much as 500V offset between input and output and needs no external power supply; it operates entirely on signal power. Input voltage can range from ±15 V; output range is up to 150 mA. Any logic signal level conversion can be accomplished without additional level converting circuits. The series can be inserted directly into Dual In-Line IC package sockets, socket backplanes, and printed circuit card layouts for DTL, TTL and HTL ICs. Iso-Switch Corp., Costa Mesa, Calif.

Circle no. 233 on Inquiry Card

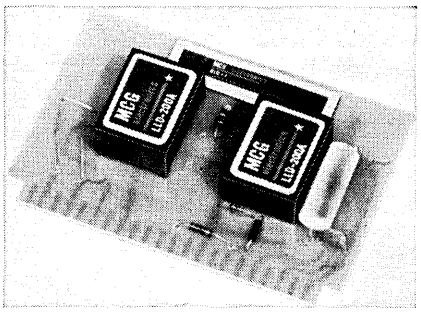
NEW PRODUCTS

A/D CONVERTER

Model HS-810 will assign up to ten million eight-bit binary numbers per second to a wideband analog signal. Codes available are straight or offset binary; 1's or 2's complement; or Gray.

The unit has a maximum error of 0.2% ±½ LSB and a maximum aperture time of 0.4 nanosecond. Complete with internal sample-and-hold, automatic test features, and power supplies. Input power 47-420 Hz; 115, 208, or 220 V. Computer Labs, Greensboro, N.C.

Circle no. 227 on Inquiry Card



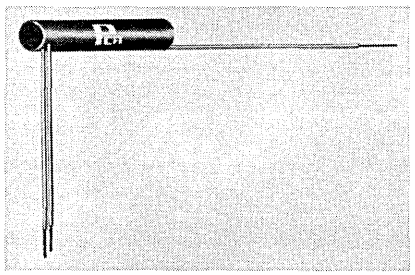
HIGH/LOW VOLTAGE DETECTOR

The HLD-1 will detect and indicate any voltage excursions—as short as 50 ns—above or below preselected voltage thresholds. The unit handles signals as high as 40V peak.

A modified version of the HLD-1 monitors sine, pulse or other repetitive input waveforms for amplitude changes on a one cycle basis up to 10 MHz. This requires that a suitably timed logic level signal be available to "enable" the unit at the proper time.

The HLD-1 is mounted on a glass-epoxy, printed circuit card measuring 4" x 2.75" x .75". The unit mates with a standard 22 pin connector. (.156 centers). MCG Electronics, Deer Park, N.Y.

Circle no. 214 on Inquiry Card



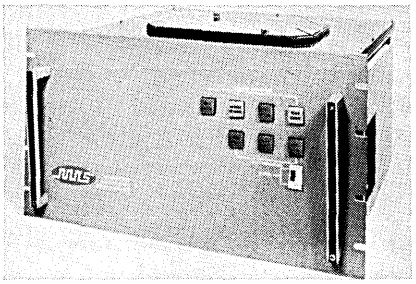
MOLDED DELAY LINE

Only 1.72 in. long, with a diameter of .308 in., this all-molded, miniature delay line is designed for use in computers, pulse forming networks, printed circuit boards and other applications where space is limited.

Delay lines feature a time delay of .21μs, ±.02μs, an impedance of 140 ohms and a maximum rise time of .04μs.

Temperature coefficient is 100PPM/C°. Standard models feature Type EE No. 22 AWG extruded, flexible Teflon leads with 1000V insulation. PCA Electronics, Inc., Sepulveda, Calif.

Circle no. 229 on Inquiry Card



DIGITAL BUFFER

Capable of accepting and storing digital information and transmitting it as required at the necessary speed and format, the Digi-Buffer uses independently-controlled dual capstan drives, one for recording and one for reading. Information is stored on a loop of standard magnetic tape; Model MS 200 is capable of storing 40,000 characters while Model MS 3000 stores up to 250,000 characters. Speeds are 0 to 200 wpm and 300 wpm respectively. The tape is driven directly from the motor shaft without the use of pinch rollers, brakes or clutches. Magnetic Recording Systems, Inc., Westbury, L.I., N.Y.

Circle no. 225 on Inquiry Card

IC OP AMP

The LM101A provides bias currents of 100nA and offset currents of 20nA over a −55°C to 125°C temperature range. Offset voltages of 3mV, offset voltage drifts of 15uV/°C, and offset current drifts of 0.2nA/°C are also guaranteed over full military temperature range.

The LM101A is interchangeable with the LM101 and the 709. The device also features: overload protection on the input and output, no latch-up modes, frequency compensation with a single 30 pF capacitor, and insensitivity to oscillation with capacitive loads or loose supply bypassing. National Semiconductor Corp., Santa Clara, Calif.

Circle no. 242 on Inquiry Card

10A NPN POWER TRANSISTORS

Three series of planar passivated transistors—the 2N4150, the 2N2811-2N2814, and the new 2N5552—provide the following electrical characteristics: Sustaining Voltage, 80 V min @ 100 mA; Current Gain, 50 min @ 5A, 30 min @ 10A; Saturation Voltage, 1.0 V max. @ 10A; Turn-on Time, 100 ns. max. @ 5A; Turn-off Time, 700 ns max. @ 5A.

Of particular significance in this series is the 2N5552, a 10 A power switch, which offers high-speed switching in a low thermal resistant (15 Watts @ 100 degrees Centigrade) TO-5 package. Solid State Products, Div. of Unitrode, Salem, Mass.

Circle no. 241 on Inquiry Card

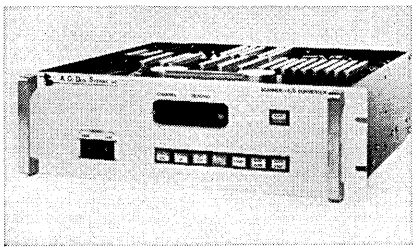
DUAL DIFFERENTIAL-INPUT AMP

The L120 dual differential-input amplifier consisting of 14 MOS FETs and 12 bipolar transistors on a single chip, 55 x 65 mils, can be used for sample and hold, integrating and fast voltage comparison applications. The amplifier is unity gain stable with no external components. Typically, input bias current is 20 pA, input resistance is 2 x 10^{11} ohms. Output slew rate is 20 V/μs and the open loop voltage gain is 360. The two amplifiers operate from ±15 volts and give ±12 volts out into a 20K load.

The L120 is packaged in the 10-lead TO-100 configuration. Siliconix, Inc., Sunnyvale, Calif.

Circle No. 249 on Inquiry Card.

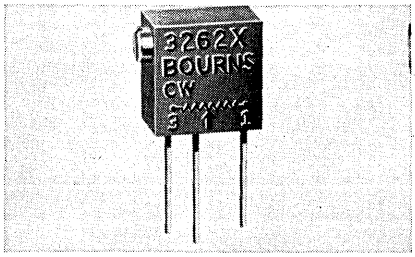
NEW PRODUCTS



SCANNER A/D CONVERTER

Series 013-022 features: Multiplexer speed to 400 samples per second; integrated circuit design throughout; A/D converter capable of 10,000 readings per second; visual, front panel readout in decimal form; channel I.D. available in BCD 1-2-4-8 with complementary logic levels or in decimal code; random access permits complete computer control of scanner if required. Accuracy of A/D converter, .025% of f.s. ±lsd; resolution of A/D Converter, 1%. Pin board allows programming of 4 functions per channel. Analog Digital Data Systems, Inc., Rochester, N.Y.

Circle No. 215 on Inquiry Card



CERMET POTENTIOMETER

Model 3262, a 12-turn pot, measures .25" x .25" x .17". It has a 0.25 watt power rating at 85°C, a standard resistance range of 10 ohms to 1 megohm, and an operating temperature range of −65 to +175°C. Standard specifications include Resistance tolerance, ±10%; Temperature coefficient, 150 ppm/°C (100 ppm/°C available); Absolute minimum resistance, 1 ohm all resistances; Mechanical Life, 200 cycles without discontinuity; Load Life, 1000 hours at rated power. In addition, the Model 3262 cermet adjustment potentiometer is rated at 30G vibration and 100G shock. It meets or exceeds all applicable requirements of MIL-R-22097. Bourns, Inc., Trimpot Products Div., Riverside, Calif.

Circle No. 212 on Inquiry Card

ANALOG-TO-DIGITAL CONVERTER

Model 8050 incorporates full digital baseline offset for any channel address from 0 to 8191. With built-in single channel analyzer, baseline restorer, flexible coincidence circuitry, channel compression; 0.01% stability and 0.025% linearity at 50 MHz digitizing rates. Used with Geoscience Series 7000 Digital Processors. Price—$2,500. Geoscience Nuclear, Div. of Geoscience Instruments Corp., Hamden, Conn.

Circle No. 254 on Inquiry Card.

READOUT INDICATOR

The MG-19 ELFIN has a maximum diameter of 0.413 inches and features a character height of 0.433 inches. In addition to numerals, the readout will display a decimal point, a plus or minus sign and some alphabetic characters. Viewing angles up to 150 degrees are obtained. The neon elements have a maximum breakdown voltage of 180 Vdc. Each cathode draws approximately 0.5 mA. External resistors must be placed in series with each cathode to limit the current to a specified safe maximum or less. The readouts are suitable for dc or pulsed operation. Maximum height of the glass tube is 1.535". Alco Electronic Products, Inc., Lawrence, Mass.

Circle No. 248 on Inquiry Card.

DATA ACQUISITION SYSTEM

Model 710 contains a 16-channel FET multiplexer which is expandable to 64 channels with a switching speed of 1μs per channel. Accuracy of the integrating digitizer is 0.015% of full scale at a speed of 15 ms per conversion. Optional successive-approximation A to D converter is available with an accuracy of 0.025% at 50 us per conversion.

Control and display panel includes a sample rate switch, 5-digit file number entry switch, and multiplexer controls. The data and MUX address are displayed on incandescent lamps, with Nixies optional.

Standard output medium is 7-track, computer-compatible magnetic tape. Packing density is 556 bpi and maximum operating speed is 300 c/s. 4,000 c/s continuous rate is optional. Dimensions are 21" x 23" x 25½". IRA Systems Inc., Waltham, Mass.

Circle No. 247 on Inquiry Card.

HIGH SPEED TAPE SPOOLER

Type 4030 tape spooler is capable of speeds up to 60 inches/second (reading speed), and contains a servo mechanized tape tension system that ensures trouble-free handling of tape at high speeds. A high speed rewind facility permits tape to be rewound at speed of up to 180 inches/second in either direction.

The unit is equipped with 8" NAB reels, which store up to 800 feet of 0.0045" paper tape. To facilitate tape loading, each servo arm can be latched at its outer extremity. Ferranti-Packard Electric Ltd., Electronics Div., Ontario, Can.

Circle No. 250 on Inquiry Card.

DISC MEMORIES

A series of head-per-track disc memories that interface directly with all types of commercial digital logic: TTL, DTL and RTL. The memories use an "in-contact" recording technique to store up to 6.4 million bits on a single disc surface.

Available are Model F6 (6.4 million bits), Model F3 (3.2 million bits), Model F1.5 (1.6 million bits), and Model F.75 (0.8 million bits). Average access time is 16.7 ms, and data transfer rates can be as high as 3 million bits per second. A complete memory system occupies 8-¾" of rack space. A separate power supply is available as an option. Data Disc, Inc., Palo Alto, Calif.

Circle No. 245 on Inquiry Card.

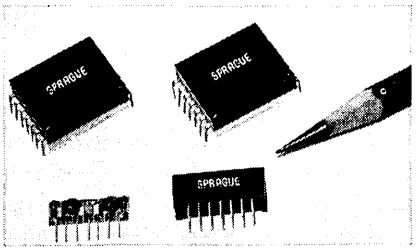
LAMP AND RELAY DRIVER

Model 831 is a hybrid cermet thick-film driver which provides a convenient pre-engineered interface between digital IC levels (typical to computer logic) and output or control devices which demand considerably larger power levels.

It provides the complete required step-up in power level without the need for external pass transistors. It features a 0 to +60 V operating range; two circuits per package; a 0 to 1 A current capability (1.8 A in parallel); standard DTL input levels, and a −55° to +125°C operating temperature range.

Completely self-contained, this solid-state unit occupies 0.5 sq. in. of board space. It is fully sealed and environmentally tested. Helipot Div., Beckman Instruments, Inc., Fullerton, Calif.

Circle No. 246 on Inquiry Card.

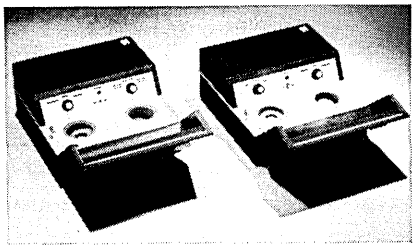


MEMORY DRIVE MODULES

Type 905Z and 906Z Moduline ™ memory-drive circuit assemblies combine miniaturized inductive elements with metal-film resistors on ceramic substrates. The hybrid driver packages are available in jumbo dual in-line packages (Type 905Z) as well as DIP assemblies (Type 906Z).

The modules make it possible to obtain, in one package, pulse characteristics necessary for functional operation without the need for developing an elaborate system of guard-band tolerances on individual components required for discrete component assemblies which have hitherto been used for computer memory-drive circuits. Sprague Electric Co., North Adams, Mass.

Circle no. 220 on Inquiry Card

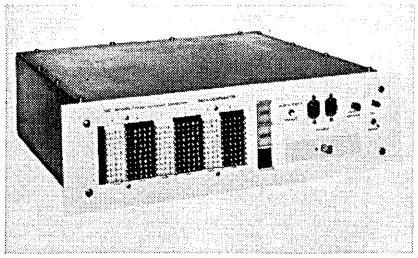


ACOUSTIC DATA COUPLERS

Model 300, with a standard telephone, can be used as a communications tool for terminal-to-computer operations, and for data conversations or information input/output between two terminals. Model 260, with a standard telephone, can be used to couple a remote terminal to a time sharing computer.

Both acoustic data couplers transmit data from the terminal to the coupler where it is transformed into modulated tone signals. These signals then are acoustically transferred to the telephone handset placed in the coupler's cradle and sent to the time sharing computer over an ordinary telephone line. Dura, Div. of Intercontinental Systems, Inc., Palo Alto, Calif.

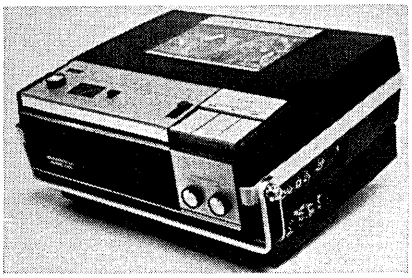
Circle no. 216 on Inquiry Card



DATA COMPARATOR

Series 800 is a programmable data comparator that provides monitoring of up to 100 points, with a point scanning frequency of 200kHz. Programming is sequential. Specifications include: Capacity, 20, 40, 60, 80 or 100 points for one limit only or coincidence detection of 10, 20, 30, 40 or 50 points for two limits; Data word length, four BCD digits, plus signal; Address, two-digit BCD set of signs; Input signal voltage, 10V p-p max. Switching threshold, +2.5Vdc or —2.5-Vdc; Output voltage, —2 to —20V (below ground) for negative swing, or from +2 to +20V (above ground) for positive swing. Systems Research Corp., Los Angeles, Calif.

Circle No. 228 on Inquiry Card



MAGNETIC TAPE UNIT

Model DV-315 completely self-contained portable magnetic tape unit has one million character storage capacity, is only 6" high x 12" wide by 10" long, and weighs approximately 15 lbs.

Standard 5" reels of ¼" tape are employed with a speed of 7½" per second. Interfaces for most commonly used small computers are packaged as part of the unit. Data is recorded using phase modulation techniques and the basic transfer rate is 3.5 Kbps.

Its portability makes it ideally suited for field maintenance and allows it to be shared among many centrally located computer systems. Betatech, Inc., Bedford, Mass.

Circle No. 205 on Inquiry Card

SQUARETRIM CERMET POTS

A line of cermet ½" Squaretrims, series 556, 557 and 558, are available in base pin, flexible lead and side pin models and offer essentially infinite resolution and low temperature coefficient. They are available in values from 200 ohm to 1 megohm, have a power dissipation of 0.75 watts @ +85° C, and feature exceptional stability when subjected to rigorous extremes of environmental stress. Operating temperature range is from —55° C to +150° C. Weston Components Div., Archbald, Pa.

Circle No. 261 on Inquiry Card.

ONE-OF-16 DIGITAL DECODER

The 9311, a MSI circuit designed to convert four digital inputs into one of 16 mutually exclusive digital active-level low outputs features a built-in enabling capability and high speed performance (20 ns through delay).

These features make the device suitable for a wide variety of cascaded decoding, demultiplexing and conversion applications. Systems which can benefit most from the 9311 design are digital systems for computers, process control, radar, display, communications, data acquisition and instrumentation.

The 9311 is available in a 24-pin hermetic Dual In-Line package and flatpack. Fairchild Semiconductor, Mt. View, Calif.

Circle No. 240 on Inquiry Card

PORTABLE 5" OSCILLOSCOPE

The PM 3221 5" (10 x 8 cm useful display area) single beam oscilloscope offers two frequency/sensitivity ranges: dc to 10 MHz at 10 mV/cm and dc to 2 MHz at 1mV/cm. A time/cm selector provides for triggering on frame and line signals of all present black/white and color TV systems as well as for horizontal deflection with an external signal (sens. 1 V/cm dc coupled to 1.5 MHz.). Other features include: dc zero reference; calibrating voltage (5 Vpp at 8 kHz, square wave); and vertical signal magnification of 3x (for 24 cm of undistorted vertical deflection); signal delay 100 ns. The time base generator allows continuous or stepped adjustment of time/cm in a 1, 2, 5, 10 sequence; sweep expansion of 1, 2, or 5x. Philips Electronic Instruments, Mt. Vernon, N.Y.

Circle No. 258 on Inquiry Card.

SIGNAL PROCESSING SYSTEM

A signal processing system, Compu-Signal System-3 (CSS-3) is a desk size unit with teletypewriter, input sampling, display, output, control, and software included. It is capable of continuously performing fast fourier transforms (FFT's) in real time to 2.0 kHz bandwidth or in blocks of real time to 35 kHz bandwidth.

The CSS-3 performs FFT's, zoom FFT's, auto correlations, cross-correlations, convolutions, averaging, histograms, a variety of filters and other standard signal processing routines. Computer Signal Processors, Inc., Waltham, Mass.

Circle No. 260 on Inquiry Card.

PUNCHED TAPE READER

The EECO 3100 ruggedized photoelectric reader will withstand 2g vibration from 5-33Hz, and 25g shock. Operating temperature limits are —40°C to +70°C.

It uses standard 8-level, 1" wide punched aluminized mylar, paper mylar or paper tape and operates free run or rewind at 300 cps. Spooling will handle up to 100 feet of tape (12,000 characters), spooled to and from removable reels. Output is 8 bits plus sprocket—the sprocket output is available as a clocking signal.

Power requirements are +5 Vdc at 1 A; 115 Vac, 60 Hz at 100 mA. It measures 8"w x 3½"h x 5¾"d and weighs 5½ lbs. Electronic Engineering Company of California, Instruments Div., Santa Ana. Calif.

Circle No. 232 on Inquiry Card

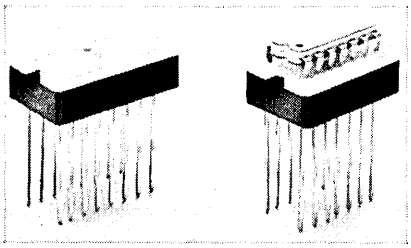
COUNTING DISPLAY

MDP Series of panel-mounted, multi-decade counting displays with built-in preset comparator consists of a counting module and digital display plus a thumbwheel-operated digital comparator. The count can be stored in the display at its preset count value or automatically reset to zero after the preset number has been reached.

The outputs from the MDP Series are: 1. a visual display of the number counted; 2. a flip-flop signal indicating when the preset number has been counted; and 3. complimentary BCD output from the counter. It also has a carry output from the most significant decade and may be reset at any time.

The MDP is available in any combination from 1 to 9 count—display—preset positions. Instrument Displays, Inc., Haverhill, Mass.

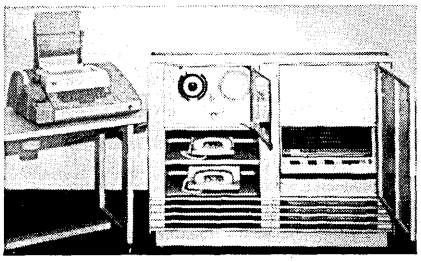
Circle No. 257 on Inquiry Card.



D.I.P. SOCKETS

Series 8359 D.I.P. sockets are universal mounting devices for all standard dual in-line package IC's with 14 or 16 pins. Compact, low profile insulator permits high packaging density. Side-by-side mounting on ½" centers; in-line mounting on .800" centers (14 pin) or .900" centers (16 pin). Easy D.I.P. insertion is due to chamfered edges on the D.I.P. lead entryways. Insulator lid is removable to allow access to contacts. Contacts have a double-leaf design for positive wiping action against dip leads. Contact tails are .025" square and are available in lengths for solder or wire-wrap terminations. Socket is mounted to p.c. card with a 1/16" rivet; metal plate mounting special adapter. Elco Corp., Willow Grove, Pa.

Circle No. 221 on Inquiry Card



DATA STATION

The DS-20 contains a small programmable computer, a 7- or 9-track compatible read/write magnetic tape system, ASR-33 teleprinter, and an interface to a Western Electric Type 103 or 202 data set. Options include a multiplexer to service up to 32 teletypes, IBM Selectric typewriter, interfaces for 201 or 401 data sets, control unit for automatic dialing, and additional tape drives. Two-way communication is effected through the TWX or Telex networks, or over ordinary dial-up or leased telephone lines. The DS-20 exchanges data with IBM transceivers, 2740 and 1050 terminals, teletypes, CalComp plotters, CRT displays, card readers, paper tape readers, other I/O devices and other DS-20's. Infotec, Inc., Rye, N.Y.

Circle No. 224 on Inquiry Card

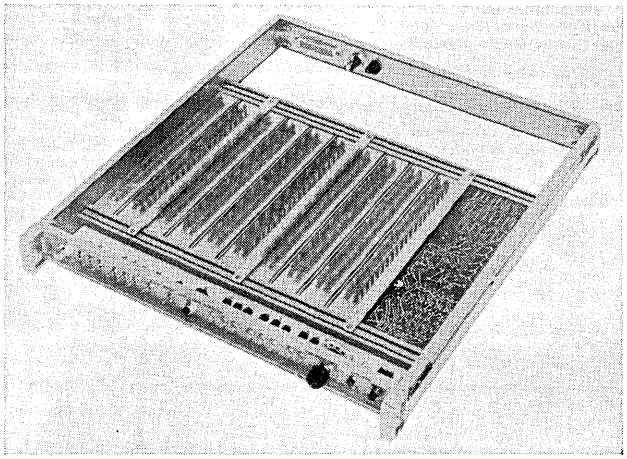
NEW PRODUCTS

PLATED WIRE MEMORY STACKS

Memory stacks have typical read cycle times of 150 nanoseconds with a 400 nanosecond write cycle. The basic stack size is 8,192 words of 18 bits. Other stack sizes, such as 16K x 9, 4K x 36 and 2K x 72, can be derived from the basic unit. The stack is designed to operate in a non-destructive read-out mode with equal read and write word currents.

The memory is made up of two double-sided planes with 256 word lines with 144 plated wires on each plane. The overall stack size is 9" high by 19½" long and 1⅞" wide. The plane construction offers single turn word line with one crossover per bit and one noise cancellation wire every four plated wires. Word line current is 900 mA nominal and digit line current is ±40 mA nominal. Output voltage ranges from 3 to 5 mV after a worst case disturb pattern. Ferroxcube Corp., Saugerties, N. Y.

Circle No. 244 on Inquiry Card.



DUAL IN-LINE PACKAGING DRAWERS

Four models of horizontal equipment drawers, specifically designed for dual in-line packaging offering integral drawer slide/side panels and one-piece multi-purpose front and back panels, are available in a new integrated circuit packaging system.

Equipment drawers, Models DHA, B, C and DHD, manufactured of sturdy extruded aluminum, are EIA standard 1¾" high and installed in a standard 19" equipment rack.

Models DHA, B, and C feature integral power buss bars running parallel to the front of the drawer which hold the DIP carrier stix running perpendicular to the front of the drawer. Model DHD has integral power buss bars running perpendicular to the front of the drawer and mounts the DIP carrier stix parallel to the front panel.

Models DHA and DHD are center mounted drawers, Model DHB is front to back mounted and model DHC is back to front mounted. Scanbe Manufacturing Corp., Monterey Park, Calif.

Circle No. 230 on Inquiry Card.

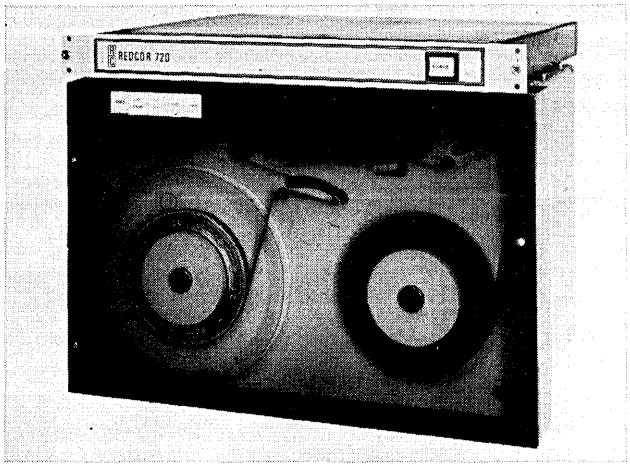
SYNCHRO/DIGITAL CONVERTER

An airborne synchro-to-digital conversion system contained in a 200 cubic inch package, converts synchro inputs to a binary code equivalent. A multiplexer selects one of five specified input synchros from an external address command signal, then the synchro under test is converted to a resolution and accuracy of 13 bits.

The maximum conversion time for a 180° change of input angle is 10 ms. At the end of the conversion period, a data ready signal is generated for data transfer as a parallel binary output. This signal indicates completion of conversion with the output data representing the equivalent input synchro shaft angle.

The unit is contained in a single package with overall dimensions of 4.5″ h x 5″ w x 8.9″ l and weighs 6.95 lbs. Astrosystems, Inc., New Hyde Park, N. Y.

Circle No. 243 on Inquiry Card.



DATA ACQUISITION SYSTEM

The 720999 System is designed to acquire analog data from a variety of scientific experiments and record the digital equivalent of that data on an incremental magnetic tape recorder to be processed by a digital computer.

Throughput rate of the system is determined by the tape recorder. The basic system consists of a multiplexer, sample and hold, AD converter, sequence control, format unit and an incremental magnetic tape recorder. Options are available for various acquisition rates, tape densities, and 7- and 9-track formats.

Features include complete system in one unit suitable for 19″ RETMA rack mounting, selectable record lengths to fit existing computer programs, and an optional digital multiplexer.

System specifications are: number of channels—16 (single ended); voltage range—±10 V full scale; sample rate—up to 500 samples per second with resolution of 12 bits; accuracy —±0.05% of full scale (±½ LSB); power—115 V, 50-60 Hz; and size—19″ wide, 14″ high, and 18″ deep. Redcor Corp., Canoga Park, Calif.

Circle No. 231 on Inquiry Card.

NEW PRODUCTS

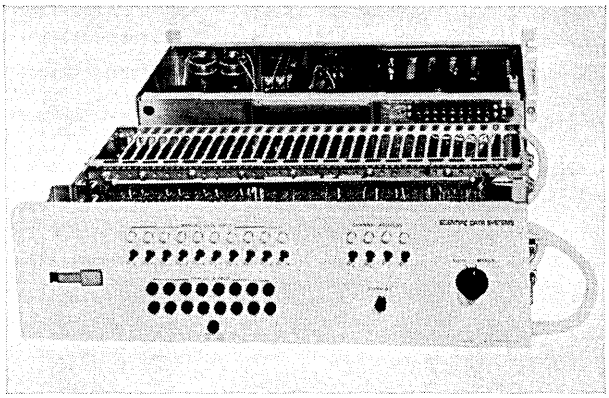
7-TRACK DATA RECORDER

The KB-600 Datascribe™ features a 64-character moveable keyboard with 16 special keys for control or BCD codes, stylized panel controls, direct-reading visual displays, keyboard interlocks, automatic audio-visual error annunciation and noise-abating tambour doors.

The datascribe's tape transport provides automatic tape positioning and recording, verifying and searching at speeds of up to 32 ips. A high-speed rewind is also featured. Recording in gapped format at a packing density of 200, 556 or 800 bpi is a standard feature. Full tape security checks are provided, including longitudinal, lateral and bit-by-bit comparison with memory.

Options available with the KB-600 include alternate programs, expandable memories, reusable program storage, left zero programming, odd or even parity and expandable record sizes from 80 to 200 positions. Vanguard Data Systems, Newport Beach, Calif.

Circle No. 251 on Inquiry Card.



DIGITAL-TO-ANALOG CONVERTER

The DA40 D/A Converter provides 16 channels of analog output (from 10-bit digital input) in a compact, self-contained package. Up to 16 DA40 assemblies can be connected to the same input lines to form larger systems with as many as 256 analog outputs. A front panel for full manual control is available and the unit contains its own power supply.

The DA40 accommodates all the digital functions associated with conversion, including unit-address and channel-address decoding. Control circuits route the 10-bit input data to the desired channel. Each channel contains an internal register to store the digital data during conversion, allowing new data to be inserted at 2μs intervals. Either a direct logic interface or a remote cable interface is provided to connect the digital controlling device. Negative values of digital input can be in either two's complement or one's complement form.

Analog output is accurate to within 0.1% of full scale; maximum output swing is −10V to +10V, at full load current of ±20 mA. Scientific Data Systems, El Segundo, Calif.

Circle No. 201 on Inquiry Card.

LOGICAL COMPUTER

Model LC44 is a small logical computer, suitable for study of Boolean relationships, including those with feedback. It has four inputs and four outputs. Each output may be programmed to be any Boolean function of the four inputs. Programming is accomplished by pinboard. The four inputs may be set by their panel switches or an external logical source. Each output has an indicator lamp and is buffered to drive external devices. Outputs may be fed back into inputs to provide logical equivalents of flip-flops, counters, linear sequences, etc. Construction is TTL, 5 volt silicon DIP logic. DVC, Dayton, Ohio.

Circle No. 255 on Inquiry Card.

AUTOMATIC WIRING AND CIRCUIT ANALYZER

An automatic test system checks point-to-point continuity of electronic equipment wiring and circuitry at speeds as fast as 3,000 termination points per minute. The OmniTester Model 1000 checks continuity resistance, hi-pot, leakage resistance and dynamic characteristics.

In continuity testing the OmniTester not only verifies the presence of required wiring, but also checks to insure that no extra connections are present. In dynamic testing, it verifies the presence of required voltages, currents, impedances, or resistances in response to programmed stimuli. Test results are printed out in permanent record form.

The tester employs a self-programming feature which enables it to prepare its own punched tape program by automatically analyzing a known working sample of a production prototype of the wiring. Expansion of the basic system capacity to test as many as 100,000 termination points is easily and economically accomplished by the addition of modular plug-in units of 30 points each.

The basic model is housed in a single console which measures 51" h x 28¼" w x 26½" d. Teleproducts, Inc., Moorestown, N.J.

Circle No. 253 on Inquiry Card.

RFI FILTERS

Four RFI filters for data processing equipment feature the following parameters:

Type E-5177, 2x30 A, 250 Vac. Dimensions: 9.75 in. long x 6.0 in. wide x 2.38 in. high. Attenuation: greater than 50 dB from 150 kHz to 1 MHz.

Type F-5120, 25 A, 250 Vac. Dimensions: 3 1/16 in. long x 1⅝ in. wide x 2⅞ in. high. Attenuation: greater than 50 dB from 300 kHz to 10 MHz.

Type F-5121, 3x50 A, 230 Vac. Dimensions: 8.5 in. long x 4.25 in. wide x 2.88 in. high. Attenuation: greater than 40 dB from 300 kHz to 10 MHz.

Type F-5122, 3x10 A, 230 Vac. Dimensions: 6 in. long x 6 in. wide x 2 in. high. Attenuation: greater than 40 dB from 300 kHz to 10 MHz. Hopkins Engineering Co., San Fernando, Calif.

Circle No. 252 on Inquiry Card.

LITERATURE

Discrete Semiconductors

A line of discrete devices from diodes to FETS to power transistors are listed in this catalog. Fairchild Semiconductor, Mt. View, Calif.

Circle No. 329 on Inquiry Card

Micro-Logic Cards

A 44-page catalog lists and describes the electrical and mechanical features of a line of 5 MHz micro-logic circuit cards, designated Series C 150 T. Control Logic, Inc., Natick, Mass.

Circle No. 303 on Inquiry Card

Brushless DC Motor

A line of miniature brushless dc motors with solid-state controls is the subject of this two-color, 4 page booklet. Siemens America Inc., Power Equipment Div., New York, N. Y.

Circle No. 320 on Inquiry Card

Instrumentation Training Aids

An illustrated brochure, titled "Instrumentation Training Aids," describes educational films and texts on instrumentation technology that may be rented and purchased. Instrument Society of America, Pittsburgh, Pa.

Circle No. 306 on Inquiry Card

Connectors and Terminals

Specifications for 0.062 miniature and 0.093 standard nylon connectors, connector housings and pin terminals are contained in a 6-page illustrated catalog. Molex Products Co., Downers Grove, Ill.

Circle No. 312 on Inquiry Card

Tape Recorders

Analysis of wideband rotary-head instrumentation tape recorders and their applications are presented in a reprinted article, "Rotary-Head Instrumentation Recorders: Description and Uses" by Robert Horn. Ampex Corp., Redwood City, Calif.

Circle No. 301 on Inquiry Card

MOS Static Shift Registers

A 20-page application report features MOS shift registers and how to use them in bipolar logic systems Texas Instruments, Inc., Dallas, Texas.

Circle No. 317 on Inquiry Card

Computers

The latest issue of *Computer Usage*, a quarterly publication, deals with "Computers and the Stock Market." Computer Usage Co., Inc., Communications Department, Mt. Kisco, N.Y.

Circle No. 304 on Inquiry Card

SDS Quarterly Magazine

"SDS and the Industry in Perspective" is the title of the feature article in the latest issue of *Interface 16*, a 12-page quarterly magazine. Scientific Data Systems, El Segundo, Calif.

Circle No. 324 on Inquiry Card

IC Cards

A performance specification and applications bulletin describes the MST—2 level comparator IC card for dc level detection, wave form restoration, pulse shaping and Schmitt triggers. Wyle Laboratories, El Segundo, Calif.

Circle No. 309 on Inquiry Card

Dual In-line Packaging

Dual in-line packaging, a new concept in high density packaging of dual in-line integrated circuit modules, is described in a 20-page designer's catalog. Scanbe Manufacturing Corp., Monterey Park, Calif.

Circle No. 313 on Inquiry Card

Cold Cathode Display Tubes

This data sheet describes the Datecon DT series of low cost cold cathode display tubes, which meet virtually all requirements—side view, end view, left and right hand decimal points. Integrated Circuit Electronics, Inc., Waltham, Mass.

Circle No. 307 on Inquiry Card

AC Generator

Brochure #2010-PDL-868 features an AC generator brush type or brushless, class 720. Kato Engineering Co., Mankato, Minn.

Circle No. 308 on Inquiry Card

Serial Printer

A basic description, features, and detailed specifications of the serial character printer SCP-12 are included in an illustrated brochure. Adtrol Electronics, Inc., Philadelphia, Pa.

Circle No. 314 on Inquiry Card

PC Edge Card Connectors

A catalog data sheet provides information on military-grade printed circuit edge card connectors on .156 centers with wire wrap terminations. Viking Industries, Inc., Chatsworth, Calif.

Circle No. 326 on Inquiry Card

Electronic Consotrol Instruments

Bulletin C-10A summarizes and illustrates the design features, applications and versatile mounting of a complete line of small-case, solid-state electronic Consotrol instruments. The Foxboro Co., Foxboro, Mass.

Circle No. 311 on Inquiry Card

Multiconductor Cable

The steps utilized in producing the multiconductor cables: extrusion, shielding, wrapping, and jacketing are described and illustrated in a four page brochure. Microdot Inc., South Pasadena, Calif.

Circle No. 327 on Inquiry Card

Unidirectional Stepping Motors

Five catalog bulletins provide detailed specifications on a series of unidirectional Cyclonome® stepping motors. A 4-page cover bulletin describes design and performance features and principle of operation. Sigma Instruments, Inc., Braintree, Mass.

Circle No. 310 on Inquiry Card

Data Generator

This bulletin contains advance specifications for the Model 214 data generator, a 13-channel pattern generator with 10 MHz stepping frequency, suitable for design and testing memory elements, memory systems, telemetry systems, and digital logic systems. Datapulse Div., Systron-Donner Corp., Culver City, Calif.

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Power Supply

A 5 to 240-volt series of all-silicon, modular power supplies is described in the two-color technical bulletin, LA968E, including full electrical and mechanical specifications. Mid-Eastern Industries, Inc., Scotch Plains, N. J.

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Stepping Motors

A 16-page brochure describes the latest state-of-the-art in stepping motors. The booklet contains a thorough explanation of PM, VR and small angle steppers, complete with detailed specifications and usage. Computer Devices, Inc., Santa Fe Spring, Calif.

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Printed Circuit Connectors

A comprehensive line of printed circuit connectors is the subject of a 24-page catalog. Included are photographs, line drawings, electrical characteristics and mechanical specifications. Amphenol Industrial Div., The Bunker-Ramo Corp., Chicago, Ill.

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Analog/Hybrid Computers

Two additions to the EAI Applications Reference Library are a 13 page report entitled "Analog Computer Simulation . . . A Way of Thinking" and a 14 page report entitled "Hybrid Simulation of an Exchanger/Reactor Control System." Electronic Associates, Inc., West Long Branch, N. J.

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Solid-State Displays

A 12-page bulletin on solid state displays discusses the three important solid-state technologies of magneto-optics, electroluminescence, and light-emitting semiconductor devices. General Electric Co., Syracuse, N. Y.

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Pushbutton Switches

A complete line of illuminated pushbutton switches and matching indicator lights, featuring a versatile range of mounting hardware and improved styling, is described in this catalog. Marco-Oak, Div. of Oak Electro/Netics Corp., Anaheim, Calif.

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Data Acquisition System

This brochure provides detailed product information, block diagrams and complete specification data on the Models 1000 and 1500 analog/digital acquisition and recording systems. Datatron, Inc., Santa Ana, Calif.

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Micro-Miniature Potentiometers

Comprehensive data on a series of micro-miniature, trimmer potentiometers is presented in an illustrated brochure, entitled "Micro-Miniature Trimmer." Electrical, mechanical and environmental specifications are detailed. Minelco, Holbrook, Mass.

Circle No. 318 on Inquiry Card

Quality Assurance

Quality assurance is the subject of this 16-page brochure which graphically depicts the three interrelated quality disciplines at Micro Switch: quality control, product assurance and quality appraisal. Micro Switch, a division of Honeywell Inc., Freeport, Ill.

Circle No. 315 on Inquiry Card

Time-Sharing

A four-page brochure describes the time-sharing concept of computer usage and analyzes the inherent advantages. Remote batch processing and on-site processing are explained, and various computer languages listed. Remote Computing Corp., Los Angeles, Calif.

Circle No. 305 on Inquiry Card

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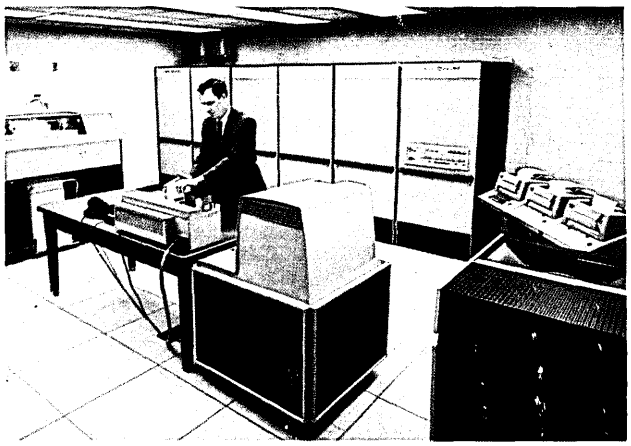

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