COMPUTER DESIGN

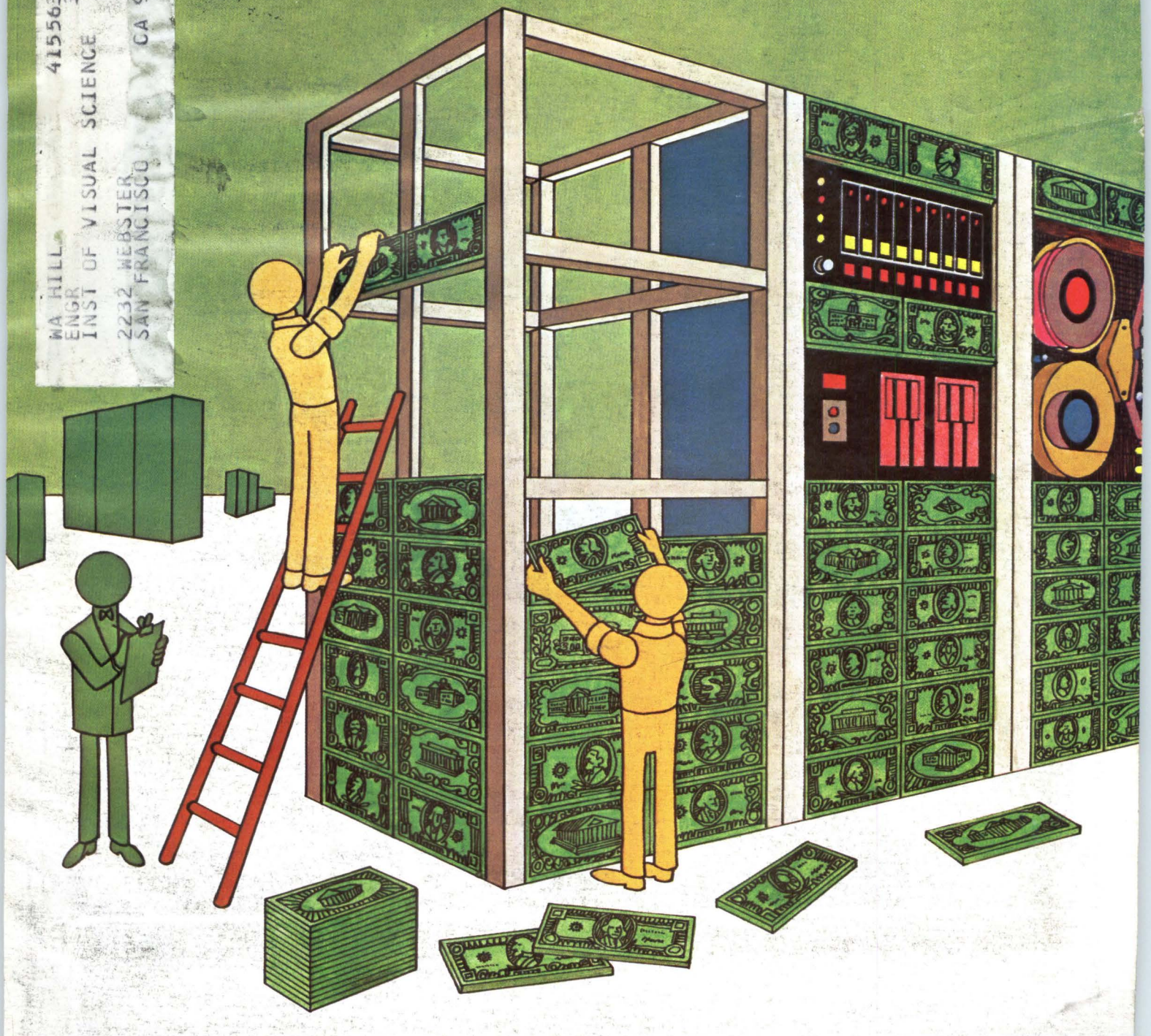
THE MAGAZINE OF DIGITAL ELECTRONICS

SEPTEMBER 1978

ANALYZING COMPUTER TECHNOLOGY COSTS
PART 1: Development and Manufacturing

DESIGNING INTERRUPT STRUCTURES FOR MULTIPROCESSOR SYSTEMS

INTERPRETATION OF DATA CONVERTER ACCURACY SPECIFICATIONS



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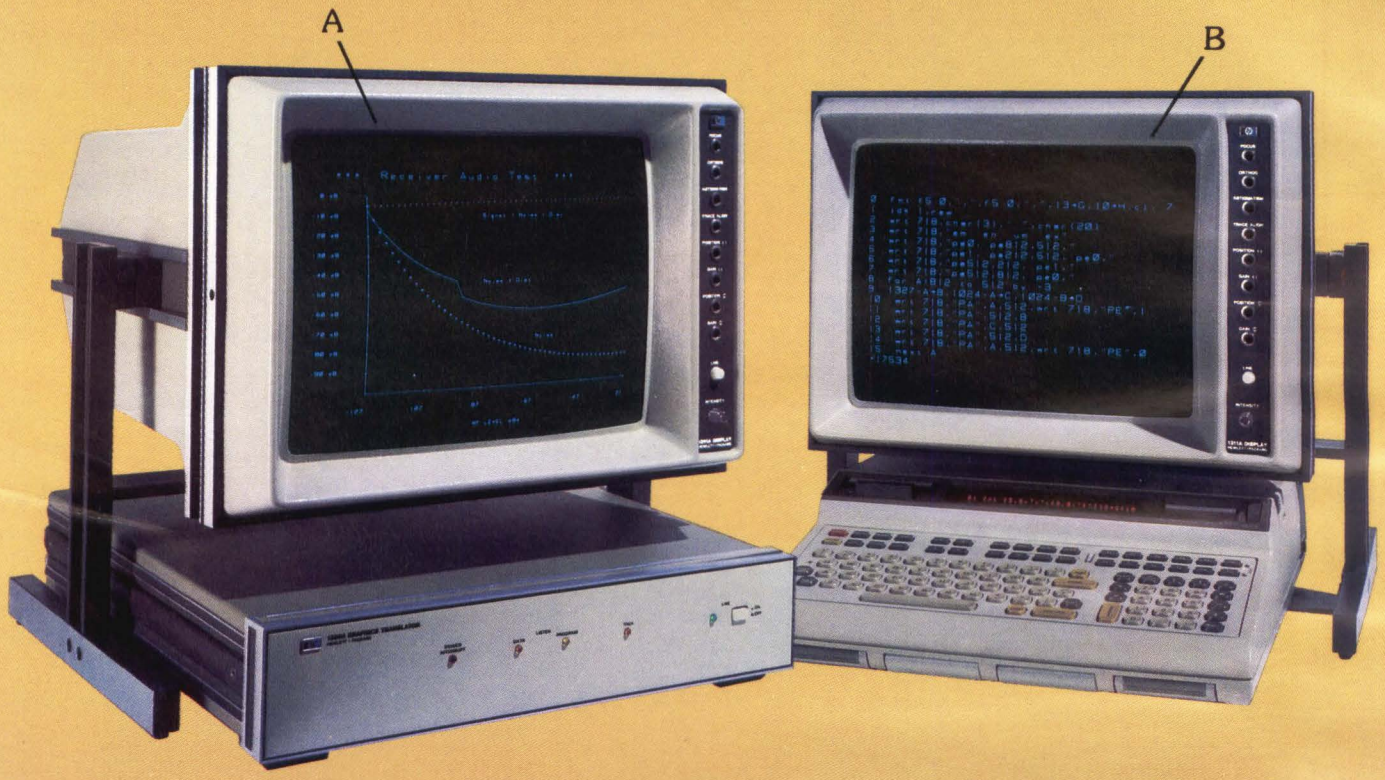

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DEPARTMENTS

BPA

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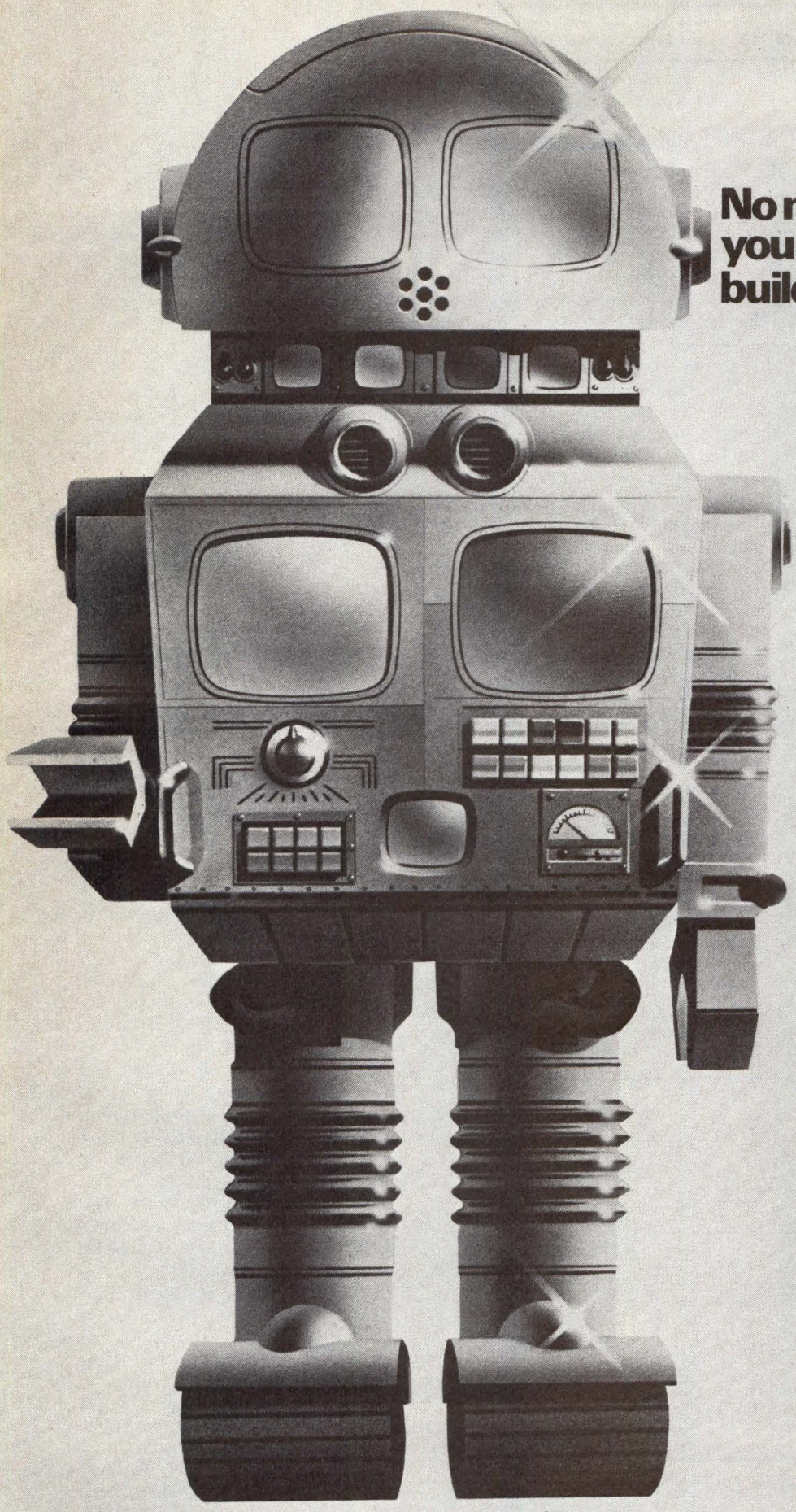

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CIRCLE 5 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

The Tech Brief entitled "Exclusive-OR Frequency Multiplier" (*Computer Design*, June 1978, p 130) interested me for a variety of reasons.

Firstly, the circuit depicted is a somewhat general configuration of those used by a variety of design engineers engaged in digital logic circuitry. Specifically, the circuit shown in the Figure here is frequently used to recover a clock signal from the least-significant binary stage of a natural binary or natural BCD counter.

The value of "recovering the synchronous clock" is an enormously powerful tool when one is comparing the 24 or more parallel data lines from a remote source against another number set in a noisy environment. This is especially so with today's high speed digital readouts found in almost all large machine shops—many of which are included in the actual servo loops of the positioning system.

It appears to be a commonplace omission that every readout furnished to customers for the past 15 or so years never provided a synchronous clock with the "optional BCD output." Hence, there is the need for a reconstructed clock to strobe high speed comparators at the change of the first binary stage. (It is impossible to have more significant stages change count during normal operation of a natural binary or natural BCD counter unless the LSB binary "flips" first—assuming, of course, that direct preloading is disabled.)

History of the "strobe circuit" depicted in the Figure appears to be somewhat obscure. However, in 1970-71, Mssrs Tripp and Plummer of Farrand Optical Co thrust the above circuit into this writer's lap when the TTL posed some interesting timing problems to the contemporary designer of that period.

The basic concept goes back even further though, since a rather slow moving Eccles-Jordan vacuum tube biquinary counter was laboratory tested using a similar concept for comparison of the digital display on Burroughs rotary "Nixie" tubes (were they called decatrons?) against a thumbswitch data source. The system clock, unavailable at the comparator, was reconstructed—this time by sensing the state change of the binary section of the biquinary LSD stage in the Burroughs display counter. Logic so used for the latter clock reconstruction was comprised of a one-shot multivibrator (pulse transformer in the anode circuit) diodes, and cathode follower gating. That was in 1957 when Boolean algebra and exclusive ORs were still back at Harvard! Again, credit for the latter circuitry, in my judgement, probably should be assigned to R. W. Tripp and whichever Burroughs field engineer worked with us on that project.

The essense of my story, I suppose, is that very little is new under the sun—especially when relatively simple circuits are released as patentable objects. One must ask whether changing the material on the conventional mousetrap is a patentable idea.

I have no grievance against Mssrs Harf of the Singer Co and Wheeler of NASA and it is to their credit that any worthwhile idea was propagated to the technical community through your journal. Just venturing into the realm of the patent office is a noble task these days and they undoubtably deserve the award for having the perspicuity to find their way through the morass.

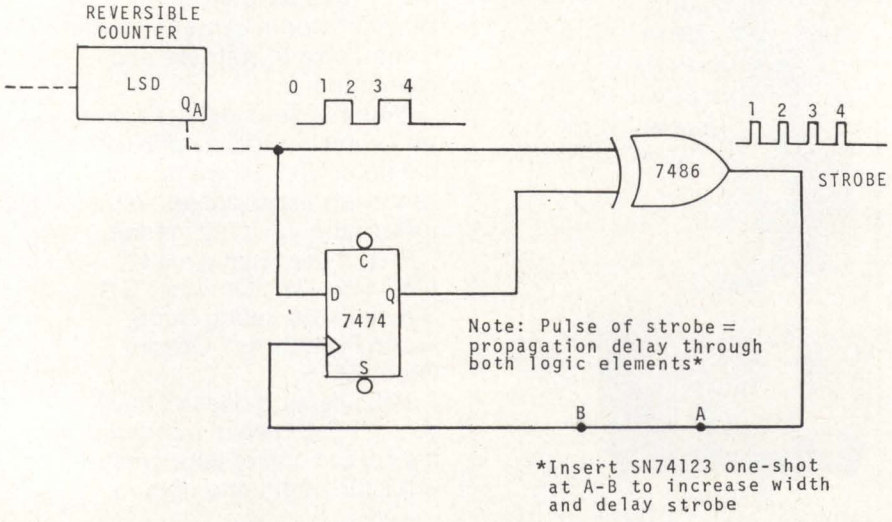
W. Thomas Hughes
W. T. Hughes & Co
Danbury, Conn

To the Editor:

As an engineer involved in logic design, I am growing more than slightly tired of people reinventing the bedpan and claiming credit for it. Yet I have grown to more or less accept it as a fact of life. However, the Tech Brief entitled "Exclusive-OR Frequency Multiplier" (*Computer Design*, June 1978, p 130) was more than I could bear.

Surely anyone who has ever done any measurable amount of logic design is familiar with the use of the "exclusive-OR" function as a frequency doubler. Furthermore, the text of the article is misleading. True, any but the most exact multiple of a 180° phase shift will effectively double the number of input transitions, but one can only talk of frequency multiplication in a real sense if the output duty cycle is maintained. Most delay circuits will produce such results over very narrow ranges of frequencies. As for cascading such circuits, two approaches are possible, but only one is practical.

As the Tech Brief mentions, one can use delays of 180°/n and cascaded stages, but it should be noted that it is virtually impossible to maintain a constant value of phase shift over any range of frequencies, except for multiples of 90°, which limits the value of n to n = 2. This approach is therefore totally useless unless the input frequency hardly varies at all, in which case the techniques normally used in radio are best suited anyway.



(Continued on p 10)

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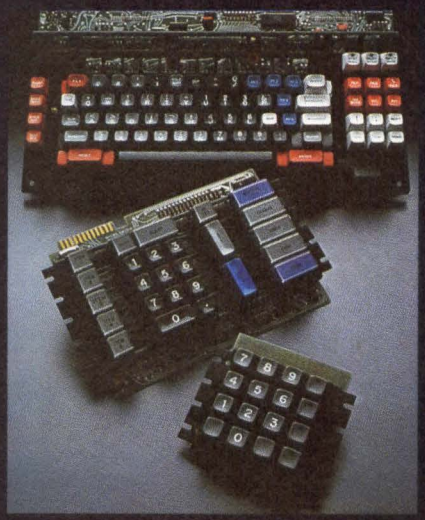

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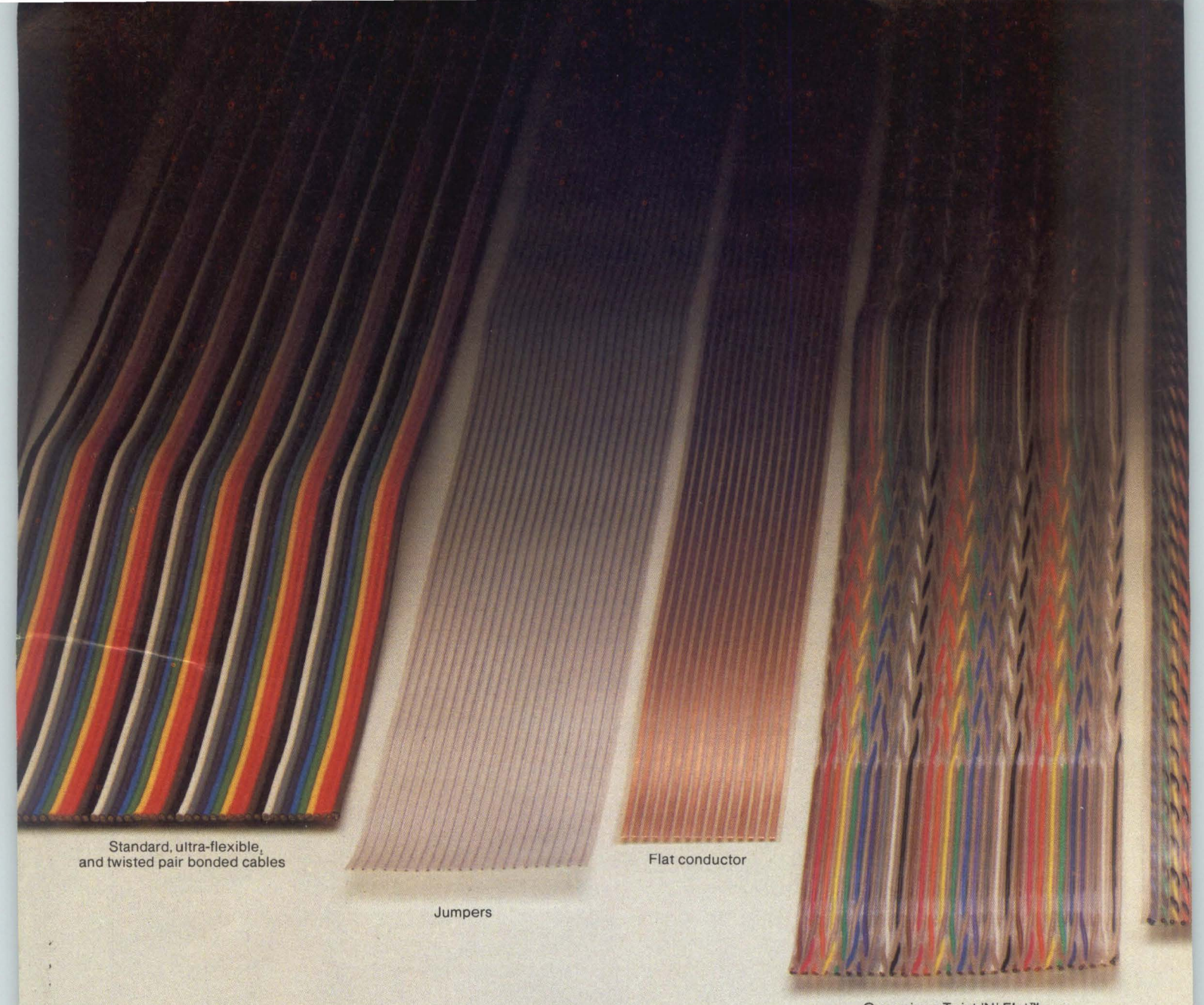

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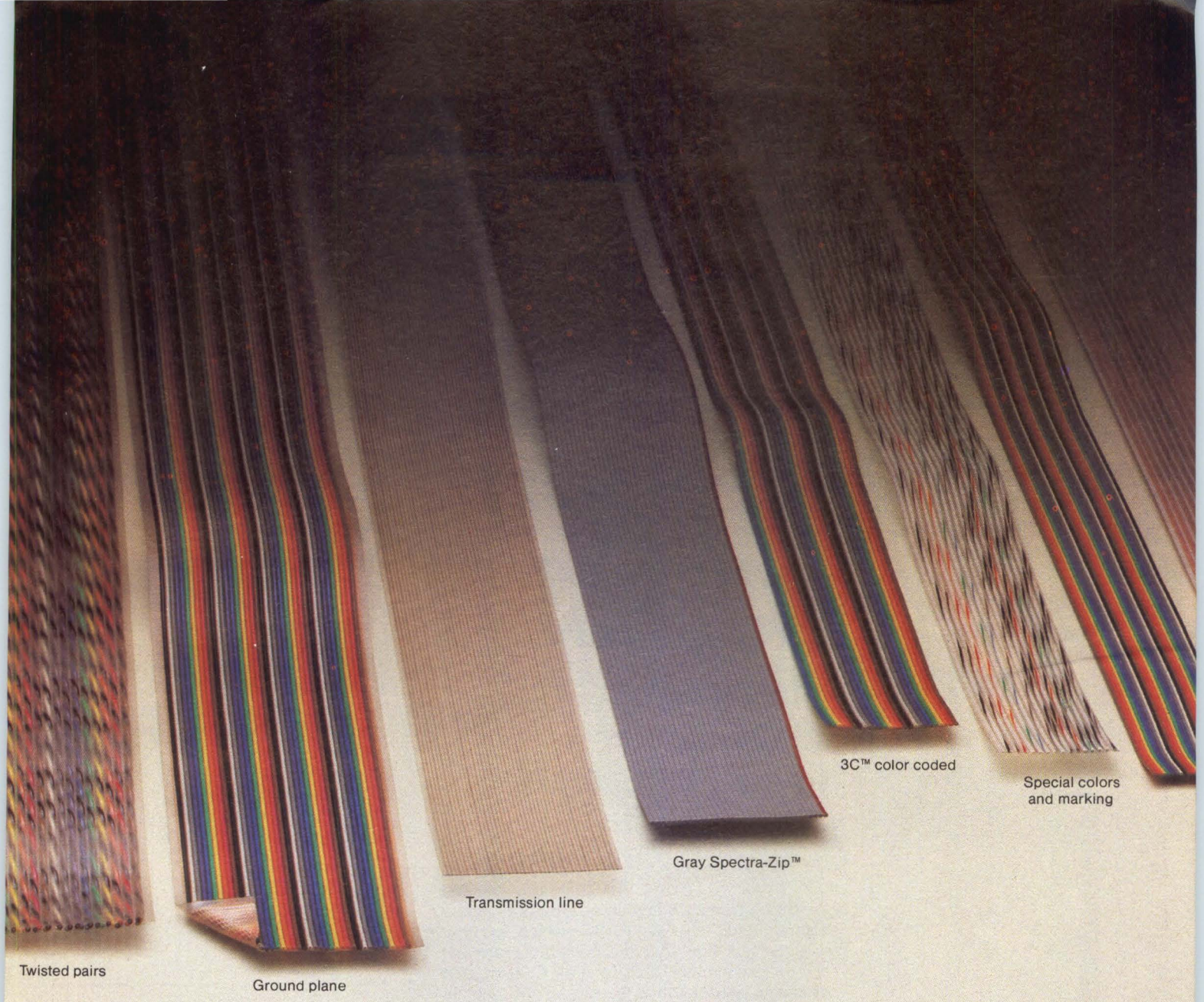

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CIRCLE 7 ON INQUIRY CARD

It is by no means the first time that I have seen such commonly known data presented as new, but it has been a while since I have seen anyone have the nerve to call such trivia an invention and claim title to it. I could not live with myself if I let this go unchallenged.

Georges-Emile April
Associate Professor—Electrical Engineering
Ecole Polytechnique
Montreal, Canada

To the Editor:

As a subscriber to *Computer Design*, let me first express my appreciation for the consistently high standard of the publication, both from a technical and literary point of view.

I was especially impressed by the comprehensive and detailed article "Current Semiconductor Memories" (*Computer Design*, Apr 1978, pp 115-126) by Eugene R. Hnatek. I feel, however, that I have detected certain ambiguities in the above article. For instance, on p 120 Mr Hnatek states: "At present, static RAMs outperform their dynamic counterparts in terms of speed . . . and power dissipation . . ." However, on p 125 the statement is made: "Dynamic memories operate at higher speeds and consume less power than static memories."

In order that the generally excellent informative quality of the above article not be impaired, I would greatly appreciate the author's comments regarding this and other apparent ambiguities.

Michael R. Webb
Honeywell GmbH
West Germany

The Author Replies:

Mr Michael Webb's letter does point up an ambiguity regarding a comparison of static and dynamic MOS random access memories as contained on pp 120 and 125 of the April issue of *Computer Design*. The information on p 120 is correct and that on p 125 in error. Specifically, static MOS RAMs exhibit lower t_{AA} and lower power dissipation than do their denser dynamic counterparts.

I apologize for this ambiguity. However, I don't find any "other apparent ambiguities" as so stated.

Eugene R. Hnatek
Monolithic Memories, Inc
Sunnyvale, Calif

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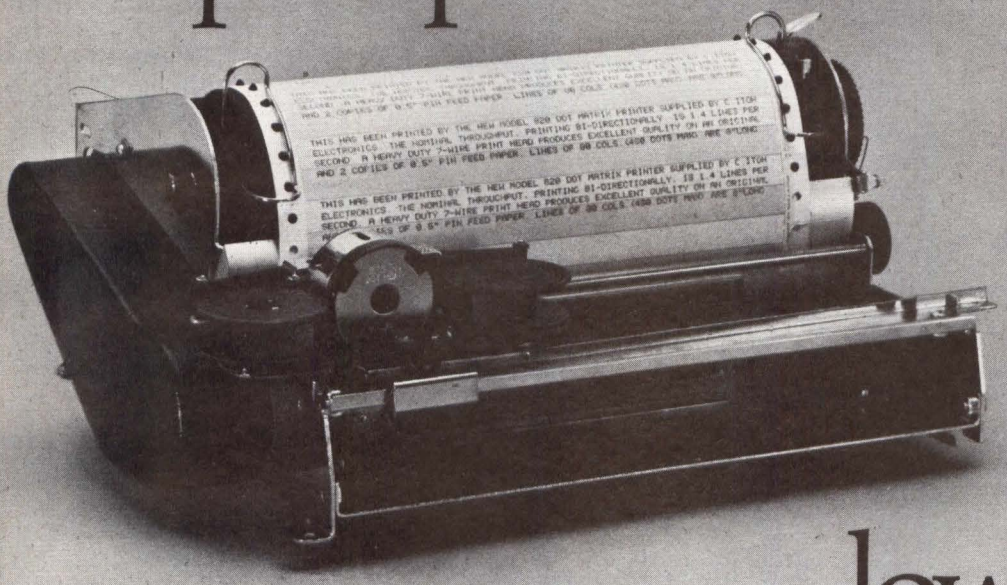
CORRECTION

In the July issue, p 184, the company identification for the product entitled "Rare Earth Field DC Motors" should be The Pittman Corp, PO Box 3, Harleysville, PA 19438.

Model 820, 150 cps, 80-column, dot matrix impact print mechanism...



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CALENDAR

Announcements intended for publication in this department of *Computer Design* must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

CONFERENCES

OCT 10-12—USA/Japan Computer Conf, Jack Tar Hotel, San Francisco, Calif. INFORMATION: AFIPS, Inc, 210 Summit Ave, Montvale, NJ 07645. Tel: (408) 245-5807

OCT 15-19—ISA/78 (Instrument Society of America Internat'l Instrumentation-Automation Conf and Exhibit), and JACC (Joint Automatic Control Conf); Philadelphia Civic Ctr, Philadelphia, Pa. INFORMATION: ISA/78, 400 Stanwix St, Pittsburgh, PA 15222. Tel: (412) 281-3171

OCT 18-20—Canadian Conf on Communications and Power, Queen Elizabeth Hotel, Montreal, Canada. INFORMATION: Jean Jacques Archambault, Chm-Technical Program Committee CP/PO 757, Succ C, Montreal, Quebec H2L 4L6, Canada

OCT 25-26—Electronic Connector Sym, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101

OCT 25-27—Sym on Computer Arithmetic, Miramar Hotel, Santa Monica, Calif. INFORMATION: Prof Milos D. Ercegovac, Computer Science Dept, U of Calif, Los Angeles, CA 90024. Tel: (213) 825-2660

OCT 31-NOV 2—Cherry Hill '78 Test Conf, Cherry Hill, NJ. INFORMATION: Pat Regan, Secretary/Registrar, Test Conf Comm, PO Box 2340, Cherry Hill, NJ 08034. Tel: (609) 983-3100

NOV 1-3—Conf on Computer Graphics in CAD/CAM Systems, Massachusetts Institute of Technology, Cambridge, Mass. INFORMATION: Conf Chm, Prof David C. Gossard, Dept of Mechanical Engineering, MIT Rm 3-453, 77 Mass Ave, Cambridge, MA 02139

NOV 1-3—Internat'l Sym on Computers, Electronics, and Control (CEC '78), Toronto Hilton, Toronto, Ontario, Canada. INFORMATION: The Secretary, CEC '78, PO Box 3243, Sta B, Calgary, Alberta T2M 4L8, Canada

NOV 6-8—Asilomar Conf on Circuits, Systems, and Computers, Pacific Grove, Calif. INFORMATION: Donald E. Kirk, Electrical Engineering Dept, Naval Postgraduate School, Monterey, CA 93940

NOV 7-9—Federal Computer Conf and Expo, Sheraton-Park Hotel, Washington, DC. INFORMATION: Federal Computer Conf, PO Box 368, Wayland, MA 01778

NOV 7-9—Mini/Micro Conf and Expo, Astrohall, Houston, Tex. INFORMATION: Robert D. Rankin, Managing Dir, Mini/Micro Conf and Expo, 5528 E La Palma Ave, Suite 1, Anaheim, CA 92807

NOV 9—Invitational Computer Conf, Palo Alto, Calif. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: (714) 644-6037

NOV 13-16—Internat'l Conf on Computer Software and Applications (Compsac 78), The Palmer House, Chicago, Ill. INFORMATION: Wallace A. Depp, Executive Dir, Processor and Computer Software Systems Div, Bell Laboratories, Naperville, IL 60540. Tel: (312) 690-2111

NOV 14-16—Interface West, Los Angeles Conv Ctr, Los Angeles, Calif. INFORMATION: Interface West, 160 Speen St, Framingham, MA 01701. Tel: (617) 879-4502

NOV 14-17—Conf on Magnetism and Magnetic Materials, Stouffer's Inn on the Square, Cleveland, Ohio. INFORMATION: Dr Hugh C. Wolfe, American Institute of Physics, 335 E 45th St, New York, NY 10017

NOV 27-29—European Communities Sym on Computer Aided Design of Digital Electronic Circuits and Systems, Hotel Hilton, Brussels, Belgium. INFORMATION: Keness Belgium Congress SA, Rue de L'Industrie 17, 1040 Brussels, Belgium

DEC 4-6—Conf of the Assoc for Computing Machinery, Sheraton-Park Hotel, Washington, DC. INFORMATION: Dr Richard Austing, Dept of Computer Science, U of Maryland, College Park, MD 20742. Tel: (301) 454-2004

DEC 4-6—Internat'l Electron Devices Meeting, Washington Hilton Hotel, Washington, DC. INFORMATION: Susan Henman, Courtesy Assoc, 1629 "K" St NW, Washington, DC 20006. Tel: (202) 296-8100

DEC 12-14—Midcon/78, Dallas Convention Ctr and Dallas Hyatt Regency, Dallas, Tex. INFORMATION: William C. Weber, Jr, General Manager, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: (213) 772-2965

DEC 13—Computer Networking Sym, Nat'l Bureau of Standards, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: (301) 439-7007

DEC 18-20—Internat'l Computer Sym (ICS), Academia Sinica, Nankang, Taipei, Republic of China. INFORMATION: K. S. Fu, School of Electrical Engineering, Purdue U, W Lafayette, IN 47907. Tel: (317) 494-8825

SEMINARS

OCT 16-18—Nat'l Communications Forum Program, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: National Engineering Consortium Registrar, 1211 W 22nd St, Oak Brook, IL 60521. Tel: (312) 325-5700

OCT 16-19—EMI Control in Design and Installation of Data Processing Equipment; and OCT 24-26—Digital Modulation, Coding, and Signal Processing Techniques, Boston, Mass; and Chicago, Ill. INFORMATION: Don White Consultants, Inc, 656 Quince Orchard Rd, Suite 410, Gaithersburg, MD 20760. Tel: (301) 840-0300

OCT 23-24—Fiber Optic Communications Marketing Seminar, Sheraton-Islander Hotel, Goat Island, Newport, RI. INFORMATION: Kessler Marketing Intelligence, 22 Farwell St, Newport, RI 02840. Tel: (401) 849-6771

SHORT COURSES

OCT 9-13—Microcomputer Workshop, Carnegie-Mellon U, Pittsburgh, Pa. INFORMATION: Post College Professional Education, Carnegie Institute of Technology, Carnegie-Mellon U, Schenley Pk, Pittsburgh, PA 15213. Tel: (412) 578-2207

OCT 11-13—Fiber Optics Systems Design; and Microprocessors; and OCT 30-NOV 3—Switched Networks for Data Communications, The George Washington U, Washington, DC. INFORMATION: Continuing Engineering Education Program, George Washington U, Washington, DC 20052. Tel: (202) 676-6106

OCT 17-18—Fiber Optics; Oct 18-19—2-Day Microprocessor; OCT 21—Introduction to Microprocessors; and OCT 26-28—3-Day Microprocessor, Boston, Mass; Denver, Colo; Milwaukee, Wis; and Tampa, Fla. INFORMATION: Vincent J. Giardina, IEEE Manager of Continuing Education, 445 Hoes Lane, Piscataway, NJ 08854. Tel: (201) 981-0060, X174/175

NOV 7-10—Microprocessors' Use in Power Electronic Systems, U of Missouri, Columbia, Mo. INFORMATION: Dr Hoft, Electrical Engineering, U of Missouri, Columbia, MO 65201. Tel: (314) 882-3491

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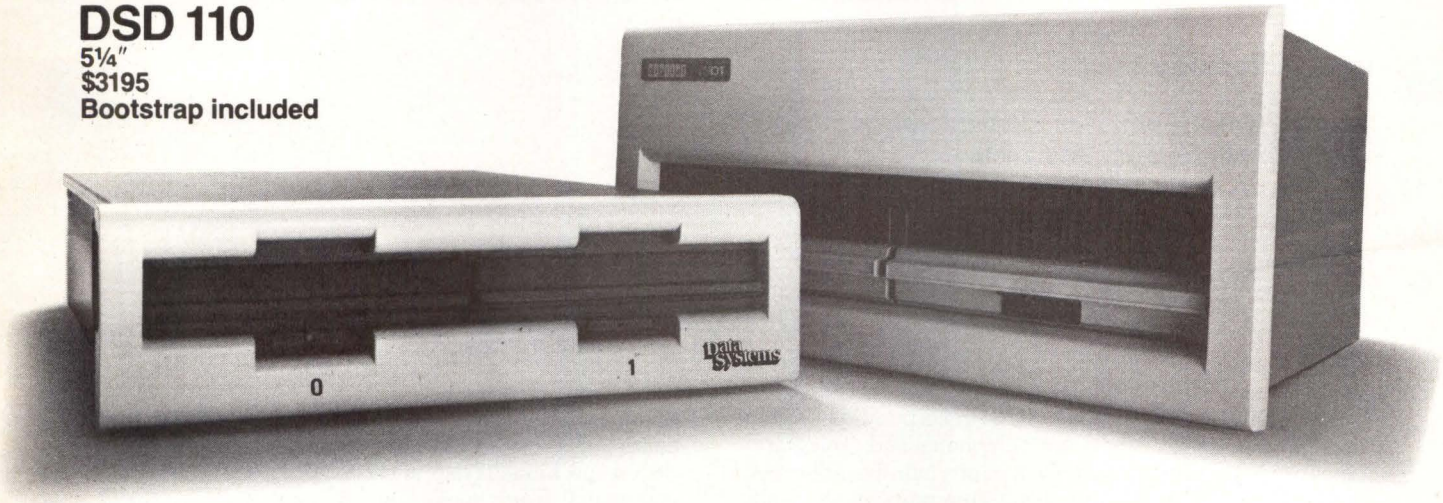

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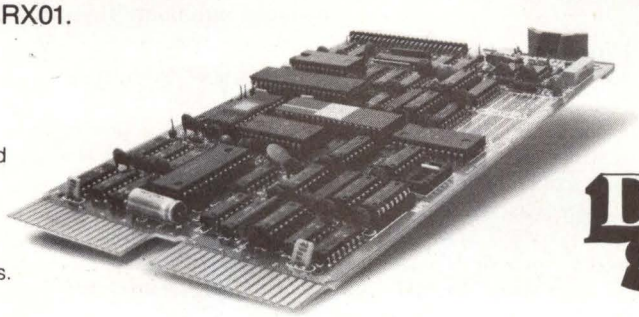

Data Systems has combined interface, formatter, controller, and hardware bootstrap on this single dual-wide card. Available separately in OEM quantities.

Data Systems

1956 CONSENT DECREE— HISTORY AND IMPLICATIONS

John E. Buckley

Telecommunications Management Corporation
Cornwells Heights, Pennsylvania

There is no doubt that the largest corporation in the United States is the American Telephone and Telegraph Company. This giant monopoly has profoundly influenced and directed the evolution of telecommunications technology through innovative developments, as well as by sheer size and presence. Through its 23 utility operating telephone companies (ie, the Bell System), AT&T has become identified with telecommunications services in the United States. AT&T has dominated and controlled this industry since the 1930s and has been justly credited with the host of inventions and patents embodied in today's telecommunications systems. It has been the prime cause of the enviable record of reliability and performance of this country's communications services.

While deserving these laurels for its many contributions, AT&T has also vigorously struggled to maintain its privileged monopoly position. Since the 1968 FCC Carterfone decision, AT&T has actively resisted inroads to its domain by competitive communications services and products. Only after the U.S. Supreme Court in Oct 1977 established the inherent legitimacy of interconnection has AT&T withdrawn its aggressive objections. One month prior to that Supreme Court action, AT&T had proposed a negotiated settlement to the interconnect dispute; the proposed settlement included a dismissal of the 1956 consent decree of AT&T.

During 1976, AT&T launched a major lobbying action to change the Communications Act of 1934 through the U.S. Congress, by means of legislation disarmingly entitled The Consumer Communications Reform Act. The FCC determined at that time that an estimated $100 million was scheduled to be expended by AT&T to support the legislation, a major provision of which was the elimnation of the 1956 consent decree.

Perhaps no other restriction is today as undesirable as that agreement executed by AT&T and the Justice Department over 22 years ago. It is viewed by AT&T as the major obstacle to its ability to capitalize on future telecommunications market requirements. The 1956 consent decree prohibits AT&T and its utility operating telephone companies from marketing services and equipment that are not directly associated with communications.

In 1949 the Justice Department filed an antitrust suit against AT&T. During the ensuing seven years these two organizations proceeded through various judicial arenas to an ultimate stalemate. The impasse was ended in 1956 when AT&T agreed to confine its business activities and those of its subsidiaries exclusively to the scope of the tariffed communications common carrier industry and of associated tariffed services and equipment.

This agreement was reaffirmed in 1970 at the conclusion of the first FCC Computer Communications Inquiry. That important inquiry attempted to differentiate between the environments of data communications and of data processing. During the 1960s the traditional line of demarcation between the regulated telecommunications, and the free-enterprise data processing territories became significantly clouded. The conclusions issued in 1970 allowed utility communications common carriers to offer non-regulated data processing services through totally separate subsidiaries that maintained both physical and financial autonomy from the associated regulated entities.

The Western Union Telegraph Co was one of the first organizations to restructure in order to offer both regulated and non-regulated services. Western Union Corp was formed as a holding company, with the utility telegraph company and the data processing entity functioning as separate subsidiaries. A specific exclusion of this 1970 FCC action was that only AT&T was expressly prohibited from forming any type of non-regulated data processing subsidiary. The 1956 consent decree provisions were clearly reinforced in the published conclusions to the 1970 Computer Communications Inquiry.

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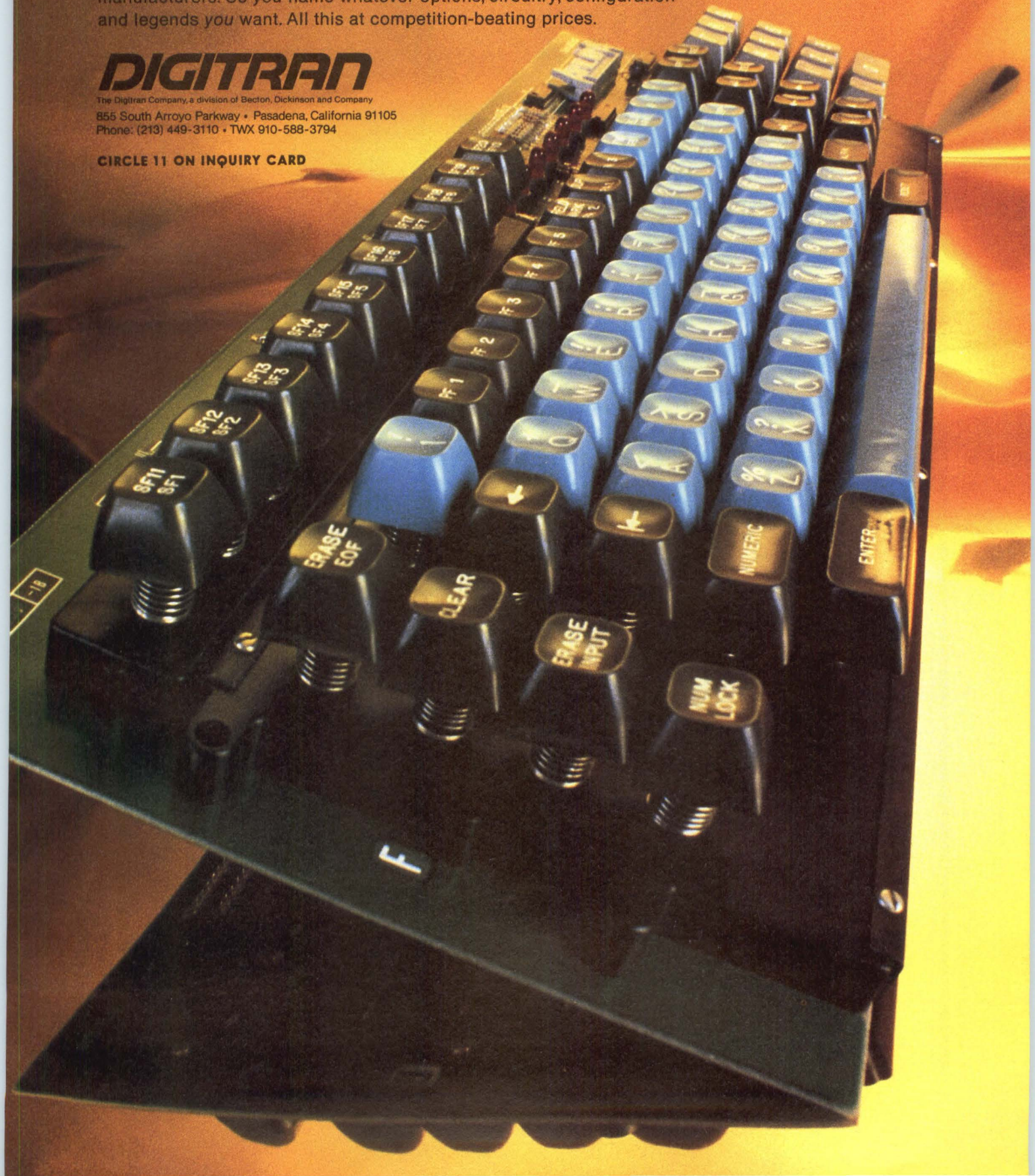
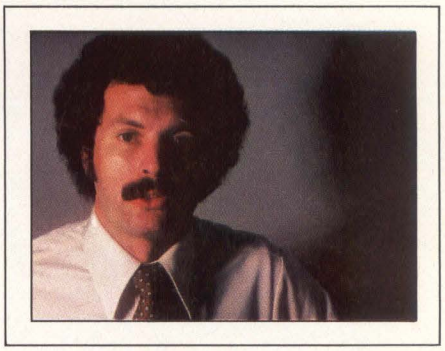


"Any bunch of hotshots can design a new microcomputer. It takes brains to improve an old one."

John Jones
Product Marketing Manager
Series/80 Microcomputer Systems



Series/80 Microcomputer Systems

"We're super aware that forcing a change in system architecture causes customers a lot of pain and agony. It costs a small fortune. And no amount of cross assemblers, translators or mode switches will make things easier.

If you want to hear real horror stories, ask the minicomputer guys. They've seen it.

It just doesn't make sense to me to force customers into a change when there are tons of things you can do to improve any system — especially once it's been in use. And with Series/80 that's exactly what we do.

80/204, 80/10
— the advantages of hindsight.

We've just begun offering the 80/204 board. And you can bet we've added some improvements.

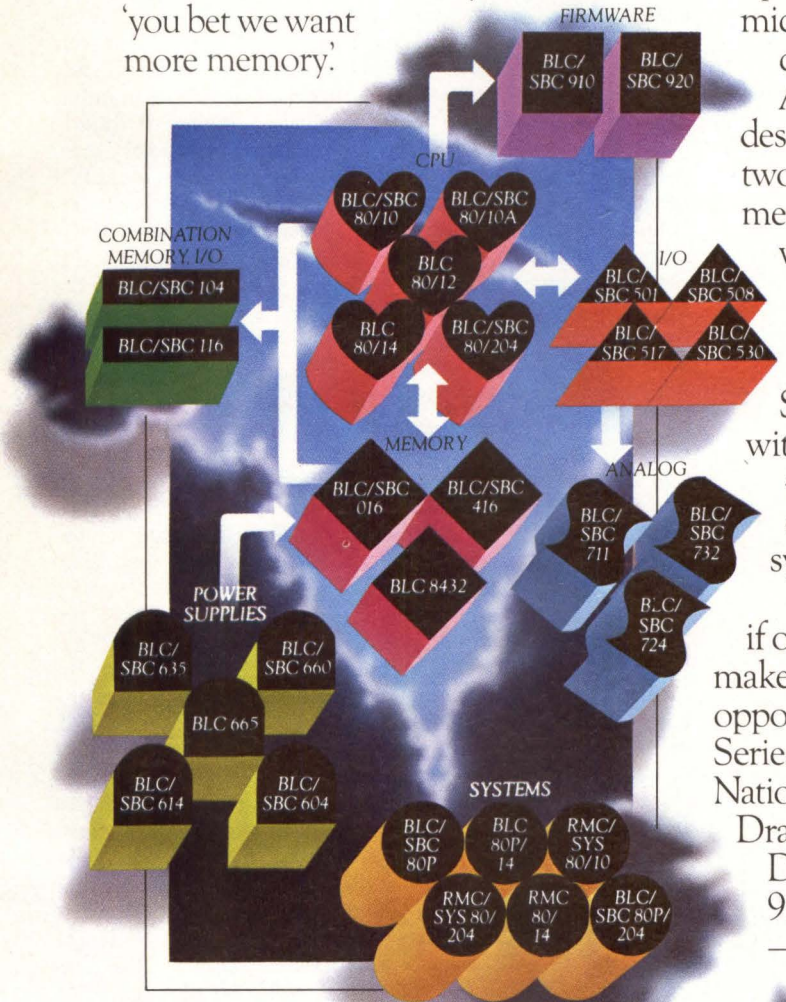
Like 'shadow ROM.' It lets ROM share the same memory address as RAM. And the ROM can be completely shut down and shut out when you don't need it.

In standby, our BLC 80/204 draws less than a watt versus 4 watts for Intel's SBC 80/204. And our bus master handles 6 masters on system bus compared to 3.

In addition to board level products, we offer a complete line of 80/204 and 80/10 rack mounted computer (RMC) systems with significant advantages over what has gone before.

Don't get me wrong. The SBC 80/204 – in fact, all the original SBC products are very good. But coming later lets us take customer reaction into account.

In 80/10 boards, for instance, we felt people might like the on-board memory beefed up. So we got out and talked to customers. They told us, 'you bet we want more memory.'



And that's what we gave them with the BLC 80/11, 80/12 and 80/14.

Customer feedback also led to the development of National's exclusive 32K BLC8432 ROM/PROM memory card, which is twice the capability of everybody else's.

It's a plain fact that National will continue to be customer driven instead of product driven. We'll come across with features customers want and need instead of what might be clever.

A New Industry Standard.

I feel the best hardware investment is one that protects a software investment. And with Series/80, we're helping create an industry standard microcomputer. So more customers can use an existing software base. And software and hardware designers will be easier to find. Also, two vendors competing for business means freedom of choice. And that's what free enterprise is all about.

Serious about Series/80.

We're dead serious about Series/80. Just last year we started with seven products. Now we're at 41 and still counting – every one designed from a top-down systems point of view.

For more on Series/80 – or, if our market-driven philosophy makes sense and you'd like to talk job opportunities, write me: John Jones, Series/80 Product Marketing, National Semiconductor Corporation, Drawer 6, 2900 Semiconductor Drive, Santa Clara, California 95051. Or call 800-538-1866 – 800-672-1811 in California."

Computer Products Group
National Semiconductor Corporation

It is illustrative of the rate of technological development in the field of telecommunications that a second Computer Communication Inquiry was instituted by the FCC in 1976. This action was prompted by the realization that definitions and decisions of the 1970 findings were rapidly becoming obsolete. Preliminary FCC action on the investigations of Computer Inquiry II were scheduled to commence July 13, 1978.

During June 1978 a new legislative replacement to the Communications Act of 1934 was part of the agenda of the House Subcommittee on Communications. A major item in this preliminary legislation was the release of AT&T from its 1956 consent decree. Obviously, in 1956, the posture of AT&T did not indicate that agreement to the provisions of the consent decree would create any major handicap to its business plans. In 1978, however, this consent decree is viewed by the company as a major obstacle to future business influence and growth. In its every action in the legislative or judicial environment, AT&T has indicated a continuing willingness to compromise its position in return for a release from its 1956 consent decree.

It is clear that products and services in the telecommunications market are becoming intimately entwined with data processing applications and will continue to go in this direction. Prohibition from actively participating in this total market, in the opinion of AT&T, will cause major stagnation of its future growth and influence in American industry.

In a recent action, the Computer and Communications Industry Association (CCIA) filed a complaint with the Justice Department that AT&T had violated the 1956 consent decree by marketing non-communications computer software packages through Western Electric. These packages consisted of non-communications programs intended for monitoring overall operation of a computer system, text editing, and typesetting, as well as for specific engineering and scientific applications. It was stated in the complaint that one of these program packages was marketed to about 600 licensees at $25,000 per license.

The CCIA complaint also challenged the 1976 opinion of Justice Department's Antitrust Div that the Model 40 OEM terminal being marketed by Teletype Corp, a subsidiary of Western Electric, did not violate the 1956 consent decree. That opinion was based on the premise that since this product was sold to Bell operating companies for communications applications, it constituted a communications product rather than a data processing product. It would appear then that the sole criterion for communication categorization is that a product or service must be sold by Western Electric to an operating telephone company for an alleged communication application; then it is a communications product or service. Since all parties to such a transaction are controlled by AT&T, virtually any product or service could be structured to meet this definition as a "communications product or service."

The future struggles of AT&T with its regulatory and legislative constraints will typically be based on the elimination of the 1956 consent decree. While it is not expected that a direct confrontation to remove this business limitation will be initiated by AT&T, the removal or deemphasis of the 1956 consent decree will be an integral part of all its future petitions and negotiations with regulatory, legislative, and judicial bodies.

AT&T recognizes that the major demands of its marketplace in future years will involve information and not merely communications. The advent of computerized telephone systems with their electronic telephone sets—actually microcomputer controlled data terminals—is merely one of the more obvious evolutions of this information through communications aspect of the future market. The home computer market is only beginning to emerge as a viable business objective. The public telephone network, controlled by digital computer systems (ESS Central Offices), already exists. With removal of the 1956 consent decree, these computer systems could easily be structured to provide computation services to every home in the country. On an equally lucrative scale, the computerized Dimension telephone system, marketed by the Bell System, could be structured to satisfy many business functions heretofore performed by separate data processing computers.

These potential applications are merely short term situations that could be quickly exploited by AT&T with a resulting realization of highly profitable revenues. The concept of the "computer utility", widely discussed in the early 1960s, is now clearly on the verge of reality, except for the 1956 consent decree.

A presently unchallenged practice of some Bell System operating telephone companies is the marketing of a minicomputer system that records all the calls generated from a Bell system-provided PBX, (Private Branch Exchange.) This application is recognized as not being in violation of the 1956 consent decree. The fact that this Bell System-provided minicomputer also includes software to produce management reports from the communications calling source data, however, makes it highly questionable. The concern of violation becomes even more profound when it is realized that this utility supplied minicomputer allows the customer to enter internal accounting codes for the purpose of direct calling activity cost allocation. The non-communications aspect of this service becomes more visible when it is realized that the processing programs also allow the customer to assign overhead or operating costs allocations to various calls and/or departments.

Elimination of the 1956 consent decree may be viewed by some as a positive conclusion to the present dilemma. It must also be recognized, however, that the rapid evolution of the data processing industry in the U.S. has been due to the participation of highly competitive forces. The history of the telephone industry, which has been unconcerned with any such competitive factors, has been characterized by a general laxity in new product and service concepts unless stimulated by outside competitive inroads. Admittedly, advancement of new technology has occurred within the telephone system, but only to the extent that it has reduced telephone system operating costs. Such examples have been automatic dialing and, more recently, the automated maintenance capabilities of electronic switching systems. Advancements in user features and applications not having direct operating cost reduction implications, however, have been notably few. The concern of many participants in the computer communications environment is that a total release from the 1956 consent decree will allow AT&T to quickly dominate the entire communication information market with the total exclusion of today's competitive factors. The final step of this action will be a total dictation of application characteristics by AT&T prompted only by its profit objectives. Many expect the consequence will be an eventual stagnation in these emerging application areas.

It is recognized that this view is not universally held by all interested parties. It would also be presumptuous to attempt to exhaustively review this matter in the necessarily condensed environment of this column and to claim that all aspects have been completely analyzed and presented. It is vitally important, however, that present and future participants in this information revolution be knowledgeable about the historical framework of this matter and be aware of the potential impact of that 22 year old agreement on tomorrow's requirements.

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Upgraded Domestic Funds Transfer System Commences Operations

Said to be the banking industry's newest and most advanced electronic funds transfer (EFT) System, BankWire II has been publicly demonstrated in New York City. Each day the system processes more than 18,000 messages, valued in excess of $20 billion, for its 185 member banks. BankWire I, the new system's predecessor, originated in the 1950s as a private wire telegraphic network for money transfer messages, and was expanded in the 1960s to use computers, probably the first EFT system operated primarily to service banks and their customers. BankWire II, three years in development, can accommodate three times today's payments message volume at speeds up to 30 times faster than BankWire I, which it has replaced.

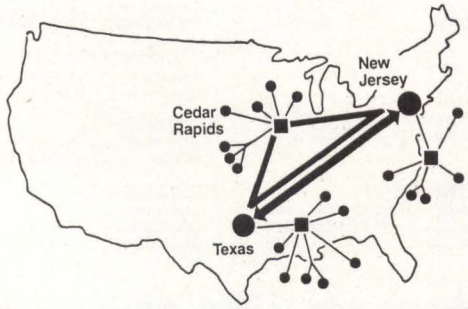
Key to the capacity and power of the system is extensive use of computer technology to control, store, and keep track of funds transfer messages as they are transmitted over a network of private lines throughout the U.S. Three types of messages are supported: funds transfer, miscellaneous reimbursement, and administrative. Average message delivery time is less than two minutes after entry into the system. Suppliers of major equipment and service components for BankWire II are Rockwell International, Western Union Data Services Co, and Incoterm Corp, a division of Honeywell, Incorporated.

Two computerized message switching centers, one in Jersey City, NJ, which is operational now, and the other in Dallas, Tex, to be operational in Dec 1978, have been furnished by the Collins Communications Switching Systems Div of Rockwell International. Both centers use two C8562 processors, connected in a redundant configuration, and six disc file units for duplicate storage of total traffic from both locations. Programmable channel termination groups (PCTGS) are used as remote concentrators, each in a redundant configuration with alternate paths to the switching centers. PCTGS handle user terminals with operating speeds ranging from low speed teletypewriter units to higher speed devices at 2400 baud. Intercity trunking is at rates to 4800 baud. The two switching centers are directly connected via 9600-baud data links.

Western Union Data Services (WUDS) has supplied subscribers to the new system with nearly 200 BankNet/1 and BankNet/2 terminal stations, with microprocessor-based terminal controllers programmed for the Bell System 8BI protocol. Controllers, with 4k memory and SMS-300 microprocessors which execute instructions in 300 ns, control a variety of 10- and 30-char/s terminals, as well as transmission and reception of traffic with the Collins 8562 computer system. The 8BI protocol allows the computer to poll all terminals either selectively or sequentially. Each terminal station arrangement provides a hardware address for both selection and polling, responds to a poll call after receiving a message to indicate correct receipt, and can operate either alone or in a multidrop circuit configuration. WUDS also provides maintenance to the system through its Termicare system, a centralized customer-support service.

BankNet/3 and BankNet/4 terminals are keyboard CRTs with associated printers for output and message logging and are supplied by Incoterm Corp. The SPD 20/20 is used in cluster, and the SPD 10/20 in standalone configurations. These intelligent terminals allow banks to store funds transfer, reimbursement, and administrative message formats locally, and recall them immediately when a message must be sent. SPD 20/20 offers up to 32k bytes program memory and supports up to 16 operator stations and a full line of peripherals. SPD 10/20 includes a 4k program and screen refresh memory. Of the 248 terminals in the BankWire II system, 38 are video display units.

BankWire II is the outgrowth of a planning study completed in 1972 by the Monetary and Payments System committee of the American Bankers Association. Membership in the BankWire is voluntary. The organization operates as a not-for-profit cooperative in which representation, management, and costs are shared proportionately by all members.



High speed communication lines connect centers with data concentrators situated in New Jersey, Iowa, and Texas. Attached to concentrators are 48 lines; each can support a number of terminals located at member banks. 248 terminals are located at 186 banks, member-users of BankWire

Low and Medium Capacity Message/Data Switching Systems

DSX 60 systems are intended for industrial, commercial and government applications requiring automation of smaller networks of from 16 to about 200 lines. They are based on the P857 minicomputer, and are available in both single- and dual-processor configurations. Specific system structure depends on traffic load, functional demands, and required level of system availability. Hardware and software modularity permits smooth expansion of system as requirements dictate.

Available from Philips Telecommunicatie Industrie BV, PO Box 32, Hilversum 1301, the Netherlands, the systems provide completely automatic handling of telegraph, data, telex, and text traffic on dedicated or switched circuits, in either store-and-forward or core-cut-through modes. Line speeds from 50 baud to 100k baud can be accommodated by a comprehensive range of synchronous and asynchronous communications control units. System configurations can support virtually any protocol governing host-processor or terminal interface, and can serve multiple independent

user groups with full protection against unauthorized access to data.

The systems are supplied as complete integrated hardware/software facilities. An equipment/operating system package, optimized for the particular application, and standard application software modules are included. Turnkey services provided with the systems include consultation on network configuration and optimization, specialized application analysis and software development, plus complete field support.

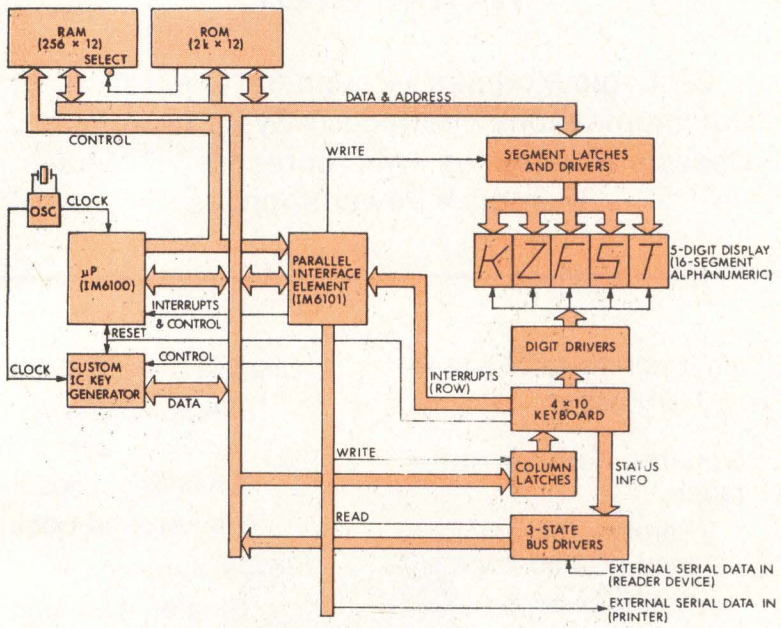
Circle 400 on Inquiry Card

Handheld Cryptographic Device Enabled by Custom LSI Chip

A cryptographic device the size of a pocket calculator provides such communications security that even the largest computer would take years to break the code. That is the performance claimed for the DH-26 message encoder/decoder, produced by Datotek, a Dallas firm specializing in communications security products. Key elements in the design are a microprocessor, and a custom large-scale integrated microcircuit. American Microsystems, Inc, 3800 Homestead Rd, Santa Clara, CA 95051 makes the 0.196 x 0.203" (4.9 x 5.2 mm) chip, which incorporates the electronic components of three PC cards, and makes possible portability, the essence of this particular product. The unit consists of a 26-letter, 10-numeral keyboard for data entry, eight control buttons, three slide switches, and a 5-character, 16-segment alphanumeric LED display.

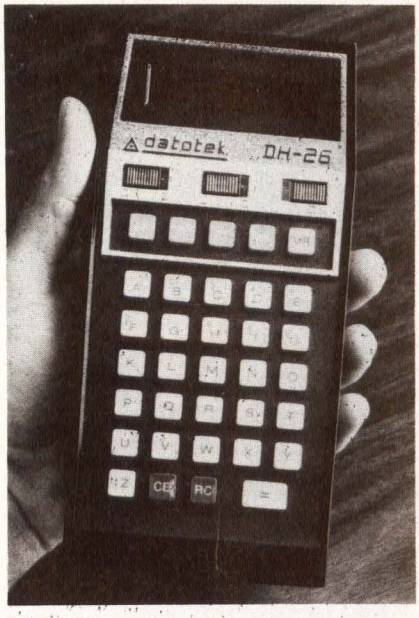
In operation, a sequence of 45 characters is entered in five groups of nine characters each. This action establishes the master code or initial state for the pseudorandom key generator—the LSI chip—and controls the generation of a binary bit stream 10^{65} bits in length. Operation of a *message* key establishes the starting point on the bit stream. The user then enters message to be sent, character by character; after each group of five characters is entered and displayed by the LEDs, the *equals* key is pushed, causing these characters to be replaced by five new ones—the coded version.

(Continued on p 22)



Simplified block diagram of Datotek portable encoder/decoder. Custom CMOS key generator in encryption unit acts as pseudorandom number generator with 10^{65}-bit long sequence. Microprocessor mixes plain text inputs with random sequence to create ciphertext displayed by LEDs

When the completed coded message is copied it may be read over the telephone, or sent by telegram, facsimile, or any other method. The receiver, who by prearrangement must use the same 45-character initialization code as used by the sender, may then decode the characters.



DH-26 encryption unit. Microprocessor-based, custom IC chip construction enables complex functions in calculator-size case weighing less than one pound

The LSI chip performs the mathematics of enciphering and deciphering. It is signal-compatible with the microprocessor and operates at 1 MHz, producing the 10^{65} bits pseudorandom key stream when commanded by the microprocessor, an Intersil 12-bit IM 6100. The chip receives the block of five input characters and serially produces the output bits that go to the microprocessor.

The microprocessor, which controls the device, initially scans the keyboard for depressed buttons. It then mixes the keyboard inputs with outputs from the chip, and uses a software algorithm to produce the alphabetic ciphertext for display. It also scans for key-generator failures, and provides a test function to validate key variables as well as proper operation.

A CMOS RAM, with battery backup to prevent loss of the 45-digit master code, combines with the message text, and ensures a unique code for each message. 10^{52} possible codes can be selected. The system is powered by a 5-V rechargeable battery pack and draws 50 mA.

Circle 401 on Inquiry Card

Turnkey Packet Switched Systems For Private Networks

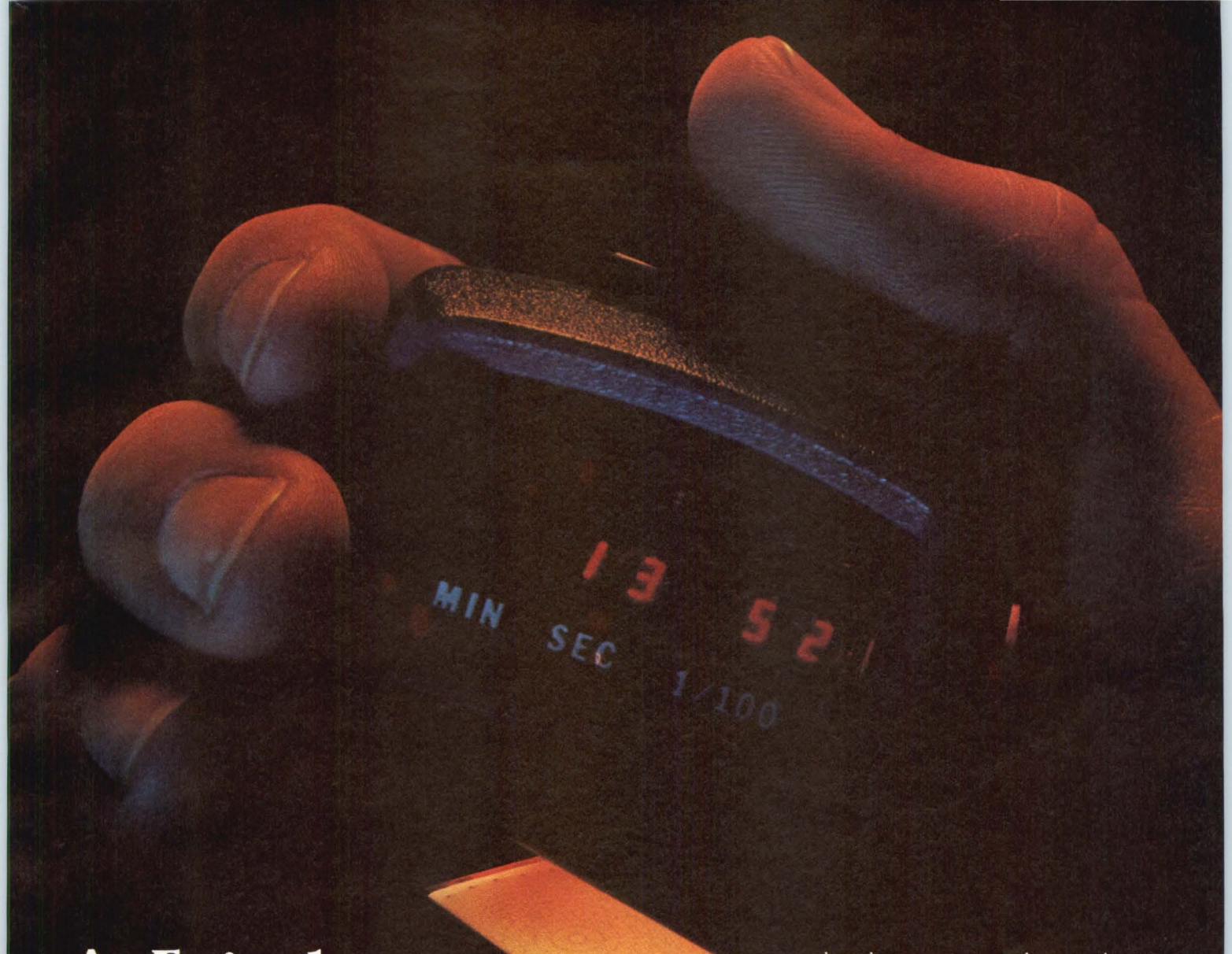
Plans to furnish packet-switched data communications systems for private networks have been announced by Telenet Communications Corp, 8330 Old Courthouse Rd, Vienna, VA 22180. The networks are compatible with virtually all computer equipment currently in use, and employ a line of microprocessor equipment and software developed by the company for its own nationwide common carrier network. Systems are designed to serve as a common corporate network utility for all user locations and data processing applications.

The turnkey networks support CCITT X.25, the accepted worldwide standard protocol for packet networks, and can be linked to X.25-based public networks in the U.S. and other networks around the world. Later in the year additional synchronous network interface protocols will be available.

Cornerstone of the private network offering is the TP 4000, a unit that functions as a packet switching network node as well as a network access concentrator for data terminals and computer systems. It provides a plug-in network interface and requires no changes to the user's existing data equipment or software.

The network offering will also include a minicomputer-based network control center (NCC), but users have the option of relying on the company's own NCC staff and facilities. The NCC's capabilities include: downline loading of software; centrally controlled remote diagnostics; continuous monitoring of operational status; and collection of statistical and accounting data.

Installation of the first private network node using the TP 4000 and a dedicated NCC is scheduled for the British Post Office (BPO) in London. The system will be used to expand the range of data communications services offered by the BPO between the U.K. and the U.S. Pilot network systems for two major U.S. corporations will be installed during the third and fourth quarters of 1978. □



An E-sized drawing in 13.5 seconds.

Gould's 5400 printer/plotter will produce an E-sized drawing in 13.5 seconds. That's faster than any competing electrostatic printer/plotter. With a paper width of 36" and a speed of 3.25"/second, the 5400 generates over 48 square feet of hardcopy per minute.

Designed for applications where fast turn-around and high throughput rates are important, the 5400 is ideal for computer-aided-design, seismic data plotting, and business graphic applications such as PERT/CPM, Gantt, and others.

Gould's patented negative-pressure, closed loop toning system ensures high contrast dry hardcopy even at the maximum plotting speed of the 5400. Print resolution is 100 dots per inch, horizontal and vertical. In addition, a staggered image head produces overlapping dots for high contrast images. A user-oriented control panel features a unique LED system for continuously monitoring paper supply.

For additional information on Gould 5400 printer/plotter capabilities, software, interfaces and special application packages contact your Gould representative. Or write Gould Inc., Instruments Division, 3631 Perkins Avenue, Cleveland, Ohio 44114 (216) 361-3315. For brochure call toll free: (800) 325-6400, ext 77. In Missouri: (800) 324-6600.

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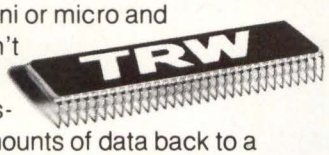
Use our new TDC 1010J multiplier/accumulator (MAC) to build a high-speed digital signal processor. With it you can analyze radar signals or X-ray data; communicate with satellites or computers; synthesize complex waveforms—even music.

A small FFT processor based on TRW's new MAC operates as a spectrum analyzer too—add one to your mini or micro and you don't have to lug massive amounts of data back to a number-crunching mainframe for reduction; you can reduce it right there on site and in real time!



It can analyze voices, earthquakes, geological soundings and submarine signatures. It can recognize a sticky valve in an automobile engine or in a human heart.

There was a time when the phrase "FFT processor" conjured up the image of an entire bay of sophisticated electronic hardware, but that's all changed now.

Starting with just a single TDC 1010J, you can design your own FFT processor on a small pc card. It will operate on just a few Watts and the CPU's microcode need never even touch the data.

Simply strobe any pair of 16-bit numbers into the MAC's on-chip input registers and zip—the chip delivers the correct 32-bit product for you in a mere 115 nsec.

An on-chip, 35-bit wide accumulator lets you choose to sum a series of products with no time penalty; that's both a double-precision multiply and a 35-bit add in the same 115 nsec!

Flexibility is a key feature of the TDC 1010J—it works on numbers as either two's complement or unsigned magnitude; the 35-bit accumulator can be directly pre-loaded, and you can round off the accumulated products to single precision.

Our new MAC is fully compatible with industry standards TTL. (It should be—after all, TRW invented TTL and patented it back in the early '60's, remember?) Of course, 3-state output buffers are provided.

TRW's TDC 1010J multiplier/accumulator is packaged in a 64 pin DIP. It consumes just 3½ Watts, uses a single +5V supply and is radiation hard. It is priced at only $205 in quantities of 100.

Like all TRW LSI Products, the TDC 1010J multiplier/accumulator is available now from stock through Hamilton Avnet. For more information, send in the coupon or talk to one of our digital signal processing experts at 213/535-1831.

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P. O. Box 1125
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Please send data sheets on the new **TDC 1010J,** 16 x 16 bit multiplier/accumulator.

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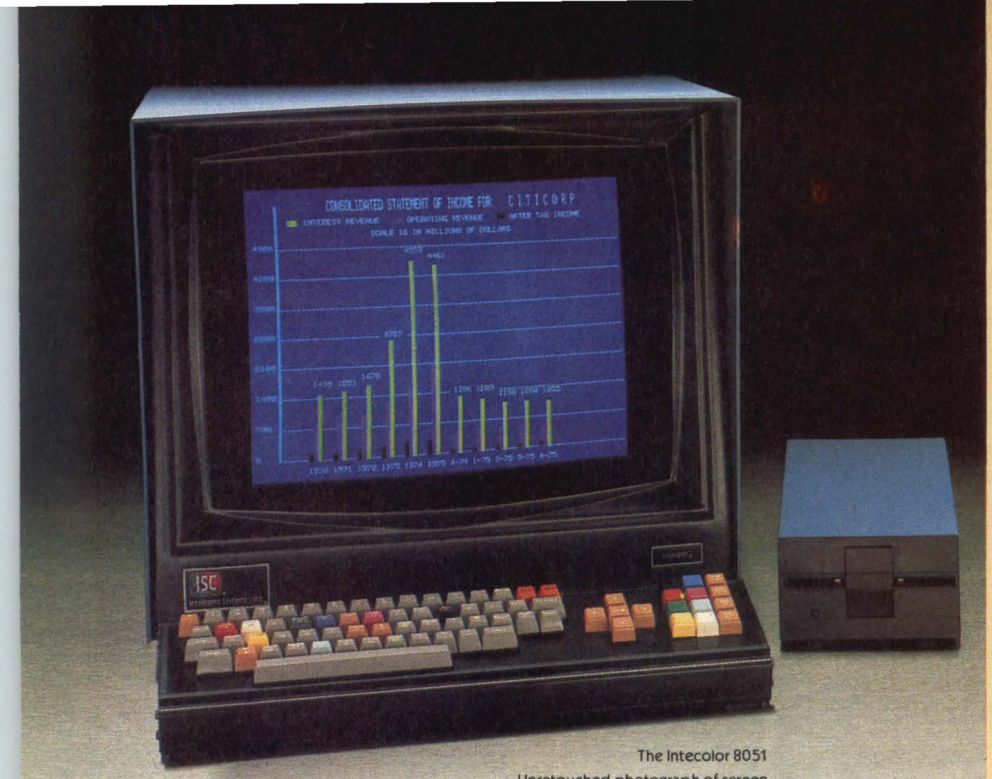
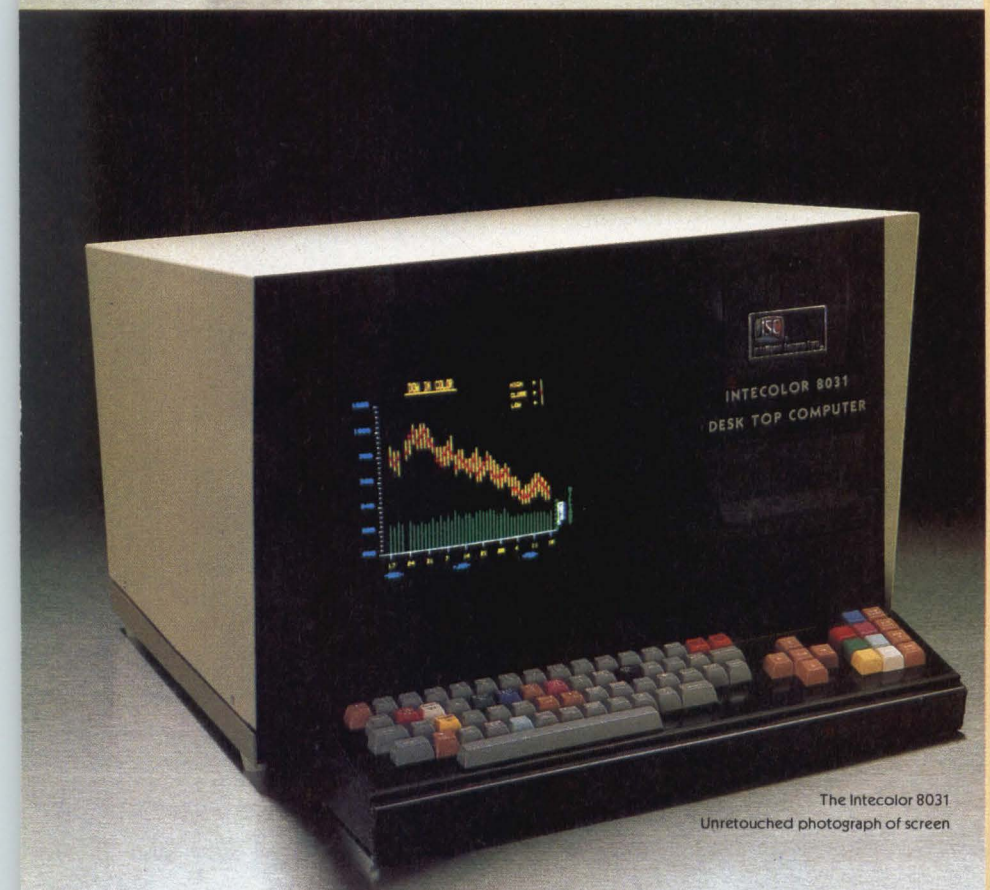
CIRCLE 15 ON INQUIRY CARD



The Intecolor 8051
Unretouched photograph of screen



The Intecolor 8031
Unretouched photograph of screen

$3,150*

Founded in 1973, we are the number one manufacturer of low-cost, 8-color data entry terminals, color graphics terminals for the process control industry and dependable color desk top computer systems.

You're looking at our two newest stand-alone desk top systems. Both were designed with the sophistication to handle a diverse range of business, control, research, and financial applications. In color. They both also have the best price/performance ratio of any compact computer system on the market.

If you're interested in a large screen format, the Intecolor 8051 is perfect. It comes complete with a big 19" diagonal screen, special graphics hardware and software, an external mini-disk drive for extra storage plus FILE handling BASIC, which lets you create, delete and retrieve program segments from storage, by name.

If your applications don't require a large screen format, the Intecolor 8031 is what you need. It comes with the same standard features as the 8051 but has a more compact cabinet, a smaller 13" display plus a built-in mini disk drive.

We also have a variety of options available for both units, so you can expand your system as your needs expand.

Call your Intecolor representative listed below for a demonstration of the Intecolor 8051, the Intecolor 8031, or both. *The $3,150 price is for orders of 100 units or more. The one unit price is $4,495, net 20 days. Less 5% prepaid. All Intecolor units are covered by a six-month warranty.

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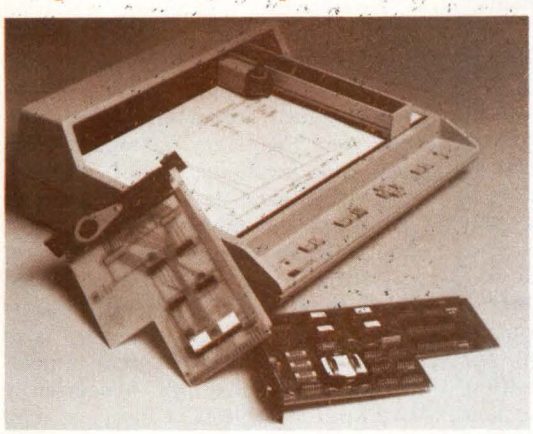
Plug-In Personality Modules Determine Plotter's Operating Capability



Plug-in personality modules for the 7225A graphics plotter gear capabilities to fit user requirements. Flexibility gained through use of modules makes this low cost plotter competitive with more costly models

A versatile interfacing capability characterizes a microprocessor based vector graphics plotter announced by the San Diego Div of Hewlett-Packard Co, 16399 W Bernardo Dr, San Diego, CA 92127. The low cost device owes its versatility to the use of circuit boards that are easily plugged into the plotter, providing it with a "personality" by determining its interface, language, and capability.

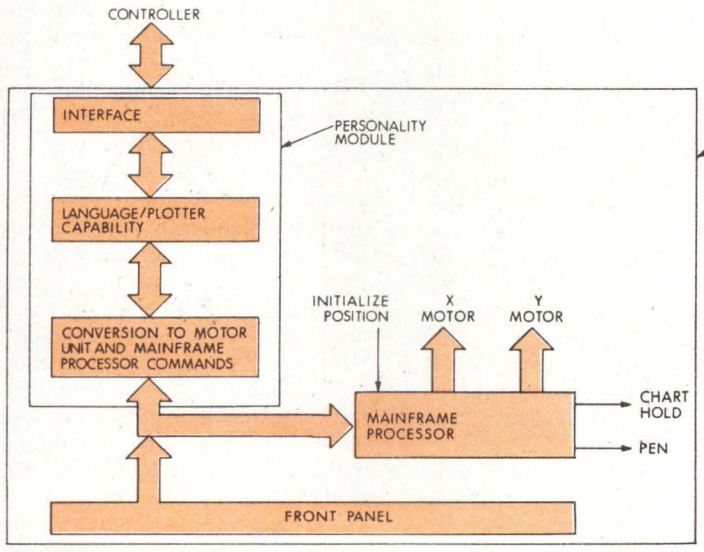
The 7225A plotter can be operated on command from front panel controls, even when no personality module is in place, or through a personality module. A 3870 single-chip microcomputer serves as the plotter's processor; it has direct control of both X and Y axis stepper motors and can step either motor in a positive or negative direction. Firmware in the plotter determines the relative stepping rate on the two axes, depending on the angle of the move. In addition, the processor controls the pen (up/down) and activates the electrostatic chart hold.

With a personality module in place, inputs are relayed to the plotter mainframe from an external computer, terminal, or other controller. ("Controller" is used to designate this external device, and is intended in a general sense, rather than designating a specialized drive-controller.) Based on information received from this controller, the personality module provides position/move commands and pen-maneuver commands to the plotter's processor.

In return, the plotter outputs status information to the personality module, including lower-left and upper-right scaling points, present position of the X and Y motors, pen state (up/down), and any digitized point entry performed by the operator. Position information passed between the plotter's processor and the personality module is in absolute motor units, where each motor unit is 0.032 mm. A lower left plotting surface limit of 0.0 serves as the reference, with positive X,Y coordinates designating rightward and upward motions along the two axes.

All that is needed for a position move and raising or lowering of the pen is that the personality module transmit X, Y coordinates with the corresponding pen maneuver to the plotter processor, which then executes the commands.

Initial members of the "17600 series" are the general purpose 17600A which uses a language consisting of binary coded data; the 17602A, an identical unit that has flexible word format involving 8-, 12-, or 16-bit capability; and the sophisticated 17601A which uses mnemonic graphics language. The 17600A's hardware interface to a controller consists of 19 parallel lines, including 2 bits of handshake, 7 bits of command, 8 bits of data, and 2 bits of status. Instructions are passed from the controller on command and data lines, with handshake lines synchronizing the data flow and status lines providing plotter conditions to the controller. Since it understands only a minimum set of



Hewlett-Packard's 7225A graphics plotter uses interchangeable personality modules to communicate with computer or terminal. Plotter's mainframe processor, which can be controlled from front panel or via the personality module, implements motor and pen maneuvers. Personality module transmits special instructions to mainframe processor, including character set selection, windowing, and preprogrammed graphics patterns

instructions—move commands and pen up/down commands—the 17600A requires the controller to provide high level graphic capabilities (such as character generation, windowing, and line type). Heavy traffic across I/O channel results, because the controller has to describe moves to the plotter in considerable detail. This requires that the user develop a sophisicated graphic software package.

The more sophisticated 17601A personality module interfaces to a controller via the Hewlett-Packard Interface Bus or HP-IB (IEEE 488). The language understood by this personality module is a mnemonic graphics language called HPGL. It provides 38 instructions for vector plotting, set and line type selection, point digitizing, user-unit scaling, and labeling, along with programmable size, slant, and direction of characters. In addition to the minimum instruction set (move, pen up/down), the 17601A module has a number of built-in graphic features. There are five resident character sets: standard ASCII, 9825 ASCII (mapping directly to the HP9825A keyboard), and three European sets—Spanish, Scandinavian, and French/German. Any one of these sets can be selected by command. Commands also control the sizing, direction, and slant of the characters. Other commands allow the user to select any one of seven dashed-line fonts, or to select an ASCII character for symbol-mode plotting. Still another set of commands allow one to define a plotting (window) area on the platen.

In general, the more sophisticated module allows the user to interface the plotter with a relatively simple controller or to a controller not extensively programmed with plotting routines. On the other hand, the less sophisticated module permits interfacing with sophisticated controllers with programs adapted to detailed plotting requirements.

All modules employ microprocessors. The processor in the simpler 17600A is a 3870 single-chip microcomputer, as in the plotter mainframe, whereas the 17601A module uses an F8 chip set.

Circle 170 on Inquiry Card

Parallel/Pipelined Computer Solves Scientific Problems at Low Cost

A microprogrammable computer system provides a powerful and low cost method of solving a large class of scientific problems involving both sophisticated and advanced mathematical techniques and many million words of data. The CHI system, developed by Culler-Harrison, Inc, 150-A Aero Camino, Goleta, CA 93107 and claimed to have speeds exceeding those of the CDC 7600 and to cost one-tenth as much, features parallel processing at several levels, a highly modular structure, and interactive online mathematical capability.

Basic system consists of six independent microprocessors and four fast discs. An array processor, the AP-120B (see *Computer Design*, Mar 1978, pp 93-100) performs high speed floating point arithmetic operations. The MP-32C macroprocessor provides control, I/O, bookkeeping calculations, and integer arithmetic operations; it also serves as host computer for the array processor, and supports an interactive mathematical system, text editor, file facilities, and appropriate assemblers and linkers.

The system's four I/O processors (IOPS) are fixed program microprocessors with direct memory access to both AP and MP main data memories. Each provides high level control over access to up to four Trident T300 or T80 disc drives.

Highly parallel structure of the system allows each processor to operate independently under control of the MP which functions as a host processor. Each processor performs a specific task, interrupts the host, and begins the next assigned task without requiring service of the host. I/O processors have a data bus into the main memory of the AP, separate to that used by the AP, eliminating many normally encountered bottlenecks.

The macroprocessor, with a 167-ns instruction time, is capable of executing 4 operations/instruction. In addition to the 64k-word central data memory which has 333-ns cycle time, there are a 512-word instruction ROM, a 64-word instruction RAM, and a 64-word scratchpad data memory.

Array processor is a 38-bit floating point arithmetic unit with maximum speed of 12M floating point operations/s. Main data memory contains 64k words, expandable to 1M words. There also is an instruction RAM containing 512 words (expandable to 4k), 2560-word fixed table memory, and two 32-word data pad memories.

Independent pipelined floating point multiplier and add units allow both a multiply and an add to be initiated every 167 ns. Two blocks of fast access accumulators are available for temporary storage of results from multiplier, adder, or memory. Addressing, indexing, and counting are performed by an independent integer arithmetic unit.

Grouping each 64-bit instruction word into program control, address control, arithmetic, memory, and I/O areas allows different operations to be performed concurrently within each cycle. For instance, data on all four discs can be simultaneously transferred to or from AP main memory or MP central memory.

Math system language, programmed in micro and macro language, is an interactive interpreter that can execute either interactively or from a program. It facilitates sophisticated mathematical operations on either real or complex vector data and graphics. AP microprogramming is necessary only to maximize efficiency of routines. Construction and testing of routines, and concatenation of microprograms is done in math system language.

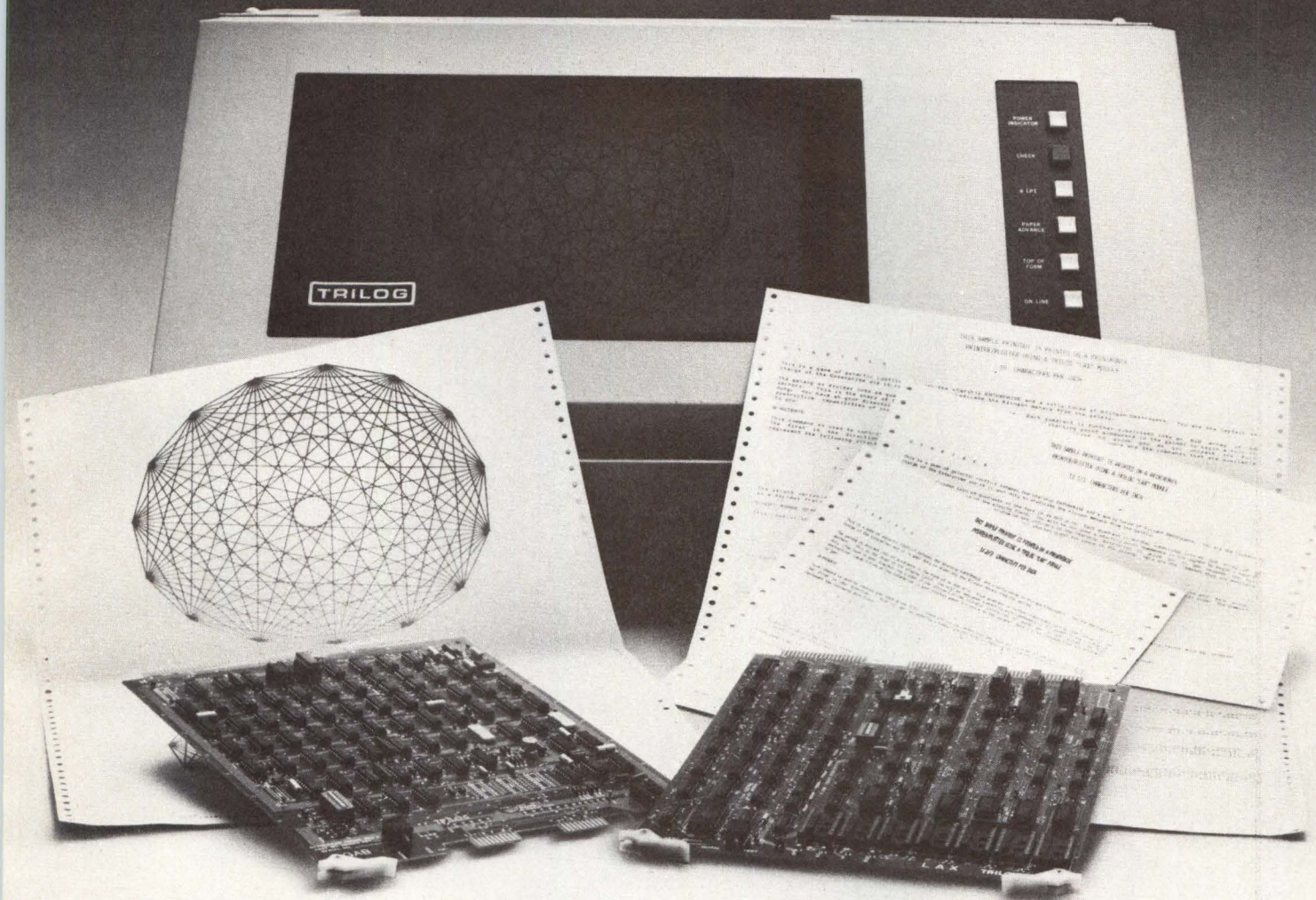
Circle 171 on Inquiry Card

Image Display System Offers Standalone Graphics Processing

RM-3000 series independent display systems are designed for standalone, offline processing in virtually any graphics or display application for users without elaborate computer systems. Based on the RM-9000 or -9050 display controller and the LSI-11 microprocessor, the system developed by Ramtek Corp, 585 N Mary Ave, Sunnyvale, CA 94086 can process display data from floppy disc, magnetic tape, or telecommunications lines, or direct from a host computer via modem control.

The completely programmable system features multiple resolutions starting from 256 elements by 256 lines up to 640 elements by 512 lines; multiple refresh rates and multiple planes of refresh memory are added features. It also provides interactive capability and multiple video options

Plug in more plotting and printing performance.



GAB gives you hard copy plain paper CRT graphics.

Trilog's Graphic Adapter Board (GAB) instantly gives the Printronix P150, P300 or P600 the ability to generate hard copies from Tektronics CRT displays.

Just plug it into a spare card slot on your Printronix printer/plotter, and it's ready to automatically handle CRT data from one or two 4000-Series Tektronix terminals as well as your normal line printing needs.

CRT image copies are produced on plain paper, up to six copies, full-size fanfold or standard 8½ x 11, in about 20 seconds. The cost per page is about ½ cent.

GAB handles CRT graphics completely off-line, but it works directly with your CPU on other printing/plotting chores.

Self test modes for both graphics and character printing are built in.

Everything from a single GAB board to a complete system including the printer/plotter may be ordered from Trilog.

For more information, circle number 125

The print thickens with LAX.

By compressing characters horizontally, LAX gives you a page thick with type. Up to 132 characters in an 8″ line.

The result can be paper and storage savings up to 40 percent.

What's more, you can easily switch from the compressed density to standard under program control, or an operator accessible switch.

Three different densities at 10cpi, 13⅓ cpi & 16⅔ characters per inch are available to choose from (any combination of two).

And in addition to the compressed and standard ASCII sets, there are four other character sets residing in LAX that are program selectable. Choose from vertical and horizontal bar codes, block characters up to 1 inch high, Katakana, Hebrew, Greek, Russian, etc.

LAX is a direct replacement for the Printronix Logic A module in Printronix P150, P300 and P600 printer/plotters. It adds a lot of extra flexibility without reducing normal capabilities in any way.

Just plug it in. No printer modifications are necessary. Test it in seconds, with the built in self test mode self-test feature.

For more information, circle number 126.

TRILOG

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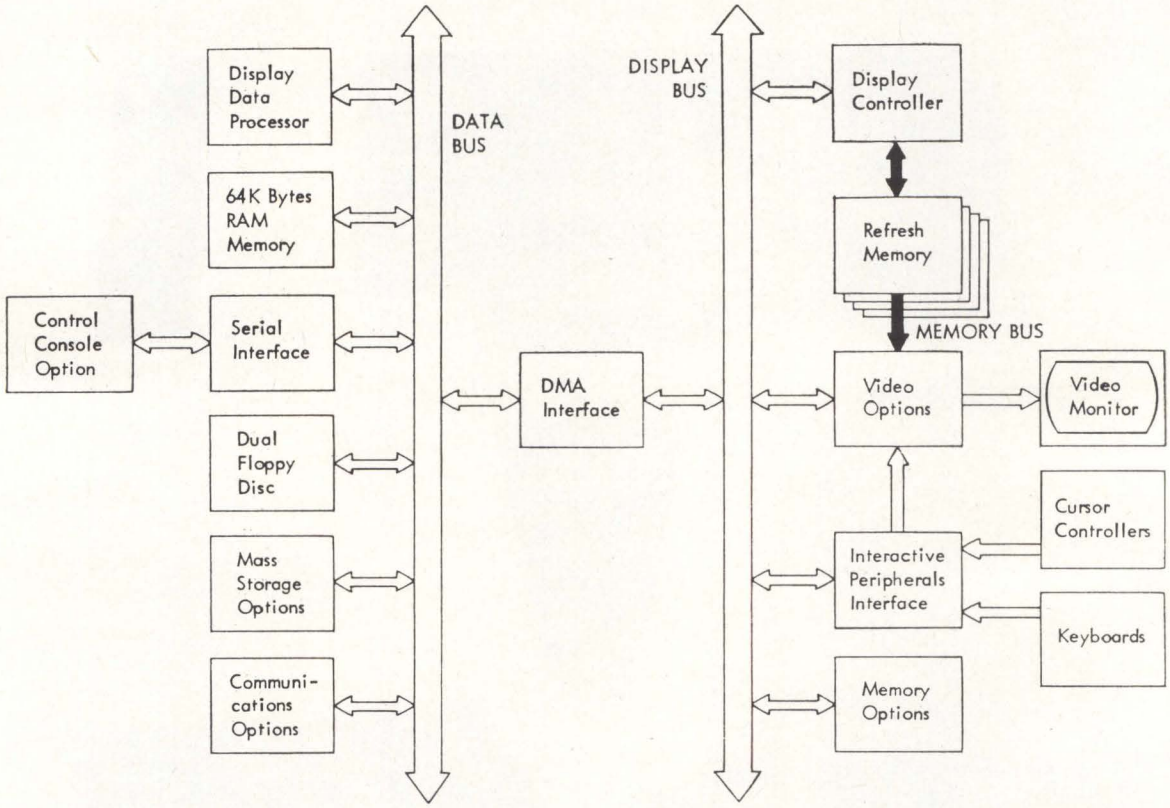

A completely programmable image display system, Ramtek's RM-3000 is based on a modular design that can start out small and add options or capability to fit changing user needs

as well as local mass storage via dual floppy disc drives. Modularity allows special applications to be accomplished with standard components. High speed data processing, fast access MOS RAM refresh, local data storage, and multiple processors allow the system to function independently of host.

System data analysis processor, based on Digital Equipment Corp's LSI-11/2 16-bit microprocessor, includes an extended instruction set which permits floating point arithmetic. Data analysis software is a foreground/background operating system that permits data acquisition and simultaneous data analysis and display. In addition, the system supports Macroassembly, FORTRAN IV, and BASIC languages.

Each model is functionally identical and interprets an identical base instruction set. Each is capable of generating multiple gray scale (black/white) or color images which may be viewed on commercially available video monitors. Display bus options include joystick, keyboard, color or black/white monitor, trackball, expanded memory, and special functions. Serial or parallel interfaces, FORTRAN, BASIC, and magnetic tape, hard disc, or alphanumeric console are data bus options.

Circle 172 on Inquiry Card

Series/1 Enhancements Double Memory Capacity, Add Processing Capability

Hardware enhancements announced by IBM Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301 for the Series/1 computer include a processor, disc storage subsystem, diskette magazine unit, System/370 attachment unit, and 2-channel switch feature card. These, combined with software enhancements, are claimed to significantly extend power and distributed processing capabilities of the system.

Featuring 64k-byte storage cards produced using an FET process that allows high density and fast processing speeds, the 4955 model E processor doubles maximum storage capacity for the Series/1. A basic model provides 64k bytes of storage which is expandable to a maximum of 256k in 64k-byte increments. It also provides the central processing unit, storage address relocation transla-

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So when you spend time and money on an interconnect system, you should consider fiber optics. And that's where we can help you.

We can help you make the right choices for your system. Choices in line attenuation, mechanical strength, environmental isolation, light coupling efficiency. Choices in every element you need.

Ours is the broadest line of optical communication cables in the industry. We've been working with fiber optics for 20 years. And engineers have already put more than 2,000,000,000 feet of our fiber optic products in use. Since we make our cables from raw materials to finished product, we can fill your needs exactly. And at the least expense.

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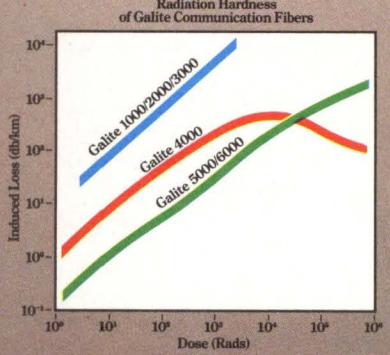
Galileo Park, Sturbridge, Massachusetts 01518

Progress made practical.

As a matter of fact, we can fill your needs more quickly, because all of our standard cables, including Galileo's highly versatile Galite® 3000, are in stock. We even stock complete lines of connectors and electronic components for you.



You can write to Galileo for a detailed information package that will give you a good idea of what fiber optics can do for you today. Or you can call Galileo's application engineers at (617) 347-9191 for specific personal help on how... and where fiber optics could fit into what you're doing today.

You will find we offer more than fiber optics. We also offer know-how.

CIRCLE 17 ON INQUIRY CARD

tor function, basic console, seven I/O feature locations, enclosure, and power supply. Storage cycle time is 660 ns nontranslated and 880 ns translated.

The 4963 disc storage subsystem combines direct access storage devices to provide capacities of 58M to 258M bytes. Multiple subsystems, composed of a primary drive to which up to three expansion drives are connected, may be attached to a processor. Primary drives tie to the Series/1 channel via a microprocessor attachment that has extensive self-checking and diagnostic capabilities.

Both primary and expansion drives have capacities of 58M or 64M bytes. 58M-byte units have additional fixed heads with capacity of 131k bytes. All models have 24-ms average access time for movable heads. Latency is 9.6 ms.

Random access to as many as 23 diskettes is provided by the 4966 diskette magazine unit which features a carriage assembly with five slots: two slots hold magazines that store up to ten diskettes each, and three store individual diskettes. Automatic selection of the desired diskette provides access to 27.8M bytes of data with instantaneous data rates of up to 125k bytes/s.

The channel attachment feature acts as a control unit with 32 device addresses at the System/370 end, and has a single device address at the Series/1 end. It can transfer data under joint consent between the two systems. Providing capability of switching a set of common I/O devices between two Series/1 processors, the 2-channel switch (TCS) plugs into the 4959 I/O expansion unit and connects by cable to the two processors. I/O switching from primary to backup processor is programmable using TCS I/O commands. Manual switching in either direction can be done by the operator.

Among the programming enhancements announced are Series/1 COBOL which allows users to construct, compile, debug, and execute programs all on Series/1 hardware; a Series/1-System/370 channel attach program that enables users to transfer data between applications programs in the two systems; and a Series/1 structured programming facility that operates with the System/370 time-sharing option to increase productivity in developing and modifying programs. Improvements to the real-time programming system and its supporting programs help simplify building of specialized hardware. Additions support complete communications provisions, such as read/write access to a number of terminals, and a sort/merge program for arranging records.

Circle 173 on Inquiry Card

Series/1 Peripherals Encompass Random Access Devices, Console Display

Certainty series equipment, designed for use with IBM Series/1 minicomputers, includes removable disc storage systems, flexible disc systems, sealed data module disc units, matrix and band printers, and an operator console display station. Also introduced by Control Data Corp, Box O, Minneapolis, MN, the 9776 fixed module drive is a high capacity functional replacement for the IBM 3350 disc.

Disc Units

Providing 63M, 123M, or 240M bytes of data storage on removable packs in each cabinet, series 270 systems transfer data to and from the Series/1 computer at 1.2M bytes/s. A controller for the systems occupies one I/O card slot in the central processor. Each drive is a standalone unit with its own power supply and cooling system. Units operate in IBM cycle steal mode to allow multiple sector transfers, and offer initial program load capability.

230 series consists of four fixed sealed data module drives and controllers that mount in the mainframe enclosure. Models 10 and 20 have two or four moving heads to read and record on one or two data surfaces; storage capacities are 9.3M and 19.7M bytes, respectively. 10F and 20F provide an additional 0.74M-bytes of fixed head storage that is accessed by 48 data heads on a single surface.

Flexible drive series 210 model 10 supports single-density, single- or double-sided diskettes and offers 606,208 bytes of storage capacity. It supports all IBM Series/1 formats and provides a data exchange capability with the processor. Exchange with other IBM devices is available through the single-sided diskette, recorded in 128-byte/sector format.

Fixed sealed media and flexible media drives are combined in the 240 series.

A fixed module drive that incorporates two spindles of moving head storage, each having 400M-byte capacity, the 9776 consists of two decks with two head disc assemblies, dc power supply, logic chassis assembly, air circulation system, and ac distribution assembly. The unit provides diagnostic microprograms for maintenance, error detection and correction capability for up to four bits, and rotational position sensing to save latency time. Data transfer rate is 1198k bits/s. Seek time is 25 ms average; average latency is 8.2 ms.

Circle 174 on Inquiry Card

Printers

Offering easily interchangeable horizontally moving character sets, 450 series print bands provide 384 characters which can be divided into 48-, 64-, or 96-char sets. Operating in cycle steal mode, print speed for 132-char lines is determined by size of the character set. Model 10 prints at 360, 300, or 220 lines/min using 48-, 64-, or 96-char sets, respectively; model 20 prints at 720, 600, or 440 lines/min. A compressed pitch feature allows printing of 15 char/in (5.9/cm) instead of the standard 10/in (3.9/cm) permitting the use of smaller forms.

A matrix printer that is capable of providing 16.5 char/in (6.5/cm) at a bidirectional speed of 180 char/s, the 420 series printer prints 132 char/line, 6 or 8 lines/in (2.3 or 3.1/cm).

Circle 175 on Inquiry Card

Display Station

A console/data entry station, the 610 series is a desktop, microprocessor controlled display with format edit features. Mode and command structure is identical to that of the IBM 4979 display station. The unit displays 1920 characters on the 12″ (30.4-cm) diagonal screen in a 24-line by 80-character format. Keyboard layout is identical to the 4979; keys are color coded.

The display station adapter card operates in cycle steal mode and requires one position in the processor or I/O expansion unit. It can be placed remote from the processor—up to 1200 m away.

Circle 176 on Inquiry Card

Small Business System Offers Virtual Memory, Large-Scale Programming

The VDP-1000 data system is a small business computer system that is designed to provide large-scale programming in BASIC, COBOL, and ASGOL. Introduced by Lear Siegler, Inc, Data Products Div, 714 N Brookhurst, Anaheim, CA 92803, the system offers a powerful virtual memory operating system with an extensive instruction set.

Included are a 16-bit CPU, 32k-word RAM, ADM-3A Dumb Terminal™ console, 180-char/s model 310 Ballistic™ printer, and either 10M-byte cartridge or 1.25M-byte floppy disc drive. All electronics, CPU, memory, and disc are housed in a desk, with the console and printer on the top.

The system uses an enhanced interactive BASIC that is compatible with ANSI proposed standards. COBOL is compatible with 1974 ANSI standards for level 2 (X3.23). For system development programming, ASGOL, a hybrid of ALGOL and assembly language, provides a tool for developing applications software.

Circle 177 on Inquiry Card

FORTRAN Compiler Creates Efficient Code for Array Processor

AP FORTRAN, a FORTRAN compiler developed for use with array processors from Floating Point Systems, Inc, PO Box 23489, Portland, OR 97223, can lower programming costs, provide better documentation of applications programs, and minimize program maintenance costs. The language allows users to run existing application programs, with little modification, on a high performance attached processor and will provide code which can run on a system offline from the array processor.

The compiler creates calculation subroutines using standard FORTRAN statements. Because the array processor is used primarily for high speed calculating, the language supports only a subset of FORTRAN IV statements. Principal exclusions are I/O statements and character manipulation facilities.

Code portion of routines is limited only by the size of the array processor's program source memory. This may be up to 4096 64-bit wide words; longer routines may be handled using overlay capability.

Circle 178 on Inquiry Card

Communications Handler Allows 24 Users to Access IBM Mainframes

Multilink channel interface, a communications handler designed for use with IBM System/360 and /370, extends mainframe power by providing realtime access to stored data, and permits file transfer from the mainframe. An integral component of the system from Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284 is a Datashare® Business Timesharing System, which includes CPU, disc storage, system software, and video display terminals. The channel adapter attaches to the I/O bus of this system's processor and to the byte multiplexer channel of the mainframe to link the systems.

Channel interface appears as two different unit record devices to the IBM system. All input to the mainframe is seen as input from a 2501 card reader; when accepting responses, the interface appears as a 1403 printer to the mainframe. Output from the mainframe may be routed to the work station initiating the inquiry, to another station specified in the request, or all output may be directed to a single predetermined workstation.

In addition to its standalone capability the interface may operate in Attached Resource Computer™ systems. In this case the interface has access to all system resources including common data base, print spooling facilities, and communications links.

Multilink configurations may contain Datashare 5500 processors with 48k bytes of user memory which support 200M bytes and 16 users; or 6600 Advanced Business Processors with 120k bytes, 200M bytes, and 24 users. 6010 and 6020 Attached

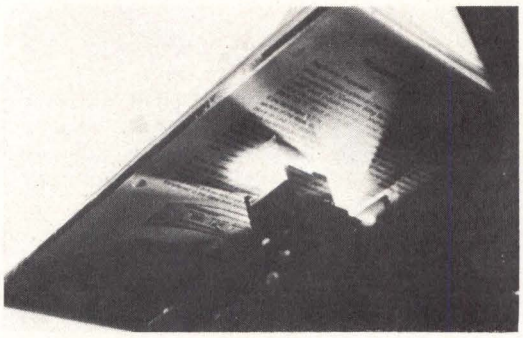
Processors are available for use in Attached Resource Computer systems. Cartridge disc storage is available in 2.5M-, 5M-, 20M-, and 25M-byte increments. System printers range from 80 char/s to 900 lines/min in capability.
Circle 179 on Inquiry Card

OCR Scanning System Converts Printed Material Into Digital Form

A system that is capable of automatically scanning and entering typed or printed documents, the Kurzweil Data Entry Machine (KDEM) replaces manual key entry. An outgrowth of omnifont recognition technology developed by Kurzweil Computer Products, Inc, 264 Third St, Cambridge, MA 02142 as a reading aid for the blind, the system converts print into digital form at approximately 30 char/s—and with an error rate as low as 1 in 20,000.

Consisting basically of an OCR scanner, a CRT for operator control, disc drive for storing intermediate and final files, and a compatible tape file for final storage, the system scans and recognizes ordinary print in any type font or combination of fonts in a range of sizes. It reads documents in their original form to provide significant cost savings over conventional methods of entry.

To optimize the system's internal character definition tables which provide the unit with omnifont capability, the system is operated initially in training mode. In this mode, one line at a time is scanned; recognized characters are displayed on the CRT for operator verification or correction. Data entered are stored for future use. Once training is complete, data entry progresses at maximum throughput in production mode.



Automatically scanning existing documents and converting to digital form Kurzweil's Data Entry machine uses optical character recognition technology to provide multifont capability at a rate of 30 char/s

A magnified picture of the character as it appears on the page along with several lines of surrounding text for context can be displayed on the CRT for operator verification or correction of ambiguous letters

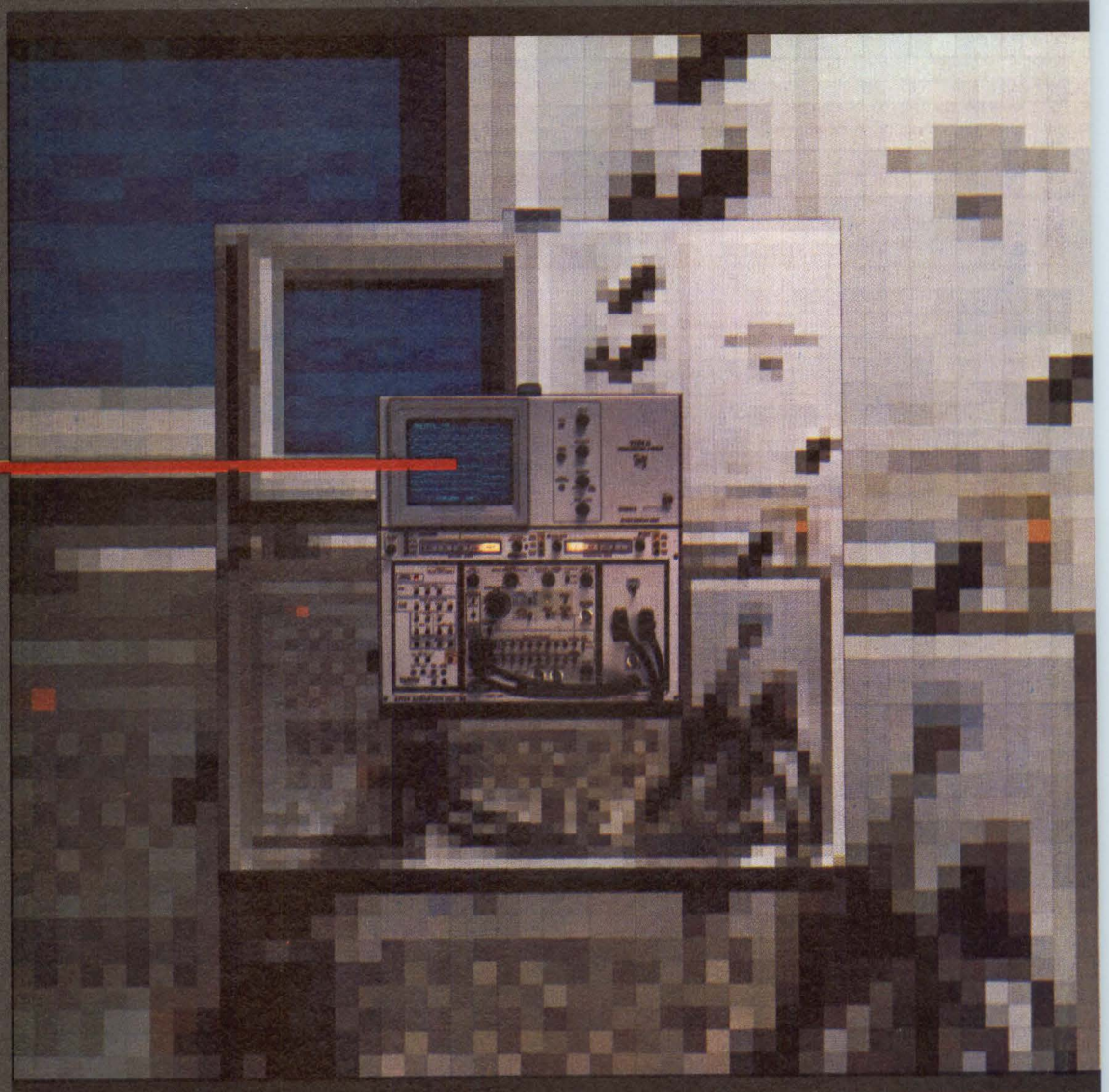
The scanner, a specially designed camera with lighting system, integrated sensing array, and preamplifier circuit riding on a computer controlled X-Y mover, scans the printed page and transmits the analog image to an image enhancement circuit. This circuit brings out features which improve the recognition process by increasing the contrast found on the page and eliminating noise. The enhanced image, now in digital form, is transmitted to the computer.

The computer, under software control, first separates the image into discrete character forms. Characters are considered to be discontiguous forms, with special algorithms handling joined and fragmented characters. Once separated, several hundred features, including topological and geometric properties such as loops, concavities, line segments, vertices, loop extensions, and the relationships of these properties are extracted for each character. This set of properties, called a Multiple Property Descriptor (MPD) is compared to MPDs in the character definition table to generate a tentative identification. This tentative identification can be changed by post-processing routines that consider size and positional relationships. Character identifications generated by the post-processing routines are then subject to possible further modification by operator interventions and editing. Special routines compensate for broken characters.

The character definition table is initialized for each data entry task with a generalized table for multifont character recognition. The table is optimized for each specific task in training mode. Character definition tables, optimized for particular combinations of fonts and print characteristics, can be stored on disc for subsequent use without retraining.
Circle 180 on Inquiry Card

TEKTRONIX thinks your logic analyzer should be as versatile as you are

So ours let you sample with *speed.* With *resolution.* With *confidence.*



Sample with confidence: up to 100 MHZ at 15 ns resolution

Versatility — it's the key to effective, efficient digital design. You've got to be versatile enough to make a variety of measurements every day. And so you need an equally versatile logic analyzer.

Speed is one important measure of logic analyzer versatility, because, especially in asynchronous measurements (say, chip to chip transactions), *faster is better.* Better because high speed means high resolution. And you've got to *see* information accurately in order to *measure* it accurately.

Use Tektronix Logic Analyzers for asynchronous measurements at 20, 50, even 100 MHz — with 15 ns resolution. You can also sample synchronously up to 50 MHz (not all logic analyzers provide synchronous *and* asynchronous operation).

Tektronix speed and resolution mean *confidence.* In the measurements you make...and in the job you do.

High speed data acquisition: it helps make our Logic Analyzers versatile. So you can do today's job and tomorrow's. So you can change applications without changing your logic analyzer.

Contact Tektronix Inc., P.O. Box 500, Beaverton, OR 97077. In Europe, Tektronix Ltd., P.O. Box 36, St. Peter Port, Guernsey, Channel Islands.

For immediate action, dial our toll free automatic answering service; 1-800-547-1512.

Tektronix®
COMMITTED TO EXCELLENCE

TEKTRONIX LOGIC ANALYZERS. THE VERSATILE ONES

For technical data, circle 26 on Inquiry Card. For a demonstration, circle 27 on Inquiry Card.

Announcing the Microcomputer Devel

Microcomputers today are revitalizing existing industries and creating new markets by the score. The reason is simple economics: Microcomputers enable manufacturers to simultaneously add features and cut costs, capturing the competitive edge.

Successful microcomputer users have discovered another basic economic law: the Intel Principle of Microcomputer Development. It proves that the key to successful implementation of new microcomputer-based designs is the control of engineering man-months spent on hardware and software development and integration. That's the reason Intel delivers the Intellec® system. It's the world's most advanced, most widely used microcomputer development system.

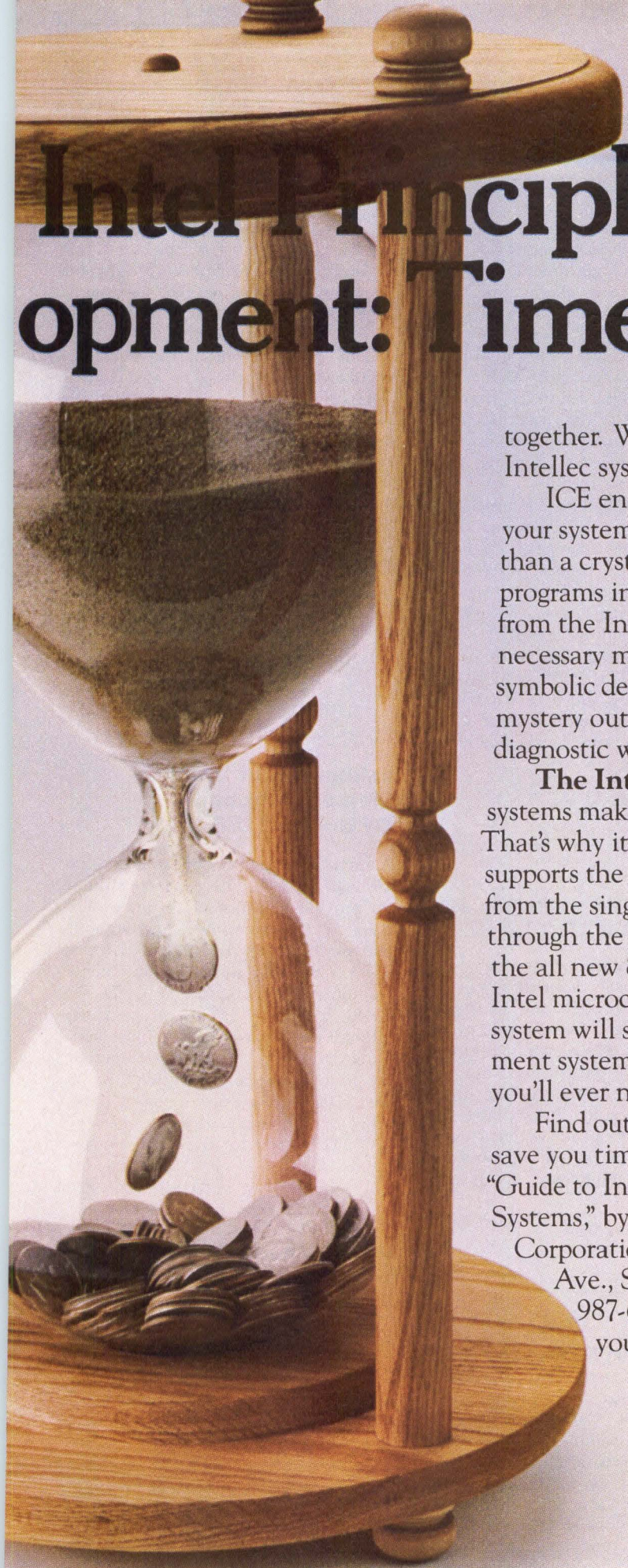
The Intellec system is the "success machine" that's making it possible—and profitable—for hundreds of companies to join the microcomputer revolution. From the twinkling in a product planner's eye, through production, the Intellec system manages, cuts and compresses the development cycle. For new users, Intellec's sophisticated simplicity ensures a smooth transition to the new technology. For experienced users, the Intellec system is the best way to stay at the forefront of microcomputer developments.

The Intellec system cuts manhours. Time is money. Two ways. First, it's the resources invested in product development. Second, it's the competitive advantage you have when you get to market first. That's why the Intellec system gives you *three* programming languages, to help you get your software written efficiently and quickly.

Only the Intellec system gives you such programming flexibility. There's assembly language, for the most memory-efficient programs. And PL/M, the industry's most popular high level language, combines the efficiency of assembly language with the simplicity of a high level language, for development of large programs. And now we've added FORTRAN ANS 77 for 8080 and 8085 users. It's the high level language most engineers are most familiar with.

All three languages compile right on the Intellec system. And with Intellec's unique and powerful relocation and linkage capability, you can use all three for modular software development, and then merge them using time-saving symbolic address references.

The Intellec system gets the bugs out. Nothing is more frustrating than trying to get your "perfectly good" design and "theoretically sound" software to work



Intel Principle of opment: Time is Money.

together. With ICE™ In-Circuit Emulation, the Intellec system ends that frustration.

ICE enables you to start debugging software in your system before your prototype is much more than a crystal and CPU. ICE lets you execute your programs in real time or single steps, with full control from the Intellec system console. And you can make necessary modifications as you go, using fast, simple symbolic debugging. The Intellec system takes the mystery out of microcomputers by giving you a diagnostic window into your system.

The Intellec system is for winners. Intellec systems make it easy to succeed with microcomputers. That's why it's important that the Intellec system supports the entire family of Intel microcomputers, from the single-chip 8021, 8022, 8041, 8048 and 8049 through the industry standard 8080 and 8085, and the all new 8086 16-bit microcomputer. And, as new Intel microcomputers are introduced, the Intellec system will support them, too. It's the only development system you'll ever need for every microcomputer you'll ever need.

Find out more about how the Intellec system can save you time and money. For a free copy of our book, "Guide to Intellec® Microcomputer Development Systems," by Daniel D. McCracken, contact Intel Corporation, Literature Department, 3065 Bowers Ave., Santa Clara, CA 95051. Telephone (408) 987-6475. To arrange a demonstration,contact your nearest Intel distributor or sales office.

intel® delivers.

European Headquarters: Intel International, Brussels, Belgium, Telex 24814.
Japan: Intel Japan K.K., Telex 781-28426.

Circle 28 for information.

Self-Contained Fixed Media Disc Drives Offer High Reliability

Self-contained fixed disc storage drives in the 2700 series have capacities for from 33M to 170M bytes. Introduced by Storage Technology Corp, 2270 S 88th St, Louisville, CO 80027, the units use Winchester technology and have a cooling system that permits their use in virtually any environment.

Modular for accessibility, the units consist of head disc, power supply, and PC board assemblies. The head disc assembly is sealed at the factory for use in any environment. Standard are dual ports which allow drives to be configured for shared access, daisy-chained, or radial access with inline disc drive communication. Port drivers are customized for implementation under microprogram code.

Command, data handling, and error correction logic are part of the system architecture, eliminating the need for those functions in a controller. Interface to any host CPU is through a single 25 signal-pair cable to an adapter card. Dedicated buffers allow data transfers from 0 to 2.0M bytes/s. The track seeking system assures precise positioning of the read/write heads. Average access time is 35 ms.

Factory installed microprocessor code performs error checking, data blocking, string searches, disc to disc copying, port priority resolution, and task queuing. Fault isolation diagnostic routines test all assemblies to subassembly levels.

Deliveries on the 2707 with 33M-byte capacity, 2710 with 80M bytes, and 2720 with 170M-byte capacities are scheduled to begin in spring of 1979. They are aimed specifically at the OEM market.

Circle 181 on Inquiry Card

Transaction Processing System Has 256k Memory For Online Files

System 730, a transaction processing system, offers a maximum memory capacity of 256k bytes to support users needing large quantities of online storage for simultaneous inquiry and update. In its base configuration the system announced by Basic/Four Corp, PO Box C-11921, Santa Ana, CA 92711 consists of 96k memory, four video display terminals, two 75M-byte removable pack disc drives, and 300-line/min printer. Full-duplex asynchronous channels support 16 directly connected or remote terminals.

The microprogrammed CPU provides fast response. Execution speeds are enhanced through use of semiconductor memory with a full cycle time of 600 ns. Memory is equipped with automatic parity checking to detect hardware errors before they cause invalid results. A continuously charged battery pack automatically maintains information in memory in the event of temporary ac power failure.

Circle 182 on Inquiry Card

Word Processing System Priced to Ease Cost-Justification

Wordplex/2, a microprocessor-based, standalone word processing system, provides hardware and software compatibility with multistation distributed logic systems. To ease the problem of cost-justification, the upward compatible system has been priced at less than $14,000 by Wordplex Corp, 141 Triunfo Canyon Rd, Westlake Village, CA 91361.

The compact system has a disc drive storage assembly built into the video display unit. Each of two slots in the assembly accommodates a removable minidiskette which provides 160k bytes of data storage. The 12″ (30.48-cm) diagonal CRT screen displays partial pages of 80 characters by 24 lines. Operator can scroll up or down and pan left and right to scan any portion of the maximum page. Pages can be 128 characters wide and 128 lines deep.

Touch and layout of the movable keyboard match those of a standard electric typewriter. Its complement of 83 keys includes 44 character keys, 10 control keys, and 13 editing function keys.

A Qume or Diablo bidirectional daisy-wheel printer produces hard-copy output at 600 words/min. Screen and printer operate independently, allowing the operator to perform other functions while documents are being printed.

Circle 183 on Inquiry Card

Enhancement Doubles Memory Capacity Of Univac 1108

A memory expansion package for the Univac 1108 has been demonstrated to provide the potential for a 50% gain in the computer's throughput and performance. Implemented using T-7005 memory modules by Telefile Computer Products, Inc, 17131 Daimler St, Irvine, CA 92714, the package, offered on a rework or replacement basis, removes restrictions placed on performance and program size by the 1108's 262k-word memory limit, allowing users to expand memory to 524k words in 131k-word increments.

While the first 262k words in the system can be any mix of Univac and Telefile modules, the second 262k must be formed of T-7005 modules (see *Computer Design*, Mar 1977, pp 42, 46). The expansion carries no memory map penalty, as an unused bit in the Univac memory address is used to provide direct addressing of the entire memory. Added 131k memory increments can be interleaved to increase the effective memory transfer rate. Modifications to the 1108 mainframe increase memory module channels from four to eight (each accessing a 64k-word module). These modifications are transparent to the operating system.

Circle 184 on Inquiry Card

The Ampex alternative to NOVA* minis. Extra value.

Ampex minicomputers are available in your choice of 800 or 1200 nanosecond operation, and feature direct addressing of 64K words of core or MOS memory. There's even a version with 64K words of MOS memory right on the CPU board.

Of course they execute the Nova instruction set, and they're compatible with peripherals and controllers designed for use with Nova computers, but that's only the start.

You'll also find front access to all components, a single bus structure, and a programmer's console with octal pad input, octal readout and LED indicators. And options include automatic program load, firmware multiply/divide and power fail/auto-restart.

Three chassis configurations let you specify 5, 13 or 21 slot capacity. The 21 slot version accepts 17 boards plus a staggering 2 megabytes of Megastore—the Ampex solid-state alternative to fixed-head disk.

The technical story is in a free brochure, and the economic advantages will be obvious when we discuss quantity, dollars and cents. Write Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Or call Charley Penrose at (213) 640-0150. Extra value makes *this* alternative the first choice.

AMPEX

*Nova is a trademark of Data General Corporation

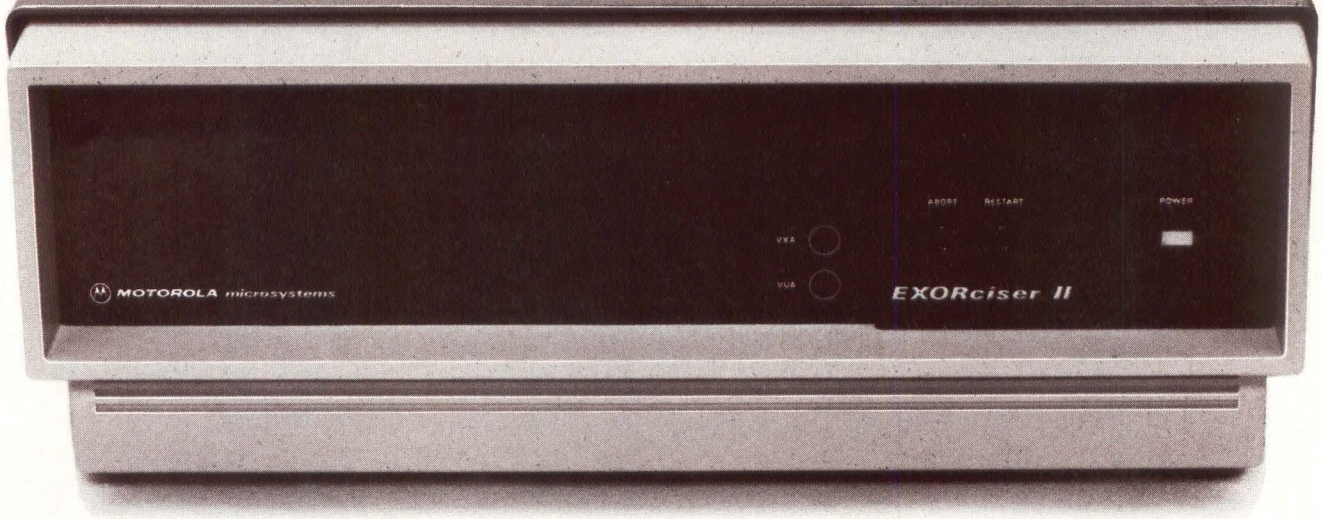
CIRCLE 29 ON INQUIRY CARD

Four new Motorola system development tools

for MPU, bit-slice, and single-chip microcomputers.

A quartet of recently introduced system development tools from Motorola Microsystems keeps Motorola's product line in harmony with the unmatched versatility of the processors they support.

The EXORciser II* Development System improves on the original EXORciser* without making it obsolete. MACE 29/800* extends the EXORciser's capability to systems using bit-slice architecture. The 3870 Emulator and 141000 Simulator are EXORciser-based development tools for single-chip microcomputers.



EXORciser II develops high-speed systems.

EXORciser II does everything the EXORciser does, adds a couple of neat new wrinkles, and operates at twice the speed. The key to the high speed is the new MPU II module, which includes both the system clock and the 2.0 MHz MC68B00 MPU. The clock circuit generates your choice of 1.0, 1.5, or 2.0 MHz signals, so the EXORciser II supports the full range of M6800 Family microprocessors.

DEbug II provides EXORciser II with a dual memory map. This capability dedicates a full 64K memory map to EXORciser II, and creates a second 64K map in which you may implement your system. EXORciser II I/O can be accessed from either memory map.

The EXORciser II includes 32K of RAM, power supply, RS-232 port, selectable Baud rates from 110 to 9600, and a Macro Assembler/Editor. Optional modules also are available.

As for software, EXORciser II operates with all Motorola standard resident software packages; FORTRAN, COBOL, MPL, BASIC and Macro Assembler/Linking Loader.

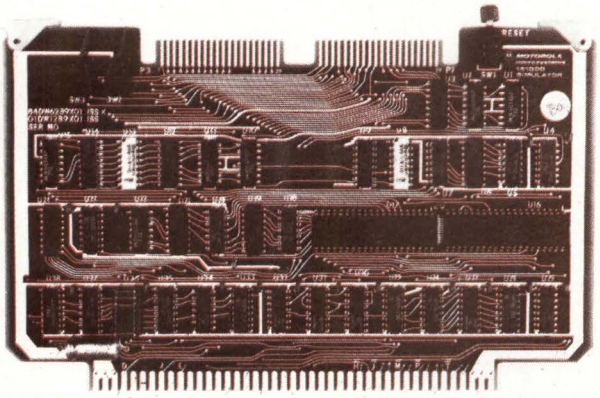
*Trademark of Motorola Inc.

MACE develops ultra-high-speed systems.

MACE 29/800 minimizes the time and trouble of producing microprograms for systems based on bit-slice families like Motorola's high-speed M2900 and ultra high-speed M10800. The MACE 29/800 includes an EXORciser bus-compatible interface module and an EXORciser-resident software package that translate all microprogramming tasks into M6800-oriented operations.

The Write Control Store (WCS) in which your microprogram will reside is expandable in both depth and width. Ratios range between 8K words by 16 bits and 2K words by 112 bits, with intermediate configurations selectable in increments of 2K words or 16 bits. A maximum of seven WCS modules can be used.

MACE 29/800 is available as a separate unit for those who already have an EXORciser, terminal, and printer, or as a complete development station.

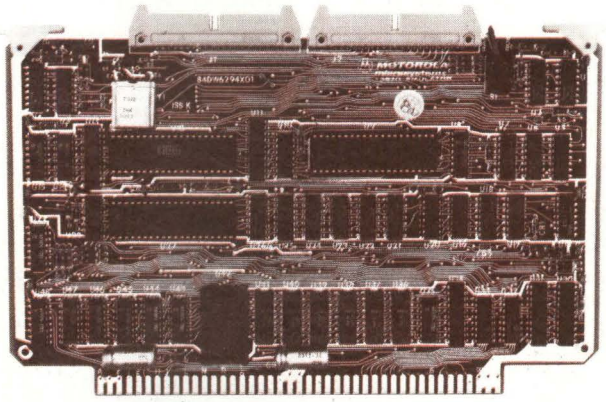


MC14 1000 Development System provides microcomputer simulation.

The 14 1000/1200 Simulator is an EXORciser-based system development tool for debugging designs using the new MC14 1000 series CMOS single-chip microcomputers. Complete software requirements are met, including cross assembler, loader, and debug package.

This module provides complete simulation of the proposed MC14 1000/1200 system hardware characteristics, for correction of problems prior to initiation of final production masks.

For additional information on any of Motorola's EXORciser or EXORciser-based system development tools, complete the coupon or write your request for specific information to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.



MC3870 Development System provides real-time emulation.

The 3870 Emulator is another plug-in extension of the EXORciser. It provides real-time emulation of the MC3870 single-chip microcomputer.

The EXORciser-resident Cross Assembler converts your 3870 source statements into an executable program. After this program is debugged, it's stored in a 2K EPROM for final evaluation. With the EPROM inserted in the socket provided, the emulator module can operate independently of the EXORciser.

To: **Motorola Microsystems**
P.O. Box 20912, Phoenix, AZ 85036

☐ I have an immediate requirement for microsystem development tools. Please contact me as soon as possible. Please send me technical information on:

☐ EXORciser II ☐ MACE 29/800
☐ 3870 Emulator ☐ 14 1000/1200 Simulator

Name _____ Title _____

Company _____ Dept. _____

Address _____ Phone _____

City, State, ZIP _____

MOTOROLA
Semiconductor Group

CIRCLE 30 ON INQUIRY CARD

Computer Controlled ATE Systems Adapt To Changing Needs

Capable of performing static, functional, and dynamic testing of analog, digital, and hybrid units, System 390 provides comprehensive testing with high throughput. Instrumentation Engineering, 169 Susquehanna Ave, Franklin Lakes, NJ 07417 designed the family with modularity sufficient to permit users to configure a solution to immediate needs while providing for growth. It can meet users test requirements and satisfy special needs such as board size, volume, or complexity.

Basic design features include modular hardware consisting of more than 300 different stimulus, measurement, and control devices and a universal unit-under-test oriented interface panel. A software time-shared operating system allows simultaneous production testing, programming, printing, and design. The time domain simulator has a library of commercially available ICs, MPUs, and UARTs. Modular construction and the library of software routines and interfaces permit station configurations to be assembled to test requirements at minimal cost. Test system changes can be accomplished by updating hardware components without change to the universal operating system.

ATLAS, the system programming language, uses common English test terminology. Online editing and compilation are provided as well as flexible software switching that minimizes the need for patch panels or adapter boards. A remote service capability permits realtime service assistance via bidirectional data transmission between user and factory service center.

Circle 185 on Inquiry Card

Digital Avionics System Demonstrates Variety Of Capabilities

A Digital Avionics Information System (DAIS) program that could revolutionize aircraft avionics and cockpit displays integrates hardware and software to permit a "pilot" to perform all cockpit functions. Functional capabilities being demonstrated by Air Force Avionics Laboratory engineers at Wright-Patterson AFB, OH 45433 include preflight takeoff and climb, cruise, navigation, management of aircraft weapon systems, weapon delivery, and precision approach and landing.

The program consists of four core elements: processors or minicomputers, multiplex hardware, computer programs, and controls and display systems. Processors are general-purpose, digital computers engineered by Westinghouse Electric Corp, Baltimore, Md for airborne use. Multiplex hardware developed by IBM Corp, Owego, NY provides standardized information transfer between other core elements in the system. Processor programs have a modular form to allow easy mission to mission sensor or weapon changes, provide flexibility for modifications, and permit transfer to other aircraft applications.

Controls and displays include five miniature TV picture tubes which function as a vertical situation display for aircraft attitude control data, two multipurpose displays for weapon sensor symbology and system status, a horizontal display for navigation data, and a multifunction keyboard that the pilot uses to operate aircraft subsystems. System displays use one common display for several functions; this sharing of controls and displays means that avionics acquisition and retrofit will be less expensive, and eases the job of flying for the pilot.

Interface Subsystems Expand I/O Capabilities of 2100/21MX Minicomputers

Three interface subsystems expand I/O capabilities and applications for HP 2100/21MX series minicomputers by providing 1-port asynchronous serial communication, 8-bit parallel output, and analog data acquisition. In designing the interfaces, Analytical Systems Corp, PO Box 533, Elgin, IL 60120 has provided a complete hardware/software package that considers the I/O interface from the viewpoint of the operating system and the peripheral device and its functional requirements.

Providing all hardware and software required for a single asynchronous serial communication port, the 21101 interface subsystem allows direct attachment of peripherals supporting interactive hardcopy terminals, video terminals, or line printers. All data and control signals conform to EIA RS-232-C specifications. The subsystem functions with 2100/21MX computers and is supported for RTE operating systems.

The 21201 parallel interface subsystem consists of RTE driver, controller card, and interface cable. It provides a DMA/DCPC driven 8-bit parallel output port. Compatibility with peripheral interface configurations is attained via switch selection on the controller card and recognition by the driver of the assigned I/O channel. Low system overhead and high throughput result from transferring data via DMA and control codes via interrupt mode.

An intelligent controller, control memory, and 12-bit resolution A-D conversion elements are provided by the single card 21301 analog data acquisition subsystem. After initializing control memory with data acquisition parameters, the interface functions independently of the computer to acquire information from designated 32 single-ended or 16 differential analog channels at specified intervals. The two RTE drivers permit processed data to be stored into a user buffer or spooled to a designated disc file.

Circle 186 on Inquiry Card

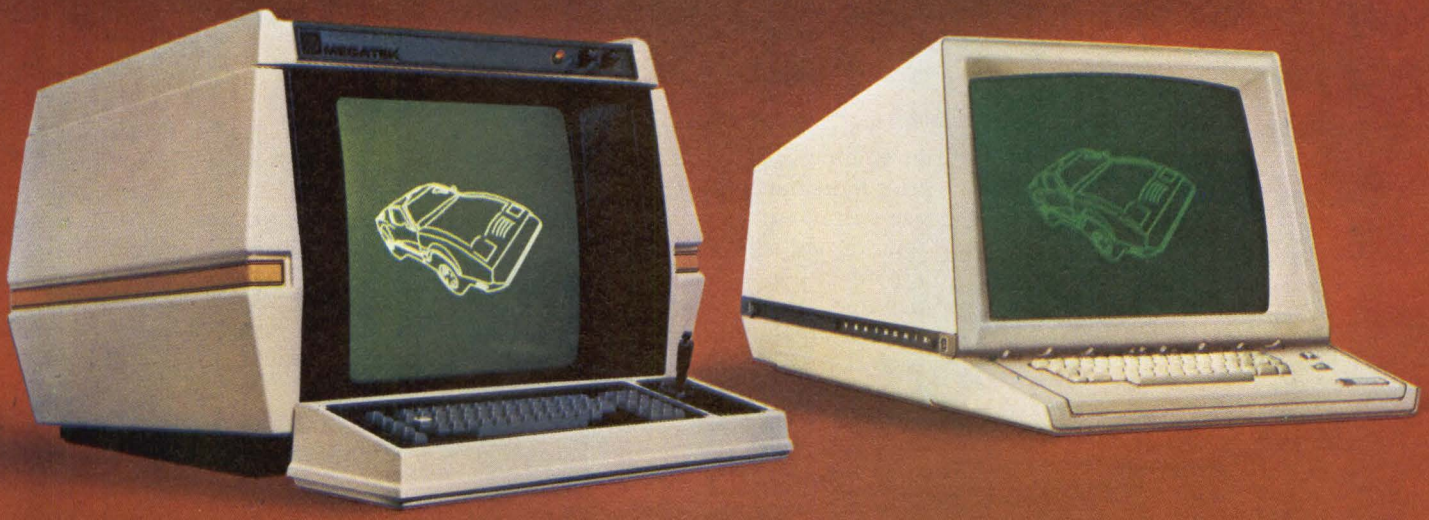
In-Circuit Test System Inspects LSI Devices And Analog Components

Troubleshooter 800 provides capability to test MSI and LSI devices, in addition to SSI and analog components. Analog and digital points are available to a maximum of 1024. The system produced by Zehntel Inc, 2440 Stanwell Dr, Concord, CA 94520 uses a signature analysis format to generate stimuli and learn the output signature that sets acceptance criteria for the IC chip being tested. This technique cuts test program preparation time dramatically.

In the programming area the TS-800 uses a high level intuitive test language. Hardware and software are provided to automatically generate test programs and debug them on initial test of a known-good board. Programs are stored on dual floppy discs. An SBC 80/20 serves as the main system controller. □

Circle 187 on Inquiry Card

Twins.



Your computer can't tell them apart.

Good product, the 4014.™ So good, in fact, that we designed our MEGRAPHIC 5014 Refresh Graphics System to do everything the 4014™ does, and more.

The secret? A high performance graphic processor coupled with a high resolution electromagnetic CRT. A built-in minicomputer. And EMUTEK,™ our proprietary emulator that makes your computer think it's talking to a *TEKTRONIX® 4014.™

But, right away, you'll see that one system delivers more graphics for the money.

Zoom, scale, clip, rotate, and "rubber band" images to your heart's content. The 5014 is a refresh graphics system and that means there is no need to erase the whole screen to make changes. The 5014 does it in real time. Plus a full FORTRAN OS.

And, unlike storage tubes, the 5014 has variable brightness levels. So you can see clearly even under the strongest office lighting.

But, best of all, the MEGRAPHIC 5014 costs substantially less than comparable systems. For the OEM, that means better margins. And, for the sophisticated end user, it simply means more interactive graphics for the money.

So before you buy any graphics system, call MEGATEK at (714) 455-5590.

Don't wait. And don't pay more for less. If your 4014™ just isn't enough system, call Peter Shaw today and ask for a demonstration of the MEGRAPHIC 5014 System.

Thirty days later, you could have twins.

*"TEKTRONIX®" and 4014™ are registered trademarks of Tektronix, Inc., use of which in no way constitutes endorsement.

The refreshing alternative.

MEGATEK CORPORATION

3931 Sorrento Valley Blvd.
San Diego, California 92121
Telephone: (714) 455-5590
TWX: 910-337-1270

14, rue de l'Ancien Port
1201 Geneva, Switzerland
Telephone: (022) 32.97.20
Telex: 23343

CIRCLE 31 ON INQUIRY CARD

Hard copy made easy.

With the help of a high-speed microprocessor, Hewlett-Packard combines exceptional performance and convenience in a new low-cost printer and printing terminal.

The HP 2631A printer and HP 2635A printing terminal with alphanumeric keyboard are the first members of a new Hewlett-Packard family of hard copy terminals.

Each machine was designed to give you a number of high-performance features. And both can support a variety of interfaces, including RS232 and CCITT.V24, to fit into systems made by HP and other manufacturers.

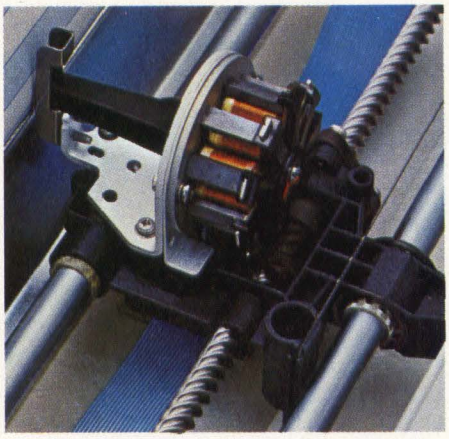
Bi-directional printing increases throughput. Both printers zip along at 180 cps in both directions, depending on your line layout. The microprocessor chooses the quickest path, and increases the speed even more by suppressing leading and trailing blanks.

High-speed slew for columnar data. When the microprocessor senses more than ten blanks in a row, it slews the print head at 45 inches per second to the next print position.

Three ways to print. The Character Compress/Expand Modes let you print more data on a page and emphasize points with headlines and titles. You can get as many as 132 characters on an 8-inch line, or 227 on a 14-inch line.

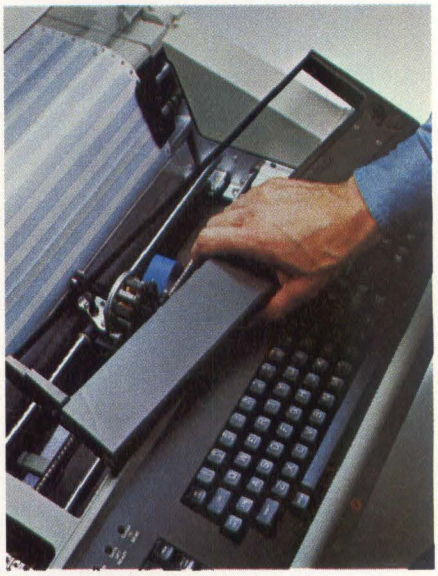
High-quality print, with six copy resolution. A 7 x 9 dot matrix (versus the usual 7 x 7) gives you clear, crisp printouts, right down to the sixth copy and meets the 128-character USASCII standard. And the extra two dot rows allow true underlining and descenders without character blurring.

Programmably interchangeable character sets. The HP 2631 can be made to print alternate character sets without reconfiguring the printer.



Long lasting, quick change print head saves service calls. The 9 wire print head is conservatively rated at a 100 million character life-span. It's also self-aligning. When you finally replace the head, you can do it yourself in a couple of minutes.

Long-life cartridge ribbon for a clean change. With a life span of at least 10 million characters, this innovative drop-in cartridge takes the mess and trouble out of ribbon changes.



Self-test for quick status checks. One key tells you if the printer is ready to go. If it isn't, the self-test feature helps you isolate the problem, reducing the time and cost for repairs.

Run everything under program control. All the features described and more can be programmably controlled. The software can take you in and out of the various modes. Or you can make a change yourself using one of the front panel switches or keys.

In a network or as part of a stand-alone system, HP now makes it simple to get the hard copy you need. If you'd like to see our printer or printing terminal in action, call the Hewlett-Packard sales office listed in the White Pages and ask for a computer systems representative. Or send us the coupon.

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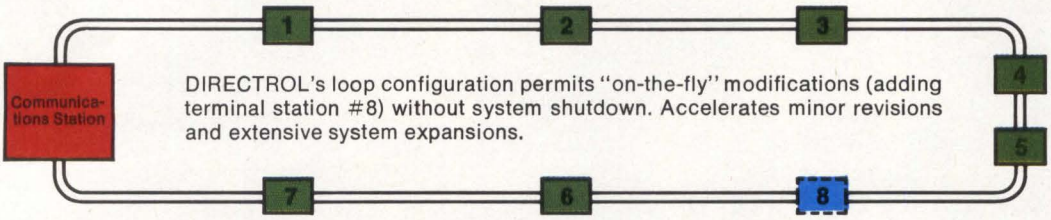
CIRCLE 32 ON INQUIRY CARD


Fast, efficient
and economical;
the new printer and
printing terminal from
Hewlett-Packard.
HEWLETT hp PACKARD

New DIRECTROL™ Multiplexer. Signaling new directions for industrial control.

Cutler-Hammer's new DIRECTROL . . . finally, here's a multiplexer that's practical for industrial control application. DIRECTROL achieves startling advantages in project simplification, system productivity and plant versatility.



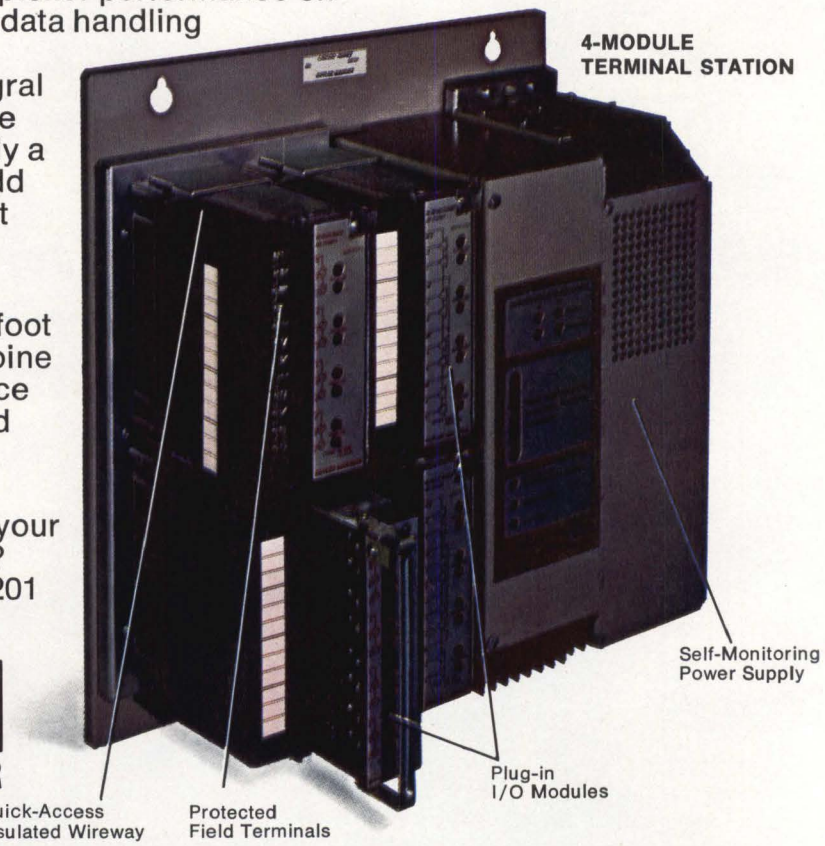
DIRECTROL's loop configuration permits "on-the-fly" modifications (adding terminal station #8) without system shutdown. Accelerates minor revisions and extensive system expansions.

Project simplification. DIRECTROL is designed and applied in a conventional control manner. But unlike the conventional, it substantially reduces wiring costs and project complexity—easily adapting to unanticipated requirements. For the first time, DIRECTROL offers control multiplexing in easy-to-apply, easy-to-order, easy-to-install modules.

System productivity. DIRECTROL's innovative approach provides high-yield features like monitoring of multiplexer performance on every signal scan, high security data handling routines, self-diagnostic/self-correcting characteristics, integral high noise immunity and multiple redundancy options to name only a few. Plus the unique ability to add new stations "on the fly" without affecting system operation.

Plant versatility. DIRECTROL's 4,096 signal capacity and 5,000 foot distance between stations combine with "stand-alone" independence or computer compatibility to add dramatic equipment selection flexibility for future needs.

Why not set a new course for your industrial control requirements? Write Milwaukee, Wisconsin 53201 for descriptive brochure.



CUTLER-HAMMER

Best by Design

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Production Processes Monitored By Microprocessor Controlled Noncontact Inspection Systems

Noncontact inspection—whether used to detect surface defects, determine position or shape, or measure size—is not a novel procedure in quality assurance. The ability to examine a product during assembly without delays or other interference to the processing operations has proven to be a valuable asset. However, tying in such inspection procedures with the control and data handling capabilities of a microprocessor has increased overall values even further.

One such basic procedure uses a solid-state imaging or scanning camera as the viewing device. Imaging cameras are functionally similar to vidicon type TV cameras except that the solid-state units have digital output, greater geometric accuracy, extended spectral range, and higher scan rates. They basically are also more rugged and have greater reliability in process control environments. In addition, they are smaller and have lower voltage and power requirements.

In imaging cameras, a solid-state sensor—either a linear or a 2-dimensional (matrix) array of photodiodes—serves in place of the film plane (Fig 1). The camera lens projects the field of view onto the image sensor which is scanned electronically to produce a train of analog pulses that are proportional in amplitude to the light intensity on the corresponding photodiodes. The pulse outputs are then thresholded and digitized for processing by an electronic controller. Depending on the application, such controllers can be programmed to display various parameters: edge position, object width, surface condition, or other factor.

Possible applications for such photosensitive viewing systems are diverse. "Typical" examples are a system that detects opaque defects in molded glass lenses and one that inspects rows of tablets of different colors and sizes in transparent holders. Both these and several other proprietary systems with related capabilities were developed by Reticon Corp, 910 Benicia Ave, Sunnyvale, CA 94086 and are either now online or in final fabrication stages.

Opaque Defect Detection for Molded Glass Lenses

Primary sensor in a system for automatic noncontacting detection of opaque particles in molded glass lenses is a line scan camera with a 512-element photodiode array. This array has a field of view of 6″ (15.2 cm) modulated by a varying light pattern created by defects and glass refractions of molded glass lenses as they pass along a conveyor. Camera optics focus the image of the back illuminated lens onto the array which is electronically scanned at very high speed. A narrow section of the lens is inspected by each scan, but the entire lens is inspected as it is transported past the camera. A defect in the lens reduces the output of the corresponding light sensitive element(s) because full transmission of the backlighted illumination is prevented. The defect can be detected and its size measured by counting the number of scans over which the condition persists.

Camera output is processed by an electronic controller containing an 8080-based microcomputer that is programmed to discriminate between opaque defects of rejectable size and the normal diffusion pattern of the molded lens. Data from the camera are continually transmitted to the controller which determines if the illumination level is at or above a preset threshold, if there is a molded lens in the field of view, and if any defects are present and meet the criteria for rejection of the lens. Defects of 0.0625″ (1.5888 mm) are detectable at a flow rate of 60 lenses/min.

Correct illumination level is determined by the light output of the illumination panel, diffusion of the sample lens under test, camera lens aperture, and camera scan speed. The system operates near the photodiode array saturation level with a panel indicator signifying that the first and last elements and a predetermined number of other elements are at the saturation level.

A diffuse illumination area source is positioned over the top of the conveyor to illuminate the concave surface of the molded lens with the line scan camera located at the opposite side in order to minimize optical refraction effects of the molded lens pattern. The resulting optical signature consists of a dark ring at the edge of the molded lens and dark spots if opaque areas are present. A defect at the edge of the molded lens would cause the edge pattern to be enlarged and, therefore, detectable. Other defects, such as chips and glass malformations, are also detectable. If the lens is to be rejected, a signal closure is sent to an air system that diverts that lens to a collection point.

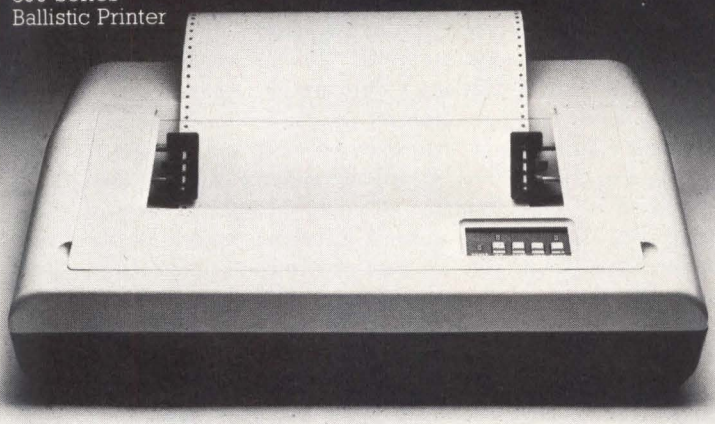
Defect limits are set into the controller by thumbwheel switches on the control panel. Illuminated indicators confirm the presence of the correct illumination level and the completed scanning of a lens. Two electromechanical counters provide cumulative totals of both passed and rejected lenses inspected since the last resetting of the counters. In addition, a thumbwheel switch, LED display, and associated pushbutton switches are provided for use during setup and corrective maintenance.

(*Continued on p* 58)

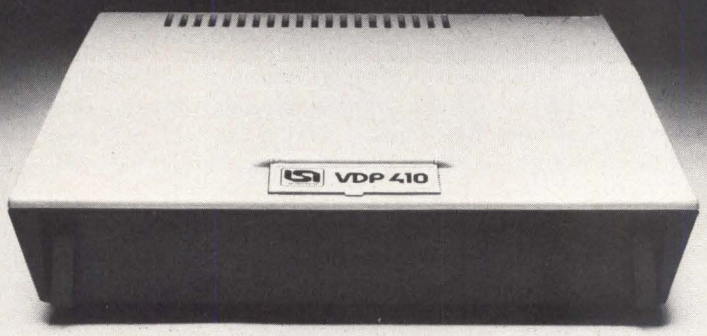
ADM 31

ADM 42

300 Series
Ballistic Printer



VDP 410



VDP 1000

These products were designed by our customers.

At Lear Siegler, we listen to our customers.

As a result, we build all our products from your point of view. So you get what you want, and we get what we want.

That's the way we've always done things at LSI. And it's the way we'll always do them.

Our new line of products reflects that philosophy. All five products come with features you said you needed.

THE ADM-31 PROVES 2 PAGES ARE BETTER THAN ONE.

A lot of people need a smart terminal with a full two pages of display. But can't get them. Not even on terminals costing several times what they want to spend.

So we listened. And then gave them the ADM-31. A low-cost, high-reliability desktop CRT terminal with a full two-page display. As standard equipment—not as an option.

We made the ADM-31 completely self-contained, with a keyboard, control logic, character generator, refresh memory, and interface. Along with full editing, formatting, and protected fields capabilities. What's more, it has a microprocessor which makes it even more reliable and easy to use. And the ADM-31's behavior modification even gives you a factory installed personality.

If this sounds like just the thing you need, it should come as no surprise. After all, you were the one who told us what you wanted.

THE ADM-42 DOES EVERYTHING BUT THINK FOR ITSELF.

Our customers told us they wanted a semi-intelligent terminal.

One with flexibility of format, security, editing, interface, and transmission. They wanted a full two-page display as standard equipment. An optionally extended memory capable of adding data space up to a maximum of 8 pages. Behavior modification. 16 function keys for 32 separate commands. And a 25th line established and reserved exclusively for status indicators and messages up to 79 characters.

So our engineers designed the ADM-42.

A terminal that actually seems to get smarter the more you use it.

THE 300 BALLISTIC™ PRINTER COMES WITH BELLS & WHISTLES STANDARD.

Our customers said they'd like to see bells and whistles as standard equipment.

And that's what we gave them.

The 300 is a low-cost printer with a built-in microprocessor that gives you 15 switch selectable form lengths, 15 perforation skip over formats, and full horizontal and vertical tabulation control. Plus a non-volatile forms retention system that retains these programmable settings when power to the printer is turned off.

And like all our Ballistic Printers, the 300 dependability originates with its ingeniously simple, patented Ballistic Print Head. Which lets it purr along at a respectable 180 cps.

So when you buy our 300 Series Ballistic Printer, there's only one thing we won't offer you much of.

Options.

Because, on the 300, most of them are standard.

OUR VDP-410 KNOWS HOW TO KEEP THINGS UNDER CONTROL.

A lot of OEMs said they needed a building block for system development. Something that would give them the flexibility to configure a variety of systems.

So we built the VDP-410. The intelligent controller in the plain brown box.

It's a low-cost, 16-bit CPU with enough speed and ports to support a variety of peripherals. And it lets OEMs build a multitude of systems. From communications controllers without external storage capabilities, to sophisticated timesharing systems with a string of terminals, printers, and disks.

The OEMs said they wanted something simple, intelligent, and powerful. So we built it.

Because what was a good idea to OEMs turned out to be a real brainstorm for us.

THE VDP-1000 SPEAKS YOUR LANGUAGE.

People told us they needed a complete small data system with the attributes of larger, more expensive systems.

So our engineers came up with the VDP-1000.

It comes standard with a choice of BASIC, COBOL, or ASGOL* programming languages. A virtual memory operating system (VMOS). A 16-bit CPU, 32K, 16-bit words of dynamic RAM, the world-renowned Dumb Terminal,™ a 180 cps, bi-directional 300 Ballistic Printer, and a 10 megabyte cartridge disk. The VDP-1000 is also available with a 1.25 megabyte floppy disk.

Once you've got the basic system, you can add additional storage as you need it. Or want it. It's up to you.

ALL OUR SMART IDEAS EVOLVED FROM A DUMB ONE.

That means the proven reliability and cost-effectiveness of the Dumb Terminal go into everything we make. And we make something for just about any requirement you may have. That's why we're known as the complete terminal company.

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LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

CIRCLE 155 ON INQUIRY CARD

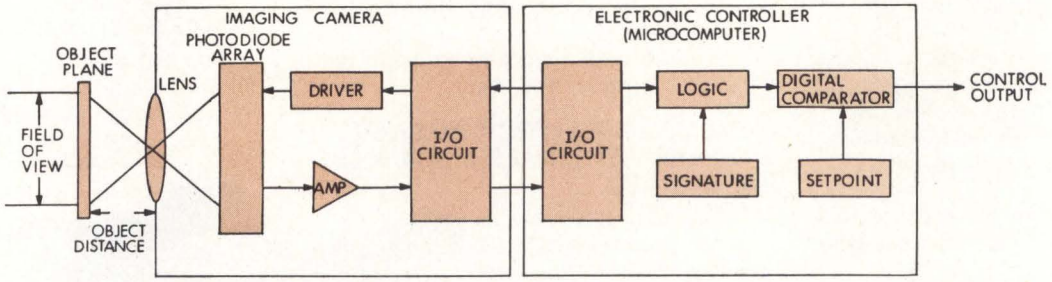


Fig 1 Typical camera-controller system diagram. Similar configurations of solid-state imaging or line scan camera, linear or 2-dimensional photosensitive array, and electronic controller are used in noncontact inspection systems. Photosensitive elements in arrays receive analog signals from camera and send them to controller for digitizing into format acceptable to microcomputer

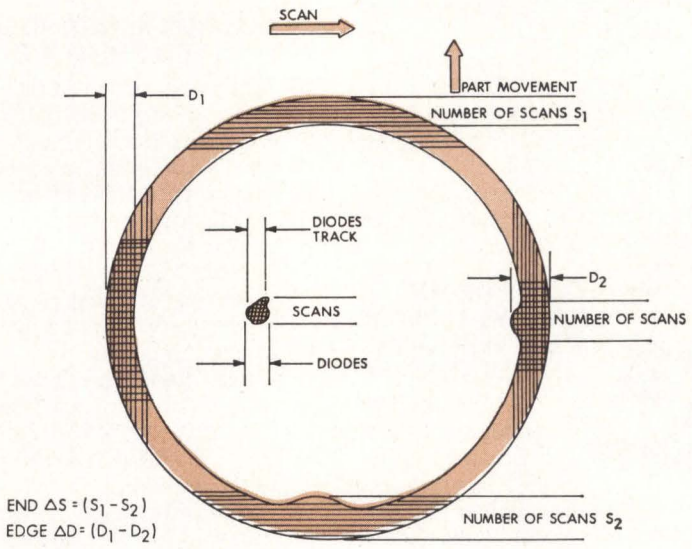


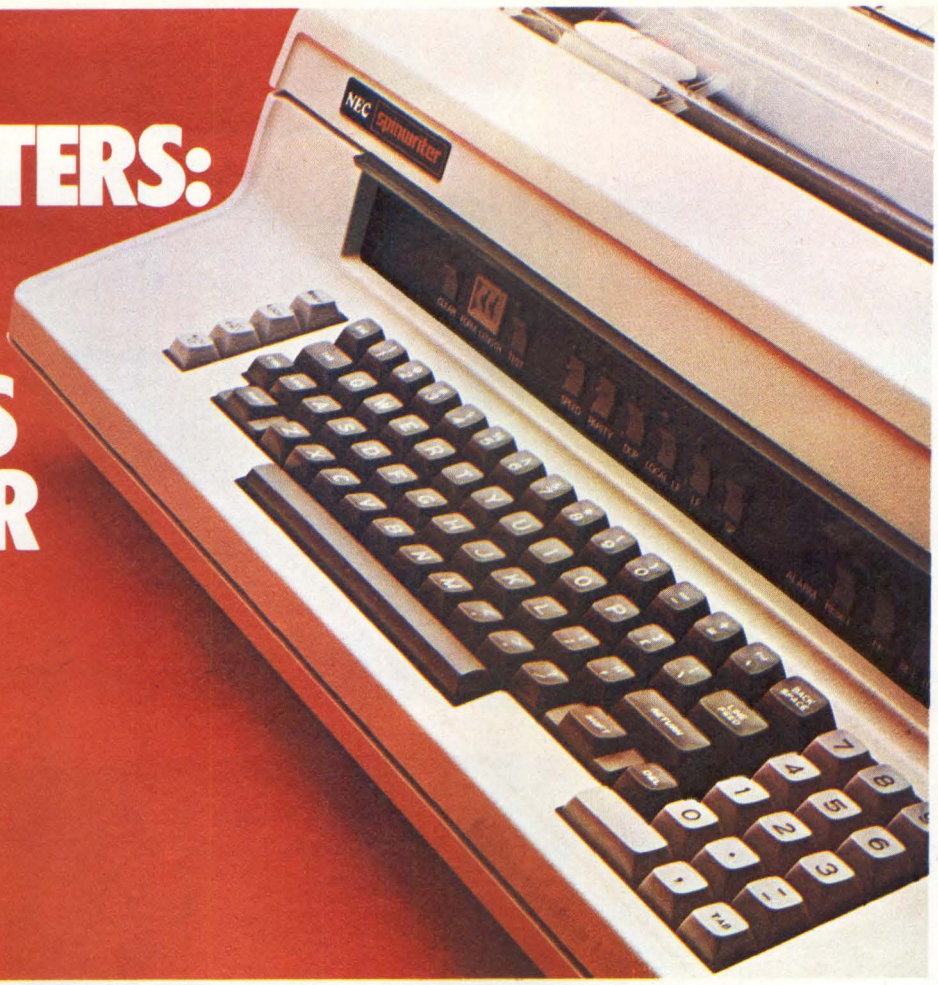
Fig 2 Pictorial representation of lens test system reject criteria. When ΔD is exceeded for more scans than are set into edge scan thumbwheel, dark area is considered cause for rejection. Diode count must exceed center diode track value before dark counts are processed for each scan

Relationship of thumbwheel switch inspection settings and physical geometry of the lens are shown in Fig 2. Defects which are at either end are detected and considered to be causes for failure by comparing the number of scans at the start and end of the lens. Because a defect creates a wider border, the difference in border width should indicate the presence of a defect. Any defect that falls along the edge of the lens is evaluated with two criteria: the added diodes (ΔD) and the number of scans for which the larger diode count exists. A center defect is detected when the diode count exceeds the center diode track settings for each camera scan.

For the duration of the defect, scan diode count is compared to the center diode thumbwheel setting. Each scan at which the center diode track setting is equaled or exceeded and for which the address of the leading edge of the defect is within 10 diodes of the address in a previous scan is noted and added to previous scans. When the total number of scans exceeds the center scan fail setting, a failure is indicated. This enables defects which

THE NEC SPINWRITERS:

PRINTERS MADE FOR PEOPLE.



It takes craftsmanship and attention to detail to make a fine automobile, a fine watch, or a fine character printer. Those qualities, available at low cost, have made the Spinwriter family from NEC Information Systems the finest character printers available.

Spinwriters offer performance beyond that of today's best character printers, at prices averaging 10 percent below competition. But NEC craftsmanship extends beyond performance and price, to features designed for the people who use Spinwriters. No other character printers are as easy to operate, as reliable, or as easy to repair.

Die-cast aluminum housings lined with sound-absorbing foam make Spinwriters quieter than office typewriters – and as easy to use.

Spinwriter housings swing open for easy operator access to ribbons and the thimble element, and easy access for service personnel to Spinwriters' modular components. Ribbons, thimble elements, and forms-handling modules can be replaced within seconds.

Spinwriter keyboard send/receive (KSR) printers also provide easier operator access to controls offering more functional capabilities than other character printers provide. A thumbwheel switch enables your operators to specify the precise forms length desired, and they can specify vertical spacing at either six or eight lines per inch. The unique Spinwriter self-test feature is enhanced to include the interface and communications lines in on-line applications.

Compare Spinwriters with the printers you use now, and see how NEC craftsmanship makes Spinwriters different. See the difference in Spinwriters' smooth-contoured styling, and feel the difference in durability. The appearance, and the ruggedness of Spinwriter printers allow them to fit well in every environment.

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CIRCLE 34 ON INQUIRY CARD

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Now when a citizen reports a crime, our minis verify the address. Examine the surrounding area for similar calls, hazards, and temporary situations (such as streets under repair). And suggest which units should respond to the call.

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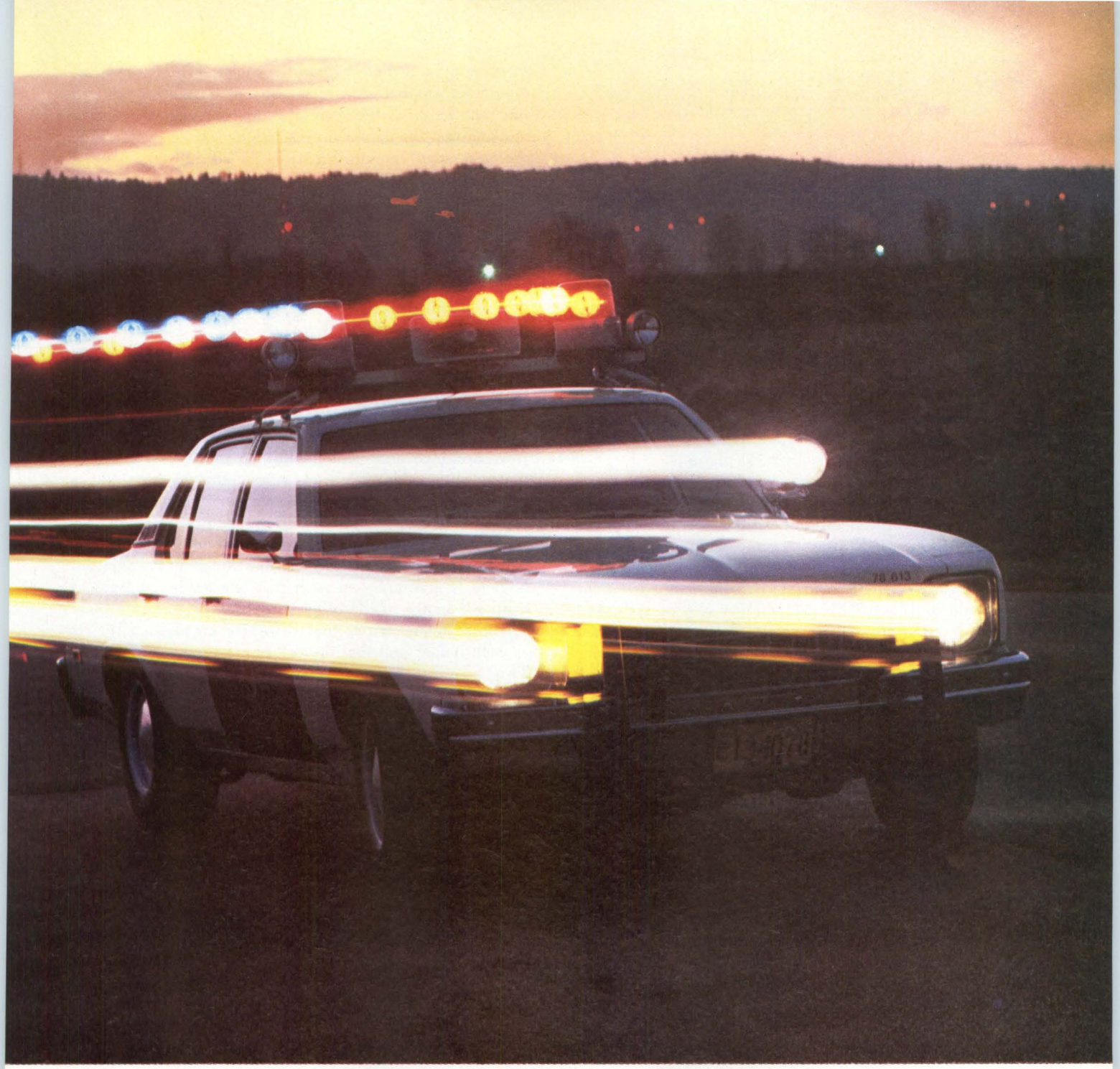
Boeing Computer Services has found that our minis are cost effective and can handle the job efficiently and with real-time speed.

The Sperry Univac minis used in Portland are just part of our complete family of minis. One and all of them are supported by our powerful software.

If you have a system application, we undoubtedly have a mini that's just right for it. Whether it be business data process-



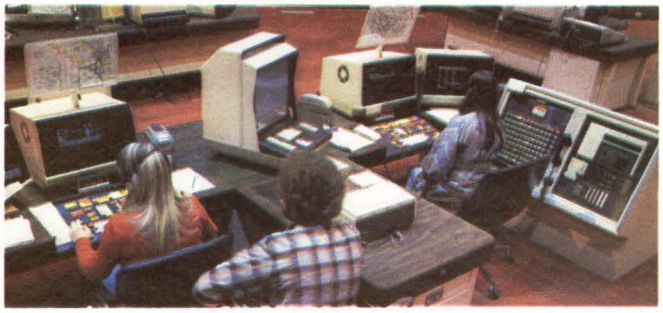
alarming things in Portland.

ing, scientific, instrument control, or data communications.

For more information, write to us at Sperry Univac Mini-Computer Operations, 2722 Michelson Drive, Irvine, California 92713. Or call (714) 833-2400, Ext. 536.

In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

We'd like to hear from you. Even if your system application isn't as arresting as the one in Portland.



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CIRCLE 35 ON INQUIRY CARD

are individually below the criteria for rejection, but which are grouped together, to be detected as cause for failure.

The number and types of light-to-dark and dark-to-light diode transitions indicate the exact portion of the lens being scanned, as shown in Fig 3. Assigned codes are condition 01, lens not in view; condition 03, start end in view; condition 05, center in view, no defect; condition 07, center in view with defect; condition 03, finish end in view; and condition 01, lens no longer in view. Information in one scan is compared to that in the next scan, and the microcomputer is provided information to enable it to initiate signal processing information for ΔD, ΔS, and other calculations.

As an example of the test procedures, when there is no lens in the field of view (condition 01), the microcomputer must first determine if there is information from the previous lens awaiting processing. A fail queue is established for each lens defect and is completed after the last measurement is made (when the lens passes out of the field of view). This information is processed, and the lens is either passed or rejected. If a defect is detected that meets the criteria for failure, the microcomputer turns on the air to reject the lens, and the system is ready for new information.

A microcomputer board contains the 8080 microprocessor, control and clock functions, and RAM. The operating program is permanently stored in 3k bytes of P/ROM. A 512-byte RAM is used for temporary storage during the data processing operation while the interrupt controller is accepting various input signals. Camera data enter the two 256-byte ping-pong RAMs which are multiplexed to enable the processor to operate on the data from one scan line while the other memory receives data from another scan line. Thus, as data are being fed into one bank of the RAM, the microprocessor retrieves and analyzes the data contained in the second bank. Then, the next scan line information is fed into the second bank while the microprocessor retrieves and analyzes the data contained in the first bank.

Inspection of Tablet Packaging

This scanner system is designed for continuous duty on an automatic tablet packaging machine where four rows of seven tablets each are deposited into a transparent holder that measures 2.3 x 3.3″ (5.9 x 8.3 cm). Two holders are indexed through the machine simultaneously in a side-by-side configuration. One holder is displaced from the other by 0.15″ (0.39 cm) in the direction of travel. The index motion is equal to 4″ (10.4 cm). One row of tablets is orange in color, while the other three rows are blue and white, with the tablets arranged so that a white tablet is always surrounded by blue tablets in both X and Y axes, and vice versa, with only one overall arrangement being correct. The orange tablets are smaller in diameter than the blue and white tablets, which are virtually the same size. Filling of two adjacent holders is accomplished such that one holder appears as a mirror image of the other.

The scanner verifies that there are no missing tablets in each holder and that the colors are properly arranged. Two adjacent holders passing these criteria are then permitted through the processor where the bottoms are sealed with an aluminum color foil and the holders are subsequently trimmed from the carrier strip into individual packages. Maximum machine index rate is 60 steps (120 packages)/min.

The scanner consists of a camera—with a 512-element photodiode array—and a light source in an integral unit, and a remote, microcomputer-based electronic controller (Fig 4). The camera lens forms an image of the tablets

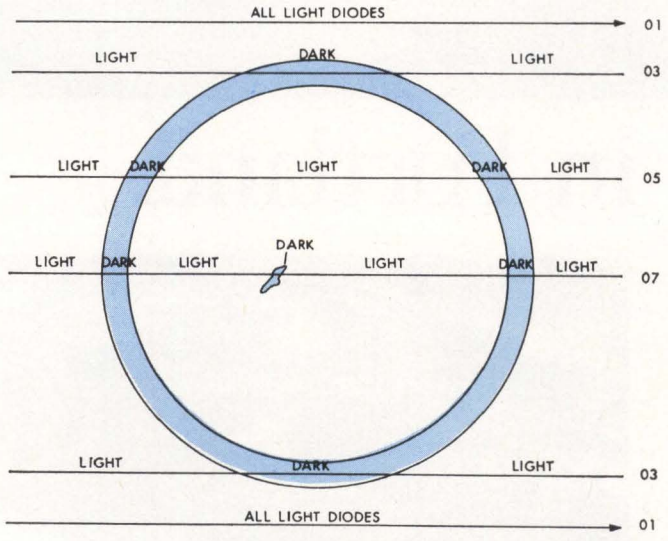

Fig 3 Transition conditions and codes assigned for lens test system. Information for each scan is processed by microcomputer to determine ΔD and ΔS of Fig 2. Dark spot (defect) is located by comparison of information from one scan to that of next

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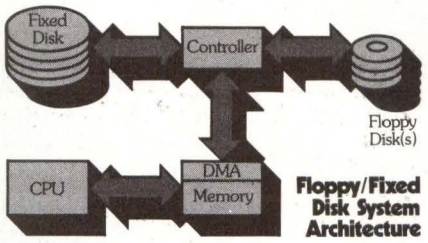

Floppy/Fixed Disk System Architecture

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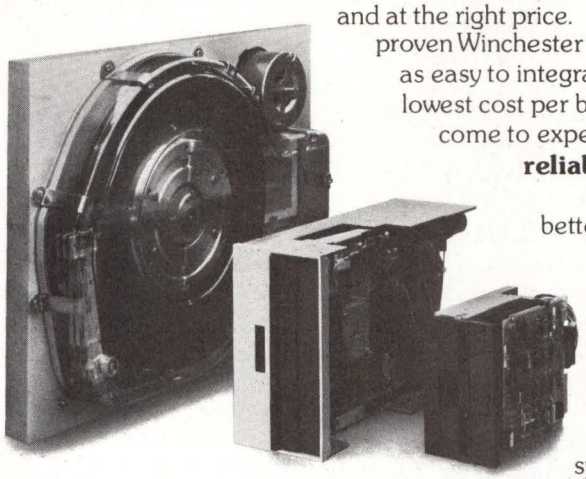

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on the photodiode array through a 0.125″ (0.318-cm) plexiglass window that covers the tablets. The photodiode array is scanned electronically to produce a train of analog electrical pulses, each having an amplitude proportional to the light intensity focused on the corresponding photodiode.

Tablets are front lighted as they pass under the camera's field of view to enable color discrimination (amplitude differences) between the blue and white tablets. However, because of the size difference of the orange tablet, absolute contrast difference is not important for its identification.

The presence of tablets results in reflected light to the camera. If the light is above a predetermined threshold level, as sensed by a photodiode, a digital 1 pulse is generated by the adjoining circuits. The absence of light above this threshold level results in a digital 0 pulse. As a result, a train of pulses is generated from the photodiodes in the linear array.

Groups of light pulses (1s) constitute tablet groupings. Dark pulses (0s) between tablets constitute the space or distance between tablets. Therefore, size of any tablet is determined by a continuous light diode count and the space between two tablets is determined by a continuous dark diode count. These counts are translated into size and distance. The counts are multiplied by the diode centers (2 mils), times the magnification factor (5) to give a size of 10 mils/count. For example, a count of 20 means the size or diameter of the tablet is 200 mils.

Array scanning is at a high rate, enabling many measurements to be taken on a row of tablets to gain the best accuracy. Ideally, one of the many scans passes through the true center of the tablets to give the largest counts consistent with the actual tablet diameter. When these counts are compared to other tablet counts on a relative basis they give arrangement according to size. Orange tablets are in cavities at the outside end of packages and are approximately 15% smaller than the blue and white ones. Thus, counts for these tablets must, of necessity, be less than the others or a misarrangement error results.

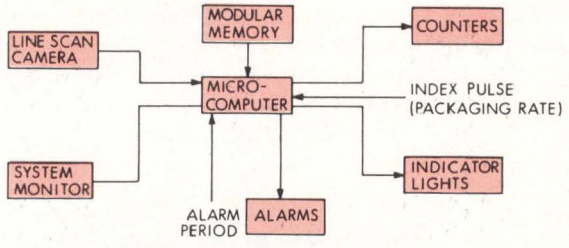

Fig 4 Tablet packaging inspection system. Camera views two lines of transparent holders, each containing four rows of tablets. One row contains all orange tablets while other three rows contain blue and white tablets with tablets arranged so that a white tablet is always surrounded by blue tablets in both X and Y axes, and vice versa. System must discriminate between colors of blue and white tablets but only check size of orange tablets since they are smaller

Video amplitude differences are used to distinguish blue from white tablets. Red and infrared rejection filters reduce energy levels of blue tablets over the white tablets. Amplitude is sampled in the middle of each tablet and converted into 1 of 16 digital gray levels. These gray levels offer a uniform change from black to white in the color spectrum, enabling the system to separate blue from white in a digital manner.

Determination that a tablet is missing is based upon "space" counts between tablets. Actual distance between tablets is a count of dark pulses (0s). Constants stored in the microcomputer memory represent the maximum distance in pulse counts the system will allow before declaring a missing condition.

A cam operated switching mechanism synchronized to the machine motion initiates and terminates the scanner data acquisition period. The microcomputer develops internal timing signals until the required number of tablets are sensed or timeout of the acquisition occurs.

Video signals from the camera sent to the electronic controller on a continuous uninterrupted basis are digitized into 4-bit binary words and are processed in accordance with the timing signals. These digital data are interrogated for the critical inspection parameters (ie, size of tablet, color of tablet, arrangement of blue and white tablets, and number of tablets). Holders which do not pass these criteria initiate totalizing counters and alarm output signals. Three 6-digit electromechanical totalizing counters on the electronic controller indicate total holders inspected, total rejects for missing tablets, and total rejects for misarranged tablets.

The controller contains two circuit cards: analog and microcomputer. In addition to its main function of converting tablet colors into gray levels, the analog card has all of the camera's I/O line receivers and drivers, plus clock and counter circuitry necessary for external camera control and tablet data formatting. It contains logic for driving the electromechanical counters, solid-state relays, lamp indicators, system status, and error status functions as well as related timing and control logic circuits.

Microprocessor, three P/ROMs, four RAMs, and supporting logic are on the microcomputer card. This card also contains a programmable interrupt control unit which is used to interrupt normal processing of the microprocessor during the period when tablet holders are out of the camera's field of view. I/O control on this card covers 10 input functions, 5 output functions, and 5 reset functions. Reset is a variation on the input (read) function, sharing common circuitry to accomplish the same end without including additional hardware.

General Technical Description

All scan cameras in the systems described here are based on use of a solid-state image sensor (Fig 5). Such sensors contain a shift register that is driven by a clock,

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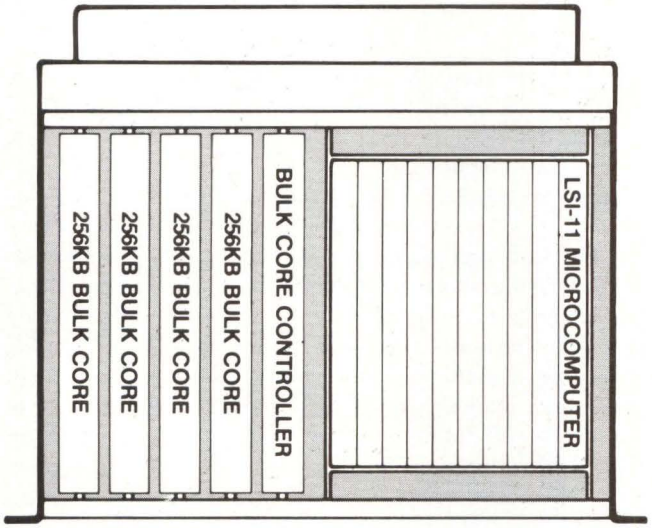

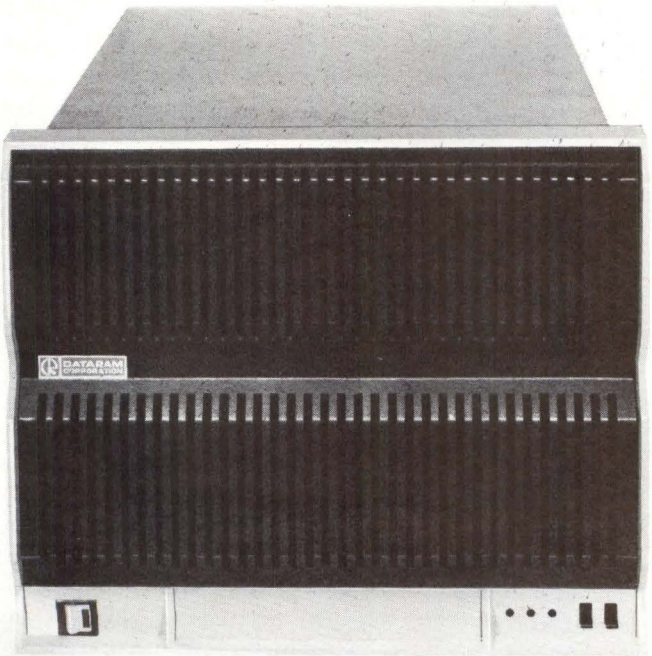

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Dataram manufactures the core and semiconductor ADD-INs for the LSI-11, which can be used with the BCM-1.

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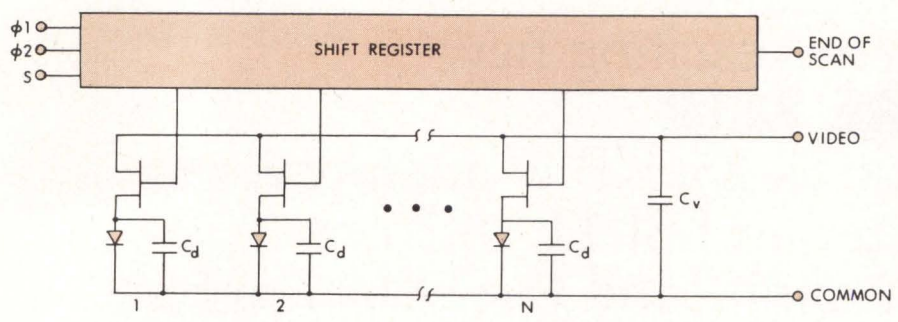

Fig 5 Simplified schematic diagram of typical image sensor. Clock drives shift register, with each scan initiated by start pulse. Video signal is train of charge pulses from individual capacitors, each proportional in magnitude to light intensity falling on corresponding photodiode

with each scan initiated by a start pulse. That pulse loads a bit which is clocked through the register, successively opening and closing switches and connecting each photodiode, in turn, to a video line. As each photodiode is accessed, it capacitance is charged to the potential of the video line and is left open-circuited until the next scan. During the interval between scans, the capacitor is discharged by an amount equal to the instantaneous photocurrent in the diode, integrated over the line scan. Each time a diode is sampled, this integrated charge loss must be replaced through the video line. The resulting video signal is a train of charge pulses, each proportional in magnitude to the light intensity falling on the corresponding photodiode. Clock and start requirements for matrix arrays are similar to those for linear arrays; output is on a single video line.

Single linear photodiode arrays contain from 64 to 2048 diodes in a single line with center to center spacing as small as 15 μm; 2-dimensional matrix arrays are in 32 x 32, 50 x 50, and 100 x 100 element configurations with 60-μm spacing. Clock and start requirements are the same for both. Output is a single video line.

Depending on working distance and choice of lens, the camera can look at any field of view from a fraction of an inch up to many feet. This field of view is imaged by the lens onto the photodiode array which is scanned electronically to produce a train of analog electrical pulses each having an amplitude proportional to the light intensity on the corresponding photodiode. These pulses are then compared to a preset threshold level to produce a train of binary pulses—logical 0 for light below threshold (black) and logical 1 for light levels above threshold (white).

Pulses before or after a black-white transition can be electronically counted to determine the position of an edge, or the pulses between two transitions can be counted to measure a diameter. Accuracy of these measurements is determined by the field of view and the number of photodiodes in the array. For example with a 5″ (12.7-cm) field of view and a 512-element array, size differences of approximately 0.01″ (0.254 mm) could be resolved. With a 0.5″ (1.27-cm) field of view, 0.001″ (0.025 mm) could be resolved.

Time required to scan a line can be varied electronically from 0.04 s to N x 10^{-6} s, where N is the number of diodes in the array. As with a photographic camera, the longer the exposure time (line scan time) the less light intensity is required to produce an image. However, the shorter the exposure time, the less likely the image is to be blurred by motion of the object being scanned. In most industrial applications it is possible to choose a scan rate slow enough for reasonable light levels and yet fast enough to produce an accurate measurement with minimum effects due to motion or vibration of the object.

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DC&AS BRIEFS

Analog Input System Extends Computer's Sensor-Based I/O Capability

A modular user-oriented signal conversion subsystem for interfacing the company's Solution series digital computers to analog signals has been introduced by General Automation, 1055 S East St, Anaheim, CA 92803. WRAIS (wide range analog input system) accommodates up to 512 analog inputs, ranging from ±5 mV to ±10 V full scale in groups of 16 high or low level channels, using relay or FET multiplexers with signal conditioning and terminator modules. The basic input system includes a programmable gain amplifier module with gains of 1 to 2048 in 12 binary steps, a 14-bit (including sign) analog to digital conversion module with sample and hold, GA-16 interface modules that control the flow of data over programmed I/O or high speed direct memory access buses of the computer, a precision programmable voltage calibration module, and an operator oriented interactive control panel.

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The low-rental rates on Mini Bee 2 will make you happy if you need a TTY-compatible terminal with cursor control and a detachable keyboard. Beehive's Mini Bee 2 is a stand-alone, operator/computer accessible remote display terminal with a detachable keyboard. You use Mini Bee 2 to transmit and receive data serially through an RS232C interface at any of several preselected transmission rates to a maximum of 9600 baud. Mini Bee 2 has a 12" rectangular monitor which displays 25 lines with 80 characters per line. It has a total page memory of 2000 characters, and each character is generated from a 5x7 dot matrix with two dot spacing between adjoining characters. Communications mode can be full duplex, half duplex, 10 or 11-bit asynchronous word. Mini Bee 2 also features character-by-character transmission, an escape sequence mode for unique CRT functions, and an erase mode. It's also available off-the-shelf from REI immediately.

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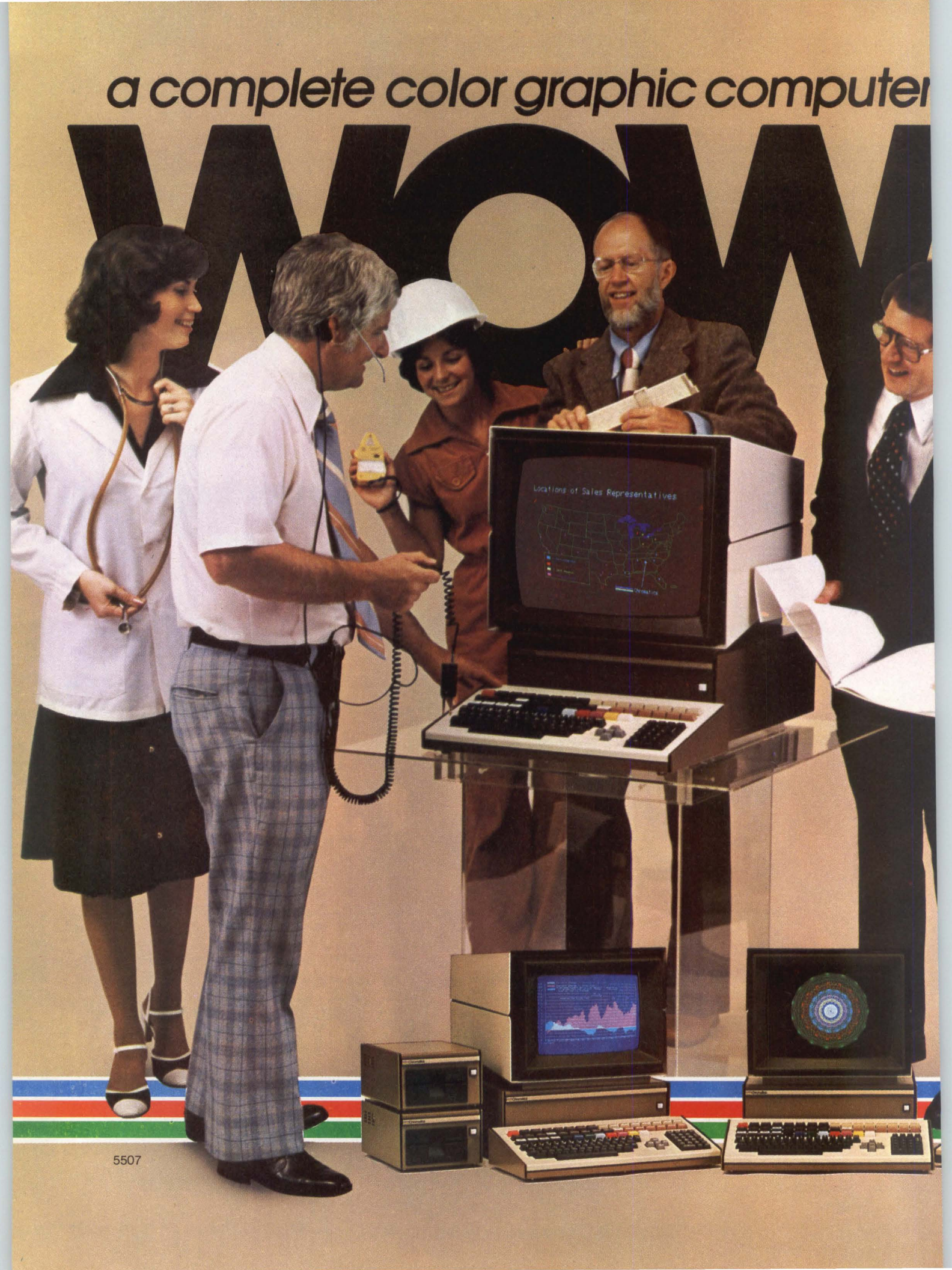
CIRCLE 38 ON INQUIRY CARD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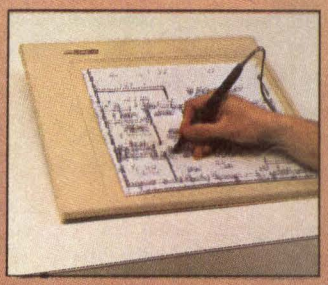

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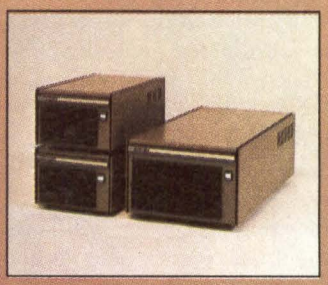

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CIRCLE 39 ON INQUIRY CARD

Surveillance and Ramp Monitoring System Added to City Traffic Management Plan

Under contract to the Minnesota Department of Transportation, Honeywell Traffic Management Div, Honeywell Plaza, Minneapolis, MN 55408 has begun installation of a minicomputer based traffic surveillance and ramp metering system on Interstate 694 in Minneapolis. The traffic management system, scheduled for completion later this year, will extend about 3 mi (5 km) to Highway 169. It will use a Honeywell Level 6/43 minicomputer to monitor traffic volume and speed and control the ramp meter signals and changeable message signs from the downtown traffic management center, and will be linked into the state's downtown traffic management center of monitoring and operation.

A microprocessor based local controller will provide local coordinated control of the I-694 entrance ramps if the link to the downtown computer is lost temporarily. This controller will collect and process information from loop detectors installed in the roadbed to monitor traffic volumes and flow and pass the information to the computer.

The minicomputer will provide overall supervision of the I-694 system and exchange traffic data with the current Honeywell computer for Interstate 35W as well as another control system on Highway 169 to coordinate traffic. Two color TV monitors will graphically map actual traffic conditions on I-694 to provide immediate indication of traffic problems to the state's traffic management personnel. In addition, the system will include master control of nearby intersections. Some added benefits that are anticipated include a reduction in air pollution, improved gas mileage for motorists, reduced accidents and congestion on I-694, and an improvement in general driving conditions on the freeway.

Circle 162 on Inquiry Card

Microcomputer and Language Developed for Control Applications

A single-board programmable microcomputer that provides high level programming of industrial and laboratory control applications, the Basic Controller™ allows the user to operate both computer and external devices it controls with a BASIC language called ZIBL™ that was written specifically for control applications. Both computer and language were developed by Dynabyte, Inc, 4020 Fabian, Palo Alto, CA 94303.

Onboard computer hardware includes a 2.5-MHz Z80 microprocessor, 32 each individually memory-mapped flag outputs and sense inputs, 8 relays, 8 LEDs, 2 RS-232 serial I/O ports, 1 each parallel input and output port, a cassette interface, 64 x 16 video I/O, keyboard input port, up to 4k of EPROM with programming capability, and up to 16k RAM (4k included). File structures allow multiple programs written in ZIBL to reside concurrently in RAM. Each program may be individually loaded, renamed, or run. Any program may access another program as though it were a subroutine, while retaining its own line numbers and variables.

ZIBL was designed to allow high level programming of control applications. It combines most of the capabilities commonly found in small BASICs as well as a number of unique features suited to control applications. It uses triple precision (24-bit) integer arithmetic in order to retain the high execution speed required by realtime control situations. This large dynamic range also allows scaling and rounding, if so desired. Interaction with the microcomputer is through the user's keyboard and video monitor that attaches to the printed circuit board.

Circle 163 on Inquiry Card

High Level Language Eases Process Control Programming

Wyle Laboratories/Computer Products, 3200 Magruder Blvd, Hampton, VA 23666 has released its latest version of process control BASIC (PCB), a high level language used in support of the company's μP industrial control microcomputer. PCB allows for scanning analog and digital inputs, processing control algorithms, and outputting analog or digital control signals with straightforward, English language statements. According to the company, the control engineer is freed from detailed machine programming and can make online changes quickly and easily.

Circle 164 on Inquiry Card

Hierarchical Computer Network Controls Manufacturing Plant

A 3-level hierarchical computer control system set up by Siemens AG in one of its manufacturing facilities in Amberg, West Germany is said to have achieved up to 10% improvement in machine utilization during a trial operation. The facility manufactures, stores, and distributes about 3000 different switchgear and control devices. Each year about 500,000 items are processed, in both large and short run quantities, with about 75% for special customer requirements.

At the highest level of the hierarchy is a Siemens 4004/150 central computer which manages data for the entire plant. Control of workshop and warehouse operations takes place at the middle level, which consists of two Siemens 330 process computers—each with 64k words of core memory backed by a 50M-byte disc drive. These "master" computers are linked in a resource sharing network. One computer monitors functions and preassembly while the other controls and manages the warehouse and monitors final assembly operations. If either computer fails, its peripherals can be switched to the other.

As many as 14 Siemens 310 terminal computers serve as the lowest level of the hierarchy. Distributed throughout the production area, these computers manage input masks, perform formal tests, and buffer inputs from terminals at the machines. □

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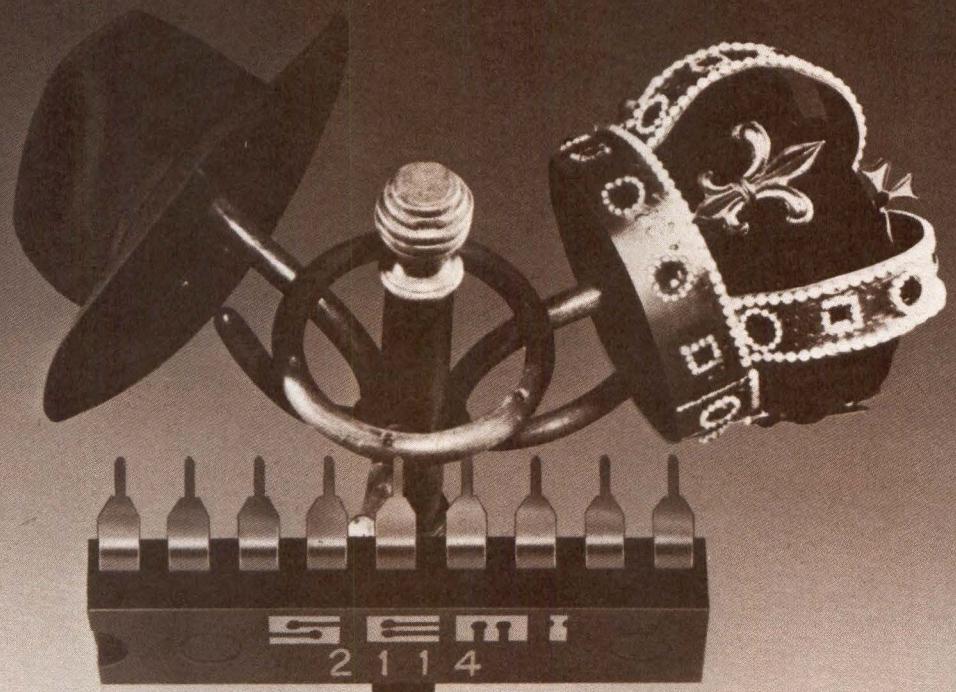
The 2114. It's old hat to us



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ISA/78 and JACC

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October 15-19

This year, for the first time, the Instrument Society of America is conducting its International Instrumentation-Automation Conference and Exhibit (ISA/78) in conjunction with the Joint Automatic Control Conference (JACC), an annual meeting sponsored by the American Automatic Control Council. ISA/78 officially begins at 10:30 am on Monday, October 16 with delivery of the keynote address by Willard J. Rockwell, Jr, chairman of the board, Rockwell International Corp, and runs through Wednesday. JACC begins at 9:00 am on Wednesday with a keynote address presented by Dr Harold Chestnut, a consultant for General Electric Co, and continues through 4:30 pm on Friday.

ISA/78 program chairman Orville P. Lovett, E.I. DuPont deNemours & Co Inc, and JACC chairman Dr Chun Cho, Fisher Controls Co, have organized a series of over 200 technical papers and presentations dealing with fundamental concepts, basic theory, current technology, and new applications and procedures in the instrumentation and control systems industry. Clinics, tutorials, short courses, and panels presented by authorities in industry, science, and education evolve around the theme of "Productivity Through Application of Theory." In addition to the technical program, short courses will be offered to provide practicing engineers and technicians with both fundamental and up-to-date knowledge of instrumentation and control systems.

Except for keynote addresses, ISA/78 conference hours will be 2:30-5 pm on Monday; and 10 am-12:30 pm and 2:30-5 pm on Tuesday and Wednesday. JACC conference hours will be 2:30-5 pm on Wednesday, 9 am-12 noon and 2-5 pm on Thursday, and 9 am-12 noon and 1:30-4:30 pm on Friday. On Wednesday some of the ISA/78 sessions will be geared toward JACC interest areas; JACC registrants may attend those afternoon sessions free of charge.

A 4-day exhibit, with displays from over 300 companies, will begin at noon Monday. Exhibit hours are noon to 6 pm on Monday, 9 am to 6 pm on Tuesday and Wednesday, and 9 am to 5 pm on Thursday.

Special Activities

The ISA President's reception will be held on Sunday, October 15, from 4:30-6 pm at the Sheraton Hotel. An important social event during this joint conference will be held at the Franklin Institute Science Museum and Planetarium on Wednesday at 6:30 pm. Exhibits will cover each floor of the Institute and the Mummers Band will entertain. Fee for that event will be $12.50 per person.

This year's ISA honors and awards luncheon will occur at 12:30 pm on Tuesday at the Hilton Hotel. The JACC awards luncheon will follow on Thursday at 12:30 pm in the Upper Egyptian gallery of the University of Pennsylvania's Museum.

Registration

Separate or joint registrations are available for ISA/78 and JACC.

	Member	Nonmember
3-day ISA Conference and Exhibit	$40	$60
1-day ISA Conference and Exhibit	20	30
3-day JACC	85	90
5-day ISA/JACC	100	115

JACC registration includes JACC Proceedings, admittance to Wednesday afternoon sessions of ISA/78, and admittance to the ISA exhibit. ISA Proceedings will be available at $75 ($60 for ISA members).

The following excerpts from the ISA/78 and JACC technical programs are necessarily limited to information available at press time. For further information on the conferences and associated events, write to the Instrument Society of America, 400 Stanwix St, Pittsburgh, PA 15222 or call (412) 281-3171.

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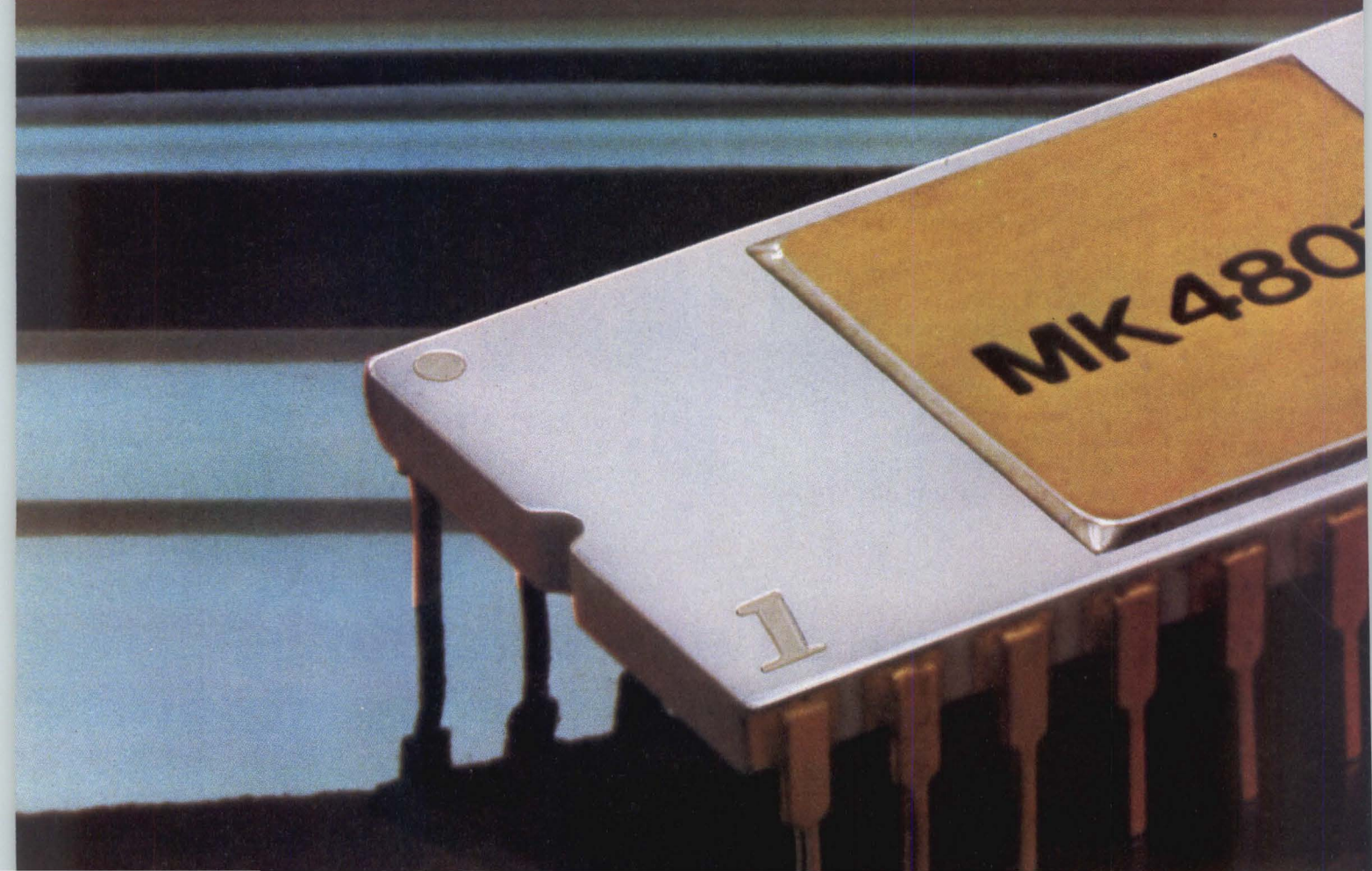
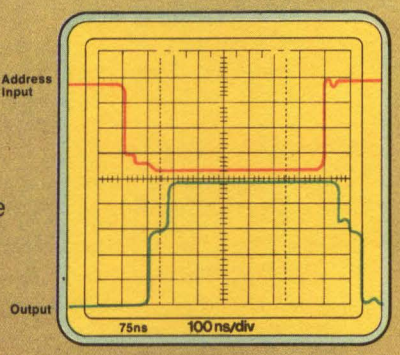
CIRCLE 41 ON INQUIRY CARD

Move over Bipolar.

Mostek's 8K static RAM is moving in!



The new MK4801 8K static RAM advances Mostek's memory technology leadership again. You can now replace bipolar technology with MOS. The advantages are significant—increased system density, reduced system cost and lower power improving system reliability.

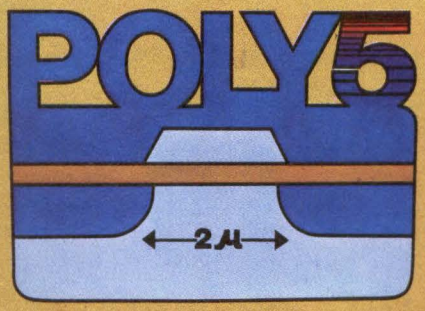


Fast access—55ns! With sub-100 ns access/cycle times the MK4801 family is ideal for wide-word cache, buffer and telecommunication applications. The 1Kx8 organization permits 1K increments in density optimizing memory size vs.cost tradeoffs. Requiring a single +5 volt power supply, the MK4801 is totally TTL compatible and as easy to use as bipolar memory.

Other features include a fast CS function (50% of address access) allowing memory expansion without impacting system access time. A fast OE, also 50% of access time, permits data interleaving and a flexible latch allows optional latching of CS and address. The 4801 uses Address Activated™ interface to permit synchronous or asynchronous operation by combining the benefits of Mostek's Edge-Activated™ concept and fully static operation. Mostek's MK4801 static RAM series includes the MK4801-55 (55ns access/cycle time), MK4801-70 (70ns access/cycle time), and the MK4801-90 (90ns access/cycle time).

The technology of the future is here today. Mostek's next generation process, Scaled Poly 5™, is accomplished through a double polysilicon process in which all physical dimensions of the transistor geometry are reduced, as are substrate doping concentrations and operating voltages. The results are next generation products available today.

The MK4801 is just the first of many Scaled Poly 5 products from Mostek. A die size of just 18,900 mils², sub-100ns access and 5-volt only operation are typical of the features you can



expect from future Scaled Poly 5 products. Production volumes of the MK4801 are scheduled for the fourth quarter. Start designing your system now. For more information, contact Mostek at 1215 W. Crosby Road, Carrollton, Texas 75006; Telephone (214) 242-0444. In Europe, contact Mostek Brussels; Telephone (32) 02/660.25.68.66013.

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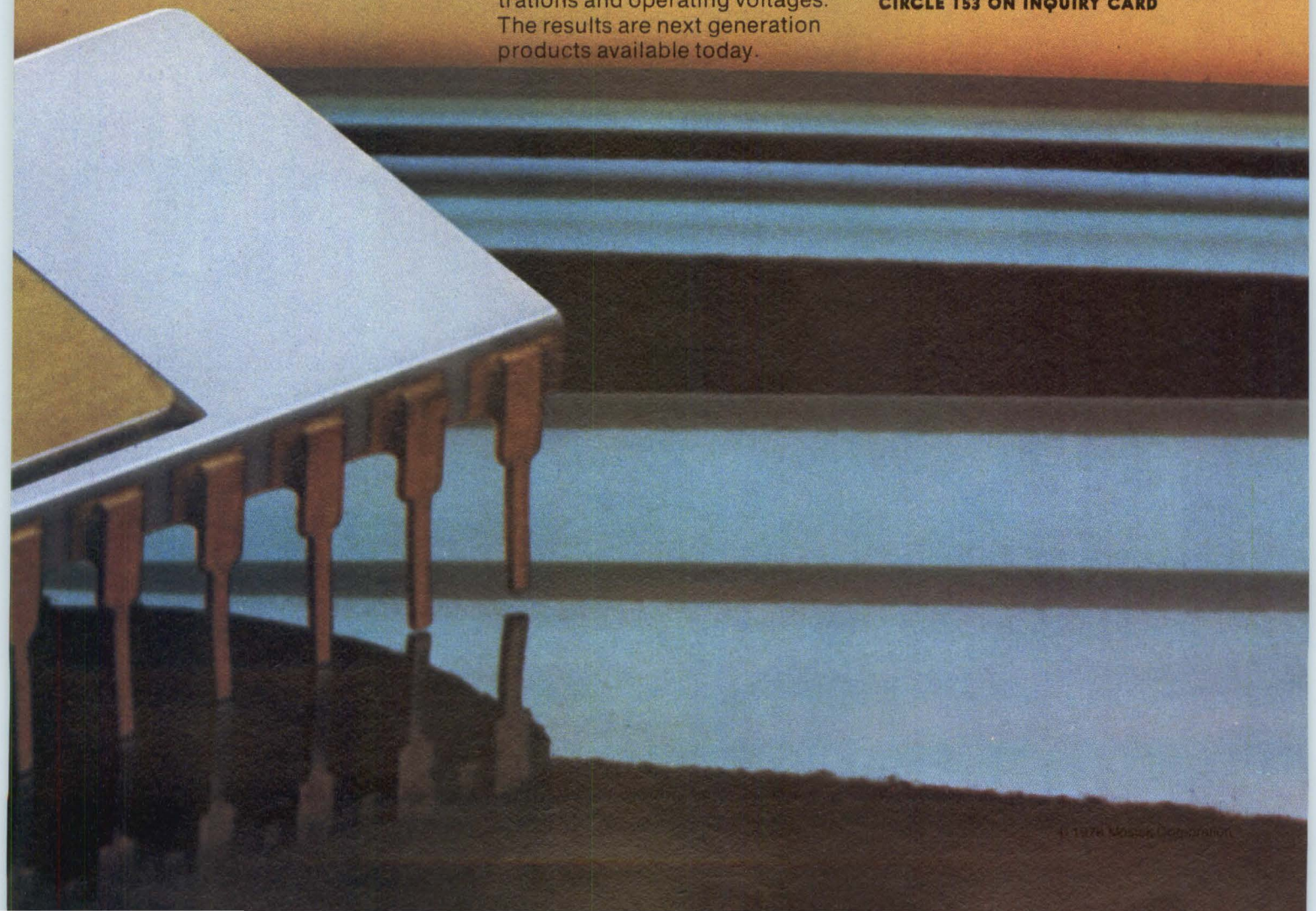

Professional Program Excerpts

Monday Afternoon

Session 2 **2:30-5 pm**

Man-Machine Interfaces

Chairman: G. F. Barnes, Monsanto Co

"International Purdue Workshop's Man-Machine Communications Committee Activity," R. F. Carroll, B. F. Goodrich

"Electronic Artist Palettes For Multicolor Process Displays," R. A. Williamson, Jr, Metromation, Inc

"Using a Color CRT With Light Pen for an Operator Console," R. B. Zey, Herco

"Using Color CRTs for Man-Machine Communication," J. Hedrick and E. Pageler, Fisher Controls Co

"Voice—A Solution to the Data Entry Bottleneck," E. J. Simmons, Jr, Threshold Technology Inc

Session 3 **2:30-5 pm**
(Repeated in Session 67)

Clinic: IEEE-488 Workshop

Chairmen: N. Kuhn and J. G. Evans, Hewlett-Packard Co

The objective of this clinic is threefold. First of all, the clinic will give a status report on IEEE-488, including where it fits in the system picture, past difficulties it eliminates, and how it operates. Customer case histories will illustrate specific measurement problems that need to be solved and why the IEEE-488 approach was chosen along with subsequent financial return. In addition, workshops will demonstrate the assembly of systems such as desktop computers and minicomputers as controllers.

Session 4 **2:30-5 pm**
(Repeated in Session 51)

Clinic: Microcomputers for Measurement And Process Control

Chairmen: J. Drakeford and P. A. Anderson, Intel Corp

Differences between minicomputer and microcomputer control solutions will be identified and highlighted in this introduction to microcomputers and their applicability to performing process measurement and control. Microcomputer component organization, board and system solutions using microcomputers, software development process, and availability will be outlined. Guidelines for successful microcomputer field implementation and process control applications that have been implemented with microcomputers will also be discussed.

Session 5 **2:30-5 pm**

Panel: Programmable Controllers For Process Control

Chairman: C. H. McClure

"Programmable Controller Utilization in an Online Mixing System," M. E. Nace, Honeywell, Inc

"Batch Control Utilizing a PC/Computer System," H. Derrick, Industrial Solid State Controls, Inc

"Instrumentation for Oxygen/Opacity Coal Combustion Control," R. E. Downey, Delco Remy

"Programmable Controllers in Process Control," L. W. Long, Allen-Bradley Co

"A User's View of the Present and Future Requirements of Programmable Controller Systems," R. E. Cook, The Foxboro Co

"The Future for Programmable Controllers," R. A. Whitehouse, Modicon

Session 11 **2:30-5 pm**

Digital Telemetry Applications

Chairman: Z. Taqvi, Lockheed Electronics Co, Inc

"Data Compression and the Use of Compressed Data," R. Baker, EMR-Telemetry

"Industrial PCM Data Acquisition System," J. S. Norton, EMR-Telemetry

"Distributed Control for Houston's MGD Wastewater Treatment Plant," R. R. Page, Lockwood, Andrews, and Newnam, Inc

Session 12 **2:30-5 pm**

Panel: Benefits of Computers To the Textile Industry

Chairman: W. L. Huff, Taylor Instrument Co

Moderator: K. Wilkinson, Taylor Instrument Inc

Panelists: J. Fortunato and E. Ford, Reliance Electric Co; and W. Huff, Taylor Instrument Co

"Benefits of Computers to Batch Control," J. Fortunato and E. Ford, Reliance Electric Co

"Benefits of Computers to Continuous Control," W. L. Huff, Jr, Taylor Instrument Co

Session 13 **2:30-5 pm**

Monitoring and Control of Water Treatment and Reclamation

Chairman: T. A. Gray, Systems Control Inc

Welcoming Remarks: C. Guarino, City of Philadelphia Water Commissioner

"Selection of a Digital Control System for the Parsons Avenue Water Plant," S. Barnes, Columbus, Ohio Div of Water; R. Graupmann, EMA Inc; and C. Moore, Alden E. Stilson and Assoc

"'Lucy' Nicholas Villes Microprocessor," G. A. Werenskjold, ACCO Bristol

"A Comparison of Control Methods for a Demineralized Water Treatment Plant," J. A. Martin and J. Price, Jr, Tennessee Valley Authority

"Three Generations of Water Systems Control," J. W. Garrett, Santa Clara Valley District

"Automated in Situ Water Quality Monitoring," K. Nishioka, NASA-Ames Research Ctr; and R. Brooks, The Boeing Co

Tuesday Morning

Session 15 **10 am-12:30 pm**

Software for Digital Control

Chairman: P. W. Palm, Hewlett-Packard Co

"Computer Control Software: Theory and Practice," D. Rosich, Hofstra University

"Computer vs Multiple Programmable Controllers," E. Long, R. Buschart, and J. W. Meeks, Monsanto Co

"FOXCAL—A Computer Applications Language for Pilot Plant and Research Laboratory Experiments Automation," P. A. Holst, The Foxboro Co

"Advanced Minicomputer Process Control Package Put Into a Standalone Microprocessor Based Multi-Loop Controller," K. Beoughter and R. Rammler, Powell Industries

"Computerized Process Control and Management Information in a Manufacturing Environment," S. Dickey, Hewlett-Packard Co

Session 16 **10 am-12:30 pm**
(Repeated in Session 52)

Clinic: How to Program Process Control Computers—Part I

Chairman: T. Montag, Fisher Controls Co

Class will focus on implementing process control on a computer. There will be a hardware overview, a discussion of the historical development of software, and an in-depth discussion on the use

Move over 2114s.
Mostek's 8K static RAM is moving in!

Double your system density by replacing two 2114s with Mostek's new MK 4118 8K static RAM. In addition, you gain significant improvements in speed, power, and design flexibility over older generation 2102 and 2114 static RAMs.

Organized as 1K X 8 bits, the MK 4118 is designed to interface directly with all present and future generation microprocessors. A Chip Select control is provided for easy memory expansion and decoding, and internal latches are available to latch the Address and Chip Select inputs, further simplifying system design. If the Latch function is not needed, it can be bypassed by connecting the Latch control input to +5V (the only power supply needed for the MK 4118). A fast Output Enable function (50% of address access) allows easy control of the data bus in all bus configurations.

MK4118 Family

	Access Time	Cycle Time
MK 4118-1	120 ns	120 ns
MK 4118-2	150 ns	150 ns
MK 4118-3	200 ns	200 ns
MK 4118-4	250 ns	250 ns

All inputs and outputs are TTL compatible, and the MK 4118 is pin compatible with standard 24-pin ROMs, PROMs, and EPROMs, such as the MK 2716.

Advanced circuit design and Mostek's Poly R™ process technology are combined to pack 8K bits of static RAM on a chip comparable in size to 4K static RAMs. Performance, reliability, flexibility, compatibility. The 4118 is the obvious choice. For information contact Mostek, 1215 West Crosby Road, Carrollton, TX. 75006. Telephone 214/242-0444. In Europe, contact Mostek, Brussels; Telephone (32) 02/660.25.68.66013.

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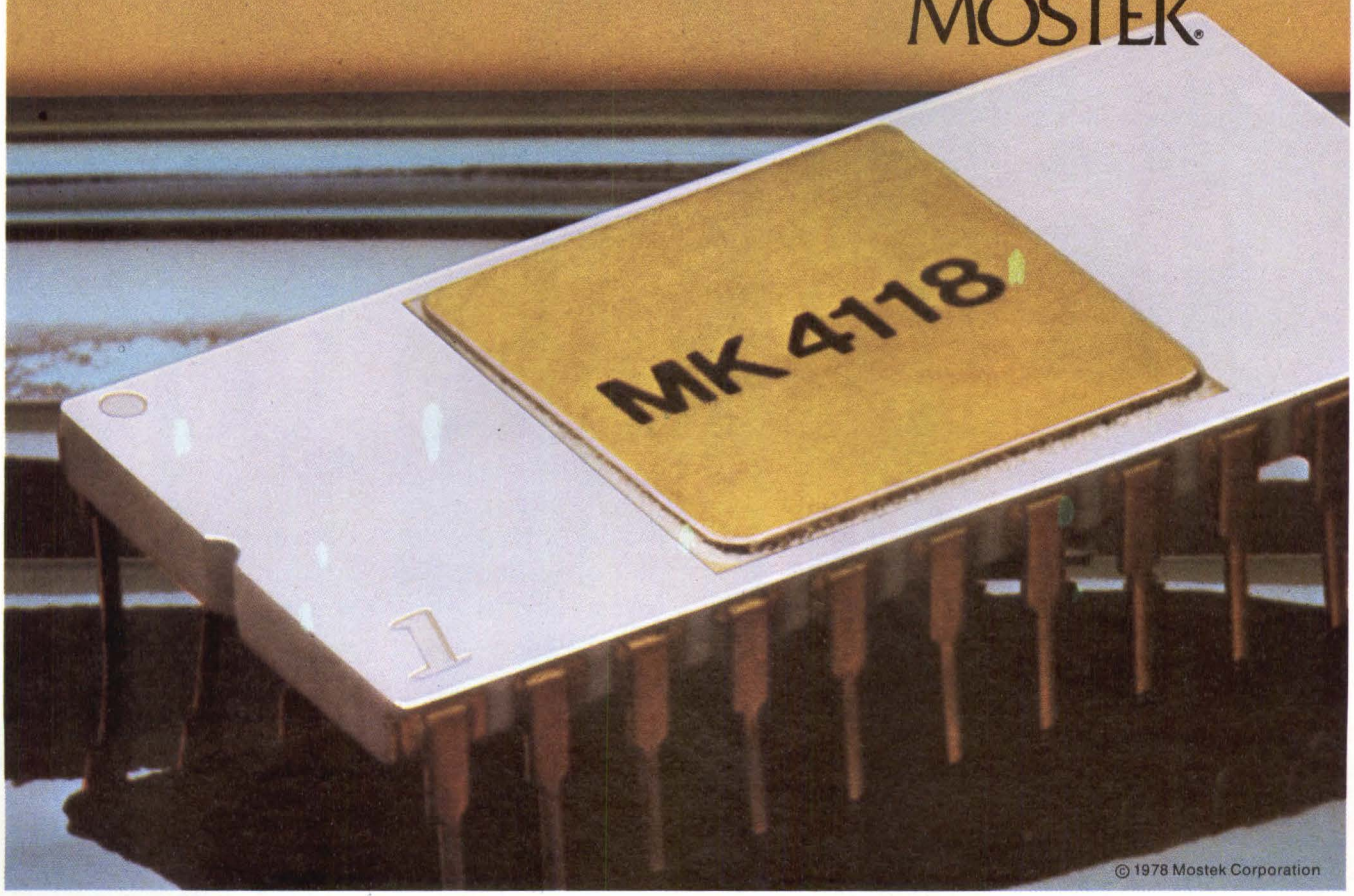

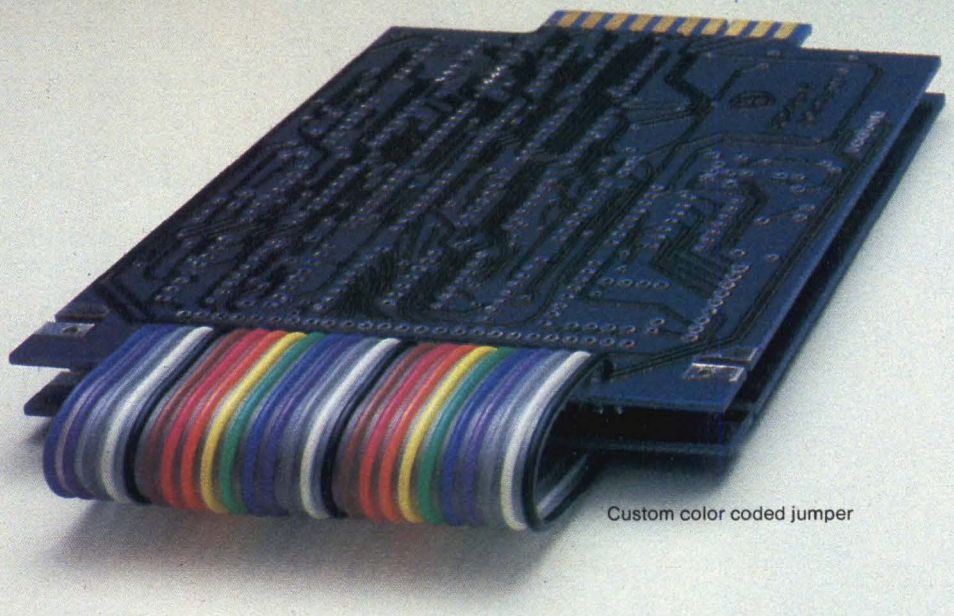

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of high level programming languages. One hour will be devoted to a hands-on workshop. Attendees will be able to operate a process simulator from an engineer's and an operator's console.

Session 17 **10 am-12:30 pm**
(Continued in Session 35; see Session 53 for Advanced Concepts)

Clinic: Programmable Logic Controllers—Basic Concepts—Part I

Chairman: R. A. Whitehouse, Modicon

Overview of programmable controllers, their history, general architecture, and applications will be presented with stress on new developments and capabilities. Basic programming will be demonstrated. The capabilities of all programmable controllers will be surveyed and units at the exhibits will be identified.

The Basic Clinic (Sessions 17 and 35) will discuss relay, timing, counting sequencing, and setpoint control. The Advance Course (Sessions 53 and 66) will cover analog control loops, data storage, advance programming, capabilities, and hierarchical system design.

Session 18 **10 am-12:30 pm**
(Continued in Session 36)

Clinic: Minicomputers for Data Acquisition and Control—Part I

Chairmen: W. Van Diehl and J. Gruneisen, Hewlett-Packard Co

Clinic will give an introduction to minicomputer hardware and programming. It will also include sensor I/O interface and distributed processing considerations. Course will outline history and development, minicomputer control, minicomputer price performance, interfacing common sensors to a measuring unit, local or remote choices, how to interface the measure unit, and levels of control distributed processing consideration.

Session 20 **10 am-12:30 pm**

Digital Control of the Microprocessor In Glass and Ceramics Manufacturing

Chairman: N. Patel, Forco-Glass Co

"Review of Process Control," J. F. Davis, Owens Corning Fiberglass

"Use of Quantitative Methods in the Glass Industry," M. J. Seiden, John-Manville Sales Corp

"Management Information Systems in the Glass Industry," R. Strong, Brockway Glass Co

Session 25 **10 am-12:30 pm**

Control Applications

Chairman: J. Gray, The Foxboro Co

"A Simplified Method of Process Control Loop Design," M. B. Rothstein, United Engineers & Constructors Inc

"A Multipurpose Override Selector for Analog Electronic Control Systems," W. S. Buzzard, Fischer & Porter Co

"A Unique Approach—Distributed Digital Process Control at the Control Valve," P. Traotman and F. Tasch, Xomox Corp

Session 30 **10 am-12:30 pm**

Measurement and Control of Municipal Wastewater Treatment

Chairman: B. B. Mishra

"Direct Digital Control of a Vacuum Filter," G. A. Mathes, EMA, Inc; and R. E. Rice, Metro Waste Control Commission, St. Paul, Minn

"Dynamic Model of Sedimentation Tank," S. Nogita and T. Ikeguchi, Hitachi Ltd; and R. Nagasaki, Tokyo Metropolitan Government

"Mathematical Models of Activated Sludge Process," S. Kato, Tokyo Metropolitan Government; M. Tanuma and K. Kashiwagi, Hitachi Ltd

"Schemes for the Control of the Activated Sludge Process via Digital Computer," S. B. Younkin and E. F. Ballotti, Greeley and Hansen; and C. F. Guarino, Philadelphia Water Dept

Tuesday Afternoon

Session 33 **2:30-5 pm**

Panel: Microcomputers for Process Control

Chairman: Y. Keiles, Honeywell Inc

Panelists: R. Rambler, Powell Industries Inc; A. Uyetani, Toshiba Corp; R. D. Hawkins, Naval Weapons Ctr; A. Finger, Analog Services; J. Stein, Stynetic Systems Inc; and J. Drakeford, Intel Corp

Session 34 **2:30-5 pm**
(Repeated in Session 65; Continuation of Session 16)

Clinic: How to Program Process Control Computers—Part II

Chairman: T. Montag, Fisher Controls Co

Session 35 **2:30-5 pm**
(Continuation of Session 17; See Session 66 for Advanced Concepts)

Clinic: Programmable Logic Controllers—Basic Concepts—Part II

Chairman: R. A. Whitehouse, Modicon

Session 36 **2:30-5 pm**
(Continuation of Session 18)

Clinic: Minicomputer Systems for Data Acquisition and Control—Part II

Chairmen: W. Van Diehl and J. Gruneisen, Hewlett-Packard Co

Session 38 **2:30-5 pm**

Microcomputer Applications in the Glass And Ceramics Industry

Chairman: J. P. Theisen, Midland Glass Co, Inc

"Simplified Mathematics of Converting a Glass Container Forehearth from Analog to Direct Digital Control," J. P. Theisen, Midland Glass Co, Inc

"What Type of Process Control Equipment Best Serves the Needs in the Batch House," C. E. Bennett and C. F. Lockert, Reliance Electric Co

"Computer Controlled Glass Forming—Past, Present, and Future," R. J. Japenga, Emhart Industries

"New Concepts in Burner Design," A. J. Syska, Wingersheek, Inc

Session 42 **2:30-5 pm**

Panel: Holography and Lasers

Chairman: R. Christenson, Iowa Illinois Gas and Electric Co

Panelists: S. Parnaf, Apollo Lasers; R. Anwyl, Eastman Kodak; M. Chang, New Port Research Corp; and R. Swartz, IBM Corp

Session 43 **2:30-5 pm**

Digital Control Applications

Chairman: E. T. Roland, Copeland & Roland Inc

"Save Energy and Prevent Pollution by Distributed Digital Control System," A. Uyetani, Toshiba Corp

"Characteristics of a Processor Based I/O System," G. Hoyle, Burr-Brown

"Computers and Sensors in Water Treatment," J. L. Francis and S. Barnes, Div of Water, City of Columbus

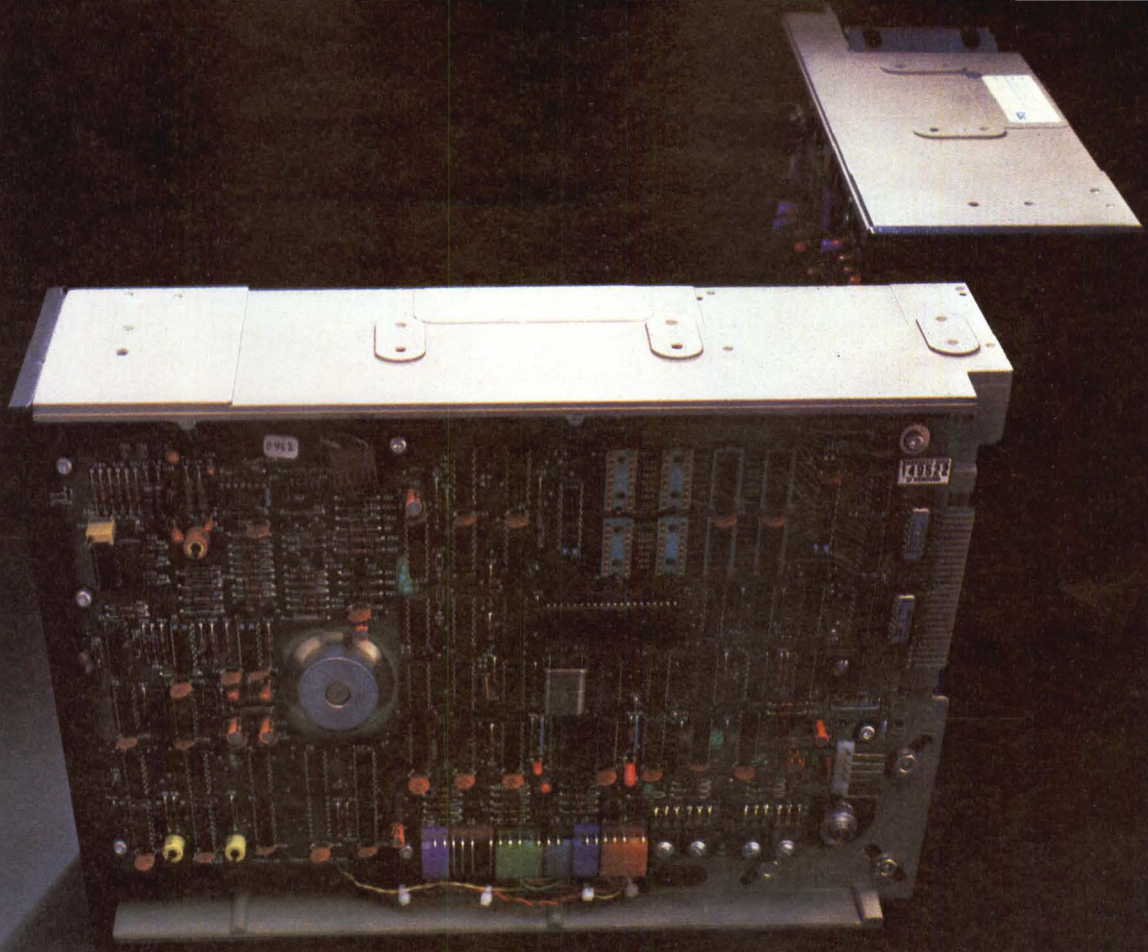
"Control Loops That Include the Operator—A New Approach to Interface Design," M. Beaverstock, The Foxboro Co

Session 45 **2:30-5 pm**

Clinic: Microprocessor Based Flow Computers

Chairmen: J. E. Moore and J. D. Perret, Waugh Control Corp

A description of applications and functions of newly developed microprocessor flow computers used to compute mass flow or



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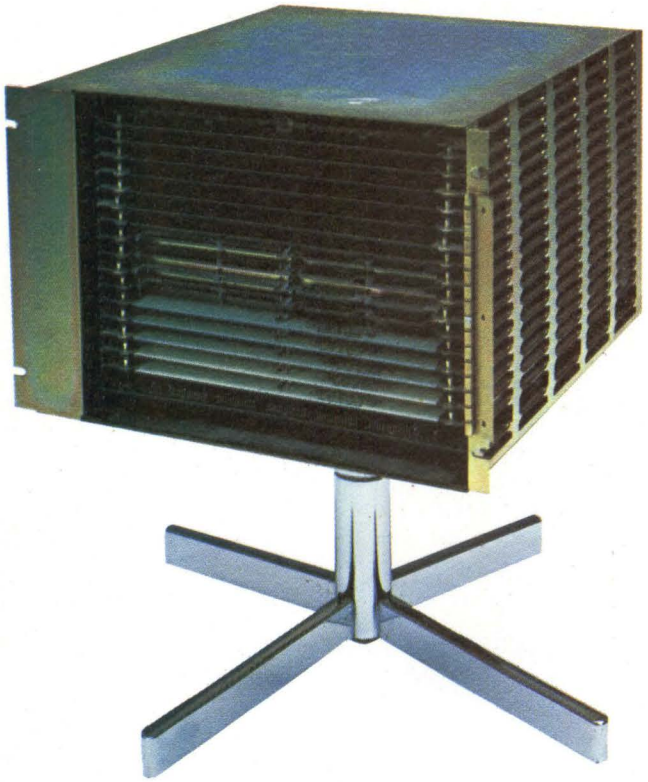

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volumetric flow corrected to a standard fluid temperature will be covered.

Wednesday Morning

Session 47 **10 am-12:30 pm**

Microprocessors and Thermographics—Selected Papers from the 24th Internat'l Instrumentation Symposium

Chairman: O. M. Friedrich, U of Texas at Austin

"Application of the Microprocessor to Surface Transportation Vehicle Testing," A. D'Agostini, Boeing Vertol Co

"Microprocessor Controlled EPROM Memory Programming," P. E. Riley and R. Chizmadia, Westinghouse Corp

"Thermographic Inspection," R. F. Friedman and H. Kaplan, Barnes Engineering

Session 48 **10 am-12:30 pm**

Advanced Control

Chairman: R. F. Sweeney, Villanova U

"Further Studies of PL Level Control," T. F. Cheung and W. L. Luyben, Lehigh U

"Ethylene Plant Computer Control—Czechoslovakia," B. M. Bergen and M. Asgarl, C-E Lummus

"Floating Supervisory Computer Control Algorithm," M. Manoff, Metromation; and J. A. Weaver, B. F. Goodrich Chemical Co

"Use of a Microprocessor Operated Terminal as a Process Controller," J. C. Finney and J. T. Brown, Chemstress Consultant Co; and G. L. Kramerich, Cleveland State U

"Smokeless Flare Control," J. Agar, Agar Instrumentation Inc

Session 50 **10 am-12:30 pm**

Distributive and Hierarchical Control Systems

Chairman: K. W. Goff, Leeds and Northrup Co

"Performance to Distributed System Architectures," J. D. Schoeffler, Cleveland State U

"Distributed Computer Control for Statfjord," F. C. Mears, Mobil Exploration Norway Inc

"An Industrial Application of Local Network Architecture," G. W. McClure and M. G. Gable, Ford Motor Co

Session 51 **10 am-12:30 pm**
(Repeat of Session 4)

Clinic: Microcomputers for Measurement And Control

Chairman: J. Drakeford and P. A. Anderson, Intel Corp

Session 52 **10 am-12:30 pm**
(Continued in Session 65; Repeat of Session 16)

Clinic: How to Program Process Control Computers—Part I

Chairman: T. Montag, Fisher Controls Co

Session 53 **10 am-12:30 pm**
(See Session 17 for Basic Concepts)

Clinic: Programmable Logic Controllers—Advanced Concepts—Part I

Chairman: R. A. Whitehouse, Modicon

This clinic will cover analog control loops, data storage, advanced programming capabilities, and hierarchical system design.

Session 54 **10 am-12:30 pm**

Process Computer Maintenance Seminar—Part I

Chairman: L. Marseilles, The Foxboro Co

This seminar will present a broad overview of process computer systems features, characteristics, and maintenance philosophies to people responsible for plant instrumentation maintenance. It will also provide a tutorial on process computer systems with functional descriptions of hardware, software, and maintenance aids.

Session 59 **10 am-12:30 pm**

Tutorial: Analog Data Converters And Microprocessor Interface

Chairman: L. Gardenhire, Pan Am

Speaker: P. Brokaw, Analog Devices Inc

This in-depth tutorial will cover the various data converters and how they are interfaced with microprocessors, including basic design ideas.

Session 60 **10 am-12:30 pm**

Panel: Experiences with Computer Control In Water and Wastewater Treatment

Chairman: A. W. Manning, SMA Inc

"Management of Technical Communication During Design," R. Werner, Washington Suburban Sanitary Commission

"Management of Staffing and Training," J. Nelson, Metro Denver Sewage Disposal District No. 1

"Management of Start-up, Testing, Acceptance, and Operational Transition," R. Skrentner, City of Detroit

"Management of System Maintenance," J. Almo, Metropolitan Minneapolis-St Paul Waste Control Commission

"Management of System Operation," P. Habrukowich, Ocean County Sewage Authority

Wednesday Afternoon

Session 61 **2:30-5 pm**

Minicomputers, Data Acquisition, and Control For Energy Systems—Selected Papers from The 24th Internat'l Instrumentation Sym

Chairman: O. M. Friedrich, U of Texas at Austin

"A Minicomputer Based Data Acquisition and Analysis System for Vertical Axis Wind Turbine Testing," B. Stiefeld and R. Tomlinson, Sandia Labs

"Solar Total Energy Control and Data Acquisition System," W. Shurtleff, Sandia Labs

"Master Control and Data System for the 5-MW Solar Thermal Test Facility," D. Darsey, Sandia Labs

Session 64 **2:30-5 pm**

Energy and Utility Conservation By Computer Control

Chairman: P. V. Bhat, Monsanto Co

"Microcomputer Applications for Electric Power System Control," G. T. Heydt and G. L. Viviani, Purdue U

"Energy Conservation Opportunities Through Use of a Computerized Building Management System," S. M. Zvolner, Johnson Controls, Inc

"Computer Control vs Energy Savings," R. Barth and J. Miller, Metromation

"Optimizing Plant Refrigeration System Costs," D. L. May and B. N. Norden, Monsanto Textile Co; C. A. Andreasen and C. H. Cho, Fisher Controls Co

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"Energy Conservation Control in Olefins Plant by Mini- and Microcomputers," R. Skrokov, M. Thor, and M. Weiss, Stone and Webster Engineering Corp

Session 65 2:30-5 pm
(Continuation of Session 52; Repeat of Session 34)

Clinic: How to Program Process Control Computers—Part II

Chairman: T. Montag, Fisher Controls Co

Session 66 2:30-5 pm
(Continuation of Session 53; See Session 35 for Basic Concepts)

Clinic: Programmable Logic Controllers—Advanced Concepts—Part II

Chairman: R. A. Whitehouse, Modicon

Session 67 2:30-5 pm
(Repeat of Session 3)

Clinic: IEEE-488 Workshop

Chairmen: N. Kuhn and J. G. Evans, Hewlett-Packard Co

Session 68 2:30-5 pm
(Continuation of Session 54)

Process Computer Maintenance Seminar—Part II

Chairman: L. Marsailles, The Foxboro Co

Roundtable discussion of maintaining process computer systems with vendors will be combined with comments by attendees.

JACC Professional Program Excerpts

Wednesday Afternoon

Session 2 2:30-5 pm

Energy and Utility Conservation

Chairman: P. V. Bhat, Monsanto Co

ISA Session 64

Session 6 2:30-5 pm

Minicomputers, Data Acquisition, and Control For Energy Systems

Chairman: O. M. Friedrich, U of Texas at Austin

ISA Session 61

Thursday Morning

Session 12 9 am-12 noon

Pattern Recognition in Manufacturing

Chairman: V. J. Tarassov, Western Electric Co

"Pattern Recognition for Inspection," V. J. Tarassov, Western Electric Co

"Experiments in the Automation of Visual Inspection," J. F. Jarvis, Bell Telephone Labs

"Automatic Visual Inspection," J. L. Mundy, General Electric Co

"A Pattern Recognition System for Difficult Viewing Conditions," J. Wilder, EMR Photoelectric

Session 15 — 9 am-12 noon

Computer Control Application in Process Industries

Chairman: A. alShaikh, Measurex Corp

"Application of Steady State Kalman Filter Theory with Field Results," W. Bailkawski, Domtar, Ltd

"Distributed Microcomputer Based Control of Flat Die Extruder Lines," L. Rastogi, Measurex Corp

"Control of Activated Sludge Processes," C. H. Wells and C. Williams, Envirotech Corp

"Computer Based Methodology for Disturbance Analysis of Power Plants," H. S. Rao and B. Frogner, Systems Control, Inc

"Application of Mathematical Modeling to Design of a Practical Controller or a Commercial Scale Fossil Power Plant," D. A. Berkowitz, The Mitre Corp

Thursday Afternoon

Session 19 — 2-5 pm

Pattern Recognition and its Applications

Chairman: G. N. Saridis, Purdue U

"Statistical Pattern Classification Using Contextural Information," T. S. Yu and K. S. Fu, Purdue U

"Pattern Recognition in Distributed Computering Environments," Y. T. Chien, U of Conn

"Application of Pattern Recognition to Industrial Inspection," T. Pavlidis, Princeton U

"Multilevel Syntax Analysis for Geological Data Compression," H. Stephanou, Exxon Production Research Co

"New Results in Image Alignment," T. R. Chow, ESL Inc

"Digital Linear Processor Theory & Optimum Multidimensional Image Reconstruction," S. Chang, State U of New York at Stonybrook

Friday Morning

Session 26 — 9 am-12 noon

Distributed Systems for Process Control

Chairman: E. H. Bristo, The Foxboro Co

"Recovery and Reconfiguration in Distributed Intelligence Data Acquisition and Control Systems," W. Rose, Case Western Reserve U

"Evaluation of a Distributed Process Measurement and Control System Reliability," R. Kenneford and F. Romey, Honeywell Inc

"Design Optimization of a Process Based Remote Multiplexing System and the Distribution of Input/Output Variables," W. L. Summers, Ebasco Services, Inc

"Distributed, Hierarchical Process Control Function Before Form," R. Ash and J. Trchka, Proctor and Gamble Co

"The Organization of Microprocessor Based Remote Multiplexing Systems," K. M. Zahr, Ebasco Services, Inc

Friday Afternoon

Session 37 — 2-5 pm

Programmable Systems for Manufacturing

Chairman: J. E. Barton, Charles Stark Draper Laboratory, Inc

"Control of a Programmable System Test Bed," D. Seltzer, Charles Stark Draper Laboratory, Inc

"Vision Control Subassembly Station," D. McGhie and J. Hill, SRI International

"Control and Systems Aspects of Flexible Manufacturing Systems," J. J. Solberg and J. J. Talavage, Purdue U

"Computer Controlled Industrial Robot: A Truly Programmable System," J. Ray, Cincinnati, Milacron Inc

Session 38 — 2-5 pm

Real World Applications of Control Systems in Pulp and Paper

Chairman: M. Mihalik, Taylor Instrument Co

"Energy Management Systems," Dick Hanson, Taylor Instrument Co

"Modeling and Computer Control of White Liquor Preparation in a Kraft Pulp Mill," P. Uronen, Purdue U

Session 42 — 2-5 pm

Computational Method

Chairman: A. Moyer, General Electric Co

"Highly Parallel Processor for Matrix Computation," A. Moyer, D. Fifolt, and W. Rice, General Electric Co

"Parallel Matrice Inversion Algorithm for Dedicated Matrix Processor Applications," A. Moyer, General Electric Co

"A Section Alyzation Solution of the Steady State Matrix Riccati Equation," D. Repperger, Aerospace Medical Research Lab

"Calculation of the Function of an Arbitrary Matrix by Finding Constituent Idempotent Matrices," F. Chang and E. Edward, Alabama A&M U □

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ANALYZING COMPUTER TECHNOLOGY COSTS—

PART 1: DEVELOPMENT AND MANUFACTURING

Computer equipment manufacturers can improve both efficiency and profitability if their design engineers fully comprehend costs of development, manufacture, and maintenance, and apply that knowledge to product engineering. Part 1 of this 2-part article demonstrates how to set up simple models of development and manufacturing costs

Montgomery Phister, Jr Consultant, Santa Monica, California

Profitability through the development, manufacture, and sale of hardware is the primary objective of a computer equipment manufacturer. However, in the normal course of business, he encounters a host of seemingly intractable problems. A potential customer unaccountably revises his procurement specifications; a major competitor unexpectedly announces a new product; a key design engineer leaves the company; a hardware, software, or documentation project misses a scheduled deadline. Consequently, while reacting quickly and sensibly to these and other problems, the manufacturer seldom finds time to analyze and understand the internal workings of his diversified organization. In practice, however, a careful study of certain measurable and controllable cost factors can provide many benefits if it balances the critical elements of product expenditures. Specifically, a quantitative, analytic examination of the costs of product development, manufacture, and maintenance helps an organization if it

(1) Calls attention to potential tradeoffs between cost elements. Development times and costs may be used to refine a design, thus reducing manufacturing costs. They may also add serviceability capabilities that increase manufacturing costs but reduce maintenance costs. These overall tradeoffs affect the development, manufacturing, and maintenance operations jointly, but potential gains also accrue from more local tradeoffs. A linear regulated power supply may be cheaper than a switching supply for a given power level, but it offers less efficiency and occupies more space. Training and placement of specialist maintenance engineers appears costly, but in fact these actions may reduce total maintenance costs by shortening the average time required to repair a failure.

(2) Identifies specific high cost areas where further study, additional development, or management actions may improve profits. A careful cost study may indicate that preventive maintenance actions can be performed less frequently with a negligible effect on equipment availability, but with a substantial reduction in maintenance costs. Another study may suggest that manufacturing final test costs seem unreasonably high, or that many documentation tasks could be automated.

Such conclusions are not likely to be derived by an organization that does not examine the costs of its technical activities in great detail.

(3) Alerts hardware and software development engineers to the company wide, long term impact of their actions or oversights. The designer should, for example, understand all the cost implications of each new component inserted into a product. Total cost savings of the component must pay for all incurred documentation, component qualification, and test equipment charges. Similarly, the programmer should thoroughly understand the maintenance cost implications of operating systems and related software. One result may be the collection and analysis of comprehensive error statistics or diagnostic information, with a subsequent reduction in average system troubleshooting and repair time. Analytic cost models will not supply automatic answers, but it is likely that designers who understand such models will take all relevant costs into account.

(4) Emphasizes cost trends, thereby helping to ensure that planning will anticipate future opportunities and problems. For example, as integrated circuit (IC) densities increase, interconnect and packaging technologies must change to make the new low cost logic practicable. As development costs of custom ICs decrease, it may be feasible to use proprietary ICs for certain applications. As labor costs rise, and test equipment becomes cheaper and better, automated checkout procedures in manufacturing will require that development engineers introduce special test circuits and facilities into systems and subassemblies. A manufacturer can anticipate factors that will influence future efficiencies and economies only by observing current cost trends.

To realize these four benefits, companies must commit resources to the collection and analysis of available data about development, manufacturing, and maintenance operations. The objective is to establish quantitative relationships—or mathematical models—between product complexity and maintainability, and product development, manufacture, and maintenance costs. Generally, an adequate start can be obtained by making use of existing company records, supplemented by estimates from experienced personnel. Then, the resulting preliminary models can be refined, modified, and improved in order to increase accuracy and to reflect new technologies and changing company practices.

Overhead Costs

The starting point for most cost analyses is labor cost of key employees. Generally, it is convenient and accurate to estimate incremental costs by multiplying the employee's time by an hourly rate. These costs must, however, include not only the employee's salary rate, but also such overhead costs as fringe benefits, supervision and secretarial salaries, and facility. Unique cost factors, together with some variability in those that are common, yield substantial variations in overhead from one organization to another; therefore, it is sensible to establish overhead rates as a first step in operations analysis.

Assume that a company has 50 engineers in hardware development; that their total annual salary is $1,000,000; and that total annual development expense, including materials, technician and drafting labor, managers' salaries, etc, is $3.20 million. The overhead rate for the engineers, defined as the ratio of all other costs to their direct salary costs, is $(3.2 - 1.0)/1.0 \times 100\%$ or 220%. Thus, a development engineering man-hour realistically costs $32 ($10 in direct salary and $22 in associated overhead). Comparable overhead rates might be 125% for software development and 185% for manufacturing and maintenance labor. Note that an analysis of actual rates in an existing organization can be rewarding if it pinpoints duplication or waste.

Development Functions

Two distinct types of development costs are technology and product. Technology development provides specific tools, techniques, components, procedures, and assemblies which, taken together, constitute a mastery of the skills required to produce a family of products. It must precede product development, which comprises one or more projects, each aimed at designing a specific product.

Technology development is itself subdivided into two parts: technology employed by the development organization to facilitate its own operations, and product technology in manufacturing. Development organization technology essentially consists of tools, such as a design automation system, stroboscope, and system performance monitor. These may be especially developed within the organization, but are often purchased outside.

Product technology in manufacturing is the more important, and is more expensive to develop. Various technology categories can be identified. For electronic products, they include components, interconnects, power systems, packaging systems, and special circuits. For peripheral products, they comprise media, mechanisms, and transducers, plus all the electronic product categories. Product development is the familiar project-type activity that starts with a particular product specification—for a processor or FORTRAN compiler, for example—and delivers a checked-out product ready for manufacture and/or distribution.

In some organizations, technology development is accomplished as part of product development. Logic design engineers, for example, also choose components and connectors. Such an arrangement can be efficient, especially if the development engineers are capable and experienced, but it has drawbacks. In a large organization, it can lead to duplication of design effort and to manufacturing inefficiencies, as several development organizations may develop different assemblies and use different components when they could be using a common technology. Even in a small organization, where duplication may not be a problem, the co-mingling of product and technology developments will probably cause problems because the project engineer, anxious to release a specific product on schedule, will not take the time to develop a technology applicable to a range of products, or to investigate and properly document the technology selected.

Technology Development Costs

The best method in determining development costs is to identify the tasks that must be performed, and then to

estimate the cost of each. Tasks necessary to develop a technology generally come under two headings: procurement of purchased items, and establishment of standard processes and assemblies.

A purchased item intended to be a part of manufacturing technology may be a material, component, media, assembly, subsystem, procedure, or process. Procurement procedures necessary to incorporate a purchased item into the technology include some or all of the following tasks:

(1) Write a purchase specification for the vendor or vendors who can supply the item. It lists the dimensional, mechanical, functional, electrical, and other properties important to the designer, giving both nominal values and acceptable tolerances on all measurements. It serves as the basis of a contract between vendor and purchaser; if the item meets specifications, it is accepted for payment.

(2) Write a test specification that establishes what tests and measurements should be taken, and how they should be conducted or obtained. This document will be used by manufacturing's quality control organization during inspection and test of incoming parts and assemblies.

(3) Provide special test equipment to measure properties of incoming items, or of assemblies at various stages of manufacture. Such equipment is sometimes designed internally and sometimes purchased. Development engineering generally works with manufacturing engineering to provide this test gear.

(4) Qualify vendors who can furnish parts which meet specifications; then the purchaser can bargain for the lowest price. A purchase specification is often generated during negotiations between buyer and several vendors. In the course of negotiations, vendors furnish parts that are tested, measured, and evaluated; ultimately some vendors are approved as being technically able to supply the part.

(5) Write usage specifications that describe items from the designers' point of view, and set forth rules and advice for their adoption into new designs. After an item has been documented, procured, and stocked in manufacturing, it should find multiple design use.

Another necessary set of tasks establishes standard processes (eg, for connecting two or more IC chips to an interconnecting substrate, and for encapsulating the result), or documents standard assemblies (eg, a removable disc pack with built-in read/write heads). The required tasks include

(1) Prepare assembly drawings and process procedures that discuss, in great detail, how to create the assembly from purchased parts and materials, or how to carry out the process.

(2) Write test specifications that define special measurements or tests to be used in the course of manufacture. Such tests reduce waste by detecting manufacturing problems at the earliest practicable time.

(3) Design tools and fixtures that facilitate manufacturing processes, (eg, clamping parts together to make for easier assembly.) While this is normally the job of manufacturing engineering, new technology often requires particularly novel or precise fixtures or tools, which are developed along with the technology and must be documented by the engineering organization.

TABLE 1

Technology Development Cost Factors

Technology Element	Minimum Program*	Substantial Program*
Components		
Simple (eg, register, light bulb, screw)	0.02	0.5
Complex (eg, transistor, IC, relay)	1	6
Interconnects		
Components (eg, connectors, wire)	0.02	0.5
Techniques (eg, soldering, wirewrap)	0.5	20
PC card	1	3
Intercabinet cables	0.02	3
Packaging		
Cabinet, hardware, cooling system	2	12
Power System		
Power supply	1.5	12
Special Circuits		
Circuit design and layout	10	20

*Time, in man-months per item listed, based upon author's experience

(4) Participate in pilot operations. When assembly drawings, process procedures, test specifications, and tooling designs have been released to manufacturing, that organization should be able to fabricate the assemblies and to operate the processes. To facilitate the manufacturing start-up process, a small pilot manufacturing operation is often set up, where assemblies and processes are conducted under the close scrutiny of development and manufacturing engineers.

It is difficult to establish a cost for many of the described functions, but Table 1 gives estimates, in man-months, for the engineering time necessary to develop various elements of an electronic-based technology. The minimum program shown represents a limited design effort—the type that might be suitable for a small or new organization—and the substantial program describes an encompassing effort typical of a large-volume manufacturer. The former employs shortcuts; wherever possible it adopts or adapts standard, commercially-available parts and assemblies, omits or abbreviates specifications, and permits sole-source vendors, even for critical parts. Shortcuts limit the scope of the technology (eg, a minimum program will not provide an ultra-high-performance technology), and present certain risks (eg, a sole-source vendor may stop making a critical part). However, a small organization may be able to accept such limitations. The substantial effort may adopt some existing parts, but is willing to undertake special development of ICs, connectors, power supplies, cabinets, etc, wherever such development will pay off in low manufacturing cost, in unique performance, or both.

Product Development Costs

A product development project generally begins with the creation of a product description specifying functions, performance, and sales price. Given these specifications, the development project comprises the following tasks:

(1) Prepare a detailed project plan, including scheduling, manpower, budgets for labor and materials, and computer time.

(2) Define in great detail exactly how product specifications will be met. Describe principal product components in block diagrams, and show how they work together. Include sequence or flow charts, showing timing of various functions. List rules or algorithms to be implemented.

(3) Conduct detailed system design. The result is a preliminary version of the complete documentation, describing how the product can be assembled and tested.

(4) Provide a first complete construction or assembly (prototype) of the product from the preliminary documentation.

(5) Conduct tests to compare actual operation of the product with requirements of the planning specification. Correct design errors or oversights, incorporating indicated changes into the documentation.

(6) Release and supply complete documentation to organizations that will deliver, use, and/or maintain the product. Include operating, technical, and maintenance manuals, as well as basic drawings and listings.

(7) Conduct extensive, detailed tests of the product, as constructed or assembled by the organization to which the documentation is released. This product verification is conducted by an organization other than development, but with participation of the development group. It includes actual or simulated application conditions, and generally results in detection and correction of design errors and oversights not noticed earlier.

TABLE 2

Development Cost Factors

	Hardware Development	Software Development
Productivity—Logic Elements		
Completed Per Man-Month*	250-330	175-250
Project Man-Month Breakdown		
Project planning	1%	1%
System design	7%	19%
Detailed design	43%	25%
Test	21%	30%
Product verification	8%	10%
Documentation	20%	15%

*Man-months refer to time spent by engineers and programmers only; does not include supporting personnel, covered in overhead costs

Much information has been published on the relationship between software project man-months and product complexity measured in number of instructions or statements. Little data are available on corresponding hardware development costs. Table 2 supplies the author's estimate of hardware development productivity, along with an estimate of software productivity based on a number of published studies.[1,2,3,4] Note that the unit of productivity is logic elements completed per man-month, where a logic element is the designer's basic building-block. For hardware projects, it is a circuit element employed by the designer, and ranges in complexity from a flip-flop or gate, to a shift register or counter, or to an arithmetic logic unit or microprocessor. For software projects, it is a machine-language instruction or a high-level language statement. Studies have shown that software productivity is roughly the same whether programmers use machine languages or compilers, so that the use of high-level languages improves productivity measured in ultimate machine instructions (often referred to as object instructions as distinguished from source instructions) per man-month. The breakdown of project effort (Table 2) is likewise based on the author's estimate for hardware design, and on published studies for software.[2,3,5]

The hardware project includes a major programming task: the completion of a diagnostic program to check out the hardware product and subsequently to be used as a diagnostic tool for the maintenance organization. However, the hardware product itself is assumed to be a classical design task not making use of microprogramming. In recent years, microprogramming has become widely used as a design technique with the result that hardware projects have taken on the attributes of software projects. Assume that the control portion of a hardware system is implemented using microcode; that it takes 20 bits of microprogram memory to replace a hardware gate; and that microinstructions are 50 bits long. Then, 1000 hardware gates, which would take 3 or 4 man-months of development effort according to the hardware project side of Table 2, would translate to 20,000 microprogram memory bits, or 400 microinstructions, requiring only about 2 months of development effort—if microprogrammers are as productive as system programmers. Thus, microprogramming has a potential for reducing development costs.

In Table 2, the data are representative of many average projects. However, the conclusion universally drawn by each study of software development has been that there are enormous variations in productivity, both from one programmer to another, and from one kind of project to another. Ratios of 40:1 in productivity are not at all unusual; for example, Daly[3] reports a range from 50 to over 2000 instructions per man-month. In reviewing the history of past projects, each organization is likely to find similar variations in productivity of its own hardware and software development. But the process of defining productivity in terms suitable to the organization, and of attempting to understand the reasons for productivity differences experienced in past projects, is likely to lead to improvements in project planning and scheduling, and to suggestions for new tools, techniques, and procedures aimed at improving productivity itself.

TABLE 3

Manufacturing Cost Factors for 1978

Item	Cost ($)	Time (Min)
Components (all purchased)		
LSI	10.00	
LSI support	5.00	
64-bit RAM	1.50	
4k P/ROM	5.00	
MSI	1.02	
SSI	0.28	
Interconnect System		
PC boards (I-H)		
Labor		$\frac{7.5 + 0.39A}{0.87(1 - 0.00053A)}$
Materials (purchased)	$\frac{0.0553A}{0.87(1 - 0.00053A)}$	
Automatic wirewrap		
Labor (I-H)		0.018P
Materials (purchased)	0.011P	
Connectors (purchased)	(0.24 + 0.024P)	
Power System		
Power supply (I-H)	(200 + 0.5W)	
Power wiring		
Labor (I-H)		1.6C
Materials (purchased)	0.03C	
Packaging System (I-H)		
Cabinet	$(145 + 4.4V_c)$	
Module mount	$(17.6 + 0.22V_m)$	
Cooling system	0.14W	
Labor Factors		
Module fabrication		
Component insertion		
16-pin DIP		0.25
24- or 40-pin DIP		0.50
Module soldering		(2 + 0.1A)
Module test		$(11.75 + 0.000625A^2)$
System assembly and test		
Install connector		0.33
Install module mount		2.0
Install power supply		5.0
Plug in module		0.25
Locate and correct "f" failures		$5f^2$
Exercise a one-cabinet system		480

Definitions:

I-H = In-house acquisition
P = No. pins/connector
V_c = Cabinet volume = product of outside dimensions (ft^3) (0.028 m^3)
V_m = Module mount (card cage) volume = PCB area x PCB spacing (in^3) (16.4 cm^3) $\leq$ 700
W = System dc power requirements (watts); $350 \leq W \leq 1000$
A = PCB area (in^2) (6.45 cm^2); $A \leq 432$
C = Number of power and ground wires to be connected

TABLE 4

Miscellaneous Manufacturing Cost Factors for 1978

Item	Value
Volumetric Factors	
Usable cabinet volume	25%
Power supply volume	1.0 in^3/W (16.4 cm^3/W)
Cooling fan volume	2.0 in^3/W (32.8 cm^3/W)
Component Power Requirements	
LSI	500 mW
LSI support	300 mW
64-bit RAM	400 mW
4k P/ROM	500 mW
MSI	150 mW
SSI	50 mW
Labor Cost Rates	
Assembly hourly wage	$5.10/h
Overhead rate	185%
Burdened assembly labor	$14.54/h
Module test labor	$17.44/h
System test labor	$21.80/h
Other Factors	
Intercabinet cable costs (as a percent of total other interconnect costs)	5%
Proportion of bad components at initial system test	0.05%

Manufacturing Costs

Manufacturing costs involve the expenses of producing quantities of a product in a manufacturing environment, where personnel without engineering or scientific training follow procedures as specified in engineering-released documentation. However, no standard method of accounting exists for manufacturing costs, and two different organizations producing the same product from the same drawings might record different costs. Two reasons for such a cost discrepancy are likely:

(1) The two organizations might follow different rules in deciding what should be included in manufacturing cost and what should be charged to other cost centers. Direct labor and materials charged to the product would be included by both organizations, but each might have a different treatment for such items as quality control labor, or depreciation of tools and equipment.

(2) Given a common definition of manufacturing costs, the two organizations would probably still record different costs for the same product because of variations in efficiency, in experience with the particular type of product, and in tool and fixture investments to facilitate product assembly and test.

In examining manufacturing costs for the purposes proposed in this article, an organization should establish a definition consistent with its goals and aims. Two pertinent uses for manufacturing cost information can be distinguished, each important in a different way. First, during the time a product technology is under development, it is desirable to estimate how manufacturing costs will vary over a wide range of hardware parameters. For example, in planning a power system and in designing system cabinets, information is needed to show how power supply costs vary with power output, and how cabinet costs vary with their dimensions. In planning a family of line printers or moving-head files, estimates are necessary that show how printhammer costs vary with printer speed, and how read/write head costs vary with recording density. Understanding these variables, the designer selects particular operating points, such as a specific power supply size or printhammer type, which serve as the basis for the product line. These choices are made so that the technology will support a range of products economically, from small low performance units to large high performance units. In general, the chosen technology limits each end of the size range. It makes systems that are below some particular size uneconomical, and systems with very high performance impossible. For example, if a standard power supply has an output of 1000 W, it is too expensive for small 200-W systems; if a printhammer is designed for a maximum print speed of 600 lines/min, it precludes entering the market for 1000-lines/min and faster printers. Of course, a smaller power supply and a faster printhammer could be designed to extend the technology, but their development will add to expenses, and their existence will cause scheduling, inventory, training, and start-up costs throughout the organization. Furthermore, the limits of potential products have been changed but not eliminated by the additional development.

The other important use of manufacturing costs arises after a technology has been established, while developing new products. During this period, the total manufacturing cost of a proposed new product design, using elements of the technology, needs to be estimated. In addition, incremental costs, such as the cost of adding or of removing a particular capability, must be evaluated.

Tables 3 and 4 provide cost models for the manufacture of an all-electronic system—models useful either in planning a technology or in evaluating product decisions. The models represent typical 1978 manufacturing cost factors; these factors are derived partly from the author's experience, and partly from industry sources. Component costs are based on large quantity purchases. The printed circuit board (PCB) formulas are for 4-layer boards having 12-mil line widths and spacings. The power supply is a switching-type, and the formula is applicable in the range of 150 to 1000 W, although linear regulated supplies are today probably cheaper and preferable for outputs under 350 W. A module is a PCB with components installed and tested. A module mount or card cage supports the modules and their connectors, and provides a channel for forced-air cooling. Module mount cost does not include the cost of connectors. Module soldering time includes the labor for flow-soldering, inspection, and repair. Automatic wirewrap machine costs include machine depreciation and wire cost.

As Table 4 shows, a relatively small proportion of cabinet volume is actually available for modules, power supplies, and cooling equipment. Listed values are appropriate for a large cabinet, where two sides and the top are not accessible for maintenance. In smaller freestanding cabinets, the usable volume may approach 40%

TABLE 5

Characteristics of a Particular System

Given Parameters	Value
Cabinet	2 x 2 x 6 ft (60 x 60 x 180 cm)
Modules	
PCB size	8.5 x 11.75 in (21.6 x 30 cm)
Layers	4
Line width and spacing	0.012 in (0.03 cm)
Number of pins per module	150
Space between modules	0.5 in (1.27 cm)
Components per module	90
Component proportions	
LSI	1%
LSI support	3%
64-bit RAM	1%
4k P/ROM	5%
MSI	45%
SSI	45%
Derived Characteristics	
Power Per 100 Components	13.3 W
Power Per Module	12.0 W
For One Module	
Module volume	50 in^3 (820 cm^3)
Power supply volume	12 in^3 (197 cm^3)
Cooling fan volume	24 in^3 (394 cm^3)
Total volume	86 in^3 (1411 cm^3)
Cabinet Volume	
Total	24 ft^3 (0.67 m^3)
Usable Volume	6 ft^3 (0.17 m^3)
Reserved for add-ons	1 ft^3 (0.03 m^3)
Volume remaining	5 ft^3 (8640 in^3) (0.14 m^3)
Number of modules per cabinet	100
Total cabinet power	1.2 kW
Costs Per Cabinet	
Components	$9900
Power	
Two supplies at 600 W	$1000
Power wiring	$ 83
Subtotal power	$1083

Given Parameters	Value
Interconnects	
Modules	
100 PCBs	$2038
Assembly labor	$ 885
Module test labor	$ 523
100 150-pin connectors	$ 384
Backwiring labor	$ 65
Wire and AWW Depreciation	$ 165
Cables	$ 203
Subtotal Interconnects	$4263
Packaging	
Cabinet	$ 251
Eight module mounts	$1241
Cooling fans	$ 168
Subtotal Packaging	$1660
Assembly and test	
System assembly labor	$20
System test labor	$220
Subtotal assembly/test	$240
Total one-cabinet cost	$17,146
Cost Ratios	
Distribution of total costs	
Components	57.7%
Power	6.3%
Interconnects	24.9%
Packaging	9.7%
Assembly and test	1.4%
Cost per IC	
Components	$ 1.10
Power	$ 0.12
Interconnects	$ 0.47
Packaging	$ 0.18
Assembly and test	$ 0.03
Total cost per IC	$ 1.90
Power Dissipation	
Per IC	133 mW
Per module	12 W
Per unit of cabinet volume	50 W/ft^3 (1766 W/m^3)

of the total. Power supply and cooling fan volumes are computed by multiplying the outside dimensions of power and fan assemblies, and dividing by the power delivered to, or to be removed from, the modules. Component power ratings are assumed averages. Assembly hourly wage is extrapolated from the average 1976 wage for production workers in Standard Industrial Code (SIC) 3573, electronic computing equipment. Module test labor is assumed to be 20% more, and system test labor 50% more, than burdened assembly labor.

To apply cost models, characteristics of a particular system are specified in Table 5. The upper portion specifies the given parameters; the remainder of the table shows resulting system characteristics and costs, derived from given data and from models of Tables 3 and 4.

Power per 100 components is derived from component ratios in Table 5, and from power dissipation per component given in Table 4. Power per module is based on the average of 90 ICs per module. Power supply and cooling system volumes per module are based on a module power of 12 W, and on the volume per watt factors of Table 4. Total cabinet space required per module is the sum of module, power, and cooling volumes —86 in^3 (1411 cm^3) per module.

Usable cabinet volume is derived from cabinet dimensions, and the ratio in Table 4. One-sixth of the usable volume is set aside for spares or options. The remaining 5 ft^3, or 8640 in^3 (0.14 m^3), support 100 modules. Cabinet power (excluding that dissipated in the power supply itself) is 1.2 kW.

TABLE 6

Logic Count for Components and System

	RAM Bits	Per IC Flip-Flops	Gates	IC Distribution	Per 100 ICs RAM Bits	Per 100 ICs Flip-Flops	Per 100 ICs Gates
LSI							
Microprocessor	32	25	125	1	32	25	125
Microprocessor support	0	7	35	3	0	21	105
RAM	64	0	0	1	64	0	0
P/ROM (4k)	—	—	205	5	—	—	1024
MSI	0	2	22	45	0	90	990
SSI	0	0.2	3.6	45	0	9	162
Totals				100	96	145	2406

Component costs are derived from Table 3, power supply and wiring costs from application of the formulas in Table 3, using the burdened assembly labor hourly cost in Table 4. PCB costs are computed from the formulas of Table 3, again using assembly labor hourly costs. Module assembly labor is based on component insertion and module soldering times in Table 3, assuming that the SSI, MSI, and RAM ICs have 16 pins, the remainder 24 or 40. Module test labor cost is computed from the formula of Table 3, using module test hourly rate from Table 4.

Connector, cabinet, module mount, and cooling fan costs are derived from formulas of Table 3, as well as backwiring costs based on automatic wirewrap factors. Cable costs are computed using the cable factor in Table 4, and system assembly costs using those in Table 3. Failure rate factor in Table 4 suggests that about five of the 9000 ICs will be defective when system test begins, and the factors at the bottom of Table 3 are used to compute test times. System test labor hourly cost comes from Table 4. Note that the total cost per IC is $1.90 (Table 5), about half of which is in the IC itself. (See Ref 6 for similar, but earlier analysis.)

Another system cost measure takes the logical complexity of the product into consideration. Table 6 provides a typical logic count for the family of ICs in question. This table attempts to measure logic complexity by counting bits stored and logic gates. A gate is an inverter, buffer, NAND, AND, NOR, or OR circuit, having one or more inputs. Flip-flops include latches. The P/ROM is assumed to be used as microprogram storage, with the further assumption that it takes 20 bits of storage to replace one gate. Note that each 100 ICs include 96 + 145 = 241 bits, about 40% of which are in RAM arrays, the remainder in logic flip-flops. For each logic flip-flop, there are about 17 gates, typical for today's systems. Thus, the full cabinet contains 9000 ICs x 2.41 bits/IC = 21,690 system bits, at a system manufacturing cost of $17,146 ÷ 21,690, or 79.1 cents/bit.

Acknowledgements

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Part 2 of this article will appear in October. It will show how maintenance cost predictions can be made, based on mean times between failures and mean times to repair. Precise, accurate predictions are not feasible, but first-order approximations are entirely appropriate to assist manufacturers and designers in achieving the listed benefits.

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CD-9

DESIGNING INTERRUPT STRUCTURES FOR MULTIPROCESSOR SYSTEMS

Designing interrupt mechanisms for microprocessor based systems involves identifying the function phase partitions, assigning prioritization techniques, and classifying software categories, but can result in optimum system throughput

Rajen Jaswa General Electric Co, Daytona Beach, Florida

Realtime multiprocessor systems are generally interrupt driven because interrupts optimize the handling of asynchronous events and facilitate the design of loosely coupled systems, in which several largely independent processors are organized in an application dependent hierarchy. Communication within the system is also initiated through interrupts and involves data, command, and status transfers; thus, excessive overhead (hardware and software) in interrupt handling can drastically affect system throughput. System control and organization in the hierarchy are implemented by the interrupt structure's prioritization algorithms; the degree of complexity depends on the system performance goals. Communication and control in such a system are necessary at four levels: within the processor, within the intelligent subsystem, at the operating system executive, and for interprocessor interaction. Ideally, the interrupt structure should optimize all performance levels.

Interrupt Definitions

An interrupt mechanism is a well-defined transaction that permits an asynchronous event (interrupt) to cause a change in the normal flow of program execution. There are several phases to the interrupt transaction and the implementations of these phases differ among processors to take advantage of the commonalities of the applications that the computer designer projected for the system design. The critical effect is that interrupts can have a wide-ranging impact on system design in terms of flexibility, future expansion, excessive interface hardware, and hardware independent software interface.

A processor's interrupt structure can be partitioned into five functional phases: (1) interrupt requests, (2) interrupt masking and enabling, (3) saving current central processing unit (CPU) status, (4) interrupt acknowledge, and (5) decoding request to access corresponding starting address of interrupt service routine. Implementation of these phases differs as the computer designer incorporates prioritization techniques into each phase.

As computers evolve into large realtime multitasking systems, they must interface simultaneously with several different types of peripheral devices, such as teletypewriters, printers, and terminals, and still operate with a tolerable degradation in system performance. This is possible because the computer cycles several orders of magnitude faster than its interfaces. Therefore, algorithms have been developed that timeshare computer processing time among various tasks and optimize utilization of valuable resources. However, these algorithms rely on assigned (static or dynamic) task priorities. These assigned priorities are incorporated by the computer de-

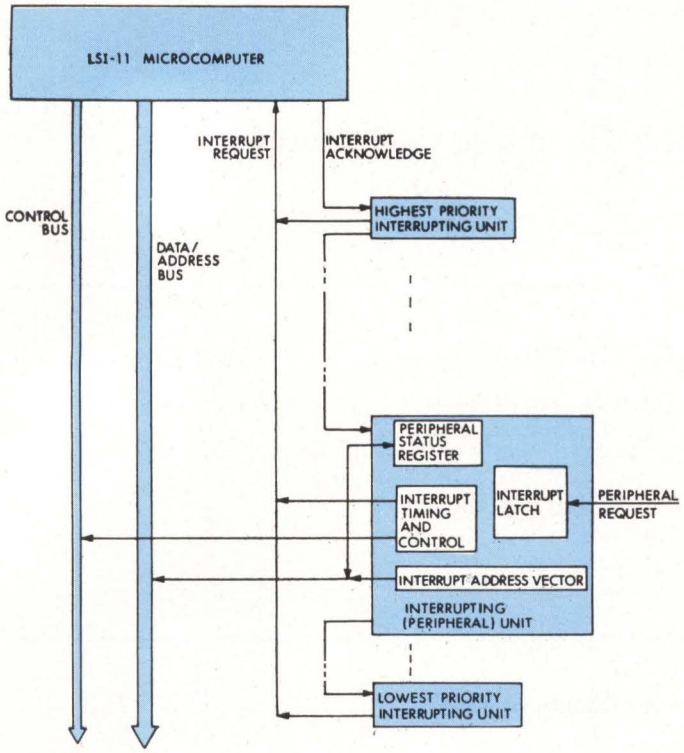


Fig 1 LSI-11 interrupt structure. This structure establishes priority by daisy-chaining interrupt acknowledge; then, interrupting unit identifies itself by its interrupt routine address vector. Considerable hardware is necessary at each peripheral to facilitate interrupt transaction

signer in each phase of the interrupt structure; the level of design sophistication introduced depends on the range of applications predicted for the computer. Each phase's implicit priority and its impact on the system must be carefully evaluated by the system designer during processor selection.

Interrupt Request Phase

This phase is asserted on the interrupt request line. There may be only one interrupt request line, to which all the interrupting units are connected, as in the LSI-11 (Fig 1). Conversely, there may be several interrupt request lines, each with a unique priority, with usually one interrupting unit assigned to a request line, as in the TMS 9900 (Fig 2), which has 16 interrupt priority levels. This wide interrupt request bus results in quicker response, since the highest priority interrupting unit can be identified immediately. Independent interrupt lines also result in simpler interfaces in the peripheral units, basically, a single interrupt request flip-flop. The obvious tradeoff is a wider bus. In addition, the total number of interrupting devices is restricted to the number of available interrupt lines (more units per priority level are possible, but that is not what is intended for the processor).

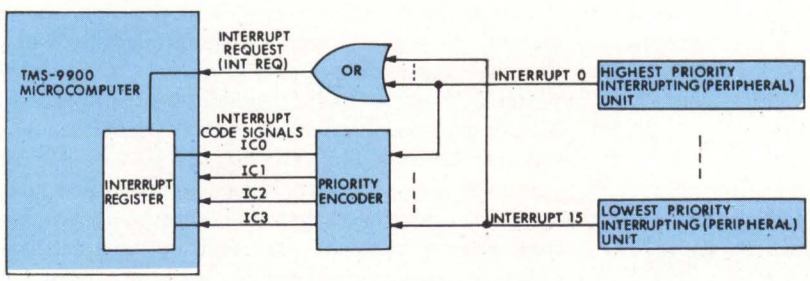


Fig 2 TMS 9900 interrupt structure. Structure has 16 prioritized interrupt request levels. Interrupt request logic at each peripheral consists of one flip-flop, and priority encoder identifies highest interrupting unit by means of interrupt code signals IC0 to IC3, along with interrupt request. Result is inexpensive interrupt interface with fast interrupt response

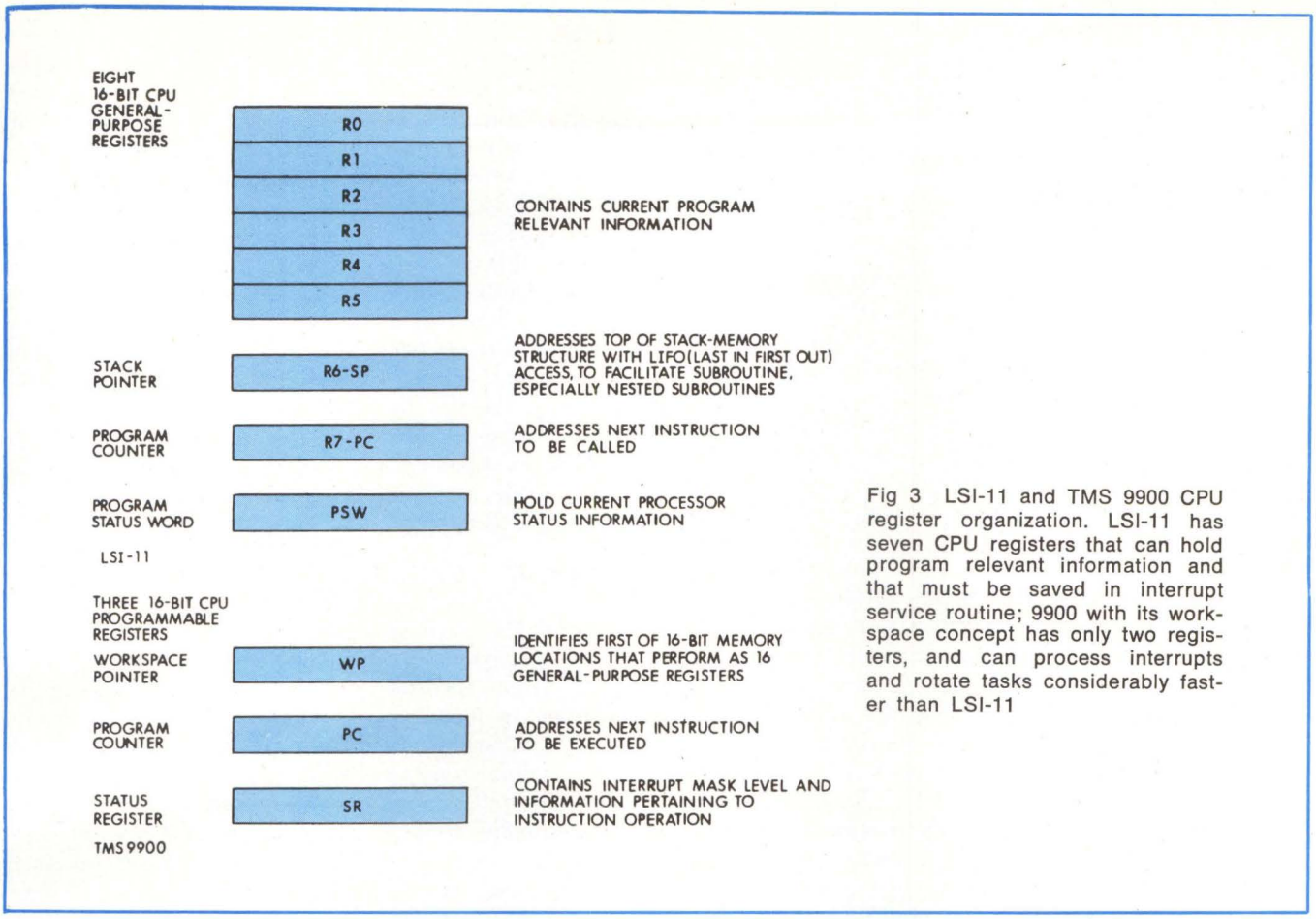


Fig 3 LSI-11 and TMS 9900 CPU register organization. LSI-11 has seven CPU registers that can hold program relevant information and that must be saved in interrupt service routine; 9900 with its workspace concept has only two registers, and can process interrupts and rotate tasks considerably faster than LSI-11

Besides these two common interrupt request designs, microprocessor designers have added some powerful capabilities to the design of the interrupt request phase. In the PPS-8 microprocessor, there are three interrupt levels. Level 0, the highest interrupt level, is dedicated to a power fail indicator; level 1 is normally dedicated to a realtime clock; and level 2 is shared by all other peripheral devices. In the prioritizing algorithm for these interrupts, level 0 cannot be disabled. However, if level 1 and 2 occur simultaneously, level 1 wins access, and it is possible in level 2 to mask out all further interrupts. This complicated algorithm is adaptable for a sophisticated set of applications.

Interrupt Masking and Enabling Phase

This functional phase can be exercised by the processor at three levels—enabling/disabling the interrupt mechanism of peripheral devices under program control; masking out all interrupts for the first few cycles after an interrupt has been accepted, so that the necessary information for interrupt nesting is saved before another interrupt occurs; and selective masking of interrupts within a program section. The first two levels are available in most processors, while different schemes of selective masking have evolved to satisfy demanding classes of applications. In the TMS 9900, it is possible to selectively mask further interrupts under program control; ie, even if an interrupt at the eighth level is being processed, it is possible to mask out all interrupts from the fifth level downward. The implementation in the LSI-11 is much more rigid; either all further interrupts are disabled or all interrupts with a priority below the present interrupt being serviced are disabled. This could be an important distinction when it is necessary to dynamically assign priority. Although priority assignment is hardwired initially, selective masking of further interrupts does allow a degree of flexibility in the 9900.

Saving Current CPU Status

Automatic saving of the current CPU status phase—critical to program recovery, either on a stack or in spare registers before an interrupt is acknowledged—is a standard capability in available processors. The task that concerns the system designer is how long this process takes and how much information must be saved; this is shown by comparing, for example, the LSI-11 and the 9900.

Fig 3 shows register organization of the LSI-11 and the TMS 9900. As a worst case, all registers could hold present program relevant information, and all might be used by the interrupt handler, which implies that all registers must be saved. The 9900 with its workspace concept and stress on indirect addressed operands can save complete current CPU status in three to four times fewer memory cycles than the LSI-11, resulting in a substantial saving in interrupt response time. However, a penalty must be paid in terms of system throughput during normal processing due to the few onboard CPU registers. Nevertheless, the 9900 provides the ability to rotate tasks at higher speed than does the LSI-11.

Interrupt Acknowledge Phase

In this phase, the processor acknowledges an interrupt request. Several microprocessors use this phase to implement a priority among the interrupting units, as well as to trigger the peripheral device to identify itself. For example, the LSI-11 has the interrupt acknowledge daisy-chained with the highest priority interrupting unit receiving it first. If this unit has not requested the interrupt, it passes on the signal (synchronously or asynchronously until the last online peripheral device is serviced. Significant time could elapse before the last device on a lengthy chain receives the interrupt acknowledge. The Z80 microprocessor has an interesting approach. Each interrupting unit receives an interrupt enable from its higher priority neighbor, if neither that unit nor higher units are requesting an interrupt. The interrupt acknowledge goes to each unit simultaneously, but only the unit that requested an interrupt and has its interrupt enabled responds. This approach not only implements a priority among peripheral devices with an economical bus, but also guarantees fast response.

The TMS 9900 does not have an interrupt acknowledge, as such, since priority is established in the request phase. The peripheral device, whose interrupt is accepted, is informed during the execution of its interrupt service routine by a program controlled reset or by servicing of the cause of the interrupt.

To appreciate some of the advances made in interrupt structure design, it is worthwhile to review the interrupt schemes of a few older designs. In single priority polled-interrupt schemes, after an interrupt is asserted, each peripheral device is polled by the processor, and then the processor takes the appropriate action. In an improved version of this scheme, the interrupting unit places its address on the select code bus, and an interlocking method of controls prevents more than one unit from loading the select code bus at one time. This allows a lower priority unit to interrupt the service routine of a higher priority unit, and requires that the processor check out the select code before rejecting the interrupt. Developments in interrupt implementation and the underlying premise of hierarchy in recent processors permit software designs that would have been impossible with the older primitive interrupt structures.

Accessing the Interrupt Handler

A tremendous diversity exists in the techniques used to determine the interrupting unit's identity and then to branch to the subroutine that services that particular unit's interrupt. The LSI-11 expects the peripheral device to load the complete 16-bit address of its interrupt service routine as data on the bus; then, the CPU takes this address and loads it into the program counter. This enables a large number of peripherals to be connected to the processor's bus, because the 16-bit address is capable of addressing the entire memory space. Also, there are few restrictions as to where the service routine is located in memory. The disadvantages are that extensive hardware is needed at the peripheral device, and that the service routine address is hardwired and is not under program control. Dynamic relocation capability is achieved by introducing a branch at the first instruction in the service routine.

Since physical limitations normally are placed on the number of connected peripherals, other microcomputers provide a more limited capability in addressing their interrupt handlers. The 8080 expects the interrupting unit to jam an 8-bit interrupt instruction on the data bus; three of these bits identify which one of eight locations (0, 8, 16, 24, 32, 40, 48, 56) the processor vectors to in memory. The SC/MP 8-bit microprocessor uses an internal register that is loaded under program control with the service routine address of the next anticipated interrupt. When the interrupt occurs, the register replaces the program counter contents; this technique may be adequate for certain dedicated systems. The TMS 9900 accesses the interrupt handler for an interrupt level by loading a doubled level number in the program counter. Since the first 32 locations are reserved for service routines of the 16 interrupt levels, the processor has a fast response.

Interrupt Applications

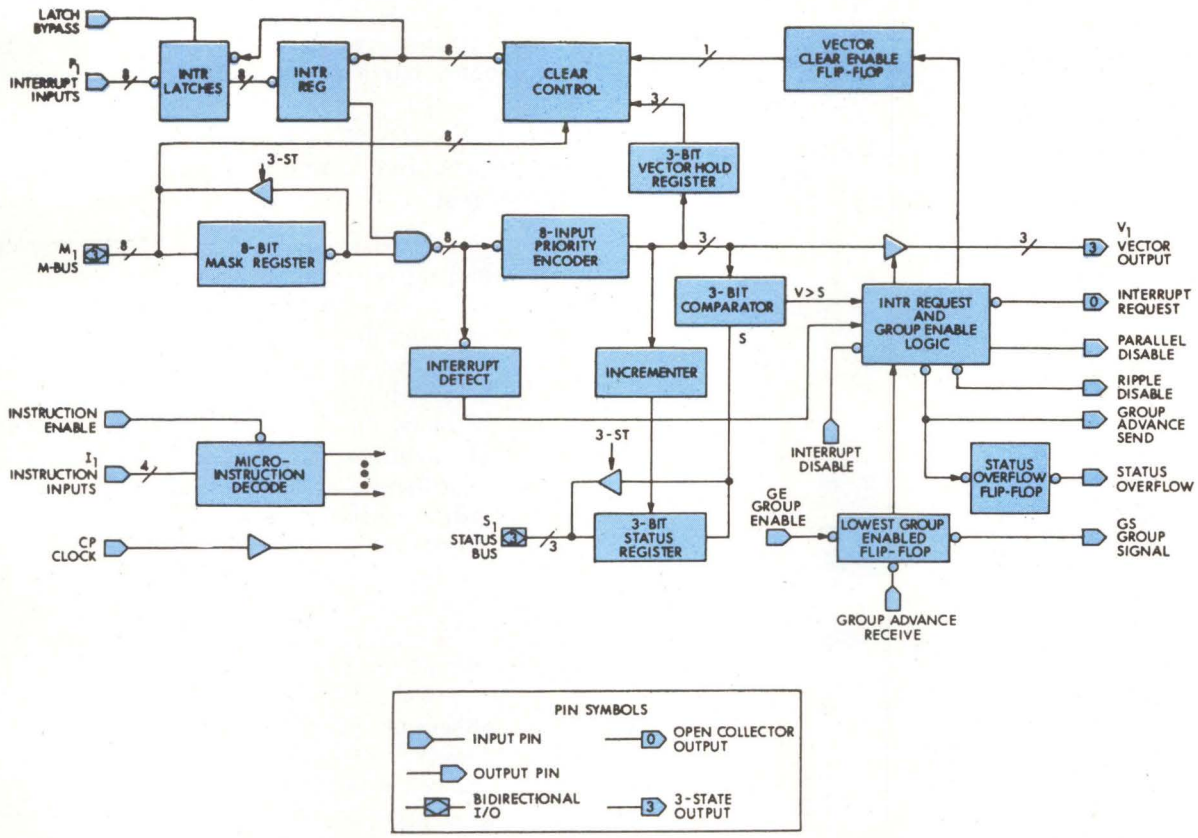
To evaluate the impact that a particular processor will have on a system, the computer designer must recognize the different applications of interrupts in the design. In addition to input/output, interrupts have been used to implement sophisticated software capabilities, such as power fail recovery and processor redundancy. In general, since the interrupt is simply a technique for handling asynchronous events, it is used to handle asynchronous events at four levels: machine level within the processor, system level with organizational ramifications, supervisory control level of the system executive, and macro-system level communication for interprocessor control. Therefore, most interrupt applications can be categorized into the following classes: (1) intraprocessor communication and control, (2) intrasystem communication and control, (3) system executive communication and control, and (4) interprocessor communication and control. A multiprocessor system operates at all four levels, and the interrupt structure that is implemented must optimize performance at each level. Since most multiprocessor systems are unique, a general purpose optimum interrupt structure has yet to be designed. Thus, choice of interrupt structure is a major design tradeoff consideration.

Intraprocessor Communication and Control

This class of applications corresponds to asynchronous events that occur within a process during execution of an instruction or function. Large mainframes cannot afford to crash due to the execution of an illegal instruction or to allow a user's program to access privileged high security data. In multiprogramming environments, tight program control is maintained; if an unauthorized program attempts to access restricted memory, that program is dumped by the interrupt routine. If a program tries to divide by zero or results in unacceptable register overflows, then these events are flagged, and the interrupt routines for these events provide for a controlled recovery. In supercomputers, the CPU has several pipelined dividers, multipliers, and other special function hardware blocks that accept operands, and some machine cycles later, have the quotient available. A sophisticated high speed interrupt scheme is needed to maximize throughput in

supercomputers. Observe that the sequence of events occurs in exactly the same order as in an input/output interrupt. However, in this case, the design goal is to minimize response time; therefore, the interrupt request phase itself must perform interrupting unit identification, obtain the interrupt service routine address, possess masking and enabling capabilities, and implement a prioritization algorithm so that only the highest priority interrupt request is serviced. In other words, a 9900 type interrupt structure is required.

Consider the Am2914 priority interrupt encoder (Fig 4). This chip has individual prioritized interrupt lines, one interrupt request, and an encoded interrupt vector that can address a programmable read-only memory (P/ROM) to access the actual service routine address. It also responds to a set of 4-bit microinstruction codes (listed in Fig 4) for dynamically assigning priority and reading the status (of interrupt inputs) under microprogram control. Under normal operation, the entire interrupt sequence is a hardwired operation. However, to provide more flexible although slower handling of asynchronous events, the Am2914 offers the capability of reading a status register under microinstruction control. Therefore, for normal operation, the interrupt structure is the same as that in the TMS 9900. Unique interrupt lines would be flagged by such events as illegal op code, register overflow, divider 1 pipeline event, unauthorized memory address, and program timeout. Priorities are assigned by the processor designer, with the flexibility of enabling under program control or dynamically masking interrupts during execution of certain microinstructions. For intraprocessor communication and control, the



MICROINSTRUCTION DESCRIPTION	MICROINSTRUCTION CODE $I_3I_2I_1I_0$
MASTER CLEAR	0000
CLEAR ALL INTERRUPTS	0001
CLEAR INTERRUPTS FROM M-BUS	0010
CLEAR INTERRUPTS FROM MASK REGISTER	0011
CLEAR INTERRUPT, LAST VECTOR READ	0100
READ VECTOR	0101
READ STATUS REGISTER	0110
READ MASK REGISTER	0111
SET MASK REGISTER	1000
LOAD STATUS REGISTER	1001
BIT CLEAR MASK REGISTER	1010
BIT SET MASK REGISTER	1011
CLEAR MASK REGISTER	1100
DISABLE INTERRUPT REQUEST	1101
LOAD MASK REGISTER	1110
ENABLE INTERRUPT REQUEST	1111

Fig 4 Am2914 priority interrupt encoder chip. Block diagram shows eight individual prioritized (P1) interrupt request lines, microprogram controlled interrupt masking and enable, and simultaneous generation of address vector (vector output to P/ROM) for accepted interrupt. Capabilities result in fast response to interrupts necessary for intraprocessor communication and control. Although normal interrupt processing is hardwired, functions listed are under microprogram control to provide for dynamic priority assignment (Courtesy of Advanced Micro Devices, Inc)

wide interrupt bus and the extra hardware are all traded-off for the goal of high speed asynchronous event handling.

Intrasystem Communication and Control

This class of interrupt applications corresponds to service requests by system peripherals. Microcomputer system designers have been innovative in implementing interrupt structures. Applications literature for commercially available microprocessor families provides an excellent reference base as to the possible areas of applications and organizations.

The organizational ramification of the interrupt structure is important to understand at the system level. In an interrupt driven system, task execution is determined by assigned interrupt priorities. Therefore, assignment of priorities determines the hierarchy in the system organization. The UNIBUS™ priority structure (Fig 5) of the PDP-11 minicomputer emphasizes this point. Seven levels of priority are available and several peripheral devices can share a priority level. The priority algorithm is defined as follows: level 7 has the highest priority and level 1 the lowest; devices closer to the CPU, on a level, have higher priority than remote devices; a routine at a priority level cannot be interrupted by a request at the same level; and most important, the CPU can set, under program control, its own priority level.* The hierarchy inherent in the interrupt structure allows the computer to interface with a variety of peripheral devices that range from high speed data storage devices to relays and sensors. It provides a setup so that unique service requirement characteristics of these devices can be met simply by assigning them to an appropriate priority level and to a position at that level. Also, since the CPU can set its priority under program control, it is possible to take care of the requirements of a low priority device whose interrupt servicing should not be interrupted. Although the ideal situation of responding to the highest priority task at a given instant is impossible, because priority assignment cannot take into account the dynamics of every situation, PDP-11 organization does provide a reasonable solution for a general purpose computer.

For intrasystem level communication and control, the optimum interrupt structure must be decided by the unique characteristics of the application. In addition to the normal considerations of speed and hardware costs, organizational ramifications must also be taken into account.

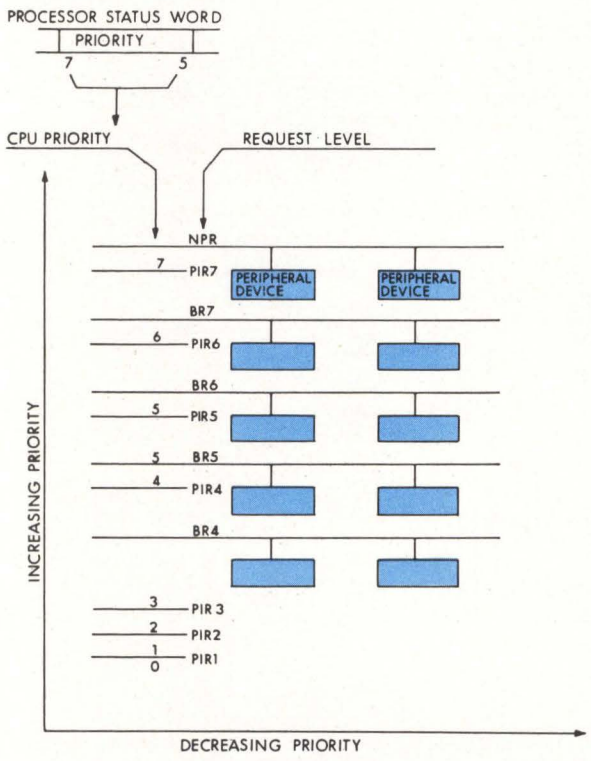


Fig 5 PDP-11 Unibus priority structure. By providing elaborate hierarchy in its interrupt structure, PDP-11 can accommodate service requirements of variety of peripherals and can manage complex system organization. It provides nonprocessor requests (NPR) for high speed direct memory access devices, four levels of bus requests (BR) for peripheral interrupts, seven levels of software interrupts for program interrupt requests (PIR), and programmable CPU operating level (Courtesy of Digital Equipment Corp)

System Executive Communication and Control

Interrupts in this class concern requests for the attention of the executive (operating system) program. As defined by Denning the operating system performs these functions: (1) creates and removes tasks; (2) controls progress of tasks, ie, ensures that each logically enabled task progresses at a positive rate and that no task can indefinitely block the progress of others; (3) acts on exceptional conditions that arise during the operation of a task, eg, arithmetic or machine errors, interrupts, addressing snags, attempted execution of illegal or privileged instructions, and protection violations; (4) allocates hardware resources among tasks, (5) provides access to software resources, eg, file editors, compilers, assemblers, subroutine libraries, and utility programs; (6) provides protection, access control, and security for information; and (7) provides a means of communicating messages or signals among tasks.

A task invokes the operating system by a software interrupt. Since the task calls the executive for a variety of services, as listed previously, and these tasks also have their unique priority (and other asynchronous events may have occurred, which could affect priorities), the software interrupt is an occasion for the executive to review complete system status before scheduling the next task. The exact manner in which this entire sequence is handled varies from system to system, but the executive interrupt structure for handling calls is critical to system throughput for multiprogramming systems.

*For completeness, direct memory access (DMA) and channel data transfers must be mentioned. Since these techniques do not divert execution of a program, but merely steal processing time, they cannot be classified as true interrupts. The PDP-11 calls them bus request/nonprocessor requests and assigns priority levels similar to interrupts (see *PDP-11/70 Processor Handbook*).

It is worthwhile to examine how different phases are implemented to facilitate executive interrupts. To speed call processing, a set of CPU registers may be dedicated to the executive; thus, calling the executive involves only switching from the designer's program counter to that of the executive. In the PDP-11/70, when a designer must run a lower priority task next, a bit is set in the program interrupt request word. The act of setting a bit triggers an interrupt, and the next task executed is the highest priority requesting task.** In the 360/370, a supervisor call is made by executing an instruction that effects an interrupt. The instruction sends a status byte to the master interrupt request register for interrupt identification. Then, the system goes through normal interrupt handling.

Prioritization techniques, however, are considerably more sophisticated than the hardwired priorities of peripherals, since the executive can change priorities under software control. For example, in realtime operating systems, like RSX-11D for the PDP-11, each user program has a priority that is initially assigned by the program user (at a price). During various phases of execution when the program must compete with other tasks for system resources, it receives priority numbers dynamically from the executive, based upon the priority assignment algorithm designed into the operating system. This algorithm is designed so that, more often than not, the highest priority task is executed at each interrupt. Unlike statically assigned hardware priorities to peripheral devices, the interrupt structure makes it possible for the executive to be somewhat aware of the dynamics of the situation and, by allocating appropriate priorities to tasks, to reach for the goal of always scheduling the highest priority task. This goal must be traded-off against the amount of processing time the executive takes up in performing its job.

In system executive communication and control, the goals set for the design also should define the exact structure for implementing a supervisor call; it should be kept in mind that prioritization algorithms are considerably more complicated than those discussed in the first two classes, since dynamic priority allocation is possible and numerous application-dependent factors govern priority allocation.

Interprocessor Communication and Control

In this class of applications, processors use interrupts to initiate data and status transfer or to transfer control to another processor. Unlike the other three application classes, where a slave requests the attention of a master (essentially), this fourth case uses interrupts between two intelligent processors; hence, the interrupt implementation should be at a different level, sometimes at several dynamically assigned levels.

To illustrate the possibilities for interrupt structures, communication between two processors in a hypothetical dual-processor system is considered for higher reliability and throughput. In this system, the current processor periodically updates the remote processor as to the present system status. Sufficient information is passed between processors that the remote processor can take over in the event of malfunctions or overloads. System malfunction is recognized when a processor fails to reset a timer at fixed intervals; this timer sends a system malfunction interrupt to the remote processor, which automatically takes over by disconnecting the current processor. The dual processors also have access to a common database on a shared high speed data storage media. In case the current processor gets tied down for a long time period while handling a critical task, the remote processor takes over servicing of lower priority peripherals. In such a system, several communication paths travel between the processors and at several levels: system malfunction interrupt, status transfer interrupt, interrupts for transferring various types of data, interrupts to access shared devices or a common database, and interrupts for taking partial control and load from a processor. The exact interrupt structure designed to facilitate communication between the two processors evolves from the philosophy established by the system designer for the application, but the possibility of dynamically programmable interrupt structures for interprocessor interrupts leads to greater flexibility, capability, and system performance.

Integrating Interrupt Structures

Processor selection is simple as long as the system designer has to select only one processor and has to optimize only at the systems level. However, in a multiprocessor system, performance must be optimized at four operating levels. Although optimum interrupt structures can be selected for individual levels, the optimum interrupt structure in general would differ for each level, confronting the system designer with the task of designing several interrupt structures and attempting to integrate them with an interrupt manager. The solution has not yet been determined, and considerable work needs to be done before the guidelines to be followed while designing a multiprocessor system can be demonstrated. Meanwhile, the following two design examples illustrate the principles involved in trying to interface two differing interrupt implementations.

Interfacing LSI-11 to TMS 9900

In this design example, the interrupt structure of the TMS 9900, with one interrupt line per peripheral device, is interfaced to the LSI-11, which has one common interrupt request and expects the highest priority interrupting unit to identify itself with an interrupt vector. Fig 6 depicts a simplified timing diagram for the LSI-11 interrupt transaction. In brief, the common interrupt request line (INT REQ) is asserted. When the computer is available, it asserts a data in (DIN) without first asserting an input/output synchronization (I/O SYNC). This indicates to all peripheral devices that an interrupt transaction is occurring, and the device that receives an interrupt acknowledge (IACK) must carry out the handshake signals that follow. Note that, since the interrupt acknowl-

**Note that when the task wants the executive to perform a function synchronously (immediately, at the present task's priority), it generates an emulator trap in the PDP-11. The executive simply performs the task, and program execution continues at the next instruction. Therefore, in a sense, the emulator trap is a technique for calling a system subroutine, rather than an asynchronous event interrupt. Although the operations are similar, there is a functional difference between them.

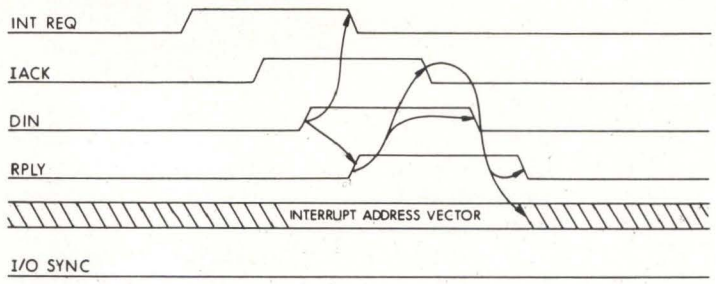


Fig 6 Simplified LSI-11 interrupt timing diagram. LSI-11 has daisy-chained interrupt acknowledge, and expects peripheral device to provide address to its interrupt service routine. Complete handshake of transaction allows LSI-11 to incorporate recovery schemes by timing out unreceived peripheral responses (Courtesy of Digital Equipment Corp)

edge is daisy-chained (Fig 1), only one interrupting unit receives it. This unit loads its interrupt 16-bit vector on the data bus and acknowledges (RPLY). The LSI-11 takes this vector and loads it into the program counter to access the service routine for the interrupt.

To interface this processor with a 9900 type interrupt structure, a frontend interface (Fig 7) is required to translate the 16 prioritized interrupt lines into 16 interrupt address vectors and to simulate the LSI-11 control signals. This interface consists of seven functional blocks:

(1) Interrupt event latch latches each interrupt until it is serviced; it consists essentially of 16 edge-triggered flip-flops.

(2) Interrupt request generator ORs all interrupts to drive INT REQ.

(3) Interrupt state latch clocks state of interrupt event latch at start of interrupt transaction so that interrupt requests during the transaction do not affect the transaction.

(4) Priority encoder identifies highest interrupting unit.

(5) Vector translator generates an interrupt vector using as address the output from the priority encoder—essentially a P/ROM.

(6) Clear serviced interrupt clears the serviced latch in the interrupt event latch.

(7) Timing and control generates LSI-11 handshaking signals.

With this frontend interface, the LSI-11—completely unaware that it is interfaced to an interrupt structure with unique interrupt lines—attains faster response times since the acknowledge is no longer daisy-chained, and requires only interrupt transaction hardware at the interface.

Interfacing TMS 9900 to LSI-11

When one of the typical interrupt levels for the TMS 9900 (Fig 2) is asserted, a common interrupt request is

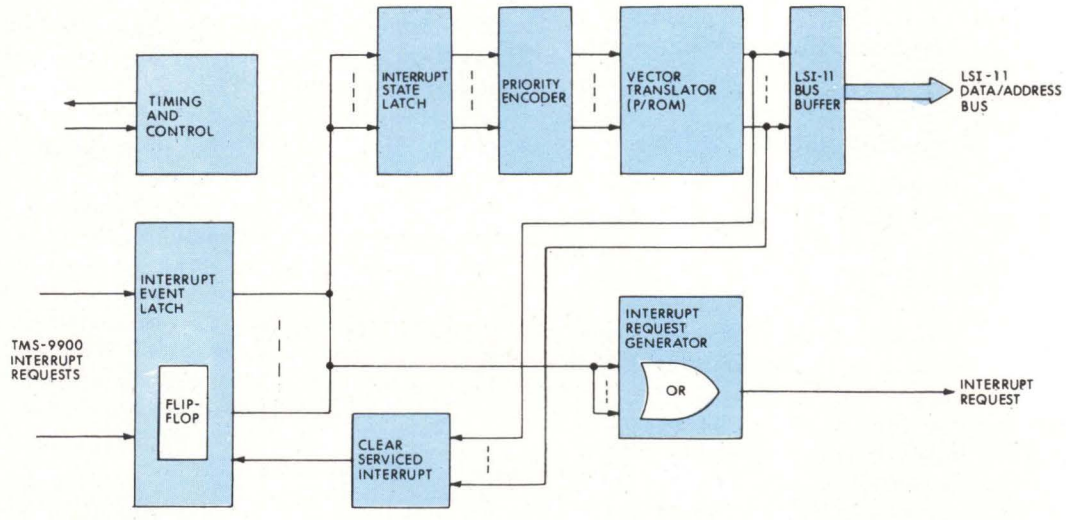


Fig 7 LSI-11 interface hardware module to TMS 9900 interrupt structure. Module translates interrupt requests to interrupt address vectors, carries out LSI-11 interrupt transaction handshake signals, and results in servicing of highest priority interrupting unit. LSI-11 is unaware that it is interfaced to 9900 interrupt structure

made to the microprocessor, and the 16 interrupt levels are priority encoded into four interrupt codes lines—IC0, IC1, IC2, and IC3. The processor compares this encoded number with its interrupt mask and, if the new interrupt has higher priority, the present routine is interrupted and a context change occurs. Since the 9900 maps its CPU registers into workspaces in memory, switching programs is as easy as changing a workspace pointer (WP) and a program counter (PC), and the system operates in a new context. The WP and the PC for the new interrupt routine are obtained from locations 0 to 32 in memory, which are reserved for the 16 interrupt level context pointers. Finally, note that level 0 cannot be masked. To use peripheral devices that are designed to interface with the LSI-11 in the 9900 scheme, hardware and software modules must be designed.

Fig 8 shows the functional blocks of the hardware interface to the TMS 9900. This interface translates interrupt address vectors and generates a 4-bit encoded interrupt request, in addition to simulating LSI-11 control signals for the peripheral units. Essentially, the six blocks serve these functions:

(1) Interface address decoder recognizes its address and enables the command decoder.

(2) Command decoder carries out two commands on the data bus—clear interrupt register and acknowledge interrupt.

(3) Interrupt register holds the address vector for highest interrupting unit to drive IC0 to IC3 from the field programmable logic array (FPLA).

(4) FPLA translates the address vector into encoded interrupt code lines IC0 to IC3.

(5) Interrupt request latch holds the interrupt request until it is cleared.

(6) Timing and control emulates the LSI-11 interrupt transaction control signals on the acknowledge interrupt command from the TMS 9900.

The associated software flowchart (Fig 9) describes the sequence of events for a typical interrupt transaction. Note that an unmaskable interrupt—level 0—is required to start the interrupt processing because LSI-11 peripherals do not identify themselves with the request; the present task may not be at a higher priority than the interrupting task. To take care of this possibility, as soon as an interrupt routine has performed its critical functions, it sets the interrupt mask to an appropriate level and clears the interrupt register to enable new interrupts. If an interrupt is waiting, an interrupt on level 0 occurs as the interrupt register is cleared. In the level 0 service routine, the interface is requested to acknowledge the interrupt. The interrupt acknowledge is daisy-chained, and the highest priority interrupting unit sends its address vector, which is clocked into the register. The FPLA encodes this address on IC0 to IC3. If this level is higher than the interrupt mask, it is serviced immediately (nesting of interrupts); otherwise, it has to wait until the present task exits.

The complicated interrupt sequence requires considerable program overhead. However, the design effort illustrates the point that although structures to implement the interrupt may differ dramatically, they can be interfaced. Therefore, it should be possible to define an optimum interrupt structure for a multiprocessor system, and then to integrate available processors into the system.

Summary

Interrupt structures are techniques for handling asynchronous events in realtime systems. The analytical ap-

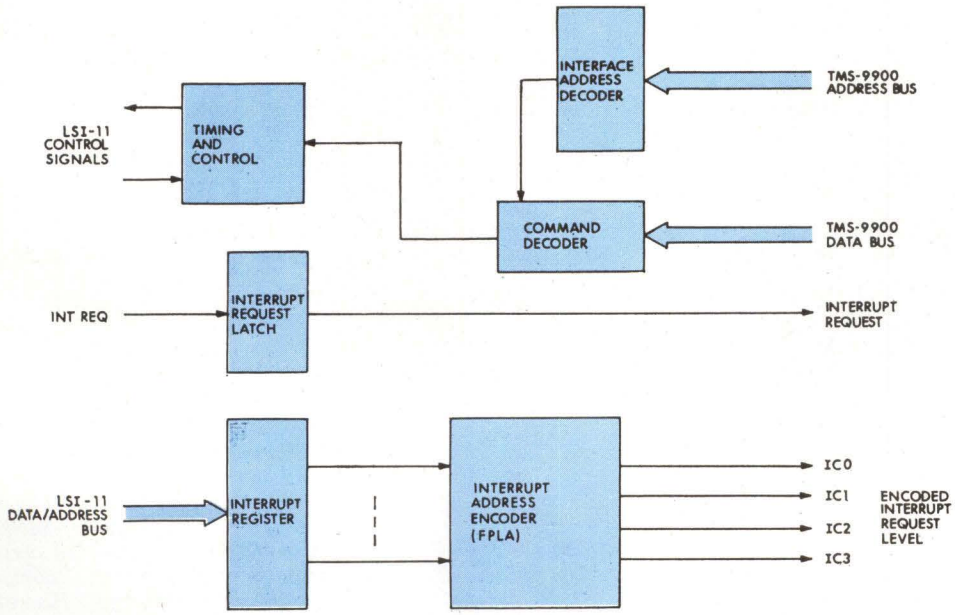


Fig 8 TMS 9900 hardware interface module to LSI-11 interrupt structure. This interface module facilitates TMS 9900 software interface to LSI-11 interrupt structure by carrying out 9900 commands, simulating LSI-11 interrupt transaction handshake signals, and encoding interrupt address vector into 4-bit interrupt identification code (IC0 to IC3)

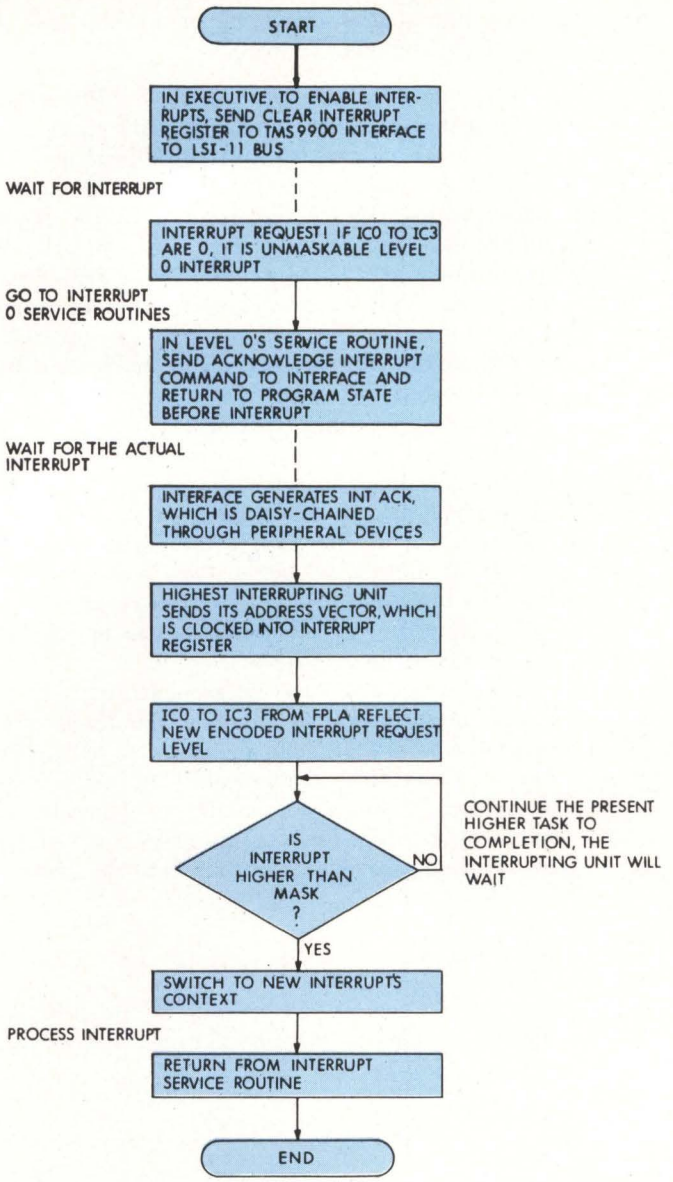


Fig 9 Flowchart for software module needed to interface TMS 9900 to LSI-11 interrupt structure. To assure that low priority peripheral does not interrupt higher priority task, device must be identified and its priority compared with present task. This is accomplished by short "unmaskable interrupt 0 routine" which acknowledges interrupt. Since highest interrupting unit responds, its priority level (IC0 to IC3) can be compared to present task before relinquishing processor control

proach identifies five functional phases in the interrupt transaction, and the unique system implementation of each of these phases optimizes that system for a particular range of applications. The pragmatic approach sees interrupts as techniques for handling asynchronous events at four system operating levels and seeks to optimize interrupt transactions at each of these levels. An integrative approach tries to generate an interrupt structure that optimizes throughput at all four operating levels for multiprocessor systems. Two design examples demonstrate that it is possible to design an optimum interrupt structure and then to integrate commercially available processors into this structure.

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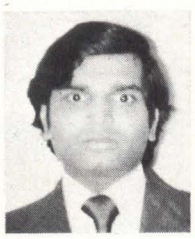

Rajen Jaswa holds B Tech and M Eng degrees in electrical engineering from the Indian Institute of Technology, Bombay, and the University of Toronto, respectively. Currently a digital design engineer at General Electric, he is involved in the design of special purpose high speed processors for computer generated image systems. His experience includes design of multimicroprocessor systems and microprocessor based products.

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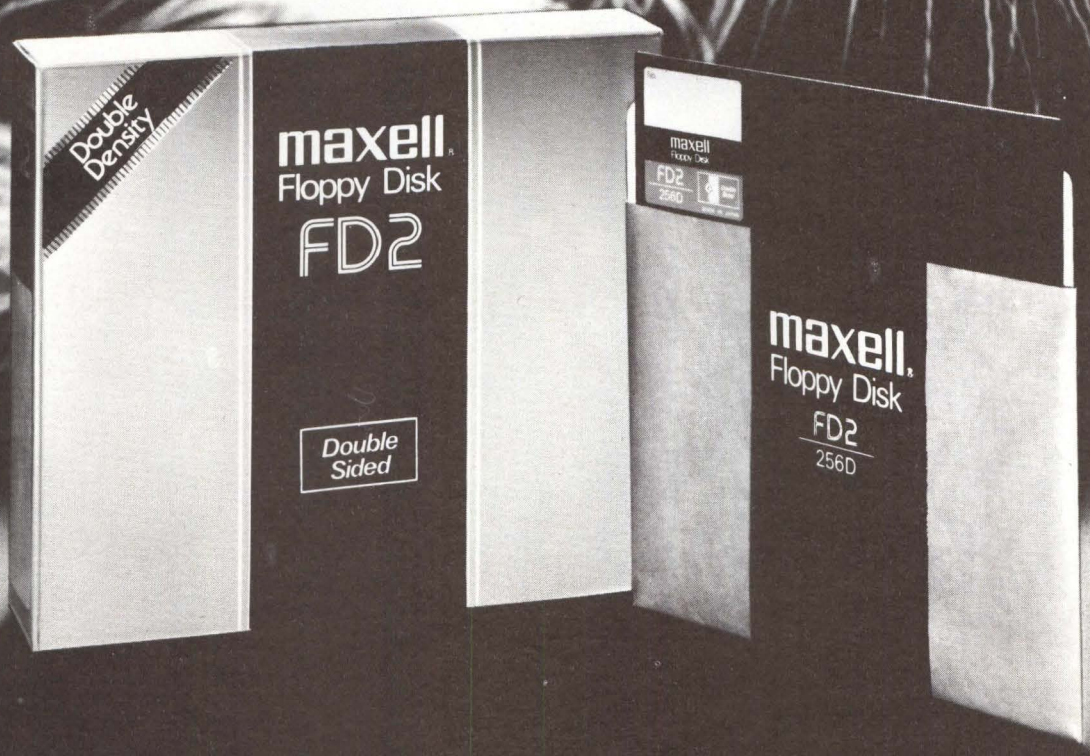

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INTERPRETATION OF DATA CONVERTER ACCURACY SPECIFICATIONS

Cognizance of accuracy factors involved when interfacing data converters into system applications permits designers to meet overall error budget constraints. Transfer functions; quantization noise; offset, gain, and linearity errors; and temperature effects must be interpreted to satisfy specification requirements

Eugene L. Zuch Datel Systems, Incorporated, Canton, Massachusetts

Analog-to-digital and digital-to-analog converters are widely utilized to interface between the physical world of analog measurements and the computational world of digital computers. Dating from the early 1950s, the application of data converters has increased enormously as the use of minicomputers and microcomputers has grown. Typical applications of data converters involve the areas of process control and measurement where the inputs and outputs of the system must be in analog form, yet the computation and control functions are performed digitally. In such a system, input variables such as temperature, flow, pressure, and velocity must be converted into electrical form by a transducer, then amplified and converted into digital form by an analog-to-digital converter for the computer to process.

Since the computer not only measures and determines the state of a process, but also controls it, its computations must be employed to close the loop around the system. This is done by causing the computer to actuate inputs to the process itself, thus controlling its state. Because the actuation is done by analog control parameters, the output of the digital computer must be converted into analog form by a digital-to-analog converter. Such a closed loop feedback control system is shown in Fig 1.

Interfacing by analog-to-digital (A-D) and digital-to-analog (D-A) converters performs a vital role. At the present time, it is estimated that at least 15% of all microcomputers function in such control and measurement applications where data converters are required; this percentage is expected to grow to about 40% within a few years. For the designer of such computer controlled systems, it is fortunate that a broad choice of data converters exists. In fact, a virtual supermarket of A-D and D-A converters of all prices, sizes, and performance specifications is available. This spectrum of converters encompasses those from simple 8-bit monolithic devices costing a few dollars, through better performing hybrid devices with higher resolution, to higher cost discrete module converters with the best performance characteristics.

Design selection involves not only price and size, but also many facets of performance: resolution, linearity, temperature coefficient, speed, and various self-contained options. In the realm of A-D converters (ADCs), there is also the choice between basic conversion methods, such as successive approximation, dual-slope integrating, and parallel (or flash) techniques. Furthermore, there exists a choice between three competing technologies: monolithic, hybrid, and modular, each with its own specific advantages. Since A-D and D-A converters are basically analog circuits that have digital inputs or outputs, the computer systems engineer who may be mostly familiar with digital techniques must become familiar

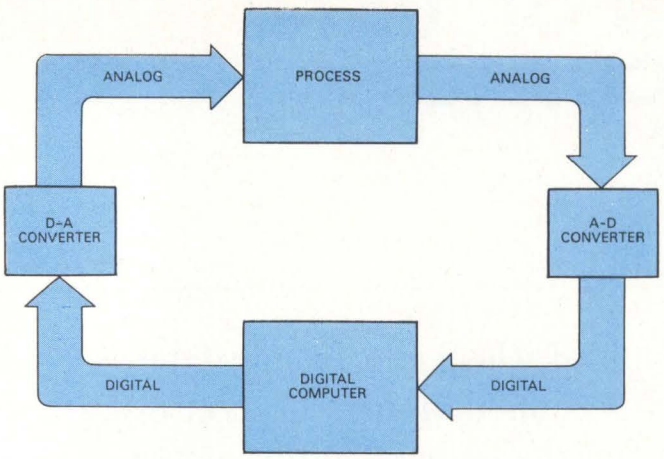


Fig 1 Computer controlled feedback control system. Computer closes loop around process to control its state. However, two interfaces are required: A-D converter and D-A converter

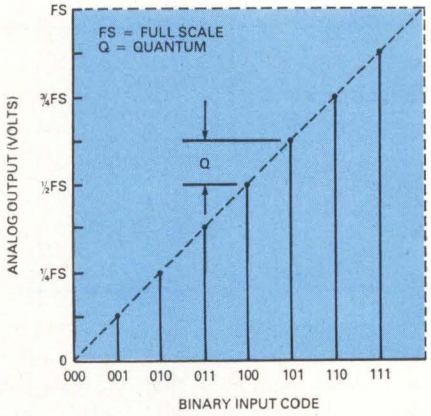


Fig 2 Ideal DAC transfer function. This I/O graph is shown for 3-bit DAC which has one-to-one correspondence between input and output

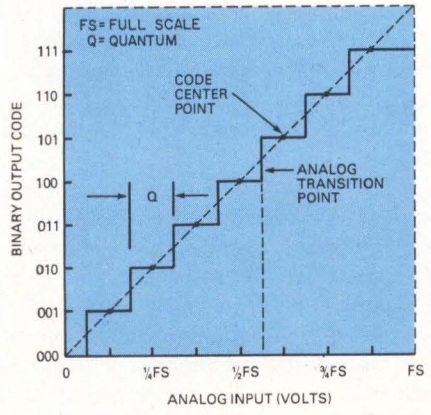


Fig 3 Ideal ADC transfer function. I/O graph illustrates 3-bit ADC which has quantized characteristic

with the many analog specifications describing data converter performance in order to choose the correct converter for a specific requirement.

Data Converter Transfer Functions

Fig 2 shows the transfer function of an ideal 3-bit D-A converter (DAC). This converter is assumed to be of the parallel type, as are virtually all DACs in use today. A parallel DAC responds simultaneously to all digital input lines whereas a serial DAC responds sequentially to each digital input. The transfer function representing a 3-bit DAC is a discontinuous function; its analog output voltage or current changes only in discrete analog steps, or quanta, rather than continuously. However, a one-to-one correspondence exists between the binary input code and the analog output value. For each input code there is one, and only one, possible output value. Analog step magnitude, or quantum, is shown as Q.

The horizontal axis is the input binary code, in this case a 3-bit code, increasing from 000 to 111. The number of output states, or quanta, is 2^n, where n is the number of bits in the code. For a 3-bit DAC, the number of states is 2^3 or 8; for a 12-bit DAC, the number of states is 2^{12} or 4096.

Fig 3 illustrates the transfer function for an ideal 3-bit ADC. This transfer function is also discontinuous but without the one-to-one correspondence between input and output. An ADC produces a quantized output from a continuously variable analog input. Therefore, each output code word corresponds to a small range (Q) of analog input values. The ADC also has 2^n output states and $2^n - 1$ transition points between states; Q is the analog difference between these transition points.

For both ADCs, Q represents the smallest analog difference that the converter can resolve. Thus, it is the resolution of the converter expressed in analog units. Resolution for an A-D or D-A converter, however, is commonly expressed in bits, since this defines the number of

TABLE 1

Summary of Data Converter Characteristics

Resolution (n)	States (2^n)	Binary Weight (2^{-n})	Q for 10 V FS	S/N Ratio (dB)	Dynamic Range (dB)	Max Output for 10 V FS (V)
4	16	0.0625	0.625 V	34.9	24.1	9.3750
6	64	0.0156	0.156 V	46.9	36.1	9.8440
8	256	0.00391	39.1 mV	58.9	48.2	9.9609
10	1024	0.000977	9.76 mV	71.0	60.2	9.9902
12	4096	0.000244	2.44 mV	83.0	72.2	9.9976
14	16384	0.0000610	610 μV	95.1	84.3	9.9994
16	65536	0.0000153	153 μV	107.1	96.3	9.9998

states of the converter. A converter with a resolution of 12 bits, then, ideally resolves 1 part in 4096 of its analog range.

For an ideal ADC or DAC, Q has the same value anywhere along the transfer function. This value is $Q = FSR/2^n$, where FSR is the converter's full-scale range—the difference between the maximum and minimum analog values. For example, if a converter has a unipolar range of 0 to 10 V or a bipolar range of −5 to 5 V, FSR in both cases is 10 V. Q is also referred to as one least significant bit (LSB), since it represents the smallest code change the converter can produce, with the last bit in the code changing from 0 to 1 or 1 to 0.

Notice in the transfer functions of both A-D and D-A converters that the output never reaches full scale. This results because full scale is a nominal value that remains the same regardless of the resolution of the converter. For example, assume that a DAC has an output range of 0 to 10 V; then 10 V is nominal full scale. If the converter has an 8-bit resolution, its maximum output is 255/256 x 10 V = 9.961 V. If the converter has 12-bit resolution, its maximum output voltage is 4095/4096 x 10 V = 9.9976 V.

In both cases, maximum output is one bit less than indicated by the nominal full-scale voltage. This is true because analog zero is one of the 2^n converter states; therefore, there are only $2^n - 1$ steps above zero for either an A-D or D-A converter. To actually reach full scale would require $2^n + 1$ states, necessitating an additional coding bit. For simplicity and convenience then, data converters always have the analog range defined as nominal full scale rather than actual full scale for the particular resolution implemented.

In the transfer functions of Figs 2 and 3, a straight line is passed through the output values in the case of the DAC and through the code center points in the case of the ADC. For the ideal converter, this line passes precisely through zero and full scale. Table 1 summarizes the characteristics of the ideal A-D or D-A converter for the most commonly applied resolutions.

Quantization Noise and Dynamic Range

Even an ideal A-D or D-A converter has an irreducible error, which is quantization uncertainty or quantization noise. Since a data converter cannot distinguish an analog difference less than Q, its output at any point may be in error by as much as $\pm Q/2$.

Fig 4(a) shows an ideal ADC and an ideal DAC that digitize and then reconstruct an analog slow-voltage ramp signal. The ADC and output register are both triggered together so that the DAC is updated in synchronism with the A-D conversions. The DAC output ramp is identical with the analog input ramp except for the discrete steps in its output (not counting time delay). If the output ramp is subtracted from the input ramp as shown, the difference is the quantization noise—a natural result of the conversion process. This noise [Fig 4(b)] is simply the difference between the transfer function and the straight line shown in Fig 3. Quantization noise from an ideal conversion is therefore a triangular waveform with a peak-to-peak value of Q.

As with most noise sources, the average value is zero, but the rms value is determined from the triangular shape to be E_n (rms) $= Q/\sqrt{12}$. Thus, a data conversion system can be thought of as a simple signal processor that adds noise to the original signal by virtue of the quantization process. Since this noise is an inherent part of the conversion process, it cannot be eliminated except with a converter of infinite resolution. The best that can be done, even with ideal converters, is to reduce it to a level consistent with desired system accuracy. This is done by using a converter with sufficiently high resolution.

In many computerized signal processing applications, it is necessary to determine the signal-to-noise (S/N) ratio, which is a power ratio expressed in decibels. It can be found from the ratio of peak-to-peak signal to rms noise as follows.

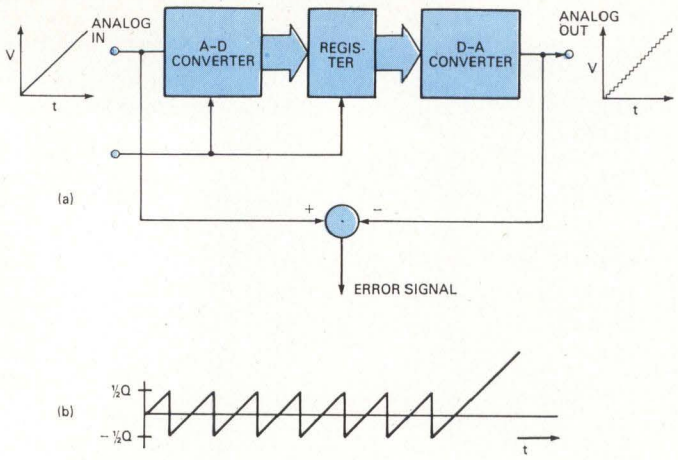


Fig 4 Signal digitization and reconstruction (a) and quantization noise (b). Quantization noise is shown as difference between input and output for ideal data conversion system

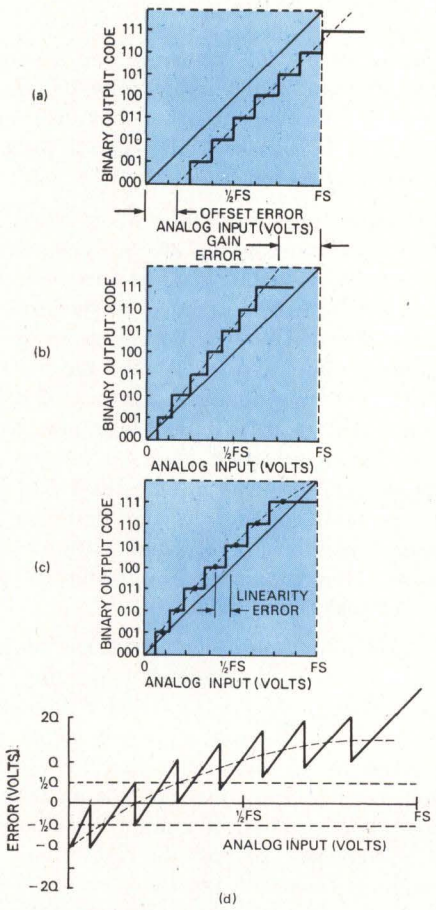


Fig 5 Errors in nonideal A-D converters. Transfer functions are shown for ADCs with offset error (a), gain error (b), and linearity error (c). ADC with all three errors present will have quantization error as shown in (d)

$$\text{S/N Ratio (dB)} = 10 \log \left[\frac{2^n Q}{Q/\sqrt{12}}\right]^2 = 20 \log 2^n + 20 \log \sqrt{12}$$
$$= 6.02n + 10.8 \qquad (1)$$

The S/N ratio increases by a factor of about 6 dB for each additional bit of resolution.

Dynamic range of a data converter, another useful term, is found from the ratio of FSR to Q. This ratio is the same as the number of converter states.

$$\text{Dynamic Range (dB)} = 20 \log 2^n = 20n \log 2 = 6.02n \qquad (2)$$

Therefore, simply multiplying the number of bits of resolution by 6 dB gives the dynamic range. S/N ratio and dynamic range are summarized for the most popular resolutions in Table 1.

Nonideal Data Converters

Real A-D and D-A converters exhibit a number of departures from the ideal transfer functions just described. These departures include offset, gain, and linearity errors (Fig 5), all of which appear simultaneously in any given data converter. In addition, the errors change with both time and temperature. In Fig 5(a), the ADC transfer function is shifted to the right from the ideal function. This offset error is defined as the analog value by which the transfer function fails to pass through zero; it is generally specified in millivolts or in percent of full scale.

In Fig 5(b), the converter transfer function has a slope difference from the ideal function. This gain, or scale factor, error is defined as the difference in full-scale values between the ideal and actual transfer functions when the offset error is zero; gain error is expressed in percent.

An ADC transfer function in Fig 5(c) exhibits linearity error, a curvature from the ideal straight line. Linearity error, or nonlinearity, is the maximum deviation of the transfer function from a straight line drawn between zero and full scale; it is expressed in percent or in LSBs (such as ±½ LSB). Fig 5(d) shows the total error of a nonideal

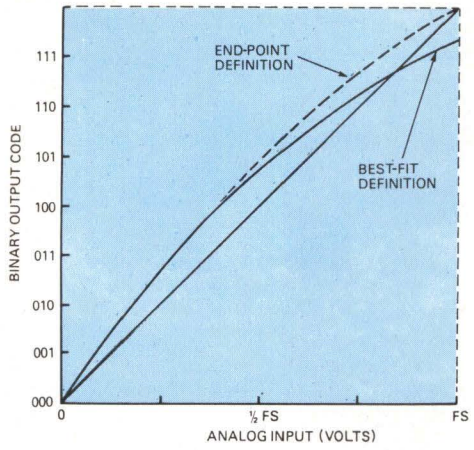


Fig 6 Comparison of linearity error definitions. Curves illustrate end-point and best-fit definitions of linearity error in an ADC

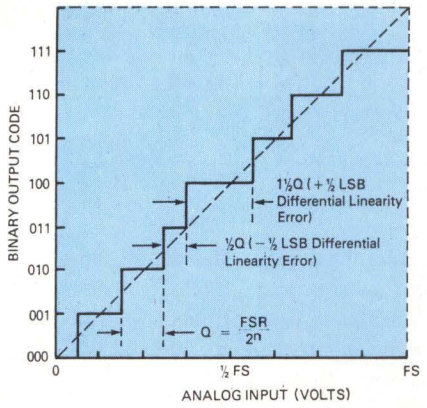


Fig 7 Definition of differential linearity error. This transfer function illustrates ±½ LSB differential linearity errors. Differential linearity error of zero means that every step in transfer function has size of precisely Q

ADC, which contains offset, gain, nonlinearity, and quantization errors. Compare this curve with that of Fig 4(b).

Fortunately, most A-D and D-A converters on the market today have provision for trimming out the initial offset and gain errors. By means of two simple external potentiometer adjustments, the offset and gain errors can be virtually reduced to zero or within the limits of measurement accuracy. Then, only the linearity error remains.

Nonlinearity

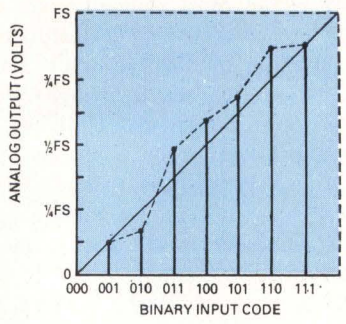
Linearity error is the most difficult error to deal with since it cannot be eliminated by adjustment. Like quantization error, it is an irreducible error. Basically, there are just two methods to reduce linearity error, both of which are expensive: either use a higher quality converter with better linearity, or perform a digital error correction routine on the data using a computer. The latter, of course, may not be feasible in many applications. There is some merit in using a more expensive converter, however. For example, suppose that an ultralinear 8-bit ADC is required. Most good quality converters have linearity errors specified to less than ±½ LSB. If a more expensive 12-bit ADC is employed with only 8 output bits used, then its linearity error of ±½ LSB out of 12 bits is the same as ±1/32 LSB out of 8 bits. This converter, therefore, becomes an ultralinear 8-bit ADC and probably at not too great an additional cost.

Actually, two types of linearity errors existing in A-D and D-A converters are integral linearity error and differential linearity error. Integral linearity error in Fig 5(c) is due to the curvature of the transfer function, resulting in departure from the ideal straight line. The definition given for integral linearity error as the maximum deviation of the transfer function from a straight line between zero and full scale is a conservative one used by most data converter manufacturers. It is an "end-point" definition, as contrasted with the normal definition of linearity error as the maximum deviation from the "best-fit" straight line.

Since determining the best-fit straight line for data converters can be a tedious process when calibrating the device, most manufacturers have opted for the more conservative definition. This means that the converter must be aligned accurately at zero and at full scale to realize the specified linearity. The end-point definition can mean a linearity that is twice as good as a best-fit definition, as illustrated in Fig 6. Notice that the curvature may be twice as great with the best-fit straight line definition.

Differential linearity error is the amount of deviation of any quantum from its ideal value. In other words, it is the deviation in the analog difference between two adjacent codes from the ideal value of FSR/2^n. If a data converter has ±½ LSB maximum differential linearity error, then the actual size of any quantum in its transfer function is between ½ LSB and 1½ LSB; each analog step is 1 ±½ LSB. Fig 7 illustrates the definition. The first two steps shown are the ideal value Q = FSR/2^n. The next step is only ½Q, and above this is 1½Q. These two steps are at the limit of the specification of ±½ LSB maximum differential linearity error. Most data converters today are specified in terms of both integral and differential linearity error. In production testing of data converters, quanta sizes are measured over the converter's full-scale range.

Two other important terms are commonly used in conjunction with the differential linearity error specification. The first is monotonicity, which applies to DACs. A monotonic DAC has an analog output that is a continuously increasing function of the input. The DAC transfer function shown in Fig 8(a) is monotonic even though it has a large differential linearity error. The transfer



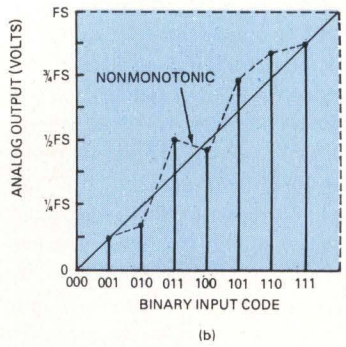
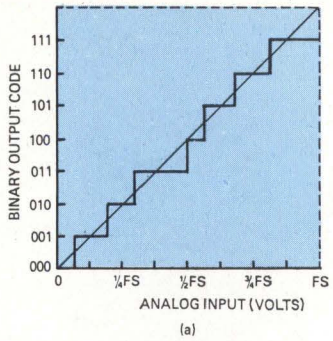


Fig 8 Monotonic (a) and nonmonotonic (b) DAC outputs. Monotonicity means output is continuously increasing function of input



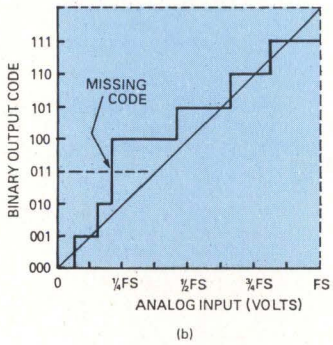


Fig 9 No missing code (a) and missing code (b) in ADC output. Differential linearity error of less than ±1 LSB assures that there are no missing codes in transfer function

function of Fig 8(b), on the other hand, is nonmonotonic since the output actually decreases at one point. In terms of differential linearity error, a DAC may go nonmonotonic if the differential linearity error is greater than ±1 LSB at some point; if the differential linearity error is less than ±1 LSB, it assures that the output is monotonic.

The term missing, or skipped, code applies to ADCs. When the differential linearity error of an ADC is greater than ±1 LSB, the output may have a missing code; if the differential linearity error is less than ±1 LSB, it assures that there are no missing codes. Fig 9(a) shows the transfer function of an ADC with a large differential linearity error but with no missing codes. In Fig 9(b), however, the differential linearity error causes a code to be skipped in the output.

For ADCs, the linearity characteristic depends on the technique of A-D conversion used; each converter type exhibits its own specific nonlinearity characteristic. Fig 10 illustrates the nonlinearity characteristics of the two most popular types of ADCs: successive approximation and dual-slope integrating. With the successive approximation ADC, and also with other feedback type ADCs that use a parallel input DAC in the feedback loop, differential linearity error is the dominant type of nonlinearity. This is due to the parallel input DAC, which is made up of weighted current sources. The worst differential linearity errors occur at the major code transitions, such as ¼, ½, and ¾ scale. If these differential linearity errors are small, then the integral linearity error will also be small.

The difficulty at the major transition points is that, for example, the most significant bit current source is turning on while all other current sources are turning off. This subtraction of currents must be accurate to ±½ LSB and is a severe constraint in high resolution DACs. This means that the weighted current sources must be precisely trimmed in manufacturing. The most difficult transition is at ½ scale, where all bits change state (eg, for an 8-bit converter, 01111111 to 10000000), and the worst differential linearity error generally occurs here.

The next most difficult transitions occur at ¼ scale and ¾ scale, where all but one of the bits change state (eg, for an 8-bit converter, 00111111 to 01000000 and 10111111 to 11000000, respectively). Relatively smaller differential linearity errors may also occur at the ⅛, ⅜, ⅝, and ⅞ scale transitions, and so on. Fig 10(a) shows a successive approximation ADC transfer function, illustrating exaggerated differential linearity errors at ¼, ½, and ¾ scale. If these errors are properly trimmed out in manufacturing, then both differential and integral linearity errors will be less than ±½ LSB.

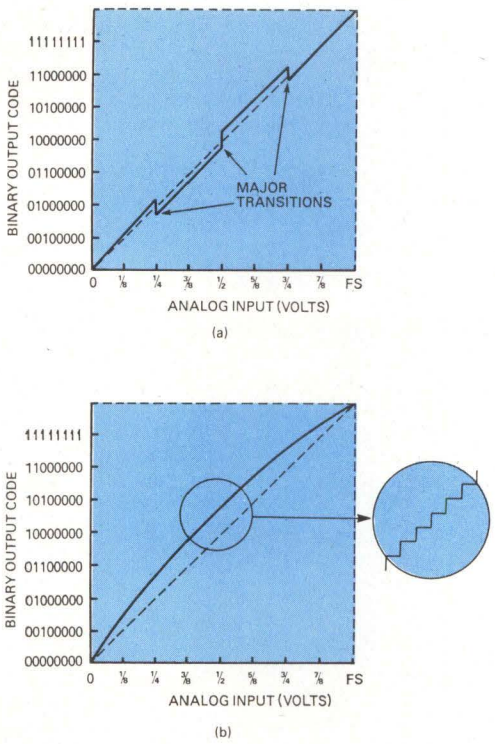


Fig 10 Linearity characteristic of successive approximation (a) and dual slope integrating (b) ADCs. Transfer function of successive approximation converter exhibits mostly differential linearity error while that of integrating converter shows mostly integral linearity error

Fig. 10(b) shows a dual-slope integrating ADC transfer function. In this case, the predominant nonlinearity is the integral linearity error; differential linearity error is almost nonexistent in integrating type ADCs, which also includes charge balancing ADCs. The curvature of the transfer function is caused by a nonideal integrator circuit. Differential linearity is determined by the time between clock pulses in the converter, and this is constant within any conversion cycle.

Temperature Induced Errors

Ambient temperature changes cause variations in offset, gain, and linearity errors. If a converter is operated at a constant temperature within its specified operating temperature range, offset and gain errors can be zeroed by external adjustment at that temperature. But if the converter must operate with changing ambient temperature, then the problem becomes acute.

Offset change with temperature is generally specified in microvolts per degree Celsius, or in parts per million of full scale per degree Celsius. Gain temperature coefficient is specified in parts per million per degree Celsius, and linearity error change with temperature is expressed in parts per million of full scale per degree Celsius.

Effective aproaches to minimizing gain and offset changes with temperature are available. If a converter operates most of the time at a given temperature, then its offset and gain should be zeroed at that temperature. If, however, the ambient temperature varies between two temperatures, the converter should be calibrated midway between those two temperatures. Another approach to minimizing changes with temperature is to use a converter with a low temperature coefficient to meet the desired specification. Data converters with low temperature coefficients are, of course, more expensive, but this may be the most economical solution to the problem when all design factors are considered. Another method of minimizing gain error is based on the fact that many data converters with internal references have provision for connecting an external reference. In such a case, it is possible to connect a lower temperature coefficient external reference to the converter. This can be particularly effective where a number of converters are used together and one reference is used for all of them.

Linearity error temperature coefficient is the most troublesome specification, since it resists correction. In many applications, it is desired that the converter be

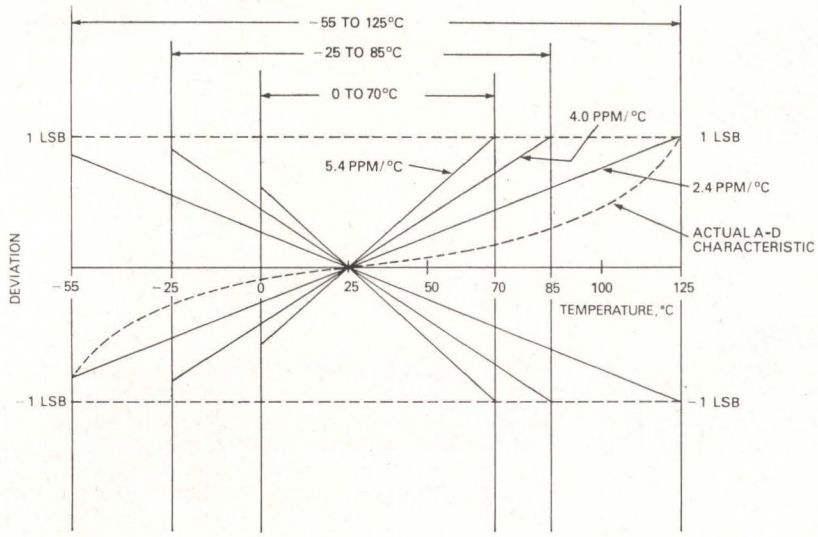


Fig 11 Butterfly gain tempco characteristic for 12-bit ADC with ±1 LSB maximum gain error. Converter is calibrated for zero gain error at 25 °C. Limits shown are for ±1 LSB error out of 12 bits over designated temperature range

monotonic, or have no missing codes, over the desired operating temperature range. From the converter differential linearity temperature coefficient, it is useful to determine the temperature range over which the converter will have guaranteed monotonicity or no missing codes. Using a conservative approach, it is assumed that the converter has a maximum initial differential linearity error of ±½ LSB. Then, if the differential linearity error changes by not more than an additional ½ LSB, a DAC will remain monotonic and an ADC will have no missing codes.

With a 12-bit ADC for example, ½ LSB is equal to 120 ppm. If the operating temperature range is 0 to 70 °C and the converter is calibrated at 25 °C, the maximum temperature change is 70 °C − 25 °C, or 45 °C. To guarantee no missing codes, the differential linearity temperature coefficient must be 120 ppm/45 °C = 2.7 ppm/°C of full scale, maximum. An even lower differential linearity temperature coefficient is required to assure no missing codes if the operating temperature range is the full −55 °C to 125 °C military range. Performing a similar computation gives 120 ppm/100 °C = 1.2 ppm/°C of full scale, maximum, for the differential linearity temperature coefficient.

Gain temperature coefficient is commonly specified by the butterfly limits shown in Fig 11. All the lines pass through zero at 25 °C, where it is assumed that the initial measurement is made. The graph of Fig 11 shows the maximum gain temperature coefficient required for a ±1 LSB gain error for a 12-bit A-D or D-A converter over three different temperature ranges. Observe that the gain deviation curve must be within the bounds shown to meet the specification of ±1 LSB maximum change. The dotted curve shows an actual converter gain deviation that would qualify as a gain temperature coefficient of ±2.4 ppm/°C over the −55 to 125 °C operating temperature range. This represents a very low temperature coefficient for an actual converter since most available devices fall in the range of 5 to 50 ppm/°C.

Error Budget Summary

A common mistake in specifying data converters is to assume that the relative accuracy of a converter is determined only by the number of resolution bits. In fact, achievable relative accuracy is likely to be far different from the implied resolution, depending on the converter specifications and operating conditions. This simply means that the last few resolution bits may be meaningless in terms of realizable accuracy.

The best way to attack this design problem is with a systematic error budget. An error budget partitions all possible errors by source to arrive at a total error. In a given system, this must be done not only for the A-D or D-A converter, but also for the other circuits, such as transducer, amplifier, analog multiplexer, and sample and hold.

As an example, using the accuracy specifications for a typical 12-bit ADC (Table 2), an error budget can be determined based on the following assumptions: operating temperature range of 0 °C to 50 °C, maximum

TABLE 2

Accuracy Specifications for 12-Bit ADC

Characteristic	Value
Resolution	12 Bits
Differential Linearity Error	±½ LSB max
Differential Linearity Tempco	±2 ppm/°C of FSR max
Gain Tempco	±20 ppm/°C max
Offset Tempco	±5 ppm/°C of FSR max
Power Supply Sensitivity	0.002%/%

TABLE 3

Error Budget for 12-Bit ADC

Specification	Error (%)
Quantization Error (±½ LSB)	0.012
Differential Linearity Error (±½ LSB)	0.012
Differential Linearity Error over Temp (2 ppm/°C x 25)	0.005
Gain Change over Temp (20 ppm/°C x 25)	0.05
Zero Change over Temp (5 ppm/°C x 25)	0.0125
Change with Power Supply (1 x 0.002%)	0.002
Long Term Change	0.02
Total Error, Worst Case	0.1135
Total Statistical (rms) Error	0.0581

power supply voltage change of 1% with time and temperature, and maximum converter change of 0.02% with time. Table 3 shows the resulting error budget with a total worst case error of 0.1135%. It is improbable that the errors will all add in one direction. Statistical (rms) addition of the errors yields a lower value of 0.0581%; this, on the other hand, may be too optimistic since the number of error sources is small. At any rate, the maximum error will be somewhere between 0.0581% and 0.1135%, a significant difference from what might be assumed as a 12-bit or 0.024% converter. The ideal relative accuracy has been degraded by one to two resolution bits.

In applying data converters, best results are achieved by reading the data sheet carefully for accuracy specifications, computing total error by the error budget method, and then carefully aligning and testing the converter in its actual application.

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TECH NOTE

Design/Application Considerations of Sealed vs Nonsealed Fixed-Head Disc Units

In nonpressurized fixed-head memory systems, the design choice between sealed and air-breathing disc units involves packaging and maintenance aspects in addition to the obvious environmental considerations

Mark Mougel Dataflux Corporation, Sunnyvale, California

In many data storage applications, fixed-head disc storage has significant advantages over both moving-head and floppy disc systems. Large data storage capacity in a relatively compact amount of space, rugged construction for operation under severe environmental conditions, and sealed packaging for applications in corrosive or pressure critical environments are all benefits of fixed-head disc storage.

Several units are available that are sealed and pressurized with an inert gas, but, in general, gas pressurization tends to create problems. Sealed disc units are difficult to maintain, must be periodically purged and refilled, and have a higher risk of sudden failure due to the possibility of leaks. Additionally, modern safety regulations increase the difficulty of shipping pressurized containers aboard aircraft. Nonpressurized sealing does not have these disadvantages, yet such seals are still relatively impervious to corrosive atmospheres, humidity, and particle contamination—all of which can cause catastrophic failures in unsealed devices.

In the absence of environmental constraints that make sealing or pressurizing absolutely necessary, design decisions must determine whether a fixed-head disc storage unit should be sealed or air-breathing. The selection depends on several design considerations, some construction oriented, such as whether to use plated or oxide-coated media, and contact or noncontact stop/start heads; and others that are related to operation and maintenance. Design and functional considerations, along with their impact on reliability, crash resistance, and product complexity are factors which directly affect both acquisition and maintenance cost, and should be carefully weighed by disc manufacturers and system designers.

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CIRCLE 55 ON INQUIRY CARD

Comparison of Air-Breathing Vs Sealed Disc Design

Design/Application Considerations	Air-Breathing Disc	Sealed Disc
Contact start/stop head	Self-cleaning	Contaminates unit
Noncontact start/stop head	No advantage	Eliminates filtering
Corrosive atmospheres	Not acceptable	Mandatory
Pressure differentials	Eliminates problem	Requires either pressure seal or equalization through leakage
Maintenance	Requires periodic maintenance	No periodic maintenance
Dirt and dust environment	Plugs filters	No problem
Humidity in environment	Enters unit	No problem
Installation	Requires clear air passage	No special mounting
Construction	Requires air passages, filter mounting, and exhaust	Simplified
Cost	Higher cost	Lower cost
Noise	Relatively higher	Relatively lower
Size	Usually larger	Usually smaller

the disc/head container. In part, the final decision involves an examination of the relative merits of one disc surface over the other.

Until recently, almost all head-per-track discs used plated surfaces, mostly nickel-cobalt, with or without a hardening overcoat. But with the advent of the IBM 3330 design, which uses an oxide disc, there has been some movement toward the use of oxide in fixed-head designs. This movement has accelerated with the availability of the IBM 3340 series Winchester design.

Two main concerns in disc design have been platter surface finish and magnetic uniformity. The disc memory storage industry continuously attempts to reduce storage cost per bit by increasing both linear and radial packing density (bits per inch and tracks per inch). Because of this approach, magnetic uniformity has become increasingly critical. Similarly, since higher densities mean lower flying heights, improving the quality of surface finishes has also become a major concern.

Before the 3330-type platter, the quality of surface finishes discouraged low flying heights necessary for high linear packing density. This difficulty was one of the primary reasons for early concentration on hard-plated platter surfaces. With the 3330, however, and later with the 3350, oxide surfaces have been developed that sustain flying heights as low as 15 μin, adequate for linear densities of over 6k bits/in. Since oxide-surfaced platters are much less expensive than hard-plated ones, the trend toward their use has been expected. Another advantage of the oxide surface, particularly in the lubricated Winchester-type disc, has been its reduced susceptibility to head crashes.

With a disc drive, particularly a fixed-head disc drive, a head crash is usually considered catastrophic, due to the extent of the physical damage to heads and recording surface, and to heavy contamination of the drive with materials abraded from the disc and heads. In the event of a crash, these conditions make further operation of the drive impossible, and unfortunately, they usually mean expensive repair work and lengthy downtime.

A major design goal of fixed-head disc manufacturers has been to reduce the likelihood of crashes, and to minimize the severity of the damage if a crash occurs. With plated discs, various overcoats, such as rhodium, nickel oxide, and silicon monoxide, have been added for extra hardness. They have the double effect of allowing the media to tolerate an occasional head contact at operating speed, and reducing abrasion either by landing heads or foreign particles. However, although this approach reduces the frequency of crashes, it does not reduce damage when a crash occurs.

With oxide media, a different approach has been taken. The oxide coating is fairly soft, and inherently more tolerant of foreign particles, since it does not throw off metal chips when abraded. This same characteristic also makes oxide media more tolerant of an occasional head bounce. In addition, with the use of a surface lubricant, the oxide platter can be made more crash resistant.

These advantages have been incorporated by the IBM Winchester-type drives and CDC storage module drives in which crashes almost never occur. When they do, physical damage is usually limited to the media surface itself, and contamination is easily removed with a cleaning solvent. Secondary benefits also exist for using oxide media. For instance, it results in a disc of lighter weight due to thinner substrate. Other ad-

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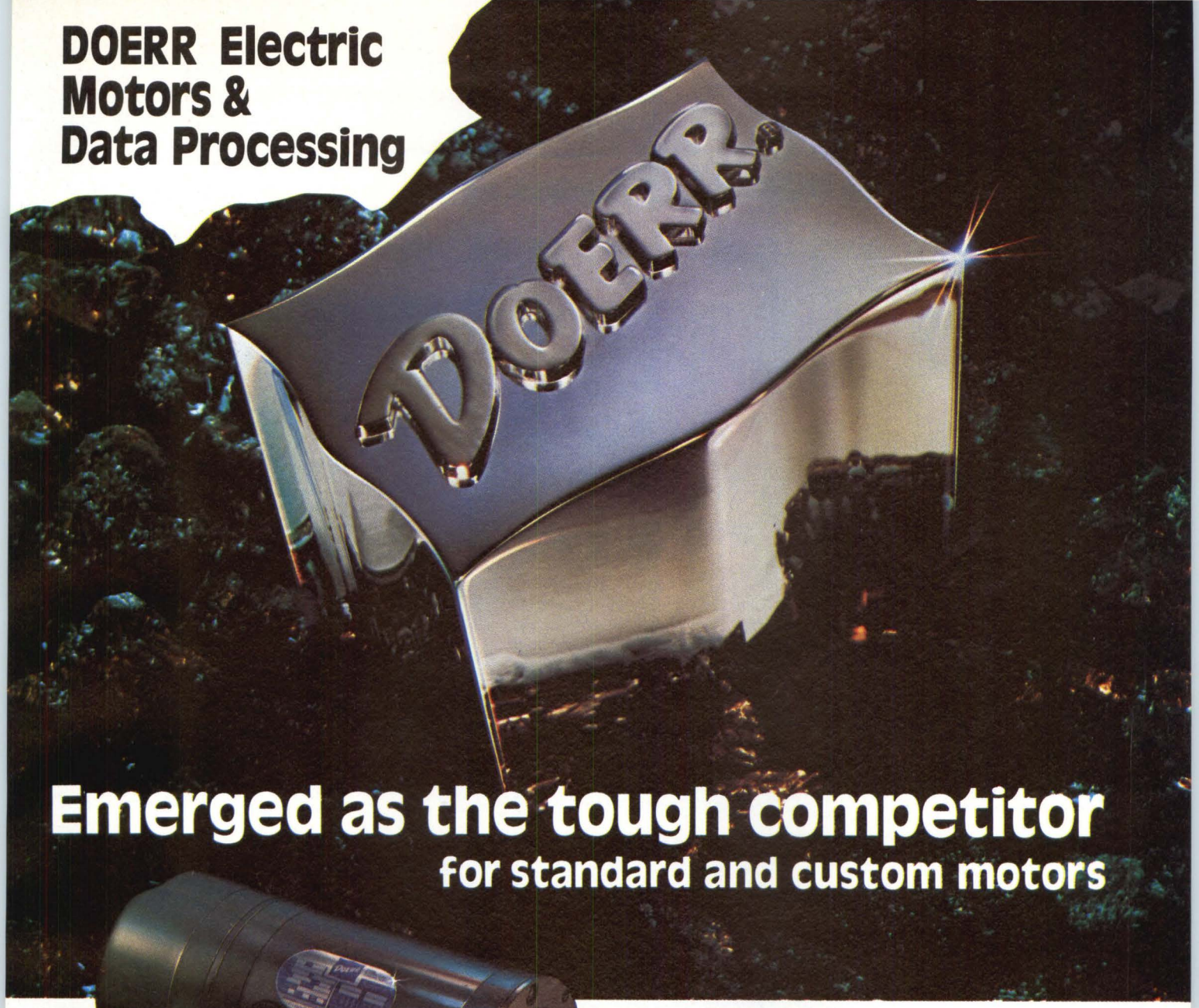

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CIRCLE 56 ON INQUIRY CARD

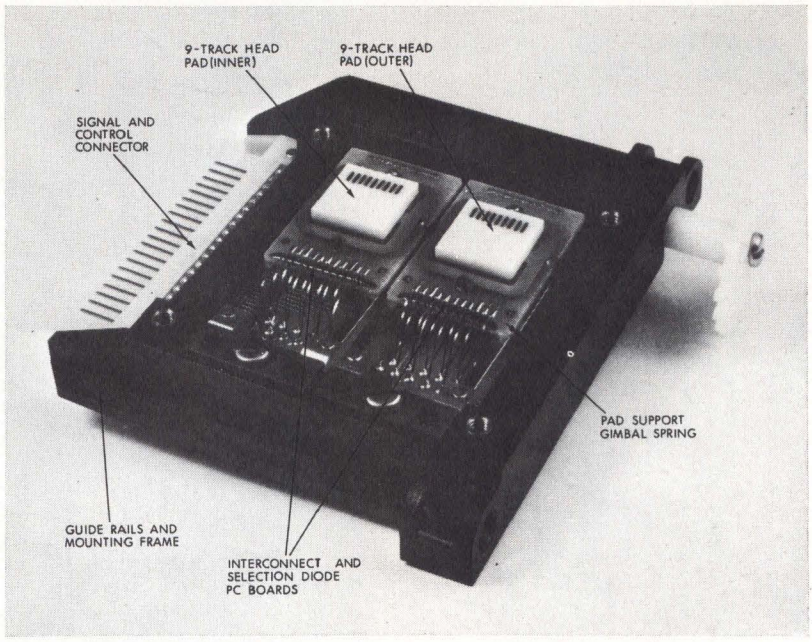

Fig 1 R/W head subassemblies of noncontact stop/start type for use on oxide surface. Shown are head pads with 16 R/W heads mounted on support gimbals, and wired to circuit boards containing head-selection diode matrix. Module plugs into cartridge shown in Fig 2

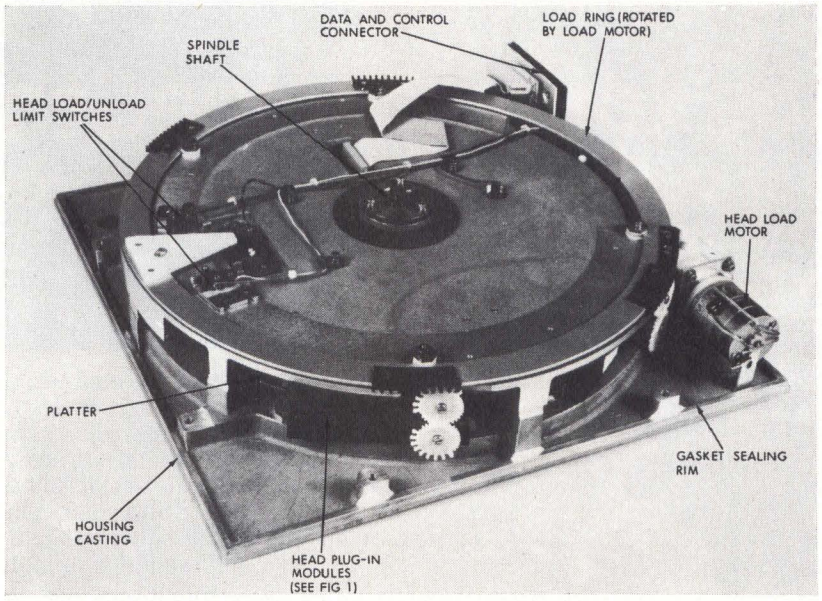

Fig 2 Fixed-head cartridge with cover removed, showing head-loading mechanism, spindle, Winchester-type media (single platter) and noncontact R/W heads. Mechanism to control head-pad actuation is operated by load motor

vantages include multiple source availability and greatly reduced process and handling problems.

Contact Vs Noncontact Start/Stop Heads

Assuming the designer has selected an oxide disc, such as the Winchester type, the next design question is whether to use contact stop/start heads or some sort of noncontact head lifter arrangement. Note that oxide discs are inherently capable of generating contamination in long-term use, because their relatively soft surfaces (compared to plated disc surfaces) will emit particles if abraded. Of course, a plated disc will also emit particles if abraded enough; but generally, such behavior indicates that a head crash has already occurred, making the evaluation of contamination academic.

If a contact head design is used with an oxide disc, the air flow of an air-breathing disc unit becomes almost mandatory, due to the likely generation of particles after repeated start/stop operation. This built-up dust would eventually cause a crash if allowed to collect at random within the container.

With a noncontact (nonlanding) head stop/start mechanism, however, an air-breathing design is neither advantageous nor necessarily desirable. Whether to use a sealed or air-breathing design essentially remains an open question, subject to the following considerations.

Requirements Affecting Disc Design

Ensuring adequate cooling, stable internal aerodynamics, and acceptable operating noise levels are particularly important objectives in making design choices for a disc unit. Other factors that should be taken into account include the desired physical size of the unit and, significantly, the maintenance and installation requirements which must be met.

The panel shows comparative advantages and disadvantages of air-breathing versus sealed disc units in various design and application areas. For instance, observe that air-breathing units, which involve filtering a constant air flow, do require maintenance on a periodic basis. Sealed units do not.

Similarly, construction requirements for sealed disc units are generally simpler and less expensive than air passages, filter mountings, and exhausts required for air-breathing units. Overall, a sealed disc unit appears to be more advantageous than an air-breathing unit, if a noncontact, stop/start head design is used as in Fig 1. The logical final evolution of design and functional considerations discussed could be a sealed drive with noncontact heads using a Winchester-type oxide platter, all mounted in a cartridge (Fig 2) that is easily replaceable in the field. □

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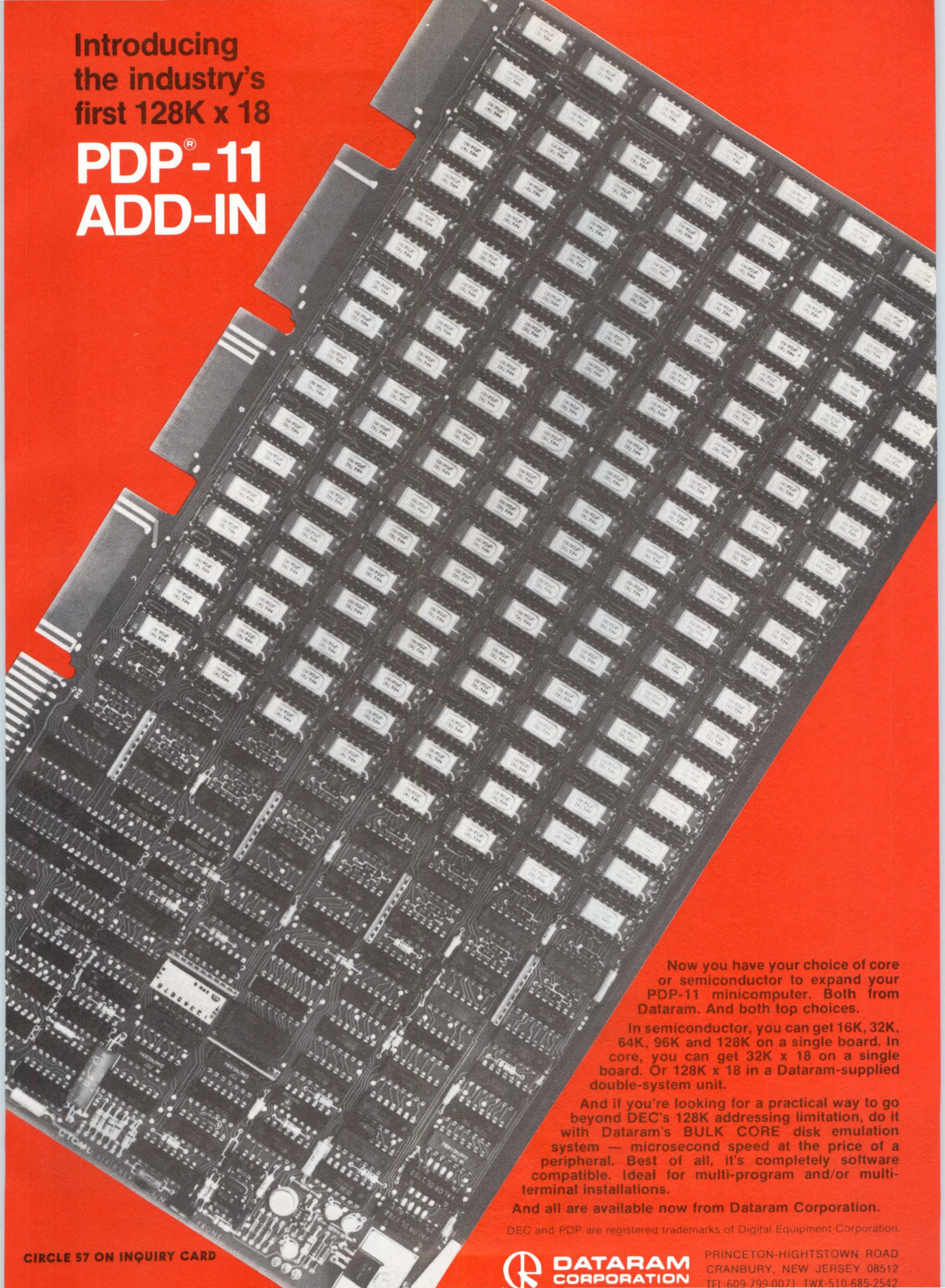

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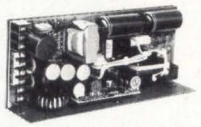
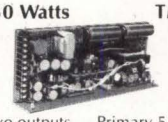
Economical, open-frame, convection-cooled, low-power, 100 - 175 watts, 1 - 4 outputs fully regulated and adjustable, UL-recognized. Input — 92 - 130 V AC or 184 - 260 V AC, 47 - 440 Hz.

100 Watts TM 11



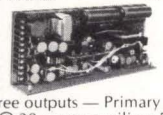
One output — 5 - 28 V DC
9.5" L x 4" W x 2.5" H.

150 Watts TM 22



Two outputs — Primary 5 V DC @ 20 amps; auxiliary 5 - 28 V DC @ up to 8 amps.
12" L x 5.15" W x 2.8" H.

150 Watts TM 23



Three outputs — Primary 5 V DC @ 20 amps; auxiliary 5 - 28 V DC @ up to 5 amps.
12" L x 5.15" W x 2.8" H.

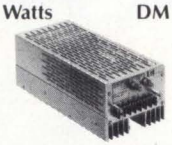
Dyna-MITE™ DM Series

NEW

DC Input

DC input, convection-cooled, medium-power, 250 - 550 watts, 1 - 4 outputs. Input — 42 - 56 V DC.

250 Watts DM 11

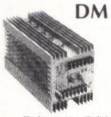


One output — 2 - 28 V DC.
12.12" L x 5.05" W x 4" H.

300 Watts DM 23

Three outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 9 amps.
12.12" L x 5.05" W x 6.45" H.

300 Watts DM 24



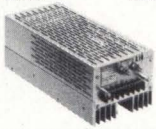
Four outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 5 amps.
12.12" L x 5.05" W x 6.45" H.

Little-MITE™ LM Series

NEW

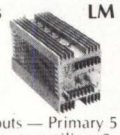
Convection-cooled, medium-power, 250 - 600 watts, 1 - 4 outputs, UL-designed. Input — 92 - 130 V AC or 184 - 260 V AC, 47 - 440 Hz.

250 Watts LM 11



One output — 2 - 28 V DC.
12.12" L x 5.05" W x 4" H.

300 Watts LM 23



Three outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 9 amps.
12.12" L x 5.05" W x 6.45" H.

300 Watts LM 24

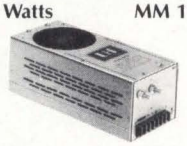
Four outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 5 amps.
12.12" L x 5.05" W x 6.45" H.

Mighty-MITE™ MM Series

UL-Recognized

Fan-cooled, medium-to-high-power, 375 - 750 watts, 1 - 7 outputs, UL-recognized. Input — 115 ±10% V AC or 230 ±10% V AC, 47 - 63 Hz; 115/230 ±10% V AC, 47 - 63 Hz (optional).

375 Watts MM 11



One output — 2 - 28 V DC
12.12" L x 5" W x 3.9" H.

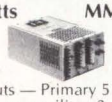
375 Watts MMX 22

Two outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 20 amps.
15.25" L x 5" W x 3.9" H.

375 Watts MM 23

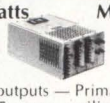
Three outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 10 amps.
15.25" L x 5" W x 3.9" H.

600 Watts MML 46



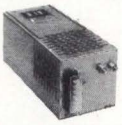
Six outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC: 2nd, 3rd and 4th outputs @ up to 12 amps; 5th and 6th outputs @ up to 5 amps.
13.5" L x 8.5" W x 5.1" H.

600 Watts MML 47



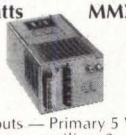
Seven outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC: 2nd and 3rd outputs @ up to 12 amps; 4th, 5th, 6th and 7th outputs @ up to 5 amps.
13.5" L x 8.5" W x 5.1" H.

750 Watts MM 31



One output — 2 - 28 V DC.
12.75" L x 5.1" W x 5.1" H.

750 Watts MMX 42



Two outputs — Primary 5 V DC @ 150 amps; auxiliary 2 - 24 V DC @ up to 24 amps.
13.5" L x 8.5" W x 5.1" H.

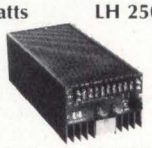
750 Watts MM 43

Three outputs — Primary 5 V DC @ 150 amps; auxiliary 2 - 24 V DC @ up to 12 amps.
12.75" L x 7" W x 5.1" H.

LH Series

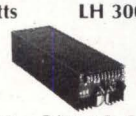
Convection- and fan-cooled, 250 - 1500 watts, 1 - 4 outputs. Input — 115 ±10% V AC or 230 ±10% V AC, 47 - 440 Hz. (externally selectable), 47 - 63 Hz (for LH-700 and LH-800 Series).

250 Watts LH 250S



One output — 2 - 28 V DC.
12.25" L x 5.05" W x 3.65" H.

300 Watts LH 300D

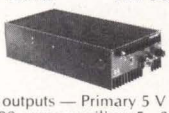


Two outputs — Primary 5 - 24 V DC; auxiliary 5 - 24 V DC @ up to 8 amps.
16.25" L x 5.05" W x 3.65" H.

300 Watts LH 400D

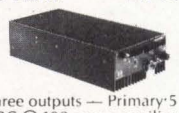
Two outputs — Primary 5 - 24 V DC; auxiliary 5 - 24 V DC @ up to 8 amps.
12.25" L x 7.5" W x 3.9" H.

600 Watts LH 600D



Two outputs — Primary 5 V DC @ 100 amps; auxiliary 5 - 24 V DC @ up to 8 amps.
16.25" L x 7.5" W x 3.9" H.

600 Watts LH 600T



Three outputs — Primary 5 V DC @ 100 amps; auxiliary 5 - 24 V DC @ up to 8 amps.
16.25" L x 7.5" W x 3.9" H.

600 Watts LH 600Q

Four outputs — Primary 5 V DC @ 100 amps; auxiliary 5 - 24 V DC: 2nd and 3rd outputs @ up to 8 amps; 4th output @ up to 2 amps.
16.25" L x 7.5" W x 3.9" H.

600 Watts LH 700S

UL-Recognized

One output — 2 - 24 V DC.
10" L x 8" W x 5" H.

600 Watts LH 700D

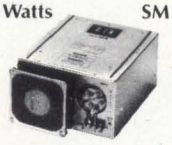
UL-Recognized

Two outputs — Primary 5 V DC @ 120 amps; auxiliary 5 - 24 V DC @ up to 8 amps.
10" L x 8" W x 5" H.

Super-MITE™ SM Series

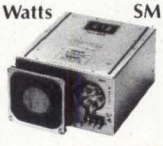
Fan-cooled, high-power, 750 - 1000 watts, 1 - 4 outputs, UL-pending. Input — 85 - 130 V AC or 166 - 260 V AC, 47 - 63 Hz.

750 Watts SM 71



One output — 2 - 28 V DC.
11" L x 8" W x 5" H.

1000 Watts SM 11



One output — 2 - 28 V DC.
11" L x 8" W x 5" H.

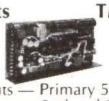
1000 Watts SM 22

Two outputs — Primary 5 V DC @ 150 amps; 2nd output 2 - 28 V DC @ up to 18 amps.
11" L x 8" W x 6" H.

# of switching regulated presents...

LH RESEARCH

175 Watts — TM 34

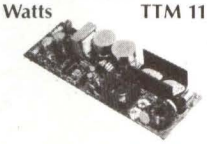


Four outputs — Primary 5 V DC @ 20 amps; 2nd and 3rd outputs 5 - 28 V DC @ up to 5 amps, 4th output 2 - 15 V DC @ up to 1.5 amps.
13" L x 6.15" W x 2.75" H.

Teeny-Tiny-MITE™ TTM Series

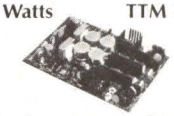
Economical, plug-in printed circuit board switcher, convection-cooled, 75 watts, 1 - 4 outputs, UL-designed. Input — 92 - 130 V AC or 184 - 260 V AC, 47 - 440 Hz.

75 Watts — TTM 11



One output — 5 - 28 V DC.
10.5" L x 3.5" W x 2" H.

75 Watts — TTM 20s



Two - Four outputs — Primary 5 V DC @ 10 amps; auxiliary 5 - 24 V DC @ up to 1.5 amps.
10.5" L x 7" W x 2" H (tentative).

350 Watts — DM 33

Three outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 4.13" H.

350 Watts — DM 34

Four outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 4.13" H.

500 Watts — DM 41

One output — 2 - 28 V DC.
16" L x 7.5" W x 4.13" H.

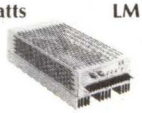
550 Watts — DM 53

Three outputs — Primary 5 V DC @ 100 amps; auxiliary 2 - 28 V DC @ up to 16 amps.
16" L x 7.5" W x 6" H.

550 Watts — DM 54

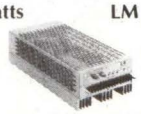
Four outputs — Primary 5 V DC @ 100 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 6" H.

350 Watts — LM 33



Three outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 4.13" H.

350 Watts — LM 34



Four outputs — Primary 5 V DC @ 50 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 4.13" H.

500 Watts — LM 41

One output — 2 - 28 V DC.
16" L x 7.5" W x 4.13" H.

600 Watts — LM 53

Three outputs — Primary 5 V DC @ 100 amps; auxiliary 2 - 28 V DC @ up to 16 amps.
16" L x 7.5" W x 6" H.

600 Watts — LM 54

Four outputs — Primary 5 V DC @ 100 amps; auxiliary 2 - 28 V DC @ up to 10 amps.
16" L x 7.5" W x 6" H.

375 Watts — MM 24

Four outputs — Primary 5 V DC @ 75 amps; 2nd output 2 - 24 V DC @ up to 10 amps, 3rd and 4th outputs 5 - 24 V DC @ up to 5 amps.
15.25" L x 5" W x 3.9" H.

375 Watts — MM 25

Five outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 5 amps.
15.25" L x 5" W x 3.9" H.

375 Watts — MMX 72

"Flat Pak"
Two outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 24 amps.
13" L x 9.5" W x 3" H.

375 Watts — MM 73

"Flat Pak"
Three outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 12 amps.
13" L x 9.5" W x 3" H.

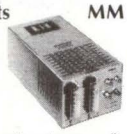
600 Watts — MML 45

Five outputs — Primary 5 V DC @ 75 amps; auxiliary 2 - 24 V DC @ up to 12 amps.
13.5" L x 8.5" W x 5.1" H.

750 Watts — MM 44

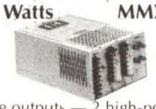
Four outputs — Primary 5 V DC @ 150 amps; auxiliary 2 - 24 V DC: 2nd output @ up to 12 amps; 3rd and 4th outputs @ up to 5 amps.
12.5" L x 7" W x 5.1" H.

750 Watts — MM 52



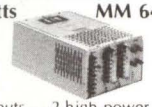
Two 375-watt outputs — 2 - 24 V DC @ up to 75 amps.
13.5" L x 6.5" W x 5.1" H.

750 Watts — MMX 63



Three outputs — 2 high-power, 2 - 24 V DC @ up to 75 amps; 3rd output, 2 - 24 V DC @ up to 24 amps.
13.5" L x 8.5" W x 5.1" H.

750 Watts — MM 64

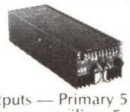


Four outputs — 2 high-power, 2 - 24 V DC @ up to 75 amps; 2 low-power, 2 - 24 V DC @ up to 12 amps.
13.5" L x 8.5" W x 5.1" H.

750 Watts — MM 65

Five outputs — 2 high-power, 2 - 24 V DC @ up to 75 amps; 3 low-power, 2 - 24 V DC: 3rd output @ up to 12 amps; 4th and 5th outputs @ up to 5 amps.
13.5" L x 8.5" W x 5.1" H.

300 Watts — LH 300T



Three outputs — Primary 5 V DC @ 50 amps; auxiliary 5 - 24 V DC @ up to 8 amps.
16.25" L x 5.05" W x 3.65" H.

300 Watts — LH 400T

Three outputs — Primary 5 V DC @ 50 amps; auxiliary 5 - 24 V DC @ up to 8 amps.
12.25" L x 7.5" W x 3.9" H.

300 Watts — LH 400Q

Four outputs — Primary 5 V DC @ 50 amps; auxiliary 5 - 24 V DC: 2nd and 3rd outputs @ up to 8 amps; 4th output @ up to 2 amps.
12.25" L x 7.5" W x 3.9" H.

500 Watts — LH 500S

One output — 5 - 24 V DC.
20.25" L x 5.05" W x 3.65" H.

500 Watts — LH 550S

One output — 5 - 24 V DC.
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DESIGN NOTE

Software-Based Single-Bit I/O Error Detection and Correction Scheme

A scheme that both intercepts and corrects single-bit I/O errors employs a software implementation for checking 4-bit characters. Existing software that reads or writes data can be modified in a nearly transparent manner, at considerable time and cost savings

George M. White University of Ottawa, Ottawa, Ontario, Canada

Modern computing systems are essentially highly reliable devices. However, associated input/output peripherals often malfunction because of moving parts and inherent characteristics of the external media on which data are stored. Traditionally, computer systems have dealt with these errors by introducing redundancy bits into the read/write operation. Adding parity bits and block check characters is an attempt to intercept errors before they can cause problems; however, these methods result in read/write inefficiencies because of the extra redundant information. Sophisticated input/output (I/O) devices use coding techniques at the hardware level to accomplish the same goal.

One major fault exists with these schemes; errors are detected but are not corrected. After an error is detected, the system will either halt or attempt a retransmission, depending on the degree of capability. Retransmissions do not guarantee success, however, and if data have been written incorrectly, retransmission wastes time. A system of error correction that not only intercepts an error when it occurs, but also corrects the error so that retransmission is unnecessary is an improvement on these schemes. The principles of error correction are well-understood and are beginning to be used as a standard software engineering tool.

The software-based correction scheme has a simple program structure that is easily coded for most computers. The two subroutines that are presented can be readily implemented; if used as an integral pair, their effect is transparent to the remainder of the system, except that single I/O errors are eliminated while double and triple errors pass through. Existing software can be easily modified to incorporate these subroutines.

The scheme's main disadvantage is that each half byte (four bits) of data is treated as an information group and the number of required check bits (in this case, three) is therefore relatively large in comparison. Since the word length is nearly doubled, twice as much external storage media is needed to record the same amount of data information, and thus read and write times twice as long are necessary. These limitations may prohibit the use of this error correction scheme in some I/O applications.

Basic Principles

Assume that four data bits (half a byte) are to be written on an ex-

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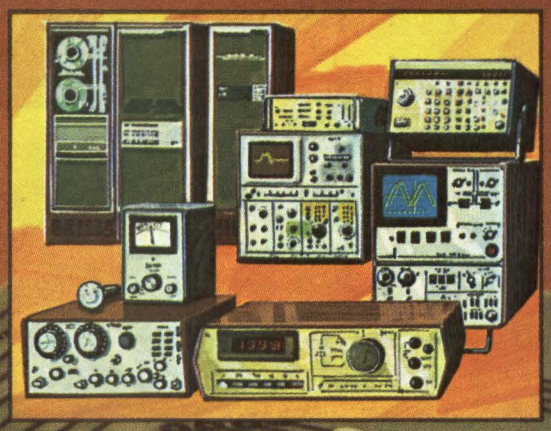

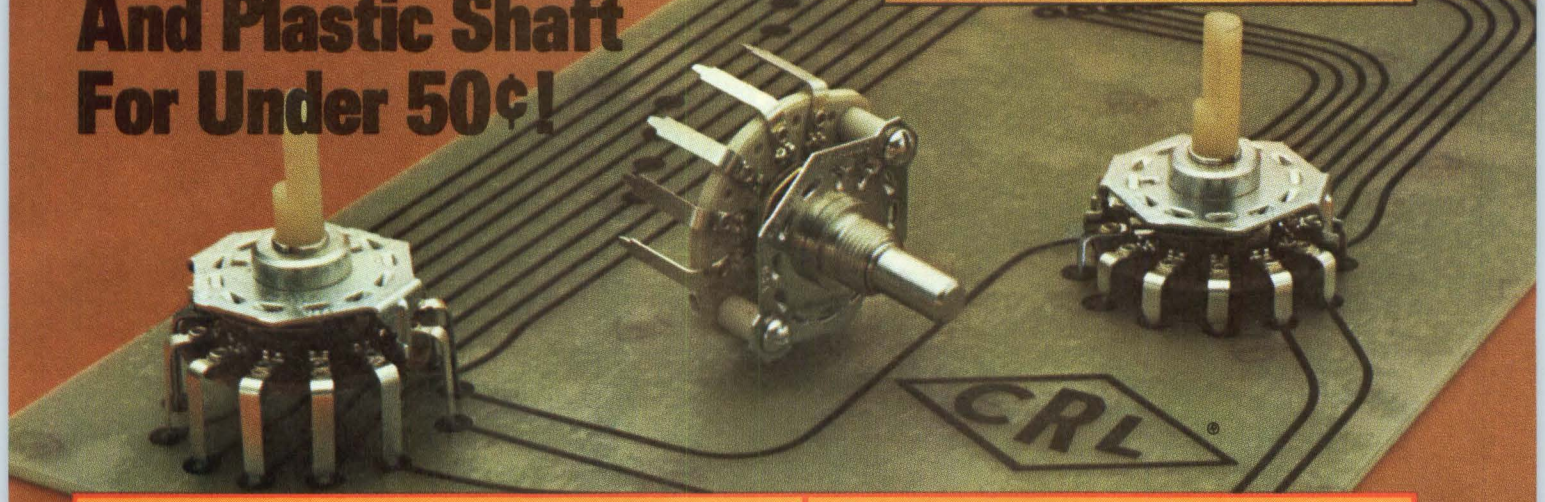

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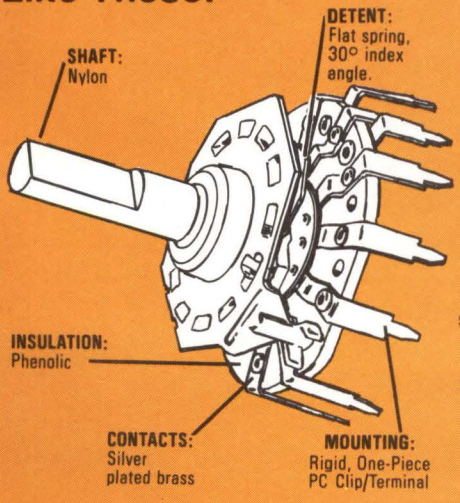

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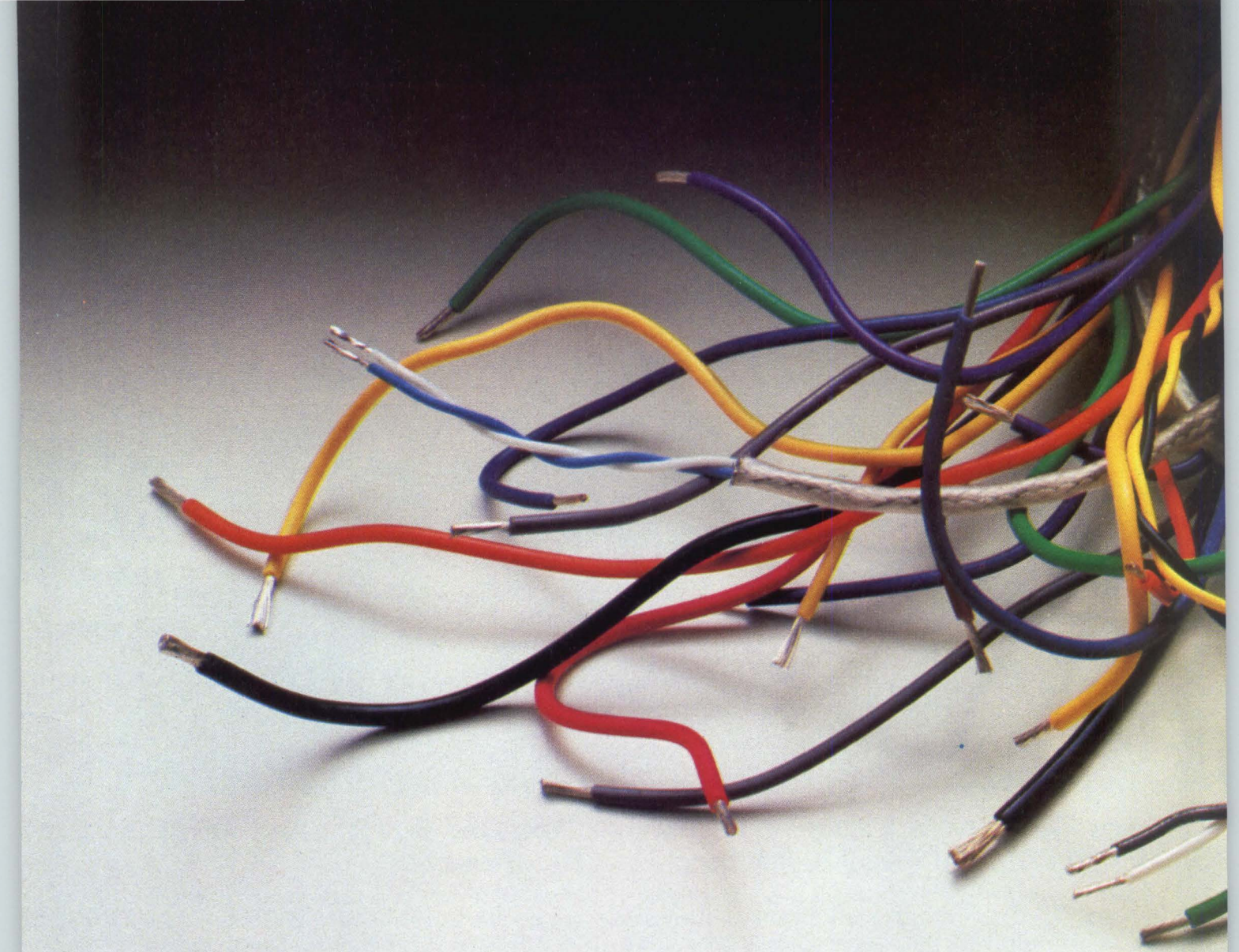

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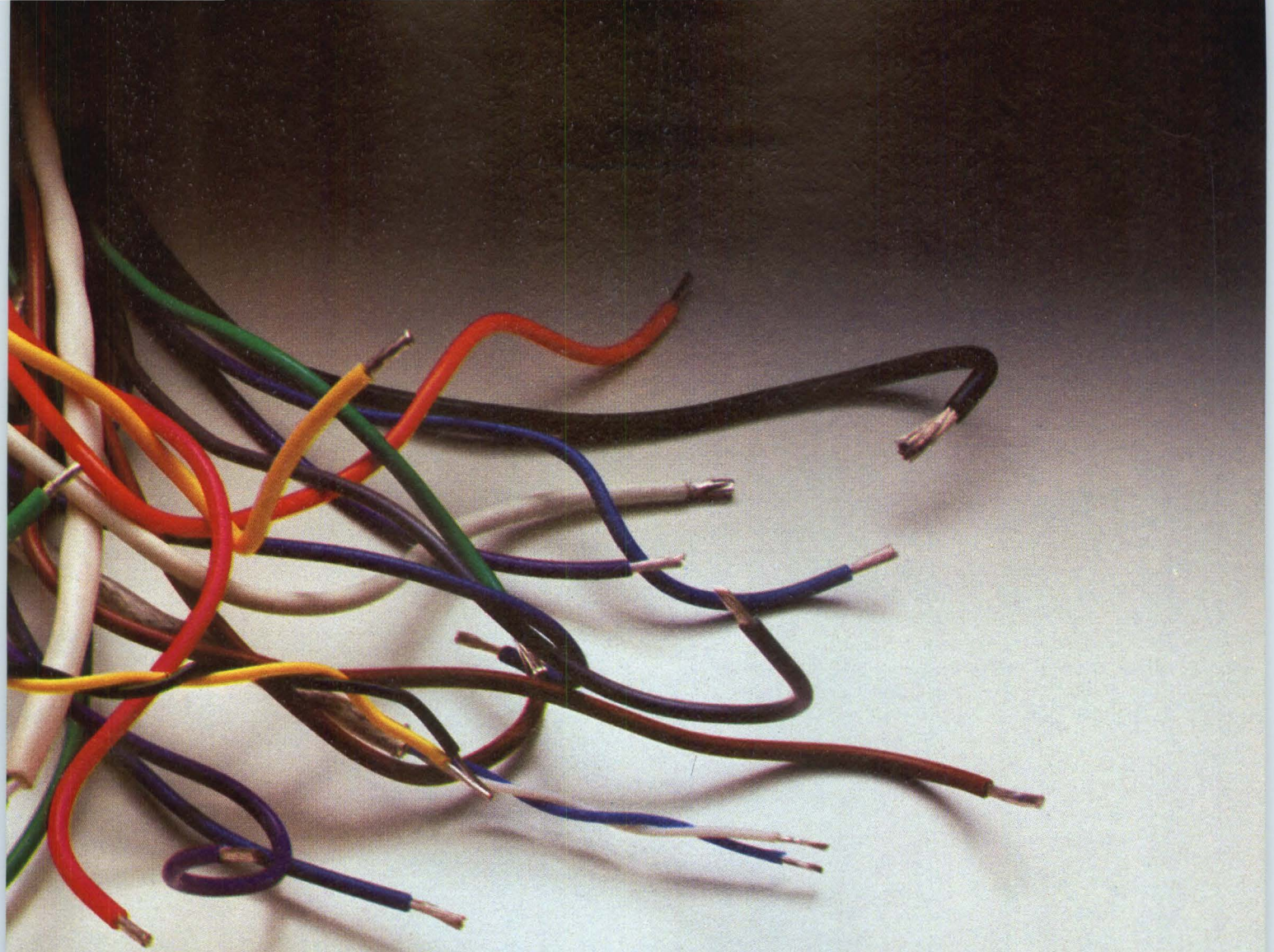

it from here.

When you're down to the wire

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ternal I/O device as I_3, I_5, I_6, and I_7. Three check bits, C_1, C_2, and C_4, can be concatenated to establish a field of seven bits.

$C_1\ C_2\ I_3\ C_4\ I_5\ I_6\ I_7$

Check bits C_1, C_2, and C_4 are calculated, so that

$$\begin{aligned} & & & C_4 \oplus I_5 \oplus I_6 \oplus I_7 = 0 \\ & C_2 \oplus I_3 & & \oplus I_6 \oplus I_7 = 0 \\ C_1 & \oplus I_3 & \oplus I_5 & \oplus I_7 = 0 \end{aligned}$$

where $\oplus$ is the logical exclusive-OR symbol and the binary 0 result is interpreted as meaning even parity. For example, consider the hexadecimal character 2, for which the 4-bit pattern I_3, I_5, I_6, I_7 is 0 0 1 0. It is easily calculated that the redundancy bits are $C_1 = 0$, $C_2 = 1$, and $C_4 = 1$, giving a 7-bit field of 0 1 0 1 0 1 0. By appending an additional bit, I_0, whose value is always 0 to this field, a full 8-bit byte is obtained that can be written onto an output medium. In practice, this is usually done by calling a put character subroutine or executing a MOVE type instruction.

Assume that an error occurs in bit I_3, changing it from 0 to 1; this could happen in either reading or writing. After data have been read and the I_0 bit is stripped off, the field appears as 0 1 1 1 0 1 0. Evaluating the left-hand side of the equations given previously yields the following results:

$C_4 \oplus I_5 \oplus I_6 \oplus I_7 = 0$

$C_2 \oplus I_3 \oplus I_6 \oplus I_7 = 1$

$C_1 \oplus I_3 \oplus I_5 \oplus I_7 = 1$

Writing this horizontally, the binary pattern 0 1 1 (or decimal 3) is obtained; thus, bit I_3 is in error. Changing this bit and stripping away the check bit gives 0 0 1 0, the original 4-bit character.

Further examination of this error correction scheme shows that (a) any one of the seven bits if wrong, can be detected and corrected, even one of the redundancy bits; (b) the error can be a 1 changed to a 0 or a 0 changed to a 1; and (c) if more than one error occurs in the seven bits, the scheme will not work. In this case, a double error would be detected but the attempt to correct it would give a false result. A triple error would be received as if it were correct; no error would be detected.

Software Correcting Modules

The subroutine listed as PUTCC (Put Coded Character) assumes that the binary representation of the character to be written occupies the lower eight bits of a 16-bit accumulator. Any convenient code, such as ASCII or EBCDIC, can be used. The upper four bits of this character are coded and written, and are followed by the lower four bits. Therefore, one 8-bit byte is converted into two 4-bit coded bytes. To implement the 16 possible characters, the conversion is done by a table lookup rather than by arithmetic manipulation. Note that since three logical equations must be satisfied simultaneously, the code words as a whole do not have any consistent parity.

Subroutine listing GETCC (Get Coded Character) reads two successive coded bytes that have been previously written by PUTCC, corrects any single errors that may have occurred, removes the check bits, and stores the reconstructed character in a register. It accomplishes this by isolating each bit of the coded character, calculating the logical exclusive-OR for the three equations, and using any non-zero result to locate and complement the single bit that is in error. To perform the calculations, three temporary variables—called first, second, and third—are

PUTCC (Put Coded Character)

```
                *SUBROUTINE PUTCC (PUT CODED CHARACTER)
                *THE CHARACTER TO BE WRITTEN OCCUPIES THE
                *LOWER BYTE OF REGISTER A
PUTCC:          Octal           0           ;return address stored here
                Store,M         save        ;save M and X registers,
                Store,X         save + 1    ;if desired
                Double right shift  8       ;shift character into M
                Load,A          zero        ;clear A
                Double left shift   4       ;shift 4 bits into A
                Add to A        adtab       ;add table address
                Exchange A and X            ;address goes into X
                Load A, indexed             ;load A with code word
                Jump to subroutine  PUTC    ;this is routine for writing
                Load,A          zero        ;clear A
                Double left shift   4       ;shift next 4 bits into A
                Add to A        adtab       ;add table address
                Exchange A and X            ;address goes into X
                Load A, indexed             ;load A with code word
                Jump to subroutine  PUTC    ;routine for writing
                Load,M          save        ;restore registers
                Load,X          save + 1
                Jump, indirectly    PUTCC   ;return
save:           Octal           0
                Octal           0
zero:           Octal           0
adtab:          Address         table
table:          Octal           000         ;table of code words
                Octal           151         ;coded 1
                Octal           052         ;coded 2
                Octal           103         ;coded 3
                Octal           114         ;coded 4
                Octal           045         ;coded 5
                Octal           146         ;coded 6
                Octal           017         ;coded 7
                Octal           160         ;coded 10
                Octal           031         ;coded 11
                Octal           132         ;coded 12
                Octal           063         ;coded 13
                Octal           074         ;coded 14
                Octal           125         ;coded 15
                Octal           026         ;coded 16
                Octal           177         ;coded 17
```

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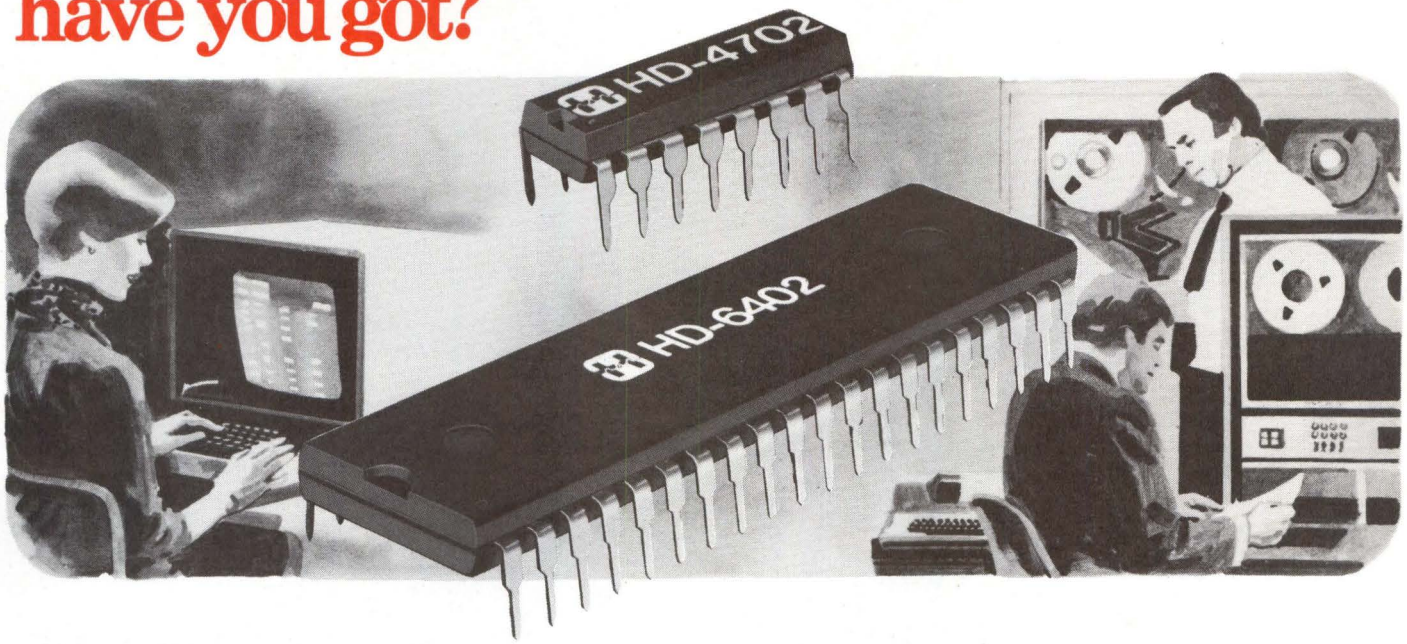

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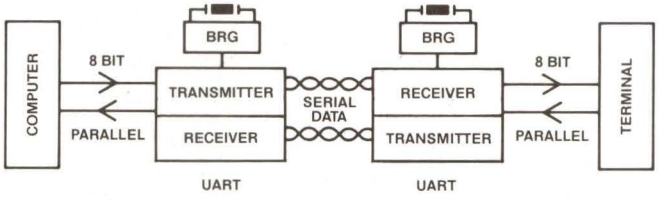

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GETCC (Get Coded Character)

```
*SUBROUTINE GETCC (GET CODED CHARACTER)
*AFTER RETURNING FROM THIS SUBROUTINE, THE
*CHARACTER OCCUPIES THE LOWER BYTE OF
*REGISTER A
*
GETCC:  Octal               0       ;return address stored here
        Jump to subroutine  GETC    ;this is routine for reading
        Jump to subroutine  DECODE  ;decode upper 4 bits
        Left shift          4
        Store,A             nib
        Jump to subroutine  GETC
        Jump to subroutine  DECODE  ;decode lower 4 bits
        Add to A            nib     ;reconstruct character
        Jump, indirectly    GETCC
nib:    Octal               0       ;temporary storage
*
DECODE: Octal               0
        Store,X             xreg    ;save register X
        Store,A             codewd  ;save register A
        Double right shift  6       ;C1 in register A
        Store,A             first
        Load,A              zro
        Double left shift   1       ;C2 in register A
        Left Shift          1
        Add to A            first
        Store,A             first
        Load,A              zro
        Double left shift   1       ;I3 in Register A
        Store,A             second
        Left shift          1
        Add to A            second
        Store,A             second
        Load,A              zro
        Double left shift   1       ;C4 in register A
        Left shift          2
        Add to A            first
        Store,A             first
        Load,A              zro
        Double left shift   1       ;I5 in register A
        Store,A             third
        Left shift          2
        Add to A            second
        Store,A             second
```

evaluated. First is a concatenation of C_4, C_2, and C_1; second is a concatenation of I_5, I_3, and I_3; and third is a concatenation of I_6, I_6, and I_5. After these variables have been formed, the logical exclusive-OR sum is easily calculated; if this result is non-zero, the resulting sum points to the bit in error.

The subroutines are written in an informal "assembler-like" language that assumes that the machine on which it runs has at least two general-purpose registers, called A and M; an index register, called X; and a single-address instruction set. No attempt has been made to minimize the code generated or to reduce execution time.

A machine for which these programs apply has the familiar load and store instructions as well as add, jump, jump to subroutine, and conditional skips. It also includes left and right shifts with operands that cause the A register to shift bits, and left and right double shifts that cause the A and M registers to be concatenated and shifted as one double-width register. Registers and memory are assumed to have a width of 16 bits.

The two subroutines should always be used as an integral pair. They can be used together with new software or can be incorporated easily into existing software. To do the latter, all calls to I/O subroutines should be replaced by calls to PUTCC and GETCC, and the original subroutines can be used by the new coding subroutines. If the I/O subroutines are all called indirectly via an address in a common memory area, all

```
        Load,A              zro
        Double left shift   1           ;16 in register A
        Skip if A≠0
        Jump                bitsev
        Load,A              sixth
        Add to A            third
        Store,A             third
        Load,A              zro
bitsev: Double right shift  1           ;17 in register A
        Skip if A=0
        Load,A              seven
        Exclusive-OR, A     third       ;calculate XOR for equations
        Exclusive-OR, A     second
        Exclusive-OR, A     first
        Skip if A=0                     ;any errors?
        Jump                error       ;Yes
ok:     Load, A             codewd      ;No
        And,A               xxvii       ;strip off check bits
        Double right shift  3
        Right shift         1
        Double left shift   3
        Load,X              xreg        ;restore X register
        Jump, indirectly    DECODE
error:  Add to A            aderms      ;correct error
        Exchange A and X
        Load A, indexed     -1
        Exclusive-OR, A     codewd      ;complement bit in error
        Store, A            codewd
        Jump                ok
ermsk:  Octal               100         ;error mask words
        Octal               40
        Octal               20
        Octal               10
        Octal               4
        Octal               2
        Octal               1
zro:    Octal               0
codewd: Octal               0
first:  Octal               0
second: Octal               0
third:  Octal               0
xreg:   Octal               0
sixth:  Octal               6
seven:  Octal               7
xxvii:  Octal               27
aderms: Address             ermsk
```

that is required is to switch pointers from the old address to the addresses of PUTCC and GETCC.

Summary

Capable of correcting as well as detecting single-bit I/O generated errors, the error correction scheme is carried out completely in software, and can be programmed into place on top of existing software with minimum modification, typically in one or two words. The code is irrelevant and any number of bits can be handled by separation into 8-bit blocks.

In several paper tape applications used by the author, an object file is generated on paper tape by an unreliable punch. When these object tapes are loaded, so many errors are found that it becomes impossible to execute the program. However, by changing the punching and reading routines as suggested here, the errors are detected and corrected, quickly and easily. Even with the extra software overhead, the input reading rate is limited by the speed of the read head itself, in this case, 300 char/s.

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S. Vasa, "Calculating an Error Checking Character in Software," *Computer Design*, May 1976, pp 190-192

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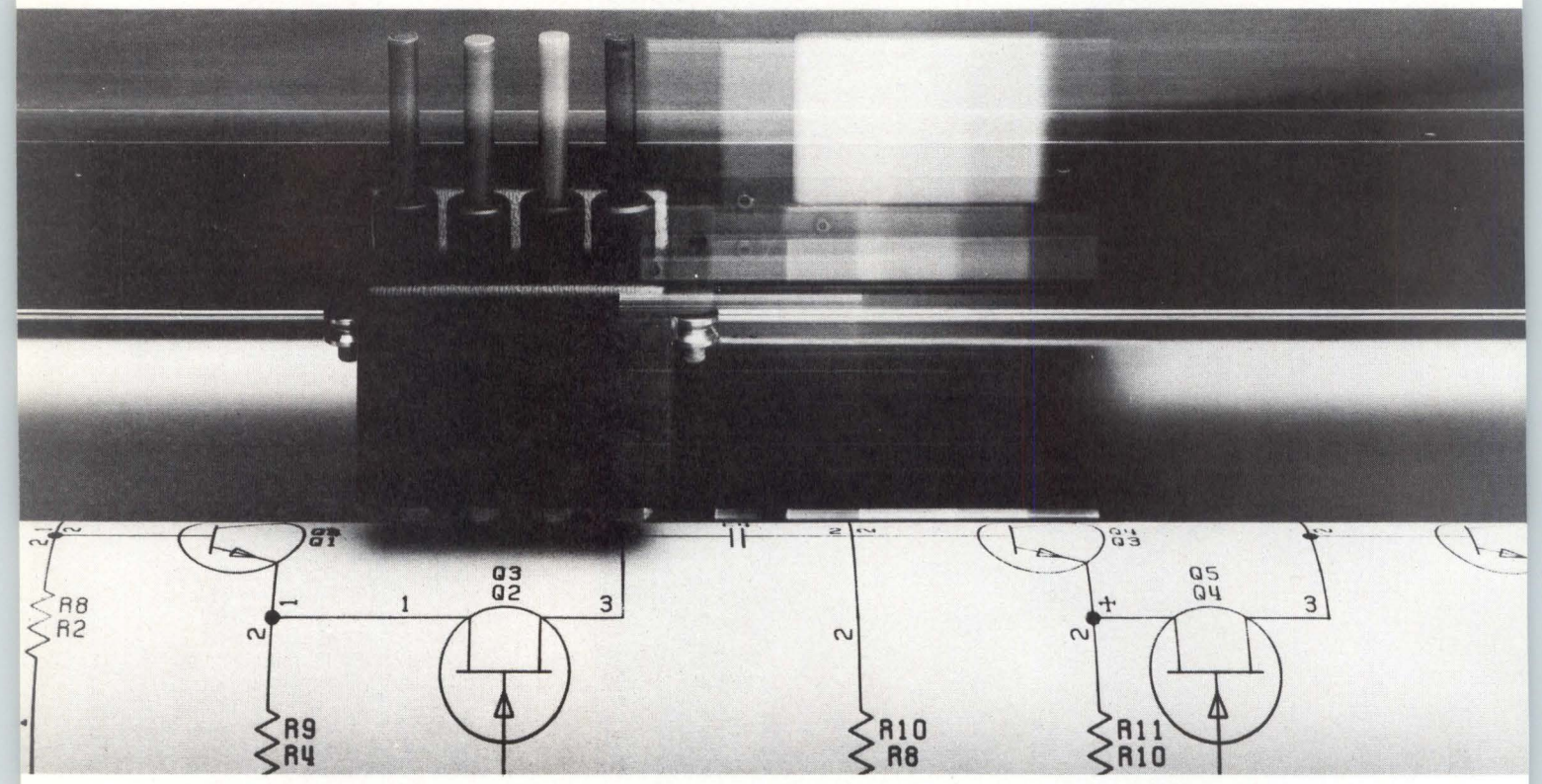

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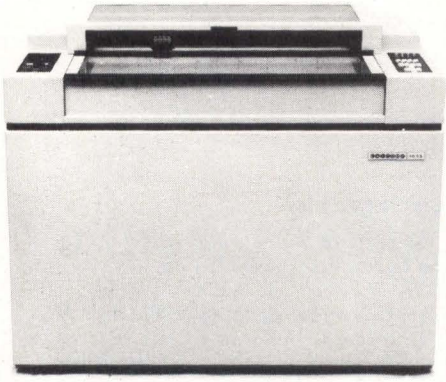

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INTERFACING FUNDAMENTALS: AN APPLICATION OF THE 8085 PROCESSOR, PART 1

Peter R. Rony and David G. Larsen
Virginia Polytechnic Institute and State University

Jonathan A. Titus and Christopher Titus
Tychon, Inc

In this month's column, the 8085 system will be used to build a small control system, configured so that eight analog channels can be monitored with a time period between measurements which may be set by the user. It is assumed that all eight channels are monitored quickly with a long period between these quick samplings. The control system's computer (the 8085) must have the following input/output devices.

(1) A fast 10-bit analog-to-digital converter (ADC) with an 8-channel multiplexer

(2) A set of thumbwheel switches to select the time period (1 to 99 s)

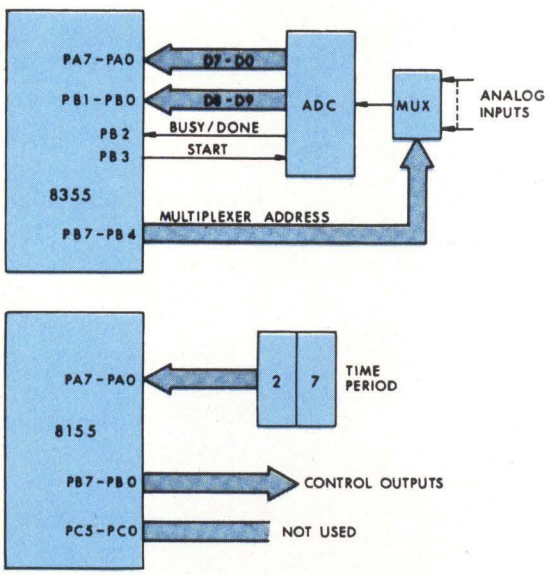
(3) A set of eight control outputs (on/off) that may be used to control the process being monitored

The intent is not to describe the entire control system, but rather to show how the interfacing takes place. The necessary software for operating the system with the various input/output (I/O) devices will also be explained.

The control function that may be required of this system could be simple or complex, depending upon how the software algorithm is set up. When based upon an 8085 system, the hardware can be simple. First hardware considerations are to the assignment of the I/O ports and bits to the various I/O devices. Required connections are:

A-D Converter	
10 Output lines	ADC data
1 Output line	Status sense line
1 Input line	Start pulse
4 Input lines	Multiplexer channel address
Thumbwheel Switches (Time)	
8 Output lines	2 Binary coded decimal digits
Control	
8 Input lines	For various control devices

These connections were assigned as shown in the Figure, in which general connections are in block diagram form. One 8155 read/write (R/W) memory and one 8355 read-only memory (ROM) device are used in the system. Notice that the six I/O lines of port C on the 8155 have not been used; they are available for later expansion.



Block diagram of connections between 8085 I/O chips and I/O devices

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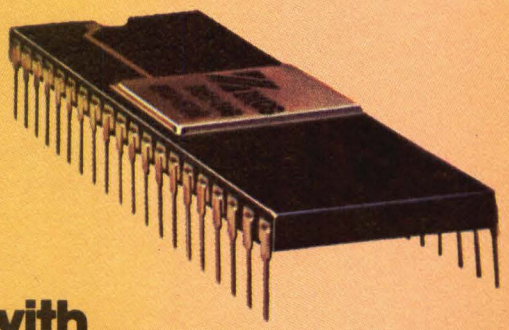

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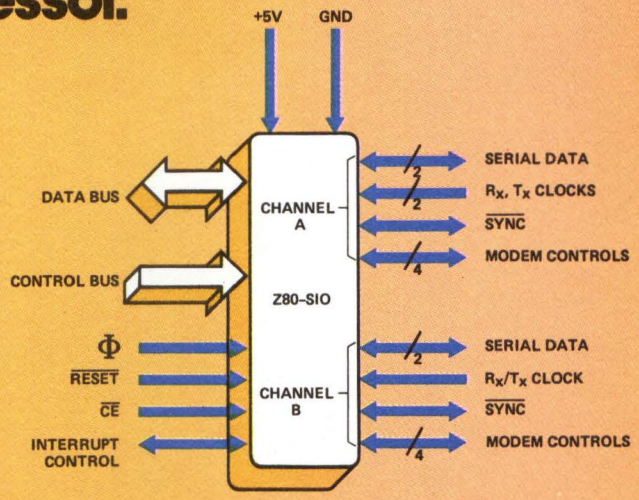

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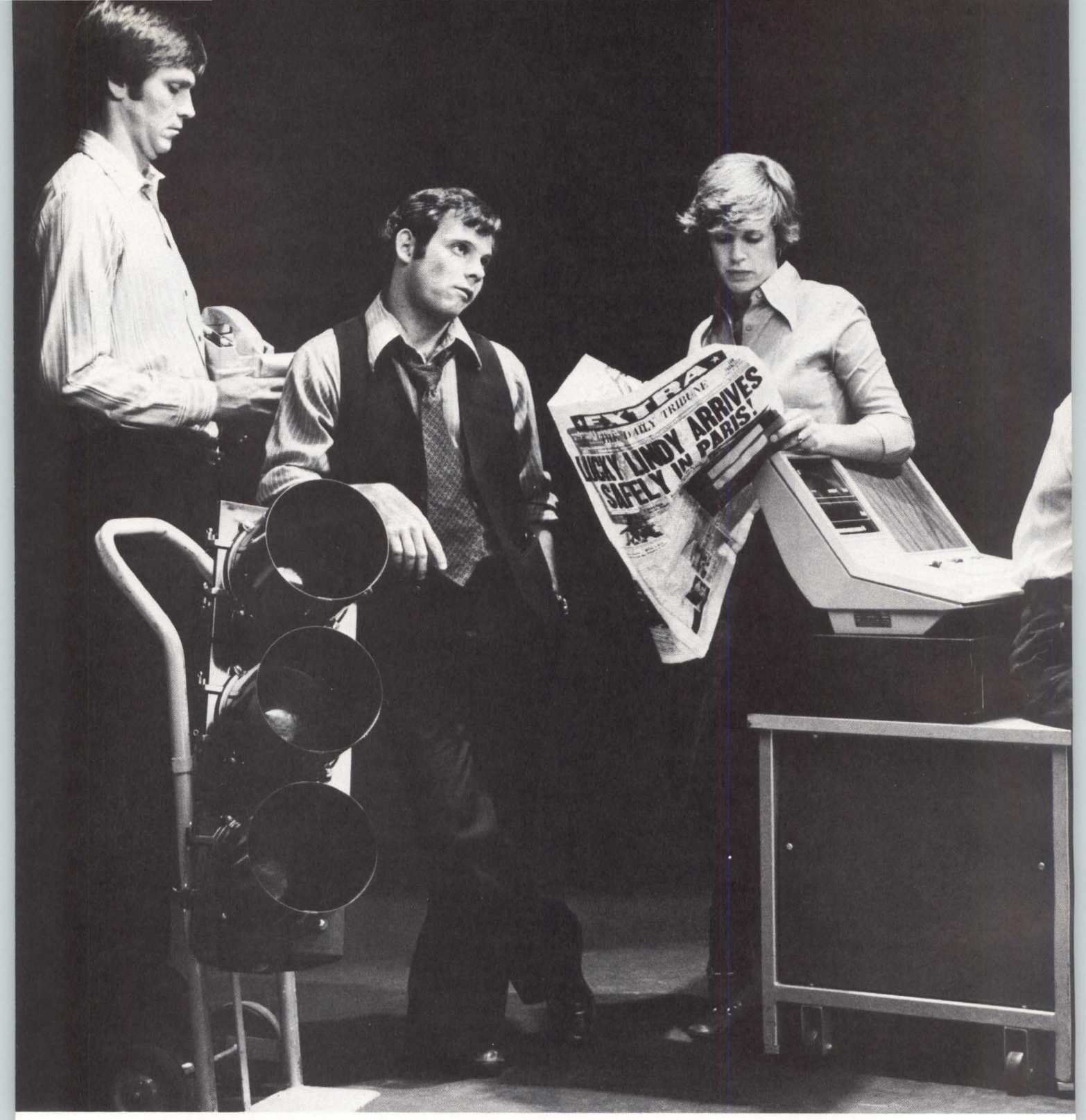

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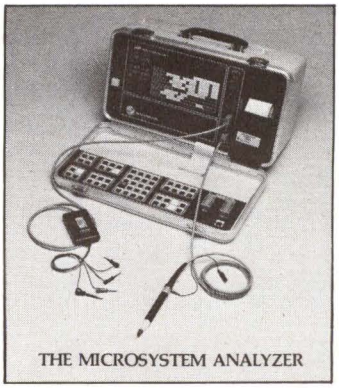


THE MICROSYSTEM ANALYZER

CIRCLE 65 ON INQUIRY CARD

LISTING 1

Program Steps to Initialize 8355 I/O Ports

```
Start,  MVIA    /Load reg A with port A control word
        000
        OUT     /Output it to the 8355 chip
        002
        MVIA    /Load reg A with port B control word
        370
        OUT     /Output it to the 8355 chip
        003
        NOP     /Program continues here
```

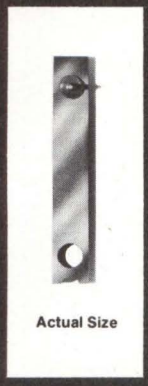
LISTING 2

ADC and Multiplexer Control Steps

```
/Conversion start portion of the program
        LDA     /Get the status word, bit PB3 = start
        STATUS
        0
        ORI     /Set the start bit to 1
        010
        OUT     /Output it
        001
        ANI     /Clear the start bit
        367
        OUT     /Output it
        001
        NOP     /Continue here
/Multiplexer update, switch to the next channel
        LDA     /Get the status word, bits PB7 to PB4
        STATUS  /are the multiplexer channel address
        0
        ADI     /Add 1 to multiplexer address
        020
        OUT     /Output it to the multiplexer
        001
        STA     /Store the new status word back in
        STATUS  /its memory location
        0
        NOP     /Continue here
```

I/O ports of the 8355 were used to control the ADC system since a combination of inputs and outputs was needed. These I/O ports can be assigned input or output functions on a bit by bit basis. The R/W memory device was used for switch inputs and control outputs since these were already prearranged in groups of eight lines each.

It is now necessary to write the software that will be used to control the ROM's I/O ports for handling the ADC. The I/O port bits must first be assigned input or output functions. The eight bits at port A are all input bits, while the bits at port B are mixed. Thus, the following control words must be sent to the two port control registers in the ROM device.



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CIRCLE 67 ON INQUIRY CARD

150 lpm **P150**

300 lpm **P300**

600 lpm **P600**

Port A Control = 00000000_2 0 = Input Bit
Port B Control = 11111000_2 1 = Output Bit

The output of these control words is shown in the short section of program in Listing 1.

When these control words are output to the control registers, the ports will be configured as required. Some caution is required when using port B if bit PB3 and bits PB7 to PB4 are to be controlled independently. Thus, when PB3 changes, bits PB7 to PB4 must not be altered. Careful thought must be applied to this problem so that the program does not start a conversion when it should only change the multiplexer's 4-bit address. A status word, stored in R/W memory, can be used to tell the program the current status of the output lines. Individual bits can then be manipulated without affecting the others. Two sections of the program are shown in Listing 2; one section shows how the multiplexer is updated without affecting the converter, and the other shows how the converter is started without affecting the multiplexer. In fact, each of these routines could be treated as a subroutine.

I/O ports on the R/W memory device are also easy to control. The bits at port A are used as inputs and those at port B as outputs. Port C is not used. Rather than use a software delay loop, the 8155 timer function can be employed to help time the 1-s period. Assuming that the 8085 has a clock period of 1 μs, periods of up to 16.36 ms are provided for with a 14-bit counter. The 10.00-ms period that we have chosen using a 14-bit binary count of 100111 00010000 must be loaded into the counter. Mode 3—automatic reload with a pulse at the end of each programmed period—has been selected for use, because the timer will be used over and over again.

LISTING 3

Program Steps to Initialize 8155 Timer

```
/Timer control program for the 8155 chip
        MVIA    /Preset the 8 LSBs of timer's count
        020
        OUT     /Output to timer
        204
        MVIA    /Output the 6 MSBs of timer's count
        347     /and 2 mode control bits, D6 and D7
        OUT     /Output them to the timer
        205
        MVIA    /Set up ports A and C for input,
        302     /port B for output, and start the
        OUT     /counter
        200
        NOP     /Continue here
```

The sequence in Listing 3 initializes the 8155 system to control ports A and B, and starts the 10-ms clock. The command/status word of 11000010 sets the clock mode and data direction for ports A and B. Port C is set for input, even though it is not used. The timer's pulse output generates an interrupt (RST 7.5) each time that a 10-ms period "times out." To make the RST 7.5 interrupt (on the 8085 integrated circuit) active, the RST 7.5 interrupt mask must be enabled with the instruction steps shown in Listing 4. The instructions clear any previous RST 7.5 interrupts and then enable the RST 7.5 mask.

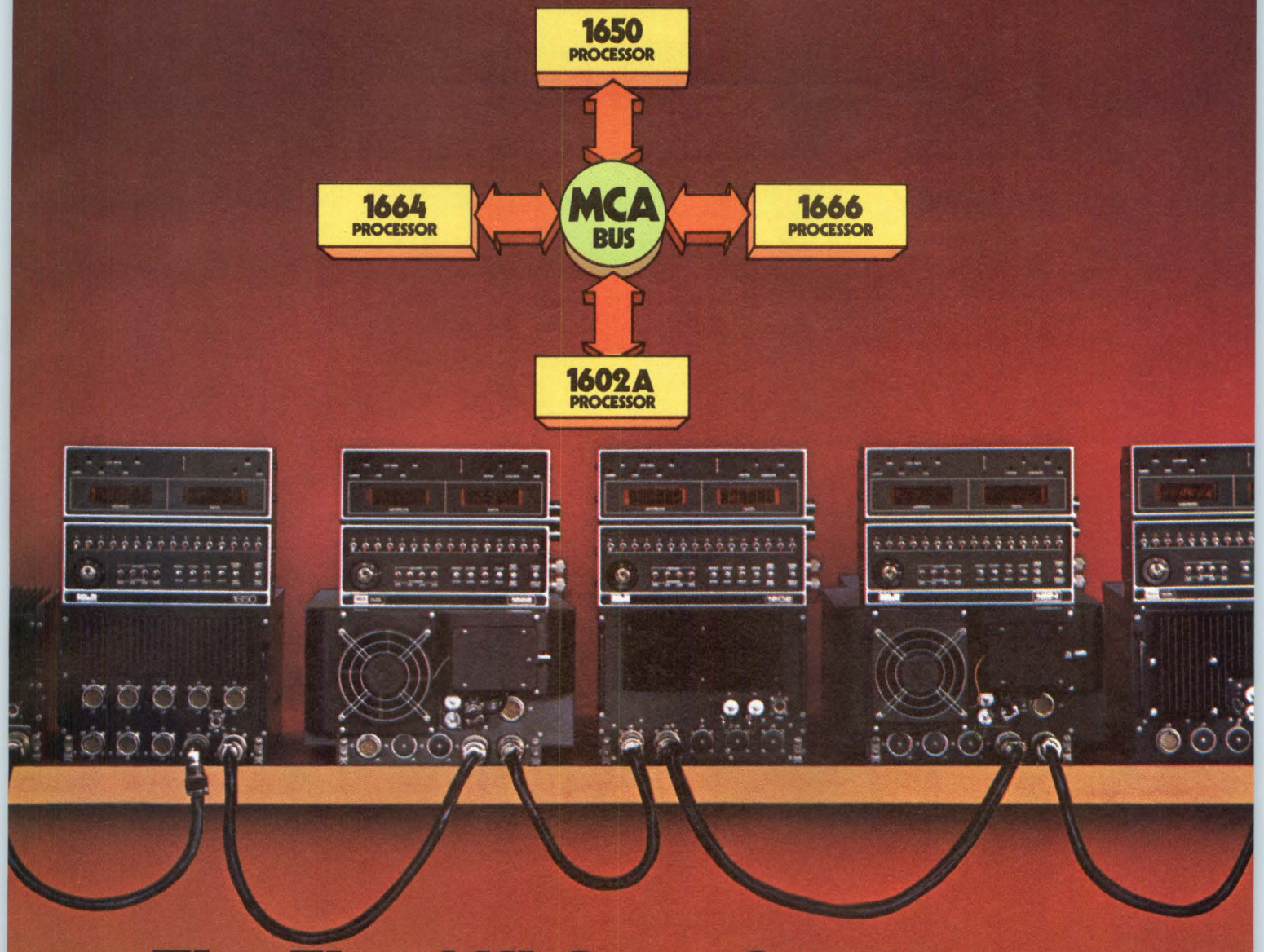
LISTING 4

Interrupt Service Enabling Steps for 8085

```
/Restart 7.5 interrupt service enabling steps
        MVIA    /Clear any previous RST 7.5
        020     /interrupts
        SIM     /Set interrupt mask
        MVIA    /Enable RST 7.5 interrupts
        013
        SIM     /Set interrupt mask
```

Combining the steps from Listings 1, 3, and 4 fully initializes the I/O ports. Remember, too, that a stack pointer has to be established before the interrupts can be used. This discussion will be continued next month, covering the overall software integration required for the application.

This article is based, with permission, on a column appearing in *American Laboratory* magazine.



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CIRCLE 69 ON INQUIRY CARD

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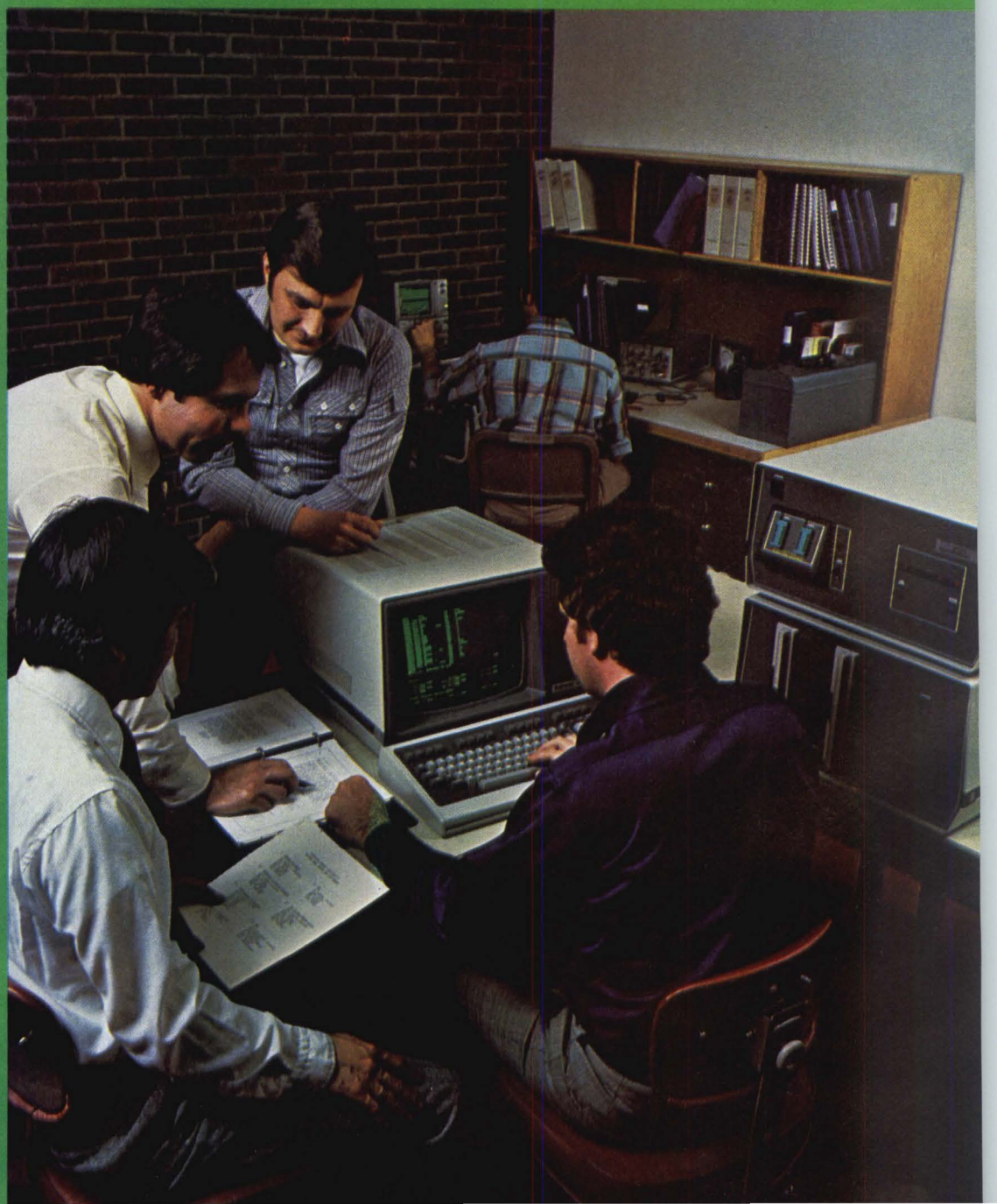

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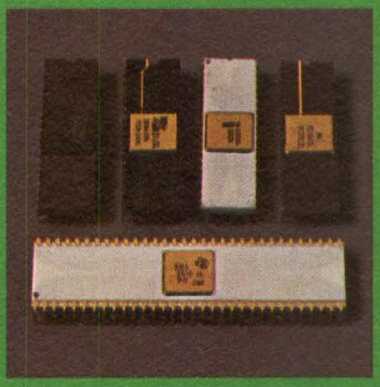

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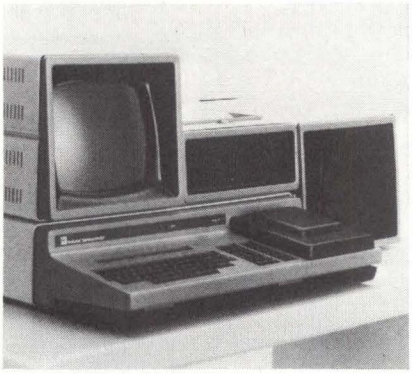
Incorporated in the development system are dual 256k-byte floppy discs for formatted bulk storage; a 1920-char, 12″ (30.5-cm) green phosphor CRT display; standard 58-key ASCII keyboard; auxiliary control pads with 8 keys for control, 18 keys for video display, and 12 keys for special functions; and a 50-char/s thermal printer, all housed in a 25 x 16 x 26″ (63.5 x 40.6 x 66-cm) modular, tabletop enclosure. Components may be reconfigured as desired. Four additional board slots are contained in the chassis for expansion with standard Series/80 I/O expansion cards, in-circuit emulator boards, or user designed interface boards. An integrated P/ROM programming station is optional.

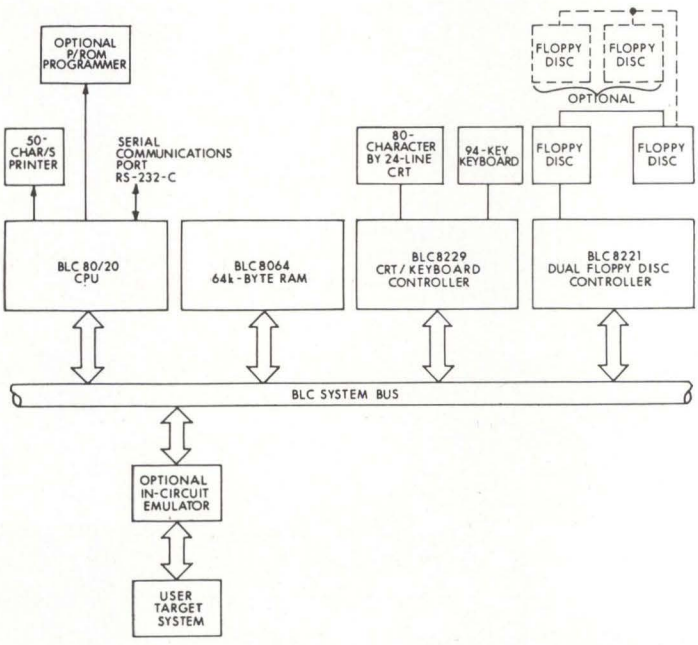
The CPU card is based on the BLC 80/204 with the microprocessor, a 19.354-MHz oscillator, multimaster bus controller, interrupt controller, interval timer, serial I/O interface, printer control, 4k bytes of onboard RAM, and sockets for 8k bytes of onboard RAM. The onboard RAM contains the startup bootstrap and system diagnostic routines used when power is applied. When completed, control is passed to the RAM based operating system, and the ROM diagnostic is programmably disabled by the operating system, which can then access the full 64k-byte RAM address space.

CRT/keyboard controller includes the microprocessor, 4k bytes of internal instruction ROM, 1k bytes of scratchpad RAM, and CRT refresh/video control circuit. Input from keyboard is 8-bit parallel; output to the CRT is vertical sync, horizontal sync, and video at TTL levels.

The floppy disc controller contains 4k bytes of ROM, 1k bytes of scratchpad RAM, 1k bytes of buffer memory,



Modular construction of National Semiconductor's STARPLEX development system for OEMs is engineered for user's ease. Standard configuration includes keyboard, CRT, two dual floppies, printer, and required software including operating system. Integrated features and high level languages reduce development time



Block diagram illustrates four major component boards of National Semiconductor STARPLEX system connecting to system bus: central processor, CRT/keyboard controller, and floppy disc controller. Multiprocessor architecture provides a microprocessor on each of these boards. 64k-byte memory board is also included. Hardware together with software improve microprocessor system development. ICE, P/ROM programmer, and two floppy discs are optional

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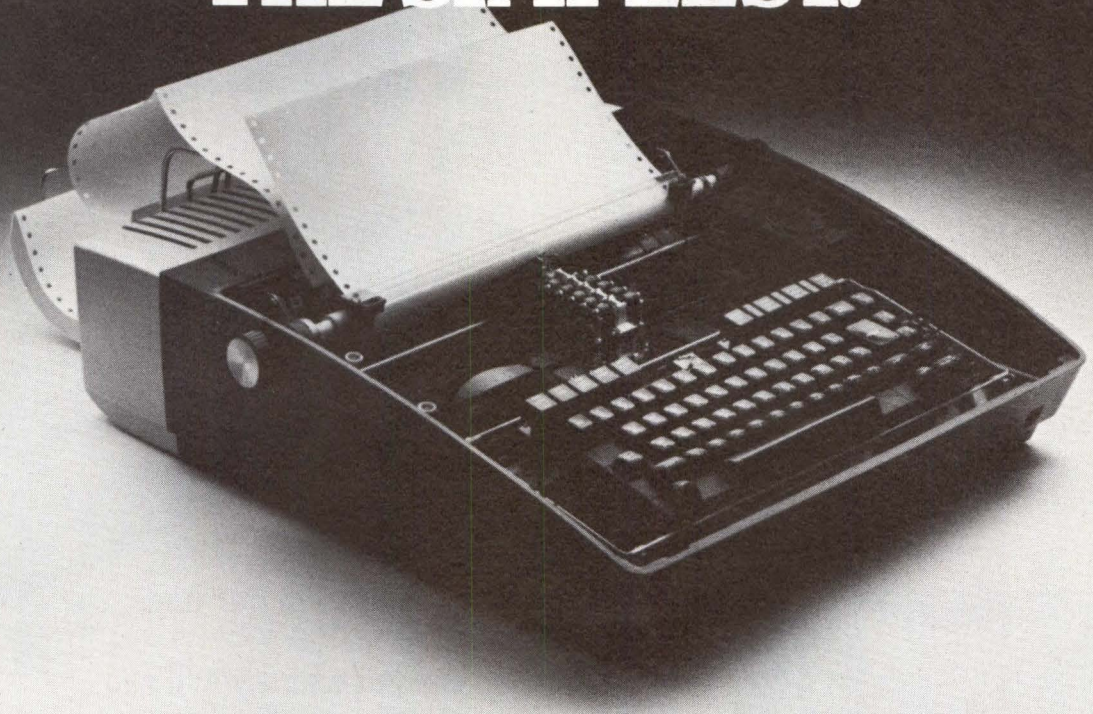

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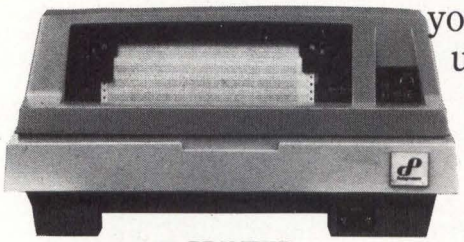

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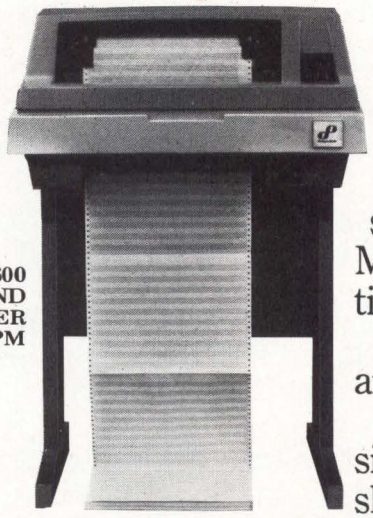

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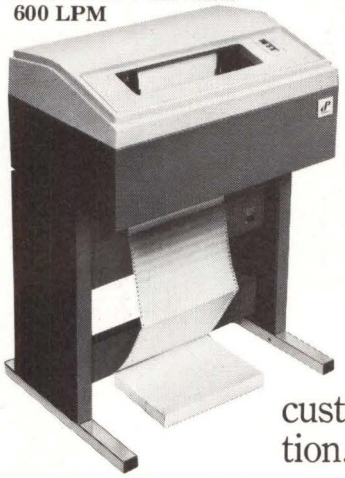

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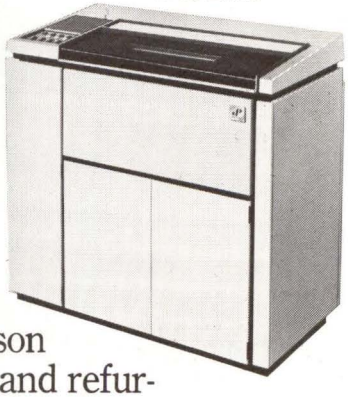

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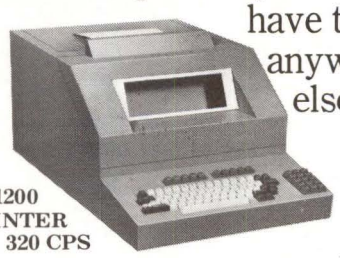

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CIRCLE 72 ON INQUIRY CARD

DMA controller, programmable peripheral interface, and logic control. It handles up to four floppy discs packaged in system modules. Standard floppies have a formatted capacity of 256k bytes/disc with an average access time of 280 ms. Transfer rate is 31.25k bytes/s.

Special function keys initiate frequently used prompting formats for P/ROM programming, debug, link, assemble, and edit, and call up menus for diagnostics and utility programs to prompt the user through microprocessor system development. Control functions include help, reset, abort, end, pause, and continue. Video keys control insert or delete line or character, roll up or down, next page, previous page, print, set or clear tab, and five cursor control keys. Users who are used to entering functions through the standard keyboard may continue to do so.

STARPLEX operating system has a consistent command set and common file and I/O structure, regardless of the language used. Macroassembler, BASIC interpreter, and FORTRAN compiler are accommodated. Transfers among memory and peripherals (treated as files) are handled automatically, with the internal microprocessors supplying the necessary protocol. Step by step prompting, clear language command structure, and audible tone for illegal operations also help to speed development while reducing programming time and errors.

Residing in the lower portion of the 64k-byte RAM, the operating system has a monitor surrounded by software levels that provides logical services and interacts with immediately adjacent upper and lower levels. The monitor supplies interval timing, establishes synchronization processes, and transforms hardware interrupts into service messages.

Software that comes with the system also includes a macroassembler; text editor, assembler, object manager, and librarian packages; disc-file-copy, disc backup, CRT/printer, loader, command-interpreter, system check, and debug utilities. An in-circuit emulator serves to aid hardware and software development and integration. Assemblers for the company's PACE and SC/MP are additional; Z80 support will be available later.

The system is to be marketed as an OEM product due to its modular subsystem construction. In quantities of 100 and up, price is $8200. It can also function as a small computer in industrial instrumentation, communications, and small business applications. Single unit price is $13,800.

Photoisolation I/O System Interfaces µProcessors In Industrial Applications

All modules in the I/O interface system provide 2500-V rms photoisolation to protect microprocessors from transients, spikes, rfi, etc, caused by industrial loads such as solenoids and motors. The system, available from Opto 22, 5842 Research Dr, Huntington Beach, CA 92649, consists of motherboards which incorporate the I/O modules.

Four basic types include ac input and output, and dc input and output. Logic signals are TTL, CMOS, DTL, or HTL compatible, with a choice of 5-, 15-, or 24-Vdc voltage levels. Ac modules come in 120- or 240-V versions; dc units in either 10- to 32-V or 200-V inputs, and a choice of 60- or 250-V outputs. Snubber filters enhance output module performance when used with inductive loads.

Boards are plug compatible with many microprocessor systems. Power leads connect by the terminal strip on the PC board, allowing modules to be changed without rewiring. Users may change the system by moving or replacing the module since the function is contained entirely within the module.

Modules are typically priced at $10.50 each in 1 to 99 quantities; 16-module board price is $57 each.
Circle 420 on Inquiry Card

Second Source Produces 8085A Microprocessors And Support Chips

As a second source of the Intel family of 8085A microcomputer products, NEC Microcomputers, Inc, 173 Worcester St, Wellesley, MA 02181 has introduced a group of devices that are designed for highly integrated systems requiring greater throughput, while using previously developed software. The family includes the UPD8085A 8-bit parallel, single-chip microprocessor with 1.3-µs cycle time; the UPD8155/8156 2k-bit static MOS RAM with I/O ports and timer; and the UPD8355/8755A masked ROM and UV-erasable P/ROM. Prices in quantities of 100 are $12, $11, and $48, respectively.
Circle 421 on Inquiry Card

Clip-On Probe Extends Analyzer Capabilities To 8085 Microprocessors

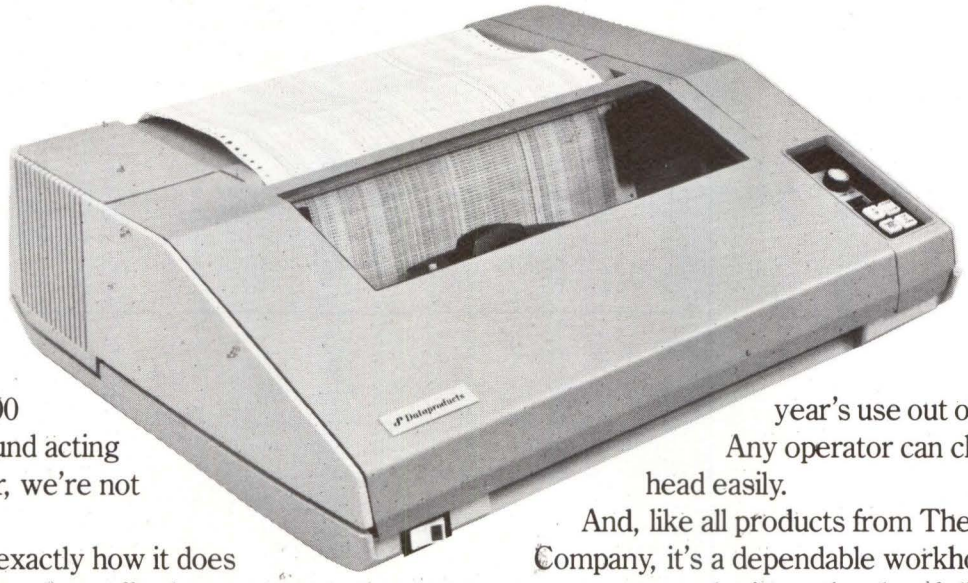
Serving as a low cost alternative to in-circuit emulators and CRT analyzers, the AQ8080 analyzer (*Computer Design*, June 1978, p 161) can be adapted to serve 8085 microprocessors through the use of a clip-on buffered probe. The possibility of damage to the chip is eliminated since the probe connects directly to the microprocessor. AQ Systems, Inc, 1736 Front St, Yorktown Heights, NY 10598 offers the probe for $495.
Circle 422 on Inquiry Card

OEM Alphanumeric Displays Interface To 8-Bit Microprocessors

Use of the alpha chip, a single-chip display/keyboard controller (see *Computer Design*, Jan 1978, p 142), enables Matrox Electronic Systems, PO Box 56, Ahuntsic Stn, Montreal, Quebec H3L 3N5, Canada to produce a complete display subsystem, including controller, display drivers, and alphanumeric LEDs on a single 8 x 3.25″ (20 x 8.3-cm) PC board. MTX-A2 and -B2 display boards for OEM applications interface directly to an 8-bit bidirectional data bus or I/O port of most microprocessors via a standard 44-pin connector.

Solid-state units consist of 16 large 0.3″ (0.76-cm) high, 5 x 7 dot matrix LED displays for the -A2 and two rows of 16 0.5″ (1.27-cm) high 14-segment LED displays for the -B2. Mounting hardware and a red filter permit installation into user equipment. Both displays scan up to 64 keys and have 22 intelligent

WHO DOES THIS PRINTER THINK IT'S KIDDING?



If the M-200 wants to go around acting like a line printer, we're not about to stop it.

And that's exactly how it does behave, cranking out an effortless 200 lines per minute, average throughput.

But the truth is, the M-200 is a serial printer. Which should certainly be obvious from the extremely reasonable purchase price of about $2000. (In OEM quantities.)

And so, if the M-200 delivers performance that can fool you, blame it on its design features.

Like our revolutionary 14-wire, dual-column print head, for instance. The design combines the flexibility of a single head with the speed and long life of multiple heads. (You can expect more than a year's use out of the head.)

Any operator can change the head easily.

And, like all products from The Printer Company, it's a dependable workhorse. Made even more so by its optional self-diagnostic system.

If something needs attention, the system tells you if you can tend to it yourself. Or if you can't, you know what to tell the serviceman. That can save him a trip, saving you down time and money.

And that's the inside story of the M-200. Acting like something it's not? Maybe. But since its delusions are all in your favor, why complain?

THE M-200 MATRIX PRINTER

THE PRINTER COMPANY

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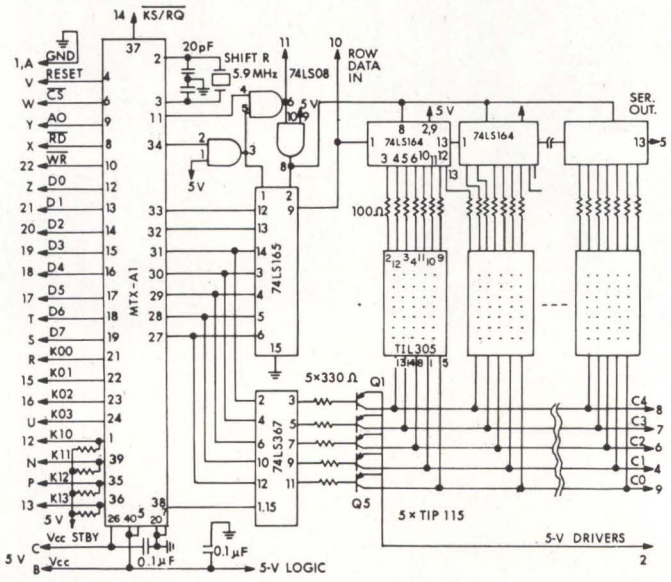
CIRCLE 73 ON INQUIRY CARD

MICRO DATA STACK
PROCESSORS AND ELEMENTS



Intelligent display/keyboard controller chip (MTX-A1) is basis of Matrox's single-board display subsystems for 8-bit microprocessors. MTX-A2 (illustrated) has 16-character display (expandable to 32), and -B2 has 32-character display. Multiple -A2 boards are used for more than 32 characters

commands. Separate 5-V power supply inputs are provided for logic, standby, and column or segment drivers; these may be connected together. Variable intensity and power savings are obtained by varying column or segment drivers voltage from 2 to 6 V.

Designed for industrial environments, both displays require a single 5-V, 800-mA power supply only. Prices start at $280 for a 16-character display ($380 for 32 characters) and drop to below $200 in OEM quantities.

Circle 423 on Inquiry Card

SOFTWARE

Higher Level Language Utilizes Floating Point For F8 Microprocessor

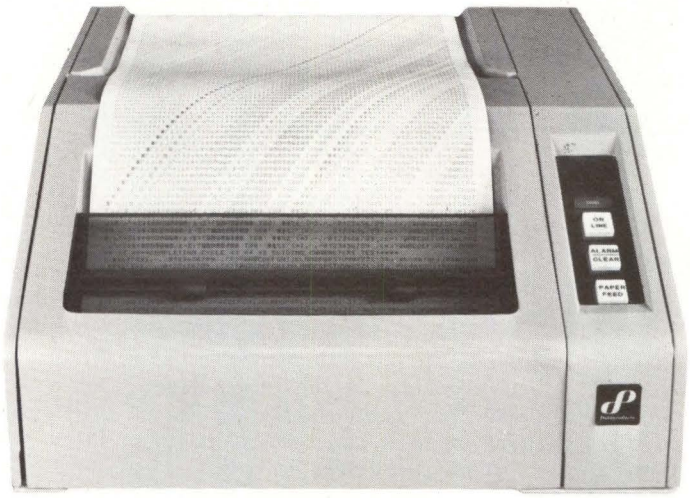
For use with Fairchild's F8 microprocessor, the MBS-BASIC© interpreter is comparable in speed and efficiency with the 8080 and Z80 BASIC interpreter due to its 9-digit precision and floating point arithmetic. All standard arithmetic operations and relations, as well as string handling, have been included by Micro Business Systems, Inc, Box 8255, JFK Station, Boston, MA 02114. Version 1.0, distributed on ASR 33 compatible paper tape with documentation, has a license fee of $179.95.

Circle 424 on Inquiry Card

Standalone Editor, Debug System, and Assembler Run With 6500 Family

E/65 text editor, A/65 2-pass assembler, and DB/65 debug system, all designed for the 6500 microprocessor family, have been announced by Computer Applications Corp, 413 Kellogg, Ames, IA 50010. E/65 is primarily designed to edit assembler source code. Line oriented commands specify I/O of text, and

KEEPS QUIET. WORKS HARD. FOR VERY LITTLE.



THE T-80 THERMAL PRINTER

Our T-80 Receive Only printer is a quiet, unassuming sort. Doesn't take up much room on the desk. Doesn't make a racket while it's doing its work.

And it doesn't require a lot of money before it'll go to work. In fact, the T-80 runs less than $900 in OEM quantities. And it continues to save you money with its low cost of ownership.

On top of all this, the T-80 prints fast. 80 CPS fast. Which is nearly three times faster than most other thermal printers.

All these qualities — low price, impressive speed, high quality, and quiet operation — have combined to make the T-80 an absolute natural for applications that demand silence. Hospitals. Open office situations. Testing and instrumentation.

And the T-80 is the logical supplement to your CRT if you want occasional hard copy printouts.

Now, you don't have to buy a T-80 RO to get T-80 performance. The basic T-80 mechanism, with the same unique operator-replaceable print head and driver electronics, is available as a module: the T-80 M.

So, it's up to you. Buy the complete T-80 RO, ready-to-run. Or just take the T-80 M mechanism and design your own printer around it.

Either way, you save money, and the T-80 goes quickly and quietly about its business.

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find specific lines to be edited. User can search for and optionally change a text string using string oriented commands. Character oriented commands allow cursor positioning and character deletion. Text may be loaded from or dumped to a bulk device other than the system terminal. A second entry point allows editing of text already in memory.

A/65 conforms exactly to specifications set forth in Rockwell and MOS Technology cross-assembler manuals. A full range of runtime options are provided to control listing formats, printing of generated code for ASCII strings, and generation of object code. Object code may be stored directly in memory, or output to a file the same as or different from the listing device; an assembly may be made for listing only, object code only, or both.

DB/65 is a complete hardware/software debug system. P/ROM resident monitor includes hardware breakpoint, eight software breakpoints, an infinite number of realtime software breakpoints using the BRK instruction, symbolic disassembly of user program, program trace of instructions and registers, scope sync output, single step, and a stack of instruction addresses. The system comes complete with 2k static RAM, and sockets for an additional 6k RAM. Any standard RS-232-C or current loop terminal, with a speed range of 110 to 9600 baud, is supported. If a current loop terminal is used, only a single 5-V power supply is needed.

E/65 and A/65 are priced at $100 each, prepaid. DB/65 price is $1450, with delivery from stock to 60 days.

Circle 425 on Inquiry Card

Software Enhances Debugging Capabilities Of COSMAC Micromonitor

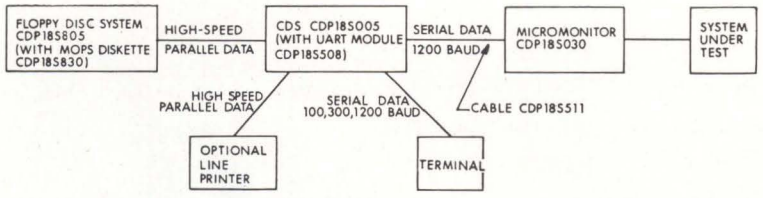
Realtime, in-circuit hardware and software debugging techniques ranging from simple terminal-Micromonitor dialogue to hands-off system testing with commands coming from disc files are obtained from the Micromonitor Operating System (MOPS) CDP18S831 software package. RCA Solid State Div, Rt 202, Somerville, NJ 08876 has introduced the package to supplement the performance of the COSMAC Micromonitor CDP18S030 (*Computer Design*, Dec 1977, p 126) by providing the user with access to the processing and storage capabilities of the COSMAC Development System (CDS) II (CDP18S005) equipped with the CDP18S805 floppy disc system.

Software consists of a MOPS diskette with a UART module and connecting cable to interface the Micromonitor to the CDS. Commands to the system are input at the terminal or are taken from command files on disc. System responses can be directed to the terminal, disc file, or both.

An extended set of Micromonitor-type commands are utilized. These include commands that switch Micromonitor commands and responses to and from system peripherals; allow greater interrogation of the CPU state; load the system under test from a disc file; save the system under test memory, registers, etc, in disc file; and facilitate automation in system debugging and testing.

Once entered to the system, standard Micromonitor commands are directed to the Micromonitor through its serial interface. Those from the extended set are trapped and processed by the operating system. In either case, the operating system provides line by line command editing capability. Single quantity prices are $350.

Circle 426 on Inquiry Card



System is configured to utilize RCA's MOPS software for CDP18S831 Micromonitor. Commands are input at terminal or taken from disc's command files. Serial interface provides standard commands to Micromonitor; extended commands are trapped and processed by operating system

Software Transfers EXORciser Programs to Development Labs

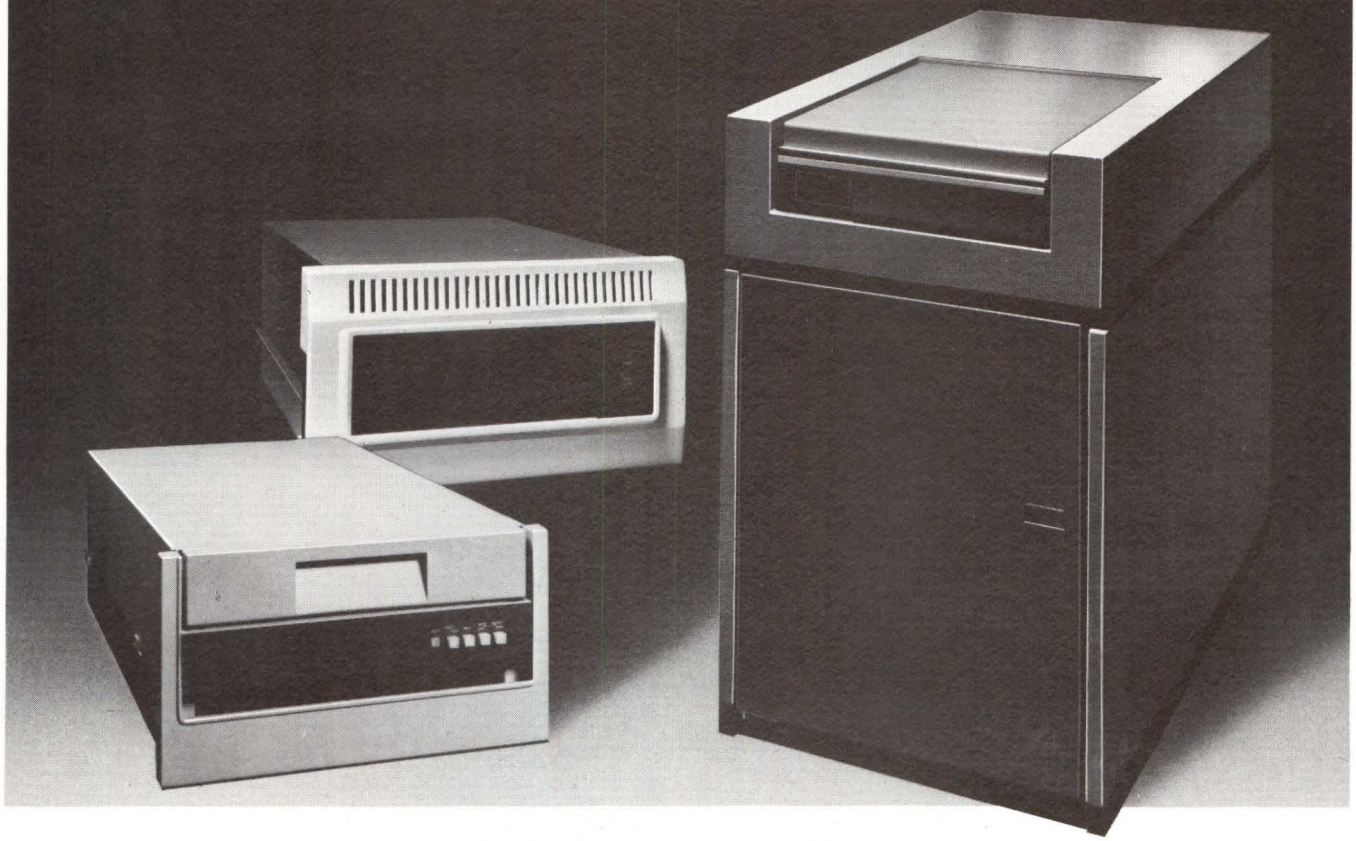
Users of the Motorola EXORciser™ microcomputer development system can retain existing programs while adding or switching to a Tektronix 8002 Microprocessor Development Lab for 6800 realtime emulation when sharing memory between the prototype and development system, and for realtime prototype analysis. The 6800 CONVERT program, offered by Tektronix, Inc, PO Box 500, Beaverton, OR 97077 at no additional charge with the 6800 software, translates 6800 programs from Motorola to Tektronix 6800 assembler format.

Input to the CONVERT program—source code written in Motorola's assembly language—may come from many peripheral devices. The 8002 provides the command for cross-loading source from the user's timesharing computer or EXORciser system. Motorola assembly language statement fields are replaced by the Tektronix equivalent; this reconciles such differences as reserved symbols, assembler directives, and expression syntax. All that may be required is minor editing of a few incompatibilities, which are indicated in CONVERT documentation. Output is Tektronix assembly language source code which can be used directly as input to the Tektronix 6800 assembler or edited.

Features of the 8002 relocatable assembler that aid in development of complex 6800 software are flexible macro capability, direct or zero-page addressing, handling of mathematical expressions, and string manipulation capability. Parts of existing programs may be linked to each other or to new programs. Thus, the converted program may be run as is or parts of it may be excerpted for inclusion in new programs. The development lab allows the designer to employ other microprocessors as well. □

Circle 427 on Inquiry Card

There are many measures of quality in an OEM module drive from Control Data.



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Our Storage Module Drive (SMD) has removable media. Our Mini-Module Drive (MMD) has fixed media. And our Cartridge Module Drive (CMD) has both. Capacities start at 12 megabytes and range to 300 megabytes.

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Control Data has a reputation for building module drives that last. We're backing it up with continued testing and feedback. And we design and manufacture all critical components in-house. We can build reliability into our drives because we built it into our heads, servos and media.

Value That Matches Performance

We know we have the best and most reliable drive for your application. But we also have the competition beat on cost of ownership.

Send us the coupon below. We will help you compare our lower cost-per-bit and our lower entry costs with others.

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CD-98

D..C. Steiner,
OEM General Manager, Product Sales
Control Data Corporation
P.O. Box 0, Minneapolis, MN 55440

Please send info on your ☐SMD ☐CMD ☐MMD

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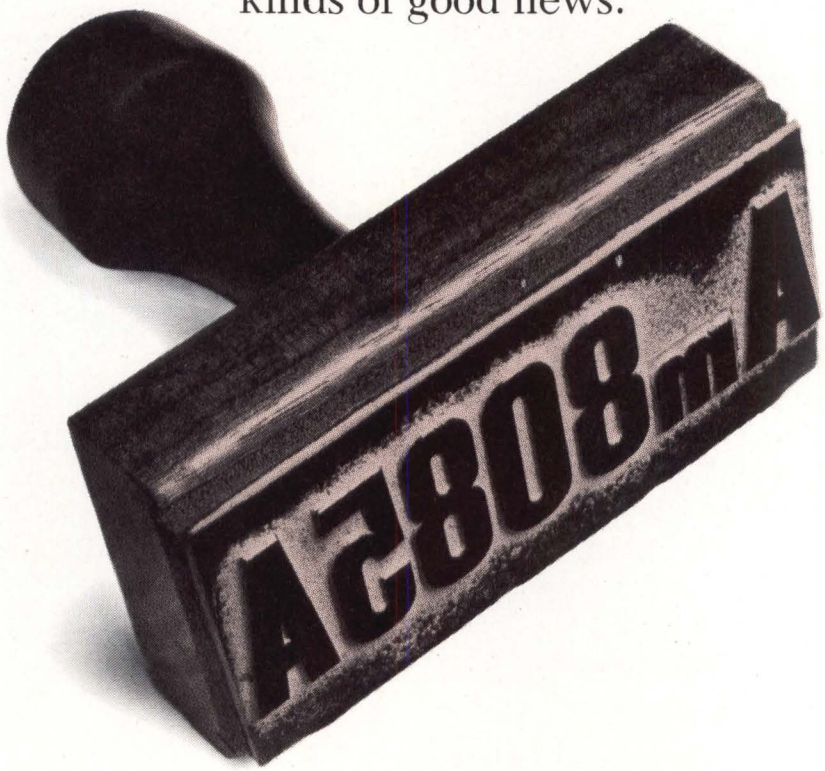
CONTROL DATA CORPORATION

More than a computer company

Advanced Micro Devices is second sourcing the industry standard 8085A, and that's two kinds of good news.



IT'S OFFICIAL.

First, the part. It's the next generation CPU. It significantly reduces the chip count. And it's totally compatible with all 8080A software.

Now the whole: Advanced Micro Devices.

That "Am" on the front of the Am8085A is like the "Am" on the front of the Am9080A. It means a continued commitment to better proprietary peripherals, better prices and absolutely no-lag, leading-edge second-sourcing. It means the rapid introduction of the 8155/56 (a 256-byte RAM) and the 8355 ROM. And of course it means MIL-STD-883 for free.

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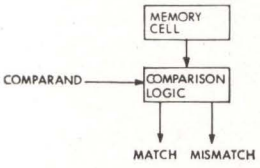
AN ADD-IN RECOGNITION MEMORY FOR S-100 BUS MICROCOMPUTERS— PART 2: STRUCTURE AND SPECIFICATIONS

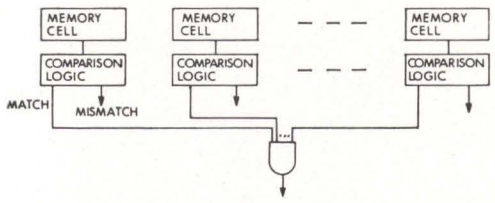
Sydney Lamb
Semionics Associates
Berkeley, California

Basics of recognition memory, a content addressable or associative computer memory that functions with any microprocessor connected to the S-100 bus, were introduced in Part 1 of this discussion (*Computer Design*, Aug 1978, pp 140-142). More extensive specifications and details of the memory's structure are presented in this continuation.

In prior art,* content addressable memory (CAM) designs have generally been varieties of the following principle. For each bit, there is a memory cell (eg, a flip-flop), and comparison logic (eg, an exclusive OR, if *equal to* is the only recognize function).



Then there must be a means of integrating the results of the bit-wise comparison. For example, the "match" outputs of the comparison cells for all bits of the word can be ANDed.



As an alternative, the "mismatch" lines can be connected to an OR.

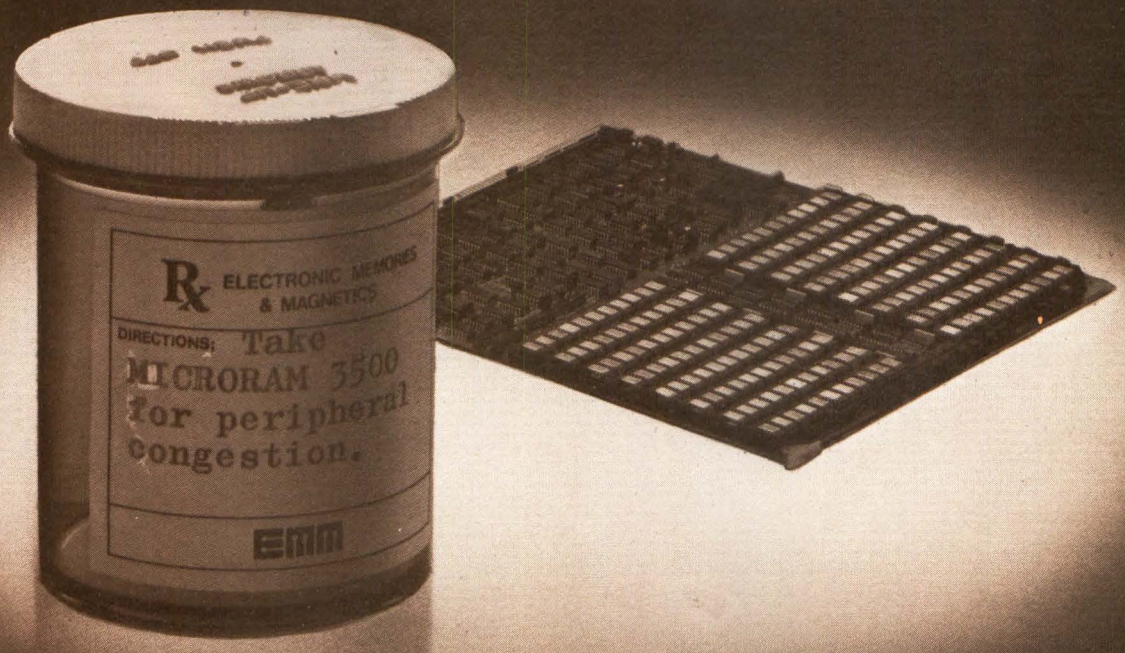
Obviously, CAM has more circuitry than a random-access memory (RAM), making it more expensive. Just how much more expensive, though, is surprising. Because of the economics of mass production of integrated circuits (ICs), prices can depend more on volume of production than on complexity of circuitry. For example, Intel Corp offers a CAM chip with a capacity of only 16 bits for $28.00 in quantities of 100 (speed is 35 ns). This comes to $1.75/bit. In contrast, the company also offers a 1k static RAM (45 ns) for $6.25 in the same quantities. (Both prices are for ceramic packages, as of July 1978.) This amounts to 0.61¢/bit. Thus, although the amount of circuitry per bit in CAM is roughly double that of RAM, the price per bit is greater by a factor of 287 to 1. If there were enough demand for CAM, density and production levels could increase and the price per bit could come down; the question, though, is how can demand increase at that price? This is the type of situation that has kept CAM almost unknown despite its far greater usefulness than RAM.

Simplification

At a closer look, it is possible to simplify the circuitry. Consider that as previously indicated, the ideal word size for CAM is much larger than that of ordinary computers. Therefore, either a special purpose central processing unit (CPU) can be built to go with the CAM, incurring still greater expense, or a CAM can be designed that easily interfaces with ordinary computers. The latter alternative has been chosen for recognition memory (REM). Now the ordinary computer has a relatively small word size, and can of course operate upon only one word at a time. Thus, if the word size is 8 bits and the REM superword is 256 bytes in length, the recognition of a sequence of bytes will

*Caxton C. Foster, *Content Addressable Parallel Processors*, Van Nostrand Reinhold, 1976

Rx for painful "make or buy" decisions



EMM multi-configuration memory

No longer need you agonize over whether to invest engineering and production time to build your own memories or settle for an available system that doesn't quite meet your requirements. The EMM MICRORAM 3500 multi-configuration memory makes all that pain unnecessary.

The 3500 offers 128K x 22 on a single card. But it can be depopulated down to 32K if that is more in line with your immediate needs, yet remain field-expandable up to maximum capacity.

The outstanding characteristic of the 3500, however, is the number and variety of available options. On-card options include ECC (single bit error correction and multiple bit error detection), and word or byte parity generation and checking. Other optional features include page mode, byte mode, error stop, a fault location LED display, and battery back-up.

No other comparable memory on the market today offers such an extensive "shopping list" of features and options. Call or write us today, and let us prescribe a configuration to solve your memory system problems.

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take place serially with respect to the several bytes of the comparand, but in parallel with respect to the superwords of the REM.

This means that if a traditional CAM design were used, only a small part of its comparison logic would be utilized at any one time. The system can be made more efficient by extracting the comparison logic from the individual bit cells (see Figure).

Besides being simpler, this design has all needed circuitry available in the form of mass produced ICs. Memory cells with the compare cells separated from them are just ordinary RAMs. As far as speed is concerned, simplification of the circuitry has cost nothing if interfaced with an ordinary CPU, since the CPU can only operate upon one computer word at a time anyway. It is necessarily serial with respect to a sequence of words.

Tag Bits

A CAM must have some means of integrating the results of the individual comparisons, for example by ANDing the "match" outputs of the compare logic cells. The 8-bit (or n-bit) compare logic modules of REM include such integration for their individual bits, but it is also necessary to integrate the results of comparisons over a sequence of words (bytes).

Since comparisons for the different bytes in the sequence are spread out in time, it is possible to use serial integration, which is structurally simpler than ANDing matches or ORing mismatches. It requires only a tag bit* for each REM superword, which is set to "true" at the beginning of a comparison. If there is a "false" (failure to meet the match or other recognition criterion) for any byte, the tag is set to false. At the end of the sequence of bytes compared, any superword whose tag still reads true has met the set of recognition criteria.

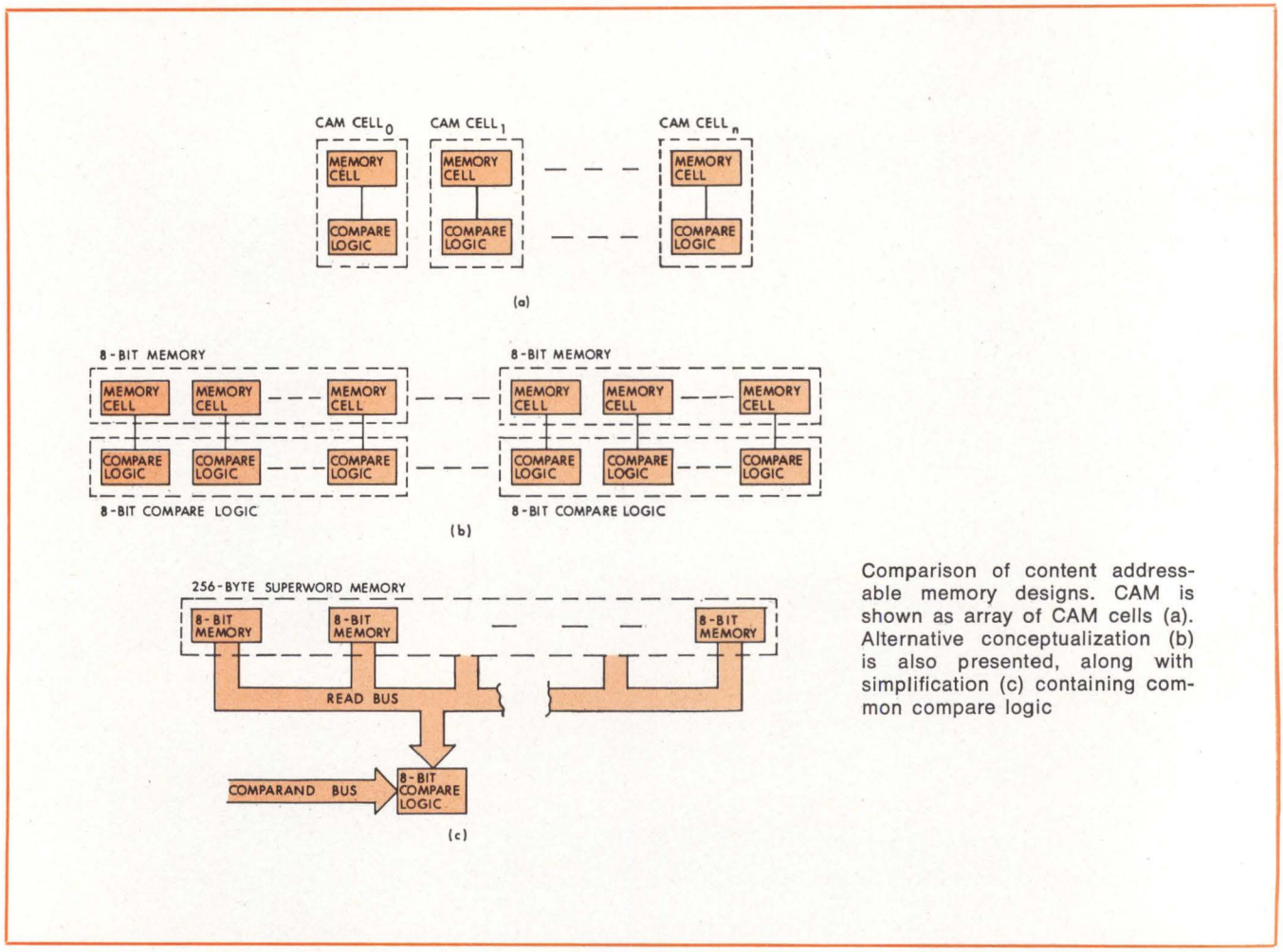
Nonmatch Comparisons

In REM, the comparison logic is elaborated to allow for six types of recognition: equal to (match), not equal to (mismatch), greater than, greater than or equal to, less than, and less than or equal to. In operating upon a sequence of bytes, the nonequal comparisons could lead to problems. For example, 1949 is less than 1978; yet looking at just the last digit (a byte if the numbers are coded in ASCII), the reverse is true. It is thus necessary, if going through the sequence from left to right, to "lock" the comparison "true" under the right circumstances. For this purpose, each superword has an associated lock bit in addition to its tag bit.

Suppose that we are asking for "greater than or equal to 1949." The tag bits of all superwords are set to true at the start of the comparison. For those superwords which have 1978, the tag will remain true for the first two bytes, where we have equality. On the third byte, there is not only true, but "decisively true," and the lock bit is set, since any subsequent false is irrelevant. The lock bit has the effect of keeping the tag bit true, even if there is a false on some subsequent individual byte.

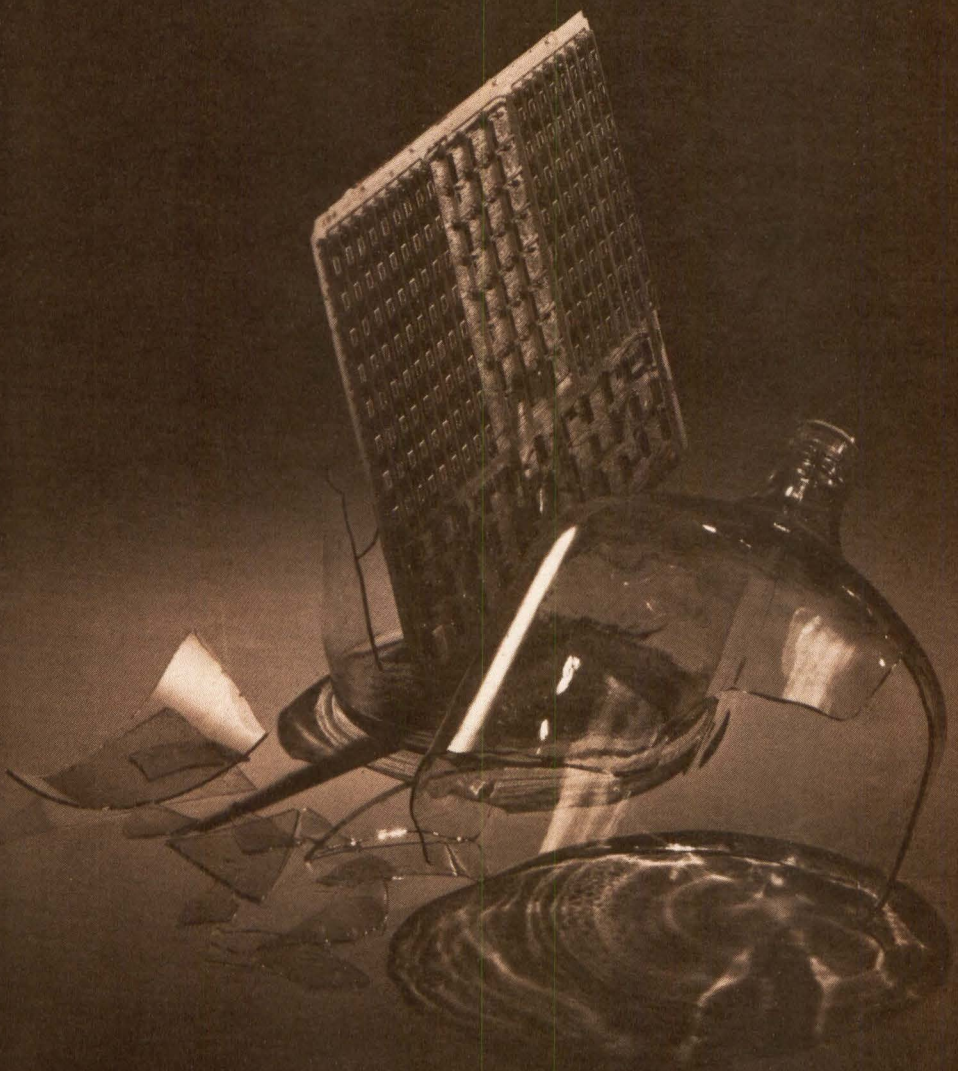
Masking

Each REM board includes a mask register whose length is that of the computer word. Masking can be used with



Comparison of content addressable memory designs. CAM is shown as array of CAM cells (a). Alternative conceptualization (b) is also presented, along with simplification (c) containing common compare logic

Break the Nova 3 bottleneck



with EMM 128K word memory

Let's face it. Even the Nova 3/12* has a limited number of card slots. In typical system applications, there just are not enough slots to accommodate needed memory, controllers, and usual options. It's the classic bottleneck and something has to give.

Relax. That's a thing of the past. With EMM's 7706 add-in memory you can put all the memory the system can handle — 128K words — into a single slot. That frees up 3 slots when compared with memory available from the computer manufacturer. If you don't need that much memory immediately, the 7706 is available in 32 and 64K versions as well. All are expandable to 128K. All offer significant cost advantages.

The 7706 is physically, electrically and functionally compatible with the Nova 3/4 and 3/12.

Call or write us today for complete details.

EMM

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CIRCLE 79 ON INQUIRY CARD

any of the memory operations, including ordinary read and write. The mask allows users to operate upon individual bits or upon any combination of bits in the byte. To perform a recognize on just the leftmost bit of a byte for example, the mask 10000000 is used.

The mask register is one of 256 input/output (I/O) ports available to the CPU. With a dual-inline package (DIP) switch on the REM board, used also for bank assignment, the user can specify any of 16 locations for the mask register. From the viewpoint of the CPU, the mask register is an output unit. It can be written into, but not read from. If there are multiple REM boards in the system, the several mask registers are given the same location number and are treated as a single unit by the CPU. Data are written to all of them in parallel.

For units larger than the byte, effective masking is available automatically without any additional structure. Those bytes which are not to be included in a comparison or multiwrite operation are simply skipped.

Specifying REM Operations

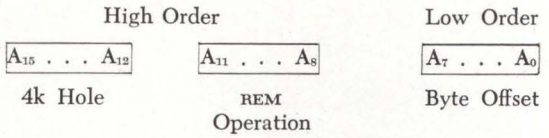
The add-in REM S-100 is able to convert an ordinary microcomputer to a content addressable parallel processor simply by being plugged into the S-100 bus. No changes to the CPU are needed.

Fortunately, certain properties of REM allow the CPU to specify REM operations, even though they are not in the instruction set of any microcomputer. The fact that REM functions operate in parallel on all superwords means that high order address bits are (largely) irrelevant. Since the superword length is 256, the low order address bits specify byte position within the superwords. However, we do not want to specify superword addresses, since all superwords are being operated on. Therefore, (some of) the high order address bits are not needed, making them available for specifying REM functions. In effect, they provide additional bits for operation codes. All REM actions use the CPU's write instruction, which is converted into the desired REM operation as specified by the high order address bits. Note that recognize operations require a comparand—data written by the CPU—which is the reason that a CPU write instruction is used for recognize operations.

Now it is neither possible nor necessary to use all eight high order address bits for this purpose. The system surely will have some RAM in it besides REM, for which the high order address bits must be used as such. Only enough bits are needed to specify a few REM operations, and some bits are needed to specify that it is *some* REM operation.

The system works as follows. First, there is a 4k "hole," an address space that is occupied neither by RAM nor by REM. More specifically, it is a 4k address space that cannot be occupied by anything that can be written into. It can be left empty, or it can be occupied by P/ROMS—and what better use than to put a package of REM subroutines on P/ROMS in this space. The 4-bit address (A_{15} to A_{12}) of this 4k hole, for instance 0111, specifies "REM action" when occurring with a write instruction. The REM S-100 board is designed to allow the user to select any of 16 possible 4k sections of address space as the hole, by means of a 4-bit DIP switch.

The remaining four bits of high address are used to specify individual REM operations and optionally to set the tag bits true (ordinarily done at the start of a sequence of recognize operations). Thus, the address bits function with write instructions to designate REM actions.



Of the four bits for REM operations, three are used for eight different REM functions, while the last one affects the setting of the tag bits and lock bits. Eight basic REM functions and their codes occupy A_{11} to A_9.

Multiwrite		Code
Multiwrite nonresponders		000
Multiwrite responders		001
Recognize		
REM field equal to	Comparand	010
REM field not equal to	Comparand	011
REM field greater than or equal to	Comparand	100
REM field greater than	Comparand	101
REM field less than or equal to	Comparand	110
REM field less than	Comparand	111

Any of the recognize functions may be used with either 0 or 1 in position A_8. A 0 sets the tag bits true and unlocks the lock bits (actions normally appropriate at the start of a sequence of recognize operations).

Data written on the data bus by the CPU are the comparand (item to be recognized) or data to be multiwritten. To illustrate, a sequence of write instructions with the following data and addresses will tag all superwords which have FOSTER in byte positions 0 through 5 if the hole address is 0111.

Data		Address		
F	Set tag bits true	0111	0100	00000000
O		0111	0101	00000001
S		0111	0101	00000010
T		0111	0101	00000011
E	Do not set tag bits	0111	0101	00000100
R		0111	0101	00000101
		Hole: REM Action	Match	Byte Offset

For multiwriting into all responders, the same convention is used: 0 in A_8 sets the tag bits true at the beginning of the operation, while 1 in this position leaves them unset. Multiwrite with tags unset is used to write into superwords which have responded to a preceding series of recognize operations. With tags set, the multiwrite writes into all superwords, since all are set true by the operation.

For multiwrite into nonresponders, only 1 may be used in position A_8—to reset the tag bits would render the operation vacuous as there would not be any nonresponders into which to write. Instead, the code 0000 in A_{11} to A_8 is used for two special operations, which are distinguished by 1 or 0 in A_7.

A_{11} to A_7	
0000 0	Set tag bits but do not unlock lock bits
0000 1	Unlock lock bits but do not set tag bits

The latter is used to change from one inequality comparison to another within the same sequence of recognize operations. The former is not commonly used in any obvious way, but is available to the clever programmer

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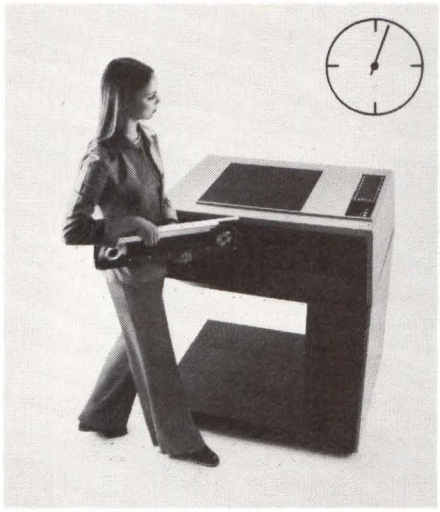

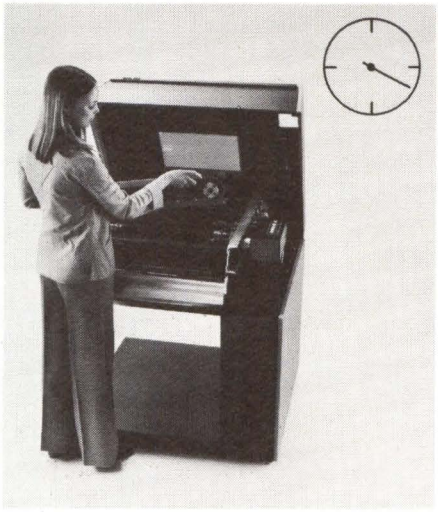

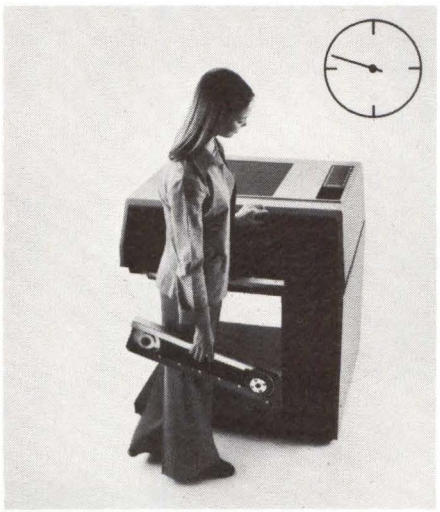

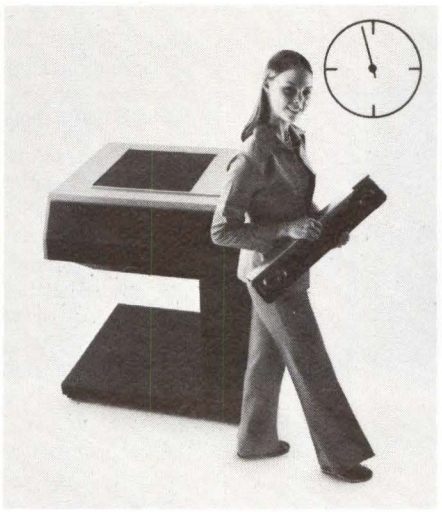

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for special situations. Position A_7 is one of the low order address bits, but these two operations do not involve any byte offset, so A_7 is available.

When performing recognition operations upon a sequence of bytes, the comparand normally is stored somewhere in RAM, and the CPU accordingly operates as if it is performing a data transfer from one block of memory to another. If the microprocessor is the Z80, the block transfer instruction may be used for this purpose. It operates at 21 cycles/byte, which amounts to 5.25 μs if the Z80 is operating at 4 MHz. Since the recognize operation requires only approximately 4 μs/byte, it can take place as quickly as the Z80 can do the block transfer when operating at 4 MHz. The same is true for multiwriting a sequence of bytes. Even when the block transfer operation is not being used in connection with REM operations, the 4-μs time requirement does not generally occasion wait states. The CPU is free to do anything it wants after the start of the REM action. Only if it accesses REM again before the REM action is complete (approximately 4 μs) are wait states put in.

Reading Responders

At the end of a sequence of recognize operations, tag bits will still be true for all superwords that have satisfied all comparisons. The next problem is how to get them. The answer comes in two parts. First, for many purposes it is not necessary to do anything further. Thus, to write some information into all the responders, it is only necessary to use the "multiwrite responders" operation which operates on all superwords with a true tag bit. Knowing where things are, essential for users of Von Neumann machines, is no longer so important.

Second, in cases where it is really necessary to locate individual responders, they must first be flagged by means of a multiwrite operation, and then the records with flags must be located. In systems with a relatively small amount of REM, such as two 4k boards, it takes very little time to loop through all 32 superwords looking for the flagged ones. For larger systems, there is a special device for narrowing down the possibilities. Each 4k block of REM has a responder bit, and up to eight different responder bits (for eight 4k boards) may be read into the CPU at a time from the responder port. The responder port is any of the computer's 256 available I/O ports, as selected by a DIP switch on the REM board. With a jumper on the REM board, the user may choose any of eight bits for the 4k block on the board. The responder bit for a 4k block is a 1 if any of the 16 superwords in that block is a responder.

It can be valuable to use the responder ports for applications in which, at some point in a sequence of recognize operations, it is desirable to know if there are any responders at all (if not, perhaps the remaining recognize operations may be dispensed with). Reading a responder port will give an immediate yes/no answer for up to eight 4k blocks (32k) of REM.

Address Space and Bank Selection

The 4k REM board has jumpers for selecting any of 16 blocks of address space, for use in RAM mode. In large systems a DIP switch is used to assign the board to a memory bank. Bank selection is relevant only for RAM operations, since REM operations apply to all REM boards in parallel. The user may have up to 15 banks of REM, each of which contains from 8k to 32k bytes (2 to 8 boards). Multiple banks must occupy the same region, as specified by the four high order bits of the 8-bit DIP switch. That is, all the boards must agree with respect to those four bits. The four low order bits may be set for any of the 15 values from 0 to 14 (0000 to 1110). Position 15 (1111) is reserved for the mask register.

Bank select, for the sake of RAM operations, is accomplished as selection of an I/O port. The 8-bit assignment of the DIP switch is the port address. The 15 available bank positions are selected from the 256 I/O ports. Bank select consists of an output command with the appropriate I/O port address. An input command with the same port address is used for reading responders from the board. Thus, the same port address applies for bank assignment and for responder port assignment.

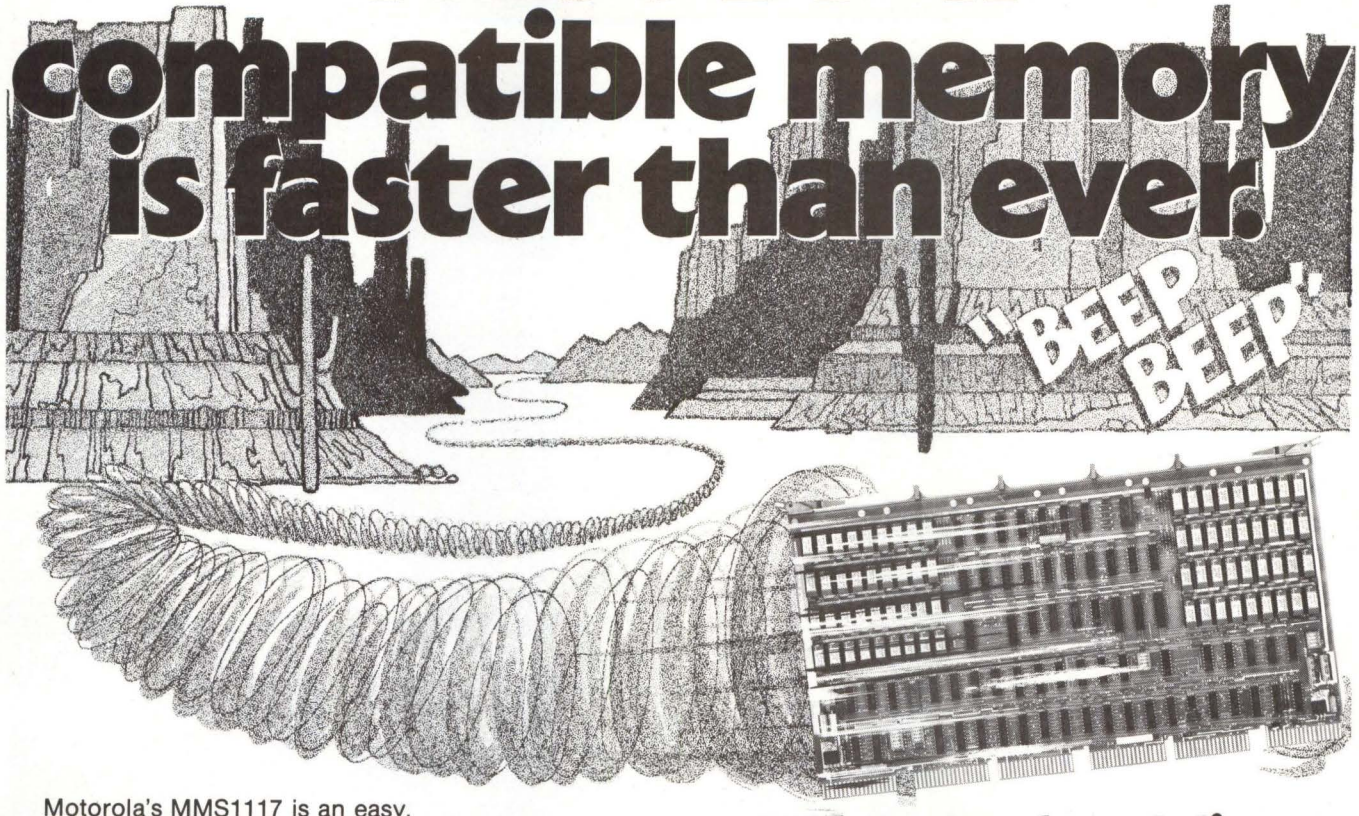
REM Board Specifications

The 4k REM board for the S-100 bus meets a variety of physical specifications. In summary, the board, with a capacity of 4096 bytes, is organized into 8-bit words and 256-word superwords (REM records). The design utilizes static, n-channel metal oxide semiconductor, single voltage memory technology, resulting in memory access and cycle times of 200 ns each. Power requirements are 8 V at 1.6 A; operating temperature range is 0 to 55 °C.

Recognize functions, mentioned previously, take place in 4 μs. Occurring at the same rate are multiwrite functions (all superwords, responders, or nonresponders). User selectable options include hole address (4-bit DIP switch), bank and responder port assignment (8-bit DIP switch), 4k address space (jumpers), and response bits (jumper).

Comparable with RAM, REM in addition features parallel processing. Combined with its increased processing speed and simplification of software, the memory is applicable to a wide area of computer applications. These aspects will be further developed in next month's column.

This PDP-11* compatible memory is faster than ever.



Motorola's MMS1117 is an easy, inexpensive way to add-in high-density, high-speed storage with parity option features for your PDP-11 system. Now it's more than 20% faster than ever before. Speeds for all three MMS1117 speed options are significantly faster, with typical system Read Access Time of the fastest version reduced from 370 ns to 290 ns.

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Each speed option of the MMS1117 is available in your choice of 32, 64, 96, or 128 kilobytes. Each offers parity plus on-board parity generation and checking logic. There's no need for an external parity control module. The system imposes one UNIBUS load regardless of memory size and parity.

MMS1117 power requirements are low despite its speed and density. A fully populated 128 kilobyte system with parity and controller operates at the following rates: 5 V ±5% @ 3.0 A (typ), +15 V @ 0.2 A standby or 0.7 A continuous maximum access, and -15 V @ 0.03 A.

128 Kilobyte MMS 1117

Speed Option	Read Access Time (typical)	Price 1-5
Fastest	290 ns	$4,305
Faster	360 ns	$3,920
Fast	390 ns	$3,530

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System	Organization	Description
MMS1110 MMS1110-1 MMS1110-2 MMS1110-3	16K x 16 12K x 16 8K x 16 4K x 16	Add-in for LSI-11 systems
MMS1118L	16K x 18	Add-in for PDP-11/05, 11/10, 11/35 and 11/40 systems with the MF11-L backplane
MMS1118 MMS1118-1 MMS1118-2	16K x 18 12K x 18 8K x 18	Add-in for PDP-11/04, 11/34 systems
MMS3400	32K x 18 or 64K x 9	For 3400N systems
MMS68102 MMS68102-1 MMS68102A MMS68102A-1	16K x 8 8K x 8 16K x 9 8K x 9	Battery backup for M6800 and other synchronous systems; pin-compatible with EXORciser† micromodule
MMS68103 MMS68103-1 MMS68103A MMS68103A-1	16K x 8 8K x 8 16K x 9 8K x 9	Hidden refresh for M6800-based systems
MMS68104	16K x 8	For MEK6800D2 Kit
MMS80810 MMS80810-1	32K x 8 16K x 8	For 8080A-based systems; pin-compatible with SBC 80/10 /20

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Our standard memory line also includes systems for the SBC 80/10 and 80/20, LSI-11, 3400N, and a variety of M6800-based systems. Motorola also has excellent custom capability for the design and manufacturing of memory systems to your exact specifications.

Regardless of your requirements, you can expect fast delivery, leadership pricing, and the high level of reliability for which Motorola products are known.

Assistance is available from your Motorola sales office. Request a copy of the MMS1117 data sheet by writing Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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CIRCLE 82 ON INQUIRY CARD

The intelligent memory for PDP®-11/70's.

More than bits in a box. The MSC 3602 PDP-11/70 add-on memory has its own microcomputer that keeps it, your 11/70 and you out of trouble.

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Turn off the ECC and you can run full diagnostics.

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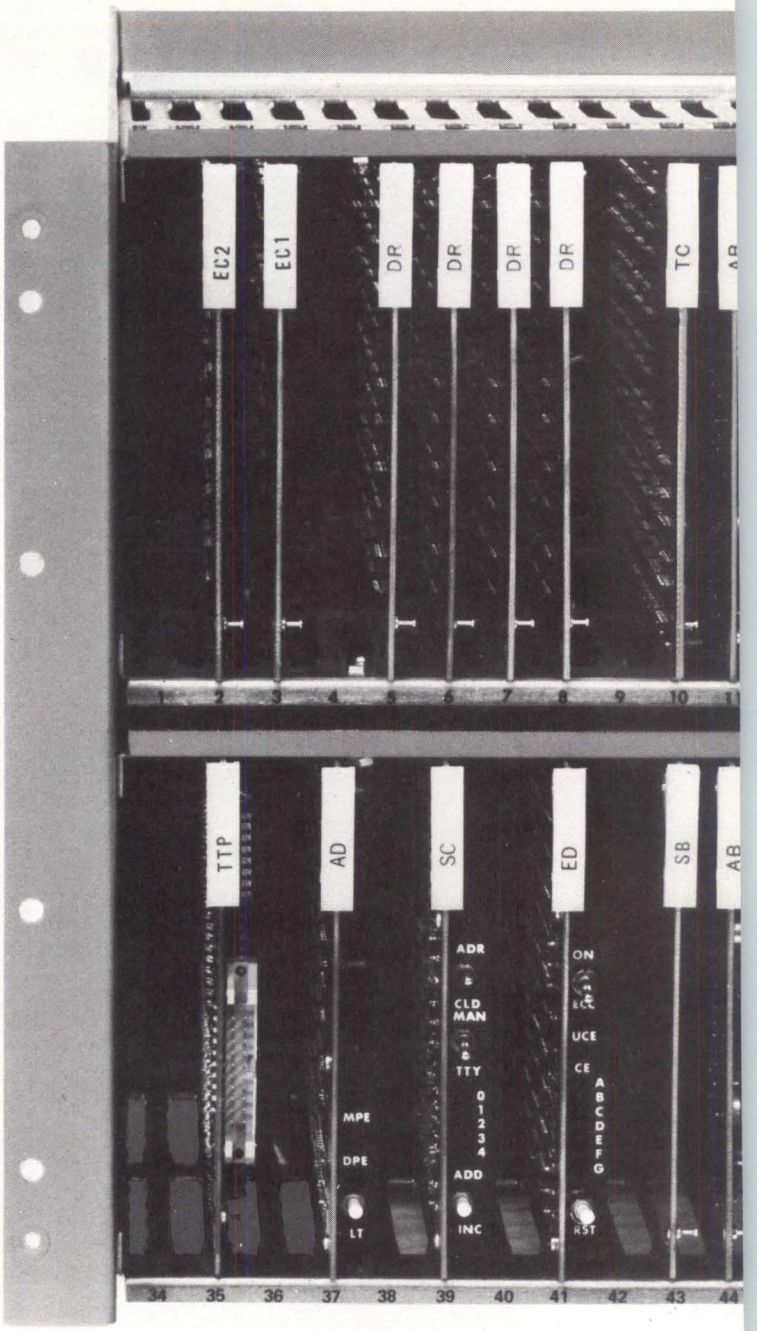
Memorizing more? The MSC 3602 will grow with you. It's expandable in 64K byte increments, with 2 megabytes in a single 10½" high free-standing or rackmount chassis including power supply and forced air cooling. An additional 10½" chassis will give you the total 4 megabyte PDP-11/70 maximum memory.

And MOS memory offers you low power requirements. Nonvolatility is available with battery backup.



Intelligent design. The MSC 3602's small size allows close placement to the CPU. Shorter bus lengths allow higher speed and reduce noise problems.

Socketed elements offer easy maintenance.

All cards are removable from the front.

Taking care of you. The MSC 3602 will help your system and your budget. It is competitively priced with unintelligent core and semiconductor add-ons.

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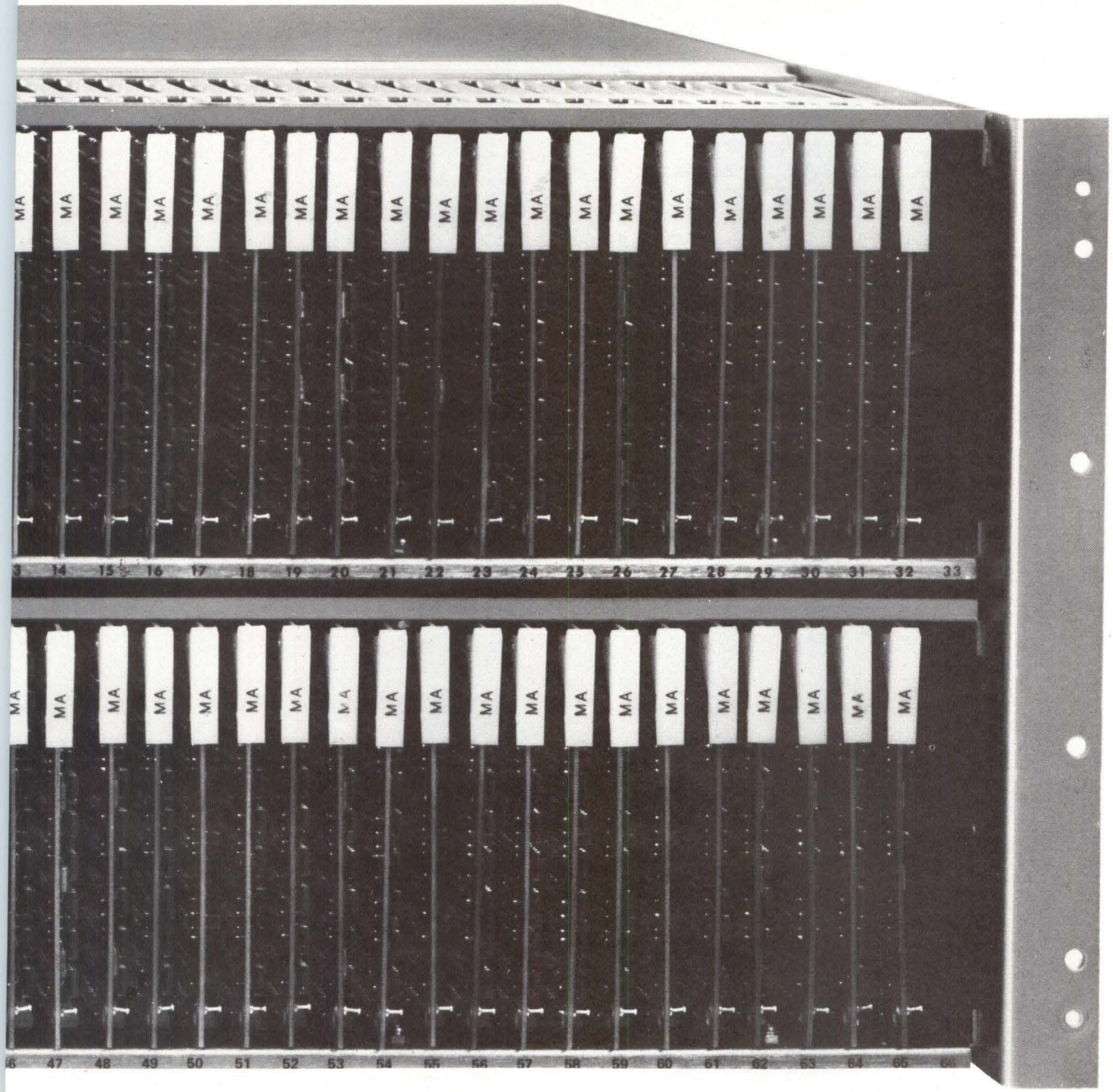

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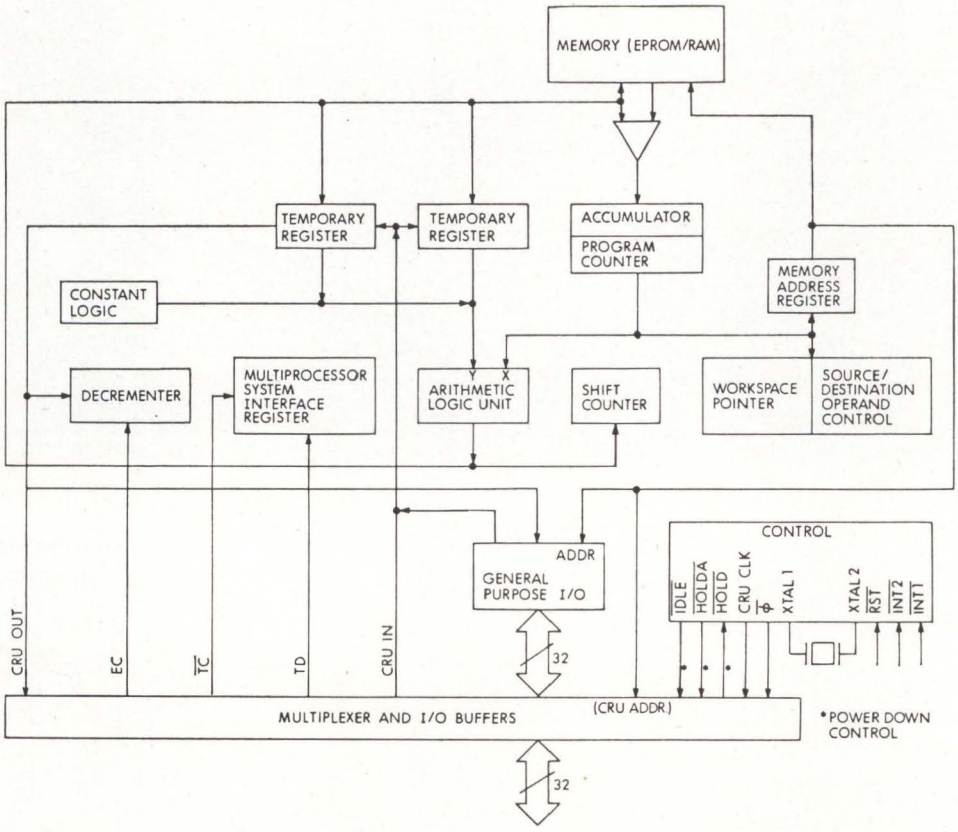
CIRCLE 83 ON INQUIRY CARD

Single-Chip 16-Bit Microcomputer With EPROM Operates In Control Applications

The latest member to be added to the 9900 family is a single-chip 16-bit microcomputer which is said by Texas Instruments Inc, Semiconductor Group, PO Box 1443, Houston, TX 77001 to be the only one with EPROM on chip. TMS 9940 also contains a CPU and extensive I/O. The instruction set used matches that of the TMS 9900 (except for four instructions that do not apply to the 9940 microcomputer). It offers minicomputer capabilities, including multiply and divide. Two instructions that facilitate manipulation of BCD data, and a single-word, load-interrupt-mask instruction are included.

Memory consists of 2048 bytes of EPROM (TMS 9940E)/ROM (TMS 9940M) and 128 bytes of RAM. Memory-to-memory architecture features multiple register files, resident in RAM, which allow faster response to interrupts and increased programming flexibility. With this structure, memory blocks designated as workspaces replace dedicated hardware registers with program data registers. Workspace-register files are nonoverlapping and contain 16 contiguous memory words. Four levels of prioritized interrupts are implemented, including an internal decrementer which can be programmed as a timer or event counter.

Memory is addressable in 8-bit bytes. A word is defined as 16 bits or two consecutive 8-bit bytes in memory. Three machine registers are accessible to the user. The 15-bit program counter contains the address of the instruction following the one currently being executed. The 16-bit status register contains the present state of the processor; the 11-bit work-



Advanced architecture of 16-bit TMS 9940 microcomputer developed by Texas Instruments includes CPU, control logic, memory (EPROM/ROM and RAM), and I/O capabilities on one chip to perform various control functions. Instruction set, similar to that of TMS 9900, includes capabilities of minicomputers

Miproc 16-AS, micropower to give you high-speed faster.

Internationally acclaimed Miproc-16 with a compute-rate of up to 4 million instructions per second is the fastest 16-bit microcomputer card family available.

Now supplied with an OEM chassis package, Miproc-16 is even more quickly brought into action.

This cost-effective application system, named Miproc-16 AS, has room for one, two or even three Miproc-16 CPU's. Smartly styled and equipped with add-in 13-slot card bay modules, fans and power supply, this new OEM chassis package eases the way into high speed microcomputing.

Instruction Power

Up to 170 instructions including multiply/divide and bit manipulation give Miproc-16 formidable processing capability.

16-bit Power

16-bit program words make programming easy. 16-bit data words maintain high precision in arithmetic operations.

Addressing Power

16-bit dual memory architecture gives 65k words of directly addressable program memory *and* 65k words of data memory with 8 powerful address modes.

Interrupt Power

Multilevel, priority vectored interrupt system handles context changes in less than 2 microseconds.

I/O Power

256 directly addressable I/O channels with data I/O rates of up to 1.7 megabytes/sec. under program control, and up to 20 megabytes/sec. for DMA.

High Speed Processing Power

The unique dual memory architecture combines with high speed Schottky TTL technology to execute most instructions in a single machine cycle.

Software Power

Easy to use cross-assemblers for mainframe or minicomputer make programming faster, *and* PL-MIPROC, a super-efficient high level assembly language.

Hardware Power

Comprehensive range of processor, memory and interface cards backed up by sophisticated hardware development aids.

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Miproc can be configured to meet any known military specification.

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space register points to the first word in the currently active set of workspace registers.

The chip has a communications register unit (CRU) drive I/O interface, with 32-bit, general purpose I/O ports. Individually controlled I/O lines can be independently programmed as input or output. While dedicated control system generally needs only one configuration setup, the software I/O structuring allows flexibility for multiple configurations dynamically changing for more I/O capacity. Direct I/O expansion for up to 256 bits is possible using a standard 9900 family CRU interface.

The 2-wire Multiprocessor System Interface (MPSI) transfers data in a multiple processor system. Since the microcomputer can execute instructions out of its RAM, MPSI allows instruction sequences to be downloaded and then executed. Thus, multiple processor systems can reconfigure themselves in system applications. The interface also can be used to transfer data to be operated on.

Also incorporated in the microcomputer are an internal 16-bit flag register and a 14-bit decrementing register which functions as a programmable realtime clock, event timer, or external event counter. Applications which have low duty cycles or which require low power dissipation can benefit from the power down capability to lower average power. Two supplies power the chip; one handles the RAM and interrupt logic, while the other powers the rest of the circuitry. Five speed ranges provide maximum performance.

Key features also include an easy test function, n-channel silicon gate MOS technology, and 5-V power supply. An EPROM device is contained in a 40-pin, 600-mil DIL ceramic package with quartz lid; a mask ROM device is contained in a 40-pin, 600-mil DIL plastic or ceramic package.

All members of the TMS 9900 family of peripheral circuits are compatible with the microcomputer. Four software and hardware development methods are available as support tools.

Circle 428 on Inquiry Card

Simple Language Is Featured in Personal Computing System

PeCos I incorporates comprehensive math capabilities, large memory capacity, and ease of programming in a simple, easy-to-learn computer language, according to APF Electronics, Inc, 444 Madison Ave, New York, NY 10022. The language is a derivative of Rand Corp's JOSS^R language, said to be the most English like computer language ever devised.

A math program permits full computation in 9-digit floating decimal arithmetic, with a number range from 1×10^{-99} to 1×10^{99}. All functions of a programmable calculator are built in, and include trigonometry, number dissection, string concatenation, transcendental functions, and ability to define functions.

Internal 24k ROM and 16k RAM are provided. Semiautomatically controlled integral dual cassette decks use standard audio cassettes, each storing up to 80k bytes. All I/O operations are done at a rate of 800-baud speed-tolerant recording.

Standard equipment supplied with the system is a 6502 microprocessor; power supply; 60-key keyboard with 110 codes and upper/lower case; 9" (22.9-cm) CRT with 16-line, 40-char/line display and automatic scrolling and speed control; dual cassette decks; and RS-232 transmit port for serial printer. Suggested retail price is $1695.

Circle 429 on Inquiry Card

Single-Chip μComputer Contains Onboard NMOS A-D Converter

All components necessary to implement many control-type applications are incorporated onboard the 8022 single-chip microcomputer, with little additional design required other than application program development. Containing a full A-D converter, the chip eliminates the need for and cost of external ADCs in applications where the OEM is interfacing analog signals. In addition, the microcomputer is software compatible with other single-chip microcomputers in the MCS-48 family.

Claimed by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051 to be the first low cost, single-chip microcomputer with ADC, the 8022 has been optimized for control applications. Various capabilities include three 8-bit input ports which, in conjunction with the ADC, permit the chip to interface up to eight analog signals; zero cross detection for creating a realtime clock or timing of an event that can be synchronized with the movement of an ac sine wave; interrupt capability for reacting to and handling randomly occurring events; and ability to operate from a 4.5- to 6.5-V power supply.

If drive is needed for high current output, two lines on the chip can drive up to 7 mA each. Input port 0 contains high gain variable threshold inputs to permit direct interface with a low voltage capacitive touchpanel; other I/O ports have high drive current output capability as well as standard interface capability.

Besides these features, the chip serves OEMS as a complete, standalone single-chip system containing an 8-bit CPU, internal timer and external interrupt capability, 64 bytes of programmable RAM, 2048 bytes of program memory to accommodate larger more complex programs, 26 programmable I/O lines, programmable interval timer/event counter, and onchip system clock and oscillator. A subset of the 8048 instruction set is executed. Hardware capability is increased by instructions that affect the contents of the accumulator, address data memory locations, provide BCD arithmetic, and allow easy table lookup, thereby reducing the amount of programming software required.

An 8-bit monotonic A-D converter has two multiplexed input channels that are selected by software. This allows inexpensive, direct interfaces to analog signals. An updated conversion takes place once every 40 μs for high speed applications; several readings can be averaged for greater accuracy. ADC implementation is in NMOS technology using a hardware successive approximation technique.

(Continued on p 178)

FREE! SPEED READING COURSE.

DECITEK's free SPEED READING COURSE gives full details on new Model 262D9 desktop punched tape reader. (The model that reads 300 cps and recognizes XON and XOFF ASCII characters as well.)

Please rush details. I understand this brush-up course on the latest in tape readers does not obligate me in any way.

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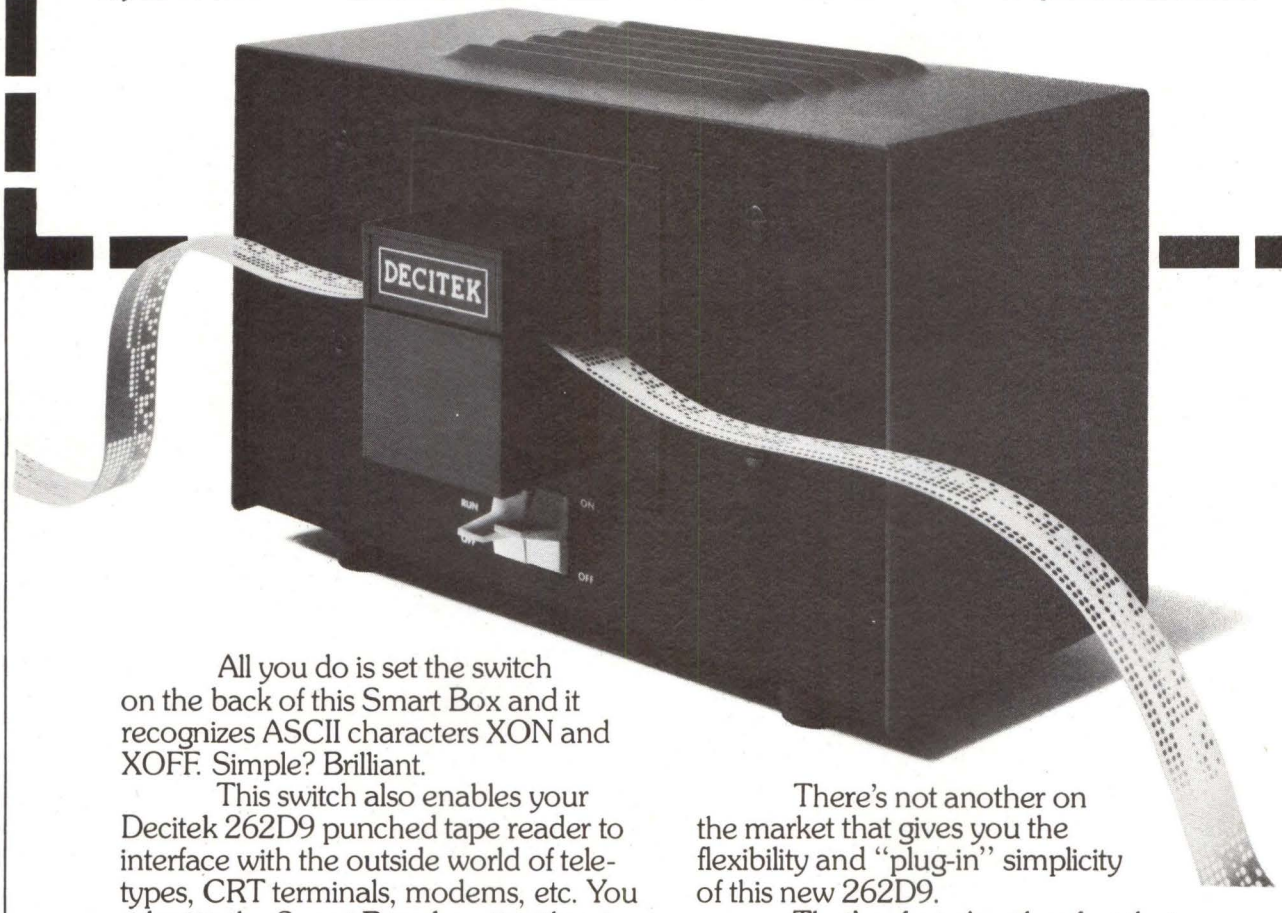

All you do is set the switch on the back of this Smart Box and it recognizes ASCII characters XON and XOFF. Simple? Brilliant.

This switch also enables your Decitek 262D9 punched tape reader to interface with the outside world of teletypes, CRT terminals, modems, etc. You select it, the Smart Box does it without internal programming by jumpers.

Then, using the second mode selector on the rear panel, you can program transmission rate (from 110 to 9600 baud), word length, parity and number of stop bits.

There's a lot more to this intelligent box. Dual-sprocket drive, 25,000 hour light source with fiber optics and stepper motor drive – that's a lot of tape reader. Add-on fan-fold boxes and 19" wing adapters provide installation versatility if you need it.

There's not another on the market that gives you the flexibility and "plug-in" simplicity of this new 262D9.

That's a fact. Another fact that will interest you is the reasonable cost of this improved Smart Box. So, do the smart thing. Mail the coupon for the FREE Speed Reading Course. Or, if you're in a hurry, call (617) 366-8334. Get the facts over the phone.

When reading matters

DECITEK

A Division of Jamesbury Corp.
129 Flanders Road, Westboro, Massachusetts 01581

Now. A static that won't give you upgrade.

Maxi-ROM™ family static when you

Welcome to the complete fully static Maxi-ROM family from National. 16K, 32K and 64K. Each completely pin compatible as specified by the JEDEC 24-pin standard.

We've made each one pin compatible so there won't be any problems when you update and change from 8K to 16K. Or 32K to 64K. There's no reason to redesign. You can take what you're currently doing as far as it goes.

Speed? Our access time is 450 ns—the same as required by most ROM applications. What's more, all ROM's in our Maxi-ROM family use a single +5V supply. They also use a streamlined NMOS ROM process. And since they're fully static, they require no clock so you can save money and precious space.

If you want big static ROM's but don't want static, check out National's complete Maxi-ROM family. Just send in the coupon below for all the information.

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, CA 95051

Gentlemen: Send me the full story on your Maxi-ROM family.

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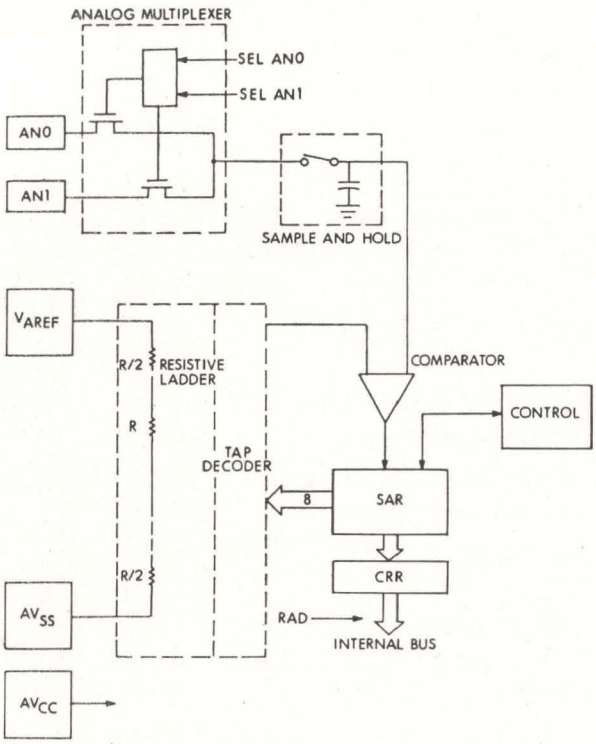
Address _____

City _____ State _____ Zip _____

CD-9

National Semiconductor



Intel's 8022 single-chip microcomputer for control applications features a 2-channel, NMOS, 8-bit A-D converter onboard. Converter hardware has three parts: series string of 256 identical resistors, voltage comparator, and successive approximation logic. Resistor configuration gives inherent monotonicity. Decoder presents voltage to comparator block. Comparator amplifies difference between analog input and voltage tap, presenting it to successive approximation logic. After eight such comparisons are automatically performed, resultant byte is transferred to conversion result register (CRR). RAD instruction moves CRR contents to the 8022 accumulator

Separate power supply and voltage reference pins on the chip afford maximum ADC accuracy.

Programs are stored in masked ROM. Applications are developed on the EM-2 emulator board which contains a 2048-byte 8755 EPROM/IO device to emulate 8022 ROM applications. An EPROM equivalent version of the 8022 is provided, speeding development and prototyping while avoiding repetitious masking charges. An Intellec® Microcomputer Development System with resident MCS-48 Macro Assembler is used for automated assembly language programming.

The microcomputer is priced at $15 in 1000-piece quantities. In large OEM quantities it drops to the $6 to $8 range.

Circle 430 on Inquiry Card

Custom Microcomputer Peripheral Drives Medium Power Loads

Under control of a microcomputer, the RS-16-I universal control interface can drive 16 medium power loads, such as relays and small dc motors. The unit, available from Cooper Computing, PO Box 16082, Clayton, MO 63105, can also sense 16 to 24 switch contacts or TTL inputs via a single 8-bit parallel I/O port. Each output line can be individually set or cleared using BASIC, machine code, or other language by means of I/O read or write commands. All outputs can be cleared simultaneously by use of a special command, or by the manual reset button. Wiring-in simple switches allows manual override of computer commands.

The 16 external status conditions can be selectively sensed by condition number; 8 inputs sense levels, and the other 8 either levels or pulses. A single removable connector accommodates all relay, switch, and logic connections.

In the event of interface failure, a special connector having looped-back wiring can be substituted, allowing faulty ICs to be found and replaced by means of a diagnostic BASIC program. The unit is priced at $229, assembled and tested, with sample BASIC programs and installation guide.

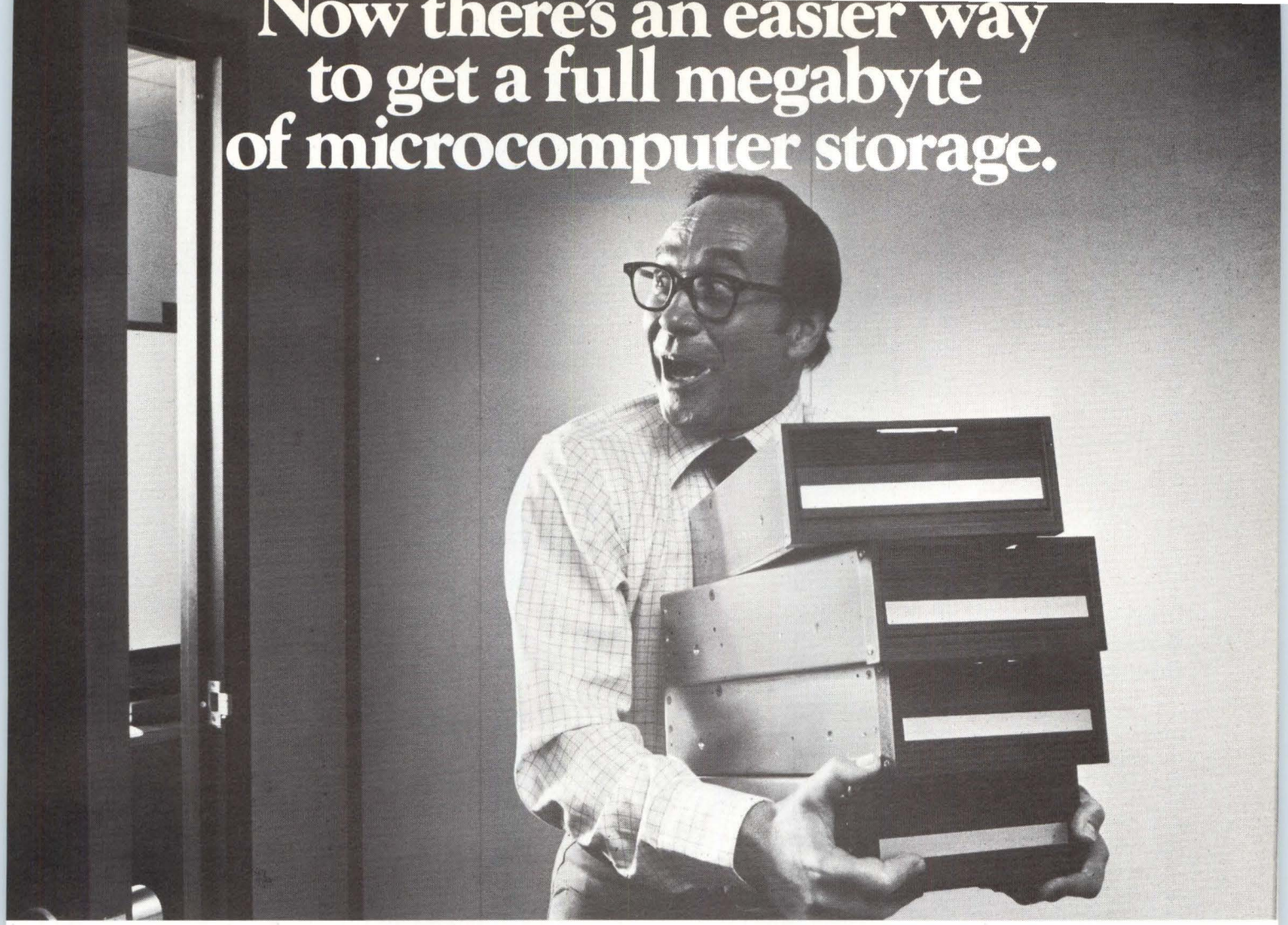
Circle 431 on Inquiry Card

Small Computer System Emphasizes Availability of Software

The LYS 16 computer is based on a 16-bit CPU using GPC/P 4-bit slice processors. Standard instruction repertoire contains 59 instructions including double precision add, subtract, multiply, and divide. Internal memory accepts any combination of RAM and ROM up to 64k words. Up to 64 external units can be connected to the I/O bus. Components of the system, available as a kit or assembled, include CPU, 4k RAM, operating system in P/ROM, RS-232/V24 interface, power supply, and manuals.

Emphasis is placed on the availability of system software to the user. The library therefore contains such offerings as ECONOMIST 1 for small com-

Now there's an easier way to get a full megabyte of microcomputer storage.



iCOM® gives you a full megabyte of microcomputer storage in our new FD3812 floppy disk system. It's a complete, intelligent system that includes two floppy disk drives, a built-in double-density controller that can handle up to four drives, power supply and cabinet. You get a compact, powerful package that simplifies your design at a price you might expect to pay for a single-density system. For use with any S-100 bus, Intel Multibus™ and others.

IBM format.

Our new FD3812 microcomputer floppy disk subsystem is compatible with the IBM double-density format used for single sided recording. And, it has the kind of features that have made iCOM the first name in Microperipherals®. Like retractable heads that extend media life. Long-lasting proven ferrite read/write heads. And, the option of direct memory access data transfer to and from the disk.

Easy conversion for FD3712 users.

If you're using our FD3712 disk systems, we've made it easy for you to move up to our new FD3812 and double your storage capacity—using our application note for system upgrade. The FD3812's cabinet size is the same. And, our double-density controller's electronics are contained on a single, compact board.

Frugal Floppy™.

We even have a "frugal" version of the FD3812 which means you have the controller and drive without the power supply and cabinet. You can order a single drive with controller. And drives can be positioned vertically or horizontally in standard EIA cabinets.

A Real Time Saver, too.

Available with our FD3812 is our exclusive Real Time Saver, a tightly written real-time operating system (RTOS) that cuts software development time, shortens lead time, and reduces programming time. In addition, the FD3812 is available with CP/M™ operating system.

For more information on the FD3812 or other iCOM Microperipherals, call us today at (213) 998-1800, TWX (910) 494-2093. Or write iCOM, 20630 Nordhoff Street, Chatsworth, CA 91311.

iCOM®, the first name in Microperipherals®

icom®

Products of Pertec Computer Corporation

Built and backed by Pertec Computer Corporation (world's leading independent producer of computer peripheral equipment and distributed processing and data entry systems).

CIRCLE 86 ON INQUIRY CARD

panies; BASIC 1; PL/L; LYSASM linked editor and assembler; LYSEDIT, a 4k-byte text editor; and FASM, a 4k-byte assembler, as well as packages of debugging programs, graphical subroutines, and a PACE crossassembler. Timesharing and Extended BASIC, inventory packages, and crossassemblers to the 8080, 6800, and SC/MP will be available at a later date. The manufacturer, AB ATEW, Box 125, S-642 00 Flen, Sweden, is also offering TERMI-LYS, a video terminal with both alphanumerical and graphical capabilities.
Circle 432 on Inquiry Card

Individual Modules Combine Into Autonomous Development System

A variety of boards and elements comprise the M68ADS1 autonomous development system for use in the design of M6800 microcomputer applications. It provides low cost, keyboard-to-CRT data input and display capability; options offered by Motorola Semiconductor Products Inc, Box 20912, Phoenix, AZ 85036 permit easy expansion into an economical development system. Any terminal with an RS-232-C or 20-mA current loop port can interface to the system. In the M68ADW1 system, a user supplied TV set replaces the CRT monitor included in ADS.

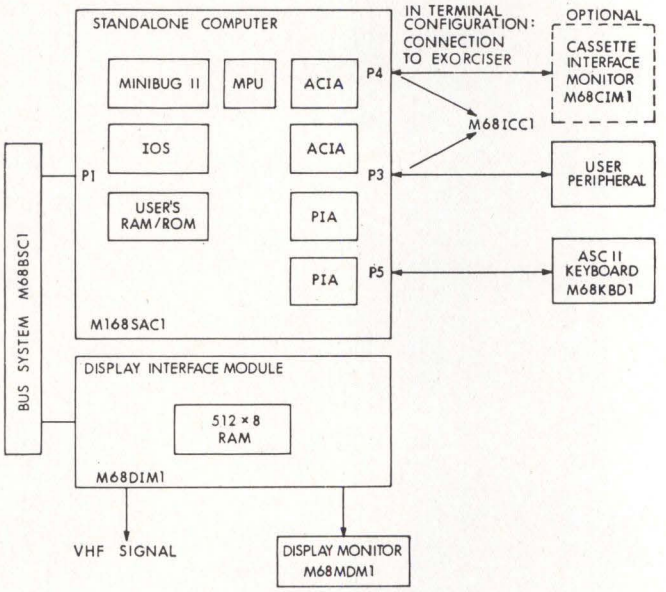
Two basic PDS modules, M68SAC1 and M68DIM1, combine to make up a system that allows the user not only to check out and execute a target program (debugging), but also to efficiently communicate with the machine (terminal capability). Debugging is derived from the MINIBUG II monitor functions stored in a 1k-byte ROM, while terminal capability is centered around I/O supervising firmware (IOS) which monitors data exchanged between the user's or MINIBUG program and ADS peripherals (CRT, keyboard, printer, audio recorder). The different approach of this system when compared to other development stations is that the teletypewriter is replaced by its equivalent peripherals.

There are four subsystems: debug section, I/O supervision section, user's section with 256 bytes of RAM and 2k bytes of AROM, and display interface section which handles ASCII character display. Debug consists of the microprocessor, 128 bytes of RAM, ROM, and ACIA through which data are transferred to or from the monitor. Based on IOS firmware, the I/O section monitors the data exchanged between the ACIA and system peripherals. Half of a PIA interfaces this section to a parallel printer, another half to an ASCII keyboard, and a third side conveys signals used to control DMA logic.

With these features a user can begin developing small programs to be fed and executed in the RAM area. Additional memory or I/O adapters are available by adding bus compatible plug-in modules.

System components are two peripheral devices [ASCII keyboard and 5" (12.5-cm) display monitor], bus system card and cable set as interconnections, and the -SAC1 standalone computer and -DIM1 display interface modules. The computer PC board operates with dynamic or static memories. The alphanumeric interface to the CRT monitor includes a 1-page memory, ASCII character generator, and video signal generator.

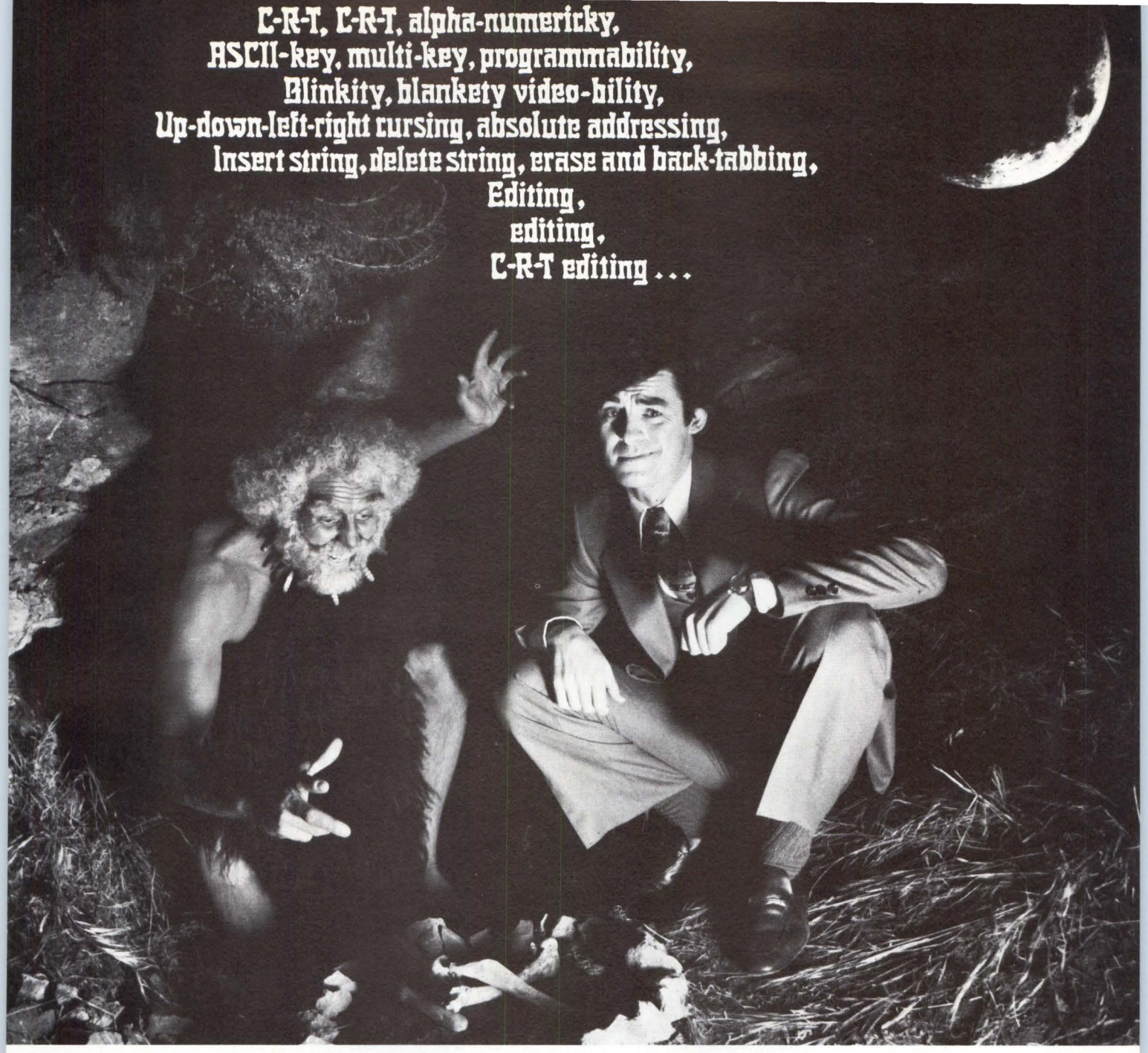
Options for expansion into a system for hardware and software development include a cassette interface module, editor/assembler module with editor program in ROM, and 5- and 10-card cages. A single audio cassette recorder is used with the editor/assembler module. Features of IOS and MINIBUG II are scroll control over DIM module, video invert and erase screen commands, cassette load and dump, cursor control, examine and change memory, and memory test.
Circle 433 on Inquiry Card



Motorola's development system components include standalone computer and display interface module which provide hardware/software debugging capabilities and communications between user and microcomputer. Separate elements of keyboard, cassette, CRT, and printer substitute for teletypewriter

Multiple Microcomputer System Performs Multiterminal Functions

Micral CM consists of a data file management microcomputer and up to four independent microcomputer stations, each with its own processor, I/O bus, serial I/O channel, and local memory. R2E of America, 3406 University Ave, SE, Minneapolis, MN 55414 says the system is particularly suited to applications where data acquisition, computing, and editing



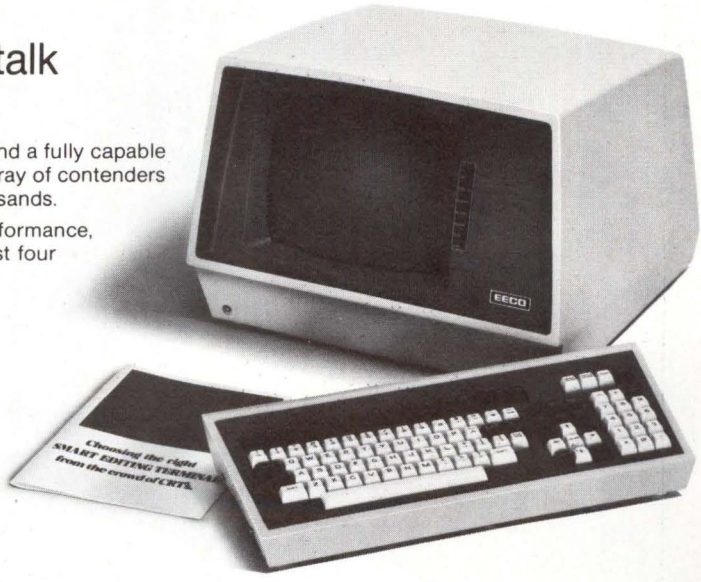
No bones about it.

What you need now is some straight talk about Smart Editing CRT Terminals.

Selecting the right CRT for your system isn't easy. You're trying to find a fully capable Editing Terminal in a CRT marketplace that's crowded with a dizzying array of contenders at prices ranging all the way from a few hundred dollars to several thousands.

You'll be glad to know that for $1500 or less, you can buy all the performance, reliability and support you need in a Smart Editing Terminal from at least four manufacturers — ADDS, Beehive, LSI, and EECO, of course. That's the conclusion of a comprehensive, straightforward report that frankly compares your alternatives model by model, spec for spec.

Get it straight — write for your free copy of "Choosing the right Smart Editing Terminal from the crowd of CRT's" today.



EECO editor

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Alumax® Mic-6 cast aluminum plate. All it needs are your finishing touches.

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See your nearby Alumax distributor. Or write for the Mic-6 brochure that gives you complete information and specs.

Mic-6 cast aluminum plate from Alumax. We started it, you finish it.

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CIRCLE 88 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS AND SYSTEMS

can be divided into several tasks, with one microcomputer per task. Tasks are linked by parameters passed through common memory; each microcomputer can have an application program running in local memory, with common subroutines and data available in shared memory.

Hardware consists of one 8080 based data management microcomputer with 16k of RAM, and up to four microcomputer stations with CPU, 4k local RAM, and serial communications channel. System resources include 48k of shared memory (expandable to 60k), CRT display and keyboard, two double-density minifloppy drives (double-sided recording optional), Centronics parallel printer interface, and a 10M-byte cartridge mass storage unit. Mass storage can be expanded in 10M- or 20M-byte increments to 80M bytes.

Standard system software includes a monitor and realtime executive; macroassembler; business applications oriented BASIC, with sequential, indexed sequential, and random-access file system; and utilities. Optional software includes an ANSI FORTRAN IV compiler with editor, formatter, and scientific subroutines.

End user price, including one data file management microcomputer, one microcomputer station, and optional CRT/keyboard, is $21,250. Introductory 50-unit OEM price is $17,000. Delivery is 60 days ARO.
Circle 434 on Inquiry Card

Intelligent Minifloppy Enhances Personal Computer Performance

Disk II, the newest peripheral for the Apple II personal computer system,

Disk II software provides dynamic disc space allocation. User need not be concerned with size or location of file on disc. Operating system also allows compatibility with existing languages via standard BASIC commands

consists of an intelligent interface card and either one or two minifloppy drives. The computer will handle up to 7 controller cards and 14 drives for instant access to more than 1.6M bytes of data, according to Apple Computer, Inc, 10260 Bandley Dr, Cupertino, CA 95014.

A bootstrap loader in ROM and an operating system in RAM combine to provide full disc capability for systems with as little as 16k bytes of RAM. Other features of the subsystem include ability to load and store files by name; random and sequential access; automatically generated filename directories; 116k bytes of storage capacity/diskette; patented design which reduces motor wear and power consumption while permitting higher speed operation of drive mechanics; and ability to be driven by the computer's power supply.

A soft-sectored format to store information on the diskette provides the 116k-byte storage capacity. The format calls for 35 circular tracks, each containing 13 sectors of 256 bytes. Data transfer rate is 156k bits/s. Average track access time is 200 ms, maximum 600 ms. Disc rotates at 300 r/min. Disc latency, or time required to move the disc one-half a revolution, is 100 ms. Price of the unit, including controller card, cable, and drive, is $495.
Circle 435 on Inquiry Card

Functioning of μComputer System Is Supported by Development Package

All hardware and software tools necessary for design, hardware/software integration, and debugging of PCS 8080A and Z80A based microcomputer systems are contained in the 3800B SuperPac Development System II. Housed in a desk unit, the system includes a dual floppy disc subsystem with 32k bytes of RAM, EPROM programmer, line printer, and CRT terminal. All required interfaces are supplied.

Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176 has developed extensive software to accompany the system. The package includes 8080A and Z80 absolute macroassemblers, BASIC, FORTRAN, relocatable macroassembler, linking loader, debug, line editor, cross reference generator, 3800B and floppy operating systems, up/down loader, and EPROM programmer.

SPDOS II is a device independent, software system providing keyboard console control. Two functional sections are the Executive and Drivers. Users can gain access to, control, and effectively use all software package modules through the Executive. The driver section contains all peripheral driver modules which control and process all I/O operations.

A reduction in the level of effort and time involved in software development, debug, and documentation is achieved with both absolute macroassemblers. The 2-pass assemblers translate 8080A and Z80A assembly language instructions into machine language operation codes.

When writing microcomputer software, the 2-pass relocatable macroassembler produces relocatable hexadecimal object code. The user can also break large programs into small segments. Other features are conditional assembly and full macro capability.

Other software components allow the user to link separately assembled

MICRO DATA STACK
COMPUTERS AND SYSTEMS

programs, subprograms, and subroutines into one operational program; to modify/change existing source programs and create new source programs; and to generate a list of all program symbols which serve as a quick reference table. To further reduce development time, the software tools allow the user to control and manage the dual floppy disc (the mass storage device); and load, debug, modify, test, and document application target system software from the console or target SuperPac 180 system console. With the interpreter and compiler, the user can write BASIC and FORTRAN language programs, respectively.
Circle 436 on Inquiry Card

Peripherals Option Card Extends Capabilities Of Pascal Machines

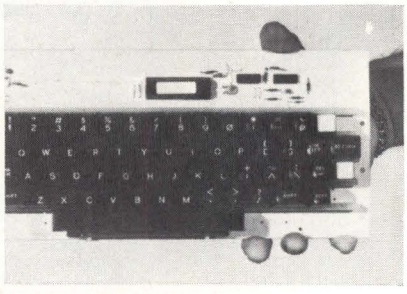
Continual expansion of options for the 8085A CPU based microcomputer systems is possible with the 85/EX peripherals option card. Northwest Microcomputer Systems, 121 E Eleventh, Eugene, OR 97401 offers as add-on features an arithmetic processing unit ($422 for the 3-MHz version, $272 for the 2-MHz version), an interrupt controller ($90), interval timer ($50), parallel I/O interface ($90), and serial I/O interface ($70). The required peripherals option card for these items retails for $158.

An arithmetic processing unit (AMD9511) provides 32-bit, fixed and floating point arithmetic, and floating point trigonometric operations to enhance the mathematical capability and performance of the company's 85/P. Featuring the Intel 8259, an interrupt controller resolves priority among eight different interrupt levels according to software algorithms provided by the user. Interval timer capability is obtained from Intel's 8253 programmable interval timer. Each timer has three user programmable 16-bit BCD or binary counters.

The parallel I/O interface uses the Intel 8255A programmable peripheral interface device to provide 24 signal lines for transfer and control of data to or from peripherals. The serial I/O interface, using Intel's 8251 USART device, can be coupled with the parallel interface option and interval timer to give complete RS-232 serial data communications including IBM Bi-Sync. It operates with most serial data transmission protocols.
Circle 437 on Inquiry Card

Features of Encoded Keyboard Are Aimed at Small Microcomputers

The MAX keyboard with features and options for personal computing uses has been introduced by Maxi-Switch Co, 9697 E River Rd, Minneapolis, MN 55433. It is MOS/LSI encoded with all 128 ASCII characters, and includes individual function keys to avoid the need for multiple key closures. Single quantity price is $69.95. A $3.95 kit allows HOME and CURSOR keys to be added.



Circle 438 on Inquiry Card

FUJITSU: KEYBOARDS & KEYSWITCHES

Every day brings about a new computer or new use for keyboards. Naturally, the larger the demand, the larger the number of companies trying to meet that demand. Choosing the right supplier for your keyboard needs can be a hit or miss proposition. Unless you choose Fujitsu.

Our reliability is known and trusted throughout the world, because Fujitsu doesn't depend on what someone else thinks is good enough. We manufacture every part of our keyswitches and keyboards. From key tops to contacts to the keyboard system. That makes for tight quality control every step of the way. And that makes for a more reliable keyboard.

Fujitsu reliability also comes from experience. Fujitsu computers are in use worldwide. We know our keyboards will work for you because they work for us. Automated production insures a standardized product. Fujitsu insures that it's dependable.

As far as service, Fujitsu considers it a point of pride, as well as good business, to cater to your company's needs before, during and after the sale. We custom build to fit your design needs for layout, keying, coding and slant. Our warehouse is stocked to supply your company with samples. Large orders come directly from the factory. And Fujitsu can match any source's lead time for processing and shipping.

Fujitsu keyswitches and keyboards are available in mechanical, reed, hall effect and capacitant modes. Our flat, low-profile keyboards give valuable tactile and audio response to touch that most membrane type keyboards don't.

Considering everything we have to offer, Fujitsu could just be the key to your keyboard needs. Quality, reliability and service are part of our product.

For more information on our superior components, call or write us.

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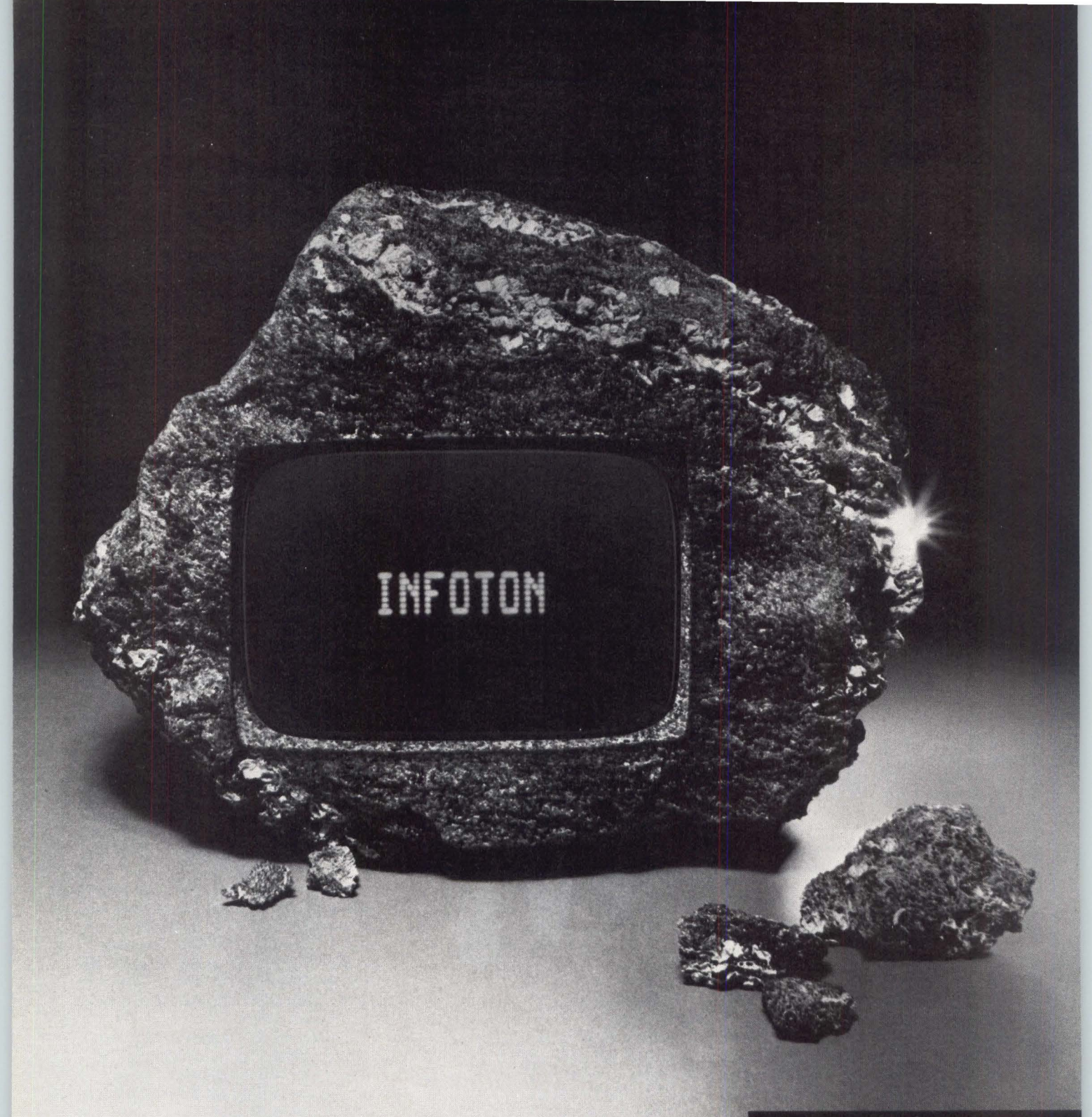
AND RELAYS AND CONNECTORS AND

CIRCLE 91 ON INQUIRY CARD



When we promise you impeccable reliability in our Infoton 400 Data Display Terminal, we assume you want our promise cast in stone.

No problem. After all, the Infoton 400 is Z-80 microprocessor based, with editing and formating capabilities. So it's not hard to understand why the I-400 is by far the most versatile terminal you can pick up for the price.

As for options, we include two additional pages of memory, a directly addressable printer interface, as well as polling capabilities.

INFOTON 400

For more solid information about reliability, versatility and pricing, call Infoton toll-free at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth at Infoton, Second Avenue, Burlington, MA 01803. In Canada, contact Lanpar Limited, 85 Torbay Road, Markham, Ontario L3R 1G7. (416) 495-9123.

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CIRCLE 150 ON INQUIRY CARD

The QM-1 Also Known As The Emulator

The "computerhunt" for a single machine that can service a wide range of needs in a development laboratory ends with Nanodata's QM-1, The Emulator. The QM-1 can assume the identity of any computer, becoming exactly like the emulated machine down to the most minute detail.

Software developed on the QM-1 will run unchanged on the emulated machine and vice versa. What is more, the QM-1 can change identities as often as the user chooses.

Challenges that the QM-1 has met include digital design verification, critical software validation and hardware/software trade-off analysis. Whatever the specific computer requirements — general purpose, avionic, military, minis, imbedded micros or HOL machines — the QM-1 can satisfy them.

A typical QM-1 configuration costs approximately $300K. A cost-effective investment considering that emulators on the QM-1 have been benchmarked at speeds 35 to 100 times faster than simulators on multi-million dollar systems.

Talk to Mike Senft, Marketing Director, about specifics.

NANODATA CORPORATION

2457 Wehrle Drive, Williamsville, New York 14221
Telephone (716) 631-5880

CIRCLE 92 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS AND SYSTEMS

Mag Tape Controller Is Software and Diagnostic Compatible With LSI-11s

A magnetic tape controller, featuring emulation of Digital Equipment Corp's TM-11/TU-10 reel-to-reel mag tape systems along with software and diagnostic compatibility for all industry standard TU-10 equivalent tape drives is a direct plug-in to DEC's LSI-11 (quad) and -11/2 (dual) backplanes. The dual-slot size module TO-3 requires only a company interconnect cable to operate with the selected tape drive. Interface with NRZI industry standard 7- or 9-track tape systems is obtained with the controller's DEC approved circuit drivers and receivers.

Manufactured by Dynus Inc, 3190K Airport Loop Dr, Costa Mesa, CA 92626, the controller also incorporates a bipolar microprocessor. The required 5 Vdc at 3.5 A is supplied through the backplane and is equivalent to less than one bus load.
Circle 439 on Inquiry Card

Auto-Answer Auto-Dial Modem Performs LSI-11 Communications Functions

As a low speed modem for the Digital Equipment Corp LSI-11, -11/2, and PDP-11/03 computer families, the dual-width board provides computer controlled answering and origination of data communication functions when used with TELCO CBS type DAA unit. Baud rates of 110, 134.5, 300, and 600, and number of data bits and parity are software selectable. Emulating a DEC DLV-11E serial interface, the modem from Nortek Inc, 2432 NW Johnson St, Portland, OR 97210 is software transparent to the RT-11 V3 and TSX operating systems, when used in auto-answer mode.
Circle 440 on Inquiry Card

4-Channel DAC Provides Low Cost Interfacing for EXORciser Systems

Interfacing the Motorola M6800 EXORciser microcomputer system, the ST-6800DA4A 4-channel DAC plug-in PC board with dc-dc converter and diagnostic test program is organized as a 16-byte memory block. Electrically and mechanically compatible with the EXORciser bus, the board slides into the microcomputer's card slots.

Features are 12-bit binary resolution, 4-μs settling time, $\pm$½ LSB nonlinearity, and full-scale output voltages of 0 to 5, 0 to 10, -5 to 5, and -10 to 10 V. Input coding is straight binary (unipolar) and offset binary or 2's complement (bipolar). Other specifications incorporated by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 include low output impedance of 50 mΩ, $\pm$20-ppm/°C gain temperature drift, $\pm$10-ppm/°C offset drift, $\pm$5-ppm/°C zero drift, and 1.2-A current drain at 5 V.
Circle 441 on Inquiry Card

Add-In Memories for LSI-11s Provide up to 32k x 18 in One Slot

Two add-in expansion memories, hardware and software compatible with Digital Equipment Corp's LSI-11 and -11/2 computer systems have been introduced by Monolithic Systems Corp, 14 Inverness Dr E, Englewood, CO 80110. The 4504, designed around a 4096 x 1 NMOS dynamic RAM, provides up to 8k x 18. It is available in 4k or 8k x 16 or 18 configurations. The 4604 has up to 32k x 18 in one option slot. It is designed around a 16,384 x 1 NMOS dynamic RAM, and is available in 16k, 24k, 28k, or 32k x 16 or 18 configurations. An additional 3k of memory is possible by utilizing I/O page for main memory.

Both offer access times of 290 ns for DATI and DATO (B) and 850 ns for DATIO (B). Switch selectable refresh modes for external and internally distributed refresh are included, as is switch selectable addressing on any 1k boundary from 0 to 128k.
Circle 442 on Inquiry Card

BASIC and 1M Bytes Of Storage Highlight Desktop Computer System

Featuring a built-in CRT with a 1920-character display, the IMPAK M-1 is based on a 3-MHz 8085 processor. Two double-density floppy disc drives provide an initial storage of 1M bytes; three optional double-density dual-disc drives allow external storage to 4M bytes.

IMEX Computers, a div of International Materials, 54 Middlesex Tpk, Bedford, MA 01730 offers a BASIC software package with the system for commercial applications, or an optional FORTRAN IV package for scientific and engineering environments. Support software includes utilities; a disc operating system with text editor, job, file, and storage management facilities; and debug and diagnostics.
Circle 443 on Inquiry Card

Disc Architecture Provides Microcomputer With High Throughput

Packaged in a 42" (107-cm) equipment rack, the C3-B has a minimal configuration with 48k of static RAM; the company's triple processor CPU board with 6502A, 6800, and Z80 microprocessors; dual floppy disc drives for program and data mobility, and a 74M-byte Winchester technology fixed disc. The disc communicates with the CPU via a dedicated high speed memory channel which services a dual port memory. Thus, high performance disc operation is achieved without degradation of processor speed or use of interrupts.

Ohio Scientific, 1333S Chillicothe Rd, Aurora, OH 44202 has allowed for expansion by designing a 16-slot case in which only seven slots are used in the $11,090 base system. An OS-65U disc operating system with Extended BASIC is included with the computer.
Circle 444 on Inquiry Card

µComputer Interface Combines Text/Graphic Video Display

Functions of text display, graphic display (320 H x 200 V resolution with the Super Dense option), keyboard input port, and 4k bytes of onboard control ROM make up the MERLIN video interface, available assembled or in kit form. As an intelligent console I/O device for a small system, the unit displays 20 lines of text with 40 char/lines, upper and lower case.

As a medium resolution graphic display for graphic development and end user systems, the interface has a standard resolution of 160 H x 100 V, true bit mapped graphics. MiniTerm Associates, Inc, Dundee Pk, Andover, MA 01810 has developed the ROM firmware to provide a keyboard driver with edit key decoding, display output, monitor functions, cursor/edit functions, graphics subroutines, and a keyboard graphic drawing mode.
Circle 445 on Inquiry Card

A Workhorse That's A Winner . . . At 1250 LPM

Model 5321 is an off-the-shelf drum printer, already engineered for your tough jobs. Jobs that demand heavy-duty print cycles, long hours of reliable operation and consistent print quality — at high speed! This is a full-size printer for mainframe-size jobs.

Years of dependable service in countless installations have earned it a reputation as "the workhorse of the computer industry." The MDS 5321 is no slouch. It can produce human-readable or machine-readable hard copy, on a wide 160-column print line, 1-up, 2-up, 3-up or 4-up, at speeds to 1250 lines per minute*.

A variety of type fonts is readily available. Gothic style, IBM-compatible, ECMA, OCR, and CMC 7 or E13B MICR fonts — so important in financial applications where secure check imprinting is involved.

The 5321 is completely buffered. A full line of print data with its associated formatting instructions is stored in memory while the previous line is still being printed. This means maximum throughput and no missed dates for your production schedule — no overruns on your print budget!

*Using standard 48 contiguous characters. 64, 96 and 112 character sets optionally available.

Consider the outstanding features of MDS 5321:

- High-speed paper slewing to 75 ips
- Additional tractor pins to minimize tearing of form holes
- Low-inertia servo motors to considerably reduce maintenance requirements
- Quick-loading VFU mechanism designed for extended form-loop life
- Failure-proof sensing switches for No Paper or Paper Low conditions
- Advanced ribbon mechanism to assure maximum usage of entire spool
- Optional extended interface for additional status monitoring.

The 8-bit interface is already in place. The next move is yours. Whether you're in the OEM business or a systems house specializing in custom applications, it will pay you to look into the MDS 5321. Quantity discounts available. Send coupon today for a detailed Fact Sheet. Or call collect, H. Johnson at (315) 866-5300 or J. Engstrom at (714) 772-0803.

MDS

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CD978

CIRCLE 93 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS AND SYSTEMS

Low Cost Prototyping Boards Aid Series/80 Microcomputer Design

Two prototyping boards, form and size compatible with Intel SBC-80/10 and -80/20 or National BLC-80/10, -80/11, -80/12, and -80/14 microcomputer boards, have five double-sided card edge connectors for bus oriented parallel or serial I/O. Available from Vector Electronics Co, Inc, 12460 Gladstone Ave, Sylmar, CA 91342, the 12 x 6.75 x 0.042" (30.48 x 17.15 x 0.107-cm) boards are prepunched with 0.042" (0.107-cm) diameter holes on 0.1" (0.25-cm) grids. They accommodate DIPS with 0.3, 0.4, 0.6, and 1.9" (0.76-, 1.02-, 1.5-, and 2.3-cm) lead spacing, as well as such components as solid-state or electromechanical relays and thumbwheel switches.

Model 4608 has heavy duty power and ground buses. It holds up to 54 16-pin DIPS in the patterned area and has a 13-in^2 (84-cm^2) unclad area for free component placement. Soldering DIPS and interconnections or easy solder mounting of wrap-post DIP sockets is possible. Model 4608-1, identical to 4608, has no etched pattern. With continuous array of 0.042" (0.107-cm) diameter holes on a 0.1" (0.25-cm) grid, it holds up to 144 16-pin DIPS.

Circle 446 on Inquiry Card

SOFTWARE

Microcomputer Language Permits Use of Structured Programming

Written in 6800 assembly language, a 3-pass compiler provides a disc based high level language for microcomputers with at least 16k of RAM. Versions are available for ICOM FDOS-II, Smoke Signal Broadcasting DOS68, and SWTPC Flex STRUBAL (STRUCtured BASIC Language) has been developed by Hemenway Associates, Inc, 151 Tremont St, Suite 8P, Boston, MA 02111, with features of fully relocatable and linkable code.

Software supports a full set of scientific functions, 1- and 2-dimensional arrays, three data types, structured programming forms, string functions, and embedded assembly language in the source program. Line numbers are unnecessary in source programs. Subroutines may be compiled or assembled separately and are called by named parameters. Price of $99.95 covers the compiler (including runtime package) provided on floppy disc, together with user manual.

Circle 447 on Inquiry Card

Programming Languages Are Designed Specifically for uComputer Systems

MCZ-1 series microcomputers are now supported with COBOL and an extended BASIC interpreter for highly interactive environments; the latter also supports the ZDS-1/40 and -1/25 development systems. The company's version of the 1974 ANSI X3.23 COBOL, incorporating many Level 2 features, is designed to allow relatively large programs in a small machine.

According to Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014, users of the microcomputer systems can compile and execute standard COBOL programs with performance and characteristics that equal or exceed COBOL minicomputer performance. Features include such extended CRT control features as accept and display; a debug structure for interactive program development; sequential or indexed file access; random files; program segmentation; library; interprogram communication; and 18-digit decimal and binary data types. Running on 48k-byte systems, the language uses the ZDOSII and runs under the standard RIO operating system.

With an optimum blend of speed and precision, the BASIC interpreter subsystem allows programs to be interactively entered, edited, run, and debugged. Real, integer, and string data can be manipulated with full file capabilities, including both string and record random access. Binary and BCD data math packages are included. The interpreter interfaces with the RIO system; programs can interface with PLZ or assembly language procedures, and can be chained to other BASIC programs.

Circle 448 on Inquiry Card

High Level Interpreter Advances Debugging Capabilities of SLAM

A second generation interpreter for the BASIC-like SLAM offers a system well adapted to resident high level programming on 8080/8085 systems, while including such capabilities as direct keyboard I/O examination, automatic breakpoint insertion, symbolic program variables listing, and direct memory display or modification. The SLAM Debugging Interpreter with all programming creation, running, and debugging facilities occupies about 5k of RAM. Standard versions are available for Intel's MDS-800, Intellec 8/Mod 80, SBC-80 board series, and National's BLC-80/10; special versions for other 8080/8085 based systems may be ordered.

Facilities to speed and ease program development have been incorporated in the interpreter by Penn-Micro, PO Box 5073, Lancaster, PA 17604. Listings may be in decimal, hexadecimal, or binary; all operations including I/O may be either 8 or 16 bits in length. A facility to translate hexadecimal or decimal numbers to hexadecimal, decimal, or binary is also included.

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8080 Program Converts English To Drive Speech Synthesizers

Hand coding of phonetic messages for speech synthesizers is eliminated by ANGLOPHONE, an 8080 program which transforms English in real time into phonetic codes. Large data bases are ready immediately for speech output.

Required hardware is an 8080 CPU, 8k bytes of memory, and a speech synthesizer. UPPER CASE books, 502 E John St, Champaign, IL 61820 has designed the program to be patched easily into any higher level programming language. Talking terminal software is available to convert an 8080 based intelligent terminal into a talking terminal for use on any computer system.

Circle 450 on Inquiry Card

Small But Comprehensive Realtime Executive Operates on LSI-11s

Applications can be developed quickly and efficiently without the user having to write a special optimized software executive, with the introduction by Scientific Systems Services, Inc, 1135 John Rodes Blvd, PO Box 610, Melbourne, FL 32901 of the 3sx-11 realtime executive program. The comprehensive, though small, realtime operating system for the LSI-11 features CRT handlers, TTY handlers, floppy disc support, I/O queuing, and intertask communications linkage. It is furnished with software documentation and a user's manual. □

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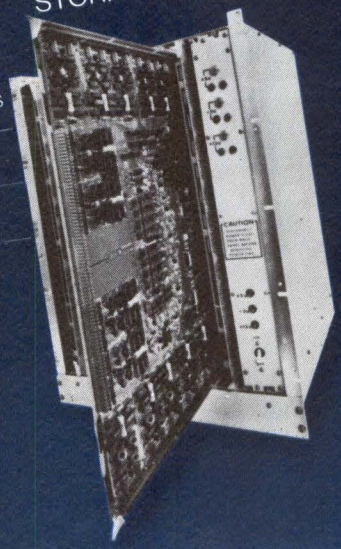
- SOLID STATE RELIABILITY



Here's the best alternative to fixed-head disk for cost-conscious users of PDP-11 & Nova computers.

- High speed random access.
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- 1.5 microseconds access time.
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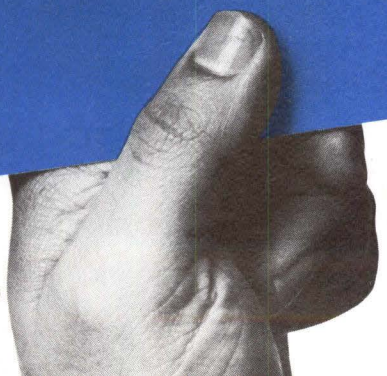
- No moving parts. Low maintenance.

The MaxiRAM System is also available for use with other computer types.



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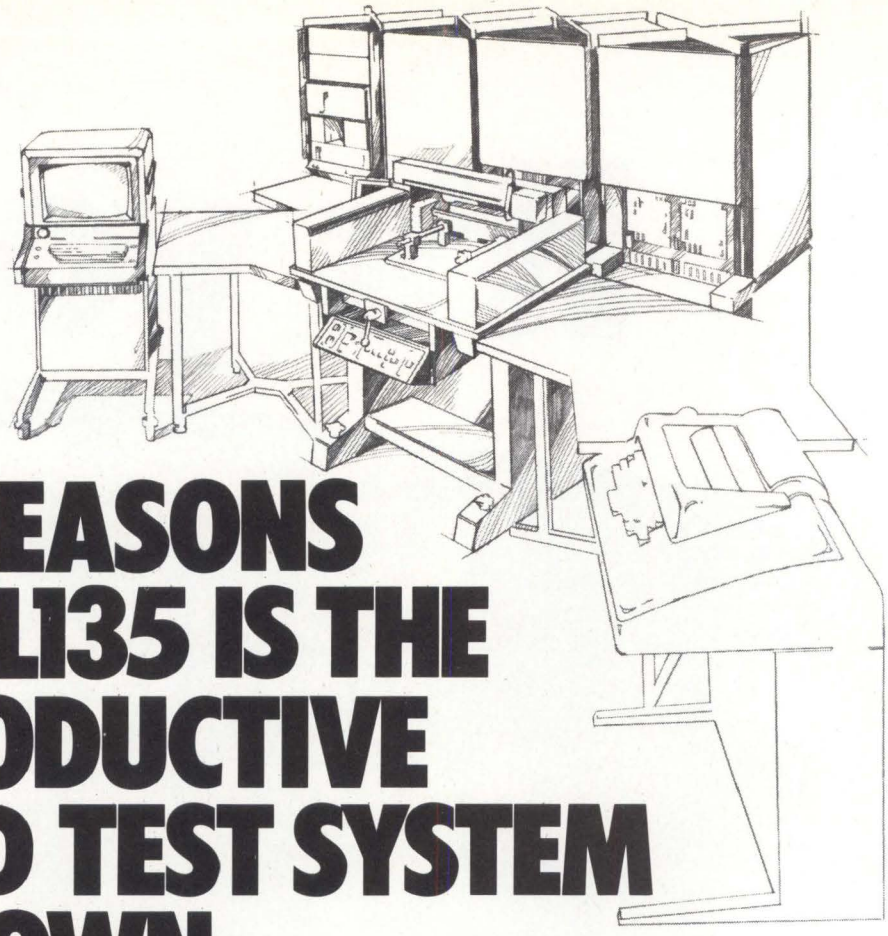

TWELVE REASONS WHY THE L135 IS THE MOST PRODUCTIVE LSI BOARD TEST SYSTEM YOU CAN OWN.

To compare productivity in LSI board testers, take their three common operations: diagnosing, testing, and programming. Now, to each operation apply the basic measures of productivity: cost, throughput, and quality of testing.

The L135 has the highest diagnostic throughput, the lowest operating cost. No other test system comes even close.

1. The L135 finds bad LSI devices on long buses.

The Electronic Knife does it. It takes just a few more probes after regular guided probing finds the failing bus. Without the Electronic Knife, you're faced with trial and error replacement of LSI chips. Or skilled technicians tying up the system for an hour or more per bad IC.

2. The L135 makes fewer diagnostic probes – by an order of magnitude.

State-sensitive trace does it. Most LSI boards are loaded with multi-input LSI chips linked through "wired-and" bidirectional buses. These often require hundreds of diagnostic probes per fault. State-sensitive trace cuts the number dramatically.

3. The L135 produces immediate probe commands.

The on-line circuit model with a large random-access memory does it. With circuit structure immediately accessible, the operator does not wait for commands between probes. Other test systems that use fault dictionaries often delay each command several seconds, adding minutes to each diagnosis.

4. The L135 mechanizes probing.

The M150 Automatic Prober does it. Seven to ten times faster than a human operator, the M150 speeds up board diagnosis even more because its operation is both error-free and fatigue-free.

The L135 delivers the highest quality of testing, thereby slashing costs for diagnosis later at systems test and service out in the field.

5. The L135 emulates LSI-board operating environments.

5-MHz clock-rate testing does it. To ensure adequate board quality, you usually have to run LSI boards at clock rates as the last step in testing. Only the L135 provides test rates of up to 5-MHz, the speed of many microprocessors seen in today's products.

6. The L135 emulates and tests CPU sets.

Multiple drive/compare phase control does it. During clock-rate testing, the test system must first replace the CPU set and then test it at speed. The associated microprocessors usually receive multi-phase inputs and generate multi-phase outputs. The L135 provides the necessary, easy-to-program, precise phase controls over driver inputs and comparator strobing.

7. The L135 tests and diagnoses analog circuits.

Integrated ac-dc-parametric capability does it. The L135 offers many analog force-and-measure functions through matrix connections, all completely integrated into system hardware and software. If these capabilities aren't integrated into the test system, they must often be added to accommodate the increasing analog content of LSI boards. That prolongs test time and slows diagnosis considerably.

8. The L135 tests at dc and clock-rate on the same channel.

All-speed pin compatibility does it. In clock-rate testing, high-speed tests are usually applied on the same pins tested earlier with dc. The L135 allows you to apply both types of tests at the same system channel, eliminating the need for awkward switching or extra channel capacity.

9. The L135 has enough clock-rate channel capacity for the big jobs.

444 I/O pins does it. Big LSI boards have upwards of 250 edge-connector pins, all active. In addition, you need simultaneous access to dozens of internal test points and devices invisible to the edge connector. The L135 offers the highest clock-rate channel capacity, enough for all foreseeable LSI boards.

10. The L135 cuts total programming time.

The P400 Automatic Test Generation System does it. The P400 automatically generates all the dc patterns and diagnostic data for the toughest part of most LSI boards: the jungle of random digital logic, as well as those portions containing modeled LSI devices. Total programming time is shorter. The best of the so-called "automated test generation" techniques offered by other systems still require manual pattern-writing. That takes longer and costs much more.

The L135 cuts the time needed to get products into the production line and out to the market place.

11. The L135 cuts system time for debugging.

Immediate-response debug software does it. During test-plan debugging, the L135 responds to the test engineer's commands and displays results immediately. Total debugging time is cut to a fraction because the test engineer is not distracted by system delays; he can concentrate on his circuit and his test plan.

12. The L135 readily assembles the many parts of LSI test plans.

Structure-merge programming does it. Test plans originate in many places: manual patterns and circuit models, learned data from known good boards, circuit and device simulators, automatic pattern generators, etc. The L135's structure-merge software and its straightforward protocol assembles them all into a coherent package, saving your engineers hours of tedious and costly work.

For more information on these and other L135 features, write Teradyne, Inc., 183 Essex Street, Boston, Massachusetts 02111.

TERADYNE

CIRCLE 95 ON INQUIRY CARD

CMOS ON SAPPHIRE

Scott Smith and Eric R. Garen

Integrated Computer Systems, Inc
Santa Monica, California

There are many in the semiconductor industry who believe that the most promising of all integrated circuit technologies is to be found in the fabrication of complementary metal-oxide semiconductor devices by means of the silicon-on-sapphire process. Nevertheless, this technology has been faced with some serious obstacles that are only now being resolved. Whether the solutions that have been developed are sufficient to bring the technology into its own as a strong contender against the leading n-channel metal-oxide semiconductor as well as integrated injection logic approaches remains to be seen.

The pairing of complementary metal oxide semiconductor (CMOS) and silicon-on-sapphire (SOS) technologies is a natural one, since SOS solves the primary speed-limitation problem of CMOS. CMOS is a circuit configuration in which complementary n and p type metal-oxide semiconductor field effect transistors (MOSFETs) are connected in series to act as a "push-pull" inverter. This structure can be viewed as a transistor having an active load—the complementary transistor—rather than the typical passive resistor load. In theory, this should result in shorter gate delays because the "load" actively assists in switching the current.

Low power consumption is the principal advantage of CMOS; when the circuits are not actually switching from one state to another, virtually no current flows (Fig 1). This is a result of the series complementary transistor arrangement. In the steady (nonswitching) state, one transistor is on and the other is off, so that no current flows through the pair. The only current is a miniscule flow between the on transistor and the gate of the next stage of circuitry. Since the gate of a MOSFET draws very little current, the entire CMOS circuit consumes very low power.

The main practical limitation on the speed of CMOS circuits is the parasitic capacitance of the aluminum conductors that interconnect the transistors. These conductors, separated by a layer of SiO_2 (glass) from the bulk silicon semiconductor substrate, restrict switching speeds by presenting a significant capacitive load for the very low current levels being switched.

SOS technology was evolved primarily to reduce parasitic capacitance—thereby significantly increasing the speed of CMOS while maintaining its low power benefits. The CMOS circuits are fabricated in a thin silicon layer grown on a sapphire substrate. Being a nonconductive material, the sapphire virtually eliminates the problem of capacitance between the aluminized conductors and the substrate. The choice of sapphire as the nonconductor stems from two properties: first, large sapphire crystals can be grown; second, and more important, its thermal coefficient of expansion is virtually identical

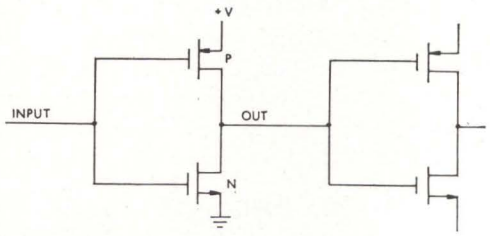

Fig 1 CMOS inverter. P-channel MOSFET conducts when input voltage is negative. N-channel MOSFET conducts when input is positive. Since only one of complementary transistors conducts at any time, no current flows from +V to ground. Only flow in steady state is along "out" lead to drive gate of next stage at very small level of current. Some power is dissipated during switching; as one device is turning on and other turning off, brief interval occurs during which both conduct

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Though it looks the same on the outside, today's Mini-Raycorder incorporates many improvements which make it even more reliable, easier to use and better performing than the original design. The Model 6409 Mini-Raycorder, which scored such a resounding success as the world's first tape recorder for ANSI proposed standard Mini-Data Cassettes, is now impossible to beat.

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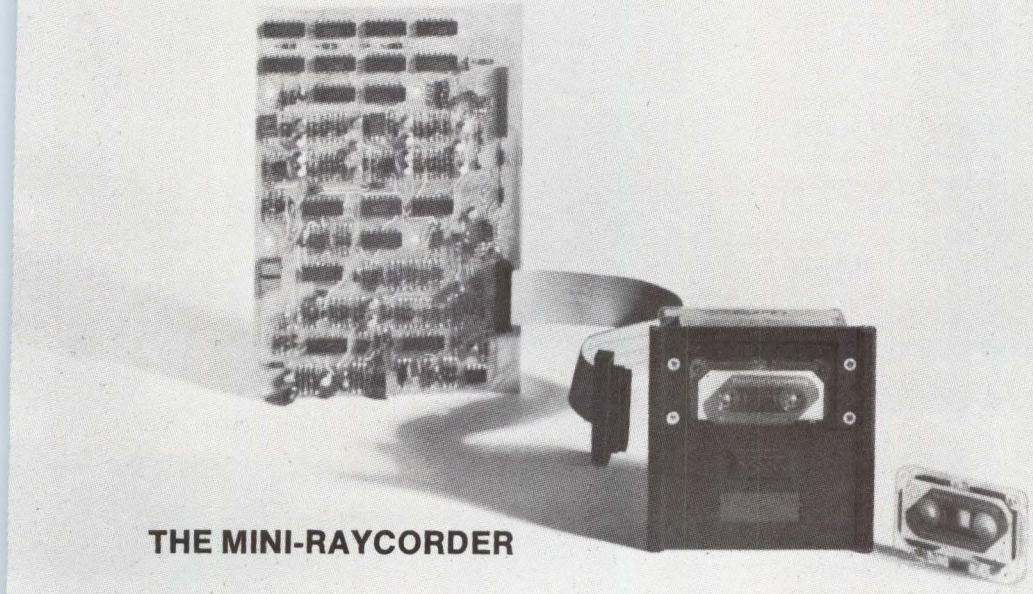


THE MINI-RAYCORDER

CIRCLE 96 ON INQUIRY CARD

Raycorder Products Division **RAYMOND ENGINEERING INC.**, 217 Smith Street, Middletown, Connecticut 06457
a subsidiary of Raymond Precision Industries

to that of silicon. If the thermal coefficients for the two materials were not matched, silicon circuits grown on sapphire would buckle and dislodge as the circuits heated.

Circuit capacitance is further reduced through elimination of the large horizontal junction structures used in other fabrication technologies. In SOS, these are replaced by vertical junctions, and junction capacitance is sharply diminished.

A side benefit is the elimination of a processing problem that, in other technologies, can cause chip failures. In SOS, as in the other technologies, the aluminum interconnects run on top of an insulating layer of SiO_2. With SOS, a pinhole in the SiO_2 layer is usually not catastrophic, because below the SiO_2 is the insulating sapphire; therefore, penetration does not result in a short circuit. In contrast, a pinhole in a non-SOS device could cause a short circuit between the conductor and the underlying silicon layer, leading to device failure.

SOS Fabrication Problems

Despite apparent advantages of SOS technology, many years of research and development efforts by many companies failed to produce significant results until last year, when Hewlett-Packard announced the development of a 16-bit single-chip microprocessor built with CMOS on sapphire. The primary obstacles have been (and are) materials and processing problems. First, significant problems are encountered in the effort to grow an epitaxial layer of silicon on a sapphire wafer; second, impurities on the surface of the sapphire present problems.

Many early attempts at SOS relied on a mesa structure (Fig 2). However, this led to difficulties in running aluminum interconnections up and down the mesas and especially across the right angle boundary of the silicon mesa and the sapphire. Other problems were encountered in bonding the metal directly to the sapphire.

Attempts to apply conventional silicon fabrication methods to SOS met still further difficulties. For example, silicon diffusion processes were found to crack the SOS wafers. This made it necessary to develop new processing methods. Because of these and other problems, one SOS effort after another resulted in failure.

In announcing its accomplishment with this technology, Hewlett-Packard attributed its success to step-by-step application of materials and process engineering. Emphasis was placed on techniques for growing sapphire crystals and concentrated efforts were made to eliminate impurities at the silicon-sapphire boundary. This elimination of impurities solved a series of problems, including that of transistor leakage. (Transistor leakage had caused difficulties for various manufacturers working in this technology; for example, RCA reportedly undertook a total encapsulation of SOS transistors to prevent leakage.) Standard silicon processes were re-engineered to adapt them to SOS; these included diffusion and ion implant processes.

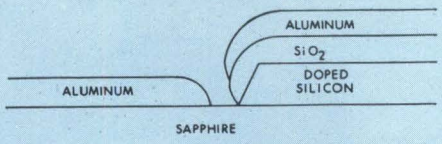
Finally, HP's SOS devices were developed along classical lines of semiconductor evolution, going from a mesa to a planar structure. This alleviated the metallization problems that arose in mesa geometries. Details on some of these innovations, as they apply to SOS fabrication procedures, are discussed in "One Solution to SOS Fabrication Problems."

Results and Future Projection for SOS

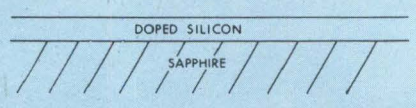
Hewlett-Packard's silicon-on-sapphire process is now being used to produce 16-bit single-chip microprocessors and related circuits. A chip occupies an area of

One Solution to SOS Fabrication Problems

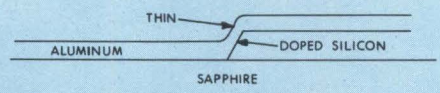
Problem 1: Fabricating conductors across a silicon dioxide-sapphire boundary



Solution: Grow a doped anisotropic crystal silicon structure on the entire wafer. This prevents any further processing interaction with the sapphire surface. The CMOS transistors will later be fabricated by altering the silicon crystal.



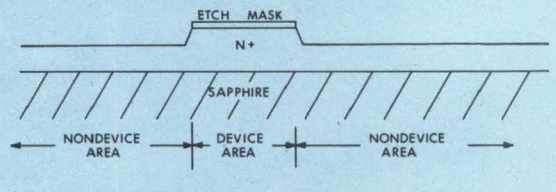
Problem 2: Metallization across uneven boundaries



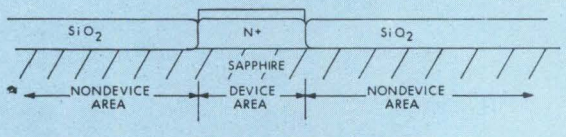
Solution: Where no devices are to exist, change the doped silicon to silicon dioxide of the same height. This is accomplished in two steps.

Starting with a layer of silicon anisotropically etch away at the nondevice areas in the silicon so that when those areas are oxidized to form silicon dioxide, the oxidation builds the etched-away nondevice areas to the same height as the device areas.

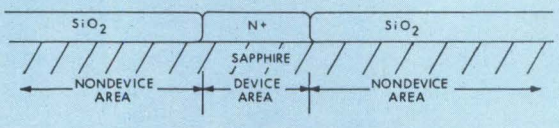
First step: Etch



Second step: Oxidize



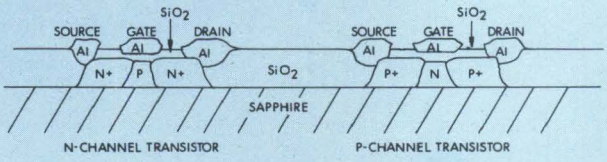
Result (after removing oxidation mask)



An added benefit is that the SiO_2 regions insulate the devices from each other.

Problem 3: Forming the npn and pnp regions in an existing doped silicon crystal

Solution: A battery of techniques were developed to diffuse impurities right down to the surface of the sapphire. These include boron ion implantation, heat diffusion from a heavily doped layer such as phosphorous doped oxide that is deposited on the surface of the doped silicon, and use of temporary masking agents such as Si_3N_4 that are later removed. The final structure is:



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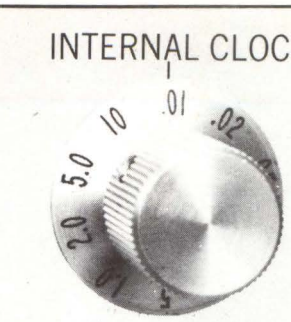
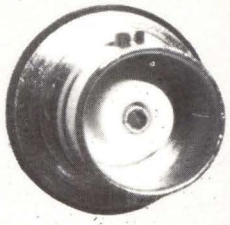
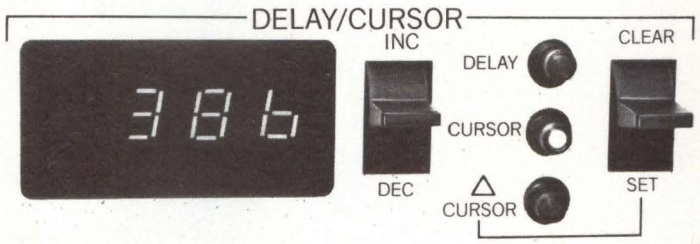


100 MHz speed
Dial in clock rate, from 100 Hz to 100 MHz.

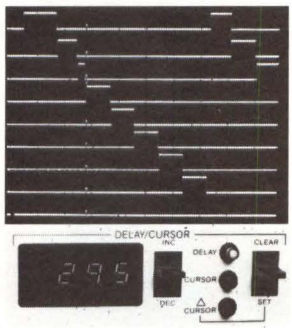


Nine channels
Ideal for debugging 8-bit-plus-parity systems.

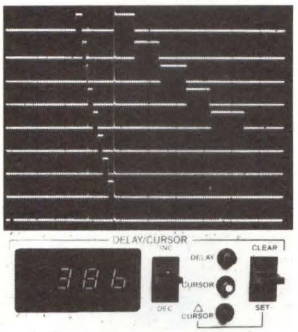


LED readout
For precise measurement of trigger delay, cursor position and time intervals.

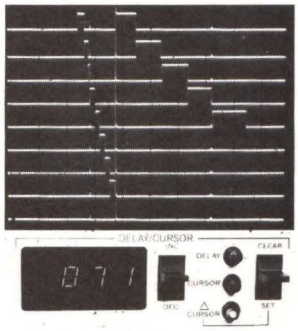
Qualifier selection
Control data recording with clock and trigger qualifiers.



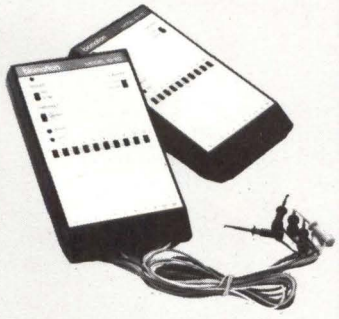
Trigger position
Marks trigger on CRT, LED readout shows trigger position.



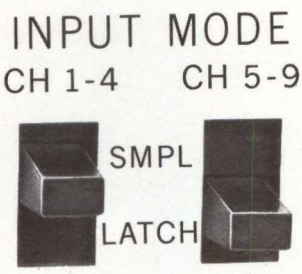
Expansion from movable cursor
Cursor position determines where expansion of display begins.



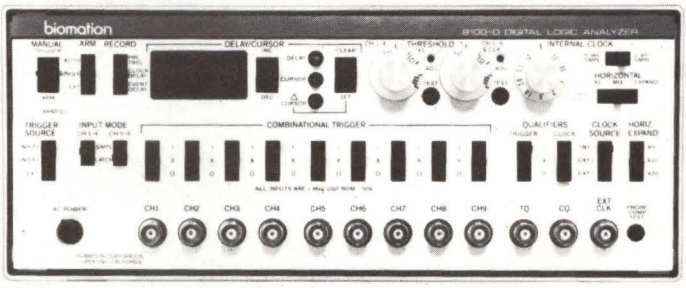
Precise time interval measurement
Readout indicates clock periods between selected cursor positions.



Trigger on 30-bit words
Optional 10-TC Probe Pods extend trigger word from 10-bit trigger.



Latch/sample selection
Catch glitches of 5ns or narrower, using Latch Mode.



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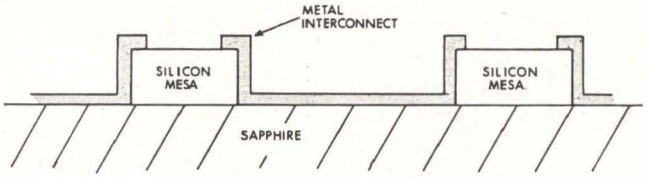


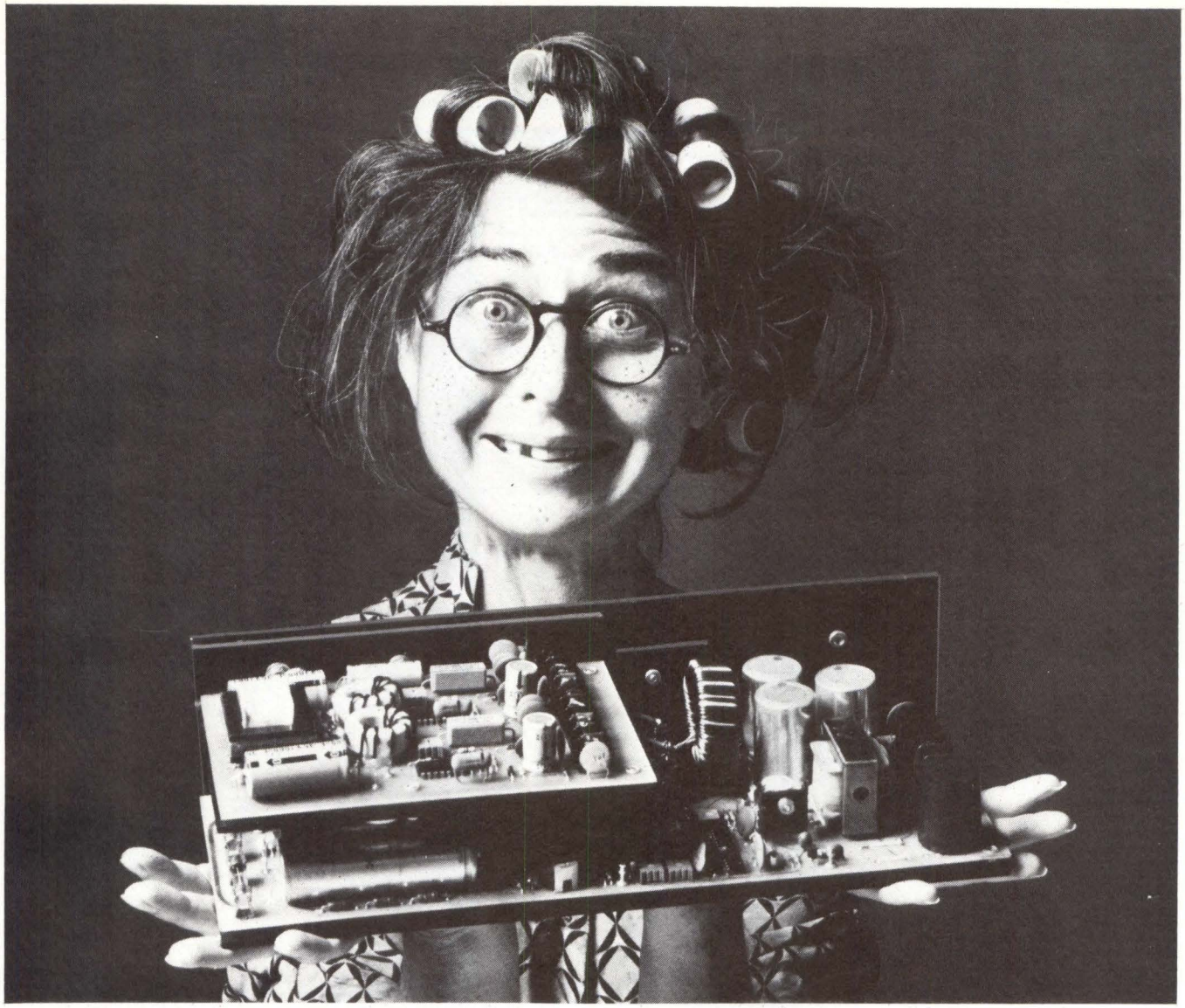
Fig 2 Early SOS configuration employed mesa structure. Difficulties arose in metal interconnect lines configured to right-angle geometry. Metal-sapphire bonding provided additional problems. Later development led from this to planar structure

approximately 50,000 mil², comparable to processors built with NMOS technology (eg, TI's 9900). These production devices contain up to 40,000 transistors, also comparable to MOS competitors. A density of 500 devices (approximately 150 gates)/mm² is typical of SOS random logic layouts, and this too is similar to NMOS densities. Thus, at the present time, device complexity of SOS and NMOS is roughly equivalent. Furthermore, future projections by proponents of both technologies indicate comparable device complexities in the future.

The speed-power product (the most typically used measure of performance) is quite good for NMOS—roughly 1.5 pJ. While better than that of conventional NMOS processes, it is similar to that achieved with HMOS processing (see *Computer Design*, Aug 1978, pp 160-162), which provides a reported speed-power product of 1.0 pJ.

Hewlett-Packard conservatively projects a reduction of the SOS speed-power product to 0.2 to 0.3 pJ by the early 1980s, while HMOS predictions are 0.2 pJ by 1980. Thus, it can be foreseen that the speeds of these two families will remain roughly equivalent in the near future. However, in the long range situation, it appears that SOS will yield superior speed, especially for pure random logic circuit configurations such as microprocessor CPU designs.

Perhaps the only major disadvantage of SOS is its relatively complex processing. Proponents claim that the processing is actually no more complex than others, only more recently developed. Therefore, it may take several years for the cost of this technology to decrease to levels competitive with NMOS circuits. In this light, we can expect SOS to actually begin competing with NMOS at the opening of the coming decade.



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Monolithic PMOS Speech Synthesizer Models Vocal Tract On Single Chip

Developed from a metal gate p-channel MOS process, the TMC 0280 monolithic integrated circuit electronically simulates human speech. The 44,000 mil² chip is combined with a pair of 128k dynamic ROMs (each able to store over 100 s of speech) and a special version of the TMS 1000 microcomputer to form a talking teaching aid, Speak & Spell™, a consumer product developed by Texas Instruments Inc, PO Box 5012, Dallas, TX 75222. The chip is not available separately at this time.

Initially, human speech was analyzed through use of linear predictive coding (LPC), a technique based on correlating consecutive digitized samples extracted from an analog speech input. The mathematical model resulting from this analysis was used to construct a time-varying digital filter as a model of the vocal tract. The filter logic was then implemented onchip.

Twelve parameters are built into the onchip logic: pitch, energy, and ten filter coefficients. Time-varying codes (representing a sequence of specific values for these 12 parameters) are stored in the ROMs. These codes serve as inputs to the synthesizer chip, providing updates every 25 ms. Pitch is specified as a periodic input to generate voiced sounds such as vowels or voiced fricatives (eg, Z, B, and D). The pitch parameter is set to zero to specify a white noise input to the digital filter in order to generate unvoiced sounds such as S, F, T, and SH. In either case, the changing coefficients filter the periodic or random input to produce speech sounds. Output of the digital filter drives a digital-to-analog converter, which in turn drives a speaker.

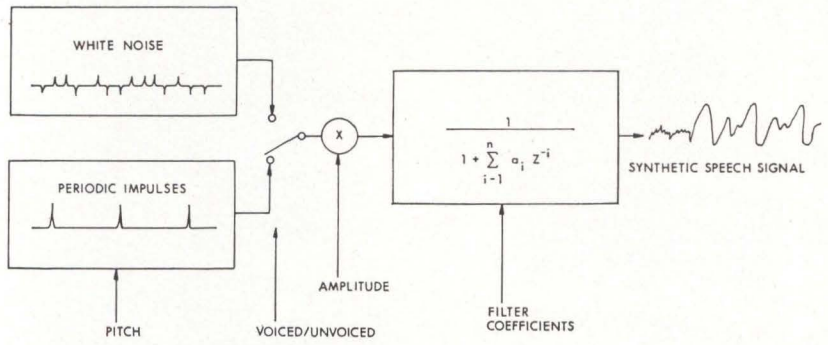
Speech updates from the offchip ROMs call for a frame rate of approximately 40 Hz. (Chip design allows a maximum frame rate of 50 Hz.) Within each frame, 48 data bits define all parameters. The data sampling rate is 10 kHz. Frequencies are provided by division of the output of an 800-kHz oscillator.

A 25-state binary parameter counter is used to provide a 2.5-ms parameter interpolation interval. Stages of the counter are used as controls for the interpolation and parameter loading process. A final 8-stage binary counter directs the interpolation sequence. During the last of these stages, new speech parameters are transferred from the ROMs.

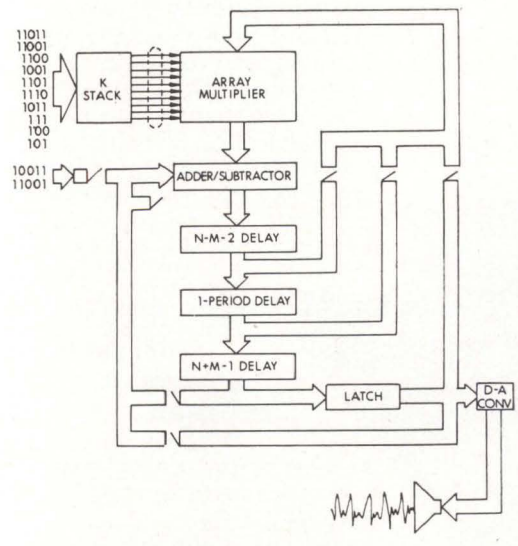
A 10-section digital filter performs 2's complement arithmetic with 10-bit time-varying reflection coefficients and 14-bit intermediate results. To combat the inherent negative drift due to truncation, a 1 is inserted as the least significant bit at the conclusion of each multiplication.

During each 100-μs sample period, the filter computes 20 values, 19 which involve a product and a sum. The values are calculated in a sequence that permits the multiply operations to overlap. An 8-state pipeline multiplier completes these overlapping multiplies at a rate of 1 every 5 μs. Inputs are provided by a recirculating register stack containing reflection coefficients and a multiplexer that selects calculated values and special inputs.

For voiced sounds, a 5-ms chirp is applied to the input at a time interval equal to the pitch period. The chirp is stored in digital form in a 50 x 8 ROM addressed by the pitch



Basic model of linear predictive coding for speech synthesis process. Periodic inputs consist of voiced sounds and white noise inputs for unvoiced sounds. Amplitude variable is applied to input, which is then processed through digital filter. Continually updated filter coefficients represent specific sound combinations. Output is synthesized speech



Block diagram of Texas Instruments' speech synthesizer chip. Human vocal tract has been electronically duplicated on single chip, reportedly for first time. Speech synthesis IC, two 128k ROMs that can store over 100 s of speech, and microcomputer serve as main electronics for talking, spelling learning aid

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period counter. Address inputs equal to zero or in excess of 50 produce a zero output. The pitch period counter is binary, incrementing once every 100 μs, and resetting itself to zero on the count following a true comparison of itself and the pitch register. A pitch value of zero is defined as unvoiced sound and causes the pitch counter to reset continually to zero. This produces a zero at the chirp ROM outputs. Special provisions are made to zero the pitch counter at a voicing transition (voiced to unvoiced or vice versa) and prior to the start of speech.

Unvoiced excitation is used whenever the pitch parameter equals zero. The excitation has a constant magnitude of 0.5 and a pseudorandom sign. Since a pitch of zero guarantees a chirp ROM output of zero, it is necessary only to include the sign bit and a 1 for the excitation most significant bit to insert unvoiced excitation.

The 12 synthesis parameters are stored in the offchip ROMs in coded form. Each parameter has only certain allowed values within the 2^{10} possible combinations. Since the number of allowed levels is related to the number of code bits required in the ROM for each parameter, a compromise is made between speech quality and data storage.

A full set of parameters for each frame would require a data rate of 40 Hz x 48 bits = 1920 bits/s. (This would be 2400 bits/s at the maximum 50-Hz frame rate.) Three special cases, in which a full frame is not necessary, allow the data rate to be considerably reduced.

(1) Since the vocal tract changes shape relatively slowly, it is often possible to repeat previous reflection coefficient data. To facilitate the repeat feature, a control bit has been added to each frame. If this bit is 1, no more data are accessed from the ROM and the previous filter coefficients are retained.

(2) Unvoiced speech requires fewer filter coefficients. When pitch equals zero, only four of the ten filter coefficients are stored in ROM; the rest are zeroed.

(3) When energy equals zero, no other data are required. This corresponds to interword or intersyllable pauses.

The combination of these three effects has reduced average data rate to a level of 1200 to 1500 bits/s.

In most cases, it is best to vary the speech parameters smoothly from frame to frame rather than updating them only at the end of the frame period. Therefore, the synthesizer chip contains logic to do an approximately linear interpolation of all 12 parameters every 2.5 ms. The interpolation logic calculates a new parameter value from the present value and the next value stored in code in the parameter RAM. Interpolation is inhibited during transitions from silence to the initial frame of a phrase, from voiced to unvoiced speech and vice versa, and from a frame of zero energy to one of nonzero energy.

Filter output feeds into an 8-bit digital-to-analog converter residing on the synthesizer chip. This DAC provides least significant bit accuracy, low pass filtering, and 100-mW push-pull speaker drivers.

Circle 350 on Inquiry Card

2k x 8 EPROM Provides Flexibility At Low Cost

Organized as 2k 8-bit words, the TMS2716L erasable and electrically reprogrammable read-only memory from Motorola Semiconductor Products, Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721 is a pin-for-pin replacement of the Texas Instruments TMS2716JL, and is available on a second-source basis for that part. Pin compatibility to the MCM2708L and P, and 68708L EPROMs is an additional benefit. Upgrading to this n-channel silicon gate device from the 2708 reduces weight and halves power dissipation; providing a chip select input to pin 18 is the only board modification required.

This memory is provided in a 24-pin ceramic package with an ultraviolet window. It is available at a cost that its manufacturer states to be the lowest in the industry for a 16k EPROM: $23.10 in 100-piece quantities.

The device is designed for operation with 12- and ±5-V standard power supplies. Maximum access time and minimum cycle times are 450 ns. Absolute maximum ratings include operating temperature from 0 to 70 °C and storage between −65 and 125 °C, and 1.8-W power dissipation.

Circle 351 on Inquiry Card

CMOS Counters Offer Multiple Features On Single Chip

A family of CMOS 4-digit up/down counters combines several capabilities on single integrated circuit chips, with each feature available either separately or combined with the others. These capabilities provide a high speed 4-decade presettable up/down counter with carry out and parallel zero detect; settable registers and comparator; settable count offset; multiplexed LED display decoder/driver system; and multiplexed BCD outputs.

Counters are set through continuous comparison with an onboard presettable register. There are three main outputs from the chip: a carry/borrow, allowing direct cascading of counters; a zero, indicating when the count is zero; and an equal, indicating when the count matches the count contained in the register.

The devices also provide multiplexed 7-segment LED display outputs, with common anode or cathode configurations available. Intersil, Inc, 10710 N Tantau Ave, Cupertino, CA 95014 claims that these are the first counter circuits on the market capable of directly driving such displays with up to 250-mA peak digit drive current. They can drive displays of up to 1″ (2.54-cm) character height at a 25% duty cycle.

There are two versions of the device. ICM7217 is designed for hardwire applications where thumbwheel switches are used for loading data and simple spdt switches are used for chip control. In contrast to this, ICM7227 is designed for use in microprocessor based systems where presetting and control functions are performed under computer control.

These are also claimed to be the first electronic counters to provide a fully integrated multiplex oscillator onchip. This scan oscillator has a nominal free-running frequency of 10 kHz, which may be reduced by the addition of a single capacitor between the scan pin and the positive supply. Alternately, the oscillator may be directly overdriven to about 20 kHz. The internal oscillator output has a duty cycle of about 25%, generating a short pulse at the oscillator frequency, which clocks a 4-state counter to provide the four multiplex phases. A short pulse width

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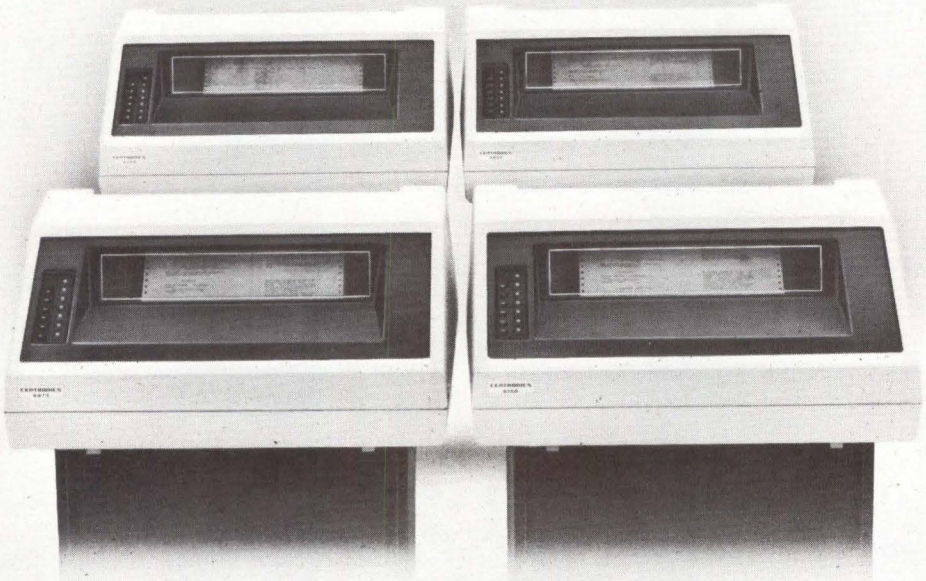

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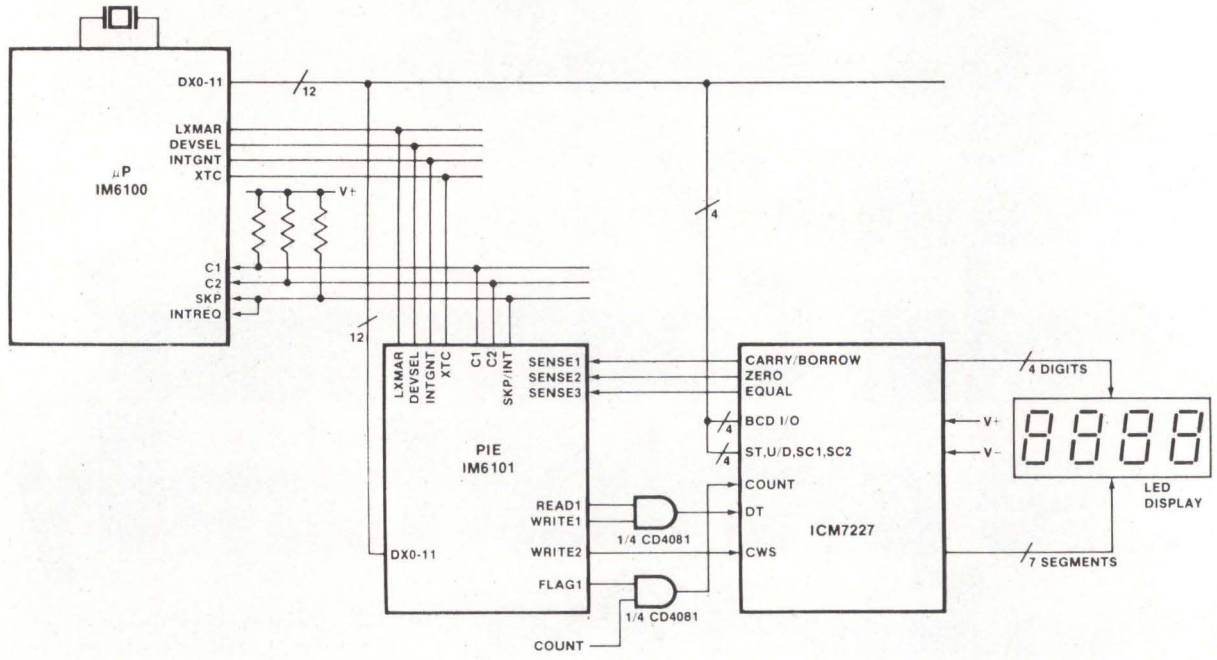

Up/down counter as peripheral to IM6100 microprocessor. IM6101 parallel interface element allows addition of one or more counters as generalized peripherals to any IM6100 system, with a minimum of external components

is used to delay the digit driver outputs, providing interdigit blanking (to prevent ghosting), and also providing decoding and leading zero blanking decision time.

Other capabilities of the family include operation up to 5 MHz on a single 5-V power supply, very low power consumption (with less than 5 mW of quiescent power), and a 3-state BCD I/O port. Data are multiplexed into and out of the device by means of this port, which acts as a high impedance input while loading. The BCD port (functioning as an output) will drive one standard TTL load; this capability is also true for the three main outputs.

Applications for these counters are numerous. For example, they can be employed as unit counters with BCD outputs, precision elapsed time/countdown timers, 8-digit up/down counters, low cost frequency counter/tachometers, low cost capacitance meters, LCD display interfaces, or microprocessor interfaces.

Absolute maximum ratings include power dissipation of 1 W (in a common anode ceramic DIP) or 0.5 W (in a common cathode plastic DIP). The supply voltage should not exceed 6 V. Operating temperature range is −20 to 70 °C, and storage temperature range is −55 to 125 °C.

Circle 352 on Inquiry Card

Digital Readout System Utilizes Bipolar IIL Modules

Two linear integrated circuits—an analog-to-digital converter and a BCD-to-7-segment decoder/driver—combine to act as digital readout system. Both ICs are bipolar devices, utilizing integrated injection logic (IIL).

The ADC, CA3162E, features dual-slope A-D conversion, an ultra-stable internal band-gap voltage reference, a hold input that inhibits conversion while maintaining the display, and internal timing (eliminating any need for an external clock.) A voltage-current converter converts the analog input into a current that charges an integrating capacitor. Clock pulses counted during subsequent discharge of the capacitor indicate the input voltage level, and a comparator converts the information into BCD output.

Timing is provided by a 786-kHz ring oscillator whose frequency is divided by 2048 to provide a multiplex rate of 384 Hz. Subsequent division by 96 results in the slow speed conversion rate of 4 Hz. However, part of the 96-divider is disabled when the hold terminal is biased at 5 V, resulting in multiplication of the slow speed conversion by 24 to produce a 96-Hz high speed conversion rate. During these conversions, the multiplex rate is maintained unchanged.

The device is capable of reading 99 mV below ground with a single supply. Overrange indications on the display modules show that the reading exceeds 999 mV or that it is more negative than −99 mV.

Absolute maximum ratings for the ADC include 7-V supply voltage, ±15-V input voltage, and power dissipation of 750 mW for temperatures up to 55 °C. Above 55 °C,

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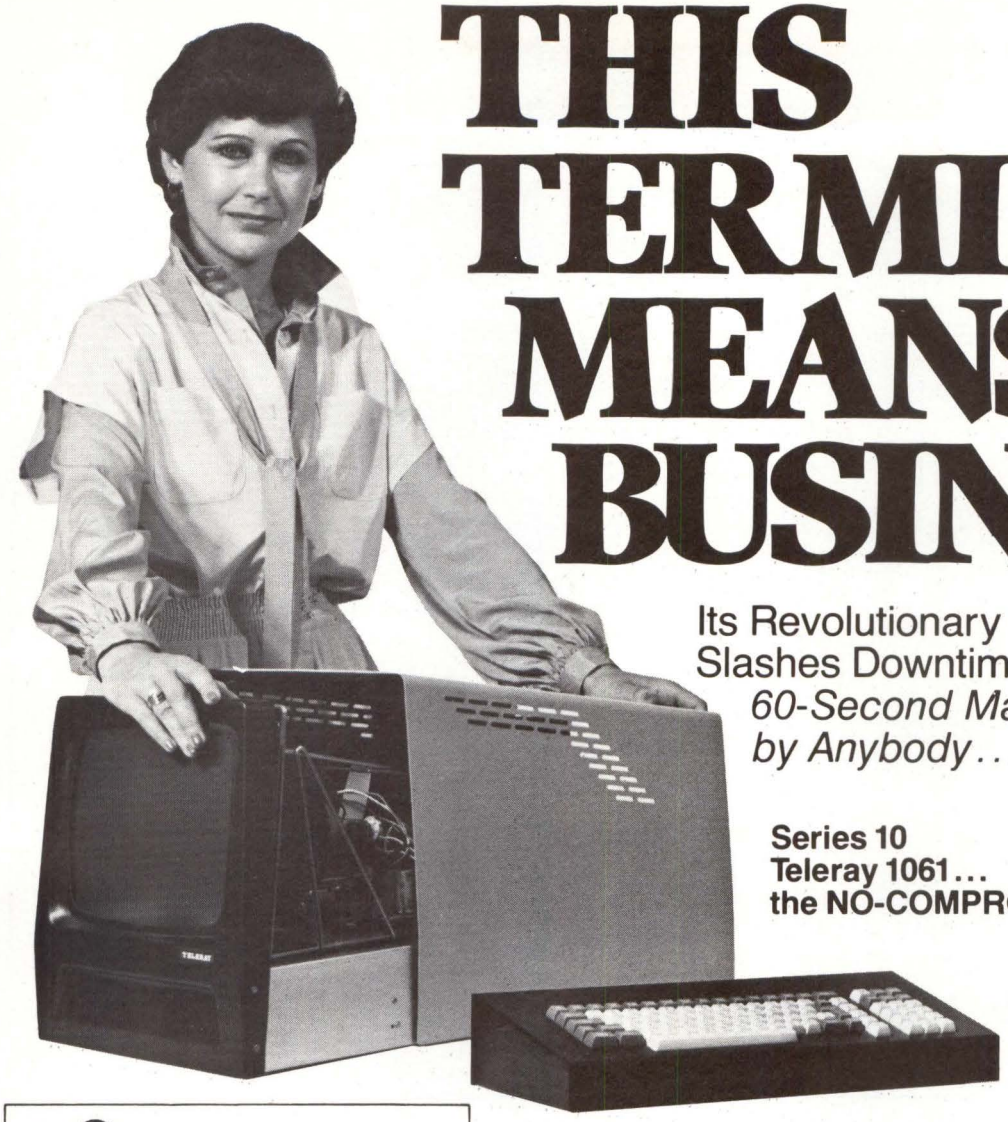

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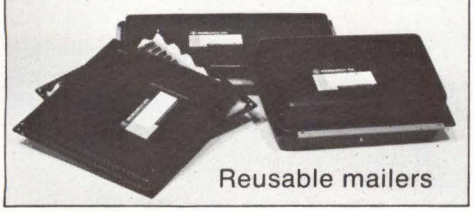

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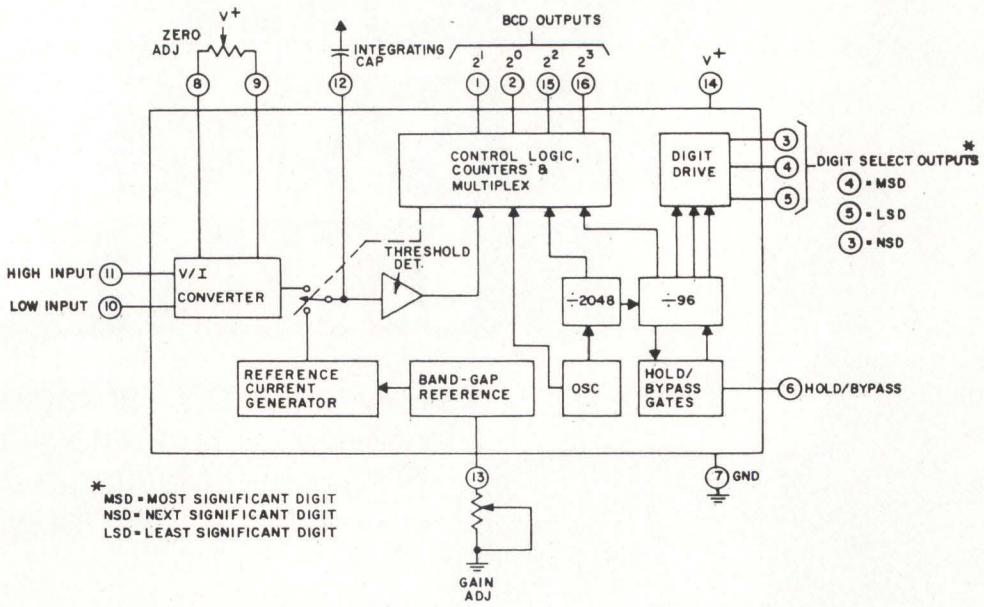
CIRCLE 102 ON INQUIRY CARD



RCA A-D converter CA3162E. Input voltage between terminals 10 and 11 is converted to current by V/I converter, charging integrating capacitor on terminal 12 for preset interval. At end of charging interval, V/I converter is disconnected from capacitor and band-gap reference contact-current source of opposite polarity is connected. Number of clock counts elapsing before charge is restored to initial value is measure of signal-induced current. Restoration is sensed by capacitor which latches counter. Count is then multiplexed to BCD outputs

dissipation must be derated linearly at 7.9 mW/°C.

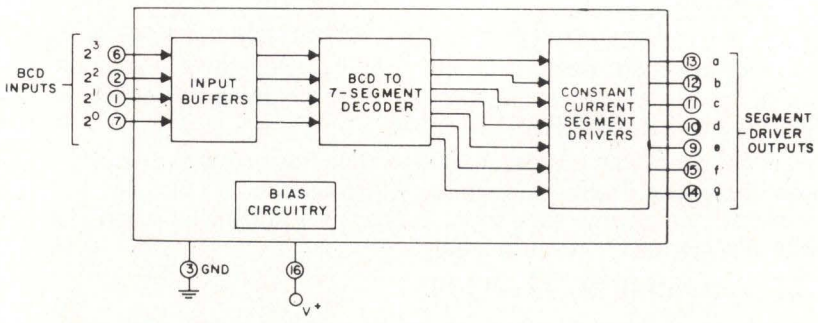
The BCD-to-7-segment decoder/driver, designated CA3161E, provides TTL compatible input levels and is compatible with other industry standard decoders. It features 15-mA (typ) constant-current segment drivers, which eliminate the need for current-limiting resistors. BCD inputs are decoded to 7-bit outputs via a truth table logic to drive selected display segments.

Absolute maximum ratings for the decoder/driver specify the following limits: dc supply voltage of 7 V, input voltage of 5.5 V, and voltage on any single output of 10 V for output on and 7 V for output off. Power dissipation limits are the same as described for the ADC module.

In the basic system application that uses these two modules, the BCD outputs of the ADC directly drive the BCD inputs of the decoder/driver. The 7-segment outputs are multiplexed to three LED displays. Digits are selected by terminals 3, 4, and 5 of the ADC, which provide base current to the external pnp resistors. Those resistors in turn, provide current to the anodes of the display.

The two modules are supplied in 16-lead plastic DIPs and operate over a temperature range of 0 to 75 °C. They are produced by RCA/Solid State Div, Route 202, Somerville, NJ 08876.

Circle 353 on Inquiry Card



CA3161E BCD-to-7-segment decoder/driver. BCD inputs go through input buffers to decoder where they are converted to 7-bit words. These are input to segment drivers whose outputs drive LED displays

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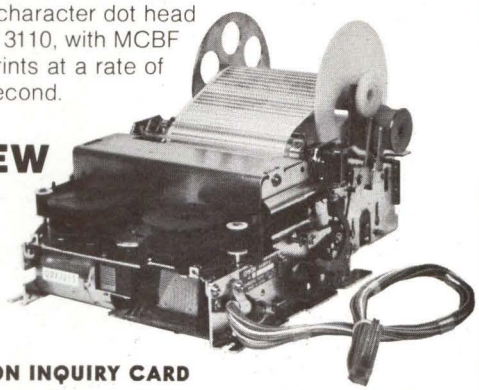
CIRCLE 103 ON INQUIRY CARD

MODEL 512
DOT MATRIX PRINTER MECHANISM
with 40 column format

This compact printer has the same 100,000,000 character dot head as the Model 3110, with MCBF of $5x10^6$. It prints at a rate of 3 lines per second.

NEW

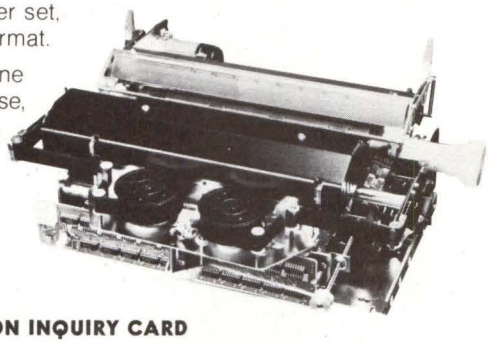


CIRCLE 105 ON INQUIRY CARD

MODEL 2610
LINE PRINTER MECHANISM
with fully formed characters

An EPSON-designed belt-impact printing mechanism gives clear, readable, fully formed characters. Model 2610 prints 150 lines per minute using a 64 character set, 80 column format.

A complete line printer with case, the Model 10, also is available.



CIRCLE 104 ON INQUIRY CARD

MODEL 6110
TAPE PUNCH MECHANISM
with full-size operation in a miniature chassis

A long-life punchblock that punches 100,000,000 characters with normal paper tape. Unique brushless motor affords long life, low power operation. Size is only 4"w x 6"d x 4¼"h. Operates at 50 characters per second.

CIRCLE 106 ON INQUIRY CARD

write for complete information and OEM prices

EPSON

EPSON AMERICA, INC.
23844 Hawthorne Blvd., Torrance, CA 90505
Telephone (213) 378-2220 · TWX 910 344-7390

Parallel 16-Bit Multiplier-Accumulator Performs 12-ns Operation

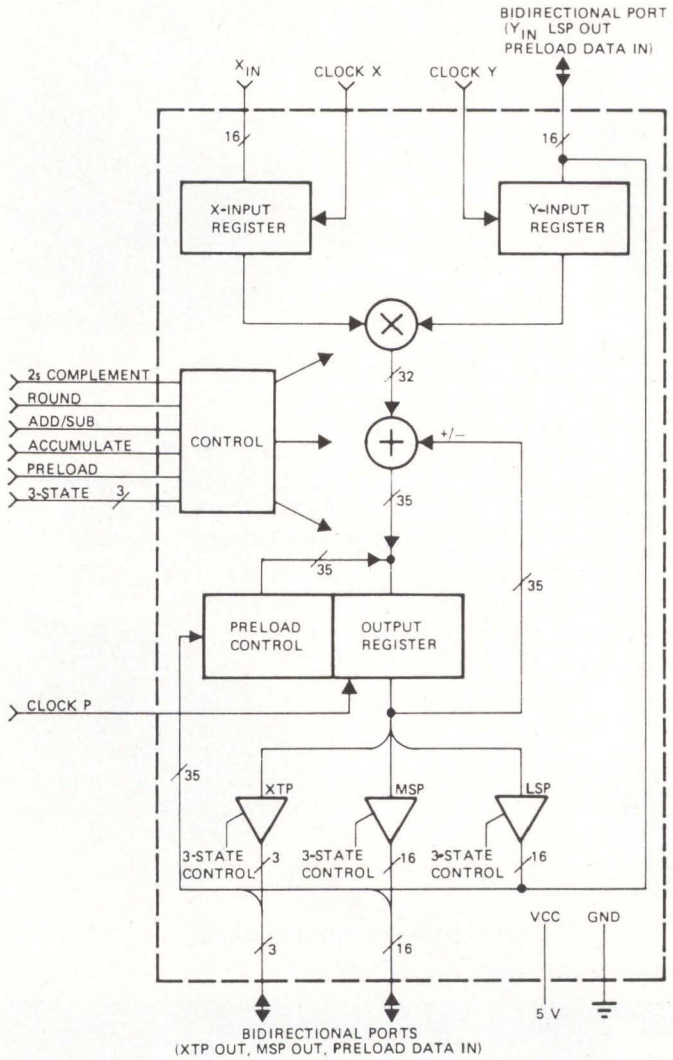
Implemented on a single chip, the TDC1010J arithmetic unit can carry out a 16 x 16-bit multiplication and product accumulation. Multiply-accumulate time is 120 ns, said by the manufacturer (TRW LSI Products, PO Box 1125, Redondo Beach, CA 90278) to be the fastest available at that word size. The device can be used as a multiplier or multiplier-accumulator and provides controllable addition or subtraction in a 35-bit accumulator subtractor. Principle application involves use as a central arithmetic block for digital signal processing devices, particularly complex multipliers, filters, and FFTs.

The numerical system can be either 2's complement or unsigned magnitude. Output contents can be added to or subtracted from the next product, or the accumulate function can be disabled for multiply-only mode. Input and output registers are provided, and initial data can be preloaded directly into the output register.

Other features include double or single precision capability, TTL compatible I/O, and three independent 3-state output controls. This radiation-hard device is provided in a 64-pin DIP, operating from a single 5-V power supply, with a 3.5-W power consumption.

Absolute maximum ratings include −0.5- to 7.0-V supply voltage, input and output voltages from 0 to 5.5 V, and storage temperature range of −65 to 150 °C. Operating temperature ranges are −55 to 125 °C for the commercial version and −65 to 150 °C for the military version (TDC1010JM).

Circle 354 on Inquiry Card



TDC1010J multiplier-accumulator. Device performs 16 x 16-bit multiply-accumulate in 120 ns. It has 3-state output controls, with all inputs and outputs TTL compatible

IIL Technology Featured In Monolithic CRT Controller

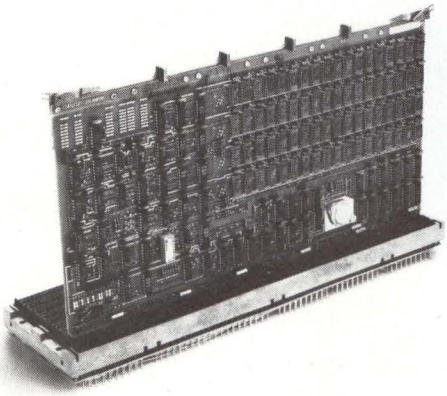
Integrated injection logic (IIL) and low power Schottky processes are combined on a single integrated circuit in the DP8350, a cathode-ray tube controller. The bipolar LSI device, developed by National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, combines an oscillator, complete timing, CRT refresh, logic, and video control circuits in a 40-pin package, replacing as many as 30 or 40 MSI, SSI, and discrete devices previously required for equivalent functions.

The chip is available in a standard configuration, providing a 5 x 7 dot matrix character in a 7 x 10 field. Overall display format is 80 characters wide, with 24 rows/frame. There are two refresh frequency options: a 60-Hz rate (providing 260 scan lines/frame) and a 50-Hz signal (providing 312 lines/frame). Horizontal scan frequency is fixed at 15.6 kHz. An internal dot rate oscillator, controlled by an external 10.92-MHz crystal, gives the device a 91.6-ns dot time. Character time is 641 ns. System control input and character random-access memory outputs are handled by a 12-bit bidirectional Tri-State® bus.

For special display requirements, the manufacturer can mask-program the chip to the user's specifications.

(Continued on p 211)

DEC® never had it so good

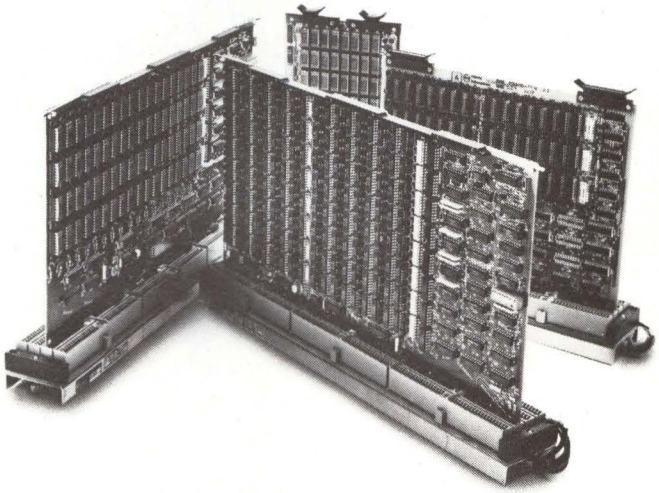


DEC's semiconductor memories:
If you want to, you can always buy semiconductor memories for your DEC mini's from DEC.

But they tend to be bulky (16K bytes to a board for some mini's and *five* boards for their ECC unit).

And you probably already know about DEC's pricing structure on additional memory.

®Registered trademark of Digital Equipment Corporation



Plessey's:
We offer a complete family of DEC-compatible semiconductor memories.

64K, 128K and 256K bytes (with ECC) for the DEC PDP-11® series. 128K words for the PDP-8A®. And 64K bytes for the LSI-11,® PDP-11/03® and our own Micro-1.

Our plug-compatible memories cost less and run faster than DEC's. Reliability is ensured through 100% component burn-in and 100% board testing. Each and every memory is then run in the minicomputer it was designed for before we ship it out the door.

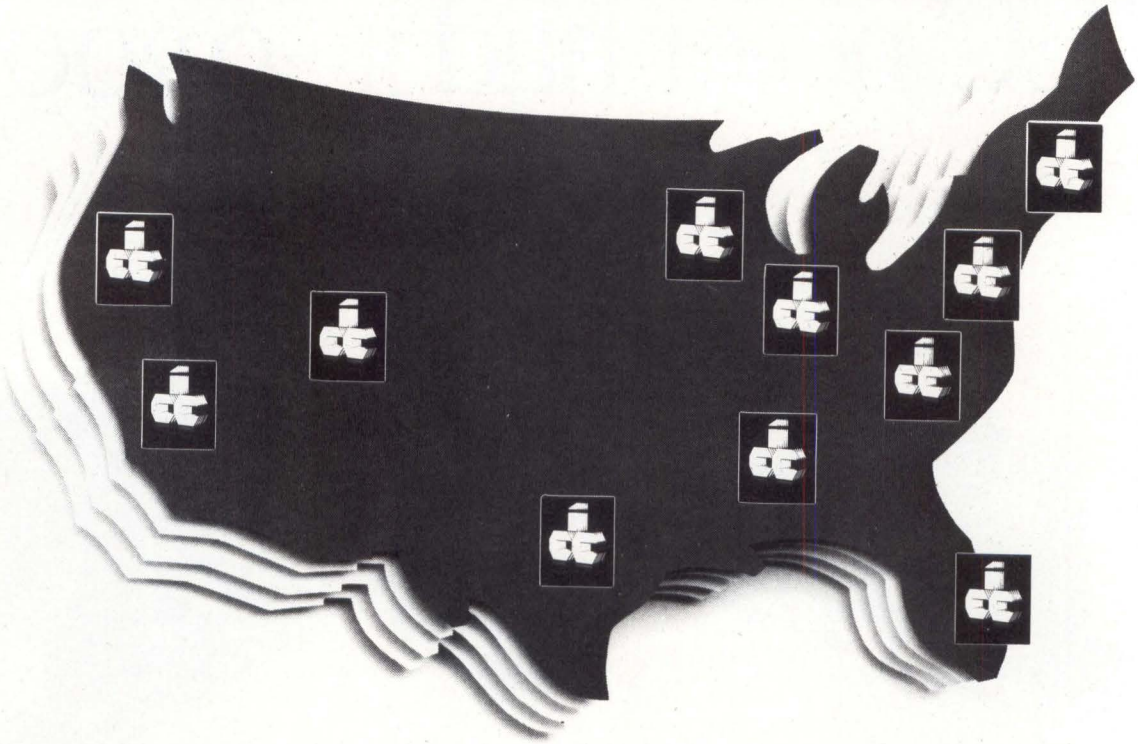
This kind of care has made us the largest independent supplier of DEC-compatible peripherals. Our product line presently includes add-in/add-on core and semiconductor memories, cartridge disc systems, floppy disc systems, mag tape systems, complete computer-based systems, and a wide variety of backplanes, expansion chassis, and other accessories.

We're the only real alternative to DEC for all your miniperipherals, a complete single source. For all the details, please contact the nearest Plessey sales office today.

Plessey Peripheral Systems
17466 Daimler, Irvine, California 92714, (714) 540-9945

CIRCLE 107 ON INQUIRY CARD

OEM America Meets



at the Invitational Computer Conferences

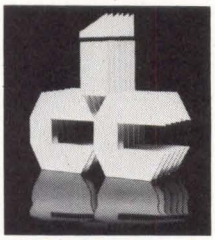
In Boston... in Ft. Lauderdale... in Denver and eight other cities, OEM decision-makers meet the country's top computer and peripheral manufacturers at the Invitational Computer Conferences – the only seminar/displays designed specifically for the unique requirements of the quantity user.

In one day, at each 1978/79 ICC, guests will receive a concentrated, up-close view of the newest equipment and technology shaping our industry. Some of the companies participating in the 1978/79 ICC Series are:

CalComp, Cambridge Memories, Inc., Centronics, Cipher Data Products, Inc., Compugraphic Corp., Computer Automation, Inc., Computer Design, Computerworld, Control Data Corp., Data 100 Corp., Datamation, Datamedia Corp., Dataproducts Corp., Dataram Corp., Data Systems Design, Inc., Datum, Inc., Diablo Systems, Inc., Digital Design, Electronic Engineering Times, Honeywell Information Systems, Houston Instrument, ISS/Sperry Univac, Kennedy Company, Lear Siegler, Inc., MDB Systems, Inc., Microdata Corp., Mini-Micro Systems, Monolithic Systems Corp., National Semiconductor, NEC Information Systems, PCC/Pertec Division, Perkin-Elmer Data Systems, PerSci, Inc., Pioneer Magnetics, Inc., Plessey Periperhal Systems, Powertec, Inc., Printronix, Inc., Remex, Rianda Electronics, Ltd., Shugart Associates, Storage Technology Corp., Sykes Datatronics, Inc., Tally Corp., Tektronix, Inc., Teletype Corp., Telex Computer Products, Inc., Texas Instruments, Inc., Trilog, Wangco.

The schedule for the 1978/79 Series is:

Sept. 6, 1978	Newton, Mass.
Oct. 3, 1978	Valley Forge, PA
Oct. 5, 1978	Washington, D.C.
Nov. 9, 1978	Palo Alto, CA
Jan. 16, 1979	Orange County, CA
Feb. 8, 1979	Ft. Lauderdale, Fla.
Feb. 26, 1979	Atlanta, GA
Mar. 29, 1979	Dallas, Texas
April 17, 1979	Dayton, Ohio
April 19, 1979	Chicago, Ill.
May 8, 1979	Denver, Colo.



Invitational Computer Conferences

Invitations are available from participating companies or the ICC sponsor. For further information contact: B. J. Johnson & Associates, 2503 Eastbluff Drive, No. 203, Newport Beach, CA 92660. (714) 644-6037

Basic die architecture remains the same; however, major video characteristics may be changed due to the changing of information contained in onchip ROMs. Within the constraints of the frame refresh rate, the user may specify character and field size, number of characters per row, and number of rows. Horizontal and vertical sync pulses, cursor enable output, and vertical blanking output are also programmable.

One application example relating to the device is a low component count video data terminal using the CRT controller and the INS8080 CPU. The CRT controller generates all the required control and timing signals for displaying information on the video monitor. In doing so, it provides dot clock, control, and counter outputs for the character generator, direct drive horizontal and vertical sync signal outputs, and a direct cursor address location output. It also acts as a bidirectional RAM refresh counter for refreshing the video RAM and allowing microprocessor loading to its own internal registers.

The manufacturer states that MOS CRT controllers cannot handle the high speed portions of the controller block, such as dot logic, whereas this IIL/Schottky CRT controller is well-suited to both control logic and high speed logic functions. This controller is usable as a minimum chip solution for a wide range of dumb, smart, and intelligent CRT terminal systems.

Both the standard and semicustom versions of the chip require a single 5-V source. Current typically drawn is 150 mA, for a 750-mW power consumption.

Hybrid Sample/Hold Features Fast Acquisition

Designed for application with high speed 12-bit A-D converters, a sample/hold circuit provides an acquisition time of 1.0 μs with a 0.01% accuracy (0.5 bit out of 12) for a 10-V step. An 800-ns acquisition time is attained at a 0.1% accuracy level. Furthermore, the input amplifier of the device is uncommitted, allowing a variety of closed loop connections; it may be connected for any gain from ± 1 to ± 10.

SHM-6 is manufactured by Datel Systems, Inc, 1020 Turnpike St, Canton, MA 02021 with thin film hybrid technology. It uses a high impedance input transconductance amplifier to drive a self-contained 400-pF MOS holding capacitor. The resulting hold mode droop is 10 μV/μs; for slower applications, the droop can be reduced by addition of an external holding capacitor. Two sampling switches direct the output current of the transconductance stage either to the holding capacitor (in sample mode) or to ground (in hold mode). The ground connection in the hold mode results in a low hold mode feedthrough of 0.01% maximum.

Other characteristics include 20-ns aperture time, 5-MHz bandwidth, and programmable gain. Maximum ratings include 18-V positive and negative power supplies, 7-V logic supply, and 5.5-V digital input voltage. The device is packaged in a miniature 32-pin case with DIL pin spacing. Size is 1.1 x 1.7 x 0.160" (28 x 43 x 4 mm). Four models cover the operating temperature ranges of 0 to 70 °C, −25 to 85 °C, and −55 to 100 °C.

Circle 355 on Inquiry Card

Small dc-dc Converter Produces Isolated Dual Outputs

Bipolar direct current outputs on two isolated channels are developed from a single input voltage by the 722 converter. The input voltage to the converter ranges between ± 5 and ± 16 V. Output voltage is of the same absolute range as input.

The device has dimensions of 1.1 x 1.1 x 0.3" (27.9 x 27.9 x 7.6 mm). In addition to these small linear dimensions, it features low leakage current (1 μA at 240 V/60 Hz), isolation impedance of 10^{10} Ω in parallel with 6 pF, and a high breakdown voltage (tested at 8000 V). The manufacturer, Burr-Brown, International Airport Industrial Park, PO Box 11400, Tucson, AZ 85734, uses the rule of thumb that briefly-applied test voltages should equal double the continuous operating voltage plus 1000 V. Thus, for this system, isolation of output from input has a maximum rating, for continuous voltage, of 3500 V. Similarly, the two output channels are isolated from one another by 2000 V continuous and 5000 V test.

Total output current of 64 mA can be divided among four outputs (two channels, each with plus and minus outputs and common). Output channels can be connected in series or in parallel to produce higher voltages or currents.

Complete system power and signal isolation is achieved when the converter is combined with the company's 3650 and 3652 optically coupled isolation amplifiers. For example, the converter can be connected to an amplifier in a configuration that provides 3-port isolation. One converter channel supplies power to the amplifier's input. The other channel supplies power to the amplifier's output. Input and output are isolated from each other and the system's power supply common. In this configuration, the converter's channel-to-channel isolation specification applies to the amplifier input-to-output voltage.

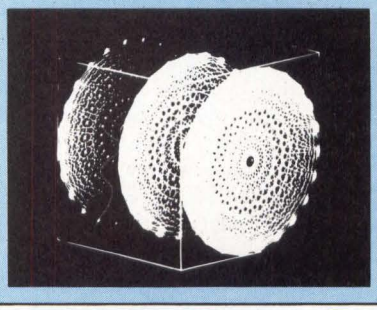
Circle 356 on Inquiry Card

ADVANCED TECHNICAL

Course 365 — Four days

Computer Graphics

State of the Art Techniques and Applications



LOS ANGELES
October 17-20

CHICAGO
November 7-10

BOSTON
December 12-15

ATLANTA
January 16-19

NEW YORK
February 13-16

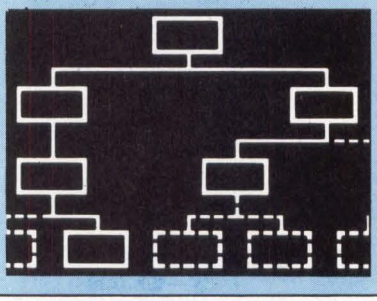
Hardware elements of computer graphics systems are presented at the level required for detailed system specification, selection and acquisition. Software techniques for computer graphic systems are developed from the elementary level of line generation and continue through advanced approaches to animated three-dimensional color displays with hidden surface removal. Off-the-shelf, commercially available software packages are analyzed and evaluated. Emphasis is placed on hardware/software tradeoffs, cost effectiveness and the advantages and limitations of alternative approaches.

- Display Hardware
- Color Display Techniques
- Two Dimensional Graphics
- Three Dimensional Graphics
- Transformations
- Software Structures
- The Hidden Line Problem
- The Hidden Surface Problem
- Software 'Build or Buy'
- Selection Methodology

Course 320 — Four days

Structured Programming

Design, Coding and Implementation Techniques



LOS ANGELES
November 7-10

WASHINGTON, D.C.
January 16-19

BOSTON
January 30-Feb. 2

NEW YORK
February 20-23

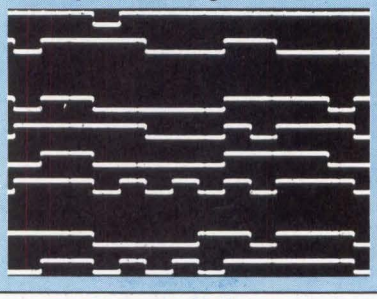
This course is designed for programmers, software engineers, systems analysts and their managers who are charged with the responsibility of creating and maintaining reliable, complex program structures. Partici- pants will develop a clear understanding of the concepts and applicatio of structured methodology, and will learn to evaluate various types of str tured programming techniques. The course will provide in depth exposu to structured design and structured programming tools and procedures The underlying theme of the course is the development of skills which w enable the production of structured programs at minimum cost, while pl ning for program changes, modifications and reducing maintenance co

- Principles of Structured Program Design
- Case Study Workshop
- Implementing Structured Coding
- Developing Structured Systems
- Productivity Mgmt and Project Control
- Organizing the Programming Team

Course 445 — Four days

Data Communications

Digital Techniques and System Design



NEW YORK
October 24-27

BOSTON
November 14-17

LOS ANGELES
December 12-15

DALLAS
January 23-26

CHICAGO
February 6-9

WASHINGTON, D.C.
March 13-16

This course is designed for engineers, scientists and system designers v are involved in the planning, design or implementation of all types of digi communications systems. The course covers the fundamental principles signal conversion, encoding/modulation, data transmission and error co trol. It analyzes the individual elements of a data communication system and clearly describes how these elements may be synthesized to form a system which best meets application specific objectives.

- Coding for Data Transmission
- Detection of Data in Noise
- Digital Modulation
- Security Considerations
- Errors and Error Control
- Analog-to-Digital Conversion
- Pulse Code Modulation (PC
- Signal and Video Encoding
- Packet Switching/ Packet Radio
- Implementing a Data Communications Syster

COURSE ENROLLMENT INFORMATION

Course Hours:

Orientation (First Day): 8:15–9:00 A.M.
Lecture Sequence: 9:00 A.M.–4:30 A.M.
Informal Discussion Session with Instructor: 4:30–6:30 P.M.

Course Fees:

Four-Day Courses: (365, 320, 350, 412 or 445): **$695.00** (U.S.)
Microprocessors and Microcomputers Series
Individual Courses: 111 or 102s (One Day): **$195.00** (U.S.)
130a (Three Days): **$495.00** (U.S.)
Combinations: 111 and 102s (Two Days): **$390.00** (U.S.)
102s and 130a (Four Days): **$595.00** (U.S.)
Complete Series: 111/102s/130a (Five Days): **$695.00** (U.S.)

Course Fees Include: lectures, lecture-coordinated notes, extensive reference materials, luncheon & coffee breaks.
Team/Group Discount: 10% reduction for three or more participants from the same organization, if invoiced at the same time.

DIPLOMA/CONTINUING EDUCATION UNITS

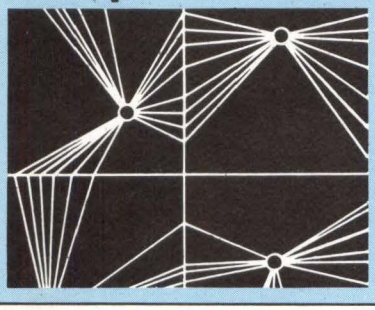
Each attendee receives a Course Completion Certificate awarding one Continuing Education Unit (CEU) for each ten hours of class participation. The CEU is a nationally recognized unit awarded by universities and educational organizations for participation in continuing educational programs.

EDUCATION

INTEGRATED COMPUTER SYSTEMS, INC.

Course 350 — Four days

Distributed Processing and Computer Networks



PHILADELPHIA
November 7-10

BOSTON
December 5-8

ATLANTA
January 23-26

DALLAS
January 30-Feb. 2

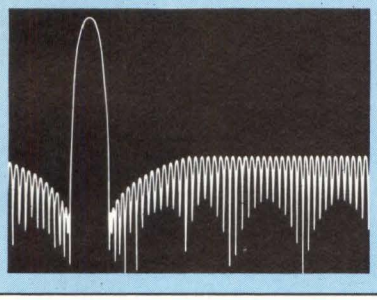
NEW YORK
February 13-16

This course provides a comprehensive introduction to distributed processing and computer network design techniques. It covers the individual elements of a distributed processing system and how these elements are synthesized to form a system which best meets application specific objectives. Throughout the course, application examples provide concrete examples of the concepts presented, with emphasis on the factors affecting key planning, design and implementation decisions.

- **What is to be Distributed?**
- **Data Communication Concepts**
- **The Computation Continuum**
- **Computer Networks**
- **Network Protocols**
- **Database Structures**
- **Database Requirements**
- **Security Considerations**
- **Evaluation and Selection**
- **Management and Control**

Course 412 — Four days

Digital Signal Processing



PHILADELPHIA
October 31-Nov. 3

BOSTON
December 5-8

LOS ANGELES
December 12-15

WASHINGTON, D.C.
January 16-19

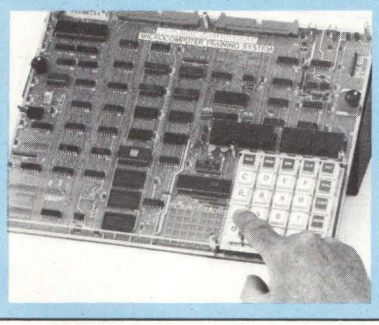
NEW YORK
February 20-23

The objective of this course is to present the necessary fundamentals of digital signal processing in a clear and comprehensible manner, to develop an understanding of new processing techniques, to survey the state of the art of hardware and software available, and to apply this information to a range of concrete design examples. The course is of benefit both for those who wish to achieve a basic understanding of this exciting area, and for those whose interest is in advanced techniques and the implementation of practical systems.

- **An Overview of Applications**
- **Digital vs. Analog Signals**
- **Operations on Digital Signals**
- **Recursive Filters**
- **Nonrecursive Filters**
- **Design Techniques**
- **Computer Aided Design**
- **Statistical Approaches**
- **Spectral Estimation**
- **Application Case Study**

FIVE-DAY COURSE SERIES

MICROPROCESSORS & MICROCOMPUTERS



SAN DIEGO
October 30-Nov. 3

CHICAGO
November 6-10

WASHINGTON, D.C.
December 4-8

ATLANTA
December 11-15

LOS ANGELES
January 15-19

DENVER
January 22-26

DALLAS
January 29-Feb. 2

Course 111: One day — Monday

MICROPROCESSOR PROJECT MANAGEMENT
From design through manufacture, QA and field service

Course 102s: One day — Tuesday

MICROPROCESSORS AND MICROCOMPUTERS:
A Comprehensive Technical Introduction and Survey

Course 130a: Three days — Wed., Thurs., Fri.

HANDS-ON MICROCOMPUTER PROGRAMMING AND INTERFACING WORKSHOP
EACH student receives a complete 8080 microcomputer and interfacing system for his personal use throughout the course.

☐ PLEASE ENROLL ME IN **COURSE:** _____

CITY _____

DATE(s) _____

MAIL TO:
Course Manager
INTEGRATED COMPUTER SYSTEMS, INC.
3304 Pico Blvd., P.O. Box 5339
Santa Monica, CA 90405

OR CALL: (213) 450-2060

A confirmation letter with complete details will be forwarded to you.

Name _____ Job Title _____

Company _____ Mail Stop _____

Address _____

City _____

State _____ Zip _____ Telephone _____

☐ Please send FREE BROCHURES describing these courses.
☐ Please put me on your mail list to receive future course schedules.

High Current and Voltage VMOS Power FET Serves Analog and Digital Uses

With input power in the microwatt range, the VN84GA produces a 50-W output at 30 MHz and up to 80 W at lower frequencies. This VMOS power FET has rated outputs of 12.5 A, 80 V, and 0.4 Ω. Siliconix Inc, 2201 Laurelwood Rd, Santa Clara, CA 95054 states that it provides approximately a sixfold current increase over previously available circuits.

Input power for the device is several orders of magnitude less than that required by Darlington bipolars of equivalent output power. Yet it retains the benefits of faster switching, high gain, and high input impedance characteristic of lower power VMOS units. It operates without failure from secondary breakdown, with no thermal runaway, and has the ability to limit current by controlling gate voltage. Rise and fall are less than 50 ns.

Applications include use in switching regulators, linear amplifiers, and logic interfacing. As a logic interface, the device benefits from its high impedance VMOS properties. In addition, no power supply connections are required.

Circle 357 on Inquiry Card

IC Drives High Voltage Fluorescent Displays

Made up of seven independent digit driver sections on a single chip, the XR-2272 acts as a buffer interface between MOS outputs and the anodes of a gas discharge panel. This display driver is characterized by high breakdown voltages and operates with supply voltages up to 60 V.

Produced by Exar Integrated Systems, Inc, PO Box 62229, Sunnyvale, CA 94088, the device is well-suited to interfacing with Panoplex II[R] type displays, although its interfaces are versatile. The circuit is especially designed to work with the XR-2271 segment-driver IC to form a 2-chip complete display driver system.

Additional features include active low inputs, low power dissipation, complete I/O isolation, and onchip pull-up resistors. Furnished in a 16-pin DIL plastic package, the device has absolute maximum ratings that include a negative supply voltage of −75 V, package power dissipation (at 25 °C) of 625 mW, and operating temperature range of 0 to 75 °C.

Circle 358 on Inquiry Card

Monolithic CMOS ADC Family Operates Over Wide Temperature Range

Analog-to-digital converters utilizing CMOS technology require only 20 mW of power and provide a conversion time of from 1 to 20 ms. They are guaranteed for ±½ LSB accuracy over a −55 to 125 °C range.

Produced by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, the family includes the 8703 (8-bit), 8704 (10-bit), 8705 (12-bit), and 8750 (3½-digit) single-chips ADCs. These devices have an infinite input range, since any positive voltage can be applied via a scaling resistor. They are easy to use because of parallel latched outputs with 3-state control, strobed or freerun conversion, and two handshake outputs for interfacing with computers. At the end of conversion the total count is latched into the digital outputs as a parallel word. A control switches the outputs to a high impedance state when held high.

Absolute maximum ratings include 18 V for V_{DD}-V_{SS}, ±10 mA for I_{IN} and I_{REF}, and a 500-mW package dissipation. The devices are provided in 24-pin ceramic packages that are either flat (H package) or DIL (N package).

Circle 359 on Inquiry Card

Wide Band Epoxy Op Amps Feature High Slew Rates

An epoxy-packaged operational amplifier from Harris Semiconductor Group, PO Box 883, Melbourne, FL 32901 provides a minimum slew rate of 60 V/μs with a settling time of 200 ns. It also offers a wide power bandwidth of 750 kHz minimum and a high gain bandwidth of 20 MHz. The device is the HA-2527, the top performer in the HA-2507/2517/2527 line. Wide power bandwidths and high slew rates are characteristic of all three versions.

Slew rate and settling time performance make these devices appropriate for high speed D-A and A-D converter and pulse amplification designs. Their bandwidths also make them useful in video applications.

Closely related to these are the HA-2607 and HA-2627. The higher performer of the pair is the 2627, which provides a wide gain bandwidth of 100 MHz, a slew rate of 17 V/μs (min), and a wide power bandwidth of 290 kHz (min). These two devices are suited to pulse amplification designs and high frequency applications. The frequency responses of both amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor.

All amplifiers are available in 8-lead epoxy DIPs. Performance is specified over a 0 to 75 °C range.

Circle 360 on Inquiry Card

Fast Analog Comparator Operates On 5-V Supply

Typical response time for the 9915 analog comparator is approximately 20 ns. The device is also characterized by operation from a single 5-V supply. Furthermore, its inputs can sense the common level, making it a high speed zero-crossing detector.

Optical Electronics Inc, PO Box 11140, Tucson, AZ 85734 states that under identical test conditions with a National Semiconductor LM192, this device showed a typical response time of 12 ns compared to 300 ns for the other part. Pinouts of both are identical.

Further characteristics of the comparator include TTL and LSTTL elements, with an output fanout of 25 LSTTL gates and a −55 to 125 °C operating range. Pins of the 8-pin mini DIP are compatible with any standard 0.3″ (0.76-cm) DIL socket.

In addition to zero crossing detection, high speed applications include A-D conversion, level detection, and use as a peripheral device for microcomputers. MTBF has been established per MIL-HDBK-217B-GF at over 1M hours. □

Circle 361 on Inquiry Card

This is the first vidicon camera designed specifically for use with digital and analog computers. The equipment is designed to shake hands with both types of computer systems. Thus it fulfills many applications as an "eye" for automated industrial inspection, image analysis, biological research and university research.

APPLICATIONS:

MEDICAL
Tissue analysis
Blood analysis
Neurological—X-Y movement analysis
Optical Instrument data analysis
Other analysis of visual data

INDUSTRIAL
Aerial photography analysis
IR Analysis—detect forest fires
Bottle inspection
Dimension analysis and control
Printed pattern analysis
Missile tracking

UNIVERSITY
Analysis of any visual information
Medical research
Physics research
Laser technology

Write for brochure

C-1000 the first TV camera designed for computer interface.

NOTES TO THE SYSTEMS ENGINEER

Ordinary TV cameras are designed to produce a picture on a monitor, not interface with a computer. Proper timing pulses are not available and their shape is inappropriate for computer use. The clock is usually a tuned circuit or a low frequency crystal. While fully adequate for viewing, the precision of these circuits becomes a limiting factor in a computer camera system. The pulses occur infrequently and at periods during the scan format that is wasteful of computer time.

The C1000 system was designed to have a basic clock of 25.39 MH_Z with its half frequency accessible to the computer using TTL logic. All sweeps, blanking and unblanking information are controlled by this computer accessible signal. The basic signal and a number of other timing signals are available and can be brought out by use of the M998 I/O buffer, M999 I/O interface, or a user designed buffer. The customer can build his own interface, or buffer, thus saving considerable money.

All of the digital lines are clock controlled to avoid jitter and to insure maximum precision and reproducibility. The video output from the C1000 is fully usable with standard TV monitors thus no function is lost by making the system computer compatible as is the case with some computerized video systems manufactured by others.

HAMAMATSU

HAMAMATSU CORPORATION • 120 WOOD AVENUE • MIDDLESEX, NEW JERSEY 08846 • PHONE: (201) 469-6640

International Offices in Major Countries of Europe and Asia

CIRCLE 110 ON INQUIRY CARD

PRODUCT FEATURE

Versatile Instrument Solves

Variety of IEEE 488 Bus Related Problems

Multiple capabilities as an IEEE bus analyzer, tester, exerciser, monitor, and controller are combined on a single but flexible instrument introduced by Interface Technology. The model 488 programmable monitor/analyzer can be used by both circuit designers and system troubleshooters. Depending on cable length, the fully IEEE 488/1975 bus compatible unit can drive as many as 14 devices simultaneously at data transfer rates up to 250k bytes/s.

Application areas for this instrument include straightforward monitor for troubleshooting minicomputer or calculator based IEEE bus systems; analyzer for evaluating compatibility and characterization of IEEE bus instruments or subsystems; exerciser for development of IEEE compatible interfaces and instruments; and controller for small bus systems. Instructions for any application can be programmed from either the instrument's front panel or a remote interface.

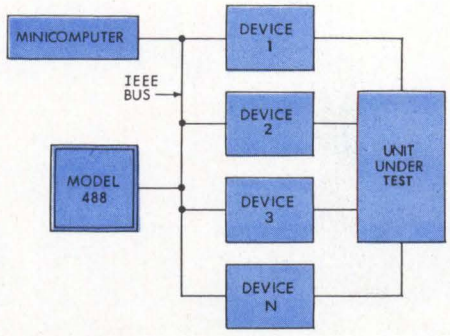
Functional Description

Because a bus system may contain 10 or even more interconnected devices, assuring compatibility is a major problem. Programming of this monitor/analyzer enables the instrument to run through repeated fixed bus sequences to evaluate devices for compatibility. By setting up faulty conditions and monitoring errors, the instrument also determines bus functions to which a device will respond and the sequence of events that could cause the device to malfunction. The instrument can be programmed to characterize a bus compatible instrument fully and then be reprogrammed to accommodate other devices added to the bus system.

Bus monitoring also is used to check out bus system devices that might be supplied by different manufacturers. This function allows users to trigger on a specific bus or device transaction to record a given number of data bytes and control states, up to a maximum of 511 transactions. Recording occurs in conjunction with the handshake activity and the data can be monitored via the front panel display either in hexadecimal or IEEE bus oriented alphanumeric language.

For applications in which the bus system controller has a peculiar mode of operation or timing condition that must be simulated for offline debugging, calibration, or exercising of unique functions of a device tied to the bus, a simulation mode may be set up. Simulation can also be used when developing new interfaces. Development time can be shortened through use of the instrument's static, dynamic, and interactive modes.

In the area of bus control, the monitor/analyzer provides almost as much versatility as a combination of calculator, minicomputer based controller, terminal, and fixed applica-



Model 488 programmable monitor/analyzer in typical application as system monitor for troubleshooting, debugging, and data logging

tion controller. Control sequences can be executed in any of several fixed formats stored on EPROM or in a unique format programmed from the instrument's front panel.

Sequences of instructions that are to be executed to activate desired bus functions are stored in program memory and can be generated at three levels: the stored program level, where programmed information has been prepared in machine language code and loaded into EPROM; the IEEE bus language level, where the information is programmed from the front panel in a "macro" level language for easy operator comprehension; and the machine language level, where programmed information is entered into the instrument via the front panel in machine language. Remote data entry and readback of memory data are also optionally available through a variety of interfaces. In addition, data memory can store data that are to be transmitted to an end device via the IEEE bus, data space that will be loaded with data from an end device, and comparison data that will be used to compare expected responses from an end device.

A 16-character display on the monitor/analyzer prompts the user and provides readout of key parameters. Keyboard and control switches, organized to minimize manual operations, provide all local inputs.

Specifications

The monitor/analyzer is both electrically and mechanically compliant with IEEE Standard 488/1975. Supplied memory is 255 bytes of RAM and 256 bytes of fixed ROM; 16k bytes of plug-in EPROM are available as an option. Both are machine coded. Data memory consists of 511 bytes. Physical dimensions are 5.25 x 17 x 16″ (13.4 x 43.2 x 40.7 cm). Weight is 28.6 lb (13 kg). Power requirements are 115 Vac, 50/60 Hz, 110 W; 100/200/220/240-Vac units are available.

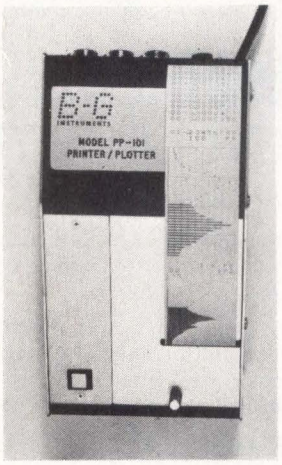
Price and Delivery

The model 488 programmable IEEE bus monitor/analyzer is priced at $3500 in single quantities. Deliveries will begin in October. Interface Technology, 852 N Cummings Rd, Covina, CA 91724. Tel: 213/966-1718.

For additional information circle 199 on inquiry card.

PRODUCTS

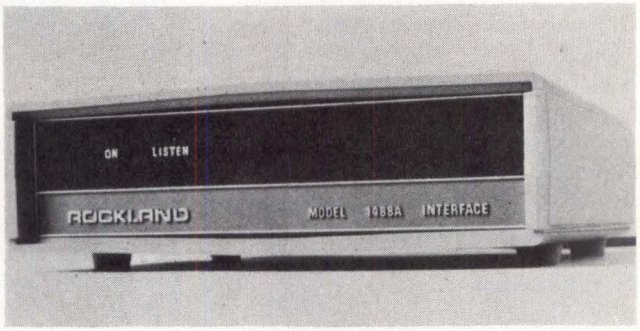
Low Cost Thermal Printer/Plotter Accepts Parallel Input Numerical Data



Accepting numerical data directly from a TTL compatible parallel data source such as DVM, frequency counter, or other BCD or binary source, PP-101 prints 5 x 7 dot matrix characters or plots in a variety of graphic formats. User selects display format and other parameters by grounding appropriate terminals on the unit's interface connector, using wires, switches, or external logic control. An onboard Intel 8035 microcomputer with 2k memory provides all necessary interface and control functions, including self-strobing for automatic data logging. The unit prints on 2.25″ (5.72-cm) wide thermal paper at 2 lines/s. Normal plotting occurs at 6 data points/s. Data are printed as 8 columns with 2-digit identifier, and decimal point and minus sign if selected. Unit is available complete with cabinet and power supply, or as print/plot mechanism and control electronics assembly alone. **B-G Instruments,** Box 67, Alta Loma, CA 91701.

Circle 200 on Inquiry Card

Standalone IEEE Bus Interface Incorporates Frequency Synthesizers in Computer Controlled Systems



Model 1488A-11, designed for incorporation of series 5600 frequency synthesizers into automatic, computerized, or microprocessor-controlled systems using the IEEE 488/1975 instrumentation bus, plugs into the associated synthesizer and the host system via std cables, and provides full compatibility with both, meeting all specified constraints of IEEE 488/1975, and providing everything the instrument needs for full control of all programmable parameters. Instrument satisfies all bus timing and loading constraints, and is significantly faster than most program sources, accommodating data transfers at up to 1M byte/s. Full buffering of data is provided; data entry is byte-serial, but no transfer is made until a load command is sent. Interface contains built-in regulated dc power supply; only ac power (115/230 Vac ±20%, 50 to 60 Hz, 40 W max) need be supplied. **Rockland Systems Corp,** 230 W Nyack Rd, West Nyack, NY 10994.

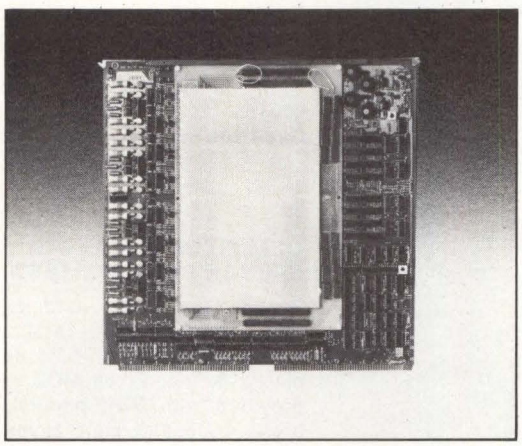
Circle 201 on Inquiry Card

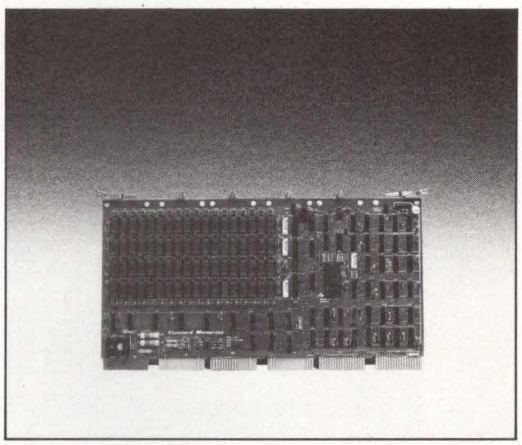
Experimenter's Kit Demonstrates Basics of Fiber Optic Data Links

To introduce basic characteristics of electro-optical systems, experimenter's kit for fiber optic data links contains all necessary semiconductor devices and PC boards along with optical connectors and cables to build 6 TTL or CMOS compatible fiber optic data links. In the package are 72 semiconductor devices from Motorola Semiconductor including emitters, detectors, comparators, inverters, op amps, and transistors. 12 predrilled PC boards allow construction of 6 transmitters, 2 10k-bit receivers, 2 100/1k-bit receivers, and 2 1M-bit receivers, capable of operation at distances of up to 44 m at lower data rates. Optical interconnection components include a preterminated optical cable assembly with measured loss, along with 3 m of unterminated cable and sufficient Optimate fiber optic terminating components to produce 10 optical cable assemblies using most common sizes and types of cables. **AMP Inc,** Harrisburg, PA 17105.

Circle 202 on Inquiry Card

If you think of us only for core memory, think again.

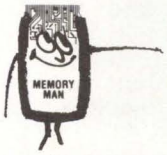




Introducing PINCOMM® PS. The New PDP-11 Semiconductor Memory from Standard Memories.

It's the first...with more on the way! PINCOMM PS is a 64K pin-compatible add-in memory for DEC PDP-11 minicomputers. Using 16K MOS memory chips, PINCOMM PS is available in depopulated versions of 48K, 32K and 16K. Features include 100 nsec write access, 350 nsec read access and 450 nsec cycle time. Plus, a parity option that eliminates the need for the DEC parity card, increasing CPU space and memory throughput.

Next in line...semiconductor memory for General Automation and Data General NOVA minicomputers. So start thinking of Standard Memories for your semiconductor needs, as well as core memory. We continue to provide a complete line of add-in and add-on core memory for Data General, DEC, General Automation, IBM and Interdata CPU models.



For an instant quotation call the Memory Man toll free: (800) 854-3792, (in California) (800) 432-7271.

Data General, DEC, General Automation, IBM and Interdata are recognized registered trademarks.

STANDARD MEMORIES
has grown into a new name

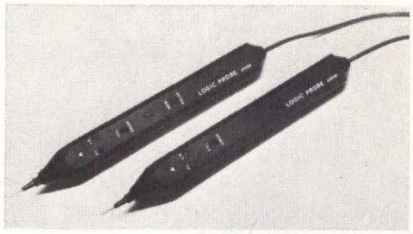
Applied Magnetics Trendata

3400 West Segerstrom Ave.,
Santa Ana, CA 92704. (714) 540-3605

CIRCLE 113 ON INQUIRY CARD

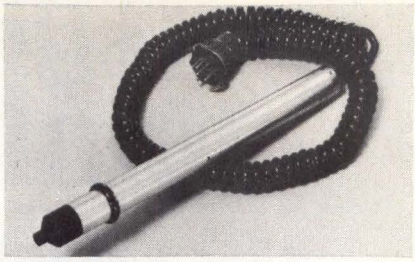
PRODUCTS

TTL/DTL AND CMOS TEST PROBES



Probes provide dual LED indication of logic states for TTL/DTL and CMOS circuits, with separate LEDs indicating high and low logic levels. Model 3100A has pulse stretcher function to capture single-shot pulses as short as 30 ns, and a memory function for latch storage of similar pulses. Model 3200A is similar but without memory and pulse stretching features. Both have clips for connection to power source and ground system of the circuit under test and high impedance data inputs to minimize loading effects. **Alco Electronic Products, Inc,** 1551 Osgood St, North Andover, MA 01845.
Circle 203 on Inquiry Card

LIGHTPEN



With electronics self-contained in pen body, the LP-600 operates from a single 5-Vdc supply at 80 mA and weighs 1.8 oz (50 g). It provides luminous sensitivity of 1 ft-L and has response time of <300 ns. Sensitivity is adjustable within the pen. Actuation is push tip, active low 0.4 Vdc max, sinking 4 mA. Touch switch or a combination of touch switch and push tip actuation are also available. **Information Control Corp,** 9610 Bellanca Ave, Los Angeles, CA 90045.
Circle 204 on Inquiry Card

OEM FIXED VOCABULARY SPEECH SYNTHESIZERS

Speech synthesizer circuit boards for small computer and OEM applications contain preprogrammed vocabulary data stored in 1 or 2 16k MOS ROMs. When provided with 6-bit parallel binary address code and start signal, LSI ROM controller fetches appropriate control data from ROM, determines speech characteristics of the word, and converts digital information to an analog signal via an onchip DAC. Result is a clear, intelligible male voice. A number of vocabulary choices are available. **Telesensory Systems, Inc,** 3408 Hillview Ave, PO Box 10099, Palo Alto, CA 94304.
Circle 205 on Inquiry Card

EPROM ERASING CABINET

C-90 industrial cabinet erases 1800 EPROMs/h. Measuring 36 x 26 x 10" (91 x 66 x 25 cm), the unit provides 15,000 $\mu W/cm^2$ of short-wave ultraviolet at the surface. There are 6 10 x 10" (25 x 25-cm) high intensity grid lamps for max UV output and ozone-free operation for personnel protection. A safety interlock device protects against accidental exposure to short-wave UV light. **Ultra-Violet Products, Inc,** 5100 Walnut Grove Ave, San Gabriel, CA 91778.
Circle 206 on Inquiry Card

See what you're missing... it's time to ask for a sample of "Vision One" quality image processing: the first choice of specialists.

Comtal is image processing.

By definition, an *image* is the digitally stored representation of the shape and shadings of objects, people or scenes. And, *processing* is the enhancement of brightness, color and definition of the image.

Printed reproductions cannot do justice to the quality of Vision One Image Processing Systems. To see what you're missing, send to Comtal for samples of Vision One image quality and standard interactive processing features.

Vision One is delivered ready to operate on digitized imagery without a host system/software development or time-consuming software installation or integration.

Vision One is an intelligent image processing system featuring real-time, completely operator interactive image processing for black and white or full 24-bit color (8 bits each of red, green and blue). Image resolution is 256x256, 512x512, or 1024x1024 pixels with internal solid state memory for up to fifteen 512x512 images (8-bit) and sixteen 512x512 graphic (1-bit) overlays.

Comtal is the acknowledged leader in digital image processing and offers the first commercial system with these features:

Real-time roam of multiple displays in very large data base memories (1977), stand-alone image processing systems, real-time small area independent color correction, and real-time convolution processing (1975). Also, 1024x1024, 256 shade soft-copy display image processing system (1974), full 24-bit color and digital image function and pseudo-color image processing (1973), with single standard digital interface for all features and options (1972).

Comtal has the only commercial systems with real-time operator interactive image processing and hardware generated display of image processing test patterns.

To get the full story on what Vision One image processing can offer you, write to COMTAL Image Processing Systems, P.O. Box 5087, Pasadena, California 91107 • (213) 793-2134 • TWX 910-588-3256

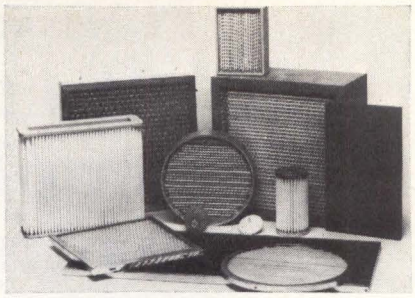
COMTAL®
IMAGE PROCESSING SYSTEMS

PRODUCTS

WIDEBAND MILLIVOLTMETER

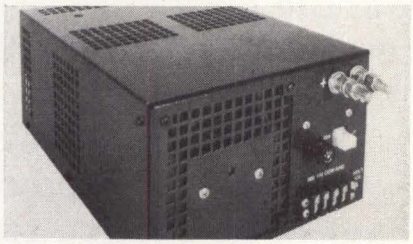
Sampling, rf millivoltmeter with high accuracy operates over a frequency range of 10 kHz to 1.5 GHz, and is usable as an indicator to 2 GHz. Model 9301A employs dual sampling process followed by rms conversion to give a true rms reading at all frequencies over voltage measuring range from 100 mV to 300 V. Intended for communications uses, it allows sinewave voltage measurements without input signal distortion. Also featured are low residual noise, and sample and hold facility. **Racal-Dana Instruments Inc,** 18912 Von Karman Ave, Irvine, CA 92715.
Circle 207 on Inquiry Card

OEM AIR FILTERS



For OEM use in disc drives, power supplies, mainframe computers, tape drives, and related equipment, air filters offer range of filtration capabilities. Low efficiency prefilters with min operating pressure drops are 50 to 80% effective on test dust. Prefilters provide max air flow and many meet military specs. Used in disc drive memories, filters feature Winchester technology. **Aluminum Filter Co,** PO Box 1311, Santa Barbara, CA 93102.
Circle 208 on Inquiry Card

1-kW SWITCHER



SW-1 series supplies, available in 2-, 5-, 12-, 15-, 24-, and 28-V models, deliver up to 300 A or 1 kW of continuous power, with up to 84% efficiency. Units utilize 20-kHz switching regulation and advanced LSI techniques and feature low parts count. Power supplies have forced-air cooling for high density packaging, MTBF of >60k h and MTTR of 6 min. Units are rated to full output in ambients of up to 50°C and feature a min hold-up time of 30 ms. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 209 on Inquiry Card

HIGH RESOLUTION CRT DISPLAY

Model 384 25" (63.5-cm) color television display operates at horizontal rates up to 34 kHz, allowing 1024 x 1024 pixel computer generated images to be displayed at a 30-Hz frame rate. The 384 can also display 1024 x 512 pixel graphics at a non-flicker refresh rate of 60 Hz. Analog computing circuits calculate convergence, dynamic blue lateral, dynamic focus, and raster geometry. Current feedback amps compensate for all external effects to assure long-term convergence stability. **Systems Research Laboratories, Inc,** 2800 Indian Ripple Rd, Dayton, OH 45440.
Circle 210 on Inquiry Card

INTRODUCING THE NEW COMPUTER THAT ISN'T.

The biggest problem with buying a new computer is that you have to buy a *new* computer. An untried, unproven computer.

The new Classic 7870, the newest member of the MODCOMP Classic family, solves that problem. Because it has all the performance features of the Classic 7860, which we introduced earlier this year. Except for one thing. It has four times the memory capacity.

With its large solid state memory (up to 2 million bytes) and an effective memory cycle time as low as 125 nanoseconds, it gives you the speed and capacity you need for demanding scientific, engineering and large process control applications.

And because the 7860 has already been tried and proven, the 7870 gives you something that no other new computer can offer you — a track record.

Classic beats DEC, Interdata, Prime and SEL.

In benchmark tests by computer users measuring both computational and I/O performance, the Classic 7860 has outperformed DEC's 11/70 and VAX. Interdata's 8/32. Prime's 400. And SEL's 32/75.

Hard to believe? Not really. Not when you consider some of the features we've built into the Classic.

Both the 7860 and 7870 have our unique multi-word (16-64 bit) architecture. Pipelined instruction processing. Our super fast floating point processor. And hardware instructions that are specifically designed for fast Fortran execution.

You don't have to trade reliability to get Classic's performance.

The best thing about the Classic isn't its performance. It's the fact that its state-of-the-art performance isn't achieved at the expense of reliability.

Since its introduction, the 7860 has been tested exhaustively by computer users in both scientific and process control applications.

They report that the Classic is as reliable as any computer MODCOMP has ever introduced. And that's saying something. Because independent surveys have consistently rated MODCOMP computers as the most reliable real-time systems on the market.

Why buy a new computer when you can buy our new computer?

The Classic is supported by a comprehensive set of operating systems and network extensions that have been used successfully by some of the most demanding computer users in the world. We also provide all the documentation you need to implement it quickly and easily. Plus a worldwide network of service specialists.

In fact, the only thing the new Classic 7870 doesn't give you is something you don't want anyway.

The problems associated with new computers.

For more information, send for our "MODCOMP Classic Family" brochure.

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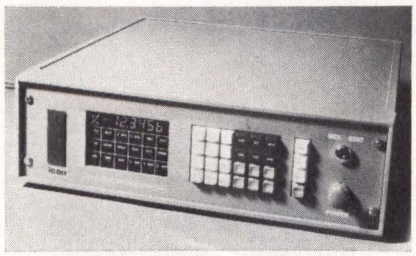
CIRCLE 117 ON INQUIRY CARD

PRODUCTS

MICROPROCESSOR BASED PROGRAMMABLE CONTROLLER



Applications involving open and closed loop drive systems, using stepping motors and servo motors, can be handled by the Universal Motion Control. Features include local and remote operation, 2k-char storage with 150-h battery backup, and oil tight front panel with edit lockout. Programs may be entered via keyboard, or via teletypewriter (tape recorder, etc) using an RS-232-C/TTY interface. Any program in the controller memory can be saved and stored external to the controller using the company's optional memory cartridge. **Icon Corp,** 156 Sixth St, Cambridge, MA 02143.

Circle 211 on Inquiry Card

DOT MATRIX IMPACT PRINTER

Standalone series DIP-40 printers contain all necessary electronics to interface directly with mini- and microcomputers. Print speed is 40 col at 50 char/s. Available options include parallel ASCII, serial RS-232-C interfaces, 20-mA TTY current loop, strappable 110- to 9600-baud rate, double width char printing, 120- to 200-char buffer storage, fast line feed, odd or even parity, and error detection feature. **Data Interfaces Inc,** 210 Lincoln St, Boston, MA 02111.

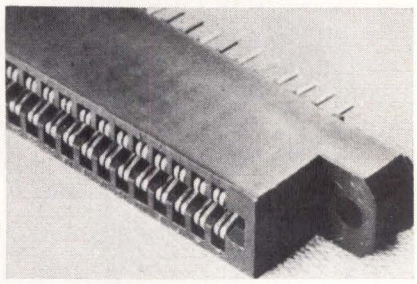
Circle 212 on Inquiry Card

LINE PRINTER CONTROLLER

Interfacing line printers to DEC's PDP-8 family, the LPC8 controller plugs directly into the Omnibus®. Onboard switches allow independent printer functions to be inverted, active true or active false, giving max flexibility to a large number of printers. Software compatibility between the LE8 and LA8 is accomplished by an onboard jumper. Device code is selected by means of a DIP switch. **Computer Extension Systems, Inc,** 17511 El Camino Real, Houston, TX 77058.

Circle 213 on Inquiry Card

PC TAIL EDGE CONNECTORS



Double-sided edge connectors meet stringent specs at cost savings. Model 6777 is on 0.100" (0.254 cm) contact and 0.200" (0.508 cm) row to row spacing; while the 6851 is on 0.125" (0.3175 cm) contact and 0.250" (0.635 cm) row to row spacing. Terminal is made of phosphorous bronze with selective gold contact area, with E-Z solder PC tail tinned. Contacts are rated at 3 A. Model 6777 is available in 10 through 70 circuit sizes while the 6851 is available in 6 through 50 circuit sizes. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.

Circle 214 on Inquiry Card

ROUND CONDUCTOR RIBBON CABLE

Manufactured on 0.050" (1.27-mm) centers to be compatible with all 0.050" (1.27-mm) insulation displacement connectors, as well as 0.038" (0.96-mm) centers for greater conductor density, GORE-FLEX™ cable is insulated with Teflon® PTFE and is manufactured with 28 AWG 19-strand high strength alloy conductors. It is capable of flexing a min of 50M times when subjected to an accelerated rolling flex of 130 cycles/min continuously at 0.75" (19.1-mm) radius. **W. L. Gore & Associates, Inc,** 1505 N Fourth St, Flagstaff, AZ 86002.

Circle 215 on Inquiry Card

MAGNETIC TAPE CONTROLLER FOR LSI-11

The TC-150 controller permits mixing of 7- and 9-track NRZ, PE, or dual-density tape units in any combination up to 8 units. It is software compatible with any system having DEC TM-11 support. Industry std tape drives, including those operating from 12.5 to 125 in (31.8 to 318 cm)/s, can be used. A Q-bus buffer allows remote installation in an expansion chassis up to 10 ft (3 m) away. **Western Peripherals Div, Wespercorp,** 1100 Claudina Pl, Anaheim, CA 92805.

Circle 216 on Inquiry Card

256k-BYTE SINGLE-BOARD ADD-IN MEMORY FOR NOVA 3

Supplying max addressable memory in one card slot, model NS D/3 for Nova 3 and 3/D computers, provides optional onboard error checking and correction circuits, error logger, and diagnostic panel. The 128k x 22-bit configuration uses 6 bits in each word for a Hamming code to identify single-bit errors, which are automatically corrected. Boards are also available in 128k x 17-bit even or odd parity, or 128k x 16-bit nonparity versions. ECC version has 450-ns access time and 600-ns cycle time. **National Semiconductor Corp, Computer Products Group,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

CARD GUIDE HEAT SINK

Kooler-Guide™, an assembly of series 1000 metal PC card guide and aluminum heat sink guide bar, offers exceptional heat dissipation since a large contact area is utilized for effective heat transfer. Guide bar and card guide assembly can be mounted with mounting clips at each end or bolted to chassis with integral stud, epoxied, or riveted directly to chassis. Both can be furnished to any specified length. **Unitrack Div, Calabro Plastics, Inc,** 8738 W Chester Pike, Upper Darby, PA 19082.

Circle 217 on Inquiry Card

COMPRESSED PRINT FOR LINE PRINTERS

Extended Logic A module (LAX) adds horizontally compressed char and multiple char set capability to Printronix model P-150 and P-300 line printers. Performing all std functions, the module replaces the Printronix Logic A. Horizontal print density can be changed to 16.67 char/in (6.6/cm) or 13.33 char/in (5.3/cm) by software command or an operator accessible switch. Up to 448 different printable char are offered. Self-test mode allows printer operation verification. **Trilog,** 17845 G Skypark Cir, Irvine, CA 92714.

Circle 218 on Inquiry Card

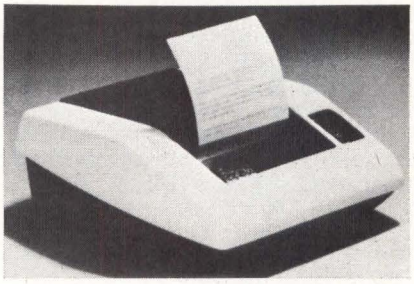
MULTIPROCESSOR SYSTEMS COMMUNICATIONS ADAPTER

With the high speed interprocessor communications system, up to 15 computers may communicate with each other. Blocks of data and program segments are transferred between processors at up to 1M bytes/s. System consists of several computers (each with adapter) and a communications bus. Available with all of the company's processors, the Multiprocessor Communications Adapter is compatible with that of Data General. **Rolm Corp,** 4900 Old Ironsides Dr, Santa Clara, CA 95050.

Circle 219 on Inquiry Card

PRODUCTS

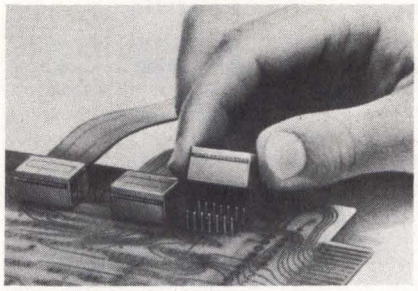
INTELLIGENT ELECTRO-SENSITIVE LINE PRINTERS



Three models including the EX-801P, which has a parallel ASCII input, -801S, with RS-232/20-mA serial input to 1200 bits/s, and -801H with serial input to 9600 bits/s, all operate at up to 160 char/s. Choice of 3 character sizes provide 80, 40, or 20 col on 5" (12.7-cm) wide electrosensitive paper. EX-801 printers feature multiline asynchronous input buffer, expandable to 2k char, permitting a CRT page dump in 1 s. 96-char ASCII is expandable to 256 char/s with user programmable fonts. **Axiom Corp,** 5932 San Fernando Rd, Glendale, CA 91201.
Circle 220 on Inquiry Card

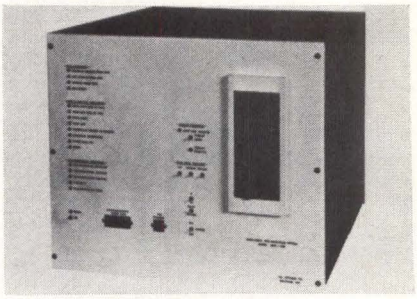
SOCKET CONNECTORS WITH PIN PROTECTION

Blue Macs® 14- and 16-position socket connectors are mass terminated to flat cable by inserting the cable into the connector opening and simultaneously crimping all conductors with a hand or bench tool. Self-aligning cable grooves position cable conductors over Tulip® beryllium copper contacts, assuring exact cable positioning. Mating contacts are enclosed in plastic housing to provide contact protection during repeated disconnect/reconnect cycles. **T&B/Ansley Corp,** 3208 Humboldt St, Los Angeles, CA 90031.



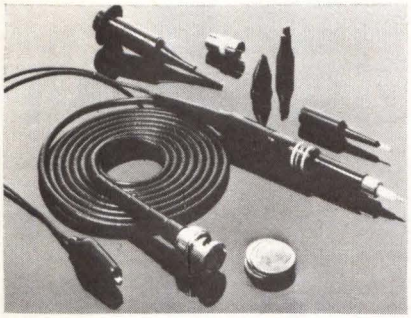
Circle 221 on Inquiry Card

MICROPROCESSOR BASED PAPER TAPE EMULATION SYSTEM



Expanding the programmability of PCB testers, numerical control, and other tape driven equipment, the ITMS-1 intelligent paper tape substitute floppy disc system with semiconductor buffer memory serves as a plug compatible replacement for paper tape readers. A diskette holds the equivalent of 5 48k-char paper tape programs. Excessive search and rewind time is eliminated. Std speed is 300/1200 char/s; up to 50 KC emulated tape speed is optional. **GSI Systems Corp,** 223 Crescent St, Waltham, MA 02154.
Circle 222 on Inquiry Card

PASSIVE PROBE

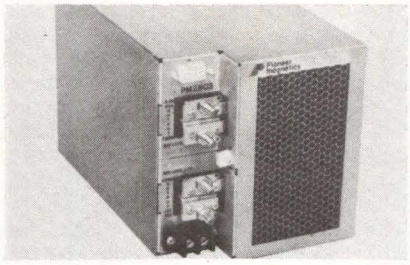


Model 4550 incorporates a 3-position slide switch in the head and has a cable length of 1.5 m. Optional accessories include insulating tip, sprung hook, trimmer tool, BNC adapter, and IC tip. Bandwidth is dc to 10 MHz in position X1, dc to 100 MHz in position X10. Other position X1 specs include input resistance of 1 MΩ, and input capacity of 40 pF plus oscilloscope capacity. Rise time is 3.5 ns for position X10. **ITT Pomona Electronics,** 1500 E Ninth St, Pomona, CA 91766.

Circle 223 on Inquiry Card

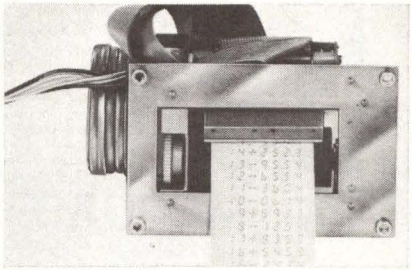
MULTIPLE OUTPUT SWITCHING POWER SUPPLY

PM2803 supply has power levels of up to 1150 W, providing regulated output at full load over input voltage ranges of 184 to 250 Vac. Extreme brownout protection is included; if input voltage fails entirely, output voltage holds up for a min of 30 ms to allow orderly system shutdown. Max power ratings of 3 output channels are 650, 500, and 300 W. Std output voltage channels are available from 2 to 48 V. Overload, short-circuit, and reverse voltage protection are std on each output. **Pioneer Magnetics, Inc,** 1745 Berkeley St, Santa Monica, CA 90404.



Circle 224 on Inquiry Card

THERMAL NUMERIC PRINTER MECHANISM

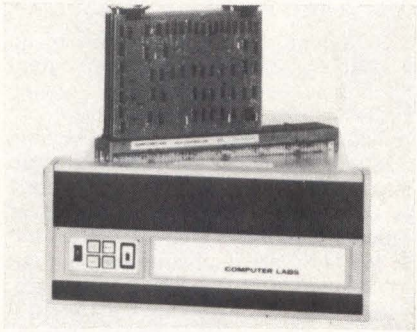


Fixed head, digital printer mechanism provides 7 col of 7-segment numbers, and plus/minus sign selectable in the first, second, or third col. Print rate is 4 lines/s. Paper tape drive is the only moving part. The need for ink supplies and ribbon mechanisms is eliminated. With the company's printhead, NP-7M produces essentially noiseless printing, using solid-state switching. **Gulton Industries, Inc, Measurement and Control Systems Div,** East Greenwich, RI 02818.

Circle 225 on Inquiry Card

PRODUCTS

20M-BYTE DISC MEMORY FOR PDP-11



A rapid access mass storage system, the M5104 disc memory is media (platter) compatible with the RK05 and completely compatible with all DEC software. 4-platter system provides user with the equivalent of 8 RK05's available online at all times with 20M bytes of storage capacity. Avg positioning time for a random move is 40 ms and transfer rate is claimed to be 40% faster than DEC's. Built-in address-defining switch allows user to reverse platter call-out. **Computer Labs, Inc,** 505 Edwardia Dr, Greensboro, NC 27409.
Circle 226 on Inquiry Card

132-COL CRT TERMINAL

Full line printer format can be displayed on the SMART ASCII terminal with up to 40 lines (4096 char) on its 15" (38-cm) CRT. Full u/lc ASCII char set is std. Special char can be designed using the font editor program. Keyboard is relegendable; foreign language fonts can be implemented. Communication is via an RS-232 line for direct hookup, or remote use via dialup lines with keyboard selectable baud rates from 110 to 9600. **ECD Corp,** 196 Broadway, Cambridge, MA 02139.
Circle 227 on Inquiry Card

MINIATURE PCB RELAYS

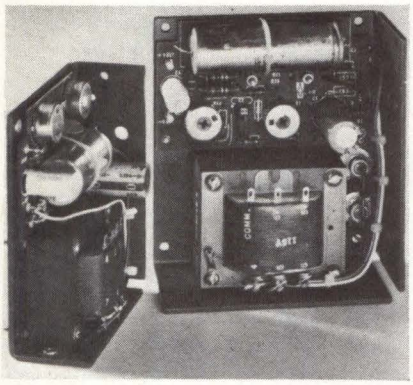
FBR 111 spdt (1 form C) relays have load handling capability of 3 A at 28 Vdc or 3 A at 120 Vac resistive, and coil power dissipation of 360 mW. FBR 211 relays feature high component density and have load handling capabilities of 1 A at 24 Vdc or 0.5 A at 100 Vac resistive. 221 series are identical to 211 models except for a dpdt (2 form C) contact arrangement. 321 series handle 3 A at 24 Vdc or 3 A at 100 Vac resistive; and have dpdt contacts. **Fujitsu America, Inc, Component Sales Div,** 910 Sherwood Dr, Lake Bluff, IL 60044.
Circle 228 on Inquiry Card

PRODUCTS

FIBER OPTIC EMITTER DRIVERS

Fibercom[R] series of fiber optic emitter drivers (FEDs) are encapsulated in 0.4" (1.02-cm) high 24-pin DIPs. A complete TTL compatible fiber optic transmitter can be configured by addition of an emitter or emitter assembly and a 5-V power supply. Driver has internally limited 100-mA drive current which may be externally adjusted for any drive up to 300 mA. Electrical rise and fall times are typically 15 and 5 ns, respectively. -2D, -3D, and -4D modules supplement series. **Radiation Devices Co, Inc,** PO Box 8450, Baltimore, MD 21234.
Circle 229 on Inquiry Card

OPEN FRAME DC POWER SUPPLIES



In addition to ±0.1% line and load regulation, 4 models of series SPE supplies provide outputs of 5, 12, or 15 Vdc. Tempco is 0.03%/°C; ac input is 115 Vac ±10%, 1 phase, 60 Hz ±3 Hz; and ripple is 1 mV rms. Thermal current limiting is built-in. Adjustable output is ±5%. Chassis weight is approx 2.4 lb (1.09 kg). Units measure 4 x 4.8 x 2.1" (10 x 12.2 x 5.3 cm). **Standard Power, Inc,** 1400 S Village Way, Santa Ana, CA 92705.
Circle 230 on Inquiry Card

HIGH RESOLUTION 20" CRT MONITOR

A high density CRT display module, the HRD-20, uses a 20" (50.8-cm) CRT to display full pages of text or graphic data. With a bandwidth of 105 MHz, the noninterlaced system scans at 50k scan lines/s. Dot resolution is rated at 0.01" (0.025 cm) with clear definition; rise/fall time is <3 ns. Std phosphor is P-4. Geared for document retrieval, text processing, and graphics applications, screen is human engineered for 8 h/day use without eyestrain. **CPT Corp,** 1001 Second St S, Hopkins, MN 55343.
Circle 231 on Inquiry Card

FLOPPY DISC DRIVES

Shugart compatible FDD 100-8 series offers both single- (3.2M bits/side) and double-density (6.4M bits/side) format on a removable 8" (20-cm) diskette using MFM encoding. Anticrunch media insertion, cooler operation at the recording surface, 85% commonality of parts between single- and dual-head drives, and double-density recording without additional prewrite compensation are featured. IBM compatible units read and write IBM 3740 formatted diskettes for up to 1.9M bits. **Siemens Corp, OEM Div,** 1440 Allec St, Anaheim, CA 92805.
Circle 232 on Inquiry Card

MOS MEMORY WITH ERROR CORRECTING CODE

Add-in memory system for DEC PDP-11 Unibus computers features single-bit error correction, and double and multiple bit error detection. PM-S11E requires only 2 DEC hex SPC backplane slots for mounting. It can be used with parity or nonparity operating systems, and is compatible with DEC hardware and software. It offers 256k bytes of memory std, and is also available in depopulated versions of 64k, 128k, and 196k bytes. **Plessey Peripheral Systems,** 17466 Daimler Ave, Irvine, CA 92714.
Circle 233 on Inquiry Card

EMBEDDED CARTRIDGE DISC CONTROLLER FOR LSI-11

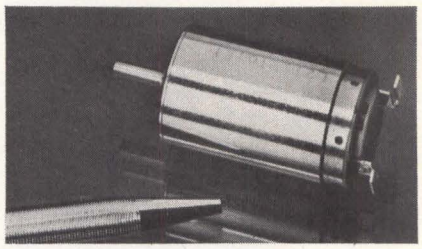
Single PC board PF-LSI-RK plugs directly into any quad LSI-11 Q-bus, and can be directly cabled to up to 4 industry std disc drives via a company disc personality card. Formatter and coupler are included in the module. Controller accommodates single and multiplatter disc drives: 1 to 4 2.5M- or 5M-byte drives, 1 or 2 10M-byte drives, or 1 20M-byte drive without modification to DEC distributed operating systems. **Pentron, Inc,** 1616 S Lyons St, Santa Ana, CA 92705.
Circle 234 on Inquiry Card

VIDEO INTERFACE BOARDS WITH PROTECTED FIELDS

CRT-2000 and -3000 are available in 50 and 60 Hz, and with user definable character sets. Both 16-line x 64-char interface boards include a 1k x 7 RAM, 64 x 7 x 5 row scan character generator, and SF.F 96364 CRT processor, in addition to supplementary logic. They accept data and control codes at TTL levels in ANSI std ASCII, and provide a composite video output which can be directly connected to any std CRT monitor. The -3000 also provides screen read. **Nucleonic Products Co,** 6660 Variel Ave, Canoga Park, CA 91303.
Circle 235 on Inquiry Card

PRODUCTS

HEAVY DUTY MICROMOTOR



Units suited to servo systems and other precision drive uses feature max efficiency ratings from 72 to 77% and avg no-load current ratings from 40 mA on the 4.5-V motor to 14 mA on the 15-V motor. With low moment of inertia, ironless rotor motor measures 23 mm in dia and 33.8 mm in length. Cylindrical skew-wound coil tolerates max of 100 °C. Available voltages are 4.5, 6, 9, 12, and 15. Power outputs for most models are 3 W. **Portescap U.S.,** 730 Fifth Ave, New York, NY 10019.
Circle 236 on Inquiry Card

BCD COMPATIBLE 4½-DIGIT DPM

Features of the AN2574 digital panel instrument include high impedance (1000 MΩ) differential input, autozero, autopolarity, 0.005% resolution, accuracy of ±0.01% of reading ±1 count, and 100- or 10-μV sensitivity. Universal power supply provides 110- or 220-Vac (±20%) operation and up to 1400-Vdc or ac peak isolation. A 5-Vdc logic powered unit is optional. DIN/NEMA packaged unit has 0.43" (1.09-cm) high LED display. Word programmable, 3-state, BCD output option allows data to be multiplexed onto a data bus in 4-, 8-, 12-, 16-, or 20-bit words. **Analogic Corp,** Audubon Rd, Wakefield, MA 01880.
Circle 237 on Inquiry Card

DMA ANALOG I/O BOARD FOR PDP-11

Access to 64 single-ended or 32 differential signal channels, with DMA data bursts of up to 45k samples/s is possible with the ST-PDP2D1C5 card that plugs directly into the block connector in the PDP-11 and interfaces to its Unibus electrical pinout. Paper tape diagnostic programs are included. The 12-bit A-D DMA card has max throughput of 20 μs, acquisition time of 12 μs, and conversion time of 8 μs. Aperture time is 50 ns, max feedthrough is 0.01%, and off-channel multiplex crosstalk is 0.01% at 1 kHz. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.
Circle 238 on Inquiry Card

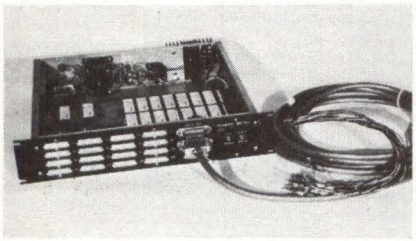
LOW COST PICOAMMETER

Model 480 picoammeter measures currents with 1 pA resolution. Input voltage drop of <0.2 mV, which is constrained by feedback techniques, does not disturb circuit under test. Unit measures current from 1 pA/digit (2 nA full range) to 2 mA, with 3½-digit precision. Input is connected into the circuit, appropriate range selected, and current read from digital display. High common-mode rejection and floating input permit in-circuit measurements. **Keithley Instruments, Inc,** 28776 Aurora Rd, Cleveland, OH 44139.
Circle 239 on Inquiry Card

PLOTTER CONTROLLER FOR TERMINET WORKSTATIONS

TermiNet III workstations and 9600 communications controllers can become plotting stations with the Complot® BTC-7/340. The microprocessor based system operates in incremental or vector/symbol mode. Controller determines whether data are a plot code or data for the line printer. Plotting codes generate pen commands for driving any Complot plotter at full capability. Host computer software support is available for the GE Mark III/RPS111 high speed service. **Houston Instrument,** One Houston Sq, Austin, TX 78753.
Circle 240 on Inquiry Card

SERIAL COMMUNICATIONS LINE SWITCH



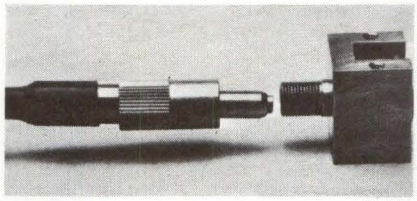
For redundant processor applications, the general purpose TS01 is a rack mountable, 16-channel terminal switch that functions as a 32-pole, double throw reed relay switch controlled by primary or secondary processors, or by front panel mounted switches in manual mode. Front panel LED indicators continuously monitor the processor controlling the switch. Primarily for DEC PDP-11 series computers, the device reverts to system A processor upon initialization or loss of power. **Pichler Associates,** 410 Great Rd, Littleton, MA 01460.
Circle 241 on Inquiry Card

FULL DUPLEX DATA SETS

T108D and E are originate-only and answer-only data sets providing 0 to 300-bit/s asynchronous data transmission over 2- or 4-wire private line facilities. Data sets are end to end compatible with Bell 108 series. Sets utilize single-card LSI technology and feature front panel diagnostic LED status indicators, which help to provide rapid fault isolation. Test capabilities for system's data sets, data lines, and terminal interfaces include analog and digital loopback, and self-test. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20907.
Circle 242 on Inquiry Card

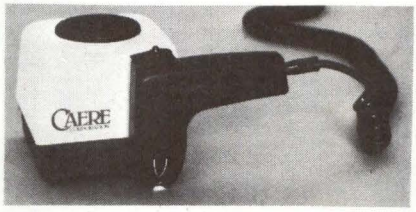
INTERCONNECTING HARDWARE FOR OPTICAL CABLES

Cable terminations, inline connectors, and source/detector receptacles are interchangeable and intermateable interconnecting elements. All hardware is compatible with the company's optical cables; precision alignment is assured.



Without the need for index-matching fluid, the copper-zinc-nickel alloy components provide low, reproducible coupling losses after repeated matings under normal environments. Typ insertion loss is <1 dB. **Siecor Optical Cables, Inc,** 631 Miracle Mile, Horseheads, NY 14845.
Circle 243 on Inquiry Card

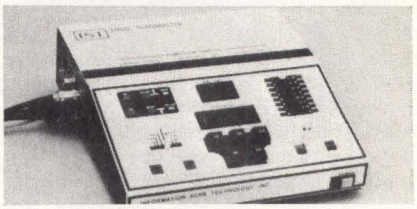
OCR SYSTEM FOR MULTIPLE DATA ENTRY



Series 700 optical character recognition system features set of Guidelights™ situated on both sides of removable nose cone. Light emanates from 2 apertures centrally located behind 0.4" (1.02-cm) vertical read window. Beams of light are visible under ambient light conditions and assist operator in accurately positioning and tracking across line of characters. Wands carry a 10' (3.05 m) retractile cable. **Caere Corp,** 345 E Middlefield Rd, Mountain View, CA 94043.
Circle 244 on Inquiry Card

PRODUCTS

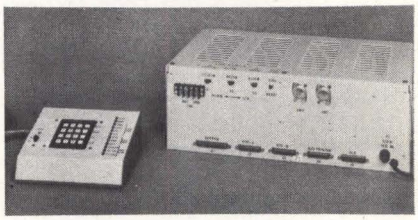
HIGH SPEED LOGIC TROUBLESHOOTER



Model 5700B Scanmaster enables users to rapidly probe pins of IC modules by pushbuttons on its panel. Any desired pin can be probed in 1 s, without counting or making an individual connection to the pin. Panel switch enables user to select logic threshold for testing CMOS, TTL, HTL, RTL, and DTL families. While probing the pin, the unit simultaneously interfaces the signal on the pin under test to an external oscilloscope, counter, or other test instrument. **Information Scan Technology,** 1725-L Rogers Ave, San Jose, CA 95112.

Circle 245 on Inquiry Card

NETWORK CONTROL UNIT



Universal unit with P/ROM interfaces high speed data terminals and word processing machinery to most carrier and private switched networks. Control unit to terminal signaling level is EIA RS-232-C; model CU355 accommodates Western Union low level (±12 V) or EIA RS-232-C compatible modem on the network side. Features include alpha or numeric keypad, and field programmable message delivery verification and station identification capabilities. **Multiplex Communications, Inc,** 123 Marcus Blvd, Hauppauge, NY 11787.

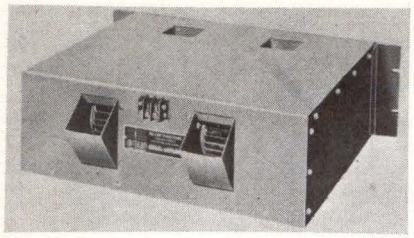
Circle 246 on Inquiry Card

CREDIT CARD READER

Credit cards may be read, edited, and written with the ANSI-std series RW-31 Creditloader™ credit card reader/writer when connected to a minicomputer or intelligent terminal. Configuration provides read-only operation on track 2 and R/W on track 3. Electronics employ an F8 microprocessor with ROM and RAM, full I/O buffering, and solid state motor control. **Vertel, Inc,** 125 Ellsworth St, Clifton, NJ 07012.

Circle 247 on Inquiry Card

MULTI-EXHAUST BLOWERS



Blowers feature vertical exhausts from front top center of blower and diagonally upward exhausts from rear of blower package. All units have std EIA notching. Motors are rust-resistant, double-shielded ball bearings per spec FF-13-171 and permanently lubricated with a −20 to 250 °F (−28 to 121 °C) lubricant. They meet spec CC-M-636A and are single phase, UL approved with 115 Vac, 50/60 Hz. **McLean Engineering Laboratories,** 70 Washington Rd, Princeton Junction, NJ 08550.
Circle 248 on Inquiry Card

MINICOMPUTER SOFTWARE SUPPORT PRODUCTS

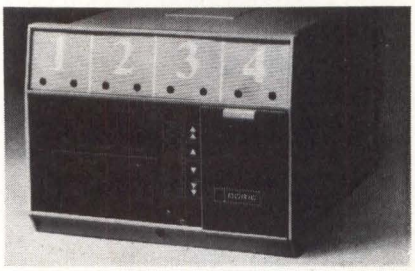
Business language capabilities of larger mainframe computers are supplied to the Eclipse C/330 and M/600 minicomputers with 5 software products. These include COBOL, RPG II, and Idea, a language tool which allows users to develop computer programs at TV-like terminals. With the additions, 30 users can work with a typ M/600 computer system employing different computer languages at the same time. **Data General Corp,** Rt 9, Westboro, MA 01581.
Circle 249 on Inquiry Card

AUTOMATIC DIGITAL PHASE-ANGLE METER

Model 305C/110 provides IEEE 488 bus compatibility, transferring measurement data and commands between the instrument and any minicomputer, calculator, or microcomputer system. Phase meter provides a 5-digit-plus-sign readout of phase angle and analog phase-angle outputs, ±0.01° resolution, ±0.03° accuracy, ±0.03° repeatability, and ±0.02° linearity. Setting of ac gain, selection of 1 of 5 output time constants, sensing of leading or lagging angle, and selection of angle range are all programmed by bus controller. **Dranetz Engineering Laboratories, Inc,** 2385 S Clinton Ave, South Plainfield, NJ 07080.
Circle 250 on Inquiry Card

PRODUCTS

MULTIPLE LOOP INDUSTRIAL CONTROLLERS



In 2- and 4-loop configurations, all with input, output, and control action selection on a per loop basis, Control:80 models handle field interchangeable inputs that include all common thermocouple types, RTD, millivolts, and process inputs. Plug-in outputs include relays and triacs rated at 2 A, 240 V, as well as voltage and current. User selected control action ranges from on/off through full PID control. Special capabilities include an alarm monitoring package with 8 field programmed alarm conditions. **Emerson Electric Co, Doric Scientific Div,** 3883 Ruffin Rd, San Diego, CA 92123.
Circle 251 on Inquiry Card

SIZE 23 FRAME SYNCHRO COMPONENTS

Control and torque transmitters, differential transmitters, torque receivers, and control transformers are each offered in 60- or 400-Hz models, all for 115 Vac. Synchros exhibit small angular errors of ≤8 min of arc. Residual voltage is typically <100 mV. The 400-Hz torque receivers develop a peak output of 290 g-cm at a displacement of 16° with a min gradient of 18 g-cm/deg. 60-Hz models have gradient of 8.6 g-cm/deg, but a higher peak of 475 g-cm at a displacement of 44°. **Muirhead-Vactric Div,** 1101 Bristol Rd, Mountainside, NJ 07092.
Circle 252 on Inquiry Card

RFI POWER LINE FILTERS

EP series filters bring switching type power supplies into compliance with VDE and proposed FCC specs and provide noise suppression. Filters furnish high insertion losses for both line to line and line to ground emissions throughout frequency range. Filters are UL recognized. Electrically, they have a max leakage current, each line to ground at 250 Vac, 50 Hz of 0.4 mA. Rated voltage is 115/250 Vac and rated current is 3 A at 115 Vac and 1.5 A at 250 Vac. **Corcom Inc,** 2635 N Kildare Ave, Chicago, IL 60639.
Circle 253 on Inquiry Card

16-BIT MINICOMPUTERS

ABLE/20, 40, 60, and 80 series computers are 16-bit machines organized around 16 registers. Operation is asynchronous with an avg execution time of 200 to 300 ns. The line is based on a single CPU configured on 2 4.5 x 7" (11.4 x 17.8-cm) boards. EZbus™ structure is comprised of 3 main buses. Data transfers take place through a 16-bit bidirectional data bus and 8-bit address/instruction bus; a 16-bit memory address bus handles memory addressing. **New England Digital Corp,** PO Box 305, Norwich, VT 05055.
Circle 254 on Inquiry Card

MULTIUSER OPERATING SYSTEM FOR PDP-11

Disc based XL/MU-11 operating system can be used on small PDP-11 configurations. For controlling realtime applications, the task scheduler supports simultaneous multitasking applications, task queuing, intertask communication, and locking or unlocking of resources. For program development, the system has system programs and utilities for editing, assembling, and linking. Up to 7 terminals conforming to std DEC DR11, DL11, or DC11 asynchronous interfaces can be supported. **Path Systems, Inc,** 333 N Turner St, Manchester, NH 03102.
Circle 255 on Inquiry Card

LED LOGIC STATUS INDICATORS

The 551 series indicator holds a T-1 LED in a 0.180 x 0.250 x 0.290" (0.457 x 0.635 x 0.737-cm) package. Lens of red, green, or yellow LED extends out 0.095" (0.24 cm) to provide a wide viewing angle. TTL, DTL, or RTL drives are possible, with typ operating characteristics of 1.6 to 2.4 Vdc and 20 mA, or 2.2 Vdc and 10 mA, depending on color, for 2.0 mcd luminous intensity. **Dialight, a North American Philips Co,** 203 Harrison Pl, Brooklyn, NY 11237.
Circle 256 on Inquiry Card

DYNAMIC RANDOM-ACCESS MEMORY BOARDS

Available in 32k- or 64k-byte versions, RAM III boards are designed for VDP desktop computers, and are S-100 bus compatible. During a normal CPU operation, refresh synchronizes to CPU timing so that refresh takes place when the CPU is not using memory. When the CPU is not running, an internal timer generates refresh requests every 6.6 μs. All boards have an access time of 375 ns and cycle time of 500 ns. **Imsai Manufacturing Corp,** 14860 Wicks Blvd, San Leandro, CA 94577.
Circle 257 on Inquiry Card

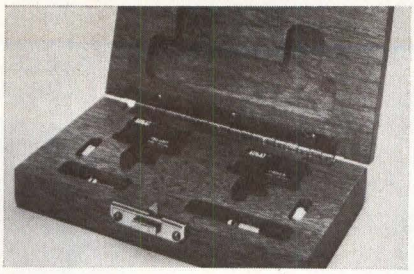
INCREASED CAPABILITIES FOR P/ROM PROGRAMMER

Programmers provide 32k-bits RAM, faster programming capabilities, and programming and device error detection tests which include sum-check and blank-check routines. Sum-check, the binary sum of all bits, is stored in an internal register when data are loaded into programmer. Then a sum-check is calculated on RAM data before all programming and after verification steps. Error is indicated here if they do not agree. Blank-check routine guards against a device that already contains data. **Data I/O Corp,** PO Box 308/1297 NW Mall, Issaquah, WA 98027.
Circle 258 on Inquiry Card

PRIMARY POWER SLIDE SWITCHES

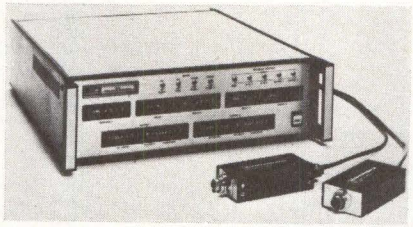
EPS1 and EPS2 are UL and CSA listed. Components with PC or solder lug terminals and 2-A, 250-Vac rating for switching of electrical and electronic equipment are available. Dpdt, 2-position, EPS1 series locking switches feature all-molded housing with mounting flanges, slotted actuators, 115 to 230 Vac legends, and choice of 4 terminal styles. Housings in EPS2 series have no mounting flanges, actuator shows legend for switch position selected, and short and long PC terminals are available. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.
Circle 259 on Inquiry Card

100-m FIBER OPTIC INTERCONNECTION SYSTEM



A powerful emitter assembly, temperature-referenced photodetector assembly, TTL compatible preamplifier, and TTL compatible emitter driver are incorporated in the 100-m system. Operating from dc to 5M bits/s, the system has a single fiber with strengthened cable construction. All cables feature ground and polished ends terminated with ferrules; connector elements use gold-plated brass construction. **Augat Inc,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.
Circle 260 on Inquiry Card

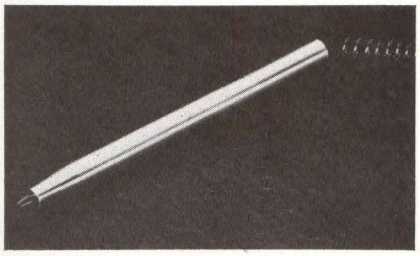
PROGRAMMABLE PULSE GENERATORS



Single-channel model 1505 and dual-channel 1506 feature 500-ps ECL pulse drivers and 3-ns timing. Output for each unit is located at end of an umbilical cord, which brings pulse directly to fixture that holds DUT. Both generators offer output amplitudes variable to $\pm$2.5 V into 50 Ω, with baseline offset variable to $\pm$1 V. In the 1506, 2 independent output channels utilize a common programmable frequency. Output amplitude, width, delay, and offset are independently adjustable for each channel. **EH International, Inc,** 515 Eleventh St, PO Box 1289, Oakland, CA 94604.
Circle 261 on Inquiry Card

0.5" DIA LIGHT PEN

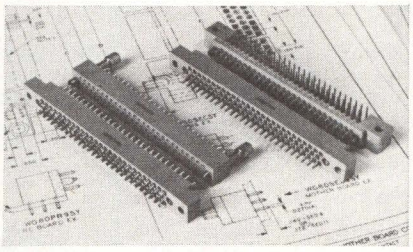
For CRT data manipulation, model 120 features stainless steel case which resists abrasion, corrosion, and discoloration. Package is 6" (15.2 cm) long and 0.5" (1.27 cm) in dia. Integral hybrid circuitry gives TTL level logic output. Pens require 5-Vdc power. Options include a noncoiled cord, alternate fields of view for special applications, and alternate spot brightness sensitivity which is factory preset to customer specs. **HEI, Inc,** Jonathan Industrial Ctr, Chaska, MN 55318.



Circle 262 on Inquiry Card

HIGH DENSITY PIN-TO-SOCKET CONNECTOR

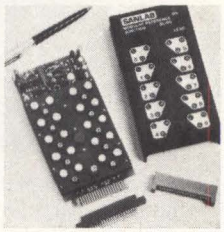
WF80 series connector compresses 80 contacts into a 3.5" (8.9-cm) long molded body featuring 3 rows, on 0.100" (0.254-cm) centers, 0.050" (0.127 cm) staggered. Various combinations of contacts, terminations, and polarizations are available for PC board to chassis or motherboard, PC board to cable, or chassis to cable applications. Connector is constructed of glass-filled diallyl phthalate body and gold-plated contacts. Performance conforms to MIL-C-55302. **AirBorn, Inc,** 4321 AirBorn Dr, Addison, TX 75001.



Circle 263 on Inquiry Card

PRODUCTS

MICROPROCESSOR COMPATIBLE REFERENCE JUNCTION



A precision isothermal thermometer which provides temperature information on 10 thermocouple wire termination pairs, SL101 combines a linear stable silicon thermometer bonded to a carefully designed thermal shunt. The module directly receives wire sizes to 14 AWG with shields and provides internal isothermal transition to copper conductors. Dimensions are 6.10 L x 3.14 W x 1.12" T (15.4 x 7.98 x 2.84 cm) with a choice of solder eye or ribbon cable edge connectors. The unit is factory calibrated and sealed and comes ready to bolt directly to data loggers, racks, and circuit cards. It is compatible with most data acquisition modules. Output sensitivity is 1 mV/°C, accurate to within 0.01 °C/°C, and stable to 0.001 °C/°C/yr. Power required is 20 mA max at ±15 V. **The San Diego Instrument Laboratory,** 7969 Engineer Rd, San Diego, CA 92111.
Circle 264 on Inquiry Card

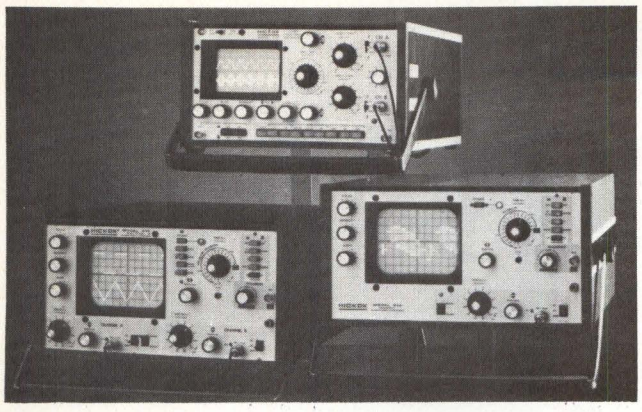
ADD-IN MEMORY FOR PDP-11

Offering up to 128k x 18 bits of high speed MOS main memory on a single std-size hex board, SuperSTOR-11 uses 16k dynamic RAM technology to enhance capabilities of DEC's PDP-11/04, /05, /34, /35, /40, /45, /55, and /60 minicomputers. Three features safeguard against total loss of memory and minimize downtime. 16k block substitution allows user to bypass a defective block (by use of jumper lines) and continue using remaining blocks of memory. A LED is illuminated when parity error originates in the memory board itself, giving immediate indication as to where the error is located. A power check LED on each board lights to indicate that memory is receiving the required power. **Cambridge Memories, Inc,** 360 Second Ave, Waltham, MA 02154.
Circle 265 on Inquiry Card

PORTABLE DATALOGGER

ML-10 has capability of logging 10 channels of analog data and 32 bits of digital data with realtime clock data on computer compatible magnetic tape. Input signal range of 0.1999, 1.999, 19.99, or 199.9 V is switch selectable. Front panel display reads time when not scanning, and shows digital and analog data during scan cycle. Scan control is either by switch selectable time intervals (10 s, 30 s, 1 min, 5 min, 10 min, 30 min, or 1 h), by external pulse control, or by manual pushbutton. A battery option will run the complete system including 8-char LCD readout for periods up to 30 days without recharging. Other options include RS-232 output to drive compatible equipment, such as printers and terminals. **A. D. Data Systems Inc,** 200 Commerce Dr, Rochester, NY 14623.
Circle 266 on Inquiry Card

PUSHBUTTON TRIGGERED OSCILLOSCOPES



Featuring automatic triggering, color-coded front panels, and conveniently grouped controls, model 532 is a dual trace 30-MHz scope with 11.7-ns risetime and built-in delay line for leading edge viewing of fast risetime pulses. Full time 4X expansion allows any portion of a pulse train up to 40 full divisions long to be viewed without use of a multiplier. Model 517 is a dual trace 15-MHz scope with 5-mV/cm sensitivity and reliable triggering up to 30 MHz. It features automatic selection of chopped or alternate operation in dual trace mode depending on sweep speed selected. The 515 offers most features of the 517 in a lower priced single trace version. TV sync separators are built-in for easy locking to complex TV video waveforms at any sweep speed. **The Hickok Electrical Instrument Co,** 10514 Dupont Ave, Cleveland, OH 44108.

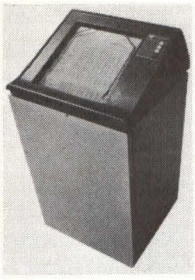
Circle 267 on Inquiry Card

FAST SCAN VIDEO DIGITIZER

Video digitization from std TV cameras in real time (0.0166 s/frame) can be accomplished with industrial quality interface which can be used for surveillance, robotics, inventory control, and pattern recognition, as well as for data transmission over phone lines when combined with a modem. Digitized picture is placed in computer main memory via the S-100 bus as a single operation using direct memory access. Horizontal resolution can be 64, 128, 256, or 512 picture elements/line and is easily varied using a DIP switch. Vertical resolution is also switch selectable. Max resolution is 512 pixels/line x 256 lines. Each pixel is encoded in 16 gray levels (4 bits/pixel). **Environmental Interfaces,** 23414 Greenlawn Ave, Cleveland, OH 44122.

Circle 268 on Inquiry Card

PRINTER/PLOTTER WITH IMPROVED CAPABILITIES

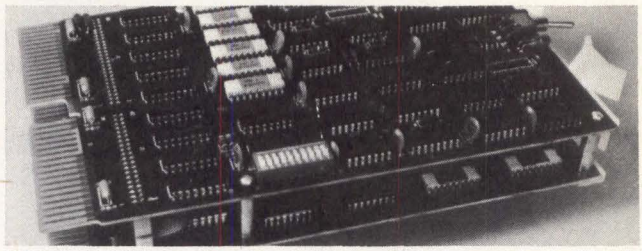


Enhanced with reconfigured backup electrode, ramp toning fountain, vacuum channel, additional toner pump, and Type S toner formulation, the 1200A provides printout and graphics output from any popular computer printing at 1000 lines/min with resolution of 200 dots/in (78.7/cm), darker, more consistent writing quality, and faster startup time. Optional software adds gray scale half tones. Optional controller allows hardcopy production from up to 8 display terminals. The unit prints 132-col lines on an 11 x 8.5″ (27.9 x 21.6 cm) roll or fanfold page at 1000 lines/min. Lines per page are adjustable from 1 to 72. It draws a 10.56″ (26.82 cm) wide plot at 1″ (2.54 cm)/s. Dual line buffer is std. **Versatec, a Xerox Co,** 2805 Bowers Ave, Santa Clara, CA 95051.

Circle 269 on Inquiry Card

PRODUCTS

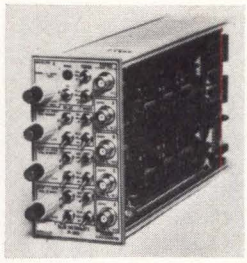
4K CACHE MEMORY FOR PDP-11



CACHE/434™ for the PDP-11/34 and /34A and Cache/440™ for -11/35 and /40 have buffer size of 8k bytes organized as 4k words x 16 bits of high speed bipolar memory. Byte parity is used to check data integrity. If parity error is detected, cache is automatically disabled, and only valid data from Unibus memory are sent to requesting device. Address parity validates addressing into cache. If an error occurs, cache behaves as if it has a byte parity error, and the system works without interruption. Upper and lower address limit switches let the user specify the exact operating range of the cache. Buffer memory can automatically detect the total address range of Unibus memory present within the system. Cache is contained on two dual wide boards designed to install in place of backplane interconnect module. **Able Computer Technology, Inc,** 1751 Langley Ave, Irvine, CA 92714.

Circle 270 on Inquiry Card

CLOCK GENERATOR FOR SSI/MSI TESTING



A 4-channel, 50-MHz clock generator that plugs into Tektronix TM-500 series power modules is designed for testing MSI, SSI, and other circuits requiring more than one input channel. Model PI-100A has 4 synchronized, 50-Ω outputs for driving TTL circuits and unterminated lines. It performs the equivalent timing and control functions of 4 conventional pulse generators in a single compact unit. Master clock A generates clock periods which are variable from 20 ns to 2 ms, and can be synchronously gated to produce pulse bursts. It can also be triggered from a single pulse to pulse repetition rates to 50 MHz. Outputs of channels B, C, and D can each be delayed from 10 ns to 1 ms with respect to that of A. **Pulse Instruments Co,** 1536 W 25th St, San Pedro, CA 90732.

Circle 271 on Inquiry Card

METAL-ON-SILICONE RUBBER CONNECTORS

Metal paths positioned precisely on a silicone rubber substrate form contact pads and interconnections for closely spaced electronic circuits. MOE (metal on elastomer) connectors based on this concept are of max benefit where close contact spacing, zero insertion force connection, easy assembly and disassembly, shock and vibration resistance, environmental seal, low profile, and potential for automated assembly are required. Paths and spaces between them are available as narrow as 0.002″ (0.051 mm). Paths are generally 0.0005″ (0.0127-mm) thick nickel, copper, gold, silver, or combinations. The silicone rubber base holds the metal paths in precise registration, provides the spring force necessary to maintain reliable contact, and forms a seal against contaminants. **Hulltronics Inc,** Hatboro, PA 19040.

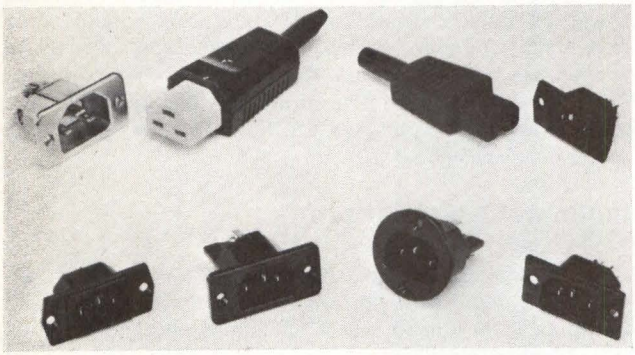
Circle 272 on Inquiry Card

KEYBOARD SEND/RECEIVE PRINTER

Model 3551 is capable of transmitting keyboarded data to a local or remote Datashare™ system or other host computer, while independently printing data received from its host at 80 or 160 char/s. Features include a dual separately controlled paper feed, automatic last character visibility, and choice of keyboard formats, printer speeds, and telecommunications signaling rates. Two integral keyboards are offered: one is std 3600 Datastation keyboard with 76 key positions, including a 10-key numeric data entry pad, shift/shift-lock functions and std ASCII alphanumeric char set with multikey rollover; the other is a keypunch-like arrangement. Unit prints at rates from 25 to 425 lines/min, depending on line length, using a 5 x 7 dot matrix impact printing technique and 96-char ASCII set to print lines of up to 132 char. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.

Circle 273 on Inquiry Card

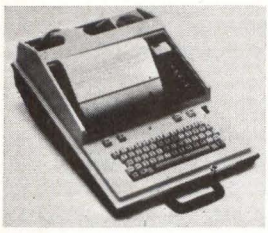
INTERNATIONAL POWER CORD RECEPTACLES



With recognition and approvals by UL, CSA, VDE, SEMKO, SEV, and other international safety testing laboratories, power cord receptacles allow the manufacturer to utilize just one receptacle for all production, simplifying the process of obtaining foreign approvals on the equipment. All receptacles conform to requirements of CEE publication 22. Use of a disconnectable power cord set makes it possible for equipment manufacturers to easily supply the appropriate power cord for each foreign country, thereby eliminating the necessity for users to modify the cord set before connection. All receptacles are rated for use to 250 Vac at currents of 6 or 10 A and at temperatures of 65 to 166 °C depending on type. **Panel Components Corp,** 2015 Second St, Berkeley, CA 94710.

Circle 274 on Inquiry Card

PORTABLE KEYBOARD SEND/RECEIVE TERMINAL



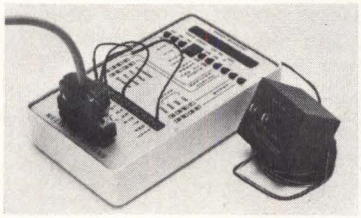
A lightweight, IBM 3275-compatible BSC printer/terminal, the em-t5 weighs 30 lb (13.5 kg) and is self-contained with keyboard, nonimpact printer, integrated 2400-baud synchronous modem, power supply, and bisync processor with 2k memory in a carrying case. Compatible with existing multipoint 3275 EBCDIC data base systems operated in a poll/select mode, it simulates the 3275 unformatted display mode, and is intended for inquiry/response applications. It also provides editing capabilities to facilitate data entry. Equipped with a fully buffered alphanumeric keyboard, its 10 embedded numeric keys are color coded for easy identification. Built-in diagnostics provide reliable operation. **NCR Corp, Terminal Systems Div,** 950 Danby Rd, Ithaca, NY 14850.

Circle 275 on Inquiry Card

PRODUCTS

MODEM PERFORMANCE ANALYZER

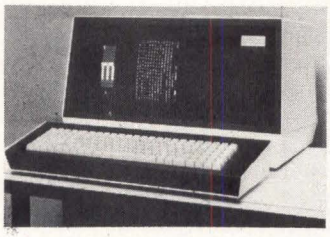
A handheld battery powered modem tester, the Modem-Microtest can be used to troubleshoot problems in transmission lines and in most modems and data sets, including Bell 103, 113, 202, 201, 208, and 209 type modems as well as modems up to 29k bits/s. The unit can internally generate 4 different data patterns including the std CCITT 511-bit pseudorandom pattern, and will detect, count, and display errors via its LED display window. Test points and display for various RS-232 interface voltages are provided as well as self-test capability, RTS and DTR control, force error, and operator controlled transmission. Power is supplied by a rechargeable NiCd battery which provides 24 h of continuous operation on a single charge. **Multi-Tech Systems, Inc,** 82 Second Ave SE, New Brighton, MN 55112.



Circle 276 on Inquiry Card

MICROPROCESSOR BASED INTELLIGENT TERMINAL

Basic 960 terminal consists of a 15″ (38.1-cm) screen, detachable keyboard with std layout, 9900 microprocessor with 256 words ROM primed with 2 bootstraps, 4k dynamic RAM store, realtime clock, and a buzzer mechanism to alert the operator to error conditions. Keyboard unit is completely programmable; ie, sensitivity may be programmed for n- or 2-key rollover. Std layout consists of 137 keys. CRT displays max of 24 lines of 80 char; however, column width and number of lines in screen/scroll buffer may be altered by operator. Terminal font consists of 256 shapes, accessed by 256 8-bit codes; char sets associated with codes may be altered on a 12-dot wide x 16-dot high matrix using font edit program. **Coltec Data Systems Ltd,** 13-19 Curtain Rd, London EC 2, England.



Circle 277 on Inquiry Card

SYNCHRONOUS MATRIX PRINTER TERMINALS

PRU1901 and TWU1901 use the company's VIP communications procedure, which provides poll and select capabilities that allow up to 32 units to be multidropped on a single communications line. PRU1901 is a receive-only printer in std configuration; an optional keyboard enables it to transmit as well. The interactive TWU1901 in addition has a typewriter-style keyboard for data entry and function commands, and can generate the full 128-char ASCII code set. Both models permit production of hardcopy reports at remote stations of a network, as well as within 300 m of the host processor. Std features include 132 print positions, horizontal and vertical tabs, multiple copy printing, self-contained print and carriage slew test routines, 960-char communications buffer, and selectable data transmission rates of 1200, 2400, and 4800 baud. **Honeywell Inc, Information Systems Group,** 200 Smith St, Waltham, MA 02154.

Circle 278 on Inquiry Card

LITERATURE

Control Loop Peripheral Devices

Guide 5300, a 6-p bulletin on 13 Unimod computing modules with microprocessor based logic, details design, application, and operational benefits, along with a functional block diagram. **Rochester Instrument Systems,** Rochester, NY.
Circle 300 on Inquiry Card

ECL Panels/Rack Assemblies

Dimensional diagrams and features are furnished in brochure on ECL panels, rack assemblies, and panel extenders which offer 4- and 5-layer construction with two ground planes on panels and extender control single impedance characteristics. **Mupac Corp,** Brockton, Mass.
Circle 301 on Inquiry Card

Rechargeable Batteries

Booklet includes color photos and descriptions of such industries as power tools, emergency and security products, microprocessors, and communications that are all served by rechargeable batteries. **General Electric Co, Battery Dept,** Gainesville, Fla.
Circle 302 on Inquiry Card

AC-DC and DC-DC Power Sources

General specs and dimensional drawings are included in 44-p reference guide on 24 power source families ranging from DIP dc-dc converters to 150-W line switching power supplies. **Semiconductor Circuits, Inc,** Haverhill, Mass.
Circle 303 on Inquiry Card

Video Display Terminals

Using keyboard photos with callout captions to describe operating and programming features, 8-p brochure gives specs and advantages of 7000 series terminals for text editing and large system environments. **Delta Data Systems Corp,** Cornwells Heights, Pa.
Circle 304 on Inquiry Card

Op Amps

Applications and technology of op amps, sample and holds, analog switches, multiplexers, and other BI-FET™ devices are contained in brochure along with data sheets and diagrams. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.

Test Instruments

Containing photos, specs, and applications, catalog depicts instruments such as oscilloscopes, frequency counters, digital and analog multimeters, and function and rf signal generators. **B&K-Precision, Dynascan Corp,** Chicago, Ill.
Circle 305 on Inquiry Card

LED Lamps

With tables and charts of optical, electrical, and dimensional characteristics, catalog includes std and high brightness LEDs; wide angle, short, and tapered lens; and low current and rectangular devices. **Chicago Miniature Lamp Works, General Instrument Corp,** Chicago, Ill.
Circle 306 on Inquiry Card

Data Acquisition Systems

Typical applications circuits for microprocessors, applications diagrams, and key specs are given for over 175 D-A and A-D converters in 24-p data conversion handbook. **Micro Networks Corp,** Worcester, Mass.
Circle 307 on Inquiry Card

Data Acquisition Components

Catalog contains tutorial sections and information on line of precision data acquisition components, data converters, signal conditioning components, temperature transducers, and digital panel meters. **Analog Devices, Inc,** Norwood, Mass.
Circle 308 on Inquiry Card

Solid-State Lightpens

Catalog on lightpens gives general characteristics and specs for models LP-210, -211, -316, and -500, all designed for symbol sensing, editing functions, and various graphics and displays. **Information Control Corp,** Los Angeles, Calif.
Circle 309 on Inquiry Card

Robot Control Systems

An Architecture for a Robot Hierarchical Control System presents advantages of applying computer controls to complex robot systems and provides documented listing of 3-level hierarchy control programs for a robot arm. Price is $4.25; stock no. 003-003-01874-1. **Superintendent of Documents, U.S. Gov't Printing Office,** Washington, DC 20402.

Solid-State Sensing

Pocket-sized glossary defines 463 electronic sensing and computer terms, and helps to clarify high level electronics language. **Honeywell Inc, Micro Switch Div,** Freeport, Ill.
Circle 310 on Inquiry Card

IC DIP Sockets

Complete specs, dimensions, and plating and material data are given for line of ICN series solder and wrap pin and ICL low profile solder sockets. **Robinson-Nugent, Inc,** New Albany, Ind.
Circle 311 on Inquiry Card

Circuitry Components

Connectors, terminals, switches, sockets, cable, headers, application tooling, and interconnection systems are portrayed in 4-color brochure. **Molex Inc,** Lisle, Ill.
Circle 312 on Inquiry Card

Subminiature Switches

With specs, PC layouts, and mounting information, catalog outlines subminiature and microminiature toggles, rockers, pushbuttons, and power switches. **C & K Components, Inc,** Watertown, Mass.
Circle 313 on Inquiry Card

Data Monitors

For monitoring and diagnosing fault conditions in data communications networks, Interview II™ standalone tool is profiled in 8-p brochure. **Atlantic Research Corp,** Alexandria, Va.
Circle 314 on Inquiry Card

Connector Tools

Descriptions, illustrations, and insertion and removal methods for line of connector contact insertion, removal, and crimping tools comprise 16-p catalog. **Jonard Industries Corp,** Tuckahoe, NY.
Circle 315 on Inquiry Card

Data Transmission Circuits

An addition to Bugbook® series, *BSR-6, NCR Data Communications Concepts* concentrates on properties and limitations of real transmission lines, and corrective techniques to optimize data transmission performance. Price is $6.95. **E&L Instruments, Inc,** 61 First St, Derby, CT 06418.

LITERATURE

Multichannel Communication System

Single-board computer with four serial I/O ports which can communicate asynchronously at 110 to 9600 baud or synchronously in excess of 50k baud is described in technical bulletin including a schematic diagram and circuit chart. **Control Logic, Inc,** Natick, Mass.
Circle 316 on Inquiry Card

Dot Matrix Printers

Folder on alphanumeric dot matrix impact printers for point-of-sale terminals, electronic cash registers, and other systems gives descriptions and features of five basic models. **LRC, Inc,** Burbank, Calif.
Circle 317 on Inquiry Card

Lightpens and Fixed Beam Systems

Brochure outlines specs of seven models of series 600 lightpen and fixed beam bar code reading systems featuring individual decoders and multiplexing systems. **Identicon Corp,** Franklin, Mass.
Circle 318 on Inquiry Card

Microprocessor Modems

Family of 9600-, 7200-, and 4800-bit/s modems available in single or multiport configurations are outlined in illustrated booklet comprised of technical data and features. **Racal-Milgo Information Systems, Inc,** Miami, Fla.
Circle 319 on Inquiry Card

Personal Calculators

Personal calculator digest includes articles on languages and programming as well as a catalog section providing background, accessories, functional explanations, specs, and software for calculator family. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 320 on Inquiry Card

Monolithic Converters

Data sheet describes 30-MHz, 8-bit A-D converter packaged in a 64-pin DIP and details with a schematic diagram the edge-connected, PC card that hosts this 2-W device. **TRW LSI Products,** Redondo Beach, Calif.
Circle 321 on Inquiry Card

Modular Multiplexing

Brochure points out system/component specs and general functions of electronic equipment used to interconnect central sensor based computers to industrial equipment. **Towne Applied Technology, Inc,** Buffalo, NY.
Circle 322 on Inquiry Card

Modular Power Supplies

Short-form catalog offers specs for dc-dc series L regulated converters, dc-dc series B miniconverters, dc-dc series D single-output converters, and ac-dc series T regulated miniature power supplies. **Wall Industries, Inc,** Bedford, Mass.
Circle 323 on Inquiry Card

Circular Plastic Connectors

Furnishing contact arrangements and specs, performance characteristics, and mated and component dimensions, 45-p catalog profiles circular plastic connectors available in three interconnection series. **AMP Inc,** Harrisburg, Pa.
Circle 324 on Inquiry Card

Photosensitive Devices

Dimensional outlines and spec charts as well as illustrations of measuring TV systems comprise 20-p catalog listing radiation detectors, photoconductive cells, infrared detectors, light sources, and image pickup tubes. **Hamamatsu Corp,** Middlesex, NJ.
Circle 325 on Inquiry Card

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

GUIDE TO PRODUCT INFORMATION

GUIDE TO PRODUCT INFORMATION

SALES OFFICES

NEW ENGLAND, NEW YORK STATE

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129 Cedar Hill Road
East Dennis, MA 02641
phone: (617) 385-2533

MIDDLE AND SOUTH ATLANTIC STATES

Hajar Assoc., Inc.
Emile H. Hajar
Paul Hajar
Silvio Mandino
521 5th Avenue
New York, NY 10017
phone: (212) 682-5844

MIDWESTERN STATES

Hajar Assoc., Inc.
Emile H. Hajar
Paul Hajar
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SOUTHWESTERN STATES

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WEST COAST STATES

Buckley Boris Assoc.
Terry Buckley—Tom Boris
John Sabo
912 South Barrington Avenue
Suite 202
Los Angeles, CA 90049
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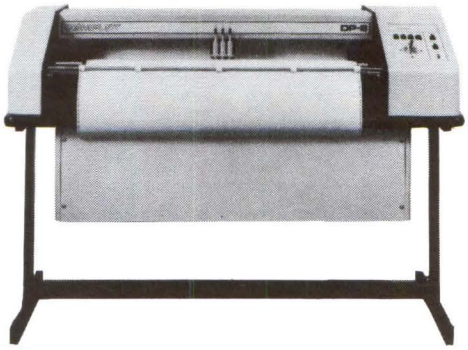
DP-8 in '78

The WIDE Plotter



CØMPLØT® DP-8

- One or 3 pens
- Speeds up to 4.5 IPS
- 6 switch selectable step sizes
- Optional paper widths
- Positive paper feed or optional roll take-up
- Prices from $7600*

*U S Domestic Price only

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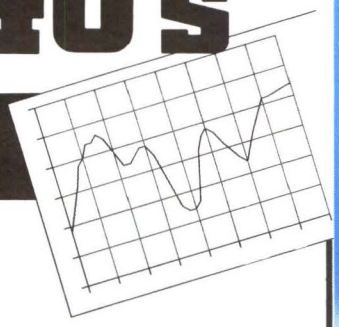
"the recorder company"

CIRCLE 146 ON INQUIRY CARD

CRT COPIER for 2640's

The new Model 8640 CRT copier provides hard copies from HP 2640 Series terminals

in less than 10 seconds



The Houston Instrument 8640 CRT copier, at $4495, provides you with permanent high quality hard copies from any HP 2640 Series terminal equipped with HP's video interface. Utilizing HI's electrostatic technologies, the Model 8640 produces permanent non-fading copies at about one third of the cost of comparable dry silver copies. The Model 8640 is the choice hard copy adjunct to your terminal.

- No warm up time
- Proven electrostatic printing technique for high contrast output and no fading
- Low operating noise
- Inherent high copying speed capability
- Provides copies from up to four terminals (with Model 8640A)
- Price for Model 8640, $4495* (Model 8640A $4995*)

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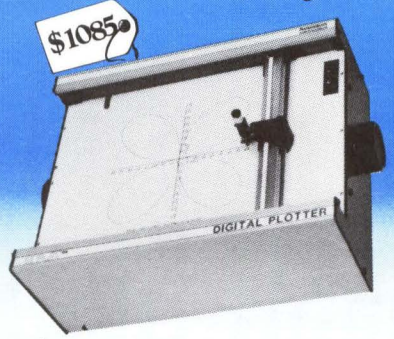

at a price you won't believe

Both serial and parallel inputs built-in

Uses standard 8½" x 11" paper

Plotting speed up to 2.4 inches per second

Resolution of both 0.01 and 0.005 inch

Baud rate and step size easily changed

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