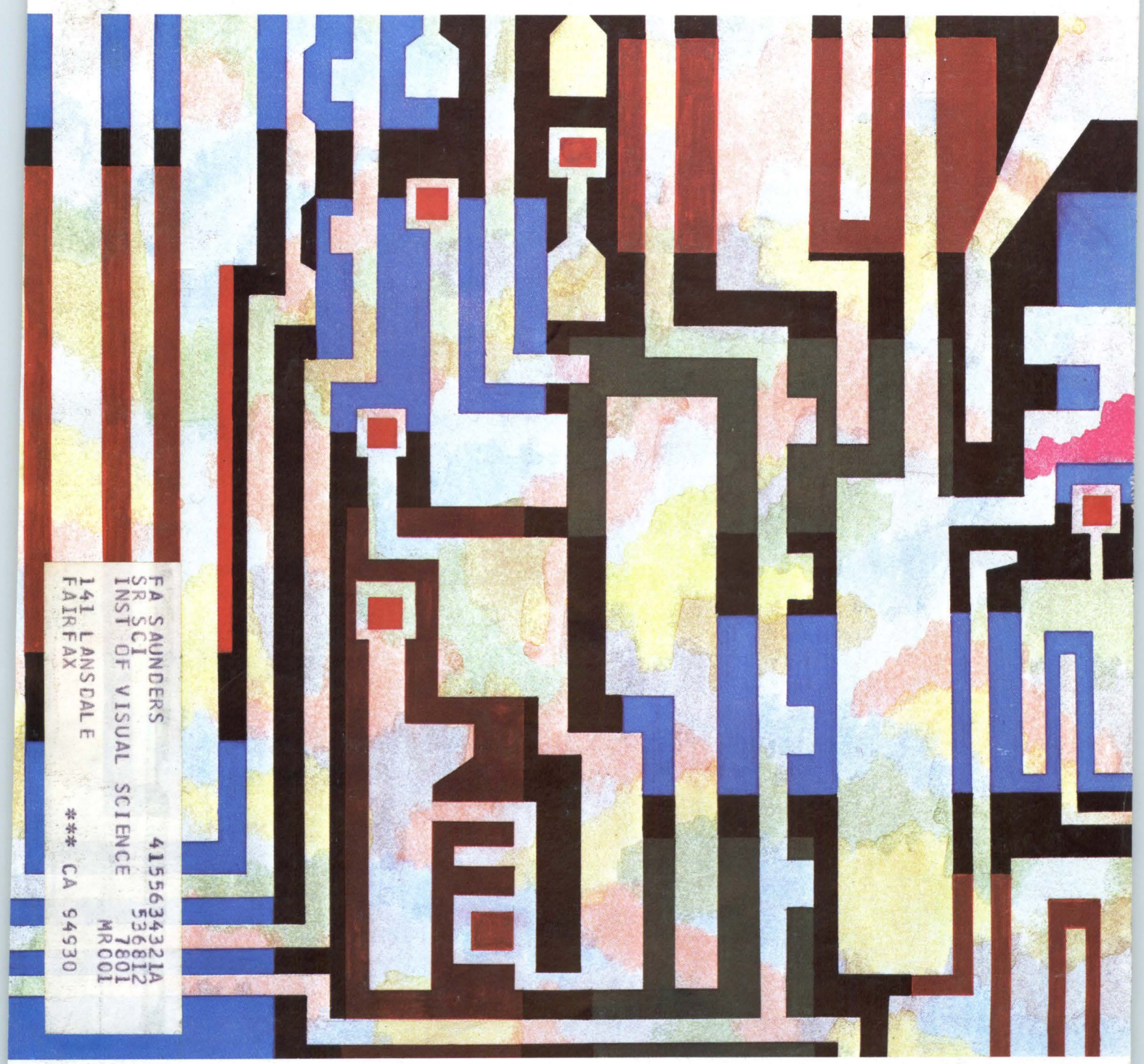
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

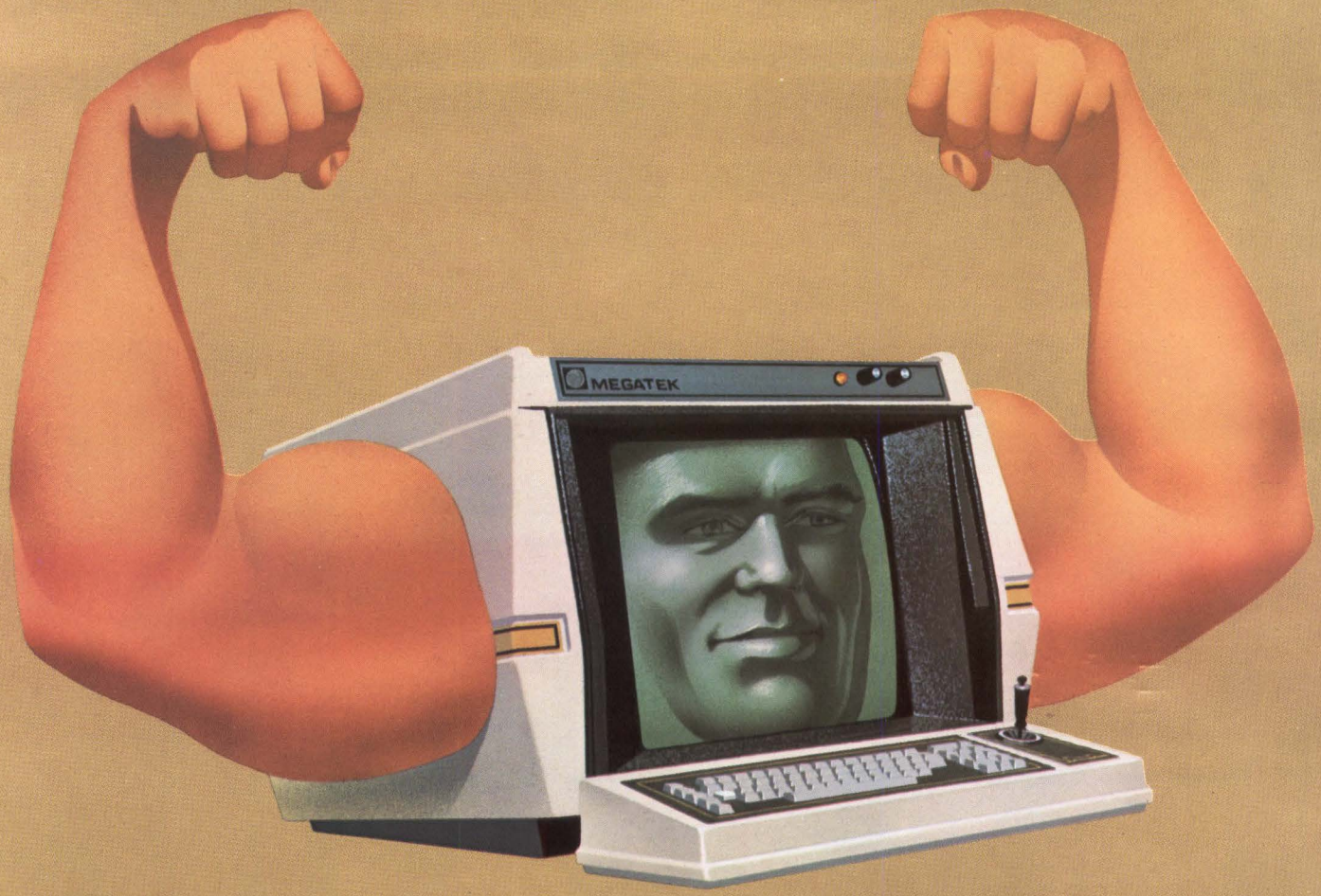
MARCH 1980



MULTIPROCESSING IMPROVES THROUGHPUT AND RESPONSE IN A VECTOR TO RASTER CONVERTER

LSI HARDWARE IMPLEMENTS SIGNAL PROCESSING ALGORITHMS

EMI SUSCEPTIBILITY TESTING OF COMPUTER SYSTEMS



All muscle and no fat.

Most refresh graphic systems are flabby. With lots of features you don't need. Without a few you do.

The MEGATEK 7000 is built lean. You get fast graphics throughput. A high resolution, real-time, interactive display. Complete system modularity. An unmatched refresh graphics system. At a price that makes sense.

A built-in 32-bit microcomputer with a 64K byte, 32-bit wide refresh memory, expandable to 128K. Lets you process graphics data fast. And, saves you host computer time. Add MEGATEK's advanced vector generator and you get unbeatable graphics throughput.

Vectors and characters are displayed instantly. With precision end point matching. And constant intensity. 12-bit resolution is standard. Vector quality that outclasses every other refresh system.

Easy-to-use real-time interactive graphics. Outstanding display

dynamics. Hardware translation, blink, dashed lines. Absolute and relative jump. All standard. And, hardware clip, rotate, scale, and zoom are available as well.

Plus, the MEGATEK 7000 is easy to look at. 16 levels of image intensity. 8 programmable character sizes. The screen is clear and readable, even in a brightly lit room. And, with selective erase, you don't have to blank the screen to change a vector or symbol.

Add a universal computer interface that connects to any host computer. Field-proven software that cuts system development cost. A full line of peripherals and accessories. Even color, if you need it. And, you have the most powerful refresh graphics terminal for your dollar on the market today.

But, don't take our word. Prove it to yourself. Call or write for a demonstration. And remember, the MEGATEK 7000 is backed by a national service network with fast, hot-line access.

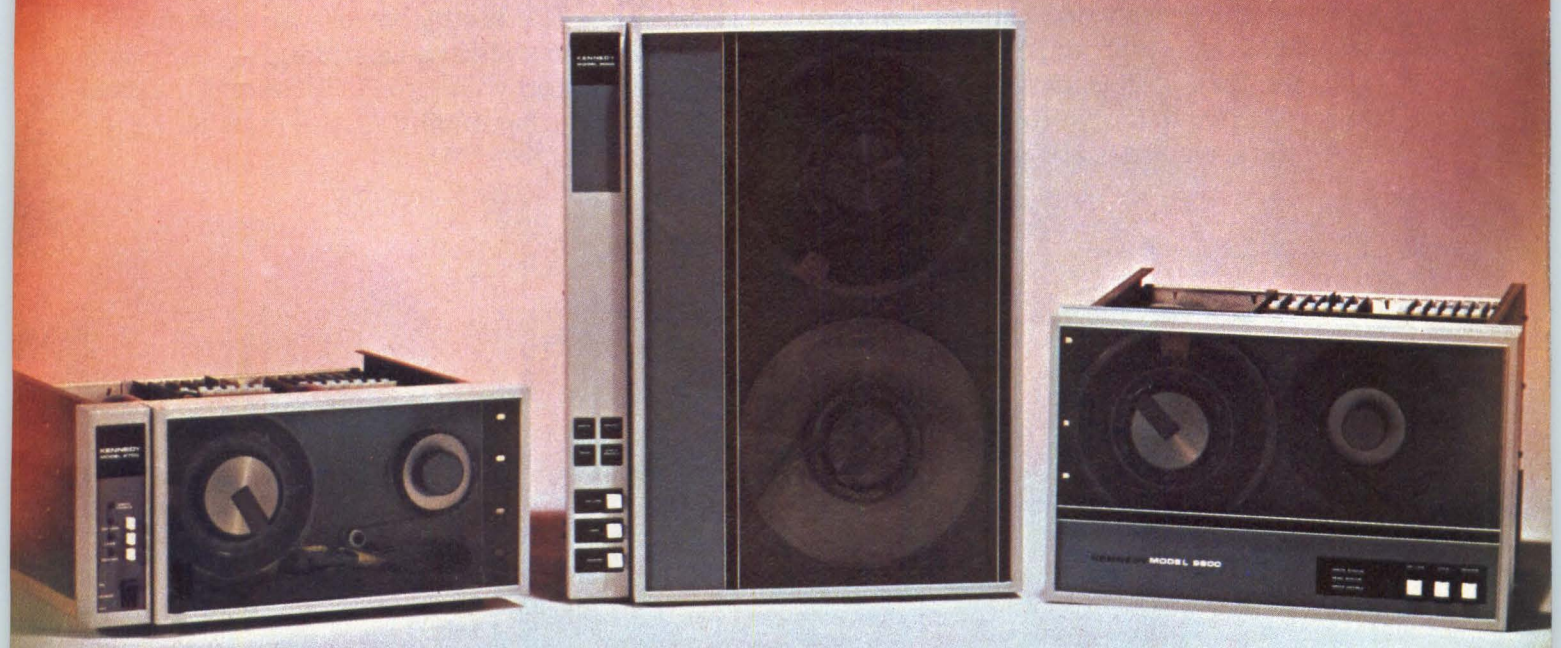
For full details, write or call Peter J. Shaw, MEGATEK, 3931 Sorrento Valley Blvd., San Diego, CA 92121. (714) 455-5590. TWX: 910-337-1270. (European office: 14, rue de l'Ancien Port. 1201 Geneva, Switzerland. Phone: (022) 32.97.20 Telex: 23343.)

The Visible Difference

MEGATEK CORPORATION

CIRCLE 1 ON INQUIRY CARD

Series 9000...
still the class act in digital tape transports.



Being the best in your business is neither boring, tiresome or repetitive—it's challenging. Now that we have the most dependable and advanced tape transports in the world—what's left?

Delivering them. On time and on-line faster than anyone. That's what! They still have all the features:

- A position arm anticipatory sensing system. An exclusive Kennedy feature, the linear, non-contact (Mag Pot) position sensor requires no lamp source and assures performance for the life of the machine.
- Interchangeable electronics on all Series 9000 transports, reduce stocking costs and down time.
- Front-accessible off-line test panel; marginal skew check; threshold scanning which automatically compensates for drop-ins or drop-outs; Read-After-Write shortened skew gate; simplified tape path and quick release hubs.
- All models are available with either 7 or 9 track, 800NRZ1, 1600 PE or 800/1600 NRZ1/PE.
- 7 and 9 track NRZ1 and PE format/control units to simplify customer electronics. Also, a variety of popular mini-computer mag tape controllers are available. Series 9000's performance is as impressive as its features, with data transfer rates to 72KHz, and tape speeds from 10 to 45 ips.

Being best is nice. So is being fast. Kennedy is both.

KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TWX 910-585-3249

CIRCLE 2 ON INQUIRY CARD

KENNEDY • QUALITY • COUNT ON IT

Yes, Tally is the best teleprinter!

Witness the Quick Tear that saves money by saving forms!

The Quick Tear option stops wasted forms, wasted money. It saves throughput time, operator time and customer time. Now you can remove a completed form after printing without wasting the next form. And for batch work, you can by-pass the quick tear assembly for continuous print runs.

Unique to Tally alone, the quick tear can accommodate variable width forms from 4 to 15 inches wide. The pin-feed tractors are adjustable from either side of the carriage. Print an original plus five sharp carbon copies. And Tally teleprinter operators give testimony to quieter operation, better key action and heftier construction.

The Quick Tear is only one of many valuable options available with the 1200 Baud T-1612 printer terminal. Contact your local Tally dealer for all the details. Tally Corporation, 8301 So. 180th St., Kent, WA 98031. (206) 251-5524.

TALLY®
PRINTERS
WORLDWIDE

Tally Corporation is a member of the Mannesmann Group.

CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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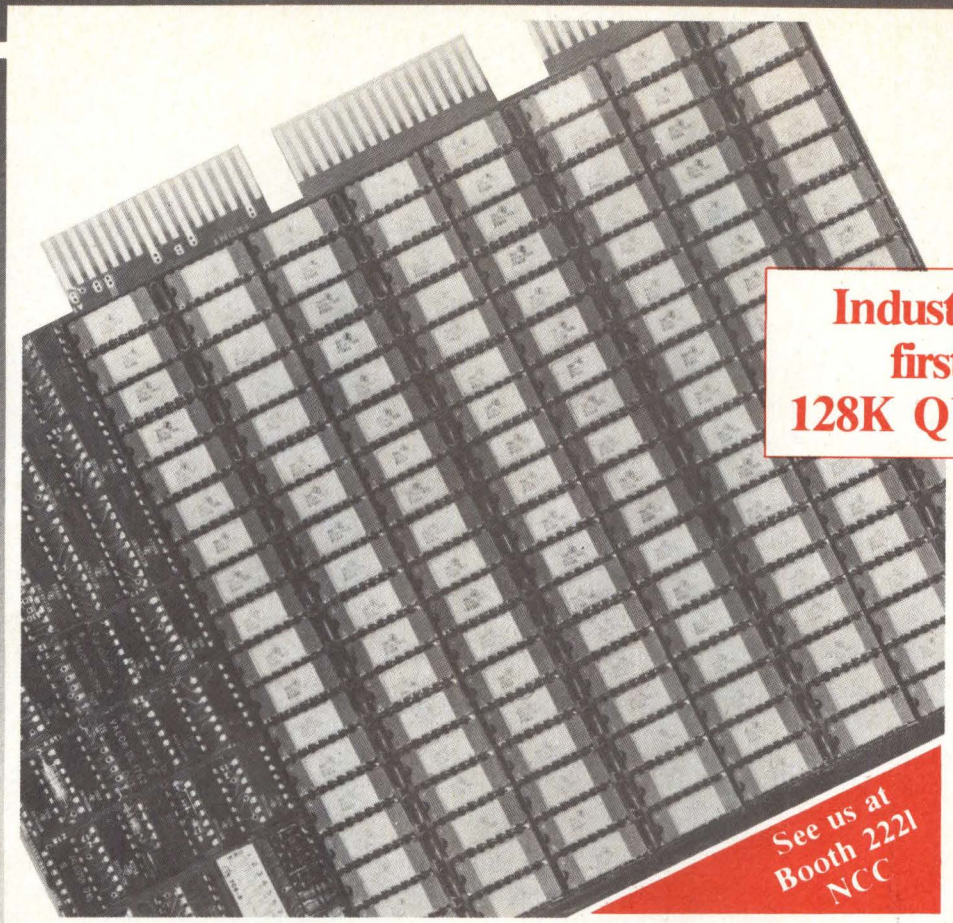

128K x 18 FOR LSI-11/23®

Dataram Corporation, first to offer a 128K x 18 single-board PDP®-11 ADD-IN, has done it again.

This time with an incredible 128K x 18 semiconductor ADD-IN for DEC®'s LSI-11/23!

This industry first, the DR-113S, is packaged on a standard DEC 8½" x 10" quad board. But more than just being a "first," the DR-113S is also a "best," saving you not only space and money, but also greatly reducing overhead circuitry, optimizing MTBF, and minimizing power consumption. And the DR-113S is also available in 64K and 96K configurations.

From Dataram Corporation, the people who provide everything you need to make a big thing out of the LSI-11 — • PDP-11/03L compatible chassis • 16K x 18 core ADD-IN • 32K x 18 semi ADD-IN (dual-size board) • BULK CORE/SEMI Disk Emulation Systems • BULK MINI • Tape and Disk Controllers • and even DEC-manufactured LSI-11 and LSI-11/23 microcomputers and other accessories.

☐ Please tell me more about Dataram 128K x 18 memory for my LSI-11/23 microcomputer.
☐ Please send me information about your other LSI-11 compatible products.
☐ Please have a salesman contact me.

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CIRCLE 5 ON INQUIRY CARD

CALENDAR

CONFERENCES

APR 8-10—Internat'l Reliability Physics Sym, Caesar's Palace, Las Vegas, Nev. INFORMATION: Glen T. Cheney, Bell Laboratories, 555 Union Blvd, Allentown, PA 18103. Tel: 215/439-7628

APR 21-24—Internat'l Magnetics Conf, Sheraton-Boston Hotel, Boston, Mass. INFORMATION: D. I. Gordon, Conf Chm, Naval Surface Weapons Ctr, White Oak, Silver Spring, MD 20910. Tel: 202/394-2167

APR 23-25—Workshop on Fault Tolerant VLSI Design, Santa Monica, Calif. INFORMATION: Daniel Siewiorek, Dept of Computer Science, Carnegie-Mellon U, Pittsburgh, PA 15213

APR 28—Invitational Computer Conf, Atlanta, Ga. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

APR 28-MAY 2—Society for Information Display Internat'l Sym, Town and Country Hotel, San Diego, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193

APR 30-MAY 2—Conf on Modeling and Simulation, Pittsburgh, Pa. INFORMATION: W. G. Vogt, Modeling and Simulation Conf, 348 Benedum Engineering Hall, U of Pittsburgh, Pittsburgh, PA 15261

MAY 1-2—An Assessment and Forecast of Computer Graphics, Stouffers Inn, Westchester, NY. INFORMATION: Bob Sanzo, Frost & Sullivan, Inc, 106 Fulton St, New York, NY 10038. Tel: 212/233-1080

MAY 6-8—Internat'l Sym on Computer Architecture, Casino, La Boule, France. INFORMATION: Jacques Lenfant, Irisa Campus de Beaulieu, 35042 Rennes, Cedex, France

MAY 13-15—ELECTRO, Boston-Sheraton/Hynes Auditorium, Boston, Mass. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

MAY 19-22—National Computer Conf, Anaheim, Calif. INFORMATION: AFIPS, 1815 N Lynn St, Suite 800, Arlington, VA 22209. Tel: 703/243-4100

MAY 20-22—CENCON '80 Industrial Electronics Conf, Public Auditorium Arena, Cleveland, Ohio. INFORMATION: Mike Lapine, Cleveland Electronics Conf, Inc, 2728 Euclid Ave, Cleveland, OH 44115. Tel: 216/241-5515

MAY 29—Computer Networks Protocol Sym, NBS, Gaithersburg, Md. INFORMATION: Helen M. Wood, Conf Chairperson, National Bureau of Standards, Washington, DC 20234. Tel: 301/921-2834

JUNE 2-5—Sym on Incremental Motion Control Systems and Devices, Ramada Inn, Champaign, Ill. INFORMATION: Incremental Motion Control Systems Soc, PO Box 2772, Station A, Champaign, IL 61820

JUNE 3-5—Networks '80, Bloomsbury Centre Hotel, London, England. INFORMATION: Online, Cleveland Rd, Uxbridge UB8 2DD, England

JUNE 3-5—Sym on Multiple-Valued Logic, Northwestern U, Evanston, Ill. INFORMATION: Jon T. Butler, Dept of Electrical Engineering and Computer Science, Northwestern U, Evanston, IL 60201. Tel: 312/492-5628

JUNE 8-11—Internat'l Conference on Communications, Red Lion Inn, Seattle, Wash. INFORMATION: ICC '80, PO Box 88465, Seattle, WA 98188

JUNE 10-12—Internat'l Input/Output Systems Sem, Stockholm Sheraton, Stockholm, Sweden. INFORMATION: Carroll A. Greathouse, Input/Output Systems Assoc, PO Box 1333, Stamford, CT 06904. Tel: 203/323-3143

JUNE 16-18—ATE Seminar/Exhibit, Hynes Auditorium, Boston, Mass. INFORMATION: ATE Seminar/Exhibit, c/o Benwill Publishing Corp, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

JUNE 17-19—Internat'l Microcomputers Minicomputers Microprocessors/ DATACOMM '80 Conf, Palais Des Expositions, Geneva, Switzerland. INFORMATION: Industrial & Scientific Conf Mgmt, Inc, 222 W Adams St, Chicago, IL 60606. Tel: 312/263-4866

JUNE 19—Computer System Integrity, Technical Sym of the ACM and NBS Institute for Computer Sciences and Technology, National Bureau of Standards, Gaithersburg, Md. INFORMATION: Angela Turvey, 4910 Butternut Dr, Rockville, MD 20853

JUNE 23-25—Design Automation Conf, Minneapolis, Minn. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JUNE 25-27—IFAC Sym on Large Scale Systems: Theory and Applications, Toulouse, France. INFORMATION: Symposium Secretariat, AFCET-156, Bd Péreire-75016 Paris, France

JULY 22-24—The 1980 Microcomputer Show and Internat'l Conf, Wembley Conf Ctr, London, England. INFORMATION: TMAC, 680 Beach St, Suite 428, San Francisco, CA 94109. Tel: 415/474-3000

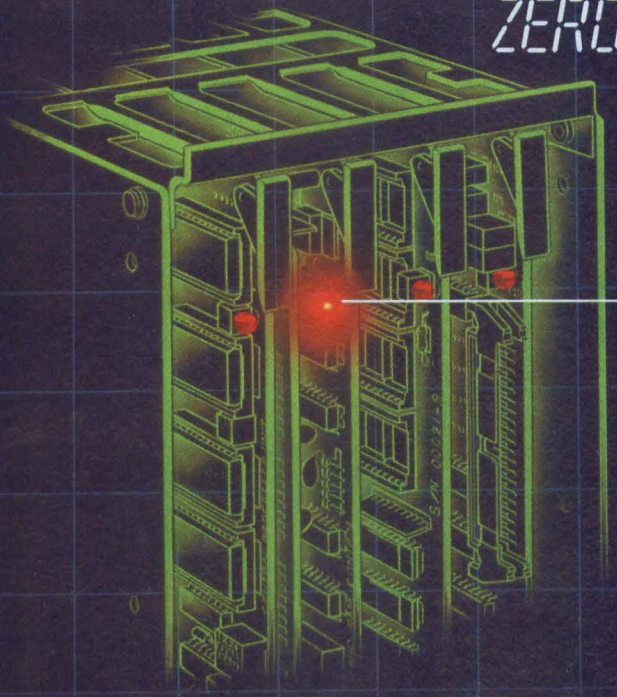
August 12-14—Computer Graphics 80 Internat'l Conf and Exhibition, Birmingham, England. INFORMATION Paula Stockham, Online, Cleveland Rd, Uxbridge UB8 2DD, England

SEMINARS

APR 10-11—Data Communications; APR 24-25 AND MAY 5-6—Data Base Management; AND APR 22-23 AND MAY 12-13—Computer Graphics: Update on Applications and Technology, Hyatt Regency, Chicago, Ill; L'Enfant Plaza, Washington, DC and Hyatt Regency O'Hare, Chicago, Ill; and L'Enfant Plaza, Washington, DC and Hyatt on Union Square, San Francisco, Calif. INFORMATION: Barbara Tarlin, Center for Management Research, 850 Boylston St, Chestnut Hill, MA 02167. Tel: 617/738-5020

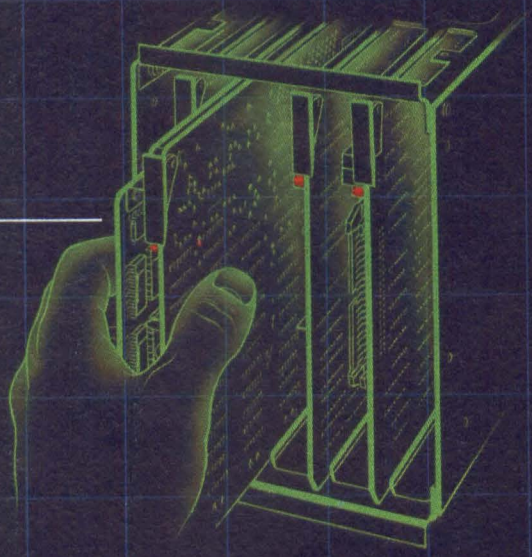
MAY 5-7—Digital Switching Trends, Digital Communication and Signal Processing, and Fiber Optical Communication, Philadelphia, Pa. INFORMATION: Ann Siegenthaler, Information Gatekeepers, 167 Corey Rd, Suite 212, Brookline, MA 02146. Tel: 617/739-2022

SCOUT™ MINICOMPUTER WITH ISOLITE™ INSTANT SELF-TEST FOR VIRTUALLY ZERO DOWNTIME.

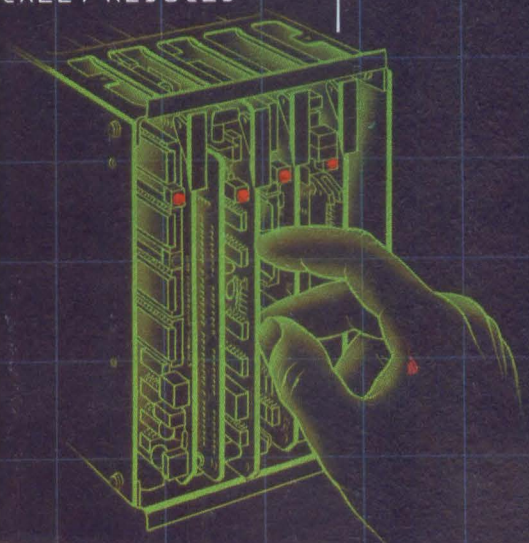


ISOLITE CIRCUIT AUTOMATICALLY TESTS EACH BOARD IN SCOUT SYSTEM.

RED LIGHT SHOWS BOARD BEING TESTED. IF LIGHT GOES OFF, BOARD IS GOOD. IF LIGHT STAYS ON, BOARD IS BAD.



USER REPLACES BAD BOARD WITH SPARE 6.25" X 8.3" CARD IN 3 MINUTES. NO TECHNICAL PERSON OR OEM SERVICE ENGINEER REQUIRED TO MAKE REPLACEMENT. MAINTENANCE COSTS DRASTICALLY REDUCED.



SAVE MONEY WITH SCOUT. GET 16-BIT CPU WITH 32K BYTE RAM, I/O AND CARD CAGE FOR $985 LIST PRICE (VOLUME PURCHASE DISCOUNTS APPLY). CALL OR WRITE FOR MORE INFORMATION.

ComputerAutomation NAKED MINI® Division

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18651 VON KARMAN, IRVINE, CA 92713, PHONE (714) 833-8830, EXT. 455.

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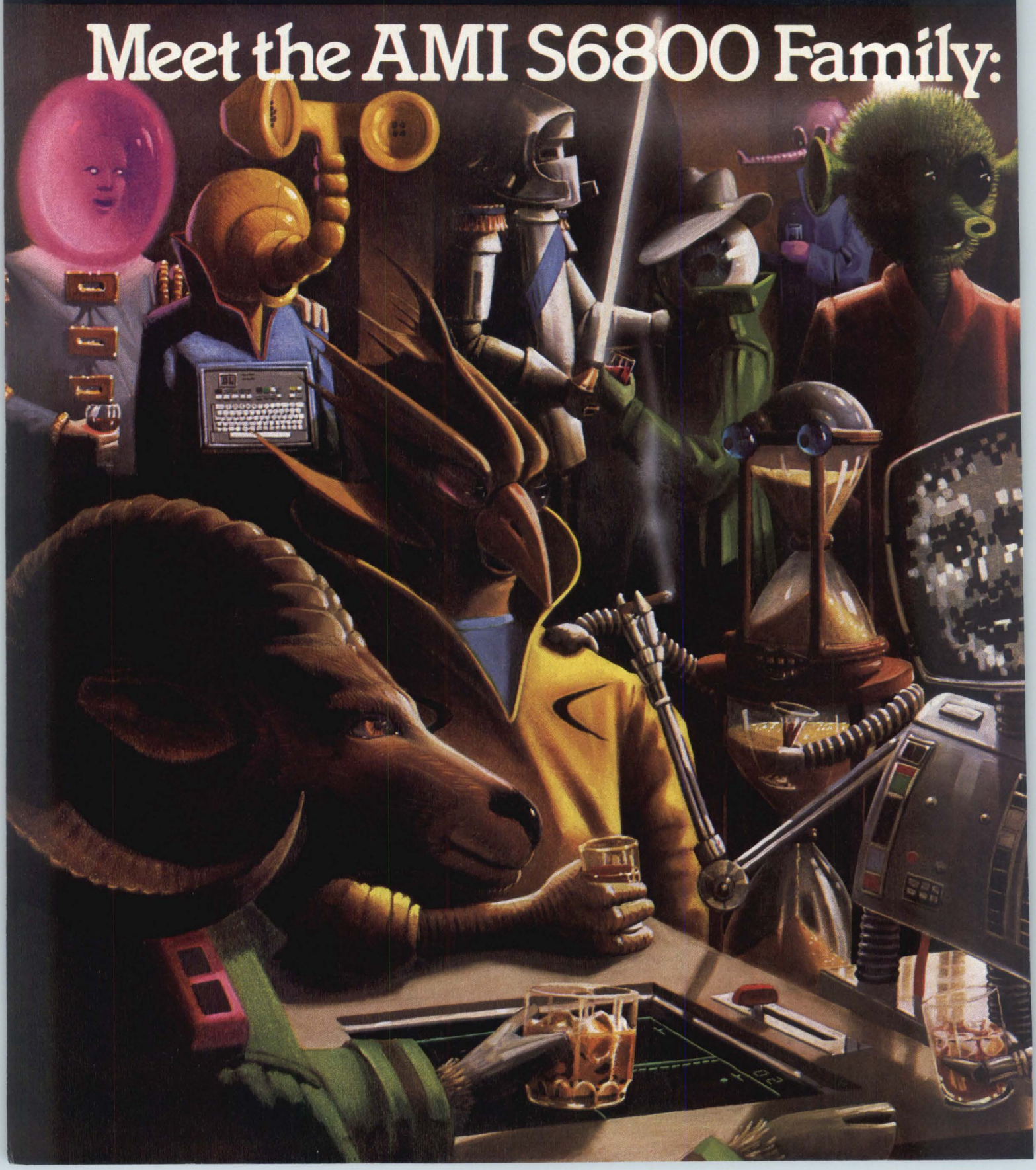
CIRCLE 6 ON INQUIRY CARD

Meet the AMI S6800 Family:



They've got all the power and versatility you need to make your wildest product dreams come true. They're already the fastest growing microprocessor family.

And we'll keep adding superior new members. So you can add futuristic features to dazzle your customers and zap your competitors.

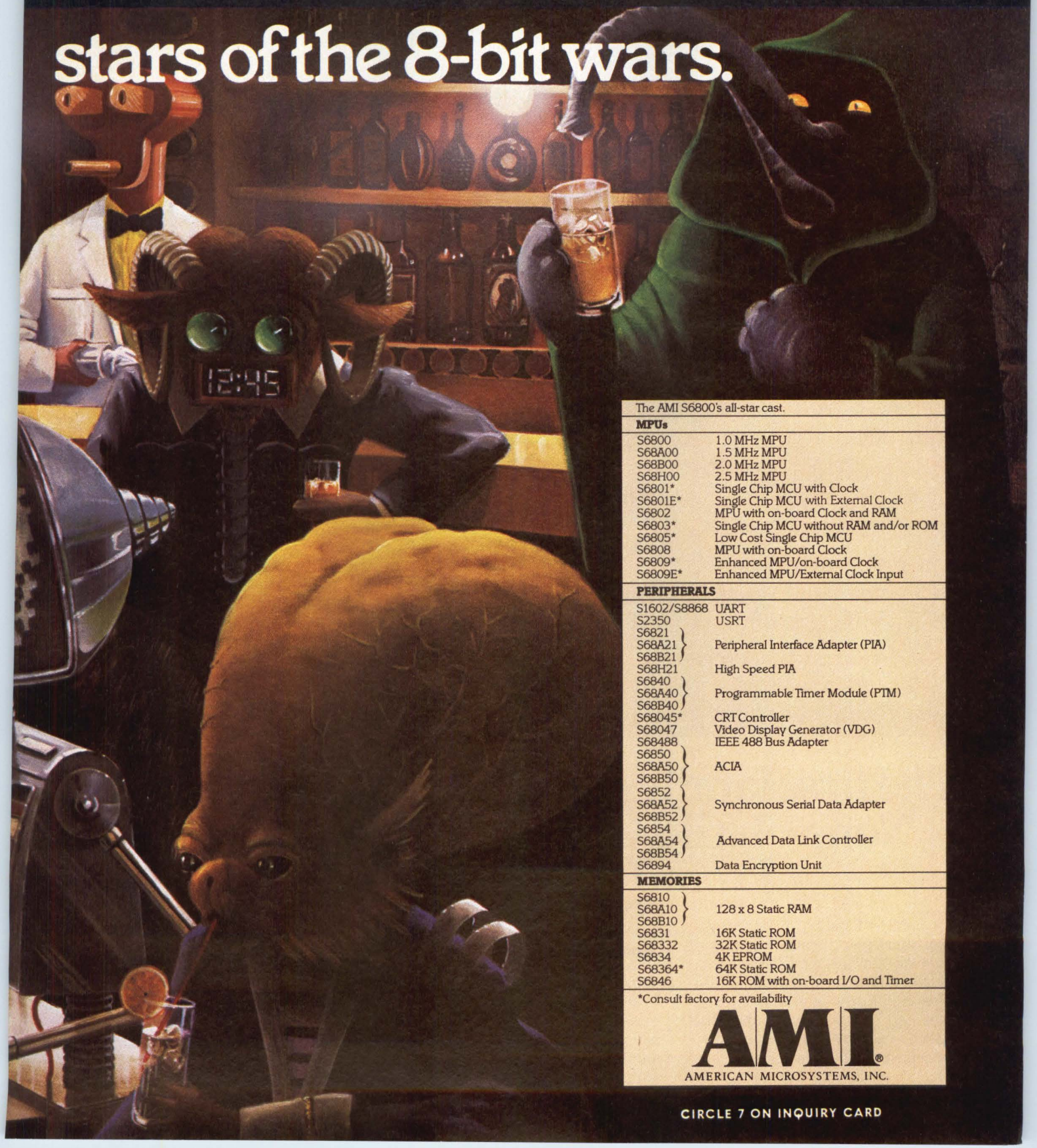
Some innovative newcomers include the brainy, omnipotent S6809. Our screen star, the cost-cutting S68045 CRT controller. Our low cost single chip MCU, the S6805. And the fastest MPU in this league, our 2.5 MHz S68H00. This isn't just a bunch of individualists, either. They're part of the stellar AMI system. Instead of merely selling you parts, we'll look over your present design and, if we can, show you how to cut out some components with a custom peripheral. Or work out a more streamlined

S6800 system, including both standard and custom parts. Perhaps even customizing the MPU.

So let's put our heads together and find the best way to control your product without putting your budget into orbit. Call up your nearest AMI distributor. Or contact us at AMI S6800 Marketing, 3800 Homestead Road, Santa Clara CA 95051. Phone (408) 246-0330.

However far-out your plans are, our family will make light work of them.

stars of the 8-bit wars.



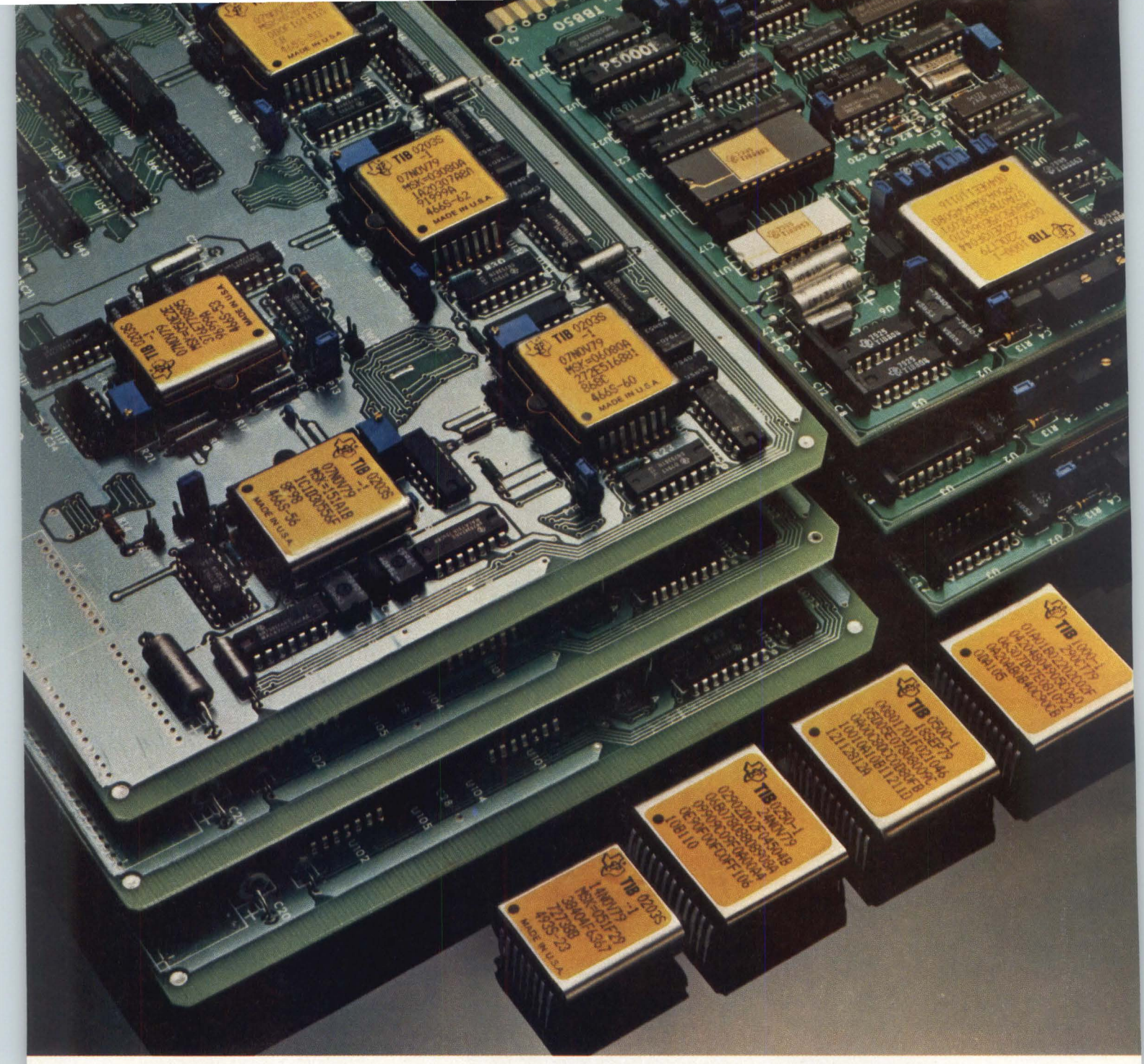
The AMI S6800's all-star cast.

MPUs	
S6800	1.0 MHz MPU
S68A00	1.5 MHz MPU
S68B00	2.0 MHz MPU
S68H00	2.5 MHz MPU
S6801*	Single Chip MCU with Clock
S6801E*	Single Chip MCU with External Clock
S6802	MPU with on-board Clock and RAM
S6803*	Single Chip MCU without RAM and/or ROM
S6805*	Low Cost Single Chip MCU
S6808	MPU with on-board Clock
S6809*	Enhanced MPU/on-board Clock
S6809E*	Enhanced MPU/External Clock Input
PERIPHERALS	
S1602/S8868	UART
S2350	USRT
S6821, S68A21, S68B21	Peripheral Interface Adapter (PIA)
S68H21	High Speed PIA
S6840, S68A40, S68B40	Programmable Timer Module (PTM)
S68045*	CRT Controller
S68047	Video Display Generator (VDG)
S68488	IEEE 488 Bus Adapter
S6850, S68A50, S68B50	ACIA
S6852, S68A52, S68B52	Synchronous Serial Data Adapter
S6854, S68A54, S68B54	Advanced Data Link Controller
S6894	Data Encryption Unit
MEMORIES	
S6810, S68A10, S68B10	128 x 8 Static RAM
S6831	16K Static ROM
S68332	32K Static ROM
S6834	4K EPROM
S68364*	64K Static ROM
S6846	16K ROM with on-board I/O and Timer

*Consult factory for availability

AMI®
AMERICAN MICROSYSTEMS, INC.

CIRCLE 7 ON INQUIRY CARD



The first family of bubble memory systems. Non-volatile. Compact. Easy interface. From Texas Instruments.

TI's family of bubble memory systems offers you the non-volatility of magnetic storage media, plus compactness, silent operation, solid-state reliability, and lower error rates and faster access times than disk and cassette systems.

Because TI bubble memory systems are easily interfaced to microprocessor systems, many designers have already made their choice.

And, they've chosen from the TI family of bubble memory systems.

It's a design decision that makes sense. That's why you'll find TI bubble memory systems improving the performance of intelligent terminals, word processors, industrial process controls, instrumentation and telecommunications equipment, add-on buffer/cache memories — and more.

Because bubble memories are so small and lightweight, they're ideally suited to portable applications such as small computers, data loggers and a variety of educational

and home entertainment products.

And the innovations keep on coming. In product breadth. Technology. Production.

New bubble memory systems with storage capacities ranging from 23K to 768K bytes are being supplied. All the custom-designed peripheral and support circuitry for bubble memory systems are available.

New wafer processing techniques, including state-of-the-art planar construction — coupled with TI's innovative two-micron technology — are making newer and better things happen all the time.

TI's eight years of experience in bubble memory design and production have provided keen insights into customer requirements.

Requirements that demanded we deliver. And we have. In fact, TI has delivered more bits of bubble memory than all other suppliers — combined.

Only Texas Instruments can offer you a full family of bubble memory systems. A family built on know-how and experience. A family that reinforces TI's established position as the leader in bubble memory technology — and products.

Systems components

TI's complete family of bubble memory systems is comprised of component devices with capacities from 92K bits to 1 megabit.With access times from 4.0 to 11.2 ms.

These various capacities, along with the necessary support circuits, offer you a wide choice of compact systems for ease of use and design configuration flexibility.

The 1 megabit TIB1000, for example, is electrically and physically interchangeable with family members TIB0500 at 512K and the 256K TIB0250. Both are supported by the same comprehensive line of custom interface circuits.

The planar processing techniques, and new refinements in photolithography allow TIB1000 to offer the highest commercial bit density ever — by a factor of two.

Custom support circuits

All TI bubble memory systems contain a complete set of interface and peripheral circuits — including two custom controllers. One for the 92K devices. One for the megabit family. So, it's not necessary to emulate controller function and you save a design step. Both are available.

These circuits, designed specifically for bubble memories, encompass state-of-the-art bipolar and MOS integrated circuit technologies. This provides high level interface between all of today's popular microprocessors and all of TI's bubble memory products.

The 92K TIB0203 is supported by its own family of custom peripheral circuits. The binary TIB0250, TIB0500 and TIB1000 are all supported by a common set of interface circuits.

TI'S FAMILY OF BUBBLE MEMORY SYSTEMS

PART NUMBER	STORAGE CAPACITY	COMPONENTS	BOARD FORMAT
TM990/210-1	23K Bytes	2 92K-bit	TM990
TM990/210-2	46K Bytes	4 92K-bit	TM990
TM990/210-3	69K Bytes	6 92K-bit	TM990
TBB5005	64K Bytes	1 512K-bit	OEM Board
TBB5010	128K Bytes	1 1024K-bit	OEM Board
TM990/211-1	128K Bytes	1 1024K-bit	TM990
TM990/211-2	256K Bytes	2 1024K-bit	TM990
TM990/211-3	512K Bytes	4 1024K-bit	TM990
TM990/211-4	768K Bytes	6 1024K-bit	TM990

Custom support circuits for all families of devices include: coil drivers, sense amplifiers, function drivers, controllers and function timing generators.

An advanced family of support circuits, coming soon, has been designed for parallel operation as well as error correction.

Bubble memory systems

To provide ease of use and a convenient production board, each new member of TI's bubble memory family is available on a completely assembled, fully tested, compact printed circuit board.

TBB5005 and TBB5010 systems

Non-volatile bubble memory systems assembled on a 4″ x 6″ board with custom controller and all other peripheral devices and using the new family components. Features common to both systems include: up to 128K bytes of memory capacity, interface with TMS9900, 8080 and Z80 microprocessors, access times of 11.2 ms, data transfer rates of 85K bits/sec., system expansion capability and a choice of board connector styles.

TM990/210 system

Here's a non-volatile bubble memory system using the production-proven 92K bit TIB0203 device. Up to 69K bytes assembled on a single board, including a full complement of custom control circuits. Interfaces directly with TMS9900-based microcomputer modules. This system is in stock and available for immediate off-the-shelf delivery from your TI distributor.

TM990/211 system

A non-volatile bubble memory system utilizing the TIB1000 with up to 768K bytes capacity. Bus compatible with TM990/100 microcomputer modules, the TM990/211 system features 11.2 ms access time with data transfer rates of 85K bits/sec. A new module, coming, will be able to be combined with the TM990/211 system to provide a megabyte bubble memory system with on-board error correction, direct memory access, and compatibility with TM990 file management.

And the innovations keep on coming

Texas Instruments is firmly committed to innovative, cost-effective bubble memory technology and product development.

So, for a full line of bubble memory systems — standard or customized to your application — turn to the leader — turn to Texas Instruments for magnetic bubble memory products.

For more information, write to Texas Instruments Incorporated, P.O. Box 225012, M/S 308, Dallas, Texas 75265. We'll send you our new 8-page brochure along with details about the bubble memory course offered at the TI Chicago Regional Technology Center.

Fifty Years of Innovation

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CIRCLE 8 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

Your readers should be warned that the arbiter circuit described in "Queue Handling Arbiter Solves Shared Resource Conflicts" (K. Søe Højberg, *Computer Design,* Nov 1979, pp 129-135) while logically correct cannot be reliably implemented. The circuit will suffer from what has been called synchronizer failure (T. J. Chaney and C. E. Molnar, "Anomalous Behavior of Synchronizer and Arbiter Circuits," *IEEE Transactions on Computers,* April 1973, pp 421-422). Specifically, because a real flipflop is not a discrete device, there are input conditions, such as data and clock inputs, changing at about the same time, which will cause the flipflop to enter a metastable state in which it may remain for an unbounded amount of time. Depending on the logic family used, this metastable state may have different characteristics such as oscillations between a 1 and 0 output or an output halfway between 1 and 0.

While Højberg's circuit will indeed work most of the time, it will fail (due to synchronizer failure) with some finite, nonzero, probability. Indeed, it is a well-known fact that it is impossible to reliably synchronize two systems which have independent time bases unless provisions are made for doing something like starting and stopping the system clocks.

Edward H. Frank
Carnegie-Mellon University
Pittsburg, Pa

The Author Replies:

For a given application an arbiter should be evaluated in connection with its job and its environment. The consequence of eventual inclusion of nonideal synchronizing elements as well as other nonideal conditions should be estimated as a whole. In this connection, noise on the power supply and reset lines, and consequences of limited component reliability can be mentioned.

The method adopted in the state machine arbiter (K. Søe Højberg, "Queue Handling Arbiter Solves Shared Resource Conflicts," *Computer Design,* Nov 1979, pp 129-135) for reduction of the probability of metastable conditions at the expense of clock interval time is the control delay method (D. J. Kinniment and J. V. Woods, "Synchronization and Arbitration Circuits in Digital Systems," *Proceedings of the IEE,* Oct 1976, pp 961-966). By means of this (and other methods) a system of known reliability can be constructed. For example, a system containing a simple flipflop with delayed sampling of its output can have a response time below 50 ns and a mean time between failures of 31,700 years (Kinniment and Woods).

K. Søe Højberg
Risø National Laboratory
Roskilde, Denmark

NEW TECHNICAL EDITOR AT COMPUTER DESIGN—Shawn Spilman has joined the editorial staff of *Computer Design* magazine as Technical Editor. Most recently managing editor of a computer hobby magazine, Shawn was previously a technical writer for Atex Corp and Digital Equipment Corp, a programmer, and a freelance editor, and is the author of handbooks on both small computers and an introduction to programming. He received a BSEE degree from Tufts University and is a candidate for an MS in Computer Science from Worcester Polytechnic Institute.

Shawn Spilman
Technical Editor

Letters to the Editor should be addressed:

Editor, Computer Design
11 Goldsmith St
Littleton, MA 01460

Note:

Formulas published in the Application Note, "Reliability Computations on a Handheld Programmable Calculator," by C. R. Lewart, p 140 of the Nov 1979 issue of *Computer Design* were from an unpublished Appendix to Ref 2 of that Note: R. Zussman, "Forecasting Computer System Reliability With a Handheld Programmable Calculator," copyright Computer Design Publishing Corp, Mar 1979. A footnote to that fact was inadvertently omitted.

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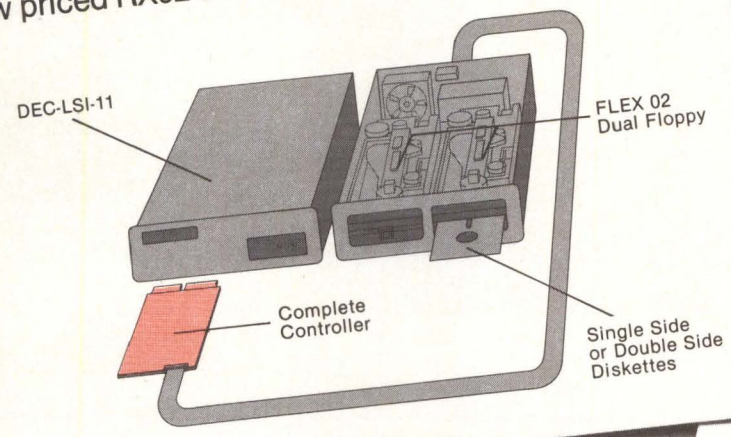

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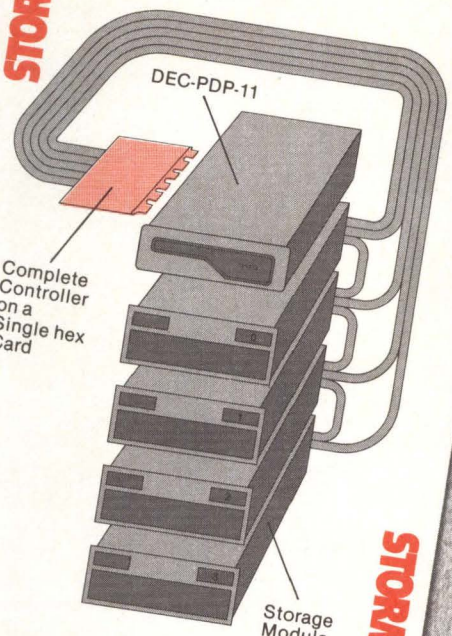

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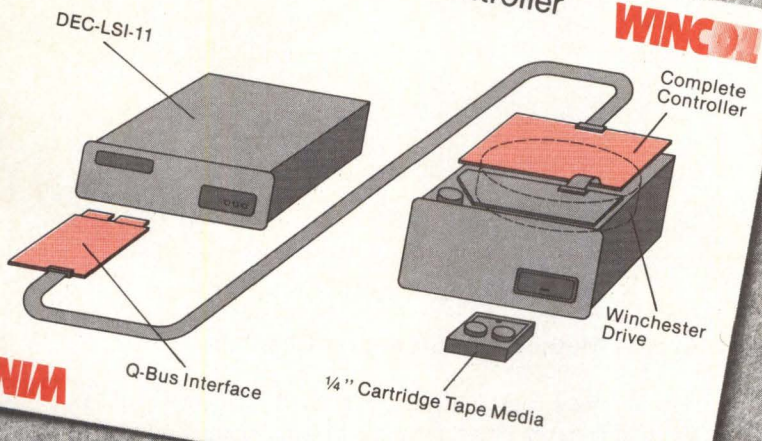

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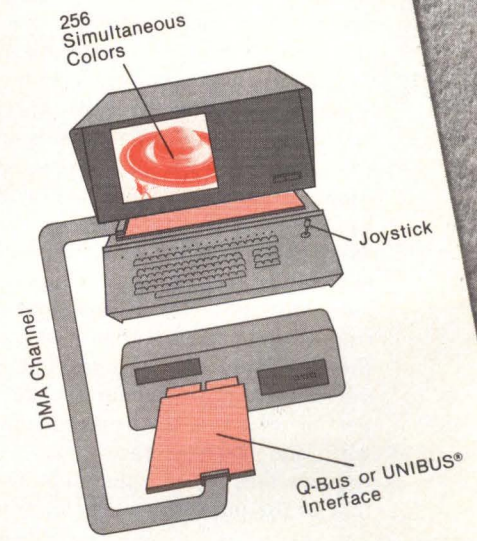

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CIRCLE 10 ON INQUIRY CARD

COMMUNICATIONS IN DISTRIBUTED SYSTEMS—PART 2: COMMON BUS AND SHARED RESOURCE ACCESS SCHEMES

Melvin G. Gable

Ford Motor Company
Dearborn, Michigan

Broadcast techniques offer a reliable system design approach for establishing communication between distributed processors. All processors share a common medium, such as coaxial or fiber optic cable, or a radio frequency channel. Arbitration or contention in accessing the medium is handled locally at each processor interface. Since the medium itself is usually passive, no active element failure will inhibit communications for other processors.

A ground radio packet switching system is one means by which many geographically distributed users may communicate. Ground radio systems have been in use for many years; one such network is the Aloha system,[1] which interconnects various islands in the Hawaiian group to the University of Hawaii Computer Center. The Aloha system uses a radio broadcast channel, with transmission occurring at random. A refinement of this access method, called slotted Aloha, provides a time slot equal to the transmission time of a single packet and all transmissions must start at the beginning of a slot. In both slotted and pure Aloha systems, when two or more packet transmissions overlap in part or totally on the broadcast channel, they will interfere with and destroy each other. However, slotted Aloha reduces the period vulnerable to interference to one-half that of the pure Aloha scheme (Fig 1).

Access Methods for Broadcast Channels

How to share and control access to the channel with an acceptable level of performance is the main problem in broadcast techniques. As an example, each of a collection of devices is attempting to transmit over a shared communications channel. When two separate source transmissions overlap, they interfere with each other. If communication channel propagation delay between any source and destination node is relatively small with respect to that of the transmission duration, it is more efficient to sense if the channel is idle before attempting transmission. The interface at the transmitting end should be able to monitor the channel through the use of a carrier detect signal. If the signal is heard, the transmitter will recognize that the channel is in use, and will defer or postpone its transmission until the channel is sensed to be idle. This method of operation is known as carrier sense multiple access (CSMA).[2]

The implementation of carrier deference does not guarantee channel acquisition. Two or more devices may detect the channel idle and attempt transmission. However, the detection of carrier from another transmitter may take the end-to-end propagation delay time of the medium. Under these conditions, interference from multiple

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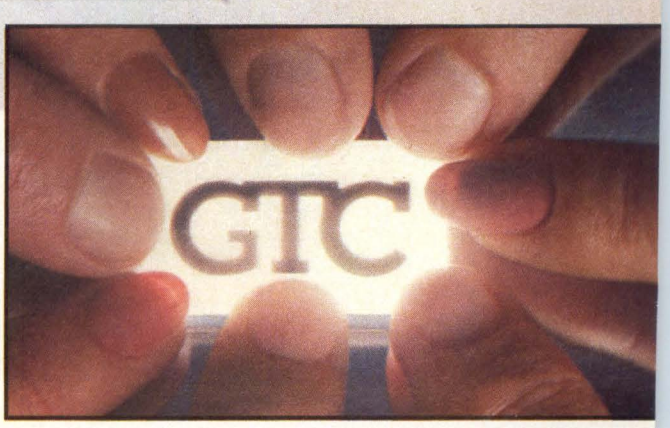

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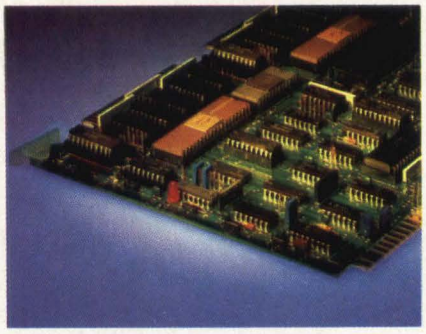

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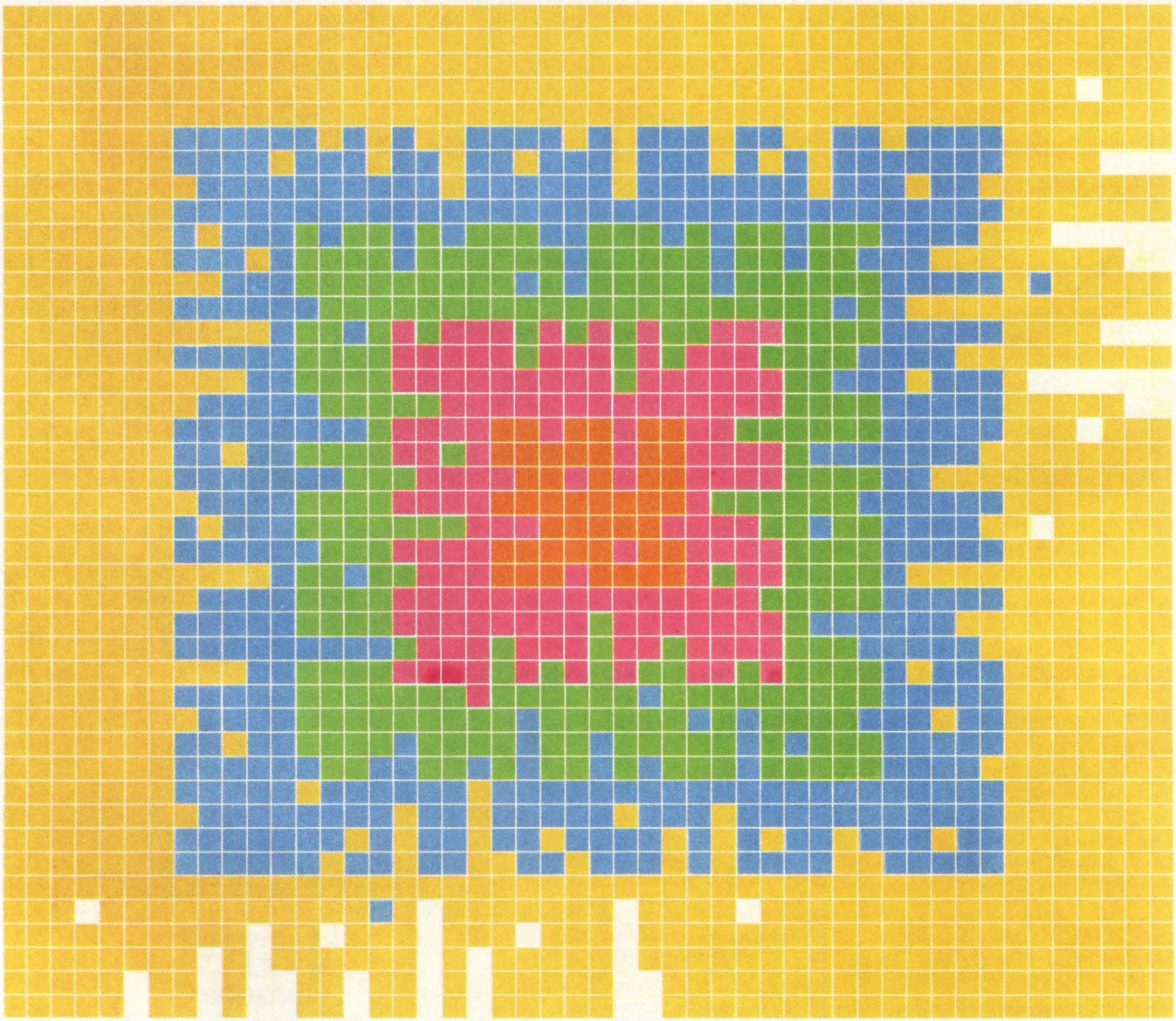

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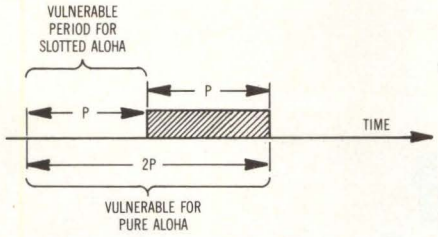
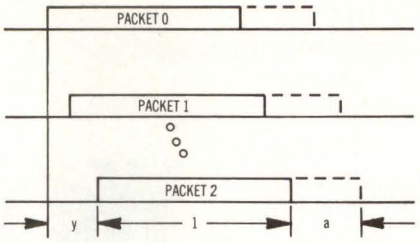


P = TRANSMISSION PERIOD

Fig 1 Vulnerability to collisions in Aloha. In pure Aloha, it is possible for one packet to interfere with two other transmission periods. In slotted Aloha scheme, transmission can only be initiated at beginning of packet slot; if it collides, only one transmission period is affected



y = ARRIVAL TIME OF LAST PACKET COLLIDING WITH PACKET 0
a = PROPAGATION DELAY
$0 \leq y \leq a$

Fig 2 Vulnerability to collisions in CSMA. Transmission is initiated only if carrier is not detected in CSMA scheme. However, interference period is equal to arrival time of last colliding packet plus packet transmission time (normalized to 1) and propagation delay of medium

simultaneous transmissions may occur (Fig 2). The transmitting node determines that its previous transmission was unsuccessful due to the absence of a positive acknowledgment from the receiving node, and reschedules its transmission of data. The receiving station itself usually determines that the transmission was in error through the use of a cyclic redundancy coding of the block.

A contention access problem arises when a device determines that its transmission was unsuccessful due to interference. It must then reschedule the packet for retransmission. To avoid collision of interfering devices upon retry, they must attempt transmission at time differences that are greater than the propagation delay between them. To a great extent, the rules for deciding when a device may attempt retransmission will determine the channel capacity.

Contention Comparisons

Three types of persistent CSMA protocols, known as 1-persistent, non-persistent, and p-persistent, have been proposed and studied. These various protocols differ in the action that the user takes after sensing the channel.

The channel can employ a non-persistent protocol that schedules packets in the following manner: if the channel is idle, the packet is transmitted; otherwise (channel busy), the packet is rescheduled for transmission at some later time according to a delay distribution function. In contrast to the non-persistent user, a 1-persistent approach can be applied. With this method, the packet is transmitted with probability-one when the channel is sensed idle. A p-persistent scheme differs only in the fact that it will transmit with probability P on detection of idle.

Analytical models and simulation results are available for several CSMA access methods.[3,4,5,6] In the analytical models, the channel is assumed to have Poisson traffic arrivals.

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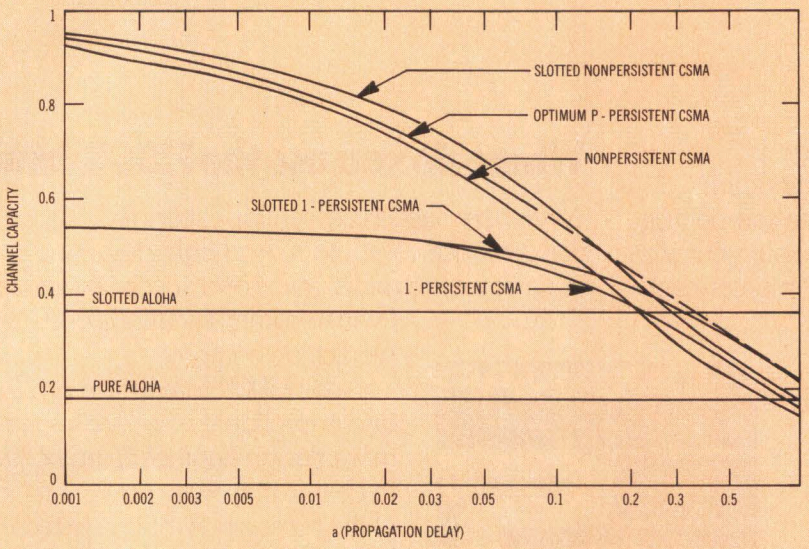

Fig 3 Effect of propagation delay on channel capacity in CSMA. Channel capacity is dependent on ratio of propagation delay to packet transmission time. When ratio becomes large, CSMA performance degrades to that of Aloha schemes

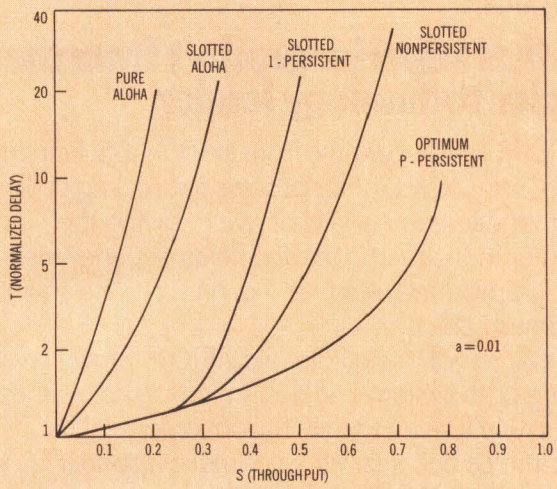

Fig 4 Delay vs throughput for various access schemes. Message delay (normalized to packet transmission time) is dependent on throughput of communication channel. Various CSMA persistent schemes provide excellent delay performance when propagation delay is small compared to packet transmission time (a = 0.01)

The models show that packet size, transmission rate, and propagation delay can be traded off to obtain an acceptable level of performance. An analysis of channel capacity relative to the ratio "a," propagation delay time per packet transmission time (Fig 3), reveals that as "a" becomes large, the channel capacity is reduced. For large values of "a," CSMA schemes approach performance levels of the pure Aloha. Hence, the CSMA scheme is useless when propagation delay time between devices is large. This is because the sensed channel state provides obsolete information about the channel. In all of these access methods, retransmission of a data packet is according to a randomly distributed transmission delay. The delay a message may encounter in transmission will be dependent on this retransmission delay, as well as the offered traffic to the channel. Communication delays of various protocols are illustrated in Fig 4. The use of messages to schedule events in other processors will be affected by this channel delay, which will vary if there are fluctuating traffic conditions. The common communication channel provides a means by which separate system components and processors can access and update shared variables and resources. The statistically varying channel delay complicates the problem of event synchronization, which is usually necessary for this sharing of resources. Research is currently being carried on in the areas of synchronization functions and primitives for distributed system architectures.[7,8]

Shared Resource Synchronization

A properly functioning distributed system must provide a mechanism that will guarantee asynchronous access to shared resources. This is necessary to protect data and devices from being changed simultaneously by two or more processors. It follows that there must be some form of mutual exclusion in order to allow one process to lock out access to a shared resource by other processors in a critical section. A critical section is a code sequence that, once begun, must complete execution before another process enters a code section that accesses the same shared resource. A Boolean variable or semaphore can be used to indicate whether or not a process is executing a critical section. Since the testing and setting of such a variable is itself

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CIRCLE 18 ON INQUIRY CARD

a critical section, this function must be performed by a single indivisible (atomic) operation. If it is not an atomic action, two or more processes may test the variable simultaneously and then set it. This action would allow simultaneous execution of critical sections, and the result could be erroneous multiple accesses to peripheral device controllers or global memory parameters.

Mutual exclusion can be accomplished in software through two primitive operations described by Dijkstra for "N" parallel processes.[9] Designated as P and V, these primitives operate on integer variables called semaphores. The V procedure increments the semaphore in a single indivisible operation, while the P procedure loops in a busy wait state until the semaphore is greater than zero, at which time it decrements it.

A bus lock operation can be issued to make certain that the fetch, increment, or decrement and store are not interrupted by another processor in a multiprocessor system. The program should test the semaphore before issuing a bus lock to avoid the continuous locking and unlocking of the shared system bus while looping in the wait state. However, a second test is required after the lock to insure that another processor has not also found the semaphore greater than zero and has tried to enter the critical section at the same time.

P and V operations of semaphores, as well as the system bus locking scheme, provide a means of mutual exclusion in a multiple processor system. These techniques permit the sharing of resources by two or more processors. However, such schemes are not very attractive in distributed systems where communication delays become rather large compared to the processor instruction cycle. Locking of the communication bus will result in inefficient utilization of the data channel. Continued research in this area will most likely uncover improved synchronization techniques.

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The third and final part of Mr. Gable's column discusses communication protocols and system design considerations. It will appear in our April issue.

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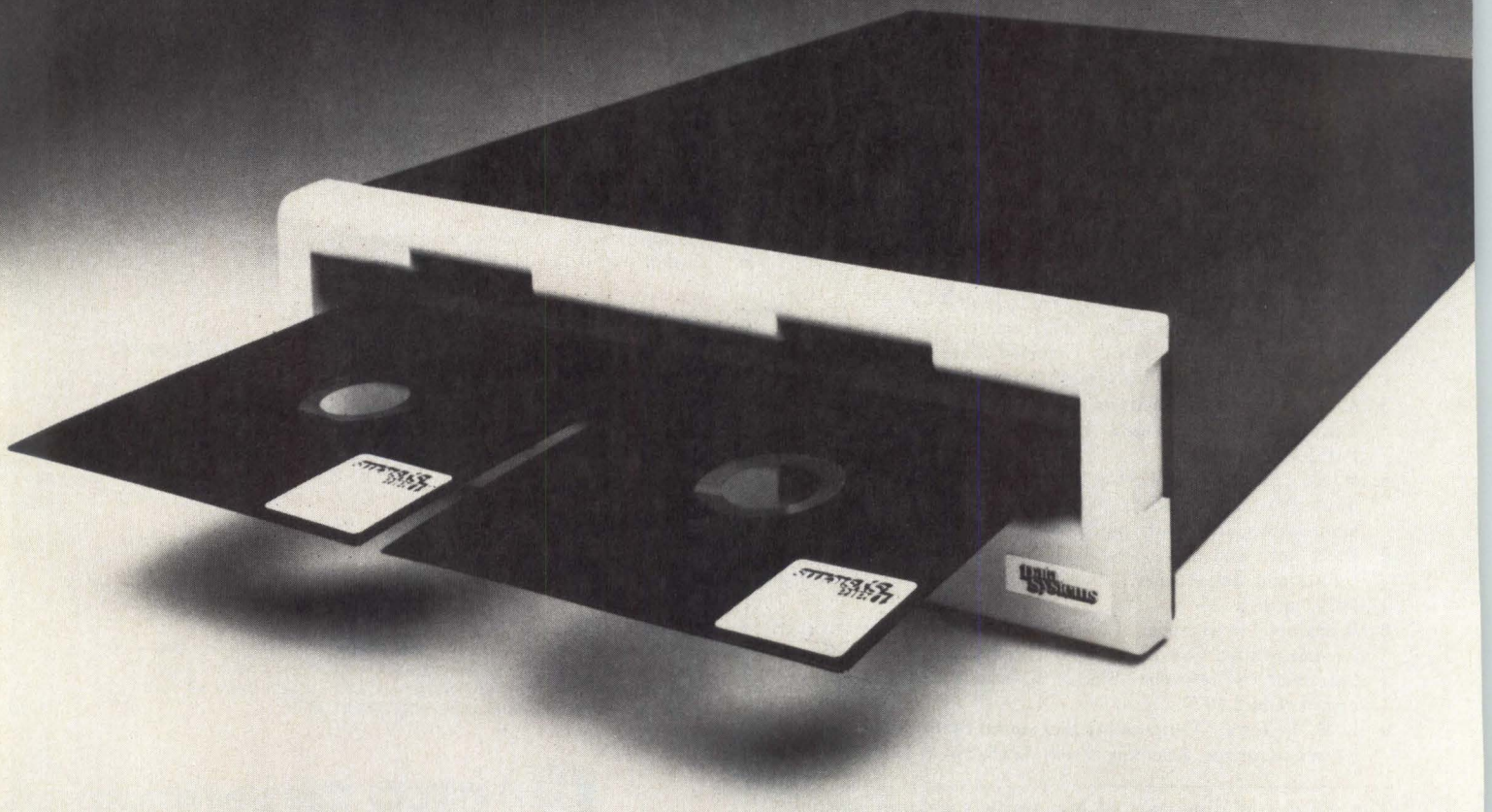

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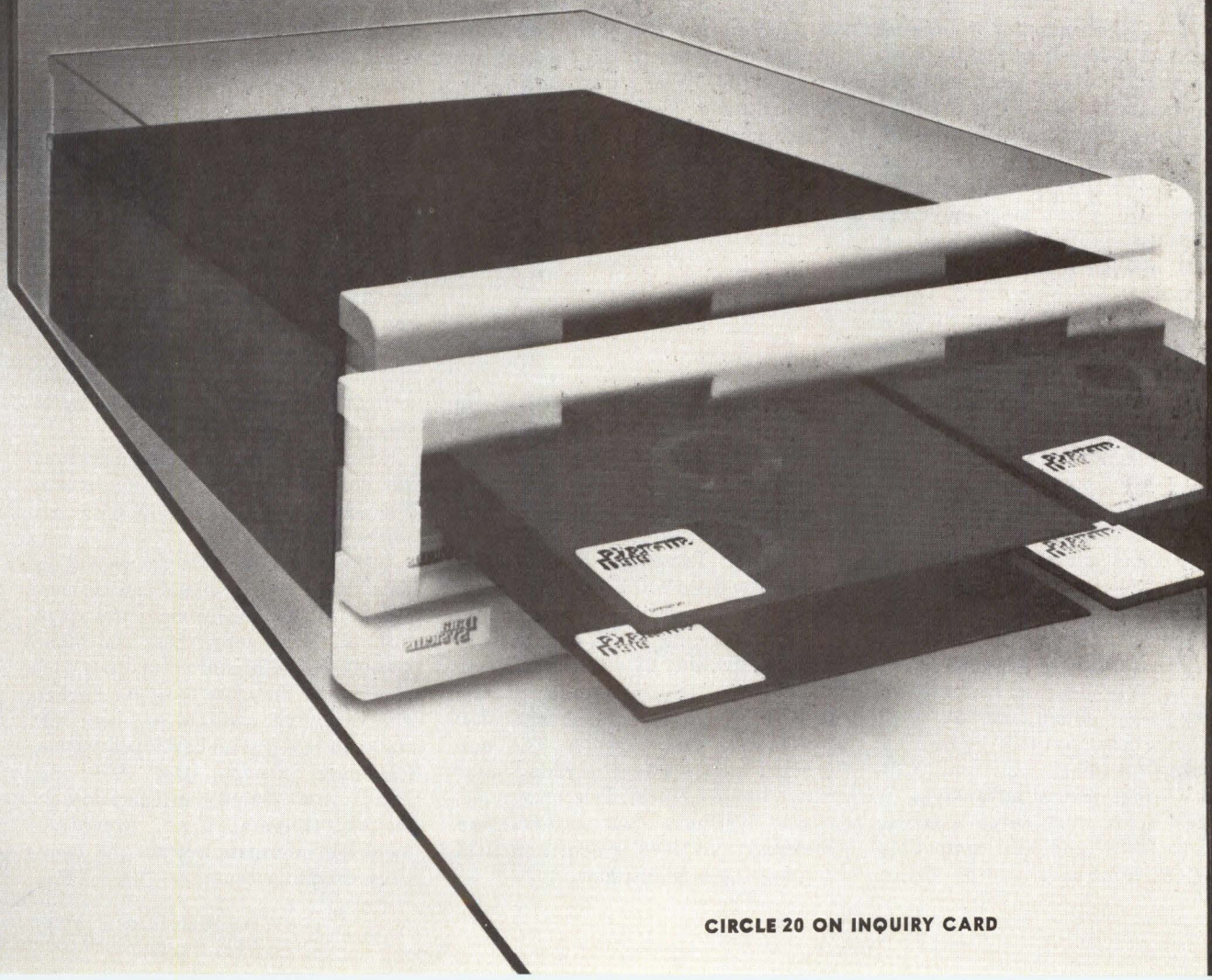

CIRCLE 20 ON INQUIRY CARD

Newly Adopted CCITT Communications Standards Find Early Support

Recently established Recommendations X.20 and X.21, terminal to network interface standards for asynchronous and synchronous transmissions respectively, were developed by the International Consultative Committee on Telegraph and Telephone (CCITT) in the early 1970s. They specify electronic and circuit level interfaces covering in scope the number of pins on a plug to the level of how call connections can automatically be made (Autocall) through the network.

Both recommendations have two parts. One calls for replacing existing EIA RS-232 and CCITT V.24 electrical interfaces with a simpler, lower cost alternative, replacing existing 25-pin with 15-pin connectors. Second part of the standards calls for the replacement of the previous RS-336 and CCITT V.25 switched network interface standards, that required two different physical connections for a computer or terminal to access a switched telecommunications network. A device with full X.20 or X.21 capability will be able to access such a network automatically through a simpler, single interface. In many respects the new standards can be thought of as performing the same functions as a full X.25 packet-level protocol, without any of the complexities of packet switching.

Among the first to support the new standards is Tran Telecommunications Corp, 2500 Walnut Ave, Marina del Rey, CA 90291, with its M3200 series network processors and network access concentrators. These will continue to support existing communications standards, and since X.20 and X.21 specify the low end, electronic, and circuit level interfaces, the new standards are expected to be used in conjunction with higher level protocols already supported by the M3200 series.

M3200 provides several forms of switching for both virtual and physical circuits: packet, circuit, and "Pacuit," a proprietary hybrid switching technology. Adding X.20 and X.21 support brings several advantages. It provides a low cost network access means for X.20- and X.21-compatible computers, front ends, and terminals; simplifies isolation of malfunctions in terminal and communications equipment; and eliminates the 50-ft (15.24-m) limitation for local terminals forced by some computer architectures.

The capacity of the M3200 architecture to concurrently support several switching technologies makes it easy to add the new standards. The need for X.20 and X.21 support is expected to grow substantially by late 1981. Tran interfaces are scheduled for the second quarter of next year.

The development of both standards, especially that of X.21, has been supported by carriers and computer vendors alike. Many of the details of the standards derive directly from AT&T and IBM contributions. Early in January 1980, IBM announced that X.21 support for some terminals and computers would begin almost immediately. This will almost certainly bring a broad base of support and acceptance for X.21, and should, indirectly, ensure a similar future for the X.20 asynchronous standard.

Systems Group Formed For Data, Voice, and Viewdata Services

Anticipating "explosive growth" in data communications and continuing strong growth in the demand for voice communications, the establishment of a new group, GTE Communications Network Systems, has been announced by General Telephone & Electronics Corp, One Stamford Forum, Stamford, CT 06904. The group will be responsible for marketing public data network services, private data and voice network systems, standalone private branch exchanges (PABXs), and electronic data base services. The new group includes three operating units (GTE Telenet, GTE Telecommunications Systems, GTE Information Systems), and development and field engineering organizations.

GTE Telenet, a key component in the new alignment, plans a major expansion of its nationwide packet-switched public data network that will add 160 central offices (switching and network access centers) to the system, bringing the total to 250 in 1980. Later this year, an electronic mail service for message communications and document distribution will be inaugurated. Included in the 1980 plan is the addition of network interface facilities to accommodate such high speed terminals as IBM 3270-type, 2780, and HASP workstations.

In 1981 the network plans to implement a high capacity, high bandwidth satellite packet broadcast system, with dedicated ground stations located at major central office sites, and using existing communications satellites. Also in 1981, portions of the basic terrestrial network will be upgraded in transmission speed from 56k to 1.5M bits/s, reducing end-to-end transmission delay time from 200 to less than 50 ms. Further downstream, the company plans to use the new 10-GHz frequency bands, expected to be allocated by the FCC for multipoint digital communications, for intra-city packet radio transmission.

In extending these network services, the capabilities and equipment of Cambridge Telecommunications, Inc, will be included. This firm, acquired by GTE Telenet in late 1979, is engaged in the development and design of equipment and software for interfacing computers and terminals to packet-switched networks. GTE Telenet is located in Vienna, Va.

GTE Telecommunications Systems will concern itself with PABX interconnect sales, and private voice/data networks.

GTE Information Systems, providing data base and communications services for the investment/brokerage business, will pursue these and other specialized information markets, including the Viewdata program. Earlier this year, GTE acquired exclusive U.S. rights to this British-developed system (*Computer Design,* Oct 1979, pp 10-17). It is currently in operation on an experimental basis, providing database information from the company computer center in Tampa, Fla.

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CIRCLE 21 ON INQUIRY CARD

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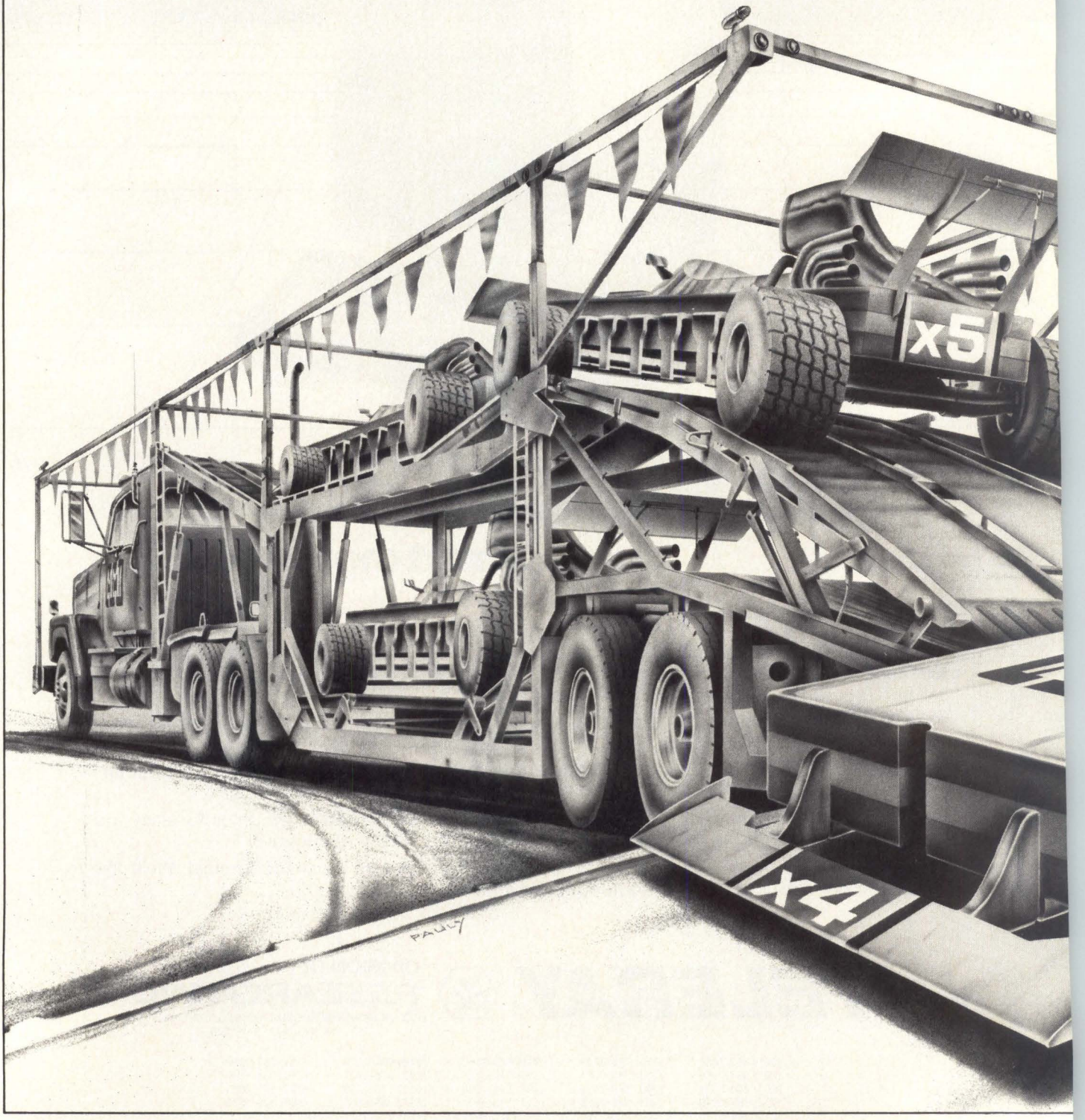

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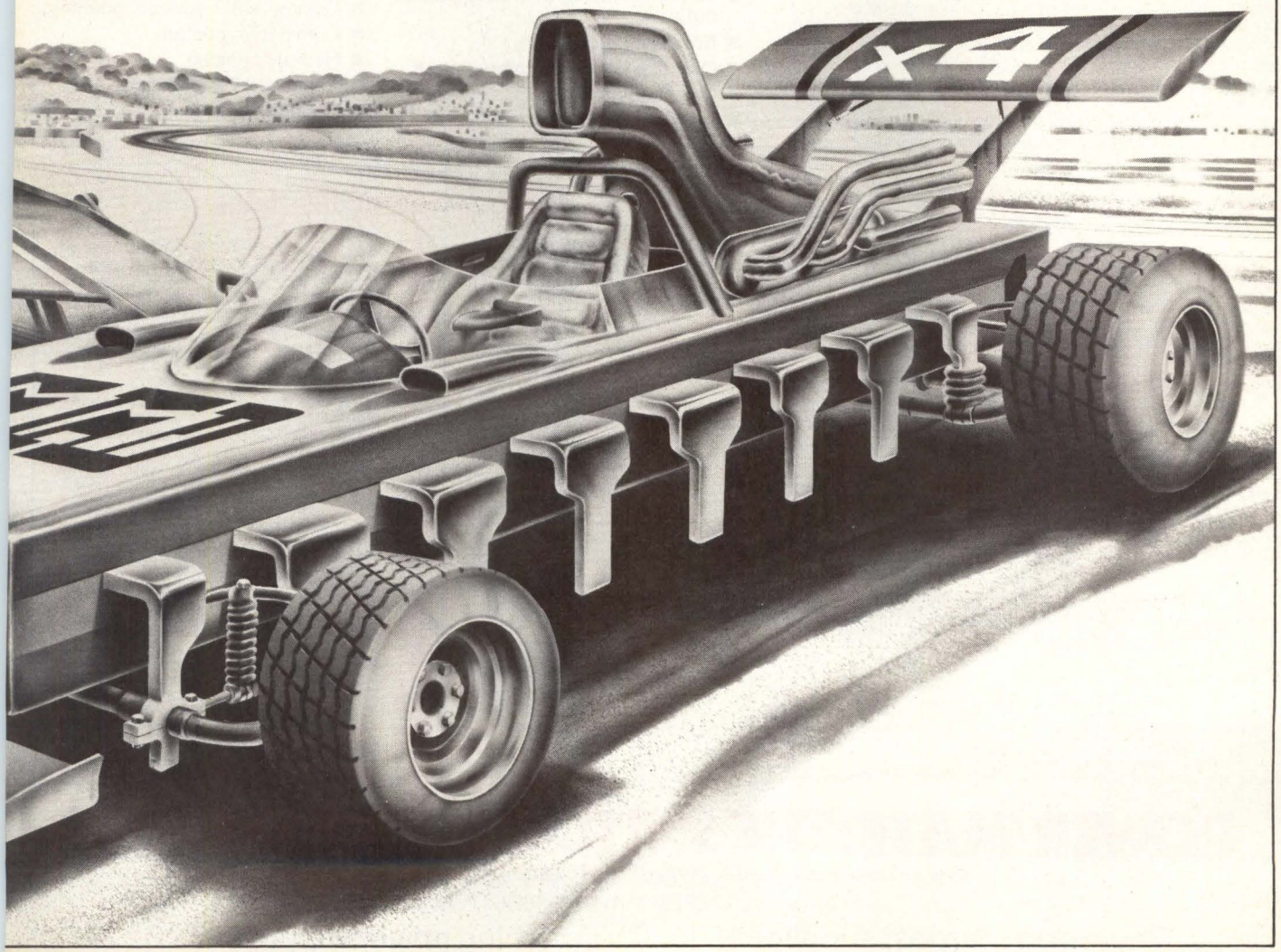
CIRCLE 22 ON INQUIRY CARD



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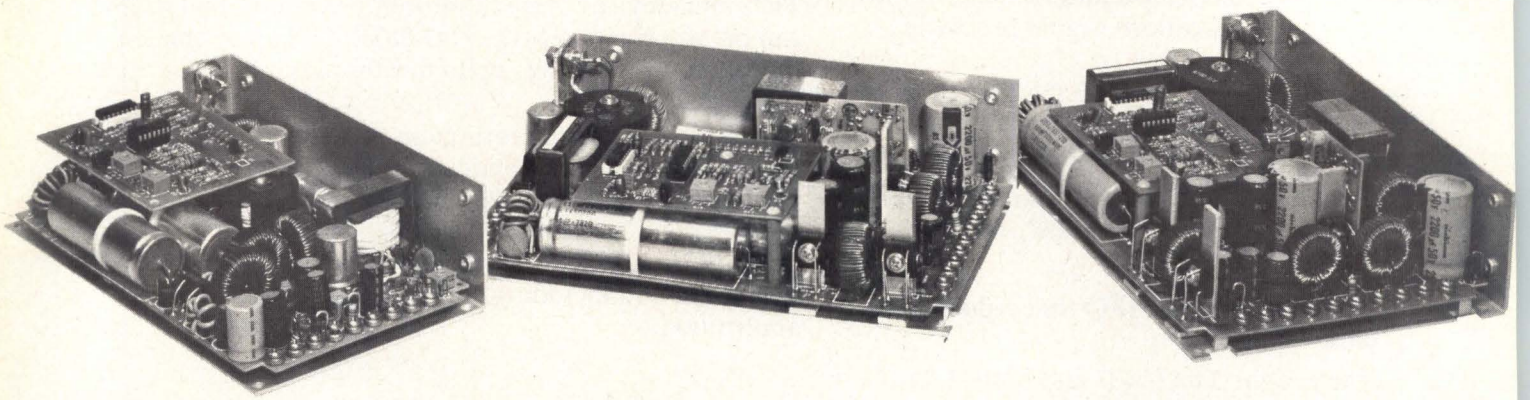

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The Econo/Switch multiple output supply gives you exceptional versatility, combined with reliability, efficiency and compactness... at low cost.

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Standard Models	ESM-100-5001	5V@10A	12V@3A	12V@3A	5V@2A	24V@2A	100W
	ESM-100-5002	5V@10A	15V@3A	15V@3A	5V@2A	24V@2A	100W
Customized Models	ESM-100-xxxx	*@10A	*@3A	*@3A	*@2A	*@2A	100W

ESM-200 Series—200 Watts — $319.

	Model	Output 1	Output 2	Output 3	Output 4	Output 5	Max. Cont. Output Power
Standard Models	ESM-200-5001	5V@20A	12V@4A	12V@4A	5V@2A	24V@4A	200W
	ESM-200-5002	5V@20A	15V@4A	15V@4A	5V@2A	24V@4A	200W
Customized Models	ESM-200-xxxx	*@20A	*@4A	*@4A	*@2A	*@4A	200W

ESM-300 Series—300 Watts — $399.

	Model	Output 1	Output 2	Output 3	Output 4	Output 5	Max. Cont. Output Power
Standard Models	ESM-300-5001	5V@30A	12V@6A	12V@6A	5V@4A	24V@4A	300W
	ESM-300-5002	5V@30A	15V@6A	15V@6A	5V@4A	24V@4A	300W
Customized Models	ESM-300-xxxx	*@30A	*@6A	*@6A	*@4A	*@4A	300W

* User specified. Consult factory or local sales office. Minimum 250 units

Note 1: Maximum specified current cannot be drawn from all outputs simultaneously. At no time should the average current exceed the maximum continuous output power. Above this point, output voltages and currents will be automatically reduced on all outputs. **Note 2:** Output 1 must be loaded to 15% of total output power to maintain proper regulation of other outputs. (Supply will not be damaged by no-load condition on Output 1.) **Note 3:** On ESM-200 and ESM-300 models, all five outputs are isolated. On ESM-100 models outputs 4 and 5 have a common return. All other outputs are isolated.

Options: Crowbar up to 8 Amps $8, greater than 8 Amps $16. Add Suffix V to Model No. Cover $10. Add Suffix C to Model No.

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AC Input. 95-132 and 190-264 VAC, 47-63Hz.

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Long Term Stability. 0.1% for 8 hours after 20 minute warm-up.

Ambient Operating Temperature. Continuous duty from 0°C to 71°C. Full rating from 0°C to 50°C, derate linearly to 50% of rating at 71°C.

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Quality Control. In accordance with MIL-I-45208.

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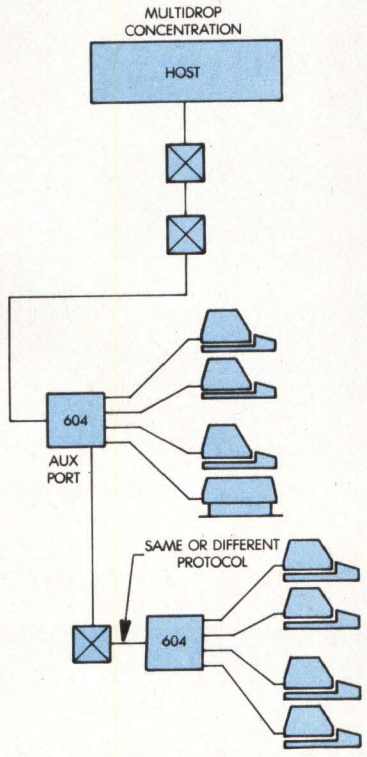
CIRCLE 23 ON INQUIRY CARD

The central memory receives and stores information from various sources, and sends data to users on demand. While using the public switched telephone network as a medium, the system also uses facilities of the GTE Telenet packet-switched network, said to be a first for such a system.

Programmable Concentrator Services up to Sixteen Terminal Ports



Typical programmable concentrator configuration. Unit provides 4 to 16 ports, multiple protocols, and automatic self diagnostics, for multiple site networking, communications monitoring or logging, and interconnection of otherwise incompatible computers and terminals

For networks operating under host computer or terminal protocols, COMDATA model 600 can support a mixture of lines, speeds, protocols, high speed route-through, multidrop, and inter-computer communications. Based on dual 8085A microprocessor architecture, the unit can operate four to 16 terminal ports, each of which may use a separate protocol and unique speed, parity, and control hierarchy. The concentrator is a product of Tectran Corp Pty Ltd, 83 York St, Sydney, NSW, Australia 2000.

A frontend 8085A services the high speed (19.2k bits/s max) primary link, which may communicate with a host computer or another model 600. Asynchronous, synchronous, and binary synchronous protocols may be programmed, including X.25 and other frame-oriented standards.

Terminal ports are serviced by the backend microprocessor which monitors port activity, allocates prime link availability, and manages protocol requirements under control of a realtime executive program. Terminal port speed is 9600 bits/s max.

A special auxiliary port is supplied on all models to provide transparent route-through, protocol conversion, interactive reconfiguration, network monitor and error statistics collection, data capture, or batch store and forward capabilities. The auxiliary port may be synchronous or asynchronous.

Other features include integral self-diagnostics, modular construction, and a 4-char system status display for operator information. Terminal port characteristics can be factory set, on-site loaded or altered, or downline loaded. CIRCLE 400 ON INQUIRY CARD

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The new demands of digital logic are what Bill Moore, Biomation's first chief engineer, had in mind when he developed the logic analyzer, back in '73. He called it a "glitch fixer," designed to track and unravel the mysterious electronic glitches that plague digital logic designs.

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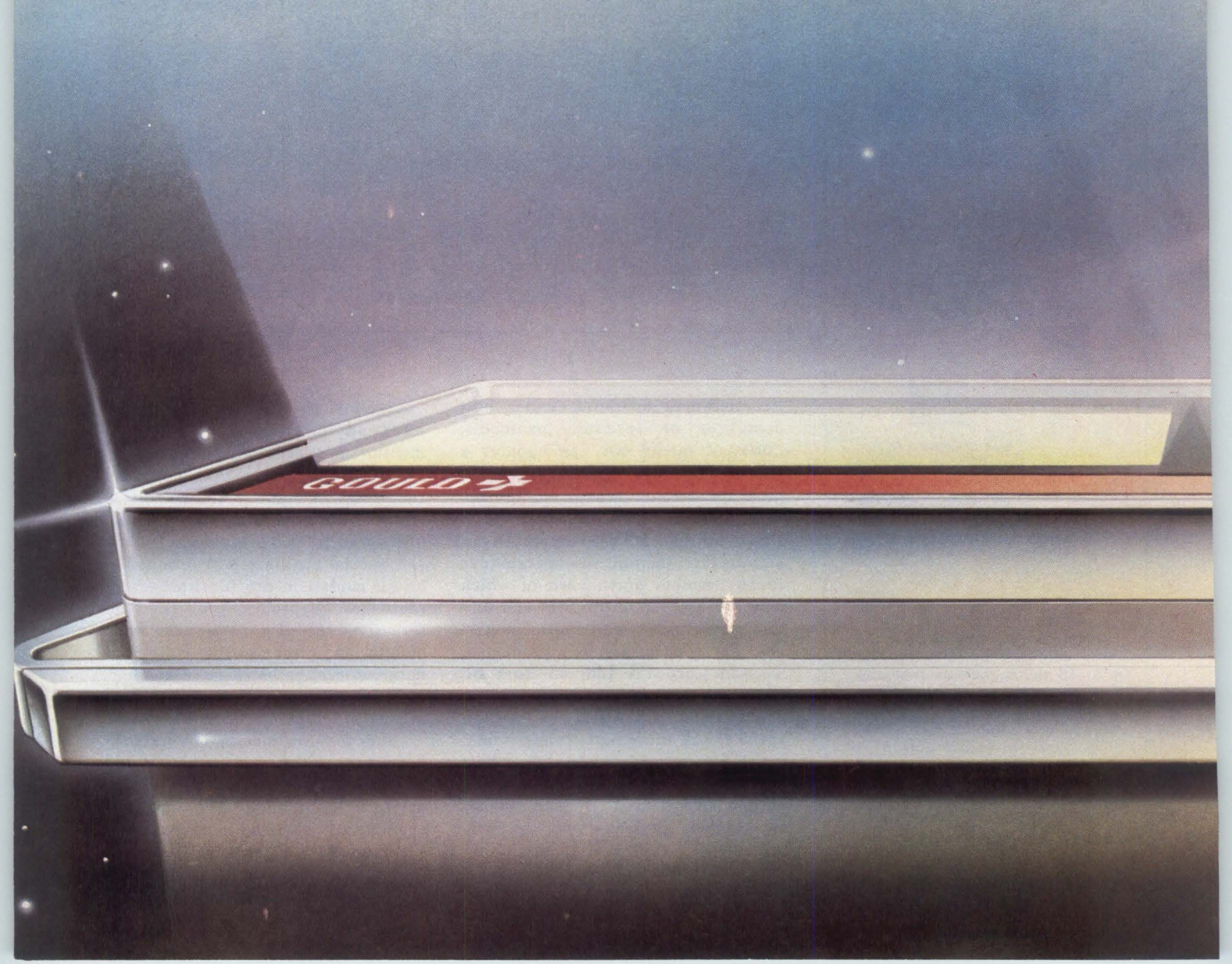

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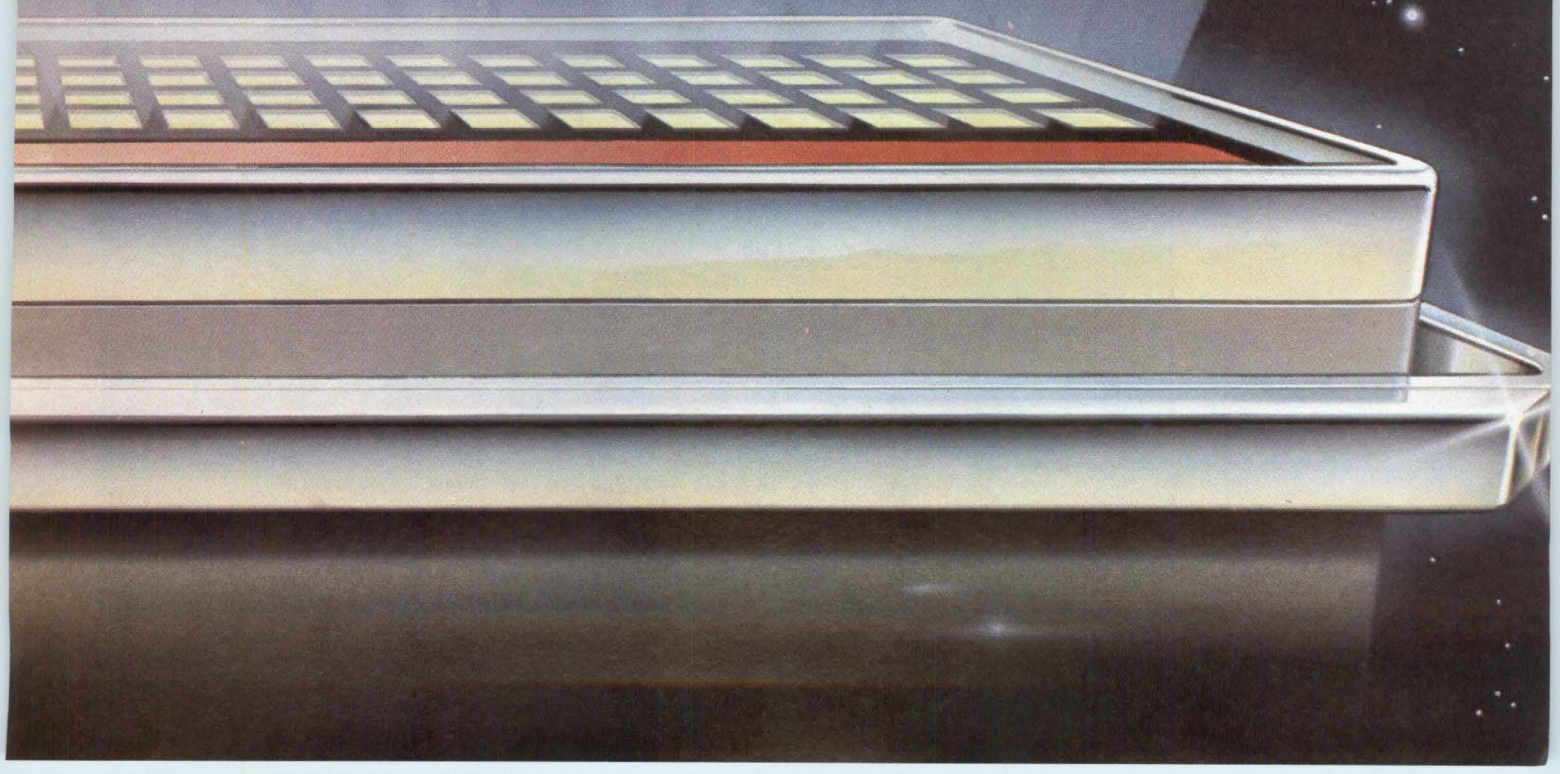
CIRCLE 25 ON INQUIRY CARD



Computer Communication System Provides Voice Response

Especially suited to applications where a data base is accessed by a large number of calls per day and where response to an entry or inquiry is short and straightforward, the ADC2000 general purpose communications processor is designed to interface audio/data communications via TouchTone® telephones into a variety of teleprocessing networks. It is comprised of up to eight ADC1500 microprocessor based buffered terminal controllers that provide computer voice response to remote terminal devices, and an ADC1700 control unit, that processes incoming calls, and interfaces incoming lines from the 1500s with the host computer. The system is available from Wavetek Data Communications, PO Box 651, San Diego, CA 92112.

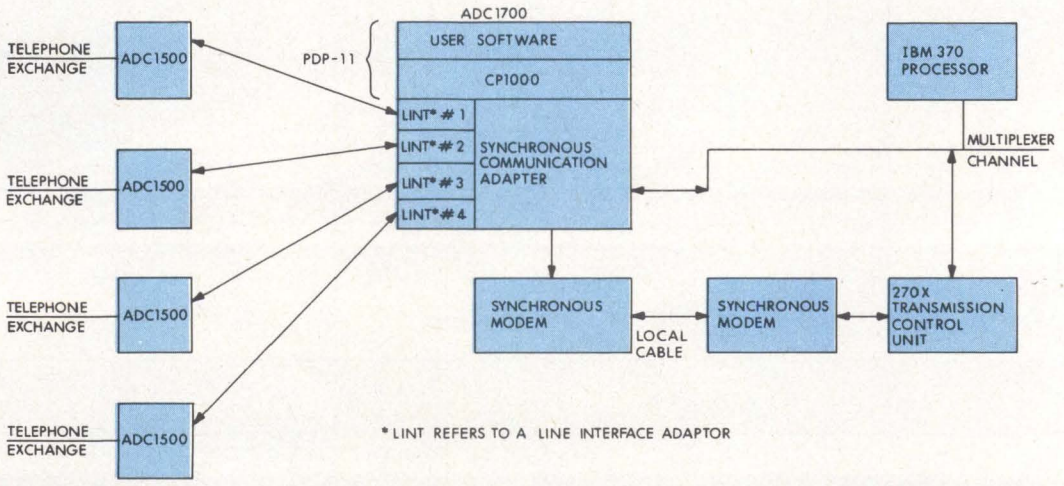
The 1500 is a multifunctioned microprocessor based general purpose controller which, when linked between the 1700 control unit and the telephone system, provides computer voice response to remote terminal devices. It can perform I/O operations on up to 32 telephone lines simultaneously, and has a vocabulary of up to 940 words and/or phrases. The 1500 multiplexes terminal lines through a single serial communications channel.

An integral data set receiver accepts serial TouchTone data, translates them into digital information, and buffers it pending transfer to its microprocessor. It also receives information from the microprocessor, converts it to a form suitable to the terminal, and transfers it to the user in either voice or "beep" response. The beep indicates reception of data and reduces computer turnaround time. The unit will also transmit frequency shift key (FSK) signals at 150 or 300 baud. The data set receiver manipulates all control signals relevant to the terminal, modem, or data access device to which it is attached.

The 1700 control unit, based on a DEC PDP-11 minicomputer, processes incoming calls, and interfaces the host computer to the incoming lines from the 1500s. Memory capacity ranges from 16k to 128k words, depending on the number of 1500s in the system. The control unit includes a floppy disc for program load and a DecWriter II™ for console control and data logging. In a standalone environment, a disc/mag tape system captures the data.

The 1500s can be remotely located from the 1700 via modems over dedicated lines. Data integrity is preserved by use of an asynchronous protocol with error checking between the 1500 and the 1700, and by bisynchronous protocols between the 1700 and the host.

CIRCLE 401 ON INQUIRY CARD



ADC2000 system concept. 1700 control unit connects to host processor in three ways: direct attachment to IBM 360/370 byte multiplexer channel; by single 9600-bit/s bisynchronous link to transmission control unit already on channel; or by BSC 3 link

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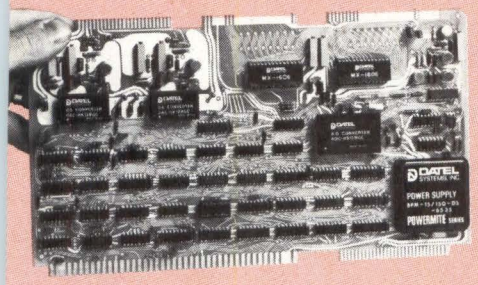

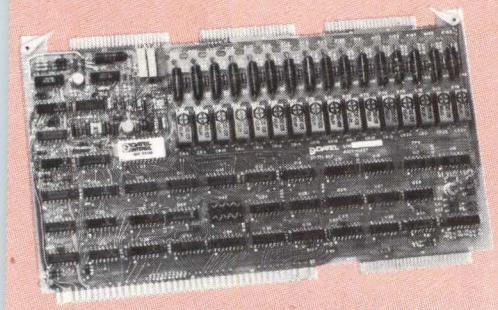

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(NON-ISOLATED)

- Model ST-711: 32S/16D A/D Channels, no D/A Channels ..... $625 (Singles)
- Model ST-732: 32S/16D A/D Channels, includes 2 D/A Channels plus current loop outputs ..... $788 (Singles)
- Full mechanical, electrical, and pinout compatibility to Intel's SBC-711/732 Analog I/O Boards.
- Operates with all Multibus and SBC-Series compatible microcomputers including the 16-bit SBC-86/12 (except SBC-80/04).
- Works directly from Intel's RMX-80 Analog I/O Driver operating software.
- Includes program-gatable Pacer start clock, 1 mS to 1 sec., crystal-controlled.
- A/D inputs accept up to 16 user-installed shunts for 4-20 mA etc. current inputs.
- Differential amplifier for high gain up to X1000 (10 mV full scale range).
- Includes Programmable Gain Amplifier.
- Includes Diagnostic Program tape for immediate TTY or CRT print-out.
- 12 bit binary conversion; 20 microsecond throughput period.

ST-711RLY8D ..... $683 SINGLES
ST-711RLY16D ... $1045 SINGLES

(ISOLATED)

- 8 or 16 differential A/D channels using a "Flying Capacitor" relay multiplexer for high common mode noise rejection (126 dB) and high isolation (±250V RMS).
- Complete hardware and software compatibility to Multibus and SBC-Series microcomputers. Uses identical programming and register assignments to SBC-711/732, and ST-711/732 A/D-D/A boards.
- 10 mV to 2V input ranges including Programmable Gain Amplifier. 12 binary bit A/D resolution.
- Includes Diagnostic Program for immediate TTY or CRT printout.
- Includes 10-stage Pacer Start Clock.
- ST-711RLY8D (8 Channels) $683, singles
- ST-711RLY16D (16 Channels) $1045, singles

ST-724 ..... $595 SINGLES

- 4 D/A Channels plus 4 4-20 mA current loop amplifiers.
- 12 binary bits, Multibus compatible.

Datel Price Savings:

	Datel	Intel*	
	ST-711, $625	SBC-711, $1180	*7/16/79
	ST-732, $788	SBC-732, $1420	OEM prices, 1-9
	ST-724, $595	SBC-724, $1105	

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INTEL, MULTIBUS AND RMX-80 ARE TRADEMARKS OF INTEL CORP.

CIRCLE 26 ON INQUIRY CARD

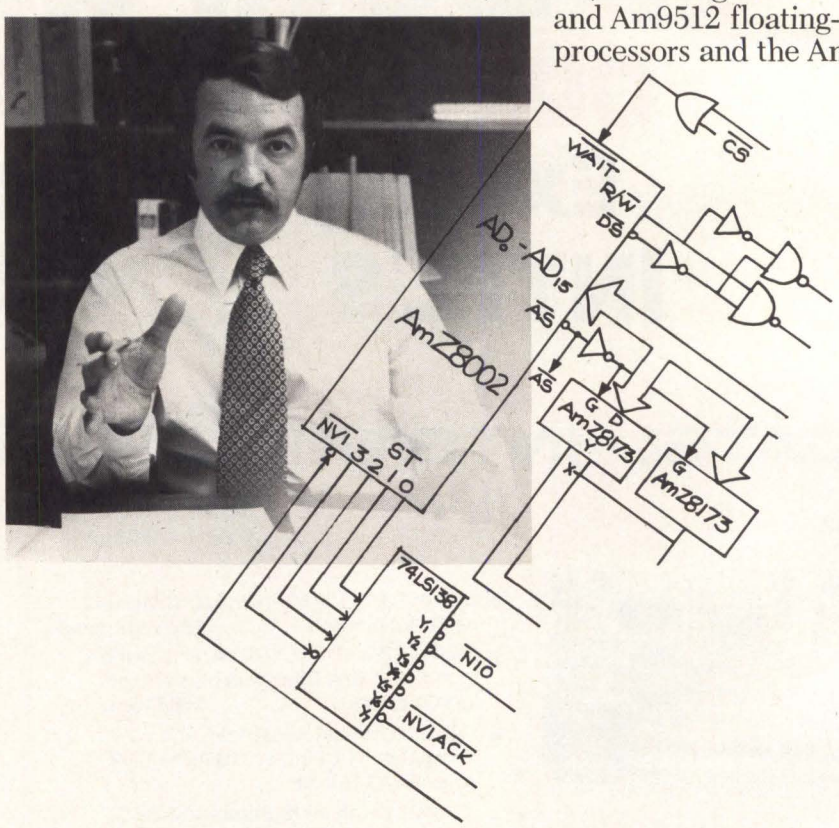
Choosing a 16-bit MPU is no easy job. We know. We went through it ourselves back in '78.

We chose the Z8000 because we believed you'd choose the Z8000. Because it's better. Here's why:

"The AmZ8000 has a better architecture."

It has 16 registers. All general. All for you. Use them for data or addresses. Use them to write more efficient software with less code and faster execution.

The AmZ8000 has gobs of address space: 8M bytes of direct addressing in each of four possible address spaces. It has memory management with sophisticated relocation and protection features. It has a rich instruction set that operates on data types from quad length words right down to single bits. You can even map the I/O into memory or keep it separate.



Sven Simonsen, Vice President and Technical Director, Advanced Micro Devices

As if all that weren't enough, the AmZ8000 has a whole series of string-oriented instructions to move, translate or compare up to 64K bytes of data in a single instruction.

"The AmZ8000 has a better future."

The AmZ8000's architecture and instructions fit perfectly with today's computation, communications and instrumentation markets. So do the peripherals. And all the popular existing parts for the 8080A/8085A, including the Am9511A and Am9512 floating-point processors and the Am9517A

"The AmZ8000 is better for your application."

DMA circuit, work great with the AmZ8000.

There's a CPU that's just right for you. For imbedded controllers, where 64K of memory is enough, there's a compact 40-pin CPU that uses less memory for programs. For addressing large memory spaces, there's a 48-pin CPU that's software compatible.

But best of all, we're getting ready to introduce a bunch of new bipolar and MOS peripherals. There's an I/O device with a built-in FIFO, a chained DMA controller, error correction circuits and an editing CRT controller, just to name a few.

As technology develops, newer and better software-compatible CPUs with higher throughput will be coming your way.

"The AmZ8000 has better support."

We know you need supporting documentation. And we've got it. Ask us for our Data Book, our Processor Interface Manual and our Processor Instruction Manual.

We know you need software development tools. And we've got them, too. There's our macro assembler with powerful high-level constructs and a relocatable linking loader, and a PASCAL compiler. Cross-software is available, too.

If you need a hardware development system, our AmSYS8/8 with in-circuit emulator was designed just for the AmZ8000. So was our Am96/4016 Evaluation Board. (To learn all about them, come to one of our field seminars or take one of the courses offered by our Education Department.)

And soon, you'll need parts. With the AmZ8000 you've got two major U.S. manufacturers with a mask-exchange agreement. We have international partners, also. When you need parts, we'll be there.

"The AmZ8000 is better because we're better."

Advanced Micro Devices didn't become the nation's fastest growing IC company by accident. We did it by design. We only manufacture high-quality, high-volume parts. And from the day we opened for business, we've thrown in a freebie with every order: MIL-STD-883.

If you want your application to be better, get the MPU that's better. Get the AmZ8000. It's the best 16-bit family for you.

Advanced Micro Devices

901 Thompson Place · Sunnyvale, CA 94086 · Telephone (408) 732-2400

Visit AMD at the Paris Salon International des Composants Electroniques, March 27 thru April 2, Hall 1, Aisle 8, Stand 41.

Coaxial Packet Network Links Office Equipment

A passive communications medium, Ethernet,* for linking different types of office equipment used at business sites, has been announced by Xerox Corp, Stamford, CT 06904. The network allows each element of an office system, such as a workstation, printer, or disc file, to exchange information with any other element. One unit may also send a message to a selected group of other stations in the network, or a document may be created at one workstation and be printed at other locations. Ethernet has no switching logic and is not controlled by a central computer; it simply accepts and passes on transmissions from attached system elements. If one element fails, others are not affected.

The network consists of a coaxial cable made up of one or more segments typically several hundred meters long, and a communication transceiver for each element in the office system. Each transceiver is under control of its attached element, which has a unique address. Information is transmitted in packets, and each packet includes the message data, the address of the destination, and the address of the source. Each transceiver monitors the network before transmission to make sure it is idle, and during transmission to detect interference due to transmission by another element. If interference occurs, the packet is retransmitted when the network is clear.

In receiving data, each element recognizes and accepts messages with its own address, and ignores others. On the completion of a transmission, the receiving station sends an acknowledgment message to the sender.

Ethernet is used to connect system elements within a building. Other transceivers with associated processors can be used to connect separate Ethernet networks to each other, and to outside facilities for long distance communication. Each Ethernet itself has a unique address that is used in internetwork communications. Once a packet has passed from one network to another, it is handled identically to one sent locally.

The 860 information processing system, recently announced by the company's Office Products Div, will be the first commercial product to use Ethernet. Interconnection of 860 system elements via the network is scheduled for fourth quarter 1980.

*R. M. Metcalfe and D. R. Boggs, "Ethernet: Distributed Packet Switching for Local Computer Networks," *Communications of the ACM*, July 1976, pp 395-404

CIRCLE 402 ON INQUIRY CARD

IBM Hosts and RJE Terminals Supported by New Service

Rates have been filed for Datapac 3304, a new access service to the Datapac network, by the Computer Communications Group (CCG) of the TransCanada Telephone System (TCTS), 160 Elgin St, Ottawa, Ontario K1G 3J4. Datapac is the TCTS packet-switched data transmission network.

The new service is designed to support IBM-compatible host computers and remote job entry (RJE) terminals. It supports the IBM binary synchronous (BSC) multi-leaving communications protocol as implemented by CCG for Datapac access. Principal users of the service will be service bureaus, government, and large business organizations with customers or branches using the services of a central computer.

A main objective of Datapac 3304 is to support multi-leaving terminals with a minimum of changes. Terminal-network connection is via a network interface machine (NIM), which supports the multi-leaving protocol and converts data blocks to packets and vice-versa. Each dedicated 3304 access line offers 2400-, 4800-, and 9600-bit/s transmission speeds.

Two methods of host to network interface are provided. Transparent communications may be established between an RJE configuration and a host without modification to customer equipment, software, or operation. A NIM-supported dedicated 3304 synchronous access line is connected to the network from each host port or RJE terminal. In non-transparent communications (customers whose host subscribes to Datapac 3000 access and whose terminals subscribe to 3304) the host will connect to the network using CCG's X.25-compatible standard network access protocol.

CCG says the new service will afford reliability, lower communication costs, and better utilization of computer resources. □

Grayhill's New
SEALED KEYBOARDS
SPILLPROOF! TACTILE FEEDBACK! LONG LIFE!

ACTUAL SIZE

Here . . . at last . . .
a sealed keyboard that lets you hear and feel the actuation!

These new Grayhill Series 88 sealed keyboards are available now in 3x4 and 4x4 button configurations with one-half inch button centers. The graphic overlay, which seals the keyboard surface and the contact system, resists the vast majority of common contaminants. Thus, these keyboards can be used out-doors as well as in applications that require a washable front surface. Graphic overlays come in a variety of standard colors and formats; custom nameplates can also be provided.

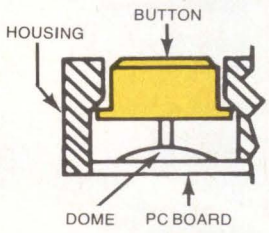
Grayhill Series 88 keyboards are flange mounted. Special gaskets seal the flange surface for either front panel or sub-panel mounting.

The Grayhill Series 88 electrical characteristics have been designed to be compatible with logic circuitry and are rated at 3,000,000 operations per button. The Series 88 is offered with matrix, 2 out of 7, 2 out of 8, or single pole/common bus circuitry. The snap dome contact system provides positive audible and tactile feedback to the operator.

Engineering data and prices are yours for the asking in Bulletin No. 297.

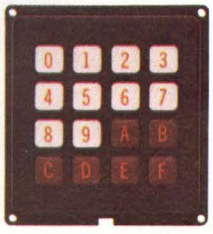
Spill-proof, contamination-proof

Snap-dome contacts give positive operator feedback



One of five standard 3x4 legends

One of four standard 4x4 legends



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CIRCLE 28 ON INQUIRY CARD

Sure Winners

Competitive systems start with Intel® static RAMs. Now you can choose a champion for any design.

High performance memory design is a fast track. The winners are those who match advanced components precisely with today's system requirements. When it comes to static memory, only one supplier has the broad selection of high speed, low power RAMs, and the delivery you need to bring your product to market ahead of the field.

Over 50 Purebred RAMs

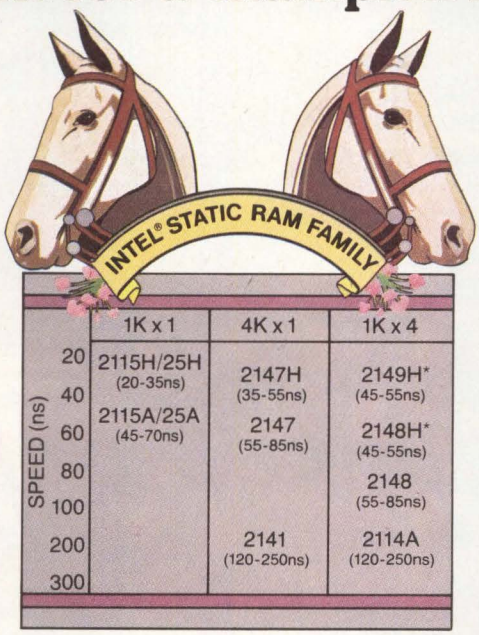
From the beginning, Intel has been the leader in practical, producible MOS memory technology. First NMOS. Then high performance HMOS,* the high reliability technology that's produced more than 14 million fast static RAMs —as well as our industry standard 16-bit microcomputer, the 8086. Now HMOS II* is here, bringing you the same reliability and a new generation of even higher speed static RAMs.

Today, Intel gives designers the widest selection of 1K and 4K static RAMs in the industry. Over 50 different versions let you tailor speed, power, density and organization precisely to your system requirements.

Record breakers for high speed systems

Nowhere is the precision matching of memory components to function more important than in high speed cache, buffer, control store and main memory. At Intel, you'll find static RAMs to cover your full range of design goals.

*HMOS and HMOS II are patented processes of Intel Corporation.



*Available Q1, 1980

For highest speed and low power, no bipolar can touch our HMOS II 2115H/25H 1K static RAMs. One version gives you record access times of 20ns; three others let you choose speed/power combinations to 35ns. For designs requiring speeds from 45-70ns, our 16-pin industry standard HMOS 2115A/25A series covers the spectrum. All of these 1Ks are pin-compatible replacements for 93415/25 bipolars, and all give you dramatically lower power, too.

In a 4K x 1 format, our HMOS 2147 is the industry standard for low power and speeds to 55ns. Today, designers requiring even higher performance will find a winner in our new HMOS II 2147H—with versions as fast as 35ns and standby power dissipation of only 30mA.

Finally, for special wide-word memories, including control store and bit slice designs, Intel's 1K x 4 bit 2148 is out in front. It gives you all the performance advantages of the HMOS 2147, plus the modularity that lets you save 75% on board space compared with 1K designs. And, you can expect even faster speeds in the future as we apply HMOS II to wide-word memory devices.

Pick the best performer for microcomputers

For years, microcomputer system designers have relied on Intel's 18-pin industry standard 2114 static RAM in 1K x 4 designs. Now we've used HMOS technology to improve performance with our new 2114A. It's a direct descendent of our 2114, but with a 30% smaller die size, 40% faster speeds, and 43% less power dissipation. The 2114A gives you performance equal to that of our 4K x 1 bit 2141, so you get optimum efficiency no matter what modularity you need—no matter how basic or how advanced your microcomputer application.

Intel gets you off and running now

We're delivering all of these fast static RAMs today. To order, or for more information, including our HMOS Reliability Report, RR18, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051.

intel® delivers.

Europe: Intel International, Brussels, Belgium. Japan: Intel Japan, Tokyo. United States and Canadian distributors: Arrow Electronics, Alliance, Almac/Stroum, Component Specialties, Cramer, Hamilton/Avnet, Harvey, Industrial Components, Pioneer, Wyle/Elmar, Wyle/Liberty, L.A. Varah and Zentronics.

CIRCLE 29 ON INQUIRY CARD

HEWLETT-PACKARD® TAPE SPEED BARRIER BROKEN BY DATUM

Need more speed than 45 ips for your Hewlett-Packard system? Datum breaks the speed barrier with compatible vacuum column tape systems operating at 75 and 125 ips, as well as 45 ips. Dual Density is standard in all 3 speed configurations.

A new concept in tape subsystems, the 1041 Series is compatible with Hewlett-Packard Models 1000, 2100, 2114, 2115, 2116 and 2100 MX minicomputers. A single EIA rack-mounted external controller is the heart of the Datum system.

Along with increased system thru-put, Datum's Series 1041 offers you multi-transport operation using NRZI and/or PE formats. Up to four tape transports may be driven by each controller.

And we're software transparent to all Hewlett-Packard operating systems.

See Datum break the Hewlett-Packard tape speed barrier for yourself; contact your local Datum sales representative or headquarters today. And Datum gives you one more very special benefit. A superior price/performance ratio!

125

75

45

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PPD 107

CIRCLE 30 ON INQUIRY CARD

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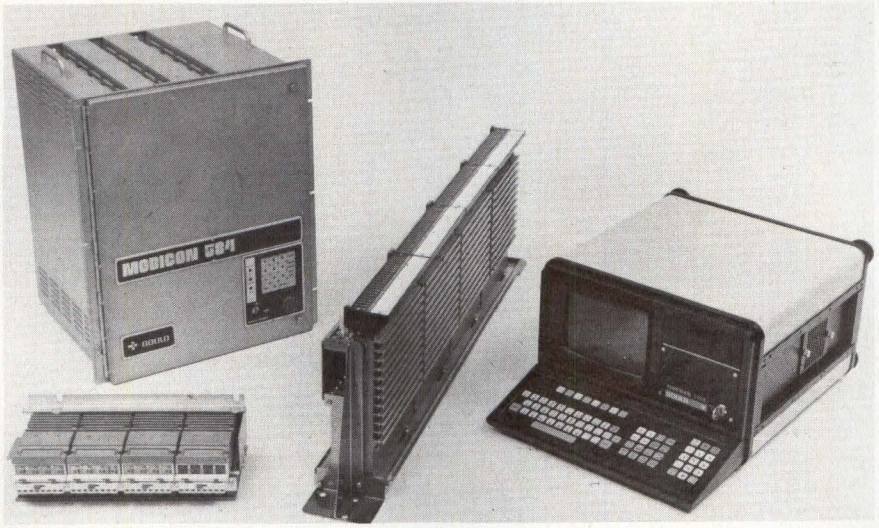
TECHNOLOGY REVIEW

Programmable Control System Decreases Maintenance And Operating Costs



584 control system (left rear) uses P190 programming panel (right) for entry of control logic in form of relay ladder diagrams, as well as 200 and 500 series I/O modules. Modules provide 4 or 16 input or output circuits each and contain circuitry to optically isolate and convert field voltages to signal levels compatible with processor

The 584 programmable controller uses state of the art technology to provide reliable solutions to a variety of control problems in a unit built to stand up on the factory floor. Developed by the Modicon Div of Gould Inc, 155 W Big Beaver Rd, Suite 104, Troy, MI 48084, the mainframe contains 32k of memory, two MODBUS communications ports, register access panel, and drivers for 4096 I/O points. It incorporates capability to increase productivity, decrease maintenance/operating costs, and reduce cost of implementation.

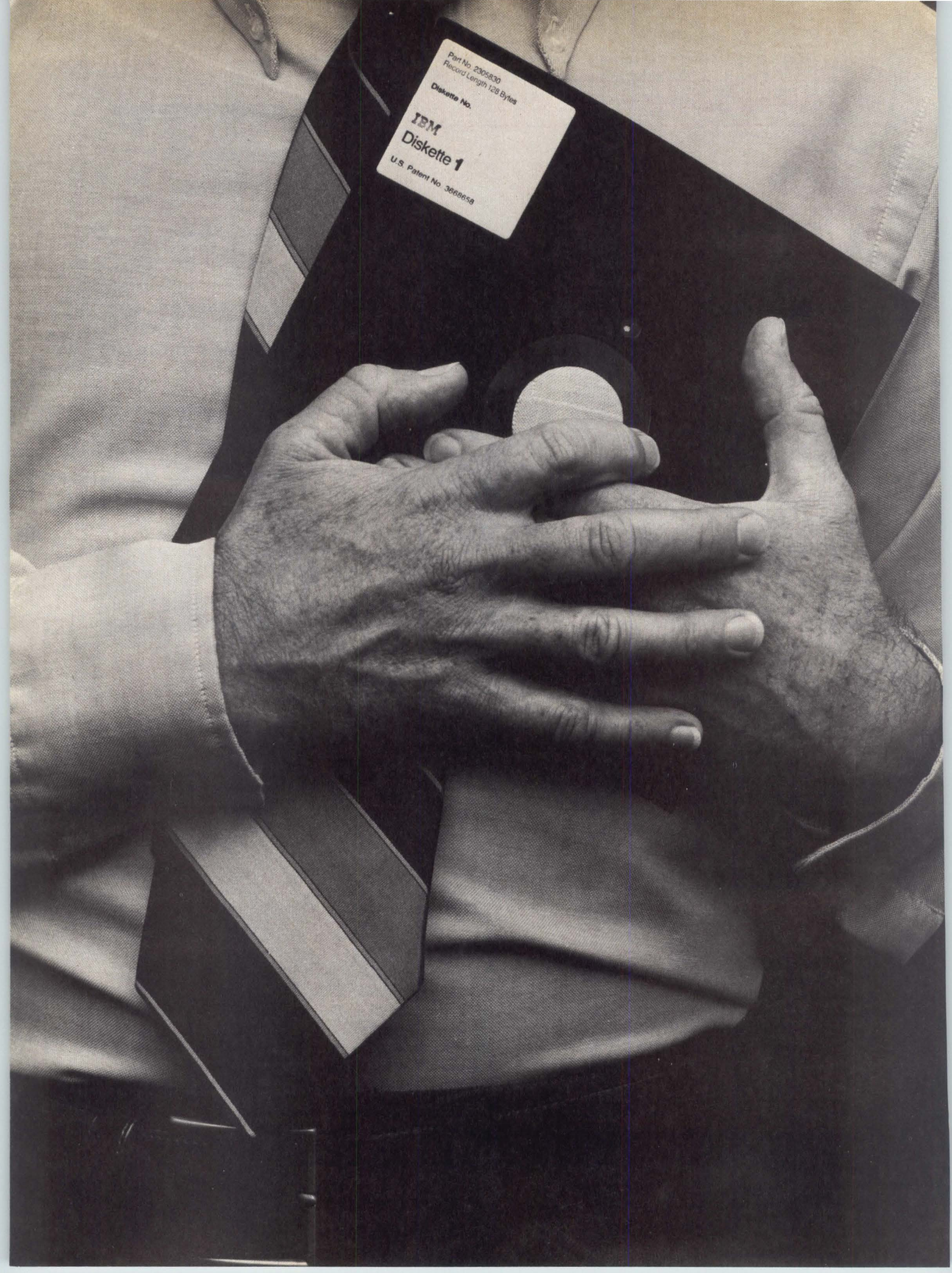
In addition to serving as an alternative to relays, counters, and timers for sequential and interlock control systems—traditional programmable controller functions—the unit can perform computer like calculations as well as control and reporting functions on analog and numeric data. It includes functions to simplify diagnostic (machine) monitoring and distributed control. Sufficient memory, I/O capacity, and speed are incorporated to allow for applications growth.

When control system equipment malfunctions, a limit switch or motor starter is normally at fault. The 584 provides indicators and displays to allow the problem to be diagnosed visually without external meters, programmers, or oscilloscopes. In addition, optional diagnostic logic can reside within the unit to detect, identify, and report faults as they occur. Repair by replacement procedures allow production to resume quickly if an internal component fails.

Using a set of logic and wiring diagrams the plant electrician can use field circuit indicators provided on the I/O modules to check limit switches and motor starters, for example. At the 584 mainframe the built in register access panel (RAP) verifies that circuits are operating properly.

The RAP displays any logic, analog, or numeric signal coming from or entering the controllers as well as preset and internal data. Internal values and outgoing signals can be manually overridden to facilitate troubleshooting.

Diagnostic monitoring implemented within the controller will provide preprogrammed logic checks to pinpoint failures. These diagnostics are


Part No. 2305830
Record Length 128 Bytes
Diskette No.
IBM
Diskette 1
U.S. Patent No. 3668658

Data Warehouse. When Floppies aren't enough. But you can't live without them.

There comes a time when your system outgrows flexible disk drives.

You need more storage capacity and higher throughput. But you don't want to give up the input/output convenience of floppies.

The Remex Data Warehouse storage system just solved this dilemma. It gives your system 20MB Winchester capacity, reliability and speed. Plus, it gives you the flexibility of floppies.

And Remex put it all together in one self-contained package under the common command of an advanced controller/formatter.

THE BRAINS BEHIND THE DATA WAREHOUSE.

The most complex and time-consuming task in building your own disk subsystem is designing the controller. We've done it for you.

Our very intelligent, microprocessor-based controller gets you to market quickly, with "capabilities previously associated only with large disk-oriented systems," to quote *Computer Design* magazine.

In fact, our built-in controller is so powerful that it increases throughput by *40% or more* over existing systems.

Normally about half of I/O overhead is between CPU and disk. We've cut these communications to a bare minimum with techniques such as DMA (direct memory access) of commands and status, as well as data.

PACKET POWER SUPER-CHARGES YOUR SYSTEM.

Whenever data is transferred to or from the disk, the controller retrieves packets containing all command data via DMA. The starting memory address of these packets is stored in the programmed I/O portion of the CPU. And that's all the CPU needs to instruct the controller to retrieve data, perform functions, transfer data and communicate status of that function to the CPU. When the function is complete, the controller returns the starting memory address of the packet to the CPU.

With DMA, multiple sector transfers of up to 64K words are accomplished with a single command.

The Data Warehouse also copies "off-line" so that updated or newly-created files can be safely stored outside the system.

Simply, the Data Warehouse distributes intelligence to the disk and frees your CPU for computing.

AVAILABLE NOW. SO YOU DON'T HAVE TO LIVE WITHOUT IT.

The Data Warehouse is built for 19" rack mounting and includes its own power supply. Only one CPU slot is needed for interfacing. And a variety of interface cards for mini-computers and microprocessors are available.

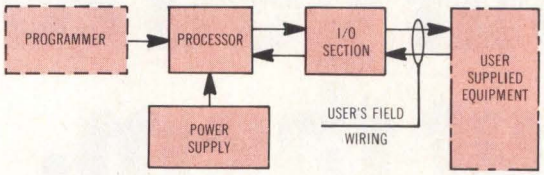
Best of all, Data Warehouse is available today in OEM quantities. Write Remex Division, Ex-Cell-O Corporation, 1733 East Alton Avenue, P.O. Box C19533, Irvine, CA 92713. Or call (714) 957-0039.

Ex-Cell-O Corporation

REMEX DIVISION

DATA WAREHOUSE

CIRCLE 32 ON INQUIRY CARD



Modicon's 585 programmable controller contains four basic components. Processor consists of I/O processor which communicates to I/O section and provides controller's fixed intelligence; processor which makes all logical decisions for controller; and memory board which stores system parameters, programmed logic, and numerical values

capable of finding problems that do not stop the equipment, (eg, excessively long machine or process cycles) and can detect faulty I/O modules and field devices.

Expanding from a 50-relay system to over 2000 relay equivalents, the 584 controller can provide relay replacement, data collection/storage, and report generation. Basic components consist of mainframe power supply, I/O section, and programmer. The processor is a solid state device made up of three PC boards: the I/O processor, controller processor, and memory board. An access port on the mainframe connecting to the processor is used to enter logic and data or to monitor previously entered information. A keyboard/display panel allows the operator to examine any logic coil or discrete input or the contents of any input or holding register.

Serving as the primary interface to user supplied devices, the I/O section offers modules with 4 or 16 circuits each. 16-circuit modules provide complete error checking by redundant transmissions and standard echo check. With the 4-circuit modules, sensors are provided on the local bus communications from the interface to detect hardware bus faults. Modules can be removed and replaced without interrupting field power.

The controller is programmed through the P190 CRT programmer which incorporates 9" (22.9-cm) CRT screen and a character generator designed specifically for relay ladder diagram displays. A tape device and ASCII keyboard are also incorporated. This unit connects directly to the controller, permitting it to be programmed in relay symbology.

Designed for use on the plant floor, the 584 can handle 60 °C ambient temperatures at 95% relative humidity and high levels of emi and rfi with no special shielding requirements. The unit's two MODBUS communications ports provide simple connection to CRT programmer and supervisory computers. The system produces extensive ladder listing tools that document the system's logic, greatly reducing the time, effort, and cost of documenting an evolving system.

CIRCLE 270 ON INQUIRY CARD

BRAIN CELLS.

Employed by smart engineers for reliable, dependable, rechargeable power.

Now available in four, basic 2V cell sizes, ranging from 2.5 to 25Ah, for dozens of battery configurations and hundreds of applications.

With outstanding float and cyclical characteristics and superior storage life.

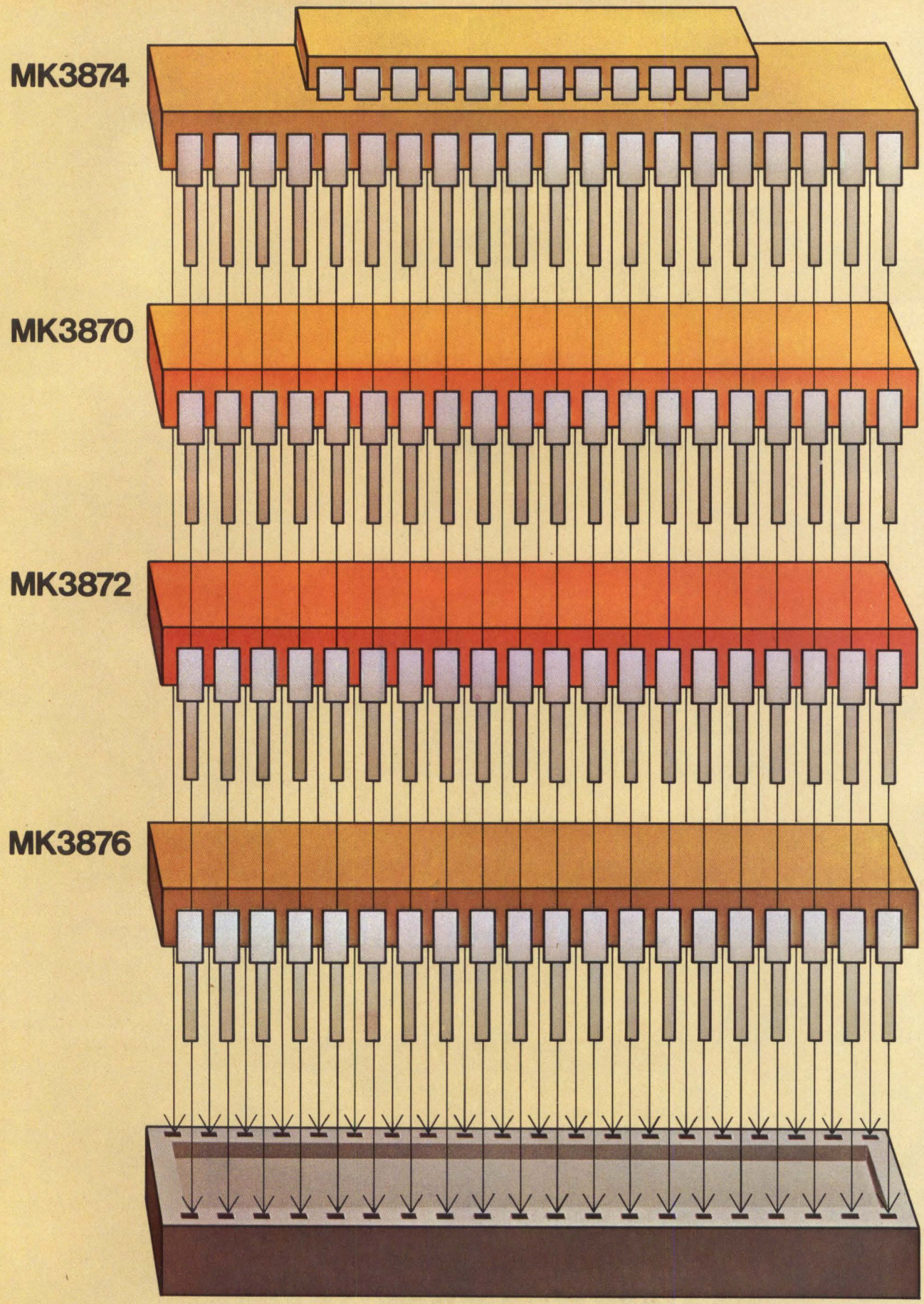
All invented, manufactured and refined by Gates Energy.

Be wise. Contact Gates Energy Products Inc., 1050 S. Broadway, P.O. Box 5887, Denver, CO 80217. Phone (303) 744-4806.

GATES ENERGY

CIRCLE 34 ON INQUIRY CARD

Circle our number on the reader service card for additional input.


MK3874
MK3870
MK3872
MK3876

Microcomputer Momentum.

Capture it with Mostek's 3870 family of pin compatible microcomputers.

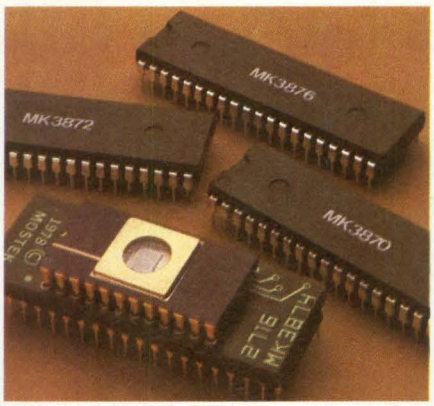
For single chip applications, no other microcomputer family can offer you more design momentum than Mostek's 3870. None.

Consider: When properly designed in, any 3870 family device may be replaced with any other 3870 family member in the same socket without hardware redesign. We call the concept in-socket expandability.

Let's say you start with the 2K bytes of ROM and the 64 bytes of RAM in the 3870. Need more RAM? Double it with the 3876. In the same socket. Need more ROM and RAM? Get 4032 bytes of ROM and 128 bytes of RAM with the 3872. In the same socket. Want to prototype and test your systems prior to ordering mask ROM programs? Plug in the 3874 with its piggyback EPROM and emulate all 3870 family members. In the same socket.

The right idea for a fresh start.

As a new design path, the advantages are compelling, too. Not only does the 3870 offer you a variety of choices for the initial design, but it also simplifies planning for subsequent designs as well. In the same socket, expansion or upgrading can be accomplished as easily as exchanging one 3870 family device for another. There's no new architecture to learn. No retooling of artwork. No new software to buy. No concerns about debugging. No new vendors to qualify. Simply stated, there's no loss of momentum.



Design it in with confidence.

Mostek's 3870 is the proven 8-bit single chip microcomputer industry standard. Over a million parts have already been shipped. For hundreds of applications. From microfilm recorders and electrocardiographs, to appliances, computer peripherals, and more. Supported by multiple second-sources, the 3870 has made a whole new technology affordable for scores of cost-sensitive applications.

It's a powerful way to design.

All the pin-for-pin compatible 3870 family members operate on a single +5 Volt power supply. All standard members have 32 lines (4 ports) of bidirectional I/O. Or you can order the standby power option to protect the extra 64 bytes of RAM in the 3872 or the 3876, and still have 30 I/O lines available. The versatile programmable binary timer can operate in three modes: internal timer, pulse width measurement, and event counter mode. And the compact instruction set has over 41 single byte instructions letting you do more in less memory.

All our 3870 family members are supported with complete development systems. Choose from the economical EVAL-70™ all the way up to our Matrix™ floppy disk development system with real time in-circuit emulation.

Mostek 3870 Family

Product	ROM	RAM	I/O	Power
MK3870	2048x8	64x8	32	+5V
MK3872	4032x8	128x8	32/30*	+5V
MK3874	2048x8 or 4032x8	64x8 or 128x8	32/30*	+5V
MK3876	2048x8	128x8	32/30*	+5V

*with standby power mode option

An intelligent choice for the future.

To continue the momentum, more 3870 family members will be available soon. Including CMOS versions. And the 3873 serial I/O version which will interface to devices such as terminals, shift registers, and CCD memories.

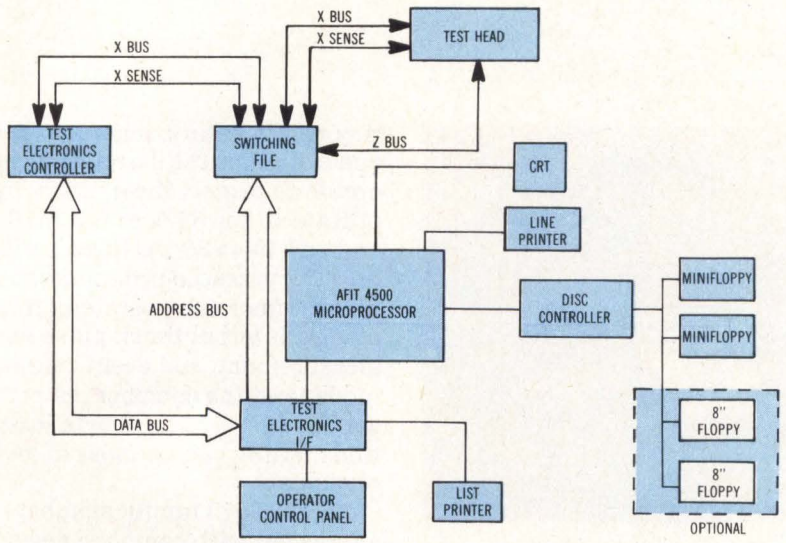
If you want an intelligent design for the future, start with the microcomputer family that has expandable designs for the future: Mostek's 3870 family.

For more information, write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006. Or phone (214) 323-6000. In Europe, contact Mostek Brussels, phone 660.69.24.

MOSTEK.

CIRCLE 35 ON INQUIRY CARD

Flexible Test System Detects Shorts/Opens In Bare or Loaded PCBs



Providing capability for from 2400 to 4096 test points, AFIT 4500 shorts/continuity tester from Fairchild is self-programmable from known-good board. Tester controls voltage to device under test in three ranges, and has dual-solenoid/dual-port option that allows testing of two devices on same fixture

Production throughput is increased by using the AFIT® (automatic fault isolation tester) 4500 to detect continuity and shorts in bare and loaded PC boards before transferring them to in circuit, functional, or system testing. Introduced by the Subassembly Test Systems Div of Fairchild Camera and Instrument Corp, Testline Instruments Facility, 1400 White Dr, Titusville, FL 32780, the system has a basic 2400 test point capability, expandable to 4096 in increments of 128, and can test at a rate of 6 to 10 s for a 2400-point board.

Typically, one of three loaded printed circuit boards contains defects that cause the board to fail after the soldering process; 50% of these failures are attributable to shorts. By testing boards with a shorts/continuity tester, nonproductive sorting and recycling of loaded boards through test systems is minimized, and throughput and utilization of existing in circuit, functional, and systems testers is increased.

The system's basic 2400 test point capability expands to a maximum of 4096 points in increments of 128 points. A dual-solenoid/dual-port option allows alternate testing of two boards on a single bed-of-nails fixture.

The unit is self-programmable from a known-good board. The system learns board topology, generates a test sequence, and transfers it to a minifloppy disc for storage. Test program generation typically requires from 8 to 10 min.

Voltage to the devices is controlled by the tester, keeping it low enough to test devices without damage. Selection of three crossover points is available to increase flexibility and to prevent unintentional turnon damage to devices on the board. Selections are 10 Ω ±20% at 50 mV, 100 Ω ±20% at 100 mV, and 1 kΩ ±20% at 2.5 V.

Single-density minifloppy discs used for program storage can hold up to ten 2400-point self-learn format programs or three in self-learn format with full translation to user printed circuit board pin code.

The system is configured as a 2-bay unit; error printout tape, test fixture, CRT, and operator control unit are located on the tabletop. Base price of a system configured for 2400 points is $39,000. **CIRCLE 271 ON INQUIRY CARD**

Standalone Small Business Computer Offers Growth Potential

Competing with small and midsize IBM Systems/34 and /38 models, Univac BC7, and some NCR and Burroughs units, the System 10, model 320 small business computer provides standalone data processing as well as communications capability. Upward growth potential and immediate cost-effectiveness are claimed by ICL Inc, Distributive Systems Div, 415 E Airport Freeway, Irving, TX 75062 to give the system an advantage against its competition.

All software developed for its predecessor model 220 (see *Computer Design*, Aug 1977, p 46) and other System 10s is fully compatible, creating a sequence of upward compatible machines behind the 320. This provides the small user with an economic growth path that preserves software investment while maintaining advantages of distributed processing and multiprogramming.

A basic model 320 processor has a 60k semiconductor memory that expands to provide as much as 200k of user memory in 60k increments. 60-, 120-, and 180-char/s matrix printers are available as well as 75-, 150-, 300-, and 600-line/min printers. Cartridge module drives have capacity for 60M bytes, while storage module drives provide up to 160M bytes capacity.

Four industry compatible tape drive units are offered. System I/O is accomplished with the standard System 85 video display unit. Under multiprogramming discipline, as many as 20 display stations with associated peripherals can communicate simultaneously with the CPU, each accessing a different program. The standard disc management facility serves as the basic operating system.

Price for a minimum 320 configuration will begin at approximately $35,000. This price will range up to $100,000 or more, depending on the amount of disc memory and peripheral mix chosen.

CIRCLE 272 ON INQUIRY CARD

System Packages Offer Processor Variations, Peripheral Alternatives

Ten low and midrange system packages incorporating CLASSIC 7810, 7830, and 7835 CPUs are intended to operate as a nucleus for larger systems or as standalone systems using MAX III or IV operating systems. Built around the high end CLASSIC 7861 and 7870 CPUs, eight packages offer memory variations from 256k to 1M bytes and disc capacities ranging from 10M to 67M bytes. All packages, put together by Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33310, include maintenance kit, diagnostics, utilities, hardware/software documentation, and installation.

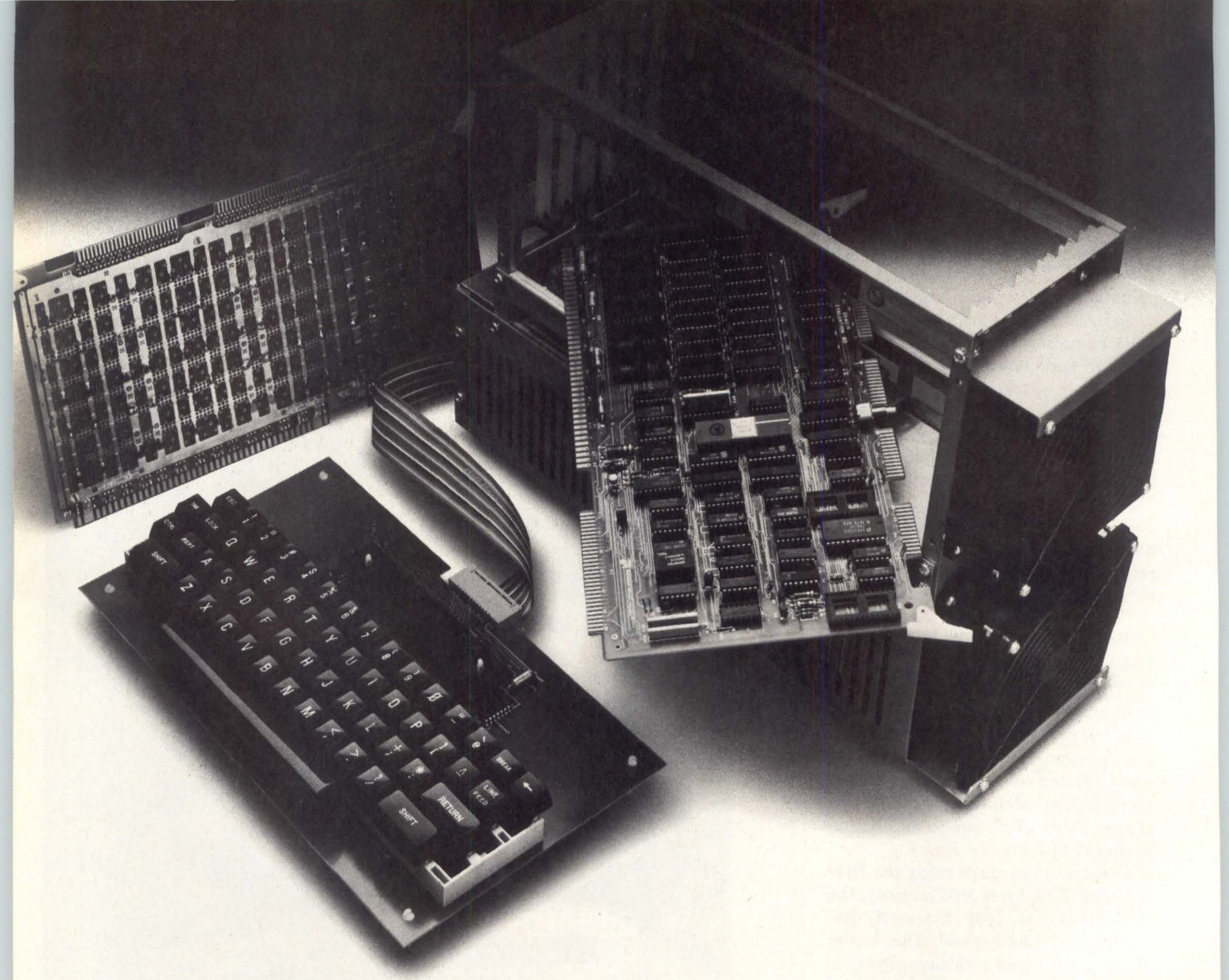
Low and Mid Range Systems

Low end 7810-A10A, built around the 7810 CPU uses MAX III realtime multiprogramming operating system with 128k bytes of parity MOS memory, system protect, and operators control panel. Priced at $23,000, the system also provides 5M of fixed and 5M bytes of removable disc storage and a conventional CRT console device.

A midrange package using the 7830 CPU with 128k-bytes MOS memory, the 7830-A10A has 10M bytes of disc storage, and CRT console. The similar -A10B is equipped with hardcopy console instead of the CRT. Using the same processor, the -A21A package provides 128k bytes of memory, 21M bytes of fixed media moving head disc storage, and a 9-track, 800/1600-bit/in (315/630/cm) magnetic tape subsystem, as well as CRT console. Additional storage is supplied by the -A67A combination which incorporates 67M bytes of high performance removable media disc storage.

Using the MAX IV operating system, the -B20A package offers 256k bytes of memory and 10M bytes of fixed and 10M bytes of removable disc storage. This communications processor and integrated communications subsystem offers direct memory access for up to eight asynchronous or synchronous full duplex channels (expandable to 16) and supports up to four conversational CRT terminals and one hardcopy console.

Built around the 7835 CPU, the midrange -A67A has arithmetic accelerator, uses the MAX III operating



The AmZ8000 is better. And we can prove it.

You've read all about the AmZ8000. You've checked the specs. You've compared it with the other 16-bit MPUs. And you think the AmZ8000 is better.

Now you can prove it.

ADVANCED MICRO DEVICES INTRODUCES THE Am96/4016 EVALUATION BOARD.

The Am96/4016 is a fully assembled and tested evaluation board designed to give you an easy, inexpensive way to put the AmZ8000 through its paces.

Use the Am96/4016 to execute AmZ8000 software at 4MHz. Use its monitor software program for register inspection, reading and changing of memory location, and debugging. Use the optional line-by-line assembler for writing the critical programs you need to prove the feasibility of your system design.

If you want to check out your specific design applications by adding other components, our Am96/6410 board is for you. If you need to add more RAM, the AM96/1064 lets you add up to 64K bytes. If you want a hard copy of your results, just connect the Am96/4016 to a serial or parallel printer.

The Am96/4016 has an optional, low-cost ASCII keyboard/display, so you can use it all by itself. Or use it with your own CRT. Or with our AmSYS8/8 Z8000 Development System.

But most of all, use it to prove once and for all that the AmZ8000 is the best 16-bit family for you.

Standard Features:

CPU:	AmZ8002
Memory:	Sockets for up to 12K bytes of PROM; 8K bytes of RAM.
Input/Output:	Two RS232 serial ports; three parallel ports; three interval timers.
Firmware:	A 4K byte monitor allowing program entry, modification and checkout.
Physical Size:	SBC Format.

Optional Features:

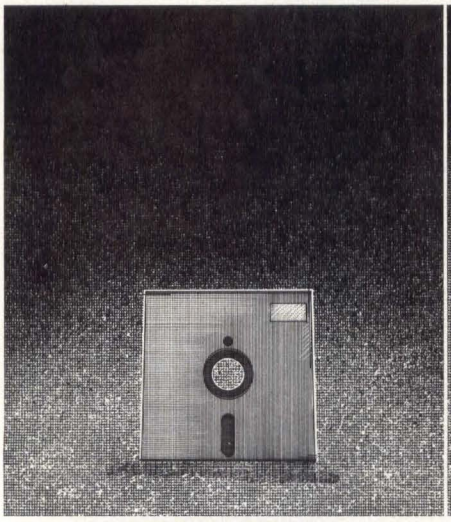
1. A full alphanumeric keyboard with 20-character display.
2. PROM-based, line-by-line assembler.
3. Additional memory expansion.
4. Universal prototyping card to add your own special circuitry.
5. Card cage with integrated power supplies.
6. AmZ8001 adapter.

Advanced Micro Devices

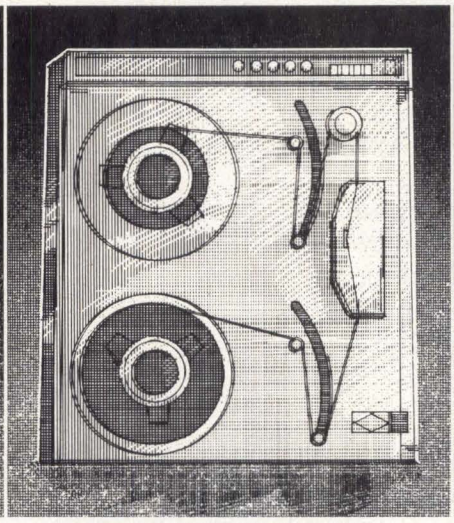
901 Thompson Place, Sunnyvale, CA 94086, Telephone: (408) 732-2400

CIRCLE 37 ON INQUIRY CARD

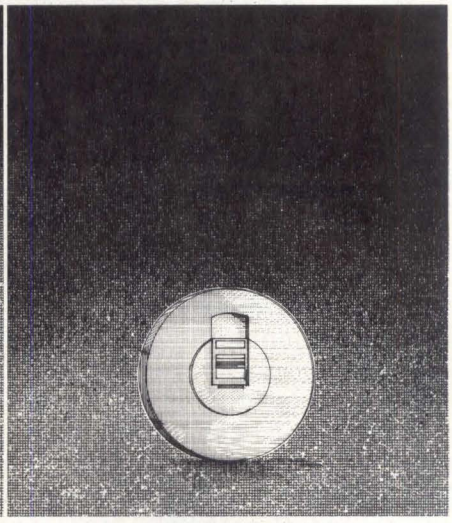
THERE ARE A LOT OF ALTERNATIVES TO THE DISK BACK-UP PROBLEM.



FLOPPY DISKS
Storage capacity: limited.
Handling problems.
Low cost.



REEL-TO-REEL TAPE DRIVES
Low performance: 36 megabyte capacity.
High performance: 90-100 megabyte capacity.
Large, bulky, high cost drives.
Cost: very expensive, up to 20 times that of floppy disks.



DISK CARTRIDGES
Storage capacity: 5-10 megabytes.
Back-up data remains on a disk.
Large drive mechanisms.
Cost: up to $5000.00.

HERE'S THE SOLUTION.

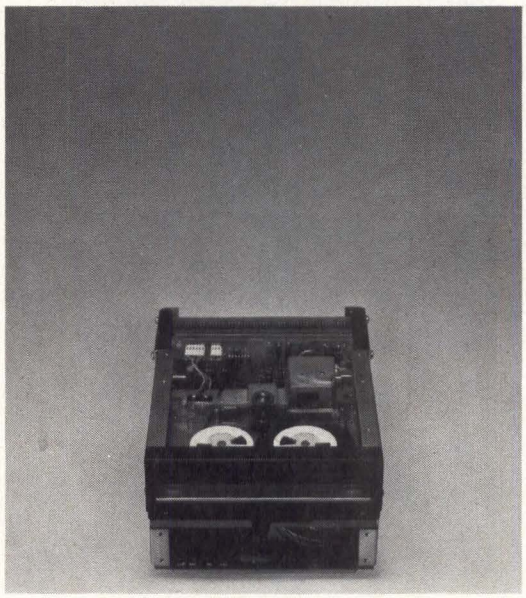
3M HCD-75 DATA CARTRIDGE DRIVE

Storage capacity: 75 megabytes formatted (144 Mbytes unformatted).

Drive dimensions: 4.62" x 7" x 8.625".

Preformatted tape, allows unlimited record replacement.

Built-in error detection/ correction capabilities.



Fully-buffered I/O channel, permits asynchronous data transfers.

Serpentine recording, eliminates wasted rewind times.

List price, including Controller, $2,150.00.

To learn more, check the listing at the right and contact the Data Products Representative nearest you. Or write: Data Products/ 3M, Building 223-5E/3M Center, Dept. **127,** St. Paul, MN 55101.

THE DISK BACK-UP SYSTEM THAT'S SUDDENLY WAY OUT FRONT.

3M

3M DATA PRODUCTS REPRESENTATIVES

Data Products/3M
3M Center, 223-5E Dept. **127**,
St. Paul, MN 55101
612/733-8892

WEST

Hefte Industries, Inc.
Los Gatos, CA
408/264-8319

CTI Data Systems, Inc.
Long Beach, CA
213/426-7375

P.A.R. Associates
Denver, CO
303/355-2363

P.A.R. Associates South
Albuquerque, NM
505/881-5000

MIDWEST

OASIS Sales Corporation
Elk Grove Village, IL
312/640-1850

Carter, McCormic & Peirce, Inc.
Farmington Hills, MI
313/477-7700

EAST

J.J. Wild of New England, Inc.
Needham, MA
617/444-2366

Wild & Rutkowski, Inc.
Jericho, Long Island, NY
516/935-6600

COL-INS-CO., Inc.
Orlando, FL
305/423-7615

3M

system, and provides 128k bytes of MOS memory with battery backup. Input is through a conversational CRT, storage is on a 67M-byte removable media, moving head disc drive.

Designed for OEM use, the 7835-AA provides controllers for a console device and all 417X disc devices. Built around the 7835 CPU, this package contains 128k-bytes memory and battery backup. Packaged with arithmetic accelerator, 128k-bytes memory, and battery backup, the 7835-based -A10A has 5M bytes of fixed and 5M bytes of removable cartridge disc storage.

High End Systems

Built around 7831 and 7870 CPUs, high end packages provide from 256k- to 1M-bytes of memory and offer peripheral equipment alternatives that consist of 10M-byte disc drive or 67M-byte disc with dual-density tape. Users can choose either hardcopy console or 4611 conversational CRT console.

A basic 7861-B10A package consists of 7861 CPU with 256k bytes of MOS memory using the MAX IV realtime multiprogramming operating system. This system offers 5M bytes of fixed and 5M bytes of removable disc storage, and is equipped with a conversational CRT console. Variations on this system include the -B10B which substitutes a hardcopy console for the CRT, the -B67A which substitutes a 67M-byte removable media disc and a 9-track tape system for the 10M-byte disc.

Designated -D67A, the basic 7870 package consists of processor and MAX IV operating system with 512k bytes of memory. This system includes 67M-byte disc and 9-track tape subsystems. With the same memory and storage, the -D67B substitutes a hardcopy console for the CRT. -H67A and -H67B increase processor memory to 1M bytes with the A configuration using a CRT and the B version a hardcopy console.

CIRCLE 273 ON INQUIRY CARD

Logic Circuit Test/ Programming System Offers Online Facilities

The microprocessor based 3PX651 provides online test program generation and management in addition to comprehensive logic circuit test and troubleshooting capability. Three Phoenix Co, 21639 N 14th Ave, Phoenix, AZ 85027, in introducing the unit, emphasized its suitability for high volume production testing as well as engineering design and field service return/repair applications.

Magiclip™, a computer guided diagnostic probe, allows rapid troubleshooting by low skill test operators by accomplishing automatic troubleshooting. For production testing, a designated test program is automatically transferred to the test head for execution. Stored program logic vectors or pseudorandom patterns are applied in a specified timing sequence to the circuit under test. Responses can be verified simultaneously at selected program steps or singularly by waveform signature analysis. Circuit test failures are reported by fail indicator lights, while failing test numbers, pin numbers, and TNT signatures are listed either on the teleprinter or CRT display.

Online programming and testing meet needs of changing logic circuit parameters and configurations by providing convenient test program verification and modification. The MIRTEST test programming language allows straightforward program generation in a high level user oriented language.

Modular design of the unit allows users to add capability as needs increase. Additional test heads are available to permit multiple department use. Other options include add-on TTL or high voltage driver/sensor pin modules, interface adapters, high speed pin subsystems, expanded RAM, and TTY or CRT keyboards. Base price of the unit is $42,000.

CIRCLE 274 ON INQUIRY CARD

From the graphics leader.

"Our energy exploration seismic modeling evaluations. there's no wait at all."

Opportunities for discovery are better, and data analysis is faster, since Conoco began using computer graphics to interactively model the seismic response of prospective rock strata.

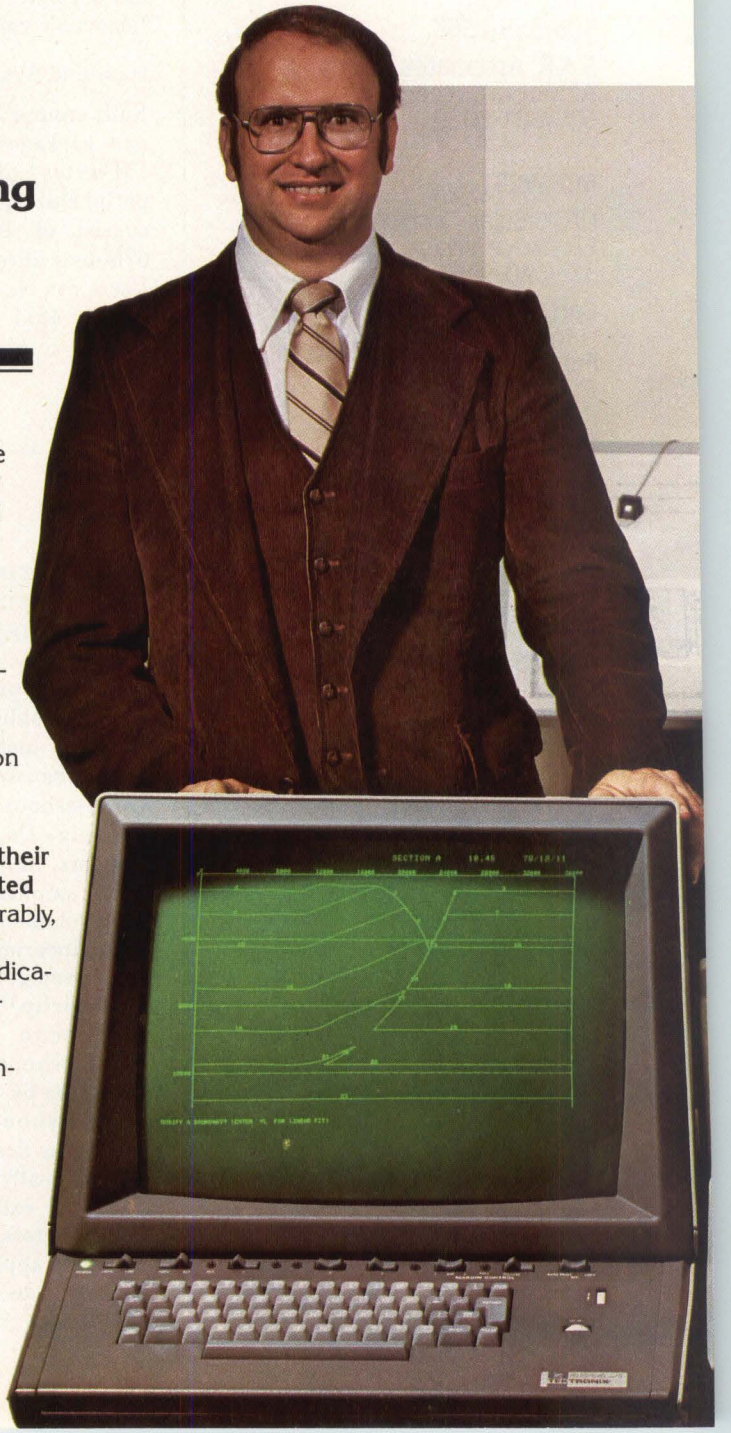
Wes Rice
Coordinator,
Computer Systems
Exploration
Research Division
Conoco Inc.

Conoco's search for hydrocarbon fuels begins by pounding the test site with mechanical vibrators, and recording reflected sound waves as two-dimensional seismic graphs.

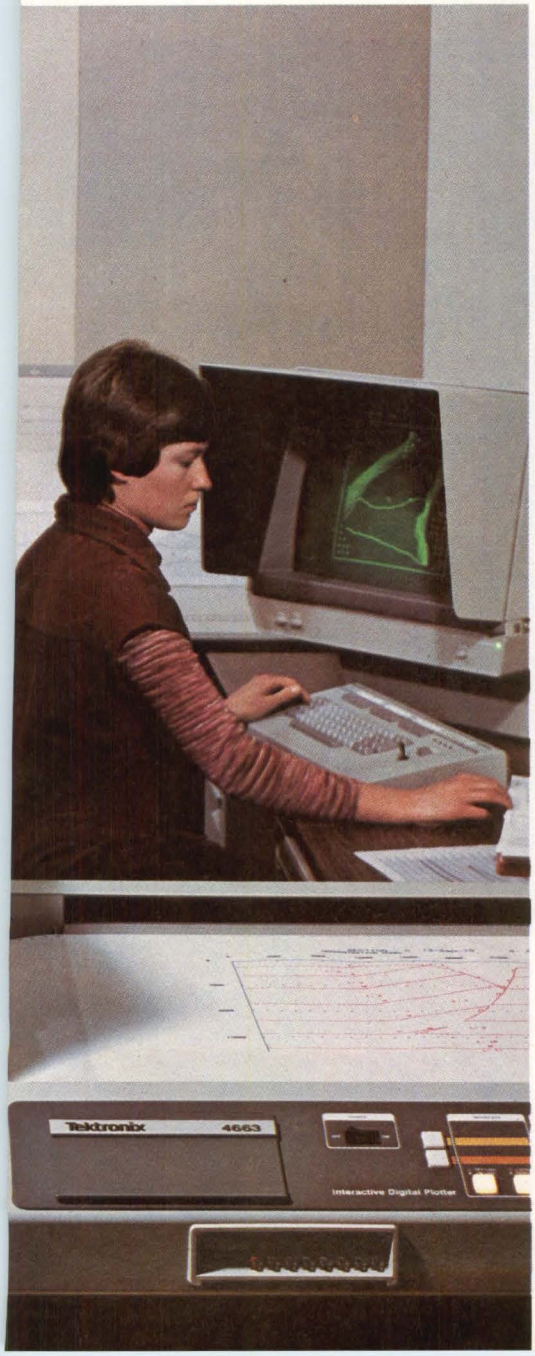
Enter Tektronix graphics. Rather than bundle guesswork interpretations of those graphs back to the home office for batch processing, geologists and geophysicists at the nearest exploration center digitize and display their theories of subsurface layer patterns on the high-resolution Tektronix 4014-1.

Users can continually compare a computer-generated seismic response of their hypotheses against the actual field-collected seismic data. When the two compare favorably, they have a highly probable picture of rock types, thicknesses, porosities, and other indicators of the character and quantity of hydrocarbon deposits.

"There can be more than 300 layers involved," says Conoco's Wes Rice. "Our

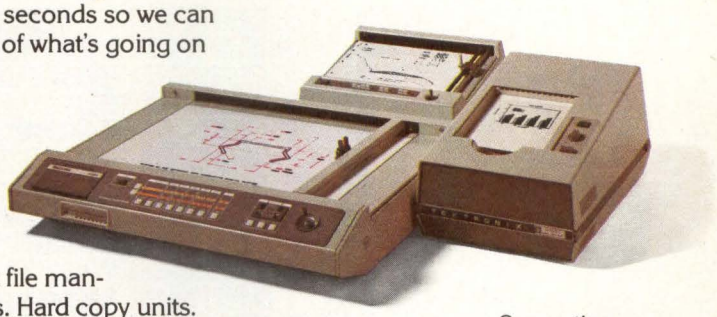


teams used to wait a week for With Tektronix graphics,



graphics equipment lets us digitize each rock layer configuration in seconds so we can quickly test concepts of what's going on in the earth."

Conoco's equipment includes more than the 4014-1. Research and operations facilities also include Tektronix file managers. Graphic tablets. Hard copy units. Digital plotters. To lessen loads on their mainframes and cut data transmission costs, Conoco is adding Tektronix' intelligent options. These fully equipped 4014 work stations, along with Tektronix 4081 graphics systems, effectively address Conoco's expanding graphics needs.



From exploration to refinery engineering, Tektronix is a proven resource for cutting the costs and speeding the processes of energy supply. Whether you're wondering what's under the earth or what's going to happen down the road, we'll give you the clearest picture. For more information, call your local Tektronix sales office or our toll-free automatic answering service at 1-800-547-1512 (in Oregon, 644-9051 collect).

Supporting our graphics terminals and desktop computers is a full line of advanced hard copiers, intelligent plotters, graphic tablets, data storage devices and more.

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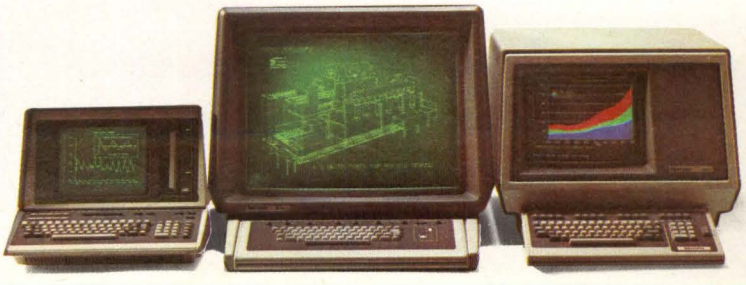
Information Display Division
P.O. Box 1700
Beaverton, OR 97075
Tektronix International, Inc.
European Marketing Centre
Post Box 827
1180 AV Amstelveen
The Netherlands

Tektronix®
COMMITTED TO EXCELLENCE

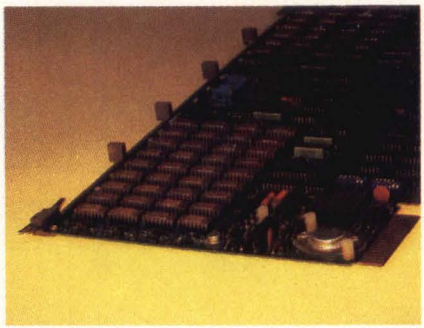
CIRCLE 39 ON INQUIRY CARD



Grow with the MSC 3605

The MSC 3605 is an add-in, single-board semiconductor memory system, designed to extend the capabilities of DEC computers, utilizing full hex-wide UNIBUS or Modified UNIBUS slots. On-board provisions include a standard parity Control Status Register (CSR) for parity generation and checking. Expandable in 32K byte increments to 128K bytes with or without parity, the MSC 3605 provides OEM designers and end-users with a number of important operating advantages:

Design Versatility The MSC 3605 is switch selectable between Modified UNIBUS and Standard UNIBUS interfaces. On-board DIP switches allow the user to quickly set up starting address and storage capacity in 1KW boundaries and CSR address.



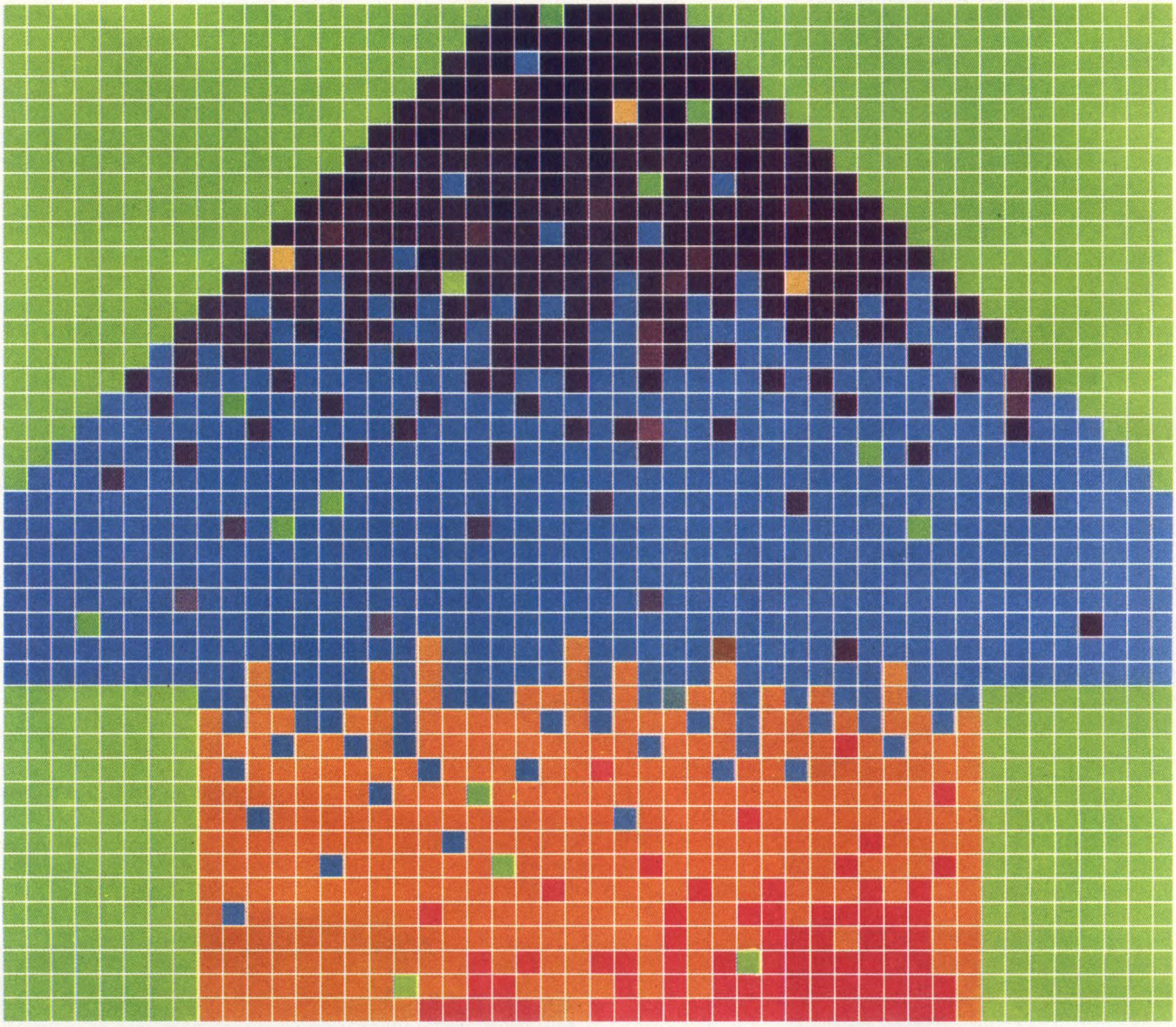
Monolithic Systems corp

Memory Reliability Low power consumption and fewer components contribute to the high reliability inherent in the MSC 3605. Predicted MTBF is over 40,000 hours.

Future Growth Socketed elements provide for both simplified maintenance and future expansion.

For additional information on the MSC 3605 and our other 41 Monolithic Systems Corp. products and systems, please contact us at 14 Inverness Drive East, Englewood, Colorado 80112. (303) 770-7400. Telex: 45-4498.

Extending the limits of information.



MSC Regional Sales Offices: Eastern Region 1101-B9 State Road, Princeton, NJ 08540, (609) 921-2240; **Central Region** 7200 East Dry Creek Road, Suite #B203, Englewood, CO 80112, (303) 773-1060; **Western Region** 49 South Baldwin, Suite D, Sierra Madre, CA 91024, (213) 351-8717

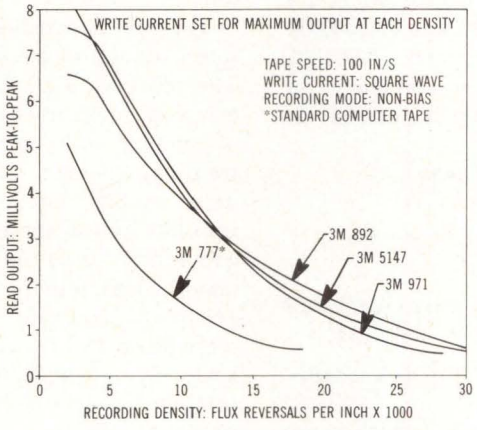
18-Track Recording Heads Quadruple Density On 0.5" Magnetic Tape

A major step towards the goal of greater storage capacity at less cost, an 18-track magnetic head, developed by Nortronics Co, Inc, 8101 Tenth Ave N, Minneapolis, MN 55427, is capable of increasing storage capacity of 0.5" (1.27-cm) computer tapes four times. In addition to doubling the number of tracks, the head can increase recording density from 6250 to 12,500 bits/in (2460 to 4921/cm) when using the group coded recording (GCR) system.

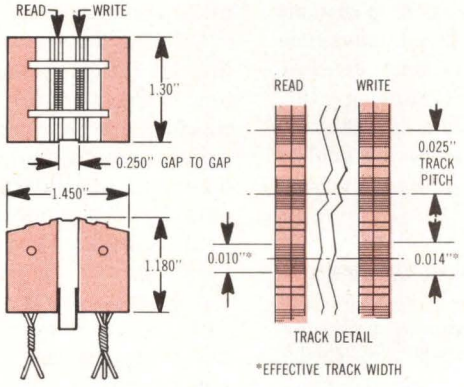
With GCR encoding, there are 9042 flux reversals/in (3559/cm) on the 9-channel format. The 18-track head can record as high as 20,000 flux reversals/in (7874/cm) using GCR techniques.

In designing the magnetic head, it was necessary to significantly reduce the size of its reading and writing tracks and to maintain practical electrical performance. Write tracks in the head are 0.014" (0.356 mm) wide compared to the 0.044" (1.118-mm) tracks used in 9-track designs. Read tracks have been reduced from the previous 0.040" (1.016 mm) to 0.010" (0.254 mm) in width. In addition, the head design permits backward compatibility—in the read function only, allowing the 18-track head to read standard 9-channel tapes.

Another facet of the development program producing the 18-track heads provides the option of using permalloy or ferrite as the core material in the head. While the use of permalloy has been extended to this high bit density system, it has limitations. The high frequency characteristics of the permalloy used in the conventional core does not provide the system with the same capability in recording high density as is supplied by the characteristics of other materials such as ferrite or thin film heads.



In addition to doubling number of tracks, 18-track recording head can double recording density from 6250 to 12,500 bits/in. With GCR encoding, head can record as high as 20,000 flux reversals/in; since standard tapes become marginal above 10,000, instrumentation grade tape is necessary for higher densities



18-channel read-after-write head developed by Nortronics is designed with write tracks that are 0.014" wide and with 0.040" wide read tracks. Backward compatibility—in read function—allows standard 9-track tapes to be read by head

Heads having ferrite cores have the potential for longer life, lower maintenance and greater density. Ferrite heads may have the potential for a cost advantage as well. However the longer time necessary to get delivery on the ferrite heads will influence the decision of drive manufacturers.

To use this head, existing tape drives will not require total new development. Some modifications to accommodate the increased number of data channels will be necessary, however. Existing electronics designed for high speed GCR tape drives should be usable in slower speed, high bit density, 18-channel tape drives.

These high recording densities, however, approach the ultimate usefulness of current 0.5" (1.3-cm) computer tapes. Although tapes now in use on 9-channel systems can be used with the 18-channel head, they are marginal when used at more than 10,000 flux reversals/in (3937/cm). Because of this, some tape drive manufacturers will use different tapes, such as those used for instrumentation recording. A quantity of the heads have been shipped to drive manufacturers for testing. Manufacture of the heads could begin late this year or early next year.

CIRCLE 275 ON INQUIRY CARD

Large General Purpose Computers Provide 303X Competitive Performance

Three general purpose computer systems targeted at the middle and upper end of IBM Corp's 303X series, the 7000 family introduced by National Advanced Systems, 3145 Porter Dr, Palo Alto, CA 94304 range from a 2M-byte, 6-channel processor to a dual-processor complex. The processors are being manufactured by Hitachi and are marketed under the recent agreement between Hitachi America and National Advanced Systems.

With up to 2.2 times the throughput of an IBM 3031, the AS/7000N is a 2M-byte, 6-channel basic processor. Expandable to 8M bytes and 8 channels, the system provides 1.9 to 2.1 times the throughput of National's AS/7031.

The larger AS/7000 has approximately 1.2 times the throughput of the IBM 3032. This unit can be field upgraded from the /7000N or obtained as a 4M-byte, 8-channel basic system. Expansion to 16 channels and 16M-bytes is possible.

The AS/7000DPC offers throughput equivalent to that of the IBM 3033 operating under MVS or VM 370. The dual-processor complex can be obtained as a 4M-byte, 12-channel system or can be field upgraded from the /7000.

The family is based on design of the AS/6 computers and uses a firmware architecture designed to track anticipated IBM announcements. With deliveries scheduled to begin in the second quarter of this year, prices are $1,000,000, $1,525,000, and $2,350,000 for AS/7000N, /7000, and /7000DPC, respectively. Add-on memory in 2M-byte increments is priced at $100,000.

CIRCLE 276 ON INQUIRY CARD

Speech Recognition Systems Double Operating Speed, Approach Continuous Goal

Doubling the speed at which voice data entry to a computer or other voice actuated systems can be operated, Quiktalk™ speech recognition systems greatly reduce the required pause time between spoken words. This development from Threshold Technology, Inc, 1829 Underwood Blvd, Delran, NJ 08075, closely approaches the goal of connected word or continuous speech recognition.

With the systems, moderately experienced speakers have attained better than 99% accuracy at entry rates of 180 words/min using the basic 32-word vocabulary (expandable to 256 words). More than twice the rate attainable with previous isolated word recognition equipment, this speed has been achieved with only a modest increase in cost. Thus prices for the units have been held to approximately 10 to 20% above those of current models. Most systems in the field can be modified to provide the high speed recognition capability.

In earlier systems, it was necessary to pause for 0.1 to 0.2 s between words to permit the device to discriminate between true word ends and certain intraword drops in signal energy that are a natural characteristic of speech. This requirement made it impossible for speech recognition equipment to match keyboard entry speeds in some applications.

To overcome this problem, the company's engineers devised an electronic means of recognizing strings of words as units rather than as individual words. Thus, the shortest possible pause between words can now be reliably detected.

The two models featuring the high speed capability are the 580 and 680. The 680 Voice Data Entry System is a complete interactive terminal capable of handling voice recognition, speaker training, speaker reference storage data, and all functions necessary to translate human speech into computer compatible data or machine commands. This unit provides a CRT or 16-char alphanumeric display and can serve as a direct replacement for a CRT keyboard or teleprinter, with no host computer modifications or special software required. It can be used for data entry, inquiry-response, timesharing, editing, or command and control applications.

Offering the same speed advantages in a lower cost system, the 580 uses a host computer for controlling the training process, operator prompting, storage of individual speaker reference data sets, and interpretation of word output codes. This type of operation permits usage as a completely host controllable speech recognizing peripheral device. Operation is achieved by interaction of the unit and the host CPU over an asynchronous serial interface using a special communications protocol. A 16-char alphanumeric display is provided.

CIRCLE 277 ON INQUIRY CARD

NO. 7

NATIONAL ANTHEM

SEMICONDUCTOR NEWS FROM THE PRACTICAL WIZARDS OF SILICON VALLEY

Series/80 microcomputer products brought back down to earth.

PRACTICAL DESIGNS FOR REAL WORLD APPLICATIONS.

Field-programmable PALs™

Ready-to-use dual PCM filters

Digitally programmable gain amps

The latest BIFET™ wizardry unveiled

Wickersham on ROMs

Complete literature from the National archives

Data Acquisition Logic Transistors Hybrids Linear Interface Bubble Memory
RAMs/ROMs/PROMs Transducers Displays Custom Circuits Optoelectronics
Memory Boards Microprocessors Development Systems Microcomputers Modules

NATIONAL ANTHEM

Field-programmable PALs™ available in quantity.

PAL offers economic alternative to TTL logic.

National now offers a family of Programmable Array Logic devices designed to replace standard TTL logic. A single PAL can replace 4 to 10 SSI/MSI packages. All PAL devices are fully field-programmable to provide the utmost in design flexibility and efficiency.

PAL's basic logic implementation is the familiar AND-OR array, where the AND array is programmable and the OR array is fixed. Variations on this theme include the number of OR gates in the array, invert or non-invert following the OR, the number of inputs and outputs, and registered or non-registered outputs.

The programmable AND array is a matrix of Titanium-Tungsten fuse links that initially connects every input and its complement to every OR gate. Programming the array removes some of these connections to form an AND function of the remaining device inputs (or their complements) on the selected OR gate inputs. For devices with registers, the register outputs are also in the AND matrix.

Saves space, time and money. A single 20-pin PAL can replace at least 4 SSI and MSI packages in a typical application. And depending on the specific logic function being implemented, a package-for-package replacement ratio of up to 10-to-1 can be achieved.

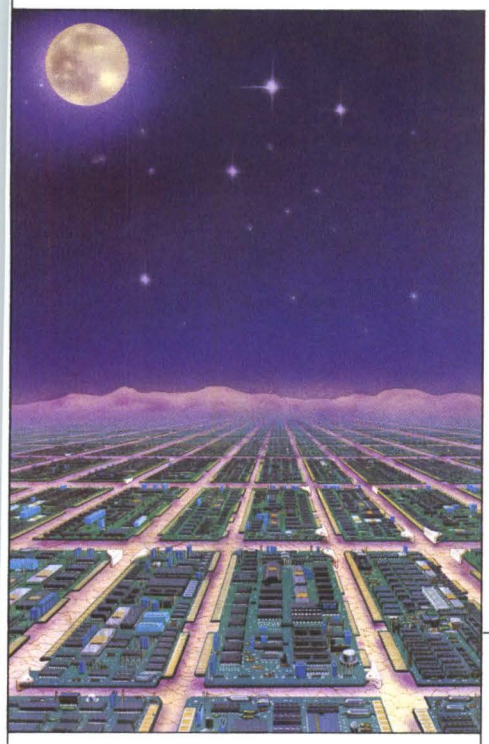
PAL's standard AND-OR logic and flexible I/O programming provide hitherto unknown design and production efficiency. Because logic modifications can be made more quickly and easily with PAL than with discrete random logic.

Reliable products from a dependable source. Under license from Monolithic Memories, Inc., National is producing TTL-compatible PALs with the same time-tested technology used to manufacture PROMs. The reliability of Titanium-Tungsten fuses is well established both through internal Rel testing and three years of field use. And with 15 different PAL devices to choose from (including both mil- and commercial temp), logic design efficiency and reliability is truly maximized.

National's high volume production capability means a dependable source of reliable PALs at the lowest possible cost.

PAL is a trademark of Monolithic Memories, Inc.

BLC Series/80 Family stresses practicality and reliability.



National doesn't just make over seventy-five Series/80 computer products. They make them practical with test points, options, functional design and availability.

Some manufacturers build flashy boards loaded with far-out technology that you don't need and won't ever use. But not National. They make practical, reliable boards that do just what you buy them for.

And National makes more kinds of those practical, reliable Series/80 products than any other manufacturer.

The Series/80 Family is by no means just a second source supply. No other supplier beats National's reliability, functionality of design, user options, or variety of products.

The Series/80 Family includes CPUs, memories, controllers, analog and digital I/O, peripheral controllers, firmware, card cages, power supplies, cables and just about anything you need for just about any application.

Test procedures make them practically pefect.

National's boards are designed to be functional, easy to design in and totally consistent in operation. That's why test points have been designed into each board. So testing becomes an integral part of the design phase and continues throughout National's unique dynamic high temperature burn in.

To further ensure reliability, you also get a full one-year warranty with each Series/80 board that you buy from any of National's distributors worldwide. The longest warranty in the industry.

All from the Practical Wizards who finally brought space-age technology back down to earth.

AF137 dual PCM filter tuned to PBX industry.

National's AF137 dual PCM transmit/receive filter was designed primarily for PBX and other digital telephone systems that are based upon an 8KHz sampling rate.

The AF137 filter is packaged in a single precalibrated package. And since it requires no tuning or external components, the laser-trimmed AF137 offers significant savings in terms of both design space and inventory costs with minimal power dissipation.

Both the transmit and receive filters incorporated into the AF137 are third order elliptic low pass filters. The transmit filter provides a flat bandpass response from DC to 3.0KHz. The receive filter compensates for the SINX/X response of the sampled input, thereby restoring it to a flat band pass characteristic.

The AF137 dual PCM filter is the least sensitive to time and temperature of any active filter available. That's because the Wizards at National feel that their filters shouldn't just be the best – they should stay the best.

LH0084-The logical choice in instrumentation amps.

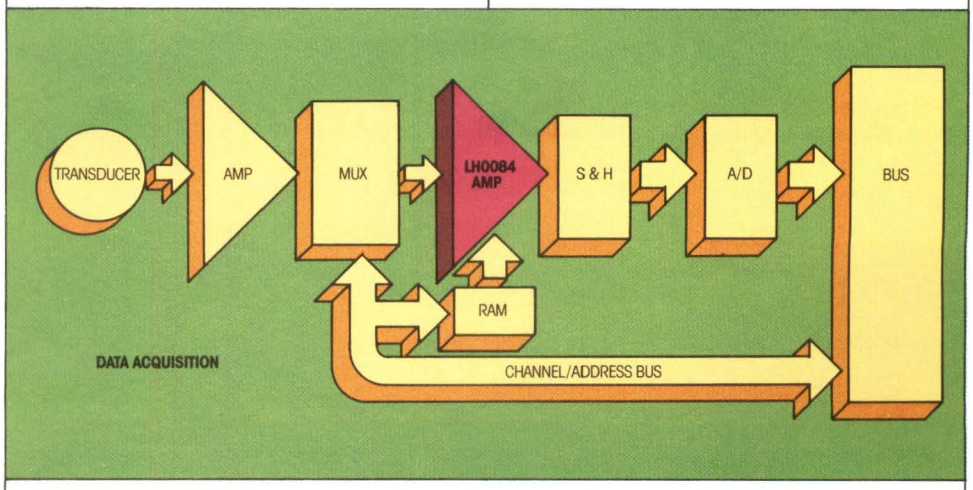
The LH0084 programmable gain instrumentation amps were designed specifically for data acquisition systems where settling time and input impedance are critical to the systems' integrity. As a result, the LH0084s settle to 0.1% in only 4μsec or less and offer 500pA input bias current and a typical input impedance of $10^{11}\Omega$.

Gains for the LH0084 are set internally in two stages. The first stage is software programmable in highly accurate gain steps of 1, 2, 5, or 10. This stage, controlled by a 2-bit TTL-level input word, allows software to set gains dynamically within the system.

For additional flexibility, the second stage can be pin-strapped to gains of 1, 4, or 10. So the gain ranges most widely used in instrumentation can now be provided by a single LH0084 high-performance amplifier.

The LH0084 programmable gain instrumentation amps are available in both military and commercial temp versions. Both versions come in hermetically sealed 16-pin metal DIPs.

The LH0084 is truly the logical choice when it comes to instrumentation amps.



National is seriously in the ROM business and is committed to capturing the major share of the market.

"At National Semiconductor we're in the ROM business in a big way. We've made a major, no-holds-barred commitment to ROM production, and our fabrication lines are now ROM exclusive – not shared.

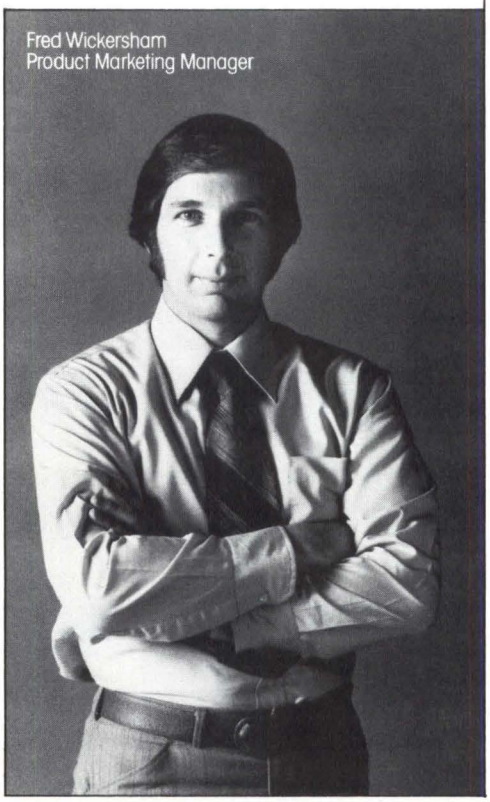
"And we're committed, also, to delivering every ROM we make on time. Without exception, thanks to our increased capability for volume deliveries. Which means no missed deadlines for our customers.

"With the number of products we offer, we're truly a first source company, and intend to stay that way. Our line features the MM52116, MM52132, and MM52164 ROMs, 16K, 32K, and 64K respectively. All are 2716 PROM-compatible, fully static, single ±5V products.

"Every model in our line has good, stable circuits which meet and, in many cases, exceed applicable specifications. Our prices are truly competitive, too.

"With the addition of a geared-up, production commitment to ROMs, National becomes a supplier for all your needs. We have focused our manufacturing capabilities on ROMs, no ifs, ands, or buts, and fully intend to dominate the marketplace.

"Call or write us here at National today and let us show you how committed we are."



Fred Wickersham
Product Marketing Manager

Low-cost commercial temp BIFET™ op amps guarantee lowest drift.

National Semiconductor guarantees the industry's lowest V_{OS} drift with their new line of commercial temp BIFET op amps. With these new low-cost op amps, the need for costly special testing has been eliminated.

The LF351A-1 and LF351B-1 single BIFET and the LF353B-1 dual BIFET op amps require 1.8mA current yet maintain a 4MHz gain bandwidth and a 13V/μsec slew rate. But perhaps of greater significance is their offset voltage drift:

	Max Initial V_{OS}	Max Drift
LF351A-1	2mV	20μV/°C
LF351B-1	5mV	30μV/°C
LF353B-1	5mV	30μV/°C

These new op amps are ideal for applications such as high-speed integrators, fast D/A converters, and sample-and-hold circuits.

The Wizards, known for their premium mil-temp BIFET op amps, are now setting the pace for high-quality, yet low-cost commercial temp BIFET op amps. Each with a guarantee that can't be beat.

BIFET is a trademark of National Semiconductor Corporation.

What's new from the National archives?

006 ☐ Special Functions Data Book ($6.00)
009 ☐ ROM MM52116 Data Sheet
010 ☐ ROM MM52132 Data Sheet
011 ☐ ROM MM52164 Data Sheet
022 ☐ LF351A-1/351B-1/353B-1 Data Sheet
025 ☐ PAL Brochure
026 ☐ AF100-1CN, AF100-2CN Data Sheets
027 ☐ AF137 Data Sheet
032 ☐ LH0084 Data Sheet
035 ☐ Additional Series/80 Information

Enclose check or money order based upon appropriate currency. Make checks payable to National Semiconductor. Allow 4-6 weeks for delivery.

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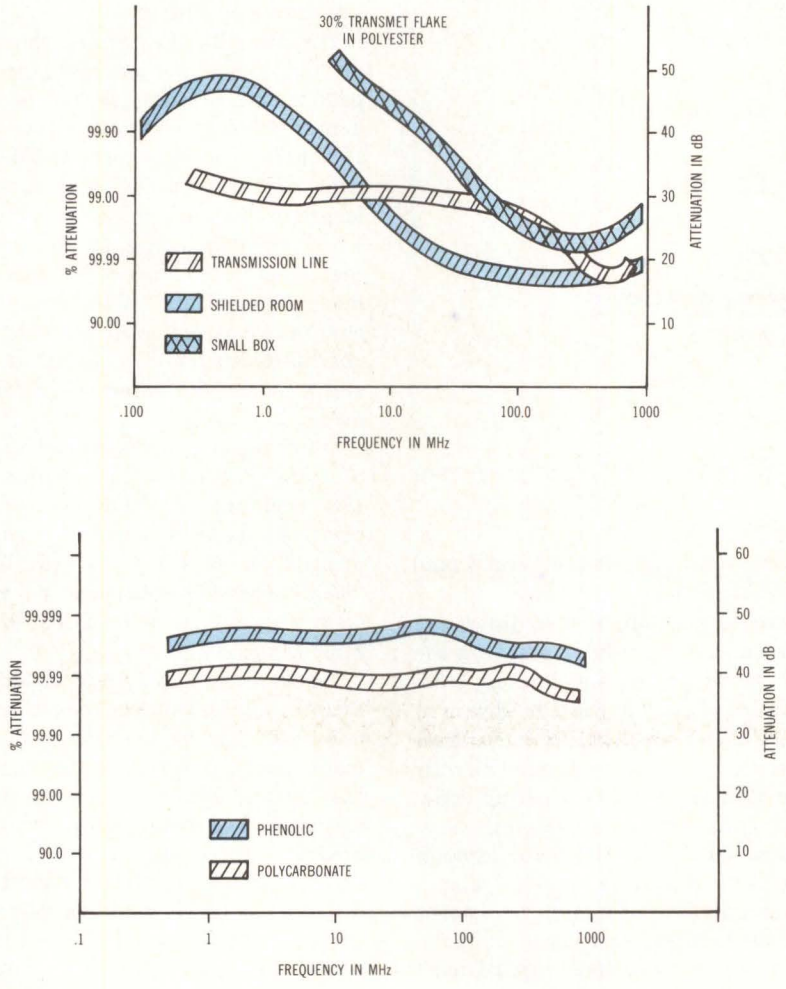
National Semiconductor
The Practical Wizards of Silicon Valley.

NA7

Conductive Modifiers Improve Electrical Properties of Plastics

Electrical and thermal properties of molded plastic products are improved by addition of series 100 modifiers. The modifiers are aluminum alloy flakes or fibers which, when added to such materials as polyesters, polycarbonates, or nylon, provide emi shielding, static charge dissipation, resistive heating, and heat conduction. Developed by Transmet Corp, 1375 Perry St, Columbus, OH 43201, the modifiers meet the demands of virtually any compounding, extruding, or molding process.



Typical curves (top) show emi shielding effectiveness of Transmet's modifiers using shielded box, shielded room, and coaxial transmission line measurement techniques. Curves on bottom show effect of frequency on shielding effectiveness in phenolic and polycarbonate materials

Equipment enclosures produced with modified plastics offer inherent shielding against electromagnetic interference. When modifiers are used in the molding process, emi shielding is accomplished, eliminating the need for the painting or metal spraying now used to provide protection. A similar cost reduction is accomplished when the modified plastics are used as an alternative to metal enclosures. In addition to the elimination of environmentally generated noise, the plastic enclosures weigh less and offer improved appearance.

Total shielding effectiveness of an emi shield is the sum of the energy reflected plus the energy absorbed. Design controllable parameters are part thickness, ϱ_B, and bulk resistivity. Thicker parts will have more modifier between the emi source and receptor, thus the amount of shielding will increase. Highest shielding effectiveness is obtained using the highest conductivity resin (lowest ϱ_B).

In general a ϱ_B less than 500 Ω-cm gives some shielding and good electric static discharge protection. A ϱ_B of less than 100 Ω-cm will yield good shielding; ϱ_B less that 25 Ω-cm provides excellent shielding.

Because modified plastics readily conduct electricity they can be used in applications where a build up of static charge cannot be tolerated. Molding the hubs and outer surfaces of wheels and rollers from modified plastics provides static bleedoff for their metal counterparts as well as lighter weight and corrosion resistance. Sudden static discharges can have disastrous effects on sensitive instrumentation with erroneous reading or erasing of accumulated data resulting from a single occurrence. Housings made of modified plastics can ensure continuous grounding and prevent the interruption of critical functions.

Although the material conducts electricity it has a finite resistance, therefore a current passing through will produce energy in the form of heat. Since the resistivity can be altered by the material's formulation and the heating ability by the configuration, resistive heaters formed of the material can conform to virtually any

Current Technology	Modified Plastics
Materials Cost	
\$0.75 to 1.27/lb	\$2.50 to 3.50/lb
\$0.029 to 0.055/in³	\$0.125 to 0.187/in³
\$0.52 to 0.99/ft²	\$2.25 to 3.37/ft²
Molding, 100 s/cycle	**80 s/cycle**
\$55/machine hour	\$55/machine hour
\$1.50/part	\$1.25/part
\$0.115/ft²	\$0.096/ft²
Secondary coatings, labor and materials	
\$3.00/ft²	No cost
Total Cost/ft²	
\$3.635 to 4.105	\$2.346 to 3.466
Total Part Cost	
\$47.26 to 53.37	\$30.50 to 45.06
Average Part Cost	
\$50.32	\$37.78
	Average Savings/Part
	\$12.54

heating application within the resin system's thermal limits.

The material's heat conduction properties also adapt them to use in removing heat from heat producing components. By molding heat sinks as an integral part of the equipment enclosure, the cost of a special piece of hardware can be eliminated. In addition to absorbing heat from specific components, enclosures made from the material keep internal equipment temperatures lower by dissipating heat to the surrounding environment.

Economic advantages of using modified plastics become apparent when the cost of manufacturing a product using current coating technology is compared with the cost of producing an identical product using modifiers. The example is an equipment enclosure with a surface area of 13 ft² and nominal wall thickness of 0.125" (1.2 m² and 3 mm) to be shielded.

Series 100 conductive modifiers are flake and fiber products based on the melt extraction and melt drag techniques developed at Battelle Memorial Institute Laboratories in Columbus, Ohio. The particles are formed directly from a molten bath, eliminating variations inherent in machining techniques. K-102 flake and B-103 through -106 fibers provide a range of shapes and lengths (3 to 18 mm) to meet needs of compounding, extruding, or molding processes. The flake orients itself to the direction of flow and gives minimal flow resistance. Higher aspect ratio fibers can also be used in injection molding. Flakes can also be used in sheet and mat molding applications; longer fibers can be used if dispersed across the E-glass mat.

CIRCLE 278 ON INQUIRY CARD

Distributed Data System Built Around Intelligent Terminals

Communications capabilities necessary for distributed processing, intelligent data entry, and distributed printing are a major feature of the 5280 distributed data system introduced by International Business Machines Corp, General Systems Div, PO Box C-1645, Atlanta, GA 30301. Comprising the family are single- and dual-keyboard/display stations which attach to a control unit.

For use with the system, the 5225 printer offers upper and lower case impact matrix printing as well as condensed printing in various sets of up to 192 characters. Print speed is independent of character set size and line length for lines of up to 7.4 to 13" (18.8 to 33 cm) depending on the model. Maximum rated speeds of the four models range from 280-lines/min at 10 char/in (4/cm) and 195 lines/min at 15 char/in (6/cm) for the model 1 to 560 and 420 lines/min, respectively, for the model 4.

Other printer attributes include 132 printing positions at 10 char/in and 198 positions at 15/in. Condensed printing allows a report previously printed on 14.875 x 11" (37.782 x 28-cm) paper to be output on 8.5 x 11" (21.6 x 28-cm) paper at 15 char/in and 8 lines/in (3/cm).

Software for the system includes a system configurations program to tailor IPL for the operating environment, initial program loader that initializes any 5280 system for program execution, and a close failure recovery program that allows users to identify and specify an end of data record in a diskette data set in the event of an abnormal program termination. DE/RPG programming facility allows interactive data entry, high volume key entry, and user defined processing. This software provides multiple screen formats, high function keyword editing, an RPG subset of calculation operation codes capability for subroutines or batch oriented standalone programs, diskette data set support, and a source

Qantex
IMPACT PRINTERS

150 CHARACTERS PER SECOND

80/136 COLUMNS PER LINE

UNDER $900 IN OEM QUANTITY

The Series 6000 is perfect for applications where high reliability at a low cost is a major consideration. Microprocessor controlled. Heavy duty operation.

Loaded with standard features. Tractor paper feed. Multi-part forms control. Top of form operation. Manual paper advance control. Built-in test capability. Cartridge ribbon. 9x7/9x9 dot matrix. Parallel or serial interfaces. Plus more.

Contact us today for a free print sample.

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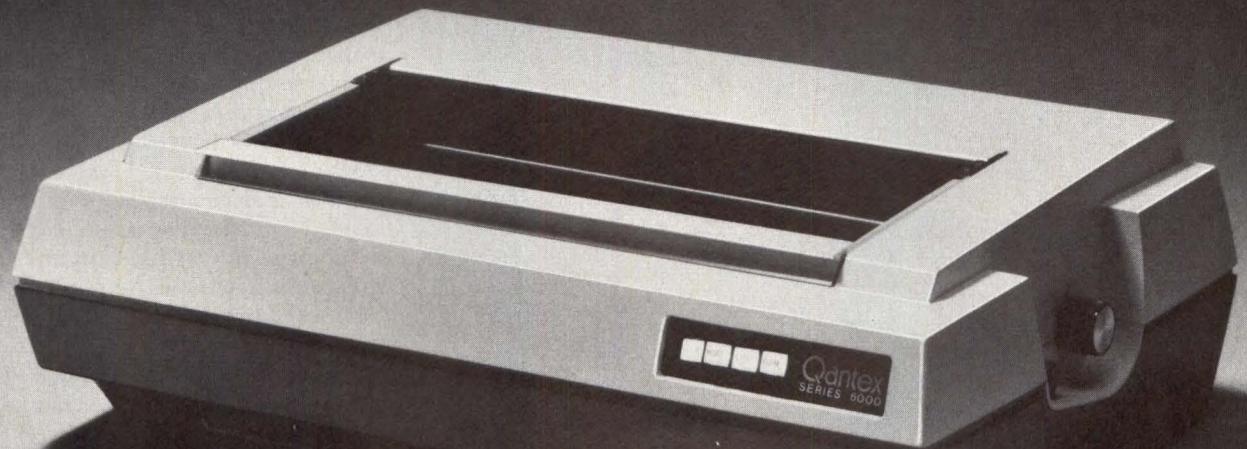


Introducing

CIRCLE 42 ON INQUIRY CARD

entry program. Both COBOL-OS/VS and COBOL-DOS/VSE host compiler and library will be available as is a sort/merge package for use with any diskette data set organization supported by the system.

Communications utilities consist of communications access method support and an interface to the access method for communications programs written in any of the system's languages. Users can communicate using BSC and SDLC in System/370, 303X, 43XX, and System/3, /32, and /34, as well as Series/1, 3740, 5260, or another 5280.

A representative 5280 configuration consists of programmable keyboard/display station with main storage of 64k characters, two diskette drives that accommodate 1.2M char each, a 120-char/s model 5256 serial printer, and a communications adapter. This system has a purchase price of $16,660. Shipments are scheduled to begin in June.

Keyboard/display stations are available with 480-, 960-, or 1920-char screen displays featuring extended highlighting with reverse image, high intensity, blink, underline, nondisplay, and column separators. Keyboards are either data entry, data entry with proof arrangement, or typewriter style. Available character sets include 94-char upper and lower case EBCDIC, 94-char ASCII, and 188-char multinational sets.

The 5285 programmable data station is a keyboard/display unit with built-in programmable controller and diskette drive. This unit provides 480-, 960-, or 1920-char displays, 32k, 48k, or 64k bytes of main storage, and a second optional diskette drive. Transmissions use BSC and SNA/SDLC communications lines.

A standalone programmable controller with one diskette drive, the 5288 programmable control unit has 32k to 160k bytes of main storage and facilities for three optional diskette drives. The unit provides for a cluster of up to four keyboard/display stations and attachment of up to four 5256 or one 5225 printer.

Consisting of dual keyboard/display station, built-in controller, and two diskette drives, the 5286 dual programmable data station provides 32k, 48k, or 64k bytes of main storage and 480-char displays. The unit functions as two independent programmable data stations.

CIRCLE 279 ON INQUIRY CARD

Conferences Will Focus On Pattern Recognition, Software Engineering, and Microcircuit Applications

Research papers on all aspects of pattern recognition are being solicited for presentation during the International Conference on Pattern Recognition in Miami Beach, Fla, on December 1 through 4. Cosponsored by the IAPR and the IEEE Computer Society, the conference will consist of long (6000-word) and short (3000-word) papers, chosen from those submitted.

Topics include methodologies—statistical, structural, and syntactic methods, and clustering techniques; preprocessing and feature extraction—image enhancement and restoration, line drawings, waveform analysis, and shape and texture analysis; and implementations—digital systems, special processors, optical techniques, interactive systems, data structures, data bases, and innovative computer architectures. Also of interest are applications in the areas of character recognition, speech recognition, robot vision, medicine, and biomedicine.

Four copies of a full length draft should be submitted by April 1 to the Program Chairman: Prof Y. T. Chien, Dept of EE and CS, U-157, University of Connecticut, Storrs, CT 06268.

The International Conference on Software Engineering will serve as a forum for technical and managerial interchange on the issues facing the field during the 80s—the need to improve productivity, enhance quality, and

Who debugged debugging?

Introducing one of The Glitch Grabbers™ from Philips: the PM3540, a new logic analyzer that's specifically designed for digital debugging. It gets the bugs out fast because the PM3540 is the only compact instrument in the field today that allows data to be displayed, analyzed and then be directly related to real-time situations.

At the touch of a button the PM3540 changes from a logic analyzer to a two-channel oscilloscope, with interactive triggering from the same data word. This gives you an exact cross-reference between data and timing—essential for digital troubleshooting.

The PM3540 allows you to work with data in binary, octal or hexadecimal formats. You can capture a data block of 64 x 16 bits anywhere along the data stream. Page the display at the touch of a button through the data stream. Analyze and track down the fault and then set the PM3540 to trigger internally as an oscilloscope.

With the PM3540 you get both logic and real-time analysis in a single, compact, high-performance instrument. An instrument that speeds up your job of locating the bugs and correcting the digital faults.

When there's a better, more innovative way to design new test equipment, Philips will do it. And we'll do it and stand behind it right here in North America. Now, more than ever, Philips wants to make *your* next piece of test equipment.

For additional information call (541) 342-9180 in Montreal; (416) 789-7188 in Toronto; (613) 224-8374 in Ottawa or contact Philips Test & Measuring Instruments, Inc., 6 Leswyn Rd., Toronto, Ont. M6A 1K2.

Philips, of course.

PHILIPS

Test & Measuring Instruments

PHILIPS

CIRCLE 44 ON INQUIRY CARD

The brains behind

Hewlett-Packard's 2649 Series terminals are making a lot of OEMs look good these days.

Here are three reasons why:

The HP 2649A. Build in the performance you want. The microprogrammable HP 2649A lets you take full advantage of your knowledge of 8080 assembler and really get "inside" the machine for sophisticated programming. What's more, all the circuitry for each specific function—data communications; keyboard interface—is on a single plug-in module. So you can pick the individual cards you need to refine your product further: serial or parallel I/O boards and RAM, ROM, and PROM memories.

HP also provides a powerful set of development tools to help you get the most from the HP 2649A in the least time. These include a RAM-based development terminal with cross assembler and debug features, comprehensive documentation, and a practical, hands-on training course.

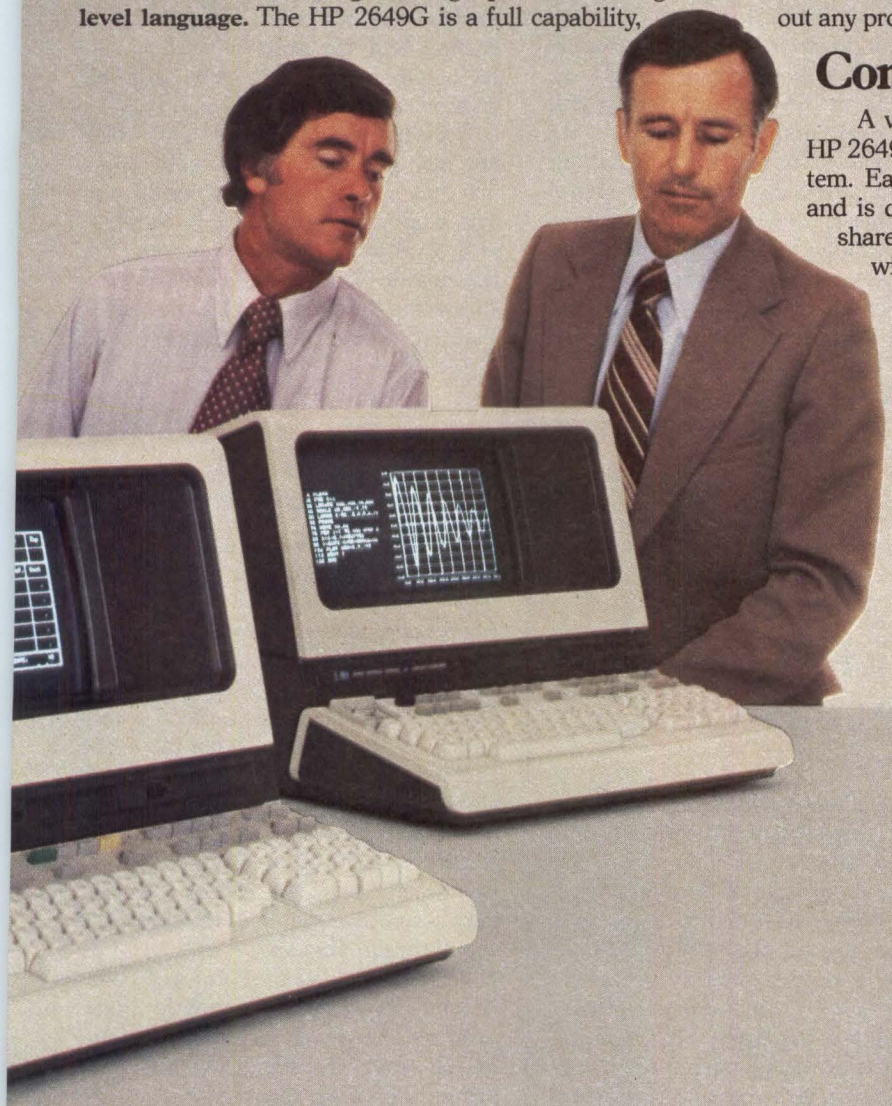
The HP 2649I. Applications programming simplified. The user-oriented HP 2649I lets you do high-level programming in BASIC. You get up to 220K bytes of mass storage on dual cartridge tapes, and

42903 HPT14

some very smart OEMs

eight programmable keys provide menu-like instructions to guide the operator step-by-step through the job. You can even split the HP 2649I memory into four separate user areas for rapid switching between data sets, instruction menus, or data entry forms.

The HP 2649G. High-level graphics with a high-level language. The HP 2649G is a full capability, OEM-discounted graphics station, with raster scan technology, selective erase, pattern definition, and much more. And with AGL, our high-level extension to BASIC, graphics is a snap. Set axis, scaling, and location, for example, with a simple three-statement program. Or you can use our powerful Multi-Plot feature to run simple pie, bar, or linear charts without any programming at all.



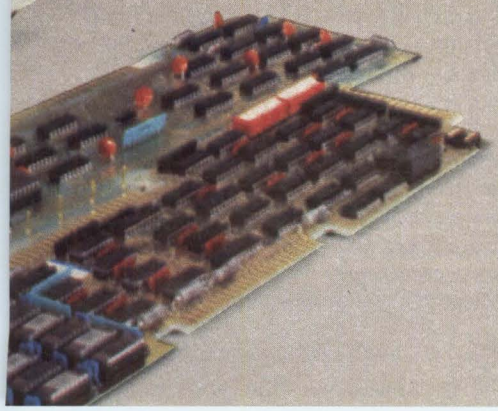
Communications made easy.

A variety of serial and parallel interfaces make the HP 2649 terminals an extremely versatile tool in any system. Each works with the RS232C interface standard, and is compatible with most modems. And the optional shared peripheral interface provides communication with a wide range of printers, plotters, and other devices.

Whether you're designing a specialized terminal, controller, microcomputer or graphics display station, the HP 2649 Series gives you a real head start in building your product. And that's what being a smart OEM is all about.

If you'd like to know more about HP's 2649 Series terminals, just call your nearest HP office listed in the White Pages and ask for full details. Or send us the coupon below. We'll be glad to fill you in.

HEWLETT PACKARD



I'm interested in the HP 2649 Series terminals. Please send me more information about the:

☐ HP 2649A Microcomputer/Controller ☐ HP 2649I Intelligent Terminal
☐ HP 2649G Intelligent Graphics Terminal ☐ Please have a salesman call.

Name Title

Company

Address

City/State/Zip

Phone

Mail to: Hewlett-Packard, Attn: Ed Hayes, Dept. 1263
19400 Homestead Road, Cupertino, CA 95014

CIRCLE 45 ON INQUIRY CARD

develop effective project management and control guidelines. To be held in San Diego, California on March 8 through 12, 1981, the conference is sponsored jointly by ACM's SIGSOFT, the National Bureau of Standards, and the IEEE Computer Society.

Papers in all areas of software engineering are invited; of particular interest are the topics of pragmatic or formal techniques or tools addressing problem definition, specification, development, certification, and maintenance of complex software systems; definition, quantification, and experimental design for assessing software productivity; models and metrics for comparing and analyzing methodologies, as well as end item software; computer aided environments for software engineering; and the impact of software engineering on the development of distributed systems and the impact of the microcomputer revolution on software engineering.

Interested authors should submit five copies of a 2000- to 6000-word paper to the program chairman: Dr Leon G. Stucki, Boeing Computer Services Co, PO Box 24346, Seattle, WA 98124; deadline is June 1.

Highlighting microelectronic applications and development trends derived from Government sponsored military or nonmilitary efforts, the Government Microcircuit Applications Conference will focus on the themes of directions of government electronics in the 80s. To be held in Houston, Texas, from November 17 through 21, the conference will discuss VLSI and terrestrial applications of aerospace technology.

To fulfill this aim, papers arising from programs sponsored or conducted by the government are being sought for presentation. Areas of interest include, but are not restricted to, digital and analog signal processing, gigabit logic, design for testability, self-repair, life cycle cost modeling and analysis, programmable signal processing, architecture and simulation, packaging and assembly, voice processing and synthesis, electro-optics, fault tolerance, and logistic support methods.

Deadline for receipt of a 35-word abstract and 300- to 500-word summary of a paper suitable for 20-min oral presentation is April 9. Submissions should be addressed to Hildegarde Hammond, Palisades Institute for Research Services, Inc, 201 Varick St, New York, NY 10014.

Display System Processes Japanese Kanji Characters

A general purpose display system that processes Japanese Kanji characters, IKIS (interactive Kanji input system) allows users of Data General computers to input and display the 6000 characters that form the Japanese alphabet. Produced in a joint venture between Data General Corp, Rt 9, Westboro, MA 01581 and Nippon Mini-Computer Corp, the system solves a long standing problem in Japanese computer applications.

Permitting keyboard entry of the simpler Katakana or phonetic character set, the system screen displays up to 768 Kanji characters. An attached printer allows hardcopy output of formatted data and reports, providing users with the ability to obtain information and reports in the familiar Kanji character set. The character conversion package includes a sophisticated dictionary that can be expanded for specific applications.

Multiple stations can be operated under the advanced operating system for the Eclipse computer. Applications can include standard commercial data processing and reporting as well as word processing.

CIRCLE 280 ON INQUIRY CARD

Our 64K ROM is like our 32K ROM is like our 16K ROM.

For new system designs and for upgrading existing systems, the flexibility of our totally static 64K ROM gives you that extra edge. And it's backed to the hilt with proven high performance.

The SY2364 is the latest addition to our family of 24-pin ROMs designed around a common industry standard pinout. That means maximum system flexibility. All three — 16K, 32K and 64K ROMs — can plug into the same socket. System upgrades are just a matter of substituting the new ROM for the old. With no increase in power.

We offer compatibility that's more than pin deep. All our ROMs are fully static (no clocks to worry about), so they all have the same timing waveforms. If speed is your concern, you can select one of our standard 450nsec versions or upgrade to our high performance 300nsec versions. All six are available now in quantity production.

	300ns	450ns
2K x 8	SY2316B-3	SY2316B
4K x 8	SY2332-3	SY2332
8K x 8	SY2364-3	SY2364

No matter what your needs, we have just the ROM for you. And that includes the SY2316A, SY4600 and SY2333 (pin compatible with the 2732/2732A 32K EPROM). For further information, contact Memory Product Marketing direct at (408) 988-5611. For Area Sales Offices and distribution references, call Headquarters Sales direct at (408) 988-5607. TWX: 910-338-0135.

Synertek performs as a major MOS supplier of high volume parts with advanced technologies and techniques behind everything we make. ROMs. Static RAMs. EPROMs. Custom circuits. Single-chip Microcomputers. Systems. 6500 Microprocessors and Peripherals.

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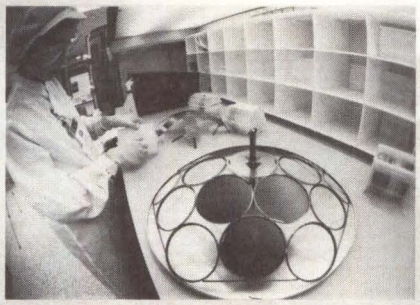


CIRCLE 47 ON INQUIRY CARD

Resistor Design Reduces Discrete Component To Planar Form

Thick film multilayer technology offers a method of reducing a discrete component or components to planar form. Producing trim factors in excess of 1000 with excellent stability, the patented design, from Electro Materials Corp of America, 605 Center Ave, Mamaroneck, NY 10543, provides circuit designers with an alternative approach to network construction.

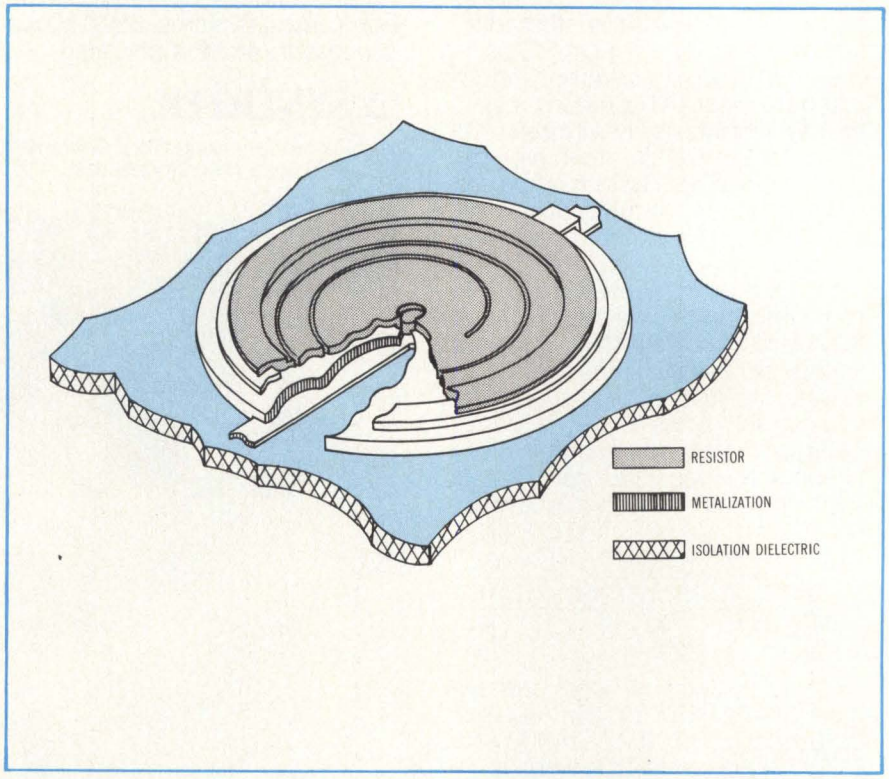
The resistor is constructed on a ceramic substrate by printing a circular geometry over a multilayer dielectric. Termination of the resistor is accomplished at its center with a via to buried conductor and at its circumference with a conductor ring on the dielectric layer (see diagram).

An initial aspect ratio equal to the radius divided by the circumference at a point midway between the center and the outer conductor ring is achieved. This gives a value of R (ohm per square) $/\pi$ or approximately one-third that of a square resistor made with the same ink.

By trimming the resistor in a spiral between the inner and outer conductors, it is possible to generate over 100 squares of length in a relatively small area. Minimum resistor widths are easily maintained and potential for hot spotting due to current crowding is alleviated.

Calculations made on a resistor of 0.480″ (12.192-mm) total diameter and maintaining a minimum resistor width of 0.040″ (1.016 mm), yield a trim factor of approximately 400:1. A reduction of minimum width to a more realistic 0.020″ (0.508 mm) increases the trim factor to 1600:1—all accomplished in less than 0.25 in² (6.35 mm²) of substrate area.

Several variations of construction are possible. The substrate can replace the multilayer dielectric as the required insulative layer. By utilizing plated through holes, electrical contact can be made with the center of the resistor from the back side of the substrate.



Porcelanized steel substrates offer another design possibility. Constructing a via in the glaze and exposing the steel base would provide a method of making electrical contact with the center of a resistor deposited over the opening.

Since wide resistance variations are possible with a single ink printing, wide-band tuning of RC networks using discrete capacitors is possible. It is also possible to manufacture planar RC networks incorporating both lumped and/or distributed capacitance by placing a thick film capacitor dielectric underneath the resistor either as the conductor isolation layer or as a sublayer to the material used for isolation.

Low power divider networks with close tracking of resistor properties can be manufactured, since all resistors will be made of the same material. Wide adjustment capability allows the same basic circuit to be used in several similar end products, saving manufacturing cost.

CIRCLE 281 ON INQUIRY CARD

Memory Board Test System Simplifies Test Program Implementation

Memory board test system DR-12/30 is a minicomputer based system supported by ATLS-12 executive software. The sophisticated production tool developed by Adar Associates, Inc, 154 Middlesex Tpk, Burlington, MA 01803 incorporates features to increase efficiency of engineering and programming personnel.

Executive software simplifies the implementation of efficient production and diagnostic test programs. With it users can write versatile engineering characterization routines that facilitate presentation of engineering data such as shmoo plots.

An optional computer guided signature test probe aids in locating faulty components or nodes on logic elements. An optional data image bank permits testing of ROM elements and driving board inputs with programmed test sequences.

CIRCLE 282 ON INQUIRY CARD

Inventory reports

Point-of-sale

Data entry

Environmental control

Financial reports

Computer graphics

Sylvania breaks the color barrier.

Introducing America's first 19-inch color data display tube.

Not just a tube with color.

A tube with gorgeous, glorious, sharp Sylvania color.

Color that provides clearer images and better contrast than anything available anywhere.

Color that makes small characters a breeze to read, with less fatigue.

Crystal clear color created by a high density tri-dot mask.

Color sharpened by a multiple-beam electron gun and enhanced by a Chromatrix dark surround negative guard band, and a rare earth phosphor system.

Sylvania color.

It's completely changed the picture in data display tubes.

Write Product Marketing Manager for our latest catalog:

GTE Sylvania
Data Display Tube Division
700 North Pratt Street
Ottawa, Ohio 45875

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CIRCLE 48 ON INQUIRY CARD

WHAT SPERRY UNIVAC IS DOING IN THE MINICOMPUTER BUSINESS.

WE'RE GIVING OEMs THE BUSINESS.

Literally.

We're out to build the biggest, best OEM base in the industry. And we've decided to do it the fastest, surest way possible. By offering OEMs the best deal in the business.

HOW DO WE DO IT?

Easy. You tell us your problem. We'll solve it. For example:

Have you ever been interested in becoming a supplier to a specific vertical market only to find you already had too much invested in software to warrant conversion to a new system with an expensive start-up price tag?

We've got a plan that provides you with a specific vertical market software package. We know where to find software that runs on our hardware with all the necessary capabilities. So we can practically eliminate start-up time and make your new system profitable with your very first sale.

WE WANT TO SUPPORT YOU.

Opening doors to vertical markets is only the first step in our plan. After we get you started, we keep you going. We'll provide marketing support suited to your specific market. And we'll provide leads from your geographic area.

YOU CAN'T LOSE.

Because we're out to win. And we've got the support that can make it happen. Sperry Univac was first in the computer industry. And we're growing from the success established by Sperry Univac with over $10 billion in installed systems worldwide.

That total support includes a heavy commitment to the kind of research and development that produced some of the first systems to run COBOL, FORTRAN, PASCAL, RPG II, TOTAL, Timesharing, Transaction Processing and a mix of communications protocols concurrently.

And we're going to keep it up. Providing a wide-range of products at the forefront of technology is as much our business as selling and delivering equipment.

We've done just about everything we can think of to make working with Sperry Univac easy. And of course, all our products are supported by 10,000 technicians servicing our hardware worldwide.

If you can think of anything else we can do for you, give us a call right now. We mean business.

For more information write to us at Sperry Univac Mini-Computer Operations, Marketing Communications, 2722 Michelson Drive, Irvine, CA 92713. Or call (714) 833-2400, Marketing Communications.

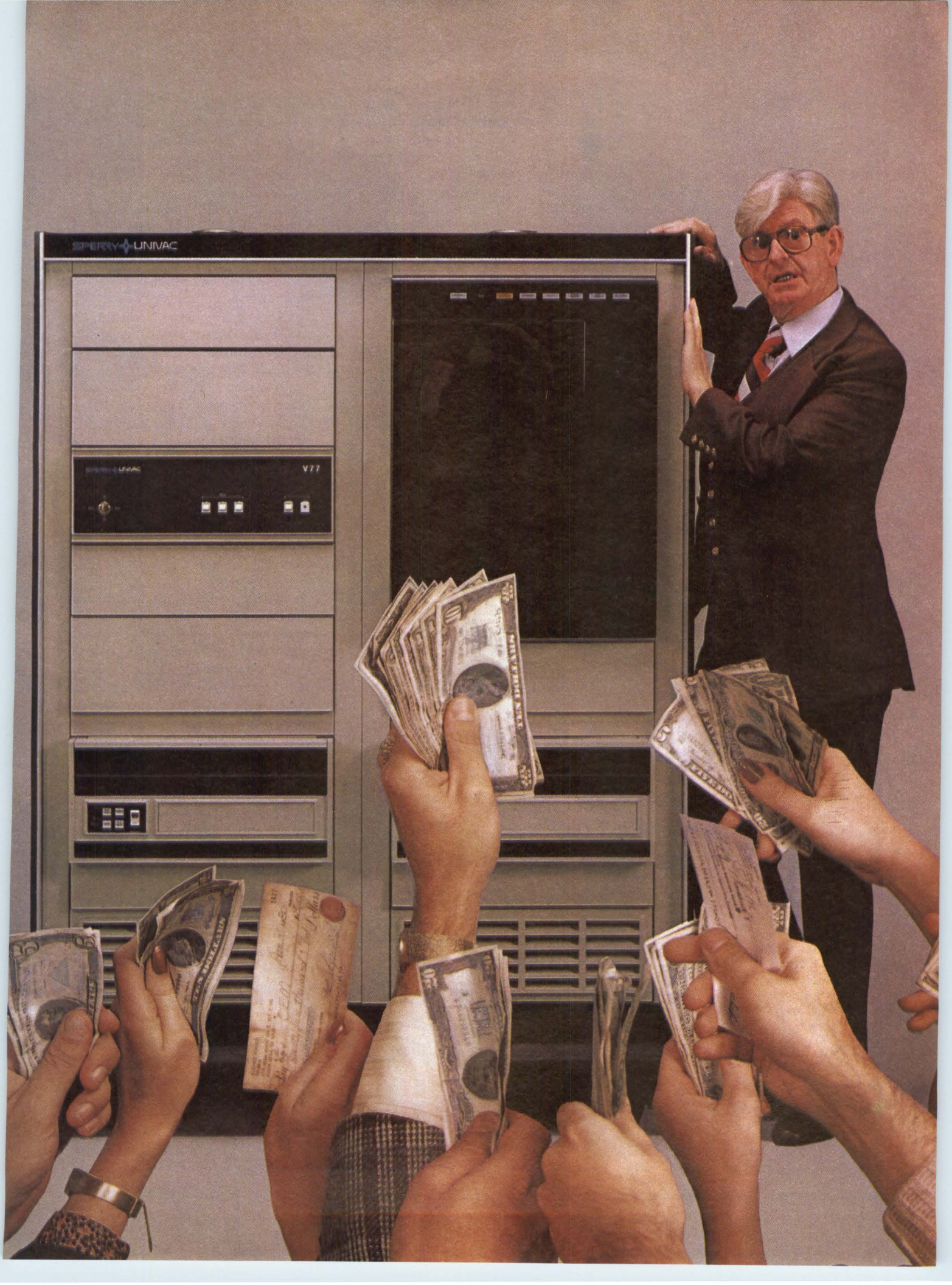
In Europe, write Headquarters, Mini-Computer Operations, London NW10 8LS, England.

In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

SPERRY UNIVAC

CIRCLE 49 ON INQUIRY CARD

SPERRY UNIVAC IS A DIVISION OF SPERRY CORPORATION


SPERRY UNIVAC
V77

Interconnection Test System Offers Software Flexibility

Interconnect verification and error detection for backplanes and bare PC board test fixtures having up to 130,000 points are provided by the N161. In this tester, Teradyne, Inc, 183 Essex St, Boston, MA 02111 has used solid state electronics packaged in fixture cards to interface to units under test. Software, together with a high performance tape system for program storage, provide increased speed, flexibility, and ease of use.

System software offers a choice of testing, and diagnostic modes for different applications. Modular architecture leads the user through job planning, editing, or testing operations using an English language menu displayed on the CRT. In this way, executive software features such as programmable job load sequence, go/no-go or error threshold testing, and single-pin and single-network testing can be implemented online.

A basic system is made up of an M365CX computing controller with 16k memory, control and measurement system, and H747 tape system with four independent cartridge drives. Standard peripherals include CRT display with interactive keyboard, line printer to output error diagnostics, network listings, and remote start unit for production line testing.

Advantage can be taken of a dynamic memory algorithm by expanding basic memory to 112k. This algorithm automatically uses available memory for job plan residence to minimize reference to the job plan on tape, saving access and rewind time. Testing speed is further enhanced by automatic optimizing of the job plan, ordering the test sequence for efficiency, and high speed characteristics of the tape system.

Fixturing configurations, based on standard 64-, 88-, or 128-pin fixture card modules, interface with different backplanes and bare board contacting fixtures. Individual fixture cards are linked daisy chain fashion with single 14-wire cables; two cables connect this chain to the system.

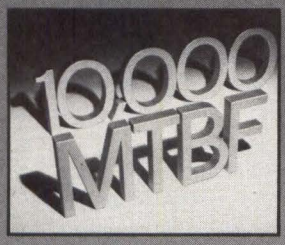
To allow for production line implementation, testing operation has been simplified by providing English language mode choices or default modes. Operator messages can be programmed in a job plan and directed to a CRT display or line printer, alerting the operator to special setup procedures or diagnostic routines. Automatic software system self-checks provide notification of setup mistakes or errors in system function.

An optional management statistics communications package provides realtime datalogging and direct serial communication with a host computer. Consisting of RS-232 interface, realtime clock, 16k of memory, and expanded executive software, the option compiles statistics such as error distribution over time and system utilization. It also permits data to be uploaded to a higher level computer for integration with other management information.

CIRCLE 283 ON INQUIRY CARD

CIRCLE 50 ON INQUIRY CARD

RELIABILITY. IT'S WHAT MAKES FUJITSU THE WORLD'S LARGEST MANUFACTURER OF OEM WINCHESTERS.



That's right! Fujitsu produces more Winchester technology disk drives for the OEM market than any other manufacturer in the industry. The reason for this success is the unequalled reliability of Fujitsu products.

For instance, Fujitsu's M228X Winchester drive delivers more than 10,000 MTBF power on hours of high performance. That's 40% better than the industry standard. And the M228X is fast: 6ms track-to-track (27 ms average) access time. With this kind of performance, up to 169 megabytes of unformatted storage, and Fujitsu's competitive pricing—there is no other choice! Optional head-per-track capacity of 655 kilobytes also available with this series.

80 and 50 MB cartridge drives with SMD interfacing

Fujitsu's advanced technology does not stop at Winchesters! The two front-loading cartridge drives with SMD capability shown here, have statistics only Fujitsu could guarantee. Like access times of 6ms track-to-track (30 ms average), and a reliability factor of over 6,000 poh MTBF. That's 50% better than the industry standard.

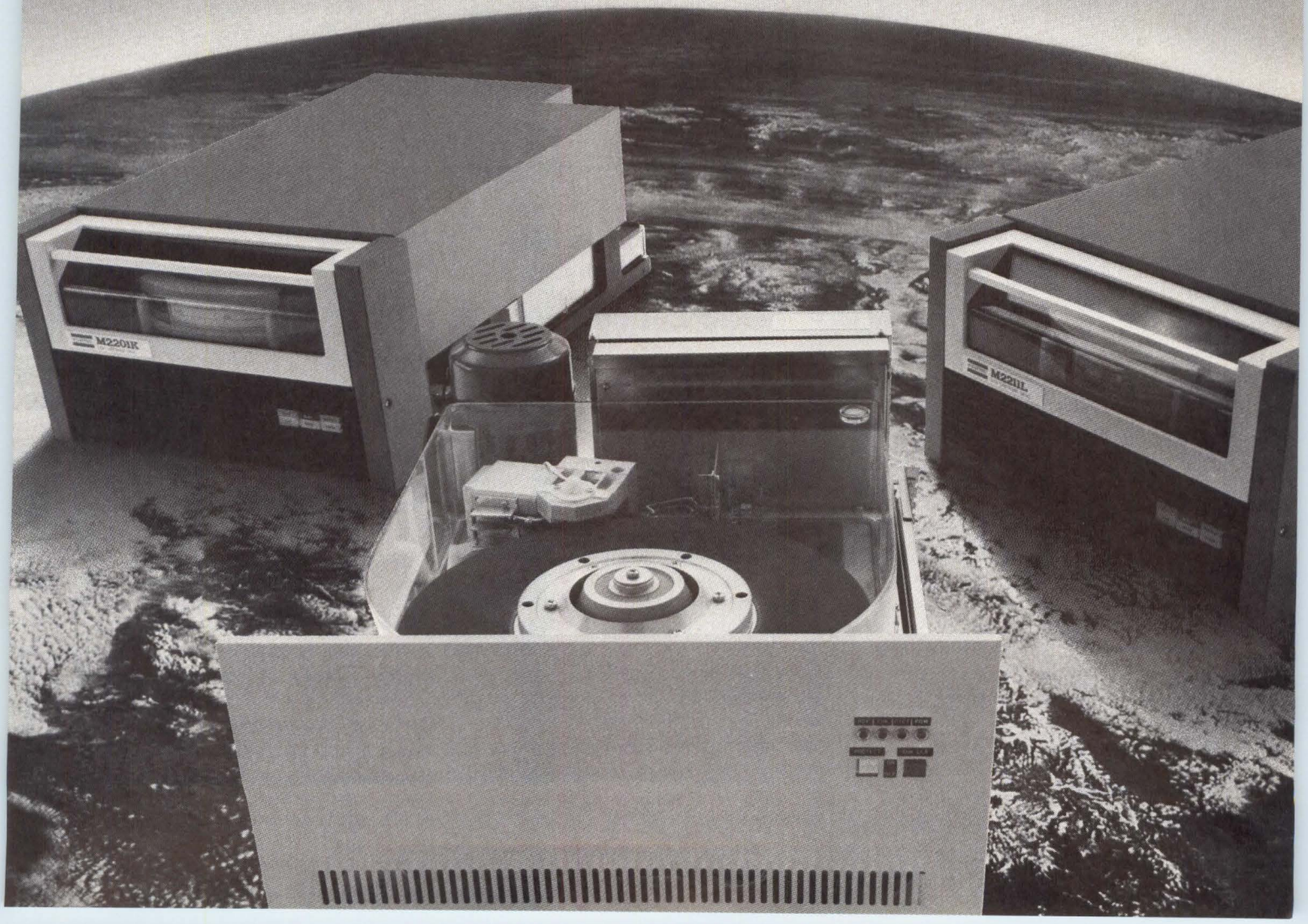
And whether you order the M2211 (80 MB) or the M2201 (50 MB) drive you can say goodbye to data staging. Plus you get a servo/track record system that assures the cartridge interchangeability you need. With features like these it's no wonder Fujitsu's got the world on a platter.

For technical information, (outside California only) phone toll-free 800-538-8175. For sales and service, or evaluation unit, contact: Fujitsu America, Inc., 2945 Oakmead Village Court, Santa Clara, CA 95051. Phone 408-985-2300, Telex 357-402, TWX 910-338-0047.

FUJITSU

The first word in reliability.
The last word in performance.

CIRCLE 51 ON INQUIRY CARD



Pros and Cons of Current 8 and 14" Winchester Disc Drives

OEM system designers who plan high capacity products around recently introduced 8" Winchester disc drives may lose a strong competitive edge, according to W. Ferrell Sanders, vice president of marketing at Shugart, Inc, 435 Oakmead Pkwy, Sunnyvale, CA 94086, a company which offers both 8 and 14" drives. Mr Sanders' concern is that designers will close their minds to the benefits offered by 14" Winchester drives because of the attention generated by the introduction of 8" units by at least eight companies. "As a result of this publicity, users may overlook advantages of the 14" Winchester fixed disc drives," he stated.

In general, he points out, Winchester drives are the most cost-effective and reliable rotating memory peripherals available. "Three of the technology's major attributes are largely responsible for this reputation. First, the drives employ low mass heads which start and stop in contact with the media. These head assemblies, which are relatively simpler and contain fewer parts than those in prior technologies, significantly contribute to the low cost factor.

"Secondly, performance is enhanced because the heads operate at a reduced flying height relative to other rigid disc technologies. This allows reading of more densely packed data than has been possible with previous products. Finally, the media and read/write heads are enclosed in a sealed environment. Thus, Winchester disc drives provide inherent protection from various kinds of contamination that may occur with removable or other types of fixed media."

Winchester drives complement the widely used floppy disc products. OEMs designing higher performance systems, however, are not presented with an alternative to use in lieu of floppy products for system residence memory, operating system storage, and mass storage memory. If the designer chooses to upgrade to Winchester technology, the 8" drives introduce the dimension of size into the capacity and performance question. Even then there are no firm guidelines because both products overlap extensively in both cost and performance.

This results from the opposing product design objectives used by the various manufacturers, according to Mr Sanders. "For Shugart and apparently one other company, low cost was the most important goal." At Shugart this was achieved by minor tradeoffs in performance to obtain the lowest cost, resulting in 5M- and 10M-byte units costing $995 and $1205 in OEM quantities. "Pertec and IMI, on the other hand appear to have targeted for higher performance and capacity . . . the Pertec drive with 20M bytes sells for about $1600 and the IMI 11M- and 20M-byte units for approximately $1600 and $1900. Between these two categories, is a 14.5M-byte 14" drive, Shugart's SA4004, which costs less than $1300 in OEM quantities." This product fits a 5.25" (13.34 cm) panel space and weighs 35 lb (16 kg). A 29M-byte version (SA4008) sells for approximately $1600.

"On a cost-per-megabyte basis, the 14" drives are usually the most cost-effective solution when the requirement is for more than 10M bytes. For example, Shugart's SA4004 has a cost/megabyte of approximately $86," according to Mr Sanders, while "the SA4008, has a cost of $57/megabyte." "Low end 8" drives, SA1002 (5M-bytes) and SA1004 (10M bytes) have an estimated cost of $187 and $113/megabyte, respectively."

Mr Sanders sees the floppy size package as being the key advantage of the 8" fixed discs. "These disc drives can be easily exchanged for floppies because some of them fit right in the same slot that a floppy does. Additionally, in Shugart's case similarity of electronics is also a design feature. This enables users to build a common interface to handle both fixed and floppy drives."

However, according to Mr Sanders, manufacturers might be wise, as system requirements for capacity and performance increase, to place less importance on package size and more on price/megabyte capacity. The user must also consider the difficulty of new product start-up when projecting system designs around 8" units, since the 8" units are not available in quantity and 14" units have been in production for sometime already.

Interactive Software Aids In Designing Efficient, Logical Data Bases

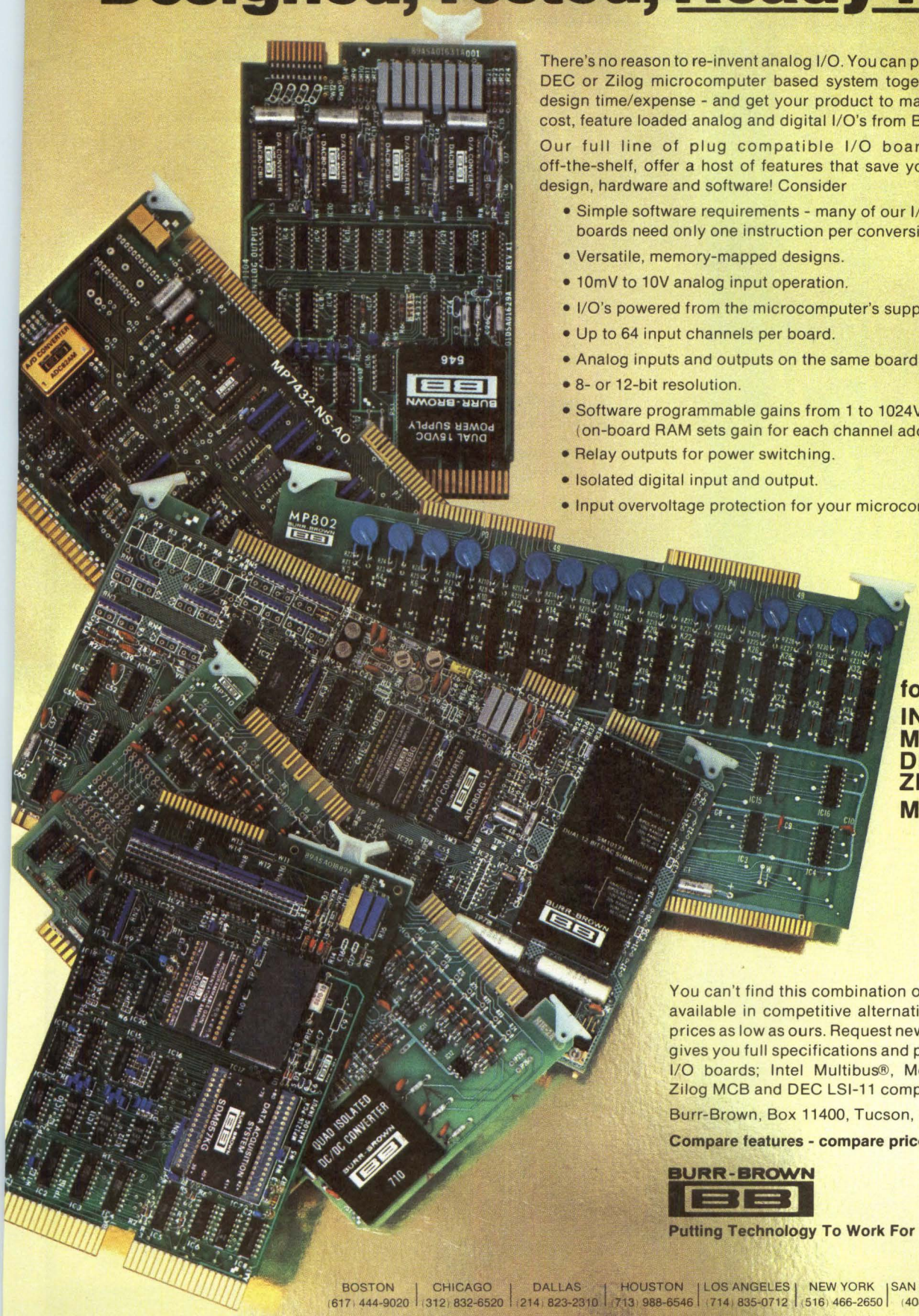
Many corporations are searching for a means to design more efficient database structures which will save time and personnel resources and lower future maintenance costs. At the same time, it is important that the companies be able to understand and define their information requirements to meet the needs of end users.

Data Designer is an interactive design tool that helps build stable, yet flexible data structures. Developed by the DMW Group, Inc, 2395 Huron Pkwy, Ann Arbor, MI 48104, the stand-alone tool aids in design of logical data bases. To perform a design process, its user interactively defines any number of user VIEWs for an application, then the package takes the defined VIEWs through a canonical synthesis to generate a database design. Resulting reports and plots describe the inherent relationships among data elements, yielding a design in third normal form. A design in that form can then be translated into any data base management system whether hierarchical, network, or relational.

Written in ANSI FORTRAN IV, the software will run on any computer that runs FORTRAN IV and has 1.7M bytes of virtual storage. It has been implemented with direct access file structures, and is fully compatible with IBM and Amdahl equipment; it can be installed with minimum effort on other system configurations. Users may have as many dictionary and user VIEW files as needed. Runs of less than 500 user VIEWS require less than 1 s of execution time. Output designs are plotted with a standard interface to CalComp and Zeta plotters as well as Tektronix gas tube plotters.

CIRCLE 285 ON INQUIRY CARD

HERE'S YOUR ANALOG I/O Designed, Tested, Ready Now!



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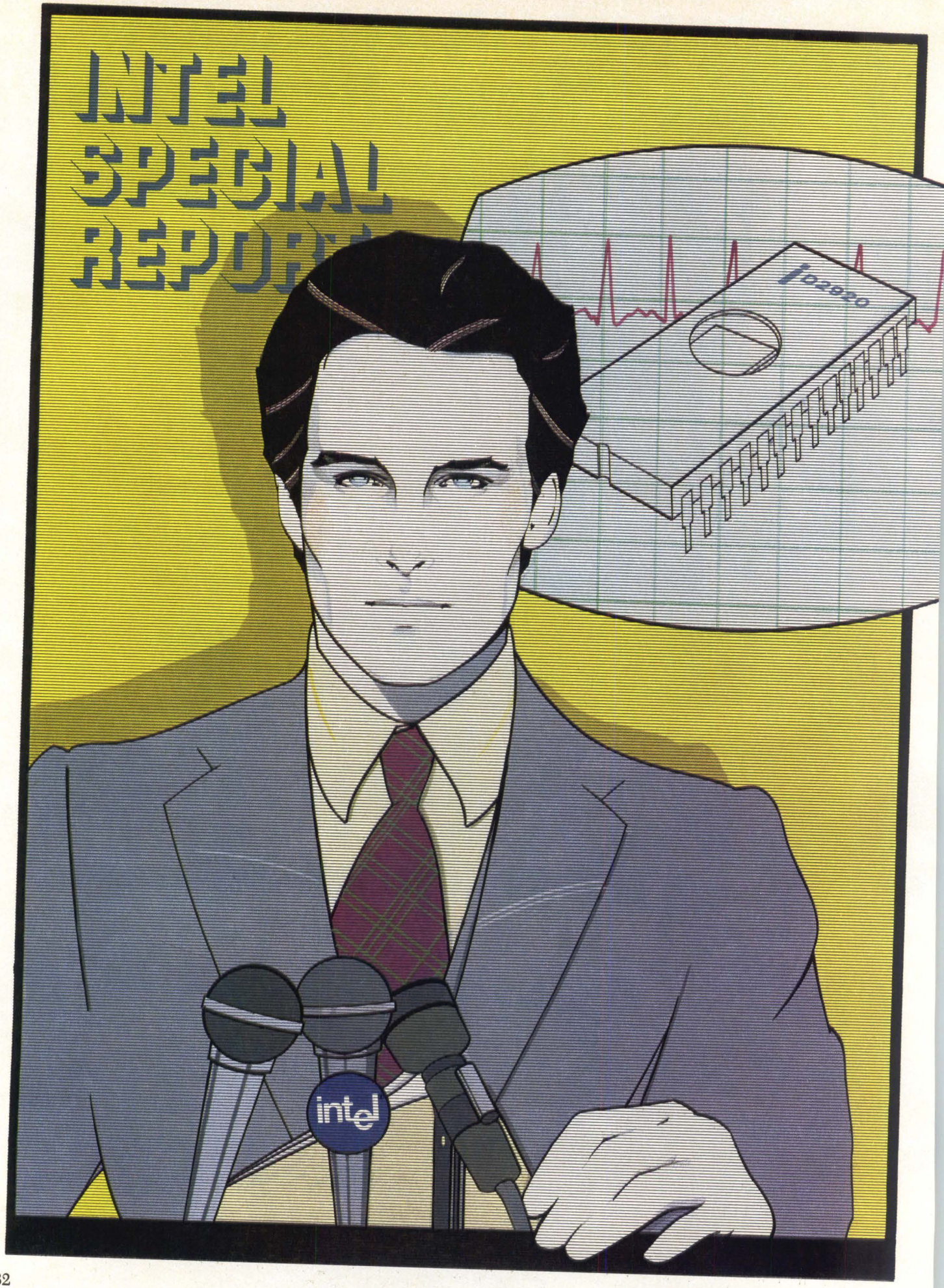
CIRCLE 52 ON INQUIRY CARD


INTEL
SPECIAL
REPORT
i02920
intel

LSI Breakthrough for Analog

Intel announces the 2920 Signal Processor, first general purpose, real-time system on a chip.

Good news for analog designers. Intel breaks a new barrier in microelectronics: The first intelligent chip powerful enough to process analog signals in real time. Plus a computer-aided development package to help speed your systems to market faster than ever before.

Intel's 2920 is a complete, micro-sized signal processing system that packs the equivalent of over 18,000 transistors on a single chip. It operates hundreds of times faster than current digital processors. And best of all, the 2920 allows designers to *program* system values quickly, instead of having to match and tweak components.

A revolution in analog design

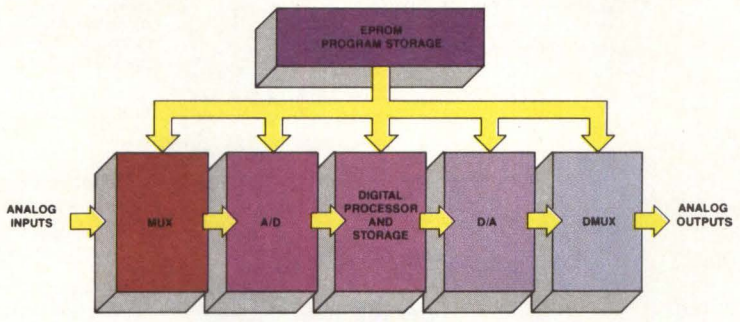
From the beginning, LSI technology has helped designers achieve dramatic improvements in product size, design cycles and manufacturing economics. But until now, the speed and complexity of analog processing has stood in the way of general purpose, single chip solutions for real-time applications.

Today, Intel's 2920 Signal Processor brings the power and flexibility of LSI to the analog world. Because of its size, the 2920 can fit in spaces too compact for traditional analog solutions. Because the 2920 is programmable, product development and time-to-market are speeded significantly. Finally, because the 2920 is a solid state device produced with Intel's proven NMOS process, reliability and manufacturing repeatability are assured to a degree not possible with previous methods.

Micro-processing for the real world

Applications for the 2920 are as broad as your imagination. Since analog designers can program the 2920 processor to perform a large number of standard building block functions, the chip can be used as an entire subsystem. Implement such functions as complex filtering, waveform generation, modulation/demodulation, adaptive processing, and even non-linear functions. This broad capability makes the 2920 an ideal single chip solution for virtually any application in the DC to 10 kHz range.

And like the digital microprocessor, the 2920 is destined to create entirely new classes of applications: products that are smaller, simpler, and less costly to produce. It gives a competitive advantage to companies in such areas as process control, test and instrumentation, guidance or control systems, telecommunications, speech processing, and seismic or sonar signal processing.



Functional Block Diagram of the 2920 Signal Processor

How the 2920 simplifies system development

Programming Intel's 2920 Signal Processor is fast and easy to learn—far less complex than the component matching it replaces. Most importantly, Intel provides the complete support tools and design workshops you need to start designing 2920 systems today.

Our SP20 Support Package and Intel's Intellec® Microcomputer Development System allow you to develop and debug by simulating your system in software. Just program functions according to your system schematic, then specify input and operating values. Together, Intel's development aids let you see how your system will work before you even build a prototype. Best of all, because you develop in digital code, your prototype system will be duplicated precisely in manufacturing.

Start making news with your product

Everything you need to begin designing a new generation of real-time analog processing systems is here today: Intel's 2920 Signal Processor, SP20 Support Package, and the Intellec Development System. For detailed information, including our new 2920 brochure, plus a schedule of Intel's nationwide 2920 Design Workshops and Seminars, contact your local Intel sales office or distributor. Or write Intel Corporation, Literature Department, 3065 Bowers Avenue, Santa Clara, CA 95051. Or call (408) 987-8080.

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CIRCLE 53 ON INQUIRY CARD

Why Verbatim® re-invented the wheel.

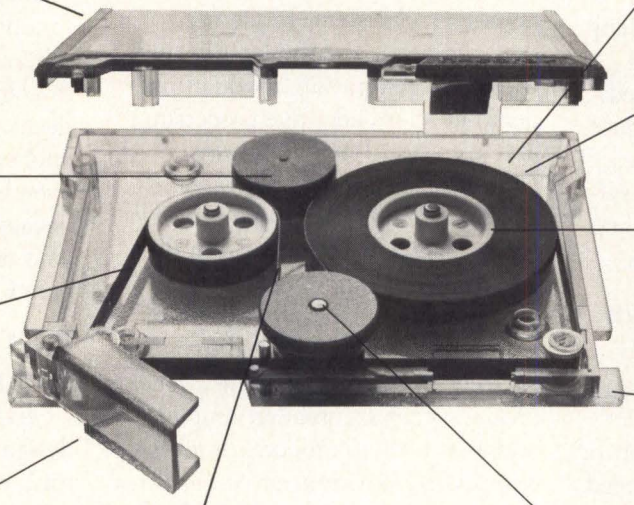
Our patented "Belt Driven Floating Roller" is the key engineering design element in the TC-150. The Verbatim TC-150 offers at least 10 improvements.

1. Our **unitized construction,** consisting of symmetrical shell halves, provides structural stability and the strength of Lexan.® The shell halves overlap to seal out dust. Construction is simpler and less expensive, yet the entire shell has thermal consistency. No differing rates of expansion to stress critical tape paths.

2. Our simplified Floating Roller design, employing fewer moving parts, **reduces variability** caused by environmental changes, age and use.

3. Our TC-150 mini data cartridge uses Verbatim's unique **gamma ferric oxide digital** tape. This special formulation has been extensively field proven to have long life and low head abrasion.

4. After final assembly each cartridge is **completely certified** to be 100% error free on first pass.



5. Our new drive belt is made of cross-linked polyurethane, so it is **more durable and temperature-stable** than other belts. This gives you better tension, mechanical and recording performance.

6. Our Floating Roller design, which eliminates the potential problems created by corner rollers, **improves recording quality** by producing repeatable tape tension across the read/write head.

7. Our metal-free Lexan® shell design **resists static buildup.** A metal baseplate can cause damage from static electricity as the cartridge is inserted into the system.

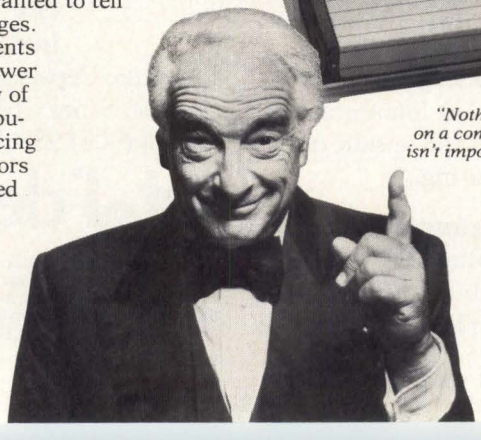
8. The tape hub material was formulated to produce a rate of thermal expansion that exactly matches the tape's. This **prevents "pack shift"** and uneven tape wear.

9. **Less power is consumed** when driving our Floating Roller cartridge because the elimination of corner rollers dramatically lessens friction.

10. Since we have eliminated the corner rollers, **we don't need the metal baseplate** which is subject to warping, dents and burrs.

Durable, re-usable, stackable plastic box provides secure storage at no extra cost.

We completely re-engineered the Verbatim TC-150 mini data cartridge for the good reasons noted above. We don't often mention product improvements, because you have come to expect only the latest and best developments from Verbatim. But we're so proud of the better-than-ever TC-150 data cartridge that we wanted to tell you about the changes. Test our improvements —happily, they'll lower your costs. Call any of the Verbatim distributors listed on the facing page. Our distributors will also be delighted to supply you with quality Verbatim diskettes and cassettes.



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CIRCLE 54 ON INQUIRY CARD

RSX-11 Family Extended to Include Forms Management

Extensions to the FMS-11 forms management software allow its use not only on small and medium systems but all PDP-11 minicomputers and terminals running the RSX-11 operating system. Consisting of a series of utility programs that use key VT100 terminal features, the package, from Digital Equipment Corp, Maynard, MA 01754, enables screen equivalents of standard forms to be developed.

The revised implementation supports applications written in FORTRAN IV, FORTRAN IV-PLUS, BASIC-PLUS-2, COBOL, and MACRO-11. Applications programs can call for data input; neither compilation or linking is required to bind the application to the terminal driver. All user and terminal I/O functions are developed separately from the program and data processing aspects of the application.

CIRCLE 286 ON INQUIRY CARD

Improved Software Expands Capacity of Multiterminal Computer

Software improvements for RX30 Marathon multiterminal computer systems save time, and provide greater security, capacity and ease of use. Among the enhancements developed by Rexon Business Machines Corp, 5800 Uplander Way, Culver City, CA 90230, is a direct file access method based on a variation of B-tree technology which greatly reduces the time required to generate a record in a direct file, while keeping access times for growing records constant.

The security feature protects proprietary software from unauthorized distribution. A pair of coded plugs are provided to authorized users. Insertion of both plugs permits unlimited access to software; without them there is no access.

In addition, the number of files which may be resident on one disc has been increased from 736 to 1500. The number of devices that may be opened concurrently from one task has also been increased from the standard 8 or 10 to a maximum of 63.

CIRCLE 287 ON INQUIRY CARD

Hardware/Software Pack Achieves Interactive Graphics with VAX

Graphic 7 display system users can achieve interactive stroke/refresh graphics with the DEC VAX-11/780 by programming in FORTRAN subroutine calls. This capability is provided by the 5714 high speed parallel DMA interface and 7771 VAX I/O driver software package offered by Sanders Associates, Inc, Daniel Webster Hwy S, Nashua, NH 03061.

Written in VAX assembly language, the I/O driver runs with the VMS operating system. Both hardware and software of the Graphic 7 system are compatible with the DR11-B interface option in the VAX.

The model 7764 FORTRAN support program for the display system permits the user to work in his own coordinate system using FORTRAN subroutine calls. This program's multiple paging feature allows highly interactive tasks to be performed with dynamic image movement and modification.

CIRCLE 288 ON INQUIRY CARD

Interactive Software Serves in Online Program Maintenance

An online program maintenance tool, PROMT is an interactive terminal oriented software product that provides easy to use facilities for program development, library maintenance, data entry, and job submission. Developed by Goal Systems Corp, PO Box 29481, Columbus, OH 43229, the software runs as an application under the Westinghouse WESTI teleprocessing system.

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CIRCLE 289 ON INQUIRY CARD ☐

Applying Microprocessors to Machine Tool Controller Design, Part 1

Thomas A. Seim

Desert Microsystems, Incorporated, Pasco, Washington

This design case study has been divided into two parts. Part 1 carries the discussion through linear interpolation and data representation; Part 2, to be published in April, begins with parabolic interpolation and completes the review.

Once strictly the province of specialized controllers and minicomputers, numerical control applications are now commonly handled by microcomputers. For instance, all normal functions found in a 5-axis contouring controller can be performed by an 8080 microprocessor, almost entirely in software. The key is the careful partitioning of software functions and the simplifying of computations.

In a typical example, a controller that provides ultra-high precision utilizes a moderate performance minicomputer. Positional information is maintained to tenths of microinches and key variables to 64 bits. This computer system uses virtually no special purpose hardware since all control functions are performed in software. However, it is feasible to replace the minicomputer with a microprocessor based controller, thereby simplifying the processing requirements for typical numerical control applications.

Numerical controllers move machine tool slides and rotary tables in response to digital commands from a paper tape reader or a control computer. Servo drives replace handcranks and gear driven screws on the machine tool. Some systems also have measurement devices, such as laser interferometers, attached to the slides for position feedback. Early controllers were built with custom digital logic and magnetostrictive delay lines for memories.

For economic reasons, the first use of computers involved control of several machine tools. This configuration—known as direct numerical control (DNC)—was generally unsuccessful due to cost and reliability problems. However, as minicomputer prices dropped, it became practical to dedicate a single computer for each machine tool. Called computer numerical control (CNC), this technique has enjoyed greater success than DNC systems.

Numerical controllers fall into one of two categories: point-to-point and contouring. Point-to-point controllers precisely position the machine tool to discrete points only; the path between points is of no importance. Examples of applications using point-to-point positioning include a numerically controlled drill press or spot welder. On the other hand, milling machines and lathes require precise control of the path of the cutter between prescribed points. In these applications the controller drives the machine tool through a specified contour, which may be a straight line or, in more complex controllers, a parabola or a circle.

Core of many numerical controllers is the digital differential analyzer (DDA). This circuit simultaneously generates servo commands for linear contouring and keeps track of the distance traveled. Combining functions in this manner was ingenious at the time digital circuitry was expensive. Some designs have tried to duplicate the DDA function in software, but with mixed results. The major problem is that the DDA function must be executed at relatively high speed (10,000/s) to provide reasonable servo control. Adapting this technique to microprocessors rapidly saturates their processing capabilities.

One solution lies in analyzing numerical controllers as separate sampled data systems, optimizing each function according to requirements of the application. To date, the use of microprocessors in numerical controllers has been limited by their reduced computational capacity. Yet, with careful system design, the capacity of many 8-bit microprocessors is more than adequate for complex numerical control applications.

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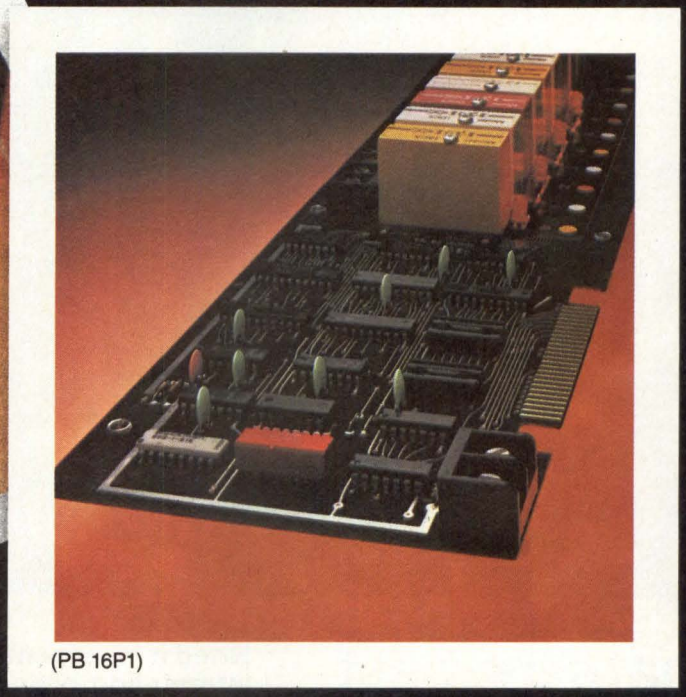

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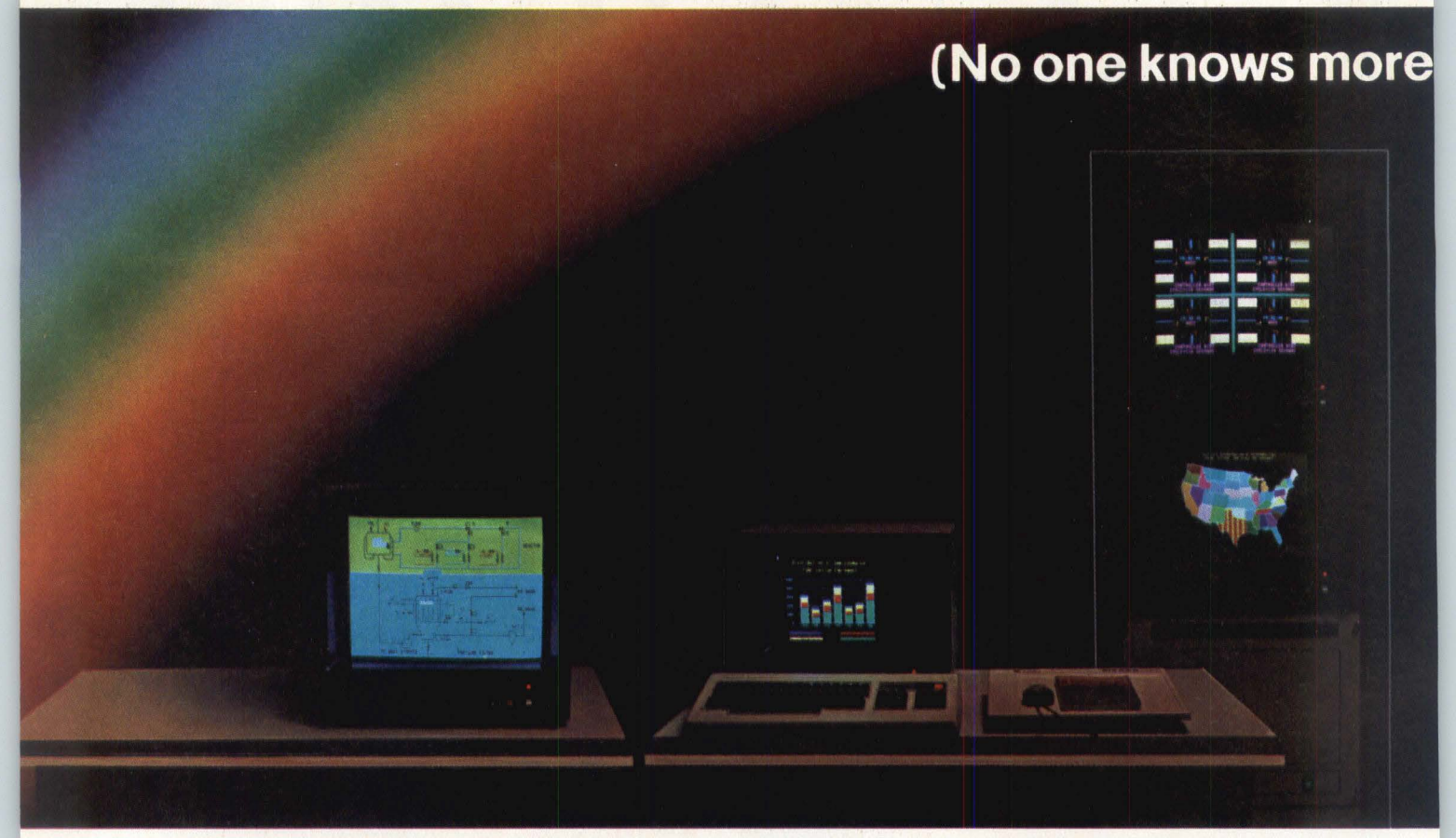

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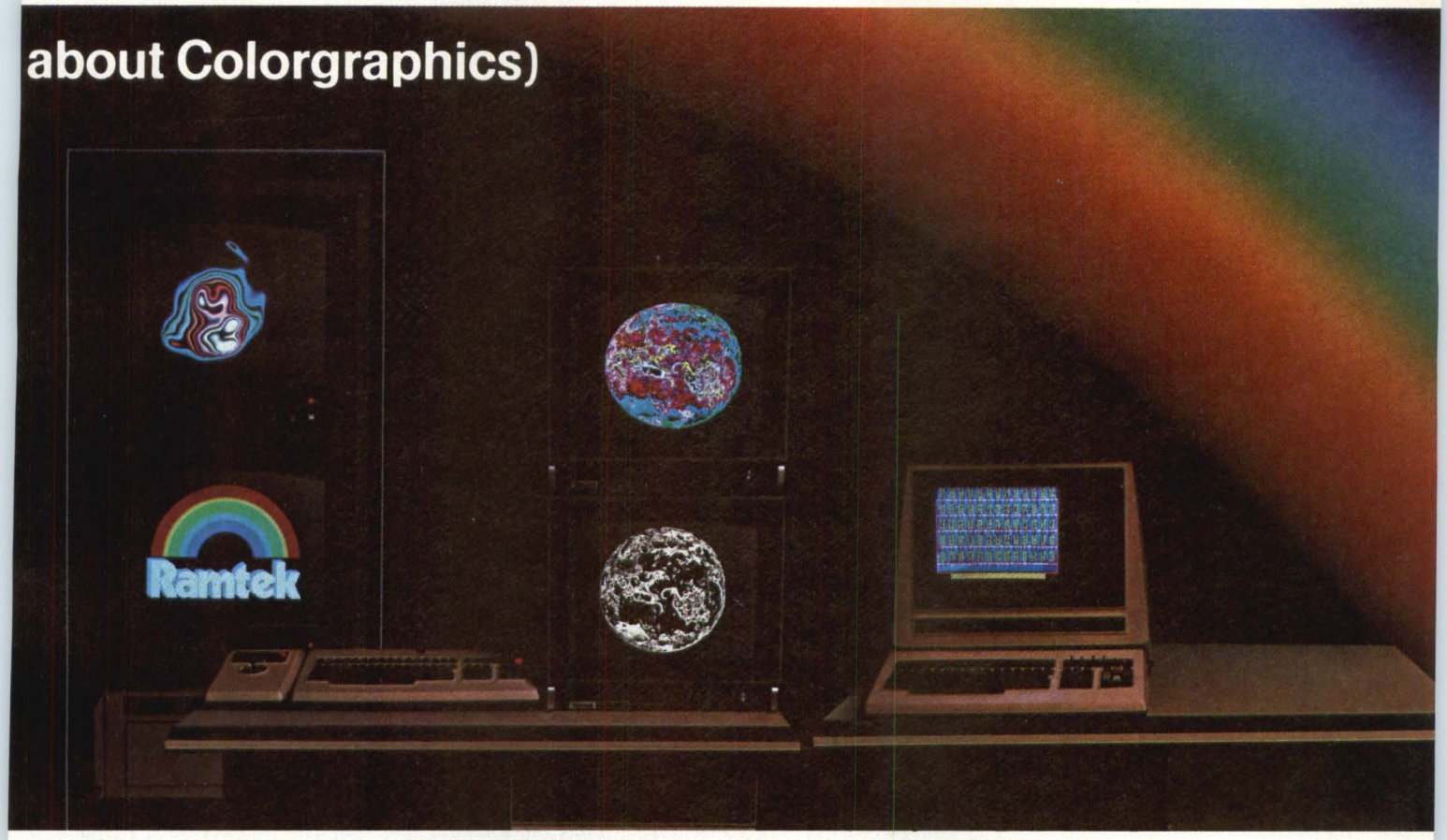

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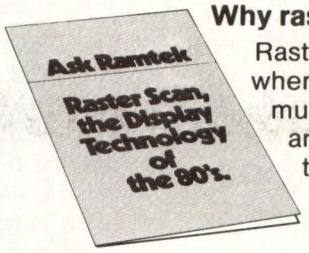

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Digital Differential Analyzer

A digital differential analyzer (DDA), which approximates the integration of a function by summation, solves differential equations for use in machine tool controllers. Consider the simple differential equation to describe linear motion in dimension x:

$$x = x_o + \dot{x} \cdot t \qquad (1)$$

where

$\dot{x} = dx/dt$

Eq (1) can be solved by digital circuits (Fig 1) that add the integrated value to the sum when given an add command; these commands are issued at a constant frequency for integration with respect to time. The initial integrand value is $\dot{x}$, and may be changed during integration with the increment/decrement command. In a machine tool control application, the overflow output directs a slide positioning servo to move a small incremental distance, such as 0.001″ (0.025 mm). Overflows from the sum register represent the integral and occur at an average rate proportional to $\dot{x}$ (velocity command); the total number approximates the integral of velocity over time. A velocity command of 75% of full-scale velocity is illustrated.

Overflows ensue at irregularly spaced intervals, a major problem for stepping motors. A solution to this problem generates overflows at a higher rate than necessary and then divides them with a counter to the desired rate. This averages the pulse rate, but it requires additions to be performed much faster than before.

The addition rate makes it impractical to implement DDA algorithms in software, especially when using microprocessors. Other difficulties arise when cascading DDA circuits for higher order functions, such as parabolic interpolation, since the errors may be integrated from one stage to the next at an unacceptable level.

Sampled Data Control Systems

Sampled data systems process signals by transforming them to discrete points with a sampler. Digital circuits in general and computers in particular are ideally suited for complementing sampled data systems because of their incremental structures. Originally, analog circuits with actual samplers were used to construct sampled data systems, but that quickly changed as digital computers became readily available.

A fundamental requirement of all sampled data systems is that the sampling must be at least twice the rate of the highest frequency applied to the inputs (Shannon's theorem). In numerical control applications, sampling will depend on the performance required of the machine, but is usually very slow (envision the rate at which a tool slide could be made to oscillate back and forth). Nonetheless, the sampling rate should be moderately high to minimize errors unavoidably created by representing a time-continuous signal with discrete points. Consider, for instance, a machine with 0.001″ (0.025-mm) position feedback moving at 1″ (25.4 mm)/s.

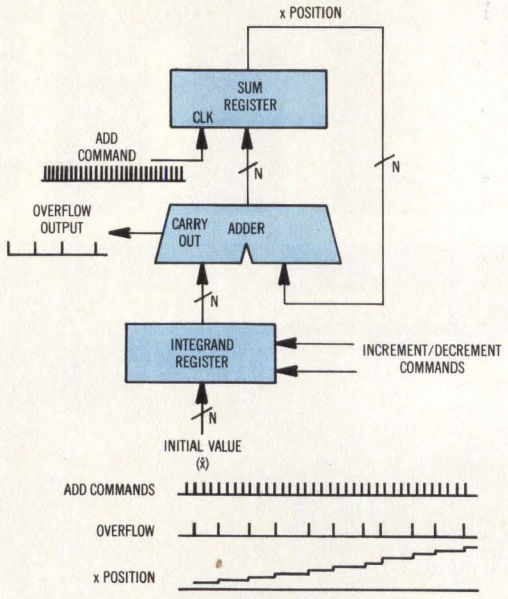

Fig 1 Digital differential analyzer circuit. DDA adds initial value of velocity, $\dot{x}$, to sum register at fixed rate. Overflows occur at frequency proportional to $\dot{x}$ and may be used as commands to incremental positioning system. However, pulse to pulse periods will probably still vary

Sampling positions at a rate of 100/s will result in data changing about 10 units/sample, which may seem excessive if 0.002″ (0.050-mm) accuracy is specified. This may be more than adequate when compared to the upper frequency response of the slide, which may be 10 Hz. Mechanical frequency responses rarely exceed 200 Hz (for very high performance servos), and heavy machine tools are usually limited to a few hertz or less.

Linear Interpolation

The fundamental control procedure drives the machine tool in a straight line path between two points [Fig 2(a)]. Computing points along the path is called "interpolation" or, since it is a straight line, "linear interpolation." (Other types of interpolation are circular and parabolic.) The interpolation process occurs in the block labeled "contour generation" [Fig 2(b)], which is fed the interpolation endpoints, x_i and y_i. A sequence of discrete points representing the contour is fed to two position feedback control loops, one for each axis.

Machine tool slides move from one position to the next in a series of small steps whose size is dependent on the velocity and the sampling rate. The previously mentioned step size of 0.001″ (0.025 mm) between samples would probably be unacceptable if the slides actually moved nonuniformly, speeding up as the position is incremented, and stopping until the position is updated again. A servo feedback control loop prevents

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this from happening; instead, the feedback loop maintains approximately the correct machining velocity between samples [Fig 2(c)]. This is the principal difference with the DDA technique, which attempts to regulate on a much finer scale. The computational process used is identical to the DDA, but the system design philosophy is substantially different.

To understand the contour generation process it is helpful to begin with the basic equations of motion. These are first presented in continuous form and are then converted to their discrete counterparts. For a first order system, the continuous equations of motion are

$$x = x_o + \int_{x_o}^{x_1} \dot{x}\, dt$$

and

$$y = y_o + \int_{y_o}^{y_1} \dot{y}\, dt \qquad (2)$$

Integrals are approximated by a summation

$$\int_{x_o}^{x_1} \dot{x} dt \cong \Sigma\, \dot{x}\, \Delta t \qquad (3)$$

This operation is performed at discrete intervals in time (Δt is the sampling period). Instead of being continuous variables, the values of x and y are also computed at discrete intervals. In the following discrete formula, the particular interval is represented by the subscript i:

$$x_{i+1} = x_i + \dot{x} \cdot \Delta t \qquad (4)$$

The continuous equation of motion is approximated by executing this computation from $x_i = x_o$ to $x_i = x_1$, where the number of iterations depends on the values of velocity, $\dot{x}$, and the sampling period, Δt. This single equation is all that is needed to implement a linear interpolator.

Fig 2(c) illustrates a few steps of the interpolation process on a magnified scale. Commanded position increases by relatively large steps at every sampling point. Initially, the x slide is not moving, creating an error. This error generates a servo command, accelerating the slide. After a few samples, the slide is closely tracking the commanded position, and the velocity between samples is constant.

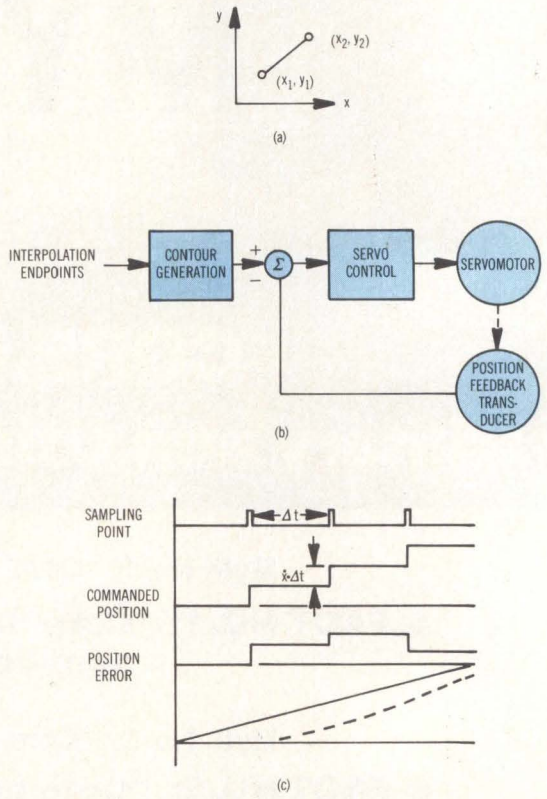

Fig 2 Linear interpolation. Contouring system has logic for each axis to generate intermediate points from endpoints (a). Intermediate points are fed to position servos to achieve smooth motion. Feedback control operates from error, or difference, between commanded and actual position to develop drive command (b). Interpolation steps are shown in (c)

Data Representation

A vital aspect of digital designs, whether using hardware or software, is the representation of data within the system. Selection of the format must not only satisfy the accuracy requirements, but also consider errors incurred during computations such that the system accuracy is within specifications. Data must be stored efficiently for the shortest computation time and, in some cases, minimal memory utilization. Since numerical controllers are used with many types of machine tools, any data representation analysis must make compromises.

A key format is positional data. Representing 100″ (254-cm) spans to 0.001″ (0.025-cm) resolution requires five decades of range. With 10 bits required per three decades (in binary), 17 bits plus 1 sign bit are sufficient. Several bytes are used to store each set of data (three, in this case), leaving six extra bits of precision. These are stored in consecutive memory locations [Fig 3(a)].

The precision that has to be carried in the discrete motion equation is much greater than the position data. A requirement of this computation is that for any movement the maximum error is ±1 least significant bit (LSB). Since 1 LSB is already one sixty-fourth of the specified control system accuracy, the error contribution during interpolation is negligible. Sixteen extra bits are added to the computation to meet this goal [Fig 3(b)], for a total of 40 bits—or five bytes—of precision being carried. Presuming that $\dot{x}_1 \cdot \Delta t$ is accurate to 40 bits, the total error depends on the number of iterations which,

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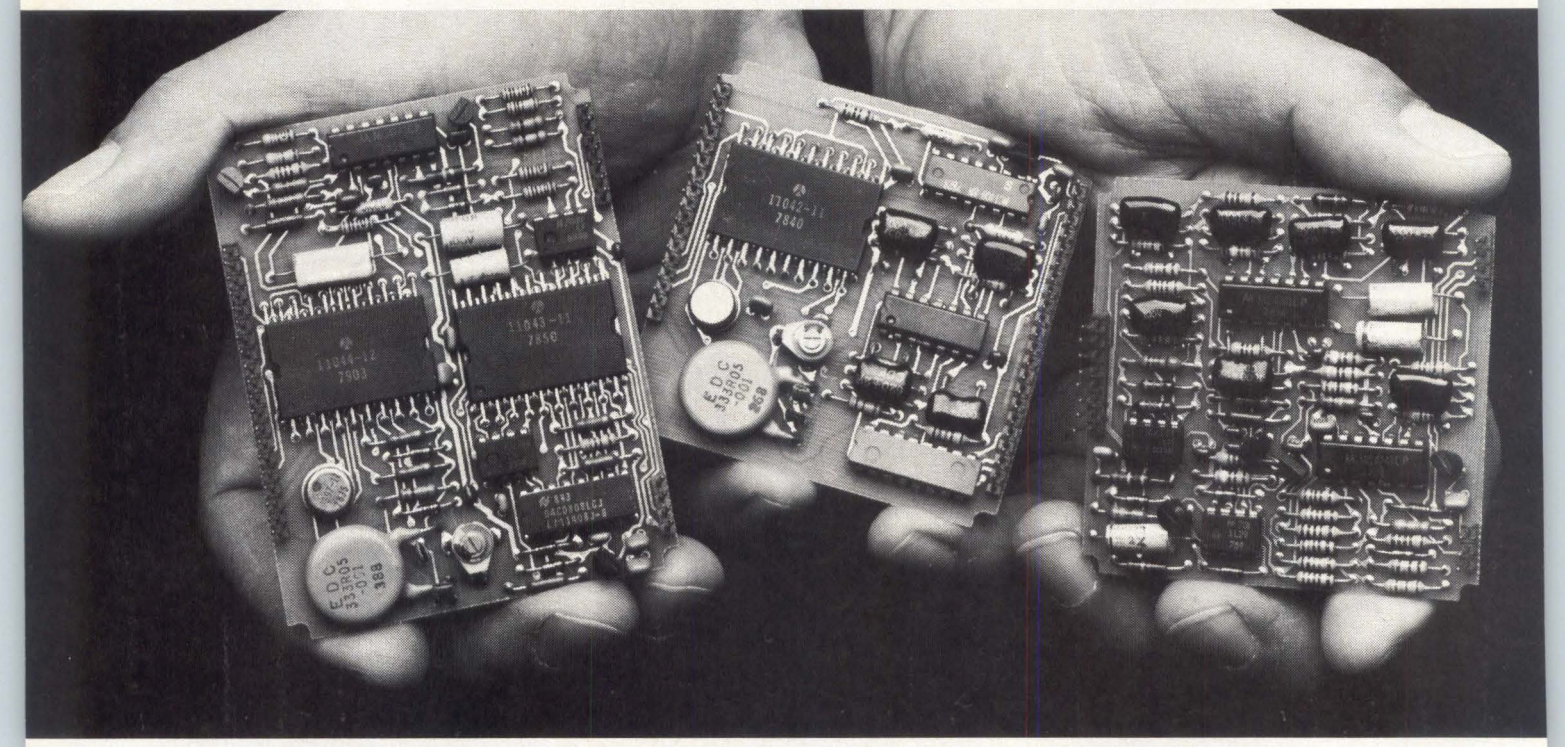

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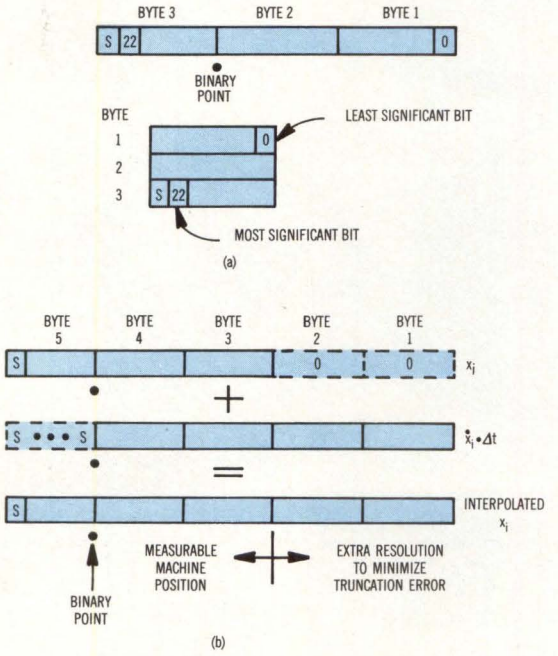

Fig 3 Consecutive memory locations. Machining data require more accuracy than afforded in one 8-bit byte; multiple precision data are stored in consecutive steps (a). Because accuracy is still insufficient for interpolation calculations, two extra bytes are carried for total of five bytes

in turn, is a function of the elapsed time during interpolation. An error in the LSB will propagate to the position data bits after 65,000 iterations, or 650 s at a 100-Hz sampling rate. Any combination of machining velocities and distances taking no more than 650 s will keep the interpolation accurate to within 1 LSB.

The term $\dot{x}_i \cdot \Delta t$ is calculated prior to starting interpolation; since it is a constant, it need only be computed once. Values for $\dot{x}$ will generally not be provided as input data, which states the "feedrate" between given points (the velocity along the machining path). The x and y velocities can be computed from

$$\dot{x}_i = \frac{\Delta x_i}{(\Delta x_i^2 + \Delta y_i^2)^{1/2}} \text{ (FEEDRATE)}$$

and

$$\dot{y}_i = \frac{\Delta y_i}{(\Delta x_i^2 + \Delta y_i^2)^{1/2}} \text{ (FEEDRATE)} \qquad (5)$$

where $\Delta x_i = x_{i+1} - x_i$ and $\Delta y_i = y_{i+1} - y_i$. A burden is placed on the software if this feedrate has to be computed to 40 bits.

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```
INPUT:
        H, L        ADDRESS of ẋ•Δt
        D, E        ADDRESS OF x_i

OUTPUT: x_i IS REPLACED BY SUM

MADD5:  LDAX  D     GET FIRST BYTE OF ONE ARGUMENT
        ADD   M     ADD FIRST BYTE OF OTHER ARGUMENT
        STAX  D     SAVE FIRST BYTE OF SUM
        INX   D  }  ADVANCE DATA POINTERS TO
        INX   H  }  NEXT BYTE
        LDAX  D  }  REPEAT SEQUENCE FOUR TIMES
        ADC   M  }  EXCEPT USE "ADD WITH CARRY"
        STAX  D  }  INSTRUCTION TO PASS CARRIES
        INX   D  }  BETWEEN BYTES
        INX   H  }
        LDAX  D
        ADC   M
        STAX  D
        INX   D
        INX   H
        LDAX  D
        ADC   M
        STAX  D
        INX   D
        INX   H
        LDAX  D  }  POINTERS DO NOT NEED TO BE
        ADC   M  }  INCREMENTED AFTER LAST
        STAX  D  }  ADDITION
        RET
```

Fig 4 5-Byte addition subroutine. Coding without loops provides shortest possible execution time

Fortunately, examination of the extreme cases shows that floating point arithmetic with 24-bit mantissas is sufficient. To make 65,000 iterations without position overflow, $|\dot{x}\cdot\Delta t|$ must have 16 leading zeros, or 24 bits carried in the computation. For the unlikely case where $|\dot{x}\cdot\Delta t|$ is a full-scale value, only one iteration is possible without overflow. This also requires only 24-bit precision. Note that 40-bit precision is not necessary, but 40-bit range is. This observation allows the use of available floating point software packages.

The principal piece of software needed for the interpolation process is a 5-byte addition routine. Fig 4 is a program listing of such a subroutine for the 8080 microprocessor. Memory addresses of x_i and $\dot{x}\cdot\Delta t$ are loaded into the D,E and H,L register pairs, respectively. This subroutine executes in 86 μs (8080 at 2 MHz), or less than 1% of the sampling interval. Clearly, this operation would not be a limiting factor in the number of axes that one microprocessor can control.

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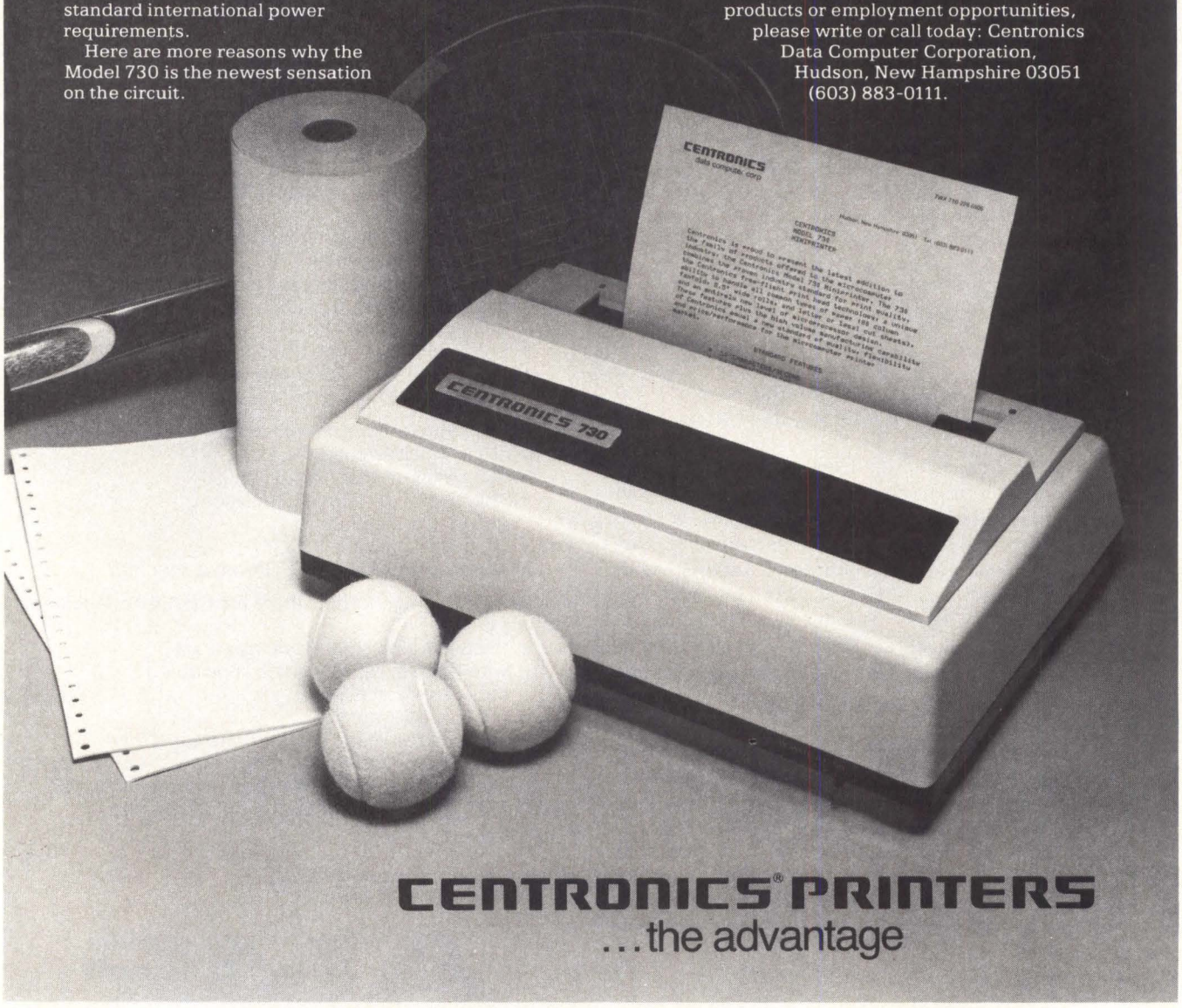


CENTRONICS® PRINTERS

...the advantage

Traffic Registration Induction Loop Detector Is Controlled by Microprocessor

A microprocessor controlled loop detector, said to be the world's first, measures highway traffic loads in a more exact manner than previously possible. Introduced by Siemens AG, Postfach 103, D-8000 Munich 1, Federal Republic of Germany, this product is not marketed in the United States but is available for application in other countries. Sensitivity of the M-detector can be set over a wide range. For instance, it can be high if all vehicles, including bicycles, are to be counted or if the detector is to be imbedded beneath a very hard road surface. If loop inductance changes over a long period of time, the microprocessor adjusts the sensitivity; in addition, an error detection circuit alerts the control processor if a short circuit or loop interruption occurs.

Circle 452 on Inquiry Card

Energy Management System Available for Buildings Using Over $1000/Month Fuel

Logical and efficient control of energy systems in commercial buildings consuming fuel at a cost of more than $1000/month can be maintained at a savings with a microprocessor based system that senses and adjusts heating, ventilating, air conditioning, lighting, humidity, and machine loads. The AET 8/16 energy management system, from Atlantic Energy Technologies, Inc, 55 Lake St, Nashua, NH 03060, provides 16 variable inputs for measurement of environmental factors and 8 outputs, as well as 8 switch inputs, realtime clock, timers, and both telephone and RS-232-C communication links. The standalone controller can be interfaced to a central processing unit if desired. Included in the system are data logging and arithmetic capabilities, RAM with battery backup, and self-diagnostics.

Circle 453 on Inquiry Card

Positioning Servo Interface Links Microcomputer Bus to Feedback Device

PS-10, a single-board Multibus compatible positioning servo interface, directly connects an Intel Multibus processor to an incremental encoder position feedback device. It is compatible with any incremental position encoding system that provides phase quadrature signal outputs and can obtain simultaneous position data for multiaxis contouring motion control by slaving two or more axes. Available from Controlsmith, Inc, 17 Airport Rd, Nashua, NH 03063, the interface provides an analog voltage that is compatible with most velocity servo loops and includes an onboard 12-bit incremental up/down counter as well as inputs and logic levels for absolute zero position sampling. Signal inputs are compatible with TTL levels for maximum common mode noise rejection.

Circle 454 on Inquiry Card

A Workhorse That's A Winner . . . At 1250 LPM

Model 5321 is an off-the-shelf drum printer, already engineered for your tough jobs. Jobs that demand heavy-duty print cycles, long hours of reliable operation and consistent print quality — at high speed! This is a full-size printer for mainframe-size jobs.

Years of dependable service in countless installations have earned it a reputation as "the workhorse of the computer industry." The MDS 5321 is no slouch. It can produce human-readable or machine-readable hard copy, on a wide 160-column print line, 1-up, 2-up, 3-up or 4-up, at speeds to 1250 lines per minute*.

A variety of type fonts is readily available. Gothic style, IBM-compatible, ECMA, OCR, and CMC 7 or E13B MICR fonts — so important in financial applications where secure check imprinting is involved.

The 5321 is completely buffered. A full line of print data with its associated formatting instructions is stored in memory while the previous line is still being printed. This means maximum throughput and no missed dates for your production schedule — no overruns on your print budget!

*Using standard 48 contiguous characters. 64, 96 and 112 character sets optionally available.

Consider the outstanding features of MDS 5321:

- High-speed paper slewing to 75 ips
- Additional tractor pins to minimize tearing of form holes
- Low-inertia servo motors to considerably reduce maintenance requirements
- Quick-loading VFU mechanism designed for extended form-loop life
- Failure-proof sensing switches for No Paper or Paper Low conditions
- Advanced ribbon mechanism to assure maximum usage of entire spool
- Optional extended interface for additional status monitoring.

The 8-bit interface is already in place. The next move is yours. Whether you're in the OEM business or a systems house specializing in custom applications, it will pay you to look into the MDS 5321. Quantity discounts available. Send coupon today for a detailed Fact Sheet. Or call collect, J. Hill at (315) 866-5300 or J. Engstrom at (714) 772-0803.

MDS MOHAWK DATA SCIENCES

Mohawk Data Sciences — OEM Division
Palisade St., Herkimer, N.Y. 13350
Please send me information on the MDS Model 5321.

Name _____

Title _____

Company _____

Street _____

City _____

State _____ Zip _____

☐ I'm in a hurry. Have a representative call.
CD380

CIRCLE 68 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Automatic System Produces NC Program From Digitized Points on Drawing or Model

By simply tracing a desired tool path on a 2-dimensional drawing with a stylus attached to a digitizer, or by guiding the stylus along the outline of a model or a sample part, the operator of the Automatic Parts Programming System (APPS) can produce a numerical control program. The system reads lines/curves in a continuous flow of points and generates a minimum number of straight line and circular interpolation commands to represent the points. Alden Self-Transit Systems Corp, N/C Div, 2 Mercer Rd, Natick, MA 01760, reports that the APPS computer accepts X, Y coordinates from the digitizer, smooths the tracing, analyzes the points, and generates a smooth sequence of circular interpolations and straight-line commands that will reproduce the trace. The system is based on a Digital Equipment Corp PDP-11/03 microcomputer with dual floppy disc memory, but software rights may be bought separately for suitable existing computers.

Circle 456 on Inquiry Card

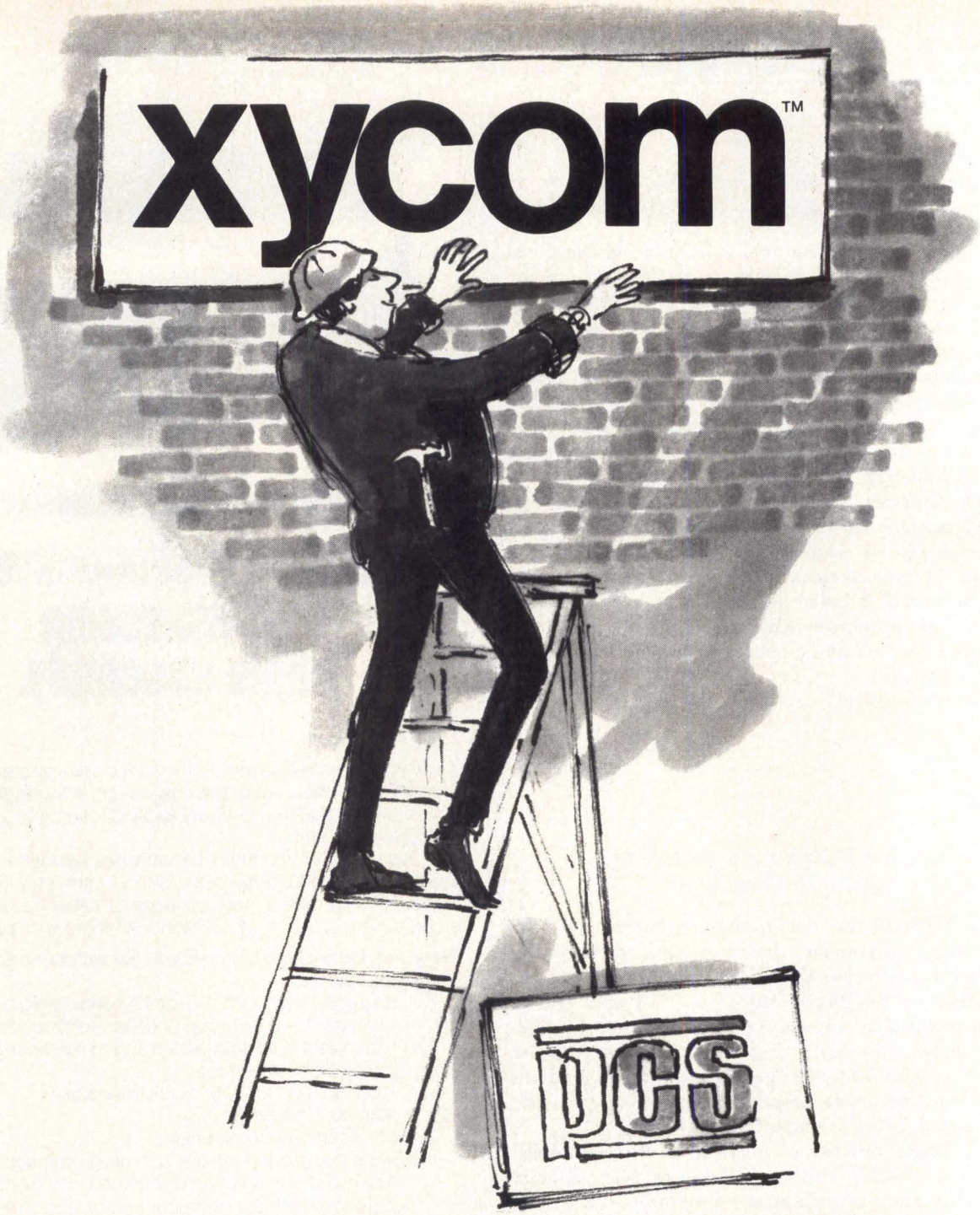
Control Programmers Maintain Up to 200 Functions

Four additions to the microprocessor based DCP 7700 digital control programmer line have been introduced by Honeywell Inc, Process Control Div, 1100 Virginia Dr, Ft Washington, PA 19034. Models 770012 and 770013 combine a variable setpoint vs time programmer with two or three controllers, respectively. Each controller functions independently to provide individual outputs, derived from the single programmed setpoint and individual process variable output signals.

Model 770022, providing two channels of programmed control, and 770033, with three channels, can configure and store as many as nine master programs with a total of up to 200 functions. Each master program includes one subprogram for each instrument channel. A function is entered as a segment in a subprogram, with all 200 functions distributed among all subprograms. Controller outputs, individually controlled either automatically or manually, may be current proportional, time proportional, time proportional duplex, and position proportional.

Inputs are set and program progress is displayed on 7-segment LED displays in engineering units. Ramp rates are programmable in 1° or 0.1° increments, or as a transition time between setpoints from 1° to 7999°. Event timing can be set from 0.1 to 999.9 hours or minutes at ±0.1% accuracy. A self-diagnostic program for all electronics and displays is stored in permanent memory.

Circle 457 on Inquiry Card



Why Did 'PCS' Become 'XYCOM'?

When you're prepared — and you know it — you can't wait to get going.

Our time has come and we're ready. We even have a new name.

Over a decade ago we started in the industrial computer field by producing industrial control systems. The problems of dust, dirt, heat, cold, vibration and atmospheric pollutants were outstanding — but so were our solutions. That was our beginning. We learned that general purpose computers wouldn't work in a hardhat environment and that we had to design, build and test differently. Solutions we take for granted today still plague manufacturers of general purpose computers that try to use them in hostile environments.

Over the past decade, our products have been used in virtually all industrial applications. As our line of modules, target and MicroHost™ computers grew, we solved more and more problems. It took over a decade of perseverance to develop the line of 'industry and environment specific' products we offer today.

Our new name, XYCOM, replaces PCS, the one we used in our 'formative' years. Our products and design integrity remain. So, call XYCOM, we're ready.

P.O. Box 984, Ann Arbor, Mich. 48106. (313) 429-4970

xycom™

The Hardhat Computer People

CIRCLE 70 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Microcomputer Package Automates Industrial Data Acquisition and Control Operations

DAS-16, made up of a 16-bit microprocessor module and several I/O modules, handles from 128 to 976 digital control points and up to 256 single-ended or 128 differential analog inputs. The system, from Technico Inc, Computer Products Group, 9051 Red Branch Rd, Columbia, MD 21045, has 16 digital to analog output ports. Each system is housed in an industrial 6- or 10-slot, 19″ (48-cm) rackmount chassis, functions with either a 3M tape cassette or up to four 8″ (20-cm) floppy disc drives, and can support as many as six RS-232-C compatible terminals, CRTs, printers, or modem interfaces. Options include front panel with alphanumeric display and hexadecimal keypad for operator input. Editor, assembler, and linking loader for assembly language, extended BASIC, and FORTRAN IV Level H are available as software packages.

Circle 458 on Inquiry Card

Programmable Controller Receives Software And Hardware Improvements

Advances for the EPTAK® microprocessor based controller system from Eagle Signal Industrial Systems, 736 Federal St, Davenport, IA 52803, include two software packages and two hardware additions. The software packages are said to provide added programming flexibility and capacity, while the hardware additions provide stable analog control.

ECL2 and ECL2/P advanced control language packages combine EPTAK control and assembly language (ECL and EAL) instructions. They are said to virtually eliminate the need to assemble and load language subroutines into the system memory separately. The base of logic instructions is common to programmable controllers. Included are 235 EAL plus 29 standard ECL instructions.

The CP750 solid state analog input module and the CP746 analog calibration card are used with the controller system's CP745 ADC module. Each input module can condition up to eight analog inputs and provide the ADC with an accurate line or output that is then converted to a directly proportional digital value. One ADC can handle up to 15 input modules under software control. The calibration card is a manually programmed constant current and voltage standard that is inserted into the controller's logic chassis to calibrate the ADC. It supplies reference and logic signals to the ADC via the controller's backplane without need for software.

Circle 459 on Inquiry Card

SOMETIMES YOU HAVE TO PAY A LITTLE MORE TO SAVE A LOT.

We know tape transports can be made cheaper; and they can be sold cheaper. A bargain, maybe, but only in the short run.

The TDI-1050 Synchronous Tape Transport is built to give the OEM and End User dependable service despite rugged, demanding environmental conditions.

That's the only way we know how to build tape drives.

We developed our electronic expertise during our years with Tandberg Data; and we've incorporated that Tandberg concern for quality in every peripheral product we design. For example, all Innovative Data Technology products pass a rigid series of quality control tests that stress the equipment far beyond any real life applications.

ANYTHING THEY CAN DO.

The 1050 Synchronous Tape Transport reads and writes ANSI, IBM and ECMA compatible ½" magnetic tape for both 7-track and 9-track NRZI and PE formats. Dual format is standard for all IDT tape drives.

Designed for reels up to 10½", the 1050 utilizes a data density of 1600 cpi PE or 800, 556, 200 cpi NRZI at speeds up to 45 ips with an average rewind speed of 200 ips.

By embedding the TDF-4050 Formatter inside the 1050 unit, saving rack space, our tape transport becomes an even more flexible unit that allows you to daisy-chain up to 4 drives.

For even greater flexibility, IDT provides an additional slot for embedding either a IEEE 488 bus controller, a RS-232C controller or a dual buffered parallel controller.

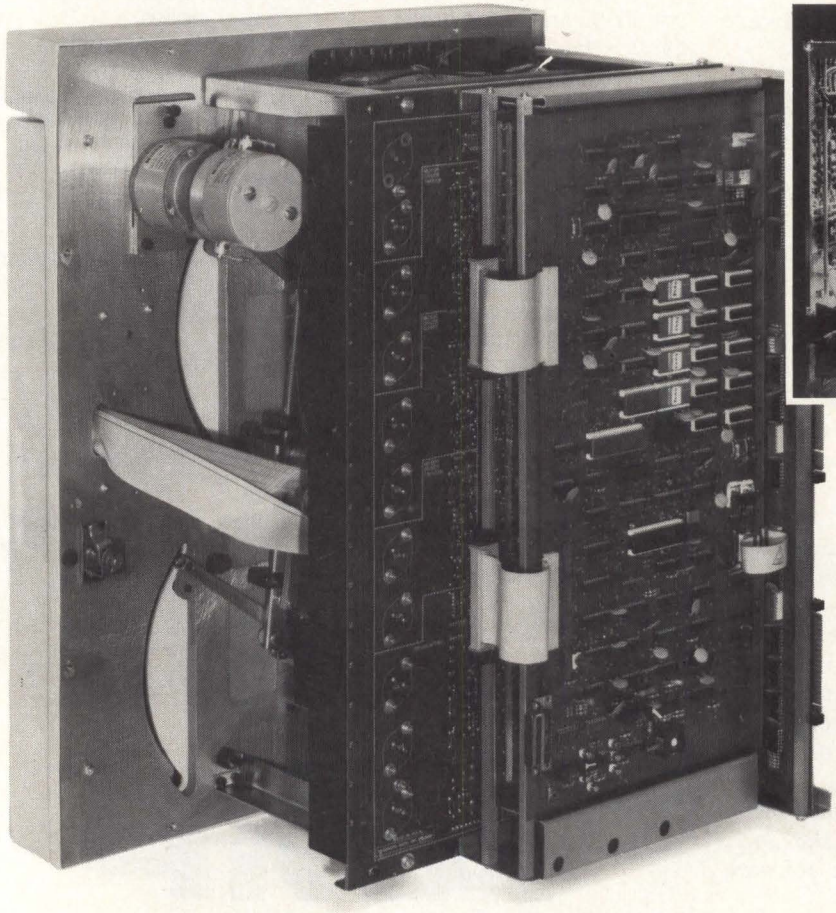
Besides being totally industry-compatible for many tape drive applications, we give you more.

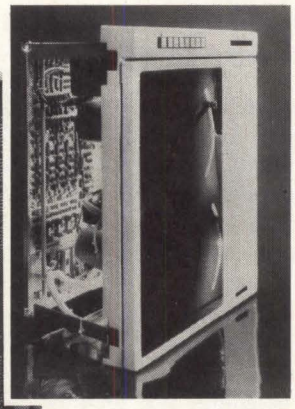
EVEN MORE FOR THE MONEY.

The 1050 has comprehensive self-diagnostic capabilities, MTBF more than 5,000 hours, a dual ceramic-blade tape cleaner and microprocessor-based control logic that gives your system the flexibility and easy maintenance that means improved performance and greater cost efficiency.

However, performance and maintainability are where the TDI-1050 and TDF-4050 really pay off.

In fact, when you pay a little more for an IDT product, you really save. In the long run.





INNOVATIVE DATA TECHNOLOGY

4060 Morena Boulevard
San Diego, CA 92117
(714) 270-3990

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Process Control Language Improves Programming Procedures

Industrial Pascal, introduced by Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176, for programming process control, allows users to maintain and extend their operating programs. It is stored in P/ROM for instant start-up without machine loading at each shift change. This eliminates the need for floppy disc units at each remote station. The block structured language also aids the program writer in developing programming habits and enables fast revisions. Featured are n-dimensional arrays, high speed floating point mathematics, integers, Boolean logic, a modified "P-code" pseudo machine, and flexible data presentations.

Circle 460 on Inquiry Card

Programming Panel Has Ladder List Options

A programming panel compatible with many RS-232-C or current loop compatible display terminals, the Deluxe P180 includes an optional ladder list feature that allows the user to obtain hardcopy listings of relay ladder programs resident in any 484 system made by Gould Inc, Modicon Div, Andover, MA 01810. Ladder listing features include the ability to list all networks resident in a 484 controller, cross referencing by type, coil to network, input to network, sequencer to network, and register to network (with contents). The panel is compatible with printers and CRTs with a minimum of 72 or 80 columns and with a T158 telephone interface for remote display terminals. It operates with choice of eight rates (selectable at the factory) from 110 to 9600 baud.

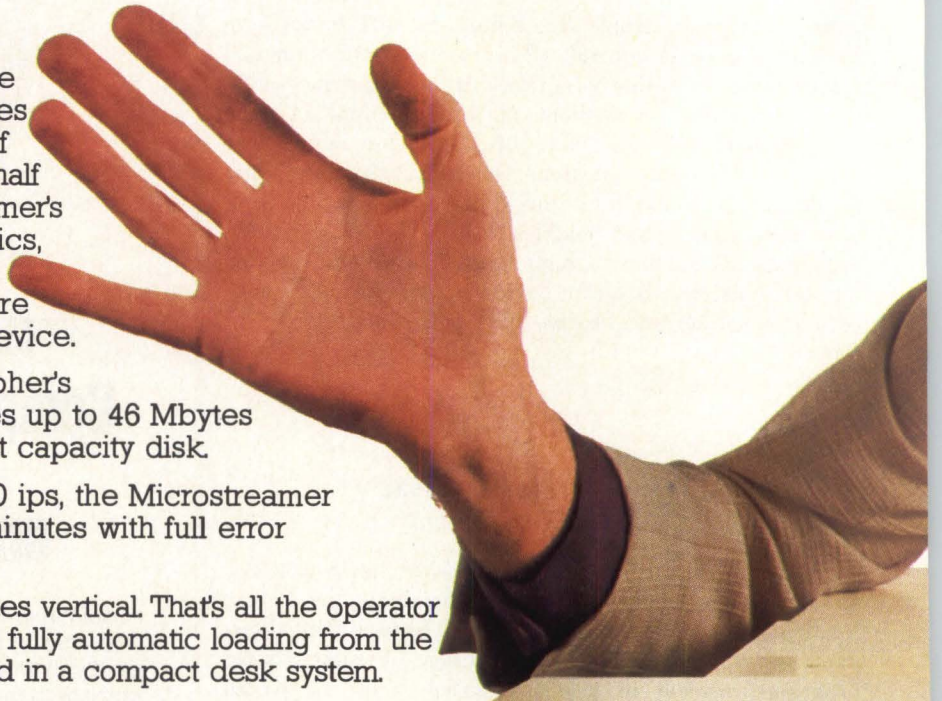
Circle 461 on Inquiry Card

Terminal Collects Factory Data For Central Computer

Automatic monitoring of production at workstations and collecting of data for periodic transmittal to a central computer are performed by a Datamonitor terminal introduced by Sierra Research Corp, Data Systems Div, 6520 Powers Ferry Rd, Atlanta, GA 30339. Terminal panels contain status indicator lights, digital display units, keyboard, operator assistance request switch, and a lock that allows only authorized persons to change the program format. Power is supplied to as many as 16 terminals through low voltage cables on the communications lines.

Circle 462 on Inquiry Card □

Introducing Microstreamer.™ The 100% solution to disk backup.



The Low Cost Solution! The Microstreamer™ Tape Drive provides the unique disk backup benefits of ½ inch tape for a cost of less than half of a standard tape drive. Microstreamer's price includes formatting electronics, power supply, chassis – even UL and CSA approval. There is no more economical tape based backup device.

The Capacity Solution! Cipher's Microstreamer Tape Drive provides up to 46 Mbytes of data to backup even the largest capacity disk.

The Speed Solution! At 100 ips, the Microstreamer transfers 46 Mbytes of data in 4.8 minutes with full error correction. No waiting.

The Size Solution! 8¾ inches vertical. That's all the operator sees, since Microstreamer provides fully automatic loading from the front and is designed to be mounted in a compact desk system.

The Compatibility Solution! The phase encoded Microstreamer is ANSI and IBM compatible using standard 10½, 8½ or 7 inch reels so the user gets worldwide interchange and access to common database.

The Reliability Solution! Spec'd at 1 in 10^{10} hard errors, the Microstreamer provides reliability approaching that of the Winchester disk – absolutely essential for effective backup.

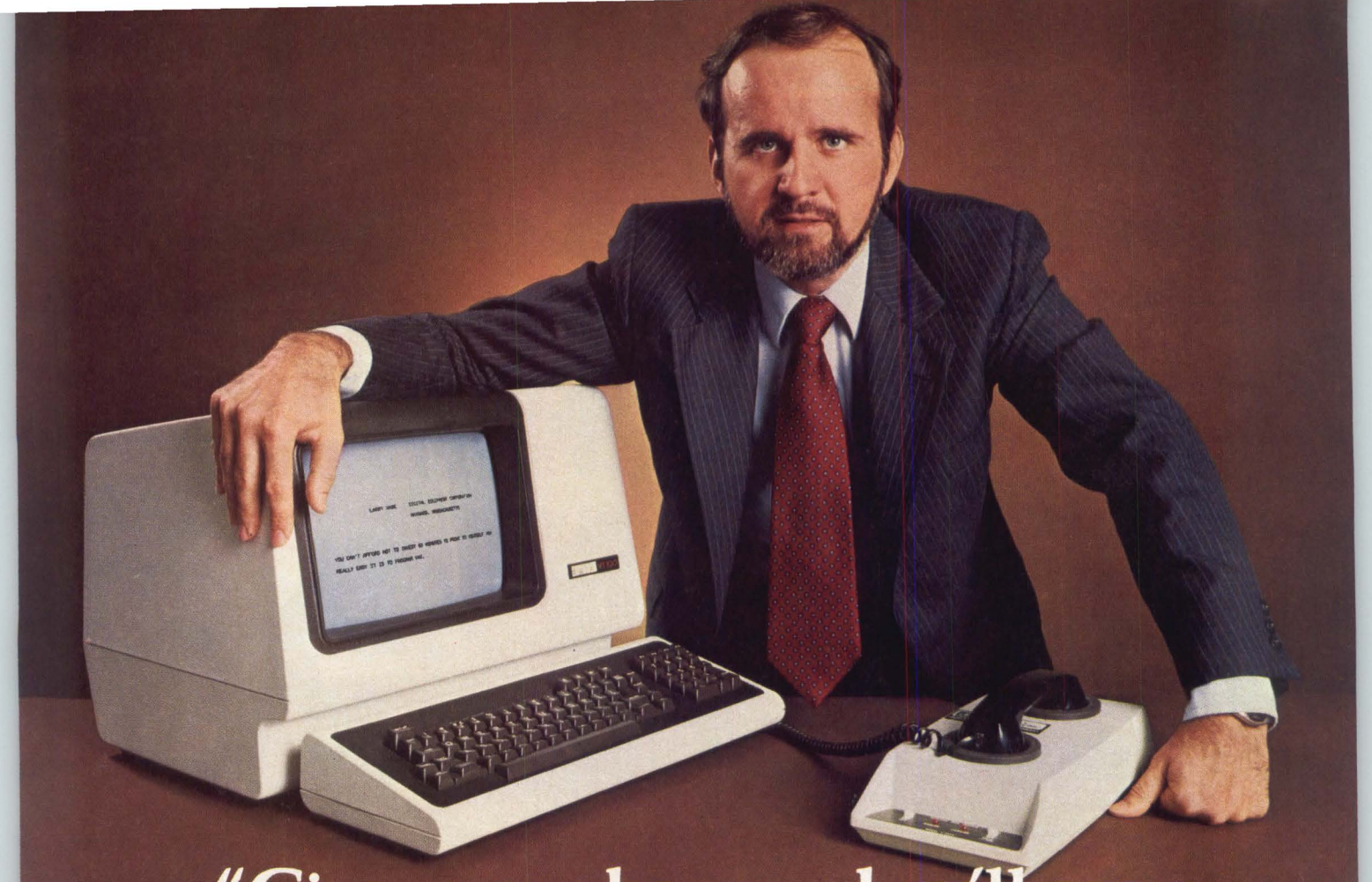
The Tape Drive Solution! The exciting Cipher Microstreamer also functions as a 25 ips tape drive for traditional applications and operates in a daisy chain of up to eight streamers and/or standard tape drives.

Don't settle for less than the 100% solution. Orders for the Microstreamer are being taken now. Call Cipher Data Products, Inc., 5630 Kearny Mesa Road, San Diego, California 92111. (714) 279-6550.

cipher data products, inc.

CIRCLE 74 ON INQUIRY CARD


Now, that's excitement!
Cipher



"Give us one hour and we'll prove you can program a VAX faster than any other 32-bit OEM computer."

Larry Wade, Marketing Manager, Technical OEM Group, Digital Equipment Corporation.

We want to prove to you the programming power of the VAX-11/780, and what it can do for your development time.

So if you have a terminal with an acoustic coupler, we'll give you a demonstration right in your own office. Then you be the judge.

"Four good reasons you should dial up a VAX."

1. You start with more software. VAX gives you more software than any other 32-bit minicomputer, so there's less system development work for you to do.

The VAX/VMS operating system is composed of a number of functional layers around a highly efficient real-time executive. This means you can either interface at the I/O level, or you can use our highly versatile file management system to set up sequential, random or multi-key ISAM file structures.

And VAX/VMS gives you unequalled networking and communications capabilities, with other Digital systems and with competitive mainframes.

2. You have to work with our programming tools to believe them. With VAX/VMS, all your programming, editing and debugging take place right at the terminal, whether you're programming interactive or batch applications. Our symbolic debugger even lets you interactively monitor and control your programs and variables—using the *same* symbolic names and data formats you created in the source program.

And if you need help at any stage of your work, simply type HELP. The Digital Command Language will help you solve your problem with clear, English-like statements.

And you can choose from five languages: FORTRAN IV-PLUS, COBOL, PASCAL, BLISS, or MACRO. Plus PDP-11 BASIC-.

PLUS 2 and FORTRAN in compatibility mode. That's more than any other 32-bit minicomputer system offers you.

With tools like these to work with, your gains in programming efficiency can be enormous.

What's more, VAX/VMS is just a simple step up for PDP-11 users. In fact, VAX/VMS runs RSX-11M programs and development tools.

"VAX/VMS gives you a total of seven languages to choose from—more than any competitive system on the market."

3. VAX is a new level of system integration. While other software systems were designed around existing hardware, Digital's software and hardware engineers worked together on VAX from the very beginning. The result is the most efficient virtual memory system on the market.

The VAX/VMS operating system gives you a virtual memory capacity of four gigabytes. And a main memory capacity that can go clear up to eight million bytes.

So you can write your programs without worrying about complex overlays, or spending time fighting with a limited memory space. Because each process can be up to 32 million bytes long—largest capacity in the minicomputer industry today. VAX/VMS automatically handles the memory mapping, providing high-performance techniques such as "page pooling" and "page clustering." In addition, many of our innovative paging algorithms are built right into the firmware for maximum execution speeds.

"With a virtual memory capacity of four gigabytes, VAX/VMS can handle your longest programs."

4. VAX/VMS gives you complete control over system resources. You can lock part or all of a program into main memory for the highest possible performance. You can also set priorities on 32 different levels—the first 16 for real-time so you can strictly separate real-time applications from others. You can even control user privileges to the point where it's practically impossible for a low-level user to interfere with people doing high-level work.

All these management tools are incredibly easy to work with, so you can spend your time planning and implementing instead of struggling with the system.

And if you have a lot of programs to convert, you'll be surprised how easy VAX/VMS makes that, too.

"Now about that offer..."

We think it's well worth 60 minutes of your time to discover what VAX can do for your development work. If you agree, just send the coupon to me, Larry Wade, at the address below.

Is one hour enough time to prove everything we've said here? Frankly, I doubt it. But it should be plenty of time for you to prove to yourself that VAX software is way ahead of the competition.

And that's exactly where it can put you.

Digital Equipment Corporation,
Technical OEM Group, 129 Parker St.
(PK3/M-86), Maynard, MA 01754.

If your business involves programming computers for technical applications and offering them for resale, we'll show you how VAX software can save you money by saving you development time.

Just check the appropriate box(es):

☐ I'm interested. Tell me how I can dial into VAX's programming power.
☐ Please send me more information on VAX/VMS.
☐ Have a sales representative call.

Name_____

Title_____

Company_____

Address_____

City_____

State_____ Zip_____

Telephone_____

0-3-0

digital

CIRCLE 75 ON INQUIRY CARD

John L. Simonds
General Chairman

Ifay F. Chang
Program Chairman

Society for Information Display

April 28—May 2
Town and Country Hotel, San Diego, California

The 17 sessions of this year's Society for Information Display Seminar and Symposium will explore the forefront of electronic display technology with the advent of the 1980s. Symposia, which will run from Tuesday afternoon, April 29, through Thursday, May 1, will cover topics including CRTs, flat panel and avionic displays, image processing, and display graphics.

Welcoming remarks by General Chairman John L. Simonds and Program Chairman Ifay F. Chang will formally open the conference on Tuesday morning. Opening ceremonies will also include the presentation of the 1979 Symposium Best Paper Awards. Following the awards, R. M. Harden, Special Assistant for Information Management to the President of the U.S., will present the keynote address. In his address, Mr Harden will provide a progress report on the Executive Office of the President and its Demonstrative Information Display System. Preceding the opening, SID president T. Du Puis will conduct the annual SID business meeting.

To augment the scheduled symposium topics, the conference will feature several invited addresses. Most of these are included within the coverage on the relevant session. One, however, entitled "Encounter with the Almost Star: Voyager Examines the Jovian System," will be presented at the Wednesday, April 30 lunch, when J. L. Mitchell of the JPL Photoscience group will discuss how the Voyager images of Jupiter may help determine the differences between stellar and planetary formation. Following in the space vein, a visit to the Reuben H. Fleet Space Center in Balboa Park, San Diego, Calif, is scheduled as a special event. Blast off will be at 5:30 pm, Wednesday, April 30.

To round out the spectrum of information display technology coverage, the program will include ten tutorial seminars, three evening panel sessions, and blocks of time scheduled for authors' interviews. Slated for 5:15 to 6:15 pm on Tuesday and Wednesday, and 5 to 6 pm on Thursday, the author interviews will be informal sessions where attendees may talk with and query the authors. Evening panel discussions are scheduled for Tuesday, April 29 at 8 pm. The one to one and one-half hour seminars are scheduled for the days before and after the conference, Monday, April 28 and Friday, May 2, with five on the agenda for each day. Selected symposia sessions, evening panels, and seminars of interest to *Computer Design* readers are profiled.

ROLM'S 1602B: An Army Standard Computer Designed for Full Integrated Logistics Support

IT'S A COMPLETE PROCESSOR IN A SINGLE 20″ CHASSIS.

The 1602B (AN/UYK-19) has space for 7 I/O modules, control panel interface, CPU and 64K of directly addressable memory. An additional 15 I/O slots can be made available with ROLM's 2150 Expansion Chassis.

IT HAS SINGLE SIDED ACCESS.

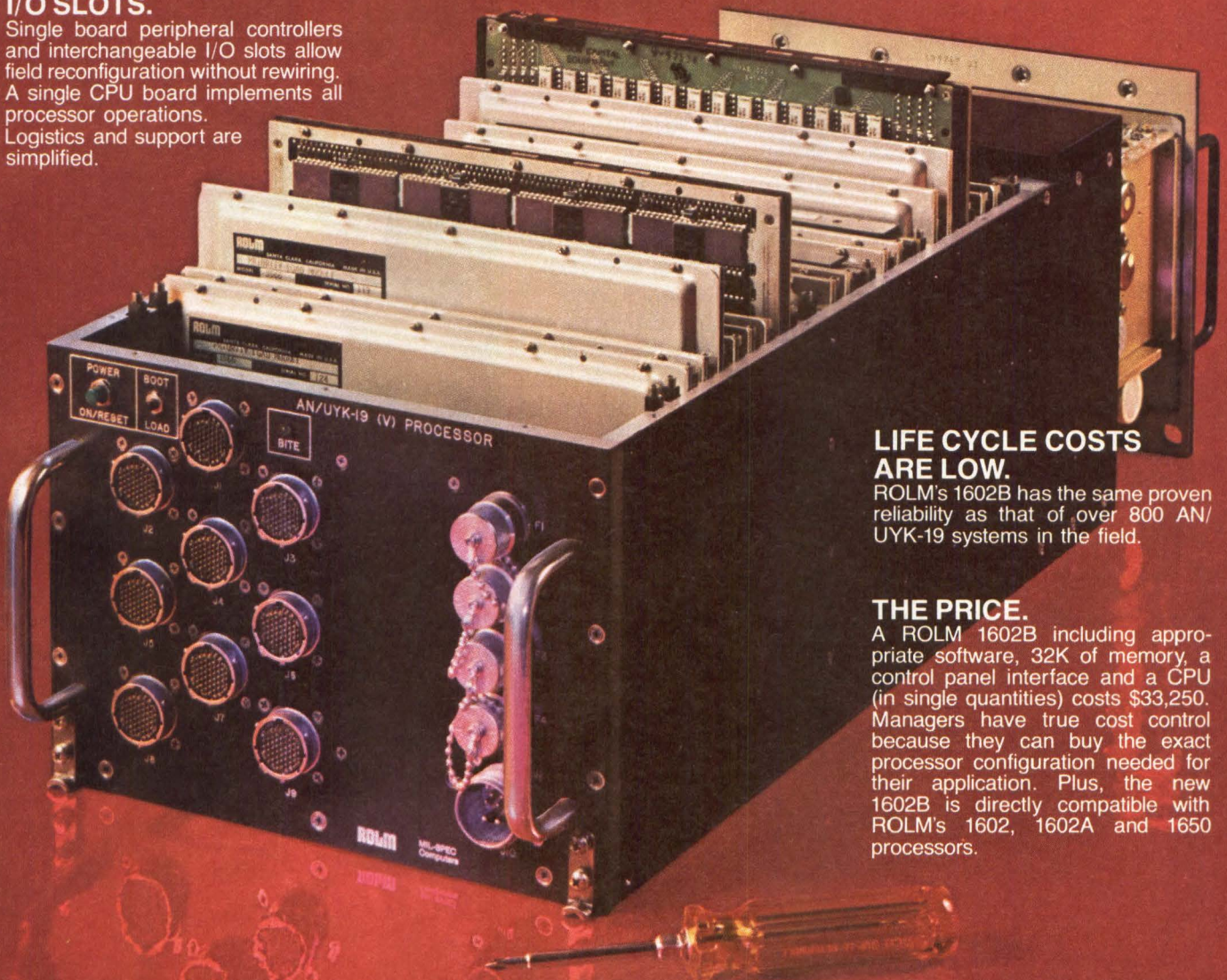
Maintenance is simplified by quick, easy access to the interior of the conductively cooled chassis. The 1602B also has a new plug-in AC or optional DC power supply.

EXCELLENT DELIVERY WITH FULL SUPPORT.

Since AN/UYK-19 processors are in continuous production, delivery is no problem. They are fully mil-qualified and backed up by complete training and documentation. And ROLM's extensive software has really impressed program managers. They find that our total support program can't be matched.

INDEPENDENT CARDS & INTERCHANGEABLE I/O SLOTS.

Single board peripheral controllers and interchangeable I/O slots allow field reconfiguration without rewiring. A single CPU board implements all processor operations. Logistics and support are simplified.



LIFE CYCLE COSTS ARE LOW.

ROLM's 1602B has the same proven reliability as that of over 800 AN/UYK-19 systems in the field.

THE PRICE.

A ROLM 1602B including appropriate software, 32K of memory, a control panel interface and a CPU (in single quantities) costs $33,250. Managers have true cost control because they can buy the exact processor configuration needed for their application. Plus, the new 1602B is directly compatible with ROLM's 1602, 1602A and 1650 processors.

That's Why We're #1 in Mil-Spec Computer Systems

ROLM MIL-SPEC Computers

4900 Old Ironsides Drive, Santa Clara, CA 95050. (408) 988-2900. TWX 910-338-7350.

In Europe: Muehlstrasse 19 D-6450, Hanau, Germany, 06181 15011, TWX 4-184-170.

CIRCLE 76 ON INQUIRY CARD

The world's best floppy disk controller. Plain.

Now there are two ways to get the simplicity, power and flexibility of our floppy disk controller: NEC's μPD765 chip, or the BP-2190 board from NEC Microcomputers.

The innovative μPD765, developed and introduced by NEC, has become an industry standard and will soon be second-sourced by a U.S. semiconductor company. It's simple to build into your system, because the standard 40-pin, +5V design is totally compatible with IBM single- or double-density format floppies and 5¼" mini-floppies, as well as standard 8" drives.

It's powerful too, executing 15 complex commands including many subroutines usually found in a disk handler software package. Plus it controls up to four double-sided drives.

And the 765 gives you unequalled flexibility in programming your controller system through such commands as Multi-Sector Reads and/or Writes, Track Formatting, and Multiple Drive Seeks. It operates in either DMA or interrupt-driven mode, and interfaces to all popular microprocessors, including our μPD8080AF, μPD8085A and μPD780 (Z80™).

For board applications, you get all the capabilities above and more. The BP-2190 board includes the 765 and 16K of dual-ported RAM (expandable on-board to 48K), along with priority and refresh logic. Disk-to-RAM transfers are under DMA control

Controller Chip REPS: Action Unlimited, Arlington, TX, Spring, TX; Cerco, San Diego, CA; Contact Sales, Inc., Burlington, MA; D/Z Associates, Inc., Denver, CO; Electronic Innovators, Inc., Minneapolis, MN; Eltron, Phoenix, AZ; HLM Assoc., Torrington, CT, Northport, NY, Parsippany, NJ; Imtech, Inc., Cleveland, OH, Dayton, OH; K-Mar Enginerering & Sales, Inc., Grandview, MO; Kaytronics Limited, Ville St. Pierre, QUEBEC, Concord, ONTARIO, Surrey, BRITISH COLUMBIA; L & M Associates, Pikesville, MD, Montpelier, VA; Harry Nash Associates, Willow Grove, PA; R.C. Nordstrom & Company, Lathrup Village, MI; Perrott Associates, Inc., Fort Lauderdale, FL, Clearwater, FL, Orlando, FL; Santana Sales, Costa Mesa, CA; Stone Component Sales, Waltham, MA; Technology Sales, Inc., Palatine, IL; Trident Associates, Inc., Sunnyvale, CA; Tri-Tronix, Albuquerque, NM; Tri-Tronix, NW., Mercer Island, WA; 20th Century Marketing, Inc., Huntsville, AL, Knoxville, TN; Wolff's Sales Service Company, Raleigh, NC.

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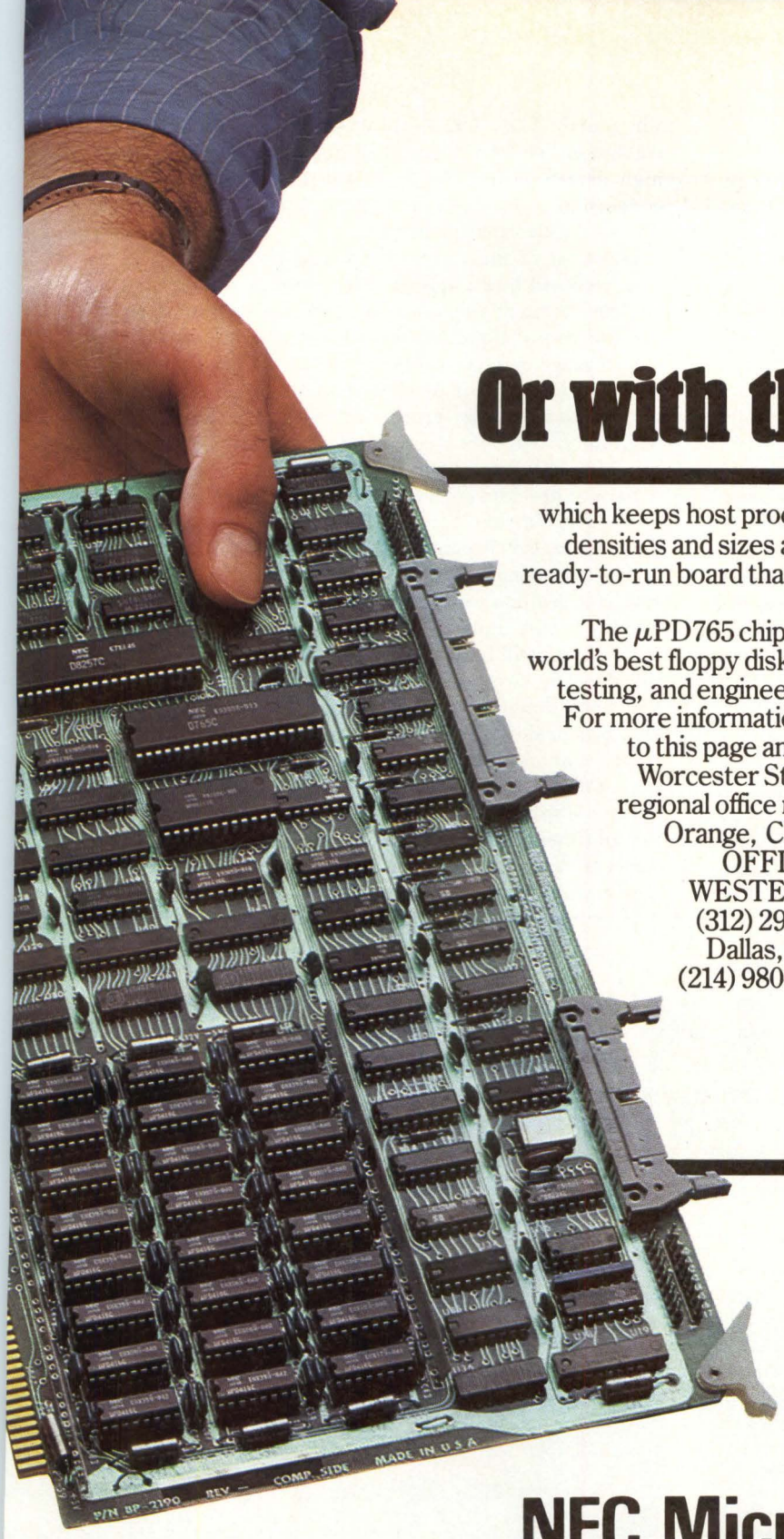

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CD 4

Symposia

Feature of the *Flat Panel Displays* session will be an invited paper on recent flat panel display developments in Japan. Technological activity areas that will be cited include liquid crystal, electroluminescent, LED, vacuum fluorescent, and plasma displays. Configurations and performance highlights of ladder mesh and slalom electron guides for flat CRT displays will be presented, as will a large area cathodoluminescent flat panel TV display system that uses electron beam guides.

The electronics, displays, control units, and realtime software for Advanced Integrated Display System, a generic system for all Navy CTOL/VTOL aircraft display and control requirements, will be detailed in two of the *Avionic Displays* presentations. A lightweight, wide field of view, helmet-mounted display system will also be covered. This system presents pilotage and navigation nighttime imaging as well as daytime symbology to attack helicopter pilots. Also offered will be an airborne electronic terrain map system that generates, via computer, a terrain map display of forward-looking perspective or planimetric data.

Thin film electroluminescent panels have emerged from research and development to practical applications in alphanumeric, graphic, and TV displays. *Electroluminescent Devices* will discuss the use of developing technologies in several applications. One use disclosed will be a matchbox size (25 x 38-mm) TV display system that uses thin film electroluminescent panels with hybrid drivers that are attached to and folded behind the display surface. The display area will contain 512 x 680 elements with a 500-line/in (200/cm) resolution. To be presented in another paper will be the high density evaporated bridge method that allows interconnection of the 500-line/in electroluminescent display to the hybrid electronic substrate.

Foremost of the *Image Processing* developments to be discussed will be an approach for realtime spatial filtering and correction of video images. In the same session, an image processing algorithm that provides halftoning for electronic image systems where I/O devices do not have consistent pixel spacing will be advanced. Also cited will be an interdisciplinary image processing research and application laboratory that produces dynamic vector displays and generates color static and dynamic images.

Several developments in the field of *Passive Displays* will be reported in one session. Performance and life testing data on sealed 7-segment digit displays that have been fabricated using either anodically grown or reactively-sputtered iridium oxide electrochromic display and counter electrodes with aqueous electrolytes will be discussed. Two other papers will focus on electrochromic displays. The first will describe electrochromic materials for data display applications, detailing the design, construction, and operation of a practical 4096-pixel display. The second will present response and lifetime improvements using oblique evaporation of the WO_3 layer. Also to be reported is progress in the encapsulation of the magnetic particles and fabrication of the addressing matrix and memory for magnetic particle displays. A dye-foil digital display whose performance and temperature rival LCDs will close this session.

Graphics data optimization techniques that are implemented at the post-processor level for immediately usable results will be discussed in the first of the *Display Graphics* papers. Another paper will report on a compact, 3-dimensional graphics generator developed for dot matrix devices. This device is comprised of a 2-dimensional graphics curve generator combined with a preprocessor to perform 3-dimensional transformations and curve projection. Also to be considered will be an algorithm, and its hardware implementation, for ultra-fast generation of analytical curves. The algorithm is based on solving differential equations in a binary logical way.

Two papers will cover *DC Plasma Display Technology.* A self-scan panel that is a complex cell sheet using a thin glow spacer and a grooved face plate will be described. The other plasma display to be presented is a dc pulsed multicolor display that has memory, uses a tetrode structure, and combines a primary channel, drift space, and display layer. Also to be discussed in this session will be three photoluminescent phosphors that have been developed for the three primary colors of a gas discharge panel display. The phosphors, $(Y,Gd)BO_3:Eu^{3+}$—red, $BaAl_{12}O_{19}:Mn$—green, and $BaMgAl_{14}O_{23}:EU^{2+}$—blue, possess radient efficiency and required characteristics to reproduce color TV pictures.

Heading the session on *CRTs* will be a report on color picture tube design trends. The transition from delta-gun orientation with dot screens to inline guns and line screens will be described, along with a projection of future developments. Another paper will compare the critical performances of state of the art penetration phosphor, high resolution shadow mask, and high performance monochromatic CRTs. Brightness, resolution, and contrast capabilities of these CRTs will be quantitatively compared. A filter phosphor composed of a combination phosphor core and a specific pigment will be the subject of another paper. Tubes with this filter phosphor can be operated at high ambient light levels without degradation of picture quality.

Three of the *Liquid Crystal Display* papers will discuss dichroic LCDs. The first will present transmission spectra, reflectance, contrast ratio as a function of incidence angle and temperature, contrast/reflectance tradeoff, and response time data for a dichroic dye, cholosteric LCD without polarizers. The second will detail a bright color, negative or positive display that uses dichroic dye doped (guest-host) nematic liquid crystals. This LCD exhibits good color contrast at low voltage. The third will cover a 6 x 4" (15 x 10-cm) dichroic liquid display with integral touch entry that displays a positive or negative image or outline via phase control of excitation applied to special electrode patterns. Also presented in this session will be a double-layer electrode LCD—two isolated electrode layers on the same glass substrate—and a 70 x 150-line, 36-line/in (14/cm) ZnO varistor controlled LCD.

An invited paper on computer output printing technologies will lead off the *Hardcopy/Printers* session. It will review the major technologies for computer output printing in the 1980s, discussing both impact and nonimpact technologies including band, laser/electro-

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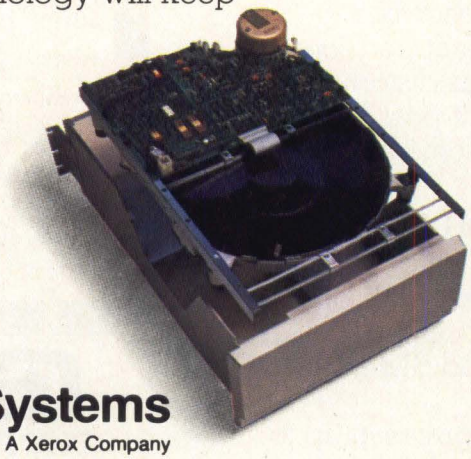

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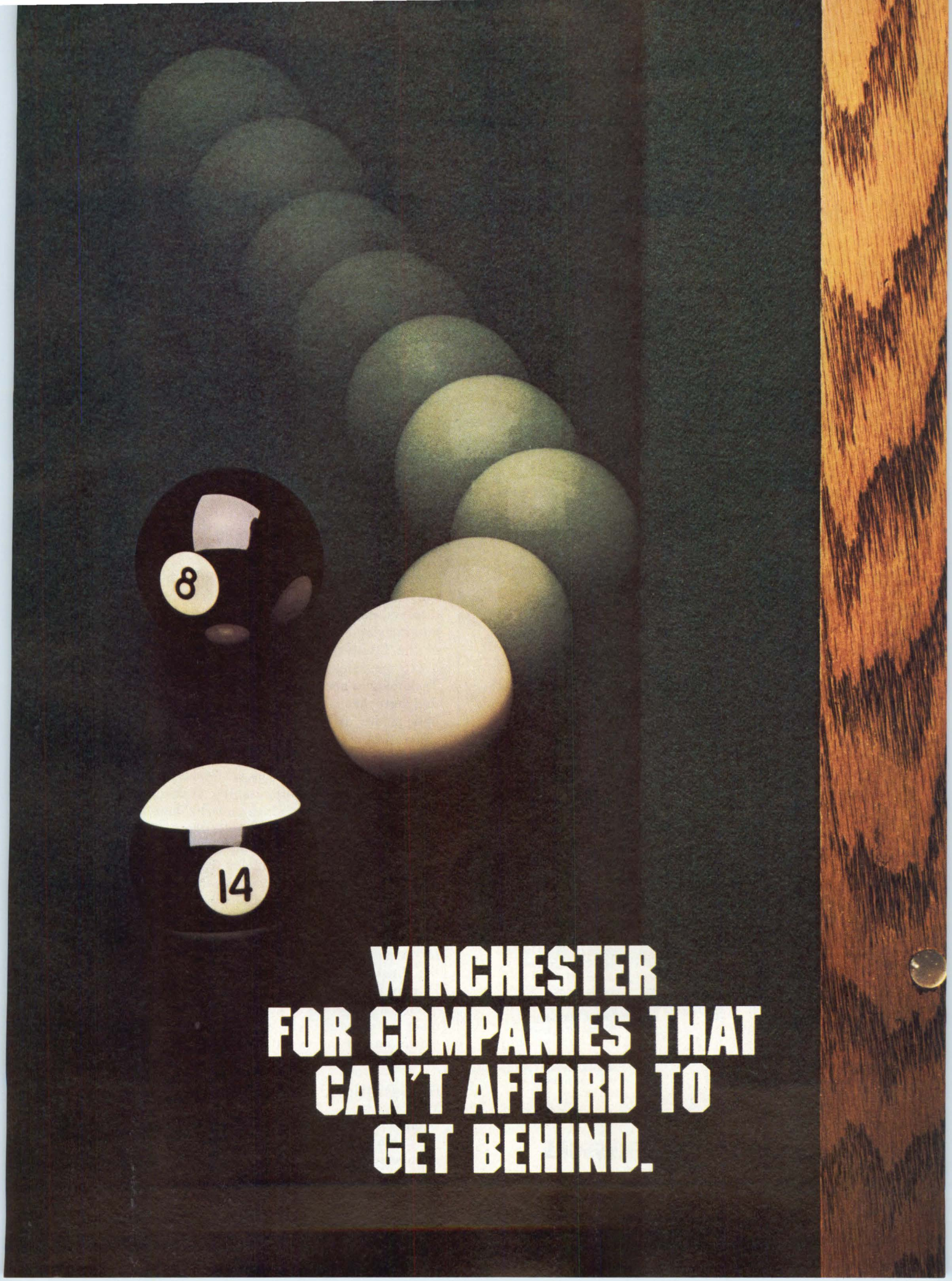
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photographic, and ink jet. A second invited paper will report on hardcopy technologies in Western Europe. Two printer designs will be advanced in this session. The first will describe a 15,000-line/min laser printer that uses the electrophotographic process; the second will detail a synchronous jet ink droplet mechanism that generates droplets by piezoelectric stimulation.

Evening Panel Discussions

"Display Technologies in Computer Graphics" will address the major role that display developments play in the expanding field of computer generated graphics. Discussed will be the trends in graphics systems, the impact of various CRT architectures including raster versus calligraphic and refreshed versus storage, distribution of intelligence and storage, and the value of color in graphic presentations.

During the past 25 years, considerable effort has been applied to the advancement of "Flat Panel Displays." Early publicity spoke of a thin TV picture on the wall. That goal has not yet been reached. But flat panel technology has come into its own in calculators, watches, terminals, and test equipment. Despite these recent accomplishments, investors and supporters in industry and government are, more than ever, questioning whether the investments will offer rewards, an appraisal that will be made by the panelists.

Seminars

Monday's seminars, which are profiled here, will highlight the various technologies being developed as flat panel displays. As many of the display technologies have limited multiplexing capability, the first seminar will offer a review of the "Active Matrix Addressing Techniques" used to overcome this problem. "Liquid Crystal Display Technologies and Characteristics" will describe prototypes that have been built using various liquid crystal electro-optic modes, drive schemes in direct matrix addressing, and active matrix concepts. A comparison of prototypes will allow the status of LCD flat panels to be evaluated. The seminar on "Electroluminescent Display Technologies and Characteristics" will discuss the characteristics of electroluminescent devices which underlie their advantages and disadvantages in various applications. "Electrochromic Display Technologies and Characteristics" will review recent developments in WO_3 devices that have lead to improved stability and reduced response times. The preparation and properties of iridium-oxide based devices, and new developments in organic and reversible electrodeposition will also be presented. The electrophoretic display is noted for its pleasing image quality and low power operation; in the final Monday afternoon session, "Electrophoretic Display Technologies and Characteristics," its optical and electrical properties as governed by choice of material and mode of operation will be discussed. Direct and assisted matrix addressing techniques for the displays will also be compared.

Registration

Symposium registration fees are $50 for members and $65 for nonmembers in advance, and $60/75 for members/nonmembers at the conference. Registration is $70 to attend one day of seminars and $110 for both days. For more information contact Lewis Winner, 301 Almeria Ave, PO Box 343788, Coral Gables, FL 33134. Tel: 305/446-8193.

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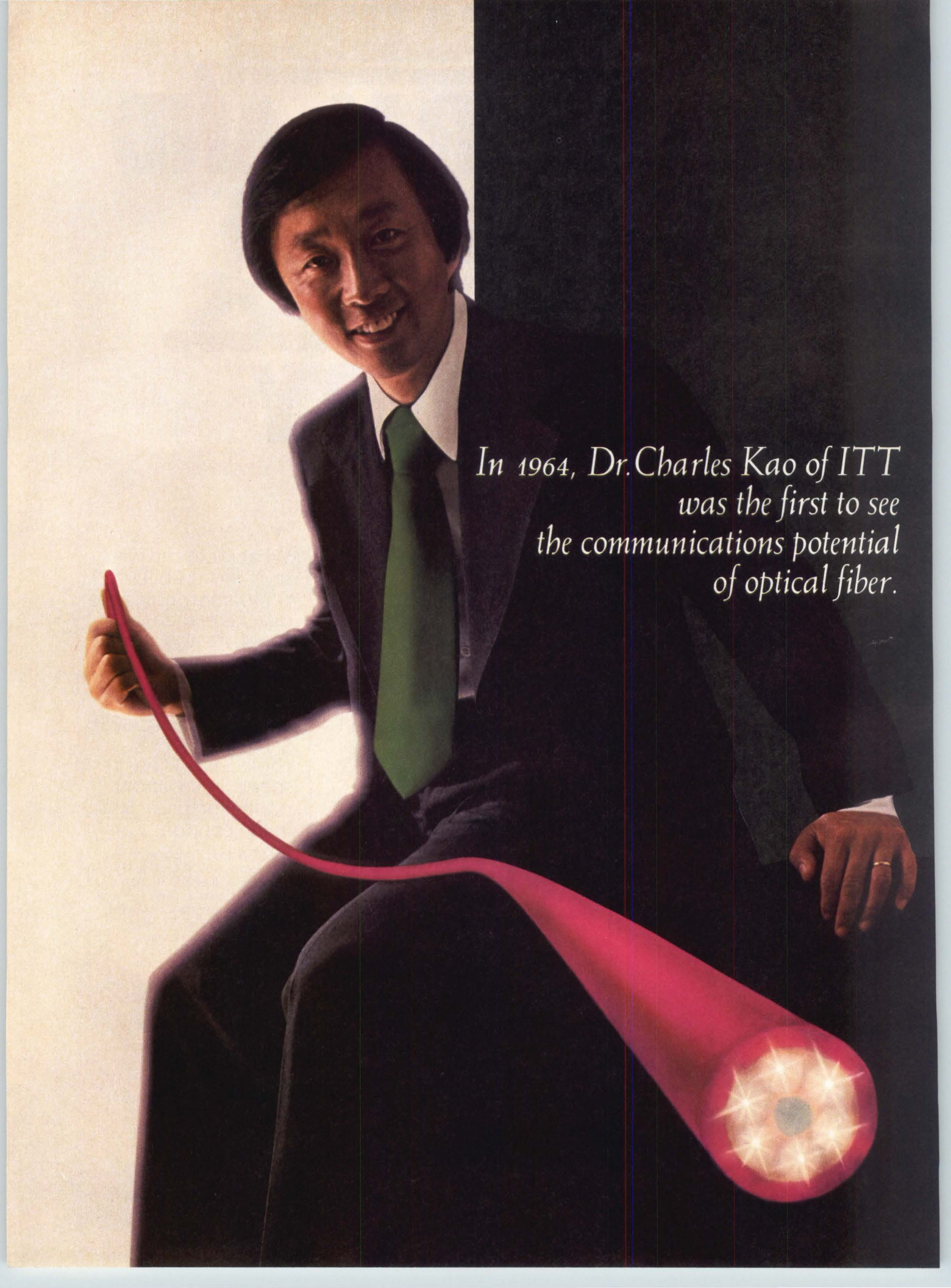
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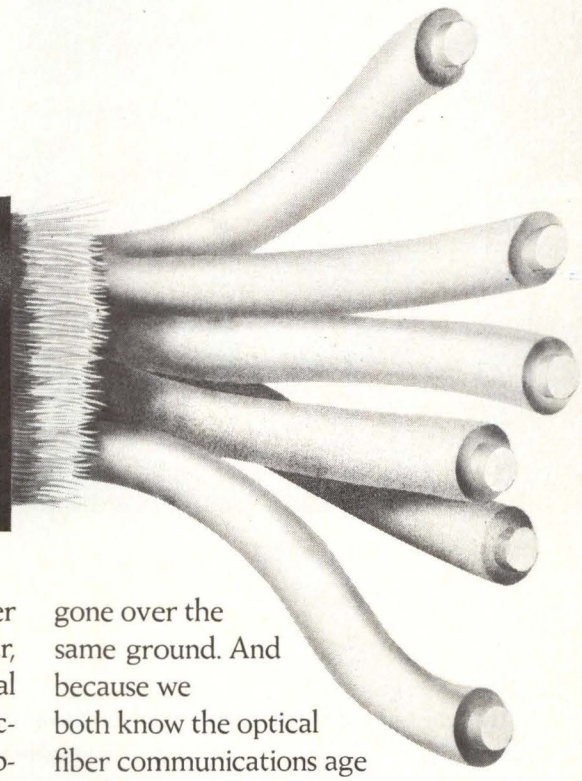

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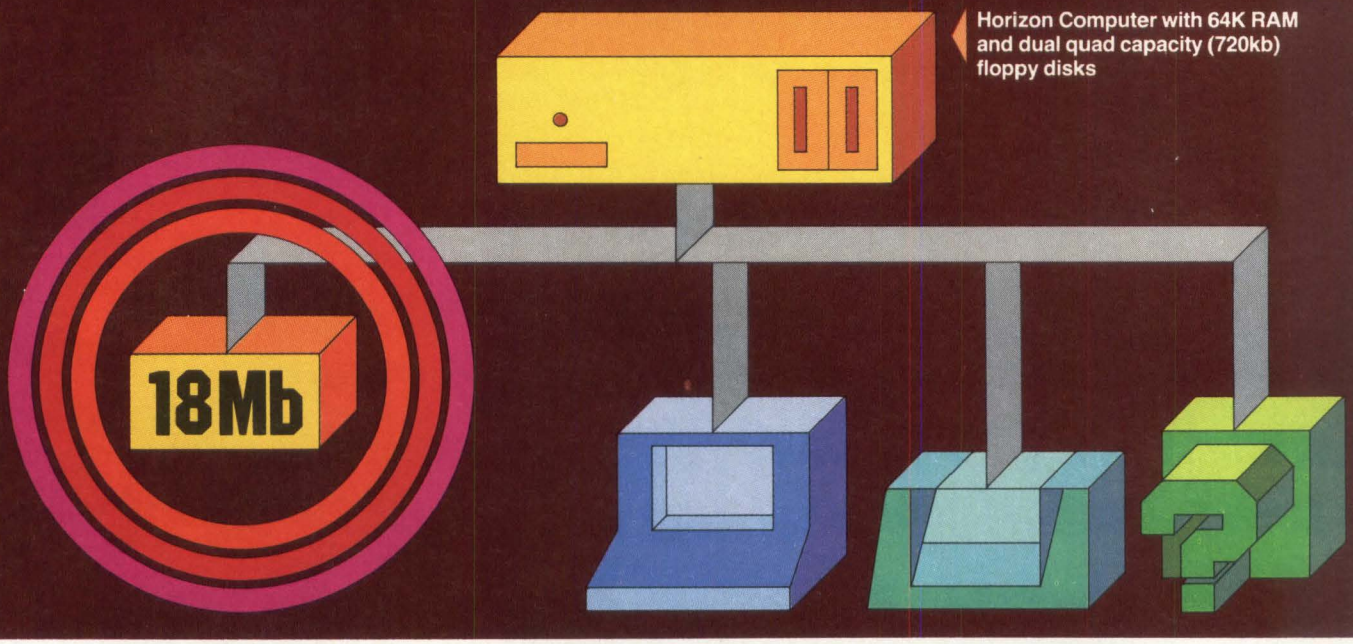

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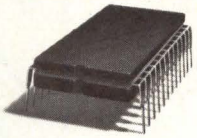

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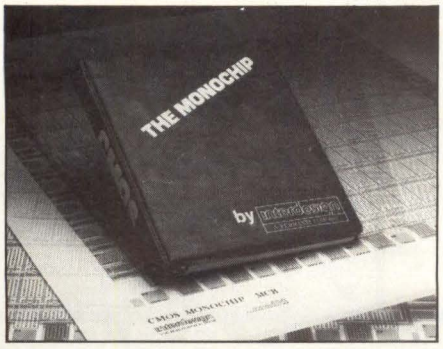

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8039	✓		✓		✓		✓		✓		✓	
8039-6	✓		✓		✓		✓		✓		✓	
8035	✓		✓		✓		✓		✓		✓	
8021	✓		✓		✓		✓		✓		✓	
8048	✓		✓		✓		✓		✓		✓	
6802	✓		✓		✓		✓		✓		✓	
6800	✓		✓		✓		✓		✓		✓	
F8	✓		✓		✓		✓		✓		✓	
3870	✓		✓		✓		✓		✓		✓	
3872	✓		✓		✓		✓		✓		✓	
Z80A	✓		✓		✓		✓		✓		✓	
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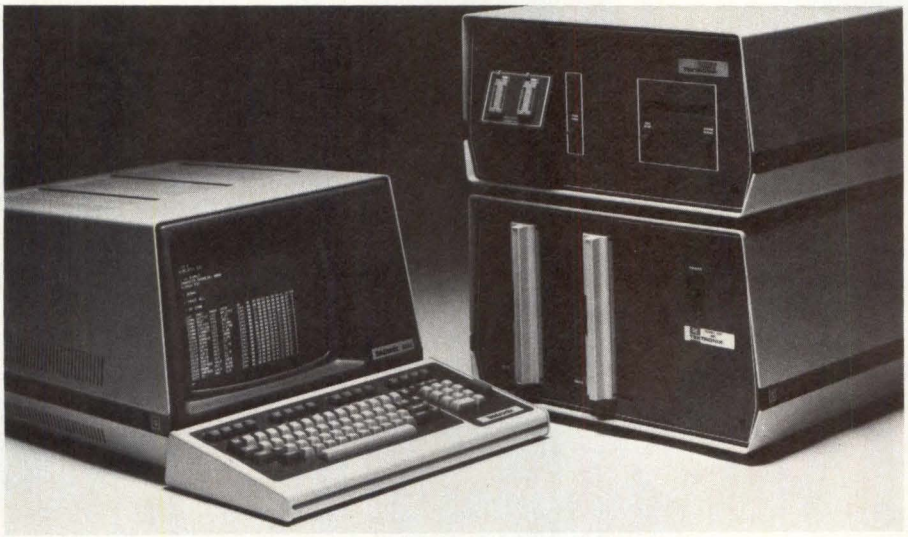

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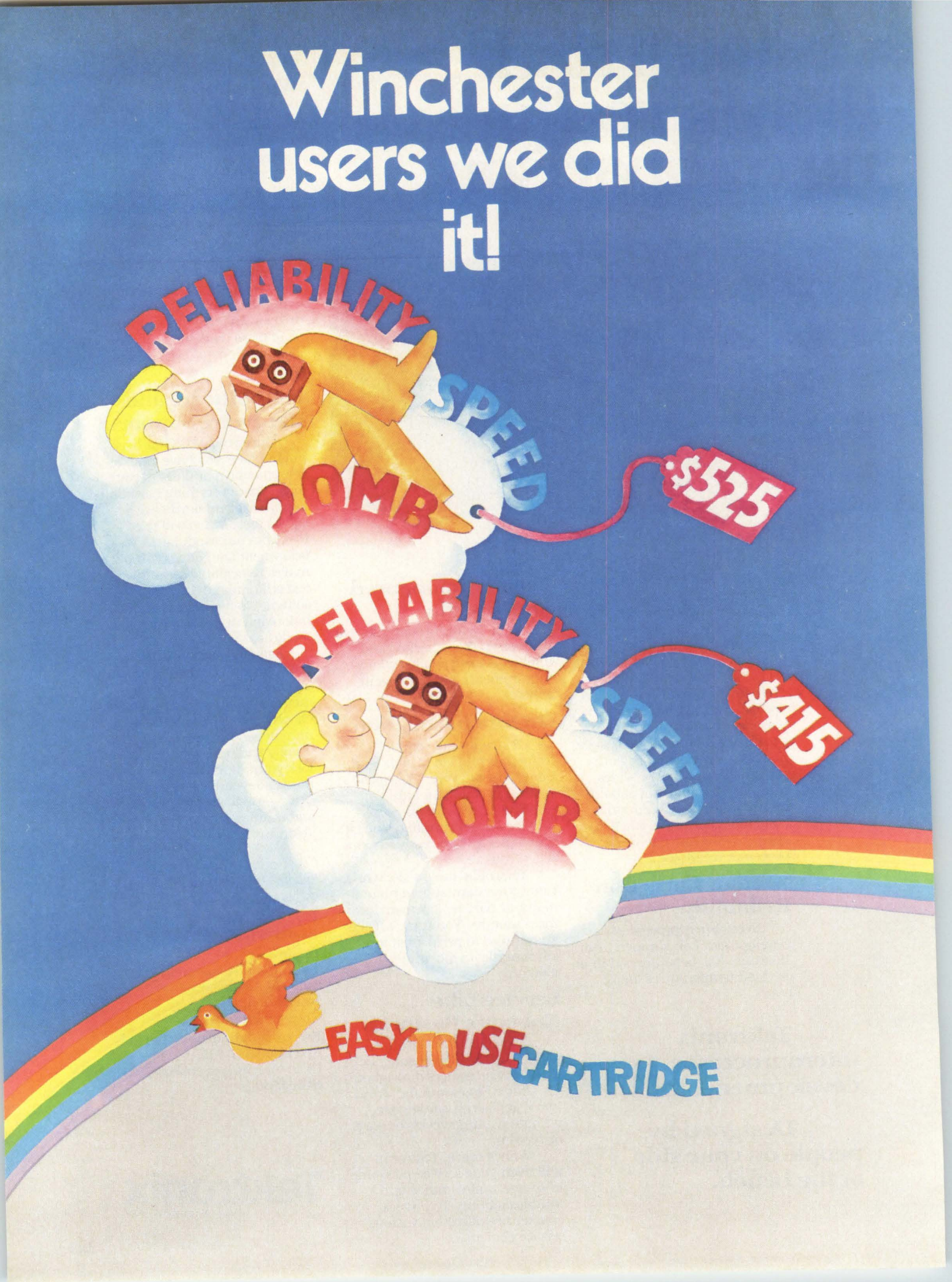

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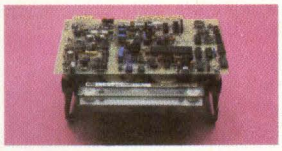

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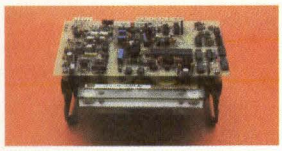

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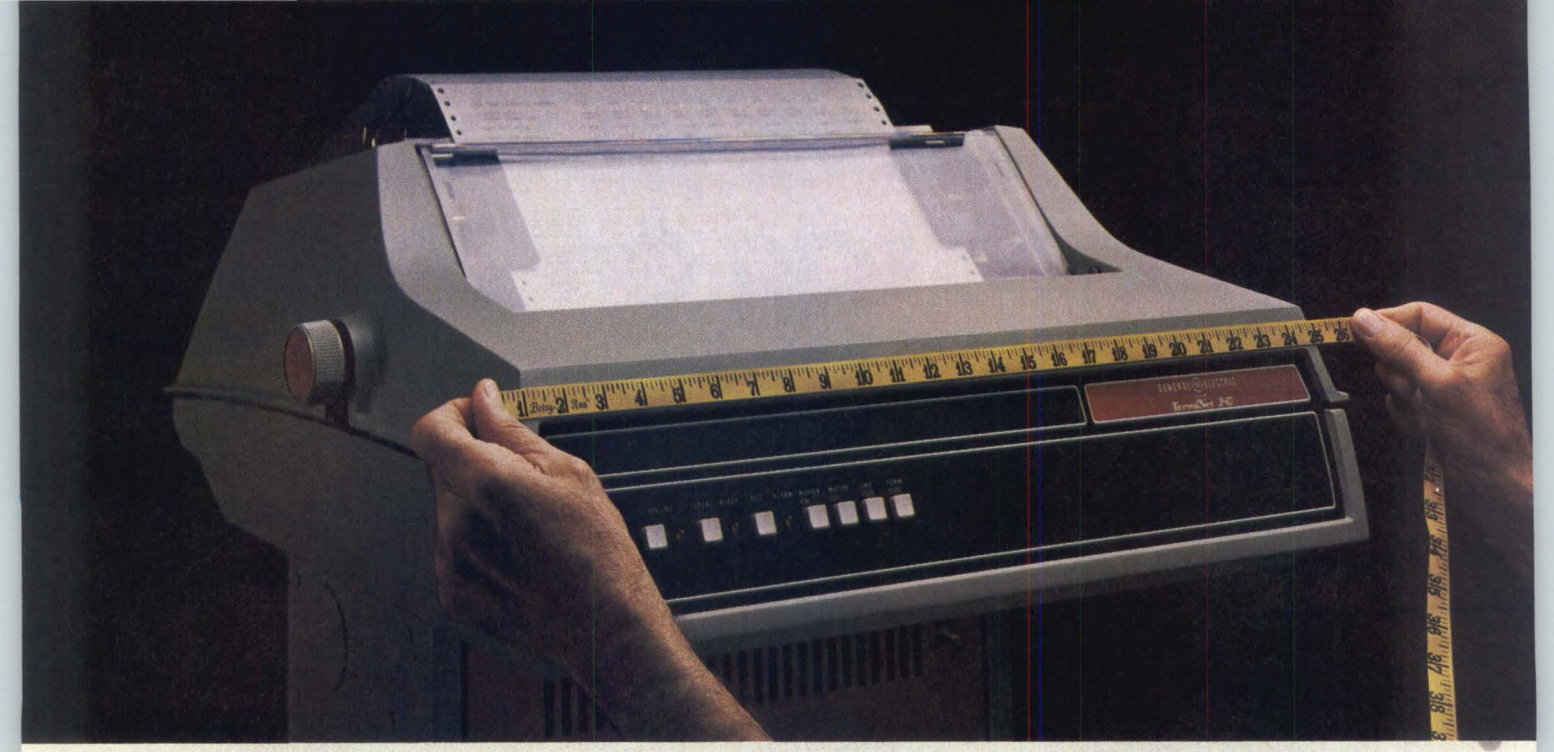

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MULTIPROCESSING IMPROVES THROUGHPUT AND RESPONSE IN A VECTOR TO RASTER CONVERTER

Loosely coupled, faster microprocessors supplant bit slice or lower level hardware technology and related microprogramming in a vector to raster converter design to achieve fast response and high throughput

James A. Mello Naval Underwater Systems Center, Newport, Rhode Island
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It is often necessary to generate hard copies of displays viewed on some type of cathode ray tube console. When cathode ray tubes with raster driven deflection systems are used, the task of obtaining a hard copy is fairly straightforward because the printer or plotter is also, typically, a raster driven device. There is little or no data conversion processing needed under these circumstances, and any processing that might be required before the cathode ray tube input display can be sent to the plotter is easily accomplished in either hardware or software. Although other types of plotters are available, only raster driven plotters will be considered.

If the cathode ray tube (CRT) has a random position deflection system, the task of obtaining a hard copy becomes significantly more complex, because vector data are used to drive this type of deflection system. In this case, a vector to raster conversion routine must disassemble each vector into discrete points before the display data can be sent to the plotter. Current designs dictate use of bit slice architectures to meet the high processing bandwidth requirements of this task. In addition to a longer and more hardware-intensive development effort, there remains the difficult proposition of maintaining the microcode.

The first approach examined the Texas Instruments 16-bit 9900 microprocessor and found that even in assembly language this machine was too slow and too limited in addressing range to accomplish the conversion in what was considered to be a reasonable amount of time. A second attempt to attain the high throughput required of the vector to raster converter used a distributed, multiple bus, multiple microprocessor system incorporating relatively powerful single-board microcomputers. A further goal was to use a high level language

DISPLAY WORD TYPE - 4-BIT CODE	DISPLAY WORD ARGUMENTS				
BASE POSITION	INTENSITY - 2 BITS	X-COORDINATE 10 BITS	PICTURE AREA 2 BITS	Y-COORDINATE 10 BITS	
CHARACTER	INTENSITY - 2 BITS	SIZE 1 BIT	CHARACTER 1 8 BITS	CHARACTER 2 8 BITS	CHARACTER 3 8 BITS
SYMBOL	INTENSITY - 2 BITS	SIZE 1 BIT	SYMBOL MODIFIERS 12 BITS	SYMBOL CODE 8 BITS	
LINE	INTENSITY - 2 BITS	RANGE DATA 10 BITS	OCTANT CODE 3 BITS	SLOPE DATA 10 BITS	
END WORD	NOT USED				

Fig 1 Simplified diagram of display control words. Combination of these control words is used to generate picture on CRT. Same display buffer which drives CRT also serves as input to raster converter. Each word is four bytes long and typical picture in this CRT format occupies about 6k bytes

for the overall program structure and to drop down to assembler code for the inner loops only.

A brief description of the CRT display console illustrates the magnitude of the storage requirements during vector to raster conversion. The 13″ (33-cm) high by 10″ (25-cm) wide CRT has a resolution of approximately 102 pixels/in (40/cm), which translates to a picture of 1382 CRT lines, with each line consisting of 1056 pixels. Four intensity levels are provided by this display; therefore, two bits of coded data represent the intensity of each pixel. Total number of CRT pixels is 1,459,392. Doubling this number and dividing by 8 yields 364,848 bytes required to hold the bit map of an entire display if the intensities are saved in coded form.

Fig 1 shows the control words used to generate the display. It is clear that these words are not in raster form and must be processed before being supplied to a raster driven plotter. The maximum total time allowed to produce a hard copy of the CRT screen on a Versatec model 1200A electrostatic plotter is 30 s in this application. Intensities can be simulated with this plotter by letting a 4-nib dot matrix represent a single CRT pixel (Fig 2). For this to be feasible, the plotter must have at least twice the resolution of the CRT it is copying. This restriction applies only to plotter width, of course, since the length of the copy may vary. The model 1200A plotter offers a total of 2112 nibs/plotter line, exactly twice the number of pixels per line of the input CRT.

The plotter generates approximately 110 CRT lines/s. Therefore, a display consisting of 1382 CRT lines would take nearly 13 s to plot, leaving 17 s to complete vector to raster conversion.

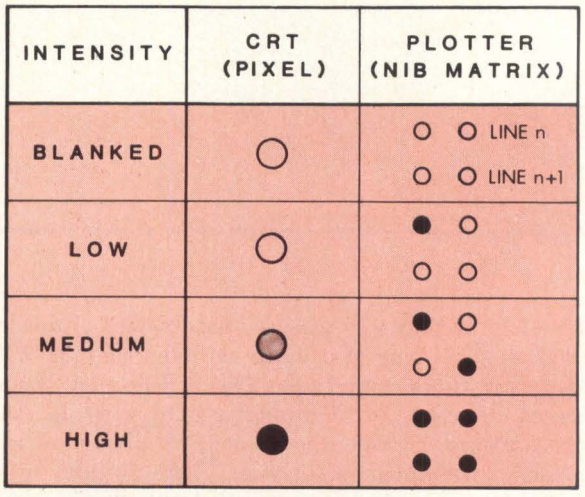

Fig 2 CRT to plotter intensity mapping. Simulating intensity on hardcopy device requires that single CRT pixel be represented by multiple points on hard copy. Plotters with high resolution will give effect of plotting intensity by appropriately filling correct number of plotter nibs being used to represent single CRT pixel

Conversion Example Based On 9900

Efficiency of a microprocessor based vector to raster converter depends, to a large extent, on the efficiency of system software. In this instance, the system software must process an input display buffer consisting of vector words. To evaluate the potential performance of this system effectively, only the conversion software need be considered. Although additional support hardware and software are needed, such as plotter hardware and software interfacing, the execution of conversion software accounts for most of the hardcopy process overhead.

Development systems, such as the Tektronix 8002 Microprocessor Lab and the Intel MDS-230, make it possible to evaluate potential application software without constructing a prototype of the target system. Besides assisting in software development, these systems can usually monitor and time the execution of application programs to give an idea of program efficiency. The 8002 system was used to develop and evaluate a conversion software routine written in 9900 assembly language.

The heart of any vector to raster conversion routine is the algorithm used to generate the individual points on a given vector. The algorithm chosen for implementation on the 9900 driven vector to raster converter is based on the equation of a line, $Y = mX + b$. This algorithm requires a floating point or fixed point scaling division routine to determine the points on lines with nonzero, finite slopes.

A second major design consideration in any vector to raster converter is its memory organization. The 9900 microprocessor has a direct addressing range of 65,536 bytes, significantly less than the 364,848 bytes required to contain a bit map of an entire display. Since system operating speed is critical, any overhead such as memory paging must be avoided. An alternative to expanding system memory is to reduce system memory requirements by processing the display in slices. This software approach makes a complete pass over the input display buffer to generate the raster for each display slice, owing to the randomness of vectors that comprise the input display buffer. A sorting routine could be implemented to sort the input display buffer so that the raster data for a particular slice would be generated by processing a corresponding section of the sorted buffer. However, the software and hardware overhead involved in the sorting process makes this approach unattractive.

Regardless of whether a sorted or unsorted input display buffer is processed, a memory organization based on a single output buffer dictates that the buffer be sent to the plotter before each succeeding pass. This forces the vector to raster conversion process into a wait state until the output buffer is ready to be filled again. If a dual output buffer is implemented and direct memory access (DMA) capabilities are included in the system design, concurrent processing and plotting are possible. Optimizing system software by limiting the unnecessary, repetitive processing performed during each pass, and implementing a DMA process to allow concurrent plotting and processing could yield a vector to raster converter with reasonable operating speed.

The multipass system was chosen for the 9900 microprocessor conversion software. The 8002 development system was used to edit, debug, perform, and time the execution of the application program. A general version of the multipass system was implemented to allow timing of various system configurations. The algorithm was verified by plotting the actual raster output on a model 1200A plotter. This was not performed in real time, but rather by transporting the raster via magnetic tape to a Digital Equipment Corp PDP-11/70 minicomputer which drove the plotter.

The Table shows timing results obtained for various output buffer sizes on the TI 9900 microprocessor and illustrates the tradeoff between memory size and number of passes required. Software divide times were measured on the Tektronix development system, while the hardware divide measurements were calculated assuming an Advanced Micro Devices AM-9511 arithmetic processor

Raster Conversion Process—Timing Breakdown*

Output Buffer Size (Bytes)	No of CRT Lines Passes/Processed Per Pass	With Software Divide		With Hardware Divide		Total† Logical Processing Time (s)	Logical† Processing Time/Pass (s)
		Total Processing Time (s)	Processing Time Per Pass (s)	Total Processing Time (s)	Processing Time Per Pass (s)		
11,056	33/42	145.2	4.4	78.58	2.38	73.52	2.23
45,606	8/173	103.2	12.91	39.18	4.90	34.32	4.29
91,212	4/346	96	23.98	32.70	8.17	27.89	6.97
182,424	2/691	92.4	46.3	29.23	14.61	24.43	12.22
364,848	1/1382	91.2	91.2	28.05	28.05	23.25	23.25

*Does not include I/O, intensity decoding, or buffer initialization
†Logical processing time equals total processing time minus divide processing time.

was implemented. Addressing restrictions were ignored. With this hardware configuration, the greatest decrease in processing time per pass came when going from a single-pass to a 2-pass system. Timings that included software fractional divides were much too slow for the required system. The faster times, which assumed implementation of the AM-9511 arithmetic chip, were much more reasonable, but still too slow.

These results indicate that it is at least feasible to perform the vector to raster conversions in software on a 16-bit microprocessor. Since system operating speed is still below the required level, several changes in the system design are needed. Initially, the algorithm upon which the conversion routine is based must be reconsidered. A delta scheme, which steps up or down through memory, is one possible alternative approach. If the delta factor—the tangent of the line segment—is known or easily determined, then the process is trivial. As Fig 1 shows, the tangent is given in line display control words, and the stroke generators for the character and symbol words could be configured to contain this type of information.

A second area of concern is how much memory beyond the 64k-byte direct addressing range of the 9900 microprocessor must be accessed. System operating speed could be increased by using a microprocessor whose direct addressing range is sufficient to handle this particular task. Intel's 8086 is one candidate, since it is capable of addressing 1M bytes directly.

Changing the CPU and the algorithm upon which the conversion routine is based dictates development of new software. Although the vector to raster conversion routine for the 9900 microprocessor was written in assembly language, the knowledge gained by implementing the first example system suggests the possible use of a high level language. Any required code optimization could then be achieved by coding inner loops of the program in assembly language. The savings in software development time when using a high level language lend credence to this approach. Intel's iSBC 86/12 microcomputer board will be the system module in the enhanced vector to raster converter. Another configuration uses two 86/12 boards for multiprocessing, with one of the boards used as an intelligent DMA controller. PLM/86, Intel's high level language for the 8086, is a candidate language for developing application software.

iSBC 86/12 Based Vector To Raster Converter Example

An iSBC 86/12 system may have a number of bus masters. The vector to raster converter incorporates two bus masters, although one of the processors acts as a slave to the other. When more than one master simultaneously requests control of the Intel Multibus, bus arbitration must occur. A bus clock, usually supplied by one of the bus masters, provides a timing reference for resolving contention among multiple requests from bus masters. This feature allows different speed masters to share resources on the same bus. Actual data transfer over the bus proceeds at a speed that depends only on the transmitting and receiving devices. Investigation of the vector to raster converter will implement the 86/12 in lieu of the 9900 microprocessor.

Fig 3 shows the target system, as well as the development system used to prepare the software and integrate that software with the hardware. Two 86/12 boards are used in this vector to raster converter. The "conversion processor" 86/12 is the system master. It is responsible for directing the operation of the second microcomputer. This second 86/12 is implemented as an input/output (I/O) processor (IOP). As a bus master, the IOP can perform DMA transfers as well as process data being transferred. Six 64k-byte random access memory (RAM) boards meet the large memory requirement of the system. Including the 32k bytes of onboard RAM, the total system memory is now 548k bytes, more than sufficient for I/O buffers, program memory, and scratch memory.

Fig 3 also shows the plotter connected to the auxiliary connector, instead of a serial or parallel I/O port, because the plotter will be hardwired so that the IOP sees it as a 64k memory space segment. Data, therefore, can be transferred to the plotter across the local IOP data bus without having to access the Multibus. Required drivers and interfacing hardware reside on a separate prototype board.

The MDS-230 development system in Fig 3 has an 800-bit/in (315/cm) tape drive tied to its bus, in addition to a flexible disc drive and a printer. Either Intel's ICE-86 in-circuit emulator or Intel's iSBC-957 INTELLEC-86/12 interface package can be used to downline load problems into the 86/12 onboard RAM and to control 86/12 execution. While the in-circuit emulator has the advantage of being able to partition memory gradually between the development system and the target system, the interface package works adequately in its absence.

Although the 86/12 appears well suited to multiprocessing applications, there are no development tools presently available for controlling multiprocessor operation during software and hardware integration. Currently, only one central processing unit (CPU) at a time can be controlled by either the ICE-86 or the iSBC-957; therefore, software must be written to commence program execution in the second processor. This software might be controlled by a reset switch. Software in the operational program could then monitor execution of software on the slave microprocessor.

Use of a high level language, PLM-86, introduces a second area of concern. The PLM-86 compiler does not allow programs to change data pointer values dynamically beyond a 64k segment. Linking to a procedure written in assembly language must be accomplished to access more than one data segment of memory dynamically. The physical addresses associated with these data segments must be calculated by a CRT to memory mapping algorithm, which effectively maps each CRT pixel to a memory location without losing the integrity of the picture.

Design Considerations With the 8086

When working with more than one 64k-byte segment of memory, it is important to understand how the 8086 formulates its 20-bit physical address. All accessible

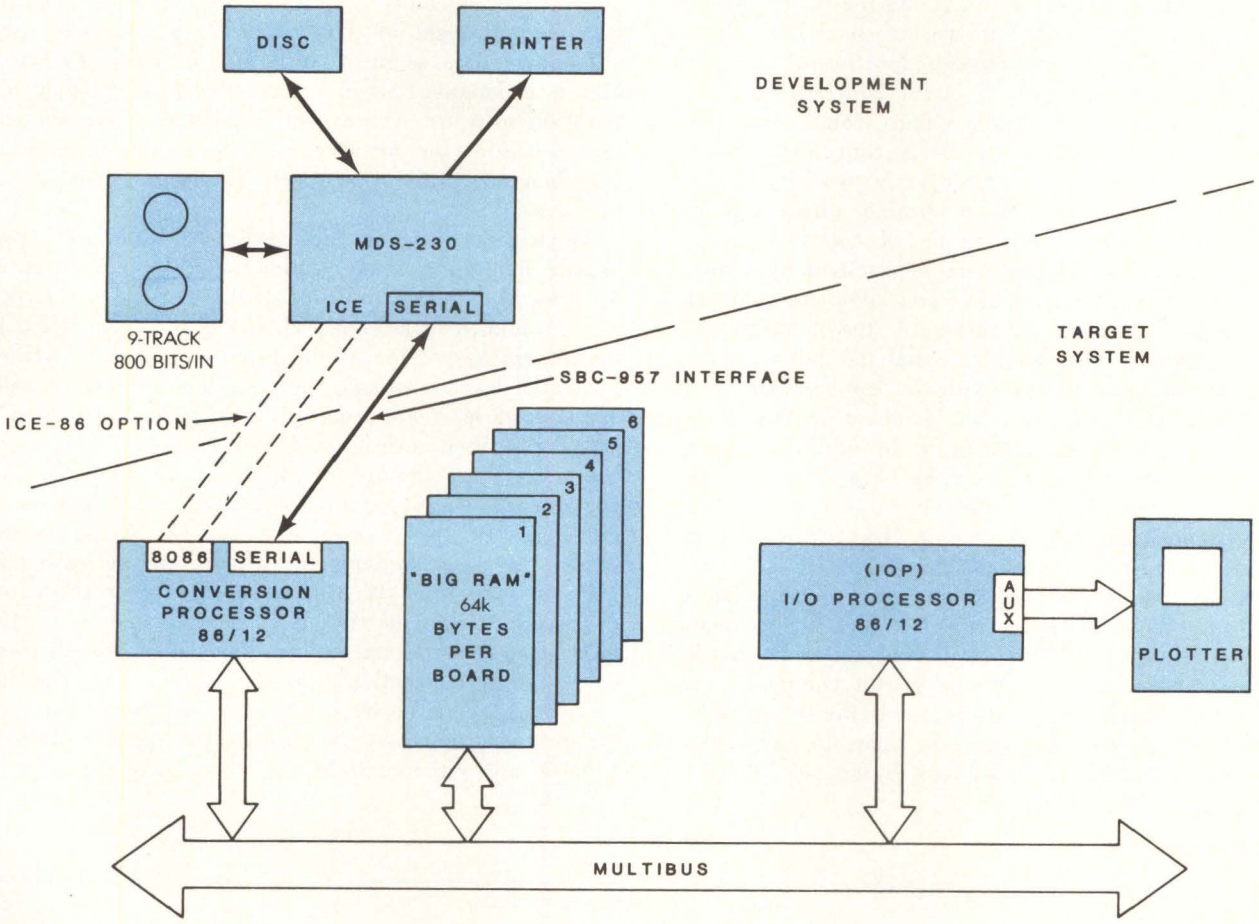

Fig 3 Development and target system block diagram. Application software development and software/hardware integration can be significantly facilitated by using microprocessor development system. Debugging aids such as ICE (in-circuit emulator) can prove to be invaluable when trying to isolate software or hardware problem

registers in the 8086, including segment registers, are 16 bits wide. The 8086 hardware, however, shifts the contents of the appropriate segment register four bits to the left before adding any offset. This is performed in an internal, 20-bit register whose output is the effective physical address. The offset added to the shifted segment address is a 16-bit value. It can address every location within a given segment. Physical address wraparound because of an offset carryout is a distinct possibility that must be considered.

One major vector to raster converter design problem is how information displayed on the CRT should be mapped into memory. The given vector data, together with knowledge of the present CRT beam position, supplies sufficient information to establish an X,Y coordinate to any point or pixel on a given vector. This X,Y coordinate is relative to a coordinate system whose origin is at the bottom, lefthand corner of the CRT display.

With a raster driven plotter, the CRT display must be copied from top to bottom and from left to right. This means that the highest Y coordinate and the lowest X coordinate must map to the lowest output buffer memory location. One way to achieve this is by subtracting each Y coordinate from the maximum possible Y coordinate; this maximum Y value varies when the picture is processed in slices.

There are 1056 pixels for each Y coordinate, which must also be considered when mapping a pixel to a memory location. Each CRT pixel is represented by a 2-bit intensity code. Each horizontal stripe on the CRT display therefore requires 264 bytes of memory. Any pixel to memory mapping algorithm must first multiply

the Y coordinate by 264. The resulting address is not unique, and must be adjusted using the X coordinate information.

An efficient mapping algorithm packs four pixel intensities into a single byte. Fig 4 shows the bit organization of a single byte with four sets of pixel intensities, or cells, packed into it. The physical location of a single pixel now includes not only a 20-bit address, but also a cell number. The cell number must come from the unused part of the coordinate, the X coordinate. Since there are only four cells per byte, only two bits of the X coordinate are needed to determine which cell is affected. The remaining bits of the X coordinate represent an offset from the address determined by multiplying the Y coordinate by 264. The complete physical address of a CRT pixel is, therefore, the combination of the calculated physical address and the cell number.

Once the physical address with the cell number of a pixel at the beginning of a line segment is known, a CRT line can be drawn in memory by adding a delta factor to the starting pixel address. Fig 5 shows the eight possible directions a pixel may move away from its present position. Any change in the Y direction is actually a change of some multiple of 264 bytes in the physical address of the pixel. The only consideration here is an increment or decrement in the Y direction. Fig 5 also shows that the pixel could move in the X direction. Since the Y coordinate is not changing and X is changing by plus or minus one, only the cell number is affected, as shown. Care must be taken to adjust the offset part of the physical address if the cell number exceeds three or goes negative. Movement away from the present pixel position at 45° angles is handled by adding in fractional parts of the delta factors. The fraction turns out to be the tangent of the line angle.

Although assembly language code must be used to generate addresses of data when these addresses span a 64k-byte data segment, it is still desirable to use a high level language whenever possible in developing application software. The executive portion of the application software, for instance, can be written in a high level language without adversely affecting system operating speed.

Applications such as the vector to raster converter usually contain a small section of code that accounts for most of the execution time. If this portion of the code is programmed in assembly language and then linked to the remaining portion of the program, which is written in a high level language, the resulting program usually executes at least an order of magnitude faster than a program written entirely in a high level language. Some compilers do not allow the insertion of assembly language code within programs written in a high level language. In these cases, subroutines or procedures written in assembly language usually can be linked in prior to load time. Writing a subroutine or procedure in assembly language that is to be activated by a high level language program requires knowledge of the parameter passing convention and the calling sequence implemented by the particular compiler to insure that procedure execution does not destroy the linkage mechanisms set up by the compiler.

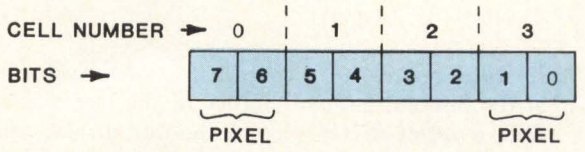

Fig 4 Data format for raster display. With 20-bit address, CPU addresses each byte, which contains encoded intensity information for four pixels or cells

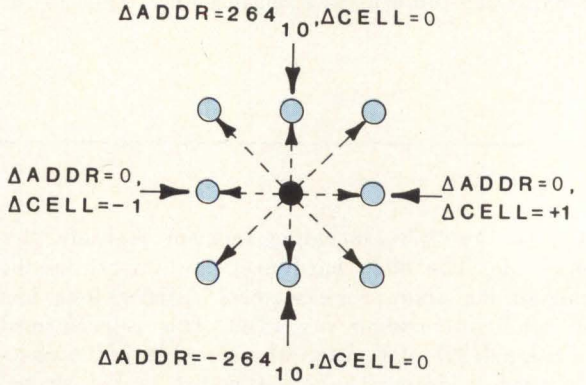

Fig 5 Possible pixel position changes. Incremental change in CRT's pixel position is reflected in memory by appropriate change in pixel's associated physical address. Actual change in address is determined by direction of pixel movement relative to its previous position

One of the most straightforward methods for interprocessor communication involves use of a common memory area. Each processor locks out the other processor when writing into common memory. The 8086 has a lock instruction prefix that performs this operation. The communication protocol used by the two processors is somewhat application dependent and can be set by the programmer to pass necessary information as efficiently as possible. In this example, most of the information that must pass between the two processors involves buffer control. Since one processor is essentially an I/O controller, it must be told when the next output buffer is ready to be sent and where this buffer resides in memory. The IOP must, in turn, inform the conversion processor when it has emptied and freed the output buffer.

Deciding where the common memory area is to be located involves consideration of bus contention possibilities. In this vector to raster converter example, the common memory area could reside on either processor board or on the separate memory boards. If it is located on either the IOP board or the conversion processor board, local bus contention between the onboard and offboard processors could result. Locating the communication area on a separate memory module would eliminate any contention on the local bus when one of the processors is polling the communication area while waiting for a particular event to occur.

Proper synchronization between processors is equally critical to successful operation of any multiprocessor system. Synchronization of the system can usually be accomplished by a system reset, either hardwired to each processor or with one processor resetting the remaining processors in the system once it has been reset externally. The master processor in the system would naturally have this responsibility and could accomplish this task through a hardwired interrupt or processor reset.

Summary

Faster microprocessors afford an alternative to microprogrammed hardware in design problems requiring both fast response and high data throughput. Although the multiple microprocessor approach introduces potential problem areas, such as interprocessor communication and system bus contention, the high throughput offered by loosely coupled microprocessors makes this design approach useful when operating speed is considered critical.

The first attempt to implement a microprocessor based vector to raster converter indicated that the software solution was feasible, but did not meet performance criteria. However, this design suggested that a multiprocessing system, programmed largely in a higher level language, would perform well if the hardware were configured to fulfill application requirements.

A second implementation combined high level language executive software with assembly language code in a dual-microprocessor hardware environment. Problem solutions treating interprocessor communication and synchronization, system bus contention, shared resource contention, and language interfacing were customized to the application, producing a high performance system that is inherently easy to enhance and maintain.

Using a second microcomputer board essentially as an I/O controller may be overkill in some applications. When slower system operating speed is acceptable, a single CPU approach could be sufficient. The introduction of special purpose I/O chips, such as Intel's 8089 and other DMA type devices with limited processing capabilities, affords increased system throughput without the overhead incurred by adding a second CPU. Advantages of microprocessor based, high level language software over microprogrammed hardware accrue in either case.

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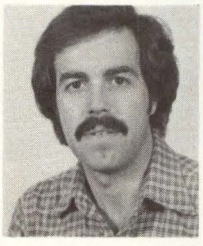

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Operating a consulting firm in Santa Rosa, Calif, John Greaves previously helped to build a program in computer engineering at Southeastern Massachusetts University, managed research grants, and did consulting work in the mini and microcomputer systems area. He received a PhD degree in electrical engineering from the University of California at Santa Barbara.

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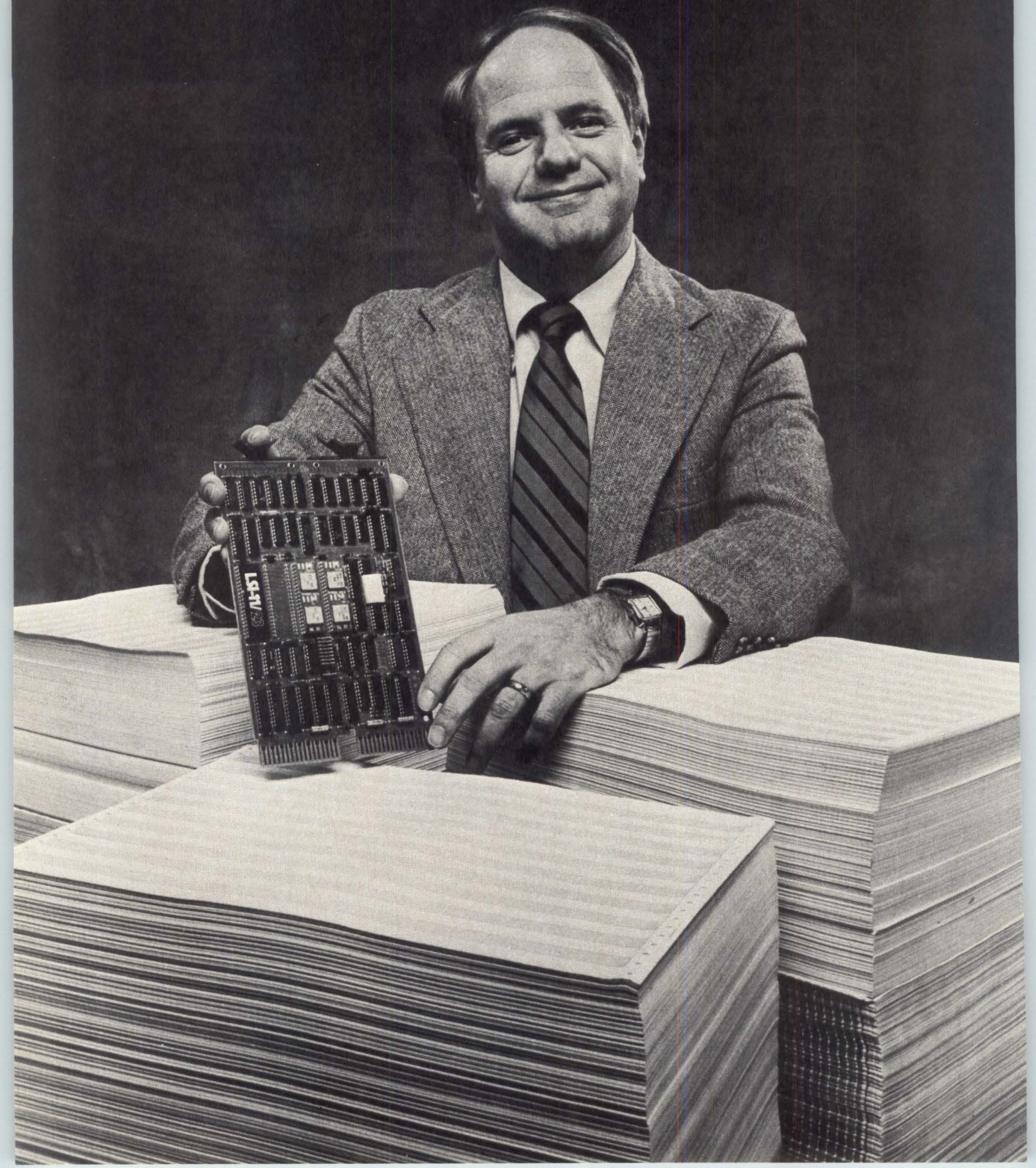

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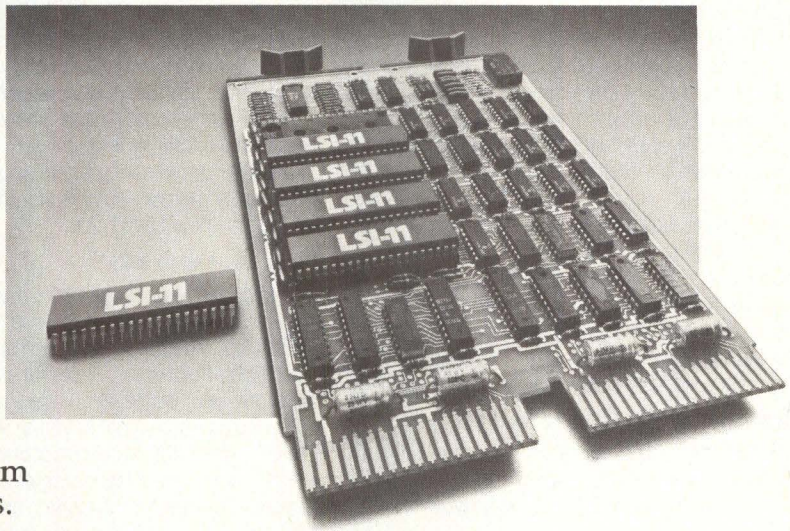

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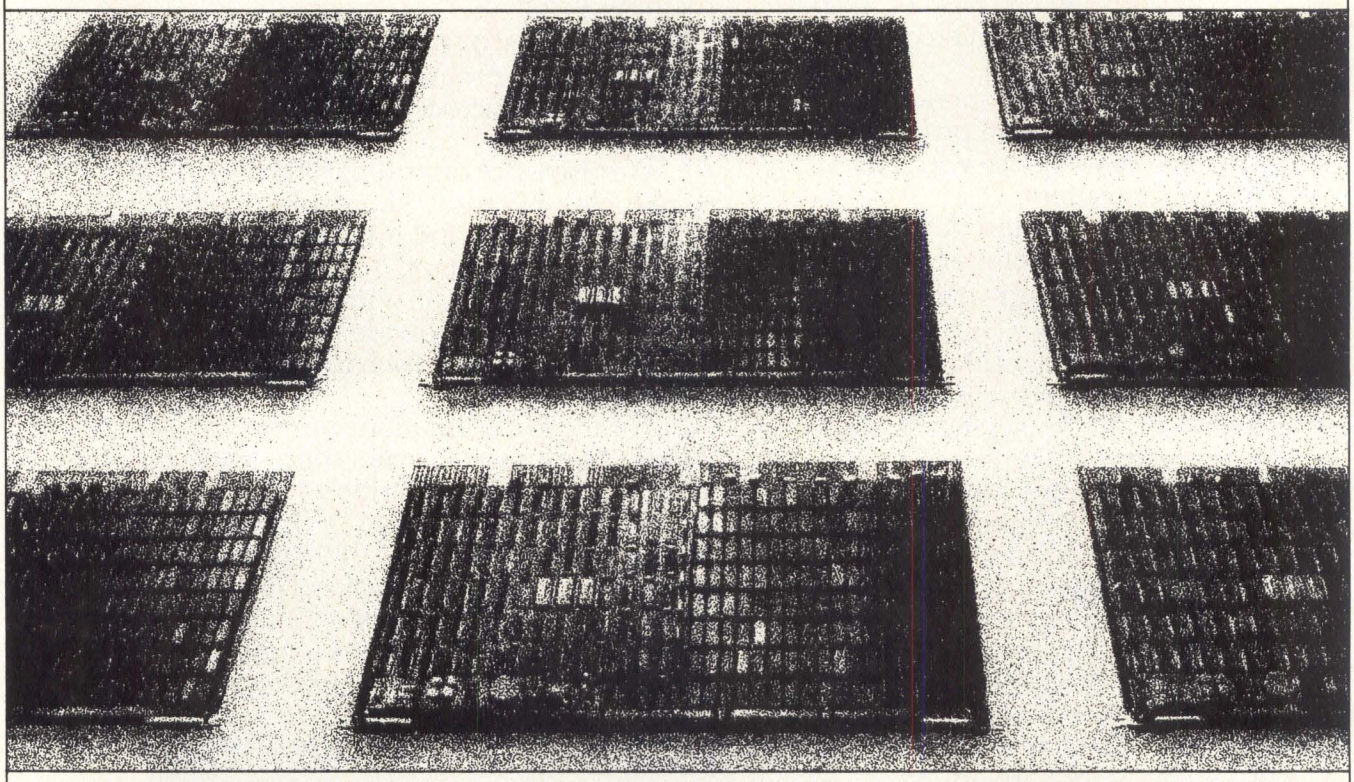

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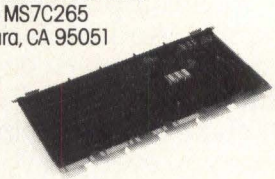

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LSI HARDWARE IMPLEMENTS SIGNAL PROCESSING ALGORITHMS

Dedicated LSI multipliers used in realtime digital signal processors achieve data rate reduction, pulse compression, high speed convolution, and fast Fourier transformation

William J. Finn TRW LSI Products, El Segundo, California

A major factor in the effectiveness of a digital signal processor is the function of multiplication. Most aspects of digital signal processing require a large number of multiplications. Unfortunately, multiplication has traditionally been the most time consuming and expensive computational function to implement. As a result, designers have been forced to deal with the hardware constraints of the signal processor.

Of the proposed approaches to the problem many have been based on exotic programming techniques intended to reduce the number of multiplies. As the schemes became theoretically complex, the move towards computational conservation was initiated. As a result, the number of multiplies and the amount of memory required became the measure of complexity for digital signal processors. A typical practice in early digital signal processors was to use a very fast multiplier and time multiplex it over all the functions requiring multiplication. As a result, very fast emitter coupled logic (ECL) array multipliers were designed and built. Array multipliers, however, are expensive and power consuming; an early proposal, a 40-ns, 17 x 17 array multiplier, used 164 ECL adders and consumed 60 W of power.

A solution to this problem lies in the monolithic LSI multiplier, which was developed by TRW in the early 1970s. This single chip is capable of performing a complete 16 x 16 multiply in 100 ns, while consuming only 3 W (Fig 1).

Most signal processing schemes require as many adds as multiplies. Consequently, there are also monolithic LSI multiplier-accumulators (MACs), ranging in size from 8 x 8 to 16 x 16 bits. The larger multiplier has a 35-bit accumulation register, which gives a complete 16 x 16 multiply as well as an addition or subtraction in 115 ns (Fig 2).

Standard signal processing algorithms used in finite impulse response (FIR) filters, matched filters, and complete fast Fourier transforms (FFTs), which depend on multiply and add operations for all data computations, can be implemented using LSI hardware. The cost per multiply per unit of time has become so negligible in a large digital signal processor that design emphasis has

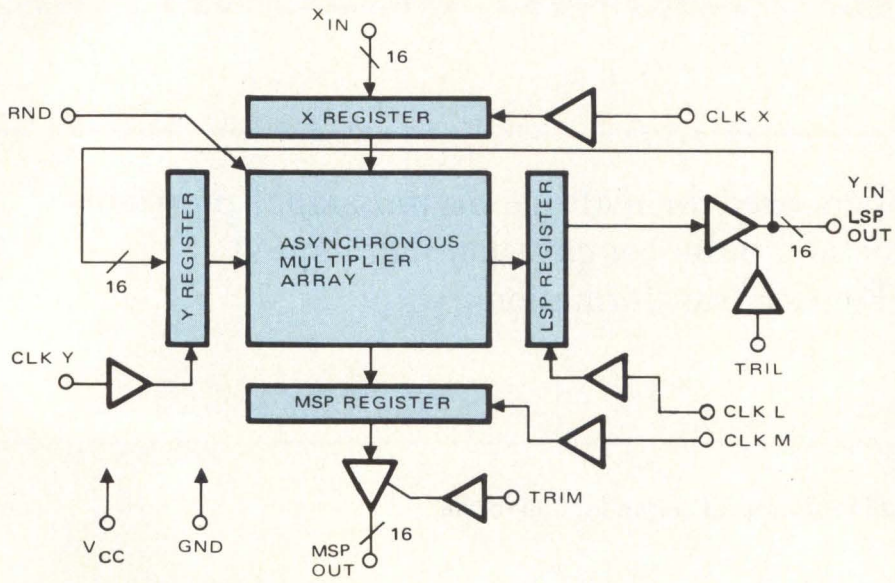

Fig 1 Fully parallel 16- x 16-bit multiplier. LSI n x n parallel multipliers are high speed transistor-transistor logic, monolithic devices capable of either 2's complement, unsigned magnitude, or mixed mode multiplication

shifted from complex software routines to a single-chip, dedicated hardware approach.

Matched Filtering

In a receiver for pulse compression radar, for example, the received signal and the original transmitted signal are cross-correlated in a matched filter. A matched filter optimizes the peak signal to noise power ratio in the presence of additive Gaussian noise, maximizing the probability of detecting a target. Since the filter is exactly matched to the transmitted signal, the impulse response is the time-reversed complex conjugate of the transmitted signal, and the output is the auto-correlation function (ACF) of the transmitted signal.

A standard approach for achieving this filter type is to use discrete Fourier transforms (DFTs). A DFT differs from a continuous Fourier transform because it operates on sampled waveforms defined over finite intervals. The resulting spectral components in the frequency domain are then coherently added, using a fast Fourier algorithm to achieve high speed DFT convolution.

In this technique, x(n) and h(n) are time sampled sequences of received and transmitted data, respectively. Each 2-point DFT (also called a butterfly) consists of one complex multiplication, two complex additions, and two complex subtractions (Fig 3). The resulting transforms, X(k) and H(k), are combined by multiplication and the product, Y(k), is inverse transformed to yield the output y(n) (Fig 4). Using the multiplier-accumulator described earlier, a 2-point butterfly can be performed in less than 1 μs.

Computational Requirements

In pulsed radar, the time span from the beginning of one transmission or pulse to the start of the next pulse is called an interpulse period (IPP). All computations must be performed within one interpulse period; thus, the convolution discussed previously must be performed in 1 ms for a 1-kHz system. The number of butterflies for an N-point, radix-2 FFT is

$$\frac{N}{2}\log_2 N \qquad (1)$$

The FFT algorithm consists of $\log_2 N$ stages, with each stage requiring N/2 butterflies.

The total computation time for one convolution is

$$T_C = (N \log_2 N)\ T_B + N\ T_M \qquad (2)$$

where T_B is the time required for one butterfly and T_M is the time required for one multiply (in most cases $T_B \cong T_M$). A 4k-point transform for such a system would require a multiplier speed of 20 ns for realtime operation on 8-bit words. However, by designing the

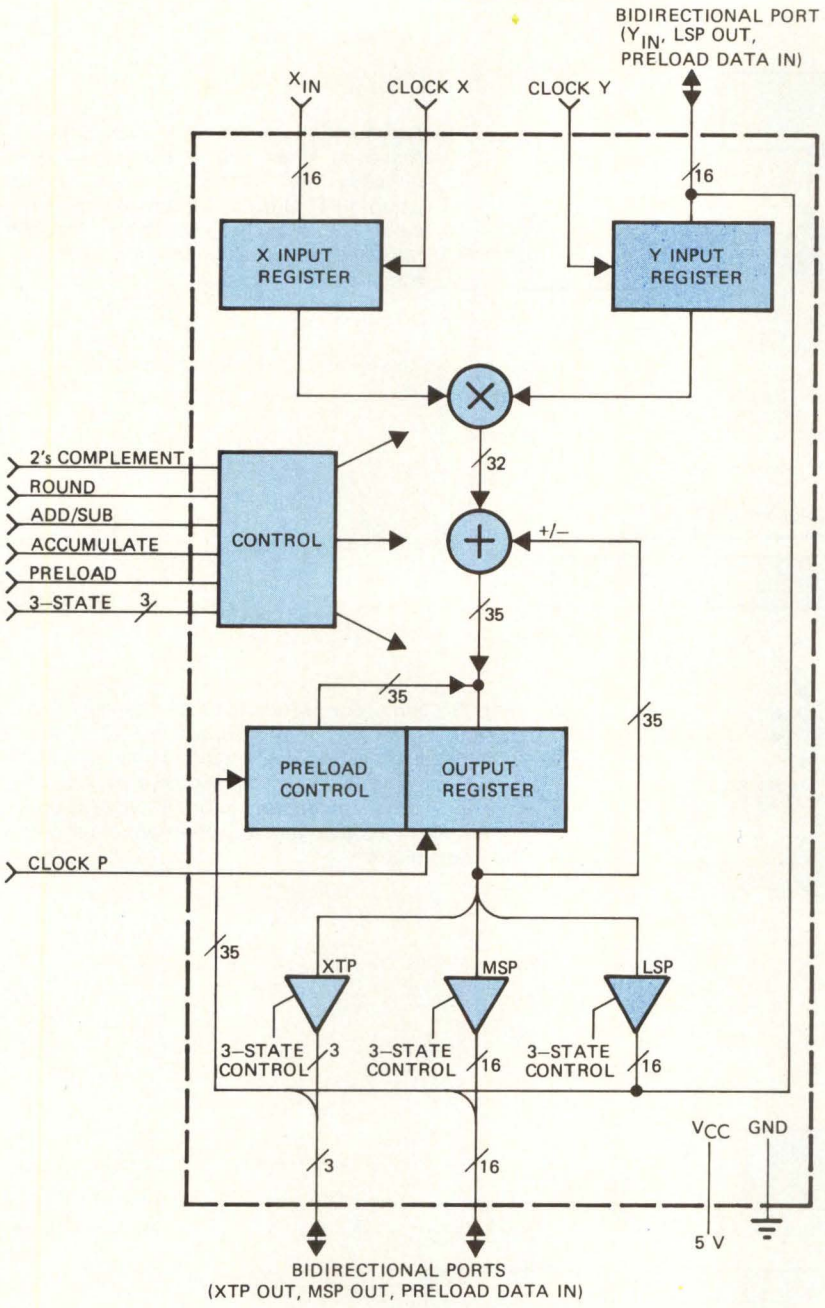

Fig 2 Multiplier-accumulator. Optimized arithmetic unit performs multiplications and product accumulations inherent in most digital signal processing algorithms

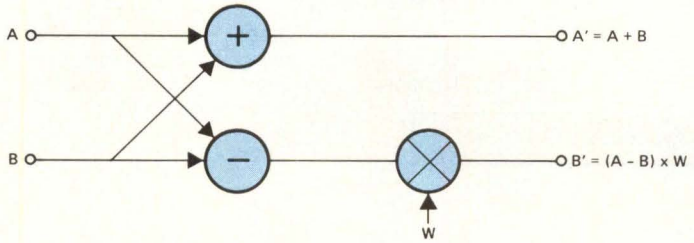

Fig 3 Radix-2 decimation in frequency butterfly. Two complex additions and subtractions and one complex multiplication are necessary. Complex multiplication requires four MAC machine cycles

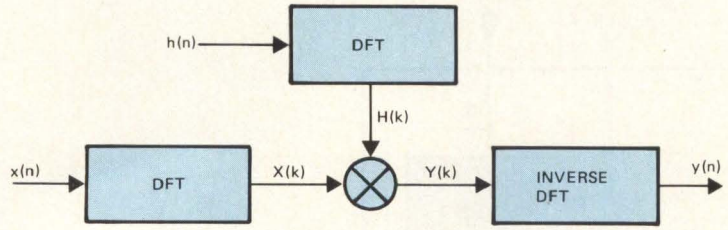

Fig 4 High speed DFT convolution. Achieved when two time-sampled sequences are frequency transformed using FFT algorithm, convolution results are complex multiplied (using MAC). Product Y(k) is then inverse transformed to complete process

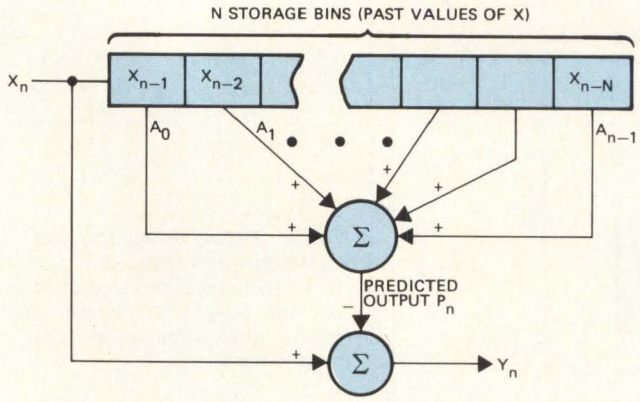

Fig 5 Nth-order predictive mechanization. Function can be implemented as FIR filter with fixed or varying coefficients which weight incoming data based on statistical analysis of previous data. Redundant information can be removed to reduce amount of information to be transmitted

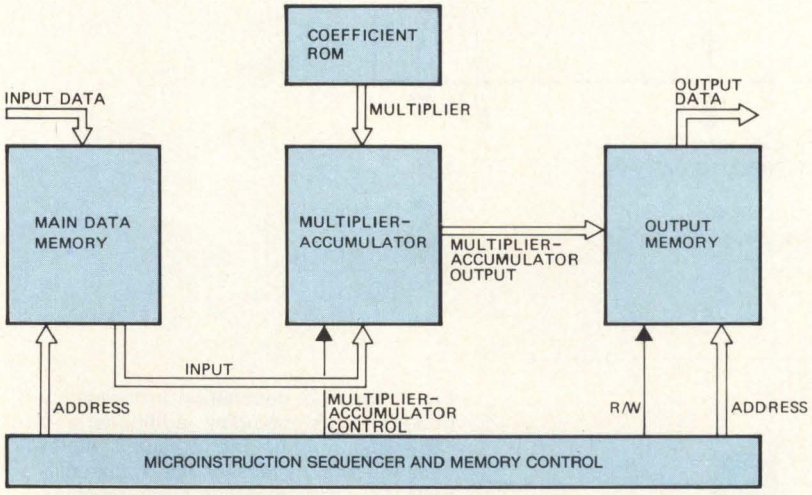

Fig 6 FIR filter architecture. In simplest form architecture consists of data memory, coefficient ROM, multiplier-accumulator to perform sums of partial products, and simple logic to control sequencing and data shuffling

architecture so that the multiplier is continuously serviced with new data to process (pipelining), computational efficiency of this process can be increased, reducing the total time to approximately

$$T_C = 3NT_M \quad (3)$$

Using the previous example, the required multiply time would be only 83 ns, well within the capability of presently available LSI multipliers.

Digital Signal Processing Architectures

A major function of a digital signal processor is data rate reduction, and an FIR filter utilizing predictive coding schemes is one method of achieving just that. A 1-dimensional, Nth-order, predictive mechanization is illustrated in Fig 5. Radar systems are particularly well suited for a predictive mechanization. The effectiveness of this kind of approach is highly dependent on the accuracy of the *a priori* knowledge (good predictions) of the incoming sampled data; in radar, knowledge of the expected signal can be very accurate.

The approach is to predict the value of X_n based on past values of X located in N storage bins. Previous knowledge of the source (statistical analysis) determines the coefficients of prediction (A_0 through A_{n-1}). Updating the coefficients allows the impulse response of the filter to be adaptively improved. If the prediction is satisfactory, $X_n - P_n$ will be smaller in magnitude than X_n, so that less information will have to be transmitted. An Nth-order predictor, like the type shown, requires N multiplies and N + 1 adds, making it a natural process for a multiplier-accumulator.

Since most transmitted radar signals are time limited, operation of a matched filter is equivalent to a finite impulse response filter, in which the convolution of the transmitted signal is used as the impulse response of the FIR matched filter. Fig 6 shows how an FIR filter can be implemented.

In this architecture, all computations are performed within the multiplier-accumulator; therefore, external arithmetic logic is not necessary. The microinstruction sequencer and memory control can be designed with presently available bit-slice elements. If computation is done in batch mode, the main data and output memories are important because they store the batch of information to be processed.

For continuous realtime processing, these memories can be as simple as local storage registers or they can be eliminated entirely, depending on the overall processor requirements and timing constraints.

The computational requirements of a digital signal processor often exceed the capabilities of the hardware if conventional architectures are used. One solution to this problem is an architecture that lends itself to a pipeline structure. The pipelined architecture (Fig 7) not only provides filter design flexibility but also helps optimize filter throughput.

Advantages of this architecture center around the two data buses. A multiplier-accumulator serves as the central computational element, but in this case, two capabilities have been added. The first, a high speed multiplexer, allows the two data buses to be switched or pingponged.

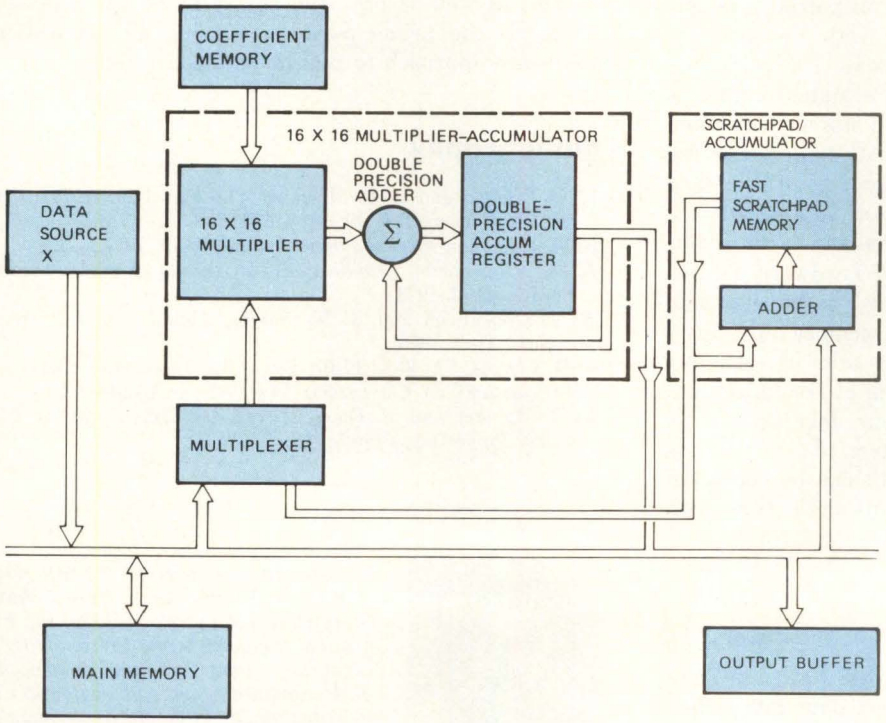

Fig 7 Digital filter pipeline structure. Two data bases, multiplexer, and fast scratchpad/accumulator are used to continually supply data to MAC, optimizing performance and increasing filter throughput

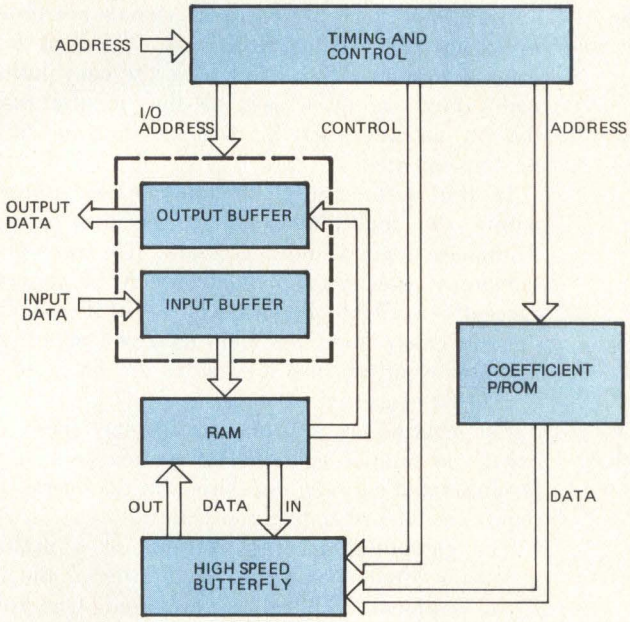

Fig 8 FFT processor. Utilizing multiplier-accumulator to perform high speed butterfly, processor can compute 1k-point FFT in less than 6 ms

Therefore, the MAC can be serviced either by incoming data from the source, or by intermediate computational results taken from local storage memory.

The second, and most salient capability, is the fast scratchpad memory and adder. This function provides local storage and, in conjunction with the second data bus and the multiplexer, maximizes pipelined computation. Throughput for realtime processing therefore is minimized. The adder is included so that partial products can be summed without interfering with the primary computation being performed in the MAC.

A standard approach to designing a matched filter is to use an FFT (Fig 8). Input data are stored in random access memory (RAM) via an input data buffer, and the associated coefficients are stored in programmable read only memory (P/ROM). P/ROM is used so that the coefficients can be easily adjusted or changed to fit a particular FFT requirement. The control hardware (which is implemented using bit-slice elements) takes data and the corresponding coefficient out of memory and buses them into the high speed butterfly; results of each DFT are then stored back into RAM. The final results are addressed and bused out via the output data buffer. By utilizing a multiplier-accumulator (16 x 16) to perform the high speed butterfly, a 1k-point FFT can be computed in less than 6 ms (assuming a 150-ns cycle time with each butterfly requiring eight cycles).

Summary

The described architectures demonstrate how LSI dedicated hardware can be utilized to effect data rate reduction by means of a predictive mechanization, pulse compression utilizing an FIR matched filter, computational capabilities via pipelining, high speed DFT convolution, and an FFT processor. Although radar is used as a vehicle for discussion, the concepts presented can be applied to any system that requires realtime digital signal processing.

Digital signal processors are particularly attractive because they provide a high degree of flexibility. A digital processor must be able to perform many different algorithms, as well as have the ability to adapt easily. Flexibility is the prime reason for using an LSI dedicated hardware approach to realtime system design.

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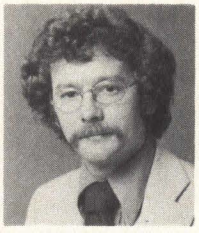

William J. Finn earned his BS degree in electrical engineering from California State University at Northridge. His background includes work in reliability engineering, new product development, and commercial aircraft navigation system design. At TRW, he has specialized in spectrum analysis and digital filtering for radar and telecommunications.

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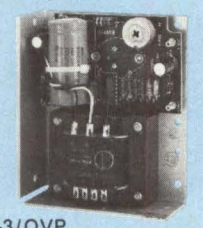
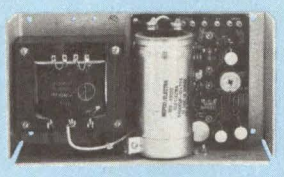
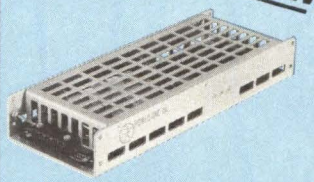
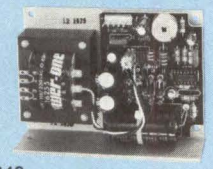
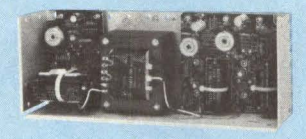
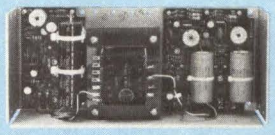
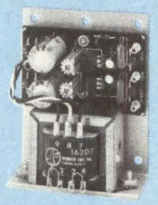
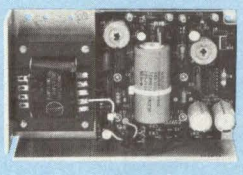
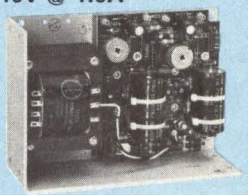
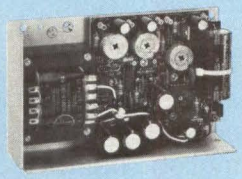
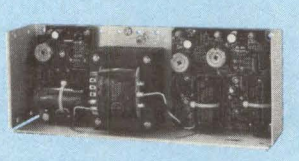
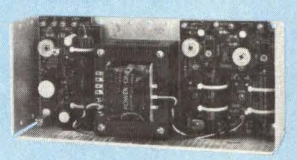
SINGLE OUTPUT & LOGIC POWER SUPPLIES • 56 "off the shelf" models • 2V to 250V, 0.1A to 40A • ± .05% regulation • 115/230 VAC input	**5V @ 3A, w/OVP**  HB5-3/OVP $24.95 single qty.	**5V @ 12A, w/OVP**  HD5-12/OVP $79.95 single qty.	**5V @ 40A, w/OVP** NEW  SK5-40/OVP Switching Model $250.00 single qty.
FLOPPY-DISK SERIES • 8 "off the shelf" models • Powers most popular drives • Single/dual drive applications • 2-year warranty	**5V @ 0.7A, w/OVP** **12V @ 1.1A/1.7A PK** NEW  CP340 For one 5.25" Media Drive $44.95 single qty.	**5V @ 1A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 1.5A/1.7A PK**  CP205 For one 8.0" Media Drive $69.95 single qty.	**5V @ 2.5A, w/OVP** **−5V @ 0.5A, w/OVP** **24V @ 3A/3.4A PK**  CP206 For two 8.0" Media Drives $91.95 single qty.
DUAL OUTPUT MODELS • 15 "off the shelf" models • ±5V to ±24V, 0.25A to 6A • I.C. regulated • Full rated to +50°C	**12V/15V @ 0.25A** NEW  HAD12-.25/HAD15-.25 $32.95 single qty.	**5V @ 2A, w/OVP** **9 − 15V @ 0.5A**  HAA512 $44.95 single qty.	**±12V @ 1.7A or** **±15V @ 1.5A**  HBB15-1.5 $49.95 single qty.
TRIPLE OUTPUT MODELS • 10 "off the shelf" models • 5V plus ± 9V to ± 15V outputs • Models from 16W to 150W • Industry standard size	**5V @ 2A, w/OVP** **± 9V to ± 15V @ 0.4A**  HTAA-16W $49.95 single qty.	**5V @ 3A, w/OVP** **±12V @ 1A or** **±15V @ 0.8A**  HBAA-40W $69.95 single qty.	**5V @ 6A, w/OVP** **±12V @ 1.7A or** **±15V @ 1.5A**  HCBB-75W $91.95 single qty.

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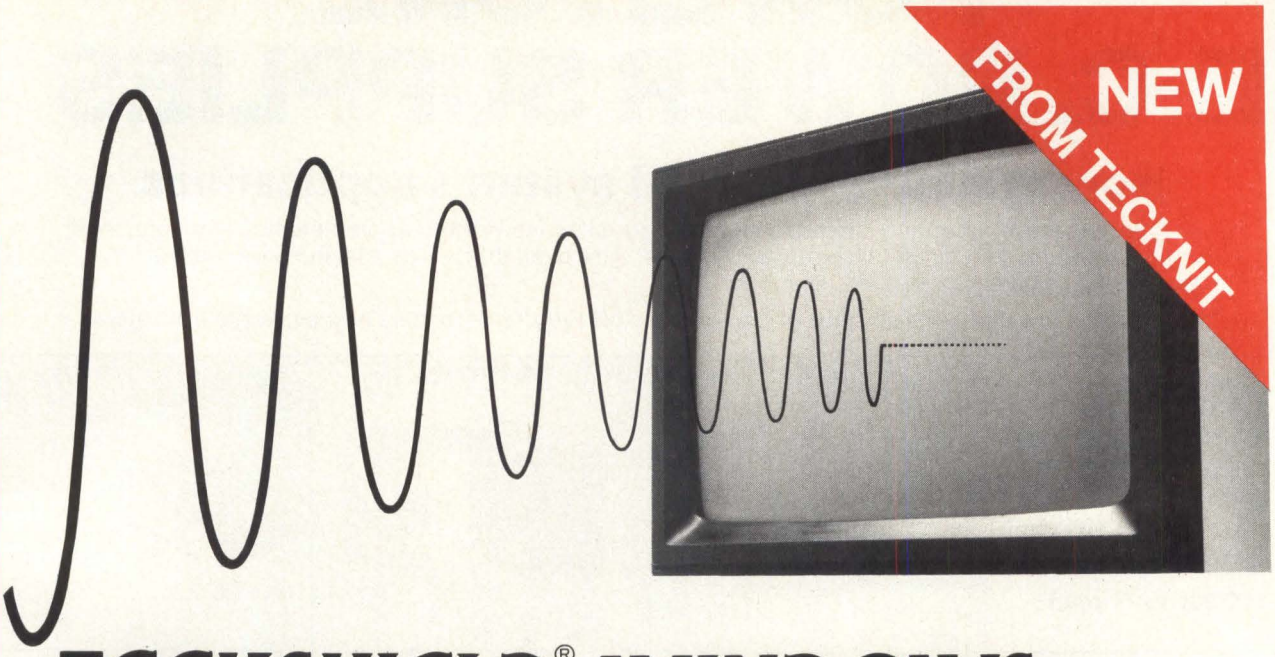

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EMI SUSCEPTIBILITY TESTING OF COMPUTER SYSTEMS

Problems caused by electromagnetic interference are examined and accompanied by a description of a test instrument that provides quantitative determination of system noise susceptibility

Joe E. Deavenport DEDCO, San Diego, California

Today's electronic circuits are characterized by ever increasing bandwidth and sensitivity. This, combined with the proliferation of sources of electromagnetic interference, has created a serious problem for equipment designers, manufacturers, and users, and calls for an examination of the nature of electromagnetic noise and of the problems it can cause. An instrument that produces standard, repeatable sources of electromagnetic noise is available for evaluating the noise sensitivity of digital equipment, and for troubleshooting noise problems in systems and components.

Electromagnetic Interference

Electromagnetic interference (emi) is any unplanned electrical signal that impinges on an operating electronic system and causes system performance degradation or malfunction. It is generally viewed as an external interference, one having many possible sources, and with no high or low frequency limit. In a computer system, problems resulting from emi can range from single bit errors to complete destruction of programs or files.

In its simplest and most familiar manifestation, emi is superimposed on dc power supply voltages in the form of drift, unplanned dc voltages, ripple, and noise. In operating circuits emi is also generated by signal reflections and crosstalk due to common impedances: resistance, capacitance, and both mutual and self-inductance. The original design of the system may result in inherent common impedances, or they may be created by such system degradations as aging or failure of components, open solder joints, leakage paths, damaged or corroded connector contacts, and loose connections.

Crosstalk, a type of emi, is particularly insidious in large digital systems. While it is always synchronous, peak amplitudes occur at an unpredictable subharmonic of the clock frequency because the amplitude is directly proportional to the number of circuits either switching into or statically residing in a particular state. Other internally generated emi may be caused by vibration in cables and connections, relay switching, transformers, and power supplies. Noise sources inherent in components such as resistors and semiconductors are generally of too low a level to affect digital systems unless the component involved is on the verge of failure.

The externally generated, asynchronous, single transient is the most elusive form of emi. It is a burst of electromagnetic or electrostatic energy, either conducted or induced into internal circuitry. External noise sources include both artificial and natural phenomena: radar and other broadcast signals, arc welders, diathermy systems, rf induction heaters, motors, power contactors, fluorescent lights, x-ray equipment, lightning, corona effect, and electrostatic discharge. Externally generated emi enters the system through cabling or openings in the enclosures, or by static discharge directly to metallic enclosures with secondary coupling to internal circuitry.

Cumulative and Statistical Considerations

Three characteristics of emi should be considered in evaluating system susceptibility. First, all forms of emi add directly to a signal. Worst case coincidence of peak emi from all sources determines the likelihood of failure. Second, circuit response to emi depends on polarity. For example, if there is a high level input to a gate, positive emi superimposed on the input may have little or no effect; however, negative emi may be amplified and transmitted. Finally, a large computer system may run for several minutes before interfering crosstalk is created by a worst case combination of signals.

These considerations dictate that, for an adequate evaluation of system susceptibility to emi, testing must last long enough to encounter the coincidence of worst case power supply variations, internally generated noise, and externally injected emi. For a reasonably sized system, this requires several minutes testing at a number of different system locations while applying thousands of external noise transients.

Susceptibility Testing

Most system manufacturers conduct power supply margin tests. In the past, when slower circuit response was involved, it was adequate to determine whether or not individual circuits could tolerate specified power supply variations. Now that circuit response is measured in nanoseconds, and interconnections reflect delays that exceed signal rise and fall times, power supply margin testing also helps evaluate internally generated emi when all circuit states are exercised to create worst case emi patterns.

The broad frequency response of today's circuits requires additional testing for susceptibility to externally generated emi, which often appears as very high frequency transients. There was no need for such testing when circuits would not respond to these transients; no equipment was developed for this purpose, and no standards were established. As the state of the art in circuit design advanced, and the need for such testing became apparent, any device that would create emi was put to use: self-chattering relays, fluorescent light banks, Tesla coils, drill motors, and light switches. These techniques were hardly productive of quantitative information or repeatability, or a potential for standardization.

The most severe and familiar sources of externally generated emi are ac line transients and electrostatic discharge from the human body. On or off switching of even such a low power device as an electric typewriter can create 1000-V line transients. A great many of these transients are coupled, either capacitively or through the safety ground connection, to other systems as common-mode signals, signals that affect all signal paths equally with respect to ground. A human body can accumulate static charges up to 25,000 V, depending on the ambient humidity. (At relative humidity above 50%, leakage is generally sufficient to prevent static accumulation.) This charge readily arcs to any grounded metal, such as a system frame.

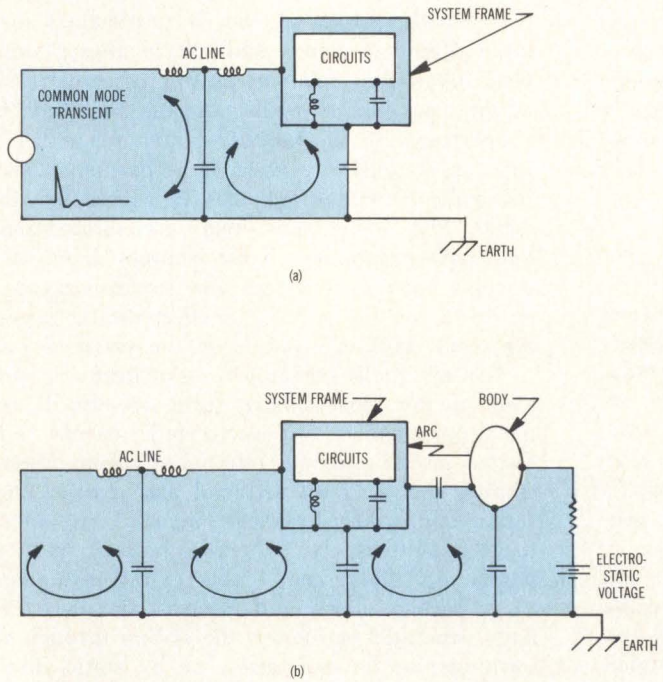

Fig 1 Two types of externally generated emi, (a) ac line transients, and (b) electrostatic discharge. Inductances and capacitances represent distributed impedance paths for noise current flow, creating common-mode resonances. Arrows indicate current flow

Both these typical transients produce similar effects. The system frame with its various distributed impedances to earth ground is shock-excited into complex common-mode resonances in the 10- to 100-MHz range. These also appear in all parts of the system contained within the frame. While common-mode signals are not a problem by themselves, unbalanced circuits invariably convert common-mode signals to differential-mode signals, signals that affect all signal paths differently and cause interference. Fig 1 illustrates these two mechanisms for external generation of emi. Conversion of common-mode transients to differential-mode interference is shown in Fig 2.

Of these two causes of external emi generation, electrostatic discharge (ESD) is generally the most severe and the easiest to simulate. ESD is an arc with a rise time in the nanosecond range. Line transients are frequently generated by arcs with similar rise times, but their source is generally remote, and their high frequency components are well attenuated by the time they reach other systems. In any event, it is considerably more difficult to simulate high frequency transients on an active ac line.

The ball and wand tester was devised to simulate ESD and thereby provide a gross indication of emi susceptibility. This device consists of a metallic ball mounted at the end of an insulating handle. A discrete capacitor is charged to high voltage and discharged into the ball through a resistor when the ball is touched to a metallic enclosure. However, this technique suffers from a lack of standardization, no repeatability, and low accuracy. These factors inhibit the utility of the ball and wand approach for design and troubleshooting applications.

There are other shortcomings to this technique.

(1) The discrete capacitor and discharge resistor are intended to simulate human body capacitance and impedance; however, there is no "standard body." Capacitance values used have ranged from 100 to 1000 pF, and resistances from 10 to 1000 Ω. Empirically derived complex networks have also been used.

(2) "Acceptable" discharge voltage levels range from 500 to 15,000 V. Generally, lower voltages and lower resistances are combined with higher capacitances; higher voltages and higher resistances are used with lower capacitances.

(3) An arbitrary distinction is made between testing a system for moderate or severe ESD in controlled and in uncontrolled environments. Environments are seldom constant.

(4) The operator controls the rate and number of discharges applied to the system under test. The rate may vary from 1 to 3 discharges/s, with only 50 to 100 discharges applied at any location on the enclosure. Except by rare coincidence, this is not sufficient to show the true noise threshold.

(5) No attempt is made to simulate distributed capacitances to earth or to the equipment.

(6) The arc is open to the ambient atmosphere, leading to inconsistent characteristics.

(7) The 6- to 8-ft (1.8- to 2.4-m) long ground return wire to the discrete capacitor is part of the discharge circuit. This will not only distort the waveform due to inductive effects, but noise radiated from this wire may also distort test results depending on the routing of the lead.

Another Approach—Background and Description

Several years ago International Business Machines Corp (IBM) recognized the need for standardized emi susceptibility testing. As a result of research into emi problems in computer systems, the Electromagnetic Compatibility Simulator (EMCS) (Type 1) was developed to provide IBM field engineers with a reliable, controllable, and repeatable test method for determining the emi susceptibility level of newly installed systems. Once these levels had been measured and recorded, the instrument could be used later to determine the effects of changes

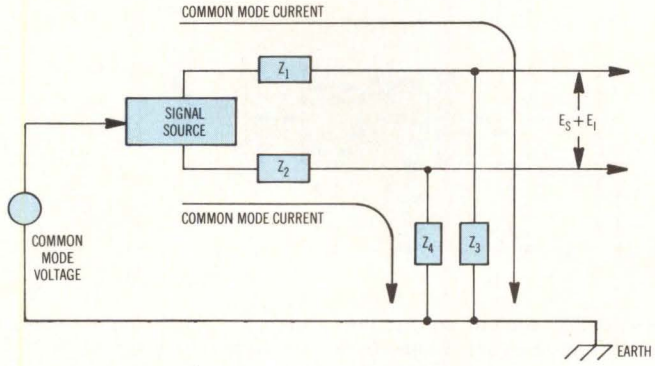

Fig 2 Common mode to differential mode conversion. Interference voltage, E_I, superimposed on signal voltage, E_S, will be zero only if $Z_3/Z_1 = Z_4/Z_2$ at all frequencies

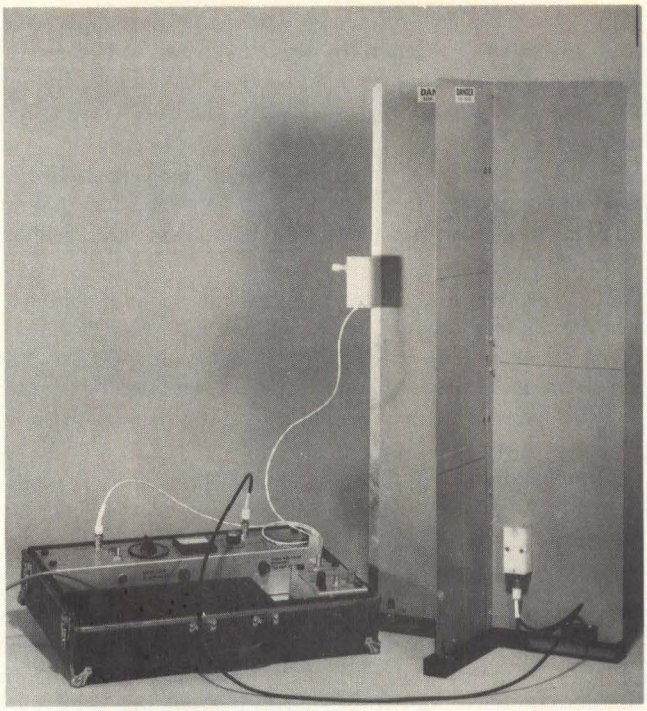

Fig 3 Zapper assembled for basic system susceptibility testing. Crossed vanes are 3′ (91.5 cm) high by 18″ (46 cm) wide. Mercury switch assembly attaches to one edge of vanes at adjustable height. Hardened steel point (covered by protective cap in photograph) protrudes from switch assembly to make direct contact with frame of system under test. Power supply in case provides high voltage to charge vane and drive voltage for mercury switch

to the system or to warn of degradation, by a direct comparison of the initial and the current susceptibility levels. This objective required precision, repeatability, and independence from environmental and operational factors not previously obtainable. The instrument also provided a standard, repeatable emi source for use in system design phases. Accessories extended its utility for application as a valuable troubleshooting tool. The EMCS (Type 1) was made available only to qualified IBM service organizations. An identical, field-proven unit, called the Zapper, is now available to the entire industry. Fig 3 shows major components of the instrument assembled for basic system susceptibility testing.

The unit achieves the required precision and repeatability for several reasons.

(1) The vane is one plate of a capacitor with fixed dimensions. With the discharge point in contact with the system under test, the distributed capacitance is established by the fixed separation and is exactly repeatable. With the vane standing on the floor, the distributed capacitance between it and the floor (earth) is established, fixed, and repeatable.

(2) Two distributed capacitances are included in the high frequency discharge path: from frame to earth, and from earth back to the vane. The only lumped inductance along this path is through the switch, resistor, and discharge point, about 3″ (7.6 cm) in total length.

(3) The rate of discharge is at the 50- or 60-Hz line frequency, but can also be controlled manually with a pushbutton.

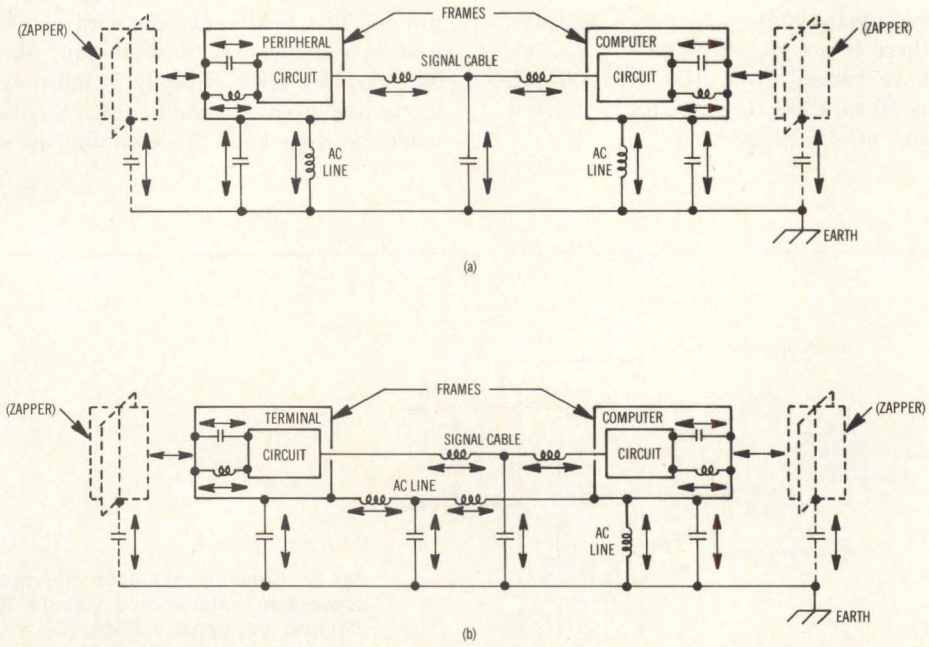

Fig 4 Alternate locations for instrument in system susceptibility testing. System with separately powered peripherals is represented in (a), while (b) shows system with local terminals. Arrows indicate potential noise current paths. Distributed impedances indicate how complex resonances can be excited

(4) Tests at any one location are run for a fixed length of time, typically 3 min. At a 60-Hz rate, 10,800 transients will be injected during this period. This is of major importance in finding the most noise-sensitive condition in the system.

(5) The vane charging voltage, up to 2500 V, is adjusted at the power supply and is read on the integral voltmeter.

(6) Very high current transients are created because the discharge current is limited by only 15 Ω.

(7) The discharge arc is inside a sealed mercury switch and is independent of atmospheric conditions.

(8) A timer is provided to switch off the high voltage after selectable durations of up to 15 min.

Susceptibility thresholds likely to cause a malfunction are precisely repeatable at any time, provided all physical conditions are duplicated, including the point of contact with the system under test. This makes it possible to evaluate changes in operational systems, and makes the tester equally useful during design evaluation. The effect of any physical change to the system, even the effect of rerouting a cable, can be measured with confidence.

The implications of identical physical conditions during tests cannot be overemphasized. No two seemingly identical systems exhibit the same noise thresholds, and a single system will exhibit different noise thresholds, in two different environments. A host of factors can affect susceptibility to noise: circuits, temperature, cable dress, floor construction, frame bonding, grounding, ambient noise, to name a few. Humidity primarily affects electrostatic noise generation, not equipment susceptibility.

The instrument provides standardized emi for evaluation of peripherals or other electronic systems as well as computers. A fixed physical configuration is all that is required. Fig 4 shows a few possible ways of using the Zapper.

Indirect Discharge

The testing system is also useful for systems with nonconducting enclosures, or for qualitative evaluation of broadband noise field effects, eg, near cable runs. In these applications, the switch assembly is lowered to the bottom of the assembled vane and the discharge point is made to contact and discharge to the grounding tab provided on the power supply, creating a broadband noise field. If the vane is fixed in orientation and distance with respect to a system with a nonconducting enclosure, capacitive coupling to internal circuitry is created, and repeatable, qualitative data regarding system susceptibility can be obtained.

Radiating Probes

Four handheld discharge probes are provided for generating more localized noise fields as an aid in isolating areas of noise sensitivity. When using these, the switch assembly is mounted inside a probe converter, and the high voltage is cabled to it. A discrete capacitor inside the converter is charged and discharged by the switch into a 15-ft (4.6-m) shielded twin-conductor cable, terminated into 50 Ω on one of the insulated handheld radiating probes. These allow the operator to probe the system discretely and isolate noise-sensitive areas.

Handheld probes have proved to be highly useful in locating faulty connector contacts and imperfect solder connections. The effect of a bad connection may be visualized by referring to Fig 2. If the illustration is viewed as a cable configuration, and the impedances Z_1 and Z_2 represent either connector contacts or solder joints, it is apparent that, if one of these changes or opens, the circuit balance will be upset, and common mode will be converted to differential mode, creating interference in the signal path.

Summary

While emi can be scientifically analyzed, exact specifications are almost impossible to define because of the many variables that affect emi susceptibility in systems. There is now a standard source of emi that can be used to determine the relative effectiveness of system designs and modifications on susceptibility to emi. Using the standard source, accurate data can be obtained, and minimum levels specified. Degradation below such levels indicates excessive noise sensitivity.

The same instrument is useful in troubleshooting noise problems. In these applications, however, emi design and troubleshooting skills must be developed by experience. This requires familiarity with those system performance, construction, and environmental features that affect susceptibility to emi.

Acknowledgment

Thanks are due to William Gross for his contributions in the preparation of this article.

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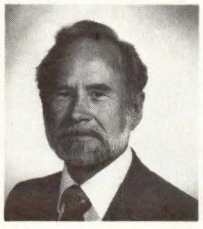
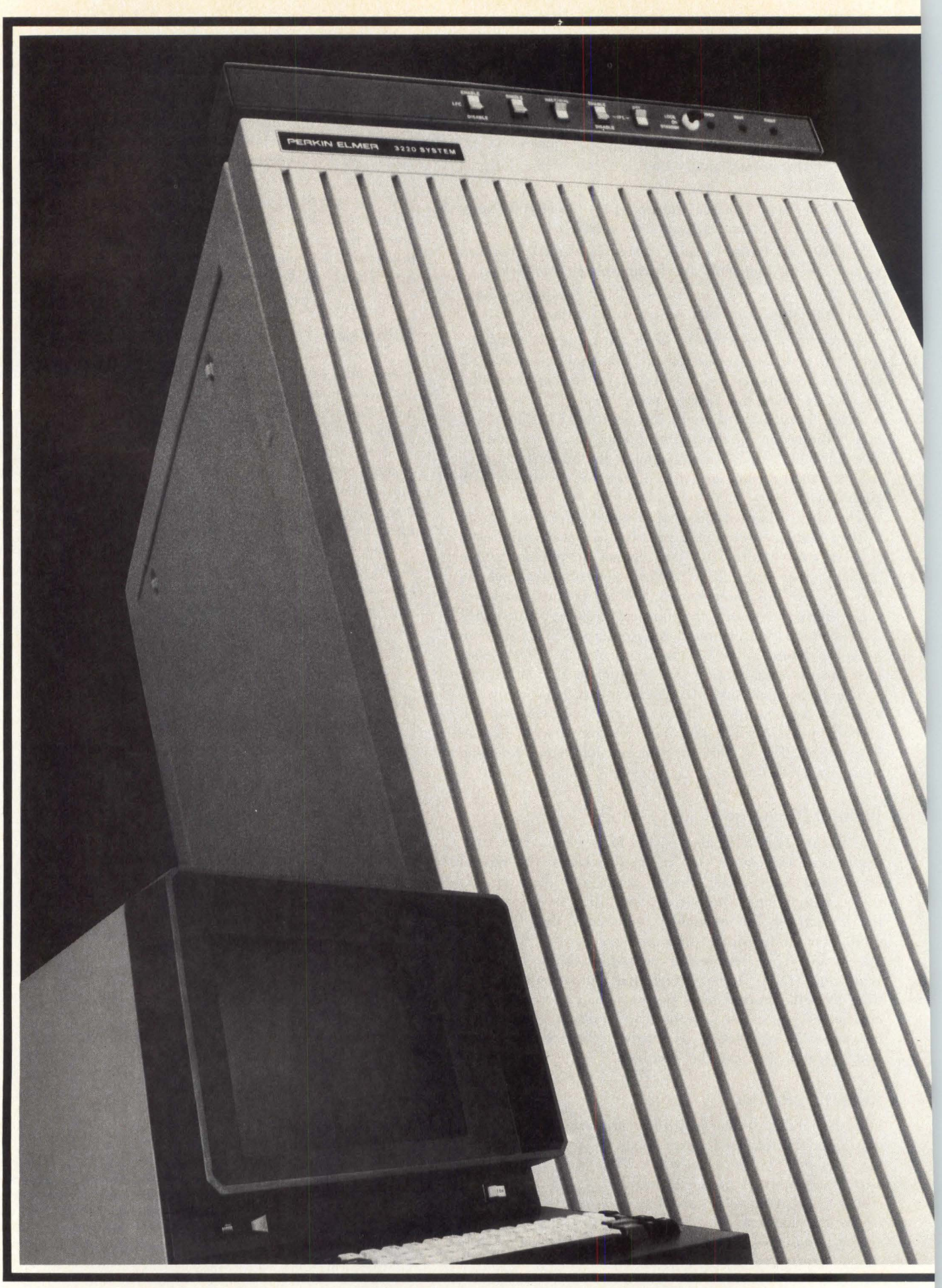


Joe E. Deavenport is a cofounder of Wavetek and has been an independent consultant for the last 17 years. His most recent work has been in the emi field related to the user environment of computers and peripherals. He has a BSEE from Texas Tech University.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DESIGN NOTE

Calculator Interface Circuit Drives Large External Display

Interconnecting large 15-digit, 7-segment readout display to a handheld calculator with a converter/driver circuit achieves increased visibility and readability

R. Alan Snyder Hewlett-Packard Company, Loveland, Colorado

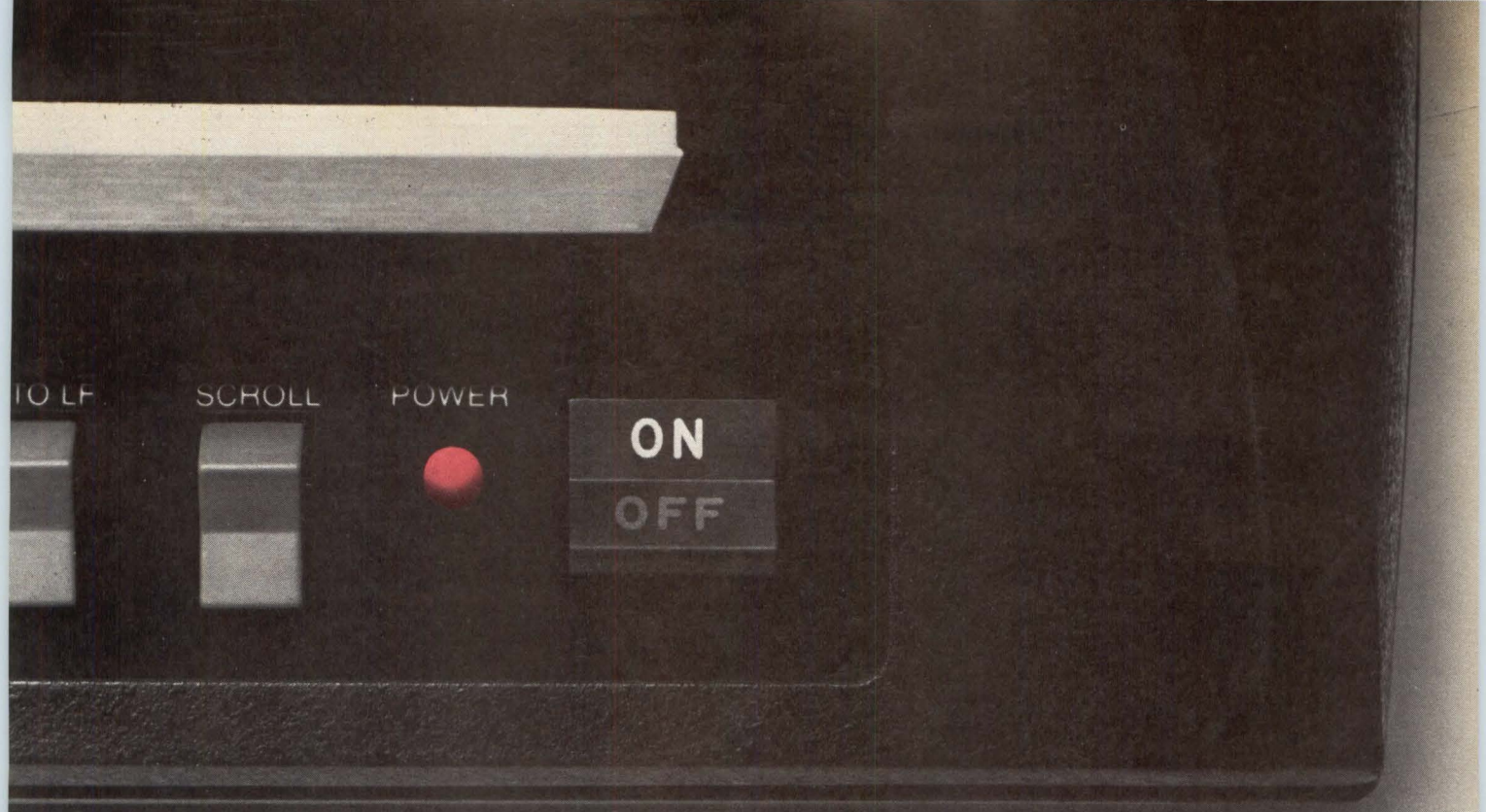
An external digital interface circuit, designed for several commercially available handheld and desktop calculators, connects the calculator to a large digit display device that enlarges readouts sufficiently to be legible at up to 40′ (12 m). The interface, designed specifically for HP. 35, -45, -46, -55, -65, -70, -80, and -81 calculators, features duplicate number of digits in display to preserve calculator accuracy and resolution; low power battery operation; small, single package containing both interface and display for portability; low parts count for reliability; minimum interference with calculator operation; and low cost. Examined are the calculator display timing and data formats, interface data acquisition and conversion methods, and interface driver and display techniques. Circuit alternatives are evaluated along with the rationale for the design selections.*

Interface Approach

The interface design approach for a large external display is governed heavily by the particular display device; no universal interface works with all displays. For this reason, the type of display must be chosen before the interface design can be started. For example, liquid crystal display (LCD) or light emitting diode (LED) displays need storage latches for each digit, but data can be off loaded rapidly from the calculator. Magnetic vane displays (MVD) do not need data storage latches, but data must be off loaded from the calculator comparatively slowly. Data decoding is independent of the display type, but how data are used after decoding is controlled by the display choice and the interface circuits.

Displays available for this application include incandescent bulbs or

*Motivation and some ideas for this design came from a calculator to Braille interface for blind students, which was designed by Dr Ruben D. Kelly of the University of New Mexico, and Dr David C. Koller of the Air Force Weapons Laboratory at Kirtland Air Force Base, New Mexico.



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LEDs that require high current power supplies, and vacuum discharge and neon-type displays requiring high voltages. LCDs offer low current and low voltage but are not yet available in sizes large enough for this application.

Light reflecting MVDs have been used in airport message boards, stock exchange monitor boards, and sports stadium displays. These displays consume power only when changing state, similar to complementary metal oxide semiconductor (CMOS) devices, require no power while resting, and have, in effect, inherent storage latches. The MVD is available in a standard 7-segment plus decimal point format. A 1.5″ (3.8-cm) high version is well-suited for this 15-digit application. Calculator output signals, MVD input signals, and required interface functions are listed in the Table.

HP Calculator Signals

	Calculator Output Signals			
Signal*	Pulse Width (μs)	Rate (kHz)	Interface Function	MVD Input Signal
A	24	**	A segment	$A_M = A \cdot clock \cdot \phi_1$
B	24†	**	B, G, DP	$B_M = B \cdot clock \cdot \phi_1$
C	48	**	C segment	$C_M = C \cdot clock \cdot \phi_1$
D	12 or 24**	**	D, E segment	$D_M = D \cdot clock \cdot \phi_1$
E	12 or 24**	**	F, G, DP	$E_M = D \cdot clock \cdot \phi_1$
ϕ_1	$\simeq$ 2	$\simeq$ 83	All segments	$F_M = E \cdot clock \cdot \phi_1$
ϕ_2	$\simeq$ 2	$\simeq$ 83	Not needed	$G_M = E \cdot clock \cdot \phi_1 \cdot B$
Clock	$\simeq$ 4	$\simeq$ 20.8	All segments	$D\ P_M = E \cdot clock \cdot \phi_1 \cdot B$
Start	$\simeq$ 10	$\simeq$ 5.5	Interface sync	

*Levels: 0 = 0.4 V; 1 = 3.5 V
**Depends on 7-segment number selected
†Except during decimal point (DP)

Calculator Display Data Format

HP calculators use a power saving technique to scan LED displays. A particular digit position is selected, and the required seven segments of the digit are selectively scanned one at a time so that not more than one LED segment is on at any given time. A custom integrated circuit (IC) extracts scanning sequence information from data in the listing. Timing analysis reveals that straight logic tables or Karnaugh reductions are not effective in decoding 7-segment data, due in part to the nonequal pulse widths of the various data lines, eg, clock ϕ_1, A. Since the MVD driver circuits need pulsed data for the 7-segment and decimal point lines, pulse width inequality is no problem.

Data Decoding

Clock pulses define the digit window that indicates the beginning of a digit scan period. The start line indicates when a full frame of 15 complete digit scans begins, with 15 clock pulses for every start pulse. This digit window is further divided by the ϕ_1 and ϕ_2 lines into four subwindows that contain the 7-segment number information, of which some is redundant for this interface design. The five data lines (A to E) roughly correlate to five of the 7-segment lines, with the remaining two lines (F and G) being decoded from the five data lines. The 7-segment lines plus the decimal point line are defined in terms of the A, B, C, D, E, ϕ_1, and clock lines at the calculator output.

This data coding technique results in pulsed data during ϕ_1 time and provides one pulsed segment per time window, except segment B, which unavoidably has two pulses per time window. The presence of the second pulse does not cause problems because data decoding formats are stored in a 2708 programmable read only memory (P/ROM).

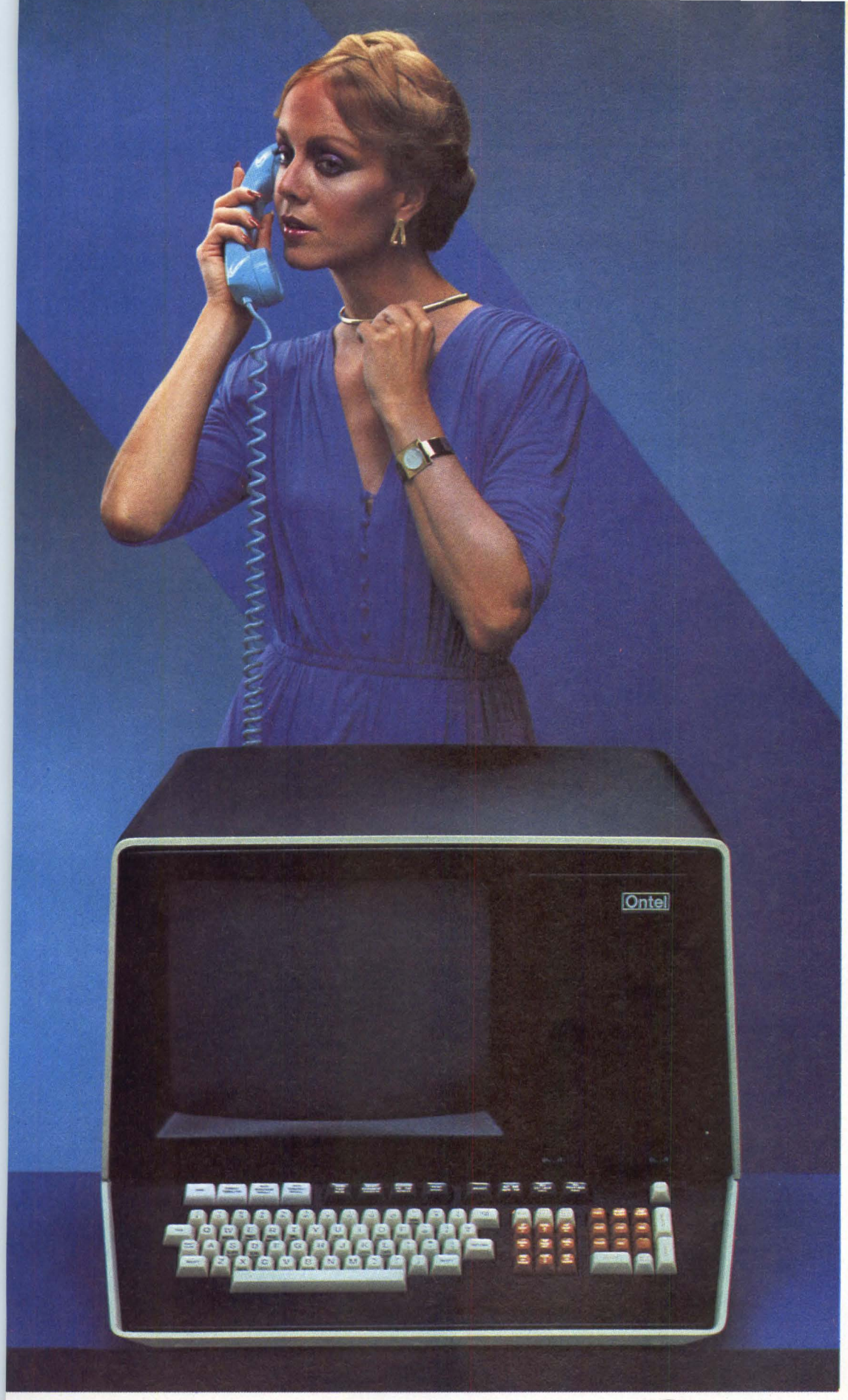
Look And Skip Scan

MVDs require special techniques in interfacing because of slow response times. The total time for one full scan cycle is approximately 1 ms. Display specifications state that 30 ms are needed to turn the display on or off. Consequently, a data stretching circuit is needed. A look and skip technique looks at a single digit frame (full 7-segment scan) and then lets several full frames go by before stopping at the next digit position. For example, the scanner looks at digit position 2 and then goes around n times before stopping at digit position 3 for the next look.

When the scanner stops at position 2, the digit information that has been decoded from the calculator for position 2 is loaded into a bank of 1-shot multivibrators. It then continues scanning and waits for these multivibrators to time out before stopping at the next digit position. In this manner, data are presented to the MVDs for sufficient time to set or reset them. Since the display set time is 30 ms and the scan cycle time is 1 ms, the scanner must go around 30 times before looking at the next digit position. Since there are 15 clock pulses per scan cycle, a divide by 450 counter counts the clock pulses and places the scanner at the same position in the display every scan cycle. To advance the counter one position, an extra count is added to move the scanner stop position one digit to the right every time it stops. Therefore, the resulting divide by 451 counter strobes data into the MVDs and progresses sequentially from digit to digit.

Output Position Counter

The output position counter (OPC) synchronizes the interface and determines which MVD digit will receive data available in the P/ROM code



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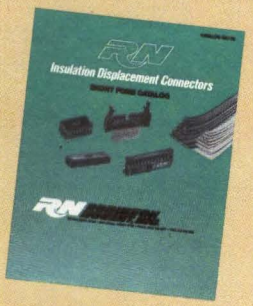

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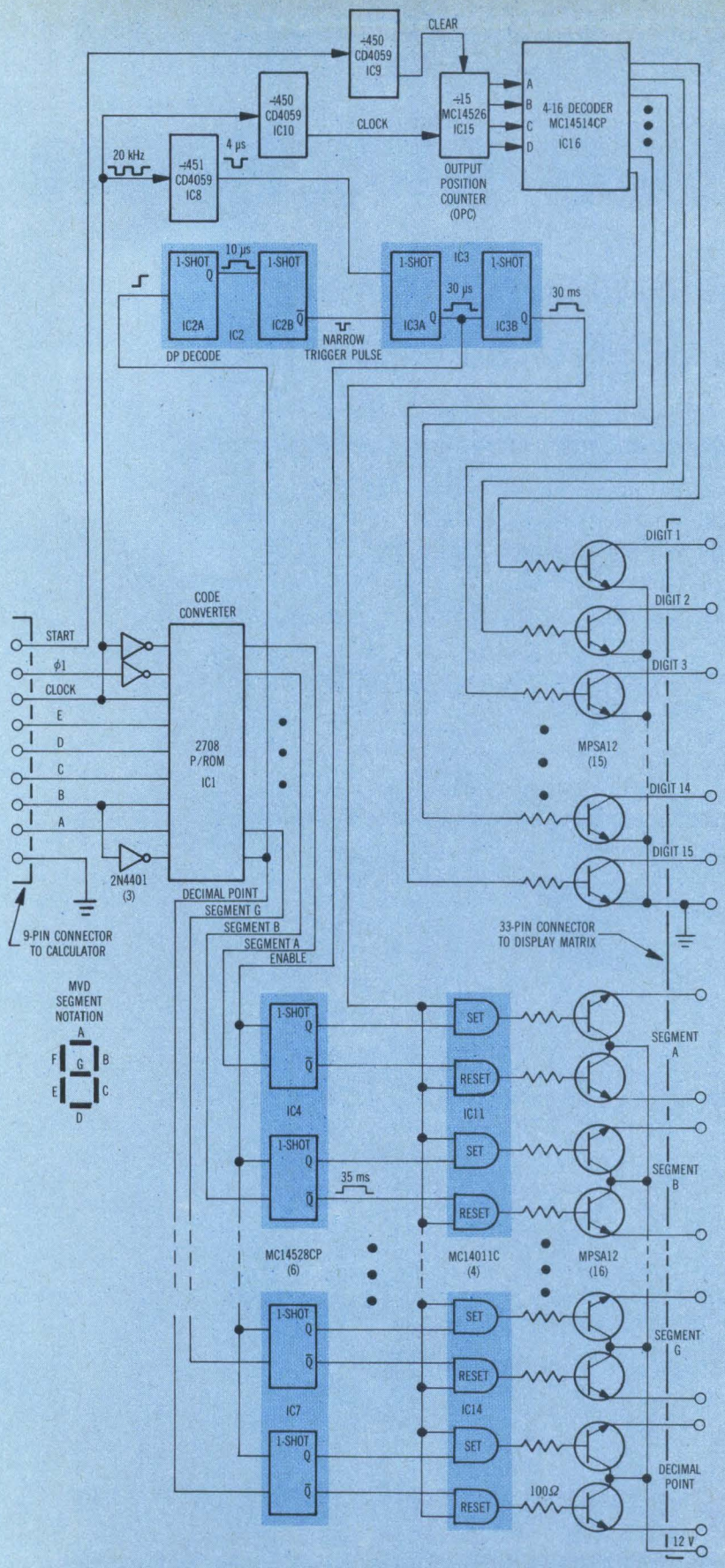


Fig 1 Converter circuit. Converter interfaces handheld calculator to large readout display. Signals from calculator are decoded in 2708 P/ROM. 1-shots compensate for magnetic vane display's slow response time

converter (Fig 1). Only one digit at a time is enabled, so that the data from the calculator can be latched into the display interface. The OPC—a programmable divide by n counter (MC14526CP)—is programmed to divide by 15; it is reset to binary 14 (1110) every 450 transitions of the calculator start line. In the event that the state of the counter does not match the position of the calculator scan, either at power on or due to a glitch, the interface needs only to wait at most 450 start cycles (500 ms) before the output display and the calculator display become resynchronized. Since the divide by 15 counter divides down, the outputs of the decoder must be reordered. Also, because the calculator scans its digits from 15 to 1, the 4- to 16-line decoder (MC14515CP) outputs must drive the MVD digits as shown.

Calculator Digit	OPC Output	Decoder Pin
1	14	16
15	13	11
14	12	9
13	11	10
12	10	8
11	9	7
10	8	6
9	7	5
8	6	4
7	5	18
6	4	17
5	3	20
4	2	19
3	1	14
2	0	13

1-Shot Display Predrivers

Twelve 1-shot circuits (IC2 to IC7) serve three separate functions. They accept look and skip data from a divide by 451 counter (IC8) and gate on all 1-shot circuits except IC1A and B; generate 30-ms set and reset signals to drive MVD drivers; and monitor shortened decimal point window and reset 1-shot circuits appropriately.

One-shot ICA, set for a pulse width of 30 µs, triggers at every 451 transitions of the clock line. Triggered output (Q) is connected to the enable input of 1-shots IC4 to IC7. As long as IC3A remains untriggered, IC4 to IC7 are disabled and will not respond to data that are constantly available at the P/ROM decoder (IC1) output. When IC3A triggers, IC4 to IC7 are

enabled for 30 μs, allowing the 7-segment data for one digit to be set into them. The Q and $\overline{Q}$ outputs from IC4 to IC7 are connected to two set and reset AND gates (IC11 to IC14), respectively, which connect to the MVD driver transistors (MPSA12). The IC3B 1-shot triggers on the falling edge of the IC3A output. The Q output from IC3B, set for the 30-ms required by the MVDs, drives all the set and reset AND gates.

The IC3B and IC4 to IC7 1-shots are triggered essentially simultaneously (30 μs apart). The IC3B is triggered for 30 ms, and IC4 to IC7 are preset for 35 ms. Therefore, the true data outputs of the AND gates can last for the full 30 ms. The extra 5 ms of IC4 to IC7 guard against false data from appearing at the AND gate outputs in the event that an IC4 to IC7 times out early.

The IC2 1-shot pair only activates during decimal point display time. The time window for decimal point data is approximately 12 μs wide, thus IC4 to IC7 must not be enabled for more time than the decimal point requires. Otherwise, data from the next digit time window may overflow and cause erroneous information. To prevent this, the IC2 pair is triggered whenever the decimal point signal from the P/ROM is present. Output from the IC2 pair normally allows the Enable input of IC3A to remain active. However, when the IC2 pair is triggered, IC3A is reset after only 10 μs and is not allowed to continue timing out for the full 30 μs, thereby preventing IC4 to IC7 1-shots from getting false data.

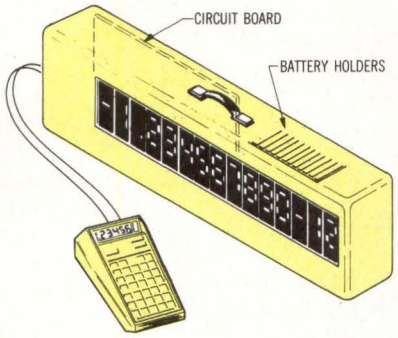


Fig 2 Display system. All electronics are contained within 20 x 3 x 6″ (51 x 7.6 x 15.2-cm) formed plastic case. CMOS circuitry and magnetic vane displays insure portability. Interface to calculator is via 9-pin connectors and cable

Magnetic Display Drivers

MVDs have two solenoids per segment. The 1.5″ (3.8-cm) high segmented displays are typically visible up to 40′ (12 m), require a 30-ms wide 30-mA pulse at 12 Vdc, and consume no power while inactive. Each segment has three control wires—set, reset, and common.

Segment driver transistor pairs (MPSA12) are driven by AND gates from the IC4 to IC7 1-shot circuits, with only the SET or RESET line pulsed since they connect to the Q and $\overline{Q}$ outputs, respectively. All eight segments (segments A to G and decimal point) for a given digit have their common lines connected and are, in turn, driven by an associated digit driver pair. For example, all IC3A segment set and reset solenoid wires for all 15 digits are respectively connected together.

Summary

The final large digit display design (Fig 2) provides increased calculator readout and visibility. A critical design problem—power consumption—is overcome with an extremely low power consuming battery type display and extensive use of CMOS ICs. Because of careful design, calculator interface connections require the addition of only a single 9-pin connector. The high cost of a P/ROM decoder can be significantly reduced by using a custom designed code converter IC. The final interface design results in a lightweight, portable, and battery operated readout device. This device can be easily modified to accommodate magnetic vane displays of up to 12″ (30 cm) in height by retiming all circuits to compensate for slower set and reset pulse requirements.

For full design information, contact R. Alan Snyder, Hewlett-Packard, Loveland Instrument Div, PO Box 301A, Loveland, CO 80537.

TECH NOTE

Drive Mechanism Design Reduces Errors in Mini-Floppies

A mini-floppy disc drive design increases track and flux densities, and ensures error-free operation even under worst case temperature, humidity, and diskette interchange conditions

Dennis Resnik Micropolis Corporation, Canoga Park, California

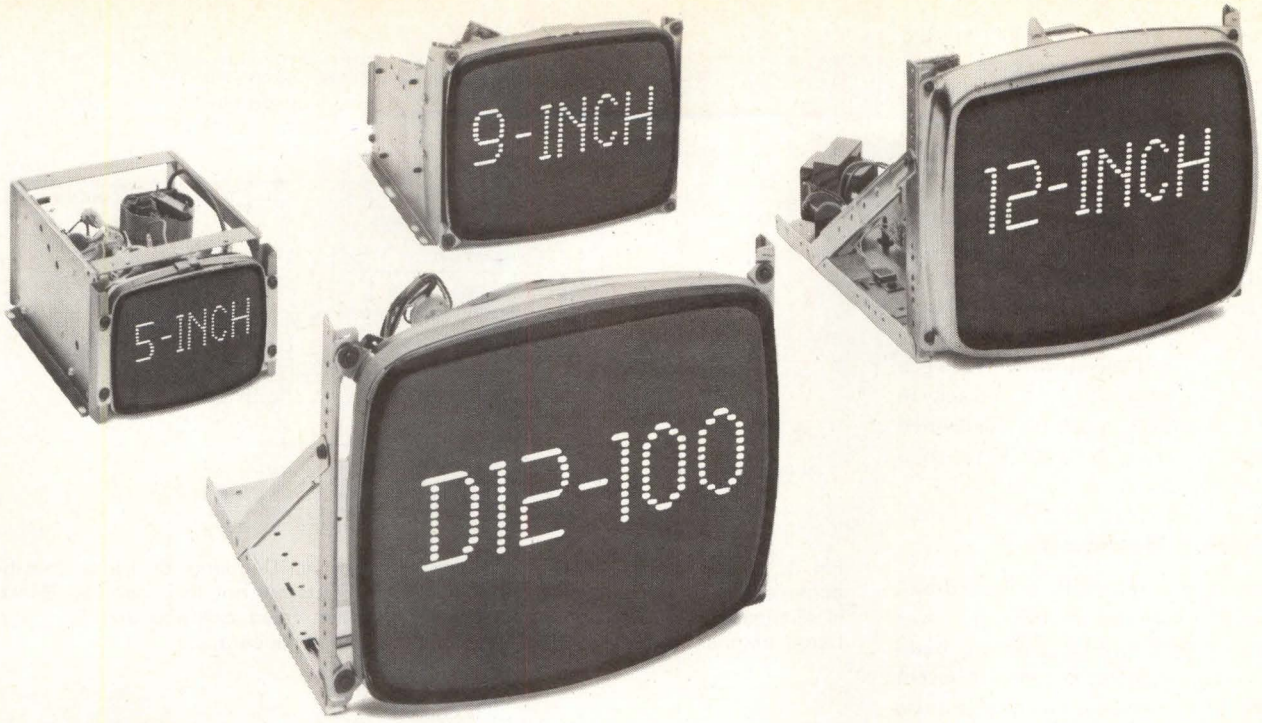
Standard mini-floppy diskette drives offer a maximum, unformatted data capacity of 110k bytes. A high capacity drive has been developed that provides 480k bytes, unformatted, for single-sided and 946k bytes for double-sided recording. The drive mechanism incorporates modified frequency modulation encoding for increased bit density, and 100-track/in (39/cm) recording for increased track density. Modified frequency modulation doubles the nominal capacity of 110k bytes. The increase from 35 to 77 nominal track yields $77/35 \times 220 = 480$k bytes.

The ability to record and read data reliably at double-bit density is achieved by using a high resolution recording head, excellent track positioning accuracy, careful read/write (R/W) circuit design, optimum selection of write current and read-gain bandwidth, and a phase lock loop data separator for decoding. "Encoding/Decoding Techniques Double Floppy Disc Capacity"* details the differences between modified frequency modulation (MFM) encoding and various other schemes. By reducing the data cell transition time from the 8 μs required for standard frequency modulation (FM) encoding to 4 μs, MFM doubles the number of cells per track without increasing the total number of flux transitions on the diskette. This technology maintains a data error rate of less than 1 error in 10^9 bits.

Increasing track density from the standard 48 tracks/in (19/cm) to 100 tracks/in (39/cm) relies almost entirely on the ability to maintain head to track alignment over the required operating temperature and humidity ranges, permitting diskette interchange between drives. Because materials used in drives have various coefficients of expansion and the diskette expands and contracts with changes in humidity as well as temperature, fluctuations in either temperature or humidity will create positioning inaccuracies.

A typical 48-track/in drive may have a total head positioning inaccuracy of $\pm 0.004''$ (± 0.102 mm). When reading a track, the R/W head

*J. Hoeppner and L. Wall, "Encoding/Decoding Techniques Double Floppy Disc Capacity," *Computer Design*, Feb 80, pp 127-135



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could be as much as 0.008″ (0.203 mm) off the written track position. With 0.021″ (0.533-mm) track to track spacing, 38% error is possible. Satisfactory performance can be achieved with up to 50% offtrack error in an MFM system. If this same drive is modified for 100-track/in operation by changing the head design and making the positioner turn about half as far, the ±0.004″ error would approach the distance between tracks. To achieve a 100-track/in design, the head must be positioned at least twice as accurately as in a 48-track/in drive.

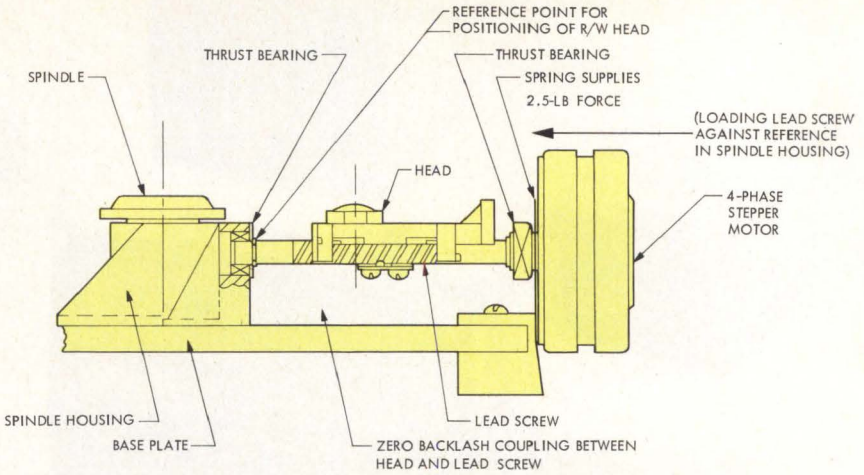

Fig 1 Precision positioner for 100-track/in drive. Doubling of track density is achieved by referencing R/W head to spindle housing, not to baseplate. Backlash is eliminated by using load ball coupler between head carriage and lead screw. Large angular movement of stepper also reduces inaccuracies

Positioning Mechanism

A steel lead screw with a loaded-ball follower combination (Fig 1) was chosen over a plastic cam or band positioner because of its inherent accuracy. The chosen mechanism also leads to a unique head referencing method. A 7.5°, 4-phase, permanent magnet stepper motor using four sections of stamped-cup type stator elements is coupled to a precision-ground lead screw with 8.33 threads/in (3.28/cm) pitch to yield a rotary to linear motion conversion ratio of 30° = 0.010″ (0.254 mm). Four 7.5° steps move the head from one track to another. While some track to track access speed is sacrificed, a significant improvement in overall accuracy is achieved by making 4 steps/track with a 4-phase stepper motor: the same stator pole is always referenced, and the drive electronics supply the required timing. The lead screw is coupled, in turn, to the head carriage using a leaf-spring loaded ball. Since the ball diameter contacts both lead screw side walls, ball and screw wear does not contribute to loss of positioning accuracy.

The motor has a nonaccumulative error of ±0.5°. Since 30° lead screw rotation yields a linear motion of 0.010″, a maximum track position error of 167 μin (4.24 μm) is expected. In practice, experiments have shown that ±0.25° accuracy is easily achieved. This leads to a motor positioner accuracy of ±83 μin (±2.11 μm).

Inherent friction is used to damp the oscillating motion of the positioning system. This leads to a dead-band angle, due to hysteresis, which depends on the maximum friction (T_θ) and the torque/angle stiffness (T_F) of the stepper motor. After a step, the motor may stop anywhere within the dead band, $\pm\theta$. In practice, θ = ±1.05°, which yields a hysteresis effect positional error, due to friction, of ±350 μin (±8.89 μm).

Temperature And Humidity Compensation

The head positioner accurately locates the head over the correct track under static conditions. Without any operational temperature and humidity compensation, expansion and contraction of both the Mylar diskette and the chassis or casting cause a worst-case misalignment of several thousandths of an inch. If the head is referenced via a cam, band, or lead screw to the positioner, which, in turn, is referenced to the chassis, the chassis will expand as temperature rises and move the head away from the spindle. Mylar has an expansion coefficient of 9.4 μin/in/°F. Over a temperature range of 50 °F (10 °C), this effects an expansion differential of 900 μin (22.8 μm) on a track at the center of the positioner stroke with no temperature compensation.

In Fig 1, the lead screw is preloaded with a force of 2.5 lb (11.1 N) against a thrust bearing, located in the spindle housing, by a flexure spring attached to the stepper motor case. This flexure provides degrees of freedom that preclude the need for accurate alignment of the motor body to the baseplate. Thus, the temperature compensation loop includes the diskette, lead screw, and spindle housing. It excludes the baseplate, and stepper-to-base and spindle-to-base mountings from the head positioner mechanism. Expansion of the baseplate results only in a change of preload.

Since the diskette and the lead screw are both referenced to the spindle housing, thermal expansions of the media, lead screw, and spindle housing occur in the same direction. Spindle housing material is selected so that when the head is positioned at reference track 36, the coefficient of expansion for the head, lead screw, and spindle housing matches that of the media. Worst case misalignment due to thermal factors (tracks 0 and 76) is less than 200 μin (5.08 μm).

Humidity, or hygroscopic expansion, is not compensated in the drive design. Floppy diskettes suffer from a dimensional stability problem because of Mylar's 6-μin/in/% relative humidity hygroscopic expansion coefficient. Error due to this hygroscopic effect can be ±350 μin (88.9 μm). Practical results of diskettes are significantly better than the design values for ordinary Mylar (see the

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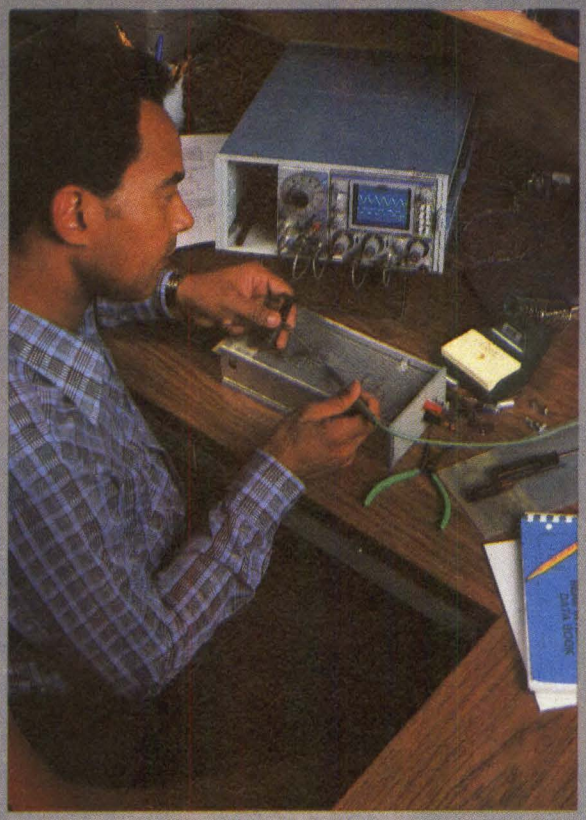

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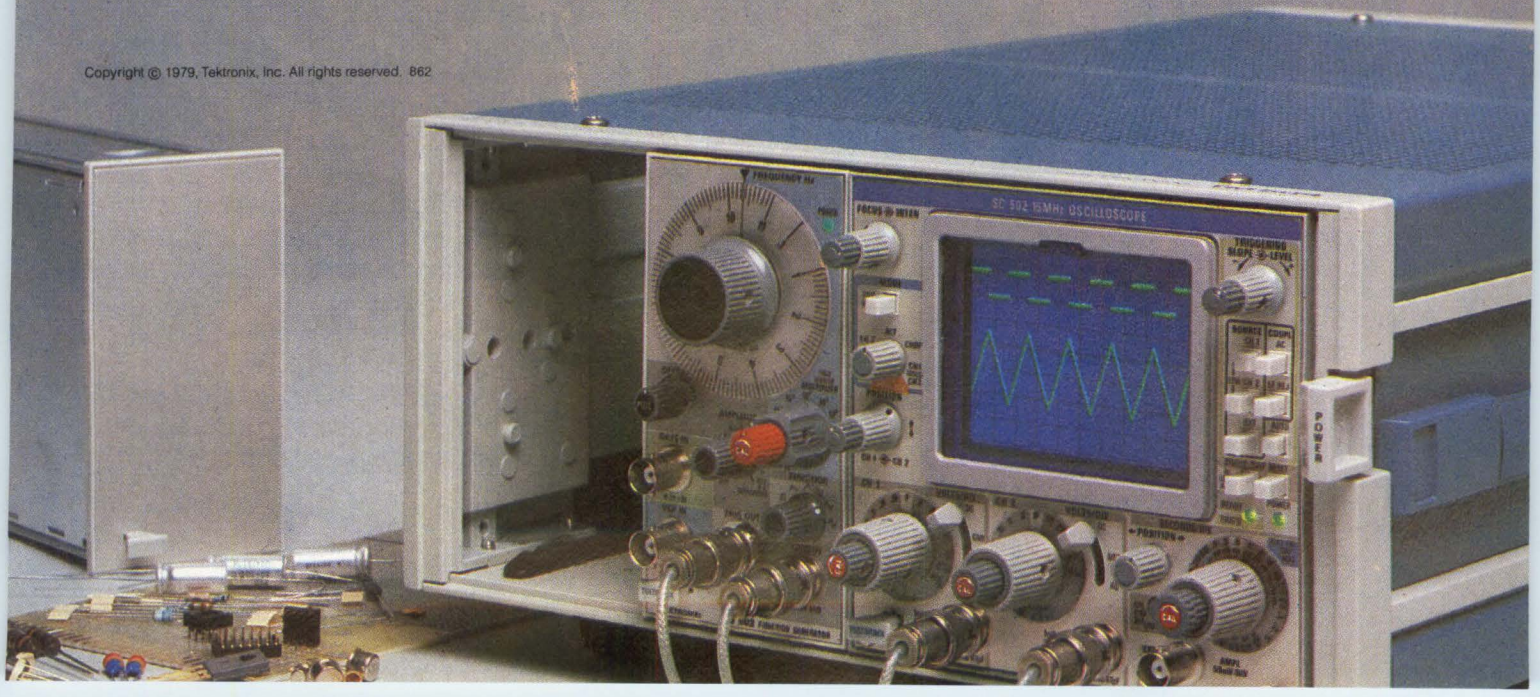

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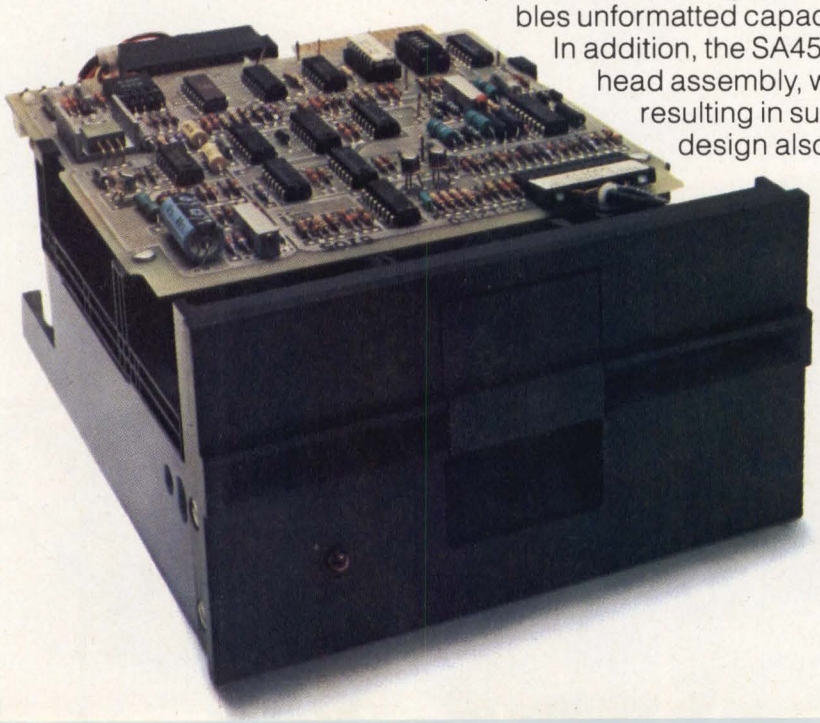

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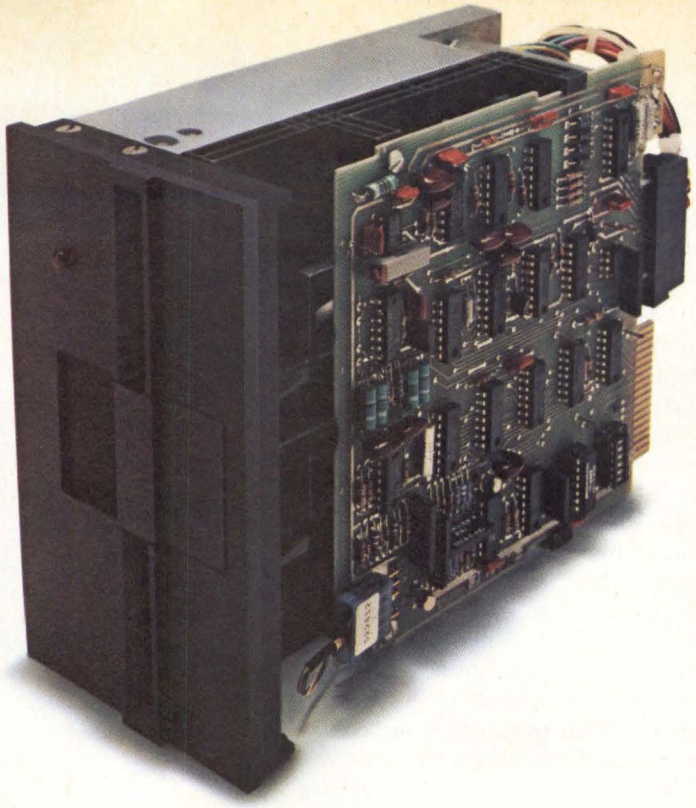

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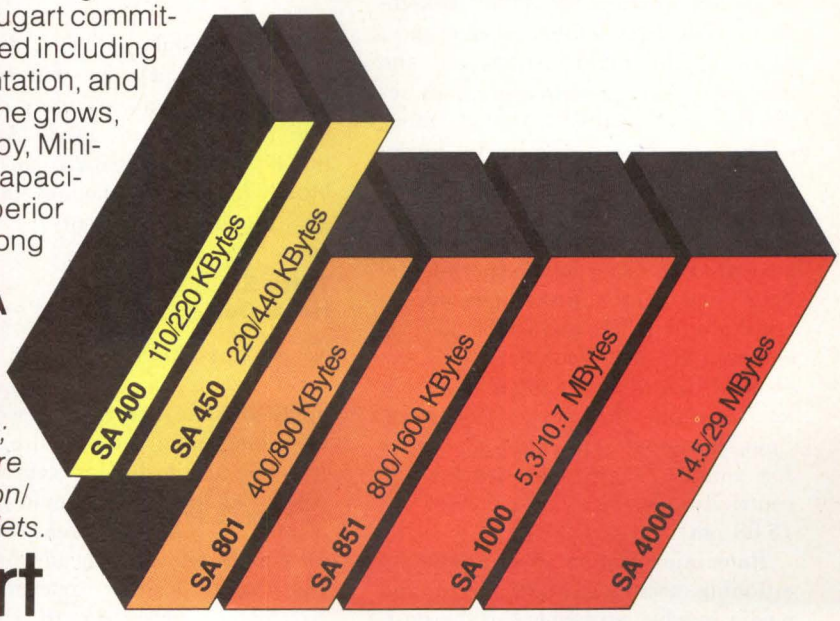

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Table) due to the stabilizing influence of the oxide recording surface.

Other Design Factors

The positioner design locates the head accurately, even under dynamic conditions imposed by temperature and humidity variations, diskette interchange, and shipment. It is also important to ensure that the diskette is accurately registered with respect to the spindle. Centering schemes that use a hub may miscenter a diskette with a maximum tolerance hole diameter by as much as 0.002″ (0.051 mm). After writing and then interchanging or reclamping the diskette, the track appears to revolve eccentrically under the head. This misalignment over part of the track is equivalent to positioning mechanism inaccuracy.

Drive design eliminates registration error as follows. After the diskette is inserted, the receiver and clamp are lowered so that the diskette center hole engages with the profiled hub on the spindle shaft, centering the diskette. Spindle rotation assists centering action as the clamp is lowered. Once the clamp is in position, a spring provides 3 to 5 lb (13 to 22 N) of clamping force. The central part of the clamp registers with a projection on the drive shaft, so that the clamp is concentric with the hub, and neither rotates relative to the other.

Hub dimensions provide a line to line fit when the hub diameter is at minimum tolerance and the diskette center hole is at maximum tolerance. Thus, at the other extreme of the tolerances, an interference fit of approximately 0.0025″ (0.063 mm) exists. This fit is taken up by movement of the diskette. The spindle contour allows for a large-radius bend in the Mylar, preventing permanent diskette distortion. Experimental data show that a diskette centering accuracy of ±250 μin (±6.3 μm) is achieved by the combination of the profiled hub, the hub rotation during loading, and the design tolerance. Spindle runout—the total allowance for spindle, shaft, and bearing eccentricity—is less than 200 μin (5.08 μm).

Remaining factors affecting the positioning accuracy of the head and media involve adjustment of the positioner, or radial alignment. An eccentric lobe or cat's eye pattern alignment disc with an accuracy of ±200 μin (5.08 μm) is used. An additional ±100 μin (0.25 μm) is allowed for human factors that may arise during adjustment.

Head-Media Positioning Errors

Contributing Error Factors	Design Goals (μin)	Practical Results (μin)
Positioning Mechanism		
Motor Accuracy	±83	±83
Hysteresis Effects Due to Friction	±350	±250
Lead-Screw Accuracy	±35	±35
Temperature Effects	±200	±250
Hygroscopic Effects	±350	±200
Disc Run-Out		
Disc Centering Accuracy	±250	±250
Spindle Run-Out	±200	±150
Alignment Accuracy		
Standard Disc Accuracy	±200	±200
Human Factors	±100	±100
Total	±1768	±1518

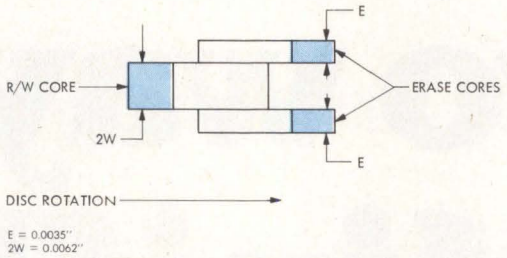

Fig 2 Tunnel erase head configuration. Widths of R/W gap (2W) and of erase gaps (E) must be carefully chosen to maximize offtrack performance

Total Error Affects Head Design

While it is highly unlikely that all error factors would simultaneously apply in one direction, a worst-case combination of temperature, humidity, alignment disc inaccuracy, and positioner inaccuracy would place the head 1768 μin (44.9 μm) off track. Maximum allowable head offset from true track position determines the parameters necessary to specify a head design for 100-track/in operation. Floppy disc systems use magnetic heads consisting of a R/W element together with two erase elements on either side. Two implementations of such a head are the tunnel and straddle erase systems. Although harder to implement because of the additional erase timing circuits required, the tunnel erase method has been chosen because of its superior data performance.

Fig 2 shows a R/W core of width 2W with two tunnel erase cores, one on each side, each of width E. The erase gaps ensure clean guard bands between tracks so that, when the head is reading an offtrack location, it does not pick up portions of previously recorded information. Fig 3

FOR DATA ENTRY . . .

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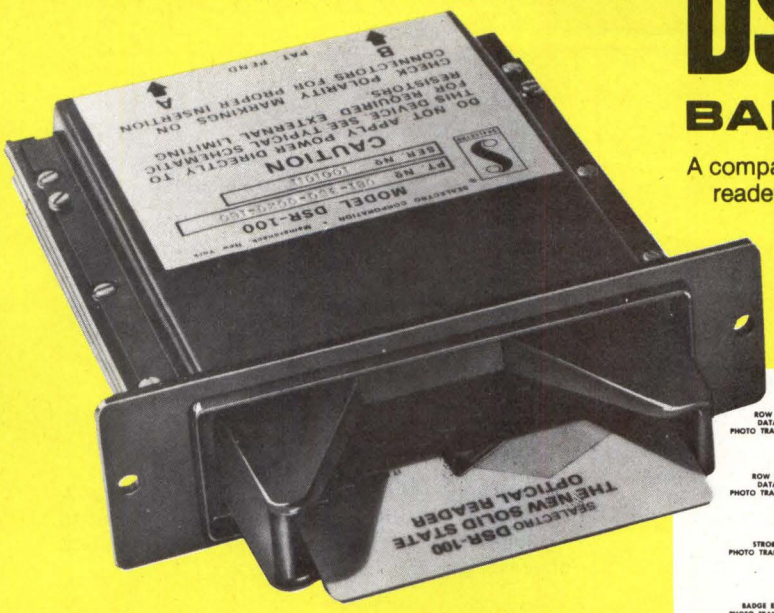

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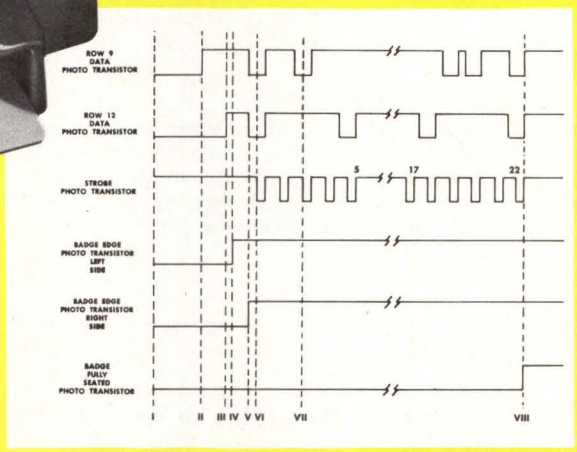

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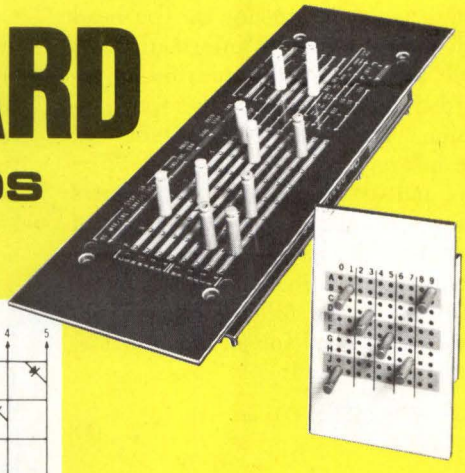

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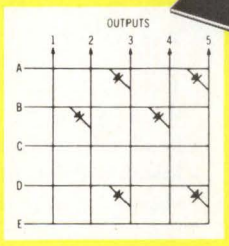

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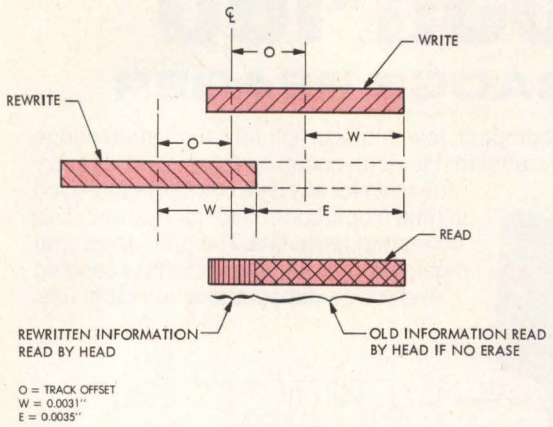

Fig 3 Track overwrite situation. When track is rewritten, even small head mispositioning will result in some old data remaining on disc. In MFM or FM reading, small residual signal may cause errors. Tunnel or straddle erase eliminates old data

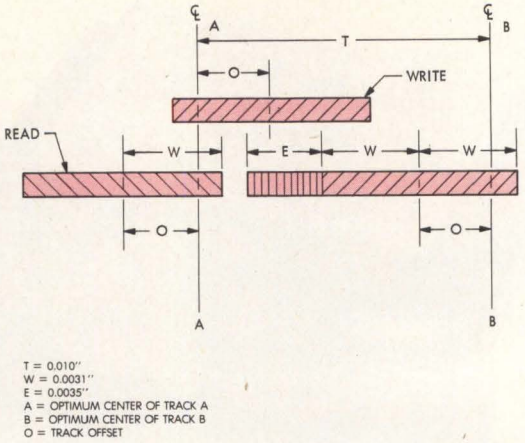

Fig 4 Adjacent track situation. With track A written offset to left and track B written offset to right, track A will be reduced in width by effect of erase gap E

depicts a track written with the head offset to the right by an offset of O, new information written with the head offset to the left by offset O without the erase head energized, and an attempt to read the new information with the head offset to the right, again by amount O. The head will read the correct information, as well as part of the previously recorded information, at the track location. The relative amplitudes of the information are: NEW = 2(W − O) and OLD = 2(O). In typical cases, without erase, the ratio of NEW/OLD approaches 1, making data recovery impossible.

In Fig 3, the following inequality must be satisfied for all old information to be erased:

$$E \geq 2W - 2(W - O), \text{ or}$$
$$E \geq 2(O) \qquad (1)$$

The width of the erase gaps must equal or exceed twice the worst-case offset. The amount of track that can be read in the worst case is 2(W − O). Two conclusions can be drawn: the greater the erase core width, E, the more offset can be tolerated; and the greater the offset, and therefore E, the less track width remains in the worst case. Since the remaining track width is 2(W − O), this condition would appear to require increased R/W width; however, other limitations apply.

Fig 4 depicts track A written with an offset to the right. When the head is reading track A with an offset to the left, the amount of track being read is 2(W − O). Suppose that track B is written with an offset to the left of its true position. Then, the erase head will erase some of track A. To prevent the erase head from reducing the amount of track A to less than 2(W − O) available for reading at any position of the read head, the following inequality must be satisfied:

$$T - (W + O + E) \geq W - O, \text{ or}$$
$$T \geq 2W + E \qquad (2)$$

Track spacing must equal or exceed the R/W gap plus the erase gap. Thus, head design essentially trades off allowable track offset for reduction in signal amplitude. The final, 100-track/in (39/cm) head design has a R/W core width of 0.00625″ (0.16 mm), and erase core width of 0.0035″ (0.089 mm). Fringing effects yield an effective erase core width of 0.00355″ (0.0902 mm).

Substituting these values into Eq (1) shows that

$E \geq 2(O) = 3550\ \mu\text{in}\ (90.2\ \mu\text{m})$, and
$O \geq 1775\ \mu\text{in}\ (45.1\ \mu\text{m})$

This is consistent with the design goal offtrack error value. Also, by substitution into Eq (2), $T \geq 0.0098''$ (0.249 mm). Since $T = 0.010''$ (0.254 mm), the inequality is satisfied. Remaining worst-case track width is $2W - E = 0.00625'' - 0.00355''$ or 0.0027″ (0.686 mm), and percent signal remaining is 0.0027 ÷ 0.00625 or 43.2%. This signal reduction is well within the dynamic range capabilities of the read electronics.

As listed in the Table, the worst-case head mispositioning, or offset, does not exceed 1768 μin (44.9 μm), and the read amplitude always exceeds 43.2% of optimum (with the head directly over the track). Therefore, error-free performance is assured, even under worst-case temperature, humidity, and diskette interchange situations.

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"1015 Flexible Disk Drive Engineering Specification," Document #100112, Micropolis Corp, Canoga Park, Calif, June 1978

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TECH BRIEF

Fast Differential Analog to Digital Conversion

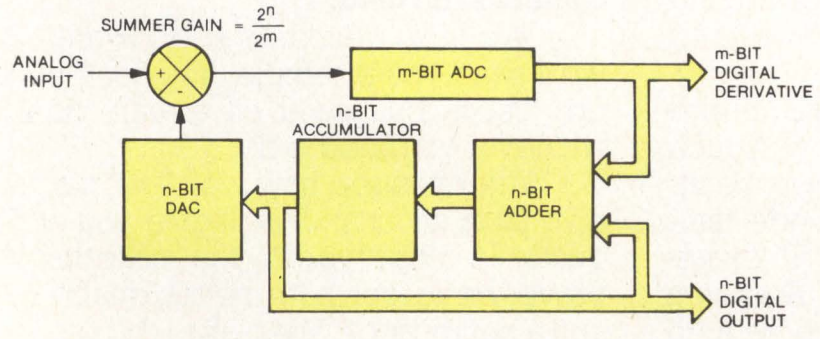
Tracking converters and successive approximations are combined in a differential A-D converter

Successive approximation converters are almost universally used for high speed analog to digital conversion. However, for high accuracy, in the order of 12 to 16 bits, conversion times increase by approximately 2^n, where n is the number of bits. Another comparison must be made for each additional bit, and the settling time is approximately doubled for each doubling of accuracy (bit).

The differential conversion technique shown in the figure is a hybrid achieved by combining tracking converters and successive approximation techniques. Analog to digital (A-D) conversion is performed on the difference between the present input signal and the last converted value, which has been stored in the accumulator. This digitized difference signal is added to the previous digitized value to attain the new value representing the digitized analog input.

Since the A-D converter used in this technique digitizes only the difference signal, it performs significantly faster than a converter required to digitize the complete answer. After the difference is digitized, it is added to the previous stored value, and the converter must be allowed to settle before another conversion cycle is started. Conversion time is one settling of the n-bit digital to analog (D-A) conversion, m bits of the A-D conversion, and the add time, which totals less than n settlings of the n-bit D-A conversion normally required.

Accuracy is limited primarily by the D-A converter. Offset and gain errors in the A-D conversion should be less than 1 bit, which is easily attained. The converter cannot handle rapidly changing inputs because it is slew limited; however, it will recover input transients without overshoot or extra settling time. Additionally, the output of the m-bit A-D converter is useful as a digital derivative of the input signal.



Differential A-D converter digitizes difference between input and previous conversion (stored in accumulator) and adds difference to previous digitized value, yielding new digital representation of analog input

Note

This work was done by Arthur G. Birchenough and William J. Rice of Lewis Research Center, 21000 Brookpark Rd, Cleveland, OH 44135. No further documentation is available (LEW-12909).

Computer Interface for Mechanical Arm

Man/machine interface simplifies operation of computer controlled mechanical arm

A computer controlled mechanical arm has six degrees of freedom and is directed through a supervisory control mode, in which all motions of the arm follow a set of preprogrammed sequences. The program is stored beforehand in a computer.

The entire set of arm movements is monitored and controlled by the operator behind the interface panel. The interface panel includes a television screen that displays the arm movements; a cathode ray tube that displays, in simple language, the exchange being accomplished, the activity being conducted, and the action required of the operator; and a set of keys to punch in the next sequence of movements.

For simplicity, only a few prescribed commands are required to accomplish the entire operation. The interface panel controls can be mastered quickly—recent tests have shown that, on the average, it takes only 10 min of training to learn the entire operation. System safety is thus improved because the operator needs no complicated checklists or procedures to follow.

This type of an interface can operate a computer controlled arm to handle radioactive or explosive materials, or command an arm to perform functions in hostile environments.

Note

This work was done by W. L. DeRocher and R. O. Zermuehlen of Martin Marietta Corp for Marshall Space Flight Center. For further information, write to: Aubrey D. Smith, Code AT01, Marshall Space Flight Center, AL 35812.

Patent Status

Inquiries concerning rights for the commercial use of this invention should be addressed to the Patent Counsel, Leon D. Wofford, Jr, Mail Code: CC01, Marshall Space Flight Center, AL 35812. Refer to MFS-23849.

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

INTERFACING FUNDAMENTALS: FLOWCHARTS, STRUCTURE CHARTS, AND WRITTEN STATEMENT PROGRAMMING NOTATIONS

Peter R. Rony
Virginia Polytechnic Institute and State University
Blacksburg, Virginia

Conditional and unconditional input/output techniques were introduced in last month's column, accompanied by discussions of handshake cycles, strobed input/output, flags, semaphores, and interlocking. Block diagrams illustrated the input/output techniques, providing an idea of how a microcomputer and an input/output device can be interlocked, as well as what role a semaphore plays in this interlocking process. This month's column, as a prelude to subsequent ones, compares flowcharts, structure charts, and the written statement form of describing microcomputer algorithms. The approach followed is patterned after the Swiss article by Baumann.[1]

Structured programming is a set of conventions and rules that yield programs which are easy to write, test, modify, and read.[2] Turner defines top-down structured programming as a method for solving a given problem or implementing a given definition in which the problem or definition is more specifically refined at each step of the procedure until a final step of refinement results in executable code. The same limited set of syntactic structures is used at every stage of the problem's refinement.[3] Refs 2 through 4 discuss structured programming in the context of microcomputers. The basic approach was first proposed by Dijkstra;[5,6] another useful reference is the book by Yourdon.[7]

This widespread technique, discussed and employed in most recent computer science texts, is still not commonly taught to engineers and scientists who usually learn either FORTRAN or BASIC. Due to space limitations, these common "structures"—the basic building blocks of structured programming—will only be summarized.

The first structure, the sequence block, is a single instruction or computational statement, or any sequence of computational statements, with only one entry and one exit. Fig 1 depicts a pair of sequence blocks. The first computational

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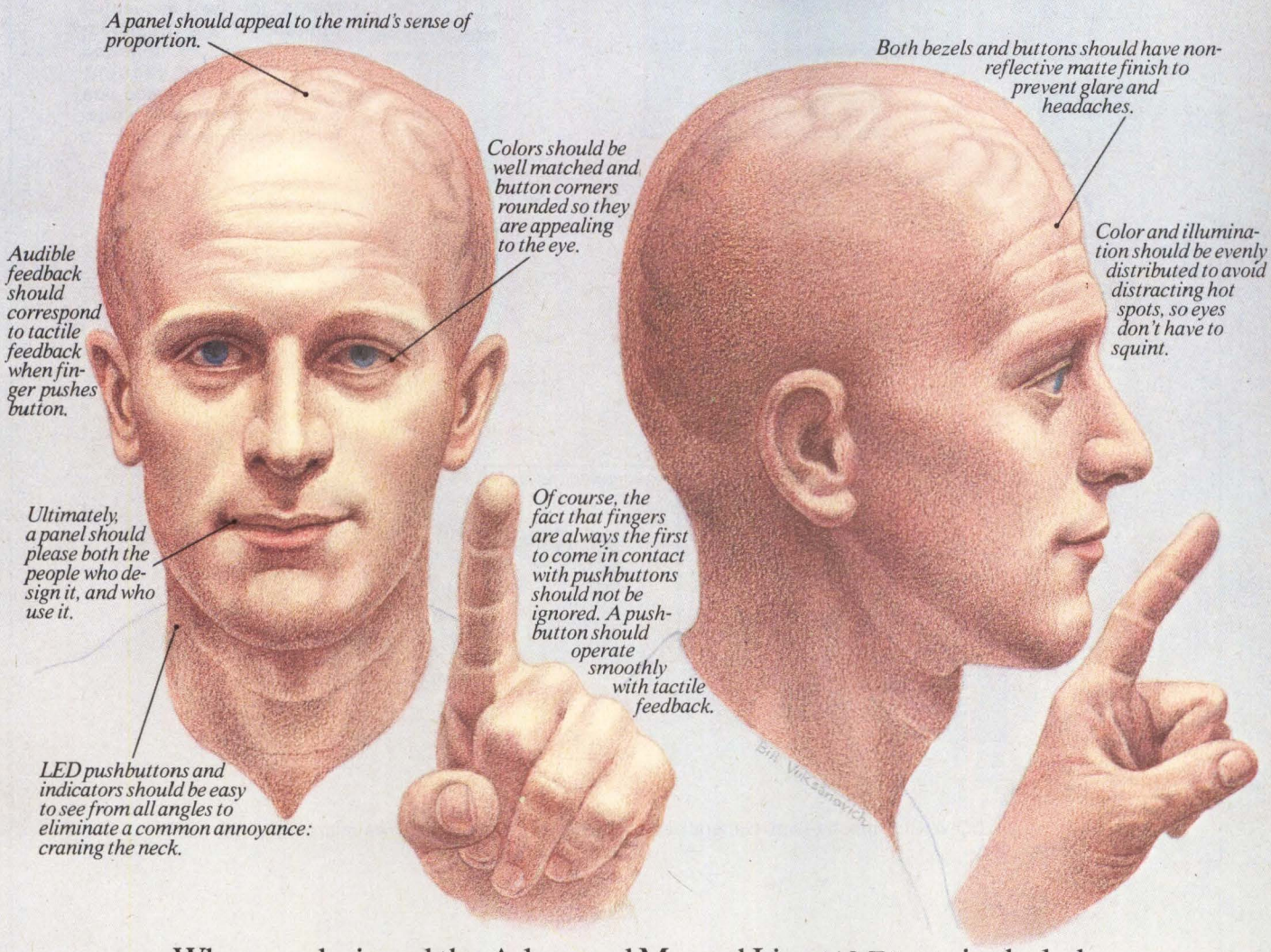

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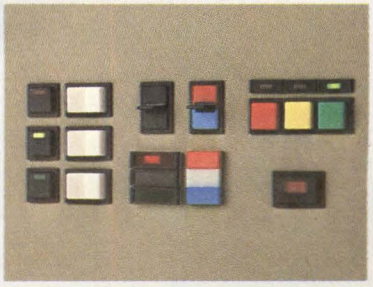

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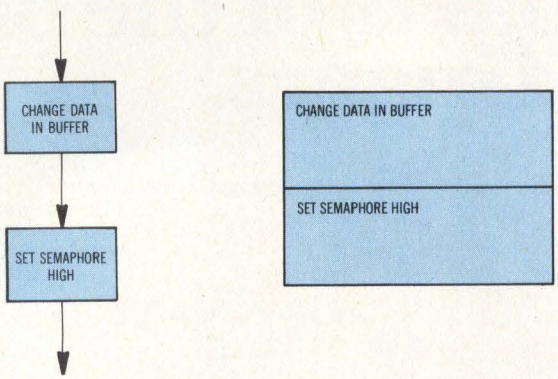

Fig 1 Pair of sequence blocks. Flowchart, structure chart, and written statements for two sequential operations are depicted; same format is followed with all subsequent Figures. One entry and one exit is common with structured programming

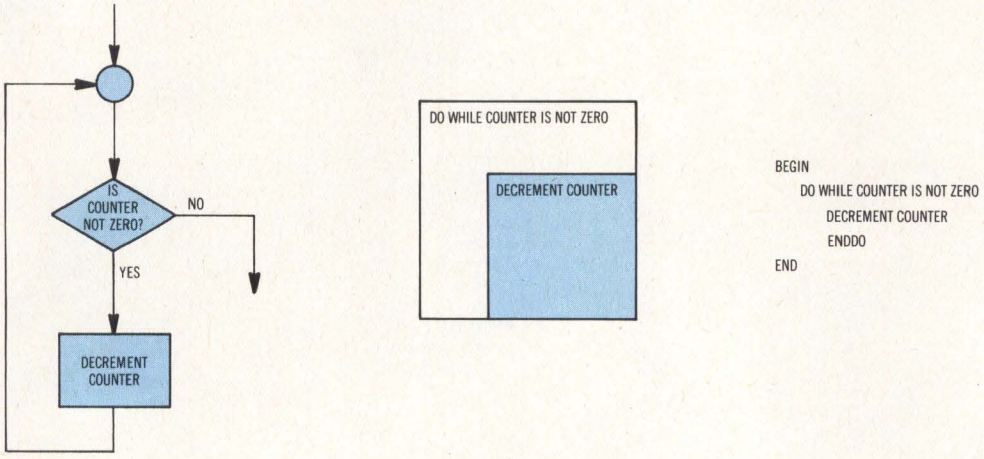

Fig 2 DO-WHILE mechanism. Generalized loop-and-test structure shows microcomputer timing loop

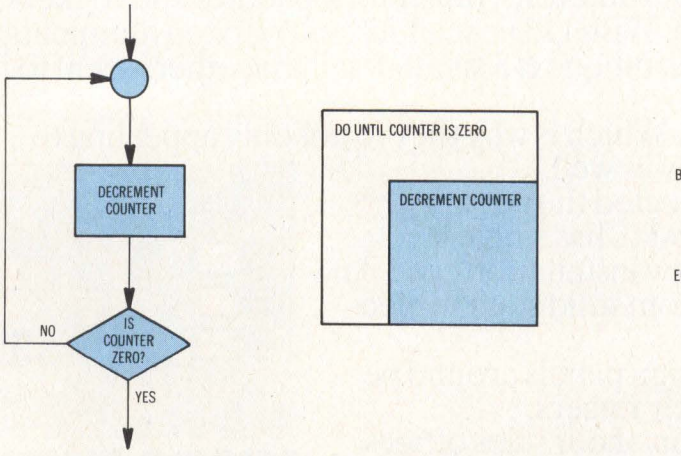

Fig 3 DO-UNTIL (REPEAT-UNTIL) mechanism. Form of timing loop is typical of that used in microcomputers

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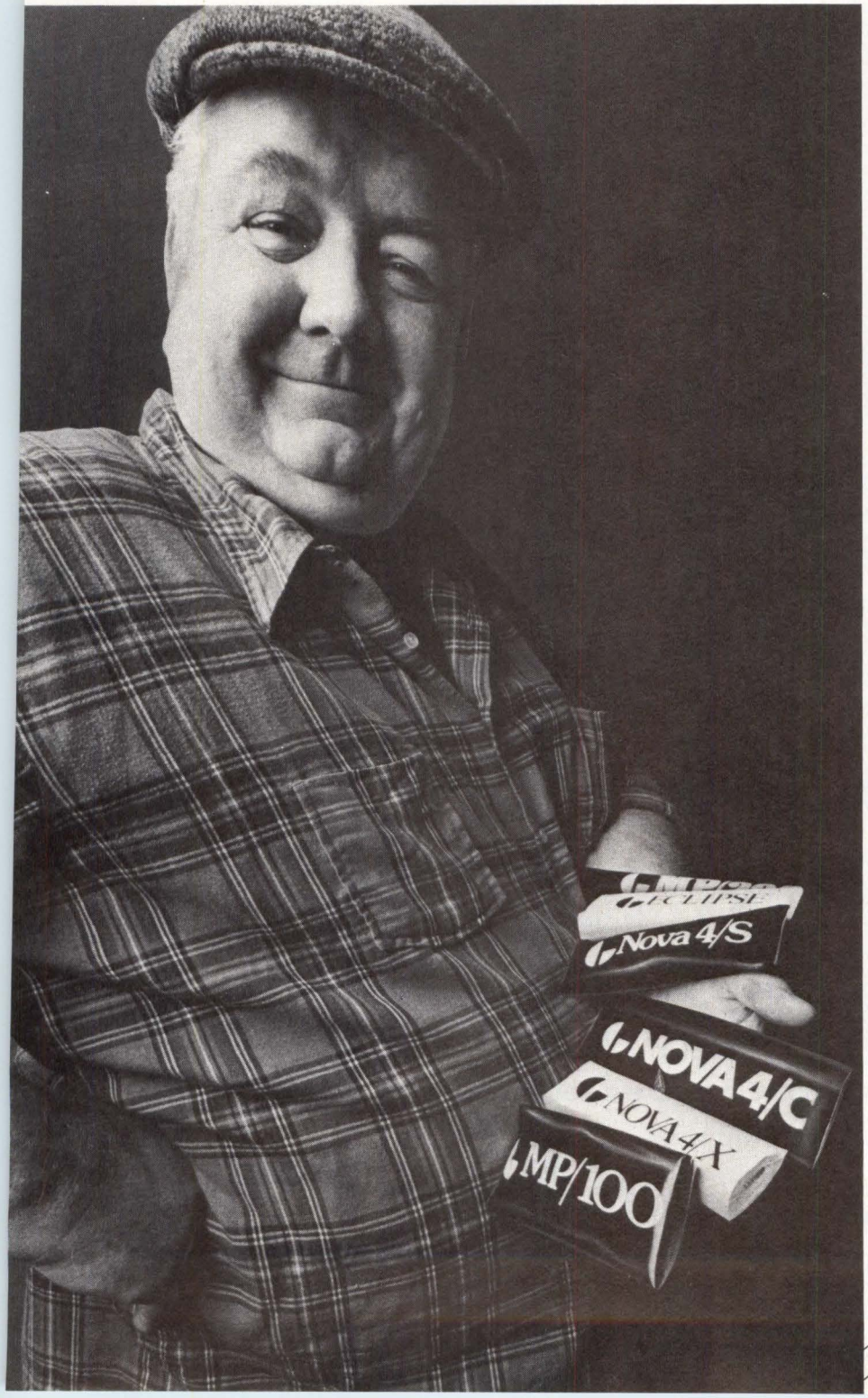

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statement is "change data in buffer," and the second statement is "set semaphore high." These two statements can be combined into a single sequence block. In Fig 1, the pair of sequence blocks is represented in flowchart notation, structure chart notation, and written statement form. The remaining Figures are set up following the same format. Computer scientists find the written statement technique convenient when developing programs on cathode ray tube terminals.

The second structure is a generalized loop-and-test structure, usually called the DO-WHILE block or mechanism. Again, observe that there is only one entry and one exit (Fig 2), a fundamental characteristic of all basic structures in structured programming. In Fig 2, the loop-and-test structure is a microcomputer timing loop, in which a counter is successively decremented until it reaches zero, at which time the loop is exited. A related loop-and-test structure is the DO-UNTIL block or mechanism, also known as the REPEAT-UNTIL block. Fig 3 provides the form of the timing loop that is typically employed in microcomputers; in other words, the counter usually is first decremented, then the zero flag is tested, and finally a branch occurs depending upon the logic state of the flag.

A selection-based-on-a-test structure is the third basic form, universally called the IF-THEN-ELSE block or mechanism. With still only one entry and one exit, the example in Fig 4 is a simple binary test—yes or no. If the answer is yes, the THEN alternative is executed; if the answer is no, the ELSE alternative is executed.

The sequence, DO-WHILE, and IF-THEN-ELSE mechanisms

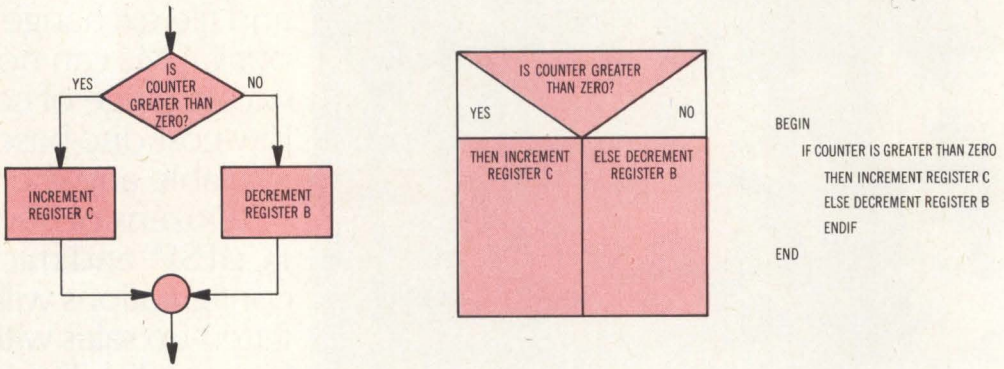

Fig 4 IF-THEN-ELSE mechanism. Simple binary test executes THEN for yes and ELSE for no

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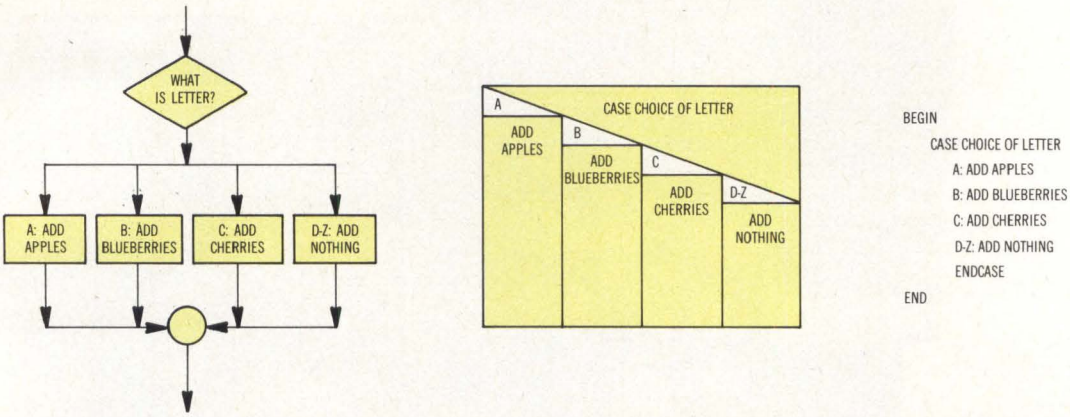

Fig 5 CASE mechanism. Also based on test, mechanism can select from more than two alternatives

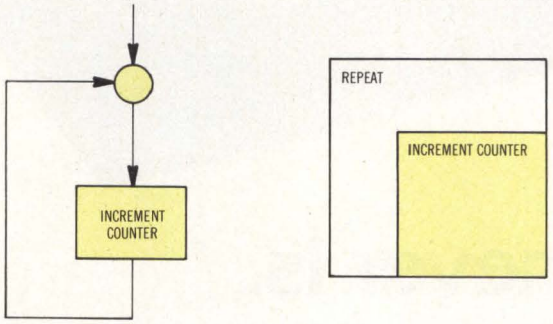

Fig 6 REPEAT (LOOP-FOREVER) mechanism. Although not basic to structured programming, mechanism causes microcomputer to loop until interrupt occurs

comprise the three basic structures. Two other structures commonly found in microcomputer programs are the CASE and REPEAT mechanisms. The CASE block or mechanism in Fig 5 is also a selection-based-on-a-test structure, but with more than two alternatives to select among. This type of structure can be implemented with microcomputers in several ways, such as by a sequence of IF-THEN-ELSE statements or by a command decoder. Single entry to and single exit from the structure are basic characteristics shared in Figs 1 through 5.

Fig 6 depicts the REPEAT mechanism, also known as the LOOP-FOREVER mechanism, which is not one of the basic structures in structured programming. Nevertheless, it is occasionally used in microcomputer programs, such as those that employ interrupt-driven input/output (I/O). In such situations, the microcomputer program loops (perhaps forever) until an interrupt occurs. These notations will be employed next month to continue the comparison of conditional and unconditional I/O techniques.

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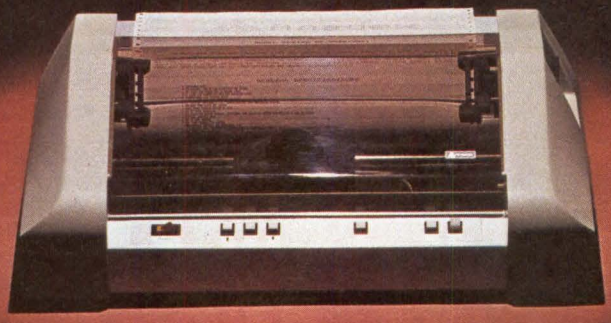
7. E. Yourdon, *Techniques of Program Structure and Design,* Prentice-Hall, Inc, Englewood Cliffs, NJ, 1976

Meet two new Printers from Anadex:

Resolutionary!



Introducing two totally new alphanumeric line printers from Anadex - Models DP-9500 and DP-9501 - featuring 132/175 or 132/220 columns, respectively.

Both models employ a new, Anadex-manufactured 9-wire print head with 150 million character life (optionally, 650 million) that makes them ideal for high-resolution printing requirements including high-density graphics where print quality and reliability must go hand in hand.

The full standard 96 character ASCII character set, including descenders and underlining of all upper and lower case letters, can be printed bi-directionally on up to 5 crisp copies at speeds up to 200 CPS. Adjustable-width tractors, accommodating paper from 1.75 to 15.6 inches wide, allow the printers to adapt to your application.

The three ASCII compatible interfaces (Parallel, RS-232-C, and Current Loop) are standard in every printer; so interfacing is usually a matter of "plug it in and print." With simplified interfacing, the printers also feature sophisticated communications capability including control of Vertical Spacing (6 or 8 lines/inch), Form Length and Width, Skip-Over Perforation, Auto Line Feed, and full point-to-point communications capability.

Other standard features are a 500 character FIFO buffer (optional, an additional 2048 character buffer), shortest distance sensing logic, self test, and replaceable ribbon cartridge with 6 million character life.

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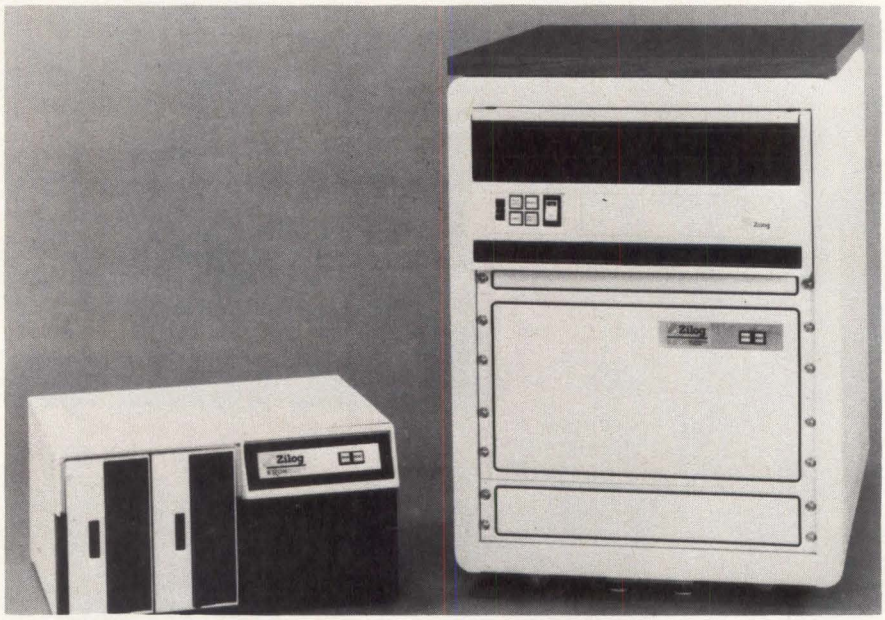
CIRCLE 104 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Modular And Packaged Systems With COBOL Support Expand Business and Industrial Computing



Zilog's MCZ-1/20A and -1/25A microcomputers are designed as modular system building blocks with Z80 CPU and 64k RAM for general purpose industrial and business uses

Hardware elements that are intended for commercial small business and industrial applications are two modular microcomputer subsystems without CRT and software, and two ready to run pre-integrated systems, each with a CRT and one of two versions of software. Zilog, Inc, 10460 Bubb Rd, Cupertino, CA 95014, simultaneously is announcing a Multi-Terminal COBOL option that accommodates up to five users.

Flexibility is the key to the desktop MCZ-1/20A and rackmounted MCZ-1/25A multipurpose microcomputer systems. Standard features of a Z80 microcomputer, 64k bytes of RAM, 4k bytes of P/ROM, interrupt driven console capability, and floppy disc controller may be enhanced by such options as additional disc capacity, Multi-Terminal COBOL capability, and asynchronous communications.

The desktop version has integral dual floppy disc drives, while the rackmounted enclosure is packaged with either integral dual floppy disc drives or cartridge disc drives. Both units are prewired for the addition of up to four floppy discs and four 10M-byte cartridge discs.

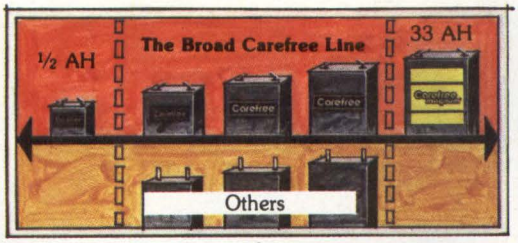
Advancing from these basic modules are the desktop MCZ-1/50 and rackmounted MCZ-1/70 systems. Extra slots in the standard 9-slot cardcage allow the systems to be configured with customized boards. Additional discs to extend the data base and up to four terminals for multiterminal functions further expand the capabilities.

Containing the same basic components as the modular computers, the -1/50 includes a CRT and integral dual floppy disc drives for 600k bytes of storage; the -1/70 with CRT has either integral dual floppy disc drives or cartridge disc drives. These packages, too, may be upgraded to four floppy disc drives and/or four 10M-byte cartridge disc drives.

The system CRT offers full cursor control, blinking, blanking, and

MORE POWER TO YOU! (OR LESS)

You really do have a broader choice.



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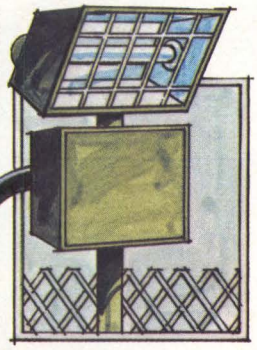
More power—or less—than you'll find anywhere else. With about 30 standard sizes in between. Popular models like our 1, 5, and 8 Ampere Hour batteries. Or **unique**, special-purpose units.



All Carefree® rechargeables feature immobilized electrolyte technology. Guaranteed to deliver 100% capacity on first cycle, unlike gels. None of the memory problems of nickel cadmium. That's why Carefree® immobilized electrolyte technology is becoming the standard of the industry. Specify it in your next design.

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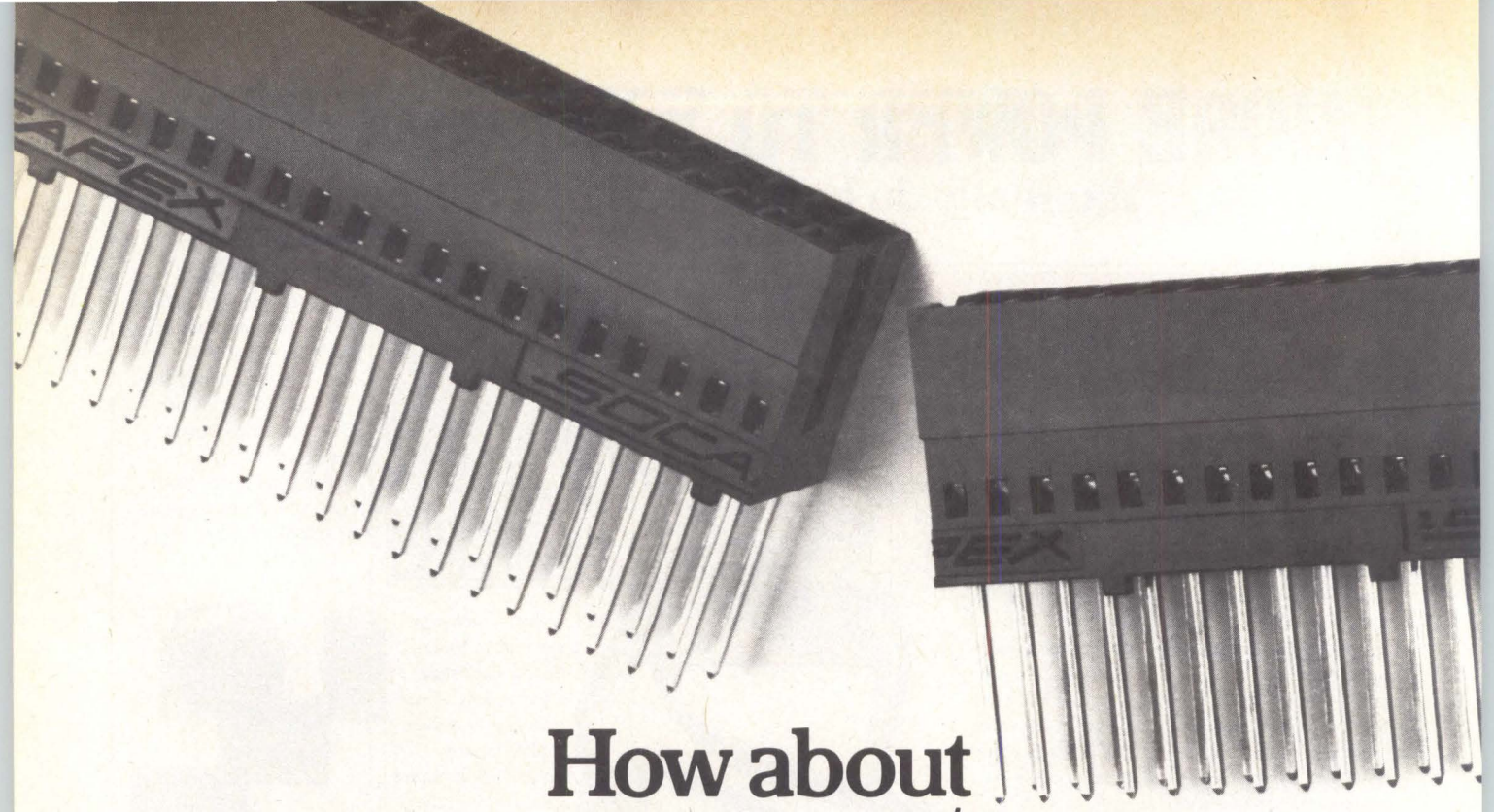
CIRCLE 105 ON INQUIRY CARD



How about changing the P/C connector to fit your design – instead of vice-versa?

Just tell us how many contacts you need—from 2 to 150—and it's yours, right now.

With no special engineering. No custom mold. No lost time. No extra charges.

The secret is in the insulator design of our new Socapex 254 DFT Series. We take the molded connector, cut it to fit your specs—then add the snap-on ears. As simple as that you have a custom connector with from 1 to 75 contact pairs (.100" pitch) with wire-wrap, dip-solder or eyelet tails.

There are some other very nice features, too. For example:

Damaged contacts are easily, quickly changed.

Series 254 DFT
2 to 150 contacts,
snap-on mounting ears.

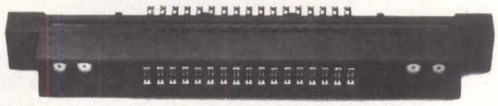
Probing ports let you check any circuit and do it with the power on.

You can't mismatch boards and connectors—special keys prevent it.

And more.

To keep out noise.

For high-speed/low noise circuits, our 254 DFC Series offers matched impedance 50 ohm contacts with low VSWR. They're available with 2 x 17 P/C contacts, plus 4 co-ax contacts. Or 2 x 31 P/C contacts with 6 co-ax contacts, in a two-piece connector.



Series 254 DFC P/C and co-ax contacts.

The 254 DFT and DFC Series. Just tell us what you want and it's yours. Call or write us today for a quote on pricing and delivery.

SOCAPEX

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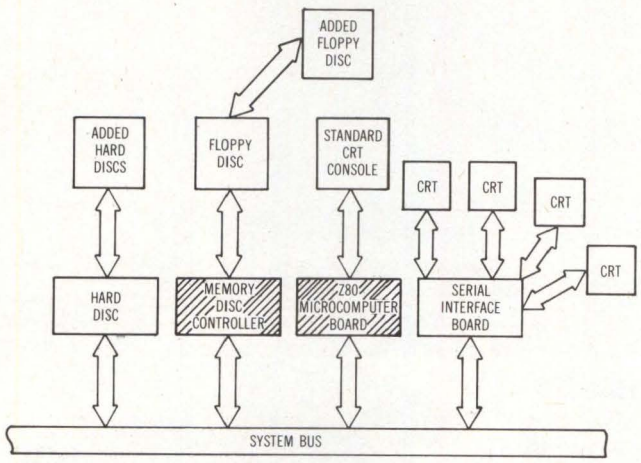

Four MCZ systems are based on minimum of Z80 microcomputer board and Z80 memory disc controller in 9-slot card cage. Packaged -1/50 and -1/70 also add CRT. Floppy and hard disc versions are both available from Zilog in modular or packaged, ready to use versions; expansion occurs with both types of discs and terminals

reverse video. An integral numeric pad is included, along with RS-232-C or 20-mA current loop interface. Baud rates range from 50 to 9600. Options for the systems are additional CRTs, a matrix printer, Z80 serial interface board, and letter quality printer with text formatting package.

All four systems are supported with the RIO operating system that handles system resource management, supports device independent I/O and user defined commands, and permits command linking. Also included are a text editor, debugger, macro assembler, and file management capabilities. High level languages are BASIC, COBOL, FORTRAN, Pascal, and PLZ. Specialized utilities are a text formatting package, along with ASYNC for intercommunication among MCZ systems. Communications and multiterminal packages suit the computers to distributed processing environments, and applications in which the same information must be accessed by several users.

Multi-Terminal COBOL, designed to be run on the MCZ systems, allows up to five users to simultaneously access a data base, or it can limit access to one user. Applications include inventory control, data entry, or other transaction processing. The interactive program offers most Level 1 and several Level 2 features of 1974 ANSI X3.23 COBOL. Existing programs for minicomputers and mainframes can therefore be executed on the microcomputers.

The software is implemented with the addition of the serial interface board, allowing four extra terminals to be connected to the system. The standard RIO operating system has been enhanced with an interrupt driven, multiterminal hardware driver to support the interface board. An interactive debugger and online program editing facility ease COBOL program development and debugging.

CIRCLE 410 ON INQUIRY CARD

Industrialized A-D Board Gives High Common Mode Noise Rejection

SineTrac ST-LSI-RLY relay-isolated inputs provide 126-dB common mode rejection and safe handling of common mode voltages up to 250 V rms. It is used with Digital Equipment Corp's LSI-11, LSI-11/2, and PDP-11/03/23 series microcomputers in industrial environments where low voltages from sensors are often obscured by high voltage noise. Full hardware and software compatibility is assured.

Fitting DEC's half-quad spacing, the 8.430 x 5.187 x 0.50" (21.412 x 13.175 x 1.27-cm) board offers eight differential A-D channels. Datel-Intersil, 11 Cabot Blvd, Mansfield, MA 02048, has included an ADC-EK12 to perform A-D conversions. A 2-bit program word controls the programmable gain amplifier for gains of X1, 2, 5, and 10. This circuit is autozeroed. A programmable gain amplifier processes analog input signals ranging from ±10 mV to ±1.0 V (bipolar) FSR or 10 mV to 2.0 V unipolar. The 12-bit ADC which provides resolution to 1 part in 4096 (±½ LSB), changes these to a digital code.

The memory mapped device uses two consecutive address words in the microcomputer's memory. Both the base address and interrupt vector address, while factory set, may be reset by the user.

Overall system throughput is 36 ms sample to sample (28 samples/s). System zero tempco ranges from 0.5 to 20 μV/°C (gains from X1 to X100, respectively). For the same range of gains, typical system gain tempco varies from 12 to 40 ppm of FSR/°C. Standard binary, offset binary, or 2's complement digital output coding may be set by the user.

A paper tape diagnostic program allows checkout of system performance. Operating temperature is from 0 to 70 °C. Power requirements are 5 Vdc at 1.5 A max, and 12 Vdc ±5% at 70 mA max.

CIRCLE 411 ON INQUIRY CARD

Endangered Species.

Habitat.

In an earlier America, every living thing enjoyed its rightful place. Our abundant country provided wild animals with every environment needed for their survival—green forests, lush wetlands, untouched deserts, and clear, free-flowing rivers.

Over the years we have made good use of our lands, waterways and other resources. But we have also needlessly defiled and destroyed many of them. Today, many of these areas, like some of the animals they once supported, are endangered species.

- In Maine on the St. John River, a proposed, unnecessary dam threatens 500,000 acres of habitat that now provide food, water and cover for moose, lynx, bobcat, osprey, and deer.
- In California's Dove Springs Canyon, reckless use of motorcycles and other off-road vehicles is driving more than 75 species of birds, reptiles and mammals from their desert home.
- In Nebraska, diversions of water are menacing the habitat of the rare whooping crane, a few surviving bald eagles, and millions of migratory waterfowl at the Big Bend of the Platte River.
- In Louisiana's Atchafalaya Basin, a plan to drain and cultivate 800,000 acres of wooded wetlands would wipe out the home of more than 300 species of birds, 50 species of mammals, and countless thousands of aquatic creatures.

These are just some of the endangered habitats the National Wildlife Federation is working to save. We can't turn back the clock, but we can protect habitats we still have. Without them, there will be no wildlife.

Join us. Write Department 201, National Wildlife Federation, 1412 16th Street, N.W., Washington, D.C. 20036.

Save A Place For Wildlife.

THE MOST FIELD PROVEN IS NOW THE MOST VERSATILE.

Telex introduces the new Tri-Density 6250 Tape Subsystem for OEM's.

In 1978, Telex introduced and delivered the first high speed 6250 BPI tape transport for OEM mini-computers. It lets you compact more data. In less space. At faster speeds. Since then we've built up more field proven reliability than any other 6250 OEM tape drive manufacturer.

Now this rack-mounted 6200 Series tape family has been expanded to include the 6253 tri-density tape subsystem. The high performance drive and formatter combines three densities—6250 BPI (GCR), 1600 BPI (PE), and 800 BPI (NRZI)—into a single unit. And as with all 6200 models, tape speeds of 50, 75 or 125 IPS are available. Telex formatters attach up to four 6200 Series drives and up to eight with an expansion option.

One key to the reliable operation of the 6200 Series is our patented Supr-Lite™ Capstan. It weighs only 1.9 grams, and combined with our patented new tape path, lets us use a smaller, more efficient drive motor. Tape handling at high program rates is improved.

Most importantly, the 6200 Series now offers you extreme versatility in matching and field converting a wide range of features and system options. The 800/1600 BPI dual density model 6240 can be easily field upgraded to tri-density. And such options as a 360/370 channel adaptor, high altitude and seismic feature, and dual speed capability will enhance your system configurations and performance many times over.

For more information about the 6200 Series—including its price/performance competitiveness—call your nearest Telex OEM representative. Or phone our OEM Marketing Department in Tulsa at (918) 627-1111.

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CIRCLE 108 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Digitizer Graphics Board Stores Video Data For Multibus Systems

Total video acquisition and display are handled by the VG-120 Intel Multibus compatible single-board graphics system. It acquires a full screen of display information from any EIA standard video source, simultaneously digitizes and stores the realtime data, and enters them into an 80k-byte onboard memory. They are available for computer read/write access and display on a TV monitor. Autoincrement screen address registers permit easy sequential data access.

The Multibus based computer can evaluate and modify video data for inplace enhancement, as well as generate its own binary memory pattern for display as video. The computer can also transmit the same memory information to a remote site for display or analysis. Applications include graphic generation, image processing, scan conversion, and transmission of TV images over voice grade telephone lines (with a modem).

High density video binary storage and regeneration offers 320 H x 240 V pixels, with 6-bit pixel resolution. Datacube, Inc, 670 Main St, Reading, MA 01867, produces two output video versions—black and white with 64-level illuminance or pseudocolor with 64 color shades. Average access time is 800 ns.

Input section consists of an EIA standard video input, realtime 6-bit ADC, computer controlled frame grab, and H-V or composite sync camera drive. The output portion contains the 6-bit realtime DAC, EIA standard video output, H-V and composite sync outputs, and RGB video outputs (on applicable models). Bus and video drive signals are TTL compatible. Video timing meets EIA spec RS-170, and the board can be crystal controlled or referenced to an external timing source.

Indirect (X,Y) memory addressing is via horizontal and vertical vector ports. Indirect addressing with an auto increment mode allows up to a 1.2M-byte/s data transfer rate. Ports may be addressed either in I/O or in memory mapped mode.

CIRCLE 412 ON INQUIRY CARD

Get quick delivery on these axial cooling fans

Capacities from 30 to 130 CFM

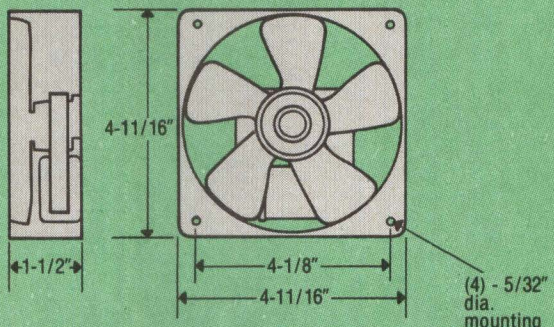
For quick delivery and competitive pricing evaluate these Lamb Electric fans for your cooling requirements. All models incorporate a sealed lubrication system for continuous circulation of lubricant in the bearing area. This patented* lube system is designed to increase fan life with the unit mounted in any position. These fans are component-recognized by Underwriters Laboratories Inc., and are available in 115 or 230 Vac designs for 50/60 Hz operation. Both Blazer and Blazer 30 fans can be supplied as a skeleton design if shrouding is not required. Cord sets and finger guards available to customer specifications.

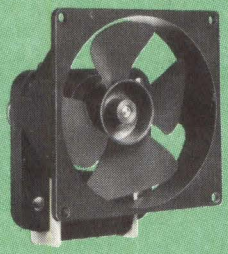
Put Lamb Electric's proven productive capabilities to work for you. For pricing and delivery details, call: Norman Anderson, AMETEK, Lamb Electric Division, 627 Lake Street, Kent, Ohio 44240. (216) 673-3451. Telex: 98-6497.

AMETEK
LAMB ELECTRIC DIVISION

BLAZER® FANS

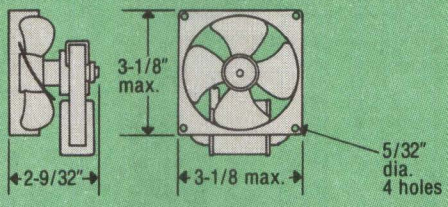
Model	CFM @ 60 Hz (Exhaust or intake)
117759-00	60
117761-00	65
117757-00	80

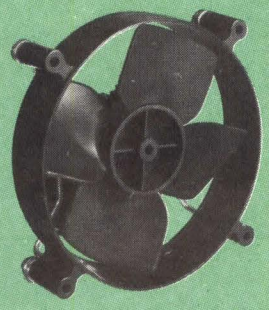




BLAZER 30 FANS

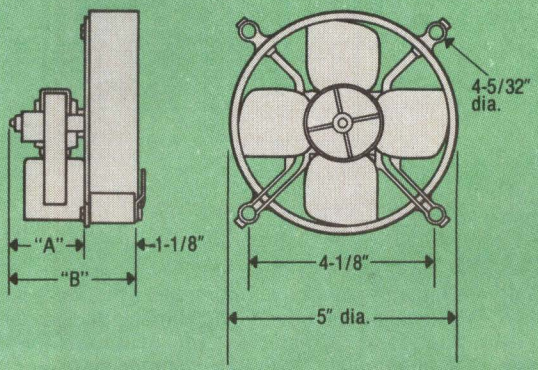
Model	CFM @ 60 Hz
117731-00 Intake	30
117733-00 Exhaust	40





ZEPHYR FANS

Model	CFM @ 60 Hz	"A"	"B"
117718-00 (Exhaust)	90	1-5/8	2-3/4
117719-00 (Intake)	80	1-5/8	2-3/4
117720-00 (Exhaust)	100	1-3/4	2-7/8
117721-00 (Intake)	100	1-3/4	2-7/8
117722-00 (Exhaust)	120	1-3/4	2-7/8
117723-00 (Intake)	120	1-3/4	2-7/8
117724-00 (Exhaust)	130	2	3-1/8



U.S. Patent 3,763,386

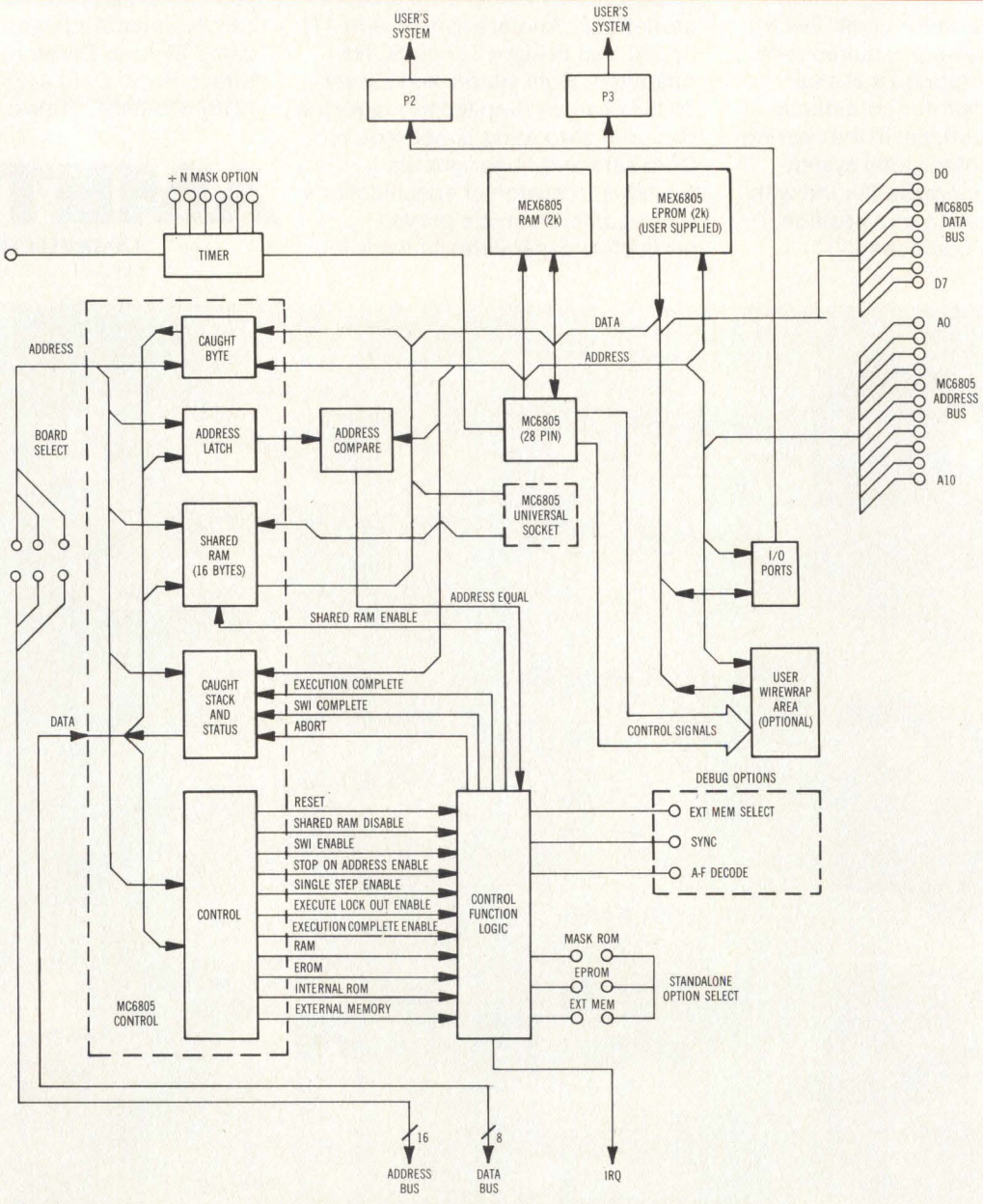
CIRCLE 110 ON INQUIRY CARD

Support Package Adapts Development System To 6805 Microcomputer

Existing EXORciser and EXORterm equipment convert to the development and realtime emulation of MC6805 microcomputer systems with the addition of the MEX6805 support system. Basis of operation is the 2-processor approach of the 6805 microcomputer operating with the 6800 CPU in the development system, isolating the 6805 from the development system buses while allowing interprocessor communication through status/control registers and shared memory. Existing M6800 hardware and software can be used to develop 6805 systems.

This support system from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, consists of the PC board module, extender cables for user systems evaluation (USE-6805), and an MDOS diskette with the 6805 macro assembler and FIVEbug, the system debug/monitor program. The module's shared memory scheme allows multiple processors (four maximum) to run in the user target system, with the debug function limited to one processor at a time. A separate socket allows use of the 6805 self-test capability to verify chip functionality.

All onboard RAM, EPROM, and external memory may be used; single-step and set one breakpoint function or halt-on-address may be applied to pro-



Emulating single- or multi-6805 systems independent of the EXORciser bus, Motorola's support system features software selectable EPROM/mask ROM/external memory options; 6805 data/address lines available for hardware analyzers; 6805 self-test socket; and jumper selectable memory options. Extensive debug capability and macro assembler are included. Memory block A-F in user wirewrap area is fully decoded to provide custom I/O implementation

grams in these memories. Up to eight breakpoints can be set for programs in onboard RAM, EPROM, ROM, or external memory programs run in realtime. System operation may be in stand-alone mode, forfeiting interrupt-driven debug capabilities.

The USE system extends debugging capabilities into the prototype hardware to evaluate combined hardware and software. FIVEbug firmware commands are for MEX6805 module configuration; data manipulation to load and verify tape or disc files and to display and change memory or registers; processor control to display, set, or reset breakpoints; and memory change or display of contents of a memory location.

The MC6805 macro cross assembler and linking loader extend software development capabilities to include assembly of 6805 source code. Macro assembler supports include macros, conditional assembly, relocation, and linking. The linking loader combines relocatable object modules to produce an absolute object image.

Unit price of the system in 1 to 5 quantities is $2000. Minimum system requirements are an EXORciser 1, 2A, or 2 with EXORterm 100 or 150; or EXORterm 200 or 220; with EXORdisk II or III/IIIE; and 24k of memory.

CIRCLE 413 ON INQUIRY CARD

Single/Multiple Emulators Support Peripheral Interface Microcomputers

Two in-circuit emulation options for debugging and integrating software and hardware designs support the iSBC-80/30™ single-board computer and other designs based on 8085 masters and 8741A or 8041A slaves. The ICE-41A™ in-circuit emulator emulates the 8741A and 8041A universal peripheral interface microcomputers while the Multi-ICE™ software package provides multiprocessor development support. They can be used on any Intellec system model with the company's standard ISIS-II diskette operating system.

Advanced techniques of symbolic debugging are provided by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, in the ICE-41A emulator, making it unnecessary for the designer to keep track of the address changes. Assigned names or symbols of subroutines are used in simple commands, while the Intellec system and ICE-41A software handle program access and diagnostic display. There are 18 commands available along with a range of modifiers. The designer can obtain trace information following

realtime emulations run at 6-MHz clock rates, or can single-step through a program.

ICE-41A is able to uncover hidden onchip functions such as program execution by providing equivalent functions and a trace memory on the emulation board. A user can access these functions through the system's CRT display/keyboard console, controller board, and ICE-41A support software. The emulation board contains the data memory and logic functions necessary to emulate the UPI-41A devices. The controller board is an 8080 microcomputer subsystem that interfaces the Intellec system and the emulator.

Enhancement to the previously introduced Multi-ICE package enables one Intellec system to control and coordinate operations of three in-circuit emulator combinations: the ICE-85/ICE-41A; two ICE-85 emulators to develop systems with multiple 8085 microprocessors or 8085 based iSBC systems; and ICE-85/ICE-49 for systems with 8021, 8035, 8039, 8048, 8049, and 8748 microcomputers.

Creating a software interface between the user and the ICE units, the Multi-ICE package executes a host process, as well as two ICE processes. The host process communicates with the user at the Intellec console and translates commands into execution lists for itself and the two ICE processes, which control the ICE units. Commands may originate from the console or from diskette files.

ICE-41A is provided with its own software support package on flexible disc for $4200. This includes emulation and control boards to plug into the development system chassis, along with buffered cabling to interface the development system and user's prototype design. The enhanced Multi-ICE package will be supplied without charge to purchasers of the original ICE-85/ICE-85 and ICE-85/ICE-49 package. Purchase price of the enhanced package is $1750.

CIRCLE 414 ON INQUIRY CARD

Peripheral Implements Storage With Magnetic Bubble Memories

TM990/210, offering nonvolatile storage without battery backup power, is designed by Texas Instruments, Inc, PO Box 225012, Dallas, TX 75265, for bus compatibility with the TM990 series of microcomputer modules. Complete with the necessary support circuitry for bubble devices, the storage peripheral contains two, four, or six 92k-bit TIB0203 bubble memories for 23k, 46k, or 69k bytes of storage, respectively.

Single- or multipage data transfers from the module occur in memory-mapped mode. Access time is 4 ms and data transfer rate is 45k bits/s. Standard 5- and ±12-V power supplies are required. The module operates over a 0 to 50 °C temperature range.

CIRCLE 415 ON INQUIRY CARD

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CIRCLE 113 ON INQUIRY CARD

Analog I/O Boards For LSI-11/2 Offer High Performance

Two analog I/O systems, each mounted on a standard Digital Equipment Corp dual-height board for backplane and software compatibility with LSI-11, -11/2, and -11/23 computers, cover the range of high and low level analog inputs. Common features are a 16-channel, 12-bit A-D conversion system, two 12-bit DAC channels, a software efficient digital interface structure, and timing and control circuits.

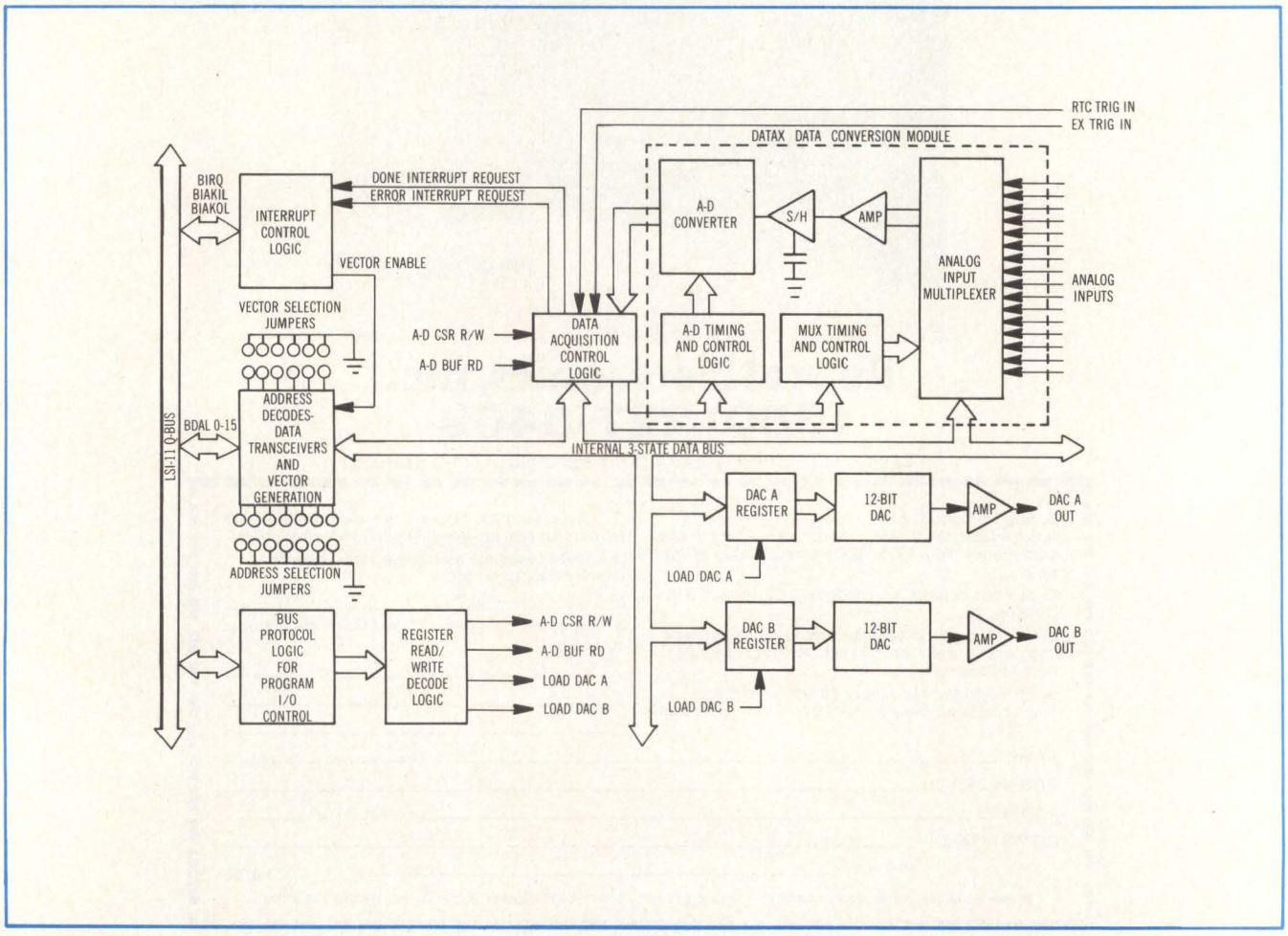
Operating from a single 5-Vdc power supply, the systems include optional 14- or 16-bit A-D conversion systems as well as a software programmable gain amplifier. Throughput rates of these versions are 10 and 2.5 kHz, respectively.

The standard 12-bit, 25-kHz version of model DT2781 is jumper selectable for single-ended or differential input configuration. Analog input voltage ranges from 0 to 5 V, 0 to 10 V (unipolar), ±5 V, or ±10 V (bipolar). With a gain of 1, input system accuracy is ±0.03%, ±0.01%, and ±0.0075% FSR for 12-, 14-, and 16-bit conversions, respectively. A PGH- option software programmable gain amplifier produces code selectable gains of 1, 2, 4, and 8.

Accepting low level analog input signals with values between 10 mV and 10 V, the model DT2785 exhibits the same accuracy and throughput rates of DT2781 versions. Field adjustment by a single resistor allows the -85 to accept voltages within any full-scale range between millivolts and 10 V. Code selectable gains from the software programmable gain amplifier are 1, 10, 100, and 500, for unipolar and bipolar full-scale ranges of 0 to 20 mV and ±20 mV, respectively.

The output system is comprised of two independent D-A converter channels which accept unipolar, straight binary input; bipolar, offset binary; or 2's complement digital input codes. Unipolar 0- to 10-V output or bipolar ±5- or ±10-V outputs can be jumper selected. Both D-A channels have guaranteed monotonicity at 25 °C, with integral and differential linearities of ±½ LSB. Each DAC has a 16-bit word selectable input buffer register to prevent indeterminate analog output states.

Both boards have been designed by Data Translation, Inc, 4 Strathmore



308 DATA ANALYZER

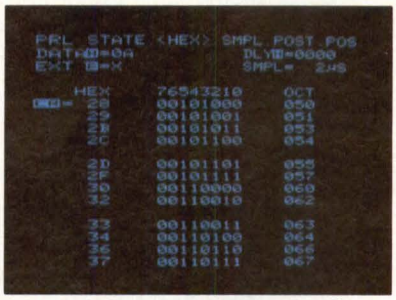
Easily acquire the data you need.

1. Select parallel state, parallel timing, serial, or signature operation. Simply press the appropriate key.

2. Choose synchronous or asynchronous sampling. Use the clock of the system under test or the 308's own internal clock. In either case, sampling rates up to 20 MHz are possible.

3. Enter the word you want to use as a trigger to acquire data. Other keys let you select an external trigger and trigger delay.

4. Press "start" and you're done. Now, you can view the acquired data in the format you want. Or, store the data in the reference memory by pressing the "store" key. Other function keys allow you to acquire new data and compare it with the reference memory.



In each data acquisition mode, all measurement parameters are displayed for your convenience.

Minimum keystroking with the new 308 Data Analyzer from Tektronix.

Of course, the 308 Data Analyzer can do a lot more than we've shown here. For example, there's a self-test routine at power-up, plus seven diagnostics, to ensure accurate results. And the 308 weighs only 8 pounds (3.6 kg), for easy portability.

For the full story, contact your local Tektronix Field Office, or write us.

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Rd, Natick, MA 01760, with two software operable input modes for two types of external trigger to initiate A-D conversion. These are a TTL level realtime clock input to synchronize the start of A-D conversion to an external event and a TTL compatible input terminal for synchronous and asynchronous triggering. Another feature is a control and status register to maximize software use in controlling the interface structure.

The programmed I/O interrupt interface structure allows these models to operate under the Digital Equipment Corp RT-11 realtime operating system. A separately available DTLIB FORTRAN subroutine support package expedites system startup and minimizes software development costs.

CIRCLE 416 ON INQUIRY CARD

Microcomputer Enclosure Holds Backplane And Supports Components

Computer systems based on the LSI-11 family can be configured with the HV-1123 enclosure. Particularly suited to communication and data acquisition applications, the expanded 8-quad slot backplane features cable access to all modules. Netcom Products, Inc, 430 Toyama Dr, Sunnyvale, CA 94086, has included the front panel switches, internal cooling, ac power control, and 5-/±12-Vdc power supplies that are required to support the system.

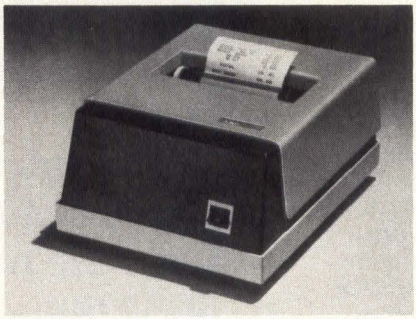
Measuring 13.34 x 43.18 x 53.34-cm, the case contains space for 16 option modules on the backplane; it accepts the LSI-11/23 microcomputer and up to 14 modules. Optional features are a 19″ (48-cm) rackmounting kit, heavy duty 5-V/25-A power supply, and power-down sequence.

Input voltage is 115 Vac ±10%, 47 to 63 Hz, with 230 Vac ±10% optional. Input power is 250 W max at full load. All power supplies have built-in overvoltage protection and automatic current limit/foldback for short circuit and overload protection. An emi filter is located at the ac input, and an on/off switch and circuit breaker on the rear panel control power within the enclosure. The circuit breaker gives protection to 6 A before it will trip; once tripped, the breaker must be reset for normal operation.

The standalone switch/indicator module has three front panel switches, two LED indicators, line time clock logic, and power sequence logic. The standard P101 switch group interfaces to the backplane via a cable that plugs into the signal connection pin pattern. This group provides interrupts on power-up sequencing only while an optional P103 group provides interrupts on power-down sequencing as well.

CIRCLE 417 ON INQUIRY CARD

Dot Matrix Printer Impacts Small Business Microcomputer Systems



Model 7000+ provides 1.25-line/s unidirectional printing across a 3.33″ (8.46-cm) line for small business and home microcomputers. Capacity is 40 columns at 12 characters/in (5/cm). Interfaces include TRS-80 parallel, Apple parallel, RS-232-C, PET IEEE, and current loop.

The rugged enclosure of the dot matrix impact printer measures 6.5 x 10 x 12.5″ (16.5 x 25 x 31.8 cm). It accepts single- or multi-ply paper rolls from 0.75 to 3.875″ (1.9 to 9.843 cm) wide.

LRC, an Eaton company, Technical Research Pk, Riverton, NY 82501, has equipped the unit with a printhead having a minimum of 100M characters; overall mechanism life of the unit is 10M cycles. The head prints continuously without overheating.

The full ASCII character set (upper and lower case) prints in a single- or double-wide font. Options are a 120-character buffer, and a version that prints 64, 40, 32, or 20 characters/line.

CIRCLE 418 ON INQUIRY CARD

Communications Interface Supports Parallel/Serial Data And Color Video

An approach that combines a Z80A microprocessor with currently available peripheral devices results in a programmable communications processor that handles any mix of 8-bit parallel (for nonencoded keyboards, digitizer tablets, and printers), asynchronous or synchronous serial, and color video graphics. The single dual-width board is compatible with the Digital Equipment Corp LSI-11 family. It may be equipped with a mix of up to 8k bytes of RAM and up to 16k bytes of ROM.

Optional low resolution NTSC color video alphanumeric/graphics are available, with fully programmable RAM resident text fonts. Display resolution is 256 x 192 points in 15 colors. Text can be displayed in a 24-line x 40-column format. The video display is suited to business and industrial control applications.

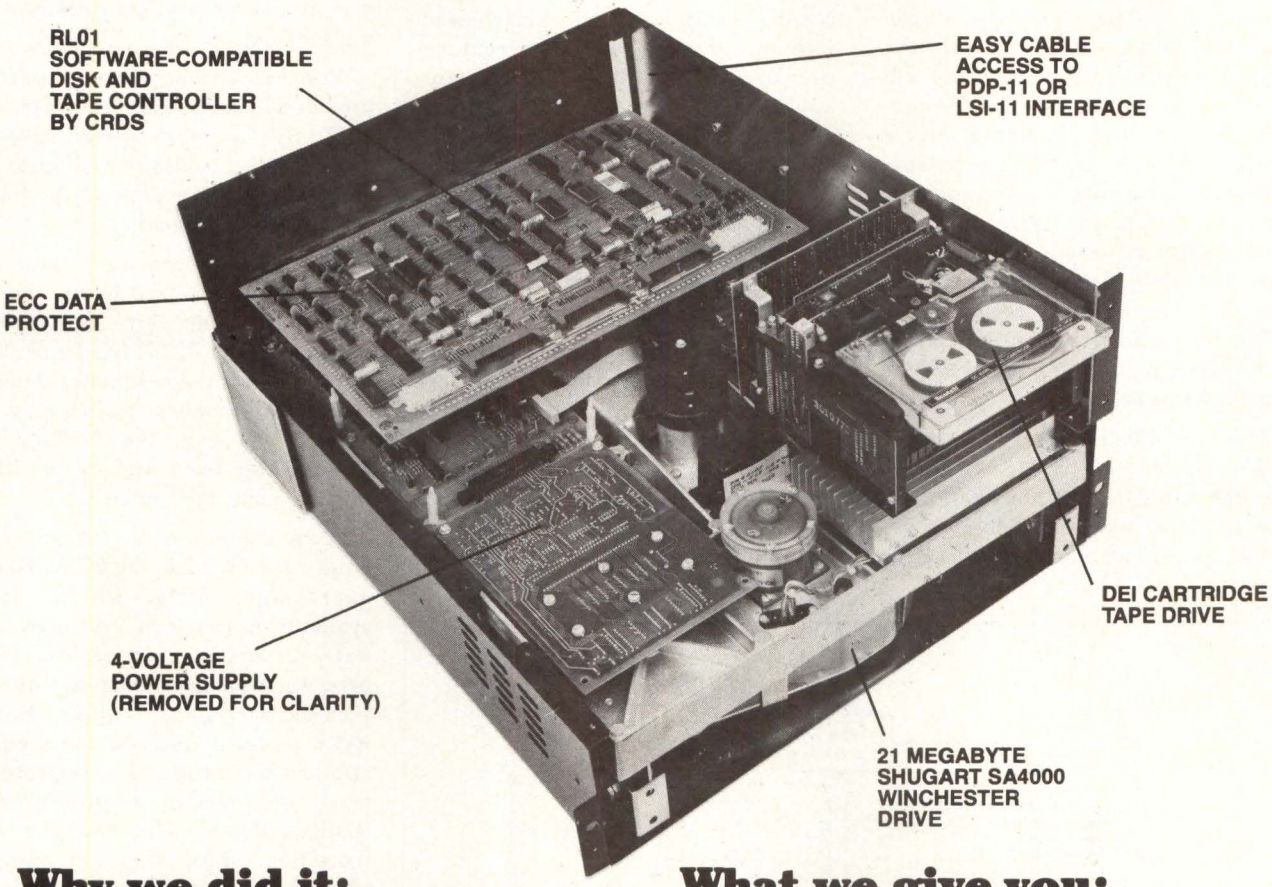
Basic configuration of parallel port, 2k EPROM monitor, and 1k RAM is priced at $525. Other configurations include a video package, an answer/originate serial unit, and various memory options. To develop and test applications control software on a host LSI-11, Nortek Inc, 2432 NW Johnson St, Portland, OR 97210, has equipped a full-option OEM development version with downline loader, debug package, source code resident monitor, model device handlers, and a macro cross assembler and relocating linker that run under RT-11 ($1950).

PCP-11L may add an optional dialer interface to provide auto-answer, auto-dial support for most serial communications protocols. Since protocol overhead is primarily managed onboard, choice of formats is invisible to the host system. Data transfer rates may exceed 48k baud.

Bisync, SDLC, DDCMP, Bell 801 Auto Calling Unit, and intelligent graphics controllers; NBS data encryption routine; resident assembler; and high level language interpreter are among the planned software modules. Control software resides onboard in volatile memory or can be downloaded from the host. The latter allows the device to be reconfigured to meet user needs.

CIRCLE 419 ON INQUIRY CARD

The inside story of our DEC-11® Winchester disk system with fail-safe cartridge tape back-up.



Why we did it:

The HD-11 Winchester Disk system is CRDS's fail-safe solution to data loss should the sealed disk ever be unrecoverable.

We've combined the industry-standard Shugart SA4000 Winchester Drive with an optional DEI cartridge tape back-up module. CRDS disk/tape controller, interface cards and all related hardware complete the package. Of course, the HD-11 is RL01 instruction set compatible, and is equally at home in a PDP-11 or LSI-11 based system.

So now you can have an ultra-reliable storage system for the most popular CPU's available, in a familiar software environment, all at a cost many times less than DEC peripherals!

We did it because we knew you needed a system like HD-11. Send for details today. Once you compare prices and check the specs, you'll be glad we did.

What we give you:

In a single, complete 10½" rack-mountable enclosure, you get the equivalent capacity of four RL01's. HD-11 disk-only system single-quantity price is $6,500; backup tape option is $2,200. Plus you get:

- 21 megabyte formatted disk storage
- RL01 instruction set compatible
- 15 MB cartridge tape backup option
- ECC data protect on both disk and tape
- Q-bus and Unibus compatible
- Four write-protect switches
- High-technology controller prevents latency while using bandwidth more efficiently
- 2-way peripheral for most cost-effective, reliable approach to storage applications

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CRDS

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CIRCLE 114 ON INQUIRY CARD

8-Bit CPU Card Appeals To Multiprocessor And Dedicated Applications

ZBC-80 is a 4-MHz Z80 based, single-board computer, compatible with the Intel Multibus. Included in the advanced chip set that maximizes processor speed and efficiency are a dedicated arithmetic processor, 16-level programmable interrupt controller, two 8255 peripheral interface chips giving six parallel I/O ports, six programmable timer/counters from two 8253 counter/timer chips, and a serial communications controller. Port modes are uni- or bidirectional with or without handshaking.

There are 16k/64k bytes of RAM and sockets for up to 40k of P/ROM-ROM. The onboard RAM does not require the CPU to insert wait states in memory access cycles; thus, the card runs 20% faster than other CPU cards, according to Matrox Electronic Systems, Ltd, 5800 Andover Ave, Montreal, Quebec H4T 1H4, Canada.

Higher system throughput for processing requirements may be achieved with two or more processors running concurrently. For these multiprocessor applications, bus arbitration logic allows up to three masters to share the bus according to serial priority; additional external logic allows up to 16 masters to be handled in parallel priority. Other masters communicate with the CPU card in a pseudo-DMA manner via an onboard input.

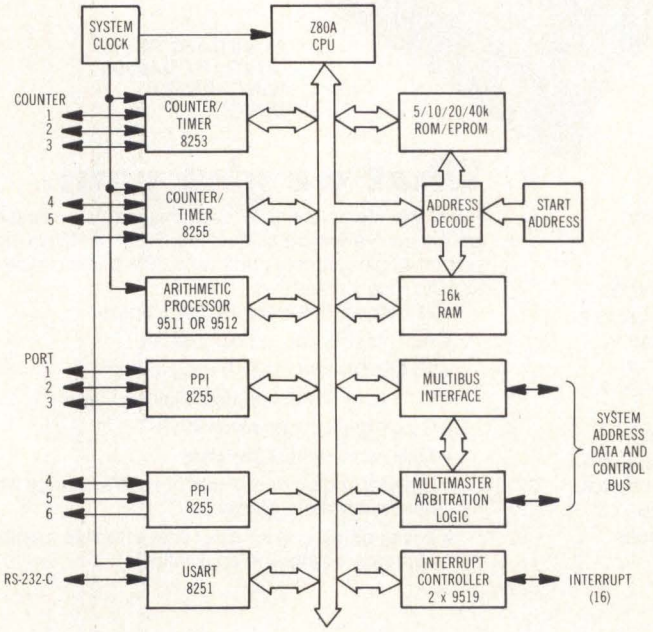
Two AM9519 8-level universal interrupt controllers with maskable interrupts are cascaded to produce a 16-level controller that operates with fixed or rotating priorities. Programmed inputs respond to positive or negative transitions on the interrupt lines. A programmable vector can be generated in response to an interrupt acknowledgement from the CPU. A vectored interrupt structure is employed; nested interrupts are permitted when a device of higher priority requests service while a lower priority device is being serviced.

A serial communications channel provided by an RS-232-C interface and 8251 USART supports synchronous and asynchronous transmissions up to 64k and 19.2k baud, respectively, with half- and full-duplex signaling.

Arithmetic processing functions of the CPU are enhanced by an optional high speed math chip. The Am9511 performs 16- or 32-bit fixed and 32-bit floating point arithmetic; trading speed and number of functions for greater precision, the Am9512 performs 32-bit fixed and 32- or 64-bit floating point arithmetic.

From the software end, the computer runs CP/M 2.0, the 8080/Z80 disc operating system, which makes available a range of packaged software—assemblers, text editors, debuggers, and high level language utilities such as FORTRAN, Pascal, COBOL, and BASIC, as well as business and scientific application programs. Reprogramming the various controller chips changes the specific hardware configuration; thus, the card can be tailored in software to meet most hardware requirements.

CIRCLE 420 ON INQUIRY CARD

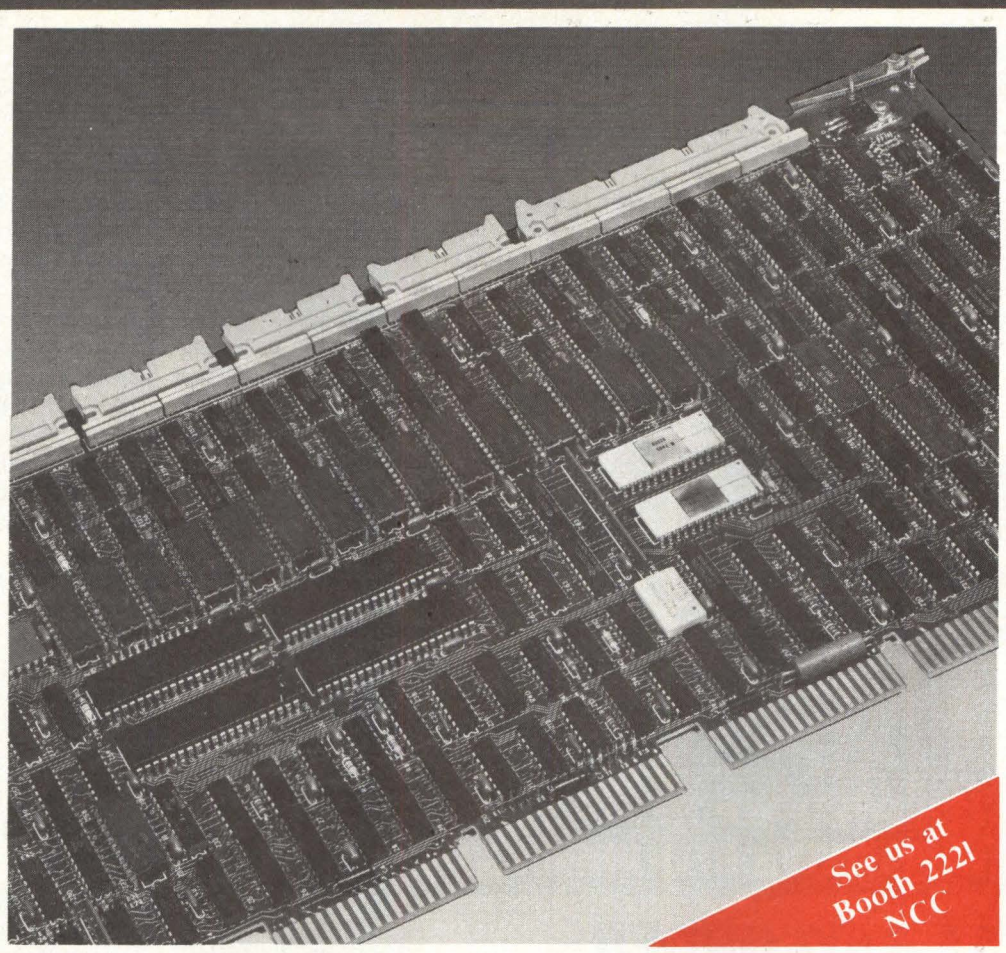


High performance hardware of Matrox Electronic Systems ZBC-80 single-board computer with 16k of RAM supports Digital Research's CP/M 2.0; hardware and software are configurable to meet desired multiprocessing and dedicated tasks

Clock/Calendar Module Operates Without CPU Involvement

Timekeeping functions may be added to Multibus systems to maintain and update the present time and date. MC1460 interfaces directly to the system bus, for such applications as system clocks, data logging systems, elapsed time measurements, resource usage monitoring, and timed task initiation.

Independent random access input ports provide binary data representing



ONE-BOARD PDP-11 SMD CONTROLLER, SOFTWARE COMPATIBLE...A FIRST!

Dataram's S33 interfaces Digital Equipment Corporation's (DEC®'s) PDP-11 series to a wide selection of SMD (storage module drive) and Winchester type disk drives. The S33 emulates DEC's RM02 and is fully software compatible with RM02 diagnostics and RM02-supporting operating systems. Up to four drives per S33 controller, almost 300 MB of disk storage. The microprocessor-based S33 controller has 2 KB of data buffering, multiple sector transfers, and built-in self-test capability. And media compatibility with DEC's RM02 drive. All this and amazingly packaged on one DEC hex board...the only controller to make this claim!

One-board means you need only one hex SPC slot. One-board means easy insertion and optimum air flow.

One-board with its attendant features of minimized interconnections and low component count means lower power, complete accessibility, higher reliability...and best of all, lower cost.

If you're interested in one of our one-board S33 controllers, or a whole bunch of them, we'd like to hear from you. If you operate in the LSI-11® world, still contact us. Our LSI-11 cousin of the S33 is on the way.

DATARAM CORPORATION
PRINCETON-HIGHTSTOWN ROAD CRANBURY, NEW JERSEY 08512
TEL:609-799-0071 TWX:510-685-2542

the month, day, hours, minutes, and seconds. Outputting the time and date to the appropriate ports sets the module. An external battery supplies power whenever the system power is shut off.

Another feature of the module from Micro/Sys, 1353 Foothill Blvd, LaCanada, CA 91011, is the periodic and power-fail interrupt system. Periodic interrupts of the CPU are enabled under software control at intervals ranging from 10 ms to 24 h. Power monitoring circuitry generates a power-fail interrupt whenever system power is lost.

The 50/60-Hz line frequency as a timing reference assures longterm accuracy. During backup power operation (5 V ±10% at 12 mA max), an onboard crystal oscillator maintains proper time and date operation. Port addressing, power monitor configuration, and interrupt level selection are switch selectable.

CIRCLE 421 ON INQUIRY CARD

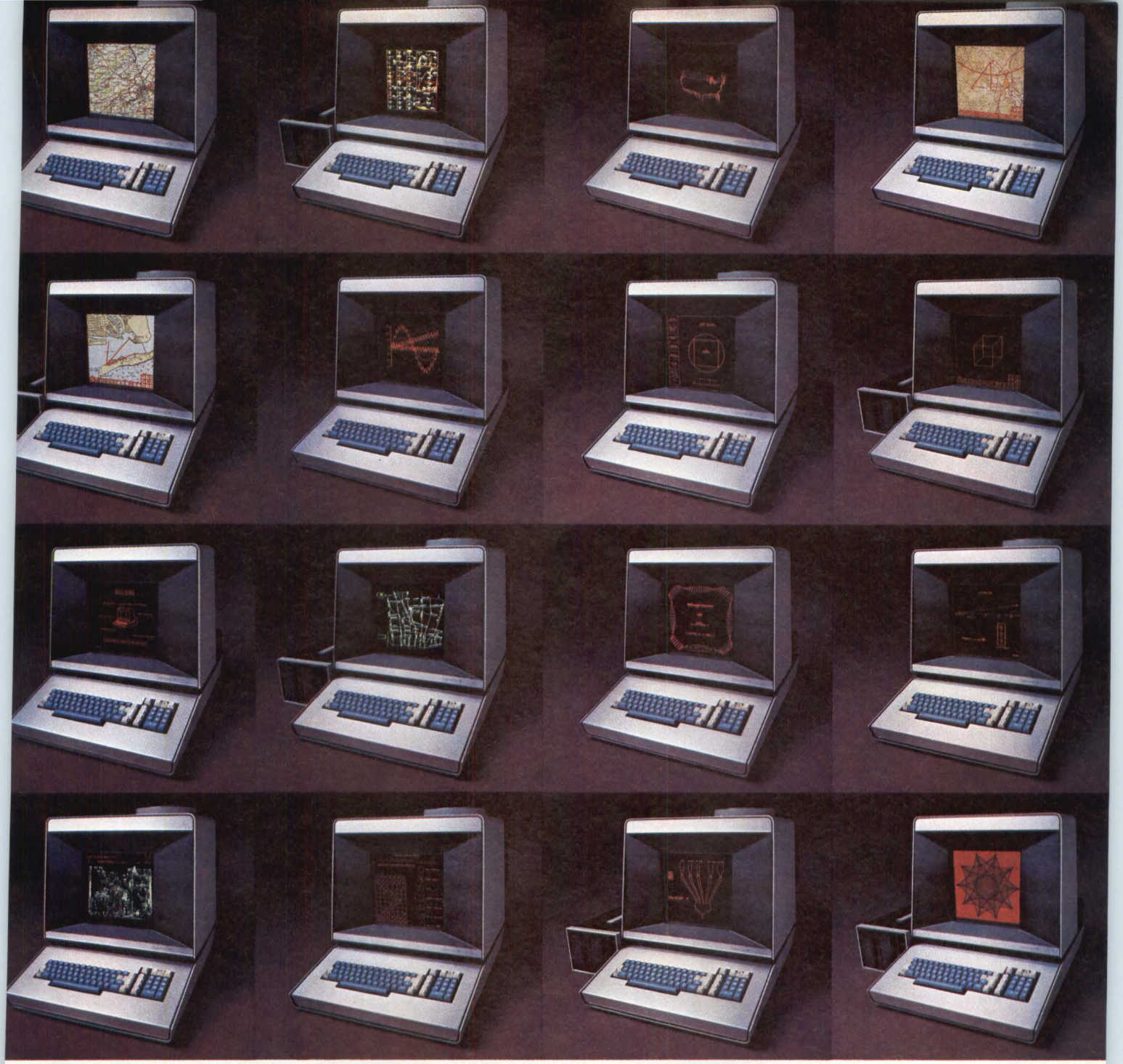
Floppy Disc Controller Increases Online Data And Doubles File Size

Disk 2+2 single-density 8″ (20-cm) floppy disc controller increases the Apple II microcomputer's online storage capacity under Apple DOS 3.1 or 3.2 to 1M bytes. This also expands the file size and reduces the number of discs handled by the user. Existing software for the Apple will run with the peripheral, providing instant upgrade for systems facing file size restrictions. Data exchange from the Apple to other IBM 3740 format users is an added feature.

Manufactured by Sorrento Valley Associates, 11722 Sorrento Valley Rd, San Diego, CA 92121, the device controls up to four industry standard 8″ (20-cm) floppy disc drives—Shugart SA800/801 or equivalent—under Apple DOS or assembly language control. Providing the industry standard IBM 3740 format, the 1771 LSI controller assures reliable data storage and compatible data exchange.

Drives are powered independently of the computer (with a 48k-byte memory). Data transfer rate is 256k bits/s. Average access time is 260 ms. Additionally, two business packages—a general ledger and financial management system—have been configured to run with the peripheral.

CIRCLE 422 ON INQUIRY CARD



WHEN IT COMES TO PUTTING IT ALL ON DISPLAY, THE ORION-60 STANDS ALONE.

A display terminal that won't stand alone can't be as versatile or as adaptable as the Orion-60, the modular plasma display system that stands by itself or interfaces with existing hardware to let you create your own programs.

To begin with, the Orion-60 is an easy touch: besides offering full alphanumeric, floppy disc and rear-projection capabilities, it lets you create displays and enter data simply by touching the screen with your finger.

That means you can project a slide onto the screen coordinates and plot your own course over it. You can program your own character sets. You can generate vectors of any length to absolute screen coordinates. In short, you'll have a flexible terminal that will keep up with your needs today—and grow with your operations tomorrow.

Of course, since Magnavox was a leader in the development of plasma terminals, you can be sure your Orion-60 will have a bright, high-contrast display free from jitter and distortion.

There's a lot more you should know about the ways this remarkable terminal can help you get more out of graphic displays. For a demonstration, call or write Tyler Hunt at Magnavox Display Systems, 2131 S. Coliseum Blvd., Ft. Wayne, IN 46803, (219) 482-4411.

Magnavox
DISPLAY SYSTEMS

CIRCLE 117 ON INQUIRY CARD

Microcomputer Adapts To Standalone Or User Control Applications

The PCU 6800 single-card microcomputer for EXORterm/EXORciser processing and control uses is delivered with 1-, 1.5-, or 2-MHz speeds. Multiple memory combinations permit up to 16k of RAM and up to 28k of EPROM or ROM. Each RAM/EPROM or ROM socket is addressable in 32-byte increments.

Memory map space requirement is reduced to only 24 bytes for peripheral addressing. These bytes may be embedded in any memory block area. The gate array's 11-bit address decoding allows the PCU to use smaller portions of the memory map.

Onboard buffers and drivers, which give address, data, and control, provide the interface to the EXORciser bus. Output of VUA or VMA by jumper selection allows the EXBUG debugging board to be used with the microcomputer.

Other components are 40 parallel I/O lines, 3 timers, and an RS-232 interface. Onboard or remote 4-position DIP switch selects 16 baud rates. A flexible clock system is composed of an internal crystal clock with provisions for an X1 external clock input and for external slow and dynamic memories.

Phoenix Digital Corp, 3027 N 33rd Dr, Phoenix, AZ 85017, delivers the board with the MDB 6800 monitor, debugger, and test stimulus generator, in a second ROM, to provide trace instructions, multiple breakpoints, memory plus register display and modification, program execution commands, and test stimulus routines. Signature analysis test techniques perform system test, diagnostics, and troubleshooting. Stimulus software provides complete hardware component test and debug, as well as system test and performance verification.

CIRCLE 423 ON INQUIRY CARD

Total System Bundles Fixed Disc Drive With Microcomputer

Dekchester is an interactive business system packaged by ABC Computers Inc, 500 Tonopah, Tahoe City, CA 95730, with all necessary hardware, software, service, and support. The 36" H x 20" W (91 x 51-cm) system is comprised of a Digital Equipment Corp LSI-11/2 or -11/23 CPU, a CRT video scope, quad I/O port, 17M-byte tape cartridge backup unit, and 20M-byte Winchester drive. Memory consists of 64k bytes. A 40M-byte Winchester disc is optional.

Specifications of the Winchester disc are a 960k-byte/s transfer rate, 2400-r/min rotational speed, and 43-ms average access time. The TC-2000 or DC300A cartridge tape is characterized by a 1600-bit/in (360/cm) phase encoded recording density, 4-track serial record mode, and dual recording head.

Digital Equipment Corp's RT-11 operating system allows execution of BASIC, FORTRAN IV, DBL (DIBOL), Macro II, and Multi-User BASIC. The word processing package is integrated with high speed database storage and retrieval. Accounting software consists of order entry invoicing and inventory control, accounts receivable, accounts payable, general ledger, and an optional payroll program.

CIRCLE 424 ON INQUIRY CARD

Intelligent performance.

The 20 or 80 megabyte Burroughs FD 210 fixed disk subsystem is the newest member of our growing family of intelligent, compatible peripherals for OEM's.

This unit has an average access time of 35 ms and a transfer rate of over 7 million bits per second. An in-built microprocessor controller lets you select the interlace factor to match your system transfer rate. The controller performs high level functions such as asynchronous file search and off-loads the following tasks from your system:

- Track seek and sector location
- CRC generation and check
- Sector relocation
- Error detect/correct
- Confidence/diagnostic tests

By working with a storage subsystem, not just a drive, you get your product to market quickly and easily. The FD 210 has a simple parallel interface and command set for fast integration with your system. It's also interface-compatible with our new 6 megabyte floppy drive, so one interface suffices for both products.

Build the FD 210 into your system. Put it in your cabinet or choose the optional rack mount or free-standing cabinet.

Call or write **Burroughs OEM Marketing,** Burroughs Place, Detroit, MI 48232. (313) 972-8031. In Europe, High Street, Rickmansworth Hertfordshire, England. Telephone 09237-70545.

Burroughs

For General Information Circle 119

For Detailed Specifications Circle 120

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Operating System Handles Access to Online Storage For Multiple Users

The Z80 based AMEX (Altos Multi-User Executive) adapts the ACS8000 series of small computers to permit up to four simultaneous users and hard disc drive control. Compatible with Digital Research's CP/M versions 1.4 and 2.0, the operating system from Altos Computer Systems, 2338-A Walsh Ave, Santa Clara, CA 95050, is written entirely in PL/M. This system requires 64k bytes of memory for one user, 112k bytes for two users, and 208k bytes for four users.

The operating system resides in the upper 16k of the computer's memory. It then uses dispatching and command control software to arbitrate CPU and I/O operations and interactions. AMEX manages a maximum of four user memory areas of up to 48k bytes each; multitasking operations can be performed within any individual block.

With direct memory access hardware, transfers of data between RAM and online floppy or Winchester fixed disc devices are handled outside the CPU by a separate smart controller chip. The use of DMA makes the implementation of any disc configuration transparent to the user.

A priority ordered, interrupt driven dispatching algorithm handles the servicing of each user at the time a console request is received. Fixed time slices are delegated to each user outside of this interrupt-priority scheme so that the user will relinquish control of the CPU during the fixed time slice or be placed at the bottom of the priority queue.

Built-in dispatcher and spooler software modules dynamically allocate and free various peripheral devices that are requested by user programs and commands. A screen oriented text editor (SOE), and 8080 assembler (ASM), file management commands, and a transient-command handler comprise the system utility programs. SOE speeds program modification and software development with features of add, delete, find/replace, block moves and swaps, patching, appending, and file annotation. In addition, an area has been included for the user to implement custom software for specific display devices.

Supporting Z80 assembly language code, the assembler produces object and output listing files. With error checking and diagnostic messages, the file management routines provide directory listings of disc files, list file contents, renumber or erase files, and control the drive's density mode.

The transient-command handler allows the user to define new disc oriented commands, separate from those implemented by CP/M, that the operating system interprets. By extending the operating system environment, the user creates system-level commands for specific applications and constructs predefined I/O control blocks. Other offerings are a full system librarian, debug facility, and submit utility to queue up a series of commands and control the system from a program file.

CIRCLE 425 ON INQUIRY CARD

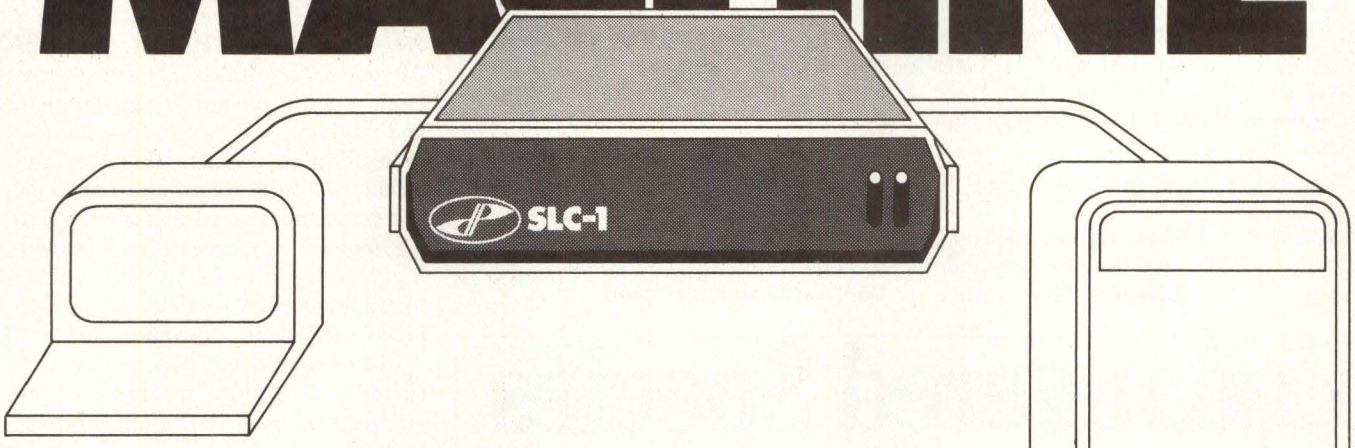
Software Tool Overcomes File Handling Problem Of Large Data Base

Micro-SEED is a CODASYL compatible database management system for microcomputers, running under CP/M with FORTRAN-80 as the host language. Distributed by Microsoft, 10800 NE Eighth, Suite 819, Bellevue, WA 98004, the initial release is written primarily in FORTRAN, with isolated assembly language routines for I/O and buffering. The software system is supported by various 64k 8080/Z80 microcomputer configurations.

CODASYL schema, subschema, and area methods are used to divide and define the data base for easy access from user programs. Database management routines are then called from the user's application programs, written in FORTRAN or other host language.

A compatible subset of the larger SEED system originated by International Database Management Systems, Inc, this system adds such features as self-optimizing Find commands to streamline access to the data base. Scheduled add-ons to the system are HARVEST, a relational query language and report generator, and DBLOOK, an interactive system utility program. CIRCLE 426 ON INQUIRY CARD

THE TIME MACHINE



- Battery supported calendar clock
- Fits all computers via standard RS-232 or 20mA loop serial interface
- No user modification to operating system required
- Dual independently selectable Baud rates
- Automatically provides time when requested by computer
- Automatic time restoration after power failure
- Complete μp computer system
- Optional ten digit display
- Price $640 (single qty.)

For more information on this timely product, contact:

Digital Pathways Inc.
4151 Middlefield Road
Palo Alto, CA. 94306
Phone: (415) 493-5544

DIGITAL PATHWAYS

CIRCLE 122 ON INQUIRY CARD

Portable Software System Compiles And Executes COBOL Programs

CIS COBOL is a software system for compiling, testing, debugging, and executing standard COBOL programs. A compact version requires 32k of RAM, while the standard version uses 48k (see *Computer Design*, May 1979, p 139). Supporting interactive operation, the system is aimed at small business systems. Micro Focus, Inc, 1601 Civic Center Dr, Santa Clara, CA 95051, supplies the package to OEMs under private label if desired, as well as to end users.

A compiler and runtime system, both portable, and interface module comprise the software. The runtime system is usually written in the assembly language of the target microcomputer—Intel 8080 or 8085, Zilog Z80, or DEC LSI-11. The interface modules are specific to the respective operating systems: ISIS-II, CP/M, and RT-11. Optional features are Forms for screen formatting and Forms 2 for program generation.

GSA certification for government use of the CIS COBOL microcomputer version exceeds government specifications for lower intermediate COBOL, a level in advance of many minicomputer COBOL versions. Conformance to the 1974 ANSI standard ensures that application programs will be portable to or from other COBOL machines, regardless of size.

CIRCLE 427 ON INQUIRY CARD

Z80 Operating System Boosts Capabilities Of Microcomputer

Providing a UNIX like tree structure file hierarchy and I/O system, OS-1 is an operating system for the Z80. Release 1.0 is single tasking, but multiple user. It is downward compatible with CP/M, and upward compatible with releases 2.0, 3.0, and UNIX. Multiuser versions 2.0 and 3.0 (multitasking) will support bank select, memory segmentation, and paging.

In addition to examining files and directories, and executing commands, the command processor performs simple logical comparisons and branching. Developed by Electrolabs, PO Box 6721, Stanford, CA 94305, it also performs redirection of standard I/O.

File structure of the software is suited to highly interactive environments, with its multidirectory, multiuser, multifile system. Each tree structure node, which must be a directory, file, or device, contains protection information. Maximum file size is set at 16M bytes, but the number of files with the tree system is practically unlimited. Random file access and dynamic allocation of disc space are used.

Two I/O tables generalize all I/O devices into block and nonblock types. Virtual names assigned to each device are posted in the file system's directories so that there is only one set of names for all devices and files. Thus, a program written to access files also works with any device, and the naming, protection, and searching features of the file system apply to the I/O system. Internal cache buffering and the kernel provide a full set of I/O routines.

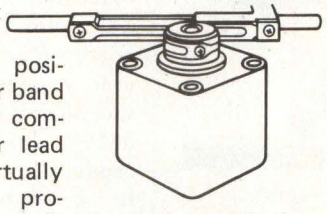
Finally, the operating system provides a software adapter with source code for CP/M. Users may write an adapter program, which is treated as a command for running programs of simple file systems, using a small amount of code.

CIRCLE 428 ON INQUIRY CARD

Five Reasons Why Engineers Rate MPI's Dual-Head Mini "Technically The Best":

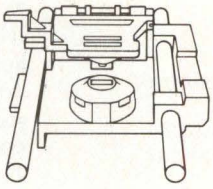
1. BAND POSITIONER

MPI's patented stepper-band positioner provides the industry's fastest access time (5ms) and most accurate positioning. The stepper band is simpler in design compared to a cam or lead screw. It is virtually frictionless, which provides extremely accurate and reliable positioning, yet requires the lowest power. As a result, it moves five times faster than other positioning systems.



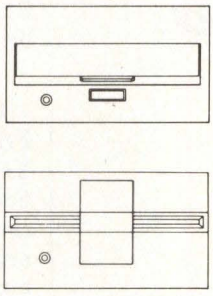
2. HEAD & CARRIAGE

Our high-performance mini floppy drive was developed as a dual-head, double-track, double-density unit. It is not an up-graded single-head, single-density design. The carriage and head concepts are based on IBM's – except for one important innovation: our bottom head is fixed, while only the top head loads. The heads are centered between two parallel rods (not cantilevered) to eliminate radial-positioning errors. To minimize media wear, we designed the longest head carriage which insures flater head landings.



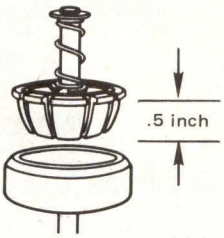
3. HUMAN ENGINEERING

Our dual-head (Model 52) and single-head (Model 51) drives are human engineered. Key features include: a full-closing, push-button front door to provide greater media protection; a patented ejector mechanism that makes diskette removal easier; and a choice of bezels.



4. DISKETTE CENTERING

True diskette centering is accomplished by MPI's proprietary clutch mechanism. As the front door is closing, our extra-long clutch expands and gently engages the mylar media. When the clutch is seated, the diskette is locked securely in position to within .0008 inches. The result: most accurate positioning, longer diskette life, and trouble-free operation. MPI's diskette ejector – an industry first – pops the diskette out within easy finger-tip reach.



5. POWER CONSUMPTION

MPI drives have the industry's lowest power consumption (6W standby, 12W operating) due to the following:

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- A low-friction positioning mechanism.

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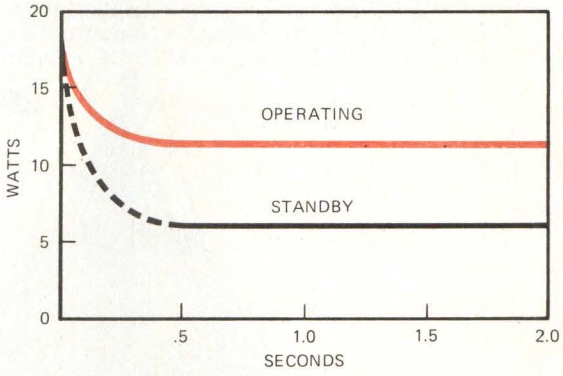

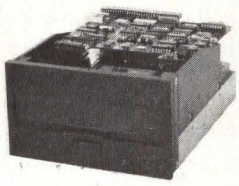

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CIRCLE 124 ON INQUIRY CARD

DS BRIEFS

Analyzer Adds Capability For Testing 6800 Microcomputer—Field interchangeable interface of the T-8 analyzer connects it to the 6800 for hardware and software debugging. The tester single-steps through the microcomputer system development, user, or diagnostic programs; Patuck, Inc, 5073 Russell Ave, Pennsauken, NJ 08109, also provides breakpoint capability. . . . **Memory Offers Add-in Expansion of 16k or 32k Words**—Available from ASR Corp International, 3-15-8, Nishi-shinbashi, Minato-ku, Tokyo 105, Japan, in two versions—16k x 16-bit MSV11-ZC and 32k x 16-bit MSV11-ZD—these memory modules are compatible with the DEC LSI-11/2 and -11/23. Access time is 240 ns. Also included are onboard memory refresh and addressing at any 4k bank boundary through the 0 to 128k address range. . . . **8048 Family Personality Modules Double Microcomputer Analyzer Coverage**—Time-domain analysis, in-circuit emulation, and signature analysis capabilities of the MicroSystem Analyzer-Series 4000 allow functional board and systems testing as well as node level fault isolation of 8021, 8035, 8039, 8041A, 8048, 8049, and 8748 systems. Three pods from Millennium Systems, Inc, 19020 Pruneridge Ave, Cupertino, CA 95014, adapt to support these microprocessors.

Optoelectronic Input Device Functions With Video Board or Terminal—Simplifying communication among the operator, microcomputer, and video screen, the light-pen features response of <100 ns and high resolution for character and graphics displays. The S-100 interface board included by Landmark Systems, Box 5516, Santa Barbara, CA 93108, requires only a video signal input. . . . **Z80 Based Small Business Microcomputer Systems**—R2E of America, 47 Bedford St, SE, Minneapolis, MN 55414, has packaged the model 80-20 as a single-board system with a Z80 CPU; 32k of RAM; two single-sided, double-density minifloppies; ASCII keyboard; and parallel Centronics printer interface. A 1024-character CRT display, BAL language, and a macro assembler complement the system.

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CIRCLE 126 ON INQUIRY CARD

Diskette Hardware System Operates With Single- or Double-Density Recording Formats—Multibus compatible bulk storage system ZX-710/720 includes two Shugart SA801 drives for up to 2M bytes of online data. The Zendex Corp system (6398 Dougherty Rd, Dublin, CA 94566) replaces Intel's MDS-710, 720, 2DS, DDS, and SBC-201, 202, 211, 212 on the MDS-800 and Series II computers . . . .**Operating System, Interpreter, and Database Management System Comprise Z80 Software**—Standalone TIS-Z80 APL for interactive applications using a Z80 based Altos Computer System, Cromemco System III, or Intertec Superbrain has been released by Telecompute Integrated Systems Inc, 251 Spadina Ave, Toronto, Ontario M5T 2E2, Canada. This implementation features monadic and dyadic APL operators, SYSTEM and FILE commands, and online program development . . . .**Magnetic Tape Coupler Interfaces LSI-11 to Dual-Density Imbedded Formatter Tape Drives**—With TM-11 emulation circuitry and handling of Streamer mode operation, the quad-size model DQ130 couples eight drives to one LSI-11 Q-Bus slot. The module from Distributed Logic Corp, 12800-G Garden Grove Blvd, Garden Grove, CA 92643, interfaces with 800-bit/in (315/cm) NRZI, 1600-bit/in (630/cm) PE, or dual NRZI/PE formatted tape transports with speed ranges from 12.5 to 125 in (31.8 to 318 cm)/s.

Assembler/Editor Runs on Computers Using North Star DOS—ASMB-48 develops assembly language programs for Intel 8021, 8022, 8039, 8048, and 8049 single-chip microcomputers, supporting the MCS-48 assembly language instruction set and pseudo-operations. Programs developed on a Z80/8080 host machine must be offloaded to the target processor for test. It may be ordered from Allen Ashley, 395 Sierra Madre Villa, Pasadena, CA 91107 . . . .**Single-Card Computer Serves Communications/Control Applications**—Vantage Data Products, 550 W 200 S, Suite 8, Provo, UT 84601, has assembled the Z80 CPU with serial I/O, parallel I/O, RAM, and EPROM (either 2k 2716 or 1k 2708) on a single card. Asynchronous RS-232 serial communications are programmable at standard baud rates up to 56k. Modem control functions are provided.

Apple Microcomputer Communicates With RS-232-C Serial Devices Via Plug-in Card—Supporting full- or half-duplex operation, the 7710A asynchronous serial interface for the Apple II is fully compatible with Apple PASCAL. Developed by California Computer Systems, 309 Laurelwood Rd, Santa Clara, CA 95050, the card functions with baud rates from 50 to 19.2k, full handshaking, and power-down ROM. . . .**Subsystem Interfaces Digital Cartridge Drive to MicroNova Computer**—DMN-1 cartridge tape subsystem from Alloy Engineering Co, Inc, 908 Concord St, Framingham, MA 01701, connects up to two 1600- or 6400-bit/in (630 or 2520/cm) DEI cartridge drives with Data General MicroNovas. Requiring no card slots or power from the computer, the subsystem allows the drive to emulate a standard 9-track NRZI tape peripheral.

Static RAM Replaces Core Memory for Multibus Computers—ASC-1600 4k-, 8k-, 12k-, or 16k-byte RAM with simple power maintenance circuitry is compatible with Multibus CPU boards and systems. Produced by Alewife Systems Corp, 26 Otis St, Cambridge, MA 02141, the board also functions as a general add-on memory with separately addressable 4k memory banks needing only 0.74 A, 5V. . . . **Digitizer and Software Drawing Package Produces High Resolution, Mass 6-Color Graphics**—VersaWriter has been designed by Rainbow Computing, Inc, 9719 Reseda Blvd, Northridge, CA 91324, to adapt to a variety of applications, acting either as a pointer or as a digitizer. Sixteen commands control cursor movement, horizontal and vertical scaling, and centering on the screen . . . .**Multibus Dynamic RAM Board Holds 32k Bytes**—Electronic Solutions, Inc, 5780 Chesapeake Ct, San Diego, CA 92123, has introduced RAM-032, which is compatible with Intel's iSBC-80 Multibus. Memory access time is 450 ns.

Buffered, Expandable 6800 Microprocessor Combines With Onboard Memory Sockets—The 7802 processor card, which interfaces with memory, I/O, and peripheral cards produced by Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940, expands a STD BUS system to full 6800 memory and I/O capacity. Memory consists of 1024 bytes of RAM with sockets for up to 4096 bytes of RAM and 8192 bytes of ROM or EPROM. . . . **Standalone Interface Requires Minimal Software Support From Host CPU**—STD BUS compatible System Video Interface 1 consists of a 64 x 16 format video interface, 8-bit keyboard and 4-bit parallel input ports, and 8-bit parallel output port. Spurrier Peripherals Corp, 10513 Le Marie Dr, Cincinnati, OH 45241, has incorporated screen refresh RAM and system clock circuitry on the single-board peripheral. . . . **Power Supply Outputs Five Voltages For Microcomputer Systems**—Used with microcomputers, single or dual Shugart floppy disc drives plug into output connectors on the power supply board, which has metal pass transistors, cermet ports, and ceramic ICs. Introduced by CEI Corp, PO Box 501, Grenier Industrial Pk, Londonderry, NH 03053, model FD502 offers 5 Vdc at 5 A, 12 Vdc at 1 A, −5 Vdc at 3/4 A, −12 Vdc at 1/2 A, and 24 Vdc at 1.5/4 A.

Floating Point Support Subroutines Run On Z8002 Microcomputers—Using a 32-bit binary floating point format, reentrant and interruptible subroutines provide fast arithmetic operations (200 to 400 μs), integer-float and float-integer conversions, float-ASCII string representation, and ASCII-string float conversions. The format used by Hemenway Associates, Inc, 101 Tremont St, Suite 208 Boston, MA 02108, gives between 6 and 7 digits of precision . . . .**CPU/Memory On Same Board Eliminates Timing Problems and Bus Noise**—Model Z80/64 features a Z80 microprocessor and 64k bytes of dynamic RAM, with provisions for 2k of EPROM and vectored interrupts. Transparent refresh occurs during unused processor time. Single-board design by CMC Marketing Corp, 10611 Harwin Dr, Suite 406, Houston, TX 77036, allows full 4-MHz operation with no wait states.

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CIRCLE 127 ON INQUIRY CARD

Software Adapts Microcomputer to Test Run COSMAC 1802 Programs—COSAPPLE, an 1802 simulator and debug package, permits a 16k or larger Apple II 6502 based computer to run programs coded in 1802 machine language. Developed by Dann McCreary, Box 16435-V, San Diego, CA 92116, the package aids checkout of modest 1802 applications, with the user controlling every aspect of 1802 operation. . . . **Powerful Single-Board Computer Supports CP/M and Pascal**—The 64k TCB-85 Multibus compatible microcomputer, manufactured by DOSC, Inc, 500 Fifth Ave, New York, NY 10033, contains dual-density floppy disc controller, CRT controller, RS-232 serial I/O port, parallel printer interface, and strobed or scanned keyboard interface . . . . **Interactive Programming Language Possesses Powerful Primitive Functions**—Comparable to full APL, SOFTRONICS APL (36 Homestead Ln, Roosevelt, NJ 08555) operates under the CP/M, residing in 30k bytes of memory. The interpreter runs in a variety of character set configurations, including standard ASCII.

Assembly Language Test Diagnoses and Repairs Memory Systems—A user interactive memory diagnostic of 14 tests and 6 combinations, selected by a single command, runs on 8080, 8085, and Z80 systems using 3k bytes. Eagles Computer Works, PO Box 22664, Denver, CO 80222, supplies a manual that relates the MEMDOC diagnostic to memory testing. . . . **STD BUS Compatible RAM and EPROM Cards Operate From Single 5-V Power Source**—SRC-2712 handles up to 16k bytes of AMD's 9124 or 2114 RAM with 300-ns access time. The second card released by Northwest Microcomputer Systems, 749 River Ave, Eugene, OR 97404, SPC-2714, handles up to eight 2716 EPROMS or combined EPROM/RAM. Access times range from 350 to 450 ns.

Trainer Aids Microcomputer Analog Signal Interfacing—EID-1 Experimental Interface Designer connects to MMD-1 or -2 microcomputers from E&L Instruments, Inc, 61 First St, Derby, CT 06418, or adapts to other 8080 based microcomputers. I/O signals are provided or simulated by built-in components; analog signals converted to digital input can be displayed via LED readout . . . . **FORTRAN Cross Assembler Handles Z80 Instruction Set**—Standard Z80 mnemonics and all standard Z80 instructions are supported by the cross assembler, available from Tufts University, Dept of Chemistry, Medford, MA 02155, on floppy disc or paper tape. Output of the assembler, which can run on a PDP-11 under RT-11, is a listing and a binary file which can be downline loaded into a minimal Z80 system. □

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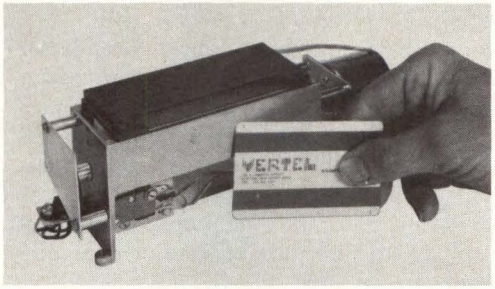

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MEETING EPROM REQUIREMENTS OF ADVANCED MICROPROCESSORS

Tim Coffman

Texas Instruments, MOS Memory Division
Houston, Texas

Increased performance requirements for semiconductor memories result naturally from advances in microprocessor capabilities. High performance microprocessors are much faster than their standard counterparts, requiring access times usually on the order of 360 ns or less. This allows less time for decoding of chip selects and acquisition of data from the memory device. Thus, the total propagation delays of memory control signals and data become more significant at these speeds.

Access Problems of High Performance Microprocessors

A typical memory read timing diagram for a high performance microprocessor (Fig 1) shows that maximum interval of 310 ns is available to present valid data after address is stable. Since conventional 5-V EPROMs have worst case access times no faster than 350 ns from address stable and chip enable, it would be possible to read invalid data from the memory because it is accessed 40 ns before data are guaranteed valid. In general, standard nonvolatile MOS

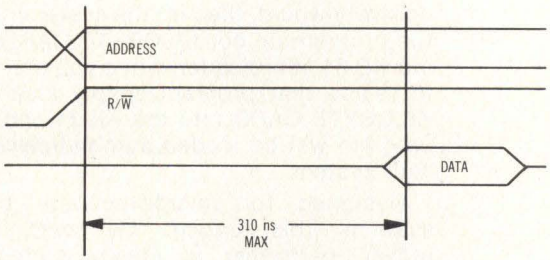

Fig 1 Memory read timing diagram. Typical high performance microprocessor makes available 310-ns max interval from address stable to data valid. Speeds in this range pose problems for standard nonvolatile MOS memories

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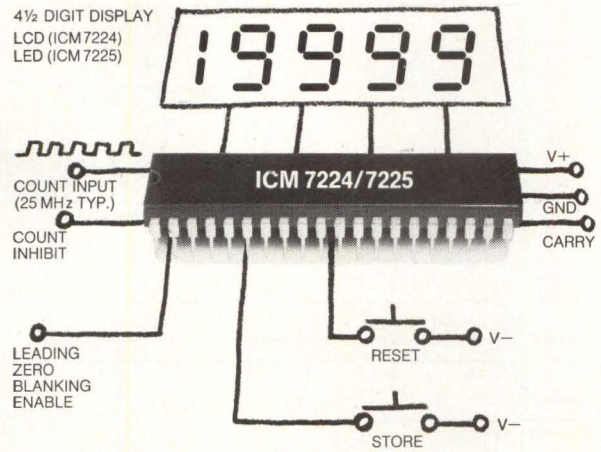

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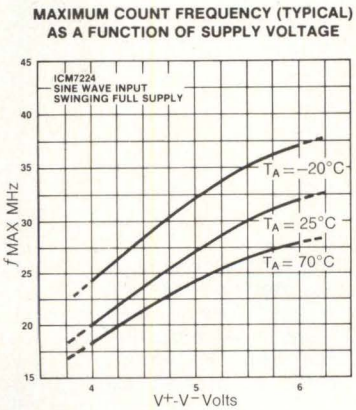

The ICM7224 offers high frequency counting, (15MHz guaranteed; 25MHz typical at 5V). For those applications that require low frequency counting, down to DC, a Schmitt trigger on the count input allows accurate operation in noisy environments or with slowly changing inputs.

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memories are not fast enough for use with advanced microprocessors because of their long access times.

One situation that exemplifies the design problem inherent in the use of standard EPROMs is indicated in Fig 2. In this simplified system a 512 x 8 bipolar P/ROM is used for decoding chip select and power-down functions. A significant savings in power is realized from this common practice, because the EPROM remains in standby mode until accessed. However, the P/ROM expends some of the available access time for address decoding. The P/ROMs max access time is 60 ns, thus microprocessors with 310-ns memory access time would require EPROMs with 250-ns max access, thereby excluding conventional EPROMs for this application.

A relatively inefficient way to utilize slower EPROMs with high performance microprocessors involves the introduction of synchronous wait states to extend the memory read access time. However, the minimum amount of time that can be added is one clock period, in this case 500 ns (Fig 3). A memory access then would take 810 ns—a much larger interval than most EPROMs would require. If the average instruction requires four clock cycles, a wait state with every instruction fetch would add 25% to program execution time. This effect becomes even more pronounced in systems involving considerable memory access, such as interactive graphics, word processing, communications, and some realtime applications.

In general, a design that uses a standard EPROM with a high performance microprocessor seriously reduces the effectiveness of that microprocessor. In some cases it might become necessary to reduce the microprocessor's operating frequency until the memory's worst case conditions are met. However, slowing the clock frequency defeats the purpose of using a high performance microprocessor in the first place.

One solution to the problem can be found in the use of bipolar memories. However, in most implementations, bipolar P/ROMs would represent an overkill, since they provide more than twice the access speed required by a high performance microprocessor. In addition, their cost would

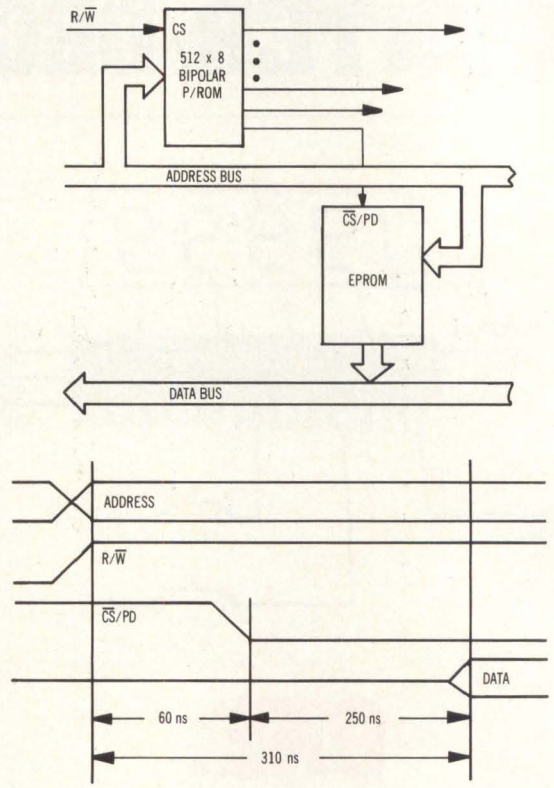

Fig 2 System using P/ROM address decoder with EPROM. Decoder reduces available EPROM access time by 60 ns, placing further burden on EPROM performance

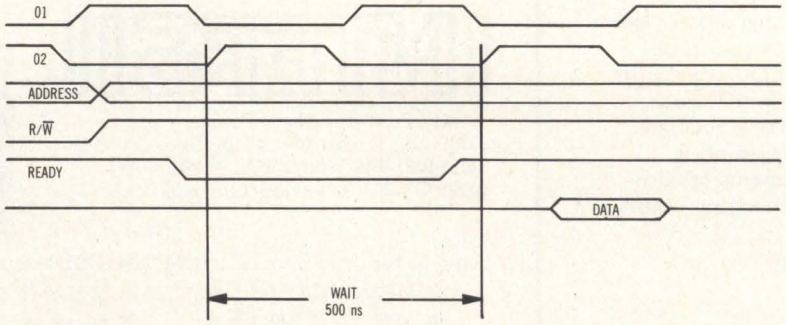

Fig 3 Introducing synchronous wait states. Addition of one clock cycle wait state on read allows EPROM to catch up with microprocessor. However, system speed is slowed excessively

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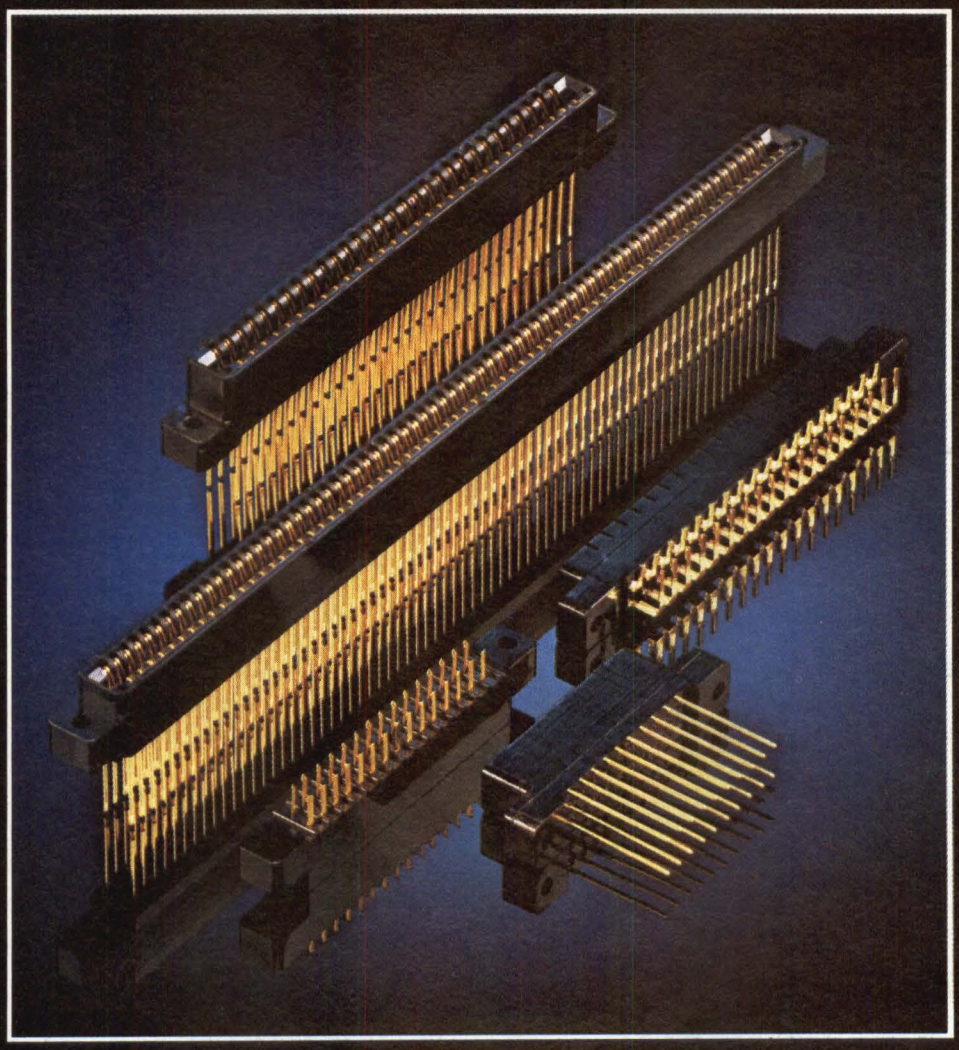

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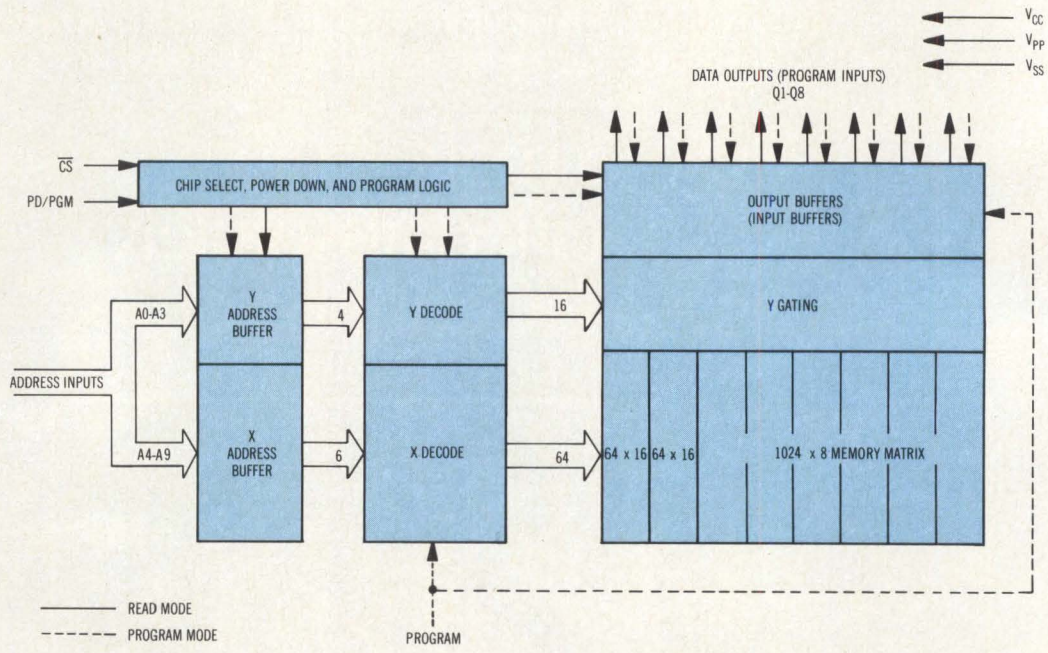

be higher than that of comparable MOS memories, including such factors as the costs of programming and power supplies. The P/ROM's nonerasability is a major disadvantage. Other penalties associated with the bipolar solution include power dissipations above 500 mW.

High Speed MOS Approach

The straightforward solution is the development of high speed MOS EPROMs, capable of providing the required access times. Evolving design and process methods have contributed to across the board improvements in MOS memory fabrication.

One example of this advancing technology is the TMS 2508 (Fig 4), a memory that has been added to the Texas Instruments 5-V EPROM family. This device, designed as an 8k memory (rather than being a partially functional 16k) is believed to have the highest EPROM speed and smallest 8k bar size in existence, occupying less than 15k sq mils (9.7 mm^2) of silicon.

Parameters of this device include maximum access time of 250 ns for the fastest version, maximum power dissipation of 446 mW active and 131 mW on standby, full TTL compatability, and a 3-state output for OR-ties. Organized as 1k x 8, the memory is fully static, with maximum access time equal to cycle time, and offers automatic chip select and power-down. With regard to the design problem posed in this column, this device satisfies the requirements of high performance microprocessors.

Continuing advances in microprocessor speed requirements and in memory design will maintain this evolution's momentum, and will lead to further design tradeoff considerations. As processor speed requirements reach the point where bipolar memory speeds are appropriate (rather than overkill), and as bipolar energy requirements are reduced, MOS EPROM designs will need to advance to stay competitive with bipolar memories. The required advances will be facilitated by the fact that EPROMs and MOS microprocessors draw on the same evolving technology. The memories will continue to track the processors in the future.

Summary

Advances in memory technology allow EPROMs and other memory types to follow a learning curve with respect to such major parameters as bar size, timing, and power dissipation. Even faster and lower power devices in higher densities can be expected in the near future. Just as MOS static RAMs have achieved access times in the bipolar realm, EPROMs can be expected to approach bipolar speeds. These evolving memories will play a major part in fulfilling the requirements arising from microprocessor advances.

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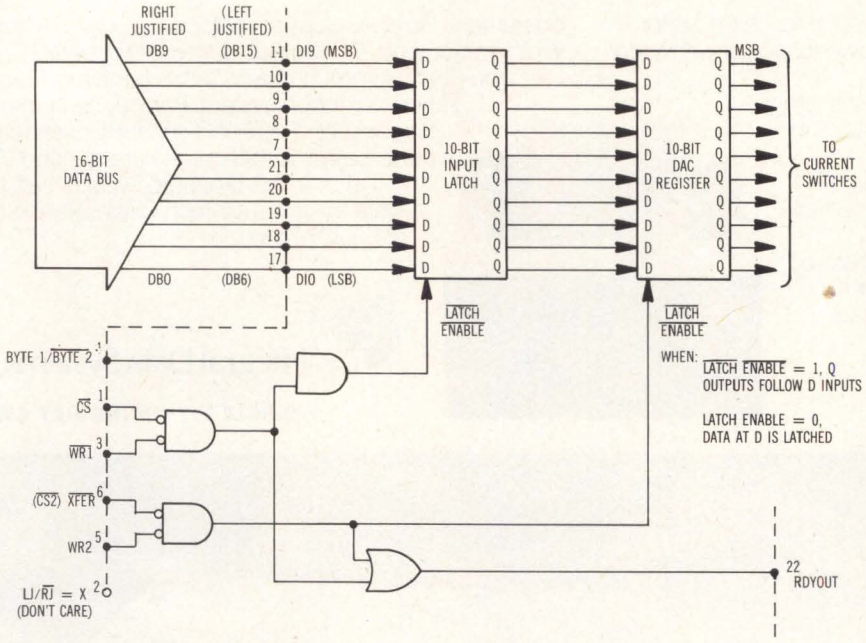
CIRCLE 131 ON INQUIRY CARD

10-Bit Double-Buffered Multiplying DACs Offer Processor Compatibility



Digital to analog converter, DAC1000-1002 from National Semiconductor. Diagram shows input connections and logic for use with 16-bit data

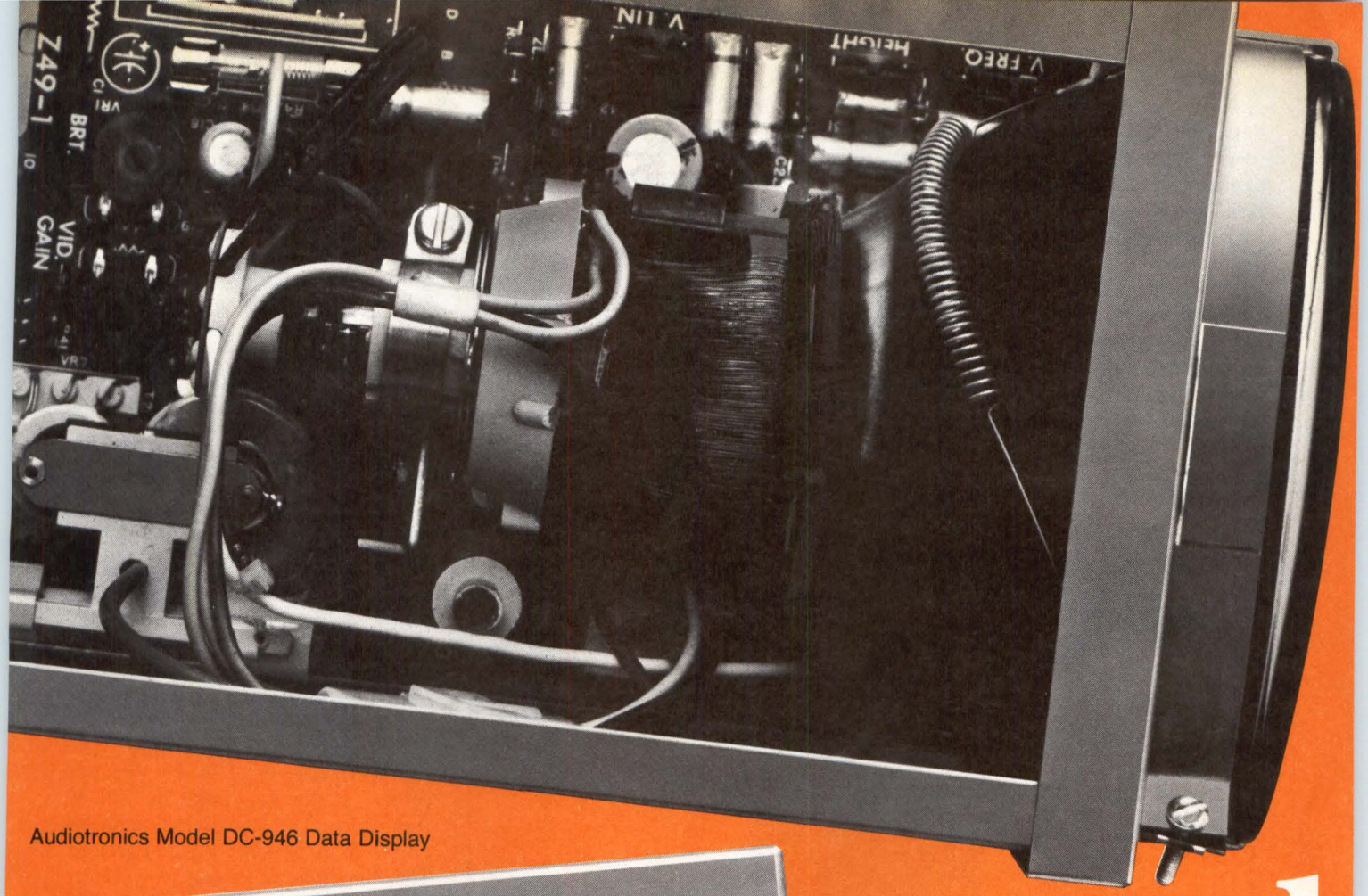
Accuracies of 8, 9, and 10 bits are available in the MICRO-DAC™ series of 10-bit resolution, CMOS, 4-quadrant multiplying digital to analog converters produced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051. These devices are double buffered and can load two 8-bit bytes with the data format either right or left justified. The MDACs appear as memory locations or I/O ports to a microprocessor, and are designed to interface directly with the 8080, 8048, 8085, Z80, and other processors. However, they can also operate on a standalone basis without a microprocessor. They are intended to fulfill the need for low cost microprocessor DACs in servo control, programmable gain amplifier, digital attenuator, and synchro to digital converter applications.

The 24-pin DAC1000, -1001, and -1002 (offering accuracies of 10, 9, and 8 bits, respectively) represent the top of the line, providing all available logic features of the series, including the capability of loading all ten bits simultaneously. They provide a RDYOUT output signal for introducing a wait state to accommodate high speed microprocessors having write strobes narrower than 100 ns.

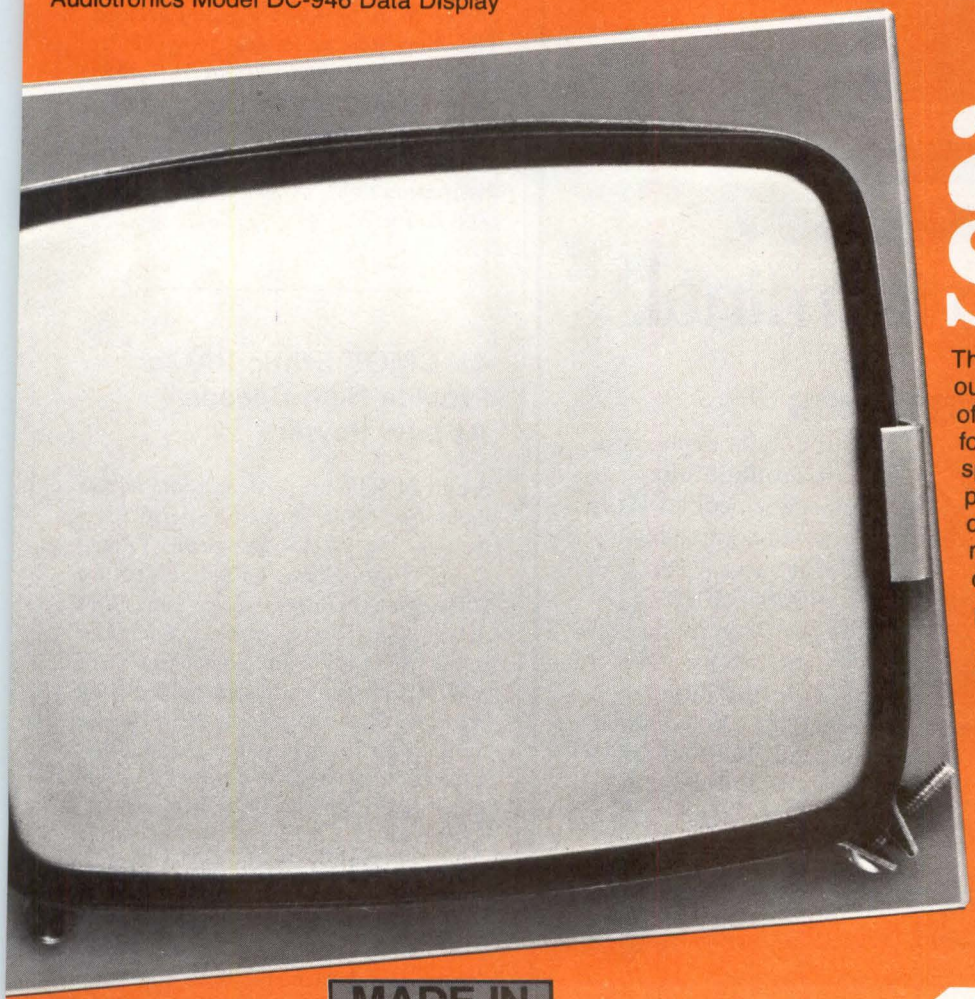
Specified for use with right-justified data, the 20-pin DAC1003, -1004, and -1005 make up a second subfamily of 10-, 9-, and 8-bit accuracies. Similarly, the 10-, 9-, and 8-bit accurate DAC1006, -1007, and -1008 operate with left-justified data, and are also provided as 20-pin DIPs.

Additional features of the family include a current settling time of 500 ns (typ), gain tempco of 0.0003% FSR/°C, and typical power dissipation (including ladder) of 30 mW, operating from a single 5- to 15-V supply and drawing only about 600 μA from a 10-Vdc reference supply. Logic compatibility between these devices and standard TTL levels is achieved through the use of a special biasing circuitry onchip that makes use of the parasitic NPN bipolar transistors which are inherent in the complementary MOS structure. The logic inputs meet TTL voltage level specifications, having 1.4-V logic threshold, independent of V_{CC}. All options make use of standard microprocessor control signals, and the data on the bus can be read by the computer in a standard write cycle.

The analog section is identical to the industry standard non-microprocessor compatible AD7520 (DAC1020). Addition of the buffers for the digital input



Audiotronics Model DC-946 Data Display



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data not only allows for storage of these data, but also provides a way to assemble the 10-bit input data word from two write cycles when using an 8-bit data bus, without affecting the analog output. Furthermore, the double buffering allows many DACs in a system to store current data as well as the next data. Updating each converter is also not time critical. When all DACs are updated, a common strobe signal can be used to cause them to change simultaneously to their new analog output levels.

Data formatting is handled by providing flexibility in the way the digital data are entered into the input latch. To allow operation with either an 8-bit (two write cycles) or a 16-bit (one write cycle) data bus, all 10 locations of the input latch are enabled on the first write cycle from the microprocessor. Then, depending on the data format, the next write cycle, if used, will overwrite two of these locations with the proper data.

The CMOS-implemented series has none of the basic problems inherent in similar bipolar designs. These devices have virtually infinite current gain and, therefore, have no alpha or beta errors. Also, there is no analog term to offset voltages in these products. Rather, an ON CMOS switch is used, which looks like a small value resistor, with its resistance value controlled by device geometry.

To avoid the temperature coefficient and piezoresistive problems of diffused resistors, silicon chromium thin film resistors are used, which track to within 1 ppm, insuring excellent initial matching and temperature tracking characteristics. A feedback resistor, normally required with an external op amp, is provided onchip to maintain a low temperature coefficient of the gain or full scale reading.

Absolute maximum ratings limit supply voltage (V_{CC}) to 17 Vdc and voltage at the V_{REF} input to ± 25 V, with voltage at any digital input required to lie between V_{CC} and ground. The allowable operating temperature range is -40 to 85 °C for LCD-suffix and -55 to 125 °C for LD-suffix parts. In storage, temperature must remain between -65 and 150 °C. Package dissipation at $T_A = 25$ °C must not exceed 875 mW.

4k CMOS Static RAMs Provide High Speeds At Low Powers

A pair of 4096-bit static random access memories from Fujitsu Micro Electronics Inc, 2945 Oakmead Village Court, Santa Clara, CA 95051, feature 250-ns (max) address access times and 370-ns (max) cycle times. Maximum power dissipation for both chips is 17 mW/MHz in operation and 275 μW on standby. These chips are suited for use in microprocessor systems and other applications where low power dissipation and high performance are required.

The MB8404E, organized as 4k x 1, is a plug-in replacement for the industry standard 6504. Organized as 1k x 4, the MB8414E can replace the industry standard 6514. Both RAMs are provided in 18-pin DIPs.

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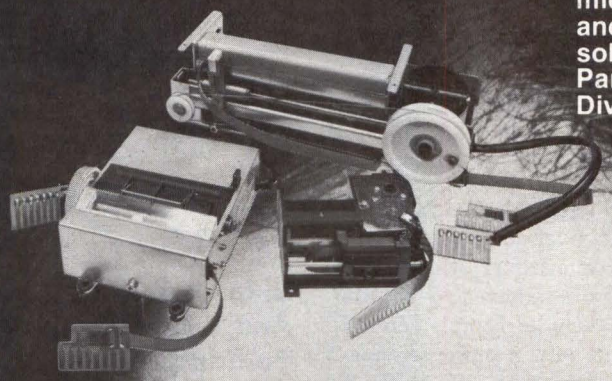

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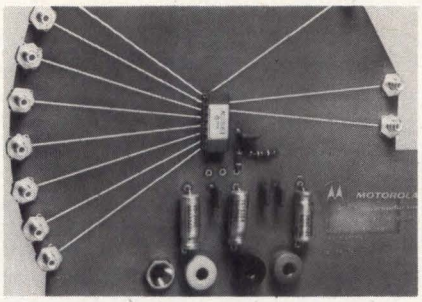


Board illustrates layout technique necessary to evaluate operational performance of Motorola Semiconductor's MC10318L9. 8-bit DAC provides 9-bit accuracy

Featuring a 15-ns settling time, 51-mA full scale output current, and MECL 10k compatible inputs, the 9-bit accurate MC10318L9 digital to analog converter finds applications in high speed instrumentation and communication equipment, display processing, storage oscilloscopes, radar processing, and TV broadcast systems. This 8-bit DAC from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, is a 9-bit accurate follow on to the MC10318L, an 8-bit DAC of 8-bit accuracy produced by the same manufacturer.

The recently announced converter guarantees ±0.10% maximum nonlinearity over the 0 to 70 °C temperature range. Operation from a standard −5.2-V supply, MECL input capability, and an output compliance range of −1.3 to 2.5 V allow convenient interfacing between high speed processors and video level circuitry.

Other characteristics, which this monolithic chip shares with its predecessor, include complementary current outputs and a power dissipation typically less than 500 mW. A board using microstrip layout techniques is available for evaluating the operational performance of the chip.

The device is provided in a standard 16-pin ceramic DIP, priced at $45.00 in quantities of 100 to 999. Maximum ratings require that power supply voltage V_{EE} lie between −6.0 and 5 V, with digital input voltage, V_I, constrained to a range from zero to V_{EE}. The upper limit on applied output voltage is 5.0 V. Reference current (I_{ref}) and output current (I_{FS}) must not exceed 5.0 and 75 mA, respectively. The allowable temperature range is 0 to 70 °C in operation and −65 to 150 °C in storage. CIRCLE 351 ON INQUIRY CARD

Chip Uses NBS Algorithm And 56-Bit Key Variable To Encrypt/Decrypt Data

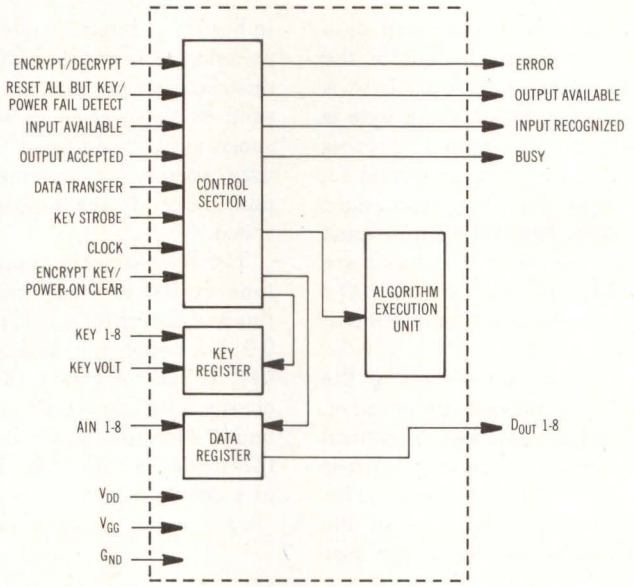
Based on an N-channel silicon gate process, the MC 884 data encryption chip uses the National Bureau of Standards Data Encryption Standard algorithm to encrypt or decrypt 64 bits of data per encryption cycle, based on a 56-bit key variable stored in the key

register of the chip. Once loaded in the chip, the key variable cannot be accessed.

Operating at 1.25 MHz (max), the device accepts either synchronous or asynchronous inputs. This chip is normally used in conjunction with an encryption control chip, MC 883, issued by the same company, Burroughs OEM Marketing Corp, Burroughs Pl, Detroit, MI 48232.

In the encryption process, the key can be encrypted before the key register is loaded. To encrypt the key, the encrypt key line should be set at high and the key will be loaded in the chip via the data input lines. In this case, the key is treated as data and is encrypted with the key variables present in the key register. The encrypted key byte is transferred to the key register as a new data byte is loaded into the data register.

When eight bytes of data are loaded in the chip, the encryption process begins. The BUSY signal remains at high level until the encryption process is complete. Upon completion of the encryption, BUSY returns to a low level and the OUTPUT AVL signal goes high. At this point, the encrypted byte can



Data encryption chip, MC 884 from Burroughs. NMOS device utilizes 56-bit key

be unloaded and a plain byte of data can simultaneously be loaded in the chip. As the eighth encrypted byte is unloaded and the eighth plain byte is loaded, a new encryption process begins. If the encryption process is required to start with less than eight bytes, the DATA TRANSFER input must be set to a high level while the data are being loaded in the chip. DATA TRANSFER goes low upon completion of data loading.

An error output is activated if the key or data shift lines are inoperative, or if an illegal combination of control functions occurs, or if a parity error is found on a key byte. A parity error does not affect the operation of the chip, so it can be ignored if the user chooses.

Other characteristics of the device include TTL compatibility, a system reset affecting everything but the key, and a battery backup option to prevent the destruction of the key variables upon power failure. Absolute maximum ratings limit negative voltage on any pin to −0.3 V, while positive voltage is limited to 16 V on V_{GG} or any input pin and to 8 V on V_{DD}, KEY VOLT, or any output pin. Temperature must stay between 0 to 70 °C during operational and between −55 and 150 °C in storage.

CIRCLE 352 ON INQUIRY CARD

16- and 8-Channel Analog Multiplexers Operate at High Speeds

Two additions to an existing family of high speed multiplexers are claimed to be the fastest monolithic analog MUXs presently available, and are also said to provide the best dc accuracy available on the market in monolithic form. The HI-516 16-channel and HI-518 8-channel versions can both be operated in either single-ended or differential modes, with selectable logic levels.

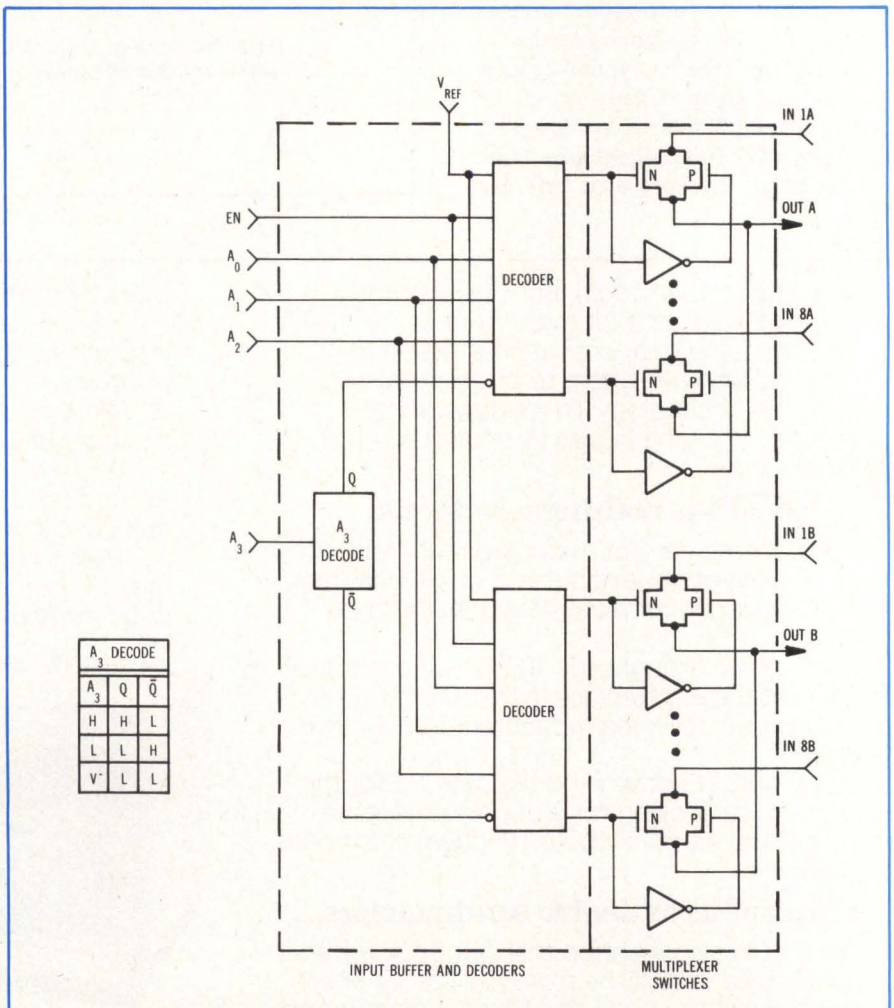
These products from Harris Semiconductor Products Div, PO Box 883, Melbourne, FL 32901, find application in high speed data acquisition systems, avionics, electronic warfare, and industrial process control. Fast devices such as these allow increased system speed at little additional cost. In many data acquisition systems, the analog multiplexer is the limiting factor for speed.

The 16-channel chip offers an access time of 100 ns (typ) and typ settling times of 250 ns (to 0.1%) and 800 ns (to 0.01%). Low output leakage current, I_D OFF, is 100 nA (max), full range, and charge injection is 0.33 pC (type). Maximum allowable power dissipation for this device is 1200 mW. It is provided in a 28-pin DIP.

An access time of 80 ns (typ) characterizes the 8-channel part. Low output leakage current, I_D OFF, is 50 nA (max), full range. Settling time and charge injection parameters are the same as those for the 16-channel model. Provided in an 18-pin DIP, this MUX has a max allowable power dissipation of 725 mW.

Each of the chips is offered in three models. Commercial versions (suffix -5) are rated for operation from 0 to 75 °C, military versions (suffix -2) are rated from −55 to 125 °C. Military versions having -8 suffix are processed to MIL-STD-883, Class B screening.

CIRCLE 353 ON INQUIRY CARD



A_3 DECODE		
A_3	Q	$\bar{Q}$
H	H	L
L	L	H
V⁻	L	L

Functional diagram of Harris Semiconductor HI-516 analog multiplexer. Device can be used as single-ended 16-channel MUX or as dual 8-channel differential MUX

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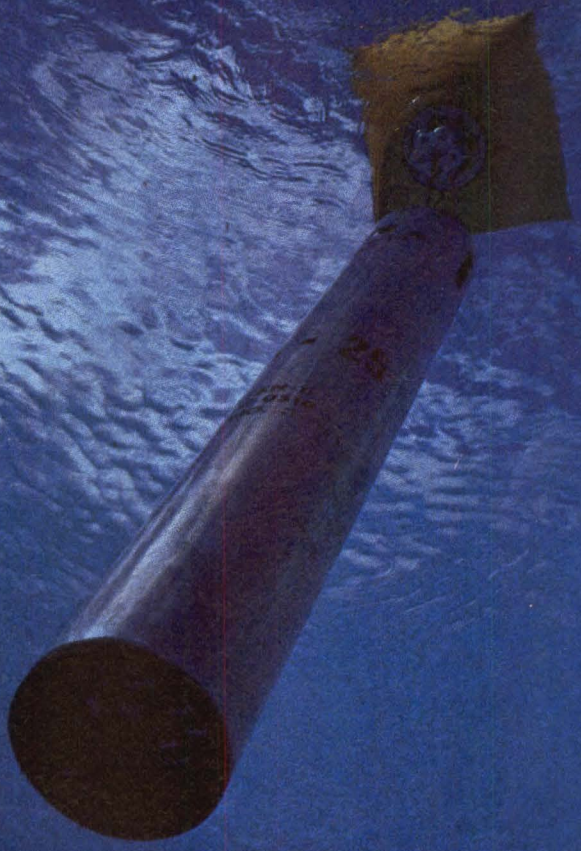

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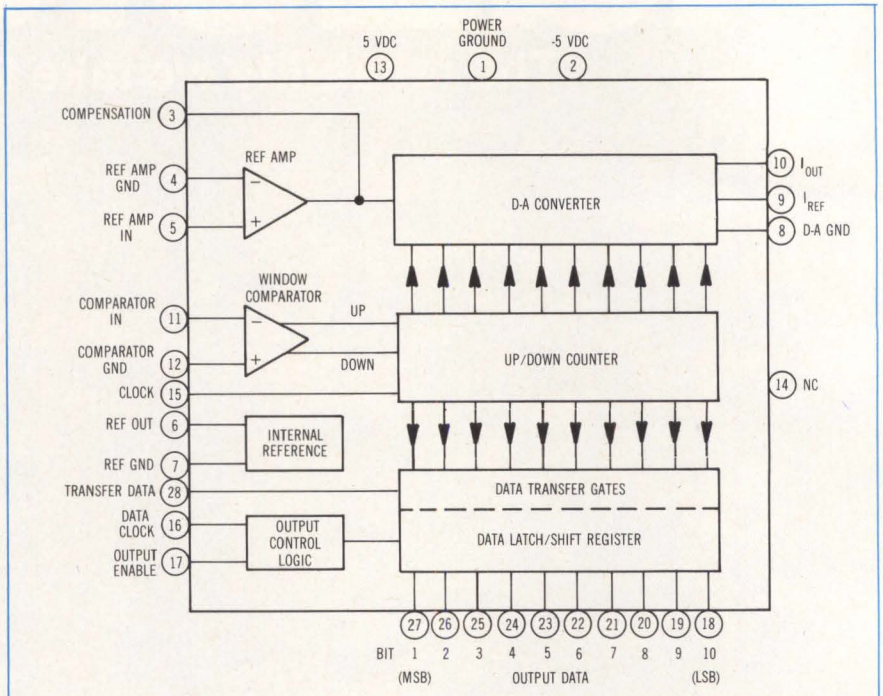
10-Bit Continuous Tracking ADC Runs 10^6 Conversions/s



A-D converter ADC-856 from Datel-Intersil provides 10-bit resolution and ± ½-LSB max linearity error

A 10-bit tracking analog to digital converter announced by Datel-Intersil, 11 Cabot Blvd, Mansfield, MA 02048, supplies continuously updated conversion data on full scale sinusoidal signals up to 300 Hz without the need for a sample and hold. The ADC-856 is linear to ±½ LSB (max) and is monotonic over its entire operating temperature range.

This circuit is implemented in bipolar, monolithic form, and contains a fast window comparator, tracking logic, an up-down counter, a D-A converter, a precision voltage reference with amplifier, data transfer gates, and a data latch/shift register. External parts required for operation have been held to a few passive components, allowing external programming of the analog input voltage range. Gain temperature coefficient of the circuit is ±10 ppm/°C, exclusive of reference.

The chip is optimized for operation in a continuous tracking mode. In this conversion technique each conversion of an analog signal is based on the last converted value of that signal. For signals that do not vary faster than the converter can track (1 LSB/μs), continuous tracking will provide a valid, updated conversion result every microsecond.

Logic control inputs contribute to this device's usefulness in many different applications. Data transfer gates allow selection of the rate at which the output latch/shift register is updated. The rate may vary from once every microsecond to updating only upon receipt of a command from an external controller. External control also allows selection of output data form, which may be parallel or serial (by supplying an optional clock input). Outputs may be disabled completely in either mode by holding the device's output-enable input low.

The ADC operates on ±5-Vdc power at 50 mA with a power supply rejection of 0.1%/V. It is packaged in a 28-pin ceramic DIP and is available in two operating temperature ranges: 0 to 70 °C (commercial) and −55 to 125 °C (military). Maximum ratings limit supply voltage to ±7 V and logic input voltage is required to lie between 0 and V_{CC}.

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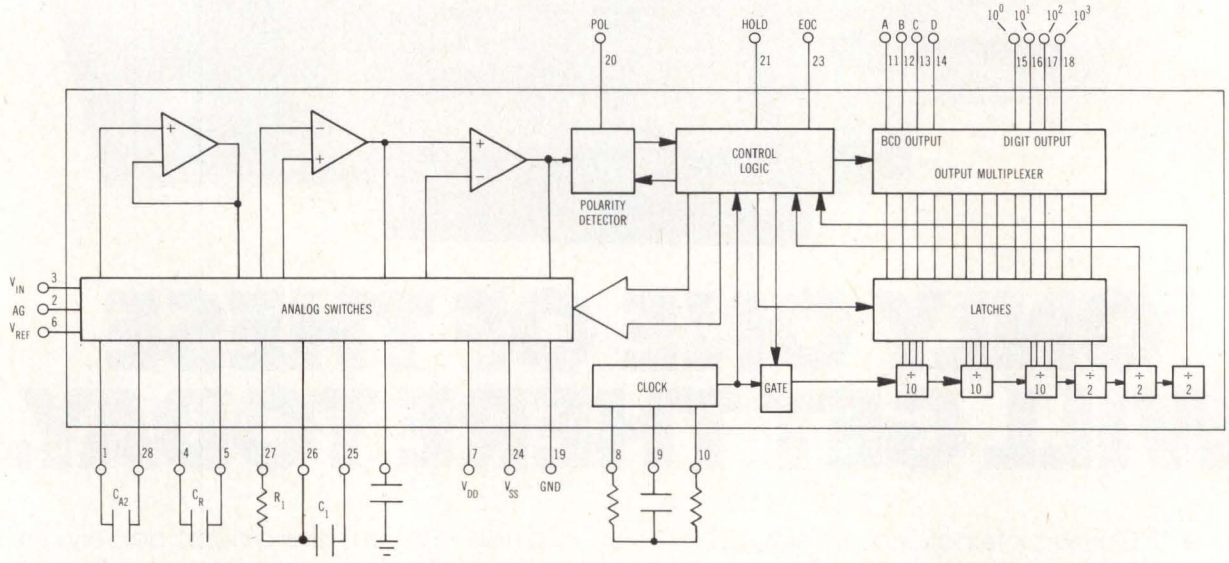
CIRCLE 138 ON INQUIRY CARD

Monolithic ADC Outputs 3½ Digits Plus Multiplexed BCD



Teledyne Semiconductor's 8751 3½-digit multiplexed ADC. Multiplexer outputs BCD or digital output

A monolithic CMOS analog to digital converter, produced by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, provides multiplexed BCD data outputs and 3½-digit outputs. It is appropriate to applications where high power LEDs and gas discharge displays are used and where microprocessor or printing interfacing is required. The circuit also finds uses in low power panel meter applications.

This chip, the 8751, contains a dual slope A-D converter and all digital circuitry necessary to provide a multiplexed BCD output. An external resistor and capacitor determine the internal clock frequency, allowing up to 15 conversions/s. Also, an internal network of analog switches provides logic output for polarity (auto-polarity) and compensation for internal offsets (auto-zero) during each conversion cycle.

The display reading may be held at any time by applying a logic 0 to the display hold input. This has no effect on the conversion cycle. The display automatically blanks when the input voltage exceeds full scale (F/S) for the selected input range. This range is set by the reference voltage, ie, F/S = 1.999 V for V_{REF} = 1.0 V, and 1.999 mV for V_{REF} = 0.1 V.

Other features include an end of conversion signal, a low input noise of 30 μV (typ), low input current of 10 pA (typ), and power consumption of 10 mW (typ). The device can be used with either an internal or external clock.

Absolute maximum ratings limit power dissipation to 1200 mW, derated by 12 mW/°C above 50 °C. Voltage limitations require that V_{DD} relative to ground lie between −0.3 and 6.5 V and that ground relative to V_{SS} lie between −9.0 and 0.3 V. Temperature must remain between −40 and 85 °C in operation and between −65 and 150 °C in storage. Clock frequency must not exceed 60 kHz. The device is provided in a 28-pin plastic or ceramic DIP.

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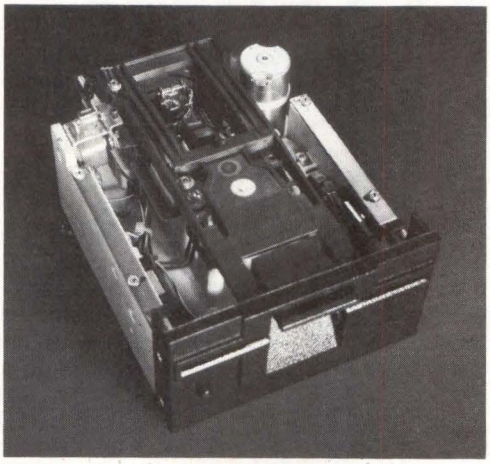
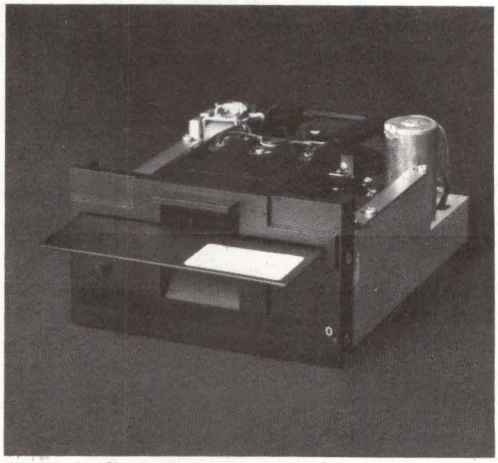
We'll take on any floppy in this magazine, head to head to head.



FD250



FD200

Judge for yourself.

Flip through this magazine and look at anyone else's advertising for 5¼" floppies. Then compare.

Our FD-250 is a double-headed wonder. It can replace the Shugart SA 400, take your on-line capacity to 437.5K bytes and not need a single screw hole re-machined.

More importantly, we can deliver them to you immediately...in quantity. Because we're already shipping them in quantity.

Our FD-200 is the single-headed 5¼" floppy answer to your system. Up to 250K bytes per side. Forty tracks. Available in quantity now.

And just in case you can't find a lot of contenders in this magazine, neither did we.

For sales information, call (213) 996-1333 (Western Region); (603) 883-2100 (Northern Region); or (305) 784-5220 (Southern Region). For technical information, call (213) 999-2020, Ext. 281. Or write Pertec Computer Corporation, 21111 Erwin Street, Woodland Hills, Ca. 91367.

PCC PERIPHERALS
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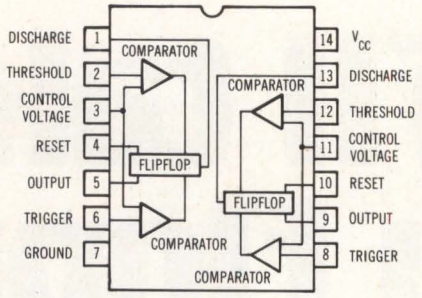
Dual Independent Timers On Single Chip Cut Power Use by 94%

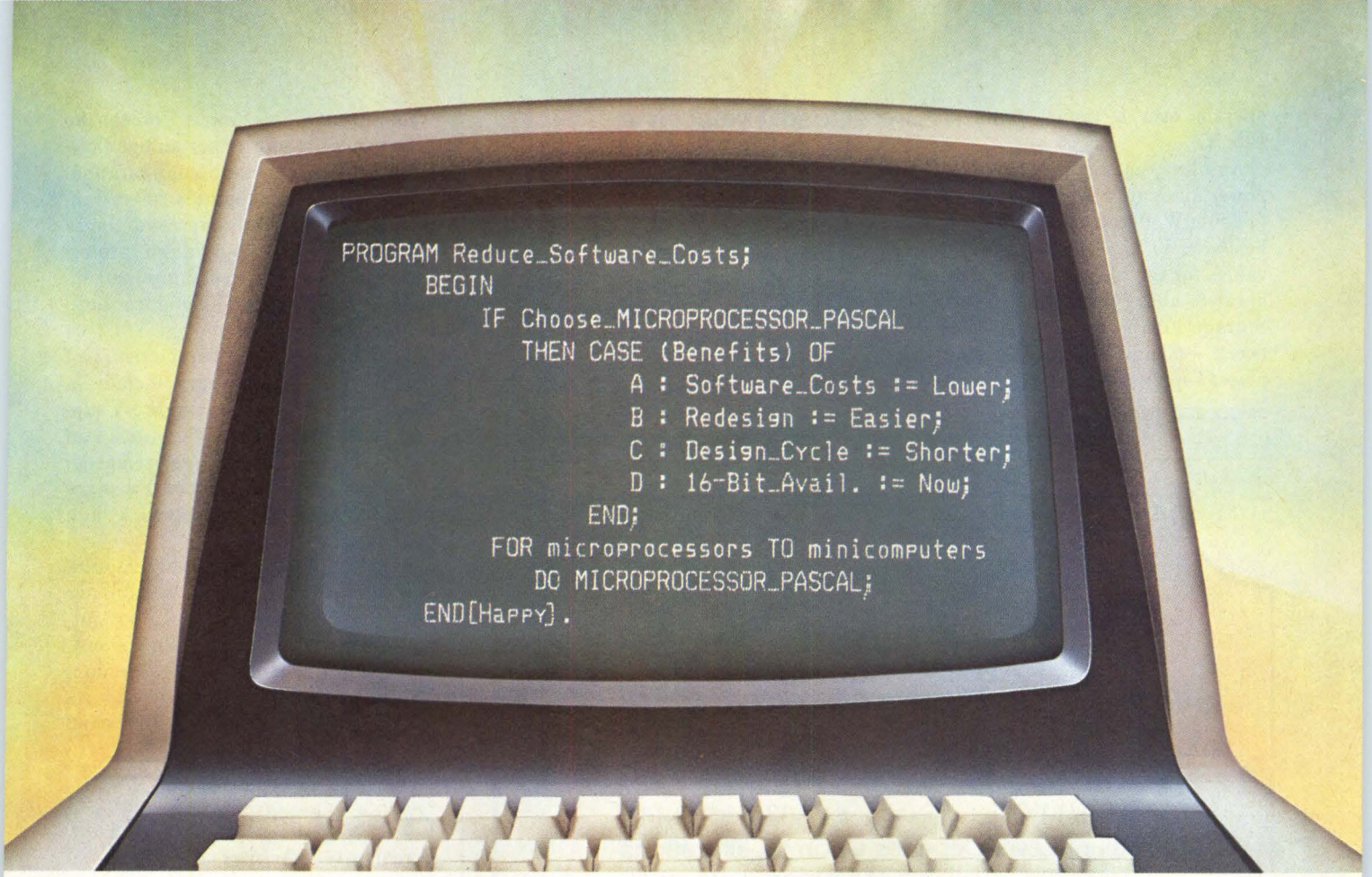
Containing two independent micropower timer sections on a single chip, the XR-L556 dissipates approximately 1/15th the power of conventional dual timers. This integrated circuit, produced by Exar Integrated Systems, 750 Palomar Ave, Sunnyvale, CA 94088, is the dual version of the XR-L555 from the same manufacturer. It finds use in battery-operated or portable equipment applications, where its low power dissipation is a critical requirement. Specific applications include pulse shaping and detection, micropower clock generators, micropower oscillators, power-on reset controllers, sequential timing, pulse width modulation, and remote control sequencers.

Power dissipation is less than 2 mW typ, (<1 mW per section), at 5-V operation. The device can operate down to 2.5 V without sacrificing such key features as timing accuracy, temperature stability, and output current-sourcing capability. It can operate in excess of 500 h with only two 300-mA-h NiCd batteries. The two timer sections have separate controls and outputs, but share common supply and ground terminals. Each output can source up to 100 mA of output current or drive TTL circuits. The output is free of switching transients ordinarily associated with conventional 555-type timers.

Other features include a timing capability from microseconds to minutes, operation in both monostable and astable modes, and CMOS, TTL, and DTL compatible outputs. Provided in a 14-pin DIP, it functions in most applications as a direct pin-for-pin replacement for the NE-556 dual timer circuit. Operating temperature ranges are 0 to 75 °C for plastic- and ceramic-packaged commercial versions designated by suffixes CP and CN, respectively. The ceramic-packaged military version, suffix M, is designed to



Functional block diagram shows Exar's XR-L556 monolithic dual timer. Chip contains two independent micropower timer sections



The program to reduce software costs. Microprocessor Pascal System. New. From Texas Instruments.

Learnability. Transportability. Maintainability.

The features of Pascal, plus the benefits of TI's learning curve experience, are offered in the new Microprocessor Pascal system.

A system designed for microprocessor applications.

A system developed for the 16-bit 9900 Family, including the TM990 microcomputer modules, and 990 minicomputers.

A system to effectively lower your software costs today. And keep them low tomorrow.

At TI, Pascal is the first and only corporate-wide approved high-level programming language. For a lot of good reasons.

Pascal lets you solve your application without getting involved in the intricacies of machine architecture. And, Pascal's block structure results in fewer programming errors, because the code is easier to write, read and modify.

TI's Microprocessor Pascal system consists of six parts and provides the most Pascal capability ever offered:

- Source Editor — specifically designed to create/edit Pascal programs and check program syntax.
- Compiler—compiles conventional Pascal programs as well as TI's Pascal concurrent extensions into interpretive code, which can then be executed directly, or converted into 9900 native machine code.
- Host Debugger — over fifteen options for tracing variables and modifying data.
- Configurator—enables the target system to retain only the parts of the run-time support necessary for program execution.
- Native-Code Generator — converts Pascal interpretive code into 9900 native machine code.
- Run-Time Support—both interpretive and native-code execution provide a speed/memory trade-off.

TI's continuing commitment to innovative, cost-effective 16-bit microprocessor software means an increased applications capability and decreased development time for you.

Find out how you can reduce your present and future software costs. Put the new TI Microprocessor Pascal system to work for you, today.

For more information, call your nearest TI field sales office or authorized distributor, or write to Texas Instruments, P.O. Box 1443, M/S 6404, Houston, Texas 77001.

Fifty Years of Innovation

TEXAS INSTRUMENTS
INCORPORATED

85582A

CIRCLE 141 ON INQUIRY CARD

operate over a range from −55 to 125 °C.

Absolute maximum ratings limit power dissipation with the ceramic DIP to 750 mW, derated above T_A = 25 °C by 6 mW/°C. The corresponding values for the plastic DIP are 625 mW, derated above 25 °C by 5 mW/°C. Storage temperature must stay between −65 and 150 °C. Max allowable power supply is 18 V.

CIRCLE 356 ON INQUIRY CARD

Quad Transceiver Drives IEEE-488 Bus

A quad bidirectional transceiver from Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086, meets the requirements of IEEE-488 standard digital interface for programmable instrumentation for the driver, receiver, and composite device load. The Am3448A provides one pull-up enable input for each pair of transceivers. This input forces the driver outputs into either an open collector or active pull-up configuration. Each receiver also features 600-mV input hysteresis for improved noise margin while power-up/down protection eliminates spurious noise and invalid information from being transmitted to the bus.

Typical operating characteristics of this TTL-compatible part include a 20-ns propagation time, single 5-V supply, high impedance inputs, and 3-state outputs. With power removed, the device bus (receiver input) changes from standard bus loading to a high impedance load.

Absolute maximum ratings require that supply voltage not exceed 7 V nor input voltage 5.5 V. Driver output current must not be greater than 150 mA. The part undergoes 100% product assurance testing to MIL-STD-883 requirements. **CIRCLE 357 ON INQUIRY CARD**

CMOS Multiplying DACs Achieve 10 and 12 Bits Without Laser Trimming

Three monolithic multiplying digital to analog converters introduced by Micro Power Systems Inc, 3100 Alfred St, Santa Clara, CA 95050, use advanced HD/CMOS and thin film technologies to achieve 10- and 12-bit performance without laser trimming. Typical applications for the 10-bit (16-pin) MP7530 and 12-bit (18-pin) MP7531 include digital-analog multiplication, CRT character generation, programmmable power supplies, and digitally controlled gain circuits. Both are DTL, TTL, and CMOS compatible, have a nonlinearity tempco of 2 ppm of FSR/°C and a 20-mW typ power dissipation, including the ladder network.

The low cost 10-bit (16-pin) MP7533 is a 4-quadrant DAC. It is used for digitally controlled attenuators, programmable gain amplifiers, function generation, and linear automatic gain control.

These devices are exact second source replacements for the AD7530, AD7531, and AD7533, with permission from Analog Devices. They are provided at competitive price levels of $7.90 for the two more advanced models and $5.80 for the lower cost model, in lots of 100.

CIRCLE 358 ON INQUIRY CARD

PENRIL'S DATACOMM SOLUTION

Means Over 25 Modem Products to Choose From...

In selecting the best modem for your data communication system, consider existing equipment compatibility, data volume, data rate, transmission distance and cost. Then choose from our FCC registered modems . . . compatible with Bell 103, 113, 202, 201, 212 or 208 . . . or CCITT V.22, V.26, V.27, V.29 compatible units for European installation . . . or our low-cost, short-haul modems for local data communication.

...With Complete User Support.

Before your modems leave our factory, they have been extensively tested and burned-in by our quality assurance team. Once your Penril modems are installed, you choose the field service plan . . . factory return, on-site service by one of our four hundred service locations or overnight spares delivery. But what really makes the Penril solution unique is our self-contained diagnostics. From the analog and digital loop-back of our 300/1200 modem to the more sophisticated integral network diagnostics of our 2400, 4800 and 9600, Penril modems help you avoid or shorten down-time.

And, Penril Modems Are Competitively Priced and Ready to Deliver.

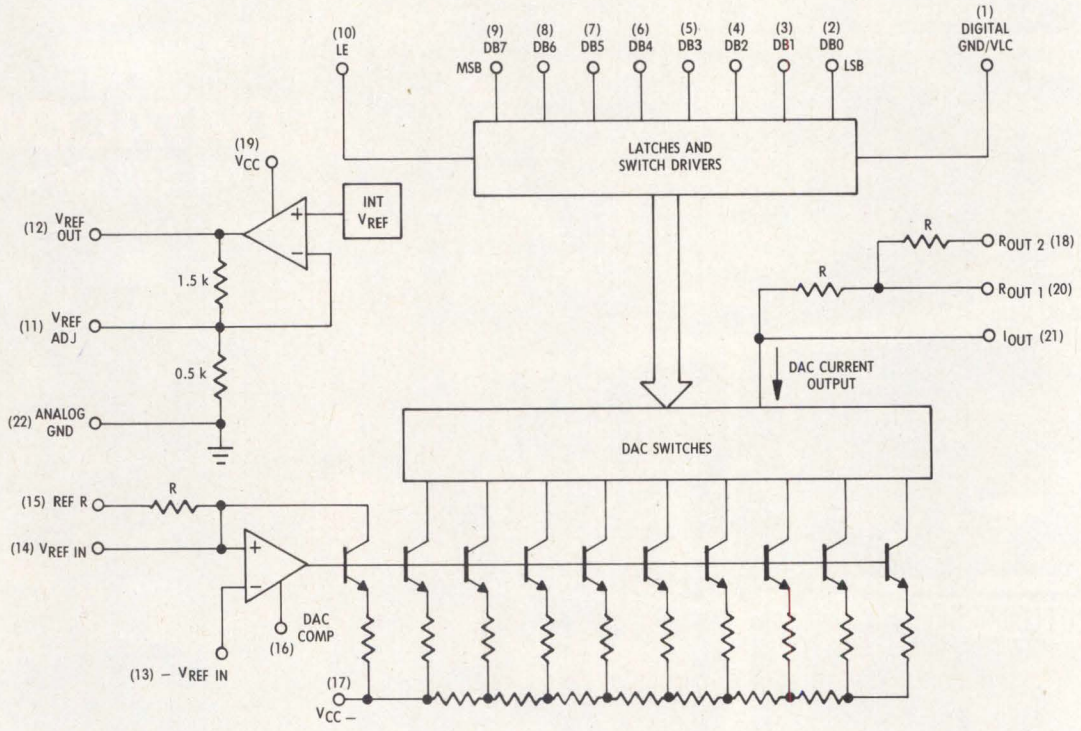
For additional information, call or write Penril Corp., Data Communications Division, 5520 Randolph Road, Rockville, Maryland 20852. 301/881-8151; TWX 710-828-0522.

Penril DATACOMM

...We Still Care.

CIRCLE 143 ON INQUIRY CARD

8-Bit DAC Features 0.1% Accuracy and 200-ns Settling Time



D-A converter NE/SE5119 from Signetics. Chip settles in 200 ns with ± ¼-bit accuracy and includes voltage reference. All R values equal 5 kΩ and are thermally matched

Features of an 8-bit digital to analog converter, NE/SE5119, produced by Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94086, include a settling time of only 200 ns (typ), an accuracy of 0.1% (±¼ bit), and low zero scale and gain tempcos of 5 and 20 ppm/°C, respectively. The NE/SE5118 is identical to this in most of its parameters, including settling time and temperature coefficients, but provides an accuracy of 0.2% (±½ bit).

These monolithic devices offer low loading data inputs of less than 10 μA, addressing capability, and complying logic levels. The series also provides a programmable current sink of 0 to 2 mA and a timing requirement of less than 1 μs. Applications are to be found in IC semiconductor test equipment, programmable power supplies, flow meters, graphic displays, temperature sensing, and A-D converters.

Data inputs have input latches, controlled by a latch enable pin. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition are latched and retained until $\overline{LE}$ goes low. This feature allows compatibility with most microprocessors.

The chip includes a stable voltage reference (5 V nominal), which can be externally trimmed with potentiometer for easy adjustment of full scale, while maintaining the low tempco. This reference is short circuit protected.

Additional characteristics include internal feedback, an output having high voltage compliance, and monotonicity to 8 bits. The operating temperature range is 0 to 70 °C for NE prefix and −55 to 125 °C for SE suffix.

CIRCLE 359 ON INQUIRY CARD

SELECTABLE STORAGE. AMPEX MAKES IT. AND MORE.

Selectable storage means getting as much disk as you need. But not having to buy more than you want.

Ampex disk storage modules are available in six models in two distinctive series. Choose from the DM-900 family; 5-high disk packs, with capacities of 40, 80 or 160 megabytes, for rack, console or table-top mounting.

Or select from the DM-9000 series of free-standing models, with 10-high disk packs, in 100, 200 and 300 megabyte capacities.

Either way, you'll get proven Ampex performance, uptime dependability, reliability and serviceability. A single industry-standard SMD interface is used for all Ampex storage modules. And with six models to choose from, you can select the storage capacity you need now, and upgrade as your requirements grow. And models within each series may be field-upgraded to the maximum capacity for that series.

Selectable storage. It's just one of the surprising Ampex line of digital systems products. From plug-compatible memories for nearly any CPU you can name, through a wide range of tape peripherals. Even intelligent controllers, our own minicomputer, and completely-packaged, all-Ampex minicomputer systems.

Call Gary Owen at 213/640-0150 for full details on our selectable storage and the full Ampex Product line. Or write to him at Ampex Memory Products, 200 North Nash Street, El Segundo, California 90245.

AMPEX MAKES IT EASY

CIRCLE144 ON INQUIRY CARD

Gas Discharge Display Drivers Offer Multiple Segment-Current Levels

Utilizing signals originating from MOS and TTL circuitry, IC segment drivers, the DI-232/242, are designed to drive gas discharge display devices. These monolithic silicon dielectrically isolated circuits, produced by Dionics, Inc, 65 Rushmore St, Westbury, NY 11590, deliver nine outputs as groups of four and five, each output group having a different and independent programmed segment-current level. This capability overcomes the difficulty of supplying the significant variations in segment current required for segmented gas discharge alphanumeric displays.

The chip can provide for simple interfaces with displays such as the Beckman, Burroughs, Cherry, Dale, or Pantek types. Each output is a switched programmable constant current sink with a voltage compliance of 80 or 125 V, for the -232 and -242 models, respectively. Input voltage capability is 40 V with an output current of 5 mA max. All output currents in each group of outputs are programmable with a single resistor.

Two of the units ganged together provide 18 outputs (two groups of 4 and two of 5), each individual group having different and independent programmed segment current levels. The manufacturer indicates that four different current levels from 18 outputs satisfy any gas discharge alphanumeric display requirement.

CIRCLE 360 ON INQUIRY CARD

IC Operates as F-V Converter

The CS-2917 series of frequency to voltage converters are particularly well suited for air core coil drive functions such as in the control of dc motor speed for tape drives. An IC belonging to this family consists of an input regenerative comparator, a frequency doubling charge pump circuit for F-V conversion with low ripple, a general purpose op amp/comparator output circuit, and a shunt regulator circuit.

These devices, produced by Cherry Semiconductor Corp, 99 Bald Hill Rd, Cranston, RI 02920, are available in three package configurations. One of these (suffix -D8) is an 8-pin DIP. The other two (suffixes -D14 and -1-D14) are 14-pin DIPs, the latter of which contains an added feature of an open collector transistor for a buffered high level output signal at a frequency equal to the input frequency.

CIRCLE 361 ON INQUIRY CARD

Low Cost ROMs Draw Low Power

Fully static CMOS read only memories, offered for as low as $5.45 each in lots of 10^5, require only 8-mA (typ) operating current and 7-μA (typ) standby current. Max values for these same parameters are 20 mA and 100 μA, respectively.

Other features of the CM3200 from Supertex Inc, 1225 Bordeaux Dr, Sunnyvale, CA 94086, include a single 5-V power supply, two mask programmable chip select inputs, 3-state outputs, and TTL compatible I/O. Access time is 450 ns (typ) and 600 ns (max). A high yield, low cost version (suffix -2) provides a max access time of 800 ns. Another low cost (suffix -3) version is 1802 microprocessor family compatible, with V_{CC} ranging from 4.0 to 6.0 V, and an access time of 1.5 μs.

CIRCLE 362 ON INQUIRY CARD

ITEM NO.
WK-7

CMOS SAFE

IC INSERTION/EXTRACTION KIT

KIT INCLUDES

- MOS-1416 14-16 CMOS SAFE INSERTER
- MOS-2428 24-28 CMOS SAFE INSERTER
- MOS-40 36-40 CMOS SAFE INSERTER
- EX-1 14-16 EXTRACTOR
- EX-2 24-40 CMOS SAFE EXTRACTOR

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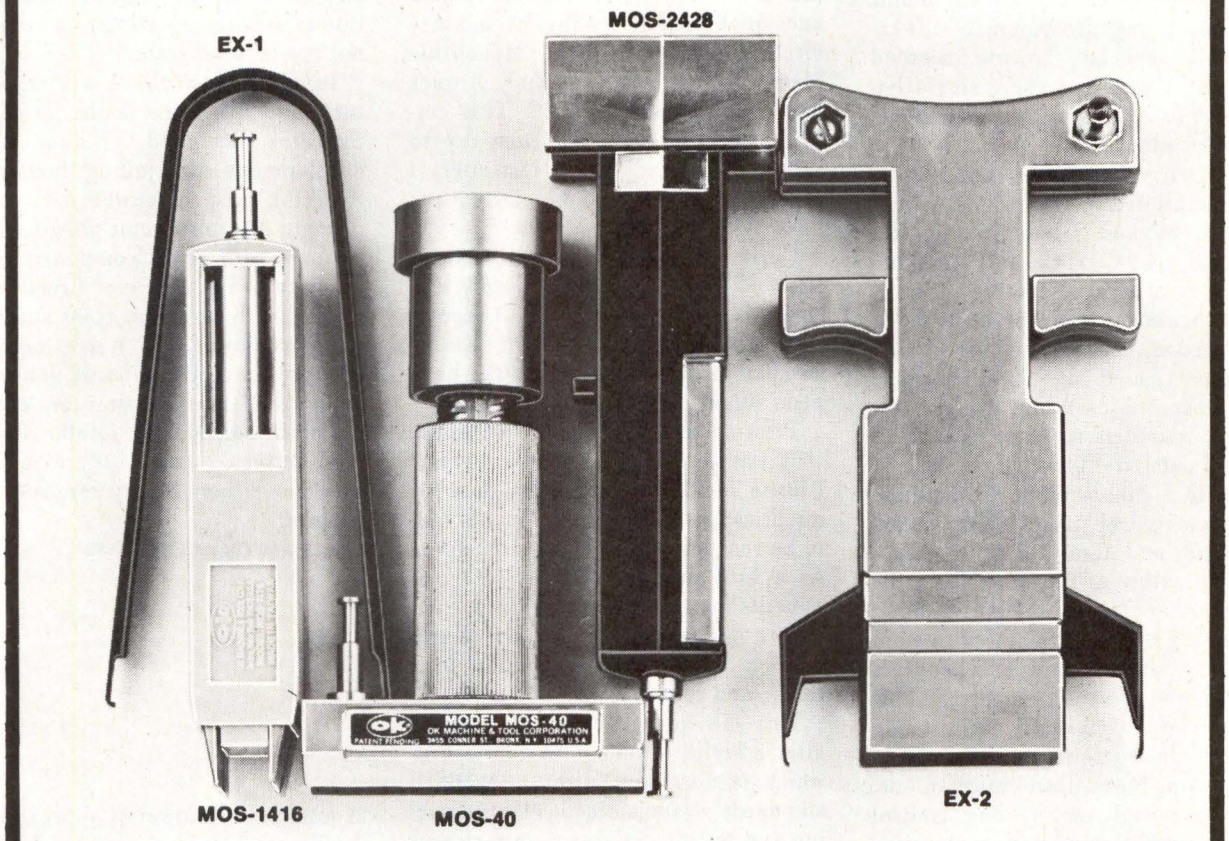
PATENT PENDING



WK-7	COMPLETE IC INSERTER/EXTRACTOR KIT	$29.95

INDIVIDUAL COMPONENTS

MOS-1416	14-16 PIN MOS CMOS SAFE INSERTER	$ 7.95
MOS-2428	24-28 PIN MOS CMOS SAFE INSERTER	$ 7.95
MOS-40	36-40 PIN MOS CMOS SAFE INSERTER	$ 7.95
EX-1	14-16 PIN EXTRACTOR TOOL	$ 1.49
EX-2	24-40 PIN CMOS SAFE EXTRACTOR TOOL	$ 7.95

MINIMUM BILLING $25.00. ADD SHIPPING CHARGE $2.00. NEW YORK RESIDENTS ADD APPLICABLE TAX.

OK MACHINE & TOOL CORPORATION 3455 CONNER ST., BRONX, N.Y. 10475 (212) 994-6600/TELEX 125091

CIRCLE 134 ON INQUIRY CARD

User Can Program Monolithic Controller For Stepper Motors

Implemented in NMOS on a single chip, and using a single 5-V supply, the CY500 stored program stepper motor controller is user programmable. It executes 22 separate function oriented commands, specified using single letters such as P for position, S for slope, and R for rate.

The TTL-compatible controller, manufactured by Cybernetic Micro Systems, 445-203 S San Antonio Rd, Los Altos, CA 94022, can be commanded by a standard ASCII keyboard. When the device is in the ASCII mode of operation, the instructions form a function oriented high level language that is easy to learn and use. In this mode, parameters are entered as ASCII decimal numbers. The chip can also be placed in a binary mode to facilitate computer control using binary coded commands and data.

A key feature of the controller is its ability either to execute commands at once in the command mode or to store a sequence of commands as a program and then run the program. This feature allows program looping using do-while instructions and program waits using wait-until instructions. Other powerful instructions control single- or multi-step mode operation, full- or half-step operation, absolute or relative positioning, and ramp-up, slew, ramp-down operation.

Numerous input and output control lines allow synchronization with external events or devices. Each step can be triggered separately, and control of direction and starting and stopping may be affected via either external hardware or via software control. One output control line is completely under software control. An abort line can be used to abort any stepping command. Control of step rates up to 3500 steps/s is possible. Asynchronous communication with the chip can be achieved either serially (using several baud rates) or in parallel fashion using a simple ready line from and a write strobe to the chip.

CIRCLE 363 ON INQUIRY CARD

DOD Grants JAN Certification

The Defense Electronics Supply Center (DESC), an agency of the U.S. Department of Defense, has granted full JAN certification for production and qualification testing of military electronic components to Monolithic Memories Inc (MMI), 1165 E Arques Ave, Sunnyvale, CA 94086. This certification will allow the company to submit Qualified Parts List (QPL) I reports to DESC for its bipolar P/ROMs in early 1980.

Currently, MMI is listed for QPL II for MIL-M-38510/203 (1k P/ROM) and MIL-M-38510/204 (2k P/ROM). QPL II reports for MIL-M-38510/207 (256-bit P/ROM) and MIL-M-38510/209 (8k P/ROM) have been submitted to DESC for review.

Prior to achieving full certification, MMI was certified to produce bipolar P/ROMs for JAN applications, but for qualification testing, components had to be sent out to a DESC approved lab. As a fully certified supplier of components for JAN applications, the company now has greater control over production schedules, can shorten lead times, and reduce its costs.

Full JAN qualification was granted after a series of on-site inspections in which conformance with MIL-M-38510 standards was examined. Manufacturing and test procedures were reviewed by DESC personnel and its representatives for over a year to make this certification.

CIRCLE 364 ON INQUIRY CARD

Peripheral Chips Are Second Sourced

Synertek Inc, 3001 Stender Way, Santa Clara, CA 95051, has granted a second source agreement for the manufacture and marketing of its proprietary SY6551 asynchronous communications adapter chip. The agreement permits Rockwell International, 3310 Miraloma Ave, Anaheim, CA 92803, to manufacture and market the microprocessor peripheral device on a worldwide, nonexclusive basis.

This chip provides interfacing for 6500 and 6800 microprocessor families to serial communications data sets and modems. A unique feature is the inclusion of an onchip programmable baud rate generator requiring only an external crystal to operate.

In addition, Rockwell will manufacture the SY6545 CRT controller chip, a Synertek designed product whose development was jointly funded by Synertek and Rockwell. Replacing discrete ICs, this circuit provides more features with fewer components at a lower cost. The device is directly compatible with both the 6500 and 6800 microprocessors, and it does not need memory contention circuits. It also has an internal status register that enables the processor to check its status, and a dual refresh memory address, which can be either binary or row and column.

CIRCLE 365 ON INQUIRY CARD

14 Models of Low Power dc/dc Converters Are Available in Series

A total power output of approximately 1 W characterizes a family of low power dc/dc converters introduced by the Power Products Division of Computer Products Inc, 1400 NW 70 St, Ft Lauderdale, FL 33309. Designed for direct printed circuit card mounting, the PM600 series converters allow the design engineer greater leeway and flexibility in determining PC card component layouts. The devices are provided in 24-pin DIPs.

Fourteen single- and dual-output models are available, providing dc outputs of 5, 12, 15, ±12, or ±15 V from inputs of 5 Vdc or 12 Vdc. All models provide tight line/load regulation and isolation voltage up to 50 Vdc. The devices also feature thermal overload protection and short-circuit protection for up to eight hours, plus epoxy encapsulation for added durability.

CIRCLE 366 ON INQUIRY CARD □

For years, manufacturers of computers, processors and other electronic equipment have improvised all too freely when running interconnecting cables *outside* cabinets. The results have been cumbersome, unattractive, often costly and sometimes hazardous.

Brand-Rex, long a leading supplier of Tape Cable® for internal use, now has the answer for external applications. A line of UL-listed jacketed Tape Cable. With shielding or without, it's made to fit a full range of temperatures and voltages up to 105°C and 600 volts. Now, interconnections can be efficient, economical, hazard-free, often even invisible.

Get complete information about Brand-Rex jacketed or shielded-and-jacketed flat cable. Write to Brand-Rex Company, Electronic and Industrial Cable Division, Willimantic, CT 06226. Or call 203/423-7771.

BRAND-REX

ELECTRONIC AND INDUSTRIAL CABLE DIVISION

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Electronic & Industrial Cable Division: wire and cable
Nonotuck Manufacturing Company: copper wire
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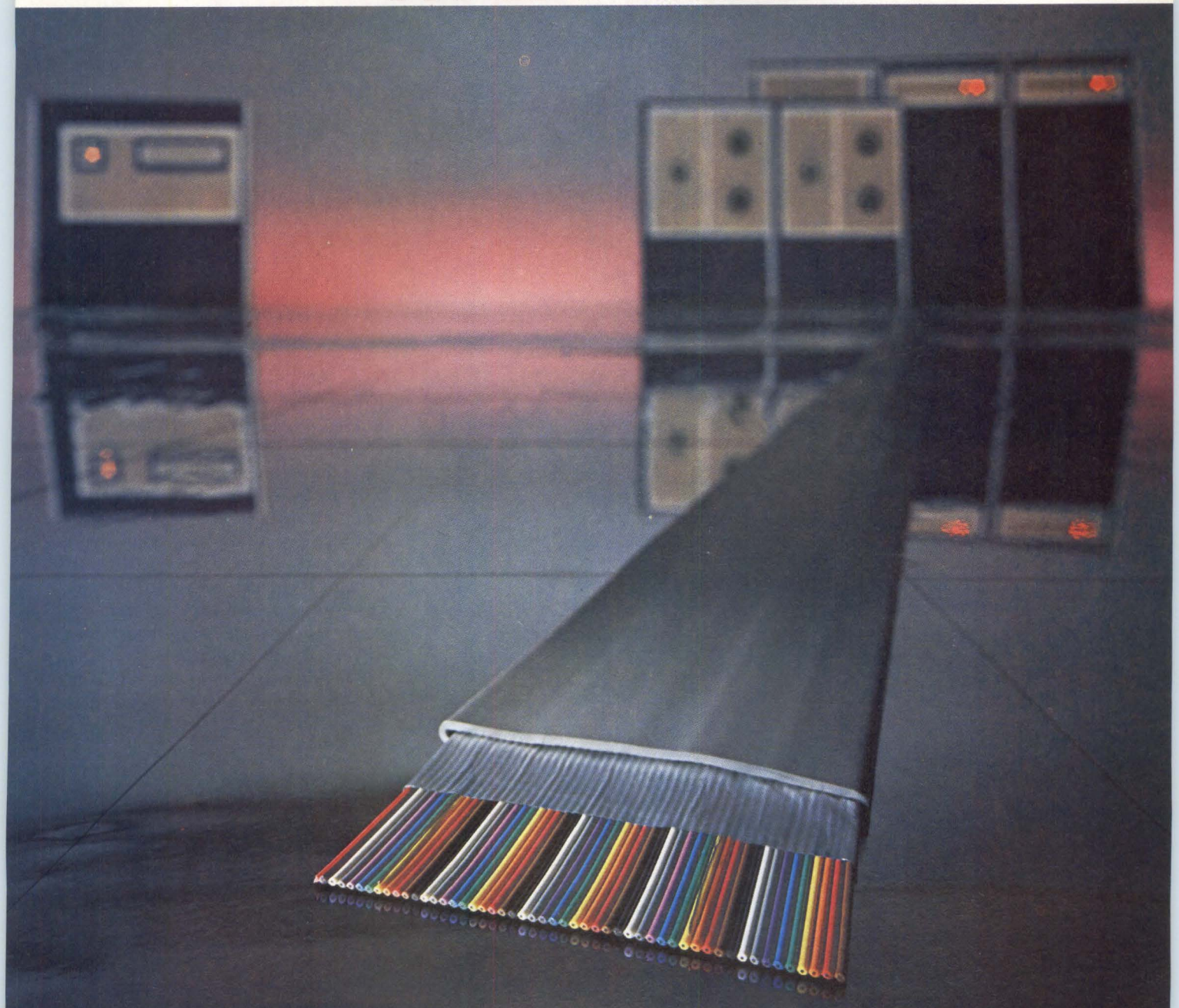
Teltronics, Inc.: telecommunications products

BRAND-REX COMPANY, A PART OF AKZONA INC.

THE SAFEST CONNECTION BETWEEN TWO POINTS IS NOW A FLAT LINE.



STATE-OF-THE-ART-SOLUTIONS

CIRCLE 147 ON INQUIRY CARD

PRODUCT FEATURE

Double-Sided, Double-Density Floppy Disc Drives Provide 1 M-Byte Storage

Two double-sided, double-density floppy disc systems introduced by Charles River Data Systems boost available storage to 1M bytes/drive. In addition, an LSI read circuitry chip increases read margins by 150 ns. Both systems use Shugart SA850 disc drives and are DEC compatible.

The MF-411 is a completely self-contained system with LSI-11/2 microprocessor, backplane, memory, power supply, and two floppy disc drives (it will accommodate the LSI-11/23 when available). FD-411 is an add-on system for Q-bus or Unibus applications.

Characteristics and Capabil

Both systems are downward compatible with the manufacturer's MF-211 and FD-211 single-sided diskette systems. A single dual-height card contains controller, interface, and formatter electronics and provides software/media compatibility with DEC's RX02 floppy disc system. Total RX02 emulation and other intelligent functions are handled by a 2901 microprocessor controller.

A bootstrap loader enables automatic loading of system diskettes on power-up or when the Init/Boot switch is activated; in the MF-411 this loader eliminates need for the BDV-11AA boot function and reduces backplane space requirements. In addition, through a feature not available on the RX02, an MF-411 user can format any diskette with IBM 3740 headers. DMA data transfer is provided on a per sector basis. Advancements in read circuitry are said to have been provided in order to assure media compatibility with DEC's single-sided, double-density diskettes.

The MF-411's front panel is removable for access to system modules, which plug directly into a 4-quad (or optional 8-quad) slot backplane. Pivoting the backplane card cage upward provides access to the floppy disc drives. Two internally mounted fans cool the MF-411.

Specifications

Floppy disc drive capacities include 77 cylinders, 2 tracks/cylinder, 26 sectors/track, 256 bytes/sector, 1M bytes/disc, and 2 heads/drive. Access times are 2 ms track to track and 91 ms average seek. Transfer rate is 500 bits/s. Track density is 48 bits/in (19/cm) and recording density is 6816 bits/in (2683/cm).

Enclosure dimensions for the MF-411 and FD-411, respectively, are 19 x 10.5 x 22″ (48.3 x 26.7 x 56 cm) and 19 x 5.25 x 22.1″ (48.3 x 13.33 x 56.1 cm). The MF-411 can be slide-rack mounted or used as a tabletop unit. Power consumption for the MF-411 (with LSI-11/2 and 32k words) is 4 A; for the FD-411, it is 2 A. Respective operating temperature ranges are 59 to 90 °F (15 to 32 °C) and 50 to 100 °F (10 to 38 °C), both at 20 to 80% relative humidity, noncondensing.

Price and Delivery

A complete MF-411 double-sided, double-density floppy disc system including front panel console with switches is priced at $6980. The FD-411 add-on system is $4250. Delivery is 30 to 45 days ARO. Charles River Data Systems, Inc, 4 Tech Circle, Natick, MA 01760. Telephone: 617/655-1800.

For additional information circle 199 on inquiry card.

PRODUCTS

Encryption Devices Ensure Integrity Of Stored As Well As Communicated Data

Placed in the communications path between a user's terminal and the host computer, either of these data encryption devices will ensure the security and privacy of stored data as well as communicated data. DataLocks accept commands from both terminal and computer via a standard RS-232-C interface. No software or hardware modifications are needed. Both units use the National Bureau of Standards Data Encryption Standard.

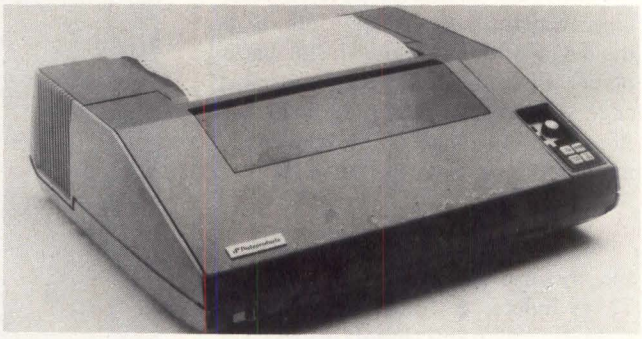
A user is able to encrypt data entered through a terminal and decrypt data returned to the terminal, encrypt/decrypt files stored in a computer, encrypt communications between two system users, and encrypt data transmission over communications links. When not in use, the units are invisible to system operation.

Model 150 is located near the user's computer terminal and connected by standard communications lines. It is controlled by the user through the terminal. The encryption process is started and stopped by brief commands at user chosen spots during data entry. Automatic decryption of retrieved data is achieved by trigger commands inserted by the unit in the encrypted data stream, or by explicit user commands. Data files sent from the computer are encrypted or decrypted by the unit and the processed version is returned. A user's entry key entered through the terminal at the beginning of a session is inaccessible by any means.

Added capabilities enable the model 250 to function with an entire system. It accepts control commands from the computer as well as the user's terminal and can operate as a shared resource. Encryption keys may be changed to accommodate different users.

Present systems operate with any asynchronous protocol; a bisynchronous protocol version will be available soon. Baud rate is adjustable from 110 to 9600. **SPI Data Systems, Inc,** 488 Cowper St, Palo Alto, CA 94301.
Circle 200 on Inquiry Card

180-Char/s Impact Printer Has 7 x 7 Half-Dot Matrix Font



A slower version of a dot matrix impact printer previously announced by the manufacturer, the M-120 has a speed of 180 char/s in a bidirectional, logic seeking mode. It uses a 7-wire printhead rather than the 14-wire, dual-column head of the faster model. Throughput averages 120 lines/min and varies from 75 lines/min for full 132-char lines to 200 lines/min for 40-char lines. Standard or expanded characters are printed in a 7 x 7 half-dot matrix font. The operator replaceable head is rated for better than 200M char and continuous loop fabric ribbons housed in cassettes have 5M-char lives.

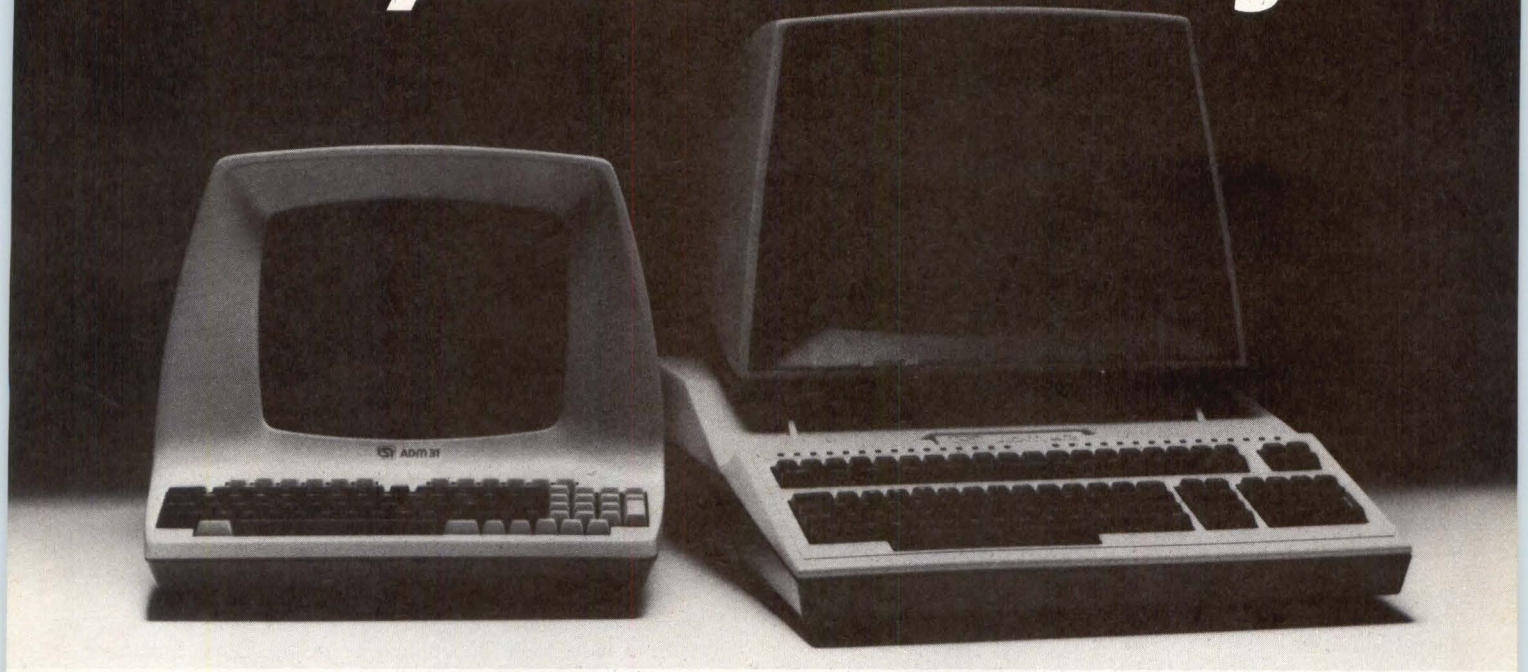
There is no required preventive maintenance. A self-test feature is built into the printer and an optional LED diagnostic display indicates which cycle the printer was in at the time it went offline.

Operating specifications include 10" (25.4-cm)/s min paper slew speed, 50-ms max single line advance, 500k-byte/s max data transfer rate, and choice of standard 8-bit parallel or optional RS-232-C interface. Character size is 0.074" W x 0.105" H (1.88 x 2.667 mm) with a 128-char ASCII set. Line spacing is 6/in (2/cm) standard, 6 or 8/in (2 or 3/cm) optional. Character spacing is 10/in (4/cm) standard with interface selectable double-width characters, 16.7/in (6.6/cm) optional.

A forms control tractor feed mechanism is adjustable from 3 to 6" (8 to 15 cm). Loading of continuous fanfold, edge perforated forms is standard front and bottom, optional rear. An original plus 5 copies can be made. A 12-channel direct access vertical format unit is standard; a tape controlled version is optional.

Physical dimensions are 7.9" (20 cm) in height, 26.1" (66.3 cm) in width, and 23.3" (59.2 cm) in depth. Weight is 70 lb (31.8 kg). A pedestal is optional. Input power is 200 W max, 125 W standby. A voltage of 115 Vac +10, −15% at 60 Hz ±1 Hz is standard; 220 Vac +10, −15% at 50 Hz ±1 Hz is optional. **Dataproducts Corp,** 6200 Canoga Ave, Woodland Hills, CA 91365. Circle 201 on Inquiry Card

Lear Siegler brings you the smart terminals designed for easy OEM customizing.



PERSONALITY PROMS AND FACTORY ASSISTANCE MAKE USER-REPROGRAMMING A SNAP.

At Lear Siegler, you don't have to decide among dozens of smart terminals, each slightly different, but none quite right for you.

We have just two smart terminals. But they can handle a range of tasks equal to four, five, or even six models from other manufacturers.

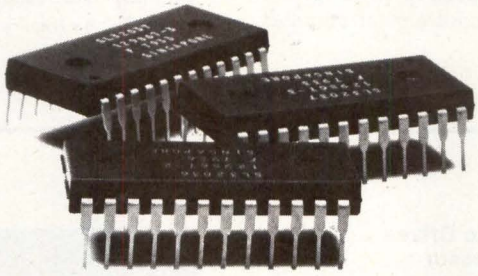
After all, we want to make your life simpler, not more complicated.

THE ADM-31 & ADM-42 WILL LET YOU CHANGE THEIR MINDS.

When we designed the ADM-31 and ADM-42, we realized that no matter what capabilities we offered, somebody would always want something different. So we did the next best thing.

We gave each a truly flexible personality by putting the instruction sets inside their PROMs. So, unlike the hardware, the firmware is capable of easy OEM reprogramming.

We even have a special Application Engineering Staff to answer any questions you may have about reprogramming, interfacing or special applications.



Feeling your life getting simpler yet?

ALL THE TERMINALS YOU'LL EVER NEED.

Even if you decide not to reprogram their PROMs, our two terminals come with all the standard smart terminal features. And then some.

Features like full editing capabilities. Formatting. Reduced intensity for identification of protected fields. Blinking, blanking, and reverse video. High resolution monitors. Even limited line drawing capabilities.

What's more, both the ADM-31 and ADM-42 come equipped with a microprocessor and function keys making them even more reliable and easy to use.

THE CHOICE IS SIMPLE.

You can choose your new smart terminal one of two ways. Start sifting through dozens of data sheets, talking to dozens of salesmen, and looking at dozens of expensive, slightly different terminals.

Or look at two smart terminals from Lear Siegler—the ADM-31 and ADM-42. Complete with user-reprogrammable personality, function keys, and an eager and willing Applications Engineering Staff to help you with any reprogramming problems.

The choice seems pretty easy to us. But if you want more information, call or write to us at Lear Siegler, Inc./Data Products Division, 714 North Brookhurst Street, Anaheim, California 92803, (800) 854-3805. We'll be happy to tell you all about the ADM-31 and ADM-42. And show you how you can make your terminals behave.

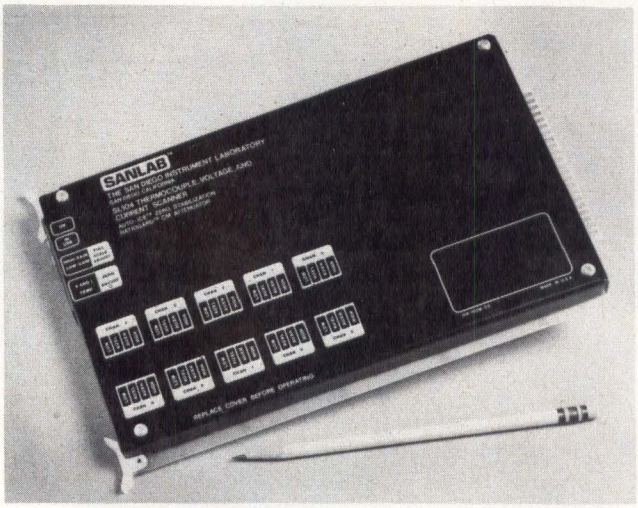
LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

CIRCLE 149 ON INQUIRY CARD

Lear Siegler, Inc./Data Products Division, 714 N. Brookhurst Street, Anaheim, CA 92803, (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157. Telex: 65-5444. Regional Sales Offices San Francisco (408) 263-0506. Los Angeles (213) 454-9941. Chicago (312) 279-5250. Houston (713) 780-2585. Philadelphia (215) 245-1520. New York (212) 594-6762. Boston (617) 423-1510. Washington, D.C. (301) 459-1826. England (04867) 80666.

PRODUCTS

Data Acquisition Device Multiplexes 10 Analog Channels



A single-card, 10-channel analog scanner, the SL104 data acquisition device connects directly to input sensors. Interchannel isolation of 1 GΩ assures the ability to obtain intermixed microvolt signals even in the presence of common mode voltage as high as 310 V. The industrial rated device plugs into a standard 6.25″ (15.88-cm) card slot. It operates with random combinations of grounded or ungrounded thermocouples, voltages, and currents and then references, scans, amplifies, filters, and controls selected signals. Voltage dividers and current shunts in individual onboard channel sites enable operation over full-scale ranges from millivolts to volts and microamperes to amperes.

Onboard CMOS control logic is fully TTL/CMOS compatible without buffering and is configured for bus operation with microprocessors. It obeys single encode commands, remembers current channel and mode selections, switches the multiplexer, and provides status signals. Group digital outputs are parallel busable up to 160 channels (16 units).

A precision reference junction automatically compensates all thermocouple inputs and passes them to a low thermal reed multiplexer. Zero stabilization provides zero referencing and eliminates time based zero drift. Following amplification, signals pass through an active filter that removes all remaining 60-Hz noise. Analog outputs can be bused together through an output multiplexer.

Digital inputs are TTL/CMOS compatible with additional protection for static discharge; digital outputs are 3-state and allow for fanout of 2 normal TTL loads. Power requirements are ±15 and ±0.5 V at 30 mA max each and ±5 V at 130 mA max. Input impedance is >4 MΩ. Other features include true isothermal reference junction, automatic thermocouple break detection, span calibration option, automatic common mode attenuator, and National Bureau of Standards traceable calibration. **San Diego Instrument Laboratory,** 7969 Engineer Rd, San Diego, CA 92111.

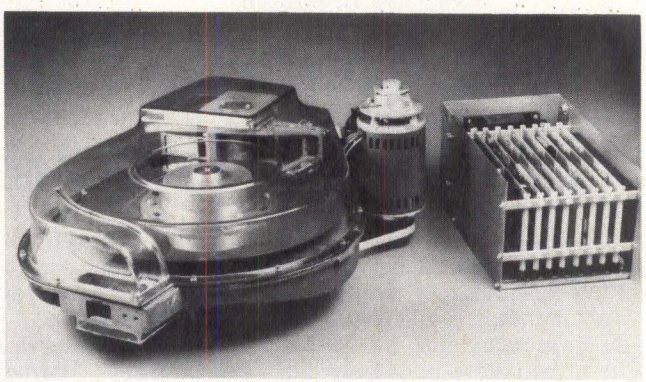
Circle 202 on Inquiry Card

Microprocessor Controlled Fixed Disc Drives Ease Software Burden on Host Processor

FD 211 (20M-byte) and FD 214 (80M-byte) 14″ (36-cm) Winchester technology fixed disc drives feature built-in microprocessor controllers that perform many of the tasks normally handled by the host systems, eg, asynchronous file search, confidence/diagnostic tests, cyclic redundancy check generation, error detection and correction, and sector relocation. These FD 210 series drives are interface compatible with the company's MD 122 3M- and 6M-byte dual-minifloppy disc drives. Both disc drive series use the same controller electronics and may be mixed on the same host system controller.

Drive modules are sealed units with 1 or 4 nonremovable discs mounted on a common spindle. Two flying heads are moved across each surface by a rotary positioner to access the data tracks. Servo tracks at specific locations on each surface are used by the microprocessor controller to correct for alignment variations caused by environmental changes. Standard interface for integration with a host system is a parallel data and control bus.

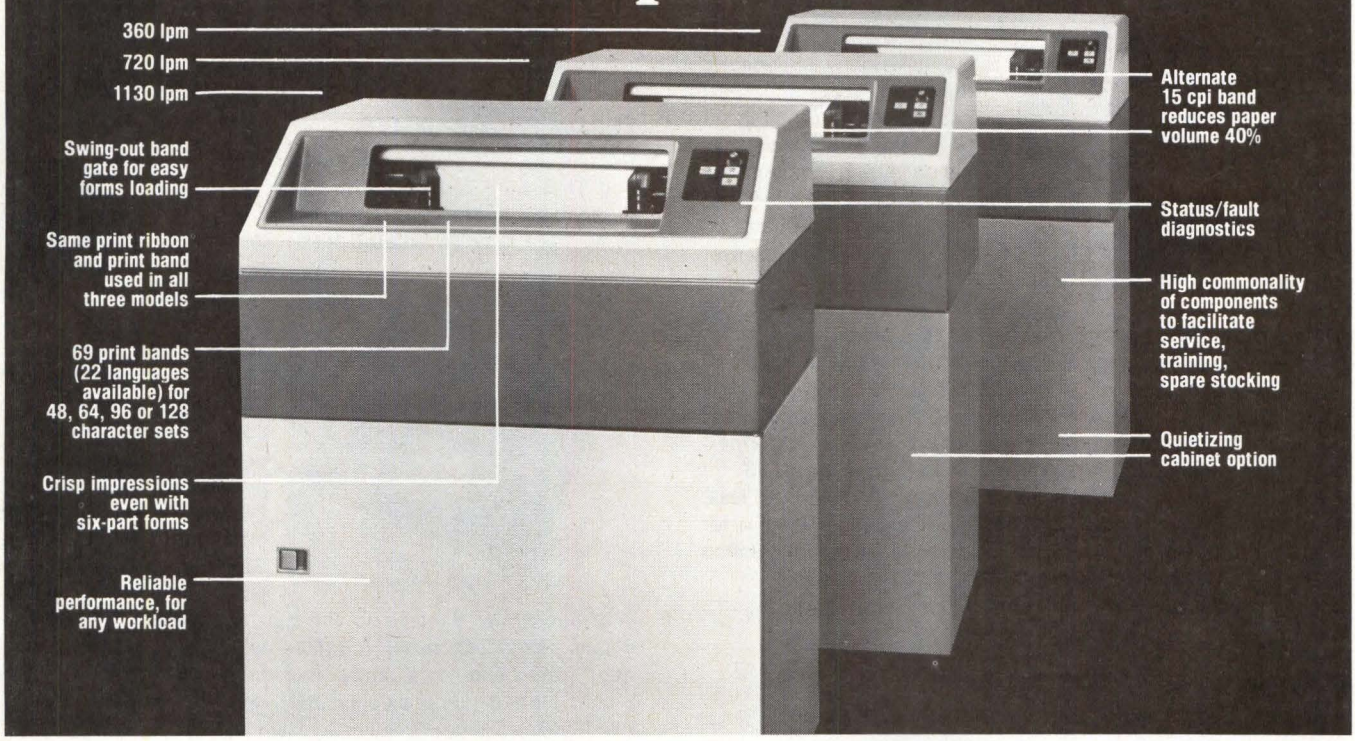
Host system software is also simplified by activities of the microprocessor controller. Because, as soon as disc drive power is turned on, the microprocessor controller determines and reports to the host system how much storage capacity



is available (20M or 80M bytes, for FD 210 series or 3M or 6M bytes for the MD 122), disc subsystems can be mixed, replaced, or upgraded without software changes.

RETMA rackmount, freestanding cabinet, and power supply options are available. The supply voltage requirement is 5 V ±10%. Absolute value of common mode voltage between host and device grounds must be <5 V. Line drivers and receivers are RS-422 compatible. Max cable length is 25 ft (7.6 m). **Burroughs OEM Marketing Corp,** Burroughs Pl, Detroit, MI 48232. Circle 203 on Inquiry Card

Quality impressions are made easily with OEM band printers from CDC



If you're an OEM, you already know what Control Data has done for disk technology. Now we're determined to earn the same reputation for excellence in band printer technology. By giving *you* versatility and maintainability. By giving *your customer* reliability, superior print quality and economical operation.

Engineered for component commonality

All three members of our 9380 family of band printers look pretty much alike. Inside and outside. So your servicing, training and inventory requirements are simplified. Yet you can choose from three print speeds, 69 print bands and lots of other options.

Built with the features and economy to attract end-users

Our 360/720 lpm models offer a compressed pitch option. That saves your customer money in paper expense. And gives him the capability to print 132 columns on standard 8½ by 11 inch paper. Bands switch in seconds. Paper loading is easier. Operator controls and adjustments are minimal. And your customer will like the clean, crisp impressions delivered by our proven hammer technology.

Put quality behind your nameplate. Let us send you data sheets and print samples. Call us at 313/651-8810 or if in Europe, contact one of our European representatives. Or return coupon to:

CD 30

Control Data Corporation
1480 N. Rochester Road, Rochester, MI 48063

Please send literature and sample printouts on your band printers.

Name_____ Title_____

Company_____ Phone_____

Address_____

City_____ State_____ Zip_____

CONTROL DATA CORPORATION

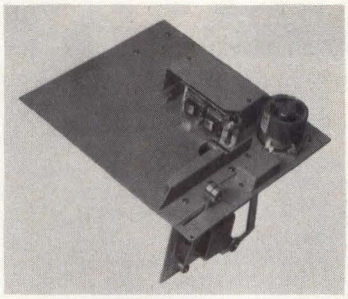
Addressing society's major needs

CIRCLE 150 ON INQUIRY CARD

PRODUCTS

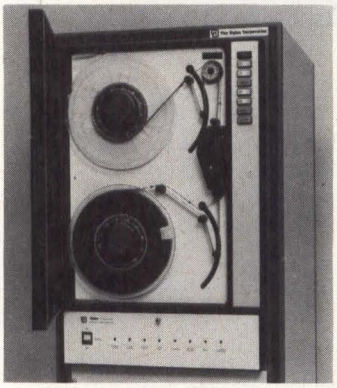
ENDLESS LOOP MAGNETIC TAPE TRANSPORT

An industrial quality unit, model 4 accepts continuous loop standard NAB, A, B, or C cartridges with from 13 to 1500′ (3.9 to 457.3 m) of tape. Precise 4-point head mounts (both head positions) provide separate zenith, height, and azimuth adjustment. Pressure roller is self-aligning and maintains constant pressure without readjustment, virtually eliminating tape edge wear and skew caused by tape pulling up or down. Preloaded precision spring components compensate for wear and hard usage. Standard ac motor is hysteresis synchronous for accurate speed in spite of line voltage variations; dc motor is governed internally for constant speed over wide voltage range and is shielded to prevent stray electrical radiation. Tape speed accuracy is specified as 1.5% (ac motor) or 2.5% (dc motor). Flutter and wow are less than 2% pulse to pulse jitter. Start and stop times of solenoid operated models are less than 100 ms. Operating temperature of the transport is in the 5 to 50 °C range, and weight of the unit is 6.25 lb (2.81 kg) or less. Unit is available in an electrically controlled version for remote operation or in an economical manual model. **Amilon Corp,** 49-12 30th Ave, Woodside, NY 11377.



Circle 255 on Inquiry Card

IEEE-488 0.5″ TAPE SYSTEMS



A GPIB (IEEE-488) magnetic tape system, the model 2101 provides transfer rates in excess of 100k bytes/s and dual buffering capacity to 16,384 bytes. Once data are on 0.5″ (1.27-cm) magnetic tape, they may be transferred into any computer for analysis. Data may also be transferred back to the GPIB controller from tape. A dedicated Z80A microprocessor manages bus interface, formatter, and tape transport functions within the system. Systems may include as many as 4 tape transports, systems may be 7- or 9-track, NRZI, PE, or dual mode, in a variety of reel sizes with or without code converters. The unit provides read after write error checking with automatic correction and automatic conversion of ASCII to/from IBM EBCDIC tape formats. **Dylon Corp,** 3670 Ruffin Rd, San Diego, CA 92123. Circle 256 on Inquiry Card

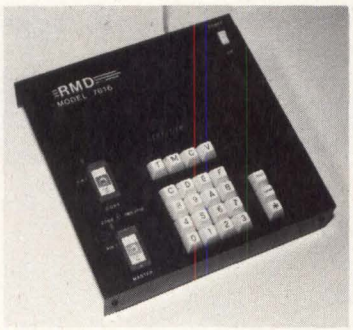
POLARIZED SUBMINIATURE CONNECTOR

Plasticon™ connectors have a snap-in mounting device, which is part of the insulator, to provide quick, hardware free connection. Units are completely interchangeable, intermateable, and intermountable with std D-type subminiature connectors. The connector is available in a 25-pin arrangement using both shell and contact polarization which assures proper and easy mating. Phosphor bronze contacts can be provided in various tail styles with gold plating. Overall max dimensions are 0.472″ (1.19 cm) high x 2.030″ (5.156 cm) long. Contact resistance is 14 mΩ max with a current rating of dry circuit to 3 A. Insulation resistance is 5 GΩ min. Temp rating under operating conditions is −40 to 105 °C. **TRW Cinch Connectors,** 1501 Morse Ave, Elk Grove Village, IL 60007.

Circle 257 on Inquiry Card

EPROM PROGRAMMER

Completely self-contained, model 7816 programs both 2708 and TMS 2716 EPROMs and requires no personality module or host computer. Operation is based on a 2k-byte editing RAM. Data may be entered into RAM from keyboard, master socket, or serial interface where it can be examined and modified as required. When editing is complete, the contents of the RAM are programmed into the copy P/ROM. After programming, copy is automatically verified against the RAM and a 4-digit checksum is displayed. Separate copy and read only master sockets prevent accidental damage to the master P/ROM. The unit includes RS-232-C serial interface with keyboard selectable baud rate, and data entry and command keyboard with 8-char alphanumeric display. **RMD Inc,** PO Box 206, Bristol, PA 19007. Circle 258 on Inquiry Card

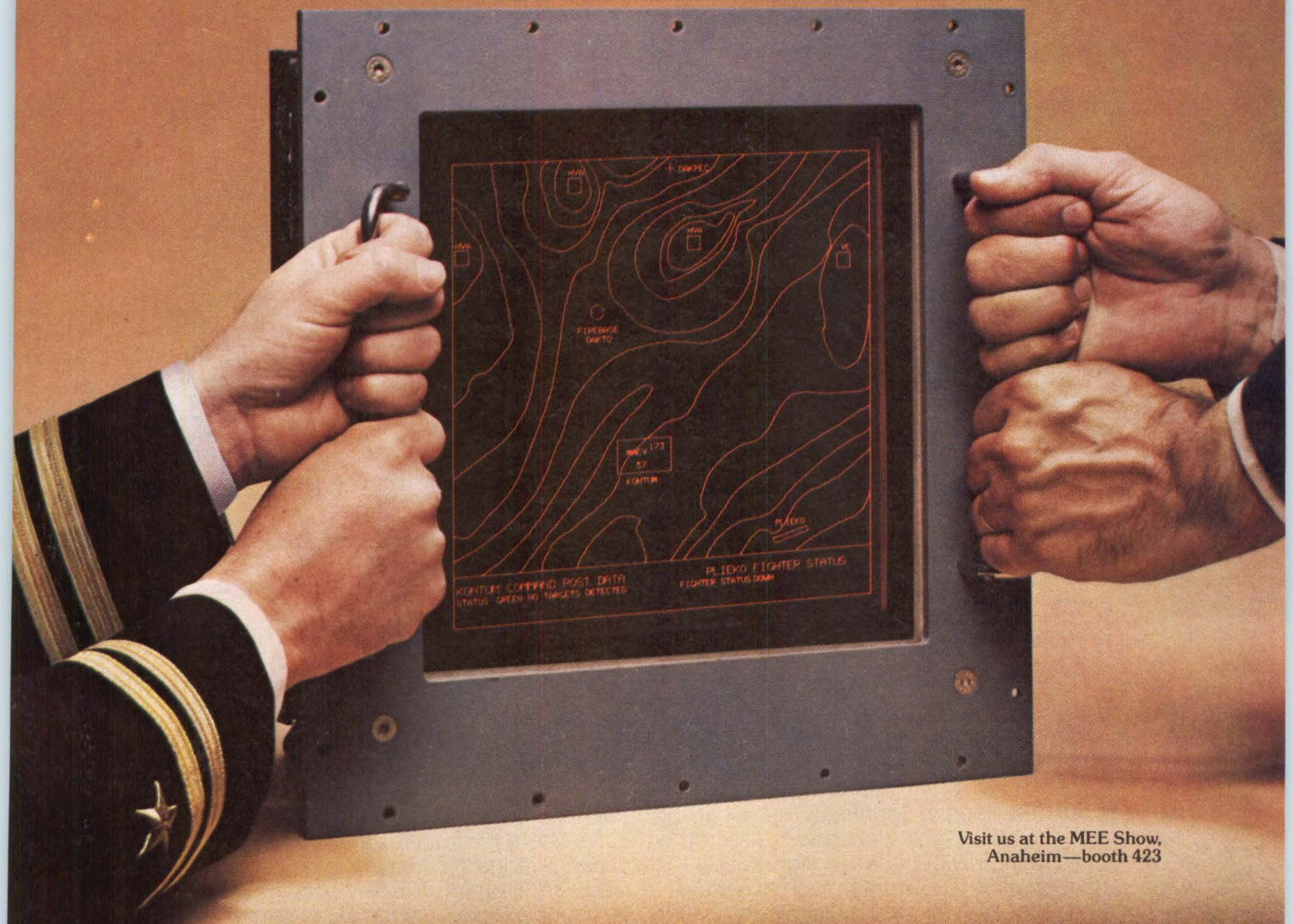


LASER BAR CODE SCANNER

Metroscan MS 106, plug compatible with lightpen systems, gives accurate high speed scans with minimal operator training and involvement. In addition to the laser scanner the unit includes a microcomputer for decoding labels and managing data, an optional CRT, and optional printer. System has a plug-in modem board and selectable baud rate. The beam from a low power (BRH Class II) helium-neon laser is scanned in a fine line that can read small labels at distances from 2 to 6″ (5 to 15 cm). This reduces wear since the scanner doesn't touch the labels; it can even read them through glass or plastic. Extra accuracy is assured by the high scan rate and constant speed; at 40 scans/s each label is read several times. Scanner mounts in any orientation for operator convenience and is ruggedly built to withstand abuse. The microcomputer decodes and validates the signal from the scanner and can interface with a line printer or computer. The unit can be programmed to read Codabar, UPC, or other bar codes on tubes, cartons, bottles, or packages. **Metrologic Instruments, Inc,** PO Box 307, Bellmawr, NJ 08031.

Circle 259 on Inquiry Card

Until today you couldn't get your hands on a plasma display without the terminal. Today you can.



Visit us at the MEE Show, Anaheim—booth 423

Introducing Interstate's PDA 300 Plasma Head. Tough, bright, with more than 10,000 hours of service life.

Now you have the flexibility to design in a rugged, long-life plasma display in tough system environments with Interstate's flat-panel PDA 300 Display Head. It displays alphanumerics/graphics, and is TTL compatible for easy interface. Inherent memory eliminates display refresh, and the unit is totally digital with no analog circuits. It has a thin profile and is designed to help meet your system RFI/EMI requirements. Optional equipment includes a touch panel, variable brightness control, rack mount, and remote-mounted power supply.

Today, for your best buy decision, consider how the PDA 300 designs into your display system. Deliverable Immediately.

For more information, call or write Don Poulos, Product Manager, Interstate Electronics, 1001 East Ball Road, P.O. Box 3117, Anaheim, CA 92803. (714) 635-7210.

INTERSTATE ELECTRONICS CORPORATION

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Information Processing and Display. Systems. Products. Services.

CIRCLE 151 ON INQUIRY CARD

Qume introduces the Wide-Body Terminal.

Thanks to our new Sprint 5/WideTrack™ Terminal, the days of worrying about wide-document preparation are over. The Sprint 5 WideTrack is a high-quality, letter-perfect printer that's wide enough to handle balance and ledger sheets, accounting reports, over-size-paper printing masters, multiple-page form letters, charts, visual aids, and even special word processing applications. And you can interface it to the Serial RS-232C interface port of your minicomputer. The possibilities are endless.

The Sprint 5 WideTrack is the widest printer on the market today. It spaces 264 columns at 10 characters per inch, 316 columns at 12 characters per inch, and can space in increments of 1/120-inch left or right. Vertical spacing is 1/48-inch up or down, and you control it through the MOS/LSI microprocessor's extensive set of software commands.

As the newest member of the proven Sprint 5 family of terminals, the Sprint 5 WideTrack offers all of the features that have made Sprint 5 an acknowledged leader in the quality font terminal industry. Features like MOS/LSI microprocessor electronic logic. Like the same printer mechanism that guarantees letter-perfect printing and RS-232C Serial Interface. Plus all of the things that have earned Qume its reputation for uncompromising quality and reliability in the thousands of printers that have been produced and delivered worldwide.

The Sprint 5 WideTrack. It's just one more in a continuing supply of innovative new products that Qume has developed to meet the needs of your growing market. And it's available today.

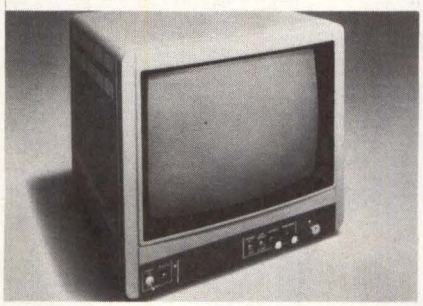
For more information on Sprint 5 WideTrack and our complete family of quality data terminals, just contact your nearest terminal dealer or Qume, 2350 Qume Drive, San Jose, California 95131.

Qume®

Qume sales offices: California: Santa Clara (408) 727-6930, Torrance (213) 326-7812. **Georgia:** Stone Mountain (404) 294-0788. **Illinois:** Oak Brook (312) 323-2802. **Massachusetts:** Needham (617) 449-1052. **New Jersey:** Upper Saddle River (201) 327-4244. **Texas:** Dallas (214) 688-0074.

PRODUCTS

HIGH RESOLUTION COLOR CRT MONITORS



HM-2619/13 and 2719/13 use wide video bandwidth and a 0.31-mm spacing between triad pairs to provide for a trio-dot density twice that of conventional monitors. 2619/13 uses a 19″/13″ (48/33-cm) trio-dot shadow mask CRT with a 0.31-mm pitch for resolution of 1280/720 trio-dots horizontal and 960/540 vertical. This provides for misconvergence of <0.6/0.7 mm within a circle whose diameter is equal to the vertical height of the display. **Hitachi America, Ltd,** 100 California St, San Francisco, CA 94111.

Circle 204 on Inquiry Card

MINIFLOPPY DISC STORAGE SYSTEM

Model 400 communication storage unit adds data storage, editing, and communication capability to distributed processing systems. The Z80 based microcomputer system performs file management, forms entry, and editing tasks, while handling the unit's communications protocol. Typical applications are communications store and forward, message handling, local program storage, and baud rate converter. Batch mode is useful for data logging and remote data collection where front panel control or simple command codes are required. Data transfers occur at rates up to 19.2k baud over an RS-232 interface; storage capacity is 180M bytes on a floppy disc. Software resides in permanent memory. Self-initialization allows use of unformatted diskettes. **Columbia Data Products, Peripherals System Div,** 9050 Red Branch Rd, Columbia, MD 21045.

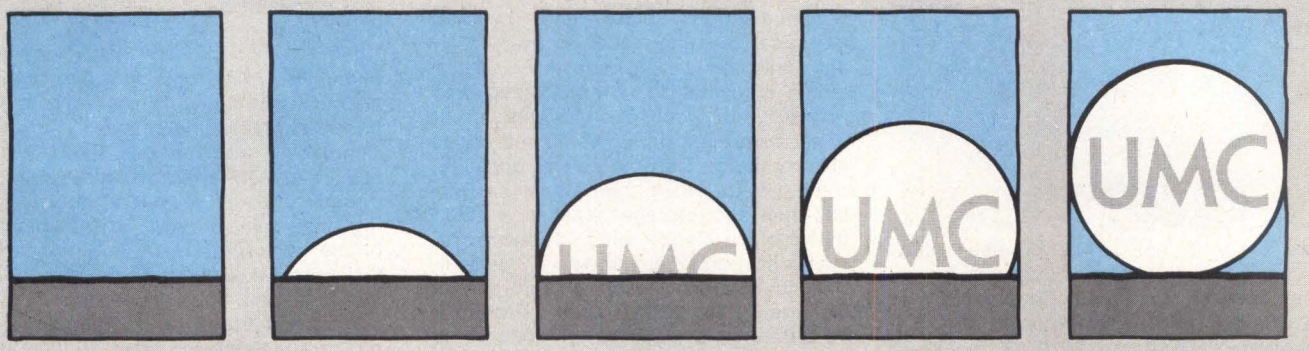
Circle 205 on Inquiry Card

DIRECT CONNECT ORIGINATE ONLY MODEM

Immunity from room noise and mechanical vibrations is provided by the portable M103 originate only modem. Compatible with the Bell 103/113 data sets, the FCC approved modem plugs directly into the telephone network using the conventional RJ11C modular phone jack or DAA. It connects to any terminal with an RS-232 or 20-mA interface and operates at a max data rate of 450 bits/s asynchronously over ordinary telephone lines, full duplex with or without local copy. Input power is 115 Vac ±10%, 50/60 Hz. Power consumption is 3 W max. Other features are red LED indicators for power and carrier detect, line connect/disconnect switch, and optional local copy. Amb operating temp is 0 to 50 °C. **Modtech, Inc,** 1958 Helsinki Way, Livermore, CA 94550.

Circle 206 on Inquiry Card

PDP-11 ready for the 80s?



The future is here. The decade is dawning. Upgrade your PDP-11 for work of a new age.

Upgrade your PDP-11 by front-ending it with our UMC processor system. It plugs into your UNIBUS, shares work with your PDP-11, and gives you powerful yet independent processing.

Use it to support network expansion. Have it control data acquisition, translation, formatting and processing. Or maybe emulate peripheral controllers. Or serve as terminal concentrator.

The UMC is a modular system of boards and support software. Since it's modular, it's flexible. It conforms and grows to meet your needs.

The UMC Processor Board might be all you need. You get a Z80 microprocessor, 4K bytes static RAM and room for 16K bytes PROM. Plus 2 full-duplex serial lines and up to 3 DMA channels.

Need more memory? A UMC Memory Expansion Board gives up to 64K bytes RAM and space for 32K bytes PROM. Need *more* memory? Add others at any time—up to a whopping megabyte.

Extra serial lines? Our UMC Serial Line Expansion Board accommodates up to 16 full-duplex lines. It has up to 8 Z80-CPUs, each with dedicated expandable memory. Extra lines? Extra boards! A system of more than 100 low-baud-rate lines is possible.

Custom work? Use our ProtoHex Wirewrap Board. It has universal layout and access to all UNIBUS and UMC Bus signals.

And as for software, run our Software Development System in your PDP-11 to support writing UMC software. Or maybe you need a turnkey network program, available soon for 2770, 2780, X.25 and other protocols.

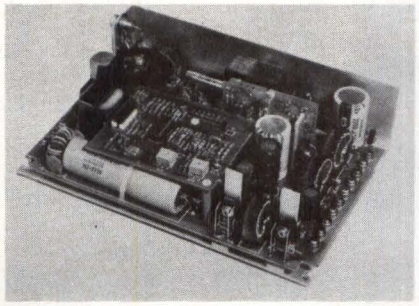
How can the UMC serve you? Check with ACC today. It may just put your system in a whole new light.

Brighten your future!

ASSOCIATED COMPUTER CONSULTANTS
228 EAST COTA STREET, DEPT. F, SANTA BARBARA, CA 93101.
(805) 963-8801. TWX 910 334-4907.

PRODUCTS

5-OUTPUT, 200-W SWITCHING POWER SUPPLY



ESM-200 features high component density using the company's monolithic chip for max wattage/in^3. The std unit has a 5-V regulated output and 2 12- or 15-V regulated outputs, plus 5- and 24-V semi-regulated outputs. Special units may be specified from 5 to 28 V for each of the 3 regulated outputs and 5 to 50 V for the 2 semi-regulated outputs. Line regulation is 0.2%, while load regulation is ±0.2% on the first 3 outputs and ±5% on the last 2 outputs with cross regulation of ±3%. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.
Circle 207 on Inquiry Card

DATA DISPLAY TERMINAL

Data are entered or retrieved from computer systems by the 7900 Model I interactive data display terminal. Built-in shields protect against emi, rfi, and electrostatic discharge. The microprocessor based system features a 12″ (30-cm) green phosphor screen, with a displayed terminal status line. Asynchronous mode operation is at rates up to 19.2k baud. Special function keys and std adding machine style keypad comprise the typewriter style keyboard. Up to 96 function codes can be user generated. **NCR Corp,** Dayton, OH 45479. Circle 208 on Inquiry Card

FLOPPY DISC CONTROLLER

As a std for double-density disc controllers, TWO-X provides over 500k bytes on each side of an 8″ (20-cm) double-headed floppy disc drive for 1M bytes/drive or a total of 2M bytes of online storage in a double-headed 2-drive system. Data transfer rate of 500k bits/s at double-density incurs an error rate of <1 recoverable error/ 10^9 bits read. Up to 4 8″ (20-cm) or 3 5″ (13-cm) drives are supported. Also included is an 8251 UART RS-232 serial port. **CMC Marketing Corp,** 10611 Harwin Dr, Suite 406, Houston, TX 77036. Circle 209 on Inquiry Card

32-CHANNEL A-D CONVERTER

Designed for use with the STD BUS, the ST4303 12-bit A-D converter has an accuracy of 1 part in 4096 (½ LSB). It accepts inputs from 32 differential or single-ended input sources with voltage ranges of ±2.5, ±5.0, ±10.0, 0 to 5, or 0 to 10 Vdc. Max conversion time is 10 μs for same channel conversion; switching channels adds 2 to 7 μs. The converter is available in the full 32-channel configuration, or in increments of 8, 16, or 24 channels. **Applied Micro Technology,** PO Box 3042, Tucson, AZ 85702.
Circle 210 on Inquiry Card

SWITCHING POWER SUPPLIES

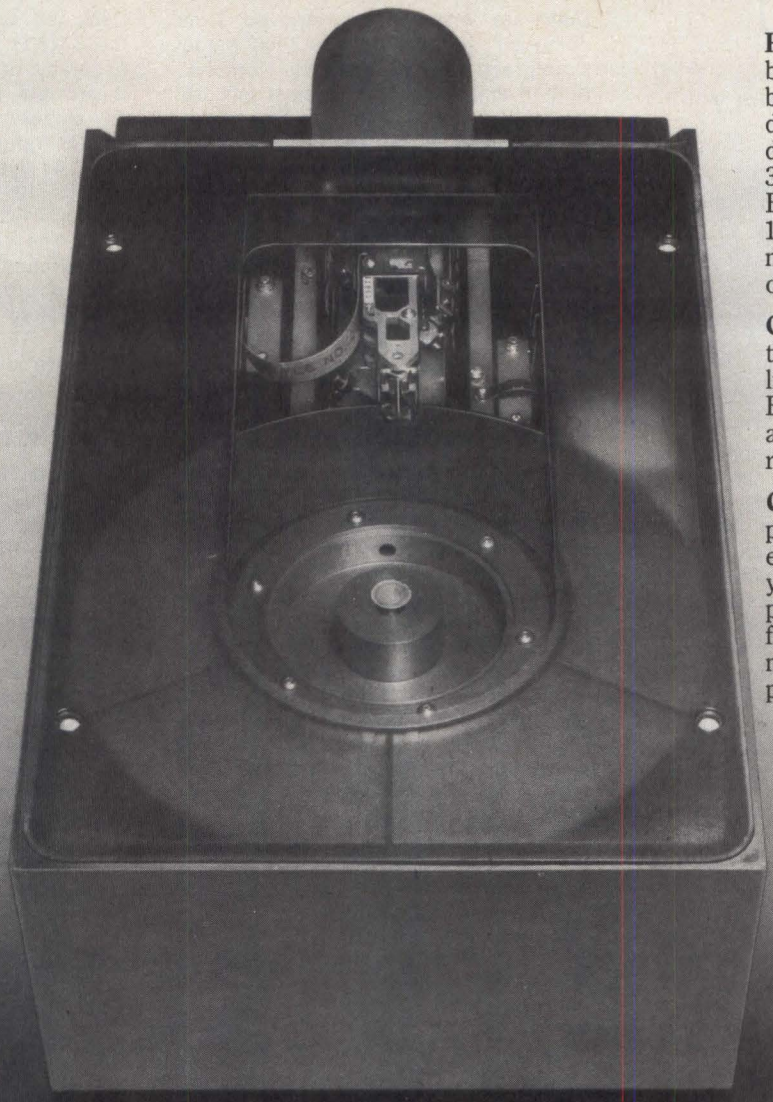
SB series feature both 115- and 230-Vac inputs, brownout protection, tight regulation, and MTBF of 100k hours. Supplies will operate over an input range of 115/230 Vac +10%, −20%. Input frequency can be 47 to 440 Hz. There are 30 models available with single 5-, 9-, 12-, 20-, and 24-V (±10%) outputs rated at 30, 55, 100, 150, 200, and 300 W. Line regulation is <0.2% for the input range, and load regulation is <0.2% for no load to full load. **KEC Electronics, Inc,** 21535 Hawthorne Blvd, Torrance, CA 90503. Circle 211 on Inquiry Card

Introducing the new BASF 6170 Series 210mm Fixed Disk Drives.

High Performance. Perfect for multi-user multi-tasking applications, the BASF 6170 Series drives give you an average time-to-data of 50 milliseconds...four to seven times faster than standard 8" floppy drives.

Capacity. The BASF Model 6171 provides 8 megabytes and the Model 6172 provides 24 megabytes of fully usable unformatted capacity. Unique BASF circuitry eliminates user mapping.

Easy System Integration. BASF's exclusive SMD interface option offers cost-effective and convenient interface compatibility with industry-supported controllers. Low-cost BASF disk bus, or intelligent BASF host bus with integral controller/formatter also available.



Proven Reliability. BASF, because of its experience in both magnetic media and drives, is highly qualified to develop drives using reliable 3350 Winchester technology. BASF 6170 drives have a 10,000 hour MTBF and require no scheduled maintenance or operator intervention.

Compact Size. Far smaller than 14" drives, the quiet, lightweight floppy-sized BASF 6170 drives are suitable for desktop office environments.

Competitive Price. Get the performance, capacity, and ease of system integration you need right now...at prices you'd expect to pay for far less sophisticated technology. Write now for competitive OEM prices.

If you need high performance, capacity, easy system integration, proven reliability, in a compact size, at a competitive price, right now...

write now.

BASF Systems, OEM Peripheral Sales, Crosby Drive, Bedford, MA 01730
Please send me complete details and specifications on the new BASF 6170 Series 210mm Fixed Disk Drives.

Name _____ Title _____

Company _____

Address _____ Telephone _____

City _____ State _____ Zip _____

In a hurry? Call Dave Edwards at (617) 271-4168 CD

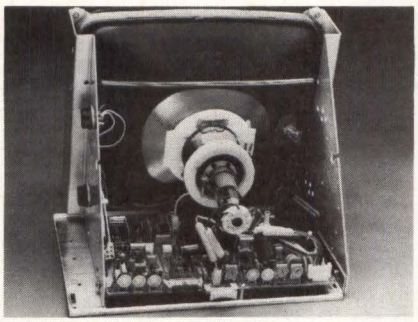
BASF

BASF

CIRCLE 157 ON INQUIRY CARD

PRODUCTS

HIGH RESOLUTION CRT MONITOR



HR-1500 raster scan monitor is capable of displaying over 1920 char in either white or green phosphor. It provides 400 active raster lines with horizontal scan rate of 25 kHz, refresh rate of 50-60 Hz, vertical step scan, and dual intensity. The 15″ (38-cm) diag CRT screen is nonreflective, using an etched bonded faceplate to eliminate glare. Electronic components are packaged in one easy to repair board. **Telex Computer Products, OEM Div,** 6422 E 41st St, Tulsa, OK 74135.
Circle 212 on Inquiry Card

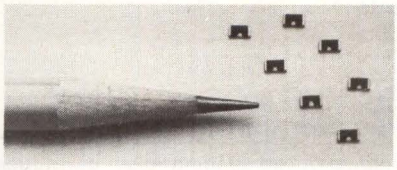
MULTIPLEXER TEST SET

PCM transmission, terminal, and multiplexer testing at 1.544M, 3.152M, and 6.312M bits/s is facilitated by the model S5102 DS1/1C/2 test set. It can measure bit error rate through an M1C or M12 multiplexer with different receive and transmit rates. Built-in latching status indicators and a timer permit long-term unattended measurements of total errors and errored seconds. The set comprises a separate receiver and transmitter, each housed in a portable case. **Tau-Tron, Inc,** 27 Industrial Ave, Chelmsford, MA 01824.
Circle 213 on Inquiry Card

300-LINE/MIN PRINTER

Plug compatible with IBM 3271, 3272, or 3274(B) control units, the LABEL/300 model 1C/3270 generates variable size char 0.1 to 2.8″ (0.3 to 7 cm) with variable aspect ratio. The printer operates both as a std 300-line/min printer and as a special char printer. Font options provide italics, reverse, half-tone, and overprinting. Interfaces and protocols allow connection to almost any host computer. **Technical Analysis Corp,** 120 W Wieuca Rd, NE, Atlanta, GA 30342.
Circle 214 on Inquiry Card

WAVE SOLDERABLE CHIP RESISTORS



MCR-18, a thick film chip resistor, attaches directly to either side of a PC board and is flow soldered along with other components. In conjunction with automatic mounting methods, devices offer improvements in packaging density, production costs, and reliability. Measuring 0.125 x 0.062 x 0.023″ (3.2 x 1.6 x 0.6 mm), the unit has tolerances of ±2, ±5, or ±10%, and is multirated from 0.0625 to 0.5 W. Values range from 2.2 to 10M Ω. **R-Ohm Corp,** PO Box 19515, Irvine, CA 92713.
Circle 215 on Inquiry Card

INTELLIGENT TERMINAL CONTROLLED SWITCH

Micro600 port selector, based on the 610 intelligent port selector, provides enhancements including support of current loop interface terminals and integral Bell 43401 local datasets for short haul data transmission. Any asynchronous terminal may be connected to the unit directly or by means of dial-up or dedicated modems or integral local datasets, to contend automatically for the computer ports attached to the unit. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.
Circle 292 on Inquiry Card

SUBMINIATURE LED REFLECTIVE SCANNER

LED reflective scanner S13224 can detect a 0.03" (0.76-mm) target at a distance of 0.3" (7.6 mm) and is able to detect small objects up close and white bond paper as far away as 1" (2.54 cm). Unit consists of IR LED, collimating lens, and matched photosensor in aluminum body. IR energy focused on target is reflected back to photosensor. Filter protects sensor from ambient visible light and attenuates most radiation from other light sources. **Skan-A-Matic Corp,** PO Box S, Elbridge, NY 13060.
Circle 294 on Inquiry Card

PRINTER CONTROLLER CARD

Magnum-3270 microprocessor controller for the Printronix 300 printer is contained on the same 9 x 12" (23 x 30-cm) card that creates variable print and bar codes for the printer. This device emulates the IBM 3284, 3286, and 3288 printer via coax connection to IBM 3270 type equipment. IBM /360, /370, or System/3 computers can thereby create block letters from 0.1 to 12" (0.3 to 30 cm) high and position any size char anywhere on a page. **Quality Micro Systems,** PO Box 1644, Mobile, AL 36601.
Circle 296 on Inquiry Card

10M- TO 12.5M-BYTE DISC CARTRIDGES

Front and top loading disc cartridges for 10M- to 12.5M-byte drives are designed and tested for use with the units manufactured by Data General, Hewlett-Packard, and Perkin-Elmer (Wangco). The cartridges feature a 0.075" (1.905-mm) metal substrate and a proprietary coating and are 100% certified to OEM standards. Both front (style 2315) and top (style 5440) loading configurations are available to match drive and system requirements. **Athana Magnetic Media,** 1815 Mullin Ave, Torrance, CA 90510. Circle 293 on Inquiry Card

RECEIPT/AUDIT PRINTER

Dot matrix impact printer with split paper feed for receipt applications offers 3-line/s bidirectional printing and 10-line/s line feed, and prints two 18-char columns at 12 char/in (4.7/cm). Line width of the M-520 is 1.5" (3.8 cm); paper width is 1.75" (4.45 cm) for each roll. The printhead consists of 7 clapper type solenoids which activate 7 printwires, and is designed for continuous service without overheating. Printhead life is 100M char. **LRC, an Eaton Co,** Technical Research Pk, Riverton, WY 82501.
Circle 295 on Inquiry Card

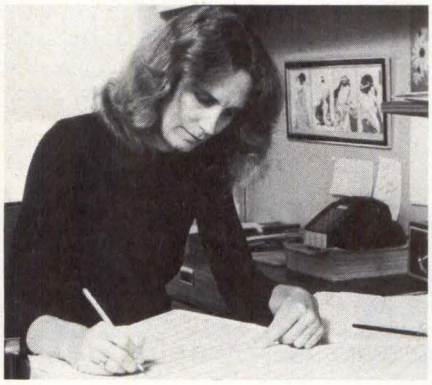
14-BIT MULTIPLYING DAC

Encased in a 24-pin double-DIP, DAC9331-14 maintains ±0.003% linearity over the specified 0 to 70 °C temp range. Dynamic laser trimming assures max accuracy and temp tracking of precision, thin-film ladder network and internal feedback resistor. Compatible with TTL/DTL and CMOS logic, the unit operates from a single 5- or 15-V supply and consumes a max of 30 mW. Reference input range is ±25 V; digital input coding is binary or offset binary for 2- or 4-quadrant multiplying operation, respectively. **Hybrid Systems Corp,** Crosby Dr, Bedford, MA 01730.
Circle 297 on Inquiry Card

TTI SYSTEMS AND SOFTWARE PROFESSIONALS

A dedication to progress.

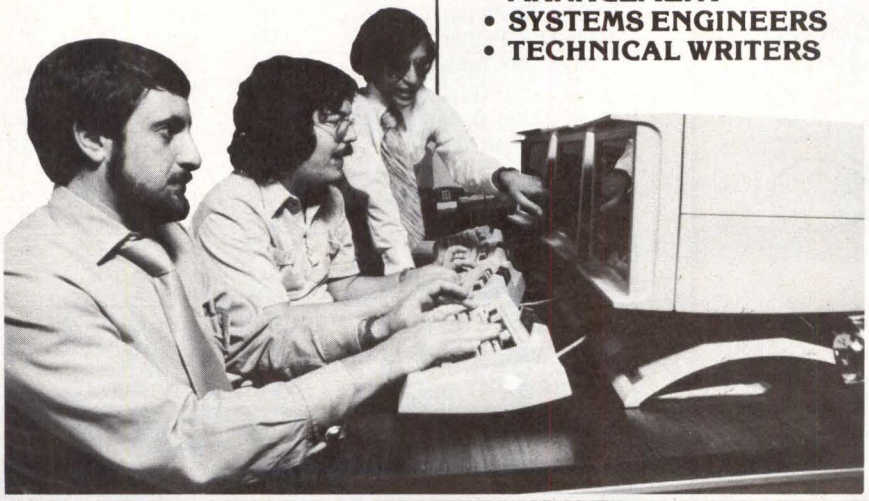
At TTI, we're excited about the future and we've created an environment where new ideas are respected and progress is the goal. We're constantly seeking talented and creative



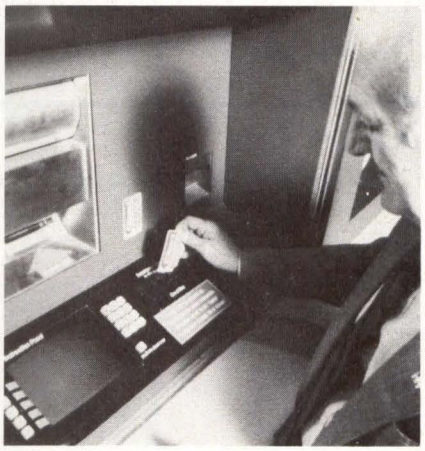
professionals who are committed to producing the highest quality technical achievements — like the sophisticated banking systems we designed for Citibank, one of the world's largest financial institutions, utilizing the latest in state-of-the-art Electronic Funds Transfer Systems (EFTS). More importantly, we're searching for people who are as excited by change and dedicated to it as we are.

Besides providing career-oriented individuals with advanced technical challenges, TTI is a firm believer in seeking out and encouraging individual recognition and advancement. Now is the ideal time to bring your expertise into one of the following career assignments:

- **SYSTEMS PROGRAMMING**
- **ON-LINE APPLICATIONS PROGRAMMING**
- **TEST ANALYSIS**
- **PRODUCT DESIGN**
- **DIAGNOSTIC PROGRAMMING**
- **TECHNICAL MANAGEMENT**
- **SYSTEMS ENGINEERS**
- **TECHNICAL WRITERS**



Selected candidates will find an outstanding environment offering total career satisfaction. For an immediate professional review, qualified individuals are invited to forward a detailed resume, complete with salary history, in confidence to: Nancy Stockinger, CD31 Professional Staffing.



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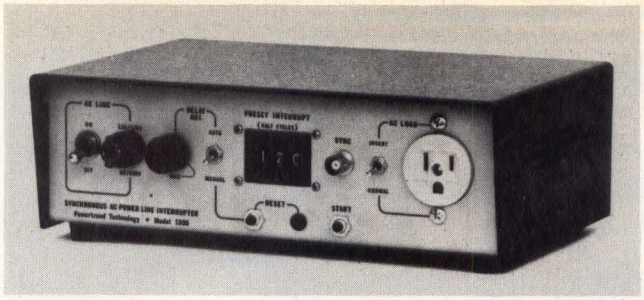
CIRCLE 162 ON INQUIRY CARD

POWER SUPPLY TEST SET



Model 1500 synchronous ac power line interrupter can simulate line voltage dropouts or apply ac load power for preselected intervals ranging from 0.5 to 499.5 cycles in half-cycle increments. A TTL level sync pulse is available for triggering external monitoring equipment and an autotriggering mode permits continuous cycling of loads for life testing. Interrupts are synchronized with zero-crossing of the ac line voltage for min load stress and rfi. The unit features all solid state circuitry and can handle loads rated up to 1.5 kW with wide ranging power factors. It can be used to drive an auxiliary booster for switching high load currents. Internal jumper connections permit operation from 125 or 250 Vac, 50/60 Hz. **Powertrend Technology,** 3139-G Los Feliz Dr, Thousand Oaks, CA 91360.

Circle 260 on Inquiry Card

INTEGRATED DISC STORAGE SUBSYSTEMS

Disc/diskette subsystems incorporate a 12.5M-byte fixed media disc and 1.26M-byte diskette. Available for Nova®/ Eclipse® and microNova™ computers, one model includes the 25M-byte disc and 1.26M-byte diskette, another consists of 25M-byte disc only. A third model includes both 12.5M-byte disc and diskette. Capacity of the permanent 25M-byte disc is 25,165,824 bytes formatted in sectors of 512 bytes each. There are 384 tracks/surface divided into two 192 track bands on each of 4 surfaces. A separate read/write head accesses each band. Each 8-track disc cylinder has 131,072 bytes in 256 sectors. The nonremovable 12.5M-byte disc has 12,582,912 bytes formatted in the same way, but with 4 tracks/cylinder. The diskette uses media with 77 tracks/side formatted into 16 sectors of 512 bytes. Exact capacity is 1,261,568 bytes. Data transfer to/from memory is at a 62,500-byte/min rate. Head positioning times, including seek settling are 25 ms track to track, 100 ms random avg, and 253 ms max. Rotational latency at 360 r/min is 83.3 ms. **Data General Corp,** Rt 9, Westboro, MA 01581.

Circle 261 on Inquiry Card

SINGLE-STATION PUSHBUTTON SWITCH

Series BXL Box Switch offers the option of incandescent or LED illuminated, or nonilluminated face as well as selection of either momentary or push-lock/push-release mechanism. The LED version features a translucent lens 0.156 x 0.25" (3.96 x 6.35 mm) centered on the pushbutton face in red, green, yellow, or orange. Incandescent and nonilluminated faces are molded of translucent plastic in white, red, green, blue, yellow, orange, or black. Solder lug/quick connect terminals are std. Leads may be soldered; or AMP Faston series 110 receptacles may be used. Mounting is in 0.625" (15.88-mm) square holes in panels from 0.031 to 0.093" (0.79 to 2.36 mm) thick. Locking tabs integral with the switch housing hold the switch securely. **Switchcraft, Inc,** 5555 N Elston Ave, Chicago, IL 60630.

Circle 262 on Inquiry Card

PORTABLE DIAGNOSTIC DATA COMMUNICATIONS TEST SET

Designed to monitor and interactively communicate with data appearing at the EIA RS-232 interface, the Hawk 4010 Datatrap displays data traffic on a 5" (12.7-cm) CRT. Capabilities are accessible through menu pages displaying instrument configuration status. The microprocessor based unit quickly locates and isolates problems in hardware and software by simultaneously displaying both transmit and receive data. It can be programmed to trap and store 4096 char and recall this data for detailed visual analysis. Operating with synchronous data rates up to 19,200 bits/s in both half- and full-duplex modes, the set provides asynchronous operation through 16 internally generated clock speeds ranging from 50 to 19,200 bits/s. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02855.

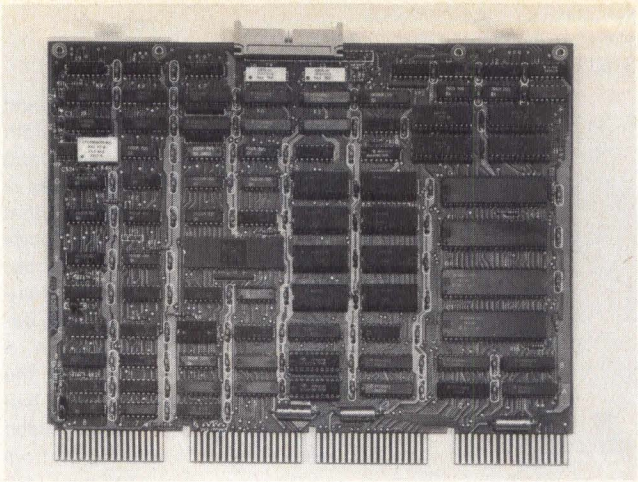
Circle 263 on Inquiry Card

DIGITAL OUTPUT BAR CODE WAND

Designed to scan bar code and output a logic level pulse width representation of bars and spaces, the HEDS-3000 uses a precision optical sensor that can read all common bar code formats printed with a min bar width of 0.3 mm. High resolution, high speed emitter/detector sensor is sealed in a module near the tip of the wand. In the module, one-half of a bifurcated precision plastic lens projects visible light from a 0.17-mm dia, 700-nm LED onto the sensing plane. The other identical lens half focuses reflected light onto an integrated silicon photodetector. An onboard transistor in the detector provides added gain. Each lens half has a numerical aperture of 0.3 for max light gathering power, and spherical aberrations are eliminated through use of aspheric lens surfaces. Signal conditioning circuitry includes analog amp, digitizing circuit, and output transistor. Energized push-to-read switch, these elements provide TTL and CMOS compatible logic level output. Unit interprets nonreflecting black bars as logic high levels (1), reflecting white spaces are read as logic lows (0). **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

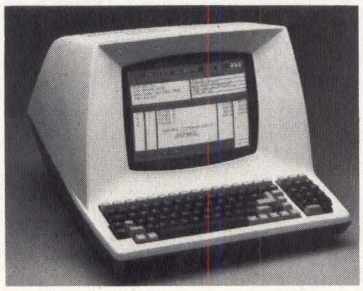
Circle 264 on Inquiry Card

WINCHESTER DISC CONTROLLER



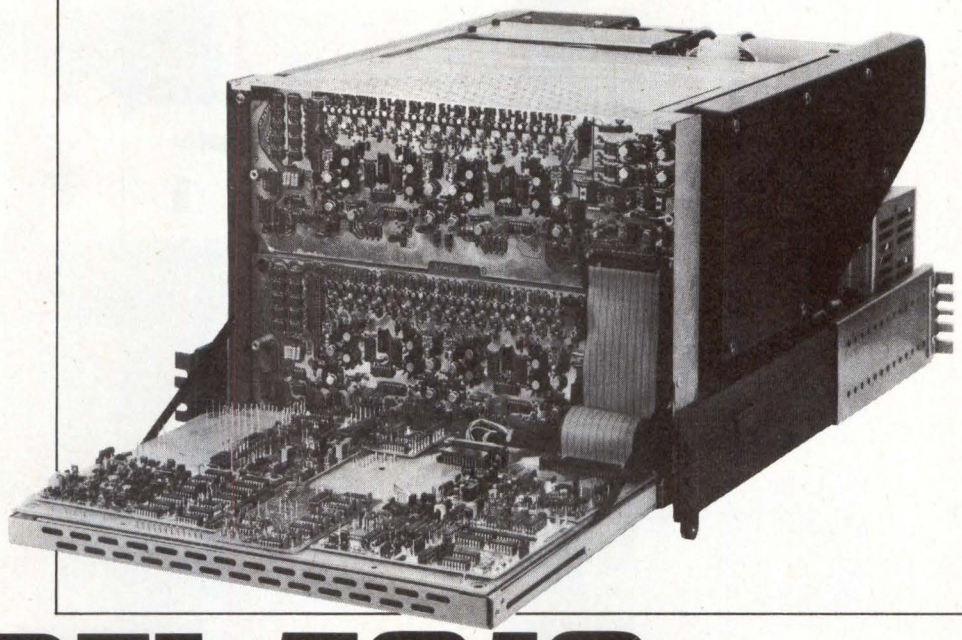
Model 530 provides up to 40M bytes of storage capacity for the DEC Q-bus family of processors. It features complete software compatibility with operating systems having RL01/RL02 support. Disc controller interface is resident on a single 2-sided, quad-width printed circuit board that measures 8.5 x 10″ (21.6 x 25.4 cm). Controller uses a bit slice microprogrammable processor along with the company's micromodule approach to design. Most current Winchester disc drives are supported including the BASF 24M byte and IMI 10M byte 8″ (20-cm) drives, and Century Data Marksman 14″ (36-cm) units. The micro module design technique allows for future expansion to handle other disc drives up to 960M bytes with simple ROM changes. Throttle and interleaving techniques synchronize each disc drive to the Q-bus, 8-sector buffering eliminates potential data lates. A CRC value computed by controller during each write operation is automatically appended to the end of each data and header field. This value is compared with the CRC value computed during read to detect errors. **Xylogics, Inc,** 42 Third Ave, Burlington, MA 01803. Circle 265 on Inquiry Card

MICROPROCESSOR CONTROLLED CRT TERMINALS



Included as standard in all models of the smart terminals are upper and lower case, printer/extension port, imbedded numeric pad, remote computer control, selectable transmission rates from 75 to 9600 baud, and editing and special functions. A serial RS-232-C communications interface and 20-mA current loop are also std. Models 920B and 920C differ from the 912B and 912C in that they offer 11 special function, 6 editing, and 2 transmission keys, all contained in an additional row on the keyboard. Keyboards are Teletype style in B models, and typewriter style in C versions. A second page of memory is optional in all. Editing and transmission functions are key selectable, and include char and line insert/delete, line and page erase, send line, send page, and tabbing. Reverse video, underline, and blink and blank are offered plus key controllable conversational and block transmission modes, built-in self-test, and protected fields. Nonglare 12″ (30-cm) diag CRT screen provides 12 x 10 dot matrix resolution and dual intensity for 1920 char. **TeleVideo, Inc,** 3190 Coronado Dr, Santa Clara, CA 95051. Circle 266 on Inquiry Card

RELIABILITY: 28,000 hr. MTBF.
ECONOMY: .035 cents per bit.



VRC MODEL 4016 MEMORY

When it comes to speed, reliability and low cost, systems users in 25 countries in every continent of the world depend on the VRC 4016 head-per-track memory.

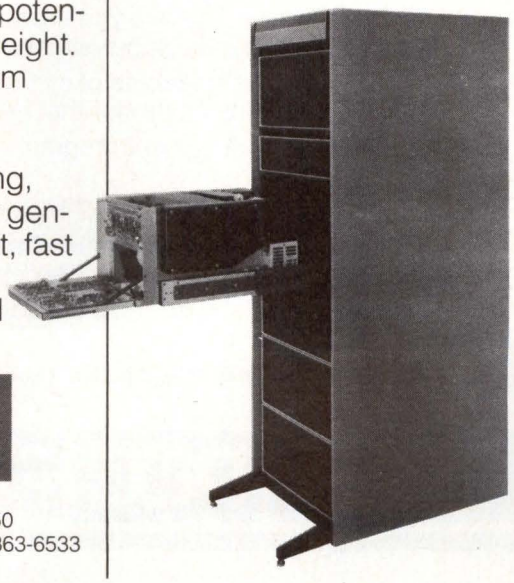
It features a fail-safe actuation system that eliminates the potential of media damage and data loss. It's compact and lightweight. All electronics, drive components and head retraction system are mounted outside the drum, making service simple and eliminating risk of contamination.

Applications are endless. Telecom and message switching, process control of all kinds, geophysical exploration, power generation, news editing, typesetting. Wherever low cost-per-bit, fast access and high data storage capacity are required.

For proven reliability, worldwide support, field service and predictable high quality, you can rely on VRC.

Write or call for complete details on the Model 4016 head-per-track memory...a simple, rugged, compact unit to improve the reliability of your system.

CAPACITY . . .	37.9 million bits
BIT RATE	4.33 MHz
ACCESS TIME	8.5 m/sec.
DIMENSIONS	Height – 12¼" (31.2 cm.)
	Width – 17½" (44.5 cm.)
	Depth – 22" (55.9 cm.)
MEAN TIME TO REPAIR . .	Less than 1 hr.



Vermont Research
CORPORATION

Precision Park
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CIRCLE 169 ON INQUIRY CARD

Pick a PCC that'll

Pick this Microperipheral® bundle and you can put together a floppy disk sub-system to meet *your* design needs.

One more example of how we save you development time and money. Because we do all the work for you. We "bundle" together the ideal sub-systems, provide all the equipment (our own) and service them, too.

Example—the 3812. A full megabyte of microcomputer formatted storage. Two floppy disk drives. Power supply. Built-in dual-density controller that handles up to four drives.

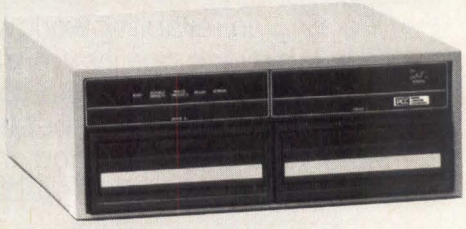
The 3812 lets you use your current programs because it reads and writes in single- or double-density. You save on design simplification.

You can use S-100 bus, Intel Multibus,™ Motorola Exorcisor™ and other interfaces.

It's IBM format compatible. Its retractable heads are long-lasting ferrite.
You can have an optimal direct memory access data transfer to and from disk.

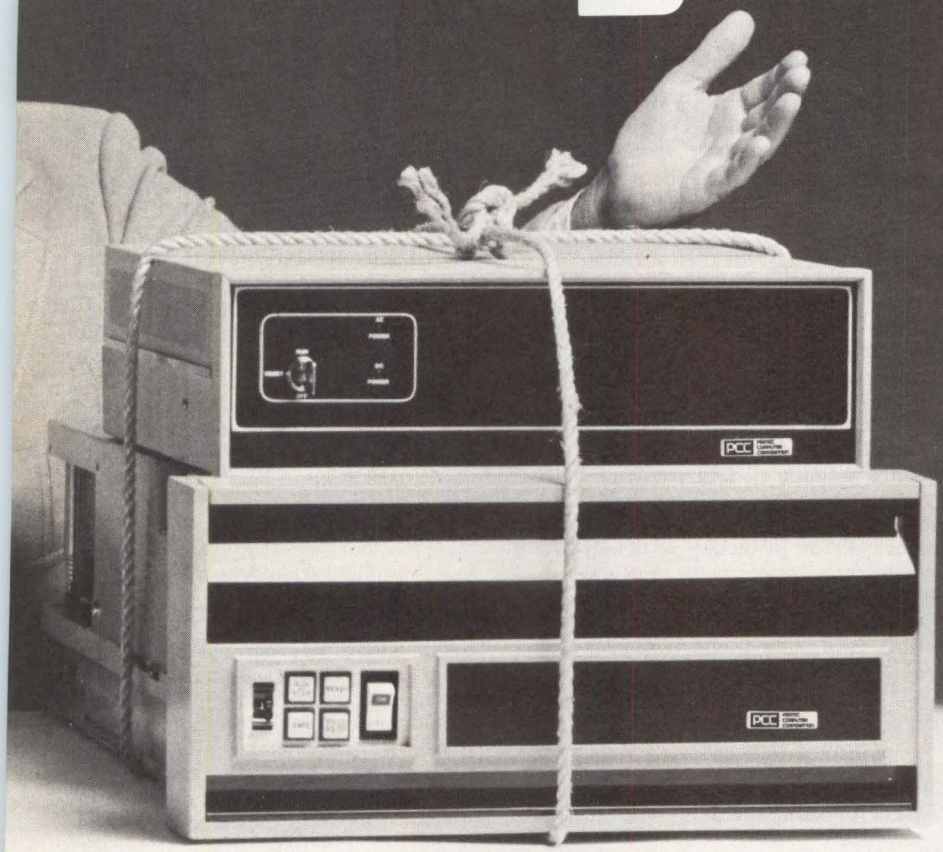
The 3812 operates under CP/M.® It supports Microsoft's FORTRAN, COBOL and BASIC.

It's the best sub-system we make. Except for the bundle on the right.



PCC SYSTEMS
PERTEC COMPUTER CORPORATION

bundle save you one.



Pick this Microperipheral bundle and you can put together 40MB from one hard disk sub-system.

One more example of how we save you development time and money. Because we do all the work for you. We "bundle" together the ideal sub-systems, provide all the equipment (our own), software and interfaces. And we service them, too.

The 4511. We start with 10MB—5MB fixed, 5MB removable. We then include a controller that lets us daisy-chain three drives to it. Which means it can go all the way up to 40MB.

We also include performance in the bundle. The 4511 has 40 Msec average access time. It transfers data at 2.5MHZ. It has a security controller that's bus-oriented, with key-lock.

It speaks FORTRAN, COBOL and BASIC. It has CP/M®

It's the best sub-system we make. Except for the bundle on the left.

The 4511 and 3812 are products of Pertec Computer Corporation, an international company that designs, manufactures and services computers and computer equipment. Microperipherals® is a registered trademark of Pertec Computer Corporation.

For more information, write Ray Kristiansen, Pertec Computer Corporation, 20630 Nordhoff Street, Chatsworth, California 91311. Or call toll-free 800-331-1001 in the continental U.S. (In Oklahoma, call collect 918-664-8300).

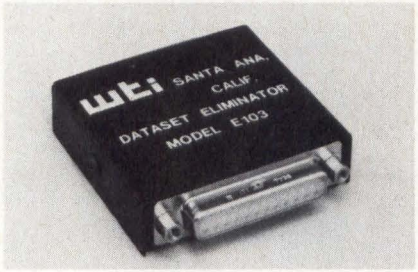
CIRCLE 170 ON INQUIRY CARD

PRODUCTS

PC BOARD TERMINALS

Rugged 1-piece contacts of terminal blocks provide low resistance connections to solid or stranded wire up to 14 AWG. Round, 1-mm dia solder pins, spaced 5.08-mm on centers, are suited to wave-solder installation on boards up to 3.2 mm thick. Tubular clamp contacts with self-locking screws accept stripped wire ends directly. Type LSV blocks, in lengths of 3, 4, 5, or 6 terminals, are rated 8 A at 150 V; MiniMod blocks, in lengths of 2 or 3 terminals, are rated 5 A at 150 V. **Cogenel, Inc, Entrelec Div,** Two Ram Ridge Rd, Spring Valley, NY 10977.
Circle 224 on Inquiry Card

MODEM ELIMINATOR

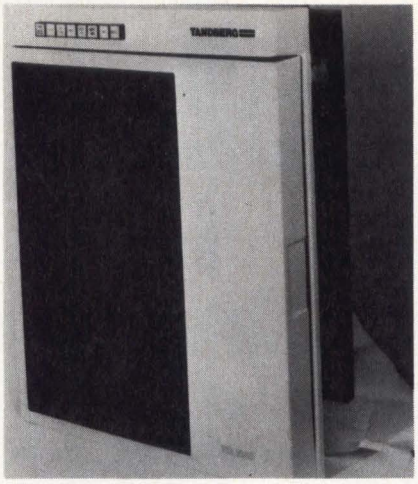


Model E103 eliminates the need for 2 modems or acoustic couplers when connecting an RS-232 I/O terminal directly to a nearby computer, or connecting terminal to terminal with a distance of 1000′ (304 m). The unit features asynchronous operation in full- or half-duplex at up to 1200 baud. Connection is accomplished by plugging the 25-pin RS-232 connector from the terminal in either E103 plug, and the cable from the CPU in the other. **Western Telematic, Inc,** 2435 S Anne St, Santa Ana, CA 92704.
Circle 225 on Inquiry Card

HERMETICALLY SEALED SIP RESISTOR NETWORK

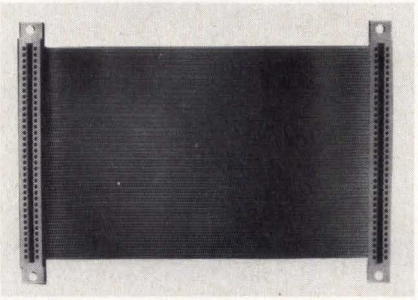
Miniature resistor networks in hermetically seam-sealed, 10-lead ceramic packages conform to MIL-STD-883B. Available resistor values range from 20 to 2M Ω, with absolute tolerances to 0.01% and ratio tolerances to 0.005%. The absolute tempco is 50 ppm std to 10 ppm on special order; TC ratio tracking is to 1 ppm/°C. Lead spacing is on 0.1″ (0.25-cm) centers. Low profile configuration has an above-board height of 0.22″ (0.59 cm). **Electro-Films, Inc,** 111 Gilbane St, Warwick Central Industrial Pk, Warwick, RI 02886.
Circle 226 on Inquiry Card

DUAL-BUFFER TAPE RECORDER FOR DATA ACQUISITION



Normally connected to a data acquisition system, DB-1050 may be used for any application requiring IBM compatible 0.5″ (1.27-cm) tape format. The data recorder with an industry standard interface provides 1600-char/in (630/cm) PE or 800-char/in (315/cm) NRZI data density at a 45-in (114-cm)/s speed. Heart of the subsystem is the TDI-1050 synchronous tape transport, which includes an embedded dual-mode formatter and a microprocessor controller with double 2048 frontend buffers. Record lengths of 2048 bytes are temporarily stored in a dual-buffer memory which achieves a 50k-byte/s data transfer rate; when 1 buffer is full, the memory content is written on tape. **Innovative Data Technology,** 4060 Morena Blvd, San Diego, CA 92117.
Circle 227 on Inquiry Card

72-CONDUCTOR CABLE ASSEMBLIES



Panel to panel and backplane to backplane interconnection assemblies mate with the company's straight and right angle cable connector families as well as with PBC edge fingers. High I/O capability (up to 72 conductors) is suitable for insulation displacement connector applications. They are available in 26, 36, 40, 50, and 72 conductors, both single- and double-ended. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 228 on Inquiry Card

RS-232 COMMUNICATION LINE MONITOR

Inline status display and true 3-level monitoring for EIA RS-232 communication lines are performed by the CMC232LT. Powered from communication lines, the monitor has 12 2-color LEDs that indicate red for mark ($\geq$3 V), green for space ($\leq$−3 V), and remain unlit for signal levels between 3 and −3 V. Low current draw of <3 mA for each LED allows continuous monitoring of marginal lines. Each signal line, except line 1, contains a DIP switch for opening any line. **Carroll,** 1212 Hagan St, Champaign, IL 61820.
Circle 229 on Inquiry Card

TAPE CONTROLLERS

Model 7800 series magnetic tape controller supports GCR at 6250 bits/in (2460/cm), PE at 1600 bits/in (630/cm), and NRZI at 800 bits/in (315/cm) tape densities. The tape controller is software and hardware transparent to host systems which may include VAX-11/780, PDP-11, Nova, Eclipse, and Interdata 7/32, 8/32, and 3220 computers. The control units allow users to read and write gapless records. **Information Products Systems, Inc,** 6567 Rookin, Houston, TX 77074.
Circle 230 on Inquiry Card

WAVE-SOLDERABLE MINIATURE SLIDE SWITCH

Contamination free Mr. Clean II (124 series) uses patented 2-piece principle. Only the exposed base of this switch is subjected to the soldering and cleaning process (fluorinated, chlorinated, or aqueous). Base has insert molded pin terminals; top half of switch which contains the switching mechanism is then snapped on the base. Hard gold over nickel barrier switches are available in spst, spdt, dpst, dpdt, and form Z circuit configurations. **Chicago Switch, Inc,** 1714 N Damen Ave, Chicago, IL 60647.
Circle 231 on Inquiry Card

GRAPHICS ALPHANUMERIC VIDEO DISPLAY CONTROLLER

Lexiscope 4000 can emulate std 96-char ASCII alphanumeric display terminals as well as provide moderately high resolution (560 H x 500 V) graphic display in Data General Nova and Eclipse series computer systems. Separate cursors and display memory allow independent programming, display, and erase of the graphic and alphanumeric screens. The display controller is contained on a single 15″ (38-cm) board that plugs directly into 1 slot in the computer mainframe. **Lexicon, Inc,** 60 Turner St, Waltham, MA 02154.
Circle 232 on Inquiry Card

PRODUCTS

PC BOARD SOLID STATE RELAYS

Synchronous switching, 2.5-A rated free-air ac switching, 3 dc input options, and industry std encapsulated packages are features of the FSSR, ISSR, and PSSR miniature relays. Each has zero voltage switching for rfi suppression, and is optically coupled for high isolation between input and output. An internal snubber network protects against false triggering by high line transients. Units are available in both 140- and 280-Vac models. **Guardian California,** 4030 W Spencer St, Torrance, CA 90503.

Circle 216 on Inquiry Card

BAC-HASP DATA CONVERTER

Communicating with host mainframe via IBM HASP multilearning RJE workstation binary synchronous protocol, converter performs all error checking and correction functions, translates EBCDIC to ASCII and ASCII to EBCDIC, and interfaces with user attached devices in serial asynchronous or byte parallel formats. Unit's multileaving feature permits console support, duplicate character compression, and bidirectional communications, allowing multiple I/O devices to operate concurrently. **KMW Systems Corp,** 8307 Hwy 71 W, Austin, TX 78735.

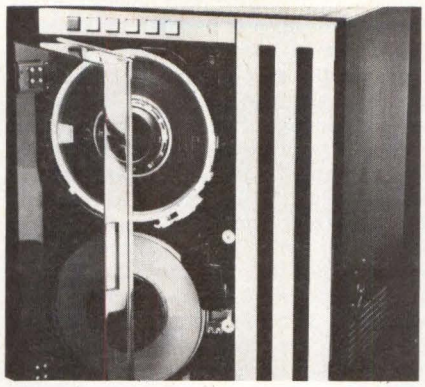
Circle 217 on Inquiry Card

MINIATURE SWITCHING REGULATORS

Offering efficiencies to 80%, the μPower-DIP dc to dc regulator series comes in input ranges of 3 to 7, 9 to 15, and 16 to 32 V, as well as a variety of output configurations. Up to 1.5 W of output power can be achieved; efficiency remains high for loads down to 0.1 W. Designed into a 14-pin DIP compatible package, devices feature low standby power drain and output protection against short circuit. External capacitors are required on each output. **Integrated Circuits Inc,** 13256 Northup Way, Bellevue, WA 98005.

Circle 218 on Inquiry Card

6250-BIT/IN TAPE STORAGE SYSTEM FOR PDP-11/70

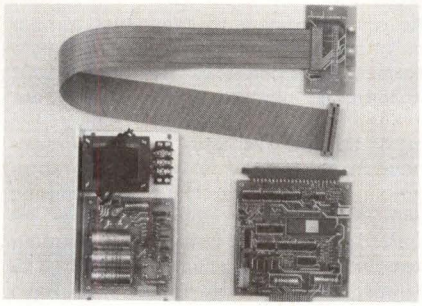


A tape transport, formatter, and tape adapter comprise the Omega, which is characterized by fast speed, large capacity storage, and easy interfacing without any changes to the DEC hardware or software. Operating at a speed of 75 in (191 cm)/s, the transport is controlled by the formatter. The system records data at 6250 bits/in (246/cm) in group-coded recording mode or at 1600 bits/in (630/cm) in phase encoded recording mode. In the former mode, a std 2400-ft (732-m) reel of tape can store approx 100M to 180M bytes of data depending on the block size being written. The intelligent tape adapter interfaces the tape transport and formatter to the minicomputer, emulating DEC's TU45 unit. **System Industries,** PO Box 9025, Sunnyvale, CA 94086.

Circle 219 on Inquiry Card

THERMAL PRINTER UNIVERSAL INTERFACE

The UTI-80 microcomputer based board, measuring 4.75 x 5.5″ (12.06 x 13.9 cm), drives TI's 12- and 20-col thermal printer assemblies. The interface includes DIP switch selectable parallel (Centronics std) or serial (RS-232 or 20- and 60-mA current loop) inputs. Switch selectable invert print mode and baud rates are 110, 300, or 1200. Built-in self-diagnostic continuously prints the 64-char ASCII set to check the interface, power supply, and printer. **Technology Marketing Associates, Inc,** 6559 E Parker Rd, Parker, CO 80134.



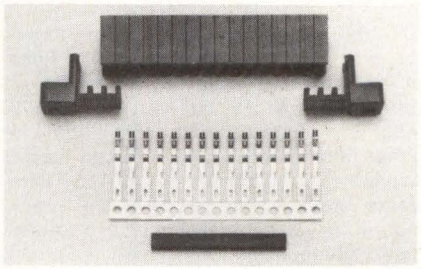
Circle 220 on Inquiry Card

10- AND 100-kHz F-V CONVERTER

Guaranteed specs over the −55 to 125 °C temp range include a nonlinearity of ±0.005% and full-scale tempco of ±50 ppm/°C for 2 hybrid frequency-voltage converters. Models 4732 and 4734 have a guaranteed dynamic range of 10 Hz to 11 kHz and 100 Hz to 110 kHz, respectively. They are MIL-STD-883 processed to include burn-in and temp cycling. Magnitude of the output voltage is linearly proportional to the input frequency, regardless of waveshape. **Teledyne Philbrick,** Allied Dr at 128, Dedham, MA 02062.

Circle 221 on Inquiry Card

PC BOARD EDGE CONNECTORS



Modular card edge connector series ESC-100A with 0.100″ (2.54-mm) centers and ESC-156A with 0.156″ (3.962-mm) centers are available with 2 through 85 and 2 through 50 contacts, respectively. The devices eliminate the need for engineers to design boards around available connectors as well as the extra tooling charges incurred for special connectors, or the need to purchase excess contact positions. **Electro-Sonic Components, Inc,** 14115 Chadron Ave, Hawthorne, CA 90250.

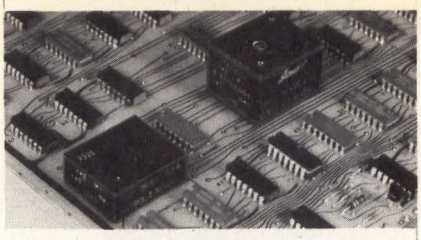
Circle 222 on Inquiry Card

DATA COMMUNICATIONS MESSAGE SWITCH

MS400 for both message and transaction processing environments combines architecture and hardware redundancy. Configurations for a single switch range from 2 to 16 processors. Capabilities can be changed or added by including software processes to support the functions; each terminal type and switching function is supported by a process that executes under the switch operating system. Each pair of processors provides up to 4800M bytes of mass storage and 2M bytes of memory. **Computer Sciences Corp,** 650 N Sepulveda Blvd, El Segundo, CA 90245.

Circle 223 on Inquiry Card

DC-DC SOLID STATE RELAY



Relays that operate over a load range of 3 to 50 Vdc switch a dc load with a dc input. Two package sizes with load current maximums of 400 mA and 2 A are offered. Inputs are logic compatible and sensitive to 3 to 24 Vdc with low drive currents. Optical isolation provides max protection for driving logic circuitry, while a clamped output provides max transient protection for the relay. Micro Cube and Mini Cube packages house the devices. **Grayhill, Inc,** 561 Hillgrove Ave, La Grange, IL 60525.

Circle 233 on Inquiry Card

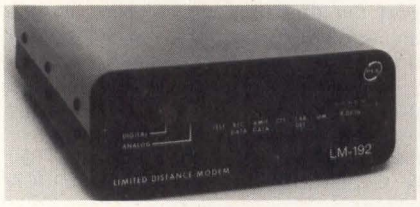
COLOR CRT MONITORS

IDT-19A, a 19″ (48-cm) color monitor, displays 200 to 300 horizontal lines of 450 to 640 dots at a nonflicker refresh rate of 60 Hz with an RS-170 input. It operates with this input in either interlaced or noninterlaced mode. Available configurations are a wire frame module, a 19″ (48-cm) rack mount, or a cabinet enclosure. Automatic degaussing and high contrast filter are featured. Electronic controls are on a display control panel normally mounted in a drawer assembly with front access. **Industrial Data Terminals Corp,** 1550 W Henderson Rd, Columbus, OH 43220.

Circle 234 on Inquiry Card

LIMITED DISTANCE MODEM

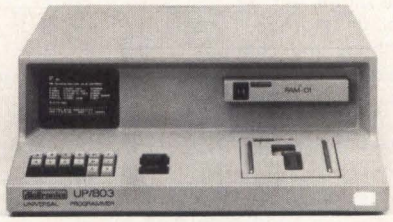
Designed for distances under 30 mi (48 km) over private lines or local telephone circuits at std synchronous speeds up to 19.2k bits/s, LM192 with built-in distortion analyzer operates in point to point, multipoint, or multidrop environments. A front panel LED bar graph display indicates receive line distortion in 5% increments from 0 to 50%. Equalization to optimize transmission distance is achieved by tuning for min distortion without external test equipment. **Data-Control Systems, div of General Indicator Corp,** PO Box 860, Danbury, CT 06810.



Circle 235 on Inquiry Card

MICROPROCESSOR CONTROLLED PROGRAMMER

Universal UP-803 reads, programs, and verifies all programmable devices. Each family of devices is handled by a single FAM (family module); every module can handle several algorithms which are software selected by a personality switch. Configurations and pinout are selected by a device adapter. Interactive operation is through a hexadecimal keyboard and 5″ (13-cm) CRT display. EIA RS-232-C and 20-mA current loop interfaces are included. The programmer handles devices over 24 address and 16 data lines. Buffer memory consists of 32k bits (up to 256k bits optional). An optional gang module can handle up to 16 devices simultaneously. **Digitronics Israel Ltd,** 3, Tevuot Haaretz St, Tel-Aviv, POB 39821, Israel.



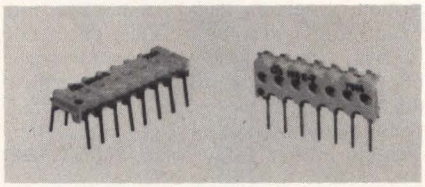
Circle 236 on Inquiry Card

DUAL-COLOR LED PACKAGES

Two bicolor matched LED chips in a T-1¾ short dome package size are available in red/red, green/red, green/green, green/international orange, green/yellow, international orange/international orange, and yellow/yellow chip color combinations. The package includes an uncolored diffused epoxy encapsulated, low profile lens for applications requiring a max OFF axis viewing angle. The lens exhibits a typ luminous intensity of 2.0 mcd at 20 mA. **OPCOA, div of IDS, Inc,** 330 Talmadge Rd, Edison, NJ 08817.

Circle 237 on Inquiry Card

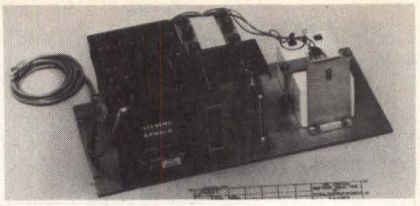
PROGRAMMABLE DIP/SIP SHUNT NETWORKS



As an alternative to individual jumper or bus wiring, both DIP and SIP style series 198 networks feature 0.100″ (0.254-cm) centers. SIP styles are available in 2 through 12 pins, DIPs in 4 through 24 pins. The interconnection package is factory preprogrammed or can easily be programmed with a hand tool before or after insertion into the PC board. Programming condition can be visually verified. **CTS Keene, Inc,** 3230 Riverside Ave, Paso Robles, CA 93446.

Circle 238 on Inquiry Card

MEMORY/LOGIC UPS



Self-contained UPS-2708B is an online system that provides regulated dc computer power for volatile MOS memory and refresh logic during an ac power outage, by establishing a battery backup dc power bus that is electrically independent of the main dc power bus. It also provides power in systems that have a separate dc power-off switch for overnight or standby system shutdown. A sealed, rechargeable 12-V battery is included. The float type battery charger has an 800-cycle battery life. **Stevens-Arnold, Inc,** 7 Elkins St, South Boston, MA 02127.

Circle 239 on Inquiry Card

SILVER EPOXY PAINT FOR RFI/EMI SHIELDING

C-608 conductive silver epoxy resin polyamide paint system with a volume resistivity of 0.01+ Ω/cm^3 in a uniform, 1-mil (0.025-mm) thick film offers rfi/emi shielding and static protection for electronics systems. Paint sprayers or brushes may be used to apply the formulation that resists settling and needs minimal agitation. Cured by air drying, the paint has a 1-h tack-free time and a 12-h pot life at 70 °F (21 °C). **Carroll Coatings, Div of Spectrum Coating Laboratories, Inc,** 217 Chapman St, Providence, RI 02905.

Circle 240 on Inquiry Card

16-CHANNEL ANALOG SIGNAL MULTIPLEXER

Programmable for random or sequential channel selection, this multiplexer functions with any data acquisition system or DMM. Features are 5-μV noise, up to 16 2-wire data channels or 8 4-wire channels, and a guard connection. Series On resistance is 0.5 Ω/wire and isolation is $>10^{9}$ Ω between channels. Max voltage on any given channel may be up to $\pm$300 Vdc or peak ac; model 3420 can handle currents up to 100 mA. Operating modes are manual, scan, remote, and slave. **Data Precision Corp, Div of Analogic Corp,** Electronics Ave, Danvers, MA 01923.

Circle 241 on Inquiry Card

ASCII/EBCDIC CLOCK/CALENDAR

Dataclock 100 communicates the date and time to all computers that support serial asynchronous communications. Installed transparently on the cable that runs from an ASCII or EBCDIC terminal to a computer system, the device can set the computer's realtime clock as part of the computer's power-up sequence. Software support can be written in such high level languages as FORTRAN, COBOL, BASIC, or Pascal. **Qupro Data Systems Ltd,** Suite 200, 501 Krug St, Kitchener, Ontario N2B 1L3, Canada.
Circle 242 on Inquiry Card

DISC PACK SUBSYSTEM FOR PDP-11/70

PM-DSW11/300 emulates the DEC RH70 for the PDP-11/70, and replaces RWP04, RWP05, and RWP06 disc subsystems. The controller replaces up to 8 DEC control logics and supports up to eight 254M-byte drives, for a max capacity of 2G bytes. Each disc pack has a formatted capacity of 253.6M bytes, and removable packs provide unlimited offline storage. The system includes error detection and correction. **Plessey Peripheral Systems,** 17466 Daimler, Irvine, CA 92714.
Circle 243 on Inquiry Card

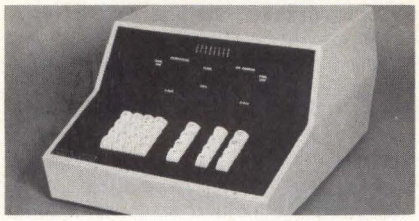
LOW PROFILE T-1¾ SHORT-LENS LEDS

Featuring 5.33-mm long encapsulations, the X-90B series subminiature tapered LEDs are designed for high efficiency, low current operation. Light-color outputs of red, green, yellow, and orange are available in 4 models each, offering variable luminous intensities ranging up to 12 mcd at 10 mA in clear orange, and total half-intensity viewing angles up to 80° in diffuse-lens styles. The light source offers guaranteed min luminous intensity, which is variable upon light-color output and lens diffusion. Max ratings of continuous forward current are 100 mA for red and 35 mA for green, yellow, and orange. Power dissipation for red is 180 mW and 105 mW for green, yellow, and orange. Storage and operating temps range from −55 to 100 °C. Silver plated leads eliminate most common solderability problems; the cathode lead is 25.40 mm long and the anode lead is 26.67 mm long. The low profile, high output, solid state lamp is suited to instrument control panels. Electrical characteristics include a response time of 50 ns. **Chicago Miniature Lamp Works, General Instrument Corp,** 4433 N Ravenswood Ave, Chicago, IL 60640.
Circle 244 on Inquiry Card

SOLDER PIN INDICATOR LIGHTS

C-series incandescent (CE and CJ), LED (CW and CY), and neon (CS and CT) lamps are equipped with 0.040″ ±0.001″ (1.016 ±0.025-mm) dia brass tin plated terminals with 0.401″ (10.185-mm) straight or 0.318″ (8.077-mm) right angle pins. Indicators fit into 0.290″ (7.366-mm) dia holes. Housings are made of anodized aluminum with high dielectric molded nylon headers. Reliability ranges from 1k to 60k hours depending on type and voltage. **Genisco Technology Corp, Eldema Div,** 18435 Susana Rd, Compton, CA 90221.
Circle 245 on Inquiry Card

MICROPROGRAM DEVELOPMENT SYSTEM



For high speed emulation of P/ROMs, the DS50 can be configured with RAMs of various sizes. Microprogram debugging capabilities such as break and trace are options. The unit may be loaded and edited via keyboard or RS-232 interface. Cassette drive for load, dump, and verify is optional. Control memory size varies from 1k x 16 to 4k x 64. Currently available RAM speeds range from 20 to 150 ns, with total unit access time down to 34 ns. **Hilevel Technology, Inc,** 14661 Myford Rd, Tustin, CA 92680.

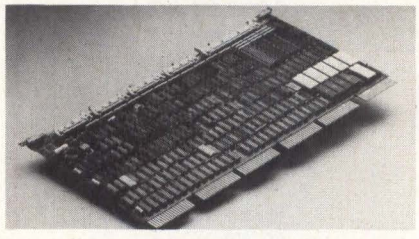
Circle 246 on Inquiry Card

FIBER OPTIC DATA LINK

Both receiver and transmitter of OTD-500 data system are packaged in a 0.5" (1.3-cm) high 24-pin DIP for board to board applications. Transmitter features a driver circuit with GaAs (infrared) LED emitter; the receiver features miniature hybrid construction. TTL compatible Op-Tec Link™ offers max noise immunity through adjustable control. A 5-ft (1.5-m) fiber optic cable is std. Operating voltage is 5 V typ. **Opto Technology, Inc,** 1674 S Wolf Rd, Wheeling, IL 60090.

Circle 247 on Inquiry Card

SINGLE-BOARD CONTROLLER FOR PDP-11/FOUR DISC DRIVES

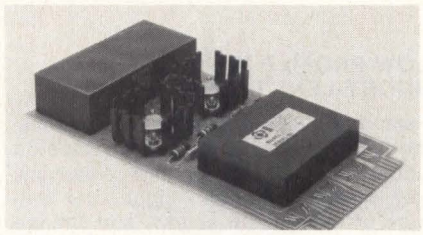


Emulating the DEC RM-02 controller, the 3211 controller provides compatible formats and interchangeable media without changes to the software disc driver of the host operating system. Up to 4 SMD type drives in any mix of capacities can be interfaced to a DEC PDP-11 series computer. The host resident controller handles data rates from 806k to 1.2M bytes/s. A 32-bit ECC, overlapping seeks, sector interleaving, and multiple sector transfers are featured. **Ball Computer Products,** 860 E Arques Ave, Sunnyvale, CA 94086.

Circle 248 on Inquiry Card

14-BIT D-S CONVERTER

Driving up to 3 size 11 torque receiver synchros with ±6-min accuracy, the 4.5 x 9.25 x 1" (11.4 x 23.5 x 3-cm), 400-Hz units accept a 14-bit natural binary angle and convert it into 3-wire synchro or 4-wire resolver signals. Output is short circuit protected and current limited. Loading of 5 VA is std. DSC40-PC-L-1 requires a 26-V reference, as well as ±15 V at 375 mA and 5 V at 50 mA. **Computer Conversions Corp,** 6 Dunton Ct, East Northport, NY 11731.



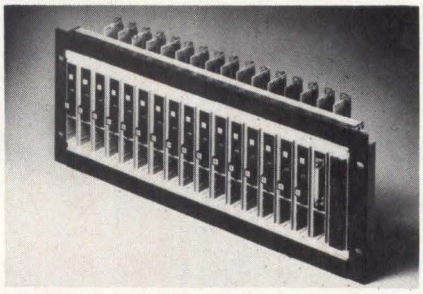
Circle 249 on Inquiry Card

RACK MOUNTABLE INSTRUMENT PRINTER

Model 5019 is a rack mounted OEM version of the 5020 printer. It offers 5 x 7 dot matrix printing of any character set programmed into the character generator P/ROM. Unit prints 32 char/line at up to 2 lines/s. Printing mechanism life time is more than 2 x 10^6 lines; printhead life is more than 7 x 10^5. Input may be ASCII or BCD. The 5.22 x 8.39" (13.25 x 21.31 cm) printer fits into almost any instrument application. **Kontron Electronic Inc,** 700 S Claremont St, San Mateo, CA 94402.

Circle 250 on Inquiry Card

CHANNEL SWITCHING MODULES



A/B switches permit switching of the EIA RS-232/CCITT V.24 interface between a modem and 2 terminals (or computer ports). This passive, 1" (2.5-cm) wide modular device has 3 std EIA rear card-edge connectors—1 for the modem and 2 for terminals; 2 color-coded A/B pushbuttons implement the mechanical switching action. Visible several feet away, a color-coded indicator shows the status of the channel switch. **Dynatech Data Systems,** 7644 Dynatech Ct, Springfield, VA 22153.

Circle 251 on Inquiry Card

8.5" RECEIVE ONLY SERIAL PRINTER

Model 877 is a bidirectional 9 x 7 dot matrix printer that features a heavy gauge, hardened metal chassis and stainless steel drive screw and utilizes a cartridge ribbon to eliminate ribbon reversing mechanisms as well as to assure print quality. The unit prints 120 char/s at 80 char/line, 10 char/in (3.9/cm) using the ASCII 95-char set. Internally contained 8.5" (21.6-cm) paper roll is friction fed. **Printer Terminal Communications Corp,** 124 Tenth St, Ramona, CA 92065.

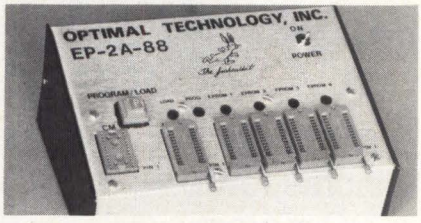
Circle 252 on Inquiry Card

MINIATURE DC-DC POWER CONVERTERS

DCE series of 8 models offers accurate 0.02% max error regulated outputs with low noise, 1 mV rms. High attenuation input filter reduces kickback spikes, noise, and reflected ripple caused by inverter switching. I/O isolation impedance of 10^9 Ω and voltage isolation of 300 Vdc permit separation of the output circuit from the dc bus. Inputs of 5, 12, 15, 24, and 28 Vdc convert to outputs of ±15 and ±12 Vdc at 150-mA output current. **Intronics,** 57 Chapel St, Newton, MA 02158.

Circle 253 on Inquiry Card

EPROM COPIER

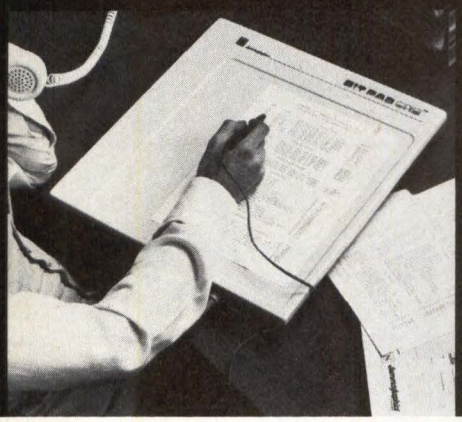


A standalone EPROM programmer copies from 1 to 4 1k, 2k, and 4k EPROMs. Model EP-2A-88 offers copy modules for duplicating 2758, 2732, TMS 2508, TMS 2516, 2716, and 2732 EPROMs. A single pushbutton control initiates the complete programming cycle, ensuring that each EPROM is erased, programmed, and verified. Status of the LED indicators is on when the programming is completed, flashing if the EPROM was not erased, and off if the EPROM was erased but did not program. **Optimal Technology, Inc,** Blue Wood 127, Earlysville, VA 22936.

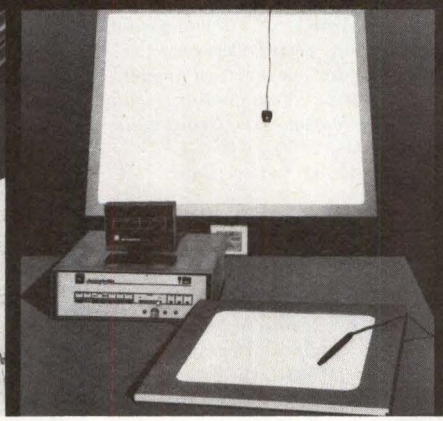
Circle 254 on Inquiry Card

from Apple® to Zeta

When it comes to computer graphics, it all starts with Summagraphics.



Bit-Pad One



Intelligent Digitizer

Datagrid II, System 4

Beginning with the digitizer, of which it is the world's largest and most experienced manufacturer, Summagraphics has developed a complete range of graphic systems for both the OEM and end user.

From the simplest data input digitizer to complete stand-alone computer-aided drafting systems, each is designed to provide flexibility to meet your future needs, and each is very competitively priced.

Digitizers for data input. Summagraphics offers a complete family of digitizers for converting graphic information into digital form for processing and for speeding the entry of alphanumeric and programming information by eliminating keyboarding.

- Bit-Pad One provides an 11-inch by 11-inch tablet and resolution to .004 inch with a choice of RS-232, IEEE-488 or parallel-byte output.
- ID series data tablets provide similar resolution in tablets ranging in size up to 42 by 60 inches.
- Summagrid provides .001-inch resolution in back-lighted tablets as large as 42 by 60 inches.

®Register mark of Apple Computer Inc.

Intelligent digitizers incorporate microprocessors to automatically perform such functions as calculating areas, linear displacements and perimeters and for relocating origins, converting binary to BCD and formatting output data.

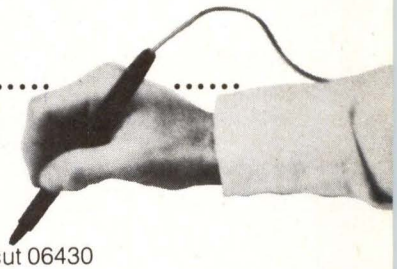
Preprocessing systems for remote job entry. Datagrid II, Systems 1 and 2, are designed for off-line digitizing and storage for subsequent entry into any graphic system or data base.

Preprocessing reduces communications and host processor loads.

Stand-alone computer-aided drafting systems. Datagrid II, Systems 3 and 4, are complete systems that provide computer processed solutions to a variety of drafting applications.

GET THE FULL STORY FREE!

Use the coupon below to get complete information on the systems that seem to fill your needs.



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☐ My needs are immediate, please have a representative call.
My phone number is ( ) _____
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☐ Stand-alone graphics systems

Name: _____
Department _____ Title _____
Company _____
Address _____
City _____ State _____ Zip _____

CIRCLE 174 ON INQUIRY CARD

LITERATURE

Power Supplies

Selection guide lists electrical and mechanical specs, and includes outline drawings and photos for PC board and chassis mounting miniaturized power modules, and for plug-in, programmable, and unregulated power supplies. **Acopian Corp,** Easton, Pa.
Circle 300 on Inquiry Card

Modular Power Supplies

Catalog features dc-dc converters, switching supplies, and a 4-output microprocessor unit; included are specs, pin configurations, and dimensional drawings for each. **Calex Manufacturing Co, Inc,** Pleasant Hill, Calif.
Circle 301 on Inquiry Card

Capacitors, Filters, and Relays

Dimensional drawings, photos, specs, and tables provided in catalog supply details on aluminum electrolytic, ac, film-metallized, mica dielectric, and disc ceramic capacitors; emi filters; relays; and decade counters. **Cornell-Dublier,** Newark, NJ.
Circle 302 on Inquiry Card

Dual Monolithic Transistors

Specs, pad designations, and performance and key parameters for matched pair transistors are outlined in catalog. **Micro Power Systems, Inc,** Santa Clara, Calif.
Circle 303 on Inquiry Card

EIA Cables

Color coded diagrams in catalog aid in selection of correct Clear Signal™ cable; also listed are transfer switches, gender changers, cable bridges, and junction panels. **Inmac,** Santa Clara, Calif.
Circle 304 on Inquiry Card

Bubble Memories

The concept of bubble memories, comparison with other memory devices, an examination of the 7110 and the 1M-bit bubble memories, and support electronics are presented in application note available from **Intel Corp,** 3065 Bowers Ave, Santa Clara, CA 95051.

Medium and High Speed Line Printers

Product slide rule presents condensed specs for band, chain, train, and drum printers. Copies are available by letterhead request to **Digital Associates Corp,** 1039 E Main St, Stamford, CT 06902.

Universal P/ROM Programmer

Brochure lists specs, standard and optional features, and P/ROM comparison chart for universal P/ROM programmer; also described are paper tape reader, ROM emulator, gang programming module, and UV EPROM eraser. **Digitronics Israel Ltd,** Tel Aviv, Israel.
Circle 305 on Inquiry Card

Ceramic Magnets

Booklet explains ceramic magnet processes, includes table of properties, details approach to loud speaker magnet manufacturing, and describes capabilities of ceramic block and motor arc magnets. **General Magnetic Co,** Dallas, Tex.
Circle 306 on Inquiry Card

Programmable Motion Control

Brochure describes advantages and application possibilities of programmable products that can control motion in industrial processes; included are stepping motor control module, and absolute encoder input module. **Gould Inc, Modicon Div,** Andover, Mass.
Circle 307 on Inquiry Card

Noise Control Materials

Descriptions and photos are listed in bulletin for absorption, barrier, and damping types of materials. **The Soundcoat Co,** Brooklyn, NY.
Circle 308 on Inquiry Card

Propeller and Tubeaxial Fans

Illustrated catalog supplies specs, dimensional drawings, and performance charts for 60-Hz, 400-Hz, multi-Hz, and dc-type Boxer and slim profile fans. **IMC Magnetics Corp,** Westbury, NY.
Circle 309 on Inquiry Card

Monolithic and Hybrid Data Converters

Handbook contains information on A-D and D-A converters, data acquisition systems, computer analog I/O peripherals, sample-holds, analog multiplexers, and op amps and includes data sheets for key products. **Datel-Intersil,** Mansfield, Mass.
Circle 310 on Inquiry Card

Positioning and Tracking Controls

Joysticks, trackballs, control grips, and interface electronics circuits are illustrated and described in catalog. **Measurement Systems, Inc,** Norwalk, Conn.
Circle 311 on Inquiry Card

Video Display Terminals And Printers

Brochure highlights Dumb-Terminal® console, smart editing terminal, semi-intelligent terminal, and Ballistic printer. **Lear Siegler, Data Products Div,** Anaheim, Calif.
Circle 312 on Inquiry Card

Telecommunications and Voice Readout Systems

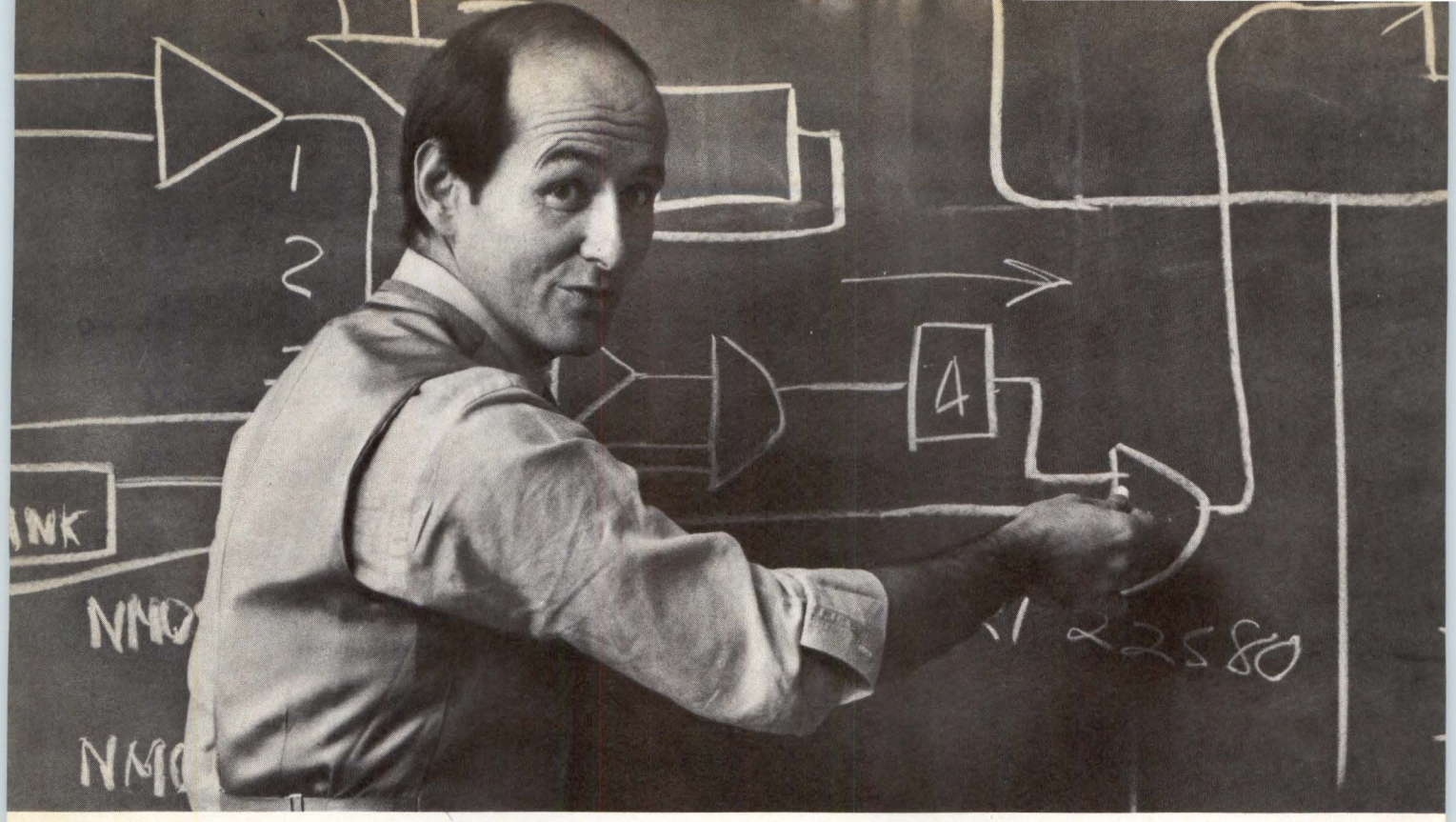
Design and operational specs for programmable voice readout system, voice response system, and automatic number announcer are among those supplied in catalog. **Master Specialities Co,** Costa Mesa, Calif.
Circle 313 on Inquiry Card

Logic Analysis Techniques

Ten applications illustrate the use of logic analyzers with system crashes, complex program tracing, asynchronous buses, and turn-on failures. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 314 on Inquiry Card

Components

Electrical characteristics and packaging specs for industrial linear ICs, vacuum fluorescent indicator panels, tantalum capacitors, and discrete semiconductors are furnished in catalog. **NEC Electron, Inc,** Santa Clara, Calif.
Circle 315 on Inquiry Card



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CIRCLE 175 ON INQUIRY CARD

LITERATURE

Stepper Motors

Technical guide explains technology, offers applications notes and formulas, and provides torque vs step rate graphs, wiring diagrams, and dimensional drawings for 12 series of motors. **Airpax/North American Philips Controls Corp,** Cheshire, Conn.
Circle 316 on Inquiry Card

Wirewrapping and Electronics

Catalog includes wirewrapping and electronic assembly tools and parts for both industrial and hobby users. **OK Machine and Tool Corp,** Bronx, NY.
Circle 317 on Inquiry Card

Wiring Accessories

Bulletin includes material specs, product descriptions, dimensional drawings, and packaging information for mounting accessories, harness board accessories, and cable tie installation tools. **Panduit Corp,** Tinley Park, Ill.
Circle 318 on Inquiry Card

Computer Aided Design And Manufacturing

Brochure describes the capabilities of the interactive design, drafting, and manufacturing computer aided graphics system which features finite element analysis, hidden line removal, and drawing layout capabilities. **Calma,** Sunnyvale, Calif.
Circle 319 on Inquiry Card

Uninterruptible Power Systems

Bulletin describes rectifier/charger, inverter, and static switch subassemblies of PWM UPS and details performance during normal operation, ac line failure, and after ac line restoration. **Cyberex, Inc,** Mentor, Ohio.
Circle 320 on Inquiry Card

Wire and Cable

Specs, illustrations, and applications information on line of wire and cable, insulation, cordsets, and electronic accessory products are furnished in catalog. **Dearborn Wire and Cable Co,** Rosemont, Ill.
Circle 321 on Inquiry Card

Magnetic Bubble Memory Devices

Illustrated sections of primer explain the principles of the magnetic bubble memory; also detailed are loop organizations and necessary peripheral circuitry. **Fujitsu America, Inc,** Lake Bluff, Ill.
Circle 322 on Inquiry Card

Information Systems Seminars

Course objectives, course outline, and instructor biography are given in catalog which supplies seminar schedule and enrollment information. **Datapro Research Corp,** Delran, NJ.
Circle 323 on Inquiry Card

Data Monitor

Data sheet illustrates 802A that monitors and stores data for lines up to 56k bits/s and describes operation, special features, and preliminary specs. **Halcyon,** San Jose, Calif.
Circle 324 on Inquiry Card

Lighted Pushbutton Switches

Dimensional drawings, mounting diagrams, switch actuation, bezel styles, lenses, and color options for instrument grade, heavy duty, and oil and watertight switches are given in catalog. **EAO Switch Corp,** Milford, Conn.
Circle 325 on Inquiry Card

Automatic Test Equipment

Test equipment ranging from benchtop manual units to microprocessor based units capable of testing up to 16k points at the rate of 1k points/s are described, and their operating modes listed in brochure. **Muirhead Addison,** Mountainside, NJ.
Circle 326 on Inquiry Card

Power Line Disturbance Analyzer

Brochure supplies specs and a typical printout for series 606 ac power line analyzer that prints data on impulse, sag, surge, and slow average voltages. **Dranetz Engineering Laboratories,** South Plainfield, NJ.
Circle 327 on Inquiry Card

Thick Film Thermal Printheads

Application report illustrates how printing rate can be maximized by using external means to compensate for the inherent physical properties of the printing element. **Gulton Industries, Inc,** Metuchen, NJ.
Circle 328 on Inquiry Card

Humidifiers

Survey sheet discusses how proper humidification during heating season can reduce static electricity and contribute to increased efficiency of desktop minicomputers. **Research Products Corp,** Madison, Wis.
Circle 329 on Inquiry Card

Communications Test Set

Brochure compares specs of the PTS-107 digital transmission test set for digital communications system testing and the HP 3780A test set. **Tau-Tron Inc,** Chelmsford, Mass.
Circle 330 on Inquiry Card

Data Communication Products

Catalog features the Hawk 4000 series Datatraps that provide a CRT display of online data communications; also described are Range Rider data test sets, and cables. **International Data Sciences, Inc,** Lincoln, RI.
Circle 331 on Inquiry Card

Miniature and Subminiature Switches

Included in catalog are dimensional drawings, electrical specs, plus descriptions of miniature and subminiature toggle, pushbutton, rocker, slide, rotary, push, and precision switches. **Impact Electrical Products, Inc,** Beaverton, Ore.
Circle 332 on Inquiry Card

LCD Circuits

Wall chart features range of LCD watch and clock circuits for radios, alarms, and automobiles, outlining each circuit with simulated displays and list of functions. **Oki Semiconductor,** Santa Clara, Calif.
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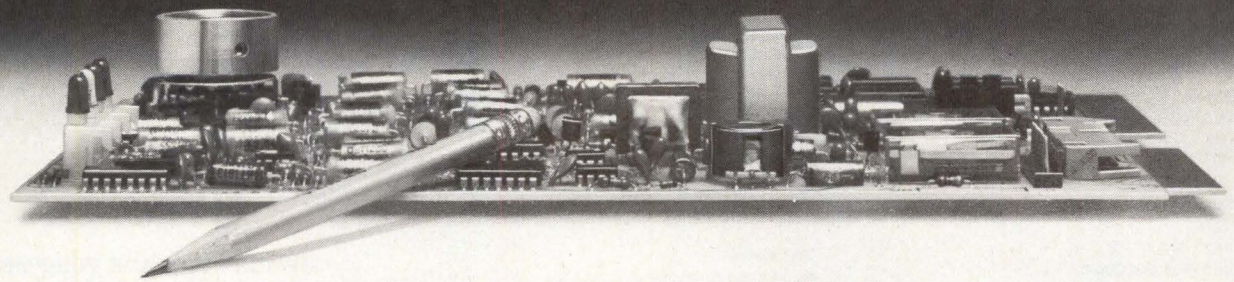

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CIRCLE 176 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

Note: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

MATERIALS AND FORMS PAGE

INSULATION

OPTICAL MATERIALS AND FORMS

HARDWARE

CABINETS AND ENCLOSURES

CONNECTORS AND INTERCONNECTION SYSTEMS

FANS AND BLOWERS

INDICATORS; READOUTS; DIGITAL DISPLAYS; LAMPS

PACKAGING

PARTS

PROGRAMMING BOARDS AND MODULES

SHIELDING

WIRE AND CABLE (See also Connectors)

WIRING PINS AND TERMINALS

COMPONENTS AND ASSEMBLIES PAGE

DELAY LINES

ELECTRON TUBES; CRTs

MOTORS; ROTATIVE COMPONENTS

PHOTODEVICES; PHOTODEVICE ASSEMBLIES

POWER SOURCES, REGULATORS, AND PROTECTORS

RELAYS

RESISTIVE COMPONENTS

SWITCHES

CIRCUITS PAGE

DIGITAL AND INTERFACE INTEGRATED CIRCUITS

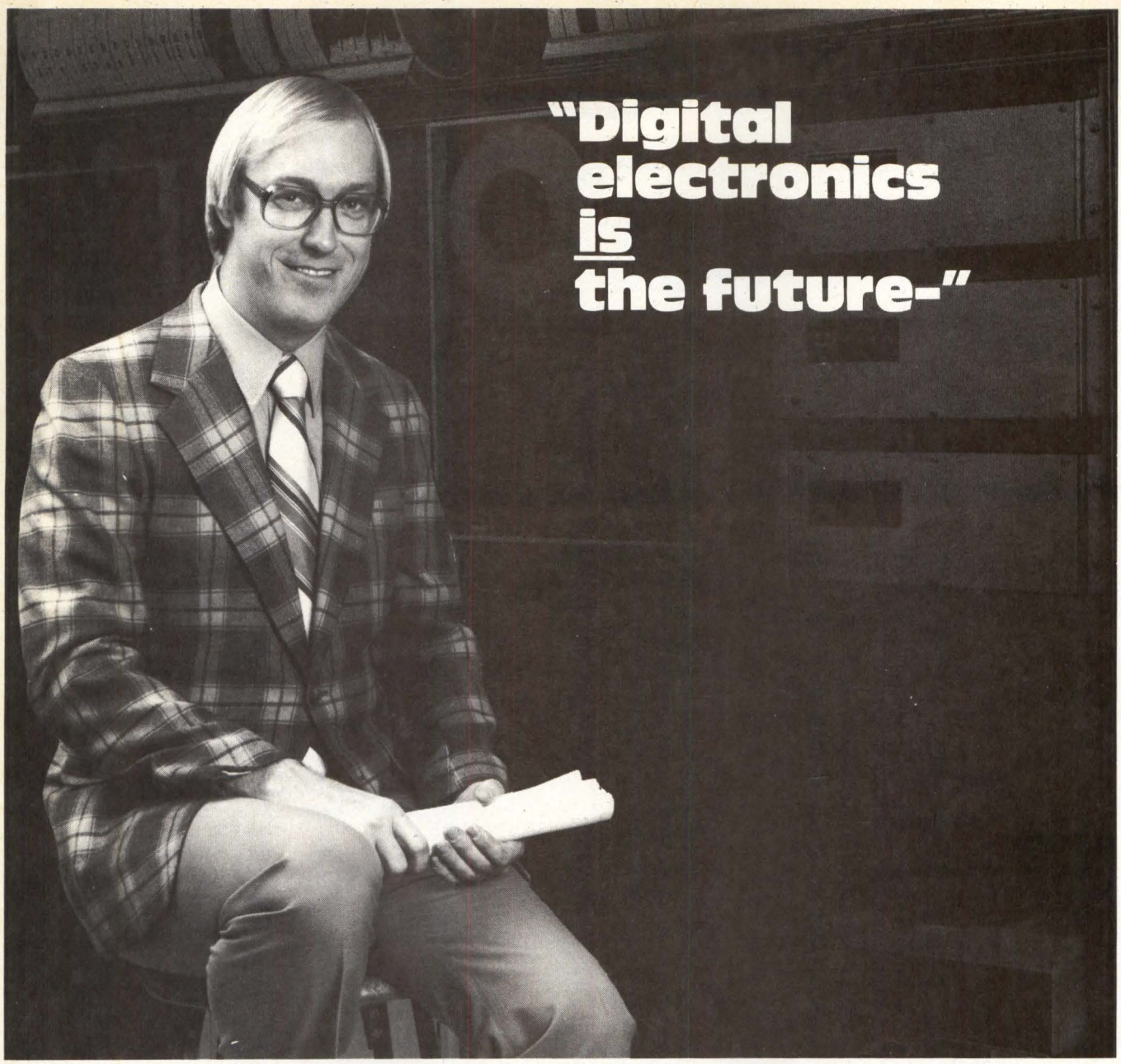
(See also Semiconductor Memories under Memory/ Storage Equipment)

DRIVERS AND DECODERS

LINEAR INTEGRATED CIRCUITS

MEMORY/STORAGE EQUIPMENT

BUBBLE MEMORIES



Harvey Schmidt, Group Engineer Test Equipment Design, BSEE, University of Wisconsin, 1968; MBA, Northern Illinois University, 1975 (through Sundstrand program)

"Working in the test equipment area of Sundstrand's aviation product lines requires not only a thorough understanding of the products, but the creativity to develop ways to test them. Sometimes, that can be more complex than the product itself!

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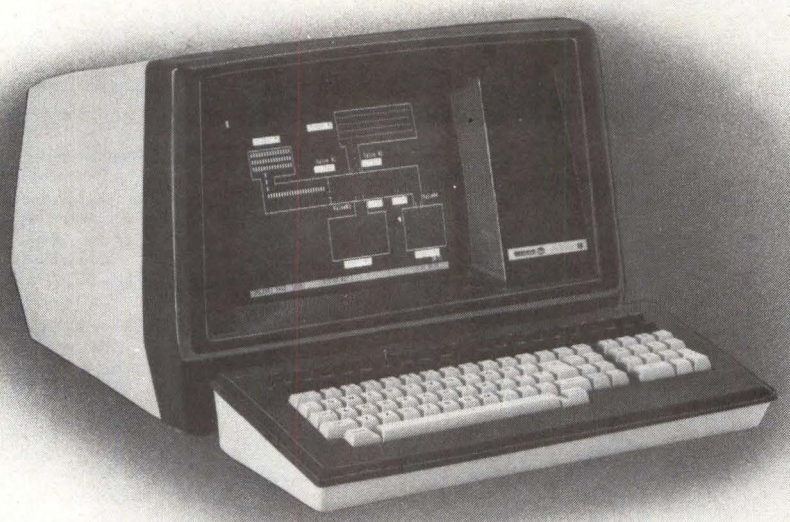
CIRCLE 177 ON INQUIRY CARD

GUIDE TO PRODUCT INFORMATION

BEEHIVE'S terminal family is designed for OEM planning



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GUIDE TO PRODUCT INFORMATION

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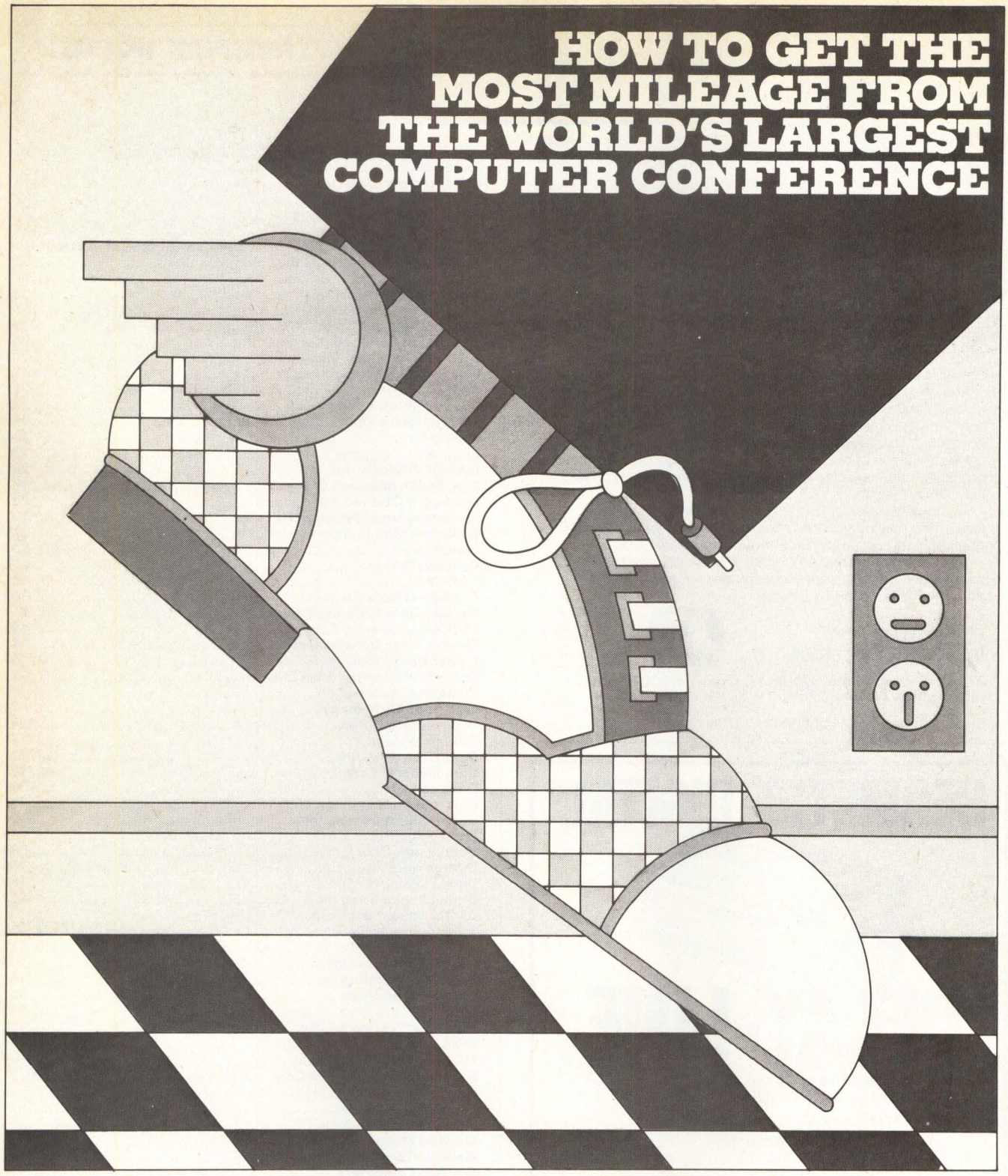

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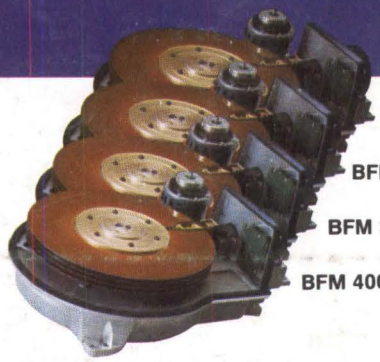

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