A PENNWELL PUBLICATION

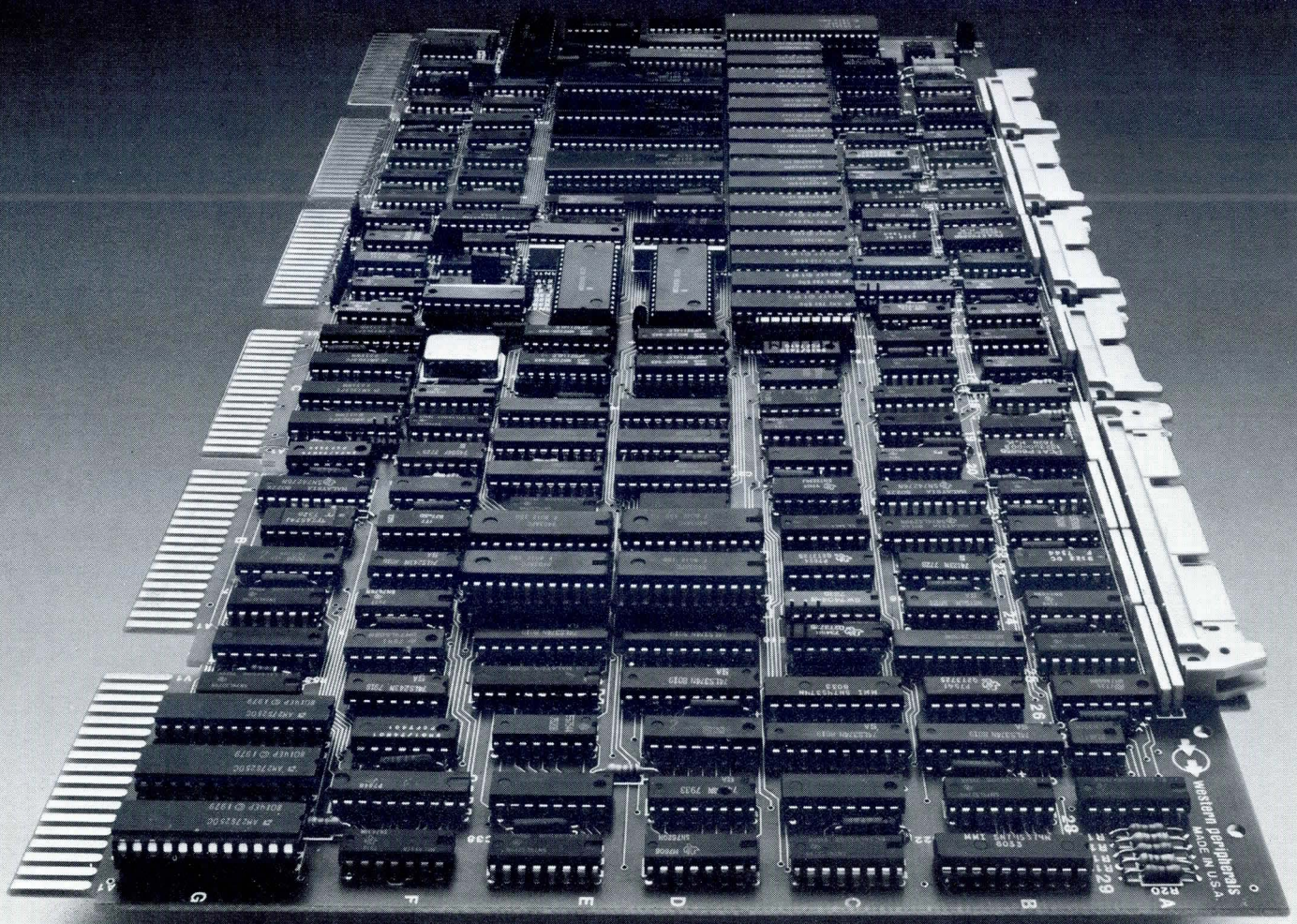
COMPUTER DESIGN

THE MAGAZINE OF COMPUTER BASED **SYSTEMS**

DECEMBER 1980

SEMICUSTOM TECHNOLOGY DRIVES MINICOMPUTER ARCHITECTURE
PRINTED CIRCUIT BOARD LAYOUTS FOR A COMPATIBLE DYNAMIC RAM FAMILY
BUS ADAPTER SIMPLIFIES INTERPROCESSOR COMMUNICATION

Introducing the DC-231 universal single board SMD disc controller.



■ Emulates DEC's controller precisely.
■ Accommodates four large capacity media multiplatter disc drives—50 to 300 megabytes each.
■ The DC-231 is a distributed processing system in miniature.
■ Fully software compatible with DEC RH-11/RM02 systems running standard functional diagnostics, RSX-11M and RSTS.
■ Comprehensive diagnostic programs.
■ 1-year warranty.
■ 30-day delivery.

Western Peripherals is the leading independent controller manufacturer.

We're known throughout the industry for quality and reliability.

Our nationwide service and worldwide distributor service network provide support wherever you are.

For complete information on the DC-231 and our entire line of controllers, call or write Western Peripherals, 14321 Myford Road, Tustin, California 92690. (714) 730-6250. TWX:910 595-1775 CABLE: WESPER.

western peripherals
Division of WESPERCORP

Number 1 in controllers.

CIRCLE 1 ON INQUIRY CARD

A Marriage of Convenience— for PDP and LSI users!

It's a marriage made in heaven—for DEC PDP-11 and LSI-11 owners who would like a low-cost, quick-to-install, high-density data storage system.
The union consists of Kennedys' Series 5300 fixed media, Winchester technology disk drives and Kennedy emulation controllers. The controllers; which use standard DEC PDP-11 operating systems and diagnostic software, are embedded inside the computer, allowing the Series 5300 to be easily attached to both PDP-11 and LSI-11 minis! In one sweet, short ceremony, Series 5300, with its' one, two or three platter versions and unformatted data capacity of 70M bytes and track density of 300 TPI can be joined with the KSC11 unibus disk controller for the PDP-11; and the KSCO1, for use with the LSI-11; And no software changes or other alterations are required.
Kennedy Series 5300, controllers and your PDP-11 or LSI-11—put them together, plug them in and you have a winning system.

KENNEDY
Subsidiary, Magnetics & Electronics Inc.
1600 Shamrock Ave., Monrovia, CA. 91016
(213) 357-8831 TWX 910-585-3249

CIRCLE 2 ON INQUIRY CARD

KENNEDY • QUALITY • COUNT ON IT

Cromemco accepts your challenge, Data General

Yes, Data General, we saw your ad.

So we realize you hope to win over some of our computer business.

And we can see you have reason to be pleased about your line of minicomputers. They *are* MINIs though.

But Cromemco produces state-of-the-art MICROcomputers.

Powerful ones.

And our micros have some outstanding advantages.

For example, ***Cromemco is the only microcomputer manufacturer to support a broad range of microcomputers with (a) 5-inch double-sided, double-density floppy disk drives and with (b) 8-inch double-sided, double-density floppy disk drives AS WELL AS (c) 8-inch Winchester hard disk drives.***

That means, of course, that our customers have a wide choice of disk storage capability.

UNEQUALLED SOFTWARE SUPPORT

OK. That was one point.

Here's another: our stunning selection of software support. ***Cromemco is the only micro manufacturer to produce both single-user and multi-user multi-tasking computers with software like this:***

SYSTEM SOFTWARE

- CDOS (a CP/M-like operating system)
- CROMIX (a UNIX-like operating system)
- RPG-II (IBM-compatible)
- COBOL
- BASIC
- FORTRAN IV
- RATFOR
- LISP
- C
- Macro Assembler

APPLICATION SOFTWARE

- Word Processing System
- Data-Base Management
- General Ledger
- Accounts Receivable
- Accounts Payable
- Inventory

All of this is available now with more coming all the time.

So there you are, D.G.

You can see why we know our microcomputers will stand the test.

Cromemco eagerly accepts the challenge.

Reproduced from the July 31, 1980 issue of *Electronics* magazine.

Cromemco logo on computer board shown in original ad

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Tomorrow's Computers Today
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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN® THE MAGAZINE OF COMPUTER BASED SYSTEMS

VOLUME 19, NUMBER 12 DECEMBER 1980

DEPARTMENTS

Cover by Darcy Gerbarg
Created at the Computer Graphics Research Laboratory of the New York Institute of Technology

Number of copies printed this issue—88,300.

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INCREDIBLE: EIGHT LSI-11 QUAD SLOTS AND TWO TU58s IN 7" ... PLUS FRONT LOADING

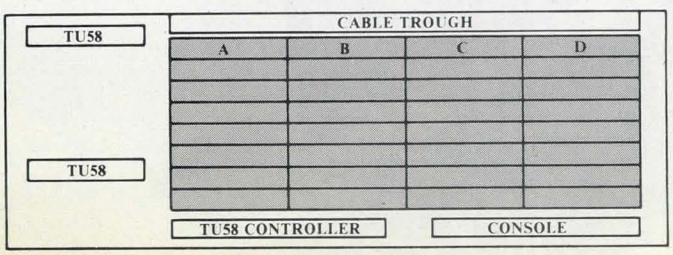
Another industry first from Dataram: The B04 chassis that lets you add TU58 capability to your LSI-11® configuration without buying two DEC® chassis (the 5¼" PDP®-11/03 and 5¼" TU58 subsystem). Now, with a single 7" B04 chassis, you can accomplish the same thing, saving space and money at the same time.

The B04 saves time and trouble, too, with its unique front-loading feature that gives you fast, easy access to the eight-quad-slot backplane through a simple snap-off front panel. And when you use DEC's LSI-11/23 along with Dataram's 256KB single-board DR-113S in the B04 chassis, there's still a lot of 5.0VDC power remaining — 20 amps — to configure the rest of your system.

There's also a lot of innovative thinking in our B04 chassis — practical engineering that makes the LSI-11 Bus available on the A and B, and C and D connectors; an Operator's Console Unit that doesn't take up a valuable backboard slot; and a trough that provides space for routing cables to the rear of the B04 chassis.

If you don't need TU58 capability, our B03 chassis provides these same features (less the TU58s) in a 5¼" alternative.

In addition to the B03 and B04 chassis, Dataram also provides LSI-11/2 and LSI-11/23 microcomputers; memory; cartridge disk, tape, and SMD controllers; and a wide range of accessories. Give us a call.



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DATARAM CORPORATION

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CIRCLE 5 ON INQUIRY CARD

What the world has been waiting for in high performance micros.

Immediate delivery.

Digital is changing the way you get your products to market.

We're making it faster.

Because right now our basic LSI-11 product family is available with off-the-shelf delivery. So you don't have to wait around to get your product started.

And once you have our micros, you can do more with them. Our unique building-block approach lets you design whatever system you need.

Start with your choice of microcomputer terminals. Either the VT103-AA—a specially configured VT100 with an LSI backplane that accepts up to 8 double-height modules. Or the VT103-BA, featuring a backplane and a TU58 dual-drive cartridge tape.

Then you add our KD11-HA LSI-11/2 CPU Board, a low-cost 16-bit processor with the power to drive virtually any small to medium-sized system.

Plus you can choose either one of these powerful modules.

1. The MXV11 LSI-11 Multifunction Module. Featuring 8 or 32Kb of RAM, up to 8Kb of PROM (user supplied), 2 asynchronous serial I/O ports and real-time clock.
2. The MSV11-DD 64Kb RAM Board. Complete with on-board refresh.

These boards, plus the VT103, are available immediately. To give you all the flexibility and performance you need to develop a great micro product. Or a great micro development system. Or both.

Of course, once you get started with an LSI-11, there's no telling where you might want to go. So we offer lots of other modules for you to plug into your VT103: 9 different memory boards, 11 I/O modules, 9 communications options, even kits for designing your own custom interfacing.

And if you need more, there are also 8 different peripherals, all running on Digital's industry-standard LSI-11 Bus, the most widely used bus structure in micros.

Great flexibility in software, too.

Our RT-11 development and applications software gives you a wealth of high level languages and development aids. Its capabilities range from multitasking, multi-terminal support for larger configurations, to a very small kernel for single-task applications. There's also SIMRT, a subset of RT-11 designed for PROM applications that's an integral part of FORTRAN IV.

And because your development software has the same RT-11 software as your target system, you can debug your programs with complete confidence.

The total approach to micros.

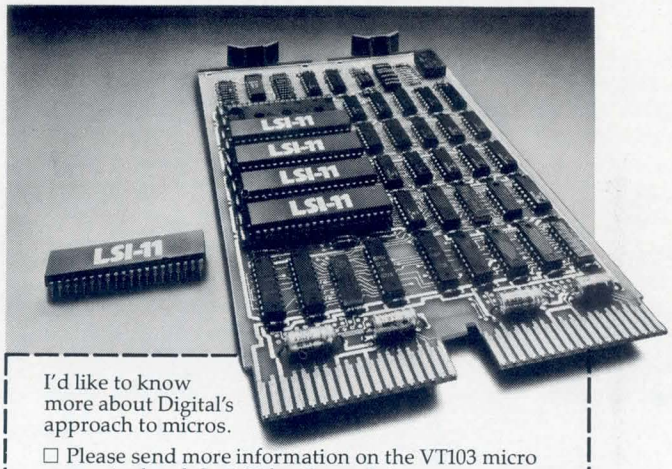
Helping you get your product to market quickly is just one of the ways we make micros easier to work with.

We also back all our boards with over 14,000 service people worldwide, technical consultation and training. Plus a range of support agreements to meet your needs.

It's the total approach to micros, only from Digital.

For more information call our toll-free LSI-11 Hotline at **800-225-9220.** (In MA, HI, AK and Canada, call 617-467-7000.) Or send the coupon.

Digital Equipment Corporation, MR2-2/M65, One Iron Way, Marlboro, MA 01752. In Europe: Digital Equipment Co. Limited, 2 Cheapside, Reading, RG1 7AA, England. In Canada: Digital Equipment of Canada, Ltd. Or contact your local Hamilton/Avnet distributor.



I'd like to know more about Digital's approach to micros.

☐ Please send more information on the VT103 micro terminal and the LSI family modules.
☐ Please have a Sales Representative call.

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Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Telephone _____

My application is _____

Send to: Digital Equipment Corporation, Microcomputer Products Group, MR2-2/M65, One Iron Way, Marlboro, MA 01752.

DEC-C-160

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digital

We change the way the world thinks.

CIRCLE 6 ON INQUIRY CARD

Compare our data and time domain logic analyzer with the industry's leading data-domain-only unit.

For complete analysis, the K100-D outperforms H-P's 1610B!

Before you settle for the Hewlett-Packard 1610B data domain analyzer, compare it with the general purpose Biomation K100-D, our fastest-selling logic analyzer ever.

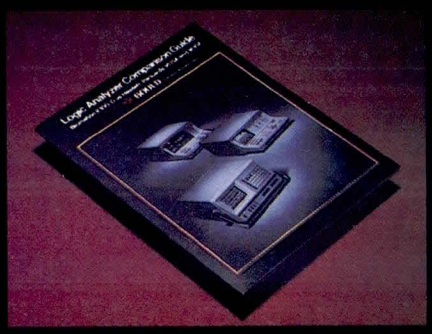
Compare depth of information.
A data domain (software) analyzer —even a unit as sophisticated as the H-P 1610B—simply does not give you all the information you need for debugging your mainframe, mini- and microprocessor-based systems. During the critical system-integration stage of a development cycle, a problem that looks like a software failure may turn out to be a not-too-obvious hardware malfunction. The K100-D's data/timing capability lets you analyze software/hardware relationships and find the problem, wherever it originates. You can display up to 16 channels of critical timing information about race conditions and phase relationships between signals.

So vital is this timing information to complete problem analysis that industry trends indicate logic analyzers of the future will have both data and timing analysis capabilities—like the K100-D has today!

Compare data domain range.
The high-speed K100-D gives you data domain capability to 70 MHz —as compared with the 1610B's 10 MHz rate—for use with faster multiplexed microprocessors, computers, and ECL bit-slice processors. At 12 to 70 MHz, the K100-D gives you 16 channels of data display, with 1024 words of memory.

Operating at 0 to 10 MHz, both units give you 32 channels of data domain information. But the K100-D's memory is 8 times as deep as the 1610B's—512 words versus 64. The 1610B's 7 levels of triggering exceed the needs of most users, and those who do need this capability can generally get it from their development system. With the K100-D, you don't sacrifice vital timing information for data domain capabilities you don't need.

The final analysis.
To help you evaluate your needs before you buy, we've prepared a point-by-point competitive comparison of the Biomation K100-D and the H-P 1610B. (Incidentally, it also shows how the K100-D beats H-P's general purpose 1615A hands down.) To get your free copy, just use the reader service number or write Gould Inc., Instrument Division, 4600 Old Ironsides Drive, Santa Clara, CA 95050. For faster response, call 408-988-6800.



Hewlett-Packard 1610B
A sophisticated data-domain-only logic analyzer

Analysis: Software
Speed: to 10 MHz
Channels: 32 data
Memory: 64 words

Biomation K100-D
The industry's finest data/timing logic analyzer

Analysis: Software & Hardware
Speed: to 70 MHz data domain
to 100 MHz time domain
Channels: 32 data to 12 MHz,
16 data to 70 MHz
16 timing to 100 MHz
Memory: 1024 words @ 16 channels
512 words @ 32 channels

BIOMATION K100-D

Got a glitch? get a GLITCH FIXER FROM GOULD

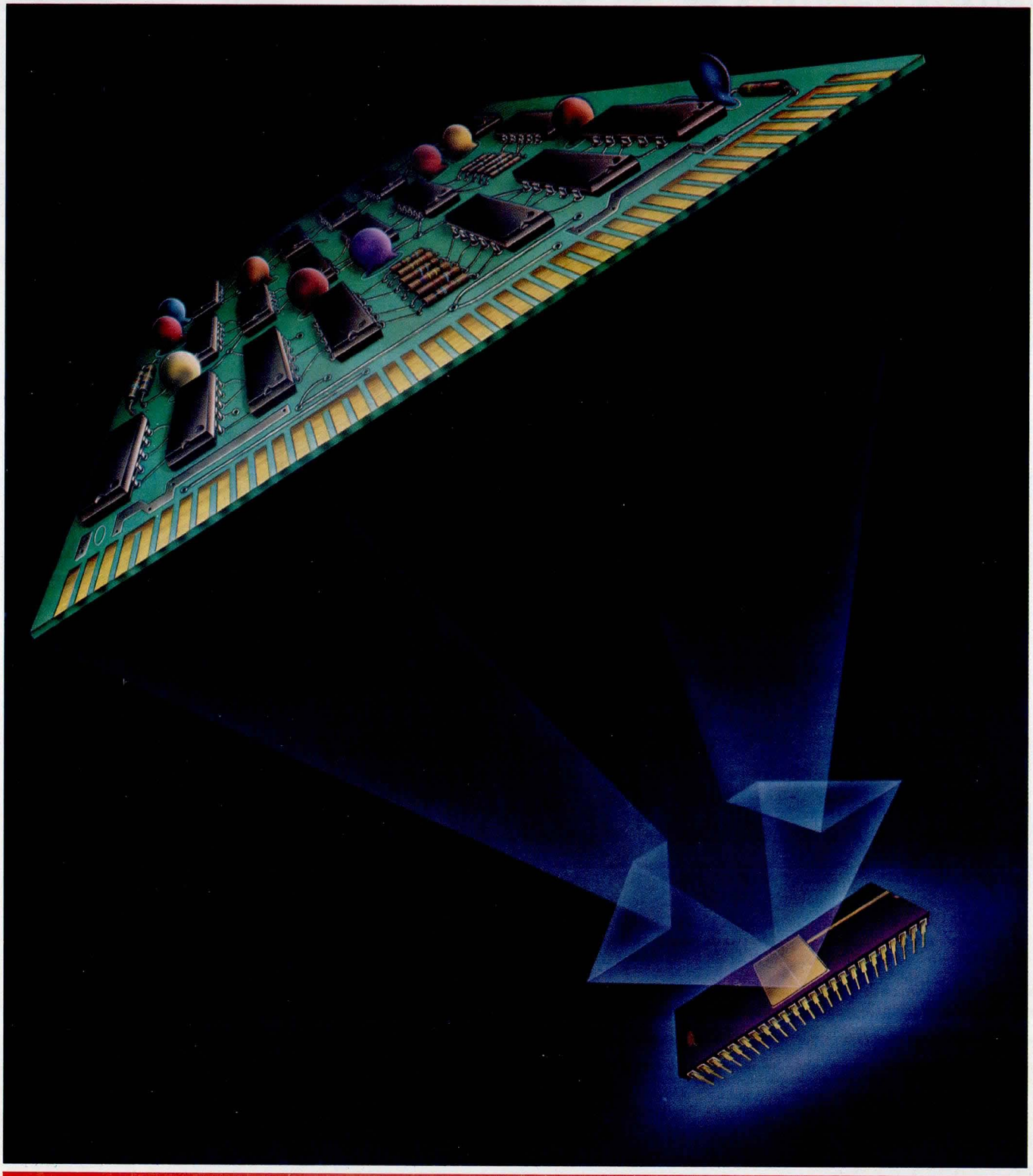
GOULD

An Electrical/Electronics Company

CIRCLE 7 ON INQUIRY CARD

FAIRCHILD

A Schlumberger Company



We just reduced your bus

Introducing the fastest single-chip IEEE-488 bus in the business.

Fairchild's 96LS488 is the first and only General Purpose Interface Bus that performs all the functions of Talker, Listener and Talker/Listener on a single low-power Schottky chip. And it's microprocessor-independent.

No one can touch the 96LS488 for speed, either. It operates at the full bus specifications of 1 MHz data rate—four times faster than its closest competition.

It drives the bus directly.

The 96LS488 contains all the termination resistors and 48 mA drivers for the management, bus handshake and parallel Poll required for the bus. It implements all IEEE-488 functions internally and features simple system handshake for ease of interface.

A bus load of features.

The 96LS488 requires only a single 5V power supply. It has:

Separate Talk and Listen address capability.

Secondary address capability.

Talk only and Listen only capability.

Source handshake delay programmable for low or high-speed data drivers.

Serial Poll and parallel Poll capability.

A device Trigger and Device Clear outputs.

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And all bus I/O signals comply with IEEE-488 input threshold, termination and output specs.

We'll route you an evaluation kit today.

The 96LS488E is available to you now. You can begin to design with it immediately by contacting your local Fairchild Semiconductor distributor for an evaluation kit. This kit includes:

Two 96LS488E's.

A complete data sheet describing the functions and parameters of the 96LS488.

An application guide showing information on hookup with various microprocessor-based systems.

The names of our 96LS488 applications specialists you can call to answer any additional questions.

There's no longer any need to spend extra time designing an interface logic. Our bus gets you there much faster. And much easier, too.

For more information call or write 96LS488 Bus at Fairchild Semiconductor Products Group, P.O. Box 880A, Mountain View, California 94042. Tel: (415) 962-3716. TWX: 910-379-6435.

Fairchild Camera and Instrument Corporation

interfacing problems.

CIRCLE 8 ON INQUIRY CARD

CALENDAR

CONFERENCES

DEC 8-10—Internat'l Electron Devices Meeting, Washington Hilton, Washington, DC. INFORMATION: Melissa Widerkehr, Courtesy Associates, 1629 K St, Washington, DC 20006. Tel: 202/296-8100

DEC 10-11—Computer Networking Symposium, Gaithersburg, Md. INFORMATION: Computer Networking, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007

JAN 13—Invitational Computer Conf, South Coast Plaza Hotel, Costa Mesa, Calif. INFORMATION: B. J. Johnson & Assoc, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

JAN 13-15—Communication Networks Conf and Expo, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Terri Hamilton, The Conference Co, 60 Austin St, Newton, MA 02160. Tel: 617/964-4550

JAN 13-15—SOUTHCON '81, Atlanta, Ga. INFORMATION: Robert Myers, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

JAN 19-22—ATE Seminar/Exhibit, Pasadena Center, Pasadena, Calif. INFORMATION: Jennifer Garlid, 1050 Commonwealth Ave, Boston, MA 02215. Tel: 617/232-5470

FEB 9-12—Internat'l Symposium on Information Theory, Santa Monica, Calif. INFORMATION: Profs Izhak Rubin or Kung Yao, System Science Dept, 4531 Boelter Hall, U of Southern California, Los Angeles, CA 90024. Tel: 231/825-2240

FEB 18-20—Internat'l Solid State Circuits Conf, Hyatt Hotel, New York, NY. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

FEB 23-26—Compcon Spring '81, Jack Tar Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 9-12—Software Engineering Internat'l Conf, San Diego, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-3386

MAR 23-25—Office Automation Conf, Albert Thomas Convention Ctr, Houston, Tex. INFORMATION: Carol Sturgeon, Office Automation Conf, PO Box 9658, Arlington, VA 22209, Tel: 703/558-3617

MAR 23-26—Internat'l Conf on Digital Communications, Congress Bldg, Internat'l Fair of Genoa, Genoa, Italy. INFORMATION: Manager, Rome Branch of Administrative Office, 5th ICDSC, Telespazio SPA, Corso D'Italia 43, 00198 Rome, Italy

MAR 24-26—FOC '81 East, Internat'l Fiber Optics and Communications Expo, Hyatt Regency, Cambridge, Mass. INFORMATION: Ellen M. Bond, Information Gatekeepers, Inc, 167 Corey Rd, Brookline, MA 02146. Tel: 617/739-2022

MAR 30-APR 1—IEEE Internat'l Conf on Acoustics, Speech, and Signal Processing, Sheraton-Atlanta Hotel, Atlanta, Ga. INFORMATION: Ronald W. Schafer, Dept of Electrical Engineering, Georgia Institute of Technology, Atlanta, GA 30332. Tel: 404/894-2917

APR 7-9—Electro, Coliseum and Sheraton Ctr, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

APR 28-30—Internat'l Telecommunications Forum, Concorde Lafayette Hotel, Paris, France. INFORMATION: Dusty Rhodes, Arthur D. Little Decision Resources, Acorn Park, Cambridge, MA 02140. Tel: 617/267-3456

MAY 19-21—INTELEC '81 (Internat'l Telecommunications Energy Conf), Royal Lancaster Hotel, London, England. INFORMATION: INTELEC '81 Secretariat, The Institute of Electrical Engineers, Savoy Pl, London WC2R OBL, England

SEMINARS

DEC 1980-FEB 1981—Data Communications for Minicomputer Users, various U.S. cities. INFORMATION: Margaret Harveston, MICOM Systems, Inc, 9551 Irondale Ave, Chatsworth, CA 91311. Tel: 213/882-6890

DEC—Special Curricula on Data and Voice Technology, various dates and locations. INFORMATION: Systems Technology Forum, Inc, 8991 Cotswold Dr, Burke, VA 22015. Tel: 703/425-9441

DEC—Data Communications: Introduction to Concepts and Systems; Advanced Concepts and Systems; and Effective Network Design, various dates and locations. INFORMATION: Joe Menendez, Datapro Research Corp, Delran, NJ 08075. Tel: 609/764-0100

Microprocessor Application Design, various dates and locations. INFORMATION: Ann Verdi, Advanced Micro Devices, Customer Education Center, 490-A Lakeside Dr, PO Box 453, Sunnyvale, CA 94086. Tel: 408/732-2400; outside Calif, 800/538-8450

FEB 24-25—Midwest Digital Equipment Exhibit and Seminar, Thunderbird Motel, Minneapolis, Minn. INFORMATION: Kim Shobe, Loonam Associates, Inc, 7720 Bush Lake Rd, Minneapolis, MN 55435. Tel: 612/831-1616

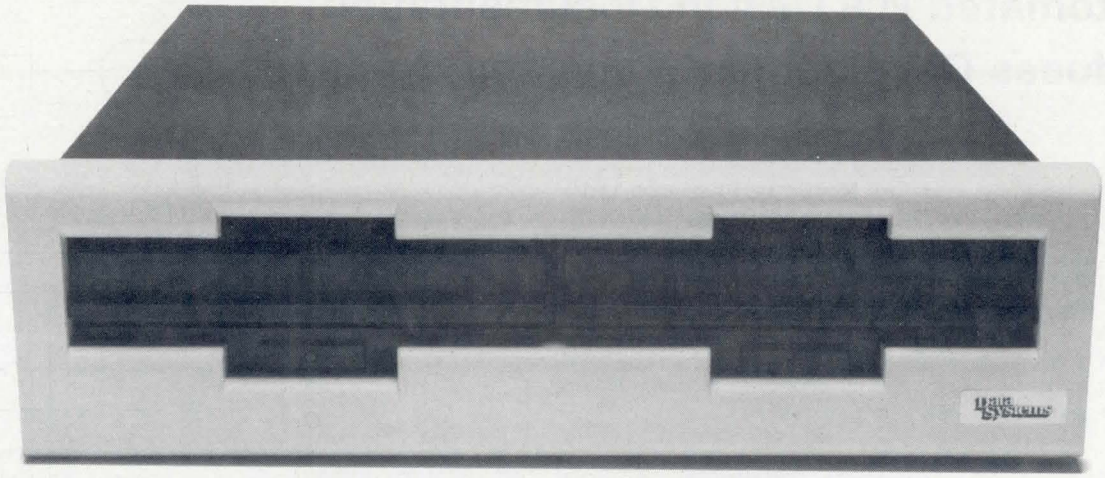
SHORT COURSES

JAN 26-30—Structured Programming and Software Engineering; FEB 2-4—Computer Communications Systems and Networks: FEB 23-25—Microcomputers in Control Systems; AND FEB 26-27—Microcomputers Interfacing Methods, George Washington U, Washington, DC. INFORMATION: Director, Continuing Engineering Education, George Washington U, Washington, DC 20052. Tel: 202/676-6106

Microcomputer Workshops, various dates and locations. INFORMATION: Intel Customer Training at 27 Industrial Ave, Chelmsford, MA 01824, Tel: 617/256-1374; Gould Ctr, E Tower, 2550 Golf Rd, Suite 815, Rolling Meadows, IL 60008, Tel: 312/981-7250; and 1350 Bordeaux Dr, SV3-1, Sunnyvale, CA 94086, Tel: 408/734-8102

Announcements intended for publication in this department of *Computer Design* must be received at least two months prior to the date of the event. To ensure proper timely coverage of major events, material preferably should be received six months in advance.

THE DSD 440. TOTAL DEC® RX02 COMPATIBILITY,



AND MORE.

The DSD 440 is the only alternative to the DEC RX02 that's 100% software, hardware and media compatible with LSI-11, PDP®-11 and PDP-8 computers, including those with extended memory. It can be configured as an RX02 for DEC double density or IBM 3740 single density recording, or as an RX01 for backward operating system compatibility.

MORE

A 512-byte hardware bootstrap is built into all PDP-11 and LSI-11 interfaces. It loads system software automatically from either single or double density diskettes. Extensive self-testing is DIP-switch selectable with the "Hyperdiagnostics" that run without being connected to a computer. The low profile 5¼-inch DSD 440 features write protection and diskette formatting.

FASTER

The optimized DSD 440 microcode increases system throughput when using the RT-11 foreground/background monitor. In particular, the DSD 440 with an LSI-11 runs fill and empty buffer operations 20% faster than an RX02.

FOR LESS

The DSD 440 is the RX02 compatible flexible disk system that combines high performance and advanced features with fast delivery... at a lower price. For further information, call or write Data Systems Design today. A data sheet and price list will be forwarded to you immediately.

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Tel: (408) 727-9353 TWX: 910-338-0249

CIRCLE 9 ON INQUIRY CARD

LETTERS TO THE EDITOR

CORRECTION

Through an unfortunate error, when the Digital Control and Automation Systems section of the September issue was printed, the names and company affiliation of the authors of the lead article were omitted. The article head should have read

Automated PCB Design Documentation Reduces Development Time and Costs

Ken W. G. Blais and Girvan L. Patterson

Bell-Northern Research Ltd
PO Box 3511, Station C, Ottawa K1Y 4H7, Canada

This article describes the Circuit Pack System developed by Bell-Northern Research to automate and integrate all elements of computer aided documentation for printed circuit boards. System design eases integration backward to include computer aided engineering and forward into computer aided manufacturing. For those readers who may have missed it, the article appears on pp 86-99 of the Sept 1980 issue of *Computer Design*.

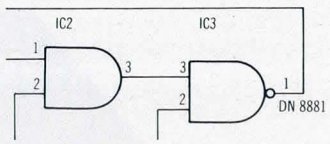
CORRECTION

Please note the following corrections to the article by Alan W. Bentley, "Single-Chip Controller Increases Microprocessor Throughput," (Sept 1980):

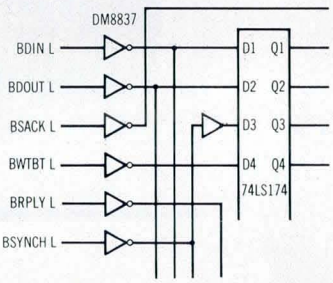
Page	Column	Line	Error	Correction
127	right-hand	second	state 1 ($\overline{Q_H}$,$\overline{Q_G}$)	state 1 ($\overline{Q_H}$,Q_G)
127	right-hand	last	(HOLD)	(HOLDA)
128	left-hand	first	state 2 (Q_H,Q_G)	state 2 (Q_H,$\overline{Q_G}$)
128	right-hand	next to last	2-state	two state

To the Editor:

I have found two errors in my article, "A Diagnostic Module Design for the LSI-11/2 Microcomputer," which was published in the Aug 1980 issue of *Computer Design*. In Fig 3 (p 124), IC2 should be an AND gate instead of the NAND gate shown.



In Fig 4 (p 124), the labels BWTBT L and BSACK L should be interchanged.



I hope that these corrections will clear up any confusion among readers who wish to construct a copy of the bus monitor.

Robert Bruce
Tektronix, Inc
Beaverton, Ore

To the Editor:

Robert Swanson's article, "Matrix Technique Leads to Direct Error Code Implementation," in your Aug 1980 issue is very interesting, but it has an error in Fig 5 (p 104). The second term in Fig 5(b) is incorrect. According to Figs 4 and 5(a), Fig 5(b) should be

$$H \cdot r = \sum_{i=1}^{15} h_i \cdot r_i = 1 \cdot \begin{bmatrix}1\\1\\0\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}1\\0\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\0\end{bmatrix} = \begin{bmatrix}0\\0\\1\\0\end{bmatrix}$$

However, this way, $H \cdot r$ is not equal to $H \cdot e$. The reason is that what is designated as code word c in Fig 5(a) is not a code word because its dot product with H is not zero

$$H \cdot c = \sum_{i=1}^{15} h_i \cdot c_i = 1 \cdot \begin{bmatrix}1\\1\\0\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}1\\0\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\0\end{bmatrix} = \begin{bmatrix}0\\1\\0\\1\end{bmatrix}$$

When corrected, CODE WORD c = 101011000100001, whose dot product with H is zero

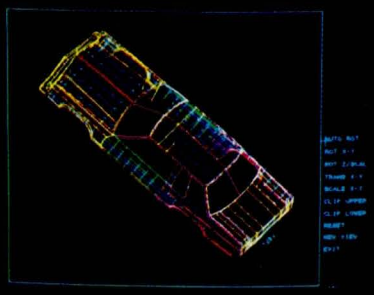
$$H \cdot c = \sum_{i=1}^{15} h_i \cdot c_i = 1 \cdot \begin{bmatrix}1\\1\\0\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}1\\0\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\0\\0\\1\end{bmatrix} = \begin{bmatrix}0\\0\\0\\0\end{bmatrix}$$

In this case, $H \cdot r$ equals $H \cdot e$, that is

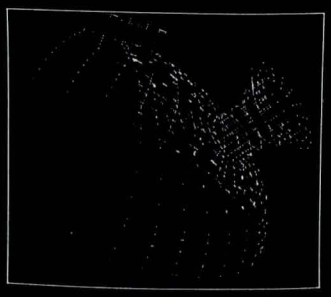
$$H \cdot r = \sum_{i=1}^{15} h_i \cdot r_i = 1 \cdot \begin{bmatrix}1\\1\\0\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\1\\0\end{bmatrix} + 1 \cdot \begin{bmatrix}1\\0\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\1\\0\\1\end{bmatrix} + 1 \cdot \begin{bmatrix}0\\0\\0\\1\end{bmatrix} = \begin{bmatrix}0\\1\\1\\1\end{bmatrix} = h_{10} \cdot e_{10}$$

Tamas Roder
Computer Center of Univ Eotvos L
Budapest, Hungary

Freedom of Expression.

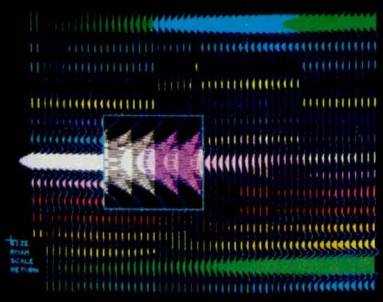


Only Megatek gives you all three, the excitement of dynamic raster color...



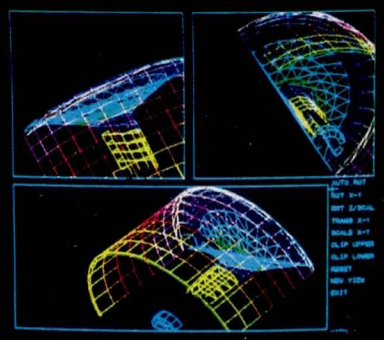
...the precision of 4096 x 4096 high resolution calligraphic Whizzard systems...

...and user-oriented software to make it easy to implement your application.

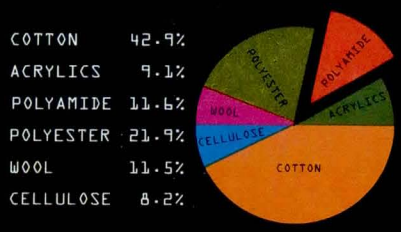


Powerful, real-time dynamics enable you to scan the display then zoom in for added detail.

A large virtual display gives you the full picture, with the added information of up to 16 colors at a time.



Rotations mean you can view models from any angle and segment the display into multi-viewports.



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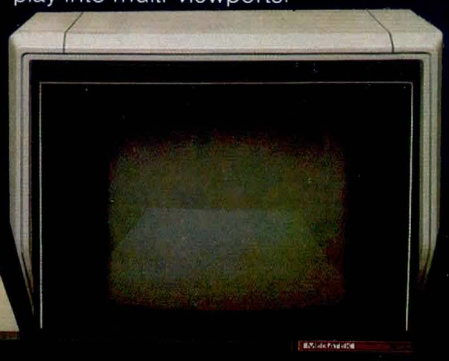

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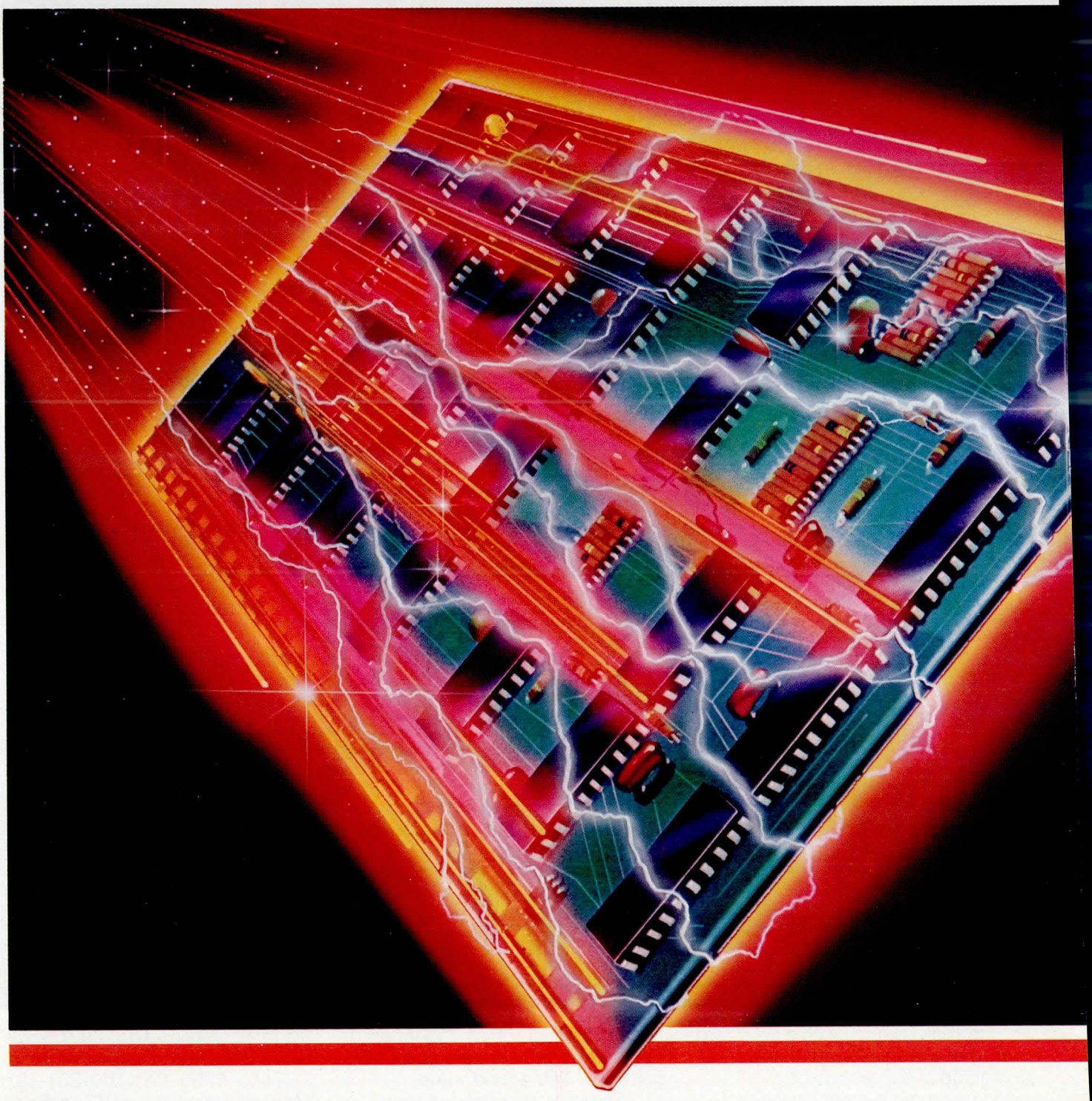

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Our latches, flip-flops and counters are unsurpassed for speed and low-power requirements.

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Our speedy specs.

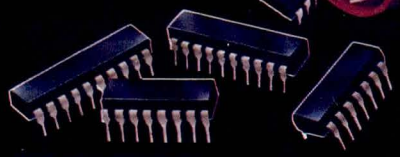
LATCHES
74F373 and 74F533 (inverted output version) 3-state transparent octal latches

Setup time. . . . . 2 ns min
Hold time. . . . . 3 ns min
Enable/disable time. . . . . 11 ns
Data-to-output propagation delay . . 74F533—9 ns max
74F373—6.5 ns max
I_{CC} . . 74F533—61mA max
74F373—55mA max

FLIP-FLOPS
74F374 and 74F534 (inverted output version) 3-state octal D-type flip-flops with common Clock and Output Enable

Toggle frequency. . . 110 MHz typ
Setup time. . . . . 2 ns min
Hold time. . . . . 2 ns min
Clock-to-output propagation delay . . . 9 ns max
Enable time . . . 10 ns max
I_{CC} . . . . . 86 mA max

Both our 3-state latches and flip-flops contain a patented output structure for easier bus interface and design.



COUNTERS
74F190 Series high-speed up/down counters

Count frequency. . . 130 MHz typ
I_{CC} . . . . . 38 mA typ
Clock-to-output delays. . . . . 5 ns typ
Clock-to-terminal count delays. . . . . 5 ns typ

This series of counters offers virtually twice the count frequency and less than one-third the power requirements of their Schottky counterparts.

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Fairchild Camera and Instrument Corp.

across the board.

CIRCLE 11 ON INQUIRY CARD

16K
32K
64K
12
V_{CC} A8 A9 V_{PP} $\overline{CS}$ A10 PD/$\overline{PGM}$ Q8 Q7 Q6
A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 V_{SS}
V_{CC} A8 A9 V_{PP} PD/$\overline{PGM}$ A10 A11 Q8 Q7
V_{PP} $\overline{CS1}$ A7 A6 A5 A4 A3 A2 A1 A0 Q1 Q2 Q3 V_{SS}
NC/V_{CC} $\overline{CS2}$ V_{CC}/NC A8 A9 A12 PD/$\overline{PGM}$ A10 A11 Q8 Q7 Q6
V_{PP} A13 A7 A6 A5 A4
NC/V_{CC} $\overline{CS}$ V_{CC}/NC A8 A9 A12

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Fifty Years of Innovation

TI's Growing TMS2500 EPROM Family

Device	Description	Power Dissipation*	Access Time*
TMS2564-45	64K	840 mW	450 ns
TMS2532-45	32K	840 mW	450 ns
TMS2532-35	32K	840 mW	350 ns
TMS25L32-45	32K	500 mW	450 ns
TMS2516-45	16K	525 mW	450 ns
TMS2516-35	16K	525 mW	350 ns
TMS2508-30	8K	446 mW	300 ns
TMS2508-25	8K	446 mW	250 ns

*Worst case over operating temperature range

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LOW COST EMULA
AND VICE VERSA.

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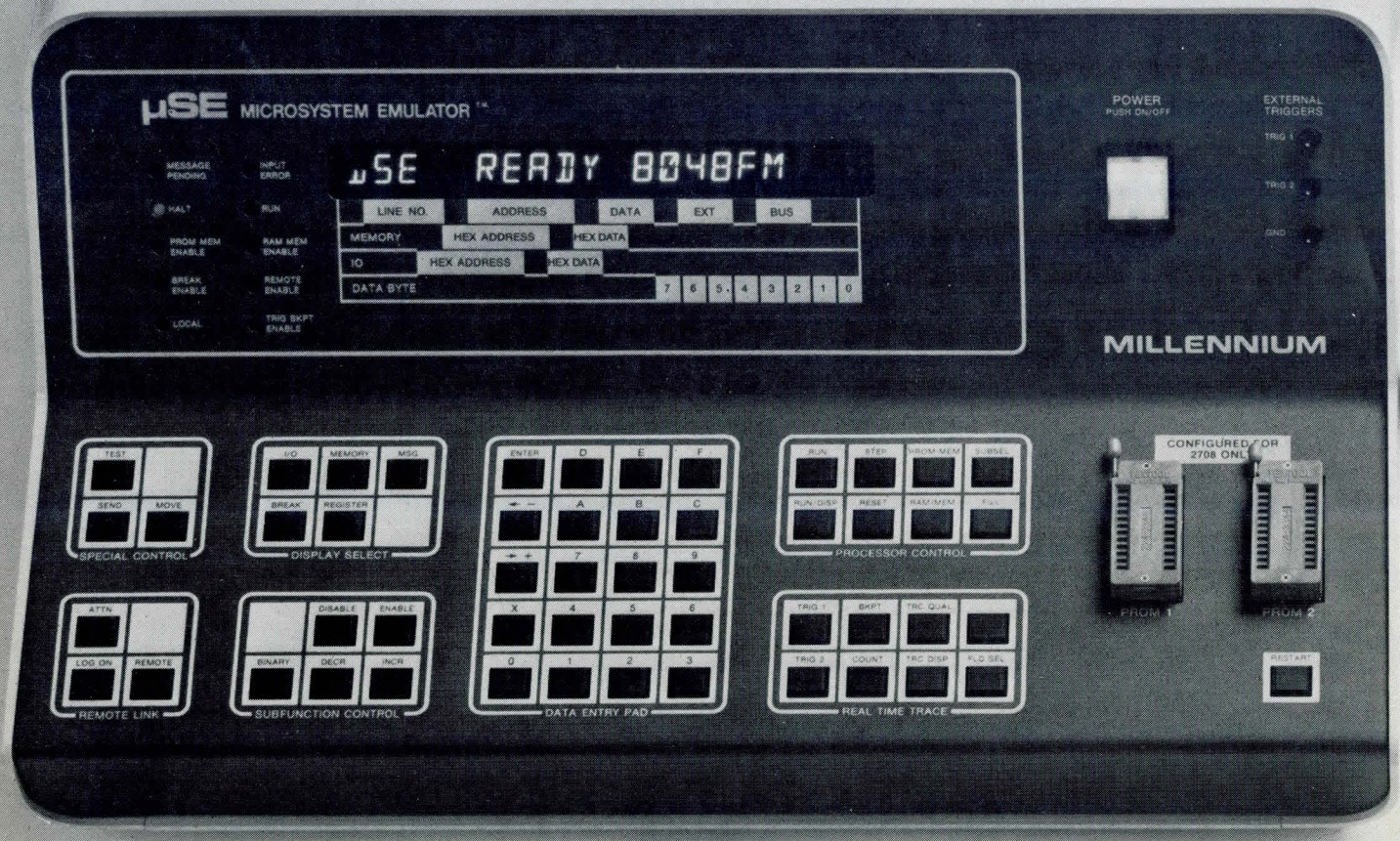

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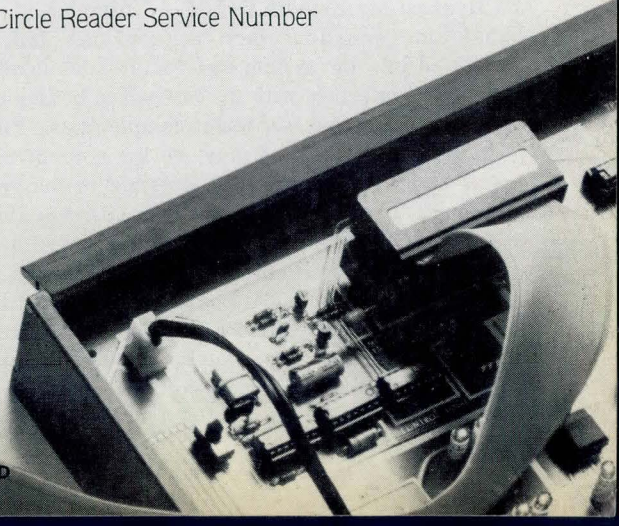


CIRCLE 13 ON INQUIRY CARD

COMMUNICATION CHANNEL

A DISTRIBUTED PROCESSING SYSTEM FOR MILITARY APPLICATIONS— PART 3: THE COMPUTERS

Ralph Mauriello Litton Data Systems
8000 Woodley Ave, Van Nuys, CA 91409

The first two articles in this series [1,2] described the Litton military distributed processing system and the 20M-bit/s serial interelement bus, respectively. Part 3 discusses some of the design considerations involved in the development of computers for the system.

The tasks required of computers for the Litton distributed processing system presented a unique design challenge. Other layers of complexity had to be added to all of the customary functions. System imposed requirements dictated that the computer be capable of bootloading not only from conventional media over standard input/output (I/O) channels, but also from the serial interelement bus (SIB). All nodes require these capabilities; the system concept permits bootload media to be located at any node. However, since economics dictate only one or two bootload media for the entire system, those nodes without bootload media must accept it from the SIB. Due to these cost constraints, and because physical transfer of the media may be impractical, a "Request for Remote Bootload" function is required to handle the situation when a previously failed node is reinserted into the system and requires bootload.

Efficient interface with the SIB had to be implemented in order to minimize software complexities. Physical implementation of the bus must be transparent to user programs and as transparent as possible to the systems programmers. The final requirement imposed by the system is to support SIB reconfiguration in the event of a failure.

A mandatory requirement is the preservation of existing software. Billions of dollars have been invested in the solution of military problems. Emulation is required because none of the new commercially available computers is software compatible with existing military computers.

Configurability is also required. The role of a military systems house requires that its systems use designated standard computers where indicated, such as Navy UYK-20 and Army GYK-12. For this reason, having the choice of any military computer architecture is vital to the systems designers. Furthermore, the wide range of problems encountered demands the availability of a range of throughput, memory, and I/O combinations to permit cost-effective solutions.

The need for simultaneous minimization for both procurement and life cycle costs presents a difficult challenge. Standardization usually lowers life cycle cost, but increases procurement cost. For example, the UYK-20 often has been used to solve problems where a smaller, cheaper unit could have performed the task.

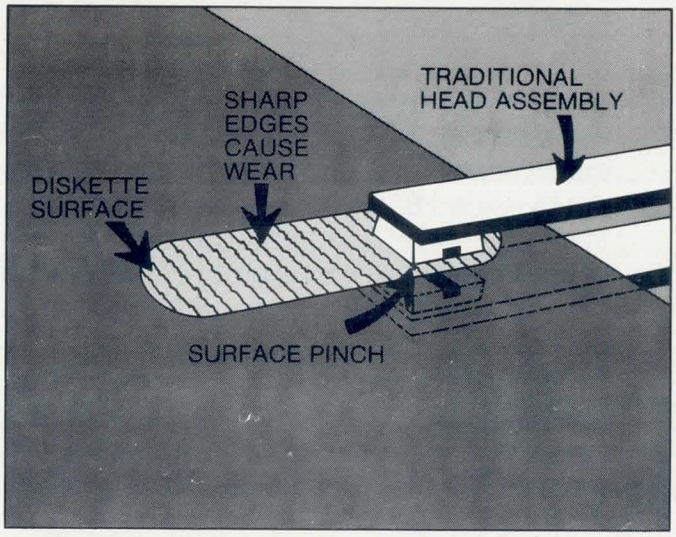
Finally, the design of the computer must permit cost-effective technology insertion. The rapid advancements in electronics technologies coupled with the extensive and time-consuming military testing procedures (lives are at stake) result in deployment of near-obsolete equipment.

The design solution to these requirements comprises a family of firmware controlled emulators with extensions to the target computer's architecture for applicability to a distributed processing system (DPS). Use of microcode control for the central processing unit (CPU) repertoire, the most effective emulation technique, permitted the use of firmware for such system functions as interface with the SIB and complete system bootload and initialization. This approach saves hardware and simplifies software design. An architecture-independent internal bus and building block modules provide life cycle cost advantages and permit technology insertion. Design features of the distributed processing system computers shown in the Panel (page 32) are discussed in detail below.

(continued on page 26)

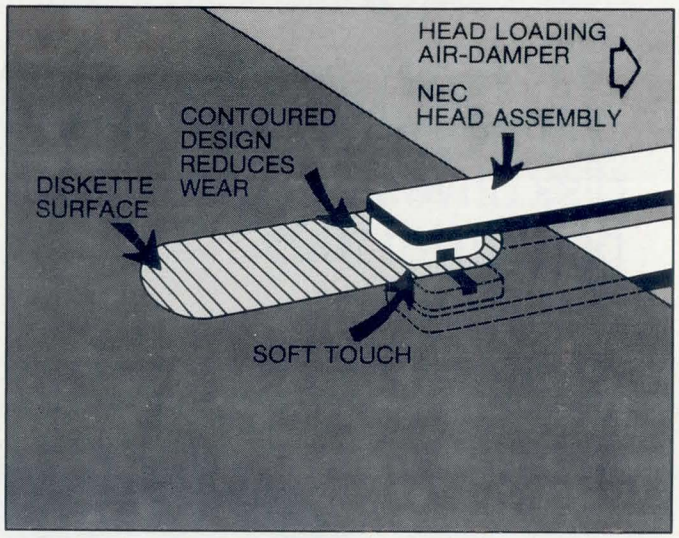
Introducing the NEC Soft-Touch.™

Other diskette drives



Dual-sided diskette drives require contact of both heads with the media to read or write. This causes head wear and a pinching action that deforms, mars and scratches the media surface, shortening head and media life.

NEC diskette drive



The NEC "Soft-Touch" drive uses advance-contour head design and a unique air-damper to load heads. These features smooth and cushion the contact of head with media surface, nearly doubling the life of both the heads and the recording media.

The industry's newest 1.6MB diskette drive. With twice the MTBF. Twice the media life.

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Head wear. An advanced design ceramic read/write head assures maximum signal transfer efficiency while drastically reducing head wear and media chafing.

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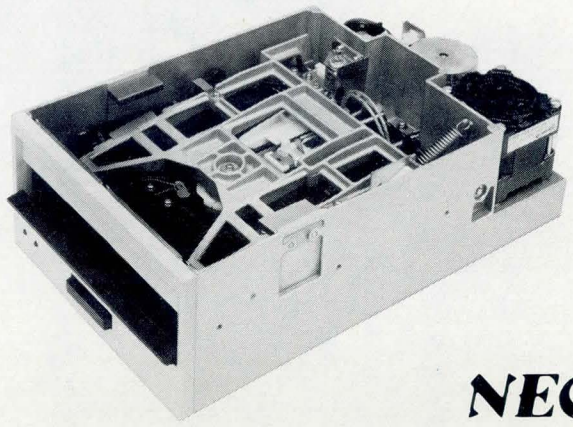

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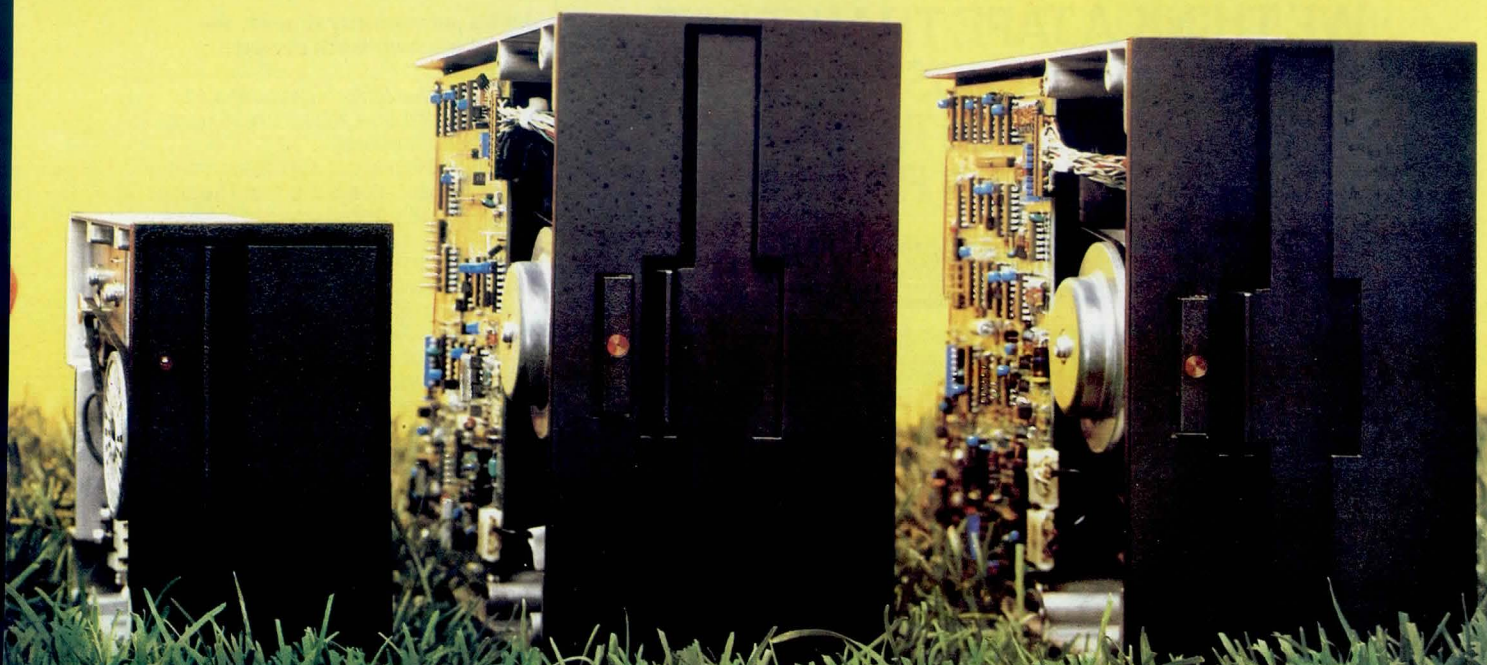

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Multiple-Speed Versions Of the Same Architecture

Two different UYK-20 CPU emulators are operational: a 2-card 7.5 x 8.75″ (19 x 22.2-cm) microcomputer, L-3220, that executes at 50% of UYK-20 throughput; and L-3320, a 3-card minicomputer that provides 100% of UYK-20 throughput. The L-3320 achieved this performance by using only one of its two internal buses; 2-port memories were not available. With both internal buses operating, it is expected that the L-3320 will achieve 120% of UYK-20 CPU speed and handle concurrent I/O operations. Both emulators have the same internal bus interface and can operate in a multicomputer mode off the same bus. Complete software interchangeability has also been demonstrated.

The microcode, operating at a 240-ns clock rate, can be subdivided as follows: (a) emulation of the UYK-20 instruction repertoire; (b) emulation of the UYK-20 I/O operations in a manner that is transparent to the programmer; (c) emulation of the architectural features of the UYK-20 (eg, L-3220 emulation of two sets of general purpose registers is achieved in firmware); (d) enhancements to architecture for distributed system operations; and (e) microdiagnostics.

These two basic units represent only two of the many throughput rates available to system designers. System growth options provide such functional capabilities as floating point hardware, cache memory, and independent I/O, to give the system designer many choices. In addition to variable throughputs, the versatile L-3220 gives the system designer the availability of multiple functions using the same hardware. In addition to its use as a UYK-20 emulator, it may be used as an independent input/output controller (IOC), 4M-instruction/s frontend microprocessor, or a multiple-peripherals controller.

Architecture-Independent Internal Bus

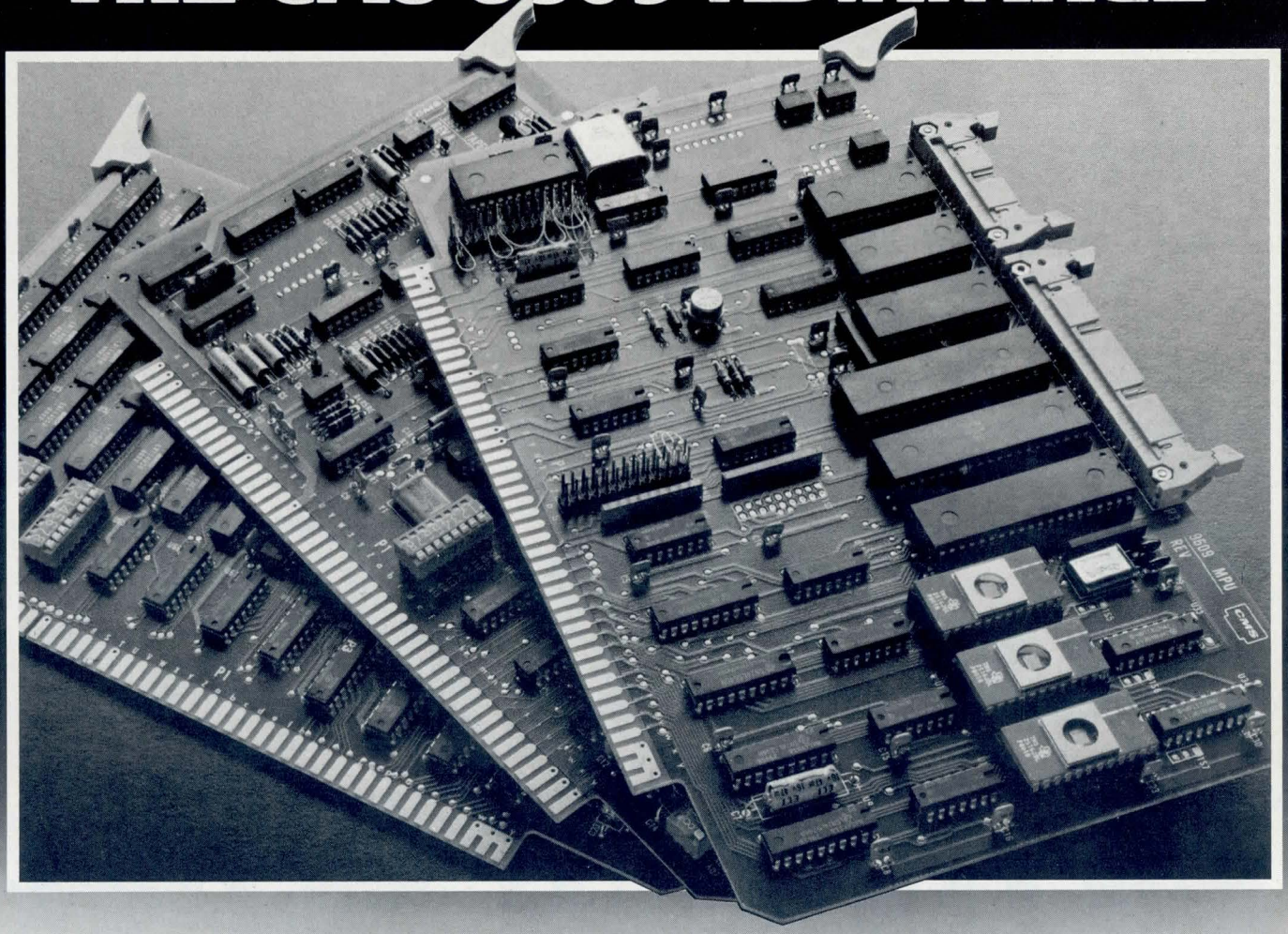
A major feature of DPS computers is an architecture-independent intra-element bus (IEB) that permits implementation of any target computer without redesign of the IEB, memories, or I/O interface cards. All data or control transfers over the IEB are fully programmable under CPU-resident firmware control, permitting architectural independence. The IEB provides data and address lines as required for the target computer, and eight control lines. The control lines have been coded to provide a programmable definition of the use of the data and address lines. This scheme permits interface to and control of many classes of devices [memories, direct memory access (DMA), I/O controllers] without impinging upon the memory address space.

Multiple-CPU operation on the IEB has been demonstrated in the DPS project with firmware that supports the multiprocessing function. All CPUs may execute a single set of executive code and, through an address relocation technique under firmware control, have access to private tables for executive control functions.

Multiple CPUs, DMA I/O devices, and the like must be permitted to gain access to the IEB; therefore, bus arbitration logic is required. Since survivability is critical in a military system, bus arbitration logic is replicated on each of the cards capable of demanding access to the bus. This

(continued on page 30)

COMPARE
THE CMS 6809 ADVANTAGE



Creative Micro Systems is proud of its line of general purpose microprocessor support modules. These M6800/M6809 based modules are pin and outline compatible with the industry standard EXORcisor* and Micromodule* bus.

COMPARE THE CHOICE

That's why we want you to compare our products with the competition before you design your next microprocessor based system.

Each module in our product line is designed to respond to the needs of a major computer system function. Our 9609 module, featured above, is a complete microcomputer on a single board. It features the MC6809 processor, 6K of EPROM, 1K of RAM, 40 parallel I/O lines, 2 RS-232C serial ports, BREAK detect, 3 16-bit programmable timers, priority interrupt vector generator and a power failure protect/restart circuit.

For more extensive system requirements, the 9609 is supported by a variety of Memory, I/O, and Data Acquisition modules, and a broad line of card cages, power supplies, mother boards, prototype boards and accessories.

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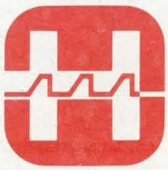

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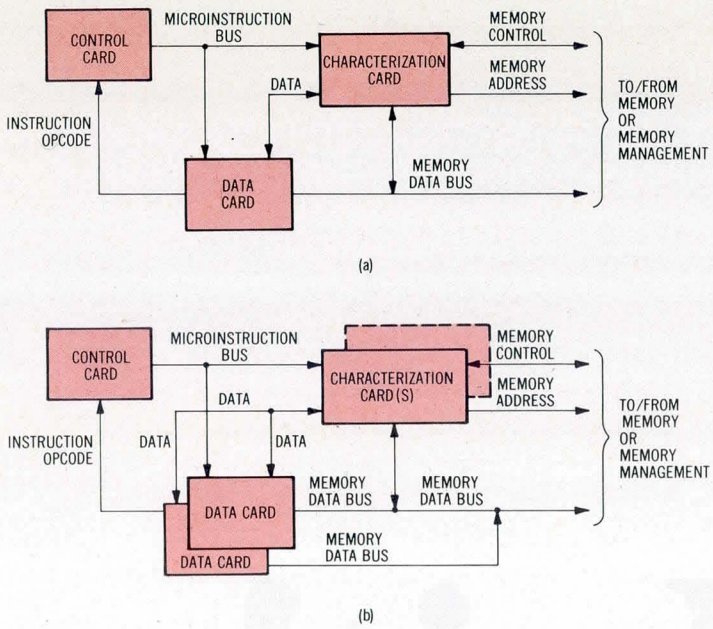


Fig 1 Two possible DPS CPU configurations. (a) DPS minicomputer CPU, and (b) 32-bit medium scale computer CPU

eliminates a single-point failure and allows each bus requester to determine for itself whether or not the bus is available. It also permits continued bus operation in the event of card extraction or failure.

DPS Standard Building Blocks

The flexibility afforded by the DPS hardware building blocks allows their cost-effective deployment in a wide range of diverse system applications. The key to this is the architecture-independent internal (CPU/memory) bus with which all DPS building blocks must be compatible. Building blocks described are realtime emulators, memory, I/O interface cards, low cost emulators, and system expansion options.

Realtime Emulators (Minicomputer)—for 16-bit machines, a 3-card CPU [Fig 1(a)], and for 32-bit machines a 4- or 5-card CPU, depending on target computer complexity [Fig 1(b)]. Both CPUs are capable of executing the basic repertoire of the target CPU at speeds equal to or greater than that of the target CPU. These realtime emulators are implemented with control, arithmetic logic unit (ALU) and register, and characterization cards.

The DPS control card contains 4k words by 80 bits of microinstruction memory, the sequencing and control of the microprogram, and the decode of the microinstruction. This single-card control unit is implemented to be totally independent of data word width, permitting extensive flexibility in its application to various emulators.

The DPS ALU and register card provides a 16-bit slice of the ALU and three sets of 16 registers each. The ALU and register card uses four AMD 2903 4-bit slice processor chips that provide one set of 16 registers of 16 bits each plus a full 2's complement ALU. One such card is used for 16-bit emulators (UYK-20) and two are used for 32-bit emulators (UYK-7).

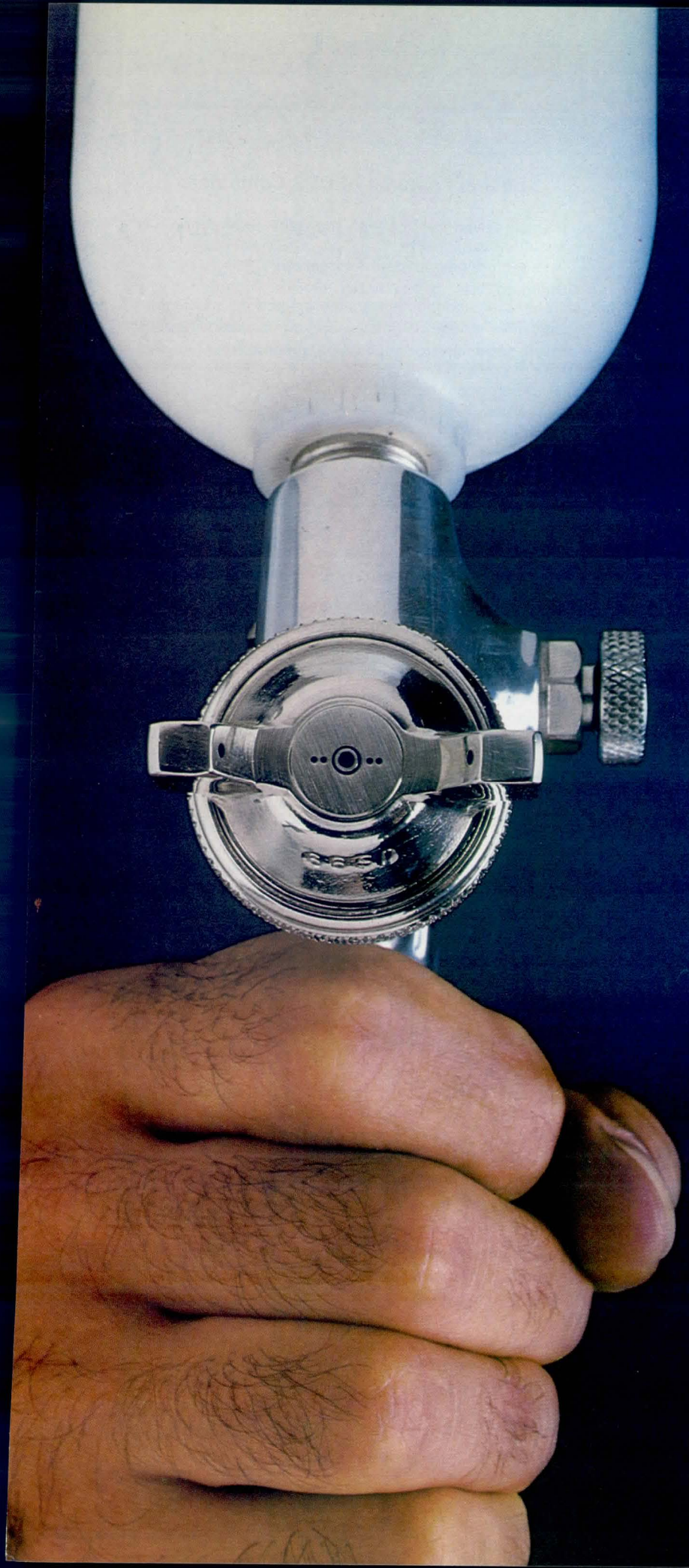
The two previously described cards, control and data, are generic to any emulator design; they are identical for all emulators. It is the characterization card(s) that provides the emulator with its "personality." Interfacing with main memory, the card(s) provides the required unique functions and registers necessary for emulation of the specific target computer. Two characterization cards are required for the AN/GYK-12 and the AN/UYK-7.

Memory—a single circuit card of complementary metal oxide semiconductor (CMOS) or n-channel MOS (NMOS) technology that is independent of CPU architecture and capable of being accessed as 8k words by 36 bits or 16k words by 18 bits. It may be used as local memory for either the low cost or realtime emulator, and for either 16-bit or 32-bit CPUs. This same card is used for common memory implementation when memory management is used.

Input/Output Interface Cards—all I/O interface cards, whether DMA or under CPU (IOC) control, are architecture-independent and thus can use any peripheral with any computer. The modularity also allows incremental upgrading of peripherals.

Three versions of the 1397 interface card exist, 1397A, -B, and -C, offering different speeds and voltage levels. This is a 16-bit or 32-bit wide parallel interface for the standard U.S. Navy computers, UYK-20 and UYK-7. Each card provides two 16-bit channel interfaces between the peripheral and the IEB. The 188-C and RS-232 card provides two channels of interface between the MIL-STD-188-C serial channel and the IEB, or between RS-232 channel and IEB. GYK-12 I/O interface card provides one channel (eight I/O addresses) between U.S. Army standard peripherals and the IEB. This card has DMA capability. Parallel DMA interface card provides a 16-bit parallel interface for peripheral devices that require DMA.

(continued on page 32)



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CIRCLE 18 ON INQUIRY CARD

Low Cost Emulators (Microcomputer)—2-card devices providing execution of the basic target machine repertoire at one-quarter to one-half the speed of the target machine. As a microcomputer, it operates at a rate of 4M instructions/s.

System Expansion Options—including an extended arithmetic card to provide floating point arithmetic, double-precision fixed point arithmetic, and a barrel shifter for high speed execution of shift algorithms. This card may be used with either the realtime or the low cost emulator.

A memory management card provides memory address extension and read/write protection compatible with the target computer. This card accommodates two IEBs and is cascadable to permit multiple-IEB access to a common memory while providing paging and protection. This card may also be used with either the realtime or the low cost emulator.

Two cache memory cards provide 8k words of cache memory plus the necessary controls for adding cache memory to the realtime emulator. This option is not available for the low cost emulator.

Dual-Mode Operation of DPS CPUs

All DPS CPUs can operate both in dual mode, a computer mode that emulates a target CPU, and in microprocessor mode, for high speed specialized functions. Through the use of firmware, these CPUs timeshare the same hardware to perform CPU or IOC functions. The system design required this timeshared mode of the DPS CPUs. Previous systems experience revealed that in many applications the I/O requirements are quite small and cannot justify the use of a computer with an independent hardware I/O controller.

The dual-mode operation is enhanced by a CPU-resident random access memory (RAM) file of 256 words for the L-3320 and 1k words for the L-3220. In addition, one set of general registers is reserved exclusively for firmware use. This firmware reserved set of general registers, plus dedication of a major portion of the RAM file to I/O operations, provides 240-ns transfer from CPU to I/O mode, or vice versa.

Where I/O data rates are low enough to ensure acceptable interference with the required internal data processing, firmware may also be used to handle I/O transfers and thus eliminate a hardware I/O unit. This firmware communicates directly with greatly simplified hardware I/O buffers. The firmware is driven by I/O demand and is responsible for movement of data between the hardware I/O buffers and the main memory so that the programmer may code as if the I/O unit of the target computer were present.

Specialized I/O processing is a further use of this microcode capability. Many specialized types of I/O processing, such as communication link error detection, are slow and awkward to handle while using standard instructions available to software. Some computers avoid this software processing by building extra processing capability into the I/O hardware buffers, but this is costly. The DPS CPU maximizes savings in both hardware and software by operating the CPU in the microprocessor mode to handle specialized I/O processing. The microinstruction provides speed and flexibility of microprocessing for detailed manipulation of bits, fields, and hardware control. Where I/O rates are too high, independent IOC and/or DMA channels are available to the system designer.

Design Features of DPS Computers

Multiple-speed versions of the same instruction set architecture
Architecture-independent internal bus
Standard set of building blocks highlighted by architecture-independent memories and I/O interfaces
Dual-mode operation (microcomputer or minicomputer)
Macro capability for application specific functions (eg, sine or cosine)
Input/output configurability
Fail-safe/soft
Maintainability

Performance Enhancement by Firmware Macros

The use of application specific macros, at no additional CPU hardware cost, can greatly enhance computer performance, and also typically reduces main memory requirements. In a recent application, the CPU demanded a high speed computer mechanization of selected arithmetic and data handling functions. Therefore, functions such as square root, sine/cosine, format, and selective substitute were implemented in firmware.

The primary advantage of firmware over software is faster execution time. A DPS CPU firmware instruction executes in 240 ns, while a software instruction is limited by main memory cycle(s) and the location of the operands. A second, though less significant, advantage is the elimination of storage space in main memory. When the macro is implemented as a callable routine, the savings are not great. However, where the macro is used as "inline" code to increase execution speed by eliminating the overhead of calling and return sequences, the memory savings can be significant.

DPS I/O Configurability

The wide range of I/O options provided gives the system designer the opportunity to achieve cost-effective I/O solutions for systems ranging from very low I/O requirements to transfer rates up to 1M words/s. These options can be summarized as follows:

(1) The DPS CPU (mini- or microcomputer) operates in a dual mode; it is timeshared for CPU functions and I/O functions.

(2) The minicomputer is used exclusively as a CPU, while the microcomputer operates as an I/O controller. When the memories have one port, both computers operate on the same bus (cycle steal).

(3) With a 2-port memory, the minicomputer may operate exclusively as the CPU on one bus, while the microcomputer operates as an IOC on a second, independent bus.

(4-6) Each of the above three configurations can be augmented by DMA capability, thus furnishing the system designer with three additional options.

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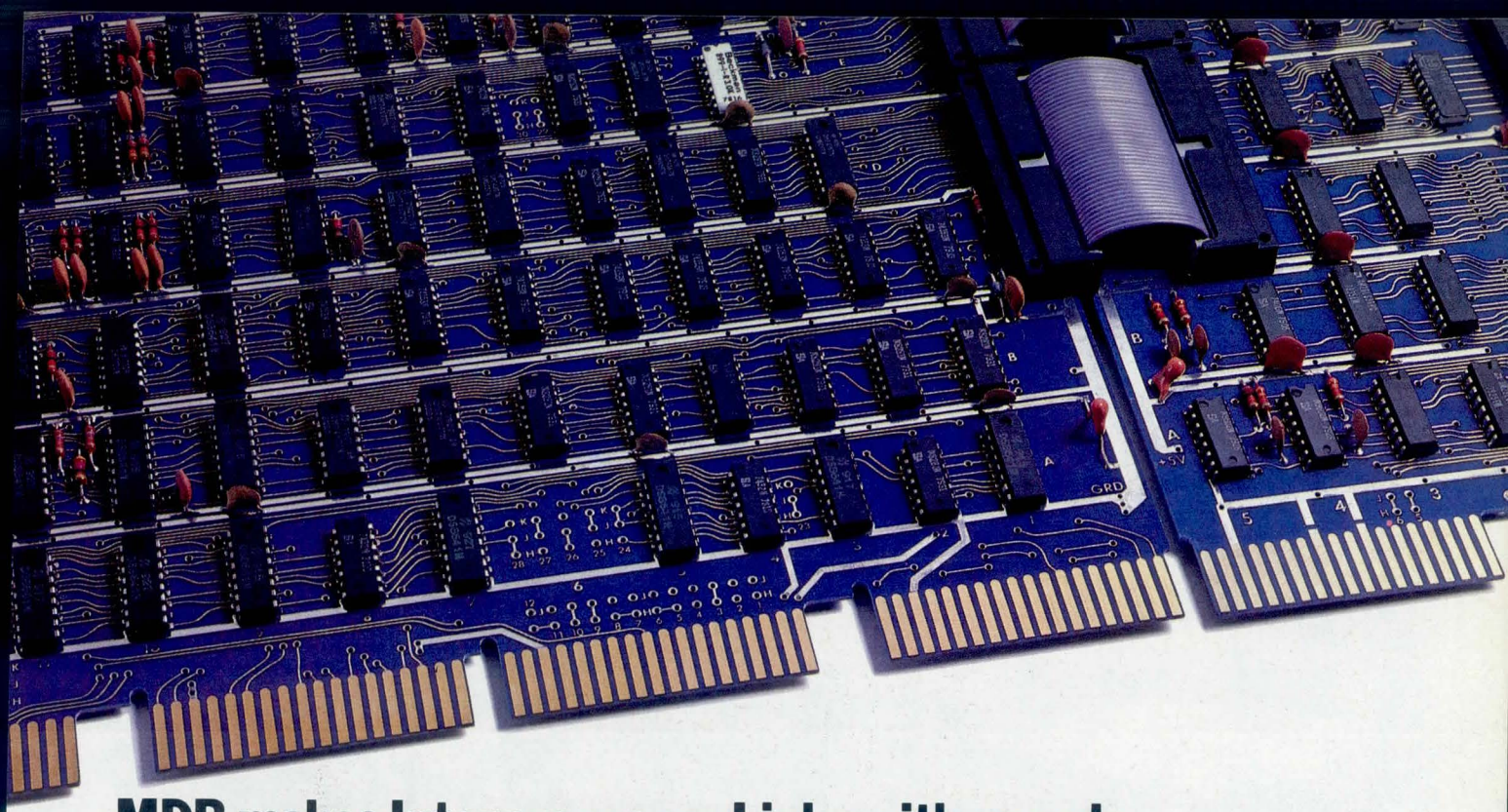

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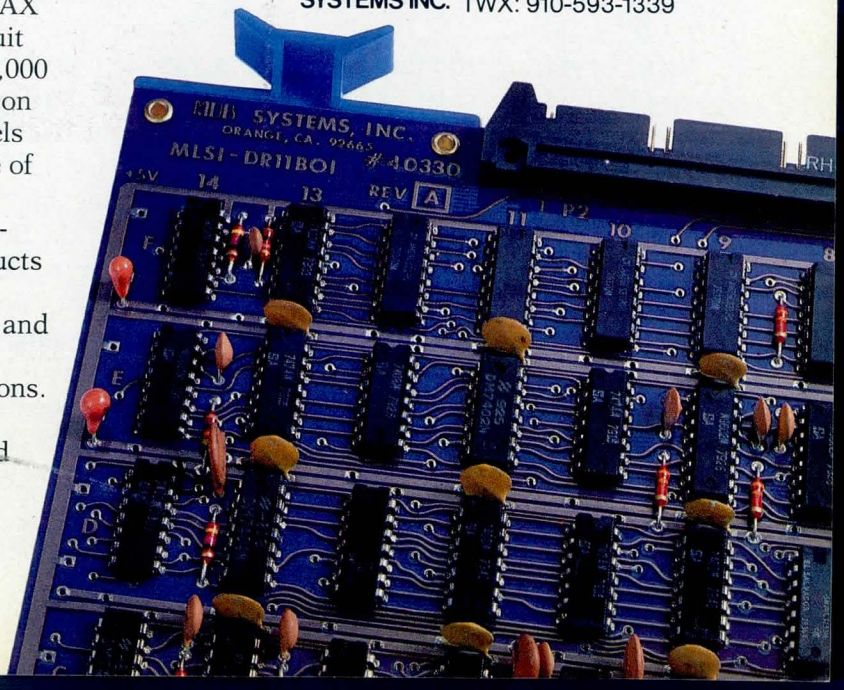

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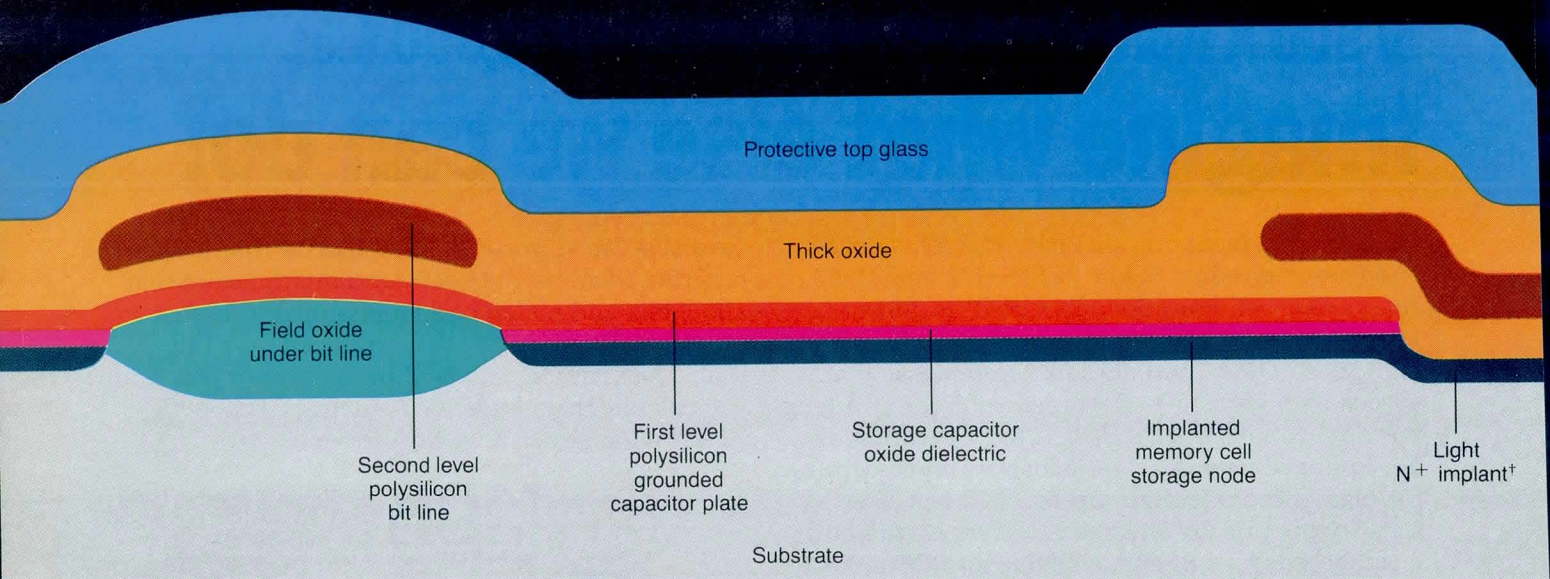
Circle 19 for LSI-11, 20 for PDP-11, 21 for DG, 22 for PE, 23 for IBM.

THE BUSINESS OF DESIGN



By now, you're probably aware that no less than 18 manufacturers have or will introduce their own version of a 64K RAM. And that each version will be at least a slightly different design. So how will you choose one intelligently? How will you base your decision knowing that each manufacturer feels strongly justified in choosing the architecture and manufacturing process it will use?

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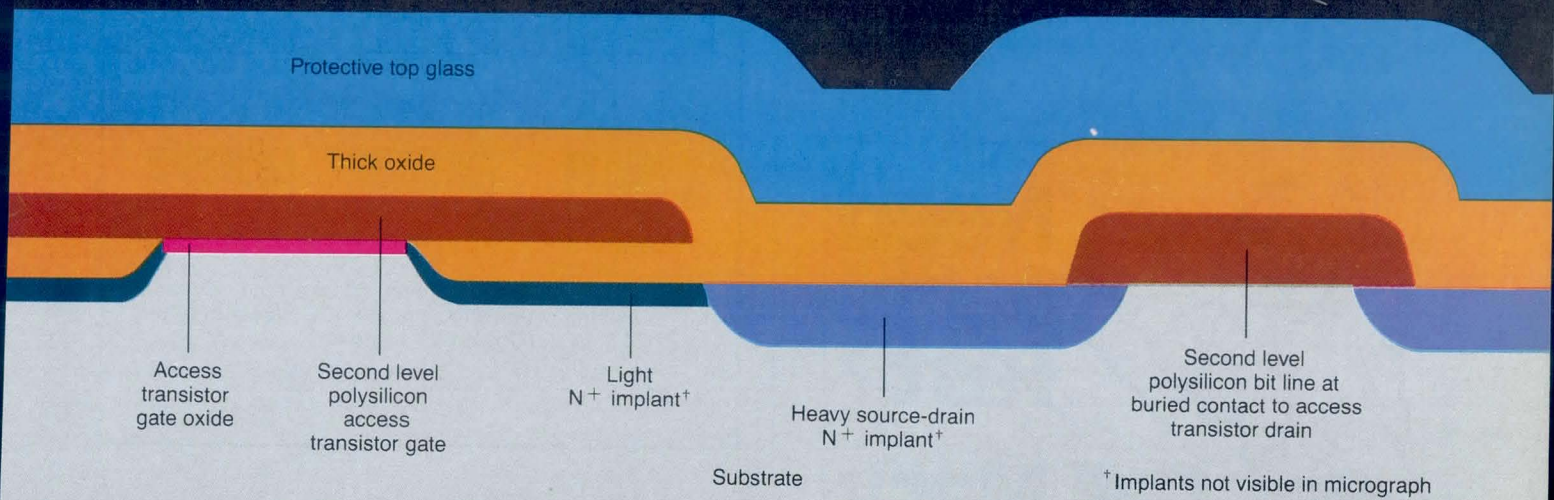

Though diffused bit lines are undeniably correct for our industry-standard MK4116, VLSI geometries precluded their efficient use in the MK4164. Consequently, we needed a new way to maximize the usable signal generated from the smaller area available for storage cells. So we switched to polysilicon bit lines. This switch significantly improved the capacitor-to-total-cell area ratio and resulted in 50% more usable signal to the sense amplifiers than if we had used diffused bit lines with the same layout rules.

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CIRCLE 24 ON INQUIRY CARD

Compatibility with the target machine and its software is offered at the interface of the peripheral device. The method used to transfer the data from the peripheral device to the memory is transparent to software so that the DPS microcomputer, coupled with as many DMA channels as are required, can provide a software compatible, full-speed I/O emulation. Potential configurations are identified and described below.

Low Cost I/O Capability—The lowest possible cost I/O configuration is shown in Fig 2 (a). The DPS CPU, operating in a timesharing mode, may be either a mini- or microcomputer, which permits use of the same hardware for CPU and I/O functions. From the standpoint of system design, this configuration is particularly cost effective for systems with low I/O data rates, as it eliminates the need for special hardware to handle the I/O. When operating in the IOC mode, the microcomputer is capable of approximately 120k transfers/s, while the minicomputer can handle 200k transfers/s; these transfers are either word or byte. Since the CPU is being used to handle I/O, I/O operations interfere with the processing capability of the CPU. For example, if a minicomputer CPU were handling a 50k-word/s I/O transfer rate, such as a disc, its processing capability would be reduced by about 25%. However, where there are such high speed devices, DMA capability is typically used, reserving CPU use for I/O control of low speed I/O devices.

The DMA capability afforded by the DPS design is 1.25M words/s. Since the DMA operates fully independently of the CPU, its only interference will be due to bus stealing. For example, in order to transfer 50k words/s, the DMA will steal the IEB for approximately 40 ms, a maximum of 4% interference with the CPU.

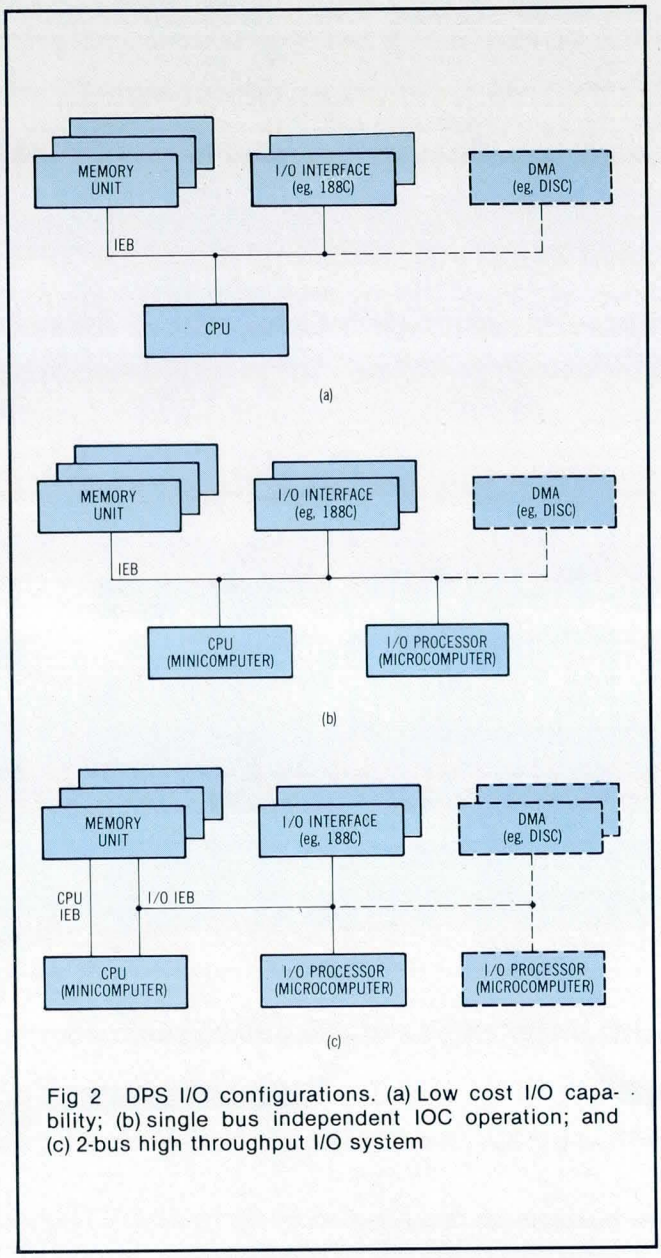

Fig 2 DPS I/O configurations. (a) Low cost I/O capability; (b) single bus independent IOC operation; and (c) 2-bus high throughput I/O system

Single-Bus, Independent IOC Operation—Fig 2(b) identifies a single IEB operation in which the minicomputer operates exclusively as a CPU, while the microcomputer performs as an IOC. If we consider this configuration without DMA and assume a 50k-word transfer rate, the microcomputer will tie up the IEB approximately 5.2% of the time (50k data transfers at 240 ns/transfer, and 50k memory transfers at 800 ns/cycle). If total I/O rates exceed 120k transfers/s, DMA channels or a second IOC may be used.

This particular configuration highlights a unique survivability feature of the DPS computers: the capability for I/Os or DMA channels to be interfaced with both computers, and permit the minicomputer CPU to pick up I/O functions in the event of microcomputer IOC failure.

(continued on page 38)

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CIRCLE 26 ON INQUIRY CARD

Two-Bus, High Throughput I/O Configuration—A dual-IEB computer organization where the CPU and IOC each have independent access to memory is shown in Fig 2(c). The CPU interfaces with its IOC via the I/O IEB, eliminating a special interface. A side benefit to this method of interfacing is that the CPU has access to the I/O IEB and can operate as its own IOC (in a timeshared mode) in the event the IOC fails. This configuration permits the CPU to operate without any interference from I/O operations as long as each of the processors is operating with different memory units.

Since the microcomputer IOC is limited to approximately 120k transfers/s, additional I/O traffic can be accommodated by the introduction of another microcomputer IOC and/or DMA channels. The I/O transfer rate of this configuration is 1.25M words/s, which is limited only by the memory speed, assuming I/O operations are in memory units not currently in use by the CPU.

Fail-Safe/Soft

Fail-safe/soft capability has been discussed previously; key factors are the distribution of the arbitration logic for bus access and the provision for multiple processors on the same bus. Providing both CPU and IOC firmware in all processors allows fail-safe/soft in I/O operations.

Maintainability

Maintainability is a key requirement in military computers. Maintenance is often handled by personnel with little or no technical training. CPU resident microdiagnostics coupled with functional partitioning provides fault isolation to a single failed circuit card for 95% of the failures. Separation of control and data paths within the CPU is the key to the success of this approach. Since a single card, the control card, contains all the microcode storage and sequence control, failure to execute the microdiagnostics pinpoints the problem to the control card. Once the control is determined to be functioning, it can test and isolate faults in the remainder of the node.

Summary

Imposition of a set of system design requirements has resulted in a computer family design that provides emulation of existing military architectures. These proven architectures have then been augmented to provide the necessary features that permit efficient use of these machines within the framework of the defined system.

The fourth and final article in this series will discuss system software.

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2. R. Mauriello, "A Distributed Processing System for Military Applications—Part 2: The Serial Data Bus," *Computer Design*, Oct 1980, pp 14-36

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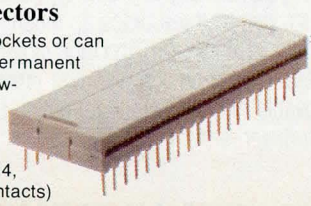

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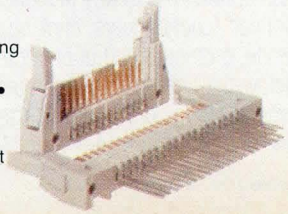

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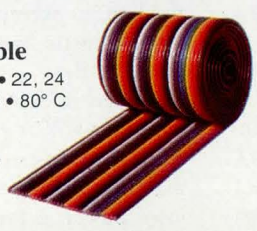
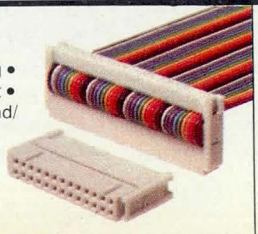


Laminated Flat Cable

• .050" (1.27mm) spacing • 10 to 64 conductors, 28 AWG stranded • 105° C temperature rating • 300V voltage rating • UL style number 2651

Socket Connectors

• .100" (2.54mm) spacing • Double cantilever contact • 10 to 60 pins • Closed-end/through-end • Dual-beamed contacts • Polycarbonate strain relief

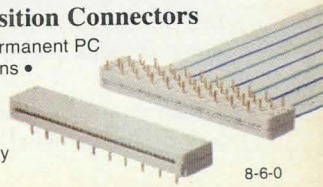


Low-profile Socket Connectors

• .100" (2.54mm) contact spacing • Double-cantilever contact • Bottom-entry contact • Dual-beamed contacts • Many diversifications (10 to 60 pins)

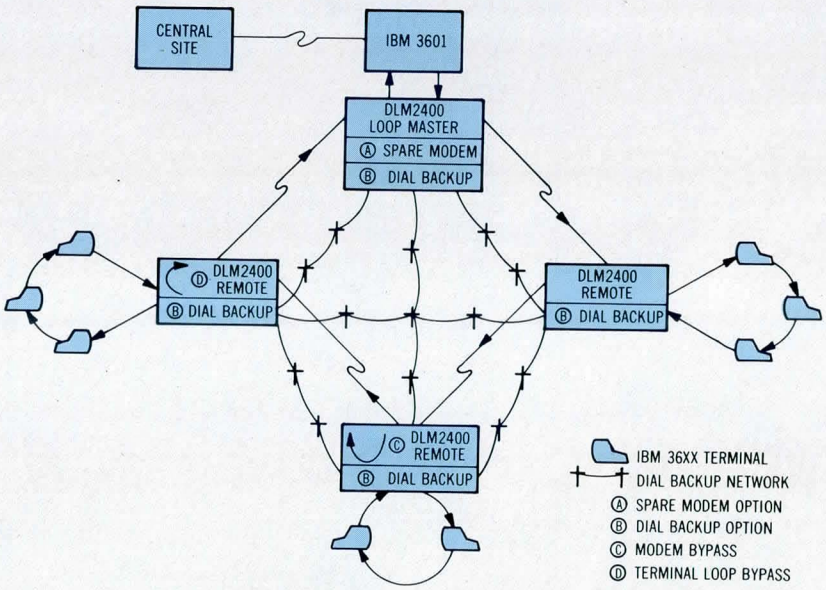
P.C.B. Transition Connectors

• For reliable permanent PC board connections • 1.6 mm (1/16") standard thickness of PC board • Many diversifications (10 to 60 pins)



8-6-0

Modems Provide for Network Monitoring and Restoral in Financial Loop Data Networks



Network control and restoral features. With network control, spare modem can be brought online to restore data communications. With dial backup option, backup numbers are downline loaded from network control console and incoming calls are answered automatically, enabling dial backup between any two network sites

Operational in any IBM 3600 finance communications system, DLM1200 (1200-bit/s) and DLM2400 (2400-bit/s) diagnostic loop modems offer a full range of network monitoring and restoral services. The devices, from Intertel, 6 Shattuck Rd, Andover, MA 01810, work in conjunction with the company's EMS-One network control system and provide the link between 3600 controllers and any number of remote terminal loops.

IBM 3600 networks operate with a unique bipolar signal structure using a simplex transmission protocol. Data are transmitted and received over a single serial path or loop that includes all network elements. The serial configuration makes the network vulnerable to single-component failures. Controlled from a central site, the modems provide network monitoring, testing, bypassing of failed components, and restoration of network capabilities.

The network control system, in automatic preventive maintenance mode, automatically performs network tests during offline times and locates and reports trends in network performance. An online automatic monitoring mode continuously monitors remote sites for trouble without affecting ongoing data communications. Any change in critical parameters generates a central site alarm signal and indicates which parameter is changing. A third or manual mode allows a central site operator to isolate a network fault to a data channel, modem, or terminal.

Diagnostic modems allow any network modem or terminal loop to be bypassed in case of equipment failure. The unit will regenerate the bypassed signals to ensure continuance of normal network operations. If a modem loses power, a fail-safe connection ties analog input and output lines together to provide a continuing analog path.

The modem chassis is prewired for internal spare modem and dial backup options. The remotely controlled spare modem restores communications should the primary modem fail. Dial backup option allows an operator to remotely establish an alternate 2- or 4-wire dial network link in case of failure of the private line. Dial backup is possible between any two remote or central network sites, attended or unattended. Because the device is FCC-registered for direct connection to the DDD network, external DAAs are not required.

The IBM terminal interface has serial, simplex data format, bipolar signal structure, and transmit jack and receive plug connectors. Leased line interface is 600 Ω ±10%, balanced, with a 4-wire terminal strip connector. Dial backup interface is via 2- or 4-wire RJ11C permissive mode connector. Transmit level is 0, −4, −8, or −13 dBm, strap-selectable; receive level, −4 to −31 dBm on leased lines, and −12 to −39 dBm on dial-up lines. FSK modulation is used at 1200, and PSK at 2400 bits/s. The modems are available in either standalone or rack-mount versions. Circle 321 on Inquiry Card

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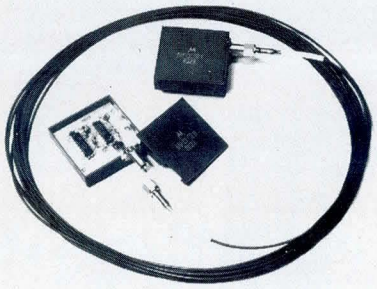
CIRCLE 30 ON INQUIRY CARD

COMMUNICATION CHANNEL

TTL-Compatible Link Kit Evaluates Fiber Optic Techniques



Fiber optic evaluation link. Pulse bipolar encoded transmitter (top) and receiver/decoder, shown with cover removed, operate from single 5-V power supplies. Module dimensions are 2.0 x 2.0 x 0.45″ (5.1 x 5.1 x 1.14 cm)

Prepared for systems designers who wish to familiarize themselves with fiber optic technology, components, and techniques for long distance optical data transmission, the Link II™ evaluation kit includes TTL transmitter and receiver modules capable of data transmission over a simplex link of more than 1-km length.

The kit is available from Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036. It is composed of MFOL02T transmitter module, MFOL02R receiver module, and 10-m Du Pont Pifax PIR 140 fiber optic cable. The cable is preterminated with AMP Optimate connectors for efficient die to fiber coupling. The single-fiber cable has a 368-μm core diameter with attenuation of 900 dB/km at 900 nm and 500 dB/km at 820 nm.

Both modules have removable covers to allow designer experimentation. Accessible circuitry in the transmitter consists of a current amplifier and driver, and in the receiver an op amp and comparator. Total power at transmitter output port is typically 70 μW at 900 nm wavelength. Receiver input sensitivity is 0.01 μW. Both modules require 5 Vdc. Link bandwidth is 200 kHz.

The kit includes component data sheets and applications literature that provides theory of link operation and basic fiber optics concepts.

Circle 322 on Inquiry Card

Device Saves Coax Costs in Local Cable Distribution Systems

Useful in configurations where large amounts of coaxial cable are used, where distances greater than 5000 ft (1525 m) are required, or where only twisted wire circuits are available, COAX ELIMINATOR™ can reduce dependence on coax cable for connecting its displays to a controller, according to Lee Data Corp, 10206 Crosstown Circle, Minneapolis, MN 55344. The product is available in three models, and widens the capabilities of the company's series 300 family of distributed data processing systems. It allows connection of up to 8 LDC displays or printers to one coax cable or 4-wire unloaded metallic circuit from any LDC 3274 compatible controller.

The coaxial unit has one coaxial input and eight coaxial output channels. It replaces the conventional "cable for each display" configuration with a single coaxial cable running to a group of up to eight displays, through the unit, and fanning out to each display via shorter coaxial cables. The design allows chaining of coaxial units every 2500 ft (762 m) so that total running length from controller to display is limited only by accessibility to power and the size of the customer facility.

A 4-wire unit comes in two models. A single-channel model can be used as one coaxial input and one 4-wire channel output or vice versa. An 8-channel model has one 4-wire input and eight coaxial output channels. It allows replacement of multiple coaxial cables with a 4-wire circuit going to a group of up to eight displays and fanning out from the unit to each display using short lengths of coaxial cable. The 4-wire units can also be chained.

The coaxial eliminator is predicated on the company's interactive display systems that are based on multiprocessor architecture. Displays and printers are all addressable so that multiple stations can share the same line to the controller. The terminals transmit data to and receive data from their controller using a data link protocol that provides required station addressing as well as high level error recovery. The 500k-bit/s data transmission rate between controller and stations allows up to eight stations on each line without performance degradation.

Circle 323 on Inquiry Card

Using bipolar PROMs? Check out the Fast Cat™ ROM. Speed is only half the story.

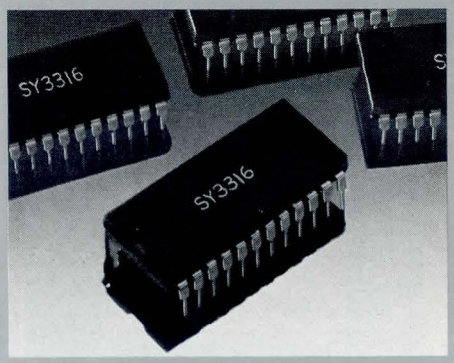
The bipolar PROM market will never be the same. Introducing the SY3316 Fast Cat™ ROM. It's not only fast—80nsec—it also slashes costs wherever high performance, large bit storage and simple interface are important design considerations.

Synertek's engineering team designed the Fast Cat™ ROM that way. Now you can make a quick, cost-effective move from bipolar PROM prototyping into volume production—without costly PC board redesign. The SY3316 can do it because it's directly pin compatible with industry standard 16K bipolar PROMs.

There's even more to this cat. Like a single +5V supply, full input/output TTL compatibility, fully static circuitry, asynchronous operation, industry standard 2048x8 organization, three mask programmable chip selects and three-state outputs to facilitate system expansion.

We make ROMs our business. So that you get total commitment to servicing your ROM needs. With wafers waiting at contact mask, we can meet fast delivery requirements—just four weeks for your SY3316 prototype. That's flexibility. Already at work for you now. And we back it all up with high performance scaled N-channel MOS technology.

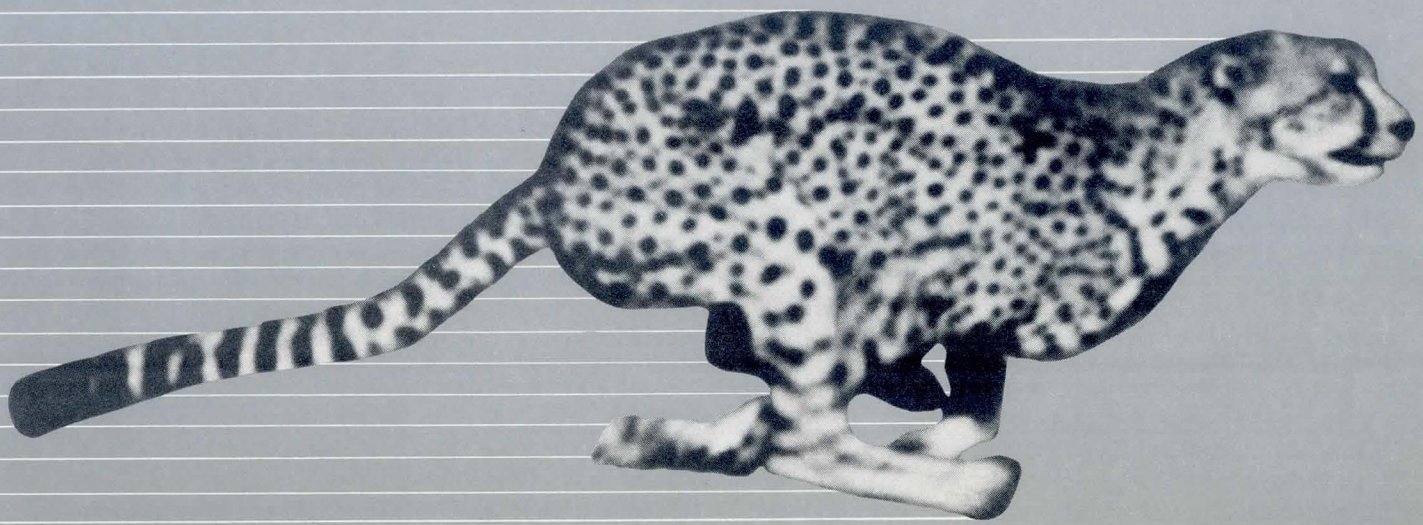
Need 8K bipolar PROMs? Then check out the SY3308 8K ROM, another fast member—at 70nsec—of the Fast Cat™ ROM family. And fully compatible with industry standard 1Kx8 bipolar PROMs. We've got a family of cats that's only going to get bigger. And better. Get a jump on the competition. And go with the MOS company. Go with Synertek. Call your area Synertek distributor now.



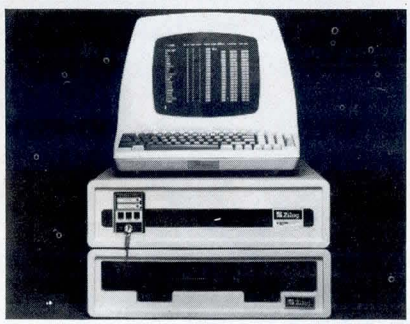
SYNERTEK

3001 Stender Way P.O. Box 552
Santa Clara, California 95052
(408) 988-5600
TWX: 910-338-0135

SY3316 80nsec



System Distributes Hardware and Software Development Stations



Z-Lab 80 configuration. Z-Lab concept links hardware and software development stations along a local computer network

Using the capabilities of the company's local computer network architecture (*Computer Design*, Aug 1980, p 39), Z-LAB can physically distribute hardware and software development stations yet keep them as part of an integrated system. The concept, announced by Zilog, 10340 Bubb Rd, Cupertino, CA 95014, is designed for those developing products based on Z8™, Z80®, and Z8000™ microprocessors.

The concept is implemented using Z-LAB 80 program development station, SDS 2/01 shared data station, and NST 2/01 network station transceiver. The program development station is based on the 4-MHz Z80 CPU, and includes the RIO operating system, 64k-byte RAM, 4M bytes double-sided, double-density floppy disc storage, and RS-232-C ports for a CRT terminal, printer, or other peripherals. Z80 and Z8000 software development packages, including PLZ high level language support, are also furnished. A Z8 package is available as an option. All three packages offer macroassembler support. Hardware development packages are available.

Z-Net local network architecture comprises a single-channel, packet-switched local computer network with fully distributed control. Development stations are linked by a common coaxial cable up to 2 km in length, and are connected to the cable by transceiver unit NST 2/01. The shared data station provides a common 10M- to 40M-byte data base for the various development stations along the network.

The concept allows physical separation of development activities for hardware, software, and hardware/software integration. The local computer network supports multiple users and allows incremental growth in system complexity and size. Addition of a 16-bit Z8000-based program development station is planned for the future.

Circle 324 on Inquiry Card

Coaxial Cable Modem Transmits to 1.544M Baud Without Adjustments

No adjustments are required for model 30-0080 modem to transmit and receive high frequency synchronous clock and data on coaxial cable at rates from dc to 1.544M baud. The device, from Computrol Corp, 15 Ethan Allen Hwy, Ridgefield, CT 06877, can transmit over distances of up to 27,000 ft (8230 m) without amplifiers or repeaters.

The unit uses multilevel FSK modulation at high carrier frequencies for transmitting clock and data over a single cable. Type of modulation and filtering effectively reject emi and rfi noise often generated in industrial and commercial environments. Data and clock are digitally reconstructed at the receiver with zero phase shift and no relative jitter. Typical bit error rates are less than 10^{-12}, with an S/N ratio of 20 dB.

Many devices may be connected at any point on the cable without gain adjustments because of the modem's high dynamic range. A gated carrier half-duplex mode allows multidrop party lining of devices on a single cable. Coupling is through a T connector. Full-duplex operation requires two cables. The modem is completely transparent to data. Since modem receiver circuits detect the very first message bit, the message structure requires no preamble. The only control signal is a gate that is turned on for the duration of the carrier's transmission.

The device enables implementation of a high speed data highway for processor to processor communication, remote multiplexing of distributed I/O functions, terminal and computer networking, and transfer of large data packets in local area networks.

The modem is packaged on a 3 x 4″ (7.6 x 10.2-cm) PC card with pins at the bottom for mounting on the motherboard. Low profile permits mounting on boards that are on 0.5″ (1.3-cm) centers in a card cage.

Circle 325 on Inquiry Card

Basic Ethernet Patents Made Available to Interested Organizations

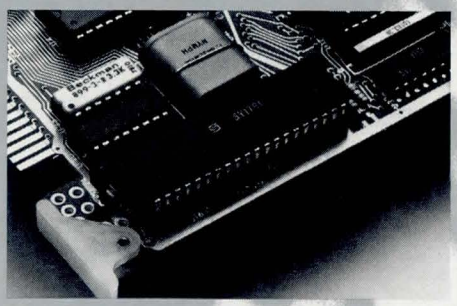
U.S. Patent 4,063,220, basic patent for the Ethernet local communications network, has been made available to all parties by Xerox Corp for a one-time payment of $1000 per license. The single payment covers any number of local area network products of the licensed companies. All worldwide counterparts of the patent are also available for license. The Japanese counterpart is available for license from Fuji Xerox, and all other non-U.S. counterparts are included in the basic Xerox license.

A second Ethernet patent, USP 4,099,024, covering an Ethernet repeater, is also available for license on similar terms. The repeaters reinforce digital information signals as they move over long distances on the Ethernet cable.

Ethernet specifications were developed by representatives of Digital Equipment Corp, Intel Corp, and Xerox Corp to help promote communications compatibility among different kinds of computers, peripherals, data terminals, and office equipment.

Xerox standard patent license agreements are being mailed to all previous inquirers about Ethernet licenses. New license inquiries should be directed to: Manager of Licensing, Xerox Corp, Stamford, CT 06904. Inquiries on the Japanese counterpart application should be sent to: Manager, Legal and General Affairs Dept, Fuji Xerox Co Ltd, 3-5 Akasaka 3-Chome, Minato-ku, Tokyo 107, Japan.

Synertek's 1791 Floppy Disk Controller can take the heat.



Data and program storage is critical. The last thing you need is to see it go up in smoke. Or even know it might. Enter the Synertek 1791 Floppy Disk Controller, the controller that can take the heat. And cool the cost of interfacing floppy disk drives to EDP systems, word processors, CRT terminals, small business computers, and more.

A single 5V power supply (their's needs two) leads a list of solid features you not only need but should expect in a floppy disk controller. Performance to specifications over the entire 0°-70°C range—with no fall out. Accommodates IBM 3740 and System 34 formats. Handles 5" and 8" floppy disks. Double-buffered data transfers. Plug compatible to the WD1791-02. Single or double-density recording formats. Plus multiple options, like the SY1793-02 with non-inverting data bus and our SY6591 which is 6500/6800 bus compatible.

There's solid support all around our SY1791, too, with a full product line of RAMs, ROMs, microprocessors and microprocessor peripherals. All ready and waiting. All in high volume production.

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Title _____

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Modem Achieves 14,400-Bit/s Transmission In Point to Point Networks

Said to be the only commercially available modem to operate beyond 9600 bits/s over D1-conditioned 3002 voiceband telephone lines, the Microprocessor 14400 from Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33541, uses an advanced modulation technique* to achieve a 14.4k-bit/s rate over these channels. It was designed for applications where 9600 bits/s is insufficient or where users are currently leasing multiple lower speed point to point lines between common sites.

Application is for full- or half-duplex, synchronous, binary serial data transmission at rates of 14.4k, 12k, or 9.6k bits/s. It is V.29 compatible at the latter rate. Various data rate combinations are available with an optional 6-port multiplexer; another option is a 100-bit/s forward signaling channel. Digital interface is RS-232-C/V.24, with a MIL-STD-188 interface as an option. Channel equalization is by adaptive digital transversal technique. Normalized S/N ratio is 1×10^{-5} at 27 dB. Initialization time is less than 1 s.

The modem uses two microprocessors, one for transmit and the other for receive functions. The microprocessor program performs all signal processing tasks including automatic adaptive equalization, filtering, demodulation, and data derandomizing. The program optimizes performance by continuously adapting to transmission line characteristics. The device is designed to communicate with the company's Analysis network management systems over an out-of-band noninterfering diagnostic channel.

*Patent applied for

Circle 326 on Inquiry Card

Async Communication Interface Adapter Has Integral Baud Rate Generator

An onchip programmable baud rate generator allows R6551 asynchronous communication interface adapter (ACIA) to transmit variable word lengths at user selectable baud rates. The ACIA is pin compatible with Motorola MC6850 and provides an RS-232 type interface between 8-bit microprocessor based systems and serial communication data sets and modems. The device is from Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92803.

The baud rate generator allows the ACIA to transmit 15 program selectable rates from 50 to 19.2k baud. The interface adapter can receive at either the transmit rate or at 16 times an external clock rate. It has programmable word lengths of 5, 6, 7, or 8 bits, parity bit generation and detection, and a number of bit stops.

The only external support needed is a crystal. The device replaces about 10 TTL components that would otherwise be required. It is designed to work with other 8-bit microprocessors and is directly compatible with the 6500/6800 bus. A control register and separate command register enable the CPU to select the ACIA's operating modes and data checks.

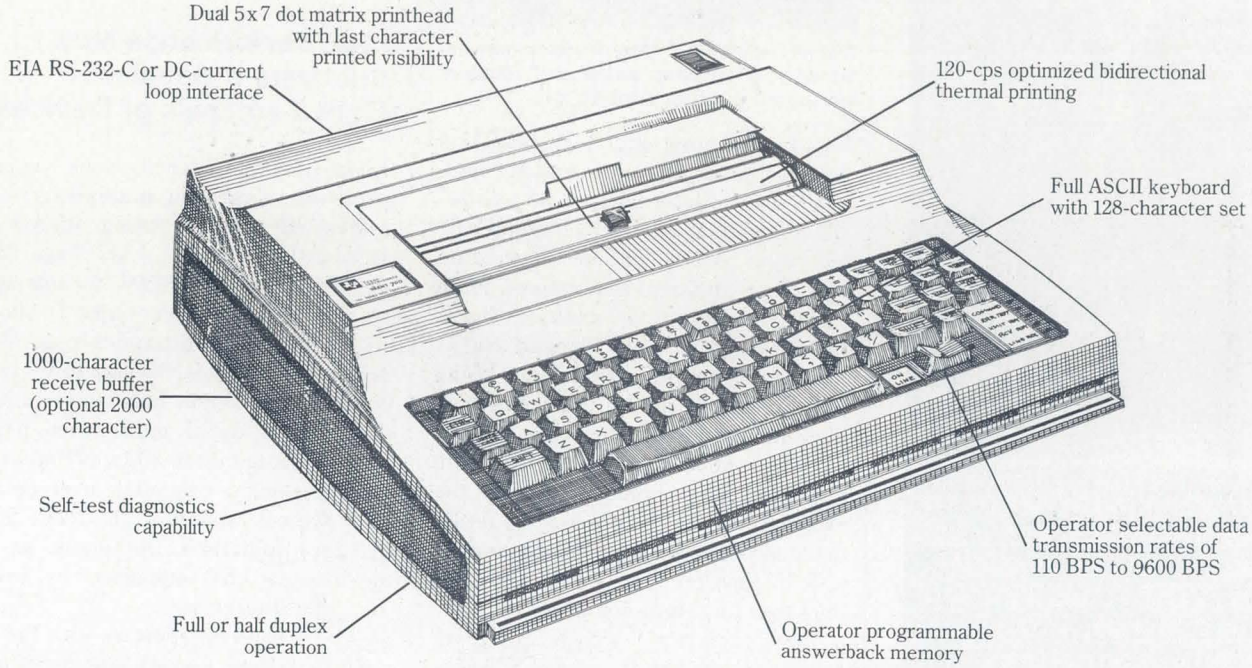
Among other features are full-duplex operation with buffered receiver and transmitter, data set/modem control functions, programmable interrupt control, and selectable serial echo mode. The ACIA, packaged in a 28-pin plastic or ceramic DIP, is designed for use in computer terminals and data acquisition.

Circle 327 on Inquiry Card

The Task Master.

783 KSR

Keyboard Send-Receive Data Terminal



Ideal for commercial applications, TI's *Silent 700** Model 783 KSR Data Terminal can master your workload with high-quality, efficient thermal printing. Offering a variety of user-oriented standard features and options, the virtually silent 783 KSR takes less work space while it maximizes printing throughput. That's why the versatile 783 KSR was designed to handle your most demanding printing tasks.

TI is dedicated to producing quality, innovative products like the 783 KSR Data Terminal. TI's hundreds of thousands of data terminals shipped worldwide are backed by the technology and reliability that come from 50 years of experience, and are supported by our worldwide organization of factory-trained sales and service representatives.

For more information on the 783 KSR, contact the TI sales office nearest you or write Texas Instruments Incorporated, P.O. Box 1444, M/S 7884, Houston, Texas 77001, or phone (713) 373-1050. In Europe, write Texas Instruments Incorporated, M/S 74, B.P. 5, Villeneuve-Loubet, 06270, France.

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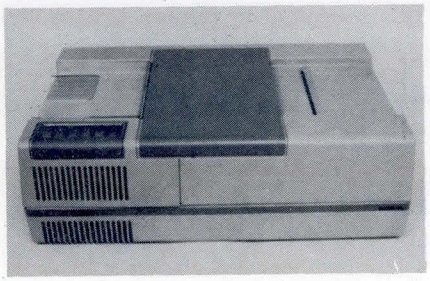
TEXAS INSTRUMENTS

INCORPORATED

CIRCLE 34 ON INQUIRY CARD

Group 2 Facsimile Terminal Uses Plain Paper Recording, Ink Jet Printing



Ink jet facsimile printer. It uses conventional roll-fed plain paper and requires no toners or other printing aids

Capable of unattended transmission over leased or dial-up telephone lines in a 2- or 3-min format, the HF 2050 facsimile terminal uses conventional roll-fed paper instead of specially treated types for significant cost savings. Plain paper recording is enabled by a sophisticated drop on demand ink jet printing technique that includes 12 ink jets. Six closely-spaced jets are used in the 3-min mode, and the other six, not so closely spaced, are used for 2-min operation. This enables six lines of the original to be reproduced simultaneously. Scanning/recording density is 3.85 lines/mm for 3-min, and 3.08 lines/mm for 2-min operation.

The terminal, available from Siemens Corp, 186 Wood Ave S, Iselin, NJ 08830, is compatible with all CCITT Group 2 devices. Unattended operation capability allows for savings in toll rates during evening and nighttime hours. The machine starts telecopying automatically if the calling telephone is not answered within 10 s. Received copy is automatically cut from the roll in 8.5 x 11″ (21.6 x 28-cm) sheets.

In the transmit mode, push buttons allow selection of 2- or 3-min operation, and also selection of one-quarter, one-half, or one-third page transmission if desired. Scanning is optoelectric at 3 lines/scanning operation in each direction of movement. Modulation is amplitude/phase/vestigial sideband, and carrier frequency is 2100 Hz. The −6 dB send level can be adjusted to other values; input sensitivity is greater than −46 dBm.

Available options include a stacking device for automatic transmission of up to 25 pages, a synthetic voice answering device, counters for registering number of transmitted/received pages, and an auxiliary communications socket.

Circle 328 on Inquiry Card

High Performance MUX Subsystem Handles Eight Terminals or Devices

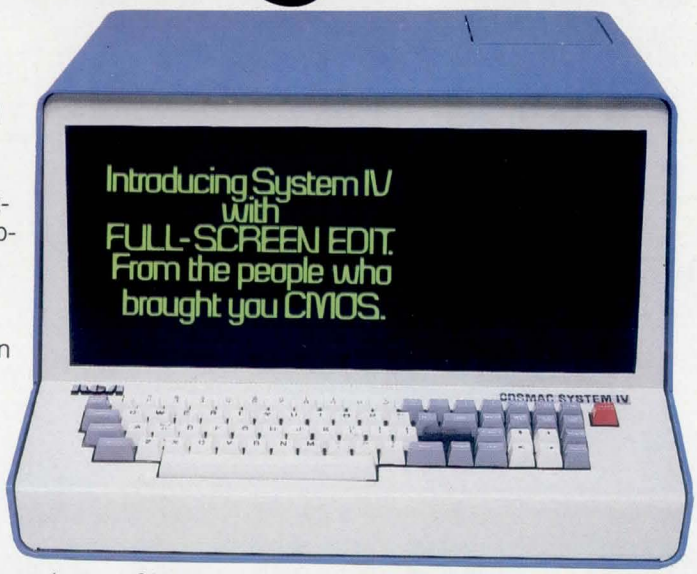
Eight-channel asynchronous microprocessor controlled multiplexer subsystem HP 12792A is being offered by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, for use with its HP 1000 series computers. It allows as many as eight terminals or electrically compatible devices to be connected to a single multiplexer interface. An optional multiplexer panel can be located up to 300 ft (91 m) away from the main computer, overcoming the typical standard RS-232-C 50-ft (15.2-m) limitation. As many as 62 devices can be supported by using multiple interfaces.

The subsystem operates with the HP 1000 M-, E-, and F-series processors and systems. Operating system RTE-IVB supports program development and execution, and memory based operating system RTE-MIII supports application program execution. Both operating systems support multiple multiplexer subsystems.

Each full-duplex channel is separately buffered. I/O processing time is reduced by direct memory access (DMA) control of all communications from interface memory to host computer backplane. If a DMA channel is currently available, I/O requests to or from the host are handled under DMA control; otherwise the request is handled on a word-by-word basis. This reduces typical computer overhead to about 3%/channel at 9600 baud for long continuous block transfers.

Circle 329 on Inquiry Card

Now CMOS cuts your design time.



Now there's another good reason to switch to CMOS.

COSMAC System IV: The complete 1802 hardware, software Microprocessor Development System.

Full-screen editing. The COSMAC System IV features an integral CRT display screen with built-in "true" full-screen editing.

Program entries and corrections appear instantly on the screen for fast, easy program editing.

The 12-inch integral CRT displays 80 characters per line and up to 24 lines. With attractive green phosphor for reduced eye fatigue.

New, high performance macro-assembler. Our new ASM8, level II macroassembler provides much faster assembly time. We've added cross-reference listings and "verbal" error messages. Plus numerous other enhancements for fast, easy operation.

ASCII keyboard. A fully-encoded ASCII keyboard contains 72 ASCII keys. Plus 14 dedicated full-screen edit keys to save you the trouble of typing control words or memorizing mnemonics.

Other on-board hardware includes: 60K bytes of user accessible CMOS RAM. Dual drive floppy disk. A built-in PROM programmer and line printer interface. And the RCA exclusive CDOS file-management operating system.

Go anywhere Micromonitor. Also included in the package is our widely acclaimed Micromonitor, the portable, in-circuit emulator. A complete diagnostic and design tool, capable of real-time, in-circuit hardware and software debugging. Plus our MOPS (Micromonitor OPerating System) software which allows complete software interrogation of the system under test.

Optional aids. For hard copy, add our 340 character-per-second, 132 column matrix printer, complete with built-in self test and diagnostics display.

Choose from three high-level languages: BASIC 1, BASIC 2, or PLM-1800.

If you already own our 005 or 007 system, move up to full-screen editing with our smart CRT terminal upgrade (CDP18S040).

"Total design support" from the CMOS people.

The $12,000* total System IV price also includes total design support from the people who brought you the 1802.

Plus a copy of "Welcome to the World of RCA COSMAC," a demonstration diskette to introduce you to your new COSMAC System IV. And a free one-year subscription to the RCA software update service.

For more information or a System IV (CDP18S008) demonstration, contact your local RCA Solid State sales office or distributor. Or contact RCA Solid State Headquarters in Somerville, New Jersey. Brussels, Belgium. Hong Kong. Sao Paulo, Brazil. **Or call Microsystems Marketing toll-free (800) 526-3862.**

*optional resale price

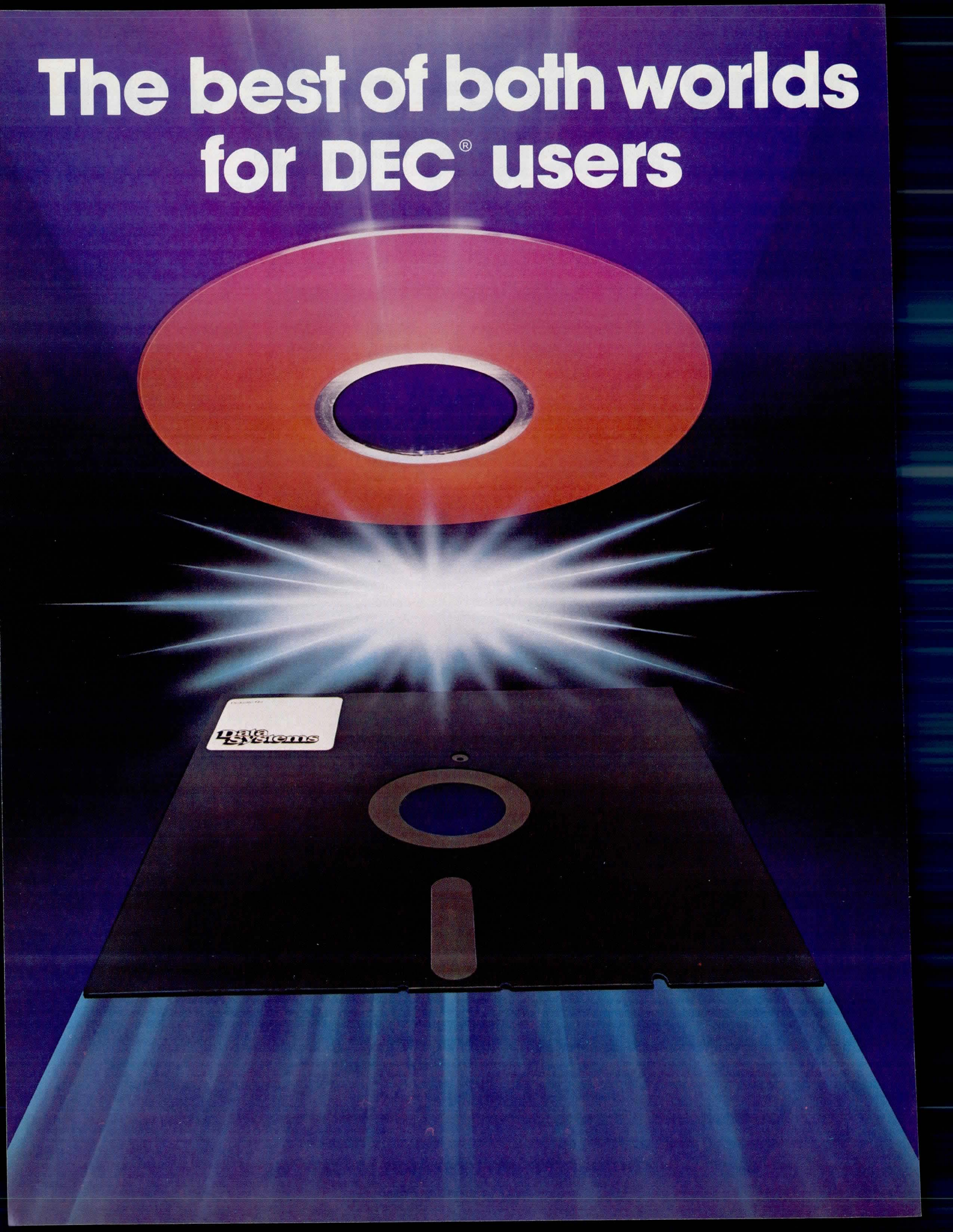
Total hardware, software development system $12,000.*

Another reason to switch to CMOS.

RCA

CIRCLE 36 ON INQUIRY CARD

The best of both worlds for DEC® users



Data Systems Design's DSD 880

Introducing the DSD 880 — A DEC-compatible disk system combining eight-inch winchester and floppy disks

For DEC users who need more capacity and performance than an RX02, the DSD 880 now offers a more cost effective alternative than a dual RL01. Consider these benefits offered by the DSD 880:

- significantly lower initial and total life-cycle costs
- the reliability of a winchester, with 7.8 Mbytes, emulating RL01
- the removability of a floppy disk, with 1 Mbyte, emulating RX02
- valuable saving in rack space (5¼" vs. 21" for dual RL01)
- unique "hyperdiagnostics" enabling fast and easy trouble-shooting to the modular level
- built-in bootstrap eliminating the need for an expensive DEC bootstrap board and saving a backplane slot
- one half-quad backplane slot vs. two quad boards for the RLV11
- versatile interface card for easy integration with any LSI-11 backplane, unlike DEC's RLV11 interface that needs a special backplane and cannot be used with the VT 103 terminal

Compare for yourself and see why nothing compares to the DSD 880.

Data Systems

The Intelligent Alternative to DEC Disk Systems

To get more information on the DSD 880 call or write:

CORPORATE HEADQUARTERS:
2241 Lundy Avenue
San Jose, CA 95131
TEL: (408) 727-9353
TWX: 910 338-0249

WESTERN REGION SALES:
2560 Mission College Blvd., Suite 108
Santa Clara, CA 95051
TEL: (408) 727-3163
TWX: 910 338-0249

EASTERN REGION SALES:
51 Morgan Drive
Norwood, MA 02062
TEL: (617) 769-7620
TWX: 710 336-0120

INTERNATIONAL SALES: Australia, Melbourne (03) 543-2077, Sydney (02) 848-8533; Canada (416) 625-1907; Denmark 01/83 34 00; Finland 90/88 50 11; France 03/956 81 42; Israel 03/ 298783; Italy 02/ 4047648; Japan, Osaka (06) 323-1707, Tokyo (03) 345-1411; Netherlands 020/45 87 55; New Zealand 4-693-008; Norway 02/78 94 60; Sweden 08/38 03 70; Switzerland 01/730 48 48; United Kingdom 01/207-1717; West Germany and Austria (089) 1204-0.

300-Baud Modem Replaces Acoustic Coupler—Direct connect signal performance with acoustic coupler convenience is permitted by Bell 103A-compatible modem HS2500. The device, available from Komda Corp, 2500 Central Ave, Boulder, CO 80301, is typically installed under a telephone. The handset is plugged into the modem, which in turn is plugged into the telephone instrument via modular jacks. Transmission mode is selected by a voice/data switch mounted on the front of the device. Phase coherent FSK modulation is used and operation is asynchronous. Signal compensation operates automatically over a 32-dB range. The modem comes with RS-232-C interface as standard; TTY interface is available on special order. Options include originate/answer and half/full-duplex modes.

Circle 330 on Inquiry Card

Serial Synchronous Data Communications Interface Developed for LSI-11 Family—A double-buffered, program-interrupt interface that couples an LSI-11 bus with a serial synchronous modem using RS-232-C or RS-423 interface standards has been introduced by Digital Equipment Corp, Maynard, MA 01754. The DPV11 interface can be used with any of the company's microcomputer based products that use the LSI-11 bus, including the PDP-11/03 and -11/23 computers. The interface can be used in both full- and half-duplex modes. Software dependent transmission speed can be as high as 56k bytes/s. Protocols for the device are DDCMP, HDLC, SDLC, and Bisync. Users may also develop X.25 links between LSI-11 based systems and public packet-switched networks.

Circle 331 on Inquiry Card

Joint Data Communications Venture Formed—The formation of a joint venture in the U.S.-Canada data communications market has been announced by SESA sa, Paris, France, and Honeywell Inc, Minneapolis, Minn. SESA, a software and telecommunications company, has installed major networks in Europe, including the TRANSPAC packet-switched network of the French PTT, and the EURONET network in the nine common market countries and Switzerland. The company also has orders for its DPS 25 packet-switching systems from the European Railroad Association, the French Railroad, and the European Space Agency. Honeywell, a computer and controls company, will contribute its resources to SESA technology to pursue the growing data network market in the U.S. and Canada. The new company, SESA-Honeywell Communications, Inc, owned 51% by SESA and 49% by Honeywell, is headquartered in Herndon, Va. Jack Pendray, former head of SESA's U.S. operations, has been named president.

Joint Effort of Satellite Business Communications Carriers and CATV Operators Predicted—The use of cable TV systems to distribute digital business communications information within America's cities will become a reality in the near future, according to a forecast by Sidney Topol, chairman and president of Scientific-Atlanta, Inc, 3845 Pleasantdale Rd, Atlanta, GA 30340. Mr Topol said that in many cities the cable operators will encourage the colocation of business satellite earth stations and CATV entertainment antenna sites, where the intracity cable distribution system starts. Since the CATV coaxial cable in many instances passes close to numerous offices, factories, and computer facilities, ..."this has the makings of a strong interest in joint efforts by the two groups for an intracity distribution system...it is a natural way of advancing the emerging business communications systems by the cooperative use of the 'wired cities' concept of the cable TV industry." Mr Topol's comments were made recently on "The Kagan Report," a live, nationally televised satellite program. □

AMERICAN OEM USERS WELCOME OLIVETTI OPE

Olivetti created a new company fully committed to the OEM market: Olivetti OPE Peripheral Equipment.

OPE is:
technology, know-how and quality;
the benefits of over 70 years' experience of the parent company.

OPE is:
200 highly skilled engineers in R & D;
1,500 highly trained production people;
430,560 square feet of plant space.

OPE is:
daisy wheel printers;
dot matrix printers;
thermal printers;
printing mechanisms;
8″ flexible disk drives;
5¼″ flexible disk drives;
8″ Winchester hard disk drives;
5¼″ Winchester hard disk drives.

OPE's commitment to the OEM market for the 80's: to service you with the best products at the best prices.

Good reasons why American OEM users welcome Olivetti OPE.

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Olivetti OPE
Elmsford, New York 10523/ Tel. (914) 592-2864
Olivetti OPE, S. Bernardo d'Ivrea (TO) Italy

CIRCLE 39 ON INQUIRY CARD

32-Bit Virtual Memory Computer Based on LSI Gate Array Technology

Second member of the 32-bit virtual memory family, from Digital Equipment Corp, Maynard, MA 01754, the VAX-11/750 uses custom gate array technology to achieve 60% of the 11/780's performance at 40% of its CPU price. Implemented using low power bipolar Schottky hardware logic, with 90% in custom LSI gate arrays, the CPU contains a total of 55 chips each with 488 logic gates. High component density results in a two-thirds reduction in printed circuit board space, permitting use of smaller cabinets, lower cooling requirements, and greater reliability.

System features include up to 2M bytes of ECC (Error Correction Code) MOS main memory; 4k-byte integral cache memory; cartridge tape drive for software updates, diagnostics, or auxiliary data storage; an integral UNIBUS interface for terminals, serial devices, and medium speed peripherals; and up to three optional MASSBUS adapters for as many as 24 high speed disc and tape units. Many features of the larger VAX-11/780 are provided such as 4.3G bytes of virtual address space, 2G-byte maximum program size, 16 32-bit general registers, 32 interrupt priority levels (16 each for hardware and software), and 9 addressing modes and 4 hierarchical protection modes, each with read/write access control. Bipolar circuit technology enables switching times as low as 5 ns per gate, and the use of cache memory yields an effective memory cycle time of 400 ns for 32 bits of information.

Options include a writable user control store of 1k 80-bit words, for special, user defined functions, and a memory battery backup that will sustain 2M bytes of memory for more than 10 min. Provision also exists for field installation of an optional floating point accelerator, expected to be announced within a year.

Extensive reliability and maintainability features are incorporated in both design and packaging. Gate array technology provides component reliability more than four times that of equivalent ICs because fewer discrete components and connections are required.

Virtual memory VAX-11/750 computer from Digital Equipment is a powerful 32-bit system that uses advanced LSI circuit technology to achieve low price and compactness. System allows use of programs up to 2G-bytes, has 2M-byte main memory potential, and uses instruction set of larger -11/780

Upon power-up, the system automatically initiates a diagnostic run to verify hardware functions. The operating system automatically maintains consistency and error checks during data transfer operations. Main memory uses a 7-bit error correction code, enabling it to correct all single-bit errors and detect all double-bit errors. The system accommodates an optional module for remote computerized diagnosis, through which problem diagnosis, performance assessment, and preventive maintenance checks can be run remotely by engineers at diagnosis centers. System packaging, outwardly compact but well-spaced inside, allows easy access by field service engineers.

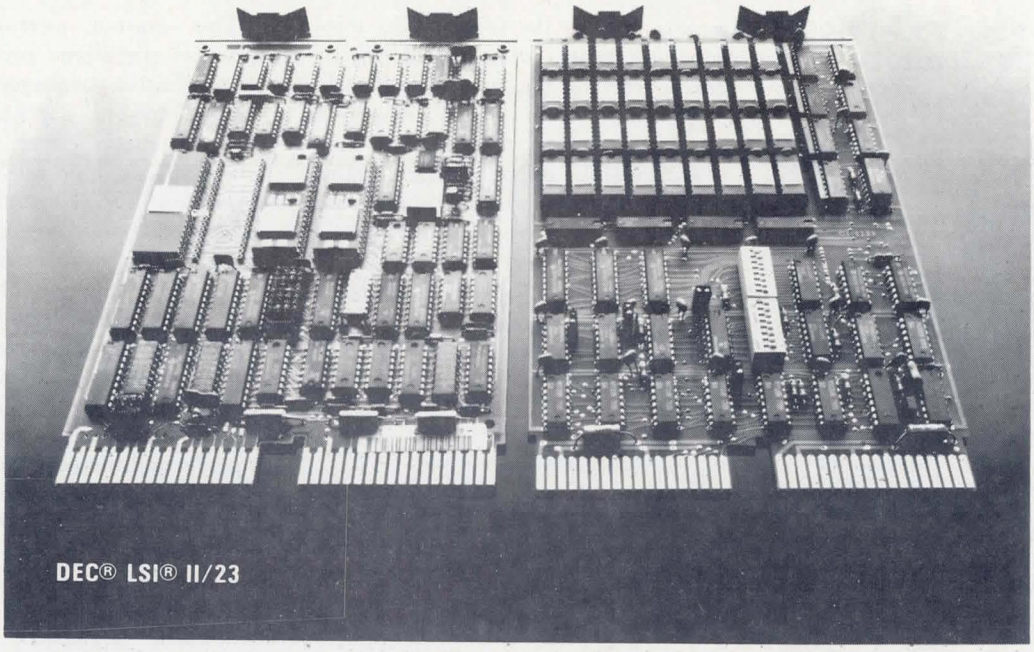
The 11/750 is completely software compatible with the 11/780. Both use the same 240-instruction set and the VAX/VMS virtual memory operating system. Both run all 32-bit VAX-11 high level languages, assembly language, software packages, utilities, and DECnet communications software, as well as a wide range of PDP-11 software in 16-bit compatibility mode.

For OEMs, the VAX-11/750 CPU, with 512 bytes of memory, communications multiplexer for eight EIA terminals, and LA38 DECwriter IV console terminal, is available for $47,000. An entry level packaged system, priced at $89,900, additionally includes two RK07 28M-byte disc drives and the VAX/VMS operating system. A larger package, with 1M byte of memory, VAX/VMS operating system, 16-bit/in tape drive, and RM80 124M-byte disc drive, is priced at $120,000. Volume delivery of RK07 equipped systems will begin in Apr 1981. Systems configured with RM80 drives will be available beginning in June 1981.

Circle 350 on Inquiry Card

THE PERFECT MARRIAGE

CHRISLIN 256KB MEMORY



NOW AVAILABLE! 256KB memory on a dual height board only **$1925.** CHRISLIN INDUSTRIES now offers state-of-the-art 64K RAM Memory system designs. Like our recently introduced 512KB MULTIBUS® compatible single card memory our 256KB LSI 11/23 memory is an industry first.

Free up critical and expensive backplane space. Saves you 3 dual slots.

Addressable in 4K increments up to 4 Megabytes.

On board parity generator checker totally DEC hardware and software compatible.

Single 5 volt power requirement.

Battery back-up capability. 256KB unit draws less than 300 ma at 5 volts in battery back-up mode.

Tested and burned in. Full year warranty.

DON'T ASK WHY WE CHARGE SO LITTLE, ASK WHY THEY CHARGE SO MUCH.

Chrislin Industries, Inc.

Computer Products Division

31352 Via Colinas • Westlake Village, CA 91362 • 213-991-2254

Multibus is a trademark of the Intel Corp. LSI II is a trademark of Digital Equipment Corp.

CIRCLE 40 ON INQUIRY CARD

Desktop Computer System Monitors and Controls Security Activities

Cardkey's Dimension 2000 offers major security management capabilities in single compact package. Designed for small to medium size businesses, the single unit provides television monitoring, access control, and control of security related building operations

All major security functions necessary to protect an office or plant are performed by Dimension 2000, a desktop unit. Enabling one person to visually monitor and control all security related activities, the system, developed by Cardkey Systems, 20660 Bahama St, Chatsworth, CA 91311, handles up to 4000 sequential and 100 random cardkeys and provides dual access levels and time zones.

Among the features of the system are a CRT/CCTV screen for English language data display and TV surveillance; computerized alarm monitoring for fire, smoke, intrusion, and related conditions; and 64-char text display that specifies alarm condition and required response. The system simultaneously monitors hundreds of supervised alarms. Each card reader can monitor eight alarms; special terminals monitoring 24 different alarm conditions can replace card readers. An event time control feature allows the system to automatically operate electrical devices, including heavy industrial machinery and processes. This feature is programmable up to 12 months in advance.

Up to 64 primary access levels can be combined during 8 primary time zones; another 64 secondary levels are possible during 8 secondary time zones. This flexibility permits large groups to have the same access level but prevents access to certain locations during certain time periods. System capabilities also include employee tracking by door, card number, or time of access, with optional printed report.

Bidirectional communication with terminals on a daisy chain loop maintains system integrity in event of sabotage. A 4-hour battery backup ensures security on power failure and minimizes downtime.

Circle 351 on Inquiry Card

Desktop Computers Offer Performance Scaled to Match Price

Desktop business computer systems 1000 and 2000 range from 32k to 64k bytes of user memory, from 325k bytes of flexible disc storage to 5M bytes of hard disc storage, and from one to three microprocessors per model. In the systems, Digi-Log Systems, Inc, Microcomputer Div, Babylon Rd, Horsham, PA 19044, has combined advanced technology, reliability, and solid performance specifications.

Entry level member of the family, the system 1000 is a single microprocessor driven computer that contains a minimum of 32k bytes of user memory and 325k bytes of diskette storage. Features include video attributes to help users identify information on the CRT screen, up to 5M bytes hard disc storage, and up to 64k bytes of expandable user memory. High processing speed accelerates transactions to eliminate operator delays, and CP/M operating system allows use of readily available standard software.

System 2000 is equipped with dual-microprocessor architecture for high speed concurrent processing and disc access operations, 32k to 64k bytes of user memory, and 650k to 1.3M bytes of diskette storage. Other attributes include expansion of diskette storage to 1.3M bytes and expansion of user memory to 64k bytes.

The system performs general business operations and is supported by applications packages that cover accounts payable, accounts receivable, payroll, general ledger, inventory control, and order entry. The system is designed for compatibility with established user conventions.

Chip speed contributes to processor cycle time. Logic density results in 75% fewer components than previous generation. Fewer parts and internal connections enable structural quality and feature depth. Reduced assembly and test labor decreases manufacturing cost and increases reliability.

With deliveries scheduled to begin in February, system 1000 prices range from $3995 to $6595. System 2000, available in January, is priced between $8500 and $11,995.

Circle 352 on Inquiry Card

Unit Processors with Cache Memory Upgrade Family Performance

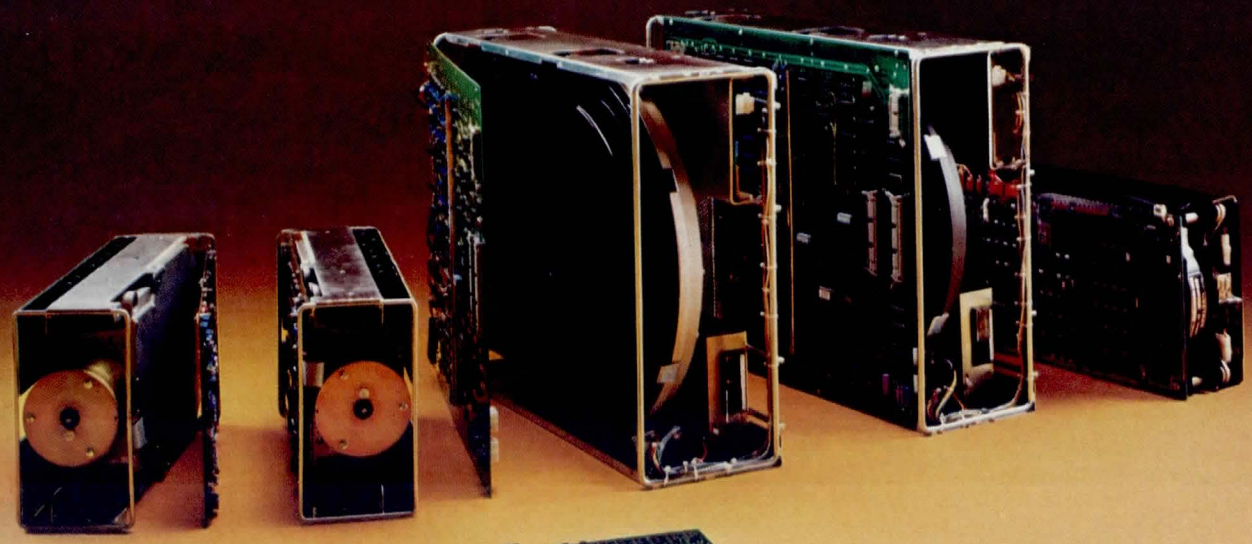
Models E1 and E2 in the 1100/60 family offer performance improvements over C1 and C2 unit processors previously released by Sperry Univac, PO Box 500, Blue Bell, PA 19424. The E1 provides a 45% improvement over the C1, while performance of the E2 with extended instruction set is 40% greater than that of the C2. Both have 2k words (8k bytes) of cache memory.

Large scale general purpose computers in the 1100/6 family implement instruction execution with multiple microprocessors. This offers a competitive price/performance ratio while substantially reducing the size of the processor and consequently power and environmental requirements.

An 1100/61 E1 central processing complex with 2M-bytes main storage, 8k bytes of buffer storage, one I/O processsor, and one system support processor is priced at $518,975. The E2 complex is priced at $555,545. Deliveries are scheduled for first quarter of 1981.

Circle 353 on Inquiry Card

THE SMART SET



Members of this exclusive circle of PRIAM Winchester disc drives have several uncommon things in common. With database capacities from 10.8 to 158 megabytes, they all have the same interface. And they all connect quickly and easily to the typical microprocessor I/O bus through PRIAM's SMART Interface.

A simple adapter, added to the SMART Interface, is all you need to provide your system with the remarkable reliability of Winchester disc drives. And PRIAM's DISKOS drives have the broadest available capacity range, with the lowest cost-per-megabtye, for microprocessor-based systems.

How Smart Is SMART?

With its own sophisticated preprogrammed microprocessor, PRIAM's optional SMART Interface gives you these disc subsystem functions:

- Controls any combination of one to four PRIAM Winchester disc drives.
- Serializes and deserializes data and formats disc with selectable sector sizes of 128, 256, 512 or 1024 bytes.
- Full sector buffering permits data transfers at any rate up to 2 megabytes per second, with programmed I/O or DMA.
- Automatic alternate sector assignment makes disc defects transparent to the host processor.
- Overlapped-command and implied-operations capability improves system throughput in multiple-drive systems.

The single 8″ x 14″ SMART Interface printed circuit board mounts on the PRIAM disc drive and draws power from the drive; or it can be mounted separately to maintain the basic drive size envelope.

Meet The Elite! PRIAM's High-Capacity, Cost-Effective 14-Inch Disc Drives

PRIAM's high-technology 14-inch Winchester disc drives are available with capacities of 34 and 68 megabytes, with a 158-megabyte version on the way. And they all fit in the same 7″ x 17″ x 20″ package, including optional power supply. Fully servoed linear-voice-coil head positioning provides fast, precise and reliable data retrieval. Average positioning time is only 45 milliseconds, and track-to-track is a fast 8 milliseconds for high throughput.

Use of a brushless DC spindle motor assures mechanical simplicity, positive disc speed control, and operation of PRIAM drives with power sources anywhere in the world without change. No relays, no mechanical brakes, no brushes, belts, or pulleys. Pure, reliable electronic control. Elegantly simple!

The Talk of the Town: PRIAM Eight-Inch Disc Drives

When you want to debut a Winchester disc drive where you now have an 8-inch floppy disc, PRIAM's DISKOS 2050 and 3450 fit right in. And they give race-horse performance to your system by expanding your database to 21 or 35 megabytes, with head-positioning times of only 45 milliseconds average and 8 milliseconds track-to-track.

From the same technical family tree as their bigger brothers, PRIAM 8-inch drives use linear-voice-coil positioning and brushless DC motors. In the next generation, they will permit database expansion to 70 megabytes, in the same small, interface-compatible package.

If a simpler, even lower-cost drive will serve your purpose, the DISKOS 1070 gives you 10.8 megabytes of capacity, with stepper-motor positioning for seek times of 73 milliseconds average and 23 milliseconds track-to-track. Not as fast as other PRIAM family members, but still just as SMART when used with PRIAM's SMART Interface.

Other Interface Options!

Is SMART too smart? PRIAM also offers a lower-cost serial-bit NRZ data interface for the OEM who wishes to design the complete controller or to purchase one. This interface, similar to the evolving ANSI standard, has an 8-bit bidirectional microprocessor interface for all spindle motor and head positioning controls.

And if you have an existing storage module controller, PRIAM offers an SMD interface to extend the life of your controller and software and put Winchester disc drive benefits into your system quickly and easily.

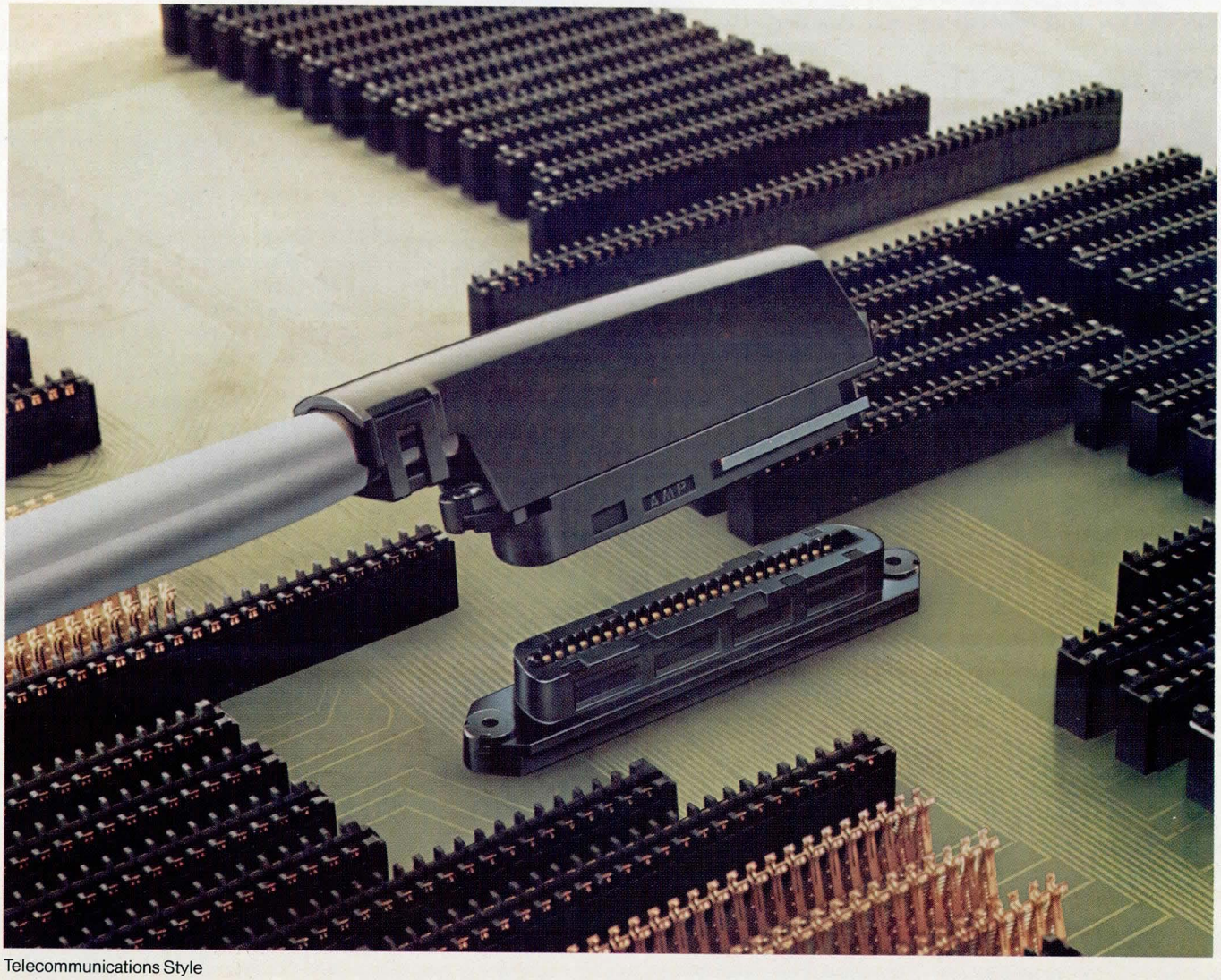
For complete information about the SMART Interface and the members of the SMART SET of PRIAM Winchester disc drives, RSVP by telephone or mail to:

PRIAM

3096 Orchard Drive San Jose, CA 95134
Telephone (408) 946-4600 TWX 910-338-0293

CIRCLE 41 ON INQUIRY CARD

"Forget solder baths. For increased reliability, ease of repair, and a lower applied cost, I'll take AMP compliant pin technology."



Telecommunications Style

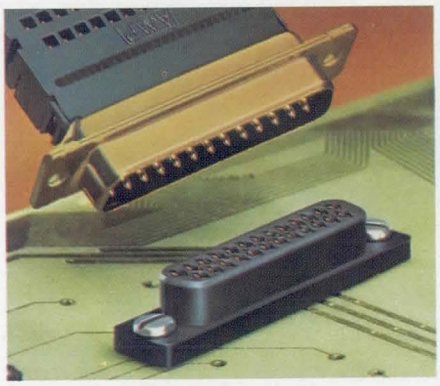
ACTION PIN was the industry's first compliant pin design. But that isn't nearly as important as the fact that since their introduction, ACTION PIN contacts have been proven reliable and cost effective in hundreds of thousands of feed-through post and mother/daughter board applications.

Now there are I/O Connectors with the same compliant pin design. Choose from subminiature D type connectors for RS 232 and 449 applications, a popular telecommunications style, or shrouds which quickly convert feed-through posts to headers for use with .050" centerline ribbon cable.

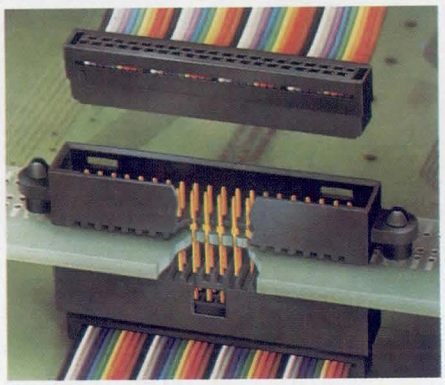
In each case, you can design completely solderless back panels. And that means you eliminate the production losses from broaching, rupturing, distortion, tearing, and damage to plated-through holes. And if contact repairs ever are necessary, they're easily accomplished without degrading mechanical or electrical performance. And that gives you cost savings across the board.

Interested in eliminating the problems and expense of solder baths? Write or call us for more information on the benefits of solderless back panels with AMP ACTION PIN contacts.

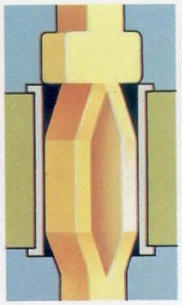
AMP has a better way.



Subminiature D Style



Shroud Style



Contacts feature unique compliant pin design.

Some facts worth knowing about AMP ACTION PIN contacts

Tooling: Complete range available from prototype to production rates in excess of 10,000 an hour.

Assemblies: Boards preassembled to your specifications with AMP components are available from panel suppliers. Contact AMP Incorporated for more details.

Environmental Tests:

Test	Type		Results in Milliohms				
			Change in Resistance, R				△R Values (95% CL)*
			Min.	Max.	Mean	Std. Dev.	
Thermal Shock and Vibration: −65° to +125°C for 5 cycles; 10-200 Hz three planes, 12 hours	Gold	3A	0.058	0.281	0.121	0.038	0.301
	Tin press fit	3A	−0.002	0.176	0.094	0.046	0.313
High Humidity: 96 hours at 40° ± 2°C. 90-95% RH	Gold	3A	−0.043	0.017	0.010	0.017	0.070
	Tin press fit	3A	−0.066	−0.016	−0.028	0.011	0.026
Salt Spray: 48 hours at 5% concentration NaCL	Gold	150mA	−0.076	0.034	−0.008	0.022	0.098
		3A	−0.052	0.051	0.013	0.021	0.113
	Tin press fit	150mA	−0.062	0.062	−0.012	0.028	0.121
		3A	−0.056	0.049	0.007	0.026	0.129

*Exceeded by fewer than 1/10,000 samples.

Where to telephone: Call the ACTION PIN Information Desk at (717) 780-8400.

Where to write: AMP Incorporated, Harrisburg, PA 17105.

AMP

NEVER BEFORE HAS A BACK-UP SYSTEM BEEN AS INTELLIGENT AS THE SYSTEM IT'S BACKING UP.

This is 3M's HCD-75 High Capacity Data Cartridge Drive. And the reason it's as intelligent as a computer is because it thinks like one.

You see, unlike other back-up systems, the HCD-75 is interfaced directly with the primary system by means of sophisticated, microprocessor electronics. When the host computer has data to feed, the HCD-75 starts automatically. When the host computer stops, it does too. And since the HCD-75 also positions to any location, it not only saves tape cost, but retrieval time as well.

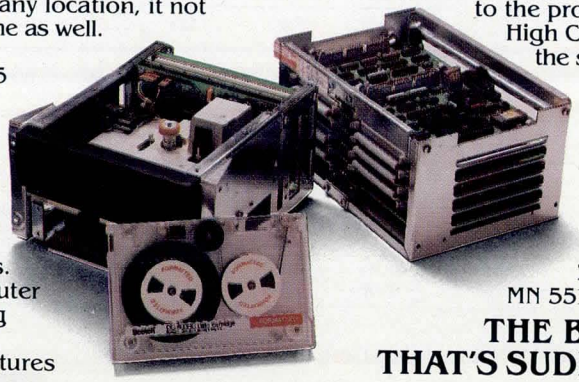
Of course, the use of microprocessors allows the HCD-75 to perform a number of other time-saving functions, too. Like block replacement, so you can easily correct errors or change files which need updating. And fast random access, which makes it useful both as an I-O device or as a storage unit for low-usage files. All of which relieves the host computer from difficult timing and formatting problems.

What's more, the HCD-75 features state-of-the-art error detection and correction capabilities. Even when the system is off-line, self-test diagnostic routines monitor its performance. And, combined with each of its $32.50 high-capacity cartridges, the HCD-75 provides a full 67 megabytes of formatted user information (144 mbytes unformatted). So costly operator interventions are sharply reduced.

If you're looking for a reliable, cost-effective solution to the problem of disk back-up, the HCD-75 High Capacity Data Cartridge Drive is the system you should be thinking about.

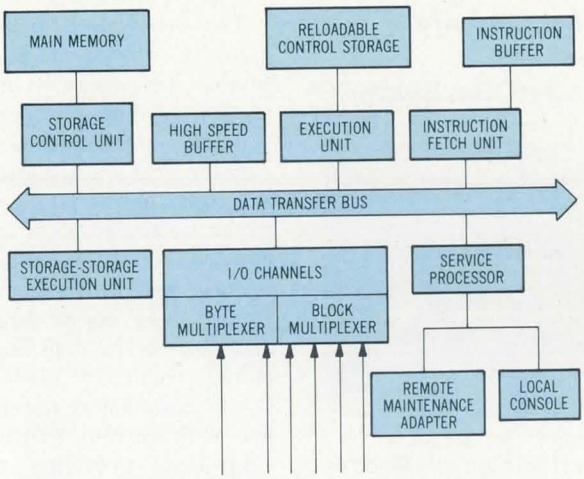
Not only has a lot of thinking gone into it. But a lot of thinking comes out of it, too.

For more information, check the listing on the next page for the representative nearest you. Or write: Data Products Division/3M, Bldg. 223-5E/3M Center, St. Paul, MN 55144.



THE BACK-UP SYSTEM THAT'S SUDDENLY WAY OUT FRONT.

4300 Compatible Processors Offer Benefits in Price/Performance



ExpandaBus architecture of IPL Systems' 4400 series IBM compatible mainframes includes central data transfer bus capable of rates to 80M bytes/s, main storage bus, and control storage bus. Adding plug-in circuit modules allows users to increase instruction execution rate, add system features, and increase channel capacity

4400 series machines, introduced by IPL Systems, Inc, 360 Second Ave, Waltham, MA 02154, are fully compatible with IBM's 4300 series and offer price/performance benefits over comparable IBM models. Various processors in the series double the channel capacity and the memory, and increase execution speed of comparable 4300 models.

The family's ExpandaBus™ architecture, a modular design concept, allows users to plug-in circuit modules to increase instruction execution rate, expand the size of main memory, add system features, and increase channel capacity. The architecture includes a central data transfer bus with transfer rate of 80M bytes/s, main storage bus, and control storage bus. This architecture also simplifies service and fault isolation.

Low- and mid-range model 4436 has twice the channel capacity of the 4331-2; model 4443 is comparable to the 4341 but has twice the memory capacity and provides superior execution speed. A higher performance unit scheduled for delivery late next year, the 4446 is field upgradable from the 4443 and comparable to the 4341-2.

Central processor has a 50-ns cycle time and provides 64k control storage, 8 floating point, and 16 general purpose registers. Memory is formed of 16k NMOS RAM with an 8-bit word size and full store operation time of 500 ns.

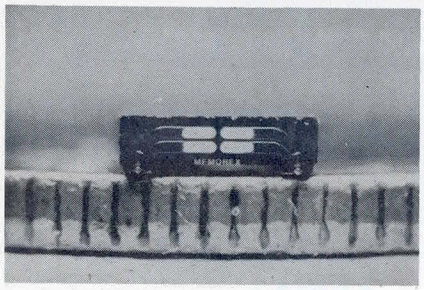
All processors provide from 1M to 8M bytes of main memory and from 2 to 5 block multiplexer channels. Reloadable control storage allows design modifications to be made as 4300 series architecture changes. Other design advantages of the series include use of ECL and MOS circuitry to permit lower power consumption, and floor space requirements.

Processors are fully compatible with IBM system control programming including ECPS: VSE with single-level addressing and virtual channel addressing; ECPS: UM/370; and ECPS: VS1. All systems attach to peripherals that connect via the 4300's I/O channel, including 3370 and 3375 disc drives.

An internal microcomputer based service processor inside the system assumes control immediately after a system malfunction. It notifies both program and operator and records data on the failure, isolating faults through diagnostic tests.

A typical 1M-byte 4436 is priced at $175,000. Price of a typical 4443 with 2M-byte memory is $225,000. Deliveries are 60 days ARO. Circle 354 on Inquiry Card

Thin Film Technology Should Lead to High Capacity Disc System



For use in high performance disc storage unit, thin film head developed by Memorex (shown resting on a dime) can accurately store and retrieve computer data on magnetic discs at densities of 10M bits of information per square inch

A high performance, high capacity, thin film technology disc storage subsystem that will compete with IBM's 3380 direct access storage device and 3880 models 2 and 3 storage control is under development at Memorex Corp, San Tomas at Central Expy, Santa Clara, CA 95052. The disc drives will attach to large 4300 series computers, to system/370 computers, and to 3031/3032/3033 processors, as well as to equivalent computer systems.

To match performance of its thin film technology disc drives, an advanced storage control unit utilizing state of the art architecture is also under development. This controller is intended to serve as the vehicle for integrating the disc drives into complete, high performance storage subsystems.

The thin film development program, on which the product is based, was conducted by the Recording Technology Center (RTC) in Santa Clara, California. RTC Laboratories, a part of the Storage Systems Group, are responsible for developing advanced digital recording technologies in support of end user and OEM data storage and retrieval equipment. Through their efforts, state of the art performance has been achieved in the application of thin film technologies to rotating magnetic memories. The program has resulted in operational thin film read/write heads, servo heads, and matching integrated circuit amplifiers.

The decision to include this high capacity subsystem in the storage product line was based on a field study of the medium and large computer systems market, and its requirements over the next 3 to 5 years. According to this study, online data storage capacity in the United States is increasing at a compounded rate of about 45%/yr for the average processing center. This means that many large computer system users are doubling their online storage capacity every two years. While customer requirements can be met with current 3650 and 3652 disc subsystems providing data storage capacities of 0.64G and 1.27G bytes per module, the thin film technology subsystem should assure users of a high performance product to meet anticipated needs for greater capacity.

Circle 355 on Inquiry Card

Raster Graphic Display System Interchangeable With TEK 4014-1

G-1000 provides high speed interactive raster graphics display capability. With the system, Genisco Computers, Div of Genisco Technology Corp, 3545 Cadillac Ave, Costa Mesa, CA 92626, has taken advantage of reduced memory cost and 16-bit microcomputers to provide a low cost raster scan unit that is a direct plug replacement for Tektronix's 4014-1 storage tube terminal, including PLOT-10™ software compatibility.

The monochrome terminal offers raster scan advantages that include selective erase of any part of the graphic or alphanumeric image, high contrast and brightness that permit viewing in standard room light, long product life, clear black and white images, continuous viewing with no damage to the phosphor, and unlimited write-through without flicker. Resolution is 1024 x 792 x 1-bit, in a 19" screen configuration. 60-Hz refresh assures flicker free operation.

Based on the Z8001 segmented 16-bit microprocessor, the terminal is user programmable, offering up to 16k words of EPROM as well as 16k RAM. Since the unit's 4014-1 function requires approximately 8k of P/ROM, the user retains 8k in which to develop his own programs. Data are configured in 10-bit members for both X and Y addresses; the microprocessor's 16-bit word permits one operation per address, greatly reducing the amount of software and hardware that would be required with an 8-bit processor.

Memory plane of the system consists of 128k bytes of dynamic RAM. This is organized as a 2-port memory: one a read/write port available to the processor and the other, a read-only port for the video display, that is also available to the logic system. Since RAM exists in the processor address space through the read/write port, the processor has direct access to the pixel image, thus providing maximum flexibility to the system.

The system controller that takes data from memory and from the screen uses both TTL and ECL devices. ECL is necessary to support the 68-MHz pixel rate of the system. Since each pixel is 15-ns wide—the propagation delay of most TTL gates—ECL speed is necessary.

Detachable keyboard for the terminal includes typewriter style alphanumeric keys, special function keys, 12-key numeric pad, and cursor controls for maximum interactive capability. The system uses an asynchronous serial interface that is RS-232 compatible with data rates to 19.2k baud. All components of the system, including display, keyboard, electronics chassis, and power supply, are packaged in a standalone configuration for use on desktop or mounted on a pedestal.

Designed to provide the precise detail and data manipulation capability demanded for applications such as CAD/CAM, scientific data analysis, and mapping and circuit board design, units are priced at $9995 in single-unit quantities. Deliveries are scheduled to begin this month.

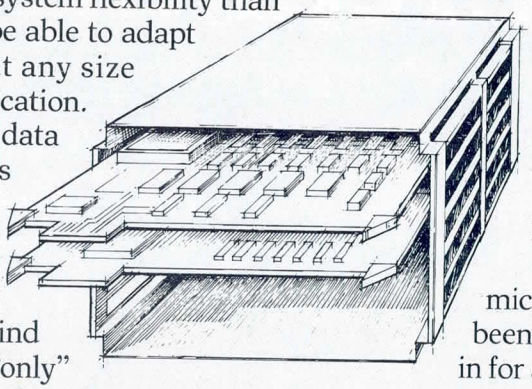
Circle 356 on Inquiry Card

Hewlett-Packard announces another small breakthrough.

The two-board, 1/2 megabyte microcomputer.

Our HP 1000 L-Series now offers state-of-the-art 64K RAMs. They're the reason we've been able to put 512 kilobytes of memory on just one 6¾" x 11" board.

With the CPU on the other board, the L-Series opens a whole new dimension in microcomputers. Because with so much memory in so little space, you have more system flexibility than ever before. In fact, you'll be able to adapt the L-Series for just about any size job—and any kind of application. Including communications, data management and process control.



Big software for small hardware.

You may have to remind yourself that the L-Series is "only" a microcomputer. With powerful software features like our multi-programming, multi-user RTE operating system and language support that includes Assembler, FORTRAN 4X, BASIC and PASCAL, there's almost no limit to the high performance products you can build. Especially if you take advantage of our proven data base management system and networking software—also upwardly compatible throughout the entire HP 1000 line.

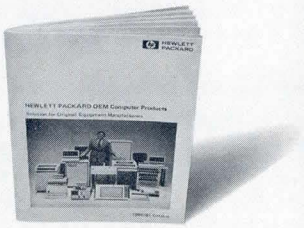
Multiple I/O processors, too.

The L-Series is designed with an innovative distributed intelligence architecture that assigns I/O traffic to separate processors located on each interface board. This means each I/O processor has its own direct memory channel—and direct access to the entire main memory. So you get exceptional I/O performance and greatly increased throughput.

Choose your configuration.

The HP 1000 L-Series comes in a wide range of board, box and system packages. Which means you'll be able to choose the configuration that's best for your application. Development units are available at $13,250* for the CPU and a full 1/2 megabyte of memory.

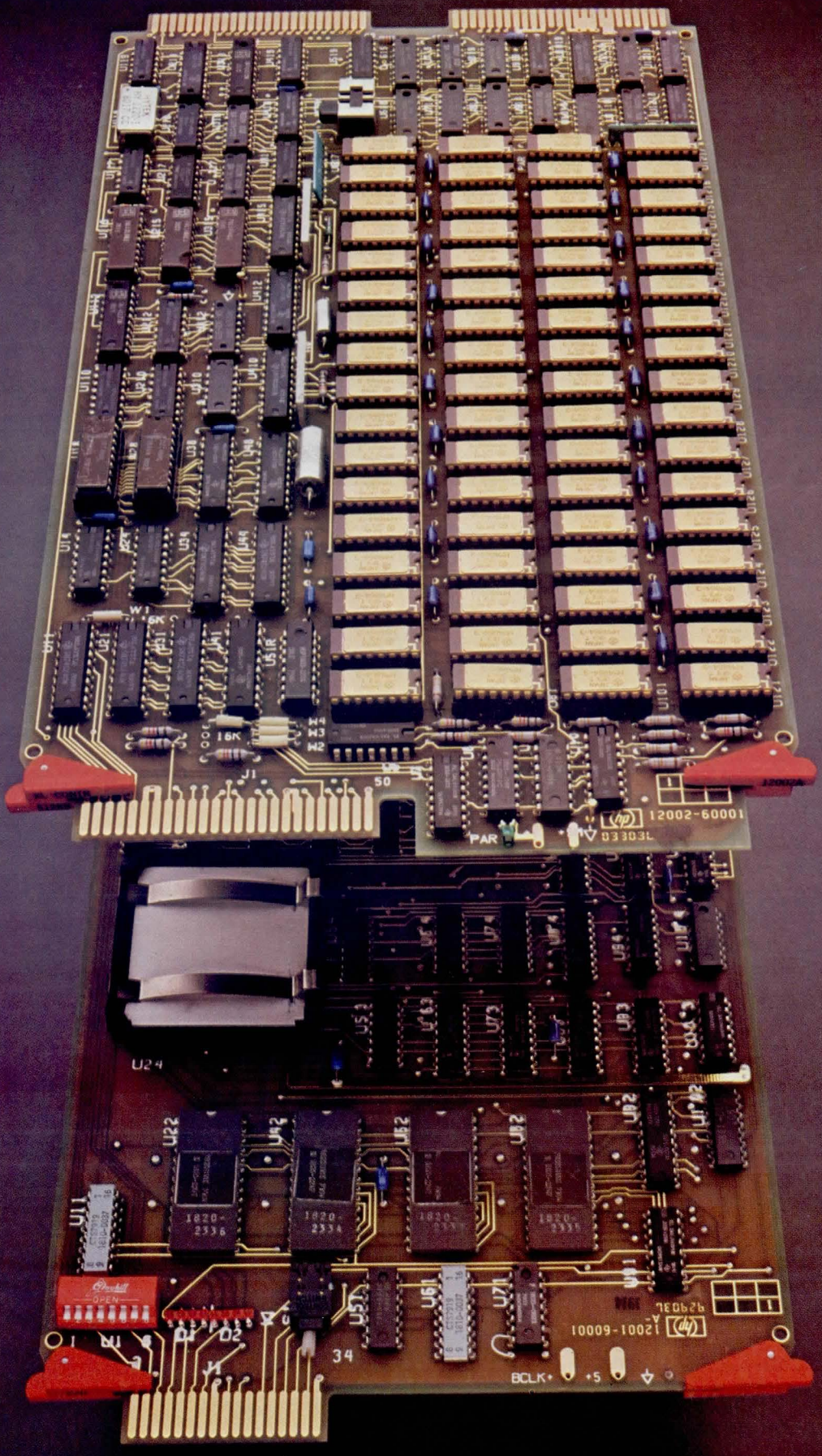
If a two-board, 1/2 megabyte microcomputer sounds like what you've been looking for, come in for a hands-on demonstration. Just call the nearest HP sales office listed in the White Pages. Or write for more information, and a copy of our new OEM catalog, to Hewlett-Packard, Attn: Roger Ueltzen, Dept. 1286, 11000 Wolfe Rd., Cupertino, CA 95014.



HEWLETT PACKARD

*Price is U.S. list.

CIRCLE 44 ON INQUIRY CARD


12002-60001
03303L
PAR
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J1
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U24
12001-60001
BCLK+
+5
34


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HM4864-2

NEW!

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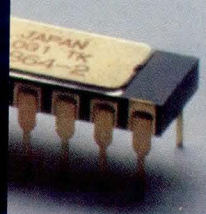
The HM4864 From HITACHI !!!

The New Hitachi HM4864 64K x 1 Dynamic NMOS RAM — In Stock, Ready For Immediate Delivery. The new Hitachi HM4864 uses the JEDEC standard 16-pin configuration, yet it provides high system bit densities and is compatible with widely available automatic testing and insertion equipment. The HM4864 features 150ns access time, a single 5V power supply, built-in VBB generator, TTL interface compatibility, on-chip address and data registers, and two chip select methods for determining appropriate speed and power characteristics of a memory system. Operation modes include read-modify-write, RAS-only refresh, and page-mode capability. The HM4864 consumes 330mW when active, and only 20mW in standby.

To order your Hitachi HM4864 NMOS Dynamic RAMs, call your local Hitachi Representative or Distributor.



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CIRCLE 45 ON INQUIRY CARD

Printer, Disc Drives, And Software Enhance Distributed Systems

Series 21 distributed processing systems from Mohawk Data Sciences, 7 Century Dr, Parsippany, NJ 07054, have been enhanced with combination fixed/removable disc drives, remote station printer, COBOL, and extended data entry capability. The disc system responds to customer demand for low cost mass storage while the station printer increases efficiency of individual workstations. The COBOL package is intended to complement MOBOL by facilitating batch processing, report editing, and general output data manipulation, while extended data entry allows disc storage to be used in data entry operations.

Ranging in capacity from 26M to 78M bytes, disc drives combine fixed platters with a removable platter on a single spindle. Configurations for system 21/50 include models 2175-1 with 13M fixed and 13M removable, 2175-2 with 39M fixed plus 13M removable, and 2175-3 with 65M fixed plus 13M removable. System 21/40 supports the 2175-1. The 21/50 supports multiple discs from a single controller.

Model 2141-1, a compact station printer, can be located with a display station up to 2000′ (609.7 m) from the controller. The unit prints at 45 chars/s on a full 132-char line, using a daisy wheel font for high quality. Four printers with display stations can be supported by the 21/50 in addition to the system printer. Printer and associated CRT may operate independently or act together.

Using standards set by ISO and ANSI, the COBOL package is an ANSI 74 implementation that offers extended key/screen handling. The package can be used within the standard hardware/software environment. It functions on 21/40 or 21/50 in 1- to 4-station configurations, and may operate in conjunction with MOBOL programs or data entry, data communications, and word processing. It supports the full range of peripherals on series 21 systems.

Extended data entry provides series 21 users with the ability to use disc storage in data entry operations. Allowing users to create a data base for higher data entry efficiency, the package provides a full range of functions and capabilities. Since the software uses disc storage, I/O rates are increased adding to the overall transaction speed of the operation.

Circle 357 on Inquiry Card

IBM Compatible Processor Doubles Performance Of 3033 Uniprocessor

As an alternative to IBM 3033 Systems, the AS/9000 manufactured by Hitachi America, Ltd is being made available by National Advanced Systems, 3145 Porter Dr, Palo Alto, CA 94304. With internal performance rated at approximately twice that of a 3033 uniprocessor, the AS/9000 uses 550-gate LSI circuits, fast bipolar RAMs, and advanced architecture to achieve optimum performance. Its firmware based architecture has been designed to protect the customer's investment in software and training by tracking anticipated IBM announcements.

The processor complex consists of several functional processors, each individually microprogrammed to ensure compatibility with IBM system architecture. 16k words of 160-bit reloadable control store in the CPU control basic machine operation and provide assistance for MVS and VM. Pipelining within the CPU allows each of the two instruction units to preprocess up to four instructions simultaneously with instruction execution. Cache memory with 64k-byte capacity reduces main storage access by both instruction and execution units. Execution of fixed and floating point multiplication and floating point division operations is performed by a high speed arithmetic subprocessor. A 512-entry translation lookaside buffer and 512-entry segment table origin stack enhance support for virtual storage operations.

The throughput obtained is attributable to the advanced technology used in its design. The base logic of the processor is a 550-gate IC with a switching speed of 700 ps. Also incorporated are single ICs with 470 logic gates plus 3 bytes of read alterable memory (RAM). These high density components combined with efficient packaging techniques allow the unit to be air cooled.

The unit's 64-byte high speed cache buffer uses 2-way interleaving to reduce system contention between the instruction unit (IU) and the execution unit (EU) when fetching information from cache during instruction decode and execution. Made up of high performance bipolar RAMs with a 40-ns access time, the buffer is organized into four 16k sets which can be independently operated for maximum system availability.

High speed arithmetic (HSA) capability is microprogram controlled and operates with a cycle time of 20 ns. The HSA processes fixed and floating point multiply and floating point divide instructions approximately three to five times faster than would a CPU processing these instructions without HSA.

Main memory expands in 2M-byte increments to the current system maximum of 16M bytes. Storage sizes in excess of 16M bytes may be addressed when supported by the relevant IBM operating system. Memory is 8-way interleaved and may be reconfigured in 2M-byte increments.

Independently microprogrammed input/output processors (IOPs) are used to control I/O operations. Two IOPs are provided in the standard configuration and control 12 channels. The current maximum of 16 channels is provided by the addition of a third IOP.

Each channel is provided with 256 unit control words (UCWs). One or two of the channels may be configured as byte multiplexer, the remaining being block multiplexer.

Operation of the processor is controlled by two independent service processors. Both contain a 20″ (50.8-cm) 4-color visual display screen and a full-function keyboard. Each may be used independently for operator control or field engineering diagnostic purposes, thus greatly enhancing the availability of the total system.

Disc storage devices including IBM 3375 and 3380 are supported. The 3380 will be supported at 3M-byte transfer rates by 3rd quarter 1981; and the 3375 in data streaming mode in 1st quarter 1982.

Price of the system configured with 16M-byte main memory and 16 channels is $4,520,000.

Circle 358 on Inquiry Card

DILOG INTERFACES DEC 11*

10 intelligent hard disc and magnetic tape controllers offer LSI-11,* 11/2, 11/23, and PDP-11* single quad slot compatibility with up to 60% power saving.

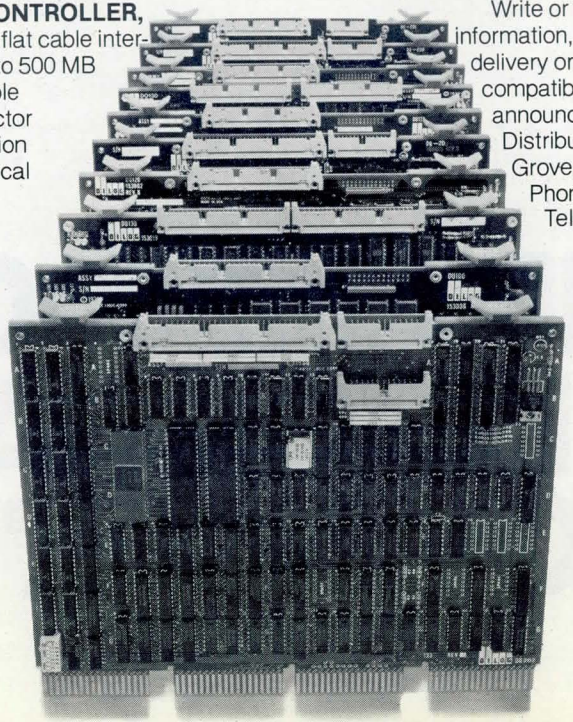
Only DILOG (Distributed Logic Corporation) exclusive automated design, common proprietary architecture and sophisticated bipolar μPs give you • all single board quad size products requiring no external power or chassis . . . just a cable to connect the drive . . . *you don't need anything else* • high reliability • automated self-test including data base protect feature and indicator. And at cost savings of 50% or more.

LSI-11 MAGNETIC TAPE CONTROLLER, Model DQ 120, interfaces 4 industry standard reel-to-reel drives • emulates TM11* • handles 7 and/or 9 track NRZI drives to 112.5 ips • selectable DEC or IBM byte order formatting • data error checking • RT-11/RSX-11* compatible • extended addressing to 128K words.

LSI-11 MAGNETIC TAPE COUPLER, Model DQ 130, interfaces dual density (NRZI/PE) formatted drives • emulates TM11 • handles up to eight 9 track 800/1600 bpi industry standard drives at speeds from 12.5 to 125 ips • "streamer" mode capability • software or switch selectable density • RT-11/RSX-11 software compatibility.

LSI-11 MASS STORAGE DISC CONTROLLER, Model DQ 200, interfaces any two SMD flat cable interface compatible hard disc drives for up to 500 MB on-line storage • mix or match compatible Winchester, SMD or CMD • variable sector size • automatic media flaw compensation with bad sector flagging • optimized logical to physical unit mapping • implements Winchester fixed head option.

NEW LSI-11 SHUGART SA4000 WINCHESTER DISC CONTROLLER, Model DQ 201, emulates DEC RK* • runs drivers under RT-11 and RSX-11M* systems • compatible with 14.5 MB SA4004 or 29 MB SA4008 drives • automatic media flaw compensation.



LSI-11 DISC CONTROLLER, Model DQ 100, interfaces 2.5, 5, 10 or 20 MB cartridge and fixed platter drives in combinations to 80 MB • RKV-11/RKO5* emulator • handles front load (2315) and/or top load (5440) drives • automatic power fail/power down media protection • RT-11/RSX-11 compatible.

NEW LSI-11 EMULATING MASS STORAGE CONTROLLER, Model DQ 202. Cost effective interface of two 8 and/or 14-inch Winchesters, SMD or CMD hard disc drives without changing controller . . . 8 to 300 MB capacity • RP emulator • automatic media flaw compensation.

PDP-11 MAGNETIC TAPE CONTROLLER, Model DU 120, emulates TM-11 and has same features as Model DQ 120 (LSI unit) • software compatible with RT-11, RSX-11, RSTS, IAS and MUMPS.

NEW PDP-11 MAGNETIC TAPE COUPLER, Model DU 130, offers features of Model DQ 130 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS software compatible.

PDP-11 DISC CONTROLLER, Model DU 100 includes features of Model DQ 100 (LSI unit) • RT-11, RSX-11, RSTS, IAS and MUMPS compatible • emulates RK-11.

NEW PDP-11 EMULATING MASS STORAGE CONTROLLER, Model DU 202, offers same features as Model DQ 202 (LSI unit).

Write or call for detailed product performance information, OEM quantity pricing, stock to 30 day delivery or warranty data on these DEC 11 compatible products . . . or several soon to be announced new DILOG products.

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CIRCLE 46 ON INQUIRY CARD

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Nobody else has an emulator with as many logic analyzer functions as ours. Not Intel. Not anybody.

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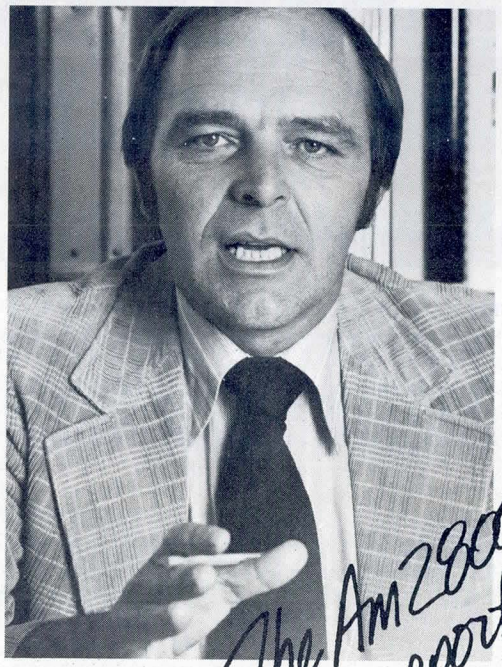
The RTE16/8050 provides transparent real-time emulation for the AmZ8000. And our high-speed emulation memory allows target execution with zero wait states. Not one. Zip.

Not only that, but the RTE16/8050 records the events in a real-time trace buffer so you can display the bus activity decoded into instruction mnemonics or trace waveforms. And thanks to a sophisticated trigger logic with trace qualifiers,



Frank W. Zurcher, President, Advanced Micro Computers, A subsidiary of AMD

The AmZ8000 is supported by the best 16-bit emulator.

"THE AmZ8000'S EMULATOR HAS IT OVER ICE."*

you will capture only those events which are critical to your target system evaluation.

But wait, there's even more: 12 breakpoint comparators, patch RAM, expanded TRACE, triple bus architecture. Everything you need for program development and system integration is right here.

And the RTE16/8050 is the first emulator to combine all these features with a user-friendly interface. We've combined screen-oriented displays with soft keys. So you don't have to remember a whole lot of command syntax. Just push a key and your format pops up automatically.

One last thing: Every RTE16/8050 system is 100% burned in. 100%!

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Right, From The Start.

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CIRCLE 47 ON INQUIRY CARD

Bare Board Tester Performs Automatic Continuity/Leakage Tests

Modular hardware architecture of the N221 bare board test system enables configuration of memory and pin electronics to test 64k points. Teradyne Inc, 183 Essex St, Boston, MA 02111, provides the system complete with software written especially for bare board test plan development, testing operations, and fault diagnosis. The combination addresses a range of bare board test requirements.

The basic system consists of test administration/system control (TASC) center and test station linked by a single ribbon cable assembly to 50′ (15 m) long. The TASC center includes the system controller, a microprocessor based single-board computer, a full alphanumeric keyboard with additional dedicated function keys, 15″ (38-cm) interactive CRT, dual floppy disc drives for loading system executive software and reading and writing test plans, measurement and address electronics, and memory. 64k bytes of RAM are standard, which is enough for the system software and a test plan for approximately 12,000 points. Memory expands in 32k pages up to 256k bytes, for storing multiple test plans in memory or for testing up to 64k points at a single test station.

Production testing occurs at the test station which houses the solid state test electronics that decode address instructions and switch voltages between points of test. Test electronics are packaged in modular cards that plug into fixture assemblies. One fixture assembly provides a connectorized interface between the test electronics and pins on an integral vacuum fixture base that uses interchangeable test heads to access each different board type. An optional fixture assembly provides either a ribbon cable or a wire-wrap interface to a fixture supplied by the user. Controls for the production operator at the test station include system status indicators, start and stop test buttons, pass and fail LEDs, a mode switch for manual or automatic operation, and a thermal printer for data and diagnostic printouts.

The system's combination of solid-state switching, fast bus addressing, and high speed testing algorithms is designed to locate shorts and opens between test points at speeds greater than 2000 points/s. In addition to the continuity test, which typically employs a 5-kΩ decision threshold, a second measurement threshold can be selected to detect leakage paths between lands that might be caused by contamination on the board, residues from the plating and etching processes, or solder slivers. A choice of three leakage thresholds is available: 100, 250, or 500 kΩ.

A single TASC center can control testing at up to four test stations, each with its own bed of nails fixture, operator's controls, and test electronics. Software uses self-explanatory menu lists to speed test plan generation and simplify interaction with the system when setting up production testing. Organized in functional modules, the software presents several menu lists simultaneously on the CRT, with the various lists providing a choice of parameters for that function.

Test plans for each board type are created in two steps. The first step defines a naming scheme for the test points, creating a one to one equivalency between points of test electronics and nodes on the board under test so that error diagnostics locate faults on the board in the user's product nomenclature. The second step is programming the networks, or shorted groups of points, on the board. The system automatically self-programs the correct interconnections from a known-good board, or the system may be programmed manually by typing in correct interconnections. With an optional RS-232-C serial communications port and translation software, test plans can be created from a customer's computerized data base, such as that used for computer aided board design.

Configured with 64k bytes of memory, and with test electronics, and an integrated vacuum fixture base for testing up to 1920 points, U.S. list price of the N221 is approximately $45,000. Initial shipments are scheduled to begin in the second quarter of 1981, with deliveries anticipated to be 12 to 16 weeks ARO thereafter.

Circle 359 on Inquiry Card

Flat Ribbon Cable Connectors Complement Existing Line

Flat ribbon cable connectors, introduced by Bunker Ramo's Amphenol North America Div, 2122 York Rd, Oak Brook, IL 60521, are intended for application in EDP, instrumentation, industrial controls, and telecommunications systems. Key features of the 840 series sockets and headers include positive header locking device, integral molded polarizing key, insulation displacement contacts, and single-motion mating.

Among the connectors in the six lines are sockets and headers for 3-A applications on 0.125″ (3.175 mm) centers (20 and 34 contact), DIP plugs for use with DIL sockets (14, 16, and 24 contacts), and card-edge connectors with and without mounting ears (34 and 40 contacts). Micro-Ribbon^{R} connectors provide for flat cable interconnection between equipment (36 and 50 contacts), and discrete wired connectors mate with existing socket and header flat ribbon cable connectors having 20, 26, 34, 40, 50, and 60 contacts.

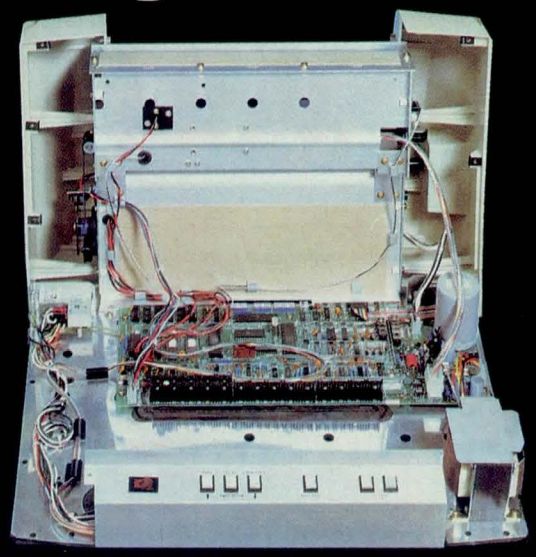
The positive header locking device prevents accidental disconnecting due to handling and vibration. Latching mechanisms automatically activate when the socket connector is mated with the corresponding header. Socket connectors are removed by opening and releasing the latches. One-motion insertion and removal simplifies connector mating and unmating.

Headers are offered in both straight and right-angle DIP and wire-wrappable configurations in two different contact lengths. Sockets are specifically designed for insulation displacement connection and will accept #26 AWG solid cable, #28 AWG solid or stranded cable, or #30 AWG solid cable.

All 840 series connectors have a voltage rating of 250 Vac (rms) and current rating of 1 A. Dielectric withstanding voltage is 500 Vac (rms) for 1 min. Insulation resistance is 1000 MΩ minimum at 500 Vdc and contact resistance is 15 mΩ maximum, at 1 Adc. Molded components, including the socket housing cover and clamps, are all constructed of 94V-O-rated flame resistant materials.

Circle 360 on Inquiry Card

Say Ahh...



Our New grafixPLUS™ 80-column printer opens wide for easy servicing.

Introducing the newest members of our grafixPLUS™ family—the DP-9000 Series 80/132 column printers—built on the same tradition of quality printout, solid design and low cost of ownership established by our 132/220 column DP-9500 Series.

A Case for Serviceability

Not that is comes up often, but want to get inside? Simple. Just remove a few screws and the clam-shell case swings open exposing all major components. This easy access plus built-in self-test and minimum component count yields an MTTR of one-half hour. The 9-wire print head replacement's even simpler . . . two screws and it's out. Without opening the case. And without a service call.

Performance Plus

The DP-9000 Series prints the full ASCII 96 character set, including descenders and underlining, bi-directionally, at up to 200 CPS. Number of columns can go up to 80 or 132, depending on character density—switch or data source selectable from 10 to 16.7 characters per inch. And all characters can be printed double width. The print head produces razor-sharp characters and high-density graphics with dot resolutions of 72X75 dots/inch under direct data source control.

Interface Flexibility

The three ASCII compatible interfaces (parallel, RS-232-C and current loop) are standard, so connecting your computer is usually a matter of plug-it-in and print. Also standard are: a sophisticated communications interface for printer control and full point-to-point communications, DEC PROTOCOL, and a 700 character FIFO buffer. An additional 2K buffer is optional.

When you're ready for a printer (or several thousand), look into the grafixPLUS DP-9000 Series from Anadex—you'll find an open and shut case for quality. Contact us today for details, discounts and demonstrations.

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With VERSAmodules, you're into the '80s and beyond.

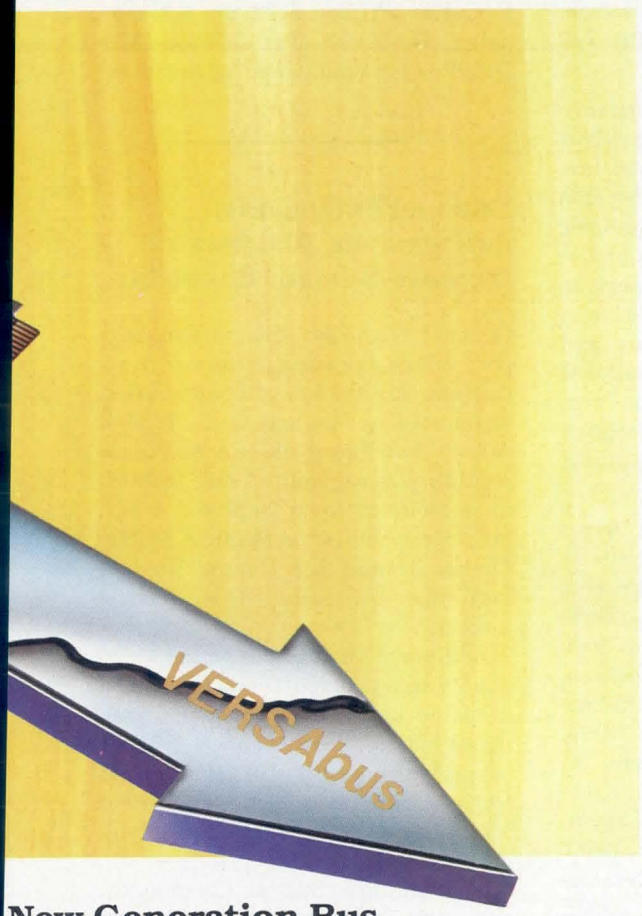
Most Powerful Microcomputer

The VERSAmodule Monoboard Microcomputer flagships the VERSAmodule family. Combining an MC68000 MPU, full VERSAbus interface, multiprocessor capability, substantial ROM/RAM, serial and parallel I/O and timer/counter functions, it's easily the most powerful single-board microcomputer yet offered. For designs requiring up to 128K bytes of ROM and RAM, plus two high-speed serial channels (up to 19.2K baud) and 40 lines of parallel I/O, this single board meets all system needs. Competitive approaches require two to four boards for the same capability, and, inevitably, more cost.

Total Software Environment

Many 16-bit applications, particularly in higher-performance, control-oriented areas, require a realtime, multitasking environment for efficient operation. By combining the ready-made RMS68K™ multitasking system software package with your VERSAmodule-based system, you can save the man-months of effort necessary to develop a system capable of managing resources efficiently in real time. Time and money saved can be used to apply your expertise to development of application programs.

to a total, 16-bit system VERSAmodules.™



New Generation Bus.

Supporting a mixture of 8- to 32-bit MPU architectures with high-speed transfer rates, VERSAbus offers a flexible, economical system bus ideal for industrial automation, communications or general business applications. VERSAbus is incorporated in the VERSAmodule chassis/card cage backplanes and willingly accomodates multiple processors. Designed-in ease-of-use for tomorrow's upgraded systems saves money by obviating major hardware and software redesign.

Inherent Reliability/ Maintainability.

VERSAmodule products support an unmatched level of system integrity. This includes reliability of the MC68000 with its advanced architectural features such as exception-processing and interrupt handling. These allow for graceful handling of common system problems such as bus error, illegal instruction, divide-by-zero, privilege violation, spurious interrupt, etc. This "soft-failure" capability alerts operating personnel and, in many cases, allows recovery before critical failure.

Reliability of VERSAbus-based systems is enhanced through power-fail detect and self-test features. AC-fail and power-down indication allow saving critical data in non-volatile memory through power outages. Self-test minimizes down-time by allowing manually-initiated self-test, when a problem is suspected, with failed boards indicated by on-board fault indication lights.

Versatile Development Support.

Unparalleled ease and efficiency in software development for VERSAmodules is yours through EXORmacs™ – a third generation 16/32-bit development system with state-of-the-art hardware architecture, advanced operating software and self-test capability. Pascal, FORTRAN and structured macro assembler allow choice of the language best suited to needs. A versatile, CRT-oriented text editor speeds up program preparation and modification. And a flexible linkage editor permits modular, top-down system development.

Again, less design time, lower cost and an earlier product operation date for a better bottom-line result.

Send for a new VERSAmodule brochure. Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 or call (602) 244-5714.

Take a big step into the '80s with Motorola VERSAmodules.

Innovative systems through silicon.

MOTOROLA INC.

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TO: Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

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City _____

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Module Permits Automatic Functional Testing of ECL Circuit Boards

Test system DTS-70 can perform functional stimulus and response testing of ECL circuits on their printed circuit boards. ECL board test module, developed by Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, provides fast edges and logic swings and eliminates the need to buffer the high speed signals on interfaces between the board and the test system.

When designing and testing PC boards using ECL devices, the possibility of distorted waveforms due to signal line reflections increases with the edge speed of the digital signal. Using the functional test system, the impedance between the ECL circuits in the tester and the PC board can be easily matched. The module has an output impedance of 75 Ω and is capable of driving transmission lines from 50 to 100 Ω. The 360 available pins can be wired with either coaxial cable or twisted pairs of wire. Crosstalk between adjacent signal leads is minimized through special ground planes for multilayer PC boards to insure excellent high speed grounds for ECL driver comparator boards. Maximum rise and fall times at the module interface are specified at less than 15 ns. The ECL test system guarantees noise immunity at less than 125 mV on its driver and 160 mV on the receiver.

U.S. price for the module (15 drivers/receivers) is $1000 each. Base price of the HP DTS-70 digital functional test system is $83,000.

Circle 361 on Inquiry Card

Conferences Issue Calls for Papers

Reliability in distributed software and database systems, enhanced performance in aerospace computers, and incremental motion control systems are the topics of conferences to take place during July and October of 1981. Prospective authors are invited to submit papers for consideration.

Sponsored by the IEEE Computer Society, the Symposium on Reliability in Distributed Software and Database Systems will be held July 21 and 22, 1981, in Pittsburgh, Pa. Long (6000 words) and short (3000 words) papers are being solicited. For consideration, submit 5 copies to Prof Charat Bhargava, Computer Science Dept, University of Pittsburgh, Pittsburgh, PA 15260, before Feb 15, 1981; Tel: 412/624-6448.

Computers in Aerospace Conference III, scheduled for Oct 26 to 28, 1981, at the Sheraton Harbor Island Hotel, San Diego, Calif, is sponsored by the AIAA with cooperation by the IEEE and NASA. The conference will provide an opportunity to access recent advances in computer technology, their application to embedded aerospace systems, and resulting improvements in overall cost effectiveness. Topics include embedded systems technology, program management, and design/development processes.

Digests of less than 1000 words should be submitted in triplicate by Mar 2, 1981, to the appropriate area organizer—Embedded Systems Technology: Maretta Holden, Support Software Mgr, Advanced Airplane Branch, MS/4A-29, Boeing Military Airplane Co, PO Box 3707, Seattle, WA 98124; Program Management: Susan K. McMahon, Technical Supervisor, MS/125-104, Jet Propulsion Laboratory, 4800 Oak Grove Dr, Pasadena, CA 91103; and Design and Development: Burton E. Hamilton, Chief, Scientific Programming, Hamilton Standard Div, United Technologies Corp, Bradley Field Rd, Windsor Locks, CT 06096. General inquiries concerning the program should be directed to Phyliss Rye, Technical Program Chairman, C.S. Draper Laboratories, PO Box 1541, Downey, CA 90241; Tel: 213/922-2936.

The Tenth Symposium on Incremental Motion Control Systems and Devices will be held at the Hyatt Regency-O'Hare, Rosemont, Ill, June 1 to 4, 1981. Sponsored by the Incremental Motion Control Systems Society in cooperation with Warner Electric Brake & Clutch Co, and the University of Illinois, Dept of Electrical Engineering, the conference will consist of tutorial papers as well as original contributions.

Theoretical and practical papers are being solicited for presentation. Areas of interest include step motors, machine tool control systems, computer controls, linear and ac/dc motors, clutch/brake devices and systems, and related incremental motion control applications. Authors should send a 500-word summary to Dr B. C. Kuo, PO Box 2772, Sta A, Champaign, IL 61820; Tel: 217/356-1523. Deadline for submission is January 1.

Channel Extensions, Performance Accelerator Increase System Capability

Channel extensions and software support and an extended performance accelerator for the 470 computer series, announced by Amdahl Corp, 1250 E Arques Ave, Sunnyvale, CA 94086, expand system capabilities and features in response to users' reported needs. Software includes the Multiple System Communication and Control product and the Universal Timesharing System.

Additional I/O channels on the 470V/7 and V/8 series computer systems will be available in 24- and 32-channel configurations. Added channels will be supported under VM with VM/Extended Channel Support software, and under MVS by MVS/Extended Channel Support package.

The Multiple System Communication and control package loosely couples two processors providing the advantages of a single-processor environment—with greater flexibility in job scheduling. A modified form of UNIX timesharing operating system Version 7, the Universal Timesharing System allows users to focus on objectives instead of system operating details. This package provides 470 system users with advanced functions of UNIX, many not previously available on a mainframe.

A 50% improvement in performance for the V/7B is provided by the performance accelerator, which increases its power to the level of the V/7. This unit assures users of necessary power when needed; the user pays only for those hours that the system operates in accelerated mode.

Circle 362 on Inquiry Card

Qantex
IMPACT PRINTERS

150 CHARACTERS PER SECOND

80/136 COLUMNS PER LINE

The Series 6000 is perfect for applications where high reliability at a low cost is a major consideration. Microprocessor controlled. Heavy duty operation.

Loaded with standard features. Tractor paper feed. Multi-part forms control. Top of form operation. Manual paper advance control. Built-in test capability. Cartridge ribbon. 9x7/9x9 dot matrix. Parallel or serial interfaces. Plus more.

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Introducing

CIRCLE 49 ON INQUIRY CARD

Electronic Laser Printer Combines Operations In Single Unit

An electronic printing system that is up to 40 times as fast as typical word processing printers and can send or receive a page of text in 3 s was introduced by Xerox Corp, Printing Systems Div, 701 S Aviation Blvd, El Segundo, CA 90245. The Xerox 5700 combines word processor printing, electronic mail, remote computer printing, and direct copying in a single unit to offer high quality printing and image versatility that would not be economically feasible for single-function office equipment.

Like the 9700, the system creates business forms electronically and prints them simultaneously with text on standard size plain paper. It also generates a virtually unlimited variety of type fonts and sizes, as well as signatures and other graphics, and can accept text from several word processing sources, communicate with other 5700 systems and computers, and be used as a copier.

In general, the unit has the same imaging characteristics as the 9700 electronic printing system, a high speed computer printer. It also uses a laser scanner to produce a pattern of very small dots, under the control of an internal computer. Its resolution is also the same—90k dots/in^2, sufficient to provide quality comparable to offset printing. Since each of the millions of dots that can be reproduced on a page is controlled—either placed on the page or not—it makes no difference what the programmed image is. It can be a box or logo as well as a numeric or alphabetic character. For the same reason, any font or size of type that is needed for an application can easily be made available.

A basic system is housed in two separate units. One contains the digital processor, user disc storage, system diskette station, and controller for the touch control screen, which is mounted on top of the unit. The other unit contains the imaging, printing, and output devices. Finishing stations have either two output trays, one for stacking output offset by job and one for stapling, or a large-capacity output stacker with job offsetting.

The touch control screen gives the operator control over all system operations and also supplies diagnostic information. Replacing the usual control panel, it displays a sequence of options in the form of pictures of buttons, and the operator simply touches the screen to initiate an operation. The screen is programmed for each possible configuration of the system. A help button produces a complete explanation for the operator if wanted.

Documents approach offset printing quality. Type sizes range from 6 to 24 point, up to 50 fonts can be stored, and a page can be printed either horizontally or vertically. Business forms are created electronically, stored in digital form, and converted to printed images by the laser scanner. Printing can be done on both sides of a page.

The system accepts input from recorded cassette, magnetic card, or floppy disc produced by a word processor. Both Xerox and IBM magnetic media can be used. In addition, the 5700 accepts input from Xerox and IBM communicating word processors.

For electronic mail applications, a network of systems can be set up and programmed to send documents automatically at 960 chars/s to designated locations selected by the operators. The documents received, up to 1000 pages, are stored in individually addressed electronic mailboxes, to be printed on demand by the recipient.

Pricing of the 5700 depends on the features chosen. Purchase price of the lowest cost system is $66,300 in the United States; this would include either a word processor media station or computer communications option. A typical system, including two magnetic media stations, communications, copying facilities, forms compiler, and automatic stapler, has a purchase price of $91,050.

Circle 363 on Inquiry Card

Intelligent OCR Units Interface to Word Processors

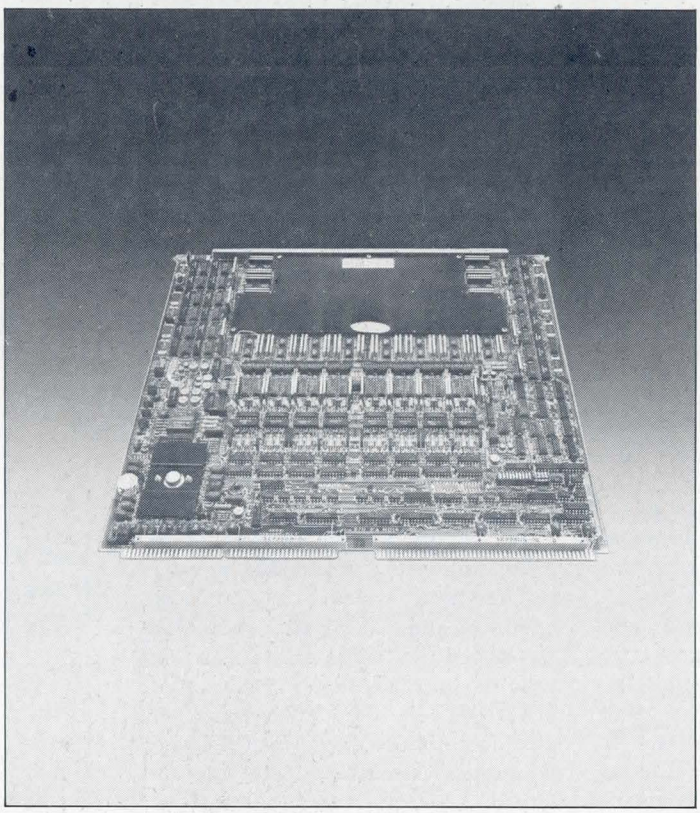
OCR page readers models TR3 and TR2S scan text at 2 lines/s, sufficient to permit recording of from 2 to 3 full pages/min. The readers, from Hendrix Electronics, 670 N Commercial St, Manchester, NH 03101, are readily interfaced with all available word processing systems.

TYPEREADER TR3 recognizes typestyles from a group that includes Courier 12, Courier 72, Letter Gothic, Prestige Elite, and Prestige Pica, as well as OCR-A, OCR-B, and Hendrix Gothic. The unit can handle such variations of Courier 72 as Correspondence, Fraction, Legal, Legal Fraction, Legal 017, and American Standard. The machine can be configured with up to four typestyles, automatically determining changes in typestyle and pitch from page to page without operator intervention. Skip-Scan is another standard feature which allows the unit to skip material to be deleted such as line art, signatures, and equations. Input forms and header sheets are eliminated by an automatic margin detection feature.

Performing all critical OCR functions needed to increase the performance and productivity of text editing terminals, the TR2S is similar to the TR2 but removes the sheet feeder, which is not necessary in low volume application. Options, however, include recognition of OCR-A, OCR-B with accented characters, or Hendrix Gothic, plus the ability to recognize underscored copy. A dual-output option allows the OCR unit to be linked with multiple computers, word processors, or communications devices. Also available is a display terminal for Telex/TWX and direct message entry.

Circle 364 on Inquiry Card

AMPEX MEMORY FOR DG NOVA™ 64K BYTES.



Ampex gives you proven, non-volatile 64K byte memories on single boards. They're specifically designed to work with the popular Nova 1200 and Nova 3 Series of minicomputers from Data General. And they're also compatible with the 32K byte boards we've sold by the thousands.

The Ampex ARM 1280 64K Byte Single Board Memory saves three ways:

SAVES SPACE—This single board has twice the memory capacity of previous boards, giving you more memory in less space.

SAVES MONEY—The ARM 1280 64K Byte Memory is priced less than two 32K byte memories, giving you more memory for the money.

SAVES YOUR CPU—This simple method of upgrading your memory capacity and increasing your computer's performance helps extend the life of your CPU.

The Ampex ARM 1280 is the most reliable memory you can use. And don't forget, you won't lose data in the event of a power failure.

For more information, write Andy Nizynski, Ampex Memory Products Division, 200 North Nash Street, El Segundo, CA 90245. Or call 213/640-0150.

AMPEX

MAKES THE DIFFERENCE.

™Data General

CIRCLE 50 ON INQUIRY CARD

Small Business Computers Expand to Multiterminal Systems

Series 100 small business and Series 200 multiterminal computer systems are built around the Z80A microprocessor and can be configured with 4M bytes of diskette capacity and up to 28M-bytes storage on hard discs. The Z80A CPU/memory board allows the systems, from CMC Marketing Corp, 10611 Harwin, Suite 406, Houston, TX 77036, to operate at a full 4 MHz with no wait states.

Features of 100 series units include a Two-X disc controller capable of handling two Shugart or Qume 8" (20-cm) disc drives. Automatically determining the density formatted, the unit can read all IBM single-density discs and run on IBM double-density. The multi-I/O board provides up to four serial ports with full handshaking and RS-232 interface. There are five parallel I/O ports as well as optional interface and software drivers for parallel printers.

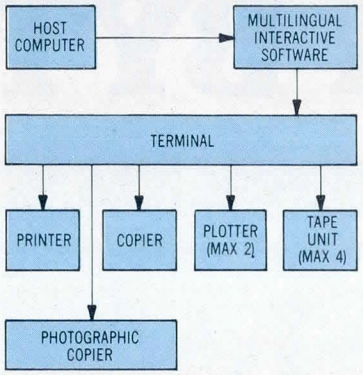
Multiterminal 200 series units add a CPU/memory board for each additional workstation to isolate functions and prevent one board's failure from interfering with the rest of the system. One CPU board serves as master I/O processor, storing and executing the MP/M operating system and arbitrating bus usage among satellite boards.

An 8-user system with hard disc requires 13 boards: master CPU/memory board, 2 multiuser I/O boards, 8 CPU satellite boards, hard disc controller, and floppy disc controller. These boards provide 576k of RAM, 8 independent CPUs, single- and double-density control for 4 floppy drives, 14M to 28M bytes of Winchester storage, 8 terminals and 2 printers, and a realtime clock.

All systems can use industry standard CP/M 2 and MP/M operating systems as well as Microsoft BASIC, the Magic Wand word processing package, and Data Base Management Software. Many applications packages are available.

Circle 365 on Inquiry Card

Word Processing System Communicates in 32 Different Languages



Computer Systems Consultants' software oriented ML-32 generates documents in up to 32 languages selectable from keyboard. Machine provides full graphics plus word processing capability, and interfaces to virtually any host computer

ML-32, a multilanguage CRT based word processing system, makes 32 languages resident in the system accessible to the operator under keyboard command. Developed by Computer Systems Consultants, Inc, 225 Main St, Chelmsford, MA 01863, the interactive system permits operators to display select sets of languages simultaneously on the screen.

The software oriented system harnesses sophisticated electronics in a user oriented design for generating single documents or complex forms in 1, 2, 6, or 32 languages at the same time. The machine provides full graphics capability in color (CML-32) or black and white (ML-32), and ability to dynamically scroll several pages of text without interrupting the host computer.

Designed to interface with any host computer system, the system displays 34 80-char lines on a high resolution raster display. It provides 80 programmable function keys and has flexible disc, cassette, and hard disc storage capability. Telecommunications capability is supplied via RS-232, IEEE (GPIB), and IBM 3270 ports. Hardcopy output can be provided on 8.5 x 11" (21.5 x 27.9-cm) dry silver paper or as variable size XY camera-ready plots.

Languages with full character sets currently on the system include English, Greek, Greek/Accent with special characters, Arabic, Hebrew, Russian, Japanese, Chinese, German, French, Welsh, Italian, Hungarian, Dutch, Norwegian, Swedish, Turkish, Spanish, Portuguese, Latin, Tagalog, Rumanian, Korean, Icelandic, Gaelic, Danish, Albanian, Ukranian, White Russian, Bulgarian, and Serbian. Bold and large characters are provided for each; ruling characters are also available.

A black and white unit has a purchase price of $17,500; a color unit costs $26,000.

Circle 366 on Inquiry Card

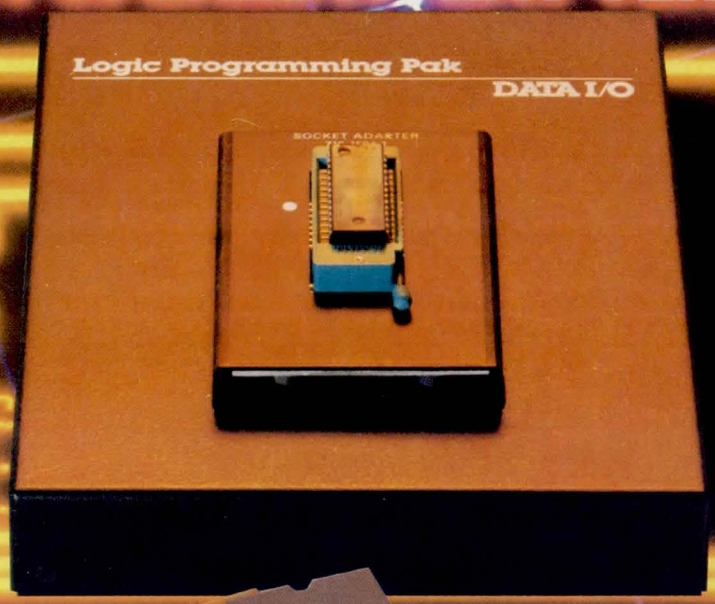
Entry Level Systems Package Hardware With Application Software

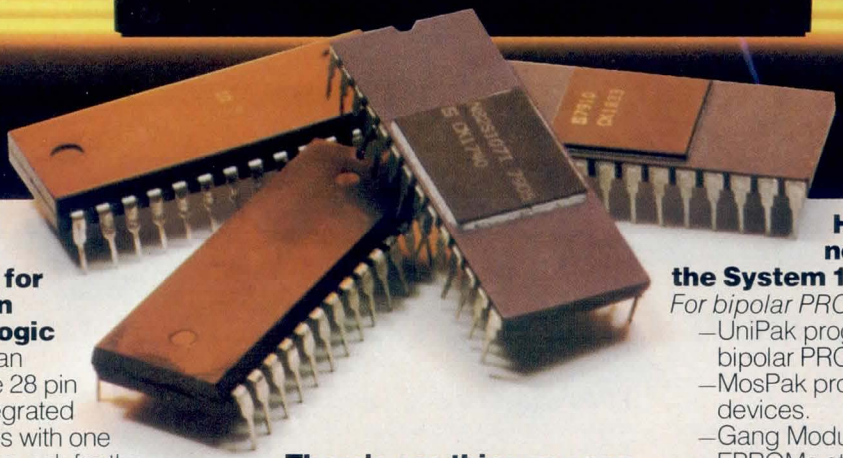
M1000 is a low cost entry level addition to the Synergist™ packaged business system line. Data General Corp's General Distribution Div, Rt 9, Westboro, MA 01581, combines processors and peripherals with software for general business or distributor applications in the unit. Prices range from $10,950 to $25,000.

Models 10, 15, and 30 support up to four display terminals, 52.4M bytes of online data storage, and several printer and communications options. Based on a 64k-byte microNOVA processor, these models run interactive BASIC under Digital Computer Controls' Extended Operating System. The operating system uses English-like operator instructions and prompts and has a copy utility to perform disc to disc data and software backup.

Circle 367 on Inquiry Card

THE PIONEERS OF LOGIC PROGRAMMING HAVE JUST OPENED A NEW TERRITORY.





Data I/O offers a new System 19 programming pak for all Signetics 28 pin Integrated Fuse Logic devices. Now you can program the complete 28 pin family of Signetics integrated fuse logic (IFL) devices with one intelligent programming pak for the Data I/O System 19 and 17.

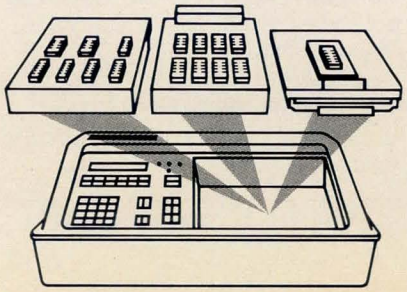
The new pak allows direct keyboard input of logic variables. There's no need to write software or use a computer to develop your programming data. You can work directly from the System 19 keyboard or a CRT terminal.

Data I/O can keep you on the forefront of programmable logic. At Data I/O, we believe that programmable logic is the wave of the future. Logic devices like the PAL,™ FPLA, FPRP, FPLS, FPGA and PMUX offer the designer the unique advantages of real estate savings, design flexibility, and speed in bringing a product to market. They also reduce "hidden" product costs through simplified assembly and lower inventory costs.

When we introduced our first logic programmer six years ago, we began our commitment to logic. Our new Systems 17 and 19 were developed with an eye to logic programming as well as bipolar and MOS device programming.

There's one thing you can depend on when you explore the possibilities of logic programming. Data I/O will be there with new ways to program new devices on programming systems that exist today. That's the theory behind our Systems 17 and 19—offer designers a standard mainframe and enable them to maintain state of the art programming capability by simply adding programming paks.

In the future we will be introducing new capabilities to complement the System 17 and 19 that will offer design engineers even more flexibility and enable them to program a larger variety of logic devices.



Here are the paks now available for the System 19:

For bipolar PROMs and EPROMs
- —UniPak programs more than 200 bipolar PROMs and MOS devices.
- —MosPak programs single MOS devices.
- —Gang Module programs eight EPROMs at once.

For individual PROM families
- —More than 40 approved programming paks.

For logic devices
- —Logic Programming Pak handles Signetics IFL 28 pin family.
- —Individual programming paks for more than 30 different logic devices.

Let us show you the future. The Data I/O interactive logic pak for Signetic IFL devices is available now. To make arrangements for a demonstration, or to get your free copy of our 32-page book on PROM and logic device programming, circle reader service number or contact Data I/O, P.O. Box 308, Issaquah, WA 98027. Phone 206/455-3990 or Toll Free 800/426-9016.

DATA I/O

CIRCLE 51 ON INQUIRY CARD

STR® technology for high data integrity. Three major tape formats for design flexibility.

We don't forget the OEM's needs.

The STR-810 digital recorder is designed for data logging, data acquisition and as a system loader. Using either the 3M DC-300A or DC-300XL cartridges, packing density is 1600 bpi, for respective data capacities of 2.3M bytes and 3.4M bytes per cartridge, using four tracks. Features include microprocessor-controlled tape movement and read/write electronics. For maximum versatility, interfaces include RS-232 and IEEE-488. Or, using control and status lines available, you can interface to specific microcomputers such as LSI-11 and 8080. EPI's optional ANSI X3.56 formatter, with NRZI or phase-encoded personality cards, turns the 810 into a plug-in component for industrial instrumentation and mini/microcomputer-interfaced peripheral markets. Price: $756 in quantities of 100. **STR-STREAM** is a high-speed, high-capacity version of the 810 designed for Winchester disc backup. Density is 6400 bpi for 17M bytes capacity per cartridge. Features include advanced head design, MFM formatting and compatibility with 8" or 14" discs.

CIRCLE 108 ON INQUIRY CARD

EPI's STR-610 is a compact, low cost digital recorder that's ideal for use with POS terminals, smart CRT terminals and as a general peripheral for mini/microcomputer-based systems. The 610's recording density is 800 bpi for a capacity of 168K bytes/track, using a two-track 3M DC-100 mini-cartridge. Formatting is ANSI Standard and interfacing is parallel, with a variety of options. Price: $280 in quantities of 1,000. **The STR-LINK III** is a high-speed (9600 baud), portable program loader that uses the STR-610's drive system and shares the same specifications. It is used as a field service tool for diagnostic work or as a peripheral in a mini/microcomputer system. STR-LINK III uses a serial RS-232 interface for data communications or data terminal applications, and it can be controlled through RS-232, ASCII control codes, or manually. Price: $1,561 in single quantity.

CIRCLE 109 ON INQUIRY CARD

STR-LINK II is EPI's proven medium-speed (1200 baud) universal portable program loader for programmable controllers and process control systems. Using a standard cassette, it features switch-selectable transmission modes for maximum flexibility. Price: $1,735 in single quantity.

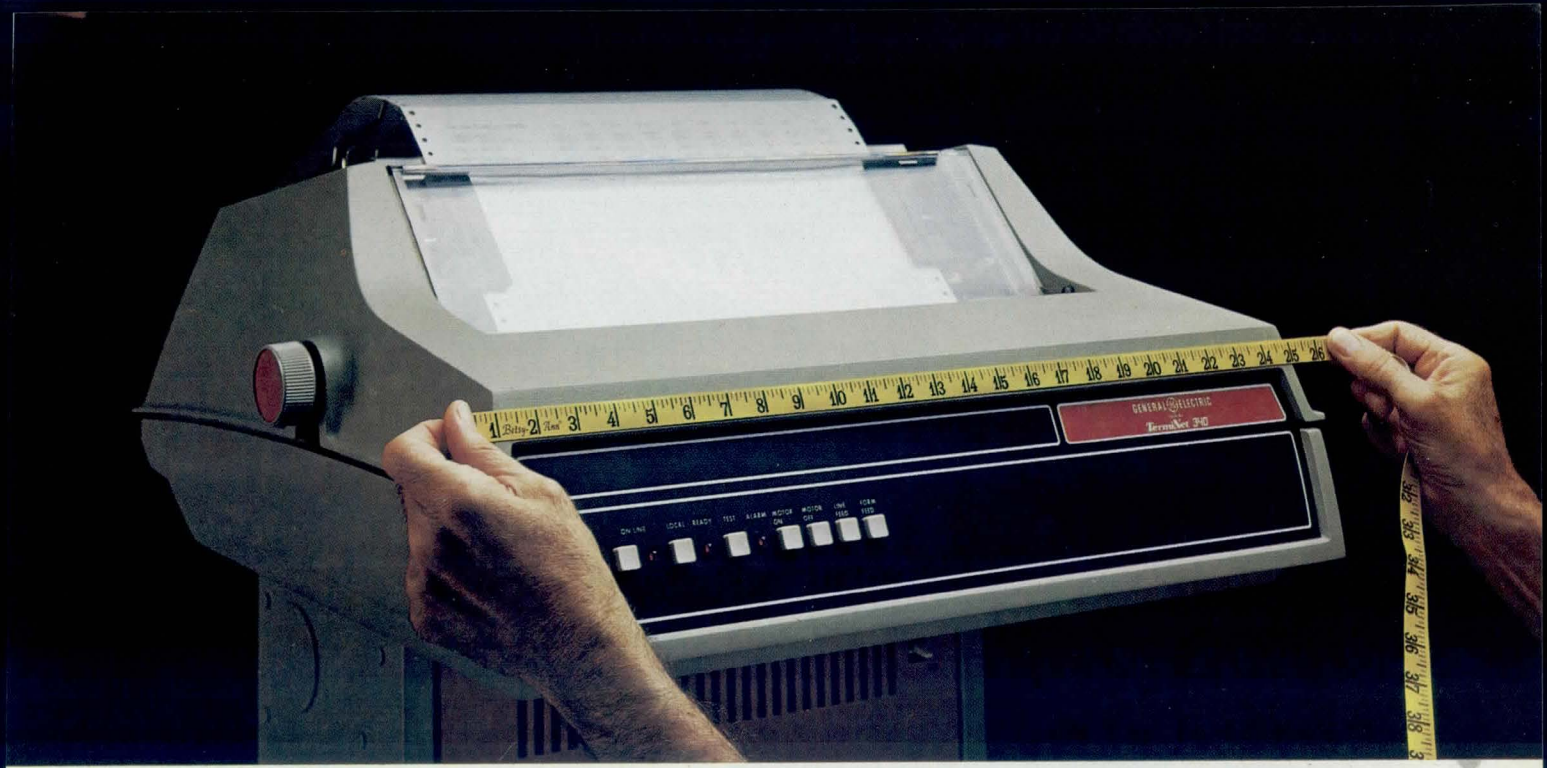
For maximum design freedom, proven reliability and high data integrity through Speed Tolerant Recording technology, remember EPI—the company that doesn't forget the OEM's needs. For more information, contact Electronic Processors Inc., P.O. Box 569, Englewood, Colorado 80110. Phone (303) 761-8540.

E0/3

CIRCLE 110 ON INQUIRY CARD

Let EPI remember for you.

ELECTRONIC PROCESSORS INCORPORATED



Solid engineering and 340 lpm speed make the TermiNet 340 a more rugged, productive line printer.

Any way you measure them, TermiNet® 340 line printers are more productive performers

Don't let the compact size of the General Electric TermiNet 340 line printer fool you. Because no matter how hard you work it, it won't quit on you. It's that tough, that dependable and that much better than typical line printers. And it's available now.

A true 100% duty cycle printer

Unlike ordinary line printers, the TermiNet 340 can take the punishment of the broadest range of operating environments—from front office to factory floor—without complaining. The key reason? A tough, ruggedly engineered design. As a result, it keeps on performing under tough-use conditions when other line printers would sputter and break down.

Engineered to stay on the job.

From top to bottom, the compact TermiNet 340 line printer is engineered with long-life components designed to keep the printer on-line. And businesses on schedule.

One reason: extra-thick, heavy-duty, environment-resistant materials chosen for the base and housing. Together, they provide this rugged printer with the impact strength, dimensional stability and resistance to adverse environments needed to keep working.

More reasons: print and ribbon systems that won't wear out prematurely and won't cause the problems other line printers do. Which is why the proven rotating-belt print system will last billions of characters. And why the ribbon cartridge will maintain very high print quality for at least 100 million characters.

Fewer service problems keep it working longer

The fact is, TermiNet 340 line printers are such productive workers, they require very little attention and very little maintenance once they're up and running. Should service be needed, you can count on getting these printers back on-line in a hurry. That's because of convenient self-test features that make troubleshooting easy and fast. And because of a responsive nationwide service network that keeps downtime to a minimum and operating costs low.

Find out for yourself. Mail the coupon today and see why so many companies have chosen the more productive TermiNet 340 line printer to get their work done.

Quality that will make a lasting impression

GENERAL ELECTRIC

CIRCLE 52 ON INQUIRY CARD

Mail today to:
J. Walsh,
General Electric Company,
TermiNet 794-43,
Waynesboro, VA. 22980
Telephone: (703) 949-1474.

☐ Send me more information about the TermiNet 340 line printer.

☐ Have a sales representative contact me.

☐ I'm also interested in a TermiNet 340 line printer demonstration.

Name _____

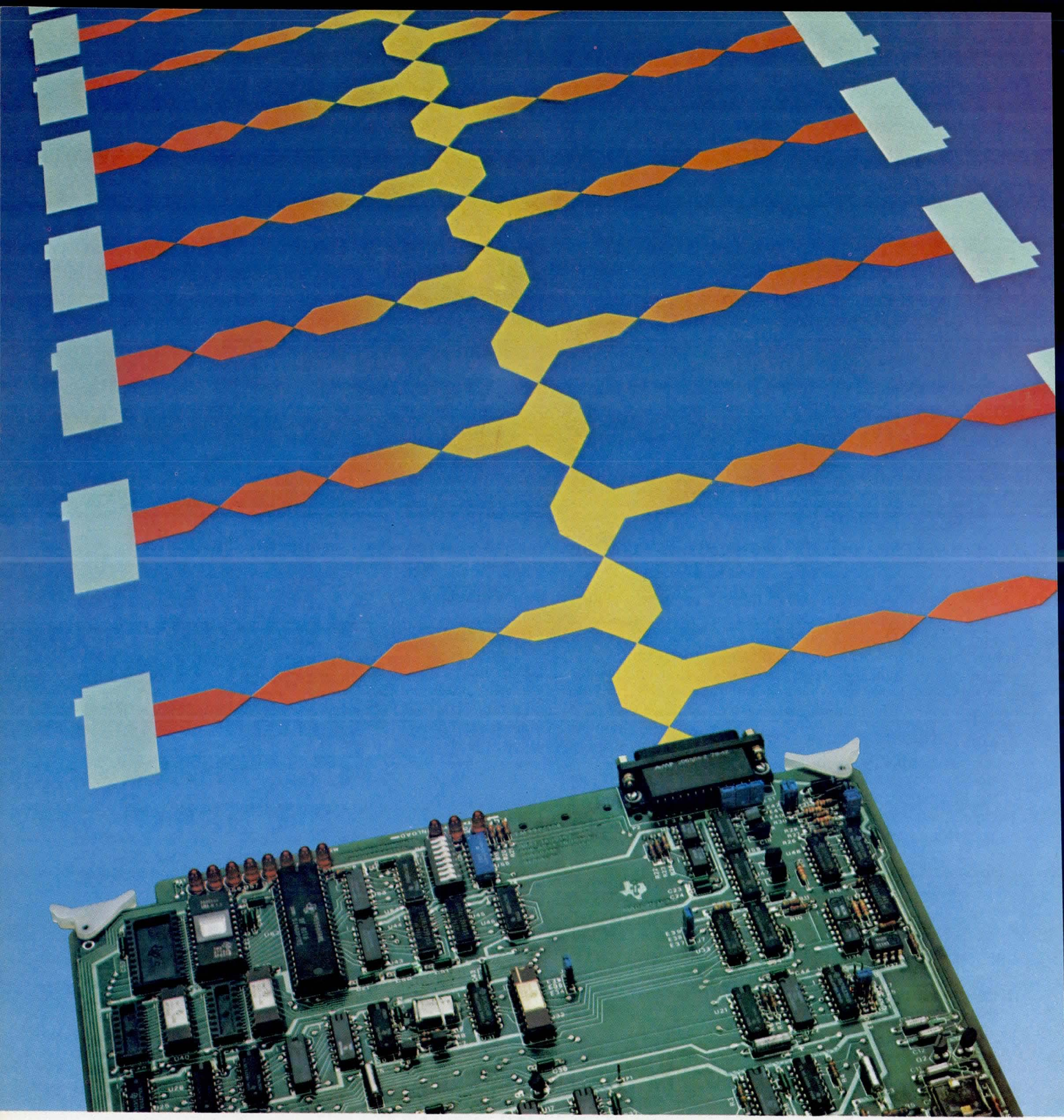
Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Telephone _____



New Industrial Communication Module: Multi-point. Long range. Simple connect. From Texas Instruments.

A new development from TI extends industrial communication to more points. Over greater distances. At less cost.

The unique, new TM990/308 Industrial Communication Module relieves a host CPU of all synchronous communication tasks. Communication, in the multi-drop mode, can be with as many as 31 other compatible TM990 systems. Over a range as great as 10,000 feet. No modems necessary — over twisted-

pair lines which substantially simplify interconnects and reduce installation costs. The interface is optically isolated (1500 V RMS).

Point-to-point communication over an even longer distance is achieved using Bell 208 type synchronous modems.

Either way, the 308 module is an intelligent interface, with processing handled by an on-board TMS9980 microprocessor. Firmware supports address decode, down-load command decoding, and other primitive functions.

New Communication Expander Module

A second new TI module — the TM990/307 — allows communication with up to four devices such as terminals or modems (see diagram at right). It provides four RS232C EIA ports using standard RS232 connectors, and one port can be RS422. A Bell 801 automatic calling unit interface is on board. Optionally, four channels of synchronous communication are possible by changing on-board devices to synchronous controllers. A loopback permits self-testing.

Demonstration Software

Demonstration software for either of the new communication modules will enable the user to check for proper operation quickly and easily. The software listing will also facilitate application programming.

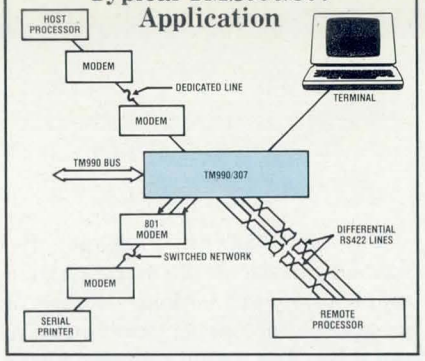
Software Support

Coming soon for the new TM990/308 module: a Data Communication Software package. One of TI's new Component Software Series, it supports point-to-point and multi-point communications. Operating with TI's Realtime Executive, the DCS package will reduce software costs substantially by providing a library of statements common to most programs.

The HDLC Data Communication Software package provides networking capabilities by interprocess communication. TM990 systems, 990 minicomputers, and PM550 controller systems may be interconnected.

The HDLC package offers programmable features like character width, parity, start stop bits, and baud rate. Each port can be programmed independently to a particular priority level, special control character set, etc.

Typical TMS990/307 Application



TM990 Series Microcomputer Modules

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TM990/101M
TM990/180M
TM990/1481

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TM990/203 Dynamic RAM
TM990/206 Static RAM

Mass Storage:
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TM990/211 Bubble Memory
TM990/303A Floppy Disk Controller

Digital I/O Modules:
TM990/305
TM990/310

Analog I/O Modules:
TM990/1240
TM990/1241
TM990/1243

Communication Modules:
TM990/307
TM990/308

Speech Module:
TM990/306

Industrial AC and DC I/O Modules:
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Fast fit: The modules are based on the memory-to-memory architecture common throughout TI's pioneering 16-bit 9900 Family. This advanced architecture, in combination with the rich 9900 instruction set, is particularly well-suited to industrial control applications, simplifying both hardware and software.

Fast help: Demonstrations of the TM990 modules can be arranged at local TI distributor Systems Centers.

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From a standpoint of time and money saved, reliability and performance gained, TI's TM990 Series modules are an extremely efficient and economical solution to design problems. For full particulars, get a copy of the TM990 Series brochure. Call your TI distributor, or write Texas Instruments, P. O. Box 1443, M/S 6404, Houston, Texas 77001.

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CIRCLE 53 ON INQUIRY CARD

SOFTWARE

Business System Uses Associative Index Method For File Access

DATASHARE 6 business timesharing system allows simultaneous execution of 24 applications programs. In the release, Datapoint Corp, 9725 Datapoint Dr, San Antonio, TX 78284, has made substantial improvements in speed and in user capabilities, and has incorporated Associative Index Method (AIM) file access software. The system runs on 1800, 3800, 5500, or 6600 series processors and can be used standalone or as part of an ARC dispersed system.

AIM software revolutionizes the method of programming data processing solutions. Through the use of content addressable files, data files need only contain data because the software eliminates the need for the wide variety of index pointers, links, networks, and trees. With the software, a simple telephone directory can reside on disc exactly as it appears in the book, yet provide direct access to subscribers by telephone number and combination of first, middle, or last name; street names or numbers; or fragments of any of these. A parts list can provide not only all of the parts for each product but all of the products which use any specific part or set of parts, without resorting to complex implosion lists. The content addressable technique allows the key to be defined at the time of inquiry, not when the file is set up by the system designer.

In addition to file access capabilities, AIM software also offers a number of user convenience features. Disc space is conserved because only one index is required on all keys for a particular record. Yet data files can be indexed so that each record can be accessed by a large number of multiple keys. Up to 64 fields can be defined for each record in a single file, with the file occupying only about 14% of the disc space occupied by the data file it indexes. A single index for multiple record keys also facilitates index updating, since only one index update is required to update all keys.

The DATASHARE package also doubles the size of the user data area, supplying more working storage in programs for string and numeric variables. The utility partition supervisor can operate with the system to optimize large memory machines, and the buffer manager can use larger memory, is more efficient, and extends to more data types.

Circle 368 on Inquiry Card

Mapping Software System Designed in Modules For Flexibility

The modular ODYSSEY mapping software system is capable of analyzing geographic data, selecting cartographic formats, and generating publication quality thematic maps. Available from Integrated Software Systems Corp, 4186 Sorrento Valley Blvd, Suite G, San Diego, CA 92121, the package consists of a basic system with five options developed by the Laboratory for Computer Graphics and Spatial Analysis of Harvard University. Written in FORTRAN, all modules use the same command language and file structure thus facilitating upgrade as requirements become more complex.

In operation, the system combines geographic data files with cartographic data bases (counties, census tracts, etc) to produce a variety of 2-dimensional shaded polygon maps and related annotation in high quality type fonts. Maps can be drawn with line or dot shading, black and white half-toning, or color shading. Color or shade values are identified with a legend or histogram, and the user has total control over size and scale.

Flexible command language interpreter, designed for interactive or batch use, offers comprehensible syntax, a high level of tolerance (free format, abbreviations, etc), graceful recovery after user error, and built-in tutorial aids.

Device interfacing technology, a feature of the package, enables interfacing to all graphics devices, including CRT displays, pen plotters, electrostatic printer/plotters, computer output microfilm units, and art generators for camera-ready artwork.

The five options available for upgrading the ODYSSEY system are 3-dimensional perspective map drawing, geographic analysis, map file modification, and manual and automatic map file creation. Price for the system is $20,000 with options ranging from $5000 to $13,000.

Circle 369 on Inquiry Card

Pascal Macro Assembler Provides Portability

A macro assembler, written in ISO standard Pascal, can be modified to run on an arbitrary host computer while assembling code for the target machine, and can be customized to operate as a cross or as a native assembler. Dependencies on number formats in both host and target computers have been separated from the main body of the assembler to allow portability. In addition, the assembler, available from Advanced Computer Techniques Corp, 437 Madison Ave, New York, NY 10022, is not burdened by the overhead of a general purpose meta-assembler.

When the assembler is modified for a specific target computer, the source form can be tailored to conform to existing assemblers utilized by that machine. It also provides specific and descriptive error messages making it easier for the user to make corrections.

Operating on a 2-pass basis, the assembler scans source code twice, and handles macro and conditional assembly functions as part of the first pass to speed processing. A cross reference listing can be made available as a third pass.

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CIRCLE 54 ON INQUIRY CARD

SOFTWARE

Application Package Serves as Interactive System Design Tool

Specifier allows application systems to be developed at a computer terminal rather than at a desk. Whereas design work has traditionally been handled by coding pages of input and then keying data onto punch cards or disc for validation, the system developed by Genasys International, Inc, 17 E 45th St, New York, NY 10017, provides 1-step data entry and actively prevents the user from making syntax errors.

The package prompts the analyst or user through the process of describing the system to be developed, including details of reports and screens that are wanted, where data needed for these inputs can be found, and what files, data base segments, and procedures are needed to transform the available data into the desired results. By itself the system can then create hardcopy design documentation for review by user and analyst. However, it can also be used to build a data base within Genasys' system development software to generate COBOL or PL/1 source programs for the system just designed, and final documentation once the programs are tested and debugged.

An interactive "help" facility lets those unfamiliar with system operation page electronically through a Genasys/Specifier manual. Menu selection options help the user find the necessary information, then return to the data entry operation at the point where the search began, or at any other point specified.

The software has been developed as a transaction processing application under the command level of CICS/VS. It can be used, concurrently with other CICS applications, under any operating system environment that supports the IBM teleprocessing monitor.

Circle 371 on Inquiry Card

Software Package Enables Minicomputers to Emulate Batch Terminals

Naked Mini computers can function as remote job entry terminals to any host supporting IBM 2770, 2780, or 3780 protocol with the software emulation package recently announced by Computer Automation, Inc, 2181 DuPont Dr, Irvine, CA 92713. This enables users to get both network compatibility and local processing.

Operating under binary synchronous communications protocol makes the mincomputer based systems appear to a host as an IBM remote batch terminal. The emulators execute under the realtime executive on Naked Mini 4/10, 4/30, 4/90, and 4/95 processors equipped with I/O distributor card, bisynchronous intelligent cable interface, and optional synchronous modem. □

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CIRCLE 56 ON INQUIRY CARD

CURRENT TECHNIQUES IN FACTORY DATA COLLECTION

William S. Holderby

Autech Data Systems

1301 W Copans Rd, Pompano Beach, FL 33064

Collection of data associated with the operation of a factory or industrial system is not a recent development. For years management has tracked personnel, individual jobs, costs, and lag times within the industrial environment—usually by systems based on amassing paper. Because such systems are labor intensive, the costs have increased substantially.

Advent of the computer, however, has enabled many firms to switch over to a computer based management information system (MIS) that provides the data needed to forecast the factory needs and more fully distribute its resources. Yet much of the data potentially available from the factory floor must still be gathered by the paper method, if it is gathered at all. This limits the effectiveness of the MIS and could jeopardize the correctness of the decisions reached by management.

Basic Problem Areas

Five fundamental areas must be considered when examining the resources and potential of the shop environment. In effect, these are *inventory*, the parts needed to build the end products; *personnel*, the labor force required to assemble the products; *job status*, data on jobs currently in production; *work station utilization*, division of the factory into stations with finite throughput times; and *work stoppage*, disruptions of work flow. Ability to obtain this information rapidly and to disseminate it to management is the key to any decision on whether or not to set up an information tracking system. It must be recognized that humans are not always meticulous in their responsibilities to update such a system and cannot be depended on to provide the necessary information. In many instances, automatic update of such data is preferable, particularly in such cases as detection of failed equipment or operator error, where it is imperative that there be no delays in providing system inputs.

Introduction of the microprocessor based smart terminal has provided a means for the foremen and other shop floor personnel to input information concerning the shop activity. However, data inputs are often made at the operator's discretion and do not always reflect either the exact nature of the operation or the time periods in which the operations occurred. This is not necessarily due to negligence on the part of the operator; many times the terminal will be in use and the operator will have difficulty accessing the system at all.

A smart terminal used in a factory environment for access to the factory's computer system is called a factory data terminal (FDT). It requires no operator knowledge of the computer methodology. Most frequently data are input in one of three methods: *keyboard*, in which the operator types data entries utilizing either standard typewriter keyboards or specially configured keyboards designed to ease the plight of those operators who cannot type; *badge or card reader*, which offers rapid data input and allows limitations on who is permitted to use the terminal; and *bar code reader*, also a fast method for the operator to input pertinent data.

Although these methods are adequate for most applications, the terminal configuration may not be able to cope with certain constraints placed on the system. Inability of the system to accept operator input without long delays during the interrogation can cause the operator to lose interest and wait until a period of lessened activity. In addition, the need to input data concerning large quantities of parts or repetitious data can result in operator carelessness and inaccuracies. Even more critical, the operator may not know enough about process quality to input the information necessary for material savings.

In reality, the FDT has been limited in its application. The very intelligence valued in smart terminals is being underutilized because the computer already performs those tasks requiring repetition and exactness. Therefore, the application of FDTs to process monitoring and control requires modification to the basic FDT configuration (Fig 1).

(continued on page 94)

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CIRCLE 57 ON INQUIRY CARD

Hardware Design

Modification of the FDT requires changes to the hardware and revisions to the terminal firmware concepts. Principal changes in the hardware design are made to enable the terminal to measure analog inputs, to direct control functions with analog outputs, to monitor discrete binary changes with digital inputs, and to provide state changes with digital outputs. It is therefore necessary to augment the terminal architecture with four functions not found in operator-only FDTs: analog to digital conversion (ADC), digital to analog conversion (DAC), digital input, and digital output.

The ADC samples analog signals and converts them to digital information for processing by the digital computer, while the DAC converts digital information from the computer to analog signals (voltage or current). Digital inputs require state transitions to occur and are stored in registers; digital outputs permit the computer to initiate a state change between any two preset levels. Inclusion of these four functions to the basic architecture permits the terminal's microprocessor to monitor process functions.

Monitoring of analog and digital information requires that another feature, the watchdog timer, be added to the terminal. This is best described as a programmable timer that functions under microprocessor control to delineate a measurable length of time in which an event or events must occur. For example, a motor must arrive at a certain speed within a prescribed period before another event is initiated. If it does not do so, the timer interrupts the normal microprocessor program operation and notifies it that the event did not occur. In practice, the device is a bank of timers that may be programmed to operate independently over various base times, such as 1 ms to 1 min.

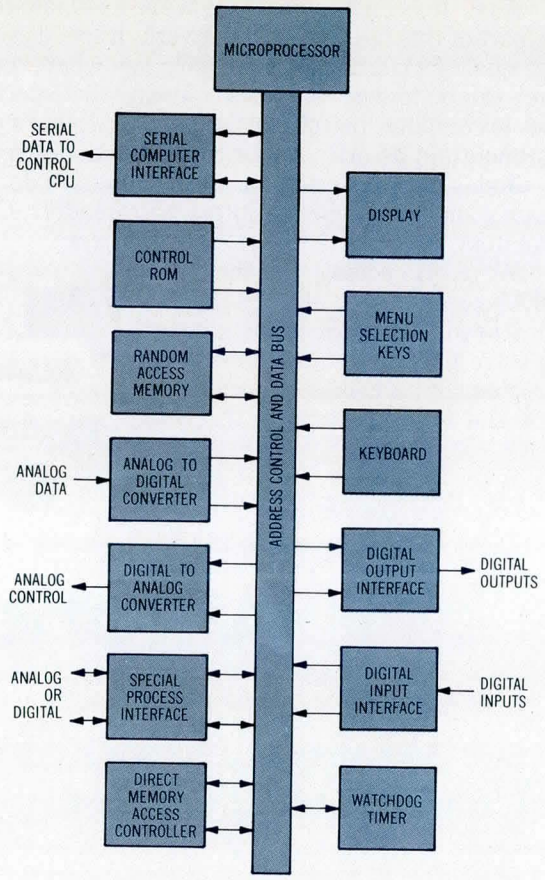

Fig 1 Architecture for FDT capable of interfacing both operator and process. Terminal has sufficient capabilities to allow multitasking of operating system. Keyboard, display, and menu selection keys permit operator to access and input information to computer system. Terminal operating system is located in ROM and utilized RAM for storage of data and system parameters. Process I/O board configuration is dictated by requirements of system design

Firmware Design

Configured with these functions, the FDT is capable of measuring process parameters such as those shown in Fig 2. However, terminal firmware must itself be capable of utilizing these capacities before the terminal can function. Software and firmware concepts are the most significant factor in the design of such a terminal and terminal network. To more fully understand the FDT, it is imperative that the terminal network and protocol be understood.

A typical factory data collection network (Fig 3) consists of three basic parts: the main central processing unit (CPU), which supports the MIS; the network or frontend processor (FEP), which provides the necessary communications to the terminal via a network by transmitting and receiving data over one or more serial communications links, and dictates the format of the protocol between itself and the various terminals; and the FDT. Main CPUs are usually mainframe computers capable of supporting large operating systems that process extensive data and service more than one user. Network CPUs or FEPs communicate with main CPUs over a high speed serial communications link. The various FDTs are located in areas dispersed throughout the industrial complex and communicate over a serial communications link to the FEP.

Protocol also can be subdivided, into two basic mutually exclusive definitions: electronic and software. Electronic protocol defines the methodology used in electronically transmitting and receiving the binary signals required to pass mutually meaningful information or intelligence between two computers. This definition extends to the signal medium voltage or current and set standards such as high level data link control (HDLC), binary synchronous, RS-232, current loop, and other less widely accepted methods. In addition to the transmission medium, the protocol defines the number of bits per word, the bit format, the number of words per block of information, and the error checking employed. For purposes of this discussion, electronic protocol can be defined as any of the accepted standards capable of transmitting and receiving 8-bit data words and operating in a multiterminal communications environment.

Software protocol is a somewhat more nebulous quantity, with few definition guidelines, because various vendors define their individual protocols differently. The most commonly used protocol conforms to a 7- or 8-bit ASCII format

(continued on page 96)

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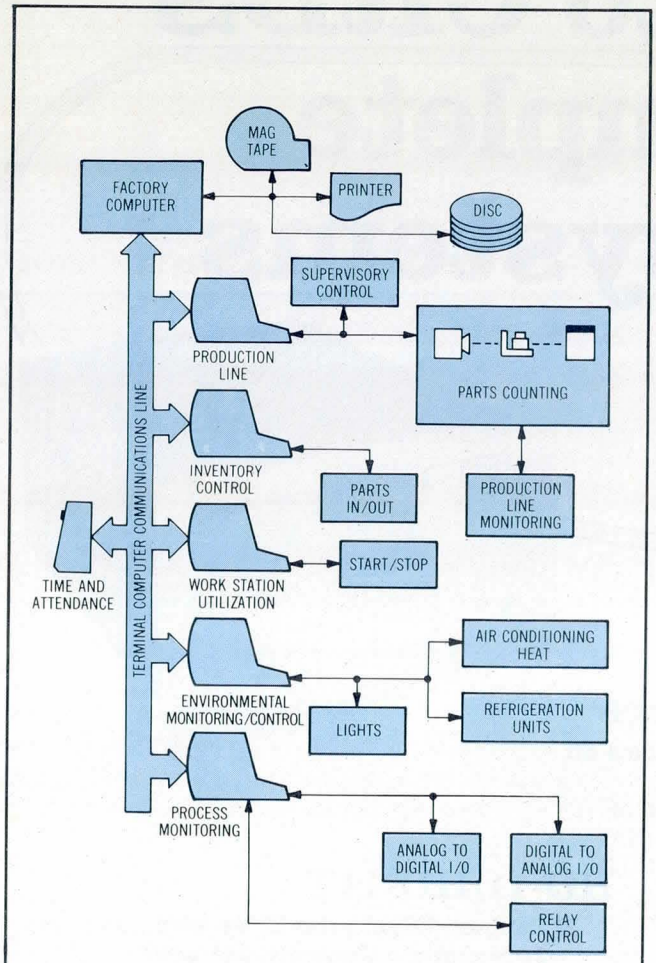

Fig 2 FDT network interfaces wide range of industrial processes or operations. It is controlled by factory computer or frontend CPU which in turn interfaces larger mainframe system. Terminals are configured on polling or shared serial communications link. Network functions on question and answer basis, eliminating any question of priority or time domain windows. Terminals receive functional packet programs and perform tasks dictated by program as standalone computers. Data gathered by terminal network are transmitted over serial link to factory computer and stored as data base for further processing. Individual terminals provide operator with means to input operational data as well as monitoring process without requiring operator intervention

that defines which bit combinations are the alphanumeric characters and control characters, eg, start of text (STX), end of text (ETX), and start of header (SOH). However, there is a wide variation as to what control character performs what function, and it is at the discretion of the systems designer to determine the definition used. Primarily, the software protocol is defined as the mutually employed methodology used to decipher intelligible information from data passed between the terminal and the FEP via the serial communications link.

The concept of software protocol extends to another widely employed concept, polling. A polled network is one that maintains a single communications link between the FEP and one or more FDTs. The network is driven by the FEP and the terminals respond only when directed to by the FEP. This direction is transmitted over the serial link as an address followed by a series of instructions from the FEP to the terminals or vice versa. Each terminal maintains a unique address on the polling network and responds only to instructions following the transmission of that address.

This polled network concept is employed to reduce the need for separate communications links for every terminal, to eliminate the need for separate controllers for every link at the FEP, and to the reduce the cost of cabling. However, in such a network each terminal must await its turn in order to accept or send information to the FEP and must contain sufficient intelligence to decipher its address and ignore transmissions to other terminals on the same network.

One of the most common network configurations deploys the terminals on a polling network and requires that every entry made by the operator be transmitted to the FEP as soon as the terminal is polled. This can require the terminal to store a certain portion of the inputted data because the frequency on which each terminal is polled is dependent on the utilization of the network. It also causes lag times or operator wait periods during intervals of high usage. Subsequently, the operators avoid accessing the network during these periods.

In order to adapt an FDT to an application involving process monitoring and control, a model protocol must be

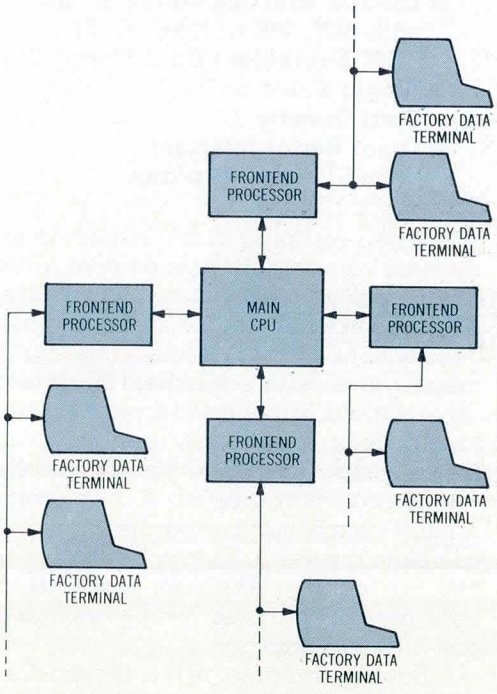

Fig 3 Typical network configuration. Network or frontend computers interface multiple terminals over polled communications links. Terminal data path passes through frontend computer to main CPU for storage, processing, or operations requiring active control

formatted. The terminal firmware must incorporate certain features that are found in most realtime operating systems, and in order to remove the restrictions placed on it by constant FEP communications over the shared line, the terminal must be capable of performing tasks in a standalone mode. This standalone capability is achievable by use of a functional packet communications protocol.

Functional Packets

A functional packet is defined as a series of commands (see Table) issued by the FEP to the terminal to perform certain terminal functions, eg, accept an operator keyboard input, read a badge, or read a bar code. These commands are written by the system designer and stored at the various FEPs for transmission to the terminals as required by either operator request or FEP direction. Functional commands can be utilized to program a terminal and cause it to perform the operations required. Mnemonics are macros capable of being assembled and transmitted to the terminals. The transmitted code utilizes the 8th bit in the 8-bit ASCII code. Functions performed by the terminal are a result of reception of these codes. Codes are combined in a packet of transmissions for the terminal to perform a required sequence of operations.

Functional packet commands are transmitted from the FEP in the form of data and are interpreted at the terminal as an action it must perform. The terminal then compiles the proper sequence of actions as an internal program to perform this action without requiring further action or transmission by the FEP until the entire sequence of commands has been completed and is ready for retransmission. Commands are decoded by utilizing the 8th bit of an incoming ASCII data stream as a command word.

The 26 alpha and 10 numeric characters are contained within the 7-bit ASCII code set. Therefore, when a data word contains 1 in the 8th bit, it can be recognized as a command word and interpreted along with any following modifiers in order to define a sequence of operations from subroutines internal to the terminal firmware. These operations are written in the terminal random access memory (RAM).

Each terminal is capable of processing 128 separate tasks, but these tasks need not be the same for every terminal. Once an incoming function packet ETX character has been received, the terminal performs the stored sequence of operations as it would a program and stores the data received from the operator or process being monitored. Upon completion of the stored program, the terminal will transmit the stored data to the FEP after receipt of its polling address.

Using this approach eliminates the need for the terminal to communicate constantly with the FEP for further operator prompts or directions. The terminal operates on its own after the function packet has been decoded and stored in RAM. Since the terminal transmits and receives in a batch mode, it need only demand resources from the FEP twice for each complete function packet transaction.

(continued on page 98)

TYPICAL FUNCTIONAL PACKET COMMAND CODES*

Mnemonic (M-Modifiers)	Code	Function
DISP, M	80, MESSAGE, 00	Display following ASCII message to operator
BADG, M	81, XX	Read badge and store data in next XX locations. XX = exact number of data words to be read from a badge input
CARD, M	82, XX	Read card and store data in next XX locations. XX = exact number of data words to be read from punched card
KEYB, M	83, XX	Read keyboard data and store in next XX locations. XX = exact number of keystrokes expected
LINE, M	84, MESSAGE, 00	Output to line printer the following ASCII message
FORE	85	Foreground mode operation
DELY, M	86, XX, YYYY	Delay—sets watchdog or XX delay timer, interrupt period. YYYY = delay in seconds or milliseconds depending on timer resolution
BACK	87	Background mode operation
RADC, M	88, XX, XXXX, YYYY	Read ADC XX and verify reading is between XXXX (high limit) and YYYY (low limit)
ODAC, M	89, XX, YYYY	Output to DAC XX, YYYY (output word)
RDIR, M	8A, XX, YYYY	Read digital input register XX and verify the reading is YYYY
ODOR, M	8B, XX, YYYY	Output to digital output register XX, YYYY (output word)
	8C to 95	Decision and branching functions
	96 to 77	Application commands

*All numbers are hexadecimal.

When the functional commands are completed, the terminal strips out the unnecessary data such as operator prompts and input restrictions that are used by the interpreter portion of the terminal firmware, thus reducing the transmission time required to return the completed packet to the FEP by a minimum of 25%. The function packet may be as extensive as required or a single step limited only by the amount of RAM available at the terminal and the peripherals attached. Transmission time is reduced by eliminating the need to precede all transmissions with the terminal identification and control characters. This technique can realize transmission time savings of up to 50% over protocols that permit random terminal inputs.

In addition to the transmission savings, data are sent from and to the FEP in a batch mode, which is more efficient in conjunction with current mass storage and data base techniques because it requires fewer peripheral accesses to accomplish the same data transfer. The batched data do not require additional communications buffers to be built to service each terminal. Batch transfers can be directly made to and from the disc or data base if they do not reside on disc.

Inclusion of the function packet concept enables the terminal to interface process functions and, within the guidelines of the function commands, determine status of the control process being monitored. For example, consider an ADC which must operate within a range of not more than 5.5 and not less than 4.5 Vdc, and which is interrogated by a function command once each millisecond. If the reading exceeds either voltage limit, the terminal must notify the FEP and send an alarm to the process operator. A terminal operating on these directives must be capable of performing this task and also be capable of allowing an operator to enter transactional information without unwanted interaction. The capacity to perform multiple functions is termed multitask and specifies that certain functions be performed to allow the terminal to interface an operator on an as-needed basis in a foreground mode and interrogate the process information in a background mode. This foreground/background technique is the same concept found in minicomputer realtime operating systems.

An FDT incorporating these additional capabilities can operate on a polled transmission line with an FEP directing both the transmission protocol and the terminal operation in batch mode, accept function packet commands sent by the FEP and interpret those commands to perform a set of tasks specified by the FEP, and interface with an operator and be capable of presenting and retrieving information at the discretion of the operator. This information would be sent to the FEP for storage and eventual utilization by the MIS. The FEP can perform process monitoring and control procedures on equipment associated with the production activities by augmenting the terminal architecture with extended functions such as analog and digital inputs and outputs. It can also function in a foreground/background mode, is capable of interfacing both the operator and the process independently as each task is required, and can analyze the process data and perform a decision function, which determines what action the terminal will take. These last decisions would be based on the data collected and the parameters supplied in the function packet commands. Decision generated actions would result in alerting both the FEP and the operator of an out of tolerance parameter, identify that parameter, and specify the programmed action to be taken by the terminal.

For example, the terminal in Fig 4 interfaces an FEP via a serial link in a polled protocol with an instrument installed on a wire extrusion machine to determine the diameter of the wire output from that machine. The terminal is also connected to a similar instrument monitoring the raw material being input to the extrusion machine. Instrumentation within the extruder monitors head temperature, machine state (on/off), and the speed of the wire being extruded from the machine, ie, product throughput. This information is also gathered by the terminal.

The FEP sends a function packet to the terminal containing the necessary commands that enable the terminal to monitor diameter of raw material (analog input), diameter of extruded material (analog input), temperature of extrusion heads (analog input), and material throughput of the machine (analog input). In addition, the terminal can log the machine's operation time (digital input), provide recalibration to the diameter measuring instruments (analog output) as the finished product is required to change dimensions, and start and stop the process (digital output). These functions are provided with tolerances and the terminal notifies both the FEP and the operator when those limits are exceeded.

(continued on page 100)

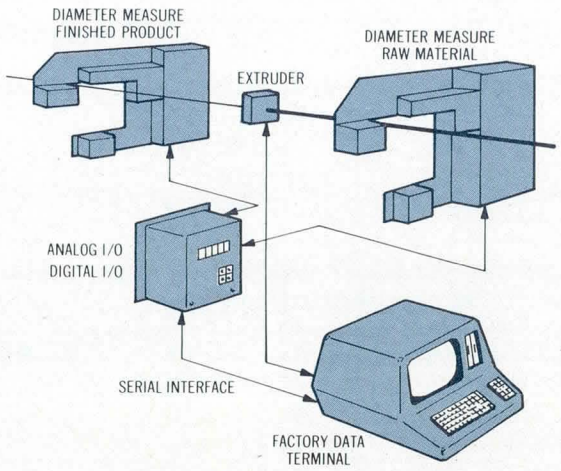

Fig 4 Typical application of FDT interfaced to operator or wire extrusion process. Terminal operates on series of functional instructions transmitted over terminal network from either frontend or main CPU. It monitors machine performance on realtime basis and evaluates performance according to criteria contained within functional program. Results of decisions are either displayed to operator or transmitted to frontend CPU, which maintains data and decisions within its operational data base. Process operator may, as needed, enter information into terminal while process monitoring is being performed

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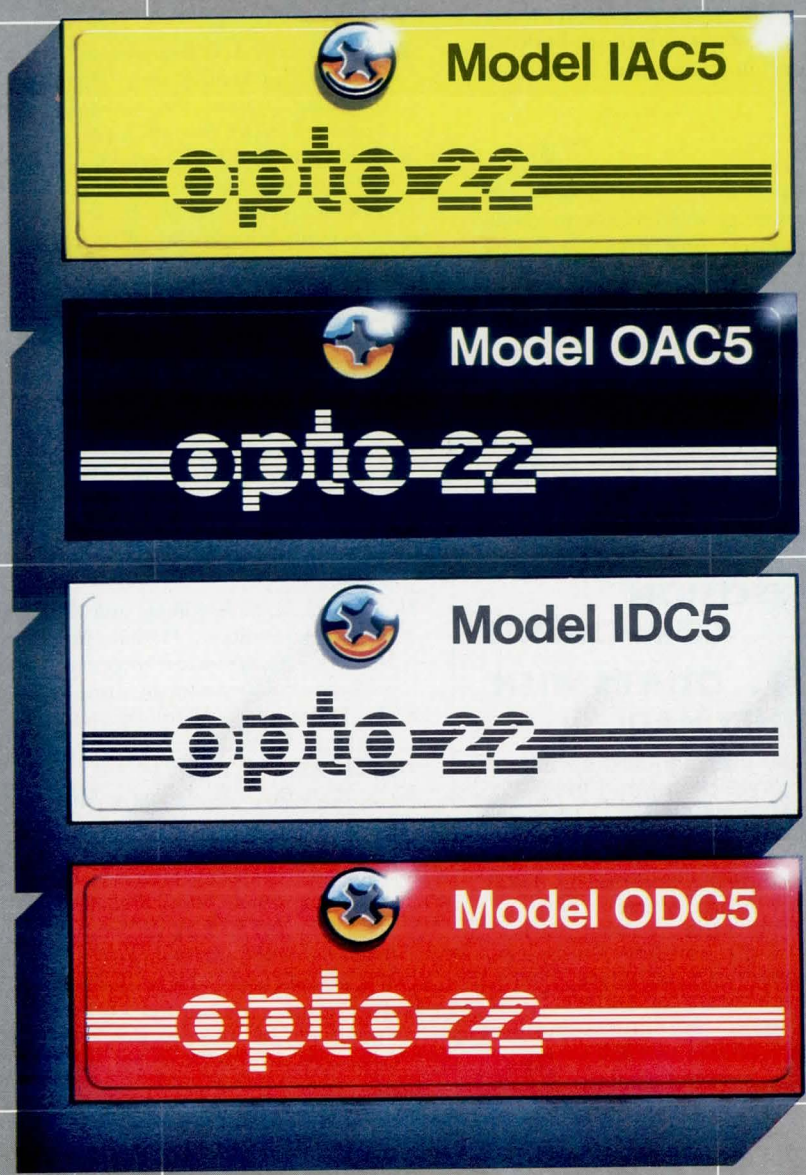

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This arrangement allows the operator and the FEP to make adjustments or curtail the production process soon after a machine problem is detected. Ability of the terminal to monitor the process reduces the quantity of information that must be input by the operator and provides a realtime update of the machine's status and production output. That information is updated to the FEP at regular intervals and eventually is retrieved by the MIS for use in determining the status of the machine, production quantities being processed, utilization of this work station, and amount of raw material being required versus the quantity of finished product. In addition to being able to compile data in the background mode, the operator can access the terminal to input data such as job number, job description, operator identity, and product destination. The foreground mode can also provide the operator with communications between the foreground and background modes to display the data being gathered from the process.

Conclusion

Adaption of computers to the production environment has dramatically increased the knowledge available to management for determining time, labor, and materials costs necessary to produce a finished product. The advent of microprocessors has enabled the factory computer to monitor with even greater exactness these same parameters at the point best suited to collect these data: the production floor. The next step is to provide higher resolution and monitor those parameters in real time and facilitate their collection by extending the capabilities of the factory data terminal. This extension of capabilities will result in savings derived from waste reduction, optimized utilization of manpower and machinery energy, reduction of downtime, and a higher resolution of product costs. Such savings, combined with the extended capability afforded the operator, make extended factory data terminals a welcome addition to the market.

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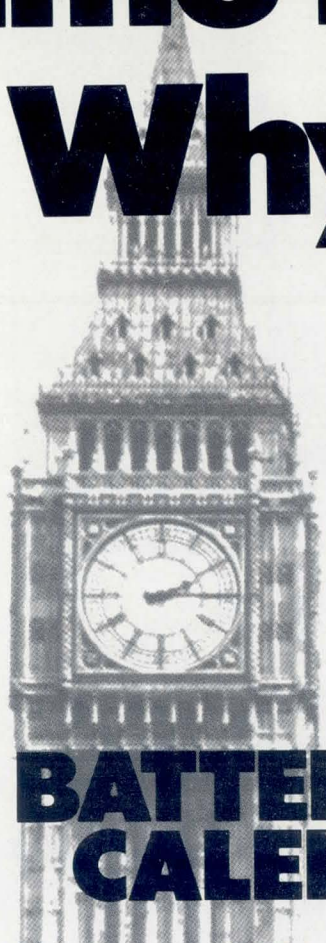

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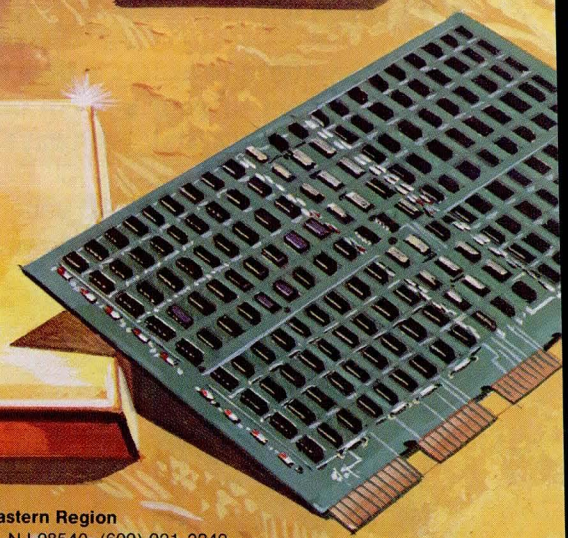

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Early in the design of the VAX-11/750 32-bit minicomputer, cost and performance goals dictated a careful, up-front analysis of the various semiconductor technologies currently available. In particular, as so much has changed since it first came into use, there was doubt as to the ability of the Schottky transistor-transistor logic family to provide a favorable price/performance ratio in the final product. This doubt initiated an investigation, the results of which revealed that metal oxide semiconductor technology, emitter coupled logic, and other transistor-transistor families, custom or off the shelf, all presented serious problems. To avoid these cost and performance problems and to meet specific, complex needs, the designers turned to gate arrays.

Selecting a Technology

The analysis of the available technologies was complicated by the extreme complexity of the VAX-11/750 target architecture. By most standards a mainframe architecture, it had to support variable length instructions, a wide variety of data types (eg, 1-, 2-, and 4-byte integers, character strings, decimal strings, 4- and 8-byte floating point data, and variable length bit fields), and a memory management scheme offering virtual memory facilities. Critical to the problem was the selection of a technology that could implement all of these features and yet still demonstrate good price and performance characteristics when benchmarked against competing designs.

Available metal oxide semiconductor (MOS) technologies offered propagation delays in the 12- to 15-ns range. Preliminary studies showed that a sufficiently elaborate internal structure using MOS technology could meet the overall design goal: the achievement of 60% of the performance of a VAX-11/780, a machine built with 5-ns Schottky transistor-transistor logic (TTL).[1] However, the development budget allowed only for the design of about five different component types, and desired performance could not be realized by using only five different parts if they were constrained to operate at MOS gate speeds.

Emitter coupled logic's (ECL) high gate speeds would allow a very simple internal structure. For example, a 16-bit data path cycled at 75 to 100 ns would yield adequate 32-bit performance to meet design goals, even with very simple

Benefits of Gate Arrays

	VAX-11/750	Small or MSI machine with equivalent performance
Printed circuit board area for CPU and memory controller	900 in² (5800 cm²)	2000 in² (12,900 cm²)
Backplane slots for total system including CPU, memory, and I/O adapters	18	35
Total system power requirements	1000 W	1750 W
Relative reliability measurements	2x hours MTBF	x hours MTBF
Cabinet size	30 x 30 x 40″ (76 x 76 x 102 cm)	60 x 30 x 40″ (152 x 76 x 102 cm)

prefetch and instruction decode logic. However, the design also required large amounts of high speed internal memory—500k bits of control storage and 70k bits of cache and translation buffer—and for these, the available selection of ECL parts was not adequate. Moreover, this selection range is much smaller than that offered by the TTL family, implying a higher part count with the use of ECL as there is a lower probability of the availability of a particular function in a single package.

The large scale integration (LSI) TTL available was capable of providing parts in the 400- to 500-gate range. Trial designs were done to understand the importance of placing various pieces of the design into custom parts. It soon became clear that LSI would not be of significant value unless the custom parts implemented a substantial part of the total design. As a general rule, this reflects the relatively small fraction of total product cost that is invested in any product's semiconductor content. To achieve the desired level of performance with conventional off the shelf TTL, components would have required about 1500 packages. A machine with such a level of complexity would incur substantial costs for printed circuit boards, backplanes, card cages, power supplies, and cabinetry. Elimination of as many as several hundred of the semiconductor devices would not reduce overall product cost significantly. Instead, the key to effective use of LSI lies in changing the nature of a design to improve final size, power consumption, reliability, and other significant aspects of product cost. For the VAX-11/750, this level of savings in areas other than semiconductor cost was possible only by the implementation of at least 75% of the logic with custom parts. (See the Table.) Partitioning trials showed that it would take about 40 different custom designs, each in the 300- to 500-gate range, to achieve a suitable level of integration. At an estimated cost of up to $150,000 per design, developing 40 or so custom components would be prohibitively expensive, even in the event a large enough design team could be assembled. So, as an alternative, the gate array was selected.

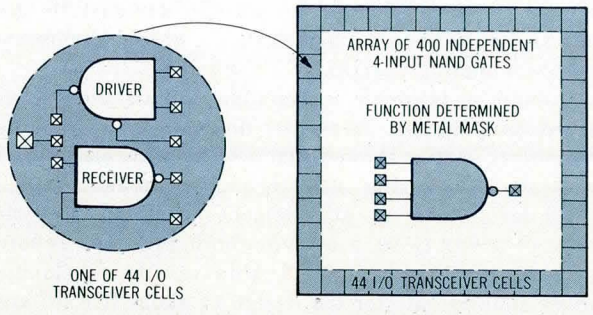


Fig 1 Basic gate array. Vax-11/750 gate array supplies 400 NAND gates, each with 4 inputs and about 8-ns propagation delay. Forty-four signal pins can be used for input or output or as bidirectional transceivers

The Gate Array Alternative

A gate array consists of a basic set of diffusions that define a large number of primitive circuit elements, such as logic gates or flipflops. Each array is customized by final metallization layers that interconnect the primitive circuit elements in a particular way. (See Fig 1.) An advantage to this structure is the commonality among different designs, allowing use of computer aided design tools to reduce development time and cost across an entire family of designs by a factor of three- to five-fold over the time and cost of a fully custom design project.[2,3,4] Although both the basic gate array and the computer aided design tools were developed for proprietary use, many semiconductor vendors now offer similar products as standard items.

Gate arrays also reduce costs at the wafer processing stage. Because of the common diffusion layers, 8 of the 13 masks required to process the wafers are identical in all of the different designs. Use of the gate arrays decreases mask generation time and cost as well, and importantly, it also reduces the overall development time from schematic to finished chip. This is accomplished because the diffusion

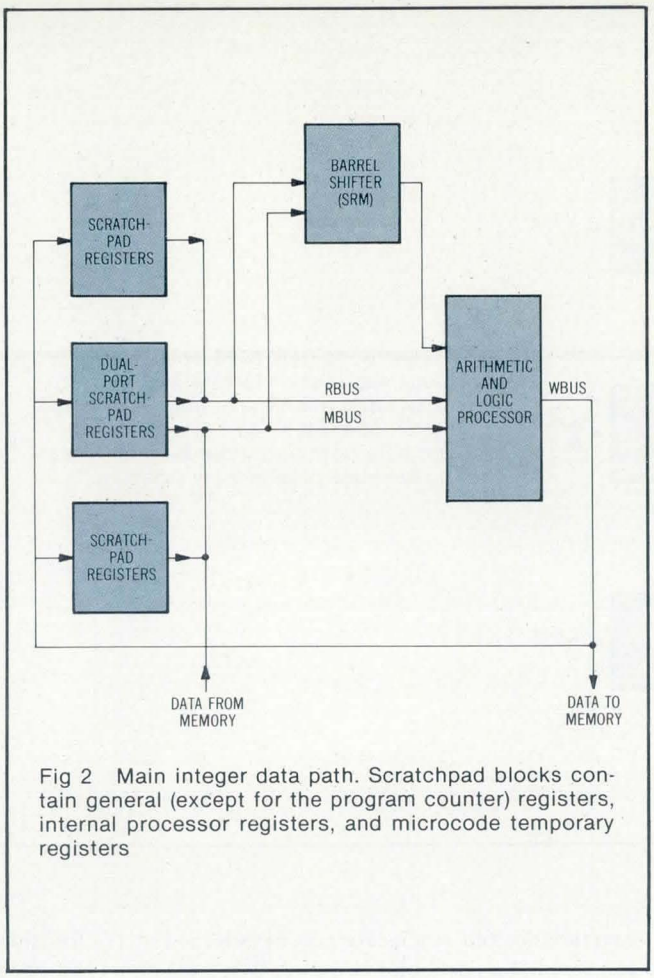


Fig 2 Main integer data path. Scratchpad blocks contain general (except for the program counter) registers, internal processor registers, and microcode temporary registers

steps that account for more than half of the wafer fabrication time can start even before the final metallization masks are ready. Partially fabricated wafers can be stockpiled to await the final processing steps that can begin as soon as the metal masks arrive for personalizing.

Machine Structure

In the main integer data path (Fig 2), scratchpad blocks contain three types of registers. In addition to the general registers, with the exception of the program counter, they contain internal processor registers which comprise a set of architecturally specified registers that are visible only to privileged program codes. These include, among others, memory management registers, the vector table pointer, and the software interrupt register. The microcode temporary registers, although not part of the architectural specification, are necessary for its implementation. Available only to the microcode, these registers are used to hold intermediate results calculated in the course of instruction execution. The RBUS has a total of 40 registers: 15 general registers, 10 internal registers, and 15 microcode temporary registers. There are 8 microcode temporary registers on the MBUS, and 8 dual-port registers can be accessed from both buses. Two sets of standard scratchpad random access memories (RAMs) implement the dual-port registers. The scratchpad addressing (SPA) gate array controls scratchpad RAM addressing to ensure that information is copied into both sets of RAM, thereby making the data available on either side of the arithmetic and logic processor (ALP) during subsequent microinstructions.

The shifter, rotator, and multiplexer (SRM) is built from four copies of a bit slice part that implements the first level of a 2-level, 64-bit input, 32-bit output, barrel shifter. Intended primarily to enhance performance for variable length bit field instructions, shift instructions, and rotate instructions, the barrel shifter reveals the flexibility provided by the low cost gates of gate array technology. It is somewhat unusual for a minicomputer in this price range to include a barrel shifter.

In using gate arrays, it is apparent that the cost of a part rises only very slightly in response to an increase in the use of its internal gates. This means that any performance enhancements that are added to an existing part cause virtually no increase in cost. In the particular case of the barrel shifter, the added ability to convert numeric strings into binary coded decimal digits allows the VAX-11/750 to translate character data into numeric data at the rate of 4 bytes per cycle. Although this feature probably would not be justified if its implementation required additional components, in this case incorporating the feature into the existing gate array enhances performance at little additional cost.

Allocating Bits Among Chips

The implementation of the barrel shifter, and in particular its division across two chip types, illustrates another fact that must influence any decision to partition logic among chip types. Because each output bit depends on the value of every input bit (and on the shift count), the gate array lacks sufficient pins to implement this entire function in a single part. Instead, the barrel shifter function is split into two subfunctions (Fig 3). The first level subfunction, implemented in the SRM chips, rotates the input either to the left or to the right in 4-bit (1-nibble) increments and in doing so, requires a part that has the nth bit of each nibble on its input pins. Thus, bit slice 0 receives bits 0, 4, 8, etc, and bit slice 1 receives bits 1, 5, 9, etc.

The second stage subfunction of the barrel shifter performs a shift of up to three bit positions, but only to the right. Hence, in combination these two subfunctions can achieve any arbitrary shift. Chips that implement the second level must have consecutive bits supplied as input to their pins, precisely the same bit allocation required for functions that propagate a carry, such as the addition and subtraction functions performed by the ALP chips. Splitting the barrel shifter operation into two subfunctions permits using the excess capacity in the ALP chips to implement the second stage subfunction at almost no additional cost.

Identification Pins Reduce Part Types

The memory interface section of the machine (Fig 4) consists of the address logic, memory data routing, cache, transaction buffer, and memory bus interface. The address logic chips implement the virtual address register and the

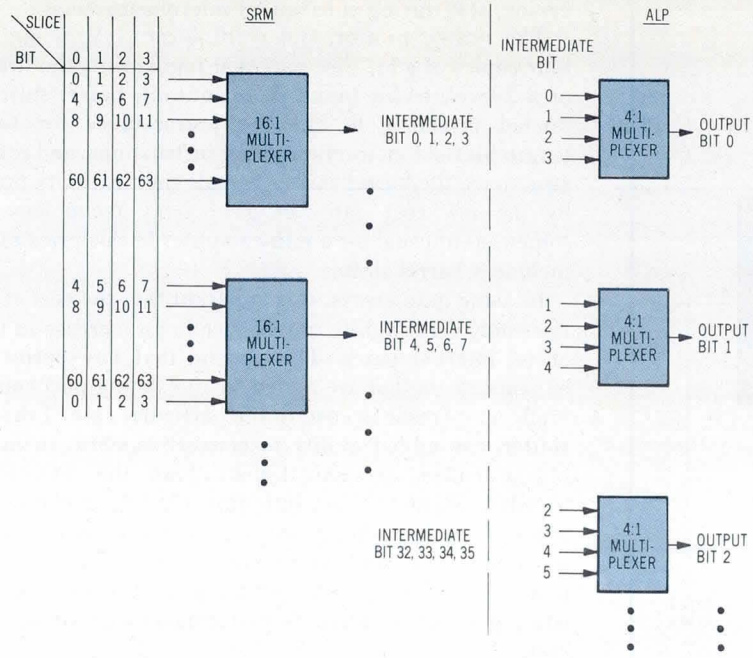


Fig 3 Barrel shifter. SRM chips perform first stage subfunction by rotating input left or right by whole nibble amounts. ALP chips complete operation by rotating intermediate data right up to four bit positions, making best use of gate array pins

program counter (PC), while the address logic adder is used to increment the PC during prefetch, add offsets to the PC during displacement mode addressing, and increment the virtual address to address the second portion of an unaligned operand that spans more than one long word of memory. These chips are partitioned into four 8-bit slices, each holding one byte of a 4-byte long word but not performing identical functions. The low order slice must add 1, 2, or 4 to the PC, depending on the microword, and the other three slices need only increment the PC when there is a carry from a lower slice. The two high order slices must force their outputs to 0 when the machine is running in its 16-bit compatibility mode. Since these four chips perform three slightly different functions, the design situation could be approached in any of the three ways.

Extra components added to the printed circuit board outside of the gate arrays can customize four identical address logic chips by modifying their individual functions. For example, the value 1, 2, or 4 can be created outside of the chip and fed in to be added to the PC as a constant. Also, the outputs from the high order two bytes can pass through external gates that will force them to 0 in 16-bit compatibility mode but will add to the cost. Additional part types can be fabricated to implement the three different functions using three different types of parts. Although this approach does not increase the product cost, it does add to the overall development time and expense and discounts the basic similarity of the three functions.

The optimal alternative uses four identical chips and dedicates one or more input pins to identify or personalize each chip. The printed circuit board is designed to tie the identification pins either high or low, depending on the function desired at a location as determined by the bits that are wired to a particular chip site. When the chip is plugged into a printed circuit board location, the printed circuit layout programs it to perform the function required at that location. Its only drawback is that it requires use of dedicated chip pins, a resource that is often in short supply.

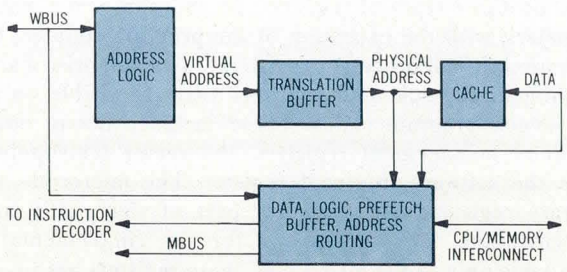
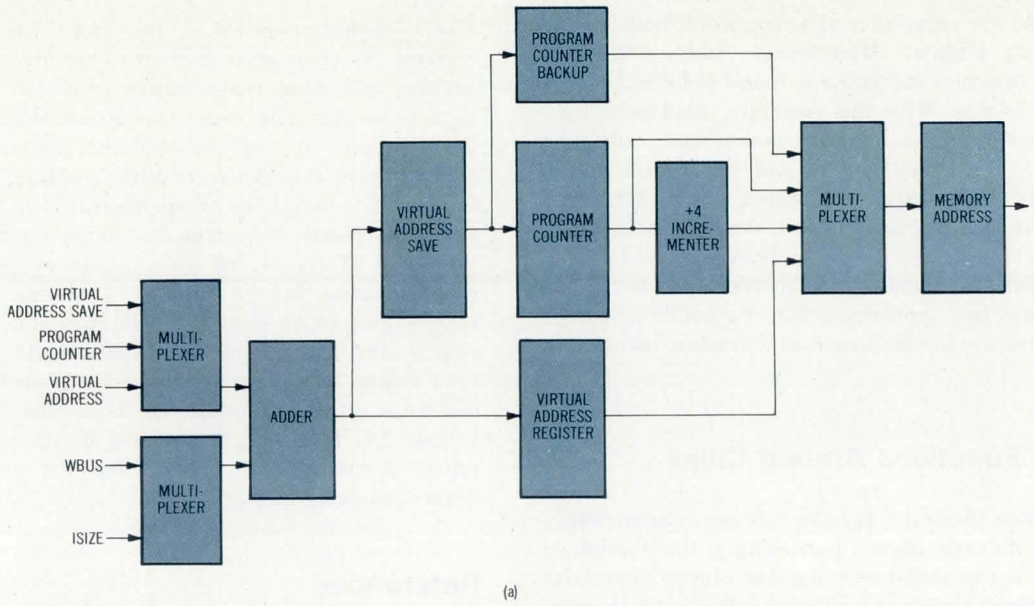
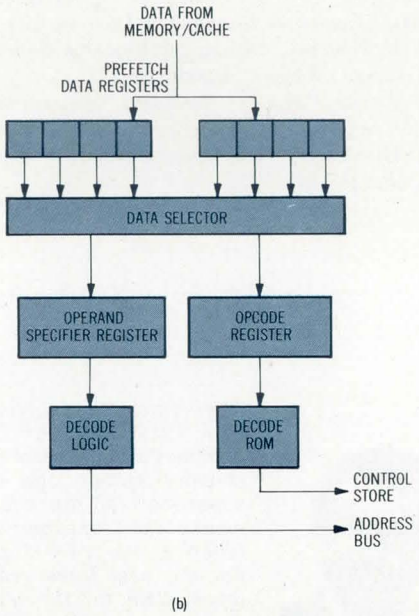


Fig 4 Memory interface. Address and data logic combine with cache and translation buffer to service all memory requests made by data path and instruction decoder



(a)



(b)

Fig 5 Prefetch logic. Dedicated incrementer following program counter (a) enables memory requests ahead of current instruction to keep prefetch data registers (b) full. This reduces instruction execution time by supplying steady stream of instructions to decode logic

Gate Cost Impacts Design

Partitioned into eight 4-bit slices, the memory data register (MDR) chips receive one bit from each of the four long word data bytes, allowing the MDR to rotate memory data while it is en route to or from the data path. This is consistent with the architectural requirement that allows operations to be performed on data that reside at arbitrary byte addresses in memory. One interesting characteristic of the memory interface is that it shows how gate array technology influenced design decisions at early stages of this project.

Designing with LSI components, as in this architecture, allowed a certain freedom to envision more complex structures than could be achieved with medium or small scale integration because the extremely low cost per gate makes them practical. Here instruction encoding used opcodes that designated the operation to be performed and operand specifiers that identified the location of the operands. These opcodes are one or two bytes long and can take up to six operand specifiers, each up to six bytes long. Consequently, instructions have an arbitrary alignment in memory and must be parsed in a serial manner.

Initially, the problem of handling instruction decoding was approached using microcode prefetch and a 4-byte register to hold the remainder of a long word fetched from the instruction stream. After some study, the more sophisticated structure of Fig 5 was found to be within product cost guidelines. With this structure, hardwired logic takes advantage of idle cache cycles to maintain instruction stream data in an 8-byte buffer and flushes the buffer automatically during program branches. It also controls a rotater to maintain instruction bytes that are available to the decode circuitry while the PC is being updated during opcode and specifier decoding. In contrast to the microcode prefetch scheme, this approach achieves a net 20% to 30% increase in machine performance at a modest increase in final cost.

Allocating Functions Among Chips

Use of MDR chips illustrates the three device characteristics that most significantly impact partitioning: the number of gates; the number of signal pins; and the propagation delay penalty paid for entering or leaving the chip, an important characteristic of nearly all LSI devices. Compared to a printed circuit board environment, the gate array with its light capacitive loading and low noise environment gives internal gates substantially shorter propagation delays than offchip driver circuits. Typically, offchip drivers have two to three times the propagation delay of internal circuits.

With 44 signal pins and 400 internal gates, the VAX-11/750 gate array offers about 9 gates per pin. A typical bit slice part may have three ports; this implies that there are about 27 gates per bit. For NAND gates that can be wire-ORed within the array, a pass latch most often needs four gates per bit, an edge triggered register six gates per bit, a multiplexer one gate per bit, and an adder about five gates per bit. These figures suggest that the best partitioning schemes will slice each functional unit of the design in a way that is deep (many functions performed per bit) and narrow (a small number of bits handled). Compared to a partitioning scheme that is shallow and wide, this strategy offers several advantages: a higher utilization of internal array cells, a minimum penalty paid for slow input/output gates, and a smaller number of different chip types. The chip types are minimized because a deep slice can implement more functions per chip type, requiring fewer types to create a complete system.

MDR chips implement functions associated with the flow of data between the memory, cache, data path and instruction decode unit. They are sliced as deeply as possible in the sense that the MDR has data ports connecting it to each of the four functional units, and only a single part type implements all necessary functional capabilities. The UNIBUS interface provides another example of functions partitioned onto chips. A single chip contains the logic that handles data and address flow between the memory interconnect and the UNIBUS. Two alternative techniques were also considered: one using a data chip in conjunction with an address chip, and one using a UNIBUS interface chip in conjunction with a chip to interface with the memory interconnect. All three alternatives required a total of four parts; however, both of the approaches that were rejected needed two part types instead of one.

Conclusion

Use of semicustom LSI in the VAX-11/750 offered digital systems designers an important capability to produce competitive and more cost-effective products. There are two keys to success with using this approach. Semicustom LSI devices must be used in sufficient quantity to effect a change in the overall nature of the product. The goal, here, is not just to save a few components, but to reduce package size and power requirements while increasing product reliability. Moreover, full advantage must be taken of device characteristics in the tuning of system designs; mere repackaging of an existing medium or small scale integration design will not yield optimal results. In addition to their impact on system design, semicustom LSI presents the challenge of partitioning. In this area, designers will achieve the most effective results by abandoning a functional viewpoint and approaching the problem from a device capability perspective.

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After joining Digital Equipment Corporation, David Cane designed the company's first semiconductor main memory system and was the project supervisor for the microcode development of the first experimental implementation of the VAX-11 computer family. For the past three years he has been responsible for the technical development of the VAX-11/750. He received a BSEE and an MSEE from the Massachusetts Institute of Technology.

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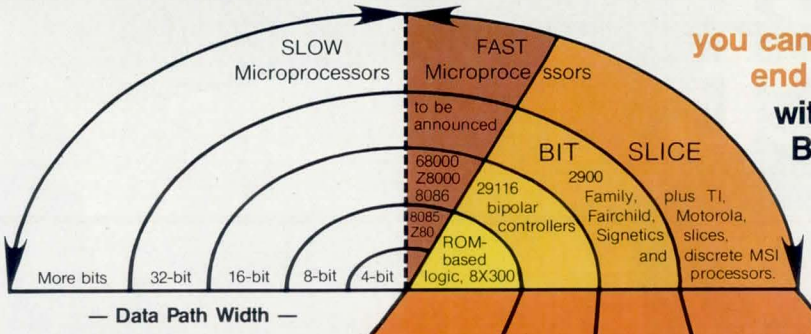

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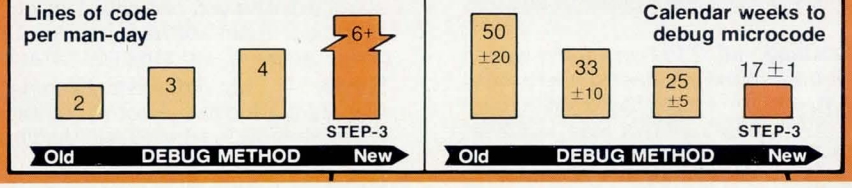

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PRINTED CIRCUIT BOARD LAYOUTS FOR A COMPATIBLE DYNAMIC RAM FAMILY

Circuit board layouts that provide the option of using several pin compatible memory devices result in long term savings by eliminating redesign when density upgrade is required

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Dynamic random access memories have come to dominate the memory marketplace, with each introduction necessitating board redesign because of additional features and increased density. A family concept minimizes this redesign effort by providing new memories with pinouts that are the same as or compatible with those of existing family members. Thus, the improved density and added features of these N-bit by 1-bit memories can be incorporated into existing systems as they become available, without major component substitution or functional changes.

Furthermore, the compatible memory concept can stretch the lifetime of a memory system design with minimum effort—important in engineering environments where design costs are rising rapidly. The option of using several different density devices in a memory site results in a long term savings by eliminating the need for redesign when a density upgrade is required. A significant savings also results from extending the usable life of the design over a longer period of time. Typically, memory system design costs are amortized over a 3- to 5-year life cycle for the board; however, the compatible family concept can extend this life cycle significantly.

To attain full benefits from these address multiplexed, pin compatible memories, the differences between devices within the family must be considered when designing system boards. Since multilayer boards that support different devices are relatively easy to design, they will not be discussed, although many of the recommendations apply to them. Double-sided printed circuit boards that accept numerous members of the family are more difficult to design; however, they are commonly used with dynamic random access memory, and demonstrate adequate margins when properly designed.

RAM Component Pinouts

Packaging techniques used in the compatible family of address multiplexed RAMs offer single- and double-density RAM in compatible 16- and 18-pin packages. The 18-pin, double-density package adds two lower pins for row and column select controls that access the second chip carrier device. In other respects, family members exhibit nearly identical pinouts. Three different compatibility concepts can be used to design boards to accommodate family members with various pinouts. (See Fig 1; some of these devices are not yet available, but are included to demonstrate that family concept allows both versatility and expandability in design.) These concepts provide 3-supply, single-supply, or fully compatible layout.

To design a memory board that is compatible across the family or within a subset of it, fundamental differences between various family members must be understood. Five basic areas of difference are:

Power Supply—The 16-pin MK4116 and the 18-pin MK4332 both require a 3-supply power system offering 5-, 12-, and −5-V power. Other members of the family require only a single source of 5-V power.

Addressing—The 16-pin MK4164 (pin 9) and the 18-pin

General Design Guidelines For MOS Dynamic RAM

Always design well within the vendor specification limits. Adequate supply and signal voltage margins, timing margins, and temperature margins are essential for trouble-free operation.

Lay out array as densely as possible while maintaining adequate power buses and array power decoupling.

Use low impedance power distribution through the array. Gridding is essential with double-sided PC boards.

Place high frequency decoupling capacitors within the array matrix. At least one capacitor per critical supply for every two devices is recommended. A 0.1-μF capacitor is suitable for this purpose.

Where possible, place bulk decoupling capacitors around the perimeter of memory matrix.

Use transmission line terminations on all signals to RAM. Conventional termination techniques are effective when used with constant impedance transmission lines that have a predictable impedance. Many of the single-supply RAMs will tolerate as much as -2 V negative excursion below ground on input signals. This does not indicate that line terminations are optional; when excessive overshoot occurs, even within the specification limit, the positive excursions resulting from the damped ringing will reduce noise margins and generally result in a VIL (MAX) violation. High speed dynamic RAM can respond to nanosecond spikes that may cause unpredictable behavior.

Avoid long parallel runs for signals that cannot tolerate crosstalk. If long runs are necessary, provide an effective ground plane by routing power or ground runners on the adjacent layer. This reduces the crosstalk and results in a nearly constant impedance transmission line for signals traversing the array. When solid enough to appear as an ac ground plane, power grid inclusion yields an effective microstrip characteristic. Placing decoupled power or ground runners between the signal traces also reduces crosstalk.

When possible, avoid stubbing array signal lines. Stubbing reflects an impedance discontinuity with resulting energy reflections that can reduce noise margins or violate vendor specification limits.

Locate the driver circuits as close to the array as possible with short, direct routing of interface signals between the drivers and the RAM.

Place both high frequency capacitors and bulk decoupling capacitors near the array driver circuits.

Provide sufficient ground busing for drive circuits and between the drivers and the array to minimize ground bounce and ground offset conditions.

Avoid using driver gates in a common transistor-transistor logic package when crosstalk caused by ground bounce or other internal coupling mechanisms cannot be tolerated.

If any device is being used in an unconventional way, verify with the vendor that the device will support the desired operation.

MK4528 (pin 11) require an additional address line to accommodate the increased storage capacity. A_7 is used for this purpose; not bonded on the MK4516 and the MK4532, it is used for V_{CC} at 5 V on the MK4116 and the MK4332.

$\overline{RAS}$ and $\overline{CAS}$—Double-density packages, MK4332, MK4532, and MK4528, require an additional row address select ($\overline{RAS}$) and column address select ($\overline{CAS}$) pair (pins 9 and 10) of strobe signals to select the second chip on the package. Two extra pins at the lower end of the package receive these two signals $\overline{RAS2}$ and $\overline{CAS2}$.

Pin 1 Refresh—MK4516, MK4532, and MK4528 have an onchip circuit that simplifies the refresh operation and reduces battery backup power requirements. Refresh is achieved by strobing pin 1 active low at the appropriate time. With this feature, the refresh address is provided on the chip to lower component count in chip support circuitry and also lower the power requirements. Pin 1 may be floated, if the onchip refresh function is not used, but pullup resistors to 5 V are recommended to guarantee a solid inactive high level. The 3-supply RAM lacks the onchip refresh feature; instead, pin 1 provides the V_{BB} connection to this device.

V_{CC} Location—The single- and 3-supply parts have V_{CC} connected to different locations. In fact, the primary power pin remains unchanged, but the primary power is 12 V for 3-supply and 5 V for single-supply parts.

Compatible 3-Supply Layout

The PC board layout shown in Fig 2 has been used successfully both with the older MK4096/MK4027 4k-bit RAM and with the MK4116 16k-bit RAM; this layout can be modified to accept the double-density MK4332 RAM. Two supplementary pins must be added at the lower end of each device site to provide the additional $\overline{RAS2}$ and $\overline{CAS2}$ strobe signals required to select the second half of the double-density package. The additional $\overline{RAS2}$ and $\overline{CAS2}$ strobe signals do not require increased vertical spacing between rows of RAM, even though the bottom two pins are used for signal traces instead of for power. As with the 16-pin layout, vertical spacing can remain at 300 mils (0.8 cm); the 18-pin layout, however, requires 0.05 in^2 (0.33 cm^2) more board area per RAM than is required with the 16-pin version.

Further changes to the 18-pin version of the basic 16-pin layout in Fig 2 eliminate the geometric complexity of the metal traces. Fig 3 shows a simplified layout, derived from Fig 2, in which the capacitors have been moved to the center of the horizontal power bus channel and aligned directly above the memory devices. This arrangement allows use of capacitors with either 300-mil (0.8-cm) or 200-mil (0.5-cm) lead spacing. For 300-mil spacing, the capacitors are inserted directly above the integrated circuit (IC) locations; for 200-mil lead spacing, the capacitors are inserted above the space between the IC locations (Fig 4). Relocation of decoupling capacitors simplifies the routing of the vertical signals and power traces, also permitting auto-insertion of capacitors within the memory array matrix.

Recommended and alternative MK4116 and MK4332 compatible PC board layouts in Figs 5 and 6 reflect a slight change over the layout of Fig 3. The vertical power busing has been routed down the 300-mil (0.8-cm) spacing under the IC, and the data in and data out paths have been routed

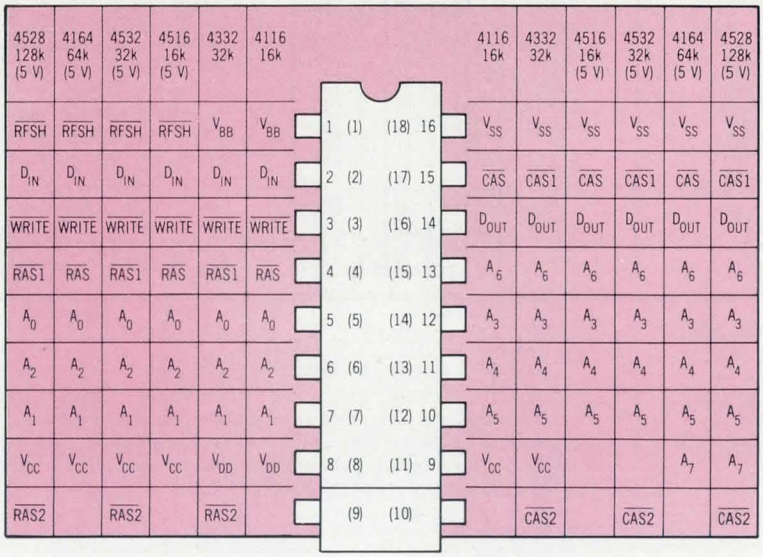

Fig 1 Conceptual table for compatible RAM pinouts. Parentheses enclose pin number for 18-pin packages. Compatible 16-pin devices are top-justified in 18-pin sockets. Double-density 18-pin package adds two strobe signals required to select second half of device. Pin 11 accommodates increased capacity, supplies V_{CC}, or is not bonded. Pin 1 feature provides refresh address on chip, for new technology components, to reduce support circuitry requirements

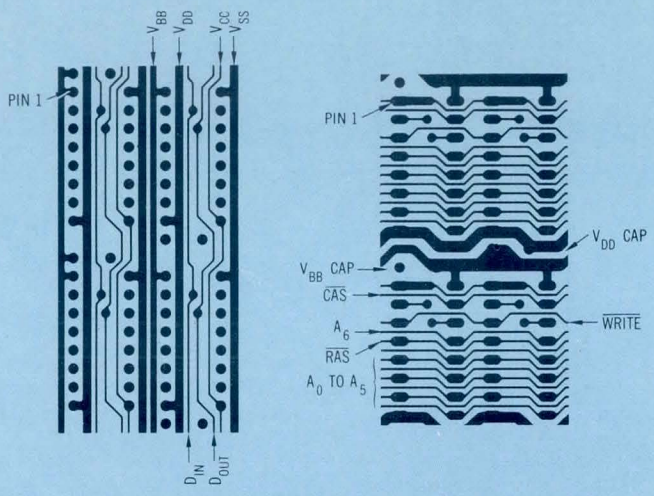

Fig 2 Modified RAM layout. With 18-pin double-density devices, two supplementary pins must be added at bottom of each device site for $\overline{RAS2}$ and $\overline{CAS2}$, but 300-mil spacing between rows of RAM need not increase

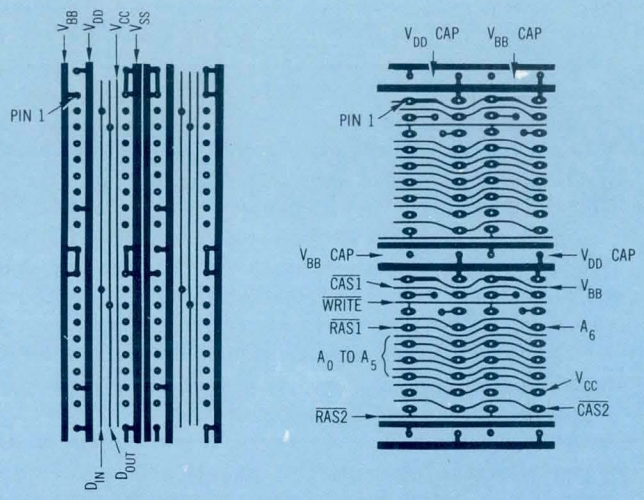

Fig 3 Simplified 3-supply layout. Changes to Fig 2 layout eliminate geometric complexity of metal traces in an 18-pin layout that accepts either 16k- or 32k-bit, 3-supply RAM. Layout requires 0.05 in² additional chip area but preserves 300-mil spacing between rows, even though bottom pair of pins now handles $\overline{RAS2}$ and $\overline{CAS2}$ signals instead of power

down the 200-mil (0.5-cm) spacing between the IC sites. This arrangement results in a straight line routing of data paths. Heavy vertical power buses reduce the trace inductance and provide a substantial ground plane for the horizontal signal traces within the memory array.

The layout in Fig 5 (like all subsequent layouts) provides considerable isolation between data out and data in traces by running a decoupled supply or ground trace between them. Generally, data out coupling to data in is a problem only during late write cycles when transitions on the data out line can cause perturbations on the data in line if sufficient coupling exists between the two lines. This can result in a violation of either data in setup time or data in hold time during the write cycle. In most cases, time discrimination avoids any such problem. Direct connection of V_{DD} and V_{SS} to the RAM pins and the decoupling capacitors suggests that Fig 5 is the preferred layout. The simplicity of this layout is very attractive, although it has the disadvantages of a V_{CC} feedthrough at 5 V under all RAM packages. Layouts shown in Figs 2 and 3 also have this feedthrough under the RAM. Should design rules prohibit feedthrough under ICs, an alternative layout eliminating feedthrough, as depicted in Fig 6, is practicable.

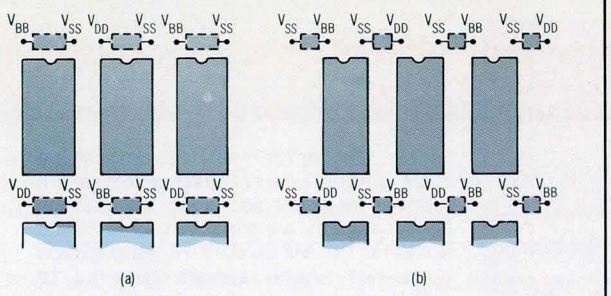

Fig 4 Decoupling capacitor options. In the compatible layout of Fig 3, decoupling capacitors mount either directly above ICs, for 300-mil lead spacing (a), or directly above space between ICs, for 200-mil spacing (b), streamlining vertical signal routes, straightening power traces, and permitting autoinsertion of capacitors

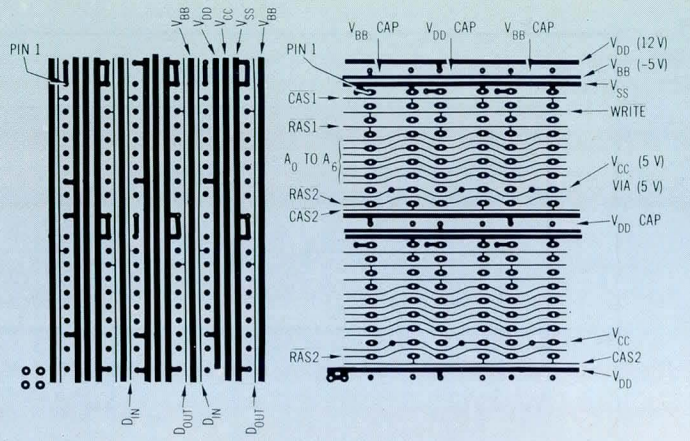

Fig 5 Recommended 3-supply layout. Further changes to Fig 3 layout route vertical power buses down 300-mil space beneath ICs. Straight line data in and data out paths now occupy 200-mil space between chip sites. Heavy vertical buses reduce power trace inductance providing effective ground plane for horizontal traces within array. Decoupled supply trace isolates data in from data out

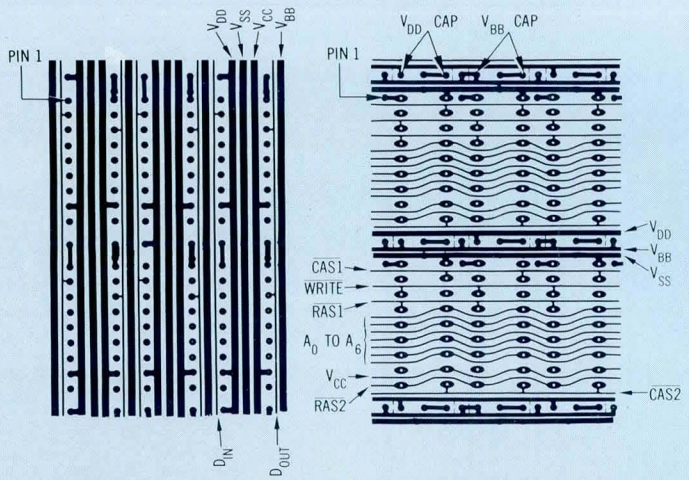

Fig 6 Alternative 3-supply layout. If design rules prohibit feedthrough under chips, use of this layout eliminates feedthrough. However, Fig 5's direct connection of V_{DD} and V_{SS} to RAM pins and decoupling capacitors must be sacrificed here, making Fig 5 the preferred layout

Two special considerations apply to the use of any of these layouts with the MK4116: the 16-pin RAMs must be top-aligned in the 18-pin sites, and the address decoding logic must be designed to select on 16k boundaries and provide a $\overline{RAS}$ signal to the RAM at $\overline{RAS1}$, pin 4. A $\overline{RAS2}$ signal will be ignored because there is no connection to pin 9 of the 18-pin site when an MK4116 is used. $\overline{RAS}$ decoding is recommended for the RAM selection.

When the MK4332 is used with any of these layouts, the 18-pin device is inserted directly into the site. Since the 16k address boundary requirements for the MK4332 $\overline{RAS}$ decoding are identical to those for the MK4116, full compatibility requires no major modifications. The additional $\overline{RAS}$ and $\overline{CAS}$ inputs must be based on 16k boundaries, which does not require jumper wires to handle the $\overline{RAS}$ clocks. Fig 7 shows a method for avoiding jumper wires in the $\overline{RAS}$ decoding logic. Usually jumpers or switches are needed to adjust the board selection logic so that the memory subsystem acknowledges changes in memory density and responds to these changes. One final MK4332 consideration requires a power supply that can provide the additional current needed to support the double-density 32k devices.

Compatible Single-Supply Layout

Single-supply devices employ the same operating procedures as 3-supply devices, but call for a more demanding design effort primarily because of the higher transient currents required by the 5-V single-supply components. Suggested PC board layout for compatibility across the entire subfamily of single-supply high density RAMs is mapped out in Fig 8. Power busing in this layout is as heavy as possible, to provide low inductance and an effective ground plane in the array power supply traces. This technique for "beefing up" the horizontal power traces can be applied also to the layouts of Figs 3, 5, and 6.

Since all of the single-supply subfamily members have the pin 1 refresh function, the layout of Fig 8 supports use of onchip refresh without modification and includes the pin 1 signal trace. The typical memory subsystem block diagram of Fig 9 shows how the pin 1 refresh capability achieves lower chip count and reduced power requirements.

Fully Compatible Layout

Previous examples showed how PC board layouts accommodate either the full range of 3-supply devices or the full range of single-supply devices, with each layout offering compatibility across a subset of the complete memory family. Fig 10 combines the best features of these layouts into one that offers full compatibility across the entire family.

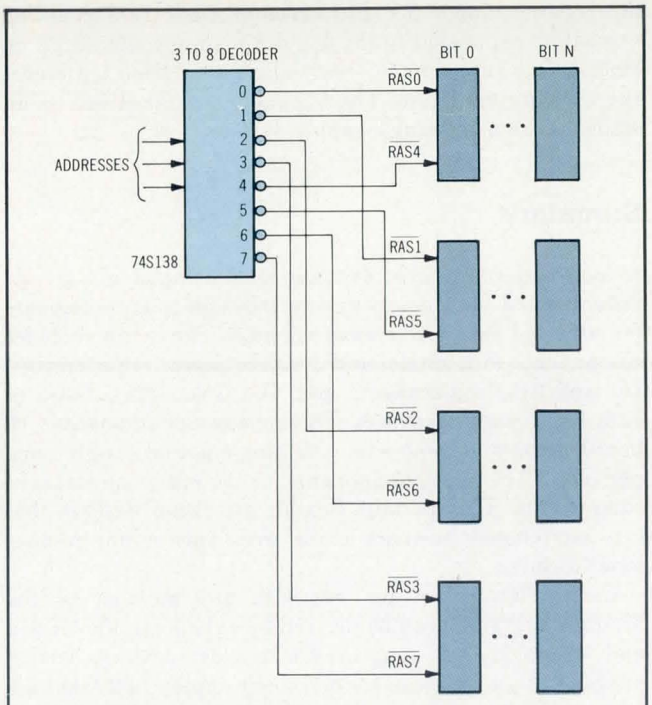

Fig 7 Simplified $\overline{RAS}$ decoding diagram. This approach shows one way to eliminate jumper wires in $\overline{RAS}$ decoding logic; but jumpers or switches are needed for memory system to acknowledge density changes

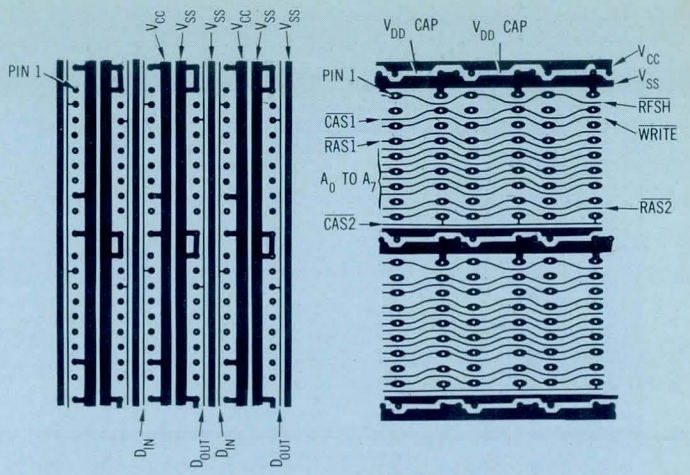

Fig 8 Compatible single-supply layout. Devices that use only 5 V require more demanding design effort because of higher transient currents. In this layout, for either 16k-, 32k-, 64k-, or 128k-bit RAM, heavy power bus provides effective ground plane and low power supply trace inductance, a technique that could benefit the previous layouts. Pin 1 signal trace supports onchip refresh function

In the fully compatible layout (Fig 10), the V_{BB}, V_{DD}, and V_{SS} power buses are very wide, providing an effective ground plane and reducing noise from transient currents. V_{CC}, however, is handled with only a standard 15-mil (0.04-cm) horizontal trace. A trace this size seems inadequate to supply the required V_{CC} current level to devices in the array, but in normal operation there is current drain from the V_{CC} supply only when data are being read from the RAM. Furthermore, the current is required only when the data out is at a high level. In the multiple-supply devices, MK4116 and MK4332, the output can be treated as an open drain device by using pullup resistors on the data out port. The output buffer circuitry is designed to make a monotonic change from the high impedance state to a high (for a logic 1) or from the high impedance state to a low (for

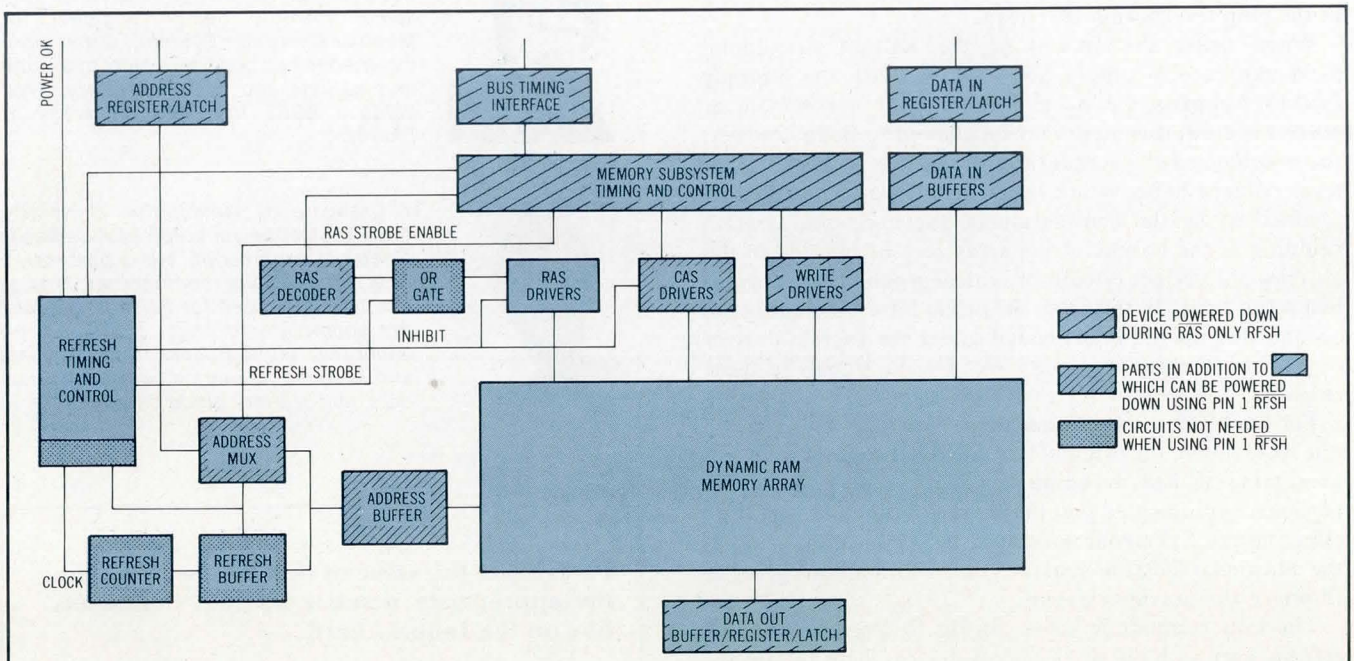

Fig 9 Onchip refresh benefits. Strobing pin 1 active low achieves refresh at address provided on chip. Onchip refresh capability lowers power requirements and also reduces component count in single-supply memory systems

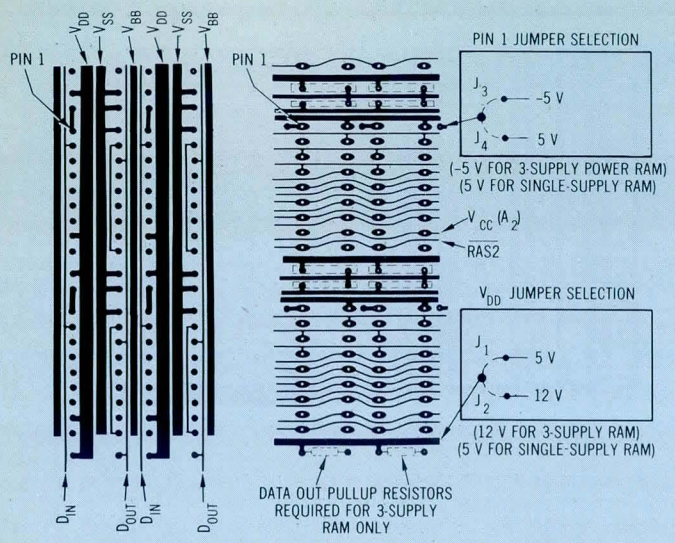

Fig 10 Fully compatible layout. Best features of previous layouts combine in layout usable with any member of compatible RAM family. Layout requires $\overline{RAS}$ only refresh, even with single-supply devices, because pin 1 is tied to V_{BB} gridding for 3-supply operation. Horizontal ground gridding at bottom of array can be omitted in absence of interface circuitry and critical ground paths. Exact location of pin 1 jumper and V_{DD} jumper depends on overall board layout

a logic 0). In other words, glitches or spikes that would delay data access due to the resistance-capacitance time constant of the open drain configuration do not occur during a read operation. Placement of data out pullup resistors is not critical, and the most convenient location is at the top or bottom of the array. Fig 10 shows the pullup resistors placed at the bottom of the array, a method that does not sacrifice access time provided that there is no interleaving at the chip level within the array.

When using the MK4164 or the MK4528, the 15-mil (0.04-cm) trace to pin 11 (used for V_{CC} with the 3-supply devices) supplies the A_7 address line. If the MK4516 or MK4532 is used, this input may be allowed to float; however, the recommended procedure of tying it to a high or low level reduces noise within the array. When layout is constrained by spatial considerations, the horizontal ground gridding at the bottom of the array may be omitted in the absence of interface circuits or critical ground current paths below the array. In this case, the power buses, including the ground bus, should be extended under the bottom devices to provide the ground plane effect for the signals to these chips.

For double-density devices, the second $\overline{CAS}$ line, $\overline{CAS2}$ on pin 10, is tied to the original $\overline{CAS}$ line, $\overline{CAS1}$ on pin 17. This is acceptable if $\overline{RAS}$ decoding selection is performed. Experience has indicated that the short stubbing has very little effect on the $\overline{CAS}$ signal waveform. If $\overline{CAS}$ decoding is used, the additional $\overline{CAS2}$ line must be routed through the array as shown in the previous layouts.

The fully compatible layout of Fig 10 requires $\overline{RAS}$-only refresh, even with the single-supply devices, because pin 1 is tied to the V_{BB} gridding required by the 3-supply RAMs. Therefore, for proper operation of single-supply devices, the pin 1 trace must be tied high, through a resistor or a direct connection to 5 V. Furthermore, all of the decoupling capacitors connected to the V_{CC} drain supply should be installed. One capacitor for every alternate device represents the absolute minimum. The V_{BB} capacitors need not be installed when using single-supply devices.

Summary

A family of compatible dynamic RAM components greatly reduces need for memory system redesign to accommodate features and increased memory density. The family includes components with single- and 3-source power requirements; 16- and 18-pin packages; and 4k-, 16k-, 32k-, 64k-, or 128k-bit storage capacities. Three classes of compatible PC board layouts accommodate all single-power supply components, all 3-supply components, or the entire spectrum of components. This permits flexible hardware designs that can interchange memory chips with only minor jumper modifications.

Compatible layout for use with any member of the 3-supply subfamily can be derived by enhancing the MK4096 and MK4027 layouts, long used with older devices. A compatible subfamily layout for 5-V single-supply RAM takes advantage of the onchip refresh function to reduce battery backup power requirements and lower the chip count in supporting logic circuitry. The fully compatible layout combines the best features of both subfamily layout designs for maximum useful life expectancy with any member of the dynamic RAM family.

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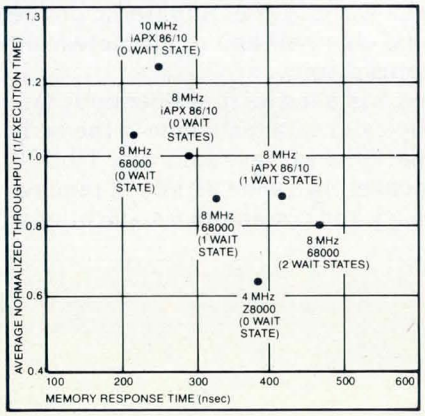

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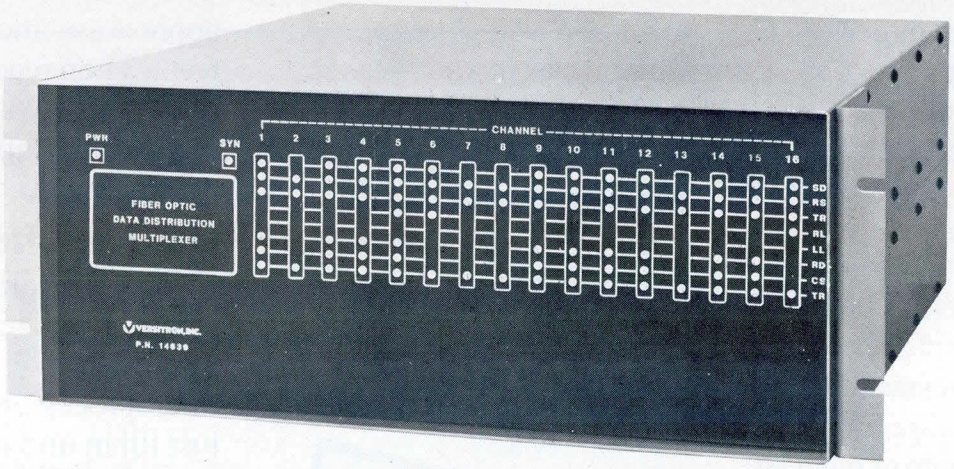

handles 16 channels of local distribution data

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BUS ADAPTER SIMPLIFIES INTERPROCESSOR COMMUNICATION

Using only inexpensive line buffers, bus adapter connects various microprocessors to the IEEE 488 bus and implements the necessary handshaking protocols to achieve effective communication with minimum overhead in localized microprocessor networks

Gerald R. Samsen Texas Instruments, Incorporated
Roger D. Hudson PO Box 1443, Houston, TX 77001

Multiple microprocessors enable a system to execute tasks in less time than that required by a single processor, but the losses resulting from poor communication between the processors can exceed the gains made with a multiprocessor design. In general, two communications techniques have been used in multiprocessor applications. One relies on a serial protocol to implement low speed, relatively long distance, parallel communication between loosely coupled microprocessors. The other uses a multiprocessor bus to provide fast parallel communication between tightly coupled microprocessors separated by comparatively short distances. Both approaches have advantages and disadvantages; their most serious common drawback is that many multiprocessor applications cannot benefit from either technique. Low speed, excessive software support requirements, and the inability to link microprocessors from different manufacturers in a single system limit the effectiveness of both approaches.

Overcoming many of the disadvantages encountered in older communications techniques used in multiprocessor applications, the TMS9914 general purpose interface bus adapter (GPIBA) improves system performance at lower cost than alternative methods. In conjunction with the SN75160 and the SN75161 or SN75162 line buffers, it can interface most popular microprocessors to the IEEE Standard 488-1975/1978 bus, an 8-bit parallel bus that is general enough for use in most multiprocessor applications. Because it reflects an industry standard, the IEEE 488 bus is a good choice in tightly coupled multiprocessor systems. This bus adapter allows extremely flexible and efficient communication to take place between microprocessors and can designate each microprocessor as a talker, listener, or controller. Therefore, it is likely to benefit any design that requires interprocessor communication and that has intelligent processor controlled devices in a localized area.

Among the bus adapter's capabilities are automatic performance of IEEE 488 interface functions and handshake protocols and implementation of a known and accepted industry standard that can simplify design. The bus adapter also helps ensure reliable performance, and lends itself to use with various microprocessors—even those from different manufacturers. In addition, interrupt capabilities eliminate any need to poll the bus continuously and, therefore, allow fast response to changes in the interface

configuration. The device can be implemented inexpensively with only a few line buffers. It requires no additional hardware or software, apart from that of the host system.

Basic Operation

The GPIBA communicates with a microprocessor through a memory mapped 8-bit data port and provides a 16-bit bus to interface with the IEEE 488 bus (Fig 1). Protocol is handled automatically in the talker, listener, and controller modes. Each peripheral device responds to its own unique address established by external switch settings. Information, consisting of either device data or interface control data, is transmitted in byte serial, bit parallel format. Device data can be sent by any one device, designated as a talker, and received by a number of other devices, designated as listeners. Both instructions (such as range or function select) and data (such as measurement data for processing or output) can be sent in this way. One of the devices on the bus, designated as the controller in charge, can also send interface control signals. Devices can be assigned to the bus dynamically, as listeners or as talkers, by sending their unique listen or talk addresses, and they can be switched dynamically between remote and local control.

Physically, the IEEE 488 bus consists of a 24-wire shielded cable. Eight bus lines carry data, eight are control lines, and eight carry signals or serve as system ground lines. Both the dimensions and the actual pin locations for the connector are described in the standard. The connector is a 24-pin, male/female type; however, interconnecting cables used with the interface system have dual connectors that can be stacked to accommodate a variety of physical layouts by allowing more than one connection to any device. All connectors are readily available standard parts.

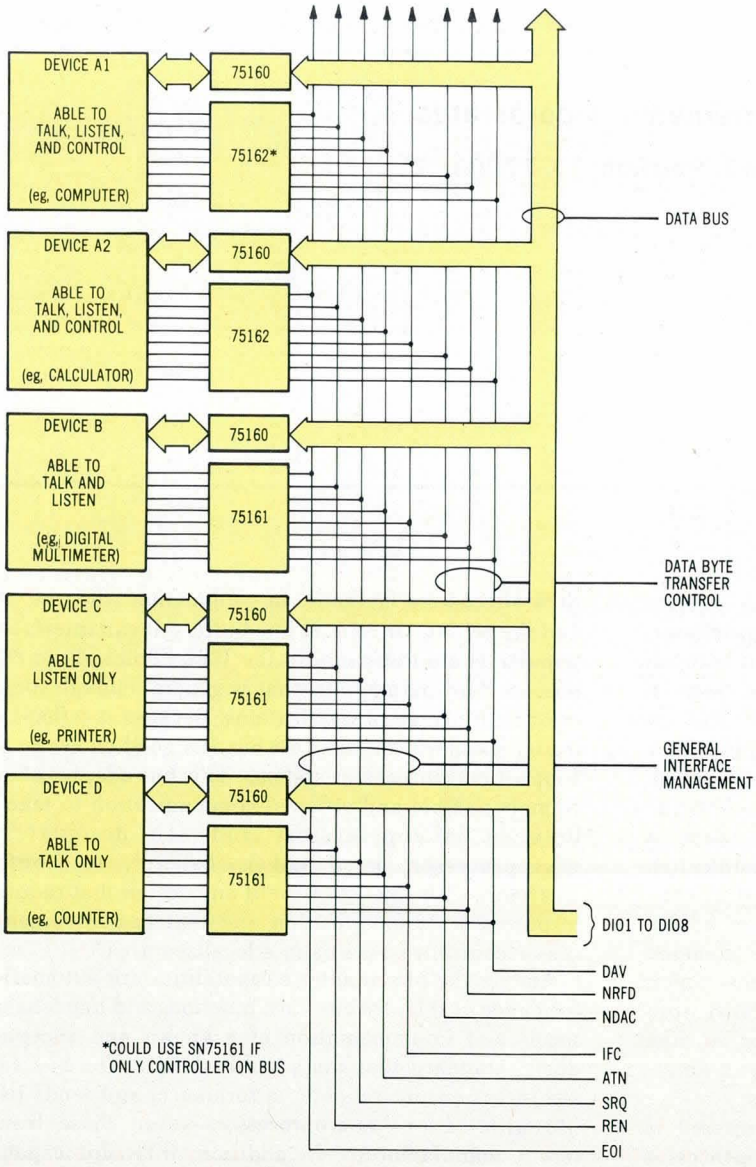


Fig 1 GPIBA microprocessor interface block diagram. In conjunction with line buffers, GPIBA interfaces most popular microprocessors to IEEE 488 bus and allows each processor to act as talker, listener, or controller. Eight data lines and eight control lines achieve IEEE 488 interface

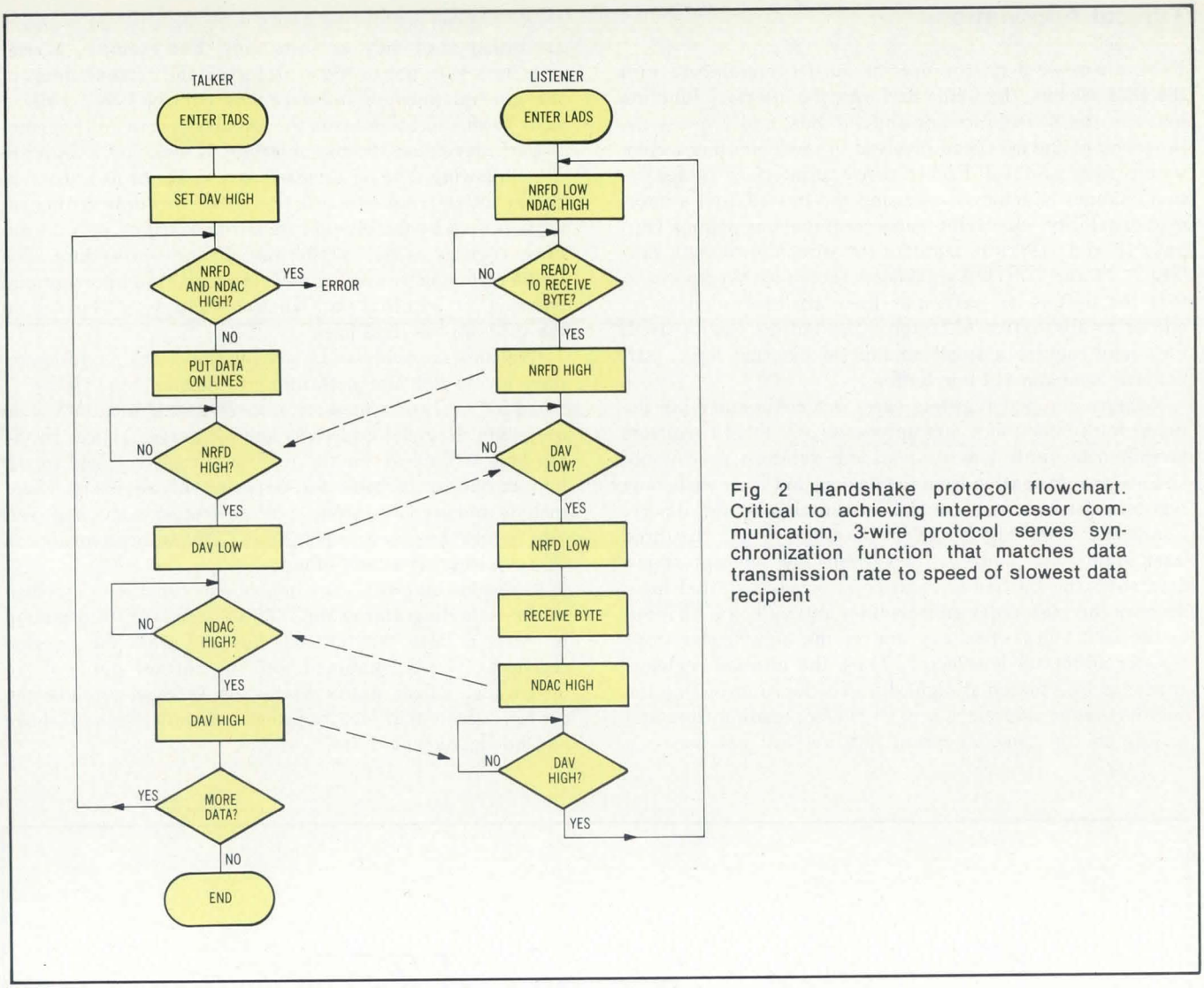


Fig 2 Handshake protocol flowchart. Critical to achieving interprocessor communication, 3-wire protocol serves synchronization function that matches data transmission rate to speed of slowest data recipient

The GPIBA uses the 16-bit bus and the line buffers to communicate with peripheral control devices attached to the IEEE 488 bus. Half of the 16 lines are input/output (DIO1 to DIO8), and the remaining eight lines are network management lines identified in Fig 1. The eight data lines carry all messages for the IEEE 488 bus, and the management lines carry control information from the GPIBA to the bus by means of the line buffers. Five of the eight control lines provide a general interface management function to regulate data transfers across the interface. The Interface Clear (IFC) line is asserted by the system controller to set the interface system into a known quiescent state; then, the system controller becomes the controller in charge. An Attention (ATN) signal is sent by the controller in charge. When ATN is true (low), interface commands are sent across the DIO lines; when ATN is false (high), these lines carry data. The Service Request (SRQ) line is set true by a device to indicate a need for service. A Remote Enable (REN) signal is sent by the system controller to select control either from the front panel or from the IEEE 488 bus. End or Identify (EOI) indicates the end of a message block when the ATN signal is false. If the ATN signal is true, EOI indicates that the controller is requesting a parallel poll.

Critical to achieving interprocessor communication, the remaining three lines—Data Valid (DAV), Not Ready for Data (NRFD), and Not Data Accepted (NDAC)—are all data byte transfer control lines that regulate the handshaking process. These lines control the transfer of each byte across the data lines from the controller or from a talker to one or more listeners. The DAV line is controlled by a data source to show when valid data are present on the bus. NRFD is sent by an acceptor to indicate readiness for the next byte. NDAC is set false by an acceptor when it has latched the data from the input/output lines.

A handshake procedure, which ensures proper data transfer, is controlled by a source to indicate to an acceptor a readiness to receive the next byte of information. The 3-wire handshake protocol serves a critical synchronization function. No new data will be sent until each device addressed to listen has received the last byte of a transmission and indicated that it is ready for the next. This method of asynchronous communication is important in multiprocessing applications because it ensures that the data rate is suited to the slowest active listener and guarantees compatibility across a wide range of devices. Fig 2 shows the detailed operation of the 3-line handshaking protocol.

Typical Applications

Used whenever a microprocessor must communicate with the IEEE 488 bus, the GPIBA performs the interface function between the microprocessor and the bus, and relieves the processor of the overhead involved in implementing a communications protocol. Fast response to interface configuration changes is achieved by using the bus adapter's interrupt capability, which eliminates continual bus polling. Outputs TE and $\overline{\text{CONTROL}}$ regulate the direction of data flow (Fig 3). TE and $\overline{\text{CONTROL}}$ signals are routed within devices so that the buffers on particular lines are controlled as required by the GPIBA. Although other buffers can be used, they may require a small amount of external logic, particularly near the EOI line buffer.

Memory mapped registers carry out communication between the GPIBA and a microprocessor. Of the 13 registers identified in Table 1, 6 are read only registers used to obtain status information from the device, and 7 are write only registers used to pass control information to the device. Connected to the register select lines, RS0 to RS2, the three least significant address lines from the microprocessor determine the particular register selected. External logic decodes the high order address lines and pulls the $\overline{\text{CE}}$ input to the GPIBA low when any one of the eight consecutive register addresses is selected. Thus, the internal registers appear to be situated at eight different locations within the microprocessor address space. Of course, reading from and writing to the same apparent location will not access a single register within the GPIBA twice because all registers are either read only or write only. For example, a read operation with RS0 to RS2 as 011 gives the current status of the general purpose interface bus control lines, while a write to this location loads the auxiliary command register.

Each device on the bus interface is assigned a 5-bit address allowing it to be accessed as a talker or as a listener. Set by an external switch before power is applied, this address is read by the microprocessor and written into the address register as part of the initialization procedure. The GPIBA responds by causing a My Address (MA) interrupt and entering the required state when this address is detected on the IEEE 488 bus data lines.

Registers are accessed by placing the relevant address on lines RS0 to RS2 and performing a memory read ($\overline{\text{WE}}$ = 1 and DBIN = 1) or a memory write ($\overline{\text{WE}}$ = 0 and DBIN = 0) operation. Register addresses and bit usages appear in the top half of Table 1 for the read only registers, and in the bottom half of the table for the write only registers. These include remote call, group execute trigger command, service request has occurred (and the GPIBA is the controller in charge), interrupts, and others.

A 488 state diagram block implements functions described in the state diagrams of the IEEE 488 standard. Information is received from the IEEE 488 bus and from the internal registers, then is combined with the current status of the device (eg, Talker Active Status, or TACS) to produce the control signals that load registers or handle the handshake and bus management lines.

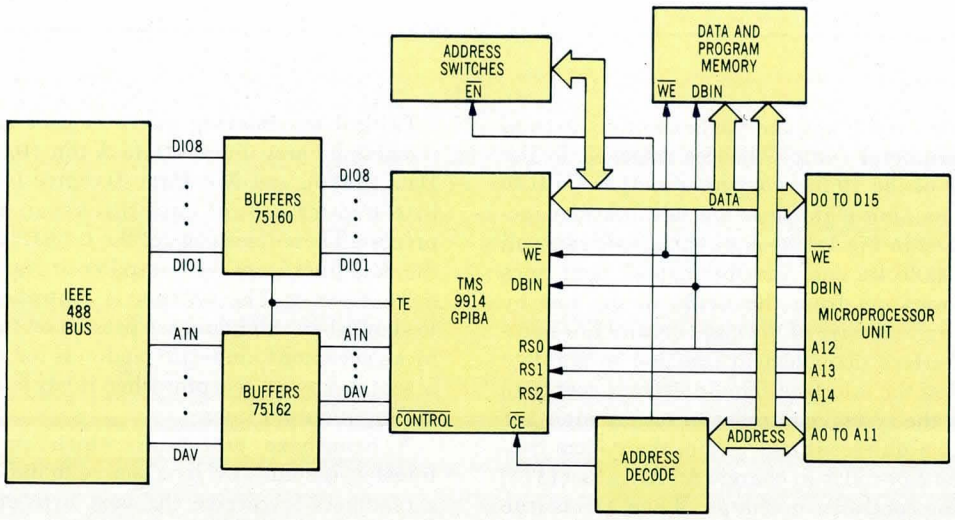


Fig 3 Bus interface block diagram. Apart from interface function, GPIBA also relieves processor of overhead required to implement communications protocol. GPIBA inputs, at right, designate type of transfer and identify one of 13 internal registers. TE and $\overline{\text{CONTROL}}$ outputs, at left, designate transfer direction

TABLE 1

GPIBA Register Assignments

Read Only Registers

Address RS0	Address RS1	Address RS2	Register Name	Contents D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Interrupt status 0	INT0	INT1	BI	BO	END	SPAS	RLC	MAC
0	0	1	Interrupt status 1	GET	UUCG	UACG	APT	DCAS	MA	SRQ	IFC
0	1	0	Address status	REM	LLO	ATN	LPAS	TPAS	LADS	TADS	ulpa
0	1	1	Bus status	ATN	DAV	NDAC	NRFD	EOI	SRQ	IFC	REN
1	0	0	Address Switch 1	edpa	dal	dat	A5	A4	A3	A2	A1
1	1	0	CMD pass through	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1
1	1	1	Data in	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

Write Only Registers

Address RS0	Address RS1	Address RS2	Register Name	Contents D0	D1	D2	D3	D4	D5	D6	D7
0	0	0	Interrupt mask 0	X	X	BI	BO	END	SPAS	RLC	MAC
0	0	1	Interrupt mask 1	GET	UUCG	UACG	APT	DCAS	MA	SRQ	IFC
0	1	1	Auxiliary CMD	C/S	X	X	f4	f3	f2	f1	f0
1	0	0	Address register	edpa	dal	dat	A5	A4	A3	A2	A1
1	0	1	Serial poll	S8	RSV	S6	S5	S4	S3	S2	S1
1	1	0	Parallel poll	PP8	PP7	PP6	PP5	PP4	PP3	PP2	PP1
1	1	1	Data out	DIO8	DIO7	DIO6	DIO5	DIO4	DIO3	DIO2	DIO1

Formats and Operations

Three types of messages can be carried on the IEEE 488 bus between interconnected control devices. Interface messages change the network configuration by addressing devices as talkers or listeners and by transferring devices between remote status and local status. Device dependent messages control device dependent operations, such as range or function selection. Data messages allow readings to be taken for subsequent processing, storage, or hard copy output. Sent by placing the ATN line in the active state, interface messages originate only from the controller in charge. Only one of the devices in the system can be controlled at any one time. Transmissions in the device dependent message and data message categories are not defined in the IEEE 488 standard. These can be sent by any one device acting in the talker mode and received by any number of devices in the listener mode.

The GPIBA can enter the controller mode under either local or remote control. If the device is the system controller, Interface Clear can be sent. The auxiliary register is loaded with the Send Interface Clear (SIC) auxiliary command, which is cleared after the IEEE 488 minimum time of 100 μs by loading SIC with the C/S bit set to zero. The GPIBA enters the Controller Active state automatically when an IFC has been sent to the other devices on the bus. Control can also be obtained when the GPIBA is in the Talker Addressed State and the Take Control (TCT) command is issued by the present controller. If unmasked, an Unrecognized Command Group (UCG) interrupt occurs with an Accept Data State (ACDS) holdoff. The local microprocessor then reads the command from the Command Pass Through Register before releasing the holdoff with a DACR auxiliary command. The device becomes controller in charge when the previous controller releases the ATN line.

When in the controller state, commands are sent over the bus by loading them into the Data Out register. The handshaking operations are completed automatically by the GPIBA with a byte that is generated by a byte output interrupt. The ATN line is asserted until the GPIBA can be put into the controller idle state or the controller standby state, using either the Release Control (RIC) or the Go to Standby (GTS) auxiliary commands. Twenty-five different addressed and universal commands that can be sent while the GPIBA is in the controller state appear in Table 2.

A device that must send data (or device dependent control information) across the bus places the GPIBA in the talker addressed state. To implement the talker function locally, the host microprocessor loads the auxiliary command register of the GPIBA with the Talk Only command. This would normally occur in a system without a controller, or when the controller addresses itself to talk.

TABLE 2

GPIBA Commands

Command	Acronym
Addressed command group	ACG
Device clear	DCL
Group execute trigger	GET
Go to local	GTL
Listen address group	LAG
Local lockout	LLO
My listen address	MLA
My talk address	MTA
My secondary address	MSA
Other secondary address	OSA
Other talk address	OTA
Primary command group	PCG
Parallel poll configure	PPC
Parallel poll enable	PPE
Parallel poll disable	PPD
Parallel poll unconfigure	PPU
Secondary command group	SCG
Selected device clear	SDC
Serial poll disable	SPD
Serial poll enable	SPE
Take control	TCT
Talk address group	TAG
Universal address group	UAG
Unlisten	UNL
Untalk	UNT

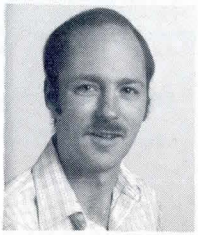
The GPIBA can be placed in the listener addressed state, locally, by loading the auxiliary command register with the Listen Only command. This would normally occur in a system without a controller, or when the controller addresses itself to listen. Alternatively, the listener function is enabled when the controller in charge sends My Listen Address (MLA) for the device across the system bus. Since there can be a number of listeners active at any one time, neither of these operations affects any of the other devices. The Unlisten command is used to clear all listeners if some devices are not required to receive the data.

The GPIBA can be operated with or without the secondary addressing feature. By setting a bit in one certain register, the GPIBA is made to respond only to primary addresses. If secondary addressing is required, it is easily accomplished by setting one bit in a specific mask during initialization. Then, conditions in the system determine how the GPIBA will respond to data supplied as input.

Whenever an event capable of causing an interrupt occurs, the corresponding bit in one of the interrupt registers is set. When the microprocessor responds to the interrupt, it first reads the contents of interrupt registers 0 and 1 to find the cause, and then executes the appropriate interrupt service routine. The interrupt registers are cleared when they are read. If the interrupt register is being read when an interrupt occurs, the associated bit is stored until the read cycle has been completed and only then introduced into the interrupt register. In a polling system, in which the status registers are periodically examined by the host microprocessor, the interrupts are not used. They may be disabled without affecting the holdoffs on unrecognized addresses or commands.

Software Considerations

Typically, and regardless of the application, the low level software that controls the IEEE 488 standard protocol remains basically the same. It consists of routines that initialize the GPIBA, set all devices in the system to their proper initial state (talker, listener, or controller), and establish the message format. High level software that controls system data transmitted on the buses will be application dependent for the most part. Type and number of devices, and the manner in which they are used, determine the routines required to perform necessary tasks. Most application dependent routines reside in read only memory.



Since joining Texas Instruments in 1977, Gerald R. Samsen has been involved in design engineering, systems engineering, and marketing. He is currently 9900 family components strategy manager in Houston, Texas, and holds a BSEE from Ohio State University.

Roger D. Hudson, who joined Texas Instruments in 1978 as 9900 family components strategy manager, is now a field systems engineer in Huntsville, Alabama. He has a BSEE from the Georgia Institute of Technology and an MBA from Augusta College.

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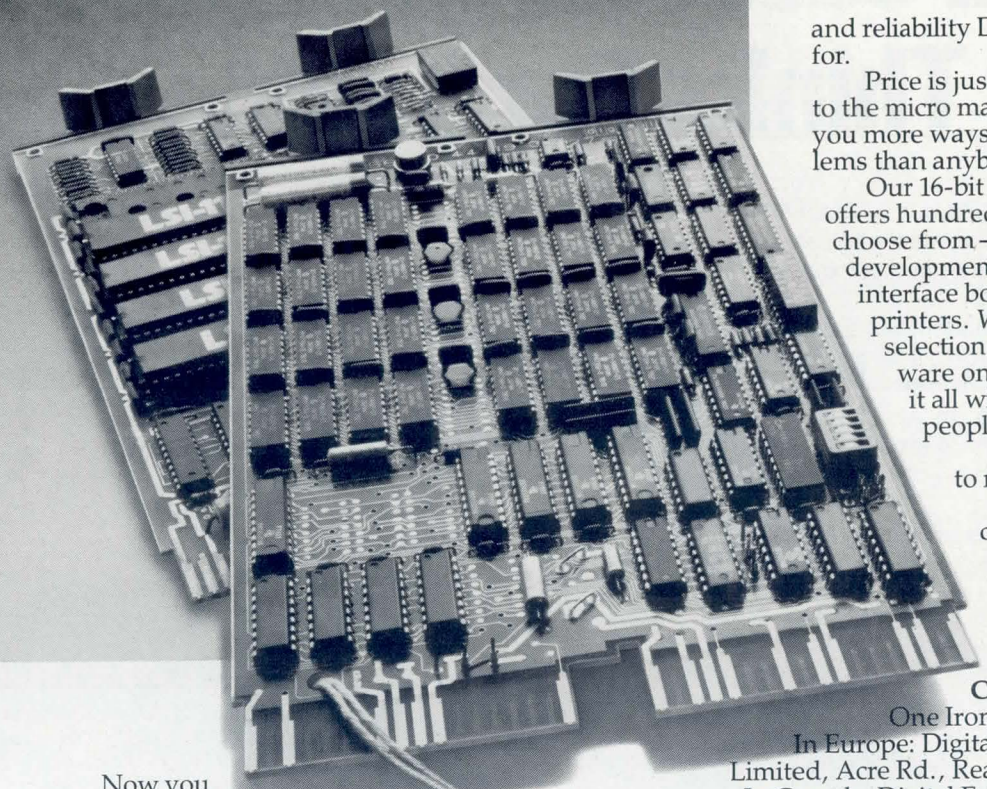

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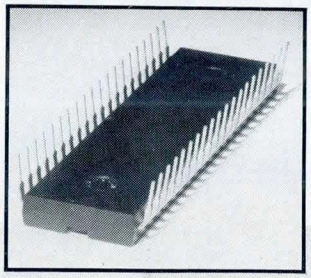

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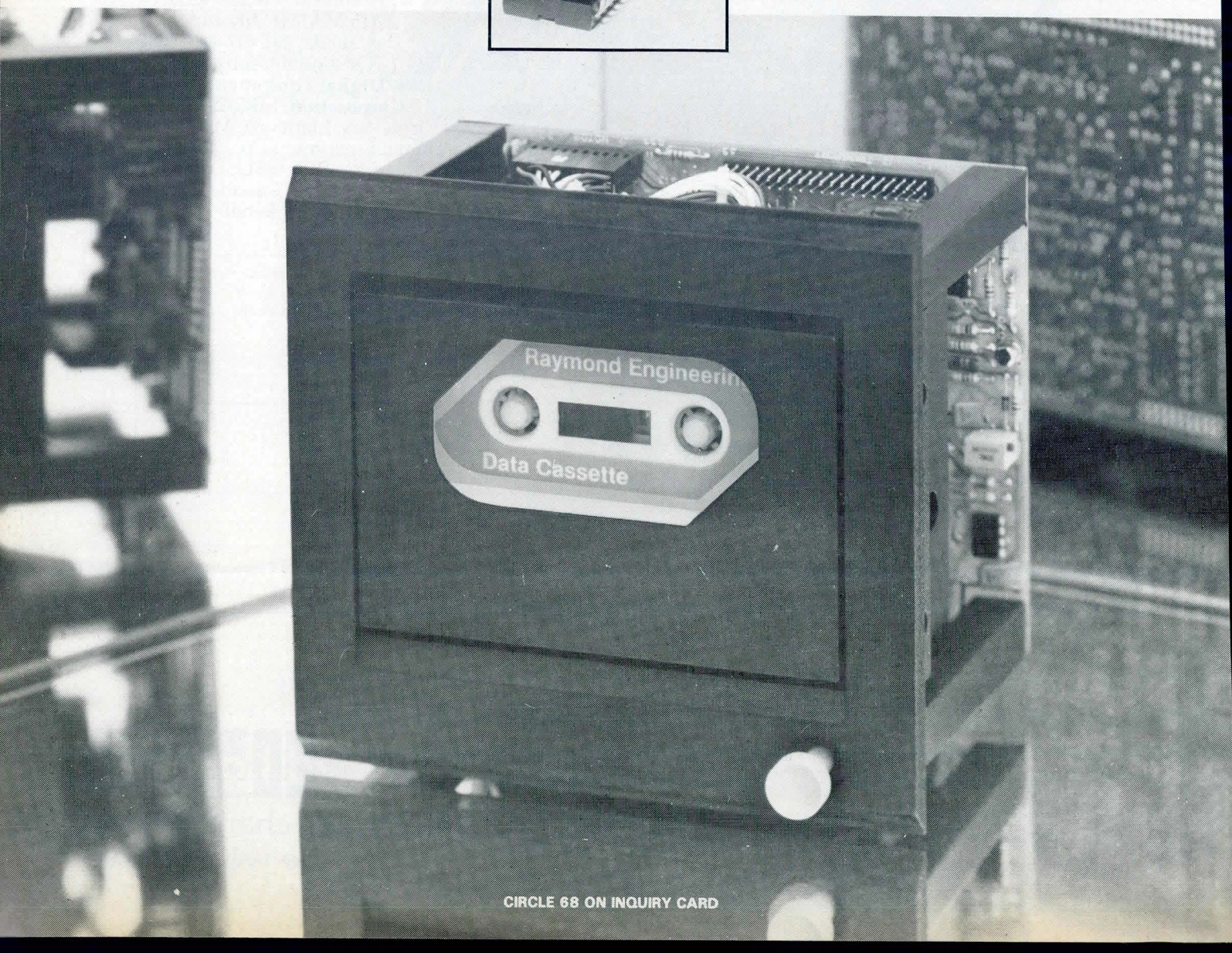

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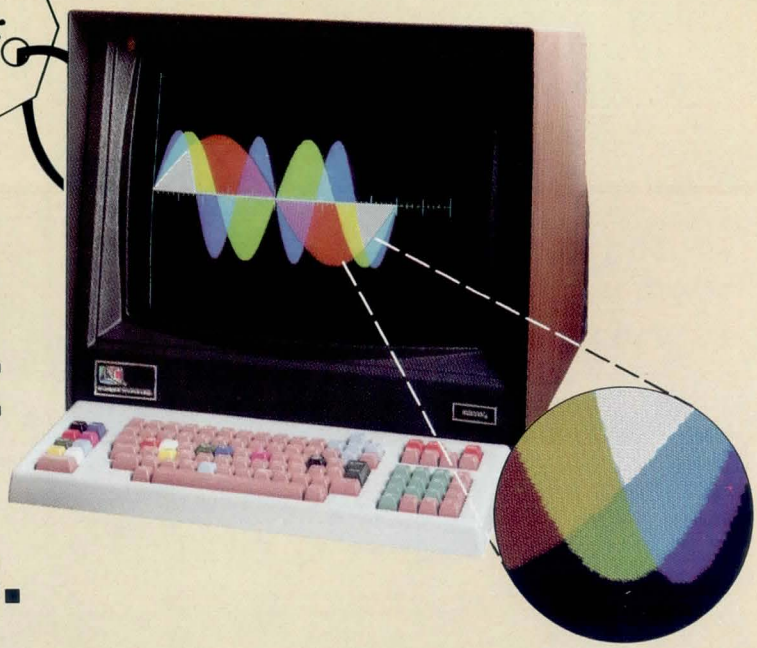

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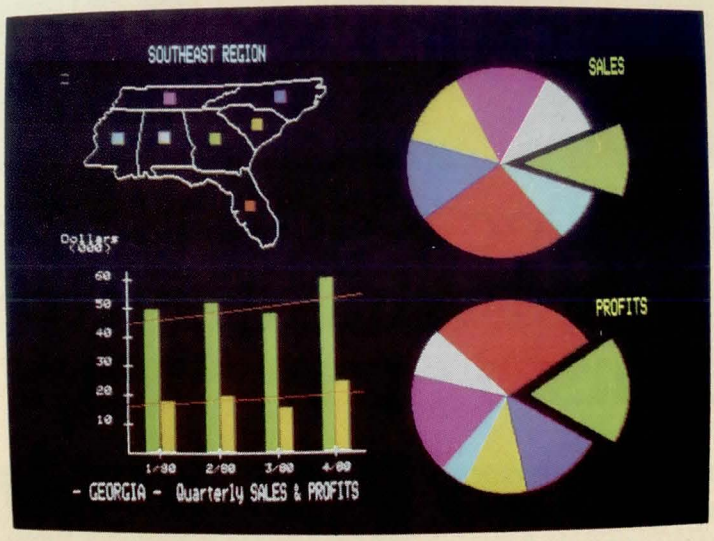

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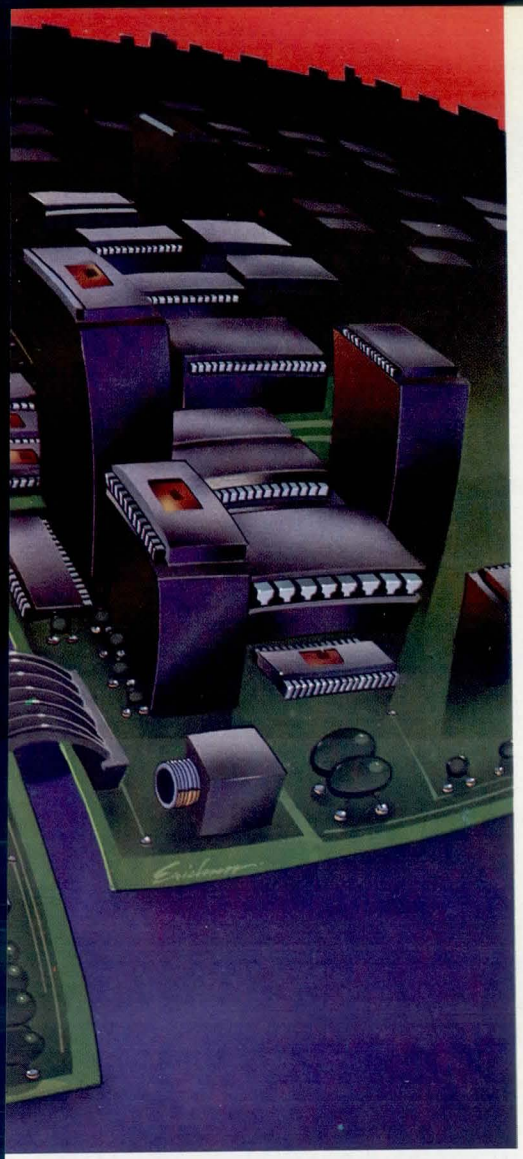

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	iAPX 88	ASM88, PL/M Pascal, FORTRAN ICE88™
16-BIT	iAPX 86	ASM86, PL/M Pascal, FORTRAN ICE86™ ICE86/88™ Extensions ASM89 Real Time Breakpoint Facility (RBF)
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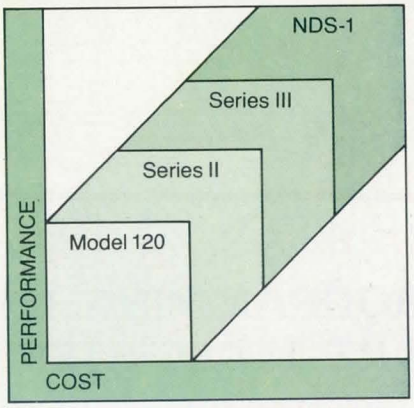

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PROGRAMMING THE 8086— PART 1: REGISTER INSTRUCTION ORGANIZATION

Stanley Mazor Intel Corporation
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Numerous articles have been published about the architecture and hardware capabilities of the 8086 microprocessor since its introduction—and, more recently, about the 8088, which uses virtually the same instruction set. However, little technical material has appeared on the symbolic assembly language and some of the advanced features of the 8086 assembler. This column—first of a 3-part series on 8086 programming techniques—focuses on register oriented instructions and immediate data coding, and contains sample assembly language programs that demonstrate compatible 8-bit and 16-bit data handling operations. This information applies equally to the 8088 processor. Part 2 will cover addressing modes and Part 3 will consider procedures and parameter passing.

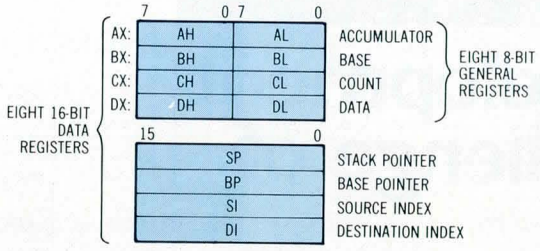

Fig 1 8086 programmable registers. Of eight 16-bit registers, four can be accessed either as word registers or as 8-bit byte registers. Register nomenclature determines mode of access

All programmable registers in the 8086 microprocessor can be used for arithmetic, logic, and shifting operations; they also perform special functions as indicated by their nomenclature.

Accumulator (AX)	I/O and multiply/divide
Base (BX) register	Base address
Count (CX) register	Shift or loop counter
Data (DX) register	Data register
Stack pointer (SP)	Addresses top of stack
Base pointer (BP)	Addresses stack frame
Source index (SI)	Index register
Destination index (DI)	Index register

Four of these programmable registers—the accumulator, base, count, and data registers—are general registers that can be accessed either as 8-bit (byte) or as 16-bit (word) registers (Fig 1). When programming in symbolic assembly language, the programmer selects both the register and the data type by using the appropriate 2-character register abbreviation (eg, AH, AL) in the instruction.

Data Type Control

In Fig 1, the 8-bit general registers are designated using an H (high order half) or an L (low order half) as the second character of their nomenclature. When these four registers

(continued on page 132)

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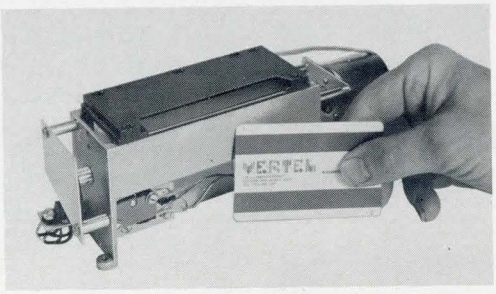

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are used for 16-bit operations, the letter X replaces the H or L (eg, AX). The 8086 assembler uses the register nomenclature to establish the type of operation code to generate for either byte or word operations. For example, INC BH causes the assembler to generate a machine operation code that adds 1 to the 8-bit (byte) quantity in the high order byte of the base register, whereas INC BX generates machine code that adds 1 to the 16-bit word quantity in the base register. The symbolic operation code, INC, contains no explicit reference to the type of data (word or byte) involved. Instead, the assembler uses the register designated in the operand to determine what type of operation code to generate.

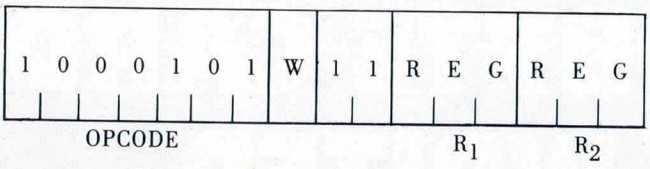
Machine Codes

Most 8086 operation codes contain a W-bit that specifies whether the data constitute an 8-bit byte or a 16-bit word. This bit is set to 1 for word operations and cleared to 0 for byte operations. The assembler generates machine codes with the W-bit set to the proper value for the type of data to be operated upon, depending on the symbolic register specified by the programmer, as follows:

INC BX	Set W-bit for word data
INC BH	Clear W-bit for byte data

Double-Operand Instructions

Some instructions, such as MOV, require two register references. In this case, the data type must be the same in both references and the symbolic register names must designate the same register type. For example, the machine code for the MOV register instruction is



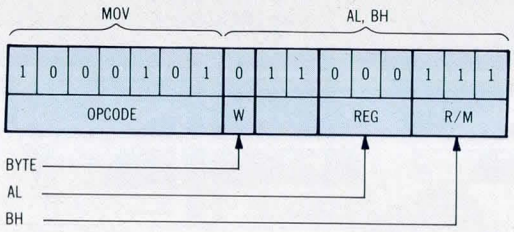


Fig 2 Assembly language example. Symbolic instruction MOV AL, BH (move BH byte to AL) determines each field of corresponding machine code instruction. R/M field can designate either register or operation mode

where R_1 and R_2 each designate one of the eight registers and the W-bit indicates the data type. The assembler uses the register names to generate the correct machine code for the register number. The assembly language example in Fig 2 shows how each field of the machine code instruction is filled by using information from the symbolic instruction, MOV AL,BH. The Table shows several double-operand instructions along with their symbolic operation codes and functional descriptions.

(continued on page 134)

Double Operand and Immediate Instructions

Symbolic Opcode	Operation	Double-Operand Instruction	Immediate Mode Instruction
MOV	Move	$R_2 \rightarrow R_1$	Data $\rightarrow R_1$
ADD	Addition	$R_1 + R_2 \rightarrow R_1$	$R_1 +$ Data $\rightarrow R_1$
SUB	Subtraction	$R_1 - R_2 \rightarrow R_1$	$R_1 -$ Data $\rightarrow R_1$
CMP	Compare	$R_1 : R_2 \rightarrow$ Flags	$R_1 :$ Data $\rightarrow$ Flags
AND	AND	$R_1 \wedge R_2 \rightarrow R_1$	$R_1 \wedge$ Data $\rightarrow R_1$
TEST	Bit Test	$R_1 \wedge R_2 \rightarrow$ Flags	$R_1 \wedge$ Data $\rightarrow$ Flags
OR	OR	$R_1 \vee R_2 \rightarrow R_1$	$R_1 \vee$ Data $\rightarrow R_1$
XOR	Exclusive OR	$R_1 \oplus R_2 \rightarrow R_1$	$R_1 \oplus$ Data $\rightarrow R_1$
XCHG	Exchange	$R_1 \leftrightarrow R_2$	
IN	Input	AL (Port #)	

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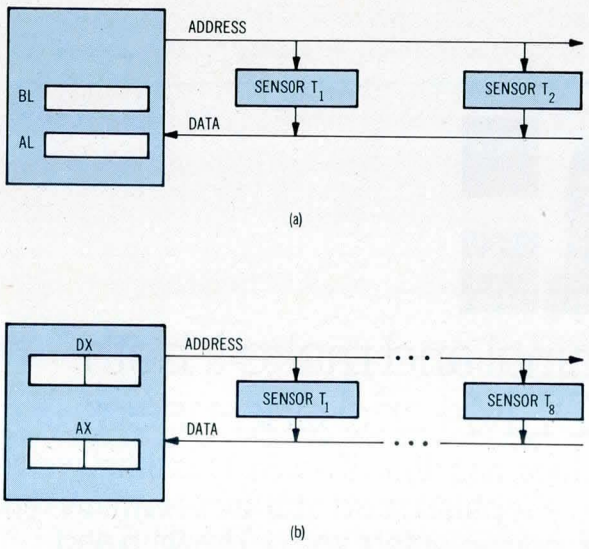

Fig 3 Application block diagram. In (a), microprocessor samples two sensors and computes average temperature using Program 1. In (b), extension to eight sensors and 16-bit data uses modified version of Program 2

System Applications

Suppose a microcomputer samples two digital temperature sensing and converting devices, then computes the average value of the two temperatures [Fig 3(a)]. It is known that sensors T_1 and T_2 produce 6-bit binary values representing temperatures in the 10 to 60 °C range. A solution is found by computing first the sum ($T_1 + T_2$) and then the average value (SUM / 2). With binary logic, division is achieved by shifting the sum one bit position to the right. Symbolic assembly language for this problem solution is given in Program 1. If sensor T_1 reads 16 and sensor T_2 reads 20, the result of (16 + 20) / 2 = 18 will appear in register BL.

Since both sensors transmit data to the microprocessor across the same set of data lines, an address from the microcomputer is used to select and enable the appropriate converter's output to the data bus. The input (IN) command in steps 1 and 3 of the program contains the device address, symbolically represented as T_1 or T_2 but actually an 8-bit code. This device address selects a sensor and transfers sensor data to the AL register within the microprocessor. It is necessary to save the T_1 value in the BL register in step 2 because the value from T_2 also must be read, and data are read as input only into the AL register.

Addition of the AL and BL registers in step 4 leaves the result in BL. Step 5 divides the data in BL by two, by shifting one bit position to the right, computing the average temperature value in BL. This illustrates an advantage of the 8086 over earlier microprocessors: arithmetic and shifting operations may be performed on data in any register, not just on data in the accumulator.

Although the previous example dealt with 8-bit data for all operations, the same problem could be solved using 16-bit data. It is only necessary to change the register designations in Program 1 because the register name alone distinguishes between byte and word operations. Suppose, then, that a microcomputer is to sample eight digital temperature sensors [see Fig 3(b)] and to compute their average temperature reading. Now, the 12-bit binary values represent temperatures in the range 10 to 300 °C. Program 2 can sample each temperature sensor in a loop and accumulate the sum of their temperature readings. Then, shifting the resultant sum three bit positions to the right divides this result by eight to obtain the average temperature as shown.

When several I/O devices are to be polled, it may be preferable to use the indirect I/O address capability of the 8086 by selecting the DX register to address the device. In this case, a program loop counts from 0 to 14, spanning the eight physical addresses 0, 2, 4, ... , 14. In step 6 of Program 2, the compare operation actually subtracts 14 from DX and leaves the original value in the register. The result of the comparison affects only the status flags. Following this step, the jump instruction in step 7 tests the condition specified in the flag register and branches to step 3 if condition "less than or equal to" is true. If the condition is not true, and DX contains a value in excess of 14, the next sequential instruction will execute. Here, in steps 8 and 9, the program loads a 3 into the CL counter register and shifts the BX register three bit positions to the right.

(continued on page 136)

PROGRAM 1

Average Temperature Computation from Two Sensors

Step	Mnemonic Opcode	Symbolic Operands	Comment
(1)	IN	AL, T1	; Input byte to AL
(2)	MOV	BL, AL	; Save byte in BL
(3)	IN	AL, T2	; Next byte to AL
(4)	ADD	BL, AL	; Form sum in BL
(5)	SHR	BL, 1	; Compute average

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PROGRAM 2

Average Temperature Computation from Eight Sensors

Step	Symbolic Label	Mnemonic Opcode	Symbolic Operands	Comment
(1)		MOV	BX, 0	; Set sum = 0
(2)		MOV	DX, BX	; Set port number = 0
(3)	STP 3:	IN	AX, DX	; Input word to AX
(4)		ADD	BX, AX	; Add to BX
(5)		ADD	DX, 2	; Advance port number by 2
(6)		CMP	DX, 14	; Is port $\leq$ 14
(7)		JLE	STP 3	; Yes go to step 3
(8)		MOV	CL, 3	; Set shift count to 3
(9)		SHR	BX, CL	; Divide by 8 by shifting

Immediate Data

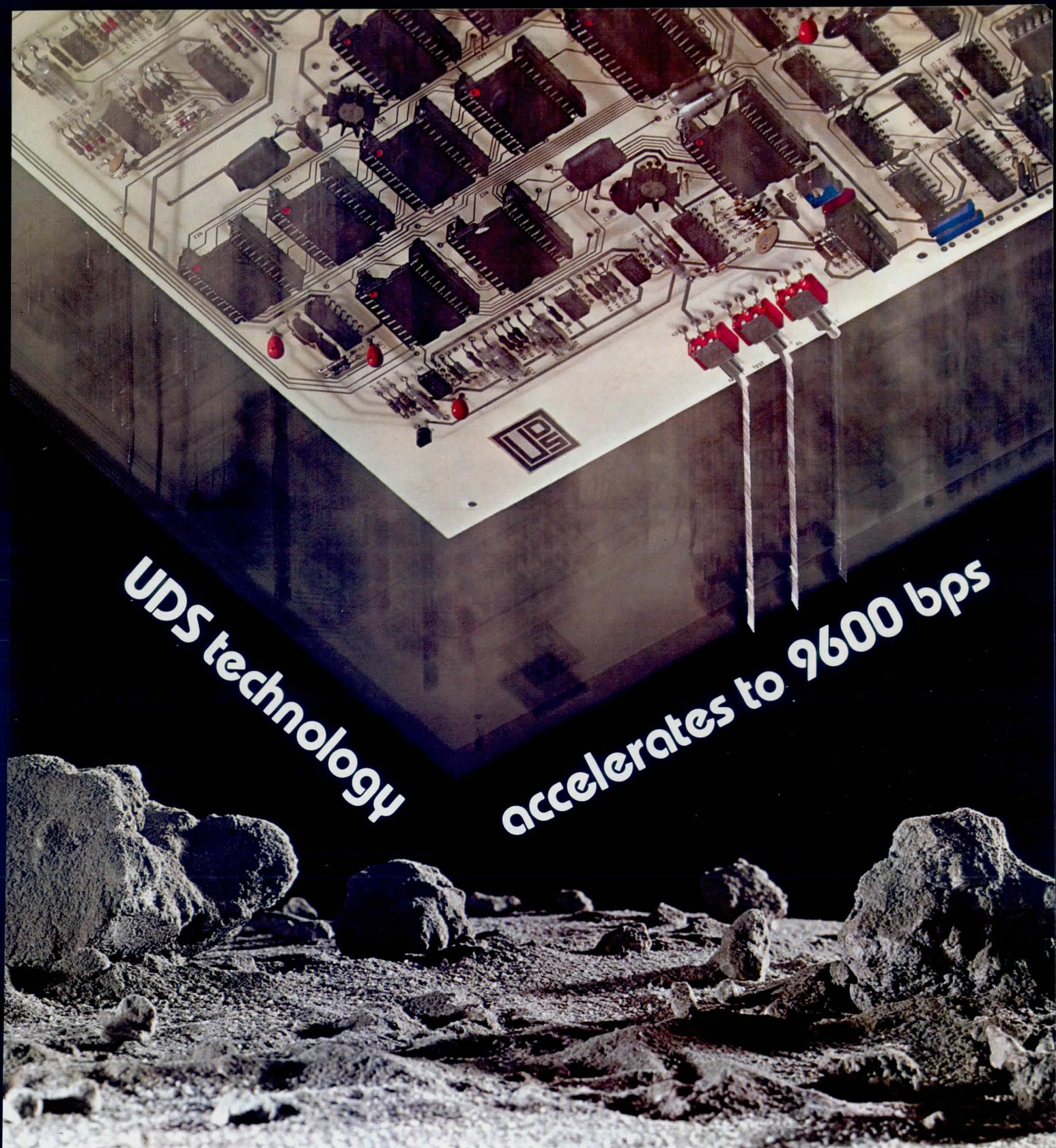
Several instructions in Program 2 contain immediate data as the second operand, rather than a register reference. These data occupy a byte or word of program memory immediately following the operation code. Some of the instructions listed in the Table are used for both register operations and operations on immediate data.

Unlike earlier assemblers, such as that for the 8080, the 8086 assembler does not use separate symbolic operation codes for immediate instructions (eg, MVI on the 8080). Programmers enter the same symbolic operation code, such as MOV, regardless of the data type or mode of operation. The assembler can recognize that a constant is being used as an instruction operand and assemble the appropriate immediate mode machine code. It determines whether immediate instructions need a byte constant or a word constant by checking the type of register designation coded in the instruction. For example, MOV BL,0 generates an 8-bit constant in the instruction with the W-bit reset, whereas MOV BX,0 generates a 16-bit constant with the W-bit set to 1.

An exception to this rule occurs in arithmetic operations, such as those in steps 5 and 6 of Program 2, where 16-bit word constants are required. If the constant can be represented in 8 bits, a special bit set within the instruction indicates to the 8086 that only an 8-bit byte constant is present and that this value must be expanded to 16 bits. This technique saves eight bits of space in the program and is handled automatically by the 8086 assembler. Overall, the assembler's treatment of immediate mode instructions is straightforward for the programmer; only one symbolic operation code is required for the register and immediate data modes of both the word and the byte form of an instruction.

Summary

Two brief examples demonstrate the 8086 instruction set symmetry and illustrate how the assembler handles both 8-bit bytes and 16-bit words. A total of eight registers for arithmetic operations simplify programming, yet certain special functions always use predefined registers: the AX register for I/O, the DX for I/O pointers, and the CX register for counting. Register and immediate data are handled by a single operation code for each basic instruction, reducing complexity of the assembly language. As a special space saving technique, the assembler handles words of immediate data as though they were bytes whenever possible, and instructs the 8086 to expand the byte before using its full, 16-bit value as immediate data.



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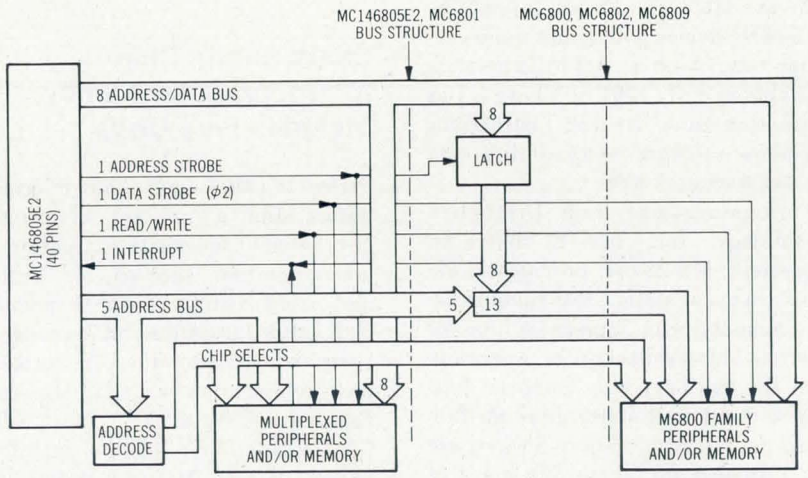

Multiplexed bus structure of MC146805E2 MPU. Eight low order address bits appear on bus during first portion of bus cycle; during second portion of cycle data bytes share same lines. Five high order address bits as well as read/write signal that indicates data transfer direction are outputs. Peripheral and memory ICs can be interfaced directly with bus; nonmultiplexed peripherals and industry standard memories are connected to MPU through octal latch to demultiplex address

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The MPU can address 8k bytes of memory and I/O registers, with address space divided into internal memory space and external memory space. Internal memory space, located within the first 128 bytes of memory, consists of the I/O port locations, timer locations, and 112 bytes of RAM. The MPU can read from or write to any of these locations. A program write to onchip locations is repeated on the external bus to permit offchip memory to duplicate the content of onchip memory. Program reads to onchip locations also appear on the external bus, but the MPU accepts data only from the addressed onchip location. Any read data appearing on the input bus are ignored.

A stack pointer is used to address data stored on the stack. Data are stored on the stack during interrupts and subroutine calls. When data are removed, the stack pointer is incremented. 64 bytes of RAM are available for stack usage.

Within the timer is a single 8-bit software programmable counter with 7-bit software selectable prescaler that can be preset under program control and decrements towards zero. When the counter decrements to zero, the timer interrupt request bit is set. At this point, the computer allows the software to determine the number of internal or external input clocks having occurred since the timer interrupt request bit was set. At any time the counter may be read by the processor without disturbing the count. Contents of the counter become stable prior to the read portion of a cycle and do not change during the read. The timer interrupt request bit remains set until cleared by the software.

Ten different addressing modes allow optimum programmed codes in most situations. Various indexed addressing modes locate data table, code conversion tables, and scaling tables anywhere in the memory space. Short indexed accesses are single-byte instructions, while the longest instructions (three bytes) permit access to tables throughout memory. Short and long absolute addressing is also included. Two-byte direct addressing instructions access all data bytes in most applications. Extended addressing permits jump instructions to reach all memory.

Three versions of the MPU are available: a plastic package with thermal resistance of 100 °C/W, and cerdip and ceramic packages with 50 °C/W. Supply voltage (V_{DD}) is −0.3 to 8 Vdc. The operating temperature range is 0 to 70 °C, with storage at −55 to 150 °C.

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(continued on page 140)

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

and hardware; built-in P/ROM programmer, and built-in printer interface for the CDP18S050 matrix high speed printer.

The CRT display has full-screen text editing that provides instant verification of program development and changes. Dedicated keys provide cursor positioning including tab, overtype, character or line insertion, character or line deletion, scrolling (next or previous line of buffer), and windowing (next or previous page of buffer).

Program development is simplified by the CDOS disc file management and operating system. Because CDOS references files by name rather than by track number, the user has access to the files and need not be concerned about file size or disc space allocations. In addition, the file has improved protection from inadvertent damage.

The system loads binary files, providing users with faster loading and reduced storage needs. Assembler outputs can be directed to a disc file or line printer with symbol table and references either added or suppressed.

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8″ Floppy Disc Drive

Compatible with TRS-80 models I and II, Apple II, and S-100 systems, the 8″ (20-cm) MS-800 disc drive has a capacity of 77 tracks, 26 sectors/track, 128 bytes/sector, for a total of 256,256 bytes, 2.2 times the capacity of a 5.25″ (13.3-cm) drive. Data transfer rate is 256k bits/s, 1.6 times the transfer rate on the smaller disc. Track-to-track access time is 10 ms.

In a 4-drive configuration, the system—offered by Matchless Systems, 18444 S Broadway, Gardena, CA 90248—provides a storage capacity of over 1M bytes on an Apple or 2M bytes on a TRS-80 model II. The drives are powered independently of the systems with which they are used. Every drive is completely assembled and tested.

Circle 463 on Inquiry Card

Multibus Compatible CMOS Microcomputer Uses Only 1W of Power

CBC series single-board microcomputers, Multibus compatible and executing the Z80 instruction set, operate at up to 20:1 reduced power dissipation over many comparable units. First to be available, the 800 will initially be a 2.5-MHz device with a minimum execution time of 1.6 μs. A 4-MHz version, available in early 1981, will have a 1-μs instruction time. Its 158 instructions will allow software compatibility with the Z80, 8085, and 8080.

Various versions from Diversified Technology, Inc, 112 E State St, Ridgefield, MS 39157, provide 4k, 8k, or 16k bytes of static CMOS random access memory with jumper option for external battery backup or operation from the auxiliary bus. Onboard RAM runs without wait states allowing full-speed processor operation. Sockets are also provided for up to 32k bytes of CMOS or NMOS read only memory, or P/ROM.

Optional operating systems will allow a broad range of languages and utilities. CP/M 2.2 from Digital Research, Inc will provide access to assemblers, text editors, and debuggers plus high level languages such as FORTRAN, Pascal, PL-1, and BASIC. In addition, the company's EPROM based, multiuser, interactive operating system called IOS-4 will be available. This system is based on International Standard FORTH (1979), and provides assembler, text editor, disc operating system, FORTH compiler, multitasker, ROM compiler, and interactive compile/debug interpreter. The compact object code generated by the ROM compiler allows the entire language and operating system to be located in 14k of EPROM.

Bus arbitration logic is offered for multiple masters to share the system bus in a serial or parallel priority mode of operation. Two bus interface versions will allow either standard Multibus compatibility or interface to a CMOS Multibus standard.

Two peripheral interface chips incorporate 44 programmable, parallel I/O lines and four 16-bit programmable counter-timers. Serial RS-232 communications are provided by a universal asynchronous receiver/transmitter chip (UART) with software programmable standard transmission rates up to 9.6k baud. Onboard logic will allow for 20 prioritized interrupts with three operating modes. User options will be selected by movable shunts allowing ease of configuration.

Circle 464 on Inquiry Card

CMOS Single-Chip Microcomputer Family Includes Five Units

Series 40 CMOS single-chip microcomputers and a full set of program development tools with evaluation and documentation support, as well as associated NMOS and CMOS memories and CMOS I/O peripheral circuits, are being introduced to the U.S. market by OKI Semiconductor, 1333 Lawrence Expressway, Suite 401, Santa Clara, CA 95051. Three of the microcomputers (MSM5840, MSM5842, MSM5845) are currently available and the others (MSM58421 and MSM58423) will be available in the first and second quarters of 1981, respectively.

The 5840, a single-chip peripheral device, contains a 2k by 8-bit mask ROM, 128 x 4-bit RAM, programmable timer counter, and 30 I/O lines. It features an 8-bit parallel I/O port and 4-bit wide data paths, and permits connection to an 8-bit system. Onboard ROM can be externally expanded via a multiplexed bus structure, enabling use of 2k of ROM internally and 2k externally or 4k of external ROM, using an external ROM or EPROM for a 2-chip solution.

Three different program development package options are offered, each designed around existing industry standard systems. The MPSP-I, based on Intel's ISIS software, consists of MPB-201/203 boards and ISIS compatible disc containing cross-assembler, download, and execution software; the MPSP-C, based on Digital Research's CP/M operating software, consists of MPB-201/203 boards with CP/M compatible disc containing cross-assembler, download, and execution software; and the MPSP-S, designed for users who do not own a development system, consists of MPB-201/203 boards and monitor/self-assembler software for paper tape software development, debug, and emulation.

Circle 465 on Inquiry Card

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Single-Board Microcomputer Products Based on 16-Bit CPU

First members of the VERSAmodule™ series of board level microcomputer products and accessories include a single-board microcomputer, chassis, card cage, and realtime multitasking system software package. Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, claims that the microcomputer is the most powerful 16-bit single-board computer yet announced and, when combined with the chassis and system software, provides a total environment for 16-bit applications.

The microcomputer board's CPU is an MC68000 operating at an 8-MHz clock frequency. Features include 16M-byte direct addressing capability, asynchronous data bus, vectored priority interrupts, 32-bit wide internal data paths, 15 general purpose 32-bit registers, 15 addressing modes, two levels of program privilege, exception processing, and architecture optimized for high level language support. A full VERSAbus interface is contained for 16-bit system applications.

Onboard and ROM are accessible by the MC68000 processor. The RAM is offered in either 32k or 64k bytes. It is implemented as dynamic RAM using 4116 type parts with onboard automatic refresh control, plus byte parity with automatic retry. ROM capability is offered by providing eight sockets for industry-standard pinout 5-V ROM, P/ROM, or EPROM devices of up to 64k bytes maximum capacity.

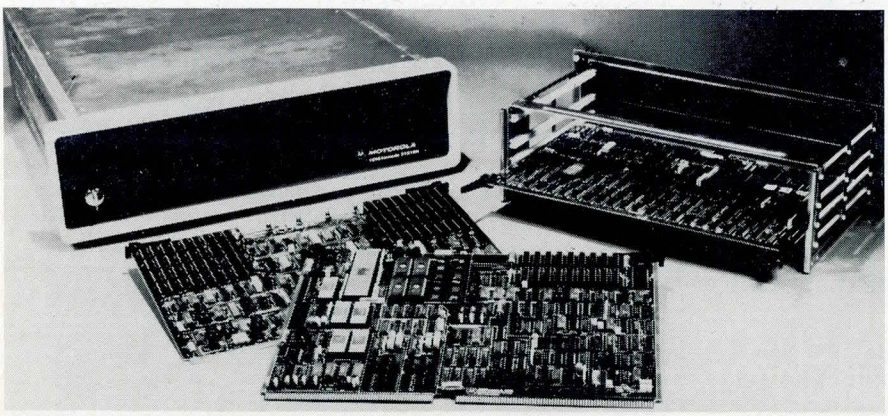
Two independent and versatile serial ports offer several programmable modes of operation and support the RS-232-C terminal or interface in asynchronous operation to 19.2k baud. One serial port also can be user-configured for synchronous operation, and for an RS-422 interface. Parallel I/O is implemented as four independent bidirectional ports, each having eight data lines and two handshake lines, for a total of 32 lines of general purpose parallel I/O capability.

Several powerful timer/counter functions are provided by a programmable timer module integrated into the microcomputer. Three independent 16-bit counters are available to support applications such as frequency measuring, event counting, and interval measuring.

A 4-slot, 24″ (61-cm) deep chassis occupying 5.25″ (13.3 cm) of vertical rack space, and containing power supply and forced air cooling, provides a secure mounting and power environment for the boards. The cage consists of a motherboard and card guides, and is offered separately for applications where serial enclosure, packaging, or power support is required. An expansion kit is optionally available for expansion up to a total of three sections. The standard power supply unit is a regulated switching supply providing 30 A at 5 V, 3 A at 12 V, and 1 A each at 15 and −15 V. It provides a power fail detect capability and generates appropriate power failing and power down signals for distribution on the bus. An optional smaller supply provides 15 A at 5 V, 2.5 A at 12 V, and 1.5 A at −12 V.

The software package features task priority resolution and task dispatching, software and hardware interrupt processing, intertask communication, dynamic allocation and management of RAM, task synchronization, initialization, exception (fault) processing, and modularity, with system generation features. It is memory resident and can be configured by the user to operate out of RAM or a combination of RAM/ROM.

Circle 466 on Inquiry Card



Principal elements of VERSAmodule product family. Shown are 4-slot chassis, boards, and card cage

64k RAMs Enable Design of 512k-Byte, 2-Board Microcomputer

Memory capacity available in much larger computers has been provided on the HP 1000 L series computers from Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, through combining enhanced memory management capabilities with 64k RAMs. The 512k-byte, 2-board microcomputer provides DMA per channel, I/O capabilities, and software features that are usually found on the larger systems and can be used in applications such as communications, process control, automation, and instrumentation where large amounts of main memory are necessary.

Compatible with all other HP 1000s, the L series has a complete IMAGE database management facility for use with its multiprogramming realtime executive operating system. The computers support program development in Pascal, as well as FORTRAN, BASIC, and assembler languages, and meet requirements of the HP 1000 distributed systems network (DSN).

A 128k-byte version, using 16k RAMs, is also available. Memory boards can be added to increase memory to 512k bytes.

U.S. prices for a single L series microcomputer with 512k bytes of 64k RAM main memory is $13,250 for a 2103LK board level processor; $15,450 for a 2103L rack mountable computer; and $33,500 for a model 10 system complete with a CRT terminal, 1.2M-byte flexible disc drive, cabinet, and a 12M-byte Winchester-technology disc. OEM and volume-end-user discounts are available. Prices of the 128k-byte versions begin at $3750. Additional 128k memory boards cost $2500 each.

Circle 467 on Inquiry Card

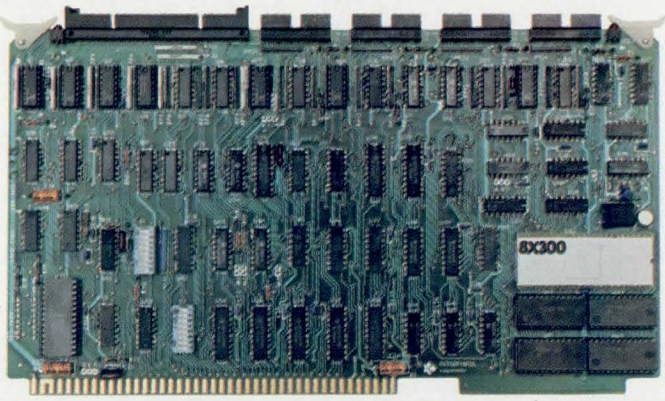
Microcontrol Mastery with Signetics 8X300

Compact Hard Disk Controller Spawns 6 New Controller Designs.

How one company realized design objectives with the world's fastest microcontroller.

Interphase Corporation of Dallas, Texas not only realized their design objectives for a moving-media controller, but were able to create six different high-speed single-board peripheral controllers simply by changing PROMs or modifying the I/O interface.

Their initial design goal was a controller that had to fit on a single Multibus-type circuit board, be highly competitive in both cost and performance, and fit a tight development schedule. The answer to all these requirements was Signetics' 8X300 microcontroller.



Interphase SMD 2180 single-board Storage Module Controller measures only 6.75" x 12" and handles up to four SMD drives. Its closest competition uses twice as much board space and three times as many discretes.

According to Interphase, design requirements dictated the need for a very high-speed microcontroller that would lend itself to a generalized architecture. Moreover, they quickly realized the value of an existing instruction set and readily available development tools to minimize design time.

With the generalized architecture developed around the 8X300, they produced a 5440 Cartridge Disk Controller on a single board that measures only 6.75"X12". Equivalent discrete logic controllers require at least three times the board space and use three or four times as many discretes.

A significant cost savings in engineering time was realized when the basic design led to the development of six other controller products: two Storage Module Controllers, a Winchester Disk Controller, Color Graphics Expander, 1-Mbit Communication Protocol Controller, and a I/O Applications Language Interpreter.

To a large degree, the "elegant simplicity" of the Interphase designs is due to the 8X300's exceptional speed. At 4 million operations/second virtually all logical decisions can be made in firmware. It was—and still is—the only device of its type: a bipolar microcontroller with both bit *and* byte I/O oriented instruction set.

To find out why the 8X300 Microcontroller is "in a class by itself," write us today. Or contact your nearby Signetics sales office or authorized distributor. *Signetics Corp., 811 E. Arques Ave., P.O. Box 409, Sunnyvale, CA 94086. (408) 739-7700.*

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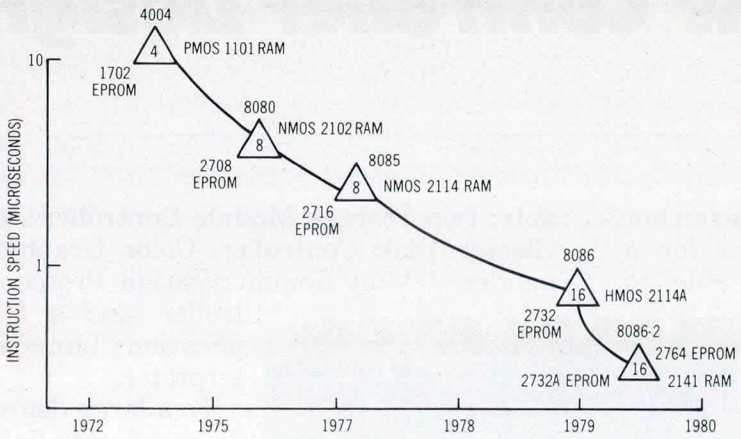
250-ns 64k EPROM Has JEDEC Approved Package



System performance trends. Although more expensive than masked ROMs or P/ROMs, EPROMs are more economical in applications requiring alterations. Nonvolatility enables retention of data for years without being powered, and contents can be erased and reprogrammed. 250-ns access time of 2764 EPROM is compatible with operating speed of recently introduced microcomputers

Industry standards for high density byte-wide memories are met by a 64k-bit erasable programmable read only memory with a worst case access time of 250 ns. A 28-pin configuration of the 2764 EPROM introduced by Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, matches the one recently approved by the JC-42 MOS memory standardization committee of the Joint Electron Device Engineering Council (JEDEC). This format permits 2-line control, which ensures proper system operation at high speed and can be used as a universal pinout for all byte-wide memories, including ROMs, EPROMs, and RAMs.

Because the 28-pin format allows 2k-, 4k-, 8k-, 16k-, and 32k-memories to be interchangeable socket to socket, system designers can work with a single universal memory board layout employing 28-pin sockets. Upgrade to higher density memory devices is possible, and boundaries within the memory map can be altered after the board has been manufactured.

The UV erasable device is completely static (no clocks are required) with 2-line control and low power dissipation. In active mode, it draws 150 mA from a single 5-V supply. When not enabled, the chip automatically goes into standby mode so that current consumption drops to 35 mA and the eight output lines go into a high impedance state.

HMOS-E, the manufacturer's patented process technology, is used for fabrication of the EPROM. Die size of 32,400 mil² (0.2 cm²) is said to be the smallest for 64k EPROMs currently in production.

The chip is programmed by a 50-ms pulse of 21 V; it is erased by UV light applied for 15 to 20 min. Operating range is 0 to 70 °C.

Circle 468 on Inquiry Card

Single-Chip Microcomputer Uses BASIC-Like Language

The INS8073, an 8-bit single-chip microcomputer introduced by National Semiconductor Corp, 2900 Semiconductor Dr, Santa Clara, CA 95051, operates with a high level language similar to BASIC. NSC Tiny BASIC, an enhanced version of the company's industrial BASIC, is an interpretive language that resides in 2.5k bytes of ROM contained within the microcomputer.

In addition to 64 bytes of scratchpad memory in onchip RAM and 2.5k bytes of onchip ROM that stores the NSC Tiny BASIC interpreter, the microcomputer contains an 8-bit arithmetic logic unit, an 8-bit accumulator, an 8-bit extension register, and four internal 16-bit registers. There are 16 address lines and eight data lines. Separate read and write strobe outputs indicate when valid I/O data are present on the 8-bit data bus. The remaining I/O lines are dedicated to initialization, bus management, interrupt request, I/O cycle extension, and software controlled I/O.

Major features of the microcomputer include automatic RAM search following power-on or reset to determine the address range of the external RAM, automatic execution of ROM programs following power-on or reset to execute user NSC Tiny BASIC programs, N-BASIC programs stored in memory as ASCII characters, program protection, execution of RAM-resident programs, and built-in or custom I/O routines.

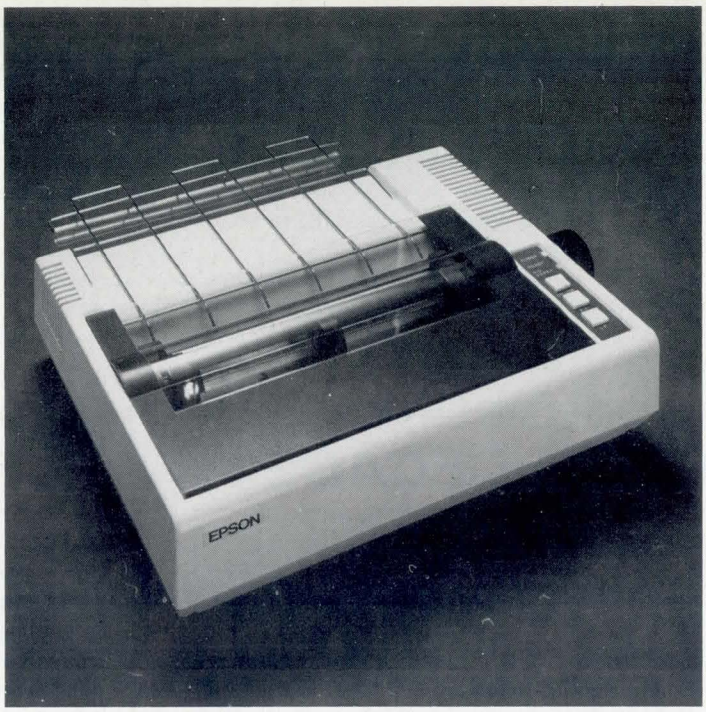
S-100 System Boards Extend Capabilities

Dramatic reduction of central processor overhead is promised through use of the V-100 video controller board introduced by Piiceon Inc, 2350 Bering Dr, San Jose, CA 95112. Fully compatible with the IEEE S-100 bus standard, controller board is I/O mapped so that screen memory does not use up space in the user's system. All interface to the video monitor is handled by writing control information to onboard logic. After initial setup, when input is written to the board, it immediately appears on the screen.

The display consists of 24 lines x 80 characters of data in 7 x 9 dot matrix format. Fonts are available for standard ASCII, or German, French, or Japanese characters. The board also provides 16 user-programmable graphic characters. Data are accepted by the board at a 2M-byte/s rate (or 1 char/500 ns), which allows data to be transferred to the screen at the processor speed, usually about 300k bytes/s.

Circle 469 on Inquiry Card

The MX-80. It not only does everything, it does everything well.



Epson.

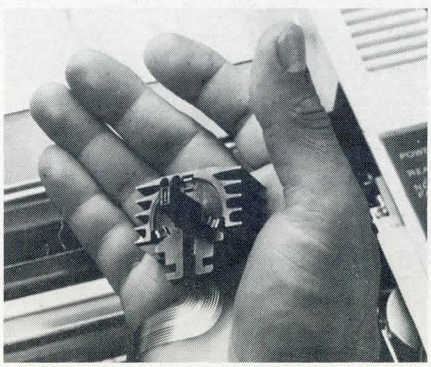
This is the new Epson MX-80 dot matrix printer. It does just about everything you could ask a printer to do. Quickly. Quietly. Reliably. In fact, for OEM installations, the MX-80 may be the single best, all-round printer you can buy. But that's not the best reason to buy it.

The MX-80 prints bidirectionally at 80 CPS in a user-defined choice of 40, 80, 66 or 132 columns. And if that's not fast enough, its logical seeking function minimizes print head travel time. The MX-80 prints 96 ASCII, 64 graphic and eight international characters with a tack-sharp 9x9 matrix. For a long time. Epson printers are known for reliability and the MX-80 is no exception. But that's not the best reason to buy it either.

The print head has a life expectancy of up to 100×10^6 characters, and when it wears out, just throw it away. A new one costs less than $30 and the only tool you need to change it is attached to the end of your arm. The MX-80 is compact, weighs only 12 lbs., and the whole unit, including the two stepper motors controlling carriage and paper feeding functions, is precisely controlled by an internal microprocessor. But even that isn't why you should specify the MX-80.

The best reason is this: because Epson makes more printers than anyone else in the world, we can afford to sell each one for a little less. So you can get one Epson MX-80 Printer for less than $650. And more than one for even less than that.

That's what we call a small price to pay for a printer that does everything well.



The world's first disposable print head. When it wears out, just throw it away. A new one costs less than $30, yet it's so simple, you can change it with one hand.

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CIRCLE 76 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Modules Expand Microcomputer Family

A single-board computer module, a 32k dynamic RAM module, and a general purpose I/O and timer module have been added to the Microflex 65 board family by Rockwell International, Electronic Devices Div, 3310 Miraloma Ave, Anaheim, CA 92083. All three also serve as additional expansion options for the AIM 65 microcomputer line.

The RM65-1000 single-board computer module includes R6502 CPU, 2k bytes of static RAM, 16k bytes of P/ROM-ROM capacity, an R6522 interface adapter, and support circuitry. Selectable memory map compatibility allows programs developed and debugged with the AIM 65 to be easily reconfigured for installation on a standalone microcomputer. Minimum instruction execution time is 2 μs. Bank select and enable switches allow one or two 65k-byte memory bank operation.

RM65-3132, the dynamic RAM module, contains 32k bytes of RAM, arranged into eight independent 4k-byte sections, with selectable starting addresses for each section. All refreshing of the dynamic RAM devices is automatic and transparent to the Microflex 65 bus.

A parallel I/O interface to the bus is provided by the RM65-5222 general purpose I/O and timer module. Two interface adapters supply four 8-bit bidirectional data ports and four 2-bit control ports. This module may be assigned to either or both memory banks.

Circle 470 on Inquiry Card

STD BUS Microprocessor Has 20-Bit Memory Addressing

DM-8800, a 16-bit microprocessor board, features an 8088 CPU; 1k, 2k, or 4k of onboard P/ROM; 5-MHz operation; two interrupt lines; 256 vectorable interrupts; and hardware multiply/divide. A 20-bit full addressing range is achieved by multiplexing the four higher order address bits over the data bus at the beginning of each memory cycle. By using memory boards that can demultiplex this information, 1M bytes of memory can be addressed. When the onboard P/ROM is enabled, 512k bytes of external memory can be used while the upper half of the 20-bit address space is reserved for the P/ROM.

Since all 16 bits are generated during I/O cycles, the processor can address 64k I/O ports. Full 8088 processor status information is presented to the STD BUS so that cycle status is clearly defined. A single 5-V supply with 1 A max is required. Desert Microsystems, Inc, Star Rte 1, Pasco, WA 99301, states that this board is the first of several microprocessor based products that it is introducing; others will include 64k-byte RAM, EPROM, and DMA interface boards.

Circle 471 on Inquiry Card

Cable design has come a long way since data transmission systems were handled only by twisted pairs. Today, many sophisticated EDP systems have evolved making miniaturization and higher speeds prime design objectives. Brand-Rex has been involved in these developments from their beginning.

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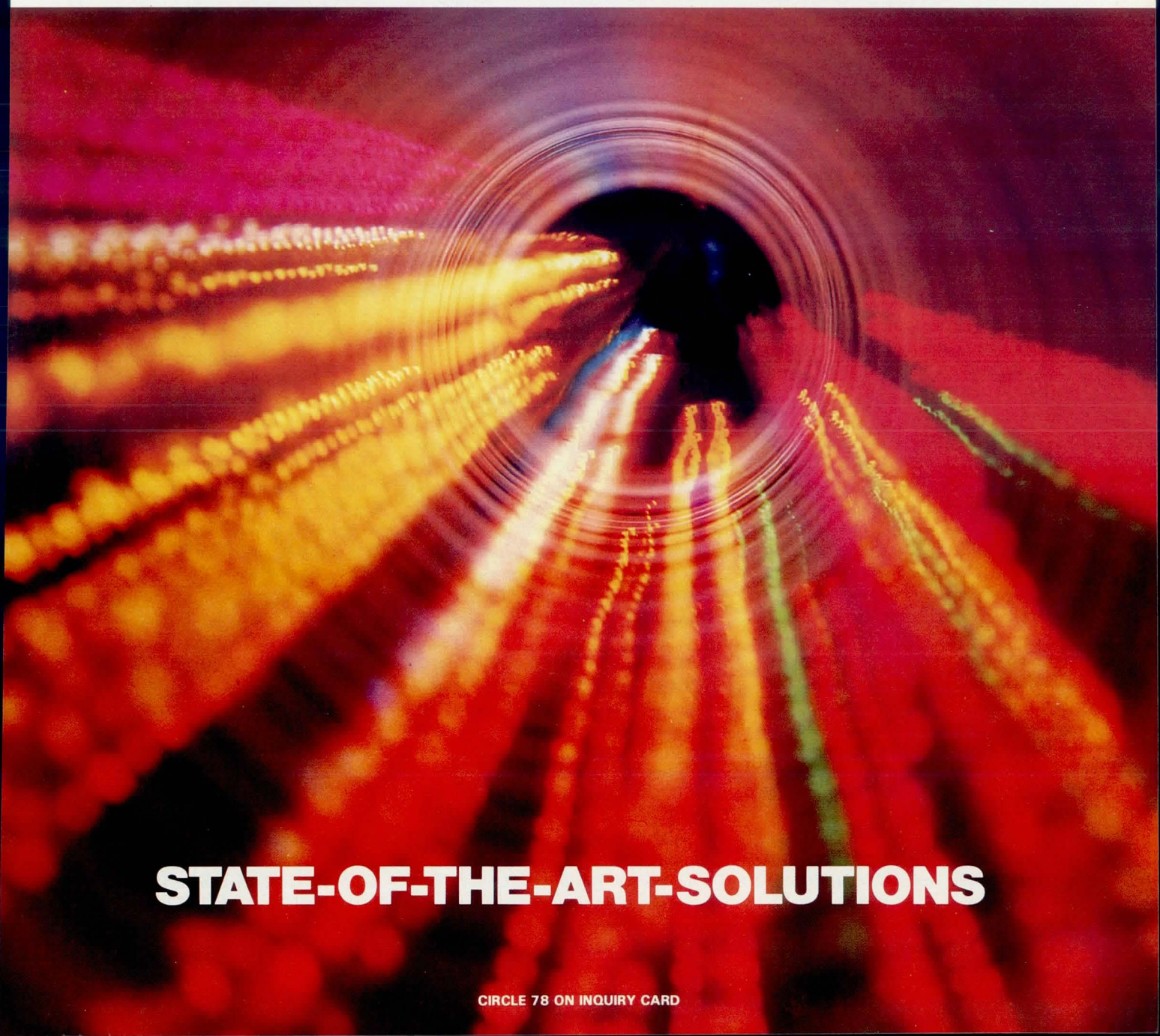

CIRCLE 78 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

STD BUS Card Rack Converts for 19″ Form

As many as 24 STD BUS cards fit into the CR24A card rack, which in turn bolts into an EIA standard 19″ (48-cm) rack; 16 card slots are on 1″ (2.54-cm) centers and 8 are on 0.5″ (1.27-cm) centers. Pro-Log Corp, 2411 Garden Rd, Monterey, CA 93940, has introduced the rack, with improved motherboard to reduce crosstalk and reduce noise between signal lines, as well as a number of STD BUS cards.

The motherboard operates at a free air temperature range of −15 to 125 °C, with a relative humidity range of 0 to 95%. All STD BUS cards are accepted regardless of manufacturer. The rack comes completely assembled, including motherboard assembly and a locking 9-pin power supply cable assembly with mating connector.

Among the cards are the 7308 fully programmable multichannel counter/timer, which provides three 16-bit counter/timer channels with six operating modes each. This card adds a crystal oscillator for accurate programmed timing, a tapped clock divider, an 8-input multiplexer for each channel, and programmable logic states at each clock, gate, and output signal.

The three channels are configured independently by the program. Each is suitable for event counting from dc to 2.5 MHz, marker and square wave generation, time interval measurements, 1-shot simulation with hardware and software triggering and retriggering, and repetitive interrupt generation. This card operates as a standalone peripheral after receiving setup instructions from the system processor card. An onboard interrupt and status polling system identifies completed operations. A special feature allows any channel to interrupt after the Nth programmed event of loop iteration.

Another card is the 7703, containing up to 16 bytes of high speed (350 ns) nonvolatile CMOS RAM. An onboard memory protect circuit monitors the 5-Vdc power and automatically generates a memory save signal prior to switching to lithium battery backup. Data will be retained for a guaranteed minimum of two years.

Write protect switches (4k blocks) are provided for preservation of critical data and for nonvolatile program execution. The card decodes all 16 address lines, and onboard jumpers permit mapping in any consecutive 4k, 8k, or 16k address blocks. A lithium battery included has a shelf life of 10 years. A low battery status signal is provided via an LED indicator. No battery charging time is required.

7701 NMOS and CMOS RAM cards have sockets for up to 16k bytes of P/ROM or read/write memory. Each card has sockets for up to 16 pairs of 2114 and 6514 type or equivalent RAMs. Alternately, each card will accept pin compatible P/ROMs or equivalent. (RAMs and P/ROMs cannot be used on the same card.)

The cards decode 16 address lines and can be mapped into either 8k or 16k bytes of consecutive address space. An onboard jumper system allows users to select card address for a 64k microprocessor.

Circle 472 on Inquiry Card

Single-Board Microcomputer Is Multibus Compatible

A faster CPU, a system timing controller, and a bus vectored interrupt capability have been added to the existing features of 8-bit MonoBoard™ computers to form the Am95/4006 member of the Supercomponent™ family. Standard CPU is a 2-MHz Am9080A with 2-μs instruction cycle, although a 4-MHz version with 1-μs instruction cycle can be specified.

Features of the microcomputer board from Advanced Micro Computers, 3340 Scott Blvd, Santa Clara, CA 95051, include 4k bytes of static RAM; sockets for 16k bytes of EPROM/ROM, Am9511A or Am9512 arithmetic processing units, and I/O line drivers and terminals; 48 programmable I/O lines; RS-232-C serial interface; MultiMaster bus control; 8-level vectored priority interrupt controller; and programmable realtime clock.

The system timing controller provides five completely independent, general purpose, 16-bit counters with five hardware and five software gating inputs that can be used in any combination with any counter. An onchip oscillator and frequency scaler is used for baud rate generation. Counters can be concatenated internally and counters 1 and 2 include a time of day mode with alarm registers.

Bus vectored interrupt capability adds to the power of the onboard interrupt controller and allows recognition of and response to an interrupt vector placed on the system bus by another board in the system. An address decoder P/ROM maps the logical address to memory location and matches EPROM/ROM type to specific sockets. The Am95/4006 allows this memory map to be program switched between two configurations. After the system is operational, this P/ROM can shadow out the bootstrap program and make that address space available to RAM.

Circle 473 on Inquiry Card

Z80 CPU Board

Maximum user flexibility and capability for a wide range of options is offered by the CB2™ Z80 based CPU board. It operates at 2 or 4 MHz by DIP switch selection and includes sockets for two 2716 or 2732 EPROMs or HM6116 2k RAMs. If desired, the memory sockets can be enabled or disabled. Separate run/stop and single/step switches on the board permit system evaluation without the need for a front panel.

Available from SSM Microcomputer Products, 2910 Paragon Dr, San Jose, CA 95131, the board features firmware vector jump and an output port to control eight extended address lines that permit the use of more than 64k of additional memory with the CPU board. Jumper options on the board generate S-100 signals.

User selectable options through onboard switches and wirewrap jumpers include a CPU clock dynamic speed change and one wait state if needed. The board will emulate 8080 I/O addressing and is provided with an 8-bit output port that can be used as extended addressing with a simple header connection.

Onboard EPROMs have a capacity of 2k or 4k x 8 bits; onboard RAM has a capacity of 2k x 8 bits. The board requires 8 V at 0.75 A typ (less EPROMs).

Circle 474 on Inquiry Card

8086 Strike Force

Intel announces the M8086, the most powerful 16-bit military microprocessor available today.

Intel's new M8086 now gives designers the architectural base to launch an attack on previously inaccessible military applications. Offering up to an order of magnitude higher performance than previous devices, the M8086 is the most powerful 16-bit military microprocessor available today.

But just as importantly, Intel also offers the M8086-compatible support components and development tools you need to build complex VLSI systems for military applications. Components such as those shown in the table. Plus the industry's most complete array of hardware/software support tools. That's the *system* solution you need to deliver your military products—hitting time, budget and performance targets precisely. That's the 8086 Strike Force.

Proving once again that Intel puts military equipment manufacturers in command of the latest advances in VLSI technology. From our JAN-approved 8080A, through the M8085 and M8048, to the new M8086: Intel is committed to delivering military solutions.

The new military standard

The M8086 sets a new standard for military microcomputer applications. With super-efficient architecture for implementing high-level block-structured languages. A full megabyte of addressable memory space. A powerful new instruction set, including hardware Multiply and Divide. Plus flexible system configurability through the Multibus™ interface. All of which makes it possible to use the M8086 in applications that used to require multiple-chip CPUs, such as bit-slice designs and minicomputers. And because Intel designs M8086 systems for future expansion, you'll be able to take advantage of further enhancements—such as co-processors and IO processors—as military versions become available.

The HMOS*-process M8086 and support components are ready today to be drafted into your hi-rel military systems. All components conform to Class B standards of MIL-STD-883B, Method 5004, while meeting all military inspection criteria and lot conformance testing requirements of Method 5005. Futhermore, the M8086 family has been selected for military standardization under the MIL-M-38510 program (JAN slash sheet M38510/530).

The M8086 Family (Class B, MIL-STD-883B T_A: −55° to 125°C)	
Microprocessor/Support Components	
M8086	Microprocessor
M8282/3	Octal Latches
M8284	Clock Generator and Driver
M8286/7	Octal Transceivers
M8288	Bus Controller
Standard Memories	
M2114A	4K Static RAM (1K x 4)
M2148H	4K Static RAM (1K x 4
M2147H	4K Static RAM (4K x 1)
M2118	16K Dynamic RAM (16K x 1) T_A: −55° to 85°C
M2716	16K EPROM (2K x 8)
M2732	32K EPROM (4K x 8)
M3636	16K Bipolar PROM (2K x 8)
Peripherals	
M8251A	USART
M8253	Counter/Timer
M8255A	Programmable Peripheral Interface
M8259A	Interrupt Controller

Getting your products off the ground

You can begin designing your next generation of 16-bit military microcomputer systems today, using Intel's total hardware/software support tools. Hardware support such as the Intellec® Series III Microcomputer Development System, with ICE-86™ in-circuit emulation. And software tools like the RMX/86™ real-time multitasking executive, PASCAL-86, FORTRAN-86 and PL/M-86 compilers, ASM-86 assembler, and a full range of utility and M8080A/M8085A conversion software.

To stay at the forefront of VLSI technology, and capture larger segments of military business, specify the M8086 family for your next design. It's the only *complete* 16-bit military microcomputer system available today. To find out more about the M8086 and Intel's full line of military products, contact your local Intel sales office/distributor, and ask for our *Military Products Catalog*. Or write Intel Corporation, 3065 Bowers Avenue, Santa Clara, CA 95051. (408) 987-8080.

*HMOS is a patented Intel process.

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CIRCLE 79 ON INQUIRY CARD

Prototyping Card

An S-100 wirewrap prototyping card that meets IEEE-696 bus standard, compliance H, provides designers with nearly twice the area previously available. It will accommodate more than 100 16-pin or other sockets on 0.3″ (7.6-mm) or 0.6″ (15.2-mm) centers.

The 9″ (23-cm) deep board has been introduced by Inner Access Corp, PO Box 888, Belmont, CA 94002, complete with onboard regulators that provide 5 V at 3 A and ±12 V at 1 A. Twenty-six 0.1 μF decoupling capacitors are distributed at either end of the board. Silk screened letters indicate rows (A-M) and columns (0-8). The double-sided, plated-through board is tin-plated except for gold over nickel connector fingers.

Circle 475 on Inquiry Card

CPU and I/O Boards

Two S-100 compatible products—a Z80A based multifunction processor board and a serial I/O board—have been announced by Measurement Systems & Controls, 867 N Main St, Orange, CA 92668. Both multi-user boards are part of the "2nd Generation" series.

Eight vectored priority interrupts on the CPD-280 processor board allow the CPU to maximize its execution time by eliminating the need for polling. A realtime clock generates interrupts required by the available multi-user operating systems. Two serial and two parallel ports are optimized for high speed data transfer by utilizing DMA. In addition, hardware interfaces are customized through use of external personality boards.

The INO-288 I/O board is intended for use in expanded S-100 systems requiring either four or eight additional serial I/O ports to support terminal and/or printers. All ports are fully programmable, using the 8251A programmable communication interface. Each port supports RS-232-C with full handshaking. I/O ports can operate either asynchronously or synchronously with 16 selectable baud rates. Selection is made through software of DIP switches.

Interrupt features offered by the two universal interrupt controllers include fixed or rotating priority and 16 individually maskable interrupt inputs. Jumper options select one of the nine S-100 bus signals to be driven by the interrupt output. Up to four programmed bytes are supplied in response to each interrupt. When used with the CPD-280 processor, the interrupts can be daisy chained with the interrupt structure on that board.

Circle 476 on Inquiry Card

Preview our new double feature.

Now that our 9″ and 12″ CRT monitors have become big box office hits, we're ready to show you two new performers: a 15″ model for fans of the big screen, plus a 5″ model in the compact category.

As with all C. Itoh CRT monitors, you'll be impressed by the superior bandwidths and resolutions of our models. For example, our 5″ features 15 MHz and a 600 line resolution while our 15″ offers 30 MHz and 1200 lines on a large 239 mm x 171 mm display area.

Our popular medium-sized 9″ and 12″ screens offer a horizontal rate of 15.72 KHz. All screens feature separate horizontal drive, vertical drive and video inputs which eliminate composite sync and video signal processing. The simple output circuitry and integrated PC board construction contribute to the high reliability of our monitors.

Our screens are available in kit or chassis version, equipped with standard P4 phosphor or optional P31 and P39 phosphors. The heavy duty zinc chromate plated chassis can be furnished with a power supply.

Make your reservations for a private screening today and get ready to judge our performance for best picture of the 80's. Contact your nearest C. Itoh representative or C. Itoh Electronics, Inc., 5301 Beethoven Street, Los Angeles, CA 90066; Tel. (213) 390-7778; or 666 Third Avenue, New York, NY 10017; Tel. (212) 682-0420.

C. Itoh Electronics, Inc.

CIRCLE 81 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

Single Quad Board Serves as NRZ Tape Controller

A universal magnetic tape controller that provides 9-track NRZ format on a single quad board, the TC-151 can mix up to eight NRZ, PE, and dual-density tape units in any combination by adding a dual-width board. A 33-word buffer provides flexibility in assigning priorities to the computer. Read/write on the fly allows automatic nonstop operation without special software when doing consecutive read/write operations.

The controller, introduced by Western Peripherals, 14321 Myford Rd, Tustin, CA 92680, is software compatible with all DEC LSI-11 series computers. The PC board plugs into the computer and connects with the tape drive through the rear of the computer. All tape drives designed to be compatible with industry standard interface can be used.

Circle 477 on Inquiry Card

Replacement Disc System Increases Memory Capacity

A plug compatible Winchester disc drive, the 11L emulates 3.75 RL01 discs in an LSI-11 microcomputer. Its interface is completely transparent to the RL01 I/O drivers and operating system, and it appears to the LSI-11 bus as an RLV11 controller with 3.75 RL01 drives attached. A 10M-byte version serves as a plug compatible replacement for two RL01 drives. Rack mounting or tabletop configurations are available. A total of four drives can be operated from one Z80 controller, providing total capacity of either 80M or 40M bytes of formatted data.

Backup for these discs from Corvus Systems, Inc, 2029 O'Toole Ave, San Jose, CA 95131, is provided by a 120M-byte "Mirror" cassette system. In addition, a Constellation backend network option allows the disc to be shared by up to eight microcomputers.

Circle 478 on Inquiry Card

Parallel I/O Board is LSI-11 Compatible

Completely hardware and software compatible with LSI-11 and PDP-11/03 microcomputers, the PIO L11 parallel interface requires one dual-width option slot in the computer cabinet. Standard interrupt vector and address selections are provided. A 10-position DIP switch is used for address selection and a 5-position device is used for choice of vector address. The board is transparent to the host computer's diagnostics, drivers, and operating systems.

Introduced by Computer Extension Systems, Inc, 17511 El Camino Real, Houston, TX 77058, the interface permits program controlled transfers at rates of up to 40k words/s. It has 16 diode clamped inputs and 16 latched output lines.

Circle 479 on Inquiry Card

Development System Supports Bit Slice Processors

Modular design of the EZ-PRO universal development system for bit slice or fixed word length processor support allows OEMs to configure each system to meet exact application requirements. All TTL and bit slice products are supported. Microprogram word lengths to 128 bits and depths to 2k words can be accommodated normally or up to 8k words can be handled with a shorter microprogram word. Memory cycle times are better than 60 ns.

The basic system has 32k bytes of static memory which can be expanded to 80k by adding modules. Up to 64k bytes of memory can be used for user programs. Systems are available from American Automation, 14731 Franklin Ave, Tustin, CA 92680, with in-circuit emulators for the 2650, 6502, 6800, 6802, 6808, 6809, 8080, 8085A/A-2, Z80, and four members of the 3870 family.

Circle 480 on Inquiry Card

Computer Sciences Corporation

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MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

SOFTWARE

Pascal Compiler Extends Microcomputer Development

Specific extensions based upon the ISO draft standard qualify Pascal for microcomputer development by including chip level I/O, interrupt handling, and linkage to assembly language. The language compiles directly into 8080/8085 machine code rather than to P-code as do Pascal P-code interpreters. The result is faster and often more compact code. The first offering from Tektronix, Inc, PO Box 1700, Beaverton, OR 97075, supports Intel 8080 and 8085 microprocessors. Except for interrupt and I/O routines, source code developed for the 8080 and 8085 will compile to object code for the Intel 8086, Zilog Z8000, and Motorola 68000 as the compilers become available.

The compiler allows an ORIGIN attribute to be associated with variables and has predefined functions and procedures that allow data to be input and output through the microprocessor's I/O ports. All I/O capability is available to a Pascal program running in emulation mode 0. Pascal can access the terminal, disc, line printer, and remote I/O ports. This allows the operating language to be used as a general purpose computer when it is not needed for development work.

Unlike standard Pascal, which has no interrupt handling capabilities, with the extension interrupt service routines are written as Pascal procedures and connected to the specific processor's interrupt vectors with convenience routines that are included with the compiler. If the user wishes to switch from one supported chip to another, he need only modify his routines which connect the interrupt vectors to the interrupt service routines.

To provide assembly code for applications that have time critical program segments, the compiler has been made compatible with the TEKDOS (Tektronics operating language) linker, enabling Pascal generated code to be linked to assembly code. The code written in assembler could include libraries of existing code.

Multi-User Oriented Database Management

A complete database management system as well as a sophisticated program development system, ANDI™ generates complete file maintenance and interactive select-sort-display programs using only the database description and a CRT data entry mask. Its complete CRT formatting subsystem allows operators to use word processing type editing functions such as delete word, insert characters, etc. Operator I/O is handled by entry masks that can be built with two different interactive mask editing programs, one for inexperienced users, the other towards more sophisticated operators. All CRT control functions are user definable.

Dravac Ltd, 150 Fifth Ave, Suite 530, New York, NY 10011, has released the software system for use on the Alpha Microsystems AM-100 series of computers. It is fully multi-user oriented, and offers record exclusive use which locks at the record level rather than at the sector level, as in less sophisticated systems. A key access system, based on a B+ Tree algorithm, provides fast access to the keys in large or small key files using a minimum of program memory. Symbolic keys can be accessed randomly or sequentially from the last fetched key. Any number of key files may be defined for use with a file.

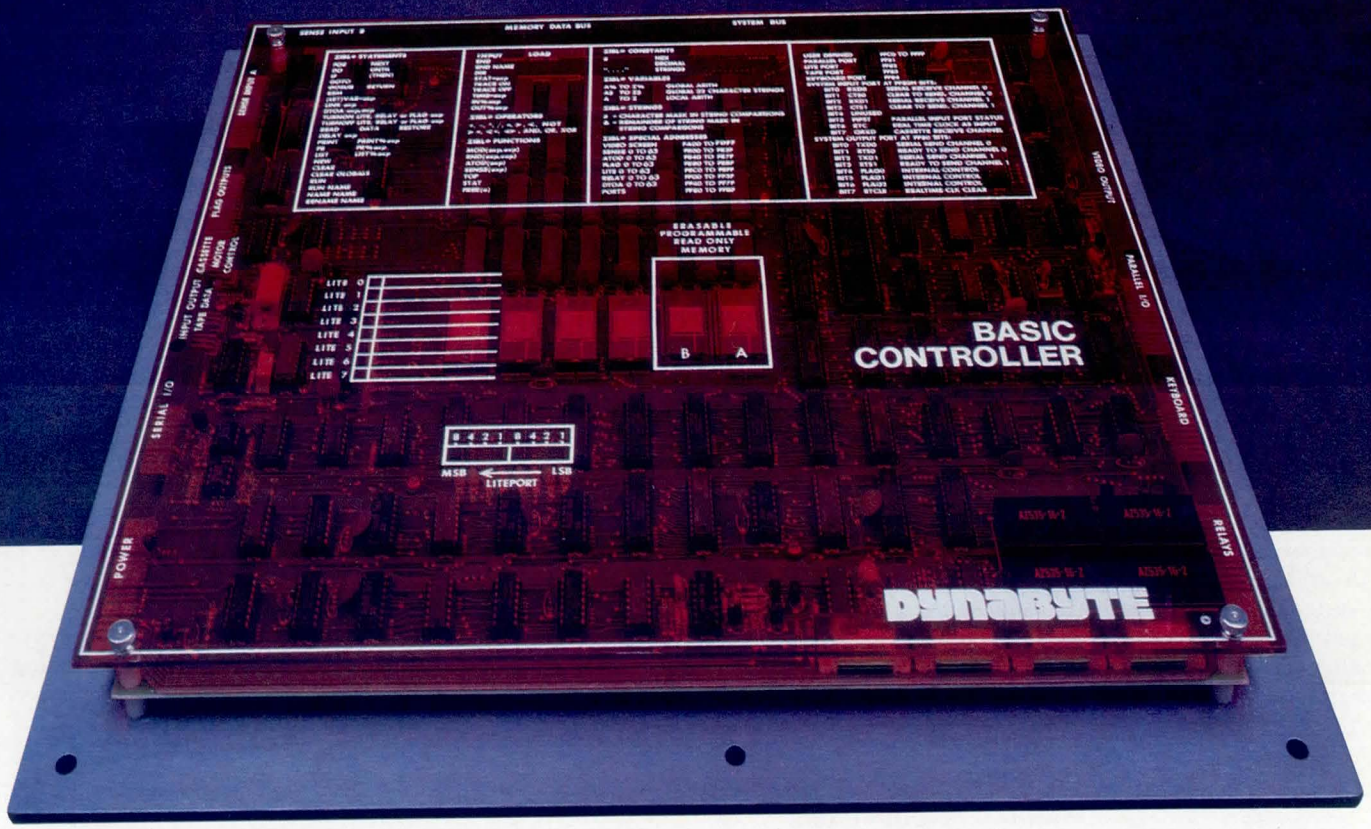
Circle 481 on Inquiry Card

FORTRAN Support Library Enhanced for LSI-11 Series

Like the original, an enhanced version of the DTLIB SP101 software support package for the company's family of LSI-11, LSI-11/2, and LSI-11/23 compatible analog I/O, digital I/O, and control peripherals, is a subroutine library designed to operate under the DEC

(continued on page 156)

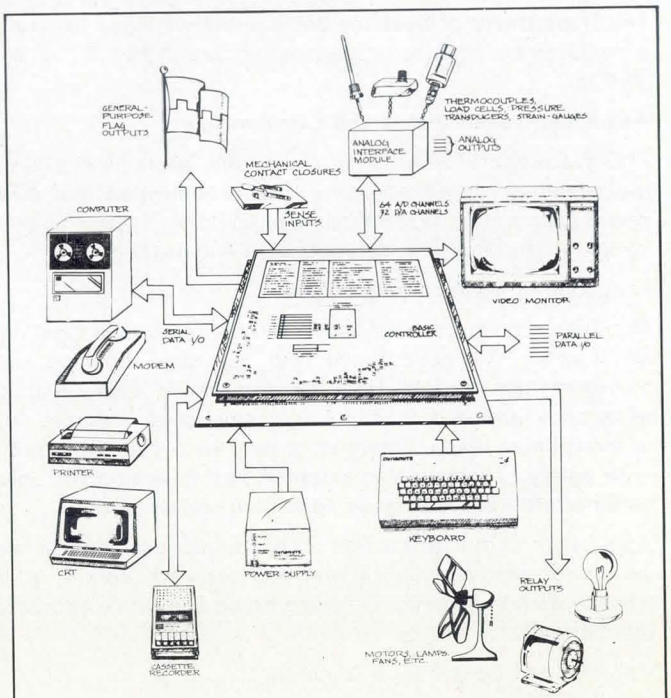
The Single-board Computer System for the Man Who Doesn't Have Time to Build His Own*



***Or can't afford to**

So-called "single-board" computers are a long way from being single-board computer ***systems***. Analyze what it really takes to make one: CPU board, memory boards, I/O boards, rack-mount, software development system, and weeks (sometimes months) of construction, programming, and debugging.

Now consider the BASIC CONTROLLER™: one board. Period. CPU, RAM, EPROM sockets, video generator, keyboard and cassette interfaces, 24 hour clock, serial and parallel ports, a multitude of "real-world" I/O's — even an EPROM programmer — are all included. And our built-in ZIBL™ (Z80 Industrial BASIC language) interpreter will reduce your programming time to hours, instead of weeks. So you can concentrate on your application, not hardware and software. If your needs are less than 200 ***systems*** per year, you really can't afford to use anything but a BASIC CONTROLLER™.



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CIRCLE 84 ON INQUIRY CARD

MICRO DATA STACK
COMPUTERS, ELEMENTS, AND SYSTEMS

SOFTWARE

RT-11 realtime operating system and to be linked to user FORTRAN IV programs. Data Translation, 4 Strathmore Rd, Natick, MA 01760, states that the enhanced SP101.V2 library provides a total of 20 subroutines, rather than the original seven. Added functions include bilateral conversions between binary and BCD numbers and display function that offers the choice of either one time or continuous display of realtime X-Y outputs for an oscilloscope or a hardcopy plotter.

Instead of the single 16-channel analog input system supported by the original package, the V2 version supports up to 256 channels of analog inputs or four analog I/O systems in any combination. It supports four programmable realtime clocks rather than just one; up to eight analog output boards containing up to 32 D-A converter channels, instead of a single output board with a maximum of four D-A channels; and 128 digital I/O points, rather than 16. It also supports DMA, which the equivalent package does not, providing standalone capabilities for two analog output channels and up to four 16-channel analog input systems under DMA.

Circle 482 on Inquiry Card

Operating System Combines Previously Separate Functions

UniFLEX™, an operating system for 6809 or 68000 based microcomputers, retains both the flexibility of FLEX™ and accepted structures of Bell Laboratories' UNIX. Each user on the multitasking operating system communicates with the system through a terminal and may execute any of the available system programs. Thus one user may be running the text editor while another is running BASIC and still another is running the C compiler. In addition, one user may run several programs at a time.

A very complete operating system with no practical limitations built into the software, except those that are hardware imposed, it supports a hierarchical file system allowing file sizes up to 1 G bytes and disc capacities of over 8 G bytes. All files are fully protected. A user may read, write, or execute protect files on an individual basis. All system I/O is device independent since I/O devices and files are treated in an identical fashion. Any combination of interrupt driven devices may be attached to the system. Any running task may initiate another task in an asynchronous manner. Intertask communication is also supported. Task swapping may take place on those systems incorporating an appropriate swapping device. In realtime applications, where swapping may be detrimental, it is possible to lock a task in main memory. This operating system has been announced by Technical Systems Consultants, Inc, 1208 Kent Ave, W Lafayette, IN 47906.

Circle 483 on Inquiry Card

IEEE Format Floating Point Library for OEM Microprocessor Systems

A software package that enables systems engineers to integrate floating point operations into products based on 8080/8085 or Z80 microprocessors, the FPAC™ floating point library conforms fully to proposed IEEE standards for single precision floating point representations, and to all error handling conventions. It is available in source assembly language form for inclusion into OEM floating point system applications.

The library, from Cognitronics Corp, 5470 NW Innisbrook Pl, Portland, OR 97229, provides immediate access to basic arithmetic operations (add, subtract, multiply, divide); trigonometric functions (sine, cosine, tangent, arc tangent); exponentiation; logarithmic functions (logarithm, natural logarithm); square root; data conversion procedures (ASCII string to/from floating point representation, word integer to/from floating point representation); and floating point utility procedures. It can be used in virtually any development system environment, and can be customized by its users to fit particular application requirements. A user's guide fully documents operation, including numerical representations, individual module sizes, module execution times in CPU cycles, and error handling conventions.

Circle 484 on Inquiry Card □

DIGI-DATA SERIES 40

the more OEMs demand of tape systems, the more we deliver.

OEMs are demanding. They want different models for different applications, the highest possible reliability, and value that reflects in their final product. Our Series 40 continues the 17 year Digi-Data tradition of satisfying these OEM requirements.

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Within our Series 40 family, they can choose from 192 combinations of NRZI, PE and NRZI/PE models with reel sizes from 7 to 10.5 inches and speeds from 12.5 to 75 ips — all featuring a new control block with more functions, such as a density select switch and an optional unit select switch.

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CIRCLE 86 ON INQUIRY CARD

ATTAINING MICROPROCESSOR INTERFACE COMPATIBILITY WITH DAC AND ADC DEVICES

Doug Grant Analog Devices
Rte 1 Industrial Park, Norwood, MA 02062

The designer who selects a data converter based on its alleged microprocessor compatibility often discovers that it will not fit the bus and control architecture which he has chosen. To ensure compatibility, the microprocessor control signals and their relationship to the data converter logic must be considered. When a microprocessor communicates with a peripheral device, three events must occur. First, the processor must tell the system which device it wants to talk to. This is usually accomplished by sending the address of the desired device (generally 16 bits) out on the system address bus where local decoding logic provides a signal at the addressed unit. Once the desired location has been alerted, and others deactivated, another signal must be provided by the processor to tell the device whether to supply or accept data. Finally, the data must be supplied.

Microprocessors provide these signals in a variety of ways, which is a problem for converter manufacturers. While it would be a simple task to build a digital to analog converter (DAC) with the onchip bus interface optimized for, say, the 8085 microprocessor, using this DAC in conjunction with other microprocessors generally ends up adding more gates than were saved by using a "microprocessor compatible" converter. Adding enough onchip logic to a converter to accommodate several processor types adds package pins, and as many pins may end up being used for control signals as for the basic function. In any specific application, this can result in as many as six to eight unused pins on a 40-pin dual-inline package—a waste of packing density, board space, and money.

Another option for the converter manufacturer is to design one integrated circuit with all interface logic available onchip, and then offer versions with subsets of the control signals brought out to a smaller set of package pins. Or, to go one step further, the manufacturer could provide a mask option to produce separate chips for each interface type. Both of these approaches, however, would create production nightmares. Also, a change in timing specifications initiated by one microprocessor manufacturer could render the chip obsolete.

A more effective solution to the converter interface problem is achieved by the time-honored engineering practice of compromise—eg, decide which portion of the interface is most universally required, then implement that portion on the chip. More specific elements are then left open to the user, who can best select the logic to suit his particular system.

Consider the logic necessary for a memory mapped interface to a peripheral chip. Address decoding, a system variable function, is the first requirement. Small systems may directly use an address line, which locates the device in a large block of memory locations. Larger systems can decode one specific address out of the 65k available on all 16 address lines. Therefore, adding address decode logic on the chip is likely to create more problems than it would solve. A single active-low chip select ($\overline{CS}$) input is usually adequate, or at most one active-high and one active-low $\overline{CS}$. Of course, when more than one byte of data is needed, as in the case of a 12-bit DAC, or in an analog to

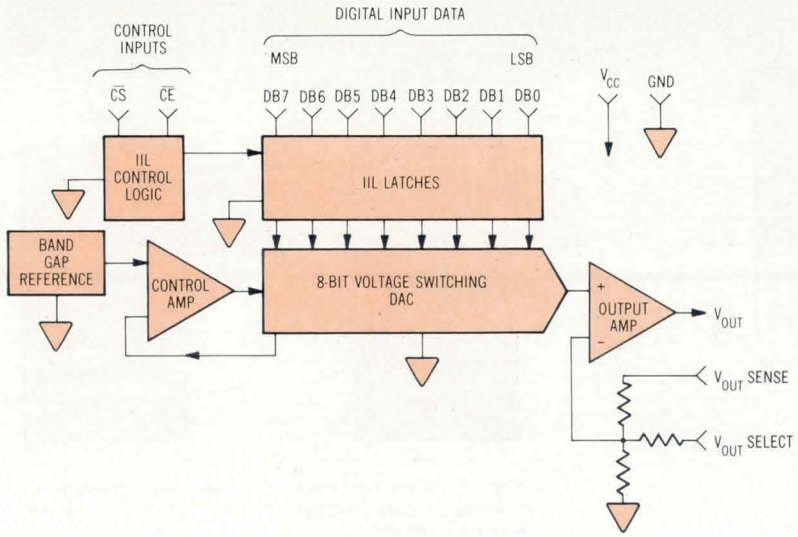


Fig 1 AD558 DACPORT block diagram. Level triggered latch will cause analog output change with any data input during enable period. Implemented in IIL, latch will operate in 100 ns

digital converter (ADC), more addressing capability is required.

DAC-Microprocessor Interfacing

A typical converter-microprocessor connection is exemplified in the simple case of a microprocessor which generates an analog output using an 8-bit DAC. The coincident occurrence of two signals is required to tell a latch to grab the data on the bus and pass them to the DAC. Once an address has been assigned to the DAC, decoding circuitry produces a low-going signal when the address is present, and a system $\overline{WR}$ ($\overline{I/O}$ $\overline{W}$ or $\overline{MEMW}$) produces a low-going signal when data flow out of the processor. The logic to be implemented onchip, a 2-input NOR gate and an octal latch, is relatively simple.

The AD558 DACPORT shown in Fig 1 is implemented in integrated injection logic (IIL), which provides high speed, low power, and compatibility with the standard linear bipolar process. Control signals and data inputs are transistor-transistor logic (TTL) or 5-V complementary metal oxide semiconductor (CMOS) compatible, and timing is suitable for interface to most processors. The latch is level triggered; any activity on the data inputs during the enable period will cause the analog output to change. This allows the user of a single-chip microcomputer to tie the enable inputs low and sit the DAC directly on one of the latched ports already available. While several DACs, including onchip latches, are available, many of the latches are too slow to keep up with faster processors. Many also require bus data to remain stable for some time after strobing the latch, a condition which complicates the interface to 6800 type machines. The latch shown in Fig 1, however, operates in 100 ns, and has no data hold time requirement. In that it requires no negative power supply, the DACPORT is distinct from other "microprocessor compatible" DACs. It offers buffered analog output voltage ranges of 0 to 2.56 V and 0 to 10.0 V, pin selectable. The 2.56 V range is available when operating on a 4.5 V or higher power supply; the 10.0 V range can be used if the power supply is 11.4 V or higher.

The bus interface latch is straightforward; the active-low decoded address is applied to $\overline{CS}$ and the system $\overline{WR}$ connects to chip enable ($\overline{CE}$). This connection will work in any system in which a valid address bus and a valid $\overline{WR}$ indicate valid data. When both $\overline{CS}$ and $\overline{WR}$ are low, data enter the latch; when either returns high, data are held (see Fig 2). In systems where data are valid only on clock edges, a simple one-shot will provide a usable control signal.

ADC-Microprocessor Interface Examples

The AD574 12-bit converter is an example of an analog to digital device. Built with standard bipolar processing, it uses IIL to implement the control and successive approximation register (SAR) functions. Microprocessor handshake capability is included in the 28-pin double-width package; an improvement over the usual 32-pin, triple-width package used for 12-bit ADCs. The device can accommodate analog

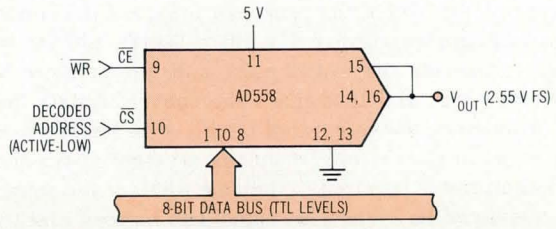


Fig 2 General interface connections for DAC. Data enter latch when $\overline{CS}$ and $\overline{WR}$ are low. Data are held when either $\overline{CS}$ or $\overline{WR}$ returns high

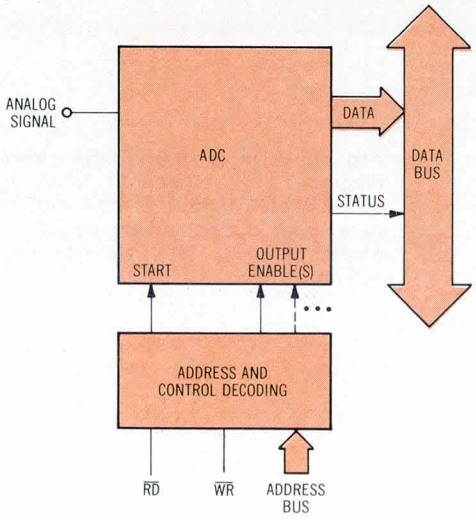


Fig 3 ADC handshaking. STATUS output indicates completion of conversion cycle. STATUS signal can be tested by microprocessor or used as interrupt with slow converters

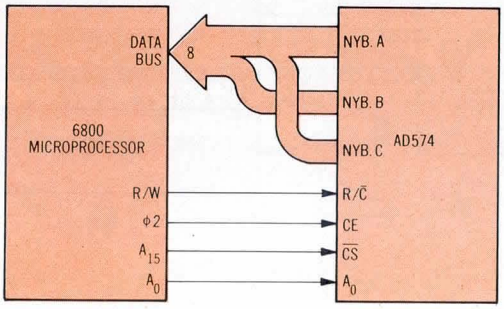


Fig 4 Converter-microprocessor interface. Converter can interface to 16-, 12-, or 8-bit wide bus. In 12-bit mode, all 12 outputs can be simultaneously enabled. In 8-bit mode, READ operation while A_0 is low enables eight MSBs. Reading with A_0-high places four LSBs on bus, followed by four trailing 0s

input ranges of 0 to 10 or 20 V and ±5 or ±10 V, with full-scale accuracy determined by an onboard 10 V reference.

A problem arises when 12 bits of data must be loaded into an 8-bit wide bus. Specifically, the data must be placed in two locations and accessed one piece at a time. Two possible formats can be used: left-justified, where the data indicate a fraction of the full-scale range, and right-justified, where the data represent an integral number of least significant bits (LSBs). The left-justified format also permits "coarse reads" of data in systems where an 8-bit word may momentarily provide sufficient resolution. Arithmetic is not hindered by left-justified data as long as the programmer recognizes that the data represent a binary fraction.

Interfacing an ADC to a microprocessor requires a slightly different control sequence than interfacing a DAC to a microprocessor. First, the processor must tell the converter when to begin converting. Usually a WRITE address is decoded to provide the START pulse and one or more READ operations are needed to place the converted data on the bus. Also, since few integrated circuit ADCs (certainly none over eight bits) can convert during a single instruction, a STATUS output is required to indicate whether the converter has completed its cycle. This signal can be read and tested by the microprocessor or used as an interrupt in the case of a very slow converter (millisecond or longer conversion times). Alternately, the program can execute sufficient dummy instructions to timeout the converter's maximum conversion time. Fig 3 shows such a handshaking arrangement.

The AD574 can interface to a 16-, 12-, or 8-bit wide bus. In the 12-bit mode, all 12 data outputs can be enabled simultaneously. The control signals are organized such that direct connection to 6800 and 6502 buses is possible. Addition of a few external gates permits interface to other processor types. The converter may also be used in a stand-alone mode, offering performance equal to many hybrid designs at the price of an integrated circuit (IC).

In 6800 type systems, the read/write (R/W) signal is applied directly to the read/convert (R/$\overline{C}$) input. CE and $\overline{CS}$ inputs allow use with a wide variety of decoding schemes for the higher order address bits. Usually a partially decoded address is applied to $\overline{CS}$ and $\phi 2$ is applied to CE. A WRITE operation ($\overline{CS}$-low, CE-high, R/$\overline{C}$-low) initiates either a full 12-bit conversion (if A_0 is low) or a short-cycled 8-bit conversion (if A_0 is high). When the 35-μs conversion time has passed, or if the status (STS) line has been polled, the data can be read. A READ to the even address (A_0-low) enables the eight most significant data bits (MSBs). Reading the odd address (A_0-high) enables the four LSBs and forces the four trailing bits to logic zero. Fig 4 shows the bit overlapping for 8-bit bus interface.

Perhaps the ideal situation for a microprocessor compatible ADC is one in which no handshaking is required. The AD7581 is a CMOS device which includes an 8-channel, 8-bit continuous-cycling ADC and 8 bytes of random access memory (RAM), both controlled by a built-in direct memory access controller. The processor thus sees only eight

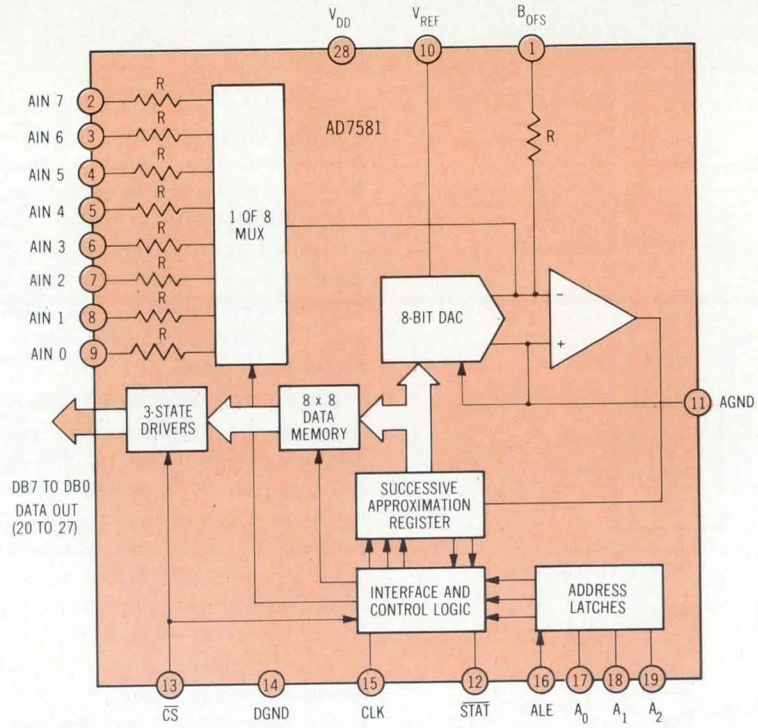


Fig 5 AD7581 functional diagram with conversion, handshaking, and storage integrated on one chip. Conversion is independent of CPU operation

memory locations with up-to-date results from each of the eight internal ADC channels. The block diagram of the device (Fig 5) shows the high level of digital and analog integration on the chip.

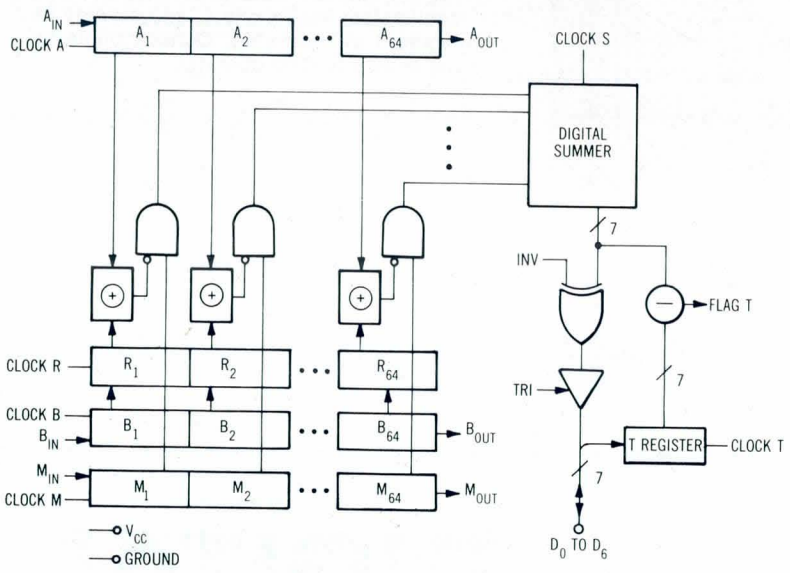
Of the successive approximation type, the ADC completes a scan of all eight channels in 500 μs. As a channel is converted, the 8-bit result is deposited in the onchip RAM. Internal logic prevents the update from occurring during memory READ cycles. A single clock signal, which can be the system clock in 6800 or 6502 type processors, is required; address latch enable (ALE), while not necessarily symmetrical, can be used in 8085 type systems. In systems such as the 8085, which use a single bus to carry data and the least significant address bits, the onboard address latch can be used and is driven by ALE. If the address latch is not needed, ALE can be tied high, thus rendered transparent. Access time of the CMOS RAM is 250 ns. Total device power requirement is 40 mW for a 5-V supply.

Conversion is totally independent of central processing unit operations. It is continuous, with a status line providing a short negative-going pulse to signify a channel update. This pulse is extended when the last channel is converted, so that systems can detect when an 8-channel scan is completed.

Summary

Microprocessor compatibility with conversion devices is presently obtained by three methods. In the first, no interface is added, and the user is required to custom-build his own. The compromise method allows some user flexibility, but vital functions are onchip. With the processor transparent method, conversion, handshaking, and storage are all integrated on a single chip.

Single-Chip Digital Correlator Compares Stored 64-Bit Reference Word



TRW LSI Products TDC1023J digital output correlator. Four 64-bit independently clocked shift registers, labeled A, R, B, and C, are onchip. Incoming data are clocked into A register. Correlation takes place between A and R registers

A single-chip correlator that replaces 40 to 50 SSI/MSI devices compares a stored 64-bit reference word with an incoming 64-bit serial word at a rate of 20 MHz. The total number of bit for bit agreements between the reference and incoming data are indicated by a 7-bit, binary weighted output. TDC1023J, introduced by TRW LSI Products, 2525 E El Segundo Blvd, El Segundo, CA 90245, meets requirements of digital signal processing systems where signal patterns are compared. Correlation is widely used to detect a desired signal in the presence of other signals or noise, to identify specific signal patterns, and to measure time delays through various mediums.

Operation of the device is centered around four 64-bit, independently clocked 40-MHz shift registers. Incoming data are clocked into the A register. The reference word is entered into the B register and then parallel dumped in the R register, allowing the user to serially load a new reference word into the B register while correlation takes place between the A and R registers. An M, or mask register, permits the user to select bit positions where no comparison is desired.

Data in the A and R registers are continually compared bit for bit by exclusive OR gates, whose outputs are applied to a digital summer via AND gates. The output of the digital summer is a 7-bit word that represents the binary weighted sum of the bit positions in the A and R registers that are in agreement. The mask register allows the user to work words of less than 64-bits and to eliminate bit positions of no interest. This register is employed by inserting logical 0s in the no comparison bit positions. Masked bits are prevented from reaching the digital summer because the outputs of the M register are applied to AND gates that also contain outputs from the exclusive-OR gates.

Either true or inverted binary outputs can be obtained from the correlator through use of the INV control line, which is applied to seven exclusive-OR gates that accept outputs from the digital summer. Outputs from gates are applied to 3-state output buffers controlled by a signal TRI. Logical 1 applied to TRI disables the buffered outputs by placing them in their high impedance state. When INV is a logical 1, the output lines are inverted and when INV is logical 0, they are true.

A correlation threshold, indicated by flag T, can be established with the independently clocked, 7-bit T register. This is accomplished by first placing the output lines (D_0 to D_6) in their high impedance state through the use of TRI. Then these output lines can be used to insert the binary weighted threshold number into the T register. When the binary weighted number from the digital summer is equal to or greater than the threshold number stored in the T register, flag T becomes a logical 1, showing that the threshold conditions have been met.

Expansion of correlation codes in multiples of 64 bits can be accommodated using the A_{OUT}, B_{OUT}, and M_{OUT} lines available on each chip. These outputs are applied to the corresponding A_{IN}, B_{IN}, and M_{IN} lines of the succeeding chip. With this arrangement an external digital summer must be used to obtain the final sum, a function obtained by a binary adder. Also, an external IC equivalent of the threshold register must be used if that function is desired. The maximum number of correlators that can be used in cascade is limited by the loading and speed of the external circuits. The device is housed in a 24-pin DIP and operates from a single 5-V supply. Inputs and outputs are TTL compatible.

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Advanced Design and Construction Improve Op Amp Performance

Four recently released operational amplifiers exhibit performance gains attributable to improved construction and design. The first is a monolithic BIFET buffer operational amplifier integrated circuit, claimed to be the first of its type in the industry, from Texas Instruments Inc. The low power unity gain voltage follower amplifier, designated TL068, is an ideal buffer for tight space, single-line, impedance matching, remote sense applications because of its high impedance JFET input (10^{12} Ω typ), its special design, and its small size.

Advancements by Texas Instruments Inc, PO Box 225012, Dallas, TX 75265, in the construction of monolithic ICs made this n-channel junction field effect input operational amplifier possible. This technique overcomes process contamination and noise that restricted the development of practical NMOS op amps. A p-well isolates the n-type epitaxial layer from a p-implanted top gate and n-implanted channel. The device exhibits the same input common mode voltage handling capability found in bipolar circuits using PNP transistor inputs and is suited for operation in single supply systems.

Typical performance specifications include power dissipation of approximately 3.5 mW, input bias current of 30 pA, and quiescent power dissipation of 200 μA. Its high slew rate, which is set by the value of the resistor between V_{CC+} and its output, is typically 7 V/μs.

Circle 442 on Inquiry Card

Described by Intersil Inc, 10710 Tantau Ave, Cupertino, CA 95014, as "almost ideal" in terms of error free operation, low power consumption, and dc stability, the ICL7650 CMOS amp has an input offset voltage of 1 μV. Low input offset voltage and a thermal drift of 0.01 μV/°C over full temperature range are attained by virtue of a design approach in which inverting and noninverting voltages are compared in a nulling amplifier that spends alternate clock phases nulling itself and the main amplifier. Two low cost external capacitors are required to store the correcting potentials on the amplifier null inputs. Long term offset drift is 1.0 μV/year.

The dc input bias current is 10 pA and the gain is in excess of 120 dB. High slew rate is 2.5V/μs and the gain-bandwidth product is 2 MHz. Low intermodulation effects are maintained between the applied signal and the chopping frequency, so that phase error is less than 10 deg. The circuit also has a clamping option in the feedback network to reduce the gain just before the maximum output is reached. This feature avoids the overload behavior problems and slow recovery times typical of the conventional chopper stabilized op amp.

Circle 443 on Inquiry Card

PA10 and PA73, two hybrid high voltage, high current op amps available from Apex Microtechnology Corp, 1130 E Pennsylvania St, Tucson, AZ 85714, are rated for output currents up to 5 A into resistive or slightly reactive loads and up to 1.35 A into highly reactive loads. The PA10 can operate with dual supplies between 10 and 50 V and with single supplies between 20 and 100 V. Typical specifications include slew rate of 5 V/μs, unity gain bandwidth of 1 MHz, and input offset voltage of 5 mV.

These hybrid integrated circuits utilize thick film resistors, ceramic capacitors, and silicon semiconductor chips to maximize reliability and performance. Ultrasonically bonded aluminum wires prolong life at high substrate temperatures. The modified TO-3 package has light pins, all isolated from the metal case.

Circle 444 on Inquiry Card

Logic Circuit Family Speed Is Doubled

One-seventh the size of Motorola's MECL 10K transistors, the components used in the company's recently introduced MECL 10KH logic circuits reduce propagation delay time by 50%, with no increase in power dissipation. This performance improvement is the result of a high density, oxide isolated manufacturing process that Motorola Semiconductor Products Inc, PO Box 20912, Phoenix, AZ 85036, calls MOSAIC. Developed for use in the MECL Macrocell Array, this process can be used for circuits encompassing a complexity of up to 1000 gates.

Initial circuits in the family will be both electrically and pin compatible with existing 10 circuits. Circuitry will be voltage compensated and will offer improved noise margins, typically 20% better than MECL 10K, as well as improved speed. At least 11 products are scheduled for sampling during the first quarter of 1981.

Circle 445 on Inquiry Card

I/O Chip Has Three Functions

A general purpose peripheral device that combines counter/timer, parallel I/O, and interrupt controller functions is now available in sample quantities. The Z8036 Z-CIO from Zilog Inc, 10340 Bubb Rd, Cupertino, CA 95014, contains three I/O ports: two are independent; one is a double-buffered bidirectional 8-bit port. Pattern-match logic allows the ports to be used as interrupt controllers. The chip also has three independent 16-bit counter/timers, each with up to four external access lines.

Two versions allow interfacing to many microprocessors. Z8036 Z-CIO is designed for multiplexed address/data bus structures such as that of the 16-bit Z8000, and Z8536 CIO is intended for non-multiplexed CPUs such as the 8-bit Z80. CIO interfaces with peripherals such as printers and display drivers. A number of programmable options allow the device to be tailored for specialized uses. It is seen, by the manufacturer, as suitable for realtime applications such as the counting and timing of events and for externally controlled time-out functions. Ceramic and cerdip packages are offered as well as the standard DIP.

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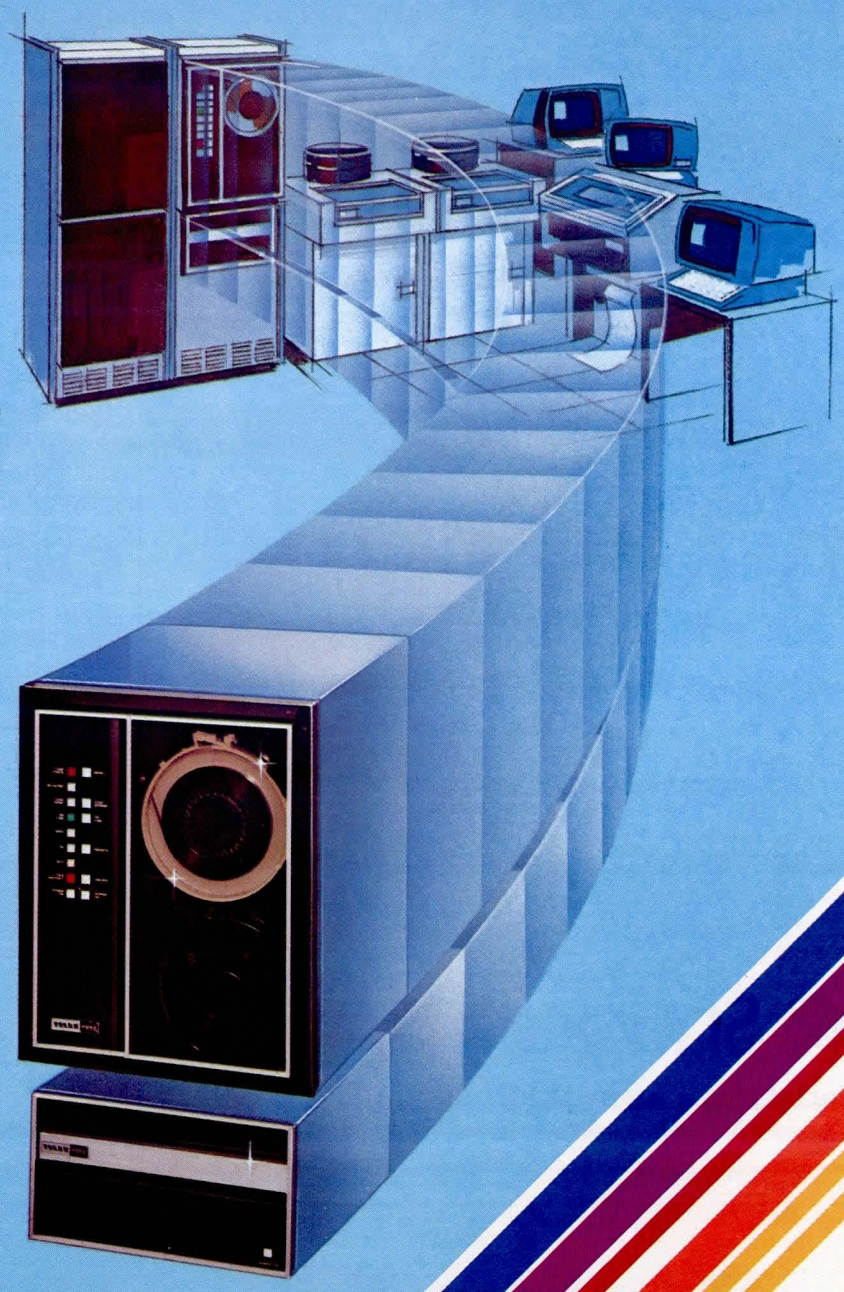

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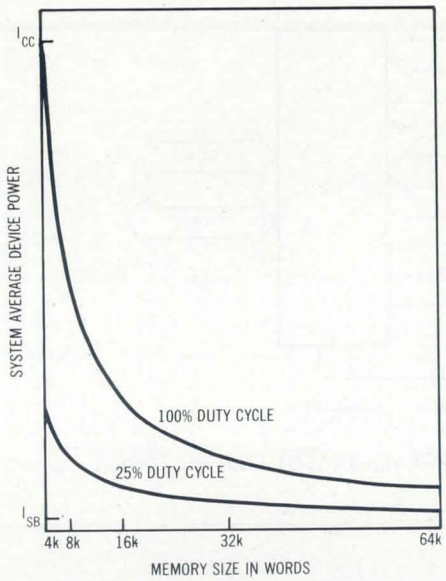
Static RAM Includes Automatic Power-Down Without Clocks



Average device dissipation as function of memory size. Power consumed by Motorola MCM2147 declines as system size increases, asymptotically approaching shown standby power level. In large systems, where most devices are deselected, power savings of 85% are claimed

A 4096-bit static RAM, MCM2147, implemented in N-channel silicon gate MOS technology, provides the simple timing features of fully static memories and the reduced standby power associated with semi-static and dynamic memories. It is produced by Motorola Semiconductor Products, Inc, 3501 Ed Bluestein Blvd, Austin, TX 78721, with a high performance MOS technology that combines onchip substrate bias generation with device scaling to attain high speed.

The low power standby feature is controlled with the chip enable input. Chip enable is not a clock and does not have to be cycled. This allows the user to tie chip enable directly to system addresses and use the line as part of the normal decoding logic. A clock or timing strobe are not required.

When the device is deselected, it automatically reduces power requirements, resulting in significant systems power savings. Unselected devices draw low standby power, and only the active devices draw active power. Power-down is obtained without any performance degradation since access time from chip enable is no greater than the access time from address valid. Because the fully static design yields access times equal to cycle times, multiple read or write operations are possible during a single select period. Data rates are 14.3 and 18 MHz for the MCM2147-70 and MCM2147-55, respectively.

Circle 447 on Inquiry Card

Static RAM Available with Military Testing

Claimed to be the densest static RAM available with full military testing, the MKB4118 has access and cycle times of 150 ns for model P-82 and 200 ns for model P-83 and is designed for wide word memory applications. The 1k x 8-bit device is powered by a single 5-V supply and has a low power operation of 400 mW active.

Processing is to Class B requirements of MIL-STD-883, method 5004, and the allowable operating temperature range is −55 to 125 °C. The device is suitable for performance upgrade applications and is packaged in a 24-pin ROM and P/ROM compatible DIP.

Output enable and chip select (CS) controls are provided for interface in microprocessor or the other bus oriented systems. A flexible latch function permits latching of the address and CS status at the user's option. Common data address bus operation may be performed at the system level. The device is available from Mostek Corp, 1215 W Crosby Rd, Carrollton, TX 75006.

Circle 448 on Inquiry Card

Programmable Channel Selection Plus Linearity

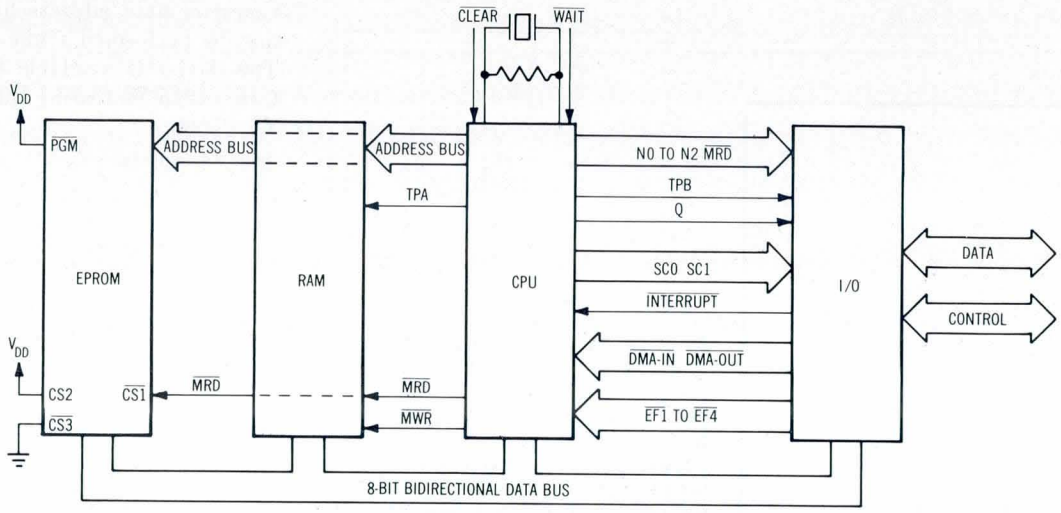
Integrated circuit series can be programmed for three to seven channels in digital encoding and decoding applications and can replace as many as four conventional ICs as well as several discrete components. Three devices are included: the NE5044N, an encoder circuit programmable for from three to seven channels of information; the NE5046N, a 7-channel decoder that accepts either positive or negative serial inputs and provides parallel outputs; and the NE5046N, a 2-channel decoder for systems of lower complexity.

Improved linearity is claimed for the devices, typically 0.3% versus about 5% for conventional ICs of this type, resulting in improved control and monitoring performance. According to Signetics Corp, 8811 E Arques Ave, Sunnyvale, CA 94086, conventional ICs of this type have a fixed number of channels, and the encoder and decoder must be paired. The NE5044N can be used in applications requiring three to seven channels and be paired with the 7-channel NE5045 decoder. This combination can replace four conventional ICs and a number of discrete transistors, resistors and capacitors.

Compatible with almost any transmission medium in remote control applications, the encoder/decoder ICs work with either pulse width modulation or digital encoding techniques. Applications include data transmission and security systems. The NE5044 and NE5045 are available in either standard DIP or an SO microminiature plastic package.

Circle 449 on Inquiry Card

Asynchronous EPROM Designed for Microprocessor Interface



CDP18U42CD EPROM from RCA/Solid State Div directly interfaces CDOP1802 microprocessor. Three CHIP-SELECT signals ($\overline{CS1}$, CS2, and $\overline{CS3}$) are provided

Designed for simplicity and low power consumption, a 256-word by 8-bit static CMOS electrically programmable read only memory is intended for general purpose asynchronous ROM applications. CDP81U42CDE, from RCA/Solid State Div, Rt 202, Somerville, NJ 08876, is compatible with, and will interface directly to, the CDP1802 microprocessor. It has common data inputs and outputs and uses a single power supply during read operations. The EPROM is implemented with the company's ion implanted, silicon gate CMOS technology.

Erasable with 2500-Å ultraviolet light, the device is suitable for uses where rapid design changes are necessary. The erase procedure is a bulk erase in which all 2048 bits assume a 0 state (outputs = low), allowing the user to program a new bit pattern. Erasure occurs with exposure to light of wavelengths shorter than approximately 4000 Å. (Extended exposure of the device to sunlight or certain types of fluorescent lamps that have wavelengths in the 3000- to 4000-Å range will require that opaque labels be placed over the transparent lid to prevent unintentional erasure.)

After being erased, the device exhibits a 0 state (output = low) in all locations. Introducing a 1 state (output = high) in the desired bit locations programs the EPROM. Programming is done on a byte basis; any previously erased bits may be selectively programmed to a 1 state. This feature allows the user to change any 0 bits to 1s within a particular byte without having to bulk program or bulk erase.

The program procedure consists of addressing a word, selecting the device with the program (PGM) input at a logic 0, and raising the inputs to the proper program voltage. During a read operation, the device functions as a normal CMOS ROM. Reading is accomplished by addressing a word and selecting the CDP18U42C, with the PGM input at a logic 1.

A functional replacement for 1700-series UV erasable P/ROMs, the device has 1-μs maximum access time, 5-s typical programming time, typical data retention of over 17 years, and a write/erase endurance of over 300 cycles. The EPROM is supplied in a 24-lead hermetic DIP.

Circle 450 on Inquiry Card

Realtime Clocks Designed with Bidirectional Bus

A bidirectional data bus facilitates microprocessor interfacing with the MM58167 and MM58174 Microbus compatible realtime clocks. Both devices from National Semiconductor, 2900 Semiconductor Dr, Santa Clara, CA 95051, are suited for use in point of sale terminals, word processors, bank terminals, event recorders, and computer systems requiring realtime operation.

The 16-pin DIP MM58174 measures from tenths of seconds through months and includes a write only register for leap year calculation. Housed in a 24-pin DIP, the MM58167 measures thousandths of seconds through months and has corresponding addressable latches for alarm functions. Both feature addressable realtime counters. CMOS technology allows for a separate power-down mode that disables all outputs except interrupt outputs. The timebase is generated from a 32,768-Hz crystal controlled oscillator.

Baud Rate Generator Provides 13 Bit Rates With Crystal Accuracy

Controlled by a crystal oscillator, the QT 1010 baud rate generator from Q-Tech Corp, 2201 Carmelina Ave, Los Angeles, CA 90064, provides 13 commonly used bit rates and is capable of controlling up to 8 transmission channels. Baud rate output is selected by the application of appropriate logic highs and lows to the four rate select inputs. The baud rate generators are fully compatible with Mil-spec environmental requirements. Frequency tolerance over operating temperature ranges can be specified from ±0.01% over 0 to 70 °C to ±0.005% from −55 to 125 °C. Applications are seen in modems and data transmission UARTs.

Circle 451 on Inquiry Card

8-Bit DAC Implemented Without Laser Trimming

A low power 8-bit buffered multiplying monolithic DAC, designed as a replacement for the AD7524, will directly interface microprocessors such as the TMS 8080A, MK3870, MC6800, SY6500, S6800, 8080A, 9080A, and S9980. MP7524, from Micro Power Systems, 3100 Alfred St, Santa Clara, CA 95050, is implemented in advanced HD/CMOS and thin film technology, thereby eliminating the requirement for laser trimming.

Accuracy to ±1/8 LSB with power dissipation of 10 mW is claimed. Multiplying characteristics (2- or 4-quadrant) and low cost make the device suitable for many microprocessor controlled gain setting and signal control applications. Other specifications include accuracy of ±0.05%, 10-ppm gain tempco, and a settling time of 100 ns.

Circle 452 on Inquiry Card

Hybrid Manchester Converter Interfaces MIL-STD Data Bus

A MIL-STD-1552B command/response Manchester II converter from ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716, provides multiple functions in a single hybrid package. Bus-8937 accepts serial Manchester II encoded data from transceiver, decodes the data, performs a serial to parallel conversion, and delivers 16-bit parallel TTL data to the operational bus system through double-buffered 3-state outputs. When parallel data are presented to the device, the operational sequence is reversed. Data to and from the subsystem are transferred on a common 16-bit line bus.

The 48-pin hybrid performs in severe military and industrial applications. Operating temperature limits are −55 to 125 °C. In storage the temperature limits are −55 to 135 °C. The unit operates from a 5-V input at 200 mA max. Power consumption is less than 1 W. Other features include built-in address decoding and recognition and wraparound self test capability.

Circle 453 on Inquiry Card

CMOS P/ROM Is Electrically Erasable

Providing the low power advantages of CMOS in a nonvolatile memory, the HNYM 3008 can replace low power ultraviolet erasable P/ROMs or high density nonvolatile memories. The electrically erasable P/ROM is organized 1024 x 8 and is compatible with TTL, NMOS, PMOS, and CMOS. Available from Hughes Solid State Products Div, 500 Superior Ave, Newport Beach, CA 92663, the device has 3-state outputs for microprocessor bus compatibility.

Access time from chip enable (an edge triggered input) is typically 500 ns. Erasure or programming can be done while the device is in-circuit. The entire chip can be erased and reprogrammed in 0.1 s. Erasure or programming is accomplished by raising the supply voltage of 17 V. The program mode typically draws 1 mA from the 17-V supply.

Retention time is estimated at 10 years at 100 °C, and endurance or the number of erase program cycles is at least 100k cycles. Both characteristics are about 10 times greater than present nonvolatile memory devices.

The device is the first in the manufacturer's series of CMOS nonvolatile memories. A 4k (512 x 8) version is planned. Electrical programming and erasure is possible because of the proprietary nonvolatile CMOS process that uses a floating silicon gate for storage within a thin tunnel oxide.

Nominal standby power is 50 μW, and operating power, at 200 kHz, is 5 mW. A single 5-V supply is required in normal read operations.

Circle 454 on Inquiry Card

Fast Octal Transceiver Offered for Microprocessor Interface

Designed for high speed asynchronous 2-way communication between data buses, the SN74LS245 bipolar transceiver can replace two quad transceivers or two octal buffers and is implemented in a 20-pin skinny DIP™. The dual 8-bit device from Monolithic Memories Inc, 1165 E Arques Ave, Sunnyvale, CA 94086, has 3-state outputs and a data path logic delay of 12 ns max. With outputs low, typical supply current is 62 mA. Pin compatible with the company's first octal transceiver, the device provides improved speed, reduced input current, and reduced high impedance state leakage currents.

Data transmission between buses is allowed and depends on the logic level at the direction control input. The enable input can be used to disable the device so that the buses are effectively isolated. Control function implementation minimizes external timing requirements. Typical applications are single-board microcomputers, memories, peripherals, high performance TTL minicomputers, byte multiplexing memory interfaces, and communications equipment.

Circle 455 on Inquiry Card

3½-Digit A-D Converter Second Sourced

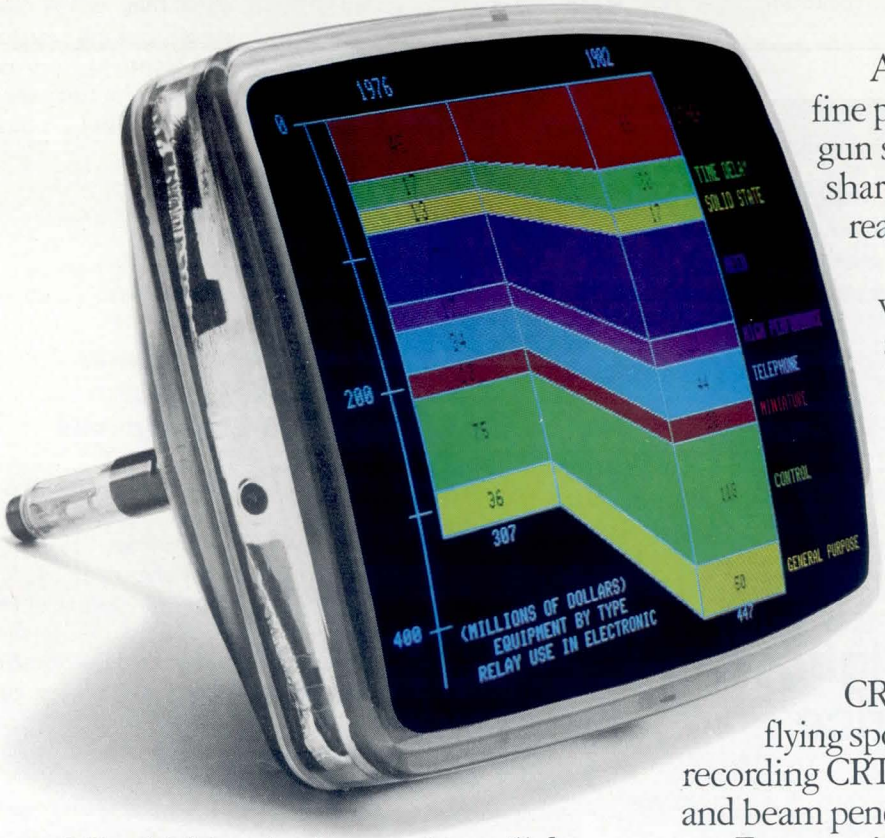
A 3½-digit monolithic CMOS single-chip A-D converter recently announced by Teledyne Semiconductor, 1300 Terra Bella Ave, Mountain View, CA 94043, is an alternate for the low power device that is used in low speed data conversion applications requiring display. The 7106/7107 contains 7-segment decoders, display drivers, references, and clock. Model 7106 interfaces with a liquid crystal display and includes a backplane drive; model 7107 directly drives an LED display with 8 mA per segment.

A panel meter can be built by adding a display, four resistors, four capacitors, and a single power supply. Assembled, the panel meter has a full scale as low as 200 mV with input noise of 10 μV pk-pk. It is claimed to autozero to within 10 μV, have zero drift of less than 1 μV/°C, input bias current of 10 pA max, and rollover error of less than one count. Internal reference is typically 100 ppm.

In addition, the device has true differential input allowing for the output measurement of load cells, strain gauges, and other bridge type transducers. Offered in 40-pin plastic or ceramic packages, the device is available in normal or reverse pin configuration.

Circle 456 on Inquiry Card

FOR A CLEANER, BRIGHTER PICTURE, TRY A TUBE OF MITSUBISHI.



Mitsubishi cathode ray tubes will do wonders for your image.

Because each of our high-resolution color CRTs actually discriminates among 64 distinct colors.

Our radar CRTs give your data systems the kind of pin point clarity that assures pin point accuracy.

And our black and white CRTs differentiate between shades of grey.

We begin with our own phosphors, specially developed for their brightness. They give our screens their notably short, or long flicker-free persistence.

Our precision electron gun system insures that each beam is perfectly aligned with the shadow mask.

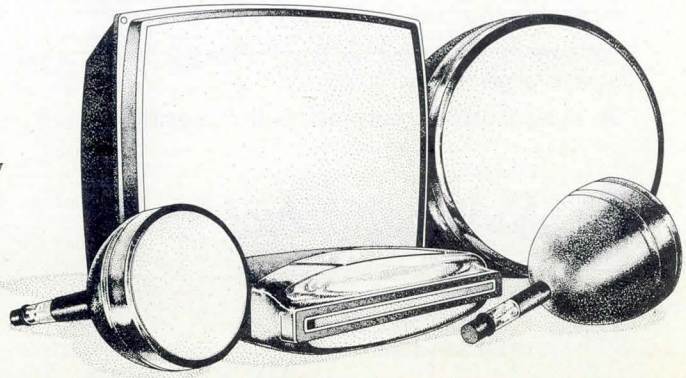
And, combined with our ultra-fine pitched shadow mask, the gun system produces a picture so sharp, it actually encourages reading fine print.

Another Mitsubishi innovation is our internal magnetic shield. It not only more efficiently eliminates exterior magnetic forces, but makes the unit much easier to service. Not to mention what the magnetic shield does for a purer image, in both monochrome and color.

Mitsubishi's complete CRT line includes high-resolution flying spot scanner CRTs. Fiber optic recording CRTs. High-precision display, radar and beam penetration CRTs.

For more information on a display that's worthy of your data system, call our Display Products Group at (213) 979-6055 (or in New Jersey, call (201) 753-1600) or write Mitsubishi Electronics of America, Inc., 2200 W. Artesia Blvd., Compton, CA 90220.

We'll gladly show you a CRT for sore eyes.



MITSUBISHI ELECTRIC COLOR CATHODE RAY TUBES

CIRCLE 92 ON INQUIRY CARD

ICs Provide Low Cost Dc-dc Converter Function

A family of miniature dc-dc converters from Power General, 152 Will Dr, Canton, MA 02021, finds uses in analog and digital applications. The devices are suited for powering A-D or D-A converters, op amps, RAMs, and P/ROMs.

Designated the 500 series, the converters provide a variety of isolated outputs from either 5- or 12-V inputs. Input to output isolation is 300 Vdc min with an impedance of 10 MΩ.

These ICs are provided in 24-pin, dual inline packages that allow direct mounting on a PCB. Model types are available with single polarity outputs of 5 V at 100 mA, 12 V at 80 mA, and 15 V at 65 mA. Dual output models provide ±12 V at 80 mA or ±15 V at 65 mA. Prices are $29 for the single and $34 for the dual output versions.

Temperature coefficient is ±0.015%/°C over the full operating temperature range of −25 to 70 °C. Other basic specifications include ±0.3% time regulation, ±1% load regulation, 100-mV pk-pk output ripple and noise, transient recovery time to within 0.1% of the final value in 25 ms, and an output voltage tolerance of ±5% max.

Circle 457 on Inquiry Card

16-Bit MDAC Features Input Storage Registers In Two 8-Bit Segments

Not all applications requiring 16-bit resolution need full 16-bit linearity. Therefore, Hybrid Systems, Crosby Dr, Bedford Research Park, Bedford, MA 01730, has announced two new versions of its 16-bit hybrid latched multiplying digital to analog converter (MDAC). Both are suited for lower cost systems where critical 16-bit linearity is unnecessary, but where 16-bit resolution is desired.

The DAC9331-16 series incorporates input storage registers in two 8-bit segments, with independent latching and offers 14- (±0.003%), 15- (±0.0015%), and 16- (±0.0008%) bit linearity while maintaining 16-bit resolution. Additionally, all units provide 2- and 4-quadrant multiplication, 2-μs settling time, and a gain drift of ±2 ppm/°C. All are TTL/DTL and CMOS compatible and are constructed utilizing 2-chips within a 24-pin DIP. The device operates from a 15-V power supply, dissipating <60 mW.

One chip contains switches, storage registers, and other electronics for high resolution and low linearity error. The second provides the precision 16-bit resistor network. Based on CMOS technology, this MDAC constitutes a system that is compatible with microprocessor data bus interfaces. It is specified for a temperature range from 0 to 70 °C in operation and 0 to 85 °C in storage.

Circle 458 on Inquiry Card □

How to lose excess wait.

Mil-spec plasma displays in 90 days.

Now you can take delivery on our PD 3500 in just 90 days ARO. We're building our mil-spec plasma unit in assembly-line style.

You still get the same rugged unit that shrugs off heat, vibration and grime. It's perfect for aerospace, military and severe industrial use.

And plasma gives you a clear, bright image with no flickering. A big, easy-view, flat plane screen. Plus a skinny, 6-inch body that fits where you want it.

The cost is actually lower than a ruggedized CRT. And it lasts up to five times longer. You save money.

It's mil-spec quality at a mass-production price. Get the complete data package on the PD 3500.

Call or write today to Marketing Manager, Display Products, Interstate Electronics Corp., 1001 E. Ball Road/P.O. Box 3117, Anaheim, CA 92803, (714) 635-7210.

INTERSTATE ELECTRONICS CORPORATION

SUBSIDIARY OF ATO

CIRCLE 94 ON INQUIRY CARD

Replace CRT's With Rugged $249 TERMINAL

Tough, waterproof TM25 Microterminal doesn't sacrifice function or efficient man/machine interface for its low cost. Yet TM25 can replace expensive, fragile CRT's when all their data entry, editing and display features aren't needed - or when their size or environmental limitations prevent their use.

TM25 communicates in serial ASCII (at 300 baud) with 20mA current loop and RS232C/V.24 conditioning up to one mile from your CPU. Its buffered data feature allows message verification before transmitting - then sends data to the computer on-line at maximum speed.

Eight-digit LED display reports system data and visually verifies keyboard entries with hexadecimal (0-F) and numeric characters. Hex or numeric keyboard and function key pad offer tactile response. Seven function keys initiate preprogrammed computer action with single key input. Function indicators confirm CPU response or call for operator action.

MULTIDROP/POLLING NOW AVAILABLE!

New TM25 - Multidrop allows a number of terminals to be connected to the same serial interface. The computer polls each unit for data. Price of the TM25 Multidrop is $325.

Mount the 8.5" x 4.5" x 0.6" module on any flat surface - a DB25 connector provides signal I/O and power. Warranted one year!

BURR-BROWN

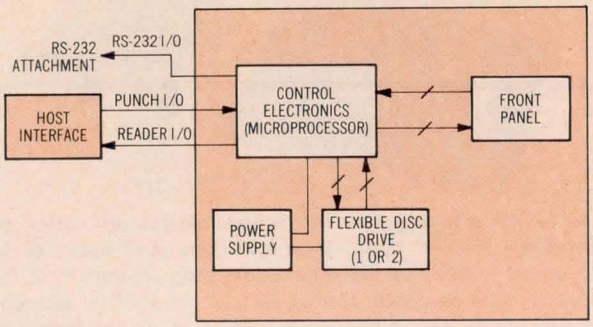
Putting Technology To Work For You

For details call Burr-Brown: **BOSTON** - (617) 444-9020 - **CHICAGO** - (312) 832-6520 - **COLUMBUS** - (614) 746-9764 - **DALLAS** - (214) 823-2310 - **HOUSTON** - (713) 988-6546
LOS ANGELES - (714) 835-0712 - **NEW YORK** - (914) 253-9333 - **SAN FRANCISCO** - (408) 984-7700 - **TUCSON** - (602) 746-1111

CIRCLE 95 ON INQUIRY CARD

PRODUCT FEATURE

Flexible Disc Subsystems Replace Slower Paper Tape Peripherals without Changes in Software



Flexible disc based, microprocessor controlled subsystems that appear to the user as if they were paper tape based peripherals have been introduced by Remex for applications usually handled by paper tape reader/punch combinations—such as numerical control—or for backup to other storage systems. Although these tape emulating subsystems, RT20XX and -40XX, provide the advantages of faster data transfer and greater memory storage gained from flexible discs, they require little or no modification to the familiar paper tape based software and hardware. One version is a single-drive read only model; the other will read and write and is available with either one or two disc drives.

Component Features and Capabilities

Standard components of the tape emulating subsystem are the flexible disc drive, control electronics, a power supply, an enclosure for the components, and a front panel. (See diagram.) A serial interface is offered as an option.

The flexible disc drives are a "slimline" minidisc version using 5.25" (13.3-cm) single-sided media. They operate in single-density mode using a modified frequency modulation (MFM) encoding scheme and can access 35 tracks/diskette (34 tracks for data, 1 track for system directory). Diskette format is 10 sectors/track, 512 bytes/sector. Capacity is 87k bytes/diskette, which is equivalent to 725 ft (221 m) of paper tape.

Control electronics—the microprocessor, its related devices, status indicators, and all interface and buffer electronics—are on a single PC board. The data buffers consist of random access memory that reads and stores four sectors of data per sweep, for a total of 1k bytes.

All subsystem enclosures measure 5.25 x 71 x 11" (13.3 x 43.2 x 28 cm) and are sealed to prevent external contaminants from entering and damaging the media. An optional cover provides further protection by sealing the openings of the drives when they are not in use. The subsystem's power supply is housed within the enclosure. The front panel contains an 18-key keypad for entering various commands into the system, the on-off switch, and LED indicators for displaying system status.

A parallel interface is standard but a serial interface is available as an option. With this option, choice of interface is made through a user accessible switch in the rear of the enclosure that selects whether the unit will operate through the serial or parallel interface port. The serial interface operates in either RS-232 or current loop mode. For the parallel interface, the user has the choice of either the 20-mA source in the subsystem or a supply current within a 20- to 60-mA range from an external source. Read speed is 150 to 1500 char/s.

Actual interface consists of 12 lines, 2 to transmit and receive data in RS-232 mode, 4 to send and receive data in current loop mode, 3 modem controls (RTS, CTS, and DTR), 1 as an optional reader start/stop control, and 2 for chassis and signal grounds. The reader start/stop line has TTL style rather than RS-232 compatible input.

A PC board switch is used to choose either TTL or the CTS modem control input as reader control. Other PC board switches allow selection of baud rates (75 to 19.2k), number of stop bits (1, 1.5, or 2), and character bit length (5, 6, 7, or 8); and choice of parity control (odd, even, or no), mode (local or remote), and delays between the transmission of characters (0 to 750 μs in 50-μs increments) to allow time to control the CTS line for reader control.

Operating temperature range for the subsystem is 10 to 65 °C (but presently limited to 40 °C because of temperature range of medium); nonoperating range is −40 to 85 °C. Relative humidity range is 20 to 80% without condensation. Operating pressure range is 500 ft (0.15 km) below sea level to 10,000 to (3 km) above; storage range is 1000 ft (0.3 km) below sea level to 50,000 ft (15 km) above.

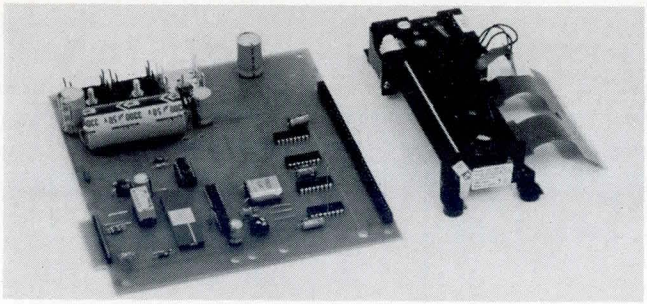
Price and Delivery

The single-drive read/write combination subsystem is priced at $1795 in single quantities. Other prices were not available at press time. Deliveries will begin in the first quarter of 1981. Remex Div, Ex-Cell-O Corp, 1733 E Alton St, Irvine, CA 92713. Tel: 714/557-6860.

For additional information circle 199 on Inquiry Card.

PRODUCTS

Variable Speed Thermal Printer/Plotter Reproduces Full CRT Display as Hard Copy in 14 s



Sprinter 40, a high speed matrix thermal printer/plotter plus control electronics, operates at a variable print speed of 120, 180, or 240 full 40-char lines/min under program control (2, 3, or 4 lines/s). The character format is 5 x 7 dot matrix, with complete 96 ASCII u/lc characters; in graphic mode, the format is a full 280 x n dot matrix. The time required to print hard copy of a complete 280-line CRT display is 14 s. Programmable ASCII controls include automatic carriage return, automatic line feed, reset, right justification, form feed, graphic control, and multiline feed.

An EM1840 interface electronics board provides user selectable parallel interface of 7-bit ASCII, Strobe, Busy, and ACK, as well as RS-232 serial interface with selectable baud rates of 110, 150, 300, 600, 1200, 2400, 4800, and 9600, with 1 or more stop bits. A full 40-char line buffer is provided by the printer controller. The printer can be connected with Radio Shack TRS-80, Apple II, Atari 800, Commodore PET, and other computers using standard interfaces. Printer/plotter dimensions are 10.5 x 7.5 x 4″ (26.7 x 19 x 10.2 cm). Its power requirement is 117 Vac, 50 to 60 Hz; consumption is 30 W. **Alphacom, Inc,** 3031 Tisch Way, San Jose, CA 95128.

Circle 200 on Inquiry Card

Low Cost Programmable Digital Multimeter Provides Capabilities of Expensive Units

Standard user oriented features of the model 192 programmable DMM are claimed by the manufacturer to normally be found in competitive instruments costing 3 to 5 times as much. Among these features are 0.005% accuracy, 1-μV sensitivity, 6.5-digit resolution, front panel math functions, data storage capability, 150-ms per range change autorange, 1-button zeroing, speed of over 25 readings/s at 4.5-digit resolution (or 20/s at 5.5 digits), and input impedance of 10^9 Ω up to the 20-V range.

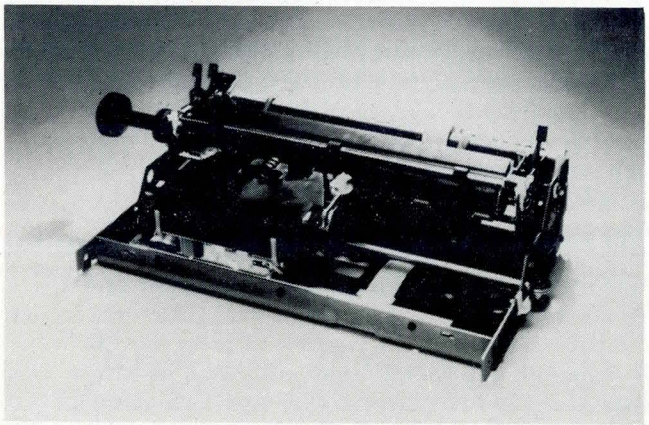
An ac volts function using ac averaging and full IEEE-488 interface capability are available options that can be added at any time. Math functions include scale factor and offset modifications (Y = sX + b), percent deviation from an entered nominal value, storage of min/max values (also serving as peak-hold memory), and hi/lo/pass limits.

Separate inputs for ac volts, dc volts, and ohms improve accuracy because the best cable type can be used for each function. This feature also eliminates the need for a switching matrix in small systems and increases system speed because dc volt measurements can be made while the ac volts reading is settling—a savings of 1.5 s/ac measurement.

The data storage feature enables the DMM to serve also as a datalogger. Ten different reading rates may be programmed from the front panel, allowing up to 100 readings to be stored over a period of up to 4 days. Data may be manually read back through the display, or transmitted over the IEEE-488 bus for curve tracing or other manipulation on a controller. The data transmission rate depends on the controller and is independent of the reading rate. With the IEEE-488 interface, the unit becomes a fully programmable systems DMM. All ranges, functions, zero, and a choice of 9 reading rates can be programmed. **Keithley Instruments, Inc,** 28775 Aurora Rd, Cleveland, OH 44139.

Circle 201 on Inquiry Card

Character Wheel Printer Offers Increased Performance but at Lower Price



Substantial increases in the performance of several electronic and electromechanical assemblies normally found on this type of printer have been added to the Stylist™ 360 daisywheel printer. According to the manufacturer, however, the price of this unit is as much as 50% lower than existing printers on the market in spite of these improvements.

Among the features of this bidirectional, letter quality printer are a character wheel with a life expectancy of over 50M strokes (as opposed to 4M to 10M on most other such wheels), microprocessor based self test and control functions, stepper motor drive of carriage and forms feed mechanisms, and modular construction that permits onsite replacement of any of five modules. Whereas most other printers have flat character backs and flat hammers for character impression, this unit has a V-shaped notch in the hammer and an inverted wedge on the back of each symbol to ensure steady, vibration free letter impact and constant character alignment. Noise reduction of up to 10 dB below that of comparable printers has been achieved.

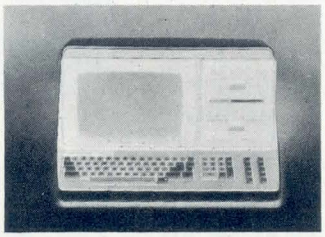
Each printwheel accommodates up to 100 char in any of several different sizes, fonts, and languages. Printing is u/lc with proportional spacing. Operation is at 17 char/s with bidirectional logic seeking for optimal utilization of the print path. Horizontal spacing is 10, 12, or 15 char/in (4, 5, or 6/cm) in 132, 158, or 198 col. Noise level is no greater than 60 dB. Included in the 28.66 lb (13 kg), 20.86 x 5.51 x 12.99″ (53 x 14 x 33 cm) housing are a 1k-bit buffer, 8-bit microprocessor bus interface, and a power supply for 220 to 240 Vac at 50 Hz or 100 to 115 Vac at 60 Hz. **Pertec Computer Corp, Peripherals Div,** 12910 Culver Blvd, Los Angeles, CA 90066.

Circle 202 on Inquiry Card

PRODUCTS

Intelligent Workstations Support Distributed Data Processing Systems

MPT/80, /83, and /87 microNOVA™ based intelligent workstations are software compatible with all of the company's processors from the 16-bit microNOVA to the 32-bit MV/8000, enabling OEMs and sophisticated end users to program in Pascal, FORTRAN IV, or assembly language. Software can be written with existing software development tools, loaded into the workstation, and executed in the field to reduce overhead on the host computer. Data can also be captured and validated and local files maintained by the workstation without the host.



In addition to a single PC board containing a 16-bit microprocessor with 60k-bytes of RAM, two RS-232-C programmable synchronous/asynchronous ports, and an external I/O bus, the model /80 has a 12″ (30.5-cm), 25-line by 80-char CRT screen and an 83-key keyboard. The model /83 has one 358k-byte dual-sided, dual-density drive, and the /87 has two drives for a total of 716k bytes of offline storage. ROM based fonts for the video display include the full 96-char ASCII set plus British, Swedish, French, German, Spanish, and Danish. Included on the keyboard are a 14-key cursor control/numeric keypad and 10 user definable special function keys.

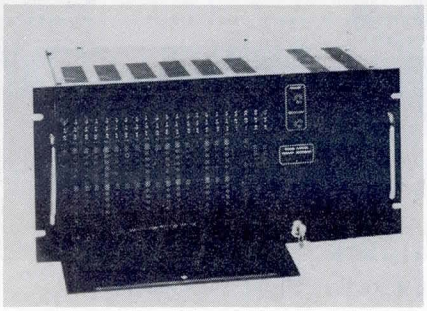
All stations execute a runtime version of the company's MP/OS realtime, multitasking operating system. MP/OS Pascal allows individual program modules containing data and procedures to be separately compiled before transfer to workstation; MP/OS FORTRAN IV provides multitasking and reentrant coding for efficient operation in realtime environments; and assembly language subroutines interface with FORTRAN IV programs to increase execution efficiency. Additional workstation software includes disc formatters, diskette copy routine, bootstrap for mini-floppy drives, disc verification utility, screen menu driver/editor, asynchronous file transfer program, software for DASHER™ D200 terminal emulation, autoprogram load software for asynchronous interfaces, and power-up self diagnostics. Diagnostic routines in dedicated ROM activate automatically on system power-up and test logic boards; CPU; communications logic; memory logic, disc drive controller logic, drives, and media; keyboard; and the diagnostic processor itself. Detected errors generate appropriate diagnostic messages.

The RS-232-C ports are used to drive a printer, to load programs from a local or remote processor, or to perform other data communications at user selectable speeds up to 19.2k baud. Other peripherals interface through the I/O bus. **Data General Corp,** Rt 9, Westboro, MA 01581.

Circle 203 on Inquiry Card

PRODUCTS

WIDEBAND MULTIPLEXER

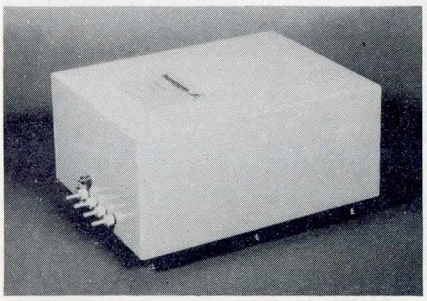


Micro750, a high speed TDM designed to function on wideband data circuits operating at speeds to 250k bits/s, allows bandwidth to be divided in any way to derive synchronous channels at lower speeds such as 2400, 4800, or 9600 bits/s. Up to 38 channels are supported. Single-ended configuration selection from central site facilitates reconfiguration in the field. The unit supports dial-up synchronous terminals as well as directly connected terminals, and leased line point to point and multipoint tail circuits, including DDS. **Micom Systems, Inc,** 9551 Irondale Ave, Chatsworth, CA 91311.

Circle 204 on Inquiry Card

SEALED SWITCHERS FOR HARSH ENVIRONMENTS

Modular, sealed, encapsulated series V-80 switching regulated power supplies are designed specifically for operation under severe conditions. Outputs range from 2.8 to 250 Vdc with power ratings to 100 W. Series is designed for MTBF of 35,000 hours at op temps from −20 to 80 °C. Specifications include ±0.05% + 5 mV line regulation, ±0.1% + 5 mV load effect, and 0.2% + 10 mV ripple. Input voltage ranges from 105 to 125 Vac, 50 to 400 Hz. All units have overvoltage and short circuit protection, slow start, remote sensing, and floating output. **Technipower, Inc,** PO Box 222, Danbury, CT 06810.



Circle 205 on Inquiry Card

INTELLIGENT COMMUNICATIONS CONTROLLER

"Digilink" features interactive communications through a modem control port, text editing through an assigned terminal port, and data collection through a printer control port. Base machine includes editor program, user prompter program, and 4k of memory (expandable to 16k). Optional firmware provides async/sync conversion, code conversion, serial to parallel connection, and IEEE-488 interface. **Digicom Data Products, Inc,** 1440 Koll Circle, San Jose, CA 95112.

Circle 206 on Inquiry Card

BUBBLE MEMORY SYSTEMS

Single-board memory systems contain 1M- or 2M-bit bubble devices, onboard controller, and all necessary electronics. The 1M-bit RBM411 retains the block replicate architecture, pin assignments, and package design of the 0.25M-bit RBM256. Constructed using 2-μm technology, the device is composed of 572 storage loops, each containing 2052 bubble positions. It is a block oriented component using redundancy to increase yield and reduce cost. Of the 572 loops, 528 are operative and include 512 for data, and 16 for addressing and error correction. Systems, each containing a controller and support circuitry, include: RMS121, a 32k-byte system containing one RBM256; RMS122, a 64k-byte system containing two RBM256s; RMS141, a 128k-byte system containing one RBM411; and RMS142, a 256k-byte system containing two RBM411s. Family members are card compatible with AIM 65 microcomputer, System 65, Motorola Exorcisor™ and Micromodule™ family, and bus compatible with 6500 or 6800 system. Each module measures 6 x 9.75″ (15.2 x 24.7-cm) and operates at 100 kHz. Host system communicates with boards via programmed I/O. **Rockwell International, Electronic Devices Div,** 3310 Miraloma Ave, Anaheim, CA 92803.

Circle 207 on Inquiry Card

INTERACTIVE CRT TERMINAL

Model 14 allows recall or replay of up to 7680 char of previously displayed data. The terminal provides a trailing-space and trailing-line suppression feature that allows both foward and backward scrolling through the previous 200 or more lines of data. Terminal also features limited block mode capability, programmable tabs and cursor symbol selection, and a function memory of 1920 chars reserved for up to 32 programmable functions (24 on dedicated keys). **Teleray, Div of Research Inc,** PO Box 24064, Minneapolis, MN 55424.

Circle 208 on Inquiry Card

MEMORY BOARD FOR WANG COMPUTERS

SMS3515 is completely compatible with Wang MVP, VP, and LVP memory boards and meets or exceeds all specifications for these boards. Parity errors on incoming and outgoing data are detected, stored in memory array, and indicated by card edge LEDs. Indicators can be manually reset. Boards are warranted for one full year. **Automated Control Systems, Inc,** 1801 130th NE, Bellevue, WA 98005.

Circle 209 on Inquiry Card

IMPACT MATRIX PRINTER

Model 88G features 100-char/s bidirectional or unidirectional printing with short line quick cancel feature, giving throughput rates of up to 150 lines/min. Full upper and lower case 96-char ASCII set is printed in a 7 x 7 matrix with print line formats of 80, 96, or 132 col over an 8″ (20-cm) print area. Serif style 11 x 7 font in 80-col mode fits correspondence applications. Clear printing on original and 2 copies is formed by 100M-char print head. Double-wide char are software selectable in any font style or density and can be intermixed on a line for message highlighting. Microprocessor controlled interface accepts either RS-232-C data up to 1200 baud or TTL level parallel data in excess of 1000 char/s. **MPI,** 2099 W 2200 S, Salt Lake City, UT 84119.

Circle 210 on Inquiry Card

RECTANGULAR CONNECTORS

RIN connectors are molded from flame retardent plastic materials and provide a positive locking mechanism that engages with an audible snap. Three shell sizes are available with 26 + 1, 51 + 1, or 74 + 1 ground contact. Ground contacts provide the earth connection prior to coupling of other contact pairs for circuit and personnel safety. Contacts are available with silver or gold plating in crimp, dip solder, solder eye, or wirewrap configurations. **Socapex**, 6660 Variel Ave, Canoga Park, CA 91303.

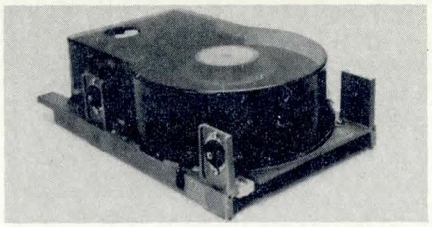
Circle 211 on Inquiry Card

SYNCHRO/RESOLVER TO DIGITAL CONVERTER

Self-contained model 5201C is capable of accepting inputs from either 1- or 2-speed (36:1/18:1) sources in either random or sequential order. No calibration or adjustments are required and the multiplexed capacity may be expanded to 128 channels. Use of continuous demodulation rather than peak sampling ensures accuracy even though system noise is present. Various synchro or resolver input combinations can be supplied to satisfy specific requirements. Interconnection with a computer is simplified via 3-state outputs. The system is completely wired, incorporates required dc power, is checked out and ready for turn on. The unit has single-speed resolution of 14 bits; output is stable and jitter free. Single-speed accuracy is ±6 arc min. Tracking rate is 360 deg/s, and channel capacity is 88 single or 44 dual. Power requirements are 115/220 Vrms ±10%, 50 to 500 Hz, and operating temp range is 0 to 70 °C. Standard PC cards are available that will convert either analog or discrete signals into digital form to become part of the multiplexed system. Logic control PC is programmed such that the channel select will set up the customer's output format. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.

Circle 212 on Inquiry Card

8″ WINCHESTER DISC DRIVE



Models 2311 and M2312 display fast average access time and high capacity achieved with a permanent magnet rotary actuator using the closed loop servo system. Complete head positioning specs are 5 ms track to track, 20 ms average, and 40 ms maximum. Enhanced Winchester 3350 type technology contact-start/stop heads are used at densities of 9550 bits/in (3759/cm) and 720 tracks/in (283/cm). Direct drive dc spindle motor rotates at 3600 r/min which yields a data transfer rate of 1.229M bytes/s. Model 2311 uses 2 platters to store 48M bytes and 2312 uses 4 to store 84M bytes. Fixed and variable sector length formats are internally selectable. Complete drive electronics are contained on 3 PC boards and provide all drive control electronics including SMD interface. **Fujitsu America, Inc,** 2945 Oakmead Village Ct, Santa Clara, CA 95051.

Circle 213 on Inquiry Card

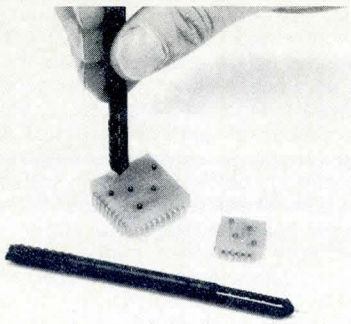
MULTICHANNEL VIDEO CONTROLLER

Single-board MCV-1023 Multibus video controller is designed for online information, graphics, and data processing applications. Compatible with Multibus architecture and various low cost CRTs, the board offers graphics capability as well as alphanumeric character generation on 2 independent displays. Onboard microprocessor performs control and logic functions, providing intermixable text and graphics display, 3 software selectable character fonts, user defined custom chars, addressable cursor, indepedently addressed status line, and onboard date and time clock. Users may intermix 24 lines of 80 char (6 x 10 field size); 16 lines of 60 char (8 x 15 field size); or 12 lines of 40 char (12 x 20 field size) on the screen. Char may be displayed with any combination of underlining, strike-through, blink, box, or reverse. Paging feature allows video on single display to be switched between sources. Communication between board and user's system is accomplished with combination of programmed I/O and shared 2k-byte block of addressable RAM. Graphics operations such as animation, facsimile, and block generation may be done with minimal software overhead. **Metacomp, Inc,** 7290 Engineer Rd, San Diego, CA 92111.

Circle 214 on Inquiry Card

PRODUCTS

MINIATURE MATRIX BOARD



10 x 10 Mini-Matrix board is designed specifically for mounting on PC boards and provides 100 crosspoints in 1 in² (6.5 cm²). PCB terminations with lead in points are provided. Gold-finish brass terminations are 0.04″ (1-mm) dia and are on 0.1″ (2.5-mm) centers. Standoffs that raise the matrix board 0.03″ (0.8 mm) above the board surface are furnished. The matrix board is also suitable for soldering applications. **Sealectro Corp, Programming Devices Div,** Mamaroneck, NY 10543.

Circle 215 on Inquiry Card

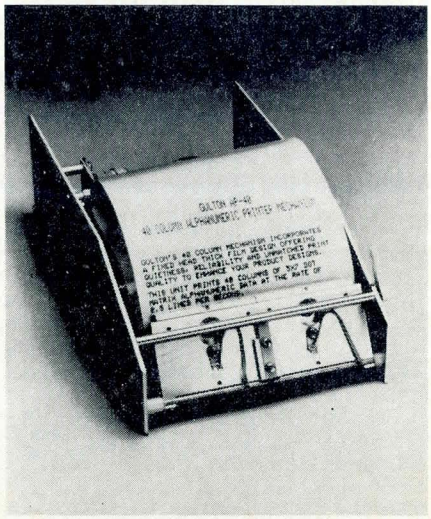
DIGITAL FIBER OPTIC SYSTEM

FDT-5/FDR-5 provides a reliable interference free transmission path for digital data at TTL levels. Offering dc to 20M-bit/s response, the system is suitable for all digital signals from completely random to virtually indefinite series of 1s and 0s. No coding, edge detecting, or system calibration pulses are necessary to institute proper operation or set thresholds. Distance limits on specified performance are determined by cable chosen for use. Using supplied cable assemblies, distances from several meters to greater than 2 km may be spanned with low bit error rate. Transmitter couples in excess of 600 μW into large core, low loss, single-fiber cable; receiver offers sensitivity of 2 μW for 10^{-10} or better bit error rate. For this combination, system will operate over a path loss of 24 dB, or 2 km of 8-dB/km fiber with one splice and a margin for time and temp degradation of 6 dB. Packaging offers PC board and panel mounting options with shielding of both transmitter and receiver against emi. All power supply inputs are bypassed to insure low susceptibility to conducted interference. **LeCroy Research Systems Corp, Fiberoptic Systems Div,** 10024 York Rd, Cockeysville, MD 21030.

Circle 216 on Inquiry Card

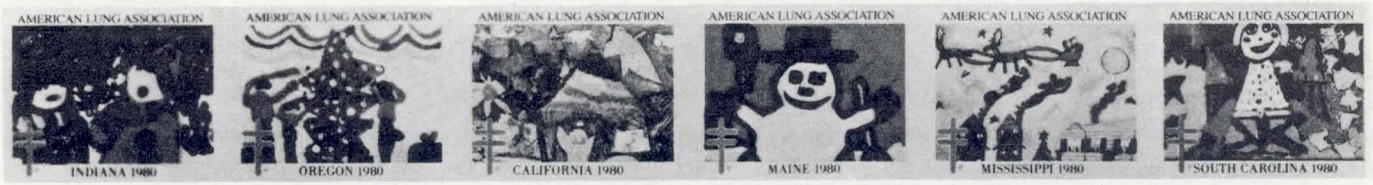
40-COL ALPHANUMERIC PRINTER MECHANISM

Designed for instrumentation output requirements preferring text format, AP-40 TM fixed head thermal printer mechanism provides 2 fixed 20-col dot matrix printheads and paper drive that feeds paper under heads to emerge in text format. Drive roll is only moving part. Printheads provide 40 cols of 5 x 7 chars 0.11″H x 0.08″W (2.8 x 2.03 mm) or 5 x 14 tall chars 0.22″H x 0.08″W (5.6 x 2.03 mm). Design also provides half-step, half-size, or bold characters. Print speed is 150 lines/min. **Gulton MCS Div,** East Greenwich, RI 02818.

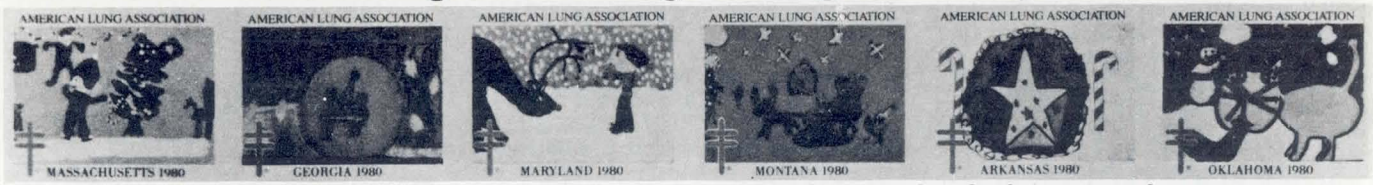


Circle 217 on Inquiry Card

THOSE CLEVER, PRETTY, USEFUL CHRISTMAS SEALS



Kids in kindergarten through third grade designed your

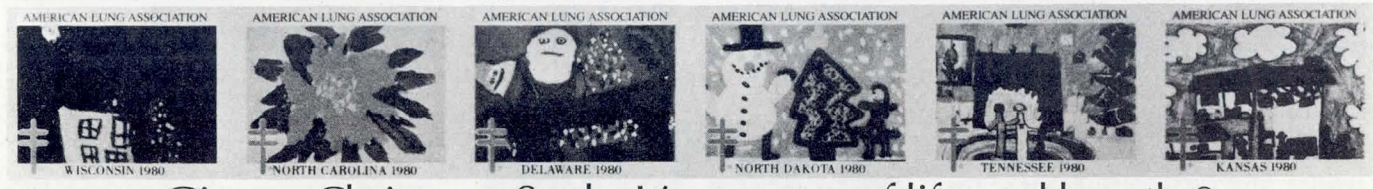


1980 Christmas Seals. To be used. On holiday cards.

Letters. Gifts. Invitations. Decorations. Each Christmas Seal

you use represents another resource put to use in the

fight against lung diseases, smoking and air pollution.



Give to Christmas Seals. It's a matter of life and breath.®

AMERICAN LUNG ASSOCIATION®

The Christmas Seal People®

Space contributed by the publisher as a public service

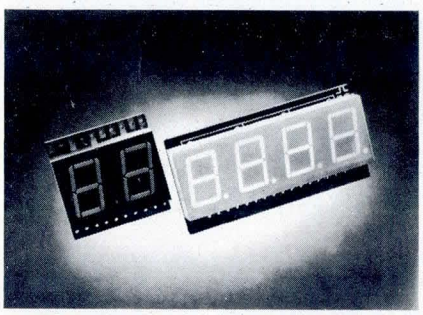
PRODUCTS

SEALED ROCKER SWITCHES

In addition to sealing the actuator, these dust and moisture resistant sealed rocker switches feature a silicon rubber seal between the base and frame that protects switch contacts and mechanisms better than conventional seal and boot combinations. Available in 5 frame styles, 6 types of rockers, single- and double-pole configuration, momentary circuits, and illuminated and non-illuminated versions, the switches have electrical ratings of 6 A, 125 Vac, 3 A, 250 Vac, and 15 A, 125 Vac, 10 A 250 Vac. **Eaton Corp, Commercial Controls Div,** 4201 N 27th St, Milwaukee, WI 53201.

Circle 218 on Inquiry Card

MULTIDIGIT 0.5″ LED STICK DISPLAY



MMN50000 series using high performance GaSsP on GaP substrate LED dice, achieves approx twice the light intensity performance of std sticks. Sticks are rated at storage and op temp of −40 to 85 °C and are available in end-stackable, 2- and 4-digit packages. Colors (prematched for brightness and hue), are orange, yellow, high efficiency red and special lens color options tailored to particular applications. **General Instrument Corp, Optoelectronics Div,** 3400 Hillview Ave, Palo Alto, CA 94304.

Circle 219 on Inquiry Card

SYNCHRONOUS LINE DRIVER

Designed for limited distance communications, synchronous line driver SLD1920 operates in both point to point and multipoint configurations at speeds ranging from 2400 to 19.2k bits/s. The unit provides error free transmission over extended distances, up to 18 miles (28.8 km) at 2400 bits/s, using local telephone loops and twisted pair lines. A special bit rate sampling technique allows handling of asynchronous devices. The device incorporates multiple self-test functions including digital loopback diagnostics. **Intertel,** 6 Shattuck Rd, Andover, MA 01810.

Circle 220 on Inquiry Card

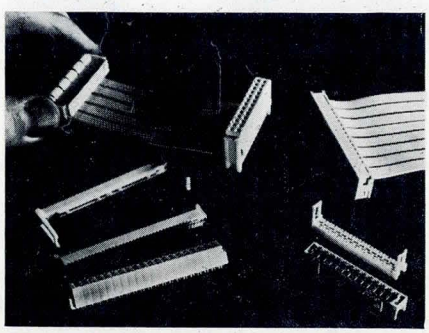
MODEM EXPANDER

Allowing 1 modem to be shared between several polled remote terminals, ME4 reduces data communications hardware costs, while retaining advantages of point to point modem operation in multipoint network. Network management features include automatic or manual disabling of streaming terminal, 3-state status monitors for modem and terminal interfaces, and terminal priority allocation. The expander is code transparent to synchronous or asynchronous data up to 19.2k bits/s. It meets EIA RS-232-C and CCITT V.24, V.28 specs and is available in standalone or 19″ (48-cm) rack-mounted versions. All CMOS design saves both space and power. Built-in proprietary Powerguard and Interguard protect the unit from external surges, increasing reliability of unit and its associated modem and terminals. Interfaces of terminals and modem are also protected indirectly. To facilitate remote site management, selected remote terminals can be taken offline using front panel push buttons. Optional data transceivers allow terminals to be located as far as 40 mi (64 km) from the expander. **Kapusi Laboratories,** 2121 S El Camino Real, San Mateo, CA 94403.

Circle 221 on Inquiry Card

FLAT RIBBON CABLE SOCKET CONNECTORS

Insulation displacement socket connectors for mass termination of 50-mil flat ribbon cable are offered in sizes from 10 to 60 pins. 8S series is designed for low profile applications and daisy chaining; 9S is available in through- and closed-end configurations and incorporates a strain relief to protect cable terminations when repeated insertion and extraction cycles occur. Positive connection between U contact and 28-gauge round conductors is insured by a special double-action slot design using two cutting surfaces. Dual-beam design of the contact receptacle grips header pins firmly aiding mating action. Specs include −55 to 105 °C temp range, 1-Adc current rating, 20-mΩ at 6-Vdc and 0.3-A contact resistance when mated with header, and 3.5- to 21-kg insertion force with header. **Belden Corp,** 2000 S Batavia Ave, Geneva, IL 60134.



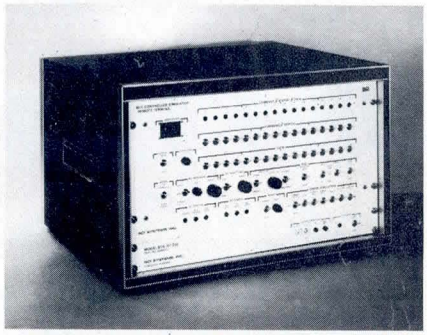
Circle 222 on Inquiry Card

CARD READER ACCESS CONTROLLER

Computer add-on intelligent card access controller ICAC has a microprocessor to decode card reader pulses, check validity, transmit card number to computer, search its internal memory, and release an electronic lock. Online capacity is 16k cards; in standalone mode (computer down) unit can control up to 1k cards. Three additional inputs can be used for other devices. ASCII code is used for data communications via either RS-232-C or 20-mA current loop interface. **Access Control Systems, Inc,** PO Box 71, Stanhope, NJ 07874.

Circle 223 on Inquiry Card

MIL-STD-1553A/B DATA BUS TESTER



BCS/RT202, operating from standard 120-Vac power, is compatible with MIL-STD-1553A/B and MCAIR A3818. Tester is capable of performing as a bus controller and remote terminal. It features several error stimulations in both operating modes and provides LED display of command, data, and status words. Contained in a 12.5 x 14.5 x 20.25 ″ (31.75 x 36.8 x 52.07-cm) cabinet, the tester can be used as a portable instrument for fault isolation. **SCI Systems, Inc,** 8600 S Memorial Pkwy, Huntsville, AL 35802.

Circle 224 on Inquiry Card

GRAPHICS/IMAGING POST-PROCESSOR

Model 3032-8 processor's 256 x 13 video lookup table (VLT) extends capability of high resolution color or monochrome display terminals, accommodating color and monochrome images requiring 256 selections per pixel and/or multilevel high resolution graphics, Processor provides 13 parallel VLT bits in color configurations of 4 red, 4 green, 4 blue, and 1 blink. In monochrome, VLT can drive 2 monitors and provides one 8-bit output, one 4-bit output, and 1 blink. **Genisco Computers, Div of Genisco Tech Corp,** 3545 Cadillac Ave, Costa Mesa, CA 92626.

Circle 225 on Inquiry Card

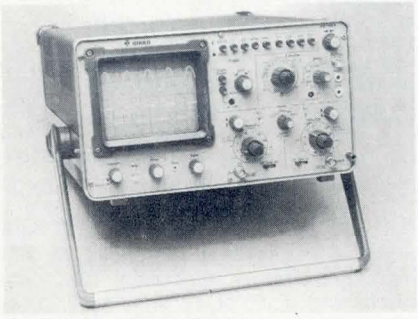
CARTRIDGE DISC CONTROLLER

DMA transfers to or from up to 4 std cartridge disc drives having capacities of 2.5M to 20M bytes are allowed by controller board. A microprogrammed control program provides range of custom commands when written to customer specs. All information transfers are accomplished through a specified area of memory, resulting in simplified operations. Errors are detected by a CRC generator that allows overlap seeks on up to 4 drives. **Central Data Corp,** 713 Edgebrook Dr, Champaign, IL 61820.

Circle 226 on Inquiry Card

30-MHz DUAL-TRACE SCOPE

Compact OS1100A features variable sweep delay. Trigger-delay feature introduces a variable delay between the selected trigger point and start of timebase sweep, permitting detailed analysis of a portion of a repetitive waveform. Delay time is variable from 10 μs to 100 ms in 4 ranges with variable vernier providing continuous selection of delay time between range limits. 8 x 10-cm CRT has 10-kV accelerating potential for bright, clear displays. Sensitivities are switch selectable from 2 mV/cm to 10 V/cm, and variable gain control can be used to increase maximum sensitivity to 1 mV/cm on both channels. Time base speeds range from 200 ns/cm to 2 s/cm and X10 magnification permits top sweep speed of 20 ns/cm. **Gould, Inc, Instruments Div,** 3631 Perkins Ave, Cleveland, OH 44114.



Circle 227 on Inquiry Card

1.8-DEG PM STEPPING MOTOR

Size 17 1.8° permanent magnet stepping motor has shielded end caps to protect against emi and provides a 5% positional accuracy. The device is offered in 2- or 4-phase versions wound for both unipolar and bipolar modes. Rotor inertia is rated at 20 g/cm². The motor is specified at 12 Vdc and 0.2 A/phase. The 1.8° step angle meets requirements for double track spacing in minifloppy disc drives. **Novatronics East, Inc,** 10 Progress Dr, PO Box 521, Dover, NH 03820.

Circle 228 on Inquiry Card

MINI-FLOPPY DISC DRIVE

A double-sided 5.25″ (13.33-cm) flexible disc drive, the model 9409 features full industry compatibility and unformatted data storage capacities of 218.8k bytes (single-density) or 437.5k bytes (double-density). Single-density operation is achieved by using FM encoding; double-density recording uses MFM. To load the unit, the operator opens the access door and inserts a diskette into the drive. When the door is closed, an expanding cone automatically centers and clamps the diskette to the drive spindle. The diskette rotates within the jacket, cushioning and cleaning the medium. Mechanical sensing through an onboard switch detects the presence of the write protect slot to safeguard against copying other data in read-only mode. This function can be disabled by covering the slot with opaque tape. Head positioning is accomplished by a band stepper mechanism that provides increased reliability. The drive requires no electrical adjustments or preventive maintenance during its estimated 5-yr service life. It requires only 12- and 5-Vdc operating power. Up to 4 drives can be configured on a single controller. **Control Data Corp,** PO Box O, Minneapolis, MN 55440.

Circle 229 on Inquiry Card

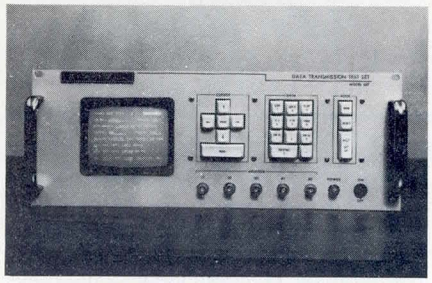
CONVERTED DEC VT100 VIDEO DISPLAY TERMINAL

Retro-Graphics VT100, a converted DEC VT100 video display terminal, features full graphics capabilities in addition to alphanumerics. Graphics upgrade features include multiple character sizes, dot-dash lines, point plotting, vector drawing, and selective erase. Emulating Tektronix 4010 series units, the terminal is completely compatible with most existing graphics software, including Tektronix' Plot 10 and ISSCO's DISSPLA and TELLAGRAF. Graphics are displayed in green tone on the 12″ (30-cm) diagonal screen at 640 x 480 resolution. Refresh raster scan technology allows display to be read in high ambient light environments. Other features include 96 u/lc ASCII chars, up to 132 char/line, numeric and function keypad, and detachable keyboard. **Digital Engineering, Inc,** 630 Bercut Dr, Sacramento, CA 95814.

Circle 230 on Inquiry Card

PRODUCTS

100M-BIT/s DATA TRANSMISSION TEST SET



Test set 607 measures bit errors, BER, block errors, second errors, and block and second throughput. Formatted 5″ (12.7-cm) CRT displays measurement results. Operating range is from 10 to 100M bits/s, and operation is simplex, or half- or full-duplex. Unit is IEEE 488 bus compatible for computer setup or hard-copy printer. Self diagnostics include clock and data loopback, insert error, slip-sync, and processor memory test. **Aydin Monitor Systems,** 502 Office Center Dr, Fort Washington, PA 19304.

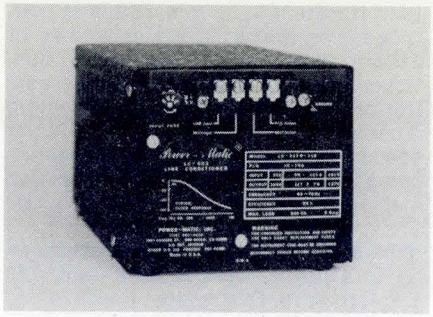
Circle 231 on Inquiry Card

PORTABLE BAR CODE READER

Lightweight compact model 9400 features rapid wand response and excellent first read rate to save operator time. Bar code alphanumeric key pad is provided for manual data entry. Variable length alphanumeric Code 39^{R} bar code labels up to 32 char long may be scanned. Solid state memory has capacity of 20k alphanumeric char and is organized into variable length records up to 63 char long. Records may consist of one or many fields. To maximize operator productivity users may select between belt clip and shoulder strap to carry the unit, keeping hands free. With campanion model 9401 charger/interface unit, flexible minicomputer interface is provided. This unit features dual RS-232-C connectors, allowing the reader to use an existing computer port. It may be operated online in terminal mode without affecting data in its memory. Data may be transmitted from memory in blocks with user defined preamble, postamble, and end of record characters. A realtime clock is available to automatically store time and date information with each record. 16-char LCD provides large easy to read chars. **Interface Mechanisms, Inc,** PO Box N, Lynnwood, WA 98036.

Circle 232 on Inquiry Card

500-W, AC LINE CONDITIONERS

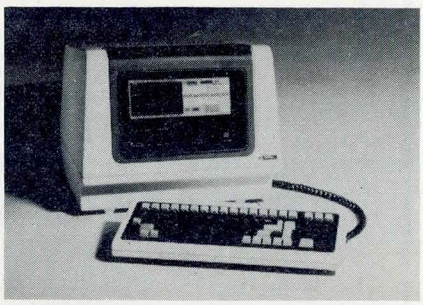


Available in 4 input ranges for brownout, narrow and wide range, and overvoltage regulation, LC-503 conditioners are rated for 500-W load, continuous duty, and can be supplied for 110- and 220-V lines. Units use patented Multi-Primary switching regulator circuit which operates at 99% efficiency and generates no spikes, noise, or distortion. Worst case, complete correction is one-half cycle. Units are insensitive to frequency, load, and power factor changes. Operating frequency is 45 to 70 Hz. Heavy duty, ac motor run capacitors are combined with basic regulator and rf filter chokes to form effective filter network that achieves normal mode noise rejection of 40 dB/decade from 6 kHz up. Network includes spike suppressor that can absorb 30 J. **Power-Matic, Inc,** 7667 Vickers St, San Diego, CA 92111.

Circle 234 on Inquiry Card

DETACHED KEYBOARD CRT TERMINAL

Multifeature model 950 offers 11 special function keys (22 functions with shift key), that can be programmed through 256 bytes of onboard RAM. These 256 bytes of memory can be distributed among the special functions keys, or concentrated within one or several. Customizable firmware results from microprocessor based design. The terminal has a display with high speed resolution that provides a 25th status and message line, and Selectric style keyboard, and operates at rates between 50 and 19,200 baud. A line drawing character set, featuring 15 special graphic characters, is standard as is the 128 displayable ASCII character set. Split screen with line lock allows operators to hold lines of copy on screen while scrolling other lines up or down. **TeleVideo, Inc,** 249 Paragon Dr, San Jose, CA 95131.

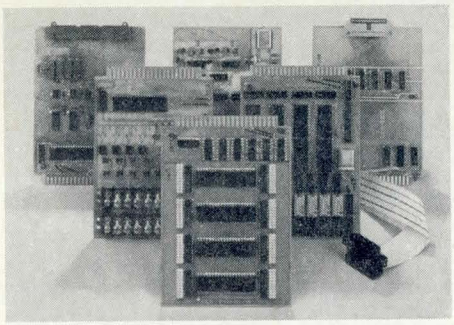


Circle 233 on Inquiry Card

SYSTEM/34 and /38 LETTER QUALITY PRINTER

A printer for IBM System/34 that is compatible with the 5250 information display system, the 5200WP consists of NEC Spinwriter^{R} quality character printer and controller. Intended for applications which require high quality printing, the unit accepts single or multipart forms, operates at speed of 55 char/s with 96-char set, and features choice of font styles, operator selectable 10/12-char pitch, and 6, 8, or 12 lines/in (2, 3, or 4/cm). Controller permits convenient workstation controller attachment to System/34, /38, or other system attaching IBM 5256 printers. With standard cable through feature controller allows 1 or more printers to attach to the workstation controller via an addressable multidrop line using twinaxial cable. The controller also provides compatibility with 5256 printer software, permitting operation with existing programs. It is compatible with all IBM workstations and operates in any system configuration consistent with normal cabling procedures. Std self-test feature is available through test switch on controller's front panel. **General Business Technology, Inc,** 2630 Walnut Ave, Suite A, Tustin, CA 92680.

Circle 235 on Inquiry Card



6800 MICRO MODULES

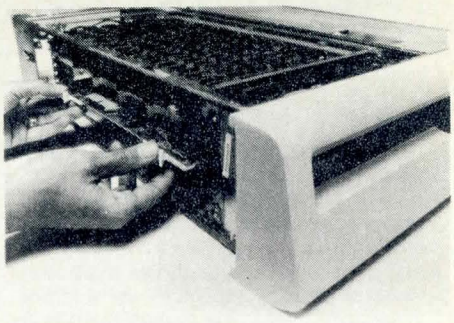
FOR INTERFACING TO: sensors, transducers, analog signals, solenoids, relays, lamps, pumps, AC motors, DC motors, stepper motors, keyboards, displays, 488 GPIB.
ADDITIONAL FEATURES: 6800 MPU, counter/timer, fail safe battery back up.
WINTEK CORP., 1801 South Street, Lafayette, IN 47904; 317-742-8428.

CIRCLE 525

STD BUS?

*Prom Programmer: Software controlled 25v generated from bus 12v static or dynamic RAM, I/O or memory mapped, Z-80, 808X, 680X. Only $165 with software listings. *Floppy Disc Controller: New chip set from WD includes PLL data separation DMA, single/double density 5/8" software selectable. Only $440 with I/O drivers for 8080/Z-80 6800; with CP/M2.2 or FLEX add $250. *CP/M2.2 for MOSTEK MD-FLP. Only $350.
INTELLIGENCE SYSTEMS LTD., 124 So. Delaware St., Indianapolis, IN 46204 (317) 631-5514.

CIRCLE 526



CHOOSY ABOUT LINE PRINTER CONTROLLERS?

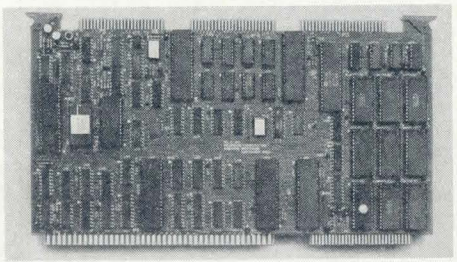
CHOOSE DATASYSTEMS. Our Line Printer Controllers are fully compatible with DEC, Data General or IBM/Series 1 computers. We offer SELF TEST verification, 12 months warranty, next day delivery and consultation on call.
DATASYSTEMS, 8716 Production Ave., San Diego, CA 92121 (714) 566-5500.

CIRCLE 527

MULTI-USER TERMINAL SYSTEM

Probably the most powerful and versatile microcomputer-based system available, Intertec's new CompuStar™ offers unparalleled price/performance value. Up to 255 terminals (called Video Processing Units) can be connected into either a 10, 32 or 96 megabyte hard disk to "share" its resources. Four models of terminals are offered, some of which contain integral floppy disks, at prices as low as $2495. Substantial OEM discounts are available.
INTERTEC DATA SYSTEMS, 2300 Broad River Road, Columbia, SC 29210 (803) 798-9100.

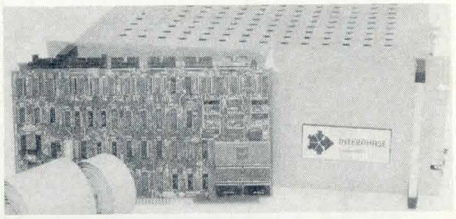
CIRCLE 528



MICROCOMPUTER WITH MORE

Heurikon MLZ-90A micro sports Z80A CPU, on-card floppy controller, DMA, 73K on-card addressable memory, 20 bit multibus compatibility, memory mapping RAM, AM9511, four 8 bit ports, four counter/timers, two RS232 ports, dual baud rate generator and XTAL, jumper selectable wait states, and monitor with CP/M bootstrap.
HEURIKON CORPORATION, 3001 Latham Drive, Madison, Wisconsin 53713 (608) 271-8700

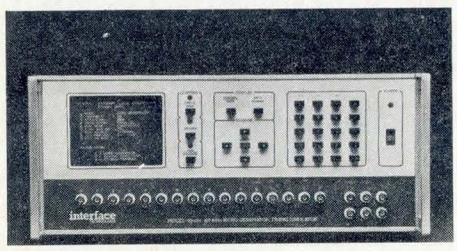
CIRCLE 529



MULTIBUS 8" WINCHESTER SUBSYS

The SMS 2180-24.R is a 24 Megabyte Winchester Subsystem for the Intel MULTIBUS. Consists of a 8" Winchester drive and power supply in a 19" rack mount enclosure, plus our Interphase SMD 2180 Storage Module Controller and cables. Software drivers for CPM, ISIS II, and RTOS operating Systems. Use as mass storage upgrade to an Intel MDS development system, or in OEM applications. List price is $7,850. Controller also available separately.
INTERPHASE CORPORATION, 13667 Floyd Circle, Dallas, TX 75243. (214) 238-0971.

CIRCLE 530



100 MHz PROGRAMMABLE DIGITAL SIGNAL GENERATOR

Model RS-680 combines the advantages of an intelligent terminal with a digital word generator. Microprocessor prompting. Test patterns can be viewed as a contiguous table. Word generator mode for synchronous serial or parallel data trains. Timing simulator mode for complex waveforms with 10 ns resolution; up to 256 states. Clock rates up to 100MHz.
INTERFACE TECHNOLOGY, 150 East Arrow Highway, San Dimas, CA 91773. (714) 599-0848.

CIRCLE 531

CP/M SYSTEM

The ISC 8300 colorgraphics CP/M system features a 13" screen that displays 48 lines by 80 characters. A special line of CP/M business software is available which has been enhanced to capitalize on the machine's vivid color displays. The General ledger package, for example, displays data with meaningful comparitive charts and graphs. The word processing system uses color to reduce operator fatigue and improve productivity.
INTELLIGENT SYSTEMS CORP. 5965 Peachtree Corners East, Norcross, Georgia 30071, (404) 449-5961.

CIRCLE 532

Presenting:

System Showcase

Your product could be represented here next month...

CALL
MAUREEN SEBASTIAN
(617) 486-8944

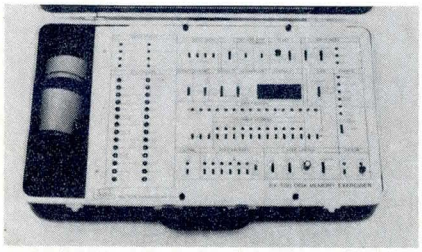
PRODUCTS

UPS GEL/CELL BATTERY

GC12550, a 55-Ah, 12-V battery, serves as power source for deep-cycle or standby power applications. Thin wall polypropylene construction allows for more active material within the battery, and gelled electrolyte allows the battery to be shipped or stored in any position. Pressurized vent seal makes the battery completely maintenance free. Low internal impedence, discharge capability in excess of 500 A, and peak power in excess of 5 kW adapt the battery to use as power source for UPS. **Johnson Controls, Inc, Gel/Cell Battery Div,** 900 E Keefe Ave, Milwaukee, WI 53212.

Circle 236 on Inquiry Card

DISC DRIVE TESTER/EXERCISER



Pluggable PC adapter modules permit SX-530 to test storage module disc drives of CDC models 9448/9760/9762/9764/9766; Kennedy model 5300; and Trident series T-25 through T-300, as well as Winchester drive. Tester automatically reads and writes data in 5 formatted modes using a selection of 3 data patterns: data composed by a bank of 16 switches, 16-bit random pattern, and cyclic pattern continuously varying throughout data field. Digital display shows data rate, data error, error per revolution, seek time, cylinder address, pass count, and sector count. **Wilson Laboratories, Inc,** 2237 N Batavia St, Orange, CA 92665.

Circle 237 on Inquiry Card

CHASSIS MOUNTABLE DC/DC CONVERTERS

CM series consists of 25 models designed for dc inputs of 5, 12, 24, 28, and 48 V. Converters are available in a 10-W single-output model that provides line regulation within 0.02% and load regulation within 0.05%, and a 12-W dual-output model that provides both line and load regulation within 0.02%. Outputs are 5, 12, 15, ±12, and ± 15 Vdc. Pi-type input filters minimize reflected ripple current and 6-sided continuous shielding offers emi/rfi protection. **Power Products, Div of Computer Products Inc,** 1400 NW 70 St, Fort Lauderdale, FL 33309.

Circle 238 on Inquiry Card

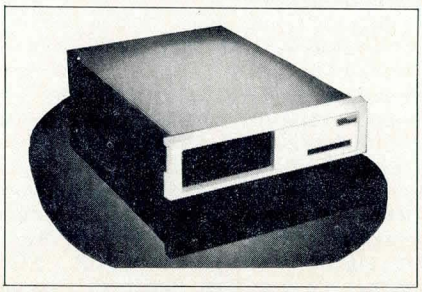
DATA COLLECTION TERMINAL

TM25M provides multidrop capability that allows a number of Microterminals to be connected to one serial computer interface. This microprocessor based data entry/data display terminal provides simplified man/machine interface at lower cost than printing terminals or full scale CRTs. The unit communicates in serial ASCII at 300 baud with 20-mA current loop and RS-232-C/V.24 conditioning. A waterproof front panel protects an 8-digit LED display and 7 function indicators as well as hexadecimal or numeric keyboard and 7 function keys. 7-segment LED display provides numeric as well as hexadecimal char. All keys have tactile feedback. Buffered data entry permits message verification before transmission to CPU and allows terminal to transmit complete messages to CPU at max speed. Depressing a function key generates preprogrammed action by user's CPU. Key functions are defined in CPU software and identified on front panel. Measuring 8.5 x 4.5 x 0.6″ (216.0 x 114.3 x 15.3 mm), the unit mounts on any flat surface. A single DB-25 connector provides power and signal I/O. **Burr-Brown,** Box 11400, Tucson, AZ 85734.

Circle 239 on Inquiry Card

WINCHESTER/FLOPPY DISC SYSTEM

Combining an 8″ (20-cm) Winchester disc and an 8″ floppy disc in a compact 5.25″ (13.3-cm) high rackmountable unit, with 8.8M-bytes total capacity, the 880 serves as an alternative to RX02 floppy and RL01 cartridge disc system. Both LSI-11 and PDP-11 interfaces are offered. The Winchester drive emulates RL01 and provides 7.8M bytes of formatted online capacity. Double-sided/double-density floppy drive emulates RX02 and provides 1M-byte formatted capacity. Control panel enables selection of operating modes, offline functions, and 'hyperdiagnostics. Offline functions include capability to copy from Winchester to floppie or to load Winchester from floppies. Hyperdiagnostics are microprogrammed routines that enable users to troubleshoot a drive without host CPU. **Data Systems Design, Inc,** 3130 Coronado Dr, Santa Clara, CA 95051.



Circle 240 on Inquiry Card

60-MHz DUAL-TRACE OSCILLOSCOPE

SC60 Widebander achieves solid waveforms on hard to hold digital signals under adverse conditions by use of ECL and differential amplifiers throughout the triggering circuits. The fast triggering circuits respond at a 100-MHz rate even when measuring a 10-Hz waveform. The scope covers virtually all digital logic families. No peaking coils are used in the vertical amplifiers, providing true waveform reproduction through its entire bandwidth. 6-ns risetime and a post-deflected CRT produce sharp bright waveforms. Sensitivity of 5 mV/cm on both channels enables the unit to be used in low level circuits. Measurement capability up to 1600 V pk-pk and protection to 2 kV allow use in circuits that would damage other scopes. **Sencore, Inc,** 3200 Sencore Dr, Sioux Falls, SD 57107.

Circle 241 on Inquiry Card

VIDEO DATA TERMINAL

Based on microprocessor controlled logic board that interprets the output of each keyboard switch, XL-83 features smooth scrolling, detachable keyboard with numeric pad, and a nonglare green phosphor CRT. Feature and code compatible with the low end LGR-2, the terminal allows direct cursor addressing, read cursor address, read character at cursor, keyboard lock/unlock, clear to end of screen, and smooth scroll on/off. **Cybernex Ltd,** 2457 Dunwin Dr, Mississauga, Ontario L5L 1T1, Canada.

Circle 242 on Inquiry Card

FIBER OPTIC CABLES

Fat Fiber cables 142 and 242 are designed for use in indoor applications over short to moderate distances. Cables have attenuation of less than 7dB/km and bandwidth greater than 20 MHz·km. Numerical aperture is 0.3 and core diameter is 100 μm. Features include high coupling efficiency, low cost sources and detectors, long link length, and an expanded range for source selection. The all-glass conductor provides immunity from interference. **Siecor Optical Cables Inc,** PO Box 489, Hickory, NC 28601.

Circle 243 on Inquiry Card

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STANDARD MICROSYSTEMS NEW 256 PAGE CATALOG

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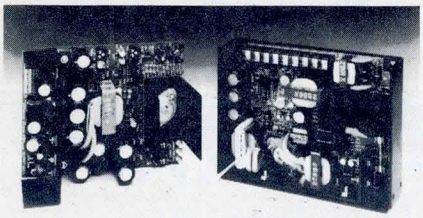
PRODUCTS

40- AND 60-W SWITCHING POWER SUPPLIES



5A and 5B series units, providing 40- and 60-W, respectively, come in 2 package sizes incorporating single- and multiple-output versions. All units incorporate an extended range ac input of 90 to 132/180 Vac for worldwide applications. Single-output models 5A5 and 5B5 deliver 5 V at 7 A and 12 A, respectively, at full load. The 40-W multiple-output 5AXMP delivers 5 V at 4 A, ±12 V at 0.5 A, −5 V at 0.5 A, and 15 V at 1.0 A. The 60-W multiple-output 5BXMP outputs 5 V at 7 A, 12 V at 1.5 A, −12V at 0.5 A, and −5 V at 0.25 A. **Sierracin/Power Systems**, 20500 Plummer St, Chatsworth, CA 91311.

Circle 244 on Inquiry Card

STEPPING MOTOR ADVANCE FOR DOT MATRIX PRINTER

Dot matrix printer DX486 has stepping motor that improves control of paper advancement and makes it well suited to such graphics as UPC code. Std 7 x 5 or 7 x 7 dot matrix characters are 0.11″ (2.8 mm) high. Justification is either right or left. Printing is on std paper and ribbon drive reverses automatically. The 12-V dc motor is 5-V TTL controlled and all control inputs are made via a rear mounted connector. **Amperex Electronics Corp, Hicksville Div,** 230 Duffy Ave, Hicksville, NY 11802.

Circle 245 on Inquiry Card

ADD-IN MEMORY AND MEMORY CONTROLLER

For use in Honeywell Series 60, Level 6 computers, PINCOMM H6 memory modules provide 64k bytes of storage capacity on a single card and are offered in either 18-bit parity or 22-bit error detection and correction version. Memories are form, fit, and function equivalent to Honeywell high density "Memory Pac." Modules install on top of memory control cards into connectors provided for that purpose. MCH6 memory controller is also offered in parity and EDAC versions. **Trendata Corp**, Standard Memories Div, 3400 W Segerstrom Ave, Santa Ana, CA 92704.

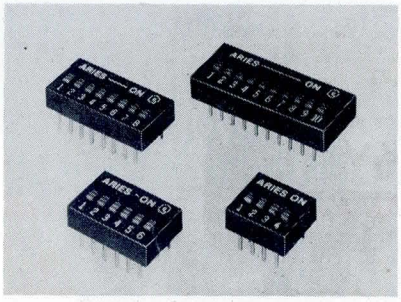
Circle 246 on Inquiry Card

CONTIGUOUS BAND MULTIPLEXERS

Available with up to 7 sections/channel, 2- to 5-channel multiplexers achieve tight performance specs in the 50- to 1500-MHz range. The multiplexers are 0.1-dB ripple Chebyschev designs, with the housing milled from a single block of aluminum for package integrity and mechanical stability. A typical triplexer would have passbands of 100 to 200, 200 to 400, and 400 to 1000 MHz. The upper section can be either a bandpass or lowpass filter. Units have typ insertion loss of 0.2 to 0.3 dB, with crossover insertion loss of $\lesssim$5.0 dB for operating temperatures from −20 to 50 °C. **Telonic Berkeley**, 2825 Laguna Canyon Rd, Laguna Beach, CA 92652.

Circle 247 on Inquiry Card

DIP SWITCHES



Spst 4-, 6-, 8-, and 10-position DIP switches have self cleaning 10 μm gold plated contacts for low contact resistance throughout switch lifetime, or 10k operations/position. Pins are sealed to prevent contamination during soldering. Op temp range is −20 to 80 °C. Severe vibration tests show no mechanical damage or electrical discontinuities. **Aries Electronics, Inc,** PO Box 130, Frenchtown, NJ 08825.

Circle 248 on Inquiry Card

HARD DISC CONTROLLER AND MAGNETIC TAPE COUPLER

Low power, quad size DQ202 (LSI-11) or DU202 (PDP-11) controllers and DQ130 (PDP-11) couplers plug into one slot of CPU. Controllers run DEC RP software supported by RT-11/RSX-11/RSTS operating systems and interface any 2 hard disc drives with SMD interface having capacities of 8M to 160M bytes. Couplers emulate TM-11, are RT-11/RT-11/RSX-11/RSTS compatible with software or switch selectable density control, and interface up to 8 dual-density (NRZI/PE) formatted magnetic tape drives. **DILOG (Distributed Logic Corp),** 12800-G Garden Grove Blvd, Garden Grove, CA 92643.

Circle 249 on Inquiry Card

MULTIPLE PRINTER CONTROLLER

Microprocessor based VIP-201 multiple-printer controller PC board plugs into a single slot of any Data General minicomputer. It controls three independent line printers, any mix of Dataproducts or Centronics interface compatible printers, or Teletype model 40 printer. With the latter, line driving capability is up to 2000 ft (610 m) via its SSI interface. The controller is fully compatible with Data General RDOS. Integral self tests provide thorough line printer subsystem diagnostics. **Vetra Systems Corp,** PO Box 714, Melville, NY 11746.

Circle 250 on Inquiry Card

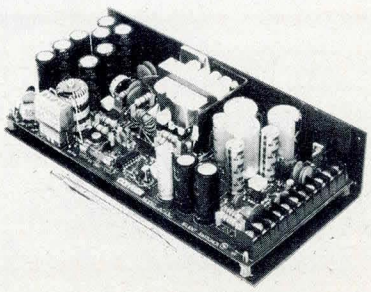
GRAPHICS ADAPTER BOARD

Interfacing Printronix printer/plotters with Tektronix 4025 raster terminal, board produces up to 6 high resolution hard copies on plain paper. Technology of adapter, which allows 2 raster CRT terminal devices to be served automatically and efficiently, provides for multiplexing of CRT data with no waste of CPU time. Built-in self-test is selected using a switch on the module, making it easy to check both graphics and character printing. Self-test mode prints 132 col of 96-char ASCII data, and plots 132 diagonal lines. **Trilog, Inc**, 17391 Murphy Ave, Irvine, CA 92714.

Circle 251 on Inquiry Card

130-W MULTI-OUTPUT SWITCHING POWER SUPPLY

Model AC-130 has 200-W pk output capability and is completely compatible with Boschert OL-130, providing wider input voltage tolerance (80 to 140 V/160 to 264 V), tighter output voltage regulation, and higher pk power capability. Outputs are ±5 V, ±3%, 15 A; 12 V, ±5%, −4 A; −12 V, ±5%, −2 A; and −5 V, ±5%, −1.0 A. Output voltage tolerances cover variations from all causes. Std features include adjustable, built-in power-fail signal. **Conver Corp,** 10629 Bandley Dr, Cupertino, CA 95014.



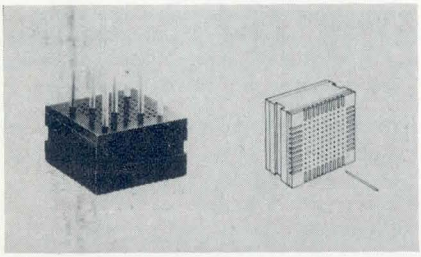
Circle 252 on Inquiry Card

SINGLE-BOARD MAGNETIC TAPE CONTROLLER

Unibus compatible interface UCI connects the company's series 40 formatted mag tape transports to DEC PDP-11 minicomputers. It emulates the DEC TM-11 and is compatible with standard software. It offers dual-density NRZI/phase encoded operation without software modification. Interface supports 9-track 800-bit/in (315/cm) NRZI, 9-track 1600-bit/in (630/cm) phase encoded, and dual-density 800/1600-bit/in operation. Tape speeds from 12.5 to 75 in (31.8 to 191 cm)/s can be used. Device is mounted on single modified quad-board and plugs into any small peripheral controller slot in PDP-11 units. **Digi-Data Corp,** 8580 Dorsey Run Rd, Jessup, Md 20794.

Circle 253 on Inquiry Card

MINIATURE MATRIX PINBOARDS



Pinboards measure 0.64 x 0.70″ (16.3 x 17.8 mm) for 5 x 5, and 1.14 x 1.2″ (29 x 3.1 mm) for 10 x 10 matrices and provide manual programming facilities in minimum space in PC board applications. I/O terminals are on 0.100″ (2.5-mm) centers; units can be wave-soldered in place. Pinboards extend only 0.23″ (5.8 mm) above PC board after mounting. Gold-over-nickel contact system is rated at 125 V and 2 A non-switching and has less than 125-mΩ contact resistance. **AMP Inc,** Harrisburg, PA 17105.

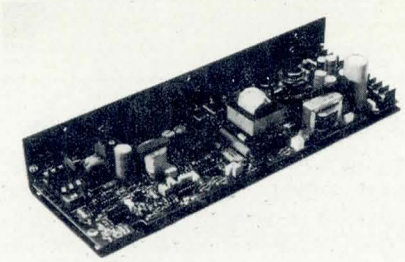
Circle 254 on Inquiry Card

SINGLE-INLINE RESISTOR NETWORKS

I-SIP networks feature triple-strength leads that are "wrinkled," soldered, and sealed in a solid ceramic body. Three package profiles and 11 package styles provide packaging heights of 0.200, 0.250, and 0.350″ (5.08, 6.35, and 8.89 mm), and pin choices of 6, 8, and 10 pins with 0.100″ (2.54-mm) lead spacing. Large design area permits a larger number of resistors, higher power ratings, and resistor values from 22 Ω to 1 MΩ, with a tolerance of ±2%. Networks meet MIL-R-83401 requirements and have an operating temp range of −55 to 125 °C. **Allen-Bradley Co, Electronics Div,** 1201 S Second St, Milwaukee, WI 53204.

Circle 255 on Inquiry Card

OPEN FRAME SWITCHING POWER SUPPLIES



Available in 8 std models and custom designs at ratings of 50 to 65 W, Etatech series units supply primary outputs of 5 V at up to 8 A; ±15 V and −12 to −15 V at up to 12 W; 5 to 15 V, either polarity, at up to 18 W, and substrate bias at up to 0.25 W. Regulation on primary output is ±15 mV line and 10 mV load to 10% to full load. Input voltage range is 85 to 135 Vrms, 47 to 440 Hz, single-phase, or 115 to 185 V. **Adtech Power,** 1621 S Sinclair St, Anaheim, CA 92806.

Circle 256 on Inquiry Card

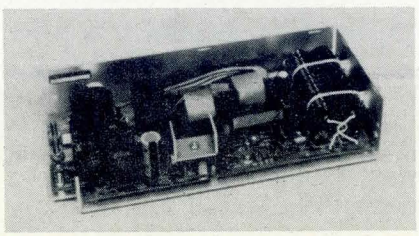
PROTOCOL CONVERTER

Printer interface for IBM System 34, model PQ protocol converter directly connects to the system via twinaxial cable. Converter output permits selection of any RS-232 quality printer. It emulates the 5256 printer, has internal device address select switches, automatically converts EBCDIC to ASCII for the standard graphic characters, and supports special control character strings. **Expandor Inc,** 400 Sainte Claire Plaza, Pittsburgh, PA 15241.

Circle 257 on Inquiry Card

SWITCHING POWER SUPPLIES

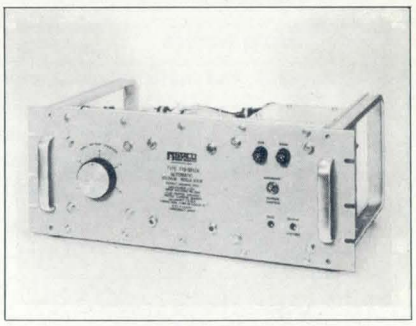
Open frame, switching, regulated power supply series ES-J measures 12 x 4.88 x 2.75″ (30.5 x 12.4 x 7 cm) and comes in six models: 5 V at 45 A, 12 V at 22 A, 15 V at 18 A, 24 V at 12 A, 28 V at 10 A, and 36 V at 8 A. Dual inputs of 85 to 132 and 170 to 264 Vac provide brownout protection. Other protective circuits include overvoltage, overload, shorts, reverse polarity, and soft start. Monolithic chip contains all regulation, modulation, and protective circuitry. MTBF exceeds 50k hours. **Power/Mate Corp,** 514 S River St, Hackensack, NJ 07601.



Circle 258 on Inquiry Card

CORRECTING VOLTAGE REGULATOR

Proprietary IC control network within regulator compensates for line voltage fluctuations, yielding performance suitable for sensitive electronic circuits. Distortion free regulators can withstand short current overloads up to 10 times their continuous duty rating. Units for 120-V lines are rated at 50 or 70 A with a 0.25% regulation tolerance, and at 25 and 37.5 A with a 0.5% tolerance. For 240-V lines, units are rated at 20, 37.5, 40, and 80 A with a 25% regulation tolerance, and at 10 or 18.8 A with 0.5% tolerance. **Staco Energy Products Co,** 301 Gaddis Blvd, Dayton, OH 45403.



Circle 259 on Inquiry Card

LITERATURE

Keyboards and Switch Modules

Catalog describes 3 x 4 and 4 x 4 keyboards with 0.5 or 0.75″ button centers and flange or post mounting, as well as snap dome contact and long, wipe contact pushbutton switch modules. **Grayhill, Inc**, La Grange, Ill.

Circle 300 on Inquiry Card

Digital Thermometers

Series 2160A and 2170A digital thermocouple readout meters are profiled in full color bulletin that includes general, environmental, and accuracy specs, electrical data, options, and common accessories. **Omega Engineering, Inc**, Stamford, Conn.

Circle 301 on Inquiry Card

Switching Power Supplies

Catalog and applications handbook lists common and mechanical/electrical specs and describes performance characteristics of ac-dc and dc-dc switching, linear open frame, and ferroresonant power supplies. **Acme Electric Corp**, Cuba, NY.

Circle 302 on Inquiry Card

Electronic Packaging System

Modular hardware packaging system 2^2M is announced in pamphlet which presents its components, quick assembly and disassembly characteristics, and customizing possibilities. **Protronix, Inc**, Minneapolis, Minn.

Circle 303 on Inquiry Card

Ceramic Capacitors

Containing technical information on line of monolithic, disc and high voltage ceramic capacitors, 32-p catalog includes mechanical and environmental performance specs. **Murata Corp of America**, Marietta, Ga.

Circle 304 on Inquiry Card

Microcomputer Reliability Program

Detailed in illustrated brochure are 5 stages of program for LSI-11: design analysis, design qualification, production qualification, process control, and field performance. **Digital Equipment Corp**, Marlboro, Mass.

Circle 305 on Inquiry Card

24- and 48-Bit Computer Software

Directory featuring more than 150 different software items for independent evaluation is presented in 80-p booklet. Write to: Marketing Communications Dept, **Harris Computer Systems**, 2101 W Cypress Creek Rd, Ft Lauderdale, FL 33309.

All Purpose EMI Filters

Photos, dimensional drawings, and specs are presented in catalog describing 8 series of filters that meet national and international requirements. **Cornell-Dubilier Electronics**, Newark, NJ.

Circle 306 on Inquiry Card

Fans and Blowers

Color catalog presents complete line of tubeaxial and open fans and blowers with air capacities of from 22 to 560 ft^3/min, together with specs, photos, dimensional drawings, and sound level graphs. **Howard Industries**, Milford, Ill.

Circle 307 on Inquiry Card

Incremental Optical Encoders

Configurations by quanta/revolution, angular resolution (arc seconds), power requirements (milliamps), and max operating speed for DIGISEC^R RI__/35(C) series are outlined in 2-p data sheet. **Itek Measurement Systems Div**, Newton, Mass.

Circle 308 on Inquiry Card

Microcomputer Analog I/O Systems

Engineering manual specifies performance, dimensions, and usage of more than 100 products, and includes applications section with tutorial articles. **Data Translation**, Natick, Mass.

Circle 309 on Inquiry Card

Cooling Power Supplies

Note describes how user can remove heat from power supply to improve supply (and system) reliability and MTBF; included are graphs, figures, and charts. **Boschert Inc**, Sunnyvale, Calif.

Circle 310 on Inquiry Card

Hardware for Industrial Environments

Illustrated brochure details increase in mechanical and electrical integrity and environmental tolerances to temperature, humidity, vibration, and contaminants of 180+ CPU, memory and I/O modules, and controllers. **Xycom**, Ann Arbor, Mich.

Circle 311 on Inquiry Card

Large Scale General Purpose Computers

Aided by charts and photos, 72-p brochure provides summary description of application products, models, database formats and structures, communications/networking software, languages, and utilities for DPS 8 line, **Honeywell**, Waltham, Mass.

Circle 312 on Inquiry Card

Printed Circuit Pin and Socket Connectors

Featuring configurations of from 10 through 120 high precision contacts with low insertion forces and super density hard gold plating finish, pamphlet incorporates photos, charts, and diagrams. **Continental Connector Corp**, Woodside, NY.

Circle 313 on Inquiry Card

Data Acquisition Components And Subsystems

Tutorial sections, data sheets, specs, and application information are included in 1000-p catalog detailing data conversion and signal conditioning products, op amps, linear test systems, and power supplies. **Analog Devices**, Norwood, Mass.

Circle 314 on Inquiry Card

High Reliability Capability

Illustrated 18-p brochure and 22 x 30″ wall chart are used to describe commitment, approach, manufacturing flows, assessment and enhancement, and Government program participation with regard to Hi-Rel. Available, by letterhead request only, from **Harris Semiconductor**, Dept 53-035, PO Box 883, Melbourne, FL 32901.

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SUBJECT INDEX

DATA INPUT/OUTPUT

DATA TRANSMISSION

DEBUGGING

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DESIGN

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DIGITAL CONTROL AND AUTOMATION

DIGITAL TO ANALOG CONVERSION

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EMITTER COUPLED LOGIC

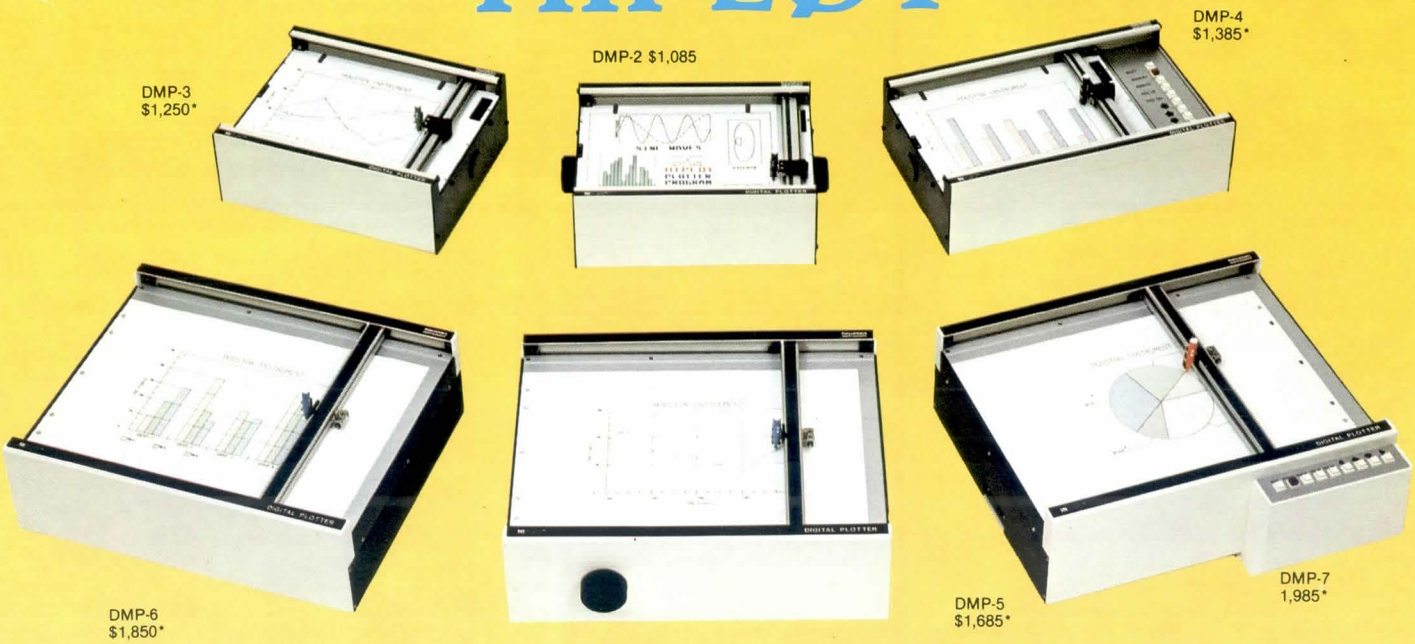
ENCODING, DATA

See **DATA ENCODING AND FORMATS**

ENGINEERING STANDARDS

AUTHOR INDEX

Look what's happened to HIPLØT™



It's grown into a complete family of quality low cost digital plotters

*Yes, they are UL listed!***

In just two short years, the HIPLØT has become the most popular digital plotter among small systems users. With a record like that, what can we do for an encore? WE'VE INTRODUCED A COMPLETE LINE OF HIPLØTS...with a model suited for just about every plotting application.

The HIPLØT DMP Series is a new family of digital plotters with both "standard" and "intelligent" models available with surface areas of 8½" x 11" (DIN A4) and 11" x 17" (DIN A3). For the user needing a basic reliable plotter, we have the "old standard" DMP-2 (8½" x 11") and the "new standard" DMP-5 (11" x 17"). For those needing a little more capability, there are the DMP-3 (8½" x 11") and the DMP-6 (11" x 17")—both microprocessor controlled and providing easy remote positioning of the X and Y axes (perfect for the OEM). For those who want this intelligence plus the convenience of front panel electronic controls, we've provided the DMP-4 (8½" x 11") and the DMP-7 (11" x 17").

The "standard" plotters come complete with an RS-232-C and a parallel interface. The "intelligent" DMP plotters accept data from either an RS-232-C or Centronics data source. For the "standard" plotters, software is available from our ever expanding "Micrographic Users Group." The "intelligent" HIPLØTs use our exclusive DM/PL™ language which minimizes plot software to a fraction of that normally associated wth digital plotting.

With the new DMP Series, high quality digital plotting can now be a part of your system. It just doesn't make sense to be without this valuable tool when there is a DMP plotter with the plot size, speed and capabilities that are exactly tailored to your specific needs...and your budget.

Prices for the DMP series range from $1,085* to $1,985*.

For complete information contact Houston Instrument. One Houston Square, Austin, Texas 78753. (512) 837-2820. For rush literature requests, outside Texas call toll free 1-800-531-5205. For technical information ask for operator #5. In Europe contact Houston Instrument, Rochesterlaan 6, 8240 Gistel, Belgium. Telephone 059/27-74-45.

houston instrument
GRAPHICS DIVISION OF
BAUSCH & LOMB

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*U.S. suggested retail prices only.
**DMP 2, 3 and 4 UL listed
DMP 5, 6 and 7 UL listing pending

Circle Number 103 for Literature. **Circle 104 to have a Representative call**

Use the microprocessor you like.

Some card manufacturers would have you believe you must use the Z80 microprocessor if you want the 'simple-to-design' STD BUS system. Not true.

Pro-Log builds 8085, Z80 & 6800 CPU cards.

Our STD 7000 CPU cards feature the three most popular microprocessors. But we don't force them on you. All our peripheral cards work with any 8-bit microprocessor you choose. And they're all totally unbundled, so you can buy one card or the whole system.

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We build them to our own high standards.

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