

Hal Alles on:  
Trade-offs in  
simulation

# COMPUTER DESIGN

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and Design  
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

## Mixed-signal board designers resist the siren call of simulation

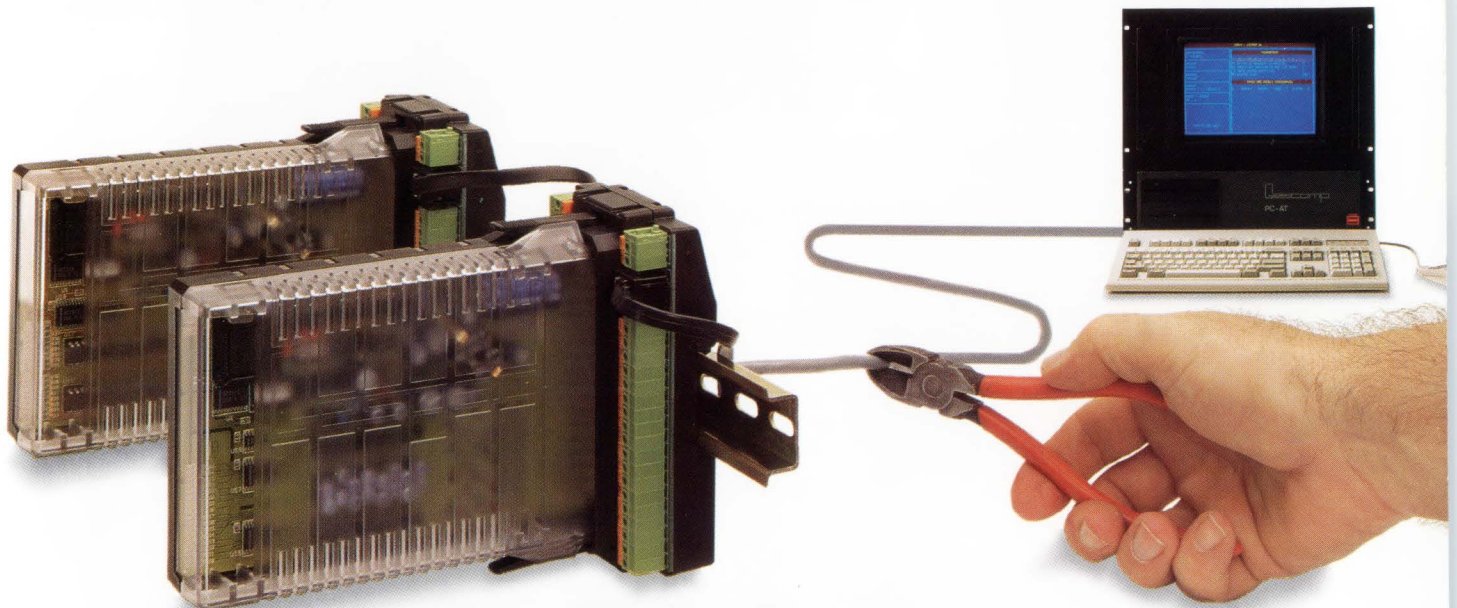
Real-time multiprocessing  
pushes software limits

Designers look beyond DIPs  
to meet application needs





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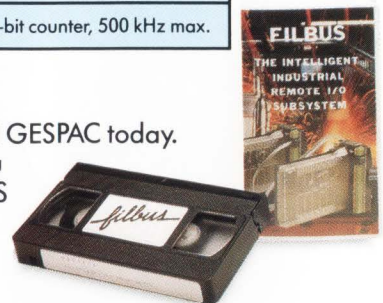
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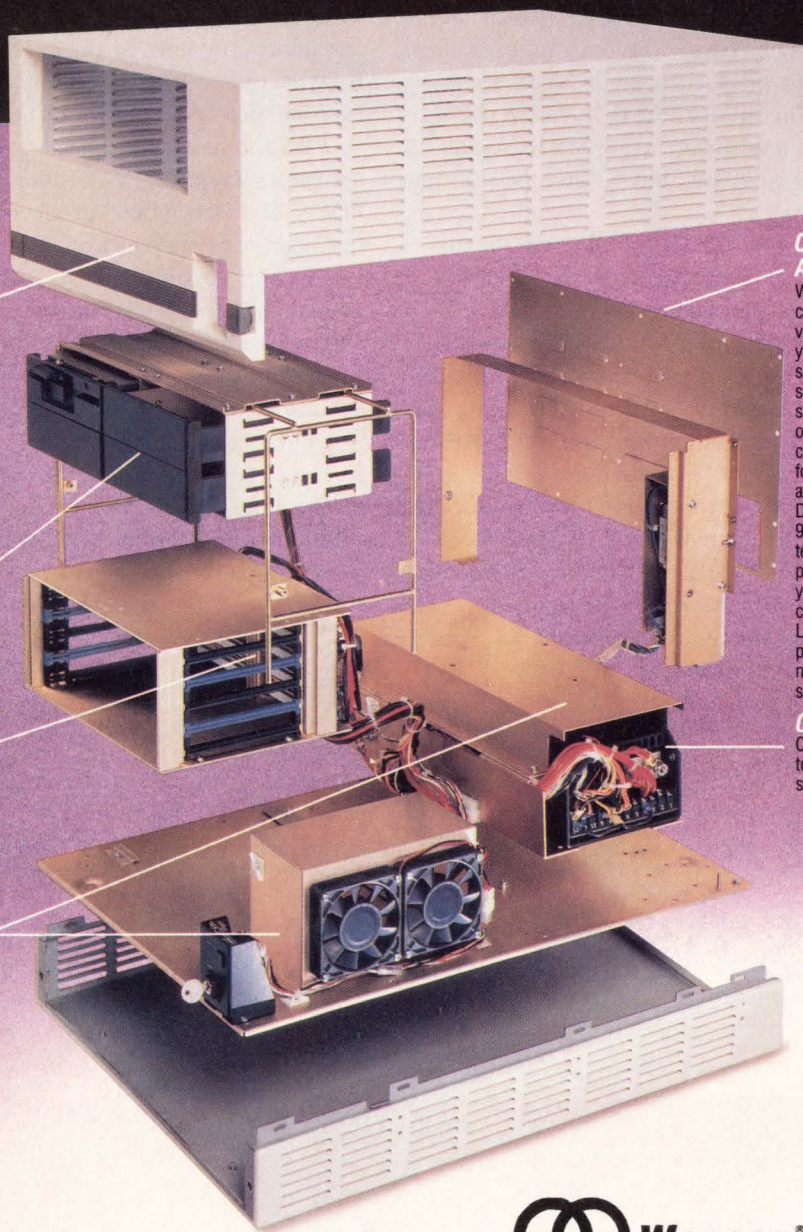
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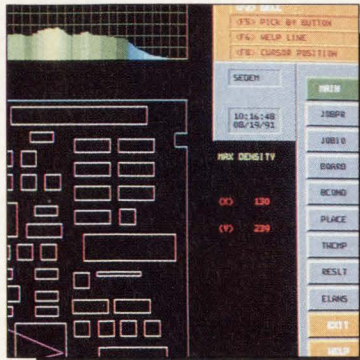


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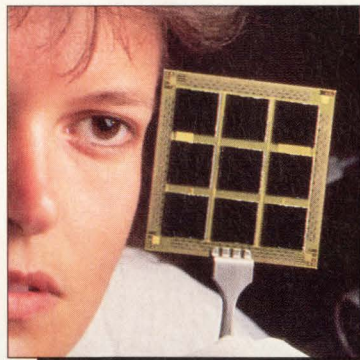
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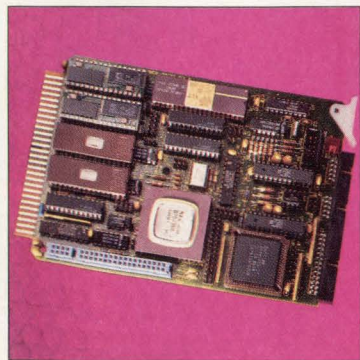
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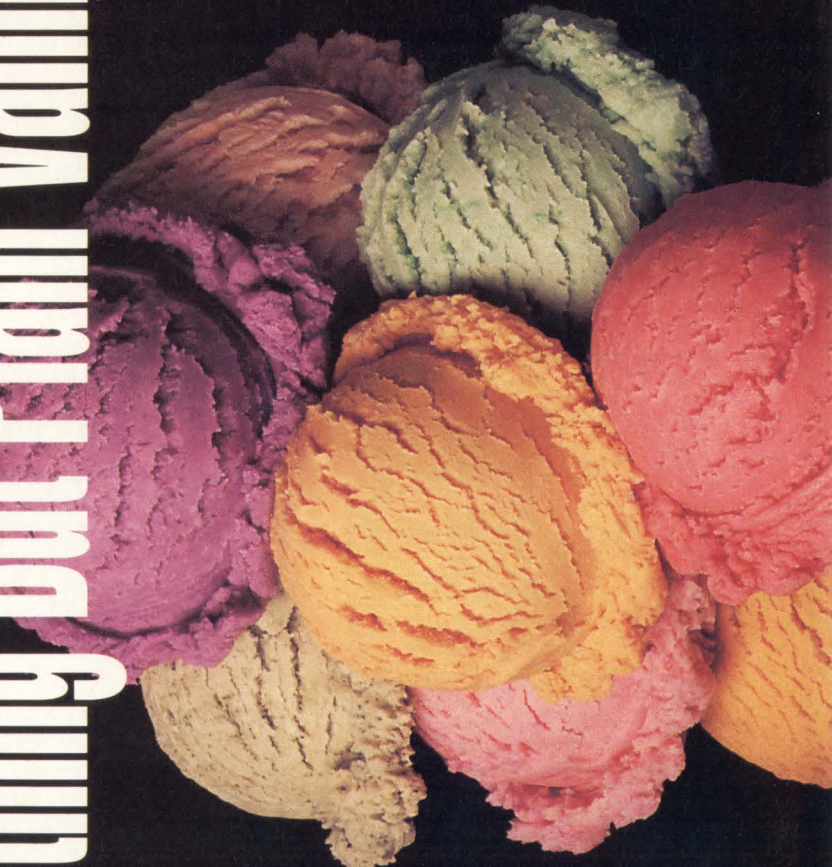
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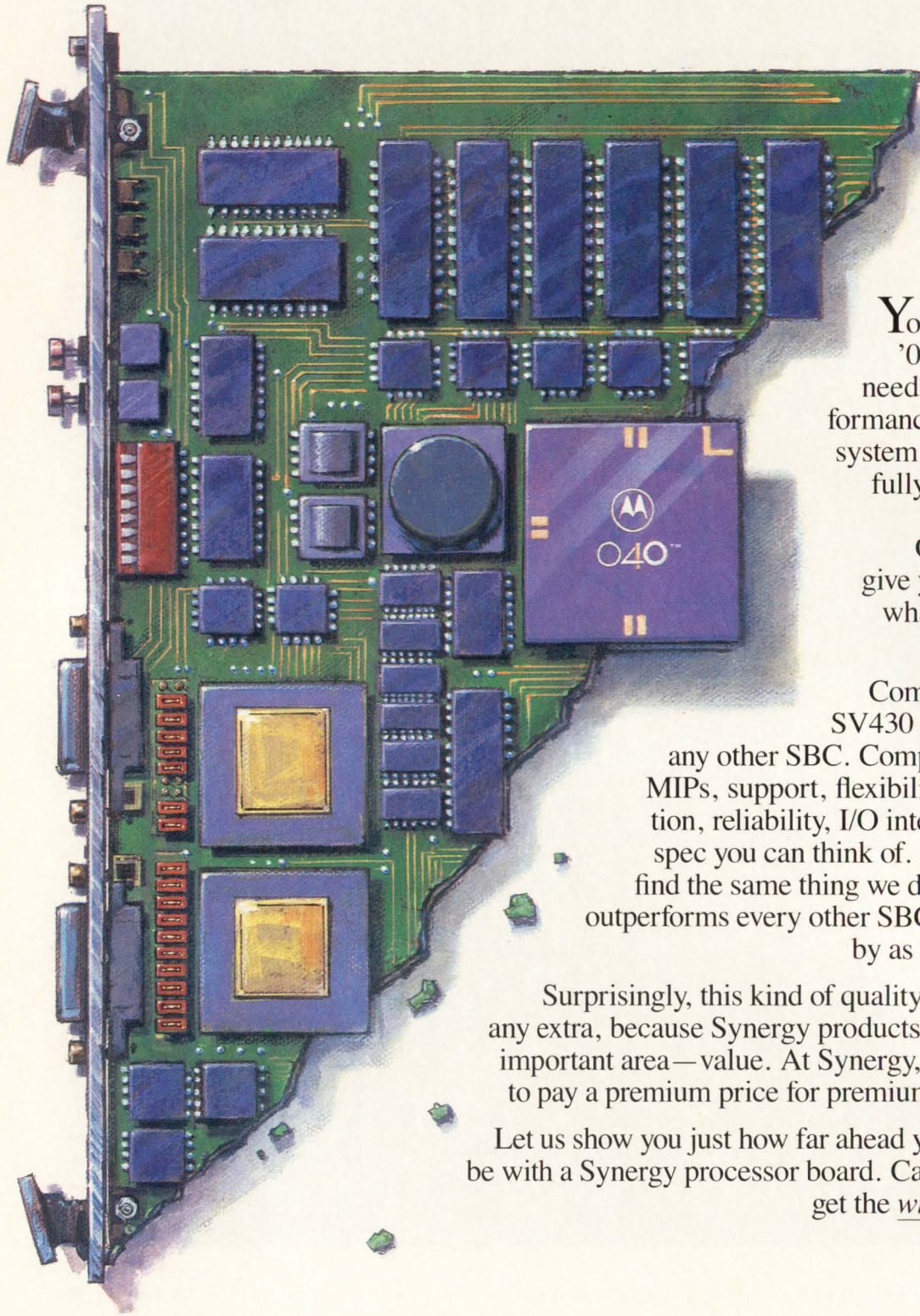
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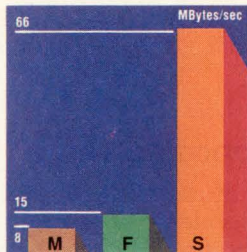
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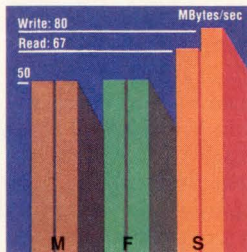
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### VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison.

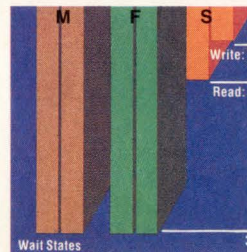
Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



### DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 performance you're gaining. SV430 bursts are 26% faster than Force and Motorola.

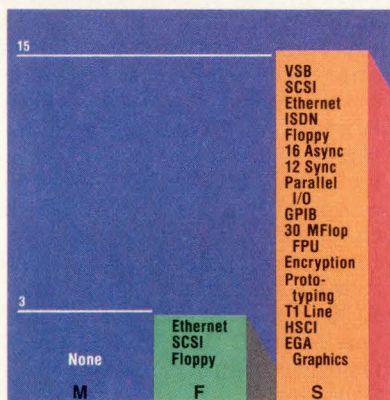
ance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



### DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66% faster than Force or Motorola, it supports twice the on-board memory—32 MB.

faster than Force or Motorola, it supports twice the on-board memory—32 MB.

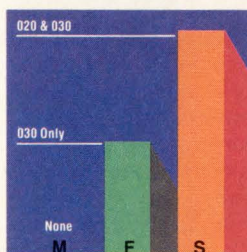


### I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

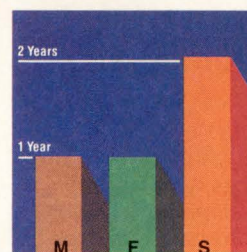
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### '020/'030 Compatibility

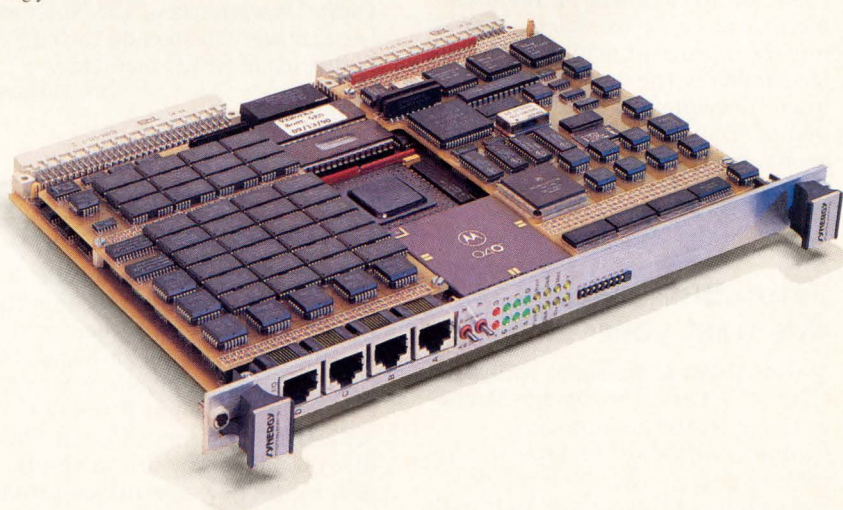
Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and

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### Product Warranty

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CIRCLE NO. 5



## Multibus II becomes an EISA PC

Launched at Buscon, the \$5,500 33-MHz 486DX EISA-based PC-compatible Multibus II board from Intel represents a strategic change in direction for the Hillsboro, OR-based board maker. Sources close to Intel disclose that all future Multibus II CPU boards from the division will be based on a PC architecture. The reason? Inexpensive PC chip sets make it the only cost-effective route to take for Multibus II CPU design. In other EISA developments, look for Texas Instruments (Dallas, TX) to give Opti (Santa Clara, CA) a run for its money when TI samples the TACT84500 four-chip EISA chip set in December. Price of the TI chips is claimed to be \$130 versus \$150 for the Opti solution.

—Dave Wilson

## A new multimedia chip

While debuting its Cornerturn 2-D VME-based image-processing board at Buscon, Array Microsystems (Colorado Springs, CO) revealed that a joint development effort with Samsung (San Jose, CA) is expected to result in a multimedia processor sometime next year. Although Array Microsystems representatives were reluctant to comment on the architecture of the device, it's possible it may be a programmable MIMD device similar to the device currently under development at Texas Instruments' (Dallas, TX) multimedia research operation.

—Dave Wilson

## Futurebus+ silicon due next year

National Semiconductor (Santa Clara, CA) and Newbridge Microsystems (Kanata, Ontario, Canada) will jointly adapt, manufacture and market Newbridge's Futurebus+ protocol and datapath controller ICs. The products, dubbed the CA91C896 and CA91C897 by Newbridge and DS3805 and DS3815 by National, are expected early in 1992. New-

bridge plans to use the devices in the development of a range of wide area network products.

—Dave Wilson

## Group establishes benchmarks for NFS performance

First it was Whetstones, then Dhrystones, then we discovered X-Stones. Now, we've got Nhfstones—benchmark measurements for the performance of network servers using the network file system (NFS) developed by Sun Microsystems (Mountain View, CA). A consortium calling itself the LADDIS Group (after the first initials of its founding companies) has submitted the benchmark to the Systems Performance Evaluation Cooperative (SPEC).

Nhfstones measure the number of I/O operations/s from the outside of a server system. The benchmark program is designed to characterize real-world workloads in a software engineering environment, not just read/write operations on a server. The Nhfstone benchmark is derived from work done in the SunOS environment which focused on a single-client operation; the new version is designed to measure multiple-client operations. Currently running on Data General, Sun and Digital workstations, the Nhfstone benchmark will soon be ported to all platforms of SPEC members.

—Tom Williams

## Apple/IBM deal may add to Unix GUI confusion

Among the rumors confirmed at the media non-event marking the final signing of the agreement between Apple Computer (Cupertino, CA) and IBM (Armonk, NY) was the one surrounding Unix—or AIX, IBM's version of Unix. The line is that IBM will contribute its AIX to the new operating system effort and Apple will supply its Macintosh user interface technology. Oh boy! Yet another graphical user interface integrated with Unix to confound those already

torn between the Open Look and OSF/Motif implementations of X-Windows! The only way this arrangement can make sense is if Apple is prepared to bring existing Macintosh software into the new OS environment by making it possible to recompile and run them under the operating system that is, after all, to be named PowerOpen. And even then, when the thing is ready a couple of years from now, there will be many more Unix/X-Window applications that will not run.

—Tom Williams

## In the opposing camp

Meanwhile, Microsoft (Redmond, WA) demonstrated a pre-release version of its New Technology (NT) operating system at the rollout of the MIPS R4000 RISC processor, which is to be the backbone of the ACE (Advanced Computing Environment) effort. The NT operating system lets existing applications written for MS-Windows 3.0 run in a simulation mode on an R4000-based ACE system, in which case they should perform comparably to an 80386-based machine. Or, Windows applications can be recompiled to native R4000 code and run much faster. The ACE effort also includes a Unix version from The Santa Cruz Operation which features the OSF/Motif-based Open Desktop environment. Despite the continued hoopla, ACE shows the greatest promise of bringing along huge numbers of existing applications and win whatever war Apple and IBM think they are fighting.

—Tom Williams

## 386 vendors wage low-power struggle

As Advanced Micro Devices (Sunnyvale, CA), Chips & Technologies (San Jose, CA) and Intel (Folsom, CA) quarrel over the 386 market in the United States, a new player across the Pacific has decided to join the fray. VM Tech-

*Continued on page 10*



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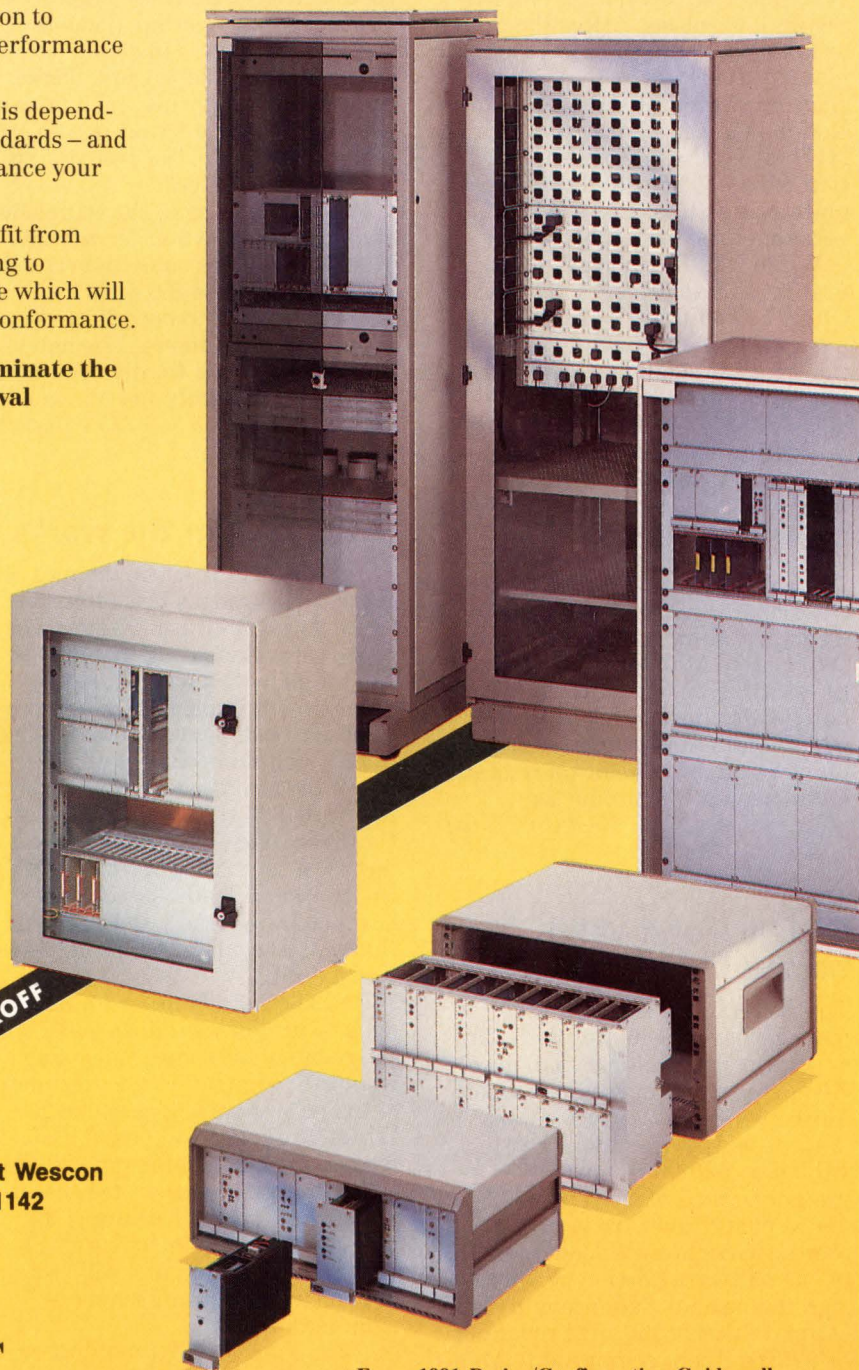
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*Continued from page 8*

nology (Tsukuba, Japan) reportedly plans to put its 386SX clone on the market by Christmas, and it hopes to claim new territory in the 386 war with an extra low-voltage chip in the near future.

Responding to the trend towards portable, battery-powered systems, VM Technology is focusing on low voltage. After the standard 386SX clone, the company plans to come out with a 3-V version. According to VM, the 3-V version is being designed to run at 10 MHz, at  $\frac{1}{3}$  the power consumption of Intel's 386SX. Their ultimate goal is to create a 2-V version of the 386, they claim.

While VM Technology is the first to talk about a 2-V 386, AMD, Chips & Technologies and Intel have all had low-power consumption on their agendas. For AMD's part, power consumption is reduced due to the fact that its 386 processors have static cores that let the CPU current be reduced to zero, without losing data, by halting the processor clock. Chips' 386 provides for power-management through software with its Superstate operating mode. Intel takes a roughly similar approach with the System Management Mode in its 386SL chip. Chips & Technology also has said that its 386 will operate at 3 V and reportedly plans to qualify one or more of its foundries for 3-V production.

—Jeffrey Child

## Cadence and Valid tie the knot

The incredible shrinking EDA market just got smaller with Cadence Design Systems (San Jose, CA) penning an agreement to acquire rival Valid Logic Systems (San Jose, CA) in a stock swap valued at \$200 million. The merger immediately vaults Cadence past former frontrunner Mentor Graphics (Wilsonville, OR) in the software portion of the design tool arena. Cadence and Valid estimate their combined revenues at \$390 million, compared to Mentor's software sales of \$177 mil-

lion. The remainder of Mentor's \$435 million in revenue is in design hardware, a market in which neither Cadence nor Valid compete.

Though at first blush the deal seems like a match made in heaven (Cadence is strong in IC tools, Valid in PCB and system design), the merger will undoubtedly raise a lot of concerns in the newly combined customer base. In areas where there's product overlap, Cadence and Valid will have to decide which tool to market and support. This could signal a difficult and time-consuming transition for users who are painfully aware of the ever-ticking time-to-market clock.

For the short run, the confusion generated by the merger will give Mentor Graphics some time to sell its Falcon release 8.0 tools as a unified solution to both IC and system design customers. The much-delayed Falcon is finally beginning to ship—apparently not a moment too soon.

—Mike Donlin

## SSBLT chip in the works

The ink is barely dry on the idea of source-synchronous block transfer (SSBLT) capability on VMEbus but reports are circulating that at least one company has a chip under development implementing the protocol. It's been broadly rumored that Force Computers (Campbell, CA), one of the strongest proponents of the SSBLT in the VFEA (VME-to-Futurebus Extended Architecture) technical committee of VITA (VME International Trade Association), has a chip well under development that will implement both VME64 as well as SSBLT.

It's expected the new chip will debut with Force's anticipated Sparc-based 2E board. While Force wouldn't comment on the exact date of the new board's release, the 28-Mips CPU board will probably surface at—or before—Buscon 92/West in February. It's anticipated that it will include all the features of its precursor, the 1E, including SCSI and Ethernet ports, and will probably include a Force Flexi mezzanine connector.

—Warren Andrews

## Multibus III?

Multibus II has been steadily chugging along, picking up a few major contracts along the way, including some major European telecommunications companies as well as being selected to be the brains behind a new ZIP-code mail sorter for the U.S. Postal Service. But like STD and VME, Multibus II is starting to show its age (the initial protocol was put together in the early 1980s) and may be in line for a face lift. To forge ahead and satisfy some telecommunications companies' needs, the Multibus Manufacturers Group (MMG) put together a technique giving the bus complete live insertion capability. This was demonstrated at Buscon 91/East in Washington, DC.

The group has also been making noise about speeding up the transfer rate of the bus. A recent die shrink of the message-passing coprocessor lets that part operate comfortably at twice the speed of earlier versions. By swapping the bus drivers and including some faster—but still inexpensive off-the-shelf devices—the MMG has demonstrated it can increase bus transfer rates at least 50 percent, and perhaps 100 percent.

Will the next step be an expansion to 64 bits? It's already rumored that if the connector mechanics are opened up as a possible discussion area for a "next rev" of the specification, it could prove to be a whole new can of worms. Connector companies are battling out new connector designs, some favoring a 2-mm connector, others a 2.5-mm spacing. It's been reported that Seimens, one of the major supporters of Multibus II, favors a 2.5-mm spacing on a new connector—a format not supported by a number of U.S. connector makers. It's been suggested that rather than go through this problem with Multibus II, the committee should decide on an entire new specification—Multibus III?

—Warren Andrews





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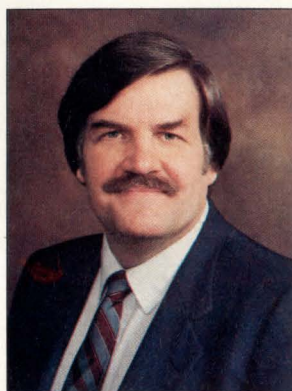
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**February will be bubbling with our technical programs**



**John C. Miklosz**  
Associate Publisher/  
Editor-in-Chief

## It's going to be hot in February

**A** few issues back, I brought you up to date on some of the things *Computer Design* was doing in the realm of conferences and exhibitions. Another update is called for now because a lot has happened since then.

As many of you know, *Computer Design* has had, for some time, a close association with Conference Management Corporation (CMC) and the Buscon shows it stages. Under the guidance of Warren Andrews, our senior editor for computers, computer subsystems, bus architectures, and board-level products, we recently assumed full responsibility for organizing the technical programs for both Buscon/East and Buscon/West. And since we don't like to do anything in a small way at *Computer Design*, we reached an agreement with CMC to undertake a major expansion in the size and scope of the technical program. In addition to the full-day Futurebus+ Seminar to be held February 3, the day before Buscon/92-West opens in Long Beach, the technical program will offer 66 individual sessions (six four-hour tutorials and 60 one-hour lectures) from which to choose. It's a block-buster program on design, bus architectures, real-time software, programming, and applications for anyone working with backplane-based systems.

If that wasn't enough to get February off to a hot start, we also came up with SysComp—The First OEM Systems/Subsystems Conference and Exposition—scheduled for February 18-20 in San Jose. The focus of SysComp's technical program (in the able hands of John Mayer with whom you're familiar through his outstanding work on our News Edition) is on the larger OEM integration issues: the evaluation and selection of microprocessor and bus architectures, system software, power supplies, mass storage, displays and user interfaces, as well as EMI/RFI, thermal management, design for manufacturability, concurrent engineering, and management of the hardware/software development and integration process. In essence, we've positioned SysComp somewhere between a low-level component show like Wescon and an end-user computer show like Comdex. Actually, there's never been anything like SysComp. For more details, see the SysComp Call for Papers on page 113.

And if both Buscon/92-West and SysComp weren't enough to keep February bubbling, we came up with still another first—RISC'92, the First International Conference on the Design of RISC-based Systems. To make everyone's lives a little easier, however, RISC'92 is being held in conjunction with SysComp. The technical program for RISC'92, which will run February 18-20 in San Jose—the same days as the SysComp technical program—is being coordinated by Andrew Wilson (yes, Andy is senior editor Dave Wilson's brother). RISC'92 doesn't need much elaboration beyond pointing out that it will focus on all the issues related to the design and development, of both the hardware and the software, of RISC-based products. You'll find more details in the RISC'92 Call for Papers on page 132.



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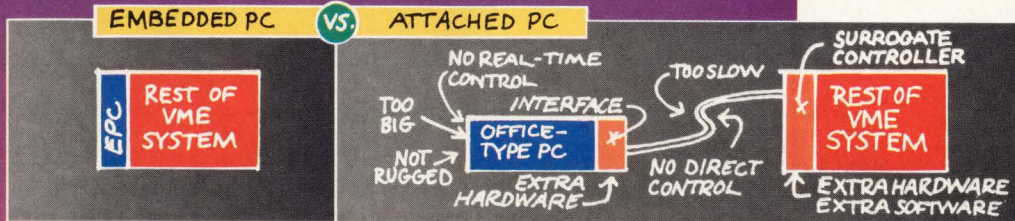
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Advanced Technology Group  
Dr. Morris R. Levitt, Senior Vice-President  
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One Technology Park Drive  
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CALENDAR

CONFERENCES

November 19 - 21

WESCON

Moscone Convention Center, San Francisco, CA. More than 45,000 are expected to attend the 40th annual WESCON conference and exhibition. Exhibits, technical sessions, short courses, and several special events will be featured during the three-day conference. There will be sessions on design, test and production engineering focusing on semiconductors, EDA tools and board-level components; test and measurement sessions; and manufacturing sessions on materials and supplies. There will be a special conference on exploring business opportunities in Eastern Europe. Information: Electronic Conventions Management, 8110 Airport Blvd, Los Angeles, CA 90045, (800) 877-2668, fax (213) 641-5117.



Circle 367

November 19 - 21

AFCEA Hawaii

Sheraton Waikiki Hotel, Honolulu, Hawaii. The sixth annual AFCEA Pacific international defense electronics conference and exhibition provides an opportunity for discussions between military and



industry leaders from the United States and the Pacific region. The conference will be in four parts: Pacific Defense Electronics Acquisition Day, Maritime Day, Land-Air Battle Day, and Joint International Day. Information: Beth Blose, Spargo & Associates, 4400 Fair Lakes Ct, Fairfax, VA 22033, (703) 361-6200 or (800) 336-4583, fax (703) 818-9177.

Circle 368

December 3 - 5

Technology 2001

San Jose Convention Center, San Jose, CA. Technology 2001, the second national technology transfer conference and exhibition, focuses on the latest advances in computer technology and software engineering, as well as electronics, materials, manufacturing technology, and biotechnology. Sponsored by NASA, the Technology Utilization Foundation, and NASA Tech Briefs, the conference will feature 50,000 ft<sup>2</sup> of exhibits and over 120 technical presentations. Information: Joseph Pramberger, NASA Tech Briefs, 41 East 42nd St, Suite 921, New York, NY 10017, (212) 490-3999.

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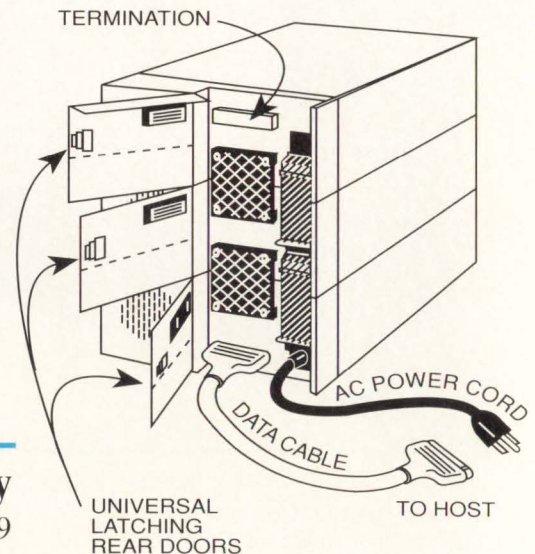
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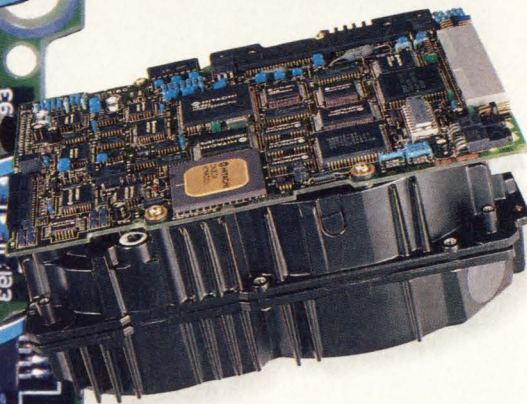
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# Hal Alles on: Trade-offs in simulation

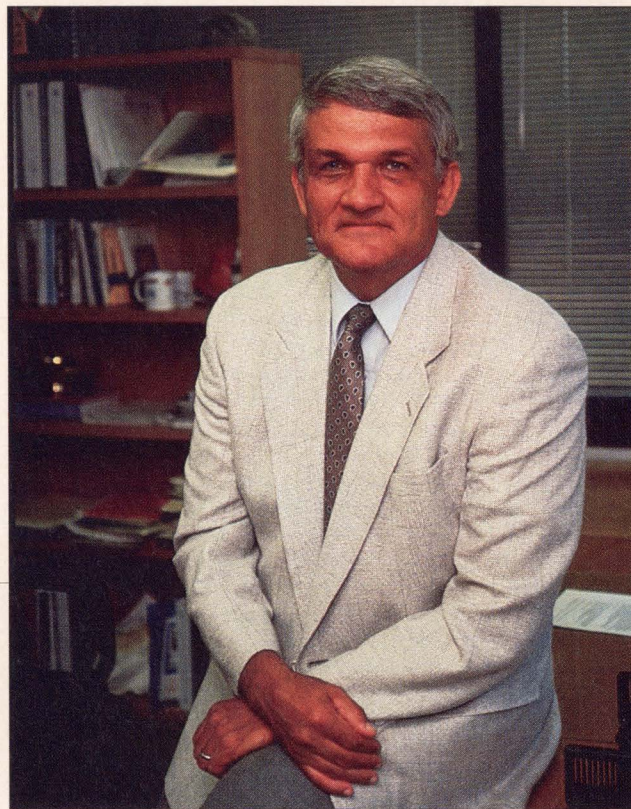
**S**imulation and verification products are rapidly evolving as numerous technological, economic and market conditions combine to overtax current products. In fact, the simulation and verification step is becoming the bottleneck in the process of bringing new electronic products to market. While vendors of EDA and computers can make up much of the gap, designers must also become more involved in the application and execution of the products to meet complexity and time-to-market requirements.

## Needs growing twice as fast as capabilities

The bottleneck results from an expanding set of designer needs which simulation and verification products must address. Electronic products consistently incorporate more complexity, higher-performance components, integrated packaging, and mixed technology than their predecessors. Designers need a range of simulation technologies, including behavioral simulation using a hardware description language, structural simulation of register-transfer-level (RTL) and gate-level descriptions, and device-level simulation such as Spice-like analog or switch simulation to manage these enhancements. In addition, vector-independent timing analysis tools are becoming essential as logic synthesis drives up complexity and small geometries and high frequencies boost the effect of physical interconnects on system performance.

Test tools must also be included as part of the design process to verify the function and performance of each manufactured unit. Fault grading and automatic test generation are dependent on simulation technology and component models and must be part of a complete design solution.

Unfortunately, these simulation and verification products suffer from the relationship between the size of the problems and the capabilities of the available computing resources. Designers simulate electronic products using workstations, general-purpose computers and sometimes even specialized hardware. The amount of simulation that can be done is dependent on the performance of the currently available computing resources.



Because the capabilities of electronic technology double about every two years, designers are working on the next-generation products using CAE tools running on the current generation. With electronic technology growing at an exponential rate, the need for simulation and verification grows faster than the available computing power. Complex systems require more simulation for each cycle and more cycles must be simulated to verify the system. High-speed circuits, small device geometries, low-power active components, and integrated packaging require more extensive, accurate and time-consuming simulation.

In total, the need for simulation and verification is growing about twice as fast as available computer power. Designers can't complete this design process phase by simply buying more computers. Instead, they must understand the trade-offs in available simulation and verification products and apply them in a manner which best suits their design methodology.

## Abstractions determine trade-offs

Creators of simulation and verification products have an intimidating number of engineering trade-offs: speed, accuracy, detail, capacity, generality, design iteration time, ease of use, and others. The specific set of trade-offs that impact the simulation user depends on the simplifying assumptions or abstractions the simulator uses to model the system.

Spice-type simulators are generally regarded as the least abstract and most general (i.e., closest to "reality.") The models of active components, however, are still simplifications of real behavior. The more detail and accuracy that the simulator accepts in the models, the slower the simulation runs.

Spice simulators also have the nasty property that



simulation time grows exponentially as circuit size grows. This limits its practical application to circuits of "thousands" of active components. Experienced designers understand these Spice limitations and often "trick" the simulator into providing meaningful information. They work around the limitations.

Similarly, with simulators using higher levels of abstraction, designers need to understand their specific benefits and limitations and how to work around them. Digital simulators abstract the signal continuum of the analog world into a few states and strengths, and use simple models to resolve signal conflicts. They use these digital states to model the interaction between active function blocks. For example, a switch-level simulator uses a model for each active component in the design. The signals are abstracted, but the structure still has all of the original detail.

Gate- and RTL-level simulators abstract the detail to larger functional blocks, using the same abstraction for the digital signals between blocks. The function of the blocks are expressed by built-in primitives of the simulator or through a general-purpose language such as VHDL or C. With a good HDL such as VHDL, the designer can control the abstraction of the functional blocks as well as the "signals" that communicate between the blocks. A single simulation signal can represent a whole group of signals or a block of data, such as an Ethernet packet.

### Simulation demands balancing trade-offs

By using all these levels of abstraction, designers can improve the productivity of their simulation cycle. For example, simulation speed increases as the design becomes more abstract. Complex systems are easier to understand and verify. And the language description serves as input to design synthesis tools. Depending on how a designer takes advantage of the abstraction, simulation times can be reduced many orders of magnitude. However, several layers of detail may be lost, affecting resolution and accuracy.

When applying multiple levels of model and simulation abstraction, designers need to understand the trade-offs which can be made at each level. The current generation of digital simulators provides selectable modes which substantially affect simulation speed and often the behavior. Unit-delay, full-timing and timing-constraint-check modes, for example, may all be available in a single simulator. The simulation speed may be a factor of 10 faster for the unit-delay than for the full-timing mode with constraints. The simulation results,

however, may be functionally different between the two. To take advantage of the speed-up, the designer may have to use more constrained design techniques to get functional agreement between the modes.

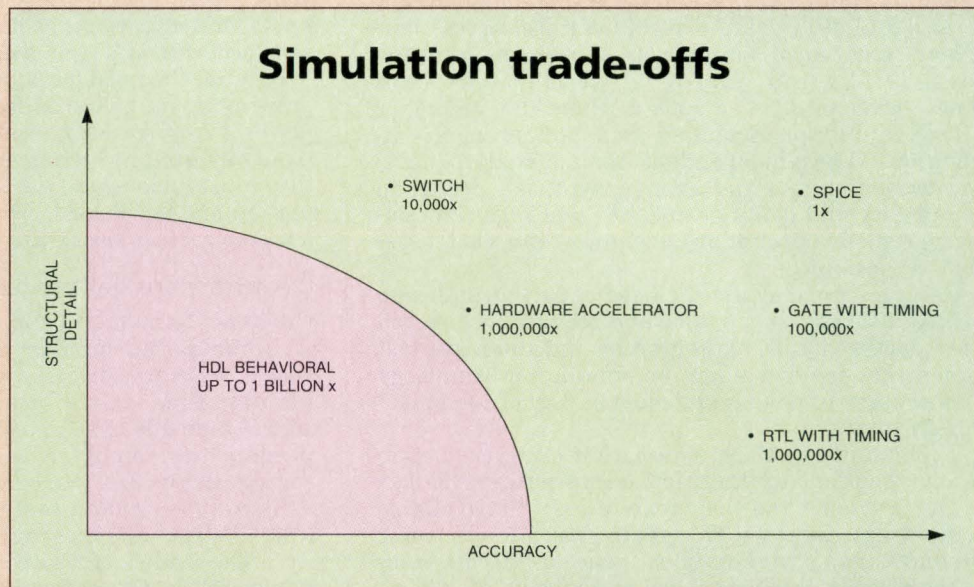
A simulator may also offer an option to trade pre-processing time for faster run time. A gate-level circuit, for example, can be processed into "levelized compiled code"—in effect, an abstracted behavioral model. These models can run significantly faster (10x) than their gate equivalents.

The availability of specialized hardware also adds to the diversity of simulation and verification solutions. Hardware accelerators, hardware modelers and emulators based on field-programmable gate array (FPGA) technology are all specifically designed for simulation and test application and more general-purpose parallel processor systems may also be applicable. For this specialized hardware, designers must be more concerned with the trade-off of speed versus cost, because the hardware typically accelerates only a certain level of abstraction.

### Designers make the full range of trade-offs

The top-down design methodology encouraged by VHDL and synthesis affects the way designers can best apply simulation and verification technology. Designers can use VHDL descriptions to verify all functionality without device-level detail. They can then use synthesis tools which naturally work with basic, straightforward gate-level abstractions, avoiding many of the tricks and pitfalls a traditional gate designer might use. Designers can direct synthesis tools to follow conservative design practices which make unit-delay simulation valid. They can then verify gate-level behavior with fast, abstracted, unit-delay simulation. Fault grading and test pattern generation also benefit from this simpler and faster abstraction.

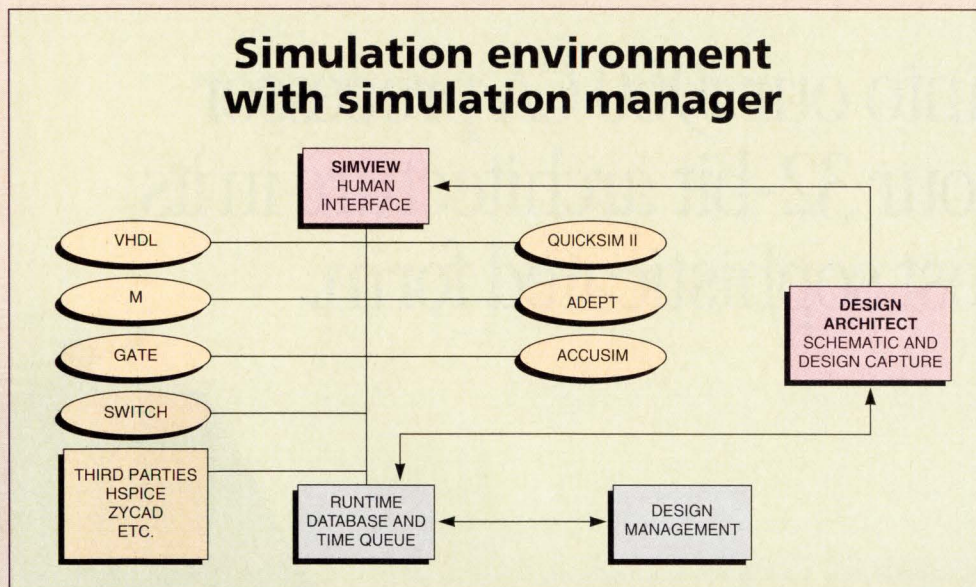
When designers use synthesis to produce a detailed gate design for a large ASIC, timing verification be-



An approximation of the trade-off between speed, accuracy and detail of several popular simulation techniques shows that the simulation speed of a high-level abstract model can be more than a billion times faster than a Spice simulation.



## Simulation environment with simulation manager



Mentor Graphics' Simulation environment, for example, includes a built-in simulation manager.

comes a more difficult problem. Since the designers don't create the gate-level design, it's difficult to identify the critical paths that limit performance. In addition, the interconnect parasitics of large ASIC designs dominate the performance. Designers need a tool which can search the design for critical timing paths that include the effects of the physical layout without the need for specific stimulation vectors.

Given the multitude of trade-offs in the top-down design process, designers need a complete range of consistent and interoperable sets of trade-offs to use concurrently. Within the top-down design methodology, designers use an HDL to help manage complexity by efficiently describing and verifying the functionality, yielding an executable specification. They then hierarchically decompose the design into component blocks with progressively more detail. They must verify each level of hierarchy with the appropriate degree of accuracy and detail. An IC design, for example, might require the following simulations: VHDL, RTL, gate, switch, and Spice.

### Unified simulation environments are essential

The design process is most efficient and effective if all of these simulations appear as a single simulator with the same human interface, stimulus, results analysis, database interface, and modeling techniques. In addition, all the simulators should be able to run at the same time, synchronized to a single time queue, freely exchanging signals in real (simulation) time. This gives designers the most flexibility to use the appropriate simulator for each part of the design at each stage of the design process. Designers can also get the best balance of simulation trade-offs and required simulation and verification performance.

System-level simulation and verification creates similar needs. High-frequency effects and packaging constraints along with mixed technology are making system-level simulation a necessity. Prototypes are too costly and time consuming, and don't produce accurate results. Most system-level simulations require the com-

bination and synchronization of many different kinds of simulation, including hardware models, hardware accelerators, behavioral and analog simulation. What's more, the availability of component models may force the use of two or more different simulators that basically do the same type of simulation.

The requirements of top-down design and system simulation point to the need for a unified simulation environment built upon simulation manager technology.

The simulation environment must provide a consistent human interface, database, model

technology and more, so that all of the simulation and verification tools have the same look and feel and the same interfaces to design data. The simulation manager couples multiple simulator kernels together at the signal exchange level and keeps time queues synchronized.

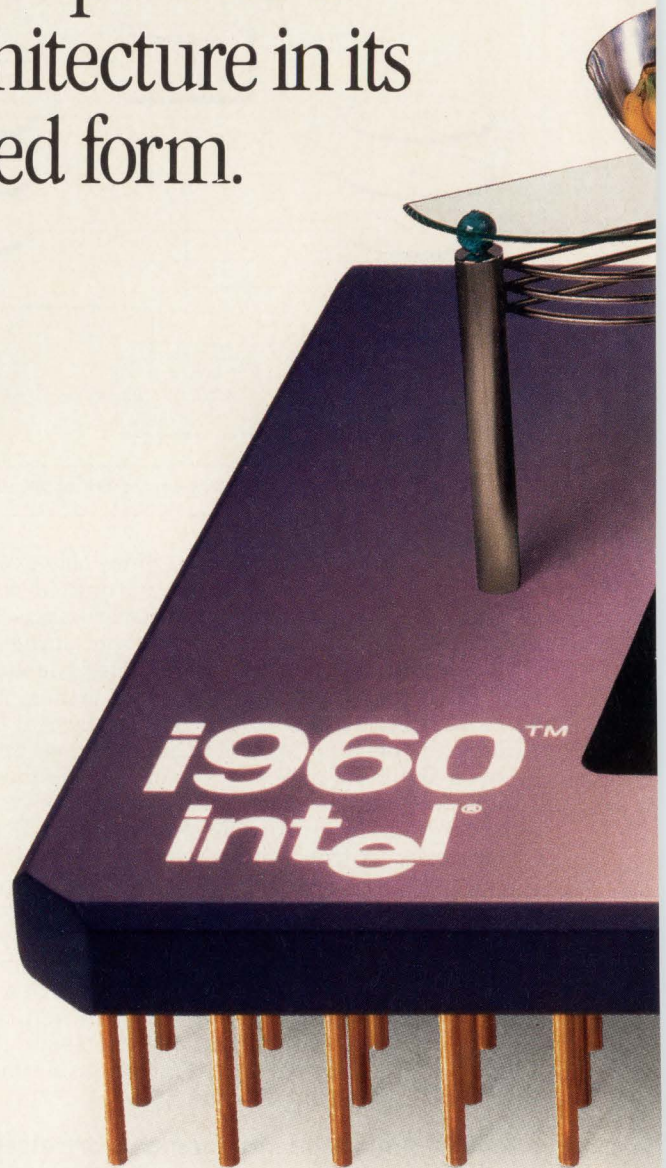
A well-designed and engineered simulation environment includes the most-used simulation types such as VHDL, gate, switch, and analog. It should also accommodate specialized hardware models and accelerators. In addition, the environment should support the easy integration of third-party and proprietary simulator technology. The ability to integrate other simulators provides a guarantee for non-obsolescence and protection of investment. Outdated or current simulators that will not continue to evolve can be integrated to preserve model investment. As new simulation techniques are needed or become available, they can be integrated without affecting previous investments.

The adoption of new tools is important because simulation and verification will continue to grow and change rapidly. As these changes occur, designers will need to learn more about different simulation trade-offs and how to use them effectively. A unified simulation environment and manager can give designers easy access to different simulation capabilities and ensure protection of past and future investments.

*Hal Alles is general manager of the simulation and test division at Mentor Graphics (Wilsonville, OR).*



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## Serial bus extension boosts VMEbus performance ten-fold

Warren Andrews, Senior Editor

In its infinite wisdom, the IEEE Microprocessor Standards Committee (MSC)—the group with final authority over bus standards—has insisted on the inclusion of a pair of pins reserved for a serial bus interconnection on most bus standards it has approved, including VMEbus. Originally intended for such things as board diagnostics, the serial pair has remained largely unused on most boards and systems. Now, a new approach uses these serial lines to transfer information at blazingly fast speeds, up to 400 Mbytes/s (3.2 Gbits/s). The technology, dubbed Autobahn by its developers at PEP Modular Computers (Pittsburgh, PA), is basically targeted at VMEbus, though company president Josef Kreidl says it's adaptable to other bus architectures.

Introduced last month at the 10th anniversary VMEbus celebration held in Munich, PEP announced the new technology and simultaneously released it into the public domain. This latter move opens the way for the technology to be adopted by the VMEbus community and ultimately, Kreidl believes, appended to the VMEbus specification. It's hoped the approach might even make it into Rev D (currently under consideration). Initial prototypes have been developed using a conventional VMEbus backplane, but Kreidl says a low-noise backplane would be desirable in applications where the maximum transfer rate will be used.

PEP's approach takes advantage of the serial clock (SERCLK) and serial data (SERDAT) lines detailed in the initial VMEbus specification. The technique takes advantage of the parallel bus as a traffic manager, but doesn't otherwise affect the standard VMEbus operation. In fact, it's completely compatible with existing IEEE 1014 VMEbus specifications as well as proposed extensions, including VME 64 and SSBLT (source synchronized block transfer).

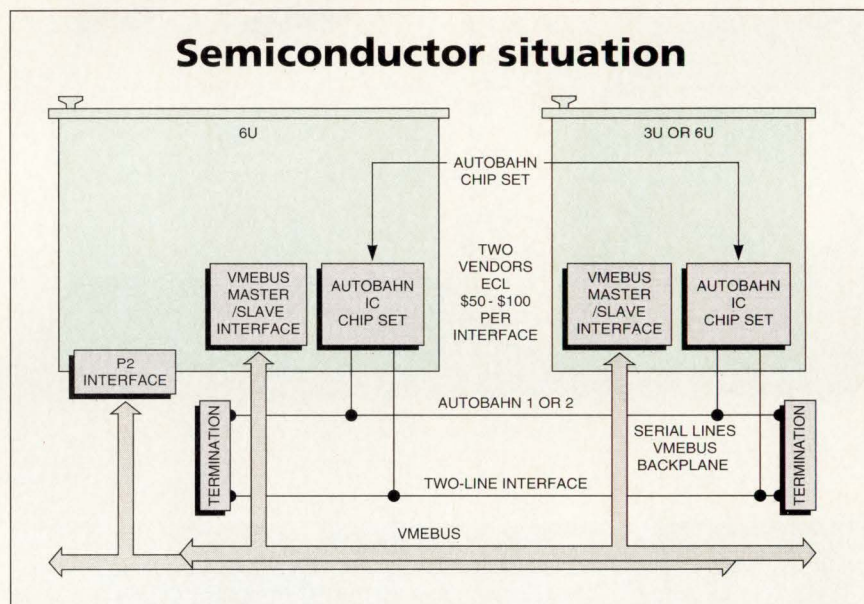
PEP envisions two versions of its Autobahn technology—the first, a discrete approach, is expected to appear as early as the first quarter of

1992 and offer 200-Mbyte/s transfers, and a monolithic version is expected to appear near the year's end. The approach is based on what Kreidl calls an "advanced, though mature technology," and takes advantage of Motorola's (Austin, TX) family of high-performance ECL parts. Initially, PEP felt it was nec-

will purchase chips directly from the semiconductor maker, not from PEP.

### Implementation

The first implementation, looking at speeds in the 200-Mbyte/s range, is a five-chip set. It consists of an ECL multiplexer/demultiplexer in a 28-pin PLCC and three SO-packaged logic chips (a PLL, a prescaler and a VCO). The fifth chip provides dc/dc conversions to let the 5-V supply operate the ECL devices. Kreidl says that the second version will provide a monolithic solution reducing the required board space and doubling



**PEP Modular Computers' Autobahn technology relies on a pair of seldom-used serial lines included in the VMEbus specification. The high-speed transfer rates are possible because of an ECL chip set which will originally be implemented as a five-part chip set in Motorola's ECL gate array, and later as a single custom chip. According to PEP, transfer rates up to 400 Mbytes/s will be possible at an incremental cost of between \$50 and \$100 per board.**

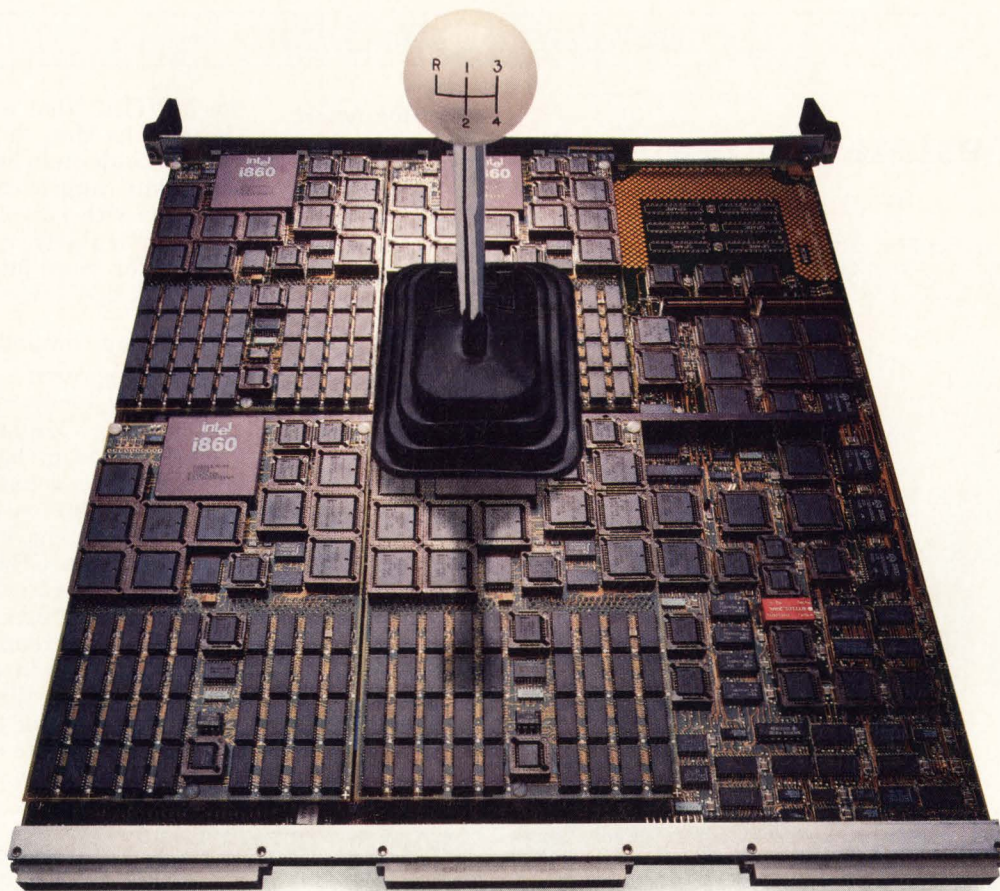
essary to use gallium-arsenide ICs, but switched to ECL because multipoint backplane noise problems couldn't be solved with GaAs.

"Not only does Motorola's ECL solve our technical problems," says Kreidl, "but it also offers a future migration path to higher levels of performance and the reality of second sourcing." Current designs are based around one of Motorola's ECL gate array families, and Kreidl reports that discussions are already underway with a second major semiconductor maker as a second source. Kreidl emphasized that customers

the data rate to 400 Mbyte/s. According to Kreidl, one of the major benefits of using the mature ECL technology is cost: in volume, the complete implementation is expected to cost between \$50 and \$100.

Prior to its formal introduction, Autobahn was paraded to a number of VMEbus makers as well as the VFEA (VME-to-Futurebus Extended Architecture) technical committee of VITA (VME International Trade Association). Early indications point to a favorable response by the committee. "This is one of those ideas," says Ray Alderman, technical direc-





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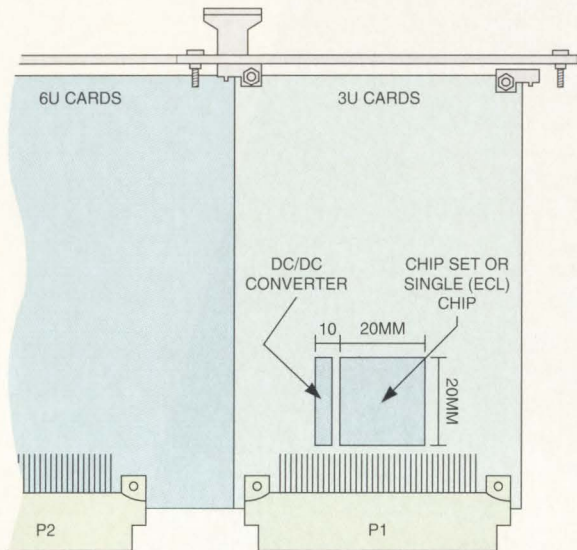
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## Real estate requirements



Both the chip set (containing one 28-pin PLCC and three SO packages) and the single-chip solution (expected later this year) are expected to take only a minimum amount of real estate—about 20 mm × 20 mm. An additional 10 mm × 20 mm will be required for the dc/dc converter needed to convert the VME systems' 5 V to ECL voltage levels.

tor of VITA, "that everyone's wondering why they didn't think of it sooner." Alderman believes that the Autobahn approach will provide VMEbus with a lot of added flexibility—particularly in applications calling for very fast transfers of large blocks of information.

### Backward compatible

The new approach is intended to be completely backward compatible with existing VMEbus cards, but the backplane will probably have to be modified. The values of capacitors and terminators on the serial lines (clock and data) have to be adjusted to accommodate GHz clock rates and ECL drive levels. In addition, the two lines can be configured conventionally (signal and ground) or as a differential pair for reduced noise levels. Other than that, the backplane remains the same, and the parallel system bus can operate unimpeded.

Data transfers over the serial bus

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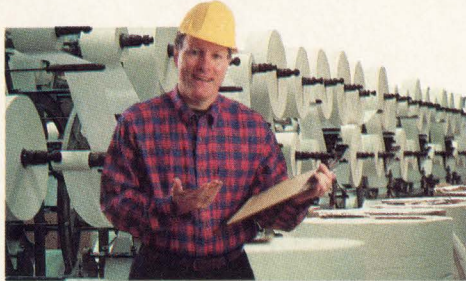
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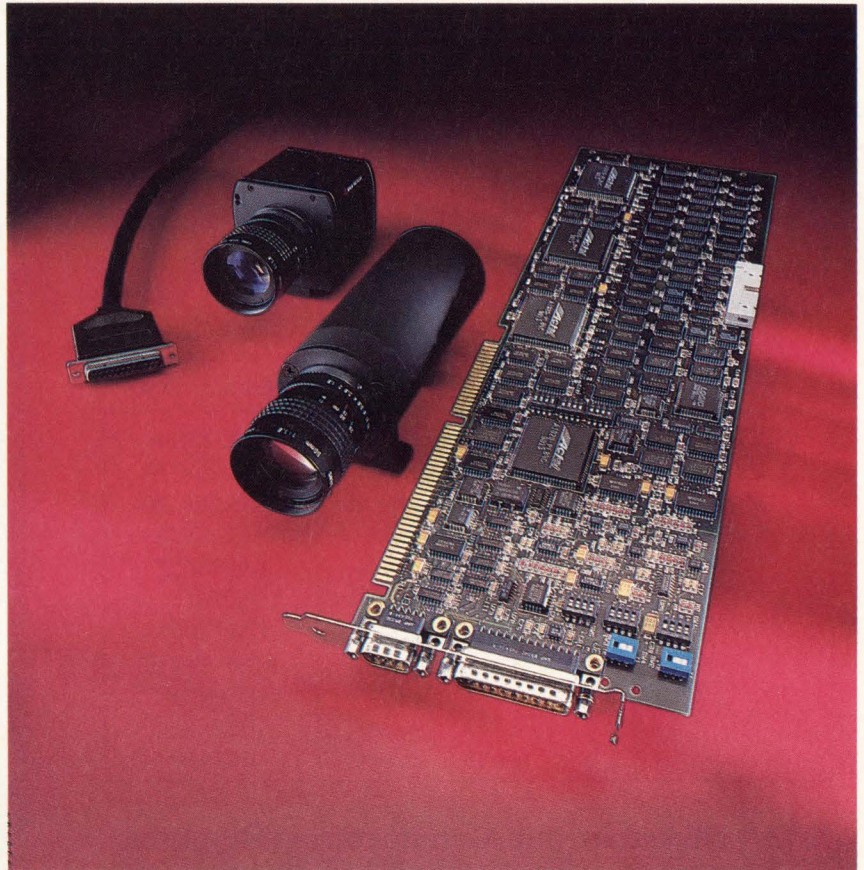
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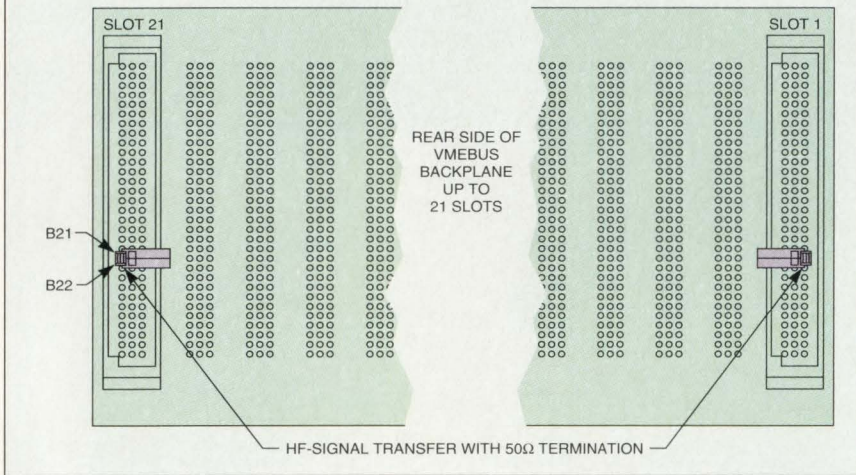
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### Backplane/signal transfer



*Though Autobahn has been tested using a conventional VMEbus backplane, it will require a somewhat modified backplane to provide maximum performance. It must have 50 Ω terminations and be designed to minimize attenuation, cross talk and RFI. It's also suggested that for maximum performance, a differential pair (rather than signal and ground) be used.*

are managed using the main system control lines. Proposed techniques call for an address modifier code to signal a serial transfer and the receiver address to be placed on the parallel bus address lines. This opens the connection for the serial transfer of a pre-specified period of time, leaving the parallel system bus free to continue its normal workload. Because the serial link communication time is specified, there's no need for additional logic for recognition of data collisions. Further, all arbitration is handled through the parallel system bus' arbitration circuitry.

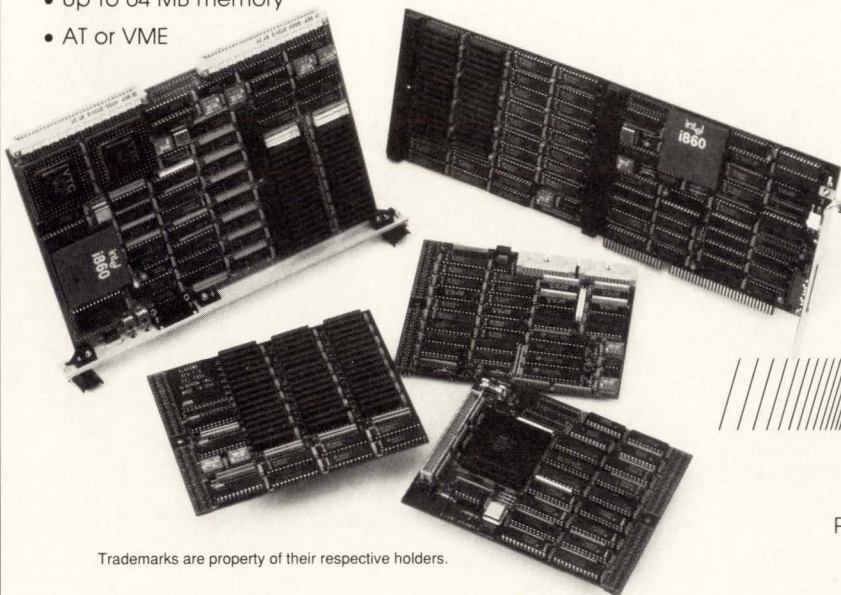
There are four possible methods for data transfer in the proposed Autobahn approach. First, the system can transfer only a single data word with corresponding data length and termination of the transfer via the normal VME DTACK signal on the VMEbus at the end of the cycle. Since Autobahn is a serial

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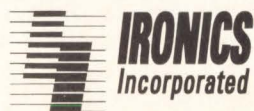
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link, data words may be specified of any length, and are not limited to either the 16- or 32-bit length normally associated with VMEbus. In fact, words can even be arbitrarily defined to be 64, 128, 256, or even as high as 1024 for specific applications.

The second transfer method involves the transfer of only one data word with corresponding data length, terminated via the standard VMEbus DTACK signal only in conjunction with specified address pipelining.

In addition to the two methods

of single word transfers, Autobahn provides for the transfer of data blocks with or without protocol. Block transfers without protocol require some additional logic. It calls for the start address, sent during connection time, to be reswitched by the recipient. The maximum block size is determined by the system at configuration time. The sender module can transfer data in any amount, limited only by the maximum block size. Data transfer runs as long as necessary, ended by a timeout which occurs when the system recognizes that no further data is on the line.

Transferring blocks of data with a protocol is accomplished very

**Besides two methods of single word transfers, Autobahn provides for the transfer of data blocks with or without protocol.**

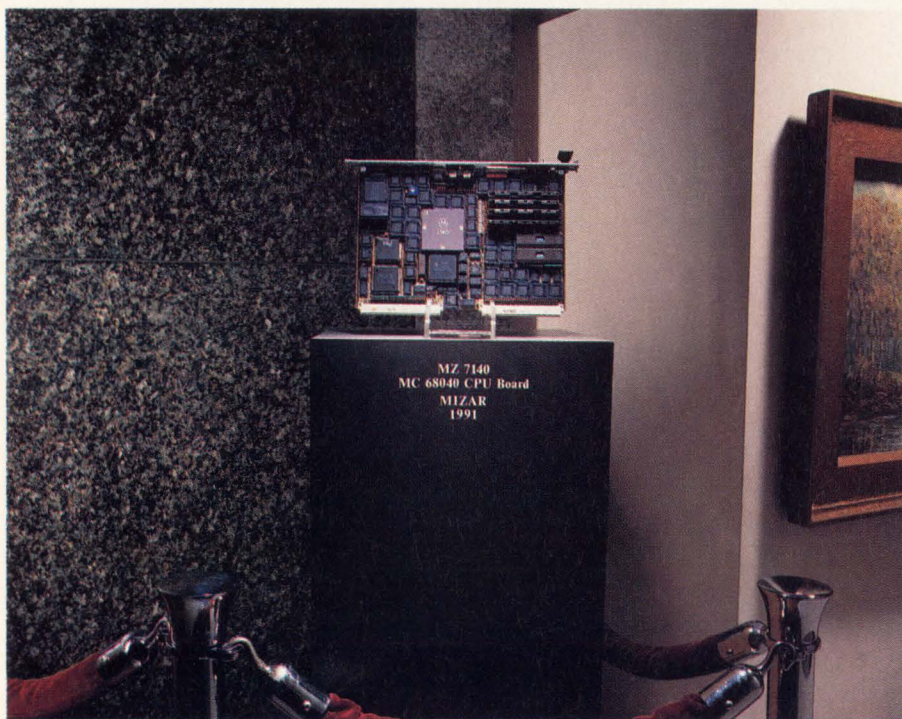


much the same as without, only all pertinent data for the transfer is reported to the receiving module first. This includes start address and block length. When the connection has been established, the parallel VMEbus is free, since block transfer occurs completely and solely on the serial bus.

Initially it's expected that Autobahn will find applications in high-speed telecommunications such as cellular telephone switches. With transfer rates in the 400-Mbytes/s range, however, there is a broad range of other applications which can benefit. For example, in graphics and imaging systems, large image files can be quickly moved from one processor to another. Similarly, high-performance peripherals could also benefit from the extremely fast transfer rates, as could redundant and fault-tolerant systems.

**Additional uses**

Though Autobahn may still be a ways off from being a complete specification—and part of IEEE 1014—there are also some other interesting uses for the serial bus. One is a sim-



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ple, high-speed bridge between technologies such as VMEbus and Futurebus+. But more importantly, Autobahn may take its place as the medium connecting multiple boards in massively parallel systems. The high-speed capability and independence from the system bus would let systems use Autobahn to provide transparent cache transfers on either a board-to-board or broadcast mode.

The serial bus, as defined by PEP, contains no costly overhead in terms of arbitration or contention logic, and isn't bogged down with a lot of software overhead in terms of transfer protocols. This provides the advantages of permitting very fast data transfers. The housekeeping is all maintained on the parallel system bus. It's therefore conceivable that applications requiring fast data transfer, such as graphics files or images, could use Autobahn as the main transfer bus and reserve the standard VMEbus for housekeeping and coordination between modules. ■

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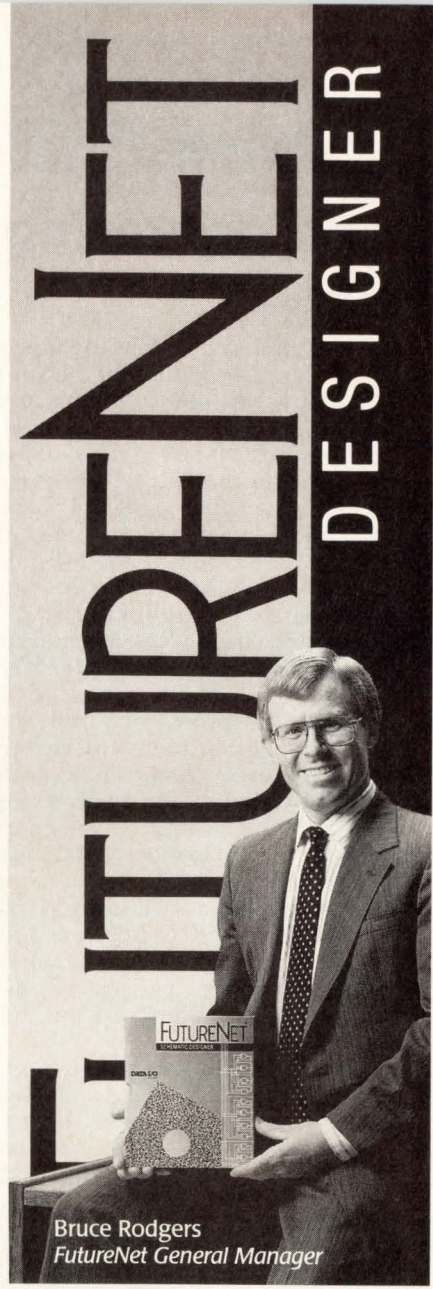
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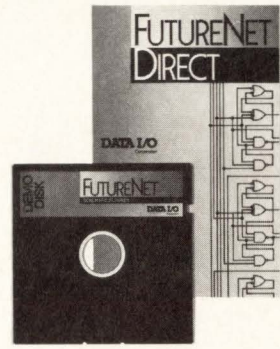
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# Now operating at three volts...

Dave Wilson, Senior Editor

The benefits of operating a processor at less than 5 V became obvious last month when Chips and Technologies (San Jose, CA) demonstrated the use of its 3- to 5-V PC/chip Intel-compatible processor in a next-generation personal portable computer that could run on AA batteries. This month, Intel (Santa Clara, CA) follows suit with some new processors also running at 3 V. But rather than address designers of 386 or 486 systems, Intel has chosen to debut three new members of its 80186/80C186 processor family instead. In addition to new peripherals, the processors have a new static CPU and a variety of power-saving modes, also of benefit to designers using the part in low-power applications. Aside from Intel, other vendors have 3-V processors in the wings too, both PC and non-PC compatible. And it won't be long before a lot more low-power micros, peripheral controllers and PC chip sets hit the streets.

The most highly integrated member of Intel's new microcontroller family is the new 80C186EC device. It sports four DMA channels, two serial channels, two interrupt con-

trollers, 22 input/output pins and four timers, in addition to standard 80C186 processor peripherals. As important as the variety of new on-chip peripherals are the power management modes that are offered. The "Idle" mode, for example, freezes the CPU clock while keeping peripherals active; the "Powerdown" mode freezes all internal clocks; while "Powersave" is a programmable internal clock divider that lets processes occur at a slower rate and hence, with lower power consumption. A second device, the 80C186EA, has both 3- and 5-V modes of operation in addition to the power-saving modes. Intel claims that applications using the 3-V EA version can run on two AA batteries with an 80 percent reduction in power when compared to the 80C186. Finally, the XL device is similar to the 80186, except that it operates at speeds up to 20 MHz.

With 3-V microcontrollers announced, it might seem an obvious next step for Intel to produce 3-V versions of its 386, 486 or some version of it like the 386SL. Intel phraseologists agree that migration towards 3-V systems is an "impor-

tant power consumption enabling technology." And Intel has publicly stated that it's planning "platform solutions" that will take advantage of 3.0-V microprocessors and DRAMs. But the company notes that over the next 18 months, it's "unlikely" that the industry will be able to implement full 3-V systems and that 3/5-V partitioning or hybrid implementations will be a "transition methodology" into full 3-V systems.

No one else thinks it will take 18 months. Certainly not Advanced Micro Devices (Austin, TX). The company disclosed its own 3-V 386 near the end of October. "Our new 25-MHz Am386DXLV and 20-MHz or 25-MHz SXLV are extended voltage 386 processors that will run between 3 and 5 V. We are a year ahead of Intel with these designs," brags Mike Webb, the director of marketing and system engineering for the personal computer products division at AMD. "This part has the same fully static design as the original Am386, so you can stop the whole CPU between keystrokes on a PC and still have full performance when you want it," he says.

Other microprocessor manufacturers are also working on 3-V processors. Motorola's (Austin, TX) MC68340, for example, (a member of its the H68300 family of microcon-

Low-Power Microcontrollers

	Modular Core	Speeds (MHz)	Input Levels	Clock Generator	Timer/Counters	Watch-dog Timer	Chip Select/Ready Logic	Chip Select Pins (max)	DMA Channels	Interrupt Control	Refresh Control Unit	Serial Channels (max)	I/O Pins (max)	Power	3 Volt	Test Mode
80186/80188		8	TTL	Yes	3		186-Style	13	2	Yes						
80C186/80C188		10, 12.5, 16	TTL	Yes	3		186-Style	13	2	Yes	Yes		Powersave			Yes
80C186XL/80C188XL	Yes	10, 12.5, 16, 20	TTL	Yes	3		186-Style	13	2	Yes	Yes		Powersave, Static			Yes
80C186EB/80C188EB	Yes	8, 13, 16	CMOS	Yes	3		Enhanced	10		Yes	Enhanced	2	16	Idle, Powerdown, Static		Yes
80C186EA/80C188EA	Yes	12.5, 16, 20	CMOS	Yes	3		186-Style	13	2	Yes	Yes		Powersave, Idle, Powerdown, Static			Yes
80L186EB/80L188EB	Yes	8	CMOS	Yes	3		Enhanced	10		Yes	Enhanced	2	16	Idle, Powerdown, Static	Yes	Yes
80L186EA/80L188EA	Yes	8	CMOS	Yes	3		186-Style	13	2	Yes	Yes		Powersave, Idle, Powerdown, Static	Yes	Yes	Yes
80C186EC/80C188EC	Yes	13, 16	CMOS	Yes	3	1	Enhanced	10	4	Yes	Enhanced	2	22	Powersave, Idle, Powerdown, Static		Yes

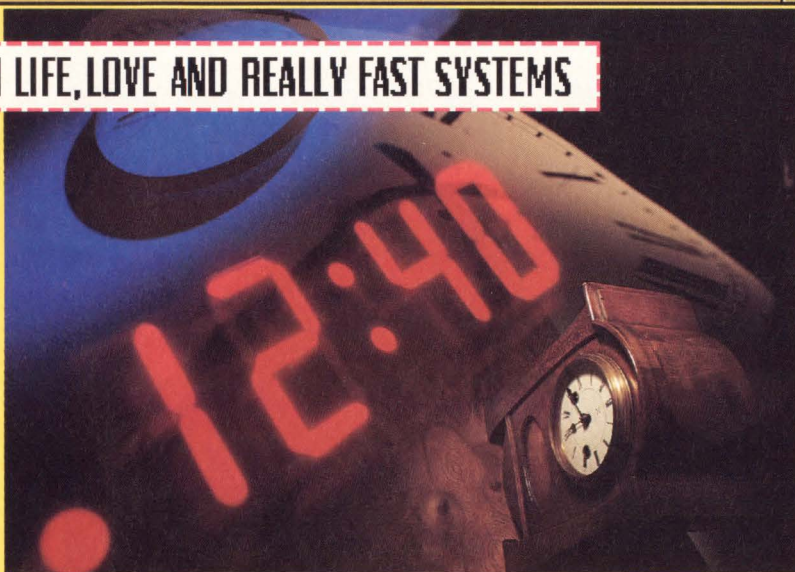
Adding to the line of 80186 microcontrollers are the EC, EA and XL devices. Not only do some of the processors in the 80186 family offer low-power modes, they also sport 3-V operation.



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Editorial contributions: Tim Wilhelm, Luis Pineda, Ali Mesri and Cynthia Jones.

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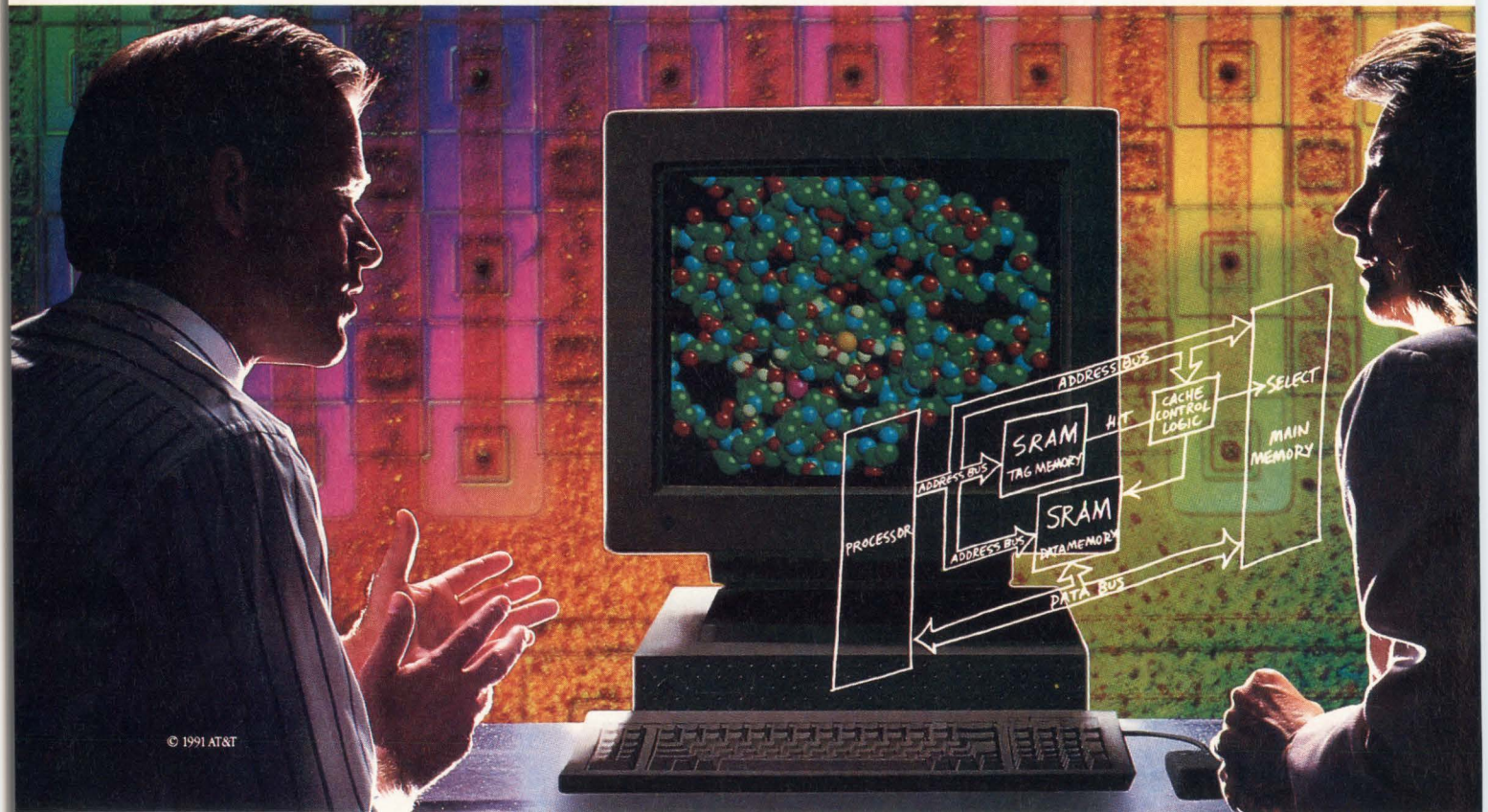
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trollers) is also designed to work in the 3-V range. It's a fully-static design targeted towards where DMA is important: one of its primary features is a pair of high-performance DMA controllers which reside on-chip. Next year, Motorola will also announce 3-V versions of its HC11 series of microcontrollers. "We expect to come out with a description of the operation of (HC11) parts in Q1 '92 and start to supply parts thereafter. Right now we are in a position where we can respond to a specific customer requirement, but we don't have a standard offering in the 3-V area" says Dick Spilo, Motorola's strategic marketing manager.

*Mike Webb, AMD's director of system marketing and engineering, checks AMD's "reference platforms" for the company's 3-V 386 processors announced late in October.*

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For its part, National Semiconductor (Santa Clara, CA) has had 3-V parts for some time. "We have a number of 3-V processors," says Ian Olsen, director of marketing for National's embedded control group. "Our COP 800 line runs at 3 V. We also have some 4-bit processor in the COP 400 line that also run at 3 V. 3-V seems to be very popular. But there are some customers that demand processors that can operate in the 1.5- to 1.7-V range when the requirement is to run the system on one battery rather than two," he adds.

It's not just the processor vendors that have caught the 3-V bug. Manufacturers like S-MOS Systems (San Jose, CA), for example, are building disk drive controllers that are also characterized at 3 V as well. S-MOS plans to sample its SPC20553V AT/XT floppy controller chip in December and is aiming for volume shipments in Q1 '92. In ad-

dition, S-MOS plans to unwrap a 3-V 8k x 8 SRAM soon. Other products wait in the wings. Late in the second quarter of 1992, S-MOS plans a 3-V graphics VGA controller as well as a hard disk controller. Other manufacturers of graphics controllers, memories and chip set vendors are right behind them. Like S-MOS, Cirrus Logic (Fremont, CA) is building 3-V disk controllers and graphics controllers as well. Others, like Western Digital (San Jose, CA), VLSI Technology (San Jose, CA) and Headland Technology (Fremont, CA) are concentrating on 3-V PC chip sets, some of which were discussed at Comdex in October. ■

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ATT7C166	16Kx4	10,12,15, 20,25ns	Common I/O Output Enable
ATT7C185	8Kx8	10,12,15, 20,25ns	Common I/O Output Enable Two Chip Enables
ATT7C174	8Kx8	12,15,20,25ns	Tag RAM, Flash Clear & Comparator
ATT7C183	2x4Kx16 or 8Kx16	25,35,45ns	Cache RAM for 386 Systems
ATT7C194	64Kx4	15,20,25ns	Common I/O
ATT7C199	32Kx8	12,15,20,25ns	Common I/O
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## Chip vendors look to integrate micromachined sensors

Dave Wilson, Senior Editor

At first glance, micromachining, a technology used for manufacturing tiny mechanical structures in silicon, might seem a tad "off the wall." But, in fact, the technology has already been used to develop the ADXL-50, claimed by developer Analog Devices (Norwood, MA) to be the world's first micromachined acceleration sensor. It's not surprising that other vendors including Texas Instruments (Dallas, TX) and Motorola (Phoenix, AZ) are all working on similar projects, even though products haven't formally been announced. The potential for such devices—in anti-skid braking systems, suspension systems and air bags—is enormous.

### ■ New fab process

Micromachinery itself isn't all that new. But to date, all commercially available micromachined sensors have used a bulk micromachining manufacturing process. The Analog Devices' part breaks new ground by using a surface micromachining process that lets the company integrate a sensor, as well as control circuitry, on the same die.

Typically, bulk-machined accelerometers consist of a silicon membrane or diaphragm roughly 10  $\mu\text{m}$  thick formed by chemical etching. In the center of the membrane is a large block of silicon called the test mass. On the top surface of the device, near the center of the membrane, thin film piezo resistors are deposited. The resistors, whose resistance changes when they are deformed, are connected in a bridge circuit. Acceleration causes the test mass to move, deforming the dia-

phragm. The deformation results in a change in the resistors' resistance which in turn results in a small voltage output from the bridge circuit.

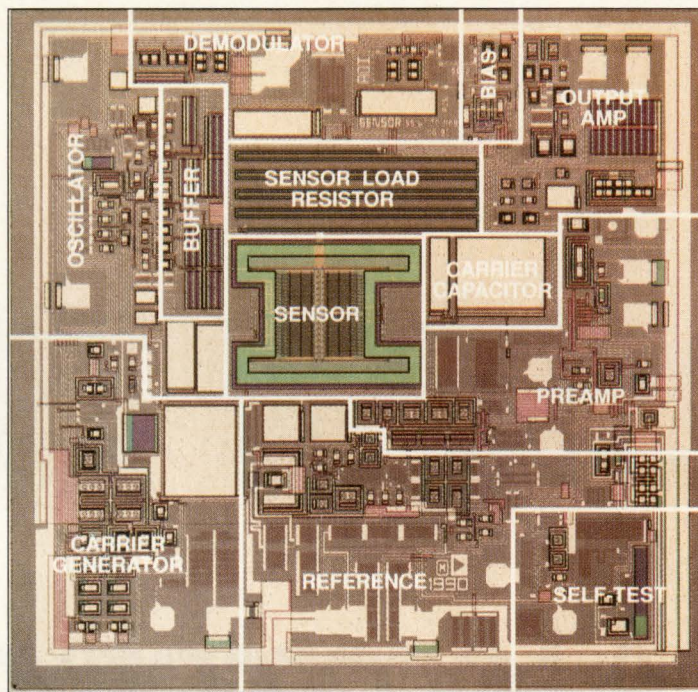
Surface micromachining, on the other hand, is a much more sophisticated technique than bulk micromachining. Various beams, masses and other structures can be formed by depositing and etching multiple thin films and layers of silicon and

section manager at Motorola's Custom Technologies Center. According to Dunn, because of the characteristics of capacitive or piezoresistive devices, such as dc response, no shift due to shock, and the requirements for self-test features in many applications, they are the preferred choice in many applications. Analog Devices agrees. The ADXL-50 chip, in fact, makes use of a surface micromachined capacitive sensor. In addition, on-chip excitation, self-test and signal-conditioning circuitry have been provided.

When viewed from above, the micromachined capacitive sensor looks like the letter "H." The thin arms of

the H are the tethers anchoring the micromachined element to the substrate. The thicker central mass is free to move in a plane perpendicular to the tethers. A series of filaments project from the mass of the central mass. Each is one plate of a series of parallel plate variable capacitors. The other plates interleave with the moving mass plates and are secured to the substrate. Acceleration or deceleration in the axis of sensitivity exerts a force on the central mass which moves and displaces the interdigitized capacitor plates. This causes a fractional change in capacitance. Actually, the mass doesn't move. It's prevented from doing so by the application of an equal but opposite force created by applying charge to the capacitor plates. Acceleration can be derived by measuring the charge applied to the plates.

On-chip signal-conditioning circuitry produces a scaled-referenced and temperature-compensated output voltage between 0.25 and 4.75 V. In addition, a digitally controlled self-test function lets the sensor deflect at any time, producing a precise output voltage corresponding to the equivalent g-force for a healthy sensor. In that way, designers of systems that embed such a device can



The ADXL-50 is claimed to be the industry's first micromachined accelerometer. In addition to the on-chip sensor (highlighted in green and inset), the chip sports on-chip signal conditioning and self-test circuitry. The sensor measures 500  $\mu\text{m}$   $\times$  625  $\mu\text{m}$ . The capacitor plates are approximately 115  $\mu\text{m}$  long and about 4  $\mu\text{m}$  wide. Accuracy of the device is guaranteed at 5 percent over the  $\pm 50$  g range.

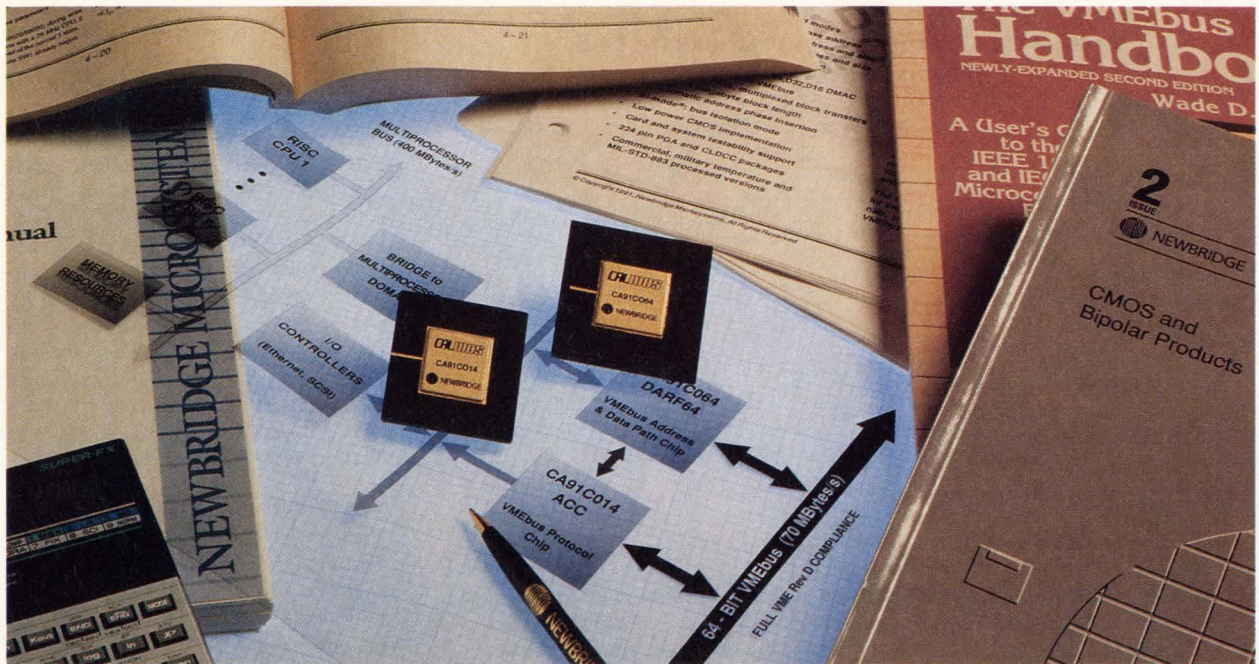
silicon oxide. The feature dimensions of such devices are 1-2  $\mu\text{m}$ , roughly the same as conventional electronic circuits.

### ■ Three methods of sensing

Capacitive, piezoelectric and piezoresistive are three methods of sensing that can be used in micromachined structures, according to William Dunn, sensor circuit design



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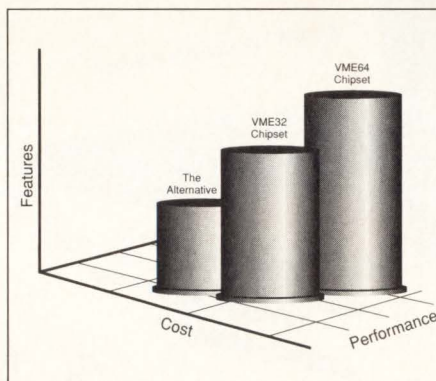
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CIRCLE NO. 30



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Comparison of capacitive, piezoelectric and piezoresistive sensors

	Capacitive	Piezoelectric	Piezoresistive
Loading effects	High	High	Low
Size	Small	Small	Medium
Temperature range	Very wide	Wide	Medium
DC response	Yes	No	Yes
Sensitivity	High	Medium	Medium
Shift due to shock	No	Yes	No
Self-test features	Yes	No	Capacitive
Damping available	Yes	No	Yes

At the Microsystem Technologies '90 conference (Berlin, Germany) last September, Motorola researcher William Dunn presented this comparison of capacitive, piezoelectric and piezoresistive sensors, leading some industry observers to conclude that Motorola will commercialize a capacitive device soon.

be assured that the device is working after years in the field.

"We can manufacture this thing on a conventional semiconductor process and make the sensor 1/20th the size of a bulk micromachined sensor," says Ian Bruce, senior technical marketing engineer at Analog Devices. "That leaves us a lot of room to put signal-conditioning circuitry on the same chip. By doing so, we can sell a complete signal-conditioned micromachined sensor to General Motors for five bucks. There's no way you can get to that price point with bulk micromachined technology," he concludes.

Where will it lead?

Clearly, the potential for micromachined devices is great. And it's interesting to speculate where Analog Devices or other silicon vendors may be considering using micromachining technology. "We are going to develop some more devices that mea-

# How well does Texas Instruments support





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sure different g ranges. We will have a family of devices that will span  $\pm 2$  g to  $\pm 200$  g. That should cover most of the application requirements," exudes Analog's Bruce.

Both Texas Instruments (Attle-

***It's interesting to speculate where silicon vendors may consider using micromachining technology.***



boro, MA) and Motorola are secretly working on such devices too. Motorola is rumored to be currently pursuing the development of a product "very much like Analog's ADXL-50" that's capacitive and surface micromachined. As a parallel development, Motorola is also supposedly

designing a bulk macromachined device that uses "better understood" techniques, according to sources close to the company. One or both products may be available as samples in 1992 with production slated for the latter half of the year. Motorola is also examining how the sensing function can be integrated into a signal-processing chip, according to sources close to the company. Indeed, some products are presently in pilot line production at Motorola, but they aren't available commercially. They're simply being evaluated and tested.

For its part, Texas Instruments is also conducting research into such devices in its Freising plant just north of Munich in Germany. Like Motorola, TI hasn't made any commercial disclosures. And TI spokespeople would not comment on rumors that the company has already sampled devices to a major automotive company. But TI has

demonstrated that it has the know-how to build micromachined devices. "We do have a development program ongoing. We are in the process of making [accelerometer devices]. And we are targeting airbag systems using micromachined silicon technology," says Greg Noelte, program manager for TI's micromachined acceleration sensor group. "But I don't want to get into any more details at this time." ■

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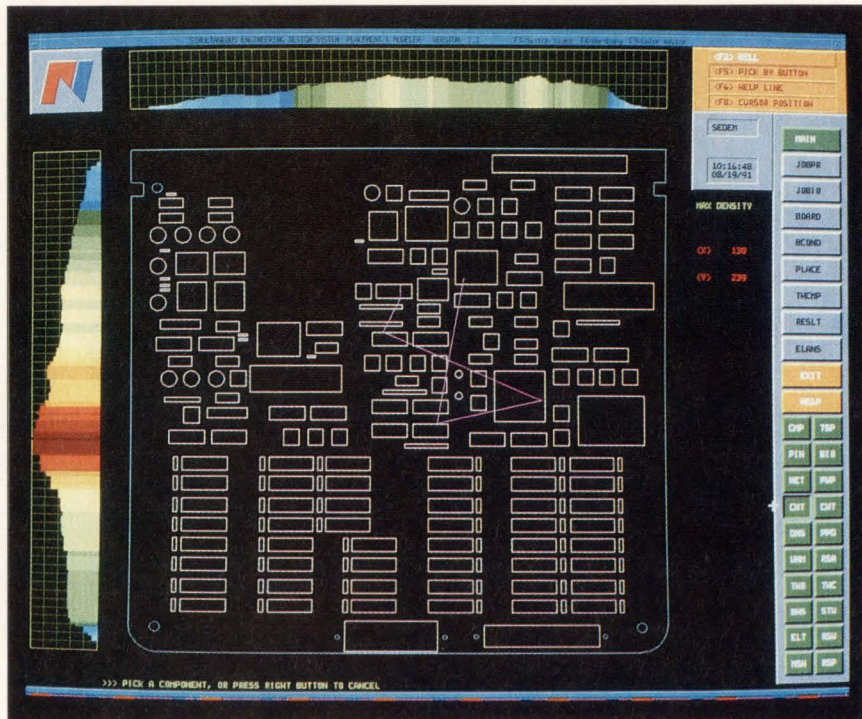
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## PCB placement tools tackle today's layout constraints

Mike Donlin, Senior Editor



This circuit board laid out with the PCB Place tool from Pacific Numerix shows a histogram of the board's wiring density and a net that didn't meet the desired maximum delay time. In this case, the automatic placement will have to be run again.

Printed circuit board placement tools are facing the same uphill battle autorouters have fought over the last 10 years. Not only do both tools have to adhere to design rules to produce a working, manufacturable product, they must do it faster and better than a human designer or no one will buy them. Until recently, most EDA vendors have put their efforts behind routing algorithms, because that's what designers wanted. Now that autorouters have proven their worth for all but the most complex designs, EDA vendors are concentrating their efforts on placement tools that assist the board layout specialist in adhering to a host of constraints laid out by the design engineer, the test engineer and the manufacturing capabilities of the fab.

Many of these considerations, such as the thermal behavior of components and constraints of automatic

pick-and-place equipment, were traditionally left until late in the design cycle. But the high cost of multiple iterations and tight time-to-market windows are signaling the end of the leisurely design cycles of the past.

"We've been in the back end of the process for too long," says John Roth, vice-president of sales and marketing for Pacific Numerix (La Jolla, CA). "By the time our tools discover a parasitic or thermal problem it's almost too late in the design cycle to do anything about them. So we want the design engineer to get more involved in component placement. We envision an environment where the layout specialist initially places the connectors and some of the components that relate to the physical constraints of the system's chassis and then sends the project back to the design engineer for placement of critical components. This brings the

designer into the layout portion of the design cycle where his expertise can do some good."

### Tool encourages involvement

To encourage the evolution of this type of environment, Pacific Numerix has recently unveiled PCB Explorer, a preroute signal integrity tool that complements printed circuit board design systems. The PCB Explorer lets engineers place components relative to signal integrity, thermal characteristics and device fatigue constraints. Board design and component placement can be electrically validated by the use of built-in parasitic parameter extraction and transmission line analysis capabilities, including wave propagation delay, reflection and crosstalk conditions. After the first pass with the PCB Explorer, the system will check the Manhattan distance (the shortest routable distance between two points) and line delay requirements to insure that each net's length is within the maximum allowable assigned propagation delay. Nets that don't meet the criteria are highlighted. The tool will also schedule pin ordering of all nets and minimize the wiring length and logical connections.

Though tools such as PCB Explorer try to bring as much information as possible to the layout portion of the design cycle, some engineers are still skeptical that placement tools have proven their worth. "Right now I don't think that most placement tools fit the bill," says John Umina, president of ProDesign (Newton, MA), a printed circuit board design bureau. "Some of the interactive ones can bring up parts for placement that have the most connections to the component you just placed, and that's useful, but the fully automatic ones take so much time to set up that most engineers would rather just place components by hand."

EDA vendors are trying to answer this objection by bringing sheer computing speed into the game—speed which would make the set-up time and learning curve worthwhile. "It's true we ask designers to set a list of priorities," says Pacific Numerix' Roth. "These might include maximum propagation delay or parasitic parameters, but we've benchmarked our tool and it can place a 250-com-





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I got a tip that a major military contractor had to simulate a system defined in VHDL at the behavioral level. The problem was, they had to process a minute of real time data through the design to verify it. Using a SPARC 2 with enough memory for a herd of elephants, it still would have taken months. But these guys simulated that minute of real time data on the entire design in a few hours. How? Turns out they were a beta site for the new IKOS VHDL Accelerator. The brass was impressed.

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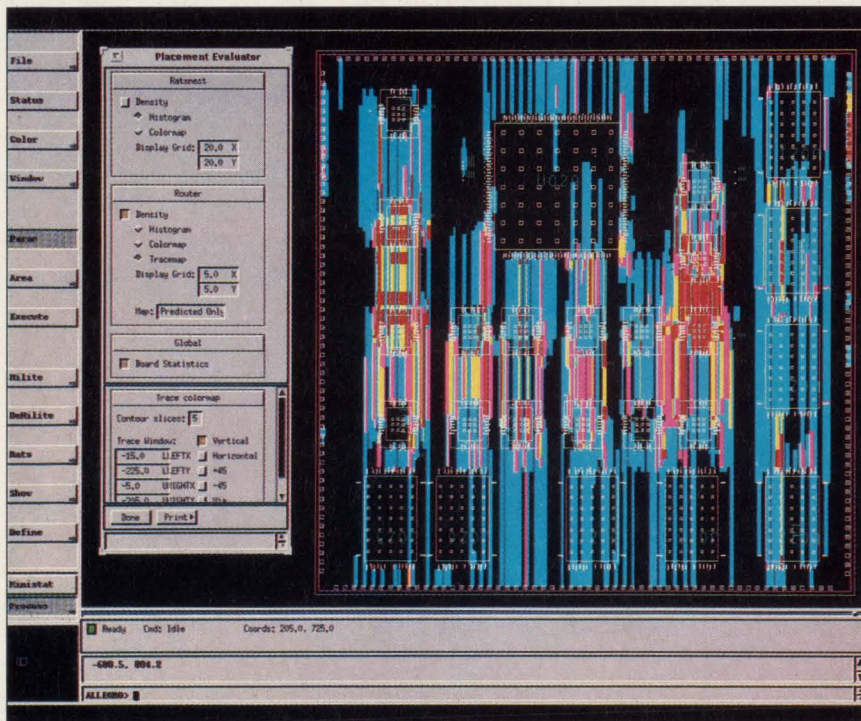
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## CAE/CAD TOOLS



When run in route density mode, Valid Logic's Placement Evaluator looks at printed circuit board component placement relative to the number and direction of layers, parameter and grid settings, line widths and design rules. Colormaps overlaid on the board identify potential trouble areas for the autorouter.

ponent board in less than a minute. I'd say that makes up for quite a bit of set-up time, especially if a designer needs to play 'what-if' games with the layout to get an optimum design."

### Too many details

If placement tools do gain acceptance, it will undoubtedly be for the same reasons routing tools gained a foothold—design rules are getting too complex for any engineer to keep them in mind during a lengthy design cycle. But no matter how many design rules are included in the autoplacement routines, the experienced engineer still has the upper hand when it comes to analyzing a design during placement.

"I think that the drawback to most placement tools is that they can't look ahead like a human designer can," says ProDesign's Umina. "An experienced designer might place a component on top of another one just to get the design partitioned, and then spread the parts out to fill up an area. An autoplacement tool just looks for an empty spot and puts a device down. EDA vendors

need to find a way to make their tools shove components around like a designer does if they want to compete with human expertise."

Currently, printed circuit board placement tools work on a limited set of parameters to make decisions about where a component should go. They work on a user-defined grid according to restrictions laid out by the design engineer. If the tool tries to place a component and the result is favorable according to those guidelines, then the component is placed—if not, the tool tries again.

To expand the placement tool's decision-making capabilities, EDA vendors might consider using techniques that ASIC tools use, such as simulated annealing. This technique operates on the assumption that sometimes choices have to be made that make things worse before they get better. If the design doesn't improve after a certain amount of degradation, then everything is undone and the tool tries again. The drawback to this approach is that the tool might take too long to make decisions if there are too many

choices and an engineer is going to simply finish the design by hand. Time is still of the essence.

### Post-placement assistance

Some EDA vendors are staying out of the autoplacement fray by offering tools that examine a completed placement for routability. Valid Logic Systems (San Jose, CA) has developed the Placement Evaluator that automatically analyzes the routability of printed circuit boards, multiwire boards, hybrids and multichip modules (MCMs). The tool helps a designer determine whether a design can be routed in a given number of layers and identifies potential trouble spots for Valid's Insight router.

"We knew that placement tools that are based solely on rats nest

***For placement tools to gain acceptance, they must mimic the decision-making process design engineers use when drawing a schematic.***



density don't consider enough parameters," says Tom Leonard, member of the technical staff at Valid. "What we wanted to do was simulate a route based on component placement that took many design rules into consideration. Our tool runs in minutes instead of the hours that a real route would take, so it's not the actual routing algorithm. It takes a snapshot of the current setup for the route and notifies the engineer of hot spots via a color map overlaid on the layout."

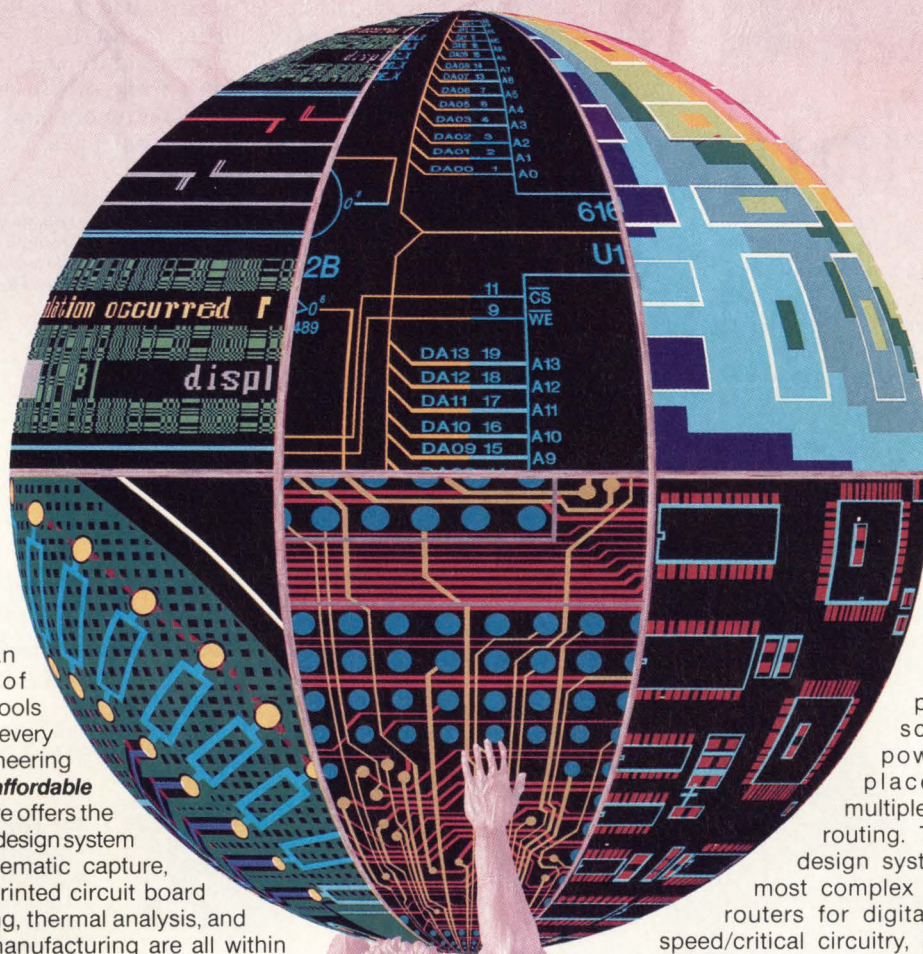
These colors designate overflow areas where there are too few available channels for the router to complete the number of projected connections. A trace map helps the designer identify congested areas and replace components for a more efficient route.

Probably the most difficult task ahead for placement tool designers is trying to emulate the decision-making process of an experienced designer. Some placement con-



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## CAE/CAD TOOLS

straints, such as parasitic and thermal effects, can be readily incorporated into a tool. But there are more subtle design rules which spring from a designer's experience which are much harder to anticipate.

"Designers can get pretty picky about how they want their boards laid out," says Tony Grzesik, printed circuit board design specialist at PictureTel (Peabody, MA), a manufacturer of video and audio boards. "A tool might look at a design and place components so that a trace adheres to a Manhattan distance, but a designer might have more in mind if he were laying out the same trace. For instance, a design engineer might want a net from a pin on an IC to go to a resistor before it goes to a capacitor and his schematic would reflect this. An automatic tool might overlook that constraint if it's just considering minimum trace lengths. Placement decisions don't always adhere to the shortest path between two points."

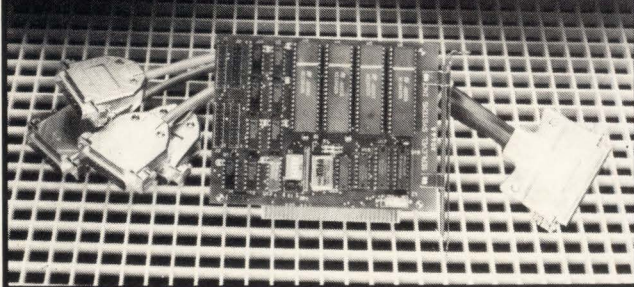
For placement tools to gain acceptance, then, they must go beyond the obvious design constraints that guide them today. In essence, they must mimic the decision-making process design engineers use when drawing a schematic. Layout engineers intuitively follow guidelines inherent in a designer's schematic. This might be the paradigm that EDA vendors will have to emulate if they want to win engineers over to autoplacement and computer-aided placement tools. ■

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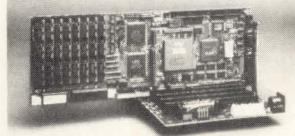
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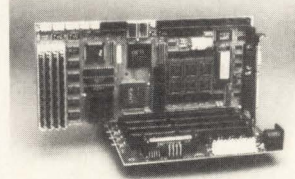
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## Claims by FPGA tool vendors bury reality in noise

Barbara Tuck, Senior Editor

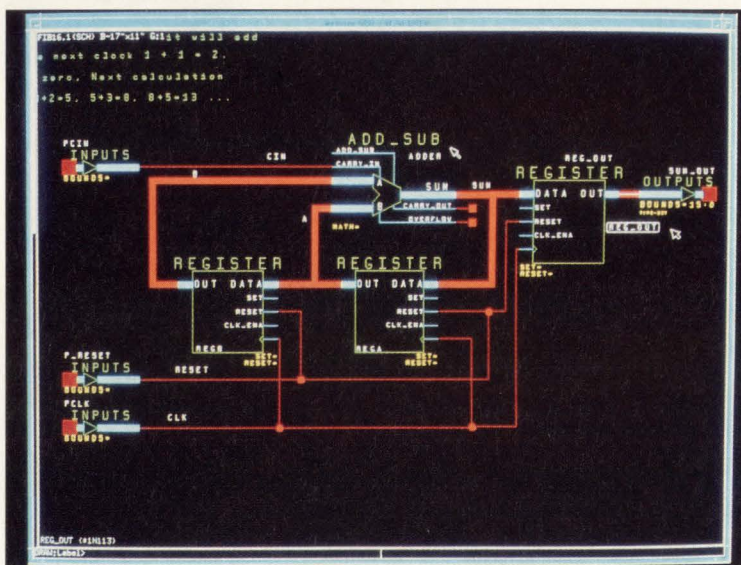
Fueled by expectations that by 1995 the field-programmable gate array (FPGA) market will be more than five times what it was last year (consuming 1/3 of the gate array market), FPGA and tool vendors continue to introduce products at a feverish rate while gate array vendors select strategies to protect their ASIC business. In the meantime, FPGA designers are sifting through vendors' claims for tools that will deliver the ease-of-design and fast time-to-market promises that first made FPGAs popular. Users wanting to migrate from an FPGA to an ASIC, or from an ASIC to an FPGA, have to sift through even more claims and evaluate more tools.

The unfortunate thing about FPGAs is that from the beginning, they've been thought of as somewhat synonymous with magic. With silicon having become so complex and time-to-market pressures so burdensome, designers wanted to believe a magical solution was at hand. Designers who have worked with FPGAs have discovered, however, that despite their potential, FPGAs and the tools available to design them are far from delivering the hoped-for magic.

### Design trade-offs

The absence of an efficient and consistent FPGA design methodology, not to mention a migration methodology, hasn't stopped vendors from engaging in an almost furious race to bring out new FPGA architectures, design tools and migration paths. Just this past month several FPGA design tools and migration paths were announced. The tools—or more accurately, the claims—

have one thing in common: ease of design. When evaluating tools, though, users need to realize that for every ease-of-design feature a vendor claims for a tool, there's more than likely a corresponding negative feature. To fully grasp the design trade-offs involved, therefore, users need to hear what vendors say, as well as what they don't say.



*Xilinx claims that the amount of time required to enter a logic cell array design is significantly reduced with Blox (Blocks of Logic Optimized for Xilinx), since the user designs at the block diagram level instead of using gates and flip-flops.*

For instance, AT&T Microelectronics (Allentown, PA) has just announced its SoftPath tool. With it come promises of technology independence, the ability to define a system independent of final ASIC technology, as well as seamless, transparent migration from an FPGA to a gate array. AT&T has covered itself by second-sourcing Xilinx Logic Cell Arrays (and developing its own FPGA architecture), offering gate arrays compatible with NEC CMOS gate arrays and by maintaining a leadership position in standard-cell technology. Nevertheless, to benefit from the technology independence AT&T offers, users have to accept being dependent on a single vendor.

When S-MOS Systems (San Jose, CA) signed an agreement last month to resell the Retargeter FPGA conversion software from Viewlogic Systems (Marlboro, MA), S-MOS also promised vendor independence. The Retargeter can, indeed, accommodate any FPGA architecture for the S-MOS user, and it can remap a design from any FPGA to any gate array—any S-MOS gate array, that is. But if a S-MOS user buys a limited-license Retargeter from S-MOS and then decides to target another gate array technology, the user has to pay Viewlogic lots of bucks to 'unlock' the software for vendor independence with regard to gate arrays.

Another claim attached to a new FPGA design tool comes from Xilinx (San Jose, CA) and touts freedom from device-specific implementation details through the use of large graphical modules that make up a generic library. That generic library, part of the Xilinx Blox (Blocks of Logic Optimized for Xilinx) synthesis system, is based on the Library of Parameterized Modules (LPM) standard intermediate format, backed by a consortium of FPGA and tool vendors. Designers will be able to use the generic library's parameterized modules, embedded in the EDIF syntax,

to describe macrolevel netlist components. But the generic library doesn't alleviate the necessity for a Xilinx user to purchase a silicon-specific library for each of the Xilinx architectures. That means that a Xilinx user, who may have already purchased the XC2000 and XC3000 libraries from Xilinx, will have to purchase two more libraries to design with the new XC4000 family parts—the silicon-specific library for the XC4000 family members as well as the Blox generic library with which to design at a higher level of abstraction.

At that point in the shopping spree, the Xilinx user would have a



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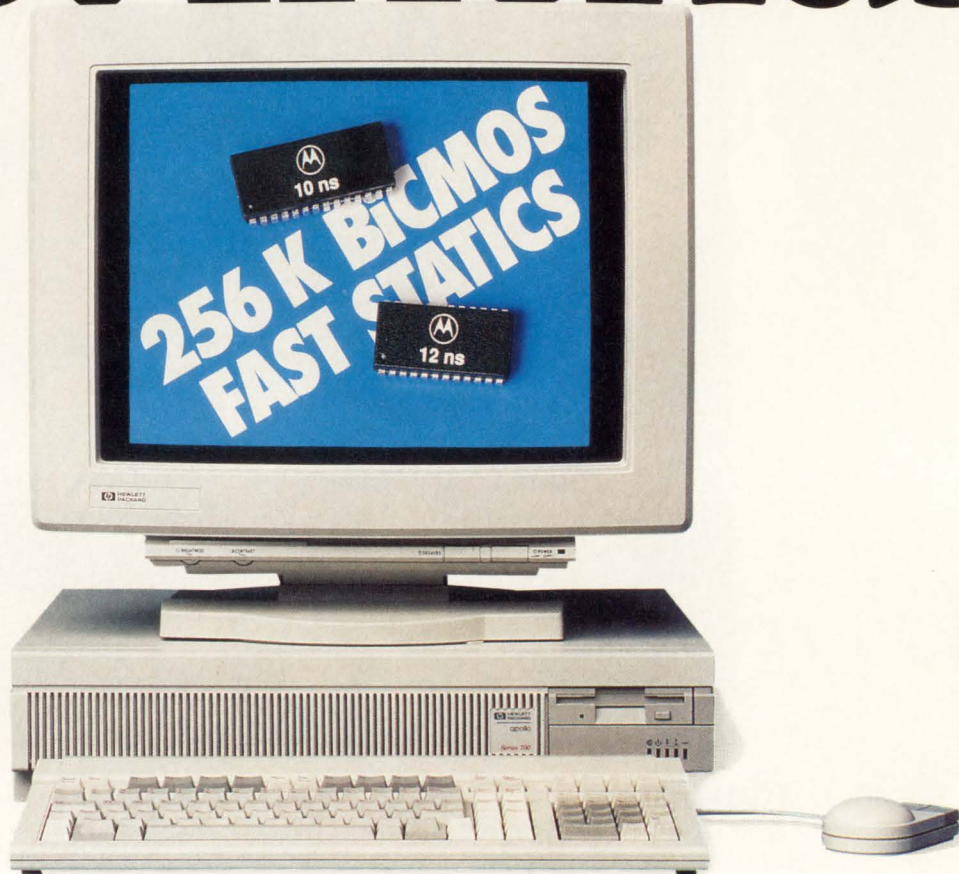
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proprietary tool providing expert knowledge of the Xilinx LCA technology, but would be locked into Xilinx as a vendor. And the user would still not have solved the migration issue unless he or she chose to go to Xilinx hardwired devices for volume production instead of going to an ASIC vendor's masked gate array.

Though Xilinx and Synopsys (Mountain View, CA) continue to claim that they're working toward a solution that would let a Xilinx library run on the Synopsys Design Compiler and thus interface to gate array vendors using Synopsys, that solution has not been forthcoming. The coarse-grained nature of the Xilinx architecture makes it far less than an ideal candidate for the Design Compiler synthesis program which was designed with fine-grained gate arrays in mind.

While Synopsys offers no help to Xilinx users, it does let ASIC designers use VHDL or Verilog to describe the function of an ASIC and then synthesize that design in an Actel, AT&T or Texas Instruments FPGA. Last month, Altera (Santa Clara, CA) joined that list and announced library support for its programmable devices on the Synopsys Design Compiler. Synopsys claims that V2.2 of its Design Compiler, which begins shipping this month, gives users doing technology translations the ability to generate a set of timing constraints for an existing design based on the current timing of the design.

But users can't benefit from any of the advantages of the Synopsys FPGA synthesis capability, unless they purchase the silicon-specific libraries of each of the FPGA families they're interested in synthesizing on the Design Compiler. And after the FPGA design is optimized, users still need to transfer the netlist to the FPGA vendor for place and route.

Too good to be true?

The ultimate toolset for the FPGA designer would be one that would offer device and vendor-independent FPGA design and layout tools. A Daisy/Cadnetix spin-off called NeoCAD (Boulder, CO) has, indeed, extended that promise to FPGA designers, along with promising a timing- and constraints-driven design environment. Several NeoCAD design modules have been in beta test since July, and the complete

toolset goes to beta test this month with first shipment expected in January. To benefit from this toolset, however, users first have to take the leap of faith required to believe that a brand-new company like NeoCAD could possibly have developed technology capable of achieving better results with an FPGA architecture than an FPGA vendor itself.

"NeoCAD will provide designers with a single set of device-independent, standards-based tools useful across all FPGA vendors' processes and architectures," says Bob Anastasi, president of NeoCAD. "We are applying our considerable CAD expertise to deliver tools that provide for technology-transparent design—the ability to design without regard to implementation technology—from one FPGA vendor to another, and between FPGAs and gate arrays." He goes beyond device- and vendor-independence to claim that NeoCAD tools will achieve higher clock speeds and greater gate utilization within existing architectures.

If NeoCAD can make good on its promise, and throw in the use of a single generic library to boot, it just might become the single most successful EDA tool vendor yet. But until designers actually use the NeoCAD tools and uncover whatever negative features might lurk behind all the positive claims, as has happened with the tools thus far, it's best to reserve judgment. Since user experience with FPGA design tools and migration methodologies can be invaluable to other users, next month's Special Report on "Migrating from PLDs and FPGAs to full ASICs" will focus on users' design and migration experiences.

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## Micro gyroscope brings motion sensing to low-cost systems

Tom Williams, Senior Editor

A series of technical breakthroughs in gyroscope technology will soon open the doors for the use of gyroscopes as motion sensing devices in a wide range of computer-based systems including navigation and dead-reckoning systems, robotics and machine control, surveying systems, optical instrument stabilization, hand-held computers and more. The enabling technology is embodied in the GyroEngine by Gyration (Saratoga, CA). The GyroEngine is, quite simply, a low-power, low-cost, very accurate gyroscope about the size of a walnut that can be easily integrated into digital systems. Conventional gyroscopes are typically expensive (\$1,000 to \$200,000), bulky, heavy, and must be manufactured with precision-machined metal parts. The GyroEngine is manufactured using injection molded polycarbonate plastic, measures 1.25x1.75 in. and consumes 0.1 W of power at +3 V.

Gyroscopes operate on the principle of the momentum of a spinning flywheel. Once in motion, the spinning mass resists changes to its angular attitude. In typical gyroscopes, the wheel is mounted on a pair of gimbals that lets the housing—and the plane or ship that contains it—rotate freely around it. Motion sensors in the gimbals relay changes in angular attitude that can then be sent to a gyrocompass or other control system. Typically, these motion sensors are magnetic or potentiometer-based and require digital-to-analog conversion to yield the digital data needed by a computer. Balancing parts requires precise machining and measurement.

### Optical motion sensor

One of the major breakthroughs in the GyroEngine was the development of an optical motion sensor. The optical sensor requires only one sensor for two degrees of motion and it gives a direct digital readout without analog-to-digital conversion. An LED shines light through a ring perpendicular to the spin axis of the

wheel. On the ring are lines for optical sensing. In a hole at the gimbal bearing perpendicular to that axis is another grid with radial lines which the light also passes. The interference or moire pattern created by the two grids changes characteristically when the housing is rotated along either axis. A quadrature photosensor picks up the changing pattern which is interpreted by a microcontroller on a small external circuit board.

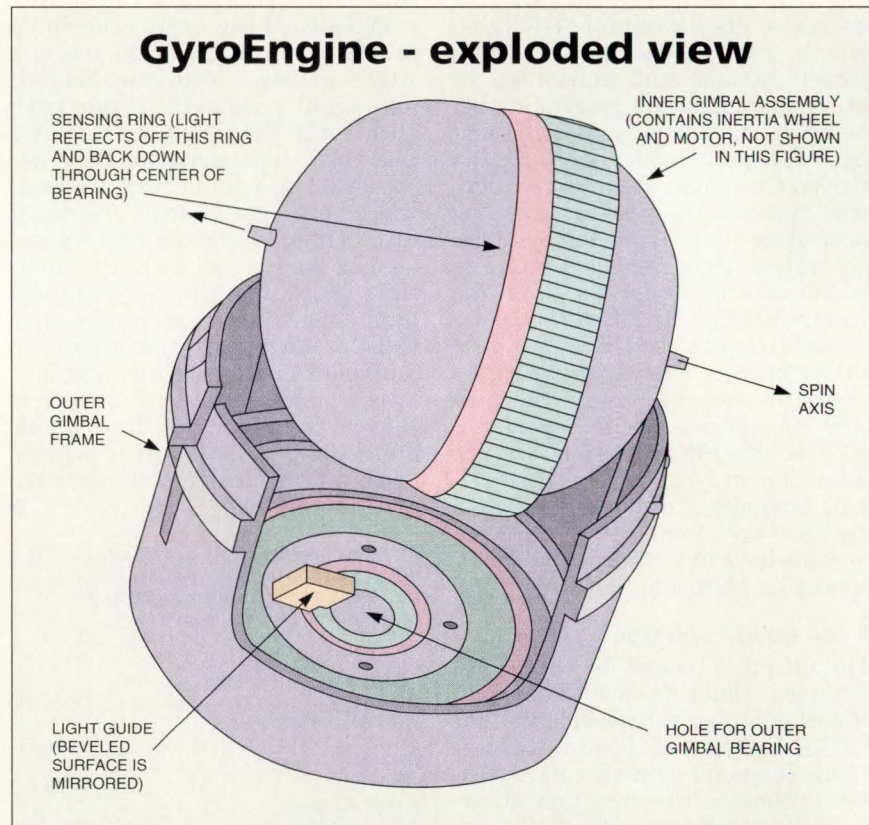
The grid resolution is 2,300 lines/in. and the angular resolution is currently 10 bits/degree. Gyration can produce GyroEngines with greater or less accuracy, with corresponding differences in price, depending on customer needs, says

president and CEO Tom Quinn. The raw output of the GyroEngine is parallel, but is also convertible to RS-232 or RS-422 for use in a cursor-pointing device, for example.

### Plastic replaces metal

Another breakthrough is in manufacturing. Quinn notes, "Plastic has an almost guaranteed volume weight." Thus, injection molded plastic yields parts of uniform weight and shape so that the only precise balancing required is in the flywheel and that's a matter of shaving just a little metal, Quinn says. The gyroscope and motor are mounted on jewel bearings and the motor control electronics are contained on a surface-mount chip within the motor itself. "This gyroscope has been designed so that we can make two gyros per minute," says Quinn.

Gyration is incorporating the GyroEngine in a product, indeed a pointing device, for use with laptop



*The GyroEngine's flywheel and motor are encapsulated in a fluid-filled shell and a system of gimbals that sense two axes. Light shines through a grid of lateral marks on one axis and through a radial grid in a hole on the other axis. The interference pattern of light passing through the two grid systems allows direct digital data sensing of angular changes on two axes.*



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of translational (i.e., lateral) or rotational motion. A system using two GyroEngines, therefore, can sense all six degrees of freedom in a 3-D coordinate system.

Gyration will be supplying GyroPoint as a development kit including the pointer device, drivers and soft-

ware. "If you could mount the GyroPoint firmly in a car, you could combine it with some software in a laptop, bring in data from the speedometer and with some software build an automobile navigation system," says Quinn. Mapping software from companies such as Etac (Menlo Park, CA), which make automobile navigations systems, currently depends on sensor data from a vehicle's wheels. Wheel sensors give forward and backward motion data and by measuring the differential between wheel rotation, also give angular turning data.

The problem with wheel sensors is that they are expensive to install and computing the turning angle from differential data requires processing that's not needed with a gyroscope, which gives direct angular data. According to Quinn, newer cars with digital instruments will soon have digital speedometer data available at the dashboard; integrating a gyroscope-based navigation system should become a lot easier and less expensive.

The small size will also make it easier to put gyroscopes in devices such as robot arms, portable surveying equipment and hand-held systems that work with the global positioning system (GPS), the satellite navigational system that let "Stormin' Norman" execute his huge flanking maneuver in Operation Desert Storm.

"GPS gives you position, but it doesn't give you a heading," says Quinn. Also, GPS updates only about every three to four minutes. While it can be used with a magnetic compass for easy navigation, use with a gyrocompass will allow automated navigation for aircraft, missiles, ships, and robot vehicles of all kinds, and a sensor as small and low-powered as the Gyro-Engine is expected to let automatic navigation penetrate into ever smaller systems. ■

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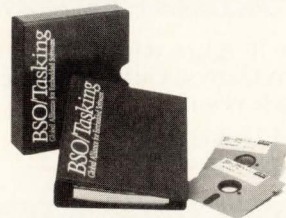
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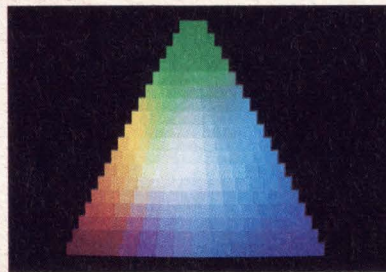
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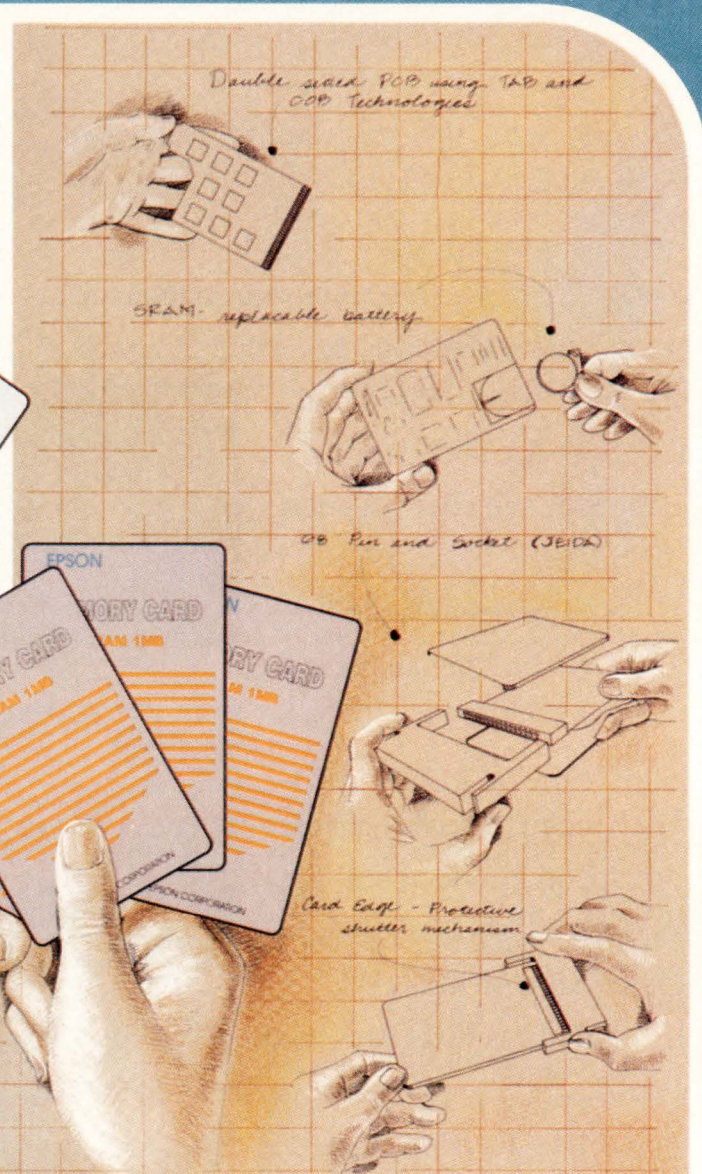
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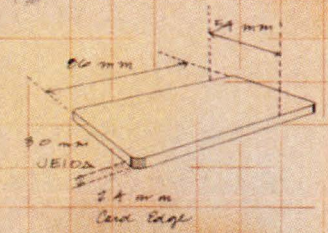


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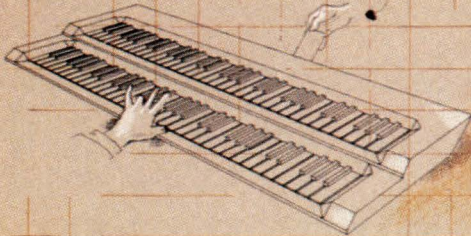
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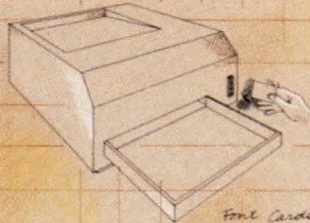
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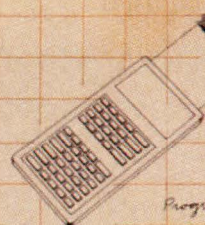
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# Real-time multiprocessing pushes software limits

*Developing software for real-time multiprocessing systems requires attention to the needs of the application, communication and system architectures. Tools to help designers are not yet mature, but are well on their way.*

Tom Williams  
Senior Editor

**W**hen the ship's captain signals flank speed, the starship captain calls for warp eight and the computer user plugs in an additional CPU, they all want only one thing: more power. None of them wants to hear any objections from engineering. It's engineering's job to see that power can be easily increased—from the user's point of view—by solving all the inevitable technical problems involved in a transparent way. The computer user expects to program a system in terms of an application's needs (i.e., in a high-level language) and run the application without regard to hardware details. A system should be flexible so functionality can be increased by adding software tasks and processing power can be increased by adding CPUs. Easily enough stated for the user, but for the engineer, those demands can pose some fairly daunting problems, especially in the arena of software design.

Developing software for multiprocessor systems is closely linked with the application's needs as well as the chosen hardware architecture. Designers need to use interprocess communications that are flexible, yet maintain real-time behavior. They need to distribute tasks across hardware resources (e.g., processors, I/O channels) and redistribute them in response to changing demands without major rewriting of code. They need tools to debug code residing on different processors, tools that can help them analyze task execution and processor utilization under load in order to optimize the use of resources in a design and still be sure that a system won't fail because of overload. These are tall orders, and while there is yet a great deal to do in some areas, there has been good progress in others.

Multiprocessing, of course, involves more than just turning a number of processors loose on different parts of an application—they have to communicate. The interprocess communication (IPC) that was formerly done between tasks on a single CPU must be mapped to a multiprocessor



*Real-time multiprocessing systems are pervading many types of equipment. This digital music-mastering system relies on real-time communications between processors to separate the studio end from noisy fans and disks while maintaining real-time control of the recording and mixing process.*



## REAL-TIME MULTIPROCESSING

architecture. This forces the designer to make decisions about IPC in the light of interprocess OR communication. That is, how a set of communicating tasks will be affected by mapping them onto a physical and distributed architecture.

"IPCs have to be real-time," says Borko Furht, senior director of research and advanced development for Modcomp (Ft. Lauderdale, FL). This means they shouldn't affect interrupt latency or interfere with task scheduling and they should be predictable. IPCs should also work at interrupt speed, provide data at

the currently running task, the message's data is transferred immediately over the system bus at bus speed. Otherwise, it's queued to be transferred in the order of its priority. The key point is that message passing can be handled and prioritized like any other task in the real-time system.

Of course, using shared memory to pass IPC data can lead to bus contention and degrade determinism. So there's a need to keep messages that pass across the bus short and to group tasks that communicate a great deal with one an-

DSP chip, which incorporate serial communications channels. On a Transputer, these channels (called links) are like interrupts that can also pass data point-to-point. There's still a need to see that such high-speed messaging capability doesn't interfere with task scheduling, (i.e. that a link, once asserted, doesn't force its data on the processor before it's ready).

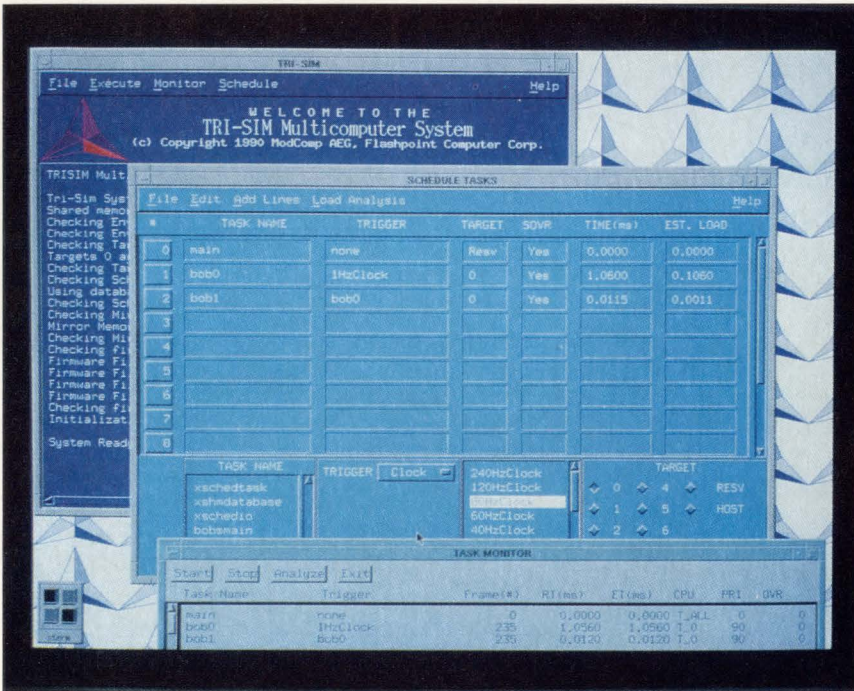
"On a Transputer, you can have guardian processes that listen to link traffic and say, 'OK, this is a message to X, so I'll pass it right away,' or, 'This goes into a mailbox for now,'" says Raul Diaz, graphics application engineer for Inmos. Interestingly, however, Diaz points out that message passing within one Transputer can be slower than over links to different processors because it's a memory-to-memory move that uses bus bandwidth while link communication is done with a DMA engine. Because of the Transputer architecture's unique nature, this would appear to be an exception to the general rule of putting high bandwidth communications on the same processor.

### IPCs should be flexible

Actually, it only helps to point up the need to analyze or experiment with different task distribution scenarios, which demand that the inter-processor communications be flexible and transparent to ease the work of redistributing tasks. It should be possible "to write an application that consists of a team of processes that run on a single machine and without any software changes to scatter those tasks on a network of machines," according to Dan Hildebrand, senior design staff member for Quantum Software Systems (Kanata, Ontario).

Within Quantum's QNX, a real-time, Unix-compatible operating system, such networking is done by the net task, one module of the operating system. The job of the net task is to make the IPC flow transparently across whatever underlying medium is used. Communication is established and tasks are assigned to processors by name within a task-creation library. From then on, according to Hildebrand, "IPC and processes finding each other are identical whether the processes are running on a single processor or on different processors on a network."

A higher-level communication interface such as Unix sockets can also



Using Modcomp's Application Worksheet, users can control a multiprocessor system, balance the processing load and schedule events for optimum efficiency from a menu-based, spreadsheet-like user interface.

least at processor bus bandwidths and provide for easy system expansion. Finally, IPCs should introduce no background traffic.

The latter stipulation eliminates several forms of IPCs such as semaphores and mailboxes. Both introduce additional overhead in the form of message acknowledgement or polling that puts traffic on the bus and makes timing less predictable. Almost exclusively, real-time multiprocessing uses message passing as the IPC of choice. Message passing is characterized by notification and data exchange. One method, used on the systems built by Modcomp, has the communicating processor issue an interrupt to the receiver. If the interrupt is of a higher priority than

other on the same processor. "The trend in multiprocessor systems," says Jeremy James, president of Precise Software Technologies (Nepean, Ontario), "is that there will be less and less use of shared memory and more and more use of microprocessors that can communicate over high-speed point-to-point links." This makes it sound like the current practice of using interrupts to signal messages and bus paths to transfer data is simply a way of getting around the limited direct communication bandwidths of present processors.

The exception is the Transputer family by Inmos/SGS Thompson (Bristol, UK) and emerging designs like Texas Instruments' TMS32C40





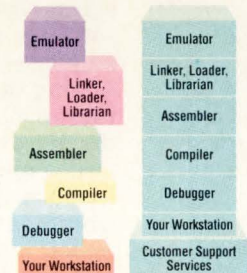
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## REAL-TIME MULTIPROCESSING

be used to make IPC transparent and flexible. VxWorks by Wind River Systems (Alameda, CA) uses sockets, which are also being standardized as a communication paradigm by the Posix committee. "Sockets are just an interface. The socket is a definition of how the program interfaces to a particular communication protocol," says David Wilner, vice-president of engineering for Wind River. "There are many protocols that can be implemented under sockets."

But the advantage is that you can code your entire application using sockets and substitute different protocols underneath. To communicate locally, you could use a very fast, very deterministic protocol; to communicate over Ethernet, you could plug in TCP/IP and the program would still see the same interface all around. The protocols would be bound to the physical media and its associated differences in speed and determinism, but the tasks could be easily reassigned by directing their communications to different sockets.

The fact, though, that communication channels between processors are hardware-dependent means that communication between processes (tasks) must be carefully considered in terms of acceptable timing and overhead. "A rough rule of

thumb," says Quantum's Hildebrand, "is to lay out your team of tasks with lines indicating what the IPC is going to be and identify the high bandwidth paths." You don't want to have those high bandwidth paths flowing across the network. The same goes for interrupt handlers and the tasks they serve.

### Tools for multiprocessor design

The main advantage of an asymmetrical multiprocessor system is to dedicate hardware resources to critical tasks and be certain the tasks will run within required time limits. Still, short of building in sufficient margins to assure a degree of comfort, how is one to know how much processing power to devote to a certain set of tasks and when a system is approaching overload and it's time to add another processor?

"That," says Inder Singh, president of Lynx Real-Time Systems (Los Gatos, CA), "is the basic issue, and most of the numbers that get published in data sheets don't address that at all. You've got to know how your system will behave under load and you've got to be able to monitor it in real-time." Timing analysis can't be taken as an average or a histogram. This means a system might have to be monitored for days or weeks to find the worst

case timing between a given critical input and an output.

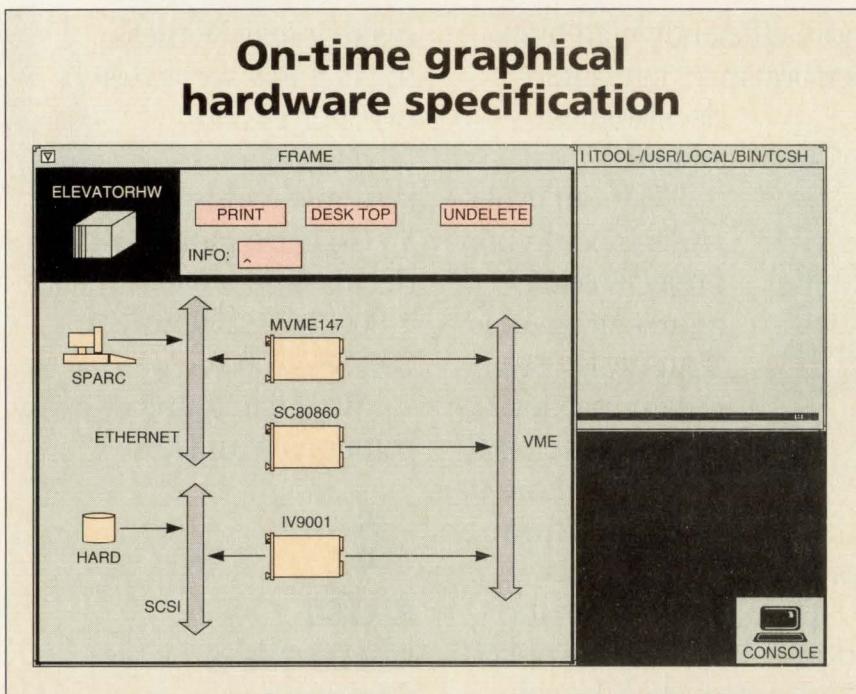
"That's typically done at the application level," Singh says. In response to needs from the space station Freedom project, Lynx has built a way for its Lynx/OS Unix-compatible real-time operating system to signal the application with a warning that the system is getting close to overload. A task can tell an error recovery routine that a deadline has been missed. If one builds in some dummy tasks with relatively low priorities, they could provide warning signals when they started to miss deadlines to alert users that the system is getting close to overload. On a space station, that would be a nice thing to know.

It's good to know you can assure reliability with empirical methods. But having met the resource requirements for critical tasks, it would be ideal to optimize the use of CPU resources in a system to keep costs down and achieve a competitive edge—particularly for commercial applications. This requires the ability to analyze CPU usage, the amount of time given tasks run and the usage of communication resources. Tools to do this in multiprocessor systems, however, are still in their infancy, although some are beginning to appear on the market.

### Approach with caution

In the absence of adequate tools, caution has been the recommended approach. "People assure themselves by building multiprocessor software and hardware taking the simplest, minimalist approach to getting the job done—knowing that they're not making optimal use of the hardware resources," says Alfred Chao, president of Software Components Group (San Jose, CA) whose pSOS+ real-time kernel also comes in a multiprocessor version called pSOS+M. This conscious suboptimal approach with people taking a realistic attitude to what they're doing, says Chao, most often leads to projects that are successful. "People who are not realistic will get bogged down in all sorts of hare-brained schemes trying to tweak the system based on the multiprocessor architecture and that usually just falls apart."

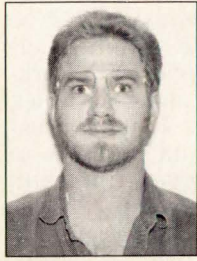
But such projects wouldn't fall apart if the designers could get sufficient information about what is happening—and that requires adequate analysis tools and debuggers.



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**Multiprocessing music in real-time**



**T**he phenomenal growth of the compact disc market has posed new engineering and economic challenges for mastering studios as they strive to meet the de-

mands of CD mastering, digital tape preparation and regeneration of catalog material. Most audio consoles, however, are based on analog technology and fall far short of the potential of digital audio processing. To meet this need we developed the Muse, a fully digital transfer console designed for digital mastering. The computing power required to process music in real-time is immense—the hard disks and cooling fans necessary to support this kind of processing power are too noisy for a mastering studio environment.

Our challenge was to achieve separation of the console/user interface from the music-processing hardware without losing the real-time link between the two functions. In addition, the complex functionality of the product required significant investments of development effort to implement a user-friendly graphical user interface (GUI). Considering the complexities of the target system, ease of development was also an important criteria. Similarly, the GUI had to meet, not compromise, our demanding real-time constraints.

The solution consists of a two-processor, networked design where the console/user interface is controlled by one processor (a 33-MHz 80386 with an EISA bus) and the music-processing hardware is controlled by a second 33-MHz 80386. The user interface processor implements a GUI and a VGA screen and also controls the various sliders, potentiometers, multisegment displays, and other devices present on the console. Specialized hardware interfaces these controls to the user-interface processor such that continuous changes of the controls can be monitored and recorded. The second processor controls a team of 30 digital signal processors and other specialized digital audio process-

ing hardware in the music processing unit. This unit actually implements the control requests coming from the user-interface and forwards the status of that processing back to the user-interface. The two control processors are connected with an arcnet to form a two-node LAN. The deterministic packet delivery inherent in a token-passing arcnet enables the two components of the system to achieve the necessary physical separation without losing the tight inter-processor communication necessary to meet the real-time constraints of the system.

The user-interface of this system requires that real-time graphs of the various response curves configured by the operator be displayed while also forwarding, in real-time, the operator's modifications to those response curves back to the music-processing unit. This lets the operator make continuous adjustments to the music processing in the system, and see those changes reflected in the various graphs displayed on the console. The messaging between the control console and the music-processing unit starts with the music-processing unit sending the results of a previous request from the control console together with current status information to the control console. The control console then processes and displays this data in the form requested by the operator. The console then replies to this status message with data containing the current settings of the controls on the console. This message loop runs continuously while the operator makes adjustments to the response curves being applied by the music-processing hardware. Simultaneously, while changes in the control settings occur, these changes are implemented by the DSPs and recorded along with the music be-

**Our solution is a two-processor design: the console/user interface and the music-processing hardware are controlled by separate processors.**



ing processed. To maintain the tight coupling required for this man/machine feedback loop, the interprocess messaging across the network has to meet a deterministic, worst-case criteria of 10 ms.

The software to implement this console is built on top of the QNX operating system by Quantum Software Systems. QNX lets the application be written as a team of cooperating, communicating processes running on a single processor. Then, without any source code changes, those processes can be distributed to run on a network and the OS will automatically cause the messages between the processes of the application to flow across the network. In addition, the network transparency lets any process use the resources of any machine in the network, regardless of whether those resources are local or remote. This lets the user-interface console boot from the network as a diskless node, and then use the disk resources of the music-processing unit to load the operator-interface software and control files. Since the OS is also inherently multiuser, we can use modems to allow dial-up remote diagnostics to support units installed at customer sites. The debugging tools can work across the dial-up links as well, letting us work closely with customers to implement customer-specific modifications.

The QNX development environment is hosted directly on our runtime system, and the support for network-distributed parallel compiles lets the runtime system double as a complete development system. Rather than cross-developing from another platform and using in-circuit emulation and other techniques for debugging, the natively hosted debugging and profiling tools let us debug and performance tune both local and network remote processes to meet our requirements.

The flexibility of a distributed real-time OS lets the physical packaging needs of the Muse be met without compromising the real-time performance of the application. And, as a bonus, there's additional capacity for future enhancements since our system's processors experience a 30-percent idle time.

**Mark Schmid**, Muse team leader, Audio Animation Inc



## REAL-TIME MULTIPROCESSING

"The only way you're going to be able to build reliable systems is to have tools that function on a higher level," says Chao. Now a number of companies are beginning to address analysis tools for multiprocessing.

Quantum Software, for example, has released a profiling tool called Prof that can profile several tasks running simultaneously. In addition to producing histograms of task execution, Prof can look at each processor and see how much of a load it's taking in an application. Furthermore, the tool can gather statistics on the volume of messages passing between nodes and help identify which are the high bandwidth paths between processes. Prof helps identify which processes are consuming the bulk of a processor's capacity and might need to move to another processor. Identifying the high-traffic communication paths helps avoid putting a high-bandwidth path across the network between two processes that could be running on the same processor.

Prof merges the link maps of as many processes as are ascribed to it into one profile set. While the system runs under load, Prof takes the information from all the named processes and generates a merged profile report. Quantum has released Prof in source form to designers, and hopes, according to Hildebrand, they will "begin using it in generic form to begin with and then modify it with the idea of making it an application-specific tool to help more accurately profile that application."

### Who's carrying the load?

Multiprocessor Toolsmiths (Nepean, Ontario) has added multiprocessor analysis capability to its Remedy debugger. Remedy is a part of Toolsmiths' CASEworks/RT integrated CASE environment. The facility lets users look at task loading across all processors on a task-by-task basis. Thanks to the integration in the CASE environment, according to Toolsmiths' president Kim Rowe, "If you want to redistribute the load, you just drop into the CASE tool, change the processor number of a task, rebuild and that's it."

This CASE tool, called OnTime, provides graphical hardware specification complete with software configuration parameters and switch settings. Users define the hardware architecture using off-the-shelf boards, user-specified boards, buses, disks, tapes, networks, backplanes,

and other basic elements. From this graphical description, users can automatically generate documentation on a mixed multiprocessor runtime environment. To add a board, the user selects the board type, fits it into the memory map, specifies the software environment, and regenerates the system (by setting switches and physically inserting the board).



*Alfred Chao of Software Components Group feels that current debuggers are not adequate for real-time multiprocessing. "If you're treating the multiprocessor as a system, as a black box, you want to get an overview of the status of the system at any given time."*

To tailor application software to the new board, the user simply moves tasks to it by changing the processor number in the graphical software architecture and regenerating the application. Downloading, testing and measuring performance are done using Remedy's mixed multiprocessor measurement tool that's described above.

Modcomp has developed a tool to analyze the loading of an asymmetrical multiprocessor system and give the developer a command interface to quickly change the loading. The Application Worksheet presents system information in a spreadsheet format. A monitor menu lets the user view the performance of tasks as they execute on different processors in the system and also view the loading of individual CPUs. A build menu is used to import and edit files, compile and link programs and assign tasks to processors.

The Application Worksheet also includes a scheduler with a menu

the designer uses to create simple or complex schedules. A task, for example, might be required to trigger on completion of some other task, or a given interrupt handler might be required to complete within a certain time. The Application Worksheet can see that all tasks finish within their deadline. Finally, a control menu provides an interface to the software debugger environment.

According to Modcomp's Furht, the Application Worksheet can be used during development to experiment and see that all processors are evenly loaded and none are overloaded. During system test and operation, it can be used for monitoring the system in the real world. "The program dynamically sees what the load is on your processors," says Furht. "It sees the changing dynamics and on the basis of this you can change the load on the processors."

### Debugging multiprocessors

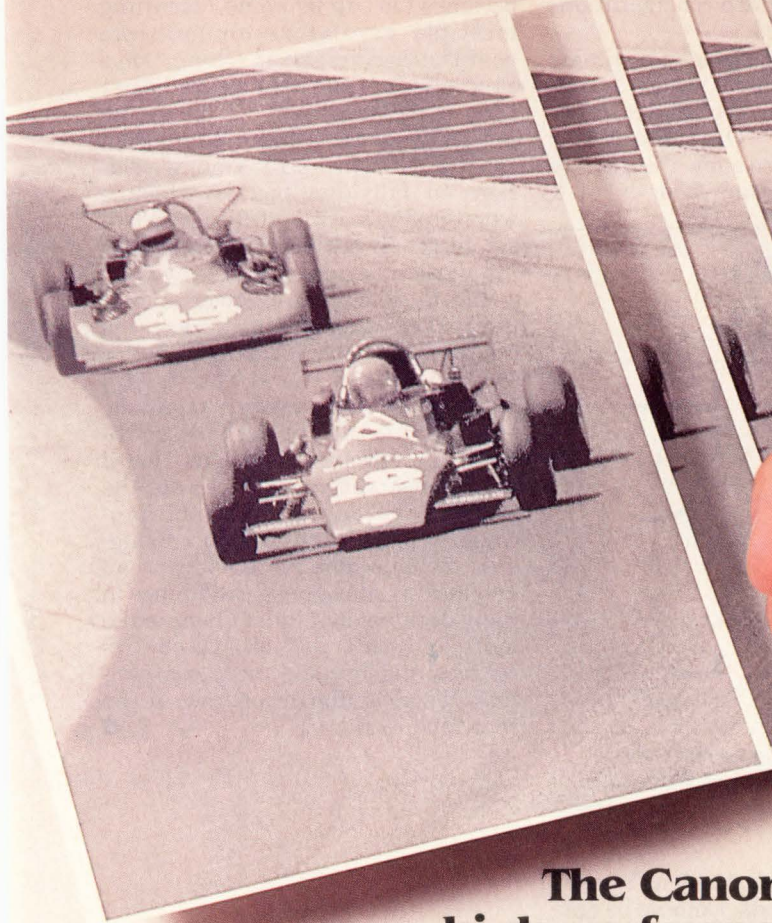
Determining what people want to see is one of the factors to be decided in debugging multiprocessor systems. As yet, there's no consensus on this. On one side are those who want a global view of the system state such that when a processor hits a breakpoint, the state of the whole system is frozen. This is a very tall order and not currently possible. So, for the time being, even debuggers aimed at multiprocessor systems can halt execution on one CPU, but the others go merrily running on. To SCG's Chao, "That's like stopping one wheel on an 18-wheeler—a lot of screeching." Tovey Barron, senior technical marketing engineer for 80386 and 80486 products at Intel (Hillsboro, OR) adds, "It's like saying this wheel's OK, then that one's OK and then you try to run and the thing falls apart because you forgot about the differential in between."

On the other side are those such as Inmos' Diaz who says, "With a multiprocessor system, it's difficult to define what the state of the system will be, based on a breakpoint for any given processor. You may be looking for a certain relationship but there may be a lot of other things going on as well." What you're really looking for are relationships between different events. For example, if something happens on processor B, what triggered it? An outside interrupt or a bug on processor A? Or was it a relatively rare combination of conditions?

Currently, multiprocessor debugging works well at debugging the



# 0 to 17 in 60 seconds

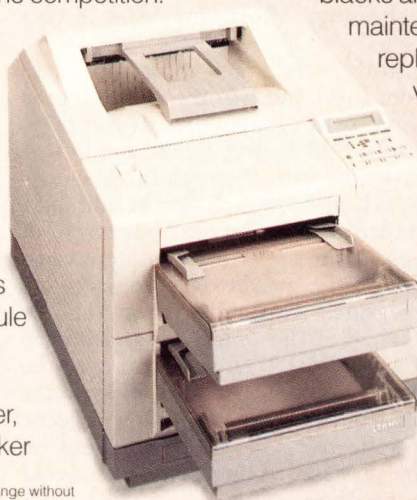


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CIRCLE NO. 43



## REAL-TIME MULTIPROCESSING

logic—algorithms and communication semantics—of programs. It really falls down on timing relationships between processors. Precise, for example, supplies a debugger called Precise/MPD for multiprocessing. It consists of two parts: one runs on the host, the other runs as a distributed application on the target system. A debugger main task communicates with agent tasks running on each processor node in the system.

The main task is in constant com-

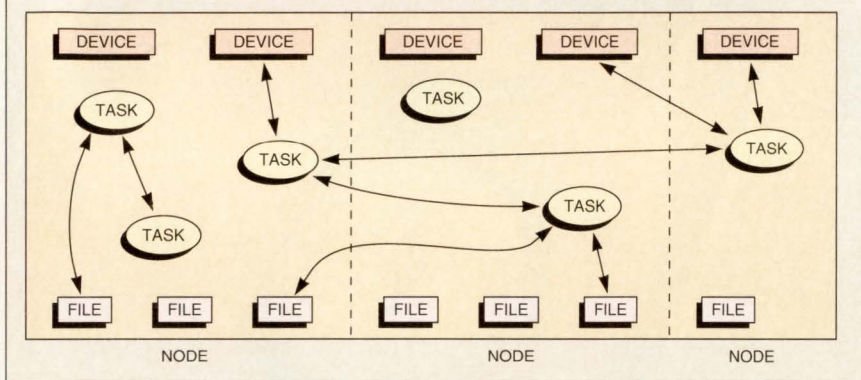
platform. At that level, the user can reliably develop and debug the logic and communications semantics of the application. Moving the application over to the target architecture, of course, involves the task assignment and bandwidth considerations discussed earlier.

So what about debugging timing relationships? That's where things can get difficult. Toolsmiths' Rowe says currently, "Our solution is geared to measure a few things. Say I need to know that from event X

That might be of some use for two or three processors where you're looking for a relation between specific events, but when it comes to trying to see the big picture on six or eight processors, the whole idea becomes too cumbersome. "Running multiple emulators on multiple boards doesn't mean anything," says Precise's James, "because you can't time-correlate them." There's no system-wide time base. Emulation can be used to verify timing relations on individual boards, which is where today's prudent designer will try to group teams of tasks whose interaction is time-critical anyway.

The push for more power is definitely a push for multiprocessing and designers are certain to follow the demands of users. There's still much to be done, however, to provide tools giving designers full confidence in optimized designs. Until then, conservative practices are the order of the day. But as multiprocessor-oriented analysis and debugging tools become more widespread and mature, designers' confidence in their designs should let them make more efficient use of system resources and become more competitive. It's all a matter of time in the real-time world. ■

### QNX operating system on multiple processors



When used with a multiprocessor architecture, the QNX operating system from Quantum Software appears to be a single computer consisting of tasks, files and devices. Boundaries between nodes are almost invisible thanks to the high-level inter-process communications in QNX.

munication with the host. It interprets all commands from the host, lets the user set breakpoints on the different processors and lets the user observe different nodes at the same time through windows on the host. Precise's James says, "We often encourage our customers to put an extra processor on their system to run the debugger main task. It's a promiscuous agent and looks at all the data by talking to the agent tasks."

The more development and debugging that can be done on a host workstation, the less one has to worry about the intricacies of doing it on the multiprocessor target. That's the advantage of having a transparent view of the hardware via high-level IPC interfaces, such as sockets, and a multiprocessing operating system such as Lynx/OS, QNX or the Unison flavor of Unix supplied by Multiprocessor Toolsmiths. Toolsmiths also provides a package called Copycat which emulates the Unison system on the single-processor host development

through the system to event Y needs to be *n* milliseconds. I should be able to measure that." Rowe sees coming improvements in the ability to measure things such as response time, throughput (CPU utilization) and to capture system state information—the big picture. "But," he notes, "I don't think in-circuit emulation technology offers anything in this area."

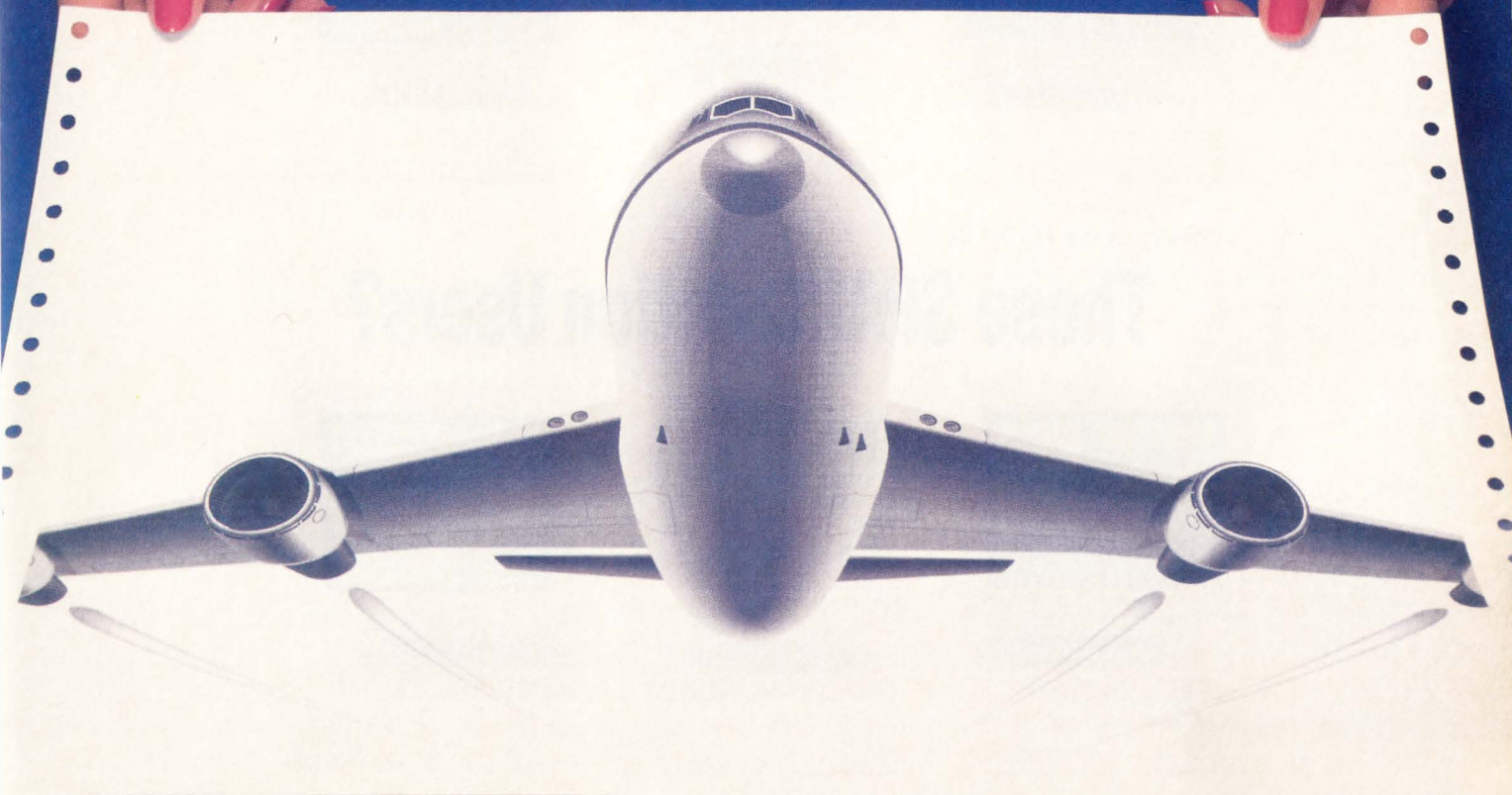
Rowe would get some argument from Intel, but has the agreement of most other software developers. Intel's 80386 and 80486 emulators have two sets of synch lines each—Isynch and Osynch (for in and out). According to Barron, one can "at least from the ICE standpoint, designate one emulator as master and the other as slave by hooking the Osynch of the master to the Isynch of the slave." The system may be treating the processors differently, but the ICEs are set up to see some specific relationship of an event on one processor triggered by an event on another.

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# Designers look beyond DIPs to meet application needs

*While the DIP will be in widespread use for quite some time, it's clear that applications are driving package selection. Designers are no longer settling for the old standbys.*

Jon Gabay  
Contributing Editor

It used to be that system design decisions were based on the best choice of standard packages. As applications became more demanding, device manufacturers kept pace with the needs of volume customers for cost-effective solutions. Engineering managers with vision realized early that smaller is better. The IC industry responded and made surface mount a reality with small outline (SO) packages, SOIC (small-outline ICs with leads bent out) and SOJ (small-outline J-lead with leads bent in). These were standard parts whose package sizes shrunk to accommodate surface mount leads. As such, they often retained the same pin outs and shape of the DIP counterpart, but used less space. This was a logical evolutionary step and was a comfortable transition for most engineers.

The resulting shrink of pin spacing, from the standard 100 mils down past 50 and now to about 25 mils spacing of SO devices, gave a boost to designers working under space constraints as well as providing density increases of 4x. Surface mount is commonly in use today and SO devices are still being made, such as the Quarter-Sized Outline Package (QSOP) from Quality Semiconductor, (Santa Clara, CA). These fast CMOS TTL logic devices replace 20- and 24-pin SO devices, saving 75 percent in space over other SOIC devices. The shorter size is useful in eliminating ground bounce usually associated with Fast CMOS Technology (FCT) devices.

The quest for reduced size isn't limited to just printed circuit board (PCB) area. Package height is also important in many demanding applications. Competing for present and near-term surface mount applications are three package types: the LCCC, the PLCC, and the PQFP. The advantages of these packages are higher pin counts than otherwise possible with DIP-



*IBM plans to use these modules to provide higher performance desktop RISC 6000 machines. The package is a joint venture between IBM (Yorktown Heights, NY), the Advance Workstation Division (Austin, TX) and the YASU Technology Applications Lab (Tokyo, Japan).*



## BEYOND DIPs

and SO-type packages, high density, reduced thicknesses, and good thermal characteristics. A family of cache RAMs from Micron Technology (Boise, ID), for example, presently boasts the smallest footprint and lead spacing. These 52-pin PQFP devices use 10-mil spacing, resulting in a package with a 40 percent smaller footprint than a 53-pin PLCC, the current industry standard configuration for cache RAMs.

While surface mount benefits are numerous, the pin grid array (PGA) package is still the most widely used for high-pin count ASICs and standard parts. A 32-bit processor, for example, may provide 32 address bits, 32 data bits, and separate 32 bit buses for cache and global resources. A PGA package is the most economical package to accommodate these pins in a typical manufacturing environment. This is especially

true since many times the micro-processor must be socketed to give circuit emulation and other debug tools access to the system.

Presently, the PGA is the most common, low-risk, through-hole package in use. But it's costly and it takes up a lot of space. The ceramic PGA package will continue to be a feasible (but a cost-prohibitive package type) for designs both now and in the future, especially in light of PGA advancements, such as the low profile 280-pin PGA that Seeq Technology (San Jose, CA) has introduced. Designed for military applications, the EEPROM parts from Seeq range from 16 to 256 kbits and feature a low-profile package which hermetically seals the die in an aluminum ceramic package with a gold-solder seal lid.

Designed to take high mechanical shock and stress, the package is being submitted to JEDEC and many designers hope it will be adapted by DESC specification 38510. The low height of .141 in.

above the printed circuit board (PCB) along with the small  $\frac{1}{2}$ - $\times$ - $\frac{1}{2}$ -in. package reduces space consumption 40 percent over an equivalent DIP package.

Other PGA packages demonstrated they can handle complex designs while dissipating heat effectively. Heatsinks for PGAs are becoming more common, and even Peltier effect device sockets are available to cool chips down to 0°C.

Of course, at over \$50/cooling unit, this becomes expensive; but

power dissipation capabilities of the PQFP (around 1.2 W). What's more, 50-MHz operation is safe with the PQFP, 80 MHz with a little care, but above that, the package has problems.

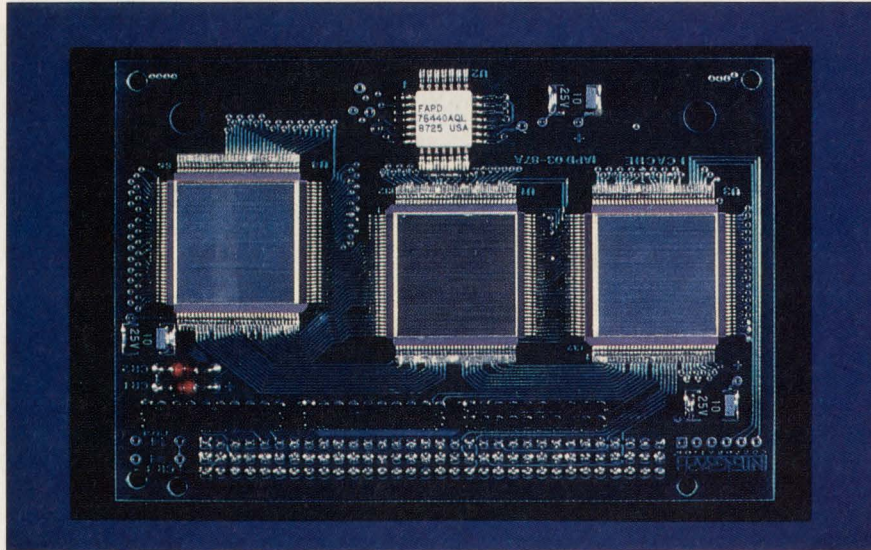
As a result, the PQFP is currently the industry workhorse, getting more new designs than any other type of package in use today. The 50- and 25-mil surface-mount PQFP achieves higher density, can have more pins, and is much lower in cost than a comparable PGA package.

One possible successor is the QFP package made of other materials. Aluminum QFP packages conforming to the JEDEC standard are starting to roll out. While they still may be a bit more expensive than plastic, they offer good heatsinking and thermal dissipation. Vitesse Technology (Camarillo, CA) offers the aluminum QFP for its high-density gallium-arsenide

arrays to overcome the thermal problems that can crop up in 30,000- to 50,000-gate designs.

The JEDEC package has advantages over the Japanese EIAJ standard, but the JEDEC package has been slower to emerge. Most engineers feel the JEDEC package is superior and will win out in the long run for two reasons. First, the JEDEC package has alignment bumpers, making it easier to manipulate them in auto insertion machines. Secondly, pin straightening is a problem with the Japanese packages. Without bumpers, QFP surface-mount devices move around in tubes so much that the finely-spaced leads get bent out of shape and are difficult to straighten, putting a crimp in the manufacturing process. The bumpered JEDEC packages, on the other hand, live in tubes without developing deformed pins.

Regardless of the status of flatpack surface-mount packages, I/O signal density is reaching its



The early C100 Clipper Module gave Fairchild (now Intergraph) a small, high-performance core processor to power its advanced workstations.

then again, this is an elaborate solution. There are other workarounds for heat absorption through proper selection of heatsinks, either on top of the package or embedded into the package as a slug. In addition, multiple power and ground pins can act as thermal transfer points to the (usually) thick power and ground plane traces.

But these solutions aren't optimal for all applications. First of all, heat sinks are expensive and add another step in the production cycle. Also, heatsinks add a lot of volume to the design which means those tight-fitting circuit boards won't stack as originally intended. Many designers are "pad limited" because there may not be more space on the board to add redundant power and ground pins. So what's the solution?

### Flat is where it's at

The PQFP is replacing the PGA in many applications, but in the long run, the PQFP may be in trouble. This is primarily due to the limited



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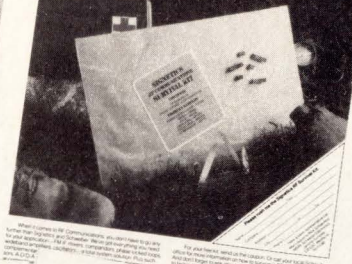
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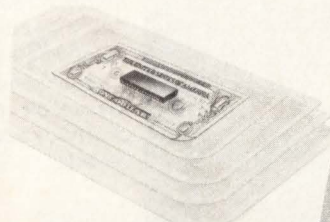
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## BEYOND DIPS

limits. Most feel that 208-pin QFPs can only go to about 256 pins in the future before the QFP tops out. It's only feasible to bring I/O pad pitch down to a point before physical limitations come into play. While most common is 7-mil pad pitch, 4 or 5 mil is about the state-of-the-art and

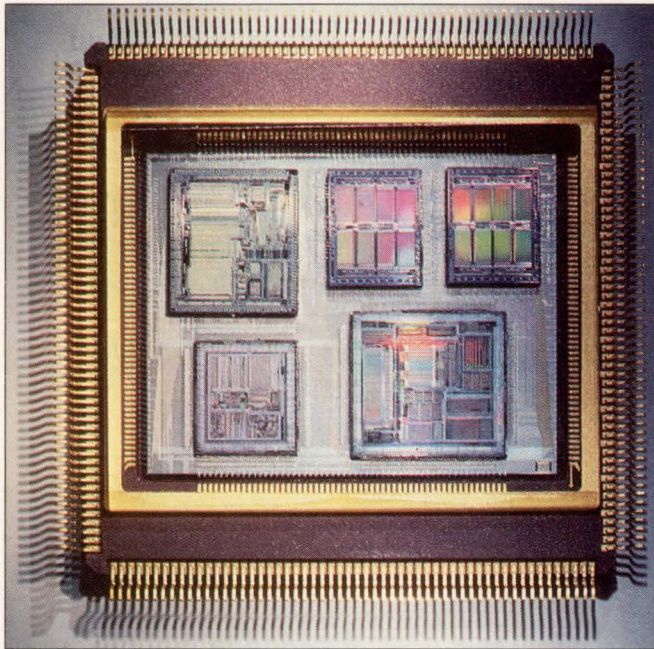
Although not available to the general public (yet), the groundwork has proven successful for future fabrication of very dense ICs.

In a collaborative effort between Motorola and TRW, the .5 $\mu$  CPUAX SuperChip has successfully been fabricated and tested for military

bonded ICs can contain more I/O signals, store-and-ship on a spool, and adapt to automated production facilities.

"Unfortunately, TAB is only available to those who have deep pockets," continues Homstad. "The smaller IC companies can't afford to invest in TAB, at least not until the price comes down." Regardless, TAB is catching on and it will be the standard as far as high-density IC's are concerned. "By the mid 90's, we should see packages with 1,000 pins or more which are not quite possible with today's level of technology," says Bob Bailey, ASIC product line director at AT&T Microelectronics (Allentown, PA).

Nevertheless, standard parts which must be small and heat worthy are breaking new ground. For example, Mitsubishi (Sunnyvale,



*This five-chip module from Ross Technology (subsidiary of Cypress) houses a Sparc CPU, a floating-point unit, a cache controller/memory management unit, and two cache SRAMs.*

what's feasible before substrate bonding techniques make this unreliable. Since the pads can't get any smaller on the substrate itself, what's the next step? One answer is to make the substrate larger. Another is to use tape-automated bonding (TAB) to allow smaller interconnects.

The idea of making the die larger isn't new. Using an entire wafer permits many more I/O than possible with a single die, and, ideally, permits systems on silicon to take place. It was tried quite vigorously by Waferscale Integration (Fremont, CA) several years ago. The real problem still is reliability and manufacturability. While economically feasible wafer-scale ASICs never came to fruition, some fallout from the attempts has contributed to the present state-of-the-art.

While advances have been made that let redundant circuitry structures exist within the wafer, most feel a trade-off is still too costly to justify wafer scale integration unless it's absolutely necessary. One good example of redundancy appears in a chip manufactured by Motorola (Austin, TX) and TRW (La Jolla, CA) for military applications.

Containing  $4 \times 10^6$  discrete devices, the SuperChip can perform 200 MFlops (32-bit). The air-cooled 17-W CPUAX measures only 2.1 in.<sup>2</sup>, and weighs only 1.5 oz.

Although quite an accomplishment, this phase 2 VHSIC success is only the start. The design team plans to build chips 150 $\times$  as dense as the DOD continues to help push the state-of-the-art, which will eventually manifest itself as commercially available technology.

### The bond issue

While the ability to make larger and more sophisticated die is evolving, so too has the ability to mount die onto a substrate and into a package. A technique that has slowly been gaining steam is tape automated bonding (TAB) which promises higher densities and pin-counts.

"TAB is like a mechanical amplifier," states Jerry Homstad, vice-president of design engineering at Gould AMI (Pocatello, ID). TAB uses a flexible interconnect film which resembles a 35-mm slide. The PCB on the film bonds to the die via bumps. The gold interconnect is simultaneously connected with the package. As a result, the TAB-

***While advances have been made that let redundant circuitry structures exist within the wafer, most feel a trade-off is still too costly to justify wafer scale integration unless it's absolutely necessary.***



CA) offers TAB-bonded PGA and QFP devices which support the company's .8 $\mu$  CMOS process. Designed for frequencies up to 100 MHz, the packages use wire-bonding technology to achieve pin counts of about 300. More than 350 pins can be achieved using TAB bonding which takes advantage of very-fine lead pitch in a small footprint. The .25-mm external lead pitch can stack 576 pins in a 40  $\times$  40-mm package and dissipate up to 3 W without a heatsink. Using a heatsink, the package can dissipate 22 W.

Of interest is the fact that TAB can be used in conjunction with other high-density packaging schemes to help make an ultimately high-density package with a reduced overall pin count. This is



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what we are seeing with the cavity and multichip modules (MCMs).

## MCMs

While ASICs helped put PCBs and card cages on a single chip, this is often not enough. Today, core processors, peripheral functions, mixed analog and digital, memory, power functions, and even interconnect must be integrated in the tightest possible space.

ASIC vendors are striving to make this possible, but are still limited by real world trade-offs and constraints. The chip areas are still

others have had to pioneer many of the technologies to deliver a system in its most compact, rugged, and reliable form. In the nose-cone of a modern anti-ballistic missile, for example, it's obviously infeasible to put a card cage. Instead, a circular 5-in. ceramic MCM controls the target acquisition, tracking, navigation, inertial response and guidance, as well as commands from a host of ground, airborne, or shipboard control systems. Here, it's the ability to produce such modules which makes the entire weapon system a reality.

MCMs provide benefits in several

MCMs. The result is a chip that looks like a regular IC which is actually composed of many IC's in a small form factor.

Third, is that hybrid houses have been effectively making MCMs for a long time, meaning the facilities are in place, and the technology is not pushed to accomplish reliable circuits. As a matter of fact, many silicon (and gallium arsenide) vendors have been customer-driven into MCMs and often the customers are farming out MCM fabrication rather than getting packaged chips from the ASIC houses. Many say MCMs are the wave of the future, especially for systems manufacturers who need the high performance and integration offered by MCMs.

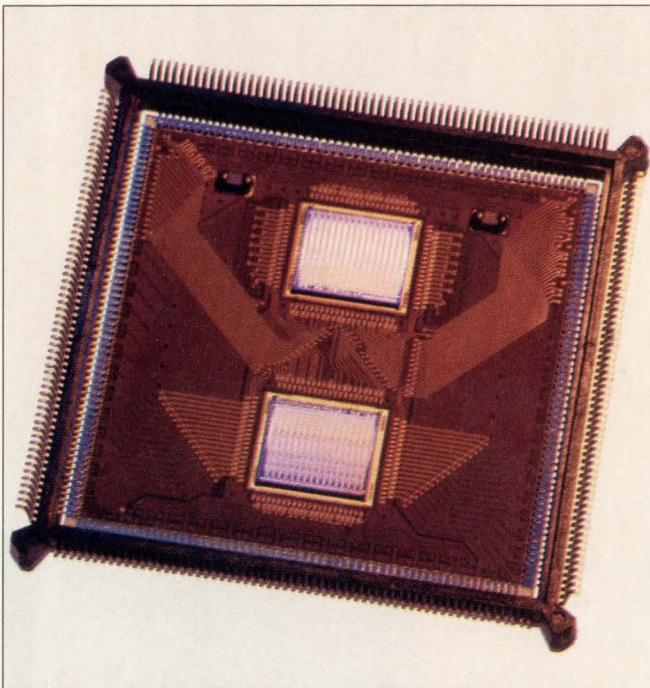
Another problem solved by MCM is thermal dissipation. "We've seen the ability to remove 600 W of power from MCMs using a standard muffin fan. Companies like Alcoa are pioneering materials to help address this need so that fast designs can take advantage of smart thermal designs," according to Jack Vandenhevel, marketing manager for ECL ASICs at Raytheon (Mountain View, CA).

Modern-day system designers strive for the highest functionality in the least area at the best cost. Trade-off factors such as power dissipation, manufacturability, yield, cost of rework and repair, and others come into play, but, if a company decides that the performance and size are critical, all the other factors are simply facts of life that must be dealt with.

While the average project is not nearly as critical, many times it's the added edge that advanced technology brings to the party that makes the difference in its acceptance into the market. For example, the race continues today to bring the smallest footprint, highest-performance desktop computer to engineers and scientists.

The Clipper chip set (originally from Fairchild, now part of Intergraph [Huntsville, AL]) was among the first of the highly integrated solutions which gave Intergraph an early advantage since its workstations benefited from the multi-Mips small-footprint processor.

More modern use of MCMs for compute-intensive tasks includes the Sparc RISC CPU from Ross Technology, a division of Cypress Semiconductor (San Jose, CA) and the Mips RISC processor module



*The Polyhic process from AT&T uses stronger ceramic substrates which are capable of holding I/O interconnects directly.*

limited, design constraints which force partitioning of functions and circuits may point to chip sets instead of single-chip solutions, and worse yet, the development tools for single-chip system-level design, debug and manufacture are not geared to handle the circuit densities, power, thermal, mechanical, and other disciplines needed to make this approach work.

For a long time, hybrid manufacturers have addressed a portion of the need but have been limited to smaller, more special functions, as opposed to system-level implementation. MCMs have been a solution for the elite few who had the resources and capital to make this technology work.

Military contractors such as Texas Instruments, Rockwell, Hughes Aircraft, Raytheon, and

ways. First, MCMs help increase reliability because they eliminate the stress that would otherwise occur when large chips are mounted in packages. Rather than fabricate a single super-dense IC, it becomes feasible to fabricate a few less-dense ICs mounted in an MCM which could have a significantly reduced I/O requirement because of the high integration. This means that testing each less-dense IC is easier, the packages are less demanding, and, hopefully, yield will be higher since the same number of wafer hits will be distributed among many more die.

Second, MCMs can mean higher performance since signal lengths are limited in distance. Technology is to the point where 50Ω channels are easily fabricated on the silicon or ceramic substrates used for



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**MOTOROLA**



## BEYOND DIPs

from Integrated Device Technology (IDT) (Santa Clara, CA). The latter's IDT7RS101 is a complete RISC computer module based on the company's 79R3000 microprocessor. Included on the module are read/write buffers, dual 64k cache memories (one for instruction, one for data), 1-Mbit SRAM, a debug ROM monitor, two serial ports, a counter timer, and an optional 79R3010 floating-point processor. Available in 12-, 16-, 20-, and 25-MHz speeds, the modules are packed in double-sided FR-4 glass epoxy laminate and measure  $3.7 \times 6.55$  in.

MCMs are manifesting themselves in two basic forms: ceramic and silicon substrates. The type of substrate governs the type of performance, strength and interconnect options that will be available. While silicon is more brittle than ceramic, it has roughly the same coefficient of expansion as the chips mounted on it. This reduces stress caused by thermal expansion. Also, since silicon is a better thermal conductor (by a factor of 3), it can transfer heat more easily to a heatsink.

Conversely, silicon is too brittle to mount I/O pins directly and while ceramic is brittle, it has the tensile strength to hold I/O pins and connector leads directly. Generally, silicon is best for matching thermal expansion while ceramic is better for mechanically stronger devices. An exception to this is with ultra-high-performance and high-speed designs where the ability to use gold traces and contacts helps match transmission line impedances. Here ceramic is more robust and flexible since tungsten, copper, aluminum, gold, and other elements and alloys can be laid down to match the application.

Silicon is easier and cheaper to produce and older existing fab lines can easily handle the 10- to 15-mil traces needed to interconnect chips. This was a primary reason IBM chose silicon as the substrate for the MCM desktop modules in its RISC System 6000 model 540 and 320 computers. The nine CMOS chips housed on the

4.5 in.<sup>2</sup> substrate reduced the original 56 in.<sup>2</sup> design by a 12 $\times$  factor.

Integrated on the single substrate are floating-point, fixed-point, instruction cache, memory-management, and data cache chips, and I/O control. The MCM presently uses 256 I/O lines but can handle 512 signals with pin counts as high as 684. Bound by flip-chip process, IBM will be using these modules in newer versions of its RISC 6000 system computer.

An interesting development for silicon MCM substrates is the idea that substrates can be manufactured and customized later, similar to gate arrays. This is happening with the Microelectronics and Com-

VLSI chips and 103 I/O lines. Kodak, too, has used this technology for memory modules which attach several MCMs on a single substrate.

## A vase or a VAX

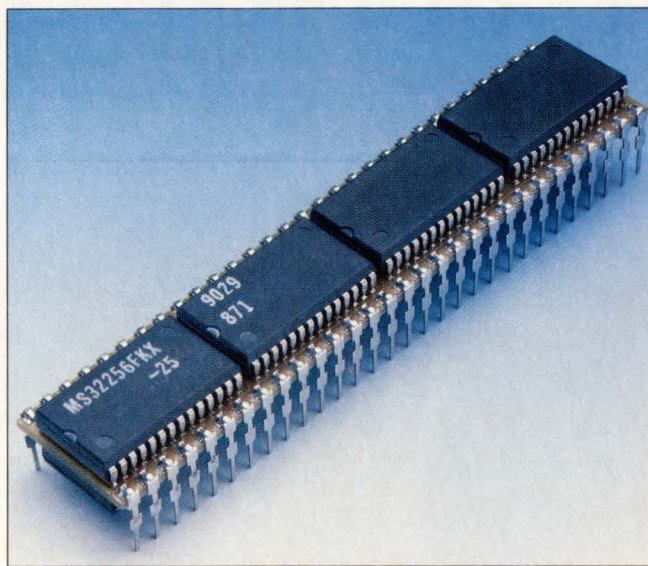
AT&T is a driving force behind ceramic substrate MCMs and has built several designs on these foundations. Its Polyhic process uses thin film circuitry isolated from the ceramic substrate by a proprietary polymer film. This permits fine line conductor widths (2 mil with 3 mil spacing), small vias (6 mil), reduces noise, and keeps dielectric losses low, even at frequency ranges into the GHz.

An advantage to the Polyhic approach is the substrate can house transistors, diodes, capacitors, inductors, and other chips that can mount with wire bond, epoxy bond, thermal compression, or solder. The substrate can handle 90 V and operate from 0 to 120 V<sub>ac</sub> and provide line impedances from 50 to 80  $\Omega$ . Already in use, the Polyhic substrate has been used to fab a 200-MHz, 244-pin JEDEC module and other designs in the works push this even further.

Other ceramic foundations were developed through research by Cherry Semiconductor (East Greenwich, RI) and Sheldahl (Clarkston, MI) which have pioneered a flip-chip bonding scheme on a flexible substrate. Material technology from Sheldahl combined with ASIC technology from Cherry is promising to deliver substrates that can be wrapped around other devices. The flip-chip mounting uses reflow solder techniques to attach tin-lead bumps to chip die.

One company helping to pioneer the ceramic substrate is nChip (San Jose, CA). It's developing three substrates for different applications. The company's substrate is designed for CMOS applications and handles 50-MHz designs quite comfortably. Aluminum interconnect is used to reduce cost and the substrates easily mount 25-mil-pitch chips.

The other two substrates are termed the C and E types and are aimed at higher-speed applications. Both substrates use copper interconnects and handle mixes of



*Custom and semi-standard memory modules have made Mosaic Semiconductor well-known for its innovative packaging. Mosaic modules are finding their way into high-performance compact systems.*

puter Technology (MCC) consortium (Austin, TX) which has developed a quick turnaround interconnect approach. By manufacturing a substrate which contains power and ground planes, horizontal and vertical routing lines, and contact planes, one to three custom layers is all that's required to make a new substrate for a new application.

Because the designer specifies the bond areas, TAB, wirebond, flip-chip, and combined bonding techniques can be used. Also, because of the power and ground plane structures, the substrate can attach CMOS, BiCMOS, ECL, and GaAs substrates on one floorplan. Harris/GE has already used this technology to create a crossbar switch that operates at 70 MHz and uses 16





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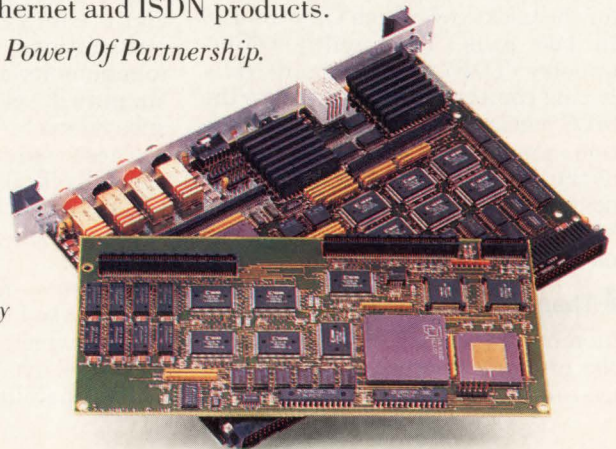
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## BEYOND DIPs

CMOS, BiCMOS and ECL components running at 100 MHz. The E substrate also supports flip-chip mounting where bonding leads are eliminated because the die is mounted upside down on solder bumps on the substrate.

The clean electronic characteristics available with ceramic substrates are not new to companies whose charter in life is speed. One such company, Triquint Semicon-

### **Memory devices are an exception to the pricing structure of devices and systems that take advantage of state-of-the-art packaging.**



ductor (Beaverton, OR), has been using ceramic substrates for its GaAs standard products and ASIC designs for some time.

Just as matched thermal-expansion characteristics for silicon chips on silicon substrates are important, so is the matching of ceramic substrates to the ceramic packages the company has developed specifically for ultra-high-speed GaAs chips. At speeds of 5-GHz digital, 1.5-GHz analog, with raw clock speeds up to 18 GHz, effects that are otherwise negligible at lower speeds in silicon manifest themselves. As a result, Triquint's multilayer ceramic packages (MLCs) were designed to deliver clean performance at high speeds.

When operating at such high speeds, a baseline performance had to be established. This is why Triquint also provides test fixtures for the packages, which vary from 20 to 196 pins. Time delay reflectometry (TDR) measurements comparing commercial packaging to the MLC packages show a 2.5x reduction in noise and distortion. Because of the MLC packages, Triquint has no rebuffs to its claim to have the highest-performance, highest-speed package to date.

### Thanks for the memory

Memory devices are an exception to the pricing structure of devices and systems that take advantage of

state-of-the-art packaging. Memory devices and modules are also pushing the state of high-density packaging because of an inexhaustible appetite for dense memory and stringent requirements for high-speed cache memory.

Because of the high volume, the price for these modules is less than system-level modules. Examples of these package types include SIPs, ZIPs (zigzag inline packages), and custom packages from Mosaic Semiconductor, NEC, Cypress Semiconductor, Oki Semiconductor, and Electronic Designs Inc (EDI). Often times, memory modules don't fall into the MCM category, but they do push packaging densities further than possible using standard packaging.

For example, the EDI EDI83265C modules house 2-Mbits of memory in a 64 by 32k configuration in a 64-pin DIP. Using standard monolithic memories requires 28-pin DIPs eating up 3¼ in.<sup>2</sup> while the EDI modules take up only 1.2 in.<sup>2</sup> of board space. Likewise, the SIP modules from NEC and TI have helped standardize the memory module expansion in most high-end PC's and the raw volume has kept pricing competitive with larger discrete chip solutions taking up much more board space.

### Power to the people

An area that benefits greatly from MCM technology is smart power and energy management. Limited MCM and hybrid technology is common inside stereo amplifiers, VCRs, disk drives, and similar products. It's these combined power devices which are mostly responsible for the compactness of VCR cameras and the lower cost of newer systems.

When power-control devices are integrated within the module, a small, rugged, highly integrated solution paves the way for more efficient energy use, smaller communications elements, increased functionality in smaller space, and simplified assembly of systems and subsystems.

These could be power drivers and specialized power control devices like triacs, SCR's, high-voltage transistors, high-current drivers, and more.

Motorola, for example, has demonstrated its 100-V BiCMOS process which combines a microcontroller with high-voltage power drive capabilities. Using 32µm, 10-

MHz CMOS logic, the process permits 32 simultaneous 25-mA outputs to be driven at a 600-kHz rate with 100-V loads.

As part of a project aimed at determining the feasibility of MCMs in the automotive industry, Z-Systems (Santa Clara, CA) has developed an intelligent power module for evaluation. Using a silicon substrate, the module uses three levels of metal integrating power diodes, thin film resistors and capacitors, and, of course, silicon chips including a core 68HC11 microprocessor, analog conversion circuitry, 50-mV FETs, 10-A regulators, filtering, 10-kV ESD protection, and 200-V power isolation. ■

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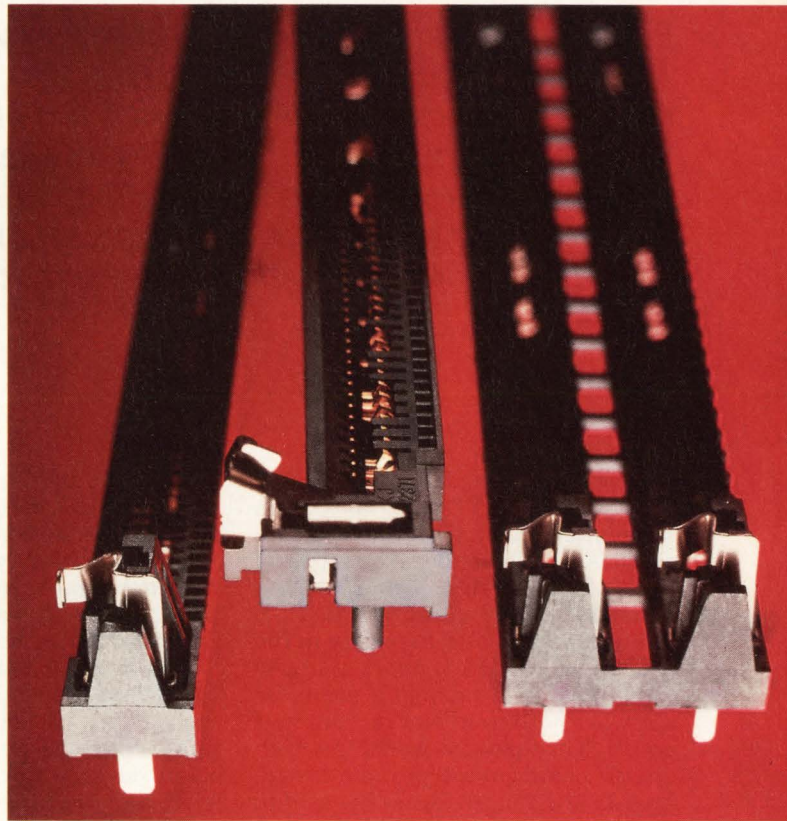
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# Mixed-signal board designers resist the siren call of simulation

Mike Donlin  
Senior Editor

*EDA vendors are developing tools that will let engineers simulate the behavior of mixed-signal circuit boards before the prototype stage. The question remains, however, whether board designers are willing to trade in their trusty prototype debugging methods for waveforms on a workstation display.*

**T**he story of mixed-signal printed circuit board (PCB) and system simulation is rife with the promises of EDA vendors, the skepticism of circuit board designers and resignation from both camps that PCB simulation will be a necessity in the near future. EDA vendors claim to have tools that provide a seamless software path from concept to circuit board. They paint a world in which circuit board prototypes and breadboards are a mere formality, as if to suggest that the real world of traces, integrated circuits and backplanes are a simple confirmation of what their software has already neatly predicted. To not invest in such electronic clairvoyance, they are quick to point out, is sheer folly.

Circuit board designers, especially those who dwell in the murky realm of analog behavior, represent the harsh realities of electron flow. Their world is a succession of events that get more unpredictable the longer they're examined. To analog engineers, molehills can become mountains if they get close enough, and noise can look like a signal if the Spice is right.

How real, then, is circuit board

and system mixed-signal simulation? ASIC and IC designers have been using simulation for years, mainly because they can't rely on the safety net of a prototype to debug and jumper until their designs are correct. But in the dicey realm of circuit board behavior, it seems the expensive simulation tools of today are reserved for those at the cutting edge of PCB design, while the majority of circuit board designers are content to use tried and true methods of debugging a prototype.

## ■ Need isn't there

"We really haven't run into the need for mixed-signal simulation," says Jim Toy, president of Broadband Communication Products (Melbourne, FL) a manufacturer of high-speed communications boards. "In our products, which can exhibit some pretty wild analog effects, the parasitics are typically the problem. If we know what the parasitics are to begin with, we can usually design around them. If we don't know what they are, we probably wouldn't know enough to simulate them anyway. For the present, we find it easier to build a board and debug it. After all, about

90 percent of what happens we know from the start. The rest of it we learn the hard way, so I'm not sure what we'd get by simulating—it certainly wouldn't be 100 percent."

Testimony like this isn't unusual in the circuit board arena, and even EDA vendors admit that most of their simulation tools have played to a rather elite audience. They hold out the hope, however, that their tools are a market waiting to happen, and circuit board designers will abandon much of the prototype debug stage as clock rates increase and board real estate decreases. As this transition takes place, prototypes will no longer reflect the real world behavior of the final product. After all, say EDA vendors, a 10-in.<sup>2</sup> breadboard can't exhibit the same transmission line effects or timing constraints as the 4-in.<sup>2</sup> circuit board it's meant to emulate. "There are a lot of problems with breadboards," says Wolfram Blume, president of MicroSim (Irvine, CA). "The time and effort to build them will eventually be greater than the benefits they provide. In addition, it's hard to measure current and noise on a breadboard. We present these



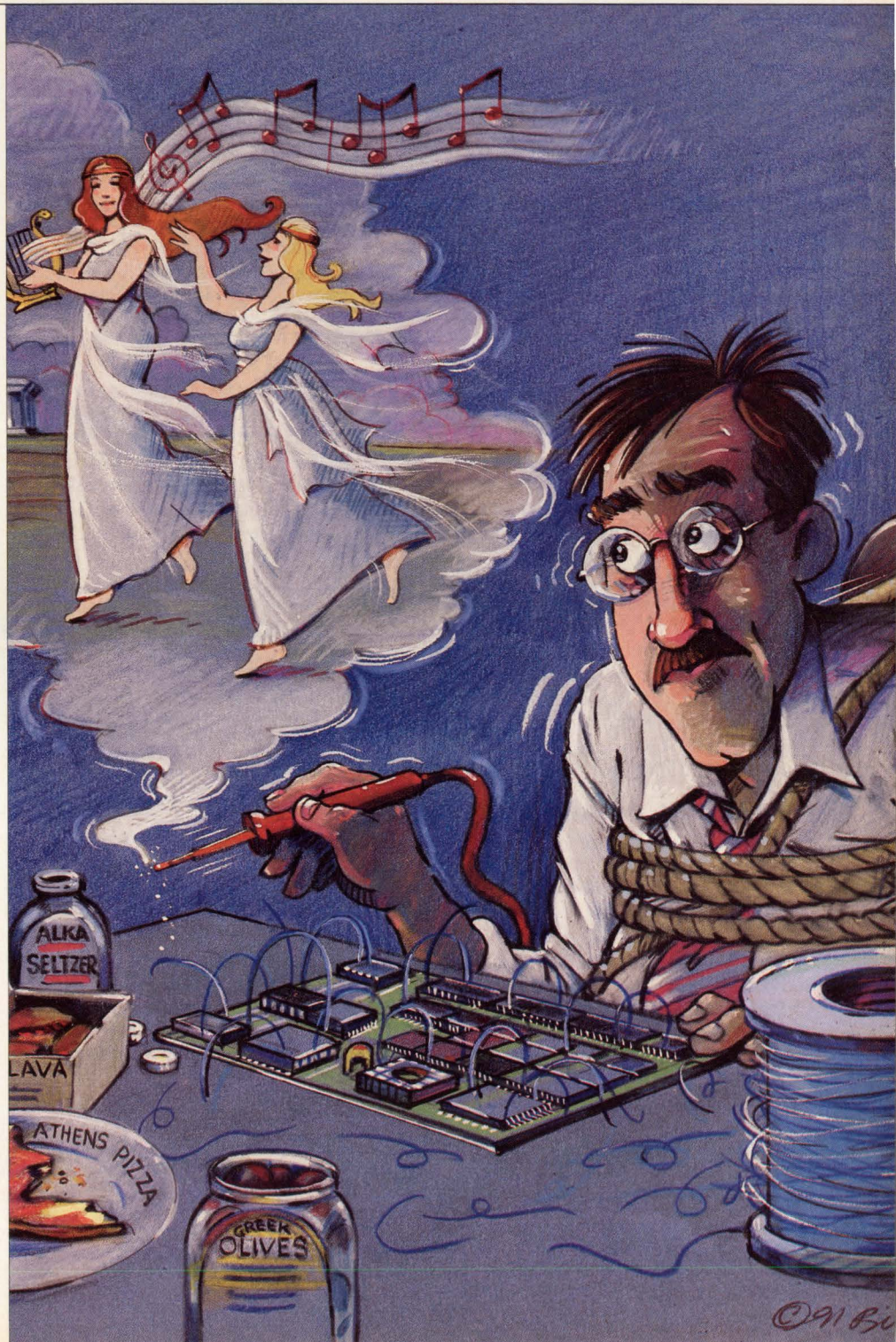
as reasons to do as much as possible in software before prototype.”

EDA vendors and PCB designers alike, however, admit one of the main drawbacks of a prototype is it doesn't show the variances that will occur during manufacturing. The beauty of simulation, they say, is it predicts as many problems as possible across a large cross-section of PCB behavior.

#### ■ Models are key

Reality, undoubtedly, lies in a blending of both simulation and prototype. “I don't see simulation as a replacement for a prototype,” says David Hardman, product planning manager at Logic Automation (Beaverton, OR). “If anything, simulation is meant to be a compliment to the prototype—a tool to develop the most accurate circuit board possible for debugging purposes. It's absurd to think that any designer would go straight to the manufacturing stage without a shot at debugging a hard copy of a PCB.”

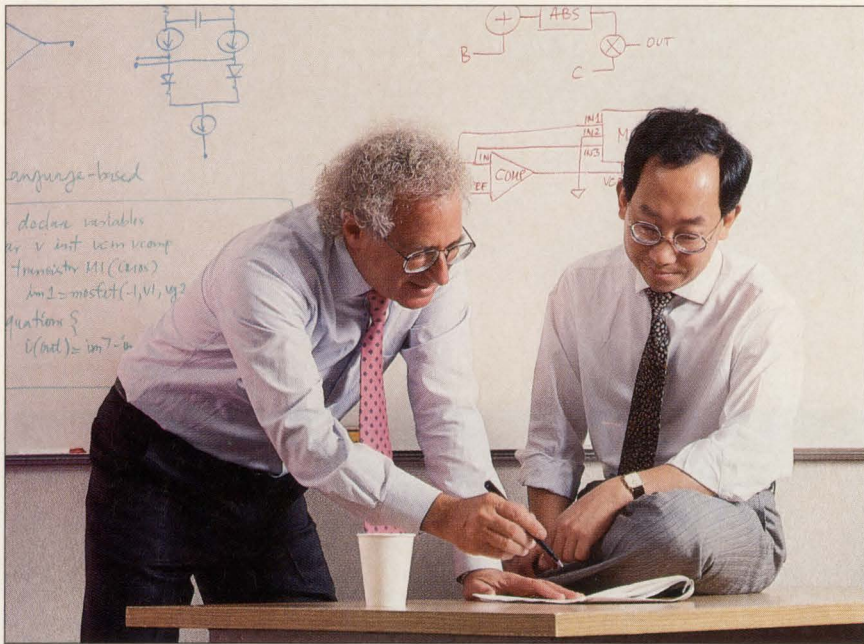
No matter which scenario is right—simulation, prototype or a combination—mixed-signal PCB simulation will remain a tough sell,



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## MIXED-SIGNAL CIRCUIT BOARD



Jim Solomon (left), president of Cadence's analog division and Tom Quan, director of analog solutions, compare the speed, accuracy and ease-of-use trade-offs between the three major approaches to analog behavioral modeling: circuit-based macro-modeling, language-based modeling and graphics-based modeling. "The competing simulators don't really post vast speed differences," says Solomon. "It's the level of modeling detail that translates into simulation speed and accuracy."

mainly because the device models that drive them are either hard to find or lack sufficient accuracy to guarantee a realistic simulation. This is true, not necessarily for standard parts, but for state-of-the-art devices designers want to use for next-generation circuit boards. "Part of the problem is getting models for our leading edge designs," says Joseph Ampulski, hardware engineering manager at Heurikon (Madison, WI). "We've designed a lot of models and developed our own libraries in-house, but getting accurate model information costs a lot of money, time or both."

### Models not a problem

The problem isn't necessarily in obtaining models, but in getting the level of detail that satisfies a particular design's simulation needs. Silicon vendors often have the necessary information to characterize a device's behavior, but they're reluctant to commit themselves to a single set of parameters. "Silicon manufacturers are leery of getting involved with a PCB designer's simulations," says MicroSim's Blume. "The data book specs are what the manufacturer tests and guarantees, but there are always designers who want more information. They ask for things that aren't on

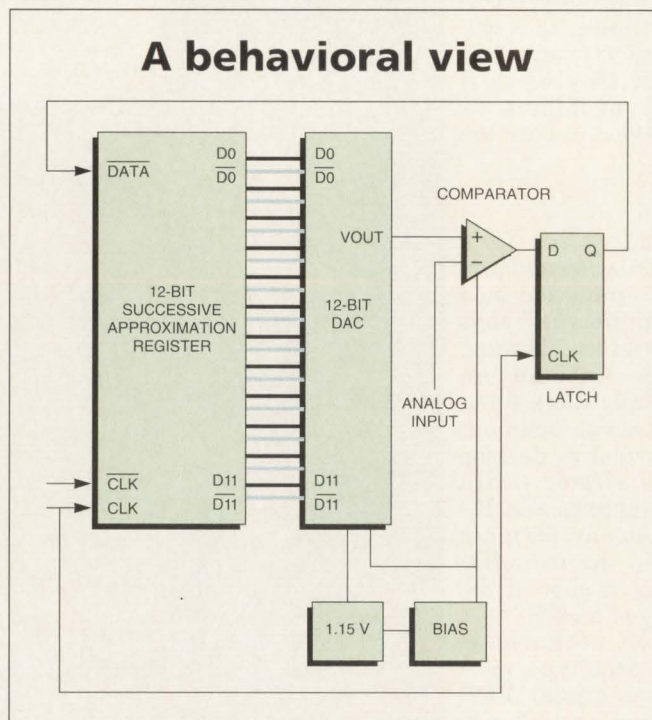
the spec sheet and that puts the silicon vendor in a difficult position. Even if they measure certain characteristics for a group of parts, there's no guarantee that all the devices going out the door will be to that spec. It's far more feasible to provide information that will cover

90 percent of a customer's simulation needs than to go out on a limb and try to guarantee behavior that can vary and wouldn't be of interest to most of the market anyway."

In addition to model availability, another question plagues the engineer who explores the uncharted waters of mixed-signal simulation—at what point does a design engineer trade accuracy for simulation speed? For system verification, behavioral models will suffice to qualify a design for further execution. When designers get down to actual circuit simulation they must make decisions about what level of intricacy is sufficient. Too general a specification can result in inaccurate simulation, while a too-detailed model, particularly on the analog side, can take days to run. Some vendors have produced behavioral models in Spice which they claim provide adequate accuracy, but with less of the time penalties high levels of detail require. Even in the relatively simple world of behavioral models, however, vendors disagree.

### Differences in models

"A lot of Spice vendors claim to have behavioral models," says Prasad Subramaniam, supervisor in the CAD external service group at AT&T Bell Laboratories (Murray Hill, NJ). "But what they've really done is create macromodels of a circuit. And there's a distinction be-



The successive approximation A-D converter is excellent for testing the mettle of mixed-signal simulators because the circuit relies on both analog-to-analog and analog-to-digital feedback. In this model, over 400 active devices are represented as hierarchical or behavioral elements. This technique lets engineers think of complex circuits as functions rather than components.

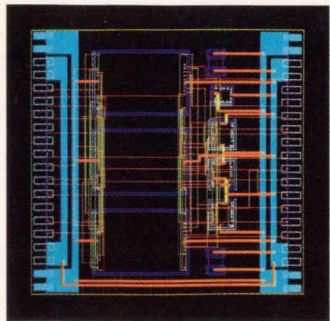


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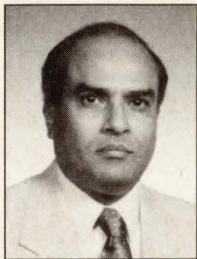
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**Unified vs. glued mixed-signal system simulation**



**S**ystem designers continue to confront growing issues in mixed analog and digital designs. To alleviate these concerns, they would ideally like to perform a true system

verification of their design including both the analog and digital sections simultaneously. With the tools commercially available today, however, that's impractical because of the inordinate time required to simulate a mixed-signal system. This is primarily due to the architecture of the existing simulators.

**■ The glued approach**

Basically, these simulators consist of a backplane or simulation manager that manages two different simulators, one analog and the other digital. This is best known in the industry as the "glued" approach to mixed-signal simulation.

Often, the simulators brought together in this scheme are from different tool vendors. Sometimes, there are three vendors involved: one providing the backplane, one the analog simulator and one the digital simulator. This technique is also called shuttle simulation because signals are shuttled from one simulator to the other. In such an application, the circuit is divided into two blocks: one digital and one analog. The digital simulator works on the digital block, stops, and transfers those signals that are common to both blocks to the analog simulator. Then, the analog simulator starts working on its block; once it has completed its task, it propagates the same signals back to the digital simulator. Since the analog simulator normally takes longer, it slows down its companion digital simulation. If there's a signal change at the input of the digital block while the analog simulator is working, the analog simulation has to roll back in time and be re-evaluated.

Because traditional techniques are used in the analog simulator, regardless of which part of the circuit is active, the complete analog circuitry is simulated. For instance, there could be several

blocks of analog circuits, which are distinct or disjointed, and they would be forced to be simultaneously evaluated, even though the inputs to each individual block haven't changed.

This is because traditional analog simulation techniques treat the entire analog circuit as one block and evaluate all signals in the block simultaneously. A significant overhead is introduced as a result of shuttling data between the analog and digital simulators. The simulation manager coordinates the propagation of signals between the two simulators and the vast amounts of data that are written to each simulator. In virtually

***True system verification of a mixed analog and digital design is not practical because of the amount of time required to simulate a mixed-signal system.***



every case synchronization of signals is needed and may require a large overhead in CPU time. From a broader perspective, the sheer amount of data transferred introduces so much overhead that complex simulations are performed very slowly. From an engineering perspective, system designers spend hours on the simulation because of the analog simulation portion. This is because in the glued approach, there can only be one analog block and since the analog simulation uses traditional techniques, the entire simulation is held hostage when designs are heavily laden with analog sections. Essentially, the other part of the process goes to sleep until the analog simulation is completed, and not until then does the digital simulation portion kick-start again.

**■ Unified simulation**

Unified or integrated simulation architectures, though, use only one process: the analog and digital are one and the same, supported by the same centralized database and controlled by the same simulation manager which is integral to the system. Consequently, process overhead is drastically reduced compared to the glue approach.

A tightly-woven mixed-signal system simulation like this also opens the door for exploiting event-driven simulation for analog sections. Previously, event-driven simulation was utilized only for digital blocks. With event-driven simulation for analog blocks, only those blocks that have signal events (i.e., input, output or state changes), are simulated. With this approach, latency in analog circuits is fully exploited, the extra time taken to evaluate idle analog blocks is eliminated and overall simulation performance is increased.

The integrated simulation architecture also permits the partitioning of analog blocks, not feasible in the glued approach. This partitioning is automated so that the system designer doesn't worry about slicing portions as analog or digital. In this regard, it's important for system designers to take a further look at automatic partitioning and what's behind it. The right modeling approach, for instance, can make it easier for software to recognize how to coalesce blocks together during automatic partitioning.

**■ The ABCs**

Partitioning of this caliber also plays a major role in dividing analog sections into various blocks for higher simulation speeds and efficiencies. In addition, behavioral modeling brings additional speed, especially when using an analog behavioral circuit (ABC) description language that's extended from digital modeling. Here, an ABC model comprises analog and digital I/O, as well as analog and digital bidirectional signals that carry current. A mechanism like this provides considerable flexibility in the simulation processor describing elements with varying levels of detail. ABC models also eliminate the need for interface models and allow modeling of true mixed-signal components.

When ABC modeling, automatic partitioning, event-driven simulation, and latency exploitation for analog sections are combined, the result is well over an order of magnitude increase in the speed and efficiency for simulating today's leading-edge mixed-signal designs.

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**CIRCLE NO. 51**



## MIXED-SIGNAL CIRCUIT BOARD

tween a macromodel and a behavioral model. An op amp model, for example, has resistors, capacitors and transistors in it. Some vendors have taken a portion of the functional attributes of that op amp and modeled it using current sources, voltage sources and simpler circuit elements with a few transistors here and there. This is a simpler model, but it's still based on circuit elements. A truly behavioral model, on the other hand, is a simple equation which doesn't have the intricate

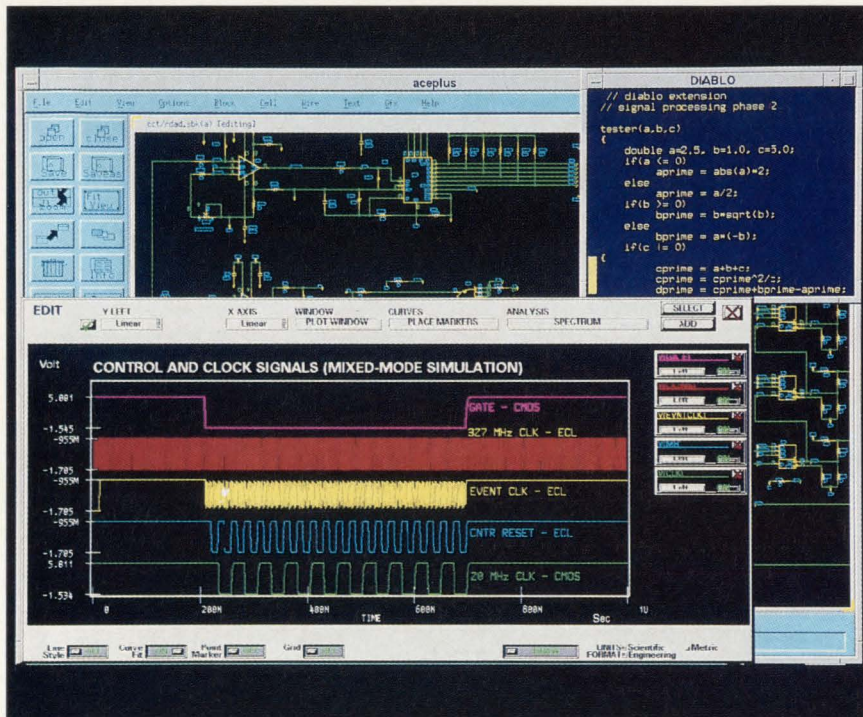
accurate results defeat the purpose of simulating to begin with, so in critical paths, we recommend a more detailed approach. If a signal is going from the digital to the analog side, it would be easy for a simulator to present an idealized signal based on a zero or one, but if it's a critical connection and the shape of that digital waveform is a big deal, we advise customers not to run that last layer at a logic level. We recommend that they go back a step and simulate at a transistor

component will be more accurate than a digital one because the digital representation is an approximation of a device's behavior," says Leon Gordon, a principal engineer at Racal-Redac (Mahwah, NJ). "When the approximation is good, it's more than worth it because you get two to three orders of magnitude speed-up over an analog simulation. After all, a digital simulation is chasing an event cue whereas an analog program is integrating a set of coupled, non-linear differential equations."

There are other advantages to the digital approach if the approximation is accurate. Digital simulations can apply worst-case timing analysis and fault simulation to portions of the circuit—a capability that's lacking in analog simulation. In addition, digital simulations have the luxury of using hardware models, a capability that's especially useful when modeling complex devices such as microprocessors. When all is said and done, however, a lot of the decisions about partitioning a circuit and which model to use come down to the expertise of the designer. "Every designer must remember that these are models he's working with, not real devices," cautions Kevin Jorgensen, product marketing manager for Viewlogic Systems (Marlboro, MA). "Understanding the limitations of device models is a fundamental problem of system simulation. The engineer must understand the trade-offs when using a Spice model, a hardware model or a VHDL model. He may use a transistor as either a linear device or as a switch. He just has to know the consequences of his decisions."

### Automating the process

Because circuit partitioning is a chore fraught with difficulty, some EDA vendors are producing simulators with automatic partitioning where simulation manager software decides which simulator— analog or digital—to invoke. Simulation vendors have to be careful how this interface is executed or needless intersimulator communication can occur. "In our simulator, we use a master-slave approach," explains Viewlogic's Jorgensen. "In an instance where the analog simulator is the master and the digital the slave, the Spice portion signals when there's an interface point to the digital simulator. Likewise, the



Dazix has tied its analog simulator, Apex, to its digital tool, AdvanSim, via a remote procedural-call mechanism which coordinates the timing of the two simulators. In this screen, the multimode schematic in the upper-left window contains primitive models, behavioral models and fast-executable ICs. The bottom window displays the associated analog and digital simulation waveforms, while the upper-right window shows code written in Dazix' C-based modeling language, Diablo.

detail of a components-based model, but which posts impressive gains in speed and flexibility."

AT&T holds that its behavioral models also employ latency and are event-driven, capabilities that analog circuit models can't encompass.

### When to use which

In addition to decisions about model detail, designers must also decide whether to use an analog or digital model for their simulations. "There will always be accuracy/performance trade-offs in simulation," says Jim Solomon, president of the analog division at Cadence Design Systems (Santa Clara, CA). "But in-

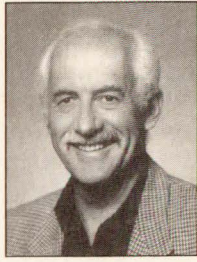
level. It might slow things down a bit, but accuracy goes way up."

The accuracy/speed trade-off affects not only the level of detail in defining device models, but also how a design is partitioned for simulation. Obviously, some components are purely digital and some purely analog, but there are hazy areas, like the analog effects in digital circuits, which must be partitioned by the designer. EDA vendors are taking different approaches to assist designers in making these partitioning decisions, or relieving them from the burden altogether. As always, there are trade-offs involved.

"In general, an analog model of a



## Analog simulation of digital systems



**A**t high frequencies, problems occur within interconnect media that don't occur at lower clock speeds. These "transmission line effects" must be assessed

through electromagnetic field analysis to define possible parasitic effects. To understand the essence of the problem, look at some simple—albeit exaggerated—examples.

At low speeds, a clock with a pulse width of 1  $\mu$ s, for example, has transmission line effects that are barely noticeable in normal electronic circuitry. In such a situation within stripline, with a dielectric constant of four, it takes about 1 ns for a signal to travel about 6 in. This is only 0.1 percent of the pulse width. Because this time delay is imperceptible in comparison to the pulse width, the signal appears at both ends simultaneously.

Now let's take a case where the pulse width is 0.5 ns. By the time the leading edge of this pulse reaches the receiver, the driver signal will be 0 V as the trailing edge of the pulse will have passed the input end.

Determining the velocity of electromagnetic propagation along transmission lines then, is a critical, but not a very simple matter. Let's consider a microstrip line as an example. Microstrip lines are those on the surface of a typical PCB. These traces have fiberglass or other dielectric material on one side and air on the other. If you imagine lines of electric field intensity starting from a microstrip trace, passing through the air, going back into the dielectric (fiberglass) substratum and then to the ground plane, you will appreciate that the energy in the system is distributed throughout both the air and the dielectric medium. The velocity of propagation would be somewhat less, being inversely proportional to the square root of the dielectric constant. For a microstrip trace, therefore, the velocity of propagation will be intermediate between these two extremes because energy is distributed in an unclear way throughout both media. When several traces are in proximity, the situation becomes even more complex because it's necessary to worry about the energy dis-

tribution for each possible mode of propagation to obtain a correct simulation. For example, three adjacent traces can establish three propagating modes each with its own velocity of propagation. The determination of the actual velocity for this situation has to be resolved by the solution of a field problem. (There are handy design-book formulas that exist, but these are useful only in a very few restricted situations.)

### ■ Speed has its price

What problems can occur because of high-speed effects? Timing problems can result from narrow pulse widths and unequal transmission line lengths. If one signal travels a short distance toward an AND gate, it arrives at the gate faster than a signal that travels over a longer trace. If the signal widths are wide, then the delay will be imperceptible and the pulse will appear at the AND gate output port. But if the pulse widths are of the order of 1 ns, then it's possible one pulse will arrive after the other has vanished with the result that the output is 0 V. Because this isn't what the designer intended, a logical error results and the system fails. In complicated systems, such timing problems occur even for considerably wider pulses operating at frequencies of 50 MHz. To avoid overly conservative designs, therefore, it's essential to have accurately determined propagation velocities for timing simulations. And these can only be determined through electromagnetic field calculation.

Another high-clock-rate problem is crosstalk. Basically, crosstalk is the result of one conductor acting as an antenna to produce a near-field signal on an adjacent trace. It may also be viewed as the transfer of a signal through inductive and capacitive coupling. If the receiving trace is intended to be quiet but acquires a phantom signal through crosstalk, this false signal could be interpreted by the logic. For example, if two traces are terminated in an AND gate, the gate could interpret crosstalk on the quiet line as an intended signal and produce a pulse as output. An error results.

Signal ringing, due to multiple reflections, results in the degradation of signal integrity and causes other logic problems. A pulse launched on a transmission line reflects a portion of the signal at the termination if—as is rarely the case—its

impedance isn't equal to the circuit's characteristic impedance. Except for very simple cases, the characteristic impedance has to be found by field analysis.

The reflected signal returns toward the sending end. Once it reaches the sending end it's reflected yet again, this time depending upon the source impedance. This happens many times with the result that the initial approximate square wave begins to exhibit a standing-wave pattern with overshoots and undershoots, not unlike what one sees in a bathtub. The overshoots are not of too much concern but the undershoots—if they are deep enough—could be mistaken for zeros by the logic.

### ■ Back to basics

It's clear, therefore, that at the heart of the solution of interconnect problems is the requirement to solve field problems accurately for stray capacitances, inductances and resistances (the latter due to skin effect) and finally to solve for currents and voltages on complicated networks of traces, connectors, cables, and packages. Basically, we have to perform analog simulations of large digital systems.

As the impact of analog effects on digital circuitry grows, with higher clock speeds, the opinions of analog designers are increasingly solicited. Even electromagnetic field theorists—who were rarely noticed in years past—are now being pressed into service.

Before starting PCB layout, design rules are set up to work out trade-offs between a range of parameters. Here, simulation tools such as Qantic's Greenfield can be used to experiment with different types and sizes, and placement of ground, signal and power planes. Layout can then proceed according to design rules. Once the layout is complete, the entire board design can be screened for nets with crosstalk and signal integrity problems. Geometrical descriptions, as well as components used, can be extracted from the layout tool and read by the screening tool. Likewise, every trace selected in the board layout can be screened for crosstalk and signal integrity violations. The screener then attaches drivers, receivers and loads to the transmission line net models and time-domain analysis can be used to determine signal integrity and crosstalk measures.

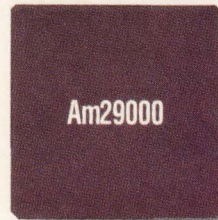
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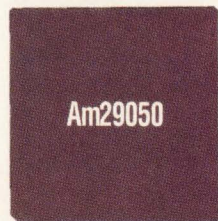
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## MIXED-SIGNAL CIRCUIT BOARD

digital simulator can run until such a time when there's an analog event. This is more efficient than an interface where the analog simulator tells the digital simulator every time it takes a step. Naturally, the more of these interface points the slower the simulator, but we try to keep them to a minimum. Most designs that we see are loosely coupled, that is, they have rela-

approach are leaning toward a "simulation backplane" which integrates digital, analog and mixed-signal algorithms into a homogeneous environment. There are problems with such an approach, namely, in timing the events of multiple simulators to reflect the real-world behavior of a circuit board as it transfers functions from the digital side to the analog side. As with any meld-

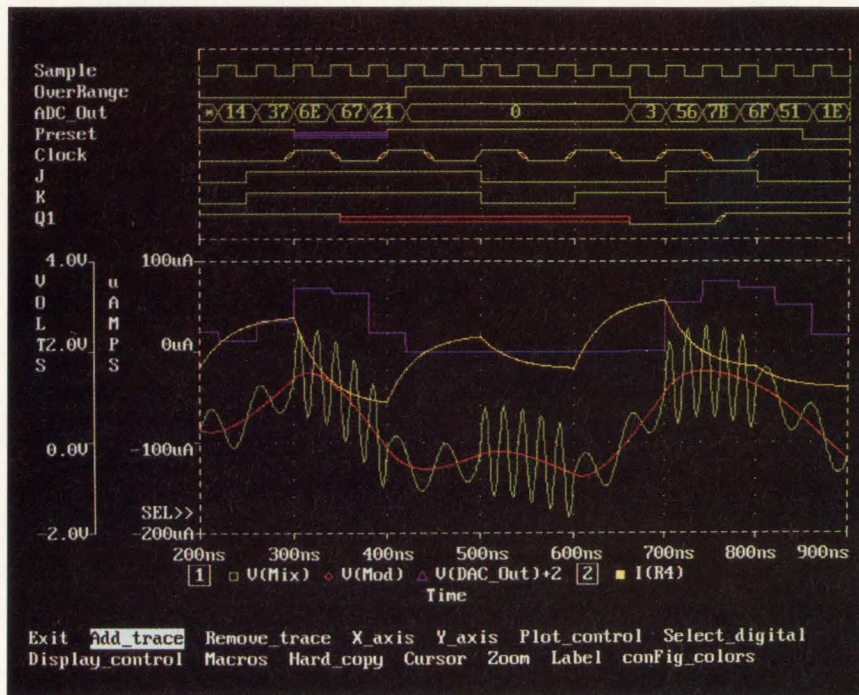
sign house and EDA tool vendor. "First of all, you're assuming that someone understands the complex issues of mixed-signal design well enough to define them accurately. Second, even if you do describe them sufficiently, they have to be translated to code that's often written by a software engineer. If you try to cram too much expertise into one environment, you're liable to end up with an unwieldy, inefficient simulation tool."

### Moving forward anyway

Undaunted by messages such as these, EDA vendors are forging ahead with tightly coupled simulation environments. Analog (Beaverton, OR) and Racal-Redac have tied together the two worlds with the Saber/Cadat simulator. Analog's Saber provides the analog simulation engine, while Racal's Cadat takes care of the digital side. The tools are tied together in a master/slave configuration and the user assigns which simulator will assume the dominant role via the user interface. The simulators run concurrently and are synchronized via the Calaveras algorithm, which lets each simulator run as long as it can until an event is scheduled for the other. The simulators leapfrog down the simulation run, each executing as much as it can until the other catches up. "The trick here is not to make a simulator have to back up and repeat what it's already done," says Racal-Redac's Gordon. "It would also be catastrophic to keep the simulators in lock step, especially for digital events. If a digital simulator can leap ahead in one microsecond increments, it would be deadly to shackle it to one nanosecond steps because of the analog simulator's constraints."

The models for Saber are written in Mast, Analog's proprietary language. Though Mast lets users implement systems spanning levels of description from behavioral to primitives in both analog and digital domains, the analog behavioral approach speeds up simulation in the Saber/Cadat combination. While not as detailed as simulators running Spice models, Analog's behavioral method runs faster and can incorporate device models not easily defined in Spice.

Proponents of behavioral level mixed-signal simulation hold that their approach is a logical alternative to the timing and interface prob-



In this screen display of MicroSim's PSpice Probe waveform analyzer, the analog and digital waveforms are displayed together on a common time axis. PSpice results can also be saved to a table of X and Y values that can be used as input to graphics programs, spreadsheets or other programs for further data manipulation. Multiple Y axes (in this case, volts and  $\mu$ amps) can be invoked for analog analysis.

tively few areas where the digital side needs to be in communication with the analog."

At the heart of the decision to use two simulators in tandem—a "glued" approach—is the realization that no one tool is best suited for the many tasks encountered during a complex mixed-signal simulation. "We're finding that it's not possible for a single algorithm to solve all problems," says Jim Griffith, business unit director for the simulation and test division at Mentor Graphics (Wilsonville, OR). "We'll see an algorithm for a switched capacitor filter that won't handle anything else, but is five to 10,000 times faster than Spice. The main problem is getting something to make all these specialized algorithms play together."

EDA vendors who use such an

ing of technologies, the level of integration is key.

A deeply embedded algorithm in a simulator might work seamlessly, but interfacing the complex code of the algorithm, without changing its essence, can take months. Again, simulation vendors must ask themselves if it's worth the effort. Most board designers that were interviewed for this report expressed interest in an integrated approach, but were skeptical of the ability of any piece of software to efficiently unite the disparate simulation requirements of digital and analog circuits. "You're making a lot of assumptions when you claim to have a piece of software that's so comprehensive," says Lee W. Ritchey, vice-president of engineering and marketing at Shared Resources (San Jose, CA), a circuit board de-



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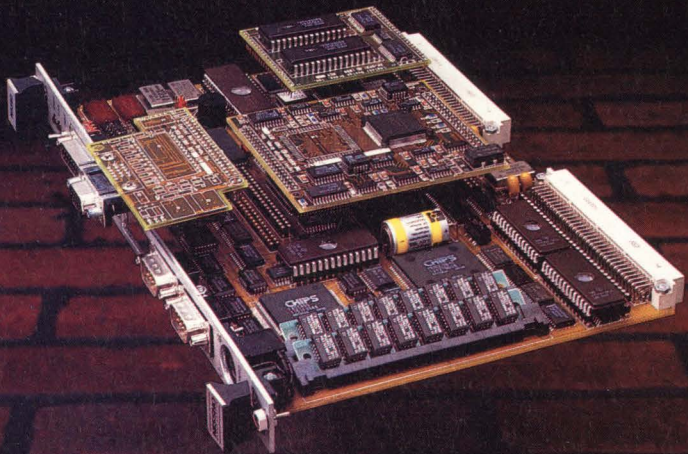
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CIRCLE NO. 53



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lems associated with glued or back-plane simulation environments. AT&T hopes to make a splash with its Design Verification System, an in-house tool it's going to market as a stand-alone mixed-mode simulator. The simulator uses AT&T's analog and digital models written in C and supplements it with a library of modeling constructs. The system also supports VHDL and models from Logic Automation's Smart-Model library and interfaces to the family of hardware modelers from Logic Modeling (Milpitas, CA). AT&T decided to take a behavioral, single-simulation approach to address some of the objections of design engineers who can't envision multiple simulators as a solution to mixed-mode problems. "We think the single process approach gives us several advantages," says AT&T's Subramaniam. "The integrated simulation architecture reduces computing requirements so you can handle much larger circuits. We also address automatic circuit partitioning because both sides, analog and digital, are handled by the same engine."

This is especially valuable, AT&T claims, in the analog domain where traditional simulators force designers into thinking of analog behavior as one large block. "If you look at a typical system, there are going to be several analog blocks and not all of them are going to be active at any one time," Subramaniam points out. "In the glued approach you're forced to include all those analog subsystems as one big chunk and essentially simulate each for every interval of time. By using a single simulation process, you address each analog function on an 'as needed' basis. Now you could conceivably do the same thing with a glued approach, but if you had multiple simulation blocks you'd have multiple analog simulations running, which means additional

processes and additional intercommunication between processes. That translates to more overhead, which just isn't practical."

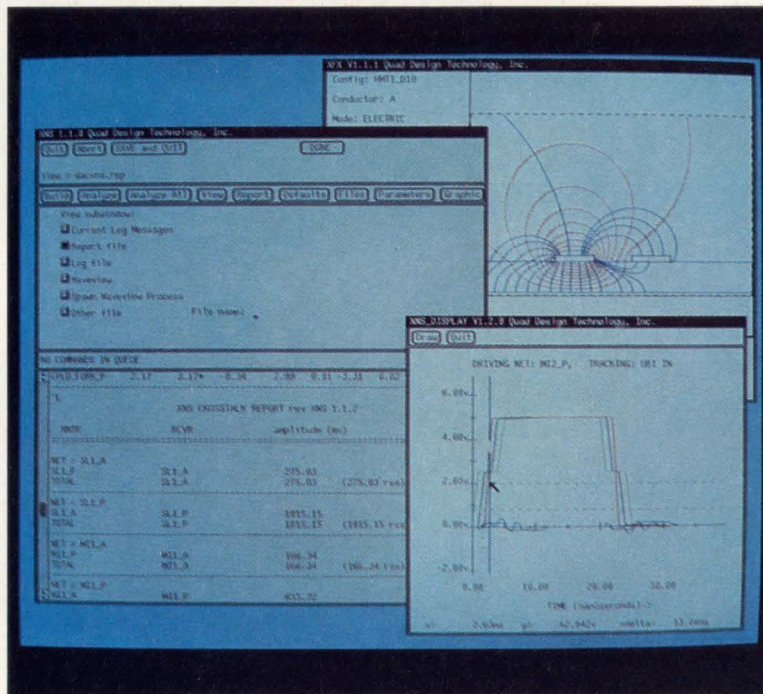
Unfortunately, these claims and counter claims of EDA vendors about which approach is best—glued or single simulator—is liable to muddy the waters in a market which is already reluctant to attempt board-level simulation of any kind. Most tool vendors are trying to ease the skepticism surrounding the need for their products by assuring the design community that the soft-

encounters and adapts to the type of device encountered. ACP also predicts which simulator should move ahead and by how much, minimizing the need to back up."

Most of the various simulator approaches do have something in common—they assume that the user wants to simulate an entire design. And though the EDA community is banking on the demise of prototype debugging to fuel the need for complete design simulation, most board vendors still dwell in a "divide and conquer" world, where the digital portion of a circuit board is designed and simulated and the analog portion is considered separately. "Remember, any shift to circuit board simulation will be evolutionary," says Shawn Hailey, president of Meta-Software (Campbell, CA). "The computers might be getting faster and the tools better, but our brains aren't getting any bigger. We're still limited by the human element. The real challenge will be in partitioning the problems so we can still understand them."

For places where the two meet, Spice models can provide the connection. "We've been doing digital simulation since 1983," says Jim Veres, director of engineering design at Alliant Computer (Littleton, MA). "We also use some Spice, but haven't seen the need to integrate the two. We'll do a complete Spice analysis of the data lines all the way from the microprocessor module to the backplane and on to the crossbar switch card, including getting the models from the ASIC vendor for the switch itself. But those are still separate simulations as far as we're concerned."

Other PCB designers feel that the analog section of any circuit board will have to be prototyped anyway, and feel that spending inordinate amounts of time modeling in Spice could be a waste. "We put a lot of effort into really strict design prac-

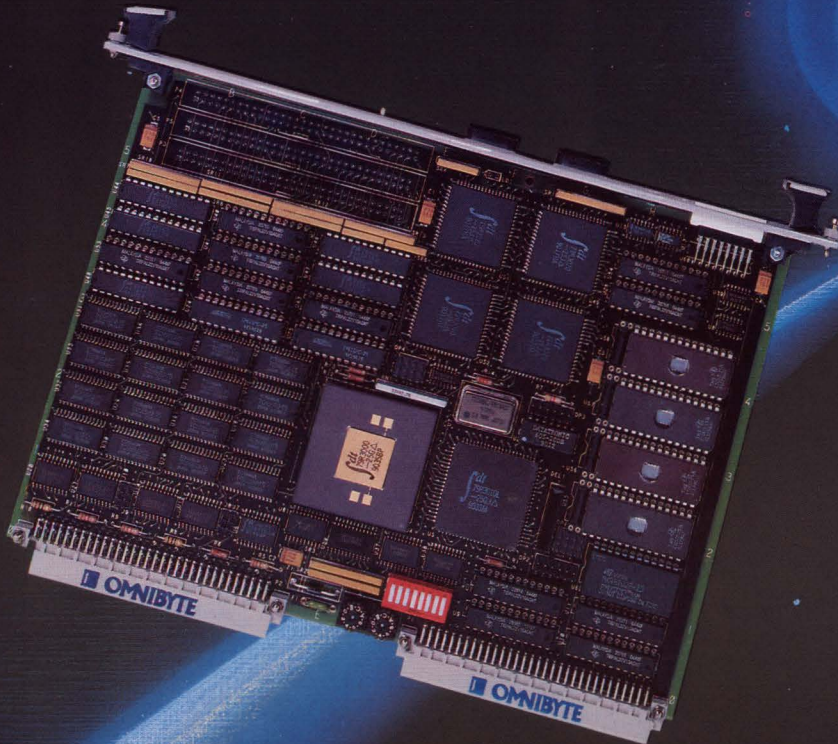


*Quad Design's Crosstalk Toolkit (XTK) simulates transmission line effects and the effects of signal coupling or crosstalk from parallel signal traces on printed circuit boards. In the upper right, XTK calculates the coupling effects of parallel conductors on a printed circuit board through field extraction techniques. At the bottom right, the tool generates waveforms, delay and signal-quality reports. At the left is a cross talk report of the simulated effects.*

ware will be easy to use and will do most of the work in tracking the two sides of the simulation equation. Dazix (Boulder, Co), a division of Intergraph (Huntsville, AL) is touting the efficiency of its glued simulation approach with its Adaptive Control Processor (ACP), which links its analog simulator, Apex, with its digital offering, AdvanSim. "ACP uses a remote procedural call mechanism to synchronize the analog and digital simulators," says Tim Ghazaleh, senior manager for analog CAE marketing at Dazix. "It's essentially a separate piece of software that looks at all the different types of models that a simulator



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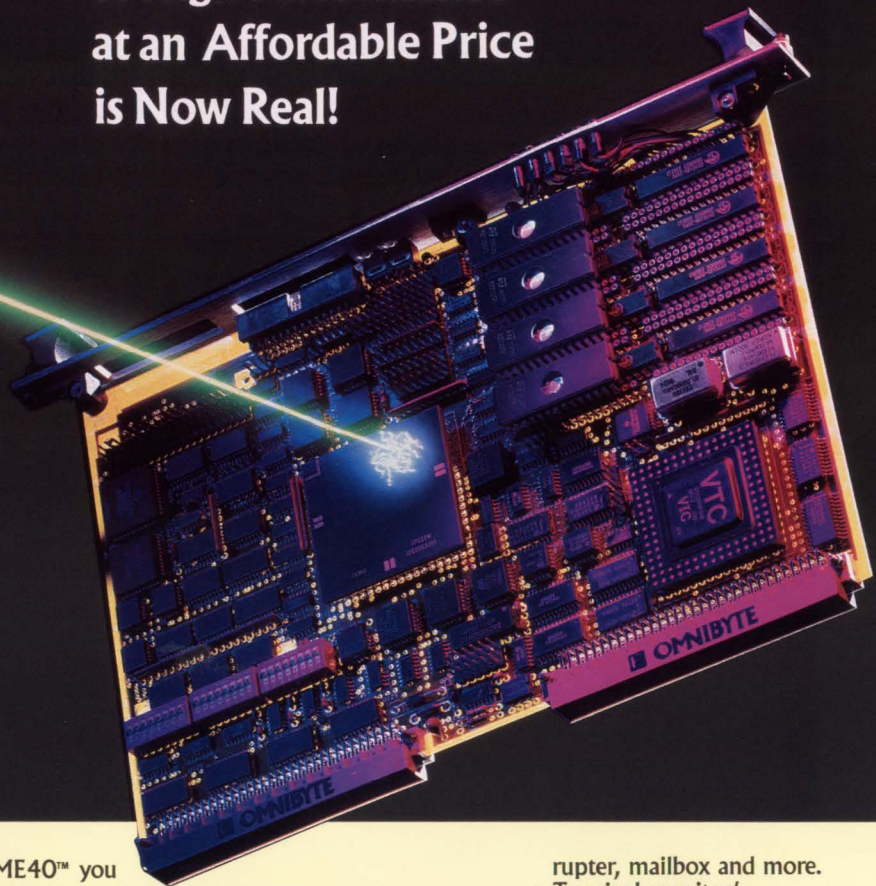
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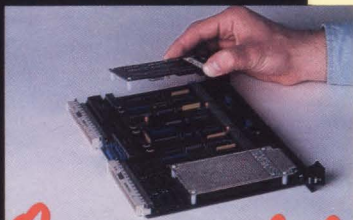
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## New products need new simulators



Let's survey the horizon of product development in the near future. The general trend of using more and more mixed-signal designs where digital and analog technologies are closely intertwined is building momentum. Another trend is the ever increasing operating frequencies of these systems and devices. Compact video equipment, for example, evolved from analog systems at several MHz to more than 10 GHz. Supercomputers operate in the range of 100 MHz to over 2 GHz. Office automation equipment typically has frequencies in the range of 40 to 200 MHz. Another trend is ever-shrinking device sizes, where unintended effects, such as electromagnetic couplings and signal reflections of the packaging, multichip module (MCM) interconnects, or interconnects within the chip, may render nonfunctional end products.

In other words, though system designs are mixed digital and analog in nature, their frequency of operations is reaching into microwave ranges, and the secondary and tertiary electromagnetic effects have to be taken into consideration during design. Similarly, simulation tools used for such systems must have all the capabilities within one integrated simulator employing one unified algorithm for simulation. An ideal simulation program should have the capabilities of solving a variety of problems such as nonlinear algebraic equations, nonlinear ordinary differential equations, digital Boolean functions, and frequency-dependent functions.

### Integration a must

It becomes clear that simulation tools can no longer be compartmentalized as logic simulation, circuit (analog) simulation, transmission line simulation, electromagnetic fields solver, antenna design software, etc. Future simulators must take multiple aspects of designs into consideration simultaneously. The simulation technology has to cut across several related disciplines to accurately predict design performance.

A new approach to native-mode, mixed-signal simulation is to use a new

logic system where Boolean functions are evaluated in floating-point numbers. For example, the "AND" function is equivalent to finding the minimum of the inputs. Using this new logic system, which Contec calls Infinite State Logic Simulation (ISLS), logic devices ranging from basic AND gates to edge-triggered flip-flops can be implemented in a circuit (analog) simulator based on the highly reliable direct method used in Spice. Public domain Spice has the reputation of not being able to converge to a solution for difficult circuits. But the faults are not with the direct method itself. Programming bugs, model equation abnormalities and discontinuities and incorrect implementations are the main culprits. Compared with other circuit (analog) simulation algorithms developed over the years, the direct method, based on a modified Newton's method and implicit integration, is the most general and reliable algorithm.

A mixed-signal simulator based on ISLS for logic simulation uses only one simulation algorithm, the direct method. No logic-analog translation interface is required. Furthermore, there's only one "time" measure for simulation that simplifies the time coordination problem in other mixed-signal approaches. The waveforms from ISLS are in the continuous analog form. With accurate modeling of digital devices in ISLS, simulation results can be virtually identical to the results from the transistor-level circuit (analog) simulation—a 10 to 20x increase in simulation speed can be achieved.

### Analog effects in digital

To provide accurate analog continuous waveforms, input-output characteristics, nonlinear input and output impedances, rise and fall delays, and rise and fall times should also be modeled in the digital devices. Since the direct method for partial differential equations represents multiple coupled lossy transmission lines in ISLS, such a simulator can be used to simulate a digital system together with the electrical effects of the interconnects, packaging, connectors, cables, and backplane.

New techniques are needed to include microwave devices in a mixed-signal simulator. In addition to including distributed-parameter devices (such as transmission lines) anywhere in the sys-

tem, a mixed-signal simulator also lets devices be described in terms of frequency- and voltage-dependent scattering parameters. This type of simulator will handle systems composed of elements such as digital gates, nonlinear transistors and microwave devices. Simulators based on harmonics-balanced techniques have severe limitations and difficulty in analyzing mixed digital and highly nonlinear analog circuits.

### Hierarchical analog descriptions

Mixed, hierarchical-level description and simulation for logic simulation, on the other hand, are well-known. For circuit (analog) simulation, analog functional-level descriptions of analog subsystems and devices can easily be achieved through nonlinear equations or transfer functions relating the inputs to the outputs. The analog behavioral-level descriptions of analog subsystems can be constructed from a functional block with an electrical structure to model input and output impedance and delays. The analog macromodels represent subsystems with equivalent circuits constructed from basic elements built into the simulator. The lowest level of abstraction is the basic, built-in element. A mixed-signal simulator based on ISLS can describe the systems in terms of mixed hierarchical levels, from the functional, behavioral, macromodel, and gate and element levels, for both the digital and the analog parts of the systems.

Using a top-down design methodology, a system design can be simulated at the functional level for its digital, analog and distributed-parameter subsystems. As the more detailed subsystem designs are realized, the complete system can be simulated with some of the subsystems represented at successively more detailed levels. Simulation can still be carried out for the complete system with subsystems at different levels of representation, thus the interactions among the various subsystems are completely modeled and simulated.

Simulation tools for the next generation of products should employ a seamlessly integrated and truly unified algorithmic approach. All the effects that influence system performance can be simulated with all the interactions taken into consideration without oversimplification and without sacrificing accuracy.

**Paul K. U. Wang**, PhD, PE, president, CAE Division, Contec Microelectronics USA







## MIXED-SIGNAL CIRCUIT BOARD

chosen the dynamic timing approach which simulates the flow of data transitions across a circuit over time. This method is based on a circuit's behavior, because some devices' delays are dependent on what the components are doing at a given time. This approach differs from the static method favored by some EDA vendors, which sums up the delays that a signal encounters along a given path and identifies critical paths where timing violations will occur. There are pros and cons to each method.

While dynamic timing analysis has the advantage of incorporating a circuit's behavior into simulation, such exhaustive treatment usually takes time to set up and run. Static timing, on the other hand, can give comprehensive reports about potential delays in a circuit, but requires designer expertise to sift through the data and determine which paths are critical and which aren't. Some timing tools, like Quad Design's Motive, meld the two domains to eliminate the time-consuming set-up time of dynamic tools while controlling the false path analysis of static methods. In any case, the advent of sophisticated timing verification tools might win back some simulation skeptics who have been put off by the inadequate timing tools of the past.

### Does danger lurk here?

If there's a hidden danger in all of these tools that promise automation of difficult design tasks, it's that

they might wrest too much autonomy, and discourage the creativity of the circuit board designer. A delicate balance is necessary if the tools are to fulfill their main promise—to relieve designers from the drudgery of analyzing infinitesimal physical constraints. EDA vendors must also be careful not to promise too much, or designers, particularly the newer generations who are proficient with computers and software, might lose sight of the basic rules that underlay every circuit, complex or simple, digital or analog.

"There's this hope that you can buy an automatic tool so you don't have to engineer anymore," cautions Ritchey of Shared Resources. "That's a flawed vision. Our industry is in danger of turning out engineers who never got trained in the basics but who desperately need to know them to design correctly. Technology is getting to a point where noise can look like a signal. Anyone who can't tell the difference is going to lose." ■

## Postscript

**E**ditors are in a unique position. Like customers, they hear the sales pitches of vendors, read the glossy brochures and witness the mud-slinging as competitors offer alternative solutions. Unlike customers, however, editors are spared the ultimate fate—making a buying decision and writing a check.

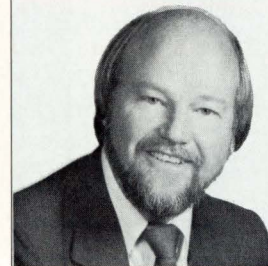
To hear the EDA community tell it, high-speed clock rates and their analog effects will soon render prototype debugging virtually useless. The main question won't be whether to use mixed-signal simulation, but which approach to use.

The various techniques available to achieve this integration of analog and digital circuit simulation are both dazzling and confusing. And the vagaries of the physical world rarely enter the realm of slick demos and colorful user interfaces.

The circuit board designers I interviewed for this story tell the true tale. They speak of frustrations when they try to obtain accurate device models, simulation requirements that would choke a roomful of Crays and price tags on simulation software that make their current debugging techniques look economical. One system designer from the Lone Star State confided, "Mixed-signal board simulation? Naw, we don't see the need for that yet. Besides, I don't believe it's legal in Texas."

The upshot of all this, I suppose, is whether the EDA community is busily working on software solutions to problems that are still best solved by experienced engineers and elegant design practices. It's true, the days are coming when multichip modules and high performance CPUs will sound a death knell for the blue-jumpered prototype. But at \$100,000 a copy for a mixed-signal simulator, the tolling had better be pretty loud.

Mike Donlin



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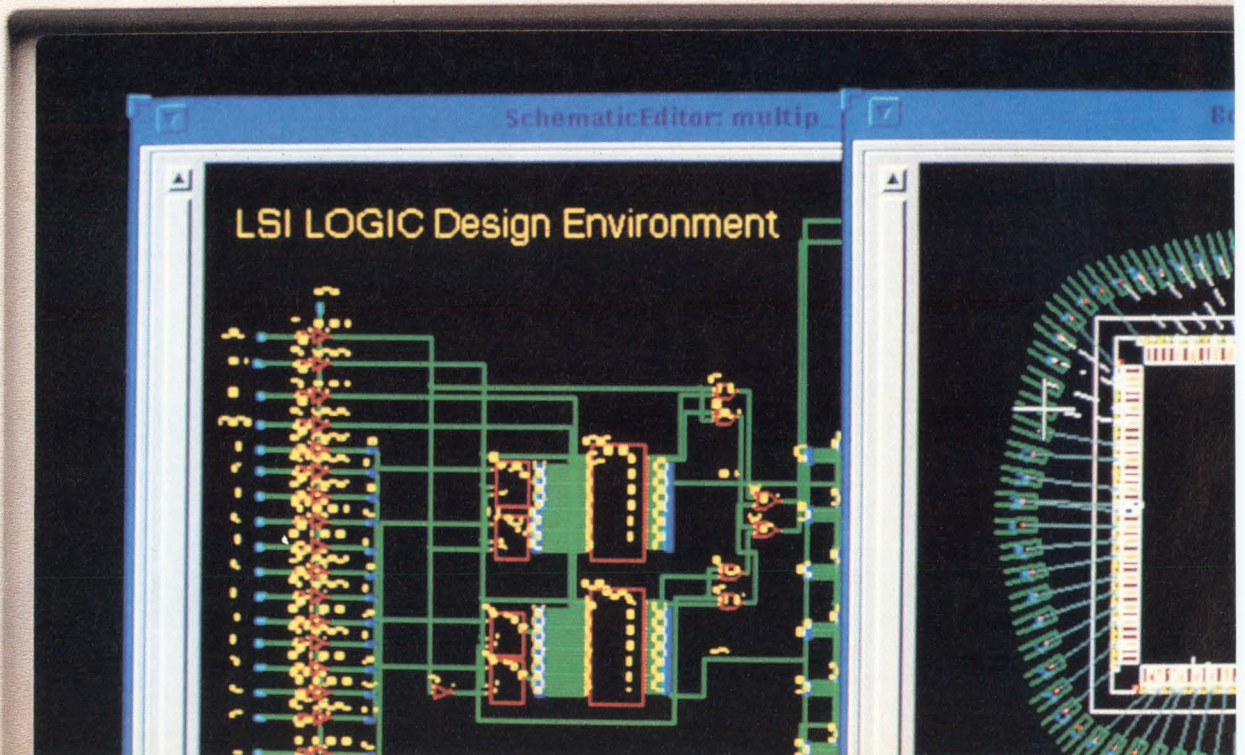
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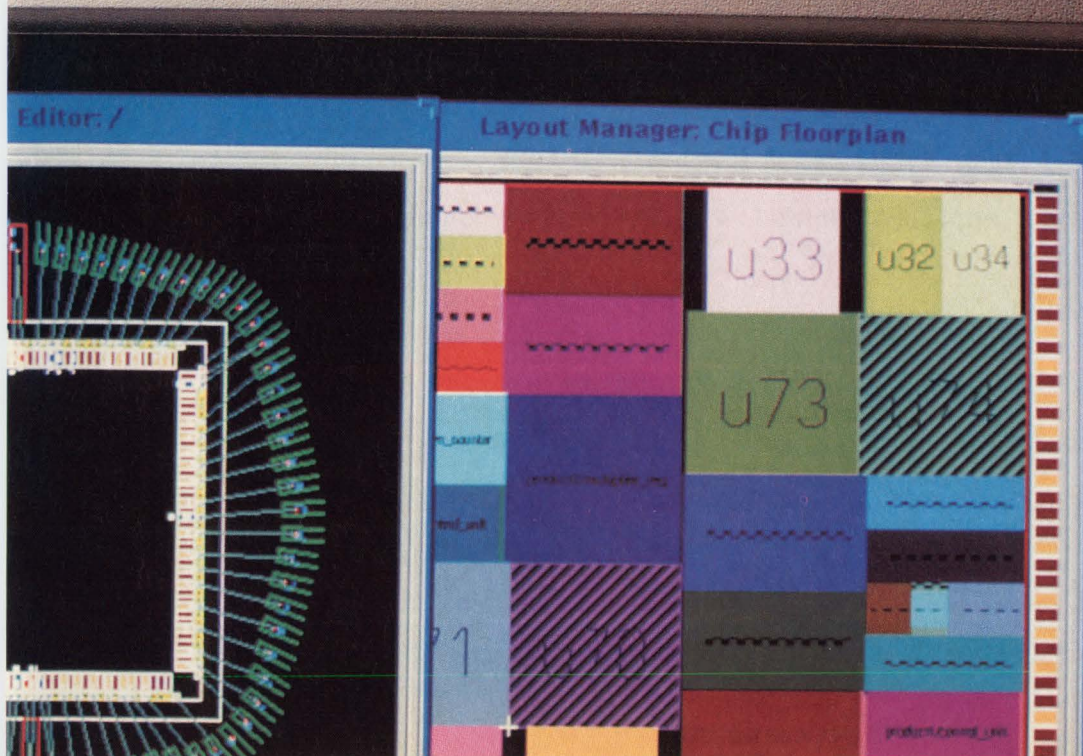
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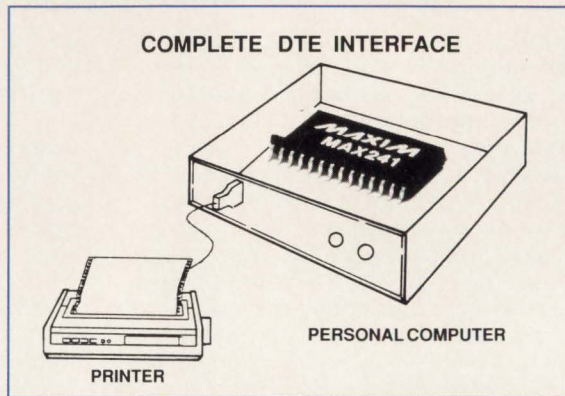
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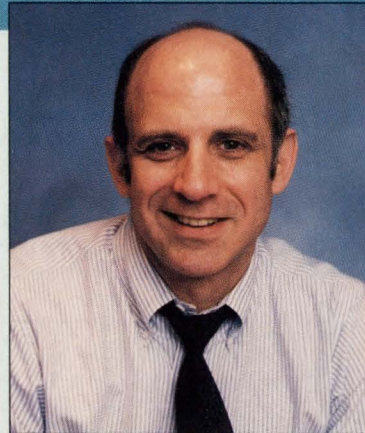
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## Sometimes, you can't beat an op amp

III



I knew a Field Applications Engineer (FAE) in the Minneapolis area who is rumored to have told Cray Research, "If you can't do it with an op amp, it isn't worth doing." The FAE's claim has merit: operational amplifiers are mathematical integrators and there are signal combinations—multiplication and logarithmic functions—that can implemented much more cheaply and efficiently with analog means.

But this story about an op amp enthusiast underlines the sometimes outrageous cultural differences between analog and digital designers. Where digital systems designers are learning to manipulate CMOS circuit blocks with literally millions of transistors, analog circuit designers will express awe and reverence toward bipolar circuit blocks with little more than 32 transistors. Linear Technology's Jim Williams, a staff scientist—who went so far as to show the world how to use op amps to stabilize cathode voltages on vacuum tube audio equipment—is reputed to have authored a bumper sticker that said: "One op amp is worth 1,000 microprocessors."

With system designs reflecting digital building blocks and design philosophies, op amp enthusiasts have to be in the same category as those who spend their Sunday afternoons polishing their 1955 Thunderbirds or 1957 Cadillacs. Analog design, especially op amp system design, occupies a smaller proportion of the engineering thought process.

And yet, there are situations—thousands of them, in fact—where nothing else will do. Op amps remain the basic building blocks for practically all analog circuits. They form the front ends for practically all test-and-measurement equipment, communications gear, audio and video signal processors, and servo loop controllers.

### ■ Smaller signals, noisier environments

"The reasons for doing analog may seem to evaporate," acknowledges Bruce Trump, an engineer with strategic marketing responsibilities for op amps at Burr-Brown (Tucson, AZ). Trump says Burr-Brown's forte is signal processing, an activity which includes "signal acquisition," as well as data conversion and

manipulation. The signal acquisition portion, he believes, becomes a smaller slice of the pie as the world turns digital. But the signals that must be acquired become more diverse and challenging. Trump points out—not without a certain amount of pride of accomplishment—the difficulty of acquiring ever smaller signals from increasingly noisier environments. It's a job that op amps do best.

Precision low-noise op amps are chief among the analog designer's bag of tricks, though the electronics trade press finds these increasingly less newsworthy. Precision Monolithics (Santa Clara, CA), now a division of Analog Devices (Norwood, MA), for example, got a magazine cover story for its OP-27, a precision op amp which shaved a half  $nV/\sqrt{Hz}$  (What's a "nanovolt-per-route-hertz"?! you ask) from the best available noise figures. The OP-27 offers a noise figure of  $3.0 nV/\sqrt{Hz}$ . (The previous record holder was the NE5534, whose typical noise spec was  $3.5 nV/\sqrt{Hz}$  at 1 kHz.) When the Linear Technology LT-1028 entered the electronics world with very little fanfare—a press release, but no magazine covers—it was a testimonial to how much engineering sensibilities had changed. The LT-1028 has a record-breaking noise figure of less than  $1 nV/\sqrt{Hz}$  at 1 kHz.

This noise figure—a process-dependent measure of the collective buzzing generated by the op amp's own transistors—is important primarily in those applications where the small signal generated by the input sensors can be overwhelmed or distorted by any extraneous electrical noise. The sensitivity of magnetic sensors, infrared and sonic detectors used in current medical equipment, will demand ultra-quiet amplifier electronics. Other op amp specs that become important in a precision sensing application are input offset voltage, input impedance, temperature drift, common mode rejection, and voltage gain. Each of these specs is a reflection on the sensitivity and overall accuracy of the amplifier.

### ■ Trade-offs are a way of life

Bandwidth (speed), settling time and drive capability are entirely different considerations. The most avid op amp freak will verify that op amp design and



## MIXED-SIGNAL DESIGN

selection invariably involves trade-offs or optimization between one set of specifications and another. An amplifier's ac characteristics will often sacrifice dc performance. The requirement for speed, for example, will generally require trade-offs in precision and drive capability. High gain will often sacrifice linearity and low-noise. It will be hard to maintain a 10- $\mu$ V input offset if you're processing 100-MHz signals.

Op amp designers and manufacturers, as a consequence, are constantly evolving and tweaking their fabrication processes to provide a different balance of trade-offs. But instead of evolving universal amplifiers, manufacturers have generated encyclopedic catalogs of part types, each specially-tweaked to a different application.

Compared to microprocessors and memories, the volumes of op amps required in each application are puny (the entire worldwide op amp market—about \$900 million—is only about  $\frac{1}{4}$  the size of Intel). But there are two application areas which are currently generating a great deal of excitement for systems people: speed and low power consumption. The requirement of wireless communications and emerging application areas such as personal computer multimedia and high-definition TV is speed. The requirement of all kinds of portable equipment is low power consumption. HDTV scanning systems will require amplifiers that operate well above 50 MHz, while hand-held communications systems will look for amplifiers that consume 10  $\mu$ A standby from a 3-V source.

Improved process technologies are letting op amp designers resolve some of the trade-offs between high-speed, low power, and low noise. Bipolar technologies which produce complimentary npn and pnp transistors let designers build current-mode op amps. The result is IC op amps like Analog Devices' AD9630 or Comlinear's CLC110 which have 750-MHz bandwidths, 1200 V/s slew rates—and still show noise figures less than 2.4 nV/ $\sqrt{\text{Hz}}$ . These devices are used for driving flash A-D converters, baseband communications and fiberoptic cable systems.

With the ever-increasing proliferation of op amp types, the talent of the analog designer is in picking the right op amp for the job—out of the hundreds available—and carefully matching these to other components. The advantage of using a low-noise op amp, for example, is totally shot if you hang carbon film resistors on the input.

### ■ Enter analog emulation

The real challenge to the authority of the op amp guru isn't the proliferation of digital design techniques and philosophies. It's something I call "analog emulation" technology. (This is equivalent to what Gus Richard, a senior analyst at VLSI Research [San Jose, CA], calls "digitized analog.") Analog emulation is the ability to perform a primarily analog function by primarily digital means. One example is the analog memory device created by Information Storage Devices (ISD), in San Jose, CA. Here, a high-density EEPROM is adapted to store analog waveforms in the range of 0 to 5 V. The device will capture 20 s of information with

a bandwidth of 3 or 4 kHz, which makes it ideal for speech recording applications (though devices with higher analog bandwidths and larger storage capacity will appear in the not-too-distant future).

Digital signal processors are the most accessible examples of analog emulation. These machines perform complex waveform manipulations—multipole filtering, for example—with greater speed and precision than is usually possible with strictly analog devices. The major drawbacks to using DSPs for conventional analog filtering, however, is the time and expense required to program the DSP chip. No matter how many resistors, capacitors and unity-grain buffers you need to implement a steep filter function, many analog and mixed-signal system designers find it friendlier, less costly and less time-consuming to work with op amps than with DSP chips.

This too will change: the design system revealed recently by Star Semiconductor (Warren, NJ) promises to do for custom analog design what programmable logic devices have done for digital design. Perhaps one of the most sophisticated applications of analog emulation, the system uses DSP techniques to transform block-level diagrams of analog functions drawn on a workstation screen into working silicon. The system can create 100-to-200 separate op amp functions, says Star's founder Jeff Robinson. It approaches the ideal of a silicon compiler dedicated to analog functions.

But until systems like Star Semi's fully take hold of the design community—until the current generation of analog gurus retires—there will remain a dichotomy of thinking about how signal-processing jobs should be done. There will be a clash of cultures, with assorted sniping.

You've heard the conjecture that a million monkeys banging away on a million typewriters collectively might produce the works of Shakespeare or Milton's *Paradise Lost*. Digital design is probably the embodiment of the million monkeys. A microprocessor clock, after all, is nothing more sophisticated than a monkey jerking up and down on a pump handle—albeit, 25 or 33 million times a second. But everything in the digital system is harnessed to that microprocessor clock, and figures like CMOS gate delays are more-or-less standardized for the entire electronics industry. Digital logic builds a very *mechanical* system.

There's no specification with similar universality among op amp users. The analog design will require much more precision and craftsmanship. However, all engineering—analogue or digital—requires designers to balance functionality against costs. And though it continues to give up territory, there remain places in a complex system where the op amp wins.

*Stephan Ohr is editor/publisher of the monthly newsletter, Mixed Signals.*



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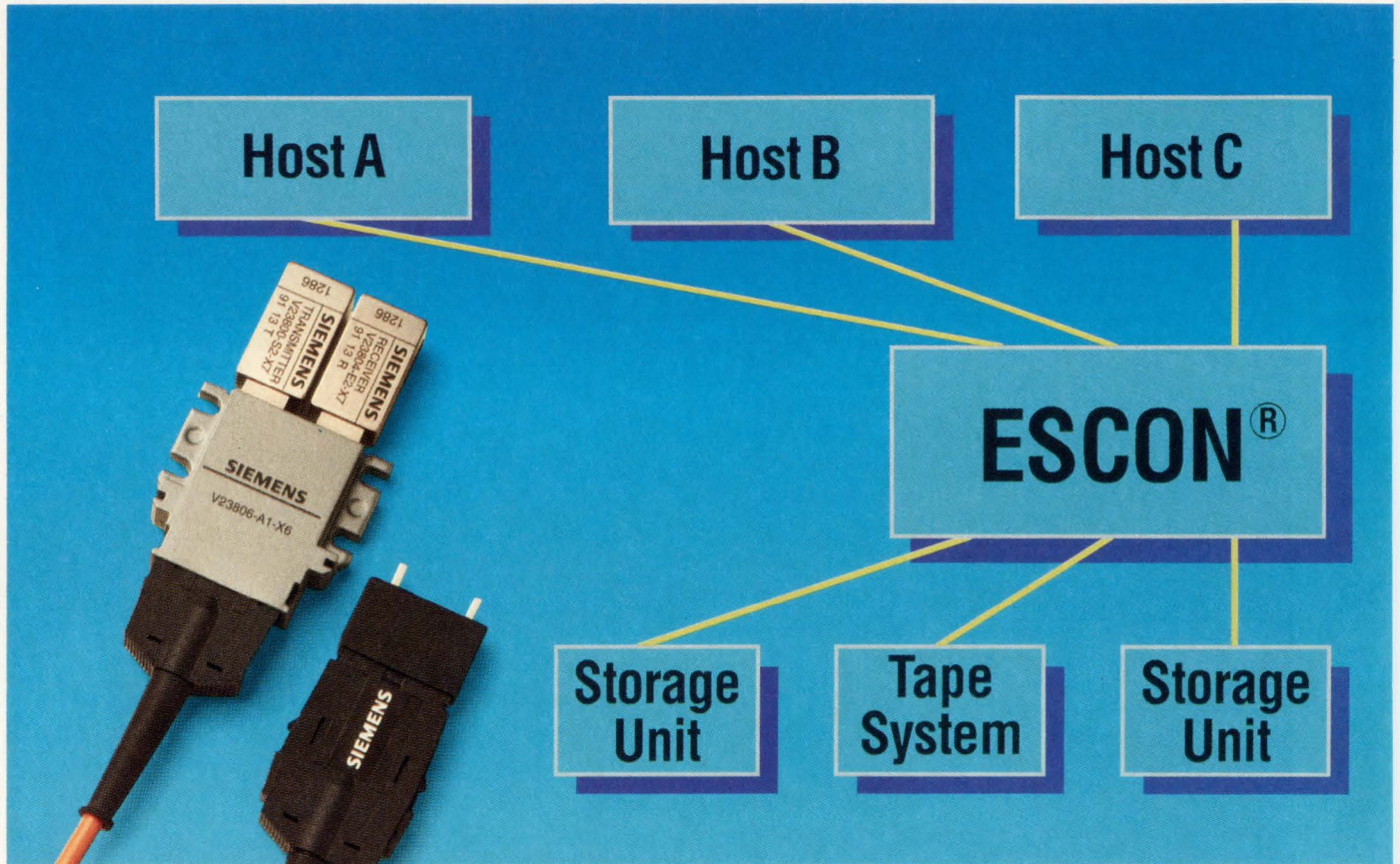
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## From napkin to production



**M**any of the world's greatest accomplishments started out as scribbles on a napkin. Whatever medium for expression is available when a brainstorm occurs is fair game for conceptual capture.

While pencil and paper have survived for hundreds of years as the key means of conceptual capture, their days are numbered. True, paper and pencil will probably be around forever, but their use as a principal means of data exchange is already gone.

### ■ Get the lead out

Young engineers moving up through the ranks today may not remember the days of ammonia blueline drawings and microfiche. Using a logic template, paper and a pencil (or pen for the confident), an engineer could quickly capture one or multiple pages of a schematic. When completed, copies were passed through a blueline machine, or photographed for microfiche and stored by the Configuration Management department.

The method is straightforward and efficient. But a problem arises when editing is necessary. In the highly iterative world of design, rarely (if ever) is a schematic drawn just once. Most often, the original schematic is completely different than the finished production schematic. This is because design refinement is taking place manually through the redundant and time-consuming iterative loop. Each time, a new schematic must be drawn, often from scratch.

Computers enter the scene. While the initial feeling of schematic capture on a computer was "Wow, that's neat," what shackled the growth of schematic capture was the reluctance of many engineers to take the time to learn the software well enough to be productive. Early software was not very user-friendly or intuitive, and it was often clumsy in the ways it captured and stored data.

Modern schematic capture, however, is clean, streamlined, efficient, and *cheap*. What's more, it's senseless to have many high-cost and higher performance workstations around just to perform schematic capture when the PC can easily handle all aspects of schematic creation, editing and output in formats usable by other back-end design or layout programs.

As a result, many of today's PC-based schematic capture programs are finding widespread use and acceptance as they provide engineering managers with low-cost, yet highly productive, design seats for their engineering teams and departments. But with the many choices comes wading through advertising and media hype to find the features that make one package or another the most suited to your needs.

### ■ Tools of the trade

An effective modern schematic capture tool creates an automated way of solidifying concepts in graphical form. Primitive elements from vendor supplied libraries or user-generated libraries are placed on a graphical workspace, moved around and interconnected. Labels define key signals, text for documents and comments, connectors, headers, standoffs, and module ports connected to all signals that are I/O, power, test points, and inter sheet schematic pages. Output is generated as documentation and as formats to be passed along to other design tools.

Choosing the right schematic capture program is similar to buying a car without trade-in allowances. Price is a factor, as well as speed and performance (with options which can be used to tailor both for your specific purpose). Especially important is compatibility. Don't buy a sports car if you need to haul furniture. With schematic capture software, you won't want to get a package more suitable for ASICs if you're making printed circuit boards (PCBs).

What differentiates some schematic capture programs today is whether or not they're bundled into applications packages or come as flexible, general-purpose packages. Both exist and both have their merits.

Bundled packages like EE Designer from Visionics (Santa Clara, CA), Highwire from Wintek (Lafayette, IN) and PC-CAPS V. 5.02 from P-CAD (San Jose, CA) offer bundled systems with consistent user interfaces and operating environments best suited for PCB design. Included in many of these packages are digital and analog simulators; layout aids like rats nesting and force vectors; library maintenance tools for schematic, simulation and layout models; autorouters; design and electrical rule checkers; automated place-



## PCs IN DESIGN

ment of components; and photoplot generation tools for Gerber output.

Special features also differentiate these packages. Visionics, for example, includes a thermal analysis package for heat modeling. P-CAD features a unique trace density histogram as a placement aid. Viewlogic Systems (Santa Clara, CA) supports VHDL in and out, making its simulator ideal for ASICs, programmable logic devices and field-programmable gate arrays (FPGAs).

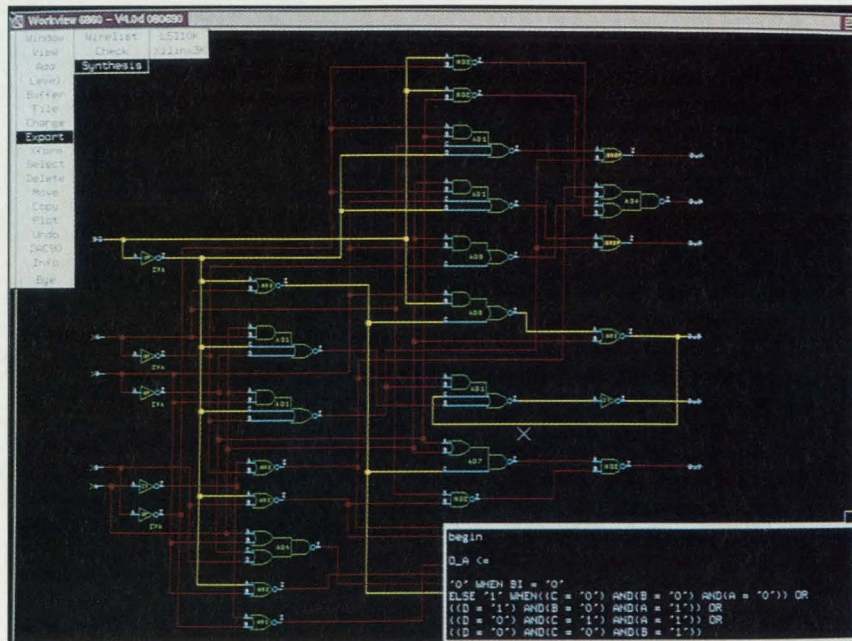
Others, like Accel Technologies (San Diego, CA), Omation (Richardson, TX) and OrCAD (Hillsboro, OR) provide general-purpose schematic capture programs to be used with a variety of independent third-party back-end packages. It's like saying, "I'll take a Ferrari body with a Mercedes chassis, and a Rolls Royce engine with a Chrysler transmission." You're assembling the vehicle which best suits your needs and desires, even though it may be a little more complicated at first to build and learn.

The first approach is best for entry-level designers who shouldn't be inundated with an entire system design tool. Learning to do just schematic capture can be accomplished quickly, and within a week, a designer is productive. Seasoned designers can take advantage of general-purpose tools to put a system together that exactly suits their needs. For example, one designer's needs might be satisfied with software from OrCAD for schematic capture; from Aldec for digital simulation; MicroSim for linear simulation; Data I/O for PLD design; Accel for printed circuit board design; and Viewlogic for FPGA design, and make these discrete packages communicate with each other to pass data back and forth.

### ■ Tangled in a net

Netlists contain all the connectivity information for the entire schematic including reference designators of each device, pin name and number, net name, and even timing attributes and thermal properties. As a matter of fact, every component can have multiple properties associated with it to describe electrical values, tolerances, types, etc.

As such, netlists can drive simulators, printed circuit board design programs, PLD and FPGA fitting programs, and even ASIC design tools. The simple automation of schematic entry travels along a system's growth path—and its best benefit comes when schematic capture netlists are passed to other specific back-end design tools. Both de facto and "agreed upon" standards are used. For many years, the FutureNet format was adopted as a de facto standard. As a result, many companies geared their programs



*In anticipation of increasing user demands, Viewlogic provides support for VHDL in synthesis of schematics and VHDL output generation.*

to accept FutureNet format data files. Recently, EDIF Vers. 2x has been adopted as the basic interchange format and hardware description languages (HDLs) such as VHDL may be overtaking this soon.

Nevertheless, each company's software uses its own internal format, so either the translators in back-end programs must decode files from other systems, or the schematic capture programs must generate netlists in the format of another tool. Both are done, but it's probably best to have a flexible schematic capture tool that can generate multiple output formats just in case.

For example, the OrCAD schematic capture program can generate standard EDIF (Electronic Data Interchange Format) and FutureNet formats, as well as a dozen or so different specific formats. This lets them source schematic files to most anyone's software. Accel's Tango also generates netlists in standard EDIF notation as well as FutureNet, PSpice and P-CAD formats. Likewise, Omation's Schema generates netlists in 15 formats including PSpice and EDIF.

The piecemeal system approach is more work than using a bundled system, but permits cherry picking for your needs. The key thing to be aware of is the standard interconnection format used to transfer data between programs. Many users write translators and converters themselves to make tools talk to one another in an automated fashion, even though the interchange formats are "compatible."

The schematic capture tools may represent pin names as AC 1, AC 2, DCOUPLUS, and DCOU-MINUS. The layout footprint in the printed circuit board program may represent the pins for the package as pin 1, 2, 3, and 4. The netlist will not recognize these components, nets and interconnections. The



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## PCs IN DESIGN

same may be true with transistors (emitter, base, collector), diodes and polarized capacitors (anode, cathode), and other devices depending on how the libraries represent this data.

While these will be trapped out as error messages and warnings, it requires either manual editing of the netlists, writing utilities to do your conversions, or editing the libraries to make the software compatible (even though it's already supposed to be).

All modern schematic capture tools have some form of library editing and maintenance. While the different structures and logical approaches taken to library maintenance vary from program to program, they are all either graphical or textual descriptions of library elements. When choosing, check out the library editing features for yourself.

Also, check out the supplied libraries which come with the schematic capture program. Many times, extensive libraries of thousands of parts and shapes are available from the schematic capture program company, or even included with the schematic capture program. The editing technique is often a matter of personal preference, and the supplied library robustness may make your life easier.

### ■ Design structure for top-down approach

In contrast to a single-sheet schematic, multisheet or hierarchical schematics can house massive designs while keeping track of all signals and nets. Multisheet schematics are just that, many sheets which hold all the elements and interconnections for the system they represent. Hierarchy is a bit more complex, and introduces a little more overhead, but provides the best way of performing top-down design.

Hierarchical designing is sort of like cocktail napkin designing. Upper-level abstract symbols represent large blocks of overall functionality. Elements on a top-level hierarchical design are pushed into revealing lower-level, less abstract and more specific elements which again can be pushed down until at the lowest level, only library elements in primitive form are seen.

An advantage of hierarchical designing is self-documentation. Upper-level blocks can be used for training of users and sales persons, and even in manuals and promotional pieces. Lower-level blocks can be used for tech support, and the lowest levels can be used for repair, rework and diagnostics. Also, after a short transition time, the designer's thought process conforms to the hierarchy and makes larger designs more simple to grasp and understand.

Key in the list of benefits associated with schematic capture are the electrical and design rule checking that can take place automatically. With humans checking, errors are easily introduced, and even with 99 percent efficiency, that's still 10 errors in a 1,000 net design.

With computers checking the design, tests for outputs shorted together, undriven inputs, unconnected outputs, and even fan out and loading can be done in the wink of an eye. This one step eliminates the tedious and time-consuming chore of manually inspecting each sheet after each iteration.

Other areas to check out include manuals, user interfaces and tech support. It's nice to have comprehensive manuals, but a rack of 10 or so full-sized 8½ in. by 11 in., three-ring binders may intimidate many users and make it harder to find simple but specific information. On the other hand, single-book manuals may not contain all the information needed to answer your questions. This too is a matter of preference, but the availability of tech support may minimize this problem.

While some companies have voice lines, others have bulletin board systems and user groups to find out how responsive and available the tech support is for the product you're investigating. Make a call or two, even before you buy, to see how long you're on hold and what week you get a call back. After all, a design can be stopped dead in its tracks if the designer doesn't know how to proceed to the next step.

User interfaces have come a long way in simplifying the learning and using of today's schematic capture tools. The mouse or keyboard can provide an excellent vehicle for computer control when properly interfaced to the software. While this is a matter of choice, a demo or video will give insight as to what personality the tool has.

One new development is the use of a shell to tie together different but related tasks in the design process. P-CAD, for example, uses a system shell which makes it easy for the designer to traverse from one stage of design to another. OrCAD now also provides a control panel shell which not only links OrCAD tools to each other, but also helps users link OrCAD's schematic capture with competitors' back-end tools. This approach is analogous to the framework efforts under way among workstation-based CAE vendors.

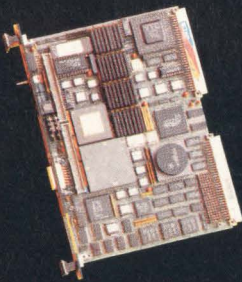
Always key in the decision-making process is price. While simple, yet powerful, schematic capture programs can sell for under \$1,000, others may be \$10,000 or more per design seat. Find out what features you really need and know what the ultimate goal of the design system is to be. For example, a design team designing circuit boards may choose a low-cost package from Accel, Omaton or OrCAD. A more advanced design team aiming at FPGA, ASIC and multichip modules (MCMs) may opt for Viewlogic's more expensive package which is designed with networking built-in and many third-party links to ASIC and FPGA manufactures.

Program and data migratability are related, but separate. Most PC-based schematic capture tools provide growth paths to other workstation platforms. In today's world, the hardware may be outdated within a year or so, but the database is a valued effort worth conserving and passing along to future generations of hardware and software. Either way, it's good to be aware of the growth path option available to you before you buy.

*Jon Gabay is a free-lance editor with extensive design experience. He has written for all of the specialized CAE/CAD publications at one time or another, including High Performance Systems, Engineering Workstations and, most recently, Design Automation.*



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**SysCOMP**

## **Who will attend SysComp/92-West?**

Attendees will be primarily design engineers and design engineering managers involved in the development and integration of OEM systems and subsystems. Given today's emphasis on cost, quality, time-to-market and concurrent engineering, **SysComp/92-West** will also attract attendees from the ranks of test, manufacturing, QA/QC and purchasing. Simply put, the technical program is aimed at all those engineers and managers who play a critical role in making the performance, cost, quality and time-to-market decisions pivotal to the success of state-of-the-art OEM systems and subsystems in today's competitive markets.

### **In particular, the SysComp/92-West Technical Program is targeted at engineers and engineering managers who are:**

- Involved in the selection and integration of microprocessors, as well as those working with bus architectures (either proprietary or open such as PC/AT/EISA and VME), and who are concerned with the impact of their decisions on the performance, functionality and marketability of the products and systems they're developing.
- Evaluating, selecting and integrating mass storage subsystems (e.g., disk drives, tape drives, optical drives), mass storage controllers and interfaces.
- Evaluating, selecting, customizing and integrating power supplies (switching, linear and UPS), regulators, converters, and batteries into equipment and systems.
- Evaluating, selecting and integrating CRTs, flat panel displays, graphics controllers, graphical user interfaces (GUIs) and other user interfaces into products.
- Evaluating, selecting and integrating software for general-purpose computing (e.g., MS-DOS and Unix-based systems), embedded control and real-time.
- Directing design-for-test, design-for-manufacturability, EMI/RFI, packaging and thermal management efforts, and managing the interaction between system design, manufacturing, purchasing and test.
- Implementing concurrent-engineering programs that bring together design, manufacturing, test, purchasing and marketing to reduce costs, improve quality, cut time-to-market and compete in world markets.

## **What products are attendees designing?**

- Within the computer and peripherals industry, designers are concerned with microprocessor architectures, operating systems, mass storage, display technologies, and input/output devices. And with the proliferation of laptop computers, compactness and ruggedness have become critical design and manufacturing issues.
- Within the telecommunications and networking industry, designers are developing new modems, MUXes, bridges, routers, etc. for LANs and WANs. They're concerned with protocols, standards, and physical and link layer solutions in silicon, modules, and at the board level.
- Within the process control and factory automation industries, data acquisition, motion control and robotic systems are being designed. Many of these are microprocessor based board-level systems and rely heavily on data converters, machine vision, and power handling subsystems.
- Within the military and aerospace industry, engineers are designing fault-tolerant systems, radiation-hardened computers, and hardware that meets appropriate emission specifications. These systems make heavy use of fiber optics and secure interconnects, EMI/RFI suppression techniques, and advanced packaging techniques.
- Consumer electronics engineers are designing low-cost systems that rely on automated assembly, clever packaging, and test—all at the lowest possible cost. Future applications such as HDTV and multimedia will play a major role in the revitalization of the U.S. electronics industry.



## What's the focus of the Technical Program?



**SysComp/92-West** is a three-day systems-oriented conference and exhibition with opportunities for presentations on a wide variety of OEM system-level design and integration topics. **SysComp/92-West** is intended to bridge the information gap between passive/discrete component shows such as Wescon, and VAR/VAD/end-user exhibitions such as Comdex. The program will combine lectures and tutorials (of varying length) on a broad array of topics critical to the timely and cost-effective evaluation, selection, development and integration of major system components—both hardware and software. Several key areas of concern will be addressed in the Technical Program:

- Microprocessor/system architectures, and their impact on OEM integration.
- Bus architectures, including VMEbus, Multibus II, ISA/EISA, MicroChannel, and Futurebus+ bus, and their impact on OEM integration.
- Power sources, including developments in switching technologies, converters, and batteries, with emphasis on their relationship to the size, cost and manufacturability of electronic/computer products.
- Display and interface technology, including advances in hardware, hardware/software interfaces and graphical user interfaces.
- Mass storage technology and the impact of new developments in media (disk, tape, optical), interface standards, and controllers on system performance, cost and reliability.
- Embedded software programming, with an emphasis on realtime kernels, standards and development tools.
- System packaging, including EMI/RFI control, thermal management, and designing for manufacturability.
- Concurrent engineering and achieving cost, quality and time-to-market goals.

### **You are invited to submit proposals for presentations in the above areas of interest, addressing specific topics such as:**

Microprocessor architectures and their impact on subsystem design.  
Nonvolatile memory and its applications.  
The system costs of microprocessor selection.  
Embedded PCs as building blocks.  
Backplane bus performance and selection.  
Next-generation bus architectures.  
Design for testability and built-in self test.  
Distributed power systems.  
FDDI and other high-performance interfaces.  
Battery technology and its impact on portable system design.  
Cost vs. performance tradeoffs in displays.  
Emerging mass storage technologies and the impact on system design.  
High-density cartridge tape drives.  
Fault-tolerant and mission-critical software.  
Advances in printed circuit board technology and impact on test and manufacturing.  
Software quality control and maintenance.  
Controlling EMI/RFI and EMI/RFI standards.  
Cost/performance alternatives in electronic packaging.  
Evaluating power supply performance vs. cost.  
High-density packaging and interconnects.  
ICs for power distribution and management.

Applications of "smart power" technology.  
Flat panel display design, manufacturing, cost, yield and integration.  
Optimizing quality through concurrent design.  
Power-management schemes.  
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Quick turnaround techniques for multi-chip module development.  
Shock, vibration and reliability issues in hard disk drives.  
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Trends in embedded software and software-development tools.  
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Display specifications and choosing a display.  
Design-for-manufacturability strategies and solutions.  
Choosing the most cost-effective manufacturing process and contract manufacturing.  
Using multichip modules to shrink product-development time.  
Thermal management and system cooling.



## How can you participate?

If you or your organization would like to participate in the **SysComp/92-West** Technical Program, submit a brief proposal to the Technical Program Coordinator no later than **November 8, 1991**.

Proposals should be 1- to 1 1/2-pages in length and contain a one-paragraph abstract that summarizes the content and goals of the presentation and a brief outline of the major topics that would be covered in the presentation. Presenters must be technically qualified and able to answer questions from attendees. A short biography of the presenter, describing his or her technical background and accomplishments must accompany the proposal.

Acceptance of proposed presentations will be made by November 15, 1991 and a complete copy of the presentation, including all visuals and graphics, will be required no later than **December 31, 1991**.

Presentations given at **SysComp/92-West** will be published in a Proceedings and copyrights shall be assigned to *Computer Design*.

For more information or to submit a proposal contact:

John Mayer  
Technical Program Coordinator  
*COMPUTER DESIGN*  
P.O. Box 538  
Belmont, MA 02178  
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FAX: (508) 692-7780

or

John Miklosz  
Editor-in-Chief/Associate Publisher  
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In addition to the technical program, **SysComp/92-West** will feature exhibits by vendors of OEM computers, ICs, CPU boards and other board-level products, mass storage devices, displays, power sources, backplanes and enclosures, software and software development tools. For information about exhibiting at the conference, contact:

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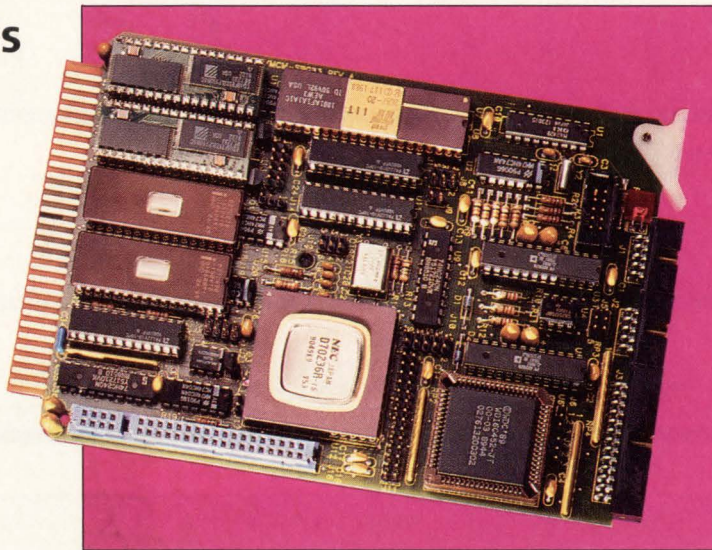
*Computer Design* magazine will be publishing the **SysComp/92-West Conference Guide**. In addition to distribution at the conference, the Guide will be mailed with the February, 1992 issue of *Computer Design*. For information about advertising contact:

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## STD CPU boards thrive on a PC budget

Jeffrey Child, Associate Editor



*WinSystem's MCM-SBC53 uses the 286-compatible NEC V53 processor. The board supports up to 1 Mbyte of memory and offers three counter/timers and an 8-channel interrupt controller. For I/O, the board provides three RS-232 serial channels, a printer port and support for SBX daughtercards.*

**A**lthough the STD Bus may not seem as glamorous as higher-end bus architectures, many system designers find the lower cost of STD boards hard to beat. While the speeds and capabilities of boards based on high-performance buses such as VME and Multibus II may be needed for some applications, such solutions, however, often don't make sense because of cost and software issues.

Today, designers integrating STD boards into their embedded control designs are facing pressures from all sides. With budget concerns tighter than ever, overall system cost is always an issue. At the same time, upper and middle management are coaxing designers to consider an upgrade path that will suit future performance needs. And engineering managers, under pressure to get their systems to market quickly, have to minimize their software development time as much as possible.

To keep pace with these needs, STD CPU board vendors are striving to produce low-cost products at performance levels that suit the end application. Meanwhile, the debate continues among STD vendors over the proper course for future STD Bus performance. Believers in STD 32 (the 32-bit extension of the STD Bus standard), including Ziatech (San Luis Obispo, CA) and a handful of others, say 32-bit memory accesses are necessary for multiprocessing and to suit future performance demands. Others disagree, saying communication across the bus should be

reserved for I/O, since most I/O devices only need eight bits anyway.

The current selection of boards for STD Bus CPUs range from highly-integrated, single-board computers to high-performance engines for handling the central processing tasks of a multiboard system. And there's still a selection of 68000- and Z80-based STD boards for those who don't need to upgrade performance or don't want to abandon their software investment. If there's a trend in new STD CPU board designs these days it's toward personal computer compatibility, or more specifically, toward board designs based on processors that can run DOS.

Providing DOS compatibility helps ease the task of software development. Users can operate both DOS programs on STD Bus computers and implement the familiar DOS structure in the target applications. This allows debugging of programs on the target system using advanced DOS-based hardware tools, whether it runs with or without DOS in the final system.

### ■ Riding the PC wave

Easing the task of software development isn't the only reason STD CPU manufacturers are focusing on PC-compatible designs. Hoping to maintain STD's position as a low-cost, workhorse bus for embedded control, board makers recognize the cost advantages inherent in using chips targeted for the PC market. The extreme price pressures and high volumes of the PC marketplace are

expected to favorably impact the price and availability of microprocessors and chip sets designed for those systems. "It's almost like the PC has become the minimal building block for embedded intelligence," says Bob Burckle, vice-president of WinSystems (Arlington, TX). "There's many other contenders like Sparc and RISC, but you can't deny the installed base of PC systems out there."

Leveraging off hardware developments in the PC world doesn't necessarily mean building STD boards based on Intel's 80X86 family of processors. Since the 8088, 286 and 386SX processors were designed for desktop systems, not for embedded control, there's no true high-speed, high-integration, 16-bit processor in the Intel 80X86 line. Intel doesn't offer a high-speed derivative of the 286, for example, even though the 286 can outperform the 386 at equivalent speeds. With this in mind, many of the latest STD CPU boards use processors like the V40 and V53 from NEC (Mountain View, CA).

One such board is WinSystem's MCM-SBC53, an AT-compatible STD CPU board based on the 10- or 16-MHz V53 processor. The board supports up to 1 Mbyte of memory in the form of EPROM, EEPROM, flash memory, or battery-backed SRAM. I/O on the board includes three RS-232 serial channels and a Centronics-compatible parallel printer port. In addition, on-board expansion is provided via an 8-/16-bit interface to SBX daughtercards. The SBC53 also



## PRODUCT FOCUS/STD CPU Boards

Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	RAM (bytes)	Non-volatile memory (bytes)	DMA channels (no. and width)	I/O ports	On-board/inter-board expansion	Price
<b>Advanced Micro Systems</b> 2 Townsend W, Nashua, NH 03063 (603) 882-1447									<b>Circle 301</b>
BAS-52	8052-Basic	12	—	32k	8k to 64k	—	24 output drivers, 24 filtered inputs	2 RS-232	—
CPU-32	8032	12, 20	—	32k	8k to 64k	—	same as above	2 RS-232	—
<b>Andufet Digital</b> 545 W Allen Ave, Unit #6, San Dimas, CA 91773 (714) 394-0171									<b>Circle 302</b>
500-001	80188	16	—	256k	256k	2	16 TTL I/O, 1 RS-232, 1 RS-485	—	\$415
<b>ASC Systems</b> Box 566, St Clair Sh, MI 48080 (313) 882-1133									<b>Circle 303</b>
PC/286	80286	12, 16, 20	80287	4M	128k	1 16-bit	2 parallel, 2 serial	local memory and I/O bus	\$990
PC/88	80C188	5, 10	80C87	1M	64k	1 8-bit	2 parallel, 1 serial	local memory and I/O bus	\$490
PC/386	80386SX	16, 20	80387	8M	512k	1 16-bit	2 parallel, 1 serial	local memory and I/O bus	\$1,490
<b>C-Matic Systems</b> 2 Millbrook Business Pk, Crowborough, E Sussex, UK TN6 3JZ 44-892-665688									<b>Circle 304</b>
1804	Z80	4	—	64k	64k	—	1 RS-232	—	—
1806	Z80	4	—	64k	64k	—	1 PIO	—	—
1868	68010	8	—	8M	64k	—	—	—	—
<b>Computer Dynamics</b> 107 S Main St, Greer, SC 29650 (803) 877-8700									<b>Circle 305</b>
CPU-AT	80C286	20	80287	4M	512k	2	2 COM, 1 printer	CGA, VGA, flatpanel	\$995
CPU-XT	8088/V20	8	8087	640k	128k	4	2 COM, 1 printer	same as above	\$695
CPU-186	80C186	16	80187	512k	256k	2	2 RS-232, 24 PIO, 2 RS-232/422/485	iSBX	\$595
CPU-188	80188	10	8087	1M	128k	1	2 serial, 28 PIO	iSBX	\$470
<b>Cubit Div, Proteus Industries</b> 340 Pioneer Way, Mountain View, CA 94041 (415) 962-8237									<b>Circle 306</b>
8660R	80C186	12.5	—	256k	256k	1 16-bit	4 8-bit parallel, 2 RS-232	iSBX	\$849
8700	80C186	16	—	2M	256k	1 16-bit	—	—	\$760
8020	64180	4.6	—	64k	128k	2 8-bit	2 8-bit parallel, 2 RS-232	—	\$465
<b>Enterprise Systems</b> 6 Grove St, PO Box 698, Dover, NH 03820 (603) 742-7363									<b>Circle 307</b>
10812	6502	1, 2	optional	24k	24k	—	1 serial, 2 parallel	MEMEX, IOEXP	\$262.50
10809	6809	1, 2	—	24k	24k	—	1 serial, 2 parallel	MEMEX, IOEXP	\$262.50
<b>Matrix</b> 1203 New Hope Rd, Raleigh, NC 27610 (919) 231-8000									<b>Circle 308</b>
TS9B	6809	2	—	64k	64k	—	2 serial, 32 parallel	—	\$325
MF9B	6809	2	—	64k	32k	—	2 serial	—	\$305
SP9B	6809	2	—	80k	32k	—	1 serial	—	\$255



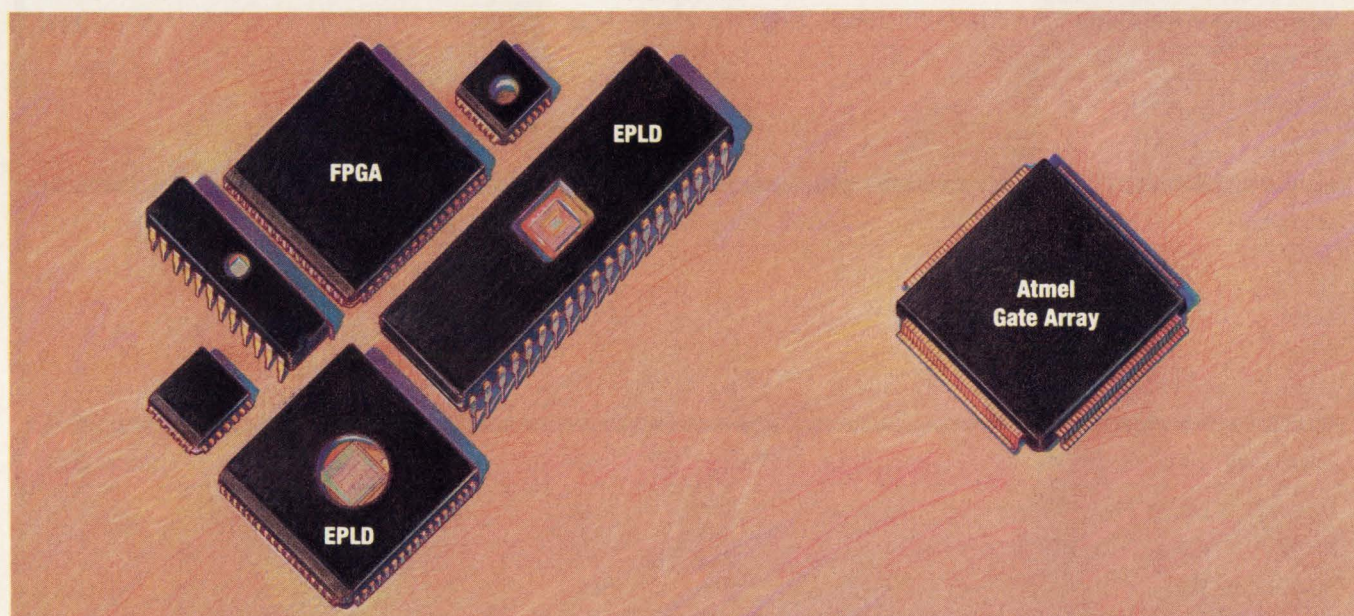
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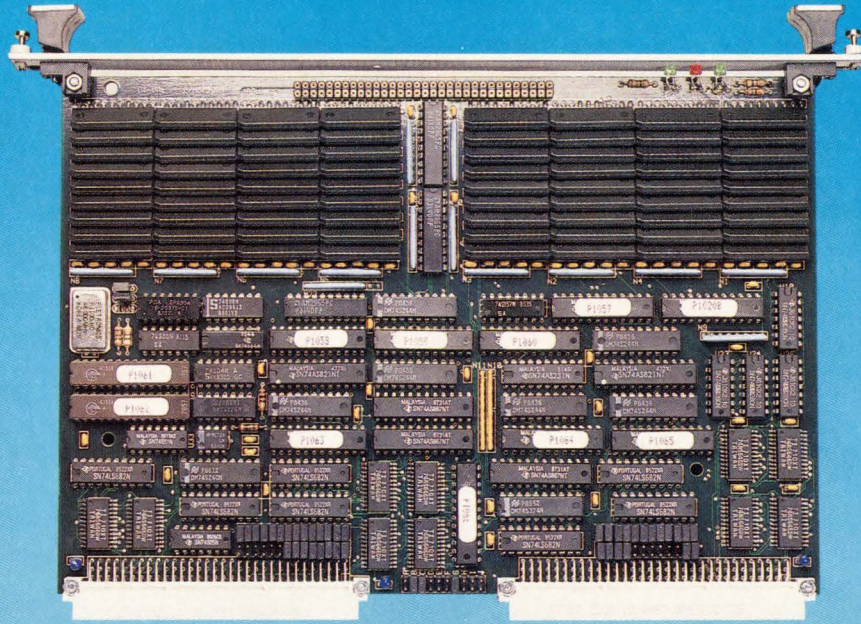


**PRODUCT FOCUS/STD CPU Boards**

Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	RAM (bytes)	Non-volatile memory (bytes)	DMA channels (no. and width)	I/O ports	On-board/inter-board expansion	Price
<b>Micro-Aide</b> 685 Arrow Grand Cir, Covina, CA 91722 (818) 915-5502 <b>Circle 309</b>									
80-0040	V40	8, 10	—	1M	1M	—	1 RS-232, 1 RS-485, 1 parallel	—	\$295
80-0046	V40	8, 10	—	1M	1M	—	2 RS-232, 1 parallel	—	\$385
80-0386	386SX	16, 20	387SX	16M	1M	—	—	—	\$600
80-0026	Z80A/Z80B	4, 6	—	128k	128k	1 8-bit	2 RS-232, 1 8-bit I/O	MEMEX, IOEXP	\$245
80-0036	Z80A/Z80B	4, 6	—	128k	128k	1 8-bit	2 RS-232, 1 IEEE-488	—	\$275
80-0037	Z80A/Z80B	4, 6	—	128k	128k	1 8-bit	2 RS-232, 1 PIO	—	\$260
<b>Microcomputer Systems</b> 1814 Ryder Dr, Baton Rouge, LA 70808 (504) 769-2154 <b>Circle 310</b>									
MSI-C988	V20	5	—	64k	64k	—	3 digital I/O, 2 RS-232	—	\$395
MSI-C850	NSC800	4	—	32k	32k	—	—	—	\$285
MSI-CZ82	Z80A	4	—	16k	16k	—	2 RS-232	—	\$285
<b>Micro-Link</b> 14602 N US Hwy 31, Carmel, IN 46032 (800) 428-6155 <b>Circle 311</b>									
STD207	68000/10	8, 12	—	512k	—	—	1 RS-232, 1 RS-232/485, SCSI, Centronics	—	\$500
STD220	68020	12, 16, 20	68881	2M	—	—	2 async serial	—	\$715
STD224	68020	12, 16, 20	68881	16M	—	—	—	—	\$895
<b>Micro/sys</b> 3447 Ocean View Blvd, Glendale, CA 91208 (818) 244-4600 <b>Circle 312</b>									
SB8186	80C186	10, 12, 16	yes	512k	384k	2 16-bit	2 serial, 1 parallel	—	\$550
SB8082	V20	5, 8	yes	64k	64k	—	1 serial, 1 parallel	—	\$295
SB8090	V20	5, 8	—	512k	512k	—	1 serial, 1 parallel	—	\$340
<b>Mitchell Electronics</b> PO Box 2626, 180B Mill St, Athens, OH 45701 (614) 594-8532 <b>Circle 313</b>									
M/E200	Z80	2.5, 4, 6	—	64k	64k	—	2 RS-232, 1 IEEE-488, GPIB	—	\$350
M/E300	Z80	2.5, 4, 6	—	64k	64k	—	2 RS-232, 2 8-bit parallel	—	\$250
<b>Octagon Systems</b> 6510 W 91st Ave, Westminster, CO 80030 (303) 430-1500 <b>Circle 314</b>									
8700	V20	9.5	—	1M	256k	—	1 parallel, 2 serial	—	\$595
9600	V25	8	—	768k	256k	—	24 parallel, 2 serial	iSBX	\$595
7100	64180	6	—	64k	32k	—	32 parallel, 2 serial	—	\$445
<b>Pro-Log</b> 2555 Garden Rd, Monterey, CA 93940 (408) 646-3654 <b>Circle 315</b>									
7870	80C286	12, 16	80287	512k to 2M	256k	7 8/16-bit	2 serial, 1 parallel	IEEE-969 iSBX	\$995
7872	80386SX	16, 20	80387SX	512k to 8M	256k to 512k	7 8/16-bit	2 serial, 1 parallel	—	\$1,495
7873	80386SX	16, 20	80387SX	512k to 8M	256k to 512k	7 8/16-bit	2 serial, 1 parallel	—	\$1,995



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- 20ns write/20ns read ACCESS TIMES in BLOCK CYCLE
- 90ns write/140ns read ACCESS TIMES in SINGLE CYCLE
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- 195ns write/195ns read CYCLE TIMES in SINGLE CYCLE
- 4MB, 8MB, 16MB, 32MB, 64MB in one VMEbus/VSB slot
- Byte Parity Error Detection
- Memory start and end addresses selectable on 256KB boundaries
- VMEbus and VSB memory start and end addresses configured independently

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### THE CI-VMEemory FEATURES:

- Low-cost high-power VME memory with 4, 8, or 16MB
- VME Revision C.1 compatibility
- Lower and upper memory addresses independently selectable in 64K byte increments
- Byte Parity Error Detection with selectable trap on Parity Error
- On-board Control Status Register

### THE CI-VSB-EDC FEATURES:

- Low-cost high-power dual-ported VMEbus/VSB EDC (Error Detection and Correction) memory
- 4, 8, 16, 32 or 64MB in one VMEbus/VSB slot
- VME Revision C.1 compatibility, VSB Revision C
- Lower and upper memory addresses independently selectable on 256K byte boundaries
- Single-Bit Error Detect and Correct, Double-Bit Detect



**Chrislin Industries, Inc.**

31312 Via Colinas, Suite #108, Westlake Village, CA 91362

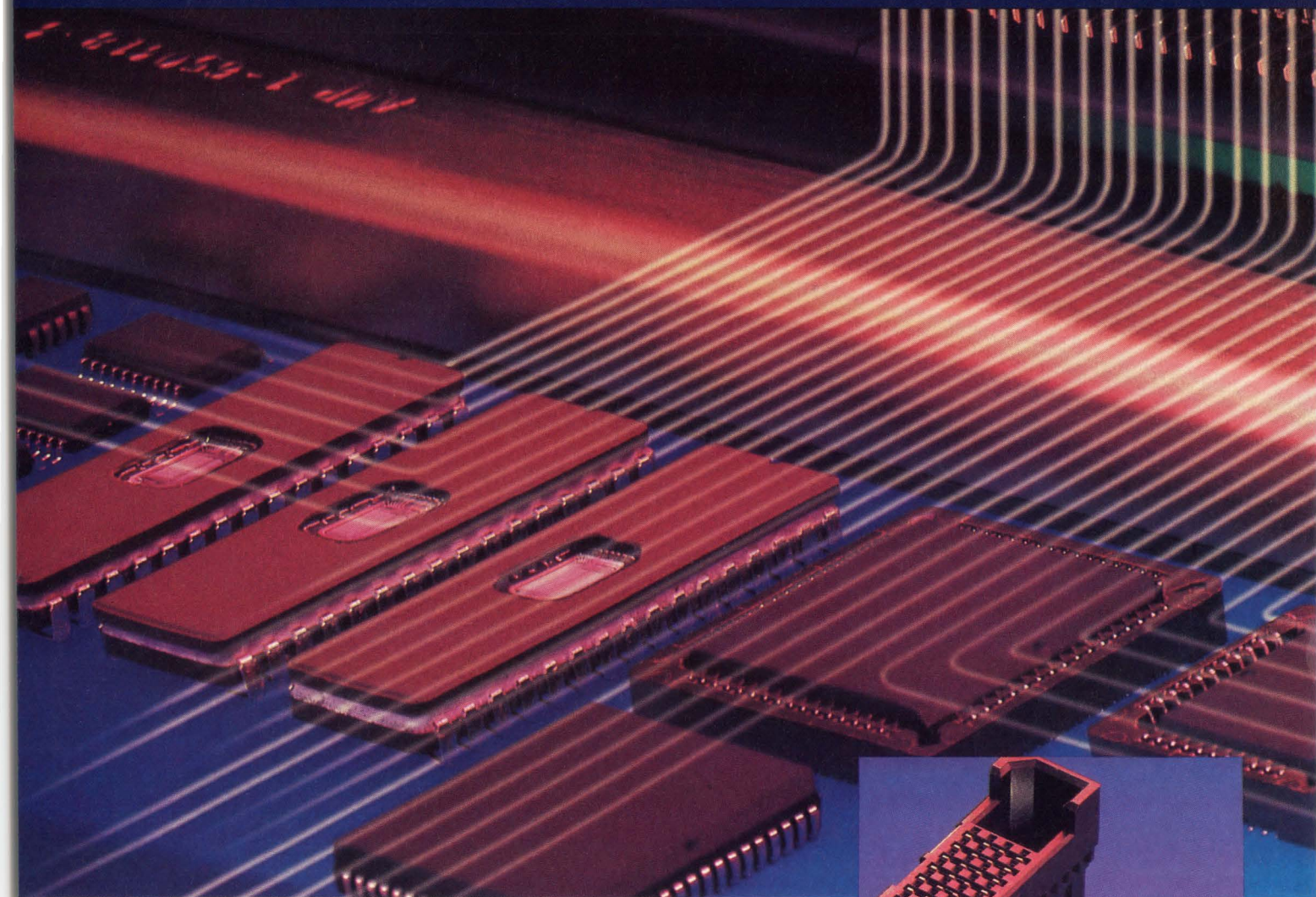
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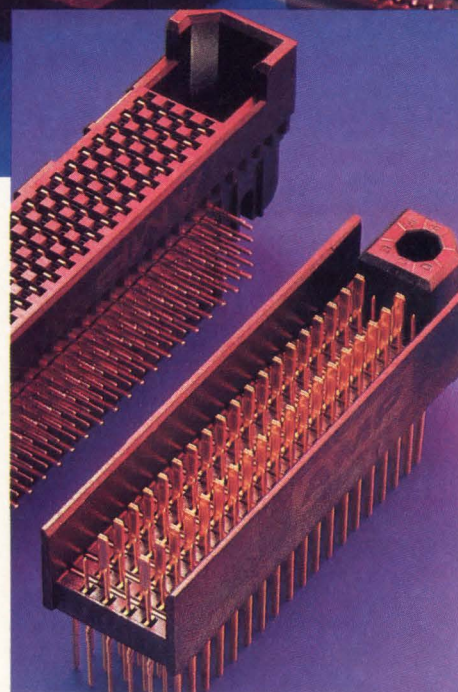
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to sub-nanosecond rise times.*

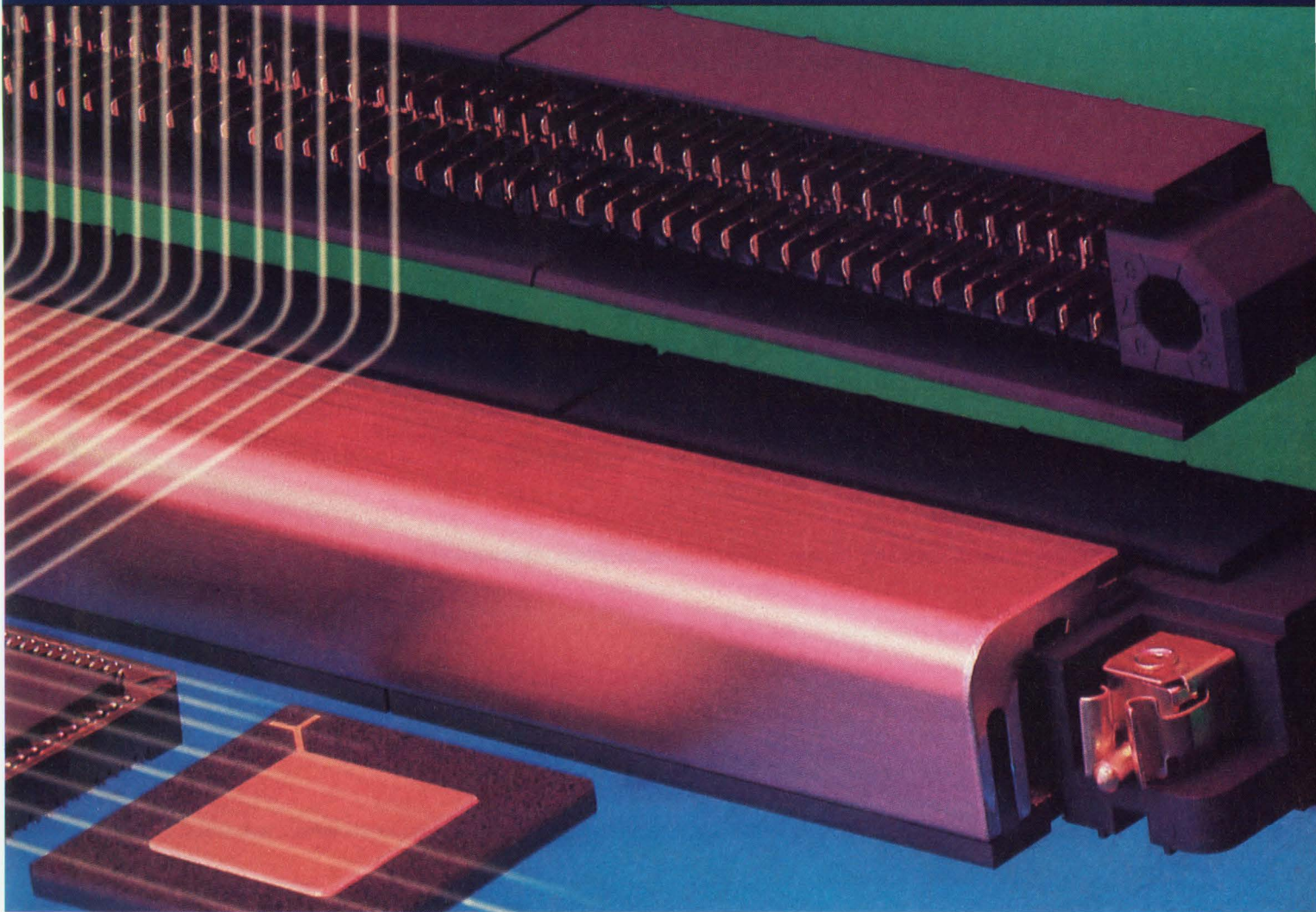


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parent to high-speed logic.

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# AMP

CIRCLE NO. 65



**PRODUCT FOCUS/STD CPU Boards**

Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	RAM (bytes)	Non-volatile memory (bytes)	DMA channels (no. and width)	I/O ports	On-board/inter-board expansion	Price
<b>R L C Enterprises</b> 4800 Templeton Rd, Atascadero, CA 93422 (805) 466-9717									<b>Circle 316</b>
TSBC-C186	80C186	10, 12.5, 16	80C187	256k	256k	2 16-bit	2 RS-232	—	\$725
<b>Robotrol</b> 925 W San Martin Ave, PO Box 990, San Martin, CA 95046-0990 (408) 683-2000									<b>Circle 317</b>
RSD7832	UPI452	12	—	32k	64k	—	1 serial, 8 parallel, 16 analog input, 2 analog output	—	\$595
RSD7808	Z80A	4	—	64k	64k	—	2 serial, 20 parallel, 3 16-bit timers	—	\$255
RSD8088	8088	4.77	—	64k	64k	—	1 serial, 20 parallel	—	\$240
<b>Systek</b> 415 N Quay St, Suite 6, Kennewick, WA 99336 (509) 735-1200									<b>Circle 318</b>
8825	V25	5, 8, 10	—	256k to 512k	512k	2 8-bit	24 parallel, 2 serial	iSBX	\$395
8850	V50	8, 10, 12	8087	512k to 128k	256k	2 16-bit	1 Centronics, 3 serial	1 bi-directional	\$595
8887	8088/V20	5, 8, 10	8087	—	64k	—	—	—	\$225
<b>WinSystems</b> 715 Stadium Dr, Suite 100, Arlington, TX 76011 (817) 274-7553									<b>Circle 319</b>
MCM-SBC53	V53	10, 16	optional	1M	1M	3 8-bit	3 serial, 1 parallel, 3 16-bit counter/timer, 1 watchdog timer	iSBX	\$595
MCM-SBC41	V40	8, 10	—	1M	1M	—	3 serial, 1 parallel, 3 16-bit counter/timer, 1 watchdog timer	—	\$295
MCM-386SX	80386SX	16, 20	optional	4M	256k	4 16-bit, 4 8-bit	1 keyboard, 2 serial, 1 parallel, 1 watchdog timer	—	\$1,495
<b>Versalogic</b> 3888 Stewart Rd, Eugene, OR 97402 (800) 824-3163									<b>Circle 320</b>
VL-186-1	80C186	16	—	1M	256k to 1M	2 programmable	1 RS-232, 1 RS-232/422, 1 Opto-22	iSBX	\$645
VL-188-1/2	80C188	5, 8, 10	—	512k	512k	2 programmable	1 RS-232/422/485, 16 parallel I/O	—	\$325-\$350
VL-7806	Z80	3, 4, 6	—	128k	128k	—	2 RS-232	—	\$221-\$250
<b>XYZ Electronics</b> 4700 North 600 West, McCordsville, IN 46055 (317) 335-2128									<b>Circle 321</b>
CPU-9A	68B09	1, 2	—	64k	32k	—	1 RS-232	—	\$325
CPU-68K8	68008	10	—	96k	96k	—	1 RS-232, 8 single bit	—	\$395
CPU-68K16	68000	16	—	3M	3M	—	2 RS-232/422/485, 1 printer, 1 SCSI	—	\$595
SB-68K16	68000	16	—	768k to 3M	1M to 3M	—	2 RS-232/422/485, 1 printer, 1 SCSI	—	\$1,300
<b>Ziatech</b> 3433 Roberto Ct, San Luis Obispo, CA 93401 (805) 541-0488									<b>Circle 322</b>
ZT 8808/8809	V20	5, 8	8087	384k	256k	—	2 RS-232/422/485	—	\$475
ZT 8830	8088	8	—	32k	32k	—	16 parallel I/O, 1 serial	iSBX	\$395
ZT 8832	V40	8	8087	512k	512k	1 8-bit	24 parallel I/O, 1 RS-232/485, 1 RS-232	iSBX	\$695



Model	CPU(s)	CPU clock speed (MHz)	Math coprocessor	RAM (bytes)	Non-volatile memory (bytes)	DMA channels (no. and width)	I/O ports	On-board/inter-board expansion	Price
<b>Ziatech</b> 3433 Roberto Ct, San Luis Obispo, CA 93401 (805) 541-0488 <b>Circle 322</b>									
ZT 8801	V40	8	—	128k to 1M	128k to 512k	—	48 digital I/O, Opto-22 compatible	iSBX	\$375
ZT 8910	386SX	16, 20	387SX	2M to 4M	64k to 256k	3 8-bit	33 digital I/O	IDE disk interface, 16-bit	\$1,850
ZT 8901	V53	16	80C287	1M	512k to 1M	2 8-bit, 1 16-bit	48 parallel, 2 RS-232/485, 1 RS-232	iSBX	\$975
ZT 89CT30	DSP56001	27	—	128k	128k	—	2 RS-232/485, 1 parallel	iSBX	\$1,050
<b>Zwick Systems</b> 17 Fitzgerald Rd, Suite 104, Nepean, Ontario, Canada K2H 9G1 (613) 726-1377 <b>Circle 323</b>									
ZSTD-112	Z84C11/13/15	10	—	1M	1M	—	40 I/O lines	—	\$475
DSTD-101	Z80	4	—	40k	40k	—	2 parallel	—	\$255
DSTD-102	Z80	4	—	64k	64k	—	2 RS-232-C	—	\$315
DSTD-103	Z80	4	—	40k	40k	—	2 parallel	—	\$255
DSTD-109	Z80	4	9511	64k	64k	—	1 RS-232-C	—	\$320
DSTD-160	68000	8	—	64k	64k	—	1 RS-232-C	memory modules	\$395
DSTD-168	68008	8	—	64k	64k	—	2 RS-232-C	—	\$345
DSTD-188	8088	8	8087	64k	64k	—	2 RS-232-C	—	\$375

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CIRCLE NO. 66



# STD BUS PRODUCTS FROM MICRO-AIDE, INC.

685 Arrow Grand Circle, Covina, CA 91722

## PROCESSOR

### MODEL

80-0026	Z80A,B CTC,DART,Memory
80-0027	Z80A,B Bat.-Backed Memory,Calendar Clock
80-0033	6809E ACIA,VIA,Bat.-Backed Mem,Cal. Clk
80-0036	Z80A,B Memory,CTC,DART,IEEE488
80-0037	Z80A,B Memory,CTC,DART,PIO
80-0040	V40 8,10Mhz Memory,LPT1,COM1,2
80-0046	V40 8,10Mhz Bat.-Backed Memory, Calendar Clock,LPT1,COM1,COM2

## MEMORY

80-0001	EIGHT 28 PIN SOCKETS FOR RAM/ROM
80-0002	512K Bat. Backed RAM
80-0017	256K RAM/ROM I/O Addressed
80-0031	256K Bat.-Backed RAM/Cal. Clock

## INPUT/OUTPUT

80-0022	24 Channel I/O Rack Interface
80-0023	24 Channel Opto-Coupled Input
80-0024	24 Channel Opto-Triac Output
80-0025	24 Channel Opto-Coupled Output
80-0028	8 Channel "In Rack" I/O
80-0030	24 Channel Opto-Output with Relay
80-0032	64 Channel (4 VIA's) I/O
80-0034	24 Channel High Speed Opto-Input
80-0025	24 Channel High Speed Opto-Output
80-0048	8 Channel "In Rack" Opto-Input with Change Of State Detector
80-0049	8 Channel "In Rack" Opto-Coupled High Power AC/DC I/O

## SERIAL I/O

80-0021	6 Port RS232 (CTC/DART)
---------	-------------------------

## MODEMS

80-0029	300/1200 Baud MODEM with optional Dual RS485/232 Serial Port and DTMF Receiver
80-0029/24	300/1200/2400 Baud MODEM with optional RS232 Serial Port

## SPECIAL FUNCTION

80-0047	Opto Isolated 8 Bit Switched Power DAC for 24/90V Brakes and Clutches
80-0003	12/24/48V to 5,+/-12V DC/DC Power Supply
80-0050	High Speed 12,14 or 16 Bit A/D Converter < 20 uSec.

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CIRCLE NO. 67

## PRODUCT FOCUS/STD CPU boards

### COMPUTERS & SUBSYSTEMS

offers three 16-bit counter/timers, a battery-backed real-time clock and an 8-channel interrupt controller.

In the last five years, most of the growth in STD CPUs has been in DOS-compatible boards. Recently, however, at least one vendor, Computer Dynamics (Greer, SC), has gone one step further by providing all the functions of a PC/AT on one STD single-board computer. Called CPU-AT, this board offers an 80C286 processor running at speeds up to 25 MHz, up to 4 Mbytes of DRAM and 256 kbytes of EPROM. Other standard features include two serial channels, a printer port and floppy and hard disk controllers. Several display options are available with the CPU-AT thanks to on-board display controllers that plug directly into CRTs and directly drive flat-panel displays. As a result, the board is able to drive a wide variety of flat-panel display types including electroluminescent, liquid crystal, plasma, and vacuum-fluorescent displays. CRT display options include CGA, EGA and VGA.

For embedded designs, Computer Dynamics offers a version of the CPU-AT without controllers for a display and disks. An embedded operating system, with all the DOS functions except drive support, is provided in EPROM. As such, the board can boot-up and run programs directly from the EPROM if a diskless system is required.

### Reluctant to migrate

System designers with a heavy investment in VME systems and 680X0-based code may be reluctant to migrate to the STD Bus. However, boards like the 7850, a 68030-based STD single-board computer from Pro-log (Monterey, CA) may provide a lower cost alternative to VME without forcing an abandonment of software investments. Aside from a 68030 processor running at 25 Hz, the 7850 features up to 4 Mbytes of RAM, two serial ports, a counter/timer, and bootable ROM.

Benchmark tests on the 7850 board, done by Pro-log customers, revealed some impressive results. Based on processing speeds in Mips, one test suggested that the board performs over 3x faster than a DEC VAX Workstation 2000.

While disagreement persists regarding the need for a 32-bit STD





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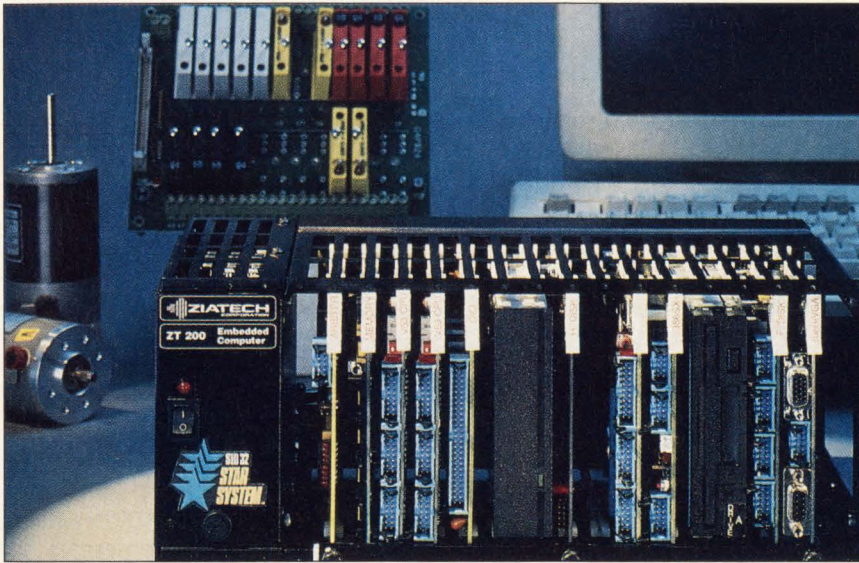
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CIRCLE NO. 69



COMPUTERS & SUBSYSTEMS



The Star System, Ziatech's new STD 32 multiprocessing system, uses the company's V53-based ZT 8901 CPU board as its main master. Up to six other ZT 8901 boards can be used in the system as real-time processors. Based on the NEC V53 processor, each ZT 8901 provides up to 1 Mbyte of RAM and can drive 48 digital I/O lines.

DOS-compatible, single-board computers that operate independently while sharing the same disk and video controllers. The system uses the company's V53-based ZT 8901 CPU board as the permanent master, and up to six other ZT 8901 boards can be used in the system as real-time processors. As an option, Ziatech's 386SX-based ZT 8910 CPU board can be substituted as the permanent master.

Based on the 16-MHz V53 processor, the ZT 8901 provides up to 1-Mbyte RAM, 512-kbytes PROM, three serial ports, and 48 lines of digital. Ziatech designed its own ASIC to do the digital I/O. Because the ASIC is totally bidirectional on all 48 lines, it lets users program each I/O line as either an input or an output. If optical isolation is required, the I/O can be attached to standard OPTO-22 modules. ■

Bus, STD 32 does appear to be gaining acceptance for its multiprocessing capabilities. In fact, at the first meeting of the STD 32 Special Interest Group at Buscon/91-East, the multiprocessing capabilities of STD 32 was the main theme. At the meeting, new STD 32 boards were announced including a slave I/O processor from Universal Systems (Flint, MI), and a CPU board from Versalogic (Eugene, OR). And Ziatech introduced a complete multiprocessing system based on STD 32.

Developing multiprocessing systems on STD 32 is much easier than on other buses, such as VME, claims Alan Beverly, engineering manager at Ziatech. "VME systems have had multiprocessing for a while, but it's fairly difficult for the average user to sit down and develop code for it," says Beverly. "In VME, there's no standard software, like DOS, that the average designer is familiar with." Due mainly to its multiprocessing capabilities, Beverly sees the STD Bus marketplace actually overlapping the low-end VME market. There's software available that lets users run multiple copies of DOS in the same backplane while letting different boards share the same disk resources.

According to Ziatech, the Star System, its new STD 32-based system, is the first to incorporate multiple

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CIRCLE NO. 70



## Software generates test patterns for boundary-scan boards

As printed circuit boards incorporate more high-density, small-scale packaging technology, boundary-scan is emerging as a logical alternative to traditional bed-of-nails test procedures. But developing test patterns for densely-packed printed circuit boards can be a time-consuming prospect, especially when boundary-scan devices are mixed with conventional components. The latest version of Teradyne's printed circuit board test software, Victory 2.0, promises to address these time-consuming test development problems with several major enhancements.

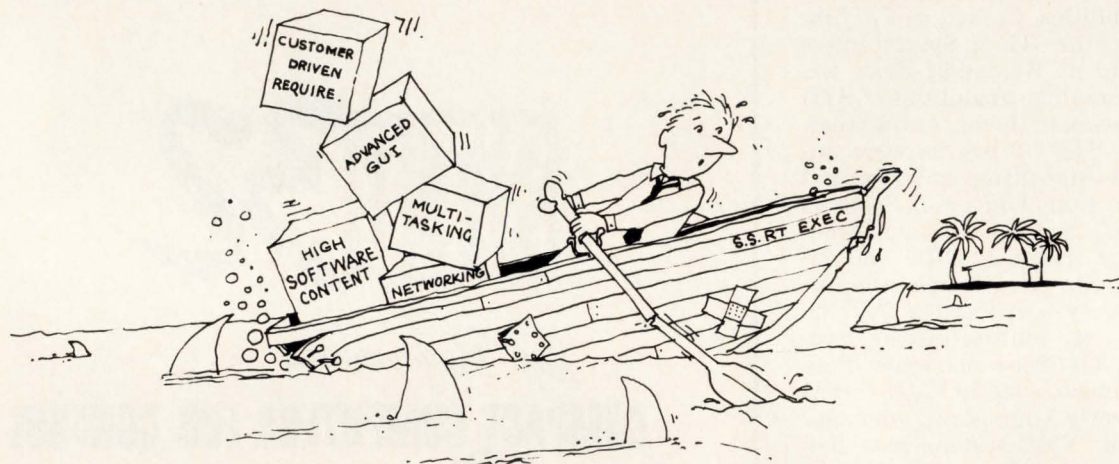
Victory 2.0 features two new software modules, one for testing non-boundary-scan circuitry that lacks bed-of-nails test access and the other for testing the internal circuitry of boundary-scan devices. In

addition, the software includes a process-oriented graphical user interface (GUI) based on X-windows, OSF/Motif and Microsoft Windows 3.0. The new release also supports the IEEE 1149.1 boundary-scan standard and can be adapted to other boundary-scan designs.

The Victory software package accepts industry-standard Boundary-Scan Description Language (BSDL) data about a circuit's boundary-scan implementation. It then analyzes this data and automatically generates the go/no-go patterns needed for particular test applications. Before using a BSDL description as input for test generation and diagnostics, users can employ Victory to generate BSDL verification patterns, which are used to test each boundary-scan device and verify the

accuracy of each BSDL file. Checking that each scan cell matches its expected physical location identifies any BSDL errors and avoids potentially time-consuming debugging of board-level tests and diagnostics later on.

For boundary in-circuit testing (BICT) of boundary-scan devices that can be accessed through conventional bed-of-nails fixturing, the Victory software automatically generates patterns that provide 100 percent pin-level fault coverage of defects such as open circuits and stuck-at pins. Victory takes into account device constraints (such as pins tied to power or ground or pins tied together) to eliminate manual editing of the patterns. In addition to the BICT patterns themselves, Victory generates patterns that control components surrounding the device under test (DUT) in the boundary-scan chain, ensuring proper isolation of the DUT and test repeatability.



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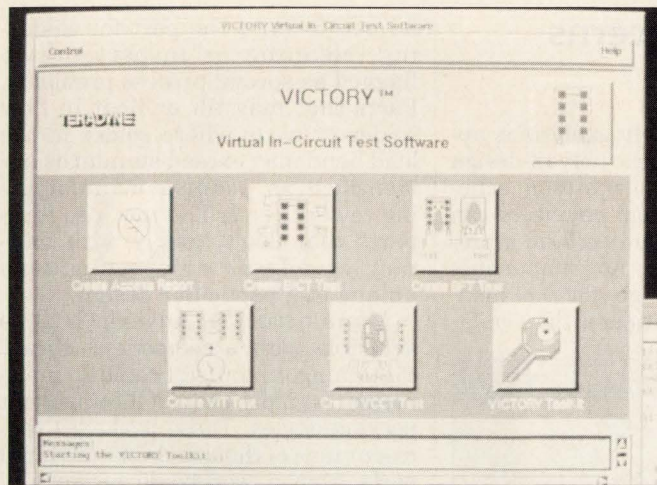
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## CAE/CAD TOOLS



Teradyne's Victory 2.0 software features a graphical user interface (GUI) which lets users select test generators, launch processes and access databases by clicking on icons.

Victory Boundary Functional Test (BFT) software lets users test the internal circuitry of individual boundary-scan devices. BFT can be used to verify that the correct device is loaded on the board and to verify that a device is functioning properly. The Victory BFT performs four types of tests: the software automatically generates patterns to test the internal logic of the IEEE 1149.1 test access port circuitry and scan registers; it applies conventional parallel patterns to the DUT through the boundary register; it executes a device's built-in self test (BIST) and it applies serial scan patterns through the boundary register to devices designed with internal scan.

Another feature of the latest release, Virtual Component/Cluster Test (VCCT), lets the boundary-scan register be used as a virtual channel to test nonboundary-scan devices which can't be accessed by a bed-of-nails test fixture. The embedded circuitry can be either a single component or a collection of components (a cluster). The VCCT feature permits the stimulus for the embedded device(s) to be developed for conventional tests where tester channels are located at all the primary inputs and outputs of the component or cluster. VCCT software accepts these parallel patterns as one of its inputs and performs the necessary serialization so that the patterns can be applied through the boundary chain. VCCT also automatically accommodates situations where the DUT leads are accessed with a combination of real tester channels and virtual boundary-scan channels.

Victory's user interface lets users

select test generators, launch processes and access databases for viewing or editing by clicking on icons. Each of the software's test generators is represented by a graphical flow diagram that guides users through the program generation process.

Victory 2.0 software runs on VAX and PC platforms and generates tests for Teradyne's L-series testers and the Z-series of in-circuit testers. The software is priced at \$5,000.

—Mike Donlin

### Victory 2.0 at a glance

- Features software modules that test nonboundary-scan circuitry that lacks bed-of-nails access, as well as internal circuitry of boundary-scan devices.
- Accepts industry-standard BSDL data about a circuit's boundary-scan implementation.
- Generates go/no-go patterns for boundary-scan test applications.
- Generates tests for Teradyne's L-series functional and combi-national testers and Z-series in-circuit testers.
- Adheres to IEEE 1149.1 standard for boundary-scan test.
- Available now on VAX and PC platforms for \$5,000.

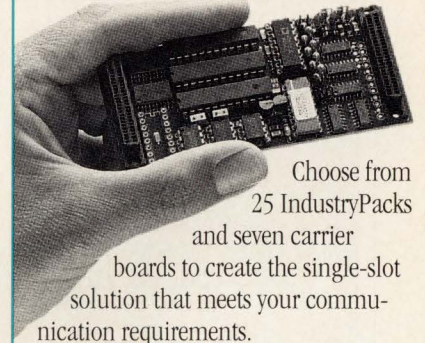
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THE CHOICE WITH A FUTURE



## Tool assesses manufacturing concerns during PCB design

Mentor Graphics' Manufacturing Advisor/PCB from gives designers the ability to consider downstream effects of early design decisions on manufacturing resources. One of a series of Mentor software releases supporting concurrent engineering environments, the tool provides de-

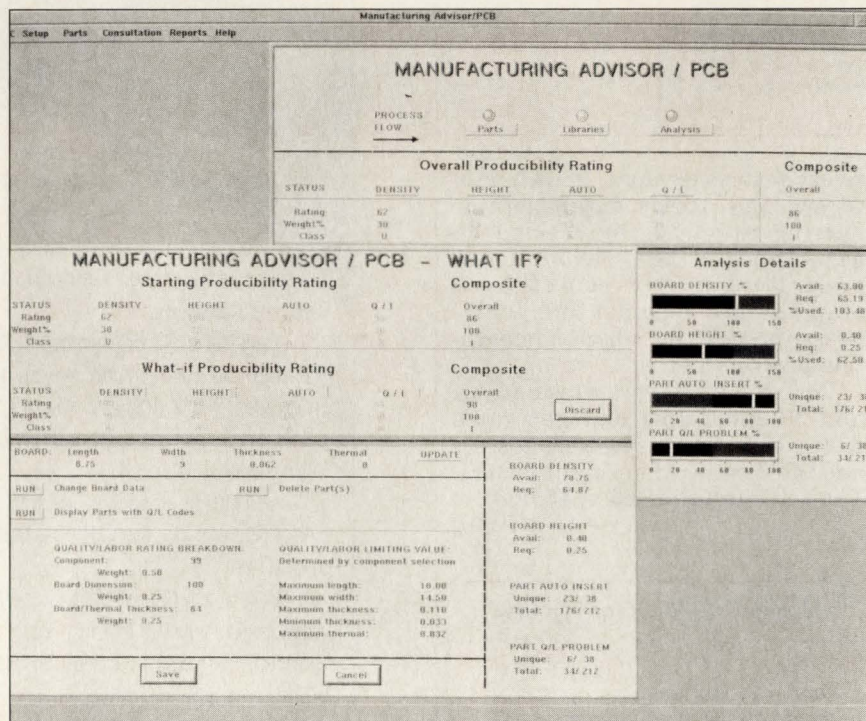
parts-based assembly analysis is applied throughout the circuit-design process. Prior to beginning schematic capture, design engineers can enter a parts list and perform a preliminary analysis. As components are added to a design, the tool monitors the consumption of the availa-

formed to raise the part for soldering, cleaning or inspection are flagged as special process problems. Parts that may tilt or float in flow solder or parts where solder in the lead bend may exceed standards are identified as possible manufacturing rework risks. The tool also flags parts that don't comply with military standards or specifications unique to a particular design.

Manufacturing Advisor/PCB is available with a component library containing manufacturability information on more than 800 component package styles. These packages represent tens of thousands of individual parts from a worldwide network of component manufacturers. The tool also supports a standard format for ASCII file input which can be used to input netlists created by an external parts list editor. This feature is provided for engineers who have a preference for their own text editor. Using this capability, an engineer could create a netlist at a different node and load it into Manufacturing Advisor/PCB for analysis.

The tool is priced at \$16,900 and is available now on HP/Apollo platforms. Sun and HP Series 700 compatibility is slated for Q1 '92. The optional parts library costs \$1,500.

—Mike Donlin



In this photo of Mentor Graphics' Manufacturing Advisor/PCB, the analysis sheet in the background shows initial manufacturing ratings in four areas. The text in the Density column indicates a critical problem with component density. The sheet in the foreground shows the user has interactively tested design alternatives and found a solution as seen in the "What-if Producibility Rating."

sign engineers with early identification of parts-related manufacturing problems in PCB assemblies. Designers can use the tool to perform "what-if" analyses to test the effects of recommended design alternatives.

Manufacturing Advisor/PCB was developed by Texas Instruments' Information Technology Group (Plano, TX) using Mentor Graphics' Decision Support System. TI developed the product as part of its internal design for manufacturing strategy and, through a joint agreement with Mentor, re-engineered the technology for the commercial marketplace.

Manufacturing Advisor/PCB's

ble placement area and, if exceeded, will identify those components that could be mounted in an alternative configuration with a smaller footprint.

In addition, Manufacturing Advisor/PCB assesses the auto-insertability of components selected for a design. As a design is refined through schematic capture and PCB layout, the tool continues to identify parts with unique labor requirements. These components may require special processing and are identified as potential manufacturing problems. Components with leads that can't be clinched, for instance, or can't be

### Manufacturing Advisor/PCB at a glance

- Lets designers consider the downstream effects of early design decisions on manufacturing resources.
- Identifies parts during schematic capture and layout with unusual labor requirements, special manufacturing processes, rework risks or that fail to comply with standards.
- Optional parts library contains information on more than 800 component package styles.
- Available now on HP/Apollo platforms for \$16,900. Sun and HP Series 700 release scheduled for Q1, 1992.

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ASICs & ASIC DESIGN TOOLS

10-ns PLAs for complex decode applications

Two new PLA devices from Signetics (Sunnyvale, CA) are designed for high-speed I/O and memory address decode functions in personal computers and workstations. The maximum propagation delay of each device is 10 ns, regardless of array loading or the number of outputs simultaneously switching. The PLUS153-10 and PLUS173-10 PLAs can be compared to 5-ns PAL devices, according to Signetics, because two PALs are often needed to achieve the functionality of a single Signetics PLA when implementing complex decode functions. "A single PLUS PLA can replace two 5-ns PAL devices in product-term-intensive decode applications," says Kathryn Douglas, product manager for PLDs at Signetics.

The PLUS153/173 are based on application-specific programmable architectures. The 20-pin PLUS153 has a programmable AND array and a programmable OR array. Signetics claims that 100 percent product term sharing is supported. Any of 32 logic product terms can be connected to any or all of 10 output OR gates. Where most PALs are limited to seven AND terms per OR function, the PLUS153 can accommodate a full 32 AND terms per OR gate for advanced memory mapping. The polarity of each output is programmable as either active high or active low, thus allowing AND-OR or AND-NOR logic implementation. The PLUS173 is a 24-pin version of the PLUS153, with four additional dedicated input pins.

The user-programmable OR array of the PLUS PLAs, when combined with the programmable AND

array, makes the parts suitable for complex decode and code conversion applications. Designers can reuse a single product term representing a unique expression in several other hybrid decode expressions. And with 10 bidirectional I/Os, the PLUS153/173, even when used for real-time data manipulation (e.g., modifying eight bits of data), have two unused bidirectional pins for handshaking and/or parity functions.

The PLUS153-10 and PLUS173-10 are available now in plastic and ceramic DIPs as well as in PLCCs. In 100-piece quantities, the 153 is priced at \$7.75 in a plastic DIP and at \$8.25 in a PLCC. Also in 100s, the 173 is \$11.70 in a plastic DIP and \$12.45 in a PLCC. —Barbara Tuck

PLUS153/173 at a glance

- PLAs with complex decoding functions
- 10-ns (max.) propagation delays
- Can accommodate 32 AND terms per OR gate
- Suitable for advanced memory mapping
- 10 I/Os with feedback
- 10 additional control terms for I/O direction control

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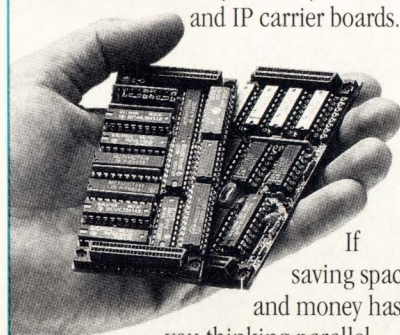
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## NEW PRODUCT HIGHLIGHTS

## ASICs &amp; ASIC DESIGN TOOLS

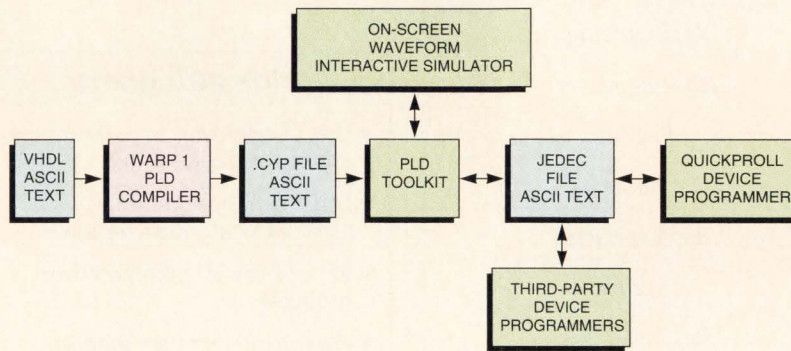
## VHDL PLD compiler for state-machines

The Cypress Semiconductor Warp 1 PLD Compiler uses a subset of VHDL to describe state-machine PLD designs. Specifically, Warp 1 provides high-level language design synthesis support for the Cypress 125-MHz CY7C361, claimed to be the industry's fastest state-machine PLD.

to implement the design.

After Warp 1 compiles VHDL, performs state and logic minimization, and 'routes' a design, it produces a ".CYP" output file that can be assembled with the Cypress PLD Toolkit. The Toolkit has an on-screen waveform-oriented simulator

## Chain of tools in a fully functional programmed device



The Warp 1 Compiler accepts a user-written VHDL design description and produces a .CYP output file that can be assembled with the Cypress PLD Toolkit.

With Warp 1, designers can work with the "hot-coded architecture" of the Cypress CY7C361, which uses a state macrocell to uniquely identify each possible state in a given design (hot-coding). Warp 1 reduces the number of states required to synthesize a design and then performs conventional logic reduction. Altera claims it's the only software that optimizes at both the state and logic levels.

Though Warp 1 supports only the CY7C361, the compiler is the first phase of a product family that will support Altera's line of CY7C33x and 36x devices. The CY7C361 can implement ordinary sequential state machines, concurrent state machines and parallel, hot-coded state machines.

The Warp 1 accepts a user-written VHDL description of a design. Once the design is created, it performs a two-pass optimization. First, it maps the state machines of the design to a concurrent form, adding states where necessary to remove deadlock conditions and to enable design fitting. Then the compiler reduces and factors the logic required

and JEDEC mapping capabilities that produce programming files used with Cypress' Quickpro II and other PLD programmers.

Warp 1, bundled with the PLD Toolkit, is available now for \$195.

—Barbara Tuck

## Warp 1 at a glance

- High-level PLD development language
- Uses subset of VHDL
- Supports 125-MHz CY7C361 state-machine PLD
- Performs state and logic minimization
- Supports sequential, concurrent and parallel, hot-coded state machines

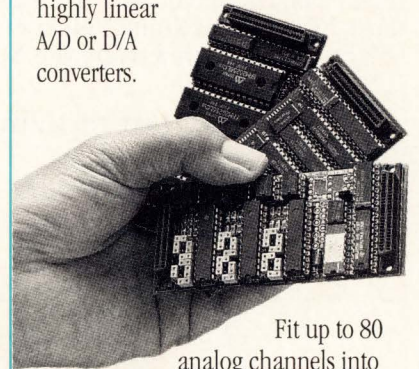
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## Blox eliminates gate-level design for FPGAs

A synthesis tool from Xilinx called Blox (Blocks of Logic Optimized for Xilinx) eliminates gate-level design entry for FPGAs. With Blox, the FPGA user can describe a design at the block diagram level with generic modules that can be parameterized. After the design is described at a high level, it's converted into a standard, hierarchical Xilinx Netlist File (XNF) and processed using the Xil-

specific needs of each module. The implementation of a comparator, for instance, will depend on the size of the data feeding the comparator and whether the equal to, greater-than or less-than outputs (or a combination) are used. Functions without a support module can be implemented using gate-level primitives or other macro library functions.

A Blox user need only specify the

contain logic block partitioning and relative placement and routing information. After the expanded modules are merged together, the entire design is written as an expanded, generated netlist.

Blox for the XC4000 family, which runs on the XACT 4000 development system, will be available in January. Versions for the XC2000 and the XC3000 families are scheduled for the second half of next year. Blox is priced at \$2,995 for a PC version and \$4,995 for workstations.

—Barbara Tuck

### List of Xilinx Blox Modules

Adder/Subtractors	Accumulators
Data Registers	Shift Registers
SRAMs	PROMs
Comparators	Inputs
Outputs	Bus Interfaces
Bidirectional I/Os	Counters
Multiplexers	Bus Inversions
Force a value onto a bus	Bus-Wide Boolean Functions
Three-State Buffers	

The Xilinx Blox system currently offers 30 different parameterized module generators that, according to Xilinx, provide a designer with literally thousands of possible logic functions.

inx Blox software. Through built-in expert knowledge, Blox architecturally optimizes the design to take advantage of special features of the Xilinx XC4000 FPGAs.

Lee Farrell, vice-president of marketing at Xilinx, says FPGA users need tools that provide efficient logic solutions without burdening the designer with a lot of architecture-specific details. "With Blox, it's like getting a Xilinx expert with every software system", says Farrell.

To design with Blox, the user calls up generic function modules from a library while in a schematic editor. The parameterized modules can provide thousands of logic implementations for various popular logic functions, according to Xilinx. Attached to each module symbol is a parameter sheet where the designer enters the specifications for that particular application. The module generator within Blox custom tailors the logic implementation to the

width and type of a bus once anywhere along the data path. The widths and types of data carried on the data path are automatically propagated throughout the design and all hierarchical levels. The size of an entire design can be modified, claims Xilinx, by changing just a few fields on the schematic.

Blox uses the system features of the Xilinx XC4000 architecture including fast carry logic, clock buffers and on-board RAM and ROM. Expert knowledge of the logic cell array architecture is built into Blox through rules-based algorithms implemented in an artificial intelligence language by Quintus.

Initially, Blox provides 30 different parameterized modules for popular editors including FutureNet Dash, Mentor, OrCAD, and ViewDraw. Where most modules are expanded into a netlist description of a function, arithmetic functions are expanded into hard macros which

### Blox at a glance

- Use of a familiar schematic editor for design entry
- Large graphical modules eliminate gate-level design
- Set of over 30 parameterized modules
- Parameter sheet for entering specifications
- Design can be modified by changing one parameter
- Automatic use of XC4000 system-level features
- Built-in expert knowledge via Quintus' AI language

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# CALL FOR PAPERS

# RISC '92

**The first international conference  
on the design of RISC-based systems**

**Le Baron Hotel/San Jose Convention Center  
San Jose, California, USA  
February 18-20, 1992**

To be held in conjunction with SysComp/92-West, **RISC '92** will be the premier gathering of designers and design managers involved with Reduced Instruction Set Computer (**RISC**) architectures, systems, programming and applications. The heart of the conference is a Technical Program that will give both hardware and software designers a deeper understanding of the concepts underlying **RISC**, its advantages and disadvantages, and its future directions. More than that, **RISC '92** will provide practical, hands-on, application-oriented information needed to design **RISC** into general-purpose computing, embedded and real-time applications.

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Sponsored by *Computer Design*/PennWell Publishing  
in conjunction with SysComp, the OEM Systems/Subsystems Components Conference & Exposition



# A profile of **RISC '92** attendees

**RISC '92**, the first international conference on the design of **RISC**-based systems, will be a must for every hardware or software engineer designing products or systems based on either **RISC** or **CISC** microprocessors. Attendees will have design and development responsibilities that run the gamut from evaluating and specifying **RISC** microprocessors, memory and peripheral ICs, to **RISC**-based CPU boards, bus architectures and high-speed interfaces, to operating systems, real-time kernels, compilers, debuggers, emulators, development systems and applications software.

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## Specifically, **RISC '92** is targeted at engineers and engineering managers who are:

- **Designing RISC-based computers** — RISC is still in its infancy and building the highest-performance, most cost-effective workstations, file servers, array processors, and personal computers demands a clear understanding of the various RISC architectures, memory subsystems, I/O strategies, etc.
  - **Designing embedded and real-time RISC systems** — At present, most embedded applications and real-time designs are CISC based. But the plummeting cost of RISC processors has made RISC a viable alternative in the next generation of laser printers, fax machines, photocopiers, phototypesetting equipment, engine controls, antilock braking systems, etc.
  - **Programming RISC-based systems** — RISC CPUs present the software engineer with a different set of programming opportunities and constraints than their CISC counterparts, making it essential to identify the best operating systems (especially critical in real-time applications) and programming methodologies.
  - **Integrating RISC-based board-level solutions** — Using off-the-shelf RISC-based boards can save precious development time and provide an easy path to improving the performance of existing products, especially those built around standard, open bus architectures such as telecom and datacom equipment, multimedia systems, test equipment, navigation and military/avionics systems.
  - **Designing ASICs with RISC cores** — As RISC finds its way into more and more embedded and real-time applications, designers will begin looking to achieve greater product differentiation by embedding RISC in semicustom silicon.
  - **Specifying RISC development tools and integrating them into the overall hardware/software development effort** — Knowing what tools are available to support RISC processors, and how effective those tools are, is essential before embarking on a design.
-



# The focus of the **RISC '92** Technical Program

A combination of lectures, workshops, half-day tutorials and panel discussions will cover all the areas of critical importance to design engineers, programmers and engineering managers developing products around **RISC** processors and architectures. In addition to discussing the theoretical aspects and concepts essential to a complete understanding of **RISC** design and software development, the presentations are intended to give designers the practical information needed to evaluate, select and execute a **RISC**-based design. Whenever possible, the advantages and disadvantages of a particular approach, as well as the hardware and software trade-offs, will be emphasized.

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**You are invited to submit proposals for presentations in any of the following areas or to suggest other topics that may be of interest to attendees.**

Fundamentals of Sparc, MIPS R3000/4000, 88000, 29000, i860, i960, Transputer, PA, and R/6000 architectures.

RISC vs. CISC performance trade-offs and choosing a RISC processor.

RISC-based multiprocessing systems.

Incorporating RISC features into CISC architectures.

Optimizing the RISC processor/memory interface.

RISC processor interrupt handling.

Programming Sparc, MIPS R3000/4000, 88000, 29000, i860, i960, Transputer, PA, and R/6000 processors.

Writing superscalar and/or superpipelined code.

Software scheduling.

Using RISC register windows.

Building I/O subsystems around RISC.

Performance and trade-offs of cache memory architectures (on-chip and off-chip).

Maximizing DRAM and SRAM cache memory subsystem performance.

Electrical effects in RISC designs running at 50 MHz and above.

Multichip modules and other packaging issues associated with RISC processors.

Internal/external bus structures in RISC.

Timing issues in RISC designs.

Benchmarking RISC processors and RISC systems.

Estimating the computing needs of high-performance embedded applications.

Selecting RISC compilers to best match the RISC architecture.

Out-of-order instruction scheduling.

Software pipelining techniques.

Add-in buses for RISC workstations.

Advances in RISC-based CPU boards for standard buses.

Using RISC to accelerate graphics functions.

RISC in image-processing applications.

RISC as LAN/WAN communications processors.

RISC in multimedia applications.

RISC in laser printers and other peripherals.

Using RISC processors with DSP.

Designing RISC processors into array processing applications.

Emulation of RISC processors.

Debugging and development tools for RISC.

Real-time operating systems and kernels for RISC.

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# Guidelines for participating in **RISC '92**

If you or your organization wish to participate in the **RISC '92** Technical Program, submit a brief proposal to the Technical Program Coordinator no later than **November 8, 1991**.

Proposals should be 1- to 1 1/2-pages in length and contain a one-paragraph abstract that summarizes the content and goals of the presentation and a brief outline of the major topics that would be covered in the presentation. Presenters must be technically qualified and able to answer questions from attendees. A short biography of the presenter, describing his or her technical background and accomplishments must accompany the proposal.

Acceptance of proposed presentations will be made by **November 15, 1991** and a complete copy of the presentation, including all visuals and graphics, will be required no later than **December 31, 1991**.

Presenters will be given free admission to the Technical Program and to the exhibits associated with **RISC '92** and SysComp/92-West.

Presentations given at **RISC '92** will be published in a Proceedings and copyrights shall be assigned to *Computer Design*.

For more information or to submit a proposal contact:

**Andrew Wilson**  
Technical Program Coordinator  
*COMPUTER DESIGN*  
313 Allston Street  
Brookline, MA 02146  
TEL: (617) 734-9903  
FAX: (508) 692-7780

or

**John Miklosz**  
Editor-in-Chief/Associate Publisher  
*COMPUTER DESIGN*  
1 Technology Park Drive  
P.O. Box 990  
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*Computer Design* is read every month by more than 100,000 engineers and engineering managers designing electronic products that incorporate microprocessors, board-level and OEM computers for use in computers and computer peripherals, telecommunications, test and measurement equipment, data acquisition, control and automation, and imaging, diagnostics and analysis equipment.

In addition to the Technical Program, **RISC '92** will feature exhibits by vendors of **RISC** microprocessors, SRAMs and DRAMs, high-performance peripheral and interface ICs, fast PLDs and FPGAs, real-time operating systems and kernels, compilers, emulators and other microprocessor development tools, and application software suitable for use on **RISC**-based systems. The vendor exhibition will be held in conjunction with SysComp/92-West at the San Jose Convention Center. For information about exhibiting at the conference, contact:

**Paul LaGris**  
Exhibit Sales  
3432 Timberlake  
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*Computer Design* magazine will be publishing the **RISC '92 Conference Guide**. In addition to distribution at the conference, the Guide will be mailed with the February, 1992 issue of *Computer Design*. For information about advertising in the Guide, contact:

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# The Official **SysCOMP/92 WEST** Show Guide

**COMPUTER DESIGN and SYSCOMP Team up to provide you with a complete Show Guide package before and during the show.**

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- Value-added Editorial:** This winter's official SysComp Show Guide, mailed with the February issue of **COMPUTER DESIGN** and distributed to all show attendees, will feature the usual show information — technical session descriptions and schedule, exhibitor listing, dining and events in the San Jose CA area — but will be enhanced by editorial features of special interest to **COMPUTER DESIGN** readers, SysComp attendees and exhibitors:
- Distribution:** The guide will be polybagged along with the Western portion of **COMPUTER DESIGN**'s February issue for a total distribution of 50,000+. In addition, a special mailing will go to all of the pre-registrants...and it will be distributed to each attendee at the show.
- Issue Date:** February 1, 1992
- Pricing:** \$2,200 Per Page — including color.
- Savings Opportunity:** Advertise in the February Show issue of **COMPUTER DESIGN** and save \$500 per Show Guide page.
- Closing:** January 10, 1992



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## Real-time Unix debugger features GUI and kernel access

A new debugger for 80386 Unix- and Posix-based systems features a fully graphical user interface (GUI) with pull-down menus, icons, command buttons, and multiple, resizeable windows, as well as features oriented toward debugging multiprocessor systems. The Lynx Debugging Toolkit (LDB) from Lynx Real-Time Systems (Los Gatos, CA) includes support for debugging multiple threads, multiple processes and remote debugging of a target system over a network. In addition, the user can open a separate window and examine the real-time kernel in the same session the application is being debugged.

The GUI has four resizeable windows: one shows the status of the current process; another displays source code or interleaved source and assembly code; a text window for entering commands and displaying output messages from the debugger; and one where watch and

trace points are displayed.

Setting breakpoints is as easy as highlighting a line of code and clicking a button. But breakpoints can also be conditional. They can be set to trigger macro commands so when execution halts at a breakpoint, for example, a macro can take the user to some other place in the code. Or, the user can set a breakpoint to trigger a macro to look at another process outside the current linear stream of execution. For multiple Posix threads, as well as for multiple processes, the user can also set breakpoints in multiple concurrent points of execution. This is important in a multiprocessor real-time system because a run-time bug that doesn't exist during the execution of a single thread or process may show up during the concurrent execution of multiple threads or processes.

The LDB source-level debugger can be set up to handle signals— asynchronous events, such as inter-


rupts or message alerts—that can occur and the program must handle in a predictable way. LDB can pass a signal to the process being debugged, print a message when the signal is received or block the signal, as the user wishes. Using watch and trace points, the user can set the debugger to watch for some variable to change to some user-defined truth value. At that point, it can halt execution whenever a condition variable changes, or trigger some macro. Trace points can be set to simply monitor the changes to a selected set of variables. The user can log trace and watch points to a file and examine their history later.

Since real-time applications carry on a good deal of interaction with external devices at the kernel level, there's a need to debug kernel-level operations. The kernel debugger can be started as a separate operation and run kernel and application debuggers in different windows at the

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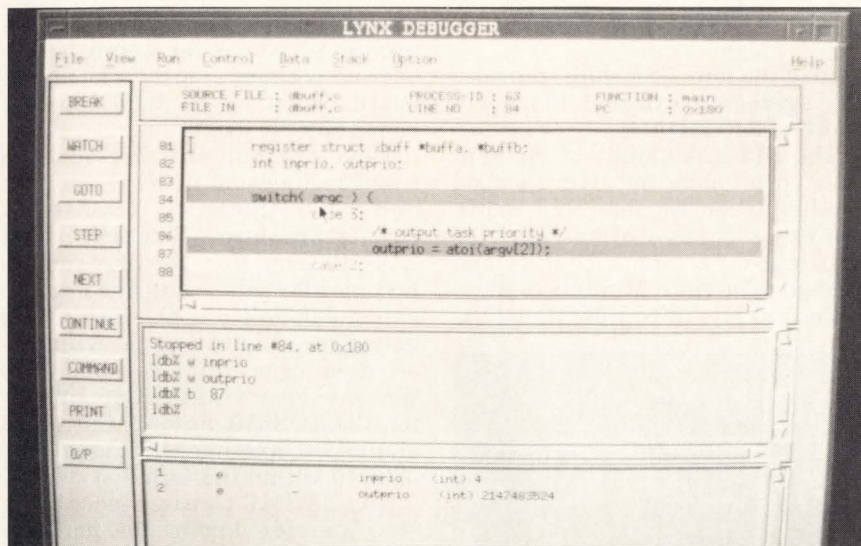
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CIRCLE NO. 79





The LDB debugger's GUI shows four windows: status, source, command and data display. Along the left side are commonly used command buttons, the top has pull-down menus for more commands that can be executed with a simple mouse click. Debugger output such as watch and trace points can be logged to disk for later review.

same time. Kernel-level debugging, of course, doesn't show source listings. But the user can examine system stacks and frames, set watch and trace points in device drivers and examine memory and registers.

LDB's remote debugging feature lets the source debugger run in a host machine with only a small re-

mote debugging server in the target. Host and target are then connected over a TCP/IP network. Remote debugging is also useful in multiprocessor systems where one processor can be dedicated as a "host" or the processor to communicate with the remote host and the user can move around tasks on processors as easily

as among threads.

Lynx Real-Time Systems currently offers its standard, text-based debugger (called GDB) as a bundled part of its Lynx/OS real-time operating system. LDB will be available as a shrink-wrapped product for \$895.

— Tom Williams

### Lynx Debugging Toolkit at a glance

- OSF/Motif X-Window GUI
- Source and assembly language debugging
- Access to kernel code and data debugging
- Debugging multiple threads and concurrent processes
- Ability to build command sequences with macros
- Unlimited conditional break-points
- Watch points and trace points

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† A 16 microsecond preemptive context switch on a 33 MHz 486 (100 microseconds on a 16 MHz 286).  
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## Coprocessor VMEbus board hits 1.1 Bops

A new leader in VMEbus coprocessor boards boasts an unprecedented peak performance of 1.1 billion operations/s (Bops), 200 MFlops and an I/O bandwidth topping 240 Mbytes/s. The VMEbus board from Ariel (Highland Park, NJ) takes advantage of four Texas Instruments' (Houston, TX) TMS320C40 digital signal processor chips to double the processing performance and quadruple the I/O performance of its nearest competitor.

Called Hydra, after the many-headed serpent of Greek mythology, the four-processor board is targeted at many compute-intensive multiprocessor applications ranging from speech and pattern recognition to simulation and visualization. Each of the four 320C40 chips is capable of 50 MFlops, 275 Mops and contain dual 32-bit memory buses. Each bus is capable of 100-Mbyte/s transfer rates. In addition, each processor has six parallel communication ports, each capable of 20-Mbyte/s transfers for a combined transfer capability of 1.3 billion bytes/s.

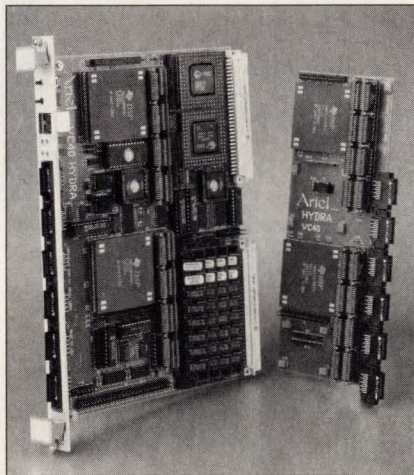
Up to 64 Mbytes of DRAM can be shared between DSP1 (one of the four DSP chips) and the VMEbus interface. In addition, the four DSP chips share up to 5 Mbytes of zero-wait-state SRAM, organized in eight banks. Four of the eight banks serve as local memory, the other four, global memory. Each DSP chip has direct access to one local bank and one global bank via its two independent 32-bit, 100-Mbyte/s memory buses.

To handle the high-speed I/O, each 320C40 chip has six byte-wide, FIFO-buffered, 20 Mbyte/s, bidirectional, parallel I/O ports. Each DSP also includes a high-speed DMA controller. This controller features six independently programmable DMA channels and can be programmed to transfer data simultaneously via all six ports without interrupting program execution.

Three of each DSP chip's six parallel I/O ports are used to link it with the other three chips on the board. The other three ports are pinned out and available as external communications ports. The combination of the 12 external ports (three for

each of the four DSP chips) provides the aggregate external I/O bandwidth of 240 Mbyte/s.

The added flexibility of the multiple ports make the Hydra a good candidate for sophisticated multiprocessor configurations such as hypercubes, 2- and 3-D grids and hexagonal arrays. Multiple configurations of Hydra boards can be im-



*Ariel's Hydra 6U VMEbus coprocessor board features four TMS320C40 DSP chips to achieve an unprecedented 1100 Mops.*

plemented by interconnecting the processor ports with external cabling, while the VMEbus handles the interprocessor communications.

In addition to its 12 byte-wide communication ports, the Hydra includes Ariel's own 24-bit parallel ADbus. The ADbus may be used to access any of Ariel's family of data acquisition cards which can provide samples up to 12 bits at rates as high as 10 million samples/s. Also, up to six 3U analog modules may be connected in series to each Hydra board, and pairs of analog modules may be ganged in a single 6U slot. Conventional serial I/O is handled via two RS-232C serial ports.

The Hydra incorporates a full VMEbus interface and can serve as either a bus master or slave with full slot-one capability. The board supports 8-, 16- and 32-bit bus transfers and supports block transfers up to 35 Mbytes/s. An optional VME subsystem bus (VSB) interface is available for systems using the

subsystem bus. For stand-alone applications, where the board has to operate without a host CPU, an on-board bootstrap EPROM lets the board boot by itself.

Development support for the board includes an ANSI C compiler and the TMS320C40 XDS510 in-circuit emulator. The PC-based XDS510 emulator, the first to support parallel processing, includes an assembler, linker and C source-level debugger. Featuring a window-oriented user interface similar to that provided with the C40 simulator, the XDS510 provides full-speed emulation and monitoring of the 320C40 within the target system.

The XDS510 features global run, stop and breakpoint for multiple DSPs; register and memory loading; inspection and modification; and single-step execution. It also features software breakpoint, trace and timing with up to 30 software breakpoints, and hardware breakpoint and trace on all programs and data addresses. A five-wire Joint Test Action Group interface provides a JTAG scan path to every location within each DSP chip's memory and registers. Spectron Microelectronics (Santa Barbara, CA) is currently creating a version of Spox, its real-time DSP operating system, to support multiple C40 systems.

Ariel's Hydra will be available in December for \$9,995, single-unit price.

— Warren Andrews

### V-C40 Hydra at a glance

- 4, 50-MHz TMS320C40 processors
- 1100 Mops, 200 MFlops
- Up to 64-Mbyte DRAM
- Up to 5-Mbytes zero-wait-state SRAM
- Master/slave VMEbus interface with slot-one controller 6U board
- 24-bit ADbus parallel interface for up to six daisy-chained analog I/O modules
- JTAG-compatible emulation port

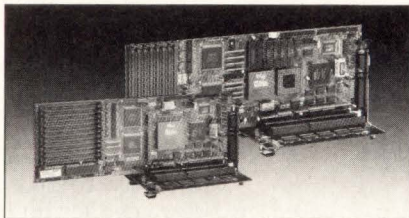
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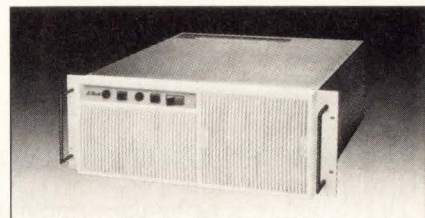
Built around a 25-33MHz 80386DX, the versatile I386 features 32K cache (I386/25), or 128K cache (I386/33), with up to 32MB of 70ns SIMM DRAM, plus either an 80387DX Coprocessor or a Weitek 3176 Numeric Data Processor. The I486 offers superior processing power for any system configuration using either the 80486DX (25 or 33 MHz) or 80486SX (25MHz) CPU, with optional 256K cache. Both incorporate an IDE hard disk interface, a floppy disk controller, two serial and one parallel port, and a programmable Watchdog timer. **Contact I-Bus, 9596 Chesapeake Drive, San Diego, CA 92127. Tel. (800) 382-4229, Fax (619) 268-7863.**



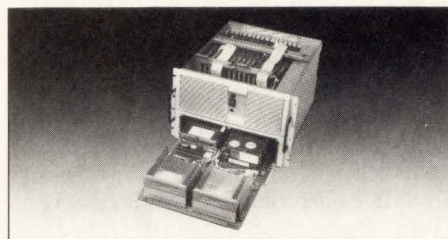
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**Model 4820 — maximum slots, maximum disks**

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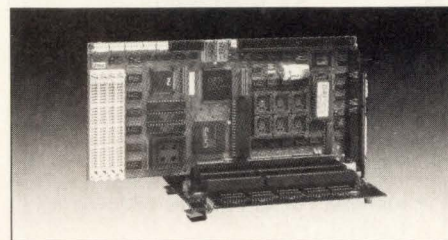
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**Customer input guides Model 161 Enclosure design**

Design and development of the revolutionary new 161 PC Bus System from I-Bus has been totally governed by customer input – as the 161's unparalleled array of features demonstrates. The 161 offers 16 full-length AT slots, with an adjustable mechanical hold-down bar. 275W or 375W power supplies are optional. Or, if the backplane is segmented (8X8), two separate 150W power supplies are provided, one dedicated to each segment. Power supplies are easily replaced on their own service module. Up to eight half-height drives or four full-height drives (or any combination) are located in a shock-mounted drive bay, accessed from the front via a slide-out drive drawer for easy drive addition or replacement. Rack mount, tower and desktop configurations are available. **Contact I-Bus, 9596 Chesapeake Drive, San Diego, CA 92127. Tel. (800) 382-4229, Fax (619) 268-7863.**

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**CIRCLE NO. 104**



## Chip set targets tape drive designers

Developed in a technology partnership with 3M, International Microelectronic Products (San Jose, CA) claims it has built the first chip set to integrate the read/write and servo channels for magneto-resistive (MR) tape drive subsystems. It will let designers produce 6-Gbyte 1/4-tape drives based on QIC standard specifications. The chip set's flexibility lets designers produce tape drives that are backward compatible with existing QIC-based tape drives.

What's more, tape drives based on the chip set can read various tape speeds because of a patented phase-locked loop (PLL) function that maintains constant gain, regardless of the bit stream.

The four-chip set includes a quad magneto-resistive preamp (IMP52C414), a quad write driver (IMP52C434), a read channel signal processor (IMP52C464), and a servo analog front-end (IMP52C484). The 52C414 preamplifier features four

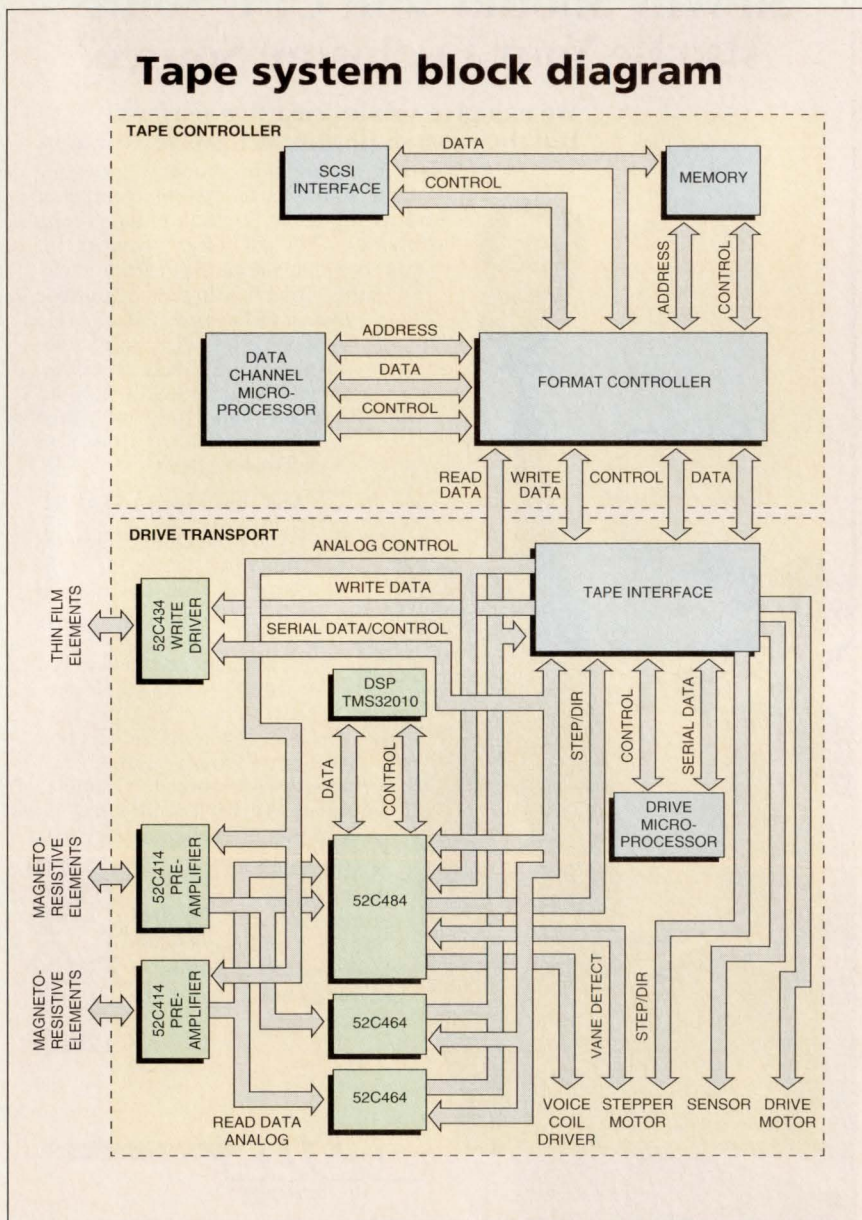
independent amplifiers connected directly to the head, eliminating the need for multiplexing. This also allows multiple tracks to be read simultaneously: two data tracks, the servo track and a special track for QIC-1350 compatibility. The 52C434 quad write driver includes four write outputs for direct connection to the write elements and permits simultaneous writing on up to four tracks. Drive manufacturers can vary the output current to the head, minimizing intersymbol interference and maximizing dynamic range.

The 52C464 incorporates a programmable linear phase low-pass filter. The filter may be programmed to optimize its response for different media and different standards. The read channel provides all the functions needed for equalization, gain control, filtering, pulse detection, and clock and data recovery from one of eight input sources. The 52C484 servo analog front-end features dual channel demodulators to allow averaging of the servo signal and compensation for rotation of head assembly, resulting in accurate positioning of the head.

The integrated read/write and servo channel chip set is expected to be available in Q1 of '92. Single set pricing is \$300. OEM quantity pricing is expected to be \$35 to \$65, depending on drive configurations.

—Dave Wilson

### Tape system block diagram



Four ICs from International Microelectronic Products form the heart of this tape drive transport mechanism.

### Tape drive chip set at a glance

- Developed in conjunction with 3M
- First chip set for magneto-resistive drives
- Increases data storage capacity to 6 Gbytes
- Backward compatibility with QIC standards
- Reads various tape speeds

#### International Microelectronic Products

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Circle 352



## Multiprocessing pixel processor offers smooth scaling

Multimedia ICs must not only acquire, convert and process video information from a number of different sources, they should also be able to interactively resize the video on the CRT screen. Now, Pixel Semiconductor (Plano, TX), a subsidiary of Cirrus Logic (Fremont, CA), has debuted a solution to part of the multimedia problem. In fact, the company claims that its Px0070 Video Window Generator (VWG) chip is the first single-chip video processor to provide smooth scaling of

screen. Scaling in the horizontal direction is based on true linear interpolation. The output from the linear resampling unit is then fed to a variable-pixel processor that, as its name implies, lets the designer vary the number of bits associated with each pixel stored in memory. For the highest-quality photorealistic systems, a full 24-bit frame buffer is typically used. For cost-sensitive systems, the output data depth is programmable to a minimum of 8 bits/pixel. "For designers who want

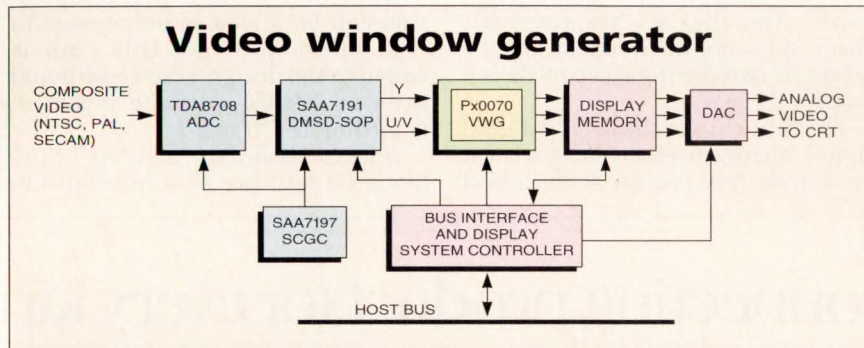
buffer. The data can be read onto the pixel output pins from the FIFO. An external memory controller transfers pixels from the FIFO to the display buffer memory using addresses calculated by an external pixel address calculator.

The Px0070 provides output-control signals that simplify these pixel output operations. The programmable control unit has two primary functions. First, it provides a programming interface to the VWG over its control bus interface. This is a byte-wide bus that controls the timing of reads and writes to the VWG like an SRAM. Second, it sports a set of control registers that coordinate the operation of the format and color converter, the linear resampling unit and the FIFO, controlling the color conversion, I/O, scaling, and windowing of the incoming video stream.

The accompanying diagram illustrates a true-color video/graphics scaling system using a single Px0070 VWG. The device interfaces with the Philips/Signetics digital TV decoder chip set (see "New multimedia chip sets aimed at niche applications," *Computer Design*, Sept. p 38). The chip set converts composite video into YCrCb data. The display system controller transfers the scaled image data from the VWG to the multiport display memory. Finally, the D-A converter converts the 24-bit digital pixels to analog RGB video.

The CL-Px0070 video window generator is packaged in an 80-pin PQFP. Samples are now available at \$55 in 1,000 quantities. Volume production is planned for Q4 '91.

—Dave Wilson



Capable of providing smooth scaling of real-time video for desktop windows environments, Pixel Semiconductor's Px0070 is shown here interfaced to a Philips/Signetics digital TV decoder chip set.

full motion, real-time video for desktop windows environments. To do so, the chip integrates five major functional blocks: a format and color converter, a linear resampling unit, a variable-pixel processor, a 16 pixel-deep output FIFO, and a programmable control unit.

The Px0070's real-time format and color converter lets a system receive broadcast video by converting various input formats (ranging from 16-bit gamma-coded YCrCb to 24-bit linear RGB) into 24-bit RGB color space at data rates found in most computer systems.

The linear resampling unit is a 2x1 decimation filter that scales and clips the video window. It performs independent X and Y real-time scaling of the RGB video data with single-pixel resolution. Video window sizes can be varied in single-pixel increments in both the X and Y dimensions. Real-time video ranges from full screen to any window size, and can be placed anywhere in the

to cut their system memory bandwidth by one-third to two-thirds, this is a great solution. They can use an inexpensive 8-bit frame buffer to store video in. Although you can tell the difference between 8- and 24-bit resolution, it still looks very good," says Jim Fontaine, president of Pixel Semiconductor. The processor uses a proprietary error diffusion algorithm that has been implemented in hardware by the company.

Large amounts of data are associated with real-time video. Bandwidth requirements are also very high, and continuous access to the display subsystem frame buffer isn't always available. As a result, users require some type of intermediate data storage between the scaling device and the frame buffer memory. This is achieved by an on-chip FIFO. After the data has passed through the variable-pixel processor, the resulting data is temporarily stored in the FIFO which elastically connects the resampling unit to the display

### Px0070 at a glance

- Smooth scaling of full-motion video
- Format and color converter
- Variable-pixel processor
- 16-pixel-deep output FIFO

### Pixel Semiconductor

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Circle 351



INTEGRATED CIRCUITS

Modem chip set combines data/fax/voice

As designers of notebook computers and stand-alone modems scramble for ways to pack more capabilities into their products, the timing couldn't be better for a set of silicon combining the electronics of the fax machine, the data modem, and the voice answering machine. The CLMD1424EC, a chip set designed jointly by Cirrus Logic and Crystal Semiconductor (recently acquired by Cirrus), does just that. With only two devices, the set implements a complete modem capable of transmitting and receiving both data and fax. It also adds a voice capability, enabling the modem to act as an answering machine.

According to Cirrus, designers can build a complete modem without adding an external microprocessor or UART (universal asynchronous receiver/transmitter). No additional firmware is required either, the com-

pany claims. This level of integration means the complete modem can be squeezed into a 3½ × 2-in. form factor—about the size of a business card. The chip set is intended for both stand-alone and integral data/fax modem applications. As a data modem, the chip set operates at speeds up to 2,400 bits/s and up to 14,400 bits/s as a fax modem.

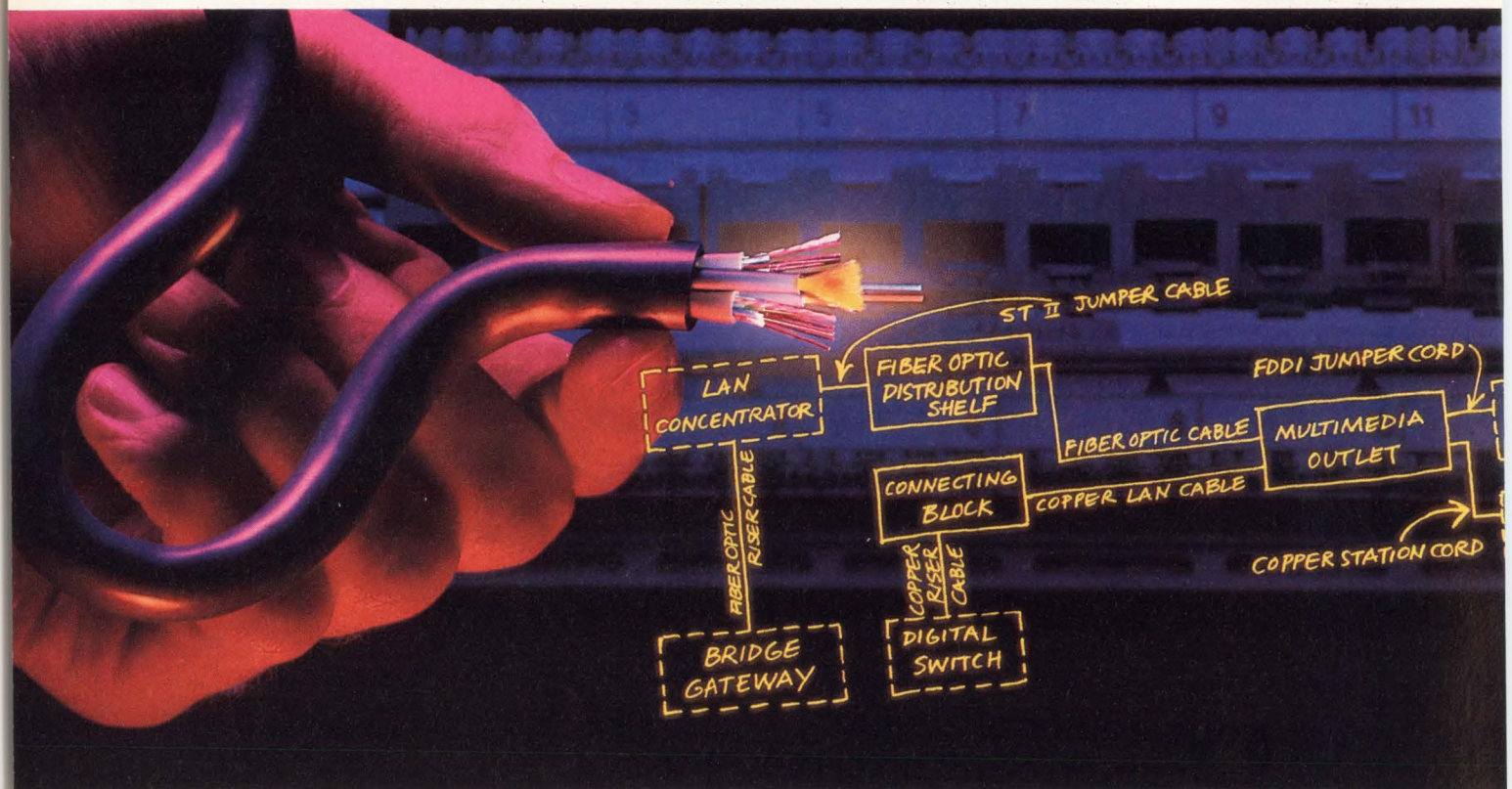
Because today's modem designs tend to be under strict power budgets, the chip set offers low operating power and provides some power-management features. Operating from a single 5-V supply, the chip set typically draws only 250 mW of power. The chip set has automatic sleep and wake-up functions and the power drawn during sleep mode is a meager 11 mW.

The first chip in the set is a digital signal microprocessor. Where most modem designs require some kind of

separate 8-bit microcontroller, this chip handles the modem's processing functions without the need for any external processor support. The second chip performs the analog front end (AFE) modem functions. Based on a proprietary sigma-delta scheme, the AFE chip provides higher conversion accuracy than traditional AFEs. Unlike switched capacitor-based AFEs, this chip offers improved performance at low receive signal levels while making the device less sensitive to board layout restrictions due to noise. An optional third protocol chip may be added to the set to provide V.42/MNP Class 4 error correction; V.42bis/MNP Class 5 data compression can be added to enhance data transmission. When this chip is added to the design, some additional external SRAM must be included, according to Cirrus.

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## INTEGRATED CIRCUITS

the chip set so designers can develop a Hayes-compatible modem with a minimum of effort. The command set includes various subsets for implementing the data, fax and voice functions. The fax command set lets any data terminal with communication software that supports EIA-578 Class 1 communicate with the Group 3 Fax machine. A voice mode command set is also provided which lets a host computer and a CL-MD1424-based modem emulate a telephone answering machine.

Protocols supported by the chip set include CCITT V.17, V.29, V.27ter and V.21 Channel 2. These allow speeds from 300 to 14,400 bits/s.

Samples of the CD-MD1424 chip set will be available mid-November. The price is \$45 (1,000s).

—Jeffrey Child

### CL-MD1424 chip set at a glance

- Complete, two-chip modem
- 2,400-bits/s data modem capability
- 14,400-bits/s fax modem capability
- Voice capability lets modem be an answering machine
- 250-mW power operation/11 mW in sleep mode
- Adding a third chip provides V.42/MNP Class 4 error correction and V.42bis/MNP Class 5 data compression

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## INTEGRATED CIRCUITS

## Memory, modem PC cards meet new U.S., Japanese standards

With the long-awaited advent of a memory card standard, Intel (Santa Clara, CA) has announced the first products in a family of plug-in IC cards for laptop, notebook and palm-top computers. The credit-card-size IC cards are also expected to find use in portable instrumentation, communication and industrial equipment. The initial offerings are a 2-Mbyte flash memory card and two modem cards, along with an interface controller IC for interfacing to ISA computer systems. The products support the recently finalized Personal Computer Memory Card International Association (PCMCIA) 2.0 specification, which is in step with the Japanese Electrical Industry Development Association (JEIDA) 4.2 specification.

PCMCIA 2.0 specifies a 68-pin credit-card-size physical format. In addition, it specifies two card thicknesses (3.3 and 5.0 mm) to accommodate different IC technologies. Cards can be used in either 8- or 16-bit modes. The specification includes a parameter definition called card information structure (CIS) that requires the system to read on power-up or reset and an execute-in-place feature that lets it run on-card software. Cards can also have standard I/O capability.

Because of the I/O capability, a card can do more than just extend memory; it can contain peripheral devices. For this reason, Intel has unveiled both a memory device and modem products as an example of the diversity of card-based devices that will be possible for system designers. The flash memory card joins two other (1- and 4-Mbytes) flash cards in Intel's lineup. The IMC002FLKA boasts a read time of 200 ns and is based on Intel's ETOX

II flash memory technology. According to Intel, flash cards of this size can easily store an OS and several applications, as well as data, in a nonvolatile package. Intel has upgraded its previous flash cards to meet the 200-ns read time as well.

The modem card comes in two versions: one certified for the North American telephone system and one

compatible systems based on Intel processors using the 80386SL low-power CPU. The 82365SL implements Intel's exchangeable card architecture (ExCA). The interface controller chip supports a direct interface to the ISA (AT) bus for two PCMCIA-compatible sockets. In addition, for systems needing more than two slots, multiple 82365SLs can be cascaded for up to eight slots. Any systems implementing the ExCA interface to their internal architectures, therefore, will be able to use PCMCIA-compliant cards interchangeably.

The 82365SL contains automatic power-management circuitry and eliminates jumpers for configuration because it dynamically configures cards in the system on power-up or reset. Using the 82365SL, where 160 pins take up 2 in.<sup>2</sup>, a complete interface with a set of buffers can be implemented with only five ICs. The buffers allow cards to be inserted and removed with power on.

Production units of the flash memory card are now available. Samples of the Modem 2400+ are also available with production quantities available in Q4 '91. Pricing for the flash card in 1,000 units is \$375. Pricing for the North American Modem 2400+ is \$200 and for the Japanese version, \$230. The 1,000-unit price for the 82365SL is \$35.

— Tom Williams



Intel's initial offering of standards-based PC card products includes a flash memory card, two modems and an integrated interface controller to aid designers of PC-compatible portable computers, instruments and equipment.

for the Japanese. The Modem 2400+ is a 2400-baud modem housed in a 5-mm thick PC card. It contains a UART (universal asynchronous receiver/transmitter), a microcontroller, analog front-end, and other circuitry. The modem supports the Hayes AT command set and the Microcom MNP Class 4 error-correction and Class 5 data-compression protocols. It supports, therefore, all the major PC-based communications software.

Along with the PC card offerings, Intel has introduced an integrated circuit to help system designers quickly and easily incorporate PC card technology. The 82365SL is especially designed for portable PC-

### Intel's PC Cards at a glance

- Flash memory with 2 Mbytes and 200-ns read time
- Modem 2400+ with 2400 baud, North American and Japanese versions, Hayes compatible, MNP Class 4 and 5 protocols
- 82365SL with automatic power management, dynamic configuration (no jumpers), direct interface to ISA bus, and cascadeable for up to 8 card slots

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The MVC's advanced features benefit both the integrator and programmer. Port and VMEbus parameters are soft-configured and set line-by-line. Modem control is standard. Full software support is also included,

along with diagnostics and a Streams driver.

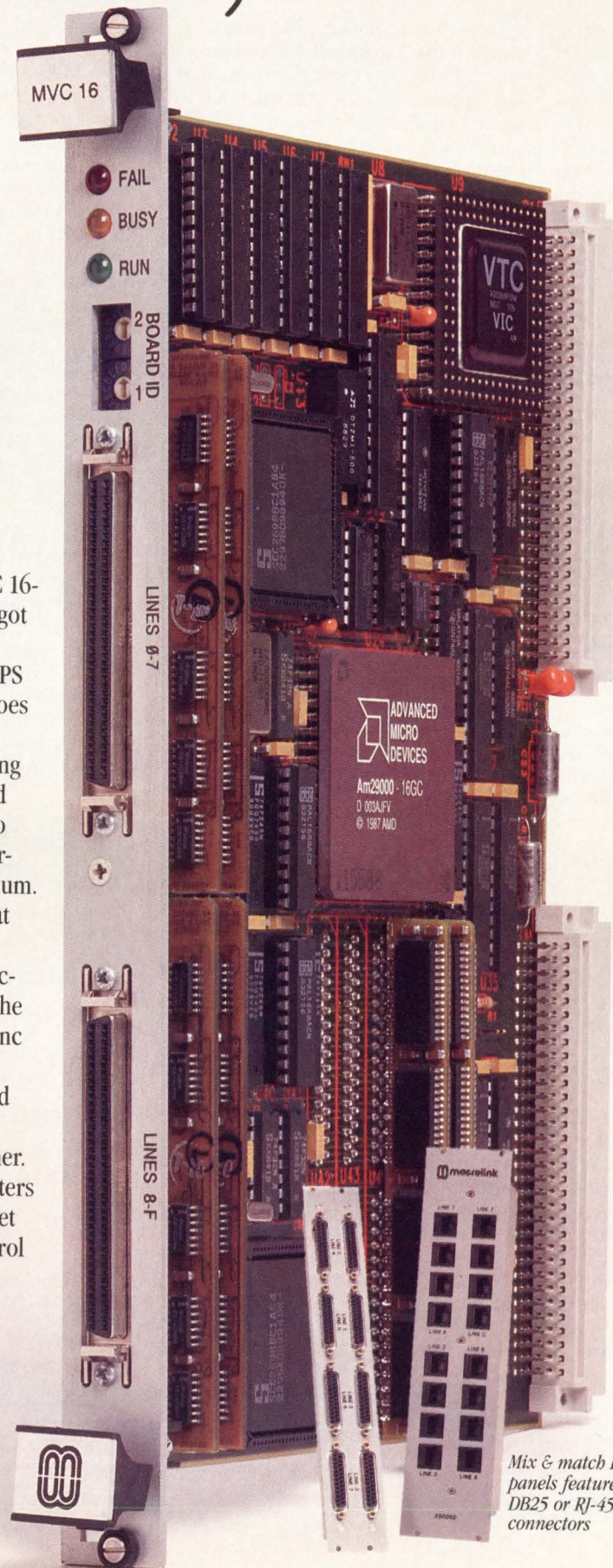
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INTEGRATED CIRCUITS

PSD attends to MCU's basic needs

Medieval knights depended on their faithful squires to carry their many weapons and support equipment for them. To wage their embedded control battles, microcontrollers also need many support devices. Including glue logic, typical designs require seven or more support devices just to perform basic functions. Providing microcontrollers with their own squire-at-arms, WaferScale Integration (WSI) invented Pro-

smaller, lower-power products, while simplifying the system development process and shortening time-to-market factors. Such applications include cellular telephones, hard disk controllers, modems, computer peripherals, and automotive systems. An alternative solution might be to pack the needed functions onto a field-programmable gate array (FPGA) or gate-array. But for cost-sensitive designs, off-the-shelf

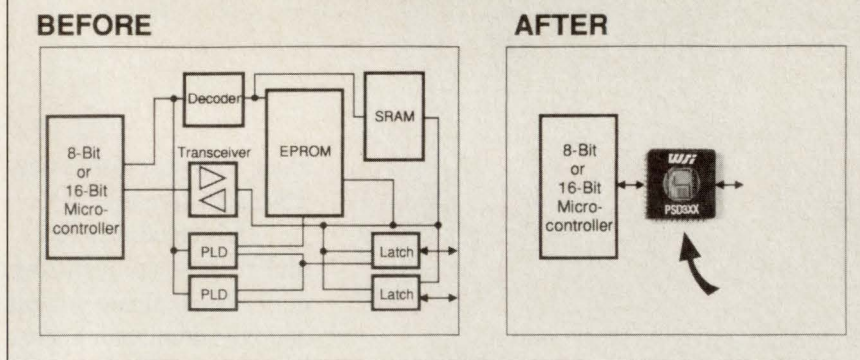
troller's external bus interface with other chips. In larger systems, designers can connect the parallel ports to the chip select outputs from the address decoders, using the address logic to select other chips. In addition, the PSD3XX offers a programmable security mode which locks the contents of the programmable decoders and all the configuration bits, making unauthorized duplication virtually impossible.

Because each PSD3XX family member is pin-compatible, designers can easily migrate from one to the other as memory needs increase. The speed grades available for the devices—120 ns, 150 ns, 200 ns—are nothing special by 32-bit standards but are more than adequate for 8- and 16-bit applications. These speeds include all the elements on the device's architecture such as propagation delays in the address decoders, latches, transceivers, PAD, SRAM, or EPROM access times, etc.

The PSD302 and the PSD312 are currently available in a 44-pin, windowed ceramic leaded chip carrier and a plastic leaded chip carrier. Prices of the PSD3XX parts vary according to the amount of memory on-chip. Prices of the 512-kbit versions range from \$9 to \$11.

—Jeffrey Child

WSI's PSD3XX PROGRAMMABLE MICROCONTROLLER PERIPHERAL



Many 8- and 16-bit MCU applications need seven or more support devices to perform basic functions. Using WSI's PSD3XX eliminates the need for these extra parts, while letting the MCU access other chips in the system through the PSD3XX's I/O ports.

grammable System Device (PSD)—a single-chip microcontroller support device with port expansion, latched addresses, page logic, programmable logic arrays, interface to shared resources, EPROM, and SRAM. Now WSI's added five new members to its PSD3XX family of devices offering designers a choice of memory configurations and special features.

Providing standard microcontrollers with all the basic support capabilities, the PSD3XX family of devices interface with many popular 8- and 16-bit microcontrollers including 8051s, 6805s, 68020s, Hitachi H8/300s and Zilog Z80s. All PSD3XX parts have 16-kbit SRAM. Using its proprietary, extremely small EPROM-cell design, WSI also squeezed 256 kbits to 1 Mbit of EPROM onto the parts.

Using the PSD3XX family lets embedded-control system designers, who use microcontrollers, build

parts usually make more sense.

Each member of the PSD3XX family offers a unique programmable single-chip solution for microcontrollers needing I/O reconstruction and more EPROM and SRAM than the microcontrollers' internal memory. Other peripheral functions—such as chip-selects, control signals or latched address lines—are also integrated on the chip.

At the heart of the PSD3XX devices are two programmable address decoders. Basically PALs without latches, the decoders can be programmed to set the address ranges of the memory. For microcontrollers with limited address ranges, memory can be arranged in pages and broken up into non-adjacent areas.

The PSD3XX devices are more than the sum of the parts they replace. To enhance system I/O capability, two 8-bit parallel ports and one 3-bit parallel port are included on the device. These let a microcon-

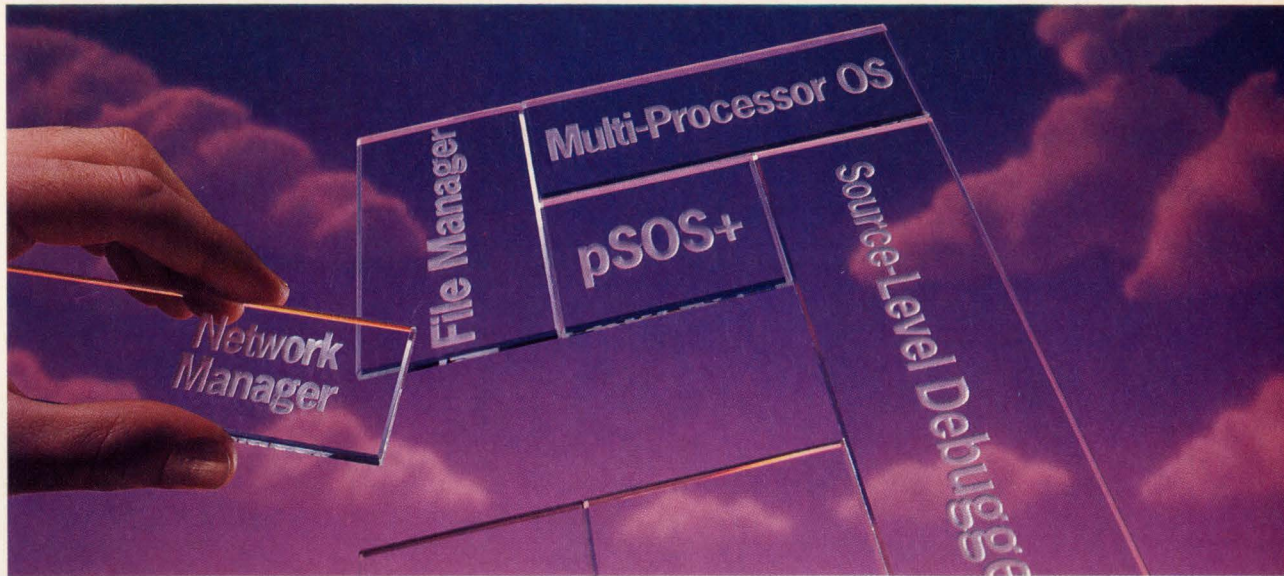
PSD3XX family devices at a glance:

- Single-chip support for 8- and 16-bit microcontrollers
- 16 kbits of SRAM
- 256 kbits to 1 Mbit of EPROM
- Compatible with 8051s, 6805s, and several other MCUs
- Access times down to 120 ns
- Security mode prevents code duplication
- MCUs can access other chips through the PSD3XX
- Programmable decoders allow memory paging

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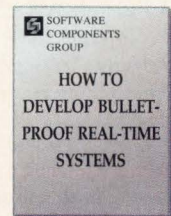
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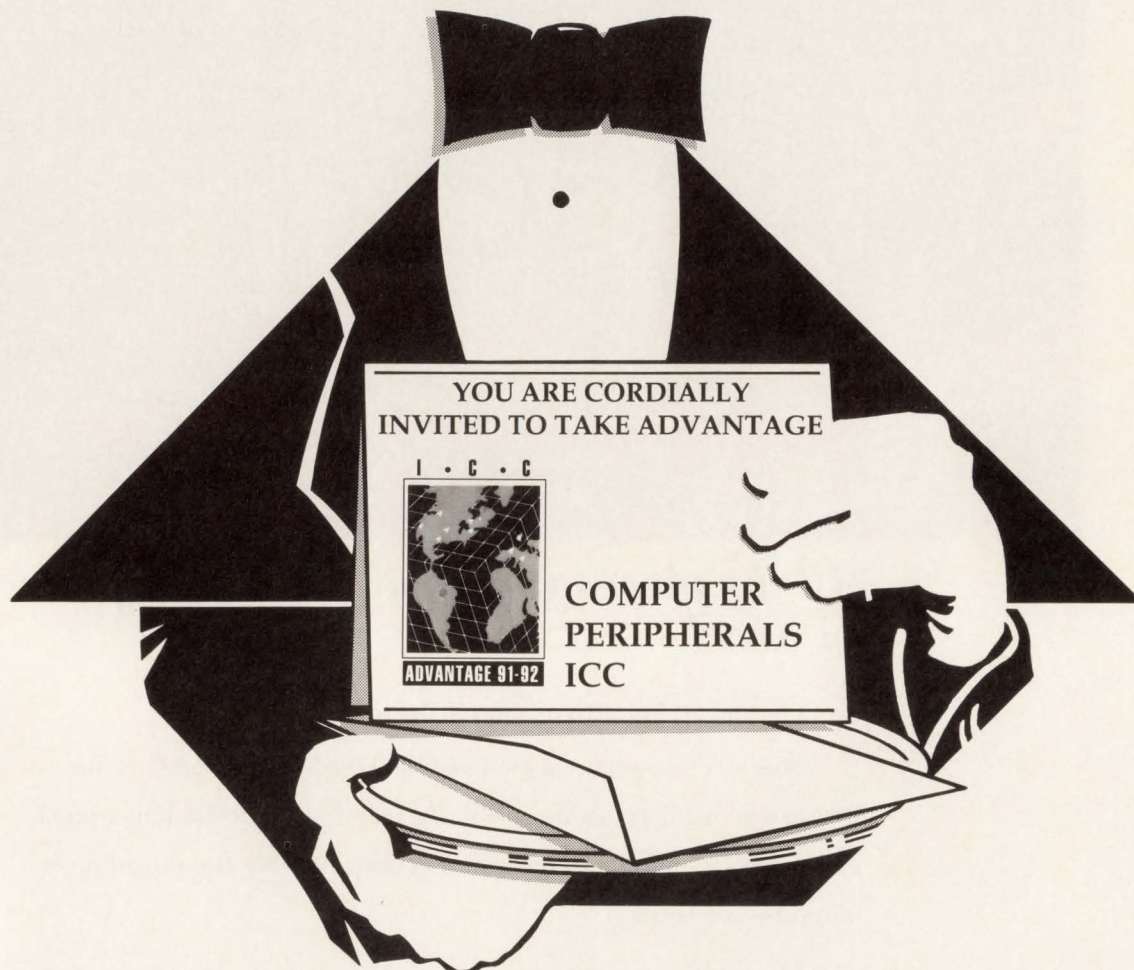


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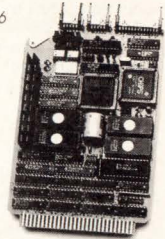
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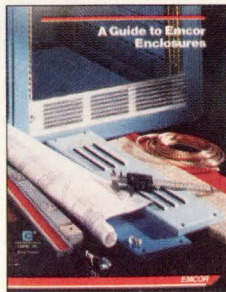
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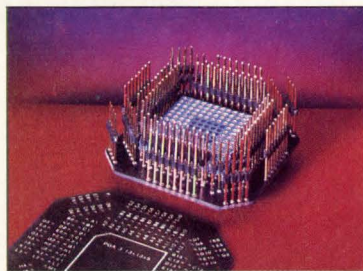
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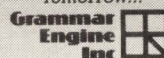
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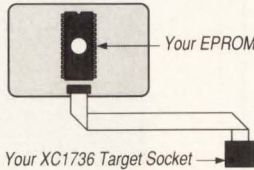
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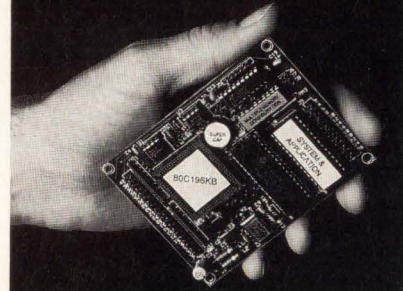
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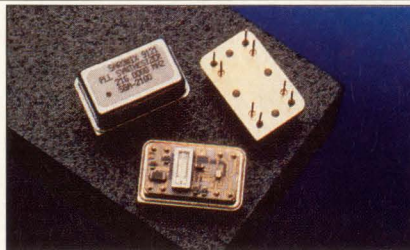
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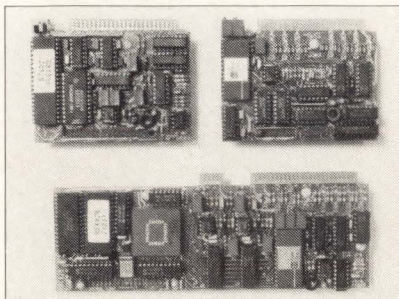
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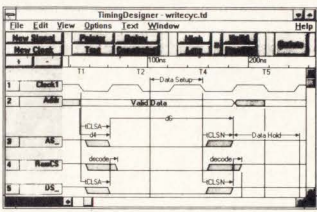
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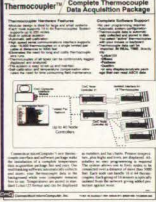
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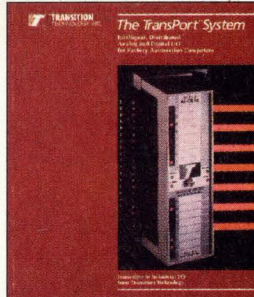


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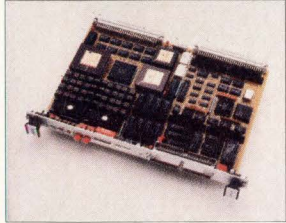
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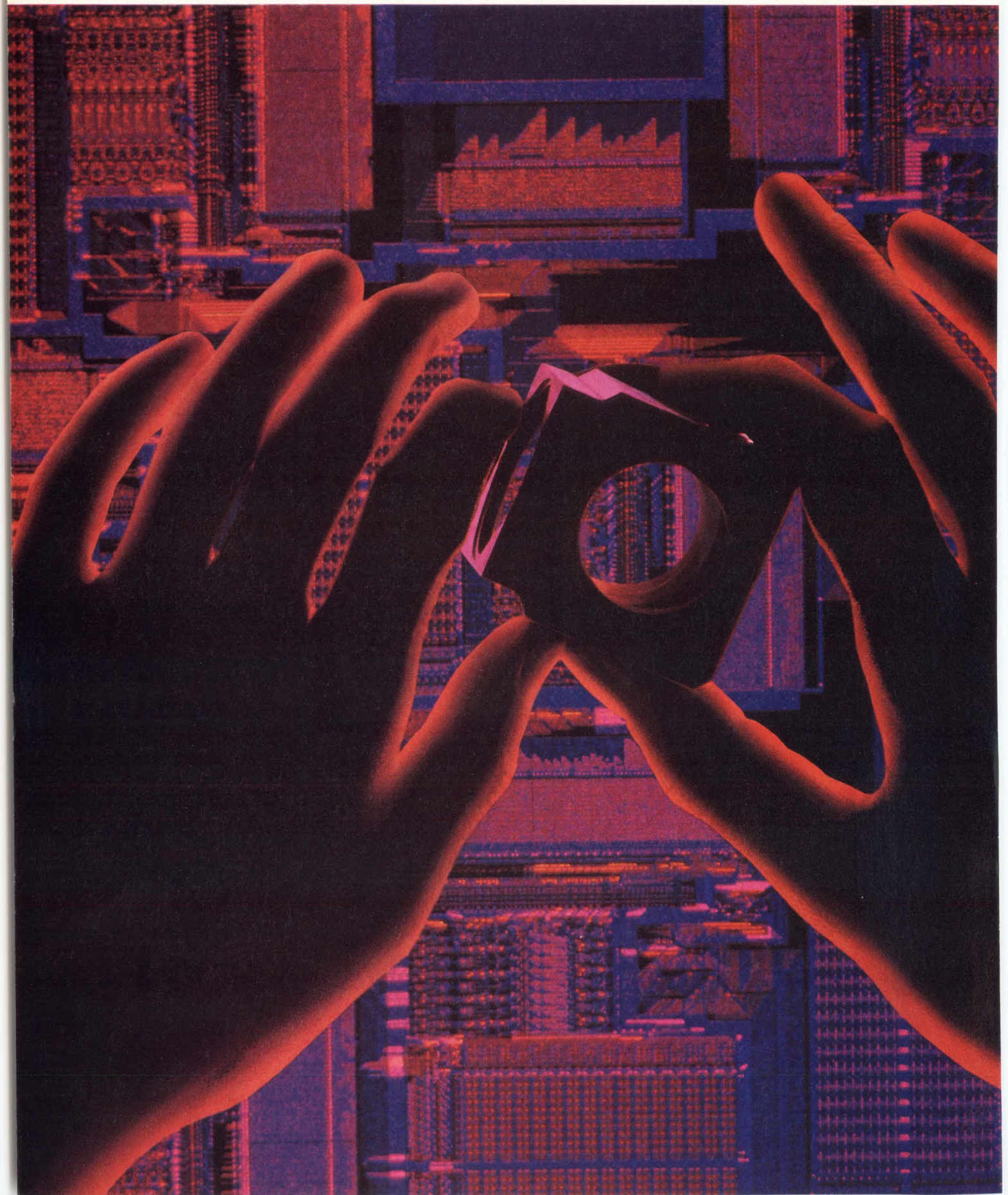
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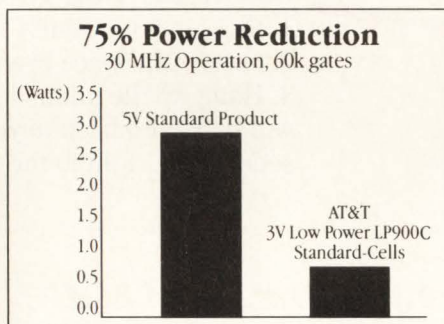
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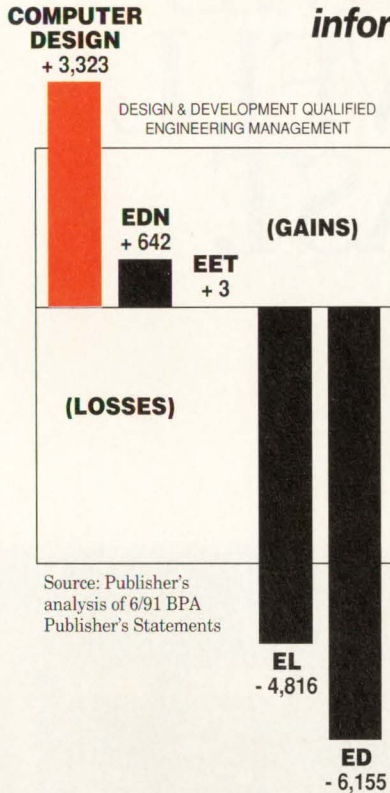
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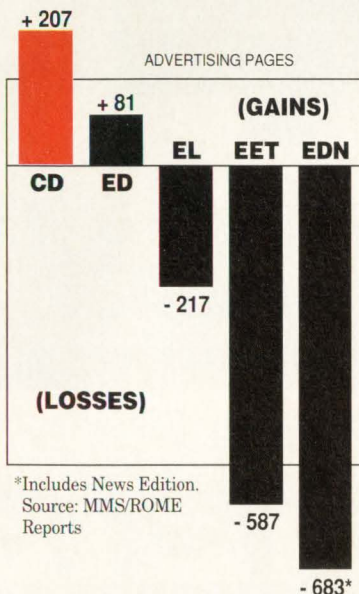
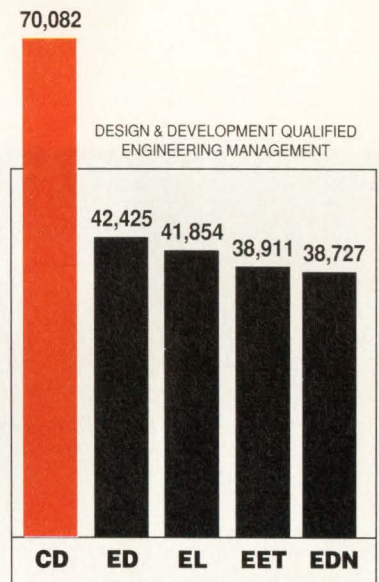


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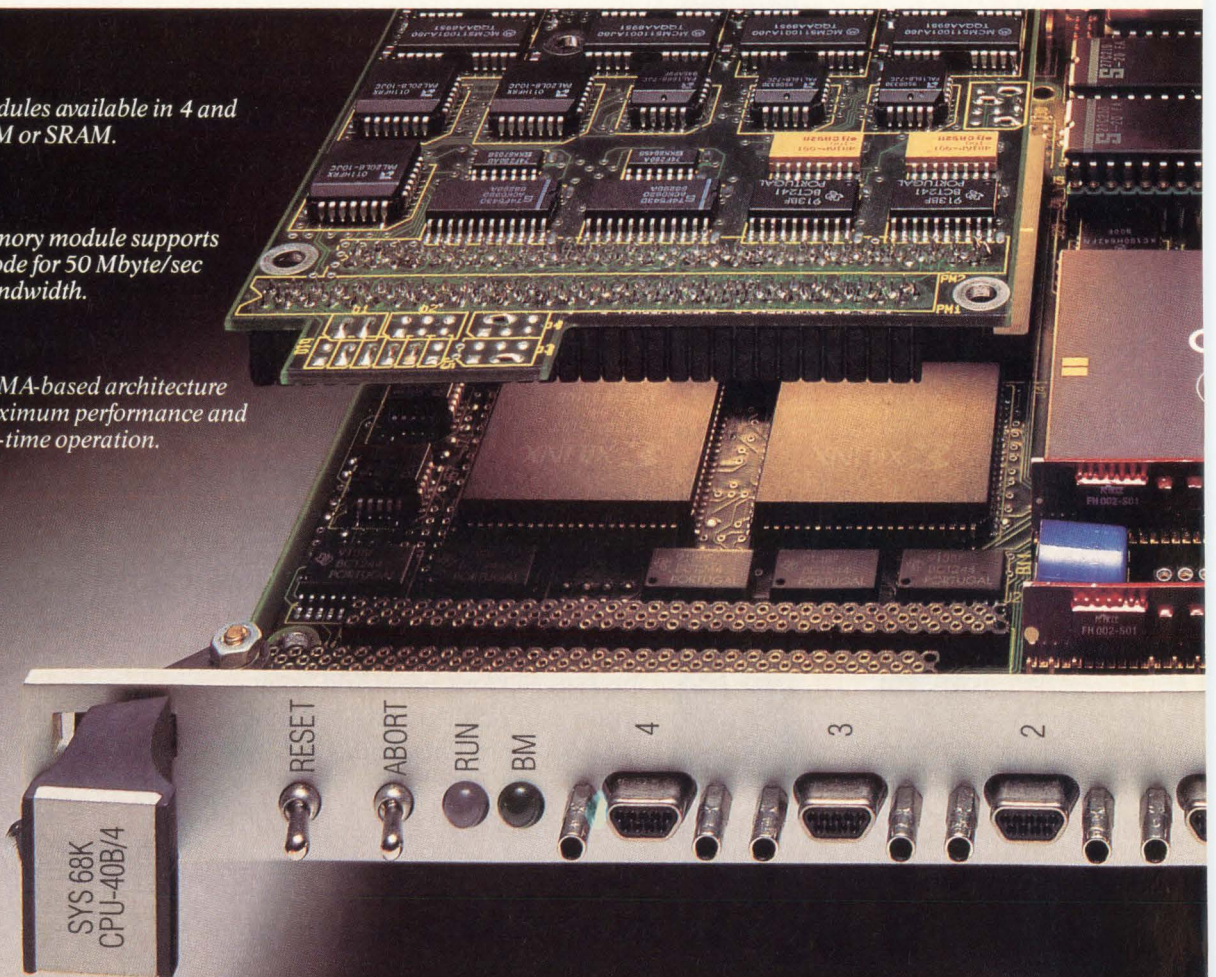


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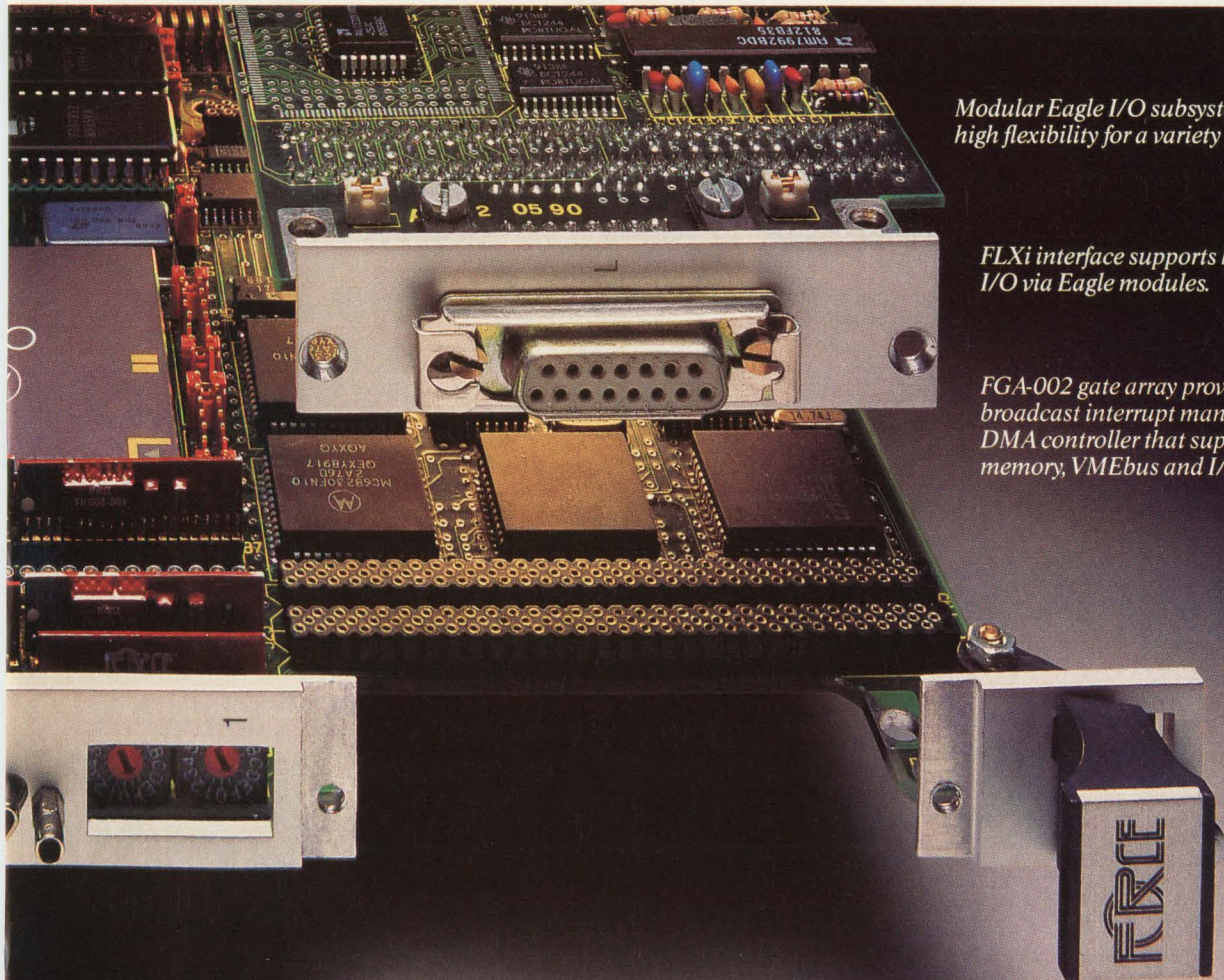
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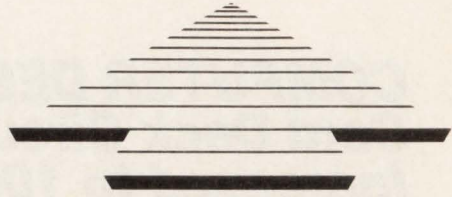
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# COMPUTER DESIGN



Coming in January from **COMPUTER DESIGN...**

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**The Guide:** The Guide will include the full exhibitor listing and descriptions, a dining and entertainment guide, a major value-added bus/board market overview and analysis— plus, a new products section— and inquiry card.

**Value-added Editorial:** This winter's official Buscon Show Guide, mailed with the January issue of COMPUTER DESIGN and distributed to all show attendees, will feature the usual show information — technical session descriptions and schedule, exhibitor listing, dining and events in the Long Beach, CA area — but will be enhanced by two editorial features of special interest to COMPUTER DESIGN readers, Buscon attendees and exhibitors:

- First is a marketing overview of the bus/board industry written by Warren Andrews. This overview will analyze the often confusing and contradictory data on the size of the board business and projections for its future development and growth.
- The second feature will be New Products, in which the products being introduced at Buscon, or which were introduced to the marketplace since Buscon/91-East, will be highlighted.

**Distribution:** The guide will be polybagged along with the Western portion of COMPUTER DESIGN's January issue for a total distribution of 50,000+. In addition, a special mailing will go to all of the pre-registrants...and it will be distributed to each attendee at the show.

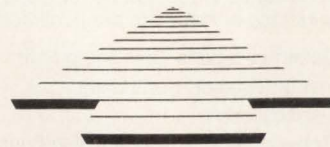
**Issue Date:** January, 1992

**Pricing:** \$2,200 Per Page — including color.

**Savings Opportunity:** Advertise in the February Show issue of COMPUTER DESIGN and save \$500 per Show Guide page.

**Closing:** December 10, 1992

**BUSCON/92-West**  
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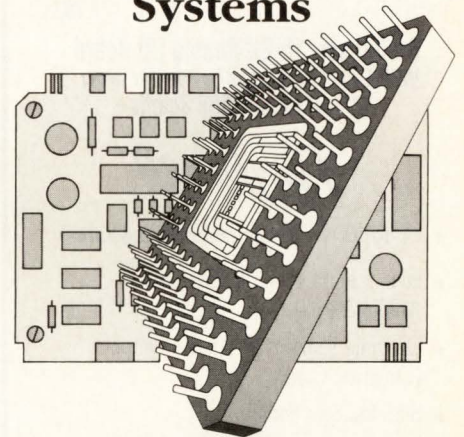
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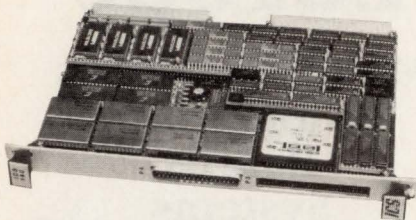
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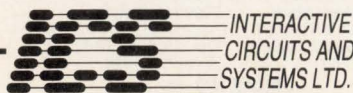
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(508) 692-0700 Fax: (508) 692-7780 Telex: 883436

**Publisher:** David L. Allen (508) 392-2111

**Associate Publisher/Editor-in-Chief:** John C. Miklosz (508) 392-2114

**Associate Publisher/National Sales Manager:** Tim L. Tobeck (508) 392-2116

**Administrative Assistant:** Peg Alexander (508) 392-2112

**Marketing Specialist:** Betsy Anderson (508) 392-2209

**Ad Traffic Manager:** Kelly Rice (508) 392-2198

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## SALES OFFICES

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Tel: (508) 392-2118  
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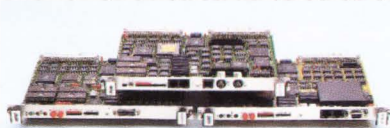
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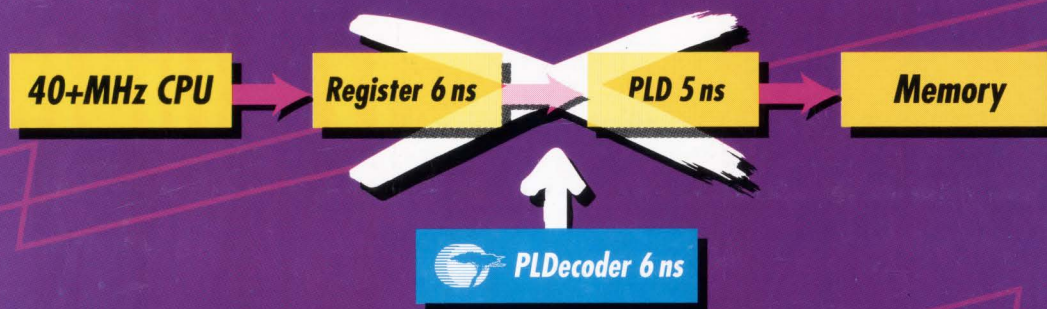
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