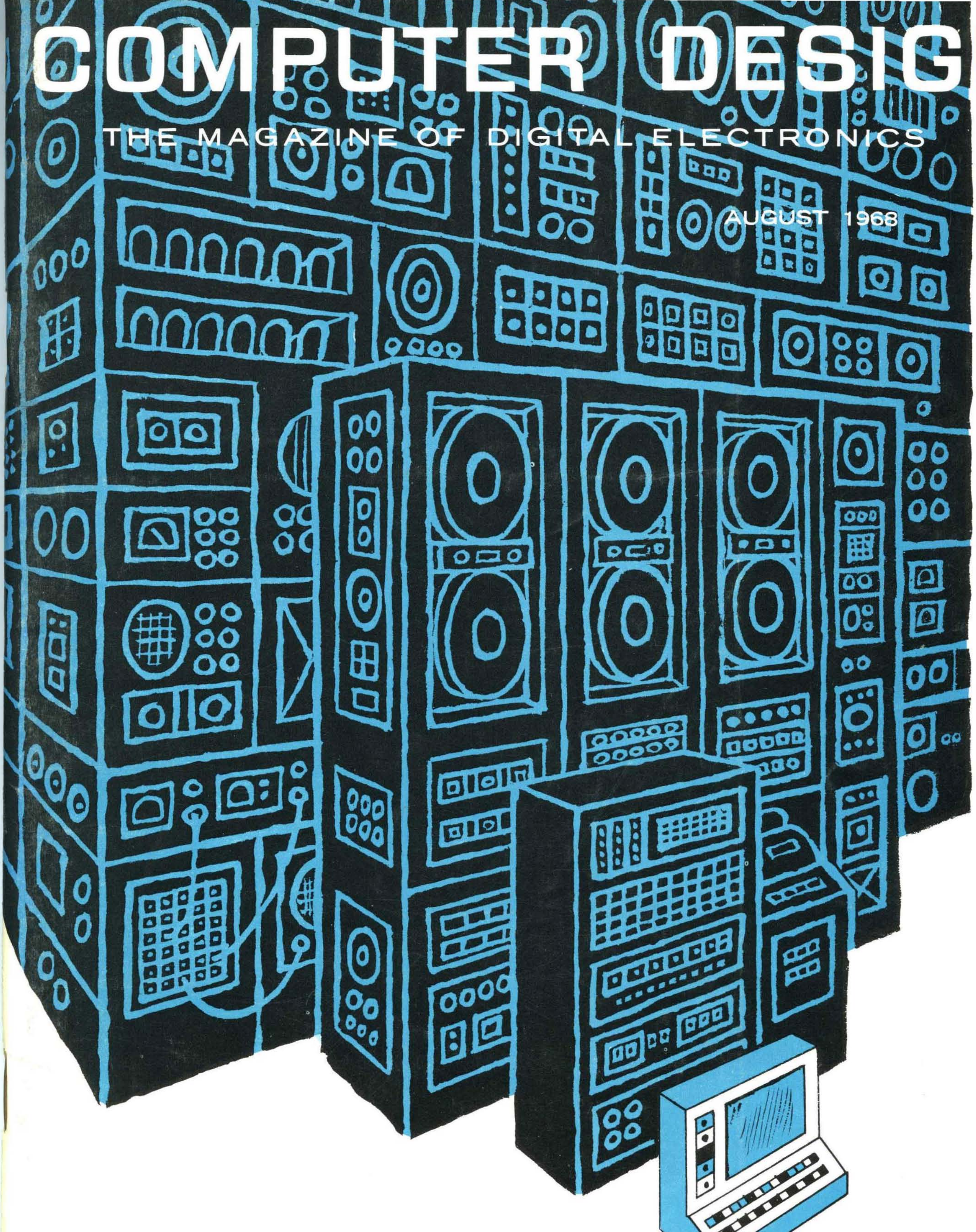
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1968



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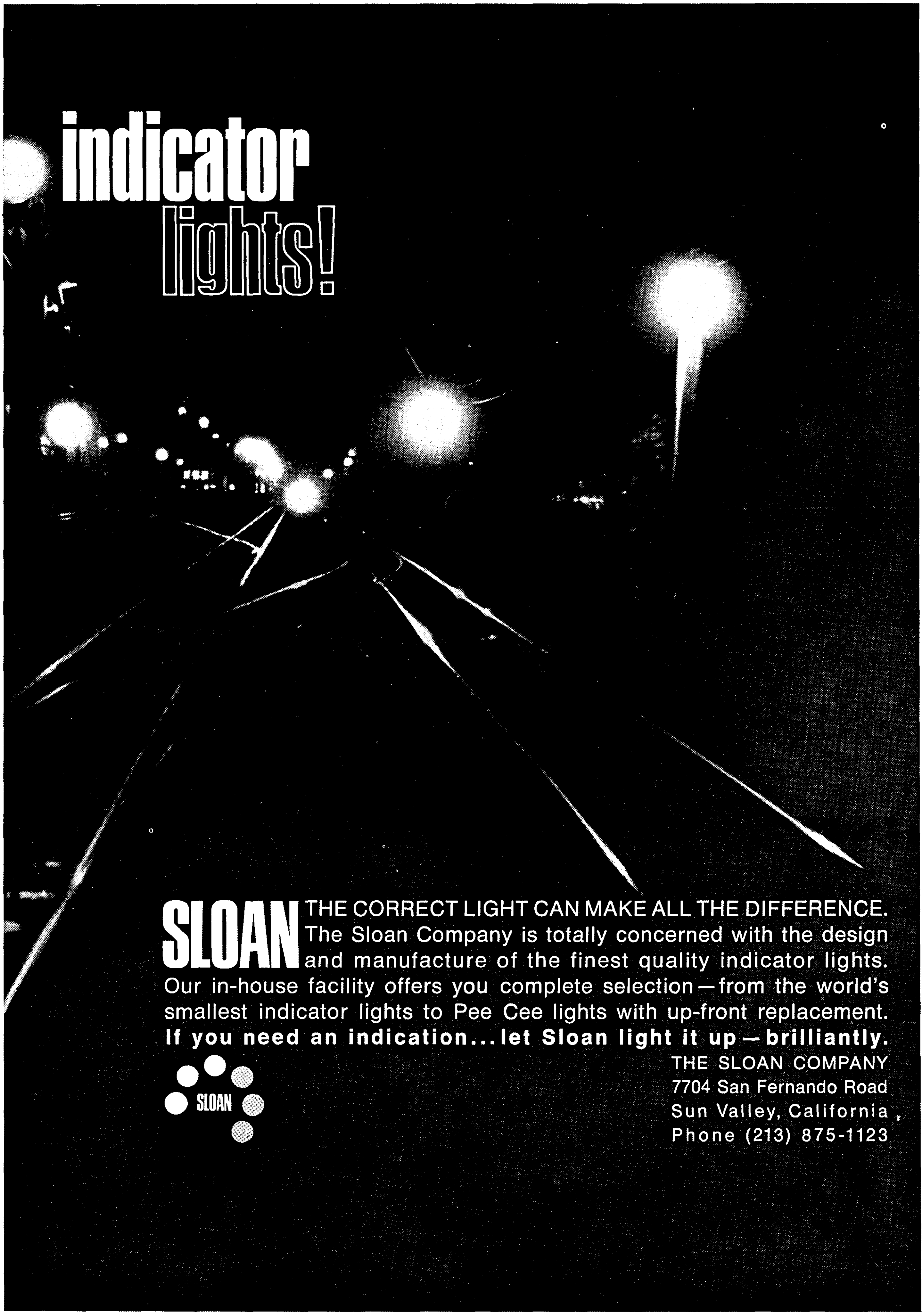
A PREVIEW OF WESCON 68


indicator
lights!
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The Sloan Company is totally concerned with the design and manufacture of the finest quality indicator lights. Our in-house facility offers you complete selection—from the world's smallest indicator lights to Pee Cee lights with up-front replacement.
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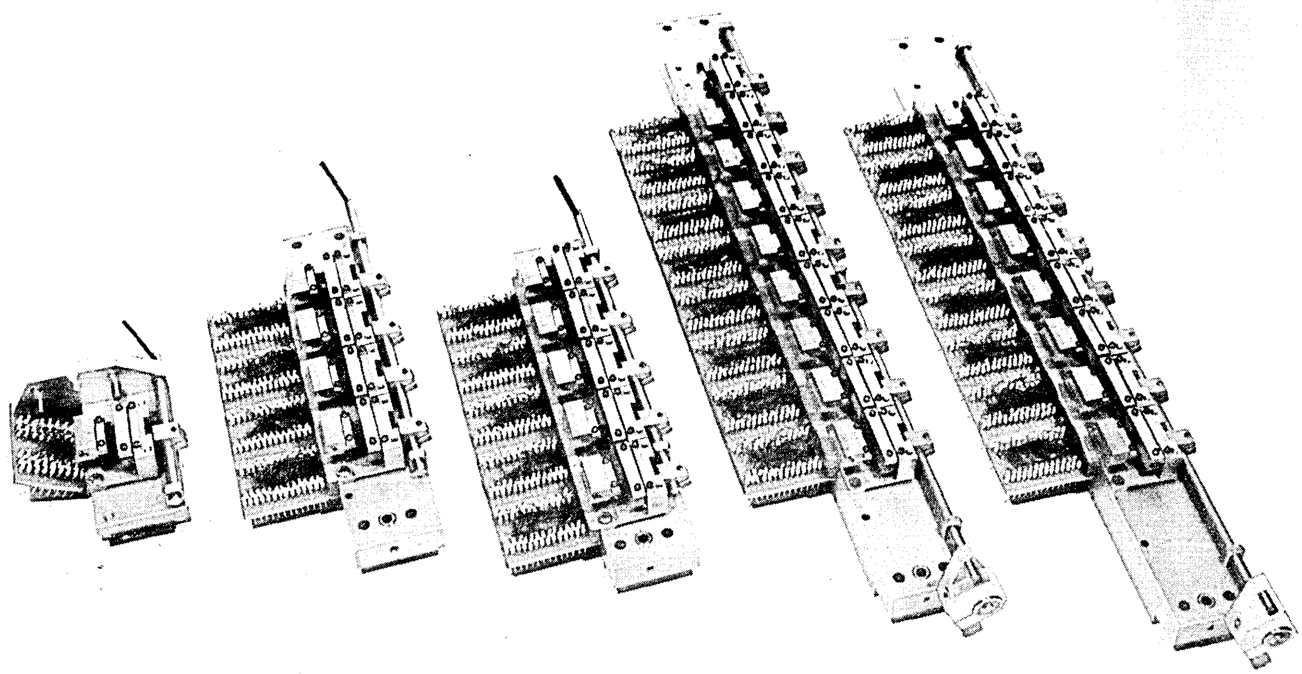

Fact:

One Head is better than Five

When you look closely at the head assemblies used on our five standard drums, you can see they're really all the same. The same 16-head flying pads. The same unique compliant-reed mounting. The same connectors. The same spare heads. The same reliable head actuating mechanism. Whether the drum has 128, 512 or 1024 tracks . . . measures 10″ or 20″ in diameter . . . is partially or full implemented.

In other words, the VRC common-design concept means one head is better than five. And the standard heads are only one facet of this concept. All five of our standard drums use the same self-clocking interface micro-electronics. All five share the same connector pin layouts . . . the same speed sensors . . . and the same 1-year warranty.

Thanks to common design, VRC drums (2.6 to 67.5 megabit capacities) give you reliable, flexible economical performance. And that means application, installation, training and service costs stay low, no matter which VRC drums, or how many drums, you use.

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. . . so is **Vermont Research CORPORATION**

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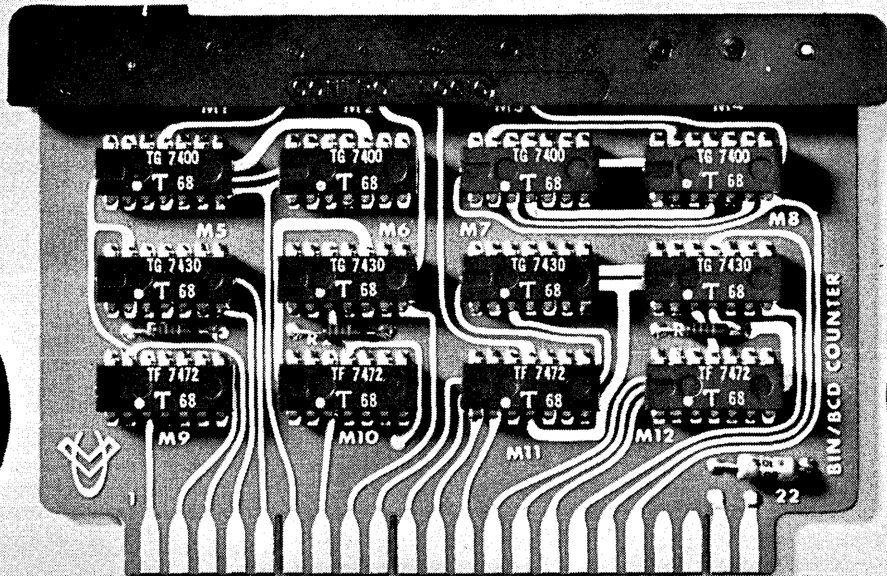
CIRCLE NO. 2 ON INQUIRY CARD

we've added another to the series



The 7400 T^2L, our latest micro-logic circuit card. How did we do this? We just placed a comma after our last development, the automatic wire-wrap assembly. The series now looks something like this: T^2L SUHL I, T^2L SUHL II, DTL, AW, 7400 T^2L, and . . . We've placed a comma after the 7400 because we're not done yet. Write or telephone for more information about our methods of punctuation.

CONTROL LOGIC, INC., 3 Strathmore Rd., Natick, Mass. 01760 · 617/235-1865.

Visit Control Logic at Wescon — booth nos. 182-183

Editorial & Executive Offices
Prof. Bldg., Baker Ave.,
W. Concord, Mass. 01781
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BPA Circulation over 40,000

← CIRCLE NO. 3 ON INQUIRY CARD

AUGUST 1968 • VOLUME 7 • NUMBER 8

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

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While developing the industry's broadest memory line, we've built billions of cores. Fast cores with wide operating margins, cores for all the major computer programs and cores on most of the satellites. In fact, we've got all the core types you're most likely to need. As a result, you'll get the convenience and economy of filling all your requirements from a single source.

Our magnesium-manganese cores come in diameters from 18 to 80 mils and operate over the temperature range of 0 to +65°C. We can provide cycle times under 600ns and make so many for our own systems that we know they'll work for you.

For our wide temperature, coincident current memories, we make 18 to 30 mil lithium ferrite cores. They operate from −55 to +125°C, require minimum current compensation and offer wider operating margins than standard ferrites.

We have these and other core types in production now. Write for full details.

electronic memories EM

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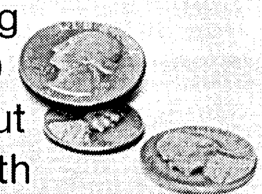
We've decided it's time we stopped being our own best core customer.

CIRCLE NO. 4 ON INQUIRY CARD

Is it possible to get a really good computer for less than $10K? How about $9,950 and some odd change?

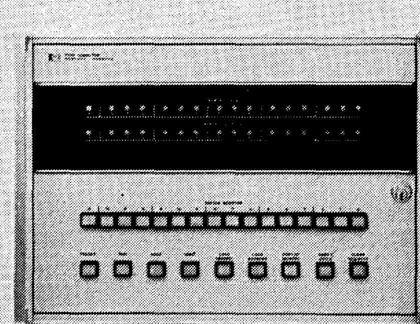
That's what the new Hewlett-Packard 2114A will be pegged at. But it'll heave to just like its big brothers. Throwing around big 16-bit words. Storing 4000 (or 8000) of them at a time in memory. Fetching them out of memory in two microseconds. It'll tie in I/O devices with standard plug-ins and use the same set of programming languages—FORTRAN, ALGOL and Conversational BASIC. It may be the littlest computer in the HP family... but even at that it more than holds its own against its big brothers.



That's right. The HP 2114A offers the most desirable price/performance ratio of any computer on the market. And it won't take up much room, either, not even on your desk. One compact package 12¼" tall houses both processor and power supply.

Yet the economy model is fully compatible with all the 2115/2116 software and I/O interfaces. The main frame accepts either 4K or 8K memory, has eight I/O plug-in slots and operates within a wide temperature range. Low-cost options include parity error check and power-fail protection.

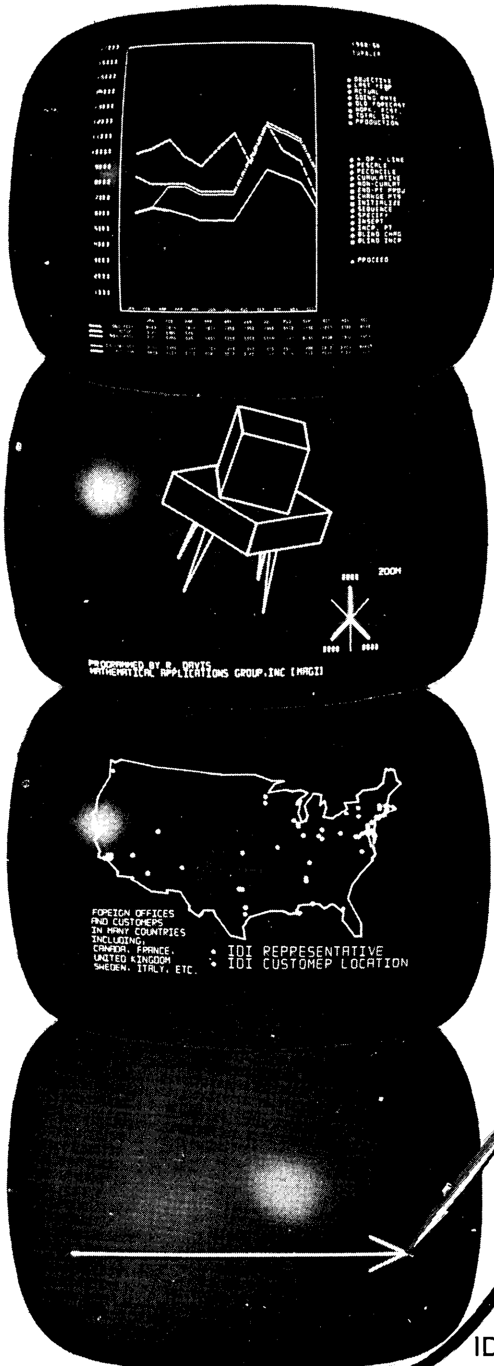
If you think this powerful little computer is right for you, get more information from your local HP field engineer. Or write Hewlett-Packard, Palo Alto, Calif. 94304; Europe: 54 Route des Acacias, Geneva.



HEWLETT *hp* PACKARD

DIGITAL COMPUTERS

06810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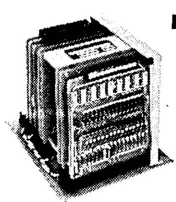
The case for our micromemory.



There is none.

Most memories available today come in nice packages. Totally-enclosed, well-protected, and looking like they still belong to the original manufacturer.

We've got one that doesn't look like it belongs to anyone. Our newest system for industrial/commercial applications, the MICROMEMORY™ 1000, provides up to 32K bits of storage with a cycle time of 2.5 usec for less than 7 cents/bit. And it's just as economical with space (400 cubic inches) and power (35 watts maximum).

But it has no case. The system consists of a stack and five cards of electronics that plug into an unenclosed mother board, with a single connector providing the I/O interface for integration into your system. Maintainability is enhanced by this configuration even though you'll probably never have to take advantage of it. The same advanced 3D drive technique that gives you the lower price because of a lower component count also yields a correspondingly higher MTBF.

The MICROMEMORY 1000 will fit almost anyplace in your system. Its open construction leaves access unhampered, while its low power dissipation eliminates the need for additional cooling. Mount it upside down or sideways, show it off or hide it. It looks like it belongs in your system because it does.

Price and delivery, true random access and ease of electrical interface all strengthen the case for the MICROMEMORY 1000. Write us for the full story.

EM electronic memories

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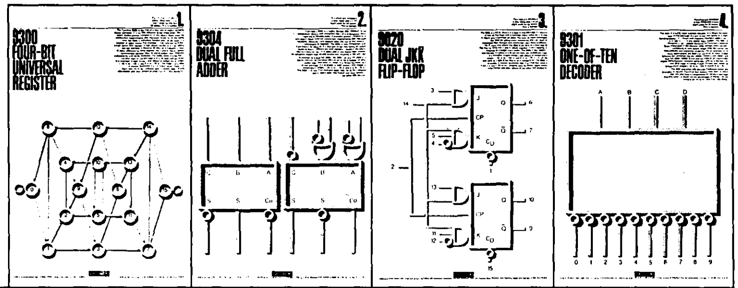
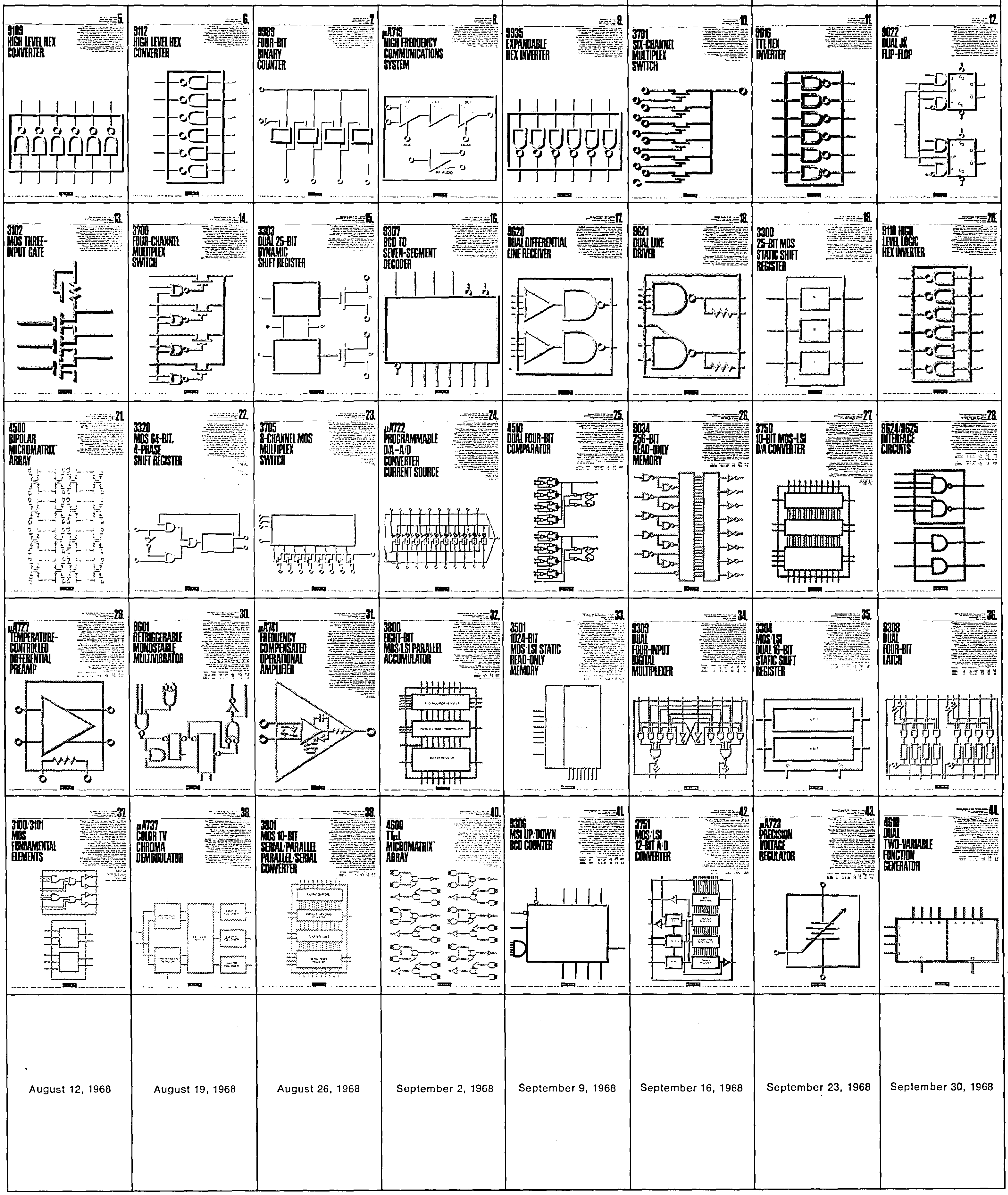
CIRCLE NO. 7 ON INQUIRY CARD

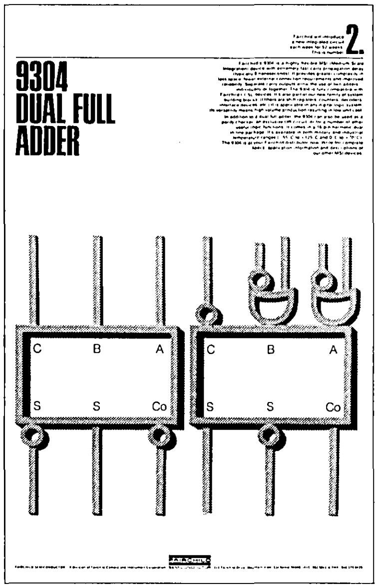
Fairchild has introduced 44 new products in the last 44 weeks.

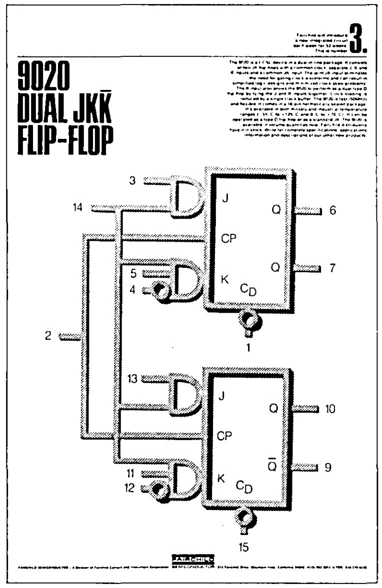
Our goal is fifty-two new integrated circuits in fifty-two weeks. To obtain the Reader Service number for any product announcement ad, simply add 100 to the new product number. For example, New Product No. 3 is Reader Service No. 103.

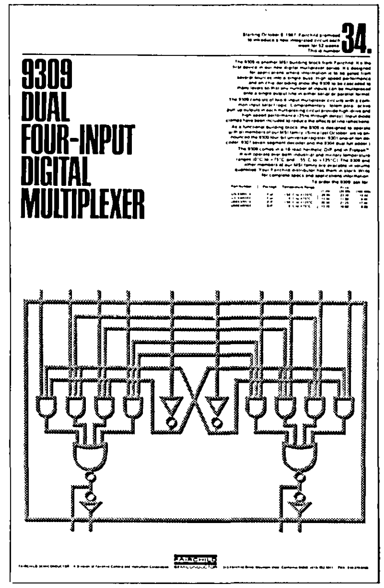




More about:

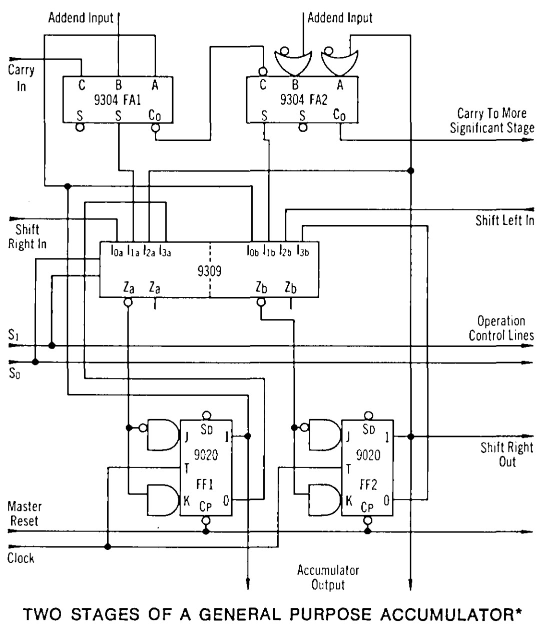






General purpose accumulator

Three new Fairchild ICs will give you two stages of a general purpose accumulator that can shift left, shift right, add, complement and clear.



TWO STAGES OF A GENERAL PURPOSE ACCUMULATOR*

Two of the new devices are highly versatile MSIs: The 9304 Dual Full Adder and the 9309 Dual Four-Input Digital Multiplexer. They provide the same gating functions as seven or more discrete components. This low device count is the result of Fairchild's systems approach to designing complex circuitry. Our MSIs (and LSIs) are specifically designed to work together without interface circuitry. And, each device is highly versatile. For example, the 9304 used in this application can be used in other systems as an adder, parity checker, exclusive OR circuit, or for a half-dozen other useful logic functions. You get the benefits of lower costs for design and devices, and higher reliability because of fewer connections. The third new device is our 9020 Dual JKK̄ Flip-Flop. Like the 9304 and 9309, it is a dual device with the flexibility of two functional elements per package.

OPERATION CODE LIST		
S_0	S_1	INSTRUCTION
0	0	Shift Left
1	0	Add
0	1	Shift Right
1	1	Complement

The key device in this application is the dual four-input multiplexer. It provides logical implementation of a two-pole four-position switch that routes data to the commoned J and K inputs of the dual JKK̄ flip-flop. (Note that in this application we have taken advantage of the inherent symmetry of the 9020; the J and K inputs have been reassigned so the faster negation output of the 9309 can be used.) Depending upon the condition of the S_0 and S_1 inputs of the multiplexer, the data provided to the flip-flops cause a left shift, right shift, addition of an externally supplied number, or the complementing of the register. A common direct clear sets the register to the all-zero condition.

The 9304, 9309 and 9020 come in 16-pin hermetic DIPs. They're available from your Fairchild distributor in both military and industrial temperature ranges. For complete specs and other applications information, circle Reader Service numbers 102, 103 and 134.

*Additional stages can be produced by repeating the same functional design.

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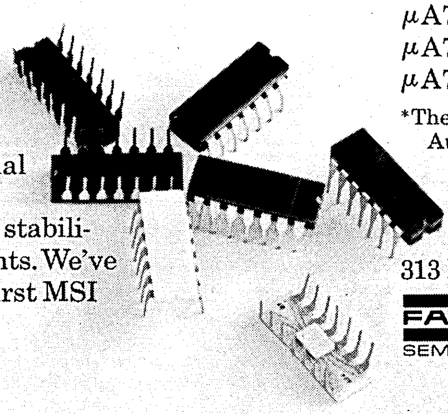
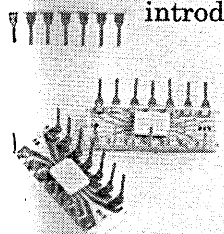
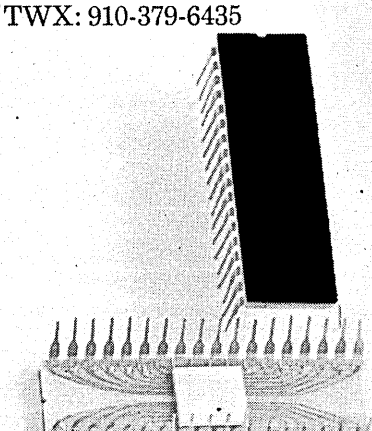




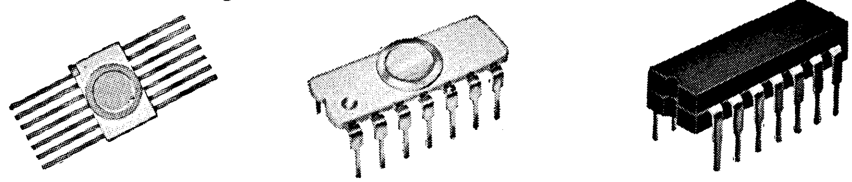


RCA CD2300 DTL Family

direct replacements for 830 and 930 series

45 types / 3 package styles / 2 Temperature Ranges
Gates / Expanders / Flip-Flops / Inverters
2KΩ and 6KΩ Output Pull-Up Options

- For Your Military Applications:
  CD2300 Series—15 circuits in RCA's Unique Ceramic Flat Package.
  CD2300D Series—15 circuits in RCA's Unique Ceramic Dual In-Line Package.
- For Industrial and Commercial Applications:
  CD2300E Series—15 circuits in RCA's Dual In-Line Silicone Package.



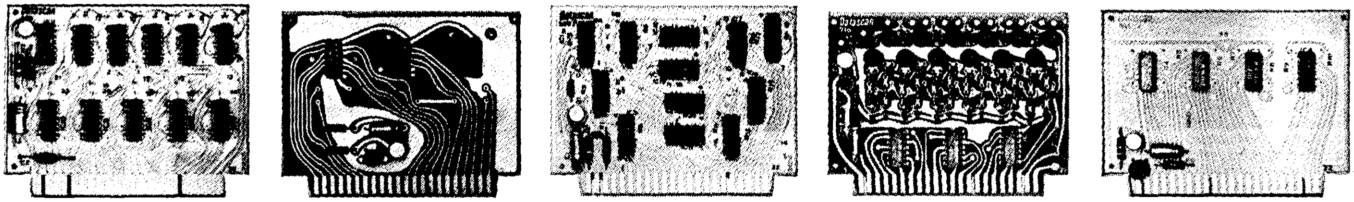
	–55°C to +125°C Operation				0°C to +75°C Operation	
Circuit and Pull-up Option	**14-Lead Ceramic Flat Pack**	**Price (1000 Units)**	**14-Lead Ceramic Dual In-Line Package**	**Price (1000 Units)**	**14-Lead Dual In-Line Silicone Package**	**Price (1000 Units)**
NAND Gates						
Dual-4 Expandable (6KΩ)	CD2300/930	$2.50	CD2300D/930	$2.50	CD2300E/830	$1.05
Dual-4 Expandable (2KΩ)	CD2301/961	$2.50	CD2301D/961	$2.50	CD2301E/861	$1.05
Dual-4 High Fanout, Expandable (transistor output pull-up)	CD2306/932	$2.75	CD2306D/932	$2.75	CD2306E/832	$1.15
Dual-4 High Fanout Expandable (no output pull-up)	CD2307/944	$2.75	CD2307D/944	$2.75	CD2307E/844	$1.15
Triple-3 Input (6KΩ)	CD2308/962	$2.75	CD2308D/962	$2.75	CD2308E/862	$1.15
Triple-3 Input (2KΩ)	CD2309/963	$2.75	CD2309D/963	$2.75	CD2309E/863	$1.15
Quadruple-2 Input (6KΩ)	CD2302/946	$2.75	CD2302D/946	$2.75	CD2302E/846	$1.15
Quadruple-2 Input (2KΩ)	CD2303/949	$2.75	CD2303D/949	$2.75	CD2303E/849	$1.15
Hex Inverters						
Diode Input (6KΩ)	CD2310/936	$2.90	CD2310D/936	$2.90	CD2310E/836	$1.45
Diode Input (2KΩ)	CD2311/937	$2.90	CD2311D/937	$2.90	CD2311E/837	$1.45
Expandable Input (6KΩ)	CD2312	$2.90	CD2312D	$2.90	CD2312E	$1.45
Expandable Input (2KΩ)	CD2313	$2.90	CD2313D	$2.90	CD2313E	$1.45
Flip-Flops						
Clocked RS with JK Capability (6KΩ)	CD2304/945	$3.00	CD2304D/945	$3.00	CD2304E/845	$1.90
Clocked RS with JK Capability (2KΩ)	CD2305/948	$3.00	CD2305D/948	$3.00	CD2305E/848	$1.90
Input Expander						
Dual 4-Diode	CD2314/933	$2.25	CD2314D/933	$2.25	CD2314E/833	$ .90

Ask your RCA Representative for details. See your RCA Distributor for his price and delivery. For technical information, write Commercial Engineering, Section ICZB-8, RCA Electronic Components, Harrison, N.J. 07029.

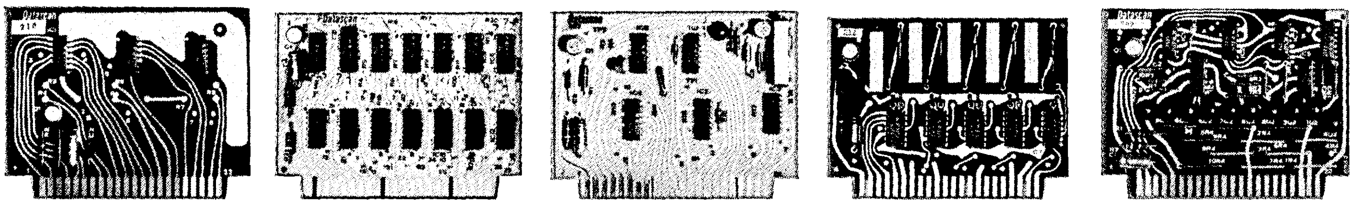
RCA
Integrated Circuits

CIRCLE NO. 27 ON INQUIRY CARD

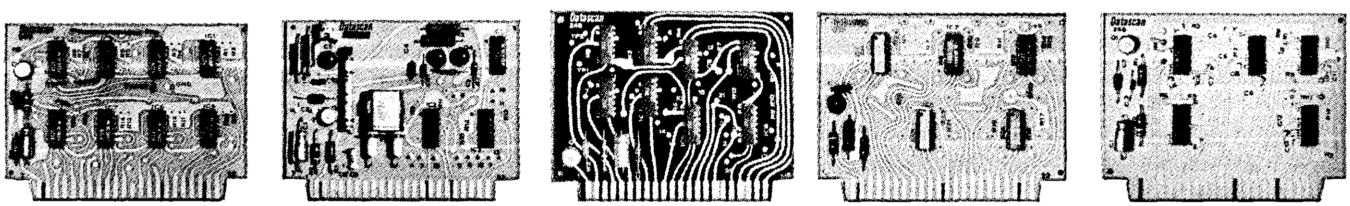
Let's talk about high noise immunity . . . number of



available logic functions . . . number of test points



per card . . . and economical logic system design

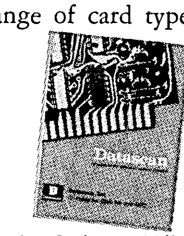


Datascan Integrated Circuit Logic Cards

Two complete lines — the Standard Series 200 (DTL) and the high noise immunity Series 400 (HTL) offer system designers maximum flexibility and economy in developing high performance systems. And, on every Datascan IC card you get these exclusive features:

- DYNAMIC DECOUPLING (Optional) — this is the only integrated circuit card that offers an active power supply decoupling element, to eliminate noise, particularly in larger systems.
- PULL-UP RESISTORS — provision has been made for adding resistors directly on individual cards.
- MORE TEST POINTS — located at all convenient circuit nodes, not limited in number — valuable in simplified system troubleshooting.
- CODED CARDS — color coded for quick identification of same-function cards; slot interpin keyed to prevent interchange of card types or card reversing.

Contact your local Datascan representative or call us direct, for complete technical catalog information or to arrange for engineering consultation.



System Designers: Write, on your company letterhead only, for a copy of the complete Datascan technical catalog and Application Notes — the most complete publication of its type in the electronics industry.

Datascan

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CIRCLE NO. 11 ON INQUIRY CARD

3 ways to get hermetic ICs at epoxy prices.

1. Call a Fairchild Distributor
On July 1, we reduced the price of all our DTL and TTL integrated circuits in hermetic DIPs. Now, they cost the same as competitive epoxy devices. And, you can buy them from any Fairchild distributor.

2. Call a Fairchild Salesman
If you get your samples from one of our salesmen, you might as well get quantity prices from him, too. Now he can quote on Fairchild ceramic devices from our competitor's epoxy price list.

3. Call Fairchild
Anyone who wants to call Mountain View can get the new ceramic prices directly from Fairchild. Ask for Larry Frankfurt. Dial (415) 962-2103

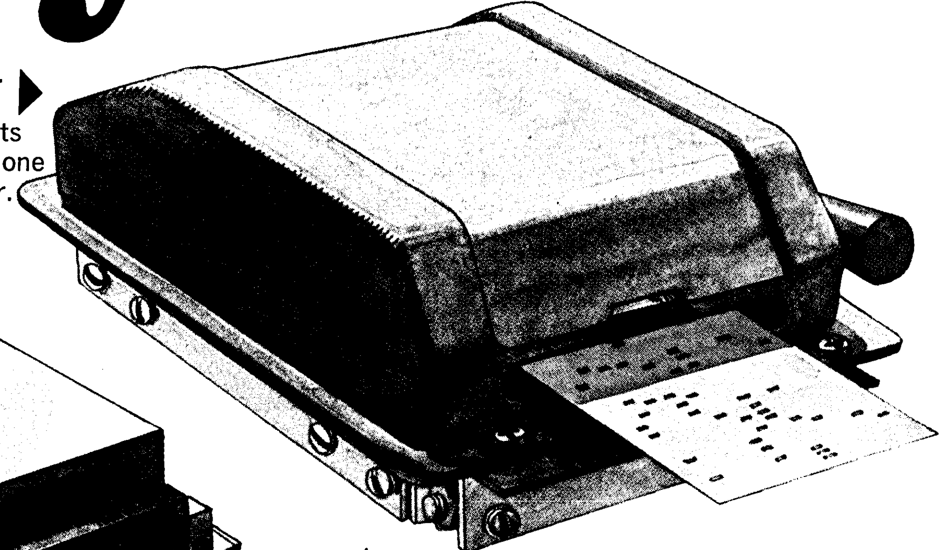
FAIRCHILD
SEMICONDUCTOR

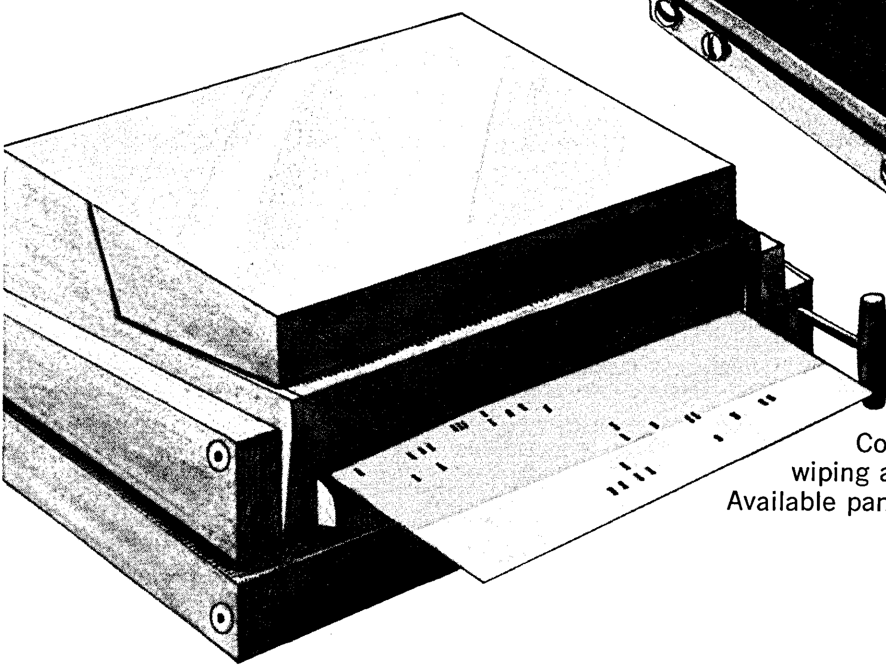
Fairchild Semiconductor/ A Division of Fairchild Camera and Instrument Corporation
313 Fairchild Drive, Mountain View Calif. 94040
(415) 962-5011 TWX: 910-379-6435

CIRCLE NO. 10 ON INQUIRY CARD

For your in

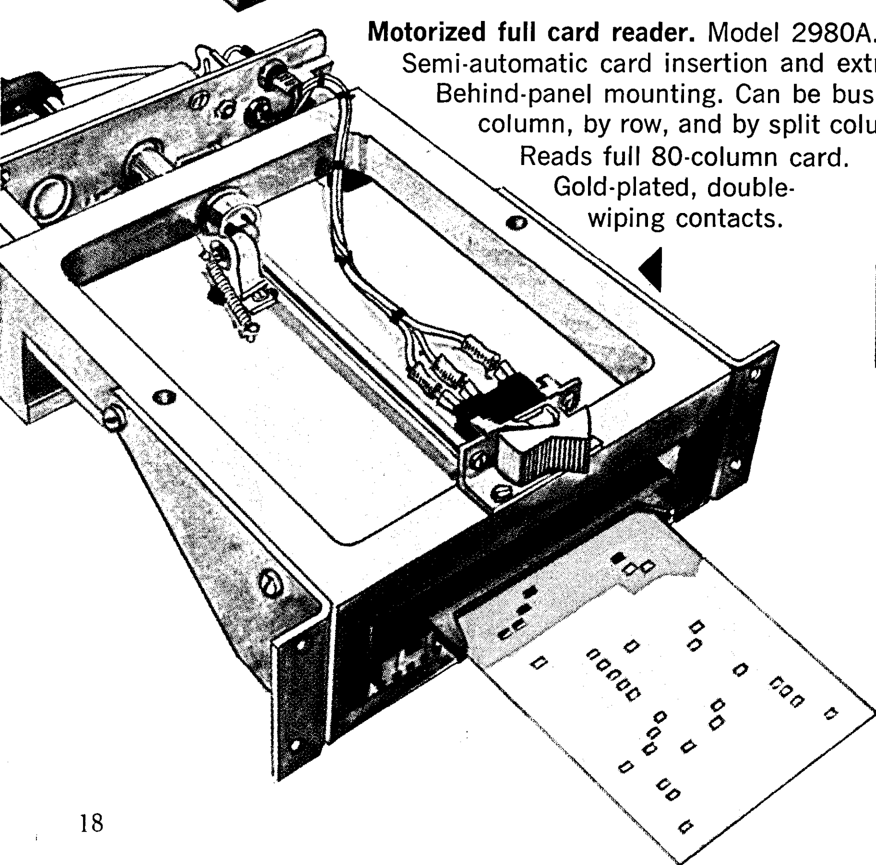
Industrial programmer. Model 2924. Isolated switches. Remote switch contacts. Precious-metal-clad contacts take 2 amps DC. Contacts tested to one million cycles. Full 80-column reader.

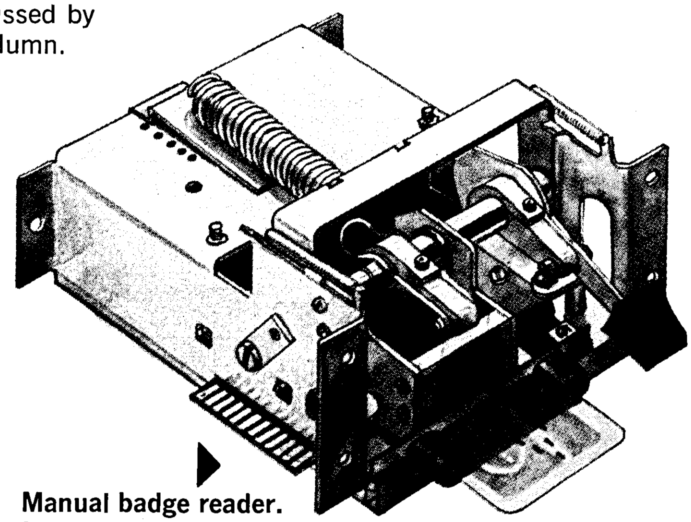




Desktop card reader. Model 1040. Up to 960 switches, 80-column format. Available in matrix or isolated outputs. Contact rating of 0.25 amp DC. Double-wiping action cleans contacts at each use. Available panel mounted.

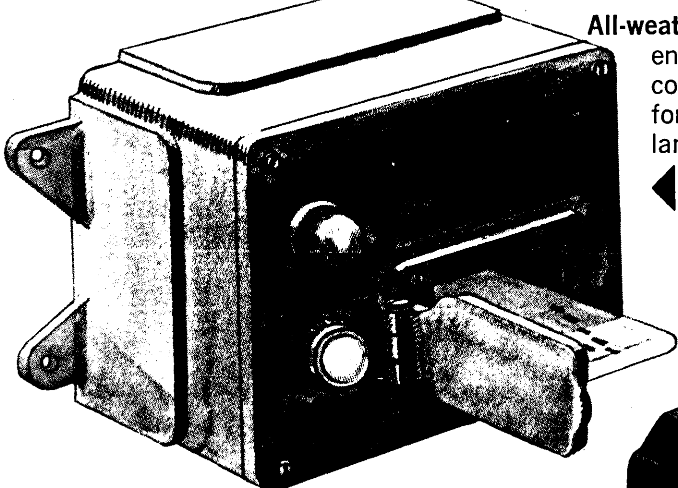
Motorized full card reader. Model 2980A. Semi-automatic card insertion and extraction. Behind-panel mounting. Can be bussed by column, by row, and by split column. Reads full 80-column card. Gold-plated, double-wiping contacts.





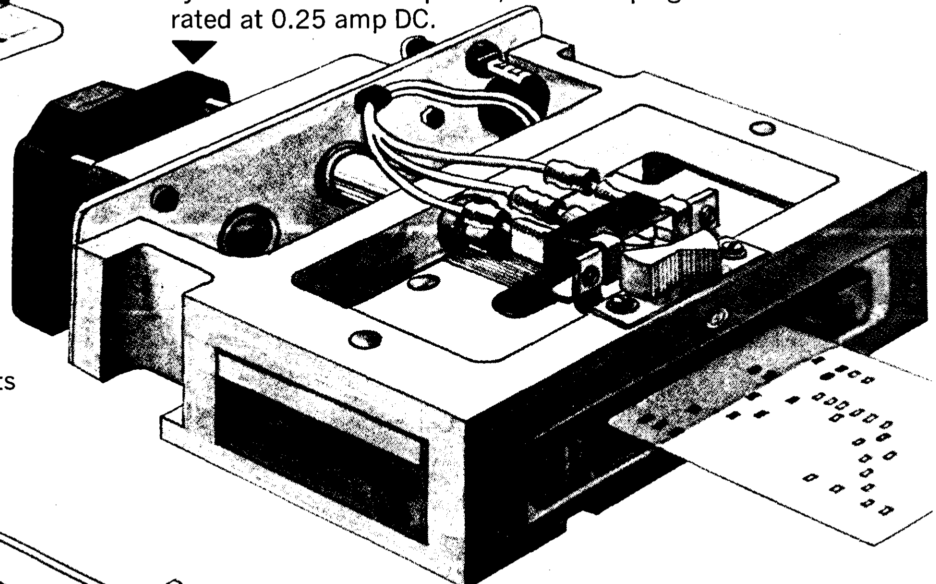
Manual badge reader. Model 361. Cross-matrix or individual outputs. Takes 15-, 20- or 22-column badge up to 0.040″ thick. One-hand operation. Up to 264 switches. Designed for one million cycles.

formation:

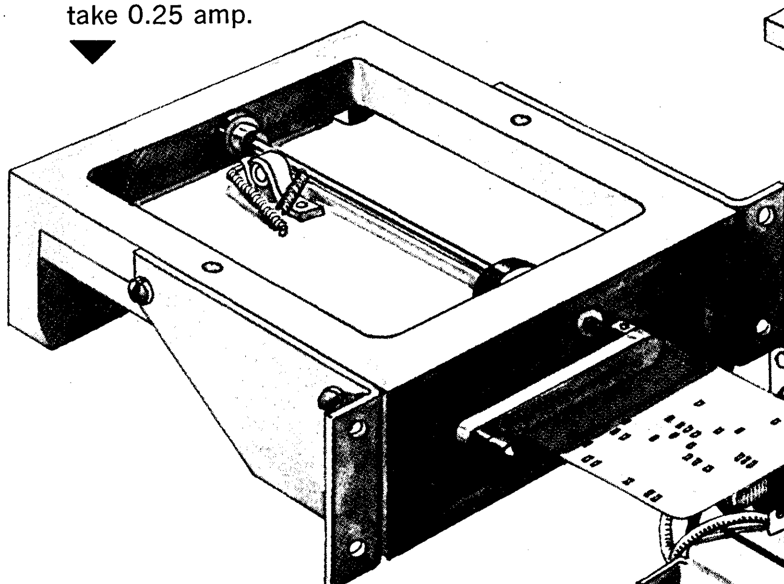


All-weather reader. Designed for outdoor or industrial environments. Suitable for air purge system. Bifurcated contacts — up to 264 cross points. Credit card format up to 12 x 22, matrix or individual. Indicator lamps and card release switch available.

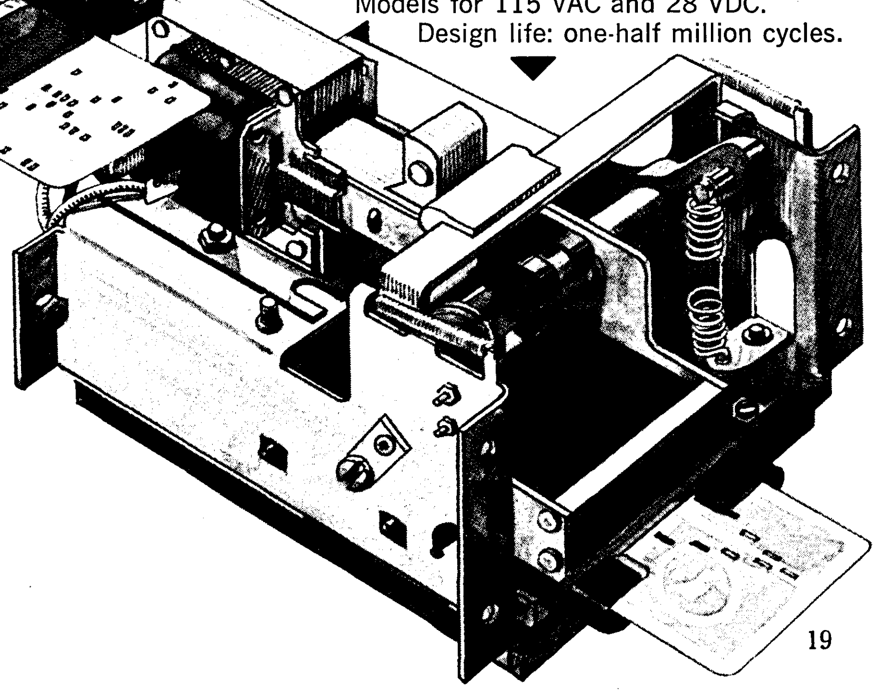
Low-cost industrial reader. Model 2900A. Motor-operated or manual model 2901A. Up to 264 switches, 80-column format. Bussed by row, by half-column or by full column. Gold-plated, double-wiping contacts rated at 0.25 amp DC.



Behind-panel reader. Model 2981A. Industrial full 80-column card reader. Complete alphanumeric coding and 160 six-bit word capability with only 160 diodes. Can be bussed by column, by split column, or by row. Gold-plated contacts take 0.25 amp.



Solenoid badge reader. Model 360. Reads 15-, 20- or 22-column badge — up to 264 switches. Operates similar to time clock. Models for 115 VAC and 28 VDC. Design life: one-half million cycles.



Put your data here . . . for process control, test programming, computer input, machine control, production control, status indication, access limitation, credit validation. The biggest and most versatile card reader family around. For more information, write **AMP INCORPORATED, HARRISBURG, PA. 17105.**

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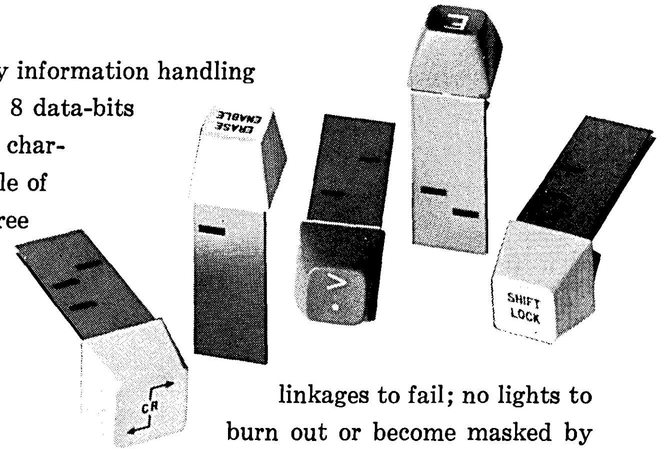
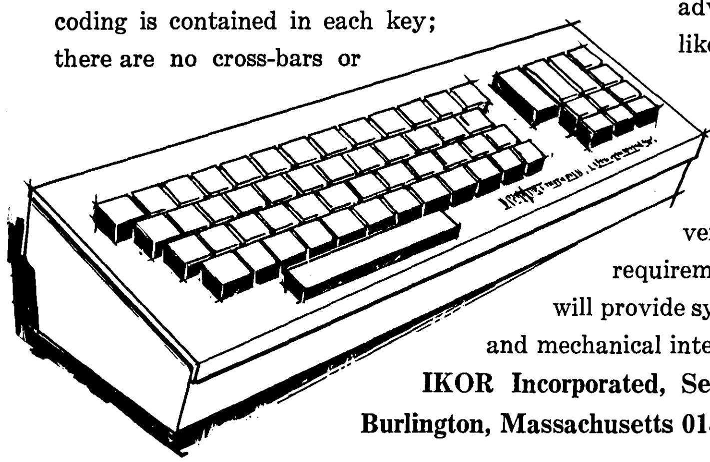
CIRCLE NO. 14 ON INQUIRY CARD

As you like it

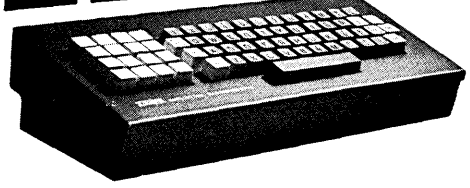


It's that easy to design your own keyboard for any information handling system using the IKOR Universal Keyboard with 8 data-bits available for coding both shifted and/or unshifted characters. A completely different all-electronic principle of operation (patents pending) provides for error-free performance plus the ability to interface with any system. It permits you to specify virtually any keyboard configuration without requiring major modification of the basic design and can be supplied with either serial or parallel output. A minimal maintenance procedure is incorporated into this simple, highly reliable design — coding is contained in each key; there are no cross-bars or linkages to fail; no lights to burn out or become masked by dust or dirt. These are but a few of the design advantages. The IKOR keyboards look like, feel like, and operate like the best electrical typewriters available. The IKOR keyboard functions without error at all speeds. But you can find that out and much more by asking us for a demonstration at your convenience. IKOR will work with you on special requirements, in the development of special designs and will provide systems engineering services to assure electrical and mechanical interfacing to your satisfaction.



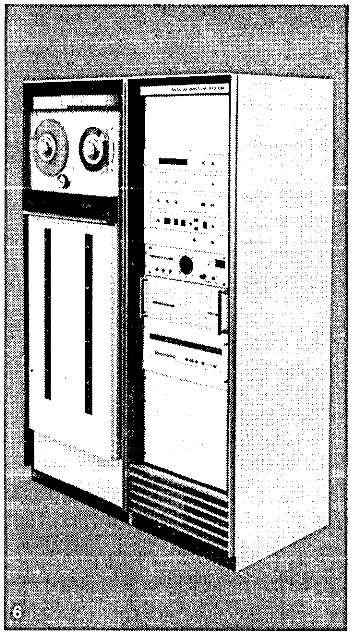
IKOR Incorporated, Second Avenue, Northwest Industrial Park, Burlington, Massachusetts 01803 — Telephone (617) 272-4400

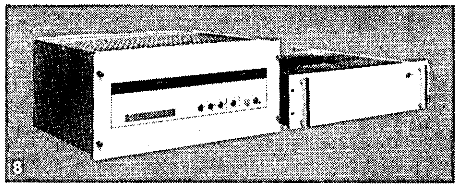
IKOR A BETTER WAY TO COMMUNICATE

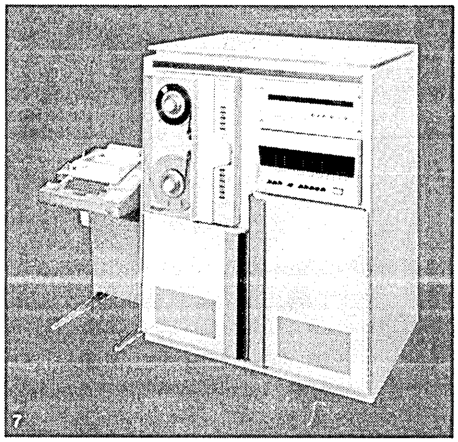


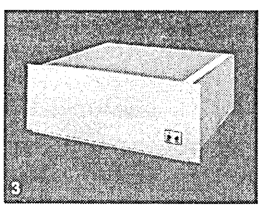
CIRCLE NO. 13 ON INQUIRY CARD

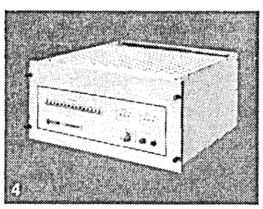
Keep your computer in touch with the world. How fine a touch is up to you... It's your data.

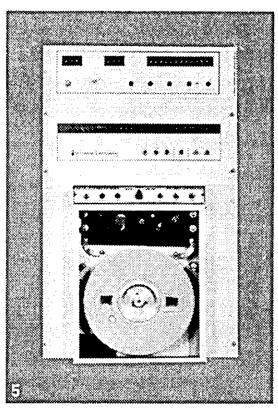


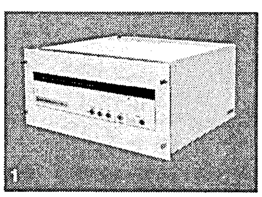


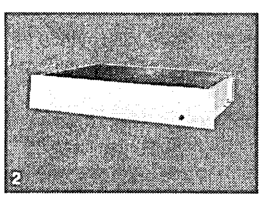












The world is analog. Most computers are digital. Redcor has eight ways to bridge the gap immediately available, from a comparatively simple Analog to Digital Converter to a sophisticated Data Acquisition System.

Each system uses digital monolithic and linear hybrid integrated circuits with all silicon construction in a completely modular format for additional flexibility. After 10 years of "front end" experience, each of these new systems has been designed with room for your future requirements, in addition to the ability to immediately meet your present ones.

1. The 663 Multiplexer/Analog to Digital Converter
This versatile instrument features up to 256 channels single-ended or differential. 15 bit resolution and attendant accuracy. Throughput rates up to 60 KHz. Output coding that matches your digital computer.

2. The 720 Multiplexer/Analog to Digital Converter
The little brother to the 663. Up to 256 channels. Output is 12 bits at a throughput of 20,000 samples per second.

3. The 725 Low-Level Multiplexer/Analog to Digital Converter
Can directly accept signals as low as 5 millivolts full scale on a random or sequential basis. Your computer can dynamically program the range. Output is 12 bits at throughput rates up to 20 KHz.

4. The 645/646 Digital to Analog Converter
Up to 48 digital to analog converters in a single chassis. Input coding to match your digital computer. 15 bit resolution and attendant accuracy. Transfer rates up to 100 KHz.

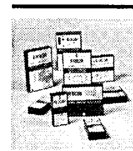
5. The 683 Data Acquisition System (Incremental Magnetic Tape)
Acquires, digitizes and records 32 channels of data at rates up to 500 samples per second. Complete with the 663 multiplexer/A-D converter, magnetic tape formatter and incremental magnetic tape transport.

6. The 684 Data Acquisition System (Hi-speed Magnetic Tape)
All the equipment of the Model 683 above, but designed for hi-speed usage with sample rates up to 60 KHz.

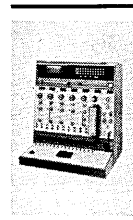
7. The 685 Data Acquisition System (Computer Based)
Acquires, digitizes, and reduces 32 channels of data which is then recorded on tape for input into a large scale data processing system. Complete with the 663 Multiplexer/A-D converter, multiplexer/A-D controller, stored program processor, magnetic tape controller, magnetic tape transport, and a keyboard/reader/punch unit.

8. Computer Interface Systems for the IBM 1130, IBM 1800 and Others
Analog front ends and back ends complete with interface logic for your computer. You choose the computer, Redcor can put it in touch with reality. Contact Redcor or your computer manufacturer. Chances are they'll recommend Redcor.

For detailed specifications, circle the reader service card number.



An Open-Ended Approach to Closed-Loop Modules
You'll find that by using plug-in closed loop modules, it's possible to stay open-minded about system expansion and redesign because modification is possible without all the problems inherent in hard-wired systems.



World's largest selling IC tester now becomes one of the fastest for an extra $2,500.
Now Redcor's low cost IC tester can test 10 devices per second by just adding the new 990101 high speed Automatic Sequencer. Cost: $2,500. The new option has 1000 discrete steps and up to 21 tests per step, moving the effective test rate as high as 210,000 test/sec. Want to know more? Call collect.

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CIRCLE NO. 16 ON INQUIRY CARD

CIRCLE NO. 18 ON INQUIRY CARD→

INDUSTRY NEWS

THERMAL FATIGUE PROBLEMS IN TO-3, TO-66 PACKAGES ELIMINATED — Fairchild Semiconductor, Mountain View, Calif., has completely eliminated thermal fatigue problems associated with TO-3 and TO-66 packages by changing to a copper construction with a matching disc and utilizing a gold-silicon eutectic die-attach, according to an announcement by John Bosch, Marketing Manager of discrete devices.

This packaging development affects Fairchild's entire line of power transistors in the 2-, 5-, and 10-ampere range, which are designed primarily for the military market and for the high grade industrial and computer markets.

The improved products, which include seven families of complementary paired NPN and PNP devices, replace power transistors incorporating solder die-attach technology.

The power transistor series achieves increased reliability through the new copper packages and provides burn-in capabilities as part of standardized testing procedures.

The eutectic die-attach technique relies on a thermally matched disc to give freedom from thermal fatigue. The bonded joint is not affected by repeated temperature stressing, and this is in contrast to solder die attach systems, where the failure rate is 100 per cent predictable through a complete cycle range.

Having a copper base, the new TO-3 and TO-66 are said to offer extremely low thermal resistance and thus, achieve superior heat transfer characteristics over their steel-base counterparts.

Both high reliability packages are constructed with welded-in pin assemblies of Kovar and glass, which result in a matched glass seal to assure hermeticity. With glass and copper completely separated, the packages are able to pass the Radiflow hermeticity tests with leak rates less than 10^{-8} cubic centimeters per second. They also pass all other tests in the environmental test series of Mil Standard 750.

All basic chip types can be adapted to the new packages including Fairchild's 200V NPN switch and discrete emitter devices in the 30W, 50W and 100W transistor series.

STANDARDIZED TRANSISTOR CHIPS SALES PROGRAM INITIATED — Fourteen silicon Annular™ transistor chips have been selected to form the basis of a new program at Motorola Semiconductor Products Inc., Phoenix, Ariz. to supply chips to manufacturers of hybrid devices. The program is organized to provide users engaged in breadboard design or prototype development with completely characterized chips, off-the-shelf availability, and small-quantity pricing.

The selected chips fill a broad range of application categories and include both NPN and PNP devices for general purpose use as well as specialized switching and amplification. Data sheets for each device type are available and fully describe maximum ratings, electrical and physical characteristics and include typical performance curves.

The unencapsulated transistors are gold-backed for ease of die bonding and have aluminum metalization suitable for all standard wire bonding techniques. Transistors of a type intended for both encapsulation and sale as chips are fabricated on the same line. They undergo identical processing up to the point of wafer classification, then wafers selected for sale as chips receive the special handling essential to their intended use.

To accommodate the needs of customers for both small and large quantities, the transistor chips are supplied in two specially designed carriers:

1. The Deka-Pak™ — a 10-chip plastic carrier providing storage and handling protection, easy inventory control, and in-carrier visual-inspection.
2. The k-Pak™ — a 1000 chip plastic carrier providing all the advantages of the Deka-Pak plus one — the carrier actually contains 1020 chips. This version of the baker's dozen provides statistical assurance that 1000 chips per carrier will be within dimensional limits.

Although a wide variety of applications are served by the 14 standard chips, designers occasionally have unusual circuit requirements. On a specially negotiated basis, therefore, virtually any transistor may be purchased in unencapsulated form either as a wafer or individual chips.

Under these special terms the customer may prescribe certain 100% tested electrical specifications within a specific set of ground rules. If need dictates, he may arrange to have other characteristics tested on a sample basis.

Devices purchased on a special basis are packaged in two additional carriers supplementing the Deka-Pak and k-Pak. Wafers, needing a carrier of their own, are shipped between two layers of mylar, sandwiched between two slabs of polyfoam, all in a plastic box. Large volume-users may elect to have their transistor chips packaged in a glass vial, the most economical shipping method.

NEW MIL STANDARD FOR MICROCIRCUITRY TESTING — The Department of Defense has released the first military standard specifically designed for microcircuitry testing.

Test method 1014 of MIL STD 883 describes the procedures to be used in determining fine and gross leaks that would cause electronic device failures when the component IC's were exposed to high humidity and gas contaminated atmospheres.

Of particular interest to manufacturers of electronic equipment and components, the new MIL STD defines two gross leak procedures that specify the use of completely fluorinated liquids.

The joint DOD/NASA standard, prepared by the Air Force's Rome Air Development Center after a year of testing, notes that the use of perfluorinated, rather than partially fluorinated liquids, eliminates the possibility of contamination from moisture and dissolved greases. The completely fluorinated liquids also drain clean leaving no residue and will not damage the markings or other elements of the device structures being tested.

The first gross leak test procedure, for package leaks greater than 10^{-3} atm/cc/sec. uses FC-43 maintained at 125 ±5°C as an immersion fluid to detect severe package leaks. These leaks may be caused by package cracks, solder voids or tilted lids, flange leaks and blow holes in the package or lid sealing materials.

The second procedure, used for leaks greater than 10^{-5} atm/cc/sec uses FC-78 under pressure to determine leaks caused by fine package cracks or pores, minute pinholes in solder, minute weld flange pinholes and leaks around metal to glass seals. This second procedure overlaps into the helium fine leak test range as well as the first test procedure noted for gross leaks.

FC-43 and FC-78 are two of a family of six Inert Fluorochemical Liquids made by 3M Company, St. Paul, Minn. They are clear, nonflammable, colorless, relatively dense and of low viscosity. The major difference between the six lies in their respective boiling points, ranging from 88°F to 345°F. Characteristically, their pour points are quite low, in most cases being well below −100°F. Dielectric strength of the fluids exceeds 35,000 volts per 0.1 inch gap.

VARIAN DATA MACHINES OCCUPIES NEW QUARTERS — Varian Data Machines has recently completed its move into a 100,000 square foot headquarters plant in the Irvine Industrial Park, located next to the Orange County Airport, Irvine, Calif. The new building is a few miles from the previous facility in Newport Beach.

According to Robert Herman, President: "Our new plant has doubled our production facilities, which enables us to meet the large demand for our 620/i and 520/i digital computers at an ever increasing rate. For example, because of the facilities expansion, we have increased production so that we can now offer 30-day delivery on a standard 620/i computer."

RCA BREAKS GROUND FOR NEW COMPUTER EQUIPMENT PLANT — RCA recently broke ground for the construction of a $12 million plant in Marlboro, Mass. for the engineering and production of computer peripheral equipment. The new facility, to be located between Boston and Worcester, is expected to be opened for operations in April, 1969, according to James R. Bradburn, Executive Vice President, RCA Information Systems.

Mr. Bradburn noted that an initial group of engineering and manufacturing personnel are presently occupying a 50,000-square-foot building leased in Framingham, Mass. In addition to designing and producing prototype models of peripheral devices, the facility is being used to recruit and train personnel to staff the permanent operation once it is completed.

Initially, a limited number of different types of electronic data processing devices for RCA's Spectra 70 systems will be assembled at the Marlboro plant. At full operation, a broad range of computer peripheral devices will be designed and manufactured there.

The new plant will be built with an eye toward additional expansion in the early 1970's. "It is expected that future requirements for Information Systems' manufactured products will rise sharply," he said, "particularly in the area of on-line communications systems with emphasis on data collection, display devices, and mass random access storage."

VERSATILE USER - ORIENTED COMPUTERIZED SYSTEM DEMONSTRATED — A versatile computerized system that will assist U.S. military installations in coping with the "information explosion" was recently demonstrated at Andrews Air Force Base, Md., to 500 representatives of the Department of Defense and other federal agencies.

The system, called ADEPT-50 was designed by System Development Corporation (SDC) under a two-year, $3,350,000 contract from the Advanced Research Projects Agency of the Department of Defense.

Essentially it is a user-oriented system of computer programs that greatly increases the flexibility of standard, third generation data processing equipment. It provides military installations with the capability for immediate access to a central computer from different locations at a base or installation at reduced cost.

Working from terminals that are connected to a centrally located computer, the system gives many users complete freedom in manipulating, retrieving, updating and storing data.

A military base commander, for example, by using a terminal to a central computer could get immediate response to questions about the training and readiness of forces or of the logistics of men and materials. At the same time the computer would be available to other base personnel for simulation, computations, document retrieval, personnel records, statistics, and many other management information needs.

Ordinarily these functions would have to be accomplished by several computer systems. But ADEPT-50 provides the flexibility for a single system to serve a variety of facilities, users and applications.

The system is presently being installed in two major DOD installations for tests and evaluation: the National Military Command System Support Center and the U. S. Air Force Command Post.

ADEPT-50 is composed of three separate components:

(1) A large-scale time-sharing control system, or executive, that allows multiple users on a variety of terminals to simultaneously exchange information with the central computer. Each user receives instantaneous response and needs no programming or computer experience. Users can work independently, each having the feeling that he has sole use of the computer, or can work on a problem together sharing the same store of data in the computer.

The executive is equipped with file security measures that prevent unauthorized access to restricted files and prevent accidental damage of data or programs.

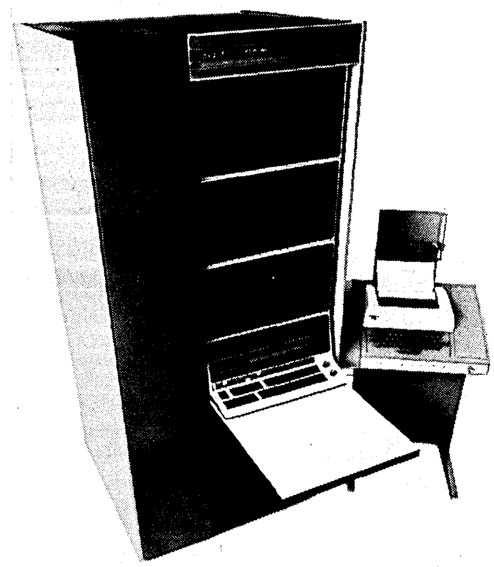
(2) A data management system which allows users, without sophisticated knowledge of programming, to have complete control in manipulating large amounts of data and complex programs in the computer. The user can request selected portions of data be printed on his typewriter-like terminal or other types of output devices for analysis. He can ask questions, change values, perform arithmetic operations and combine or rearrange groups of data. He receives only the information he really needs, at the time he needs it and in the form most usable in answering his question.

(3) A programmers' package that permits construction and debugging of programs. Using a terminal, the programmer can construct, modify, delete or insert programs or parts of programs. Having a direct and immediate link with the computer allows him to "see" his program developing and to experiment with various alternatives.

NEW SOFTWARE FIRM TO SPECIALIZE IN COMPUTER GRAPHICS — A new software firm, Graphtek Corp., has recently been formed in Phoenix, Ariz., and will specialize in the development of computer graphics software for individual customer applications. Graphtek provides the full range of software support from system studies, conceptual design through implementation, documentation and maintenance.

The founders are Dr. Marvin T. Ling, formerly with General Electric's Advanced Systems and Technology Operation, and Mr. Walter F. Cook, previously with General Electric's Large Systems Department in Phoenix.

Specifically, Graphtek Corporation will offer services in such areas as development of generalized basic graphic display systems, computer aided design, systems simulation, remote and/or interactive APT for numerical control, design automation, dynamic management information system, and many others where improved methods of design or problem solving may be accomplished by Man-Machine interactions using CRT display with light pen type of devices.



The world's first medium size computer at a small computer price. $19,900 complete.

Never before has a computer with the power of the PDP-9, the 18-bit word length of the PDP-9, the programmability, the multi-channelling, the expandability of the PDP-9 been available at a price near the price of the new PDP-9/L.

PDP-9/L is a leaner version of the PDP-9, but it's a medium size computer by any standards. Expandable 4K memory, with 1.5 μsec cycle time. Teletype. Standard I-O bus. Eight built-in high-speed data channels. Devices interface directly to the I-O bus by inexpensive FLIP CHIP modules.

And it can be expanded to 32K memory. When you reach 16K, background-foreground programming becomes available. But even the 4K software includes assembler, editor, debugging aids, math package, and utility programs.

If your investigations require a medium size computer, but you simply couldn't afford one before, write us. The new PDP-9/L is designed for you.

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CIRCLE NO. 23 ON INQUIRY CARD

SUPER-SPEED COMPUTERS PUT INTO OPERATION BY NASA — Formal acceptance of two, new super-speed computers — IBM System/360 Model 95s — by NASA's Goddard Space Flight Center has been announced by International Business Machines Corporation.

The two computers are the first and only ones in IBM's Model 90 series equipped with ultra-high-speed thin-film memories. Over a million characters (bytes) of information are stored in each on magnetic "spots" four millionths of an inch thick.

With an access time of 67 ns, these are the fastest, large-scale memories in user operation.

Both of NASA's Model 95s are handling space exploration problems which require unusually high computation speeds. The Model 95s are capable of computing 14-digit multiplications at a rate of over 330-million in a minute.

One Model 95 serves as the primary data processing facility for the Center's Tracking and Data Systems Directorate. It provides additional computing support to the Project, Technology and Systems Reliability Directorates.

The second Model 95 is being used by astro-physicists at NASA to create massive mathematical models of the universe. The boost in computing capability is enabling them to simulate the evolution of galaxies, stars and planets to a degree never before possible.

The speed of the thin-film memories gives the Model 95s a performance edge — up to twice as fast on certain problems — over the Model 91 which was the first super-speed computer in the Model 90 series. IBM's initial Model 91 was placed in operation earlier this year by NASA-Goddard.

These memory units, developed and manufactured by IBM's Component's Division facility at Burlington, Vermont, utilize advanced array and circuit technology to achieve high speed. The magnetic storage element consists of a very thin nickle-iron-cobalt film, which is vacuum deposited on a copper plate. These storage elements are driven and sensed by means of thin copper strip lines. New circuit and packaging techniques are used with the unique memory array to achieve the fast — 120 ns — cycle time.

Each Model 95 is equipped with 16 thin-film memory units. The data width, at which information is transferred to the processor, is eight bytes.

In addition to the thin-film memory, the Model 95 has a 4-million character core memory. The core memory has a cycle time of 750 ns. The memory combination gives the Model 95 a 5-million-plus character main storage system — more than twice the storage capacity of the Model 91.

The Model 95 has auxiliary storage of about one billion alphanumeric characters. It consists of disk, drum and data cell devices. With five high-speed printers, it can generate up to 5500 lines of information a minute.

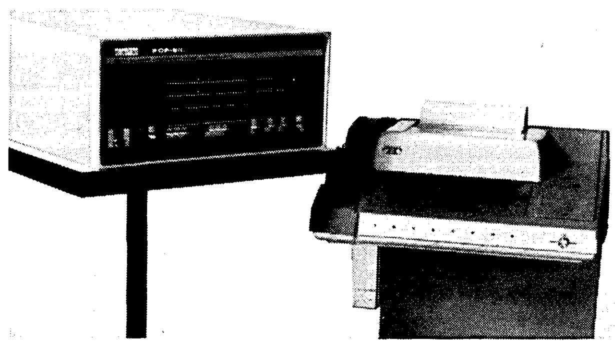
The Model 90 series was initiated by IBM as a program to advance the state of computer art and to serve a limited number of sophisticated data processing users. With its program objectives met and all deliveries now scheduled over the next 12 months, IBM has stopped accepting orders on the series.

MAJOR BREAKTHROUGH IN SOFTWARE DEVELOPMENT — Datamation Services, Inc., New York, N.Y., has developed a 1401/360 Simulator which marks a major breakthrough in software development, according to a recent announcement by, Thomas T. Connors, president. This powerful and versatile programming tool makes it possible to run on an IBM System/360 model 40 and up, a program originally written for an IBM 1401 or 1460 computer.

"This is a true load-and-run simulator, and under a normal input-output mix can equal or better the original 1401 speeds. Through this advancement Datamation has now developed a simulator to operate with RCA Spectra 70 equipment," Connors said.

The SIM 1401 can run in a multitasking environment. The program mix may include 360 as well as other 1401 programs under these conditions. It operates with the following supervisors: OS (Operating System), DOS (Disk Operating System), and TOS (Tape Operating System), etc.

The simulator makes possible an elimination of cost in hardware emulation on 360/30, hardward based simulation on 360/40 and in some cases will enable the user to eliminate the cost of complete 360 and 1400 systems, presently maintained only for 1401 compatibility. Datamation is prepared to market SIM 1401's to other computer users now that field testing has been successfully completed.



a report on the

OPTIMAL SYSTEMS PLANNING SYMPOSIUM

NEW METHODOLOGY FOR STRUCTURING LARGE SYSTEMS EXPLORED AT SYMPOSIUM — Scientists from both sides of the iron curtain contrasted new methods for optimizing large systems at the Optimal Systems Planning Symposium sponsored by the International Federation of Automatic Control in Cleveland, Ohio on June 22, 1968. Under the chairmanship of G. L. Hollander, President and Technical Director of Hollander Associates in Fullerton, Calif. (and Consulting Editor, Computer Design), delegates from Bulgaria, Czechoslovakia, California, England, Mexico and the U.S.S.R. disclosed new approaches by which large economic, industrial and possibly military systems can be designed to produce the most effective results at the least cost. Not unexpectedly, the representatives from the eastern countries were concerned with planning of state economic functions and industrial complexes, while the representatives from the western countries were more concerned about maximizing the profit of industrial and educational undertakings.

In his opening remarks, Mr. Hollander pointed out the similarity of the methods irrespective of their ultimate application. He cited examples from his own organization in which methods developed for military, industrial and commercial applications could be transferred with little change. In fact, unique research of his firm in another field will prove to be of greatest benefit in commercial applications.

Dr. Jiri Benes, from the Institute for Information Theory and Automation, Praha, Czechoslovakia, in his paper entitled, "Probabilistic Planning of the Spread of Means in an Interconnected System", developed models whereby he could determine the best way of introducing catalysts into production processes for large interconnected systems. The paper by Dr. D. W. Gillings, of Imperial Chemical Industries in Reading, England, "Evaluation of Profitability of Industrial Production Supported by R & D Activity", develops a model for the seeding of research funds in the profit-building of a large chemical complex. Chairman Hollander pointed out the similarity of characteristics, if one visualized the stimulating research funds as a catalyst in accordance with the paper presented by Dr. Benes.

Mr. A. E. Eulberg, of Gulf General Atomic, Inc., of San Diego, California, in his paper, "Soft Decision Engineering", contrasts how some business decisions must be made with less than complete information, and assesses the risk and cost related to decision-making with incomplete information. I. Popchev, of the Institute of Engineering Cybernetics of the Bulgarian Academy of Sciences in Sofia, Bulgaria, in his paper, "On The Behavior and Evaluation of the Efficiency of a Class of Large Scale Systems," formulated methodical relationships for hierarchical systems. Paul Alper, of the National Polytechnic Institute in Mexico City, Mexico, applied his decision-making and optimization process to the educational policies for a state. Probably the most ambitious paper entitled, "To the Question of Functioning of the Economy of a Union Republic in the All-Union System of Planning and Regulation", by A. N. Pirmukmamedov, of the Institute of Cybernetics of Uzbek, U.S.S.R., attempts to address the planning of an entire economic unit, namely one of the states of the U.S.S.R.

In his closing comments, Chairman Hollander reiterated the similarity of objectives despite the different applications. He urged not only the 250 scientists attending the meeting, but other system planners and executive decision-makers, use the ideas from these papers for their own applications.

The Optimal Systems Planning meeting is sponsored by the American Automatic Control Council (AACC), the Systems Science and Cybernetics Group of the Institute of Electrical and Electronics Engineers (IEEE), and the Systems Engineering Committee of the International Federation of Automatic Control (IFAC). Although attended by several hundred scientists from all over the world who were interested in planning large communication, transportation, engineering and industrial systems, a special evening session of invited talks relating economic and organizational systems under the chairmanship of M. D. Mesarovic of Case Western Reserve University received a paper from V. A. Trapeznikov, Academician of the Institute of Automatics and Telemechanics, in Moscow on "State Planning of Industry". His views were contrasted by three papers by United States authors from M.I.T., Case Western Reserve University, and I.B.M.

Proceedings containing all papers formally published at the meeting can be obtained from the headquarters of the Institute of Electrical and Electronics Engineers, 345 East 47th Street, New York, New York.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DEVELOPMENTS

Glass-Epoxy Laminate Eliminates Measling

A copper clad laminate that will not measle, blister or warp has been developed by John Harrington and Smith A. Gauss, engineers at the Industrial Micarta Division of Westinghouse Electric Corporation, Hampton, S.C. Due to its moisture-resistant properties, the glass-epoxy laminate, designated Micarta 65M27 eliminates "measling" in the normal manufacture of printed circuits.

Measling is the occurrence of "measles" or minute opaque spots, frequently caused by moisture absorption through high humidity conditions during storage or distribution of the laminate, from the time it is manufactured to its ultimate use as a printed circuit. Considered a defect by many end users, measling is a factor in rejected material, particularly by the military.

Moisture absorption by conventional G-10 copper clad laminates has long been a problem. At the latest Electrical Insulation Conference, a major resin producer urged laminate manufacturers to help solve the problem and give some consistency to processing.

The glass-epoxy laminate is designed for use in airborne computer circuits where weight and space savings are important, and in electronic circuits that must support heavy components on a small area. In tests conducted by both Westinghouse and independent companies, the 65M27 laminate proved to be far more resistant to measling, blistering and delamination than conventional G-10 laminates, according to the engineers.

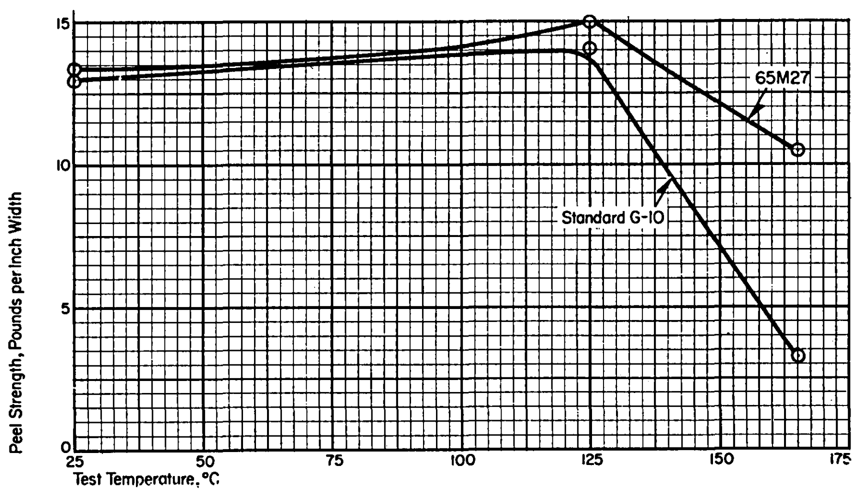
To simulate high humidity conditions, Harrington and Gauss took 5-inch square samples of 1/16-inch thickness with 2-ounce copper on one side; and exposed them to 90 per cent relative humidity at 95°F. Test specimens were removed daily from the humidity cabinet and floated on molten solder at 500°F. for one minute or until the first measle appeared. The Micarta 65M27 specimens showed no effects after a full month, while conventional G-10 copper clads began to measle at 4 days and showed increasingly worse signs of crazing, blistering and delamination.

In standard industry test specifications, smaller samples are called for. But Harrington and Gauss reasoned that the 5-inch square samples gave better tests for measling and warpage.

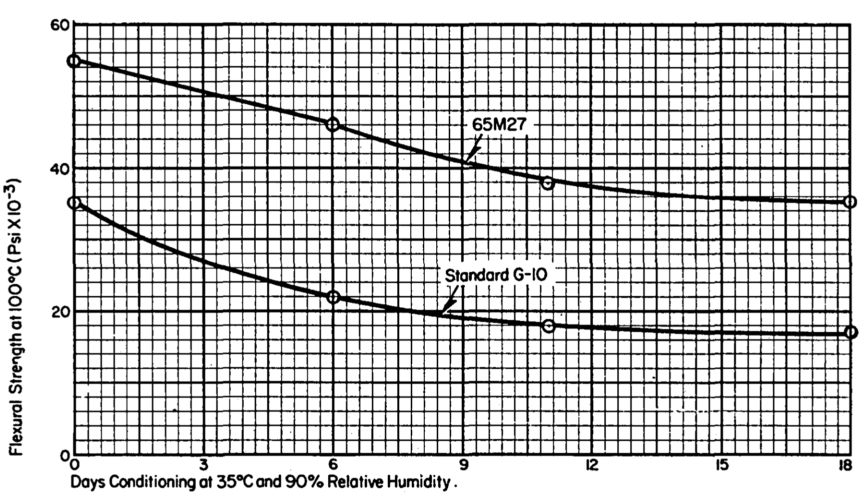
Under independent testing, the glass-epoxy laminate not only withstood the solder bath, but it was exposed to Hydro Squeegee for one minute at 450°F.; placed in a humidity chamber for 160 hours; fused for 45 seconds at 475°F.; and baked for 30 minutes at 250°F. The new laminate showed no effects after the five-stage tests, while conventional G-10 laminates warped, measled or delaminated at various stages.

In drilling, routing, shearing and punching tests, the 65M27 laminate was found to be as good as, if not

(continued on Page 36)



Flexural strength of Westinghouse's Micarta 65M27, improved copper laminate is graphically compared with the Standard G-10 copper clad. After 18 days of conditioning at 35°C. and 90 per cent relative humidity, it is as strong as G-10 at the beginning of the test.



This chart compares peel strength of Micarta 65M27 with Standard G-10 at temperatures ranging from 25 to 175°C.

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Intermediate and senior openings exist for engineers to work in advanced development of mass storage devices including magnetic drums and discs. Openings exist in all areas of mass memory storage development including magnetic recording techniques, read-write circuit design, electro-mechanical servo systems, magnetic head design, packaging and tests. Requirements are 2-5 years' experience in magnetic recording devices or related areas with BS in EE or physics.

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DEVELOPMENTS

(continued from Page 34)

better than, conventional G-10 copper clads.

Manufactured under "clean room" conditions, the laminate is produced by a new epoxy-resin formulation which, the engineers said, give it high flexural strength and high flexural modulus, even under elevated temperature and high humidity conditions. The formulation provides the 65M27 laminate with twice the hot flexural strength of conventional G-10 laminates of the same thickness, when subjected to high humidity and temperature. Other tests showed the material to have as much as three times the peel strength of conventional G-10's at 165°C. (329°F.), an important feature in high reliability printed circuit boards.

Experimental Optical Store For Computers

As part of the Advanced Computer Technique Project sponsored by Great Britain's Ministry of Technology, International Computers and Tabulators Ltd., Putney, G.B. is investigating the practicability of developing a special-purpose mass-information optical store for computers. The store has been designed to provide an inexpensive means of holding permanent information to which access is required rapidly, but which changes infrequently.

Interest in such stores arises from the fact that the performance of a modern computer depends as much upon its software as its hardware. The operations of multiprogramming and multiaccess computers are controlled by supervisory programs that are permanently held within the computer.

Currently supervisory programs and other fixed operating information required for immediate use have to be held in a computer's core store. Core stores are expensive and therefore, usually only limited data storage capacity is available for such information. Furthermore, core stores possess qualities that are not needed for storing fixed information. For instance, information can be written into a core store as rapidly as it can be read. Fixed information need only be retrieved rapidly — writing speed is not critical. Hence the search to find a new technique of storing fixed information en masse which dispenses with some of the expensive facilities of conventional computer stores.

A secondary though no less important reason for seeking to evolve a new type of store for fixed information is the desirability of having on-call other software like compilers that translate programs written in different languages into machine code instructions, and formalised information processing procedures such as data sorting and editing routines. At present this software is loaded into a computer, often on magnetic tape, the relevant sections being transferred to the core store when required, but it would be of considerable operational benefit if this software were immediately available within the machine at all times.

The general requirement, therefore, is for a means of storing vast quantities of permanent or fixed information at low cost. The rate at which fixed information can be recorded in the store is not important, but access speed is. Moreover capability must be provided for retrieving fixed information at random and as rapidly as with a conventional computer store — that is within 2 to 3 microseconds.

Photographic methods are attractive because information stored on plate or film can be readily and accurately reproduced by proven, simple, cheap and reliable techniques. To achieve the necessary speed of response obviously the data must be handled electronically, and the current research at I.C.T. into stores for fixed information seeks to combine these features in an optical store.

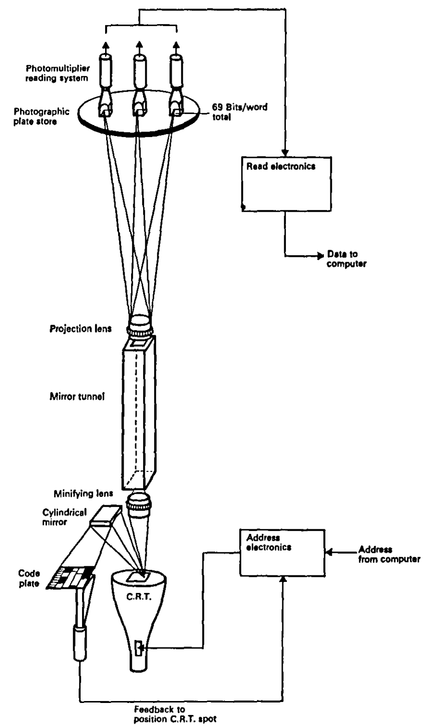

Fig. 1 Block diagram of the optical fixed store.

The experimental optical store is being built at I.C.T.'s Stevenage Advanced R & D Laboratory. The research model being constructed to evaluate the idea can accommodate 65,000 68-bit words. It is envisaged that 50 bits would be used for data with up to 18 available, if necessary, for use as check bits. Access time to a word is expected to be 2 microseconds — all 68 bits being read in parallel.

The optical store Fig. 1 comprises a cathode ray tube, a minifying lens, a mirror tunnel, a projection lens, the photographic plate holding the information and a photo-multiplier assembly.

Binary data are stored as a pattern of black and white areas on a circular glass photographic plate 10 in. in diameter.

(continued on Page 38)

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DEVELOPMENTS

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OPTICAL STORE GEOMETRY

A spot of light appearing on the screen of the cathode ray tube is focussed by the minifying lens in the plane of the aperture of the mirror tunnel. This tunnel consists of four mirrors arranged in the form of a square with their reflecting surfaces inwards. The tunnel is 14 in. long with sides 0.7 in. wide. The purpose of the tunnel is to produce a pattern of light spots from the one spot generated by the cathode ray tube.

The mirror tunnel acts as a kaleidoscope, the internal reflections of the single spot within the tunnel producing a multiple array at its exit. This image is then focussed on to a photographic plate by the projection lens.

Within the 10 in. diameter target area of the experimental store a pattern of 69 light spots is generated from the single spot of the cathode ray tube. If the position of the spot on the screen of the tube is changed the positions of all the spots on the photographic plate also change, with alternate spots moving in the same direction but adjacent spots moving in opposite directions. In effect the area covered by the screen of the cathode ray tube is reproduced as 69 one-inch squares on the photographic plate.

One of the 69 one-inch squares is used for control purposes, leaving 68 available for data.

Provision has been made for the spot on the CRT screen to be projected at 256 positions in the x axis and at 256 positions along the y axis. Thus the spot can be positioned at any one of 65,536 (256 x 256) discrete positions on the face of the tube. Similarly the spots projected in each of the 69 inch-squares on the photographic plate can occupy any of 65,536 discrete positions within each square.

STORE OPERATION

Data are read from the store in the following manner. Assume that a photographic plate containing fixed data is fitted in the store. The data will be recorded as clear or opaque areas in each of the 65,000 or so possible positions in each of the 69 one-inch squares on the plate. Behind each one-inch square area is a photomultiplier. To read a specific word, a spot of light is positioned on the screen of the CRT at the relevant position, say $x = \pm 10$, $y = \pm 10$. As a result 69 spots of light will be projected at $x = \pm 10$, $y = \pm 10$ in all 69 one-inch squares on the photographic plate. Opposite signs apply to adjacent squares. Where these spots fall on clear areas in the photographic emulsion the light will be transmitted through the plate and be detected by the photomultiplier situated behind that particular one-inch square. As a result, the photomultiplier will issue a signal. Conversely, where the spot of light falls on an opaque area, the corresponding photomultiplier will issue no signal. Hence, the projected light spots interrogate a specific location in all 69 areas of the photographic plate simultaneously and the signals from all 69 photomultipliers will be converted into the 69 bits of the complete word stored at that location. All 69 bits (68 data bits plus 1 control bit) will be available simultaneously.

One of the problems that had to be solved to enable the machine to work at all was to be able to position the interrogating spot on the screen of the CRT at an accurate location (or address) relative to the remainder of the optical system. This is achieved by means of a digital servo system. A cylindrical mirror aligned along one axis reflects light from the CRT spot onto a digitally coded scale. In this manner the exact position of the spot, expressed digitally, along one axis is obtained. A similar optical system is used to detect the position of the spot along the other axis. The actual co-ordinate position of the spot is then compared with the position commanded, and control voltages applied to the CRT to move the spot to the correct position and maintain it there.

Besides conferring precision, this control system enables any cathode ray tube of the correct type to be fitted to the optical store since the accuracy of spot positioning is not a function of the characteristics of the particular tube.

To produce a master photographic plate for use in the optical store the technique is akin to reading except a special shutter mechanism is required. This shutter will expose only one-inch square of the plate at a time. To prepare a plate the shutter is set to expose the required one-inch square and the spot on the cathode ray tube is controlled to dwell where binary O is to be recorded at each of the 65,000 discrete positions on the screen. In such positions the film, when developed, will be opaque. When binary 1 is to be recorded the position is left unexposed and the corresponding area on the film after development will be transparent.

The entire data recording sequence will be controlled by computer and to record bits in all 65,000 positions in all 69 one-inch squares is estimated to take about one hour. Once a master photographic plate has been made however duplicate plates can be produced in quantity quite simply by normal photographic methods.

The store has been designed so that the photographic plates can be quickly and easily changed. In fact one of the major design requirements is that the photographic data plates be interchangeable between stores.

To avoid interference with correct operation due to temperature changes and vibration the optical elements of the store are fixed in a tetrahedral framework of struts which is supported on three low-frequency anti-vibration mountings. To prevent optical distortion, the mirror tunnel is held vertically with the cathode ray tube below and the photographic data plate above.

commentary

Comments and opinions on topics of current interest to digital design engineering personnel. A monthly column organized and prepared under the direction of **T. PAUL BOTHWELL, Contributing Editor.**

Data Format Considerations in Head-Per-Track Mass Memories

THOMAS M. DUNDON

Head-per-track disk and drum mass memories allow the system designer unusual freedom in choosing his data format. Other secondary storage devices (e.g., magnetic tape and moving-head disks) tend to have data formats determined by industry conventions which allow inter-systems compatibility. These devices also tend to require the computer to locate data by *content,* rather than *address.* Head-per-track devices, on the other hand, locate data in *space* (head address) and *time* (clock count or sector mark).

The format freedom offered by head-per-track mass memories permits the designer to:

1. Trade off hardware cost against system performance.
2. Tailor data format to the application.

The following discussion considers some specific cost/performance tradeoffs and some useful data formats obtainable with head-per-track devices.

We assume that the designer has already determined total storage capacity, bit density, track length, and rotation speed, based on his needs and the current state of the art. Within these constraints, the following basic parameters may still be varied independently:

1. Number of tracks which transfer data simultaneously.
2. Amount of data addressed per "location" or block.
3. Nature and size of gaps between blocks of data.
4. Sequence in which data is transferred to and from the memory.

The author of this month's CD Commentary, Mr. Thomas M. Dundon, is a Section Manager in the I/O Department at Honeywell, Inc., Computer Control Division. He is responsible for selecting and interfacing peripheral equipment for CCD's line of computers.

Track Organization

Single vs. parallel track transfer is depicted in Fig. 1. Parallel track transfer trades hardware simplicity for high data transfer rate. A data read/write channel must be included for each simultaneously active track. The computer interface must be capable of handling

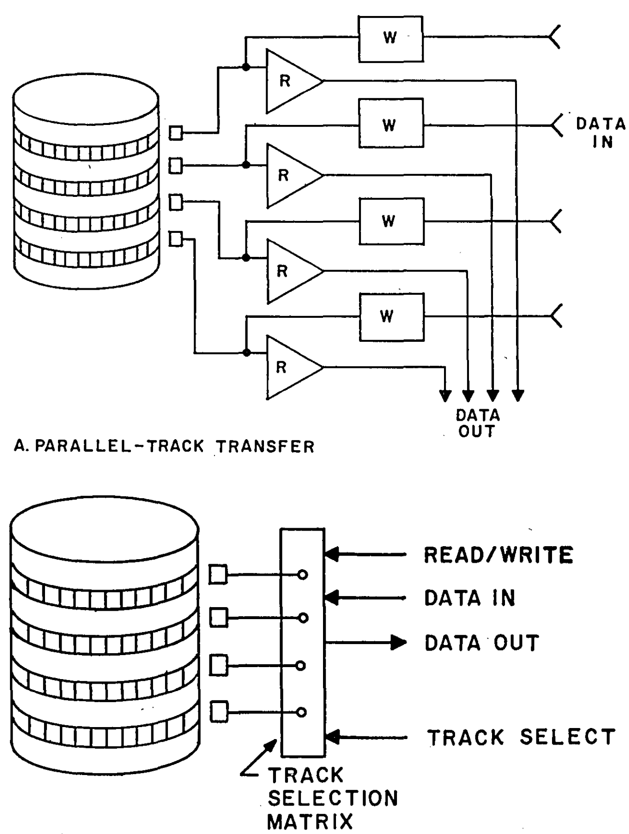

Fig. 1 Mass memory track transfer schemes.

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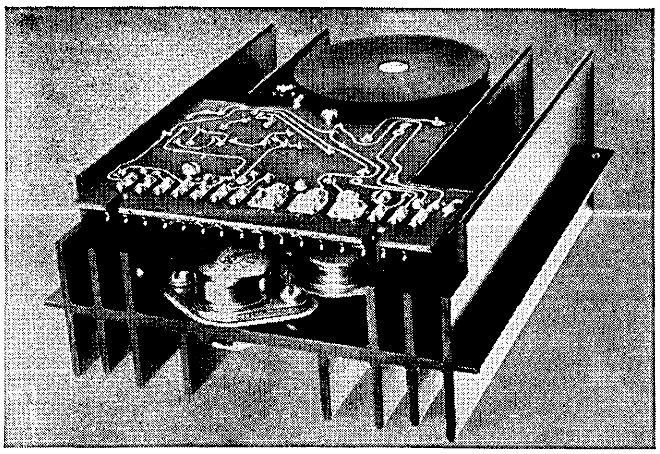

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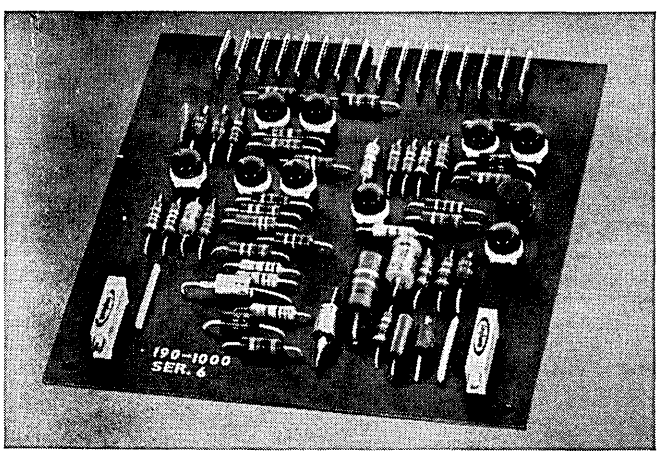

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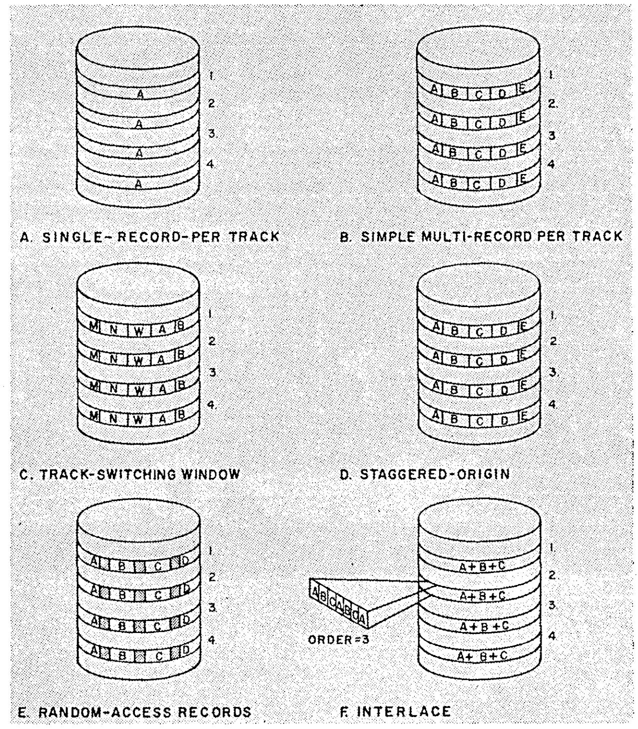

Fig. 2 Mass memory data formats.

N times the bit rate of a single track, where N = number of simultaneous tracks transferred. N is usually chosen to be a byte or a mainframe word length. Parallel track organization is mainly used in time shared system "paging" applications. A separate core memory port is usually dedicated to the mass memory.

Head-per-track memories are addressed by track number and distance along the track from a defined "origin" or "index" location. It is common practice to allow addressing of individual tracks (or track groups, in the case of parallel transfer organization), but the resolution of access within a given track may vary from a single bit to the entire track (Fig. 2 A & B). The designer must consider the following factors in choosing the minimum accessible data "block" on a track:

1. What is the smallest data field which will be commonly manipulated?
2. How much core space can he afford for buffering (and double-buffering) mass memory transfers?
3. What is he willing to pay for high-resolution data access?

Often, a card image, source text line, or object block is used as the benchmark for minimum block size. As block size decreases, core buffer size decreases, but address register and counter size increase. If only one block may be accessed per device revolution, the mass memory will be inefficient if block size is low. It is usually a mistake to treat the mass memory as a byte or word-addressable core memory with large average access time. The best data block choice is usually the largest block which, in practice, does not result in a large percentage of unfilled space within blocks.

System Efficiency

Overall system efficiency is not always maximized by placing data blocks (or *records*) around the track in an unbroken chain, all beginning at the system index mark. Because latency time is large compared to the data transfer period, it is often advantageous to invest hardware cost or a small amount of storage space to minimize latency. Three possible schemes are shown in Fig. 2C, D and E. A "window", or index gap is used in Fig. 2C to allow the computer system time to decide which track will be transferred next and to accomplish re-initialization of the memory. The window can be as small as 1-5% of track length. Often, track capacity is determined by a convenient power-of-two number of records. When this determination has been made, a 1-5% increase in bit density will yield the "window". In Fig. 2D, the first record in each track is advanced with respect to the previous track. This technique avoids loss of storage area, but incurrs higher cost for addressing hardware and fails when addressing is retrograde. In Fig. 2E, a gap is left between every record on a track so that the next record on *any* track is available upon completion of a transfer of a given record. This technique is wasteful of storage space, but is often used in time-sharing applications in which "random" access is paramount.

Latency can sometimes be minimized by a software technique that does not involve a "window". The program senses current head location along the track by interrogating the record address counter. The program, then, rearranges the queue of pending memory transactions so that they start at the next addressable record. Latency is, thus, reduced by a large factor, but only in applications which are characterized by large sequential record queues.

Interlacing

A final parameter, interlacing, is open to the system designer. Interlacing involves an ordered stringing of related data elements along a track. The usual goal is to slow down data transfer rate to match computer characteristics without employing expensive hardware buffers. Fig. 2F shows interlacing results in a series of sub-tracks, or "rings", in which each element is separated by a member of each of the other sub-tracks on the track. The "order" of the interlace refers to the number of sub-tracks per track and is a measure of the buffering time chosen. For example, an interlace of order 3 reduces the transfer rate of a data element (bit, byte, word) by a factor of three. The number of data elements on a sub-track is also one-third of the number on the entire track. Sub-tracks may be further divided into sectors, as described above. Interlacing usually incurs a certain amount of wasted track space in isolating sub-tracks from each other. For this reason, it is rarely implemented on a bit level. Byte and word interlacing are most common. Interlacing allows the designer to tailor transfer rate to his computer at low hardware cost.

In summary, head-per-track mass memories differ fundamentally from content-addressable secondary storage media. The system designer can exploit these differences to obtain the highest performance/cost ratio for his application.

SETTING CHARACTERISTICS FOR FOURTH GENERATION SYSTEMS COMPUTER

This is the first in a series of three articles which contain reasoned extrapolation concerning probable characteristics of hardware and software and the use of large scale integration (LSI) in fourth generation computer systems. To predict future developments in the computer industry is to speculate — to theorize on the basis of observable trends and anticipated needs. In these articles the authors confidently predict changes that will occur.

Computers of prior generations emphasized computation. Fourth generation computers, as envisioned in this series, will emphasize communication and control. The intent of the authors is to suggest a solution to a fundamental EDP problem: How can computers and applications be integrated within a total communication and control system?

Part I is primarily a discussion of fourth generation computer system characteristics. Major topics include family planning, design approach, and functional organization within a computing environment. Use of read only memories, associative memories, and programmable logic arrays to replace operating system and control programs and to establish logical system organization is proposed and analyzed.

Unsupported statements that "executive programs will be simplified by LSI" are considered by the authors to be irresponsible and unprofessional. Proponents of such oracles first discuss LSI technology and then postulate its impact outward on user software. In the second article to be published in the September issue, the authors will begin by considering the user and his software and reflect its impact inward on the hardware. Hardware features that will lead to new approaches to software design will be proposed. Also included will be a reasoned extrapolation of how hardware designers can offer solutions to many EDP problems.

The third article will appear in the October issue and will cover a discussion of the impact of LSI on fourth generation computer planning from the viewpoints of both the manufacturer and the user. Materials and fabrication techniques for LSI designs are in various phases of exploratory research, development, or pilot production. Therefore, to formulate exact plans for LSI activities is difficult, but the authors will offer definitive guidelines in this area.

Part 1 Hardware

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EVOLUTION

First generation computer systems were developed primarily for computational purposes. The concept of storing a program to control the operations of a computer and the ability of a computer to cycle repetitively through a sequence of instructions pointed toward use of the computer for computational purposes. Later, the marketability of machines that could be programmed to perform EAM operations was recognized. Thus, EDP was born.

To provide modularity and flexibility in general purpose machines, computer designers delegated obvious hardware functions to software (e.g., floating point arithmetic, interrupt features, and several multiplexing and control functions). A primary design objective was to provide a computer which the user could specialize for his particular application. Utility, service, and other software routines were developed to perform common functions, but these routines were designed to make a general purpose computer fit a particular area or application. The same application was modified or reprogrammed as details within the area or application changed.

Computer professionals are slowly viewing internal organizations of computers and/or software in perspective and realizing that a computer is a general purpose device primarily for ease of manufacturability. Furthermore, a computer is only one of many system components in a user's environment. The typical user's lack of ability to tailor a general purpose machine to a particular application is a major factor inhibiting extensive use of computers. Even if funds and required capabilities are available, the user may not wish to reinvent the wheel that constitutes his application. Valid questions arise when considering specialized functions such as data collection systems and are apt to be widely prevalent when considering more mundane areas such as payroll, accounts receivable, and inventory control. Should the small user acquire a special purpose device to perform many of the mundane activities and subscribe to a time sharing system to process complex data processing applications?

Many persons learned to program with little understanding of computers or of applications to which computers could or should be applied. The development of large data management systems and/or operating systems resulted primarily from a lack of understanding of the nature of these applications. Operating system designers tried to blend hardware, software, and applications. Currently, the application area is exploding and will become dominant.

Operating systems were introduced to improve hardware utilization and to increase system throughput. Programmer time was deemed less expensive than machine time, and effort was expended to separate the user from the machine. Maximizing throughput, however, often impaired or limited the quality of services provided. To achieve flexibility in general purpose computers, software designers introduced programming complexities not readily understood by most programmers. Operating system facilities were developed to simplify programming, but user preparation of executable programs became increasingly difficult. A primary example of such increased difficulty is the task of debugging a program in a multiprogramming environment.

The nature of computing has changed significantly in the past decade, but the primary objective (maximizing throughput) of operating system designers has not changed accordingly. Computers replaced EAM operations and were initially used to generate reports. The user analyzed the data and performed a function accordingly. Today report generation should be regarded as an available option. The challenge of computing is not to program a computer to generate a report that enables a person to perform a function; rather, the challenge is to design and program a computer so that it performs the function — and thereby directly assists in the operation of business or industry.

During the past 12 to 15 years, users developed operating systems to solve particular operating problems. Initial efforts were directed toward reduction or elimination of idle time resulting from human intervention during computer operation. In fact, operator time often exceeded processing time. Operator intervention to select and load the next program, to mount data files, to check labels, to collect output, and to log both a completed program and a program being initialized, was regarded as undesirable. Special control and service programs were developed to perform many of these functions. Today an operator communicates primarily with control programs, and his efforts are minimized. Control and service programs perform a vast majority of input/output operations and recovery procedures.

What has the user seen with regard to hardware? First generation hardware was characterized by vacuum tubes, second generation by transistors, and third generation by integrated circuits. Of greater importance to the user, however, were the reduction in cost of main memory (from approximately one dollar per bit to approximately five cents per bit) and the increase in reliability of the machine. Major advances were made in the reliability of both logic and memory with the change from vacuum tubes to transistors. More memory available at reduced cost led to the development of more and better software and an attendant increase in the complexity of applications to which computers could be applied. As main memories became larger, more programs could be resident in memory. Throughput was increased by reducing time loss due to execution of program load and unload routines and relocation functions.

Today's user is interested in total system performance and in the total cost of the system rather than in only the cost of the central processing (CP) unit (currently 15-20% of the hardware cost). The user desires a variety of complex applications. He wants to tell a computer what to do — not how to do it. The user is not as impressed by advanced hardware as he is by efficient application. Designing total systems which not only are based upon reliable, efficient hardware but also can be easily programmed is a practical objective.

CHARACTERISTICS

The major design criteria of fourth generation computers will be optimal use of available communication interfaces. Intrasystem and intersystem communication interfaces are required for both hardware and software. The system will be classified as a communication and control system and will be capable of widely diversified processor applications.

Fourth generation systems will be controlled primarily by data rather than by programs as were previous machines; i.e., overall system control will be established primarily by input rather than by stored information. Development of this characteristic is dependent upon submission of information in real time. Fourth generation systems will accept inputs as they are made available and process those inputs within the constraints imposed by desired response times. Feedback is a key consideration. The interrelationships between data (communication bits) and programs (information bits) must be carefully defined.

Hardware will govern communication and control procedures; use of control programs will be substantially reduced or eliminated. Focalizing system design by application of communication networks will eliminate much of the need for software and facilitate system control. Again, consideration of both intersystem and intrasystem data flow is important. When such techniques are applied, control program requirements will be minimized.

The system will be readily expandable. Hardware and software will be modular in design. Computing power will be modified without redesign of the system. A variable instruction set is not implied. However, nested subsets of hardware will be available to complement nested subsets of software. In fact, this nesting of software is currently practiced. The user's software commonly includes both action macros and system macros. System macros commonly contain nested macros which perform communication functions for specified terminal devices. Such macros can be removed or specialized: system modularity results. Impetus is given to applying the family concept in terminal design.

An example of functional modularity is a multiplex control device which consists of plug-in elements such as a channel unit, speed/code format decoder, data control unit, and power unit. Desired speed/code combinations in the format decoder can be implemented by replaceable majorboards. Character-rate regulation features for a variety of remote terminals can be established by means of plug-in majorboards.

Construction of special purpose computers by specialization or combination of generalized hardware and software modules will be possible. Tailoring hardware to the user's particular needs and/or applications appears straightforward.

Hardware modularity can also be applied to interconnected elements. Interconnect designs will include inter-junction, inter-flat pack, inter-majorboard, inter-unit, inter-shelf, and inter-blackboard. Disciplined interfaces can be established between the unit interconnect system, the structural system, and the cooling system; each of which will be constructed as a separate and virtually independent element. All modules can be constructed as plug-in functional entities. Hardware malfunctions will be corrected by immediate replacement of disabled modules. Malfunctions in real time systems will be corrected by replacement of disabled modules within a time span of less than one minute.

Functional modularity not only will help to alleviate interconnection problems within the module but also will premit the interconnection of modules such as processors, I/O channel handlers, memory elements, and peripheral devices. Dynamic system reconfiguration will be possible.

Modular design of system hardware is a basic determinant of the degree to which a system can be updated and of the ease with which such updating can be performed. Functional plug-in elements permit the system to be updated. Advancements resulting from technical developments can be readily incorporated in systems currently in operation. However, modular design should not be regarded as a permanent deterrent to obsolescence of fourth generation equipment.

Device-specific software routines will be eliminated; required functions will be performed by a general software routine and interchangeable functional hardware modules.

Collection of data at its source is a trend in the computer industry. On-line collection of data will be the standard rather than the exception in fourth generation systems. Translation of data from a medium understandable by the user to a medium understandable by the computer will be an accepted function of the computer hardware. Cards and attendant keypunching operations will be a secondary source of input.

Hardware diagnostic routines will be completely compatible with normal input/output routines and will be executed during normal system operation. Indication of malfunction will be detected and corrective procedures will be initiated. Thus, costly delays will be avoided. For example, a diagnostic routine can be run periodically to check multiplex operation. If the speed/code format decoder in a multiplex unit begins to fail, the operating system powers up another multiplex unit. Operations are switched to the alternate unit. A message on the typewriter console indicates that the speed/code format decoder has failed. Maintenance personnel can insert a new functional unit.

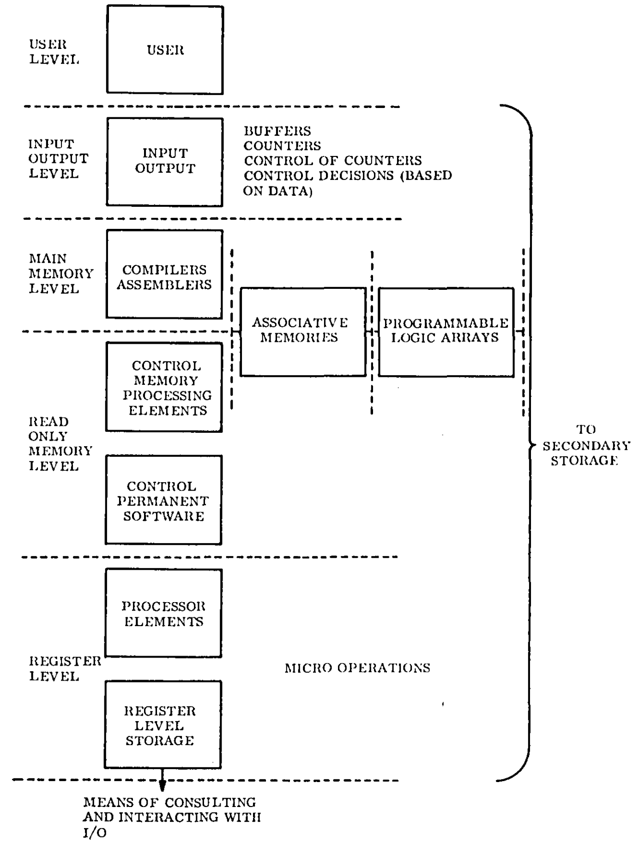

Fig. 1 Major memory level interfaces.

Compatibility of diagnostic routines and I/O routines achieves the following goals:

1. Minimizes system downtime due to malfunction of hardware elements,
2. Permits graceful degradation, and
3. Eliminates the necessity to interrupt normal processing to detect and correct minor hardware malfunctions.

FAMILY PLANNING

Before developing a new computer family, a manufacturer must answer the question "What fundamental EDP problems do I wish to solve?" Effort must be preceded by forethought; abilities and resources can then be channeled accordingly.

Fourth generation computer designers should consider carefully memory levels and interfaces when planning a new computer family. The major levels of memory and interfaces are shown in Fig. 1. The memory levels depicted in this illustration differ to some extent from the memory levels common in previous generations; the differences are possible because of LSI.

The disconnected lines in Fig. 1 indicate major interfaces which shift as required for particular family members. The roles of associative memories and of LSI programmable logic arrays also vary.

Read only memories (ROM), write optional memories (WOM), and associative memories can be used ex-

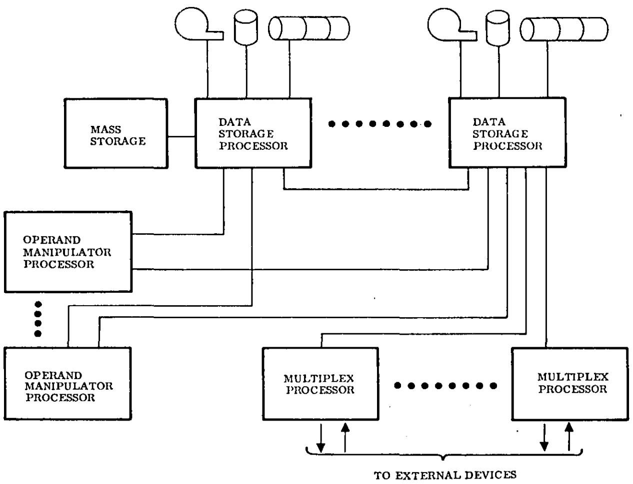

Fig. 2 Fourth generation computer systems.

tensively in medium and large family members — particularly in establishment of system management. Associative memories can be used for compiling, job assignment, parallel processing, search operations, handling of priorities and interrupts, and recognition of I/O commands. A most critical problem of third generation computing, particularly, in a multiprogramming environment, is limited concurrent operation of high-speed peripheral devices. Associative memories can facilitate concurrent operation of high-speed peripheral devices. If the cost of associative memories is reduced, use of these memories for information storage and retrieval will also be feasible. Designers should consider associative memories as applicable for associative processing.

Programmable logic arrays can perform many of the executive processes currently performed by software and can be used to tailor the system to meet particular user needs. These arrays and associative memories can replace operating system programs and be used to establish logical system organization.

Register-level designers can correlate software modular designs and physical modular designs (functions, translations, data formats, instruction formats, etc.). One group of system/software/LSI designers working at the register level can establish characteristics of the total system — register size, instruction set, multiprogramming, multiprocessing, etc. This group must also answer questions such as whether register logic, counters, comparisons, and control logic can be optimally performed by integrated circuits (IC) or by LSI.

Registers are used for temporary storage of data and instructions, for implementing arithmetic and logic operations, and for memory addressing. IC flip-flops are currently the primary method of implementing registers. Registers of fourth generation computers will be fabricated on a single monolithic chip. Metal-Oxide-Semiconductor (MOS) technology will be used where speed requirements are less stringent.

Control memory processing elements are used for temporary storage of intermediate results, frequently used data, constants, etc. Batch-fabricated, bipolar-transistor arrays will predominate this area in the near future. MOS arrays will be used in areas typified by slower speed requirements.

Main memories are used for the primary addressable storage of data and instructions of programs during execution. Ferrite core technology will continue to dominate this area if anticipated speed-cost improvements are realized. Contending technologies include thin-film (Bicore) for small units and plated wire for larger machines.

The input/output level interface includes auxiliary on-line secondary storage for storing tables, data, and alternate programs that require accessing speed comparable to that of main memory. Presently, disks, drums, and data cells provide this storage. Low-cost bulk core and plated wire memories will be widely used for on-line storage.

Reliability requirements for secondary storage in a single job stream environment differ significantly from requirements for secondary storage in a multiprogramming system. In the single job stream, all storage is reset to zero before initiating a new job. However, in a multiprogramming system, some vital information is retained in the system between jobs in secondary storage. The state of the system is continually changing. The organization and partitioning of secondary storage, inter-program protection and communication, and provision for backup and failure recovery are important.

COMMUNICATION AND CONTROL

What is the fundamental nature of computing? We believe that the basis for computing is data handling (data communication) and data control. Data must be communicated to the system, among system elements, and to external recipients. Data is accepted by the system, stored, and processed. Since the system requires I/O, storage, and processing capabilities, why not develop separate processors to perform these functions in an optimal manner?

Current multiprocessing systems are frequently characterized by identical processors used symmetrically. Such an arrangement reduces a multiprocessor system to a multiprogramming system if interlocks and interprocessor communications are ignored. Techniques of multiprogramming are known and give some insight into multiprocessor systems.

Traditional symmetric operation of identical processors used in a multiprocessor arrangement requires a complicated operating system. Instead of identical processors used symmetrically, we suggest separate processors for storage, for execution of application programs, and for multiplexing functions. If processors are allocated for these specific functions and if other features proposed in this article are implemented, hardware can control switching between programs, channel allocations, multiplexing, and most of the storage functions. Operating systems will be easier to design and operating efficiency will be significantly improved. We suggest that multiprocessing systems similar to the configuration shown in Fig. 2 can be widely used. By characterizing classes of programs, designers can determine system tradeoffs among desirable capabilities to be included in each functional block for specific families of programs.

The three functional processors can be contained within the same hardware unit. The dots in Fig. 2 indicate that additional processors can be added to the system. The communication architecture of this system will enhance and encourage modularity by assigning to hardware many of the functions currently performed by software. Failure of one processor will decrease system performance only to the extent that remaining processors cannot handle the workload.

The level of computing or data processing capability built into the hardware of each processor can be guided by the desire to achieve effective data compaction and thus, minimize data transfer between units. Such a design goal may lead to the incorporation of more hardware in a given processor than is necessary to make the unit self-regulating and self-reporting for availability. The design goal of increased overall system efficiency should take precedence over less comprehensive goals.

The operand manipulator processor will perform the application programming function. The communication control system program will reside in this processor. All logical processes other than system control functions will be executed by this processor.

The data storage processor will handle the requirements for associative memory, secondary storage, mass memory, and communications between processors. The logical structure of the system will be centered around this processor. The data storage element will be divided into zones based upon retention times of stored data. All logical communications between processors or processes will be handled by this processor. This arrangement will permit asynchronous communications.

The multiplex processor will include high-speed record channels with interrupt capability and a multiplex channel designed to service a large number of low-speed devices on a time division multiplex basis. These low-speed devices will include badge readers, teletypewriters, process control stations, bank teller window devices, on-line factory test devices, touch tones, keyboards, and CRT's. Automatic poll and call functions for devices requiring such services will be generated by hardware. Input lines will be scanned automatically by the multiplex channel unit, and data will be brought into main memory where it can be easily accessed by the data storage processor. The multiplex processor will be capable of continuous operation. Its functions will include accepting data into the system, making queue entries to provide the proper data processing functions, receiving the results of processing, and distributing these results to the external system.

Multiprocessing offers potential benefits of:

1. Speed, because execution is in parallel instead of serial;
2. Flexibility, because processing modules can be added without redesign of the system; and
3. Increased reliability, because redundant processors allow the system to degrade gracefully.

Such systems are readily adaptable to potential processor applications.

Fourth generation multiprocessor systems will be characterized by record channel units for communicating among processors and a multiplex processor for communicating to external elements. Record channel units will terminate devices which operate on a record-by-record basis and communicate asynchronously with the processor; e.g., drums, disks, and magnetic tapes. The multiplex channel will terminate independent low-speed devices which operate on a character-by-character basis. The channel will be a serial time division multiplex loop divided into a number of time division slots. Direct digital control loops can be attached to the multiplex channel.

Fourth generation computer designers will be cognizant of the importance of tradeoffs and of design interfaces and critical paths between physical modules, physical and software modules, and software modules. Designers of current software are more concerned with software-human interfaces than with intrasoftware interfaces structured to maximize applicability. Tradeoff and interface analyses must answer the questions "How will each change affect the user?" and "How much will each change affect the user?" System tradeoffs in four generation computers within communication and control systems will be expressed in terms of response times, communication channel bandwidths, equipment complexities, and numbers of channels.

In the multiprocessing system discussed in this article, standardization of interfaces and specifications of standard response times and bandwidths will permit the relocation of application devices in the system.

When the basic nature of computer applications is considered from a communication and control point of view, the following functions can be identified: data acquisition and reduction, algorithm computation, monitoring, and process optimization and control. These functions can be structured as a horizontal unification of computing elements, I/O and communication elements, and user devices, or data-generating elements. Within all applications, a vertical structuring is determined by the specific assignment which the system is initialized to perform. Hardware and software designers should jointly consider the functions identified above. After joint consideration of these functions, hardware designers can concentrate on the horizontal structuring, while software designers can focus primarily on the vertical structuring identified above.

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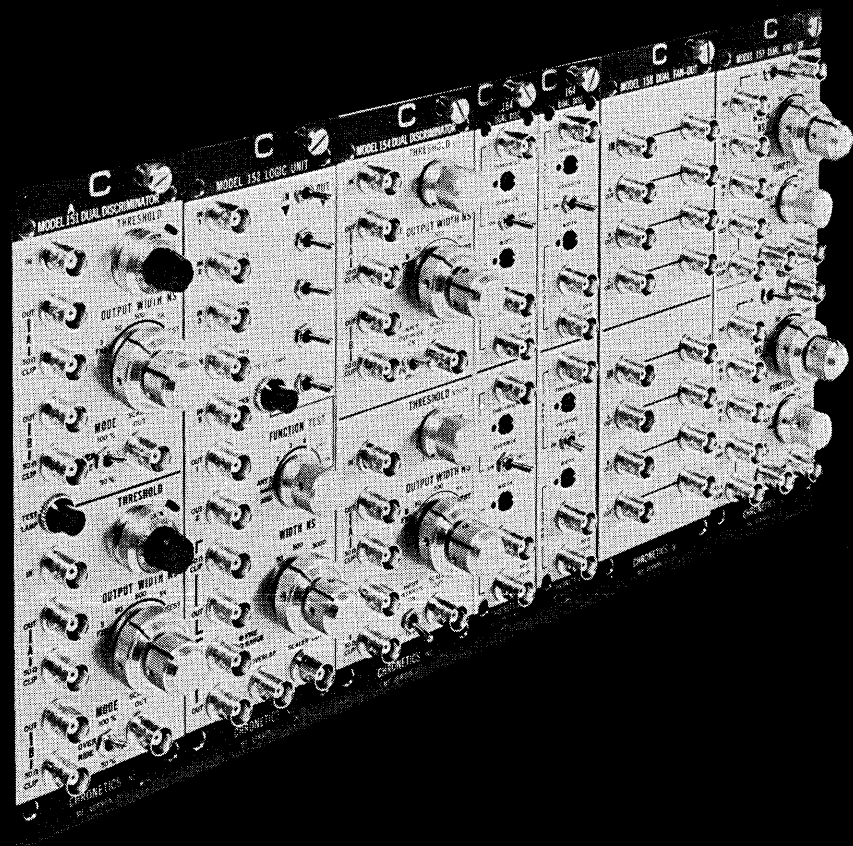
Part II of this series will cover Software and will appear in the September issue.

The Fast-Memory Measuring Machine



SERIAL BUFFER STORES USING DELAY LINES

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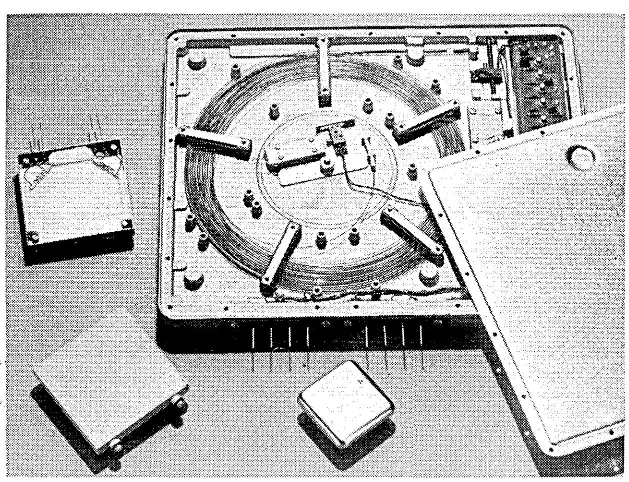
Considerations for choosing the right type of ultrasonic store for buffer applications are discussed in this article. Information on the performance and advantages of wire sonic, glass and quartz delay lines is included in order to allow the system designer to make the best choice for his particular store application.



Group of digital stores. Largest unit is wire-sonic type with 17,000 bit storage capacity at cost of approximately ½ cent per bit. Input transducer in center converts electrical signal to sonic energy which propagates through wire (coiled into multi-layer helix) until it reaches output transducer which reconverts the energy. Remaining stores contain glass. Unit with cover removed is 2,000 bit store.

The expanded use of computer terminal equipment has resulted in a growing interest in buffer stores for visual displays, printers, teletype equipment and modems. The logical organization of terminals often makes it desirable to use buffers which store data in serial form. Traditionally stores using wire-sonic delay lines have been employed in these applications; however, cores, discs, drums and MOS shift registers have found some acceptance. Recently, glass and quartz delay lines have been added to the list of devices used in serial stores.

In spite of the proliferation of new techniques and adaptations of old ones to serial buffer stores, the wire-sonic store remains the most widely used. However, when special requirements such as extraordinarily large bit capacities, operation in severe military environments, small size or low weight are more important than cost, quartz or glass stores can offer distinct advantages.

The purpose of this article is to describe the performance and advantage of each of the types of ultrasonic storage[1] — wire-sonic, glass, and quartz — enabling the sytem designer to make the best choice of store for his application. No attempt is made to compare ultrasonic stores to other types.

An ultrasonic store is assumed to consist of a drive circuit, an ultrasonic delay line, a recovery circuit, and facility for reading in, reading out and recirculating data. In this article the recording mode — NRZ, RZ, or bipolar — refers to that used on the delay line. It is assumed that the information to and from the store will always be NRZ. This means that the store appears to the user exactly like a shift register with the shift line driven by a crystal clock.

STORAGE CAPACITY LIMITATIONS IMPOSED BY SIGNAL ABSORPTION IN DELAY LINES

The maximum storage capacity of a single ultrasonic store is limited by the mechanical Q of the delay medium at the frequency of operation and by the temperature coefficients of time delay and amplitude

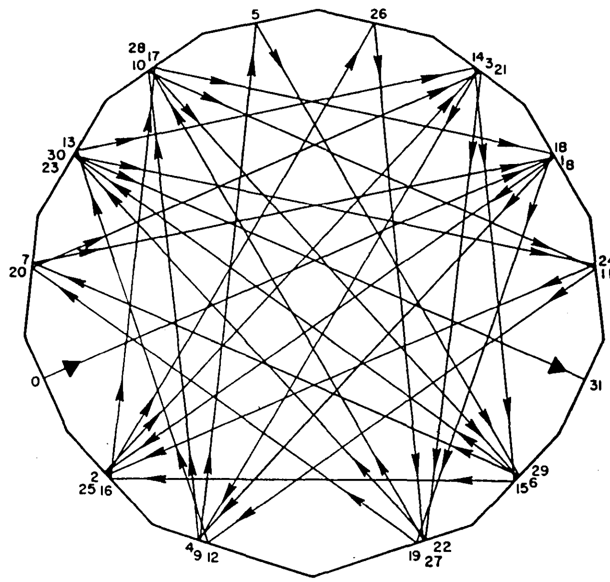
TABLE I

STORAGE CAPACITY LIMITATIONS DUE TO SIGNAL ABSORPTION

Type of Store	Frequency Range	Capacity Max. Storage	Operating Temperature Range
Wire-Sonic	1.5 to 2 MHz NRZ	30,000 Bits	15°C to 55°C
	.75 to 1 MHz RZ	15,000 Bits	
	1.5 to 2 MHz NRZ	8,000 Bits	—55°C to +75°C
	.75 to 1 MHz RZ	6,000 Bits	
Glass	20 to 40 MHz NRZ	5,000 Bits	15°C to 55°C
	10 to 20 MHz RZ	3,000 Bits	
	20 to 40 MHz NRZ	2,000 Bits	—55°C to +85°C
	10 to 20 MHz RZ	1,500 Bits	
Quartz	60 to 100 MHz NRZ	60,000 Bits	50°C to 100°C
	30 to 50 MHz RZ	40,000 Bits	
	60 to 100 MHz NRZ	30,000 Bits	15°C to 75°C
	30 to 50 MHz RZ	20,000 Bits	

Note 1: Capacities in the bipolar mode are generally slightly larger than for the RZ mode.

Note 2: The worst case access time of the store is equal to the capacity divided by the frequency.



Wave propagation pattern in polygonal quartz delay line serial store.

of the delay medium at the operating frequency over the desired temperature range.

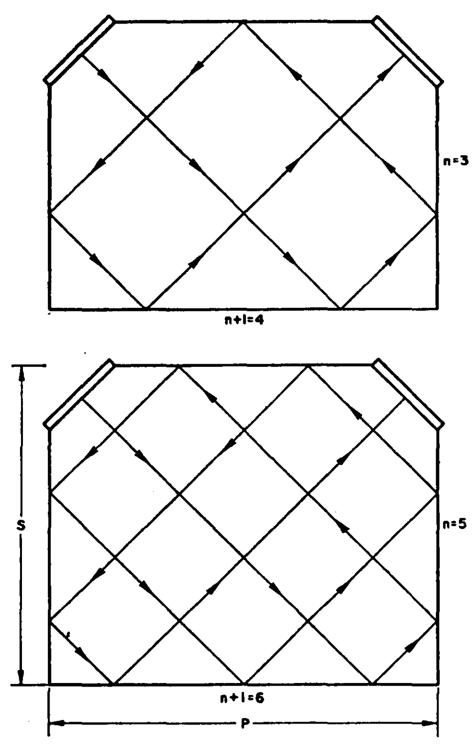
The mechanical Q of the material is a measure of how much of the input signal is lost due to the absorption mechanisms of the delay medium. If the loss is high, the storage is limited by the fact that the output data becomes undetectable. The loss mechanisms are many and complex, and for the purpose of this discussion, Table I, which illustrates the capacity limitations due to signal absorption in a general way, is sufficient.

The reason that the storage capacities of acoustic stores decrease with increasingly wide environmental temperature ranges is that signal absorption in delay media generally increases with decreasing temperature, resulting in undetectable output signals.

For bulk storage applications, the frequency and access time of an individual store are not important, since increased access time can be achieved by putting stores in series, increased frequency can be achieved by putting them in parallel and decreased frequency results from interleaving bits. Nothing can be done to decrease access time once the capacity and frequency of an individual store has been fixed.

STORAGE CAPACITY LIMITATIONS DUE TO TEMPERATURE COEFFICIENTS

Table I describes storage limitations imposed only by signal absorption. In practice realizable storage capacities of ultrasonic stores are rarely limited only by absorption, but also by the temperature coefficient



Wave propagation patterns in two typical digital glass delay line stores.

of time delay, which affects the ability to reclock the data at the output and by the temperature coefficient of the signal absorption which affects the ability to recover the signal from the delay line. The capacities in Table I can usually be achieved in systems in which the clock frequency is derived from the length of the delay line and the output amplifier gain is AGC'd. Slaving the clock to the length of the store does not limit a system to the use of one store, since temperature coefficients of time delay are reproducible store to store, and isothermal chambers which will hold all stores at the same temperature are easy to construct.

It is customary to assume that temperature drift of time delay can consume no greater than 80% of the bit period for RZ recording, 60% for NRZ operation and 40% for bipolar. Exceeding these limits will seriously jeopardize the ability of the store to clock the data out of the delay line without errors.

Stores Using Quartz Delay Lines

The delay line in quartz store has a temperature coefficient of time delay of -73.5 ppm/°C. If the store is to be used in a system with a fixed clock frequency, the temperature control for RZ operation which must be used for the store oven is:

$$\triangle\theta = \frac{\pm 5.44 \times 10^3}{N}$$

where N = The number of RZ bits in the store

$\triangle\theta$ = Temperature variation from nominal in °C.

Ovens with stabilities of ± .01°C are common, and stabilities of better than this are possible, so the storage capacities of quartz stores are not limited by realizable oven stabilities. If the clock frequency is derived from the length of the delay line, the temperature coefficient of attenuation limits capacity, particularly below 15°C, where the attenuation begins to rise rapidly with lowering temperature.

Stores Using Wire-Sonic Delay Lines

The situation for wire-sonic stores is quite different. Wire-sonic delay lines are almost never operated in ovens. The delay vs. temperature of the delay line takes an approximately quadratic shape across the range from −55°C to +125°C and this curve is approximately parabolic in the region from +15°C to +55°C (Fig. 1). The parabola is slightly steeper on the high temperature side of its minimum than on the low temperature side. The temperature of the minimum is adjustable and the low and high temperature legs take the form

$$\triangle D_{\text{low}} = 4.5\, D(\triangle\theta)^2_{\text{low}} \times 10^{-8}$$
$$\triangle D_{\text{high}} = 5.0\, D(\triangle\theta)^2_{\text{high}} \times 10^{-8}.$$

$\triangle D$ is the delay change in μsec from the delay at θ, D is the length of the line in μsec, and $\triangle\theta$ is the temperature difference in °C from the temperature at the minimum. To calculate the delay shifts across a commercial range of operating temperatures such as +15°C to +55°C, we assume that the parabolas are set at 35 ±5°C and find the expression for the largest shift as a function of delay is

$$\triangle D = 3.125 \times 10^{-5}\ D.$$

25°C, instead of 20°C, is used here as the difference in temperature from the parabola minimum to the extreme temperature, taking into account the uncertainty in the position of the parabola.

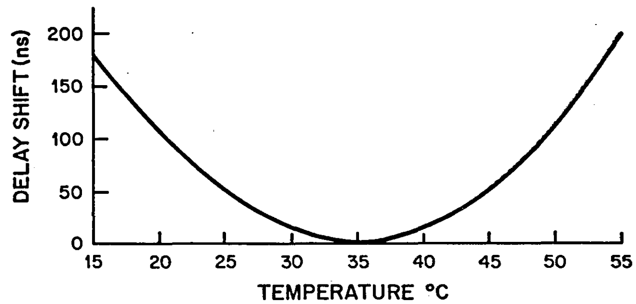


Fig. 1 Typical delay shift vs. temperature curve for a 10,000 foot μsec wire-sonic delay line.

Using our criteria for the portion of the clock period which can be consumed by delay drift of 80% for RZ, 60% for NRZ and 40% for bipolar, we can now calculate the maximum capacities possible for the various recording modes.

Thus, $\triangle D = \frac{.8}{f} = 3.125 \times 10^{-5} D$; Df = 25,600 bits RZ

and Df = 19,200 bits NRZ

Df = 12,800 bits bipolar.

It can be readily seen from this analysis that the limitation on wire-sonic storage comes from temperature considerations for fixed clock systems, and not the insertion loss considerations as shown in Table I. It should also be noted that bit capacities reduce rapidly as the temperature range increases beyond the 40°C spread assumed, until the range begins to cover the low temperatures where the assumption of a parabolic shape is no longer valid. One method of overcoming capacity limitation by temperature is to use a clock with a frequency derived from the length of the line.

Before leaving the subject of temperature limitations on capacity, it should be noted that amplitude change with temperature rarely imposes a capacity limit below that already imposed by delay drift or insertion loss in wire-sonic stores. Most stores with high capacities, however, require either gain compensation with temperature or AGC in the electronic circuits to avoid error generation with changing delay line output amplitude. This is due to the noise that is generated in wire-sonic delay lines, and if the detection circuit in the store has a fixed threshold, it may trigger on noise if the amplitude of the output signal of the line is high or lose the data if the amplitude is low.

Stores Using Glass Lines

The capacity limitations of glass stores have some of the same features as the limitations of wire-sonic stores. The delay vs. temperature curve of the delay line is parabolic as it was with the center of the wire curve, and its minimum point is controllable.

Expressing the glass store parabola in the same way as for the wire-sonic stores we find that

$$\triangle D_{low} = 2.6 \times 10^{-8} D(\triangle\theta)^2_{low}$$
$$\triangle D_{high} = 3.8 \times 10^{-8} D(\triangle\theta)^2_{high}.$$

The minimum of the parabola can usually be held to +35°C ±20°C. The expressions for maximum drift as a function of length for the temperature range +15°C to +55°C and −30°C to +85°C are

$$\triangle D = 6.1 \times 10^{-5} D\ (+15°C \text{ to } +55°C)$$
$$\triangle D = 1.9 \times 10^{-4} D\ (-30°C \text{ to } +85°C)$$

Solving for the number of bits stored in NRZ, RZ and bipolar recording for the two temperature ranges chosen yields:

Df = 13,100 bits NRZ	+15°C to +55°C
Df = 9,800 bits RZ	
Df = 6,650 bits bipolar	
Df = 4,200 bits NRZ	−30°C to +85°C
Df = 3,100 bits RZ	
Df = 2,100 bipolar	

Referring to Table I, this data indicates that signal absorption rather than drift limits capacity even across a range from −55°C to +85°C. As a matter of fact, drift limits capacity only when the range —55°C to 125°C is considered and even then the capacities just calculated are only reduced by about 40%.

Since glass delay lines usually have capacities well within the maximum allowed on a drift basis, they are rarely put in ovens or run with clocks slaved to line length. In addition AGC or amplitude compensation with temperature is not needed if the line is used in a commercial environment. However, over a military environment AGC is required in stores of maximum capacity. The amplitude change with temperature is not linear.

TABLE II

TEMPERATURE RANGE	AMPLITUDE CHANGE/ 1000 RZ BITS
—55°C to —30°C	+1.4 dB
—30°C to +15°C	+1.7 dB
+15° to +55°C	+ .8 dB
+55°C to +85°C	+ .4 dB
+85°C to 125°C	+ .2 dB

The change in amplitude is not the same across the frequency range so that pulse shape, as well as amplitude, changes with temperature. This sometimes prevents the achievement of the maximum bit capacities predicted by other criteria in lines intended to operate over wide temperaure ranges.

FREQUENCY RANGES FOR STORES USING ULTRASONIC DELAY LINES

The previous discussion looked at storage capacity from the point of view of the significance of signal absorption in the delay line and time delay drift and was based on the assumption that the store was being operated in its ideal frequency range. The three types of stores are all capable of operating over very wide frequency ranges with capacities reduced outside the ideal frequency range for many reasons. The explanations for capacity reduction outside the ideal frequency range are involved and a discussion of this is not appropriate for an article which does not deal with the physics of delay lines. This discussion will merely report the results of these considerations.

First, it is important to remember two basic rules.

1. In the ideal frequency ranges previously described, the length of the store in μsec can always be made shorter reducing capacity proportionately until a minimum capacity imposed by fabrication techniques is achieved. The minimum lengths are 1 μsec for quartz and glass stores and 10 μsec for wire-sonic stores.

2. The operating frequency of an ultrasonic store can always be reduced to zero frequency without changing its design. Bit capacity reduces proportionately. This can be accomplished merely by spreading out the pulses that propagate the zero's and one's in the delay line without changing the shape of the applied pulses. For instance a 100 μsec glass line designed to operate at 10 MHz RZ can be operated at 5 MHz RZ by spreading the input pulses out; however, since the frequency spectrum of the pulses of the signal applied to the delay line are the same at 5 MHz as they were at 10 MHz, the delay line will behave like a 10 MHz line over temperature. It should be noted that if RZ and NRZ frequency is reduced without changing the pulse characteristic, the reclocking window is increased. This is not, however, true of bipolar operation. In bipolar operation, the maximum window is 40% of the clock period of the fastest frequency at which the store *is* operated.[2]

Often it is desirable to design the delay line in a store to operate outside its ideal frequency range. One might for instance want a wire-sonic store because of its low cost, but need a frequency above 2 MHz, or one might want a glass line to operate at a low frequency to take advantage of its stability in extreme environments. Under these conditions merely changing the frequency of the store without changing the pulse drive shape and delay line bandwidth does not accomplish the desired goal.

Table III describes the range of delays over which wire-sonic delay lines will operate at various frequencies. Frequency, here, represents the highest frequency the store is designed to accept.

TABLE III

	MAX. DESIGN FREQUENCY	MAX. LENGTH	MAX. BITS
Below Normal Range	500 kHz RZ	20,000 usec	10,000
	500 kHz Bipolar	20,000	10,000
	1 MHz NRZ	20,000	20,000
Above* Normal Range	1.5 MHz RZ	4,000	6,000
	1.5 MHz Bipolar	4,000	6,000
	3.0 MHz NRZ	4,000	12,000

**Note:* *Above the upper frequency shown the mechanical Q of the delay medium falls off sharply and fabrication difficulties became extreme, so that only very short lines can be produced.*

Analyzing the situation for glass lines is more complex, because the Q of the material remains good throughout a wide frequency range and there is considerable freedom in the design of the line. Again tabulating the results without detailed analysis of the problems, we find capacities limited approximately as shown in Table IV.

TABLE IV

	MAX. DESIGN FREQUENCY	MAX. LENGTH	MAX. BITS
Below Normal Range	1 MHz RZ, Bipolar	150 usec	150
	2 MHz NRZ	150	300
	5 MHz RZ, Bipolar	200	1,000
Above Normal Range	50MHz NRZ	125	6,240
	50 MHz RZ, Bipolar	50	2,500
	100 MHz NRZ	50	5,000
	100 MHz RZ, Bipolar	20	2,000
	200 MHz NRZ	20	4,000

It is obvious from this that zero temperature coefficient glass stores offer real opportunities for high speed serial memories.

Quartz lines have very limited ranges of performance, but exceptional performance in these ranges. They have the unusual characteristic that when the frequency for which they are designed increases, the length can increase — thus, the maximum capacity increases rapidly with increasing frequency up to a limit of about 50,000 bits (Table V).

TABLE V

	MAX. DESIGN FREQUENCY	MAX. LENGTH	MAX. BITS
Below Normal Range	10 MHz RZ, Bipolar	100 usec	1,000
	20 MHz NRZ	100	2,000
	20MHz RZ, Bipolar	250	5,000
	40 MHz NRZ	200	10,000
Above Normal Range	75 MHz RZ	350	26,000
	150 MHz NRZ	350	52,400

For frequencies above 100 MHz RZ or 200 MHz NRZ, it is necessary to use sapphire rods with cadmium sulfide transducers for the delay lines in the stores. These devices can store up to 2,000 bits at RZ frequencies up to 1 GHz. Their temperature coefficient of time delay is +20 ppm/°C. They are still in the development stage, but appear to hold great promise for ultra high speed operation.

SIZE, MECHANICAL CHARACTERISTICS, POWER CONSUMPTION

Wire-sonic delay lines are usually constructed in multilayer helixes. There is a minimum diameter into which the helix can be constrained and still allow satisfactory performance. This minimum diameter increases with increasing delay time according to Fig. 2.

Usually the delay line case is square and approximately ½" deep. The electronics can take a great variety of forms, depending on whether it uses discrete components or microcircuits. Since the electronics, generally, has a small volume and is sometimes contained within the helix, it is not necessary to consider its volume when calculating the bit den-

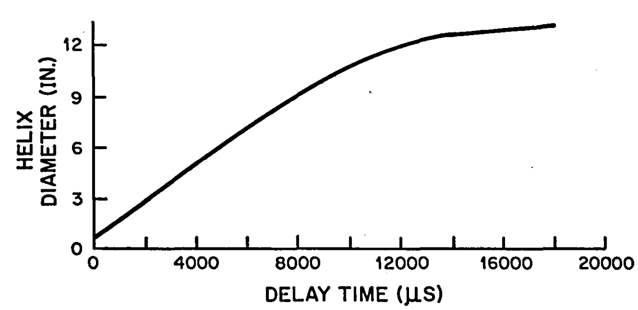


Fig. 2 Minimum helix diameter vs. delay time curve for wire-sonic delay lines.

sity of wire-sonic stores. In order to obtain some feeling for bit density one can use the graph to determine that the density of an 8.3 msec store operating at 2 MHz NRZ is 333 bits/in^3.

Stores with lower capacities have lower densities and stores with greater capacities have greater densities. Wire-sonic stores are usually either hermetically sealed or humidity sealed because delay time is slightly sensitive to humidity and the delay line wire will corrode when left in a highly humid environment for long periods of time.

Mechanically, the packages are quite rigid, but severe shock and vibration environments can be troublesome for stores requiring long delay lines. Wire-sonic stores up to 20,000msec can be made to sustain commercial vibration of a few G's without difficulty, but military versions can only be a few milliseconds long, to withstand 10 G's or more.

The mechanical situation for quartz stores is very straight forward. For capacities of 5000 to 50,000 bits the raw quartz blank for the delay line usually has a volume of approximately 6.3 in^3. Thus, the density varies from 800 bits/in^3 to 8,000 bits/in^3. However, this is only true of raw delay lines, and does not include the electronics or the packages. For asynchronous operation, where temperature control is not required, packaging halves the bit density and the volume of the electronics reduces it by another 25%. For temperature controlled units, the bit density reduces radically because of the volumes of the ovens and temperature controller, and it depends, to a large extent, on the number of lines placed in the oven. Thus, it is difficult to make generalizations about the bit densities of heated quartz stores, but it is usually safe to say that for large storage applications bit densities are somewhat higher than for wire-sonic lines.

The glass store usually represents a substantial improvement in bit density when compared to wire-sonic or quartz store. A two channel glass line operating at 40 MHz NRZ with a delay of 100 μsec can store 12,000 bits/cu. in. in a plate of glass 1/8″ thick. Packaging reduces this by half and the circuitry reduces it again by 50%. No ovens are required so the resulting bit density is 3000 bits/in^3. The volume of glass lines generally varies directly as the length of the delay and inversely as the cube of the frequency. As frequency is increased, the size of the total package cannot be reduced proportionately because glass lines become very small at very high frequencies while the size of the circuitry remains approximately fixed. It is again very hard to make generalizations; however, it should be noted that under the right conditions glass memories can be made extremely small, competing favorably with MOS shift register arrays and other integrated circuit techniques and often consuming less power. They are generally very rugged and can be used in severe military environments.

The power consumption of ultrasonic delay line stores can be extremely small. Nearly all delay lines can be driven by low voltages. Insertion losses are sometimes great, but not so great that high drive levels are required to keep the signal out of the noise. Thus, it is possible to store a tremendous number of bits in a delay line with very little power. As a matter of fact, wire-sonic stores have been built which consume only 6 μ watts/bit, and this does not represent a limit.

PRICE

Thus far, we have discussed at great length many technical considerations. In many commercial applications, however, price per bit often dominates all other considerations.

In stores using delay lines, price is only slightly dependent on length of delay. It does not cost much more to make a wire-sonic delay line out of 100 feet of wire than one foot. The most favorable pricing, therefore, for a delay line store occurs for capacities which are maximized just short of pushing the state-of-the-art. Table IV summarizes the pricing for the various types of stores when bought in quantities of thousands under idealized capacity conditions:

TABLE VI

TYPE	MODE	IDEAL CAPACITY	PRICE	PRICE/BIT
Wire-Sonic	NRZ	16,000 bits	\$ 75 - \$100	.5 to .6 cents
Glass	NRZ	5,000	100 - 150	2.0 to 3.0 cents
Quartz	RZ or NRZ	30,000	200 - 400	.7 to 1.3 cents

The quartz calculation is based on either multiple lines in an oven or asynchronous operation. Clearly the leader in this field is the wire-sonic store; however, quartz is close behind in applications when large total storage capacities are required per system. Glass is a poor third, but new fabricating techniques may help it become more competitive. Some people have predicted 0.1 cent/bit for glass.

CONCLUSION

This article has summarized the considerations in the choice of ultrasonic stores for buffer applications. Wire-sonic stores have been shown to be the most economical choice for commercial applications. Glass holds the edge for small size and military applications, and quartz is a contender for large capacity applications.

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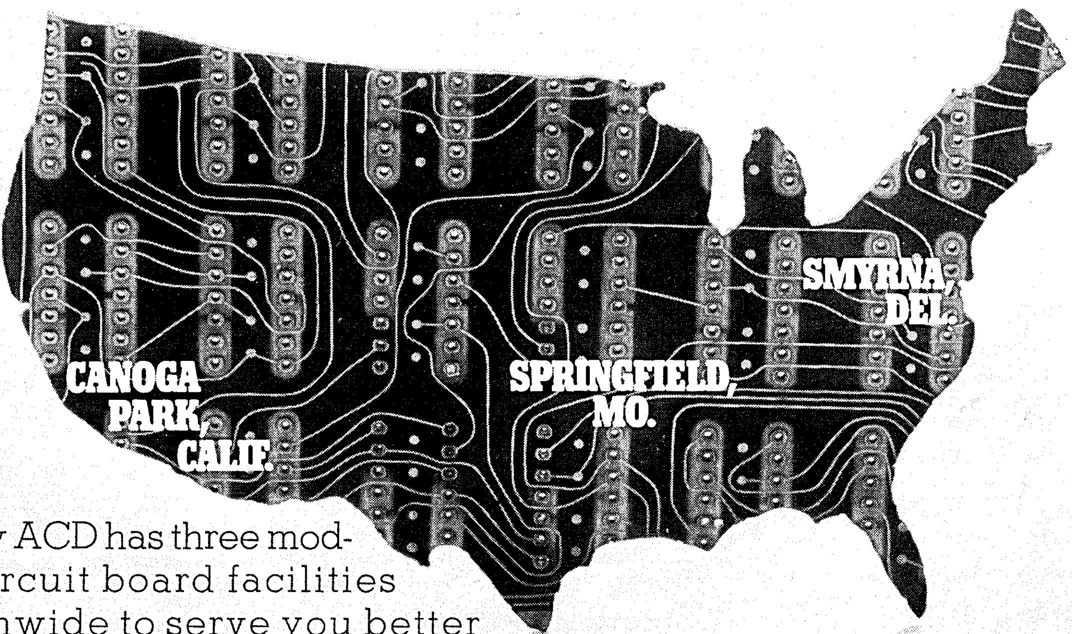

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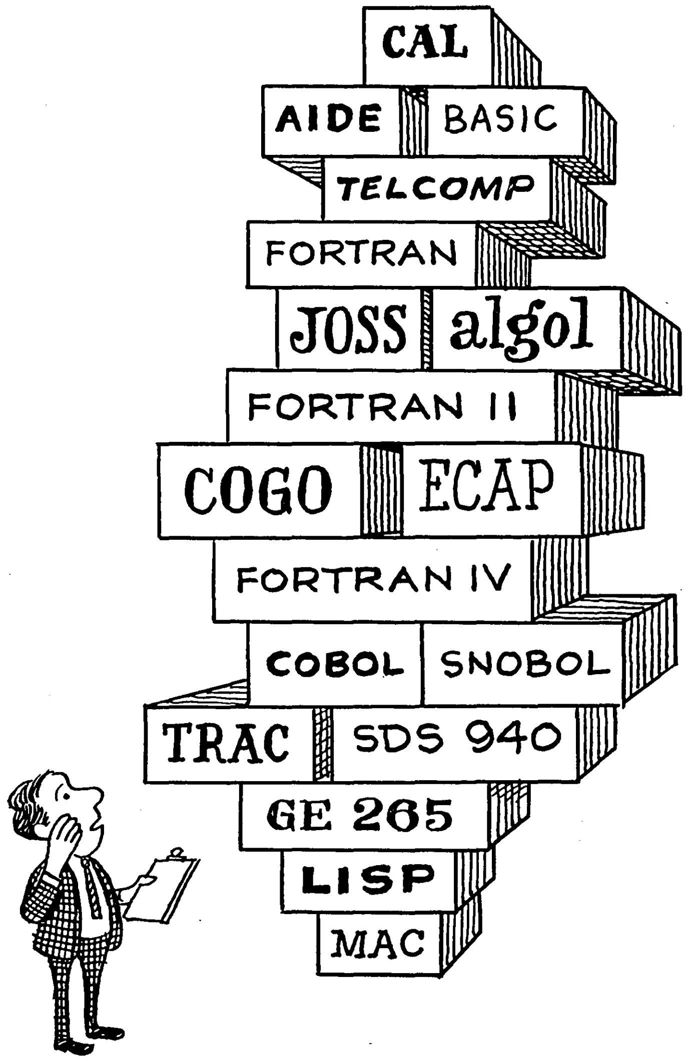

HOW TO PICK A TIME SHARING SERVICE

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This article is a synthesis of hundreds of conversations that I have had with people who have visited Applied Logic, or called us on the telephone seeking to learn about the new and interesting services offered by time shared computers and their various owners. In this article, I shall attempt to simulate a consumer-
As it is easier to talk to a familiar person, I shall oriented view of the industry, and warn of some of the pitfalls awaiting the unwary.
address this article to a person frequently called a computer coordinator. This may not always be your name, but you, in effect, coordinate the purchasing of outside computing for some corporate department or group. At the present time most computer coordinators are purchasing time on batch processing systems, and handling this function for various scientists, engineers, statisticians, or analysts, but you have been told to investigate time sharing systems and make a recommendation that will be worthwhile for the needs of the various people you serve.

Probably the easiest course is to go forth and hire a consultant who knows the field and can prepare a recommendation. This course of action is fraught with some uncertainty as many time sharing consultants have found the business so appealing that they have purchased their own time shared computers. So let us, for the purposes of this article, decide that you are going to listen to some salesmen, talk to some friends in the business who are using time sharing systems, and carefully study the charts and tables, such as the one we present at the end of this discourse. These charts, while frequently exciting more questions than they answer, serve as an excellent starting point for such analyses, and, if nothing else, get you organized and pointed in a rational direction. And by the way, speaking of rational directions, please note that this article does not point to things available in 1969 or 1970. It treats the time-sharing situation as it exists in the summer of 1968. The hardware and software devices — and services — that are mentioned are available right now to any person wishing to use a commercial time-sharing system through the dial-up telephone facilities.

The various subjects below are ordered according to my personal prejudices as to their relative importance. First, you will find a discussion of *languages*, then *costs of operation, mass storage, hardware* and *system software, security,* and, finally, *input and output methods and devices.*

You should first of all look at the people you serve to try to evaluate what they really need for what they are doing, for there is no point in using an elephant gun to shoot a squirrel, nor would it be wise to hunt grizzly bears with an air rifle. Are they engineers presently using slide rules and comptometers? If so, there is a family of languages called variously CAL, AIDE, and TELCOMP. They are all derived in some measure from JOSS, a language system developed by The Rand Corporation. They all speak reasonable English, can do some fancy mathematics, and will remember programs that you have written. This is a wonderful starting tool for a beginning computer user.

Next in our informal hierarchy is a language system called BASIC. It was developed by Professors Kemeny and Kurtz at Dartmouth College as a tool to get the Dartmouth College students familiar with computing. BASIC is a bit more complex, but still has some English-like qualities: it does mathematics for you, will set up matrix operations and has some logical capabilities. The BASIC system also allows you to store programs and data within itself more or less indefinitely. It is an excellent beginning tool for anyone needing to use both the logical and mathematical capabilities of a computer. The leading time sharing services offer BASIC in almost identical forms, each using a reference manual copied practically word for word from the Dartmouth College publication.

Both of the foregoing languages are not just languages, but are "systems"; that is, large programs which relieve you of the need to know anything about the computer you are using. The time sharing vendor's BASIC manual will supply you with the few commands needed to get you in and out of BASIC and on and off the computer. Naturally, every computer has restrictions on program size, and generality is paid for with complexity. So there are restraints on the JOSS-type languages and BASIC, mainly concerning the size of things that you write and store, plus the complexity and logical ability of the programs that you write. Because of the many housekeeping chores done by these systems, the cost to compute something will be relatively high in terms of computer time; however, this cost may be trivial compared to the man-hours saved in getting the problem solved. If the program, written in either BASIC or the JOSS-type language, is useful enough to be run frequently, you can save money and time by having it converted to one of the more complex but more efficient languages mentioned below. Find out if the time sharing vendor has a translator program that will do this for you.

We will now leave the beginning computer users and turn to those who have had some experience in computing, and are looking forward to speaking directly to a computer rather than through a batch system. It is beyond the scope of this discourse to treat the pros and cons of FORTRAN vs ALGOL. ALGOL has many admirers and is offered on most systems, but the vast majority of scientific and engineering work has so far been done in FORTRAN. There exist many packages of programs, such as the IBM Scientific Subroutines, or COGO, or ECAP, which are written in FORTRAN, and are available to the resourceful programmer. So, therefore, let us, for the purposes of this article, consider only FORTRAN.

Something to watch for is the ease (or lack thereof) of transfer from one FORTAN system to another. There is FORTRAN II, and there is FORTRAN IV as defined by ASA (American Standards Association). Then there are FORTRANS which have been augmented by various extra features — the GE FORTRAN being a good example of this genre. These extra features can be very useful within their own system, but cannot in most cases be transferred out to another time sharing or batch processing system. Programs written in this "non standard" FORTRAN must be run through a "sifter" or edited by hand for use outside — this can be a very tedious and expensive job, depending on how much the extra features have been used, and the sophistication of the sifter.

Ease of FORTRAN transfer becomes interesting if you are using the time sharing system to write programs for your own batch system; this is a not an uncommon practice as it saves a great deal of debugging time. Ease of transfer is also interesting if there is any chance that your programs may outgrow your present time sharing vendor, either in core demands or storage needs. When in doubt, present your prospective time sharing vendor with a FORTRAN deck taken from your batch processing computer and observe how much sweat is needed to make it run. The calls to tape drives, card readers and line printers will usually no longer be valid, as time sharing systems operate primarily with I/O files in discs, but aside from that, there should be minimal trouble if your batch and time sharing systems are to be used together.

There is one other area to survey in the FORTRAN capability that depends on the system software and hardware; that is the compiler and its use. There are two modes of operation. In one mode, you wait until the source (FORTRAN) program or routine is completely written, and then you have it translated (compiled) into the binary code that the computer understands. This binary program can be saved as is, with its subroutine calls, or assigned to its core locations (loaded) and saved as a "core image". The diagnostics, of course, appear when you compile, but not before. You can initiate the running of the program from any one of these three positions, i.e. source, object (binary) or core image. In such a system there is no need to compile before each run, a money and time saving feature for a program which runs often without changes. Within such a regimen, the efficiency of code produced by the compiler becomes more important than its speed.

In the other mode of operation, the order to compile sets into motion a more or less unbroken chain of events culminating (hopefully) in an answer. There is no way of saving object (binary) or core images, and you must compile every time you run. In such a system you have a greater need for a fast compiler rather than for one which produces optimized code. Check the costs carefully if you plan to run a production program often; the compile and load costs may eat you out of house and home.

On the other hand, if you are running lots of new programs, it doesn't matter, as you would be compiling most of the time under either system. Colleges and schools giving computing courses fall into this category.

While on the subject of FORTRAN, beware of the term "Conversational" FORTRAN". I frankly am not sure what it is; and I am sure that you could find as many definitions of "Conversational FORTRAN" as you can find definitions of the Democratic Party. Ask a few computer people and see for yourself.

Some of the more sophisticated users want to, or must, for one reason or another, program in the assembly or symbolic language written for the computer they are using. Perhaps they wish to write highly efficient subroutines, use non-algebraic qualities not available in FORTRAN, write a processor or system, or do something like packing characters into a word, so that they can only be retrieved with a special program. This last should be especially interesting to anyone setting up a data bank. The ability to work in assembly language can save a great deal of money in unit retrieval and storage costs. Several, but not all, of the time sharing vendors offer assembly language to the customers.

There are some other "high level" languages available from the various time sharing vendors which do other things than mathematics; one of these is COBOL, which (as the name implies) is good for Common Business-Oriented work; then others are SNOBOL, TRAC, and LISP, all of which are concerned with various aspects of text manipulation.

An interesting facet of multiple language capability is the ability (or lack thereof) of programs written in one language to call or access subroutines written in another language. This is possible and frequently very useful. An even more useful feature is the ability of a datafile to be accessed by programs or routines written in more than one language. That is, you would not need to have a FORTRAN or COBOL data file, but could have a data file accessible from programs written in either language.

An essential tool on a time sharing system is a good editor. This program lets you do the things you would ordinarily do with your own card deck; i.e. remove and/or insert cards to change the text, program, or data. At the very least, an editor will allow you to insert or delete entire lines of your text, program, or data. It will also type selected lines from your file or type the whole thing (on your teletype). A couple of other nice features which you might look for are: first, the ability to correct *part* of a line without retyping everything. This feature is especially useful if you have a long complicated format statement, as it might take two or three attempts to type the entire thing correctly. It is far easier to retype only the offensive part and have the editor insert it for you. A second good feature is the ability to make multiple corrections to a program or data file with a single command. This is useful if you have a misnamed variable which appears throughout a large program. Tell the editor what it is, and how you wish it changed, and it will do all the dog work.

As you become more sophisticated in your programming and your use of a time sharing computer, you may wish for a higher degree of interaction with your program, particularly while it is running. When using FORTRAN on a time shared machine, you can run your program or routine, and if it bombs for some reason, you can look at the diagnostics or the answers, make appropriate changes to the FORTRAN (source) code, and compile and run again. It is one of the great joys of time sharing that you can do this quickly and at one sitting. But what if the program is very large and complicated? What if the compile time is long? Or further, do you wish to see whether a reaction is diverging at a particular point, when it should be converging?

The answer is a program like DDT (for debugging, naturally) which is available on the Digital Equipment machines and some of the SDS 940's. Such a program is mainly for the use of sophisticated programmers and allows you to make changes to a running program in order to correct logical errors or change parameters.

COSTS OF OPERATION

Having narrowed the field down somewhat by selecting which language capability is available, where, you might now consider costs. Time sharing vendors as a class do not differ from those in any other field of endeavor in consciously or unconsciously plaguing the buyer with confusing rate structures and hidden charges. Just as you must check closely with the automobile salesman to be sure that everything is in the quotation and that the sales tax or the spare tire will not be added on after you have made your commitment, so you must warily approach the time sharing vendors to make sure that you know what is in store for you when the first bill arrives.

Let us first dispose of communications. Somehow you must be able to converse with the time shared computer from your remote location. These computers do not understand speech; and despite all the exciting pictures that you see in computer magazines, video terminals are several years away. So you must make do with a typewriter-like device which can transmit and receive your dialog with the computer. The common currency is, of course, the teletype [Models 33 or 35, ASR (paper tape) or KSR]. Order one from the telephone company along with a Dataset, or buy a teletype-voice coupler package (ask your time sharing vendor about these). You could become involved with an IBM 2741 bouncing ball terminal which has the advantages of easy type font changing, and the possibility of upper and lower case, if the time sharing vendor will support it. The difficuty is that the 2741 runs slightly faster than a teletype and therefore confuses many time sharing systems (fortunately not IBM's). Here, again, is the problem of transferability from one system to another.

The line and calling costs will be borne by you directly or indirectly. If you are close to the time shared computer, call direct; if you are too far away, use the time shared vendor's Foreign Exchange lines, or nearby multiplexers or data concentrators for a local phone call, and possibly pay a higher connection charge.

The connection charge buys you a computer port and continues for as long as you are connected to the computer, whether or not you touch a key on your teletype. The computer remembers when, and for how long, you were connected, and notes it down in its accounting file.

Once you are "connected" you may use the computer for compiling, running, debugging, etc. The computer will watch your particular job as it is processed, and rack up the time increments, it deems adequate for the work it is doing for you. At the end of the run, it will add up the time increments and print out a number it calls "processor time" or something like that, although it may actually have little to do with the fourth dimension. The measurement of the central processor time needed to process a particular job in a time sharing environment is a non-trivial task, and subject to the prejudices of the system's designers and programmers. In other words, when comparing time sharing systems by running benchmark programs, comparing processing times is all right, but the real test is to compare the dollar figures. And, by the way, when running "benchmarks" make three or four runs, preferably on two different days. The load peaks are usually between 10:00 A.M. and noon, and between 2:00 and 4:00 P.M. Run the benchmarks during a peak and then after hours, to see any differences in cost and total elapsed time.

There are other charges found on some systems which you should know about, such as a charge to change an account number, mount a tape, transfer files from active to inactive status, or to use peripheral devices at the computer center. Some charge an initiation fee to get on their systems; some have a monthly minimum.

People are always asking, and with good reason, how much it is going to cost to use a time sharing system. Unfortunately, this is like asking the gas company how much gas you are going to burn next month. It depend entirely on what sort of people you have, how many there are, and what they are doing. You could roughly say, though, that the use of a time sharing system will run between ten and twenty dollars per hour for editing, debugging, compiling, and running an average program, disregarding communication costs.

If you have just straight production jobs, then the cost is reasonably predictable; if there is much R&D work, the variances will be wide. However, the per hour costs are still cheap compared to the per hour costs of useful workers.

Examine the vendor's billing format to see what sort of invoice and "backup" you will receive at the end of the month. If you have several departments or projects, it is useful to have the invoice "backup" break these down, with subtotals, if possible. This makes the apportioning of the charges much easier and equitable. A consultant with a client using one of his programs would find this feature particularly useful.

I have been saving storage charge for last, as that seems to be the most complicated and frequently the most expensive subject. Almost all the time-sharing vendors offer more or less permanent storage on disc files, and their individual rate structures are functions of not only what the market will bear (value pricing), but also how much disc space their computers can actually handle, due to hardware and software constraints. In other words, the more disc space an individual system can handle, the lower the storage rates, and vice versa.

The worst part of this business is being sure that you are comparing oranges with oranges and not apples. Storage is rated by characters, bytes, bits, and words. A bit is a bit, but characters vary from 5 to 8 bits. A byte is usually 8 bits, and words vary from 12 to 48 bits. Here again I would confront the vendors with a known file or files, and ask how much it costs to store it for a month (or week, or day, or hour). Find out if you pay for what you actually use, or if you must commit for particular *units* of storage, one for each program, for instance, with the unit being of a fixed size, possibly much larger than your program.

Questions on related aspects of the storage problem are: How much do you pay for "scratch" storage while running a program? If you use a large quantity of extra storage on one or two days in a month, do you pay for the peak usage figure extended over the entire month? An unexpected, and brief use of a large amount of storage could raise your monthly bill to unexpected heights. If there is a tape backup or a tape facility for infrequently used files, how much does that cost, and how much to transfer them to the disc, or off?

MASS STORAGE

We will leave the business of how much it costs, but continue with the subject of storage for a while and cover a few more points. For instance, how much storage can you have at any one time? Some vendors have more to sell than others. Of course, if you don't need much, the question is irrelevant, but if you are contemplating some sort of data bank, it is important. Does the system care what is being stored? Some systems want to keep data in one place and programs in another. Still other systems do not care, and binary can be stored in the same place with a letter to your grandmother. If the computer you are using crashes and burns, can you reach your files through another computer nearby? This is a very important attribute for anyone with production programs that need to be accessed on a frequent basis (say every hour or so). And one other feature that should be mandatory is frequent incremental dumping on magnetic tape. Disc files do, once in a blue moon, get wiped out; and, as Charlie Brown is always saying, happiness is having backup files on tape.

Although all time sharing systems have at least a drum or disc file, or both, or several, and the term "random access" is used with great enthusiasm throughout the industry, make sure you ask how the system actually finds a file or record on the mass memory device. The easiest thing to do is treat the disc like magnetic tape and do a serial search, looking at each record or counting each record. This can take a long time! A better way is to reference a "block" or position on the disc the way you would reference a place in core memory, using an address. Thus, you can speed directly to the area where your file is stored, and start searching there; the only requirement is that your program should know what area to investigate before starting. This ability is an essential part of a viable information retrieval system.

HARDWARE AND SYSTEM SOFTWARE

You could make a reasonable short-term choice of a system without considering the shape of the hardware or systems software, providing your needs are not too demanding in the areas of sophistication, program size and performance. But for those of you with "demanding needs", I will note some features that should be considered in both hardware and software. I will remark first of all that if you use time-of-genesis as an index of worth, a good working time sharing software system is worth three to four times more than the associated hardware. Furthermore, the generation of a time sharing software system seem to be independent of scale. Having any more than one or two persons working on it seems more of a hindrance than a help (as IBM discovered when writing the 360/67 software). Tangentially, it is amusing to recall that three of the better known time-sharing systems were written by university students, i.e. the SDS 940, GE 265, and Project MAC. Is there some lesson to be learned here?

An important question to be asked about the hardware is — how old? Although the older hardware is well understood and debugged, still advances in the technologies of connectors, soldering, and solid state and integrated circuits will give the newer machine the edge in reliability and speed. If the system you like is currently running on an old machine, make sure that when the new model comes out you can transfer to the newer machine without going through the pain of a 1401 to 360/30-like conversion.

The word size is an often overlooked, but important feature, bearing upon the ease or difficulty of doing floating-point arithmetic. A computer with a 24 bit or less) word size will need to use two words per number and will give up to seven place accuracy. If there is a preponderance of code in your programs, OK; but if you are using large arrays or matrices, you will find that you have half as much core as you thought you had, and your program is running slower than you think it should. A larger word size will solve this problem, as for instance the 36 bit word used in the 7094 and PDP-10 will supply 8 place accuracy in floating point without using double precision. The Control Data 48 bit word is like Santa Claus.

The speed of the hardware, and the number of index registers or accumulators, and their speeds, the number of instructions, etc., should be of little interest to the ordinary user as the effects of these features are generally blanketed by the system software. If you're a slow driver driving a Ferrari, you could well be beaten by a fast driver piloting an old Ford. Likewise, the size and complexity of time-sharing software systems being what they are, an efficient system with 6 micro-second core memory can give a better performance than a poorly written one using one micro-second core memory.

In the words of the Prophet, "Programs expand to fill the core memory available, or, programmers can never get enough 'core'." Naturally, a question frequently asked about the capabilities of a time sharing system is: "How much core can I have?" You may discover upon investigation of the needs of your people that they will only write small programs, although this would be in violation of the law stated above. But certainly, a great many people are happily using machines of small core capacity and doing very useful things. If you do expect to see your program size increase as your professionals become more adept at computing, you should either make sure that the programs written on the small machine are readily transferable to a larger machine, or you should, at the outset, engage the use of a machine having a large core size.

Core available to the individual user varies from system to system, and can be as little as 6,000 characters, or run to apparent infinity if the machine has demand paging. Here, again, be very sure that you are not comparing 24 bit words with 36 bit words or worse yet, 36 bit words with 8 bit bytes. Most of us in the business casually refer to 20K of core or 50K of file storage; it is your task to understand what "K" we are talking about.

Sometimes, even though the allowable core area is ample for most of your work, you really need more. In that case you turn to "overlaying" or "chaining" programming devices known to 1401 and 7094 programmers, if not many more. These devices are available on several time sharing systems, and it is your job to discover how difficult they are to use. Must your people do the necessary coding, or will the loader handle most of it automatically? With such facilities you can run a 70,000 word program on a machine with a user core limitation of 24,000 words. Of course, if you have an array or matrix that is too big for your allotted core area, chaining will not help; and you had better find a larger machine, or make a deal to run during the wee hours of the morning when no one else is on the machine.

If you represent the interests of a large company or a software house, you may have a situation in which a person writes a program or system intended for use by others either at other locations within the company, or outside the company at customer or third party locations. One way to treat this situation is to allow each user to have his own copy of the program. Of course, you cannot tell how much he is using it, nor can you conveniently update or maintain it, and it is somewhat wasteful of storage. Another method is to have one copy of the program in a special location in the time sharing system which is used in a re-entrant mode. This presupposes a closer-than-usual relationship with the time sharing vendor, but is not only more economical of storage, it also allows the monitoring of useage.

SECURITY

File security is a function of various parts of the hardware and software and the system/customer interface. You enter the time sharing system using one or more passwords and you can have the computer interogate the "answer back" drum in your teletype. The passwords should not be common knowledge, and should be subject to rapid and convenient change should you desire. Once into the time-sharing system, you are protected by software and (hopefully) hardware devices.

COMMERCIAL TIME-SHARING SYSTEMS

ORGANIZATION	COMPUTER	CONVERSATIONAL LANGUAGES	TERMINALS	NO. OF* USERS	MINIMUM CHARGE PER MONTH	AVG. CHG. PER TER. HR.	CHARGE PER MIN. OF CPU TIME	DISC § STORAGE/ CUSTOMER
Allen-Babcock Computing, Inc. **Palo Alto, California**	IBM 360/50[1]	PL/1 (on-line subset)	IBM 2741 IBM 1050 TT-33, 35, 37, Friden 7100 Datel Thirty 21	90	$100.00	None	$5-$10[2]	100K+
Applied Logic Corp. **Princeton, New Jersey**	DEC PDP-6, PDP-10	FORTRAN IV, DDT, AIDE, BASIC MACRO-10 Compact COBOL, LISP, SNOBOL-6	TT-33, 35, 37 CRT; PLT IBM 2741	40	None	$10-$25	[3]	0+[4]
Bolt Beranek and Newman Inc.[5] **Cambridge, Massachusetts**	PDP-9/8 PDP-7/8	TELCOMP	TT-33	32	None	$12.50	None	Unlimited
CDC-CEIR	GE-235 DATANET-30 GE-420 DATANET-30	BASIC, ALGOL, FORTRAN	TT-33, 35	40[6]	$125.00	$6.25	None	
Computer Network Corp. **Washington, D.C.**	B-5500	FORTRAN IV, ALGOL, BASIC (4/15/68) SNOBOL, ALPS, DYNAMO	TT, Friden 7100, DCT 2000 CRT (6/68)	24	None	$8.50	$12.00	75K+
Computer Sharing Inc. **Bala Cynwyd, Pennsylvania**	SDS 940	CAL, ARPAS, BASIC, DDT, FORTRAN IV, FORTRAN II	TT-33, 35	32	None	$10.00	$2.50	60K+
COM-SHARE Inc.[7] **Ann Arbor, Michigan**	SDS 940	BASIC, CAL, QED, FORTRAN IV, SNOBOL, TAP, DDT, FORTRAN II	TT-33, 35, 37 CAL-COMP & HI PLT	40	$100.00	$10-$20	$2.50	0+
DIAL-DATA, Inc. **Newton, Massachusetts**	SDS 940	CAL, DDT, QED, FORTRAN II, BASIC, SNOBOL, FORTRAN IV, ARPAS	TT-33, 35[8] CAL-COMP PLT	40	$100.00	$13.50	$3.00	60K+
DIAL-DATA, Inc. of Washington **Rockville, Maryland**	SDS 940	CAL, DDT, QED, FORTRAN II, BASIC, SNOBOL, FORTRAN IV, ARPAS	TT-33, 35[8] CAL-COMP PLT	40	$100.00	$13.50	$3.00	60K+
General Electric Co.[9] **Information Service Dept.** **Bethesda, Maryland**	GE-235 DATANET-30	BASIC, ALGOL, FORTRAN	TT-33, 35 PLT	40	$100.00	$10.00	$2.40	0+
International Business Machines[10] **New York City, New York**	IBM 7044	QUIKTRAN	IBM 1050 IBM 2741	80	$125.00	$12.50[11]	None	0+
Intinco Limited **London, England**	UNIVAC 418 (2)	Stockbrokers Language	TT-33 (70) TT-35 (12)	82	[12]	[12]	[12]	[12]
John P. Maguire & Co., Inc. **New York City, New York**	IBM 360/30	D. O. S.	IBM 2740 IBM 1050	50	$1,500.00	[13]	[13]	[13]
KEYDATA Corp. **Cambridge, Massachusetts**	UNIVAC 491	KOP III	TT-28	200	[14]	[14]	[14]	[14]
On-Line Systems, Inc. **Pittsburgh, Pennsylvania**	GE-255[15]	BASIC, ALGOL, FORTRAN	TT-33, 35	30	None	$12.50	None	0+
Pillsbury Management Systems **Phoenix, Arizona**	DATANET-30	TRAC Test Editors Management Information Systems	TT-33, 35, 37 IBM 2741	15	$100.00	$5.00	$.60-$1.20[16]	0+
Pillsbury Occidental Company[17] **Raleigh, North Carolina**	GE-265	ALGOL, BASIC, BIICAC, FORTRAN, FORCAC, EDIT	TT-33, 35 PLT, CRT	40	$108.50	$10.00	$3.00	0+
Rapidata **New York City, New York**	GE-420 DATANET-30	BASIC (extended) FORTRAN IV	TT-33, 35	33	$100.00	$11.00	$3.00[18]	0+
REALTIME Systems Inc. **New York, New York**	B-5500	FORTRAN IV, COBOL, ALGOL	TT, TLX, TWX, CRT	15	$500.00	$10.00	$8.35	0+
TYMSHARE Inc. **Los Altos, California**	SDS 940	CAL, BASIC, QED, DDT, FORTRAN IV, ARPAS, ALGOL	TT-33, 35 PLT	60	$80.00 or $390.00	$13-$16	None	60K+
VIP Systems Corp. **Washington, D.C.**	IBM 1460	IBM Administrative Terminal System	IBM 2741	40	$100.00	$7.50	None	0+
White, Weld & Company **New York City, New York**	SDS 940	QED, DDT, FORTRAN II, FFL (First Financial Language)	TT-33, 35	24	$1,500.00	[19]	[19]	[19]

* In all cases the number of simultaneous users can be increased by addition of equipment or by duplicating the computer system.

§ Number denotes amount allocated in characters or bytes, + indicates more available at extra charge.

NOTES

1. Special operation codes for efficient conversational interaction added.
2. Dependent on amount of core used.
3. $.015 for each 10,000 instructions executed.
4. 60K free of charge for customers who pay the minimum charge of $100 per month.
5. Systems located in Cambridge, Massachusetts, East Orange, New Jersey, and London, England.
6. GE-420 handles 30 users.
7. Service also available from centers in Chicago, Houston, and Hackensack, New Jersey with more centers planned for the future.
8. Other terminal devices capable of connecting with 103 Data Sets and utilizing ASCII code may be interfaced with the system.
9. Service available from offices located in 33 major metropolitan areas.
10. Other systems in Chicago, Cleveland, Philadelphia, Los Angeles, and Toronto.
11. For first 5 hours, $11 for hours 6 thru 75. $9 thereafter.
12. A charge of approximately $5,000 per year plus a usage charge of $.05 per inquiry.
13. For accounting and other commercial uses. Charges are negotiated on processing and storage requirements.
14. For accounting and management uses. Charges on basis of message transmissions, processor time and storage used.
15. Time-sharing services also available on a PDP-10.
16. Depending on system used.
17. Trade name Call-A-Computer, service available from Atlanta, Boston, Chicago, Baltimore, Minneapolis, Omaha, New York.
18. I/O is charged at $1.80/minute.
19. Information not available.

(Excerpted from "Time-Sharing System Scorecard," No. 6, Spring 1968, and reprinted through the courtesy of Computer Research Corporation, Newton, Mass.)

The best and most certain protection against unauthorized access to files and running programs is through the use of hardware devices such as protection and relocation registers. Even though you consciously reference locations outside of your memory area, the hardware should positively prevent it. In the absence of hardware protection, it is possible to run in a so-called "interpretive" mode, as in the BASIC system with reasonable, but not rigorous security. When the system allows the use of assembly language, or the manipulation of the object program with DDT, then hardware protection is essential, or you may someday find yourself in the middle of some stranger's program.

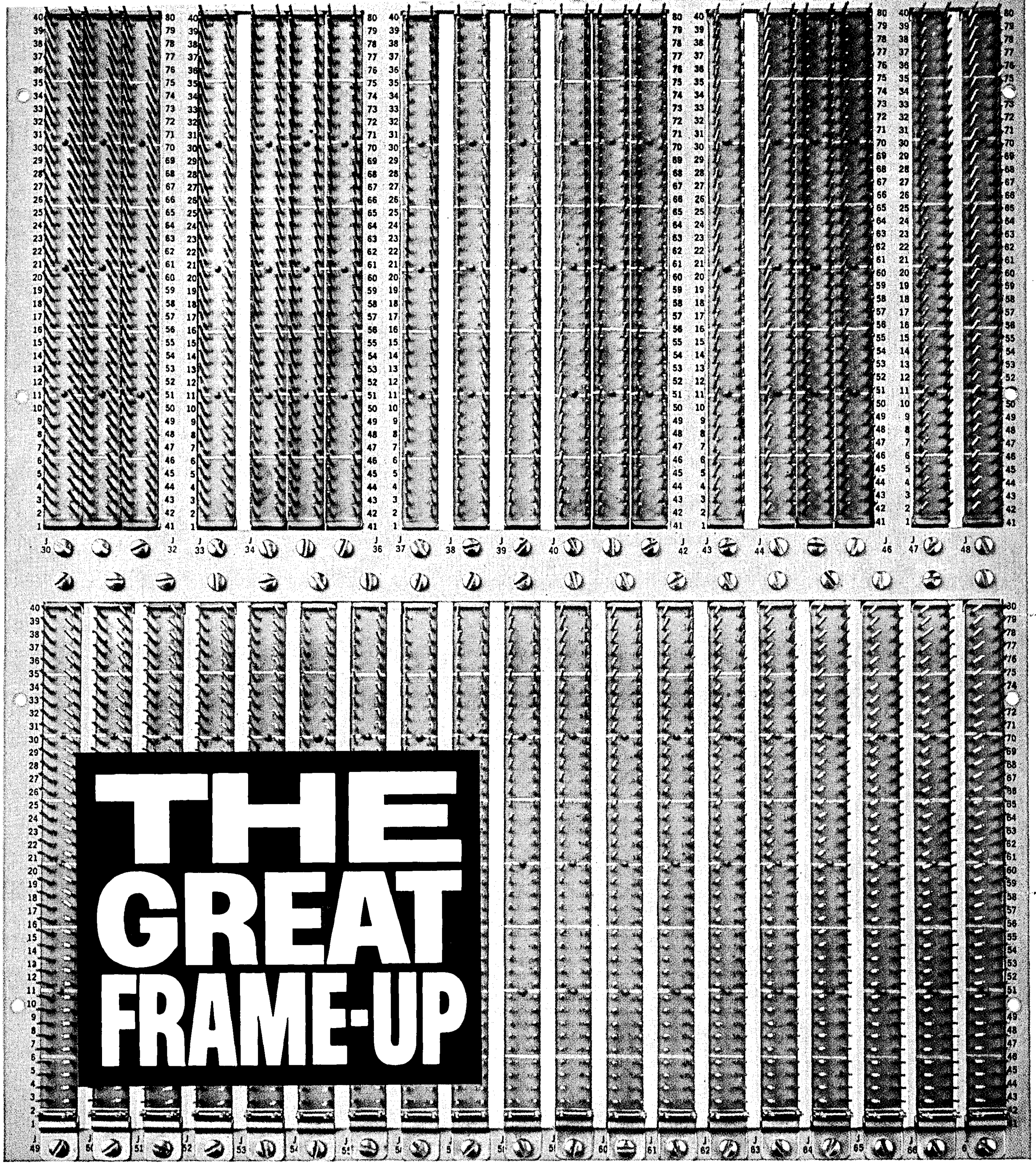
INPUT AND OUTPUT METHODS AND DEVICES

There are other ways of getting input and output from a time shared system than from a teletype. One thing to make clear at the outset is that unlike batch processing systems, programs running on time sharing systems cannot call I/O devices. If they were able to do this, there would be chaos in the computer room as when two concurrently running programs both called the line printer for output. I/O devices are simulated by files on the mass storage device and separate transfer programs can transfer output files from mass storage to the line printer, card punch, plotter, or tape drive. Check to see what sort of output facilities are available (aside from your teletype) and how the output can be delivered to you. The same goes for input. It does not have to go in through the teletype. It can go through the mail as a box of cards or a reel of tape. Just be sure that both parties have agreed on the format and density to be used.

There is much talk and high optimism about the use of remote data terminals on time sharing systems. They are now available on remote batch systems and have been for some time. But that is a far cry from being available on a time sharing system. If you think it would be interesting to have a small computer with a line printer and a card reader sitting at your place of business and acting as a funnel for the data coming from the machine, inquire about the prospective vendor's plans in this regard. He might even give you a quotation, but check the delivery closely!

One device you can have on your property is a Calcomp plotter; this has a data rate close enough to a teletype so that they can work in concert (using a special controller) and save many hours of making graphs by hand. The calls to the plotter are not difficult, and it is a wonder more people do not have them. Ask if your time sharing vendor provides the necessary software.

In summing up, try time sharing; it's great! If seriously used, your engineers and other professionals can increase their output to an astonishing degree, do things they wouldn't have attempted before, and have fun at the same time, as a quickly available computer can minimize so much of the drudgery associated with difficult problems, leaving only the interesting decisions to ponder.


THE
GREAT
FRAME-UP

Biltmore Hotel, site of the Wescon technical sessions.

WESCON 68

Los Angeles / August 20-23

TECHNICAL PROGRAM EXCERPTS

Thirty-two technical sessions have been scheduled for Wescon 68. The program will run for four days August 20-23. All sessions will be held in the Biltmore Hotel. Morning programs will be held from 9:30 AM to noon and afternoon programs from 2 to 4:30 PM. Dr. Robert M. Ashbey, V.P. of Technology, Autonetics Div. of North American Rockwell, is the Technical Program Chairman. The sessions were chosen to offer wide variety in subject matter. Three sessions deal with technical management and marketing questions; four are devoted to electronics, law enforcement, educational instrumentation, and urban affairs; two cover advances in digital systems; and others cover medical instrumentation, fluidics, utility power, computer controls and advances in materials for electronics. The regular $2 Wescon registration fee is good for all these sessions. As a supplement to the technical program, a Science Film Theatre, with a daily program will be presented at the Holllywood Park exhibit area.

In addition to the regular technical program, Wescon will present two "Concurrent Symposia" on Electronic Circuit Packaging Aug. 19-20 and Hybrid Microelectronic Circuits Aug. 21-22 at the Statler Hilton Hotel. There is a $40 fee for each of these sessions which includes lunch and the complete symposium record. Program excerpts of interest to the readers of Computer Design follow:

Tuesday, Aug. 20

Special Session A:

Management Successment

2-4:30 pm, Biltmore Ballroom

Chairman: Don C. Hoefler, *Electronic News,* San Francisco, Calif.

A/1 IDENTIFICATION OF TALENT FOR TECHNICAL MANAGEMENT, Alfred G. Scheid, Shareholders Management Co., Los Angeles, Calif.

A/2 RECRUITMENT OF TOMORROW'S MANAGERS, Jack Yelverton, Wilkinson, Sedwick & Yelverton, San Francisco, Calif.

A/3 TRAINING: HOW TO DEVELOP MANAGEMENT SKILLS, Lloyd Kelly, General Precision, Tarrytown, N.Y.

A/4 HOW TO PLAN FOR MANAGEMENT IN A GROWING ORGANIZATION, (speaker to be announced).

Wednesday, Aug. 21

Session 7:

Marketing Electronic Products in Europe

9:30-noon, Biltmore Ballroom

Chairman: C. Gerald Diamond, Sensus International, San Francisco, Calif.

7/1 HOW TO RESEARCH AND PLAN FOR EUROPEAN ELECTRONICS MARKETING. G. B. Levine, Mentor International, San Francisco, Calif.

7/2 U. S. EXPORT CONTROLS AND ELECTRONICS MARKETING IN EUROPE. Rauer H. Meyer, U. S. Department of Commerce, Washington, D.C.

7/3 HOW TO SELECT AND WORK WITH REPRESENTATIVES AND LICENSEES IN EUROPEAN ELECTRONICS. Pierre F. Simon, Machine & Products Co., New York N.Y.

7/4 HOW TO ESTABLISH AND MAINTAIN A COMPANY SALES FORCE IN EUROPE. William P. Doolittle, Hewlett-Packard Co., Palo Alto, Calif.

Session 8:

Digital Encoding (Source Encoding) Systems

9:30-noon, Biltmore Renaissance Room

Chairman: J. B. O'Neal Jr., North Carolina State University, Raleigh, N.C.

8/1 INFORMATION RATES FOR DATA COMPRESSION. L. D. Davisson, Princeton University, Princeton, N.J.

8/2 PREDICTIVE CODING OF SPEECH SIGNALS. B. S. Atal and M. R. Schroeder, Bell Telephone Laboratories, Murray Hill, N.J.

8/3 CONTOUR CODING OF IMAGES. W. F. Schreiber and T. S. Huang, M.I.T., Cambridge, Mass.

8/4 FRAME-TO-FRAME DIGITAL PROCESSING OF TV PICTURES TO REMOVE REDUNDANCY. F. W. Mounts, Bell Telephone Laboratories, Holmdel, N.J.

(continued on page 68)

WESCON TECHNICAL PROGRAM EXCERPTS

(continued from page 67)

Session 9:

Integrated Circuits: How Do You Test Them? How Much Testing Must You Do?

9:30-noon, Biltmore Bowl

Chairman: Raymond D. Speer, *Electronic Design Magazine,* New York, N.Y.

9/1 IC TESTING — THE PROBLEMS OF THE INDUSTRIAL USER, Dick Hall, Systron Donner Corp., Concord, Calif.

9/2 THE PROBLEMS OF THE MILITARY-ORIENTED USER, (Speaker to be announced.)

9/3 THE MANUFACTURER'S VIEWPOINT, Gene Blanchette, Motorola Semiconductor Products, Phoenix, Ariz.

9/4 THE CAPABILITIES OF THE LOW-VOLUME TESTER, Gary Strong, Signetics Corporation, Sunnyvale, Calif.

9/5 THE CAPABILITIES OF HIGH-VOLUME TESTER, Gordon Padwick, Fairchild Instrumentation, Sunnyvale, Calif.

Session 10:

Flat Panel Displays

9:30-noon, Biltmore Galeria Room

Chairman: L. A. Murray, RCA Electronic Components, Somerville, N.J.

10/1 BATCH-PROCESS ALPHANUMBERIC DISPLAYS. R. Klein, S. Caplan and A. Elsea, RCA Electronic Components, Somerville, N. J.

10/2 SOLID-STATE INJECTION ELECTROLUMINESCENT ARRAYS. S. Caplan, L. Murray, and W. Agosto, RCA Electronic Components, Somerville, N. J.

10/3 A 5-VOLT SOLID-STATE NUMERIC READOUT WITH MONOLITHIC MEMORY - DECODER - DRIVER. J. F. Caldwell, D. K. Hillman, and D. Seymour, Monsanto Company, St. Louis, Missouri.

10/4 PLASMA DISPLAY PANEL. R. H. Willson, Defense and Space Center, Westinghouse Electronic Corp., Baltimore, Md.

Special Session B:

Planning for Company Growth

2-4:30 pm, Biltmore Ballroom

Chairman: Dr. John M. Salzer, Salzer Technology Enterprises, Los Angeles, Calif.

B/1 TECHNOLOGICAL FORECASTING. Dr. Harper North, TRW, Inc., and Donald L. Pyke, TRW, Inc., Los Angeles.

B/2 CHOOSING CORPORATE STRATEGY IN THE ELECTRONICS INDUSTRY. Phillip F. Meyers, Electronic Specialty Co., Los Angeles.

B/3 CORPORATE PLANNING FOR DIVERSIFICATION AND GROWTH. I. Gordon Odell, North American Rockwell, El Segundo, Calif.

B/4 NEAR-TERM IMPLEMENTATION OF LONG-RANGE OBJECTIVES. J. W. Stark, Librascope Group, General Precision Systems Inc., Glendale, Calif.

Session 12:

New Developments in Digital Communications

2-4:30 pm, Biltmore Renaissance Room

Chairman: R. E. Heckert, Hughes Aircraft Co., Fullerton, Calif.

12/1 ADEM, A NEW ADAPTIVE DATA EQUALIZED MODEM. D. M. Motley and G. K. McAuliffe, Anaheim, California, R. Northrup, USAF Rome Air Development Center, Griffis AFB, Rome, N.Y.

12/2 SOME FEATURES OF THE HC-278 MODEM. J. E. Toffler and P. N. Winters, Hughes Aircraft Company, Fullerton, Calif.

12/3 QUADRATURE SIGNAL PROCESSING TECHNIQUES: P. N. Winters, Hughes Aircraft Company, Fullerton, Calif.

12/4 EQUALIZATION FOR DATA TRANSMISSION. D. M. Motley and G. K. McAuliffe, Autonetics, Anaheim, Calif.

Session 13:

The Computer as a Control Device for Testing Equipment

2-4:30 pm, Biltmore Music Room

Chairman: John J. Szalay, Industrial Corporation of America, Los Angeles, Calif.

13/1 PROGRAMMING REQUIREMENTS FOR TESTING CONTROL COMPUTER. William W. McGhee, Litton Industries, Woodland Hills, Calif.

13/2 INTERFACE DESIGN CONSIDERATIONS AND CONSTRAINTS. Wallace W. Mingus, Litton Industries, Woodland, Hills.

13/3 HARDWARE-SOFTWARE TRADE-OFFS WHEN APPLYING COMPUTERS TO TESTING. James E. Stuehler, IBM Systems Manufacturing Div., San Jose, Calif.

13/4 ADVANCES OF MAGNETIC RECORDING MEDIA. George E. Wilhelm, Thin Film Inc., Los Angeles, Calif.

Session 14:

Application of Mathematical Programming Methods in Engineering Design

2-4:30 pm, Biltmore Galeria Room

Chairman: Daniel Tabak, Wolf R&D Corp., Riverdale, Md.

14/1 IDENTIFICATION OF LINEAR SYSTEMS USING MATHEMATICAL PROGRAMMING. R. W. Harrison, Leeds & Northrup Co., North Wales, Pa. and K. A. Fegley, University of Pennsylvania, Philadelphia, Pa.

14/2 OPTIMIZATION OF A MULTI-STAGE FLASH DESALINIZATION PLANT. J. H. Beamer and D. J. Wilde, Stanford University, Stanford, Calif.

14/3 DESIGN OF DIGITAL CONTROLLERS FOR NONLINEAR SYSTEMS BY MATHEMATICAL PROGRAMMING. G. Porcelli, General Electric Co., Philadelphia, Pa., D. Tabak, Wolf R&D Corp., K. A. Fegley, University of Pennsylvania.

14/4 A COMPUTATIONAL PROCEDURE FOR FIXED-TIME FUEL-OPTIMAL CONTROL OF LINEAR STATE-CONSTRAINED SYSTEMS. A. F. Fath, Boeing Scientific Research Labs., Seattle, Washington.

Thursday, Aug. 22

Session 15:

Fluidic—Electronic Analogies

9:30-noon, Biltmore Bowl

Organizer: Dr. John M. Salzer, Salzer Technology Enterprises, Los Angeles, Calif.

Chairman: Albertus E. Schmidlin, General Precision Systems, Glendale, Calif.

15/1 ANALYTICAL TECHNIQUES FOR FLUIDIC ANALOG SYSTEMS. Ruel Ross Clark, Imperial-Eastman Corp.

15/2 DEVELOPMENT OF A FLUERIC AMPLIFIER TRANSFER MATRIX. Francis J. Manion, Harry Diamond Labs, Washington, D.C.

15/3 A-C FLUIDICS. Carl W. Woodson, General Electric Co.

15/4 FLUIDIC DIAPHRAGM LOGIC. D. F. Jensen and R. R. Schaffer, IBM Systems Development Division.

Session 16:

Optics and Electro-Optics in Computers

9:30-noon, Biltmore Music Room

Chairman: B. R. Shah, IBM Corp., Poughkeepsie, N.Y.

Co-Chairman: T. J. Harris. IBM Corp., Poughkeepsie, N.Y.

16/1 SOME CONSIDERATIONS IN THE DESIGN OF A LASER THERMAL-MICRO IMAGE RECORDER. C. O. Carlson, D. Ives, National Cash Register Corp.

16/4 RESEARCH ON LASERS FOR LOGIC CIRCUITS. W. F. Kosonocky, RCA Laboratories, Princeton, N.J.

16/5 OPTICAL INTERCONNECTIONS IN COMPUTERS. K. L. Konnerth, B. R. Shah, IBM Corp.

16/6 UNCOMMON ELECTRO-OPTICS FOR DISPLAY AND PROCESSING. W. J. Poppelbaum, M. Faiman, University of Illinois.

Session 17:

Significant Developments in Magnetic Devices

9:30-noon, Biltmore Galeria Room

Organizer: Herman I. Tillinger, Bell Telephone Labs, Whippany, N.J.

Chairman: Harold Lord, Consulting Engineer, Mill Valley, Calif.

17/1 RELIABILITY CONSIDERATIONS IN ELECTRONICS TRANSFORMERS FOR SPACE APPLICATIONS. E. Wiler, Jet Propulsion Laboratory, Pasadena, Calif.

17/2 THE PARAFORMER — A NEW PASSIVE POWER CONVERSION DEVICE. S. D. Wanlass, Wanlass Electric Co., Santa Ana, Calif.

17/3 MINIATURE LAMINATED CORES OF IMPROVED PERMEABILITY FOR LOW FREQUENCY TRANSFORMERS AND REACTORS. G. B. Finke and W. T. Mitchell, Magnetic Metals Co., Camden, N.J.

17/4 NEW MAGNETIC SWITCH EXPLODING BRIDGE WIRE FIRING SYSTEM AND DESIGN PROCEDURE. K. Aaland, Lawrence Radiation Laboratory, Livermore, Calif.

17/5 DESIGN CONSIDERATIONS OF A TWO-TRANSFORMER SERIES FEEDBACK CONVERTER. R. L. Peterson, Litton Industries, Woodland Hills, Calif.

Session 21:

Computerized Pattern Recognition and Communication

2-4:30 pm, Biltmore Music Room

Chairman: Edward A. Patrick, Purdue University, Lafayette, Ind.

21/1 FEATURE SELECTION IN PATTERN RECOGNITION AND COMMUNICATIONS. K. Fukunaga, Purdue University, Lafayette, Ind.

21/2 ESTIMATION AND RECOGNITION WITH COMPUTER OUTPUT DISPLAY. E. A. Patrick, Purdue University.

21/3 DEMO I—A SUPERVISED/UNSUPERVISED PORTABLE LEARNING COMPUTER. F. C. Monds, The Queen's University of Belfast, Northern Ireland, and G. Carayannopoulos, Purdue University.

21/4 FEEDBACK SIGNAL DESIGN FOR MULTI-CLASSES SOURCES. J. Y. S. Luh, Purdue University.

Friday, Aug. 23

Session 24:

Advances in Materials for Tomorrow's Electronics

9:30-noon, Biltmore Renaissance Room

Organizer: P. Michael Sinclair, Industrial Research Magazine, Beverly Shores, Ind. Chairman: Irwin Stambler, Industrial Research Magazine, Los Angeles, Calif.

24/1 FOURTH PERIOD COMPOUND SEMICONDUCTORS. Rudolph August, Autonetics, Research & Engineering Division, Anaheim, Calif.

24/2 FERROMAGNETIC MATERIALS. Eberhard Schwabe, RCA Memory Production Division, Needham, Mass.

24/3 ADVANCES IN SUPERCONDUCTIVE MATERIALS. Juri Matisoo, IBM Watson Research Center, Yorktown Heights, N.Y.

24/4 THE ALL-PLASTIC TRANSISTOR. Jerome J. Surran, General Electric Electronics Laboratory, Syracuse, N.Y.

Session 25:

Qualitative Pattern Recognition Through Image Shaping

9:30-noon, Biltmore Music Room

Chairman: H. Hemami, Ohio State University.

25/1 QUALITATIVE PATTERN RECOGNITION VIA OPTICAL SYSTEMS. H. Hemami, Ohio State University, Columbus, Ohio.

25/2 EDGE ENHANCEMENT OF PHOTOGRAPHIC IMAGERY—A MATHEMATICAL REPRESENTATION AND OPTICAL IMPLEMENTATION. W. F. Haagen, Bendix Electro-Optics Division, Ann Arbor, Mich.

25/3 CHARACTER RECOGNITION VIA FOURIER DESCRIPTORS. E. L. Brill, Battelle Memorial Institute, Columbus, Ohio.

Session 26:

High Power Solid-State Inverters

9:30-noon, Biltmore Galeria Room

Chairman: David W. Borst, International Rectifier, El Segundo, Calif.

26/1 THREE-PHASE STATIC INVERTERS. Stuart J. Jackson, Solidstate Controls Inc., Columbus, Ohio.

26/2 STATIC INVERTERS IMPROVE CONTROL RELIABILITY. Robert Rosko, Public Service Electric and Gas Co Newark, N.J.

26/3 INVERTERS AND THE APPLICATIONS. K. Lach and J. Riordan, Networks Electronic, Chatsworth, Calif.

26/4 INVERTER THYRISTORS—WHAT AFFECTS THEM—HOW TO CHARACTERIZE THEM. D. Cooper and D. Borst, International Rectifier, El Segundo, Calif.

Session 27:

The Computers Impact on Power Systems

2-4:30 pm, Biltmore Renaissance Room

Chairman: P. G. Lowery, Department of Water and Power, Los Angeles, Calif.

27/1 GRAPHIC DISPLAY FOR POWER SYSTEM CONTROL COMPUTERS. Raymond C. Burt, Los Angeles Department of Water and Power.

27/2 DYNAMIC SIMULATION OF POWER SYSTEMS. Robert C. Durbeck, IBM Research Laboratory, San Jose, Calif.

27/3 COMPUTER CONTROL OF POWER SYSTEM. M. D. Liechty, Leeds and Northrop Co., San Francisco, Calif.

27/4 THE ROLE OF COMPUTERS IN VERY LARGE POWER INTERCONNECTIONS. (Author to be announced.)

Session 28:

Panel: The Impact of New Technology on Data Communication

2-4:30 pm, Biltmore Music Room

Chairman: Richard A. Gibby, Bell Telephone Laboratories, Holmdel, N.J.

Moderator: George Gilman, Mitre Corp., Bedford, Mass.

The panel will discuss imminent changes in the data communication field resulting from present-day and predictable technological improvements.

28/1 James Babcock, Allen Babcock Computing Inc., Los Angeles.

28/2 Dean Gillette, Bell Telephone Laboratories, Holmdel, N.J.

28/3 Richard Petritz, Texas Instruments, Dallas, Texas.

28/4 Virgil Vaughan, American Telephone & Telegraph, New York City.

28/5 Ted Glaser, Case Institute, Cleveland, Ohio.

28/6 Merlin Smith, IBM Corp., Armonk, N.Y.

28/7 Charles Strom, Rome Air Development AFB, N.Y.

1968 INTERNATIONAL ELECTRONIC CIRCUIT PACKAGING SYMPOSIUM

WESCON 68

August 19 and 20/Statler Hilton Hotel

Monday, Aug. 19

Session 1:

Evaluating Plastic Encapsulated Semiconductors

9:30 am-11:45 am

Moderators: E. J. Lorenz, IBM Corporation, Poughkeepsie, N. Y., C. E. Smith, Lockheed California Company, Burbank, Calif.

1/1 RELIABILITY OF SILICONE ENCAPSULATED INTEGRATED CIRCUITS. R. C. McCoy, Signetics Corporation, Sunnyvale, Calif.

1/2 STATUS OF PLASTIC SEMICONDUCTOR ENCAPSULATION. Dr. Stephen Baird, Texas Instruments Inc., Dallas, Texas.

1/3 CHEMICAL AND MECHANICAL CONSIDERATIONS. Dr. E. D. Metz, Motorola, Inc., Phoenix, Ariz.

1/4 TEST OF PLASTIC ENCAPSULATED SEMICONDUCTORS. E. B. Hakim, U.S. Army Electronics Command, Fort Monmouth, N.J.

Luncheon Speaker: Dr. Morgan Sparks, Bell Telephone Laboratories

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Session 2:

Beam Lead Interconnection Technology

1:15 pm-3:15 pm

Moderators: H. J. Scagnelli, Bell Telephone Laboratories, Whippany, N. J. M. I. Ross, Milton Ross Company, Southhampton, Pa.

2/1 WOBBLE TABLE FOR THERMOCOMPRESSION BONDING BEAM-LEAD SILICON INTEGRATED CIRCUITS. J. E. Clark, Bell Telephone Laboratories, Whippany, N. J.

2/2 CROSSOVERS FOR USE IN HYBRID INTEGRATED CIRCUITS. W. L. Harrod, Bell Telephone Laboratories, Naperville, Ill.

2/3 MECHANICAL THERMAL PULSE MULTIPLE LEAD BONDING. R. H. Cushman, Western Electric Company, Princeton, N. J.

Session 3:

New Hybrid Microelectronic Packaging Techniques

3:30 pm-5 pm

Moderators: G. E. Gless, University of Colorado, Boulder, Colorado. Alfred Levy, RCA West Coast Division, Van Nuys, Calif.

3/1 THERMAL DESIGN PARAMETERS OF MULTICHIP INTER-CONNECTION SYSTEM PACKAGING. Maurice B. Shamash, Westinghouse Electric, Baltimore, Md.

3/2 TERNARY ALLOY ELECTRODE PASTES. L. F. Miller, IBM Components Div., Hopewell Junction, N.Y.

3/3 MICROELECTRONIC INTERCONNECTIONS THROUGH HIGH TEMPERATURE INSULATIONS. S. A. Biroczky, IBM Components Division, Hopewell Junction, N.Y.

3/4 COMPUTER-AIDED HYBRID MICROCIRCUIT MASK LAYOUT PROGRAM. D. M. Meadows, Lockheed-Georgia Company, Marietta, Georgia.

Tuesday, Aug. 20

Session 4:

Packaging Design—Testing and Analysis

8:30 am-10:30 am

Moderators: W. J. Prise, Lockheed Missiles & Space Company, Sunnyvale, Calif. T. A. Telfer, General Electric Company, Utica, N.Y.

4/1 VIBRATION ANALYSIS OF COMPLEX PACKAGED ELECTRONIC EQUIPMENT. S. F. Mercurio, Sperry Gyroscope Division, Great Neck, N.Y.

4/2 EFFECTS OF THE STERILIZATION PROCEDURE ON EMBEDDED ELECTRONIC MODULES. Robert R. Prudhomme, Martin Marietta Corp., Denver, Colo.

4/3 A MULTIPLE ENVIRONMENT TEST SYSTEM FOR COMBINED VIBRATION-VACUUM-TEMPERATURE TESTING. William L. Tierney, Lockheed Missiles & Space Co., Sunnyvale, Calif.

4/4 USE OF SILICONE AND URETHANE IN HIGH DENSITY AND HIGH VOLTAGE PACKAGES FOR SPACE. John R. Dow, Sylvania Electronic Systems, Needham Heights, Mass.

Session 5:

Meeting the Challenge in Electronic Packaging

10:45 am-3:15 pm

Moderators: R. C. Mayne, Jet Propulsion Laboratory, Pasadena, California. E. C. Neidel, Sandia Corporation, Albuquerque, N.M.

5/1 TERMINATING ALUMINUM CONDUCTORS. Timothy Lemke, AMP Inc., Harrisburg, Pa.

5/2 MECHANICAL PACKAGING DESIGN OF ANTENNA CONTROL ELECTRONICS FOR INTELSAT III. Paul E. Hirtle, Sylvania Electronics System, Needham Heights, Mass.

LUNCH, Noon-1:15 pm

5/3 THERMAL CONSIDERATIONS AND TECHNIQUES FOR ELECTRONIC CIRCUIT PACKAGES IN MODERN DIGITAL COMPUTERS. R. C. Chu; M. G. Cohen; J. H. Seely, IBM Corporation, Poughkeepsie, N.Y.

5/4 THE SELECTION OF HOUSINGS FOR ELECTRONIC PACKAGING IN THE SPACE INDUSTRY, James J. Kaufman, Astrionics Laboratory, NASA, Huntsville, Ala.

5/5 QUALITY CONTROL IN SEMICONDUCTOR MANUFACTURING—A PLANT-WIDE APPROACH. John E. Wilford, IBM Corp. Hopewell Junction, N.Y.

Session 6:

Linking the Electronics

3:30 pm-5 pm

Moderators: D. A. Beck, Bendix Research Laboratories, Southfield, Michigan, J. R. Goodykoontz, TRW Systems, Redondo Beach, Calif.

6/1 USE OF FLAT CABLES IN THE SPECTRA 70 COMPUTER. G. R. Gaschnig, RCA Information Systems Division, Camden, N.J.

6/2 PRINTED CIRCUIT CONDUCTOR WIDTHS FOR HIGH CURRENT APPLICATIONS. M. Friar and R. H. McClurg, IBM Corporation, Kingston, N.Y.

6/3 OPTIMUM MULTILAYER TRANSMISSION LINE DESIGN HIGH DENSITY PICOSECOND DIGITAL APPLICATIONS. John J. Surina, RCA, Camden, N.J.

6/4 A PATTERN-GENERATOR SYSTEM HARDWARE/SOFTWARE. Frank E. Grace, IBM Corporation, Poughkeepsie, N.Y.

DESIGNING WITH HYBRID MICRO-ELECTRONICS SYMPOSIUM

WESCON 68

August 21 and 22/Statler Hilton Hotel

Wednesday, Aug. 21

Session 1:

An Introduction to Hybrid Microelectronic Circuits

9:20 am-10:30 am

Moderator: Frank Siegel, Philbrick-Nexus, Canton, Mass.

1/1 HYBRID MICROELECTRONICS TERMINOLOGY AND CLASSIFICATIONS. Stanley M. Stuhlbarg, Raytheon, Company, Bedford, Mass.

1/2 HOW TO GET STARTED IN HYBRID MICROELECTRONICS. Wayne Moyers, Lockheed Electronics, Plainfield, N.J.

Session 2:

Design and Layout of Hybrid Circuits

10:45 am-noon

Moderator: Frank Siegel, Philbrick-Nexus.

2/1 THICK FILM HYBRID CIRCUITS. F. Z. Keister, Hughes Aircraft Company, Culver City, Calif.

2/2 THIN FILM HYBRID CIRCUITS. Harold Larsen, Halex, Inc., El Segundo, Calif.

Luncheon Speaker: Dr. Daniel Noble, Motorola, Inc.

Session 3:

Network Processing

1:30 pm-2:45 pm

Moderator: Jules Rothman, IKOR Corporation, Burlington, Mass.

3/1 THICK FILM HYBRID CIRCUITS. Dr. Henry Nester, Microtek Electronics, Inc., Cambridge, Mass.

3/2 THIN FILM HYBRID CIRCUITS. Dr. C. E. Drumheller, Megadyne, Inc., Rochester, N.Y.

Session 4:

Device and Array Microassembly

3 pm-5 pm

Moderator: Jules Rothman, IKOR Corporation

4/1 DEVICE MICROASSEMBLY — AN OVERVIEW. Michael Ohanian, Oak Electro-Netics Corporation, Crystal Lake, Ill.

4/2 BEAM-LEAD DEVICES. Paul Mallery, Bell Telephone Laboratories, Murray Hill, N.J.

4/3 MEDIUM-SCALE INTEGRATION. W. Peter Dean, Philco-Ford Corporation, Spring City, Pa.

Thursday, Aug. 22

Session 5:

Why Use Hybrid Microelectronics?

9:00 am-10 am

Moderator: Donald Sherman, Raytheon Company, Andover, Mass.

5/1 COST EFFECTIVENESS. E. Ross Mullen, U.S. Navy Air Development Center, Johnsville-Warminster, Pa.

5/2 RELIABILITY. E. F. Platz, IBM, East Fishkill Facility, Hopewell Junction, N.Y.

Session 6:

Packaging of Hybrid Microelectronic Circuits

10 am-noon

Moderator: Donald Sherman, Raytheon Company.

6/1 HYBRID CIRCUIT PACKAGING—AN OVERVIEW. David Nixen, Autonetics Division, North American Rockwell, Anaheim, Calif.

6/2 MICROCIRCUIT PACKAGING AND HERMETIC SEALING. Dr. Gerald K. Fehr, Texas Instruments, Inc., Dallas, Texas.

6/3 ENCAPSULATION. John Hull, Hull Corporation, Hatboro, Pa.

Session 8:

Applications and Case Histories

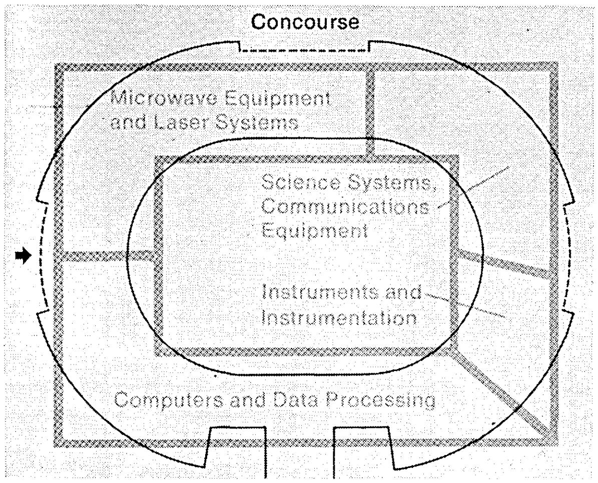
3 pm-5 pm

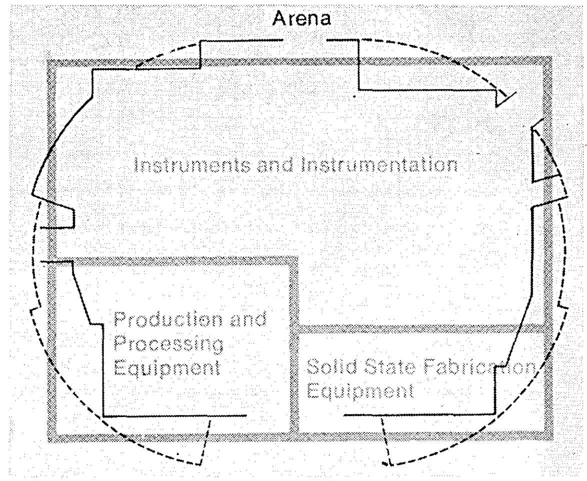
Moderator: Wayne Martin, Zenith Radio Corporation.

8/1 LARGE SCALE USE OF THICK FILMS. Robert R. Leonard, Honeywell Corporation, Waltham, Mass.

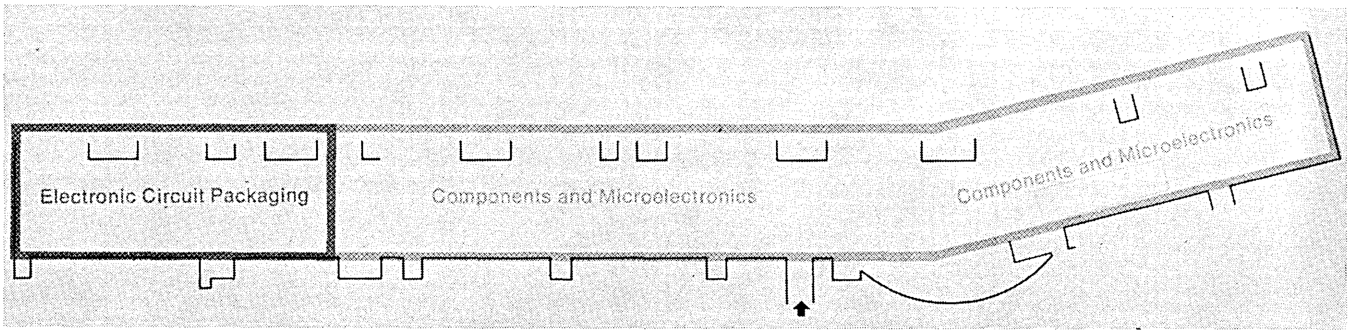
8/2 THIN FILM CIRCUITS. William L. Shockley, Collins Radio Company, Dallas, Texas.

8/3 SPACE APPLICATIONS. J. R. Frissora, Space & Tactical Systems Corporation, Burlington, Mass.





Sports Arena



Hollywood Park

WESCON 68 EXHIBITS

Show hours at the Sports Arena and Hollywood Park

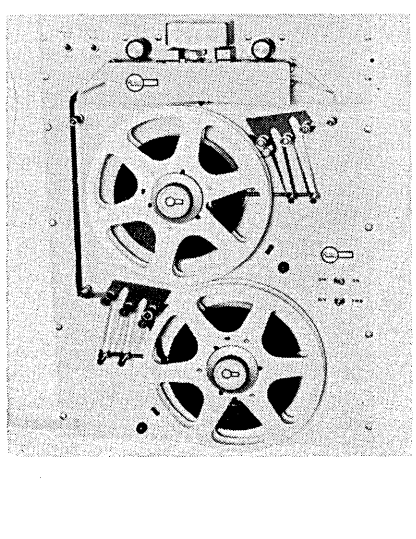
Tuesday, August 20 — 10 a.m. to 5:30 p.m.
Wednesday, August 21 — 10 a.m. to 9:30 p.m.
Thursday, August 22 — 10 a.m. to 9:30 p.m.
Friday, August 23 — 10 a.m. to 5:30 p.m.

PRODUCTS TO BE INTRODUCED AT THE SHOW

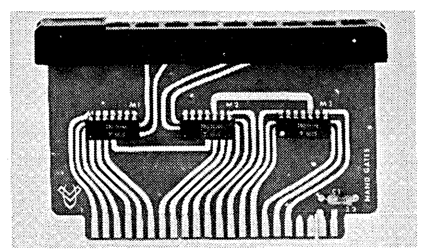
Booth assignments have also been included in the New Product Section in this issue for additional products that will be shown at WESCON.

TAPE READER/SPOOLER

An ultra high speed, photoelectric punched tape reader, model RR-1002, and matching tape spooler, model RS-1000, operate at a reading speed of 1000 characters per second and rewind or search at 2000 characters per second. They are available in unidirectional and bidirectional models with 10½ inch diameter reels having tape storage capacities of up to 2040 feet. The reader is available with several output and drive modes including integrated circuit compatible modes. Remex Electronics, A Div. of Ex-Cell-O Corp., Hawthorne, Calif. See at WESCON Booths 3122-3123.
Circle No. 261 on Inquiry Card.

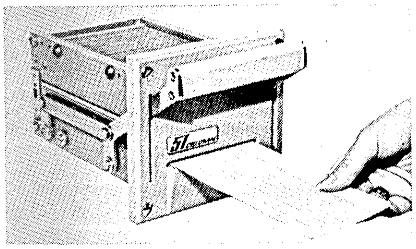


MICROCIRCUIT LOGIC CARDS



A family of TTL microcircuit logic cards designated Type C150 P feature plastic plug-in package integrated circuits. The C150 P Series is electrically and mechanically identical to the standard C150 Series and offers up to 30% savings in price where the hermeticity of a ceramic package is not required. The logic cards cover the complete spectrum of logic functions including: gates, flip-flops, pulse shapers, clock sources, drivers, counters, shift registers, adders, converters, amplifiers, and multiplexers. These logic cards combine the reliability and light, compact features of monolithic circuit modules with standard proven packaging techniques to provide exceptional economy without trade-offs in performance. Control Logic, Inc., Natick, Mass. See at WESCON Booths 182-183.
Circle No. 260 on Inquiry Card.

TAB READER

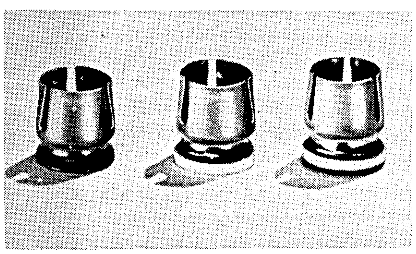


A 51 x 12 tab reader which supplies a full 612 bits from a standard 80 x 12 IBM punched card, is designed for data acquisition, process control and production control applications. The tab reader has an advanced contact system that eliminates unreliable thru-card contacts and prevents lint and dirt from impairing operation. The new design also does away with varying contact resistance caused by the accumulation of contaminants on conventional P.C. switch elements under a punched card.

The unit includes an electrical lockout to prevent contact closure before a card is fully inserted and properly oriented. Units can be supplied with different terminations to fit specific customer requirements. Sealectro Corp., Mamaroneck, N. Y. See at WESCON Booths 204-206.

Circle No. 257 on Inquiry Card.

CUP CLIP HEAT SINKS

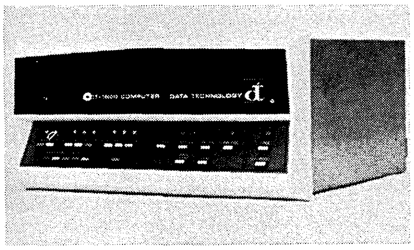


The Series 260 cup clip heat sinks for TO-5 and TO-18 case style transistors, are insulated or non-insulated, with three types of bases. There is a plain mounting base which can be soldered into place, can be epoxy bonded, or can be used with pan head screws. The tapped base and stud mounting base are the other two types of mountings. There are two types of insulated Cup Clips: epoxy insulated for economy and beryllium oxide insulated units for applications requiring low stray capacity to the heat sink.

The cup clips are made of beryllium copper alloy #10 per MIL-C-81021 with brass bases per QQB626a COMP. 22, each having black cadmium plate finish per MIL-QQ-P-416 Type II Class 2. Wakefield Engineering, Inc., Wakefield, Mass. See at WESCON Booth 734.

Circle No. 256 on Inquiry Card.

GENERAL PURPOSE COMPUTER



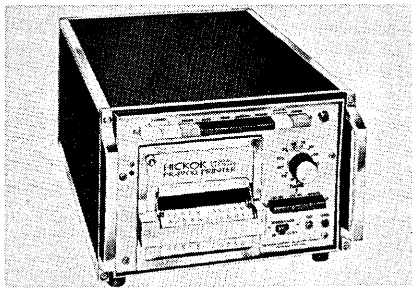
The DT-1600 general purpose, digital computer is an ideal machine for industrial applications where reliability and economy are key user requisites. It features all IC digital circuitry, 17,000 hour MTBF, 8 bits word size, 4K memory (expandable to 16K), small size (8¾ × 17 ×22"), light weight: 28 lbs., and low cost, including complete software.

The machine's memory cycle time was designed at 8 μs to eliminate critical pulse timing problems, especially when communicating with peripheral devices. Large memory cores are used with high threshold level circuits to establish high noise rejection.

A conservative circuit design allows user replacement of any card (including the memory stack) without special circuit tuning. The machine operates reliably to 45°C. The set of 73 instructions are optimized to make input/output and test-and-branch operations extremely flexible, efficient, and easy-to-use. The DT-1600 interfaces directly with DTL integrated circuits. Data Technology Corp., Mountain View, Calif. See at WESCON Booths 3132-3133.

Circle No. 259 on Inquiry Card.

IC DIGITAL PRINTER

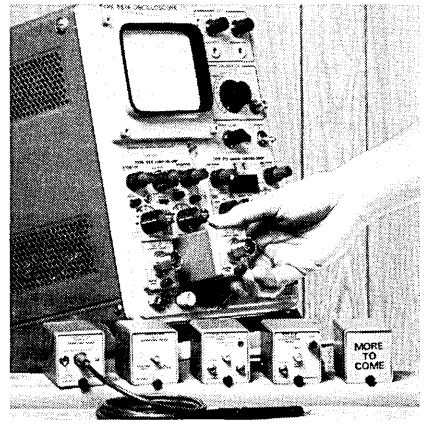


An integrated circuit digital printer, Model PR4900, has been designed primarily as a companion to Hickok's digital measuring system. However, it may be used with any device which provides 10-line decimal or BCD coded data. Voltage, frequency, time period, resistance, capacitance, or event counts are examples of the type of data which can be recorded on the printer. Up to ten lines of numeric and coded data can be printed from one or even two independent digital systems. The print command can be remote, local, or at calibrated time intervals switched in 36 steps from the front panel from 10 seconds to 120 minutes. Maximum print rate from external command pulses is 1 print per second.

Simple ten-line decimal logic is standard for the basic printed input. However, by adding the appropriate decoding board (an internal plug-in), 1248, 1242, 1224 BCD codes can also be used to drive the unit. Print is either by pressure-sensitive paper or by inked impression of standard paper. The Hickok Electrical Instrument Co., Cleveland, Ohio. See at WESCON Booths 1401-1402.

Circle No. 274 on Inquiry Card.

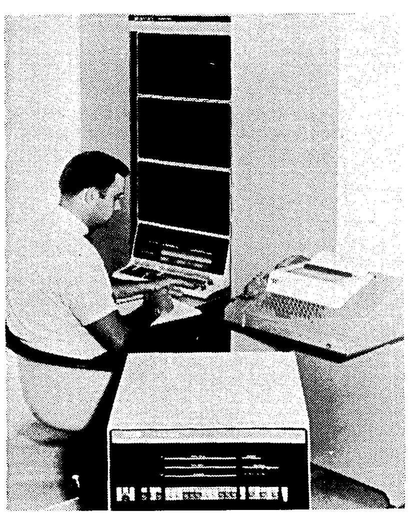
OSCILLOSCOPE SAMPLING HEADS



Four sampling heads provide new measurement capabilities in Tektronix Type 561A, 564, 567 and 568 oscilloscopes. The Type S-4 sampling head features a 25-ps risetime and DC-to-14 GHz bandwidth. This 50-Ω sampling head gives increased detail and resolution making fast pulse measurements. Type S-3 sampling probe head has 350-ps rise-time and an input impedance of 100 kΩ paralleled by 2.3 pF. The Type S-3 is designed to measure high impedance signal sources and is easy to use when probing into miniature circuits.

The Type S-50 pulse generator head has a 25-ps risetime and features high resolution, 25-ps TDR measurement when used with the Type S-4 sampling head. Type S-51, 1-to-18 GHz trigger countdown unit provides stable oscilloscope triggering to 18 GHz and displays to 14 GHz and above with the Type S-4 sampling head. Tektronix, Inc., Beaverton, Oreg. See at WESCON Booths 1606-1612.

Circle No. 281 on Inquiry Card.



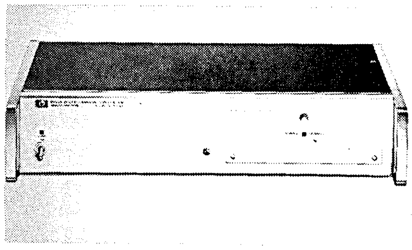
LOW COST COMPUTERS

The PDP-8/L ,the lowest cost, full-scale, 12-bit computer now available, and the 18-bit PDP-9/L are designed for the OEM market and end users in education research, instrumentation and numerical control. The systems feature basic core memories of 4K words, expandable in the 8/L to 8K and in the 9/L to 32K. The 8/L, featuring a 1.6 μsec cycle time, accepts software identical to that of the 8/1 including FORTRAN and DEC's recently announced conversational language, FOCAL. A wide range of peripheral options, such as paper tape readers and punches, card readers, plotter, scopes, DECtape, disk and drum is also available.

The basic 9/L features a 1.5 μsec cycle time and a new Compact Software System consisting of assembler, debugging routines (Octal Debugging Technique and Trace), Editor, Math Package and Utility Programs. Expanded to 8K and larger, the 9/L will accept all PDP-9 software and most of its hardware including DECtape, plotters, data communication devices and A/D and D/A converters. Expanded to 16K and beyond, the 9/L, like the PDP-9, has the capability for background/foreground programming. This allows program development to be conducted concurrent with on-line activities. Digital Equipment Corp., Maynard, Mass. See at WESCON Booths 3178-3181.

Circle No. 263 on Inquiry Card.

DIGITAL-TO-ANALOG CONVERTER



In response to digitally-coded inputs, the Model 6933A digital-to-analog converter generates output voltages in a range between −10 V and +10 V. Voltages can be selected with a resolution of 1 mV and with ±0.01% full-scale accuracy.

The converter will find wide use in automatic systems for supplying test voltages or for operating voltage-controlled instruments. Stepping to a new voltage in less than 20 μs, the converter is especially useful in systems where many tests must be performed quickly. Output is free of switching transients, overshoot is less than 1%.

Of special importance, the digital input ground is isolated from the dc output ground. This makes it possible to ground the controlling equipment without compromising a floating ground at the output. Furthermore, isolation removes the danger of ground loops, which can be troublesome sources of interference in large systems. Hewlett-Packard, Harrison Div., Berkeley Heights, N.J. See at WESCON Booths 1809-1822.

Circle No. 252 on Inquiry Card.

TRANSMITTER/RECEIVER IC's

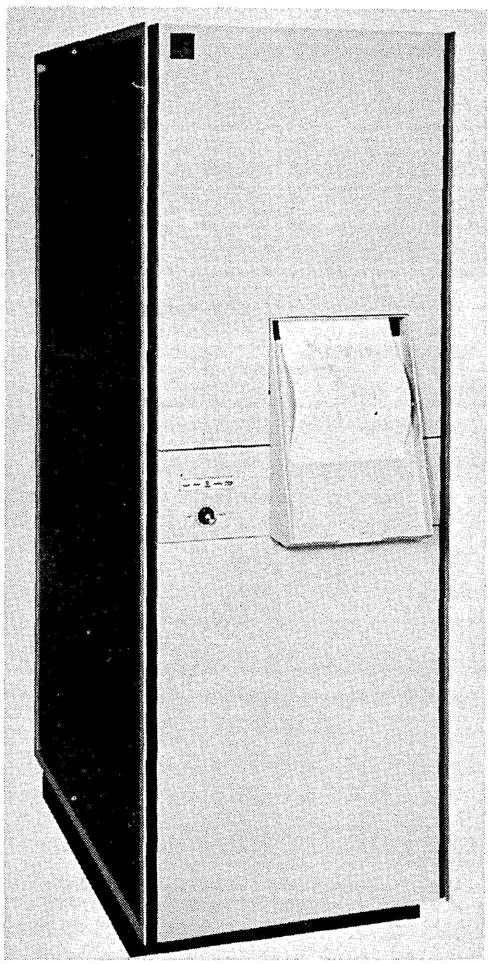
The RA-245 triple line transmitter, and the RA-246 triple line receiver integrated circuits will operate three high-speed data lines up to 30 MHz simultaneously. The units are compatible with all saturated logic IC's currently available. In addition, they feature high-noise immunity, high common mode rejection, insignificant electromagnetic generation and susceptibility, improved speed/power performance, and easily incorporated ground isolation between interfacing equipment, as compared to conventional line drivers now available. Designed to operate over the full military temperature range of −55°C to +125°, the units provide an interface between two systems or subsystems linked together by 50 ohm balanced transmission lines. Terminating 50 ohm resistors are part of the monolithic receiver design. The circuits are available in TO-84 flat packs and ceramic dual in-line packages. Radiation Inc., Microelectronics Div., Melbourne, Fla. See at WESCON Booths 147-148.

Circle No. 265 on Inquiry Card.

HARD-COPY CRT PRINTER

Produces Page Size Prints In Seconds

BETA INSTRUMENT CORPORATION
Newton Upper Falls, Massachusetts



The Model HC610 Betagraphics hard-copy CRT printer produces $8\frac{1}{2}$ x 11 inch prints of computer-generated graphics and alphanumerics in seconds. The paper is exposed by images on the high resolution CRT and developed completely dry, no liquids being used. The Model HC610 is designed to be interfaced to a computer through d/a converters, coupled directly to a display controller or slaved to any other graphical computer display.

The printer may be operated locally or remotely. Upon an EXPOSE-DEVELOP command, the unit delivers a print of the graphical and/or alphanumeric image being produced by the computer in approximately 10 seconds. An EXPOSE command causes exposure, but not delivery until the DEVELOP command is initiated. This allows the Printer to perform graphical data processing by slow image build-up or multiple exposure. The former is useful for data which cannot be displayed at a flicker-free rate on a conventional CRT display due to high image content or speed or memory limitations of the processing computer. The latter is useful for multi-step images from data that requires processing between overlays. The printer can also be used as a remote terminal where hard-copy reproductions of computer-generated data are required. Applications other than computer peripheral include the recording of medical data such as EEG waveforms and the printing of motionless TV images.

PRINTER DESCRIPTION

The printer is a random-access X-Y device with dc-coupled inputs. It features high-speed magnetic deflection, geometry correction of the image and dynamic focus correction of the electron beam. The unit contains a printing module, optical assembly, high-resolution CRT assembly, stable and linear solid-state circuitry and regulated power supplies. The paper is suppied in rolls, and easily loaded from the front of the machine. If required, a viewing screen can be furnished as an option.

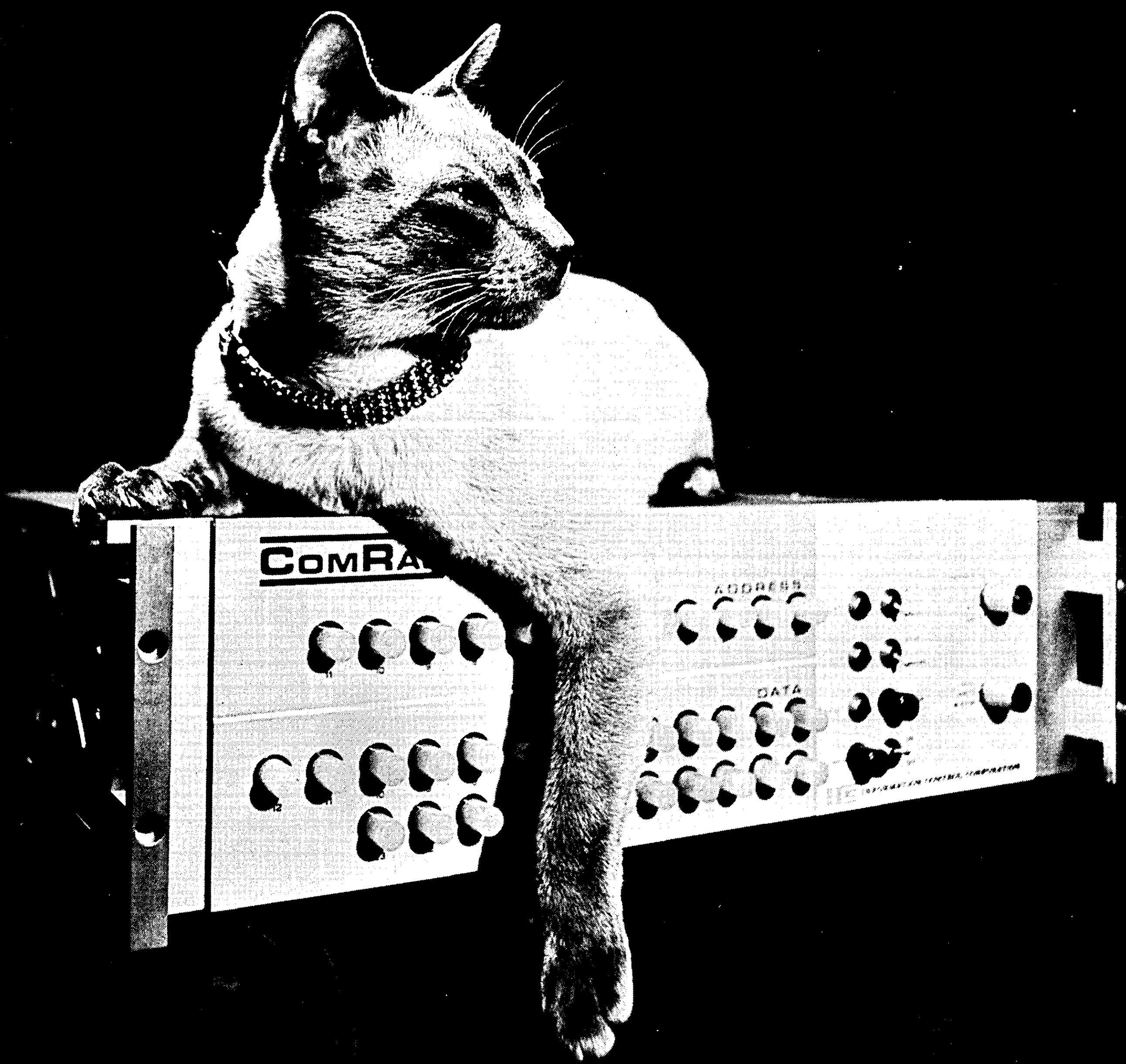
Two deflection inputs are provided for each axis — one for primary positioning, plotting and vectoring, the other for character deflection. Two intensification inputs are provided — one for unblanking, the other for varying the intensity level.

The deflection circuitry features excellent repeatability and linearity. Beam settling time across the 8 x 8 inch copy area is less than 12 μs. The point-plotting rate is 500,000 points per second, the line-writing rate is 2 μs per inch, and the character-writing bandwidth is greater than 1.0 MHz.

OPERATION

Operation is simple, with only three controls in addition to the power switch — an EXPOSE switch for the multiple overlay or slow-buildup mode, an EXPOSE-DEVELOP switch for single exposure, development and delivery, and an exposure TIMER

CAT ON A HOT CORE MEMORY



See Us At Wescon Booth No. 3167

INFORMATION CONTROL CORPORATION

1320 EAST FRANKLIN AVE., EL SEGUNDO, CALIFORNIA 90245 / (213) 322-6930 / TWX (910) 348-6672

(continued from page 76)

(generally left alone once set). Lighted indicators show the operator when the unit is ready for printing and when the paper is depleted. All command and status interface signals are available for remote operation.

SPECIFICATIONS

Image Characteristics

Paper Deflection: Repeatability is ±0.2%; Linearity is ±0.75% and Jitter is ±0.03% where maximum deviation from ideal location is anywhere within useful copy area referenced to full copy width or height. Settling Time to 0.1% of final value anywhere within copy area is 12 μs. Point Plotting Rate is 500,000 points per second. Line Writing Rate is 2.0 μs. per inch. Character Writing Bandwidth is 1.0 MHz. Maximum Character Size for 1.0 MHz bandwidth is .125 inches. Copy Area is 8 x 8 inches. Density Background is approximately .15 and Density Image: 1.5 minimum. Line Width is .020 inches for maximum image density.

Paper Characteristics

The Maximum Print Size is 8½ x 11 inches. Roll Size is 500 feet providing approximately 545 prints per roll. Paper Thickness is .003 inches, with a Shelf Life of 6 months typical. Print Exposure Time is approximately 2 to 3 seconds, with approximately 8 seconds required for Processing and Delivery for a Total Retrival Time of approximately 8 to 10 seconds. Operating Temperature range is 65° to 85°F and Humidity limits are 10 to 60%.

Front Panel Controls and Indicators

Controls include: a Power Switch, Exposure Timer, a continuously variable knob that adjusts the exposure time over a range of 1 to 20 seconds., EXPOSE Switch, a momentary contact type that initiates an exposure., EXPOSE-DEVELOP Switch, a momentary contact type that initiates an exposure, development and paper delivery cycle, VIEW Switch (For units with a view screen only) which unbanks the CRT for visual presentation. Indicators included are a READY Light and a PAPER OUT Light.

Interface Signals for Remote Operation

All interface signals are +3 volts for assertion, 0 volts for negation (compatible with TTL, DCL IC Logic). From the Printer Module: Cycle in progress, Print in progress (paper being exposed), Paper out, and Ready (printer module on and ready for cycle). To the Printer Module: Start expose cycle, Start expose-develop cycle and End exposure (for remote timing).

Inputs

Power: 105-125 volts ac, 57-63 cps, single phase, 2500 watts approximately. Main Deflection: Amplitude — ±5 volts for a full 8 x 8 inch print format and will withstand overload inputs up to ±20 volts. Impedance — 5000 ohms. Secondary Deflection: Amplitude — ±2 volts for a .125 inch character height. Impedance — 5000 ohms. Intensification: Amplitude — +3 or −3±0.5V Unblank, 0±0.5V Blank. Rise & Fall from 10% to 90% points on the output pulse, with a 75 ohm termination — 33ns Unblank, 35ns Blank. Delay from 50% point on the input pulse to 50% on the output pulse with a 75 ohm termination — 3ns Unblank, 20ns Blank. Impedance — 2000 ohms (a 75 ohm removable termination is provided). Gray Level Amplitude is continuous from −5 to +5, −10 to 0 or 0 to +10V. Bandwidth — 300 KHz minimum (to −3 dB point). Impedance — 2500 ohms, minimum.

Mechanical Outline

The printer is packaged in a table-top cabinet and it can be rack mounted if desired. Cabinet dimensions are 22¼″ wide by 63½″ high by 32″ deep. Thirty inches of cabinet height are available for the digital controller and/or interface equipment.

Price and Delivery

The Model HC610 printer sells for $16,500 in quantities of 1 to 4 and $12,425 in quantities of 5 to 9. Delivery is 90 days after receipt of an order.

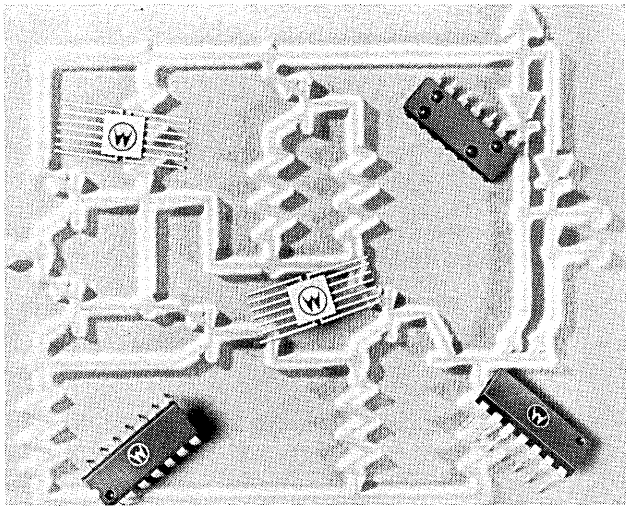
For additional information circle No. 199 on Inquiry Card.

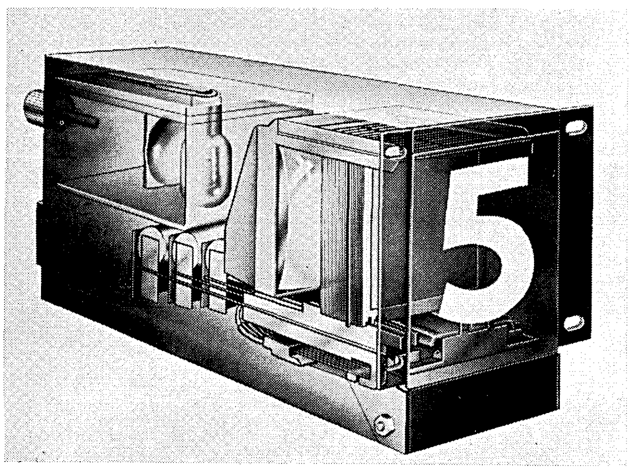
NEW PRODUCTS

TTL LOGIC LINE

The MTTL III line of transistor-transistor logic has speeds approaching the limit of saturated logic and demonstrates improved performance over previous forms of TTL. In addition to five flip-flops and NAND gates, NOR, AND, and OR gates are available, thereby reducing system pack age count by eliminating inverting circuitry when a complementary function is needed. The MTTL III line exhibits a typical propagation delay of 6 ns and a power dissipation of 22 mW per gate. The 18 initial functions in the line are designed for operation over the commercial and industrial temperature range of 0 to + 75°C and are available in the standard dual in-line Unibloc™ plastic package and the 1/4 inch square ceramic flat pack. Known as the MC3000 Series, the commercial circuit line will soon be followed by the MC3100 Series designed for operation over the full military temperature range of − 55 to + 125°C. Motorola Semiconductor Products Inc., Phoenix, Ariz.

Circle No. 200 on Inquiry Card.





BINA VIEW® READOUT

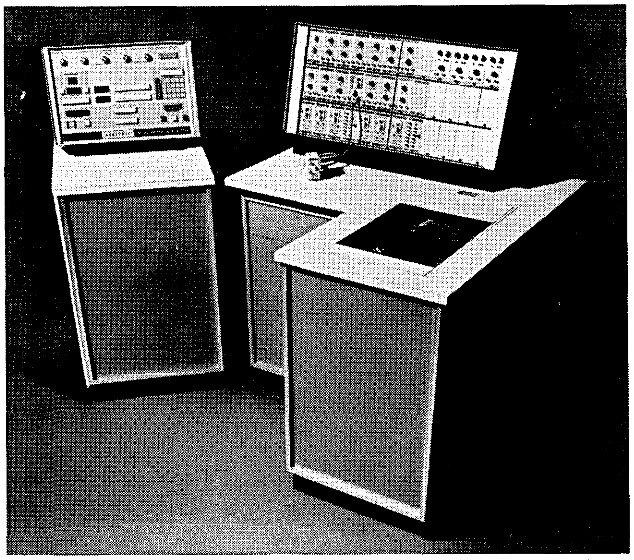
The Bina-View® readout accepts any binary or teletype code up to six bits, does its own decoding and displays as many as 38 different characters or messages, with a standard character height of 1 3/8 inches. It may be driven directly from computers or other electronic equipment, and will operate on as little as 128 mW per bit and 4W per set pulse. This unique readout incorporates built-in memory and will not only continue to display the chosen message when all bit and set pulse power have been removed, but in the case of total power failure, the unit will retain and re-display the last character selected whenever power is restored. The standard displayed character color is white, and average character brightness is 85 foot lamberts when using the recommended 1886 lamp in a unit containing 12 character plates. Average lamp life is 3000 hours. Industrial Electronic Engineers, Inc., Van Nuys, Calif. See at WESCON Booths 566-567.

Circle No. 210 on Inquiry Card.

MEMORY PLANE AND STACK TESTER

The Model 3702 memory plane and stack tester is designed primarily to test 2 1/2D configurations and may be modified with standard options to provide 3D tests. Rise and fall times as fast as 30 ns can be achieved at line-to-line scan rates to five μs. Maximum address-to-address deviation is one per cent. System timing holds jitter to less than ± 0.5 ns or ± 1% and stability to ± 1 % over eight hours. The system automatically store up to 16 errors locations and codes. The stored error locations are used as address skips or can be observed by selecting "cycle on error." The error register's content can be manually interrogated. The tester has an automatic programming mode that allows the system to sequence through selected modes while advancing through pattern selections. It also features a simplified control panel designed to minimize operator error and increase machine efficiency. Honeywell Computer Control Division, Framingham, Mass.

Circle No. 225 on Inquiry Card.

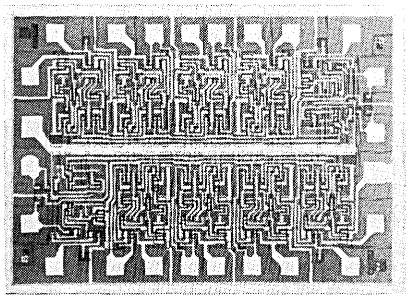



O.K.

NEW PRODUCTS

housing remains in the panel. Lamp replacement can be done in 5 seconds without the use of tools. Constructed of light-weight aluminum and thermoset plastic the weight is held under 0.9 oz. Single or double line engraving on 1 in. and ½ in. lenses are offered. All aircraft color lenses are available with lighted legends or lighted backgrounds. Clare-Pendar Co., Post Falls, Idaho.

Circle No. 213 on Inquiry Card.

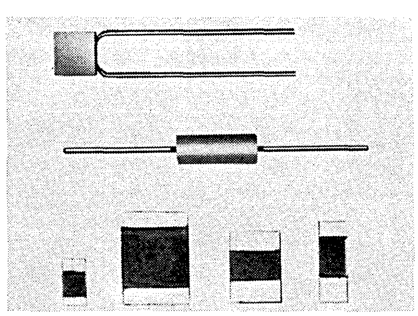


DUAL FOUR-BIT LATCH IC

The 9308 dual four-bit latch monlithic circuit can be used in military, computer, and industrial digital systems requiring high speed performance. The circuit features a latch time of 25 ns. Compatible with current sinking logic, the 9308 provides a multifunctional capability at a substantially lower cost than comparable discrete integrated circuits. The design consists of two independent four-bit latch sections, each with input enabling logic and an asynchronous overriding master reset terminal. High-drive and high-speed performance are achieved by active pull-up "totem pole" outputs.

The 4-bit latch is ideal for use in such applications as data distribution systems, active memory stores, and register-to-register transfer networks. The circuit is available in a 24-lead hermetic Dual In-Line package and flatpack. Fairchild Semiconductor, Mountain View, Calif.

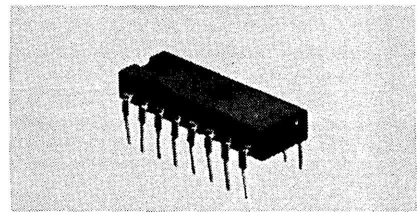
Circle No. 204 on Inquiry Card.



REDUNDANT CERAMIC CAPACITORS

Using an exclusive new floating electrode design, these small ceramic capacitors are said to be the first multi-layer redundant capacitors. They have half the inductance of normal multi-layer ceramic capacitors and improved high frequency characteristics due to the symmetry of design. This new construction technique features two capacitors in series within a single multi-layer structure, providing a high level of assurance against the short-circuit failure mode. They are available in radial or axial cased capacitors, or in "chip" configurations with both High-K (W5P), and High-Q (COG) characteristics. Electro Materials Corp., San Diego, Calif.

Circle No. 211 on Inquiry Card.



BCD TO DECIMAL/DRIVER

A TDD1100 low power monolithic BCD to decimal decoder/driver has been designed for driving gas filled indicator tubes or miniature dc components such as relays and miniature lamps, without the use of additional components. The circuit design utilizes High Level Transistor-Transistor Logic (HLTTL) gating and offers BCD inputs compatible with either HLTTL or DTL output levels. The TD1100 provides a 70 V minimum breakdown voltage at 1.0 mA, which completely eliminates oscillation and unwanted background glow in indicator tubes. The unit is available for operation over the 0°C to 70°C temperature range in either a 16 lead dual-in-line plastic package, 16 lead dual-in-line hermetically sealed ceramic package, or a 22 lead hermetically sealed flat pack. Transitron Electronic Corp., Wakefield, Mass. See at WESCON Booths 352-354.

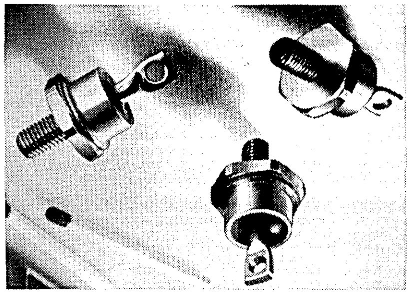
Circle No. 205 on Inquiry Card.

FOUR-BIT MOSFET ARRAY

A complex monolithic MOSFET array, Type HRM2302 consisting of four type D flip-flop and twelve switches, is designed for digital-to-analog and analog-to-digital applications. The array is capable of performing 12-bit conversions at rates of approximately 100 μs. The Type D flip-flop allow DTL voltage levels to selectively set the MOSFET switches in their on or off condition. The .55" x .072" chip consists of 52 MOSFET devices which perform both digital and analog functions. All gate inputs are diode protected, and the device is assembled in a ⅜ run 22-lead flat package. Hughes MOSFETS, Newport Beach, Calif. See at WESCON Booth Island "G".

Circle No. 207 on Inquiry Card.

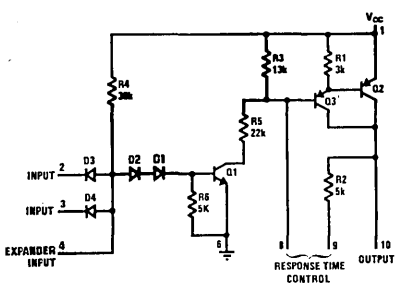
NEW PRODUCTS



VOLTAGE PROTECTED RECTIFIERS

A line of 70 A transient voltage protected silicon rectifiers, designated as the ST-11 series, are available with PIV ratings from 100 to 1000. The units are hermetically sealed in stud mounted cases measuring only 15/16" in height, exclusive of the mounting stud. These high current rectifiers are designed primarily for application in computers, speed controls, power supplies, battery chargers, switch gear, variable drives, motors and generators. Sarkes Tarzian, Inc., Semiconductor Division, Bloomington, Ind.

Circle No. 201 on Inquiry Card.



INTEGRATED RELAY LAMP DRIVER

This integrated relay lamp driver, designated the MH0006C, is designed to accept standard DTL or TTL logic levels and drive a load of up to 300 mA at 28 V. Dual AND inputs are provided long with an EXPANDER connection, should additional gating be required. The addition of an external capacitor provides control of the rise and fall times of the output in order to decrease cold lamp surges or to minimize electromagnetic interference if long lines are to be driven. National Semiconductor Corp., Santa Clara, Calif.

Circle No. 202 on Inquiry Card.

SYSTEMS DISPLAY INDICATOR

A systems display indicator has been created specifically for airborne and weapon support systems. The new design is based on a combined lens carrier and circuit module that is easily removed by hand while the indicator

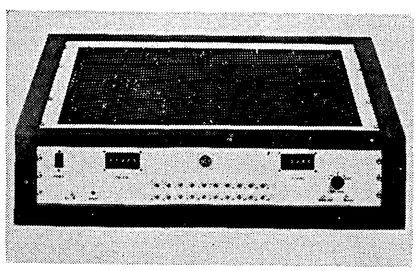
NEW PRODUCTS

POWER TRANSISTORS

These registered high current NPN silicon power transistors are capable of controlling and/or switching a collector current of 100 amps. Identified as the 2N5250 and 2N5251, the package is a 1-1/16" hex, double ended for stud mounting. Combined with the 100 amp current capability is the ability to dissipate up to 350 W. The sustaining voltages are 100V for the 2N5250 and 150V for the 2N5251. These devices have a minimum cut-off frequency; of 10 MHz.

The transistors are characterized by a h_{FE} of 10 to 40 at 70 A and maximum collect current of 100 amps. The saturation voltage is less than 2.5V collector to emitter at 70 A collector current with a base current of 7 A. Total switching speed at 70 amps is 4.0 μs maximum. They are high reliability transistors which meet or exceed MIL-S-19500, and are applicable as high current inverters for power suplies and regulators. Solitron Devices, Inc., Riviera Beach, Fla.

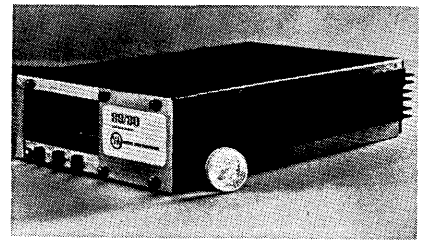
Circle No. 206 on Inquiry Card.



WORD GENERATOR

The Model 22-1 word generator is designed to stimulate MOS large scale integrated circuit devices while under test. The generator provides 22 channels of synchronized digital words at 100 bits per channel and bit rates to 2 MHz. The content of each word is rapidly programmable on a diode matrix board. Minimum setup time and few diodes are required with NRZ (non-return to zero) format. Precise output levels between +15 volts and −15 volts are programmed in 10 mV increments on thumbwheel switches. Sync output to associated equipment is available on a BNC connector. Expanded capability including real time logic, level comparison and multiphase clock are also available. Non Linear Systems, Del Mar, Calif. See at WESCON Booths 1823-1826.

Circle No. 237 on Inquiry Card.



SMALL STORE MEMORY

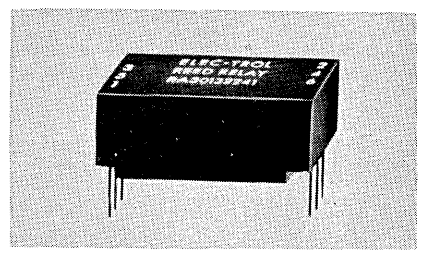
The SS/30 small store, low cost memory is a 4-wire coincident current core memory and is only 8⅝" wide, 3¼" high, and 13" deep.

It features 2.4 μs full cycle time, storage capacity of 512 or 1024 words with word lengths of 8 and 16 bits. Word lengths of 4 and 12 bits are also available as an option.

The memory is ideal for data storage, time buffering between asynchronous systems, code conversion, format conversion, and many other data manipulating operations.

The system provides operation modes of full cycle (clear/write and read/restore) as well as read-modify-write (or split cycle), and half cycle of read only and write only. Other features are buffered single rail address inputs and 600 ns access time. Varian Data Machines, Irvine, Calif. See at WESCON Booths 3004-3008.

Circle No. 226 on Inquiry Card.

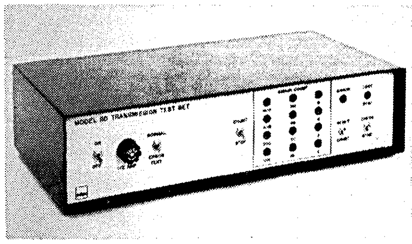


REED RELAY

This miniature sensitive relay was specifically designed to have maximum coil resistance providing minimum contact thermal EMF and minimum operating power; available in 1, 2, 3, 4 and 6 poles; contacts capable of switching dry circuit loads to 10 watts, .5 A maximum current and 250 V maximum switching voltage; epoxy encapsulated to provide protection for coil and contacts. High shock and vibration immunity; terminals on .1 inch grid spacing; electro-magnetic and/or electrostatic shielding available.

Environmental ratings are temperature: −55°C to +85°C (125°C special), vibration: 15 G to 2000 H_z, shock: 150 G, bounce time nominal (ms) 0.25, actuate time norminal (ms) .5 to 1.0, de-actuate time nominal (ms) 0.1, pickup power at 20°C (mW) 26 to 98. Elec-Trol, Inc., Saugus, Calif.

Circle No. 219 on Inquiry Card.



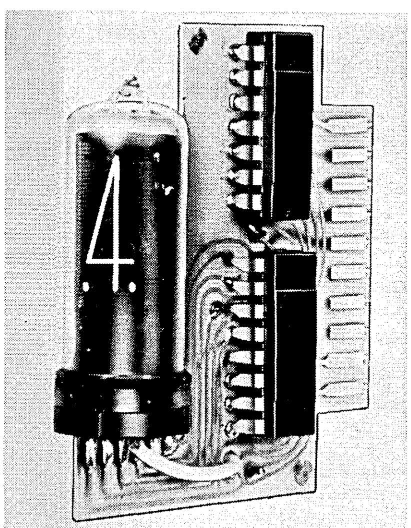
TRANSMISSION TEST SET

The Model 110 transmission test set developed for field testing of data modems is small enough to fit into a standard attache case. It weighs only 8 lbs., and measures 3" high and 12" wide.

The test set evaluates data transmission systems using synchronous modems operating at any speed from 10 to 10,000 bits per second, which are equipped for RS232B/CCITT V.24 interface, supplying their own clock. The unit is solid state throughout, with integrated circuits and silicon devices insuring high reliability in extreme environments.

The unit allows data processing equipment to operate normally during the testing period. The self-contained unit connects directly to the data modem, providing a 2047-bit pseudo-random pattern for transmission. It synchronizes itself with the received digital data stream, detects errors, and displays these errors on front panel lights. Milgo Electronic Corp., Miami, Fla.

Circle No. 231 on Inquiry Card.



IC NIXIE® TUBE DRIVER

The Type BIP-8910-1 driver module, employing integrated circuits is the first in a planned series of drivers for use with the B-5750 series NIXIE tubes. Intended for non-memory (follow) operation, the driver module accepts 4-line positive 8-4-2-1 BCD logic and is compatible with TTL, DTL and RTL circuitry. The B-5750 NIXIE tube has two internal decimal points both of which are available at the module's terminals. The assembly consists of the B-5750 NIXIE tube mounted in a socket at the front of an open printed circuit module. The module has an edge connector with gold-plated fingers at the rear. A receptacle SR-121 is available for use with this module. Burroughs Corp., Electronic Components Div., Plainfield, N. J. See at WESCON Booths 1414-1415.

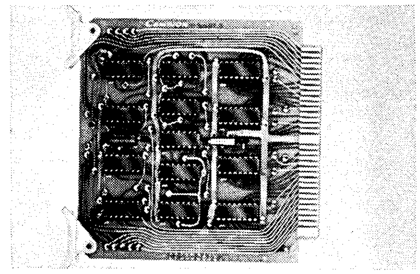
Circle No. 217 on Inquiry Card.

PLUG-IN RELAY

A 3 amp 4PDT plug-in relay is designed for use in computers, data processing, logic systems and business machines. Molded parts are glass-filled diallyphthalate for higher arc resistance. The new 1310 series relay is available ac or dc, plug-in or quick-disconnect, 6 to 115 Vac and 6 to 110 Vdc. Contact rating is 3 amps at 30 Vdc or 115 Vac resistive. Expected life is in excess of 100 million operations dc, 50 million ac. Guardian Electric Mfg. Co., Chicago, Ill.

Circle No. 220 on Inquiry Card.

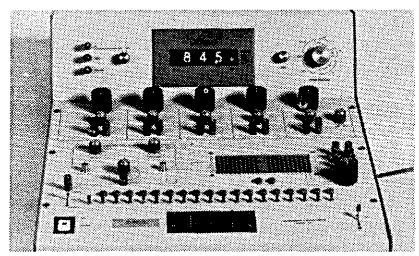
NEW PRODUCTS



IC LOGIC COUNTERS

A BCD single card 4-digit decade counter/Nixie™ driver combination, designated part number 790-2204-01 provides output drivers capable of driving most cold cathode display tubes. The decade counter can operate at speeds of 25MHz. A logic card with 4, 3, 2 or 1 digit is available. Cambridge Thermionic Corp., Cambridge, Mass. See at WESCON Booth 228.

Circle No. 267 on Inquiry Card.



INTEGRATED CIRCUIT TESTER

The Model 718 is a low cost, efficient instrument for manual testing of integrated circuits. Five separate power supplies provide the forcing functions to test a wide variety of circuit types including RTL, DTL, TTL, and MECL. Test connections and metering are made through a flexible programming matrix and convenient lever switches which speed testing and reduce the possibility of error. A built in square wave generator provides dynamic inputs up to 10 MHz.

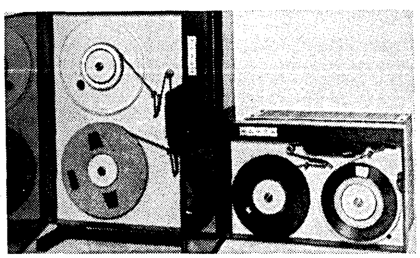
Model 718 was primarily designed for engineering analysis, however, it can be utilized for incoming inspection and quality control. It measures and displays with three decimal readout all the important dc parameters of integrated circuits. All controls and indicators are clearly readable on a sloping front panel, designed to provide a convenient working surface and to prevent operator fatigue. The instrument is packaged in a sturdy, lightweight metal cabinet. Microdyne Instruments, Inc., Waltham, Mass. See at WESCON Booth 3156.

Circle No. 270 on Inquiry Card.

SEMICONDUCTOR TEST SYSTEM

The Model 700 automatic semiconductor test system can perform all transistor dc and pulsed breakdown tests to 1A as well as leakage and forward conduction tests on diodes. The system uses plug-in test modules which can be programmed for up to 12 tests, all performed sequentially at the rate of approximately 12 per second. Programming of bias conditions, test limits and circuit modes is set in by means of controls on the front of each test module. Bin computer programming is by pushbutton matrix. Once programming is set, doors to the test module compartment are shut, and an unskilled operator may take over the routine performance of the testing and sorting devices. Testing may be programmed as Go/No-Go, or to classify devices into bin categories from 1 to 9 plus a zero or "reject" category. Bin selection is indicated by visual numeric readout. The Birtcher Corporation/Instrument Division, Monterey Park, Calif. See at WESCON Booths 1920-1922.

Circle No. 291 on Inquiry Card.

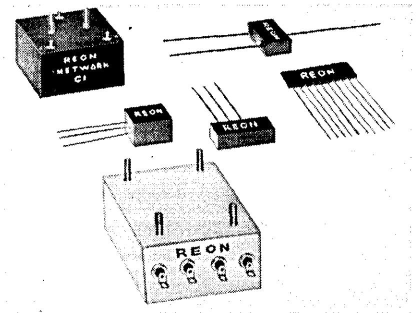


DIGITAL TAPE RECORDERS

A family of high performance incremental and synchronous digital magnetic tape recorders available either with 8½ inch or 10½ inch reels, utilize a single capstan velocity servo system. A number of write and/or read combinations are available. The similarity of design for incremental and synchonous units makes possible the unique hybrid Incremental Write/Synchronous Read model. Thus, a compact single digital magnetic tape unit can accept random data from sources such as keyboards, transmission lines, digital voltmeters, counters, converters, or automatic test systems, and can then read the prepared tape at speed up to 25 ips into a digital computer.

The incremental tape units operate at rates of 1000, 700, 500, and 350 characters a second at densities of 800, 556, and 2000 bits per inch. Synchronous models can be ordered at any single speed from 1 ips to 25 ips at densities of 800, 556, and bits per inch. Peripheral Equipment Corp., Chatsworth, Calif. See at WESCON Booth 2323.

Circle No. 258 on Inquiry Card.



PRECISION RESISTANCE NETWORKS

A series of precision resistance networks with fast rise time and a close temperature coefficient match (1 PPM) are miniaturized, hermetically sealed and available in a variety of configurations. These encapsulated plug-in networks are capable of providing peak performance in ac parameters, voltage division, accuracy vs. temperature, t.c. tracking, and long-term stability.

Specification features include: nominal resistance tolerances to ±.005% (dc), resistance ratio tolerances as close as .001% (dc), long term resistance stability of ±.002% per year, low reactances to provide rise times as low as 50 ns, and temperature coefficients of resistors that track as close as 1ppm/°C from −55° to 125°C. Designed to meet all MIL-Specs and withstand the most severe environmental conditions, the networks offer a broad range of applications, such as ac resistance networks, matched sets, summing networks, RC networks, binary resistive networks and A to D converters. Reon Resistor Corp., Yonkers, N. Y.

Circle No. 286 on Inquiry Card.

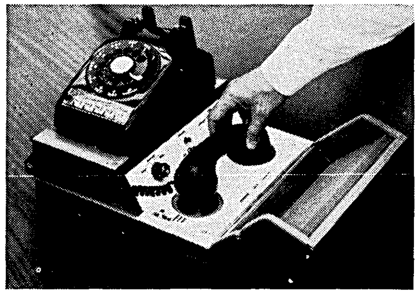
HOT MOLDED TRIMMER

Single-turn trimmers for printed circuit board applications designated Type Y, will fit the commonly used ⅜" space between stacked printed circuit boards. This adjustable resistor features a solid hot-molded resistance element and a molded carbon brush for long life and reliable performance. Operation is exceptionally smooth, and no abrupt changes occur during setting. The enclosure is splashproof and dust-tight, and the metal case is isolated to prevent accidental grounding.

The trimmer is rated ¼ watt at 70°C and available in resistance values from 100 ohms to 5.0 megohms with tolerances of ±10% or ±20%. Standard and special tapers are available. Allen-Bradley Co., Milwaukee, Wis. See at WESCON Booths 428-430.

Circle No. 287 on Inquiry Card.

NEW PRODUCTS



DUAL PURPOSE DATASET

The ADC 300 originate/answer acoustic data coupler meets the need of the user of computer time-sharing to communicate in the "originate" mode with a time-sharing computer from a remote location over ordinary phone lines and also in the "answering" mode with other terminals. In terminal-to-terminal communication, one of the terminals must be in "originate" and the other in "answering" mode.

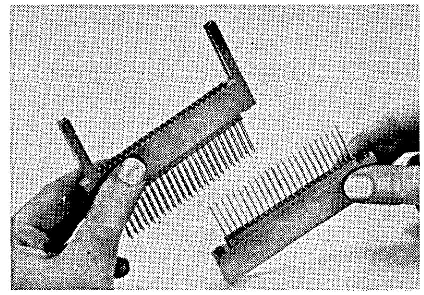
During the day, the user can, in "originate" mode, dial up the computer. Information can also be punched out on tape during the day in an off-line mode and transmitted over phone lines to the computer or to another terminal at low rates in the evening. In full duplex operation, punched tape or keyboard information can be transmitted in both directions simultaneously, thus halving telephone charges. Its data rate is 300 BAUD. Anderson Jacobson, Inc., Mountain View, Calif.

Circle No. 230 on Inquiry Card.

PRECISION RESISTORS

PW4 precision power resistors achieve high power rating in small size without need for expensive special material cores. Volumetric efficiency of the resistors is 266 watts/cu. inch. They have extended resistance ranges and the line covers 1.5 W thru 12.5 W ±1% standard tolerance down to ±.1%. Maximum resistance is 775K ohms, and minimum resistance .3 ohm. The resistors have a temperature coefficient of ±20PPM/°C, and are suitable for general use or applications involving voltage division where precise ratios must be maintained under load. Resistance Products Co., Harrisburg, Pa.

Circle No. 218 on Inquiry Card.

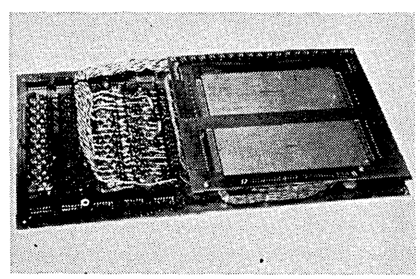


P.C. EDGE CONNECTOR

A 48-contact, double readout printed circuit edge connector has been designed to provide high reliability connections under humid conditions in a salt atmosphere. Special heat-treated and gold-plated berylium-copper contacts are used in this product for resistance to severe environments and for added strength. The contact design provides for very low insertion forces and a larger than normal contact area.

This connector meets the material and workmanship requirements of military specification MIL-C-21097. Contact tails are .025″ square and are spaced .125″ apart. The two rows of contact tails are .125″ apart. Tails are .716″ long. The insulator body can be provided either with or without a card guide. It is also provided with molded-in stainless steel bushings for a size 4-40 screw. Cinch Manufacturing Co., Elk Grove Village, Ill.

Circle No. 212 on Inquiry Card.

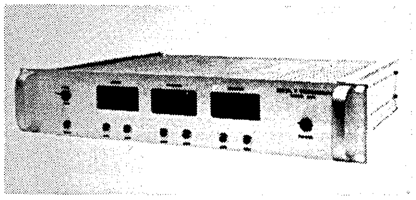


MAGNETIC CORE MEMORY

The Model DC-51 magnetic core memory, measuring 7½″ by 14½″, is a 2¼ D, half cycle random access memory utilizing wide temperature range, 50 mil lithium cores. The cores, address and data drive circuits, sense circuits and timing and control logic are mounted as a single printed circuit package. Address and data registers are optional and are contained on an additional printed circuit board.

The unit was designed for applications requiring inexpensive, non-volatile storage such as CRT Display refresh, data transmission buffering, and data terminals. The maximum capacity available is 512 x 9 or 256 x 18. Datacraft Corp., Ft. Lauderdale, Fla.

Circle No. 227 on Inquiry Card.



DIGITAL CLOCK

The Model 3100 Digital Clock is designed for use as an independent precision time source which provides a visual and electrical indication of time of day or elapsed time. Nixie displays provide a visual indication of hours, minutes and seconds with controls available for manually advancing the count of each individual display. A manual reset switch allows all displays to be reset to zero. A hold control allows the operator to stop the counting sequence and the displays will retain the last reading.
Delta-T Engineering Co., Sarasota, Fla.

Circle No. 288 on Inquiry Card.

INCREMENTAL TAPE RECORDERS

Series 1300 incremental tape recorders permit recording of asynchronous data at rates from 0-300 char/sec to 0-1200 char/sec. Other specifications include a packing density of 200, 556 or 800 BPI and 7 or 9 tracks. All of the requirements necessary to assure compatibility with the IBM 360 computer are provided, including parity, skew, IR gap characters (IRCC and CRCC, IR gap spacing, beginning of tape (load point), erasing and end of file generation. The recorders are designed for 19″ rack mounting and are 12¼″ high by 16″ deep. They weigh 40 lbs. Digi-Data Corp., Bladensburg, Maryland.

Circle No. 290 on Inquiry Card.

NEON INDICATOR LIGHTS

A series of permanent mounted neon indicator lights designated as the E-Lite Series, with and without built-in resistors and including a special version of RFI shielded models, has been designed to meet applicable requirements of MIL-L-3661. Rugged and simple to install, they have aluminum cases with either a black or clear anodized finish, high dielectric insulation and two pin plated turret terminals. Lenses are available in a choice of five colors and a variety of shapes for display requirements. Two basic types are available — The EG group which has only a neon lamp, and the ER group which has a neon lamp and a series resistor packaged within the unit. Eldema, Compton, Calif.

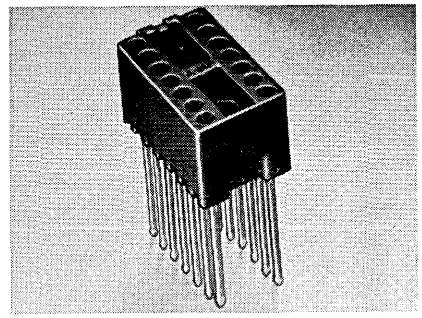
Circle No. 285 on Inquiry Card.

NEW PRODUCTS

DIP HEADER

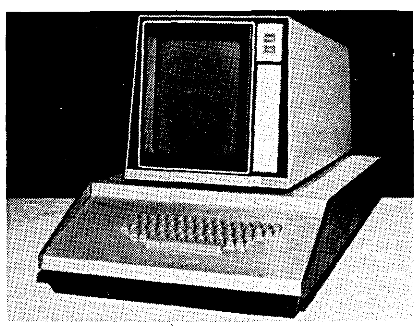
DIP headers with terminations suitable for solderless wrapping or for wave soldering, accept dual in-line packages with round or flat leads from .015″ to .023″. The headers are available loose (for eyelet or screw mounting) or mounted on double-sided printed circuit boards. The solderless wrap posts are positioned to tolerances compatible with automatic machine wiring. The glass-filled nylon headers are available in black and white.

In addition to the contact protection provided by the closed entry design of the housing, the one-piece phosphor bronze contacts have an anti-overstress feature. Available in three lengths (for soldering into multi-layer boards and for two and three level wrapping), the .025″ square terminations are "U" or



channel shaped. Designed in accordance with MIL-STD-1130, this four-corner channel shaped post of spring hardness delivers unusual advantages for wrapped terminations. The contact post plating is hard gold-over-nickel, but tin plating is optional. Other features include the availability of bridging contacts which make direct contact between a post and printed circuitry on the front or back panel. AMP Inc., Harrisburg, Pa.

Circle No. 216 on Inquiry Card.

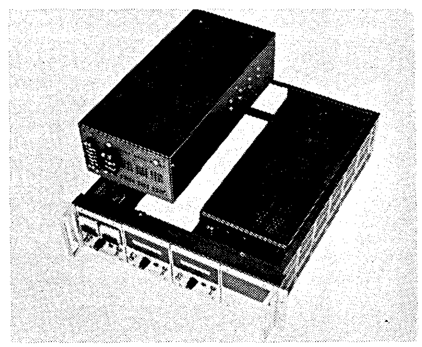


GRAPHIC DISPLAY TERMINAL

ARDS (Advanced Remote Display Station) a self-contained, desk-top console containing a keyboard, vector generator, symbol generator and scope, is capable of displaying over 4000 symbols or an equivalent amount of graphic data in precise detail. Yet all information presented is absolutely free of flicker or drift. ARDS is able to achieve this by use of a direct-view storage CRT.

ARDS is designed to communicate with any computer over a standard telephone line. Its low cost and simplicity make it ideal for the time-sharing environment. A very important feature of the unit is its ability to display to the user line drawings on its CRT. The user may generate these drawings himself for input to the computer or the computer may generate them in response to a request for information. In addition, text may be displayed concurrently with the drawings, put on the screen either by the computer or by the user with a keyboard. Computer Displays Inc., Waltham, Mass.

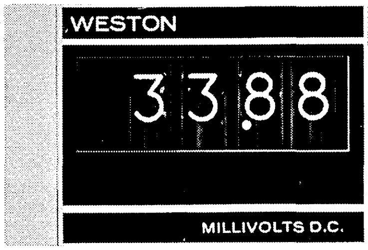
Circle No. 228 on Inquiry Card.



MODULAR POWER SUPPLIES

The EE series power supply offers the highest power available in a half-rack module, up to 150V (at 22A) with current up to 33A (at 3V). A rack adapter, Model LRA-7, designed for use with the EE package, mounts up to two EE modules, or up to eight smaller LM-"A" or LM-"B" modules. The LM-EE power package is all-silicon, programmable, and convection-cooled. There is no heat sinking or forced air required, giving greater mounting flexibility. The unit meets military specifications. Specifications are as follows: line regulation — 0.05% + 4mV; 0.01% + 1.0mV optionally; load regulation. — 0.03% + 3mV; ripple and noise — 1mV RMS, 3mV p-p (0.5mV, 1.5mV p-p optionally); temperature coefficient — 0.03%/°C (0.01%°C optionally); ac input, line — 105-132 VAC, 45-440 Hz; input power — 750 watts; ambient operating temperature: −20° to +70°C. Lambda Electronics Corp., Melville, N.Y. See at WESCON Booths 401-402.

Circle No. 229 on Inquiry Card.



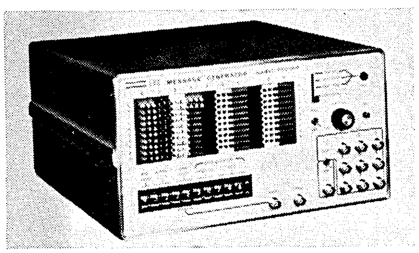
FOUR DIGIT PANEL METER

The Model 1280 digital panel meter, designed with a full four nines presentation, is a true, four digit panel with extremely high accuracy and solid state reliability. It is available in a choice of ten voltage and current ranges, from 100 MV and 10 μa up.

Other features are: accuracy—0.05% F.S. ±1 digit; resolution—1 part in 10,000 (10 μV on 100 mv Range); sample rate—1 per second; BCD J 1-2-4-8 (4 decades); overrange—20% approx. and stability—short term 8 hours—0.05% or less after 1/2 hour warm-up.

Weight is approx. 3 lbs. and dimensions—Front, 3-5/16" × 4-1/8" × 1-1/8" Case (behind panel), 4-15/16" × 6-1/4" × 4-1/2". Weston Instruments Div., Weston Instruments, Inc., Newark, N.J. See at WESCON Booths 2101-2105.

Circle No. 273 on Inquiry Card.



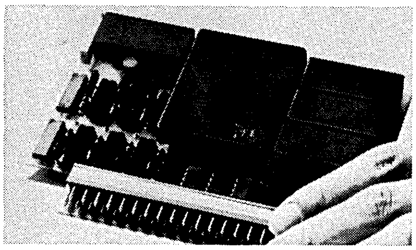
DIGITAL DATA SIMULATOR

The compact Model 912 digital data simulator programs 960 bits of binary information at the front panel, using 320 tiny octal-weighted programing pins. 960 serial bits can be clocked out at rates to 10 MHz. In the parallel mode, up to eighty 12 bits parallel words can be outputed at clock rates up to 5 MHz.

One of the most important applications of the unit is the simulation of computer words. Up to 12 parallel outputs can be generated with a single simulator. To simulate larger parallel words, such as 18 or 24 bits, additional simulators can be synchronized in a master-slave configuration. Other applications include: Checking and/or programing 7 and 9 track magnetic tape units; programing punched tape perforators; and checking IC shift registers where a large number of bits at high clock rates are needed. SRC Div., Moxon Electronics, Los Angeles, Calif. See at WESCON Booth 1914.

Circle No. 269 on Inquiry Card.

NEW PRODUCTS

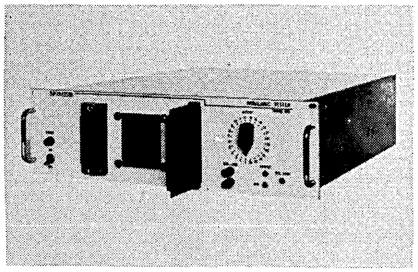


THIN FILM SHIFT REGISTER

The Model 1024S-1 DTPL magnetic thin film shift register is designed to satisfy the non-volatile storage requirements in data transmission and peripheral data processing systems. It has a serial storage capacity of 1024 bits operating at bit rates from 0 to 50 KH_z, requires from 0.5 to 5 watts of power depending upon the bit rate and duty-cycle and includes shifting and input/output electronics. The shift register can be organized for various serial/parallel input/output applications.

Other features of the unit are: asynchronous operation; radiation and shock resistance; modular construction; flexible organization; DTL or TTL interface; high storage density; small size and low cost. Electronics Div., Laboratory For Electronics, Inc., Boston, Mass.

Circle No. 262 on Inquiry Card.

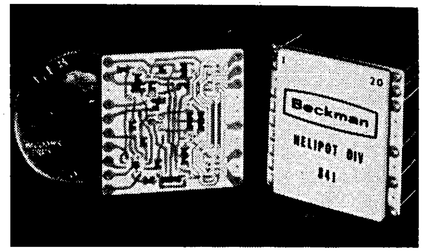


LOGIC CARD TESTER

The Model 872 monilogic card tester has been designed to test logic cards at high speeds, typically 15 seconds per card. The tester internally generates more than forty different combinations of pulses, logic levels and voltages to provide the means for performing functional, dynamic tests on all standard MONILOGIC TTL and DTL cards, some linear and certain types of relay cards.

The unit is used in conjunction with a cathode ray oscilloscope. Thus, all primary power for a complete set-up is 110 V, 60 Hz. Available to the user is a test procedure for each standard DTL and TTL MONILOGIC card. The test procedures include oscilloscope test patterns which permit rapid visual analysis of the card performance while in operation. Monitor Systems, Fort Washington, Pa.

Circle No. 240 on Inquiry Card.



MINIATURE LADDER SWITCH

A miniature thick-film ladder switch Model 841 — is designed for use in digital to analog conversion systems. The switch is compatible with the Model 811 high-speed ladder network and offers four switching sections, each using two bipolar transistors. Switch offsets of 0 to 2 mV and resistance of 4 (±2) ohms make the unit compatible with 12-bit operation. Rise and fall time is typically 200 ns, and load range is 0 to 5 mA. The unit can be actuated by standard RTL, DTL, or TTL inputs. Operating temperature range is −55° to +125°C.

An unusual feature of the switch is its independence of reference voltage. Plus-and-ground, minus-and-ground, or plus-and-minus arrangements may be used without degradation of specifications. Helipot Div., Beckman Instruments Inc., Fullerton, Calif. See at WESCON Booth 2317.

Circle No. 214 on Inquiry Card.

D-TO-A CONVERSION SYSTEMS

Y-Series multichannel digital-to-analog converters are designed explicitly for incorporation into hybrid data systems. The interface is easily adapted to a wide variety of standard computers, with isolation between analog and digital signal domains. The systems are structured to include data distributors (including the interface to the digital computer as well as address logic and transfer control), digital-to-analog converters and/or multiplying digital-to-analog converters. An internal DAC reference power supply that can be slaved to the overall system reference and power system elements available include inversion amplifiers to complement multiplying DAC inputs and permit four-quadrant multiplying, a Control Panel for off-line system test and manual control, and system racks.

Y-Series DAC systems are characterized by their fully integrating system design and include the following performance features: flexible addressing structure for up to 128 channels; single or double buffered input channels; 8, 10, 12, or 15-bit data inputs, in any combination; various output options up to ±100V; and 500 kHz data transfer rate. Adage, Inc., Boston, Mass. See at WESCON Booth 1307.

Circle No. 239 on Inquiry Card.

SAMPLING VOLTMETER

Model 215 uses average rather than peak detection to minimize effects of noise. It will measure the average value of ac signal in 100 μs, sample and hold circuitry, provide dc outputs for analog and digital data handling systems, with up to 2000 samples per second possible. Other features: Measures CW, gated CW or single tone burst; provision for internal sampling delay to avoid measurements during signal transients; direct panel meter readout and dc outputs; compatible with commercially available oscilloscope probes.

Specifications include: Signal frequency range — 100 Hz to 1mHz, Sampling times — 100 microseconds to 10 ms, 1 cycle minimum, Signal input impedance — approximately 1 megohm, Input signal levels — Full scale ranges of 0.0, 0.25, 0.5, 1, 2.5 and 5 volts rms. (up to 5,000 V and 100 A with probes. Input circuit configurations, — Single ended or differential. Accuracy — ±2% of reading ±1/2%FS for single ended input, Sample delay — for eliminating noise or transient effects, and Sample and hold facility — Output hold circuit is transferred to each computed level after sampling and computation. No "discharge" and "reset" action in output signal. Dranetz Engineering Laboratories, Inc., Plainfield, N.J.

Circle No. 238 on Inquiry Card.

DC MOTOR

A .3 HP dc permanent magnet motor, which will deliver its rated continuous output at any speed selected in the range of 4,400 to 10,000 rpm, is available in a wide range of configurations depending upon individual user specifications.

The Type 3100 dc permanent magnet motor, on a 3 1/8-inch diameter frame, also features speeds up to 13,000 rpm with reduced life, and with speeds down to 2,000 rpm at reduced output power. For intermittent duty, outputs up to 1.2 HP can be obtained from the .3 HP motor.

The motor is designed for industrial and aerospace applications requiring a precision lightweight DC motor in conformity with applicable portions of MIL-M-8609

Totally enclosed construction is provided by the precision-machined steel housing. Weight is 5 lbs. maximum, but can be less depending on the configuration chosen. Standard mounting is with pilot and four tapped holes in end bell. Servo or other special mounts are also available. Diehl Division, The Singer Co., Los Angeles, California.

Circle No. 215 on Inquiry Card.

CIRCLE NO. 52 ON INQUIRY CARD

CIRCLE NO. 53 ON INQUIRY CARD

CIRCLE NO. 54 ON INQUIRY CARD

NEW PRODUCTS

MOS-FET NULL DETECTOR

The 2437 null detector is designed as a "drop-in" detector for use with custom-built instrumentation. It features an advanced solid-state circuit, large easy-to-read meter, and all models can be specified for either battery or line operation.

A MOS-FET input chopper is used in the 2437 detector which results in an exceptionally stable zero and low noise ... less than 0.5 μV noise peak-to-peak at 50,000 ohms source resistance. Zero drift is less than 1.0 μV per hour, non-cumulative, after warm up.

Sensitivity is better than 1.0 μV per division all the way to 50,000 ohms source resistance. Below 5000 ohms, sensitivity is greater than 0.5 μV per division. The sensitivity control is continuously adjustable permitting sensitivity to be reduced by a factor of 100 to 1, if desired. Leeds & Northrop Co., Philadelphia, Pa. See at WESCON Booth 1830.

Circle No. 276 on Inquiry Card.

MULTIMETER

A unique feature of the PM-2400 multimeter is its ability to sense, thru the use of logic circuits, "dc (either polarity) or ac" inputs without the need for switching. Another unique feature is its ability to always read upscale. The solid state, multimeter operates 1000 hours on one set of batteries. Ideal for laboratory and production lines, it is self-calibrating and provides 42 direct reading ranges with long, high-resolution scales. Offering unprecedented sensitivity and high accuracy, it automatically measures Current (ac and dc) from 1 u A f.s. (20 n/A/division) to 3A f.s., Voltage (ac and dc) from 100 mV f.s. (2 mV/division) to 1K Vf.s. and Resistance from 0.5 ohms to 50 megohms. Philips Electronic Instruments, Div. of PEPI Corp., Mount Vernon, N.Y.

Circle No. 241 on Inquiry Card.

DIGITAL MULTIMETER

The Type MM110 digital multimeter functions as an integrating digital instrument with facilities for dc voltage, current and resistance measurement. An optional plug-in converter card provides ac voltage and current measurement at frequencies between 25 Hz and 25 KHz. The multimeter provides ac and dc voltage measurement up to 2000V ac, dc current up to 2 amps and dc resistance up to 2 megohms. Each of these five functions is covered in five basic ranges (giving a total of 25 ranges) and a divide-by-two and divide-by-four facility provides an additional 50 ranges.

Accuracy of dc voltage measurement is 0.05% of indication ±0.05% of full-range value. Input impedance on the lower dc voltage ranges is greater than 1000 megohms and resolution on the lowest voltage ranges is 100 μV. The divide-by-two and divide-by-four facility provides full scale accuracy at a half and a quarter full scale, effectively increasing the resolution on the lowest voltage range to 25 microvolts. The ac converter card enables the unit to provide the same facilities for ac measurement as for dc, with an overall accuracy for voltage measurements of 0.2% of indication ±0.1% of full range value. Whittaker Corp., Gencom Div., Plainview, L.I., N.Y. See at WESCON Booths 1519-1520.

Circle No. 277 on Inquiry Card.

IMPEDANCE-COMPARISON BRIDGE

The GS 1681 is a fully automatic, all-solid-state comparison bridge which is direct-reading in impedance magnitude and phase angle. It provides a BCD output representing the impedance of any R, L or C to ±0.005% in ½ second. It can be used in either of two ways. As a manually-operated device, the self-balancing bridge can be used by even relatively unskilled personnel for routine comparison measurements. Or it can form the nucleus of a high-speed, fully automated measuring system. Measured data are presented in both visual digital in-line form with decimal point and measurement units indicated and in 10-digit BCD, 1-2-4-2 coded form for printers and other ancillary equipment. The 1681 will measure impedance-magnitude differences as great as 100%. Phase angle differences up to 1 radian can be measured over a /Z/ range of 2 to 20 megohms. Comparisons can be made to an accuracy of +0.005% with 0.001% resolution. General Radio Co., West Concord, Mass. See at WESCON Booths 1613-1616.

Circle No. 236 on Inquiry Card.

TAPE READERS/REELERS

PTR-60, 70 and 80/90 series photoelectric tape readers and compatible RS series tape reelers are designed for digital data handling communications, numerical control, phototypesetting, and other tape programmed systems. The complete product line offers reading capabilities up to 1,000 characters per second (cps). PTR-60 series readers feaure both unidirectional and bi-directional models operating at speeds to 125 cps. PTR-70 series operates at speeds up to 500 cps. Both are through-the-tape readers. The high-performance PTR-80/90 series utilizes a reflected light principle of reliability in reading any punched tape at speeds up to 1,000 cps. Printer-Reader Business Section, General Electric Co., Philadelphia, Pa. See at WESCON Booths 451-460, Unit "E."

Circle No. 251 on Inquiry Card.

SWITCHES/MATCHING INDICATOR LIGHTS

Momentary action switches (N.O., N.C. or two circuit) and alternate action switches (S.P.D.T. or two circuit) with matching indicator lights are available with snap-in mounting feature. No tools are required for panel mounting — and down-time is reduced to a minimum. Switches and indicators can be used with new low-profile push button caps. Rectangular caps require the same mounting hole needed for most 4-lamp displays.

These new caps, ⅝" round or square and ¾" × 1" rectangular, have ³⁄₁₆" front-of-panel projection. Caps provide fingertip grip for ease of removal. ⅝" caps are offered in a full range of translucent colors, with or without engrave and fill legends.

¾" × 1" rectangular caps can be furnished in a full range of translucent colors; or with clear face with reverse engraving for "positive" reading legends; or with clear face and underlying film disc for "negative" or "positive" reading legends. Caps with hidden legends (visible only when caps are illuminated) can also be obtained. Dialight Corp., Brooklyn, N.Y. See at WESCON Booths 143-144.

Circle No. 255 on Inquiry Card.

Digital-Voltmeters

Catalog 850, provides a complete listing of a line of digital voltmeters and DVM accessories. The spectrum of instruments ranges from the medium-priced Model 4400 up to the top-of-the-line Series 5700, designed for the most exacting systems applications. The 32-page catalog provides an overview of the state of the art in electronic instrumentation. Dana Laboratories, Inc., Irvine, Calif.

Circle No. 301 on Inquiry Card.

Reed Relays

This capability and specification catalog covers complete performance characteristics for 17 models of magnetic reed relays. Also included is information on quality control procedures, reliability applications, electromagnetic and electrostatic shielding, voltage and resistance values over temperature range, and special features available. The catalog provides complete ordering information and part number explanation. Elec-Trol, Inc., Saugus, Calif.

Circle No. 319 on Inquiry Card.

Digital Angle Readout

The data file No. 110, 4-page brochure describes applications and specifications of the A603-5 digital angle readout. The unit is completely electronic providing a simple, reliable and highly accurate method of converting rotational angles to visual and electrical digital formats. The brochure also describes a variety of special adaptations and modifications available such as multiplexing, angle limit alarms, special readouts and multispeed inputs. Astrosystems, Inc. New Hyde Park, N. Y.

Circle No. 322 on Inquiry Card.

Wiring Components

This 38-page catalog of wiring components contains complete product information on the STA-STRAP® harness tying system, cabling tools and accessories; PANDUCT® plastic wiring duct; and spiral wrapping. Also included are price sheets, listing of nationwide sales representatives, and a return card for use in obtaining free product samples and application assistance. Panduit Corp., Tinley Park, Ill.

Circle No. 309 on Inquiry Card.

Ceramic Capacitors

A 10-page catalog covering microminiature ceramic capacitors provides information on epoxy tubular, epoxy rectangular, moulded, wafer and chip type ceramic capacitors. Complete operating specifications and temperature characteristic curves are provided. Detailed charts show unit dimensions for each capacitance offered in each series. Complete ordering information and a coded part numbering system is illustrated. Southern Electronics Corp., Burbank, Calif.

Circle No. 306 on Inquiry Card.

Lited Devices

Catalog, CM-1 describes lited hardware devices designed for easy readability and reference. The opening pages discuss technical aspects of subminiature and miniature lited devices. The product pages that follow begin with smaller assemblies, such as those containing T-1 lamps, and progress through T-1-¾, T-2 and larger T-3-¼ types. Lens endlite assemblies and beam emitters are illustrated. Also included is an index which references applications to product pages. Chicago Miniature Lamp Works, Chicago, Ill.

Circle No. 316 on Inquiry Card.

Logic and Control Modules

A brochure entitled "Solid State Control" describes a line of solid state logic and control modules. It depicts each module and points out the unique features of the line including: color coding according to function, finger tip controls, logic symbology printed on each module face and compactness. A list of solid state accessory equipment is described. Lehigh Valley Electronics, Inc., Fogelsville, Pa.

Circle No. 318 on Inquiry Card.

2 ½ D Memory Arrays

Advantages of mass memory economy, high speed store capacity and low system noise offered by 2 ½D memory arrays are discussed in this 4-page bulletin. Typical specifications of 5 different styles of 2 ½D memory stacks are tabulated by core type and spacing, number of wires, plane type, word and bit size, overall dimensions, cycle time speed, special specifications and/or packaging, and applications. Electronics Div./Memory Products, Indiana General Corp., Keasbey, N. J.

Circle No. 305 on Inquiry Card.

Time-Sharing System

The SDS 945 time-sharing system featuring interactive, conversational service for up to 24 simultaneous users, is described in a 12-page brochure. Software for the system is described, including the following specialized program processors: CAL, BASIC, FORTRAN II, Conversational FORTRAN, QED, TAP, and DDT. Also included are the system's hardware features and potential applications. The standard peripheral units required in the system are listed. Scientific Data Systems, Santa Monica, Calif.

Circle No. 300 on Inquiry Card.

Indicator Lights

A series of indicator lites for a broad range of military, industrial and commercial applications is described in an illustrated, 4-page catalog. Listed are specifications for dome lens, flush lens, short flat lens, smooth lens and fluted lens types in the EG and ER series. The EG series is a neon lamp without resistor and the ER series is a neon lamp with a built-in resistor. Included in the catalog is order information with a table to allow for choice of lamps, choice of resistor and recommended resistor values. Eldema, Compton, Calif.

Circle No. 310 on Inquiry Card.

Printed Circuit Connectors

This 24-page catalog features photographs, line drawings, electrical characteristics and mechanical specifications on over 3000 different printed circuit connectors. Included in Catalog PC-4 are: complete data on standard and multiboard PMT lines of precious metal tip connectors, card guides, snap-wrap and mini-wrap modular connectors, plugs and receptacles and miniature PC configurations. A selection guide provides information necessary for finding the right connector for any printed circuit board application. Amphenol Industrial Div., The Bunker-Ramo Corp., Broadview, Ill.

Circle No. 302 on Inquiry Card.

Frequency Counter Selection Guide

A 6-page brochure lists 22 electronic frequency counters in a chart that simplifies comparison, making it easier to select the best choice for particular applications. Easily determined are frequency range, input characteristics, time base stability, price, and basic functions (e.g., frequency, period average, time interval, etc.). Another chart displays graphically the frequency ranges of available frequency extender plug-ins. Also described are special instruments, such as preset and reversible counters, automatic frequency dividers, and digital-analog converters. Hewlett-Packard Company, Palo Alto, Calif.

Circle No. 315 on Inquiry Card.

DC Motors

Size 9 Series 9DA, permanent magnet DC motors are described in this bulletin. Also provided are applications, specifications, a performance chart, dimensional drawings with wiring diagram and available accessories. The units, designed primarily for precision airborne accessory equipment applications, are finding wide acceptance in a variety of other applications where size, weight and the ability to perform at extreme environmental levels are critical parameters. Electro-Mechanical Group, American Electronics, Inc., Fullerton, Calif.

Circle No. 317 on Inquiry Card.

Teleprinter Data Terminals

DATAPORT™ VDT-2 and VDT-1 portable teleprinter data terminals are described in a 4-page brochure. The computer terminals include a teleprinter, an electronic control module, and a telephone coupler in two luggage-type cases, that can be carried on trips, then acoustically or magnetically coupled to an ordinary telephone. Design features contributing to the operating ease of the data terminals are illustrated and described. The automatic answering and hang-up feature of the VDT-1 is also highlighted. The brochure lists complete specifications. Vernitron Corp., Data Devices Div., Farmingdale, N.Y.

Circle No. 304 on Inquiry Card.

Circuit Card Guide

This data sheet describes a snap-in circuit card guide, a one-piece molded nylon unit designed for mounting on pre-drilled 1/16″ or 3/32″ metal plates. Obtainable in six lengths, ranging from 2.500″ to 6.500″, the guides also come in three different mounting pin spacings ranging from 1.500″ to 5.000″, and three card retention lengths ranging from 1.000″ to 4.500″. The guides, made of nylon-white, per MIL-M-20693, Type 4A, may be staggered for multi-row applications, and provide a 0.12 clearance in excess of card width. Scanbe Manufacturing Corp., Monterey Park, Calif.

Circle No. 321 on Inquiry Card.

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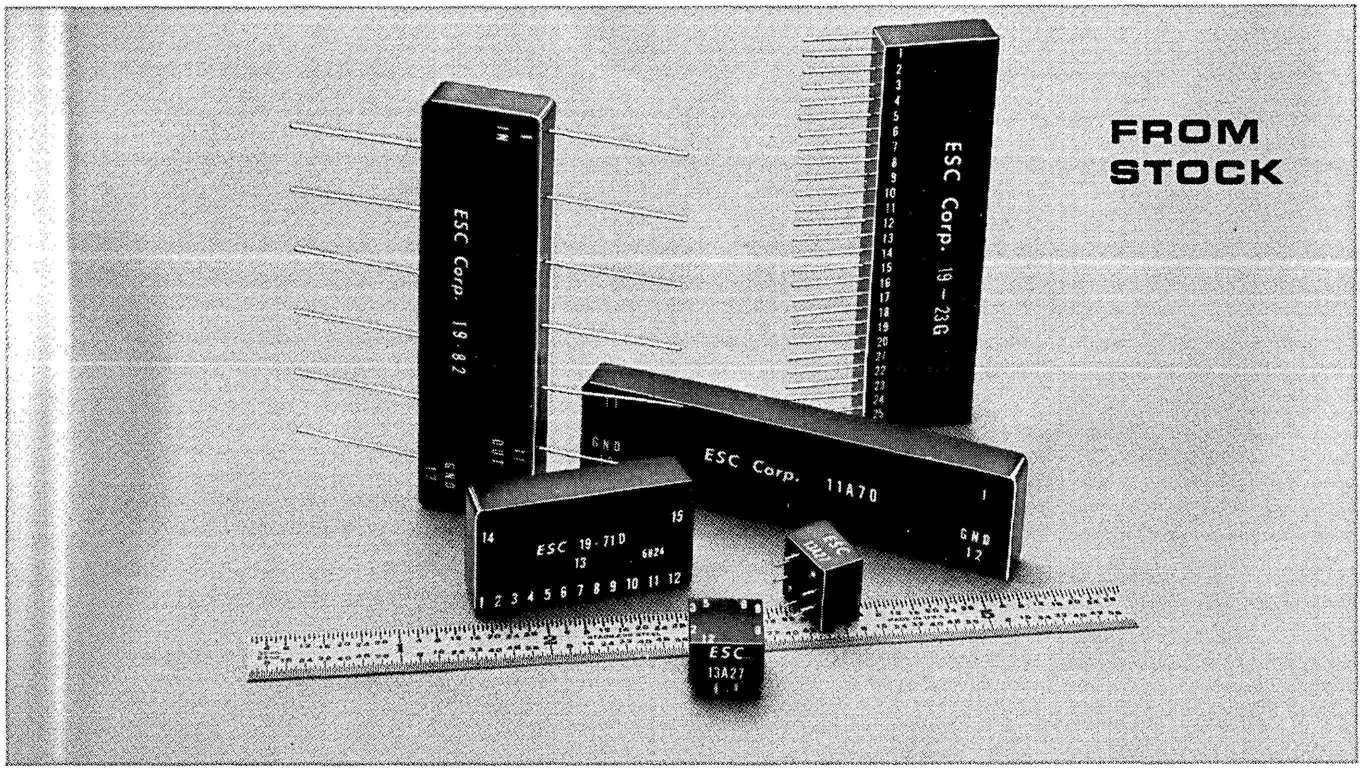
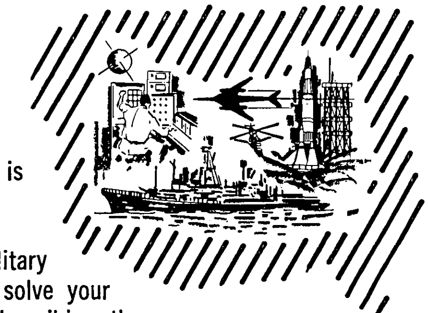
NEW! LOW COST

DELAY LINES



FOR DIGITAL CIRCUITRY



ESC's new Digit-Line series of epoxy molded delay lines contains 17 different types covering a range of delays from 7 to 1000 nanoseconds. This series exhibits relatively fast pulse rise time, exceptionally fine pulse fidelity and low attenuation. Impedance is approximately 100 ohms. Most important is the versatility of these units due to their fine resolution taps, or adjustable sections. The smallest unit in the series is only .490″L x .490″W x .370″H. All of the units will meet the most frequently encountered military specifications. ESC's staff of nine design engineers will also be pleased to help you solve your custom delay line and filter problems. Write today for our comprehensive brochure describing the physical and electrical characteristics of our new Digit-Line series.

ESC ELECTRONICS CORPORATION

a subsidiary of Simmonds Precision

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World's Leading Producer of Delay Lines

The parts we took out–gears, belts, pulleys, and pinch rollers–put reliability into Tally photo readers.

Tally faced the moving parts dilemma by replacing most of them with three low-inertia servomotors to create a fast, smooth, quiet and more reliable photoelectric tape reader. The motors attach directly to the capstan wheel and the reeling, eliminating all troublesome gears, belts, pulleys and pinch rollers. No adjustments are necessary. Maintenance is greatly reduced and accurate read out over long periods of time can be expected.

Tape movement through the read head is in exact accordance with the rotation of the motor armature. The high speed response of the motor allows a great variety of reading operations by merely controlling the current applied to the motor terminal.

It's fast. Searches at 1,000 characters per second. Reads synchronously at any rate up to 500 char/sec and stops before the next character. Reads asynchronously under control of external signals at any rate up to 200 char/sec. Runs in either direction in all modes.

It's easy on the tape. The smooth, quiet action of the servo-controlled reels eliminates tape breakage, reduces tape wear and prevents reading errors.

It's offered with many options. Many optional configurations are available, including recessed mount, flush mount, integral reeling, external reeling, and fully militarized construction.

For complete information contact Tally Corporation, 1310 Mercer Street, Seattle, Washington 98109. Phone (206) MA 4-0760. In the U.K. and Europe address Tally Ltd., 6a George Street, Croydon, Surrey, England. Phone: 01-686-6836.

See us at WESCON '68 → **TALLY**

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