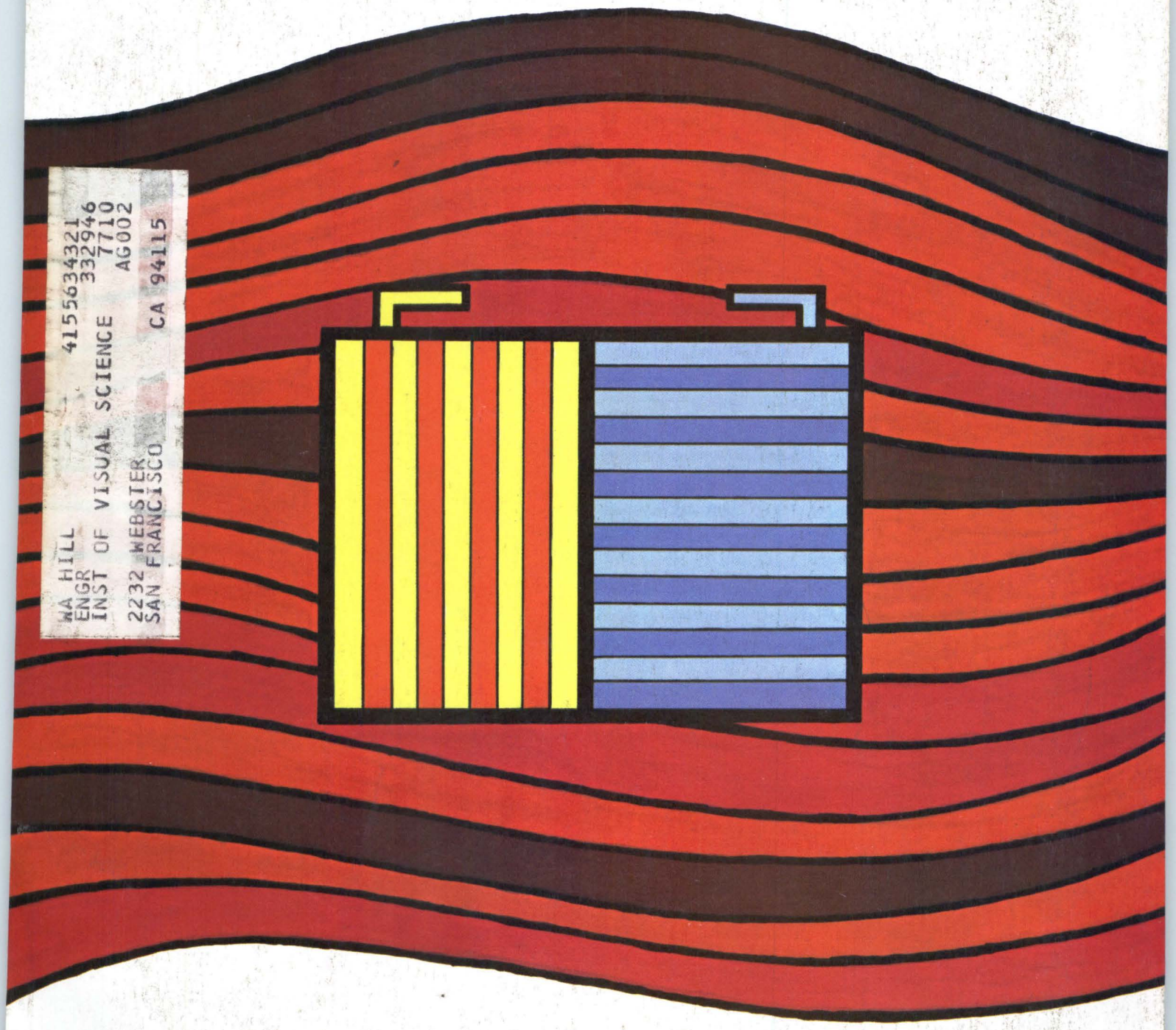
COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1979



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CIRCLE 3 ON INQUIRY CARD

COMPUTER DESIGN

THE MAGAZINE OF DIGITAL ELECTRONICS

AUGUST 1979

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DEPARTMENTS

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FEATURES

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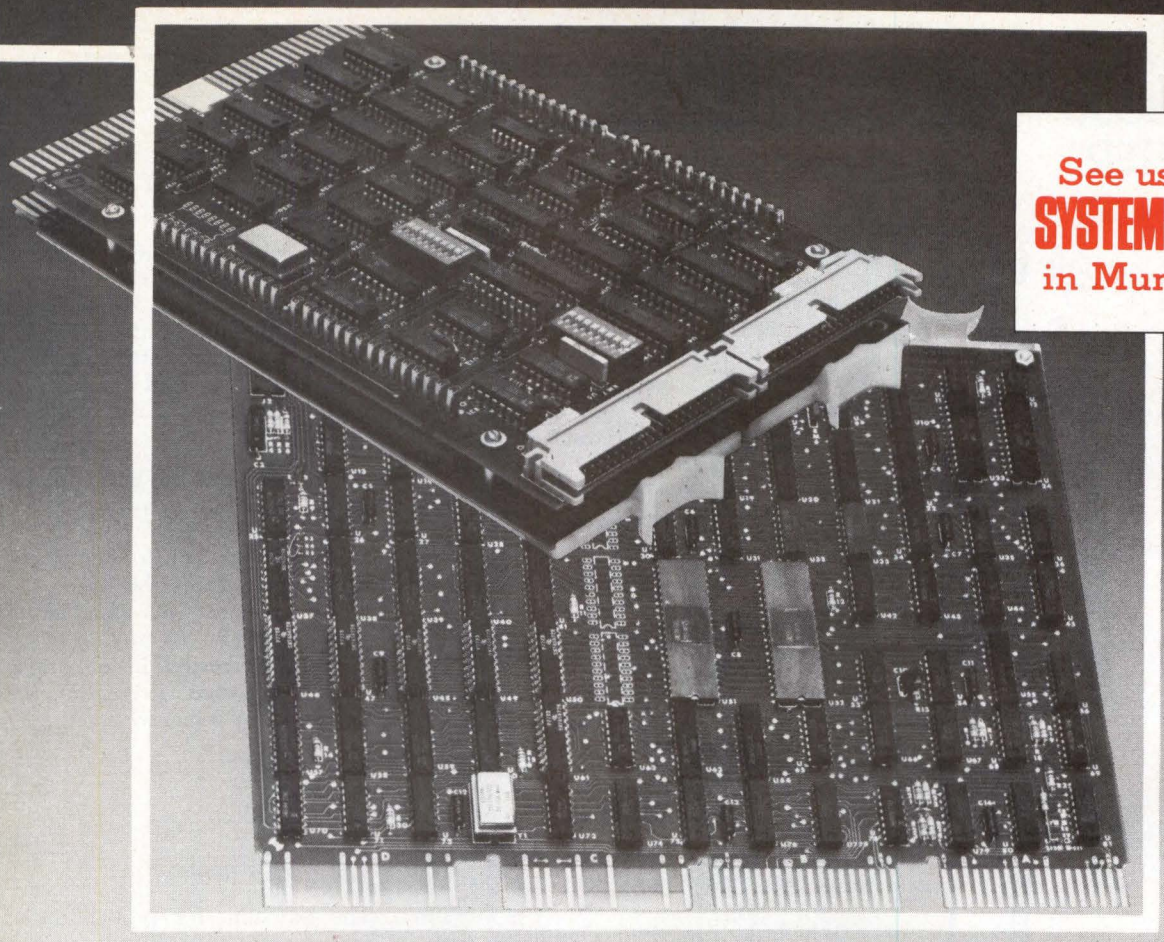

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CIRCLE 5 ON INQUIRY CARD

LETTERS TO THE EDITOR

To the Editor:

Messrs Bhargava and Chandra ("Logic Variable Format Techniques for Efficient Process Control I/O," *Computer Design*, May 1979, pp 203-211) seem to be trying to write around some of the clumsier aspects of the 8085 instruction set. Use of the SET, RES (reset bit), and BIT (test bit) instructions in the Z80 instruction set would greatly simplify and shorten all of the algorithms in the article, eg for LK = LA • LB • LC

```
        BIT 6, (IX + 0)      ;test LA
        JRZ ZERO
        BIT 4, (IX + 1)      ;test LB
        JRZ ZERO
        BIT 3, (IX + 2)      ;test LC
        JRZ ZERO
ONE:    ...
ZERO:   ...
```

The bit numbers and index offsets are arbitrary. Note that this coding is easily read, and does not disturb any registers, unlike the 8085 coding which destroys the accumulator. Also, the decision portion of the code is only six bytes in length.

The Z80 instruction set is superior to the 8085 for any operations involving logical constructs and/or memory manipulation. Inasmuch as it is also less expensive than the 8085, doesn't multiplex address and data, and contains onchip dynamic memory refresh, it would seem a much wiser choice for process control applications.

Richard A. Rodman
Envo, Inc
Vienna, Va

To the Editor:

The floating point working group of the IEEE Computer Society's Microprocessor Standards Subcommittee has been working on a proposed standard for microprocessor floating point arithmetic.

Several innovative and controversial proposals have been discussed but so far none has been widely circulated outside the working group.

Persons interested in receiving the current working documents for the various proposals may write to me.

David Hough
PO Box 384
Wilsonville, OR 97070

To the Editor:

There is an erroneous equation in Ronald Zussman's article "Predicting Queue Performance On A Programmable Handheld Calculator" (*Computer Design*, Aug 1978, pp 93-100). The equation in error appears on page 94 as "Probability of response time exceeding T":

$$P(TR>T) = e^{-uT}(1+(B/s))$$
$$((1-e^{-us\,T(1-U-(1/s))})/(1-U-(1/s)))$$

Notice that if T is set to zero this equation produces the result P(TR>T) = 0 whereas the equation should produce P(TR>T) = 1.

I am interested in obtaining the correct equation, preferably with a derivation or reference.

John Pustaver
Raytheon Co
Sudbury, Mass

The Author Replies:

The equation for probability of response time exceeding T (*Computer Design*, Aug 1978, p 94) should be corrected as follows: remove right parenthesis in middle of equation, and add right parenthesis at end of equation. The corrected equation should read:

$$P(TR>T) = e^{-uT}(1+(B/s)$$
$$((1-e^{-us\,T(1-U-(1/s))})/(1-U-(1/s))))$$

The calculator program has been verified and is correct.

The reference requested is "Introduction to Operations Research," Churchman, p 406, Eq 42.

Ronald Zussman
Securities Industry Automation Corp
New York, NY

Letters to the Editor should be addressed:

Editor, Computer Design
11 Goldsmith St
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CIRCLE 7 ON INQUIRY CARD

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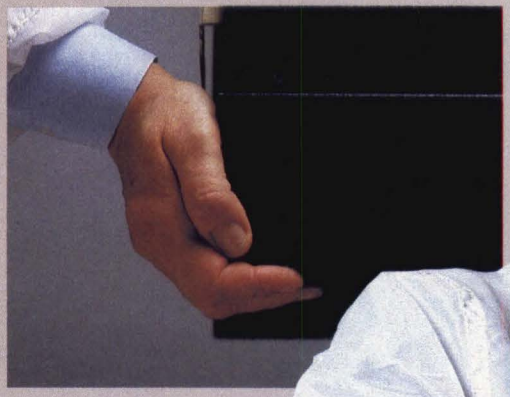
Unlike competition, it has a tunnel cover which keeps contaminants from reaching the pack area.

What's more, the Hunter reminds operators not to leave the cartridge bottom cover out to gather contaminants during operation.

And finally, the Hunter clean air seal isn't broken when the drive is serviced. (The competition's seal must be broken just to replace a fuse.)



Hunter wins hands up.

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MPETITION IN DUST.

servo surface to position on the cartridge disk. Seeks are faster and surer than the competition by a time factor of more than 13 to 1.

Our loader is really tops.

The Hunter cartridge receiver is as simple as can be.

Complex mechanisms with bearings, rods, plates and switches just aren't needed.

On the top-loading Hunter, gravity does the loading. And gravity behaves the same way time after time.

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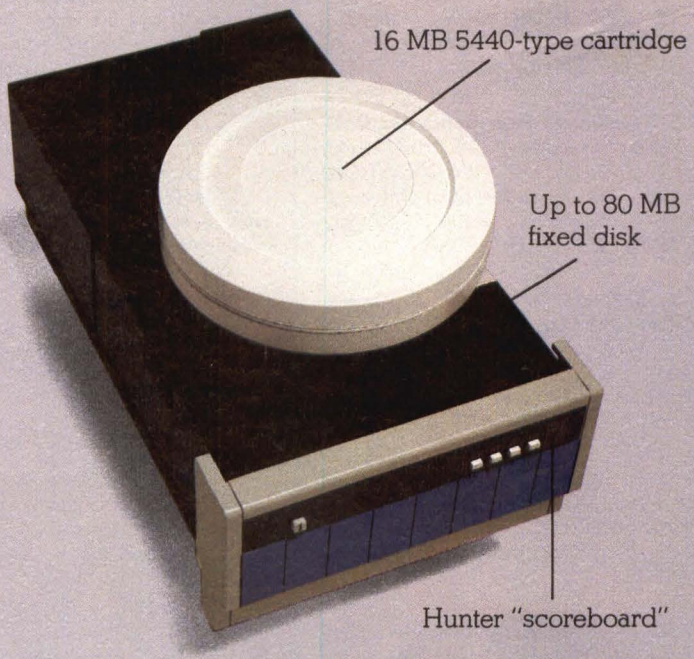

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CIRCLE 8 ON INQUIRY CARD

CALENDAR

CONFERENCES

SEPT 4-7—COMPCON, Washington, DC. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901

SEPT 5-7—Internat'l Fiber Optics and Communications Exposition, Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Michael A. O'Bryant, Information Gatekeepers, Inc, 167 Corey Rd, Suite 111, Brookline, MA 02146. Tel: 617/739-2022

SEPT 6; SEPT 26; AND OCT 10—Invitational Computer Conf, Palo Alto, Calif; Minneapolis, Minn; and Newton, Mass. INFORMATION: B. J. Johnson & Associates, 2503 Eastbluff Dr, Suite 203, Newport Beach, CA 92660. Tel: 714/644-6037

SEPT 18-21—WESCON, Brooks Hall and St Francis Hotel, San Francisco, Calif. INFORMATION: William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

SEPT 25-27—Mini/Micro Computer Conf and Expo, Anaheim, Calif. INFORMATION: Robert D. Rankin, 5528 E LaPalma Ave, Suite 1, Anaheim, CA 92807

SEPT 25-28—Euro IFIP, The European Conf on Applied Information Technology, Wembley Conf Ctr, London, England. INFORMATION: Euro IFIP 79, Box 46, Cleveland Rd, Uxbridge, Middlesex UB8 2DD, England

SEPT 28-30—Northeast Personal and Business Computer Show, Hynes Auditorium/Prudential Ctr, Boston, Mass. INFORMATION: Northeast Expositions, PO Box 678, Brookline Village, MA 02147. Tel: 617/522-4467

OCT 2-5—Internat'l Conf on Distributed Computing Systems, Huntsville, Ala. INFORMATION: B. D. Carroll, Electrical Engineering, Auburn U, 207 Dunston Hall, Auburn, AL 36830. Tel: 205/826-4330

OCT 3-5—Internat'l Conf on Very Large Data Bases, National Hotel, Rio De Janeiro, Brazil. INFORMATION: Prof Stanley Y. W. Su, 500 A Weil Hall, U of Florida, Gainesville, FL 32611. Tel: 904/392-2371

OCT 8-9—Sym on Hardware Descriptive Languages, Palo Alto, Calif. INFORMATION: Waldo Magnuson, Lawrence Livermore Labs, PO Box L-156, Livermore, CA 94550. Tel: 415/422-9550

OCT 9-11—Compusign, Anaheim, Calif. INFORMATION: Golden Gate Enterprises, Inc, 1307 S Mary Ave, Suite 210, Sunnyvale, CA 94087. Tel: 408/735-1122

OCT 9-13—U.S. Computers and Peripheral Equipment and Electronic Computers Catalog Exhibition, Ineltec Fair, Basel, Switzerland. INFORMATION: Caroyln Swope, Catalog Exhibitions Section, U.S. Dept of Commerce, Industry and Trade Administration, Washington, DC 20230. Tel: 202/377-3973

OCT 14-17—Electronic and Aerospace Systems Convention (EASCON), Stouffer's Inn, Washington, DC. INFORMATION: William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

OCT 17-18—Connector Sym, Hyatt House, Cherry Hill, NJ. INFORMATION: Electronic Connector Study Group, Inc, PO Box 1428, Camden, NJ 08101

OCT 22-24—Computers in Aerospace Conf, Hyatt House Hotel, Los Angeles, Calif. INFORMATION: Richard R. Erkeneff, McDonnell Douglas Astronautics Co, Dept 236, Bldg 13-3, 5301 Bolsa Ave, Huntington Beach, CA 92644. Tel: 714/896-4975

OCT 23-25—Semiconductor Test Conf, Hyatt House, Cherry Hill, NJ. INFORMATION: Tess Mitchell, PO Box 38, Collegeville, PA 19426. Tel: 215/489-9387

OCT 29-31—Sym on Foundations of Computer Science, San Juan, Puerto Rico. INFORMATION: Prof Ronald V. Book, Dept of Math and Computer Science, U of California, Santa Barbara, CA 93106. Tel: 805/961-2778

OCT 30-NOV 1—CAD/CAM VII at Automated, Integrated Factory of Tomorrow Conf, Cobo Hall, Detroit, Mich. INFORMATION: Jeff Spire, SME Technical Div, PO Box 930, Dearborn, MI 48128. Tel: 313/271-1500, X405

OCT 30-NOV 1—Interface West, Anaheim Convention Ctr, Anaheim, Calif. INFORMATION: Interface Group, 160 Speen St, Framingham, MA 01701. Tel: 617/879-4502

NOV 5-7—Asilomar Conf on Circuits, Systems and Computers, Asilomar Hotel and Conf Grounds, Pacific Grove, Calif. INFORMATION: Donald E. Kirk, Naval Postgraduate School, Monterey, CA 93940. Tel: 408/646-2081

NOV 5-8—Computer Software and Applications Conf (COMPSAC), The Palmer House, Chicago, Ill. INFORMATION: Dr William Smith, Bell Laboratories, Naperville, IL 60540. Tel: 312/690-2389

NOV 6-8—COMPEC Peripherals, Systems, and Mini and Microcomputer Specialized Exhibition, Olympia Grand Hall, London, England. INFORMATION: Iliffe Promotions Ltd, Dorset House, Stamford St, London SE1 9LU, England

NOV 6-8—Federal Computer Conf, Sheraton-Park Hotel, Washington, DC. INFORMATION: Federal Computer Conf, PO Box 368, Wayland, MA 01778. Tel: 617/358-5181

NOV 6-8—MIDCON, O'Hare Convention Ctr and Hyatt Regency O'Hare, Chicago, Ill. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 999 N Sepulveda Blvd, El Segundo, CA 90245. Tel: 213/772-2965

NOV 14-16—Micro and Mini Computer Conf, Astro Village, Houston, Tex. INFORMATION: Dr Sam Lee, School of Electrical Engineering and Computer Science, U of Oklahoma, 202 W Boyd, Norman, OK 73019. Tel: 405/325-4721

DEC 10-15—MESUCORA (Measurement, Control, Regulation, Automation) Exhibition, Physics Exhibition, and Internat'l Exhibition of Electrical Equipment, Parc des Expositions, Porte de Versailles, Paris, France. INFORMATION: Sepic/Mesucora, 40 Rue du Colisée, 75381 Paris Cedex 08, France

SEMINARS

SEPT 10-11; OCT 22-23; AND NOV 28-29—Microprocessors: Hardware, Software, and Application, Worcester Polytechnic Institute, Worcester, Mass; Copley Plaza Hotel, Boston, Mass; and Worcester Polytechnic Institute. INFORMATION: Continuing Professional Education, Worcester Polytechnic Institute Worcester, MA 01609

OCT 22-26—Pascal Programming for Mini and Microcomputers, Ramada Inn, Woburn, Mass. INFORMATION: Prof Donald D. French, Institute for Advanced Professional Studies, 1 Gateway Ctr, Newton, MA 02158. Tel: 617/964-1412

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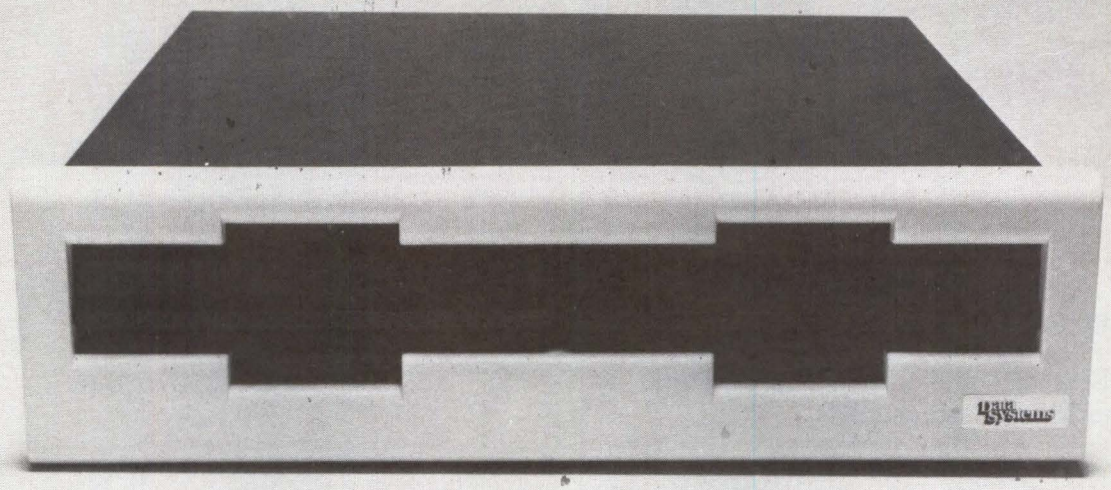

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CIRCLE 9 ON INQUIRY CARD

COMMUNICATION CHANNEL

TRENDS IN THE DIGITAL TRANSMISSION OF VOICE AND IMAGE SIGNALS— PART 2: IMAGE DIGITIZATION

Ira Richer

Bolt Beranek and Newman Incorporated
Cambridge, Massachusetts

Binary imaging, where only two levels (black and white) are used to characterize each image point, is the most widespread application of image digitization. This category includes most textual material as well as various forms of graphics. Facsimile is an important application.

As with digitized voice,[1] there is a tradeoff between sampling resolution (and hence number of bits) used to represent the input, and quality of the reconstructed output. For business facsimile a resolution of 100 to 200 points/in (39 to 78/cm) is generally used, although quality at the low end of this range is only marginally acceptable.[2] In applications where higher quality output is required and where transmission costs can be ignored, resolution of 300 points/in (118/cm) is becoming the standard. Specialized applications such as newspaper page transmission may require a resolution of 1k to 2k points/in (394 to 787/cm).

Scanners and Printers

Of the many types of scanners currently used to convert the image into digital form, laser scanners and solid state linear arrays are emerging as favorites and are likely to remain so for a number of years. A dual 1728-element charge coupled device (CCD) linear array scanner was used in the Litton Datalog Washfax secure digital facsimile, and the same company used a laser scanner in its equipment for the tri-services facsimile network.

At the receiving end, most new generation facsimile machines use multistylus (linear array) electrostatic printers. For computer use, IBM, Xerox, and Siemens have laser based electrostatic printers at 300 points/in (118/cm). The inkjet plotter, whose major advantage is its color capability, is another category. All three types will coexist in the near future, but laser based printers will probably emerge as the preferred type.

Laser scanners and solid state linear arrays are emerging as favorites

Data Compression

Reducing the quantity of digital data that must be transmitted for each image requires some form of redundancy reduction coding. One of the proposed international standards calls for transmissions of one minute or less over the public switched telephone network. With no coding, about seven minutes would be required for a resolution of 200 points/in (78/cm), a 100-in^2 (650-cm^2) page, and a data rate of 9.6k bits/s. To meet the goal set by the proposed standard, a compression factor of seven or higher is needed. Business facsimile is providing the impetus for both development and standardization of encoding techniques, and Ref 3 shows the 8-document CCITT test ensemble.

The high degree of correlation between neighboring picture elements (pixels) is the basis for achieving data compression of images. The techniques applied to business facsimile use raster coding and can be grouped into two categories: 1-dimensional, where each scan line is individually encoded, and 2-dimensional, in which the encoding is applied to pairs of lines.

One-dimensional schemes first take advantage of the lengths of successive black and white samples within a

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CENTRONICS® PRINTERS

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CIRCLE 10 ON INQUIRY CARD

scan line (run-length coding) and then encode these run-lengths using a block coding technique. This scheme is based on a Huffman code, which minimizes the average codeword length for given relative frequencies of run-lengths. With 1-dimensional coding, a channel error introduces errors in only a single scan line.

Two-dimensional encoding techniques are of two types. One is essentially an extension of 1-dimensional run-length encoding to successive distinct pairs of scan lines. The lengths of runs are encoded for the four possible combinations occurring at corresponding samples in the paired rows. The second type uses a moving window to encode pairs of lines—lines 1 and 2, then 2 and 3, then 3 and 4, etc. The encoding principle here is to transmit changes in white-black transition positions, as well as information on when new transitions appear and old ones disappear.

Business facsimile is providing the impetus for development and standardization of encoding techniques

With the first 2-dimensional encoding method, the effect of a channel error is confined to a particular pair of lines, whereas in the second, an error can propagate. To limit error propagation, single encoded lines are periodically transmitted. It should be noted, however, that although the more effective compression techniques are more sensitive to channel errors, they require fewer transmitted bits per document, so that errors in the reconstructed image, while more noticeable, are less likely to occur.

In general, the higher the input resolution and the more sparse the information on the image, the greater will be the compression obtained with 2-dimensional, relative to that of 1-dimensional techniques. Some representative compression factors at 200 points/in (78/cm) for a businesss letter that is not dense (CCITT facsimile test document 1) are 17:1 for 1-dimensional coding, 20:1 for 2-dimensional coding of distinct line pairs, and 25:1 for 2-dimensional coding using a window.[3]

Grayscale Images

In grayscale images each pixel can take on a continuous range of intensities as opposed to the simple black/white of binary images. Some examples of grayscale images are conventional photographs, x-rays, computer axial tomography (CAT) scans, etc. Acquisition of grayscale images involves some sort of scanning process, since the 2-dimensional image must be converted to a 1-dimensional signal or waveform for transmission. The most common technique for scanning is with a vidicon camera tube. In the future it is expected that CCD electronics will supplant the bulkier vidicon in most systems.

The other approach to scanning uses a device similar to that used for binary images. The principle disadvantage of such scanners is the drift in amplitude sensitivity. However, they are capable of much higher spatial resolution, repeatability, and freedom from geometric distortion.

The CRT is and will likely continue to be the most widely used method for grayscale image display, possibly joined by the flat panel plasma discharge device. The latter, due to limited response time, is particularly well suited for static grayscale displays, although it has also been demonstrated for color TV. With mass production, plasma displays could eventually be less expensive than CRTs.

For hard copy, techniques used by AP and UPI wirephoto facsimile machines are becoming increasingly popular. The AP machine uses laser writing on dry silver film. UPI uses a binary electrostatic printer; grayscale is created by electronic halftoning.

Image compression is unquestionably the major area of technical investigation and development pertaining to grayscale displays. Without compression, a photograph with a dynamic resolution of 64 levels requires the transmission of six times as much information as a binary image of equal spatial resolution and size. Two broad classes of compression techniques are spatial encoding and transform encoding.

Spatial encoding. PCM is the simplest form of spatial encoding. Typically, eight bits, corresponding to 256 gray levels, are used. A first step toward compression involves the use of differential PCM which recognizes that interpixel intensity differences rarely span the entire dynamic range. Thus, fewer bits are needed if two to four bits are used to represent the difference between gray levels of successive pixels on one or more scan lines. Such a technique may suffer inaccuracies if the assumption about interpixel differences is violated, that is, if two successive pixels have high contrast. Therefore, unless the image is oversampled, differential PCM methods are bound to be approximate, resulting in outputs that differ from the source.

If some degradation is acceptable, even higher degrees of compression are possible. One such technique is adaptive differential PCM, in which inter-pixel differences are encoded with a single bit, but the bit represents an increment which varies with the local properties of the picture. These systems tend to be somewhat more sensitive to channel errors, and they typically require a limited amount of buffer memory, usually one pixel or one scan line, and a modest amount of processing power to implement the encoding/decoding algorithms.

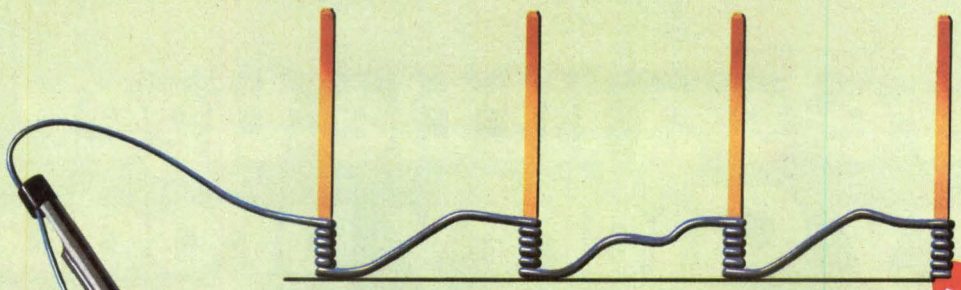
Transform encoding. Transform, or frequency domain methods, such as Fourier, cosine, and Hadamard-Walsh[4] transforms, rely on the observation that the "transform image" (the frequency domain representation obtained by a discrete Fourier transform) can often be transmitted in truncated or approximated form, yielding a degraded version of the original image at the receiver. A major

In the future it is expected that CCD electronics will supplant the vidicon for grayscale imaging

area of research is the investigation of how the compression of the transformed image maps into perceptual degradation in the receiver, such as blurring or "ringing" of edges, ghosting, dc drift, etc. Transform techniques, even those operating only on small sub-blocks of the entire picture, require large amounts of image buffer memory. More importantly, even with techniques like the fast Fourier transform, the transformations themselves are computationally expensive. Because of these disadvantages, and because differential PCM techniques generally require fewer bits to achieve a given quality image, transform methods will not find wide acceptance in the commercial market.

Color Images

In principle, a color image requires no more than three times the amount of data as the corresponding grayscale image. In fact, the human visual system is remarkably forgiving in dynamic range, intensity resolution, and spatial



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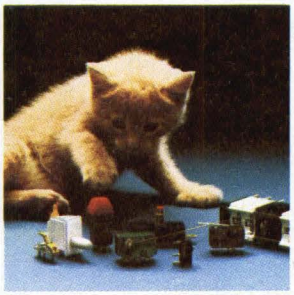

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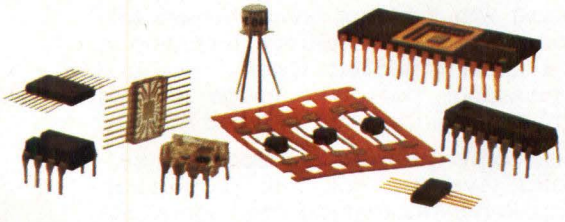

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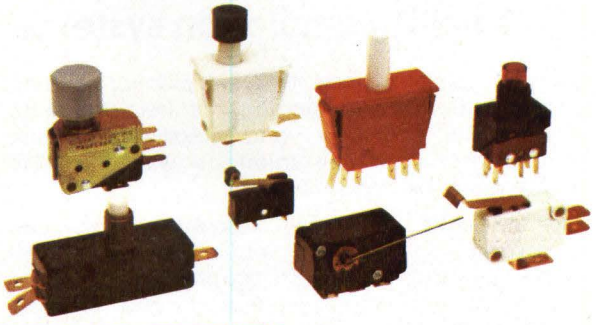

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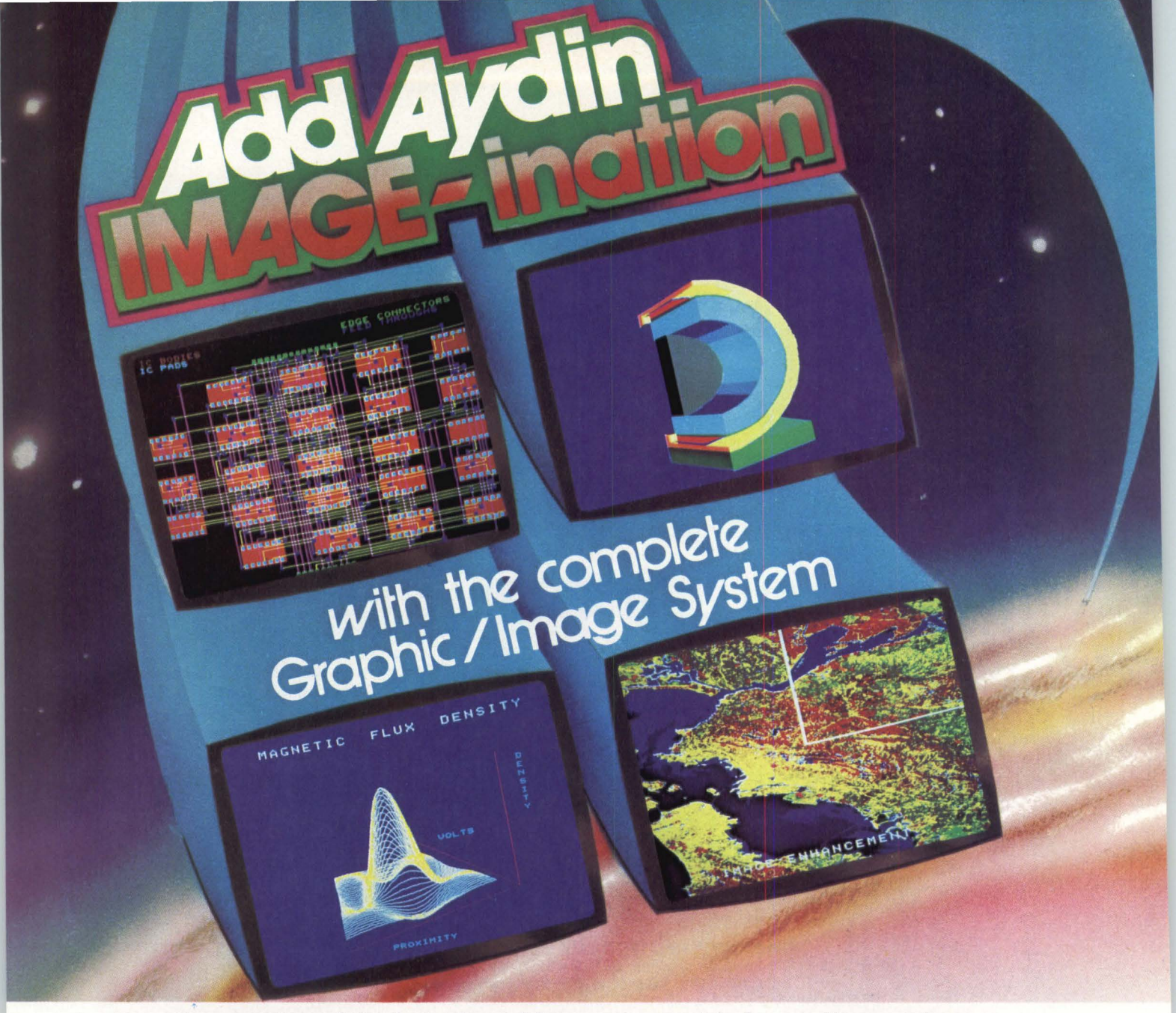

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CIRCLE 16 ON INQUIRY CARD

AY-101

resolution of the "chromaticity" component of the signal, provided that the intensities are reasonably accurate. Thus, color images can be transmitted with only a slight increase in bit rate over that required for black and white images.

Moving Image Digitization

Most coding techniques for moving images attempt to take advantage of the frame-to-frame correlation inherent in the images: in the absence of rapid movement, successive frames are quite similar, especially if the background is static. As a result, moving-image encoding techniques employ differential PCM in the time dimension, possibly also with intraframe encoding of the type discussed for static grayscale images. Interframe methods require a memory of at least one frame. Both interframe and intraframe compression techniques have been extensively studied at Bell Telephone Laboratories and more recently in Japan. The present emphasis is on teleconferencing applications.

Color images can be transmitted with only a slight increase in the bit rate required for black and white

Bandwidth of conventional broadcast TV in the U.S. is about 6 MHz, which requires about 96M bits/s after digitization at 8 bits/sample (the Nyquist rate). Excellent quality color images have been demonstrated in Japan, for U.S. TV format, with intraframe differential PCM but with no interframe coding, at 32M bits/s. Below this rate, motion degradation begins to appear. As an example of current research in this field, computer simulations of a picturephone format (200 lines) coder with a data rate of 64k bits/s have been conducted.[5] In this experiment, the moving images are sampled more coarsely because they do not require as high resolution as do static images. While motion degradation is clearly visible, it may be tolerable for some specialized applications.

Prediction of the motion of objects, rather than merely of edge transitions, is an interesting area of research. The quality of the resulting images depends on the motion, with more degradation as motion increases. Good quality TV images at 10M bits/s will be possible with interframe coders for motion compensation in the not too distant future.

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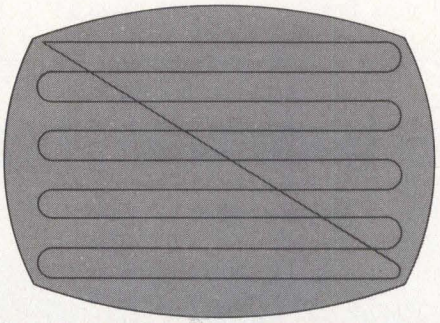

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Transparent RAM addressing allows the CRTC to address the refresh memory "transparent" to the MPU—the refresh memory can be configured to be a slave to the CRTC instead of being shared with the MPU. The SY6545 does all the work of generating memory addresses for display refresh and memory updates. The memory can be updated either during horizontal and vertical blanking periods or interleaved with screen refresh during the display period.

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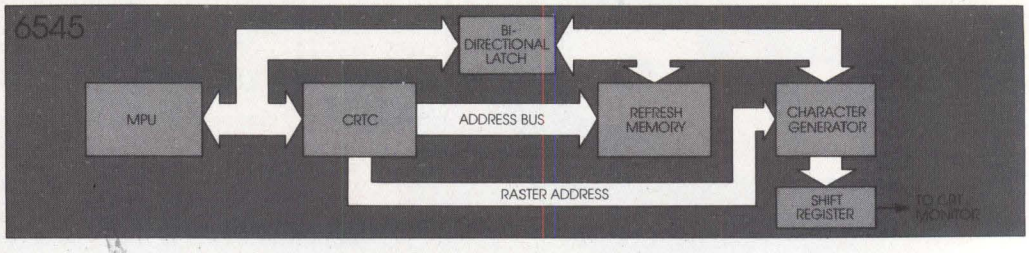
The SY6545 is plug-in replaceable with Motorola's MC6845, working in all systems designed for the MC6845—without the need for system modifications of any kind. That's compatibility. And more, too. Because the SY6545 does even more than the MC6845, operating in more modes and possessing additional features above and beyond the MC6845. That's upward compatibility.



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The 6551's on-chip programmable baud rate generator eliminates the need for external components and features 15 programmable rates up to 19.2 kilobaud. For non-standard baud rates (up to 125 kilobaud) the 6551 allows the use of an external 16X clock. This wide-ranging programmability allows accommodation of a variety of applications—from point-of-sale, financial and intelligent terminals to front end processors, remote data concentrators, computer-to-computer links and more. Whatever your communications application, the 6551's built-in versatility delivers.

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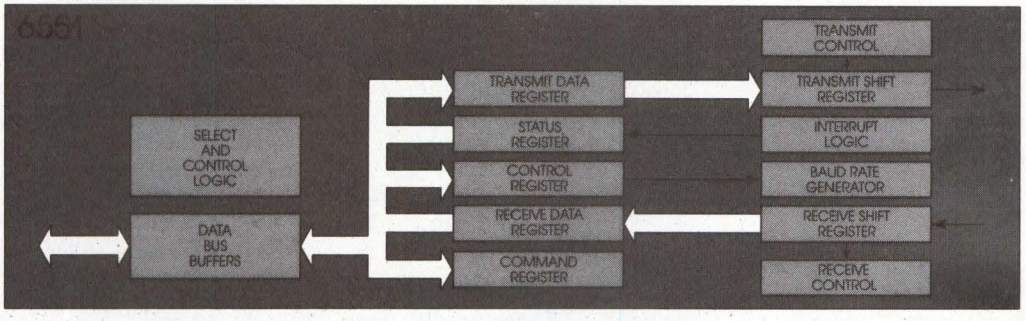

CIRCLE 18 ON INQUIRY CARD

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Gentlemen:
I have immediate needs for technical information on the following: ☐ SY6545 (CRTC) ☐ SY6551 (ACIA)

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Some Pragmatics in Applying Fiber Optic Systems—Case History of a Computer Communications Application*

At first the project appeared to be ideally suited to the application of fiber optics: a new Library of Congress building, with 50 acres (20 ha) of floor space, to be wired up to connect a computer center to more than 1000 computer terminals located at widely dispersed sites throughout the structure. A communications system was needed that would serve staff requirements for a long time; and while the bandwidth capabilities of fiber optics systems were not required at the outset, it was apparent that in a few years the system would be handling signals in the megahertz range. For these reasons there was initial enthusiasm for cabling the entire building with a fiber optics system adequate for both present and future traffic.

However, after a study of installation parameters, Sander says, there was a 180° shift away from the fiber optic approach. First came the fact that the computer terminals would constantly move. Staff structures change, floor plans are altered, and terminal sites move around—a situation not uncommon in many computer operations. A communication system was needed that could easily follow that movement.

"With careful planning and engineering I'm now merely eight months behind"

In addition, the cable had to be run in ceiling-mounted cable trays, without any protective conduit, and be installed by normal cable crews, more or less hired "off the street." Furthermore, personnel would be moving into the building at a rate of 50 to 100/day, and the system had to work reliably from the first day.

"Worse than that, the schedule was pushed up by six months, so that from day one, I was six months behind. With careful planning and engineering, I'm now merely eight months behind."

It is clear that fiber optics have been used very successfully in communications links. However, most such links have been used to connect point A to point B, where there are fixed end points, a fixed route, and protective conduits. The Library of Congress case was very different. Granted the application may have been unique, but perhaps some benefit may be derived from the following considerations.

System Constraints

First, it was necessary to connect the computer center to 1000 locations. With installation costs in mind, multiple fiber cables, with extra fibers as spares, would be run. The cables would rise to the various floors of the building, and at each floor fan out to the terminal sites. This required cross-connection, similar to that of a telephone installation. Here is where serious problems became apparent. There were variable end points, unprotected routes, and the necessity to cross-connect. All this led to a consideration of alternatives, resulting in essentially three choices for the communications medium: fiber optics, coaxial cable, or twisted pair.

Transmission Line Differences

These media types differ in several important areas: performance, maturity of the technology, risk in availability and reliability of the product, and the ability to react to and accommodate change.

A summary of Sander's conclusions is found in "Media Characteristics." In this listing data rates are compared to those over voice grade lines. In product technical maturity, many critical fiber optic components are in the laboratory stage and not yet into production; coaxial is still relatively new, while twisted pair is a well-proven medium. In product availability, fiber optics rates very low, coaxial low, and with twisted pair, many suppliers are available to supply the product. Where costs are concerned, Sander says, "It would cost me at present 40 times as much to install a fiber optic system compared to one of twisted pair. I told my management that if we could wait four or five years for these products to come out of the laboratory and be put into production, there would be a dramatic reduction in cost."

Fiber Optic Advantages

The initial interest in a fiber optic system was due to the many benefits to be derived from its inherent qualities.

Noise immunity. In any transmission system the effects of emi, rfi, and perhaps even of a nuclear magnetic pulse are serious worries.

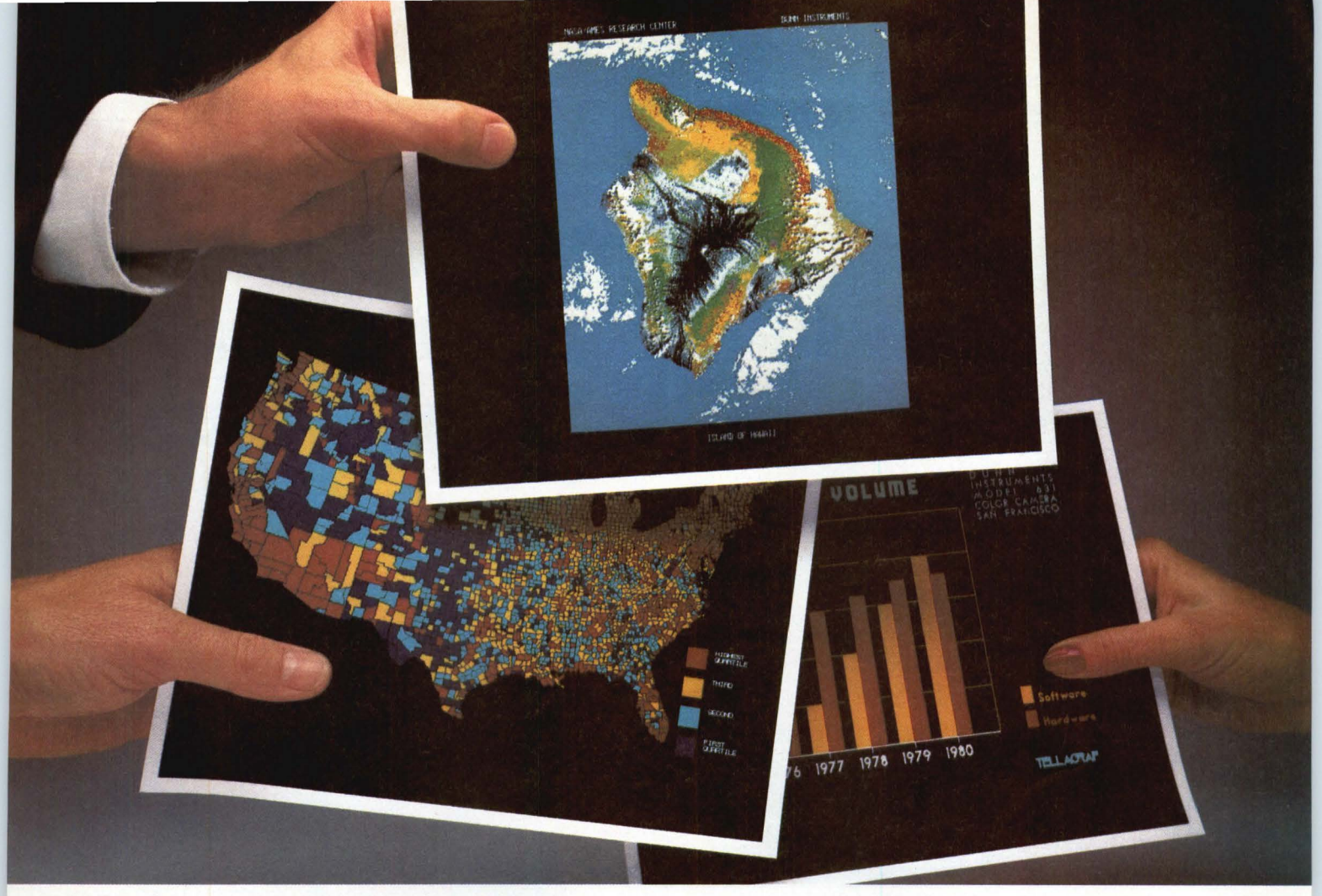
Electrical isolation. Ground loops can really hurt!

High data security. While the system specifications do not include a security requirement, who knows what may come up in the future? Security means that no one can tap into the data stream—but this is a 2-edged quality. It means also that the system can't be tapped for diagnostics or troubleshooting, either.

"Security . . . means also that the line can't be tapped for diagnostics"

Other well known benefits of a fiber optic system were also considered: no crosstalk; no circuit loading by short circuits; no ringing or echoes; high bandwidth capability; last but not least, small size and

*This item is based on a presentation by R. C. Sander, Sr Program Manager, Library of Congress, at Interface '79, Apr 11, 1979



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DUNN INSTRUMENTS

CIRCLE 19 ON INQUIRY CARD

From the graphics leader.

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Carol Mersch
Information Systems
Manager
Agrico Chemical Co.

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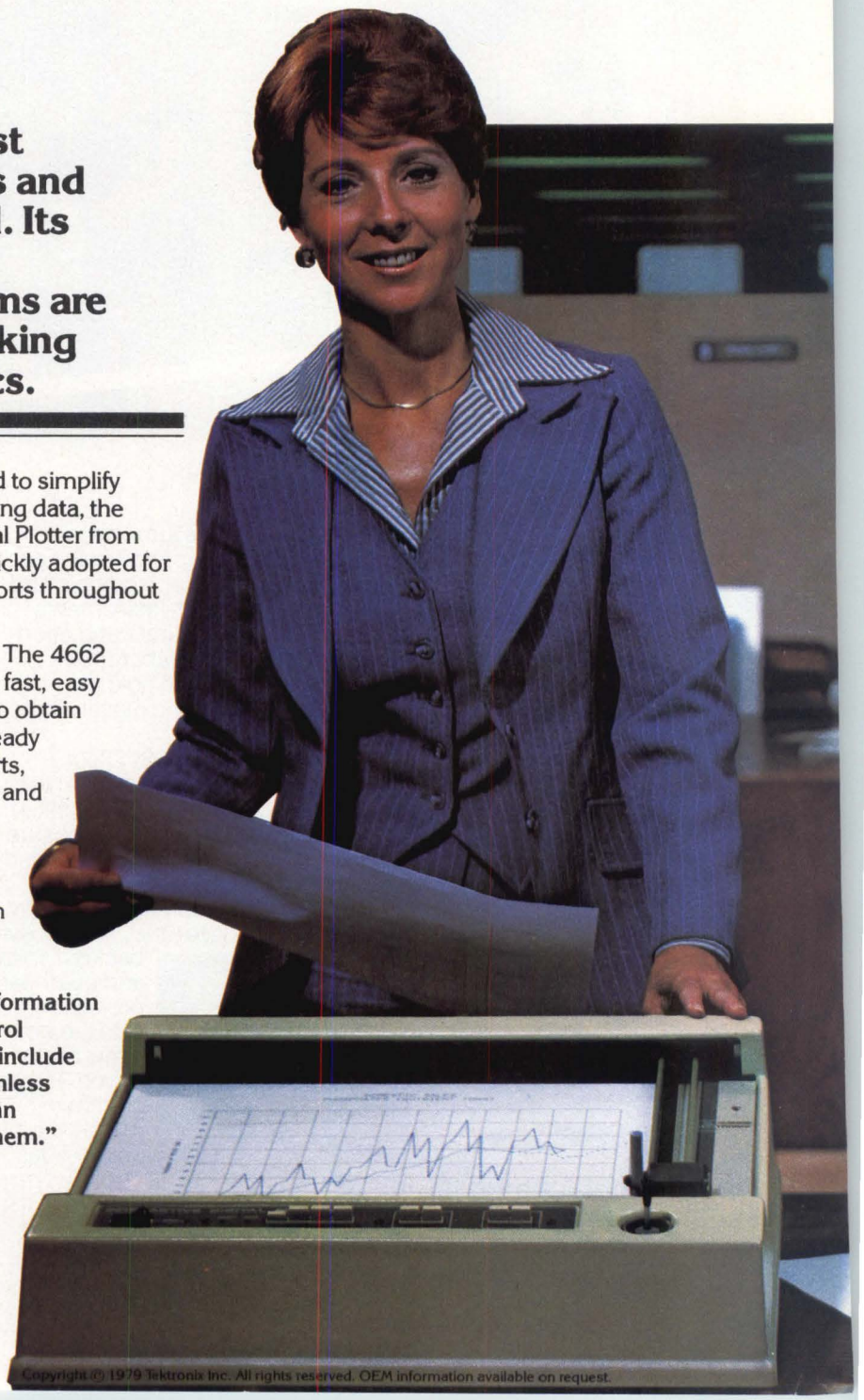
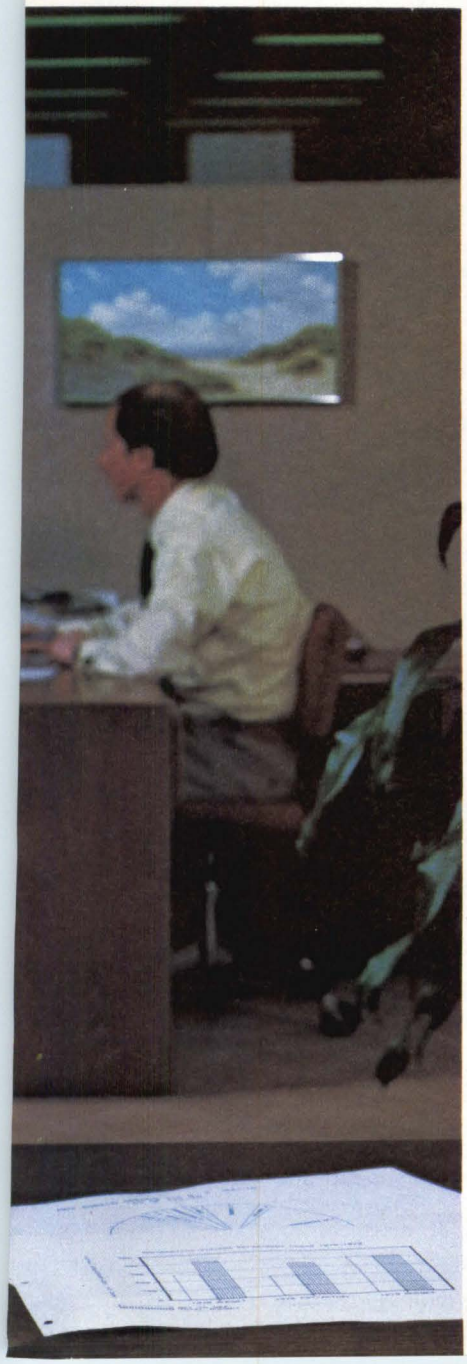
It's not surprising. The 4662 provides a remarkably fast, easy and economical way to obtain precise and camera-ready multi-colored bar charts, pie charts, line graphs and more, on either paper or overhead projector film.

Result: people can understand more by reading less.

"Before," says Information Systems Manager Carol Mersch, "we couldn't include graphic summaries unless we had five days and an artist on hand to do them."

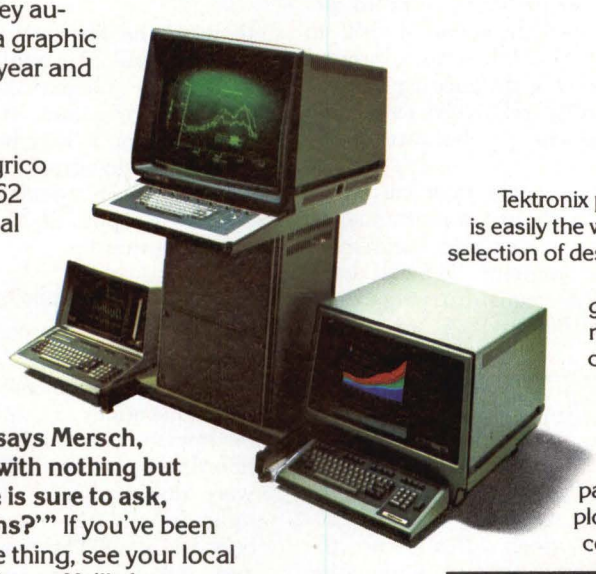


operations reports now summaries. That's a convenience afford before."



Now, when Marketing requests a sales analysis or Planning asks for an analysis of harvest trends, they automatically receive a graphic overview of year-to-year and even week-to-week comparisons.

In the future, Agrico will be using the 4662 for three-dimensional contour plots of county-by-county sales densities, and to interactively illustrate "what if" type situations.



"These days," says Mersch, "if a report slips by with nothing but numbers, someone is sure to ask, 'where are the graphs?'" If you've been wondering the same thing, see your local Tektronix Sales Engineer. He'll show you the easiest, most reliable answers of them all, including B and C size plotters, copiers and our other computer graphics products. Or call our automatic answering service now, at 1-800-547-1512. In Oregon, call 644-9051 collect.

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low weight. All these attributes are very attractive to the system designer.

Cable Categories

Plastic and glass are the two principal types of fiber optic cables. These cable approaches differ in cost, signal attenuation, bandwidth capability, ease of connectorization and splicing, and in the care required in physically handling the cable.

Plastic is a comparatively thick cable and therefore less difficult to handle than glass. It is also lower in cost, but attenuation runs typically 200 dB/km. Plastic is being used to locally connect computers to peripherals where distances of 100 to 200 m are involved. It is not at present practical for long distance runs. Connectorization is relatively easy, and is faster and cheaper because of the larger size.

Glass cables come in a variety of types, each with its own attenuation characteristic, cost, and degree of difficulty in handling. Typical diameters of the signal-carrying cores range from 60 to 125 μm. Bandwidths are much greater—in the multi-megahertz range. Attenuation is very low. There have been reports of fiber with a loss of 1 dB/km, which is excellent. Glass is currently very expensive, but costs are coming down rapidly.

"When dealing with fiber optics, Murphy was an optimist"

A few rules of thumb should be considered. Maximum bandwidth in almost any circuit right now, including driver, cable, and receiver, is about 400 MHz. Connector loss seems to vary between 1 and 1.5 dB. Up to about 200 m there are few data rate limitations. Between 200 and 500 m, bandwidth decreases linearly with length; above 500 m, bandwidth seems to vary as the square root of the length.

It has also been recommended that every cable installation include extra fibers, be connectorized, and have extension cables on both ends. People have an uncontrollable urge to wind the fiber optic cable around a pencil and play with it when they are on the phone. While the fibers are stronger than steel, they are thinner than a human hair and are very easy to break. Things do go wrong. When dealing with fiber optics, Murphy of the famous law was an optimist.

Media Characteristics

	Fiber optics	Coaxial cable	Twisted pair
Data rates/voice grade	10^4:1	300:1	10-50:1
Technology maturity	lab	new	proven
Availability	very low	low	high
Cost now	40:1	5:1	1:1
Cost 1984	4:2	4:2	2:1

Connecting and Splicing Problems

"One of the things that bothered me about fiber optics," Sander says, "was that before I got into computer communications I was involved in microwave communications. Frustration drove me out of that field. There were tiny connectors that had to be tightened by tiny wrenches to precise torques. The connecting parts and surfaces were so critical that you could never get back to the same place, and this really concerned me about using fiber optics. I'd be working with something even more sensitive."

Connectorizing glass fibers is a delicate operation. Fiber ends must be polished so that they are perfectly parallel, placed into connector ferrules that maintain nearly perfect axial alignment, and butted and joined. The connectors themselves are precision devices, are fragile, and are intolerant of more than a few connects and disconnects. They are also expensive, though prices are falling as suppliers move into production.

Splicing fiber cable is another area where polished ends and axial alignment are required. The ends are butted, but there is always a small gap between them. This gap is flooded with an epoxy whose refractive index must match that of the fibers. The process takes from 20 to 30 minutes, is not a 1-man operation, and is low yield—about 70 to 80% probability that there is a good connection.

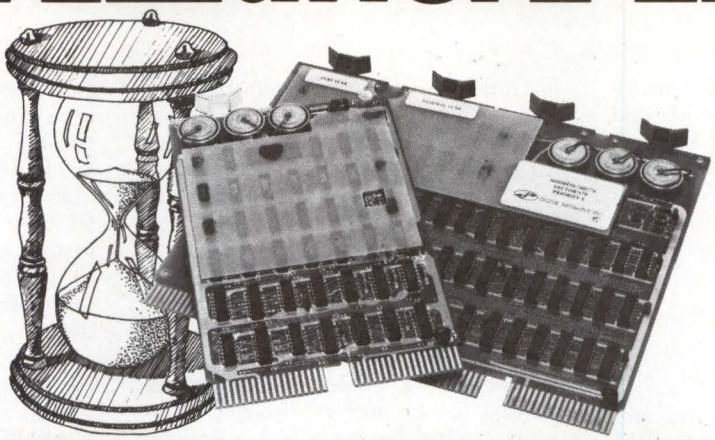
On the other hand, says Sander, "When connecting twisted pair, you join the wires, make a check with a cheap ohmmeter, and have considerable assurance that the splice will work. You can't do that with fiber optics. You can't touch an instrument to it. You need a source at one end, someone at the splice location with a microscope and earphones, and someone at the receiver end to determine how much power is being transmitted."

Modems

What is needed for this application is a device with an RS-232 interface that can be plugged into a conventional data circuit. There are, according to Sander, about four vendors in production of fiber optic asynchronous modems, at prices in the area of $1800/pair. "I was concerned that they have limited diagnostics, not the sort that we're used to when working with conventional modems; and these asynchronous units have limitations imposed by the bandwidths and the distances involved."

Two suppliers now provide synchronous fiber optic modems. The units from one vendor are specified for synchronous operation up to 56k bits/s at distances to 3000 ft (915

TIME after TIME



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TCU-410 • $325

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- SBC/BLC compatible.

HP 2100

TCU-2100 • $395

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CIRCLE 21 ON INQUIRY CARD

m), and are priced in small quantities at $650 per end. The second modem has the same speed capability, but using a different light source and receiver, can cover up to 16k ft (4877 m). Because of the greater distance capability, these units are priced at $2000/end.

Instruments and Troubleshooting Aids

There are relatively few instruments available for the fiber optics field. There are power meters. There are reflectometers that diagnose the nature and distance from the source of discontinuities and imperfections along the cable. These are a number of companies that furnish attenuation and transmission measuring sets, as well as splicing and connectorization aids.

"I must be able to troubleshoot problems that will inevitably occur"

"As a system designer," Sander says, "I want a data link that is connectorized so that it can be easily relocated. I want compatible interfaces, like RS-232. I must be able to diagnose my link and troubleshoot problems that will inevitably occur on the link or at the terminals. I need the capability to monitor transmissions, instrument the link, and patch around problems. None of these areas is now being economically addressed."

What is Needed

The fiber optics community needs development emphasis on cables with lower attenuation and less dispersion, that are physically stronger and less expensive. Because of concerted efforts by suppliers, Sander says, the cable area is in the best shape with respect to his application.

There is also considerable development in light sources, aiming at higher output power with lower noise, greater reliability, and packaging designed for user convenience. Receiver sensitivity is being increased in order to allow longer distance transmission without the need for repeaters. Noise and stability characteristics are being improved. Transmitter and receiver technologies are coming along well because of the efforts of manufacturers.

There is a need for more RS-232 compatible synchronous modems, a broader range of instrumentation, tee couplers, and an easier way of connectorizing cable. Standards are needed for connectors. Splicing techniques must be simplified. "Basically, lower costs are needed throughout the component area."

Starting Out

The system designer beginning to look at fiber optic applications, Sander says, should start experimenting. It's a new technology that is coming along rapidly and the experience will be valuable. However, it should be considered as an experiment unless there is an A to B transmission path with fixed end points, fixed routing, and a protected path. An excellent way to start is with the complete data link packages available from several manufacturers for routes shorter than 300 m. This will be a useful introduction to the concept, without the worry about the nitty-gritties of optical circuity and interfaces. Certainly, fiber optics should be considered where there are unusual and severe environmental factors such a lightning, rfi, emi, and emp.

"In my Library of Congress application," says Sander, "I concluded that a twisted pair system was the most convenient and economical. I am very much encouraged, in fact enthusiastic, about fiber optics; but the variable end points present a really tough problem to tackle at this time. Where I have fixed end points, I will definitely install fiber optic links."

Word Processing System Functions Expanded by Controller Option

Single-package multipurpose controllers to support both asynchronous and bisynchronous communications as a single facility on its word processing systems have been made available by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851. The controllers, resident in system workstations, allow the stations to perform as interactive or batch terminals as well as word processing devices, and to communicate with comparably equipped Wang, or other compatible word processing and computing systems when equipped with a suitable modem.

The options for standalone system 5, and for workstations of systems 20, 25, and 30, permit the systems to operate as asynchronous interactive Teletype® or 2741 timesharing terminals, at speeds to 1200 bits/s, for a variety of computer access applications.

Using the same option in the bisynchronous mode, the systems can be used for batch processing. The communicating bisynchronous systems with speeds up to 2400 bits/s are compatible with 2780/3780 protocols and are well suited to source document capture, remote job entry, and electronic mail applications. In this mode the controllers also allow alternative use of a CRT in a full line monitor mode to display in real-time data link control characters for increased diagnostic capability.

Circle 400 on Inquiry Card

Carrier Offers Message Storage/Editing Unit

An offering of a diskette storage unit for increasing transmission speed and improving the economy of data communications systems has been made by AT&T, 195 Broadway, New York, NY 10007. The Comm-Stor* II communications storage unit is a single (256k-char) or double (512k-char) drive system for storing messages received online or for pre-

*Comm-Stor is a registered trademark of Sykes Datatronics, Inc.

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"Tough" doesn't do the design justice

Start with the base. It's a heavy-duty, thicker-gage metal base chosen for the extra stability it gives the entire printer. So no matter how often you move or handle our printers, printhead alignment and print quality will not be affected.

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A printhead that won't quit on you

Everything about our matrix printheads says they won't have the problems most printheads do.

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Another reason: a unique bronze-filled plastic insert that enables the printhead to maintain high print quality longer.

And, unlike ordinary printers, ours has a straight-wire printhead design. There are no curved wires or jeweled guides to create friction, impair character resolution or wear out quickly.

Servo motors cause fewer problems

That's why, instead of conventional steppers, we opted for individual D/C servo motors to drive the printhead and paper handling systems. As a result, operation is much smoother and more reliable. Plus, the motors last longer. In fact, test motors have undergone over 20 million reversals without a single failure.

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Look at the printhead carriage. To prevent friction and lubrication problems, it's mounted on graphite bearings. Not ball bearings. Result: the carriage moves more smoothly and the life of the printing system is extended.

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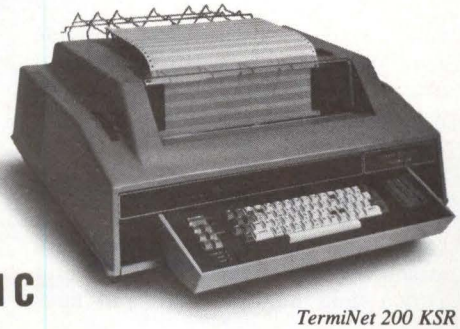
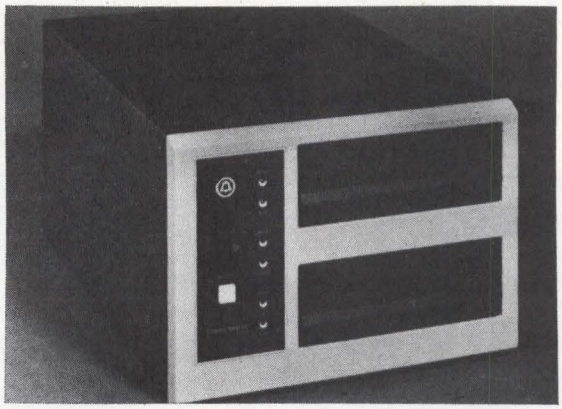
TermiNet 200 MSR (ASR also available)



TermiNet 200 KSR

GENERAL ELECTRIC

CIRCLE 22 ON INQUIRY CARD



Communications storage unit. Shown is dual-drive system with 512k-char capacity. System allows conversion of ASCII data on diskette to or from EBCDIC in 3740 data exchange format

paring messages offline for transmission. Both single and dual configurations have three ports for interfacing an asynchronous terminal, a printer, and a data set via EIA RS-232 connections. 1k to 4k buffering is provided for terminal and printer ports.

The unit automatically generates and maintains a directory that lists all messages stored on the diskette. Capacity is 1738 fixed or variable length messages. All messages can be retrieved or transmitted in alphabetic or historic sequence by message name, group, or range. Operation is in full or half duplex mode. Each port operates at speeds from 50 to 9600 bits/s asynchronously, with batch receiving speeds to 4800 bits/s. The unit will also operate up to 4800 bits/s isochronously at the data set port.

Tariffs governing the storage unit are presently filed in several jurisdictions, and tariffs covering the unit and optional features, such as forms prompting, editing, and file management, are expected to be filed in all jurisdictions by the fall of 1979. Further information on the unit is available from Bell System account executives or from local Bell System business offices.

Networking System Operates Independently of Mainframe Software

Self contained PIXNET can provide communications between IBM mainframes and a variety of peripherals without using conventional teleprocessing (TP) access methods. Major components include a local control unit (LCU) which attaches to the mainframe, and remote control units (RCUs) to which peripherals are attached. A network control unit (NCU) links multiple LCUs and RCUs in a number of intelligent network configurations.

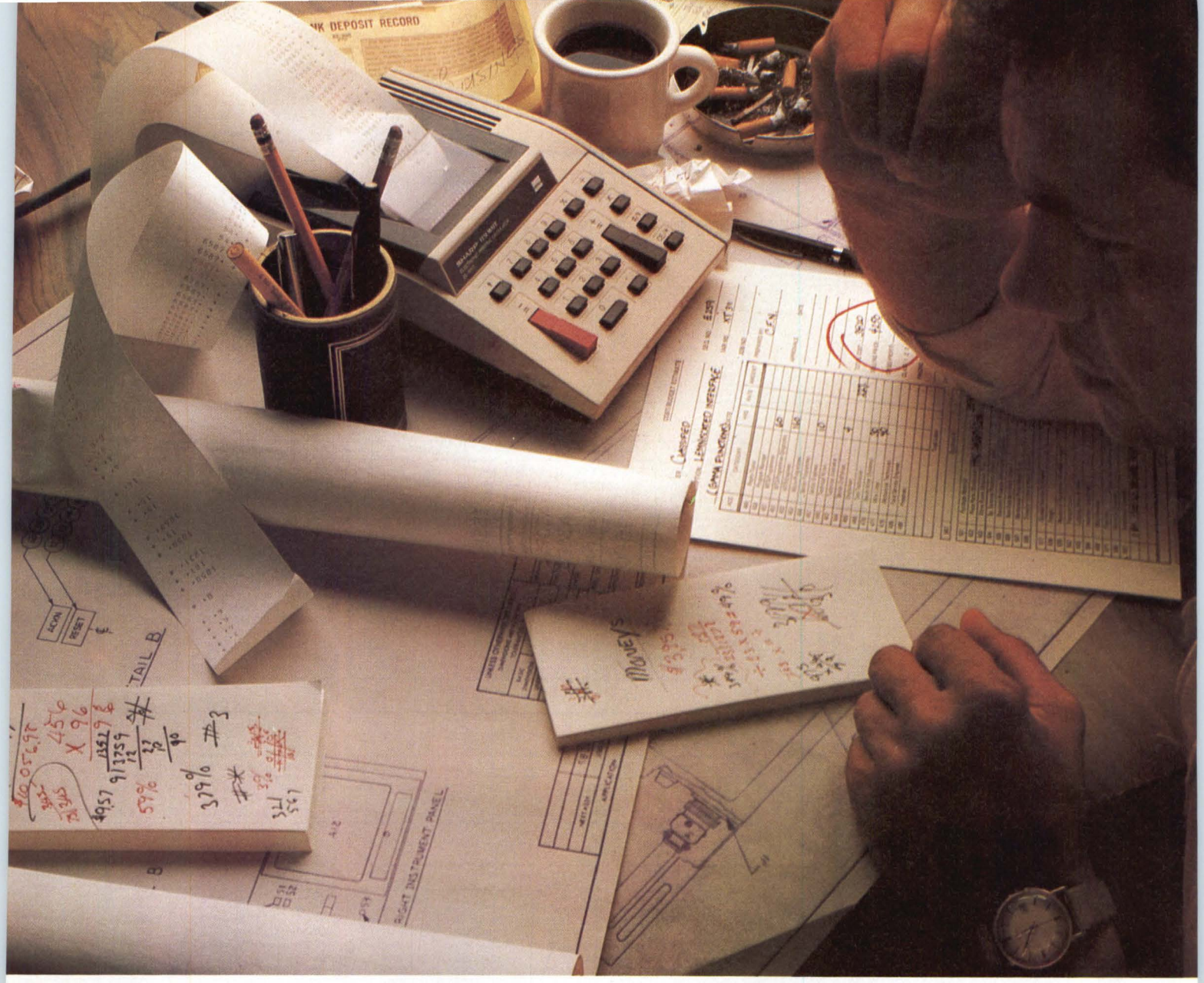
The system is available from Paradyne Corp, 8550 Ulmerton Rd, Largo, FL 33541. It incorporates standard features of the company's PIX II virtual data links, such as full duplex SDLC, elimination of communications overhead including polling, data compression, multiple device type support on a single communications line, and fast terminal response over satellite links as well as over land lines.

Among the benefits cited is the ability to easily connect a single interactive terminal to multiple application programs throughout the network, including different programs stored on the same mainframe. Data can also be transmitted via low to medium speed lines from several sites to a NCU, and relayed to a mainframe over a single high speed line, providing line concentration as well as full duplex communication and data compression. The system allows address of any mainframe from any terminal without interaction and disruption in the IBM mainframe. Automatic routing needed to balance data flow through the network is also provided.

PIXNET deliveries are scheduled to begin in the fourth quarter of 1979.

Circle 401 on Inquiry Card

Continued on page 39



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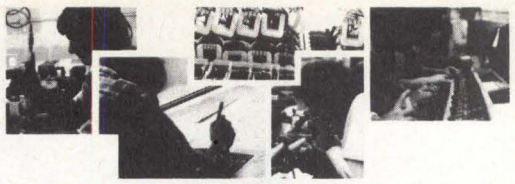
CIRCLE 23 ON INQUIRY CARD

Microcomputer Power, Inc.



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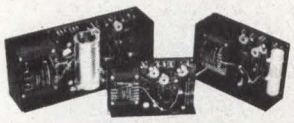

Output No. 1	Ouput No. 2	Output No. 3	Model	Size (inches)	Price (1-9)
+5V @ 2.0A	+(9-15)V @ .4A	−(9-15)V @ .3A*	TAA512	6.50x4.00x1.62	$ 49.95
+5V @ 4.0A	+(9-15)V @ 1.0A	−(9-15)V @ .3A*	TBB512	7.00x4.87x2.50	71.95
+5V @ 9.0A	+(9-15)V @ (1.5-1.7)A	−(9-15)V @ (1.5-1.7)A*	TCC512	11.0x4.87x2.75	110.00

* −(9-15)V jumper selectable to −5V

Microcomputer Series

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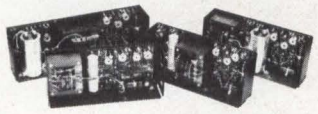
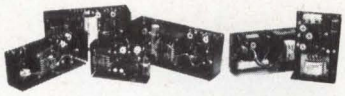


Output No. 1	Output No. 2	Output No. 3	Output No. 4	Model	Size (inches)	Price (1-9)
+5V @ 6.0A	+12V @ 1.0A	−12V @ .5A	−5V @ .5A	CP120	11.0x4.87x2.50	$ 99.95
+5V @ 6.0A	+12V @ 2.0A	−12V @ .5A	−5V @ .5A	QCBB512	11.0x4.87x2.75	104.95
+5V @ 9.0A	+12V @ 2.0A	−12V @ .5A	−5V @ .5A	QTCC512	11.0x4.87x2.75	119.95
+5V @ 12.0A	+12V @ 2.0A	−12V @ .5A	−5V @ .5A	QDBB512	15.0x4.87x3.75	129.95

Floppy-Disk Series

Shugart • Wangco • Persci



Output No. 1	Output No. 2	Output No. 3	Output No. 4	Model	Size (inches)	Price (1-9)
+12V @ 1.2/1.7A Pk	+5V @ .7A	None	None	FAA512	6.50x4.00x1.62	$ 39.95
+24V @ 1.5/1.7A Pk	+5V @ 1.0A	−5V @ .5A	None	FBAA524	10.2x4.00x2.50	69.95
+24V @ 1.5/1.7A Pk	+5V @ 2.5A	−5V @ .5A	None	CP142	7.00x4.87x2.50	74.95
+24V @ 1.2/3.0A Pk	+5V @ 2.5A	−5V @ .25A	+8V @ 2A/10A Pk	CP128	8.56x4.44x2.95	79.95
+24V @ 3.0/3.4A Pk	+5V @ 2.5A	−5V @ .5A	None	FCBB524	11.0x4.87x2.75	91.95
+24V @ 5.0/6.0A Pk	+5V @ 3.0A	−5V @ .6A	None	FTCC524	11.0x4.87x2.75	120.00

Fixed-Disk Series

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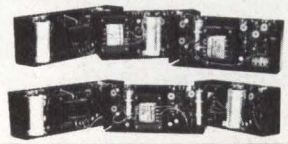
Output No. 1	Output No. 2	Output No. 3	Output No. 4	Output No. 5	Model	Size (inches)	Price (1-9)
+5V @ 6A	+24V @ 2.5/4A Pk	+12V @ 1.2A	−12V @ .5A	None	CP139	11.0x4.87x2.75	$114.95
+5V @ 8A	+24V @ 2.5/4A Pk	+12V @ 1.2A	−12V @ .5A	−5V @ 3.0A	CP140	14.2x4.87x2.75	149.95
+5V @ 10A	+24V @ 3.5/6A Pk	+12V @ 2.0A	−12V @ 1A	−5V @ 3.0A	CP141	15.0x4.87x3.75	169.95

Micro/Disk Series

Floppy-disk based microcomputers

New!

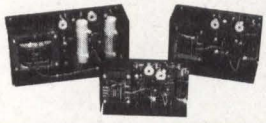


Output No. 1	Output No. 2	Output No. 3	Output No. 4	Model	Size (inches)	Price (1-9)
+5V @ 6A	+24V @ 1.3/1.7A Pk	+12V @ 1.0A	−12V @ .5A*	CP125	11.0x4.87x2.75	$104.95
+5V @ 9A	+24V @ 1.3/1.7A Pk	+12V @ 1.0A	−12V @ .5A*	CP132	11.0x4.87x2.75	124.95
+5V @ 12A	+24V @ 1.3/1.7A Pk	+12V @ 1.0A	−12V @ .5A*	CP133	14.2x4.87x2.75	144.95
+5V @ 6A	+12V @ 3.4/4.0A Pk	−12V @ .5A*	None	CP134	11.0x4.87x2.75	99.95
+5V @ 9A	+12V @ 3.4/4.0A Pk	−12V @ .5A*	None	CP135	11.0x4.87x2.75	119.95
+5V @ 12A	+12V @ 3.4/4.0A Pk	−12V @ .5A*	None	CP136	14.2x4.87x2.75	139.95

* −12V jumper selectable to −5V

Dual Output Series

Linear & Digital systems

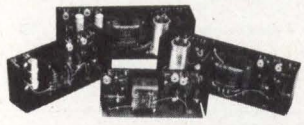


Output No. 1	Output No. 2	Model	Size (inches)	Price (1-9)
+(12-15)V @ (1.0-0.8)A	−(12-15)V @ (1.0-0.8)A*	AA15	6.50x4.00x1.62	$39.95
+(12-15)V @ (1.7-1.5)A	−(12-15)V @ (1.7-1.5)A*	BB15	7.00x4.87x2.50	49.95
+(12-15)V @ (3.4-3.0)A	−(12-15)V @ (3.4-3.0)A*	CC15	9.38x4.87x2.75	79.95
5V @ 2.0A	(9-15)V @ 0.5A*	AA512	6.50x4.00x1.62	44.95
5V @ 3.0A	(9-15)V @ 1.25A*	BB512	7.00x4.87x2.50	54.95
5V @ 6.0A	(9-15)V @ 2.50A*	CC512	9.38x4.87x2.75	86.95

*−(12-15)V and (9-15)V jumper selectable to −5V

Triple Output Series

Process controllers • Instrumentation



Output No. 1	Output No. 2	Output No. 3	Model	Size (inches)	Price (1-9)
5V @ 3A	+(9-15)V @ (1.0-0.8)A	−(9-15)V @ (1.0-0.8)A*	BAA512	10.2x4.00x2.50	$ 69.95
5V @ 6A	+(9-15)V @ (1.7-1.5)A	−(9-15)V @ (1.7-1.5)A*	CBB512	11.0x4.87x2.75	91.95
5V @ 9A	+(9-15)V @ (1.7-1.5)A	−(9-15)V @ (1.7-1.5)A*	DBB512	14.2x4.87x2.75	126.95
5V @ 12A	+(9-15)V @ (3.4-3.0)A	−(9-15)V @ (3.4-3.0)A	DCC512	15.0x4.87x3.75	149.95

* −(9-15)V jumper selectable to −5V

Specifications

115/230 vac input • .05% line & Load regulation • Fold back current limiting • 3mv pk to pk ripple • Remote sensing • OVP Built-in on +5V outputs • 0°C to 50°C full rated • 30μ seconds transient response • 2 year warranty

Representatives

CAL: Santa Clara, Microcomputer Power, Inc., (408) 988-0265; Encino, King Engineering, (213) 981-8677/ **COL:** Denver, Western Marketing Associates, (303) 841-2788/ **CONN:** New Haven, Forestberg Sales, (203) 239-5111/ **IND:** Indianapolis, Holsapple Associates, (317) 353-9441/ **MD:** Baltimore, Stemler Associates, (310) 944-8262/ **MASS:** Brocton, Forestberg Sales, (617) 522-6300/ **WASH:** Seattle, Underwood Associates, (206) 575-0123/ **UTAH:** Logan, Western Marketing Associates, (801) 735-0073/ **EXPORT:** Prima International, Santa Clara, California, (408) 727-2849

Microcomputer Power, Inc. 2272 Calle de Luna, Santa Clara, CA 95050; (408) 988-0265, TWX 910 338-7694

CIRCLE 44 ON INQUIRY CARD

CIRCLE 24 ON INQUIRY CARD →

If you buy switchers off-the-shelf keep this guide on yours.

MG Series

50-500 Watts, AC-DC, single output

This well established range of convection cooled units has UL478 approval and represents the best specifications available in an industrial unit – top of the Gould line.

INPUT

Voltage: 92-132 or 176-264
Frequency: 45-440 Hz
Hold up: 28 mS @ 100% load from 115 or 220 – 10%

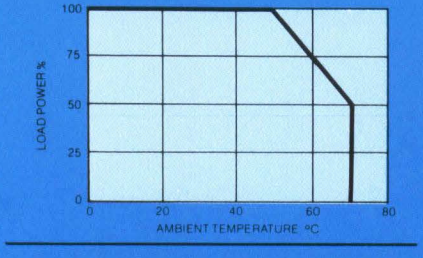
OUTPUT

Regulation: 0.1% full line & load
Ripple: 50mV pkpk DC-30MHz
Temperature Coefficient: 0.01%/°C
Remote Sensing: up to 5 volts
Transient Response: 500mV for 90% load change. regulation in 2mS
Overload: Constant current. 110%
Overvoltage: Standard

PART #	VOLTS	AMPS	SIZE	WEIGHT
MG5-20	5	20	3½ x 4⅛ x 6 7/16	4.4
MG5-40	5	40	3½ x 6 5/16 x 6⅞	7.5
MG5-60	5	60	3½ x 8½ x 6⅞	9.9
MG5-100	5	100	5 x 8 x 11	16
MG12-10	12	10	3½ x 4⅛ x 6 7/16	4.4
MG12-43	12	43	5 x 8 x11	16
MG15-8	15	8	3½ x 4⅛ x 6 7/16	4.4
MG15-16	15	16	3½ x 6 5/16 x 6⅞	7.5
MG15-33	15	33	5 x 8 x 11	16
MG24-5	24	5	3½ x 4⅛ x 6 7/16	4.4
MG24-10	24	10	3½ x 6 5/16 x 6⅞	7.5
MG24-15	24	15	3½ x 8½ x 6⅞	9.9
MG24-21	24	21	5 x 8 x 11	16
			INCHES	POUNDS

Note: *Order suffix "A" for 110V and "B" for 240V except MG5-100. MG5-60. MG24-15. MG12-43. MG15-33. MG24-21. which are user changeable.*

TEMPERATURE RANGE



SMG Series

8-250 Watts, AC-DC, single output

A broad family of convection cooled, enclosed, powe supplies at lower prices than the MG range; built to narrower specification but the same high Gould quali

INPUT

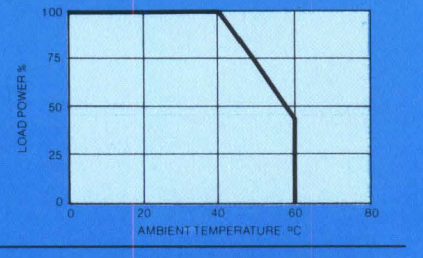
Voltage: 103-127 Vac
Frequency: 47-500 Hz
Hold up: 24mS and up at 100% load from 103v line

OUTPUT

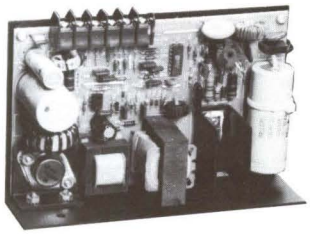
Regulation: 1.5% full line & load
Ripple: 1% pkpk DC-20MHz
Temperature Coefficient: 0.01%
Remote Sensing: 20% 5-16 to 5- 12-8 and 24-4
Transient Response: 10mV for 1 load change. regulation in 2mS
Overload: Constant current @ 1
Overvoltage: Standard except 5-

PART #	VOLTS	AMPS	SIZE	WEI
SMG5-1.6	5	1.6	3.9 x 3.9 x 1.2	
SMG5-3.2	5	3.2	3.9 x 7.8 x 1.2	1.
SMG5-8	5	8	3.9 x 7.8 x 1.7	1.
SMG5-16	5	16	3.9 x 7.8 x 3	3.
SMG5-24	5	24	3.9 x 7.8 x 5.9	7.
SMG5-40	5	40	3.9 x 7.8 x 8.9	11.
SMG5-50	5	50	3.9 x 7.8 x 8.9	11.
SMG12-1.6	12	1.6	3.9 x 7.8 x 1.2	1.
SMG12-3.2	12	3.2	3.9 x 7.8 x 1.7	1.
SMG12-8	12	8	3.9 x 7.8 x 3	3.
SMG24-0.8	24	0.8	3.9 x 7.8 x 1.2	1.
SMG24-1.6	24	1.6	3.9 x 7.8 x 1.7	1.
SMG24-4.0	24	4.0	3.9 x 7.8 x 3	3.
			INCHES	POUN

TEMPERATURE RANGE



LMG Series



75, 100 & 150 Watts, AC-DC; 1, 3, 4 outputs

The LMG range is specifically designed for the replacement of low cost linear supplies in applications where weight and efficiency have become more important. Physical dimensions similar to popular linear sizes.

INPUT

Voltage: 75 Watt units: 92-138
100 and 150 Watt units:
92-138 and 184-264

Frequency: 47-440 Hz

Hold up: 20mS at 75w @ 115v line

OUTPUT

Regulation: 0.6% full line & load

Ripple: 50mV pkpk 47Hz-10MHz

Temperature Coefficient: 0.02%/°C

Remote Sensing: 500mV

Transient Response: 5% maximum for 50% load change, regulation in 500 μSec .

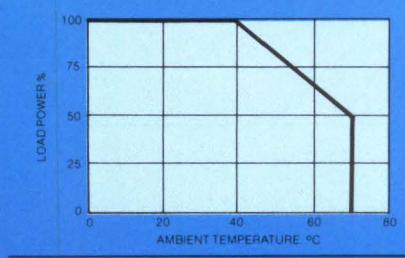
Overload: Foldback to 40%

Overvoltage: Main output. (optional)

PART #	MAIN OUTPUT	AUX 1	AUX 2	AUX 3	SIZE	WEIGHT
LMG5-15	5-15				7 x 4.9 x 2.1	1.5
LMG15-5	15-5				7 x 4.9 x 2.1	1.5
LMGT75/12	5-15	12-1	12-1		9 x 4.9 x 2.1	2.0
LMGT75/15	5-15	15-1	15-1		9 x 4.9 x 2.1	2.0
LMGQ75/12	5-15	12-1	12-1	5-1	10 x 4.9 x 2.1	2.0
LMGQ75/15	5-15	15-1	15-1	5-1	10 x 4.9 x 2.1	2.0
LMG5-20	5-20				9 x 4.9 x 2.1	1.8
LMGT150/12	5-20	12-3	12-3		12 x 4.9 x 2.1	2.4
LMGT150/15	5-20	15-2.4	15-2.4		12 x 4.9 x 2.1	2.4
LMGT150/12/5	5-20	12-3		5-1	12 x 4.9 x 2.1	2.4
LMGT150/15/5	5-20	15-2.4		5-1	12 x 4.9 x 2.1	2.4
LMGT150/24/5	5-20	24-1.5		5-1	11.5 x 4.9 x 2.1	2.4
LMGQ150/12	5-20	12-3	12-3	5-1	13 x 4.9 x 2.1	2.6
LMGQ150/15	5-20	15-2.4	15-2.4	5-1	13 x 4.9 x 2.1	2.6
					INCHES	POUNDS

Note: *Multiple outputs require 3 amp. minimum load on main output to ensure auxiliary regulation on 75 watts and 4 amp. minimum on 150 watts.*

TEMPERATURE RANGE



DC-DC Series

250 Watts, DC-DC, triple

This versatile DC/DC unit operates from both standard and telecommunications batteries which provide excellent specification of outputs including all facilities for use in a fully redundant parallel mode.

INPUT

Voltage: 21-56 V.D.C.

Frequency: DC

Hold up: N/A

OUTPUT

Regulation: TEB = +3.5% – 1.5%

Ripple: 1% pkpk DC-30MHz

Temperature Coefficient: See reg

Remote Sensing: 5% min.

Transient Response: 3% for 25% load change, regulation in 2mS

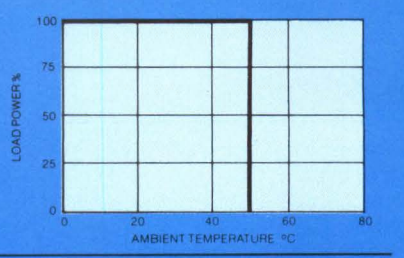
Overload: Constant current 120%

Overvoltage: All outputs

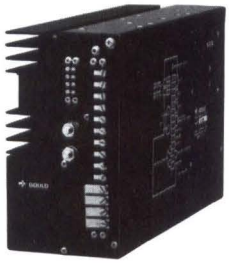
PART #	MAIN	AUX 1	AUX 2	SIZE	WEIGHT
MGT 250	5-25	12-8	12-8	19"rack 3½ x 12	20
				INCHES	POUNDS

Note: *see data sheet for controls and alarms.*

TEMPERATURE RANGE



Multiple Output Series



150-650 Watts, AC-DC, 2, 3, 4 outputs

These products have been designed to meet the needs of major DP and telecommunications users where multiple outputs are demanded by different system technologies. Individual specification sheets highlight their major features. Most types are re-packages of the MG family.

INPUT

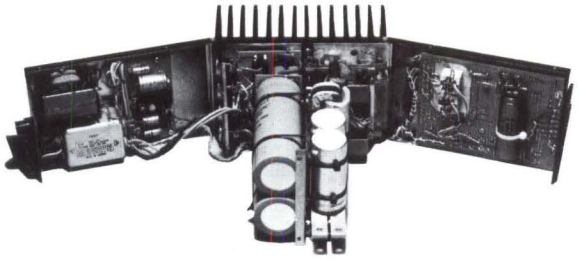
Voltage: 92-132/176-264
Frequency: 47-63Hz
Hold up: 28mS at 100% load from 103.5 or 198 volts

OUTPUT

Regulation: 0.1% full line & load
Ripple: 50mV pkpk DC-30MHz
Temperature Coefficient: 0.01%/°C
Remote Sensing: 500mV
Transient Response: 500mV for 90% load change, regulation in 2mS
Overload: Constant current 110%
Overvoltage: All main outputs most auxiliaries

PART #	MAIN OUTPUT	AUX 1	AUX 2	AUX 3	SIZE	WEIGHT
*MGD500	5-80	2-50	—	—	5 x 8 x 11	12
MGT5-20/12	5-20	12-1.75	12-1.75	—	3½ x 6 5/16 x 6⅞	7.5
MGT5-20/15	5-20	15-1.75	15-1.75		3½ x 6 5/16 x 6⅞	7.5
MGT400	5-60	12-8	12-8	—	5 x 8 x 11	16
**MGQ300	5-30	6-6	28-2	28-2	3.9 x 7.5 x 12.25	13
MGQ400	5-30	5-5	12-7.5	12-7.5	5 x 8 x 11	16
*MGQ650	5-110	5-10	12-10	12-10	7 x 5 x 18	18
					INCHES	POUNDS

Note: *Fan cooled.
**Requires external fan cooling



Custom Capabilities

Gould is a multi-national company with multi-national power supply design capability. We are just as familiar with designing power supplies to meet the RFI or safety specs in Europe as in Japan or the U.S. In fact we have service facilities in more than 34 countries.

Here are five ways we work with our customers to meet their custom needs in the most economic manner:

1. **Adjusted Catalog —** sometimes a slight adjustment of a standard catalog unit is all that's needed such as changing a 5V to a 6V unit.
2. **Assembled Catalog —** assembling a number of standard units in a custom rack.
3. **Modified Catalog —** making substantial internal changes during manufacturing.
4. **Re-packaging Custom —** using standard circuits in a custom design or package.
5. **100% Custom —** building a unit from scratch to meet the exact customer need. This often involves technology development.

SMG Series

(Fan cooled)

500-2250 Watts, AC-DC, single output

High power, fan cooled units designed for large computer and telecommunications applications. Extensive software controls on every model and excellent price/watt with better than average specifications on temperature and hold up.

INPUT

Voltage: 103-127 & 207-253 (front panel switch)
Frequency: 47-63Hz
Hold up: 22mS at 110% load from 103V or 207V line

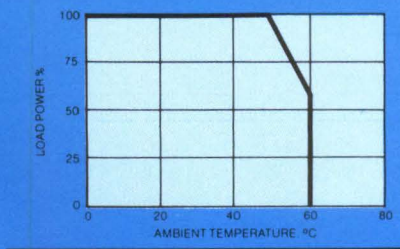
OUTPUT

Regulation: 1.0% full line & load
Ripple: 60mV pkpk (100mV on 5-450) DC-20 MHz
Temperature Coefficient: 0.01%/°C
Remote Sensing: 1000mV @ 5 volts
Transient Response: 50mV for 10% load change, regulation in 2mS
Overload: Constant current @ 110%
Overvoltage: Standard

PART #	VOLTS	AMPS	SIZE	WEIGHT
SMG5-100	5	100	3.1 x 7.8 x 10	11.44
SMG5-100L	5	100	5.2 x 14.4 x 5	14.96
SMG5-150	5	150	5.2 x 14.4 x 5.9	16.28
SMG5-150S	5	150	5 x 8 x 11	16.28
SMG5-300	5	300	5.2 x 14.4 x 10.8	28.60
SMG5-450	5	450	5.2 x 14.4 x 14.8	48.40
			INCHES	POUNDS

Note: *SMG5-450 is 3 phase only @ 230 V. ALL UNITS have TTL signals for overvoltage, overcurrent and undervoltage. Overtemperature signalled by relay closure.*

TEMPERATURE RANGE



MMG Series

25-50 Watts, AC-DC, single output

Optionally card mounted, this compact family is especially designed for worldwide use and units meet all major international safety specifications.

INPUT

Voltage: 99-132 & 198-264
Frequency: 48-63Hz (400 optional)
Hold up: 28mS at 50W from 115 or 220V – 10%. 25W requires external capacitors.

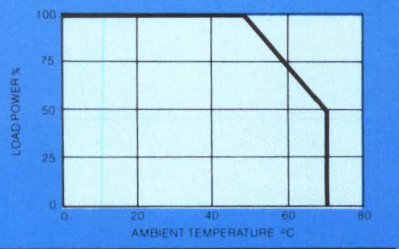
OUTPUT

Regulation: 0.1% full line & load
Ripple: 50mV pkpk DC-30MHz
Temperature Coefficient: 0.01%/°C
Remote Sensing: 250mV
Transient Response: 300mV for 90% load change, regulation in 2mS
Overload: Constant current 110%
Overvoltage: Standard

PART #	VOLTS	AMPS	SIZE	WEIGHT
MMG 5-5	5	5	6.3 x 3.46 x 1.3	1.15
MMG12-2.5	12	2.5	6.3 x 3.46 x 1.3	1.15
MMG15-2	15	2.0	6.3 x 3.46 x 1.3	1.15
MMG24-1.4	24	1.4	6.3 x 3.46 x 1.3	1.15
MMG 5-10	5	10	3.46 x 2.75 x 6.5	2.3
MMG12-4.8	12	4.8	3.46 x 2.75 x 6.5	2.3
MMG15-4	15	4	3.46 x 2.75 x 6.5	2.3
MMG24-2.5	24	2.5	3.46 x 2.75 x 6.5	2.3
			INCHES	POUNDS

Note: *25W unit available P.C. card mounted.*

TEMPERATURE RANGE



A Gould applications engineer is ready to answer your applications/ technical questions concerning switching power supplies. Just call us on our new toll free line (800) 423-4848. Or consult the Gould representative below covering your state.

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August 1979

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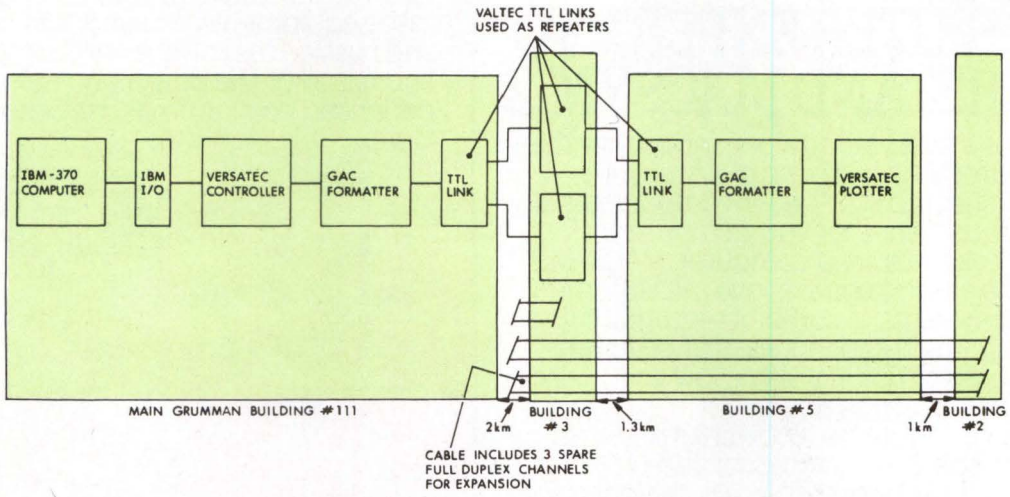
Fiber Optic System Links Plotters to Computer

A high capacity fiberoptic data transmission system installed at Grumman Aerospace Corp, Bethpage, NY, allows 2-way transmission between an IBM 370 mainframe at the company's headquarters building and interactive plotter terminals located in another building more than 3 km distant. The system employs MGO-5 cables and TTK data links by Valtec Corp, W Boylston, MA 01583, using one of four available pairs of fibers; the remaining three pairs are for future expansion of the system.

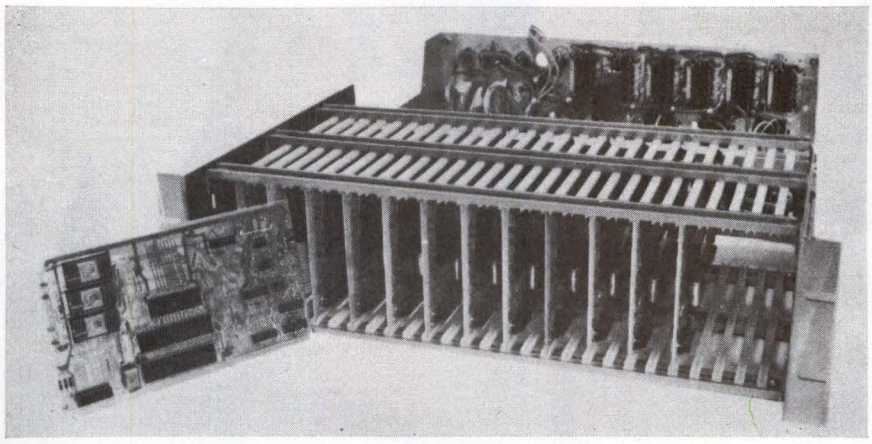
The optical system is designed to interface with electronic systems, which allows non-specialized technical personnel to connect additional data links. The main computer and its inhouse designed data formatters deal only with electronic signals; all optical signal conversions are performed within the data links. Link units are also used as repeaters or boosters enroute.



Fiber optic data transmission system. 3-km+ system enhances Grumman's existing interactive computer aided graphics operation, which uses computers to generate, maintain, and update engineering drawings and other material

Variety of Protocols Accommodated by Line Controller

DLC data line controller provides any computer with proper electrical interface and signalization protocol for Telex, leased lines, and others as appropriate. The microprocessor driven unit allows computer communications software and hardware to be isolated from external line requirements. DLC is a per-line printed circuit board unit that interfaces a variety of terminals and computers with differing protocols to their switching and data processing systems. It is being offered to end users and OEMs by Plessey Fairfield, 1275 Bloomfield Ave, Fairfield, NJ 07006.



Data line controller rack and card. Each rack can house up to 24 DLCs. Power is self contained within rack, and panel containing power displays, switches, fuses, and external connectors is mounted at rear of rack

Heart of the DLC function is the microprocessor module driven by a 4 MHz crystal from which is derived a 1-μs cycle time. 128-word scratchpad RAM and internal clock driver are added features. The module performs its tasks via stored programs that can be changed to fit specific applications.

A 6k maximum P/ROM module has three chip locations which accommodate either 1k or 2k P/ROMs for holding the stored program. The RAM buffer storage module contains up to two chips with a 1-chip configuration capacity of 512 bytes max.

The peripheral interface adapter module controls the output signals to the computer and communication circuits and receives inputs from them. It has two 8-bit registers; register A controls the computer interface, and register B the communication line interface. □

Circle 402 on Inquiry Card

IN MEASUREMENT MACSYM 2 STANDS

YOU DON'T HAVE TO BE A COMPUTER EXPERT TO UNDERSTAND MACSYM 2.

MACSYM 2 is a basic, stand alone interactive real-time measurement and control system. It's human-engineered so it's easy-to-understand and easy-to-use whether you're more comfortable with a calculator or a computer. MACSYM 2 stands alone among competitive measurement and control systems. It combines integral signal conditioning, multi-tasking, ease of programming, and ease of use in a single low cost, self-contained system.

MACSYM 2 gives you a powerful minicomputer with a fast 16-bit processor and up to 128 K bytes of memory specifically designed for a variety of applications involving signal conditioning, data collection and concentration, measurement and control, storage, manipulation, computation and display. It puts real-world computer power at your fingertips without prior computer experience or separate development systems. For less than $10,000*, you can get a complete MACSYM 2, ready for operation, packaged as a single compact, desktop unit (also rack-mountable) for all of your real-time measurement and control applications.

MULTITASKING BASIC MAKES IT SIMPLE.

Like the MACSYM 2 hardware, its software has been designed specifically for measurement and control. MACBASIC is an enhancement of easy-to-use, problem-oriented standard Dartmouth BASIC. It features real-world I/O statements, real-time interactive multitasking (you can run as many as 18 independent programs simultaneously), real-time reference, data reduction, storage and presentation.

MACBASIC is a friendly programming language that lets you write programs the way you want. And lets you communicate with your process or experiment in plain English and simple algebraic expressions. For instance, real-world signals can be treated like any other variable. You can also monitor and change variables while your programs are running. And you can develop your programs on the same equipment you run them on. It's easy and hassle-free for the non-computer expert and has all of the power and flexibility the experienced programmer has been waiting for.

* Attractive quantity discounts are also available.

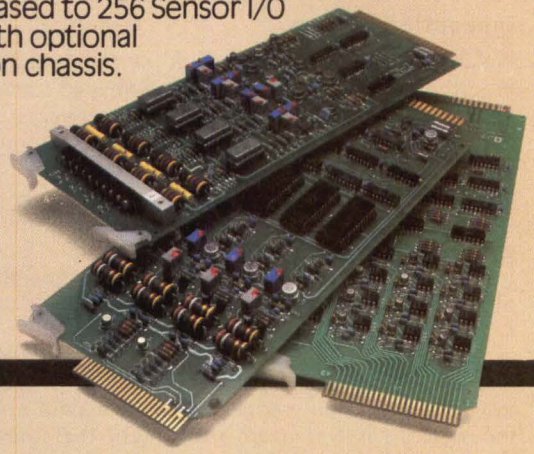
This program assigns values to variables K and L. Instructs MACSYM 2 to input analog data from channel 0; to output data on channel 1; to compare X to L. If greater, to sound alarm on channel 1; if less, to turn off alarm. Wait ½ second, read again. It's that basic.

```
40 K=0.5
50 L=5
60 X=AIN(8,0)
70 AOT(0,1)=K*SIN(X)
80 IF X>L DOT(1,1)=1
90 IF X<L DOT(1,1)=0
100 WAIT .5 GO TO 60
```

AND CONTROL, ALONE.

SENSORS CONNECT DIRECTLY TO MACSYM 2 FOR STAND ALONE REAL WORLD CONTROL.

The key to configuring a low-cost, easy-to-use, sensor-based, real-time multitasking measurement and control system is Analog Devices' unique Sensor I/O cards. They contain all necessary signal conditioning and interface directly with sensors. You can select and match as many as 16 dedicated low-cost Sensor I/O cards in a single, stand alone MACSYM 2. They plug directly into the MACSYM 2 chassis and allow direct sensor hookup by simply bringing your field wiring right into the MACSYM 2 screw terminals. Changing needs merely means changing Sensor I/O cards. Total MACSYM 2 capacity can be increased to 256 Sensor I/O cards with optional extension chassis.



Multi-channel Sensor I/O cards are available for low level and high level analog inputs; voltage or current analog outputs; digital I/O; direct sensor interface with thermocouples, strain gages, RTD's, limit switches and solenoids; pressure, frequency, temperature, flow and motion measurements; IEEE, isolation and other special functions. The unique architecture also makes hookup of optional peripherals such as disk drives, X-Y plotters, line printers or terminals just as easy.

MACSYM 2, the Basic System for Measurement and Control that stands alone. For all the basics, call (617) 329-4700. Analog Devices, Inc., Systems Division, 385 University Avenue, Westwood, MA 02090.

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CIRCLE 26 ON INQUIRY CARD

TECHNOLOGY AND ECONOMICS: POTENTIAL COMPUTER MARKET ELASTICITY—II

Montgomery Phister, Jr

Systems Consulting
Santa Monica, California

Limited both by the number of organizational units that have data to be processed and by the amount of processing that these units must do, the computer equipment market retains a degree of elasticity as discussed in last month's column. While growth in the general purpose segment has leveled off, the minicomputer market remains in a near-exponential expansion phase and the small business computer market is just gaining headway. This month's discussion attempts to identify those areas where activity may be found in a saturated market and what type of activity to expect.

Users replace systems if they wear out, or if maintenance costs become too high compared with equivalent costs of a new system. While equipment "life" in this sense is not precisely known, it probably is greater than 10 years, and certainly greater than the actual 5- to 7-year life of systems replaced today (see Ref 1, pp 12-13). Users will also replace or augment a system to implement new applications. Thus there has continued to be a great deal of activity in the "saturated" GP market, as users replace and add equipment to increase capacity and implement new applications. Whether this replacement/augmentation activity in a saturated market should be expected to die out when and if new applications dry up remains a question, however. Will that occur, and if so, when?

Influential Factors

Nolan argues that the growth of the computer budget in an organization follows an S-shaped curve, leveling off to a fixed annual cost after some years of growth.[2] However, he focuses attention on the management activities associated with various stages of growth, and hardly mentions the applications which are presumably the basis for growth. Lucas and Sutton, in a study of governmental uses of computers[3] find no evidence of a leveling-off of computer budgets, and argue that a model of applications is needed to predict how budgets will grow. Let's examine a possible applications model.

At any given time, any user has a specific DP workload. One way of describing this workload is to recognize that anything stored on media is data; that data are not stored unless there is a nonzero probability that they will some day be processed; that some fraction f (f can be greater than one) of the average number of bytes on file in a year (D bytes) will be processed in that year; and that it takes s elementary DP operations, carried out by machines

The NEC Hammer.

It drives Spinwriter printers at 55 CPS with quiet precision.

NEC Spinwriter™ character printers run at up to a full 55 CPS for a number of reasons.

One key reason is the NEC print hammer. It is unlike any other print mechanism, and its differences make it better.

The Spinwriter hammer is controlled by a simple voice-coil rather than by complex mechanical links and springs. Special alloys in the hammer provide improved reliability and longer life. There are no moving parts, only the hammer itself. No periodic maintenance. No gap adjustments. No lubrication. Ever.

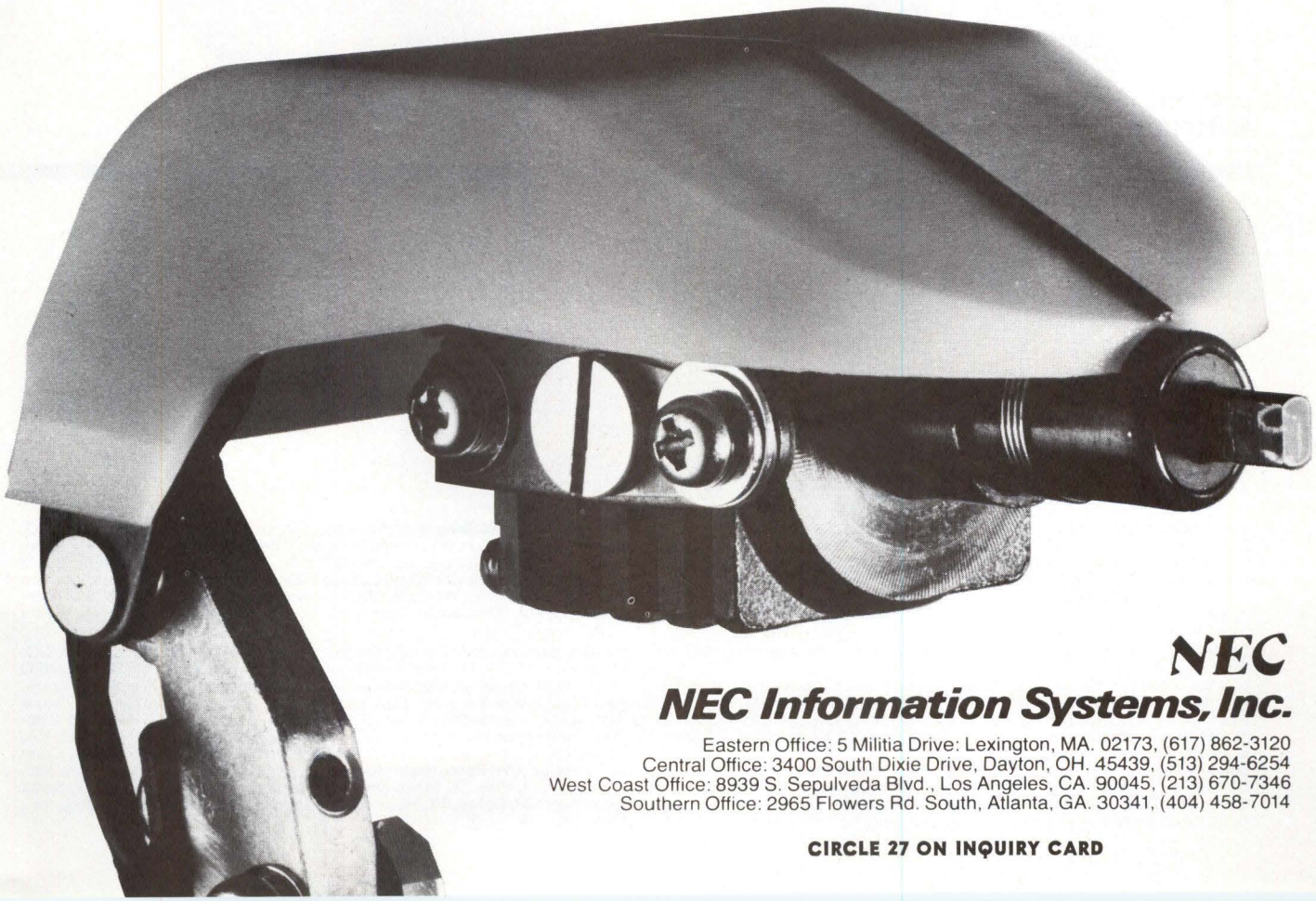
When it prints, the NEC hammer is driven automatically at one of seven preset impact levels, depending upon the size of the character being printed at that instant. An operator-controlled "impact scaling" switch modifies hammer energy to light, medium or heavy impact, depending on the form type and thickness.

This precision of speed, stroke and impact has a number of other advantages, too. One is print quality; Spinwriter printers produce superb correspondence-quality output. Another is quietness; at 62 dbA, Spinwriter printers are quieter than other character printers. And a third is durability; Spinwriter printers are rated at over 2000 hours MTBF, the new industry standard.

The NEC hammer. Its many technological innovations demonstrate NEC's commitment to making the perfect printer.

Send for our new printer brochures.

NEC. Going after the perfect printer.



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CIRCLE 27 ON INQUIRY CARD

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The innovative μPD765, developed and introduced by NEC, has become an industry standard and will soon be second-sourced by a U.S. semiconductor company. It's simple to build into your system, because the standard 40-pin, +5V design is totally compatible with IBM single- or double-density format floppies and 5¼" mini-floppies, as well as standard 8" drives.

It's powerful too, executing 15 complex commands including many subroutines usually found in a disk handler software package. Plus it controls up to four double-sided drives.

And the 765 gives you unequalled flexibility in programming your controller system through such commands as Multi-Sector Reads and/or Writes, Track Formatting, and Multiple Drive Seeks. It operates in either DMA or interrupt-driven mode, and interfaces to all popular microprocessors, including our μPD8080AF, μPD8085A and μPD780 (Z80™).

For board applications, you get all the capabilities above and more. The BP-2190 board includes the 765 and 16K of dual-ported RAM (expandable on-board to 48K), along with priority and refresh logic. Disk-to-RAM transfers are under DMA control

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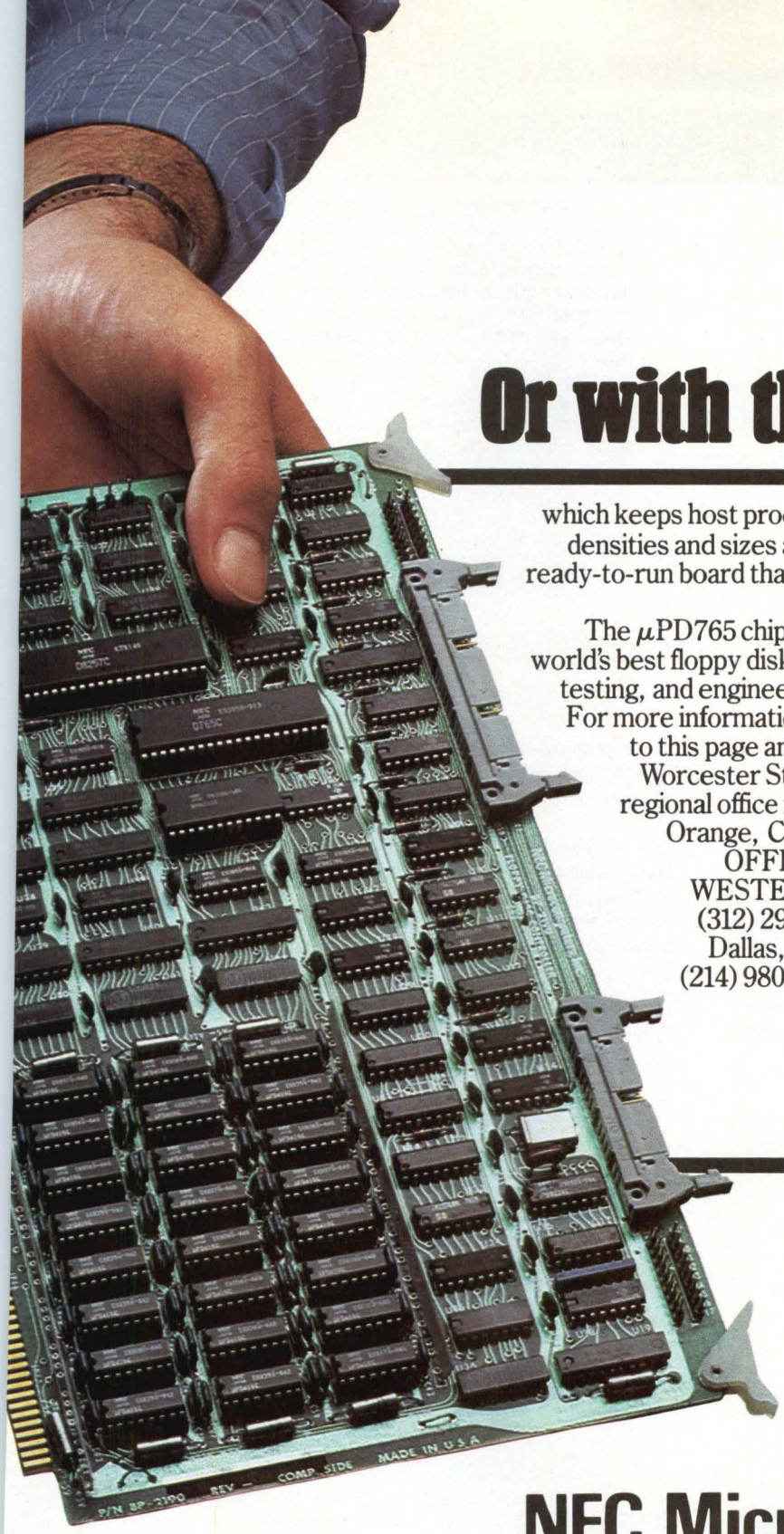

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which keeps host processor overhead to a minimum. And mixed densities and sizes are handled with ease. All of this on a single ready-to-run board that plugs directly into a Multibus™ system—and we'll supply the software drivers, too.

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CD-1

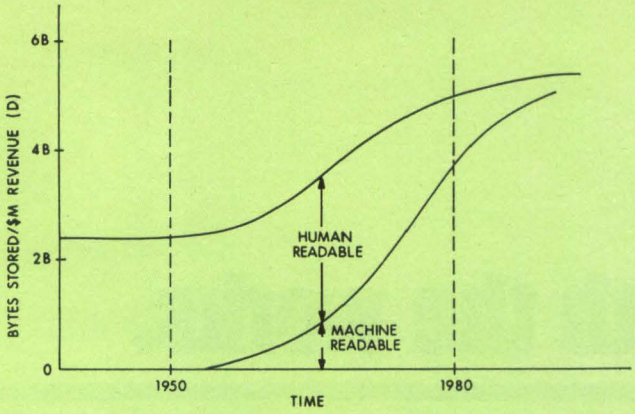

Fig 1 Stored data. At any time, organization has great deal of stored data, some in machine readable form (eg, punched cards or magnetic tape), and some in human readable form (eg, paper in file cabinets). Graph estimates growth in total stored data per million dollars of revenue, and shows how it is distributed between machine and human readable forms in large organization

or humans, to process one byte of data. Then the organization's total workload in any given year is

Workload = fDs operations/yr

In a given organization, f, D, and s are all functions of time.

Some processing is done by DP equipment, and some is done manually. As time goes on, a higher and higher proportion of total processing is done by computers. We may conjecture that:

(1) D increases with time due to increases in business complexity, government regulations, etc. It also increases if the organization itself grows; this effect can be neutralized by normalizing D—dividing it by annual revenue or number of employees.

(2) f has been increasing because computers make it cheap and easy to do calculations (once the programs are written), because some data previously never analyzed are now analyzed, and because new data processing applications manipulate the data in different ways.

(3) s has been increasing because computers make it possible to carry out more complex calculations than were possible before. It also tends to increase as the processing

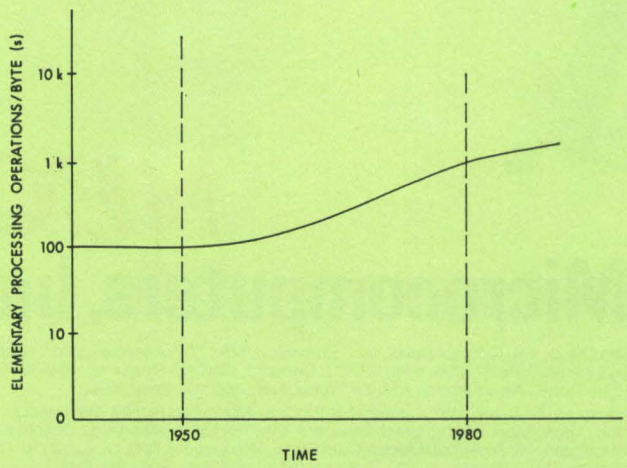

Fig 2 Processing operations per byte of data. "Processing" of data refers to retrieving data from storage, manipulating them, and returning results to storage. Certain elementary operations must be carried out to effect this processing, and this graph estimates growth in number of operations required to process one byte of data

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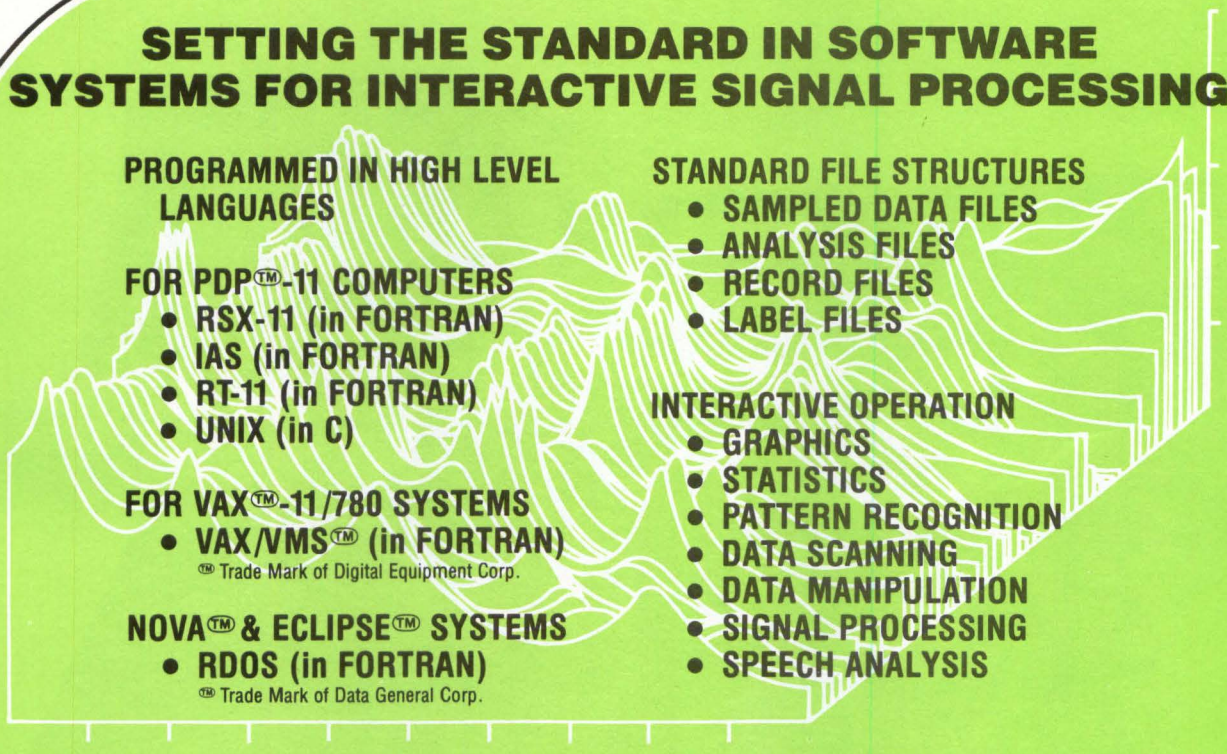

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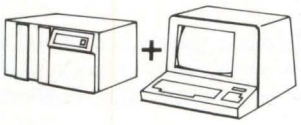
Zilog's powerful Z8000, the generation-ahead 16-bit microprocessor that delivers big computer performance at microprocessor prices, is on the shelf today at Zilog distributors around the country. Order it as the 40-pin Z8002 with 64KB direct addressing, $107.10* Or, choose the 48-pin Z8001 with 8 MB segmented addressing, $139.30* Supporting it is the versatile PDS 8000 family of development systems.

The base package, the Model 10.

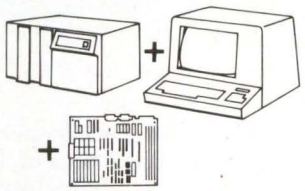
Your most economical entry to Z8000 product development. Everything you need to start your Z8000



software development: a 64K byte microcomputer, CRT, dual floppys, interfaces, 9-slot card cage, power supplies, a Z8000 software development package, operating system, editor, linker and utilities. $10,500*

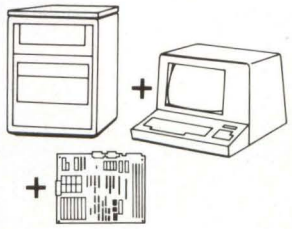
Try it out with the Model 15.

Everything in the PDS 8000 Model 10, plus Zilog's Z8000 Development Module, a Z8000 based computer board with 2K words



of EPROM (expandable to 8K words), 16 K words of dynamic RAM (expandable to 32K words), dual serial interface, 32 programmable I/O lines, four 8-bit programmable counter-timers and a generous wire wrap area. $11,995*

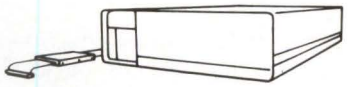
For more complex ideas, Models 25 and 30.



These two PDS 8000 models parallel the capabilities of the Model 10 and 15 but give you the added power of 10 megabytes of rack-mounted hard disc drive. $20,000* and $21,500*

For complete hardware characterization.

Coming soon, an emulation subsystem for your PDS 8000. It will provide total hardware development



support capability for the Z8000 as well as the Z8.

For more information, write.

We'll send you a complete packet of technical data on the PDS 8000 family and Z8000 Development Module together with the name and location of your nearest Zilog distributor. Address: Zilog, 10460 Bubb Road, Cupertino, CA 95014. Or call (800) 538-9367 toll free. (In California call (408) 446-4666.)

*Suggested Domestic U.S. prices only. Z8001 and Z8002 prices are for quantity 100.

CIRCLE 29 ON INQUIRY CARD

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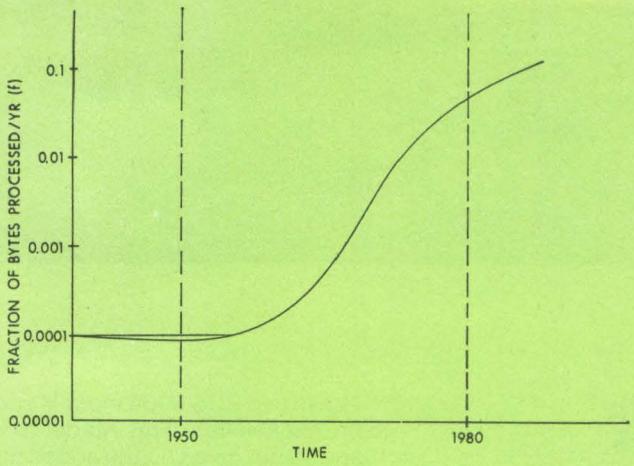


Fig 3 Processed stored data. Not all data stored by organization are processed in given year. Graph estimates fraction of average data in storage during year, which is processed during that year. Author conjectures that proportion has grown remarkably since advent of computer

overhead contributed by operating systems and other tools grows.

(There are, of course, factors which tend to reduce f and s—eg, government regulations or legal worries that encourage the formation of files which have a very low probability of ever being processed; and very simple, low s applications that are encouraged by low cost data processing.)

Average Levels and Trends

Figs 1, 2, and 3 present a suggested set of plots for D (normalized), s, and f as function of time. Fig 4 shows the resulting total workload and indicates how it has been divided between computer and manual operations in a moderately large organization. I have seen no published data on D or f, or on the rate of change of s (Ref 1, pp 82-92 gives some data on s), though these parameters are surely susceptable of measurement. Thus the graphs represent only an educated guess regarding average levels and trends. However, the analysis generally leads to the following conclusions, independent of the exact nature of the curves.

(1) D, f, and s all increased at unusually high rates (compared to the past) with the introduction of computers.

(2) Electronic equipment today surely accounts for the vast majority of data processing done in the U.S. (To convince yourself that this is so, multiply the number of

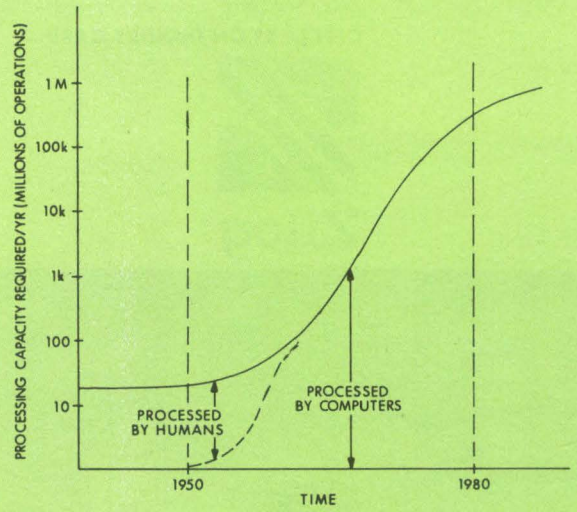
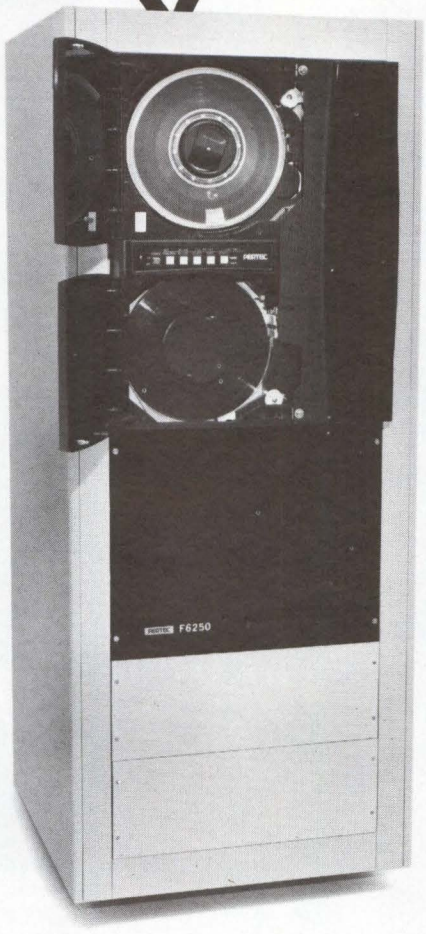


Fig 4 Processing capacity required. Total number of elementary operations required per year to process organization's data is given by fsD, product of elements in Figs 1 to 3. Graph shows that product, and estimates what proportion of total operations are handled by computers. Author conjectures that this curve is S-shaped, that its inflection point has been passed, and that in future, users will not require more computing capacity per million dollars of sales

"Golly, I found a pain in my parity."



The only GCR tape sub-system for minis that troubleshoots itself 3 ways.

This GCR tape transport subsystem gives you three self-diagnosing systems, each in a different mode.

First, there's the only continuous self-circuit-checking system on the market. Then, in the off-line mode, via a built-in key-board, there's full fault isolation right down to the board level. And finally, in the on-line mode, there's PCC's superior total check-out diagnostic system which also has fault isolation to the board level.

Besides this unique 3-level diagnostic capability you get GCR recording density of 6250 bpi and a transport speed of 125 ips all in a 19"x24" package.

You also get the simplest interface in the business. By far. Direct parallel transfer 16-bit words, all in only 29 lines.

The PCC GCR—the tape transport system with three built-in doctors. So there's no waiting.

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Introducing the 100 MHz 465B.

For years, the 465 Portable Oscilloscope from Tektronix has been considered the industry standard by those who service high performance or computer-based electronic systems.

The best just got better. Now there's the 465B. It still does everything that made the 465 so popular. But it's even more versatile. New alternate switching capability between intensified and delayed sweeps lets you view both displays for analysis. There's third channel trigger view with delay adjustable to zero so you can view both data channels and the trigger signal simultaneously. Improved trace selection switching provides unmatched flexibility in waveform display. And we've upgraded the magnified sweep speed to 2 ns/div so you can analyze signals in even greater detail. These new features help you interpret complex timing signal relationships more clearly.

We've improved it beneath the cover, too. Though it looks like a 465 on the outside, the 465B is different inside. We've used modern IC's in place of discrete components. That means improved performance, reliability, and trace quality for you.

Service you'd expect from the leader. Our worldwide service team goes where you go. We're with you all the way, with more than 500 service personnel at 46 Tektronix centers in the U.S.A. and hundreds of Tektronix-supported service engineers in over 50 other countries to calibrate and maintain your Tektronix scope.

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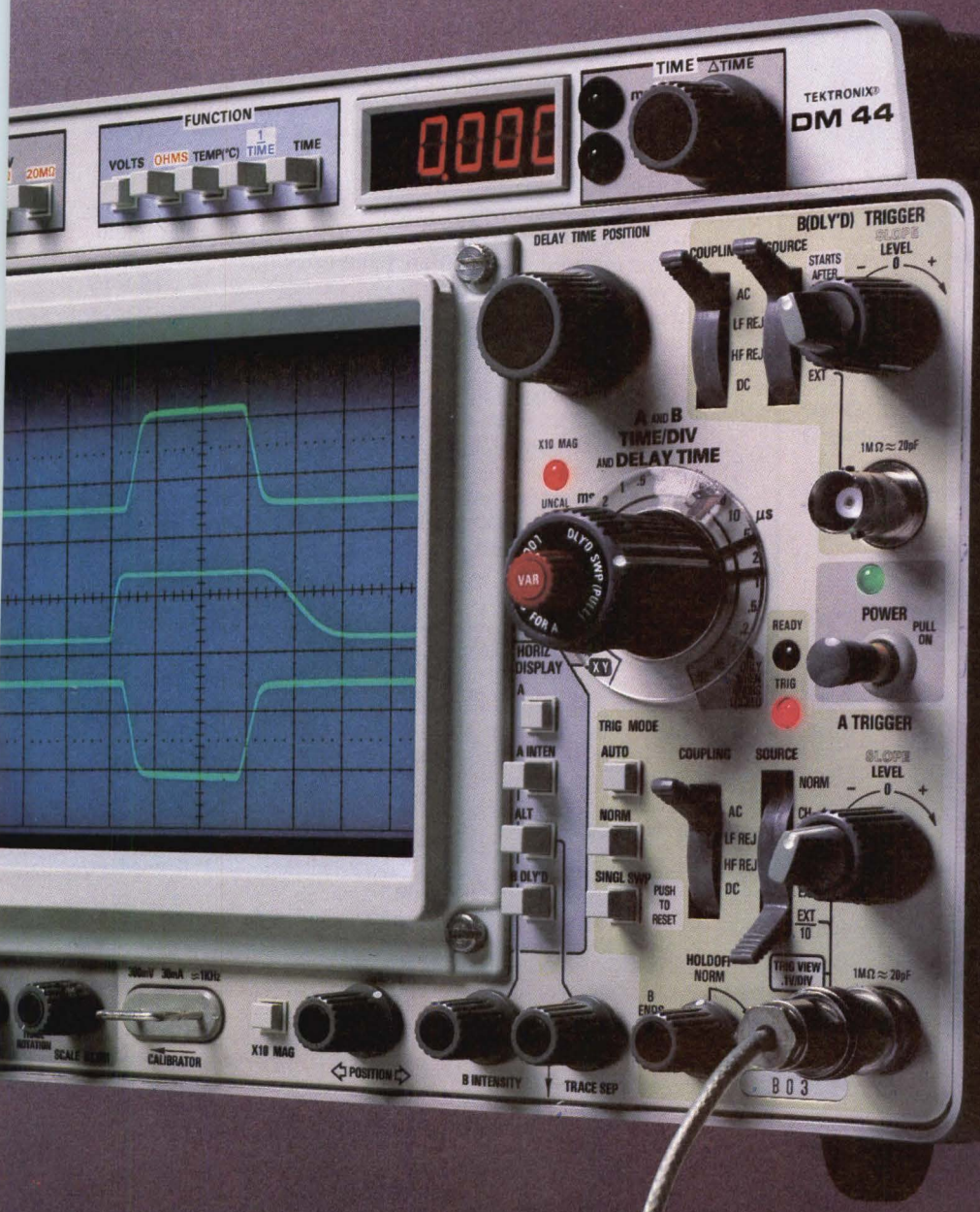
We're going places

raised standard.



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U.S. clerical personnel by your estimate of the number of processing operations each can perform per second, and compare the result with the U.S. computer population multiplied by your estimate of its average processing rate. I estimate that the computer rate became equal to the clerical rate in about 1960.)

(3) If my conjecture about the nature of the curves for D, s, and f is correct, then Nolan's conjecture about the S-shaped nature of the history of a computer budget will not hold. For my conjecture implies that, at some point, users will find no new applications to implement, and the processing to be done per revenue dollar (or per employee) will level off. However, with every passing year, the computer power required to do that processing becomes cheaper; and with fewer or no new applications, the manpower required to prepare programs also becomes cheaper. Therefore, the DP budget per employee should level off *and then decrease* as time goes by. The DP industry, which has during its infancy grown much faster than the economy, will grow more slowly than the economy and will ultimately shrink. That is to say, there will come a time when computers are, for the most part, sold as replacements only. Since the replacement cost of a system which cost $1 million 10 years ago will be $0.1 million today, annual dollar hardware sales will actually decrease.

That potentially interesting situation remains some years away although (as noted previously) the general purpose market has entered the phase when mostly replacement systems are sold. In addition some existing factors tend to put off the day of reckoning. For example, some scientific and engineering problems have a seemingly inexhaustable appetite for computing power—in some design or analytic situations there seems to be no end to the permutations and combinations to be tried, or to the fineness of the grid to be examined. For another example, most organizations have a fixed annual budget for data processing, and do not tie their budgets to the cost of computing or to the amount of computation to be done. As long as such policies hold, those organizations will continue to acquire both computing power and new facilities for the collection and distribution of data.

We in the industry must, however, be aware of the possibility that the ultimate market is fixed and limited, and must be interested in studies that refute or confirm the conjectures presented here. The alternative conjecture seems to be "we'll always be adding new applications," which goes with the Parkinsonian concept that the work will expand to fill tomorrow's ever-growing computer capacity.

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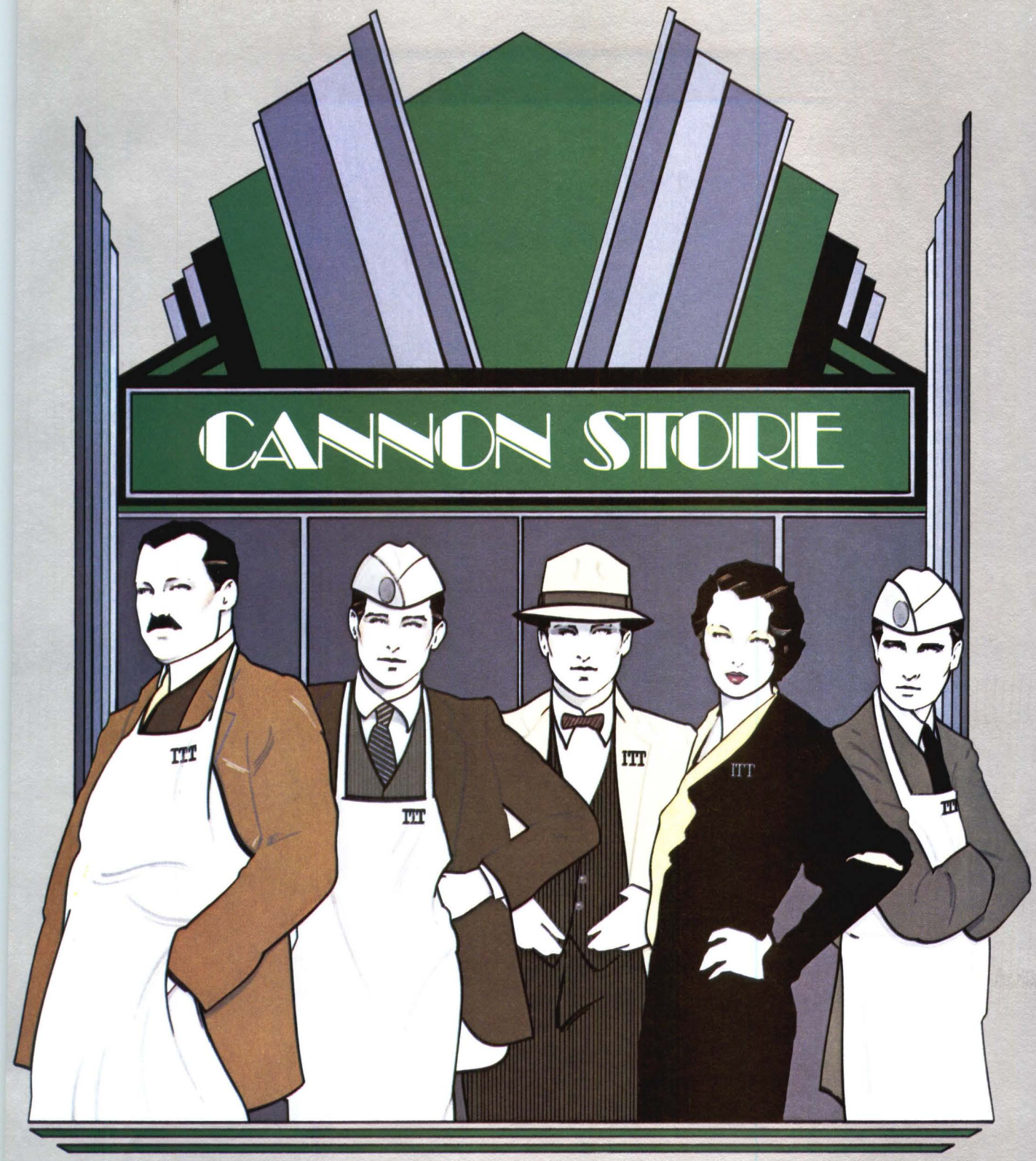
1. M. Phister, *Data Processing Technology and Economics*, Santa Monica Publishing Co, Santa Monica, Calif, 1976
2. R. L. Nolan, "Managing the Computer Resource: A Stage Hypothesis," *Communications of the ACM*, July 1973, pp 399-405
3. H. C. Lucas and J. A. Sutton, "The Stage Hypothesis and the S-Curve: Some Contradictory Evidence," *Communications of the ACM*, Apr 1977, pp 254-259

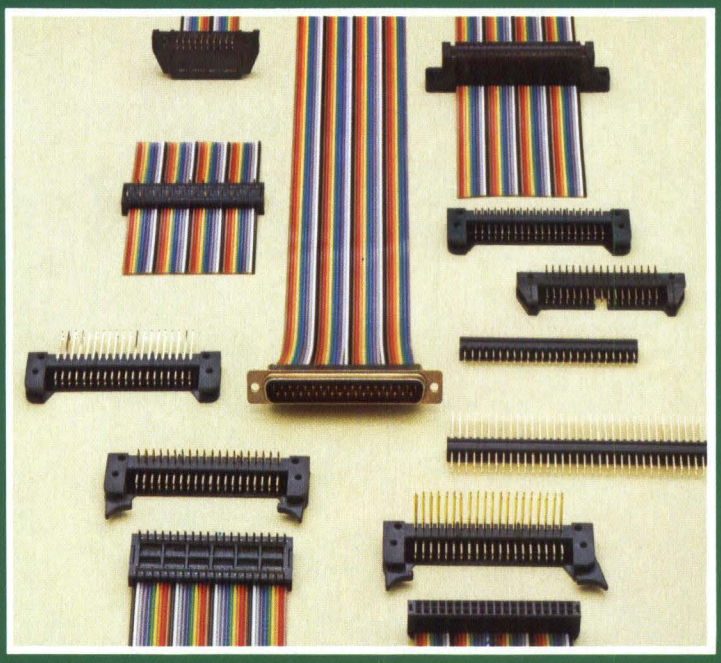
The Author solicits comments on the material presented here, data supporting or contradicting his approach, and suggestions for topics to be explored in future articles.—**Ed.**



WHO CAN SOLVE ALL YOUR MASS TERMINATION AND ZERO FORCE CONNECTOR NEEDS?

ITT CANNON CAN!

THE CANNON® MASS TERMINATION CONNECTOR STORE KEEPS GROWING.



Packaging success in low cost, high performance connectors.

In the news today, the ITT Cannon Electric store expands mass termination products.

Why? In-depth reports show big need for low cost, high quality packaging in communications, computer, control and other electronic industries.

What is ITT Cannon doing?

Expanding their product line with a comprehensive array of interconnects. Mas/Ter™-D Subminiatures. Edgecard. DIP. PCB. Receptacle. Header and transition connectors. And ribbon cable in #26/28 AWG stranded and solid wire.

What's the big story?

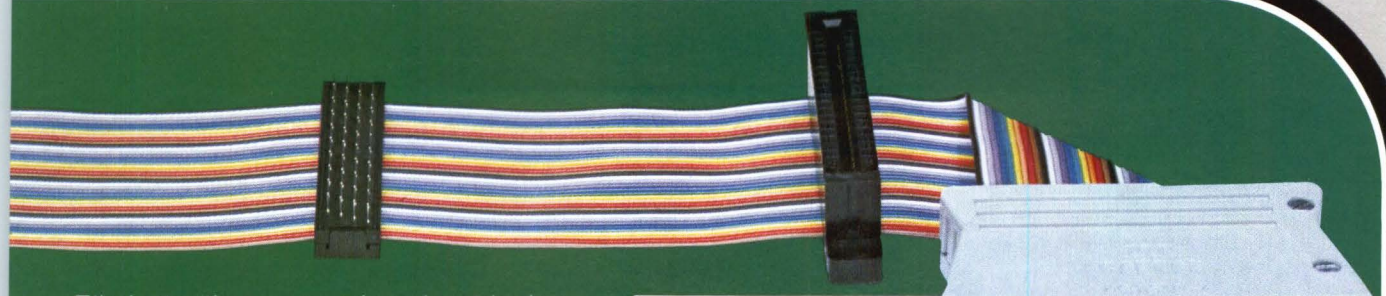
Mas/Ter™-IDC insulation displacement connectors. Here are the key facts.

..High speed mass termination of round conductor flat cables.

..Up to 60 mass terminations handled in a single, simple operation.

MAS/TER™- IDC PRODUCT

	NUMBER OF CONTACTS: 8	9	10	14	15	16	20	24	25	26	34	37	40	50	70
Mas/Ter-D CONNECTORS D Subminiature pin and socket connectors provide reliable, high-speed mass terminations of flat ribbon cable at a lower total installed cost.		●			●				●			●			
Mas/Ter 90° D*P CONNECTORS 90° PCB flame-retardant connectors, fully intermateable with all D Subminiature types, can be mounted directly over PC patterns without short circuiting.		●			●				●			●		●	
Mas/Ter G08 HEADERS (SHROUDED) For 2-piece connector applications requiring fast and dependable disconnect/connect capability, headers are permanently mounted on a PC board and mate with the ribbon-terminated G08 receptacle.			●	●		●	●			●	●		●	●	
Mas/Ter G08 HEADERS (UNSHROUDED) Double readout male connectors useable with both Mas/Ter G08 receptacles or UBC crimp housings.	●	8 thru 70 (even increments)													●
Mas/Ter G08 RECEPTACLES Socket receptacle for termination directly to ribbon cable, mates with PC board-mounted headers or PC boards having .025" (0.64) square pins on .100" x .100" (2.54 x 2.54) grid patterns.			●	●		●	●			●	●		●	●	
Mas/Ter RTG08A DUAL INLINE PLUG CONNECTORS DIP connectors terminate directly to ribbon cable and can be permanently soldered to the PCB board or used as a plug-in to IC sockets.				●		●		●					●		
Mas/Ter RTG08B PC BOARD TRANSITION CONNECTORS High density PCB connector provides soldering interface between ribbon cable and PC board. When terminated, interconnects electrically with all .050" (1.27) centers etched circuitry.			●				●			●	●		●	●	
Mas/Ter G03 EDGECARD CONNECTORS Edgecard connectors are designed for .050" (1.27) center direct ribbon cable interconnections to standard .062" (1.57) thick PC boards having .100" (2.54) center spacing.							●			●	●		●	●	
Mas/Ter RIBBON CABLES Available as twisted pairs or flat cable; fully compatible with Mas/Ter Interconnect System.															
Mas/Ter TOOLING Versatile termination hand press tools and shears to assure fast, reliable assembly.															



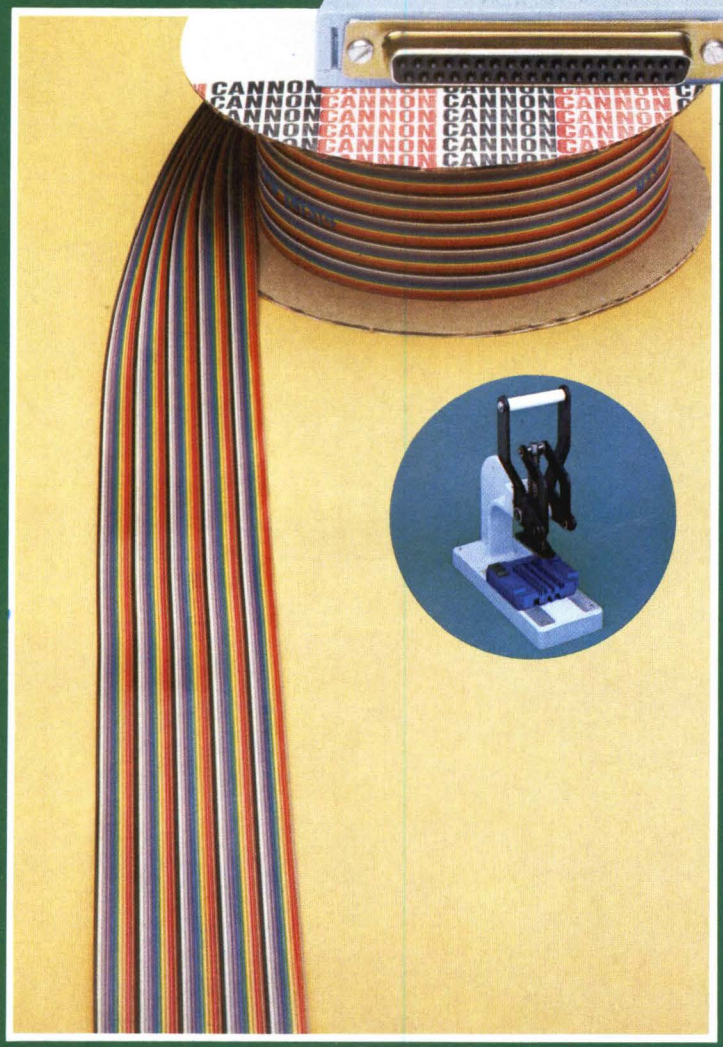
..Eliminates time-consuming wire stripping, crimping and soldering.
..Simple hand tools do the job.

The results?

High speed mass termination and reduced labor costs. In summary—lower total installed costs than other types of mass termination connectors.

Want more details? Tune into the rest of this report. Beginning with a product summary. An availability report. And a technical support feature. Later, we'll tell you where to write for product literature.

You'll see why when it comes to mass termination connectors... Cannon's got it!



No shell game with ITT Cannon Electric

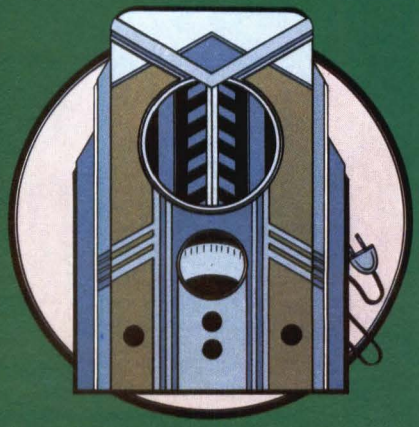
ITT Cannon gives you complete component compatibility from shells to ribbon cable. The story is availability and it all adds up to broad product choice and single source supply. Here are the facts.

..Junction shells for Mas/Ter-D ribbon cable connectors are made of tough, gray thermoplastic and available with optional locking mechanism.
..Mas/Ter-D ribbon cable available as twisted or flat pairs. Light and flexible. UL recognized conductor styles.
..Flat ribbon cable made with #28 AWG 7 strand conductors. Precisely positioned on .050" (1.27 mm) centers. PVC laminating material standard. Others optional. 20 to 50 conductors per cable.

Do-it-yourself tooling

A big part of the ITT Cannon growth story is the customer tooling you get for quick, simple terminating. The entire operation takes place at a single work station with one stroke of the lightweight press. No insulation stripping. No complex tooling.

All Mas/Ter-IDC connectors can be terminated with one press. A simple change of locator block position makes this possible.



OTHER PRODUCTS FROM THE CANNON STORE.

"ZIF"...ZERO INSERTION FORCE CONNECTORS.

A TWIST IN THE NEWS.

The news is full of stories reporting growth in electronic, micro-processor and peripheral markets. That means the need is also growing for low cost, high-performance, multiple-wire power and signal connectors.

The Cannon® DL Series of zero insertion force connectors fills the need. Here's the report.

..Minimum rated life of 10,000 connection cycles with no performance loss.

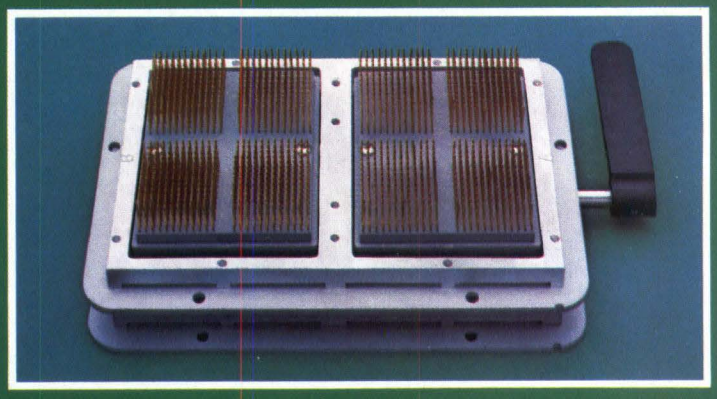
..Mating time is less than 2 seconds. Even with as many as 2496 contacts.

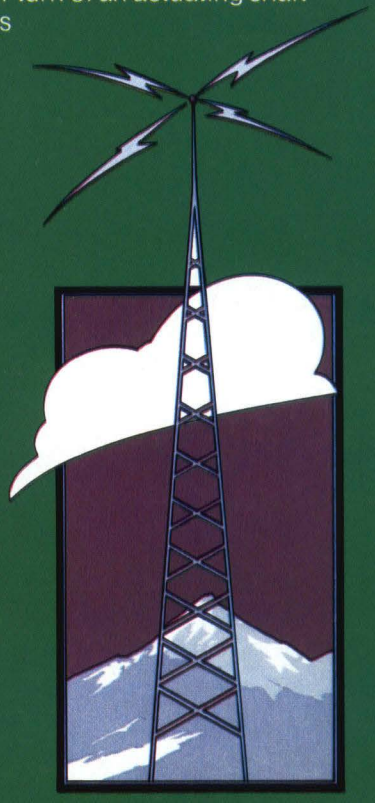
..Cost less per mated line than competitive high-density rack-and-panel connectors. Up to 25% less in some cases.

..ZIF design is the key. Contacts in plug and receptacle don't touch while connector halves are being engaged.

..A simple quarter turn of an actuating shaft mates all contacts at once.

..Engagement force is zero—connector life dramatically increases.





AND NOW A RECAP.

The growth of the ITT Cannon store is good news for you. Product offering is broader. Availability is increased. And our technical support gives you added service.

That's why we conclude, for mass termination connectors...Cannon's got it!

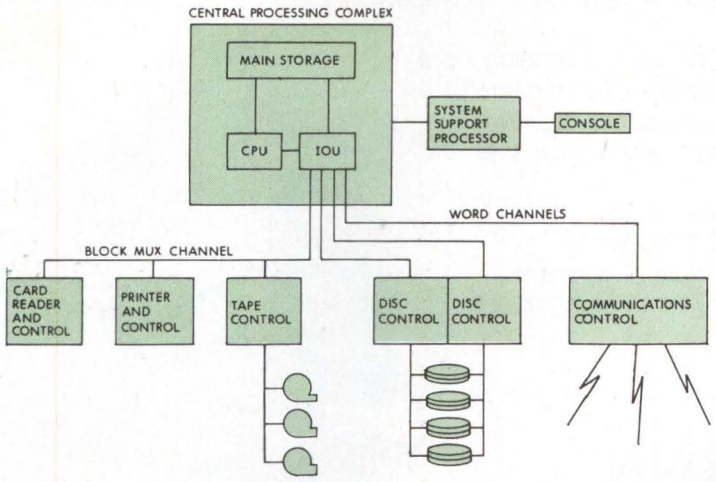
GET THE FULL CANNON STORY.

For more information on the full range of products available from the Cannon Mass Termination Store write to: Manager Rectangular Division, ITT Cannon Electric, 666 East Dyer Road, Santa Ana, California 92702. For 24-hour service, call toll free (800) 854-3573; in California (800) 432-7063. In Canada, contact Marketing Manager, ITT Cannon Electric, Canada, a Division of ITT Industries of Canada Limited, Four Cannon Court, Whitby, Ontario, LIN 5V8, (416) 668-8881.

Six decades on the leading edge of interconnect technology.

CANNON ITT

Large Scale Computer Gains Performance With Multimicroprocessor Architecture



Designed for efficient multiprocessor capability, Sperry-Univac's Series 1100/60 processor architecture permits CPUs to perform multiple tasks simultaneously under control of single common executive system. Central processing complex made up of single or multiple CPU, input/output units, and main storage unit is basis of six different configurations

Implemented in LSI with a multiple microprocessor based architecture, the Series 1100/60 announced by Sperry-Univac, PO Box 500, Blue Bell, PA 19424 uses paralleled microprocessors to gain design flexibility, improved performance, and increased reliability. The design strategy allows a competitive price/performance ratio and permits reductions in size of processor, main memory, and I/O hardware with consequent savings in power and environmental requirements.

Units can be configured in six different processing levels, producing nearly a 5-fold growth in performance. Unit processor models account for four levels, while multiprocessor configurations offer an additional two. In addition main storage capacities for each processor start at 524k 36-bit words and can be expanded in 256k-word increments to a maximum of 4M bytes for uniprocessors (8M bytes for multiprocessor configurations). Main storage is formed from 16k MOS RAMs that operate with an 575-ns average access time.

System performance ranges from about twice to almost nine times that of a Univac 1106. In relation to IBM units, the performance spectrum ranges from below the 4341 to approximately equal to a 3032.

Unit processor complexes contain central processor, I/O unit, and main storage, and are housed in a single cabinet to reduce costs, cabling, and interconnection time. The CPU incorporates LSI microprocessor chips (10800 4-bit slice circuits) with ECL circuitry functioning under microprogrammed control. The processor's instruction set is microprogrammed using a separate random access control store. Reliability is enhanced through the use of duplex checking, instruction retry, extensive parity generation and checking, and control store error detection and correction.

Arithmetic and logic operations are performed in 36-bit master microprocessors, each made up of nine 4-bit ALU slice chips. Each of the two master microprocessors is paired with a second duplicate microprocessor that performs the same function on the same data every microcycle. At the end of a cycle, a comparison check is made between the output of the main and duplicate microprocessors to insure validity of operation. Shifter, logic function computer, and control store address generator are also duplicated. A hardware instruction retry mechanism allows the system to recover from most transient faults, transparent to the operating environment.

Microcontrol store is error checked and includes an error correction technique to assure continuous operation. All memory in the system includes parity or ECC with parity; buffer storage includes an override mechanism which automatically bypasses inoperative portions of the buffer.

An input/output unit includes one block multiplexer channel and four 36-bit parallel word channels. Expansion capabilities allow channels to be added to a maximum of 3 block and 8 word channels or 2 block and 12 word channels.

Interfacing directly to the main processing complex, the system support processor (SSP) is a separate miniprocessor dedicated to support functions for the central processor complex. Its principal functions are to handle the system console, perform systems management functions, and support diagnosis and maintenance of the central processing complex.

Fault detection capabilities of the system enable faults to be detected and isolated to a small area of circuitry—usually to within one or two printed circuit cards and frequently to the chip level. Among the maintenance and diagnostic support features incorporated in the machine are integrated scan set circuitry, fault isolation diagnostics, built-in logic analyzers, fault injection, and error logging.

Series 1100/60 central systems range in price from $318,975 for an

Adac System 1000 handles a ton of I/O functions.

In its simplest form, the System 1000 functions as a low cost peripheral expander to minicomputers. When incorporating a DEC LSI-11 microcomputer, it acts as a stand-alone data acquisition and control system or as a remote intelligent terminal.

No other data acquisition system comes close to offering so many analog and digital input and output modules. Functional analog cards communicate directly with thermocouples, load cells, strain gauges, isolation amplifiers, transmitters and strip chart recorders to name a few. Discrete cards communicate with switch contacts, relays, thumb wheel switches, pumps, motors and many other devices.

A single System 1000 provides up to 700 high level analog input channels, or 128 analog low level input channels, or 700 digital I/O functions. For even greater capacity, a bus repeater card allows additional System 1000s to accommodate as many modules as desired.

System 1000 in the stand-alone configuration can be supplied with up to 32K of memory and DEC RT-11 software.

If you are interested in an extraordinary data acquisition system, you must check out the System 1000. Nothing compares with it.

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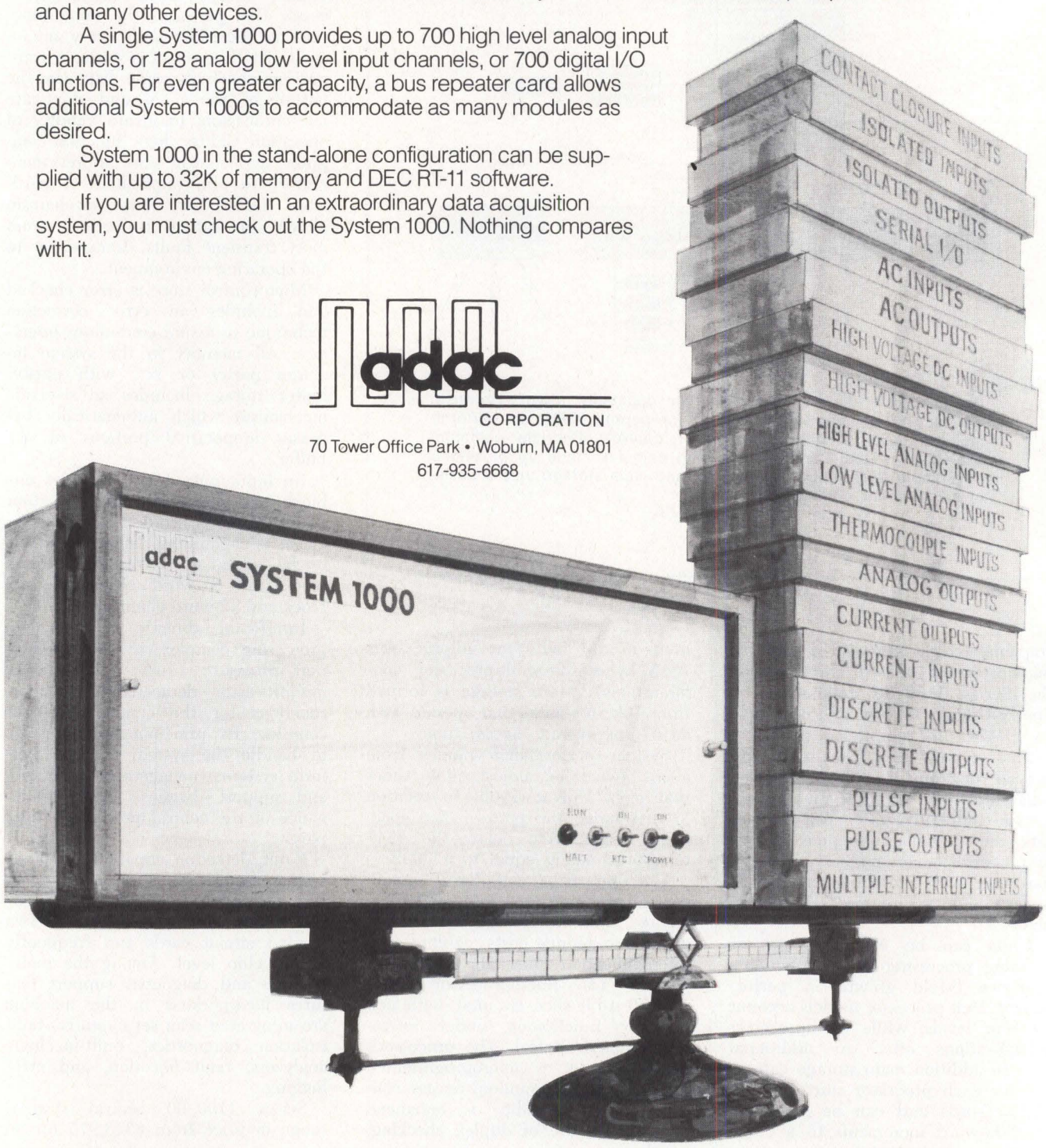


entry level model C1 with 2M-bytes memory to $1,442,075 for a multiprocessor model H2 with 4M-bytes main memory. C1 uses the basic 1100 instruction set; C2 has an extended instruction set designed to increase the efficiency of high level business oriented languages and systems software. H1 and H2 processors are high performance systems featuring an integrated high speed buffer storage and multiprocessor capability as well as basic or extended instruction set. H1 and H2 models expand to multiprocessors with fully redundant tightly coupled features, and are designed to address situations where high performance and maximum system availability are needed.

Circle 175 on Inquiry Card

Cluster Controller Eases Transition to Distributed Processing

AOS Remote Cluster Executive 70 (RCX70) software emulation package, designed for Eclipse computer systems running under the Advanced Operating System (AOS), allows easy transition from existing IBM 3270 applications into distributed data processing. In addition to using the standalone capabilities of an AOS system, the software provides a dynamic link to the remote host computer, and allows access to all data whether stored in the central system or at the local site.

This software emulation package, from Data General Corp, Rt 9, Westboro, MA 01581, permits immediate and transparent replacement of 3270 equipment, emulating 3271 cluster controllers and allowing AOS tasks and terminals to appear as 3271 and 3277 terminals to the host computer. It allows implementation of distributed applications processing and local standalone processing, and supports concurrent communications with the company's other IBM compatible communications software packages running in the same AOS based system.

Running as a separate process under AOS, the emulator concentrates data entered on AOS terminals and supervises its communication to/from local Eclipse system terminals. Data can be routed to the IBM /360, /370, or 303X mainframe or to another AOS program in the local Eclipse system. This results in faster response times and lower communications costs.

With the software, several AOS based systems can be added to a multidrop communications line serving 3270 equipment. The Eclipse system can share that line with 3271 controllers, or can be connected to several communications lines, permitting interactive 3270 emulation concurrent with remote job entry emulation such as HASP II or 2780/3780.

Up to 16 terminals connected locally or through dialup or leased lines are supported by AOS RCX70 at each Eclipse system. Additional terminals on an AOS system can be dynamically assigned to perform concurrent program development and other activities. AOS RCX70 supports IBM BSC protocol allowing local system to communicate with remote hosts using leased or switched synchronous lines at rates to 9600 bits/s; a DCU/200 control unit adds support for transmission rates to 56k bits/s.

Circle 176 on Inquiry Card

Mostek's MD Series.™ 16 new boards.

Since its introduction, Mostek's MD Series of Z80-based, 4.5"x 6.5" microcomputer boards has received overwhelming acceptance. Engineers have found both MDX functional modules and MD single-board computers offer maximum versatility at minimum cost. And our 16 new boards will open the door to even more microcomputer applications.

Mostek MD Series

MDX-CPU1	Z80 CPU with 2 PROM sockets and 4 timers
MDX-DRAM 8	8K Dynamic RAM
MDX-DRAM 16	16K Dynamic RAM
MDX-DRAM 32	32K Dynamic RAM
MDX-EPROM/UART	Combination EPROM/UART
MDX-DEBUG	EPROM/UART with 10K ROM-based software
MDX-PIO	32 bit programmable parallel I/O
MDX-SIO	2 channel programmable serial I/O
MDX-SST*	Hardware single step
MDX-FLP*	Floppy disk controller
MDX-MATH*	High speed floating point math
MDX-A/D 8*	8 Bit A/D
MDX-D/A 8*	8 Bit D/A
MDX-A/D 10*	10 Bit A/D Converter
MDX-A/D 12*	12 Bit A/D Converter
MDX-D/A 12*	12 Bit D/A Converter
MDX-UMC*	Universal Memory Card
MDX-SRAM 4*	4K Static RAM
MDX-SRAM 8*	8K Static RAM
MDX-SRAM 16*	16K Static RAM
MDX-EPROM-4*	EPROM Module
MDX-CPU2*	New Z80 CPU Board
MDX-SC/D*	System Controller and Diagnostic Board
MDX-INT*	Interrupt Expander and Timer Board
MD-SBC1	Z80, 8K PROM, 2K RAM, 40 I/O lines
MD DOS*	Dual Floppy Disk Operating System Software
MITE-80*	Multiple Independent Tasking Executive Software

* New

See us at WESCON booth #1500 and #1501

STD-Z80 BUS Flexibility

All our MDX cards are STD-Z80 BUS compatible. Just match the proper MDX modules to your design. Choose either 2.5MHz or 4MHz versions. Modify your system at any time by simply adding, exchanging or deleting MDX cards.

This allows you to buy only what you need, reduce hardware development time, and quickly respond to changing product definition and market conditions.

And with more and more manufacturers multi-sourcing the STD-Z80 BUS, you're assured of a long-lived industry standard.

Mostek's MD Series has the extensive support of our powerful Matrix Development System,™ plus a wide range of software and accessories for quickly developing and prototyping your system.

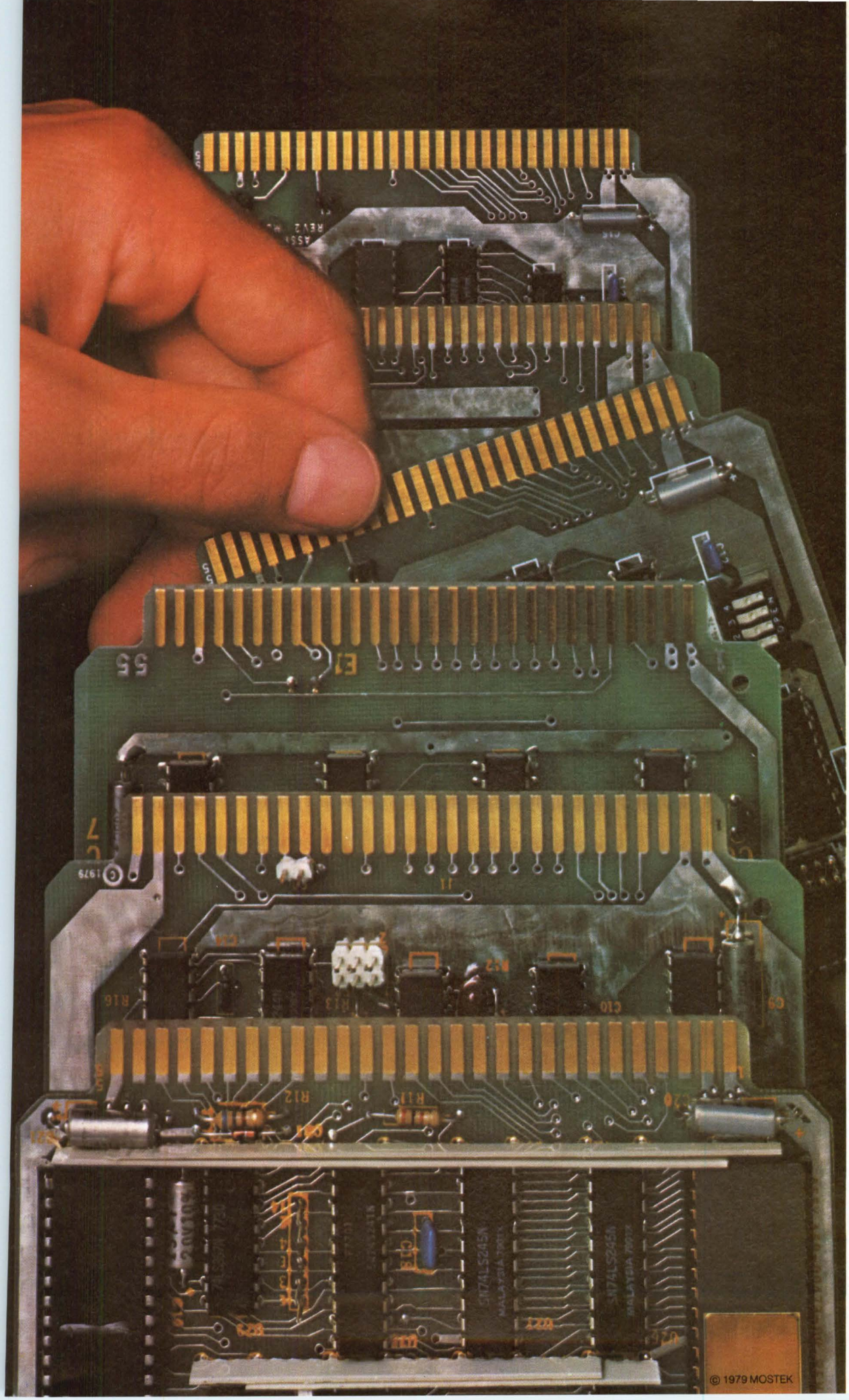
Distributor Availability

The best way to evaluate the MD Series is to call your local Mostek distributor and ask about the MDX-PROTO kit. This powerful evaluation kit is available now for only $1095.

For the complete MD Series update, see your local Mostek distributor. Or call or write Mostek, 1215 West Crosby Road, Carrollton, Texas 75006; phone (214) 242-0444. In Europe, contact Mostek Brussels, phone 660.69.24.

MOSTEK.

CIRCLE 35 ON INQUIRY CARD



MDX-UMC

MDX-MATH

MDX-EPROM-4

MDX-SST

MDX-A/D 8

MDX-FLP

Virtual Storage Processor Supports Word/Data Functions

Virtual storage processor vs 100, providing top end throughput in the IBM 370/158 and 3032 range at an entry level price below that of IBM's 4331, supports both word and data processing functions. Introduced by Wang Laboratories, Inc, One Industrial Ave, Lowell, MA 01851, the processor features 32-bit hardware architecture, 64-bit high speed system bus, and 32k cache memory.

Bus adapters on the processor facilitate additional input/output processors by acting as a buffer between up to eight I/O processors and the CPU and main memory. This approach improves the rate of data transfer between devices, increasing system throughput and performance.

Expandable from 256k-bytes up to 2M-bytes capacity, main memory is augmented by a 32k-byte cache that provides high speed access to the CPU, allowing it to run at maximum speed. A CPU lookahead feature can initiate prefetching of data from main memory before required by the CPU.

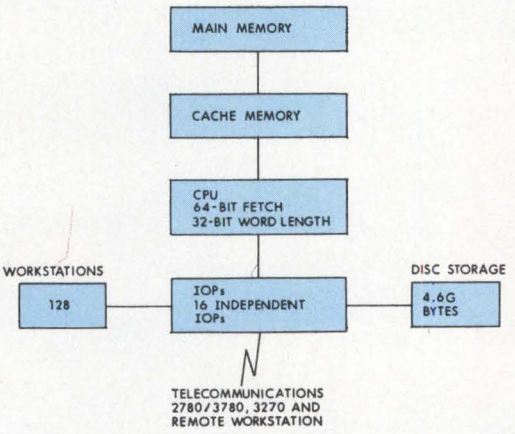
Online storage capacity is 4.6G bytes, double that previously available. Space compression on disc can increase this capacity by one-third. Up to 128 workstations plus 128 peripherals can be attached to a processor with virtually no response time degradation. Data communications software and protocols including 2780, 3780, and 3270 are supported.

All virtual storage files, source and object code, and peripherals are compatible. The system also supports FORTRAN and PL/1 languages, as well as an advanced data management system, an extension of the existing DMS support, that provides logical data retrieval, error checking, and backup recovery facilities. The database management system features a data modeling technique that combines the performance of a network system with the simplicity of a relational model.

Complementing the system's data processing functions is complete interactive functionality at remote locations. This supports both batch and interactive telecommunications connections to a mainframe as well as providing support for standalone and clustered remote workstations.

An integrated information terminal, the 2246C supports both word and data processing functions, enabling the operator to switch back and forth between the two. This terminal merges the functions associated with a data processing terminal with those of a word processing terminal, allowing a single system to satisfy all of an organization's processing needs.

Circle 177 on Inquiry Card



Combining virtual memory techniques, 32-bit architecture, independent I/O processors to offload CPU, and cache memory for enhanced throughput with support for 128 interactive terminals, Wang's VS 100 provides throughput equal to that of IBM's 4331 at approximately 60% of the price

Medium Range Systems Offer Performance At Moderate Cost

Filling the moderate cost/performance slot in the CLASSIC family of computers from Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33309, 7830 and 7835 models are compatible with existing operating systems. The CPUs execute most register to register instructions in as little as 300 ns and have memory management capability that provides addressability to 512k bytes. System architecture meets real-time environment requirements, providing processing capacity addressed to measurement and control, communications, and scientific and information processing applications.

Architecture of the 7830 features a context register file containing 16 banks of general purpose registers, with each bank consisting of 15 registers. This enables context switching among several tasks without having to save and restore register content. Four address mapping files, expanded instruction set, direct memory processor I/O channels, and fast interrupt response time also enable system overhead to be kept minimal.

An 8-slot card file houses the single-board CPU/I/O processor module and single-board 128k-byte, 2-way interleaved MOS memory circuit card. An I/O connector panel is used for peripheral interface, to accommodate remote file interface, and to extend the local I/O bus.

Virtual memory addressing gives the ability to address memory systems larger than 128k bytes, handle multiple dynamic tasks, address fragmented memory contiguously, and handle dynamic memory allocation. The 1024 registers in the map files enable most high priority programs to remain concurrently mapped, and provide these advantages: address translation within nanoseconds, 512-byte page sizes, noncontiguous page allocation, and fast task switching.

Error correcting MOS memory module arrays consist of two 64k-byte modules combined on a single wire-wrapped PC board. 2-way interleav-

SYNERTEK PERFORMS

16K ROMs. 3 weeks. 32K ROMs. 4 weeks.

When it comes to service, product availability and fast prototype turnaround, we can't be beat. And that means 16K ROM prototypes in three weeks, 32K ROM prototypes in four weeks. Volume production in five to six weeks. Even quicker if it's absolutely needed.

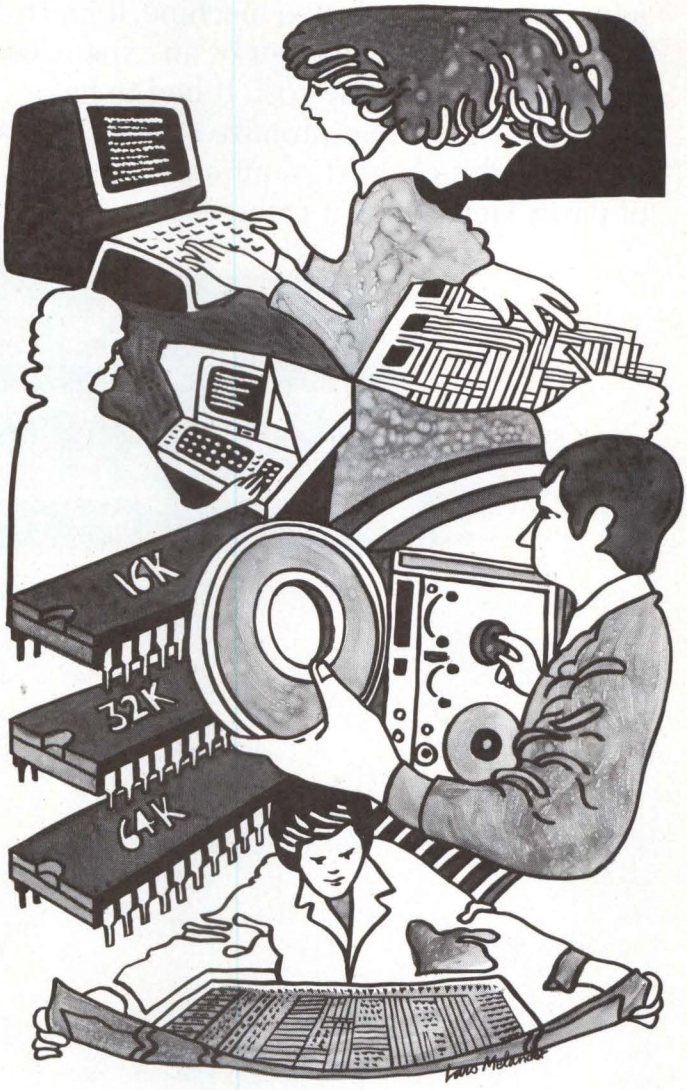
We know there is no product area where responsiveness to your needs is more important than in mask programmable ROMs. So we pioneered a unique dual capability—first mask programming for lowest cost in high volume production, and last mask programming for fastest delivery to meet critical production schedules in as little as two weeks.

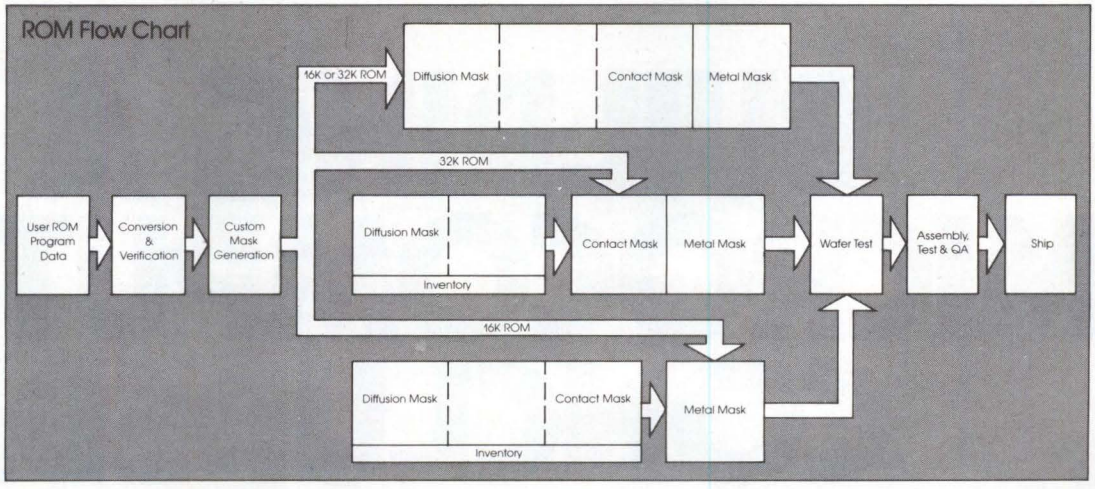
Take a look at the ROM Flow Chart and you'll see how we do it. With our "varied stage inventory" we can put your ROM codes into our production cycle at three different stages: diffusion mask, contact mask or metal mask. The choice is yours. Because the needs are yours.

Our SY2316B, SY2316A, SY4600, SY2332 and SY2333 ROMs come in the standard speeds you need—300nsec and 450nsec. And soon you can add our 64K ROM to the list. Pin compatibility in our 2048x8, 4096x8 and 8192x8 ROMs gives you built-in memory expansion capability. And you can usually do it with no hardware changes.

When you buy ROMs from Synertek, you're buying total service. For samples, data sheets and our comprehensive folder "Synertek ROMs ASAP," contact your local Synertek distributor, sales representative or Memory Product Marketing, Synertek, Inc., 3001 Stender Way, Santa Clara, California 95051. (408) 988-5611. TWX: 910-338-0135.

Synertek sales offices: **Eastern Region,** Boston (617) 329-5522; **Mid America Region,** Chicago (312) 986-8989; **Western and Northwest Regions,** Santa Clara (408) 255-3941; **Southwest Region,** Los Angeles (714) 752-5535; **Europe,** London, Direct Dial: 44-344-24555.





SYNERTEK, INC. 3001 Stender Way, Santa Clara, California 95051 (408) 988-5600. TWX: 910-338-0135.

CIRCLE 36 ON INQUIRY CARD

For the past several months, Advanced Micro Devices has been publishing an advanced course in microprogrammable microprocessing. This discussion ends the series.

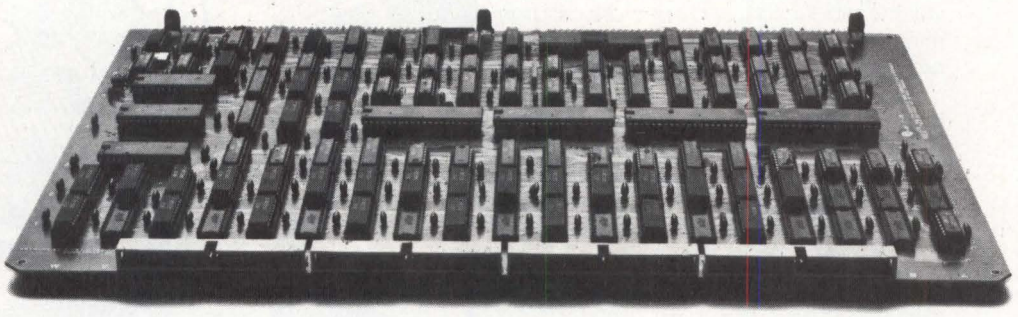
Our goal was to show you how to build a fast, microprogrammed machine. It had to have the processing power of an expensive computer without the cost. It had to have a design you could customize to your own needs. And it couldn't require a room full of parts. Here's how it came out:

CHAPTER 8: THE BASIC 16-BIT MICROPROGRAMMED MACHINE.

It's your basic miracle.

This machine has a register-to-register cycle time of 320ns. It has an absolutely straight-forward architecture. It's easy to modify and easy to understand. And it comes with the complete microcode for 90, count 'em, 90 instructions.

Look a little closer and you'll see that we've done 90% of the design work for you.



The HEX-29. A commercially available computer based on the design in Chapter 8.

BUILDING A MICROCOMPUTER, CONCLUDED.

After you figure the time and money you'll save, you still have to get used to the idea of skipping all that dirty work.

THE DELUXE MACHINE.

Some people can't leave well enough alone, and you may be one of them. For you, Chapter 9.

It describes a 16-bit microcomputer with unheard of power and performance. This machine has an advanced architecture with overlapped instruction fetch, a unique high-speed synchronous bus, and a register-to-register execution time of 200ns.

Basic or deluxe, send for the information. With the running start it will give you, you'll be well on your way to building your very own microprogrammed machine. And that, after all, is what this series has been all about.

BUILDING YOUR LIBRARY, CONCLUDED.

With Chapters Eight and Nine on the Basic and Deluxe microcomputers, you can have yourself a ton of theory and applications information. If you're not already on our mailing list, send in the coupon and we'll send you the whole book.

Advanced Micro Devices
901 Thompson Place
Sunnyvale, California 94086

I want to build a microcomputer this year. Sign me up.

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Title_____
Mail Stop_____
Company_____
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City_____
State_____ Zip_____

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Advanced Micro Devices

901 Thompson Place, Sunnyvale, CA 94086. Telephone: (408) 732-2400

ing is standard; 4-way interleaving may be configured with additional memory options.

The processor uses three of the logical memory access paths to provide concurrent CPU and I/O access capability with associated high throughput I/O operations without interrupting CPU process execution. One path is used by CPU, one for the internal I/O processor, and the third for the memory bus control option. Each path communicates with memory through the time multiplexed memory access bus. Memory access overhead is reduced by allowing the I/O processor to execute previously called instructions or conduct DMI transfers while the CPU timeshares another memory location. In single-word mode the resident I/O processor provides throughput of 600k bytes/s (output) or 800k bytes/s (input). Double-word mode supports 1M byte/s output and 1.2M byte/s input.

Extended I/O processing capabilities are available with optional single-bus I/O processor dual-bus I/O processor. Each is mounted on an individual plug-in circuit board, is functionally similar, and interfaces with either one or two I/O buses, respectively. Demands for up to 4M-bytes/s I/O throughput can be met when the dual-bus I/O processor is installed.

The basic I/O structure consists of party line bus capable of transferring words or characters between any of 63 peripheral device controllers and any of 15 general registers. The bus is suited both for realtime applications and asynchronous and moderate speed peripherals.

Software available for the systems includes MAX IV realtime multiprogramming operating system, which supports FORTRAN, COBOL, and TOTAL. The MAXNET network operating system is intended for distributed network configurations; and MAX III operating system for realtime capabilities.

Circle 178 on Inquiry Card

64-Bit Array Processor Performs Iterative Math With 16-Digit Precision

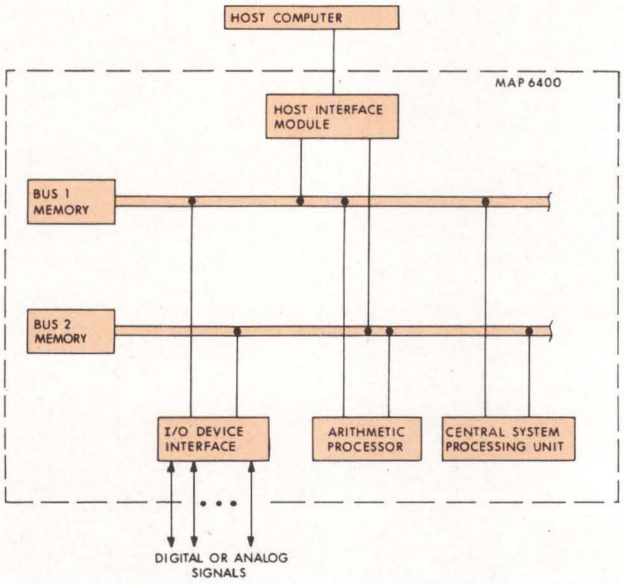
Capable of performing iterative mathematical functions with the accuracy of mainframes, when interfaced to a minicomputer, the MAP-6400, a 64-bit array processor, brings interactive computing within economic reach of scientific and engineering laboratories. Among the features of the processor, developed by CSP, Inc, 209 Middlesex Tpk, Burlington, MA 01803, are asynchronous processor and memory architecture and an internal controller that relieves the host of routine monitoring and control tasks during periods of heavy array processor computation.

Interfaced to a 16- or 32-bit minicomputer, the unit performs all hexadecimal arithmetic operations in full 64-bit floating point format, providing over 16 decimal digits of precision. All internal data storage and arithmetic operations are in IBM 64-bit format. The 56-bit mantissa maintains 16 full decimal digits of precision throughout a computation.

Multiple high speed arithmetic units carry out proper unbiased rounding after every operation without sacrificing any arithmetic throughput capacity. The 64-bit format permits routines such as matrix inverse and eigenvalue calculations, unstable on conventional single-precision array processors, to be accomplished at higher speeds than on the host's single-precision counterparts.

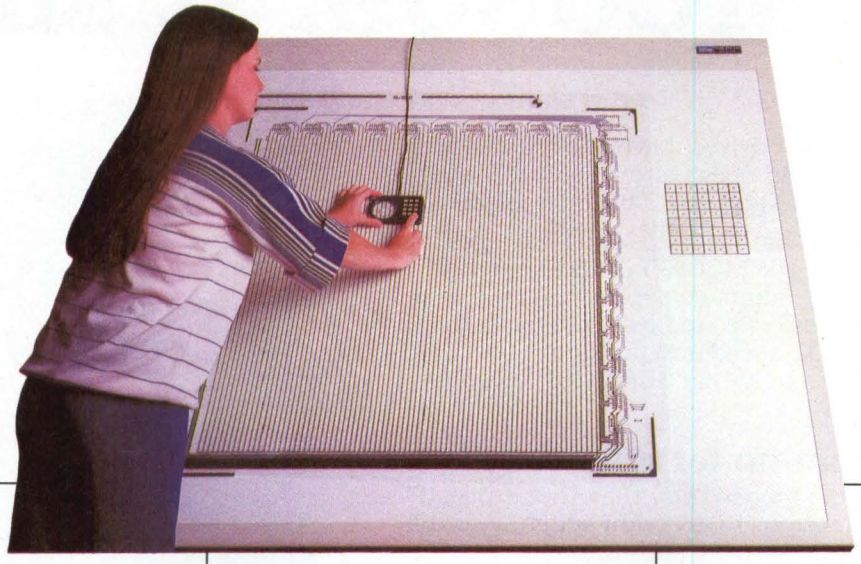
The basic unit consists of an arithmetic unit, internal controller, multiple memory systems, and interface boards. The array processor uses parallel hardware to overlap the data fetch and store operations with instruction decoding and execution. Parallel operation of arithmetic circuits achieves concurrent floating point multiply and add operation. Computational speed on arithmetic algorithms is 1.0 s for a 100 x 100 real matrix to matrix multiply and 22 ms for a 1024-point complex FFT. When compared with execution times for similar 64-bit calculation on minicomputers, these times range from 10 to 100 times faster.

Hardware features of the array processor include standard hardware and software interfaces to a range of host computers, program memory configurations expandable from 16k words to a maximum of 56k words

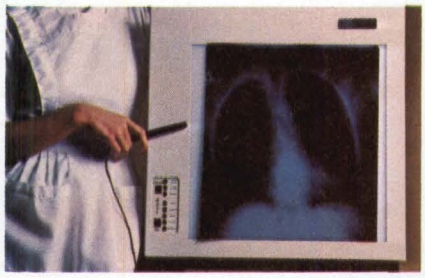


CSP's MAP-6400, 64-bit array processor, uses asynchronous processor and memory architecture and internal controller to perform 64-bit floating point operations with accuracy of mainframe computer and at speeds 10 to 1000 times greater than those of minicomputers

Tālos...the best buy in Digitizers.



Extensive Selection.

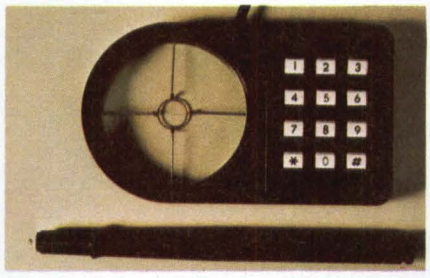


We know that digitizers are used for many projects (from tracking icebergs to mapping to radiology to CAD/CAM). That's precisely why we've developed the most extensive line of digitizers available. Active surface areas range from 11″ x 11″ to 44″ x 60″ and are offered with capabilities for Backlighting & Rear Projection in addition to our rugged solid surface.

We've Got Smarts...

Our "SMART" option is actually a microprocessor in a digitizer. Some of the functions selectable from the movable menu include distance, area, and volume calculations, coordinate translation, independent X, Y, scaling, and origin relocation as off-line functions, saving valuable computer time.

Quality Construction.



Our pens and cursors are built with sturdy aluminum for durability. The digitizing surface is solid and not susceptable to magnetic fields, temperature, humidity, noise, or age.

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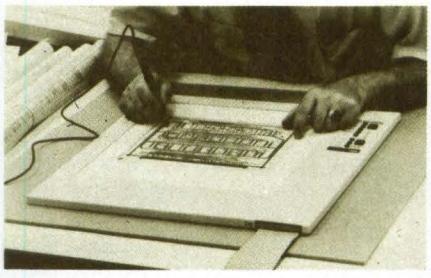
Dependable Performance.



We design, build and inspect each Talos digitizer to the highest quality standards in the industry. Before any digitizer meets our approval it has been run under operating conditions for at least 96 hours while over 50 control functions are tested. Our highly trained staff checks and re-checks resolution and accuracy. 1000 lines per inch is standard at Talos – and remember the higher the resolution the greater the potential for accuracy.

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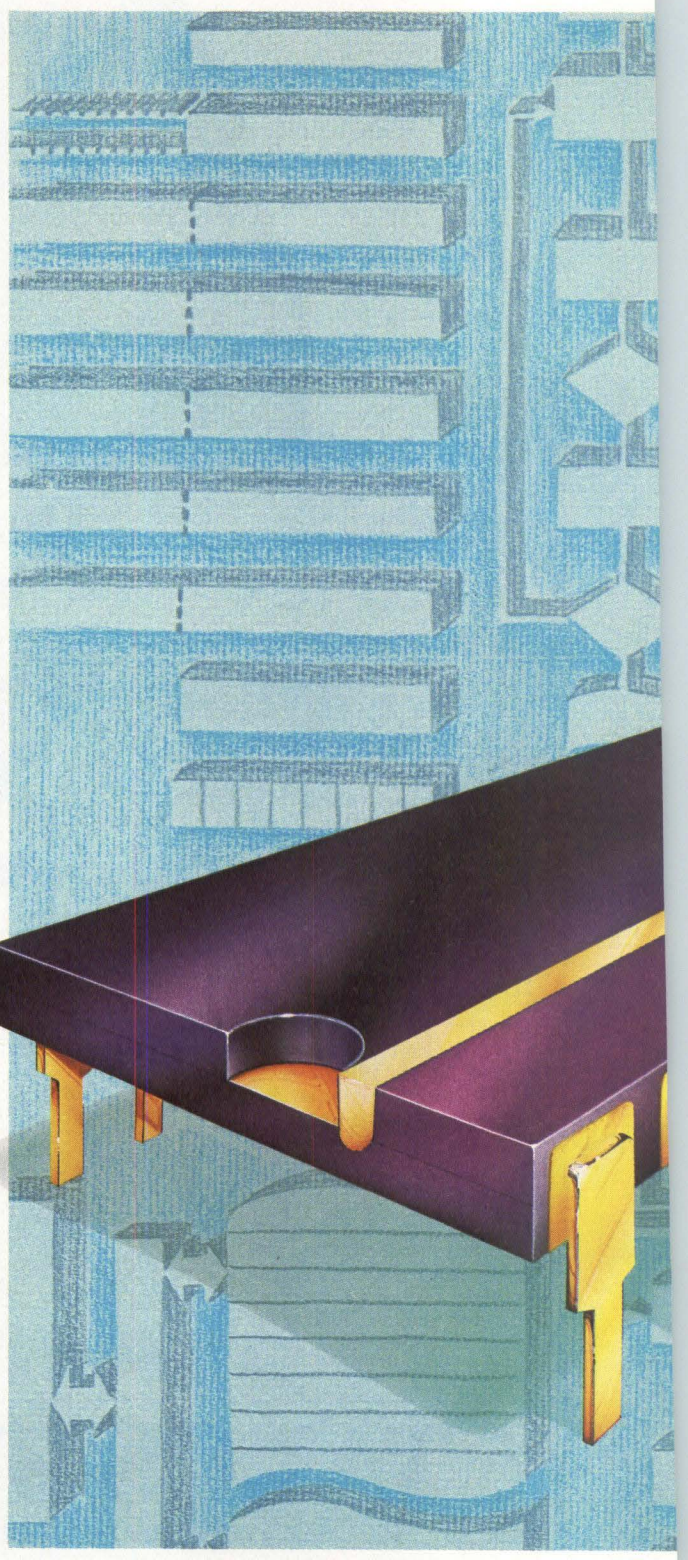
CIRCLE 37 ON INQUIRY CARD

The most powerful 8-bit MC6809. It shrinks



Motorola's MC6809 drives down the high cost of software generation and does more for future systems than any other general-purpose 8-bit microprocessor.

While designed to handle high-level languages like PASCAL and BASIC, the MC6809 is also superbly efficient in assembly language applications. Efficiency means less code, and less code means lower costs. MC6809 speed and power are unbeatable, too. Not only that, the MC6809 is available right now.

Features team-up for efficiency.

More addressing modes than the other 8-bit MPUs, an optimized consistent instruction set enhanced by powerful 16-bit instructions, and uniquely versatile data manipulation on stacks work synergistically for increased software efficiency.

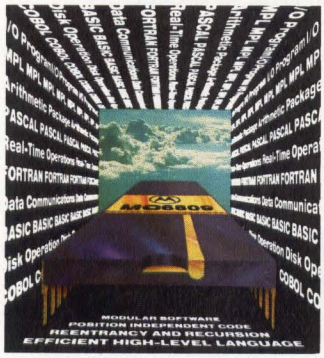
These features, plus 24 indexing submodes, promote the use of modern programming techniques like position independent code, re-entrancy and recursion. Auto-increment and auto-decrement indexing permit efficient block and string moves. Stack pointer indexing accommodates structured programming.

With these features you can develop a library of modular routines, even in ROM, for a variety of systems and at any convenient memory location.

Full M6800 family compatibility.

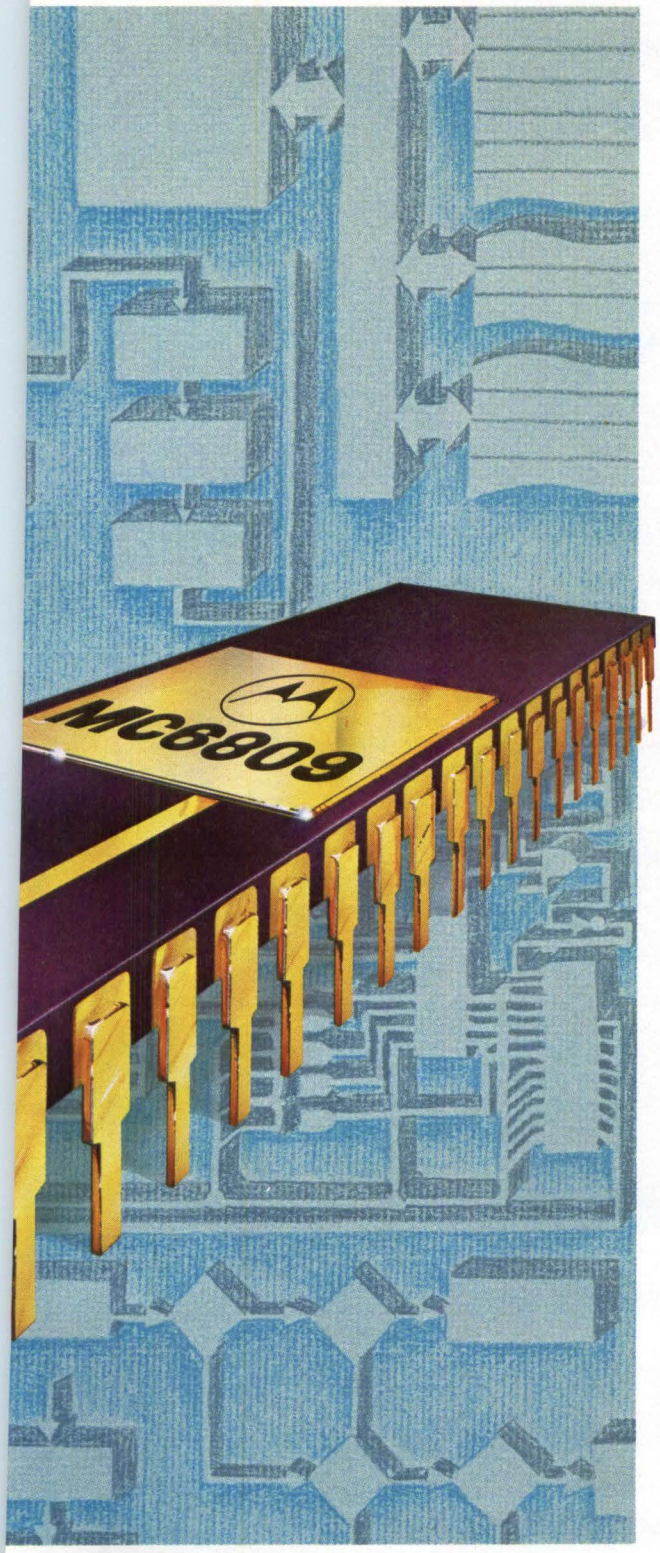
Full M6800 family compatibility is useful for the MC6809 in a variety of ways. For example, the widely benchmarked MC6800, recognized and respected for its performance, efficiency and ease of use, provides an ideal reference for comparison. Keeping its high performance in mind, see just how sensational the MC6809 is.

The MC6809 is significantly faster than the latest '6800. It takes only about one-third the time to run a comparable program with the MC6809 than it does with the 2-MHz '6800 version, and about one-fifth the time of the original MC6800.



Typically, less than two-thirds the program memory of the MC6800 is required with the MC6809, so byte efficiency is superior. Equivalent MC6809 programs use less than 60% of the instructions needed for the MC6800, cutting programming costs nearly in half.

general-purpose MPU. software costs.



M6800 family compatibility also means +5 V single-supply operation, and permits total usage of all the family I/O, peripheral control, communications and memory components.

Hardware designers can take advantage of the on-chip system clock generator, fast interrupt, interrupt acknowledge, memory ready, DMA request and the signals for multiprocessor synchronization. System designs generally require less external parts with the MC6809 than with other 8-bit or 16-bit microprocessors.

Although the memory address capability is actually greater than needed for many applications, a memory management unit is planned to meet the demand of new systems and future growth.

Hardware and software support.

Family compatibility pays off again, as Motorola's EXORciser® and EXORterm™ development systems support the MC6809 microprocessor. Both development systems are now available equipped with either the MC6809 or the MC6800 CPU module.

Support Available Now for MC6809

- 6809-based EXORciser and EXORterm
- 6809 User System Evaluation (USE)
- 6809 Upgrade for 6800-based EXORciser
- Macro Assembler/6800 Translator/Editor
- Disk Operating System (MDOS)
- PASCAL Interpreter

Coming Soon

- MPL Compiler
- PASCAL Compiler
- FORTRAN Compiler
- BASIC Interpreter

For additional information, contact your Motorola sales office or authorized distributor, or write to Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, AZ 85036.

The MC6809, good as it is, is only a part of the story on our full line of microprocessors, single-chip microcomputers, memories, peripherals and support from Motorola for designers creating

Innovative systems through silicon.

MOTOROLA INC.

CIRCLE 38 ON INQUIRY CARD

in 8k increments, and multiported 64-bit data memory in 32k- and 64k-word configurations expandable beyond 64k using standard bulk memory interfaces. Direct access disc storage peripherals, analog input and output peripherals that allow direct connection of analog signals, and programmable digital I/O devices that support custom interfaces accommodate changing application requirements.

By retaining compatibility with existing software written for 32-bit MAP-200 and -300 series processors the processor is able to benefit from software written in custom assembly code and a FORTRAN subroutine library. Optimized library routines that exploit the processor's computational capacity can be taken advantage of through the library of host support FORTRAN routines.

Within the processor all sequencing and control of tasks are carried out by an internal monitor, the executive. This realtime monitor operates in conjunction with the host operating system to maintain integrity of data areas internal to the MAP as well as those shared with the host CPU in host main memory. It is also responsible for multiprocessor task synchronization including data transfer between MAP and host.

Programming, operation, and maintenance of the unit are simplified by standard utilities that include assembler, simulator, and debug routines for program development; loader for system bootstrap and Executive modifications; and host loadable diagnostics for fault location determination.

User communication with the array processor occurs through the SNAP-II host support library. This set of disc resident FORTRAN routines is searched by the host operating system after compilation. Then as subroutine calls in the library are encountered in the application program, the equivalent SNAP-II host support routines are substituted. These routines serve simply to pass sets of parameters to the MAP via a host resident driver program.

The system executive can handle more than just single calls from the host. Totally independent parallel processing can be achieved by definition of function lists—string of array function calls that are constructed as a group in the host program. These lists may be executed repetitively. Control calls may also be imbedded in function lists to provide nested function list capability.

Base price of the unit is $89,000 configured with 16k program memory and 32k x 64-bits data memory. Production units will be available in January 1980.

Circle 179 on Inquiry Card

Memory System Permits Static and Dynamic RAMs To Be Combined

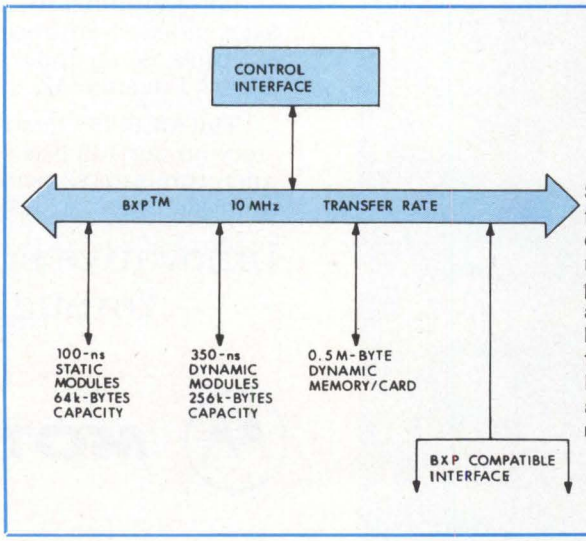
Series 90 memory system meets users' flexibility and expansion requirements by combining both static and dynamic RAM technologies in a single system. The family of general purpose memory products, from Intel Corp, Commercial Systems Div, 3065 Bowers Ave, Santa Clara, CA 95051, based on the BXP™ bus, consists of control interface modules and static and dynamic memory modules.

Designed specifically for memory systems, the BXP bus contains 24 address lines, 4 module address lines, and a bus select function providing substantial expansion potential. Bus wiring, signal level, and timing specifications provide a standard that permits interconnection of different memory types that share a common connection to the user's equipment. The bus accommodates word sizes ranging from 22 to 88 bits without ECC or from 16 to 80 bits with ECC.

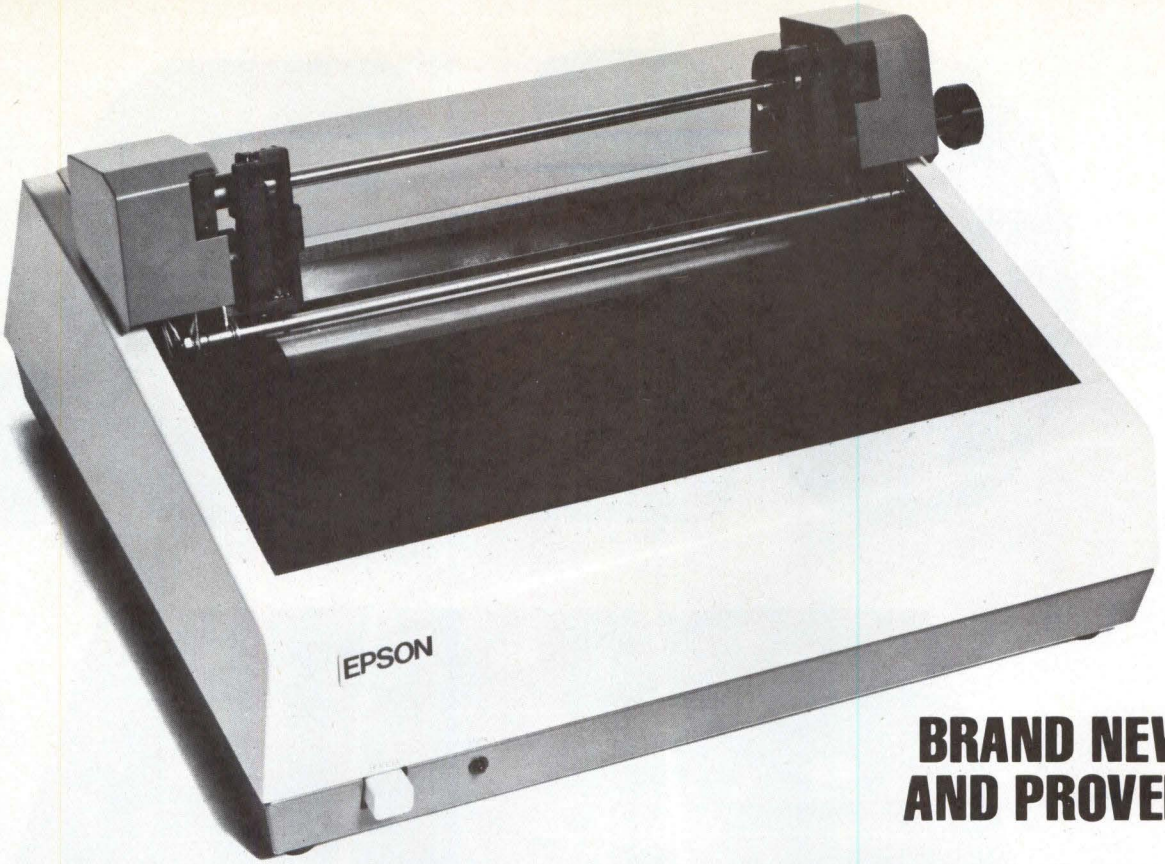
Maximum word transfer rate of the system is 10 MHz, providing maximum transfer rates of 80M bytes/s with byte addressing and ECC, or 110M bytes/s without. This maximum transfer rate can be achieved either with static memories operating in random access mode or with dynamic memories operating in an interleaved mode. Static memory modules (CM-92) built from 4k RAMs have cycle times as fast as 100 ns; dynamic memories (CM-90) are built using 16k RAMs and operate at cycle times as fast as 350 ns.

Users can interface the system directly to the BXP bus, to a custom control interface, or to standard control interface modules. The memory system operates in either synchronous mode or in one of several asynchronous protocols. Pipelining protocol enables memory to execute one cycle while storing a second for subsequent execution, permitting static and dynamic operations to be mixed over long cables without performance degradation.

A primary function of the control interface is to provide single-bit error correction and double-bit error detection. Single- and double-bit error flags are transmitted in the event of



Series 90 memory system from Intel operates in synchronous or asynchronous mode and uses pipeline protocol to permit static and dynamic operations to be mixed. Maximum transfer rate of 80M bytes/s can be attained with both static and dynamic memory modules



BRAND NEW AND PROVEN

TX-80 DOT MATRIX PRINTER FOR OEM

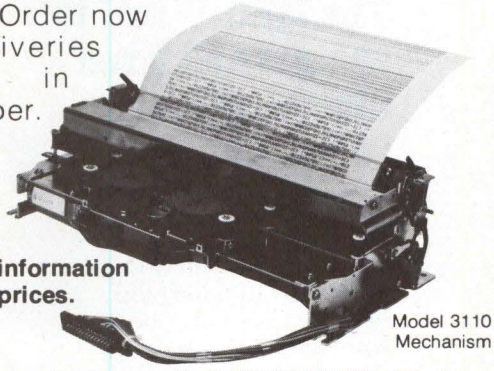
All the advantages of the proven Epson 80-column Model 3110 Dot Matrix Printer Mechanism are now available in our new complete, ready-to-go TX-80 Dot Matrix Printer.

The TX-80, complete with electronics and case, features tractor feed, a 100,000,000 character dot head, and 150 characters per second printing using 96 ASCII characters.

It comes with a connector compatible with either a Centronics plug or an EIA standard 25-pin connector.

Sold to OEM, the TX-80 fills the needs of large and small suppliers who want to avoid the costs of custom packaging and electronics. Order now for deliveries starting in September.

Write for complete information and OEM prices.



Model 3110 Mechanism

EPSON products are manufactured by SHINSHU SEIKI CO., LTD., Japan

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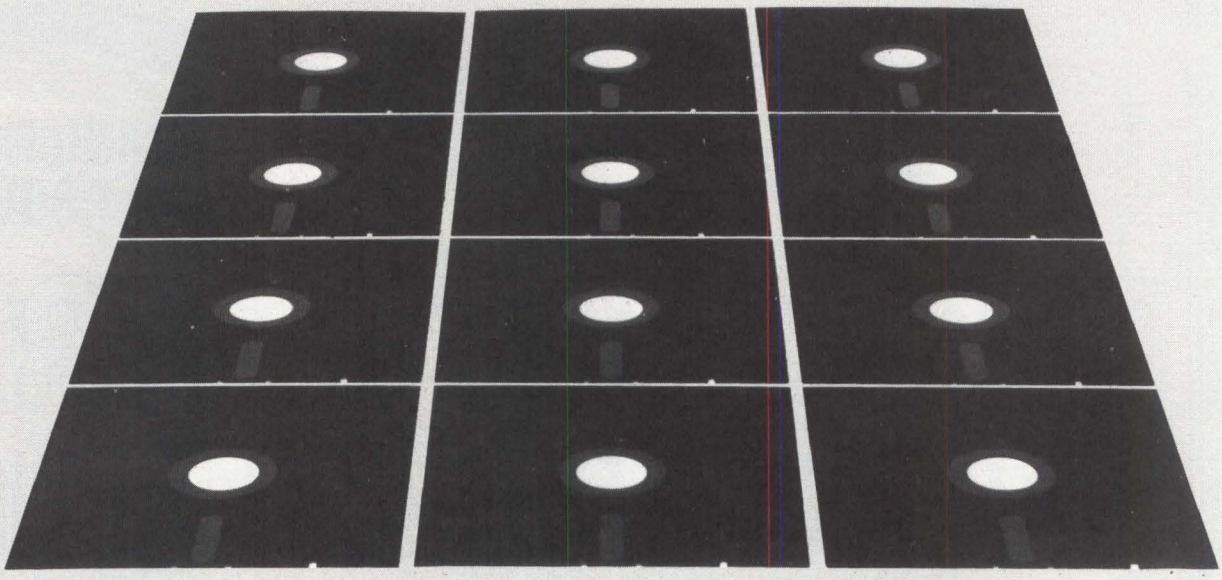
CIRCLE 39 ON INQUIRY CARD

O.L.D.



The Mini-Wini™ is the new 8" fixed disk that stores 20 megabytes.

That's right, 20 (count them) megabytes. The same 20 megabytes you'd have to string more than 12 floppy disks together to get. We thought it was about time somebody offered the reliability and efficiency of a fixed disk in a smaller size, at a smaller price. So here it is. We call it the Mini-Wini. Otherwise known as our D8000 fixed disk.

Mini-Wini is a trademark of Pertec Computer Corporation.

The Mini-Wini fits in the same size slot as an 8" floppy disk drive.

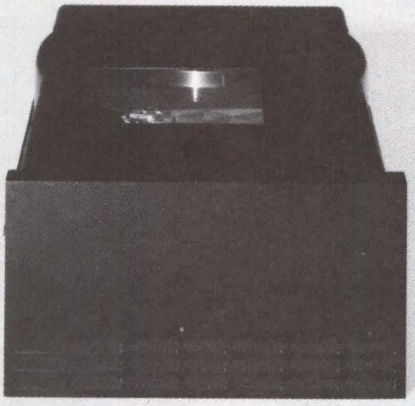
When we say the same size, we mean the same size. That means you can upgrade your storage capacity easily. All you have to do is buy the Mini-Wini. Of course, some controller redesign will be required.

The Mini-Wini saves you money.

It's the lowest-cost way to get 20 megabytes in an 8" floppy slot. With it, you can expand the on-line capacity and value of your present desk-top system without having to redesign the chassis you now have.

The point is, the Mini-Wini allows you to put out a better product without spending a lot of money. It also allows your customers to save money. Why hassle with stacks of floppies or large old-fashioned disk drives, when one small fixed disk will do?

NEW.



The Mini-Wini™ offers ease of interface.

Small wonder. It has a microprocessor controlled interface, featuring a bidirectional command/status bus and serial data transfer. It's easier and simpler to design the CPU interface.

The Mini-Wini uses Winchester technology.

When you've got it, you've got it. And the Mini-Wini does. The heads and the media are sealed in a safe environment that protects against contaminants.

The Mini-Wini has another big advantage.

It's made by Pertec Computer Corporation. Which is reassuring. We not only have the capabilities to produce innovative new products, we also have the production capacity to supply them when we say we will. So if you want the Mini-Wini, check with us.

PCC PERIPHERALS
PERTEC COMPUTER CORPORATION

They won't let you down.

For further information, call toll-free 800-528-6050, Ext. 1323.
(In Arizona call 800-352-0458.)

errors to notify the user of memory status. ECC functions also support an optional error logger and display assembly. Hexadecimal display provides direct readout of physical location of a failing memory device.

Completely integrated packaged Series 90 memory systems are available in a 19″ (48 cm), 5.25″ (13.34-cm) high unit with self-contained power supplies and side to side air flow, or in a vertical slot 10.5″ (26.7-cm) high unit without cooling. Accessories include an extender card for troubleshooting and a utility card that enables rapid design of BXP compatible control interfaces. Prices range from $9900 for 128k bytes of 100-ns static storage to $91,000 for 4M bytes of dynamic storage with ECC and error logger.

Circle 180 on Inquiry Card

Word Processing Systems And Software Extend Intelligent Terminal Line

Word processing systems and software as well as expanded capability for existing user programmable intelligent terminal systems, introduced by Ontel Corp, 250 Crossways Park Dr, Woodbury, NY 11797, are designed for OEM market. Among the software offerings are a multitasking operating system, SDLC communication controller, PASCAL language, and assembler and editor.

An extension of the OP-1 user programmable intelligent terminal system, the OP1/RW can be used as a word processing secondary station in a clustered word processing environment. With the same architecture of the OP-1, the unit is fully user programmable and may be attached as a remote secondary processor in a clustered system. Word processing programs may be executed at a remote location that requires no attached local storage device. In addition, the unit will execute all communications and data processing programs available for the company's systems.

Based on the OP1/64 programmable intelligent terminal system, the OP1/50 has a maximum of five logic boards. These include any available display microprocessor, 200-ns cycle time memory/CPU board that incorporates the 8085-2 CPU and 64k memory with parity checks, I/O microprocessor, and any two device controllers. Options include two double-sided, double-density mini-diskette drives.

Permitting the word processing program to run as a task while the unit concurrently executes other tasks, the MFTOS multitasking operating system runs under any language currently available from the company. Among the features offered are up to 255 tasks, code and data segments shareable by all tasks, round robin within priority dispatching, and up to 16 priority levels. The system also provides extensive intertask message facilities, a communications task supporting up to 16 secondary processors, ability to dynamically create and delete tasks, and the ability to wait on user defined events or resources.

Other available software includes an SDLC communications controller that operates at speeds to 9600 baud

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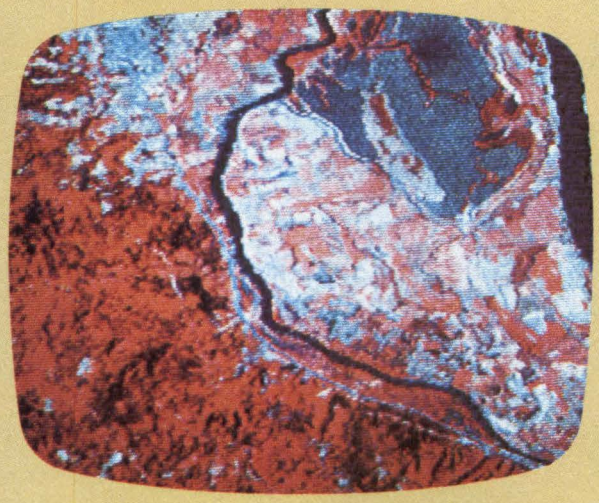

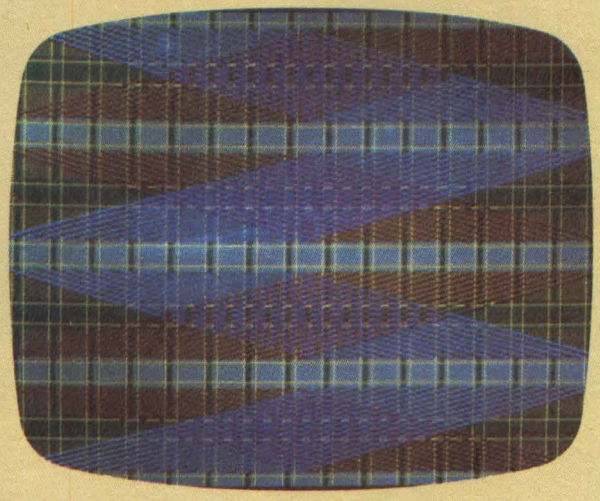

Now, with the Grinnell GMR-270 Image Processing System, you can have pipeline image processing tailored to fit your application.

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In addition, the GMR-270 has a display resolution of 512 x 512 pixels and a video format that is RS-170 compatible. It is housed in a rack-mountable chassis and drives standard TV monitors.

Besides the GMR-270, Grinnell manufactures two complete lines of graphic television display systems: the GMR-27 Series and the GMR-37 Series. GMR-27 units are high speed, graphic and image display systems; GMR-37 units are low cost graphic display systems. Both are available with display resolutions from 256 x 256 to 1024 x 1024.

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CIRCLE 42 ON INQUIRY CARD

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The minicomputer industry has been growing by 20% - 35% every year. And as the industry grows and develops, applications for minicomputers appear virtually limitless.

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Sperry Univac is one of the few companies in the world offering a complete range of data processing equipment from minis to mainframes.

Our goal at Mini-Computer Operations has been to provide our customers with dependable, up-to-the-minute equipment. Equipment that can be readily adapted to incorporate new capabilities and give end users control advantage by standardizing their DDP systems.

Our entire line of minis was designed to let you develop sophisticated distributed networks with Sperry Univac or IBM hosts. Or in both environments concurrently.

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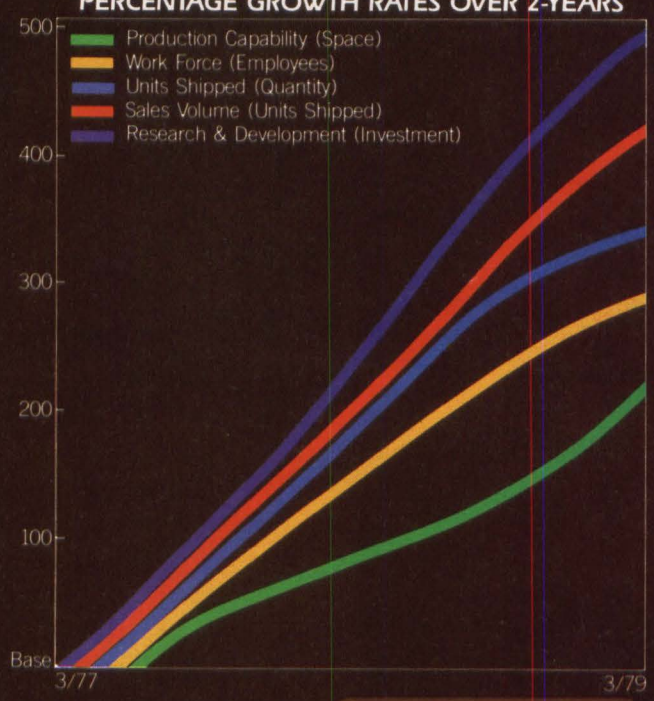
WE DO IT ALL.

We not only build the minis, we provide complete support with competitively priced peripherals and software. In fact, we offer QL-77, an easy-to-use query language and we were one of the first vendors to provide Pascal.



Sperry Univac was the company that developed SUMMIT, the operating system that allows you DDP capabilities with either IBM or Univac hosts.

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The Sperry Univac sales and service network is one of the largest and most responsive in the world. With over 8000 customer engineers available to keep our minis up and running, we can provide prompt, complete service worldwide.

And that service is the finest available. We've established a major computer education center in Princeton, New Jersey and several regional training schools throughout the United States and Europe. Our educational system insures the degree of excellence and competency in our service staff necessary to maintain our equipment at peak performance.

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At Sperry Univac we have a reputation for quality, performance and service in the computer industry.

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In Canada, write Headquarters, Mini-Computer Operations, 55 City Centre Drive, Mississauga, Ontario, L5B 1M4.

SPERRY UNIVAC

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CIRCLE 43 ON INQUIRY CARD

and a self-contained Pascal system that includes compiler, P-code execution unit, and operating system; two text editors; BASIC compiler, and utilities. To facilitate program development, the LINKASM assembler incorporates macro facilities, symbol cross-reference, and relocatable and linkable object code. LINKEDIT translates object code into executable binary load modules, relocates segments, and resolves interprogram references as required.

Circle 181 on Inquiry Card

Connectors Join Dot Matrix LCDs To PC Board Without Pins

A Zebra Step connector element used in conjunction with a self-supporting Zebra element connects dot matrix LCDs to printed circuit boards. The connector, developed by Technical Wire Products, Inc, 129 Dermody St, Cranford, NJ 07016, allows connections to be made between the back plane of the dot matrix LCD and the PC board without lead straightening, hole drilling, or soldering.

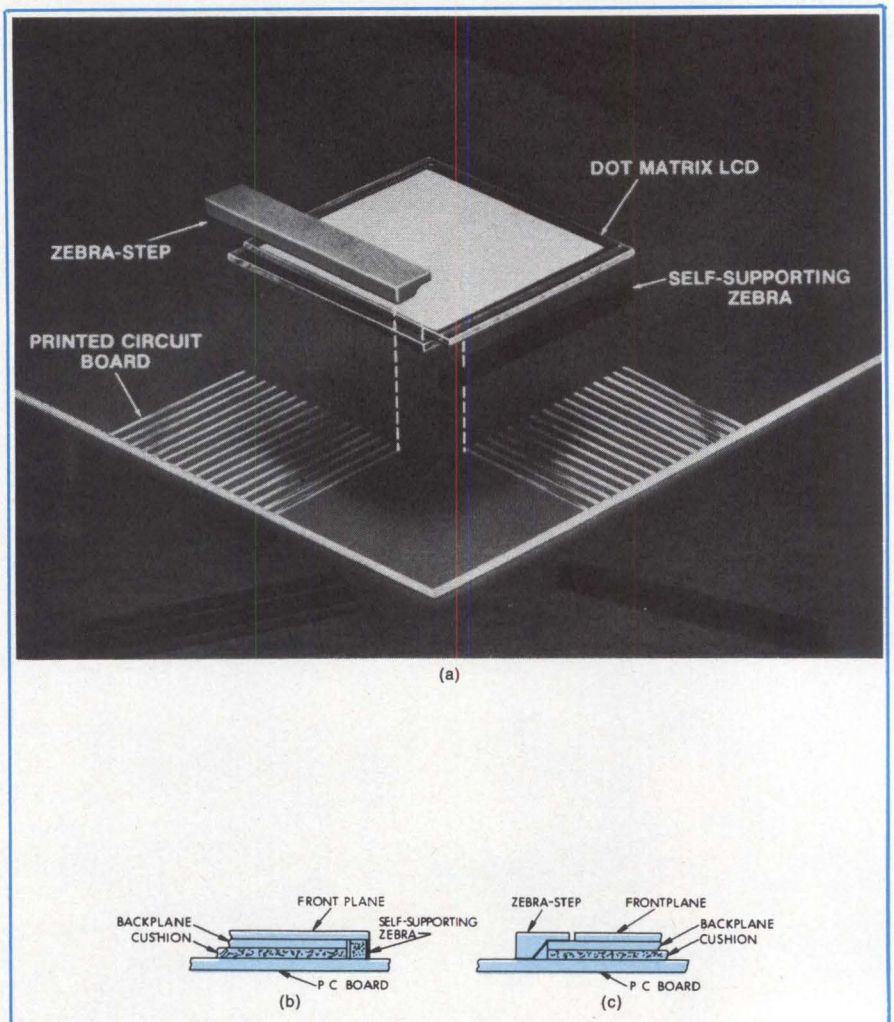
Typically, a dot matrix LCD is constructed similarly to a dual-inline LCD, with the front plane or glass overlapping the bottom plane or with overlapping front planes. Many have contact pads on the underside of the front plane and on top of the back plane. Connections to the front plane have traditionally been made by sandwiching a self-supporting Zebra connector between display and PC board. Connection between the back plane and PC board, however, has been made with metal pins, therefore requiring reflow soldering of any LCDs found faulty and replaced. Connections of this type can be made effectively using connector elements which require no metal pins, no aligning, no drilling, and no soldering.

A Zebra connector is made of alternating layers of conductive and nonconductive silicone rubber. A self-supporting Zebra is a silicone sponge laminated to one or both sides of a Zebra, eliminating the need for a holder. This type may have a colored insulating barrier added to its open side to prevent shorting. The Zebra Step consists of a series 1010 Zebra molded into a step configuration and backed with an insulating pad of silicone rubber. This element is positioned between the back plane of the LCD and the printed circuit board. Pressure applied by securing a bezel makes the connection.

The series 1010 Zebra used in the connector accommodates dot matrix LCD spacing of 0.050″ (1.27 mm) center to center. This spacing assures that there is at least one conductive layer between opposing contact pads and at least one insulating layer between adjacent pads. Current carrying capacity for 0.035 x 0.035″ (0.889 x 0.889-mm) contact pad is 0.050 A with resistance of 10^{12} Ω. Operating temperature range is from −65 to 500 °F (−53 to 260 °C) at 0 to 100% humidity.

Since the connector elements are made of silicone rubber, the glass LCD is protected from shock and vibration damage. A gas tight seal is created at the contact interface to maintain operation in a chemically corrosive atmosphere.

Circle 182 on Inquiry Card



Connection between dot matrix LCD and PC board can be made efficiently using Technical Wire Products' Zebra and Zebra Step connectors (a). Self-supporting Zebra makes contact with dot matrix LCD pads facing PC board (b), and Zebra Step makes contact with pads facing away from board (c)

High Level Language Has Control and Efficiency of Assembly Language

SL/300, a block structured high level language, offers programming control and efficiency normally found only in assembly language. Hewlett-Packard Co, 1507 Page Mill Rd, Palo Alto, CA 94304, designed the language for use by OEMs and programming specialists in tailoring distributed application systems to their HP 300 computer systems.

Through the language, application designers can directly and efficiently exploit the HP 300's architecture. Virtual memory, with respect to code and data, removes many normal barriers to the creation of large applications. Multitasking in a multiprogramming environment as well as communication and synchronization facilities among tasks and programs allow many dedicated operations to run under control simultaneously. The language's power is further extended by its file system, range of data types, and data base management facilities.

Programs translate into efficient code because the language and machine features fit one another. Thus the language can simultaneously offer advantages of high level programming for rapid program development plus the potential for performance optimization.

Among the capabilities are provision for implementing programs using structured programming concepts, dynamic array allocation for efficient use of runtime resources, high level statements with unlimited nesting, macro capability, both recursive and reentrant procedures, and flexible data manipulation expressions.

Circle 185 on Inquiry Card

High Performance Systems Extends Upper End of Minicomputer Family

Priced typically at $138,000, the META 4^R/5030 is a high performance minicomputer that offers reliability and convenience features usually associated with medium and large scale mainframe systems. An upward compatible member of the 5000 series computer systems from Digital Scientific Corp, 11425 Sorrento Valley Rd, San Diego, CA 92121, the system is based on a microprogrammed CPU capable of sustained instruction execution rates and throughput that rival those of 32-bit machines, and can handle more than 2M bytes of 200-ns semiconductor memory.

A design feature that contributes to the system's performance is a proprietary memory interfacing technique that nearly halves the time required for an I/O device to gain direct access to memory. Other features that are standard on the machine include memory protection, memory error detection, and sentry system monitor, which warns of variance in voltage or system cooling parameters through audio and visual alarms.

The system is driven by the DNA multiprogramming timesharing operating system (MTSO). This software supports concurrent timesharing, teleprocessing, and batch mode processing. Support is offered for COBOL, FORTRAN, BASIC, APL, and RPG II languages. Other operating system features include support for up to 32 interactive or batch partitions, I/O spooling, and complete set of user interface subroutines.

Circle 186 on Inquiry Card

Bubble Memory Tester Balances Engineering/ Production Requirements

To fully test magnetic bubble memory devices a test system must provide the accurate interface functions, flexible and efficient data generation and error processing, and extensive software analysis tools required by the devices. Fairchild Camera and Instruments Corp's Xincom Systems Div, 20450 Plummer St, Chatsworth, CA 91311 has met these challenges with its model 5585 magnetic memory test system.

Designed to test currently available bubble memory devices and future devices of up to 65M bits, the system can accommodate serial, major/minor loop, block replicate, and even/odd memory architectures. Strong diagnostics and device evaluation testing capabilities are balanced to serve both engineering and production test requirements. For production testing, the unit effectively provides parallel functional testing capabilities. The system is also an excellent diagnostic tool that offers capability to isolate and define design problems.

Key to the 5585 is a bubble memory pattern computer (BMPC), a high speed, custom designed computer constructed using ECL technology, that provides the speed and versatility required to generate complex, sophisticated test patterns on a variety of bubble memory architectures.

The BMPC features an instruction/execution rate of 6 MHz and can provide an uninterrupted 1-MHz data rate. It generates continuous, exhaustive test pattern streams, and can monitor and tabulate the results of multiple devices without any system attributable overhead. Overall system operation speed is up to 500 kHz.

The pattern computer has the ability to concurrently execute two independent programs in the instruction memory, providing the capability of concurrent read and write exercises. Two instruction memories hold up to 128 instructions, each 32 bits wide. An intelligent pattern processor, it can vary test parameters on the fly, perform arithmetic and logical operations, and a variety of other tasks. All device evaluations are completed without using tester overhead.

Test data patterns are defined in a 64-word by 16-bit data array in which data are specified as they would reside in memory. These patterns can be automatically replicated throughout the device.

Up to 30 independent current loop drivers are controlled by the BMPC. Each driver may provide up to 0.5 A of current with programmable resolution of 0.25 mA. Each driver edge is programmable to a resolution of 10 ns.

The system provides programmable drivers for driving inplane field coils and bias field coils for wafer sort and package testing. Signal detection is provided by remote, high accuracy signal discriminators.

A maximum of 16 independent loop error maps are maintained by the BMPC, each having capacity of up to 1024 loops. These loop error maps may be generated, read, or written from the device. Upon instruction selection, loop error maps may be used to mask data generation and subsequent data out response for determined faulty loops. Sixteen independent error counters (1 per output) record the number of errors detected per device. Up to 65,000 errors may be accumulated by each counter.

The test system controller may run concurrent with the BMPC program. At predetermined points in the test pattern, test condition parameters may be varied by the test system controller, without incurring discontinuities in test pattern generation.

The basic test system provides one test head with two device data I/O channels. To test four devices simultaneously, the tester may be expanded to two heads with four device I/O channels per head. The 5585 test satellite is a component of the Xincom III distributed system. The total system consists of a model 7710 host computer, with a medium speed printer, CRT, and a 5585 test head satellite with one or two test heads. Up to eight test satellites can be supported by the host computer. Test heads can be configured for up to 48 pins and will allow prober and handler interface.

Circle 183 on Inquiry Card

Nonimpact Printing System Produces Documents At Up To 18,000 Lines/Min

With an imbedded Level 6 Model 43 minicomputer, Page Processing System II produces quality finished documents at rates up to 18,000 lines/min. Designed by Honeywell's United States Information Systems Group, 200 Smith St, Waltham, MA 02154, the nonimpact printing system at-

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taches directly online to an IBM host computer in a distributed systems environment. Finished documents are cut, perforated, punched, collated, and addressed.

The printing system offers users the ability to custom design forms, characters, and logos and store them in the system. IBM host can be connected with the system via an optional channel interface unit that emulates a tape drive. This provides the advantages of an offline system without requiring magnetic tape units and those of an online system without adding CPU overhead. The unit prints documents in any size from 3.5 to 14″ (8.9 to 35.6-cm) long, prints forms and data at the same time, and intelligently stacks pages in five different ways in up to 32 pockets.

When operating online, the system uses the tape protocol method for data transmission. Data are transmitted directly from the host processor, where they are processed and stored on disc for output to the printer. Because the disc acts as a buffer and has overflow capabilities, data can be accepted from the host and concurrently passed to the printer, which can operate at a steady user selected speed without draining CPU cycles.

When printing offline the system reads 7- or 9-track magnetic tape from the original data processing system and transfers data to the printer. In the printer a high resolution line matrix of print stylii deposits electrostatic images of data on the paper's surface. Ink particles are attracted to charged images and then fixed to form permanent visible images.

The unit's software system is designed using structured programming techniques. To produce forms at the same time the job is printed, the user codes column headings and separators in software; the printer automatically stores, retrieves, and prints. Intricate designs requiring graphic arts resolution equivalent to 500 dots/in (196/cm) can be formed electrostatically using an easy to change metal format cylinder. Users can also design and store up to 16 different fonts of 128 characters each in the system for on- or offline use.

A multiline CRT display and keyboard allows direct communication with the system and permits the operator to monitor its operation, manage output execution sequence, and direct system operation. Priority scheduling lets the user interrupt a running job and restart it at the same point. Search and catalog commands permit stored jobs to be cataloged from the console and certain reports within them to be isolated and printed.

In a basic configuration with 8000-line/min printer, CRT, CPU with 64k memory, 12.5-char/in font, and 96M-byte disc, the system sells for $135,000. Channel interface unit is priced at $12,000, and 8-pocket stacker at $18,500. 12,000- and 18,000-line/min options are $21,400 and $47,600, respectively. □

Circle 184 on Inquiry Card

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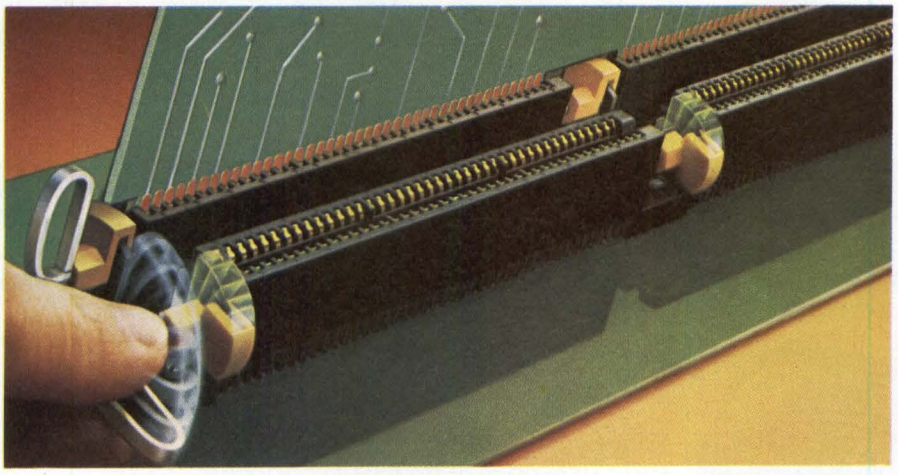

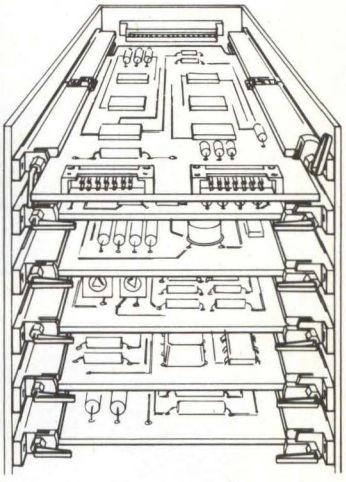

These pre-assembled edge connectors eliminate any need for force to mate with high density boards. That's why we call them ZIF. For Zero Insertion Force. Just open the contacts with the rotary cam, and slide in your board. No more jacking devices. No more mallets. No more worn contacts or damaged boards. And board costs are reduced because less gold is needed and chamfered edges are eliminated.

If you can get all your I/O's to one edge of the board, ZIF connectors will accommodate up to 240 lines. If you can't, use side entry ZIF connectors—they replace card guides—and use up to four sides of the board. You can isolate critical circuits, separate incompatible voltages and improve real estate use at the same time. By putting connectors on the sides, you open up the ends for free passage of air and better thermal management.

Add the option of sequential actuation of ground, power and signal contacts. Now you can "power up" or "power down" at the board level with no concern for transient pulses or static discharge through sensitive circuits.

AMP Rotary Cam ZIF Connectors are available in sizes up to 65-dual positions, with ends open, or closed, and with an integral board lock that assures proper PC board registration.

Need more details? Call the AMP Rotary ZIF Information Desk at (717) 564-0100, Ext. 8400. Or write AMP Incorporated, Harrisburg, PA 17105.

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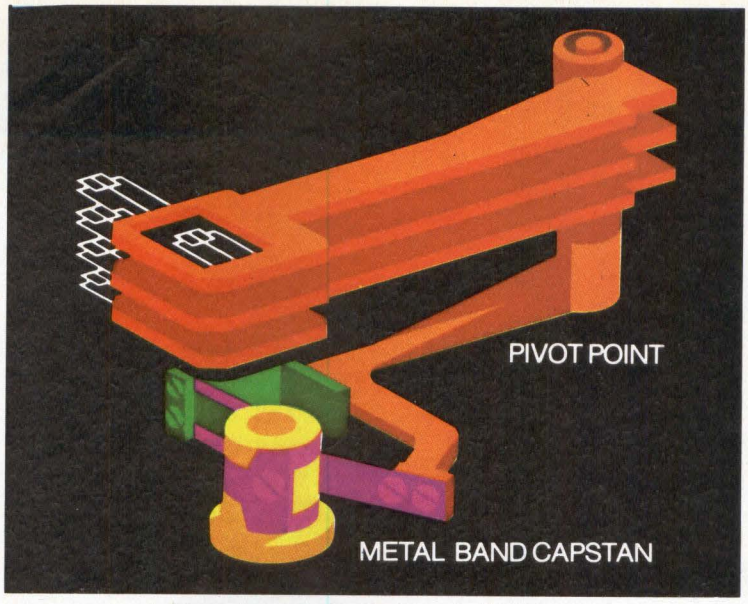
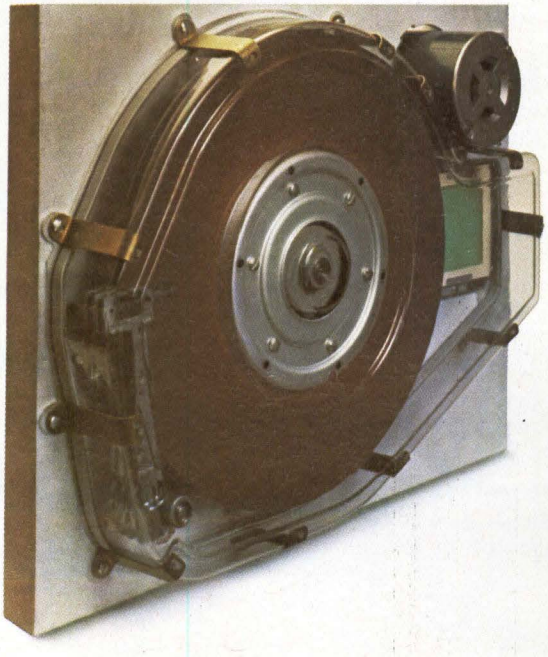
Shugart fixed disk drives use industry-proven Winchester head and media technology to preserve your data in its own safe, sealed environment. The model SA4004, with 14.5 megabyte capacity, utilizes one disk and four heads. The SA4008, 29 mbyte version, has two disks and eight heads. Eight optional fixed heads are available to give you an additional 144 kbytes (unformatted) of head-per-track storage for applications such as indexed files or table look-up. The SA4000 Series offers an easy upgrade too. Keep your floppys for I/O and system back-up. Add our rigid disk drives for the additional capacity and throughput you need to upgrade your operating systems and mass storage.



When You Think Actuators, Think Fasflex II.™ Shugart's new, proprietary Fasflex II™ is another result of Shugart's headstrong commitment to R&D. This open loop band actuator is virtually wear-proof, and it doesn't require any adjustments in the field. Heat dissipation? With Fasflex II it's extremely low—only 200 watts is typical. But the Fasflex II acutator is only one of the benefits you get with the SA4000 series. The drives weigh a mere 35 pounds—that's about half the weight of comparable units. They're compact. They use only 5.25 inches of panel space, they can be easily mounted in a 19-inch RETMA rack. The drives are rugged, yet easy to maintain. The PCB's and spindle drive motor are open and accessible on the underside of the drive. No preventive maintenance is required.

# of its class megabyte.

And If You're Looking at the Bottom Line. SA4000 drives are easy to integrate into your system. The drives utilize a simplified interface which can be easily designed into your system. In addition, you can use the same power supply for both the SA4000 drives and floppy drives, since they have the same voltage requirements. Want to get on-line quick? Our new SA4600 controller handles up to four SA4000 drives. Bottom line? Lower overall system cost. So now's the time to design a classy system with the head of its class—the compact, reliable, low cost SA4000. Shugart Associates, Headquarters: 435 Oakmead Parkway, Sunnyvale, California 94086 (408) 733-0100; West Coast Sales/Service: (408) 737-9241; Midwest Sales/Service: (612) 574-9750; East Coast Sales/Service: (617) 893-0560; Europe Sales/Service: Paris (1) 686-00-85; Munich (089) 17-60-06.



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CIRCLE 48 ON INQUIRY CARD

DIGITAL CONTROL AND AUTOMATION SYSTEMS

Microprocessors Are Key Control Elements In Energy Management Systems

A significant number of papers presented at the 5th Annual Conference of the IEEE's Industrial Electronics and Control Instrumentation Society involved control of power consumption, utility demand, or other phases of energy management. That subject, of course, is of particular interest because of the considerable activity in developing control systems that help alleviate problems resulting from the current long term fuel shortage. For that reason, the following reports are discussed separately from the larger number of IECI '79 general control and data acquisition applications covered in the July issue (pp 66-86).

Monitoring Residential Uses of Electricity

Because of cyclic variations in load, more than 30% of a typical utility's capacity regularly remains unused for several hours of each 24-h period. Yet those utilities must maintain adequate capacity to handle peak loads. It has been estimated that the equivalent effect of three or four years of construction would be gained if some of the peak load could be shifted to off-peak hours.[1]

Load management tools such as the time of day or time differential billing schemes that have been in use for some time, but which require varying degrees of cooperation and attention by residents of the homes, have not been particularly successful. Moreover, involved systems that monitor multiple loads, ambient temperatures, and total power consumed were found to be cumbersome, costly, and not well accepted by homeowners.

One prototype energy-use surveying system consists of a single data collection unit, a voltage sensor, and an individual current sensor at each device being monitored. The collection unit receives data from eight sensors, calculates energy use for each appliance, and stores 24 h of reduced data. (In a production unit, data would have to be recorded or transmitted daily to prevent being overwritten by new data.)

For this system the designers chose an Intel MCS-48 single-chip microcomputer. As well as providing timing, memory, and interfacing on one chip, this device nests subroutines with a minimum of programming effort, an essential that the system designers considered crucial. In addition, the 3-state address/data "bus appeared to be the most expedient means of multiplexing the various microcomputer peripheral devices to the microprocessor."

An 8-bit address latch (Fig 1) holds the address of memory mapped I/O and a UART handles transmission of data to a terminal. A battery backup power supply supports a CMOS time of day clock that is implemented with IC counters and latches. Time of day is read over the bus under program control.

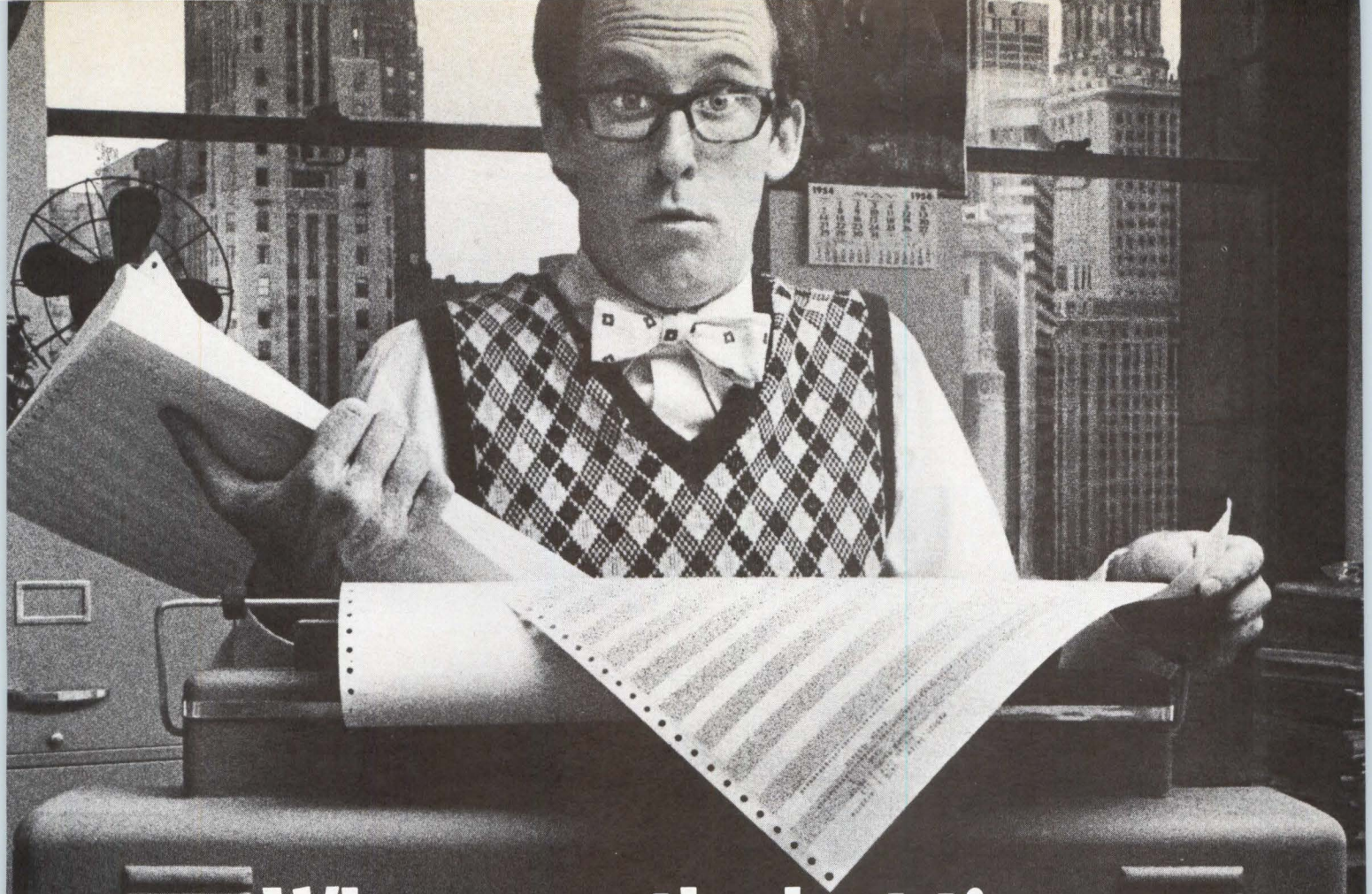
Imminent failure of the dc power supply is sensed by a power transition sequencer that disables both the CMOS RAM select line and time of day clock increment lines to protect them from unpredictable power down and up states. During the first 50 μs of program execution the sequencer maintains the CMOS RAM and clock increment lines in a disabled state while the first few lines of program initialize and stabilize the microprocessor I/O ports.

A portable control panel enables the installer to watch and correct clock time of day value, or monitor output of the sensors. The bus interface protects the microprocessor bus from forced logic states generated when the panel is being plugged in or unplugged.

Total parts cost of the prototype was $270 (based on the premise of 100-piece pricing). In a second version nearly ready for field trials, calibration constants will be stored in fusible link P/ROM. Programming will be accomplished through the control panel. Data will be transferred daily to a cassette tape and collected monthly. Original plans called for 25 of these units to be tested in residential environments this summer.

Monitoring and Controlling Residential Energy Distribution

Continually increasing costs of energy have made an energy conservation system almost a necessity—particularly in an all-electric home. Such a system, to



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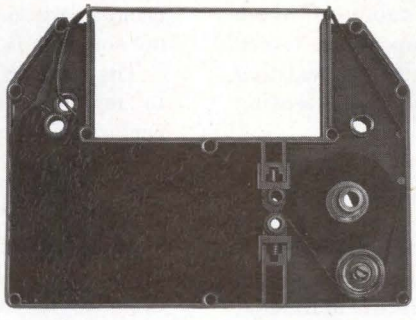

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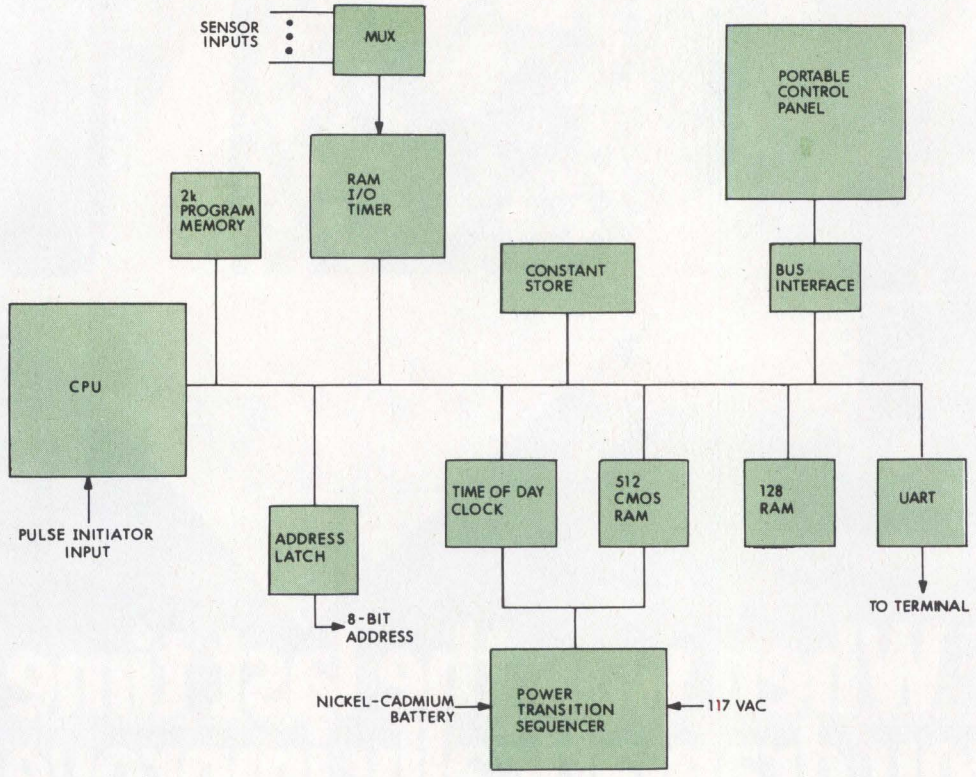

Fig 1 Prototype data collection unit hardware for residential power consumption monitor.[1] Peripherals attach to CPU via 8-bit wide 3-state multiplexed address/data bus

be truly effective, must attain sufficient sophistication to eliminate human intervention by adjusting thermostats. In one example, a dedicated realtime microprocessor controller monitors and controls energy distribution in an all-electric residential structure which contains a 45k-Btu/h (13-kW) heat pump and a forced air furnace.[2] This system can be installed in existing homes without additional wiring from remote sensing units.

Sensors located in each room of the house are scanned at regular intervals by the system controller, an Intel 8080 microprocessor. Because communication between microprocessor and sensors is maintained over the ac power line, there is no need for new wiring (Fig 2). Determination of temperatures in individual rooms governs microprocessor control of a forced air furnace.

When the system is installed, the user specifies the desired comfort temperature value for each room. After that the user has no need to touch the system unless temperature values are to be changed. In that event, changes are made through a CRT terminal. The user, however, does place each remote sensing unit into occupied or unoccupied mode depending on whether or not someone is in related rooms.

The system uses an 8k control basic interpreter to monitor and process data. Control functions are performed by machine language subroutines.

Control of Cogeneration to Minimize Fluctuating Process Disturbances

Syncrude Canada Ltd's tar sands plant, capable of producing 125,000 barrels of oil per day, uses a combined cycle cogeneration plant to provide hot water, steam, and electrical power—but is also connected to the Alberta Power Ltd system on a demand basis. Although cogeneration—the use of steam that operates power generators for a second purpose such as, in this case,

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Feature \ Printer	Integral Data 440	Tally 1200	Lear-Seigler 300	Texas Instruments 810	Centronics 779-2
96-character ASCII set, upper and lower case	YES	OPTION	YES	OPTION	NO
Software-selectable character sizes	YES	NO	NO	OPTION	NO
Throughput, lines per minute @ 10 char./line @ 132 char./line	 275 42	 100 40	 Data not available	 440 64	 130 21
Parallel and RS-232 serial interfaces standard	YES	NO	NO	NO	NO
CRT screen buffer	OPTION	NO	OPTION	NO	NO
Footprint (W x D = sq. ft.)	1.37	3.45	3.18	3.58	2.44
Weight (lbs.)	20	64	50	55	45
Forms length control	YES	OPTION	YES	OPTION	NO
Full dot plotting graphics	OPTION	NO	NO	NO	NO
Unit Price	$995	$2500	$1995	$1895	$1350

Comparison data from manufacturers' current literature.

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Integral Data Systems, Inc.

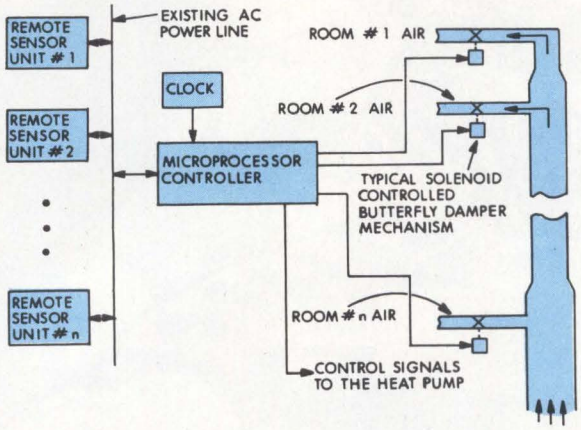

Fig 2 Portion of basic energy conservation system for all-electric home.[2] Existing ac power line serves as communication circuit between controller and remote sensing units in individual rooms. Microprocessor scans sensing units and then positions solenoid-controlled butterfly damper mechanism in forced air furnace to increase or reduce heat to rooms

to loosen tar sands—is said to be a promising partial solution to the energy crisis, control must be stringently maintained.

In the Syncrude application, the control system involves both the local generation complex and the tielines for importing or exporting electricity from or to the utility company. A control scheme has been configured that avoids demand charges and maintains plant frequency when separated from the tielines.[3]

The stringent interchange agreement between Syncrude and Alberta Power is that Syncrude will return to Alberta Power each clock hour an amount of electrical energy equal to that taken from the utility company during that hour. Any power not returned by the end of each hourly period is considered to be power purchased on a demand charge basis (defined as the highest net kilowatt hour or per joule imported in any one clock hour during the current month). There is no credit for negative billing demand or for net energy export.

Because of process conditions, fluctuations of 35 MW can occur every minute, with less frequent, 75-MW swings depending on the number of drag lines operating. Under these conditions, lack of control can result in high demand charges.

Tieline control is based on average rather than instantaneous power values. Necessary load filtering must not introduce large time constants. The error adaptive control computer was chosen to provide the required filtering. A power corrective term, a function of both energy error and time remaining in the hour, is used for convergence at the end of each demand period.

Frequency control is met by integral action. Automatic transfer from tieline control mode to frequency control mode is provided by a tieline trip, plus more rapid adjustment of generation on overfrequency and blocking of control action on underfrequency.

Control is divided into five major areas: calculation of demand control error, of adaptive controller gain, and of control action required; allocation of control action to the units; and interface of unit controllers with generating units. In essence, the control criteria are to stay within the demand limit, hold plant frequency when separated from the tieline, meet system constraints, and minimize unnecessary control action.

Automating Environmental Control In Buildings by Hierarchical System

Components of a distributed microcomputer system developed at the University of Houston for monitoring, recording, and controlling the thermal and electrical energy consumption of buildings operate either as part of the system or standalone. Almost normal operation can be maintained even when the overall system cannot function as an entity.[4]

The system, called HIDEMS or hierarchically distributed energy management system, has three separate components: motor control unit, thermal control unit, and central control unit (Fig 3). System hardware and software allow all functions of the three units to be handled either by individual microcomputers or by the central control unit alone. When implemented individually, the motor and thermal control units accept commands from an operator through a keyboard or data terminal as well as from the central control unit.

In operation, the motor control unit monitors and controls operation of motors and computes consumption of electric power. The thermal control unit monitors temperatures, flows, and pressures; controls the air discharge temperature of air handling units; and computes the energy used in heating and cooling. A slave mode of operation allows the central control unit to coordinate functioning of all other control units, to log system data for further processing, and to transfer operator commands to the other appropriate control units.

All control units incorporate 6800 microprocessors and, where possible, commercially available micromodules. I/O interface cards are functional modules

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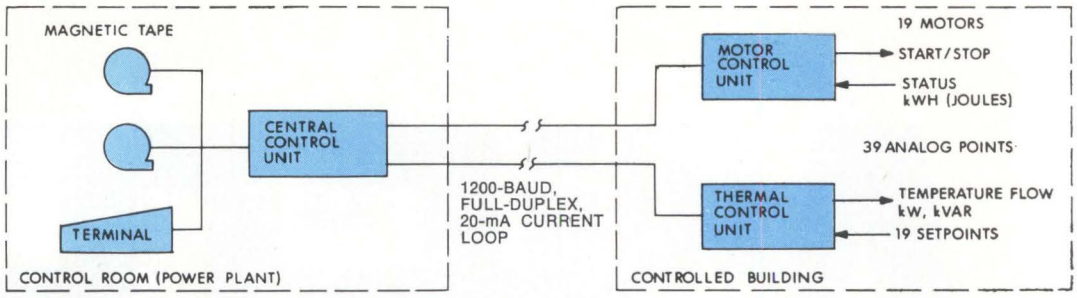

Fig 3 Configuration of hierarchically distributed energy management system (HIDEMS) for buildings.[4] Motor and thermal control units can function independently or under command of central control unit. System controls motor operation and air discharge temperature, and computes power consumed by both motors and heating/cooling units

and include all firmware and interface hardware for a specific operation.

Software consists of function tasks, diagnostic programs, and a realtime executive. The most complex software task, the man-machine interactive task, supports the front panel keyboard and display, the data terminal, and the master communication interface to another processor.

Communication between the central control unit and the other two control units is through a 1200-baud, full duplex, 20-mA current loop. Each dedicated control unit is polled by the central control unit at 10-s intervals so that the control unit essentially contains all information on the other data bases.

This system has been in operation continuously for 1 year with no malfunctions. A simplified version is being designed for implementation as a kit for use in high school installations. In addition, to increase system versatility, a control language is being developed to allow the user to create commands to perform special functions based on environmental factors and system variables.

Monitoring and Controlling HVAC Energy Consumption in Navy Buildings

Energy control requirements for Navy buildings are being met by development of microprocessor based monitoring and control modules under direction of the Navy Civil Engineering Laboratory. Under separate contracts, a microprocessor time clock and a programmable building controller have been produced. It is estimated that significant savings in energy consumed for heating, ventilation, and air conditioning (HVAC) would result from installation of such devices in 6000 of the more than 20,000 Navy buildings.[5]

Concept of the intelligent clocking device was that it should tie into a supervisory network for reporting, as well as serving as a time clock. In practice it samples interior temperatures, and then determines zone temperatures from time and space weighted averages of the samples. Zone temperatures are used to determine the times that heating or air conditioning units must be turned on to meet comfort conditions at start of work.

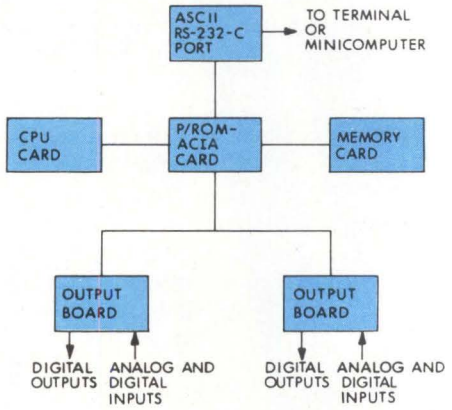

Fig 4 Programmable building controller in Navy HVAC system.[5] A-D converter on output board [which can be 2000 ft (610 m) from controller] digitizes inputs before sending them to controller

Requisites for the programmable building controller were that it not be dedicated to a particular building type or environment, that it be programmable in a high level language, and that it be capable of standard operation as a remote station in a distributed network. The resultant unit is user programmable in

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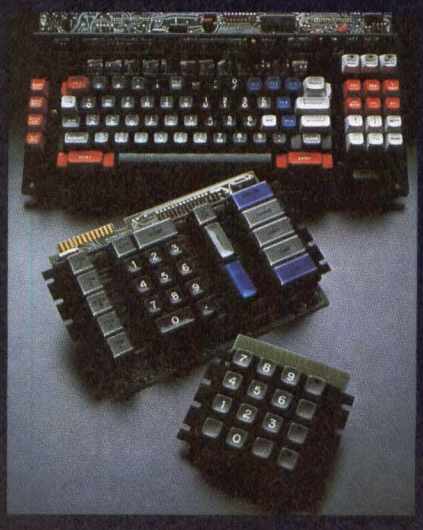

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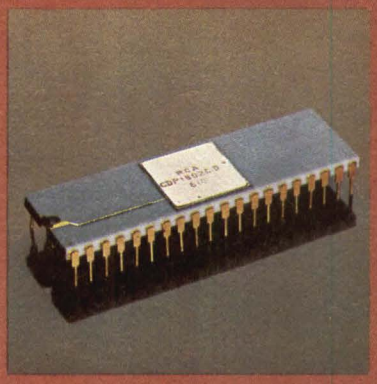

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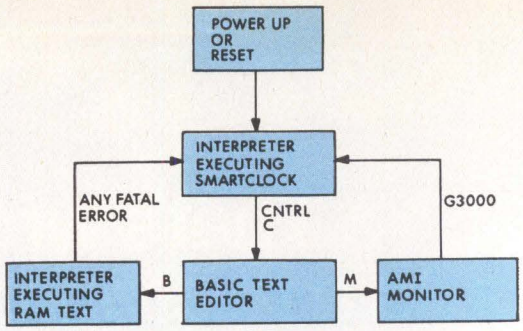

Fig 5 Software structure of programmable building controller in Navy installation.[5] BASIC interpreter was chosen because it met requisite for high level language and was easy to program. Key operating element is SMARTCLOCK. AMI monitor provides use of subroutine library for diagnostics, P/ROM programming, and other functions

BASIC and meets both other requisites by adding relevant I/O boards.

Building controller hardware (Fig 4) is based on an American Microsystems EVK 6800 microprocessor, and includes 5k of RAM, 2k of ROM, and 6k of EPROM. Onboard clocks have battery backup. Up to 64 digital inputs and 64 outputs can be handled (up to 16 analog or digital inputs and 8 or 16 digital outputs per output board). Data are transmitted in ASCII form by a universal asynchronous receiver transmitter on a balanced line current mode link.

Key software element is the block labeled SMARTCLOCK in Fig 5. The controller automatically begins executing SMARTCLOCK routine (in EPROM) on power up, power reset, or any fatal error. Because SMARTCLOCK is the intelligent time clock, the other module in the HVAC system, this serves as a failsafe operation to assure significant energy savings.

User commands cause the controller to turn to the BASIC text editor for program entry and editing. Commands may be entered for either deferred or immediate execution.

The BASIC interpreter, called MUDD BASIC and written for process control, is a subset of Dartmouth BASIC. It contains memory intensive functions such as exponentials, logarithms, and trigonometric functions. Predimensioned arrays were used for data storage, prioritizing, sensor inputs, and time decrementing.

References

All of the following items are included in the *IECI '79 Conference Proceedings.*

1. I. H. Thomae and W. Taylor, "A Multiple Input Residential Power Consumption Monitor," pp 79-82
2. S. K. Kavuru, "A Microcomputer Controlled Residential Energy Conservation System," pp 88-91
3. C. S. Ross *et al*, "Cogeneration with Utility Demand Control Employing Error Adaptive Techniques," pp 93-98
4. C. J. Tavora, "A Hierarchically Distributed Energy Management System," pp 156-160
5. R. I. Staab and D. M. Shiroma, "Microprocessor Energy Controllers for Navy Buildings," pp 110-114

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Circle 160 on Inquiry Card

Programmable Controller Memory Utilization Improved by Optional Instruction Set

Efficiency of model 484 programmable controllers can be increased even further through use of an optional Enhanced II instruction set. According to Gould Inc, Modicon Div, PO Box 83, Shawsheen Village Station, Andover, MA 01810, the added features improve memory utilization and decrease software design efforts for batching tasks, increase efficiency of reading discrete inputs and outputs, aid in developing shift registers, improve scan times for isolated high speed machine sequences, and improve controller scan times in critical monitoring and control applications.
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Voltage to Current Converter Supplies Instrument Levels

Any voltage can be converted to the 4- to 20-mA levels required for process control instrumentation with the model 930/MK298 voltage to current transducer. The device, from Calex Mfg Co, Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523, consists of a programmable current source, PC card, 15-pin mating connector, and discrete components required for interfacing. By changing one resistor other current changes can be obtained.
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English Language Programmable Controller Meets Wide Range of Requirements

Both novices and experienced programmers can use the M-2000 programmable controller acccording to Industrial Automates, Inc, 6123 W Mitchell St, Milwaukee, WI 53214. The programming format is in plain English. Inputs and outputs (16 each) function at 115 Vac and are optoisolated for noise immunity. In addition, there are one 115-Vac interrupt output and three 5-Vdc pulse outputs. Steady load current of 1 A is controlled by zero crossing triac outputs. Switch selectable RAM and EPROM of 1k each are standard.
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Automated NC Tape Preparation System Accepts Inputs from Light Pen

Preparation of numerical control tapes for automatic wire termination systems can be automated by use of the Pen-Entry 2000 design system offered by Wire Graphics Ltd, 555 Broad Hollow Rd, Melville, NY 11746. The system is made up of a 48k-byte minicomputer, dual floppy disc drives, interactive CRT display, light pen, tape punch, and 150-char/s printer. The operator displays the area of interest on the 15″ (38-cm) CRT and then inputs required wire connection via the light pen. Both the paper tape for the wirewrapping equipment and hardcopy documentation are produced by the system.
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Realtime Control Software Offered for Computer Family

Under a joint marketing agreement, AIM automated industrial monitoring and control software will be offered to run on the complete family of Classic computers manufactured by Modular Computer Systems, Inc, 1650 W McNab Rd, Ft Lauderdale, FL 33310. The process software, developed by Biles and Associates, 7207 Regency Sq Blvd, Houston, TX 77036 for realtime data acquisition and control, provides fill-in-the-blanks industrial automation language for scanning, alarming, logging, and control. Data can be displayed either by plant area or by individual points. Online addition, deletion, or modification of measurements can be made.

"AUGAT PANELS CUT OUR DEVELOPMENT TIME FROM YEARS TO MONTHS."

Bob Spencer, General Manager Exsysco,
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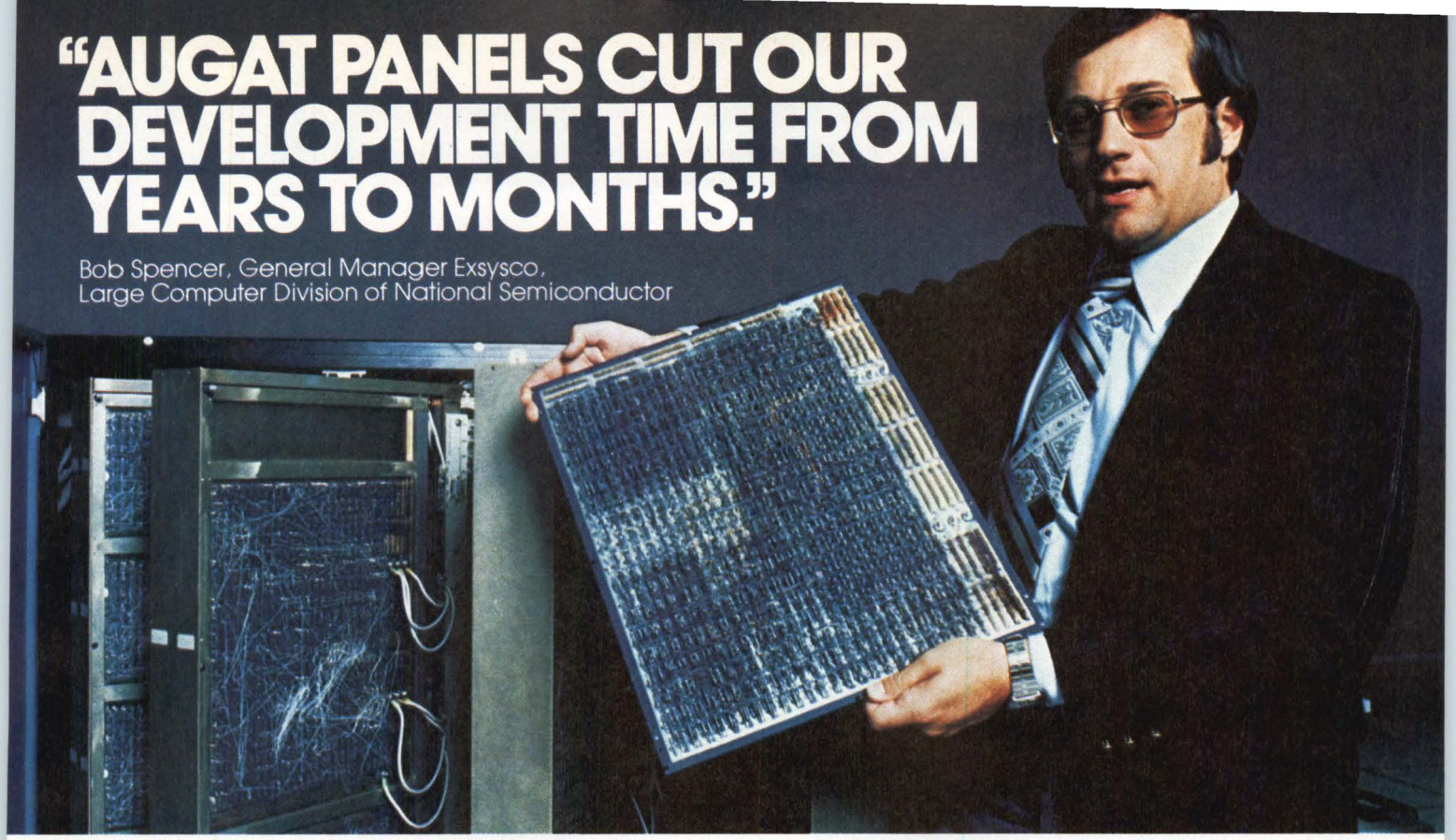

The dynamics of the computer industry demands that manufacturers capitalize on opportunities during the limited lifespan of the "current" technology. That's why initial development time is crucial. One sure way to cut that time is with Augat Wire-Wrap* panels. Bob Spencer explains: "Multi-layer boards meant a lead time of a year or more to design and prototype with another six months to get into production. With Augat boards, we reduced this cycle to a few months and started production the day we approved the prototype. Augat also gave us a flexibility to make circuit changes during the development cycle without causing delays."

Time isn't the only consideration—cost is also critical. "The expense to design and develop dozens of different, large multi-layer boards can easily run into the hundreds of thousands of dollars, not to mention staffing and equipment. The Augat approach drastically reduced these costs allowing us to concentrate our resources on other critical design elements."

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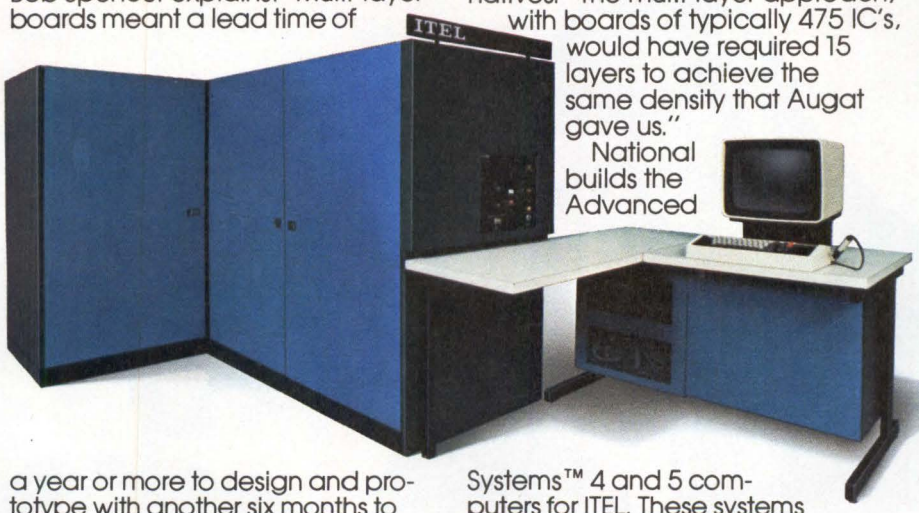

National builds the Advanced Systems™ 4 and 5 computers for ITEL. These systems must offer high reliability. "As the temperature inside a computer goes up, the reliability goes down. Augat boards reduce the temperature problem because Wire-Wrap pins are excellent radiators."

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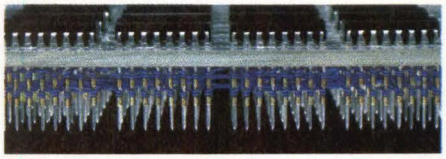

How would Bob Spencer rate the performance of Augat Wire-Wrap panels? "Excellent! Our system uses high speed ECL throughout. Augat's patented logic panel, combined with unique automatic wiring from Augat's Datatex subsidiary, performs with no noise or transmission problems."

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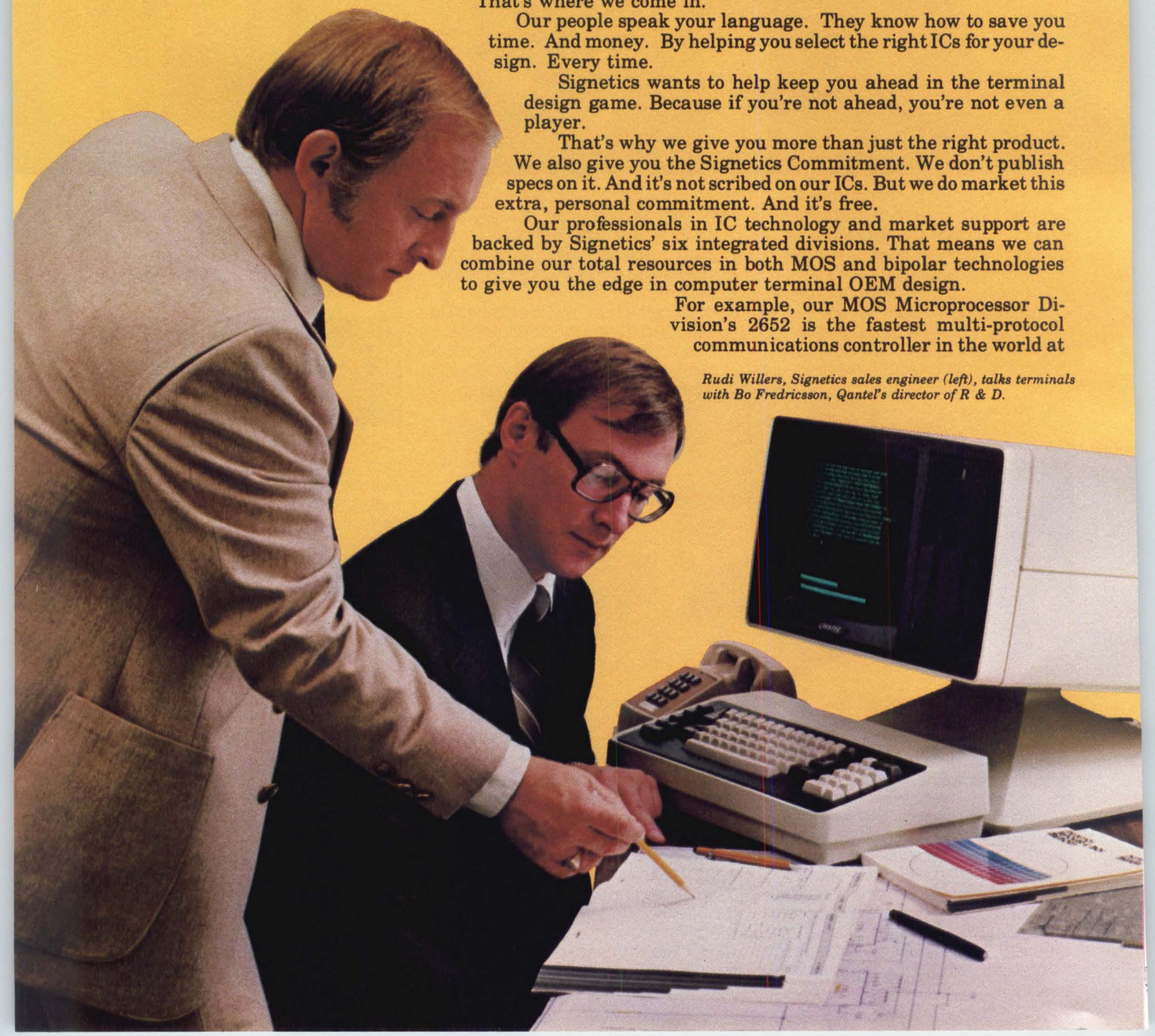
Signetics wants to help keep you ahead in the terminal design game. Because if you're not ahead, you're not even a player.

That's why we give you more than just the right product. We also give you the Signetics Commitment. We don't publish specs on it. And it's not scribed on our ICs. But we do market this extra, personal commitment. And it's free.

Our professionals in IC technology and market support are backed by Signetics' six integrated divisions. That means we can combine our total resources in both MOS and bipolar technologies to give you the edge in computer terminal OEM design.

For example, our MOS Microprocessor Division's 2652 is the fastest multi-protocol communications controller in the world at



Rudi Willers, Signetics sales engineer (left), talks terminals with Bo Fredricsson, Qantel's director of R & D.

Spoken Here.

2Mbits/second. It's right at home with most high-level protocols.

Every computer terminal OEM looks for unique logic functions. With the smallest amount of random logic practical. And Signetics wants to make it easy for the designer.

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With our family of field programmable logic, including the FPLA, FPGA, and ROM patch, we make it easy for you to out-design the competition.

And more design freedom's on the way. We'll soon be offering the world's first Field Programmable Logic Sequencer.

Responding to your needs, our Logic Division created the bipolar 8X300 μP. Its blazing speed of 4 million operations/second and control-oriented architecture make it ideal for adding state-of-the-art peripherals to your terminal system.

While our field professionals help computer terminal OEMs translate difficult design choices into the right ICs, other Signetics professionals are applying the most advanced technologies into devices to meet the OEM's future demands.

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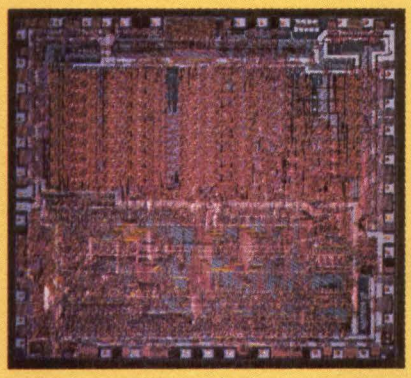
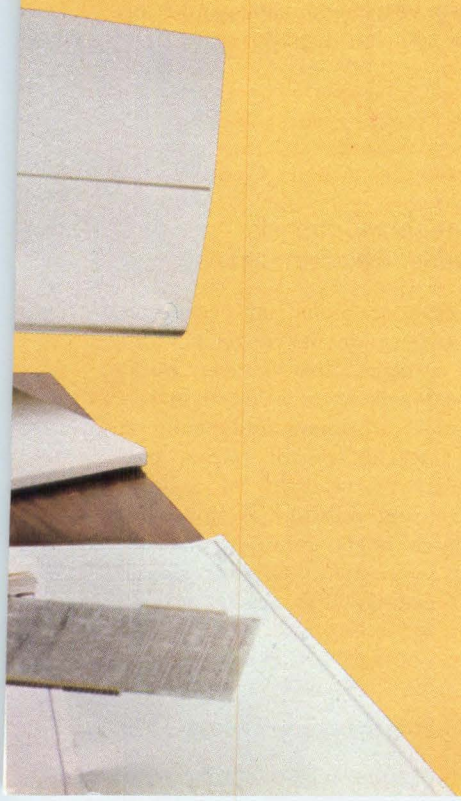
To learn how our leading-edge technologies are making innovation simpler for terminal OEM designers, write us today.

We've got a brochure that tells you how you can put our advanced ICs to work for you. On your own terms.



2652 multi-protocol communications controller



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Mapping System Designed for Municipalities and Utilities

Map planning and updating can be accomplished quickly and accurately with a minicomputer based system intended for use by either municipalities or utilities. The interactive mapping system, announced by California Computer Products, Inc, 2411 W La Palma Ave, Anaheim, CA 92801, allows users to revise a map on a video graphic display, plot a hardcopy of the new map in minutes, and obtain a hardcopy report of the latest revisions for management.

The mapping system is based on the IGS 500 interactive graphics system. As many as four users can work simultaneously on different jobs. Map subareas can be chosen for viewing simply by pointing at them.

Included in the system are a minicomputer with 64k words of memory, software, disc drive, operator's console, plotter, and printer. A user workstation contains picture processor, separate alphanumeric and graphic CRTs, keyboard, 11 x 11″ (28 x 28-cm) graphics tablet, and joystick picture controller.

Circle 165 on Inquiry Card

Data Collection System Meets Needs Of Both Large and Small Firms

Data collection system 15 provides processors and software needed to control and direct networks of data gathering terminals in factories or plants. Because it is modular, the system can be expanded in phases from a basic level to full implementation. According to NCR Corp, Dayton, OH 45479, this system from its Data Pathing Div provides a level of sophisticated capabilities not previously available at its price range.

The basic system has 64k bytes of memory, but two other processor models provide up to 256k bytes. Terminal adapters can handle from 10 to 250 units located within a single plant area or at remote locations. Optional features enable communication between system processors and central site mainframe computers.

A data collection operating system controls both terminal and processor operations and communications. AIDE, an applications program generator, provides applications handling capabilities.

Circle 166 on Inquiry Card

CNC/DNC System Uses Bubble Memory

Up to 100k bits of magnetic bubble memory are provided in the Dina-Mite control system, said to be the first application of that technology for the metalworking industry. As many as four axes of machine control can be programmed by the operator or through telephone inputs from a remote station at any distance. Available for both CNC and DNC operations in large or small plants, this system from Optograms, Inc, PO Box 3150, Oakland, NJ 07436 provides multiple commands and diagnostic capabilities through a 240-char display.

Circle 167 on Inquiry Card

Small Programmable Controller Meets Most Process Requirements

Control of virtually any type of industrial process is promised for the IMP-3 programmable controller introduced by Automation Systems, Inc, Lancer Park, Eldridge, IA 52748. It can address up to 512 I/O in any combination and any number of timers and counters. The logic unit has 256 internal control relays, half of which are retained during power-down for at least six continuous months. Program memory is stored on a light erasable P/ROM which holds up to 4k instructions. Scan time is 4 μs/instruction. Average power consumption is 10 W and average unit size is <1 ft^3 (<0.03 m^3). □

Circle 168 on Inquiry Card

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CIRCLE 58 ON INQUIRY CARD

COMPCON 79
IEEE Computer Society International Conference

September 5-7

Capitol Hilton Hotel, Washington, DC

Portia Isaacson
General Chairperson

John Michael Williams
Program Chairperson

Shirley Ward Watkins
Tutorial Chairperson

"Using Microprocessors—Extending Our Reach" is the theme of the 19th IEEE Computer Society International Conference. Chaired by Dr Portia Isaacson of Electronic Data Systems Corp, the conference will present the latest developments in microprocessor architecture, support software, operating systems, and peripheral devices. Following this theme, a variety of microprocessor applications, stressing uses in business, industry, education, and the home, will also be explored.

Three keynote addresses open the conference on Wednesday, September 5, at 9:30 am. The 30 program sessions, arranged by Technical Program Chairperson Dr John Michael Williams of System Development Corp, are slated for the three days of the conference. Topics of the program sessions scheduled for Wednesday early afternoon are novel microprocessor architecture, software development principles for microprocessor systems, and practical low cost natural language translators. The late afternoon sessions will discuss LSI minicomputers, microprogramming languages, and personal and consumer computing.

Papers presented Thursday at 9 am will cover high level language oriented microprocessors, energy and environmental monitoring applications, issues in security, and microprocessor technical standards. Data base machines, advances in voice communications (I), export

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Military operations at rugged, remote sites demand a reliable data system that provides answers to vital questions...with no waiting.

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CIRCLE 59 ON INQUIRY CARD

controls on microprocessors, and new directions in virtual machine technology are the subjects to be covered at the 11 am sessions. Early afternoon presentations will feature picture processing graphics, advances in voice communications (II), space and military applications, and microprocessor developments in the Middle East, Africa, and Southeast Asia. VLSI architectural implications in Japan and interprocess communications are slated for late afternoon Thursday.

In the Friday morning sessions, special purpose microprocessors, microprocessor communications, and small mass storage are presented at 9, with multiple microcomputers, microprocessor applications in Japan, and peripheral controller chips given at 11. The conference winds to a close Friday afternoon with sessions dealing with using tools in microprocessor system development, test technology, and design and application of intelligent scientific devices.

Tutorials

Three preconference tutorials, arranged by Tutorial Chairperson Shirley Ward Watkins of the National Bureau of Standards, will be offered Tuesday, September 4. The first of these, "Design of Microprocessor Systems," will stress the range of available microprocessor products and the development tools for microprocessor based design. The entire design effort, with emphasis on system configuration, software development, and system testing will be presented by Dr John H. Carson of RLG Associates, Inc.

In "A Practical View of Computer Communications Protocols," Dr John M. McQuillan, of Bolt, Beranek and Newman Inc, will examine the fundamental design choices in computer communications systems, investigate fundamental protocol choices within computer communiations systems, and discuss existing offerings.

The third tutorial, "Microprocessor Project Management" will synthesize the experience of hundreds of project managers (who learned the hard way) into a practical, field proven methodology for managing all phases of microprocessor application. Presented by Eric R. Garen, this course will emphasize high risk, high cost, and time critical problems unique to microprocessors.

Registration

Advanced registration for COMPCON Fall '79 must be completed by August 24. Conference only or tutorial only registrations are $65/80 (member/nonmember). Fees for a tutorial course plus the conference are $130/145. The tutorial registration fee includes luncheon and notes; conference registration includes one copy of the proceedings and two complimentary drink tickets for each of the conference hosted cocktail parties, Wednesday and Thursday evenings. Late registrations (after the August 24 deadline) are an additional $10 throughout. Late registrations at the conference will be accepted at the Capital Hilton Hotel beginning Monday evening, September 3. To register, or to request further information, contact COMPCON Fall '79, PO Box 639, Silver Spring, MD 20901. Tel: 301/439-7007. □

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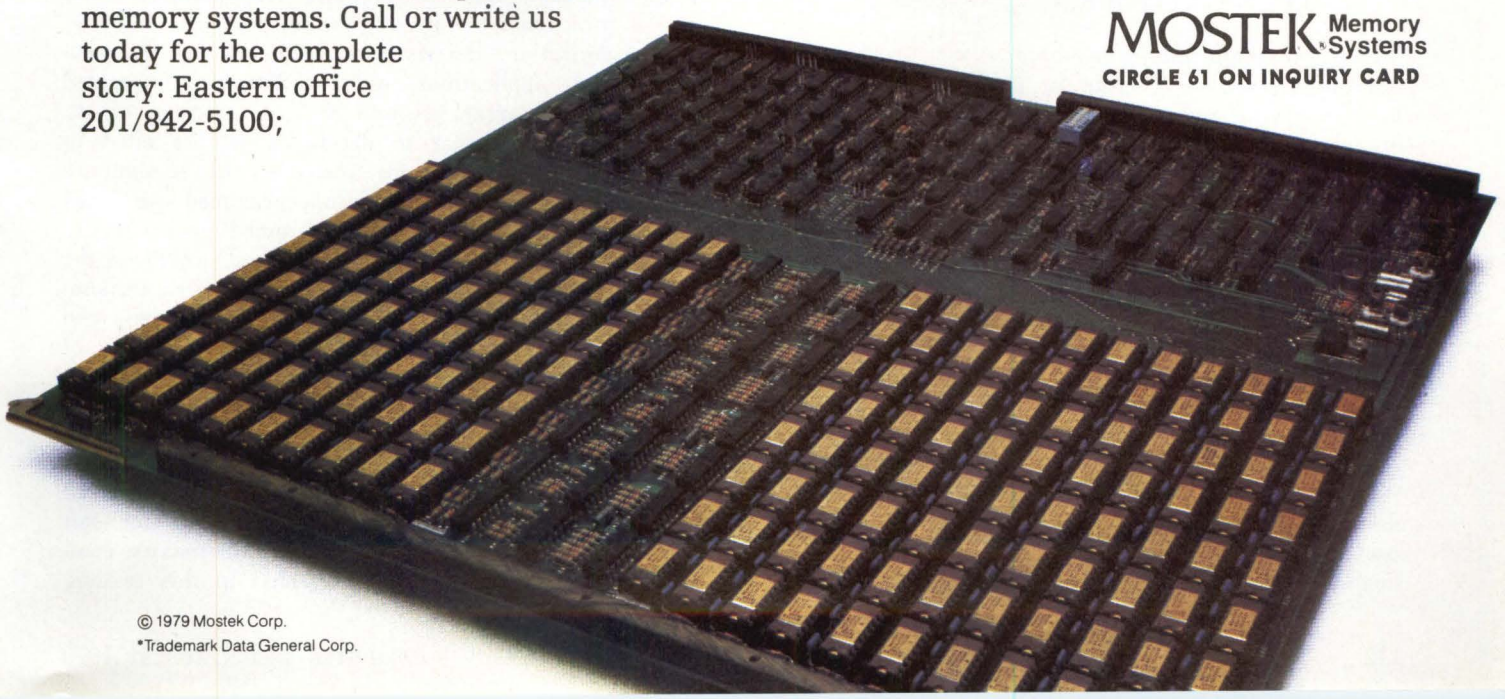

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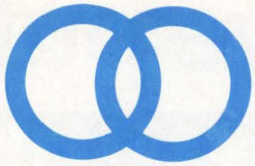

Wescon/79

Western Electronic Show and Convention
September 18-20
St Francis and Hyatt on Union Square Hotels
Civic Auditorium and Brooks Hall
San Francisco, California

Wescon/79, at the St Francis and Hyatt on Union Square Hotels will open a "Gateway to the Eighties." Focusing on product and systems innovations designed to influence industry and home in the next decade, the West's largest high technology event formally opens with a preview presentation Monday, September 17 that features an all-day marketing conference and the keynote luncheon. Presenting the keynote address will be Dr John A. Pierce, Professor of Engineering at California Institute of Technology. He will project a future in communications where "we will have one digital world in which transmission, processing, computing, storage, switching, voice, pictures, and data will be inextricably intertwined both in communication facilities and in their use."

Professional Program

While no single subject dominates the program, the microprocessor looms large in proportion among the more than 120 technical and professional presentations organized by Program Chairman Rudolf Panholzer, Navy Postgraduate School. There will be papers on memories for microprocessors, single-chip microprocessors, microcomputers in aiding the handicapped, and microprocessors in energy conservation. Professional program sessions will be held at 10 am and 2 pm all three days of the conference. Following are profiles of several sessions of interest to *Computer Design* readers.

In the session entitled "High Speed, Low Cost Number Crunchers," five authors present LSI hardware and techniques that both augment and implement floating point operations and thus speed array processors. One paper reviews the speed and cost tradeoffs of mainframes, minicomputers, and array processors. Others discuss the use of LSI multipliers, hardware shift matrices for floating point addition or subtraction, and the exploitation of LSI memory components instead of dedicated arithmetic devices. A fifth author proposes that bit-serial arithmetic hardware take the place of the traditional parallel approach for array processors and contrasts advantages and disadvantages of the two. Following each presentation will be five minutes of questions and answers. The authors, two panelists, and the moderator will hold an open panel discussion during the second part of the session. Questions will be posed to the panel from a list prepared in advance as well as from the audience.

New techniques and components available to improve high speed bipolar microprogrammable microprocessors are advanced in "Bipolar LSI for Microprogrammed Machines." Significant concepts and applications of a family of 8-bit ECL microprogrammable bit-slice circuits are described in one paper. These bus-oriented building blocks include an address and data interface unit, a multiple function network, a dual access stack, and a programmable interface unit. Physical and logical organization, design, manufacturing process, features, and applications of a 1200-gate integrated Schottky logic array, as well as a comparison of ISL technology and similar IC developments, are cited in another paper. Other topics treated in this session are predictive techniques in microprogrammed pipelined systems and a 16-bit microprogrammed controller.

"Memories for the Microprocessor Age" addresses the impact of microprocessors on memory users and manufacturers at the minicomputer level and in dedicated systems. One author explores design considerations of both memory components and memory systems for 16-bit microprocessors. The market response to pseudo- and quasistatic memories—memories that blend capabilities of static and dynamic devices to accommodate special functions needed in microsystems—is queried in another paper. Memory system strategies for soft and hard errors and bus structures for today's computers are other topics also presented in this session.

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Two Wescon sessions cover development systems. "Microcomputer Development Systems: Universal or Dedicated?" will provide information to facilitate direct comparison of several development systems including the 8002 microprocessor lab, Futuredata's universal development system, the MicroMOS universal development system, and the Intellec. One author questions whether there is such a thing as a development system in "The Impact of New Microprocessors on Development Systems," while another asks "Is There Life After Emulation?" Other authors outline a low cost development tool for next generation microprocessors, and the growing use of universal development systems by project engineers to run benchmark tests for selection of one chip vs another.

Exhibit

Booths by more than 400 exhibitors will be set up in both the Civic Auditorium and Brooks Hall. The show will open at 9:30 am all three mornings of the convention, and close at 6 pm on Tuesday, September 18; 7 pm on Wednesday, September 19; and 5 pm on Thursday, September 20.

An International Visitors Center will operate all three days of the show at the Civic Auditorium. The Center will provide foreign attendees with interpreters, registration, and hospitality facilities.

Shuttle Service

Peninsula buses will operate between the Cabana Hotel in Palo Alto and the Civic Auditorium at 20-min intervals beginning 30 min before Wescon opens, and ending 30 min after the show closes. Round trip fare will be $3. Free shuttles will run continuously between the St Francis and Hyatt on Union Square Hotels and the Civic Auditorium.

Social

"Elegant San Francisco," the Wescon/79 All-Industry Reception, will feature fountains, flowers, music, and costumes of the early 1900s. The reception will be held in the Grand Ballroom of the St Francis Hotel, and there will be a wine, fruit, and cheese buffet, barons of beef, hors d'oeuvres, and cocktails. Tickets for the reception will be $12 and include refreshments and cocktails.

Registration

Advance registration is available before August 31 for $4. In order to expedite registration at the door, the IEEE member/nonmember differentiation has been waived, and all registration will be $5. For more information, contact William C. Weber, Jr, 999 N Sepulveda Blvd, El Segundo, CA 90245, tel: 213/772-2965.

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North Star Horizon OEM Prices (includes 32K RAM, one parallel and two serial I/O ports),* assembled, burned-in and tested:

Horizon-1-32K-Q	$1645
Horizon-2-32K-Q	$2060
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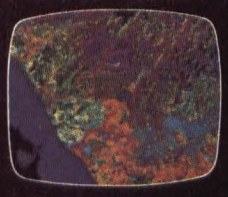
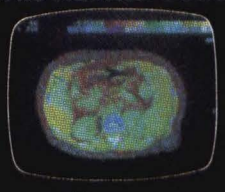


The Ramtek 9000 Series Display Controller. Four models. Total modularity. Buy just what you need; add to it at any time. The high-performance family. The industry standard in imaging and graphics raster scan color.

The Ramtek 9050 Series Display Controller. Four models. The most popular elements of the 9000 Series are here packaged for economy. All are software compatible with the 9000, have expandable memory and interactive capabilities.



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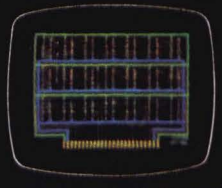

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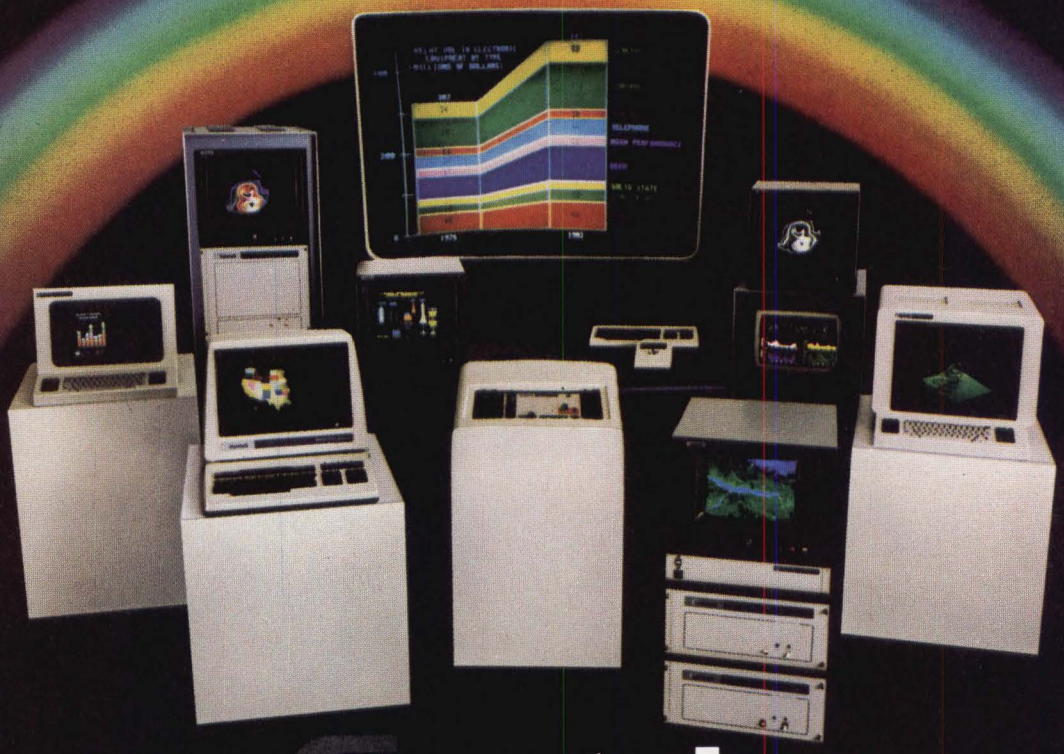

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GUIDELINES FOR DESIGNING BATTERY BACKUP CIRCUITS FOR CMOS RAMS

Providing battery backup for nonvolatile memory arrays using CMOS RAMs requires careful consideration of battery type and method of switching array power from system to standby voltage

Dennis C. Young Harris Semiconductor, Melbourne, Florida

Because of expanded availability and decreasing cost, complementary metal oxide semiconductor static random access memories are being designed into increasing numbers of large and small computer equipment and systems. Their inherent low power requirements (typically, 5 to 50 μW for 1024-bit devices), low data retention supply voltage (normally, 2 Vdc), and wide operating temperature range (−55 to 125 °C) adapt them to many uses. However, nonvolatile memory arrays remain the major application. In conjunction with a small battery mounted on the memory card, the memory array can maintain data contents for prolonged time periods in the event of primary power failure. Design techniques for switching battery backup into memory systems are relatively straightforward if basic guidelines are followed.

Design Principles

Two principal memory array design requirements for battery backup are low power dissipation for maximum battery life and spurious signal rejection to prevent data alteration or destruction. Since complementary metal oxide semiconductor (CMOS) memories have high impedance inputs, they cannot be left in an undefined or floating condition during the backup mode. As an example, consider an input buffer (Fig 1) with a protection network consisting of a resistor (R1) and two diodes (D1 and D2). If the buffer is allowed to float, the input will drift toward a voltage value midway between supply voltage V_{CC} and ground (V_{SS}); this voltage will turn on both p-channel (P1) and n-channel (N1) devices, forming a dc path from V_{CC} to ground.

CMOS logic achieves low power dissipation through its use of complementary structures. When one transistor in a buffer is turned on in a valid logic state, the other transistor in the buffer is turned off, thereby preventing current flow from V_{CC} to ground. If every input to the random access memory (RAM) is allowed to float, standby current (I_{CC}) can approach a value of 1 mA. To eliminate this increased current, the inputs must be maintained at CMOS V_{CC} or ground during the backup mode, assuring that only one of the input transistors is

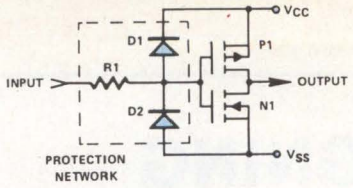
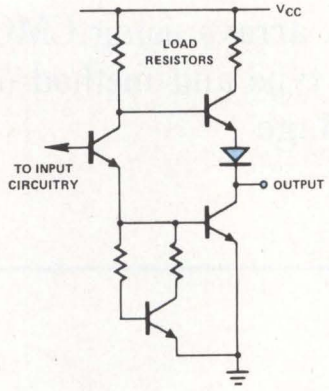
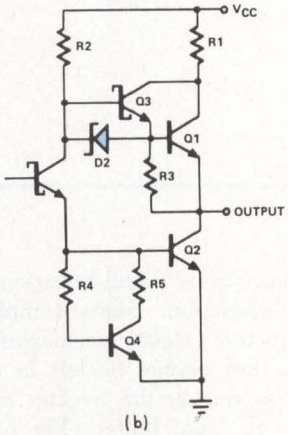


Fig 1 Input buffer protection network. All inputs to CMOS static RAMs pass through high impedance input buffer protection network. Components R1, D1, and D2 protect P1 and N1 gates from electrostatic damage by clamping overvoltage transients



(a)



(b)

Fig 2 Typical outputs for TTL devices. For standard, low power, and high speed TTL (a), output of gate will be at high impedance if V_{CC} is lost. Consequently, all output junctions will be reverse biased, allowing pullup resistor to be connected to CMOS V_{CC}. For low power Schottky TTL buffer (b), circuit will be at low impedance to ground if system V_{CC} is lost. Consequently, output cannot be pulled up to CMOS V_{CC} by resistor. If attempted, components R3 and D1 will clamp voltage to diode drop above ground

conducting. The off transistor allows only junction leakage current to flow.

Two methods of assuring proper input buffer action are the use of pullup resistors to CMOS V_{CC} or pulldown resistors to ground. For address and data inputs the choice is arbitrary; however, the enable ($\overline{E}$) input, which synchronizes the RAM's operation, must be maintained at CMOS V_{CC} during the backup period so that the memory is completely disabled. Some memories contain 3-state output buffers that are controlled only by a chip select ($\overline{S}$) signal due to the inclusion of onchip data latches. An appropriate chip select must be held at its disabled level to place the outputs in the 3-state mode. In this mode, outputs will not source current into the remainder of the system. During battery backup, the important design requisites are that the outputs are in the 3-state mode and that the memory chip is disabled. The write input ($\overline{W}$), which enables writing data into a specific RAM location, need not be held high if it can be assured that the enable ($\overline{E}$) signal will not be low simultaneously. Usually a write pin is connected common to all RAMs in an array. This pin can be held high with little additional circuitry and gives added protection against erroneous write signals during transistions into and out of the backup mode.

Driver Logic

Which family of logic devices drive the inputs to CMOS memory determines the particular interface method employed. When the V_{CC} supply is lost, the outputs of various logic families behave differently. Typical outputs for standard transistor-transistor logic (TTL), high speed TTL, or low power TTL gates, and for low power Schottky TTL devices are shown in Fig 2. For standard, high speed, and low power TTL type devices, if V_{CC} to the gate is lost by either a power failure or a short or open circuit, the output will be at high impedance. Pullup resistors to CMOS V_{CC} should be used to maintain proper VIH (input high voltage) levels during the backup period to prevent excessive power dissipation. Since leakage levels through the TTL devices are minimal, pullup resistors should be in the 10k- to 47k-Ω range.

Output of a typical low power Schottky TTL device differs from standard TTL; regardless of whether the gate V_{CC} supply goes to ground or opens, the output is a low impedance path to ground. This characteristic makes low power Schottky TTL devices undesirable for driving lines which must be held at CMOS V_{CC} during the backup period. However, for driving lines where the choice of logic level is arbitrary, such as address lines, low power Schottky is an excellent choice. Since the outputs are low impedances to ground, pullup or pulldown resistors can be eliminated. The low power Schottky device will sufficiently pull the address input line to ground potential. However, some low power Schottky devices with 3-state outputs do not exhibit this behavior; therefore, pullup or pulldown resistors must be used. Each type of memory driver should be so characterized before it is used in a circuit design.

Many microprocessor and related support circuits are fabricated with n-channel MOS (NMOS) technology. These

devices are often used to drive CMOS memories directly. The outputs of these devices go to a high impedance state when V_{CC} is lost; therefore, pullup or pulldown resistors must be installed.

If CMOS logic is used to drive memory lines, power should be maintained to these CMOS drivers during the backup period. Pullup or pulldown resistors are not required on these memory lines. However, the inputs to the CMOS driver logic cannot be allowed to float; otherwise, excessive I_{CC} current will flow. Appropriate methods should also be employed to assure that input voltage levels are defined at CMOS V_{CC} or ground potential. If power is not maintained to all CMOS interface logic, the outputs cannot be pulled up to CMOS V_{CC}. Therefore, the output will clamp at a diode voltage drop because the substrate will become forward biased (Fig 3).

Other types of devices, such as open collector TTL and open drain CMOS, can also drive the inputs to CMOS memories. Each logic family has a different set of characteristics which must be examined closely when designing the interface. Most manufacturers furnish typical schematics of their output buffers. Design characterization and simulation are probably the best methods of analysis. Designers should be aware that multisourced devices from different manufacturers may not have identical characteristics.

Battery Selection

After the interface section has been designed, the proper method of switching V_{CC} and backup power as well as battery type and discharge characteristics, should be examined. Other battery parameters, such as temperature range and current capacity (ampere-hours), and including battery backup usage (daily or only during power outages), also should be checked. Thorough parameter evaluation determines the choice of battery.

There are two classifications of backup batteries—secondary and primary. Secondary cells may be reused or recharged, since their chemical energy reaction is reversible. Batteries in this classification include sealed lead-acid, lead-calcium, or nickel-cadmium cells. Primary cells are used until discharged; then they are replaced since the chemical energy reaction is nonreversible. Primary type batteries contain either carbon-zinc, alkaline, mercury, or lithium cells.

Other types of secondary batteries are available, such as Gell* cells and sealed lead-acid cells. The Gell cell electrolyte is not a liquid but is of a gelatinous composition. This avoids spillage and permits mounting in any physical position. However, these batteries are too large for printed circuit board installation. They also have a wide operating temperature range, −60 to 60 °C, and their very low internal resistance allows high discharge rates. Gell cells are normally used where large amounts of current are required (typically, in the hundreds of milliamperes range), such as in portable equipment. Sealed lead-acid batteries have similar characteristics.

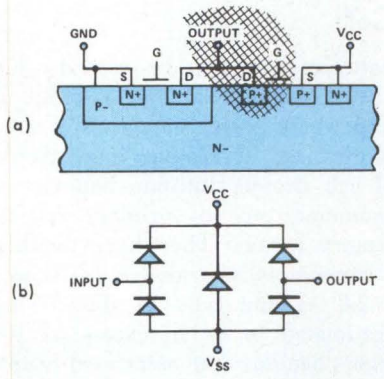


Fig 3 CMOS interface logic outputs. Output of CMOS device (a) cannot be held high if V_{CC} is at ground. P^+ channel drain in shaded area will become diode anode with substrate as cathode. This action will clamp voltage at diode drop above ground. In equivalent circuit of CMOS device (b), note that diode between output and V_{CC} is identical to diode in (a)

Secondary Cells

Nickel-cadmium batteries are ideal for CMOS memory arrays in portable nonvolatile equipment applications. Their small size (usually, AA type) allows direct placement on the memory card. In addition, they possess high energy density, and their voltage discharge characteristic is flat over the life of the cell (Fig 4). Because the output of a nickel-cadmium cell is 1.2 V, it is recommended that a 2- or 3-cell battery be used as the standby V_{CC} supply (2.4 to 3.6 V) to allow for voltage drops in the isolation circuits and for cell discharge. Nickel-cadmium batteries have a self-discharge leakage current that must be included in discharge calculations. This leakage value depends on temperature, and can range from less than 1% per day at room temperature to as much as 8% per day at 50 °C. Therefore, a nickel-cadmium cell should be fully charged before insertion to ensure that it has the capacity to maintain memory status if a power outage occurs before the power system has had sufficient time to charge the battery. To avoid cell degradation after installation, the cell should be continuously charged with a constant current source. A charge rate of 0.1 I_C can be indefinitely applied without cell damage. For example, if the capacity (or I_C rating) of a cell is 100 mA-h, 10 mA is the continuous charge current. This current can be obtained from the main power supply and should maintain the battery at full charge. A simple charge circuit only needs a series resistor (Fig 5). The resistance value of R(charge) is calculated so that the battery is charged at a constant current of 0.1 I_C.

Depending on the current required by the memory array, the voltage drop across the charging resistor in the backup mode may become significant. In this case,

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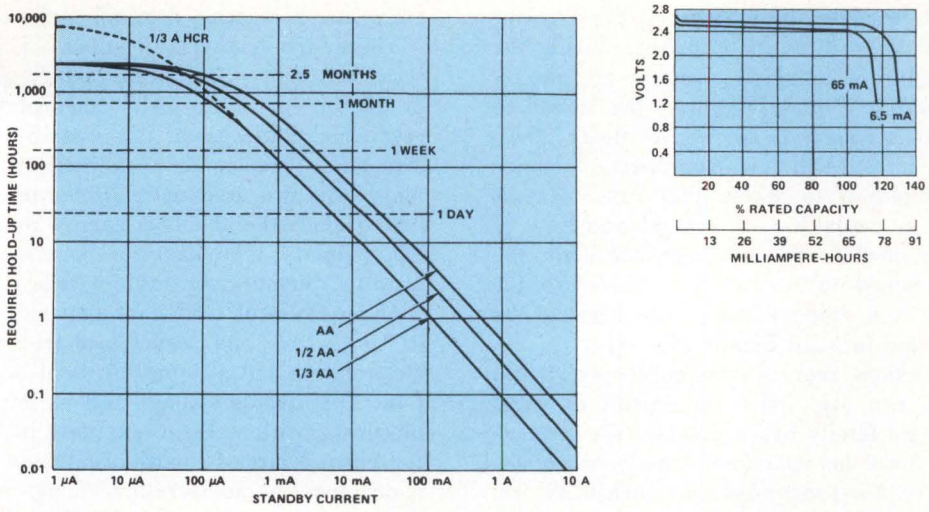

Fig 4 Voltage discharge characteristics for nickel-cadmium batteries. Discharge voltage (a) is constant until rated (100%) capacity has been exceeded (65 mA-h). Then, discharge voltage decreases rapidly, depending upon current drain. Approximate holdup or data retention times (b) for AA, ½ AA, and ⅓ AA type batteries at specific discharge rates. For example, 2.4-V AA battery maintains data in 100-μA memory array for more than 2.5 mo

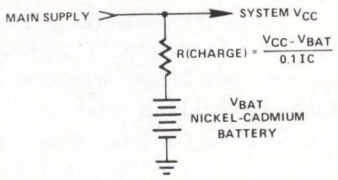

Fig 5 Simple charge circuit. Resistor [R(charge)] maintains nickel-cadmium battery at full charge by continually trickle-charging battery when system V_{cc} is available. This circuit eliminates special charger designs

a diode may be placed in parallel with the resistor to assure that the voltage drop does not exceed one forward diode drop.

Primary Cells

Primary batteries can also be used to supply backup power to CMOS memory arrays. Usually primary cells are employed where power outages are rare. These cells are usually replaced at regular intervals depending on the type of cell chosen. Lithium batteries are probably the most common type of primary cell used in nonvolatile memory arrays. They have the highest energy density of commercially available batteries, a high cell voltage of 2.8 V, and type AA dimensions. Shelf life has been estimated to be in excess of 10 years. The self-discharge phenomenom associated with other types of batteries does not apply to lithium types. Usable temperature range is very wide, −65 to 165 °F (−54 to 74 °C). When stored at temperatures as high as 54 °C, 75% capacity is retained after 8 years. At temperatures as low as −40 °C, the lithium battery can still deliver 60% of its room temperature capacity.

The lithium battery cannot be recharged and any recharge attempt will shorten the life of the battery. If a higher than cell voltage is applied to a lithium battery, severe damage can result, and the battery must be replaced. Connection of a primary battery to the memory system must ensure that no charge current can flow into the battery from the main system supply. An isolat-

ing diode, relay, or transistor should be used. A design point of concern is that the voltage of the battery must be at least 2.0 V plus the D1 diode drop to assure minimum data retention voltage to the CMOS RAMs. Low leakage diodes should be used to minimize battery charging and to prolong battery life.

Other types of primary batteries which can be used are silver oxide, alkaline, and mercury. Silver oxide and mercury batteries are employed where only small arrays need to be protected. Examples are 1- and 2-RAM arrays used as scratchpad memories.

Supply Isolation

A simple method for isolating the main supply from the backup supply is to place either a silicon or germanium diode in series with the CMOS V_{CC} supply line (Fig 6). A germanium diode has a much lower forward voltage drop (0.2 V) than a silicon diode (0.7 V), but the reverse biased leakage current of the germanium diode (1 μA) is much higher than that of the silicon diode (10 nA). When system power fails, the isolation diode reverse biases and isolates the CMOS V_{CC} from the remainder of the system.

The ideal operating condition for a CMOS memory array is for CMOS V_{CC} to match system V_{CC} when not in the backup mode. Care must be taken to avoid design conditions where the input high voltage to the CMOS array may rise above CMOS V_{CC}. This condition will cause parasitic bipolar devices in the CMOS memory to switch on and cause a high I_{CC} value. Design measures can be implemented to avoid such conditions. If open collector devices, or devices requiring a pullup resistor, are used to drive the CMOS array, the pullup resistor should be connected to CMOS V_{CC} rather than to system V_{CC}. Decoupling capacitors of 0.01 μF/device should be adequate to maintain a steady V_{CC} during switching transients. Overshoot and undershoot on signal input lines to the CMOS array should be minimized or confined within the limits of CMOS V_{CC} +0.3 V, and V_{SS} −0.3 V.

A simple design method for tracking supplies requires only one additional component (Fig 7). By inserting a diode in series with the system V_{CC} and increasing the main supply voltage to 5.7 V, both system V_{CC} and CMOS V_{CC} are identical when in the operating mode.

Another method, which requires more components, uses a saturable pnp transistor (Q1) as the isolation element (Fig 8). If properly chosen to match the current requirements of the CMOS array, the transistor saturation (V_{sat}) voltage may be as low as 200 mV. This value drives the supply mismatch to a lower value than when using only the single diode.

On-card voltage regulators make matching supplies relatively simple [Fig 9(a)], because each regulator can be individually adjusted. A 3-terminal voltage regulator is used in the examples, but more elaborate schemes employing interlocking supplies may be used. If multiple supplies are available on the memory card, the isolation method shown in Fig 9(b) can be used. A Zener diode (CR1) is included to clamp both TTL and CMOS V_{CC} in

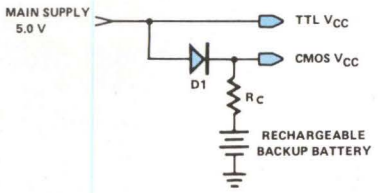

Fig 6 Single-diode isolation for backup battery. Diode D1, inserted in series with main supply becomes reverse biased when main supply fails, isolating CMOS V_{CC} from remainder of system

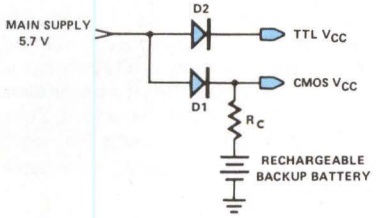

Fig 7 Double-diode isolation for backup battery. For small systems requiring less than 1-A TTL current, second diode (D2) is included in circuit of Fig 6 to match TTL V_{CC} and CMOS V_{CC}

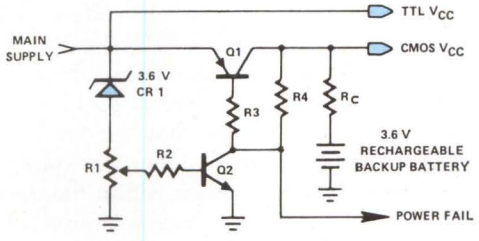

Fig 8 Transistor based isolation circuit. When pnp pass transistor (Q1) is used for isolation, voltage at which transistor conducts should closely match battery voltage to ensure that input voltages from TTL circuit are not greater than CMOS V_{CC}

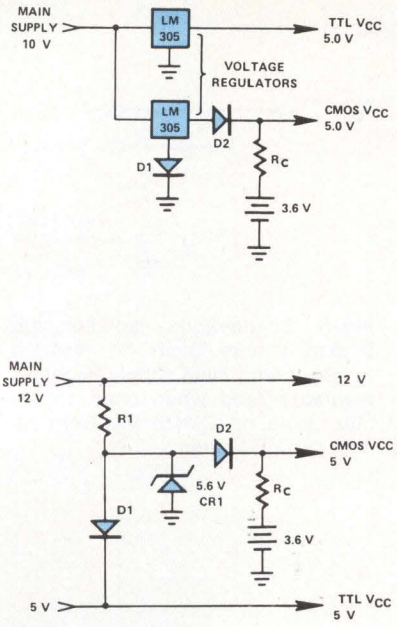

Fig 9 On-card voltage regulator circuits. Dual regulators (a) simplify matching of supply voltages by allowing each voltage to be individually adjusted. Resistor and a Zener diode form simple isolator (b), which minimizes parts count and saves cost

case the 5-V supply opens, rather than going to ground. This ensures that a maximum value of 5 V will be applied to the CMOS and TTL supplies.

If perfect matching of the supplies is required, a relay may be used as the pass element (Fig 10). The normally open relay is powered by the main supply. When the relay is closed, the main supply and CMOS V_{CC} are matched. When the main TTL supply voltage is lost, the relay contacts will open and totally isolate the CMOS array from the remainder of the system. Since the battery is always in the circuit, there is no lapse in power to the CMOS array. To assure that the relay opens as quickly as possible when the main supply voltage begins to decrease, the R-C circuit shown within the dotted lines can be added. In this case, the current required to hold the relay in the closed position is much less than that required to make it close from the open position. The parallel R-C combination will supply enough initial current to pull in the relay, and the steady-state condition will reduce the current to a lesser value than if the relay coil were powered directly.

Another isolation method uses single-pole, double-throw (type C) relay switches between main and battery standby power [Fig 10(b)]. As before, the coil—powered by the main supply—connects CMOS V_{CC} to system V_{CC}. Since the lithium battery is totally isolated, maximum cell life is assured. When the main supply is lost, the relay switches and connects the battery to CMOS V_{CC}. Capacitor C1 is chosen such that voltage will be applied to the array during switching. An approximate value for this capacitor can be calculated using

$$C1 = \frac{(I_{CCSB})\ (s)\ (10)}{\text{Initial } V_{CC}} = \frac{Q}{V} \quad F/V$$

where I_{CCSB} is the total current required by the array, s is the time duration of the switchover, and the factor of 10 assures that voltage drop during switchover is less than 10% of the original value. A low leakage tantalum capacitor is recommended, since electrolytic capacitors have relatively high leakage currents at room temperature that increase with temperature, and could become significant in small 2-device arrays.

A nonvolatile 8k-word x 8-bit RAM array design (Fig 11), for use with an 8080 microprocessor based system, employs all CMOS logic with power from the backup battery. Pullup resistors are included on all address and data interface lines to the CMOS array. By including these resistors, the memory card can be removed from the system and will continue to maintain data at low power dissipation. If the card is to be inserted while the system supply is powered up, the edge card connector should be configured as shown in Fig 12. Assuming a leakage current of 1-μA standby supply current (I_{CCSB}) for each RAM device at 25 °C, the card should maintain data for 5 years when powered from a 1-A-h lithium nonrechargeable backup battery.

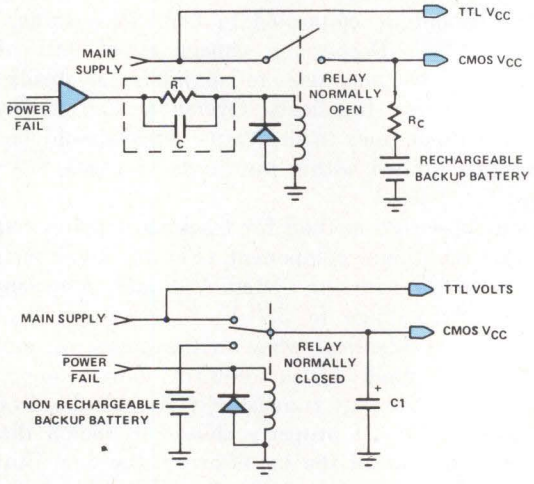

Fig 10 Relay based isolation circuits. Normally open relay (a) completely isolates CMOS V_{CC} from main TTL supply when power fails. In operating mode, all supply voltages will match. Single-pole, double-throw relay (b) is used effectively with nonrechargeable backup batteries. Battery is isolated from circuit during normal power by open relay contacts. Capacitor C1 maintains voltage to CMOS array during relay switching to backup mode

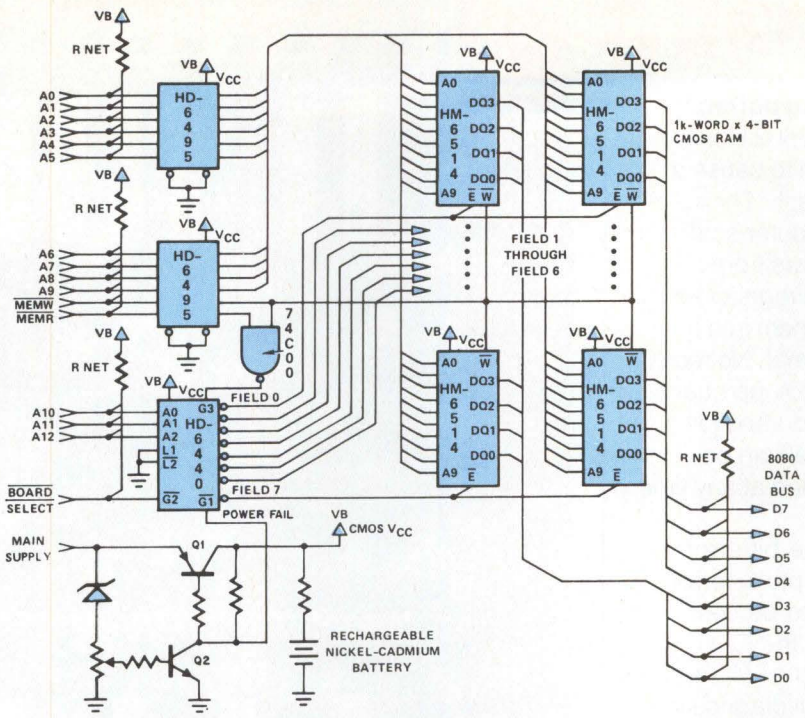

Fig 11 Typical CMOS static RAM array. 8k-word x 8-bit CMOS array typically dissipates only 100 μW in backup mode. Battery backup circuit (Q1 and Q2) isolates system V_{CC} from CMOS V_{CC} during system power loss and generates power-fail signal to disable memory array. Power is maintained to CMOS array by onboard nickel-cadmium battery

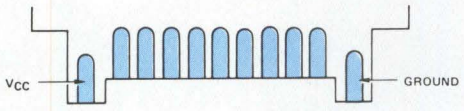

Fig 12 Edge card connector design. By extending physical length of V_{CC} and ground pins, power connections are made first, prior to any of other input pins, to avoid latchup problems

Summary

CMOS static RAMs can benefit memory designers by reducing overall system power requirements in the active and standby modes. Lower power dissipation also relates to cooler operating temperatures. Cooler operating temperatures translate into higher system reliability and higher packing densities. Considering these factors, CMOS static RAMs have become very economical.

Extremely low standby currents in the backup mode allow very small backup batteries to be mounted directly on memory cards. Previous nonvolatile memory arrays, such as core and electrically alterable read only memory, required additional support circuits, larger power supplies, and increased space. These requirements prevented their use in many applications, such as autotelephone dialers and calculators. Present nonvolatile memory arrays can be included in such devices with CMOS RAMs and small backup batteries.

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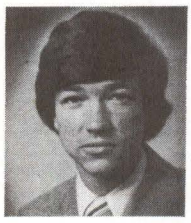

Dennis Young is a member of the memory applications group at Harris Semiconductor Products Division where his responsibilities include applications support for bipolar and CMOS memories. Mr Young holds a BSEE degree from North Carolina State University.

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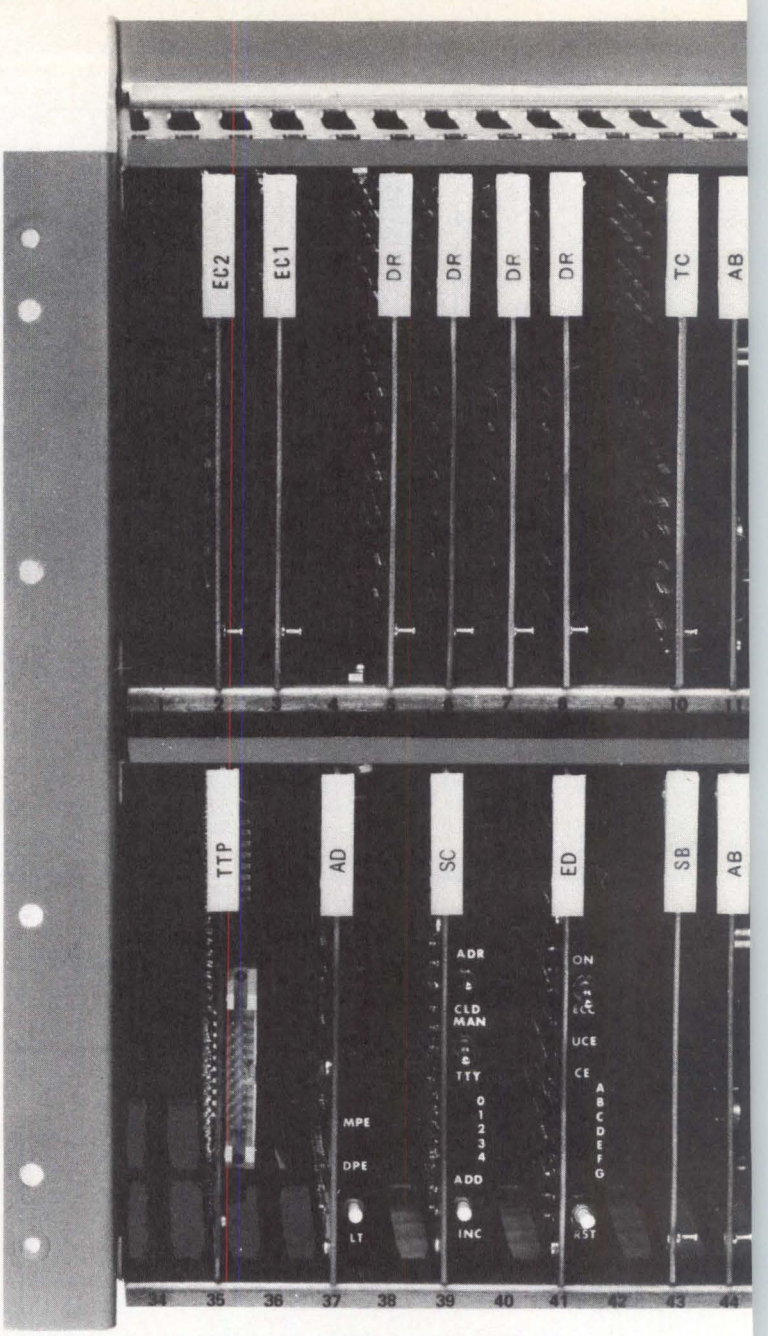

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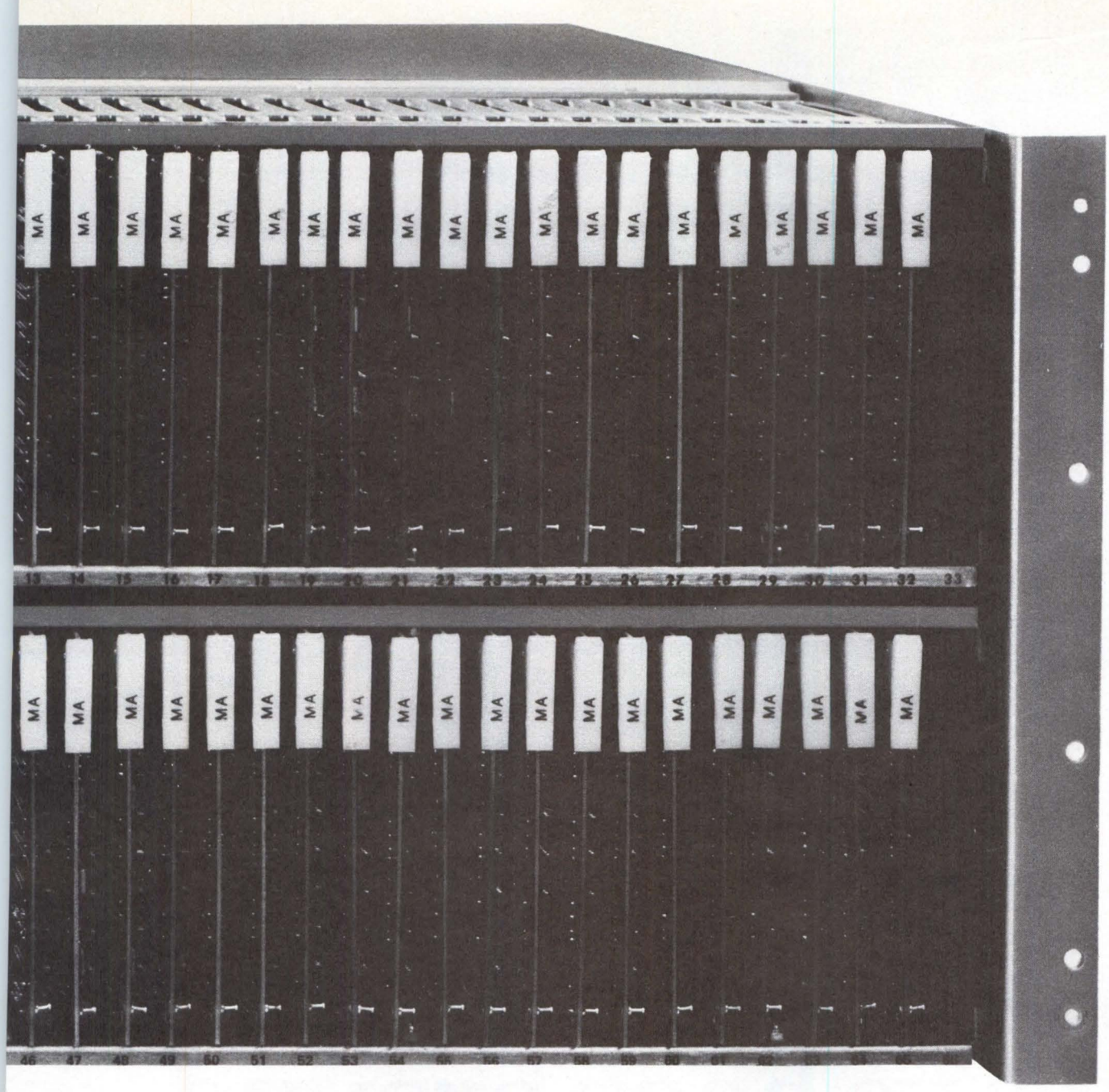

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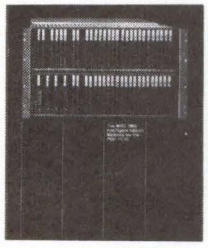

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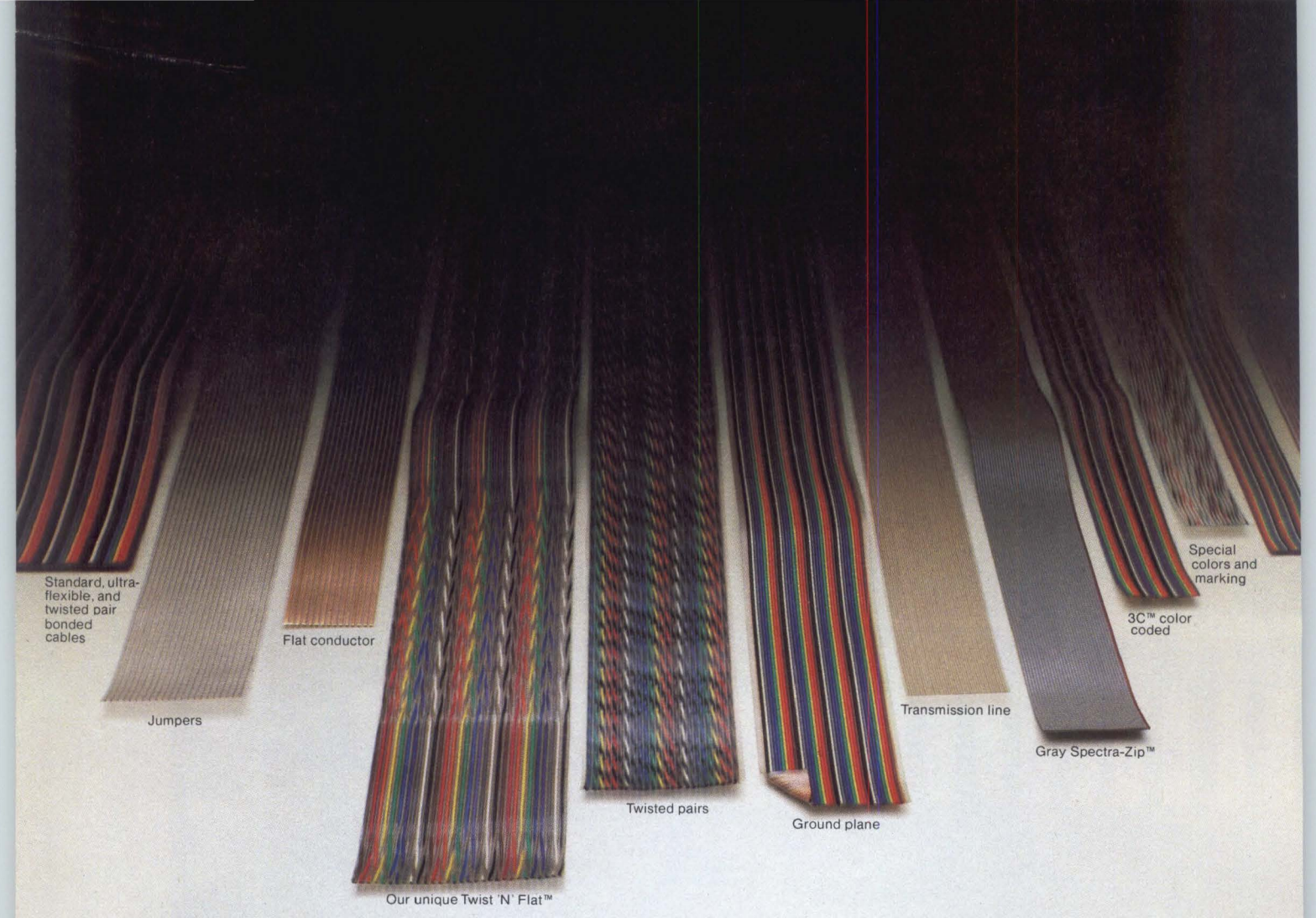

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Software designed subroutines for single-chip microcomputers, serial communication, arithmetic processing, and binary/BCD conversion stress maximum useability rather than minimum code size or fast execution time

Lionel Smith Intel Corporation, Santa Clara, California

Two main application areas for high performance single-chip microcomputers concern mechanism control and arithmetic processing. Mechanism control applications involve the use of a microcomputer to govern a mechanical device or system, such as a line printer. Arithmetic processing applications deal with the manipulation of information, either for a closed loop control system or for a visual display; examples include a digital voltmeter or a proportional, integral, and differential servo controller.

Typical program subroutines, developed in detail, demonstrate performance requirements in these two areas. Implementation of full-duplex serial input/output (I/O) communications is a typical device controller application. Simple mathematical routines, comprising binary multiplication and division, binary to binary coded decimal (BCD) conversion, and BCD to binary conversion, are used as examples of arithmetic processing. Algorithms for these programs are expressed in a machine independent design language which allows easy translation to another environment.

Full-Duplex Serial Communication

Serial communication is a common requirement in a microprocessor based system. Although this usage has been partially due to the necessity of connecting a terminal to the microprocessor based system for program generation and debug, the main impetus has been that systems which rely on serial communication (such as intelligent terminals) are an important application area for microprocessors. To interface a serial link to a multichip microcomputer,[1] the design is relatively straightforward; specialized I/O chips are readily available which will provide the required serial interface. When it is necessary to interface to a single-chip microcomputer, however, the design becomes more intricate.

Some microcomputers have a complete built-in bus interface which allows the simple connection of a universal synchronous/asynchronous receiver/transmitter (USART) to the processor chip. Other single-chip microcomputers, although lacking such a bus, can be connected to a USART with various hardware and software constructs.[2] The difficulty, however, is more economical than technical; these same peripheral chips which are cost-effective when coupled to a multichip microcomputer have a significant cost impact on a single-chip microcomputer system. The high speed of a microcomputer, however, makes it feasible to implement a serial link under software control with no hardware requirements beyond the I/O ports already resident on the microcomputer.

There are many published algorithms which implement half-duplex serial communication under software control.[3] Full-duplex operation is more complicated, since

TABLE 1

Start of Receive Routine

```
IF RECEIVE FLAG = 0 THEN
  IF SERIAL INPUT = SPACE THEN
    RECEIVE FLAG: = 1
    BYTE FINISHED FLAG: = 0
  ENDIF
ELSE  SINCE RECEIVE FLAG = 1 THEN
  IF SYNC FLAG = 0 THEN
    IF SERIAL INPUT = SPACE THEN
      SYNC FLAG: = 1
      DATA: = 80H
      SAMPLE CNTR: = 4
    ELSE  SINCE SERIAL INPUT = MARK THEN
      RECEIVE FLAG: = 0
    ENDIF
  ELSE  SINCE SYNC FLAG = 1 THEN
    SAMPLE COUNTER: = SAMPLE COUNTER − 1
    IF SAMPLE COUNTER = 0 THEN
      SAMPLE COUNTER: = 4
      IF BYTE FINISHED FLAG = 0 THEN
        CARRY: = SERIAL INPUT
        SHIFT DATA RIGHT WITH CARRY
        IF CARRY = 1 THEN
          OKDATA: = DATA
          IF DATA READY FLAG = 0 THEN
            BYTE FINISHED FLAG = 1
          ELSE
            BYTE FINISHED FLAG: = 1
            OVERRUN FLAG: = 1
          ENDIF
        ENDIF
      ELSE  SINCE BYTE FINISHED FLAG = 1 THEN
        IF SERIAL INPUT = MARK THEN
          DATA READY FLAG: = 1
        ELSE  SINCE SERIAL INPUT = SPACE THEN
          ERROR FLAG: = 1
        ENDIF
        RECEIVE FLAG: = 0
        SYNC FLAG: = 0
      ENDIF
    ENDIF
  ENDIF
ENDIF
```

it requires the receive and transmit processes to operate concurrently. The design problem is made more severe if it is necessary for some other process to operate while serial communication is occurring. Scanning a keypad or 7-segment display is a common operation of a single-chip microcomputer based system which might have to occur concurrently with the serial receive/transmit process. An algorithm can implement full-duplex serial communication concurrently with other tasks. Design goals include 2400-baud, full-duplex, serial communication while utilizing not more than 50% of the available processing power of the microcomputer.

The format used for most asynchronous communication consists of eight data bits with a leading start bit and one or more trailing stop bits. The start bit establishes synchronization between the receiver and transmitter. The stop bits ensure that the receiver will be ready for synchronization when the next start bit occurs. Two stop bits are normally used for 110-baud communication and one stop bit for higher rates.

The algorithm used for reception of serial data (Table 1) directs the onboard timer of the microcomputer to establish a sampling period of four times the desired baud rate. For 2400-baud operation, a crystal controlled frequency of 9.216 MHz is derived from $f = 480N(2400)$ (4), where 480 = factor by which the crystal frequency is divided within the processor to obtain the basic interrupt rate; 2400 = desired baud rate; 4 = required number of samples/bit time; and N = value loaded into the timer when it overflows. The value of N is selected as 2 (resulting in f = 9.216 MHz) so that the operating frequency of the microcomputer (8049) could be as high as possible without exceeding the maximum frequency specification (11 MHz).

The timer interrupt service routine always loads the timer with a constant value. In effect, the timer generates an independent time base of four times the required baud rate. This time is freerunning and is never modified by either receive or transmit programs, thus allowing both to access the same timer. Routines which do other time dependent tasks (such as scanning keyboards) can also be called periodically at some fixed multiple of the basic time unit.

The receive algorithm uses this basic clock plus several flags to process serial input data. The receive flag is set whenever the program is in the process of receiving a character; the sync flag is set when the center of the start bit has been checked and found to be a space. (If a mark is detected at this point, the receiver process has been triggered by a noise pulse; then the program clears the receive flag and returns to the idle state.) When the program detects synchronization, it loads variable DATA with 80H and starts sampling the serial line every four counts. As data are received, they are right-shifted into variable DATA; after eight bits have been received, the initial bit set into DATA results in a carry out. At this point, the program transfers all eight bits to variable OKDATA and sets the byte finished flag so that, on the next sample, the routine will test for a valid stop bit instead of shifting in data. If this test is successful, the data ready flag will be set to indicate that data are available to the main program. If the test is unsuccessful, the error flag will be set.

The transmit algorithm (Table 2) is executed immediately following the receive routine. This algorithm divides the freerunning clock down and transmits a bit every fourth clock interval. Variable tick counter performs the division. The transmitting flag indicates when a character transmission is in progress and when the start bit should be sent. Tick counter determines when to send the next bit (tick counter modulo 4 = 0) and when the stop bits should be sent (tick counter = 9*4). After the transmit routine finishes, any other timer based

TABLE 2

Start of Transmit Routine

```
TICK COUNTER: = TICK COUNTER + 1
IF TICK COUNTER MOD 4 = 0 THEN
  IF TRANSMITTING FLAG = 1 THEN
    IF TICK COUNTER = 00 1010 00 BINARY THEN
      TRANSMITTING FLAG: = 0
    ELSE  IF TICK COUNTER = 00 1001 00 BINARY THEN
      SEND END MARK
      TRANSMITTING FLAG: = 0
    ELSE  SINCE TICK COUNTER < > THE ABOVE COUNT THEN
      SEND NEXT BIT
    ENDIF
  ELSE  SINCE TRANSMITTING FLAG = 0 THEN
    IF TRANSMIT REQUEST FLAG = 1 THEN
      XMTBYT: = NXTBYT
      TRANSMIT REQUEST FLAG: = 0
      TRANSMITTING FLAG: = 1
      TICK COUNTER: = 0
      SEND SYNC BIT (SPACE)
    ENDIF
  ENDIF
ENDIF
```

routines, such as a keyboard/display scanner or a real-time clock, can be executed.

Examination of the receive and transmit routines* reveals that the bulk of the operations performed are involved in either testing or setting flags used to define the current state of the process, typical of many mechanism control applications. The 8049 supports this type of operation with the ability to set or clear any bit (or combination of bits) in the accumulator with a single 2-byte instruction. Likewise, any bit in the accumulator can be tested by a 2-byte conditional jump instruction. The following sequence of 2-byte instructions, for example, will clear bits 0 and 1, set bits 4 and 5, and then jump if bit 6 is set.

```
ANL   A,#NOT(00000011B)   ; LOGICAL AND OUT BITS 1
                          ; AND 0
ORL   A,#00110000B        ; LOGICAL OR IN THE SET
                          ; BIT PATTERN
JB6   THERE               ; BRANCH IF ACC[6] IS A
                          ; LOGIC 1
```

Arithmetic Algorithms

The routines chosen to illustrate typical arithmetic processing are multiplication, division, conversion of binary to BCD, and conversion of BCD to binary. Algorithms that implement these operations are shown in Tables 3, 4, 5, and 6, respectively. Examination of these algorithms reveals that they all follow a pattern of a series of fairly simple arithmetic operations which are performed a fixed number of times. Repetition of these loops is efficiently handled by the DJNZ (decrement and JUMP on nonzero) instructions which allow the loop control to be handled in a single instruction.

Arithmetic operations in these algorithms, aside from those involving BCD digits, are easily handled by the normal 8-bit operations found in many microcomputers. Operations on BCD digits, which are not normally handled effectively by 8-bit microcomputers, are supported by the 8049 with three special instructions: SWAP A; XCHD A,Rj; and DA A. The purpose of these three instructions is to allow 8-bit operations to be utilized on BCD variables. The SWAP A instruction exchanges the upper four bits of the accumulator with the lower four bits. This exchange allows BCD digits to be efficiently packed and unpacked from 8-bit bytes. The second instruction (XCHD) also allows manipulation of 4-bit digits. This instruction allows the lower four bits of the accumulator to be exchanged with the lower four bits of the memory location pointed to by register R0 or R1. In addition to the obvious intent of allowing the program to move digits to and from memory, this instruction can be combined with the SWAP A instruction to implement efficient multiplication and division of BCD strings by 10. The third instruction for enhanced BCD operations, DA A, adjusts the accumulator following an addition so that the binary addition can produce BCD results. The power of each of these instructions is enhanced by the general XCH (exchange) instruction which interchanges the contents of the accumulator with either a register or a memory location. This instruction allows any instruction that operates on

*Complete programs for all discussed algorithms, as they are implemented in the instruction set of the 8049 microcomputer, are included in Intel's Application Note AP-49.

TABLE 3

8 by 8 Unsigned Multiply Routine

```
MPY8X8:
MULTIPLICAND [15 - 8]: = 0
COUNT: = 8
REPEAT
  IF MULTIPLICAND[0] = 0 THEN BEGIN
    MULTIPLICAND: = MULTIPLICAND/2
  ELSE
    MULTIPLICAND[15 - 8]: = MULTIPLICAND[15 - 8] + MULTIPLIER
    MULTIPLICAND: = MULTIPLICAND/2
  ENDIF
  COUNT: = COUNT - 1
UNTIL COUNT = 0
END MPY8X8
```

the accumulator to be extended to any variable by surrounding the instruction with XCH instructions. For example, the sequence

```
XCH   A,R3  ; EXCHANGE CONTENTS OF A AND R3
SWAP  A     ; SWAP NIBBLES IN ORIGINAL R3 DATA
XCH   A,R3  ; MOVE A AND R3 TO ORIGINAL POSITIONS
```

swaps the two digits in register R3 without disturbing the contents of the accumulator or requiring any temporary storage. This useful capability is used repeatedly in the coding of the described algorithms.

Multiply Algorithms

If the efficiency of the multiply algorithm either in terms of code size or execution time is important, it is necessary to be reasonably familiar with the multiplication process so that appropriate optimizations for the microcomputer being used can be made.

To understand how multiplication operates in the binary number system, consider the multiplication of two 4-bit operands A and B. The 1s and 0s in A and B represent the coefficients of two polynomials. The operation A × B can be represented as the following multiplication of polynomials:

$$\begin{array}{r} A3*2^3 + A2*2^2 + A1*2^1 + A0*2^0 \\ \times\ B3*2^3 + B2*2^2 + B1*2^1 + B0*2^0 \\ \hline + B0A3*2^3 + B0A2*2^2 + B0A1*2^1 + B0A0*2^0 \\ + B1A3*2^4 + B1A2*2^3 + B1A1*2^2 + B1A0*2^1 \\ + B2A3*2^5 + B2A2*2^4 + B2A1*2^3 + B2A0*2^2 \\ + B3A3*2^6 + B3A2*2^5 + B3A1*2^4 + B3A0*2^3 \end{array}$$

The sum of all these terms represents the product of A times B. The simplest multiply algorithm factors the above terms as

$$A*B = B0*(A)*2^0 + B1*(A)*2^1 + B2*(A)*2^2 + B3*(A)*2^3 \quad (1)$$

Since the coefficients of B (ie, B0, B1, B2, and B3) can only take on the binary values of 1 and 0, the sum of the products can be formed by a series of simple adds and multiplications by two. The simplest program implementation is

```
MULTIPLY:
  PRODUCT = 0
  IF B0 = 1   THEN PRODUCT: = PRODUCT + A
  IF B1 = 1   THEN PRODUCT: = PRODUCT + 2*A
  IF B2 = 1   THEN PRODUCT: = PRODUCT + 4*A
  IF B3 = 1   THEN PRODUCT: = PRODUCT + 8*A
END MULTIPLY
```

To conserve memory, the above straight line code is normally converted to the following loop:

```
MULTIPLY:
  PRODUCT: = 0
  COUNT: = 4
  REPEAT
    IF B[0] = 1 THEN PRODUCT: = PRODUCT + A ENDIF
    A: = 2*A
    B: = B/2
    COUNT: = COUNT - 1
  UNTIL COUNT = 0
END MULTIPLY
```

The repeated multiplication of A by two (which can be performed by a simple left shift) forms the terms 2*A, 4*A, and 8*A. Variable B is divided by two (performed by a simple right shift) so that the least significant bit can always be used to determine whether the addition should be executed during each pass through the loop. It is from these shifting and addition operations that the "shift and add" algorithm takes its common name.

However, the "shift and add" algorithm has two areas where efficiency will be lost if implemented in the manner shown. The first problem is that addition to the partial

product is double precision relative to the two operands. The other problem, which is also related to double precision operations, is that the A operand is double precision and that it must be left shifted; then the B operand must be right shifted. Examination of the longhand polynomial multiplication reveals that, although the partial product is indeed double precision, each addition performed is only single precision. It would be desirable to be able to shift the partial product as it is formed so that only single-precision additions are performed. This would be especially true if the partial product could be shifted into the B operand, since one bit of the partial product is formed during each pass through the loop and one bit of the B operand is vacated. To do this, however, it is necessary to modify the algorithm so that both shifts are of the same type. For example, factoring 2^4 from the right side of Eq (1) obtains

$$A*B = 2^4[B0*(A*2^{-4}) + B1*(A*2^{-3}) + B2*(A*2^{-2}) + B3*(A*2^{-1})] \quad (2)$$

This operation yields a term (within the brackets) which can be formed by right shifts and adds, and then multiplied by 2^4 to get the final result. The resulting algorithm, expanded to form an 8 by 8 multiplication, is shown in Table 3. Note that although the result is a full 16 bits, the algorithm only performs 8-bit additions and that only a single 16-bit shift operation is involved. This effectively reduces both the code space and the execution time for the routine.

Division Algorithms

To understand binary division, a 4-bit operation is used as an example. The following algorithm performs a 4 by 4 division:

```
DIVIDE:
  IF 16*DIVISOR > = DIVIDEND THEN
    SET OVERFLOW ERROR FLAG
  ELSE
    IF 8*DIVISOR > = DIVIDEND THEN
      QUOTIENT[3]: = 1
      DIVIDEND: = DIVIDEND - 8*DIVISOR
    ELSE
      QUOTIENT[3]: = 0
    ENDIF
    IF 4*DIVISOR > = DIVIDEND THEN
      QUOTIENT[2]: = 1
      DIVIDEND: = DIVIDEND - 4*DIVISOR
    ELSE
      QUOTIENT[2]: = 0
    ENDIF
    IF 2*DIVISOR > = DIVIDEND THEN
      QUOTIENT[1]: = 1
      DIVIDEND: = DIVIDEND - 2*DIVISOR
    ELSE
      QUOTIENT[1]: = 0
    ENDIF
    IF 1*DIVISOR > = DIVIDEND THEN
      QUOTIENT[0]: = 1
      DIVIDEND: = DIVIDEND - 1*DIVISOR
    ELSE
      QUOTIENT[0]: = 0
    ENDIF
  ENDIF
END DIVIDE
```

TABLE 4

16 by 8 Unsigned Division Routine

```
DIV16:
COUNT: = 8
DIVIDEND[15 - 8]: = DIVIDEND[15 - 8] - DIVISOR
IF BORROW = 0 THEN /* IT FITS*/
  SET OVERFLOW FLAG
ELSE
  RESTORE DIVIDEND
  REPEAT
    DIVIDEND: = DIVIDEND*2
    QUOTIENT: = QUOTIENT*2
    DIVIDEND[15 - 8]: = DIVIDEND[15 - 8] - DIVISOR
    IF BORROW = 1 THEN
      RESTORE DIVIDEND
    ELSE
      QUOTIENT[0]: = 1
    ENDIF
    COUNT: = COUNT - 1
  UNTIL COUNT = 0
  CLEAR OVERFLOW FLAG
ENDIF
ENDDIVIDE
```

The first test asks whether the divisor will fit into the dividend 16 times. If it does, the quotient cannot be expressed in only four bits; thus, an overflow error flag is set and the divide algorithm ends. If it does not overflow, the algorithm then proceeds to determine if eight times the divisor fits, then four times, etc. After each test, the algorithm either sets or clears the appropriate quotient bit and modifies the dividend. To demonstrate this algorithm, consider the binary divsion of 15 by 5:

```
   00001111   (15)
- 01010000   (16*5)
------------
              Does not fit—no overflow

   00001111   15
- 00101000   (8*5)
------------
              Does not fit—Quotient [3] = 0

   00001111   (15)
- 00010100   (4*5)
------------
              Does not fit—Quotient[2] = 0

   00001111   (15)
- 00001010   (2*5)
------------
   00000101   Does fit—Quotient[1] = 1

   00000101   (15 - 2*5)
- 00000101   (1*5)
------------
   00000000   Does fit—Quotient[0] = 1
```

The final result is Q = 0011, which is the binary equivalent of 3_{10}—the correct answer. Clearly, this algorithm can be converted to a loop and used to perform divisions. An examination of the procedure, however,

TABLE 5

Conversion of 16-Bit Binary Value to BCD

```
CONVERT_TO_BDC
BCDACC: = 0
COUNT: = 16
REPEAT
  BIN: = BIN*2
  BCD: = BCD*2 + CARRY
  IF CARRY FROM BCDACC GOTO ERROR EXIT
  COUNT: = COUNT − 1
UNTIL COUNT = 0
END CONVERT_TO_BCD
```

TABLE 6

Conversion of 6-Digit BCD Value to Binary

```
CONVERT_TO_BINARY
POINTER0: = POINTER0 + DIGITPAIR − 1
COUNT: = DIGITPAIR
BIN: = 0
REPEAT
  BIN: = BIN*10
  BIN: = BIN + MEM(R0) [7 − 4]
  BIN: = BIN*10
  BIN: = BIN + MEM(R0) [3 − 0]
  POINTER0: = POINTER0 − 1
  COUNT: = COUNT − 1
UNTIL COUNT = 0
END CONVERT_TO_BINARY
```

TABLE 7

Subroutine Execution Times

Subroutine	Bytes	8049 Execution Time (μs)
MPY8 (8 by 8 Multiply)	21	109
DIV16 (16 by 8 Division)	37	183 (min) 204 (max)
CONBCD (Binary to BCD Conversion)	36	733
CONBIN (BCD to Binary Conversion)	70	388

shows that it has the same problems as the original multiply algorithm.

The first problem is that double-precision operations are involved with both the comparison of the division with the dividend and the conditional subtraction. The second problem is that, as the quotient bits are derived, they must be shifted into a register. It would be desirable to shift them into the divisor register as they are generated, since the divisor register always gets shifted. Unfortunately, the quotient bits are derived most significant bits first; therefore, this method will form a mirror image of the quotient, which is not useful.

Both problems can be solved by observing that the algorithm presented for division will still work if both sides of all the "equations" involving the dividend are divided by 16. The looping algorithm would then be:

```
DIVIDE:
  QUOTIENT: = 0
  COUNT: = 4
  DIVIDEND: = DIVIDEND/16
  IF DIVISOR > = DIVIDEND THEN
    OVERFLOW FLAG: = 1
  ELSE
    REPEAT
      DIVIDEND: = DIVIDEND*2
      QUOTIENT: = QUOTIENT*2
      IF DIVISOR > = DIVIDEND THEN
        QUOTIENT: = QUOTIENT +
                    1 /*SET QUOTIENT[0]*/
        DIVIDEND: = DIVIDEND − DIVISOR
      ENDIF
      COUNT: = COUNT − 1
    UNTIL COUNT = 0
  ENDIF
END DIVIDE
```

When this algorithm is implemented on a microcomputer that does not have a direct compare instruction, the comparison is done by subtraction, and the inner loop of the algorithm is modified as

```
REPEAT
  DIVIDEND: = DIVIDEND*2
  QUOTIENT: = QUOTIENT*2
  DIVIDEND: = DIVIDEND − DIVISOR
  IF BORROW = 0 THEN
    QUOTIENT: = QUOTIENT + 1
  ELSE
    DIVIDEND: = DIVIDEND + DIVISOR
  ENDIF
  COUNT: = COUNT − 1
UNTIL COUNT = 0
```

Addition of the divisor to the dividend if the dividend goes negative restores the dividend to the value it had before the comparison. For this reason, the algorithm is called a restoring divide algorithm. The restoring algorithm is commonly used in software implemented divide routines. It is possible to speed up the division process at the expense of additional code by using a common hardware algorithm: nonrestoring division.

The nonrestoring algorithm is based on the observation that following an unsuccessful trial fit (ie, a subtrac-

tion with a negative result), the following operations are sequentially performed on the dividend:

```
DIVIDEND: = DIVIDEND + DIVISOR
DIVIDEND: = DIVIDEND*2
DIVIDEND: = DIVIDEND − DIVISOR
```

Simple algebraic manipulation reveals that these three lines can be replaced by two lines:

```
DIVIDEND: = 2*DIVIDEND
DIVIDEND: = DIVIDEND + DIVISOR
```

Instead of restoring the dividend following an unsuccessful compare, the nonrestoring algorithm simply performs a trial add instead of a trial subtract on the next pass through the loop. An implementation of this algorithm is shown in Table 4. This routine does an unsigned divide of a 16-bit quantity by an 8-bit quantity. Since the multiply algorithm of Table 3 generates a 16-bit result from the multiplication of two 8-bit operands, these two routines complement each other and can be used as part of more complex computations.[4]

Binary and BCD Conversions

Conversion of a binary value to a BCD number can be done with a straightforward algorithm:

```
CONVERT_TO_BCD:
  BCDACCUM: = 0
  COUNT: = PRECISION
  REPEAT
    BIN: = BIN*2
    BCD: = BCD*2 + CARRY
    COUNT: = COUNT − 1
  UNTIL COUNT = 0
END CONVERT_TO_BDC
```

Variable BCDACCUM is a BCD string used to accumulate the result; variable BIN is the binary number to be converted. "Precision" is a constant that gives the length, in binary bits, of BIN. For example, assume that BIN is a 16-bit value with the most significant bit set. On the first pass through the loop, the multiplication of BIN results in a carry, and this carry is added to variable BCD. On the remaining passes through the loop, BCD is multiplied by two, 15 times. The initial carry into BCD is multiplied by 2^{15}, or 32,768, which is the "value" of the most significant bit of BIN. The process repeats with each bit of BIN being introduced to BCDACCUM, and then being scaled up on successive passes through the loop. Table 5 shows the implementation of this algorithm.

Conversion of a BCD value to binary is essentially the same process as converting a binary value to BCD.

```
CONVERT_TO_BINARY
  BIN: = 0
  COUNT: = DIGNO
  REPEAT
    BCDACCUM: = BCDACCUM*10
    BIN: = 10*BIN + CARRY DIGIT
    COUNT: = COUNT − 1
  UNTIL COUNT = 0
END CONVERT_TO_BINARY
```

The only complexity is the two multiplications by 10. Variable BCDACCUM can be multiplied by 10 by shifting it left four places (one BCD digit). Variable BIN could be multiplied using the multiply algorithm already discussed, but it is usually more efficient to do this by making the following substitution:

$$BIN = 10*BIN = 2*5*BIN = 2*(2*2+1)*BIN \quad (3)$$

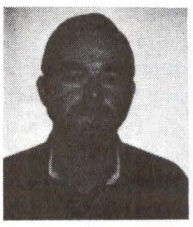
This equation implies that the value of 10*BIN can be generated by saving the value of BIN, and then shifting BIN two places left. After this shifting, the original value of BIN can be added to the new value of BIN (forming 5*BIN); then BIN can be multiplied by two. It is often possible to implement the multiplication of a value by a constant by using such techniques. Table 6 lists a routine that converts BCD values to binary. Protection has been added to detect BCD operands which, if converted, would yield binary values beyond the range of the result.

Conclusion

The capability of the 8049 single-chip microcomputer in both device control and arithmetic processing applications has been discussed. The algorithms have all been coded and tested. The central processing unit's loading required by the UART function running at 2400 baud is 42%. Table 7 summarizes the execution time performance of the arithmetic routines. All of these algorithms have been implemented with the intent of using them as viable realtime components in a larger program, rather than minimum code size or execution time. Errors, such as overflow, are detected and reported to the calling routine. The cost benefits of a single-chip microcomputer have been realized in many diverse application programs for frequently encountered design situations.[4]

References

1. Intel Corp, *MCS-48™ Family of Single-Chip Microcomputers, User's Manual,* Santa Clara, Calif, July 1978
2. Intel Corp, "Using the 8251 Universal Synchronous/Asynchronous Receiver/Transmitter," Application Note AP-16, Santa Clara, Calif, 1978
3. Intel Corp, "Application Techniques for the MCS-48 Family," Application Note AP-24, Santa Clara, Calif, 1978
4. Intel Corp, "Serial I/O and Math Utilities for the 8049 Microcomputer," Application Note AP-49, Santa Clara, Calif, 1979



Lionel Smith is currently managing the applications group of Intel's Micro Controller Operation responsible for the single-chip microcomputer product line. His work experience includes designing a process control oriented computer mainframe and microprocessor based communication terminals. He received a BS degree from Case Institute of Technology.

DESIGN NOTE

Expanding UART Word Widths for Low Speed Data Transmission*

Several UARTs have been incorporated into a graphic display communication system in order to achieve the wider data word transfers needed for connecting additional switches and indicator lamps

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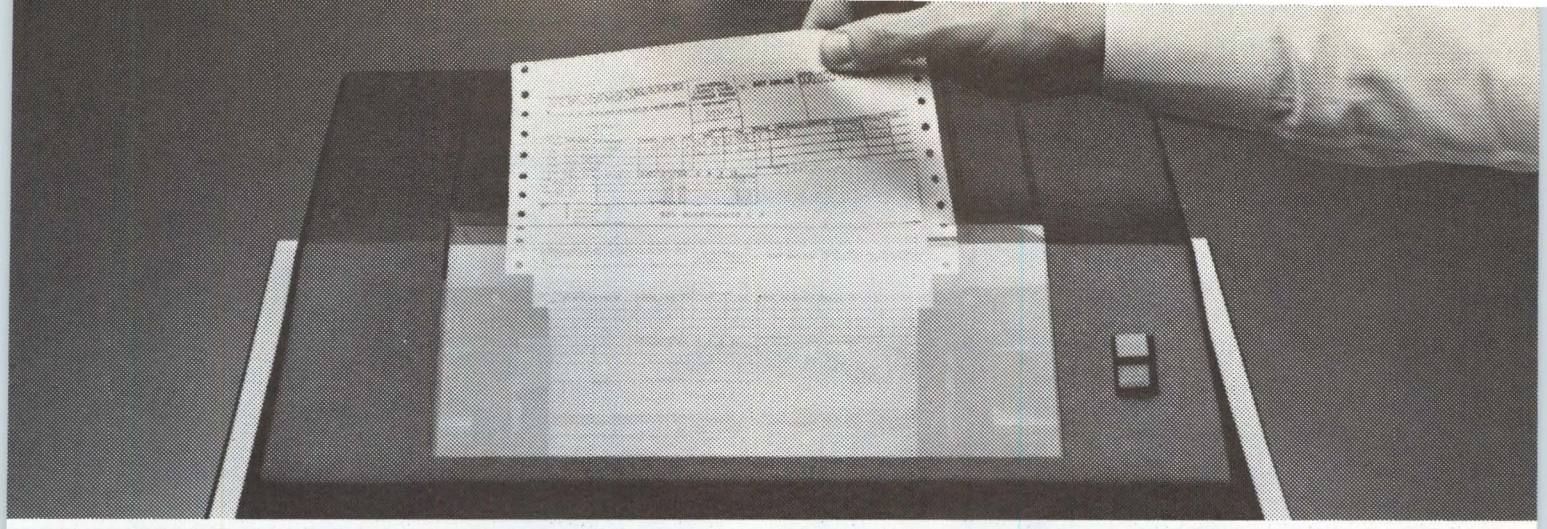
Large scale integration has merged powerful and complex functions on a single chip. However, these functions are often gained at the expense of flexibility, which could have been incorporated if the implementation used small scale integration. An example of this tradeoff is multiple universal asynchronous receiver/transmitter chips designed into a decoding and multiplexing communication system.

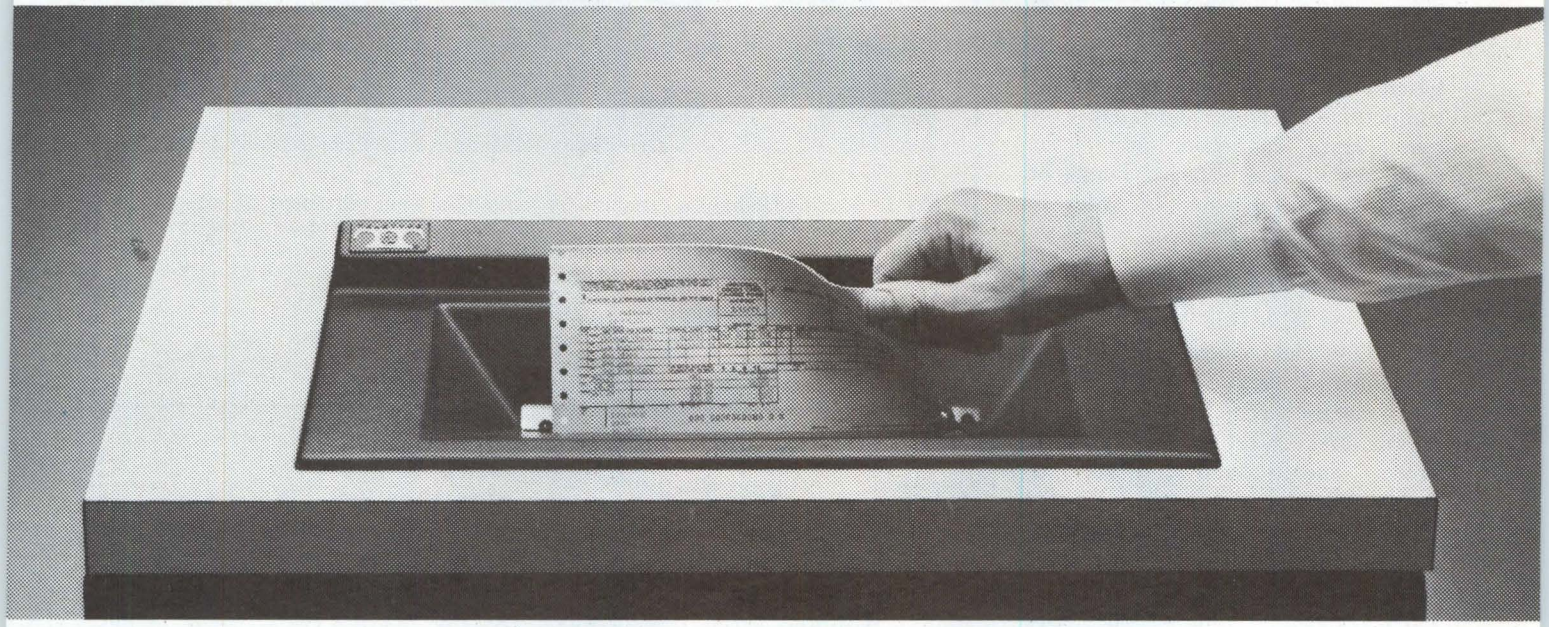
A universal asynchronous receiver/transmitter (UART) receives and transmits binary characters serially with appended error detecting and control bits. All characters contain a start bit, five to eight data bits, an even, odd, or nonexistent parity bit, and either one or two stop bits. The data rate (bits/s), parity mode, and number of stop bits are jumper-selectable on most UARTs. Standard rates seldom run above 9600 bits/s —a data byte (8-bit) transfer rate of less than 1000/s. This speed constraint is acceptable where a human operator is involved. However, 8-bit maximum data word width is unacceptable for most such communication applications, and this has led to combining extra circuits with UARTs in a decoding and multiplexing system which effectively expands the widths of transmitted and received words for low speed data.

System Background

In many nuclear science experiments, data-taking has traditionally been accomplished with digital hardware worth several thousands of dollars. It may cost hundreds of thousands of dollars, however, to interface the human experimenter to interact quickly with digital data. This part of the investment is mostly in a

*This work was supported by the Physical Research Division of the Department of Energy under Contract No W-7405-ENG-48.





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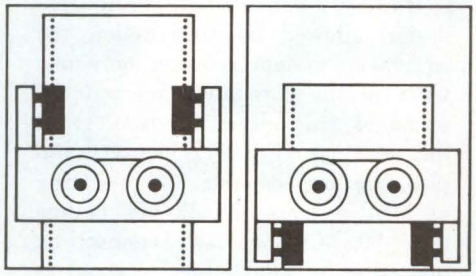

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computer mainframe and affiliated system capable of generating and manipulating complex graphic displays, some containing as many as 10^6 discrete points, under the online interactive control of a scientist-operator. In developing these systems, control switches and indicator lamps are usually added to an existing graphics terminal (Fig 1). This combination enables the operator to invoke functions with single switch movements that might otherwise require the distraction of typing a word or phrase. The indicator lamps allow the computer system to efficiently feed back information, such as which operations are legal or active. The switches contain lamps, and operational switches are illuminated by the computer. Circuits added to the switch/lamp connection allow the computer to flash selected lamps or combinations of lamps in order to alert the operator.

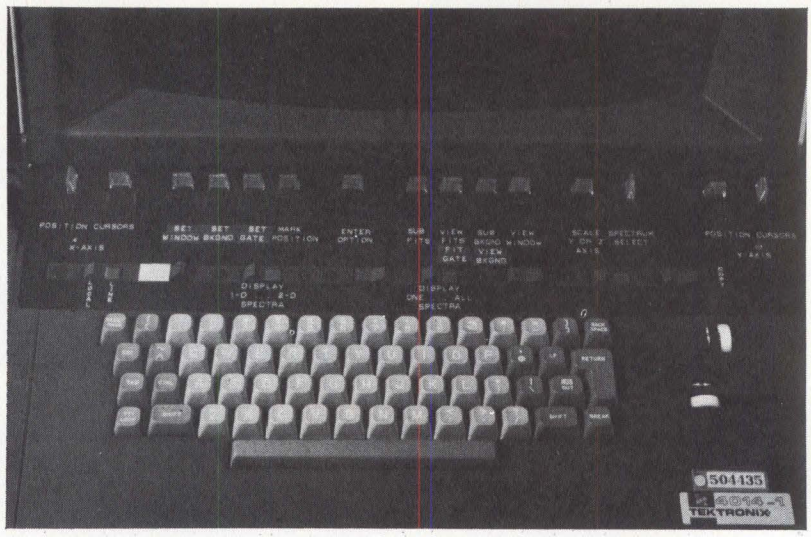

Fig 1 Modified graphics terminal. Terminal has been retrofitted by extending keyboard mounting brackets and moving keyboard forward to allow row of illuminated switches in addition to existing rocker switches and LED lamps to be inserted

System Requirements

Experience with this mode of operation in nuclear science experiments has dictated that about 32 switch positions are needed for controlling the data-taking and online analysis process fluently, and that approximately 24 lamps are adequate for status indicators. The keyboard and the display (Fig 1) normally communicate with the computer system independently of the switches and lamps via a separate serial link, but also use UART chips for serial transfer. However, the data transmission system has been modified to provide handshaking from terminal to computer. In addition to handshaking, data driver/receiver modifications have increased the transmission rate from computer to terminal to 400k bits/s, considerably enhancing the system graphic refresh capability over the original maximum 9600 bits/s.

Serial data transfer makes the terminal extremely mobile. The terminal can be used in the mainframe area while doing programming, or can be unplugged and wheeled to any one of four remote experimental sites up to 100 m distant. This serial link also reduces cable costs, and simplifies disconnecting and reconnecting the terminal.

In the initial design, addition of switches and lamps to the console required a 32-bit parallel bidirectional connection which degraded system mobility. The solution was to use serial transfer for the switches and lamps, investing in logic to make the transfer appear parallel at either end. This initial serial design was done under severe time constraints, and a straightforward transistor-transistor logic (TTL) implementation was used. Using TTL, the initial design required 45 integrated circuit (IC) packages at the computer and 43 at the terminal.

However, using UARTs in a final design allowed by time relief, the equivalent system requires only one UART at the computer and nine IC packages (including four UARTs) at the terminal (Fig 2). The TTL implementation, capable of operating at 1 MHz, transmits 32 bits in less than 50 μs. The UART connection, operating at 9600 bits/s, requires about 5 ms to transfer 32 bits of switch contact data into the computer. While the UART transfer is 100 times slower, it is still much faster than human operator response.

Design Procedure

The UART has a data available bit that is set with successful reception of a data byte. This bit on each UART is wired to the address input of a 1:8 decoder chip (Fig 2). A single serial input data line is wired to the decoder chip enable input. With all three data available lines low, output 0 of the decoder becomes active and is gated on and off by the serial input data at the enable input. Decoder output 0 is wired to the serial data input of UART I, which receives the first data word. Upon successful reception of this first data word, UART I turns on its data available line, switching the decoder to output 1, connected to the serial data input of UART II.

UART III connects to decoder output 3, and UART IV to decoder output 7. Successive serial data inputs fill the four UARTs, and all additional inputs go to UART IV. The parallel data outputs from UART IV are used to control miscellaneous functions. In Fig 2, two of the eight bits for UART IV select one of the four UART serial data output lines for connection back to the receiver at the computer. Other functions required of these eight available control bits are resetting of data available lines, and triggering of data transmissions back

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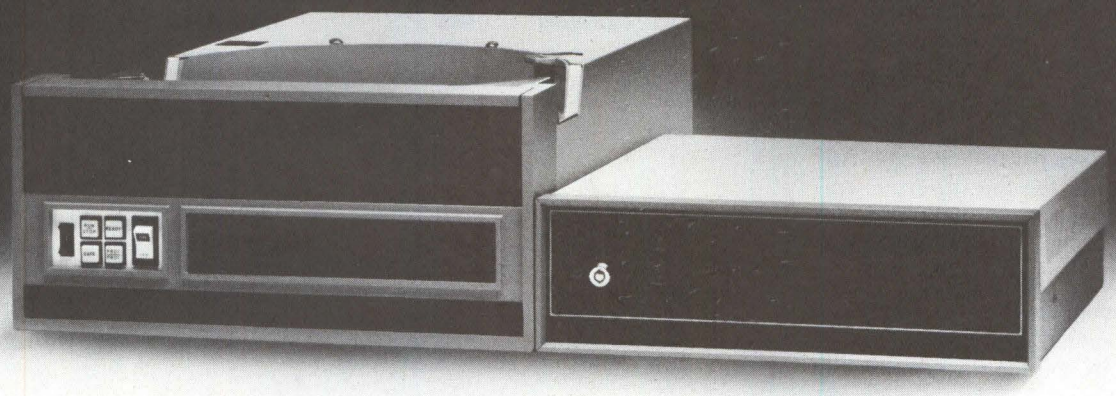

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to the computer. In Fig 2, output word width has been expanded to 24 bits (reserving 8 for control) and input word width to 32 bits, all with just two ICs in addition to 4 UART chips.

An additional priority encoder IC allows expansion to 8 UART chips with 56 outputs and 64 inputs (Fig 3). Previously, the three data available lines were used to form codes 0, 1, 3, and 7. With an 8-level priority encoder, each of the eight data available inputs generates a unique 3-bit select-address output code to drive the 1:8 decoder and to select the particular UART to receive data. UARTs I through VIII must be wired to progressively higher priority inputs, of course, because the highest priority input to the priority encoder determines the output code.

Fig 4 is the multiple-UART final system design. The 4-UART configuration is adequate for this application, producing 24 output bits and 32 input bits, eliminating need for the priority encoder. In addition to the 1:8 decoder and multiplexer (MUX), three housekeeping devices are necessary. One is a 9617 level-converting line receiver for serial data reception, the second a 9616 level-converting line driver for serial data output, and the third a dual one-shot pulse generator. Half the generator derives the clock required by the UARTs, and the other half widens the pulse to reset the data available line coming from the UARTs. Fig 4 also shows a lamp driver circuit and three blink circuits, which are turned on by control bits from UART D and which blink lamps for operator attention. In the SN74LS124 dual voltage-controlled oscillator, bits RDD3, RDD4, and RDD5, respectively, enable the three blink circuits. Bit RDD6 is attached to the frequency control input of the oscillator to set a blink frequency. The blink bus is part of the lamp driver circuit. By inverting the oscillator outputs, they could be connected to UART received data enable lines to achieve the same blink control. This would have saved 24 diodes, but would have required installation of an inverter chip. Under normal conditions, using the additional inverter would result in a lower parts count and space savings. However, one diode is mounted along with one lamp driver on the body of each switch, saving space on the

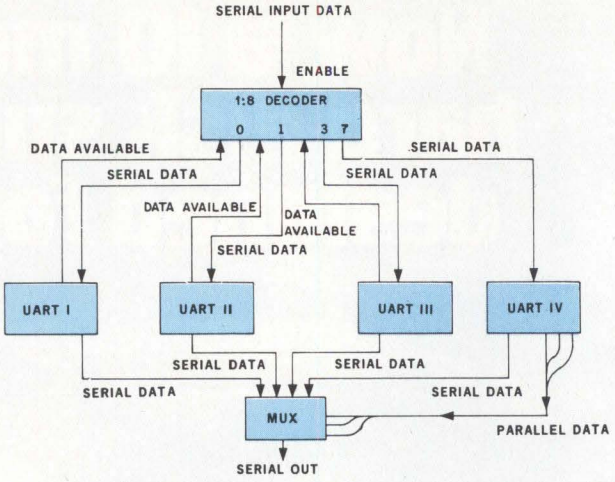


Fig 2 Decoder/multiplexer for multiple UARTs. Four UARTs in this configuration accept 24 bits from computer and provide 32 bits to computer. Computer uses single UART to drive serial input and to accept serial output. Decoder switches successive 8-bit transmissions to successive UARTs. MUX connects selected UART to single serial output

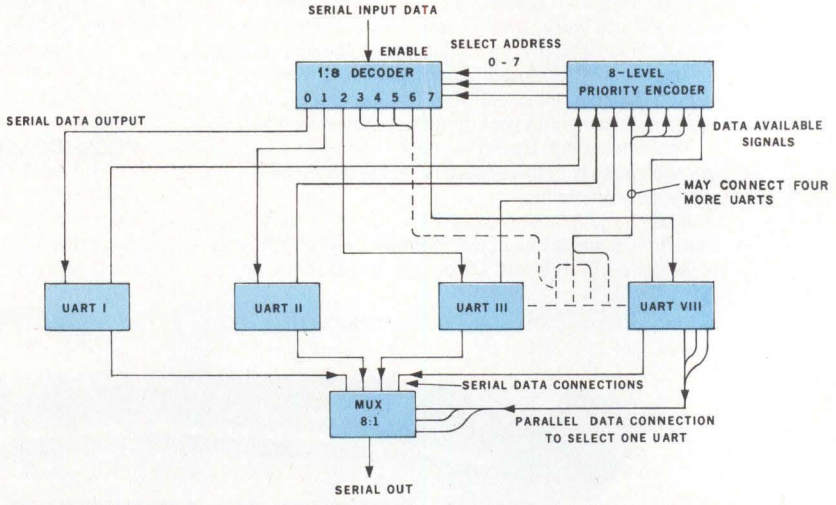
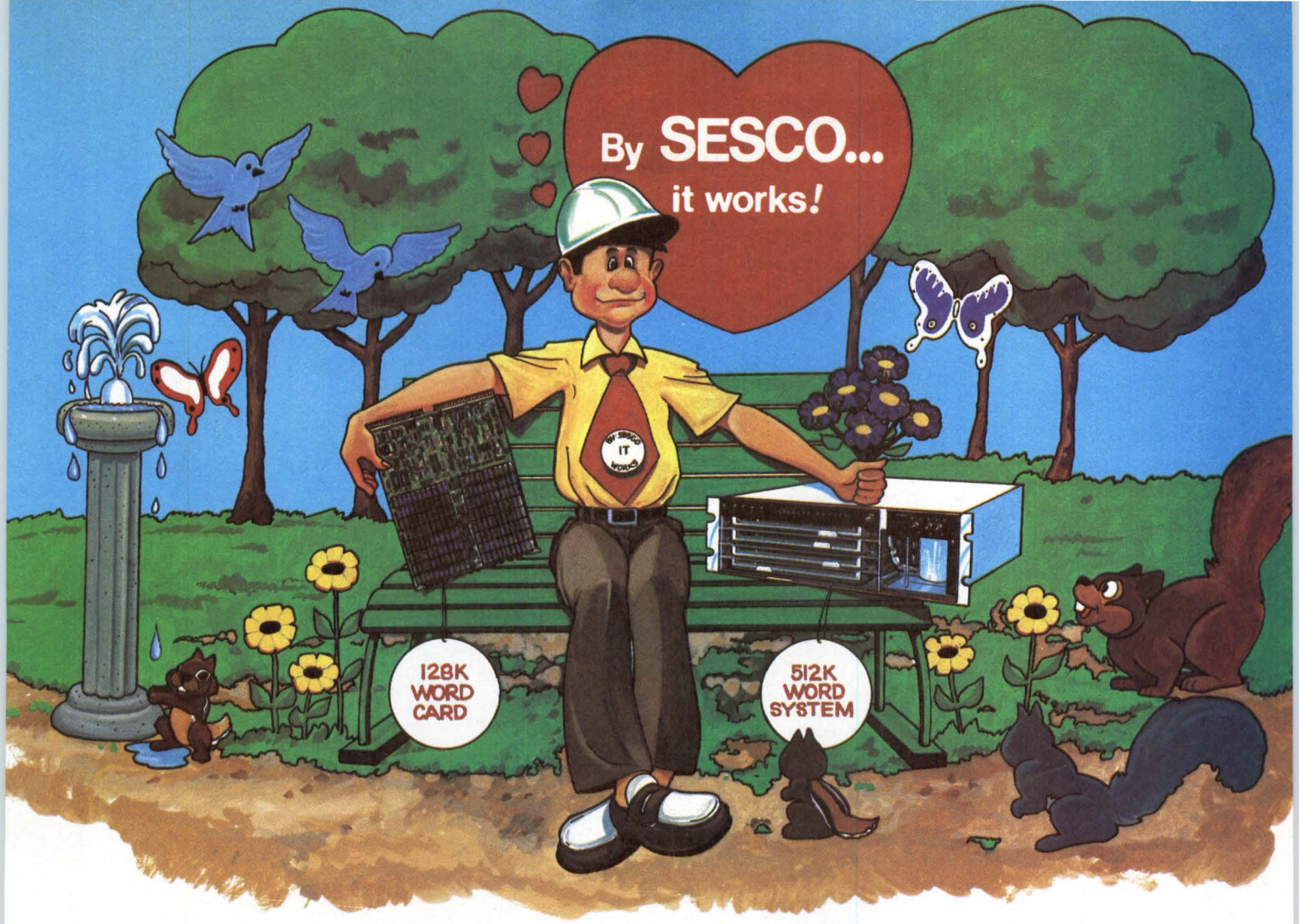


Fig 3 Priority encoder addition. Adding 8-level priority encoder to circuit of Fig 2 permits expansion to as many as 8 UARTs with 56 output bits and 64 input bits. Lowest priority input must correspond to decoder address 0, highest priority to decoder address 7 since it is used to generate select address



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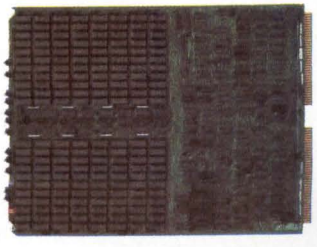

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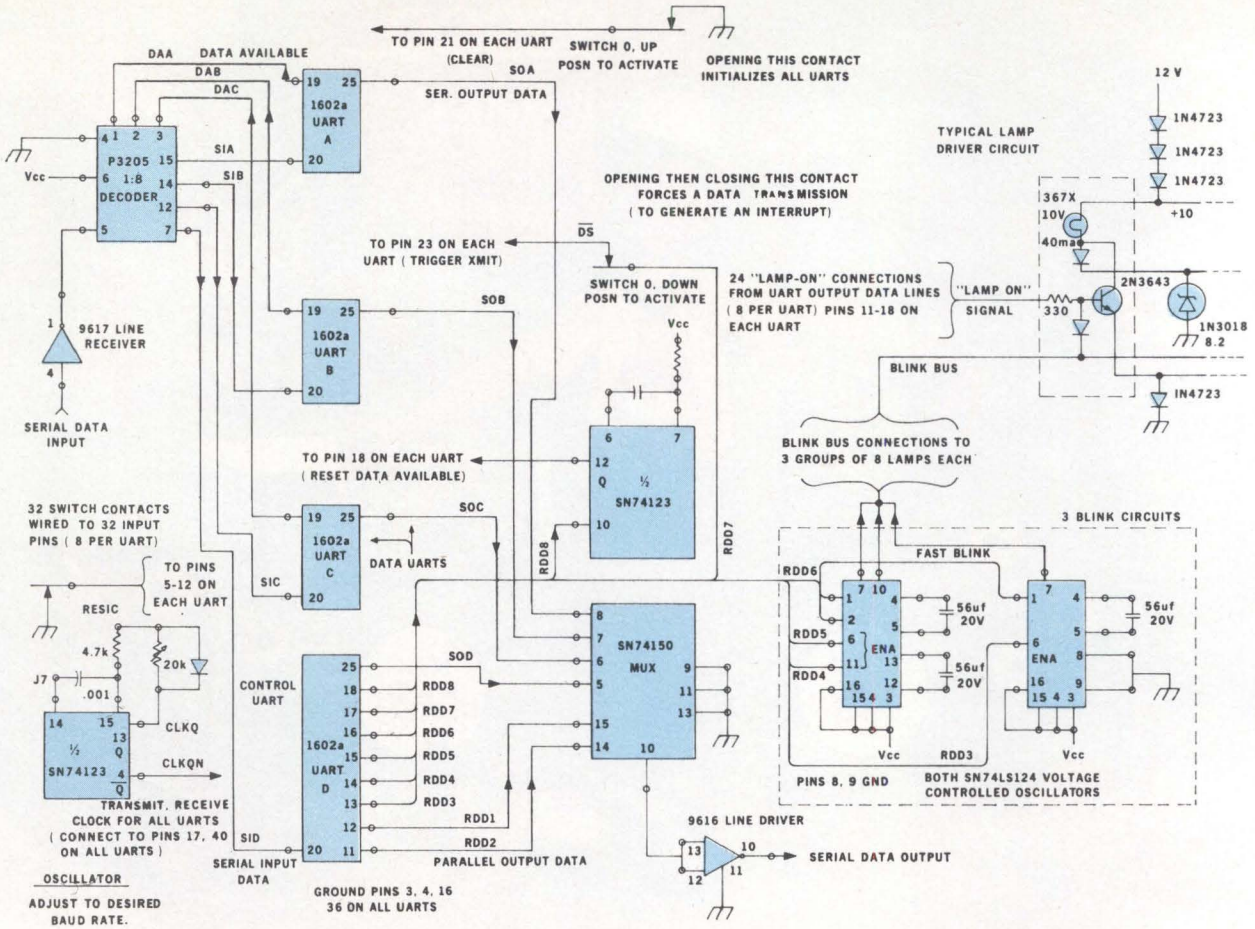

Fig 4 Final system design. This logic connects computer system to row of illuminated switches. 1602A UART was chosen because of availability. 24 bits from UARTs A to C drive 24 "lamp-on" signal lines. Switch contacts are wired to each of 32 UART input pins for transmission to computer system. Voltage-controlled oscillators independently control blink rate of three groups of eight lamps each, and are enabled by parallel outputs from UART D

printed circuit board used to hold control logic. This saving allowed the hardware to fit into existing, but limited, space at the terminal.

An additional feature of this design is the ability to send a signal back to the computer on operator command. The UART clear and transmit signals are connected to a single 2-position switch. In one position, the switch issues a clear to the UARTs, connecting UART A for both transmission and reception. In the other position, the switch triggers a transmission from the UARTs. When power is first turned on or when a hangup occurs in the attached computer, this capability can be used by the attached computer system to force recovery.

Summary

A UART used alone is limited in operating speed and in the number of bits transferred at one time. In system applications where serial data transmission is required and where an operation is being performed with a human operator, operator speed, not that of the UART, becomes the limiting system performance rate. As described, a small amount of extra logic can be added to an array of UARTs to effectively expand the width of word transmissions, allowing the connection, for example, of 32 lamps and 24 switches to a computer. An equivalent TTL implementation of the same function required 88 ICs as compared with the 9-IC UART implementation.

Acknowledgement

Mr Jaff Lin was responsible for the initial TTL implementation of the switch and lamp connection to the keyboard/display terminal.

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DESIGN NOTE

A Software Based Approach to Priority Interrupts

Software and hardware methods for priority interrupt encoding in a 9-peripheral control system are examined for memory, time, and logic requirements. Unless time is at a premium, the software approach seems the one to take, with significant savings in hardware costs

B. K. Gupta Bhabha Atomic Research Centre, Bombay, India

Microprocessors provide an efficient method for interrupt servicing in governing asynchronous events that occur external to the processing system. However, the microprocessor can service only one interrupt at a time, while in many intensive control and data processing applications, several devices are simultaneously generating interrupts. Therefore, in a hardware based interrupt approach, external hardware must determine which of several devices is to be serviced on a priority basis and then inform the central processing unit; or, in a software based approach, the central processor polls all the devices and establishes device priorities and grants.

Interrupt Structure

The National Semiconductor SC/MP microprocessor used in examining the systems approaches has a relatively simple interrupt processing capability (Fig 1). An external status input (SENSE A) signal serves as the interrupt request line, after bit 3 (interrupt enable [IE] flag) of the 8-bit status register is set to high using either the interrupt enable instruction (IEN), or the copy accumulator to status (CAS) instruction. Thus, when the IE flag is set, SENSE A input is tested prior to the fetch phase of each instruction. When an interrupt request is detected, the IE flag is reset to prevent the microprocessor from responding to any

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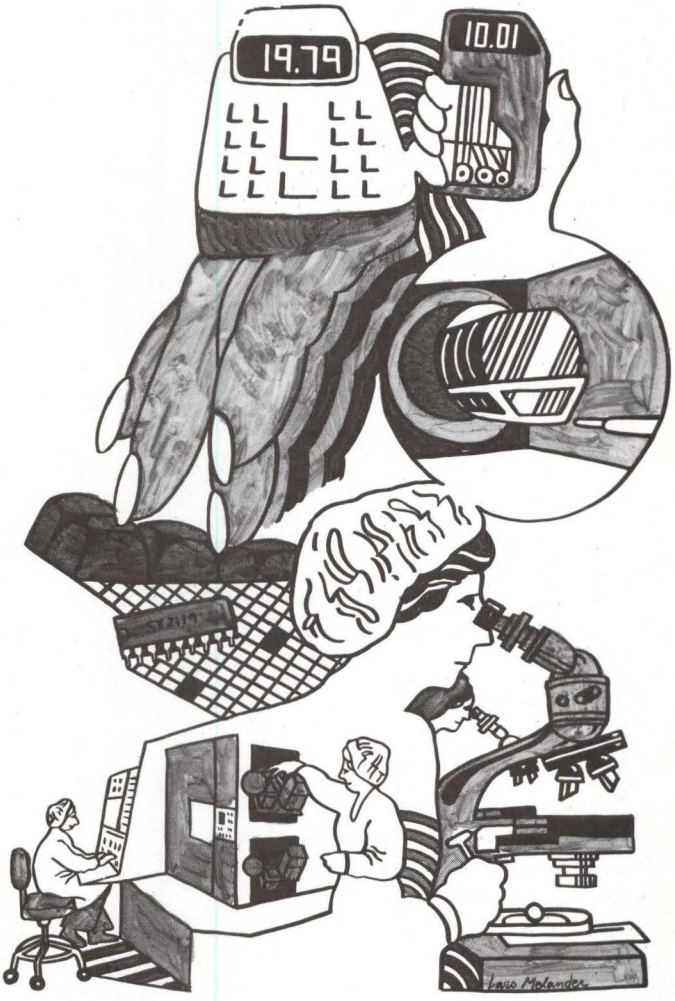

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SY2142	200-450nsec	500mW	1024x4	20 pin
SY2142L	200-450nsec	350mW	1024x4	20 pin
SY2142LV	200-450nsec	350mW	1024x4	20 pin
SY2101A	250-500nsec	275mW	256x4	22 pin
SY21H01	175-200nsec	450mW	256x4	22 pin
SY2111A	250-500nsec	275mW	256x4	18 pin
SY21H11	175-200nsec	450mW	256x4	18 pin
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further interrupt requests, and the contents of the 16-bit program counter (PC) are exchanged with the contents of the 16-bit pointer register 3 (P3); that is, P3 must contain the beginning address minus one address of the interrupt service subroutine. The return address, where program execution must continue after the interrupt request has been serviced, is now stored in P3. The return-from-interrupt sequence needs to set the IE flag to high, and then again exchange the contents of PC and P3, by using instructions IEN and XPPC P3 (exchange PC and P3), to resume the main program.

System Application

Fig 2 shows the hardware requirements of both interrupt schemes for servicing nine peripheral devices. Some hardware functions, such as latching interrupt requests from each device, clearing the corresponding request after service, and generating CPU interrupt, are common to both schemes. The bank of nine 7474 device request latches (A) receives the device interrupt requests and stores them. The $\overline{Q}$ outputs of these latches are passed through three NAND gates (7430 and one half of a 7400) to deliver a common interrupt request to the central processing unit (CPU). The CPU then clears the request of the device identified for service through a 4-to-16 decoder (74154) by executing a STORE (ST) instruction. Additional hardware needed for the software approach is enclosed by solid lines (S) and that needed for the hardware approach is enclosed by dotted lines (H). For either approach, the interrupt service subroutine must be notified of the address of the device to be serviced.

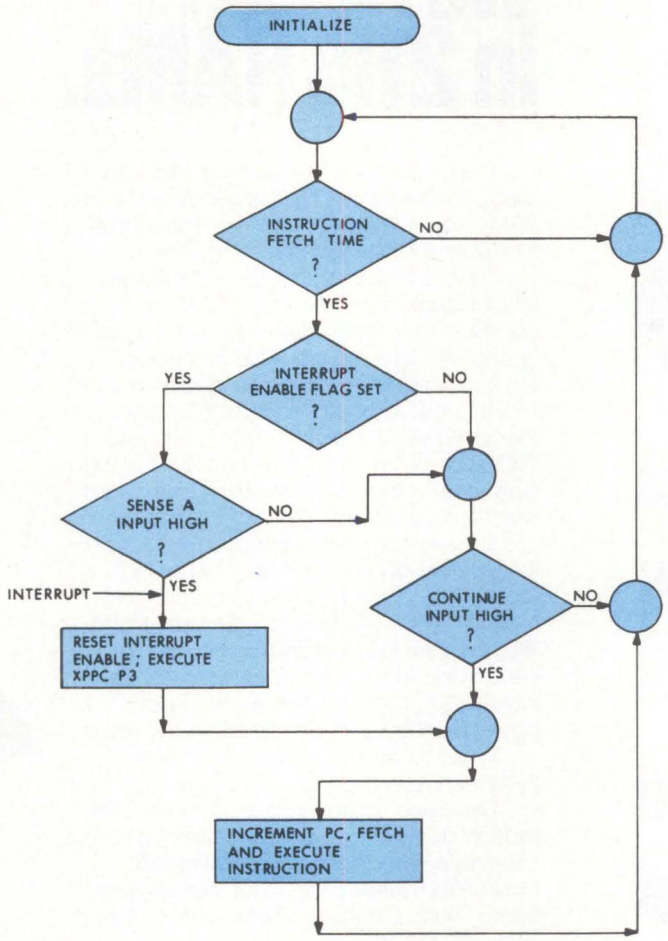

Fig 1 Interrupt request process. External status input (SENSE A) to microprocessor CPU serves as interrupt request line if bit 3 of 8-bit status register is set to high. Bit 3, interrupt enable (IE) flag, is set with interrupt enable instruction (IEN). When interrupts are enabled, SENSE A line is tested at beginning of every instruction fetch operation. If SENSE A is high, IE flag is reset and contents of 16-bit program counter (PC) are exchanged with contents of 16-bit pointer register 3 (P3)

Total Hardware Approach

The $\overline{Q}$ outputs of the device request latches are connected to the D inputs of another set of latches (two 74174s). In turn, the 74174 outputs are fed through a 74147 priority encoder (PE) and 3-state buffers (½ x 81LS96) to CPU data bus terminals DB0 to DB3. When SENSE A goes high, the CPU enters an interrupt service routine and reads the PE output, which is the address of the highest priority device currently demanding attention, by executing a LOAD (LD) instruction. This address is read into the 8-bit CPU accumulator (A) on the rising edge of NRDS ($\overline{\text{READ}}$ $\overline{\text{STROBE}}$); see Fig 3. NRDS is NANDed with the decoded port address via two NAND gates (one half of a 7400) and latches the $\overline{Q}$ outputs of the device request latches into the two 74174s on the falling edge. This logic ensures the stability of the priority encoder output at the rising edge of NRDS. Without this latching action, data read into the accumulator could be erroneous. For example, assume that only device 3 has generated an interrupt—PE output is 0011_2. The CPU enters the interrupt service state and executes a load instruction to read PE output. Assume that just prior to the rising edge of NRDS, device 4 generates an interrupt; therefore, the PE output

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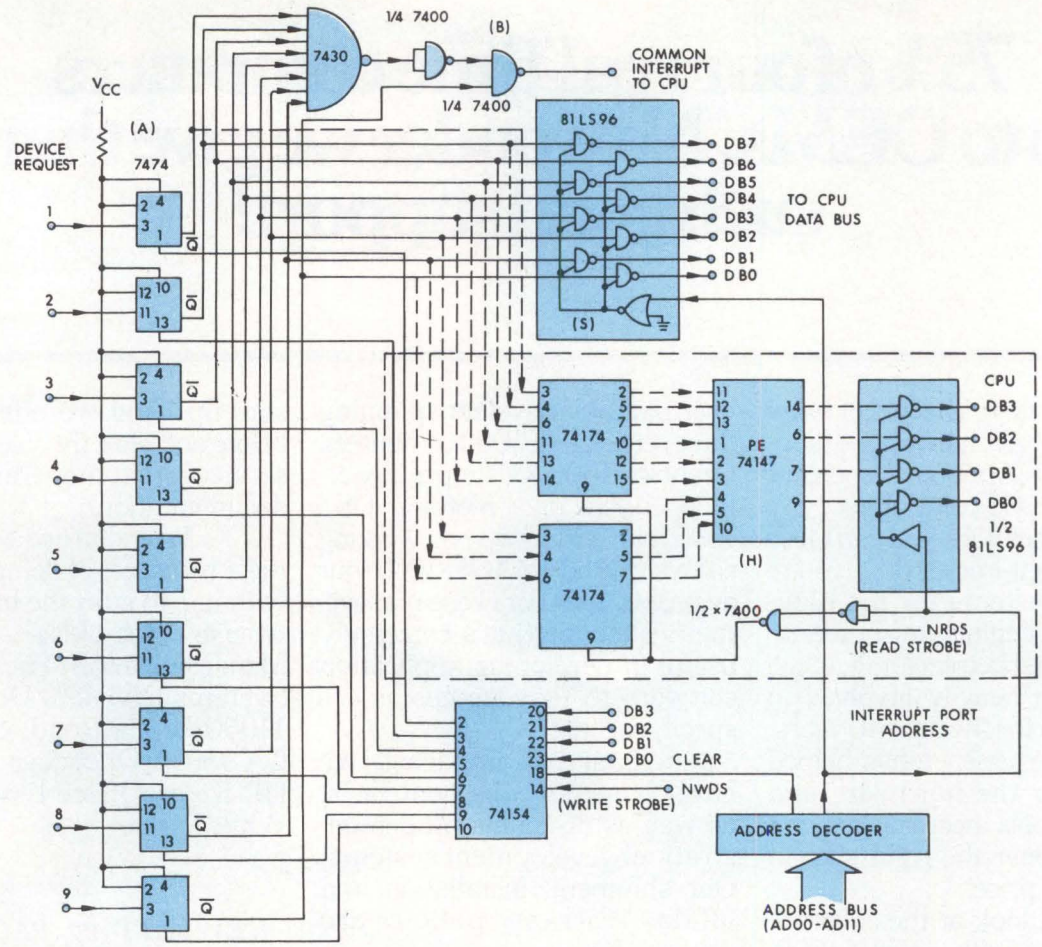

Fig 2 Software and hardware interrupt priority encoding approaches. Device requests 1 to 9 are latched at (A) and common interrupt to CPU is generated at (B). Additional hardware required for software and hardware approaches is labeled (S) and (H) respectively. In software approach, latched device requests are connected to CPU data bus. In hardware approach, latched device requests pass through two 74174 latches, priority encoder (PE), and 3-state buffers before connection to CPU data bus

changes from 0011_2 to 0100_2. The CPU could read data during this transition, which could be any value from 0000 to 0111_2. Consequently, latches are needed to stabilize the priority encoder output at the rising edge of NRDS. This technique requires two instructions to be executed: establishing priority, and clearing the corresponding device request, which takes four memory bytes and 72 μs.

Total Software Approach

In Fig 2, the outputs of device request latches 2 through 9 connect directly to CPU data bus terminals DB7 to DB0 through 3-state buffers (81LS96). Highest priority is assigned to device 9 and lowest priority to device 1 by the software program (see Assembly Language Program). Upon interruption, the CPU initializes location PRIOR to $0A_{16}$ (highest priority address plus one address) and location COUNT to 09_{16} (number of devices) by executing load immediate (LDI) and STORE (ST) instructions. Then, the LOAD instruction reads the 8-bit output of the device request latches into the accumulator. At subroutine ENCODE, the CPU executes XAE and exchanges the contents of the accumulator with those of the extension (E) register. Thus, when the CPU executes XAE the first time, extension register bits 7 through 0 will hold the request status of devices 2 through 9. Next, location PRIOR is decremented by one with the DLD instruction. Similarly, location COUNT is decremented by one, and its contents are tested for zero by jump if zero (JZ). If the value of COUNT is zero, the CPU goes to location OVER, and location PRIOR contains the address of the lowest priority device, which is 1; otherwise, the LDE instruction copies the contents of the extension register into the accumulator. The RR

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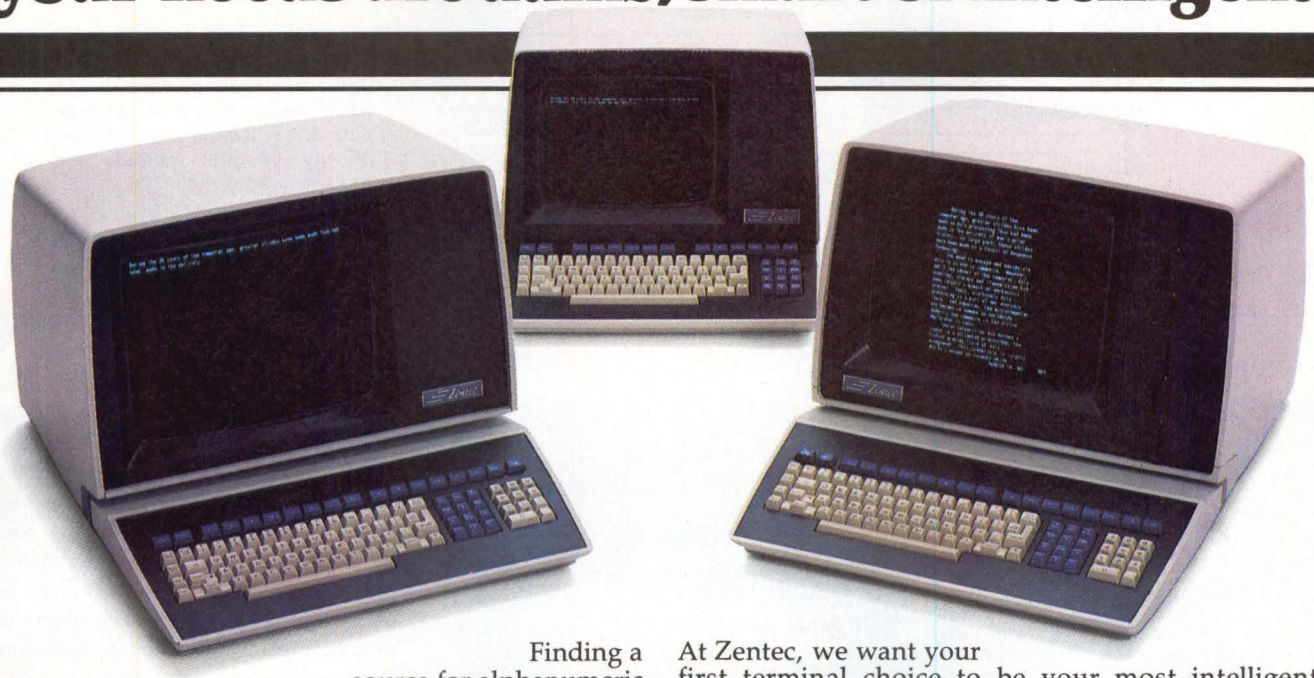

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Video Attributes	Limited	Some	Some	
Screen Character Matrix Resolution	5×7	7×8	7×9	
"Soft-Font"	No	No	Some	
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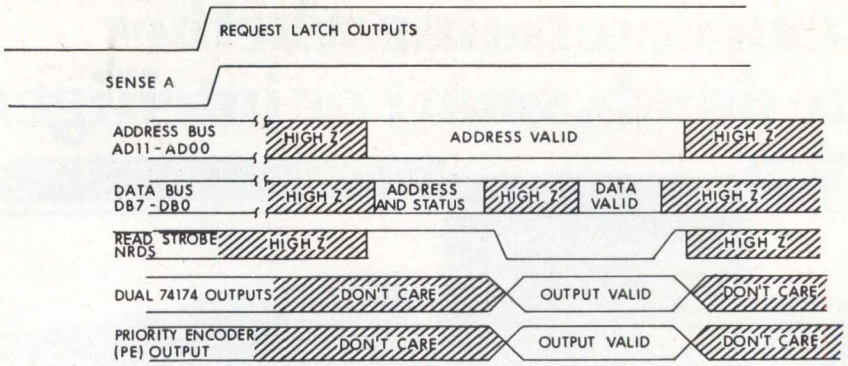

Fig 3 System timing diagram. Upon interruption, CPU reads either device request latch outputs for software approach or priority encoder outputs for hardware approach

Assembly Language Program for Software Priority Encoding

```
ENTER:    LDI   OA16      ; Initialize PRIOR to OA16
          ST    PRIOR     ; Store accumulator contents in
                          PRIOR
          LDI   0916      ; Initialize COUNT to 0916
          ST    COUNT     ; Store accumulator contents in
                          COUNT
          LD    DATA      ; Read interrupt port
ENCODE:   XAE               ; Exchange interrupt port data with
                            those of extension register or
                            right rotate interrupt port data by
                            one bit
          DLD   PRIOR     ; Decrement PRIOR; then load into
                            accumulator
          DLD   COUNT     ; Decrement COUNT; then load into
                            accumulator
          JZ    OVER      ; If accumulator contents are not
                            zero, continue; otherwise, jump
                            to OVER
          LDE             ; Load contents of extension register
                            into accumulator
          RR              ; Rotate accumulator contents right
                            by one bit; rotate low order bit
                            of accumulator into high order
                            bit
          JP    ENCODE    ; If 7th bit of accumulator is zero,
                            jump to ENCODE; otherwise,
                            continue
OVER      LD    PRIOR     ; Load accumulator with PRIOR con-
                            tents
          ST    CLEAR     ; Clear interrupt request correspond-
                            ing to device encoded
```

instruction rotates the contents of the accumulator (request status of devices) to the right by one bit. The jump if positive (JP) instruction terminates the encoding if bit 7 of the accumulator is 1; otherwise, the CPU goes back to the ENCODE subroutine. The ninth through the second device request address bits are tested sequentially, from LSB to MSB, and each zero bit detected results in decrementing location PRIOR. Encoding terminates at the first 1 bit detected or if the second through ninth device requests are all equal to zero. At program end, address of the highest priority device demanding attention is left in location PRIOR, which is then sent to clear its corresponding request by the ST CLEAR instruction because it is actively being serviced. The complete program utilizes 27 bytes, including locations PRIOR and COUNT.

Test Measurements

From system measurements, the software based interrupt approach requires a minimum of 380 μs for the ninth device and 1656 μs for the first device to encode and clear the request. It also requires 23 more memory bytes than the hardware based interrupt approach but saves considerable hardware by eliminating two latches and the priority encoder. Also, if the number of requesting devices increases, the additional hardware needed increases proportionally; however, software requirements remain about the same. In the present application, each peripheral device is capable of interrupting the system every 900 ms. The interrupt service routine takes 5 ms max, including priority encoding. If all nine interrupts are received simultaneously, it takes only 45 ms for the CPU to attend to them; during the remaining time, CPU is free to compute other tasks. Wherever throughput speed is the primary requirement, the hardware based interrupt approach is optimum, but in most cases, the software based interrupt approach saves costs and still performs the servicing task, albeit at slightly slower speed. □

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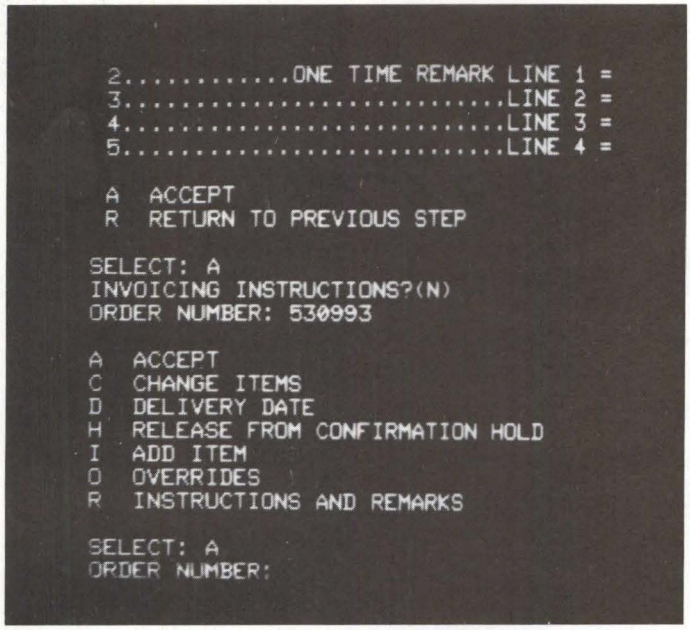
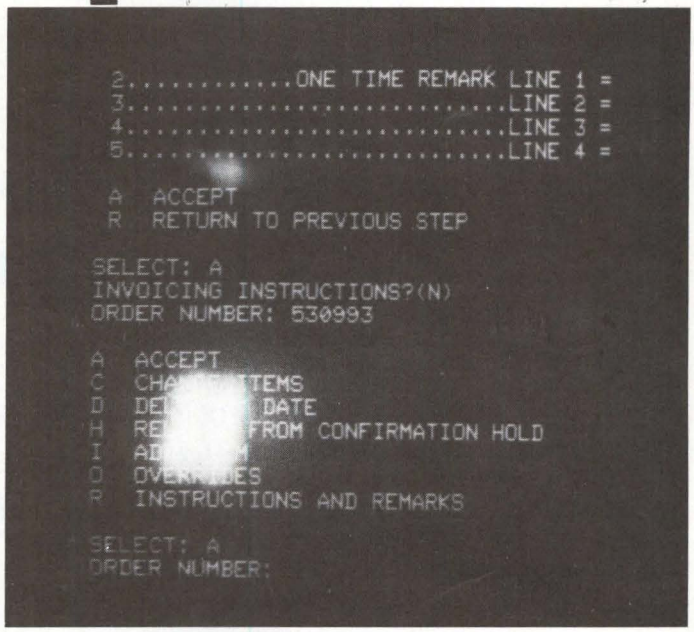


Display in ambient light with polarizer.



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APPLICATION NOTE

Weights and Scores Approach to Computer Evaluation

Planning and implementing computer systems for an emerging nationwide electronics industry allows an orderly selection methodology to be used for immediate as well as future data processing services

G. Gordon Schulmeyer Westinghouse Electric Corporation, Baltimore, Maryland
Beta Martinian Iran Electronics Industries, Shiraz, Iran

The range in capabilities of commercially available computer systems allows logical hardware growth patterns to be incorporated into an emerging foreign electronics industry. Judicious selection of computer systems to meet expected short and longterm needs supports establishment, growth, and maturity phases of information handling in an underdeveloped country (Iran).

Establishment Phase

Initial planning for the type of computer hardware suitable for the establishment phase and the beginning of the growth phase involved an investigation of computer requirements until a permanent site was ready for the ultimate large computer system. A system for the establishment phase had to meet requirements of computer training capability, engineering design processing, limited size, data handling, business processing capability, and price under $100,000.

It was immediately established that only minicomputers could be considered for the in-country price and size limitations. Of available minicomputers, only four manufacturers had foreign distribution and maintenance capabilities.

A weights and scores approach[1] was used for evaluation of the four available systems. A systems approach was taken for listing the weighted criteria, instead of the more traditional method of listing quantitative characteristics (instruction execution time, memory size, word size, etc). Table 1 summarizes the four evaluated systems.

To meet these requirements, the highest score—MSE C, a Data General NOVA 840 minicomputer system—was selected [Fig 1(a)]. In fact, because corporate headquarters are located in one city and operational divisions in another, two duplicate systems were ordered. In this setup,

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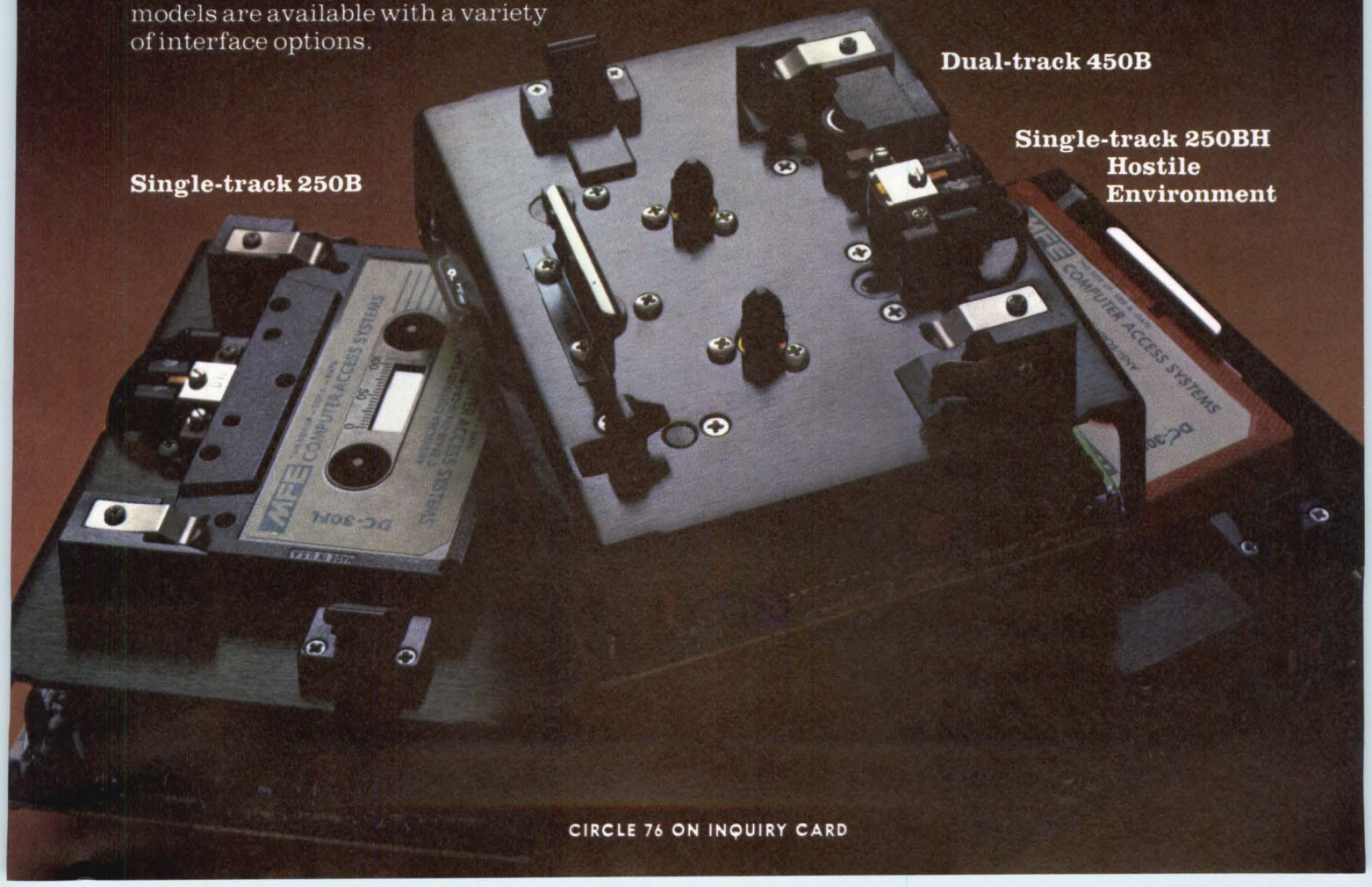

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TABLE 1

Minicomputer System Evaluation (MSE)

Criteria	Weight* (W)	System A	B	C	D
Computer Training Capability	10	5	6	9	7
Engineering Design Processing	8	8	2	10	5
Limited Size	10	9	6	8	6
Data Handling Capability	4	3	10	5	6
Business Processing Capability	4	2	9	5	6
Price	9	6	0	10	10
Environmental Requirements	7	5	2	10	9
Maintenance Availability	8	9	2	9	3
	TOTAL**	385	242	522	395

*A weight of 10 does not represent ultimate performance, only that it is a numerical coefficient assigned to express its relative importance in the comparison approach.

**TOTAL is obtained by a sum of products calculation: $\sum_{n=1}^{8} W_n \times MSE_n$

computer capability resided near the users without reliance on unpredictable telephone lines for communications linkup. Duplicate minicomputer systems had the additional advantages of providing emergency backup, if necessary, and of practicing consistency and commonality of software design.[2]

Corporate functions during the establishment phase included systems for finance and personnel, basic engineering calculations in filter design and analysis (passive LC, helical resonator, etc), and computer concept training for an unskilled local staff. Commitments of the operational divisions primarily required report generation of inventory items. The volume of data handled for sorting, although slow in processing, caused no major bottleneck to computer availability. It was basically handled by a 1-shift operation because of minimal workload.

Division contracts, engineering analyses, and corporate systems provided real-life problems requiring

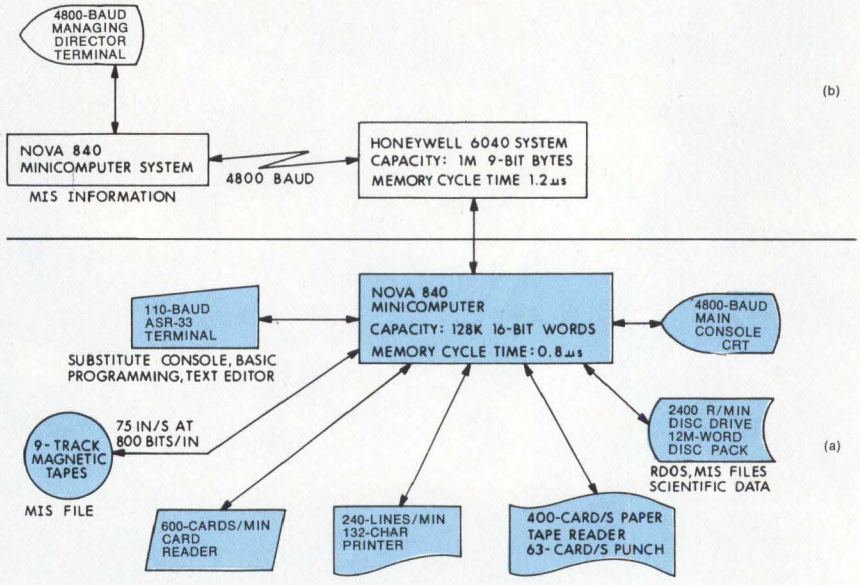

Fig 1 Computer system for establishment phase. Limited minicomputer system (a), indicated by colored blocks, proves sufficiently powerful to provide report training, engineering, business processing, and support. Other devices (b) are added in late growth and early maturity phases. Temporary connection is made to 6040 system. Benefits of tie-in include training on system similar to that due later, and conversion time for supplied corporate packages

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TABLE 2

Computer System Evaluation

	Criteria	Weight	A	B	C	D	E	F
1.	Maintenance	10	7	9	0	0	0	10
2.	Delivery	5	7	9	9	9	2	9
3.	Backup Availability	8	0	5	4	4	2	10
4.	Training Computer Immediately Available	9	0	5	7	7	1	10
5.	Engineering Support	10	40*	80	40	40	64	96
	a. Math and Statistics Package	8	5	10	5	5	8	9
	b. Configuration Control	6	0	0	0	0	0	4
6.	Manufacturing Support	10	116†	234	168	136	110	222
	a. Inventory	10	8	10	8	9	9	10
	b. Production Scheduling	6	6	9	4	0	0	8
	c. Purchasing	5	0	4	8	2	4	4
	d. Material Handling	6	0	10	4	6	0	9
7.	Financial Support	9	126#	134	118	120	120	140
	a. Payroll	6	9	9	9	8	8	10
	b. Accounting	8	9	10	8	9	9	10
8.	Personnel Support	5	2	5	2	4	2	5
9.	Marketing	2	2	7	4	2	4	6
10.	Remote Communications	8	10	10	4	5	5	9
	TOTAL		2893	4685	3332	3044	2913	4864

*5a. Math and Stat Pack: 8×5=40
5b. Conf Control : 6×0= 0
40

†6a. Inventory : 10×8=80
6b. Prod Sched : 6×6=36
6c. Purchasing : 5×0= 0
6d. Material Hand: 6×0= 0
116

#7a. Payroll : 6×9=54
7b. Accounting: 8×9=72
126

computer aided solutions,[3] and contributed greatly to introducing the unskilled staff to practical inhouse computer applications and hands-on experience.

Growth Phase

New divisions started operation in scattered sites and required substantial computer support. Initially, the corporate minicomputer was instituted under central control, thereby making it available on a corporate wide basis. This setup solved immediate needs; however, acquisition plans were formulated for more computer and/or peripheral hardware to respond to increasing and diversified division needs.

A system plan was effected that connected remote division data terminals to the central corporate minicomputer. ASR-33 terminals were added, as the workload for each division justified their inclusion, to provide local computer capability.

During the late growth and early maturity phase, a similar weights and scores approach was used for evaluation of the large scale computer. This time, however, additional company distributors were available: accordingly, six systems were evaluated, resulting in two close contenders. The particular computer was chosen through the weights and scores approach with systems requirements as the weighted criteria (see Table 2).

Although recognized as a nonstandard method for justification, this approach becomes particularly effective in explaining complex computer selection criteria in a context meaningful to nontechnical management. Tabulated data were supported with standard quantitative criteria that fell within system requirements.

System F from Table 2 is the Honeywell L6610 series computer. During the growth phase, experience is acquired by computer specialists on a similar computer system—a

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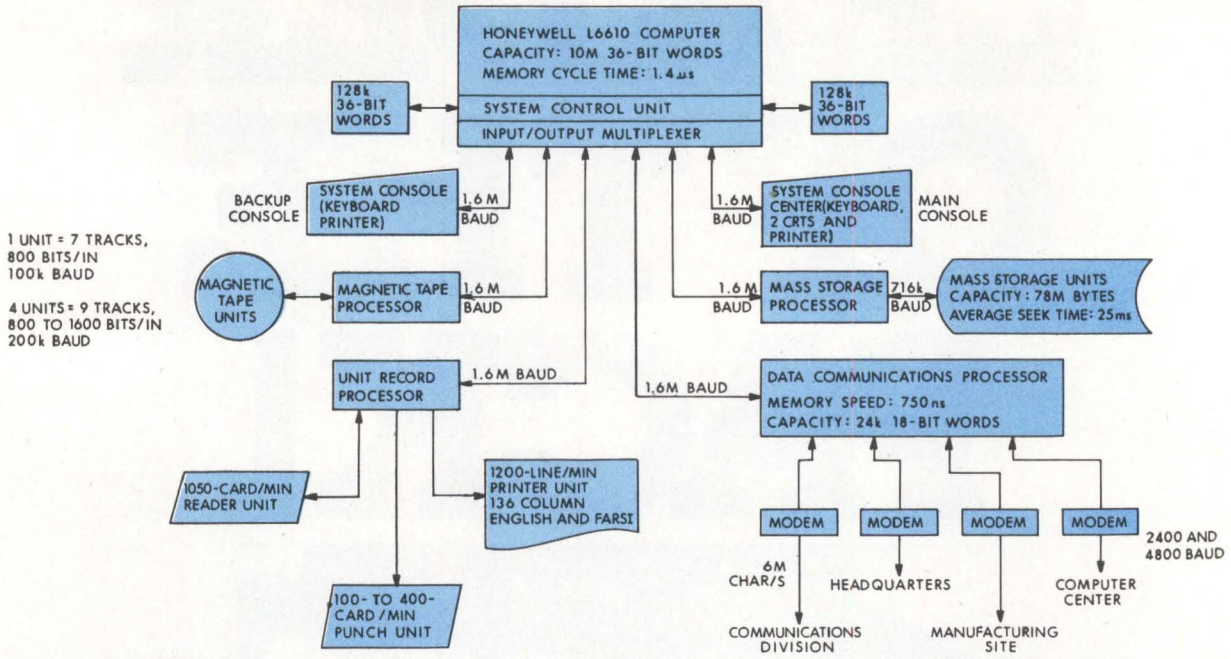

Fig 2 Computer hardware system for maturity phase. Central corporate computer maintains data bases and processes reports. Remote division growth occurs from smaller to larger terminals to provide support concurrent with division growth

system criterion. The Honeywell 6040 computer fills this role [Fig 1(b)]. Existing minicomputer systems act as satellites to the 6040 computer during nighttime operation. Daytime operation of the minicomputer sytems remains the same; they function as independent processors.

Temporary 6040 operation develops workable computer systems for the maturity phase. Also, valuable experience is gained by computer specialists for the L6610 system. Knowledge increases in tandem with computer hardware complexity.

Maturity Phase

In the maturity phase, the central objective is the establishment of a corporate L6610 computer center (Fig 2). This computer center takes over the primary corporate data processing functions for personnel, finance, purchasing, payroll, manufacturing support, engineering support, and management information systems (MIS). Division functions are handled by associated terminals; terminal size or configuration is based on expected workload. Experience is gained in chronological order: initial experimental batch applications; full range of applications, inquiry systems; network data collection, remote batch processing; integration of files, operational dispatching, and full transaction processing; and private information, simulation systems, and intercompany linkages.[4]

The choice of peripherals depends on division experience and requirements. This method allows maximum flexibility to provide optimum computer support and manageable cost. Thus, the large computer system centralizes EDP processing, as follows: corporate database access for divisional projects or personnel information, large computer capability for jobs that cannot be processed on a minicomputer, and access to application packages available from the computer manufacturer. Decentralization of control for the divisional minicomputer system permits reducing L6610 load, division management scheduling of priorities, cost benefits of placing the appropriate size programming job on the computer suited to the task, and local division availability of a computer for engineering programming training.

Acknowledgement

Mr Mahmoud Bakhtiar and his EDP staff of the Management Information Systems Department of IEI ably assisted the authors in the development of this note.

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APPLICATION NOTE

Interfacing Peripherals Directly to an Array Processor

A high speed programmable array processor coupled directly to I/O devices offers increased throughput and accuracy by supporting simultaneous data acquisition, processing, and display

Paul Wiley Floating Point Systems, Incorporated, Beaverton, Oregon

Programmable array processors are dedicated, relatively low cost computers designed to provide the high computation rates, high precision, and large numerical dynamic range required in scientific computing and signal processing applications.* The array processor functions as a specialized processing element in conjunction with either a host minicomputer or mainframe (Fig 1). While the array processor is devoted to handling numerically intensive calculations, the host computer's inherent capability for handling programming input, file manipulation, and input/output operations generally furnishes the interfaces to the outside world. In some applications, however, it is highly desirable to supply direct input/output access to the array processor.

Where Direct I/O Is Needed

Applications where direct input/output (I/O) access to the array processor is required sort into four categories: realtime applications in which the maximum I/O rate of the host is exceeded, applications in which maximum array processor throughput is necessary, applications in which the array processor requires dedicated memory peripherals, and applications in which the host is dedicated to performing data analysis on the results of computations in the array processor and is unable to simultaneously handle I/O.

In realtime processing applications, fast analog to digital (A-D) converters are often employed to feed data at transfer rates in excess of 1 MHz from the realtime process to the array processor. Typical host computers are limited to a transfer rate of 500 kHz or less. For some array processors, two direct I/O interfaces are available that offer much faster access to the array processor.

*W. R. Wittmayer, "Array Processor Provides High Throughput Rates," *Computer Design*, Mar 1978, pp 93-100

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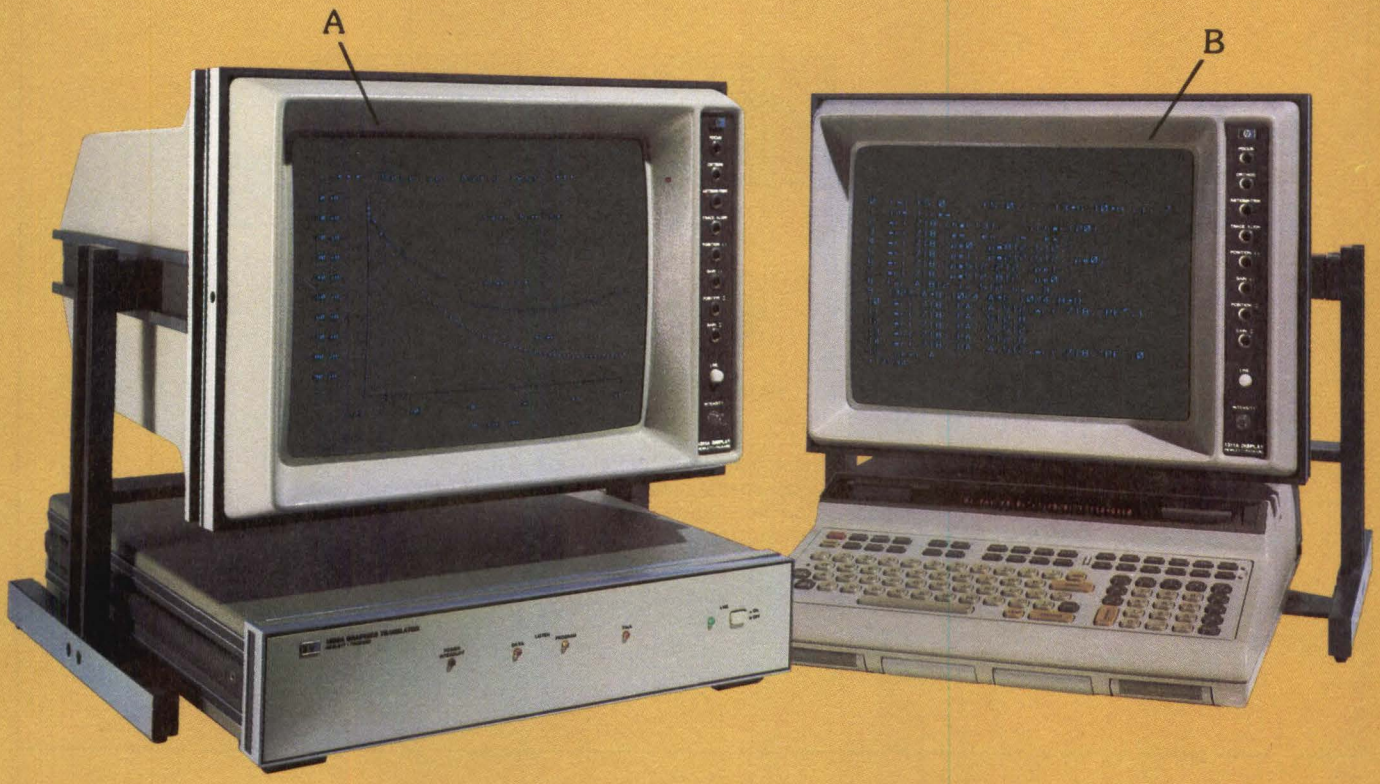

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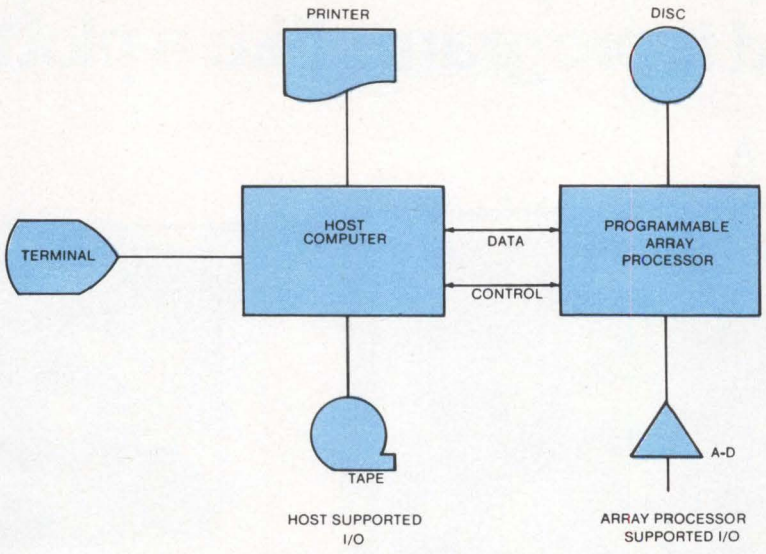

Fig 1 Array processor-host computer interactions. Programmable array processor is designed as specialized processing unit for handling scientific calculations. Communication with external devices, such as disc mass storage or A-D converters, can take place through host computer or through direct array processor I/O interface, as application mandates

In another application, large arrays of data are involved in 2-dimensional fast Fourier transforms (FFTs). Data could be stored entirely in main memory, but this would be expensive. A 512 x 512 data array, such as those encountered in video image processing, requires more than 262k words of memory. A lower cost solution is achieved by partitioning the problem so that the bulk of the data resides in less expensive disc storage with only the portion immediately needed residing in main memory.

However, going through the host computer for all main memory-disc data exchanges would be too slow to be feasible. By interfacing the array processor directly to a disc file via a programmable I/O processor (PIOP), partitioning of the problem reduces main memory requirements from over 262k words to 32k words. Although the disc is 45 times slower than the main memory replaced, execution time is only increased from approximately 1.5 s to between 6 and 7 s for almost 10M floating point operations on an array processor with a clock rate of 6 MHz and separate floating point multiplier and floating point adder hardware.

Another advantage for a direct I/O interface between the array processor and a disc file is preservation in the stored data of the extended precision offered by some array processors (eg, a 38-bit word for the AP-120B). Interface through most host computers would reduce that precision to a 32-bit word. In some applications, this can affect the accuracy of the final result by as much as two decimal digits.

Two Direct I/O Interfaces

The problem of direct I/O interfacing can be divided into a control requirement and a data transfer requirement. Control deals with regulating when, and in what manner, the array processor and an external device interface with each other; overhead is a term often associated with control. Data transfer deals with the transfer rate and the data format for communication between the array processor and a peripheral.

I/O interfacing can be provided by either fixed protocol or programmable protocol devices. In fixed protocol, the interfacing procedure is invariant. For example, addressing control may be restricted to a limited number of algorithms; data transfer protocol also follows a set format.

Programmable protocol interfaces, by comparison, provide programmable addressing of the array processor and the peripheral device. This programmability means that even random addressing of data sources and data destinations can be performed. Likewise, the method of data transfer is programmable. Programmability is accomplished with a microprocessor that has been optimized to perform both addressing and control functions between the array processor and the external device.

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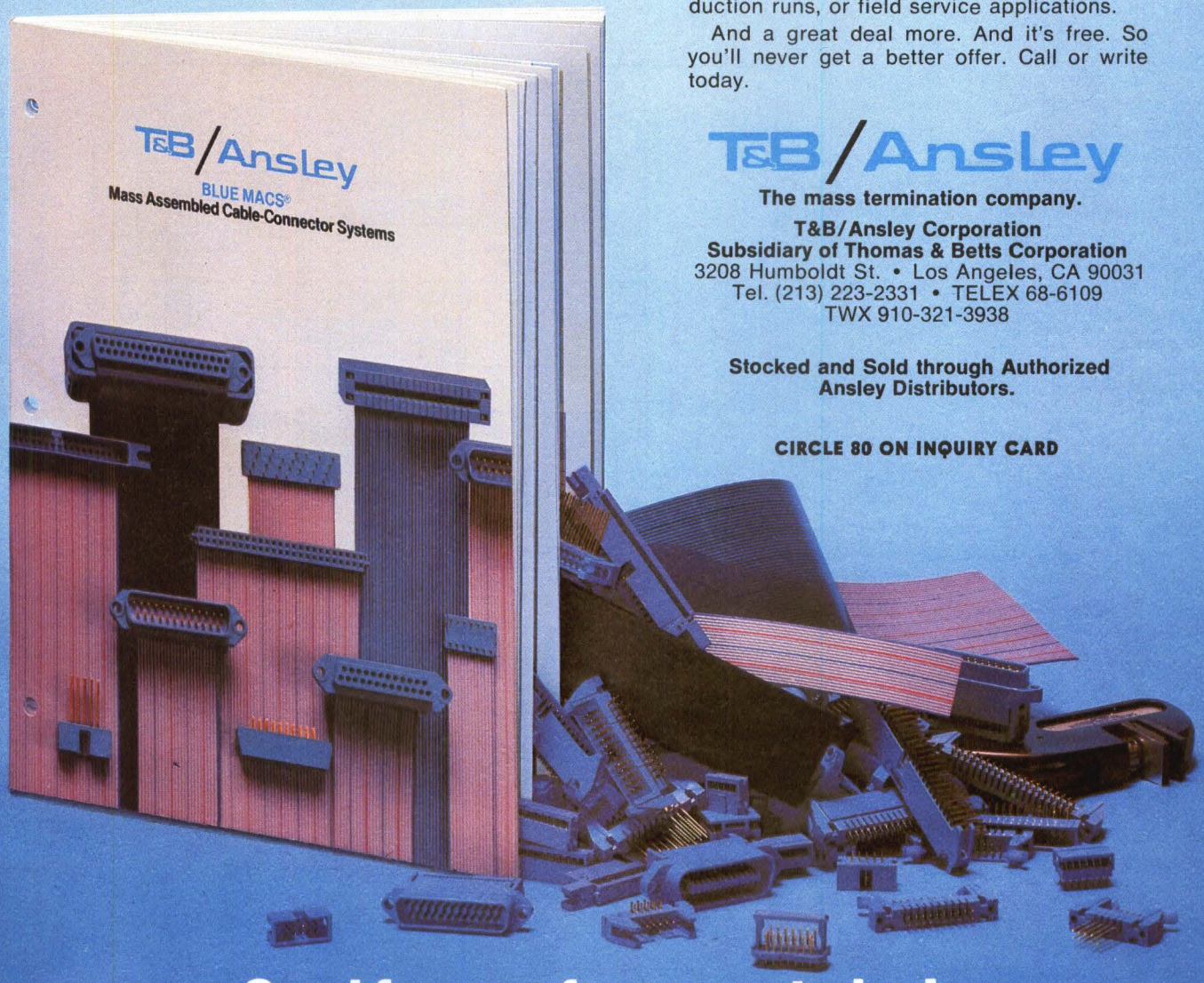

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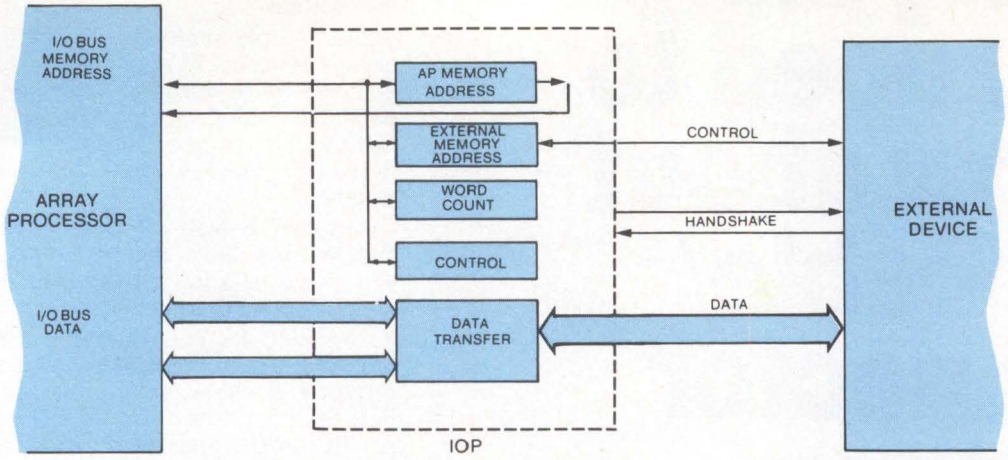

Fig 2 I/O processor. IOP provides a direct interface between array processor and peripheral device via DMA channel. Initialization of I/O operations in this approach must be supplied by array processor or peripheral

The tradeoff between fixed protocol and programmable protocol interfaces is essentially price versus flexibility. Low cost is the hallmark of the fixed protocol interface, but the peripheral device is constrained to match the protocol of the interface. While costing more, the programmable protocol interface is able to accommodate a wider range of peripherals.

Fixed Protocol Interface

An I/O processor (IOP) provides a fixed protocol interface between the array processor and a peripheral device (Fig 2). Control of data transfers, on a direct memory access basis, can be exercised by either the array processor or the peripheral. Transfers are initiated by simply loading the appropriate words into the four IOP control registers. Data transfers occur simultaneously with calculations being performed in the array processor. Transfer rates are up to 1.5M words/s into the array processor, and up to 1.2M words/s out of the array processor.

Both 16- and 38-bit versions of the IOP are available. For the former, data are transferred to or from the 16 least significant bits of the mantissa of the array processor data word. In the latter, the array processor's full 38-bit floating point word is transferred.

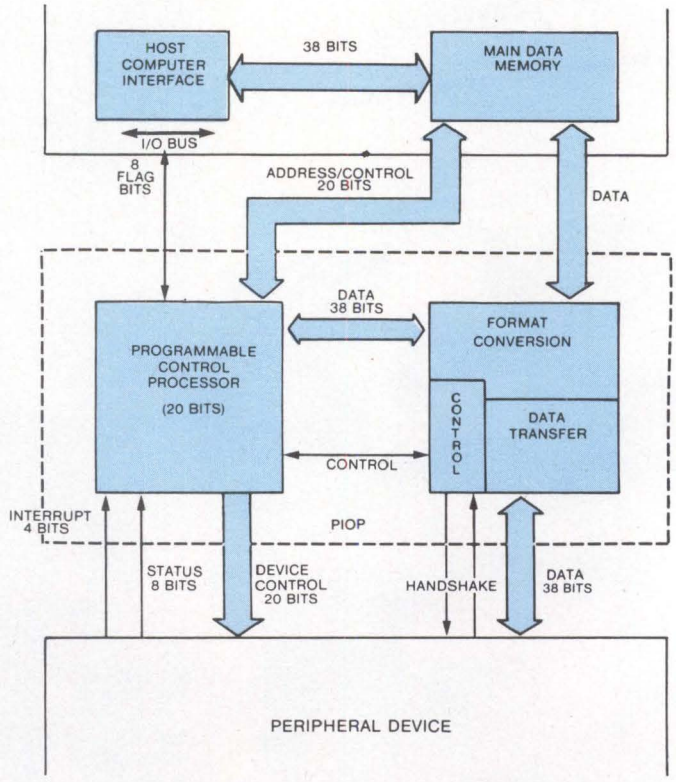

Fig 3 Programmable I/O processor. PIOP adds built-in controller to capabilities of basic I/O overhead in array processor and provides control for peripheral operation, besides serving as direct I/O interface

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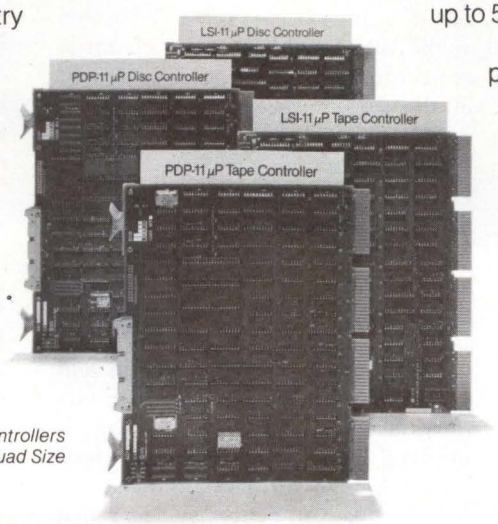

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CIRCLE 81 ON INQUIRY CARD

Programmable Protocol Interface

A PIOP furnishes a programmable protocol interface between the array processor and an external device (Fig 3). While retaining the basic IOP capabilities, the PIOP adds a programmable control processor, such that control overhead is not imposed on the array processor or the peripheral. Maximum data transfer rate varies from 2M to 3M words/s and is the same for either direction. The actual transfer rate may be degraded by the control protocol of the peripheral.

A 20-bit microcomputer, using five AMD2901 4-bit slice microprocessors, serves as the PIOP controller. Driving the microprocessor with the 6-MHz clock of the array processor results in a 167-ns instruction cycle time. The PIOP instruction set includes the full AMD2901 instruction set plus additions to improve data transfer and control efficiency.

Four priority encoded, individually controllable interrupt traps are available in the PIOP. They can be enabled, disabled, or independently recovered, resulting in a low overhead technique for responding to individual device requirements. These interrupts also offer a means of interfacing to devices requiring independent control of input and output data streams.

Three levels of programming are provided for the PIOP. In the first level, the PIOP program assembly language, symbolic programming of the 38-bit instruction word can be accomplished. This level of programmability is indispensible for controlling a unique external device or for performing peripheral processing functions with maximum throughput in time-critical data transfer operations.

A second programming level is the programmable I/O channel (PIOC). Similar to macro level programming, PIOC directs the PIOP to perform many I/O operations without resorting to detailed programming in the PIOP assembly language. This capability is primarily developed for use with disc memory. The PIOC operates by interpreting programs made up from 20 basic operating instructions and stored in array processor main memory. Absolute, direct, and indirect address modes are all allowed in PIOC instructions.

The third level of programming the PIOP is via FORTRAN calls. This higher level language approach, while lacking the capability for detailed PIOP control of the other two modes, requires minimal system design effort. With a set of 15 FORTRAN calls, the system designer is able to communicate with, test status of, and control the PIOP for predefined data transfer operations.

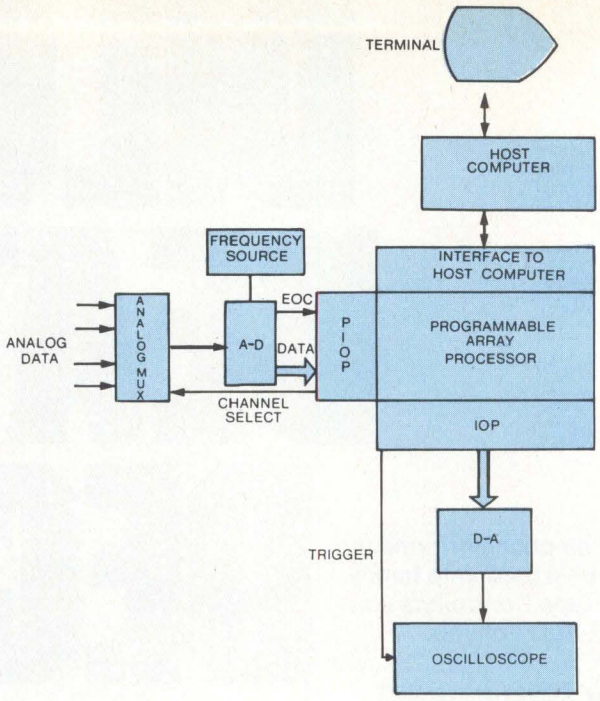


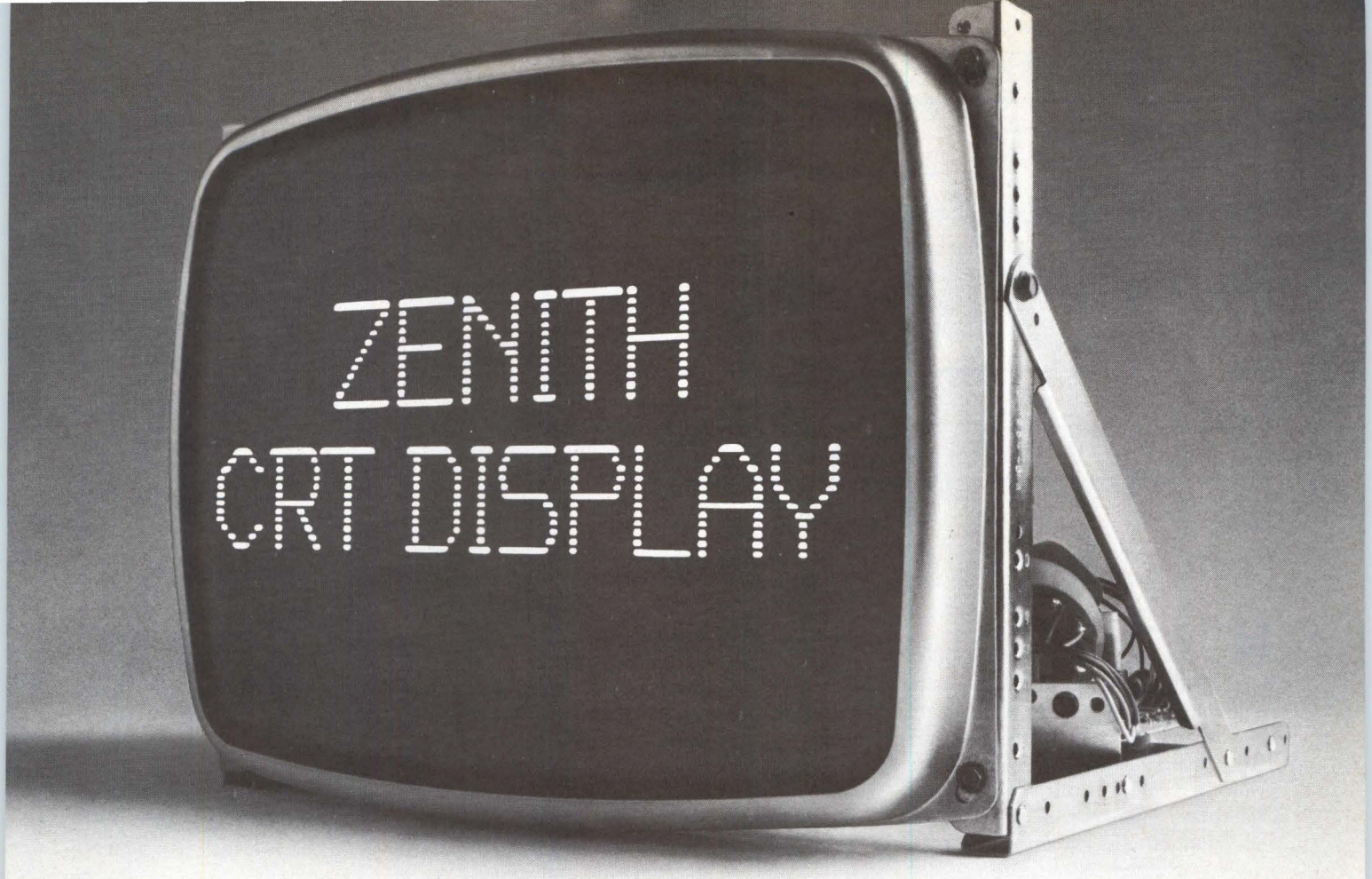
Fig 4 Realtime process control application. In this multichannel data acquisition system, PIOP provides control of analog multiplexer, as well as serving as direct I/O interface

Application Example

A realtime control application defines the role typically played by direct I/O interfaces (Fig 4). In this application, multiple data channels are acquired, each channel processed in the array processor, and the results displayed on an oscilloscope. The multiple data channels are analog multiplexed before being fed through a single A-D converter to the array processor. An external frequency source governs the A-D conversion rate. Connected between the A-D converter and the array processor, the PIOP handles data conversion and also controls the external data acquisition process. The process is initiated by the PIOP's selecting which input channel of the multiplexer is fed to the A-D converter. The end of conversion flag of the A-D converter is tied to an interrupt of the PIOP and directs the PIOP to initiate a data transfer to the array processor. Upon completion of data transfer, the PIOP issues a new channel select command to the multiplexer and waits for another conversion to take place. Because the PIOP drives the channel selection process, synchronization is automatically maintained, and complex data acquisition algorithms can be easily implemented in this manner.

When the array processor has finished calculations on the acquired data, results are output to the oscilloscope through a D-A converter. Since needed control is less complex, an IOP is used for this interface.

Although programs for the entire process are initially input to the array processor through the host computer, the host plays no direct part in the actual realtime process; therefore, process rates can be much faster. The array processor supports simultaneous data acquisition, processing, and display. This frees the host computer to perform higher level analysis on the processed results from the array processor. □



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CIRCLE 82 ON INQUIRY CARD

TECH BRIEF

Synchronous Transfer Circuits For Redundant Systems

Circuits efficiently transfer control to surviving components after a failure

New circuit arrangements for flipflops, counters, and clock drivers in redundant systems ensure that control is synchronously transferred to surviving components when a failure occurs. In addition to their original application to spacecraft systems, the redundant circuits should have terrestrial uses in power generators, solar energy converters, computers, vehicle controllers, and other systems demanding high reliability.

The two clock-driver modules [see (a)] are synchronized in phase and frequency so that if one of the modules fails, the output signal is virtually unaffected. The arrangement consists of two astable multivibrators, with their outputs in an ac coupled diode OR function so that only the output signal from the surviving module is transmitted. The synchronization and phase forcing are exerted through the common impedance R_1 and R_2 and will occur provided the frequency difference is not too great (within about 10%). Resistors R_1 and R_2 have high values so that if one fails, the effect on the frequency of the surviving module is minimal.

The redundant counters [see (b)] are arranged so that they cross-reset each other periodically. A "clear" signal is transmitted through one of the 4-input OR gates only when all of the outputs of one counter reach zero. When this happens, the output of the other counter is reset to all zeros, bringing both counters into synchronization. The counter outputs are coupled together by ac coupled diode OR gates. If one fails, the other takes over without losing count.

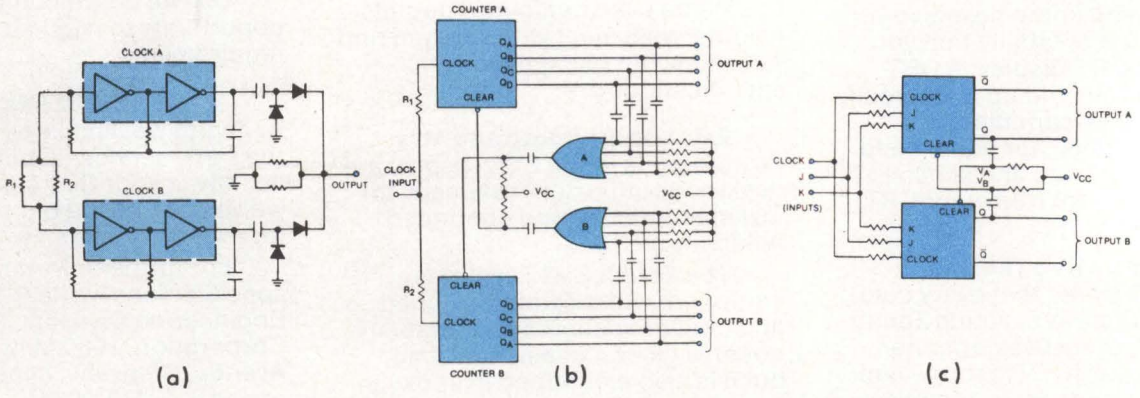
The Q output of one redundant flipflop [see (c)] is coupled to the "clear" input of the other, forcing synchronous operation of both. When flipflop A is reset ($Q = 0$), V_A activates the "clear" input of flipflop B and resets its Q output to zero. Similarly, if flipflop B is reset before flipflop A, a signal at V_B resets flipflop A.

Note

This work was done by Satoshi Nagano of Caltech/JPL. For further information, write to: John C. Drane, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103.

Patent Status

Inquiries concerning rights for the commercial use of this invention should be addressed to the Patent Counsel, Monte F. Mott, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. Refer to NPO-14162.



Clock driver (a), counter (b), and flipflop (c) circuits. Synchronous transfer of control from one element of redundant pair to another is made possible by circuits that interconnect elements. Outputs would be coupled through OR gates (shown only for elements in (a) which use diode OR gate)

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CIRCLE 83 ON INQUIRY CARD

TECH BRIEF

Noise Tolerant Computer Link

Bit data are transmitted serially over long distances, using a bidirectional computer-to-computer link

An inexpensive computer-to-computer link (Fig 1) that facilitates data communication in electrically noisy environments provides simultaneous 2-way communication over two coaxial cables, for distances up to 1000 m. Data are encoded into a form of pulse code modulation in which bit values of 1 or 0 are coded by either the presence or absence of a data pulse. Each bit period is divided into two subperiods: a clock subperiod that signals the start of the bit period, followed by a data subperiod.

In Fig 2, the clock pulse is 400 ns wide, and the data period is 1200 ns.

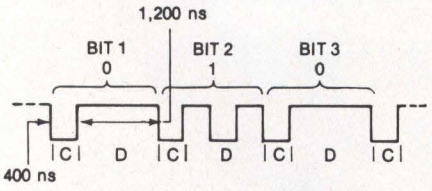

Fig 2 Modulation code. Code is sent as alternating clock (C) and data (D) periods

If a 400-ns pulse is inserted in the data period, it represents a logical 1; if no pulse is inserted, it represents a 0. The width and duty cycle of the pulses are chosen so that transient charge on the coaxial line has enough time to decay after a pulse before the next pulse comes along, and a filter has time to remove transient errors from pulses.

Selection of duty cycle and pulse repetition rate to permit the coaxial cable to return to a normal state between pulses eliminates the need for a bipolar signal. Optical isolators ensure that common mode noise is not a problem in transmitting the single-ended signal.

An interface connects the computer to the transmitter section of the link. A first in, first out (FIFO) data buffer is filled with data from the computer under the supervision of the FIFO input control.

On receipt of a transmit command, the transmitter output control/data formatter orders data to be read out of the FIFO buffer and sent over the link. (The host computer may enter data into the FIFO while the link removes data.)

At the receiving end, the signal passes through the isolation and filtering circuits and is split back into data and clock pulses. The output clock strobes the data bits into a serial-to-parallel shift register. The parallel data are scanned for a synchronization word, and if a word is found, the sync detector latch is set, and the data word is strobed into the receiver FIFO buffer. If the input data stream vanishes for a preset time period, the sync detector latch is cleared. Parity errors are reported to the host interface.

Note

This work was done by Michael W. Sievers of Caltech/JPL. For further information, write to: John C. Drane, NASA Resident Legal Office-JPL, 4800 Oak Grove Dr, Pasadena, CA 91103. (NPO-14152)

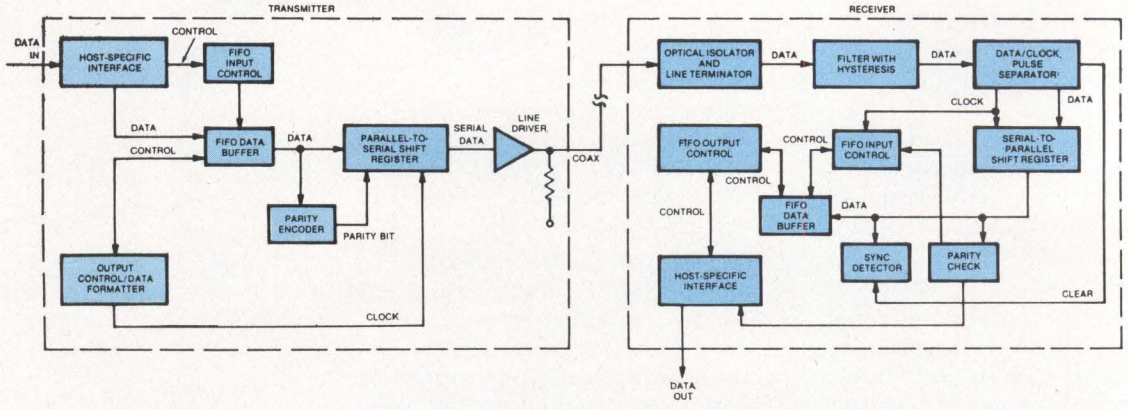

Fig 1 Computer to computer link. Transmitter and receiver communicate serially over coaxial line

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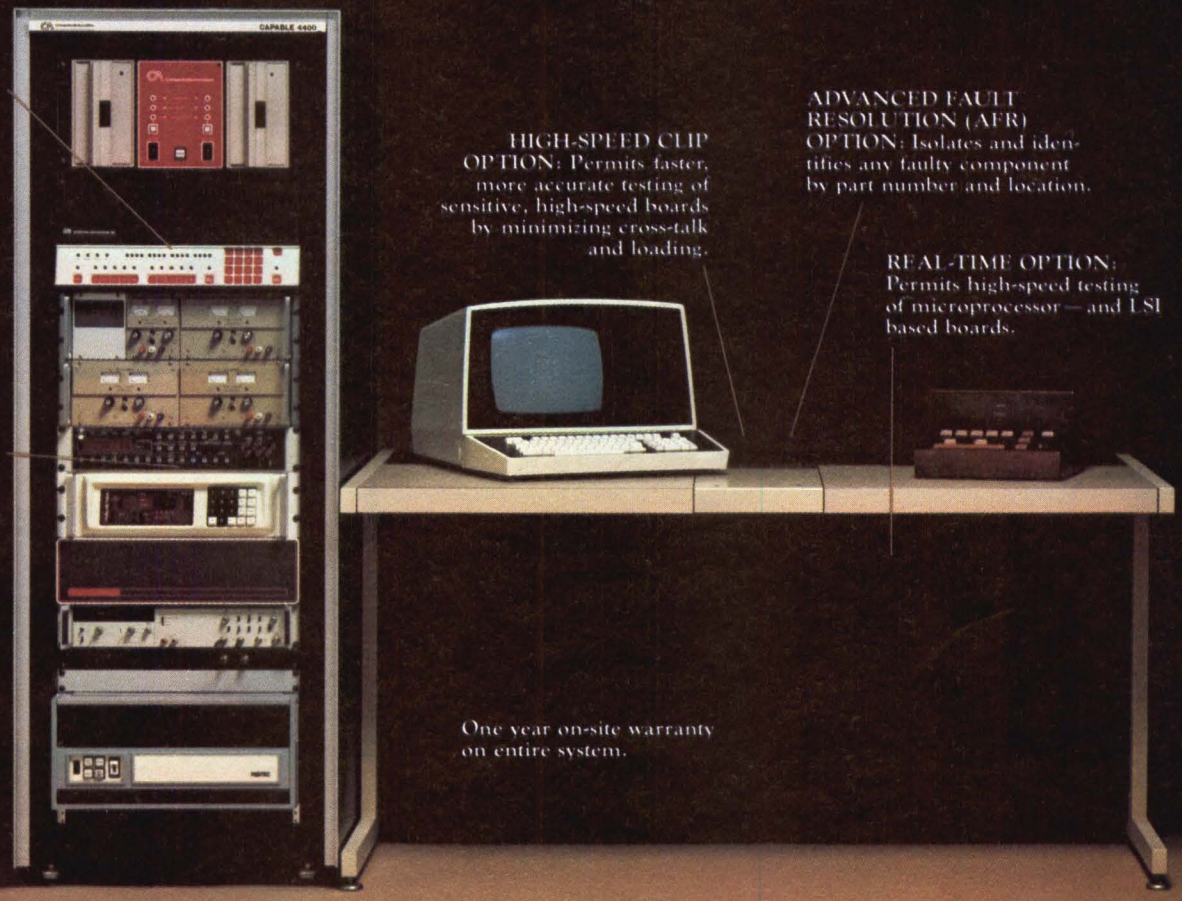

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CIRCLE 84 ON INQUIRY CARD

INTERFACING FUNDAMENTALS: AN INTRODUCTION TO THE MOTOROLA MICROPROCESSOR/MICROCOMPUTER FAMILY

Andrew C. Staugaard†
Jamestown Community College

Christopher A. Titus and Jonathan A. Titus
Tychon, Inc

David G. Larsen and Peter R. Rony
Virginia Polytechnic Institute and State University

While the primary emphasis of this column has been the Intel 8080 family of devices and software, there is sufficient interest in and use of the Motorola 6800 family—a complete line of software compatible chips developed around its standard 6800 architecture—to warrant its discussion. This family ranges from the MC6809, an advanced microprocessor with enhanced instructions and addressing modes over those of the 6800, to a complete single-chip microcomputer, the 8-bit MC6801. This broad span of software compatibility, which is not currently available within the Intel 8080A chip family, is highly desirable for serving a wide variety of application requirements. Dedicated to a continued expansion of the 6800 family, Motorola plans to provide a steady flow of new and related family products to guard against chip family obsolescence. Such a commitment was one of the important reasons for the decision by the three major automobile manufacturers to incorporate the 6800 family of microprocessors/microcomputers into their automobiles; this will help to increase the availability and decrease the expense of the 6800 family.

Each of the major central processing unit (CPU) chips within the family will be mentioned briefly; hardware and software features of each will be described in detail in later columns. Fig 1 summarizes part of the 6800 family, which has many more chips than are indicated.*

The place to start a discussion of the 6800 family is with the 6800 chip, which is the basic hardware and software model for most of Motorola's microprocessor/microcomputer chip line. All of the newer microprocessor and microcomputer chips—including the 6801, 6802, 6803, and 6809—utilize the fundamental 6800 architecture within their CPU logic to maintain compatibility. Many of the company's future chips are expected to be hardware and software compatible with the 6800, as well.

The 6800 is a n-channel 40-pin metal oxide semiconductor large scale integrated circuit that operates on a

†Andrew Staugaard is an assistant professor, currently working on a text entitled *6800 Programming and Interfacing, with Experiments*, excerpts from which will appear in this and the next several columns.

*The reader is encouraged to consult *The Complete Motorola Microcomputer Data Library* from Motorola Semiconductor Products, Inc, Phoenix, Ariz, 1978, for a full listing and description of all current 6800 family chips.

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CIRCLE 85 ON INQUIRY CARD

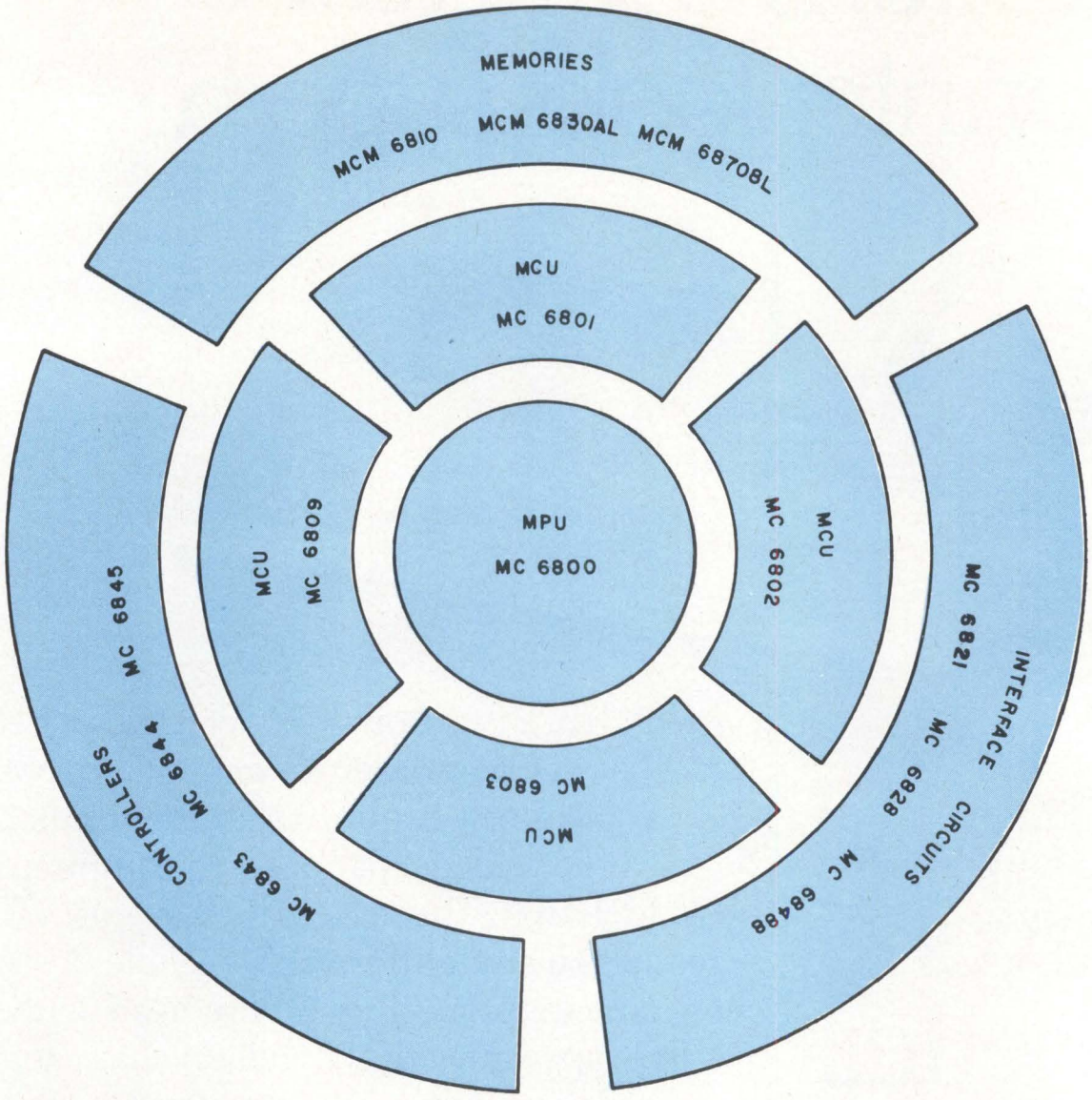
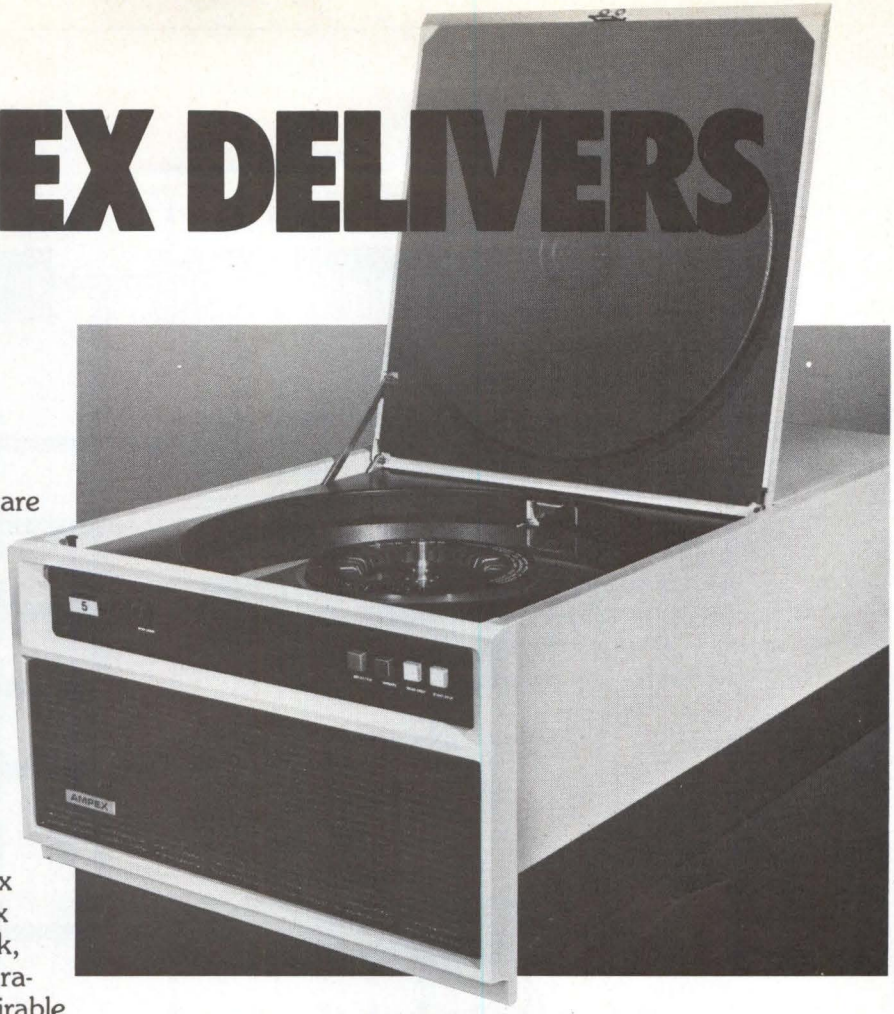


Fig 1 6800 chip family. Software compatible components fit into various categories, covering spectrum of microprocessors, microcomputers, memories, interface circuits, and controllers. This offers sampling of chips; many others are also available

single 5-Vdc supply. It is an 8-bit microprocessor that utilizes 72 fundamental instructions and 6 addressing modes to provide a total of 197 instructions. Fig 2 provides a complete 6800 functional block diagram, showing all of the external connections to the chip, the associated pin numbers, and the functional internal registers. Note that the 6800, like the 8080A and 8085, contains a 16-bit address bus, an 8-bit bidirectional data bus, and a variety of control signals. Unlike the 8080A and 8085, the 6800 contains two accumulators and a 16-bit index register, which are used with the appropriate instructions to provide some very interesting software features. Also, unlike the 8080A and 8085, the 6800 provides for the automatic "stacking" of internal register contents during interrupts. The 6800 family treats each input/output (I/O) device as a memory location (memory mapped I/O), since separate I/O commands—such as IN and OUT for the 8080A —are not available. In some cases, memory mapped I/O operation simplifies I/O control and software.

The 6802 is a 40-pin 8-bit microprocessor chip that contains the same types of internal accumulators and registers as the 6800. In addition, the 6802 contains an internal clock oscillator/driver and 128 bytes of read/write memory, located between hex addresses 0000 and 007F. The information stored in the first 32 bytes of this memory are retained in a power-down situation by utilizing

AMPEX DELIVERS



Ampex disk storage modules are both interface and *media* compatible with CDC's 9760 and 9762. And Ampex 40 and 80 megabyte SMDs offer a unique advantage over the CDC equivalents—they both can grow to a capacity of 160 megabytes with a simple field modification.

You'll find a lot more than CDC-compatibility when you look into the Ampex storage module family. Ampex can package your drive in rack, console or "Tempest" configuration, and can deliver such desirable features as variable sector format, address mark capability and on-track head servoing. The transfer rate is 1.209 megabytes per second, and access time average is 28 milliseconds.

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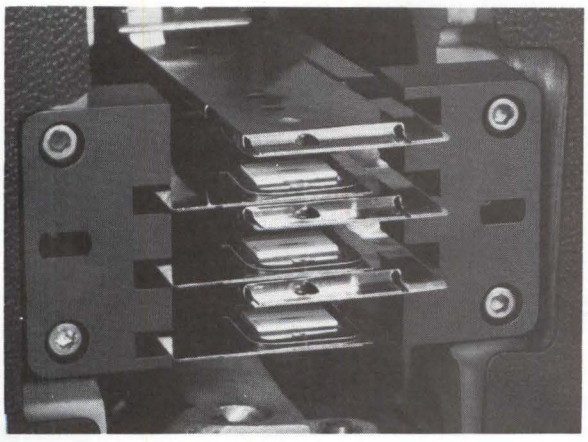
Other Ampex disk storage modules provide capacities of 100, 200 and 300 megabytes, and within a given family, you can begin with the minimum storage and upgrade to a higher capacity right in your own facility. For those with super special data needs, Ampex even has a 300 megabyte module with a parallel transfer rate of 10.88 megabytes per second.



Larry Russell has the information. Call him at 213/640-0150, and he'll prove that now there are twice as many ways to get the SMD capacity you need when you need it. Technical information and performance data is complete, and free. Write to Ampex Memory Products Division, 200 North Nash Street, El Segundo, California 90245. Immediate delivery is only a P.O. away.

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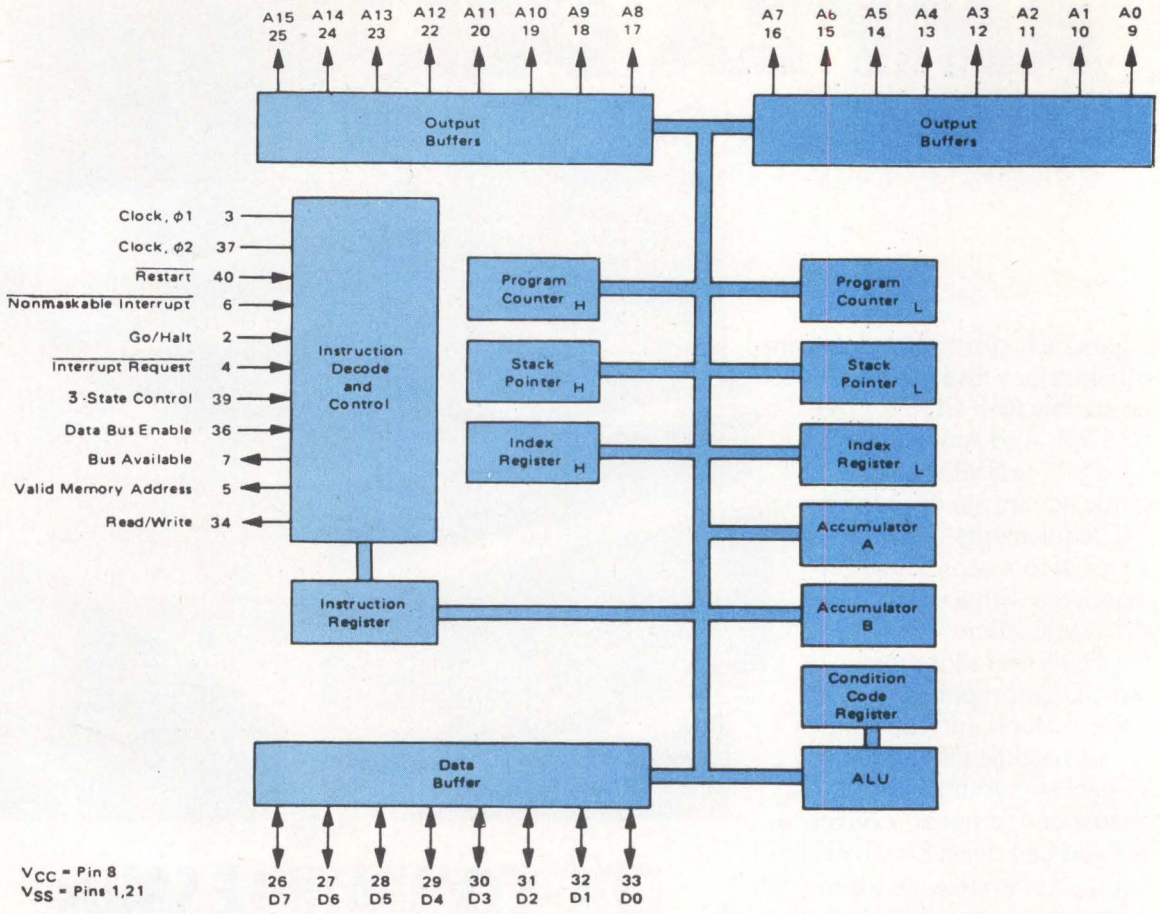

Fig 2 Expanded block diagram of 6800 microprocessor. Basic microprocessor contains similarities to 8080A and 8085—16-bit address bus, 8-bit bidirectional data bus, and control signals. Dissimilarities are that 6800 provides two accumulators, 16-bit index register, and automatic stacking of internal register contents during interrupts

the V_{cc}-standby function of the chip. This microprocessor is completely compatible with the 6800 and all of the latter's peripheral I/O features. There is very little difference between the pin assignments of the two chips, and an existing 6800 system can be easily modified to accept the 6802 chip.

The 6809, a product of very large scale integration (VLSI), adds an 8-bit direct page register for memory paging in the direct addressing mode—a new type of addressing mode—as well as a second 16-bit index register and a second 16-bit stack pointer. Also, the two accumulators can be combined through software operations to form a single 16-bit accumulator, thereby supporting 16-bit operations. Some 6809 programs require less than two-thirds as much memory and run faster than similar 6800 programs. For flexibility, it is offered as an onchip clock version (6809), as well as an offchip clock version (6809E). The former is ideal for small system applications, while the latter provides the additional signal lines required in larger systems for processor status information.

Another VLSI product, the 6801 is 100% software and bus compatible with all of the other 6800 family microprocessors, memories, and peripheral interface chips. The device can be operated as a single-chip microcomputer, or its memory can be expanded to 64k bytes. It not only utilizes the standard 6800 CPU architecture, but also allows for the software combination of the two 8-bit accumulators to form a single 16-bit accumulator, as was done in the 6809. In addition to the basic 6800 instruction set, there are 10 additional 16-bit instructions, including an 8-bit by 8-bit multiply instruction that yields a 16-bit result.

Fig 3 shows a functional layout of the 6801 chip. Note that there are 128 bytes of onboard read/write memory, of which 64 bytes are maintained in a standby mode similar to that on the 6802. The 6801 also contains an onboard 2k-byte mask-programmable read only memory (ROM). Naturally, the ROM based 6801 requires a relatively large and expensive custom order. However, an electrically programmable ROM version is also available,

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George Groth — *Unitote-Regitel V.P., Engineering*

"When you make point-of-sales systems for retail stores, your customers won't tolerate excessive downtime. And, since our reputation as a P.O.S. system pioneer is in the balance, we make doubly sure our System 430 has a synchronous tape drive that will last.

Unitote, a Digi-Data user since 1963, faced a decision to consider switching to another tape drive used by Regitel, a company acquired in 1972. However, when actual field service records for both tape drives were compared head-to-head, Digi-Data was selected. Continuing field records now show that the actual 41-month MTBF of the Digi-Data drive achieves a 33% edge, while the Formatter's 60-month MTBF was 2½ times better than the other tape drive.

This MTBF advantage, plus prices under competitive drives made Digi-Data the clear-cut choice for all three Unitote-Regitel systems. Five different Digi-Data drives are used . . . each at a remote (in-store) or main (multi-store) central processor where reliability is paramount."

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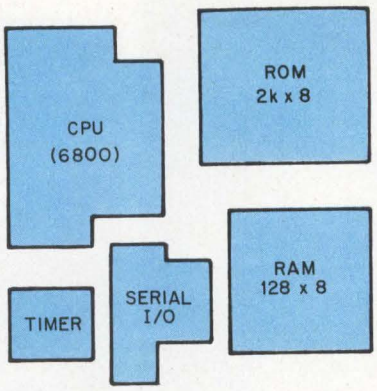

Fig 3 6801 microcomputer chip layout. This version includes 128 bytes of RAM and 2k bytes of ROM; also available is version with EPROM. If necessary, another alternative is offered with either EPROM or ROM function disabled

the MC68701. In addition, the 6801's capability can be used without either ROM or EPROM with the addition of the MC6803, which is the version of the 6801 in which the ROM or EPROM function has been disabled.

Some other significant features of the 6801 include an onboard universal asynchronous receiver/transmitter (UART), an onboard 16-bit timer, and a 4-bit I/O port. The UART, which is used for serial data communications, provides full- and/or half-duplex operation in two formats: mark/space operation for standard interfaces, and biphase operation for use between processors. The UART also provides four different software selectable bit transfer rates. The 16-bit timer has three independent timing functions, which may be used in applications that require very accurately timed periods. The 4-bit I/O port contains an associated data direction register, which permits each I/O line to be separately programmed as either an input or an output line.

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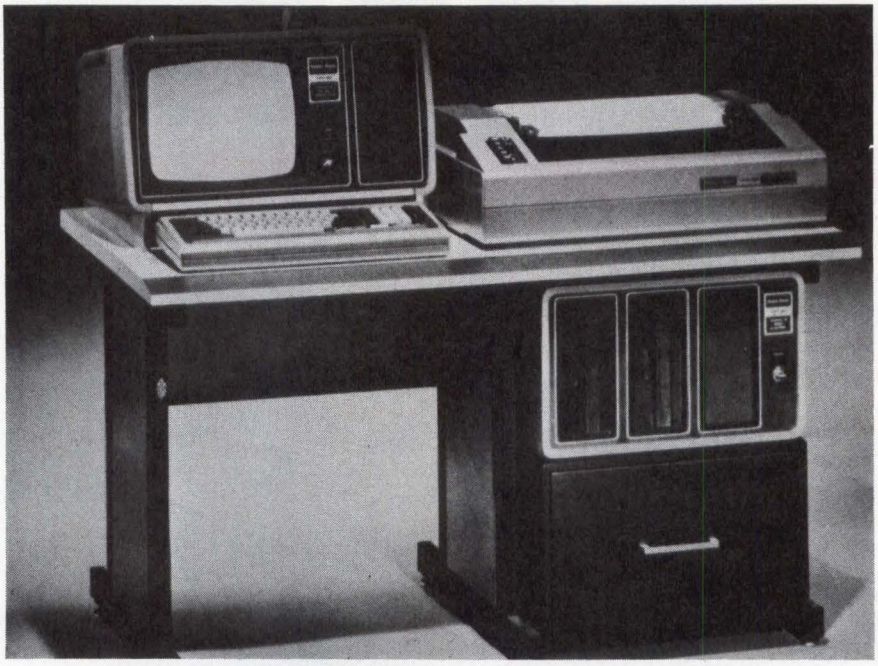
Increased Capacities and Doubled Computing Speed Of Microcomputer Extend Application Areas



Desktop computer package encloses CRT and floppy disc drive; even 3-disc drive expansion system can be integrated into Radio Shack's TRS-80 Model II. Minicomputer capabilities—enhanced facilities of original TRS-80—suit small business applications at microcomputer price

To bridge the gap between personal computers and low end commercial machines, Radio Shack, a division of Tandy Corp, Fort Worth, TX 76102, has announced the TRS-80 Model II with capabilities to perform as a general purpose data processor, an intelligent terminal, or a word processor. Software is available for general ledger, accounts receivable, inventory control, mailing list management, and payroll; others to follow are word processing software and specific application packages.

The multiple function machine's basic capabilities are intended to begin where the original TRS-80 approaches its upper limits. Implementation of LSI devices—CPU, RAM, keyboard display and floppy disc controllers, serial and parallel I/O ports, and DMA—has resulted in pricing that starts at $3450 for the 32k RAM, 1-disc system. In addition, the technology provides added reliability.

The computer is built around a high speed 4-MHz, 8-bit Z80 microprocessor with a 32k- or 64k-char RAM that operates at twice the speed of the Model I. DMA increases throughput by controlling the data transfer between memory and disc, allowing the CPU to perform other tasks simultaneously. All I/O operations are vector-interrupt driven.

One built-in 8" (20-cm) floppy disc stores 0.5M bytes, including the disc operating system. This is 100k characters more than the original system with four mini-disc drives. Addition of one to three disc drives gives a total capacity of 2M characters online.

The high resolution 12" (30.5-cm) video monitor displays 24 lines by 80 characters (or 40 expanded characters) in upper and lower case letters. This doubled capacity enhances productivity for such applications as financial reports, word processing, and software development. The 76-key keyboard with 10-key numeric pad offers such functions as control, escape, caps, hold, repeat, and two software programmable special function keys. The keyboard may be detached and moved, as desired.

Further expansion is designed into the system in the form of two RS-232-C channels and one Centronics parallel port. Also four plug-in slots and available power for other PC boards facilitate addition of options and peripherals.

A Level III version of the TRS-80's Level II BASIC and TRSDOS operating system are automatically loaded into memory when the machine is turned on. On power-up, the computer thoroughly tests itself to insure proper operation. The program can appear immediately without involving intermediate steps.

Two line printers for use in conjunction with the computer are the TRS-80 Line Printer II and III. Version II is a 15 x 11 x 15" (38 x 28 x 13-cm) unit that prints 50 char/s on 8" (20-cm) lines of 80 char each, on 9.5" (24-cm) continuous forms. Expanded letters are printed under software control. It prints a 7 x 7 dot matrix, upper/lower case, in friction and pin feed modes. Price is $999.

The wide carriage version III prints 9 x 7 dot matrix upper and lower case characters at a rate of 120 char/s, producing 13" (33-cm) wide, 132-char lines. Other features of the $1999 unit are printing in both directions, accurate positioning of preprinted forms, adjustable tractor feed, and expanded characters.

Circle 420 on Inquiry Card

Workstation Adds Modules to Build System Configurations

System 2500 is a modular, diskette based line of office computers that offer configurations to meet specific small- and medium-sized business operations. The basic workstation includes the processor, typewriter/10-key numeric keyboard, 1024-char video display, single-density disc controller, 8k-byte memory (expandable to 32k), power supply, and ACL

TRANSMISSION:
Page; Field; Modified Field; Prompted Transmission; Device Status; Function Keys.

INTERFACE:
EIA RS-232; Current Loop; 17 data rates (switch selectable) including 19, 200 chars/sec; Half duplex support; Line turnaround characters; Reverse channel.

EDITING FUNCTIONS:
Insert/Delete line and character; Columnar Tabbing; Cursor Addressability; Cursor Sense; Numeric Only fields; Security fields; Erase Variable/ Protected fields.

OPTIONS:
Buffered Printer Interface (RS-232 and parallel), separately addressable from the CPU; Standard Polling; Paging.

KEYBOARD:
Removable, solid state with international character layouts.

VIDEO:
Normal; Reverse; Blink; Low/half intensity; Underline.

When it comes to flexibility, the Infoton 400 Data Display terminal can hand you all you need.

Designed around the Z-80 microprocessor, it offers complete control of all Blocking and Editing functions through software settable modes. One thing that's especially easy to handle about the I-400 is that it's the most versatile terminal you can get your hands on for the price.

More information on the I-400 is quickly within your grasp. Call Infoton toll-free today at (800) 225-3337 or 225-3338. Ask for Barbara Worth. Or write Barbara Worth today at Infoton, Second Avenue, Burlington, MA 01803. We have offices throughout the United States, Canada and Europe. In Canada, contact Lanpar Limited, 85 Torbay Road, Markham, Ontario, L3R 1G7. (416) 495-9123.

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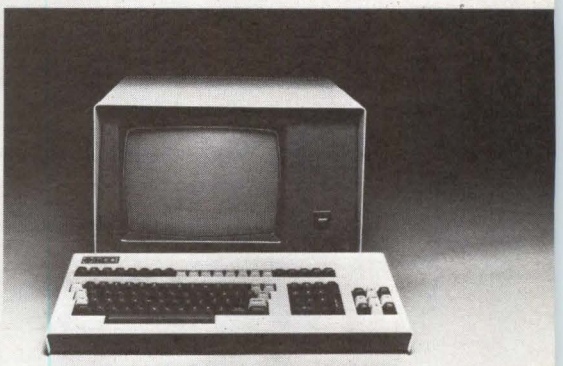


INFOTON 400

CIRCLE 90 ON INQUIRY CARD

interpreter. A 50-char/s printer is also available. With field installable modules, the system can grow to 32k bytes of memory, 4M bytes of diskette storage, and 300 lines/min of printed output.

Standard specs are a 12-bit microinstruction, 125-ns instruction cycle, 600-ns memory cycle time, and eight interrupt levels. The communication controller features IBM 2780 emulation, auto answer, and a baud rate of 1200 to 2400. Operational requirements are 115/220 Vac ±10%, 750 VA typ, and operating temperature of 10 to 37 °C.

Diskettes supported by the system offer a data transfer rate of 200k bytes/s, full diskette readtime of 30 s, full diskette writetime of 45 s, full diskette copy of 75 s, average access time of 260 ms, and 128-byte record length. Up to four drives provide direct access to 4M bytes. Three formats that can be mixed on one station are the 250k-byte IBM 3740 compatible format, the company's 500k-byte double-density format, and their 1M-byte double-density, double-sided format.

The 9" (23-cm) video display unit handles 16 lines of 64 upper and lower case characters. It guides the operator during startup and program execution, in addition to providing visual access to all online files. Keyboard input is overlapped with other I/O operations and simultaneous processing; 12 programmable function keys are included. The acoustical feedback signal for each keystroke is operator adjustable. Various international character sets are supported.

Ranging from a powerful operating system and translators to debugging functions and utilities, the software is based on a business oriented language, ACL (Application Control Language), originally developed by IBM for the 3741 programmable workstations. Features are symbolic names and labels, edit functions, I/O macroinstructions, extended table operations, I/O formatting, and straightforward program logic coding. Daisy Systems Holland B.V., Nieuweweg 279, Postbus 125, 6600 AC Wijchen, Holland, offers application packages as well.

Output is obtained from one of three printers, all of which print 132 char/line on one original and up to five copies. The M50 is a 50-char/s bidirectional printer with 45-in (114-cm)/s tabulation, 96-char interchangeable printwheel, and snap-on ribbon cassette. An automatic sheet feeder is also offered. The M-165 matrix serial printer permits 165-char/s bidirectional printing. High speed tabulation, simultaneous paper feed, and bidirectional tractor feed are standard. The final offering is the P-300 matrix line printer, operating at 300 lines/min. It features a 13.2" (34-cm) printline and 16" (41-cm) max forms width.

Circle 421 on Inquiry Card

Turnkey System Is Cost-Effective For Smaller Businesses

Portability, accessability, and affordability—features of the Apple II Computer—have been enhanced with business software to produce the Apple II Business System. Businesses ranging from small proprietorships to major corporations can benefit from the new business software programs and configurations. The latest low cost system, which lists for $4995, includes the Apple II Plus Computer with 48k bytes of RAM, two disc drives, a video monitor, printer, auto start ROM, expanded BASIC, and CONTROLLER software package. Applesoft Extended BASIC is built-in, suiting advanced arithmetic calculations and business problem solving. The autostart ROM chip provides automatic startup to run application programs, automatic disc loading as the system turns on, reset protection, and easy screen editing.

The CONTROLLER business package, which supports cash or accrual bookkeeping, is self-prompting and requires no programming knowledge. A "failsafe" feature of the data entry system signals typing errors with an audible warning. The system automatically copies data files and automatically prints reports before the monthly books can be closed out. Program modules are general ledger (maintains a file of 250 types of accounts with up to $99M in any one), accounts receivable (handles a file of up to 250 customer accounts and processes 1000 invoice statements/month), and accounts payable (files 100 vendors and allows 300 monthly invoices up to $99k each).

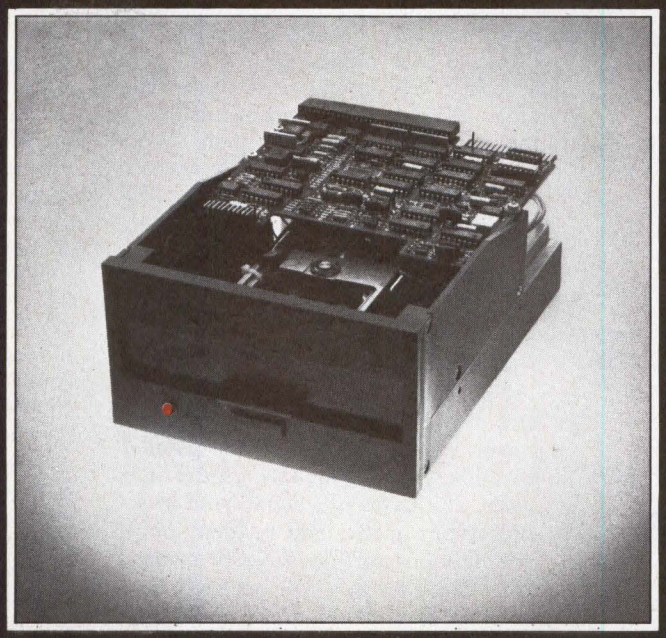
Several other programs can be added to the system for individual requirements. The Cashier is an inventory control and cash register simulation system to track customer accounts and manage inventory of more than 800 stock numbers. The Apple Post database system handles creation and maintenance of mailing lists of 500 names/diskette. Stock Quote Reporter and Portfolio Evaluator make up the Dow Jones Series that captures and processes financial wire service information.

To transform the Apple II Computer into a Pascal system, Apple Computer, Inc, 10260 Bandley Dr, Cupertino, CA 95014, in a related announcement, introduced the Language System option for developing software in that high level language. Extensions have been added to the UCSD Pascal (version 2.1) to take advantage of the computer's high resolution and color graphics, analog input, and sound generation capabilities. The efficient, readable language requires less time to write, debug, and execute and less memory space than an equivalent BASIC program. Operating with a minimum 48k disc based Apple II, the $495 package consists of a plug-in memory card; five diskettes with Pascal, Integer BASIC, and Applesoft Extended BASIC; and six manuals documenting the three languages.

Circle 422 on Inquiry Card

Dedicated Development System Handles 16-Bit Microprocessor Family

Prototype hardware and software for a broad range of 16-bit microprocessor applications—from P/ROM resident code for controllers based on the 9440 Microflame I™/9445 second generation Microflame II™ (to be introduced later this year), to real-time multitasking software for distributed processing or control—can be developed using the Microflame



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Development System. The Focus XVI™ minicomputer from Fairchild Camera and Instrument Corp, Fire Microcomputer Group, 464 Ellis St, Mountain View, CA 94042, is integrated with a 1M-byte dual-density IBM compatible floppy disc (expandable to 4M bytes) to form the basis of the system. A freestanding video display terminal and spooled 150-char/s bidirectional printer round out the system.

Focus XVI uses the company's Blaze-16 2-board minicomputer with Data General's Nova™ 3 performance; thus, users may develop applications software using the Nova instruction set. Focus XVI offers 64k bytes of dynamic RAM in a 9-slot chassis.

Assembled programs are up or down loaded into the target prototyping system over FIRELINK™. This RS-232-C communication link permits remote debugging and monitoring of execution of object code in the target hardware. With the addition of a modem/acoustic coupler, the link communicates with remote target systems or other Microflame development systems.

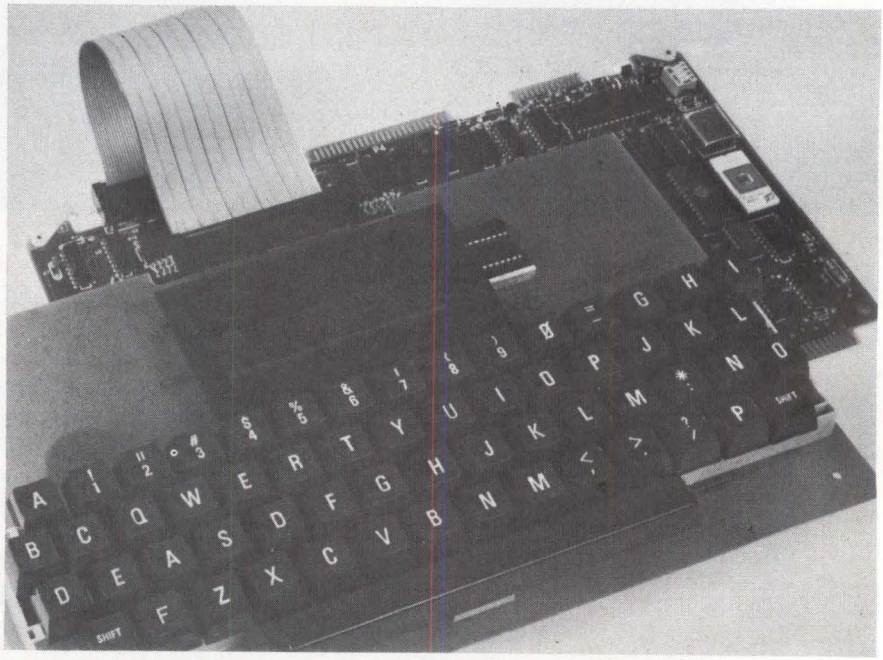
Hardware is supported by FIRE™ software, at a total system price of $23,500. FIRE-IMDOS operating system provides file management, device independent I/O, and timesharing with user supplied peripherals; software for P/ROM formatting and burning is also standard. Added features are password protection, version number control for automatic tracking and backup during debugging, and spooling capability. Among the optional high level languages are BASIC, FORTAN, and Pascal. Peripherals such as high speed readers, printers, P/ROM/FPLA programmers, modems, cartridge discs up to 10M bytes, and 80M- or 300M-byte storage modules.
Circle 423 on Inquiry Card

Total Evaluation Board Explores Features Of 16-Bit Microprocessor

Capabilities of the AmZ8000 16-bit microprocessor can be evaluated in both software development and program execution modes using the 96/4016 evaluation board. As an execution device with assemblers and cross assemblers, the unit can examine the microprocessors' execution speed and system throughput with respect to existing programs and designs. Up and down load capability exists with the Amsys 8/8 Development System recently introduced by Advanced Micro Computers, 3340 Scott Blvd, Santa Clara, CA 95051 (*Computer Design*, June 79, pp 172, 174).

The basic configuration incorporates the AmZ8000 16-bit microprocessor, 8k bytes of RAM, 24 parallel I/O lines, two RS-232-C serial I/O ports, 12k bytes of EPROM/ROM sockets, system clock, and resident monitor. Options further simplify evaluation. The first is a full decoded keyboard and 20-char alphanumeric display on a PC board that edge connects via a ribbon cable. This option, together with the EPROM resident ASCII, 1-pass, line by line assembler option, produces a mini development system. Another choice is the 95/6410 universal prototyping board with positions for up to 95 ICs, wirewrap pins at connector locations, and a plexiglass cover to protect the wirewrap side. A card enclosure mounts these boards.

Regarding I/O capabilities, one serial I/O port configures as either RS-232-C or TTY current loop interface; the other is RS-232-C only. In the Am8253 counter/timer, two 16-bit counters provide baud rates to 9600 for each serial I/O port, and the third counter is reserved for user programs. A standard CRT terminal or optional keyboard with 20-char alphanumeric display can also be directly controlled. The board is physically compatible with SBC 80 microcomputer boards.
Circle 424 on Inquiry Card



In fully assembled and tested microprocessor evaluation unit, Advanced Micro Computers integrates necessary onboard software and hardware resources to explore and use features of AmZ8000 microprocessor. Device is shown connected to optional keyboard/display unit

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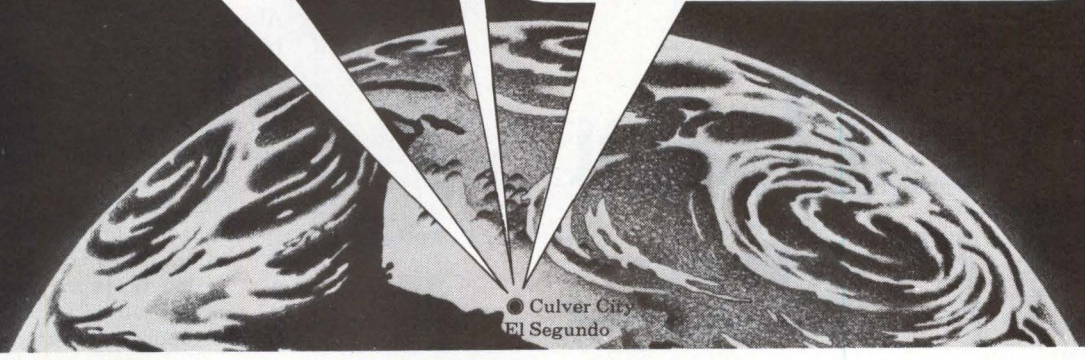

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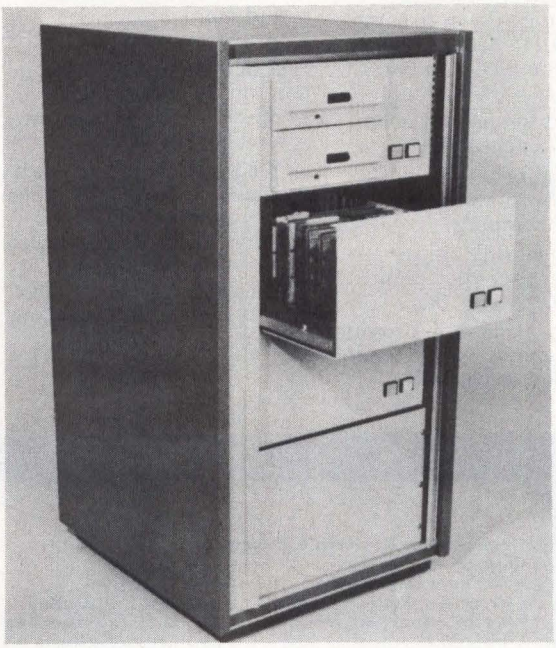
Computer With Winchester Drive Fits Between Large Disc and Floppy Systems



The C3-C multiple microprocessor computer system uses the Shugart mid-range 29M-byte Winchester disc drive, producing an alternative to the larger, more expensive 74M-byte disc offered on the C3-B. The Challenger III processor, 48k bytes of memory, and a pair of floppy discs for file backup comprise the standard configuration. The drive connects to the system via a 2-port memory which allows data transfers in and out of memory without cycle stealing from the processor. This can occur concurrent to processor operation.

Ten open slots in the unit allow for expansion. Software from the 6502, Z80, and 6800 microprocessors runs on the system. The software library includes BASIC, FORTRAN, COBOL, a word processor and information management system, and a multiuser operating system, OS-65U Level 3, which was announced by Ohio Scientific, 1333 Chillicothe Rd, Aurora, OH 44202, in conjunction with the C3-C system. Providing optimal utilization of Winchester disc based data files for information intensive small business applications, the operating system handles up to 16 independent users via dedicated memory partitions of up to 48k each. Dumb and intelligent terminals connect to the computer directly or via telecommunication links. OS-AMCAP, a small business accounting package, and OS-DMS, an information management system, can be expanded directly to multiple user operation.

Circle 425 on Inquiry Card

User Programmable Single-Chip μComputer Meets Military Specs

The M8748 8-bit microcomputer functions as a self-contained, single-chip processing and control subsystem, or it can be expanded to a larger system with additional memory, I/O, and peripheral control devices, depending on the specific military or high reliability application. Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051, screens the microcomputer to the full Level B requirements of MIL-STD-883B, Method 5004 and in accordance with quality conformance procedures of Method 5005. Temperature ranges from −55 to 100 °C.

Users who require frequent program updating can benefit from the microcomputer's 1024 x 8-bit EPROM. Also included are an 8-bit interval timer/event counter, and oscillator and clock circuits. Packaged in a standard 40-pin ceramic DIP, the unit operates on a single 5-V power supply and has a minimum instruction cycle of 4.17 μs.

Bit handling capabilities as well as facilities for both binary and BCD arithmetic suit the device to controller and arithmetic processor applications. The instruction set contains more than 90 instructions; program instructions use program memory efficiently since over 70% are single-byte and none is larger than two bytes. The interval timer/event counter allows hardware operation to replace many software counting and timing operations.

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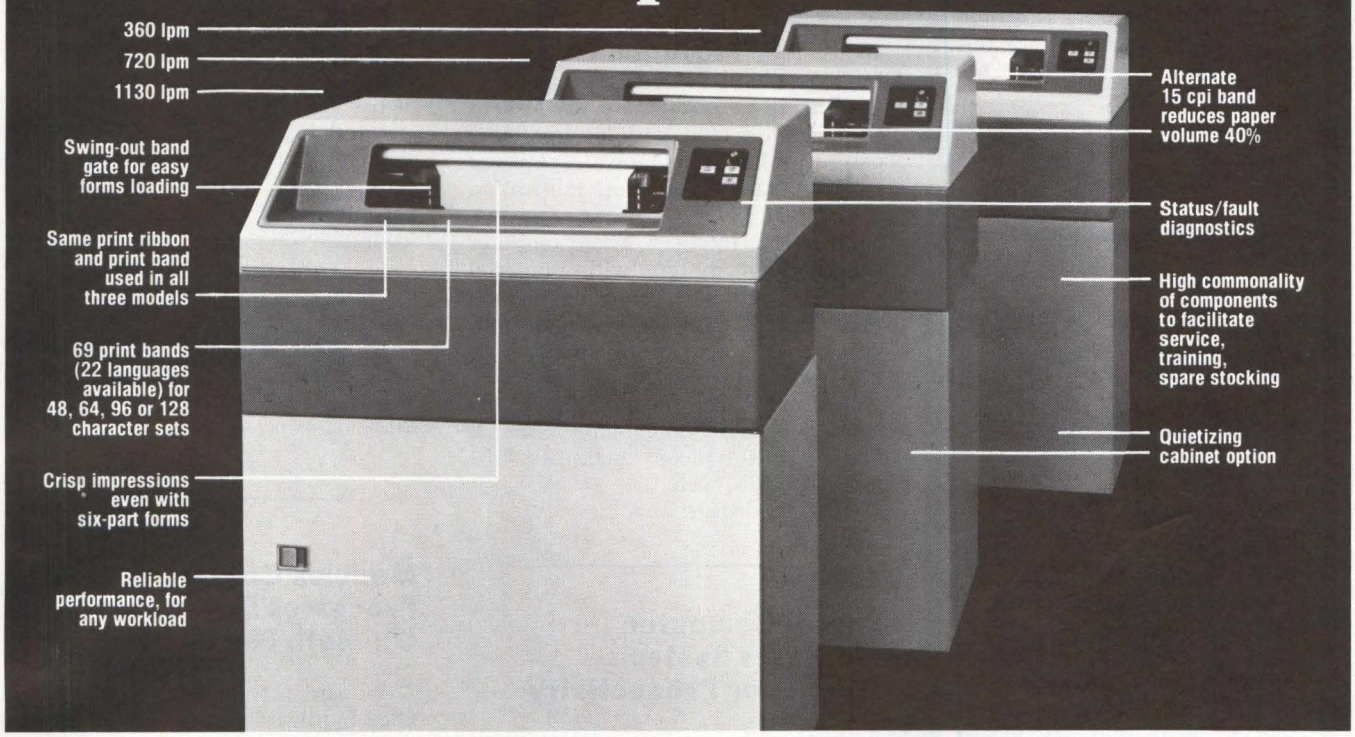

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Our 360/720 lpm models offer a compressed pitch option. That saves your customer money in paper expense. And gives him the capability to print 132 columns on standard 8½ by 11 inch paper. Bands switch in seconds. Paper loading is easier. Operator controls and adjustments are minimal. And your customer will like the clean, crisp impressions delivered by our proven hammer technology.

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CIRCLE 93 ON INQUIRY CARD

MICRO DATA STACK

COMPUTERS, ELEMENTS, AND SYSTEMS

The M8748 and M8048, which are interchangeable, can use many of the peripherals for the M8080A, M8085A, and M38510/42001BOB. This compatibility between the two devices allows ROM storage patterns for the M8048 to be developed completely in the M8748 EPROM before the M8048 chip is fabricated with custom ROM patterns, thus eliminating repetitions of the ROM masking and fabrication cycles.

Both the Intellec® Microcomputer Development System with universal P/ROM programmer and the manual PROMPT-48™ programmer with self-contained P/ROM programmer support development of application programs and storage of programs in the onchip EPROM. Single-unit price is $264; in 100-piece quantities, the price is $165 each.

Circle 426 on Inquiry Card

Pascal Computer Increases Systems Developer Productivity

Reduction of components into a single package and cost/performance benefits of an assembly language development system with the facility of a high level language interface are two aspects that Pertec Computer Corp, Computer Systems Div, 20630 Nordoff St, Chatsworth, CA 91311, considered in producing the Pascal Blaiser™. The computer consists of a Western Digital Corp single-board WD/9000 Pascal Microengine® (see *Computer Design*, May 79, p 250), housed in the company's FD 3812 dual flexible disc drive assembly, replacing the ICOM® flexible disc controller. Measuring 7.25 x 19.20 x 21.75″ (18.4 x 48.77 x 55.25 cm), the system rests on a desktop or can be mounted in a 19″ (48-cm) rack.

Also on the board is an added 64k-byte RAM. Soft-sectored, IBM double-density format FD 514 drives permit 1M bytes of mass storage. Data are transferred via DMA operating under interrupt control. Twin serial and twin parallel interface ports allow a video display terminal and printer to be connected. A power supply is configured in the package, which is priced at $5995 in single quantities. First production shipments are scheduled for fourth quarter of 1979.

The computer executes user written Pascal programs as well as the UCSD Pascal operating system, version III.0. Systems development and real-time applications are effectively handled since programs written in block oriented Pascal are compiled into P-code for direct execution by the Pascal chip set components. It also acts as a personal work enhancement tool, allowing system programmers to load code directly onto floppies and to develop applications software without having to access larger computers. Lower cost and increased programming resources contribute to productivity.

Circle 427 on Inquiry Card

Modules Control Complex Processes Dependent On Math For Decisions

A 2-board module set consists of the 2882 hardware math processor module that performs high speed fixed or floating point calculations for PCS 280 series systems controlled by the 2881 Z80 microcomputer module. The processor module, priced at $395, is compatible with other modular systems from Process Computer Systems, Inc, 750 N Maple Rd, Saline, MI 48176. The Z80 module costs $495.

When operating, the Z80 issues data and instructions to the processor module and then turns to monitoring and controlling while the calculation takes place. If the microprocessor has enabled interrupts, the processor can issue an interrupt when the calculation is complete. The Z80 can also read the status byte of the math processor, at any time, to see if it has finished the calculation.

The processor module features 16- or 32-bit fixed point or 32-bit floating point calculations; a 16-byte internal stack; and onboard voltage regulator; and double-sided, gold plated edge connections. It accepts a wide range of instructions, including add, subtract, multiply, divide, trig and inverse trig functions, logarithms, natural logs, exponentiation, Pi, and square roots.

Circle 428 on Inquiry Card

Believe it or not, there are people in this world settling for character printing that is less than perfect.

What do we mean by perfect?

We mean as perfect as the printout you are now reading. It was produced on a Sprint 5™ Daisywheel Terminal from Qume. Absolutely nothing has been retouched.

In addition to impeccable printing, Sprint 5 will also follow your orders to the letter. All standard 128 ASCII codes. Plus 43 Qume-defined, user-oriented commands for dynamic positioning, tabbing, graphics, test diagnostics, program mode, form feed and more.

Qume also offers you a large selection of printwheels and ribbons to make your printer speak over a dozen languages in a variety of typestyles and colors.

If you've been living with fuzzy printouts, help is as near as your telephone. Just contact your nearest data terminal dealer or Qume for information on Sprint 5 and our complete family of quality printers. Qume, 2350 Qume Drive, P.O. Box 50039, San Jose, CA 95150.

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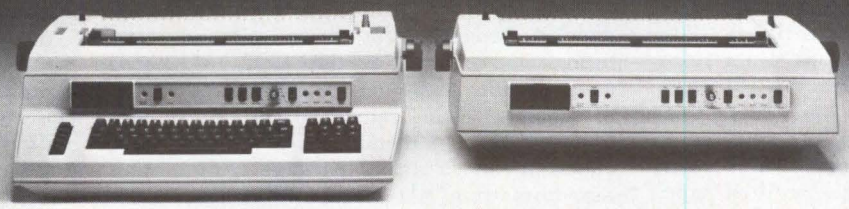

Qume®

CIRCLE 95 ON INQUIRY CARD

Expandable Systems Adapt To Support Microcomputer Product Developments

The PDS 8000 Product Development Systems family of modular systems integrate hardware with software to support development of Z8, Z80, and Z8000 based microcomputer designs. The systems are available in freestanding or rackmounted enclosures with a choice of floppy or hard disc storage. Common features among the four models are 64k bytes of memory, printer interface, 1920-char CRT console, and RS-232-C console interface.

Standard with each system is a Z8000 software development package which includes ZDOSII, Z8000 PLZ/ASM high level structured assemblers, Z80/Z8000 translator, Z8000L, and MACP macroprocessor. The Z8000 PLZ/ASM handles modular programming so that large tasks are broken into logically distinct but related parts, which are separately assembled and debugged. The assembler creates software for both segmented and nonsegmented versions of the Z8000 (see *Computer Design*, June 1979, p 174).

In a freestanding enclosure, model 15 offers 600k bytes of floppy disc storage. A Z8000 based development module permits creation and debugging of Z8000 software; simple commands from the system console communicate with the module to permit assembled code to be loaded from disc, debugged, modified, and returned to disc.

Zilog, Inc, 10340 Bubb Rd, Cupertino, CA 95014, has further expanded storage capability with the model 25 rackmounted system that offers 10M bytes of hard disc storage implemented by cartridge disc. Capability increases to as much as 40M bytes of online storage with the addition of up to three drives.

Having the same specs, respectively, as models 15 and 30, models 10 and 25, however, do not include the Z8000 development module. Addition of serial and parallel interfaces, a 120-char/s printer terminal, and P/ROM/EPROM programming capabilities can expand the system. Emulation and logic analyzer capabilities for the company's family of microcomputer components should be available by late 1979.

Circle 430 on Inquiry Card

System Applies Development Capabilities To CMOS Microprocessors

Designers who have previously used in-circuit emulation and programming to develop hardware and software for NMOS processors can now use these same capabilities with CMOS chips. The development system for 1802 microprocessors consists of a 40 x 24-char CRT display for realtime visual feedback, ASCII keyboard, 16k bytes of static RAM, in-circuit debugger board, master Z80 processor and I/O handler board, serial and parallel I/O ports, and power supplies. Data storage can consist of dual 8" (20-cm) double-density floppy units with 1M bytes of storage, dual 5" (13-cm) quad-density mini floppy discs with 630k bytes of storage, or dual tape cassettes with approximately 100k bytes of storage.

The debugger card also executes generated programs to check software integrity, and to monitor and control prototype hardware. Programs are executed from the user's memory residing on the prototype board or through memory within the development system.

Options that Hughes Solid State Products Div, 500 Superior Ave, Newport Beach, CA 92660, provides are a programmer for 2704, 2708, 2716, and 2758 EPROMS, additional memory boards, and emulators for 8080, 8085, and Z80 microprocessors. These modules, with an associated software package, allow the system to be used to develop programs for these microprocessors, as well as the 1802. A resident cross assembler for mnemonic to machine code translation, an interactive editor, a monitor for program checkout, and a utility package with disc formatting, file creation, and file movement programs comprise the software. An extended BASIC compiler will also be available.

Circle 429 on Inquiry Card

Low Cost, Programmable Video Terminal Competes In Small Systems Market

The SuperBrain Video Computer is an intelligent terminal with small business systems capability, priced at $2995 for end users and from $1945 to $2695 in OEM quantities. Standard features include two double-density 5.25" (13.3-cm) floppy disc drives with 320k bytes of storage, 48k bytes of programmable RAM which expands to 64k, and two Z80 microprocessors which transfer data to the screen at 38k baud. An S-100 bus adapter connects auxiliary peripheral devices, such as a 10M-byte disc, to the system; a universal RS-232-C communications port allows interfacing with an auxiliary printer or host computer.

A CP/M based disc operating system offers a high powered text editor, assembler, and debugger. Along with this operating system, Intertec Data System Corp, 2300 Broad River Rd, Columbia, SC 29210, has designed a variety of software that includes BASIC, FORTRAN, COBOL, and APL.

In addition, the lightweight, table top enclosure holds a full ASCII keyboard with numeric pad and function keys, a nonglare 12" (30.5-cm) screen, and a single-board design to insure easy servicing. The Video Power Supply™ combines video and power circuitry on a single board.

Circle 431 on Inquiry Card

Another new terminal from Hazeltine!

Hazeltine 1552

Announcing a significant enhancement to the renowned Hazeltine 1500 Series. With an inventory of Standard Features so impressive, this new video terminal commands your attention for conversational applications.

Standard Features

All 128 ASCII Codes
95 Displayable Characters including Lower Case plus 31 graphics symbols
✓ High Resolution Characters using a 7×10 dot matrix
ANSI Standard Typewriter layout
Cursor Control Keys
Function Keys
Alternate Key Pad Mode
Separate Integral Numeric Pad
Hold Screen Mode
Graphics Mode
✓ Dual Intensity
Cursor Addressing and Sensing
EIA and 20 MA Interface
Baud Rates up to 9600 Baud
✓ Auxiliary EIA Output
Remote Editing Commands
✓ Standard or Reverse Video
✓ Programmable Key Switch Audio Feedback
VT-52 Compatibility
✓ Clear Screen
✓ Clear Foreground
Clear to End of Line
Clear to End of Screen (background spaces)
Audible Alarm
Backspace
✓ Keyboard Lock
✓ Keyboard Unlock
✓ Insert Line
✓ Delete Line
✓ Field Tab
Column Tab
Enter/Exit Hold Screen Mode
Enter/Exit Alternate Key Pad Mode
Enter/Exit Graphics Mode
Send Terminal ID
✓ Set/Reset Audio Key Switch Feedback
Cursor Address (XY)
Incremental Cursor Control
✓ Read Cursor Address
Home Cursor

We interrupt this advertisement to bring you this special message...

VT-52 Users, here's the terminal you've been looking for. The Hazeltine 1552.

Besides fitting directly into your DEC system, it costs you much less. And it's available for immediate delivery!

But that's just for starters. Of even greater significance are these two important bonuses:

"QUALITY" BONUS...the kind of Quality you've come to expect with every terminal bearing the famous Hazeltine name, backed by Hazeltine's exceptional Warranty Program. Ask for details!

"FEATURES" BONUS... with the impressive roster of Standard Features listed on this page, the Hazeltine 1552 more than matches the VT-52. Plus! All Features checked (✓), while standard on the Hazeltine 1552, are not available on the VT-52!

We now return you to the ad in progress.

It's a Hazeltine naturally!

Hazeltine

Hazeltine Corporation, Computer Terminal Equipment, Greenlawn, New York 11740, (516) 549-8800 Telex 96-1435

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Detroit (313) 296-9510 • England 01-948-3111 Telex (851) 928572

Microcomputer Expands Online Floppy Disc Storage to 2.5M Bytes

More file storage has been provided in the VDP-180 video data processor series microcomputer with the inclusion of two Control Data Corp 9406 double-sided floppy disc drives that each offer 1.25M bytes of storage per drive in the IBM compatible double-density format. The 2-unit system contains an operator console with CRT, keyboard, reset and interrupt switches, and disc drives, together with an open chassis electronics unit with plug-in modules, power supplies, cables, and five extra motherboard slots. In normal use, the latter unit does not require operator attention since all computer functions are controlled from the desktop unit; therefore, the electronics can be placed up to 8′ (2.4 m) away.

The microcomputer includes all features of other systems from Imsai Manufacturing Corp, 14860 Wicks Blvd, San Leandro, CA 94577 (see *Computer Design*, Aug 1978, p 154). Among these features are a 10-slot, S-100 bus motherboard; plug-in modules for RAM, video and disc interfaces, and main processors; and system expansion capability for printers or hard disc.

Circle 438 on Inquiry Card

APL Language Is Adapted to Operate On Desktop Microcomputer

Full power of the APL language for distributed applications is available with the APL/DTC™ desktop microcomputer. The language is an enhanced version of the APL that Vanguard Systems Corp, 6812 San Pedro, San Antonio, TX 78216, developed for Z80 based microcomputers. Supplying 24k bytes of usable workspace, the language contains standard arithmetic functions plus Boolean, relational, selectional, structural, and general functions such as execute and format. System variables and functions—canonical representation, function fix, share offer, and share retract—are also included. The language, with disc based workspace and copy-object libraries, supports arrays of up to eight dimensions.

The standard hardware/software configuration consists of a 4-MHz, Z80 based CPU, two quad-density minidisc drives, video terminal, APL character generator, object code disc, and documentation. One auxiliary processor interfaces I/O ports and another implements an indexed file system. Three operational processors handle data communications, high resolution graphics manipulation with a 256 x 240 raster scan, and A-D conversion in control applications. Ten packaged applications cover such topics as simulation, ISAM, inventory control, general ledger, text editor, and statistical analysis. The system's use of a standard CP/M® operating system permits the application of optional packages for BASIC, COBOL, FORTRAN, and Pascal; a Z80 assembler; and word processing software.

The system can be tailored by expanding active workspace to 36k bytes, and adding 630k bytes of file space with two extra minifloppy disc drives. A 120-char/s APL/ASCII matrix printer and a daisy wheel printer provide hard copy.

Circle 439 on Inquiry Card

Use of CPU Card Frees System From Spurious Noise In Bus Lines

The S-100 single-board microcomputer based on Intel's 8085A-2 microprocessor can be used with the company's P/ROMs, RAMs, card cages, and motherboard to form a 5-MHz system for industrial and process control applications, as well as business processing. A built-in clocking mechanism allows operation at 2 MHz to accommodate systems with slower memory.

Hardware floating point, using Advanced Micro Device's Am9511 math chip, performs addition in 175 ms and multiplication in 168 ms (typ). Programs, files, and other data are permanently stored in 3k bits of Intel 2708 P/ROM; 1k of RAM serves as a scratchpad. Other features are vectored interrupts, switch selectable I/O ports for maximum flexibility in peripheral device selection, and a phantom line that automatically returns the processor to the monitor address. Onboard DIP switches control I/O ports at any baud rate between 75 and 9600 for use with a keyboard or RS-232-C terminal.

Artec Electronics, Inc, 605 Old County Rd, San Carlos, CA 94070, also provides a monitor that tests memory, performs simple debugging operations, and gives program status at any time. This allows operation without an additional video board.

Circle 440 on Inquiry Card

Plug-in Disc Controller For LSI-11 Based Systems Handles Up to 20M Bytes

Configuration of the microprocessor based PM-DCV11 on a single quad board gives users a cartridge disc controller for up to 20M bytes that plugs directly into the standard Digital Equipment Corp LSI-11 backplane. Plessey Peripheral Systems, 17466 Daimler Ave, Irvine, CA 92714, has devised the unit to be software compatible with RT11 and RSX-11 based operating systems, as well as with system and diagnostic software that supports RK05 type drives. The controller can handle a drive of 100 or 200 tracks/in (39 or 79/cm).

Several design considerations serve to enhance the controller. The use of low power Schottky reduces the system power requirements. P/ROM drive select facilitates flexible system configuration with automatic retry on seek errors and overlap seek capabilities. Finally, a FIFO buffering technique allows DMA with a transfer rate of 6.4 μs/word.

Circle 441 on Inquiry Card

Almost perfect.

Our new ADM-42 doesn't have quite everything. But it comes so close, you might never notice.

Because it's a complete, semi-intelligent terminal for just about any application you can name. And it does just what you want it to do, just when you want it done.

The ADM-42 is completely self-contained, and provides you with flexibility of format, security, editing, interface, and transmission. It also features a full two-page display as standard equipment. Not as an option. And it comes with a truly staggering array of options.

THE MORE YOU USE IT, THE SMARTER IT SEEMS.

We gave the ADM-42 a bright, easy-to-read 2000 character display. A full 128 ASCII character set. 16 function keys for 32 separate commands. And five separate cursor control keys.

The 42's behavior modification gives you a factory installed personality for an alternative ESC sequence lead-in—in addition to the standard ESC. And End Block character. A New Line character sequence. A field separator. And even a function sequence preamble.

Its status displays on the screen give you a conveniently wide range of information at a glance. While its special symbols indicate the entry of control characters in memory. Also, all control characters can be stored using the escape sequence or program mode. And the Field Protect Mode allows rapid data entry into forms or instruction pages.

THE ADM-42 WILL HAND YOU ANOTHER LINE.

The terminal's displayed data is formatted in 24 lines per page, 80 characters per line. And, to top it off, it comes with a 25th line established and reserved exclusively for status indicators and messages of up to 79 characters.

As if all this weren't enough, the ADM-42 has an impressive list of options. Like synchronous transmission with various line protocols. An extended memory capable of adding data space up to a maximum of 8 pages. And programmable function keys, to name but a few.

THE ADM-42 IS ONE TOUGH ACT TO FOLLOW.

The ADM-42 has just about everything. Including a microprocessor that increases reliability and ease of operation. Any way you look at it, in fact, it's one pretty smart buy.

So if you're thinking of upgrading to a more intelligent terminal, at a more than reasonable price, call us today. Or better yet, contact your local distributor.

We'll show you how easy it is to move up to the ADM-42.

The terminal that's so smart, you'll swear it's got a mind of its own.

ADM 42
Getting smarter all the time.

LEAR SIEGLER, INC.
DATA PRODUCTS DIVISION

Lear Siegler, Inc./Data Products Division, 714 Brookhurst Street, Anaheim, CA 92803; (800) 854-3805. In California (714) 774-1010. TWX: 910-591-1157 Telex: 65-5444.

CIRCLE 97 ON INQUIRY CARD

SOFTWARE

Microcomputer Assembler Obtains Power With Addition of Text Editor

The 6-character editor/assembler for the Apple II microcomputer improves on the basic conventions and op codes as developed by MOS Technology for the 6502 microprocessor by incorporating a text editor and 2-pass implementation. The text editor operates in two entry modes: upon data entry, a syntax check is performed on each input line, and in the command mode, 19 text editor commands are accessible.

After program origination has been completed in the text file, the assembler searches for the file and checks for errors on the first pass. Those that are detected are displayed in English along with the corresponding line number. Errors are corrected by returning to the text editor mode. If no errors exist, the object code is inserted in memory in a form that the Apple II can execute. Capabilities of a macro-assembler are obtained when the assembler is used with the disassembler/text file manager, also available from Microproducts, 2107 Artesia Blvd, Redondo Beach, CA 90278; the assembler can then insert portions of a text file into the main text file.

The assembler, available on Apple II compatible cassette tape or floppy disc, operates with the Apple II using PR-40 or Centronics 779 printer interfaces, as well as others. It can call any printer driver from any location in memory. The assembler also directly supports the company's Apple II EPROM programmer.

Circle 434 on Inquiry Card

Compiler Produces High Speed Assembly Language Code To Fit in ROM

Producing code for the Intel 8080/8085 and the Zilog Z80, the Micro-Pascal/80 compiler directly generates 8080/8085 macro assembly language code—a true object code—that eliminates the need for an interpreter as found in other P-code systems. Many operations, such as subscript calculation, are optimized to give efficient programs.

Resulting runtime modules may be as small as 1.5k bytes. The compiler programs may link to assembly language routines that are assembled separately. Compiled programs can be placed entirely in ROM. The compiler is a subset of Standard and UCSD Pascal; the user can check out programs with UCSD Pascal before committing them to hard code.

Since the compiler produces external references to routines, the user may write dedicated routines to drive devices such as special keyboards or self-scan displays. Routines are provided for operation in a CP/M environment.

Allowing complex expressions of algorithms, the compiler outputs the user's Pascal program statements as comments in the assembly language source file. The user then knows exactly what code was generated for input statements, and can correct or modify the assembly language source before assembling.

The compiler operates under the UCSD Pascal system (I.5, II.0, or III.0). Sorrento Valley Associates, 11722 Sorrento Valley Rd, San Diego, CA 92121, distributes it on an 8" (20-cm) single-density floppy diskette which also contains a compiler verification program. Well commented runtime routines are supplied in source and object form.

Circle 435 on Inquiry Card

BASIC Compiler Speeds Assembly Language Program Generation

The CDS BASIC compiler enables portions of North Star BASIC programs—generally only minor computational segments—to be compiled into assembly language to increase speed and to protect proprietary sections of code. This compiler development system requires the PDS Assembly Language and HDS Hybrid Development Systems for North Star (see *Computer Design*, July 1978, p 154, and July 1979, p 177, respectively). Versions have been developed by Allen Ashley, 395 Sierra Madre Villa, Pasadena, CA 91107, for Release 4 single-density or Release 5 double-density North Star Systems.

System components are the compiler, IBASIC (an integer BASIC interpreter), and a set of interface routines which couple the assembly language program to North Star BASIC. Arithmetic operations between floating point numbers in North Star BCD format or signed binary integer format, as well as logic and relational operations, are supported. Variable storage is shared with North Star BASIC.

Circle 436 on Inquiry Card

Business Applications Benefit From BASIC Disc Operating System

MICRODOS™, a disc operating system for Radio Shack's TRS-80™, works entirely with Level II BASIC commands, residing in less than 7k of memory. Percom Data Co, Inc, 211 N Kirby, Garland, TX 75042, has developed it especially for business and professional applications to replace TRSDOS™ as a faster and more powerful alternative.

The operating system is supplied on a diskette, along with a file management program, a disc utility program, and a sample application program, all written in BASIC. The system operates the company's TFD series of mini discs, which are small, medium, and large capacity add-on storage devices for the TRS-80 microcomputer.

Power-up or reset activates a system disc program menu. The user may include hexadecimal constants in expressions, and may add up to 10 special functions to those that exist.

Circle 437 on Inquiry Card

Extended Pascal For μProcessors Capitalizes On Structured Programming

High level language capabilities of structured top-down programming for modular, readable software programs are characteristics of the Microprocessor Pascal system for the 16-bit 9900 family. Texas Instruments, Inc, Semiconductor Group, PO Box 1443, Houston, TX 77001, has given designers the means to develop transportable and cost-efficient software on either the floppy disc based FS990 or multiuser hard disc based DS990 host development systems. Its reliability and faster execution are due to data typing and structured code. The hierarchical structure allows the task to be divided into separate modules, thereby shortening the development cycle.

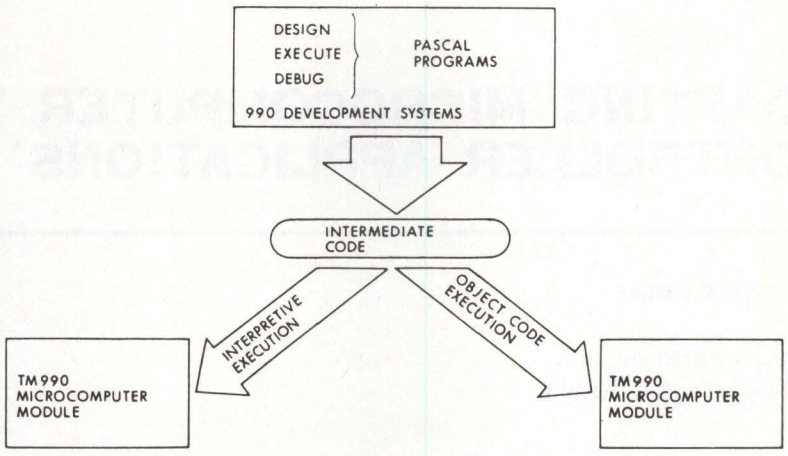
Using a superset of the proposed ISO Pascal standard, the language is a revision of TI Pascal (introduced in 1978), with the addition of a source editor, compiler, and debugger. Thus, a user may develop software for industrial and realtime control, as well as general purpose, applications.

The source editor for Pascal is a syntax checker while the compiler, checking for logic errors, generates intermediate code. It translates the source program into pseudo code, which can be executed interpretively or converted to native object code for the 9900. These two versions of runtime support offer speed/memory tradeoffs for specific applications; interpretive execution is twice as memory efficient as compiled code, but native code execution is five to seven times faster. This native code capability will be distributed in the fourth quarter of 1979.

Debugging capability is performed at two levels. The host level debugger displays and traces program data; target level debugger uses the AMPL microprocessor development system to check realtime execution. Features of program debugging are a help command, printout of the debug session, tracing, breakpoints, interrupt simulation, and concurrency debug. In addition, a configurator allows the user to eliminate unnecessary library and statement routines from the runtime support. Only the necessary portions are retained and used.

Another feature of the language is concurrency, which is actually timesharing the microprocessor through various tasks, which are able to intercommunicate. This reentrant feature duplicates a task, replicating only data, not the algorithm; it thereby separates data from the algorithm.

Circle 432 on Inquiry Card



Microprocessor Pascal from Texas Instruments provides programmers with structured language for 16-bit 9900 family. Major feature is option of interpretive or native (object) code execution of intermediate code. Former is more memory efficient while latter executes faster allowing user to adapt language development to application requirements

Structured Programming Advances Microprocessor Development Facility

Superior program development efficiency is achieved by bringing the benefits of structured high level language programming to the development of microprocessor based equipment using any Tektronix 8002 Microprocessor Development Laboratory. Programs for use on a variety of microprocessors are developed with the UCSD Pascal/8002 Universal Program Development Package introduced by the Pascal Development Co, 10381 S DeAnza Blvd, Suite 205, Cupertino, CA 95014. Its facilities include a CRT screen oriented text editor, compiler, assembler, linking loader, and other utilities.

The user writes program segments with the aid of the text editor, and stores them on floppy discs. The compiler then converts the programs into P-code format, an intermediate code that offers program portability. While easily adapted for use on actual microprocessors, this code requires only 30 to 50% as much storage space as the machine language of a typical 8-bit microprocessor. Once compiled, the Pascal programs are executed and debugged on the development system. Finally, the proven segments are linked together and transferred to the equipment under development. □

Circle 433 on Inquiry Card

ADAPTING MICROCOMPUTER TECHNOLOGY TO CONTROLLER APPLICATIONS

George Adams

Intel Corporation
Santa Clara, California

As the semiconductor industry uses advanced large scale integration to package an increasing number of functions on silicon chips, one benefit to arise is the adaptation of the technology to controller applications. A significant recent advance is the integration of an analog to digital converter on a microcomputer chip. With an onchip converter the microcomputer becomes a true microcontroller.

One such controller is Intel's 8022, a general purpose, 8-bit single-chip microcomputer fabricated using MOS LSI 5-V technology. The chip provides two analog inputs—each a general purpose input line on which conversion is performed by a successive approximation technique (similar to digital voltmeter conversion). In addition there are nine specialized linear input lines—one which detects zero crossover of an ac signal and eight voltage comparators on selected I/O ports which detect varying voltage levels, providing interfacing capabilities beyond simple TTL 1 and 0 levels.

General applications of an analog to digital converter (ADC) include interfacing analog signals from temperature sensors in ovens, pressure sensors in process control instruments, and any other transducers capable of producing analog voltage output. Applications for the zero crossover detection feature include counting cycles of an incoming 50- or 60-Hz ac line frequency to provide a stable timing reference in realtime control environments, and determining the peak of an ac line voltage to trigger phase-dependent devices such as triacs or silicon controlled rectifier (SCR)—interfaces often needed in control applications. Voltage comparators on the microcontroller's I/O ports can interface directly to devices operating at a variety of voltage levels such as low voltage capacitive touch panels.

Analog to Digital Converter

The ADC uses successive approximation logic to perform the conversion. A resistance ladder generates 256 voltage levels at equal intervals between a full scale reference voltage (V_{aref}) and ground (V_{SS}). The ADC compares the analog signal AN_X (appearing on either of two inputs, AN_0 or AN_1) to the potential at the midpoint of the ladder, determining whether AN_X is a potential in the upper or lower half of the ladder. On the basis of this test, the ADC sets the most significant bit (MSB) of the digital result.

AN_X is then compared to the potential at the midpoint of the selected half of the ladder, determining in which quarter of the ladder AN_X belongs, and setting the next highest bit of the digital result. By repeating this zeroing-in process eight times, the ADC locates the ladder tap with the potential most-nearly-matching AN_X, and accordingly sets or clears each of the eight bits to form the digital result.

To read an analog signal, only two CPU instructions need be executed. First, SEL AN_0 or SEL AN_1 selects the desired analog input (Fig 1). Secondly, RAD reads a digital result into the microcomputer's A-D conversion register. The first digital result becomes available 40 μs (four in-

The Quad Squad

If you own a PDP-11 or an LSI-11, you made a great buy. Now we've got something that will make your buy look even better. It's the quad squad, the latest in the Able line of enhancers for the PDP-11 family. We're talking about the unusual cards that give you four asynchronous communication channels each while presenting only one load to the Unibus. There are four of them. The EIA-serial QuadrAsync/B™, a DL-11B replacement. The QuadrAsync/C™, a 20 mA current-loop alternative to the DL-11C. The EIA-serial QuadrAsync/E™, a DL-11E replacement. And the QuadrAsync/LSI™, a DLV-11 replacement which gives the LSI-11 user four asynchronous EIA and/or 20 mA serial channels.

All four condense onto a single quad board four times that which is on the DEC unit they are replacing. Yet there is relatively little requirement for bus repeaters and expansion boxes to increase the number of available channels. Operation is full duplex or half duplex with both the transmitter and receiver for each channel operating at the same baud rate. Each model is system software compatible with the unit it replaces.

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CIRCLE 99 ON INQUIRY CARD

```
SEL   AN0      ; SELECT ANALOG INPUT 0.
MOV   R0,#24   ; SET MEMORY POINTER;
RAD            ; LOAD ADC VALUE INTO ACC.
MOV   @R0,A    ; MEMORY BYTE 24 = ACC.
INC   R0       ; INCREMENT MEMORY POINTER.
RAD            ; LOAD ADC VALUE INTO ACC.
MOV   @R0,A    ; MEMORY BYTE 25 = ACC.
```

Fig 1 A-D converter instructions. ADC input requires only two instructions: SEL to select input line 0 or 1, and RAD to read value into accumulator. Program segment selects line 0 and reads two values; it stores first in memory location 24, and second in location 25. Other instructions needed to support this operation come between ADC instructions, and provide necessary 4-cycle delay between successive selects and reads

struction cycles) after the select instruction is executed. Updated results become available every 40 μs thereafter without execution of another select instruction.

Connecting an analog device to the ADC is a simple procedure, as illustrated in Fig 2. To connect a thermistor, for example, make a voltage divider with the thermistor on the grounded arm and connect AN_0 to the thermistor's high end (ie, connect the ADC between the top of the thermistor and ground). Minimum readable potential is ground. Maximum readable potential is controlled by the reference pin V_{aref} and may vary from the upper supply potential V_{CC} (approximately 5 V) down to one-half of the V_{CC} supply potential.

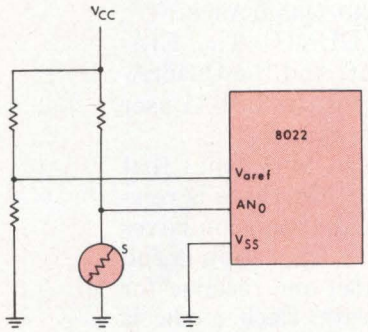

Fig 2 Connecting analog device to ADC. Resistive sensor can be connected to ADC by putting it on grounded arm of voltage divider, and connecting one ADC port across it. Diagram shows second voltage divider which provides reference voltage, V_{aref}. This should be adjusted to make V_{aref} equal to maximum value of AN_0 that ADC must be able to read

Because the ADC is simple to use, it is practical to filter the input digitally—in the microcontroller's software. For example, the software can easily be designed to average several analog readings. Furthermore, the software can apply different weights to different readings or perform reasonableness checks on them before accepting them.

A separate power supply pin is provided on the ADC to increase its isolation from digital noise. With the zero-crossover feature, the ADC readings can be synchronized with the line voltage to cancel the effects of ac hum. These features usually make it possible to dispense with almost all analog filtering.

I/O Port with Voltage Comparators

The microcontroller provides three 8-line I/O ports. In addition to TTL compatible input circuitry incorporated on all three ports, each line on port 0 is equipped with a medium gain voltage comparator which reads the potential difference between that line and the voltage applied to a reference pin (V_{TH}). It can detect an input potential difference of 100 mV.

Voltage comparators and reference pin make port 0 particularly easy to connect to 2-state devices that do not generate a simple on/off signal. An example is the capacitive touch switch which, when touched, changes its capacitance and so reduces the potential across it. Traditional circuits require 50 to 100 V across the switch to produce a touch/no touch difference that a typical microprocessor can detect. Voltage comparators make it possible to reduce the potential to 15 V. The lower voltage makes the equipment controlled by the microcontroller safer to use, and can reduce the time spent getting agency approval.

A common problem with capacitive touch switches is imbalance, random differences in touch and no touch potentials from switch to switch. On a given piece of equipment, potential range variation of the switches may not allow a single fixed-switching reference voltage at which the state change in every switch can be detected.

To handle the imbalance problem, an RC network is built to produce a range of potentials spanning the entire range of possible touch/no touch potentials (Fig 3). $P0_0$, V_{TH}, and AN_0 are all tied to the network. Other lines on port 0 can be used as sense inputs from the touch panel.

When the controlled equipment is turned on, the chip calibrates each sense line in the following way. It writes a 1 to $P0_0$, effectively grounding the network and zeroing the potential across the capacitor, V_{RC}; then it writes a 0 to $P0_0$, allowing V_{RC} to rise, Fig 4(a). V_{TH} rises with V_{RC}. When V_{TH} passes the no touch potential on the sense line, the comparator output goes from 1 to 0. The controller sees this and reads V_{RC} from AN_0, determining the no touch voltage level for that line. It stores this in RAM.

To read the sense line in operation, the calibration process is repeated; but instead of watching the sense line and reading AN_0 when the line goes to 0, the chip watches AN_0 until it approaches the no touch level and then reads the sense line. A sense line 0 indicates touch, a 1 indicates no touch, Fig 4(b).

This calibration process is done entirely in software. No electronic components are needed except the RC network. And since calibration is repeated every time the controlled equipment is turned on, it compensates automatically for variations in touch panel response caused by aging or environmental change.

Also, since calibration consists of converting a voltage level (no touch potential on each sense line) to a digital value, the same technique can be used to make port 0 act

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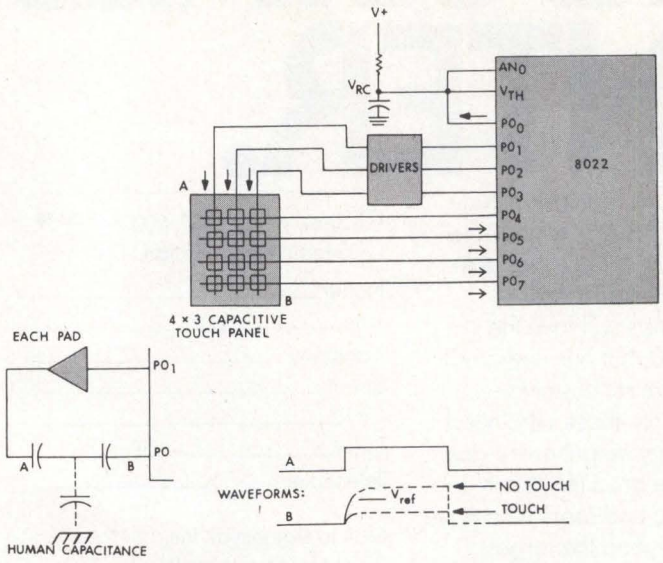

Fig 3 Calibration process. Automatic calibration of capacitive touch panel can be done with elementary RC network attached to AN_0, V_{TH}, and one line of port 0. Capacitive touch panel is strobed and sensed as X-Y keyboard scan operation. Human capacitance shunts charge away so that voltage B is lower during A strobe

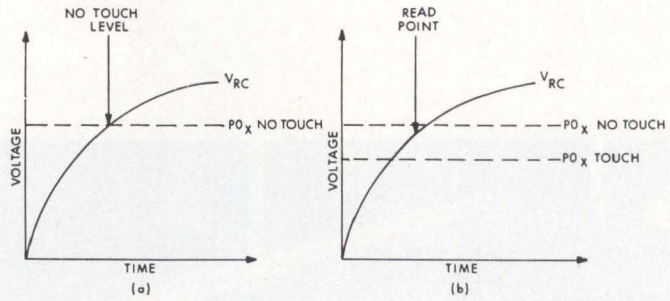

Fig 4 Sense line calibration. (a) Response of RC network is used to locate no touch level of each sense line; (b) reading PO_X just before V_{RC} and V_{TH} read line's no touch level yields a 0 for touch or 1 for no touch

as a 7-channel ADC. Accuracy on each channel is about five bits (100 mV out of a 2.5-V range).

There are other features provided by the I/O ports. If V_{TH} is allowed to float, port 0 acts as a conventional I/O port with input switching point of $V_{CC}/2$ and sensitivity of 100 mW. Two of the pins on port 1 are capable of driving 7-mA loads when the port is used for output. These pins can be tied together to drive a single load of 14 mA, enabling the 8022 to operate devices such as LEDs without discrete driving circuitry.

Zero Crossover Detection

Two test pins are provided to detect high/low signal levels. One pin, T_0, may be used as an input line or as an external interrupt line. When used as an interrupt line, it can notify the processor of any event requiring immediate attention.

The other pin, T_1, is equipped to detect the zero voltage (crossover) point in low frequency ac input, as well as conventional low/high digital signals. It also provides the capability to synchronize the software with the line voltage cycle. Line voltage synchronization can be used to filter ac noise from the analog input by taking each analog sample at the same point in the line voltage cycle or to time phase dependent events, such as firing a magnetron at an ac voltage peak to minimize current surges on the line. That can be accomplished by detecting crossover, then timing out one-quarter cycle longer in software.

Summary

This design includes many other features which allow event synchronization, counting, etc. Its multiple capabilities clearly illustrate the powerful single-chip functions that are being developed by the semiconductor industry. The monolithic integration of an analog to digital converter and a microcomputer is undoubtedly among the more important of those continuing developments.

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LSI Timing Controller Provides Counting and Timing for Microprocessor Systems

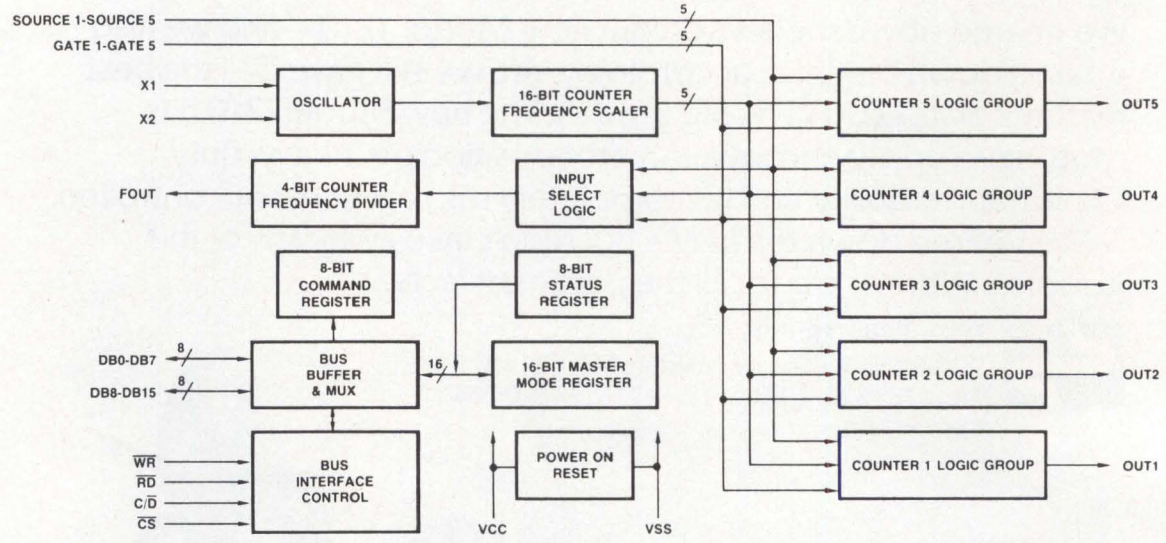

Fig 1 Advanced Micro Devices' system timing controller Am9513 is support device for processor oriented systems, designed to enhance counting and timing operations. Single device contains internal oscillator and associated frequency scaling circuitry plus five general purpose 16-bit counters, each independently configurable for variety of tasks. Data bus interface to host processor can be either 8 or 16 bits wide

Capable of replacing all counting and timing elements in microprocessor based systems, a general purpose system timing controller (STC) can be personalized for many particular applications and can be dynamically reconfigured under program control. This 5-V only monolithic MOS device includes five independent 16-bit counters and an internal oscillator frequency source (Fig 1), provides counting rates up to 10 MHz, and offers up/down and binary/BCD counting using any 1 of 16 counting sources.

The Am9513, produced by Advanced Micro Devices, Inc, 901 Thompson Pl, Sunnyvale, CA 94086, is used in programmable frequency synthesis, complex waveform generation including high resolution programmable duty cycles, digital 1-shots with retriggerability, time-of-day clocking including alarms, complex pulse generation, high resolution baud rate generation, frequency shift keying, event count accumulation, A-D conversion, and waveform analysis. Every counter in the STC can operate completely independent of the others in any one of over 20 modes and the data bus interface to the host processor may be either 8 or 16 bits wide.

Each of the 16 counting sources (Fig 2) includes five gate (GATE) inputs, five source (SRC) inputs, five oscillator frequencies, and one cascaded counter input. GATE inputs provide direct hardware and software control of count accumulation, with each gate capable of controlling up to three counters. Also, any counter can count GATE input signals. SRC inputs are external signals that can be routed to any and all counters.

The internal oscillator uses an external frequency-determining crystal or other reactive network to set a typical base frequency of 10 MHz. Then, the scaling portion of the circuitry divides the oscillator frequency by 10, 100, 1000, or 10,000 or by 16, 256, 4096, or 65,536, depending on programming. These frequencies can be selected by any counter and brought out for use in other parts of the system.

Each counter can be internally concatenated with an adjacent one to provide a larger count capability. Maximum count capacity is 2^{80}, achieved by chaining all five 16-bit counters together. All counter inputs have selectable input polarities. Any input (but only one at a time) can also be divided by an integer from 1 to 16, inclusive, using a 4-bit programmable counter that connects to the 3-state FOUT output. Each counter has its own associated 3-state output with individually programmed polarities, which, depending on counter

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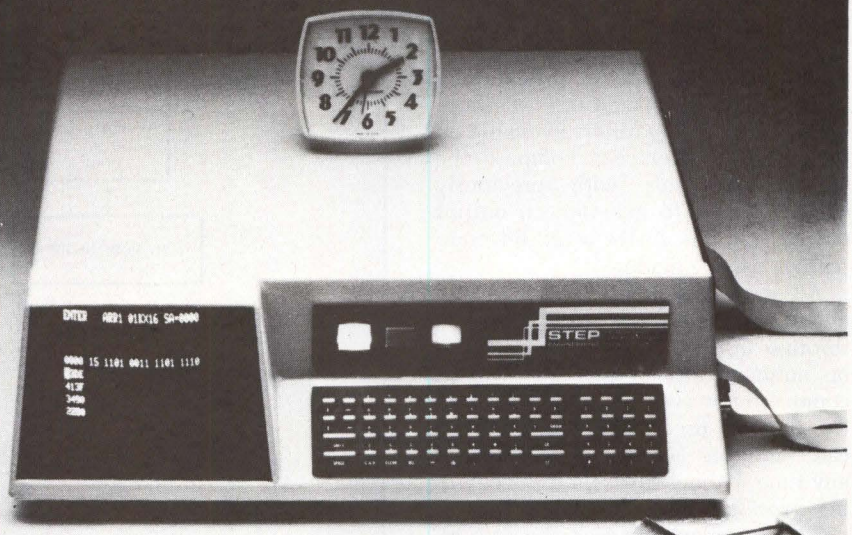
2901 design? STEP on it!



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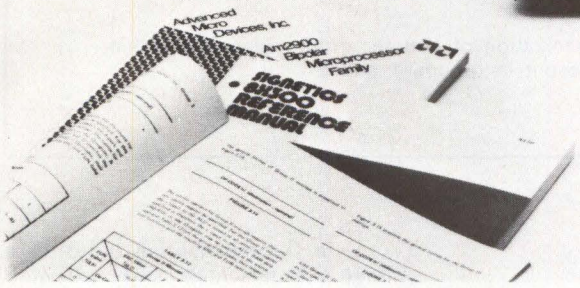

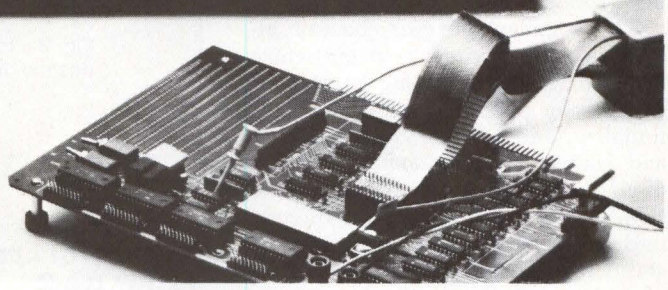

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configuration, can be a pulse, a toggle level, or a complex waveform. These OUT signals are in addition to the 16 data bus lines.

Counters 1 and 2 can also operate in a time-of-day mode, providing a 24-h realtime clock. Auxiliary alarm registers and comparators available on these two counters can compare the counters' contents with previously entered values to generate an output on the OUT pin. A 16- or 32-bit comparison can be made.

Access to the internal control and operating elements is either random through use of an address command or automatically sequential without command intervention. Regardless of the method used, the host processor can read an accumulated count at any time without disturbing the counting process.

The command set for the STC allows the host processor to customize and manage the operating modes and features for particular applications, to initialize and update internal data and control information, and to manipulate operating bits during operation. Commands are entered directly into an 8-bit command register. The status register reflects the output state of each counter.

A master mode register controls programmable chip functions that supplement the counter-specific options available within each counter logic group. Five separate 16-bit counter mode registers control the independent options available for the five general purpose counters.

Additional versatility is provided by two additional registers associated with each general purpose counter. For example, a 16-bit load register can automatically load any preset 16-bit value into a counter when the count reaches zero, this automatic initialization establishing modulo control. The 16-bit hold register reads and holds the present counter value when a "counter read" occurs. It can also double as a second load register.

The system timing controller meets the full requirements of MIL-STD-883C reliability assurance testings. Parts are available in 40-pin cerDIP, molded DIP, and side-brazed ceramic packages.

Circle 350 on Inquiry Card

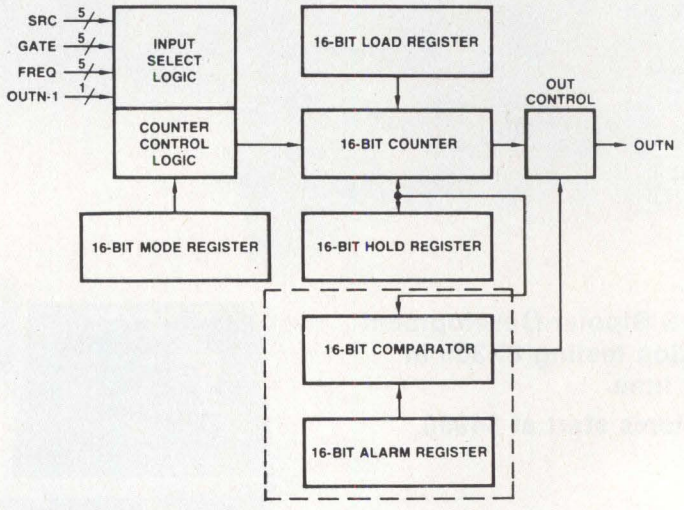


Fig 2 Internal organization of counter group. Elements within dashed line are present in groups 1 and 2 only

Low Total Error 12-Bit DAC Meets Mil Specs

Using stable, laser trimmed thin film technology, a 12-bit digital to analog converter provides a total error (untrimmed) of ±0.3% FSR and a linearity error of ±½ LSB over a −55 to 125 °C operating range. Manufactured by Burr-Brown Research Corp, PO Box 11400, Tucson, AZ 85734, the DAC87-CBI-V/MIL is 100% screened to MIL-STD-883. Other features include a ±20-ppm FSR/°C gain drift, ±10-ppm FSR/°C offset drift, 7-μs settling time (full step to ±1 LSB), and 10-V/μs slew rate (min). Monotonicity is maintained over the full temperature range. The DAC is capable of being adjusted to zero offset error and to zero gain error using external adjustment circuits.

Complementary binary output coding is indicated by the CBI term in the device designation, with complementary straight binary (CSB) or complementary offset binary (COB) selectable by external connections. The V in the designation indicates a voltage output, which can be externally pin connected to provide ±2.5, ±5, ±10, 0 to 5, and 0 to 10 V.

Recommended operating conditions call for a supply voltage range of ±14.5 to ±15.5 Vdc (for V_{CC}) and 4.75 to 5.25 Vdc (for V_{DD}). The absolute maximum ratings for these parameters are ±18 and 0 to 18 Vdc, respectively. Maximum allowable power dissipation is 1350 mW at T_A = 125 °C. Dimensions of the hermetically sealed metal 24-pin DIP are 1.4 x 0.8 x 0.25" (35.6 x 20.3 x 6.4 mm).

Circle 351 on Inquiry Card

16k and 32k EPROMs Reduce Power Usage, Raise Speed

Versions of existing 32k- and 16k-bit EPROMS, the TMS25LS32 and TMS-2516-35, announced by Texas Instruments Inc, PO Box 1443, Houston, TX 77001, are a low power version of the

TMS2532 32k EPROM and a high speed version of the TMS2516 16k EPROM, respectively.

A 40% reduction from the power used by the standard device characterizes the 32k memory, which dissipates 500 mW (max), with I_{CC} (max) equal to 95 mA. It also features an input noise immunity of 400 mV, high and low ends.

The 16k device provides reduced minimum read cycle time and maximum access time from power down. Each of these parameters is 350 ns compared to 450 ns for the standard device.

Features common to all members of this 5-V EPROM family include an 8-bit word configuration, industry standard pinout, simple programming, UV erasability, and fully static operation with automatic chip select-power down. The devices are available in sidebrazed (JDL suffix) packages rated for operation from 0 to 70 °C.

Circle 352 on Inquiry Card

2k x 8 Bipolar P/ROMs Use Schottky-Clamped TTL To Achieve 50-ns Access

Organized as 2k x 8, a bipolar P/ROM provides a 50-ns typical access time. Maximum access times are 80 ns for the 3636 or M3636 and 65 ns for the 3636-1 from Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. The military (M-prefix) version is guaranteed over a −55 to 125 °C temperature range at ±5% V_{CC} power supply tolerance.

These devices are pin compatible with 8k bipolar P/ROMs and provide three chip selects to facilitate expansion into larger arrays. With typical power dissipation of 0.05 mW/bit, the 16k devices can be used as double-density, low power replacements for 8k devices, which dissipate approximately twice as much power per bit.

The P/ROMs use Schottky clamped TTL technology with polycrystalline silicon fuses to achieve their fast access times. All outputs are initially high, and logic low levels can be electrically programmed in selected bit locations.

Absolute maximum ratings require that output or supply voltages lie between −0.5 and 7 V, while all input voltages must stay in the −1 to 5.5-V range. Output current must not exceed 100 mA. The devices are supplied in hermetic 24-pin DIPs.

Circle 353 on Inquiry Card

Accurate to 1%, Pulse Width Modulator Includes Output Driver

A series of pulse width modulator integrated circuits offer ± 1% reference accuracy and reduce external parts count when used to implement switching power supplies. These devices are designed to fill the need for a combination control IC and output driver. The SG1525 from Silicon General Inc, 11651 Monarch St, Garden Grove, CA 92641, features NOR logic in its output stage, providing a normally low output level; while the SG1527 utilizes OR logic, resulting in a normally high output level. Versions of each series are available for operation over commercial (0 to 70 °C), industrial (−25 to 85 °C), or full military (−55 to 125 °C) temperatures ranges.

These ICs perform a control function similar to that of the SG1524/SG3524 regulating pulse width modulators by

the same manufacturer, except that much of the required external circuitry has been built into the chip. For example, one significant feature is the inclusion of totem-pole output drivers capable of either sourcing or sinking currents to 100 mA. This output configuration will provide the turn-on and turn-off commands to external power transistors and is fully capable of driving VMOS power FETs at frequencies greater than 300 kHz.

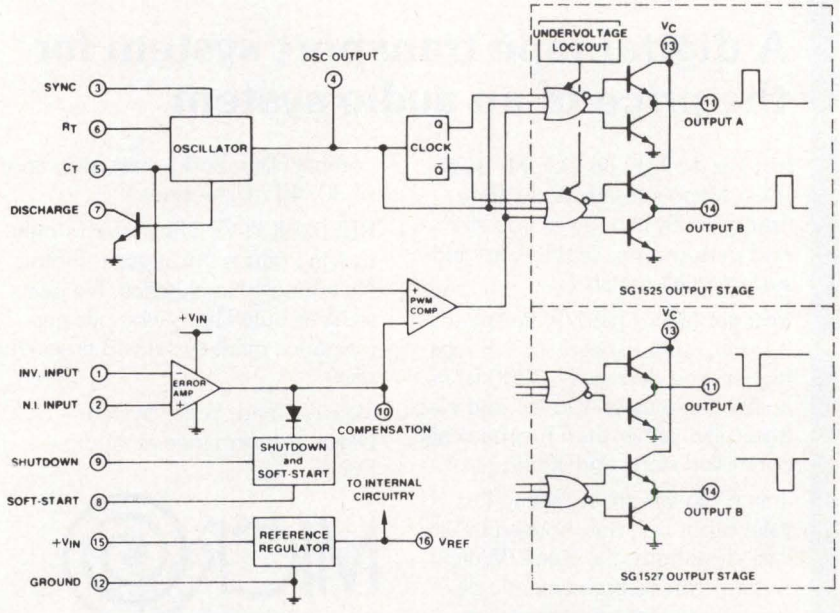
The manufacturer indicates that these chips eliminate design problems relating to addition of networks for common mode division, soft starts, oscillator synchronization, or driving of power transistors. Requirements for a separate deadband control circuit and a reference voltage adjustment potentiometer are also eliminated. The current limiting function of earlier models is omitted from the present series in order to add the interfacing and driving capabilities and thereby remove the need for over a dozen external parts.

Common mode range of the error amplifier includes the reference voltage, eliminating external divider resistors. This onchip 5.1-V reference is trimmed to ±1% initial accuracy. The 5.1-V level was selected to provide two benefits: first, since downstream line drops can only lower the output voltage to the load, starting on the high side provides more efficient use of allowable tolerances; and second, by offsetting the reference from 5 V, exact output adjustment can be accomplished with a single variable resistor.

A synchronization input to the oscillator allows multiple units to be slaved together, or for a single unit to be synchronized to an external system clock. This is designed to eliminate noise transients due to beat frequencies. A single resistor between the C_T pin and the discharge pin provides a wide range of deadtime adjustment. This resistor controls the discharge rate of a timing capacitor to provide a predictable, controllable deadband between the on-times of the two outputs. The circuits also feature internal clamp diodes and a 100-μA current source for built-in soft start, with a timing capacitor as the only external component required. A shutdown pin controls the soft start circuitry, allowing external monitoring devices to initiate soft start.

Absolute maximum ratings limit supply voltage ($+V_{in}$) to 40 V, output collection voltage (V_C) to 60 V, and output current (source or sink) to 200 mA. Reference output current and oscillator charging current are limited, respectively, to 50 and 5 mA. Maximum allowable power dissipation is 1000 mW, derated above 50 °C by 10 mW/°C. The devices are provided in 16-pin DIPs.

Circle 354 on Inquiry Card



Regulating pulse width modulators from Silicon General. SG1525 output stage features NOR logic, while SG1527 features OR logic

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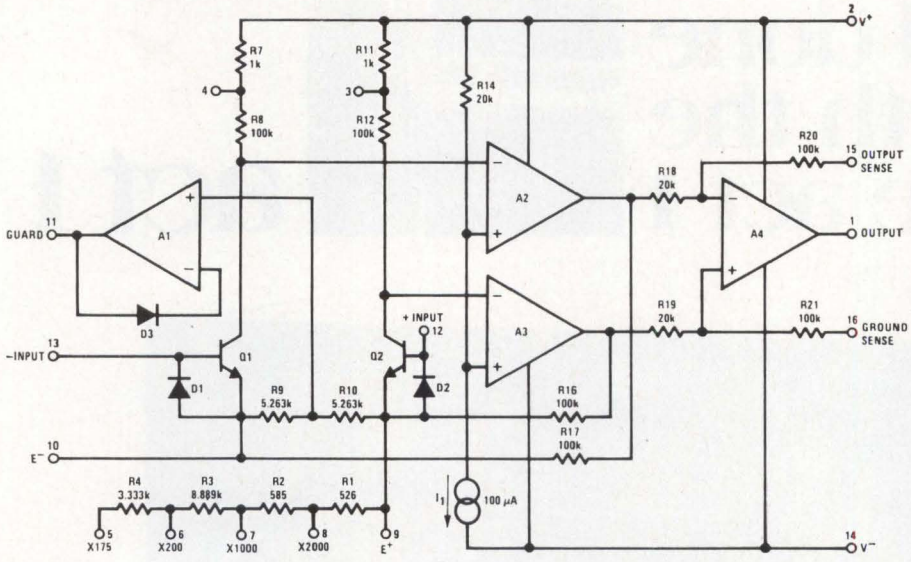
According to the manufacturer, this device equals or exceeds the performance of high precision module true instrumentation amplifiers in most of the key specifications, including gain temperature coefficient, input offset voltage, and input noise voltage. The gain tempco is 7 ppm/°C including the gain setting resistors, in contrast to amplifiers requiring external resistors whose temperature coefficients must be added to that of the amplifier. An input offset voltage of 100 μV max (25 μV typ) with an offset drift of no more than $\pm$0.25 μV/°C is guaranteed over the operating temperature range. Input noise from 0.1 to 10 Hz is only 0.2 μV pk-pk and gain nonlinearity is 1 ppm at all gain settings. Common mode rejection and power supply rejection are each 120 dB. The operating temperature range is -55 to 125 °C for the D-suffix and -25 to 85 °C for the CD-suffix version, each provided in a hermetically sealed 16-lead DIP. In addition, MIL-STD-883 processing is available.

This is a 3-stage amplifier, composed of a well matched differential transistor pair, a common mode loop amplifier, and a differential to single-ended amplifier. It is provided with a guard drive output, which will always be at the input common mode voltage. The guard drive amplifier is short circuit proof and is capable of driving several thousand picofarads without danger of latch-up or oscillation, and its output is connected to the case to provide electrostatic shielding of the system. Tied to a shielded input, the guard drive will greatly reduce noise pickup and will also improve CMRR by maintaining the shield at the common mode voltage.

The feedback network of the device may be closed directly at the load in order to eliminate errors due to lead resistance. Also, a unity gain buffer may be included within the feedback loop to increase output current capability. Offset is trimmed at the factory to a very low value, but may be trimmed further by using a 10-kΩ, 10-turn, 100-ppm/°C potentiometer.

Input bias current is about 50 nA. The input stage bias is optimized for minimum voltage noise so that the input bias currents are higher than might otherwise be expected. However, the matched input currents result in an offset current value much lower than might be inferred from the bias current. To take advantage of this low offset current, the source impedances seen at both inputs should be matched to minimize dc drift. Bias current is relatively constant with temperature (as compared to an FET stage).

The device has been overcompensated purposely to be free from any undesirable transient response. Small signal settling time is governed by the gain bandwidth product, while large signal settling time is dominated by slew rate. Settling time to 0.01% is 60 to 80 μs, large signal bandwidth is 1.6 kHz, and slew rate is 0.3 V/μs.



National Semiconductor's LH0038/LH0038C true instrumentation amplifier features ultralow values for offset voltage, offset drift, and input noise. It is designed to be equivalent to module level products at lower cost

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The schedule for the 1979/80 Series is:

Sept. 6, 1979	Palo Alto, CA
Sept. 26, 1979	Minneapolis, MN
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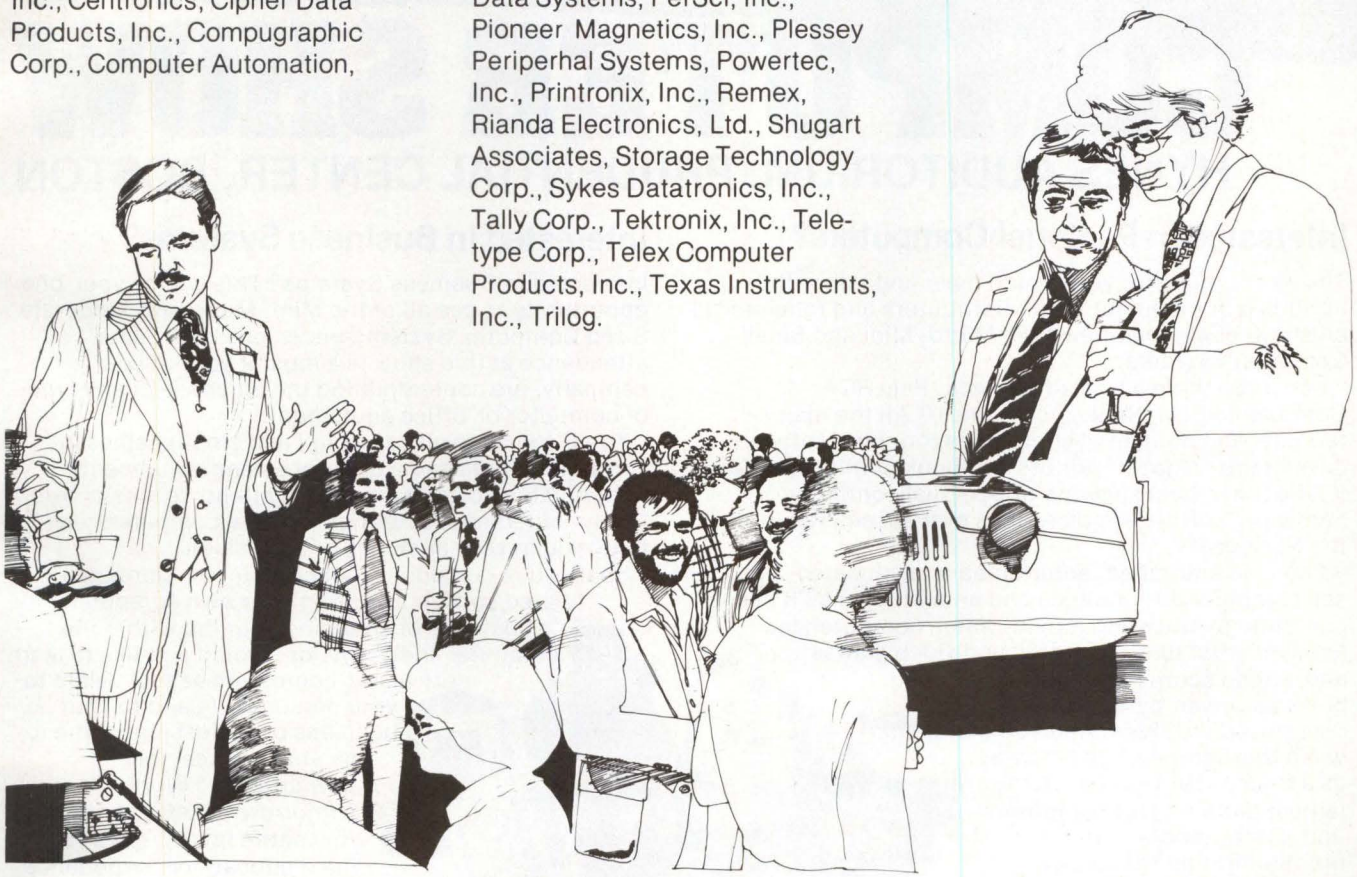
Nov. 15, 1979	Southfield, MI
Jan. 15, 1980	Orange County, CA
Feb. 6, 1980	Ft. Lauderdale, FL
Mar. 25, 1980	Dallas, TX
Mar. 27, 1980	Houston, TX
April 28, 1980	Atlanta, GA

Invitational Computer Conferences



Invitations are available from participating companies or the ICC sponsor. For further information contact: B.J. Johnson & Associates, 2503 Eastbluff Drive, No. 203, Newport Beach, CA 92660. (714) 644-6037

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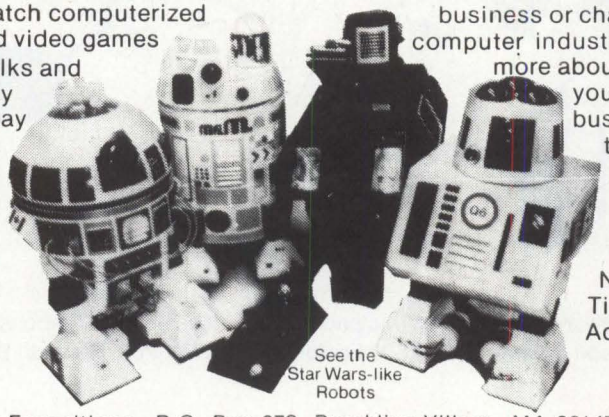

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Produced by Northeast Expositions, P.O. Box 678, Brookline Village, MA 02147 (617) 522-4467

Multichannel Analog Switch IC Offers High Reliability

Built with dielectrically isolated PMOS to provide input diode protection on the analog inputs and junction isolation for the rest of the circuitry, an analog switch IC can be used at data rates up to 500k-bits/s. The MS-300 from Lockheed Microelectronics Center, Lockheed Missiles & Space Co, PO Box 504, Sunnyvale, CA 94086, is a 9-channel expandable switch array with a common source. Mean time before failure estimates for the device are based on data that include in-service orbiting satellite usage of >90M hours without a failure.

Small signal on-resistance is 400, 500, and 700 Ω at −55, 25, and 125 °C, assuming a gate to source bias voltage of −12 V and a drain to source current of −100 μA. Off-resistance for all channels is greater than 10^7 Ω. Switch thresholds are matched to within 500 mV and on-resistances to within 75 mV. Breakdown voltages are −28, −28, and −30 V respectively for BV_{ds}, BV_{sd}, and BV_{gs} at 25 °C.

There are two versions of the IC, differing in input leakage current. At 125 °C operating temperature and gate voltage of −15 V, the drain and gate leakage currents are specified at −1.6 μA for the -003 suffix version (MS-300-003) and at −2.0 μA for the -004 suffix.

The device can operate over the full −55 to 125 °C military range and can be stored from −65 to 150 °C. Maximum power dissipation is 635 mW at 25 °C, with power derated by 5.1 mW/°C above that temperature. Both the control voltage (gate) and analog signal (drain) inputs, which are biased by the most positive and negative supplies in the system, can range from −30 to 0.3 V.

Circle 355 on Inquiry Card

Comparator/Multiplexer Chip Offers Multiple Levels

Seven levels of comparison are provided by a monolithic comparator/multiplexer circuit, the LS7240 from LSI Computer Systems, Inc, 1235 Walt Whitman Rd, Melville, NY 11747. The chip is designed specifically to take advantage of the 24 parallel BCD outputs of the 6-decade up/down counter, the LS7040, by the same manufacturer. With the addition of a single external switch, two or more chips can be used with the counter, giving the user as many levels as needed.

All seven comparators in the 24-input chip can be loaded with one set of seven thumbwheel switches, the first selecting the comparator to be loaded, and the second through sixth selecting the digit. The contents of any comparator or of the up/down counter are available at any time in the form of multiplexed BCD output for 7-segment display.

Circle 356 on Inquiry Card

Single Chip Combines Linear Multiplier and High Gain Op Amp

A low cost monolithic multiplier-detector is designed for use in amplitude modulated communications systems. Manufactured by Exar Integrated Systems, 750 Palomar Ave, Sunnyvale, CA 94088, the XR-2228 includes a 4-quadrant linear multiplier (or modulator) and a high gain operational amplifier.

The chip's multiplier section contains fully differential and independent X and Y inputs, and features a wide common mode range. Thus it can interface with any commercially available monolithic phase locked loop circuit to perform phase locked am detection, am generation, and triangle to sinewave conversion. The wide transconductance bandwidth of the multiplier section makes it suitable for am detection or generation applications up to 100 MHz.

For maximum versatility, the multiplier and operational amplifier sections are not internally connected. The op amp can also function as a preamplifier for low level input signals, or as a post detection amplifier for synchronous demodulation or sine shaper applications.

Available in 16-pin ceramic or plastic DIPs, the IC can operate with supply voltages of ±4.5 to ±16 V. Pricing is as low as $1.62 in 100-up quantities. □

Circle 357 on Inquiry Card

PRODUCTS

Desktop Computer Offers Full Flexibility For Office Environment

Modularity of configuration and ease of use are said to be key values of the model 655 desktop computer. Designed specifically for office use, the system consists of three hardware modules: electronics package, CRT display, and keyboard. Software consists of applications programs supplied by the system manufacturer or by other sources. Placement of each hardware module depends on user preference.

The electronics package is made up of central processing unit, internal memory, one or two built-in mini-diskette drives, power supply, input/output, and facilities for expansion. Internal semiconductor memory is made up of 48k to 60k bytes; direct memory access is optionally available to free the CPU during operation with high speed disc drives.

Each 5.25″ (13.3-cm) mini-diskette has a capacity of 147k bytes. In addition, for applications requiring mass storage, a hard disc option provides 19.2M bytes on removable cartridges (9.6M bytes/disc).

Location of the 12″ (30.5-cm) CRT display may be in any position desired by the user. An optional tilting mechanism provides choice of viewing angle. The presentation is 80 char by 20 lines, with a full 128-char ASCII format, plus punctuation marks, most European characters, and math and graphic symbols. Character size is said to be "almost twice as large as those on most comparable systems." A contrast enhancing filter eases viewing in very brightly lit rooms.

"Typewriter" layout of the keyboard enables operation by clerical personnel with minimal training. A full numeric keypad allows rapid entry of numeric data. Twenty user-definable keys are also provided.

A built-in interface accommodates most serial input printers. Those available with the system are a 55-char/s typewriter quality unit with 10 or 12 char/in (4 or 5/cm) and multiple type fonts that prints up to 162 columns wide, and a 160-char/s bidirectional dot matrix unit that prints up to 132 columns wide. Optional plug-in interfaces enable dual and quad RS-232-C (V.24) serial communications, synchronous to 9.6k baud, asynchronous to 38k baud, in half- or full-duplex operation.

A library of available application programs contains many developed for the company's earlier series computers plus those available from other sources. The extended BASIC language provides interpretive or compiled operation, 12-digit precision floating point, variable string length, multi-dimensioned arrays; logical operators, assembly language calls, FMS interface, word processing file interface, program chaining, access to the 20 program-defined keys, and full CRT data manipulation.

The electronics package measures 6.75 x 17.75 x 16.75″ (17 x 45 x 42.5 cm) and weighs 30 lb (14 kg); the CRT display is 9.75 x 12.75 x 16.75″ (25 x 32 x 42.5 cm) and 15 lb (7 kg); the keyboard is 2.75 x 17.75 x 8.25″ (7 x 45 x 21 cm) and 7 lb (3 kg). Power requirements are 90 to 130 or 200 to 240 V, 50/60 Hz, 100 W. Temperature ranges are 50 to 104 °F (10 to 40 °C) operating, −40 to 150 °F (−40 to 65 °C) nonoperating.

Price and Delivery

Starting price for a 655 system is $5400. Delivery is 30 days ARO. Compucorp, 1901 S Bundy Dr, Los Angeles, CA 90025. Tel: 213/820-2503.

Circle 198 on Inquiry Card

8″ Winchester Disc Drive Mass Storage Device Has 20 R/W Heads

Mikro-Disc™ 211, a small (180 in^3, 2950 cm^3) disc drive based on a modified Winchester technology, features an 8″ (20-cm) outside diameter hard disc plus a proprietary low mass multiple head assembly that provides ultrafast data access. Intended as a replacement for floppy discs or as a supplement for floppies or other mass storage devices, this drive has 20 read/write heads.

Full unformatted storage capacity per disc surface is 2.1M bytes (267k bytes/cylinder, 13k bytes/track). Formatted capacity is 1.9M bytes (24 sectors/track, 512 bytes/sector, 246k bytes/cylinder, 98k bits/track). Track to track head positioning time is 5 ms and average access time to the entire capacity of the disc is 18.825 ms.

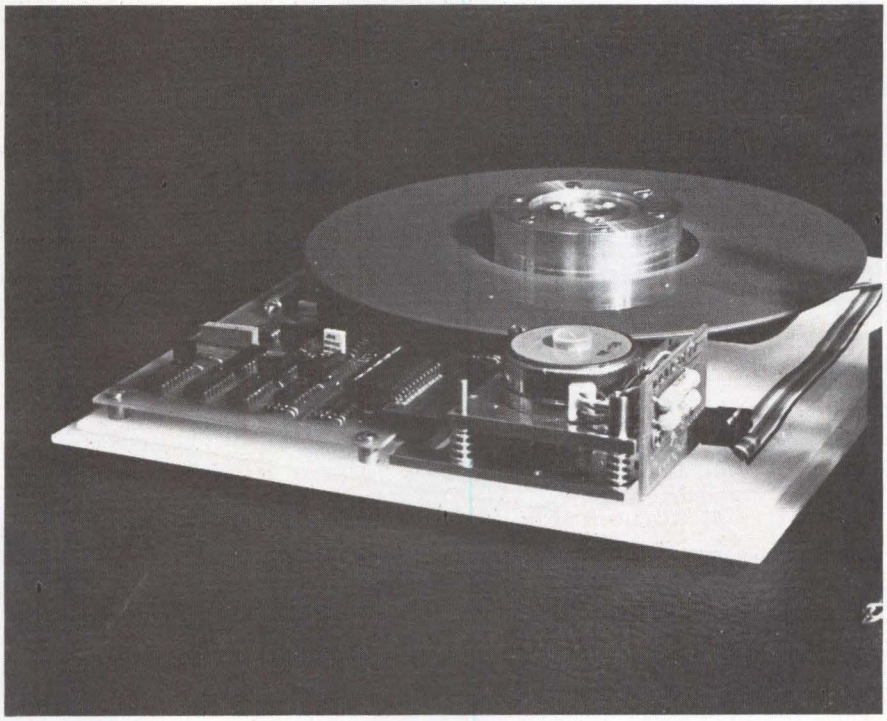
Recording area for 160 tracks on the lubricated oxide disc is 1.6″ (4 cm). (Each disc has eight cylinders with 20 tracks/cylinder.) The heads fly at 20 μin (0.51 μm) to record data in MFM format at 8000 bits/in (3150/cm). Because of the multiple R/W heads, one cylinder of 0.25M bytes is always immediately available without repositioning the head assembly.

Disc rotational speed is 3400 r/min, providing a data transfer rate of 765k bytes/s (6M bits/s). Rotational delay is 17.65 ms and average latency is 8.825 ms.

Data reliability is <1 in 10^{10} bits soft error, <1 in 10^{12} bits hard error. Positioning errors are <1 in 10^6 accesses.

Power requirements are <50 W, 110 Vac at 300 mA, 24 Vdc at 1.5 A (max), −5 Vdc at 250 mA. Physical dimensions are 9.5 x 2.0 x 9.5″ (24 x 5 x 24 cm). Weight is <8 lb (3.6 kg).

Operating environmental specifications are 41 to 113 °F (5 to 45 °C) at 20 to 80% humidity noncondensing, sea level to 10,000 ft (3 km). Storage specifications are −17 to 150 °F (−27 to 65 °C). Mean time between failures is >5000 h; mean time to repair is <30 min.



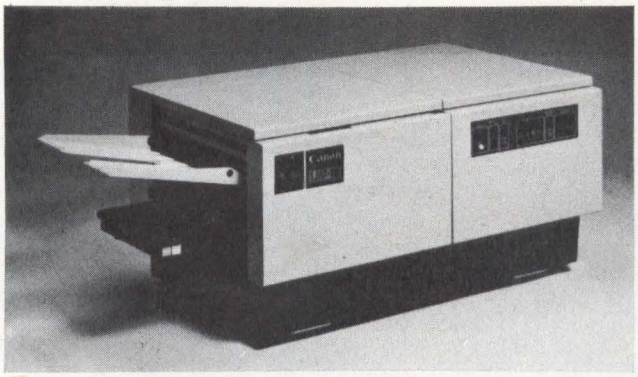
Price and Delivery

The Mikro-Disc 211 will be priced at less than $1000 in OEM quantities of 100 units. Selected customers will receive evaluation units this month; pilot production is scheduled for the first quarter of 1980. New World Computer Co, Inc, 3176 Pullman St, Suite 119, Costa Mesa, CA 92626. Tel: 714/556-9320.

Circle 199 on Inquiry Card

PRODUCTS

Compact Laser Beam Printer Adapts to Smaller OEM Systems



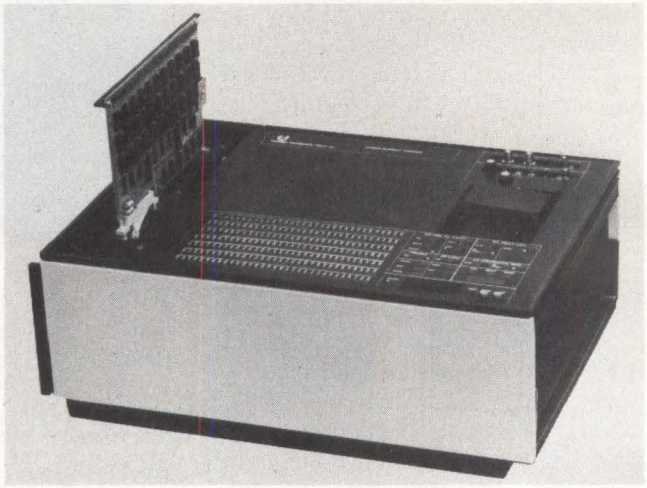
Semiconductor laser beam recording technology used in the LBP-10 is based on a high precision scanning system and high contrast NP electrophotographic technology. With the nonimpact printing method, the beam writes directly on the NP-photoreceptor. The desktop medium speed printer produces 880 lines/min and handles data and word processing, graphics, and facsimile in small systems or as part of a distributed data processing system. Noise level is under 57 dB. NP standard plain paper, available in letter, legal, and 7 other sizes, is loaded from cassettes. A liquid-dry method is used for development. Power requirements are 120 Vac, 60 Hz and consumption is 0.96 kVA (8 A max, 120 Vac). The standard interface is video signal; 8-bit parallel code interface and serial interface are optional. A built-in self-diagnosing function locates faults. **Canon U.S.A., Inc,** 10 Nevada Dr, Lake Success, NY 11042.

Circle 200 on Inquiry Card

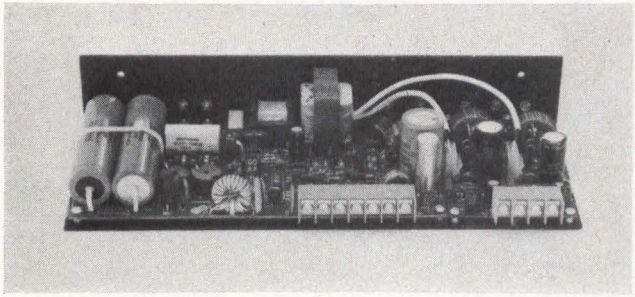
Test/Programming Station Complex Logic Circuit Boards

Users of the model 3PX550 logic circuit test/programming station with an optional TTY or CRT terminal, will be able to assemble, edit, and debug logic board test programs as well as generate test programs online. The microprocessor based system applies stored program logic vectors and/or pseudorandom patterns to the logic circuit and verifies the output response—either simultaneously at selected program steps or singularly by waveform signature analysis. Each circuit test failure is reported by a light; failures in test numbers, pin numbers, and TNT signatures are listed in hardcopy on the TTY or are displayed on the CRT. Operator inputs are converted to machine language by the resident assembler. An autolearn mode allows new programs to be tested against known-good boards. **Three Phoenix Test, Inc,** 21639 N 14th Ave, Phoenix, AZ 85027.

Circle 201 on Inquiry Card



Open Frame Switching Power Supplies Feature 0.2% Regulation On All Outputs



Circle 202 on Inquiry Card

Series of 150-W fully regulated multiple-output switching supplies with good efficiency allow full output operation in a convection environment. Single-output LR9500 models offer 5 V at 20 A, 12 V at 12.5 A, or 15 V at 10 A in a 4.97 x 2.2 x 9″ (12.62 x 5.6 x 23-cm) package. Triple-output models LR9700 contain an LR9500 main supply and 2 auxiliaries of 5, 12, or 15 V at up to 3 A or 36 W. LR9800 units add a fourth auxiliary of up to 15 V at 1 A in a 4.97 x 2.2 x 13″ (12.62 x 5.6 x 33-cm) package. Meeting UL478 requirements, the series has 0.2% regulation and true convection cooling while operating from 115 or 230 Vac nom. Each auxiliary is independently regulated and current limited, and has individual thermal shutdown. All models operate over ±20% input voltage range; input has low line protection to guarantee sufficient power transistor base drive. Ripple and noise on all outputs is <50 mV pk-pk. **California DC,** 31117 Via Colinas, Westlake Village, CA 91361.

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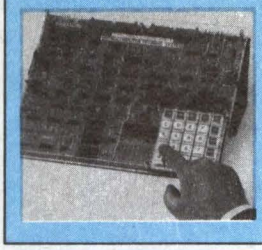
Microprocessors & Microcomputers



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Troubleshooting Microprocessor-Based Systems

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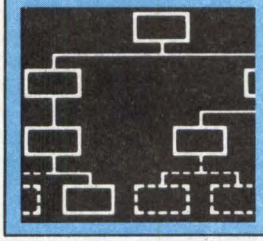
Structured Programming



LOS ANGELES
October 16-19
WASHINGTON, D.C.
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BOSTON
November 6-9
SAN FRANCISCO
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WASHINGTON, D.C.
February 5-8

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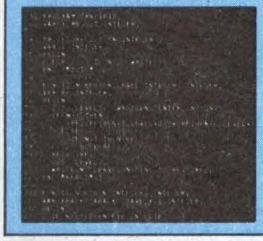
PASCAL: Programming in the Structured Language

NEW



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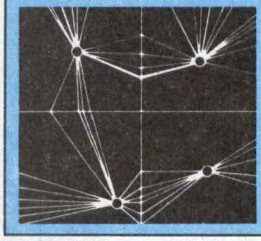
November 6-9
BOSTON
November 13-16
LOS ANGELES
December 4-7

Course 350—Four Days

Distributed Processing & Computer Networks



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LOS ANGELES
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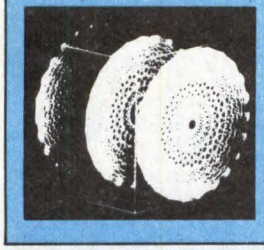
October 30-November 2
SAN DIEGO
January 22-25

Course 365—Four Days

Computer Graphics



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September 18-21
WASHINGTON, D.C.
September 25-28
CHICAGO
October 9-12
NEW YORK
October 16-19
LOS ANGELES
October 30-November 2
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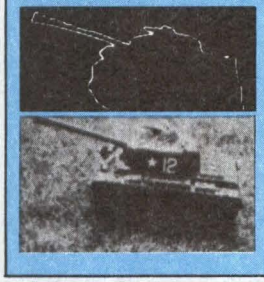
WASHINGTON, D.C.
February 12-15

Course 410—Four Days

Digital Image Processing

NEW



WASHINGTON, D.C.
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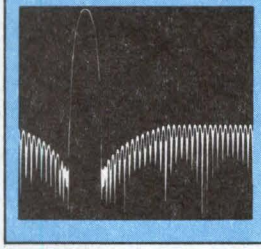
LONDON
October 23-26
LOS ANGELES
December 11-14

Course 412—Five Days

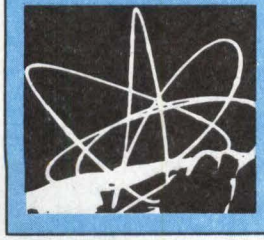
Digital Signal Processing



WASHINGTON, D.C.
September 17-21
BOSTON
September 24-28
LOS ANGELES
October 15-19
CHICAGO
October 22-26
SAN DIEGO
November 5-9
HOUSTON
January 21-25
WASHINGTON, D.C.
January 28-February 1

Course 440—Four Days

Fiber Optic Communication Systems



WASHINGTON, D.C.
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LOS ANGELES
November 13-16

Course 475—Four Days

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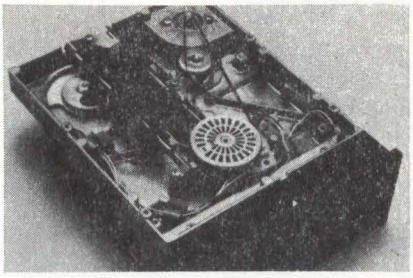
300 N. Washington St./Suite 103
Alexandria, VA 22314
(703) 548-1333
(WASHINGTON, D.C.)

CIRCLE 106 ON INQUIRY CARD

PRODUCTS

DOUBLE-SIDED 5" FLOPPY DISC DRIVE



Model 6108 offers same compact design of 6106 single-head version with twice the capacity. Unformatted capacity is 4M bits in double-density recording, 2M bits in single density. Drive allows recording on 40 tracks/side of disc, compared with 35 tracks for Shugart's SA-400 drive. Track to track access time is 12 ms, three times faster than the industry std of 40 ms. The unit consumes one-third less power than the industry std and produces less heat. It can be operated in FM, MFM, M²FM, and GCR recording modes. **BASF Systems,** Crosby Dr, Bedford, MA 01730.

Circle 203 on Inquiry Card

CONTROLLER UNIT FOR SWITCHES

Controller unit serves as amplifier and power supply for the E3N and E3S photoelectric switches and the TL-X series cylindrical type proximity switches. The UL-approved S3S controller unit is available in three types that can additionally perform standard on-off, on-off delay/memory, and amplifier control functions. **Omron Electronics,** Inc, 650 Woodfield, Schaumburg, IL 60195.

Circle 204 on Inquiry Card

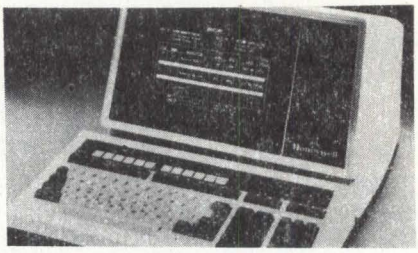
IMAGE PROCESSING LIBRARY

Scientific subroutines library is composed of 11 2-dimensional filtering, convolution, and FFT routines written in AP assembly language and callable from host FORTRAN. These computational tools filter and enhance monochrome color and multispectral scanner images involved in array processor applications. The 4 utility routines are Extended Complex Vector Move, Unnormalized Extended S-PAD Float, Extended S-PAD Float, and Unsigned S-PAD Float. **Floating Point Systems, Inc,** 11000 SW 11th St, Beaverton, OR 97005.

Circle 205 on Inquiry Card

CRT DISPLAY TERMINALS

VIP7800 family consists of 12" (30-cm) 7804 and 15" (38-cm) 7805 models that communicate synchronously with a host and can be multidropped on one communications line with other synchronous terminal products. 15" 7802 is an asynchronous unit. When connected directly to a host computer all terminals operate at transmission rates up to 19.2k bits/s. Options include buffered printer adapter, 72-line vertical scrolling feature, keylock, and choice of white or green char on dark background. **Honeywell, United States Information Systems Group,** 200 Smith St, Waltham, MA 02154.



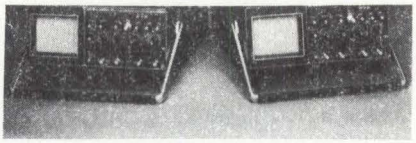
Circle 206 on Inquiry Card

12-STEP UPS SYSTEM

The pulse-width-controlled static power converters in UPS rectifier and inverter stages achieve 87 to 90% operating efficiency. Rectifier circuitry restricts input total harmonic distortion to <10% and provides regulated voltage. Inverter section employs impulse-current commutation, single-pulse-width modulation, and dual phase-shifted transformer-connected inverters. Output voltages of 75-, 100-, and 150-kVA models may be adjusted ±5% from rated UPS output. **Sola,** 1717 Busse Rd, Elk Grove Village, IL 60007.

Circle 207 on Inquiry Card

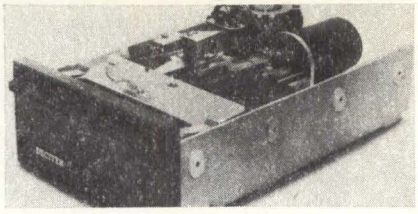
GENERAL PURPOSE 35-MHz OSCILLOSCOPES



Portable PM 3216 and 3218 have a max sweep speed of 10 ns/div and trigger hold-off facility that eliminates double triggering on digital signals. PM 3216 is a dual trace, single timebase model; 3218 is a dual trace dual timebase unit with an alternate timebase display. Units have a 2-mV sensitivity over the 35-MHz bandwidth, coupled with trigger sensitivity of 1 div, and an external trigger sensitivity of 200 mV. **Philips Test & Measuring Instruments, Inc,** 85 McKee Dr, Mahwah, NJ 07430.

Circle 208 on Inquiry Card

8" FLOPPY DISC DRIVES



Models 8000/L and /S offer 125-ms and 290-ms avg access times, respectively. Both single-sided drives have direct drive head positioning systems—/L uses a voice coil linear motor, /S a linear stepper motor; are modular in construction; and have microprocessor controlled index and sector mark generation and head motion. Recording rates are 250k bits/s single-density (FM) and 500K-bits/s double-density (MFM). **Decitek, Div of Jamesbury Corp,** 129 Flanders Rd, Westboro, MA 01581.

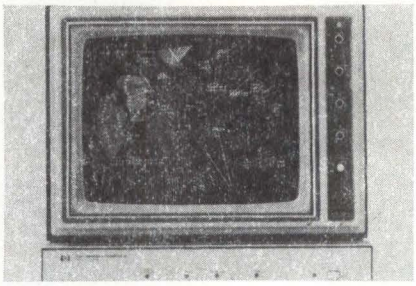
Circle 209 on Inquiry Card

LOW PROFILE DIP SOCKETS

When flush mounted in a PCB, ICO series sockets have an 0.08" (2.03-mm) height, allowing min board to board spacing. Built-in standoffs for onboard mounting allow an 0.09" (2.3-mm) space under socket for air circulation and inspection. 8-through 42-contact sockets are side and end stackable. Brass socket shells are gold, nickel, or tin plated. Beryllium contacts are gold finished. **Samtec, Inc,** 810 Progress Blvd, New Albany, IN 47150.

Circle 210 on Inquiry Card

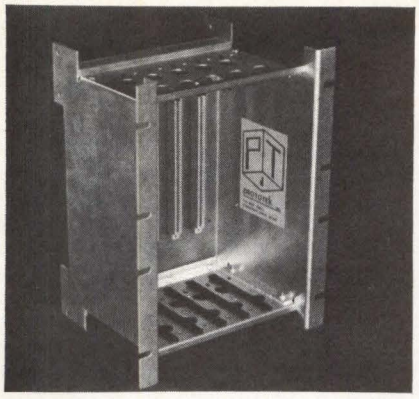
GRAPHICS DISPLAY SYSTEM



Combining a model 1350A graphics translator (with HP-IB interface) and a 1311A large screen X-Y display along with connecting cables results in the 1350S system that accepts digital data from computers and translates it into a graphics display. Data are stored in digital memory which continually refreshes the display. Any number of vectors or char can be entered without erasing or rewriting all 2k memory locations. Up to 32 files are available for storage. **Hewlett-Packard Co,** 1507 Page Mill Rd, Palo Alto, CA 94304.

Circle 211 on Inquiry Card

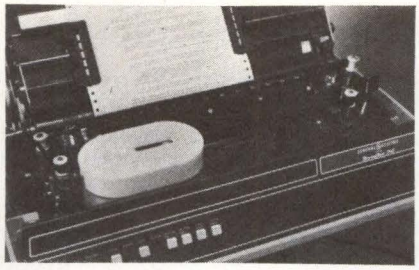
PROTOTYPING SYSTEM CARD CAGE



Series 105 modular 9.5″ (24-cm) aluminum card cage mounts in a small enclosure or can be ganged 2 together to fit a std 19″ (48-cm) rack. Dual-card packing densities of 11 cards at 0.6″ (1.5-cm) spacing or 5 cards at 1.2″ (3-cm) spacing are accommodated. Bused PC or wirewrappable card backplanes are available; both backplanes are 0.125″ (0.3175-cm) G-10 epoxy glass. Bused signals terminate with 1-kΩ pullups. The S-100 bus compatible unit is available in kit form. **Prototek, Inc,** PO Box 46512, Cincinnati, OH 45246.

Circle 212 on Inquiry Card

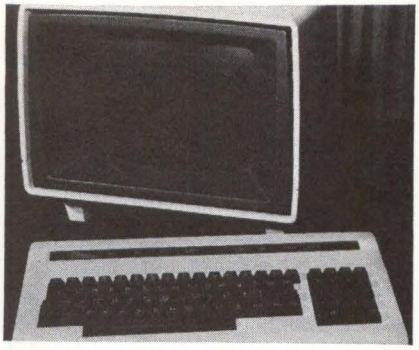
LINE PRINTER WITH LETTER QUALITY OUTPUT



Combining 340-line/min speed with print quality, TermiNet® 340 CP (correspondence printer) incorporates a rotating belt print principle and is enhanced with a multistrike carbon film ribbon cartridge that is operator replaceable and a continuous carrier that will host most letterhead stocks. Additional features include a servo controlled paper drive, operator selectable 6- or 8-lines/in (2.4 or 3.1/cm) spacing, and a programmable 8-channel vertical format unit. Printer interface is bit parallel (serial interface is available). **General Electric Data Communication Products Business Dept,** Waynesboro, VA 22980.

Circle 213 on Inquiry Card

MICROPROCESSOR CONTROLLED CRT TERMINAL



Entry "81" features a detached typamatic 81-key English language typewriter style solid state keyboard with N-key rollover. Other featuers are u/lc char with descenders, conversational and block transfer, 128 user defined functions, 19-key numeric pad, and a transparent print mode which allows the host CPU to print 132-col data at different baud rates through the CRT. Edit capability is built in. LED status display allows visual feedback about operating modes. **DTI, Data Terminals Corp,** 354 Woodland St, Holliston, MA 01746.

Circle 214 on Inquiry Card

Canon®

D.C. MOTORS for OEMS

subfractional—0.00025 to 0.05 h.p.

Canon offers OEM users one of the world's broadest selections of subfractional h.p. d.c. motors at very competitive prices. Choose from literally hundreds of existing models, or, if you are a large quantity user, we'll supply units to your precise specs. Stall torques range from 0.24 to 35 oz.-in., speeds to nearly 10,000 rpm ungeared. Most are available for broad voltage ranges.

Mountings: Most are tapped for front mount. Others available.

Shafts: Length, flats, pinions, pulleys, etc. to customer specs.

IRON CORE

Line includes low cogging models and models with extra long life brushes.

Ungoverned
0.24 to 35 oz.-in. stall torque

Governed
Mechanical and Electronic
0.5 to 20 oz.-in. stall torque

BRUSHLESS

0.4 to 4.2 oz.-in. stall torque
with or without electronics

MOTOR-TACHS

1.1 to 35 oz.-in. stall torque
a.c. or d.c. output

MOTOR-GEARHEADS

to 140 oz.-in. output torque
Reductions from 1/5 to 1/3000 offset or concentric shafts. Mate with most Canon Iron Core and Brushless Motors.

Short Form Specifications Catalog and Data Sheets on individual motors available.

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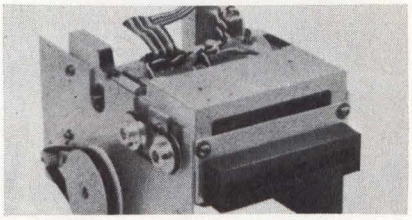
CIRCLE 107 ON INQUIRY CARD

CARD/BADGE READER



Std punched tab cards, as well as Type 3 plastic badges, are read by the CB2 series reader on an intermixed basis. Various configurations and a data communication interface up to 9600 baud are available. It mounts in a data terminal or can be used as a standalone reader. A reciprocating mechanism, which permits reading during insertion and/or on the return, allows for data verification. Options are offered for straight-through feed and for stacking captured cards. **Peripheral Dynamics, Inc,** 1850 Gravers Rd, Plymouth Township, Norristown, PA 19401.
Circle 215 on Inquiry Card

COMPUTER COMPONENT POWER DISTRIBUTION SYSTEM

System II model B accepts raw power from the building source and transforms it into the CPU's precise voltage requirements for distribution to the individual system components via flexible conduit. A master power center selects a reporting center for emergency conditions; a slave power center reports its power status to the master unit for analysis. These models may be interchanged or reassigned. The system status panel is equipped with a UPS. **Computer Power Systems Corp,** 3398 E 70th St, Long Beach, CA 90805.
Circle 216 on Inquiry Card

PLUG TO FLAT RIBBON CABLE CONNECTORS

Designed for mass termination of multiconductor cables, wirewrap and solder style right angle plugs (3612550-01) have a dual-fingered readout for mating with up to 72-position connector receptacles. Dual-readout connector receptacles (3612445-01) contain bifurcated gold plated beryllium contacts. Insulation piercing U contacts are on 0.050″ (1.27-mm) center, staggered to accept 0.100″ (2.54-mm) spaced fingers. **Mupac Corp,** 646 Summer St, Brockton, MA 02402.
Circle 217 on Inquiry Card

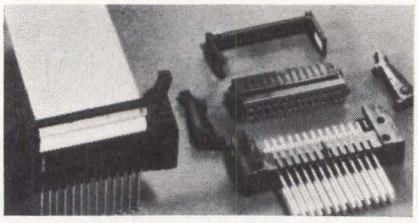
HIGH PERFORMANCE 8″ FLOPPIES

A calibrated flexible diskette, part of the Optima Series, has recorded values for amplitude, resolution modulation, and bit shift, and can eliminate the need to develop primary or gold std media. Manufacturing tests maximize recording integrity; performance values are individually recorded on a spec card included in the diskette package. A hub reinforcement ring is std. Alignment diskettes, for single- and double-sided uses, align recording heads. **Verbatim Corp,** 323 Soquel Way, Sunnyvale, CA 94086.
Circle 218 on Inquiry Card

INCREMENTAL ENCODER

Capable of resolution to 200k pulses/r, 3.5″ (8.9-cm) Digisec® R1 _/35 (C) uses solid state LEDs for long life light sources. Available with 128k, 144k, 160k, or 200k resolution power, the encoder is designed to meet military environments and operates in temps ranging from −40 to 71°C. It can be interfaced directly with a display which contains an up/down counter and readout. Typ applications include position and rate feedback of precision machine tool controls. **Itek Measurement Systems Div,** 27 Christina St, Newton, MA 02161.
Circle 219 on Inquiry Card

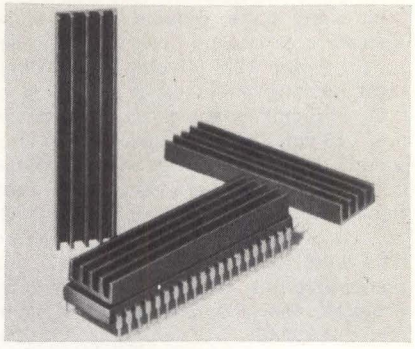
FLAT CABLE CONNECTORS AND PCB HEADERS



Preassembled lid and body of IDS series leaves only 1 part to be handled in assembly. An optional strain relief bar ensures reliable cable connection. An ejector/latch, also optional, on the IDH series keeps socket firmly in place when latched and serves as a socket ejector with opened. Headers are available for straight or right angle mounting, solder or wrap/pin termination. System is suited to high speed assembly, using tooling already in place. **Robinson-Nugent, Inc,** 800 E Eighth St, New Albany, IN 47150.
Circle 220 on Inquiry Card

DIP HEAT SINKS

Series 5085 accommodates DIPs with 24, 28, 40, or 64 pin counts. Designed to require no additional PC board space, units can be installed before or after final board assembly. Supplied in black anodized finish per MIL-A-8625, Type 11, they can be bonded to the top surface of the package with the company's Ther-O-Bond 1400 or 1500 or equivalent. **Aavid Engineering, Inc,** 30 Cook Ct, Laconia, NH 03246.



Circle 221 on Inquiry Card

COMPUTER POWER CENTERS

Producing clean power for computer equipment, the Powerpac portable peripheral provides a central node for power distribution to the computer system and establishes an effective single-point ground. Std models range from 5 to 50 kVA. The unit also provides power from its isolation transformer, which has adjustable taps and an electrostatic shield between primary and secondary windings. Up to 42 single-phase, 16 3-phase, or a combination of lines are possible. **Emergency Power Engineering, Inc,** 3595 Cadillac Ave, Costa Mesa, CA 92626.
Circle 222 on Inquiry Card

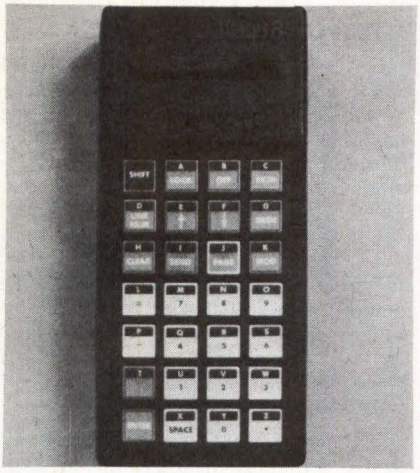
3-TERMINAL SWITCHING REGULATORS

For use in hybrid power supply designs, 3T-12AP-1001 is a noninverting step-down regulator taking 10 to 40 V and developing a user adjustable, regulated output from 4.5 to 30 V at 0 to 12 A. Magnitude of the output can be less than, equal to, or exceed by up to 5 V the magnitude of the input. 3T-5AN-1001, a similar inverting regulator, takes 10 to 40 V and develops −4.5 to −30 V at 0 to 5 A. Both feature 1% regulation from 0 to full load, 20-turn potentiometer, current limiting, and short circuit protection. **Boschert Inc,** 384 Santa Trinita Ave, Sunnyvale, CA 94085.
Circle 223 on Inquiry Card

MICROPROCESSOR BASED MINI-FLOPPY DISC DRIVE

Emulating paper and magnetic tape, Digidisk system allows an operator to prepare and edit messages and data offline for future retrieval or online transmission. The unit will operate with any data communication printer or CRT terminal through an RS-232 interface. The system uses a flexible mini-disc with a capacity of more than 73k characters. As program control resides on the disc; the latest version of the disc updates the system. **Digicom Data Products, Inc,** 1440 Koll Cir, Suite 108, San Jose, CA 95112.
Circle 224 on Inquiry Card

MULTIAPPLICATION DATA ENTRY TERMINAL

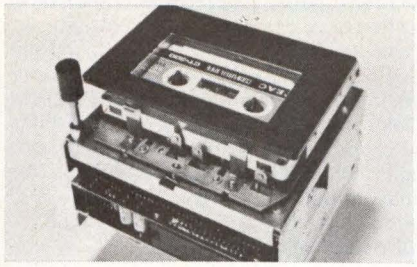


The Omega Concept of program loadable handheld 2-way communications terminal systems enables a user to design an application terminal for a specific job, and then expand. Terminals can add preprogrammed modules for order entry, cash/sales reporting, and time and attendance accounting; an ECOM module permits downloading of application programs directly from a remote host computer. Unprogrammed modules can be programmed by the user. MSI/88 terminals are offered in 3 versions. **MSI Data Corp,** 340 Fischer Ave, Costa Mesa, CA 92626.
Circle 225 on Inquiry Card

OPTICAL VELOCITY ENCODERS

For use freestanding or in conjunction with various motor series, small size encoders are available as 15, 100, or 250 pulses/r. Model 01A, which generates 15 pulses/r, is also furnished in a 2-gate version for indication of direction as well as velocity. Its linearity error is <0.4%. Linearity error in the 100 pulses/r model 04A is <1%. **Micro-Mo Electronics, Inc,** 3691 Lee Rd, Cleveland, OH 44120.
Circle 226 on Inquiry Card

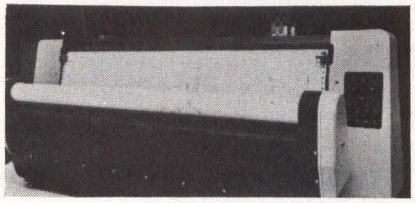
DIGITAL TAPE CASSETTE DRIVE



TEAC MT-2 is offered in 4 versions: single- or dual-gap head and with or without the interface controller. The formatted configurations are ANSI/ECMA compatible, and provide most of the interfacing to 8080, Z80, 6800, and other 8-bit parallel chips. The 3 x 4 x 5″ (8 x 10 x 13-cm) drive reads/writes 800 bits/in (315/cm) at 15 in (38 cm)/s and searches at 45 in (114 cm)/s. A 10k-hour MTBF insures reliability. **Triple I, Inc,** 4605 N Stiles, Oklahoma City, OK 73154.
Circle 227 on Inquiry Card

PRODUCTS

COMPUTER OUTPUT PLOTTERS



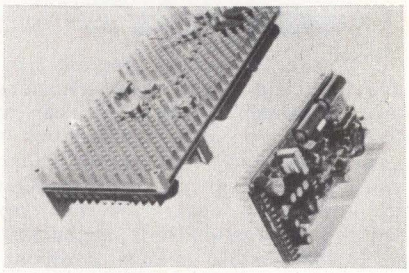
Plotters for the computer graphics industry allow both roll and fanfold paper, and range in width from 15 to 48″ (38 to 122 cm) with up to 4 plotter pens. Controller hardware/software is designed to accept logic inputs of 16-bit parallel, 8-bit parallel (GPIB), and RS-232-C serial. Compatibility is maintained with Gerber, Tektronix, and CalComp data formats. Microprocessor programmability permits acceptance of other plotter format structures. **Logic Systems,** 437A Aldo Ave, Santa Clara, CA 95050.
Circle 228 on Inquiry Card

HIGH RESOLUTION GRAPHICS CONTROLLER

A self-contained bus independent module, MMD-256 directly connects to std TV monitor and interfaces to any mini or microcomputer. The 4.5 x 6 x 0.5″ (11.4 x 15.2 x 1.3 cm) module is a complete 256 x 256 x 1 graphics subsystem that operates on std 5- and 12-V supplies and allows snow free access. X-Y addressing scheme allows the operator complete screen access, read or write, on a pixel by pixel basis. Multiple modules may be used to increase resolution to 256 vertical x 1024 horizontal or add color/gray scale capability by increasing bits/pixel. **Matrox Electronic Systems Ltd,** 5800 Andover Ave, Montreal, Quebec H4T 1H4, Canada.
Circle 229 on Inquiry Card

4-OUTPUT, 175-W SWITCHER

Replacement of extruded heat sinks with staggered heat-dissipating pins—Pin-Fins—improves performance of the Tiny-Mite[R] TM-34 open frame switcher. Turbulent flow for better heat transfer causes unit to be 19% cooler than previous models. The UL-478 recognized device, measuring 13 x 6.15 x 2.75″ (33 x 16 x 6.99-cm), mounts horizontally or vertically. Features include 70% efficiency (nom), 20-ms holdup time, and an input range of 92 to 130 Vac or 184 to 260 Vac, 47 to 450 Hz. **LH Research Inc,** 1821 Langley Ave, Irvine, CA 92714.



Circle 230 on Inquiry Card

MICROPROCESSOR BASED PRINTER/PLOTTER CONTROLLER

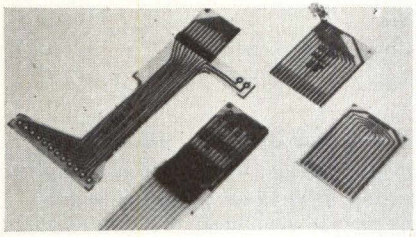
Graphware 1000 provides printer/plotter hardcopy graphic output via connection to a byte multiplexer channel, block multiplexer channel, or selector channel. The 3 field upgradable models are plug compatible with the IBM 360/370, 303X, or 4300 series. Model 50 receives raster data over the CPU's communication channel, emulating the IBM 2821 control unit/1403 printer combination. Model 51 can accept sorted vector data in addition to raster data; model 52 further accepts unsorted vectors. **Benson-Varian,** 385 Ravendale Dr, Mountain View, CA 94043.
Circle 231 on Inquiry Card

32k-BYTE BUBBLE MEMORY CARDS

FBC304D1A is comprised of four 74k-bit serial loop organized bubble memory devices. Avg access time is 370 ms, data rate is 100k bits/s, and power consumption is 5 W during operation and 2.5 W standby. The -2A consists of four 83k-bit major/minor loop organized devices and has avg access time of 4.5 ms, data rate of 50k bits/s, and power consumption of 4 W during operation and 2 W standby. **Fujitsu America, Inc, Component Sales Div,** 910 Sherwood Dr, Unit 23, Lake Bluff, IL 60044.

Circle 232 on Inquiry Card

PRINTER/PLOTTER DOT MATRIX THERMAL PRINTHEADS



Intended for medium speed alphanumeric tape and flying head printer/plotter applications, DL110/DLP110 printhead contains a single column of 10 std dots and 1 larger size plotting dot. DL110 std version is used for alphanumeric dot matrix char printing. In the DLP110, designed for plotting functions, the plot dot is factory connected in lieu of std dot and prints a trace of approx 0.020″ (0.508 mm) wide as compared to 0.015″ (0.381 mm) for std dots. It can be operated in dc mode for continuous traces, or in pulsed mode for dashed traces. **Gulton Industries Inc,** 212 Durham Ave, Metuchen, NJ 08840.

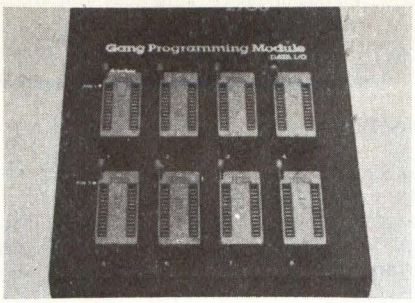
Circle 233 on Inquiry Card

DEC COMPATIBLE I/O BOARDS WITH DMA

Mounted on std DEC dual-height card with optional onboard DMA to add capability of high speed data transfers over the whole 256k bytes of memory through use of extended address bits, boards can be used in LSI-11, -11/2, and -11/23 (DMA only) systems. DT2782 has double-buffered A-D outputs to allow DMA transfer of previous data while a new conversion takes place, enabling operation at 35 kHz. System offers 12-bit resolution, 16 single-ended or 8 differential input channels. **Data Translation Inc,** 4 Strathmore Rd, Natick, MA 01760.

Circle 234 on Inquiry Card

GANG PROGRAMMING MODULE

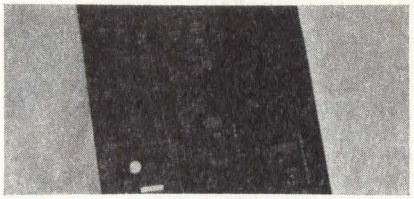


Gang programming module allows system 17 and system 19 P/ROM programmers to program from 1 to 8 n-channel EPROMs simultaneously. The module programs 2704, 2708, 2516, 2716-1 voltage, 2716-3 voltage, 2732, 2758, 2508, and 2532 24-pin devices by changing characterizers. Programmer automatically performs blank check and illegal bit checks, and can be used to reverify programmed devices after burn-in. **Data I/O Corp,** 1297 NW Mall, Issaquah, WA 98027.

Circle 235 on Inquiry Card

PRODUCTS

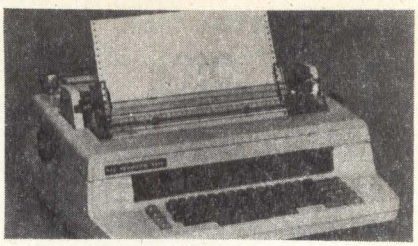
GENERIC PERSONALITY MODULE FOR BIPOLAR ICS



Designed to permit programming of all generic MMI PAL device types, the model PM9068 module provides the control lines and timing necessary to list, program, duplicate, and verify the devices using the Series 90 P/ROM programmer master control units. The module contains separate master and copy sockets, all of the PAL programming electronics, and configurators that automatically adapt the personality module to the correct PAL bit structure and device size. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 236 on Inquiry Card

KSR APL PRINTER TERMINAL



Model 5540 Spinwriter is a microprocessor controlled, serial impact terminal designed for remote printing applications requiring high quality. It prints up to 55 char/s while receiving data at rates to 120 char/s via an RS-232-C/CCITT V.24 interface. APL/ASCII print thimble contains 123 full u/lc alpha and numeric char and APL symbols, with last char visibility. Terminal is operator switch selectable or program selectable between APL and ASCII modes. **NEC Information Systems, Inc,** 5 Militia Dr, Lexington, MA 02173.

Circle 237 on Inquiry Card

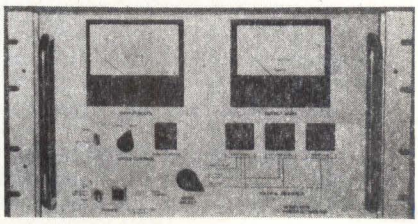
FLEXIBLE DISC SYSTEMS

Communications capabilities of the 500 series have been expanded with 4k of memory, simultaneous send/receive, and transmission file close. Using a std RS-232-C interface, the models can send or receive any type of data; 15 baud rates from 50 to 9600 can be selected by command from the terminal or remote computer. With the proper modem installed, options include unattended operation with auto answer, auto disconnect, and standby. **Trendata Corp,** 610 Palomar Ave, Sunnyvale, CA 94086.

Circle 238 on Inquiry Card

PROGRAMMABLE POWER CONVERTER

Programmable ac voltages can power systems, instruments, and machines under test for such uses as functional, reliability, and operational life testing. Model 2014 provides automatic cycling among 3 precision output voltage levels in the range of 100 to 129 Vac, 50/60 Hz, and will supply a load current of 25 A rms max. Front panel mounted thumbwheel switches select the output voltage level; duration of each level is selectable from 0 to 99 h. **YBI,** 3105 Harbor Blvd, Costa Mesa, CA 92626.



Circle 239 on Inquiry Card

MICROPROCESSOR BASED DISC CONTROLLER

Adding systems capability to Nova 3 CPUs, model 2603 provides intelligent control of storage modules. The microprocessor based disc controller relieves system overhead, improves throughput, and enhances I/O reliability. The controller is comprised of a formatter control PCB in a chassis with an independent power supply plus associated controls and indicators, an interface adapter PCB in the Nova CPU, 1 to 4 disc drives, and interconnection cables. **Mini-Computer Systems, Inc,** 2259 Via Burton, Anaheim, CA 92806.

Circle 240 on Inquiry Card

IEEE-488 INTERFACE BUS

IEEE-488/1975 interface bus plugs into any of the company's model 175 time code generators, translators, or generators, accepts data from the time code unit, and outputs data to the instrumentation bus in ASCII format. Interface uses own microprocessor for handshake and data transfer. Time updating capabilities are within one carrier cycle of serial time code being processed by time code unit (0.1 ms for IRIG A). Software control of interface functions allows addition of other functions without hardware redesign. **Moxon, Inc,** 2222 Michelson Dr, Irvine, CA 92715.

Circle 241 on Inquiry Card

HIGH BRIGHTNESS T-1 LED LAMPS

High brightness red, yellow, and green units in both long and short dome mechanical designs added to the OPL series use high efficiency electroluminescence of gallium phosphide material. Both wide angle and high intensity lamps are offered. Typ viewing angles at half intensity points are 150° and high intensity indicators have viewing angles of 80°. Typ luminous intensity varies from 1 to 4 mcd. **OPCOA,** 330 Talmadge Rd, Edison, NJ 08817.

Circle 242 on Inquiry Card

PANEL MOUNT LED INDICATOR LIGHT

The 2L7 utilizes a T-1¾ Hi-Bright LED available in red, green, or amber, with a large lens that permits 180° visibility and up to 50 mcd. The lens also incorporates Fresnel rings and flutes for max distribution of light output. Lenses are available in transparent or translucent material. The body is all-metal threaded; Wire Wrap® posts or wire leads are used for termination. Operating voltage is up to 48 V, with a built-in resistor. **The Sloan Co,** 7704 San Fernando Rd, Sun Valley, CA 91352.

Circle 243 on Inquiry Card

16-BIT, ±1-MIN S-D TRACKING CONVERTER

Holding ±1 arc min of accuracy over the full temp range and fitting into the same space as 14-bit converters, the 16-bit model 1661B produces a jitter free stable output. It is transformer isolated, exhibits no 180° hang-up, and offers a separate logic ground to minimize ground loop problems. A ratiometric conversion process makes the converter insensitive to voltage and frequency variations. The model interfaces with any std synchro or resolver. **Transmagnetics, Inc,** 210 Adams Blvd, Farmingdale, NY 11735.

Circle 244 on Inquiry Card

BCD TO SERIAL ASCII DATA CONVERTER

Redesigned and upgraded ASCII Bustle includes microprocessor circuitry. Pluggable unit transforms parallel BCD to serial ASCII for remote data logging applications. Features include switch selectable rates from 110 to 9600 baud, 2-digit selectable identification number, 32-char special message in nonvolatile memory, parity switch for selection of even, odd, mark, space, or no parity, and jumper selection for number of stop bits. **Nationwide Electronic Systems, Inc,** 1536 Brandy Pkwy, Streamwood, IL 60103.

Circle 245 on Inquiry Card

SYNCHRO TO BCD AND BINARY ANGLE TRACKING CONVERTERS

Type II tracking converters continuously and monotonically translate input synchro angle to binary and BCD output angles. Both 3- and 4-digit models in the SD580 series are available in commercial and military temp ranges. The -359 provides 10-bit binary angle output and 10-line BCD output with a full scale of 359°. The -359.9 provides 14-bit binary angle output and 14-line BCD output with a full scale of 359.9°. **Interface Engineering Inc,** 386 Lindelof Ave, Stoughton, MA 02072.

Circle 246 on Inquiry Card

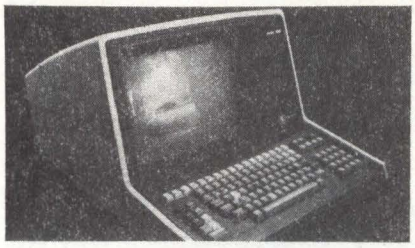
EIA ADAPTER FOR SHARING PRINTERS

MSA-4 is a unidirectional multiplexed serial data device which is code and transmission rate transparent and has equal priority for all input channels. The unit interfaces 4 computer or CRT terminals to 1 printer with an option to expand from 4 to 16 channels. All channels contend for control of the device, and all channels except for the one in control are held off with a control signal. A power supply is included. **Via West, Inc,** 2739 W Palm Ln, Phoenix, AZ 85009.

Circle 247 on Inquiry Card

PRODUCTS

COLOR DISPLAY TERMINALS



Available in configurations ranging from terminals to desktop computers, the 3600 and 8300 CRT terminals feature 13″ (33-cm) screens, molded cabinets with built-in keyboards, and 8-color displays. Both series will support high level programming languages including Business BASIC and FORTRAN. Options include a hard disc or built-in floppy disc for the 3600; graphics capabilities, light pens, and asynchronous/synchronous communications for both. **Intelligent Systems Corp,** 5965 Peachtree Corners E, Norcross, GA 30071.

Circle 248 on Inquiry Card

ACOUSTIC COUPLER/MODEM

TC3001, a Bell compatible 103/113 unit, transfers low speed data over normal voice grade telephone lines at an asynchronous data rate of 300 baud using an ordinary telephone handset. The originate only device features half/full-duplex operation, power and carrier indicators, and acoustic and DAA/private line interfaces, as well as simultaneous EIA RS-232 and 20-mA interfaces. Dimensions are 10.5 x 7.5 x 3.75″ (27 x 19 x 9.5 cm). Sensitivity is −50 dBm. **Tek-Com,** 1147 Sonora Ct, Sunnyvale, CA 94086.

Circle 249 on Inquiry Card

HOBBY LEVEL DIGITAL TAPE CASSETTE

Micro-Comp cassette uses the same magnetic tape as is used in professional units, and is 100% bulk certified at 1600 fc/in (629/cm). The unit features 50′ (15 m) of instant play computer quality tape. Physical features include acetal hubs, graphite impregnated polyolefin washers, precision machined stainless steel pins, and a large pressure pad. Intrinsic coercity is 315, residual flux 1350 gauss, and erasing field is 1000 Oe. **Magnetic Information Systems Inc,** 415 Howe Ave, Shelton, CT 06484.

Circle 250 on Inquiry Card

ADD-IN MEMORY MODULES

Doubled memory density and single 5-V operation highlight 2 modules. TMM-A50 is a general purpose, RAM module on a double-sided PC board that is customized with backplanes, controllers, and power supplies. TMM-11L is a dual-height add-in RAM, either 32k or 64k, for the DEC LSI-11/2 and /23 computers. Addressing for the -11L can be extended up to 1M bytes. Its max power dissipation is 10.5 W active and 7.9 W standby. Specs include 200-ns max read access time and 150-ns max write access time. **Texas Instruments Inc,** PO Box 1443, Houston, TX 77001.

Circle 251 on Inquiry Card

DISC DRIVER FOR PDP-11 SYSTEMS

Overlap seek disc driver increases throughput in DEC RSX-11M operating system by processing concurrent requests in parallel. Performing concurrent (overlapped) seeks, disc driver uses search command to reduce controller busy time (RM and RP drives) and supports dual porting. A compatible replacement for standard DEC drivers, OSDD software is distributed as resident or loadable source code and may be used with most DEC disc products. **Cytrol,** 4570 W 77th St, Erdina, MN 55435.

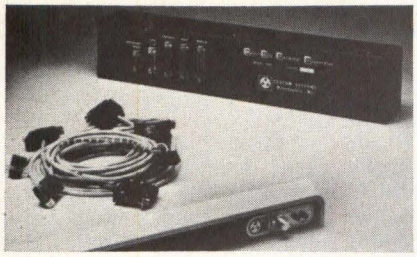
Circle 252 on Inquiry Card

OPEN FRAME DC POWER SUPPLY

Outputting 5 Vdc at 3 A, model B5-3/OVP provides ±0.03% line or load regulation and <3-mV ripple pk-pk. Short circuit and overcurrent protection are supplied by current limit/foldback, and overvoltage protection is built in at 6.4 ±0.4 Vdc. Unit requires 115/230-Vac ±10% input at 47 to 440 Hz. Other features include remote sensing, open lead protection, remote programming, and remote voltage adjust capability. **Condor, Inc,** 4811 Calle Alto, Camarillo, CA 93010.

Circle 253 on Inquiry Card

COMMUNICATIONS SWITCHING DEVICE

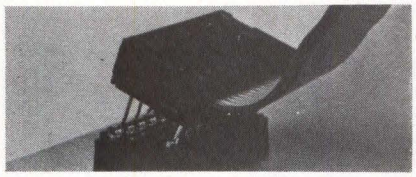


MUTT, a multi-use terminal translator, is a switch-controlled data phone access and control system. The device comprises two subassemblies. A 5 x 19″ (13 x 48-cm) panel mounts on the rear of the computer cabinet, houses all required operational logic and switching components, and terminates the systems console cable and the interface cable from an asynchronous modem. An operator switch assembly mounts on the face of the computer cabinet. **Custom Systems, Inc,** 2415 Annapolis Ln, Minneapolis, MN 55441.
Circle 254 on Inquiry Card

16-BIT A-D CONVERTERS

ZAD7200 and 7400 provide true 16-bit accuracy at conversion speeds of 20 and 10 μs, respectively. Other performance specs include no missing codes over the 0 to 70 °C op temp range, 0.4-ppm/°C differential linearity tempco, ±0.0015% accuracies, and 6-sided emi/rfi shielding. A monobit ladder network overcomes problems of binary weighted ladder networks. An error correction, feed forward conversion algorithm bypasses speed limitations of successive approximation conversion techniques. **Zeltex, Inc,** 940 Detroit Ave, Concord, CA 94518.
Circle 255 on Inquiry Card

DIP CONNECTOR

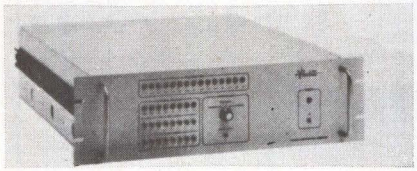


Dual inline package can be used as solderless connector for IC sockets that accept 0.015″ (0.038-cm) max thick pins or can be wave soldered direct to PC board. 6700 series connectors allow high density packaging, and as interboard busing jumpers reduce PC board area and need for multilayer circuit boards. Low profile permits high density rack mounting. Available in circuit sizes 8, 14, and 16, the devices avoid bend in cable by terminating to either side. **Molex Inc,** 2222 Wellington Ct, Lisle, IL 60532.
Circle 256 on Inquiry Card

160-CHAR/S MATRIX PRINTER

Model 9612, equipped with a serial interface, functions as the system printer of the 1500 Dispersed Processor or as a local or remote terminal printer for any Datashare Business Timesharing system. Model 9622 parallel interface version attaches directly to the I/O bus of any other company processor to serve as a system printer. A microprocessor and buffer memory allow the 9 x 9 dot matrix printer to achieve print throughputs as high as 500 lines/min through use of bidirectional printing and rapid printhead slewing. **Datapoint Corp,** 9725 Datapoint Dr, San Antonio, TX 78284.
Circle 257 on Inquiry Card

2000-CHANNEL MULTIPLEXER SYSTEM



Model 3000 consists of a multiplexer, programmable gain amplifier, S/H amplifier, and an ADC, functioning in the range of ±5 mV to ±10.240 V full scale. The system accepts differential or single-ended signals, or both. It expands to over 2000 channels in 8-channel increments. Features are open circuit detection, automatic gain ranging, and automatic calibration supply, which can be removed for calibration against an NBS certified std. **Tustin Electronics Co,** 1431 E St Andrews Pl, Santa Ana, CA 92705.
Circle 258 on Inquiry Card

COMPUTER TO CONTROL DEVICE INTERFACE

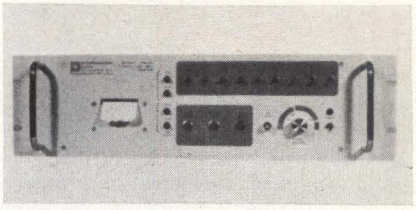
Remote control device (RDC) system is hardware interface between one standard computer and up to 1000 on/off devices located to a maximum of 2000′ (610 m). Full-duplex serial output from computer connects to RDC model 145-11 and is converted to 12 Vdc simplex for a 2-wire line. Line connects to up to 125 receivers each of which can handle 1 to 8 on/off devices. ASCII-like 11-bit line format uses bit 9 as address or command identifier. 110- to 4800-baud line speeds are available. Remote devices are operated by spdt relay which applies 115 Vac at 2 A max to device. **Remote Station Controls,** 217 Minnetonka Ave, Wayzata, MN 55391.
Circle 259 on Inquiry Card

PRODUCTS

VIDEO DISPLAY INTERFACE FOR PDP-11

VIURAM VRU-11, a single quad-height card, directly interfaces any UNIBUS® type computer with a CRT monitor. It allows direct access to all char positions in displayed or nondisplayed portions of video memory; up to 8192 char may be stored. Dynamic, software controlled format is limited only by monitor capability. The unit produces arrays of up to 256 x 256 pixels. A lightpen may operate in polled or interrupt driven mode, and a serial I/O port operates from 110 to 38.4k baud. **Computer Technology,** 3014 Lakeshore Ave, Oakland, CA 94610.
Circle 260 on Inquiry Card

DATA TEST SET PRINTER

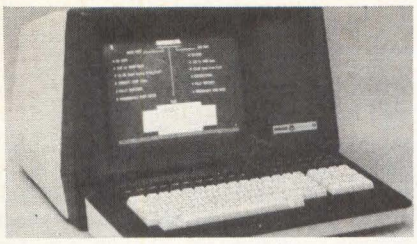


Designed to operate with the company's 3000D synchronous data transmission test set to provide a hardcopy record of V.24 (RS-232), V.35, Bell 301/303, RS-422, or MIL-188 data interface test results, the 2900D records errored seconds, total seconds, errored bits, and total bits tallied by 4 event counters in the test set. Presettable 24-h realtime clock is incorporated and time in hours and minutes is recorded with each printout. Event counters can be initiated to print out at preselected time intervals. **International Data Sciences, Inc,** 7 Wellington Rd, Lincoln, RI 02865.
Circle 261 on Inquiry Card

P/ROM PROGRAMMERS

Z80 microprocessor controlled universal programmers handle different P/ROMs through interchangeable personality modules. MPP 80-E (engineering), S (service), and P (production) models have a 32k-bit internal RAM. The microprocessor interacting with software in each module provides all programming signals. Data are transferred to the RAM through an RS-232-C interface. E and S models have hexadecimal keyboards, and the latter also has a built-in UV eraser function. **Kontron Electronic, Inc,** 700 S Claremont St, San Mateo, CA 94402.
Circle 262 on Inquiry Card

CRT DISPLAY TERMINAL



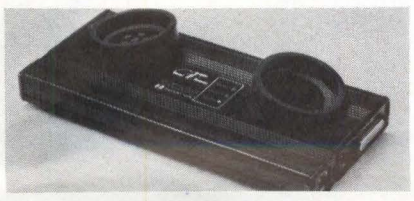
Featuring a detachable keyboard case, model DM30 provides for 2 pages of display memory, with editing, formatting, and scrolling and paging controls. The screen presents 24 lines x 80 char with a 25th line used for status—mode prompts, error messages, and a realtime clock. Serial asynchronous RS-232-C main and auxiliary ports have baud rates selectable up to 19.2k. An internal protocol passes data between ports at differing speeds. **Beehive International,** 4910 Amelia Earhart Dr, Salt Lake City, UT 84125.
Circle 263 on Inquiry Card

RS-232 INTERFACE CONVERTERS

IFA series MRA-25-2 provide convenient adapters to convert RS-232/V.24 electrical interface to either CCITT recommended RS-449, V.35, X.21, or Bell 303. Design allows the same converter to fit either std 19″ (48-cm) rackmount or desktop enclosure. All converters are interchangeable and different units may be installed in the same rack. All operate on either 115 or 220 V, 50/60 Hz. RS-232 connector may be replaced with a TTL interface. **Atlantic Research Corp,** 5390 Cherokee Ave, Alexandria, VA 22314.
Circle 264 on Inquiry Card

300-BAUD ANSWER/ORIGINATE ACOUSTIC COUPLER

Cat™ is a 0- to 30-char/s Bell 103 compatible compact acoustic modem that operates half or full duplex in answer, originate, and test modes. Interface is RS-232-C, and power and carrier (ready) indicators are provided. Receiver sensitivity is −45 dBm. Powerpack (115 Vac, 2.5 W max) plugs directly into wall sockets, isolating modem from dangerous voltages. Unit height is 2.3″ (5.8 cm), and weight is 1.5 lb (0.68 kg). **Novation, Inc,** 18664 Oxnard St, Tarzana, CA 91356.

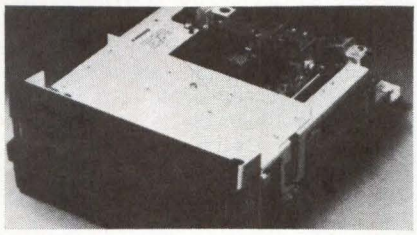


Circle 265 on Inquiry Card

MULTITASKING COMPUTER SYSTEM

Information Manager operating system supports up to 48 terminals online. Main memory is expandable from 32k to 1M bytes; 32M-bytes disc storage is expandable to 1.2G bytes. Basic system configuration includes FAST operating system, model 1602 CPU with 64k-bytes memory, 32M-byte cartridge disc drive with 16M-byte fixed and 16M-byte removable discs, letter quality 55-char/s printer, and 1 microprocessor video display terminal with 16k-bytes memory. **Cybertek Computer Products, Inc,** 6133 Bristol Parkway, Culver City, CA 90230.
Circle 266 on Inquiry Card

DOUBLE-SIDED, DOUBLE DENSITY 8″ FLOPPY DRIVES



With either dc brushless or ac motors, 700 series drives provide 10k-h MTBF and head life exceeding 4 x 10^7 wear revolutions in 8 models with either ac (115 and 220 V, 49 W PAVE) or dc (24 V, 26 W PAVE) spindle drives. Double-sided units offer double-density (1.6M bytes) or single-density (800k bytes); single-sided 500 series offers single-density (400k bytes). Compatible with IBM, ANSI, and all other industry stds, the units have soft read errors of $<1 \times 10^9$ bits; hard errors of $<1 \times 10^{12}$ bits. **MFE Corp, Digital Products Group,** Keewaydin Dr, Salem, NH 03079.
Circle 267 on Inquiry Card

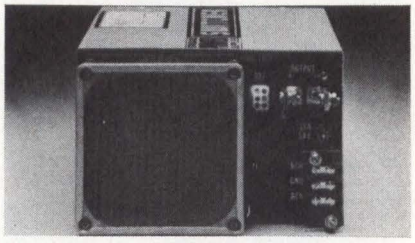
1M-BYTE RAM BOARD

Based on 128k-bit hybrid memory modules, Hypak packages 1M bytes of high speed dynamic RAM with 6-bit error correction on a single 13 x 15″ (33 x 38-cm) board. Access times are 200 ns. The units operate with GA-16/460 and /550 minicomputers. Each module contains 8 commercially available 16k dice, mounted on a ceramic substrate. Miniature multilayer thick film circuits provide pin to die interconnects, and high precision automated bonding makes die to substrate connections. **General Automation,** 1055 S East St, Anaheim, CA 92803.
Circle 268 on Inquiry Card

PRODUCTS

HI-REL SWITCHING POWER SUPPLIES

Industrial/commercial regulated dc supplies offer continuous operation, 230-Vac, single-phase input, built-in fan, and up to 80% efficiency with low energy requirements. Rated at 750 W, 5 models of SWS 751 line provide 5, 12, 15, 24, and 28 Vdc from 28 to 150 A. Soft-start circuitry extends MTBF; overtemp protection, overvoltage protection, and full load burn-in improve reliability. Performance features include low emi/rfi, paralleling capability, and brownout capability. **Standard Power Inc,** 1400 S Village Way, Santa Ana, CA 92705.



Circle 269 on Inquiry Card

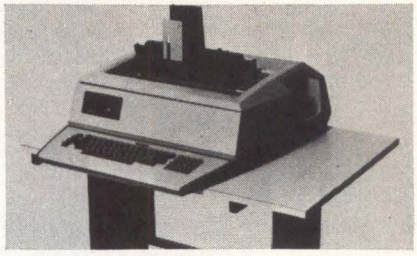
FIBER OPTIC SYSTEM TEST METER

FPM-1 measures basic electro-optical parameters to establish and maximize fiber optic link performance. Avg optical power from 20 nW to 2 mW, over the wavelength region 500 to 1000 nm, and current from 2 nA to 200 μA can be measured. Optical power and current measurements are made with accuracies of ±5% and ±0.5%, respectively. Readout is via a 3½-digit LCD. Sensing head features interchangeable connectors; 2 single-fiber adapters accept fibers with dia to 1 mm. **Radiation Devices Co, Inc,** PO Box 8450, Baltimore, MD 21234.

Circle 270 on Inquiry Card

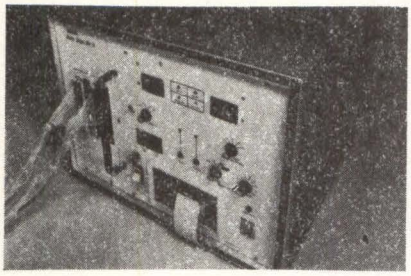
AUTOMATIC FRONT FEED PRINTER

Formatting and printing of individual cut forms is obtained from the front feed option to the T-1612 printer terminal. Attachment does not affect normal operation for printing continuous fanfold forms; ability to handle 2 forms simultaneously enables the user to have a trailing ledger journal of printing transactions. Cut form is inserted into 2 transport rollers and front feed unit moves it to the proper page position. Unit is program controlled from a microprocessor in the printer. **Tally Corp,** 8301 S 180th St, Kent, WA 98031.



Circle 271 on Inquiry Card

CABLE TEST SYSTEM

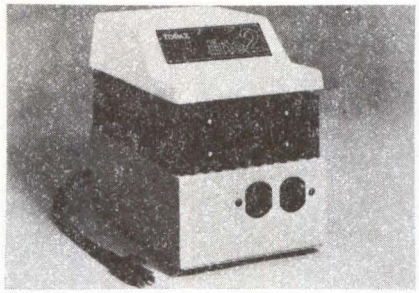


Faults such as shorts, opens, or miswires are detected by the AutoScan HiV which simultaneously locates these faults by source and destination points. To operate the system, each end of the cable to be tested is connected to the adapter cables on the test system; the operator then sets the test limit, and indicates test voltage, dwell time, and continuity and insulation resistance limits. A high speed printer provides a record of each defect on paper tape in a 5-digit code. **Muirhead Addison,** 1101 Bristol Rd, Mountainside, NJ 07092.

Circle 272 on Inquiry Card

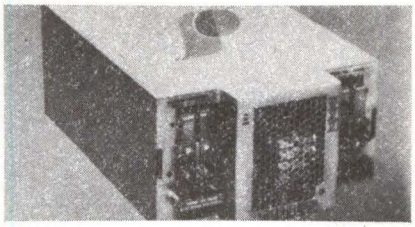
SMALL COMPUTER POWER CONDITIONERS

Single-phase Line 2 conditioners for minicomputers having mainframe capability operate at 50 and 60 Hz and are available in power ratings of 5, 7.5, and 10 kVA. They offer 94% efficiency. A tap selectable input capability of 208, 220, or 240 V is offered while consistently regulating output voltages to a narrow ±7% of nom. Transient noise and brownout protection are provided with superior dynamic regulation and negligible harmonic distortion. **Topaz Electronics,** 3855 Ruffin Rd, San Diego, CA 92123.



Circle 273 on Inquiry Card

3-CHANNEL SWITCHING POWER SUPPLIES



Two high power output channels of the model PM2809 provide voltage selections of 2, 3, 5, 12, 15, 18, 21, 24, 28, and 48 Vdc and a third channel produces 2, 3, 5, 12, and 15 Vdc. Max total output power is 800 W, including 400 W max on the main channel and 400 W max on the second channel less third channel power which may be up to 10 A at 15 V. Supplies have single-phase 47- to 63-Hz ac inputs ranging from 184 to 260 Vac. **Pioneer Magnetics,** 1745 Berkeley St, Santa Monica, CA 90404.

Circle 274 on Inquiry Card

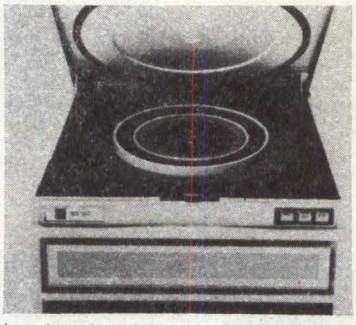
PRODUCTS

17.3M-BYTE CARTRIDGE TRANSPORT

Tape cartridge transport model 640 uses 6400-bit/in (2519/cm) recording density to give max unformatted storage capacity of 17.3M bytes, adapting it to use as backup for 8" (20-cm) hard discs. The unit has 4-track read-after-write heads and uses 3M type DC300 cartridges. Data transfer rate is 192 kHz using a MFM recording mode. With 300' (91.5-m) tape lengths, max unformatted storage is 11.5M bytes; 450' (137-m) tapes give 17.3M bytes. To reduce rewind time, the transport uses a serpentine technique in which adjacent tracks are recorded in opposite directions. Recording speed is 30 in(76 cm)/s, while rewind and search occur at 90 in (228 cm)/s. Displacement is 0.375" and 3.38" (0.952 and 8.58 cm) at 30 and 90 in (76 and 228 cm)/s, respectively. Instantaneous speed variation is only ±3% with a long term variation of ±2%. **Kennedy Co,** 540 W Woodbury Rd, Altadena, CA 91001.

Circle 275 on Inquiry Card

100M-BYTE DISC DRIVE



Rack mountable 10.5" (26.7 cm) high self-contained random access mass storage unit storing more than 100M bytes on a removable disc pack, BD-100 has 5 read/write surfaces, each carrying 1024 tracks, and storing a total of 103.22×10^6 bytes. Each track carries 20k bytes or 161k bits (including header and gaps). Track density is 465 tracks/in (183)/cm). Recording method is MFM, bit serial. A closed loop head positioner servo system receives positioning information from tracks prerecorded on one dedicated disc surface, providing reliable positioning without external references. Max access time averages 30 ms; between two adjacent tracks, 5 ms; and across max tracks (0 to 1024), 55 ms. Latency time average is 8.3 ms and max is 16.7 ms. Data transfer rate is 9.68×10^6 bits/s at a std rotational speed of 3600 r/min. Start and stop times are 20 s. **Ball Computer Products,** 860 E Arques Ave, Sunnyvale, CA 94086.

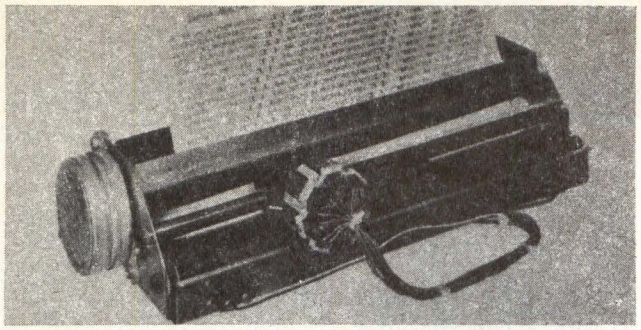
Circle 276 on Inquiry Card

DATA ACQUISITION SYSTEM FOR MINICOMPUTERS

PDAS-250 uses an overlapped conversion method to offer throughput of 250k samples/s. A-D data acquisition system is compatible with most minicomputers and high speed 16-bit microcomputers. The unit combines 12-bit binary A-D/D-A resolution; 250-kHz throughput, and channel density or 256 A-D channels/housing. A front panel binary controller with data and channel LED indicators and toggle switches allows local manual access to the system. Up to 256 single-ended or 128 differential A-D channels are available coresident with up to 32 D-A channels. Simultaneous sample/hold option allows up to 64 analog A-D channels to be sampled at precisely the same time (±1 ns) and then rapidly digitized and transmitted to computer memory. **Datel Systems, Inc,** 1020 Turnpike St, Canton, MA 02021.

Circle 277 on Inquiry Card

80-COL DOT MATRIX IMPACT PRINTER MECHANISM

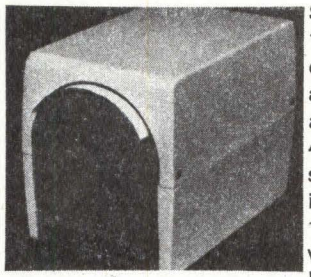


Printing bidirectionally at 80-char/s using a 7-pin dot matrix, the printhead of the model 100600 is capable of continuous duty and has a service life of 100M char. Measuring 2.5 x 5 x 12" (6.35 x 12.7 x 30.5 cm), the printer uses a stationary ribbon cartridge containing a 0.5" (1.27 cm) wide ribbon on a 1° bias and having a life of 10M char. Paper may be loaded from the rear or from directly underneath. A graphics option enables the user to space paper vertically in any desired increments as well as to slew paper at the rate of 10 lines/s. Tractor feed is available for continuous form applications. **Two-Day Corp,** 619 Fairmount Rd, Burbank, CA 91601.
Circle 278 on Inquiry Card

WINCHESTER TYPE DISC STORAGE SUBSYSTEMS

Models 6102, designed for use on microNova systems, and 6099, for use on Nova and Eclipse computers, feature Winchester type technology and microprocessor controlled seek mechanism. Nonremovable disc in the subsystem stores 12.5M bytes of data. Disc read/write head seek actuator is stepper motor driven, but controlled by a microprocessor that executes a velocity determination algorithm to optimize positioner acceleration/deceleration. Track to track seek requires 15 ms and average random seek is 60 ms. Subsystem has a self-contained power supply. Main ac power provided can be 120 V/60 Hz, 100 V/50 Hz, or 220 V/50 Hz. The unit is compactly packaged to use only 10.5" (26.7 cm) of vertical rack space. **Data General Corp,** Rt 9, Westboro, MA 01581.
Circle 279 on Inquiry Card

ROTARY PRINTERS



Series 1800 provides std 8.5 x 11 or 14" (21.5 x 27.9 or 35.5 cm) printout. Model 1800 is an alphanumeric printer with operator selectable speeds of either 4000 or 6600 char/s. RS-232-C serial and industry std parallel interfaces are available. Model 1870 uses an RS-170 composite video interface for reproducing high resolution graphics and/or alphanumerics. Graphic resolution exceeds 200 dots/in (78.7/cm) horizontal and 100 dots/in (39.3/cm) vertical. With an aspect ratio of 1.6 to 1, the unit reproduces a CRT screen in 5 s. Reproduced image is 4.85 x 7.74" (12.32 x 19.66 cm) on an 8.5 x 11" (21.6 x 27.9-cm) hardcopy. Both interlaced and noninterlaced sources can be interfaced to the unit by switch selection under operator control. **SCI Systems, Inc,** 8600 S Memorial Pkwy, Huntsville, AL 35802.
Circle 280 on Inquiry Card

PRODUCTS

HANDHELD DATA COMMUNICATIONS INPUT DEVICE

Pocket terminal can be carried in a tool kit or pocket and plugged into a digital system anywhere to input and read data. Housed in a 6 x 3" (15 x 8 cm) case, the terminal has 40 positive response keys, allowing 128 ASCII codes to be selected and transmitted as 8-bit words with parities and start/stop bits. Data received are held in the 30-char memory for access in 8-char blocks on the LEDs which display a 64-char uc alphanumeric and symbol set. A controllable cursor function permits data entry in a variety of formats as well as editing of information in a host processor's memory. The unit is supplied with a 25-way connector and RS-232-C interface compatibility. A single 5-V power supply is needed at 450 mA max. **GR Electronics Ltd,** 1640 Fifth St, Santa Monica, CA 90401.

Circle 281 on Inquiry Card

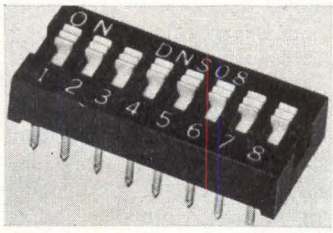
USER PROGRAMMABLE INTELLIGENT TERMINAL

Multi-Disc MDT-405 offers up to 2M bytes of mass storage on dual-density floppy diskettes. A self-contained processing system with up to 48k bytes of internal memory, CRT, keyboard, 2 dual-density floppy discs (expandable to 4), and dual serial interfaces for communications and printer, the terminal is based on an 8085 microprocessor capable of handling complex processing activities. Three additional microprocessors handle display, disc controller, and serial ports in a bus oriented DMA environment. High resolution CRT is fully scrollable through a 2560-char buffer containing 32 lines of 80 char each. 122-key keyboard allows complex file management and screen editing through single keystrokes, and features 18 user defined keys that can store fixed and variable data. **Compugraphic Corp,** 80 Industrial Way, Wilmington, MA 01887.

Circle 282 on Inquiry Card

PC BOARD DIP SWITCHES

Designed as minisized components to mount directly to a PC board with semiconductor devices, ICs, and other components, series DNS 4-, 6-, or 8-pole switches can be handled in precisely the same manner as an IC. Terminals



are easily inserted into holes of a PC board because the dual pin alignment is similar to both IC and LSI paokages. Program modification can be made by just touching, without troublesome rewiring. Multiple circuit function can be realized by adapting the DIP switches on a PC board. Terminals are sealed from soldering and flux contamination. Original contact resistance is maintained after 10k switching operations. Ratings are 50 Vdc, 100 mA without switching; 5 Vdc, 100 mA and 25 Vdc, 25 mA with switching. Contact resistance is <50 mΩ at 2 Vdc, 10 mA. **Guardian Electric Manufacturing Co,** 1550 W Carroll Ave, Chicago, IL 60607.

Circle 283 on Inquiry Card

VT-52 COMPATIBLE COMPUTER TERMINAL

Model 1552, an enhanced conversational terminal, offers total software capability to DEC VT-52 applications and has a similar keyboard layout. Separate cursor control keys, graphics mode, function keys, hold screen mode, and an alternate keypad mode operation that transforms the numeric keypad into a function key cluster are among the unit's features. Also provided are key functions, programmable key switch audio feedback, keyboard lock and unlock, field tab, and insert and delete line that are not on the VT-52. Incorporating EIA and 20-mA current loop interface, 8 selectable transmission rates, auxiliary EIA output, remote editing commands, and std or reverse video, unit has 94 displayable 7 x 10 dot matrix char and dual density display. **Hazeltine Corp, Computer Terminal Equipment,** Greenlawn, NY 11740.

Circle 284 on Inquiry Card

HIGH SPEED 1k X 16-BIT CACHE MEMORY

PM-KK11A, a high speed RAM cache, features 1k x 16-bit capacity and is designed to run with the PDP-11/34A central processor. Configured on a hex wide circuit board which resides next to the CPU, the memory simulates a system having large amounts of moderately fast memory, and substantially decreases avg access time. A direct replacement for DEC's KK11A, the unit captures data from the Unibus during CPU to main memory transfers. This allows the cache to hold words most often required by the program. Typically the cache will have required data 85% of the time, saving approximately 325 ns each time it is read. Write-through prevents data loss with nonvolatile main memory during power failure. **Plessey Peripheral Systems,** 17466 Daimler Ave, Irvine, CA 92714.

Circle 285 on Inquiry Card

MINIATURE SERIAL MATRIX PRINTER

Program controlled font selection, 200M-char head warranty, and microprocessor controlled interfaces are features of the Microline 80. Unit weighs 14 lb (6.3 kg) and measures 4 x 13.4 x 9.4″ (10 x 34 x 23.9 cm). The printer will operate continuously at 80 char/s with no duty cycle limitations, producing 9 x 7 u/lc char across an 80-col page. It also prints condensed char at 16.5 char/in (6.5/cm), accommodating 132-col formats. Line spacing at 6 or 8 lines/in (2.3 or 3.1/cm), char spacing, and font selection are under program control. The unit's low mass head is a fraction of the size of conventional 7-pin heads, consumes less power, generates less heat, and produces sharp char on 1-, 2-, or 3-part forms. **Okidata Corp,** 111 Gaither Dr, Mount Laurel, NJ 08054.

Circle 286 on Inquiry Card

PRODUCTS

SEMICONDUCTOR LASERS FOR LONG DISTANCE OPTICAL FIBER COMMUNICATIONS SYSTEMS

Permitting transmission of data at 1G-bit/s rates, over distances of more than 50 km, without need for repeaters, HLP 5000 series laser diodes have a wavelength of 1.3 μm that provides minimum transmission loss in optical fiber cables used in long distance, high capacity optical transmission systems. Diodes are produced using a crystal growing and processing technology based on InGaAsP (indium gallium arsenide phosphide). Crystals use a special buried heterostructure. Oscillation mode is stabilized, a 60-mA threshold current activates the laser, and linearity of light current characteristics is superior. Optical power output of 5 mW in fundamental transverse mode is available with distortion of less than −50 dB. Rise and fall times of optical output power are both below 0.5 ns, enabling high speed modulation at about 2 GHz. **Hitachi America Ltd,** 707 W Algonquin Rd, Arlington, Heights, IL 60005.

Circle 287 on Inquiry Card

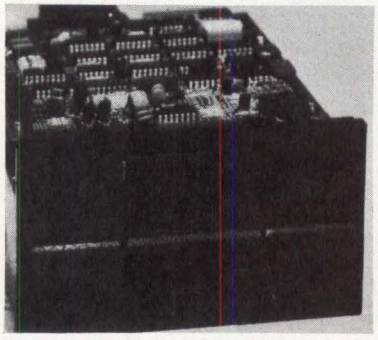
FIXED DISC STORAGE UNITS

Certainty 230 series mini-module disc storage units offer 37.9M or 50.5M bytes of formatted data storage. Each unit consists of fixed media disc drive, single-board LSI controller, diagnostics, and interconnections necessary for use with IBM Series/1. Specs for the units include an avg data access time of 30 ms and a data transfer rate of 1.2M bytes/s. Systems are fully compatible with 270 series removable storage module drives. Each model also can be configured with an optional flexible disc drive that contains up to 606k bytes of data. This combined fixed and flexible disc offering is designated the Certainty 240 series. **Control Data Corp,** PO Box O, Minneapolis, MN 55440.

Circle 288 on Inquiry Card

DOUBLE-SIDED, DOUBLE-DENSITY 5″ DISC DRIVE

A double-sided, double-density floppy disc drive, the Data-Trak™ 5 uses a proprietary head assembly design to attain a media life of >3 x 10^6 passes/track. Unformatted data storage capacity is 437.5k bytes and formatted capacity is 286.7k bytes. Recording density is 5456 bits/in (2148/cm) and transfer rate is 250k bits/s. Track to track access time for the unit's 70 tracks is 20 ms, settling time is 15 ms, and avg access time is 241 ms. Head loading, which is independent of media loading, is accomplished in 50 ms. Std features of the transport include an LED activity indicator and a door closure lockout that ensures that the drive door cannot be closed if the disc is not properly inserted. Operation is either 12 or 5 Vdc, with power dissipation of 12 W in continuous operation. **Qume Corp,** 2350 Qume Dr, San Jose, CA 95150.



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LITERATURE

Precision Measurement And Control

Specs for std data conversion and signal conditioning products, computational circuits, and measurement and control systems and subsystems are presented in 40-p short form guide. **Analog Devices,** Norwood, Mass.
Circle 300 on Inquiry Card

Multiuser Operating System For Microcomputers

5-p brochure summarizes PANA/BASIC software system for microcomputers and describes special features, performance capabilities, and language functions and statements. **Panatec Inc,** Orange, Calif.
Circle 301 on Inquiry Card

Electronic and Electromechanical Relays

Dimensional photos, specs, mounting, and cross reference charts supplied in guide cover PC mounting, general purpose, power latch, and time delay relays. **Omron Electronics, Inc,** Schaumburg, Ill.
Circle 302 on Inquiry Card

Multiple Output dc Power Supply

Booklet discloses mechanical design features, discusses safety and emi standards, and gives performance curves, block diagrams, and condensed std specs for power supply models. **Hewlett-Packard Co,** Palo Alto, Calif.
Circle 303 on Inquiry Card

Terminal Boards

Manual supplies dimensional drawings, applications and materials information, specs, and UL and CSA data for std boards, stud and turret, wirewrap, and military components. **Kulka Electric Corp,** Mt Vernon, NY.
Circle 304 on Inquiry Card

Precision Connectors and Assemblies

Specifiers' guide lists specs and photos for miniature rack and panel connectors including 4- to 24-contact screwlock, edgeboard, 2-piece PC, high density, and miniature hexagonal connectors. **U.S. Components, Inc,** Bohemia, NY.
Circle 305 on Inquiry Card

OEM Services

Brochure illustrates how company supports OEMs in gaining maximum market share profitability. **Data General Corp,** Westboro, Mass.
Circle 306 on Inquiry Card

Mass Storage Equipment

Range of magnetic tape drives and formatters are outlined in brochure with descriptions and specs. **Perkin-Elmer, Memory Products Div,** Garden Grove, Calif.
Circle 307 on Inquiry Card

Direct Drive Switching Power Supply

Data sheet cites features, specs, and mechanical drawing of 200-W SK5-40/OVP switcher. **Power-One Inc,** Camarillo, Calif.
Circle 308 on Inquiry Card

Synchronous Multiplexer

Data sheet provides description of features and options, applications, and equipment diagrams for 604 bit interleaved time division multiplexer. **Codex Corp,** Mansfield, Mass.
Circle 309 on Inquiry Card

Miniature, Subminiature, And Microminiature Lamps

Data provided in catalog include dimensional drawings, voltage and current ratings, brightness values, filament shape, and average lamp life. **Chicago Miniature Lamp Works,** Chicago, Ill.
Circle 310 on Inquiry Card

Data Communication

Catalog describes features of 300- to 19.2k-bit/s time and frequency division statistical multiplexers, data line concentrators, and network diagnostic control systems. **General DataComm Industries, Inc,** Danbury, Conn.
Circle 311 on Inquiry Card

Forced Air Convection Coolers

Catalog furnishes charts of thermal and airflow characteristics, dimensional drawings, mounting configurations, photos, and specs, for seven series of heat sinks. **AHAM Tor,** Rancho California, Calif.
Circle 312 on Inquiry Card

Compact Modular Power Supplies and Converters

Circuit characteristics, features, specs, dimensions, and pinouts for regulated ac-dc supplies and for dc-dc converters are listed in catalog. **Intronics,** Newton, Mass.
Circle 313 on Inquiry Card

Enclosures

Small cases, vertical cabinets, desks, and consoles are illustrated with photos in descriptive brochure. **Optima Div, Scientific-Atlanta, Inc,** Tucker, Ga.
Circle 314 on Inquiry Card

Fiber Optic Systems

Capabilities of three fiber optic systems, two of which are TTL compatible, are described in 4-p brochure. **Augat Inc,** Attleboro, Mass.
Circle 315 on Inquiry Card

Emi Shielding

Guide matches range of material characteristics with products, lists applicable data sheets, and includes charts of shielding properties of metals. **Tecknit, Emi Shielding Products Div,** Santa Barbara, Calif.
Circle 316 on Inquiry Card

LITERATURE

Permanent Magnet Stepping Motors

Switching sequence and performance charts, specs, ratings, and dimensional drawings for 1.8 or 0.9° Slo-Syn stepping motors are available in brochure. **The Superior Electric Co,** Bristol, Conn.
Circle 317 on Inquiry Card

Wave Solderable Slide Switches

Long life, low to medium current capacity, detented and momentary/spring return switches are profiled with photo, schematic, dimensional sketches, and suggested mounting pattern. **Standard Grigsby, Inc,** Aurora, Ill.
Circle 318 on Inquiry Card

Copper Clad Printed Circuit Laminates

Selector guide features 3-p foldout chart describing typ applications and specs plus data sheets on superpunch and superpeg laminates. **Westinghouse Electric Corp, Micarta Div,** Hampton, SC.
Circle 319 on Inquiry Card

FFT Based Spectrum Analyzer

Catalog furnishes design and performance information, characteristics, and specs on general purpose analyzer configured as plug-in for Tektronix series 7000 mainframes. **Rockland Systems Corp,** Rockleigh, NJ.
Circle 320 on Inquiry Card

PC Board Time-Delay Relays

Details and specs on temperature compensated PCB mounting time-delay relays are included in literature. **Warren Communications,** Livingston, NJ.
Circle 321 on Inquiry Card

APL Programming Terminals

APL features for Miniterm terminals and Q3 thermal printer are described in data sheet. **Computer Devices Inc,** Burlington, Mass.
Circle 322 on Inquiry Card

Test Instruments/Breadboards

32-p catalog features signal generators, electronic test instruments, logic probes, frequency counters, solderless breadboards, digital troubleshooting instruments, and IC test clips. **Continental Specialties Corp,** New Haven, Conn.
Circle 323 on Inquiry Card

Reference Desk

Line of reference desks and drafting furniture is demonstrated photographically and described in 6-p brochure. **The Huey Co,** Franklin Park, Ill.

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Digital Time-Delay Relay

Brochure introduces series DSA industrial solid state timing relays and cites operational modes, specs, and wiring and dimensional diagrams. **Control Products Div, Amerace Corp,** Union, NJ.
Circle 325 on Inquiry Card

LITERATURE

Winchester Disc Drive

Brochure contains description and specs for 33M-byte unformatted (expandable to 66M-byte) Winchester 3350-level disc drive. **Priam,** Cupertino, Calif.

Circle 326 on Inquiry Card

Data Display Tubes

Condensed physical, optical, and electrical information in brochure is designed to facilitate selection and application of CRTs. **Sylvania Electronic Tube Div,** Ottawa, Ohio.

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Precision Potentiometers

Engineering manual catalogs conductive plastic and wirewound precision potentiometers, including industrial, standard, and custom designs. **Maurey Instrument Corp,** Chicago, Ill.

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Circular Connectors

Catalog includes specs, photos, exploded view and dimensional drawings, and contact arrangement for MSA, MSB, MSE, MSF, MSR, and ER series designed to MIL-C-5015. **ITT Cannon Electric,** Santa Ana, Calif.

Circle 329 on Inquiry Card

Synchro Converters

Selection, information, and specifications for S-D, D-S, and special function converters, and synchro instruments are included in brochure. **ILC Data Device Corp,** Bohemia, NY.

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Monolithic Data Acquisition Guide

Specs and descriptions of DACs, sample and hold amplifiers, analog multiplexers, analog switches, voltage references, and comparators are included in guide. **Harris Semiconductor,** Melbourne, Fla.

Circle 331 on Inquiry Card

Electronic Instruments

Full-line catalog features specs and applications for instruments including oscilloscopes, frequency counters, and video generators. **Leader Instruments Corp,** Plainview, NY.

Circle 332 on Inquiry Card

File Compression Encryption System

Brochure supplies overview of file compression encryption system tailored to IMS/VS database environments. **Informatics Inc,** Woodland Hills, Calif.

Circle 333 on Inquiry Card

COS/MOS Integrated Circuits

Manual details design, operation, and application of devices; explains COS/MOS technology; and lists characteristics of A and B series. For a copy of 168-p manual, send $5.00 to **RCA Solid State Div,** Box 3200, Somerville, NJ 08876.

GUIDE TO PRODUCT INFORMATION

NOTE: The number associated with each item in this guide indicates the **page** on which the item appears—**not** the reader service number. Please do **not** circle the page number on the reader service card.

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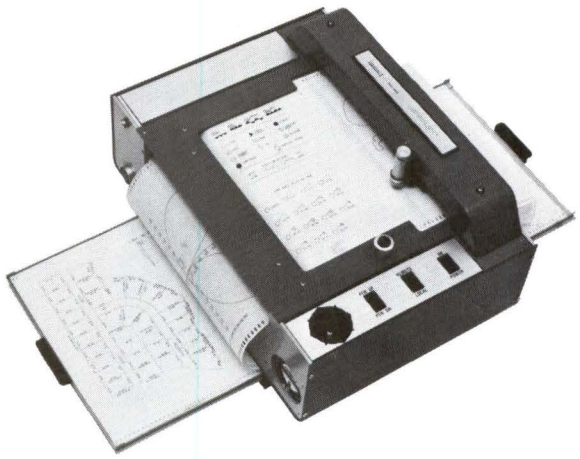

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