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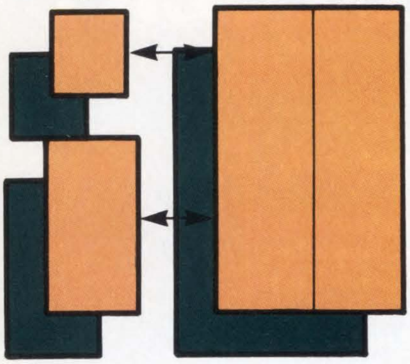

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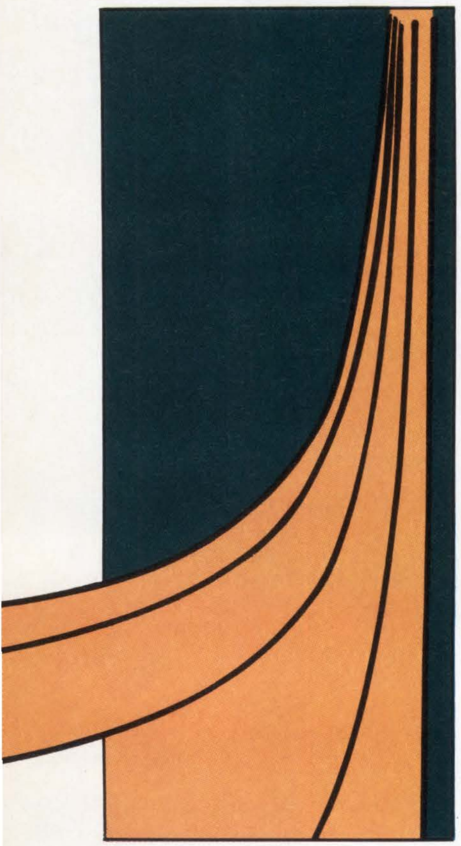
System design



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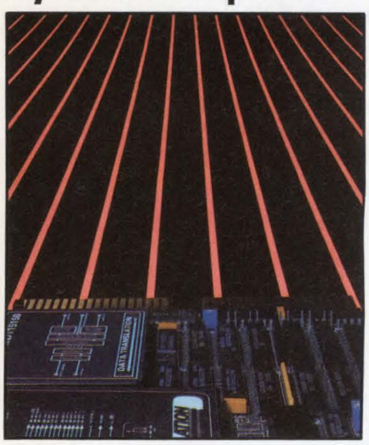
Vol 23, No. 5
May 1984

This month's cover was created and designed by Mark Lindquist on the Digital Effects Video Palette III and D-48 high resolution camera system.

Special report on graphics technology

System components



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Departments

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BPA ABP

UP FRONT

MCC adds research directors

Microelectronics and Computer Technology Corp, the Austin, Tex-based research and development group put together by former CIA deputy director Bobby Inman, at last has research directors in place for six of its seven programs, and research is already getting under way. MCC was formed in 1982 by 10 American microelectronics and computer corporations to pool research funds and personnel. Research programs currently staffed with full-time directors are software technology packaging, VLSI/computer aided design, and advanced computer architecture. The latter program, a 10-year effort, focuses on four major program directions: artificial intelligence, parallel processing, human factors technology, and database system management. MCC now offers an associate program that will allow companies with resources smaller than those of the full shareholding companies to participate. Associate members will be assured an efficient flow of nonproprietary data, as well as licensing of developments three years after full shareholders.—*T. W.*

First two-user Lisp machine promises to help technology transfer

Workstations to develop artificial intelligence-based application programs running the Lisp language set their purchasers back $100,000 or more depending on the workstation's single-user configuration. This price is a formidable barrier to the widespread use of AI by the computer design community, and limits the ability of non-AI-oriented firms to learn about the new discipline. So, LISP Machine, Inc (Los Angeles, Calif) has taken advantage of the Texas Instruments NuBus architecture and NuMachine to come up with the Lambda 2X2, a two-user, full-function Lisp machine. To be delivered July 1, the 2X2 costs only $55,000 per user. It sports two fully independent, concurrently operating Lisp processors, each built on four PC boards connecting to the 2X2's internal NuBus. Each processor provides a 128-Mbyte virtual address space for its user along with a keyboard, mouse, high resolution display, and display controller. Users share physical RAM, a 470-Mbyte Winchester, an integral Multibus I for connection of Multibus I-based peripherals, and an Ethernet interface.—*H.H.*

But will it make the top 40?

Capitalizing on its parent company's expertise with audio disk technology, Capitol Data Systems, a division of Capitol Records (Los Angeles, Calif), has developed a 5¼-in. floppy disk that can be a medium for any disk drive system, from single-sided, single-density to double-sided, double-density or quad-density systems. The "universal" disk can be used on any standard personal computer, regardless of its disk drive system, to automatically double the capacity of single-sided drives. The disk can also be inverted to record on the second side after one side has been loaded. The disk's developers attribute its universality to testing for a missing pulse threshold over the entire surface of 96 tracks on both sides. Threshold levels tested at more than 50 percent higher than usual industry levels. The user is thus assured of maximum floppy disk capacity with each disk. Two other features: two data-protect notches in the disk's sleeve allow the disk to be inserted with either side facing the read/write head, and two index holes allow the disk drive to register and index recording tracks on either side of the diskette. A pack of 10 diskettes lists for $55.—*N.M.*

A CAD workstation for the less privileged

A "personal" computer aided design system from Control Data (Santa Clara, Calif) is reported to provide 80 percent of the schematic and accounting functions an engineer needs at 20 percent of the cost incurred using large scale design workstations. In this way, the company hopes to induce engineers to use its Cybernet Services, an online data network that ties personal computers to such heavies as the Cyber 205 supercomputer. The under-$16,000 system comes with IBM PC, software package for schematic entry, netlist extraction tool tapping several design software programs, dot-matrix printer/plotter, 10-Mbyte Winchester drive, 360-Kbyte floppy disk drive, and mouse. Without the PC, the package costs about $8000.—*N.M.*

Smalltalk now commercially available

The first commercial offering of the Xerox Palo Alto Research Center's Smalltalk-80 package has been announced by Syte Information Technology (San Diego, Calif). Smalltalk is a combination of a window-oriented operating system, an object-oriented programming language, and a programming environment. The package runs on Syte's series 3000 micromainframe, which is based on National Semiconductor's 16032 microprocessor. It shares system resources with UniSyte—the company's proprietary implementation of Unix System V—via calls to the global environmental manager (GEM). The GEM provides a standard interface between programs and the computer system hardware. Pricing is expected to be in the vicinity of $1500.—*S.B.*

Videotex spurs display chip design

Videotex, installed in a variety of tentative services in Europe, is aimed at creating a home information system, and may eventually make large inroads in the U.S. as display standards and cable installations proliferate. In anticipation of such developments, expected around the 1986 to 1988 time frame, Texas Instruments (Dallas, Tex) is developing an advanced video display processor (AVDP) chip that supports the North American Presentation Level Protocol Syntax (NAPLPS). The AVDP will support a bit-mapped raster display of 256 x 210 with 16 colors/pixel and an onchip color palette with 512 color options, as well as 40- and 80-col color text. To support the rapid screen painting frequently used by NAPLPS, the AVDP will have a block-move command that will be able to simulate movement on the screen and also off-load polygon fill routines from the CPU. A video overlay feature will allow captioning on live video with videotex or teletext services; an onchip sound generator can prompt the user with beeps or synthesized music.—*T.W.*

Electronic mail merges with voice memos

Digital Sound Corp (Santa Barbara, Calif) moves closer to an integrated voice/text messaging system with its Voiceserver 1 store-and-forward system. Although presently configured to handle voice only, its 68000-based general purpose processor and dual TMS320 digital signal coprocessors can be programmed to handle text-to-speech conversion in addition to text only. Future plans also include limited speech-recognition capabilities for commands and user access, as well as Unix support for PBX-based networks. This level of integration is beyond the capabilities of the current generation of message store-and-forward systems. Typically, separate systems are needed for voice store-and-forward and electronic mail with common user interfaces used to tie the two together at the application level.—*J.A.*

Rigid disk controller board bridges multiple users

An intelligent controller that can drive up to four 8- and 14-in., 9.6-Mbit/s storage module drives, the ACD-5580 from Adaptec (Milpitas, Calif), interfaces up to seven host processors. It sports such Small Computer System Interface (SCSI) features as the disconnect/reconnect function, which lets the user run concurrent I/O tasks by handling multiple seeks and reads/writes with the I/O disconnected. The board is designed for noninterleaved operation to allow all data on one track of the disk to be accessed in one rotation. Two complementary host adapter boards interface between the host computer and the controller board. One board interfaces an S-100 bus on the host side and an SCSI bus on the controller side, while the second is for a Multibus-based system. The adapters shoot data at a 1.5-Mbyte/s clip from the SCSI bus to the host's local memory. Available in production quantities by the third quarter of 1984, the controller board will list for $980, while the S-100 and Multibus adapter boards will be priced at $425 and $460 respectively.—*N.M.*

Problems chip away at great expectations

Availability of high performance local network frontend processors may be slowed by production delays for network controller chip sets from Advanced Micro Devices (Sunnyvale, Calif) and Intel Corp (Santa Clara, Calif). Some potential customers might have to wait until summer for volume shipments of AMD's version of the local area network controller for Ethernet (the LANCE chip), while it may be as late as the second quarter of next year for another controller, the Intel 82586, to be available in appreciable quantities. At least one network vendor reportedly has had to alter plans and had to design in a less-powerful chip set from Seeq Technology, Inc (Santa Clara, Calif) because of the scarcity of the LANCE chip. The 186/10 frontend processor board from Intel may also be delayed due to the unavailability of both the 82586 controller and the 80186 microprocessor, which serves as CPU.—*J.A.*

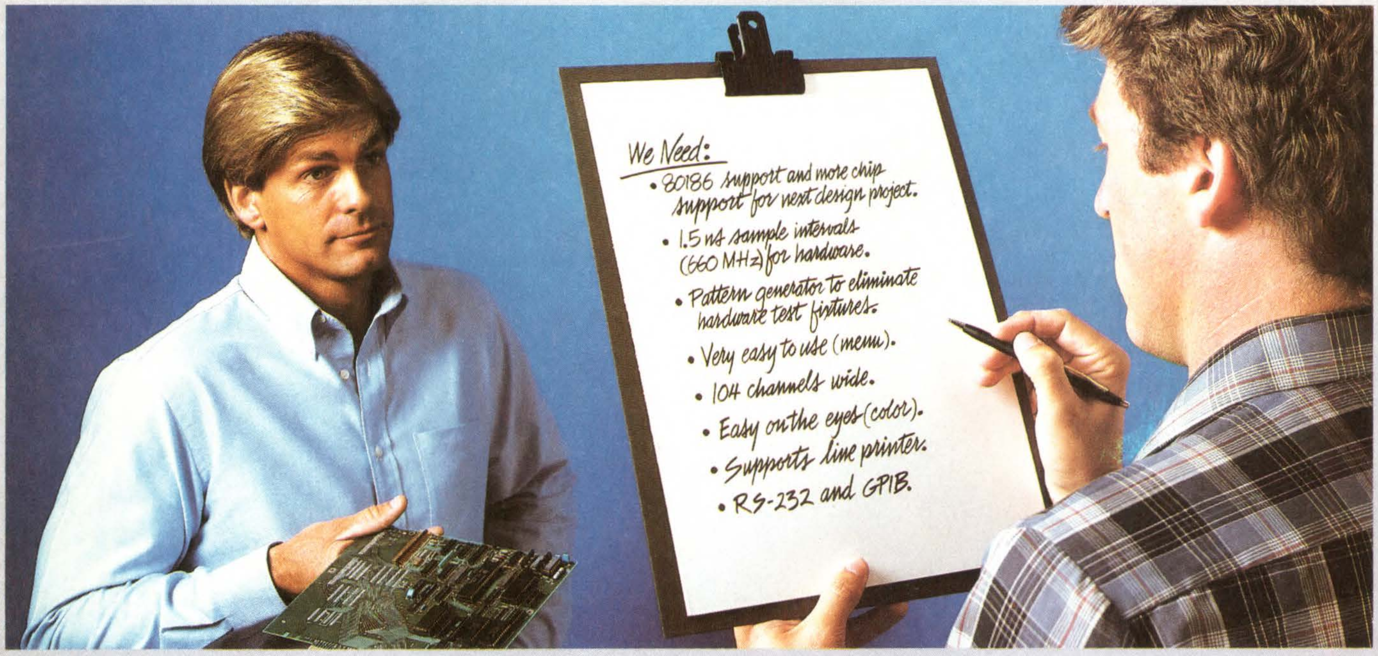
Color added to graphics workstation

An RGB color monitor and associated circuitry have been added to the low cost Cascade X integrated engineering workstation from Cascade Graphics, Inc (Santa Ana, Calif). The system has six colors plus black and white and is priced at under $40,000. It consists of a repackaged Apple II running the UCSD p-System to handle text and file generation. The system's display processor is a 12-MHz 68000 board from Digital Acoustics (also in Santa Ana, Calif). Resolution is 1024 horizontal x 1024 vertical pixels (only 796 of which can be displayed concurrently). Each bit plane is divided into two 128-Kbyte pages, one of which is displayed by the 7220, while the other is updated by the 68000 CPU. The system is scheduled for volume production in the August/September time frame.—*S.B.*

Program packages take AIM at Unix

A suite of programs written in C has been introduced by AIM Technology, Inc (Santa Clara, Calif) to provide benchmark comparisons between Unix implementations. The packages, called the AIM Benchmark Suite II, are available on half-inch magnetic tape for $2575, and include 36 programs. The programs can be combined to test how efficiently a given Unix system handles text processing, compilation, calculating, and graphics tasks. A second part of the package produces either tables or graphs that let the implementor compare the performance of different systems.—*S.B.*

You do.



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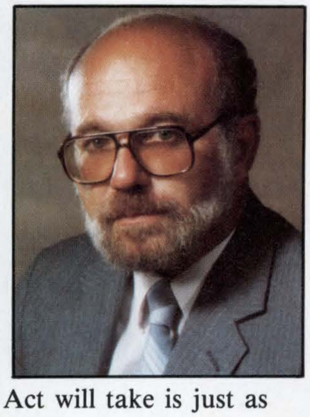


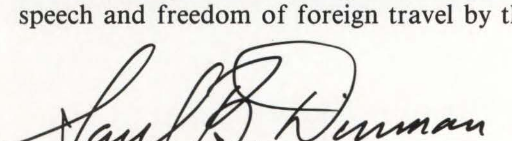
Recent front-page business news across the country presented the sensational details of how one hi-tech company—Digital Equipment Corp—was finally punished for having parts of a computer system show up on the shipping docks of certain friendly European nations. Unfortunately, those parts were being readied for shipment behind the Iron Curtain. As a penalty, DEC's just expired blanket export licenses were replaced by licenses that are only good for six months. In addition, future shipments to Norway and West Germany will require individual export licenses for each piece of equipment shipped. From the reaction, it seems that the Department of Commerce is continuing its dispute with the Department of Defense over the still-undefined Export Administration Act by testing the various provisions stuffed into the House and Senate versions. The whole subject of what form the new Act will take is just as much a political football as ever.

For DEC, the punishment is not much more than a nuisance, merely creating more paperwork and red tape. On a larger scale, however, the consequences are considerably more serious. Neither the people's press (as opposed to the trade press) nor Congress seems to understand the ramifications of this incident. The press has not informed the public of the controversy beyond the fact that we have to keep our computers out of Russia. It doesn't seem to know or care that this hardware was of commercial grade and probably has at least two or three German and Japanese equivalents. Thus, the press reflects the feeling that the U.S. can stop the "enemy's" scientists from developing new weapons by taking away their American-made pencils. The press seems to forget that other countries that freely trade with the "enemy" make pencils; the "enemy," if they have not already done so, can figure out how to make pencils and will certainly do so if pencils are unavailable through foreign trade. We do not have (and never really had) a monopoly on technical genius.

Discussion of the Export Administration Act these days may produce a variety of inputs that range from the sublime to the paranoid, but not the feeling that anyone in Washington has really put them all together. Most congressmen do not seem to know that many of our hi-tech firms depend on exports for as much as 30 to 50 percent of their revenues. They do not seem to understand that a loss or decrease of those exports will result in future unemployment in their districts. Moreover, in its rush to push the bill through, Commerce will probably settle for any version that minimizes dilution of its authority to DoD in international trade.

Due to this ignorance on all parts, the provisions of the Export Administration Act will probably be dictated by DoD. That agency will have most of the say about what technology is exportable, even though many of those same parts can be removed from a Japanese-made microwave oven purchased in a Soviet department store.

But that isn't the entire picture. This political maneuvering could have more important consequences. Allowing a department concerned with national defense to dictate the constraints on international commerce leaves the door open to other possible constraints on technical books, scientific papers delivered at meetings (many of which are already subject to DoD approval), the technical press, consulting engineers, and whatever else strikes the department's fancy. We are not just talking about the DEC incident here, we are talking about something that may eventually affect freedom of speech and freedom of foreign travel by the general technical population of the U.S.



Saul B. Dinman
Editorial Director

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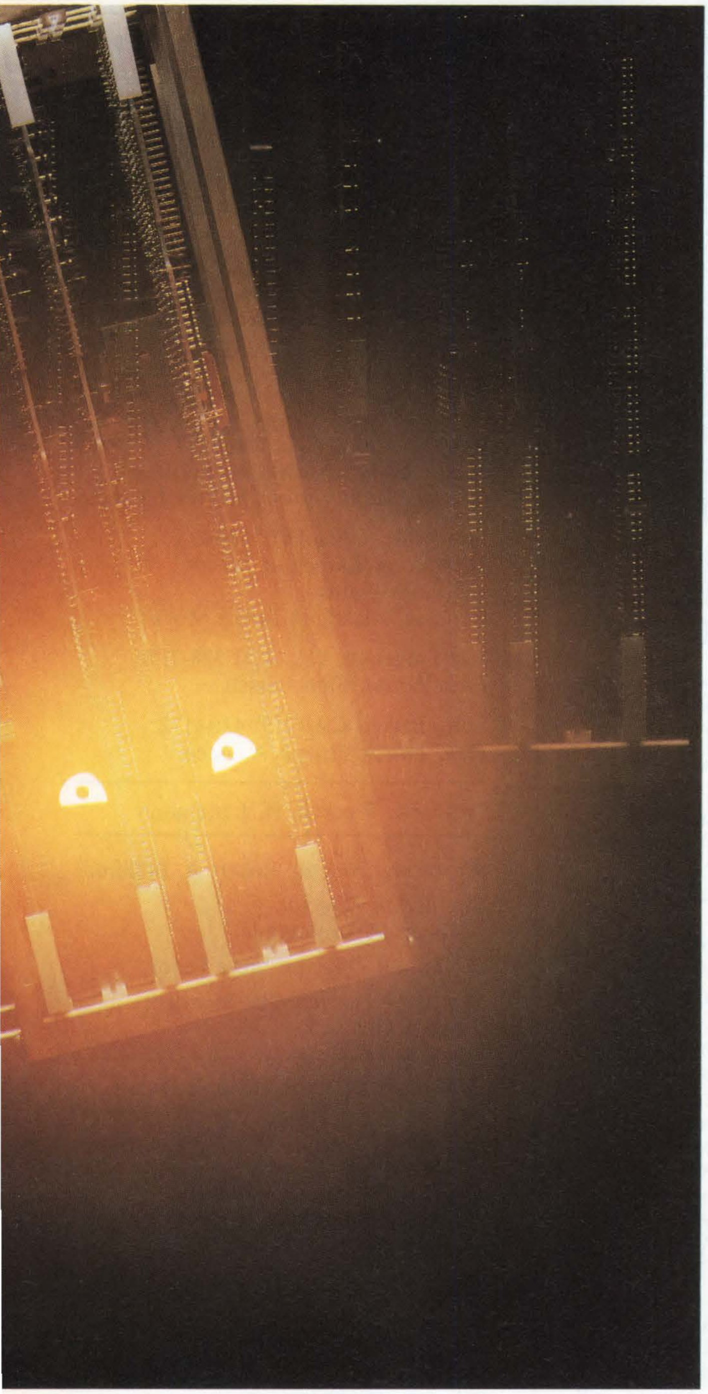

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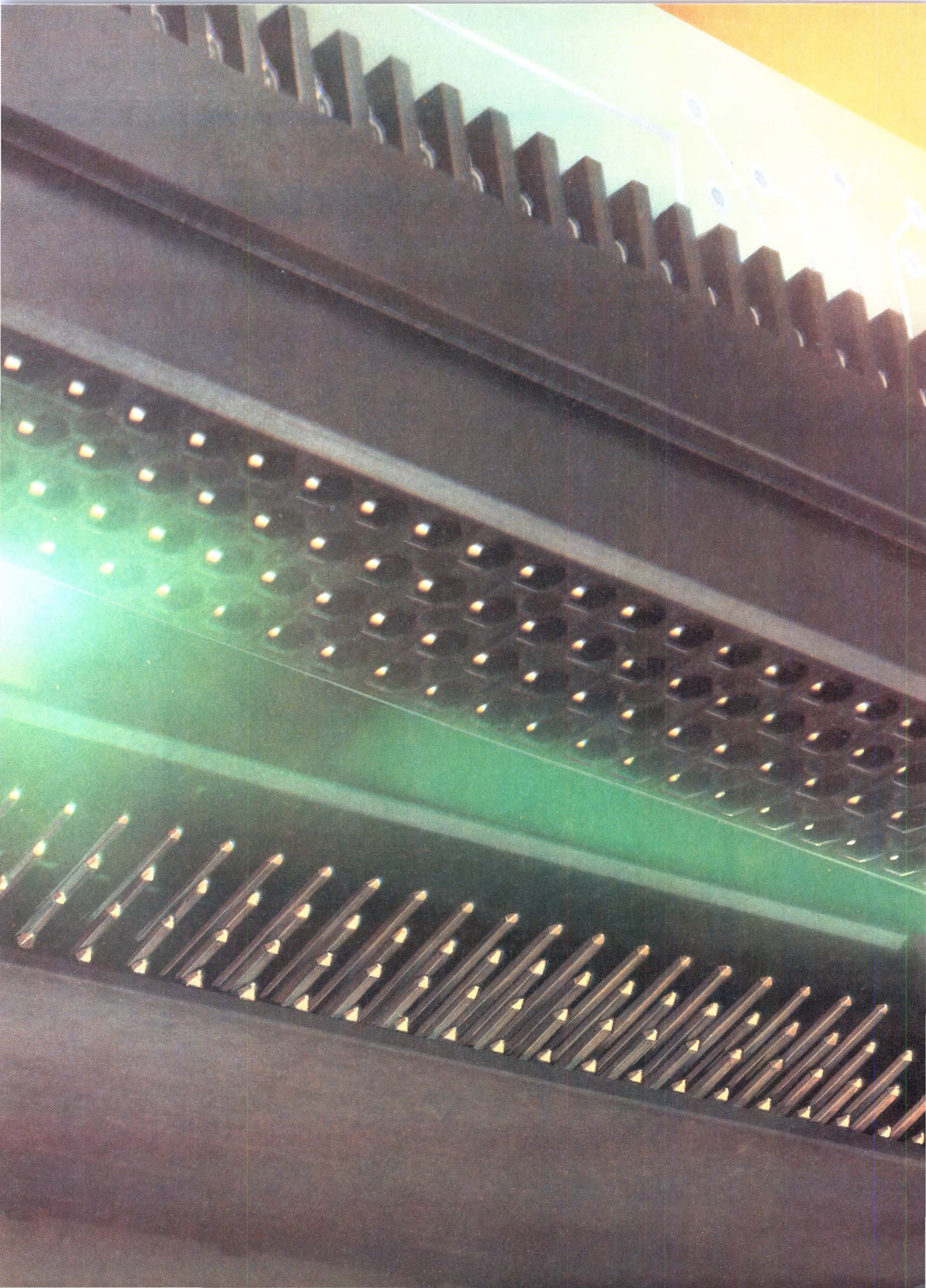

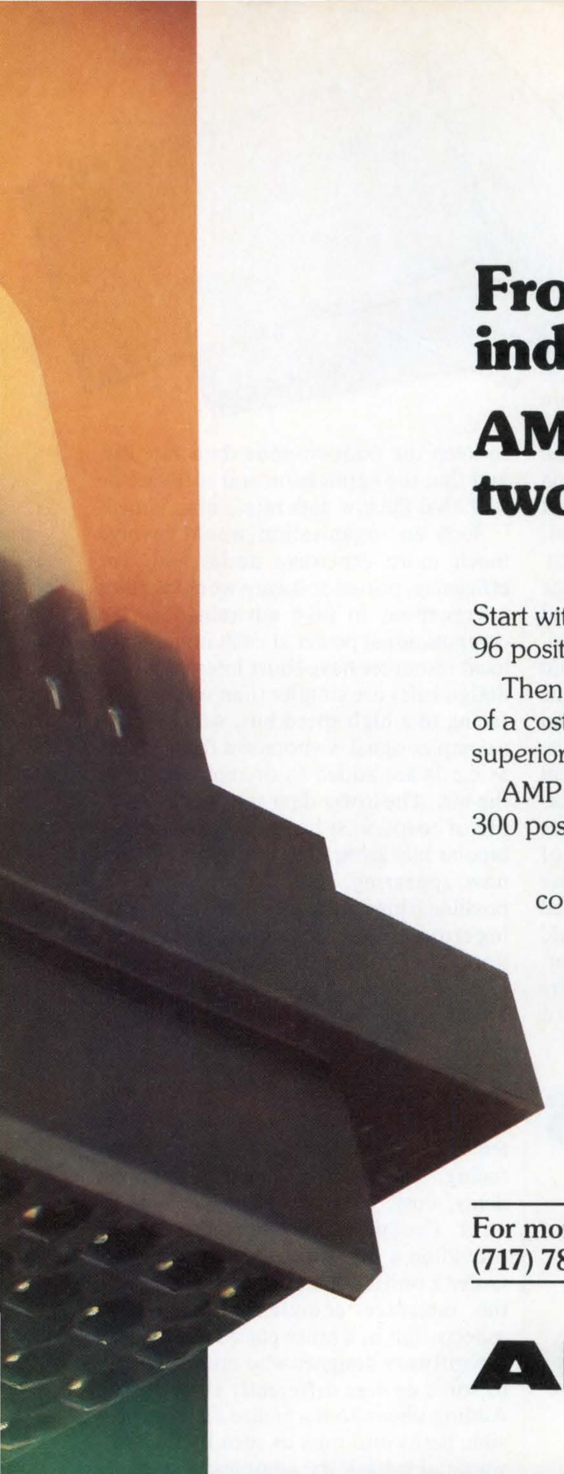

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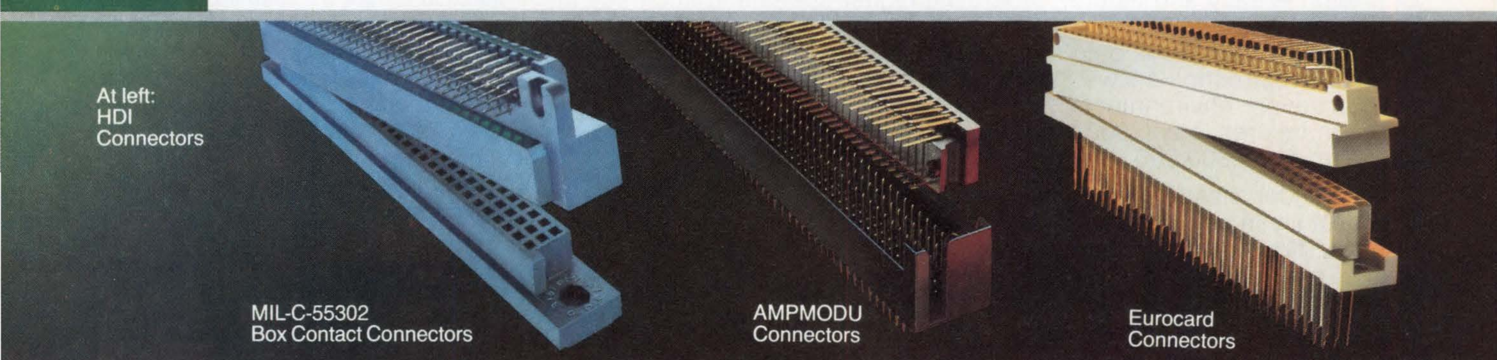

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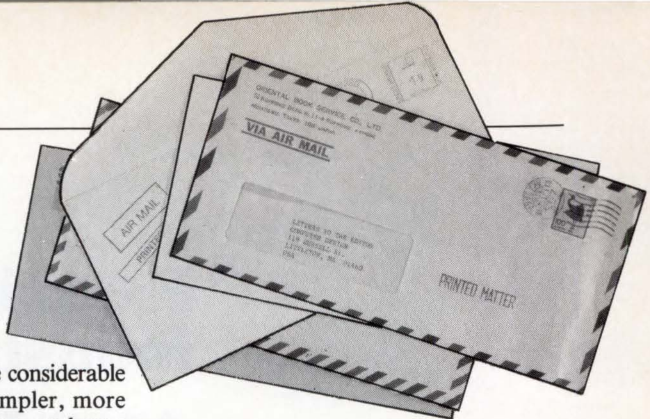

Multibus II—on the mark

The discussion of microcomputer bus systems in Harvey Hindin's article, "Thirty-two Bit System Designers Face Decision Time," (Feb, 1984, p 27) was timely and informative. The percentage of a system board devoted to the interface with these buses seems to be growing and we now find that the best designs will include or anticipate inclusion of specialized ICs to perform the interface function (or part of it). Could a less complex organization suffice in place of the VME or Multibus?

Many bus-based systems will be used as general-purpose computers in that they will have some sort of rotating memory device and an operating system. Thus, while the following argument may lack force in a dedicated analog processing system with a silicon operating system on the CPU board and only two other boards (an A-D converter/D-A converter board and a memory board), it still has some application—information is read from the A-D converter, processed, and written to the D-A converter. In a disk-based system, much of the ever-increasing bus bandwidth provided by new bus designs is occupied with mundane activities such as disk directory scanning.

It seems much more efficient to put significant local processing at any node that would otherwise generate considerable bus traffic and move to a simpler, more flexible interconnection scheme, such as a local area network or an enhanced Small Computer System Interface (SCSI). Such a node would be much more than what is currently known as a file server. Yet, this node would not be adverse to device-specific operations (thereby violating the spirit of SCSI in some ways) such as read and write physical sector, if required. This type of system organization would be sensitive to software design in the same sense that a system organization around cache memory or virtual memory is. One could not code at will for such a system in complete ignorance of its implementation. On the other hand, with some attention to software utilization of resources, it might be possible to achieve performance equivalent to high speed buses. In a sense, this organization would be very regular: every node is a processor. To work, the organization would require that every node be a sufficient processor to keep the node-to-node data rate low and that the application and software be such that the low data rate is maintained.

Such an organization would involve much more expensive nodes and, for efficiency, ported software would need to be rewritten to take advantage of the computational power at each node. Since local resources have short internal paths, design rules are simpler than when interfacing to a high speed bus, which offers a complex signal environment that changes as cards are added to or removed from the bus. The lower data rate would allow use of NMOS/VLSI instead of the various bipolar bus-arbitration and support chips now appearing, and move away from possible fringe effects such as synchronizing error, cross-coupling, signal attenuation, and voltage standing wave ratio (VSWR) mismatch (eg, reading a file on a high speed disk and controller, packaging and sync for transmission on the bus, and depackaging and sync for use by the processor).

If the file is to be modified and rewritten, the process involves additional interfacing. Each such interface involves delay, cost, power, and the chance of error. The Swiss-Army knife approach of providing a bus for every possible need under a unified specification may attack the interface complexity and speed aspects, but in a sense passes the buck to the software designer who must now talk to some devices differently than others. Adding silicon to normalize all these possible paths into one, as seen by the software, adds back the complexity or delay or both. Normalized or not, such paths are not the same, so performance suffers if they are so used and the software design suffers if they are treated separately. As described, "Multibus II" is certainly appropriately named.

Brian Converse
Warminster, Pa

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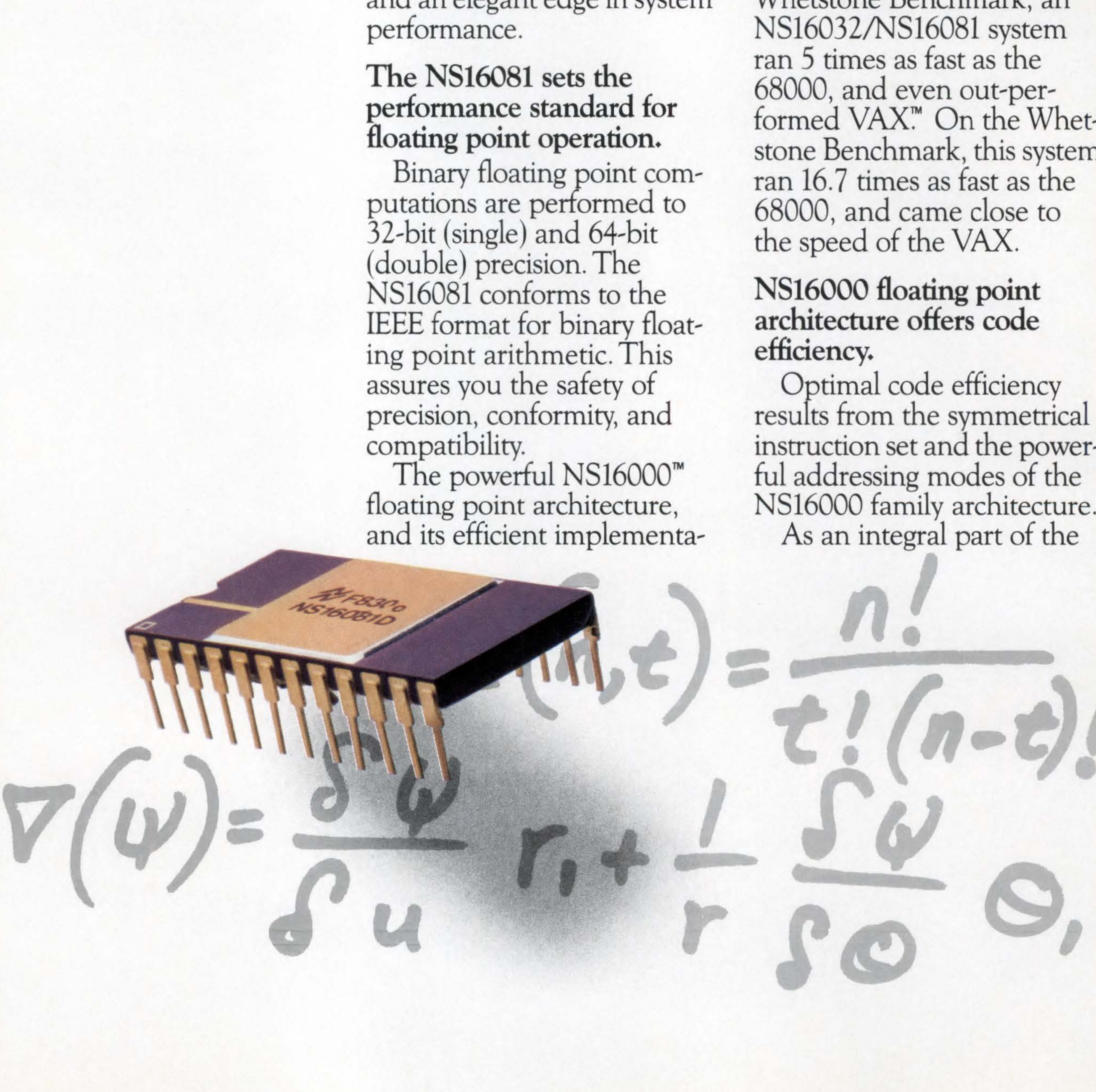

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FLOATING POINT PERFORMANCE COMPARISON		
Execution Time		
SYSTEM	FFT	WHETSTONE
NS16000 family[1] (10MHz)	3.0s	4.3s
68000 + ROM[2] (10MHz)	15.0s	72.0s
VAX-11/750[3]	4.0s	4.0s

1. Difference in execution times from previously published numbers is a result of improved numerical algorithms in the Pascal library.
2. 68000 floating point implemented in standard ROM-based software Motorola provides no floating point hardware to-date.
3. Without floating point accelerator.

REGISTER TO REGISTER ADDRESSING MODES		
NS16081 (10MHz)		
FUNCTION	SINGLE PRECISION	DOUBLE PRECISION
Add	7.4μs	7.4μs
Subtract	7.4μs	7.4μs
Multiply	4.8μs	6.2μs
Divide	8.9μs	11.9μs

Note: These timings are based on an NS16032/16081 system. They measure the entire instruction time, including communication overhead and worst-case normalization in a system with no WAIT states.

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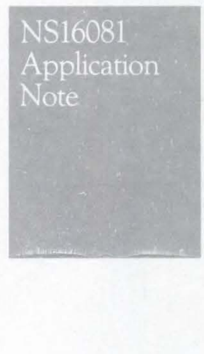

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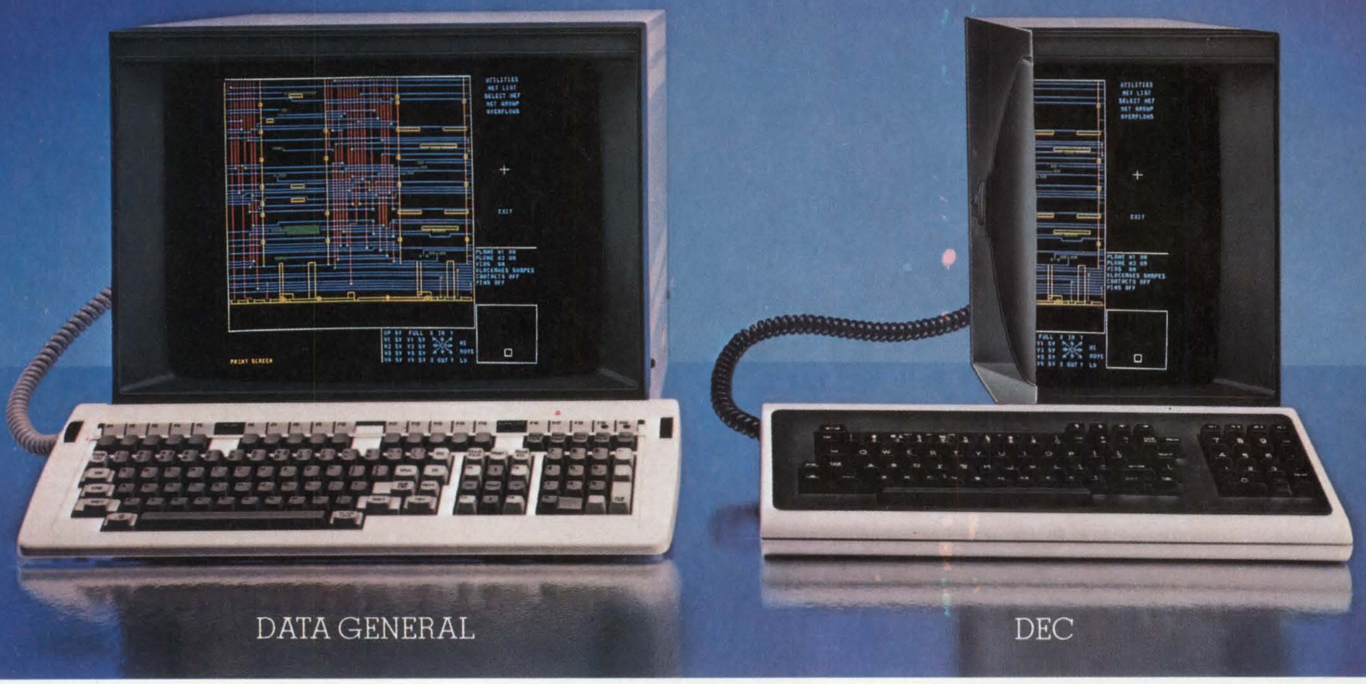

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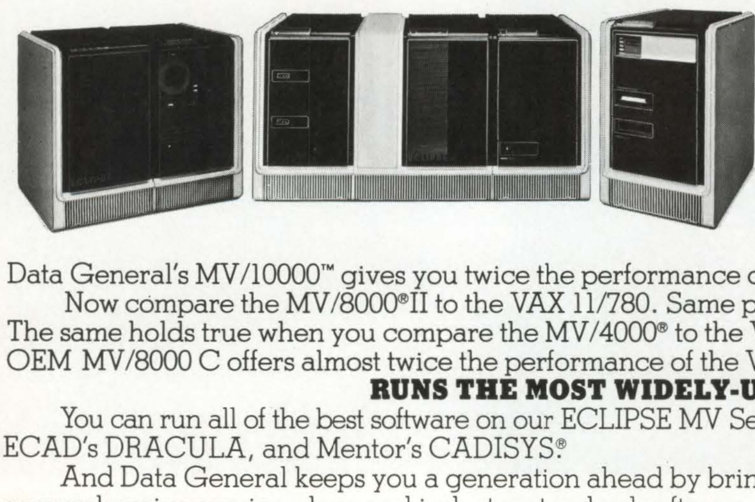

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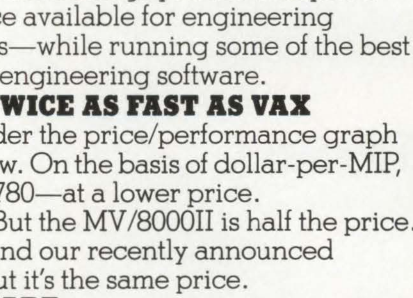

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CIRCLE 15

VLSI software components balance standardization with flexibility

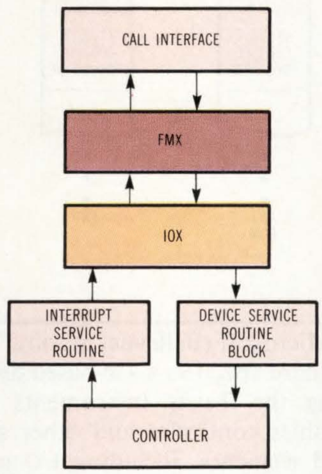
Advances in VLSI are increasing not only the capacities of memory components, but also the ability to fit significant amounts of code on chips along with other functions. This, in turn, is beginning to influence long term design considerations and is resulting in software components that are configured to optimize flexibility and efficiency when they are built into systems. In some cases, a component/address placement standard is emerging to fit system software requirements. In other cases, the silicon software designers are going to great lengths to allow maximum freedom of address placement of the silicon software components.

This trend will no doubt continue in the two areas described above and become more evident as more functions are defined as VLSI silicon subsystems (ie, more hardware functions are integrated on single chips). Another influential factor will be the appearance of more functions that might have been defined as hardware logic or as part of a RAM-based operating system as silicon software components. The system designer can theoretically place these components anywhere in a system's memory map.

Silicon subsystems

One example of the latter is the realtime multitasking operating system kernel—VRTX—by Hunter and Ready, Inc, (Palo Alto, Calif). Since its introduction a couple of years ago, VRTX has undergone several revisions and been extended to serve a number of 16-bit processors including the 8086, 68000, Z8000 and the 8-bit Z80. Recently, the company introduced two software component extensions to VRTX: IOX, a collection of I/O services that can be called by the system, and FMX, a file management extension that can support various device formats and file structures.

These two components have made it necessary to establish certain conventions. These calling conventions



With the I/O and file management (IOX and FMX) extensions to VRTX, calls for services are routed through VRTX to the call interface table. Access to a specific controller is made via a device service routine block, which is also reached via a pointer. IOX can handle multiple devices and channels in this manner.

enable systems to call VRTX services as well as IOX and FMX services in a consistent manner, while leaving the system designer free to place the components at any address in microprocessor memory. Since VRTX services are called by referencing a table of pointers, the table can be placed anywhere in memory and the pointers adjusted to fit its location.

In the same manner, the company has established a calling convention for its new products that will institute a standard for using its own services and future software components. Moreover, to avoid conflicts, the convention will also allow custom components to be written to the standard. Essentially, accessing pointers placed relative to the position of VRTX call the new services. Thus, all components can still be placed anywhere in memory and linked by their respective pointer tables.

File and I/O for VRTX

The IOX chip contains a collection of basic callable I/O services for a realtime environment. At the IOX level, these services are generic and device independent, with such features as buffering and block operation. The FMX allows the system designer to organize devices such as disks, tapes, or Ethernet controllers and to create a hierarchical file structure.

The first FMX version available will be called FMX/DOS and will support an IBM PC-DOS compatible file format. However, because it will be working with IOX in a VRTX system (although the resulting file structure will be PC compatible), the version will still come out of a realtime multitasking environment. Other disk formats, such as Unix, are possible and even likely. To ensure maximum flexibility, however, the I/O software components are isolated from the hardware on the other end.

Since IOX cannot be expected to know about all possible controllers, it accesses a given physical controller via a device service routine block (DSRB). In turn, the controller can get the attention of the IOX via an interrupt service routine (ISR). The VRTX system gets to the I/O software components via a call interface. In this manner, as with VRTX itself, the components can be anywhere in the

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VLSI software

(continued from page 27)

memory map as long as the call interface and service routines on either side contain the proper pointers.

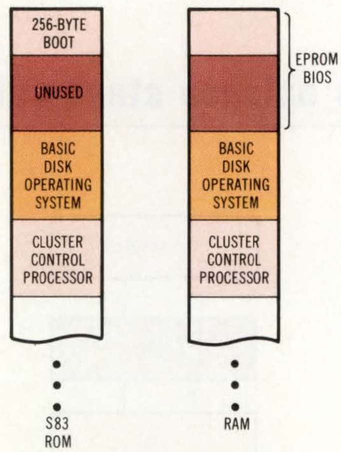
The component calling convention makes requests for software component services via a single architecture-dependent instruction. That is, for every processor the company supports, there is one instruction that can be used to cause a software-generated interrupt or "trap." These traps (eg, INT for the iAPX 86 family, SC for the Z8000, and RST for the Z80), are not like ordinary subroutine calls in that they depend only on the runtime contents of a hardware-defined trap vector location to reach their destination. Thus, because they are not bound into the calling program, they allow a kind of runtime linkage that makes them independent of the application program as well as the user's development system.

Calls from an application (eg, a program written in a high level language), first issue the trap that vectors control to VRTX's system call entry point. Next, on the basis of the function code, the VRTX decides which component and which function within that component to invoke. Such calls can be either register based, in which parameters are passed most rapidly, or packet based, due to the limited number of available registers. Packet-based calls use one more register, which contains the address of the parameters to be issued to VRTX as well as the other software components called by it.

Fixing the hardware

A different tendency appearing for some high volume designs is the definition of a set of standard hardware components and their address locations to fit a given system software convention. This makes sense because of the high function density made possible by present VLSI technology, and hence the impetus to keep component count down and use standard programming languages and application software in high volume products, such as personal computers.

An example of the above issue is the MSX specification promulgated by Microsoft (Bellevue, Wash). This standard specifies a Z80-based design using the Texas Instruments 9918 graphics controller and other standard elements, including I/O ports and disk controllers. The standard's purpose is to allow low end 8-bit machines to run standard software, including a 32-Kbyte version of Microsoft Basic. To this end, Microsoft has developed an operating system—MSX/DOS—that can be either disk or ROM based, will be largely CP/M compatible, and will allow transfer of data files between MSX and PC-DOS machines.



In the prototyping version of the S83 operating system processor, the Z80 loads from ROM into external RAM, then turns off ROM and executes from the RAM copy. In this configuration, it expects to find the basic I/O system (BIOS) in an erasable PROM.

Comparing the VRTX and the MSX shows a trend for variations in possible hardware configurations that demand great flexibility on the part of silicon operating system software. Only the MSX, however, has a fixed software standard defining the possible range of hardware configurations—both in the interests of cost and component count and application compatibility. It is also interesting to note the first choice of PC-DOS file compatibility. This choice apparently stems from the belief that realtime control and data acquisition systems using this format can easily supply data to the desktop office environment.

A possible bridge between these trends is made possible by the function density provided by VLSI. The S83 operating system processor by American Microsystems, Inc (Santa Clara, Calif) combines a Z80 microprocessor and 8 Kbytes of ROM on the same chip. The company is initially offering a prototyping sample chip containing Personal CP/M, intended for developing high volume personal computer systems with lower parts counts. While this in itself represents no great breakthrough, it has implications for future system designs using both the trends described.

In its present configuration, the S83 operating system processor leaves the area that would normally contain the machine-specific basic I/O system (BIOS) blank. The ROM portion of the chip can be turned on and off to allow Personal CP/M to be loaded into RAM and used with either erasable PROM-based BIOS or to allow the developer to write a BIOS. Subsequent, more specific versions may contain the complete operating system and run entirely from onchip ROM.

According to AMI, both the ROM-based version of MSX/DOS or the Z80 version of VRTX could easily be implemented on the S83. This would mean a futher reduction in parts counts for both kinds of systems, and that other components of VRTX-type realtime systems could use onchip drivers such as those beginning to appear on intelligent peripheral controllers in electrically erasable PROM.

—Tom Williams,
West Coast Managing Editor

Half-inch tape drives cry out for greater compatibility

Standardization remains a desired goal for half-inch tape drive vendors seeking to back up rigid disk drive capacities exceeding 40 Mbytes. Yet, the many incompatible media types, tape formats, and device interfaces threaten to engulf potential users in a veritable sea of confusion.

Conflicting needs are the driving force behind this proliferation. On one hand, many users need to maintain compatibility with existing hardware and software investments. On the other hand, new types of tape drives are needed to handle the increased capacities of the latest 5¼- and 8-in. rigid disk drives. No longer can one tape drive, such as an American National Standards Institute (ANSI) 9-track interface with 10.5-in. reels, meet all needs.

Data interchange is key

As a result, compatibility becomes the major issue for prospective users. The sheer number of tape drives attempting to meet these needs makes it more cumbersome to move data from one half-inch tape drive to another. At last count, over six types of half-inch cartridges have been proposed for capacities ranging from 40 to 330 Mbytes. This does not include the standard 10.5-in. reel used for streaming-like operations up to 46 Mbytes, nor a proposed 4-in. reel with capacities quoted at 160 Mbytes.

However, tape drive vendors do come closer to agreement on tape formats and device interfaces. One group backs the ANSI 9-track interface (at either 1600 or 3200 bits/in.) found on existing start/stop drives. However, many others have adopted the QIC-24/QIC-02 format and interface specifications originally developed for quarter-inch cartridges (see *Computer Design,* June 1983, p 48). Finally, a third discernible trend has tape drives emulating popular 5¼-in. disk interfaces like ST506 or the Enhanced Small Device Interface (ESDI). The physical formats of these drives also resemble the ST506 and ESDI.

A variety of formats

Compatible physical formats and packaging are minimum requirements for effective data interchange. For example, it does a user little good to have two drives with the same ANSI-compatible interface and format if one drive uses 10.5-in. reels while the other uses the 4-in. cartridge developed by Rosscomp Corp (Cerritos, Calif). The company packages its tape drives for 5¼- and 8-in. disk drive form factors much smaller than those required to mount the 10.5-in. reels.

Furthermore, differing tape formats make data exchange impossible even if the physical packaging is similar. A prime example are two competing cartridges proposed to ANSI by Digital Equipment Corp (Maynard, Mass) and Memorex Corp (Santa Clara, Calif). Both have the same 4- x 4-in. footprint, yet are incompatible with each other—the DEC proposal specifies a total of 22 tracks, while Memorex specifies only 20.

In contrast, device interfaces play a relatively minor role in data interchange. They essentially affect only the way that controllers and tape drives talk to each other and not the form of the data that is passed. Device interfaces cause data interchange problems only when the functions of the tapes are incompatible with those understood by the controller and associated software device driver.

To illustrate this, John Frassel, product line manager for Distributed Logic (Garden Grove, Calif), points out that DEC computers will not read tapes written on drives using the QIC-02 interface. This problem occurs because existing software drivers (eg, the TS-11) have no knowledge of streaming functions, such as tape tensioning and retensioning, which ensure even tape travel. Thus, they cannot read the data in the same manner as it was written. To overcome this incompatibility, controllers must work at two command levels—those understood by the computer and those understood by the tape drive.

The difficulty of integrating new product developments into existing systems causes many users to choose tape drives that work well with existing application programs, operating systems, and hardware. The 10.5-in. reels with 3200 ft of tape remain popular as a backup,

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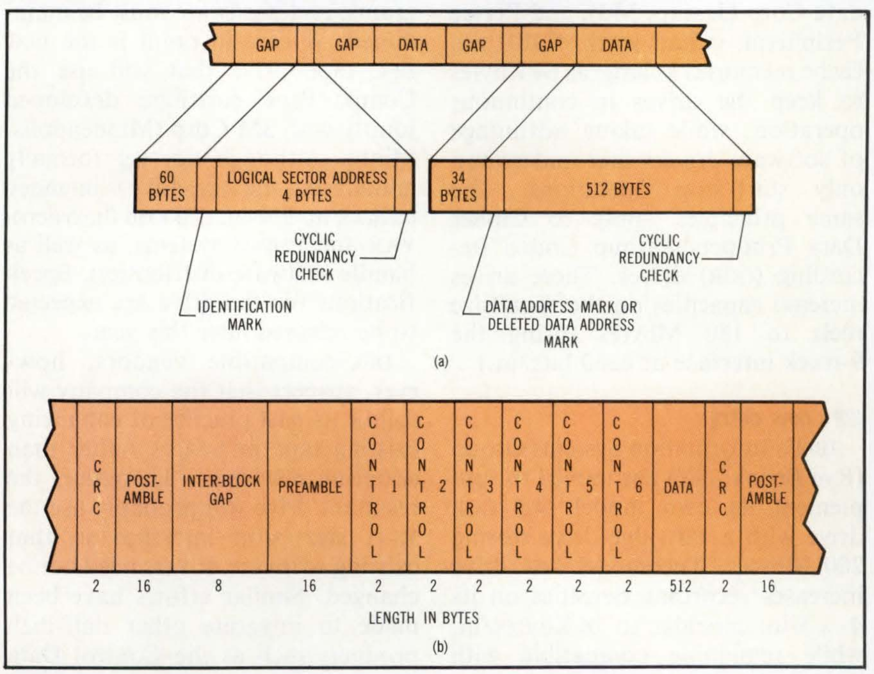

To provide maximum compatibility with existing disk controllers, one option involves using a floppy-style track format with Tandon's TM951 tape drive (a). Contrast this with the more conventional layout of the DEC TK-50 tape cartridge with large control word for file marks and byte counts (b).

Half-inch tape drives
(continued from page 29)

Half-Inch Drives for Rigid Disk Backup

	Packaging	Interface	Capacity
Cipher Data M890/M891	10.5-in. reel	ANSI/IBM	23 Mbytes 46 Mbytes
Cipher Data M990/M991	10.5-in. reel	ANSI/IBM GCR format	180 Mbytes
Data Electronics Magnum Tape	Based on quarter-inch cartridge	QIC-02	100 Mbytes
Digital Equipment Maya	4- x 4-in. cartridge	TS-11	100 Mbytes (estimate)
IBM 3480	4- x 5-in. cartridge	IBM 3420 compatible	200 Mbytes
MegaTape MT300	9.8- x 6.4-in. cartridge	Pertec FT8000	330 Mbytes
Memorex 1110	4- x 4-in. cartridge	ESDI	130 Mbytes (estimate)
Rosscomp D160	4-in. reel	QIC-02 SCSI Pertec	160 Mbytes
Tandon TM951	3.5- x 3.5-in. cartridge	SCSI floppy-like	50 Mbytes

although they can only store 46 Mbytes in streaming applications (at 3200 bits/in.). This is because data is written using the ANSI-specified recording format and 9-track interface. Vendors such as Cipher Data Products (San Diego, Calif), Digidata Corp (Jessup, Md), and Pertec Peripherals (Chatsworth, Calif) use cache memories as large as 64 Kbytes to keep the drives in continuous operation, while taking advantage of software drivers that understand only start/stop operations. The same principles apply to Cipher Data Products' Group Coded Recording (GCR) drives. These drives increase capacities on the same size reels to 180 Mbytes (using the 9-track interface at 6250 bits/in.).

IBM's new entry

IBM's Information Systems Group (Rye Brook, NY) has moved to supplement its own model 3420 GCR drive with a cartridge drive storing 200 Mbytes. The model 3480 drive increases recording densities on its 4- x 5-in. cartridge to 38 Kbytes/in. while remaining compatible with device drivers developed for the older drive. A single thin-film head traverses 18 tracks to transfer data at 3 Mbytes/s. Taking a cue from the Cipher Data drives, the IBM drive includes a 512-Kbyte buffer memory to aid streaming operations.

Vendors will either shrink their existing products or attempt to support the newer disk drives on existing systems. Investments in operating systems, application programs, and hardware must be maintained. A case in point is the new DEC tape drive that will use the CompacTape cartridge developed jointly with 3M Corp (Minneapolis, Minn). Although not yet formally announced, the tape drive is intended to back up 5¼-in. disks on the MicroVAX and PDP-11 systems, as well as handle software distribution. Specifications for the drive are expected to be released later this year.

DEC-compatible vendors, however, suspect that the company will follow its past practice of enhancing existing tape interfaces rather than adopting new ones. Therefore, the resultant drive will probably use the TS-11 start/stop interface so that existing software drivers need not be changed. Similar efforts have been made to integrate other half-inch products such as the Control Data Corp (Minneapolis, Minn) streaming drive (TU-80) and Cipher's cache drive (TS-305). In both cases, the basic TS-11 interface was modified
(continued on page 33)

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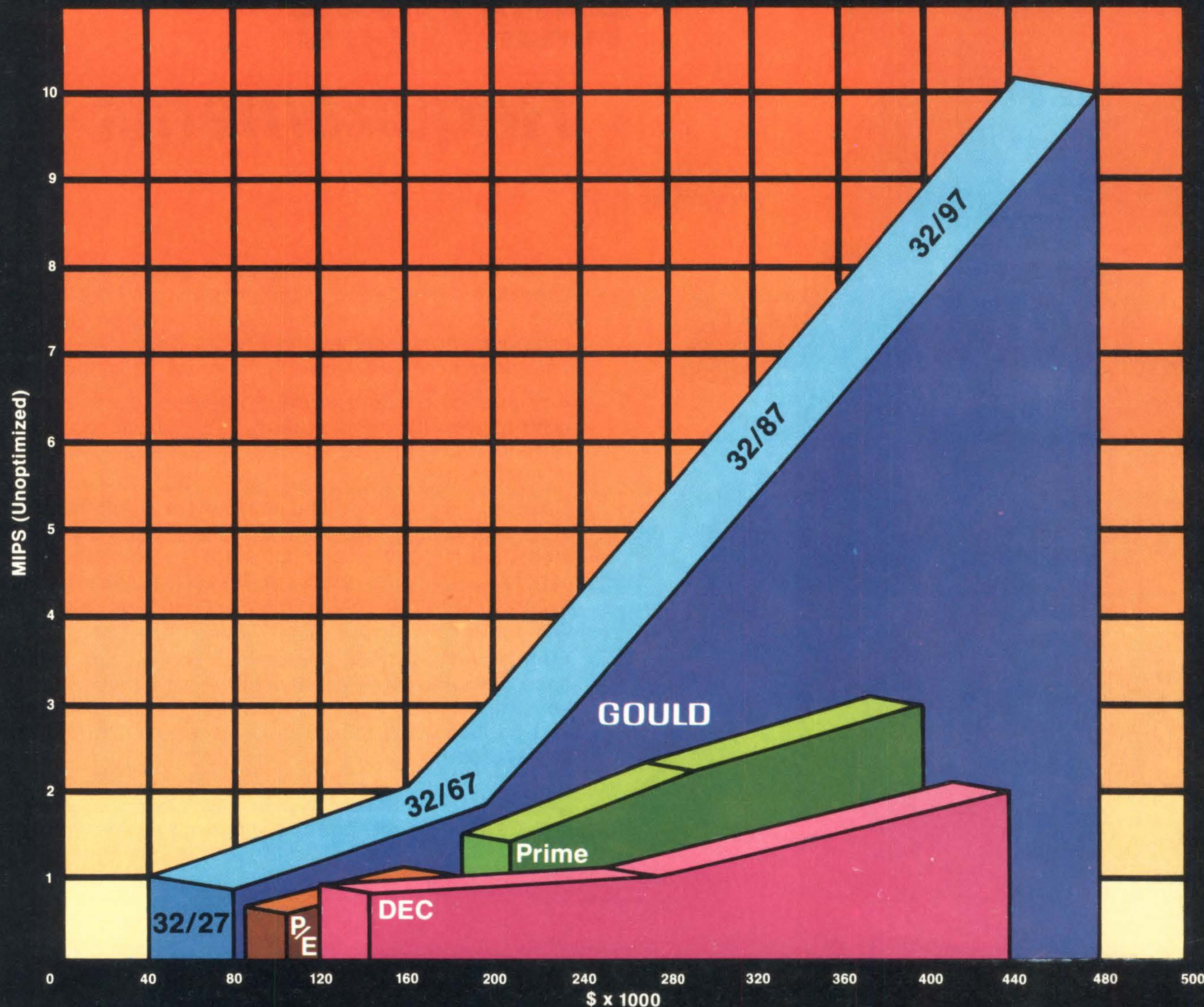

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CIRCLE 18

Half-inch tape drives

(continued from page 30)

for streaming operations. Estimated capacity for the new drive ranges between 100 and 130 Mbytes.

Bringing in the new

Tried-and-true solutions may not work, however, when the rules of the game change. Such is the case with the latest generation of 5¼-and 8-in. rigid disk drives. These drives promise storage capacities of 80 to 160 Mbytes, previously found only on the larger 10.5- and 14-in. drives. Yet, their lower prices make it difficult to justify the expensive controllers built around existing interfaces, such as the Storage Module Drive (SMD).

Likewise, microprocessor-based systems typically do not have the enormous investment in software and hardware to hinder adoption of new device interfaces and tape formats. In fact, Frassel notes that systems such as these obtain optimum performance by fine tuning their controllers and associated software drivers. Since the host processor does not offer the brute horsepower found on large minicomputers and mainframes, the software drivers play a greater role in determining data transfer speeds. Cost pressures also force these vendors to look for software solutions rather than more complex hardware solutions.

By teaching an old dog new tricks, existing specifications for similar tape drives provide readily available interface and recording formats for new half-inch drives. Rosscomp was first to the punch by adapting the QIC-02/QIC-24 interface and widely used format specifications in streaming quarter-inch cartridge drives for use on its 4-in. reel drives. Furthermore, the company claims that these drives can also read tapes written using the 9-track interface and ANSI format. Its controllers understand both interfaces and can easily switch between them.

Also using the QIC-02/QIC-24 interface and format are Data Electronics Inc (San Diego, Calif) and Tandberg Data, Inc (Garden Grove, Calif). They have plans to jointly develop a half-inch cartridge based on the same physical footprint as the ANSI standard X3.55 quarter-inch cartridge in order to provide upward compatibility.

Both the existing quarter-inch and their proposed half-inch cartridges will use the same drive. The primary difference between the two cartridges is that track density will be doubled on the proposed half-inch version. By bringing the 9 tracks called for in the original QIC-02 specifications to 18 tracks, a 100-Mbyte storage capacity can be obtained on the larger cartridge.

A related development focuses on the use of half-inch cartridges storing as much as 500 Mbytes to backup high capacity 14-in. rigid disk drives. Until recently, disk drives having capacities ranging from 500 Mbytes to 1.8 Gbytes were backed up with other drives incorporating removable disk packs, such as the Century Data Systems (Anaheim, Calif) Trident series.

As an alternative, MegaTape Corp (Duarte, Calif) uses a 24-track streaming tape drive to store 330 Mbytes on a dual-reel cartridge (similar to the Data Electronics/Tandberg scheme). Unfortunately, its tape format is unique to its drive, making data interchange to drives from other vendors impossible. The company claims, however, that the tape interface is the same as that used on the Pertec Peripherals FT8000 streaming drive.

Still, the MegaTape drive faces stiff competition from IBM's model 3480. Although its capacity is 50 percent less, the IBM cartridge can be expected to achieve *de facto* standard status for data interchange due to the company's predominant industry position.

Disks to the rescue

Eschewing tape interfaces altogether, two vendors choose popular disk drive interfaces for easier integration. Memorex favors the tape version of the ESDI for the 130-Mbyte drive that resulted from a joint development effort with Electronic Processors Inc (Overland, Kans). Meanwhile, Tandon Corp (Chatsworth, Calif) opts for a floppy-like interface for its 45-Mbyte drive jointly developed

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Half-inch tape drives
(continued from page 33)

with Microtek Storage Corp (San Jose, Calif). The primary benefit of using these interfaces is that they take full advantage of existing disk drive controllers.

The Memorex drive redefines some control signals called for in the original ESDI proposal (see *Computer Design,* Oct 1983, p 32). This allows incorporation of command and status information specific to tape drives. The preliminary track format permits variable-sized inter-record gaps to optimize for either streaming or start/stop operations. In addition, Memorex is considering implementation of the QIC-24 format specification as an alternative to its track format.

Tandon takes the same approach with a floppy-style, 34-pin control bus, but makes some modifications to account for the serial nature of the tape drive. For example, any address marks missed by the read head must cause the device to stop, move back, and then reread the record in the proper direction. Track layout also follows floppy drive practice with sector addresses, fixed-size records, and smaller inter-record gaps.

Tape vendors are also following the lead of their disk drive contemporaries in adopting the Small Computer System Interface (SCSI) as an alternative to both specific tape and disk interfaces (see *Computer Design,* Nov 1983, p 64). Thus, the host computer merely issues generic commands (eg, read or write) and the SCSI controller translates these into commands specific to each device. Jumping on this bandwagon are Rosscomp and Tandon, with Data Electronics also interested but not yet committed.

Prospective users are indeed faced with difficult decisions. No half-inch tape drive meets all needs. When data interchange is important, then the choice is largely limited to drives offering the ANSI/IBM standard format and interface. Drives incorporating the QIC-02/QIC-24 interface and format might provide a second choice, but these specifications are widely used only on quarter-inch drives. Tape backup for the smaller 5¼- and 8-in. disk drives rule out any tape drive using 10.5-in. reels, but that does not substantially limit the number of choices.

The most important criterion may be the capacity of the disk drive itself. It makes little sense to use a 100-Mbyte tape drive if the disk drive handles only 80 Mbytes. Closely matching disk storage requirements with the appropriate tape backup buys the most for the money.

—Joseph Aseo, Field Editor

Computer architectures demand languages that deal with time

Formal mathematical logic has a fatal defect when applied to computers and computing—it has no consistent, rational means of handling the concept of time. The one thing that all computers share, regardless of architecture, is a clock. Even human brains, which are orders of magnitude more complex than man-made computers, are intimately tied to one or more temporal rhythms.

Claims for the superiority of Fifth-Generation languages, such as Prolog, essentially depend on the availability of free computer time on an arbitrarily fast processor. Papers presented at the recent IEEE Compcon in San Francisco indicate that more attention should be paid to time in the design of hardware architectures, operating systems, and computer languages.

The idea of succession (that event "A" happened before event "B") is relatively easy to deal with on a pragmatic level—tying one's shoelaces in the morning would be difficult, otherwise. Formal logic, on the other hand, deals only with the truth or falsity of propositions existing in an ideal abstract universe. Even when constructs for dealing with time and sequence are built within the framework of formal logic, they are clumsy, nonstandard, and, more importantly, not part of the formal logic framework itself.

In realtime applications particularly, programmers spend a lot of time coding and debugging routines that implement timing loops, access or simulate clock hardware, or deal with carefully defined sequences of actions. Consider, for example, a routine to capture and store characters input from a keyboard. In many operating systems, this routine loops until a character appears in a hardware buffer, stores it in memory, and then it goes back to waiting in the loop.

Giving up the concept of time

In his paper "Functional Programming: A Prospectus," Jim des Rivières of the Xerox Palo Alto Research Center states that "...pure functional programming languages have no analogue of assignment statements or side-effect operations (ie, constructs that change the state of the computation)." He further maintains, "Eliminating side effects is tantamount to giving up on the notion of change, and giving up the notion of change sets one free from the concept of time."

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Languages of time

(continued from page 35)

The assignment statement referred to is the high level language equivalent of a machine instruction that stores a particular value in a particular memory location. This is usually implemented in this way by compiler writers. Assignment statements are valuable tools, especially in memory-mapped I/O, where characters sent to or from the device appear in particular memory locations.

Some claim that changing the state of a variable, such as memory location, is a side effect of an otherwise pure mathematical operation, and is therefore somewhat less than legitimate. Side effects and changes of state, however, are quite important to engineers trying to get command strings from a terminal while controlling an industrial process with A-D and D-A converters.

On balance, one of the most common bugs in computer programs is an inadvertent (and erroneous) change made in a variable by a routine that is supposed to be doing something entirely different. This is a true side effect that can be controlled by careful coding practices and by the use of a language such as Modula 2. This language requires the programmer to state explicitly (via the EXPORT and IMPORT commands) which variables can be modified by a given routine.

Dealing with time in the real world

The implementation of data flow processing elements for supercomputers, discussed by Jack B. Dennis of the Massachusetts Institute of Technology's (MIT) laboratory for computer science, requires strict attention to timing. The processing elements are essentially small routines that wait to receive the requisite number of values before performing a computation or otherwise manipulating the data.

The elements then pass results on to other processing elements. Here, timing is crucial. How long it takes to transfer data between the elements and the length of time each takes to manipulate data also represent significant factors. Functional programming concepts and languages are quite valuable in organizing data and computations for execution on parallel processors, and may indeed be the only economical means to do this. Logic programming, in turn, is a good way to deal with large data bases and other problems whose solution is a function of deductive logic—creating or recognizing patterns within a collection of known facts that do not change with time.

When dealing with the real world (eg, realtime operating systems, industrial control, telecommunications, and peripherals), however, the ability to deal explicitly with time and change is vital. The next generation of procedural languages (such as Pascal, C, and Fortran) should include explicit time-sensitive commands. The ability to access a realtime clock (or at least count the "ticks" of the system clock) simply and easily would lighten the workload of both the system and application programmer appreciably. A command such as WAIT (number of time units) is a good minimum. The ability to fetch and use the date and time in a standard format (IF Date >= 28 May 84 THEN. . .) would be even more valuable.

It is therefore as important to write programs dependent on time and change, as it is to write programs independent of time. Each serves a different function along the spectrum of intellectual problems that computers can solve. The point of much of the clamor is that languages structured for handling time dependencies are poorly designed for handling static relationships in artificial intelligence. The converse is also true, and thus both are needed. In addition, given the realities of computer architectures, at least through to 1999, languages that handle time efficiently are necessary to write the compilers and interpreters to execute time-independent languages.

—Sam Basset, Field Editor

SYSTEM TECHNOLOGY
(continued on page 44)

CIRCLE 22

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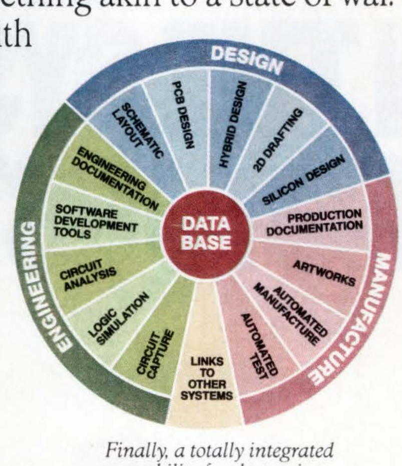

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CIRCLE 24


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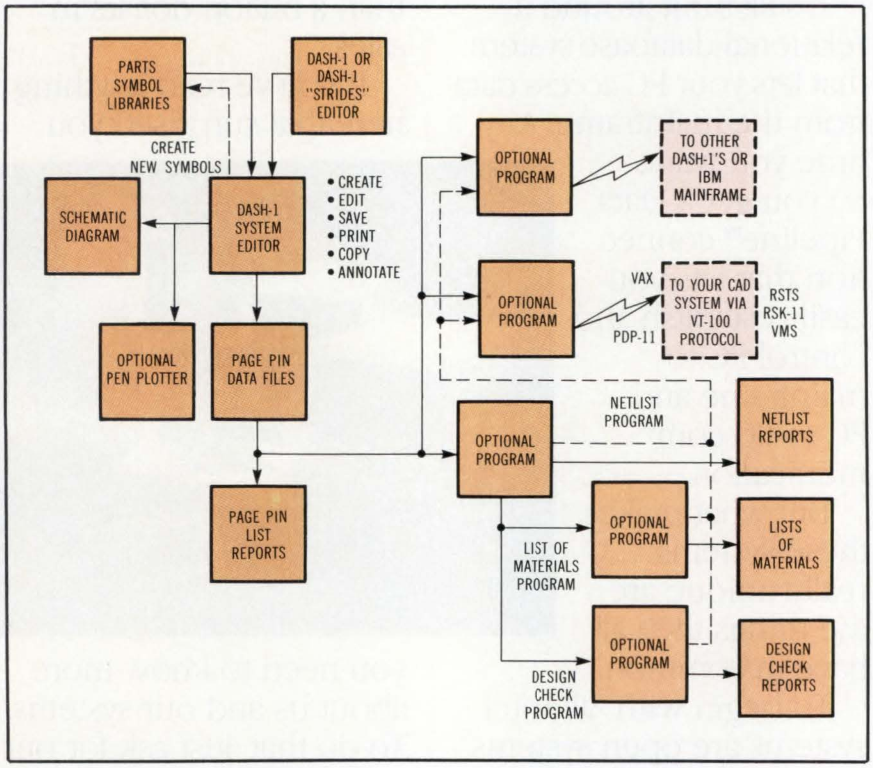
CIRCLE 25

CAD packages convert micros into engineering workstations



Personal computer-based CAD systems like DASH-1 from FutureNet Corp do not limit designers to what can fit on their desktops. Communication packages link the personal computer to mainframe or minicomputers, or to expensive peripherals like plotters and printers. Database extraction also allows list of materials, engineering change orders, and design rule checking to be performed.

Design functions, once the province of mainframes and engineering workstations, now find themselves on engineers' desks. Running on personal computers, software packages can handle both computation-bound operations (eg, logic and circuit simulation), as well as interactive tasks (eg, schematic entry and circuit routing).

Faster user response time is the key advantage that personal computers offer over their more expensive counterparts. Although the raw processing power of personal computers may be one-tenth to one-fifth of that supplied by minicomputers, all processor and peripheral resources are dedicated to a single user rather than allocated on a time shared basis to several users. Furthermore, the user response time on personal computers is the same as the time needed to execute the program.

Such is not the case when computer aided design (CAD) applications run on larger computers. In fact, several CAD vendors for personal computers note that it is not unusual in engineering departments for as many as 10 to 15 users to share a single scientific computer such as a Digital Equipment Corp VAX-11/780. Thus, the faster processing speeds are counterbalanced with longer user response times (as much as one hour for circuit simulation).

The same holds true for engineering workstations. Although they may use the same microprocessors found in personal computers, engineering workstations augment these with special purpose hardware (eg, memory management and floating point support). Since the added hardware makes them more expensive, a large number of engineering departments cannot justify allocating $35,000 or more to have a workstation for every engineer. Often, three or four engineers must share a single workstation. Thus, there exists a similar situation with long user response times (ie, waiting for your turn on the machine).

Right size for the job

In contrast, personal computers outfitted with the necessary design tools (eg, schematic editing and logic simulation) can be bought for less than $15,000, according to Roy Prasad, product manager for Personal CAD Inc (Los Gatos, Calif). He admits that the software packages designed for personal computers are less powerful than similar tools on larger computers. These packages support fewer nodes in simulation and handle smaller data bases for schematic entry. On the other hand, he points out that engineers rarely use the full capabilities of the large systems.

In fact, some tasks are more suitable for personal computers than multi-user hosts. For example, the highly interactive nature of schematic editing makes it difficult to use CAD packages (eg, SCICARDS) that run on larger machines through timesharing. Editing packages such as CAD 2000, from Chancellor Computer Corp (Mountain View, Calif); Design Automation, from Dasoft Design Systems (Berkeley, Calif); DASH-1, from FutureNet (Canoga Park, Calif); and PC-CAPS, from Personal CAD, support hierarchical structuring of logic design so that large projects can be effectively partitioned into as many as 50 different levels of detail (99 levels for DASH-1). Net lists and component values can be extracted for use as input to logic and circuit simulators, such as Tegas and Spice,

(continued on page 46)

Engineering workstations
(continued from page 44)

Schematic Editors	Personal Computers Supported	Graphics Resolution Required	Circuit Routing
Chancellor Computer Corp	IBM PC	1024 x 768 pixels 640 x 400 pixels	yes
Dasoft Design Automation	Apple II Kaypro North Star Advantage	80 x 24 cols	yes
FutureNet DASH-1	IBM PC	640 x 400 pixels	maybe (simple circuits)
Personal CAD PC-CAPS	IBM PC	320 x 200 pixels	yes

or sent to larger CAD systems, such as Applicon and Gerber, for generation of artwork or circuit layout.

Are pretty pictures needed?

In addition to schematic editing, Chancellor Computer, Dasoft Design Systems, and Personal CAD also support manual routing of printed circuit boards as well as the generation of finished artwork. However, disagreements arise concerning the minimum graphics resolution needed to route complex circuit boards.

On one hand, Chancellor Computer provides the high resolution found on more expensive CAD systems (1024 x 768 pixels on the CAD 2000) as well as the 640- x 400-pixel resolution found on many IBM PCs. Likewise, FutureNet uses the 640- x 400-pixel resolution for its schematic editor. Terry Smith, product manager with Chancellor Computer, feels that this is the minimum resolution required to accurately place pad and drill masters, trace layers, ground and power planes, and the final silk screens.

However, higher resolution exacts a higher price. For example, Chancellor Computer's high resolution system costs $10,000 more than its 640- x 400-pixel version, or about $23,500. The higher price is due to the special graphics card with its own dedicated graphics processor.

Many potential users cannot afford that premium and do not need to pay it anyway, Prasad says. He notes that the PC-CARDS routing package requires only a 320- x 200-pixel resolution (the standard resolution on IBM PC systems, but has the potential to handle printed circuit boards that approach 60 x 60 in. (25 mil grid size). Similarly, the Dasoft routing package needs no special graphics terminal, but uses any 80-col x 24-row cursor terminal for graphics editing. Line-drawing primitives on such terminals provide finer onscreen editing.

Without the pretty pictures, both systems provide the necessary ability to generate the artwork because the graphics resolution of the screen has little to do with the resolution of the hard copy generated on a plotter. Prasad notes that lines and curves displayed on a raster screen are still made up of distinct points, no matter how fine the graphics resolution. On the other hand, plotters generate solid lines and curves. In fact, all graphics packages must eventually convert the bit maps used in graphics editing to vector endpoints understood by plotters.

Small scale simulation

Beyond graphics editing, personal computers can make a more significant contribution to an engineer's productivity through logic and circuit simulation. According to several knowledgeable sources, fewer than 10 percent of circuit and logic designers currently use simulation tools. Prior to the advent of personal computer-based tools, simulators (eg, Tegas and Spice) were the province of large mainframe and minicomputers with associated costs easily exceeding $150,000. Those who had access to such systems often encountered "loopback" times (the amount of time spent waiting for the final computations) exceeding several hours.

Although the processing power of personal computers is a fraction of that found on larger machines, they do supply the user with a response immediately after the completion of computations. As a result, computations for either integer-based digital simulation or floating point analog simulations can take several minutes on personal computers and still offer superior response times compared to those offered by mainframe or minicomputers.

(continued on page 48)

Simulators for Personal Computers	Personal Computers	Type of Simulation	No. of Nodes
Blume Engineering PSpice	IBM PC	analog circuits	120 MOS or 140 bipolar transistors
E/Z CAD Logicorp	IBM PC any CP/M machine	logic	3000 (9-state)
Personal CAD PC-Logs	IBM PC	logic	5000 (12-state)
Spectrum Software MicroCAP	Apple II IBM PC	circuit	40
Spectrum Software MicroLogic	Apple II IBM PC	logic	1750 (5-state)

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CIRCLE 26

Engineering workstations
(continued from page 46)

However, maximum physical memory sizes (eg, 768 Kbytes on the IBM PC) limit the size of nets that can be simulated, with logic simulation much simpler to implement than circuit simulation. For example, Logicorp from E/Z CAD Inc (San Jose, Calif) supports nine-state logic simulation for 3000 nodes on CP/M systems with 64 Kbytes of RAM. On the other hand, the MicroCAPS circuit simulator from Spectrum Software (Sunnyvale, Calif) supports just 40 nodes. The smaller net sizes for circuit simulation result from the larger number of parameters involved in comparison to logic simulation, says Andrew Thompson, president of Spectrum Software.

The smaller net size does not necessarily mean that such tools are less powerful than their mainframe counterparts. Thompson points out that designers often break down large logic designs or circuits into smaller partitions in order to analyze the results. Thompson estimates that the typical engineer breaks up circuit simulations to around 40 nodes, while logic simulations are best managed at about 2000 nodes. Accuracy does not suffer because logic and digital circuit simulations use integer data bases, easily handled by personal computers such as the Apple II or IBM PC.

Some questions remain concerning analog circuit simulation because it requires floating point (typically single-precision) arithmetic. Vendors such as FutureNet and Chancellor Computer feel such computation-bound tasks are best handled by mainframe computers. As such, they provide the necessary interfaces (including netlist reformatting) to popular circuit simulators such as Spice. However, even mainframe-style simulators are being ported to personal computers. Blume Engineering (Irving, Calif) provides the PSpice circuit simulator, which supports as many as 120 MOS or 140 bipolar transistors. The simulator needs an IBM PC with 512 Kbytes of RAM and an 8087 floating point processor, but executes at about one-fifth the speed of the VAX-11 version.

Future prospects

There are limitations to the current generation of personal computer-based CAD tools. The graphics editors cannot handle VLSI circuit layouts (although both FutureNet and Chancellor Computer claim to support standard cells and gate arrays), or support automatic place and routing. Other computation-bound tasks that are beyond the scope of current tools include fault simulation and test vector generation. However, Prasad predicts that tools capable of these tasks will come into being with the wide availability of 256-Kbit dynamic RAMs and advanced 16-bit processors. Performance increases in the range of three to four times are thus possible.

For those who cannot wait, the current generation of CAD tools provides a cost-effective alternative to minicomputer-based CAD systems or engineering workstations if used in a standalone fashion. Increased productivity can also be gained by combining personal computer systems handling graphics editing and small scale simulations with larger machines performing computation-bound tasks and final system integration. In this case, designers benefit from the best of both worlds.

Joseph Aseo, Field Editor

SYSTEM TECHNOLOGY
(continued on page 56)

June Previews
Watch for two special articles—local area networks on June 1, system testing on June 15

 CIRCLE 27

Floating Point Systems array processor to break

The FPS-5000 Series from Floating Point Systems

Now, a new family of products from Floating Point Systems brings increased computing power and unmatched price/performance to the signal/image processing world.

With 3 to 6 times the speed and 4 times the memory capacity of previous FPS products, the FPS-5000 Series provides computing for applications that exceed their present system's capability.

The FPS-5000 Series offers fast, accurate, flexible computing for the most demanding real-time, user-interactive, and production-oriented applications.

Four basic product groups make up the new FPS-5000 Series: the 5100, 5200, 5300 and 5400. Peak performances range from 26 million floating-point operations per second (MFLOP), to 62 MFLOP. Data memory of 0.5M to 1M words is available along with program memory to 32K words.

By combining a distributed architecture concept with the latest VLSI technology, the FPS-5000 Series sets a new standard for cost-effective computing, breaking the $2,000 per MFLOP* barrier—the first time this has been achieved in any floating-point computing system.

*Based on U.S. Domestic Prices

Typical performance examples of geophysical, medical imaging and signal / image processing applications.

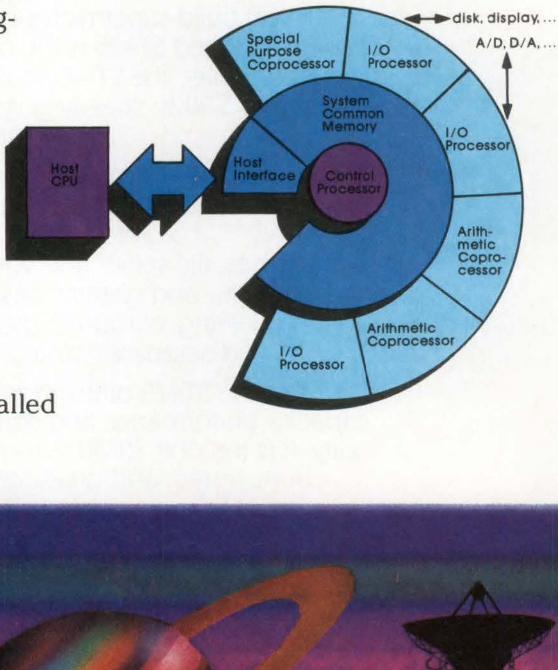
Application Example	AP-120B	FPS-5410	5420	5430
1. Demodulation / Signal Analysis	13.8 msec.	6.5 msec.	N/A	N/A
2. Tomography Preprocessing	60 sec.	25 sec.	16 sec.	12 sec.
3. Multispectral Image Classification (512 x 512 pixels 8 Bands, 4 classes)	49 sec.	25 sec.	13.3 sec.	10.5 sec.
4. 2D FFT (512 x 512 complex)	3.4 sec.	1.4 sec.	.7 sec.	.5 sec.
5. Matrix Multiply (100 x 100)	439 msec.	177 msec.	96 msec.	71 msec.

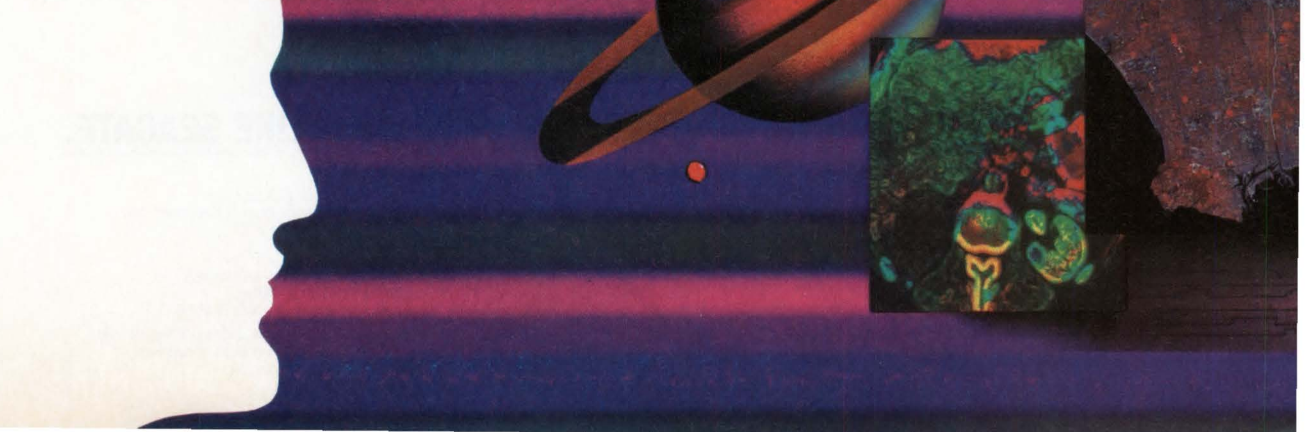
Based upon specifications subject to change.

Distributed processing architecture

The FPS-5000 Series is a distributed processing system that maximizes throughput by allocating the computational load to a set of high-performance, independent, floating-point processing elements called Arithmetic Coprocessors. Data flow is simultaneously managed

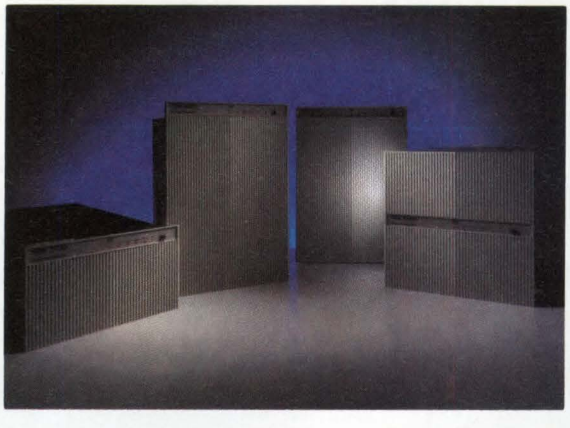
FPS-5000 Series Architecture





introduces the first the $2,000/MFLOP barrier.

by a combination of independent I/O Processors and the central Control Processor.



Each Arithmetic Coprocessor, with synchronous architecture to allow simple application debugging, functions as a self-contained unit.

The new Multiple Array Processor Execution Language (MAXL), based upon FORTRAN 77, allows the user to construct an integrated system environment which can be tuned to application requirements.

Increased performance can be achieved by adding Arithmetic Coprocessors as a field-installable upgrade as the user's requirements evolve.

Compatibility

The FPS-5000 Series maintains software compatibility with previous FPS 38-bit processors and is supported on a range of host computers. Thus, the extensive software support developed for FPS-100 and AP-120B products is maintained and users are able to move existing applications onto the FPS-5000 Series with minimal effort.

Quality and Reliability

The FPS-5000 Series was designed and built with the same quality standards inherent in all of the previous Floating Point Systems products—standards that have earned those products a reputation for unprecedented reliability and one of the best meantime between failure (MTBF) rates in the industry.

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For more information about how the FPS-5000 can be used in your specific application, call (800) 547-1445 or your local sales office.

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CIRCLE 29

HOW TO CHOOSE A DISK DRIVE, PART II:

Computers designed for the office environment are in for a shock!

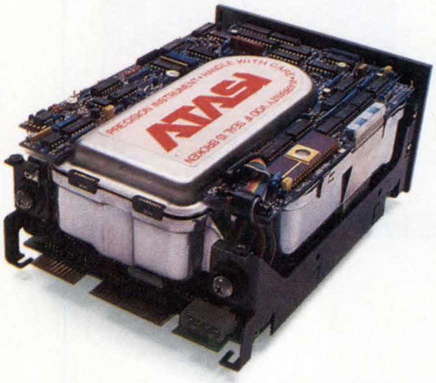
Here's a shocking fact: when someone sets a computer down on a desk, the disk drive inside can be subjected to a pulse shock as high as 30 g's. Obviously, if the disk drive (or any other component in your system) can't handle that kind of shock, your system runs the risk of breaking down under rather ordinary conditions—like every time there's an office shuffle and people move their computers. What follows is some technical information on how we handle the problem in our high performance 5¼-inch Winchester disk drives.

Shock and vibration: twin problems

Shock, and the closely related problem of vibration, have come under intense study at ATASI Corporation, and for good reason: both can cause loss of data. A severe pulse shock can cause a

AN ENVIRONMENTAL IMPACT REPORT.

drive's head to "slap" against the disk, removing a "divot" of oxide material, along with the data written there. Severe vibration can cause the head to overshoot or undershoot a track, so that the head can't find the data it's seeking. In addition, vibration can fatigue components over time, and perhaps lead to premature failure.

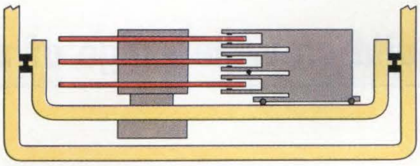


ATASI's 46 Mbyte, 5¼-inch Winchester disk drives are available in production quantities immediately.

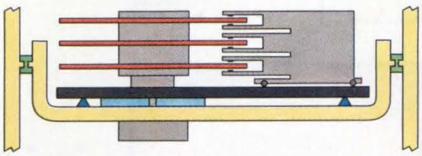
Double shock isolation

In order to sustain high shock loads, the ATASI design incorporates a unique dual system for shock and vibration isolation. Like most disk drives, ATASI drives have isolators between the frame and the head/disk assembly bowl. In addition, ATASI's proprietary design includes elastomere isolators inside the bowl, between the bowl and baseplate on which the head/disk assembly is mounted. A foam pad with high damping properties, also located between the baseplate and the bowl, further protects the head/disk assembly from vibration.

The grommets ATASI uses for isolators are far from ordinary. To handle both pulse shocks and vibration effectively—to avoid a declining spring rate with displacement while maintaining adequate damping properties—ATASI tested 330 different options before



Most disk drives only have shock and vibration grommets (black) between the frame and the bowl.



ATASI's proprietary design also includes isolators (blue) between the bowl and baseplate.

making a choice. These tests involved the use of a laboratory shaker as well as computer models.

ATASI's double isolation system more than protects its drives—and the data they store—from the shocks of the office environment.

Beyond the shock/vibration problem

Shock and vibration engineering is only one of a number of ways ATASI achieves such a high level of data integrity. ATASI drives also feature dedicated "landing zones." Upon powerdown—intentional or emergency—the back e.m.f. of the motor is used to position the carriage over data-free landing zones. A carriage lock then mechanically holds the carriage in place, protecting the data field from any head contact.

The ATASI White Paper

At ATASI, we are proud of the quality we build into every drive we make, and we encourage clients to test our products rigorously. To help, we have prepared a White Paper on shock and vibration for systems integrators. It discusses test methods and the interpretation of test data in detail.

If you are a systems integrator, contact ATASI Corporation now to receive your ATASI White Paper. Corporate headquarters: 2075 Zanker Road, San Jose, CA 95131, (408) 995-0335; Eastern region: (617) 890-3890; Southwest region: (714) 432-0757.

PERFORMANCE SPECIFICATIONS

MODEL NO.	3033	3046
CAPACITY	33 MB	46 MB
ACCESS TIME (AVG.)	30 ms	30 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

Available in high volume today.

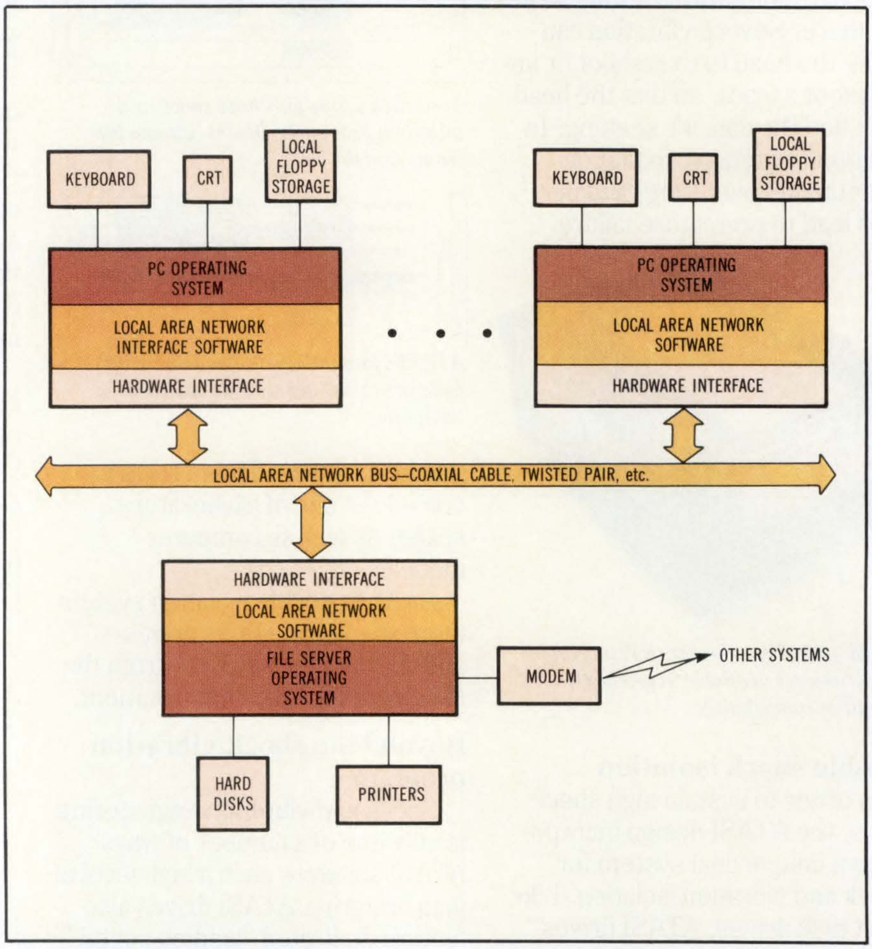
MODEL NO.	3065	3075
CAPACITY	65 MB	75 MB
ACCESS TIME (AVG.)	24 ms	24 ms
DATA RATE	5 Mbits	5 Mbits
INTERFACE	ST 506	ST 506

Available second half, 1984.

ATASI

Forthcoming PC networks build on wide range of approaches

Although distributed processing has been the subject of much discussion over the last several years, it is just now becoming reality. Propelled by the advent of the IBM PC and its potential as a genius-level terminal for mainframe computers, many hardware and software products have been developed to interconnect PCs with each other, and with other systems. Products that handle these interconnections vary from an almost transparent implementation of the Ethernet protocol on twisted-pair lines, to a standalone program that communicates via a modem.



In a general bus-oriented net, such as 10-Net or NetWare, individual PCs transfer files over a bus via a combination of hardware and software. One or more stations can serve as file or print servers.

Transparent interconnection

Using the Seeq Technology Ethernet protocol chip on a plug-in peripheral board for the PC bus, 10-Net from Fox Research (Dayton, Ohio) implements Level 2 of the IEEE 802.3 standard. The protocol uses a Carrier Sense Multiple Access/Collision Avoidance (CSMA/CA) scheme to pass packet data at up to 1 Mbits/s over twisted-pair wires.

In addition to a peripheral card, the hardware consists of a three-wire (two signal and one ground) lead-in cable and an interface box. Connection to the net is simple. An electrical connection is made to the twisted pair, and the bottom cover is replaced on the box. Then, the lead-in cable is plugged into a socket, the card is plugged into the PC, the power is turned on, a configuration program is run, and a log-in program is executed. The log-in can be made part of the boot process every time the PC is powered up.

The supplied software is a generic modification of MS-DOS 2.0. There are no IBM PC-specific routines to keep it from running on any of the PC clones. At log-in time, and each time a net access is made to a "new" (not recently accessed) node, the system queries the net to determine which nodes are active. It then builds a table of node names. In effect, the file system of each PC or clone becomes a node in a shared root directory.

Each node is given a name (eg, "Fred" or "Accounting") at configuration time. This name is used by other nodes to access its files or devices over the network. Any node can access any hardware device on any node in the net, and no dedicated print, file, or communication server is needed.

A full complement of network management facilities are provided, including insertion and deletion in shared files; user, file, and node ID security; concurrency control; and an activity audit trail. In addition, the system provides electronic mail, an electronic bulletin board, a calendar, two-party chat, multiparty CB, online communications, remote job submission, and print spooling.

The 10-Net costs approximately $700 per PC (excluding twisted-pair cable, which must be bought separately). It runs on any IBM PC or clone, requires 64-Kbyte RAM, one or more disk drives, and MS-DOS 2.0.

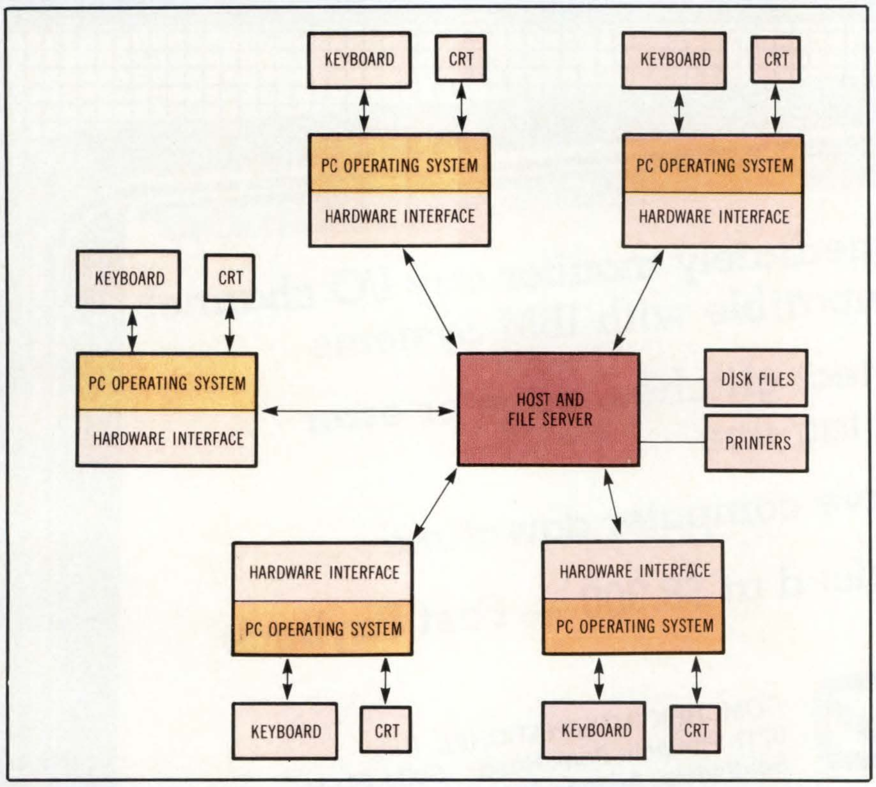
Software with optional boxes

At a slightly less transparent level, NetWare/OS, from Novell, Inc (Orem, Utah), replaces the file-handling apparatus of the PC with a sophisticated file server. Tailored to support varieties of PC-DOS, MS-DOS, CP/M-80, CP/M-86, and the UCSD p-System, it uses any of a number of network hardware systems. One of these is manufactured by the company to share files between PCs.

Based on what the company calls its Universal File Server, the operating system features ease of use through simple function utilities and extensive help files. One of these utilities allows disk storage on

(continued on page 58)

Networking PCs
(continued from page 56)



In a star network, such as Spectrum 700, each PC communicates with a central host. The host then mediates all file and message transfers and acts as the central file and print server.

any PC to be segmented in various ways. Areas on disk can be allocated to different users or different operating systems, and still remain transparent to all users on the system, within limits. A log-on password lets a user have access to specified files in the shared portions of the network's disk systems.

Multi-user file security lets the owner define which files will be available publicly, and which will be private. File and record locking, electronic mail, and print spooling are also provided. The operating system maintains duplicate file directories and utilities to recover erased or lost files, and to provide a modest level of fault-tolerance.

Physical connections to Corvus's Omninet, 3Com's EtherLink, Gateways's G-Net, Proteon's proNET, the Arcnet of Nestar, and Novell's own NetWare/S, are provided through peripheral cards that plug into an expansion slot on the PC. Generally, one PC on the network acts as the central file and print server, handling requests from other nodes. Along with special hardware arrangements (usually a PROM on the peripheral card), this allows most of the PCs in the network to operate without local storage (their own disk drives), lowering the system cost.

Novell's NetWare/S is a self-contained computer with a Motorola 68000 CPU. It connects with the various PCs via twisted-pair cables, and manages up to 300 Mbytes of mass storage and five shared printers. Disk caching, directory hashing, and seek optimization all help to speed file system throughput. Price varies according to the number and kind of options selected.

Software with its own box and net

A specialized network server with application-generating software is available from Science Dynamics (Torrance, Calif). Called Spectrum 700/Magix, the file server (the Spectrum 700 part of the name) is Multibus-based, and communicates with the PC workstations via either an Ethernet-type link, or RS-232/422.

The server is built from standard Intel single-board computers and Multibus peripheral boards. A wide range of disk, tape, and printer interfaces is available from numerous vendors. Since the file server handles all file requests, the PC workstations can operate without disk drives.

The system is relatively expensive and has a high capacity. Without the Magix software (database and application generators), as well as an MS-DOS support gateway, it would qualify as a separate computer system, rather than as a PC enhancement. The basic philosophy of the system is closer to traditional mainframe and minicomputer systems than it is to common PC applications.

The Magix software consists of several parts. A database compiler written in C, for example, accepts English-like language and produces tables and interpretable instructions for the other modules. A format definer lets the user create or change the way reports are presented. A user presenter manages entry, display, and updating the workstation screen, as well as printing via a PC printer. And, a database server creates, maintains, and updates the data bases on the system.

Since it is an 8086-based system, the Spectrum 700 can load a copy of MS-DOS, and run generic application programs. This facility is useful and supplements a system that has been created to appeal to vendors of turnkey vertical applications.

Software and a serial port

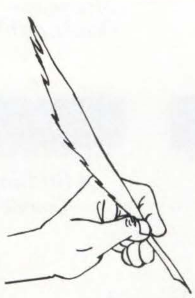
The least transparent of the PC communication schemes is Blocked Asynchronous Transmission (BLAST) from Communications Research Group, Inc (Baton Rouge, La). It allows 8- and 16-bit PCs to communicate with each other, or with minis or mainframes that have the same software.

Standard RS-232 ports are used to drive modems over the telephone lines, or to connect two systems directly. The program reads files and converts them to collections of ASCII printable characters. Then, it sends them over the link one packet at a time with error-checking and ACK/NAK handshaking protocols.

The approach does not differ significantly from several public domain programs available free from PC user's groups. It is a standalone program, which means that the user must quit an application program (eg, a word processor), load and run BLAST, send and receive files, then reload the application and continue.

Thus, BLAST is not transparent and cannot be used from inside an application program, unlike the 10-Net or the Novell system. On the other hand, the company has gone to great lengths to support the program on a wide variety of computer and operating systems. Prices vary from $250 for microcomputers to $850 and up for mainframes.

—Sam Bassett, Field Editor



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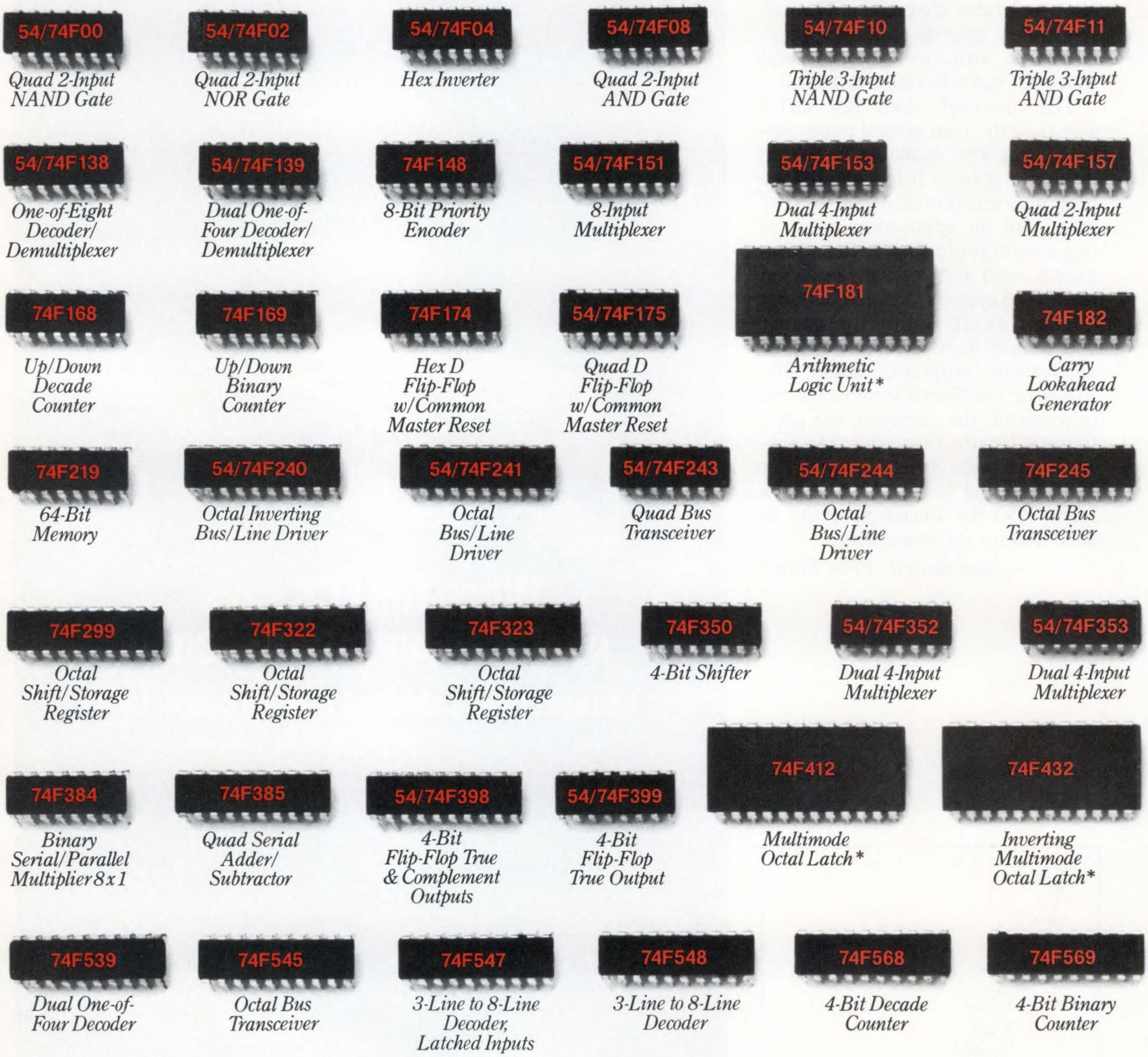

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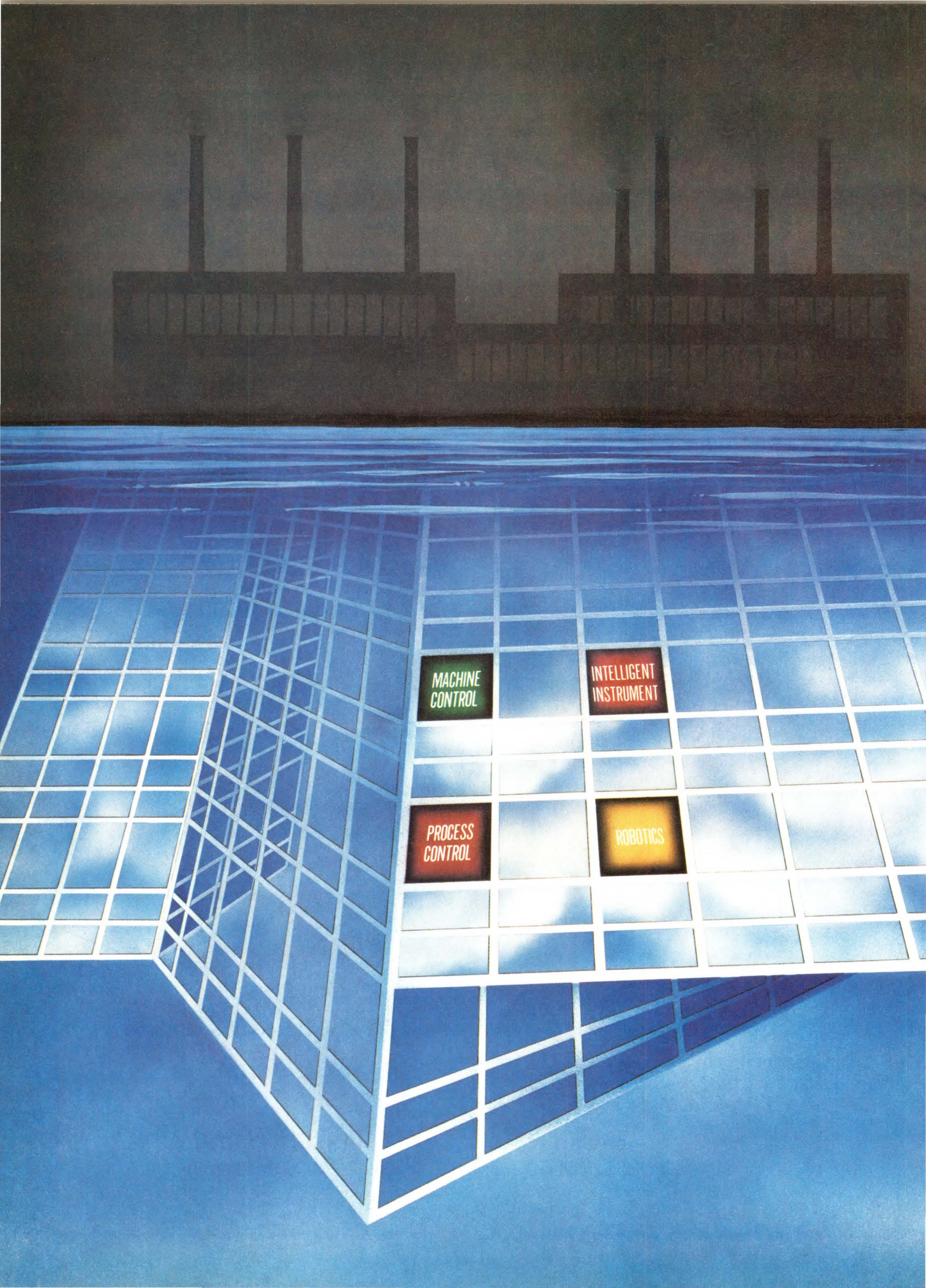
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Society for Information Display International Symposium

San Francisco Hilton, San Francisco, California June 4 to 8, 1984

Each year, the Society for Information Display closely examines up-and-coming display technology. The June conference will be for those who want to identify the best potential subsystem, and for those who want to design that subsystem from the ground up. In the process of monitoring the latest issues in international display research, SID '84 may just pinpoint a few familiars whose refinements will tempt once-shy designers. At the top of the list that designers may want to check twice is the flat-panel display—be it electroluminescent, plasma, or LCD.

In all, 88 contributed papers will examine display research, device characterization, fabrication, and system integration. In conjunction with the technical presentations will be a series of informal author interviews and evening panel debates. Besides the technical program and exhibition, which run Tuesday to Thursday, the conference will conduct background tutorial seminars on Monday and Friday.

Active flat panels slip into CRT niches

Electroluminescent and plasma display panels are beginning to vie for positions in all kinds of computer systems. In fact, these active flat panels may soon edge out CRTs in many industrial and office designs. That is over and above the emerging applications where the flat panels may be preferred from the start for size, if not performance or aesthetics. A recent Frost & Sullivan (New York, NY) study projects that within the next 10 years, flat panels will take over in 60 percent of display applications.

Each in its own way, electroluminescent and plasma displays are busy limbering up their operating characteristics and clamping down on expensive driver electronics that have skewed their price/performance ratios in the past. Electronics research is also driving high voltage technology at lower power, and as a result, is reviving thin-film approaches. As this year's technical presentations will show, plasma is still ahead of electroluminescence in color work. Color plasma is now in prototype, whereas electroluminescent models are busy refining the gray-scale performance fundamental to their future color development.

Dramatic reductions in driver electronics are also allowing electroluminescent and plasma flat panels to be larger and leaner. To that end, Supertex Inc (Sunnyvale, Calif) is spearheading the next round of development; its monolithic 64-channel driver ICs add little size to the display panel. Moreover, these drivers are implemented in DMOS, so they can handle higher voltages than electroluminescence could weather before.

Using the Supertex chips, developers at Lohja Corp (Lohja, Finland) have achieved a full gray-scale, 256- x 512-graphic ac thin-film module. The entire panel measures 140 x 260 x 9.5 mm, including all interface ICs and driver electronics. In addition, Hycom Inc (Irvine, Calif) will describe its 512 x 640, 4-line/mm thin-film electroluminescent display, which is also driven by high voltage ICs. This multiplexed display operates at 90 Hz and shows realtime television signals in 16 shades of gray.

Price aside, because these displays traditionally require a driver for every row and every column of resolution, development of large plasma screens at high resolution has been complicated, as well as bulky. Recently, several techniques to simplify driver electronics have emerged to get around that problem. Fujitsu, Ltd (Akashi, Japan) will introduce one technique, which creates a logically addressable, surface discharge ac plasma display. Intrinsic logic structure separates the writing electrode from the sustaining electrodes.

Another effort to reduce the number of driver connections was detailed by Plasma Graphics Corp (Plainfield, NJ) at last year's SID. A new product this year, the hybrid ac-dc plasma display reduces the number of driver-to-panel interconnections by combining memory self-scan with a multiplexing technique (see p 244 of this issue). This year, the company will examine new operating techniques that widen the dimming range of display brightness and improve memory margins.

High voltage plasma display drivers combining DMOS and CMOS technologies will be the subject of a Thomson-CSF (Saint-Egrève, France) presentation. Their 100-V ICs are geared to large, militarized panels displaying over 10^6 pixels. Also, NEC Corp (Kawasaki, Japan) will unveil high speed, high voltage CMOS circuits driving a 256 x 512 ac-refresh plasma panel. Together with an unbalanced-voltage driving method, the circuits substantially reduce power consumption. This improves the driving

(continued on page 66)

(continued from page 65)

frequency and, consequently, the luminance. At 1 MHz, the 102- x 205-mm2 panel consumes less than 10 W.

Several talks will sketch advances in color plasma panels. Hitachi, Ltd (Tokyo, Japan) speakers will describe an 8-in., 120- x 160-element color memory display demonstrating 2-lm/W white luminous efficacy. Another 8-in. plasma panel, with 126 x 160 color cells, is coming out of NHK Technical Research Labs (Tokyo, Japan). This one features a driving method that provides internal memory by using repetitive pulse discharges. It shows color television pictures with 256 intensity levels, 40-ft-L peak area luminance, and 0.34-lm/W luminous efficacy.

Nonemissive flat displays perk up

Of the passive flat panels, LCDs show the most potential for computer system display applications. In fact, some are saying that the LCD may yet learn to run in the field of interactive displays. Research is harvesting liquid crystal materials with better electrical characteristics to improve response times and better dyes to improve contrast, viewing angle, and color.

Already, low power consumption and good contrast make the LCD viable for portable applications. Up to now, however, operational drawbacks—among them slow response time and need for an external light source—have been major obstacles. A session on active matrix displays will track the progress of several thin-film transistor drivers, which are presently looked to for improved multiplexing. Hosiden Electronics Co, Ltd (Osaka, Japan) will describe the largest LCD panel so far: a 7.23-in diagonal with 325 x 108 tricolored pixels addressed by a-Si thin film transistors. PolySi thin-film transistors will be active in LCD presentations by Toshiba R&D Center (Kawasaki, Japan) and Suwa Seikosha Co, Ltd (Suwa, Japan).

Toshiba's 240- x 360-element, active matrix display uses integrated gate-bus drivers that consist of two 180-bit static shift registers and buffer amplifiers. Suwa Seikosha will detail two displays that each come in black and white or full color. The larger, 480- x 480-pixel panel is addressed by external drivers, while the smaller, 180- x 210-pixel panel has integrated drivers.

Fine-tuned CRTs sight 3-D and simulation

When it comes to fast response, ultrahigh resolution, unparalleled brightness, and color, the CRT is still the best of show. Shortly, monochrome flat panels will win out in some emerging display markets. In fact, they already threaten to take over many display systems that the CRT has monopolized. However, when flat-out performance and price are the criteria, the venerable CRT will beat all comers for a while yet. Only the so-called flat CRTs (or hybrids putting dc plasma into a CRT framework) may outstrip the familiar monitor for advanced applications such as 3-D and simulation.

At the high end, researchers at Tektronix, Inc (Beaverton, Ore) will take the wraps off a 19-in., 90-degree raster-scan monitor that displays three million pixels. The 1500 x 2000 terminal features a low-capacitance grid that generates a full gray scale. Moreover, astigmatism and focus-control grids dynamically correct for electron beam aberrations and deflection defocus. Another 19-in. superhigh resolution graphics monitor will be introduced by Hazeltine Corp (Greenlawn, NY). This color display can generate 0.1-in. high alphanumeric characters in seven colors over its entire screen area. It has 0.015-in. spot size and 0.012 maximum misconvergence.

Toshiba Corp (Fukaya, Japan) scientists will describe a 15-in. square color display tube that achieves white luminance of 160-ft-L and vertical dynamic convergence. Meanwhile, Hughes Aircraft Co (Carlsbad, Calif) speakers will examine how processing fine-grain P-42 phosphor can yield a miniature CRT with 3000-ft-L brightness.

A session devoted to simulation and display will detail how to take high-toned CRT monitors a step further. Scientists from Evans & Sutherland Computer Corp (Salt Lake City, Utah) will describe a microprocessor-based projector display system with the optical feedback to self-align hue, intensity, convergence, geometry, and focus. The system detects and corrects geometry drifts to within one-quarter of a pixel, and projection distortions to 30 percent.

In addition, a programmable low cost hybrid display processor for man-in-the-loop simulation will be described by representatives from Systems Technology, Inc (Hawthorne, Calif). Their digital-to-analog calligraphic display processor transforms a data base into instrument formats and perspective out-the-window scenes at a rate of 8000 vectors/s, with throughput delay of less than 40 ms.

Stereoscopic image display will be the subject of a Bright & Morning Star Co (Lawndale, Calif) presentation. Speakers will explain a system based on total internal reflection, which separates and directs the observer's converging lines of sight toward two discrete images. This system is said to simultaneously display stereo information from most imaging systems.

—Deb Highberger, Senior Associate Editor

For registration information, contact Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

(Conference coverage continued on page 68)

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(Conference coverage continued from page 66)

Technical Program Excerpts*

Session 4: DC Electroluminescent and LED Displays

Tues 2 to 4:15 pm, Continental 4

Chair: M. R. Johnson, Texas Instruments, Inc, Dallas, Tex

4/1 "A 2000-character dc EL Display"
J. W. Mayo, P. Hutchinson, R. Hayes, and R. Ellis, Phosphor Products Co, Ltd, Poole, England

4/2 "Stabilization of dc EL in ZnS:Mn Thin Films"
A. Vecht, Thames Polytechnic, London, England; and S. Chadha, Lucas Electricals, London, England

4/3 "High Contrast Thin-film/Powder Composite dc EL Devices"
M. H. Higton, Phosphor Products Co, Ltd, Poole, England

4/4 "Performance of ZnS_xSe_{1-x} dc and ac TFEL Devices"
D. Cammack, R. Dalby, D. Walz, and R. Bhargava, Philips Labs, Briarcliff Manor, NY

4/5 "High-Resolution LED Matrix Displays"
P. K. Kimber, S. C. M. Day, and G. White, GEC Research Labs, Chelmsford, England

Session 5: Large-screen Displays

Tues 2 to 3:20 pm, Continental 5

Chair: L. T. Todd, Jr, Projectron/Data Beam, Lexington, Ky

5/1 "Glass Browning in Projection CRTs"
A. Rengan, Zenith Radio Corp, Melrose Park, Ill

5/2 "A New Electrostatic Lens Designed for Projection CRTs"
M. Kikuchi, Y. Kobori, and T. Saito, Sony Corp, Tokyo, Japan

5/3 "A Deflection Yoke for Generating Trapezoidal Raster in Projection CRTs"
B. B. Dasgupta and M. D. Grote, RCA Consumer Electronics Div, Indianapolis, Ind

5/4 "Large-area LCDs for Public Information Boards"
K. Fahrenschon and W. Wiemer, AEG-Telefunken, Ulm, West Germany

Session 6: Color Perception in Information Displays

Tues 2 to 5 pm, Continental 6

Chair: G. Murch, Tektronix, Inc, Beaverton, Ore

6/1 "Perceptual Analysis of Color Monitors"
R. W. Klopfenstein and C. R. Carlson, RCA Labs, Princeton, NJ

6/2 "Simulation of Alphanumeric Characters on Color Monitors"
A. P. Pica, RCA Labs, Princeton, NJ

6/3 "Matching Video and Hardcopy Color"
P. McCanus and D. Mead, Tektronix, Inc, Beaverton, Ore

6/4 "Color and Brightness Contrast Effects in CRT Displays"
A. Spiker, S. P. Rogers, and J. Cicinelli, Anacapa Sciences, Inc, Santa Barbara, Calif

6/5 "Automatic Chrominance Compensation for Cockpit Color Displays"
K. H. Kuo and M. H. Kalmanash, Kaiser Electronics, San Jose, Calif

6/6 "Color and Gray Scale in Sonar Displays"
K. F. Kraiss and K. H. Kuttlewesch, Forschungsinstitut fur Anthropotechnik, Wachtberg-Werthhoven, West Germany

Panel 1: Active Matrix Addressing

Tues 8 to 10 pm, Continental 4

Moderator: A. I. Lakatos, Xerox Corp, Webster, NY

Panelists: D. Ast, Cornell University, Ithaca, NY; T. P. Brody, PanelVision Corp, Pittsburgh, Pa; K. Ide, Toshiba Corp, Kawasaki, Japan; R. W. Streater, Bell-Northern Research Ltd, Ottawa, Canada; and H. Take, Sharp Corp, Nara, Japan

Panel 2: Flat-panel Technologies for Computer Workstations

Tues 8 to 10 pm, Continental 5

Moderator: D. Baldauf, IBM Corp, Kingston, NY

Panelists: S. Morozumi, Suwa Seikosha Co, Nagano, Japan; G. Holz, Plasma Graphics Corp, Plainfield, NJ; A. Sobel, Lucitron Corp, Northbrook, Ill; C. King, Planar Systems, Beaverton, Ore; and M. Higgins, Hewlett-Packard Co, Corvallis, Ore

Panel 4: Touch Panels, Voice, Mouse, and Other Data I/O

Tues 8 to 10 pm, Continental 1/2/3

Moderator: D. Hanson, Boeing Commercial Airplane Co, Seattle, Wash

Panelists: J. A. Sutton, Hewlett-Packard Co, Santa Barbara, Calif; J. A. Williams, IBM Corp, Raleigh, NC; K. C. Bice, Texas Instruments, Inc, Austin, Tex; and J. Love, Apple Computer, Cupertino, Calif

Session 7: Plasma Panels

Wed 9 to 11:35 am, Continental 4

Chair: A. Sobel, Lucitron, Inc, Northbrook, Ill

7/1 "Self-scan Memory Plasma Display Operating Techniques"
G. E. Holz, Plasma Graphics Corp, Plainfield, NJ

7/2 "An 8-in. Diagonal Pulse Discharge Panel with Internal Memory for a Color TV Display"
H. Murakami, R. Kaneko, R. Toyonaga, and S. Sega, NHK Technical Research Labs, Tokyo, Japan

7/3 "An 8-in. Diagonal High Efficacy Townsend-discharge Memory Panel Color TV Display"
S. Mikoshiba and S. Shinada, Hitachi, Ltd, Tokyo, Japan

*Program sessions are subject to last-minute changes.

(continued on page 70)

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(continued from page 68)

7/4 "An ac Plasma Panel Operating with the IBM Personal Computer"
T. N. Criscimagna, H. S. Hoffman, and W. R. Knecht, IBM Corp, Kingston, NY

7/5 "An ac-refresh Plasma Panel with High Voltage CMOS Drivers and Unbalanced Power Supplies"
H. Sakuma, H. Wakaumi, T. Suzuki, and T. Aizawa, NEC Corp, Kawasaki, Japan

7/6 "A High Voltage Driver IC for Large Plasma Panels"
L. Delgrange, F. Vialettes, and J. Deschamps, Thomson-CSF, Saint-Egrève, France

Session 8: Simulation and Display
Wed 9 to 11:45 am, Continental 5

Chair: A. Wu, Singer Flight Systems, Binghamton, NY

8/1 "A Self-aligning CRT Projection System with Digital Correction"
P. Lyon and S. Black, Evans & Sutherland Computer Corp, Salt Lake City, Utah

8/2 "Fiber-optic, Helmet-mounted Display for Full Visual Flight Simulation"
C. L. Hanson and T. M. Longridge, Air Force Human Resources Lab, Williams AFB, Ariz; B. Wesch and R. Kruk, CAE Electronics, Ltd, Montreal, Canada

8/3 "A Programmable Low Cost Hybrid Display Processor for Man-in-the-loop Simulation"
R. W. Allen, J. R. Hogue, and J. C. Smith, Systems Technology, Inc, Hawthorne, Calif

8/4 "A CGI Simulator Display in a High G Environment"
J. Eyth, Jr, Naval Air Development Center, Warminster, Pa

8/5 "Multifunctional Autostereoscopic Image Display System"
E. A. Rudell and D. Sheiman, The Bright & Morning Star Co, Lawndale, Calif

8/6 "General Solution to the Problem of Stereoscopic Video"
L. Lipton, Stereographics Corp, San Rafael, Calif

Session 9: Nonemissive Displays I
Wed 9 to 10:40 am, Continental 6

Chair: A. R. Kmetz, AT&T Bell Labs, Murray Hill, NJ

9/1 "Recent Advances in LCD Technology for Automotive Application"
P. M. Knoll and F. Heintz, Robert Bosch GmbH, Karlsruhe, West Germany

9/2 "Multiplexed Dot-matrix Displays with Guest-host CNPT Mixtures in Homeotropic Orientation"
J. F. Clerc, A. Perrin, and F. Muller, LETI, Grenoble, France

9/3 "Color-free Plastic LCD with High Reliability"
P. A. Penz, J. Sampsell, D. Collins, R. Petcavich, L. Sanders, and M. Piliavin, Texas Instruments, Inc, Dallas, Tex

9/4 "PLZT Color Displays"
G. Haertling, Motorola, Inc, Albuquerque, NM

Session 10: CRT-based Systems
Wed 9 to 10:40 am, Continental 1/2/3

Chair: R. H. Schmahl, Hughes Aircraft Co, Fullerton, Calif

10/1 "Phone Slave: A Graphical Telecommunications System"
C. Schmandt and B. Arons, Massachusetts Institute of Technology, Cambridge, Mass

10/2 "The Development of a High Resolution Digital Converter"
D. Seegmiller, Digivision, San Diego, Calif

10/3 "Anti-aliasing for Broadcast Compatible Television"
W. Bender, Massachusetts Institute of Technology, Cambridge, Mass

10/4 "A 19-in. Color Graphics Monitor for Military Applications"
S. Berkoff and A. DeLorenzo, Hazeltine Corp, Greenlawn, NY

Session 11: AC Plasma Displays
Wed 2 to 4:35 pm, Continental 4

Chair: K. C. Park, IBM Corp, Kingston, NY

11/1 "IBM's 581 ac Plasma Display Technology"
P. Pleshko, IBM Corp, Kingston, NY

11/2 "Thin-film Dielectric ac Plasma Panels"
N. H. Riederman, D. L. Monarchie, R. E. Wisnieff, and A. Keyworth, Norden Systems, Inc, Norwalk, Conn

11/3 "Logically Addressable Surface Discharge ac Plasma Display Panels with a New Write Electrode"
T. Shinoda and A. Niinuma, Fujitsu, Ltd, Akashi, Japan

11/4 "Characteristics of Crosstalk in Color Doughnut ac Plasma Display Panels"
H. Uchiike, N. Awaji, and Y. Fukushima, Hiroshima University, Higashi-Hiroshima, Japan; and T. Shinoda, Fujitsu, Ltd, Akashi, Japan

11/5 "Domains in ac Plasma AND Gates"
L. F. Weber and C. N. Steiner, University of Illinois, Urbana, Ill

Session 12: Flat-panel Applications
Wed 2 to 4:10 pm, Continental 5

Chair: S. Bristow, Atari, Sunnyvale, Calif

12/1 "A Handheld Man-Machine Interface Using an Electroluminescent Matrix Display"
E. S. Darlington, Texas Instruments, Inc, Dallas, Tex

12/2 "DC EL Displays with Integrated Fixed-legend and Dot-matrix Touch Switches"
D. A. Levien, Tube Investments Research Labs, Walden, England; and R. Hayes, Phosphor Products Co, London, England

12/3 "Simultaneous Display of Eight Signal Traces on a Thin-film EL Panel"
D. Bosman and J. G. R. Van Mourik, Twente University of Technology, Enschede, The Netherlands

(continued on page 72)

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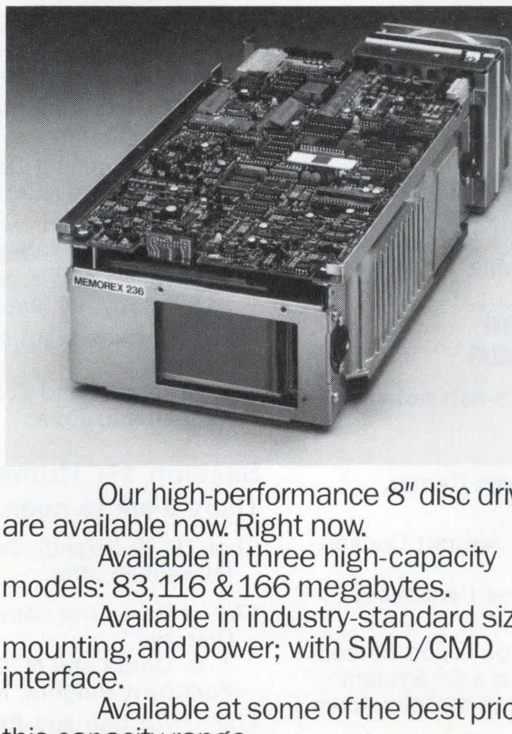

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CIRCLE 36

(continued from page 70)

12/4 "An 80-character by 25-line LCD System"
W. Harter, S. Lu, S. Ho, B. Basler, W. Newman, and C. Otasuro, CrystalVision, Inc, Sunnyvale, Calif

Session 13: Nonemissive Displays II
Wed 2 to 4:15 pm, Continental 6

Chair: P. Van Loan, Hewlett-Packard Co, Corvallis, Ore

13/1 "Hybrid Alignment in Phase-change Guest-host LCDs"
R. W. Filas, AT&T Bell Labs, Murray Hill, NJ

13/2 "New Dyes for Black Guest-host Liquid Crystal Systems"
U. Claussen, A. Brockes, E. F. Kops, F. W. Krock, and R. Neeff, Bayer AG, Leverkusen, West Germany

13/3 "Low-Birefringence Nematic Hosts and Their Performance in Reflective Guest-host Cells"
J. F. Clerc, LETI, Grenoble, France

13/4 "Multicolor Graphic LCD with Tricolor Layers Formed by Electrodeposition"
H. Kamamori, M. Suginoya, Y. Terada, and K. Iwasa, Seiko Instruments & Electronics, Chiba, Japan; and T. Nomura, J. Yasukawa, and T. Suzuki, Shinto Paint Co, Ltd, Tokyo, Japan

13/5 "Homeotropic Alignment of Nematic LCs by Oblique Evaporation of Calcium Fluoride"
S-S. Chen, Shugvang Electron Tube Factory, Chansha, People's Republic of China

Session 14: Voice Input/Output
Wed 2 to 4:10 pm, Continental 1/2/3

Chair: B. Gurman, U.S. Army Avionics R&D Activity, Fort Monmouth, NJ

14/1 "Voice Control of Displays"
D. R. Lambert, Naval Ocean Systems Center, San Diego, Calif

14/2 "Use of Voice Integrated with Aircraft Cockpit Displays"
C. A. Moore and J. C. Ruth, General Dynamics, Fort Worth, Tex

14/3 "Human Factors Comparison of Touch Screen and Voice Command Data Entry on a C^3 System"
P. M. Crane, University of Pittsburgh at Johnstown, Johnstown, Pa

14/4 "Intelligibility of Phoneme Synthesized Speech in High Noise Environments"
A. V. Dentino, U.S. Army Avionics R&D Activity, Fort Monmouth, NJ

Session 15: AC Thin-film Electroluminescence
Thurs 9 to 11:35 am, Continental 4

Chair: E. Schlam, U.S. Army ERADCOM, Fort Monmouth, NJ

15/1 "A 256 x 512 Graphic EL Display Module"
I. Linden, E. Jarvinen, K. H. Sallmen, and J. Skarp, Lohja Corp, Lohja, Finland

15/2 "Multiplex Drive of a Thin-film EL Panel"
T. Gielow, R. Holly, D. Lanzinger, and T. Ng, Hycom Inc, Irvine, Calif

15/3 "Large-area ac Thin-film EL Displays"
M. I. Abdalla, J. L. Plumb, and L. L. Hope, GTE Lighting Products, Salem, Mass

15/4 "Strontium Sulphide: The Host for a New High Efficiency Thin-film EL Blue Phosphor"
W. A. Barrow, R. E. Coovert, and C. N. King, Planar Systems, Inc, Beaverton, Ore

15/5 "New Method to Evaluate Defect Density in ac Thin-film EL Insulating Films"
M. Wakitani, K. Okamoto, S. Sato, S. Miura, and S. Andoh, Fujitsu Labs, Ltd, Kanagawa, Japan

Session 16: CRT Technology I
Thurs 9 to 11:50 am, Continental 5

Chair: W. A. Hamilton, Raytheon Co, Sudbury, Mass

16/1 "A 19-in. Very High Resolution Display CRT"
C. Odenthal, Tektronix, Inc, Beaverton, Ore

16/2 "Simulation of Cathode-region Electron Beams"
C. Loty, Laboratoires d'Electronique et de Physique Appliquée, Limeil-Brévannes, France

16/3 "An Experimental 'In-neck' Integrated Yoke"
K. K. N. Chang, RCA Labs, Princeton, NJ

16/4 "A Clamshell Deflection Yoke"
D. K. Strong, Tektronix, Inc, Beaverton, Ore

16/5 "A Flat Color TV Display with Horizontal Addressing and Vertical Deflection"
E. Miyazaki and Y. Sakamoto, Kanazawa Institute of Technology, Ishikawa, Japan

16/6 "Surface Light-emitting Fluorescent Indicator Panel"
T. Horigome and T. Miyazaki, NEC Kagoshima, Ltd, Kagoshima, Japan

Session 17: Human Factors
Thurs 9 am to noon, Hilton Plaza Room

Chair: E. R. Strandt, Delco Systems Operations, Milwaukee, Wis

17/1 "Doing the Same Work with Paper and CRT Displays"
J. D. Gould and N. Grischkowsky, IBM Corp, Yorktown Heights, NY

17/2 "VDT Use and Productivity"
L. D. Silver, University of Pittsburgh, Pittsburgh, Pa; and P. M. Jackson, Carnegie-Mellon University, Pittsburgh, Pa

17/3 "Legibility Study of a Tactical Graphics Language for High Resolution Monochrome Display"
G. A. Osga, Naval Ocean Systems Center, San Diego, Calif

17/4 "Psychophysical Problems and Solutions in Variable Acuity Displays"
R. W. Fisher, McDonnell Douglas Corp, St. Louis, Mo

17/5 "Imaging-system Design Based on Psychophysical Data"
W. E. Glenn and K. G. Glenn, New York Institute of Technology, Dania, Fla

(continued on page 74)

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(continued from page 72)

17/6 "The Display Quality of Glare Filters for CRT Terminals"
R. J. Beaton and H. L. Snyder, Virginia Polytechnic Institute, Blacksburg, Va

Session 18: Active Matrix Displays
Thurs 2 to 4:35 pm, Continental 4

Chair: D. E. Castleberry, General Electric Co, Schenectady, NY

18/1 "LC TV Addressed by MIM Devices"
K. Niwa, S. Maezawa, M. Suzuki, S. Takeuchi, and T. Kamikawa, Suwa Seikosha Co, Ltd, Suwa, Japan

18/2 "A 7.23-in. Diagonal Color LCD Addressed by a-Si TFTs"
Y. Ugai, Y. Murakami, J. Tamamura, and S. Aoki, Hosiden Electronics Co, Ltd, Osaka, Japan

18/3 "A 240- x 360-element Active Matrix LCD with Integrated Gate-bus Drivers Using PolySi TFTs"
Y. Oana, Toshiba R&D Center, Kawasaki, Japan

18/4 "4.25- and 1.51-in. B/W and Full-color LC Video Displays Addressed by PolySi TFTs"
S. Morozumi, K. Oguchi, T. Misawa, R. Araki, and H. Ohshima, Suwa Seikosha Co, Ltd, Suwa, Japan

18/5 "High Voltage TFTs for Addressing of Light Valves and EL Displays"
E. Lueder, G. Moersch, T. Kallfass, and K. Koger, University of Stuttgart, Stuttgart, West Germany

Session 19: CRT Technology II
Thurs 2 to 5 pm, Continental 5

Chair: A. Martin, Thomson-CSF, Saint-Egrève, France

19/1 "High Resolution Color CRTs Using a Tilt-array Shadow Mask"
T. Banno, S. Hayasahi, and Y. Yamaguchi, NEC Corp, Kawasaki, Japan

19/2 "A 15-in. Full-square CRT"
H. Koba, H. Mori, Y. Kawata, and E. Hamano, Toshiba Corp, Fukaya, Japan

19/3 "Saturation and Heating of Miniature CRT Single-crystal Phosphor Screens"
U. Levy and H. H. Yaffe, AT&T Bell Labs, Murray Hill, NJ

19/4 "High Brightness, High Resolution Miniature CRT"
E. E. Gritz, Hughes Aircraft Co, Carlsbad, Calif

19/5 "Frit-sealed, Metal-glass CRTs with Near-flat Faceplates"
P. Seats, Thomas Electronics, Inc, Wayne, NJ

19/6 "Miniature Laser CRTs with GaAs/GaAlAs Double Heterostructure Targets"
U. Levy and R. A. Logan, AT&T Bell Labs, Murray Hill, NJ; and Y. Niv, Rutgers University, Piscataway, NJ

Session 20: Nonimpact Printing
Thurs 1:30 to 5 pm, Hilton Plaza Room

Chair: H. L. Funk, IBM Corp, White Plains, NY

20/1 "Technology Trends in Electrophotographic Printing"
B. Grant, IBM Corp, San Jose, Calif

20/2 "A New Method for Ink-jet Character Printing"
R. Rydgren and C. H. Hertz, Lund Institute of Technology, Lund, Sweden

20/3 "Airflow Effects on Drop Formation for Air-assisted Drop-on-demand Ink Jets"
R. L. Adams, Oregon State University, Corvallis, Ore; and J. Roy, Tektronix, Inc, Beaverton, Ore

20/4 "Characteristics of a High Viscosity, Oil-based Ink-jet Head"
S. S. Bupara, Exxon Office Systems Co, Brookfield, Conn

20/5 "Droplet Emission with Micro-planar Ink Drop Generators"
M. Doering, Philips GmbH, Hamburg, West Germany

20/6 "A New Attack on Electrolytic Printing"
J. P. Pawletko, D. A. Opp, C. G. Speicher, P. L. Gendler, and E. Fey, IBM Corp, Endicott, NY

20/7 "Laser Thermal Multilevel Recording—Structure Optimization"
S. Oikawa and A. Morinaka, Nippon Telegraph & Telephone Public Corp, Tokai Ibaraki, Japan □

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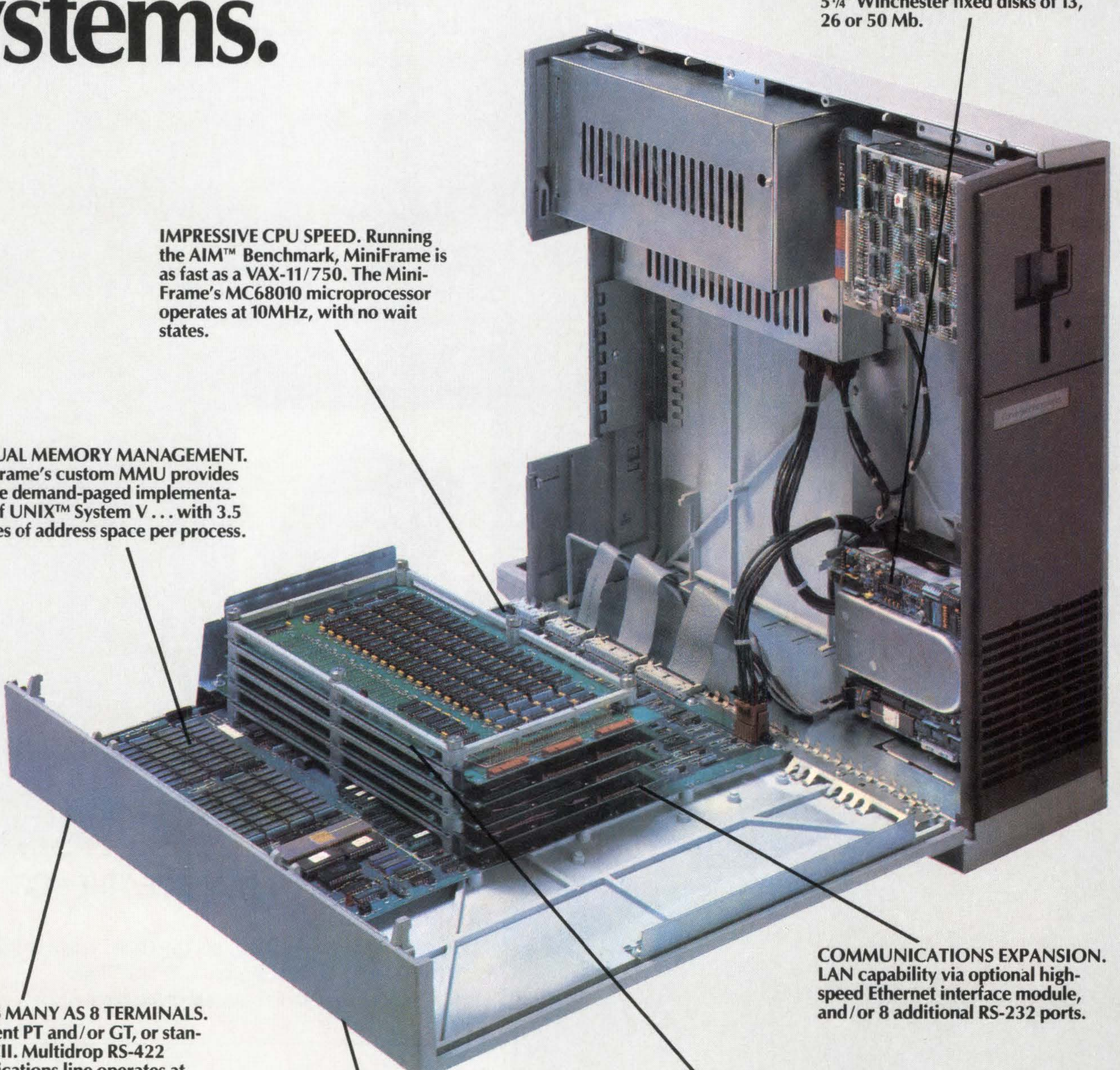

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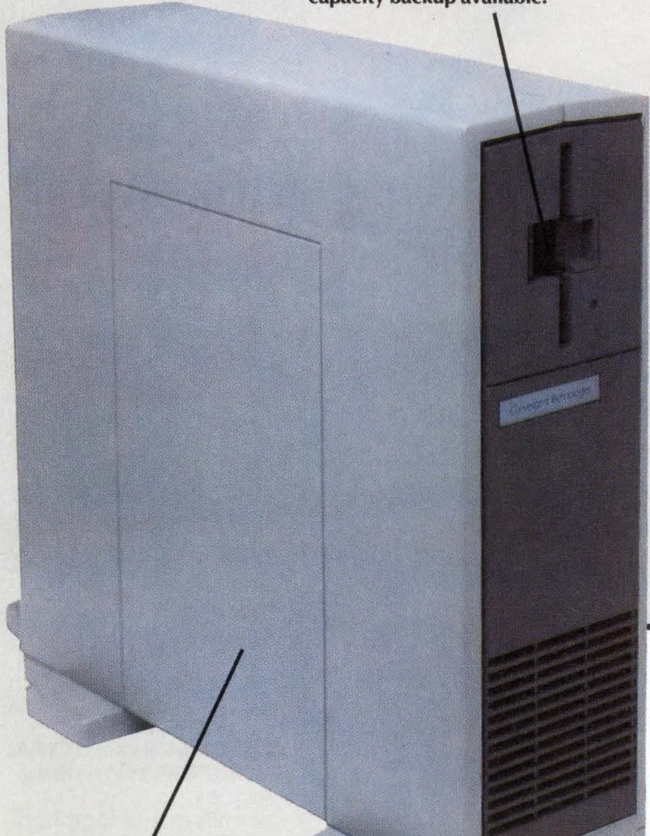

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CIRCLE 40

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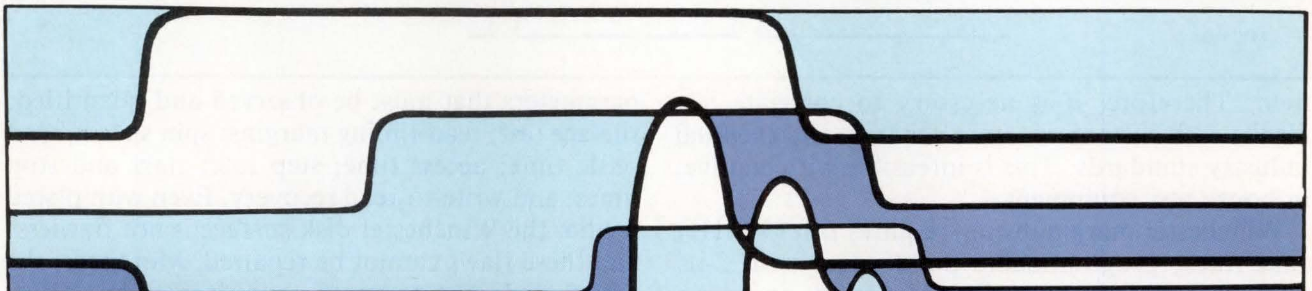
CIRCLE 41

HOW TO TEST WINCHESTER DISK DRIVES

While readback jitter has made window margins a major testing concern, flexibility, correlation, and simplicity of operation are also key issues.



by Jerry Ruoff

As shrinking sizes and lower prices propel Winchester disk drives into new applications, manufacturers are faced with demands of escalated production. Sustaining disk drive quality while increasing the manufacturing rate, however, requires a major investment in testing. Unfortunately, manufacturers have poured more resources into producing better disk drives than into improving testing capabilities.

Drive manufacturers can either use commercially available testers or their own tester built in-house. While home-built testers may be adequate for a particular manufacturer, they can cause correlation problems with customers who use commercial testers for incoming inspection.

Jerry Ruoff is vice president of engineering at Applied Data Communications Inc, 14272 Chambers Rd, Tustin CA 92680, where he is responsible for all hardware and software development. Mr Ruoff holds a BS and an MS in electrical engineering from the University of Southern California.

Testing Winchesters involves several problems. Margins for readback jitter on most Winchester drives can be used as a practical figure of merit, indicating the drive's anticipated bit error rate (BER) and mean time between failures (MTBF). But, designing a reliable, repeatable window-margin tester can be costly because it requires fast, programmable, drift-free circuitry and high flexibility. In addition, the drive's sealed media, which are always somewhat flawed, cannot be visually inspected for these flaws. Another problem involves the drive head's ability to switch rapidly between read/write modes, which is necessary to accommodate user requirements for arbitrary-length (soft) sectors within a track.

In-house versus commercial testers

There are many reasons within a manufacturing organization to design and fabricate test equipment in-house. Often, in-house design groups can present compelling arguments that influence corporate decisions. These arguments usually hinge on total control over testing techniques and intimate product knowledge. However, Winchester disk technology has grown so popular that it is almost a commodity

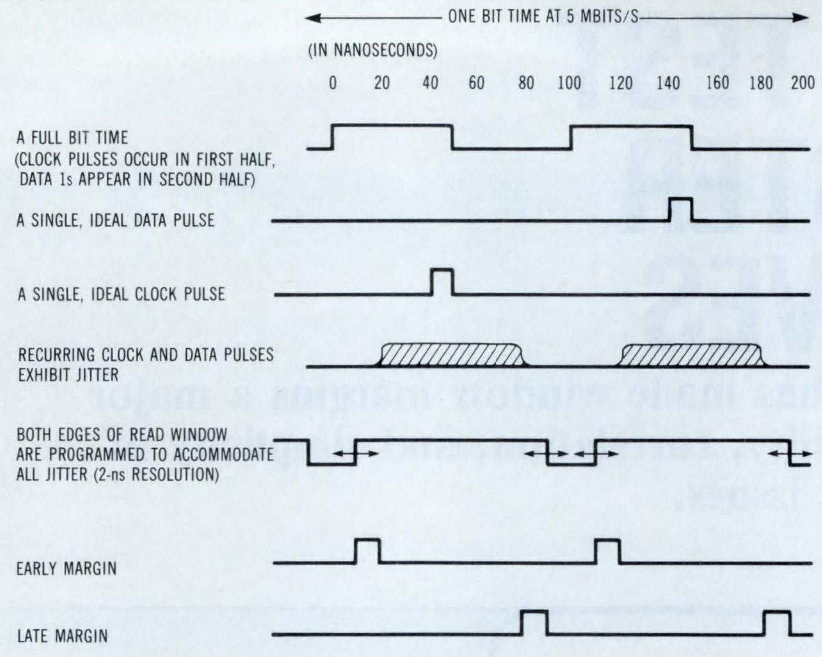


Fig 1 Read-window margins reveal more about the quality of a Winchester disk drive than any other test. The lesser of the two margins can be used as a general figure of merit to anticipate the bit error rate (BER).

item. Therefore, it is necessary to correlate test results with customers, other vendors, and eventual industry standards. This is infeasible with captive, in-house test equipment.

Winchester margin testing requires fast (5-MHz) data rates, programmable pulse edges with 2-ns sweep resolution, and a sophisticated operating system's flexibility. There are important reasons to trade off the total control of home-built Winchesters in favor of increasingly popular manufacturer testers. For example, software maintenance is automatic and ensured. Users can share a pool of helpful information, instead of working in a vacuum. Off-the-shelf test routines are available at a fraction of the cost of generating them in-house. And finally, it may not be economically justifiable to design the required hardware in-house, when proven commercial systems with continuing support are available off-the-shelf for $10,000 to $15,000.

One such commercial product, the T-650 Winchester disk drive test system from Applied Data Communications, is a production-oriented, turnkey system that provides an engineering system's power and flexibility. Simple to operate in a production environment, the system is designed to test drives with standard SA-1000 and ST506 interfaces. Connecting to four drives simultaneously, the T-650 provides over 100 types and variations of standard tests. Also, it stores user-selected test sequences and limits on a nonvolatile floppy disk. The system has disk-resident software, generates logically displaced index marks, and has a battery-backed calendar/clock for burn-in/life tests. Moreover, it is programmed in its own mnemonics, avoiding Forth and other formal user languages.

Whether drives are tested by in-house equipment or commercial testers, there are eight important drive parameters that must be observed and quantified: surface test; read-timing margins; spin speed; head settle time; access time; step rate; start and stop times; and write-to-read recovery. Even with plated media, the Winchester disk surface is not flawless, and these flaws cannot be repaired. Moreover, the sealed enclosure prevents visual inspection. Thus, executing a surface test on all drives maps out the flaws. The test system then uses the flaw map to print out a deallocation table, which is physically taped to the drive under test at the factory. Deallocation tables are used as input to the user's operating system. The operating system uses the table to truncate flawed sectors beginning with the first bad byte. Surface defects then become transparent to the user.

A close look at test parameters

After completing the surface test, each sector will begin with a sync pattern, followed by an address mark (identified by its unique characteristic of one missing clock pulse). Then, data and a cyclic redundancy check (CRC) character follow. To properly emulate the user's environment, an arbitrary number of arbitrary-length sectors must be provided in each track. This precludes the use of simple disk exercisers, which lack soft-sector capability and cannot logically displace the drive's physical index marks.

At the customer's incoming inspection, it is important to execute a surface test and compare the deallocation table with the one generated at the factory. This procedure quickly reveals the shipping damage. Beginning a test sequence with a surface test makes intrinsic sense because the flaw map will preclude further testing on obviously defective areas.

After surface testing, perhaps the most important Winchester parameter is its read-timing margin—a measure of the drive's quality. This parameter measures the dynamic range of readback jitter and how that spread relates to the drive's 100-ns wide read-timing window (see Fig 1).

In the drive under test, information bits are laid serially along a circumferential data track. The bits (encoded as magnetic flux reversals) are laid down with regular spacings between them. However, four phenomena produce readback timing irregularities, also called jitter.

Noise in the drive's read/write amplifiers causes jitter. Asymmetrical windings in the center-tapped read/write head cause jitter. Hysteresis in the drive's zero-crossing read threshold also causes jitter—positive-going and negative-going zero-crossings trigger output bits at different slope levels. And, bit shift due to flux reversal crowding causes jitter—data domains in a densely packed medium tend to migrate from where they were initially laid. While write-precompensation techniques based on the recorded bit patterns can help reduce bit migrations, they cannot eliminate them. If the accumulation of readback jitter sources is not accommodated by the drive's read circuits, with margin to spare, the drive's BER soars.

There are two popular ways to measure Winchester read margins (T-650 features both). The first is to generate a 100-ns read window and shift it early in 2-ns increments until the BER increases dramatically, then retard it in 2-ns increments until the BER again increases dramatically. The smaller of the two read margins is subsequently reported against the nominal center.

A more thorough way to measure read margins (and one that should be used throughout all other test phases) is to generate a 100-ns window and shrink it in 2-ns increments, both early and late, until the BER increases on both sides. After backing off one increment, both margins are reported simultaneously. This indicates the total dynamic range of read-data jitter. The 100-ns read window is a function of Winchester standard rotational speed—3600 rpm—and its standard data rate is 5 Mbits/s. This 5 Mbits/s translates into 200 ns per modified frequency modulation (MFM) bit cell. However, an MFM bit cell may contain either a clock or a data pulse; the difference being the 100-ns half-bit time in which it appears.

Although most test patterns are valid, the worst-case test pattern for margin testing is a repeating sequence of double pulse 1s, interspersed with individual 0s (ie, $6DB_{hex}$ = 0110 1101 1011). This is because the double pulses tend to migrate toward each other, decreasing the flux peaks and reducing amplitude changes in the read head.

As a rule of thumb, new Winchester disk drives with ferrous oxide coated media should exhibit window margins of 10 to 12 ns, early and late. New drives with plated, thin-film media can exhibit margins up to 30 ns (all the jitter is contained within the center 40 ns of read-window time). Margin times greater or less than these can be interpreted directly as a figure of merit, anticipating the drive's BER, MTBF, and useful lifetime.

Another test parameter, spin speed, is a measure of drive quality. Correct spin speed, which requires good motor speed regulation, results in a proper and constant data rate of 5 Mbits/s. If the rate varies, it works directly against the drive's window margins.

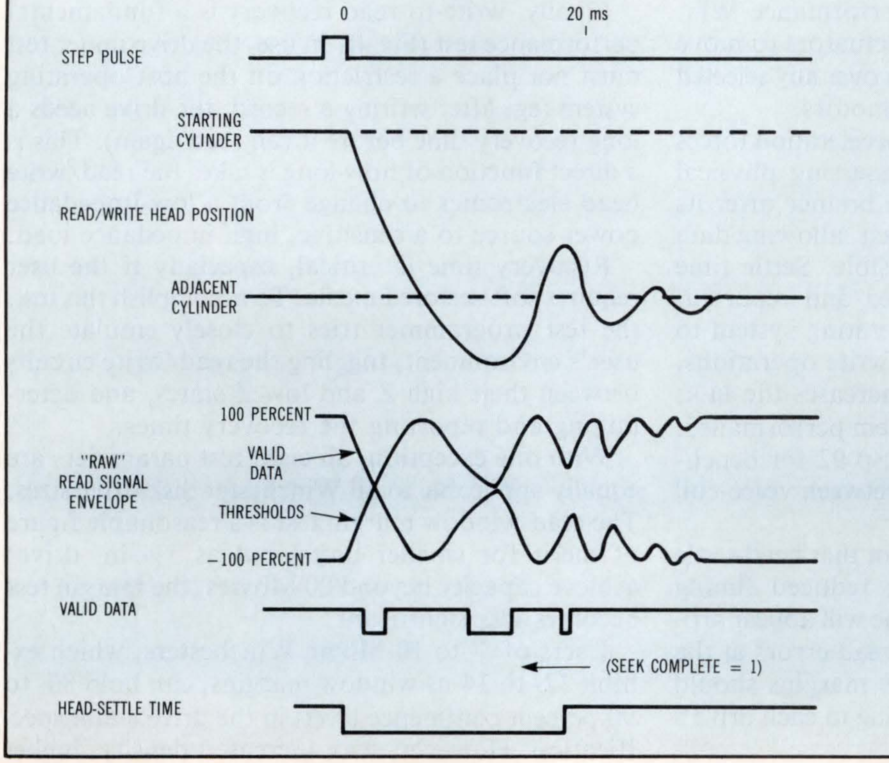


Fig 2 Head-settle time must be tested with window margins set critically short on both sides. If windows are set a normal size (100 ns), head-settle time may appear too short, causing an operating system to read/write prematurely.

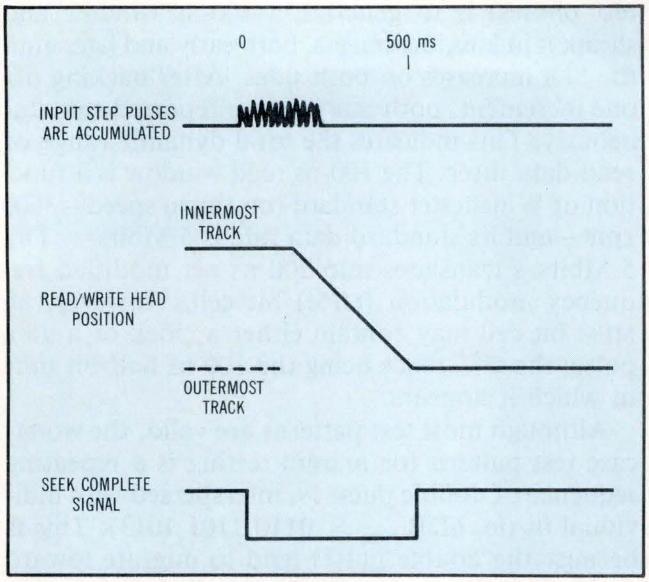


Fig 3 Access time is a performance test for smart Winchester drives featuring a buffered-step mode. The test involves the sum of the step-pulse input string duration plus lateral head motion. Manufacturers typically specify only head motion.

If spin speed were out of spec, the disk could be unreadable because disk-resident clocks and data would shift out of the 100-ns read window.

Units for spin speed can be specified in either rpm or in milliseconds per revolution (3600 rpm ±1 percent, or 16.67 ms for a 5½-in. platter). By convention, time units are preferred because a drive's total test time is more easily calculated: it takes one revolution to write a track; another revolution to read it back; and at least a third revolution to seek the next track.

Head-settle time is a parameter to the drive's performance (Fig 2). The highest performance Winchester drives use fast voice-coil actuators to move their read/write heads into position over any selected track. Slower drives use stepper motors.

Voice-coil actuators apply high acceleration forces to move the head assembly. Possessing physical mass, the head has a tendency to bounce after its arrival. Bounce decay should be fast, allowing data to be accessed as quickly as possible. Settle time needs to be accurately determined and reported, which enables the user's host operating system to know how long to hold off read/write operations. Beginning read/write too soon increases the BER; holding off too long degrades system performance. (See *Computer Design*, Jan 1983, p 92 for benchmark performance comparisons between voice-coil actuators and stepper motors.)

As with other tests, it is important that head-settle time be executed with critically reduced timing margins. Otherwise, head-settle time will appear artificially short, thus causing gross read errors at the user level. Early and late window margins should be adjusted independently, according to each drive's individual characteristics.

Access time is a performance test for the new generation of smart Winchester drives (Fig 3). Smarter drives have a buffered-step mode that accumulates step commands at high speed, then advances the head actuator mechanism at its own, optimum rate—slow enough to avoid seek errors, but fast enough to keep performance levels up. This off-loads the drive's host, but it buries arm-motion testability. When testing a drive for access time, a user tells it where to go, then counts down how much time it takes for it to report that it arrived.

Step rate is a quality test for drives that provide test access to their head-positioning logic. In this test, the frequency of step pulses is swept up and down. The maximum step rate short of producing seek errors is determined and reported. (Access time and step rate tests are mutually exclusive.)

For a Winchester drive, rapid start and stop times help contribute to its useful lifetime. Winchester heads fly 19 μin. off the platter surface, but it takes 15 s for the platters to come up to speed after power is applied. Even though the disk is lubricated and dedicated "landing zones" are provided, the head operates in a crashed mode until it becomes airborne. This produces unnecessary wear and reduced lifetime. Clearly, start and stop times should be as short as possible.

User benefits

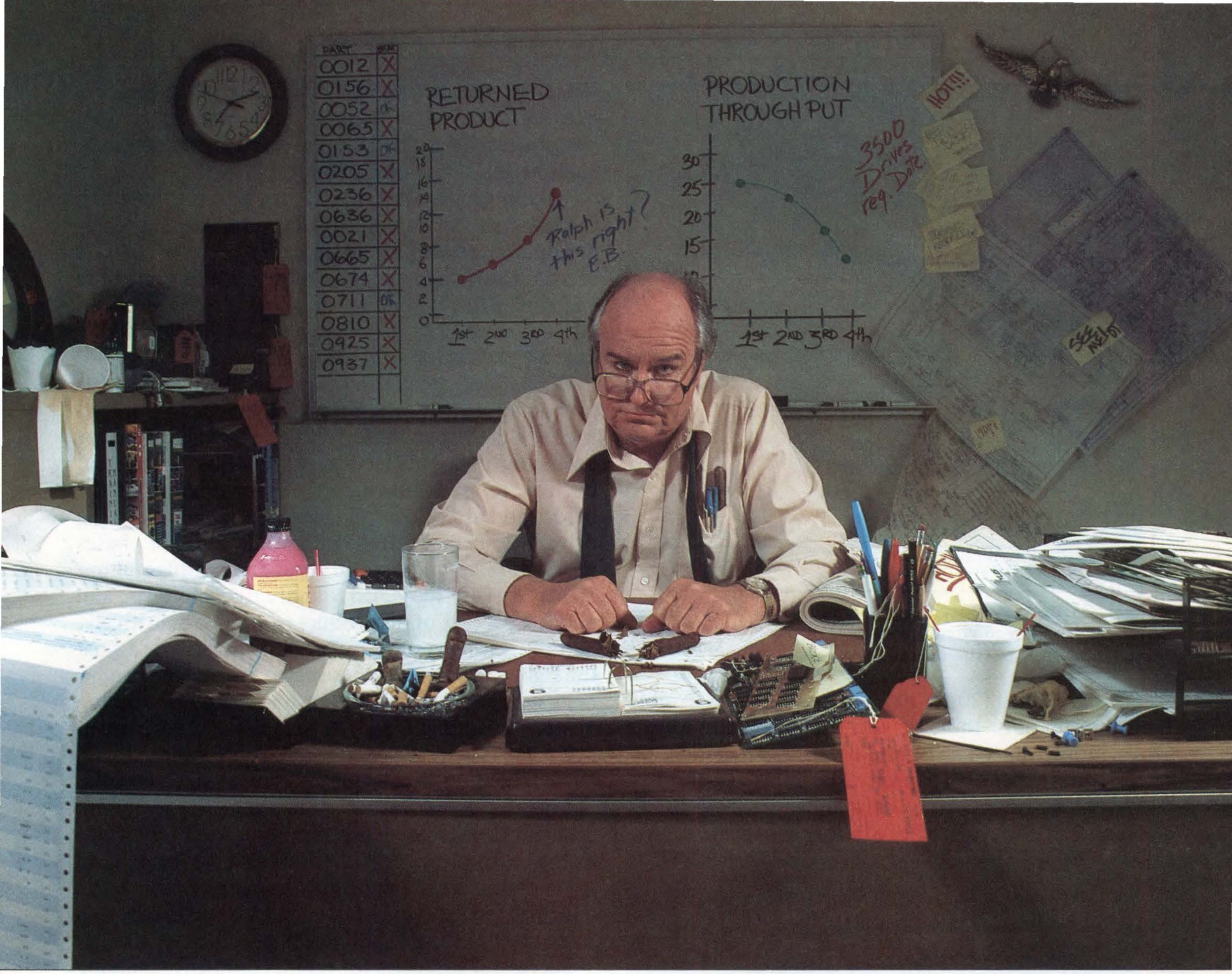
In terms of marketing, there is an additional benefit for Winchester drives with rapid start times: the user is not kept waiting as long. While this probably does not affect performance, a user, given a choice between two otherwise identical disk drives will always prefer the faster one.

Finally, write-to-read recovery is a fundamental performance test (Fig 4). In use, the drive under test must not place a restriction on the host operating system (eg, after writing a record, the drive needs a long recovery time before it can read again). This is a direct function of how long it takes the read/write head electronics to change from a low impedance power source to a sensitive, high impedance load.

Recovery time is critical, especially if the user requires soft-sectored media. To accomplish this test, the test programmer tries to closely emulate the user's environment, toggling the read/write circuits between their high Z and low Z states, and determining and reporting the recovery times.

With one exception, all eight test parameters are equally applicable to all Winchester disk drive sizes. The read-window margin test is a reasonable figure of merit for smaller units, but as 5¼-in. drives achieve capacity beyond 20 Mbytes, the margin test becomes less significant.

Users of 5- to 10-Mbyte Winchesters, which exhibit 12- to 14-ns window margins, can hold 80- to 90-percent confidence levels in the drive's BER specification. However, with increased density, higher



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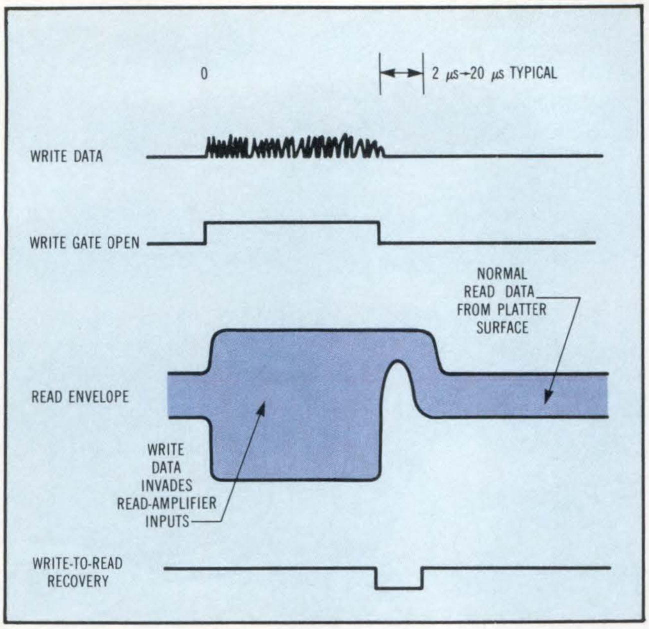

Fig 4 Write-to-read recovery determines how long it takes for the drive's read circuits to recover from high level excitation after a write operation.

capacity drives (20 to 100 Mbytes) tend to exhibit more jitter. For these drives, the BER is less keyed to window margins. Limits of 10 to 12 ns may be too stringent for high capacity 5¼-in. drives. Rather, 8 to 10 ns or less may be a more realistic limit. Beyond 20 Mbytes, the window margin test for Winchester drives should be considered more of a qualitative test than a quantitative one. Moreover, margin tests should be augmented by other tests, such as the maximum data test.

Maximum data is a brute force BER test in which the test system formats the disk under test and writes a worst-case test pattern in every sector. Then, it continuously reads back enough data to verify the specified BER.

Testing strategies

Developing the highest possible confidence levels in the shortest periods of time is the objective of testing. At the drive manufacturer and system integrator levels, outgoing inspection usually involves a test/burn-in/retest cycle with critical evaluation of the before and after deltas. Typically, 100 percent of the drives are surface tested, with additional test phases of write, read, and margin tests. Lot samples (about 10 percent) are subjected to more rigorous tests, and about 1 percent of all product is tested exhaustively. Sample testing results are used to confirm or adjust the rigor of the general testing strategy. One prominent system integrator notes that 5 min of outgoing inspection testing on a T-650 results in a 95-percent drive confidence level.

At incoming inspection, a typical strategy is to lightly test a variety of parameters. If a failure occurs, the test system is programmed to branch into intensive diagnostic test phases. For a 5-Mbyte drive, it generally takes 2 to 3 min maximum to execute a surface test; and to check all read/work heads, step rates, access times, spin speeds, and margins.

Successful strategies for rapid, confidence building tests presume that the drive under test has data, control, and power interfaces common to the industry at large. Drives that use unusual interface schemes may not be accessible to manufacturer test systems, and could be locked into testing with home-built machines. This would result in needless design cost and a lack of correlation with consumers.

Shrinking size, eroding cost, and increasing intelligence of Winchester disk drives call for testing techniques and equipment that provide simplicity, flexibility, and correlation to others. For new 5- and 10-Mbyte drives, read-window margins provide a reasonable figure of merit to gauge BER and MTBF. But, for new drives of 20 Mbytes and up, maximum data tests may be required to augment window-margin testing.

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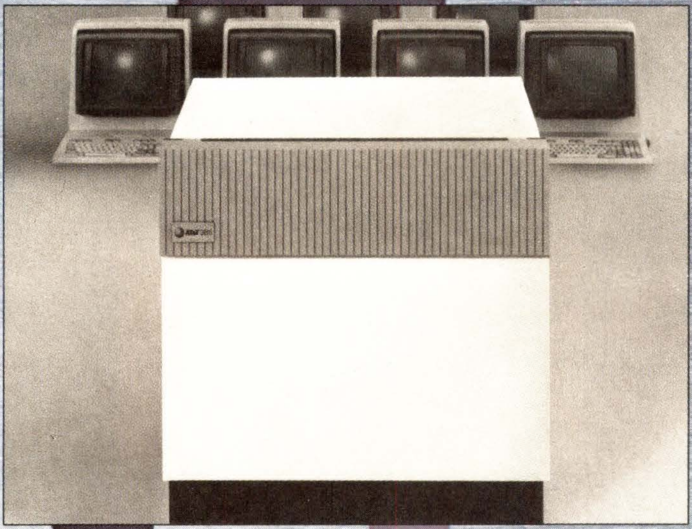

3B5

These general-purpose, midrange, true 32-bit, super minicomputers are designed to run UNIX System V and can accommodate up to sixty users without putting a dent in response time.

They are remarkably easy to use, and easy to maintain because they are self-diagnostic. They are flexible, powerful tools for a variety of applications, such as software development, office systems, and CAD/CAM.

They're the 3B5/100 and 3B5/200. From AT&T.

They can be configured to suit customer needs with a wide variety of I/O, peripheral, memory, and communications options for cost-effective growth. This makes them good investments for your customers.

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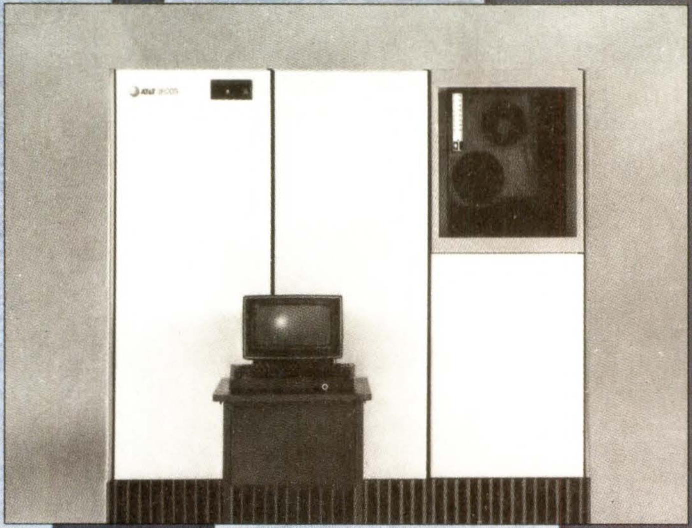

3B20S

The 3B20S computer is the high-end supermini of the 3B family. It runs UNIX System V and is designed to meet the rigorous needs of data centers, developers, office service organizations, and manufacturing locations.

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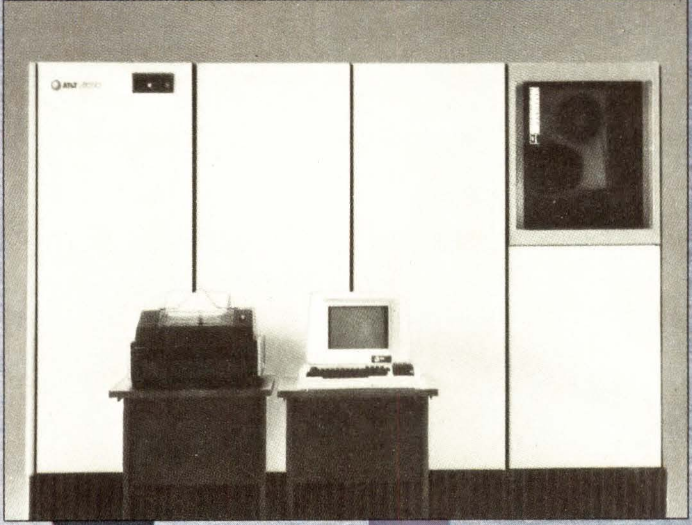

3B20D

It is a powerful, 32-bit super minicomputer that will set a new standard for uptime. It runs the new UNIX RTR operating system, providing time-sharing and introducing real time and fault-tolerant features.

It operates continuously even during hardware faults, data-base mutilations, repair, software updates and growth.

It is the 3B20D. From AT&T.

It is ideal for applications requiring ultra-reliability and fast response such as reservation systems, command and control systems, on-line banking systems, and others where computer outage means serious or intolerable business losses.

Like the 3B20S and 3B20A, the 3B20D does not require air conditioning or raised floors.

For continuous computing, the 3B20D is unsurpassed in its class.

ARRAY-BASED LOGIC BOOSTS SYSTEM PERFORMANCE

Using ECL arrays to build standard logic blocks increases gate speeds by more than a factor of four and offers 100 times the density of standard 10K ECL logic.

by Cary R. Champlin and Jerry E. Prioste

In any IC technology, LSI exhibits many advantages. In 10K ECL, speed and logic density are particularly important benefits. A family of standard ICs derived from the MCA I macrocell array, for example, gives the ECL designer greater than a fourfold increase in speed, and two orders of magnitude reduction in package count.

The MC109XX high speed family consists of an LSI multiplier, two types of ALUs, a program sequencer, and an error detection/correction unit. Each of these parts has logic densities of approximately 1200 equivalent gates and typical gate delay times of 800 ps. In comparison, an IC in 10K ECL typically has a logic density of 12 gates and gate delay times of 3.5 ns.

A common problem for high speed applications is the optimal filtering of digital signals. Optimal filtering occurs when filter characteristics are adjusted in accordance with the optimization of some signal parameter. An example of a third-order adaptive digital filter is shown in Fig 1. Two distinct areas of computation are required. In the digital filtering area, four multiplications and four additions are computed for each raw input signal sample in what is termed a "weighted-moving-average."

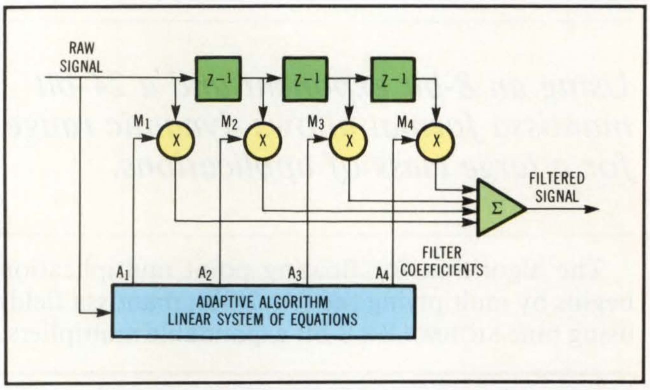

Fig 1 In this adaptive digital filter, the adaptiveness of the coefficients to the signal guarantees convergence to an optimal response with respect to a desired system parameter. When implemented in hardware, this application is intensive in arithmetic and addressing.

In the second area of computation, the adaptive algorithm solves a linear system of equations to obtain new filter coefficients. When solving a linear system of equations, variables and coefficients are organized naturally in vectors. Similarly, filter samples can be represented using vector notation. Note that in the actual implementation of the filter, the signal samples must be delayed (ie, stored) by an amount of time equal to the computation time of the adaptive algorithm. This will match—with respect to time—the filter coefficients and the signal samples.

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Jerry E. Prioste is a systems engineer in Motorola's Bipolar LSI and Memory Products Div, 2200 West Broadway, Mesa, AZ 85202. He holds a BSEE from New Mexico State University and an MSE from Arizona State University.

Traditionally, arithmetic intensive applications, such as the optimal filtering problem, require unique fixed-hardware implementations. This creates problems for the designer when the adaptive algorithm or the order of filter is modified. The alternate approach, provided the technology is sufficiently fast, is to implement the design with a computer architecture based on a linear algebra enhanced instruction set. The MC109XX family modularizes this architectural approach into three basic sections: arithmetic, memory-I/O, and control-interface.

Accelerating operations

Data is configured as a 32-bit floating point number, using an 8-bit exponent and a 24-bit mantissa format. This allows enough dynamic range for a large class of applications without compromising computational throughput. As shown in Fig 2, this also allows a specialized arithmetic module architecture based on four fundamental computations: multiply, multiply-accumulate, add/subtract, and add/subtract-accumulate.

Using an 8-bit exponent and a 24-bit mantissa format allows dynamic range for a large class of applications.

The algorithm for floating point multiplication begins by multiplying the two 24-bit mantissa fields using nine MC10901 8 x 8-bit expandable multipliers. The MC10901 is a parallel, combinatorial array based on the Dadda reduction and a fast lookahead-carry addition scheme. This method results in a maximum 8 x 8-bit multiplication time of 24.3 ns. Two mode controls (C1 and C2) are used to set the multiplier for 2's complement, unsigned magnitude, or mixed-mode operands. Through the use of C1 and C2 and the two 8-bit additive operand inputs, larger arrays are easily constructed with the MC10901.

For two left-justified operands, their product is either normalized or has 1 bit of sign extension. Examination of the top 2 product bits will detect the position of the active MSB. The MC10808 16-bit barrel shifter accomplishes the necessary shifting; two MC10808s are needed to shift a 24-bit number.

The other part of the floating point multiply algorithm is exponent processing, which requires a two-step sequence. After the exponents of the two operands are summed, the result is decremented if the MSB detect indicates sign extension in the product. The MC10902 high speed ALU is used as the exponent processor for the multiplier and the floating point add/subtract unit. OV1 is the overflow for binary arithmetic operations, while OV2 is the overflow for shift left operations. The MC10902 uses an internal 8-bit register as an accumulator or for pipeline system structures.

Floating point addition/subtraction, although more involved, is equally efficient when designed with LSI ECL. For both computations, the first step is to equalize the exponents of the two operands to align the binary point. The exponent differential is calculated and a corresponding downshift applied to one of the operand mantissas. The sign bit of the

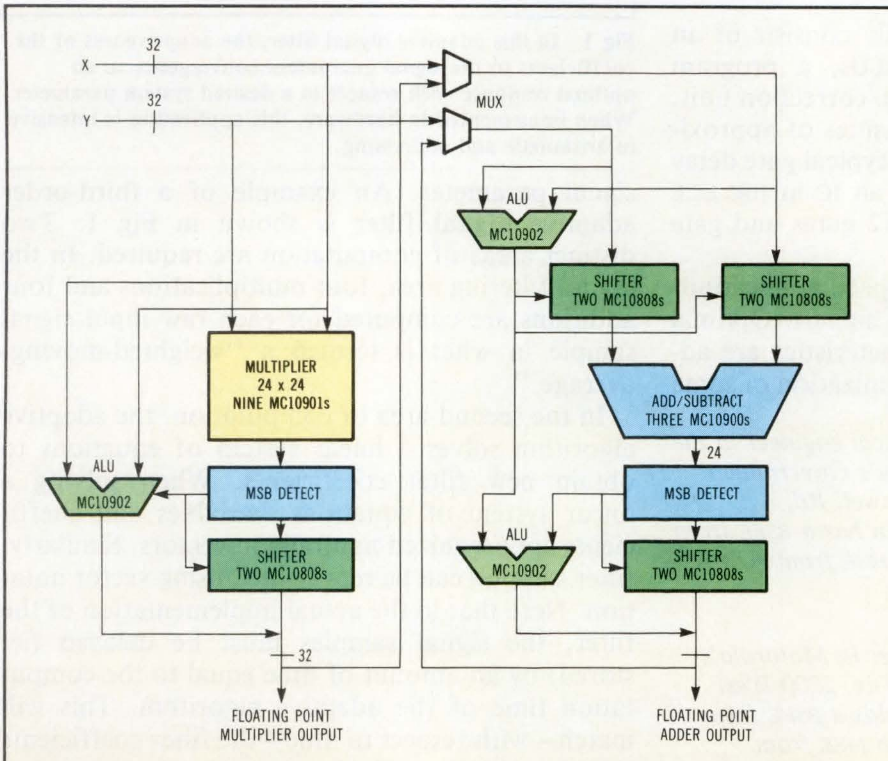

Fig 2 The 32-bit floating point arithmetic module relies heavily on LSI ECL devices. Four fundamental operations support real and complex arithmetic: multiply, multiply-accumulate, add/subtract, and add/subtract-accumulate.

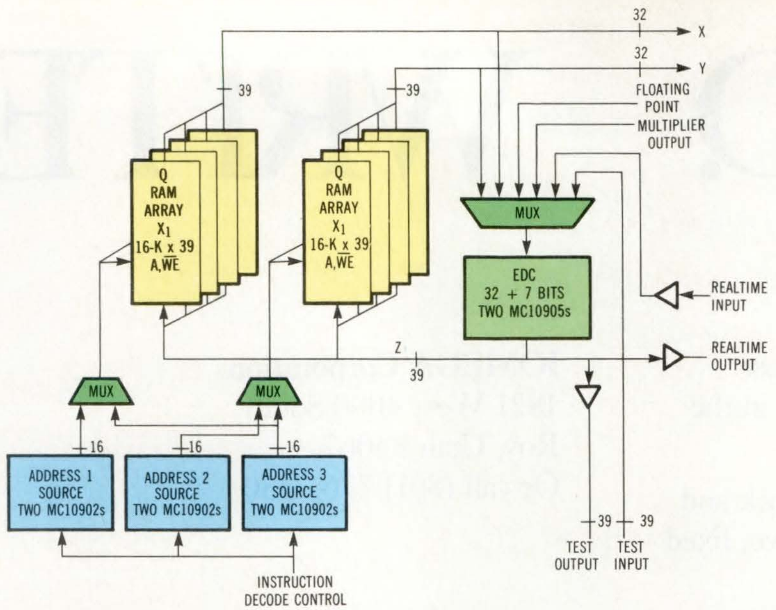

Fig 3 The MC10902 is efficient in operand address generation and arithmetic sections. To access a vector, the unit computes a sequence of locations from initial base address, displacement, index, and step-size values. The MC10905 error detection and correction (EDC) improves data validity and enhances testing diagnostics, yet only increases the pipeline by one cycle.

exponent differential selects which operand is downshifted and which exponent is used next. Two suboperations occur in the second stage. The larger exponent is gated to the second exponent ALU and the two 24-bit operands are added/subtracted.

Three MC10900 8-bit ALUs form the mantissa adder and I/O latching supports the pipelined architecture of the arithmetic module. The MC10900 generates a sum with a maximum delay of 17 ns. Using three devices and ripple carry yields a 24-bit sum in under 32 ns. Although not implemented in this application, the MC10900 maintains full parity generation and verification internally.

The third stage consists of detecting the position of the active MSB in the summation. An upshift in the range of −1 to 25 is possible at this point. Caused by an arithmetic overflow, the −1 upshift corresponds to a single-bit downshift. Total computation pipeline time for either of the two floating point calculations is 80 ns or four clock cycles. However, data is pipelined at two clock cycle intervals.

Considering memory and I/O

The continuous processing characteristic of the arithmetic module carries over to the memory architecture of Fig 3. Four interrelated sections comprise this module: dual RAM array, address generation, error detection and correction (EDC), and I/O multiplexing. Data flow during execution of a typical instruction depends on the timely interaction of these sections. First, sequences of addresses are generated from two source address ALUs and then time multiplexed to the dual RAM array during the read cycles. X and Y vector source data is routed to the arithmetic module and monitored by the EDC on a time-multiplexed basis. A flag is set upon the detection of an error. The floating point result is generated four clock cycles later and 7 check bits are appended. Finally, a sequence of addresses, generated from the destination address ALU, is applied to the dual RAM array during the write cycles. The dual RAM array is architecturally suited for three-part address, high speed vector access requirements. A dual-read/single-write memory organization nicely matches the imbalance of multiple read operations.

The continuous processing characteristic of the arithmetic module carries over to memory architecture.

Vector stack addressing is used for each operand. A 16-bit, 2's complement displacement is added to the base address, and each subsequent location is determined by the addition of a 16-bit, 2's complement step-size value. The selection of real or complex data affects addressing. To multiply complex numbers, four read multiplications and two additions or subtractions are necessary. This requires the source addressing to repeat each complex number in a specific sequence. The MC10902 ALU handles address computations (Fig 4). The internal register and the input data latches hold the current values for base, displacement, and step-size parameters. Register values load from the bit fields of the instruction decode control logic.

If applications require detailed interpretation of output data, as in image analysis, then some form of error control is warranted. The MC10905 16-bit EDC is based on a modified Hamming code that allows full single-bit correction and double-bit detection of errors. Bit-slice operation is expandable to 96-bit words. The MC10905's separate input and output buses, data latches, check bits, and

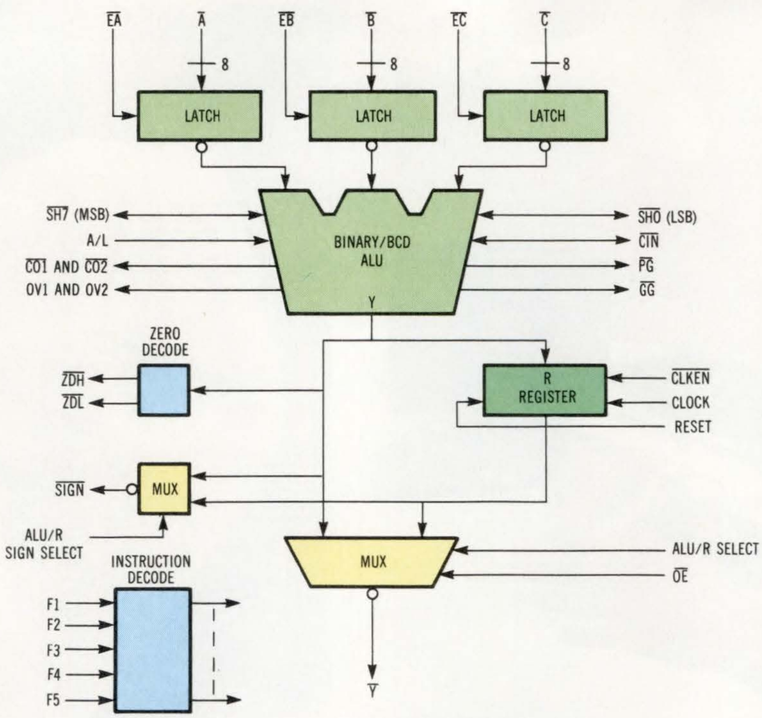

Fig 4 The high speed MC10902 ALU operates on three 8-bit data inputs with an instruction set of 32 functions. Maximum time for addition is 18 ns. Internal zero detection and separate sign bit outputs support direct application of status-bit operations.

error flags allow full support of high speed systems. For 32-bit data, two MC10905 EDCs are required, and 7 check bits are generated. Four modes of operation are possible: read and check, read and correct, generate, and diagnostic. Each of these modes is used in the 32-bit application. A read and check mode is used on the X and Y data as it is accessed for calculations. The read and correct mode is used for external data outputs. The generate mode is applied to floating point results and external data inputs. And, of course, the test lines allow the diagnostic mode to be exercised.

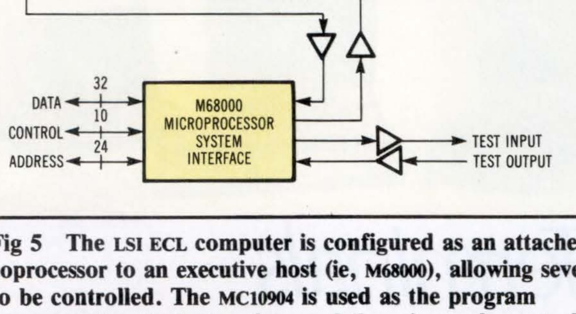

Fig 5 The LSI ECL computer is configured as an attached coprocessor to an executive host (ie, M68000), allowing several to be controlled. The MC10904 is used as the program sequencer for the instructions and the microcode control.

The input as well as output of data to the processor take two forms. The difference between the forms is in the method of handshaking. The test I/O method is non-real time, asynchronous and controlled externally by a host computer. This I/O method is used for performance simulations and its placement simplifies testing. Simple testing allows an I/O check via the EDC, an exercising of the dual RAM, and a thorough testing of the arithmetic functions. Each word of data is transferred when the assertion of an I/O request line is returned with an acknowledge signal. The second method of data transfer is in real time and controlled by sync pulses indicating the beginnings of data batches. Minimal handshake and execution overhead characterizes this method, but the external digital environment must transfer data at an identical high rate.

User access

The module that ties the high speed data processing power of the arithmetic and memory modules to a user accessible environment is the control-interface module. To the host system, the LSI ECL computer appears as an attached coprocessor. Shown in Fig 5, the module consists primarily of three subsections: program processor, microcode processor, and system interface.

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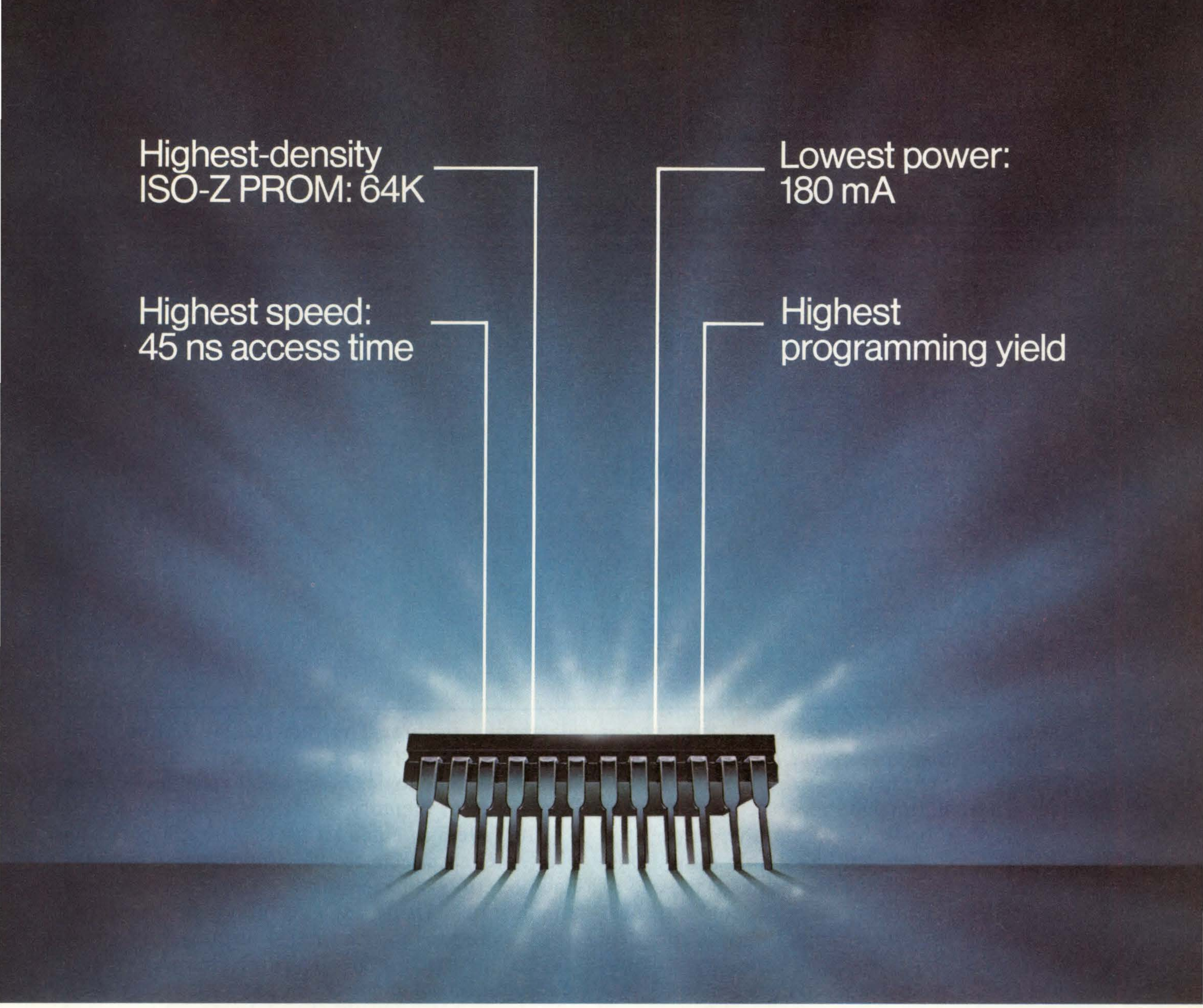

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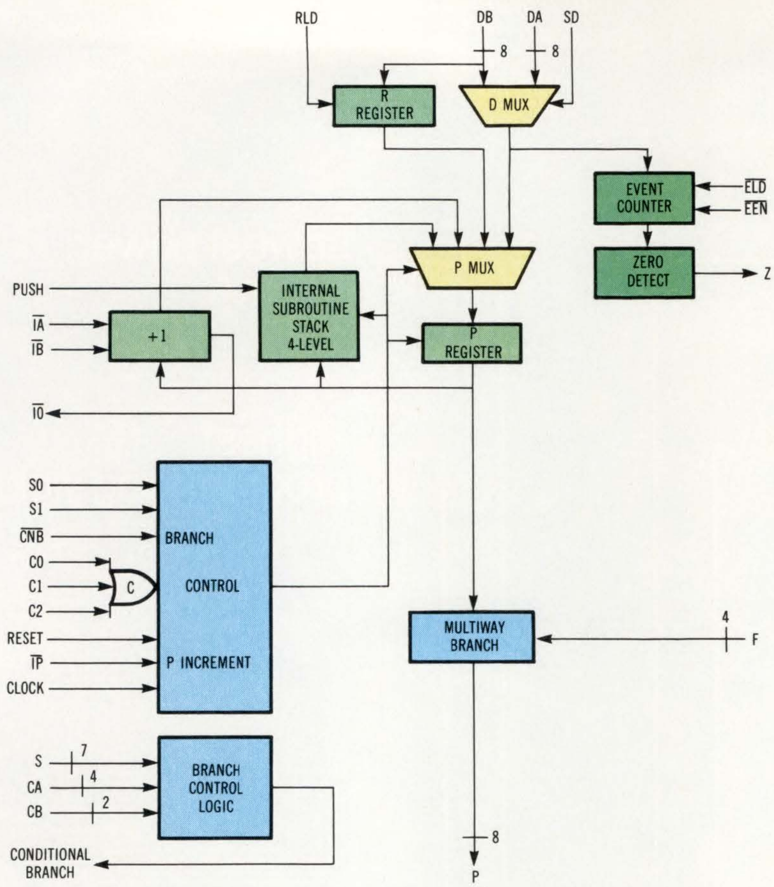

Fig 6 The MC10904 microcode sequencer controls program execution by generating an 8-bit address. The branch control logic allows a complete conditional branching capability, and the use of the "F" lines allows case branching.

The microcode processor executes a sequence of microcode controls in response to an instruction, much like a subroutine is executed in response to a main program call statement. Microcode is repeated for vector operations based on the value of a vector-length register and a simple conditional branch microcode instruction located at the end of each sequence. The MC10904 microcode sequencer slice of Fig 6 is versatile enough to house complete conditional branching and event counting operations internally. Six branch condition inputs combine into 14 logic patterns, minimizing the need for external branch control logic. An internal 8-bit event counter can repeat specific instructions or sequences.

In the program processor subsection, the MC10904 performs as a program counter register. The MC10904 supports several modern programming conventions. Two direct data inputs, DA and DB, provide jump, conditional branch, and subroutine cell destinations. An internal four-level subroutine stack eliminates the need for external logic to handle limited-stack applications. "F" control lines gate the bottom four program addresses to enable up to 16-way case branching. Controlling the $\overline{IA}$ and $\overline{IB}$ increment enable signals allows diagnostic testing of individual instructions.

The system interface attaches the high speed processor to an executive controller for non-realtime computing, program/microcode downloading, and diagnostic testing. The interface is simple, consisting of ECL/TTL translators, data latches, and address decode logic. It appears to the host system as a block of memory locations.

The system-oriented MC109XX IC family offers an alternate approach to the traditional hardwired method of implementing high speed computing applications. Using LSI ECL in system design has the advantages of shortened propagation delay times, increased logic densities, reduced power consumption, and consistent logic structures. New circuits are being identified and developed to expand the family. Exponent processors, address computation units, and activity detection units are some of the proposed candidates for MCA I implementation. Additionally, with the MCA II ECL array introduction, another family of computer-oriented ICs is being developed. With subnanosecond speed and LSI logic density, the MC109XX, and future array-based products, many opportunities exist for ECL logic design.

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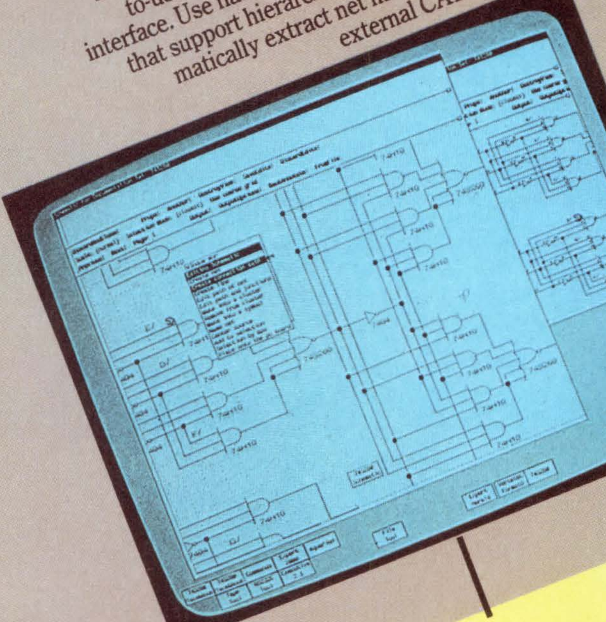

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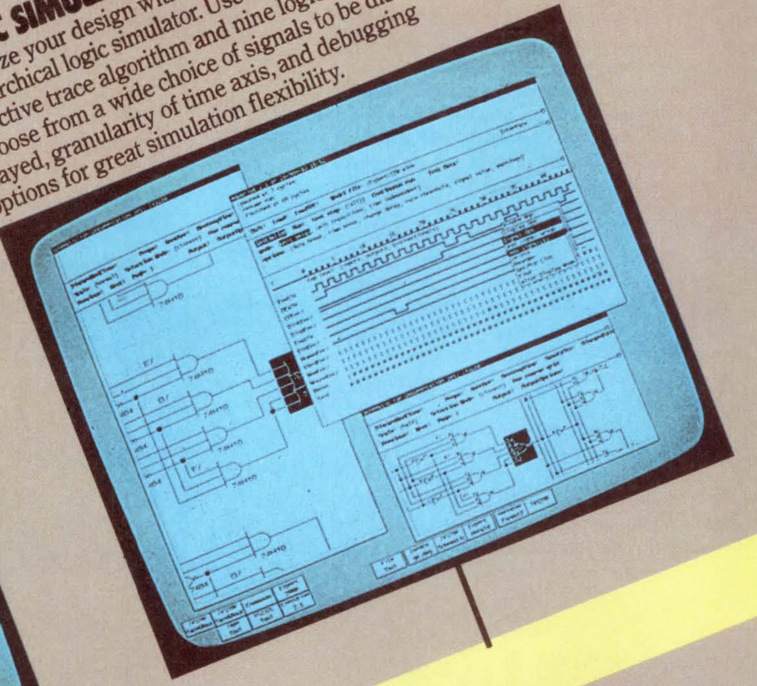

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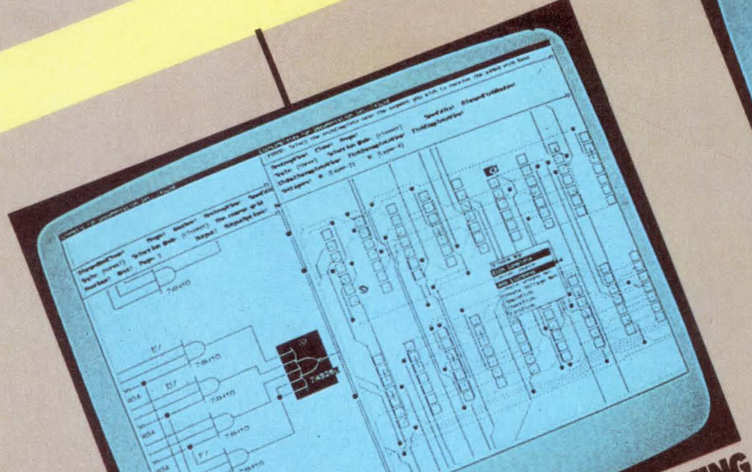

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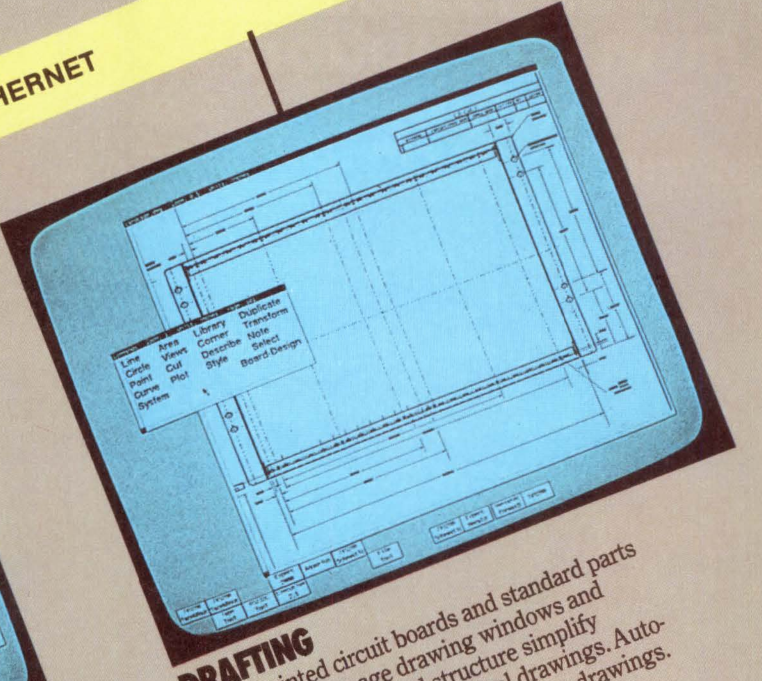

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CIRCLE 49

THE CASE F

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The evidence is persuasive. First, the superior quality of design resides with a team of engineers that has been setting standards in disk controller technology for almost a decade. Quality that continues to be supported by the most sophisticated CAD equipment of its kind in the country. Little wonder, then, that the S1410 reached the market as such a feature-rich offering. With patented VLSI architecture. Industry-standard SASI host bus. Automatic data error detection and correction, seek and position verification, command retry on drive errors, and alternate track capability. Extensive controller and disk drive diagnostics and hardware-selectable sector size. All on one compact PCB that fits the 5.25″ form factor.

Translating a superior design into superior finished goods leads us to submit *"The Case For Quality's"* second major piece of evidence: Superior quality of manufacture. This evidence includes the use of the most sophisticated and automated production facilities in the industry. A $20 million investment in computer-aided manufacturing, from advanced robotic devices to automatic insertion equipment to ATE.

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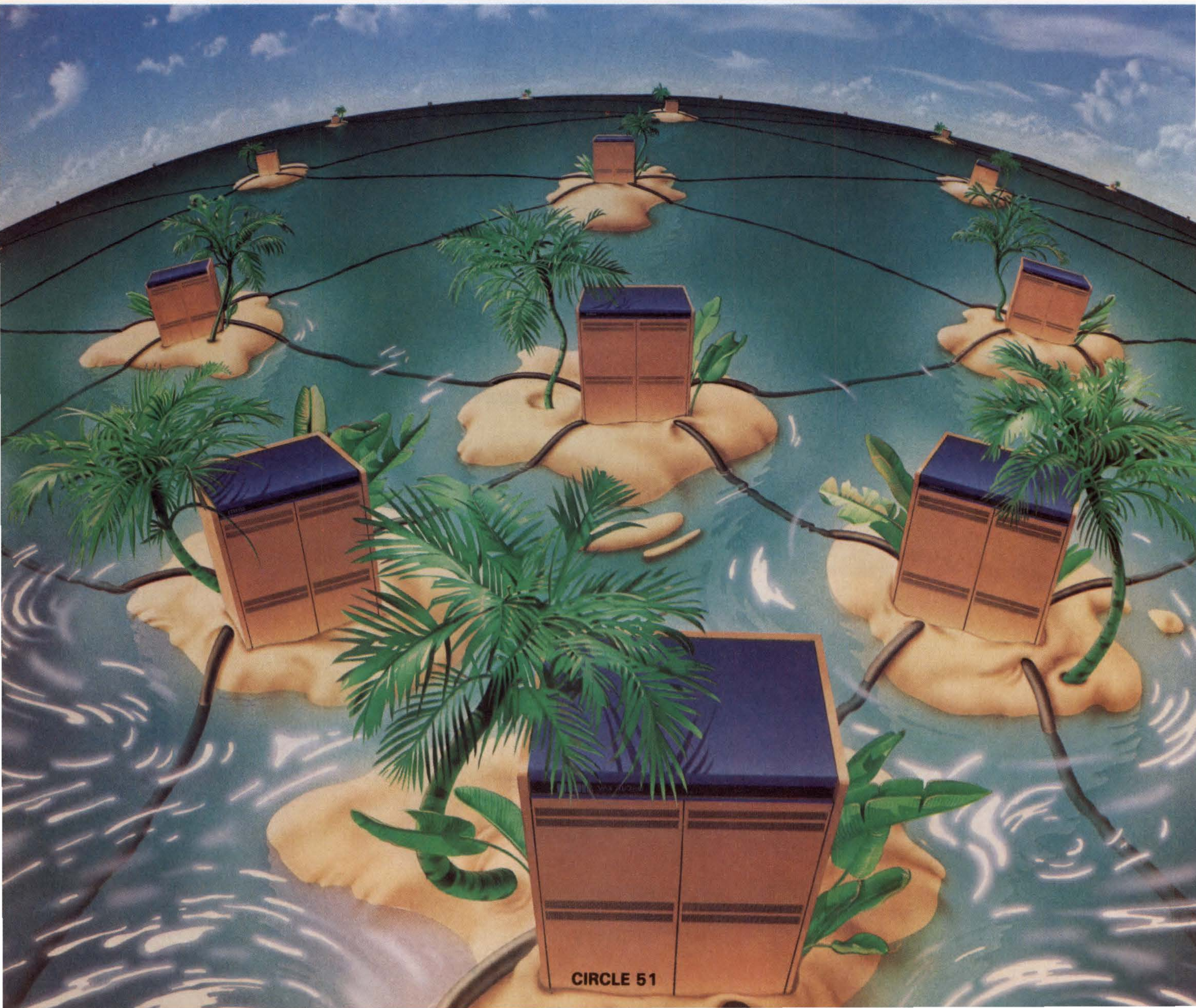
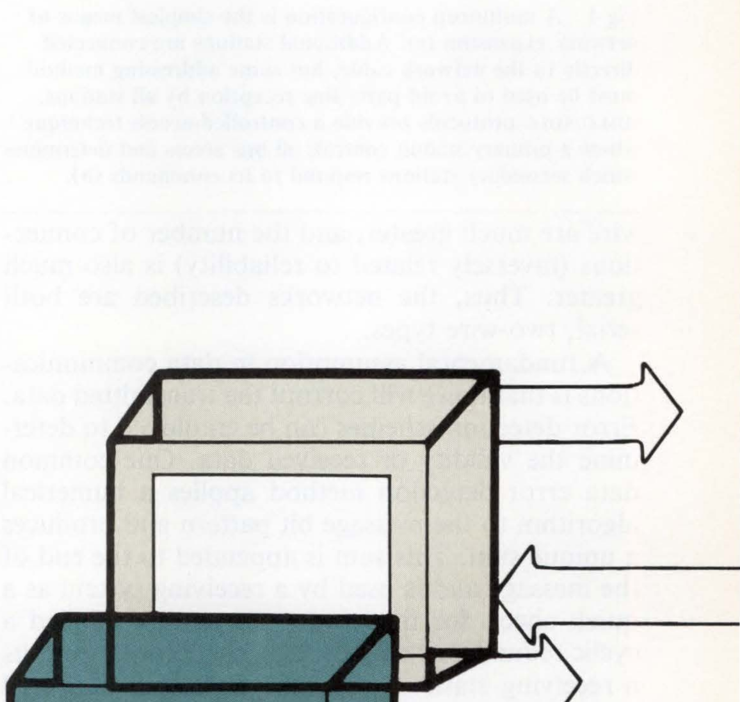


CHIPS SUPPORT TWO LOCAL AREA NETWORKS

Data communication ICs permit easy implementation of Ethernet and high level data-link control networks.



by Bob Dahlberg

All else being equal, networks supported by available LSI and VLSI components exhibit cost and development speed advantages over board-based LANs. Now, available chips support both priority-based and equal access schemes. One such network is based on the IEEE 802.3 specification, while another uses a variety of physical interface schemes overlaid by high level data-link control/synchronous data-link control (HDLC/SDLC) protocols.

The main rationale for local networks is resource sharing. Today, small, powerful computers using VLSI components sell for less than $2000. Under the circumstances, companies intending to use several such systems are reluctant to equip each one with a disk drive and printer that could more than double the price per station. Rather, they prefer to share disks and printers among several systems in order to spread the cost of peripherals across several users.

By connecting these small computers to a local area network (LAN), resource sharing with little degradation in overall system performance becomes practical. However, if the network interface costs $1000 or more per computer, the economic advantage of resource sharing wanes. Thus, network interface cost is a primary criterion in selection, particularly for low cost computers.

Access methodologies represent another important factor in network selection. And, although an equal access, first-come, first-served method might be appropriate for an office system environment, it could be the curse of a process control system. In the latter case, a priority-based (or controlled) access method might be the only realistic choice.

Bob Dahlberg is a product manager responsible for local area network components at Intel Corp, 3065 Bowers Ave, Santa Clara, CA 95051. He holds a BS in electrical engineering and computer science from the University of California, Berkeley, and an MBA from the University of Chicago.

Costly copper

In short distance networks, one can choose a serial, two-wire scheme or a parallel, multiwire interface. Parallel bus structures are implicitly faster than serial structures but tend to be more expensive and less reliable. The amount and cost of the copper

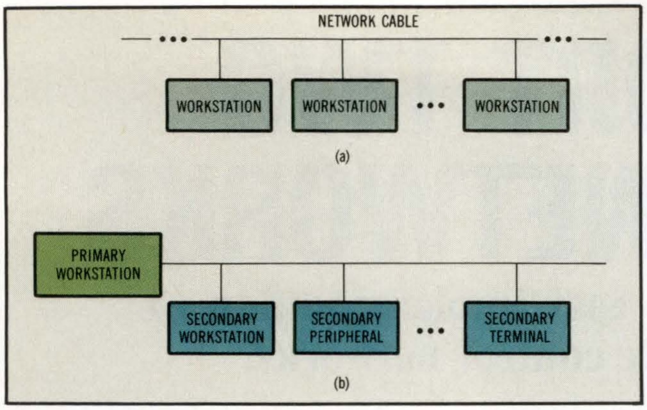


Fig 1 A multidrop configuration is the simplest means of network expansion (a). Additional stations are connected directly to the network cable, but some addressing method must be used to avoid party-line reception by all stations. HDLC/SDLC protocols provide a controlled-access technique where a primary station controls all bus access and determines which secondary stations respond to its commands (b).

wire are much greater, and the number of connections (inversely related to reliability) is also much greater. Thus, the networks described are both serial, two-wire types.

A fundamental assumption in data communications is that noise will corrupt the transmitted data. Error detection schemes can be employed to determine the validity of received data. One common data error detection method applies a numerical algorithm to the message bit pattern and produces a unique sum. This sum is appended to the end of the message and is used by a receiving system as a quick check for the proper bit pattern. Called a cyclic redundancy check (CRC), this process permits a receiving station to discard erroneous data and request retransmission. If the message frames are sequentially numbered, the retransmission request can be made specific to that frame to dispense with the request for a larger group of data. Thus, the process can be made more efficient.

As needs grow, users may want to add more workstations and intelligent peripherals to a network. It would be ideal to attach each station to the network by simply connecting the station directly to the serial network bus cable. This is called a multidrop configuration and it resembles a party line telephone circuit [Fig 1(a)]. As a party line, each station attached to the cable receives all the data transmitted on the cable. In order to route messages to their intended recipients, the messages are logic switched, or specifically addressed, to one or more receiving stations. All others will ignore the data after learning that no match existed between their addresses and those of the data being sent.

Each data packet or frame contains a set of address bits that determines which stations receive the data. In a sense, address bits constitute overhead because they are not part of the information being sent between stations. Any loss in data transfer efficiency, however, is made up by the simplicity of the network expansion interconnect scheme.

The Ethernet specification (a modified version of which was recently accepted as IEEE standard 802.3) describes its physical link characteristics in full detail. Coaxial cable is used as the network cable bus, and each station is connected to that cable via a transceiver and transceiver cable. Minimum distance between station transceivers is 2.5 m, and a network segment can extend to 500 m (and contain up to 200 nodes). Because up to five segments can be joined using active repeaters between each segment, the overall Ethernet network can be 2500 m long and support up to 1000 nodes. Individual nodes can connect to more than one station, and the number of stations connected to an Ethernet network can exceed 1000.

Data is sent at a 10-Mbit/s rate using a self-clocking Manchester encoding format. Only one data packet can be sent at a time using Ethernet, and access is on a first-come, first-served basis. Carrier sense multiple access/collision detection (CSMA/CD) methodology is used. The maximum and minimum distances between transceivers are derived from the CSMA/CD requirements based on interframe-spacing and the collision detection procedures.

A second alternative requires no specific physical link. Speed, distance, and cost parameters dictate actual implementation. The simplest and least expensive method is to drive a twisted-pair cable with off-the-shelf transceiver chips.

Choosing protocols

Both the IEEE 802.3/CSMA/CD and the HDLC/SDLC protocols provide logic-switched messaging and frame-by-frame error detection. IEEE 802.3/Ethernet treats each station equally and does not permit priority network access, whereas HDLC/SDLC enforces a primary/secondary hierarchy [Fig 1(b)]. A primary station controls the overall network by issuing commands to the secondary stations. Secondary stations comply with the primary station's commands and access the bus for retransmitting data only in response to those commands. Unlike Ethernet, which is based on probabilistic network access, HDLC/SDLC provides deterministic (or controlled) access.

SDLC is an IBM standard communication protocol and a subset of HDLC, a standard communication link control established by the International Standards Organization (ISO). HDLC and its subset are data-transparent protocols, which means the arbitrary data streams can be sent without concern that some of the data might be mistaken for control characters. Thus, unlike the Bisync protocol and its controller, an HDLC/SDLC controller need not detect special characters except for the unique opening/closing flag bytes. Moreover, unlike an

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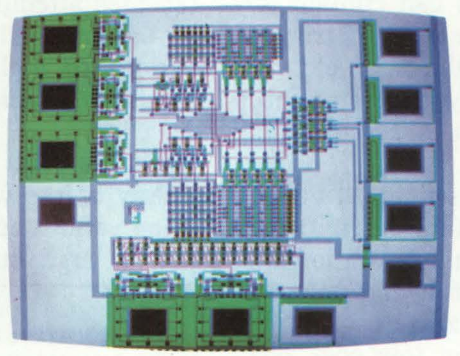

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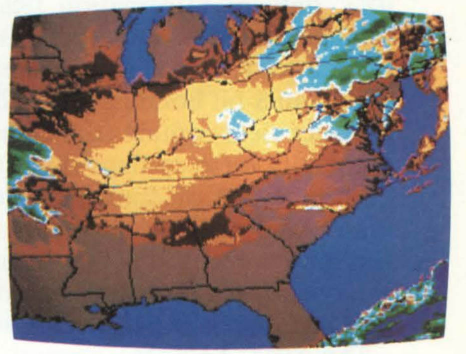

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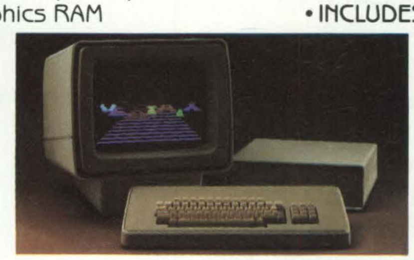

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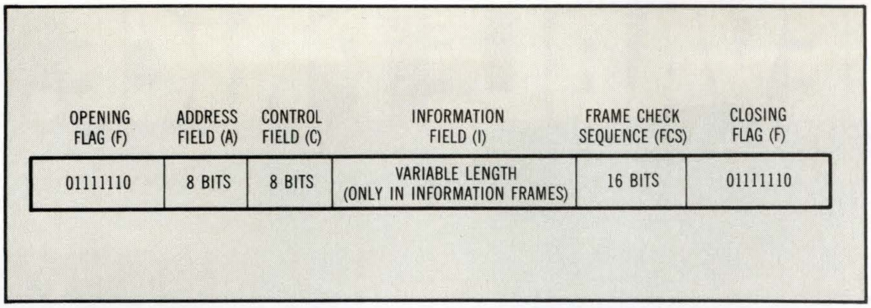

Fig 2 The prescribed format for HDLC/SDLC frames consists of four basic fields bounded by opening and closing flags. This avoids the need for start/stop bits often used in asynchronous protocols.

asynchronous protocol and its controller, the HDLC/SDLC need not provide start and stop bits.

Both HDLC/SDLC and Ethernet protocols specify particular message formats (or frames). The HDLC/SDLC protocol consists of five basic fields—flag, address, control, data, and error detection. Each frame is enclosed by an opening and closing flag. Both the opening and closing flags form a similar bit sequence—01111110—that is an individual character in SDLC/HDLC. Inserting a 0 in the information data flow whenever a sequence of five 1s occurs achieves flag character individuality in SDLC/HDLC. These inserted 0 bits are automatically stripped out upon reception. For SDLC, the address field is 8 bits wide, but can be 2 (or more) bytes long in HDLC. Similarly, the control field in SDLC is 8 bits wide, but can also be longer in HDLC. The SDLC data or information field can contain any number of bytes. However, the same is true for HDLC in certain instances where the data field must end on an 8-bit boundary. Finally, the frame check sequence field contains the 16-bit CRC result for all of the bits between flags (Fig 2).

Three types of frames are used in HDLC and SDLC. A nonsequenced frame establishes initialization and control of the secondary stations. A supervisory frame handles control, and an information frame is used for data transfers.

The SDLC protocol appears in low cost asynchronous modems using nonreturn to zero inverted (NRZI) coding and decoding. NRZI coding is used at the transmitter to enable clock recovery from data at the receiver terminal. Clock recovery is accomplished using a digital phase locked loop technique. NRZI coding specifies that the signal condition does not change for transmitting a 1, but changes state whenever a 0 is transmitted. Hence, NRZI coding ensures that an active data line will have a transition at least every 6 bit times (by virtue of the 0-bit insertion requirement). Both 0-bit insertion and NRZI coding/decoding maintain the data transparency characteristics of the HDLC protocol and its SDLC subset.

Like HDLC/SDLC, Ethernet specifies a frame format (Fig 3). It contains a destination field, source field, frame type field, data field, and a frame check sequence. The destination and source fields both contain 6 octets (8 serial bits), for a total of 48 bits. The type field contains 2 octets. The data field can have as few as 46 octets or as many as 1,500. Finally, the frame check sequence consists of 4 octets, allowing a 32-bit CRC code to be calculated and appended to the rest of the frame. The first transmitted Ethernet frame is preceded by a 64-bit preamble, made up of seven groups of 10101010 followed by an eighth group of 10101011. The next bit that follows is the first bit of the first destination octet.

In the CSMA/CD scheme, a "collision" occurs when two stations attempt to gain access to the bus at the same time. Thus, it is important that all stations on the network are notified of the collision. This way, any transmitted data can be flagged as invalid. To solve this problem IEEE 802.3/Ethernet specifies that, after collision detection, transmitting stations send a jam signal to ensure that stations on the network recognize the collision. At the end of the jam interval, each station delays bus access according to an individually calculated random backoff time interval. Should a collision occur again when bus access attempts are renewed, the next backoff interval increases in length. Up to 16 repeated attempts can occur before a system fault is automatically assumed. Thus, even during periods of high bus demand, ample bandwidth should be available and delays relatively short.

It's in the chips

Any of the working LANs can be implemented using various components. If there is enough time and a large budget, custom VLSI chips can be

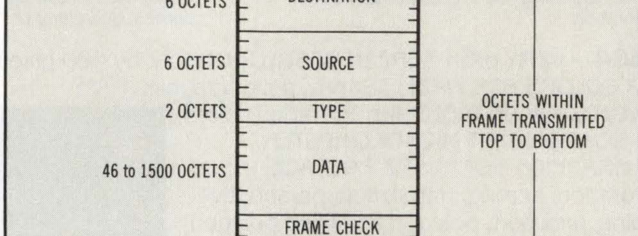

Fig 3 Each Ethernet frame consists of five fields. Destination and source fields indicate where the message is going and from which station it originated. The data field can contain as few as 46 bytes of data and as many as 1500.

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CIRCLE 53

developed and an elegant solution forged. Most engineers, however, have neither luxury. For this reason, the two networks selected are supported by off-the-shelf VLSI components.

Intel's 8273 and 8274 data communication controller ICs offer HDLC/SDLC capabilities. Teamed with a microprocessor and some random logic ICs, a capable network data-link controller could be built. The 8051 single-chip microcontroller has become a popular component for many terminal applications because of its high performance 8-bit CPU, large internal program and data memory capacity, plus onchip counter timers and interrupt controllers. In addition, Intel has combined an intelligent HDLC/SDLC controller and 8051 core processor onto a single chip, the 8044. The resulting single-chip microcontroller with onchip serial communication controller allows low cost network terminal and peripheral design.

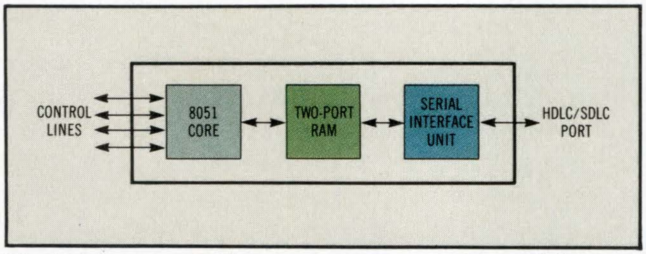

Fig 4 The 8044 combines an 8051 CPU, program and data memory, plus HDLC/SDLC controller on a single chip to build a simple, low cost network station or peripheral.

Each station would contain an 8044 (with its programmable I/O ports to provide local control) and serial HDLC/SDLC interface. Thus, to manage the network interface, 8044-based stations would be capable of acting as a secondary station within an HDLC/SDLC network (Fig 4). Since data transfer speed and electrical characteristics are not specified for these protocols, the designer has a wide choice in tailoring the physical link to the application. The single VLSI device provides local intelligence and network management, thus permitting low cost network development.

Various Ethernet controllers have been announced, with several already sampled and available. Among these is the 82586 general-purpose CSMA/CD controller. It is designed to come up in the Ethernet mode on power up, but can be programmed for other parameters as well. A companion chip (the 82501) provides the Manchester encoding/decoding function between the 82586 and a transceiver.

This chip pair operates in conjunction with the iAPX 86 microprocessor family, and is most cost-effectively used with the 80186 microprocessor. The 80186 and 82586 have identical bus interface and control signal requirements. Hence, they can be linked without adding random logic ICs. Essentially, these three ICs—the 80186, 82586, and 82501—provide the basis for an Ethernet interface. Therefore, only some buffer memory and bus interface chips are additionally required (Fig 5).

A subsystem built using these components provides an intelligent Ethernet interface that can continuously operate at the full 10-Mbit/s network speed. Moreover, these components can implement a complete computer and communication system. It is therefore possible to create an appropriate and usable Ethernet workstation out of these few VLSI components.

Different strokes

The HDLC/SDLC-based network is intended for non-Ethernet applications. HDLC/SDLC has become an accepted standard supported by a variety of hardware and software products. There is no specified standard for physical link implementation or for the software layers beyond the data-link level. Therefore, networks based on these protocols are usually "closed." That is, the vendor provides all the pieces to the network. Vendors, of course, are familiar with their own network architecture and are free to provide compatible systems. But such networks do not encourage others to develop compatible systems unless the vendor's market share is large enough and vulnerable enough to attract competition. The IBM SNA is an example.

HDLC/SDLC-based LANs are suitable for system clusters where distances are less than those of Ethernet, and where priority access is important. Networks within a box (eg, a copier), and networks on table-tops (eg, an instrumentation cluster), are examples. Although there is a parallel bus interface standard (IEEE 488), an instrumentation manufacturer may want to provide for longer distances using two-wire cables and simpler protocols.

An HDLC/SDLC LAN cluster could also be used for process control applications and data acquisition systems. An example is Intel's recent distributed control module products for the factory. Again, a priority bus access capability would be important in these applications. Office system applications where Ethernet offers too much performance at too high a cost (eg, an electronic typewriter networked to a file server) might use this network as well.

The concept of open-system compatibility comes from the ISO's Open System Interconnection (OSI) model. This provides a seven-layer model in which each layer is characterized by a unique set of functions and a specific interface to adjacent layers. The goal is to eventually arrive at a set of standards that would permit systems from several vendors to communicate with one another through common physical, data-link, and software layer protocols.

Xerox Corp developed Ethernet as a local network for its systems, but the company later joined with Digital Equipment Corp and Intel to develop a set of specifications for Ethernet that would allow it to

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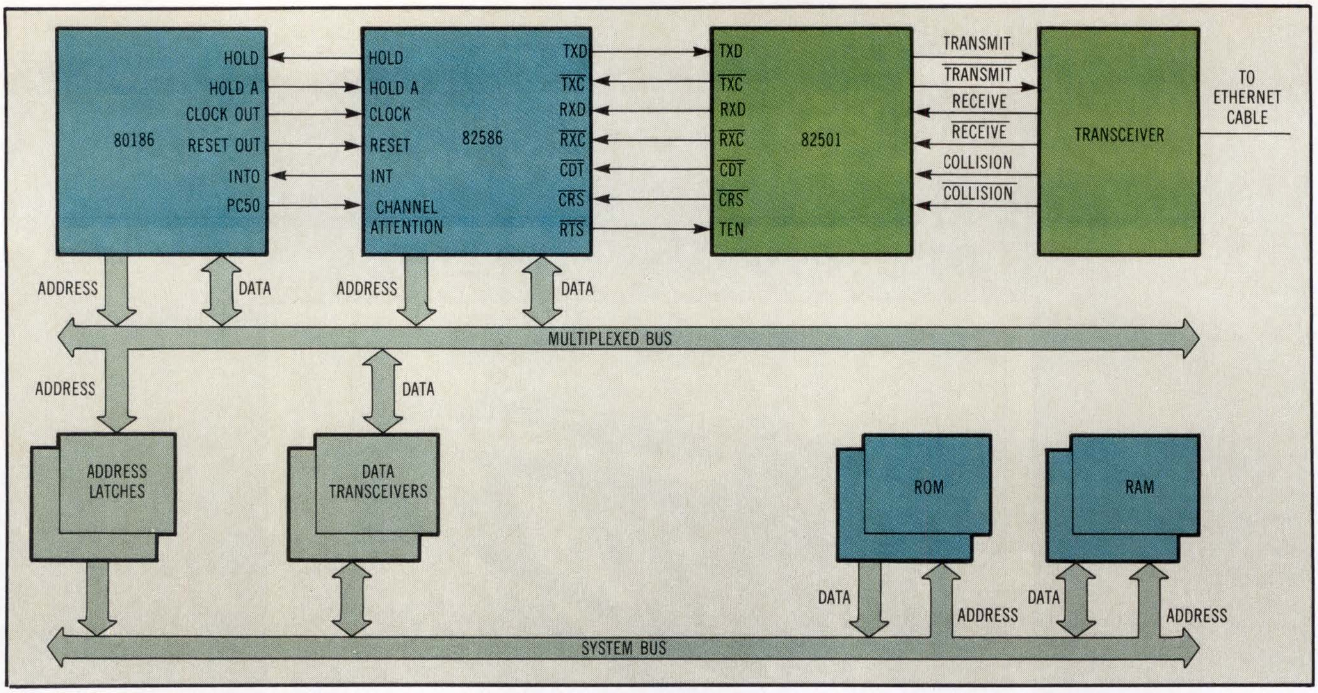

Fig 5 A combination of 80186, 82586, and 82501 chips completes the logic needed for a fully functional Ethernet interface. Data bus interface chips and some memory complete the Ethernet subsystem.

map into the first two layers of the OSI model—physical and data-link. The IEEE adopted its 802.3 specification as a result of these efforts. Efforts to develop standards for the other layers continue. An example is the ISO transport layer protocol, 8073, which provides "return receipt" quality communication services.

Today, Ethernet supports OSI physical and data packet level protocols. It is an emerging technology that is still closer to the top than to the bottom of the learning (and pricing) curve. Nevertheless, many vendors support Ethernet and will no doubt manufacture products equipped to swap data with other Ethernet systems.

Open and closed

Office automation constitutes the biggest apparent application area for Ethernet. The office has traditionally been a multivendor site in which the computer, copier, and printer are likely to come from different vendors. An open system appeals to users seeking vendor independence.

When the LAN concept was first proposed, it was described as an all-encompassing network, connecting all the intelligent subsystems throughout a facility. In fact, that is not the way local network installations have progressed. Instead, clusters of user stations (typically 10 or so) are cropping up in various places within a facility. Most analysts expect local networking to occur in tiers. The cluster tier provides the lowest cost per connection. An example is a 1-Mbit/s CSMA/CD LAN used for personal computers. Clusters would be interconnected through a longer and faster data highway (called a LAN backbone) such as Ethernet.

Will closed and open networks be able to cooperate and coexist? Quite simply, they have to. Economics will determine the network types used for connecting the systems within a cluster, and standardization will drive the methods by which clusters are ultimately joined.

Closed systems, such as microcontrollers connecting the HDLC/SDLC-based network, represent the least expensive and most flexible LAN configuration. Open systems, because of the push for standardization and subsequently larger user base, are more likely to benefit from future cost reduction through multiple-sourced VLSI components than closed systems. Similarly, open systems probably attract more third-party suppliers and enjoy greater variety and lower cost software.

Gateways will join closed and open systems. These hardware/software intermediaries will pave the way for data transfer between formerly incompatible networks. By such means, a closed engineering workstation network will gain access to information stored in the corporate data base and be available on the Ethernet data highway.

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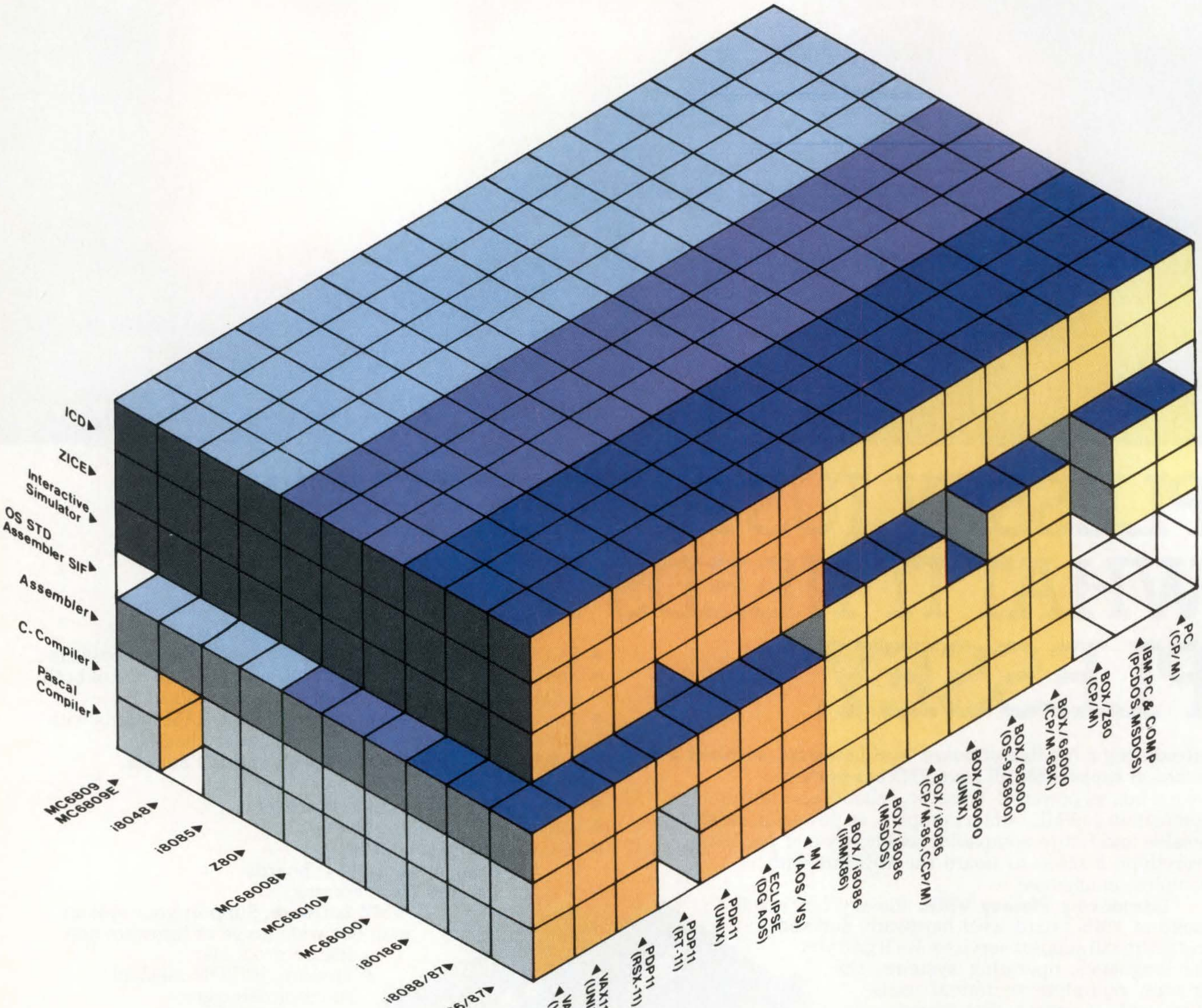

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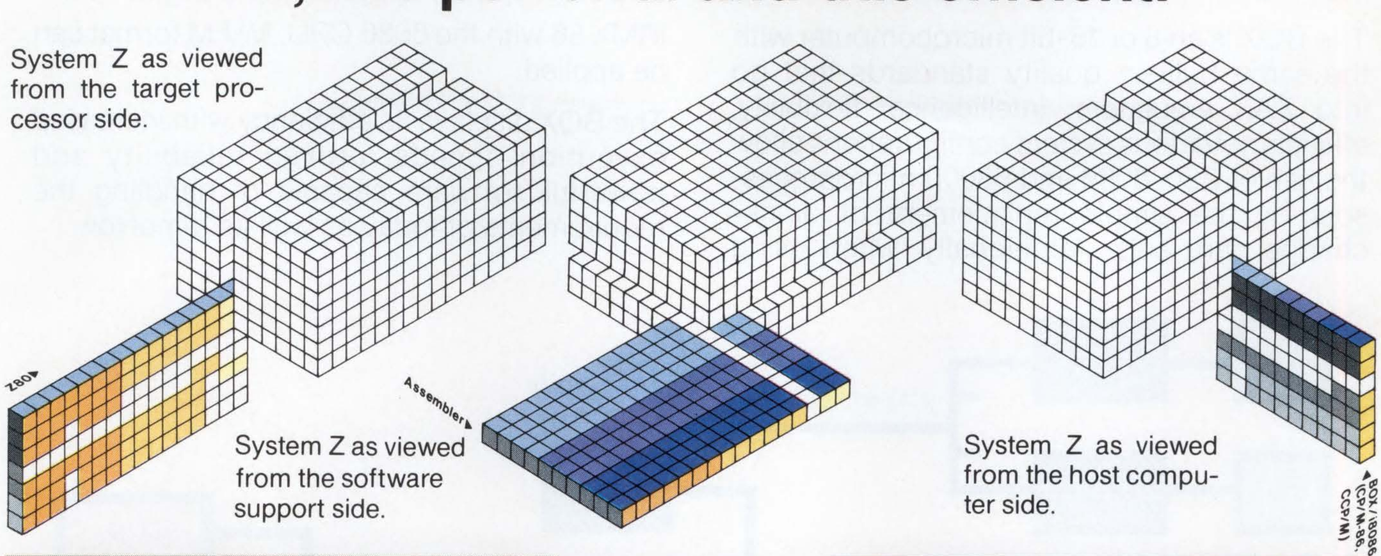

System Z as viewed from the target processor side.

System Z as viewed from the software support side.

System Z as viewed from the host computer side.

SYSTEM-Z List

HOST SYSTEM	Minicomputer System Series							BOX System Series							PC Series	
	VAX 11		PDP 11			ECLIPSE	MV	BOX/i8086			BOX/68000			BOX/Z80	IBM PC IBM PC COMP	PC
	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86

HOST SYSTEM	Minicomputer System Series							BOX System Series							PC Series	
	VAX 11		PDP 11			ECLIPSE	MV	BOX/i8086			BOX/68000			BOX/Z80	IBM PC IBM PC COMP	PC
	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86

■ i8086/87 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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■ i8088/87 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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■ i80186 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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■ MC 68000 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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■ MC 68010 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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■ MC 68008 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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E	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
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■ Z80 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
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B	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
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E	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
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G	●	●	●		●	●	●	●	●	●	●	●	●			

■ i8085 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
A				●							●				●	
B	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
C	●	●	●		●	●	●									
D														●		
E	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
F	●	●	●		●	●	●	●	●	●	●	●	●			
G	●	●	●		●	●	●	●	●	●	●	●	●			

■ i8048 Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
A				●							●				●	
B	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●	●
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D														●		
E	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
F																
G																

■ MC 6809-09E Development System

	VMS	UNIX	RSX11	RT11	UNIX	DG AOS	AOS/VS	iRMX86	MS DOS	CP/M86 CCP/M86	UNIX	OS-9 /68000	CP/M68K	CP/M80	PC DOS MS DOS CP/M86	CP/M86
A				●							●				●	
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D																
E	●	●	●	●	●	●	●	●	●	●	●	●	●		●	●
F	●	●	●		●	●	●	●	●	●	●	●	●			
G	●	●	●		●	●	●	●	●	●	●	●	●			

- A — ICD In-Circuit Emulator Debugger
- B — ZICE ICD's System Software
- C — Interactive Simulator
- D — OS STD ASM
- E — Assembler
- F — C-Compiler
- G — Pascal Compiler

SYSTEM Z-from Z...ing

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CIRCLE 56

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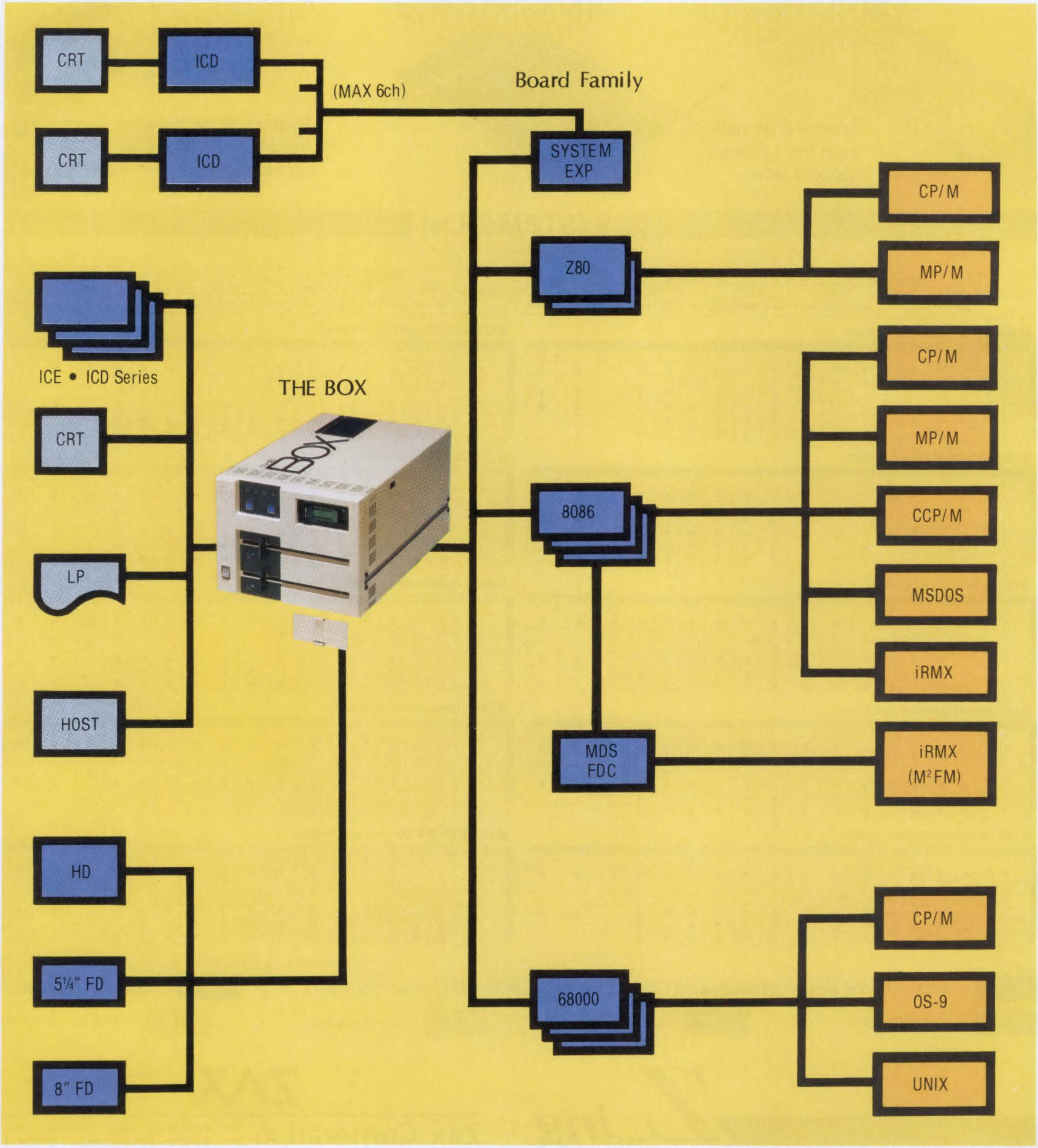

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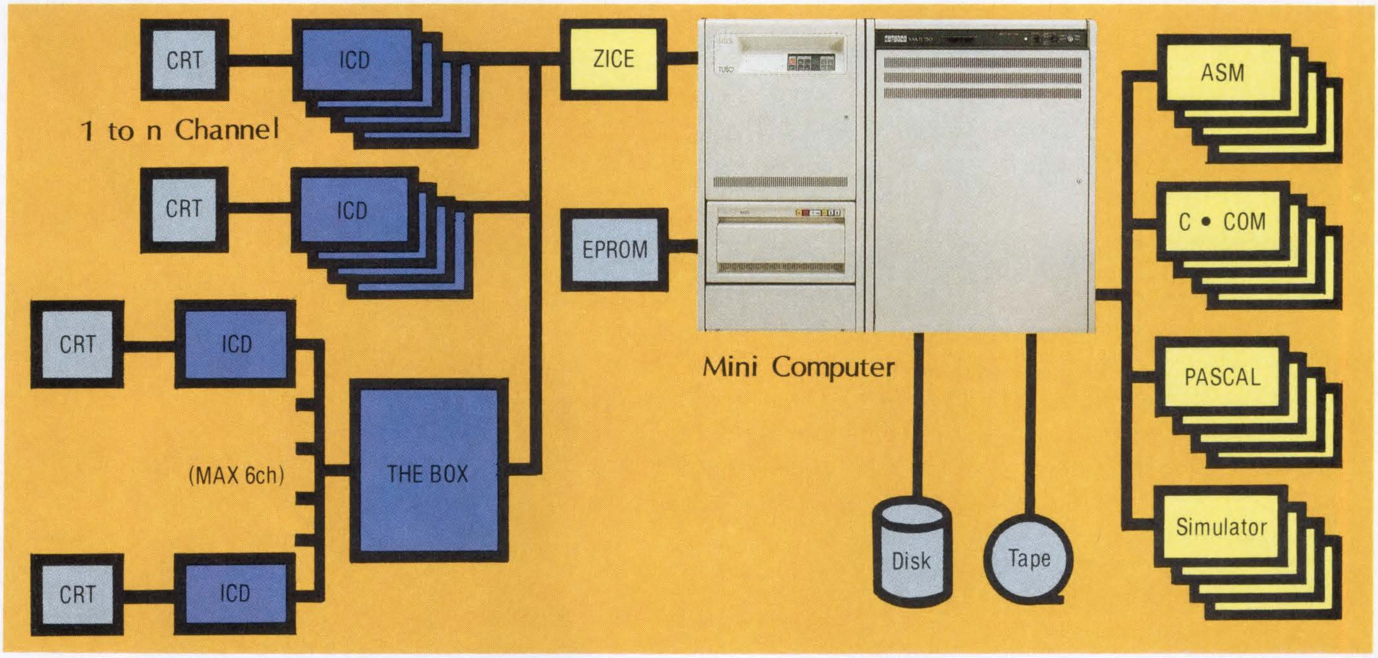

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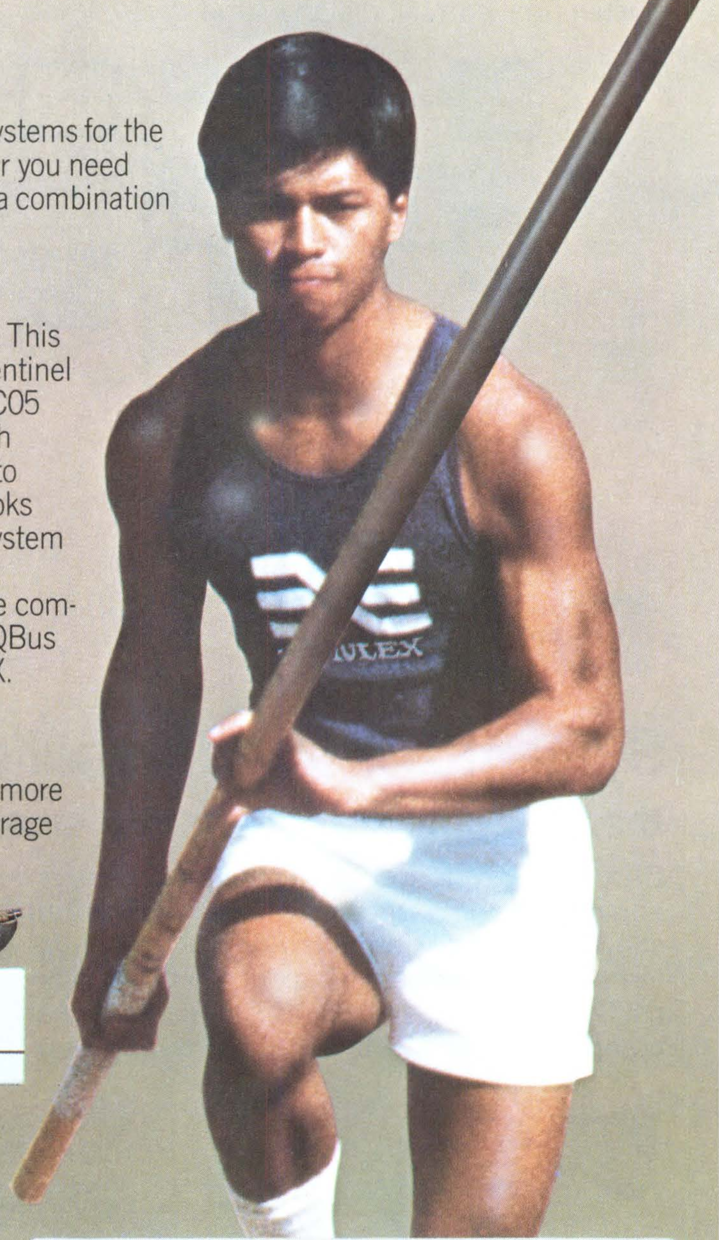

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CIRCLE 58

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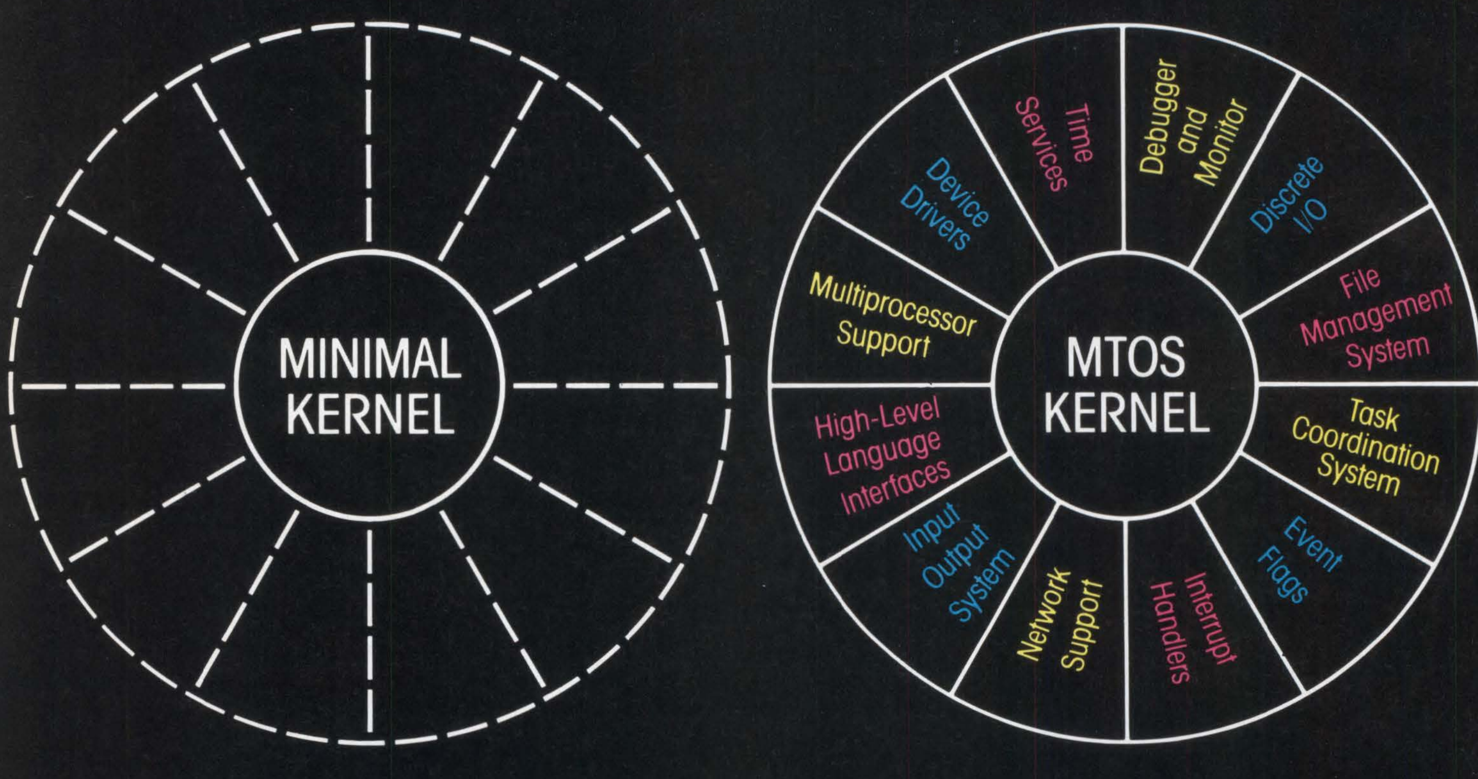

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- **MTOS-68KFG** firmware generator
- **MTOS-68KF** firmware
- **MTOS-80MP** for the 8080/85
- **MTOS-80** for the 8080/85
- **MTOS-68** for the 6800

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CIRCLE 59

DISK TRANSLATION SOFTWARE SOLVES FORMAT MISMATCHES

To provide software in a variety of floppy disk recording formats, a translation utility is needed. This, however, requires an understanding of formatting basics.

by George Mitchell, Contributing Editor

For an industry that relies heavily on standards, floppy disk recording formats have many incompatibilities. Specifically, there are more than 70 different recording schemes for 5¼-in. diskettes. Moreover, with the rise in microfloppies under 5¼ in., similar incompatible formats will surface.

One solution to the disparity in formats is a format translation utility. Translation utilities are based on the machine's controller chip, the skew (interleave) factor of the sectors on the diskette, the disk parameter block (which defines the various elements of the format), and the operating system.

Some companies have made progress in accommodating different formats. For example, Advanced Computer Technology Inc's (San Diego, Calif) Diskwriter (formerly Pirate) system accommodates 38 different formats. Vertex Systems Inc's (Los Angeles, Calif) Xeno-Copy is a software utility (designed for operation on the IBM PC and XT) that can read 23 different formats. While Xeno-Copy does not support formatting and writing functions at present, those capabilities will be added. Micro Solutions Inc's (Dekalb, Ill) Universal Disk Initializer (Uniform) offers users of the Kaypro series of microcomputers the ability to format, as well as read and write 15 different 5¼-in. formats. This utility is broader than most and includes not only the Kaypro format, but also Texas Instruments' professional computer and the CP/M-86 format for the IBM PC.

Translation program basics

Two crucial factors in developing a translation program are the skew and disk parameter block definitions. Normally, these definitions are handled as macros in the operating system's basic I/O system (BIOS). The skew macro, which generates a skew or interleave table, requires the following parameters: the number of physical sectors per track, the skew (interleave) factor, and the first sector number on each track (usually 0 or 1). For example, a typical skew macro for an IBM 3740 single-density, 8-in. diskette would take the following form: SKEW 26,6,1.

The word SKEW is used in the software to label the macro. When the operating system calls this macro, it informs the controller that the diskette consists of 26 interleaved sectors (skewed by 6). Each track starts at sector 1 (Fig 1).

Creating a translation utility

Formats that use built-in skew parameters, rather than letting the operating system establish parameters through the translation table, make developing a translation program even more difficult. However, this format is workable when used in conjunction with such controllers as the Western Digital (Irvine, Calif) WD-1793. This controller reads the disk, prior to performing a READ or WRITE sector, to locate the address mark and the expected gaps between data. Performance can be improved by starting the first sector at the index position on even tracks, and then skipping to odd tracks on a half rotation. Generally, this speeds access by reducing delays caused by rotation latency (as slow as 300 rpm for some 5¼-in. drives).

Since there is no standard for skewing on a diskette, designers implement whatever works for them. Moreover, not all formats even use a skewing technique. Instead, some buffer a full track of data, which speeds perceived access time to the user. Difficulties in creating a translation utility can arise, however, when going from a skewed format to one that is not skewed, or vice versa.

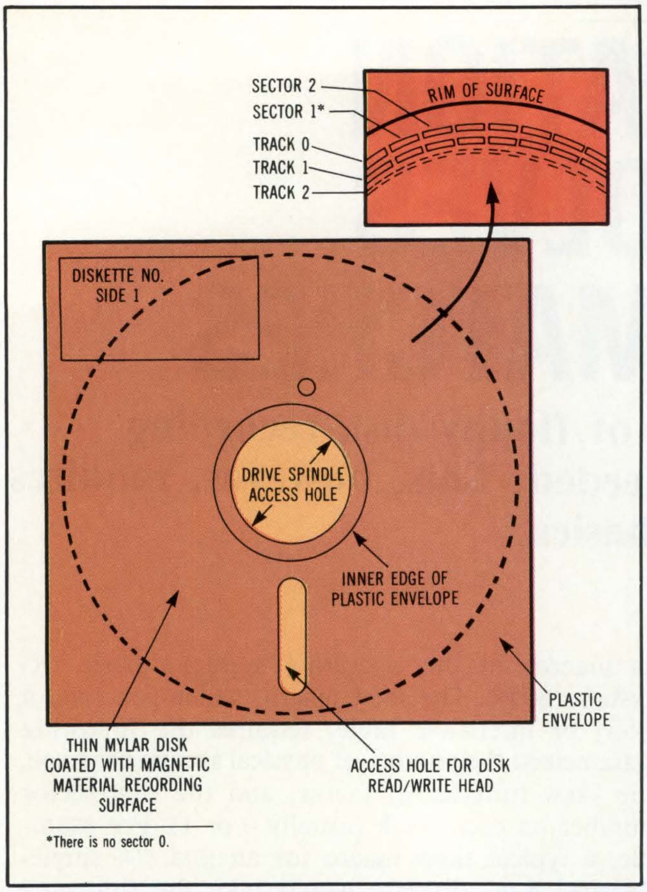

Fig 1 The IBM 3740 format for 8-in. diskettes consists of 77 tracks arranged in 26 sectors of 128 bytes each. To improve throughput efficiency, the sectors are skewed (interleaved) by a given factor, such as 6. The starting sector (0 or 1) coincides with the index mark.

Establishing the correct skewing is only one aspect of creating a translation utility. The disk parameter block (DPB) also plays an important role. The macro establishes the physical layout of the data in relation to the drive's characteristics. This requires the following six parameters: the physical sector size in 128 to 1024 bytes, the number of physical sectors per track (a function of the size in bytes), the number of tracks on the drive, the allocation unit size in bytes (the number of sectors made available per access), the number of directory entries, the number of tracks to reserve, and the number of checked directory entries as an optional parameter.

For the IBM 3740 format, the DPB appears as DPB 128,26,77,1024,64,2. DPB is the macro label. The sectors are 128 bytes in length; there are 26 sectors per track, 77 available tracks, 1024 bytes are allocated on access, 64 directory entries are allowed, and 2 directory entries are checked. Interchange problems would be minimized if all formats consisted of 128-byte sectors on 77-track diskettes. This, however, is not the case.

Increased capacity is the goal of most disk drive manufacturers. One way to double capacity is to crowd more data per sector by increasing the byte count to 256 without reducing the number of sectors per track. In addition, the sectors can be enlarged to 1024 bytes with the number of sectors reduced to 8. Making diskettes double sided further enhances capacity, but also gives the translation utility designer other factors with which to contend. With double-sided diskettes, the translation utility must deal with the skewing of the DPB, the head in operation, and the number of cylinders involved.

While the operating system plays a major role in diskette operation, it has very little impact on how the recording format is laid out. A separate formatting utility, whose operation depends on the choice of controller chip in the system, handles the diskette format.

Solving controller incompatibility

Western Digital's FD 1791X-02 family of controllers can be used in both hard-sector (physical sector holes are punched in the diskette) and soft-sector formats (sectoring is handled via software marks rather than actual holes). This family also supports the IBM 3740 single-density frequency modulation (FM) recording format, as well as a variety of double-density modified frequency modulation (MFM) formats.

These controllers have 8-bit registers that hold information such as the number of tracks and sectors. In contrast, the NEC (Lexington, Mass) PD765 controller, which can also handle single- and double-density formats, uses a memory stack arrangement for holding formatting information.

Although the controllers differ in operation and implementation, they can write the same formats, such as IBM FM or MFM (see Fig 2). Their differences, however, prohibit a format translation program written for a Western Digital controller from working with an NEC device. This would be like trying to use Z80 code with an 8086 microprocessor: the differences in instruction and operation are just too great.

While the operating system plays a major role in diskette operation, it has very little impact on how the recording format is laid out.

Solving controller incompatibility, however, may be possible. Similar to application programs that use an install function to match the application to a given system, an installation procedure for disk-format translation utilities can be built. Creating a universal install program may seem insignificant, but it involves an in-depth knowledge of the various controllers and their implementation.

Implementation techniques for controller chips are as diverse as the number of diskette formats. Memory mapped and port-addressed formats are

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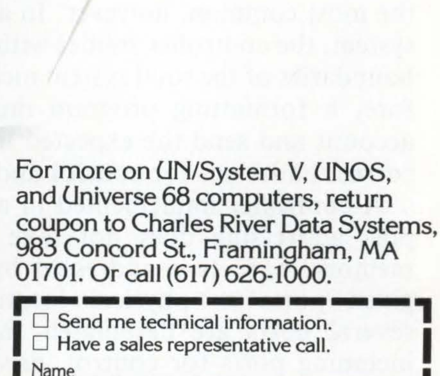

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CIRCLE 60

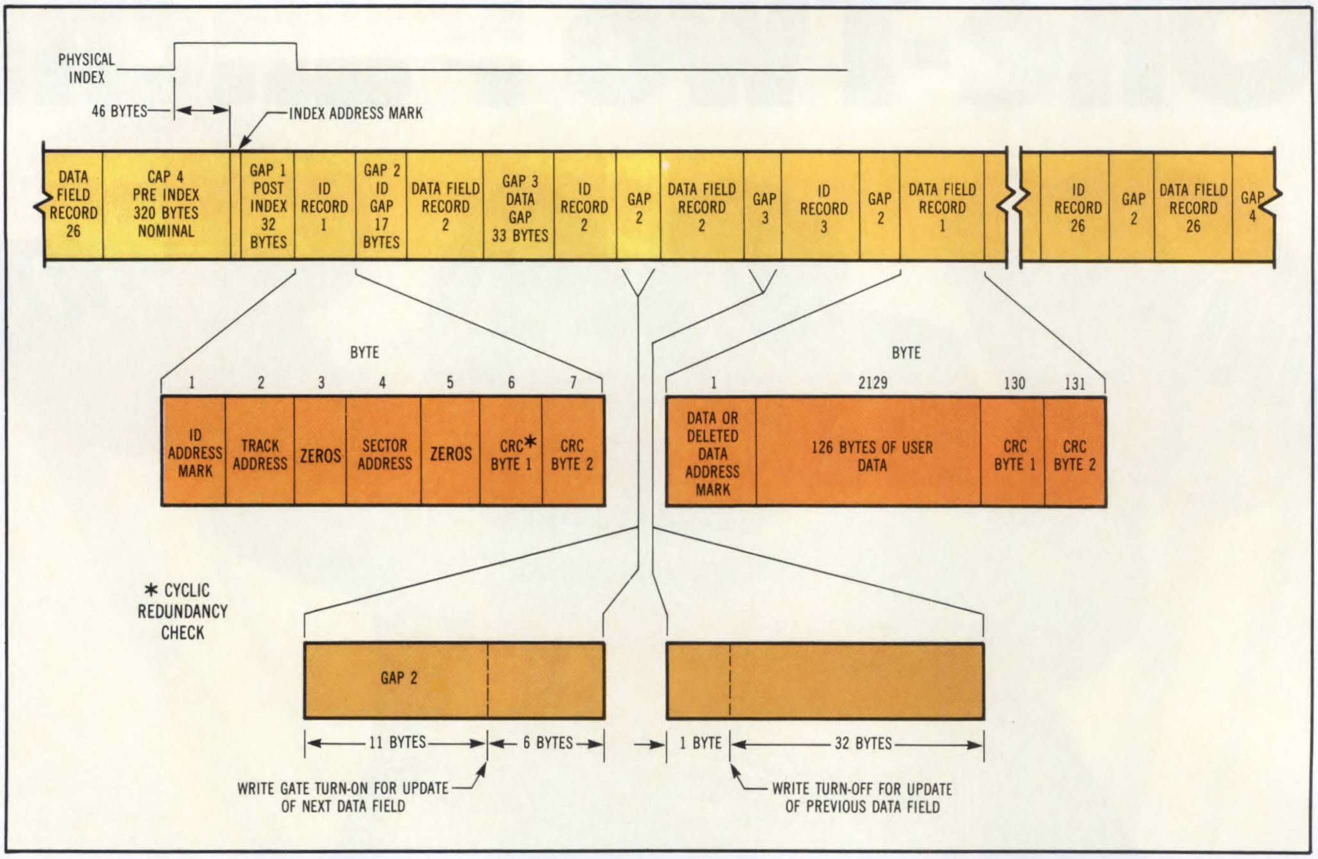


Fig 2 To format a diskette to the IBM 3740 scheme (128 bytes per sector) with a Western Digital controller, a Write command must be issued and the data register loaded with the following: the sector size in bytes, the number of sectors per track, the number of usable tracks, the identification address mark, the side number, the gap sizes, and the step rate.

the most common, however. In a memory mapped system, the controller resides within certain address boundaries of the total system memory map. Therefore, a formatting program must take this into account and send the expected information to the correct addresses for control and data.

A controller implemented in a system that uses port addressing does not take up space in the memory map. It is addressed by sending data to given ports or physical locations. Frequently, several ports are designated for a disk system, including ports for control, drive selection, track addressing, and read/write data functions.

The drive's track density presents another interesting problem. Both the controller and the software must currently be able to recognize 48- and 96-track/in. drives. In the future, densities will increase to 130 tracks/in., or more. As a result, step distance becomes a critical element in the translation formula.

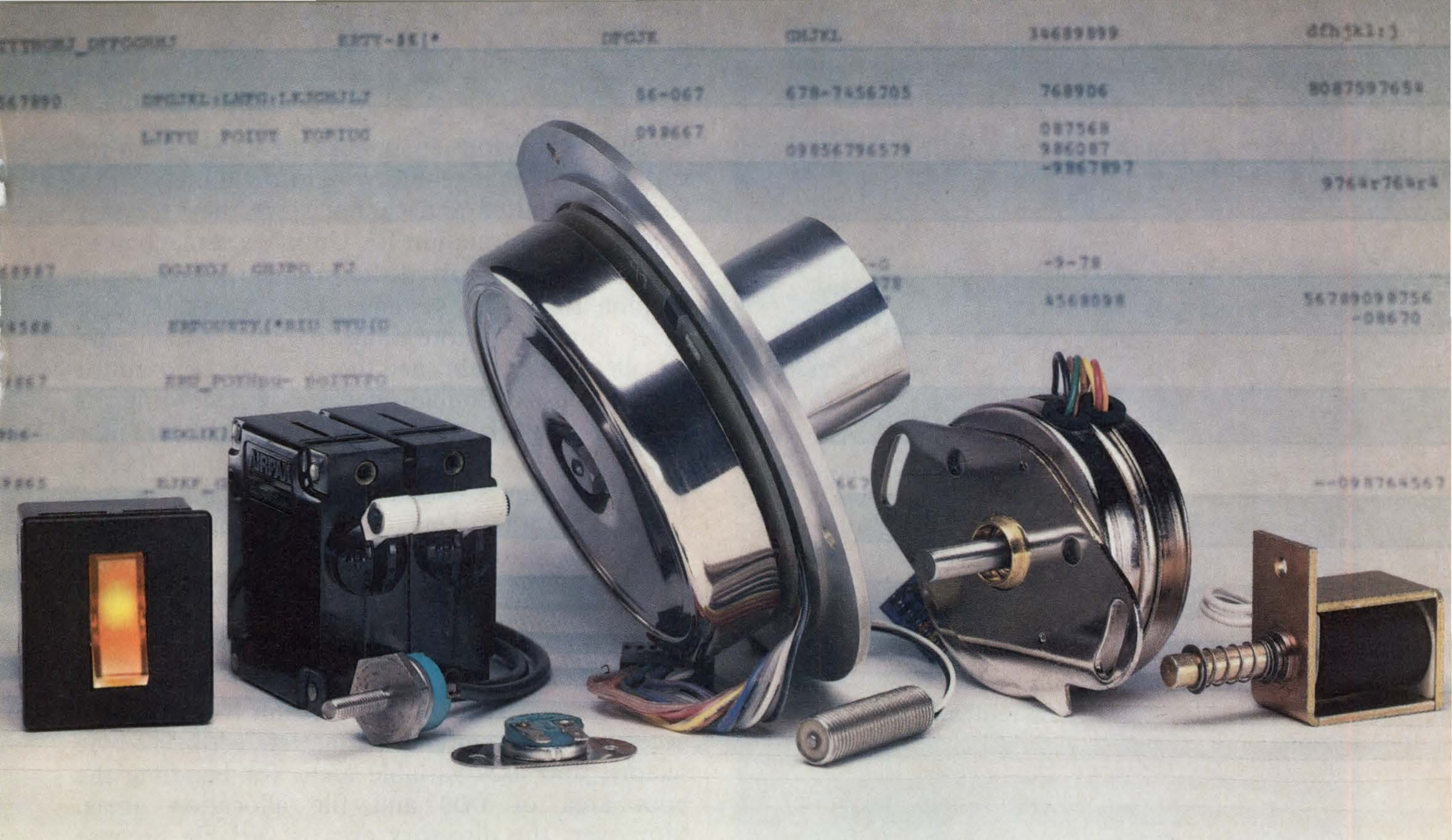
Once the diskette is formatted, some provision must be made to read and write in the newly established format. Although the format program was responsible for establishing the format on a blank diskette, it is now up to the operating system's BIOS or another utility to set up the data correctly to match the expected format.

Creating an extra utility to set the controller to the desired parameters is a popular technique. This is usually invoked by a Set command that loads the registers, or, in the case of the Nec controller, sets the stack. These parameters stay in effect until changed by another SET instruction. Moreover, the BIOS can be enhanced (eg, the Advanced Computer Technology system) to send data to the controller in the expected manner. This involves establishing a lookup table that the BIOS invokes from a menu choice made by the user.

Unix V may solve the problem

Most of the format differences have occurred in desktop systems using 8- and 16-bit operating systems, such as CP/M and MS-DOS. In an effort to get the most from their designs, system designers have opted for unusual formats, thus creating mismatches. But, with the growing use of Unix, and a push for a standardized implementation of Unix System V by Western Electric and a number of semiconductor manufacturers, standard recording formats may benefit as well.

One important goal in creating a standard Unix operating environment is to make software totally transportable between systems using System V. But, dozens of disk recording formats short-circuit



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this plan. At present, only the IBM 3740 single-density, 8-in. format is suitable for system-to-system interchangeability. Unfortunately, this format is limited and cannot store the necessary amount of information for Unix-based machines.

IBM may have solved the problem, however, in relation to 5¼-in. systems. The IBM PC, due to sheer numbers (more than 700,000 systems are installed), has established the *de facto* standard for double-density, double-sided 5¼-in. recording. Its 48-track/in. format, with either eight or nine 512-byte sectors—depending on whether or not MS-DOS 1.1 or 2.0 is used—yields either 320 or 360 Kbytes of storage. Due to a unique lookup system, the PC can automatically handle eight-sector diskettes under DOS 2.0 without conversion. To handle this complex control, the PC uses the NEC 765 controller and a stack operation.

The PC also uses a full-track buffer (4608 bytes) and a least recently used algorithm to speed data access. The diskette is formatted with 512-byte sectors, and uses variable areas for handling the boot area of DOS and file allocation areas. Moreover, the directory area is variable because MS-DOS provides for a hierarchy of directories rather than flat files. The allocation scheme is kept in sector clusters and used on an as-needed basis. The system keeps track of which track side and head are in use, and dynamically switches. Therefore, a utility to match the PC format must not only keep track of the format variable, but also the relationship of the head movement.

It is unlikely that varying disk formats will become uniform. However, even smarter controller chips, designed specifically for operation with 16-bit microprocessors, may become available. These controllers will most likely contain specialized user accessible microcode that matches the characteristics of different controllers. Ideally, the next generation of controllers will permit specific parameters to be downloaded. A system could thus be profiled to match any given disk format.

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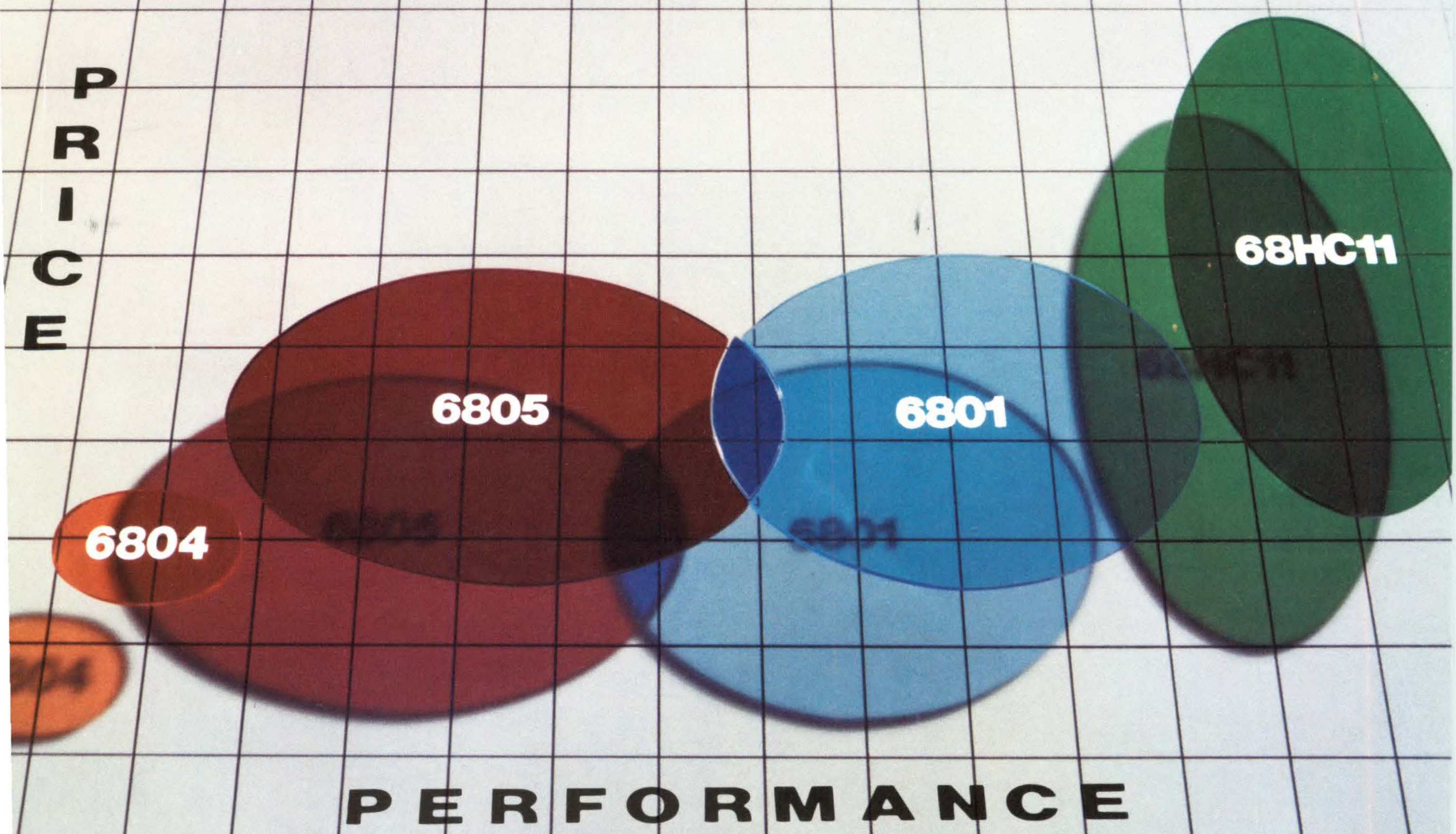

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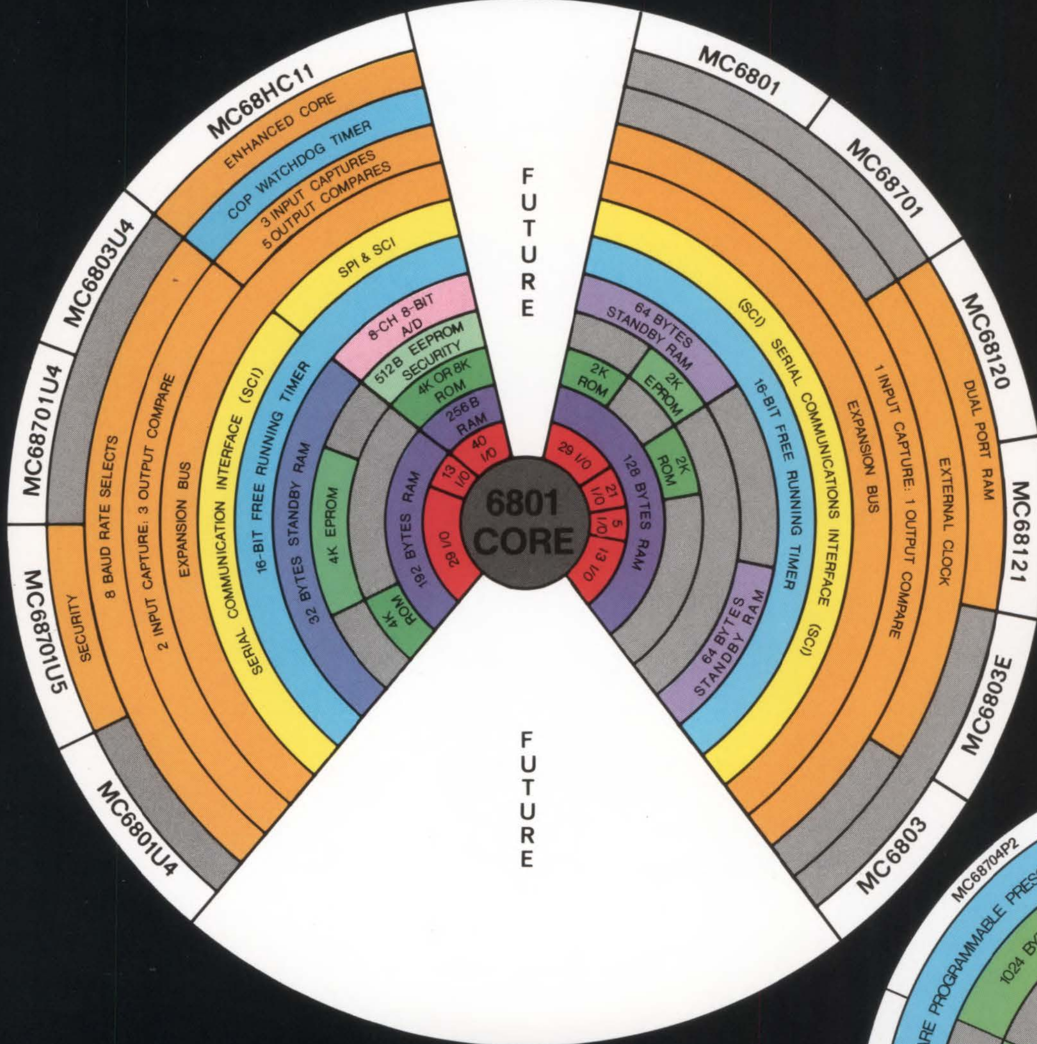

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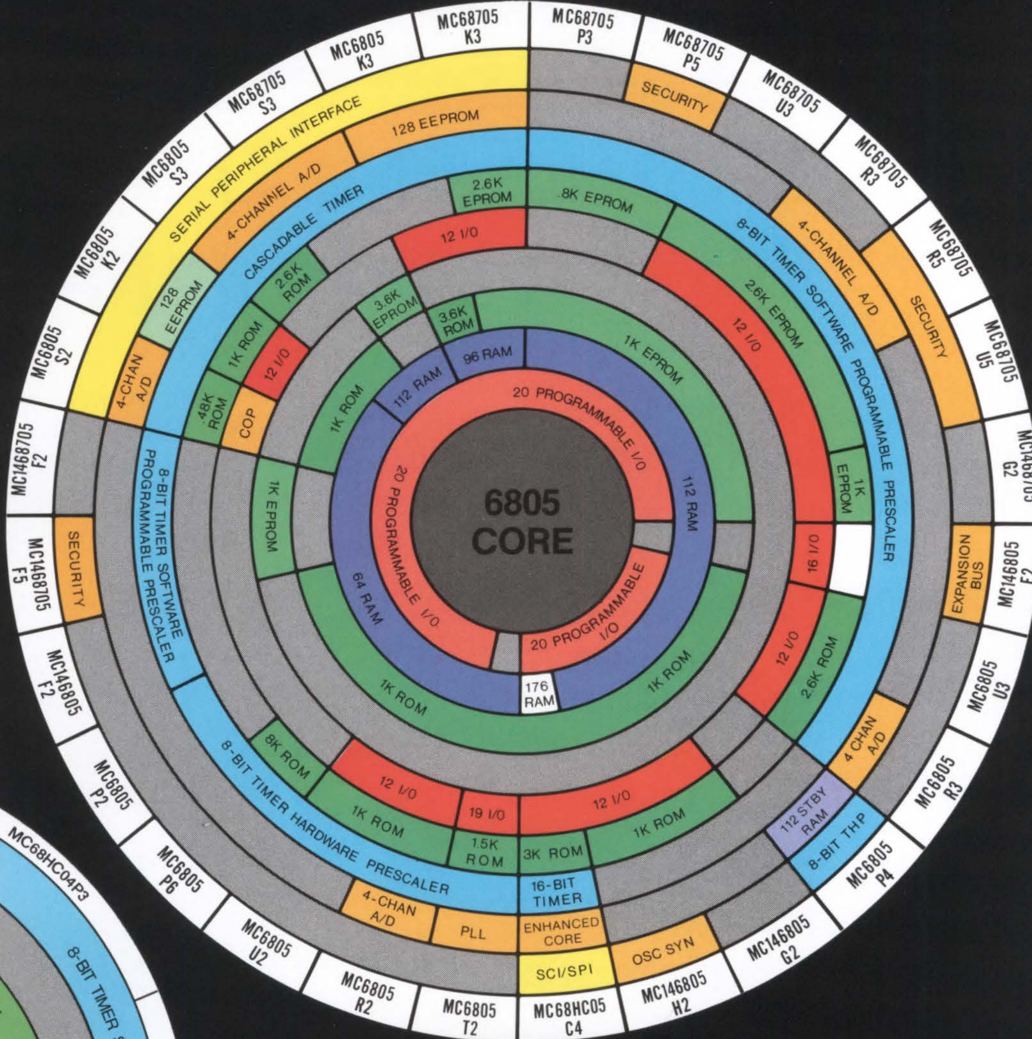

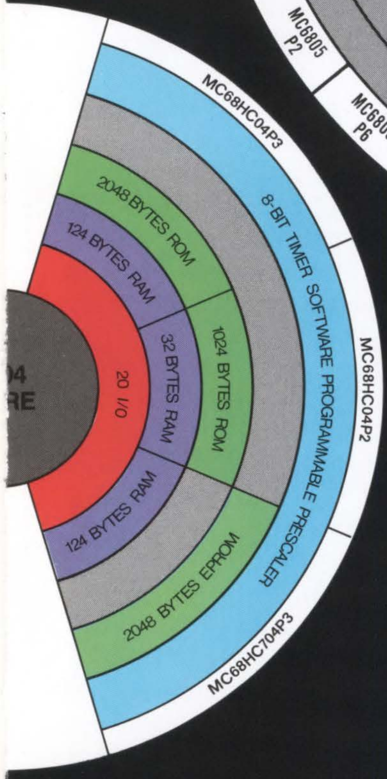

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ADVANCED ICs SPAWN PRACTICAL SPEECH RECOGNITION

ICs can provide the memory bandwidth and signal processing power for practical speech-recognition systems. However, harnessing chip capabilities to speech-recognition tasks does require more advanced algorithms.

by Michael W. Hutchins and Lee K. Dusek

Based on acoustic pattern-matching algorithms, today's speech-recognition technology produces speaker-dependent systems with 50- to 100-word vocabularies. Research is underway, however, on more sophisticated, perceptually based algorithms that will propel speech-recognition technology toward higher performance connected-speech recognition and larger vocabularies.

Current speech-recognition technology is at the speaker-dependent, connected-word level. Previously, only mainframes had this capability. Now, however, some processor chips, such as the 5-million instructions per second (MIPS) Texas Instruments TMS320, have enough fast computational power to accommodate speech-recognition algorithms.

One speaker-dependent connected-word recognizer is TI's digital signal processing (DSP) board that produces both voice output and input. As a word recognizer, it handles both isolated and connected words with a maximum capacity of about 32 s of vocabulary, or about 50 utterances. Any single vocabulary item can have a maximum length of 3 s; a single utterance can contain upwards of 21 connected vocabulary items.

The isolated word as the norm

Today's more popular commercial recognizers are relatively low cost, speaker-dependent, isolated-word types. Such recognizers perform well in industrial applications (eg, quality control inspection) or during process control command entry. Isolated-word technology does impose a major restriction, however. Between spoken words, the silence required is 200 to 300 ms.

Users of both isolated- and connected-word, speaker-dependent recognizers must enroll a predetermined vocabulary into the system to create a word template library. Thus, spoken words are recognized when they match templates stored in system memory. Constructing a template involves finding the beginning and end points for each sample word spoken, dividing the word into discrete time

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Lee K. Dusek was an applications engineer at Texas Instruments when this article was written. Ms Dusek holds a BS in math from Longwood College in Virginia, and an MS in math and industrial and systems engineering from Ohio State University. She is now a systems analyst at Sohio Petroleum, Houston, Tex.

slices, and characterizing each time slice with about 32 measures of acoustic parameters. With multiple samples of a particular word, these acoustic characterizations are usually merged to develop fewer templates.

During word recognition, actual input features are compared with those of the various reference patterns. Time alignment, or the synchronization of input features with reference patterns, is an initial critical step. However, time alignment requires very high precision that poses a major problem for isolated-word speech recognizers.

Generally, energy levels at the beginning and end of a word signal alignment. A word begins at the onset of significant speech energy and ends when speech energy drops below a certain threshold for a length of time. The recognition pattern is constructed by selecting input features based on the beginning and end point prescribed for the input word.

Reliably determining word end points has been a major technological stumbling block for isolated-word recognizers. Misaligned end points account for virtually all word-recognition errors. A comprehensive solution for the end point detection problem, however, has been achieved for connected-word recognizers. This gives the recognizers greater potential for higher performance levels, even in isolated-word applications.

Dynamic programming and a related technique called "time warping" have solved the time-alignment problem. Dynamic programming optimizes the residual error between the speech input and its reference pattern (or template) collected from among all speech frames. This approach focuses on gathering an utterance's cumulative residual error. It avoids individual frame residuals, minimizing the error over a sequence of frames. Hence, dynamic programming helps the system decide if a spoken word matches its intended template, and is therefore recognizable.

Formerly, reference and input data from speech frames of the same time period were computed with the results compared at each frame. The time warping technique introduces new dimensions that compensate for variations in the length and timing of spoken words without altering their meanings. It stretches a reference frame period to twice as long as the input period. This results in two significant advantages: stored reference data and the number of essential dynamic programming operations are cut in half; and memory, otherwise required for frame comparison, is eliminated, thus simplifying dynamic programming.

Moreover, time warping does not have to start and stop on specific input frames. This makes word endpoint detection unnecessary. Thus, 200- to 300-ms pauses between isolated words become a thing of the past in connected-word speaker-dependent recognition.

For example, dynamic programming and time warping algorithms are applied to TI's speech recognition technology (Fig 1). After time registration, input data undergoes a high level decision-logic operation. In this example, a threshold-comparison test and a next-closer-error threshold test determine which word or words are to be chosen.

Once the input's residual error is below the threshold, dynamic programming helps to determine if the difference between the template yielding the lowest residual signal and the next smallest residual is great enough. If the difference is sufficient, the algorithm orders a word match. When two templates have residual errors that are too close together, the input word will be rejected, and the host system prompts the user to repeat the word.

In contrast with the speaker-dependent system, the speaker-independent system, without being trained to individual speaking, recognizes any user's voice. Speaker-independent recognizers are complex, however. For each word accepted, even at the isolated-word level, hundreds of speech samples must be collected, properly processed, and clustered. Only then can unknown speech be reliably recognized. Over the short term, collective speaker-independent templates will likely be lower quality voice models than speaker-dependent ones.

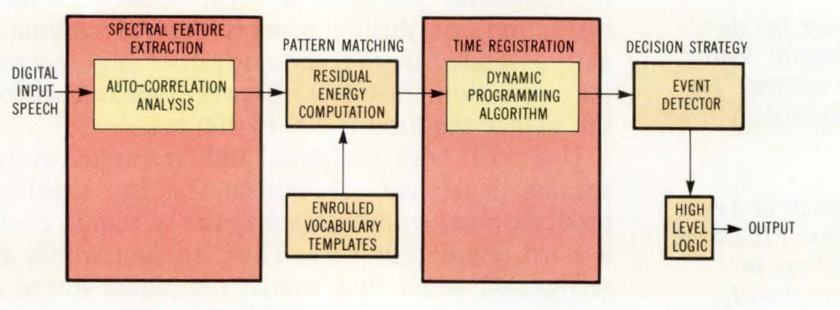

Fig 1 After the analog waveform is sampled, digitized speech input undergoes auto-correlation analysis to perform spectral feature extraction. These features are then matched against stored reference templates, generating a residual energy proportional to the difference between the two feature sets. Dynamic time warping adjusts for speed variations between input and template.

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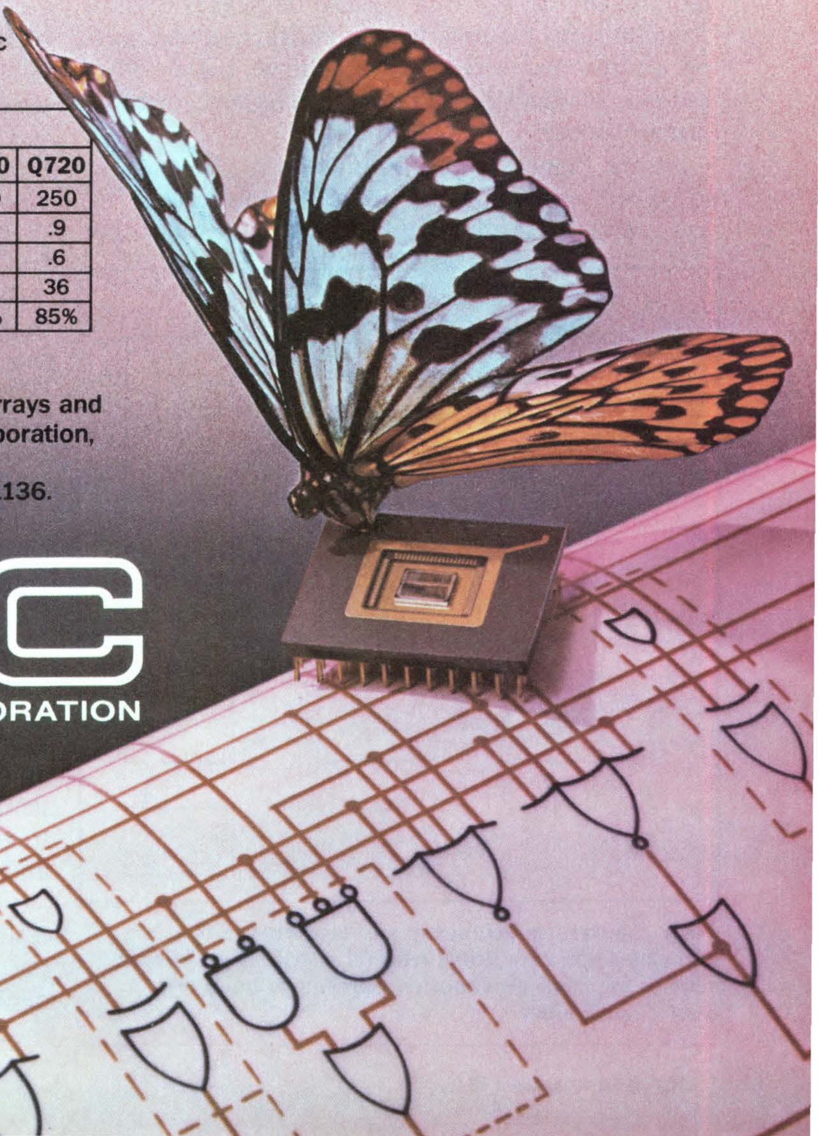

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As a system's vocabulary increases, so does the number of acoustically similar words it contains. Hence, simpler acoustic measures used by isolated- or connected-word systems do not provide adequate power to distinguish between the many words required by continuous-speech recognizers.

Substantially faster and more natural than isolated- or connected-word recognition, continuous recognition offers the greatest operating advantages. But at the present level of technology, this is difficult and expensive to produce. Continuous-speech recognition requires about 10 times more computational power than connected-word systems. Also, continuous recognition requires new classes of algorithms and techniques. In the next decade, however, continuous recognition is expected to automatically and accurately transcribe natural conversation.

Multidisciplinary method

Speech-recognition technology requires a multidisciplinary effort. It demands knowledge and research in machine intelligence, acoustic phonetics, signal processing, speech perception, and human factors engineering. Greater insight into the physiology of hearing, the psychology of learning, and the structure of natural languages is vital. Contributions from various scientific and engineering camps are essential to achieve higher level machine recognition of smoothly spoken, unstilted human speech.

Future speech-recognition work, leading to advanced technology, demands considerable involvement by phoneticians, linguists, and other speech-oriented scientists. Current laboratory efforts, however, are producing promising recognition applications. An automated directory listing retrieval system, based on connected-word recognition, is one of the more salient applications. The system in Fig 2 can recognize spoken, spelled names from a directory of names. Over a dial-up telephone line, these names are spelled without the need to pause between spoken letters.

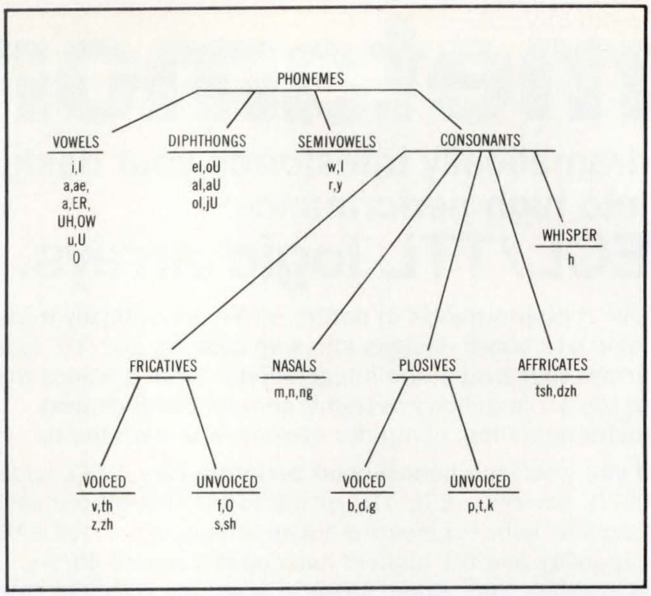

Fig 3 The speech recognition system works on phonemes, which are the basic units of English.

The speech input consists of two letter sequences: the first represents the last name; the second, the person's initials. After the input is digitized, a set of global beginning and end points is determined for each of the two connected-letter strings.

Key to this experimental system is a level-building, dynamic time warping (DTW) algorithm that matches the test string to a set of stored letter-reference templates. The DTW algorithm's task is to locate the sequence of reference patterns that best matches the test input. A group of reasonable alternative candidates is also generated. These candidates are interpreted according to letter-equivalence classes to provide a list of potential name-equivalence classes. The name generator then uses the list of potential name-equivalence classes to search the directory for names within a particular name-equivalence class.

Next, a score generator examines the names to determine how closely each name matches the given test input. At the decision point, the list of names and the names' associated scores are checked to determine a match and to make sure it is not ambiguous.

For speaker-dependent letter templates, system tests resulted in name accuracies ranging from 91 percent for a normal talking rate to 99 percent for a deliberate talking rate. Accuracies for speaker-independent templates ranged from 88 percent for

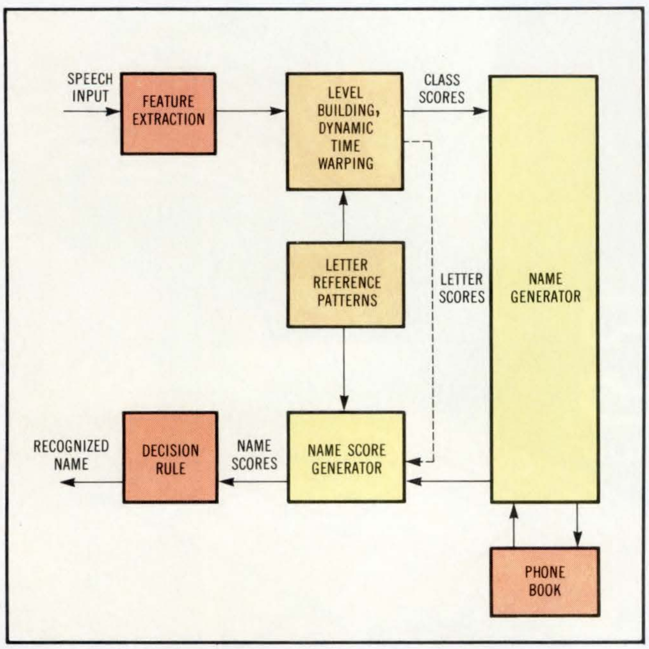

Fig 2 Spoken, spelled names are recognized in this automated directory listing retrieval system. The syntactic rules of the name generator use subsequent input to resolve ambiguities.

a normal talking rate to 94 percent for a deliberate talking rate.

Other studies involve speaker-independent, isolated-word digit-recognition systems that can achieve high accuracy without training for different speakers. In this approach, a digit-classification format is based on dividing the unknown word into three regions and then making categorical judgments as to which of six broad acoustic classes each segment falls into.

Phonemes, basic speech units comprising English words, are at the heart of this system. Fig 3 shows the various categories of phonemes—vowels, diphthongs, semivowels, consonants, fricatives, nasals, plosives, and affricates. The Table lists the sequence of phoneme categories for each of the 10 digits, 0 through 9.

For speaker-independent digit recognition, a set of robust measurements is applied to classify the phonemes into six broad categories. The measurements include energy, zero-crossing, two-pole linear predictive coding (LPC) parameters, and normalized error of the LPC analysis.

Fig 4 shows the digit-recognition system. After endpoint alignment, word input is analyzed every 10 ms to obtain the zero-crossing rate, energy, two-pole LPC coefficients, and residual LPC estimation error. The input is then divided into three well-defined regions, allowing initial classification decisions to be made.

All data is fed in parallel into a preliminary decision-making algorithm (Fig 5) that selects one of several possible digit classes for the input word. A final decision is then made, based on the presence or absence of certain key features in the input speech. Error rate for this system was reported at 2.7 percent for a carefully controlled recording room, and 5.6 percent for online recordings in a noisy computer room.

Sound Class Characteristics

Digit	Sequence of Sound Classes
0	VNLC→FV→VLC→BV
1	VLC→MV→VLC
2	UVNLC→FV→BV
3	UVNLC→VLC→FV
4	UVNLC→BV→MV
5	UVNLC→MV→FV→VNLC
6	UVNLC→FV→UVNLC
7	UVNLC→FV→VNLC→FV→VLC
8	FV→UVNLC
9	VLC→MV→FV→VLC

VNLC – Voiced, noise-like consonant
UVNLC – Unvoiced, noise-like consonant
VLC – Vowel-like consonant
FV – Front vowel
MV – Middle vowel
BV – Back vowel

Computational intensity

From the beginning, computational power has been closely associated with speech-recognition algorithm complexity. Axiomatically speaking, the greater the speed and power a processor offers, the more sophisticated the recognition algorithms can be. This results in greater speech-recognition accuracy, and—with memories of appropriate organization, speed, and capacity—larger recognizable vocabularies.

The more computationally intensive the algorithm that determines the speech parameters, the higher the level of recognition performance. This requires that each parameter represent a robust measurement. A robust measurement must be simply and unambiguously measurable, able to

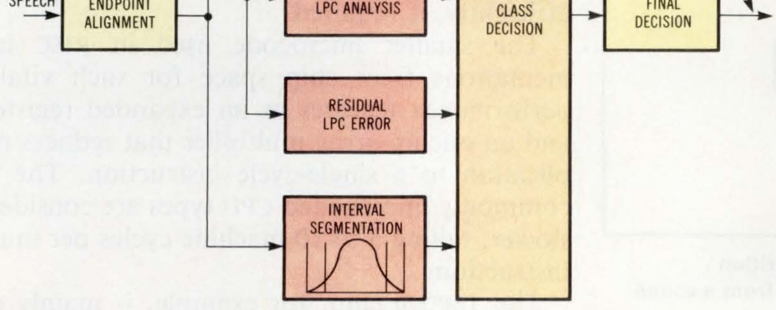

Fig 4 Several robust measurements, including linear predictive coding (LPC) analysis, are calculated for each digit and then combined in a parallel fashion to determine the sound class for each time interval. This class is then input to final decision logic where the sequential nature of the input is used to recognize the appropriate digit.

grossly characterize a large proportion of speech sounds, and conveniently interpreted in a speaker-independent manner. For example, a set of robust measurements for a digit-recognition algorithm includes zero-crossing rate (the number of zero crossings in a fixed interval on the order of 10 ms), energy (the sum of the squared values of the digitized speech waveform in a given interval), LPC analysis (which represents the speech signal in terms of parameters of a filter whose spectrum best fits that of the input speech signal), and normalized error (obtained from a two-pole LPC analysis of a given speech frame). These robust measurements each demand varying levels of computational intensity.

Mainframes and minicomputers have historically carried the bulk of required computations for speech recognition. More recently, expensive custom microprocessors, with sufficient horsepower for relatively acceptable levels of speech processing, have served as cost-effective intermediaries. Now, programmable digital signal processing (DSP) microcomputers herald an era of

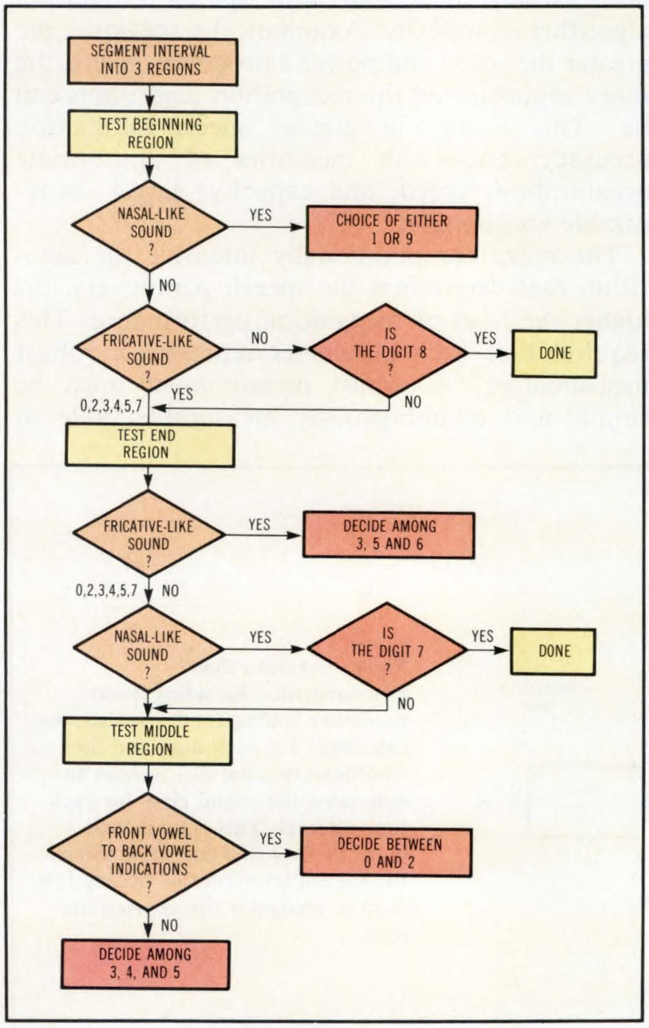

Fig 5 The preliminary decision-making algorithm determines which digit is spoken using input from a sound class generator.

raw computational speed onchip and dramatically reduced computing costs. In addition, programmable DSP chips perform a variety of functions, including speech synthesis, vocoding, voice verification, and nonspeech applications (eg, fast modems). Particularly in speech processing, high speed DSP chips, using superior performance algorithms, perform such computationally intensive tasks as speech analysis, feature extraction, word recognition, pitch tracking, and speech synthesis.

DSP microcomputers herald an era of raw computational speed onchip.

Speech-recognition algorithms are at a relatively primitive stage. This means that programming will be important for speech processing. As recognition technology advances, new features and improvements will be incorporated through programming, rather than through costly system redefinition and processor-chip redevelopment.

For example, the TMS320 DSP chip powers a trio of high performance algorithms—auto-correlation analysis, a modified LeRoux-Geuguen transform, and LPC analysis—to perform realtime feature extraction in TI's speech processing systems. After feature extraction, the measured similarity between the extracted speech parameters and stored reference patterns is computed. When the reference data matches the input data, a low energy residual-error signal results. If there is a perfect match, the error measure is normalized to 1. To be within recognizable limits, the value must be less than 1.2 in the speaker-dependent system. Parameters used to compute the difference between input samples and stored-template reference patterns are also computed by the auto-correlation and residual-energy algorithms.

Optimizing microcomputer chips for high speed, realtime DSP calls for instruction set and architectural alterations to reap speed from silicon real estate. A disciple of the Reduced Instruction Set Computer (RISC) concept, DSP focuses on essential instructions—MOVE, ADD/SUB, MULT, and DIV—that represent 87.5 percent of all instructions executed. Other instructions can be synthesized efficiently, if required.

The smaller microcode used in RISC implementations frees chip space for such vital DSP performance features as an expanded register set and an onchip array multiplier that reduces multiplication to a single-cycle instruction. The more commonly microcoded CPU types are considerably slower, taking 5 to 10 machine cycles per multiply instruction.

The TMS320 chip, for example, is mainly occupied by a 16- x 16-bit, 200-ns array multiplier; a single-cycle barrel shifter; 144 words of RAM for data; and 1536 words of onchip ROM. Because of its single-cycle multiplier and powerful load/accumulate/data-move instruction, the TMS320 sustains chained 16- x 16-bit multiplication with true 32-bit accumulation at 2.5 MHz.

A modified Harvard architecture, which separates program and data functions in the chip, further enhances speed. This allows it to pipeline its operations (ie, fetch data simultaneously from program and data memories) so that a previous instruction's execution cycle can overlap the next instruction's fetch cycle.

Future direction

State-of-the-art DSP chip computational power at 5 MIPS is good for a 30- to 50-word speaker-dependent, connected-word vocabulary that can cover 40 percent of voice-input applications. Going to 10 MIPS can increase a vocabulary to the 75-word range, spreading voice input to 75 percent of the available applications. To cover 90 percent of the potential voice-input applications, a 200-word vocabulary, requiring 20 MIPS, would be adequate.

Phonetically based, isolated-word, speaker-dependent speech recognition with a 5000-word vocabulary is likely to be the next level of commercially viable systems. This approach, which does not require speaker enrollment, is based on acoustic units or parts of sounds, concatenated by a stochastic or Markovian process to model speech recognition. Accuracy is approximately 97 percent. Stochastic processing methodologies compute the likelihood of matching all possible variations of the vocabulary words against the unknown speech input.

Increasingly powerful chips and algorithms will allow computers to hear as naturally as humans do.

Speaker-independent continuous recognition will likely make a radical move from mathematically based algorithms to perceptually based ones, which require considerably more computing power.

The frequencies at which speech energy peaks are key to human speech perception. These frequencies, called formants, are the resonant frequencies of the mouth cavity, controlled by the tongue, jaw, and lips. Determining the first two or three formants is generally adequate to characterize the sound as a human would perceive it.

Formants are the basis for perceptually based algorithms for speech recognition. Today's methods for automatically extracting formant frequencies require large computers. Yet, with increasingly powerful chips, sophisticated algorithms, and greater knowledge of human speech perception, it will be possible to teach computers to hear as naturally as humans do.

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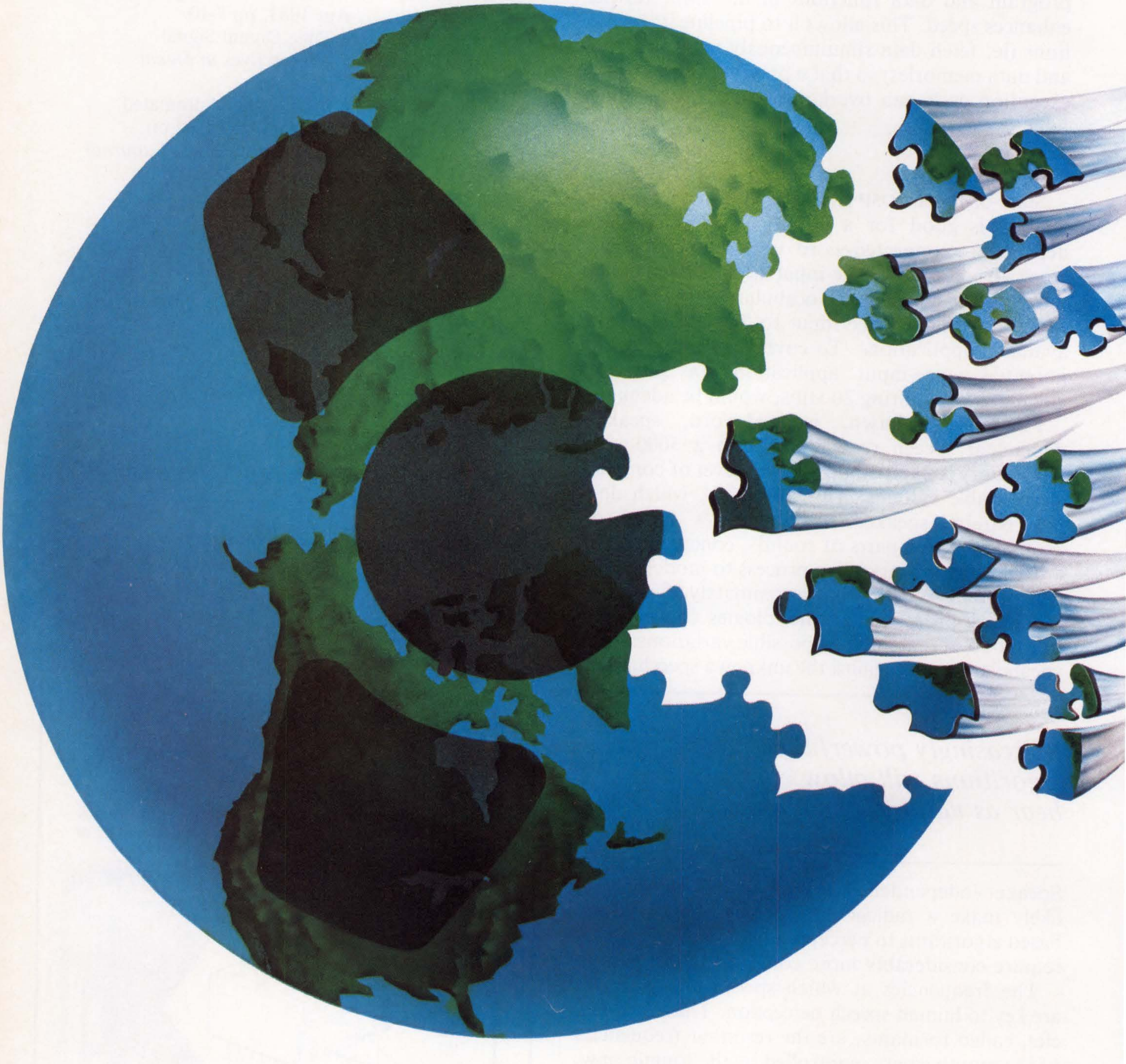

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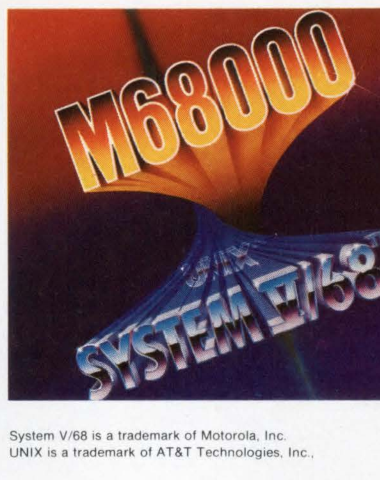

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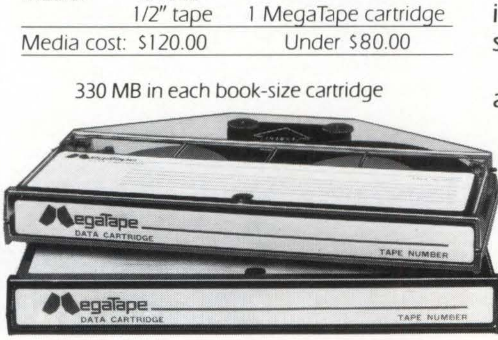

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QUEUING ANALYSIS COMPARES DISK ORGANIZATION

Using a queuing model together with computer analysis shows that for a realistic range of parameter settings, a multiple head moving arm organization can improve disk performance.

by Alexander Thomasian and Kayvan Kiamanesh

As processor speeds increase, computer system performance becomes critically dependent on disk subsystem execution. Using a sophisticated queuing technique, instead of a first-come, first-served method, is one way to improve such performance. However, this improvement only shows up when there are several requests queued up for the disk at the scheduling instant—a situation that rarely occurs. Another solution for seek time reduction (or elimination), is the use of a fixed head disk, but this is an extreme measure, and very costly. Therefore, a compromise solution, one involving a large number of equidistant read/write heads on each moving arm, offers the most significant improvement in performance.

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Kayvan Kiamanesh is chief engineer at Alpha Data Inc, Chatsworth, CA 91311 where he is responsible for development of disk drives and controllers for minicomputers. Mr Kiamanesh holds a BS in electrical engineering from Northrop University.

A disk organization with a set of 50 read/write heads evenly spaced over the disk cylinders offers the advantage of a reduction in seek time by increasing directly accessible disk capacity without requiring disk arm movement. A simple computer system queuing model underscores the importance of reducing individual device delay in order to improve overall performance. A queuing formula for the mean response time of a single-server system analyzes individual disk performance. This queuing formula compares the new disk organization, called ATLAS, with several conventional moving arm disk organizations.

The queuing network model of a computer system consists of a CPU and multiple disks. There, L denotes the rate at which transactions (processing requests, interrupts, etc) arrive. Each transaction requires a certain processing time at the various devices, called the device loading (Yi at device i). The use of device i (Ui) is the product of the arrival rate and the loading. The equation is as follows:

$$Ui = L \times Yi$$

Device utilization is an important factor, since the mean response time at device i (E[Ri]) is inversely proportional to (1 − Ui). Also, the mean response time of transactions equals the sum of device response times (provided there is no initial delay for transaction activation due to memory constraints). Therefore, it follows that reducing the response time of each disk is quite important.

Balancing disk loadings by rearranging files, for example, results in a reduction in overall response time. In most cases, accessing frequently needed information from disks requires an even greater improvement in disk subsystem performance. Computing the mean response time characteristic of a single disk unit in isolation (E[Ri]) versus the arrival rate of disk requests (Li) results in the mean and variance of the service time for a single request. The service time of a request at the disk has three components: seek, search, and transfer time.

Seek or access time

The time it takes for the moving arm to travel from its current position (on cylinder j) to the next position, k ($k \neq j$) to serve a new request, is known as seek or access time. The seek time is a function of the number of cylinders to be traversed, $d = k - j$. Note that the cylinder numbers k and j are from the set 1,...,C where C is the maximum number of cylinders. For the new disk organization, the seek time characteristic A(d) is shown in Table 1. The mean (E[A]) and variance (V[A]) of seek time is a function of the probability that the arm moves d cylinders, P(d) as follows:

$$\begin{cases} E[A] = \sum_{d=1}^{c-1} P[d]A(d) \\ V[A] = \sum_{d=1}^{c-1} P[d](A(d))^2 - (E[A])^2 \end{cases}$$

A model for the disk reference pattern states that with a certain probability (P), the arm does not move for successive references, and that when the arm does move, it accesses all other cylinders with equal probabilities. This model is the basis for computing P(d). The probability (P) has been observed empirically to be rather high ($P = 2/3$). Earlier disk studies, based on the assumption that disk accesses are uniformly distributed, have been misleading. The number of two successively referenced cylinders is a pair chosen from C ($C - 1$) possibilities, while the number of such pairs with a distance d between the two cylinders is $2(C - d)$, therefore:

$$P[d] = \frac{2(C - d)}{C(C - 1)} \qquad 1 \leq d \leq C - 1$$

Noting the probability that the arm does not move/moves is P and $1 - P$, respectively, it follows:

$$P[d] = \begin{cases} P & d = 0 \\ \dfrac{2(C-d)}{C(C-1)} & \\ (1-P) & 1 \leq d \leq C - 1 \end{cases}$$

Successive seek times are actually dependent on the arm position. For example, a very long seek is possible only when the arm is located on the innermost or outermost cylinders. Results based on a model that takes into account the dependence of successive disk requests on seek time indicate that such an effect on seek time is small and can therefore be ignored.

TABLE 1

Seek Time of Three-plated Disk Organization

No. of cylinders traversed	1	2	4	8	16	32	48	64	96	128
Delay (ms)	5	6	7	9	12	15	18	20	24	28
Additional delay cylinder (ms)	5	1	1/2		3/8	3/16		1/8		

Considering rotational delay

After the seek is completed, the additional delay for positioning of information under the read/write head is known as rotational delay or latency. While latency is dependent on the track organization, it is usually distributed uniformly over the time interval (0,T), where T is the time required for a full disk revolution (for a 3600-rpm disk $T = 16.7$ ms). The mean and variance of the latency (D) are expressed in the following equation.

$$\begin{cases} E[D] = \dfrac{T}{2} \\ V[D] = \dfrac{T^2}{12} \end{cases}$$

The transfer or transmission time is the time required to read or write requested information. It is simply given as the ratio of the length of the data record (b) to be transmitted and the transfer rate of the disk (X). The disk transfer rate is the ratio of the track capacity (B) and its revolution time (T). It

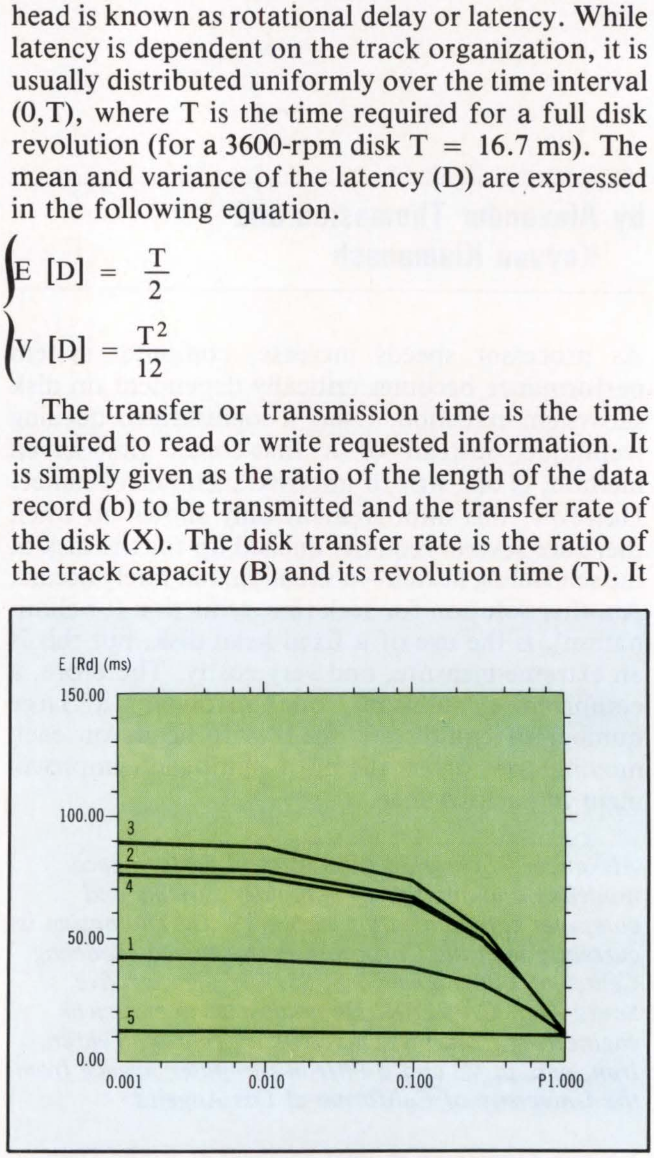

Fig 1 Computer analysis produces mean disk response times of five disk organizations. Plots of disk times converge at the fastest response time—when the probability of no arm movement equals 1.

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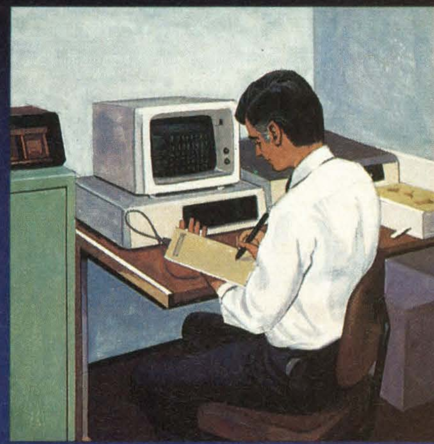

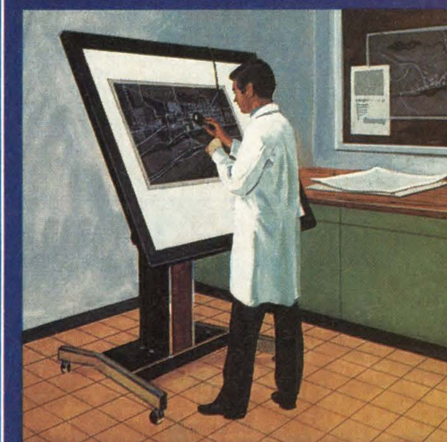

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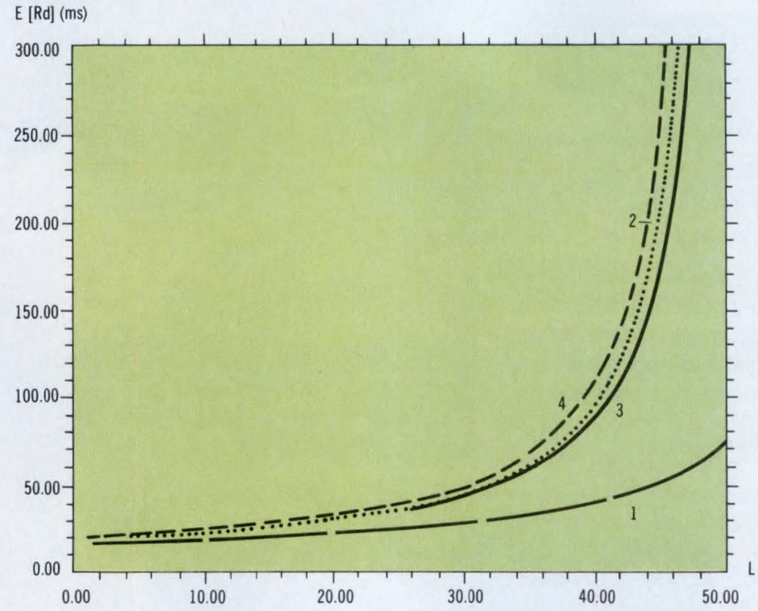

Fig 2 Disks tend to reach a saturation point as the number of requests/s increases. Disk 1 manages to avoid this saturation. In this instance, P = 0.6

follows that the mean and variance of transmission time (X) for fixed-length records (or length b) are

$$\begin{cases} E[X] = \dfrac{b}{B/T} = \dfrac{bT}{B} \\ V[X] = 0 \end{cases}$$

Note that b/B is the angular distance of the record on the track. When multiplied by the revolution time, it gives the transmission time.

Disk service time per request can be expressed as the sum of seek, search, and data transfer times. The mean and variance of disk service time (S), which are required for the analysis, are

$$\begin{cases} E[S] = E[A] + E[D] + E[X] \\ V[S] = V[A] + V[D] + V[X] \end{cases}$$

By treating the disk as an M/G/1 queuing system, the mean response time for the disk can be obtained. M denotes random (Poisson) arrivals with a fixed-rate Ld requests/s. G denotes a general service time distribution for requests with a mean and variance given in the above equation. Only a single request can be processed at a time, resulting in an M/G/1 single-server system. The mean response time can be expressed as

$$E[Rd] = E[S] + Ld\,\frac{(E[S])^2 + V[S]}{2\,(1 - Ud)}$$

The second term on the right-hand side is the mean waiting time in the disk queue due to the interference among disk requests. The utilization factor of the disk is Ud = Ld x E[S]. Since E[Rd] is inversely proportional to (1 – Ud), reducing the components of disk service time in the mean and variance of disk service time equation results in a reduction in E[Rd]. One approach is to have multiple heads covering more than one physical cylinder. Staggering the read/write heads along the radius of the disk provides a shorter access time. Such directly accessible cylinders, although physically apart, are logically contiguous.

The new disk organization, ATLAS, comprises three-plated disks. Called disk 1, five surfaces record user data. The disk rotates at 3600 rpm and its characteristic seek time is shown in Table 1. Data transfer uses 50 heads (plus two heads for servo control purposes) that are divided into five groups of 10 heads/ surface. There are 1280 tracks/ surface and the 10 heads are equally spaced 128 cylinders apart. Therefore, at any time there are 10 physical cylinders (constituting a logical cylinder) with 50 tracks that are readily accessible after an

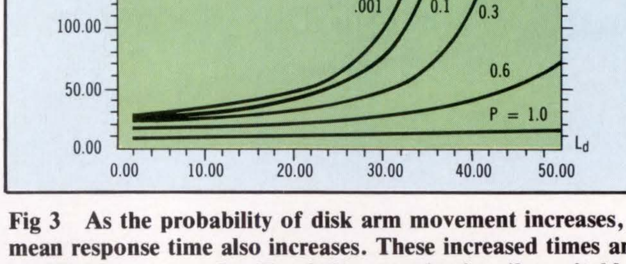

Fig 3 As the probability of disk arm movement increases, mean response time also increases. These increased times are justified by cost trade-offs of this organization (for suitable values of P).

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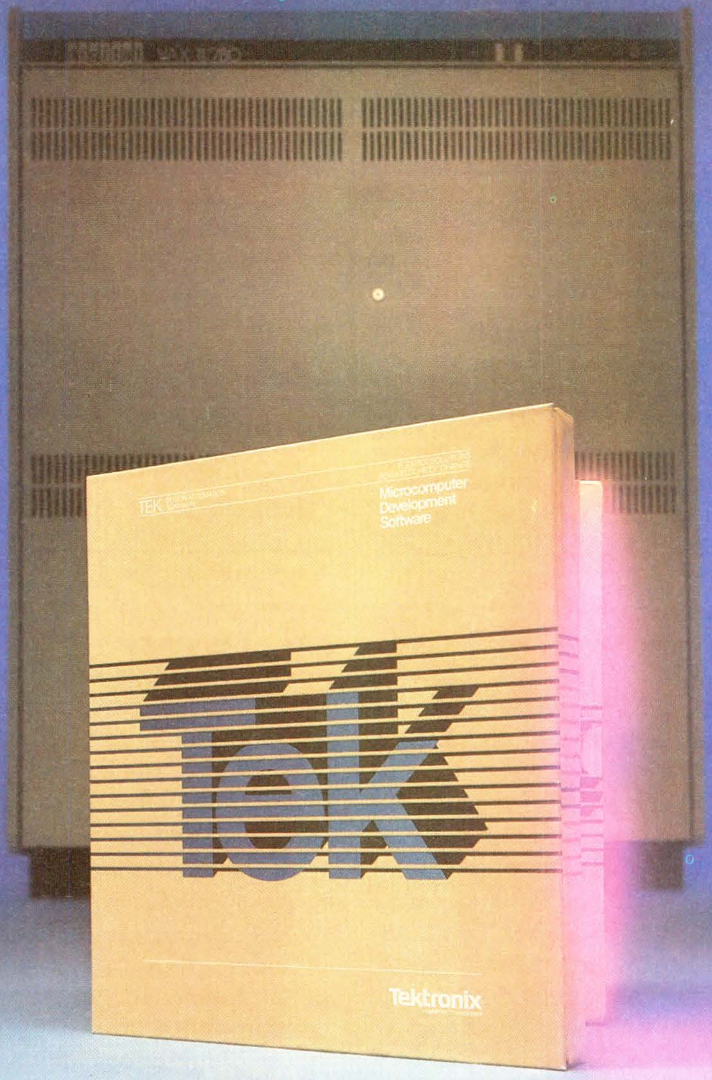

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TABLE 2

Disk Response Times

(20 requests/s)

Disk No.	P=0.60	P=0.30	P=0.10	P=0.01	P=.001
1	22	33	41.5	46	46.5
2	31	54	78.5	94	96
3	33	59	88.7	109	111
4	32	54	76.5	91	92

TABLE 3

Disk Performance

(30 requests/s)

Disk No.	P=0.60	P=0.30	P=0.10	P=0.01	P=.001
1	28	49	73	91	93
2	45	128	S	S	S
3	49	163	S	S	S
4	46.5	127	S	S	S

average rotational latency of 8.33 ms. The track capacity is 20,160 bytes; therefore the logical cylinder size is 1 Mbyte. The advantage of equal head spacing is a total head movement of about 1/4 in. This ensures a full stroke time of under 30 ms with a total disk capacity of 128 Mbytes.

Disk 2 has seek time characteristics similar to disk 1, except that it has only 10 heads distributed over two physical cylinders (five surfaces), that are 640 cylinders apart. Capacity per logical cylinder is 200 Kbytes. Disk 3 is also like disk 1 except that it has one head/surface, each covering 1280 cylinders. Capacity/logical cylinder is 100 Kbytes.

Disk 4 has 19 heads distributed over one cylinder, comparable in capacity to previous disks (100 Mbytes), with 13,030 bytes/track and 400 cylinders with 19 tracks/cylinder. The capacity/cylinder is approximately 250 Kbytes. Seek time characteristic for this disk is defined by (c + a x d) where c = 10 ms, a = 10 ms, a = 0.1 ms and d is the number of cylinders traveled. Disk 5 is a fixed head disk, which is otherwise similar to disk 1.

Computer analysis of the previously derived formulas compares the performance of Disk 1 (ATLAS) with the other disks. Fig 1 shows the mean response time with an arrival rate of 18 requests/s, for the five disk organizations as a function of P (the probability of no arm movement), using the previous mean response time equation. Disk transfer block size is set at 2000 bytes in all cases. Disk 1 outperforms disk 2, disk 3, and disk 4.

The degradation in its performance with respect to disk 5 (fixed-head disk) is quite acceptable considering the reduction in cost. Since the value of P depends on the logical cylinder size (the number of bytes accessible without arm movement), then considering an equal value of P for the conventional moving arm disk organizations is unsuitable for disk 1. The response times for disk 2, disk 3, and disk 4 are therefore quite favorable since their cylinder size is considerably smaller than disk 1.

Fig 2 shows the mean disk response time versus L. Assuming the value of P to be equal to 0.6 for the first four disk organizations, the mean response time for disk 1 is 72 ms at 50 requests/s, while the other disks are saturated, ie, their response time increases indefinitely. Disk 5 was not considered since its response time will be the same as in Fig 1.

Fig 3 plots the mean response time for disk 1 versus the arrival rate of requests for different values of P. The case P = 1.0 corresponds to a fixed-head disk (disk 5). Again, considering the cost reduction of disk 1, the increase in response time is acceptable for reasonable values of P(=0.6).

In typical applications, transaction handling is more than 50 percent faster compared to conventional disk format.

Tables 2 and 3 summarize response times for the arrival rate of 20 and 30 requests/s, respectively. The performance of disk 1 remains satisfactory, while other disks are saturated. These tables also show implied performance improvement by examining each column in each table. In addition, if disk 1 were examined at 30 requests/s and disk 2, disk 3, and disk 4 were examined at 20 requests/s, then disk 1 would still outperform the other disks.

In this analysis of five disk organizations, then, using a well known queuing formula for mean response time of a single-user system, the new disk organization shows considerable improvement in performance. In typical applications, such as control or online processing, better than 50 percent faster transaction handling is achieved as compared with conventional disk organization. If cylinder sizes are considered, this improvement is better than 100 percent. And, as disk request arrival rates increase, this disk organization results in only a moderate increase in response time, whereas conventional disks become totally saturated.

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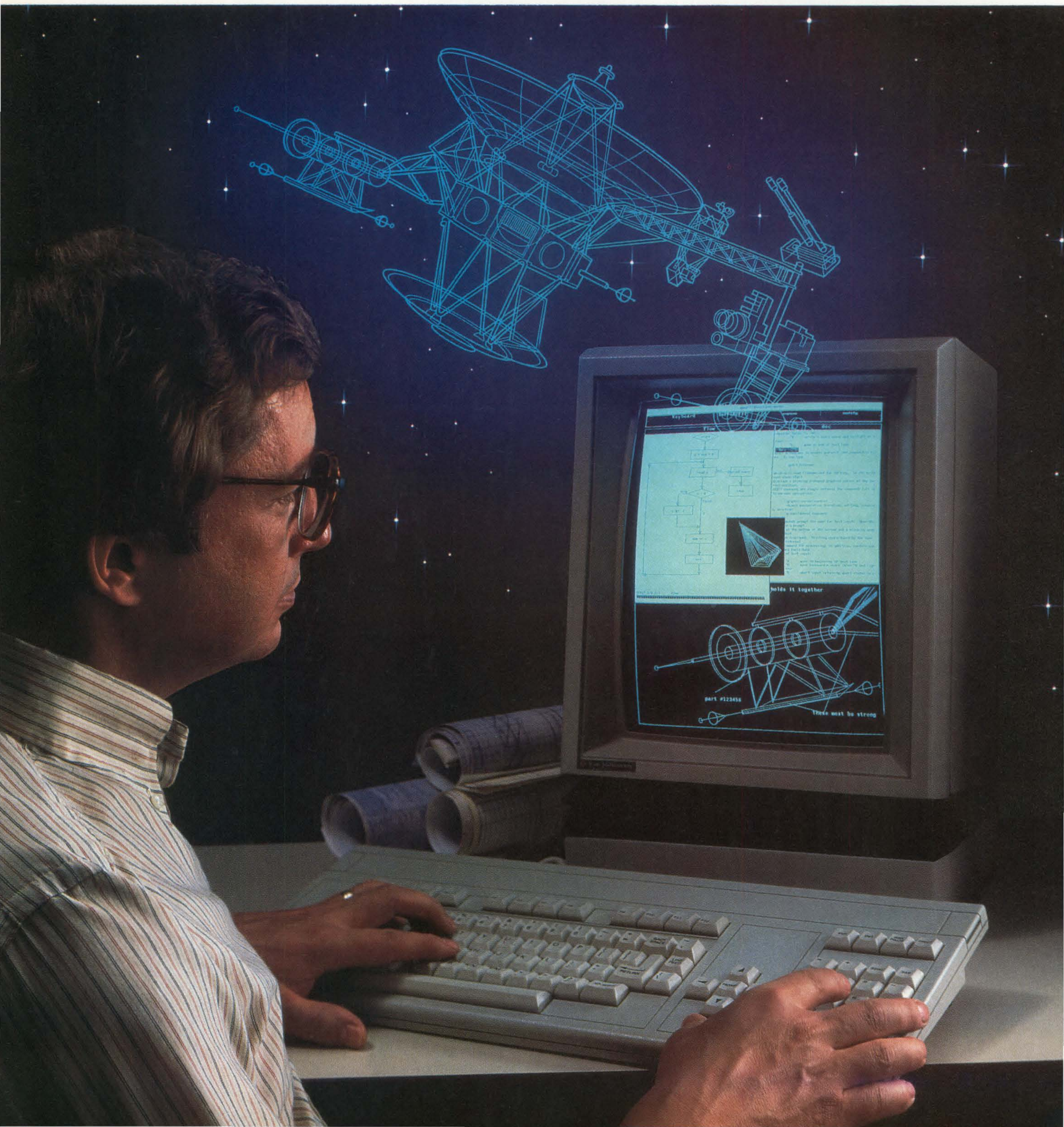

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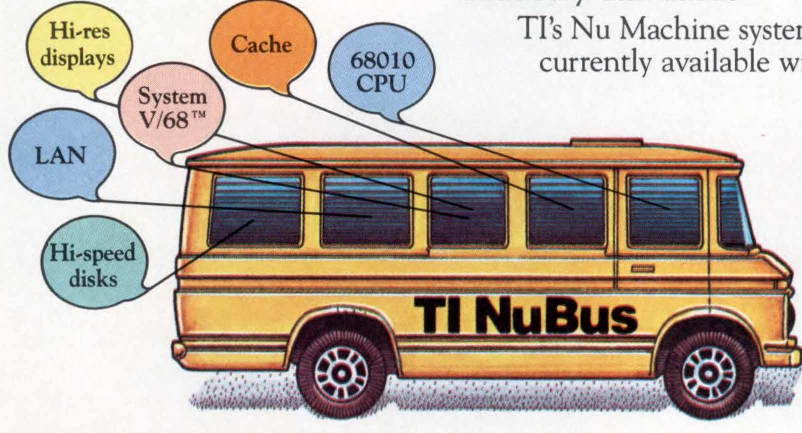

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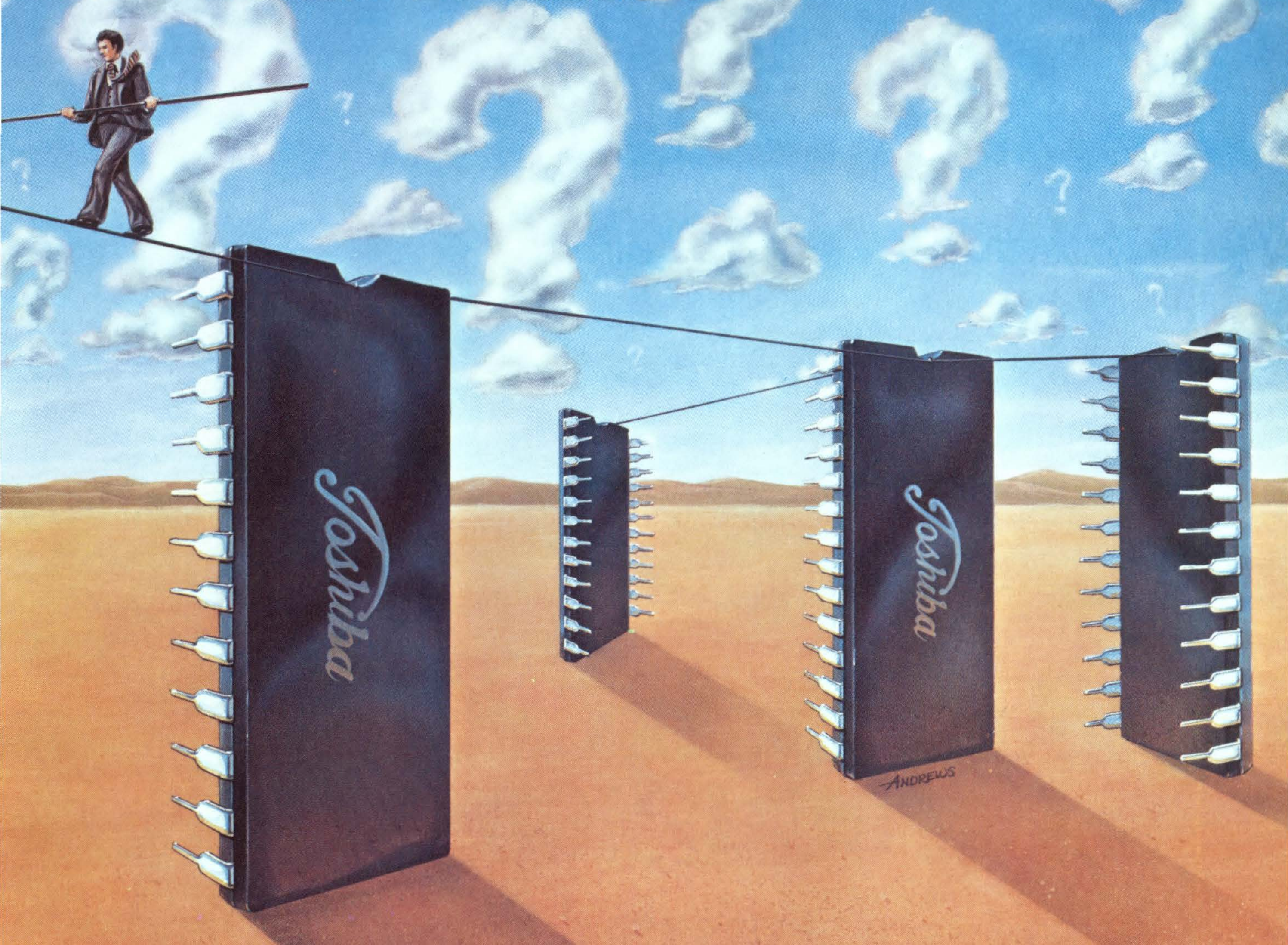

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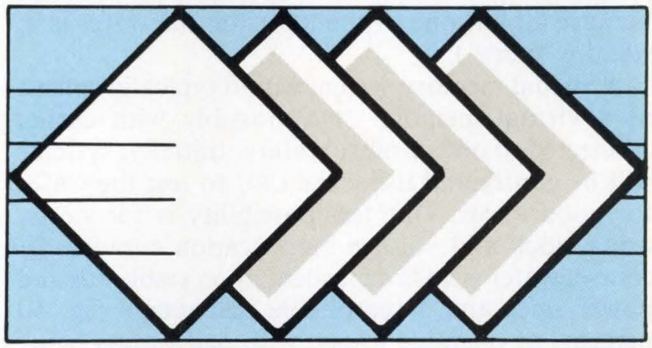
by Gilman D. Chesley



Early wafer scale integration attempts were based on discretionary wiring techniques. Using this method, circuits on the wafer were probe tested during processing and a final interconnect layer connected only operable circuits. Dynamic techniques led to the addition of permanent circuitry to the wafer. Testing then occurred with either fusing or erasable PROM techniques, or by test and reconfiguration after power was applied.

These approaches are unpopular today for a variety of reasons. The cost and space for the extra processing steps and reconfiguration logic prove to be drawbacks. Since conventional RAM densities double every few years and RAMs constitute the majority of chips in today's systems, there was no need to develop a novel technology. The technical culture of semiconductor processing was pursuing a successful direction with little motivation to change.

RAMs are now approaching the knee of the development cost/benefit curve so that future densities will probably come slower and at a greater cost than before. Given these factors, wafer scale integration (WSI) systems, particularly as main memory in a virtual memory system, can be both practical and cost efficient.

Many of the current LSI CPUs, and presumably most under development, use virtual memory techniques. In these systems, the CPU uses a virtual address space that lacks a fixed or predetermined relationship to the physical space where data is stored. This physical space consists of a disk memory for bulk storage and a RAM main memory with a smaller capacity for fast access. The virtual memory system must translate between the CPU's virtual addresses and the physical addresses that memory devices require. A page table converts the virtual address requested by the CPU to a physical address. This table is usually an associative memory where physical addresses are filed under virtual address tags. If the address is in the domain of the main memory, it is sent; otherwise it must be located on the disk.

Virtual addresses tend to be contiguous (eg, in programs and data files). Physical addresses, on the other hand, are randomly allocated as data migrates between disk and main memory on a demand basis. Since physical pages need not be contiguous, the wafer does not require adjacent RAMs, and inoperable RAMs can be treated as permanently allocated pages.

The simplest and most direct way to create a wafer of RAMs for use as a virtual main memory is by employing conventional byte-wide RAMs. The addition of a demultiplexer and address comparator modifies the devices so that each RAM on the wafer is uniquely addressable (see the Figure). A common bus of eight data/address lines and one clock line connects to all of the RAMs on the wafer and to the virtual memory CPU. The added logic and interfacing add only a small percentage to the total RAM area.

Gilman D. Chesley is a Los Altos, CA based consultant specializing in computer architecture. He holds a BSEE and an MSEE from Columbia University.

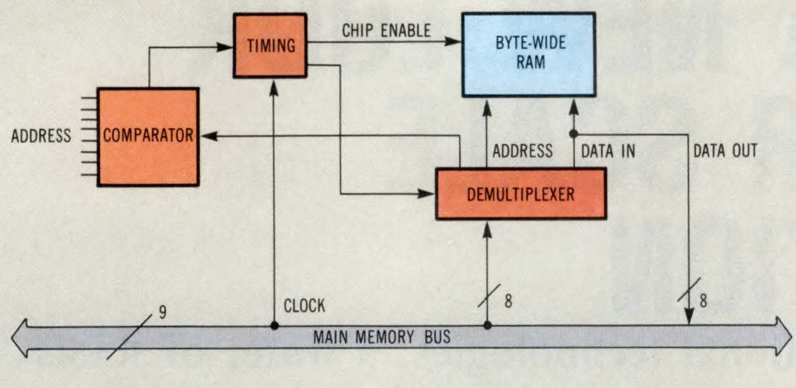


Fig 1 Creation of a wafer of RAMs for virtual memory occurs via alteration of conventional byte-wide RAMs. With the addition of a comparator and demultiplexer, all addresses are uniquely addressable.

Using this method, a wafer memory operation occurs in several bus cycles: opcode/RAM address, column address, row address, and data. (Note that power dissipation on the wafer is not a problem because all but one of the RAMs on the wafer is in standby mode.)

A virtual memory system would typically consist of a virtual memory CPU, possibly with cache, connected to one or more wafers. Initially, systems will be configured using the CPU to test the wafer for good RAMs. One test possibility is for stress, using clock and voltage modification circuits. Of course, wafer yield is dependent upon viable bus and power lines and a reasonable percentage (eg, 50 percent) of operable RAMs, with bad wafers being rejected at the factory. This testing reoccurs each time power is applied, for maximum system reliability. Alternatively, permanent media could hold page table contents.

WSI systems will be fast, compact, reliable, and low powered; however, the primary motivation of WSI will be economic. A specific example compares a PC board of 64K RAMs and a wafer of 64K RAMs. Assuming a byte-oriented 64K RAM and a fast bus synchronous transfer rate of 10 ns (since most bus loading is on the wafer), the RAM cycle time increases by 30 ns.

Parameters of this example could include 2.5-μm geometry, 1/4 square mil bit, and a total area of 32,000 square mils. Furthermore, the RAM is 180 x 180 mils with an active area (excluding pads and scribe area which are not needed with WSI) of 170 x 170 mils. It is constructed in two bit arrays, each of 170 x 85 mils. Since yield is a function of chip size, half a normal chip (built in two halves) increases chip yield. Adding support circuitry could increase chip size to 170 x 100 mils interconnected to 255 other chips on a wafer via a common bus of 9 lines.

To increase yield, chips reside in the central area of the wafer, because chips on or near the periphery tend to have a high failure rate. Each bus line is 2.5 μm wide and 25,600 mils long for a line capacitance of 64 pF. Chip inputs would have high impedance for a capacitive load, and chip output drivers would be tri-state. Bus yield would be on 23,040 square mils of passive area.

Power lines are fused at each chip and bus shorts are burned at factory test time. Since wafer scribing is not required, cutting a thick substrate and growing a thick passivation layer after mechanically masking external macro-contacts provides the self-packaging technique. With a bus, wafer, and chip yield of 50 percent, and a wafer cost of \$35, the result is a \$70 wafer containing 512 Kbytes of RAM with 9 external connections.

Comparing this wafer with a PC board containing 64K RAMs plus support circuitry, the boards have 2048 internal bonds and 1024 external connections, totaling more than 3072 connections, at a system cost of, perhaps, \$640. Thus, RAM WSI offers the possibility of an order-of-magnitude cost savings over printed circuit technology with a considerable savings—in space and power—and significantly increased reliability.

With this same technique, a CPU with a cache and a block mode RAM on the wafer can be the basis for a high performance system. For example, using a RAM with a 256-bit wide internal array, a block of 32 bytes could transfer each memory cycle at a 10-ns byte rate. Total block memory cycle time is then less than 500 ns. A wider bus, with some sacrifice of wafer yield, produces even higher performance.

In the future, the ultimate system would seem to lie on a single wafer (except for peripherals). This would include redundant virtual memory CPUs on the wafer with a self-test capability. Then the first operable CPU tests and configures the RAMs via the page table. The result is a compact, reliable, low power, high capacity wafer system offering a high level of system sophistication at a very low price.

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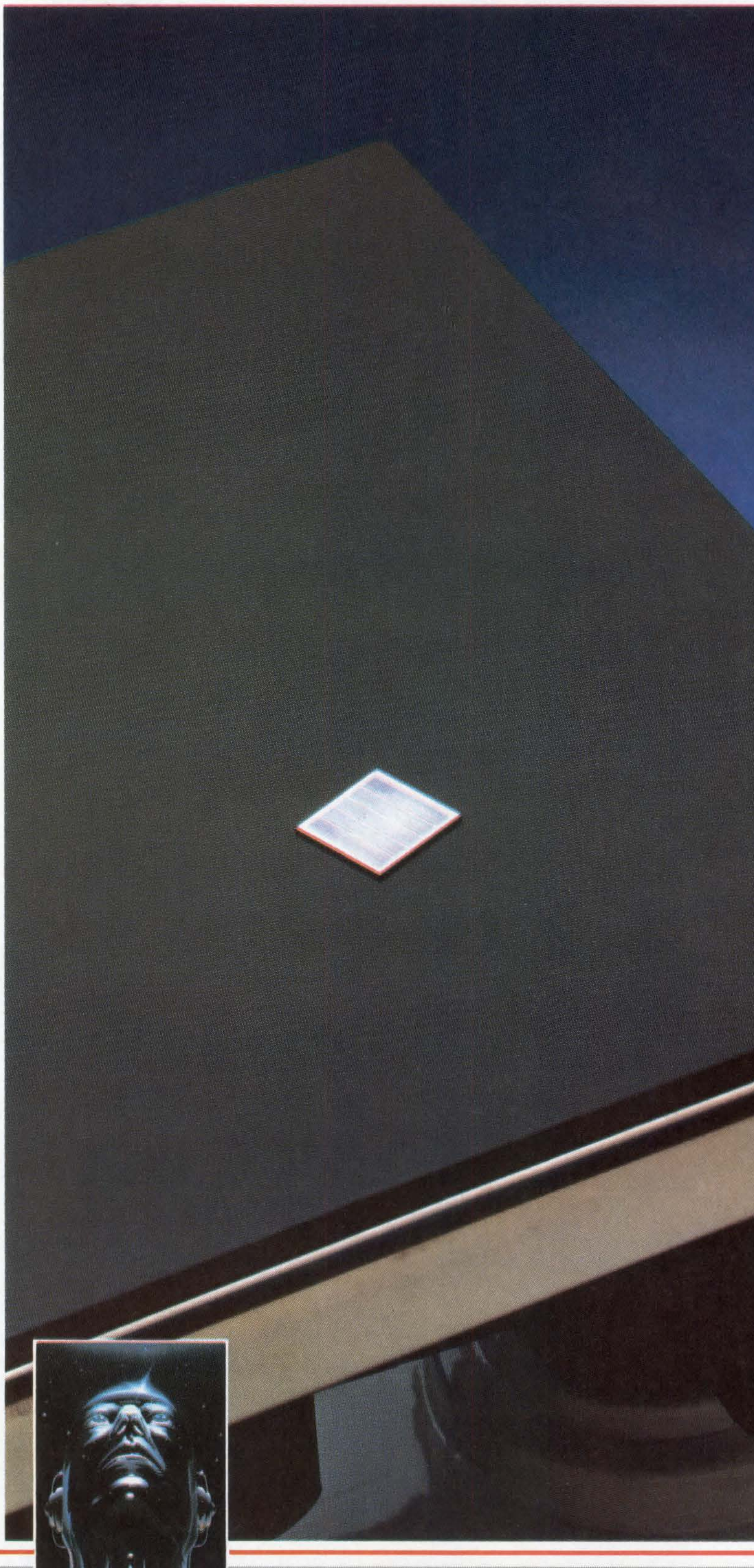

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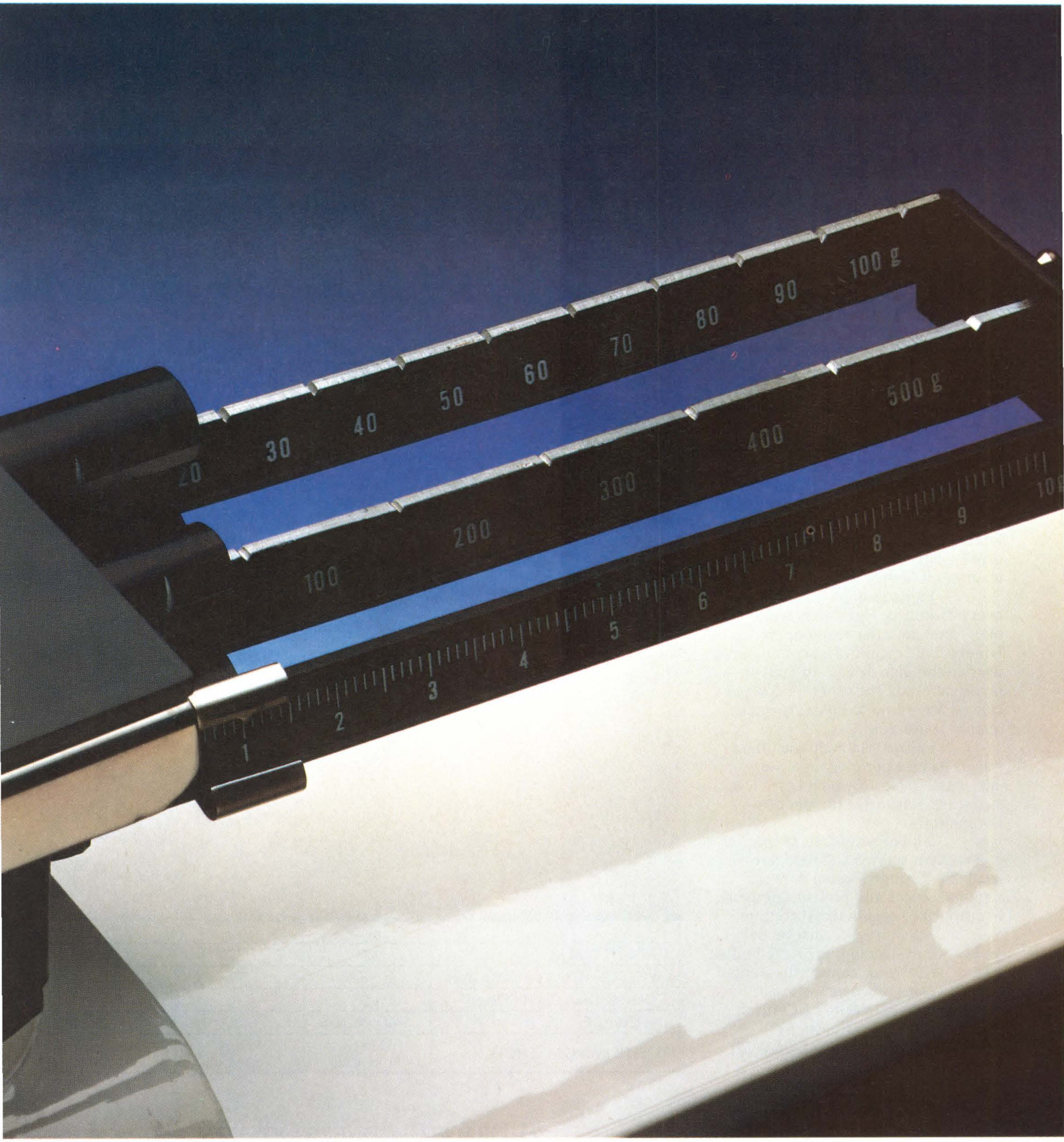

Special report on graphics technology

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CIRCLE 77

SPECIAL REPORT ON
GRAPHICS TECHNOLOGY

After some 10 years of effort by thousands of specialists working countless hours, national and international graphics standards are ready to serve graphics system vendors and users alike. Some graphics standards have been formally blessed with a standards-making body's imprimatur, others will soon follow, and some are still in the definition phase of their development. To meet a variety of market needs, these standards will perform their chores both as standalone graphics packages and as part of proprietary value-added offerings.

Ideally, graphics standards would immediately allow system integrators to incorporate a graphics subsystem into their computer systems with minimal frustration. In addition, graphics manufacturers could have a uniform graphics software specification to build to before adding their bells and whistles. Graphics software developers could also rest assured that their application programs—if they meet the appropriate specifications—would run on any computer or terminal. Finally, these standards would immediately free end users from being locked into one vendor.

These are the ultimate goals of graphics standards. But, as is the case for any standards, these goals can only be met asymptotically with time. The six technical articles to follow illustrate that the standards evolving first are but a small step toward lofty final goals. Many vested graphics interests must be satisfied before agreements can be reached on rules governing their behavior. And, they tend to first agree only about somewhat older, minimal-capability technology.

Despite the elapsed time, controversies, minimal capabilities, and some bitterness, the graphics industry has some standards, and is acquiring more—flawed though they may be. The staff report reveals what these standards are, who developed them, how they are related, and what they do. It sets the stage for the five articles to follow.

These articles focus on various positions and markets in the graphics community and, therefore, reflect a difference in implementation details. Still, although the authors each approach the graphics market differently, they all support the graphics standards that will inevitably come.

Harvey J. Hindin
Special Features Editor

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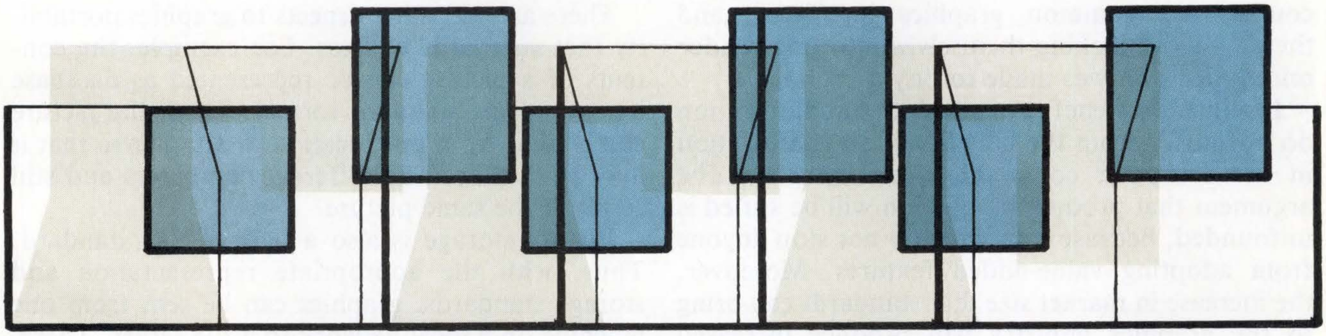
CIRCLE 78

SPECIAL REPORT ON GRAPHICS TECHNOLOGY

GRAPHICS STANDARDS FINALLY START TO SORT THEMSELVES OUT

As the computer industry adopts sophisticated graphics technology for both low cost and high performance products, standards-making activities ensure that applications, data bases, and graphics devices can communicate.



by Harvey J. Hindin, Special Features Editor

From IGES and NAPLPS to ANSI and SIGGRAPH, a bowl of alphabet-soup-like mnemonics represent the bewildering array of graphics standards under study today and the organizations that are studying them. These organizations are working to achieve graphics industry standards that promise a variety of benefits to computer system designers, integrators, and end users. They have, after a long and painful process, met with some successes, and more are on the way. It is important that the computer community, which freely uses graphics technology and is predicted to use it even more, be aware of what is going on.

To do their jobs properly, members of the computer system design community must learn the benefits of graphics standards. This knowledge will enable them, their companies, and their industries to take full advantage of the computer graphics capabilities that are developing apace. They must also have an overview of the relationships between the different standards under development, what the standards do, and how they differ. Equally important, is a knowledge of the organizations active in the standards-making field. Finally, the community must be aware of the various standards controversies so it can look out for its own interests and, perhaps, help resolve problems by actively participating in standards bodies.

A good analogy

The advantages of computer communication standards have become obvious in recent years as disparate machine markets have developed from disparate manufacturers that can, nevertheless, communicate. Like graphics standards, computer communication standards have taken years to develop. After many years, computer communication standards have recently evolved because market forces demanded communication between different machines. The days of end users depending on one vendor for all their computer system needs are over.

A similar phenomenon is taking place in the computer graphics industry. Until recently, it has not had the market demand for graphics-based machines that are transparent to programmer and end user alike. Now, however, as graphics technology becomes ubiquitous on mainframe and microcomputer, the industry has both the motivation and the obligation to provide for, and adhere to, standards.

Consider the benefits

The industry's commitment to standards stems from the many benefits that they offer. These include, among others, host computer portability, display-device independence, ease of application program design, and graphics-containing database portability.

Ideally, a computer graphics industry with agreed-upon and observed international standards would enjoy a market that knows no geographic boundaries. In addition, since each graphics device would have its fundamental behavior well-specified, manufacturers could concentrate on value-added features to make their products unique. They would not constantly have to reinvent the graphics wheel. End users could, of course, use common graphics interfaces, and thereby avoid locking themselves into one vendor once a decision was made to buy a product.

In short, the benefits of graphics standardization do not differ from the benefits of standardization in the computer communications industry. The argument that product innovation will be stifled is unfounded, because standards do not stop anyone from adopting value-added features. Moreover, the increase in market size that standards can bring to the graphics industry will produce increased opportunity for all without stifling innovation—witness what has happened in the home entertainment and local network industry.

As might be expected, each segment of the computer graphics industry has its own viewpoint on what should be standardized and how. And, as might be expected, these views are colored by proprietary considerations. Still, benefits are so great that agreements are being made in major areas.

For example, all groups realize the need for a standard that allows an application program using graphics to work on a host computer, regardless of its manufacturer or operating system. End users of such software are not locked into one computer vendor and can, if they wish, run the applications on a local network containing different computers—said by many observers to be the backbone of the office and factory of the future.

End users are not the only beneficiaries. Software designers can look forward to a larger base of machines that can use their products. Manufacturers will find it easier to sell a new computer (with its "latest" hardware) when it does not make the user's graphics software library obsolete.

Portability does not only apply to users enjoying application programs capable of running on different hosts. Application program developers would be equally happy to enjoy display-device portability. They would favor having application programs that could use any number of different display devices without concern for individual hardware characteristics. How nice it would be if different, CRT-based displays, pen plotters, or printers could use the same application program.

The advantages of such end-user device independence also accrue to end users, who need not worry about having to change their display devices. Clearly, the display-device designer will also have more software product that can run on a machine. In addition to allowing more software product on a machine, a standard software interface to a display device can be implemented as a VLSI-based chip—with all the economies of scale that such technology implies. This is of particular importance to display-device manufacturers. Ideally, a standard graphics device interface chip could be made by a variety of semiconductor firms at a remarkably low price.

There are still other aspects to graphics portability that standards address. For example, the contents of a picture can be represented as database items in some standard format. Then, the picture can be sent from one location to another so that it may be displayed by different computers and still result in the same picture.

Picture storage is also a part of this standard. Thus, with the appropriate representation and storage standards, graphics can be sent from one machine on a local network to a file server. There, it is later called by another computer and displayed on its particular (different) display.

Unscramble the letters

The key to understanding why there is a wealth of graphics standards is to realize that, like the software standards now being adopted—to implement the upper layers of the International Standards Organization's (ISO) seven-layer model for computer communications (the so-called open systems interconnection or OSI model)—graphics standards represent a hierarchy, or set of software layers. And, since the potential users of these layers are a diverse constituency, a variety of specific standards implementations is needed.

The analogy between graphics and computer communication standards is not perfect. For example, the functionality and the number of layers are different. But, it is adequate to help the computer system designer who is likely to be somewhat familiar with the philosophy behind the ISO model.

A significant point to note about graphics standards layers is that, like the computer communication standards layers, just which ones are used for

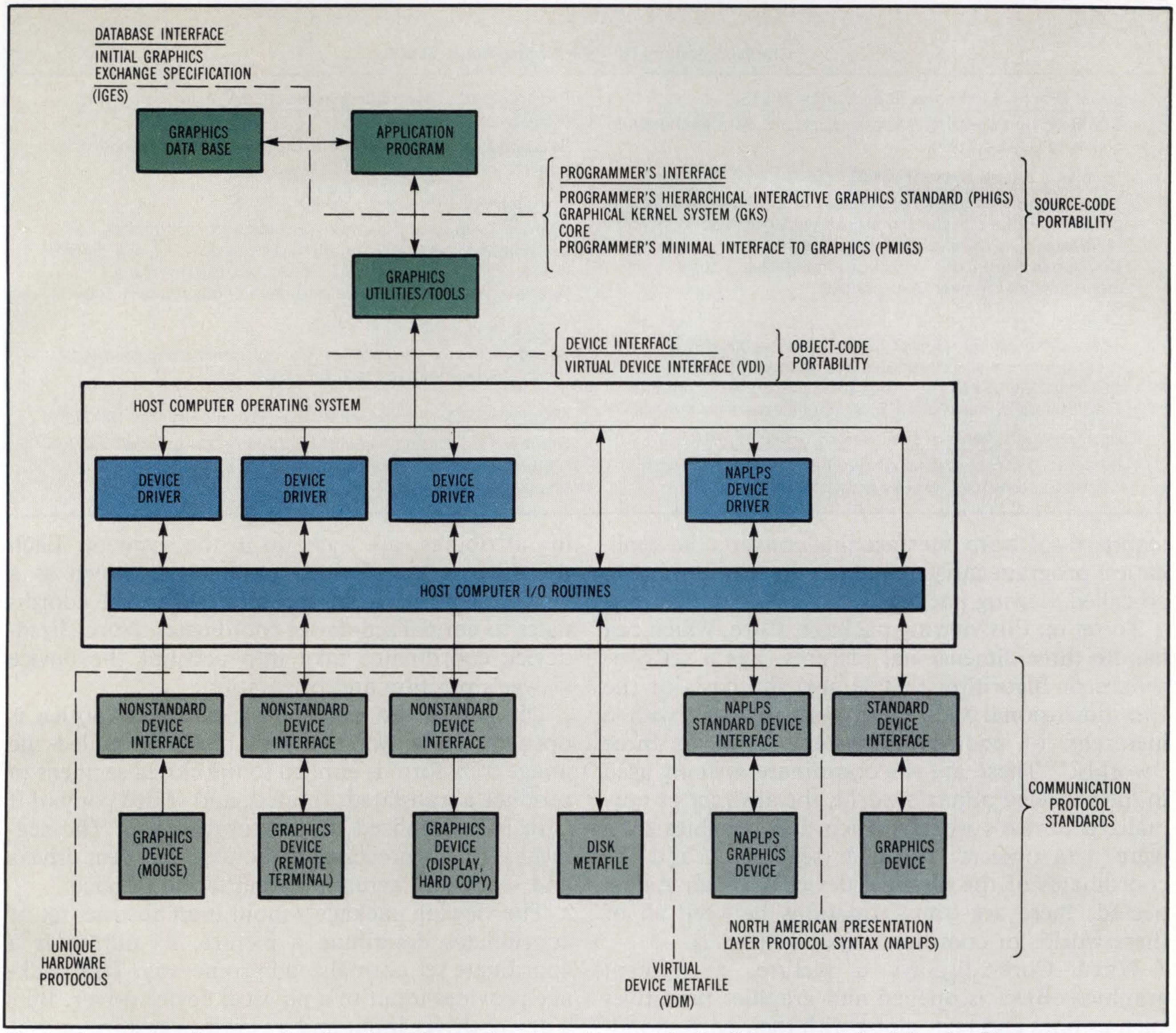


Fig 1 Accepted and proposed national and international graphics standards all have carefully defined software to provide separate, different-functionality interfaces between data bases, programmers, and devices in a graphics-based computer system. The schematic represents relationships, not actual positioning.

a particular application depends on the functional ability of the graphics system under design. For example, because of their relatively "high" position in the hierarchy (Fig 1), it is likely that Core and the Graphical Kernel System (GKS) will be used in computer aided design (CAD) or other sophisticated applications. The needs of simpler graphics software might be satisfied with just a Virtual Device Interface (VDI). Similarly, many "upper" ISO computer communication software layers are not needed if only simple file transfers between identical computers are performed.

While Core and the GKS occupy the same layer in the graphics standard hierarchy, they differ somewhat in performance (see Table 1). Alas, there is as much politics as technology associated with choosing between the two.

The purpose of the GKS/Core software layer is to help someone writing specific graphics application software to work with, or interface to, graphics software utilities and tools. These utilities and tools help provide descriptions of the graphics objects that are to be displayed and used by the application software. Normally, these objects are defined in terms of two- or three-dimensional coordinates in some coordinate system accessed by various graphics-oriented software commands known as graphics primitives. In a business application, these graphics primitives and coordinates might be used to describe the points on a bar chart. In a CAD application, they might describe a VLSI chip's multiple layers.

Once an object's description in a data base is incorporated into the application program itself (by a software standard discussed later), it is the function of the GKS or Core (or yet other standards at the same hierarchical level)—to change the "description" of any picture that the application program uses into an almost actual (ie, normalized) picture. In short, the GKS/Core layer provides a

TABLE 1

Graphics Standards: Their Chores Made Simple

Initial Graphics Exhange Specification (IGES) Standard that specifies file structures for data exchange in high end CAD systems.	Programmer's Hierarchical Interactive Graphics Standard (PHIGS) Extended, high end version of Core for computer modeling applications.
Graphical Kernel System (GKS) Two- or three-dimensional standard that allows application programmers a standard interface with graphics utilities/tools to incorporate graphics into their programs. Developed from Core ideas but emphasizes picture distinguishability over user control.	Virtual Device Interface (VDI) Standard supporting as many graphics I/O devices as possible with as many functions as possible. Device drivers may or may not be needed. The VDI is the interface between device-dependent and device-independent code.
Core Three-dimensional standard that allows applications programmers a standard interface with graphics utilities/tools to incorporate graphics into their programs. First standard, basis of GKS, it emphasizes user control.	Virtual Device Metafile (VDM) Standard for file formats for storing/transmitting pictures in device-level primitives (eg, for disks).
Programmer's Minimal Interface to Graphics (PMIGS) Minimal, low end version of two-dimensional Graphical Kernel System for business graphics/graphics arts.	North American Presentation Layer Protocol Syntax (NAPLPS) Standard for storing/transmitting/compressing videotex-like pictures in device-level primitives (eg, for raster-scan display).

standard software interface that converts the application program carrying picture descriptions into a so-called viewing package.

To set up this viewing package, Core, which can handle three-dimensional pictures, has a set procedure or algorithm that is also the basis of the two-dimensional GKS. Both systems work with a hierarchy of coordinate systems used in three "worlds." These are the coordinate systems used in the modeled object's world, the abstract or normalized device's world (which uses graphics software data objects known as segments), and the coordinates of the physical device's world. As expected, there are transformations between all of these worlds or coordinate systems (Fig 2).

When Core displays a picture, a segment graphics object is opened and graphics primitives such as lines and text, along with their corresponding attributes, are built up in the segment. Each primitive is transformed by what is known as a view transform from the modeled-world coordinates to normalized-device coordinates. Normalized-device coordinates take into account the device viewer's position and orientation.

Ultimately, the segment is closed and another is opened. Then, yet another transform called the image transform is applied to the closed segment to produce a translated, rotated, and scaled copy of it (still in normalized device coordinates). The segment is finally processed by device-dependent drivers and sent to an actual physical display device.

The viewing package's input is an abstract set of coordinates describing a picture; its output is a coordinate set normalized in some way. This package provides input to a physical device driver. But, a device driver input and a viewing package output

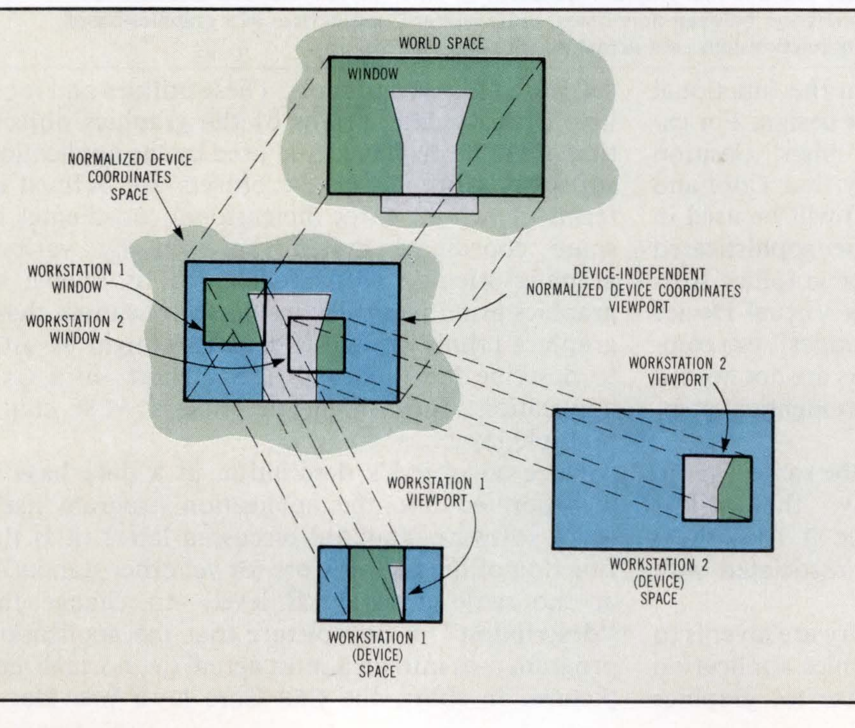


Fig 2 In the "world" space of a real object and its physical coordinates, a graphics window may transform part of the object to graphics display device-independent, "normalized" coordinates. Yet other windows may provide "actual-device" coordinates to a device driver for workstation display of object parts.

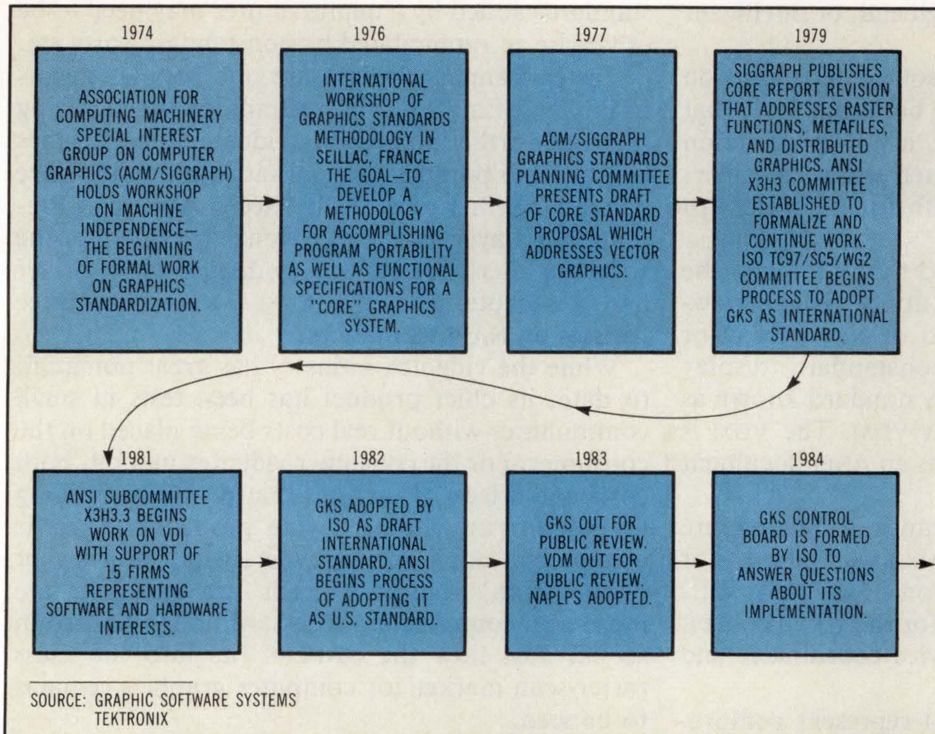


Fig 3 The long march toward graphics standards has many milestones, some of which are shown. ACM/SIGGRAPH started it all with its Core specification. Core will not be an ANSI or ISO standard but will probably be an ACM standard.

must be made to communicate (or be combined into one) by another software standard. This standard is known as the VDI.

The device driver is designed to take normalized picture coordinates as its input and provide physical device coordinates as its output. These physical device coordinates then drive specific graphics devices—be they raster-scan displays or pen recorders. Note that as Fig 1 shows, so-called standard display devices can be driven directly by the VDI interface without the need for a device driver.

Compare and contrast

"Invented" first (Fig 3), Core can handle three-dimensional graphics while the GKS is now a two-dimensional standard. However, work is going on in Europe to define a three-dimensional GKS under the auspices of the ISO.

The American National Standards Institute (ANSI) is the U.S. national delegate to this international body. Both organizations feature an elaborate hierarchy of committees and review procedures to develop and approve their standards. As a result, formal, approved-by-all-concerned-parties documents can take years to appear.

There are other differences between the GKS and Core. For one, the Core task group of ANSI's committee X3H3 is working to extend Core for computer modeling applications that require very realistic object representations. This work, in its early stages, is known as the Programmer's Hierarchical Interactive Graphics Standard (PHIGS).

Core also differs from the GKS concerning control of image representation. In Core, with CAD and computer aided manufacturing (CAM) as the primary application, the graphics system user defines image representations and their attributes. In contrast, with a GKS system, the user does not lose performance ability (ie, commands are obeyed) but the GKS software makes many image representation choices (eg, color or dashed lines). It does this because the GKS system emphasizes (and takes care of) feature distinguishability over user control of color, dot or dashed lines, and the like.

The ANSI X3H3 committee is also writing a standard known as the Programmer's Minimal Interface to Graphics (PMIGS). The PMIGS is important because it is a basic system that programmers without graphics experience can use. It sits in the hierarchy with Core and GKS and is a minimal GKS subset.

More than VDI

It is important to note that the VDI design must be the essence of compromise. On the one hand, the simplicity of a low level VDI is desirable if one wants to, for example, implement VDI software in firmware. On the other hand, the VDI must interface with a variety of high level sophisticated graphics applications like CAD/CAM that use GKS or other high level software. Therefore, it often needs the ability to incorporate high level, specialized graphics device features.

Placing the VDI is a major concern in graphics software design since it is the interface between device-independent and device-dependent code. If the interface is placed too "high," or contains too many functions, then device drivers for simple graphics devices will be large in size and difficult to write. However, if the interface is placed too "low," the device drivers will not be able to take advantage of the features of high end, or intelligent graphics display devices.

Obviously the trade-off is resolved depending on what graphics software will be used for what devices. As might be imagined, a VDI specification is a major feat for a committee whose members represent diverse interests. Unfortunately, the VDI specification is lagging.

Along with the VDI standard that addresses the interface between the graphics utility system (viewing package) and the standard display device (or the device driver for the nonstandard display device), there is the companion standard known as the Virtual Device Metafile or VDM. The VDM is currently under public review as an ANSI document (see Table 2).

Standards for storing and transmitting a picture are just as important to have as standards for presenting it. Thus, the function of the VDM software is to specify file formats for these two chores. The VDM uses normalized device coordinates and primitives to do this job.

Because both VDI and VDM represent compromises in their attempt to provide device-independent presentation, storage, and transmission of graphics, neither standard allows a particular display technology to be used to its full potential. Thus, certain value-added features (perhaps, nonstandard) added by a manufacturer may need to be otherwise accommodated by nonstandard software.

Raster-scanned displays are one popular means of implementing a display technology. Recognizing this, and further hoping that videotex-type displays will become popular, several industrial firms have banded together to push the North American Presentation Layer Protocol Syntax (NAPLPS) as the software interface between a videotex device driver and a videotex display. ANSI's X3L2 committee focuses on NAPLPS matters.

While the videotex industry has great potential, to date, its chief product has been tests in small communities without real costs being placed on the consumer. For the consumer videotex market, both costs and a lack of pictures that people are willing to pay for are industry-wide problems. Specific commercial applications, wherein an industry or organization's business needs are satisfied, are more of a commercial success, although limited in scope. Just how the NAPLPS fits into the mass raster-scan market for computer graphics remains to be seen.

Three dimensions?

The ongoing work to establish graphics standards has generated many controversies. For example, two-dimensional graphics are clearly not

TABLE 2

Status of Key Graphics Standards at ANSI

Standard (Mnemonic)	Draft Proposal To ANSI X3H3 Committee	Public Review	Final Proposal To ANSI X3H3 Committee
Graphical Kernel System (GKS) two dimensional	October 1983	March to June 1984	depends on reviewers' comments
Virtual Device Metafile (VDM)	October 1983	February to May 1984	depends on reviewers' comments
Programmer's Hierarchical Interactive Graphics Standard (PHIGS)	work in progress (November 1984?)	—	—
Virtual Device Interface (VDI)	work in progress	Summer or Fall 1985	—
Graphical Kernel System (GKS) three dimensional	depends on ISO GKS (Fall 1984?)	—	—
Initial Graphics Exchange Specification (IGES)	final document adopted but revisions under study	—	—
Programmer's Minimal Interface to Graphics (PMIGS)	October 1983 (Level m of ANSI GKS)	March to June 1984	depends on reviewers' comments
North American Presentation Layer Protocol Syntax (NAPLPS)	final document adopted	—	—

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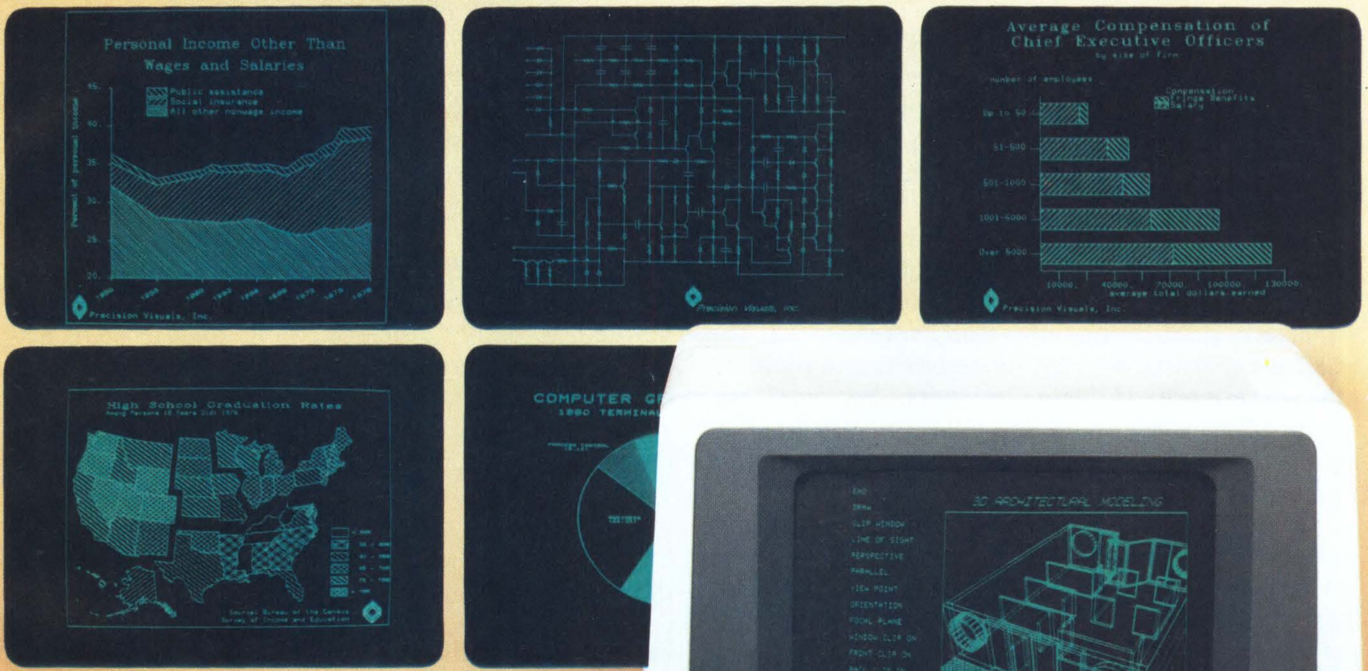

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Horizontal Resolution	**768**	**768**	640	640	800	800	1225	1225	780
Dot Density Ratio	**1:1**	**1:1**	1:2	1:1	1:3	1:1	1:4	1:4	1:1
Screen Size	**14″**	**14″**	12″	12″	12″	12″	12″	12″	12″
Tektronix 4014 Compatible	**STD**	**STD**	NO	NO	NO	STD	NO	STD	STD
Data Tablet Support	**STD**	**STD**	NO	NO	OPT	OPT	NO	NO	NO
Multi-Vendor Printer Support	**STD**	**STD**	OPT	OPT	OPT	OPT	OPT	OPT	OPT
8 Dir. Cross Hair Cursor	**STD**	**STD**	NO	NO	NO	NO	OPT	OPT	OPT
Programmable Function Keys	**STD**	**STD**	NO	NO	NO	NO	NO	NO	NO
Tilt/Swivel Enclosure	**STD**	**STD**	NO	NO	NO	NO	NO	NO	NO
Compatibility	**VT52 ADM3A H1500 D200**	**VT100 VT52 ANSI X3.64**	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52	VT100 VT52
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enough and three dimensions are needed for such applications as high end CAD. Core was the first standard to address three dimensions. At first, Core viewed three dimensions from the line drawing perspective, but it later took raster scanning into account. GKS, which evolved from Core, confined itself to two dimensions.

The realization that Core cannot be an international standard coupled with the need for three dimensions, has sparked a movement to expand GKS to three dimensions. Experts raise no objection to the concept of expanding GKS to three dimensions, according to a study by David H. Straayer, senior engineer at Tektronix Inc's Information Display Division (Wilsonville, Ore). Conducted by letter appeal in *Computer Graphics* (ACM/SIGGRAPH's quarterly publication), the study revealed that the GKS is extensible because its designers can build on the experience of Core designers. For example, before Core came on the scene, proprietary graphics software expressed the graphical rotation of text strings as an angle in degrees.

Core experience proved that this design approach is difficult for the graphics software person to implement in three-dimensional scenarios. So, text strings are rotated in Core by the specification of a so-called text-up vector. This consists of a two-dimensional vector for two-dimensional Core subsets, and a three-dimensional vector for three-dimensional Core. In the GKS, text is also rotated by a text-up vector that is extendable to three dimensions.

Work on three-dimensional GKS is just starting and it will be some time before a fully specified, accepted standard is available. Yet, such an event will happen. ISO's TC97/SC5/WG2 committee, which focuses directly on graphics standards development, has told the Netherland Normung Institute (NNI) standards-making body (Table 3) to produce a document as the basis for a three-dimensional GKS. To help ensure compatibility, this specification will allow two-dimensional GKS operations to be degenerate cases of three-dimensional GKS operations.

Slated for development by mid-1984, this document must go out for ISO comments (Table 4) before it is further processed on its road to being a full-fledged international standard. Of course, once the document is available, aggressive graphics vendors will be busily searching for products to design around it, in order to gain a market edge. This approach is quite typical, as vendors cannot afford to wait for a final document (see the technical articles that follow for examples of this philosophy).

Further complications

While three-dimensional GKS will be compatible with two-dimensional GKS as a degenerate state, it will not be the only three-dimensional graphics

TABLE 3

Who's Who In Graphics Standards

Organization (Mnemonic) (Region of influence)	Membership	Representation	Standard-making task and influence
International Standards Organization (ISO) (International)	voluntary by country*	standards bodies in participating nations. U.S. representative is ANSI	creates world standards
American National Standards Institute (ANSI) (United States)	voluntary	manufacturers organizations end users	U.S. representative to ISO, creates U.S. standards
Deutsche Institute für Normung (DIN)(Germany)	voluntary	manufacturers organizations end users government	German ISO representative, creates German standards
Netherlander Normung Institute (NNI) (Netherlands)	voluntary	manufacturers organizations end users government	Dutch ISO representative, creates Dutch standards
Association for Computing Machinery (ACM) (United States)	voluntary	dues-paying individuals	not yet defined**
Industrial firms	self	self	determined by market share

Notes:
* About 12 countries active

** ACM has voted to generate standards much like IEEE starting this year.

TABLE 4

Status of Key Graphics Standards

Standard (Mnemonic)	Activity Level	Draft International Standard	International Standard
Initial Graphics Exchange Specification (IGES)	under study by DIN	?	—
Graphical Kernel System (GKS) two dimensions	draft standard under review	November 1982	September 1984?
Graphical Kernel System (GKS) three dimensions	work item	Fall 1984	—
Virtual Device Interface (VDI)	not yet work item	—	—
Virtual Device Metafile (VDM)	work item	June 1984	—
Programmer's Hierarchical Interactive Graphics Standard (PHIGS)	not yet work item	1985?	—
Programmer's Minimal Interface to Graphics (PMIGS)	deferred	—	—
North American Presentation Layer Protocol Syntax (NAPLPS)	no activity	—	—

standard. As mentioned earlier, ANSI's X3H3 committee (analogous to ISO's TC97/SC5/WG2 committee) is working on PHIGS, a three-dimensional graphics standard that is richer than either Core or the upcoming three-dimensional GKS. Today's top-down design principles require that graphics systems be allowed to have entities or software commands that call or invoke other graphics entities such as macros and subroutines at multiple levels. This is one rationale for PHIGS. Thus, to facilitate stepwise refinement of a graphics program and subsequent display, a graphics subroutine should be able to call a subroutine, and so on.

Such a hierarchical approach is unavailable in either Core or GKS. Both have what is known as single-level segmentation. In this design philosophy, picture storage and manipulation facilities (ie, segmentation) are limited to a single list of independent subpictures or segments.

Just how the PHIGS will interact with the GKS is unclear. And, the thought of yet another graphics standard pains many observers. The graphics industry continually comes up with state-of-the-art standards before formalizing the previous ones. In any case, PHIGS proponents say it better represents what is needed in three-dimensional top-down graphics design because it is a hierarchical structure. In addition, ISO and ANSI members are already looking into how the PHIGS, GKS, and Core may be made compatible.

When all is said and done, neither the Core, the three-dimensional GKS, nor the PHIGS will disappear—all will be used to some extent. Which will become a "market leader" is an open question. Core, of course, already has an established constituency. Three-dimensional GKS will most likely be an international standard. For its part, the PHIGS is in the early design stages and could end up being a "competing" standard, abandoned, or be made compatible with the three-dimensional GKS. Only time will tell.

The great debate

However, there is more to the controversy between Core and the GKS than mere parochial interests, the not-invented-here-syndrome, and wounded egos. Core came first, is three-dimensional, and is a *de facto* standard with some limited (if incompatible) versions in the marketplace. For its part, the GKS is first making its two-dimensional mark. Critics say it is taking too long to reach the market, a three-dimensional GKS will take even longer, and Core already exists.

First and foremost is the question of whether the ACM is in the standards business (See Fig 4). It has not been in the past but ACM voted in February to become a standards-making body this year, just like IEEE.

Traditionally, U.S. national standards-making activities belong to ANSI, which is the U.S. delegate to ISO. As far as the international voluntary standards system is concerned, U.S. proposals can only be made from ANSI to ISO. Thus, since ANSI has opted for the GKS, even if ACM adopts Core as its "standard," there is no chance it will be an ISO standard.

There is as much heat as light being generated in the Core versus GKS debate. Passions run high on both sides (ACM/SIGGRAPH versus almost everyone else, more or less) and arguments soon leave a level of technical detail that is comprehensible only to experts, and which approach religious zeal.

For some, Core is an attempt by a U.S. body to dominate the graphics standards arena. Others say Core, if made a standard, will confuse users by competing with the GKS, which will be a U.S. national and ISO standard. Thus, a standard Core is seen as an anti-standards step.

There are technical issues too. Designed in 1979, Core has deficiencies and ambiguities, and represents that year's art. More specifically, it lacks provisions for the performance, structuring, portability, and device independence ideas that have evolved in the last five years. Of course, it may be that such things will be said about the latest proposed ANSI/ISO standards if they are not quickly adopted. And, with time, any graphics standard will need upgrading.

Core lacks the language bindings that are essential for real standardization and application portability between different implementations of a standard. In contrast, the GKS has bindings under development for Ada, Basic, C, Fortran, Pascal, and PL/1. Unfortunately, each Core implementation today has its own set of routine names, ordering parameters, and so on. In short, a program written for one Core implementation cannot run on another. Of course, a revised Core need not have this problem.

Core has not been the subject of the extensive peer review process that awaits both the GKS and PHIGS. Core's sponsors, however, intend to review Core this year when they bring it up as an ACM standard. They will use the ANSI review procedures.

The lack of an extensive international review process by members of many interested technical communities implies that Core may not satisfy the needs of experts in related software areas such as programming languages, virtual terminals, transmission protocols, and text processing. Thus, its compatibility with these disciplines is open to question. The GKS, in contrast, is going through a formal procedure.

Those who have labored long and hard in the national and international graphics standards effort (where diplomacy is as important as in the international political arena), see ACM/SIGGRAPH as circumventing their efforts. It is doing this by first trying to get Core through ANSI, and then declaring it a standard on only ACM's say-so. Consider the evidence. The consensus of the computer graphics community is against a Core standard, as evidenced by the recent ANSI committee 47-to-1 vote supporting current graphics standards projects. ACM/SIGGRAPH was the lone dissenter.

Firms point out that multiple graphics standards restrain trade because harried graphics system purchasers limit the number and diversity of systems that they buy since these systems cannot readily talk to one another. They use this as an anti-Core argument. Other observers view this argument as weak since "official" ANSI and ISO standards already proliferate at the same hierarchical level as Core. Finally, in another counter-argument, some say that since Core exists now, if it were a standard, manufacturers would design to it and intergraphics system communications would be a reality quicker than if the industry awaits a three-dimensional GKS.

Other technical differences can be discussed until all but the afficionado are bored. Indeed, the technical arguments become endless and, what

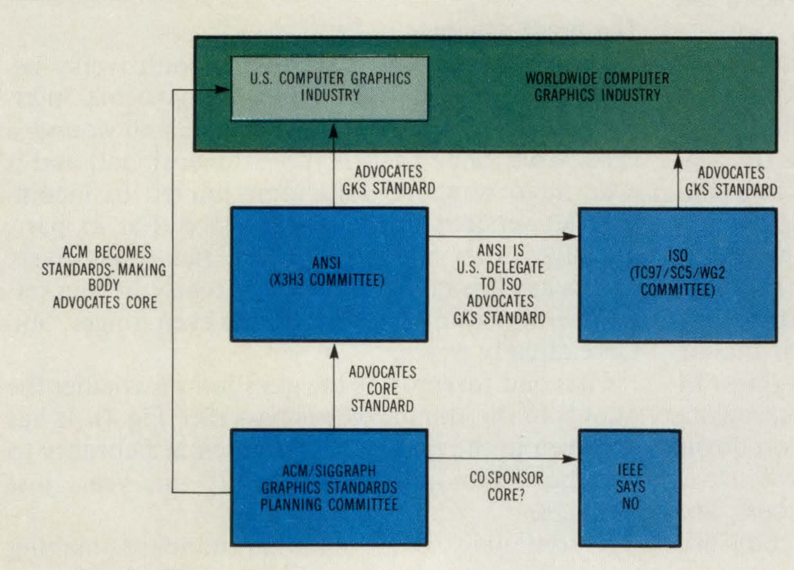

Fig 4 Not able to convince ANSI to opt for Core as a U.S. standard, ACM tried to get the IEEE as a cosponsor. This year, ACM may become a standards-making body on its own and promote Core.

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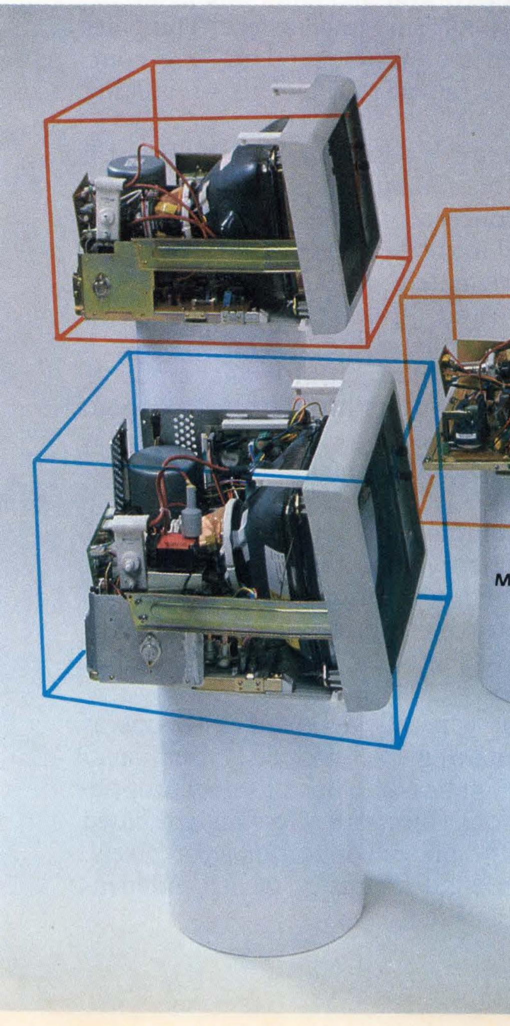

HX-12 SPECIFICATIONS

CRT	12" Diagonal, 76 degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface (NEC 320CGB22)
Input Signals	R, G, B, channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video Bandwidth	15 MHz
Scan Frequencies	Horizontal: 15.75 KHz Vertical: 60 Hz
Display Size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 240 lines (non-interlaced) 480 lines (interlaced)
Misconvergence	Center: .6mm max Corner: 1.1mm max
Display Colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows—8x8 dots)
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

MAX-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
Input Signals	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
Video bandwidth	18 MHz
Scan frequencies	Horizontal: 18.432 KHz Vertical: 50 Hz
Display size	204mm x 135mm
Resolution	Horizontal: 900 dots Vertical: 350 lines
Input Connector	9 Pin (DB9)—cable supplied to plug directly to IBM PC

SR-12 SPECIFICATIONS

CRT	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
Input Signals	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
Video bandwidth	25 MHz
Scan frequencies	Horizontal: 31.5 KHz Vertical: 60 Hz
Display size	215mm x 160mm
Resolution	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
Misconvergence	Center: .5mm max Corner: 1.0mm max
Display colors	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
Characters	2000 characters (80 characters x 25 rows)
Input Connector	9 Pin (DB9)—cable supplied

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amounts to personal preference—an admittedly valid and important factor—plays a strong role. The bottom line is that Core cannot, and will not, be a national and international standard as these terms are understood. And, in the long run, that is the end of the matter as far as large firms in the multi-billion dollar computer graphics industry are concerned. Yes, they have used Core and will continue to support it as market demand indicates. But, in the long run, a graphics standard that is officially accepted worldwide is needed in these days of international trade dependence.

Not dead yet

It should not be thought that Core has no chance to compete with the GKS in modern graphics systems. Core has enough power to make designers of the most modern workstations incorporate it into their products, regardless of standards or political questions. A case in point is the Berkeley Unix 4.2 bsd-based workstation recently introduced by Sun Microsystems, Inc (Mountain View, Calif). It is a good example for system integrators and computer designers to analyze and see if the company's thinking affects what it does in its next graphics system design (for different approaches read the technical articles to follow).

While many disagree with their choice, the company's use of Core is an example of what the firm and the industry perceive to be a need for a delicate balance between tracking the state-of-the-art of standards technology and adhering to established technological standards. Not enough of the former renders a product obsolete. Not enough of the latter makes it difficult to use the product with other gear.

Fully aware of this problem, the company's compromise workstation graphics solution (known as SunCore) is an implementation of the Core standard at the so-called output level 3C, input level 2. Like the GKS, Core allows a variety of input and output levels (see Fred Langhorst's article, "VDI promises graphics software portability," p 197).

For Sun's Vaughan R. Pratt, who discussed SunCore at the Spring CompCon meeting in San Francisco (February 27-March 1), the problems with Core for the designer and system integrator of a state-of-the-art, high end workstation/computer system are threefold. One problem is that the segment is the only structured graphical data object. This means that once they are placed in segments, neither primitives nor their attributes (except for nonappearance attributes) can be individually modified. If a change is needed, the segment must be rebuilt from the beginning.

The second objection lies in that the only global modifications that can be performed to affect Core primitives are limited to changes in image transforms. Moreover, since image transforms are limited to translation, rotation, and scaling, with no view transform, rotation other than around the z-axis is not useful in most cases.

Finally, as far as hierarchy is concerned, a segment is the end of the matter. Simply put, a segment cannot be part of another segment. In Pratt's opinion, limitations one and two swamp three but are tolerable. But, one and two can be fixed while three cannot. If one and two were fixed, three would become an important limitation.

As mentioned earlier, three limits what can be done using today's top-down design and programming techniques. Clearly though, for Sun, design alternatives available to Core are flexible enough, three dimensions are absolutely necessary, and most importantly, the Core standard exists, and has a strong base in the computer graphics community. Finally, the SunCore started when two-dimensional GKS was even more uncertain than now and three-dimensional GKS was mere speculation.

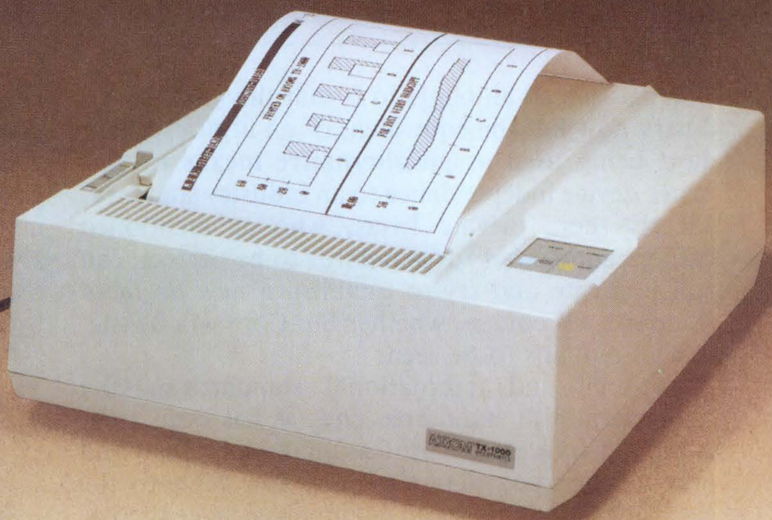
The bottom line is that Core cannot, and will not be a national and international standard as these terms are understood.

Sun did not stop at "minimal" Core standards and the firm has also implemented a major portion of the proposed raster graphics Core extensions including shading, polygons, and rasters. Thus, yet another version of a graphics standard—the company has added further embellishments—is seeking a market niche.

Moreover, the firm's design philosophy has still another lesson for computer system integrators. While Core is concerned with continuous linear figures embedded in three dimensions, raster operation (which originated at Xerox's Palo Alto Research Center some 10 years ago) is concerned with rectangular regions of binary pixels. As a result, while Core is concerned with what amounts to linear transformations in three dimensions to go from one "world" to another, a raster operation is concerned with Boolean combinations of rectangular regions.

The Boolean combination raster operation is of interest for one major reason. It is a two-dimensional resolution-dependent operation, closely matched to modern software, hardware, and VLSI-chip technology for raster-oriented or bit-mapped graphics devices.

Since there is no generally accepted raster operation graphics standard, neither proprietary, national, or international, Sun has developed its own proprietary raster operation, object-oriented standard based on what it calls the pixrect or rectangle of pixels. Indeed, SunCore achieves raster device independence based on pixrects.



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What this all amounts to is that the graphics industry now has the equivalent of an in-house standard being used as an alternative means to give raster device independence to an industry standard. Clearly then, private firms, who as mentioned earlier cannot wait for standards to be perfect, can still innovate and try to establish a new *de facto* standard. Of course, whether SunCore will be successful remains to be seen.

National and international standards-making bodies establish standards, and, as has been seen, computer-interested professional societies and graphics-oriented manufacturers can get into the act. Indeed, anybody can get involved since there is no law against it. For example, aircraft manufacturers and the National Bureau of Standards were behind the Initial Graphics Exchange Standard (IGES), a metafile-like graphics standard now part of the ANSI Y14.26M standard.

The IGES exists because it was impossible to communicate design and data files between different CAD/CAM systems used in the aerospace industry. It has been adopted by computer system designers and integrators interested in serving this industry. With the IGES, for example, an engine mount design tape, built up on one CAD machine can be modified on another.

As shown in Fig 1, the IGES is a graphics standard that allows database information to be used in an application program in a standard way. Once GKS evolves, it is expected that standard software will allow IGES to "talk" to GKS.

What is really available

It is all well and good to talk about best-case standards. But, firms that want to put products on the marketplace today cannot wait for the last word from ANSI or ISO. Moreover, they may have customer bases to protect. The five technical articles that follow well represent the details of what both new and well-established firms are doing with the evolving graphics standards. Because they are relatively easy to implement, offer many applications, and are the most advanced, and therefore offer the least risk of major change, the GKS and VDI have received the most vendor interest.

Communication Dynamics's (Wilsonville, Ore) Terry Hamm and Gar Bergstedt explain how they took another graphic software firm's implementation of the VDI and designed application software to enable managers to prepare personal computer-based illustrations for their presentations. No mere happy end-user story, the article shows how the choice of an implementation was made, what the practical problems were in developing the application software, and what pitfalls the previous user of a VDI implementation must look out for.

VDI is one of the standards that has been quickly adhered to by the graphics software industry and Digital Research Inc's (Pacific Grove, Calif) Fred Langhorst explains why, and how his firm implemented its version to make device-independent graphics application software for hardware manufacturers, software designers, and end users alike. His careful explanation of what portability really means is must-reading for those overwhelmed by unrealistic portability claims by vendors.

Private firms can still innovate and try to establish a new de facto *standard.*

Integrated Software Systems Corp (San Diego, Calif) more commonly known as ISSCO, has had proprietary graphics application software for years and, like other firms with *de facto* standard software, must protect its market and its customers from obsolescence. Therefore, as explained by Thomas Wright, it has opted to incorporate its version of the GKS graphics standard in its products. The company's comparison of the minimal capability, low end GKS with its full-function, high end product points out just what can be expected from standards and what they can do, in contrast to what may be obtained from a mature product.

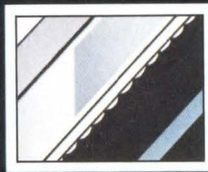
Lexidata Corp (Billerica, Mass) also has a product line that has a well-defined market share. With one eye out on standards, the firm has chosen, at least for the specific product line discussed in its article, to emphasize the line's open-system architecture and extensibility as a top-of-the-line offering. According to Jack Huisman, it offers accommodation of graphics standards such as GKS as "conceptual constructs." The firm's article emphasizes the upgrading approach as a way to incorporate new graphics functionality.

For its customers, Tektronix, Inc (Wilsonville, Ore) is offering a GKS implemented in software as part of its proprietary, high end graphics software. Author Andrew Davis explains how the two graphic software systems work together to provide all the advantages that one might expect from combined packages. Tektronix's Level 2B GKS is a company-enhanced version that offers such features as memory management. Its existence well represents the real-world evolution of graphics standards as the firm changes with the times and supports (and continues to support) first its own *de facto* standard, then the ACM's graphics standard known as Core, and then the national and international standard-to-be GKS.

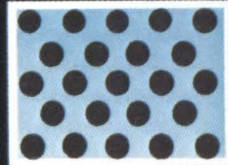
Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

High 722 *Average 723* *Low 724*

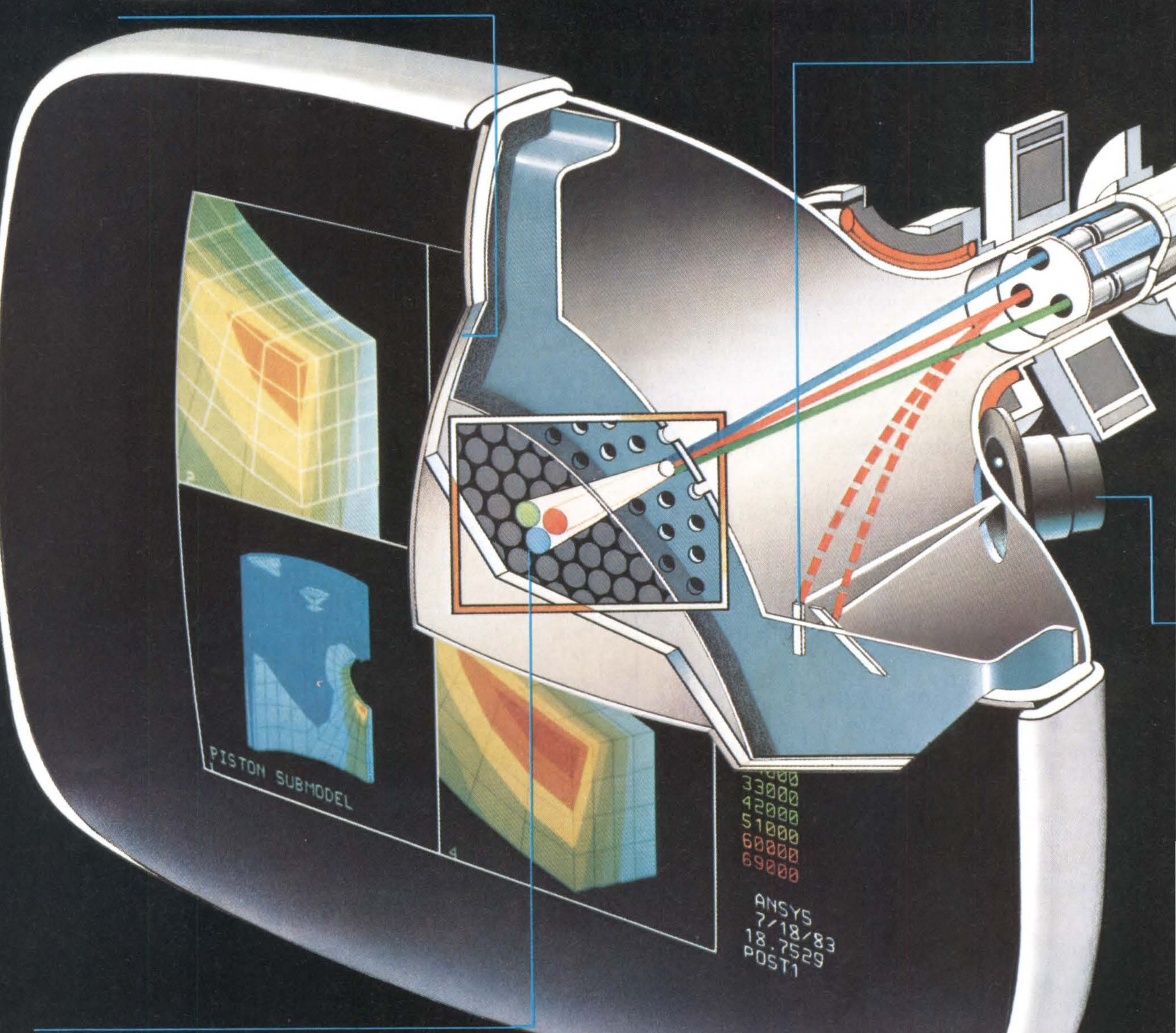
Who solves the misconvergence problems no one else will talk about?

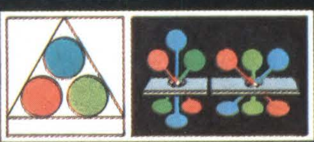


An aluminum layer between the shadow mask and the screen reflects light from the phosphor dots out toward the viewer and at the same time prevents errant screen light from reaching the photodetector.



The 4115B's patented AutoConvergence is accomplished by applying non-parallel indexing phosphors at precise angles and positions at the rear of the CRT shadow mask, detail at left.





Delta configuration of the electron guns helps maintain both high resolution and optimum spot profile throughout the screen—not just the center.

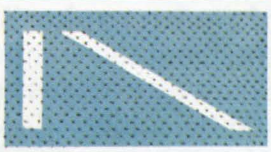
Tektronix.

The higher the visual resolution of a color display, the more difficult it becomes to converge the color beams at a precise point.

Yet, without precise control of convergence, productivity gains promised by high resolution graphics simply can't be realized.

That's why Tek designed the 4115B with AutoConvergence as our engineering prerequisite.

The engineering work environment is tough on high resolution displays. A shift in display angle for better viewing. Mild vibration from a stray elbow. Minor temperature change. Circuit drift. Tube aging. The earth's magnetic field.



A photodetector picks up light from the indexing phosphors. A microcomputer then compares instantaneous beam positions with factory specifications. Convergence corrections are generated to make the two coincide.

They all can cause the color line blurring effects commonly called *misconvergence*.

Loss of detailed information, especially in corners. Fuzzy, fringed colors. And visual ambiguity. All of which can lead to user fatigue, error and loss of productivity.

Until the 4115B, manual reconvergence was typically up to an hour-long task for a service technician—resulting in even more lost time.

No wonder most display manufacturers won't talk about the problem. But Tek will. Because we solved it with our exclusive AutoConvergence.

Push one button on the 4115B and all three electron guns are converged automatically. In 20 seconds. Not just in the screen center but from corner to corner.

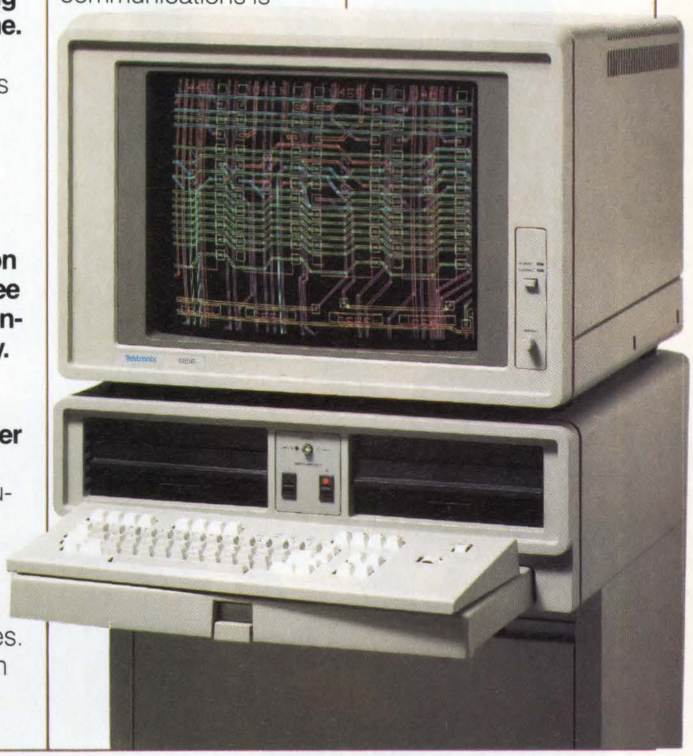
Convergence accuracy is within .25mm, as compared to the 0.3mm to 1.0mm achievable by manual or other techniques. There's no interruption to work, so there's no loss of productivity.

The 4115B's high performance doesn't stop with AutoConvergence. It just begins there. You can apply its 60 Hz non-interlaced, 1280 x 1024 display, 50,000 vector/second redraw speed and user selectable 32-bit coordinate space to optimize productivity on any application.

Large area fills are accomplished at 125 million pixels per second. Standard host communications is 19.2K baud.

So if you want to start with the highest resolution and work at your best all day, every day, call your Tek Sales Engineer. For literature or the location of your local Tek sales office, call toll-free: 1-800-547-1512. In Oregon, 1-800-452-1877.

Call Tek



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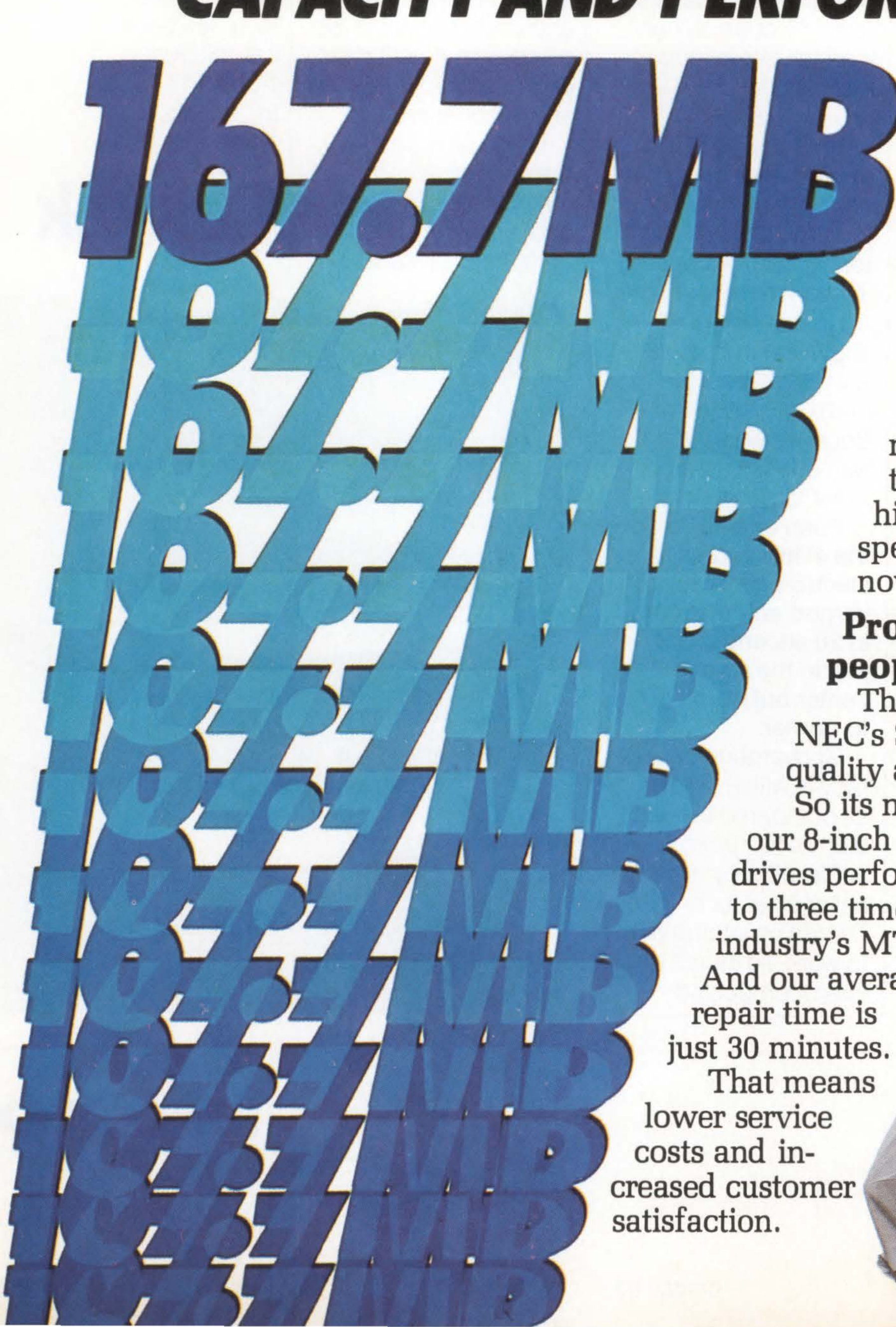
CIRCLE 83

DRIVE YOUR SYSTEM TO NEW HEIGHTS.

UNPARALLELED 8-INCH WINCHESTER DRIVE CAPACITY AND PERFORMANCE.



The drive is on. Your customers expect more and more from computer systems today. And one of the best ways to stay ahead is to specify 8-inch Winchester drives from NEC Information Systems.

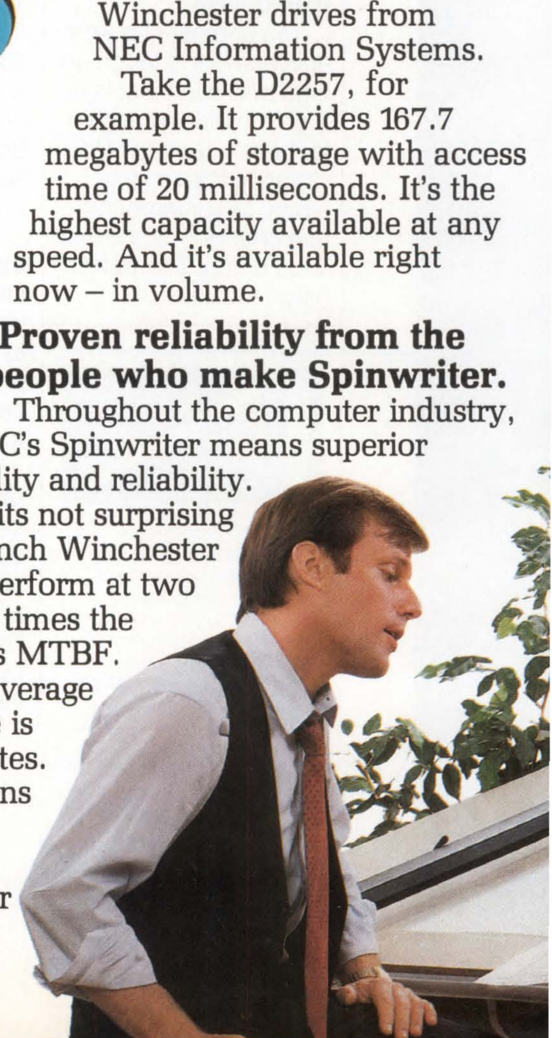
Take the D2257, for example. It provides 167.7 megabytes of storage with access time of 20 milliseconds. It's the highest capacity available at any speed. And it's available right now – in volume.

Proven reliability from the people who make Spinwriter.

Throughout the computer industry, NEC's Spinwriter means superior quality and reliability.

So its not surprising our 8-inch Winchester drives perform at two to three times the industry's MTBF. And our average repair time is just 30 minutes.

That means lower service costs and increased customer satisfaction.



We use a conventional SMD interface.
So our drives are easy to use.

It's simple to integrate NEC's 8-inch Winchester drives into your system. The reason is our standard Storage Module Device (SMD) type interface.

In addition, you wind up with significant savings in installation, packaging, maintenance and cost-of-ownership.

NEC. Technology drives us.

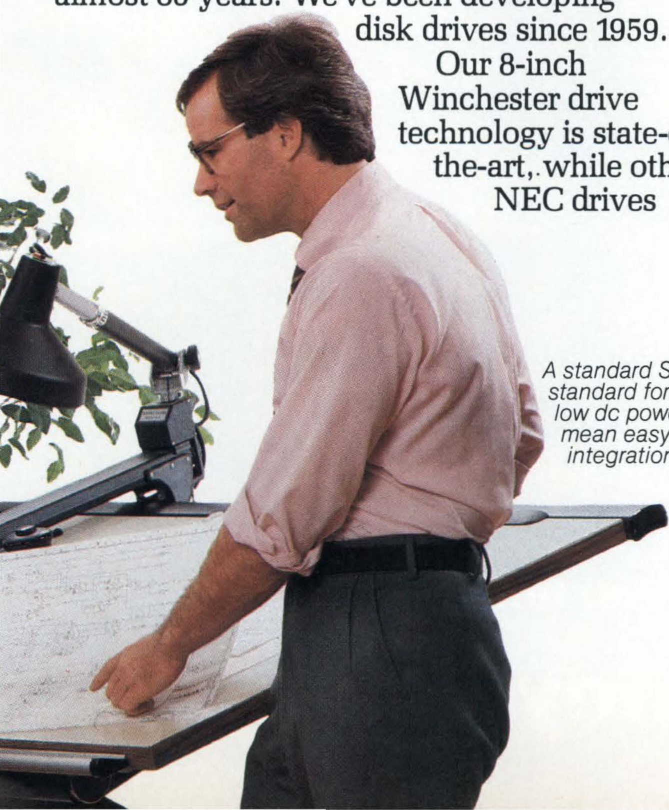
NEC has been pioneering advancements in electronics for almost 85 years. We've been developing disk drives since 1959. Our 8-inch Winchester drive technology is state-of-the-art, while other NEC drives incorporate such advanced technology as plated media, thin-film heads and optical recording.

Clearly, NEC remains at the leading edge.

For more information on NEC 8-inch and 5¼-inch Winchester and flexible drives, or the name of your nearest NEC representative, call 1-800-343-4418 (In Massachusetts, call 617-264-8635). You'll find out why more and more OEM's are saying "NEC and me."

An evaluation unit will be shipped within 72 hours from the time your PO is received.

Choose from four high performance capacities: 25.7, 42.5, 85.0 and 167.7 MB.



A standard SMD interface, standard forms factor and low dc power requirements mean easy system integration.

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CIRCLE 84

ANATOMY OF A GRAPHICS EDITOR—THE INSIDE STORY

Designers can benefit from a detailed analysis of how standard-based software creates a real world graphics application.

by Terry Hamm and Gar Bergstedt

Research proves that the use of overhead presentations can greatly enhance engineering or business presentations. However, there is a problem in developing such presentations. Currently, managers have three means of obtaining transparencies. They can hire a graphics artist, scribble out something of their own, or use one of the few available computer graphics software packages.

Unfortunately, fees for graphics artists are high, and waiting for the finished product is time consuming. Many computer graphics software packages require large mainframe systems and/or the equivalent of a college degree in computer graphics to run them. This leaves the most-used method—scribbling out the overhead by hand. This last option can cause frustration for speaker and audience alike.

To solve this problem, Communication Dynamics has created a graphics editor known as Sound Presentations. As the company recognizes, to be useful, a graphics editor must be easy to learn (30 min for the average first-time user), easy to use (an infrequent user should be able to produce output for a presentation in just a few minutes), and able to do graphs, maps, and text with diagrams. Furthermore, the editor must be portable and, without changing the developed program, be able to run on multiple microcomputer systems.

A graphics editor must also have certain functionality, such as the ability to create text, lines, boxes, circles, and polygons. It must also copy, delete, move, scale, rotate, group into symbols, ungroup, and change attributes on these objects. Additional functions needed are the ability to save, restore, preview, and list pictures and symbols, and undo any action taken (ie, delete a line and then bring it back again). Finally, the editor must provide online help for all its functions.

How to design a graphics editor

With these functional constraints in mind, the primary graphics editor design consideration is deciding on an appropriate development approach (Fig 1). The major question here is the usual one of "make versus buy." This dilemma focuses on whether the program can be built from the ground

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Gar Bergstedt is vice president of research at Communication Dynamics, Wilsonville, OR, where he is responsible for new product ideas and user interface design. He holds a BA from Evergreen State College.

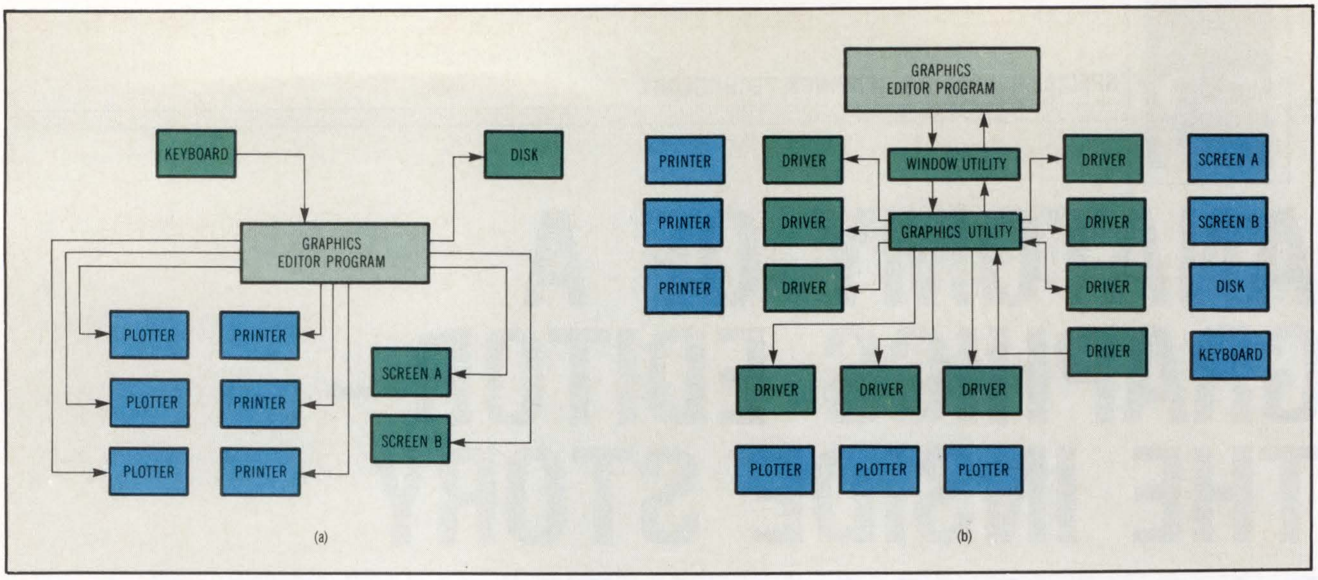

Fig 1 The Sound Presentations graphics editor can be developed from the ground up (a), or with the aid of a graphics tool kit (b). Tools allow a faster time-to-market while custom design offers only incremental technology advantages.

up or if use can be made of graphics software development tools currently on the market.

For Communication Dynamics, time-to-market proved to be more important than the incremental advantages that could be obtained by its own custom graphics utilities. Therefore, the firm set about establishing the need for a graphics tool kit, and creating the requirements for these tools. They had to be complete, easy to use, efficient, and portable. It is important to define these four attributes of a graphics tool kit. A complete set of tools offers a full set of utilities that enable developers to concentrate on construction of the specific application. They need not spend time developing the tools themselves.

An easy-to-use set has a good match to the development language in use. Its primitives blend well with the application being developed. Of course, an efficient tool kit is such that the data structures and code for its primitives are not costly in memory utilization nor in runtime performance.

Finally, portable tools make transporting the application between different microcomputer systems easier. This means that an application is source-code-portable between machines (assuming language compatibility between machines), and the application can continue to deal with hardware-specific graphics devices in a device-independent manner.

Making a choice

Two approaches were available to the company to take care of the requirements and constraints already mentioned. The company could use a language with built-in graphics capabilities, such as Microsoft's Gwbasic; or it could use a library of callable graphics primitives. The second option was selected as no language with built-in primitives existed that would provide support for multiple devices, nor did one exist that was portable to a wide variety of hardware environments.

The next decision focused on which library to use. There were just two graphics utility packages available at the time the choice was made on microcomputers—Graphic Software Systems' (Wilsonville, Ore) GSS-Drivers, and Digital Research Inc's (Pacific Grove Calif) DRI-GSX. Experience with both packages, and the importance of versatility, led to the choice of the GSS-Drivers. This choice also offered a window system called GSS-Toolkit:Window Manager to assist in creating what the company felt was the most friendly, and easy-to-use, window interface.

There were several other reasons for the choice of GSS-Drivers. For one, it works under both MS-DOS and Unix and supports a high level C language interface to its library. In contrast, GSX is available in CP/M and MS-DOS, but only has an assembly language interface. For another, as mentioned, GSS-Drivers offers performance and user- and developer-friendly features not included in GSX. These include symbolic driver names, preserving aspect ratio so that pictures will map from one device to another, and additional graphics input features like rubberbanding.

GSS-Drivers also provides error indicators back to the calling routine. This feature lets the program catch certain runtime errors and respond accordingly.

Explaining some GSS-unique features can aid in the understanding of their utility. For example, a symbolic driver name is a name like "display" or "printer." GSS-Drivers uses these names rather than a preconfigured device number because they can be equated to other devices. Thus, system reconfiguration is simplified.

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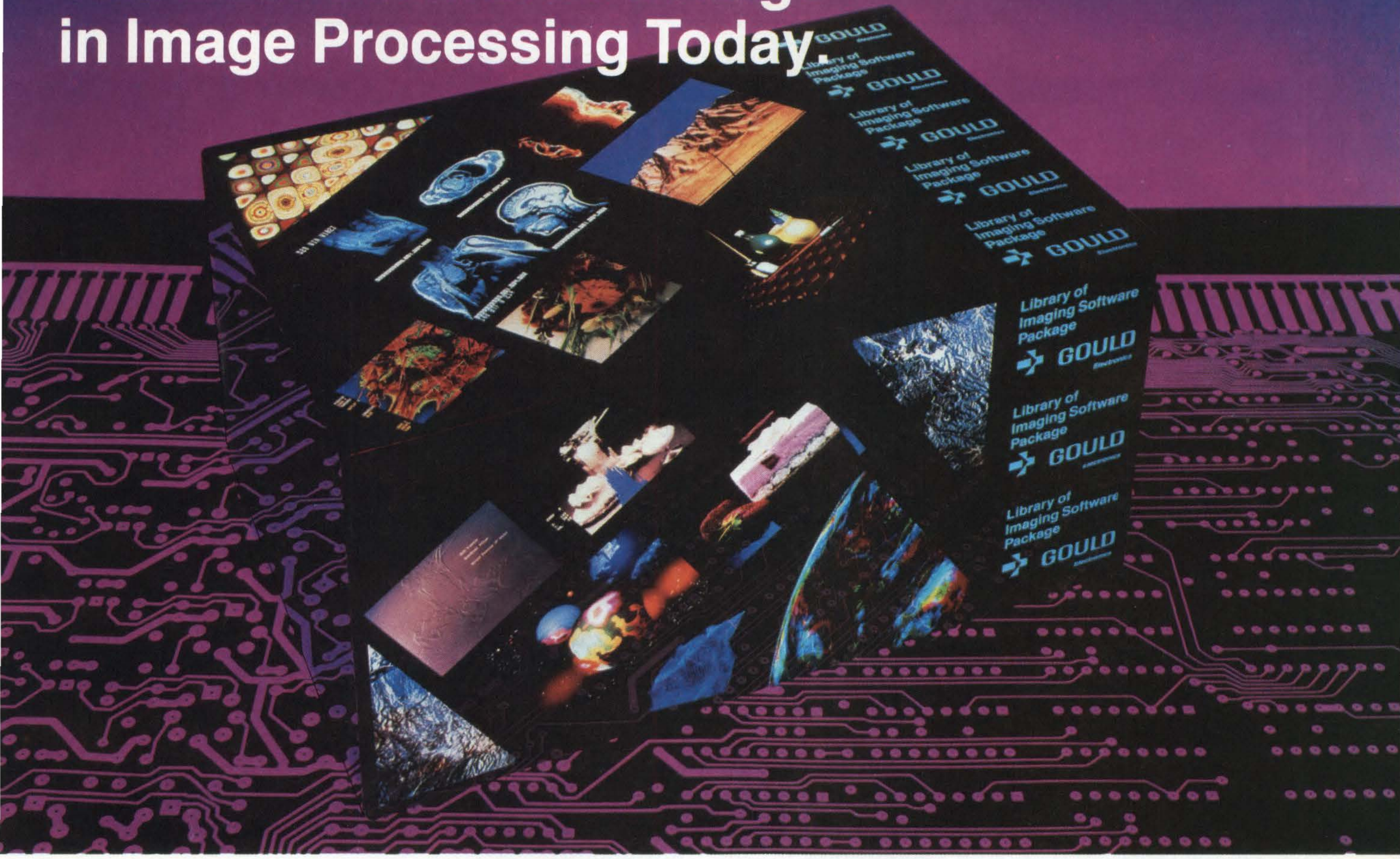

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To assist LANDSAT, specialized classification, and recognition applications, Gould proudly announces LIPS Plus with the following features:

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- Thorough measurement and analysis—spatial and radiometric quantification. Near real-time histogramming.
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IMAGE CAPTIONS

Top:

- *Left back corner: 2-D FFT processed in 2 minutes with LIPS Plus.*
- *Four 1024^2 medical images: multimodality, split screen display.*
- *Face: CT scans in 3-D modeling, plastic surgery at Mallinckrodt.*
- *Mountains: LIPS assists fast graphics hardware and large memory matrices with GKS-based Auxiliary Graphics Processor. Courtesy S.A.I.*
- *Pseudo-colored flowers: shows LUT manipulations. Note graphic load display plus intensity reference scale.*
- *Same 1024^2 flowers: shows color cut and paste in 1 frame time.*
- *Jars and pens: Synthetic image like #4, courtesy Pacific Data Images. Photo by Jim Weil.*

Bottom:

- *Two corners: LIPS driver supports 1024^2 LANDSAT imagery, courtesy NASA-Ames Research.*
- *Top bas relief: Matrix filter, the basis of classification and recognition. LIPS allows kernels of any shape and size and executes at video rates.*
- *Histogram: line or pixel analysis under LIPS.*
- *Spheres: fast Z-buffer merge, courtesy Rensselear.*
- *Cake and strawberries: 1024^2 looks good enough to eat.*
- *Bottom: mesh algorithm, courtesy Lunar & Planetary.*
- *Weather satellite: shows graphics overlay, courtesy MacDonald Dettwiler.*

GOULD
Electronics

CIRCLE 86

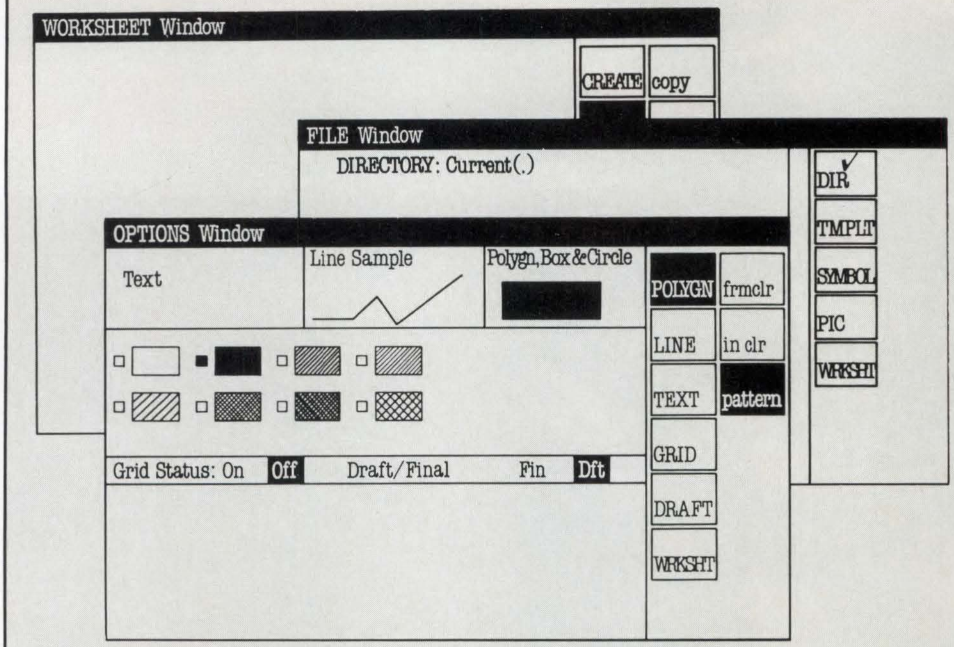

Fig 2 The Windows package, under the control of a window manager program, offers logical I/O devices. As shown, they may overlap and perform a variety of functions for the graphics designer. Their size can vary and they can switch in and out of the screen.

Preserving the aspect ratio means that the graphics software is cognizant of the relative dimensions of the output device it is using. For example, a printer has a longer vertical dimension than horizontal. On the other hand, a plotter and display usually have a longer horizontal dimension than vertical. Drivers takes this into account when graphical data is displayed.

Simply put, GSS-Drivers is a set of subroutines that provides a standard way of communicating computer graphics to devices. As a proposed standard, it is also known as the virtual device interface (VDI).

Indeed, this VDI is an implementation of the proposed American National Standards Institute (ANSI) device interface level graphics standard (a proposed international protocol by which a program communicates to graphics devices like displays, printers, plotters, and mice). It provides Sound Presentations with two advantages.

First, GSS supports a large number of graphics devices. Second, if this VDI is accepted as an international standard, then the Sound Presentations product can run on even more devices.

GSS-Toolkit:Window Manager, the other part of the graphics development tools, offers a set of routines to ease development of an interactive graphics application. A window is a logical I/O device (Fig 2). It appears on a screen as a rectangular area in which output can be drawn, and to which input may be directed.

There may be several (potentially overlapping) windows on a screen. The window manager controls the input and output from each window and regulates the visibility, overlapping, and other window characteristics. For this design, the combination of GSS-Drivers (VDI), and GSS-Toolkit:Window Manager meets the previously mentioned requirements for completeness, ease of use, efficiency, and portability.

Implementation process

With the selection of a graphics utilities package, the development cycle for Sound Presentations began with the prototyping of several user interfaces. Here, GSS's tool saved development time. Indeed, the graphics primitives were extensive and powerful enough so that it was easy to build most of the interface prototypes in less than two days.

These prototypes also played an important role in the user interface design. For example, they showed aspects of the interface that would otherwise be difficult to envision. These aspects include hand and screen coordination for menu selection, object creation and selection, and inconsistencies in design event sequencing. Other prototyping aids were valuable in the best placement of text input, and the determination of the visual feedback needed during line drawing.

As with any design, proper placement of text input is important and should enable users to see text as they enter it into the graphics editor. Initially, Sound Presentations used the bottom line of the display as a text buffer. Then, the text was moved to a specific location after it was typed in.

The font, color, alignment, and size of the text were then changed. After prototyping this approach, the designers saw that it did not provide sufficient user feedback. In a new approach, designers made

a change in which the text appears immediately with its attributes at any location the user chooses. The tool feature allowing this design is the ability to input characters one at a time, and then write them out in either a visible, or in an erase mode.

The much-needed visual feedback during object creation comes from actually seeing the line that is about to be drawn. The first design approach was to have the user select points, and then correct them after they were selected. By using the VDI mode known as rubberbanding, the user can see the line as it is being drawn.

Once it was determined which design details performed well, and which did not, the software designers were able to complete the design process. In this way, the design was verified with the firm's marketing department and continued to the implementation stage.

The two sides of device independence

The implementation stage demonstrated the double-edged sword of device independence. When tools designed to run on many different graphics devices are used, the designer has to pay the price of generality. Simply put, generality means that the tools may not support the special features of any one device, but rather support the broadest feature range of all devices.

In one case, sampling input from the keyboard and mouse in order to move the text cursor with the mouse and, at the same time, type text to the screen, was desirable. This feature is currently beyond the tools' capability. In another case, it was valuable to use various text rotation angles. However, neither the tools nor the device hardware supported such a feature.

The beneficial side of device independence can bring more than what is initially expected. First, there are the expected benefits like portability (ie, being able to run on a large number of devices without any program changes). Then, there are others such as a graphics mode that makes it possible to move the company's own cursor across the screen.

In a new approach, designers made a change in which the text appears immediately with its attributes at any location the user chooses.

Throughout the implementation process, the GSS tools really do the job. The graphics primitives like polyline, circle, polygon, and text are used to create graphics. For file access, the I/O package included in GSS-Drivers is used to connect to a directory, list a directory, open, read, and write. In fact, most of the attributes associated with displayable objects, such as color and size, are supported with the underlying VDI structure. As mentioned, the single, most beneficial aspect of the GSS tools, however, is the time saved in design and development.

Inside sound

Out of the development and implementation cycle emerges a graphics editor that is easy to use, easy to learn, portable, and extensive. Its four parts comprise a worksheet window (where pictures are composed and edited), an options or attribute window (where line colors and text size, among others, can be changed), a file support window (where a designer can save or restore pictures or parts of a picture), and a help window which provides online help for the current set of menu items.

The worksheet window is used for picture composition and editing. In this window, the user creates

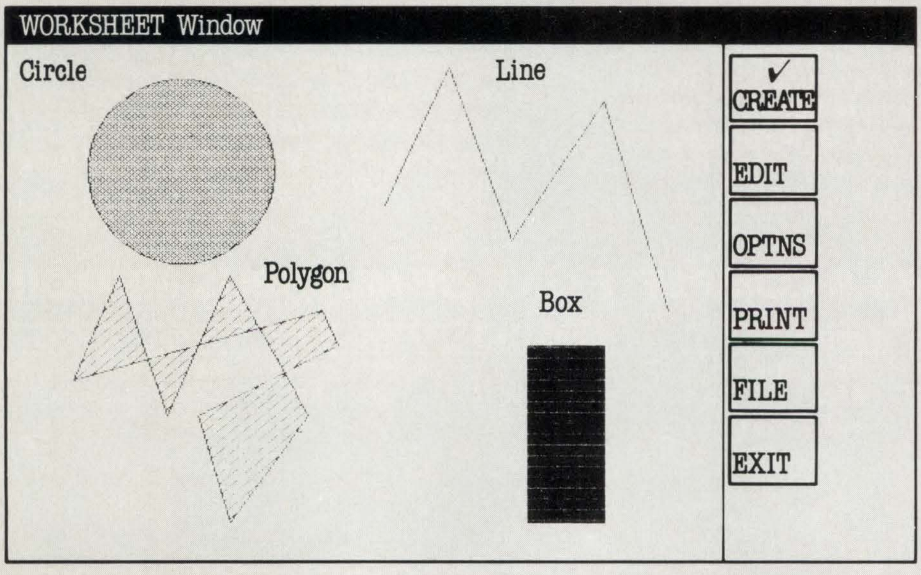

Fig 3 It is in the worksheet window that users create, edit, refine, and finalize, their graphics application program. The typical objects shown can be combined or deleted in an interactive process that takes only minutes to learn.

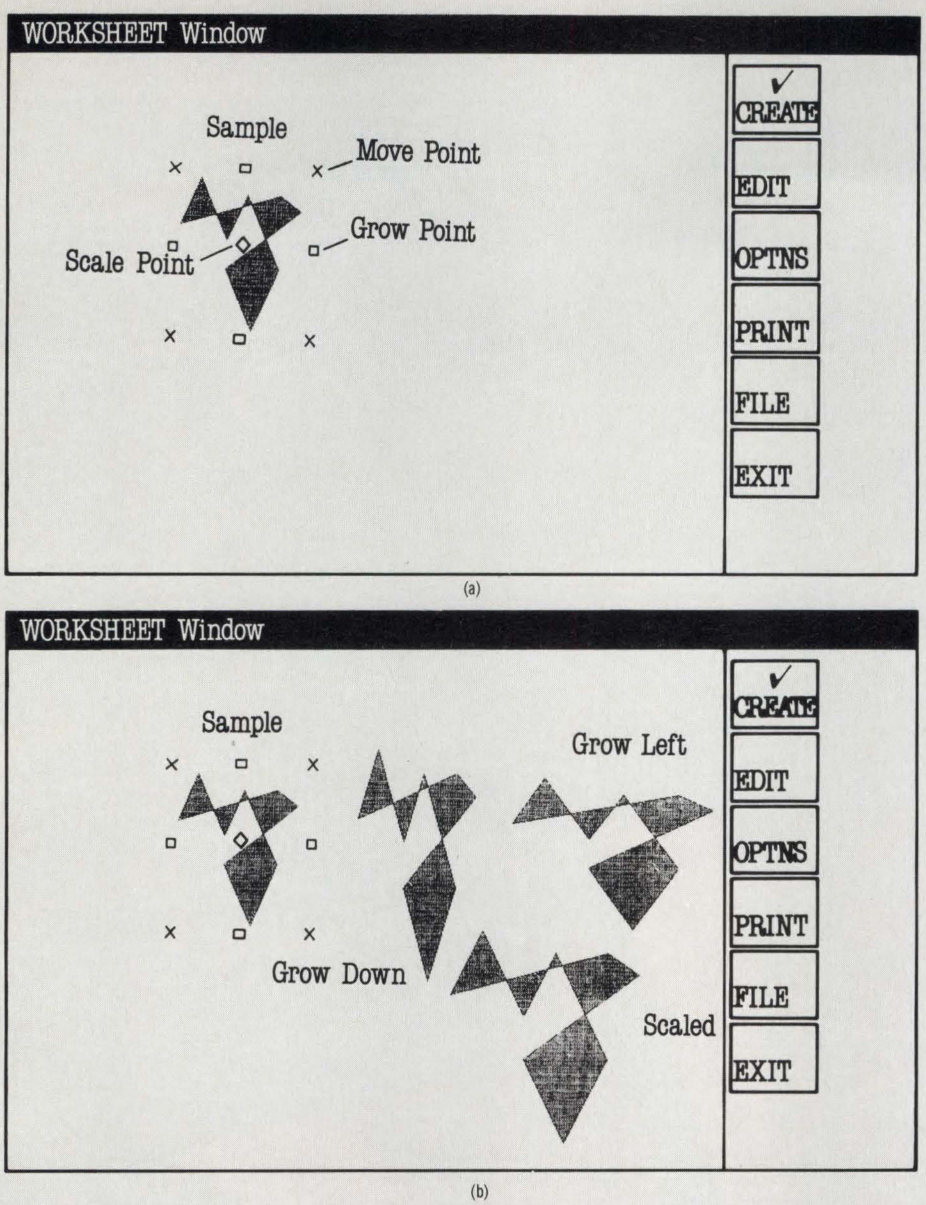

Fig 4 As shown, tag points allow the combining of move and scale operations in a worksheet window (a). When a diamond is selected (eg, with a mouse) the corresponding object is scaled (b). The "grow" feature is useful for sophisticated picture-making.

objects such as text, lines, boxes, circles, and polygons (Fig 3). All of these creation processes can be undone with the backspace key. Moreover, each of the worksheet objects can be deleted, moved, scaled, rotated, copied, grouped, or ungrouped. These functions, like the creation functions, can also be undone.

Move and scale were combined through the use of "tag" points [(Fig 4 (a)]. When an X is selected, the object can be moved. When a box is selected, the object is grown from that edge. When the diamond in the center is selected, an object is scaled [Fig 4 (b)]. In the option window, attributes of a selected object or the default object can be changed. The option window also controls a grid- and text-quality override mechanism.

For its part in the graphics software design process, the file window is the user interface for saving and selecting picture files to graphically edit. It provides an interface to the computer file system. With it, directories can be specified, and files can be previewed, loaded, saved, or deleted.

Finally, the help window is displayed whenever Sound Presentations is executed. It can also be accessed anytime during execution. And, based on the current context, the help window can provide help for whatever action is being performed. The help window models the other three windows by presenting the same menus and selection method.

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High 725 *Average 726* *Low 727*

State 7, 60 channel, 68000 emulation bus
Trace List
68000 Mnemonic
hex
SRC_ADDR:Mon 68K 1012 supr data
MAGIC_SQU+00001C FFFE supr program
MAGIC_SQU:E68000 - line
Pascal program to generate a magic square
matrix of numerical entries where the sum
column, or diagonal is constant. The
of entries on a side, specified by the
BEGIN { M_Square_Gen }
COL := SIZE/2;
MAGIC_SQU+00001E MOVE.W
STAT4:Mon 68K 0000 supr
MONITOR_CONTROL: 8000 supr
MAGIC_SQU+000020 0008 supr
MAGIC_SQU+000022 EXT.L D0
STATUS: Awaiting state command
_source on
display <LINE #> disassemb
Trace_List
State 7, 60 channel, 1750A emulation bus
Label: line # ADDRESS 1750A Mnemonic
Base: hex hex
Map: ADDR_MAP and symbols ADDR_MAP and
+011 12* aHANOIa+1109 LISP R2,1
+012 NUMBER_DISKS:aHANOIa 0014
+013 12 aHANOIa+110A STB
HANOIa:MILO - line
" Jovial routine for solution of the
L3: IF NN<>1;
+014 13* aHANOIa+110B
+015 NUMBER_MOVES:aHANOIa
+016 13 aHANOIa+110C CB
+017 13 aHANOIa+110D
+018 NUMBER_DISKS:aHANOIa
HANOIa:MILO
Begin NO(JP)=NN;
+019 14* aHANOIa+110E
STATUS: Awaiting state command - userid
_source on
display <LINE #> disassemb source
State 7, 60 channel, 68000
Trace List
68000 Mnemonic
hex
symbols
MAGIC_SQU+00003E MOVE.W 0008[A6],D1
MAGIC_SQU+000040 0008 user program read
MAGIC_SQU+000042 MULS.W D1,D1
MAGIC_SQU+000044 MOVE.W 2006[A5],D2
MAGIC_SQU+000046 2006 user program read
MAGIC_SQU:E68000 - line 40 thru 42
/* this procedure, written in -C- fills out the square matrix
ROW = 0; /* initialize the row pointer */
for (COUNT = 1; COUNT <=SIZE*SIZE; COUNT++) {
MAGIC_SQU+00004A BGT.W MAGIC_SQU+00009A
MAGIC_SQU+00004C 004E user program read
MAGIC_SQU+00004E MOVE.W 2002[A5],D3
MAGIC_SQU+000050 2002 user program read
STATUS: Awaiting state command - userid CONTROL
_source on
display <LINE #> disassemb source
show
execute

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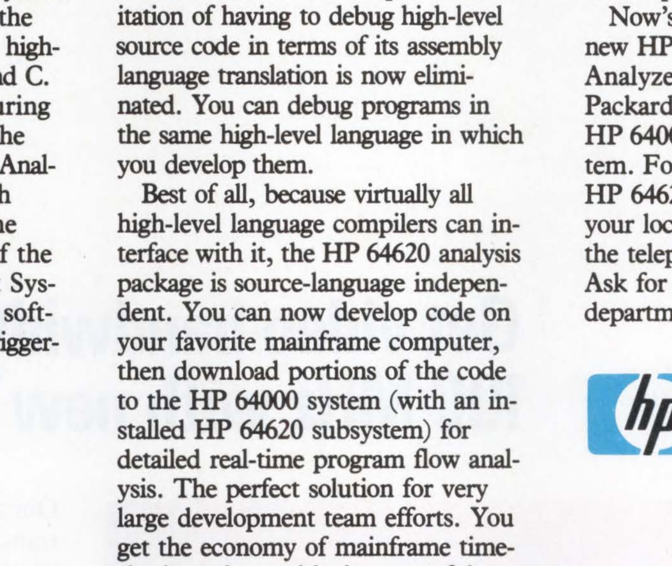

CIRCLE 88

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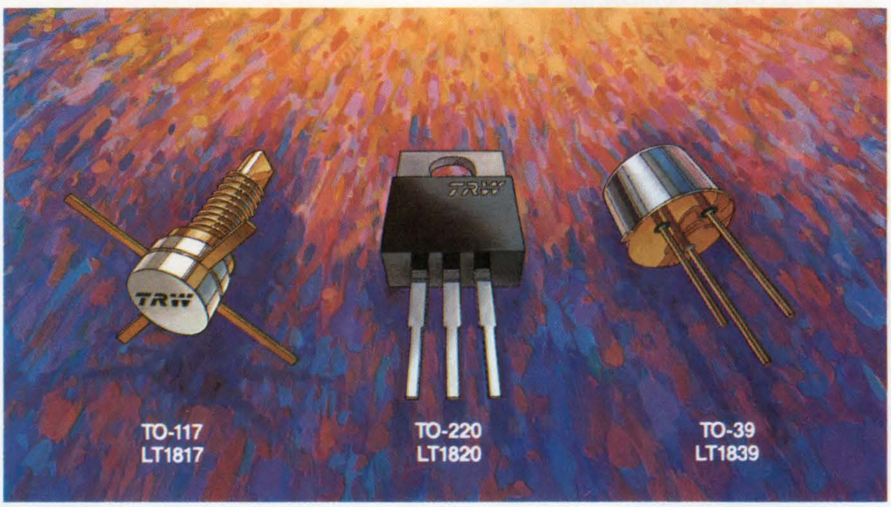

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CIRCLE 89

SPECIAL REPORT ON GRAPHICS TECHNOLOGY

VDI PROMISES GRAPHICS SOFTWARE PORTABILITY

Hardware manufacturers, software designers, and users benefit when application software using graphics is display-device independent.

by Fred Langhorst

The natural evolution of more sophisticated graphics hardware features and the need to migrate application software from one computer to another define the necessity for a full-function graphics interface standard. An ideal standard would provide an application program with access to future graphics devices without any limitations on resolution, the number of colors, performance, or the technology used in the display or hardcopy device. Such a graphics standard would also make object-code portability possible so that recompiling or relinking of application programs would not be required when the standard is combined with industry-standard operating systems. Unfortunately, the attributes of this standard are just now becoming available with today's microcomputer graphics and products such as the Digital Research Graphic System Extension, or GSX (see Panel, "Real-world microcomputer graphics").

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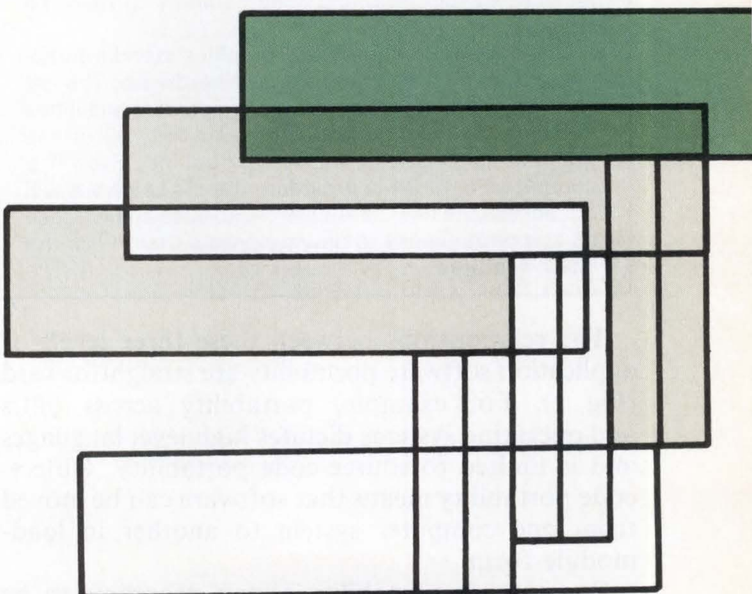

Having graphics application software that is computer-system independent is the goal of graphics standards. Indeed, it would benefit both the software developer and the consumer. To achieve application portability, the differences between computer systems that have to be accommodated include computer CPU instruction set, operating system interfaces, and graphics device I/O functions and protocols. In fact, three levels or degrees of computer independence can be defined as far as graphics standards are concerned. These are source-code portability, object-code portability, and communication protocol commonality.

Real-world microcomputer graphics

Until five years ago, the use of computer-generated graphics was limited primarily to engineering design and scientific applications where the high cost of hardware could be justified. The Apple II lowered the cost barrier substantially, and a number of games as well as entry-level commercial applications began using Apple's bit-mapped graphics.

Today, the Apple, the IBM PC, and other second-generation microcomputers have brought computer graphics to millions of desktops. However, the device dependence of most programs has restricted the availability of high quality software products employing graphics.

The widespread acceptance of the IBM PC, with its optional color graphics adapter, has established an interim bit-mapped display standard. Moreover, many PC-compatible computer manufacturers have designed their display hardware to be identical with IBM's hardware, and can run the many graphics applications that address the PC.

There is both good and bad news in this strategy. The good news is that the number of PC graphics applications is significant and users have a choice. The bad news is that hardware manufacturers are not free to differentiate their machines with higher resolution and more colors. Also, most of these applications are unable to drive high quality peripherals such as ink-jet printers, plotters, and slide cameras to their full capabilities, if at all.

Clearly, a hardware-based graphics standard cannot last, even if it is based on IBM hardware. The IBM PC will naturally have increased graphics capabilities at some future time and, at that point, all of the graphics applications will be left behind. Even if a compatibility mode is provided, the old software will not access the new hardware capabilities and will lose its competitiveness to new programs that utilize the latest features.

The relationships between these three levels of application software portability are straightforward (Fig 1). For example, portability across CPUs and operating systems dictates high level languages and is limited to source-code portability. Object-code portability means that software can be moved from one computer system to another in load-module form.

Source-code portability allows programs to be ported from one computer to another through the use of a common language compiler. For example, applications written in languages like Pascal, C, or Fortran can be recompiled and linked to operate on any computer systems that support compatible compilers. Source-code portability also provides software developers with a convenient means for moving their programs to new computers. However, retail distribution requires custom load modules (object code) for each computer system. Moreover, source code is seldom distributed to retail customers for two reasons. First, users typically do not have the tools or skills to build executable modules. Second, proprietary technology would be revealed.

Graphics standard activities over the last 10 years have almost exclusively focused on a means for accomplishing source-code portability. The challenge is to create a set of graphics primitives that is simple, consistent, and can be applied across a wide range of graphics devices.

In the mid-1970s, the Association for Computing Machinery/Special Interest Group on Computer Graphics (ACM/SIGGRAPH) took the initiative and formed a graphics standard planning committee. In 1979, it published the first comprehensive functional specification for a graphics programming interface called the Core graphics system or simply, Core. The Core system has been implemented by many universities and firms. However, it is not a national standard and it will not be. A stronger international standard, the Graphical Kernel System (GKS) has emerged.

The GKS was initially defined in Germany and was subsequently adopted by the European community as a draft International Standards Organization (ISO) standard. In late 1982, the U.S. representative to ISO accepted the draft GKS standard and it is now on its way to becoming both an American National Standards Institute (ANSI) and ISO standard. The first GKS standard contains a comprehensive set of two-dimensional graphics and text functions along with bindings to the Fortran language, and potentially others. A language binding defines subroutine names and argument syntax so that complete source-code portability is feasible. Future GKS standards are expected to include three-dimensional primitives that will be helpful in scientific and engineering applications.

Object-code portability

Software can be moved from one computer system to another in load-module form when compatible operating environments exist. This is the most comprehensive form of device independence and makes it possible for software to be distributed in a single version for a number of different computers. An identical CPU chip and operating system are, of course, required to accomplish object-code portability across a number of different computer systems. The first large-scale example of object-code portability in the microcomputer industry is the combination of CP/M and the 8080 or Z80 chips in thousands of personal computers, thus causing rapid growth of software products.

Graphics standards that accomplish object-code portability are still in the definition stage. ANSI's committee on graphics programming standards (X3H3) has a subcommittee pursuing a Virtual Device Interface (VDI) standard to accomplish the object-code portability chore. The VDI's functional ability is concise, yet comprehensive, and represents the best interface model for accomplishing object-code portability. Furthermore, the VDI functions

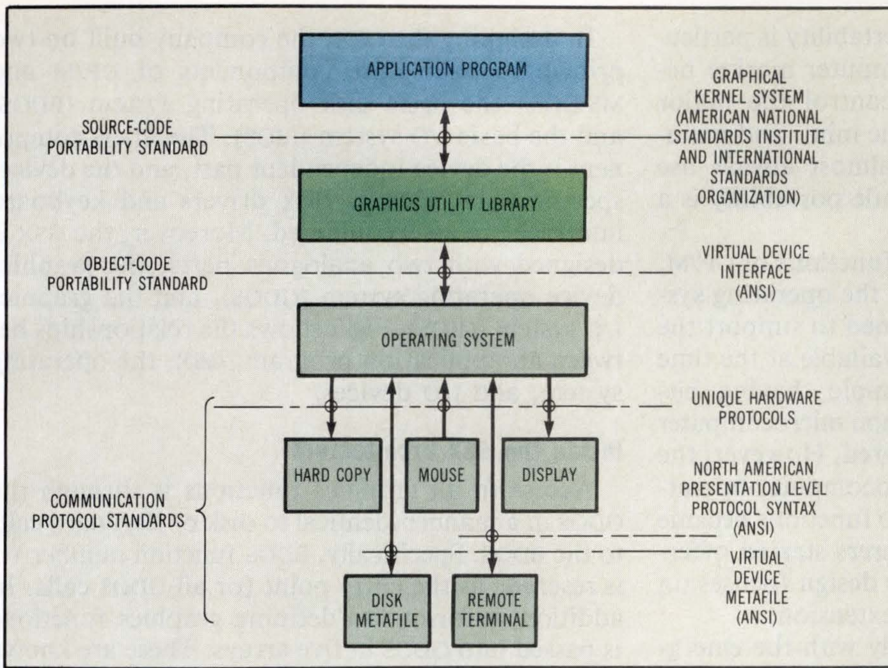

Fig 1 The graphics standards proposed by national and international standards-making bodies are hierarchically related. Each of them bears a specific relationship to the software portability problems that many firms are currently addressing.

represent a good set of capabilities to be incorporated at the operating system level where the application program object code-to-system interface exists.

Standards that define the serial flow of graphics information from a computer to an output device are communication protocols. There are a number of *de facto* communication protocols in the industry today as a result of the success of their respective graphics terminals. The most widely used is the Tektronix 4010 terminal protocol. Others include the IBM 3279 color terminal control interface and the Digital Equipment Corp Remote Graphics Interface Standard (Regis).

ANSI's X3L2 committee is active in standardizing a graphics protocol called the North American Presentation Level Protocol Syntax (NAPLPS). The NAPLPS protocol was designed for videotex services by the Canadian government's Telidon project during the 1970s. In 1981, AT&T endorsed the Telidon work and added some functional ability to arrive at the current NAPLPS.

The X3L2 standard is now in the final approval stage and should be published later this year as the U.S. videotex standard. This protocol standard will be widely used in host computer-to-remote terminal communication of graphics images. Indeed, home banking and video shopping services in North America will be NAPLPS based. This protocol may also find applicability in transmitting graphics over corporate computer networks and local networks.

A second ANSI standard, the Virtual Device Metafile (VDM), may also become significant as a communication protocol. The VDM is a project of the ANSI VDI committee. It is a protocol made up of the VDI functions encoded for disk storage or network transmission.

As summarized in Fig 1, the discussed standards form a graphics software hierarchy. Each of these standards will have an impact on different aspects of computer graphics and some will no doubt be more significant than others. According to Digital Research, for example, the VDI and NAPLPS will have the greatest impact on the microcomputer industry.

Microcomputer VDI

In light of the various developments in national and international standard activities, Digital Research has created its Graphic System Extension (GSX) product strategy. To provide a graphics standard with the aforementioned attributes in microcomputer graphics, the company (which began extending its system software line with graphics in 1982) has defined six goals. The first is to accomplish object-code portability for graphics application programs. Second, the company wants to support device-independent graphics I/O with its own operating systems and provide consistent interfaces for other operating systems such as PC-DOS, MS-DOS, and Unix. Third, the firm wants to follow the operating system model that made CP/M so successful and extend it to include function calls for graphics.

Two of the last three goals focus on supplying independent software vendors with a compact and high performance graphics interface that would offer them significant value, and providing device-independent access to graphics hardware from the company's line of high level language compilers. Finally, there is the goal to design graphics interfaces to comply with national and international standards where possible.

The first-listed objective is seen as the key to successful device-independent graphics in the microcomputer industry. As the basis for the rapid growth in the CP/M software market, object-code portability continues to be an important factor in the MS-DOS software market. Object-code portability is particularly significant in the microcomputer market because only a few CPU chips control the major industry share. In contrast, in the mini- and mainframe market, manufacturers almost always use proprietary CPUs and load-module portability is a moot point.

In considering the origin and functions of CP/M, Digital Research concluded that the operating system's calls (opcodes) were designed to support the hardware that was commonly available at the time of CP/M's invention. For example, having bit-mapped graphics was not a common microcomputer feature and no support was required. However, the need for the extension of a microcomputer operating system to include graphics I/O functions became obvious as computer manufacturers started offering graphics displays. The GSX's design focuses on fulfilling the need for such an extension.

The GSX is designed to comply with the emerging ANSI VDI because the VDI provides the minimal functionality required and because there are no other alternatives. For example, the GKS is a high level language interface that employs a floating point coordinate system and has too many functions to be a compact and efficient operating system interface. For its part, NAPLPS is a serial protocol that requires too much coding and decoding to be an efficient interface between a bit-mapped display and a CPU on the same bus.

In January 1983, the GSX for CP/M-80 was released as the first microcomputer industry VDI. According to the company, this GSX also represented the first time object-code portability for graphics applications had been accomplished on any size computer. A GSX for CP/M-86 was released in April, and in September, the first support for PC-DOS and MS-DOS was available. Future versions of the GSX will provide an identical graphics VDI on Unix.

In designing the GSX, the company built on two principal architecture components of CP/M and MS-DOS—the basic disk operating system (BDOS) and the basic I/O system (BIOS). The BDOS component is the device-independent part, and the device-specific parts such as disk drivers and keyboard interface are BIOS contained. Moreover, the GSX is designed with two analogous parts, the graphics device operating system (GDOS), and the graphics I/O system (GIOS). Fig 2 shows the relationships between an application program, GSX, the operating system, and I/O devices.

Inside the GSX architecture

Access to all graphics functions is through the GDOS in a manner identical to disk or keyboard calls to the BDOS. Specifically, BDOS function number 115 is reserved as the entry point for all GDOS calls. In addition, information defining graphics functions is passed into GDOS in five arrays. These are known as the graphics operation code, input parameter array, input points coordinate array, output parameter array, and output points coordinate array.

All graphics data points are passed to the GDOS in a normalized device coordinate (NDC) space extending from 0 to 32767 in both X and Y directions. The GDOS processes these points by first converting them into the device coordinate space of the target device and then passing the graphics commands on to the GIOS. This transformation is possible in the GDOS because the necessary information about the device is passed from the GIOS to the GDOS at device initialization. Such a design provides a VDI-compatible method of passing coordinate values. Moreover, the use of integers makes a high performance interface possible.

The GDOS is also responsible for the dynamic loading of GIOS device driver files. Each graphics device is associated with a workstation identifier number (WIN). When GDOS receives a request to

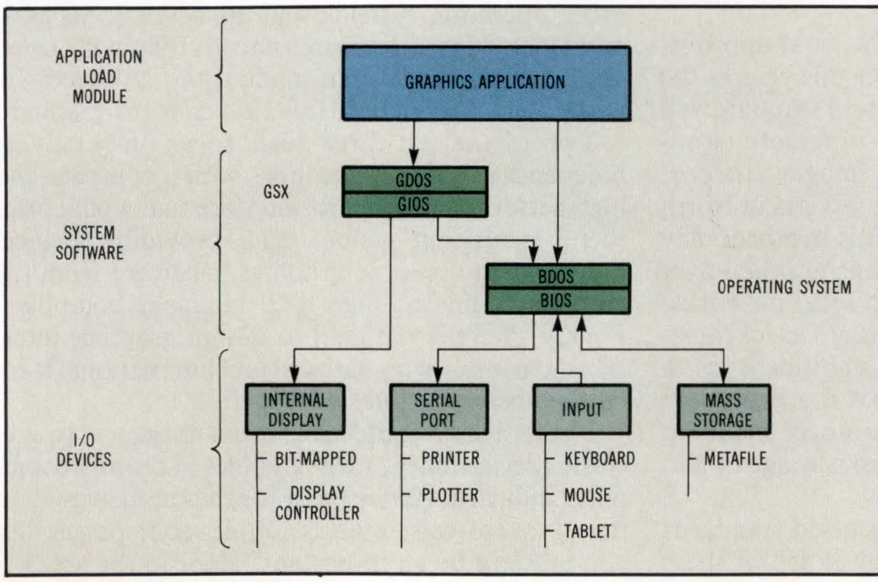

Fig 2 The GSX graphics software standard is a Virtual Device Interface (VDI) implementation that is closely tied to, and has parts analogous to, a microcomputer operating system. As shown, its two major parts are the graphics device operating system (GDOS) and graphics I/O system (GIOS).

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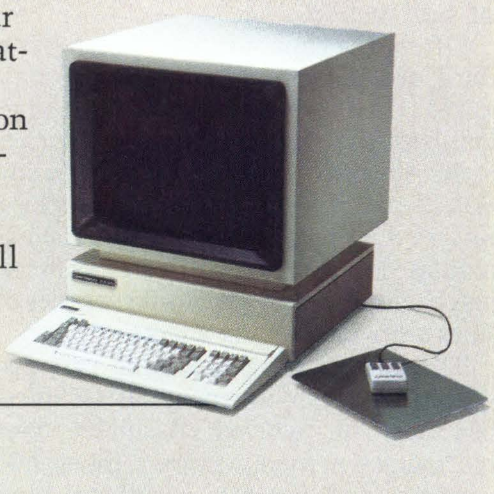

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CIRCLE 90

GSX Operation Codes

Opcode description

1	Open workstation: initialize a graphics device (load-driver routine if necessary)
2	Close workstation: stop graphics output to this workstation
3	Clear workstation: clear display device
4	Update workstation: display all pending graphics on workstation
5	Escape: enable special device-dependent operation (eg, cursor control)
6	Polyline: output a polyline
7	Polymarker: output markers
8	Text: output text starting at a specified position
9	Filled area: display and fill a polygon
10	Cell array: display a cell array
11	Generalized drawing primitive: display a generalized drawing primitive function
12	Set character height: set text size
13	Set character-up vector: set text direction
14	Set color representation: define the color associated with a color index
15	Set polyline line type: set line style for polylines
16	Set polyline-line width: set width of lines
17	Set polyline-color index: set color for polylines
18	Set polymarker type: set marker type for polymarkers
19	Set polymarker scale: set size for polymarkers
20	Set polymarker-color index: set color for polymarkers
21	Set text font: set device-dependent text styles
22	Set text-color index: set color of text
23	Set fill-interior style: set interior style for polygon fill
24	Set fill-style index: set fill style for polygons
25	Set fill-color index: set color for polygon fill
26	Inquire color representation: return color representation values of index
27	Inquire cell array: return definition of cell array
28	Input locator: return value of locator
29	Input valuator: return value of valuator
30	Input choice: return value of choice device
31	Input string: return character string
32	Set writing mode: set current writing mode (replace, overstrike, complement, erase)
33	Set input mode: set input mode (request or sample)

open a workstation, it determines which GIOS module corresponds to the WIN and loads that file into memory. The new GIOS is loaded into memory in the same location occupied by the previous driver to minimize memory requirements.

The logical association of WIN to a particular GIOS module is made in an assignment table. This is a text file stored on the system disk. New devices can be added or the correspondence between logical WIN and physical GIOS file can be altered simply by editing the assignment table file.

The GIOS component of the GSX contains the device-dependent code that translates from the VDI functions to the unique functions of a real graphics device. This VDI model makes all graphics devices appear identical to application programs using the GSX. The application programmer has 33 graphics operation codes available with the GSX. The Table lists these opcodes, some of which have a number of subfunctions.

Often, the capabilities specified by the VDI standard are not provided by a particular graphics device. In these cases, the device driver software emulates the required function. For example, line styles specified by the VDI include solid, dashed, dotted, and dashed/dotted. If a graphics device cannot produce these styles directly, their generation is emulated in the GIOS software. Thus, a dashed line can be produced by generating a series of short solid lines with intervening spaces.

The extension of operating systems to include graphics device-independent features provides benefits to all involved: consumers, computer original equipment manufacturers, independent software vendors, and graphics peripheral manufacturers. Consider, for example, the GSX features of object-code portability for graphics applications across computers with the same CPU chip, and source-code portability across many other computers. The benefits of these features include reduced cost of application program development, maintenance, and distribution (benefits independent software vendors), and a greater number of applications on the market (benefits users, original manufacturers, and graphics peripheral manufacturers).

The virtual graphics interface between application programs and graphics hardware is also beneficial. This interface layer makes the evolution of graphics hardware capabilities (resolution and color) possible, without requiring application program rewrites—a benefit for original manufacturers and independent software vendors. In addition, application programs can access many graphics peripherals with little or no effort. This is a great benefit for users, independent software vendors, and graphics peripheral manufacturers. Because system software suppliers and hardware manufacturers will develop the device drivers, independent software vendors will not have to do their own.

In the GSX, dynamic loading of device driver (GIOS) modules is part of the operating system and not part of the application. Thus, different devices can be selected at run time without requiring them to be always resident, thus benefiting users and independent software vendors. And, applications written today will be able to access new devices in the future and benefit from most, if not all, of the new device capabilities—advantageous to users, independent software vendors, and graphics peripheral manufacturers. Finally, there is the benefit of high performance and compact device drivers. This benefit allows good application software performance on computers that are commonly available, and is thus of great value to both users and independent software vendors.

Future directions

The GSX product family represents a first-generation VDI. The interface functions are designed to be consistent with the emerging ANSI VDI standard. However, in order for a standards committee to reach a consensus, the technology covered must not be controversial. Therefore, standards usually lag technology by several years and graphics are no exception.

Within the rapidly evolving computer industry, leading-edge technology is required to remain competitive and software products based solely on standards may not be competitive. Thus, a second-generation GSX is under development and will be available later this year. This GSX 2.0 product family will include many functions that go beyond the ANSI VDI. For one, there will be advanced text attributes and formatting functions such as superscripts and subscripts; underline, boldface, and italic; line spacing and margin definition; and font size, pitch, and style. There will also be bit-block transfers and raster operations from screen to screen, screen to RAM, and RAM to screen. Finally, GSX 2.0 will allow optional normalized device coordinate systems, which are possible because of the economies of scale in one vendor supplying the software to be used by many.

Over 70 microcomputer manufacturers have licensed the GSX and many independent software vendors are using it. Moreover, when IBM introduces its next-generation graphics card for the PC, the benefits of the GSX will become even more apparent than they are today. Digital Research will be developing GIOS modules for new IBM hardware as well as other manufacturers' hardware. Independent software vendors who have built their products on a GSX will be able to quickly port to the new hardware. In contrast, independent software vendors who have not built on a GSX may find that months of conversion effort are required and multiple product versions will need to be maintained.

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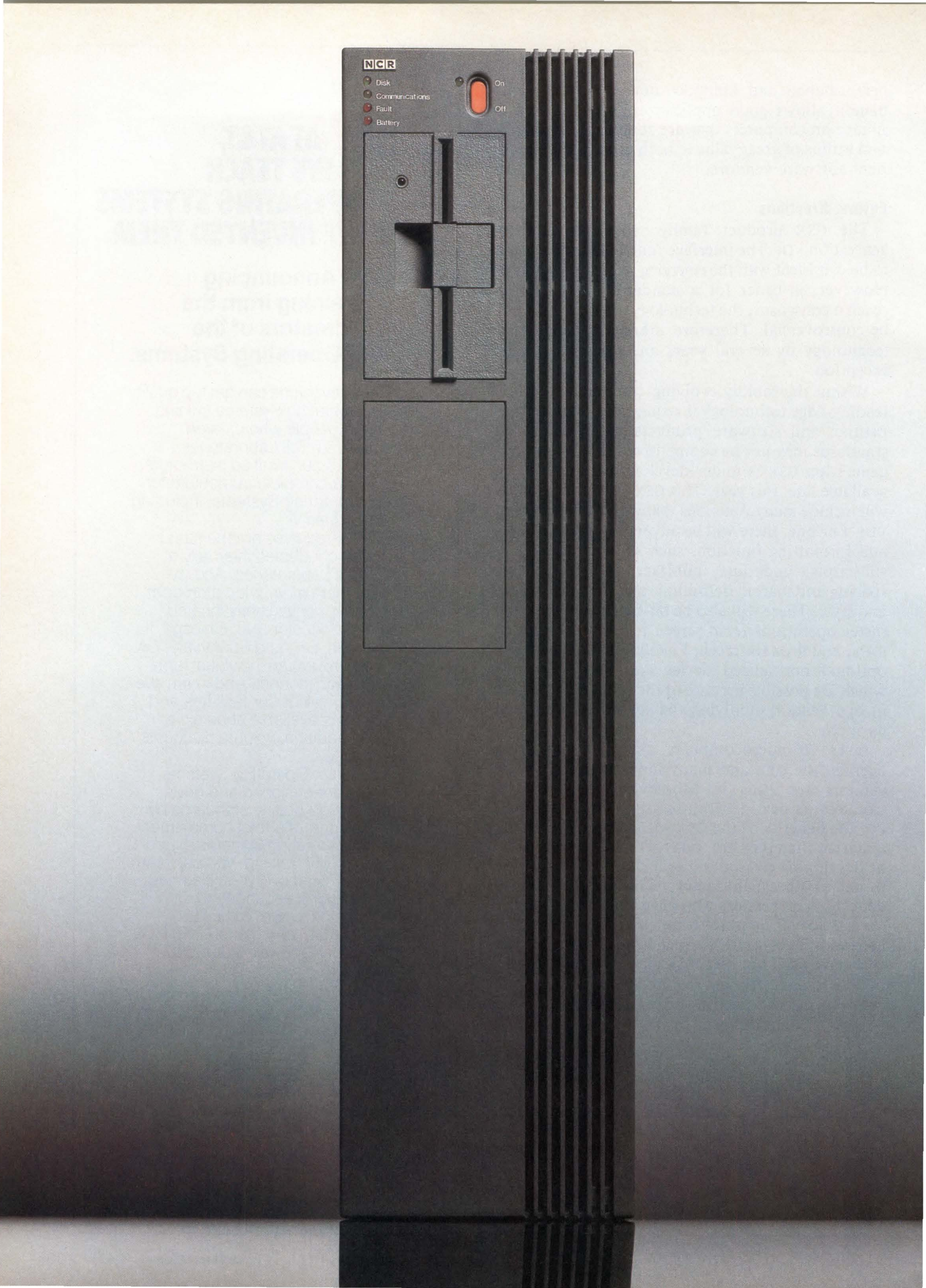
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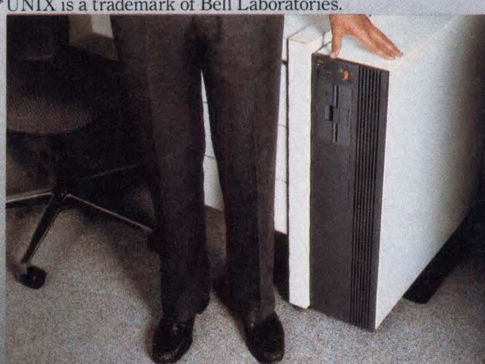

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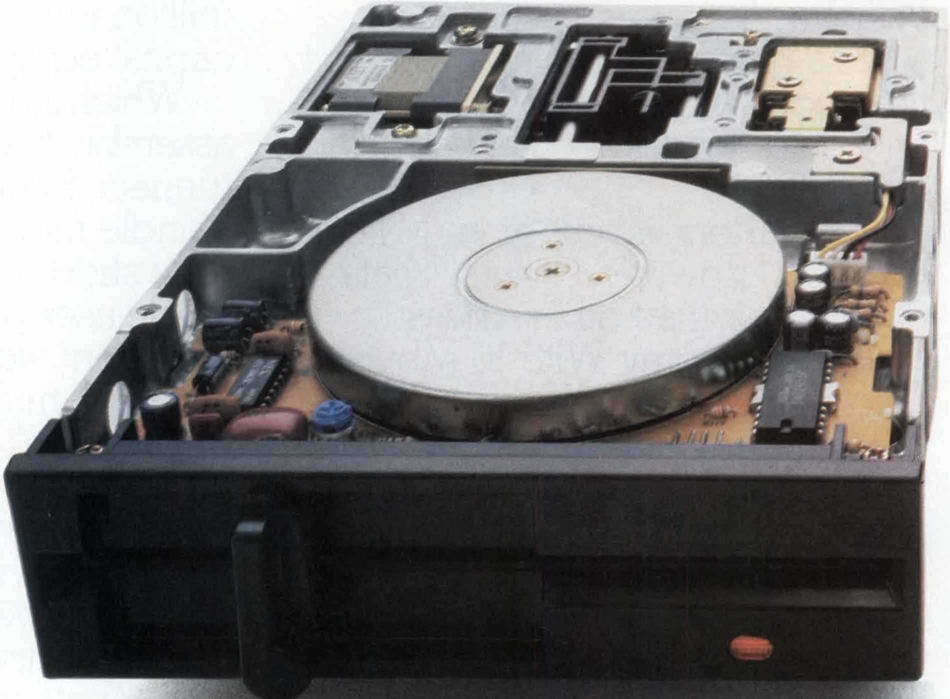

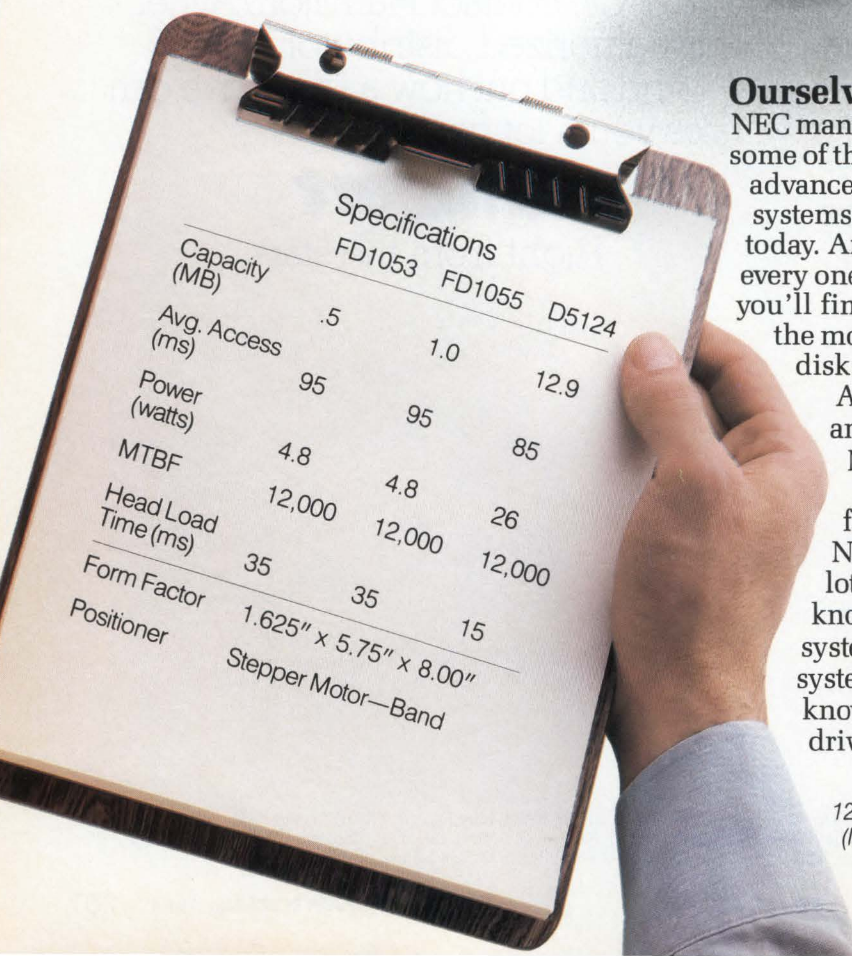

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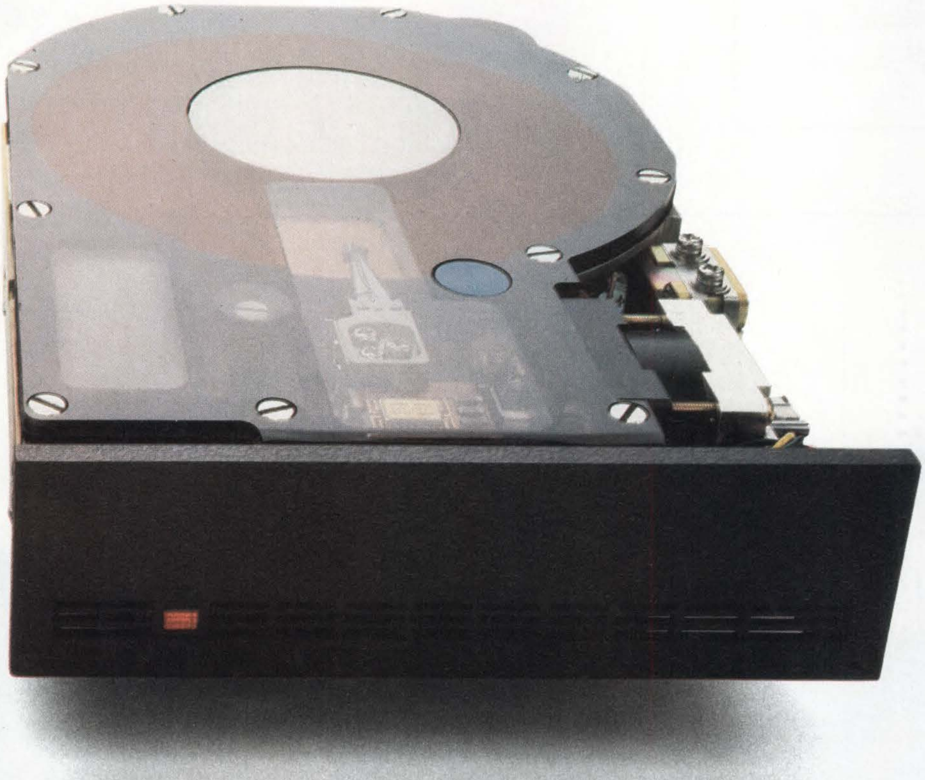

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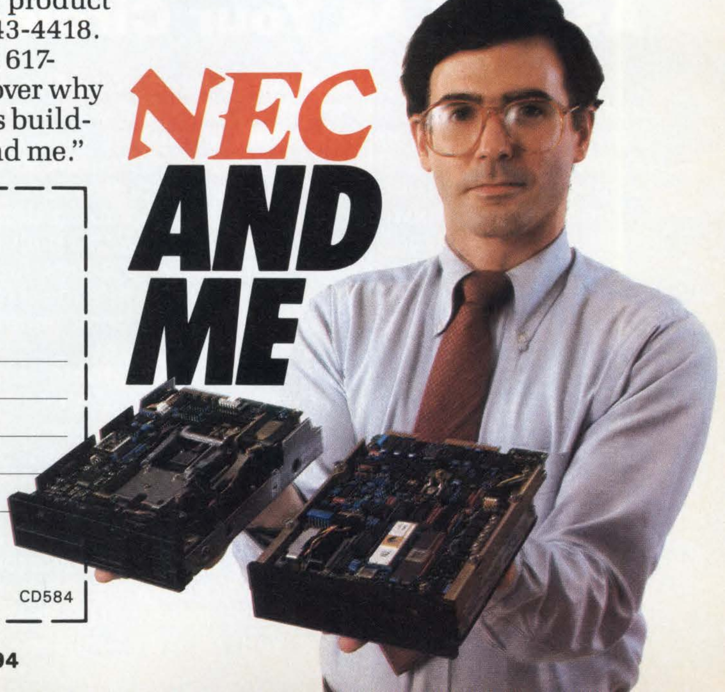

CIRCLE 94

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CIRCLE 95

SPECIAL REPORT ON GRAPHICS TECHNOLOGY

IS GKS POWERFUL ENOUGH FOR THE APPLICATION?

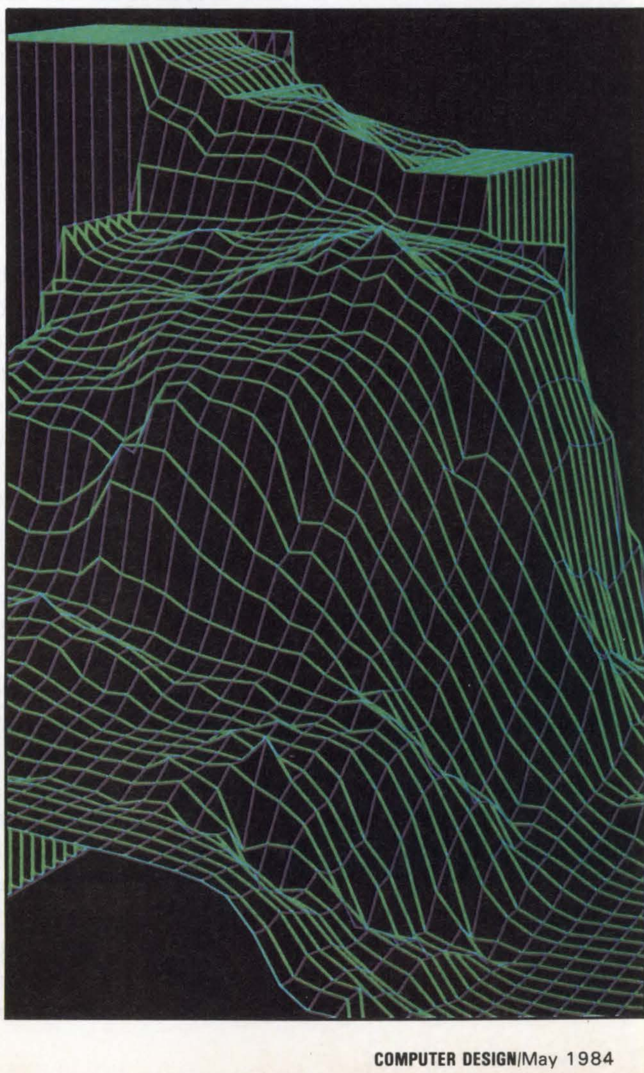
For a minimal standard or proprietary product, making the graphics software choice depends on the application.

by Thomas Wright

The emergence of standards in the computer graphics industry provides the technically educated computer system integrator or designer with a challenge. While some will blindly adhere to all available standards regardless of application, others will configure computer graphics systems that address the real needs of the users being represented. Graphics vendors can lessen the problems by helping educate the buyer in forming the best combination of standards and proprietary products.

As standards have merged in graphics software, Integrated Software Systems Corp (ISSCO) has been one company faced with this challenge. For over a dozen years, the company has been marketing its graphics software subroutine library known as DISSPLA. This system is, in effect, a *de facto* standard, with over 1200 active installations. Yet, there is now the question of how it can be combined with the new standards under development.

At first glance, the Graphical Kernel System (GKS), which will achieve American national standard status within months, seems to address the same graphics needs as DISSPLA. ISSCO is prepared for the



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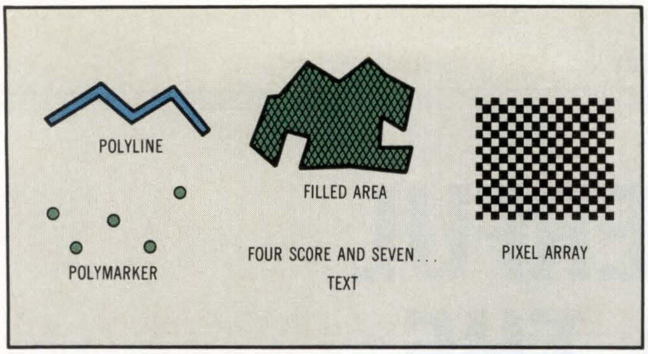

Fig 1 The primitives or basic drawing functions in the Graphical Kernel System (GKS) standard are limited to the five capabilities shown. As the GKS is designed, these may be called in a program through standard Fortran language binding.

GKS's emergence and sees a healthy relationship between the GKS and DISSPLA that will make both useful to the computer graphics community.

The two graphics software routine packages form a pair of complementary products. They allow an application programmer to choose between a small, fast, lean system (the GKS) that may sacrifice programmer productivity to attain performance and portability, and a large, powerful system with high end graphical quality and flexibility. In addition, both the GKS and DISSPLA are useful tools for the graphics application programmer. As such, a graphics system integrator or designer should carefully review the capabilities and advantages of each when configuring a system. It will often be desirable to use these and other systems to support the diverse applications under the heading of computer graphics.

DISSPLA versus GKS

The first hurdle a graphics system integrator faces is properly applying—or not applying—standards to the various subsystems within a graphics software configuration. Conforming to the GKS standard in a turnkey, end-user system achieves none of the benefits of software standards, such as program portability, programmer portability, or product synergism. This is because the vendor writes the application, and access to the underlying graphics system is unavailable to the user.

In the case of a software library supporting graphics application programming, the GKS quite properly rates careful attention. The GKS is a system specifically created to support graphics application programming. It is being published with a Fortran language binding that lists the data types and calling sequences for the GKS functions. Thus, programs and programmers should move with relative ease among different implementations. Such ease of movement means that multiple applications can be built on a common base to create a graphics system of greater value than the sum of its parts. But, the GKS is a low end system, while DISSPLA has held its position as a high end graphics software library for over a decade because it contains many useful capabilities not found in the GKS.

Some of the functions not included in GKS may be surprising. The system is without axis generation, nonlinear transformation support (eg, logarithmic scaling, mapping, and data coordinates), or interpolation. Also, the GKS is strictly a two-dimensional system. Other omissions may be more expected in a minimal system. There is no pie chart or bar chart generation utility. Moveover, the GKS is without blanked-out area capabilities, map generation, contouring, shaded fonts, or user-supplied transformations. Yet, with the addition of ISSCO's Dynamics graphics software to DISSPLA, both the GKS and DISSPLA will gain segmentation and contemporary graphics input mechanisms.

The differences between DISSPLA and the GKS are clear. The former is a larger, more robust system with greater functionality and resulting higher programmer productivity. The latter is a more linear system for minimal environments and highly dynamic applications. Here, lower programmer productivity is acceptable because of other graphics system requirements. Since ISSCO users will have the choice of which system to use, its GKS (offered as a DISSPLA option) is free of extensions that could impact performance, both in size and speed. Potential purchasers of GKS systems should carefully examine any extensions to the standard and see how these affect the graphics system and its needs.

Inside the GKS

A more detailed description of GKS functions will help potential users assess its capabilities. The output capabilities of the GKS are limited to primitives: polyline, text, filled areas, polymarker, and pixel arrays (Fig 1). There is also the concept of generalized drawing primitives in the GKS but these primitives cannot be depended upon from one installation to another because they are not fully specified. This severely limits their utility.

A polyline is a set of coordinates to be linked with straight line segments. User-selectable attributes of the straight line segments include color index, width, and dash-pattern. In the Fortran binding of the GKS, a polyline subroutine is called GPL. (All GKS

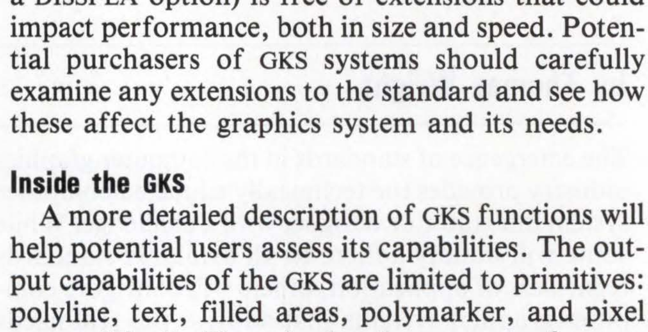

Fig 2 ISSCO offers not only the standard GKS graphics software but also its proprietary DISSPLA graphics software. DISSPLA allows the equivalent of graphics software macros to substitute for thousands of lines of GKS code.

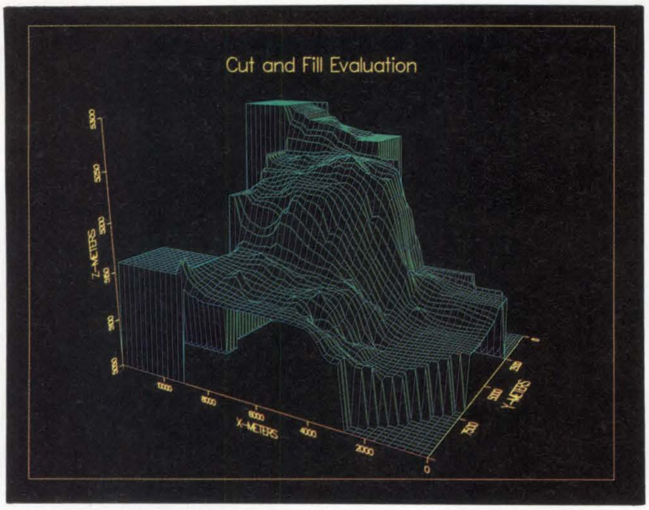

Fig 3 It is difficult and time consuming (if even possible) to write the thousands of lines of code the GKS or its variations require to produce a three-dimensional figure like the drawing shown. For programmer productivity, DISSPLA graphics macros reduce the effort.

routines start with the letter G at the time when their Fortran binding is named.)

As might be expected, text (called GTX) is a string of characters to be drawn. The many attributes of text include color index, height, and orientation. For its part, a filled area is a set of coordinates enclosing an area to be colored-in with a solid or cross-hatched pattern. Attributes for filled areas are color index and pattern. This routine is known as GFA.

A polymarker is a set of coordinates, each to be marked with a symbol such as a dot or a plus. The attributes are color index, marker type, and marker size. The routine is known as GPM. Finally, a pixel array is a rectangular (before transformation) area to be filled-in with a specified, repeated pattern of different colors. Its routine name is GCA.

Comparing these, the lone GKS graphics-producing routines, with just three of the software routines in DISSPLA, shows why DISSPLA represents a substantial increase in programmer productivity. For one, SHDPIE (Fig 2), produces a shaded pie chart with complete external or internal annotation. External annotation can be justified to the pie or to an external imaginary rectangle.

With SHDPIE, collisions that might result from small pie slices are automatically avoided. Moreover, internal annotation is automatically switched to external when the slice is too small to hold the annotation. Finally, slices are solidly shaded in different colors or cross-hatched, and individual slices can be exploded or slightly offset from the pie center for emphasis.

SURMAT is another good example of DISSPLA capabilities. It draws a wire-mesh styled representation of a two-dimensional data array, treating the data values as heights. Lines that would be invisible if this representation were a real object are automatically suppressed. Annotated axes corresponding to the three space coordinate directions can easily be added with a SURMAT software system call.

As the last example, consider BLPOLY. It protects a polygonal area from further drawing. This routine can be used for generating effects such as drop-shadows for shaded-in characters, and removing hidden lines in three-dimensional figures. It also allows cut-and-paste effects that give the appearance of one piece of graphics having been pasted over another.

Some DISSPLA functionality can be duplicated in the GKS; some cannot. To duplicate any of the three described functions would take considerable effort—perhaps many thousands of lines of code. Clearly, such reinventing of the wheel is not cost effective for many applications. As mentioned, DISSPLA has scores of functions like SHDPIE, SURMAT, and BLPOLY; whose duplication would also involve a major effort.

Other considerations

To make matters worse, implementing DISSPLA functions on top of the GKS dilutes some of the advantages of a standard. Nonlinear scaling is a good example of this additional problem. Often, an application uses data in a form that the GKS cannot directly handle. Thus, the scientist can have data with such a large range that it requires logarithmic scaling. Or, the business application programmer can have data with a date component.

If a software utility is added on top of the GKS to handle these transformations for drawing lines, for example, then programmers will be writing programs that invoke the utilities rather than the GKS function GPL. The portability and understandability of these programs are thereby greatly reduced. On the other hand, in DISSPLA, the subroutine CURVE is used to draw a polyline regardless of the transformation in effect. An application program remains readable to anyone familiar with DISSPLA.

Both the GKS and DISSPLA will have a place in the market. The GKS is a long-needed step toward graphics standards for the application programmer, and it will grow more powerful as time passes. But, the GKS is a two-dimensional system. Many application programmers must produce sophisticated graphics displays (Fig 3) requiring, for example, three dimensions in either Cartesian or spherical coordinates. Thus, high end, proprietary packages such as DISSPLA will remain the graphics systems of choice for the foreseeable future.

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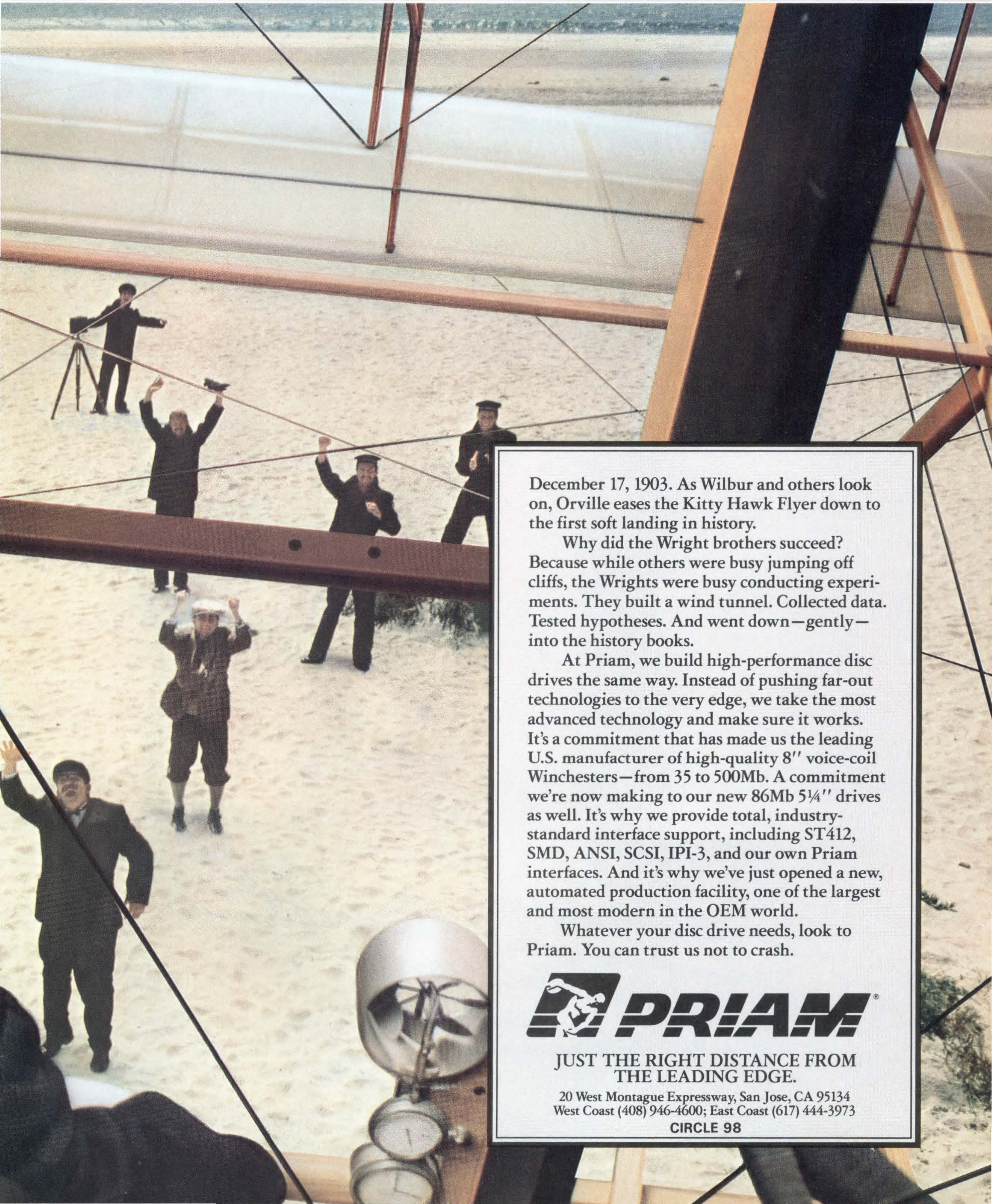

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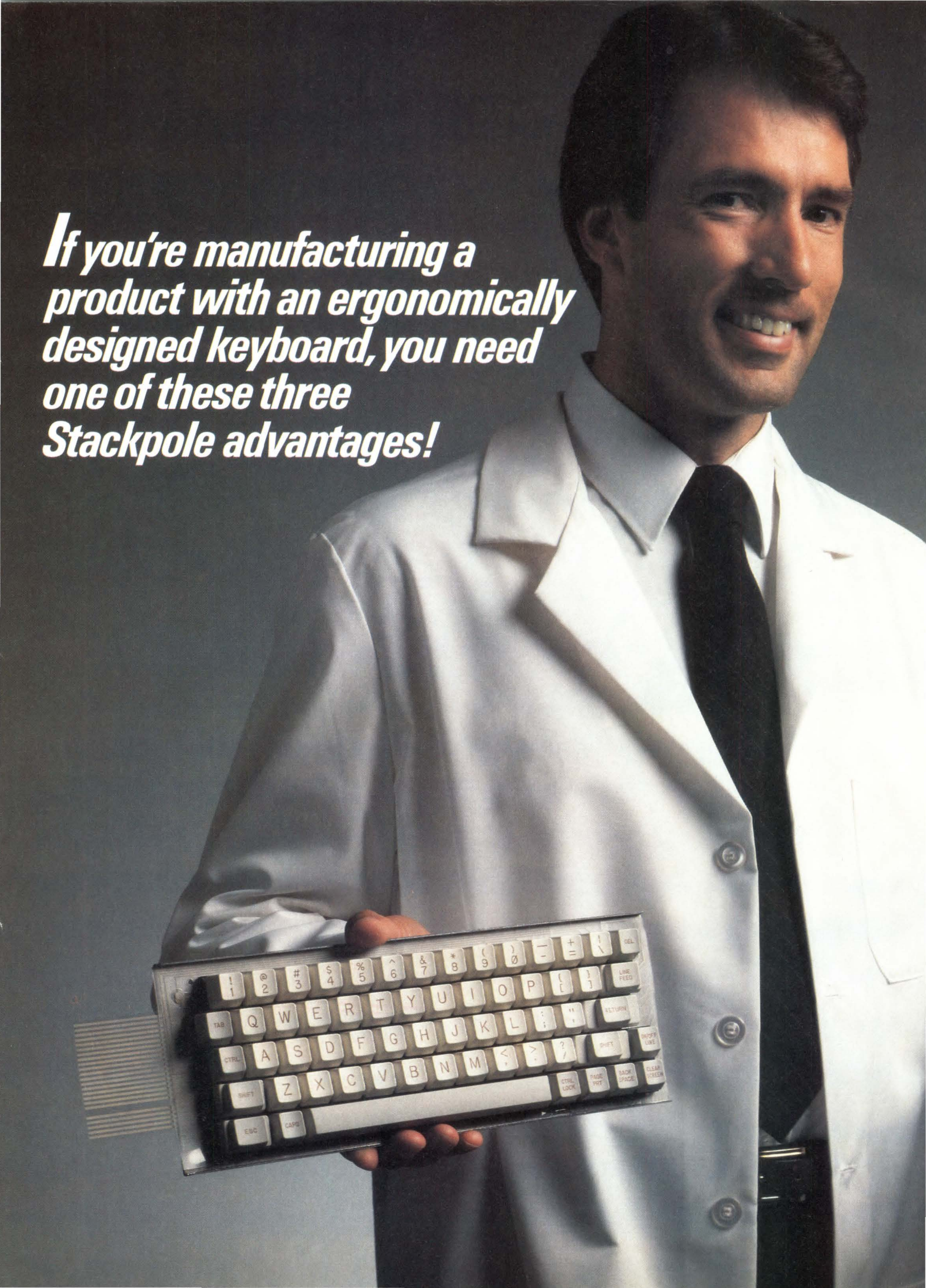
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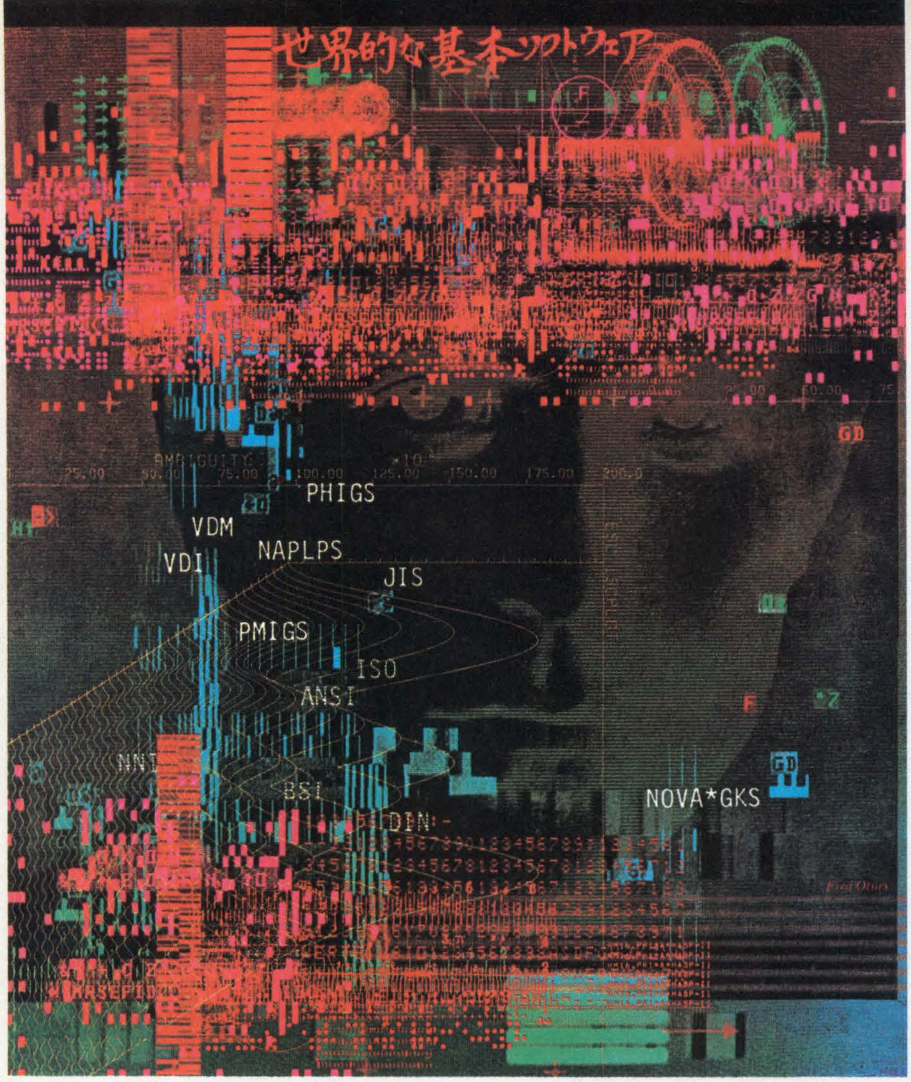

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CIRCLE 100

PIPELINE MODEL PROMOTES EXTENSIBLE DISPLAY SYSTEM

An open system architecture allows computer system integrators to upgrade as new graphics software and hardware debut.

by Jack Huisman

Recent trends in the design of interactive graphics systems for computer aided design, computer aided manufacturing, and computer aided engineering applications have placed new demands on display subsystems. These demands are, in turn, changing the way such subsystems are designed. The display subsystem can no longer be viewed as merely an electronic pen plotter that accepts and displays precomputed vectors with the host computer carrying the major burden of the interactive graphics task. Instead, high performance interactive graphics subsystem design requires that the display subsystem be viewed as an integral, coprocessing part of the entire graphics system. In fact, the display subsystem must be viewed as sharing the interactive task with the host computer, in what amounts to a distributed processing system.

As an example, one group of raster display systems was designed with this system requirement in mind. Using multiple buses, multiple processors, and an open architecture, Lexidata's Lex 90 family has its own proprietary, high end graphics that conform only conceptually to the various proposed national and international graphics standards. On the other hand, the family now fits the needs of high performance interactive graphics systems, from boards to terminals to workstations, in a cost-effective manner. And, because of its modular design, it can perform the same chores for tomorrow's graphics systems.

Jack Huisman is manager of product marketing at Lexidata Corp, 755 Middlesex Tpk, Billerica, MA 01865. He holds a BA in mathematics from Dartmouth College, and an MBA from Amos Tuck School of Business Administration at Dartmouth.

Surveying the system models

The graphics display pipeline (GDP) model of an interactive graphics system is at the heart of this family design (Fig 1). The GDP is a functional model of how all interactive graphics systems are built (from a conceptual viewpoint). It is a series of data representations and processes arranged in a pipeline, beginning with the user's application model and ending with the displayed graphics image.

The application model is a data base containing both graphical and nongraphical object data in a structure suitable for the user's application system. Besides containing a graphical description of the user's design, the application model supports nongraphical information such as part numbers, material properties, performance characteristics, and other data relating to the entire design, engineering, and manufacturing task.

The display file compiler maps the application model into a hierarchical graphics representation known as the structured display file. For its part, the structured display file is a world coordinate-

What's new in graphics hardware

In recent years, all the major hardware components of an interactive graphics system have undergone significant technological changes. For example, disk drives have increased in performance and capacity, and at the same time, have decreased in price.

Semiconductor RAM has been one of the strongest forces in graphics system design. It too has increased performance and lowered prices. This, in turn, has led to the almost universal use of high level languages. RAM developments have also given rise to the higher quality and performance of the raster scan graphics systems that are replacing older technologies such as the direct-view storage tube.

Clearly, single-chip microprocessors and related VLSI technologies are the other major hardware forces in graphics system design. Not only do they replace minicomputers at a fraction of the cost, they make it possible to assign separate processors to separate processes in the graphics pipeline.

based graphical object description of the object being designed. It builds a graphical description of an object through reference to proprietary graphics primitives and sub-objects that, in turn, reference other objects and primitives.

The structured display file is processed by the display processing unit to build a linear display file. In doing so, the display processing unit carries out the expansion of the hierarchical structured display file, and any geometric transformations of coordinates to account for scaling, rotation, translation, clipping, and perspective transformations. The output of this operation is a linear display file containing primitives in display-device coordinates. As expected, these primitives include vectors, arcs, circles, and polygons.

Also included are display attributes such as color and texture. The display controller processes the linear display file sequentially to produce a displayed image. This image is stored as a pixel array in a frame buffer that refreshes the raster display system's CRT.

Adapting to specific system needs

In a typical interactive graphics display system, not all of the data representations just discussed for the GDP need to exist in explicit terms. For example, the application model and the structured display file may be identical in a simple system. Moreover, the linear display file may only be calculated and processed for display without being saved as an intermediate data base. Generally however, each of the data bases is at least calculated in a typical computer aided design (CAD), computer aided manufacturing (CAM), or computer aided engineering (CAE) system.

Most past, and many present day, systems have been designed so that not every process in the GDP is executed in a separate processor. For example, in a system that has a simple display device that accepts only vector data, the display file compiler, the display processing unit, and much of the function of the display controller, are all processes handled by a single processor—the host computer. This burden on the host computer severely limits its performance, the number of terminals that the host can support, or both.

Recent progress in the performance of interactive graphics systems (regardless of the manufacturer) has been achieved, not only by increasing the performance of hardware in the GDP, but by explicitly allocating a processor to each process in the pipeline (and even multiple processors to a single process). All other hardware and software being equal, the more processors per process and per workstation, the higher the system performance will be.

The GDP model provides another valuable insight into the design of an interactive graphics system. The model makes it clear that total system performance is limited by the lowest capacity pipeline element. In fact, optimum system design requires that the performance of pipeline processors be matched. Thus, if one pipeline element has significantly higher performance than the others, it probably costs more than it needs to for the overall level of system performance. Determining the narrowest pipe—the system bottleneck—allows the system designer to improve performance by moving part of that element's burden to another pipeline part. This design procedure improves that element's performance by splitting a subsystem into two or more processors and processes.

This family of display and graphics systems is designed with the graphics pipeline in mind. System designers can choose from single or multiple processors to build a system with a performance level matching individual application requirements. Moreover, designers can ensure that total system cost is consistent with performance. As needs

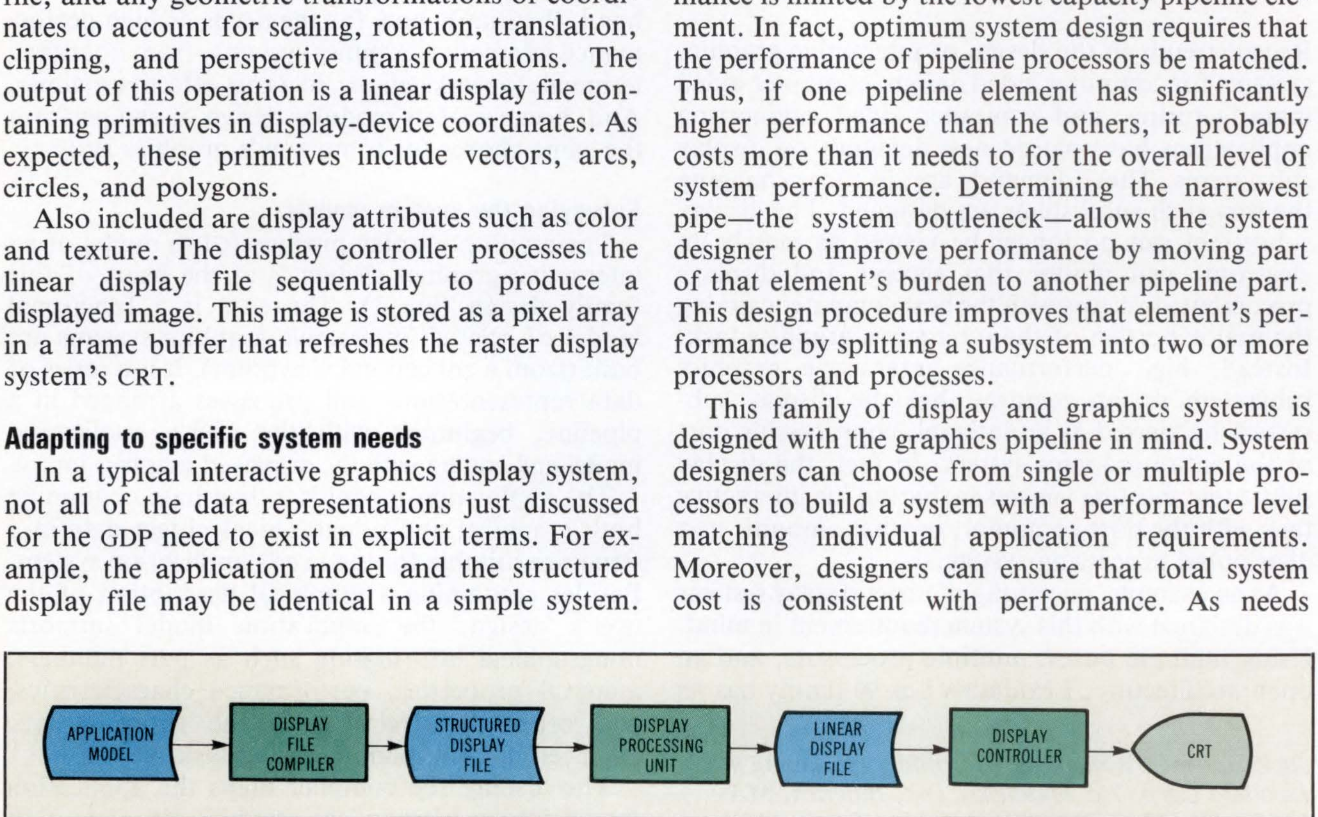

Fig 1 An interactive graphics system can be modeled by means of the GDP. All the parts of this linear, conceptual model need not be implemented in separate modules, but the functionality is usually present somewhere.

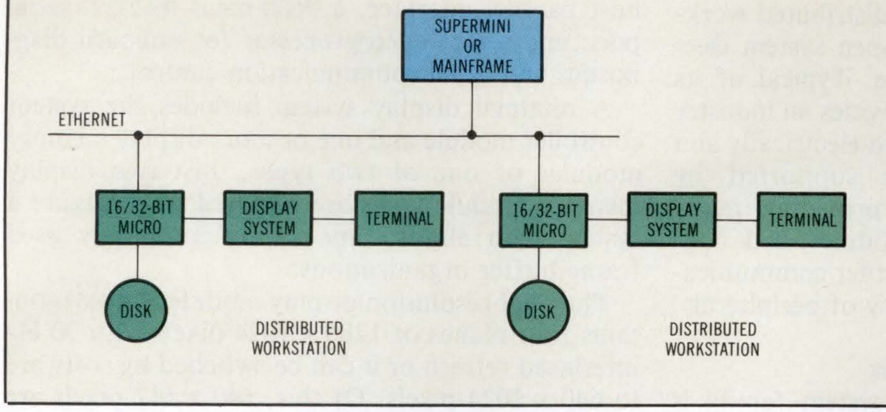

Fig 2 An interactive graphics system may consist of a network of workstations, with a host computer providing archiving, batch operations, and access to expensive, seldom-used peripherals.

change, upward migration paths within the family of display systems allow compatible products upgrade with controlled software costs since all family members share a software architectural standard.

The pace of technological change as it affects graphics system design has never been quicker. In the past, the graphics industry has relied on technology developed for the computer industry. This is changing so that new technology, such as VLSI display controllers and memory organized for display systems, is aimed at the needs of graphics system designers. Future industry success will be highly dependent on architectures that can take advantage of new technology (Panel, "What's new in graphics hardware").

Plotting the technological trend

The result of all this technological change has been the unmistakable trend toward standalone, multi-function distributed workstations that are loosely linked to each other in a network or to a central host computer (Fig 2). The standalone workstation depends on the network or central host for batch-processed application software, archival database access, and access to expensive, seldom-used peripherals such as plotters.

All of the interactive graphic applications, however, are supported locally in the individual workstation. The advantages of a distributed architecture include lower initial cost, lower incremental cost to add a workstation, reliability, performance, and maintainability.

Typical of this generation of workstations are the recent emergence and rapid growth of the CAD/CAM/CAE workstations from new, startup enterprises. Unburdened by past product history, designers at these firms have used the best available architecture that fits the available technology—the distributed, intelligent, standalone workstation.

The established interactive graphics system vendors have been slower to adapt this new technology because of their existing product investment (especially in software). While many of the older systems still consist of a shared central computer with relatively unintelligent terminals or workstations, system designers are developing architectures for use with more price- and performance-effective technology.

Such movement generally results in a partially distributed architecture with the display system in the workstation off-loading some of the host computer's load (Fig 3). Again, the trend is clear—more processors per GDP and per workstation. In time, nearly all interactive graphics systems for CAD, CAM, and CAE will probably be totally host dependent for all but the centralized functions. This evolution will be accelerated with the widespread use of new 32-bit microprocessors that support the same type of virtual memory operating system and software available on today's superminicomputers.

The design of the Lex 90 product family encompasses both the needs of the newer distributed graphics system architectures and the older, centralized, host-based designs. For example, rack-mounted models within the user's host computer satisfy the needs of the central host architecture. These models can be configured to provide only a simple display controller function to the GDP. They can also be upgraded to provide more processing within the display system to off-load the host computer and provide an evolutionary step toward a distributed workstation architecture.

For a distributed processing workstation architecture, models are available both in rackmount and floor-standing models, depending on the system

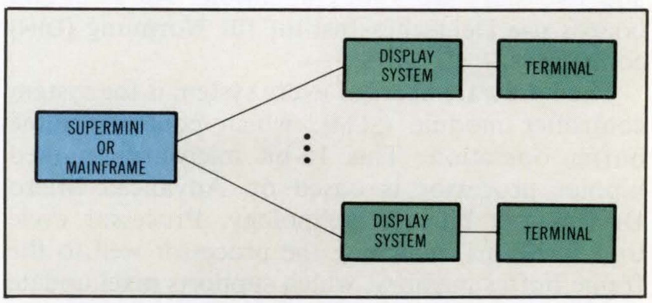

Fig 3 Open system architecture supports host-controlled graphics, distributed network graphics, or a partially distributed system architecture in which major portions of the graphics display pipeline are off-loaded from the host computer.

designer's needs. Building a fully distributed workstation is aided by the family's open system electrical and mechanical architecture. Typical of its open system design, the family provides an industry standard 32-bit computer bus, both electrically and mechanically. This VMEbus is supported by numerous third-party vendors, providing many choices for selecting computer modules, disk controllers, local network adapters, other communication controllers, and a wide variety of peripherals.

Providing hardware for many needs

The hardware in the display system family is designed around a series of modules for each part of the GDP. By design, a limited set of modules can be configured to meet the needs of a wide variety of system design situations. These modules accommodate variations in processing needs; different display resolutions and numbers of colors; dynamic displays; and special needs for the display of three-dimensional shaded surfaces. The limited number of modules simplifies inventory, spares for maintenance, and system upgrade as requirements change.

All printed circuit cards are based on Eurocard form-factor standards. These include the VME standard as well as the larger sizes more suited to the needs of a high performance, raster graphics display controller. System performance is enhanced through the use of multiple buses. For example, multiple buses reduce bus contention and allow the graphics display controller to have its own high speed synchronous bus.

Technological change has resulted in a trend toward standalone multifunction distributed workstations.

Actual internal package design depends on the application. For example, a typical system might be supplied in a six-slot chassis wherein four slots are reserved for the display processor's private bus and two slots are VME compatible. All slots and boards use Deutsches Institut für Normung (DIN) connectors.

The hardware heart of every system is the system controller module (SCM), which controls frame buffer operation. This 16-bit microprogrammed bipolar processor is based on Advanced Micro Devices 2901 bit-slice technology. Processor cycle time is 175 ns, matching the processor well to the frame buffer memory, which supports pixel update rates of 375 to 750 ns with an average update time of 600 ns. The SCM supports 8 Kwords of 56 bits of control store in PROM, 8 Kbytes of character PROM, and 16 Kbytes of scratchpad static RAM. The SCM also contains a VLSI video/memory controller, a host parallel interface, a 9600-baud RS-232-C serial port, and a 6801 microprocessor for onboard diagnostics and serial communication control.

A minimal display system includes the system controller module and one or more display memory modules of one of two types. Just two display memory module types are required to configure a system with almost any of the commonly used frame buffer organizations.

The dual-resolution display module (DRDM) contains four planes of 1280 x 1024 pixels with 30 Hz interlaced refresh or it can be switched by software to 640 x 1024 pixels. Of this, 640 x 512 pixels are usable at 60-Hz noninterlaced refresh supporting two buffers of eight image planes.

Multiple modules can be configured in the same system to support 1024 and 512 line images simultaneously. This feature allows high resolution line drawings to overlay medium resolution images. The DRDM includes a color lookup table that allows up to 256 simultaneous colors from a palette of 16.7 million. It also supports an overlay lookup table for four overlay planes, a blink lookup table for flexible blink-by-plane, by-pixel, or by-area operation, and an edge flag register that allows solid areas to be displayed rapidly by describing only their outlines.

The second type of display memory is the high resolution display module (HRDM) which, in its basic configuration, supports eight planes of 1280 x 1024 display memory at a 60-Hz noninterlaced refresh rate. The HRDM contains an 8-bit color lookup table, is software-configurable to four-plane double-buffered operation, works with 60- or 30-Hz monitors, and supports 2X zoom. Combinations of DRDM or HRDM memory modules can be used to achieve a wide variety of display memory organizations including double-buffered and Z-buffers for three-dimensional surface processing.

The Lex 90 display system frees the SCM and the host computer from the burden of interfacing to system peripherals or a host serial interface by means of an I/O processor. The I/O processor contains a Motorola 68000, four RS-232-C serial ports, an RS-422 interface to optionally connect remote peripherals up to 4000 ft away, and electrically erasable PROM to save baud rate, parity, and other local parameters during power-down. It also has sufficient PROM and RAM to execute I/O processor interfacing tasks.

To increase system performance, the GDP can be augmented with an additional processor to off-load the host processor. This display list processor module resides on the VMEbus. It contains a 68000, a DMA controller, RS-232-C serial communications, and a parallel interface to the SCM. It also supports a serial or parallel host computer interface and 256 Kbytes to 1 Mbyte of memory on the display list

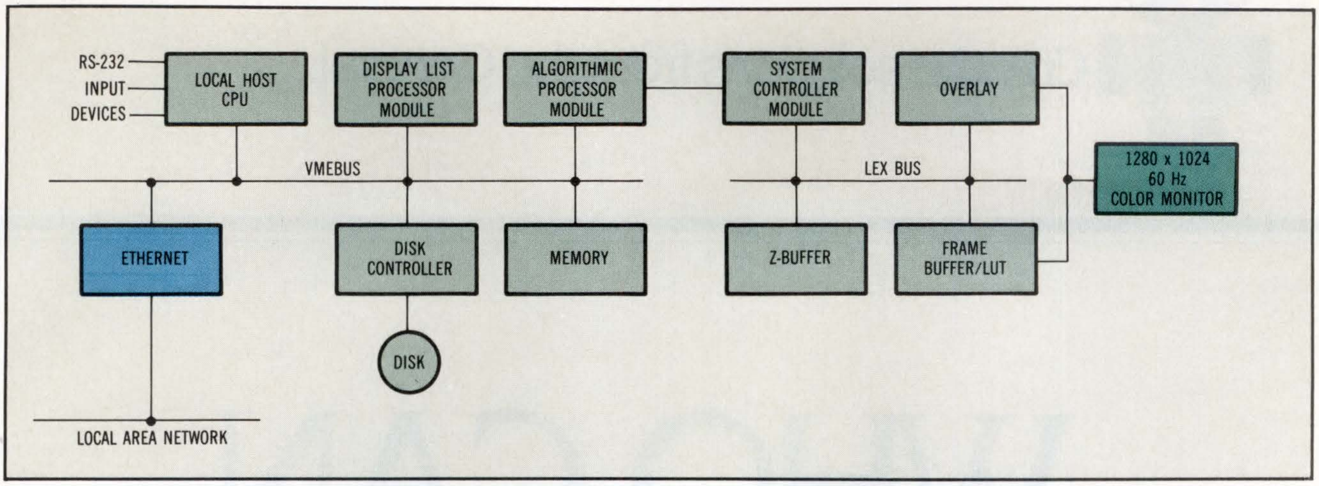

Fig 4 In this architecture, the display system supports workstation design with a range of options for both the GDP and the 32-bit VMEbus-based open system architecture. The hardware options take care of medium and high resolution graphics designs.

processor module with expansion of 2 to 8 Mbytes per board through additional expansion modules. The display list processor module supports expansion and transformation of the user's display list with minimal host computer interaction.

Further performance increase is provided by an optional hardware accelerator. This module, known as the algorithmic processor module includes a bipolar, bit-slice processor and floating point hardware to support 32-bit, IEEE standard, floating point data bases. With the optional arithmetic processor module, a display system is capable of near realtime generation and manipulation of three-dimensional images in its display list.

Both the software and firmware for the product family are as modular and flexible as the hardware.

Together, modules supplied with the family of display systems, modules designed for the family's open system architecture, and VMEbus-based modules from third parties, form a strong base for medium to high resolution interactive graphics systems. Indeed, the entire GDP is provided for, including the decomposition of pipeline processes into separate processors for increased performance (Fig 4).

Software versatility

Both the software and firmware for the product family are as modular and flexible as the hardware. Again, by design, the system designer can choose from upward-compatible sets of software functionality, depending only on the application and the distribution of processes in pipeline implementation.

At its most basic level, the system implements simple, but complete sets of two-dimensional display functions for vectors, text, circles, arcs, polygons, and area-filling. Users can select colors, patterns, and textures. Advanced display functions process three-dimensional data including points, lines and polygons, with removal of hidden surfaces, visible surface shading (constant, Gouraud, or Phong), and surface texturing for transparency and translucency.

With the expansion of the processing pipeline to include the display list processor module or algorithmic processor module, the basic software is augmented with advanced functionality to build, maintain, and invoke a hierarchical, segmented display list for two- or three-dimensional applications with local coordinate transformations and linear display file generation. Besides off-loading graphics display functions, this graphics display capability locally processes graphics inputs, drags objects, and provides other local dynamics.

Regardless of the level of software functionality, the display system is supported by a host software interface that resides on either a host CPU or a local processor on the VMEbus. The host library support insulates the designer from system operation details and provides facilities for application debugging.

System software also supports many of the conceptual constructs of standards such as the Graphical Kernel System, while giving system designers control over low level functionality without sacrificing flexibility and performance. The resultant software architecture allows the display system to be adapted to almost any new or existing two- or three-dimensional CAD, CAM, or CAE application no matter what its distribution of processes and processors.

Please rate the value of this article to you by circling the appropriate number in the "Editorial Score Box" on the Inquiry Card.

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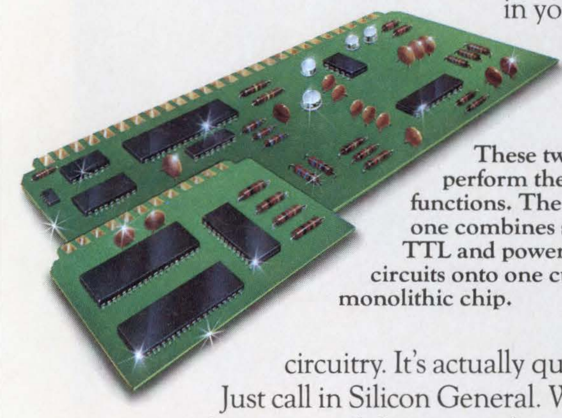

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	SG3635A	40	2.0	Yes	Yes	
H Bridge	SG3636	35	1.5	Yes	Yes	
	SG3638	40	4.0		Yes	External
	SG3638A	50	4.0		Yes	External
	SG3639	40	4.0		Yes	External
	SG3639A	50	4.0		Yes	External
	SG3640	40	4.0		Yes	Internal
	SG3641	40	4.0		Yes	Internal
	SG3643	40	4.0		Yes	External
	SG3643A	60	4.0		Yes	External
Dual H Bridge	SG293	40	1.0	Yes		
	SG293D	40	1.0	Yes	Yes	
	SG298	46	4.0	Yes		
Quad Darlington Driver	SG2064-77	50	1.5		Yes	
	SG2841	50	1.75			
	SG3637	50	2.0	Yes	Yes	
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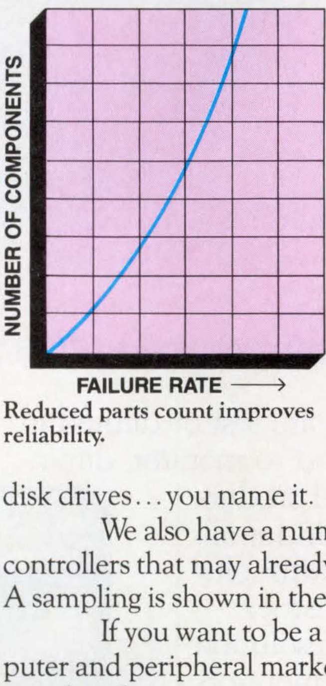

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CIRCLE 101

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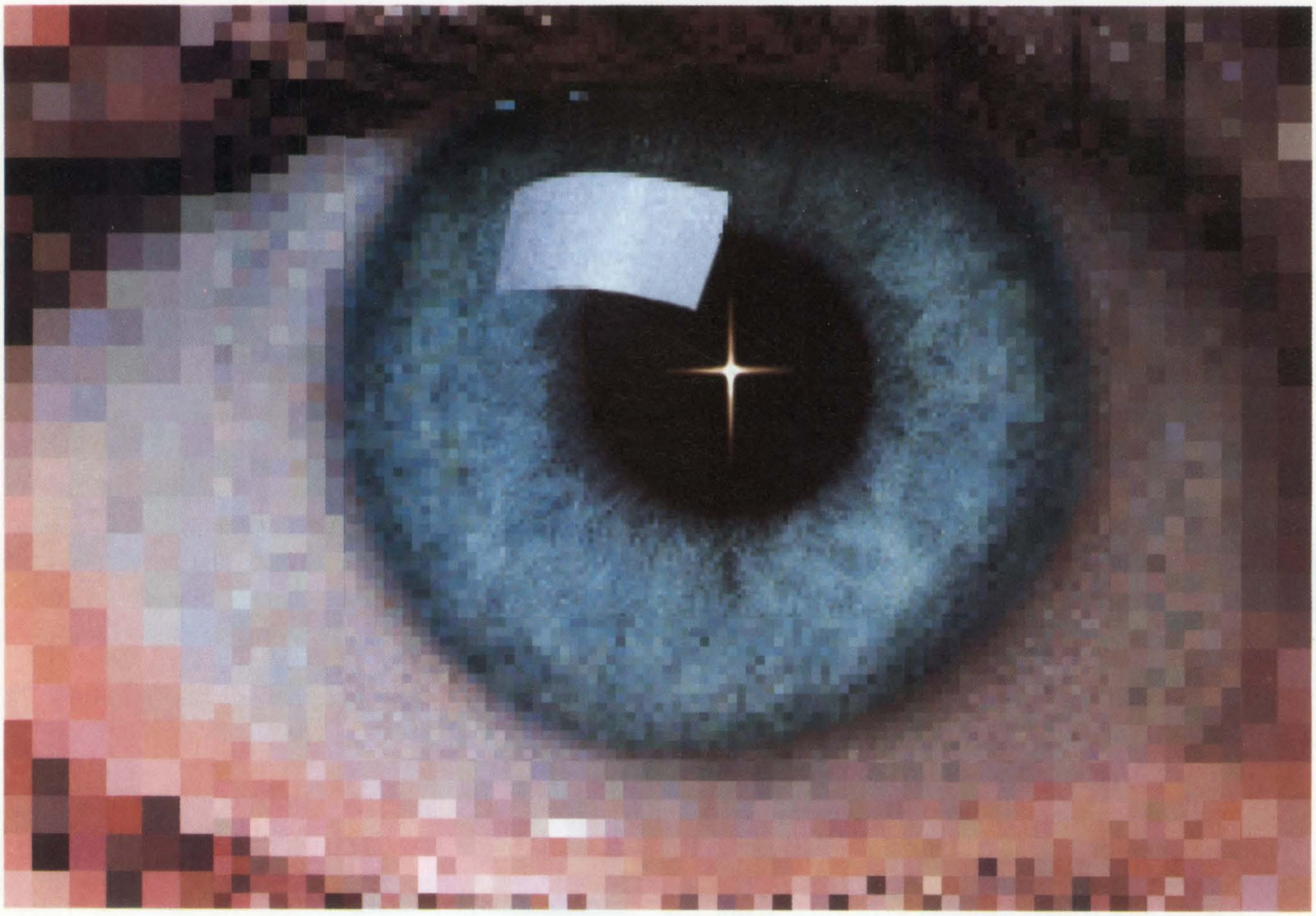

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CIRCLE 102

PROPRIETARY/STANDARD GRAPHICS SOFTWARE MIX TO GIVE MORE

A Graphical Kernel System implemented in software provides a tool, used in a family of high end plotters, that increases programmer productivity.

by Andrew Davis

The history of graphics standards is one of evolving solutions. These solutions came early in the form of *de facto* standards to answer the hardware and software compatibility problems brought about by the proliferation of graphics devices. In the beginning, every computer graphics device spoke a different language; the more successful a device was, the greater the chance of that language, or protocol, becoming a *de facto* standard.

Such was the case with the Tektronix 4010 graphics terminal, the PLOT 10 Terminal Control System (TCS), and CalComp's plotting utilities. But, as the market grew and users became more sophisticated, these standards were not enough. With the appearance of new technologies, the market saw the necessity of device independence and software portability.

Recognizing this trend, Tektronix has implemented its version of one of the emerging standards, the Graphical Kernel System (GKS). This PLOT 10 GKS package represents a logical extension of the PLOT 10 family of graphics software tools.

Andrew Davis is marketing manager of graphics software products at Tektronix, Inc, Information Display Group, Wilsonville Industrial Park, PO Box 1000, Wilsonville, OR 97070. He is responsible for the marketing of the PLOT 10 family of graphics software tools.

Examining the decision to design such a package, with all the design details and capabilities, can provide useful information to the computer system integrator, software designer, and end user alike because each is faced with similar problems. Integrators, for example, must decide if combined graphics packages are suitable for their system, while software designers must understand how high and low end graphics software subroutines are best combined. Moreover, users need to understand just what they can gain from an integrated high and low end package.

In the last few years, there has been a great deal of graphics standard effort. Standards have been studied, proposed, and are now being adopted. Simply put, formal graphics standards bind the concept and functionality of graphics hardware and software and everyone benefits. Today's graphics standards are a direct result of market demand. For example, users demand protection for their software investments, and the graphics industry is responding to this need.

The realization of computer- and device-independent graphics also presents an opportunity for writers of graphics application programs, who will enjoy a wide base of compatible systems for which they can market their products. This availability creates an environment that will draw software and hardware together to provide versatile system solutions to graphics-oriented problems. The benefits will be software compatibility, and host and device independence—all of which add up to using graphics to increase productivity.

Compatibility: the problem

The hardware and software compatibility issue, as well as the consistent interface problem, is being addressed on different levels by new American National Standards Institute (ANSI) proposed standards. These standards support all the basics of graphics programming methodology that have been proven by thousands of real-world applications. In fact, for Tektronix, the new standards are not so much new as they are a formalization of the best of industry practices (Fig 1).

The GKS is a perfect example of the graphics standards evolutionary process. It is the programmer-level standard and addresses the problem of software compatibility. With its roots in earlier graphics standards proposals, including the ANSI/Special Interest Group on Computer Graphics (SIGGRAPH) Core proposal, the GKS has been influenced by many national organizations like ANSI. It is in the final editorial process before formal adoption.

GKS provides source-code portability. It allows graphics application programs to be transported between different installations by dictating a consistent interface. It does this with a high level language binding that defines the exact calling syntax for each graphics function. An exact calling syntax ensures that graphics programmers will be able to work on different application implementations without going through a costly learning curve. GKS also provides a common graphics model to the programmer by standardizing the way graphics functions are accessed, and by providing graphics output on a virtual device. This approach allows the application program to control the way individual workstations interpret a graphics representation.

Two other standards address the hardware compatibility issue and focus on the device interface level. The first, the North American Presentation Level Protocol Syntax (NAPLPS), is based on the videotex concept. Developed in Canada, this idea was adopted by ANSI and provided by AT&T as a standard for transmitting text and graphics over telecommunication lines.

The NAPLPS is primarily aimed at providing a way to connect television sets and other low cost raster devices to telephone lines or cable television networks. In this way, consumers can access public, commercial data bases. Providing only one-way-at-a-time communication, the NAPLPS precludes interactive graphics applications. On the other hand, its powerful data-compaction facilities allow complicated graphics to be quickly transmitted over low cost communication lines.

The NAPLPS may become available in many low cost terminals, and application programs may soon be developed to utilize those terminals. For this reason, computer graphics vendors are starting to look at NAPLPS with keen interest. Although NAPLPS is important because of the number of devices that could potentially use it, it is not an optimal interface for general computer graphics applications. It is inferior for this purpose to another, more general device interface called the Virtual Device Interface (VDI).

The VDI is being developed by the ANSI X3H3 committee as a standard interface between device-independent software and graphics devices. It makes

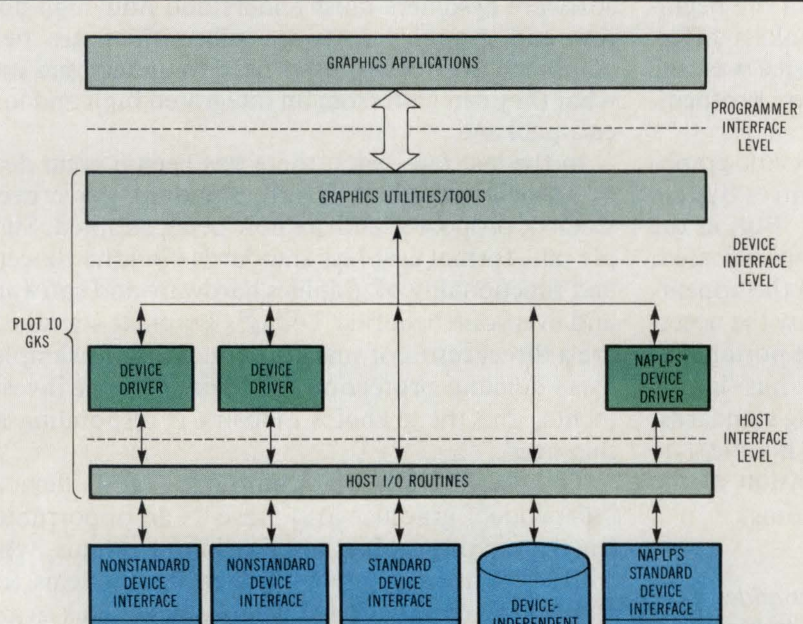

Fig 1 There are multiple graphics software interfaces, as shown in this hierarchy of standards. For example, the Tektronix PLOT 10 GKS operates at the programmer interface level but includes the device interface and host interface levels as well.

all devices appear as "identical" graphics devices by defining a standard I/O protocol for them. Moreover, the VDI is intended to do for graphics what the ANSI standard X3.64 or the VT100 compatibility standard did for text editing. Thus, the VDI offers the potential to eliminate the need for numerous device-specific drivers.

A VDI interface is a part of the graphics utility itself. As such, it can directly communicate with the device supporting the interface standard (VDI). This elimination of a layer of code has obvious throughput benefits to the end user.

There is yet another interface layer known as the Virtual Device Metafile (VDM). The VDM appears at the same level as the VDI in the graphics standards hierarchy. Because application software speaks in only one form of generic graphics commands, the VDM must be able to accept the same information as the VDI. In addition, the VDM is intended to be a standard file format for graphics. Thus, it contains the output functions of the VDI. However, it does not contain the input or control functions associated with interactivity.

The VDM's power lies in its ability to compress graphics information into a small memory space and save it—usually on disk. Since the input to the VDM is device dependent, the ability to replay a VDM picture on any device is a natural result of the VDM structure. The VDM also addresses an important aspect of picture portability by having versions of itself that are both host computer dependent and independent.

Standards implementation

Together, all of these standards define the interfaces and protocols that will eventually define hardware functional ability. Clearly, they must be implemented in a way that takes into account the overall architecture of standards, as well as the interrelationships of the individual levels. At first glance, the implementation options seem to be wide open. Upon closer inspection, however, it is clear that a responsible implementation, both from a technical and economic point of view, has certain constraints.

First, not all the standards have been formally adopted by the participating standards bodies. Some are further along the cycle than others. For example, the NAPLPS has been adopted. In contrast, the GKS, its Fortran binding, and the VDM are out for review. Unfortunately, the VDI standard is lagging behind. This lag is a result of the real-world problems of implementing standards in hardware.

Since some of the standards are not finalized, the interrelationships between all of them are blurred. Today, any implementation of a proposed standard needs to be able to take future changes into account. To minimize the risk associated with standards not yet adopted, it makes sense to choose the most stable and nearly complete standards.

Initially implementing any standard in software offers flexibility to both the developer and the user. A software layer makes it easier to adjust to user needs, and it insulates the user from the inevitable shift in evolving standards. And, once the standard is fixed, the implementation focus can change from the software's flexibility to the hardware's speed and efficiency. This move should not occur until the standards have settled and it is known how users apply them.

Using the GKS

The problem of implementing new and evolving standards is compounded for a company whose products supplied the *de facto* standard for over a decade. Tektronix has the added responsibility of providing a growth path for its past and current graphics users as well as future customers. Consequently, as might be expected, Tektronix chooses to implement the GKS in software.

The GKS gives the application programmer a common graphics model and syntax to speed up the programming task and increase productivity. To the experienced graphics programmer, Tektronix's PLOT 10 GKS is a natural evolution of past tools that requires only short study. To the new programmer, it is the foundation on which most graphics tools, hardware, and applications will be built.

Since GKS provides the conceptual model of computer graphics and because it is out for a final review, it is the most secure standard. Viewed in conjunction with the GKS Fortran binding, NAPLPS, and VDM, the basis exists for the implementation of a powerful, standard-based graphics tool.

Functions supported by the GKS in its Tektronix PLOT 10 software implementation provide a wide range of basic graphics capabilities. Since the Fortran GKS language binding is fully specified, PLOT 10 GKS is implemented as a library of ANSI Fortran 77 graphics subroutines adhering to the GKS Fortran binding. Tektronix opted for an implementation of GKS Level 2B (Fig 2) and supplies all the tools the programmer needs to create and manipulate graphics segments and software text fonts. Level 2B also allows standard digitizing input functions and multiple windows and view ports to be utilized.

The GKS itself supports a full set of drawing primitives and the setting of primitive attributes. The basic drawing primitives in the GKS are the polyline, polymarker, and text primitives. The polyline primitive draws vectors (straight lines) between a sequence of points specified as an array. A single line is merely a special case of the polyline defined by specifying both end points. Note that the polyline marker primitive is similar to the polyline except that it draws a marker symbol at each specified point rather than connecting the points with lines.

For its part in the GKS, the text primitive displays text strings at any position or with any orientation.

GKS LEVELS

OUTPUT LEVEL \ INPUT LEVEL	A	B	C
0	NO GRAPHICS INPUT. MINIMAL CONTROL. PREDEFINED BUNDLES ONLY.	REQUEST INPUT. MODE SETTING. INITIALIZE INPUT DEVICE. NO PICK. NO INPUT PRIORITY.	SAMPLE AND EVENT INPUT. (NOT SUPPORTED BY FORTRAN 77)
1	FULL OUTPUT INCLUDING FULL BUNDLE CONCEPT. MULTIPLE WORK-STATION CONCEPT. GRAPHICS SEGMENT SUPPORT. METAFILE STORAGE.	ALL OF 0B ABOVE, PLUS REQUEST PICK MODE. SETTING AND INITIALIZE FOR PICK.	SAMPLE AND EVENT INPUT. (NOT SUPPORTED BY FORTRAN 77)
2	ALL OF 1A ABOVE, PLUS WORKSTATION INDEPENDENT SEGMENT STORAGE.	ALL OF 1B ABOVE.	SAMPLE AND EVENT INPUT. (NOT SUPPORTED BY FORTRAN 77)

Fig 2 To satisfy a myriad of applications and interests, there are nine parts (not just one) to the Graphical Kernel System (GKS). The PLOT 10-based GKS implementation in software represents Level 2B and is based on a Fortran 77 binding.

PLOT 10 GKS has improved on the appearance of the GKS text by implementing dynamically filled characters. This implementation means that, even on devices that do not support polygon fill, characters will always be filled solidly, regardless of their scale.

The GKS supports raster devices with fill and cell array primitives. The fill operation paints the interior of a closed polyline (a polygon) with a specific color or pattern such as a crosshatch. The cell array primitive allows a two-dimensional array of different-colored pixels to be defined. The cell can be replicated by specifying the desired boundaries. Replication means that computer graphics can overlap imagery data (eg, satellite images).

Some graphics devices incorporate powerful capabilities (eg, the ability to draw arcs, circles, and bars). The GKS allows an application program to access these capabilities through a special escape mechanism called the Generalized Drawing Primitive. By passing a function number and the required parameters to a device's hardware driver, any unique device feature can be invoked.

Workstation flexibility

The GKS adds to the concept of a graphics workstation, which is traditionally defined as a collection of hardware devices connected in some manner. With older workstations, the controlling software knew only one window and one view port and only one set of display attributes. In contrast, the GKS allows multiple window-view port transformations (known as normalization transformations) on each workstation.

The GKS has yet another workstation feature. It allows a special transform—known as a workstation transform—to easily perform two chores that were previously difficult in device-independent graphics. The first chore is to produce scaled drawings in inches or millimeters. The second is to easily utilize a rectangular screen without restricting graphics to a square area (Fig 3).

With PLOT 10 GKS, each workstation (defined as an active display or input device) can have its own group of display attributes such as line style, line color, or character geometry, set to take advantage of specific device characteristics. With this design, application programs can dynamically assign I/O devices without having to reset display attributes.

The GKS also supports a full set of input operations that allows application programs to receive input from a broad range of interactive input devices. The GKS's input operations are grouped into five classes: Choice, Locator, Pick, String, and Valuator. These classes of the GKS support the optimum input device for a particular working environment. The result of this support is improved interactivity.

The Request Locator function returns a position in world coordinates while the Request Valuator function indicates the current value of a continuous valuator device such as a potentiometer. The Request Choice function returns an integer that represents one of a set of choices. For its job, the Pick function returns the graphics segment number that corresponds to the objects being selected with graphics input. Finally, the Request String function reads character input from a keyboard device. The way these logical functions are implemented (ie, with joystick or mouse) is workstation dependent.

The GKS has two other input modes besides the Request mode supported by PLOT 10 GKS. The level structure of the GKS (Fig 2) specifically allows implementation of the Request mode only. This is

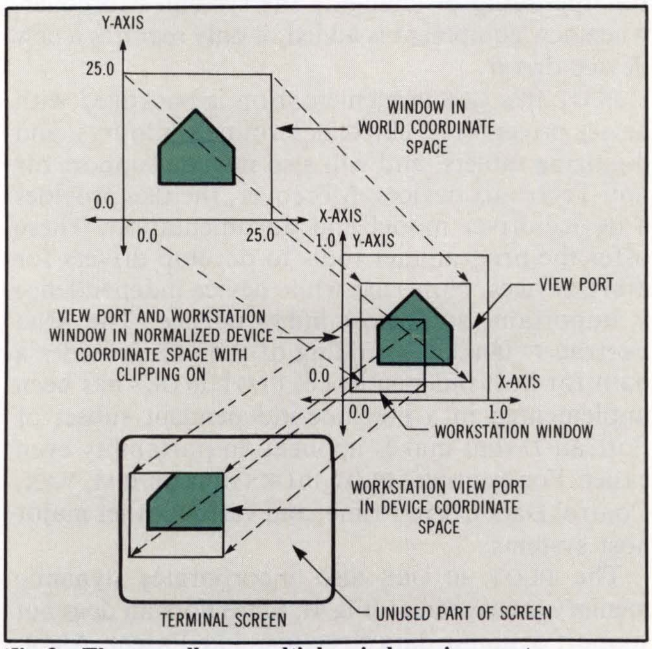

Fig 3 The GKS allows multiple window-view port transformations at a terminal screen. This feature allows scaled drawings and the use of a rectangular screen without restricting graphics to a square area.

because Sample and Event modes require I/O capabilities unavailable in Fortran 77. These limitations provide useful information to the designers of standard programming languages.

The GKS also supports graphics segments. A segment is a collection of output primitives that can be manipulated as a whole. Once created, segments become graphics entities that can be used as building blocks to create more complex pictures. Designers can manipulate segments in many ways including translation, rotation, and scaling. Segments can also be renamed, deleted, inserted into other segments or into a stream of output primitives, made visible or invisible, and more. The use of segments allows a programmer to access a variety of powerful graphics functions. It offers the ability to treat graphics data in a logical, picture-oriented manner.

Although it is not incorporated in the GKS standard, PLOT 10 GKS implements a VDM to allow the designer to have permanent storage of graphics (and non-graphics) data. Metafile processing involves the retrieval of stored graphics information and the manipulation of the "picture" into a desired presentation. It can scale, rotate, translate, or modify the stored graphics. It can then send the output through the VDM again for storage or through the device driver to any output device.

Device independence featured

The GKS defines a device-independent graphics system. Thus, applications can be written without concern for a device's physical attributes because its specifics reside in device-dependent software modules. The system integrator's or end user's initial software investment is protected and a path is opened for upgrading or changing the system. Moreover, when new equipment is added, it only requires a new device driver.

PLOT 10's GKS implementation is packaged with device drivers for Tektronix terminals, plotters, and digitizing tablets, and will also include support for non-Tektronix devices. Moreover, the GKS provides a device-driver model and documentation. These offer the programmer tools to develop drivers for more devices. Note that while device independence is important, so is host independence. The ANSI Fortran 77 language binding of the GKS provides a path for host independence. PLOT 10 GKS has been implemented in a machine-independent subset of Fortran 77 that makes application portability even easier. For example, PLOT 10 GKS runs on IBM, VAX, Control Data Corp, Prime, and various other major host systems.

The PLOT 10 GKS also incorporates dynamic memory management (Fig 4). Since Fortran does not support dynamic data structures like Pascal, Algol, and other languages, sufficient memory space must be allocated (dimensioned) to allow storage for the maximum number of workstations with the maximum number of allowable input devices. This procedure consumes a lot of memory that is not likely to be used, while the space available for segment storage, pattern arrays, and character fonts may be very restricted and fragmented.

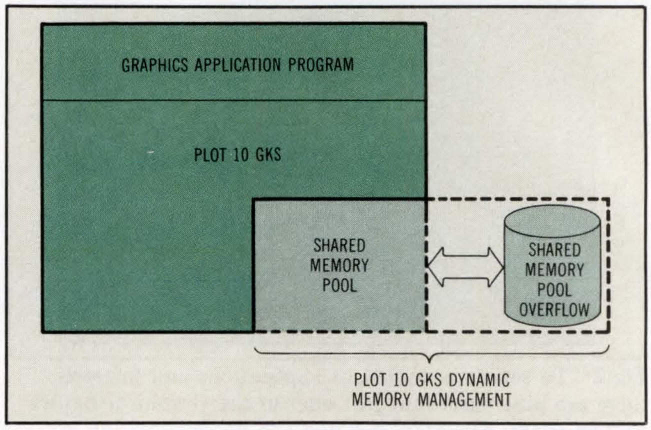

Fig 4 A dynamic memory management facility exists in PLOT 10's GKS and allows allocation and reuse of a memory pool. When the pool is full, parts are copied to a disk file. The parts copied are intelligently chosen for minimal system impact.

To solve this memory problem, a dynamic memory management system enables allocation and reuse of a memory pool. Memory not currently used for workstation variables can be used for segment storage, pattern arrays, and character fonts. When the memory pool becomes full, the system copies part of these data structures to a disk file in a "smart" way, based on the type of structure and its potential impact on system performance. This single view of storage is transparent to both programmer and user.

Through the use of installation tools, the PLOT 10 GKS can enable or disable this memory management feature based on the requirements of the installation and the size of the memory pool. Moreover, any disk overflow area can be independently configured. This feature offers the strength of a "virtual-like" function for nonvirtual machines and the benefits of a nonpaging, large, shared pool on virtual systems.

Optimized for implementation in hosts with 32-bit or larger word sizes, the PLOT 10 GKS is today software based. But, as mentioned earlier, when standards are stable and it is known how they are being used, software functional ability will be implemented in hardware. In effect, this implementation will move the standards and interfaces down into the graphics device itself.

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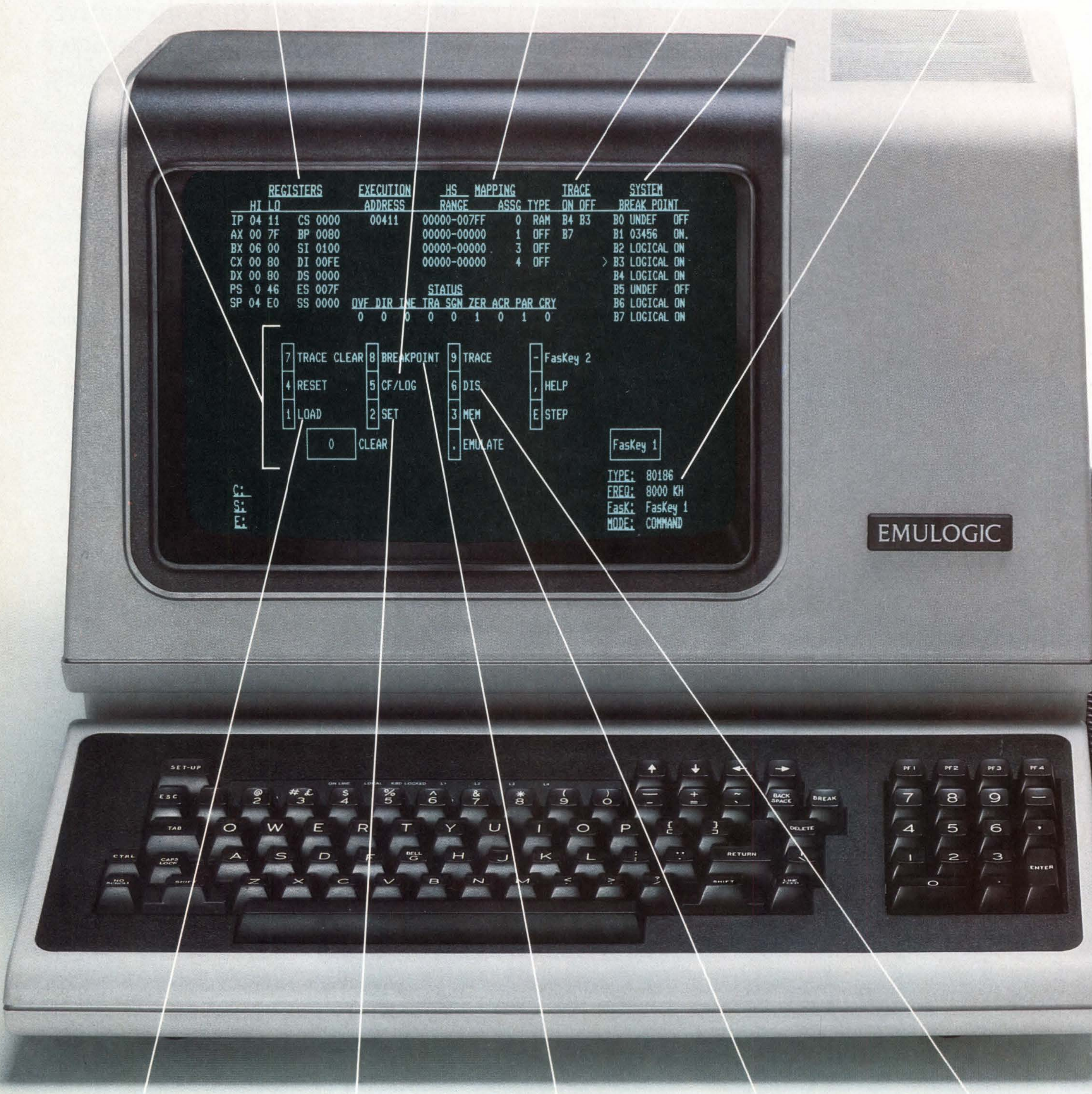

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Selects LOAD screen with all options.

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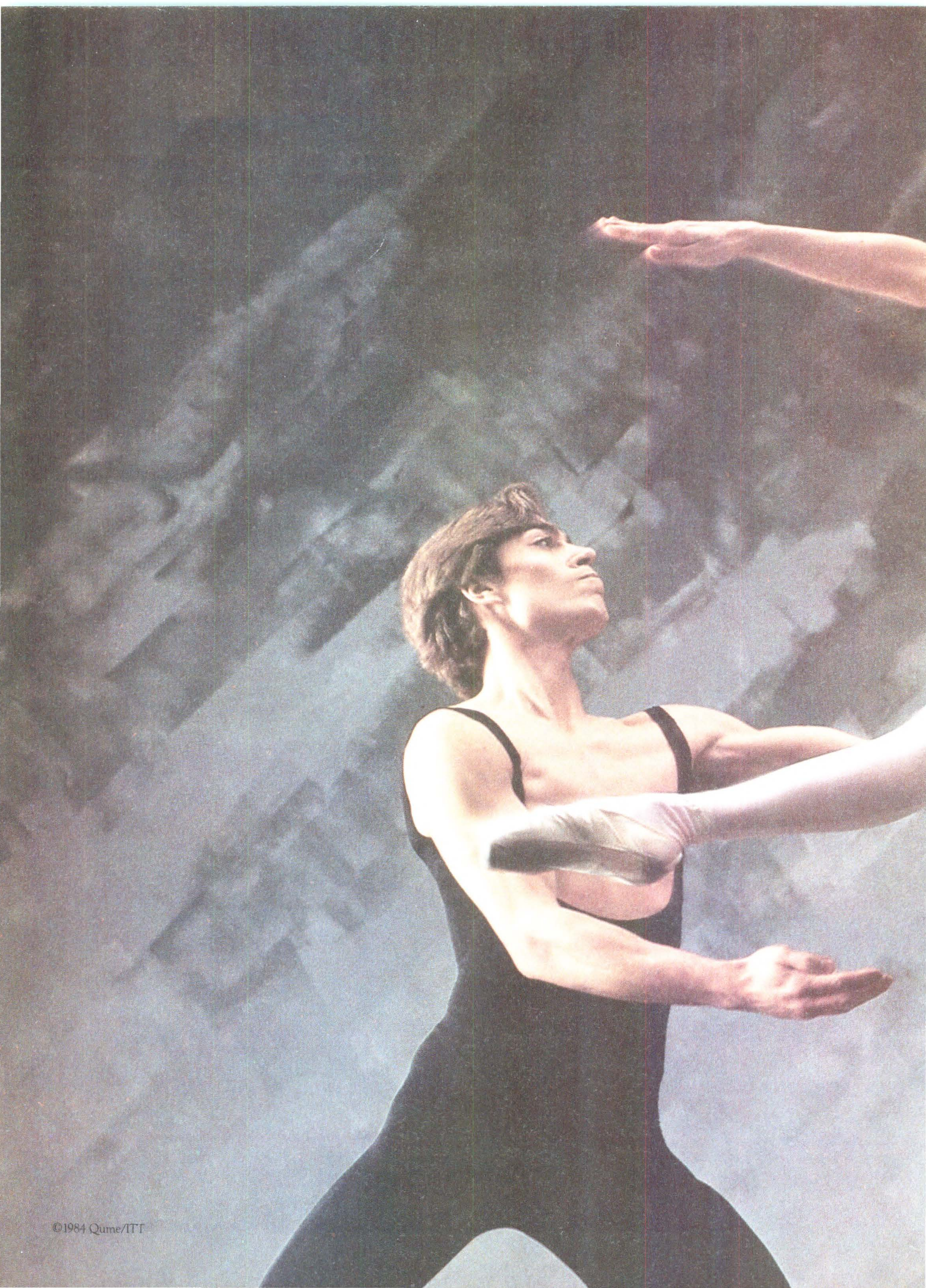
United Kingdom: MSS, (44 494) 41661; **West Germany:** Instrumatic Electronic GmbH, (49 89) 852063.

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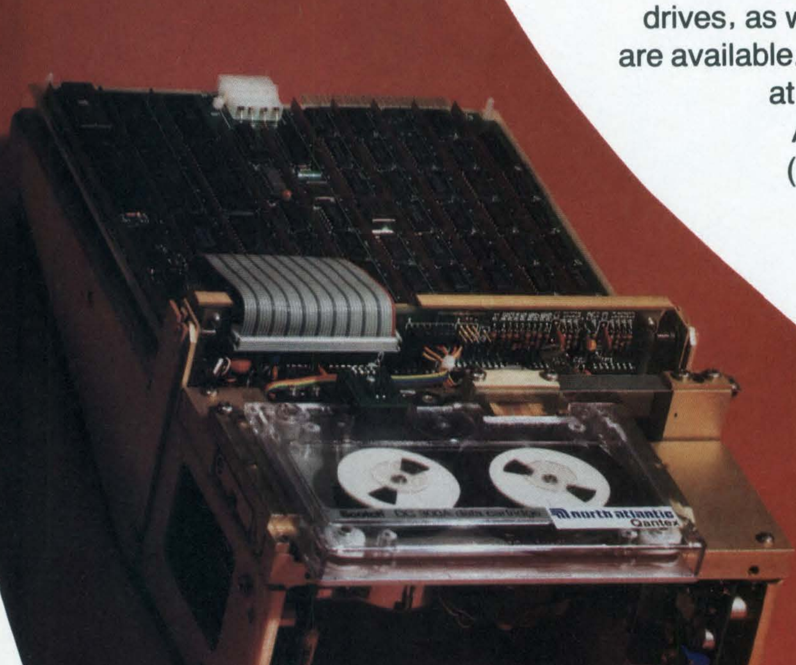
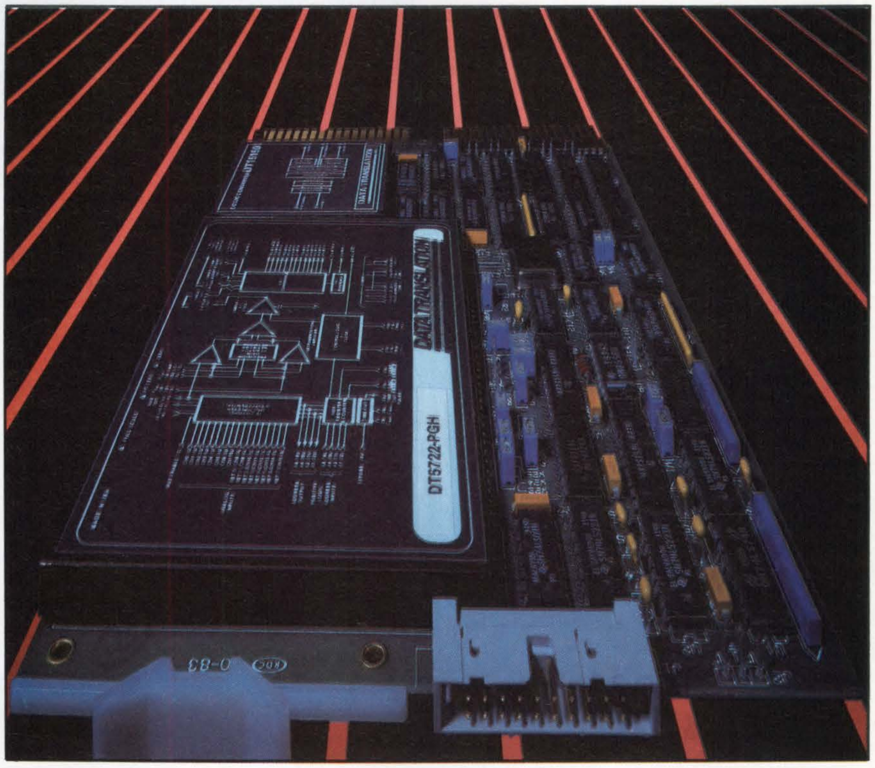


Fast A-D boards pump data into LSI-11 bus without transfer loss

A family of data conversion interfaces is stepping up transfers to mass storage, maintaining data collection rates of 250,000 samples/s and throughput rates to 100 kHz. Traditionally, transfers as fast as this suffer from undetectable error conditions, such as data loss during data buffer switching and time shifts due to data gaps—as well as buffer overruns from bad sectors or tracks. Together with CPLIB and RSXLIB software packages, the DT2752 family's continuous-performance architecture conquers these problems. Moreover, the boards are fully compatible with LSI-11/23 and LSI-11/73 CPUs.



Taking advantage of true 22-bit addressing, the boards collect and store large amounts of data as a single contiguous block in any user-defined memory section. This technique differs from quasi 22-bit addressing, which breaks up large data blocks and stores them in separate buffers. The 16 LSBs of the starting memory address load into the DMA current address register, while the 6 MSBs load into the DMA extension register. The upper 6 bits can be dynamic or static depending on the jumper. If they are dynamic, the A-D system increments both registers to make room for any volume of data up to 4 Mbytes, stored contiguously as a single block. If the upper 6 bits are static, the data is stored contiguously until a 64-Kword boundary is reached. At that point, the address register automatically wraps around to the other end of the memory segment.

For enhanced DEC compatibility, four-level interrupts and an arbitration mechanism allow the board's bus location to be independent of its interrupt level. When multiple interrupts occur, the DT2752 services every one in order of priority. This is unlike some other boards that service only the highest priority interrupt, then clear all others. As part of the multilevel interrupt structure, the boards have two internal interrupts. Each is a separate interrupt source with a unique vector. The Done interrupt is generated when a data point is collected and ready for transport to the CPU. It occurs in the DMA mode after all the data is transferred to memory. The error interrupt is generated when an error condition occurs in the data acquisition process.

The boards transfer data to memory by DMA or programmed I/O. In either mode, the system can be polled or interrupt driven. Setting the DMA and Done interrupt bits through software selects the DMA mode. Up to 64 Kwords can be transferred without program intervention. After 64 Kwords, the process must be restarted.

Conventional methods of transferring more than 64 Kwords usually result in data loss while the first buffer transferred to disk and the registers on the board are reset. Software libraries are instrumental in overcoming this problem by providing proprietary program techniques that acquire data continuously without gaps.

Realtime software support runs under RT-11 (DTLIB and CPLIB) and RSX (RSXLIB) operating systems. The software packages consist of two parts: a loadable or resident device driver and a subroutine library. An application can call subroutines to collect, store, and output data. Fortran programs call DTLIB and CPLIB, while Fortran, Macro, or Basic can call RSXLIB.

Two methods of data conversion are available—single conversion per start and multiple conversion per start. Clearing the multiple conversion bit makes way for single-conversion mode selection. In this mode, the system collects one data point for each start (software or clock) issued. After data is collected, it is stored and the system waits for another start to acquire another data point.

The multiple-conversion mode can only be selected in conjunction with the DMA transfer mode. Once data acquisition starts it continues automatically until the specified words are collected and transferred. In this mode, data acquisition occurs at the maximum throughput rate.

To meet applications in signal processing, speech research, high speed process monitoring, and laboratory research, the boards come in three models. The 50-kHz 8DI/16SE has optional programming gain. Also available are 125- and 250-kHz versions with the optional gain feature.

The 50-kHz version is priced at $1495, the 125-kHz version at $1795, and the 250-kHz version at $2495. The programmable gain option is an additional $175. First deliveries are scheduled for mid-July. **Data Translation,** 100 Locke Dr, Marlboro, MA 01752. —*M.B.*

Circle 260

Development system based on IBM PC puts 8088/80188 on STD bus

To strengthen STD bus applications, Ziatech is introducing a software development package for 8088/80188 processors along with a line of STD bus based single-board computers using the 80188. Extended capability for the 8-bit bus will be particularly useful in controller architectures, where STD systems address a wide variety of applications.

The series 8800 prototype development system, which runs on an IBM PC or compatible, consists of an 8088-STD target system in an eight-slot card cage, a power supply, software, and documentation. Offering a 16-bit internal capability, the ZT 8812 processor board is specially designed to work in the STD bus development process. It contains the 8088 processor with a socket for an optional 8087 floating point processor. An 80130-6 interrupt processor with counters and timers provides Intel's iRMX-86 operating system kernel. In addition, the DBUG 88 PROM monitor resides on the CPU board.

Software forms the major portion of the prototype development system. It consists of the DBUG 88 monitor and a disk-based development package, PC/STD 88, which runs on the PC. The user can

prepare object code for the development system, using PC-compatible assemblers or compilers, as well as any convenient editor. The PC/STD 88 package then structures the object file for use on the target system. It lets the user specify memory address positions, links modules for use with other programs, and formats the files for loading into the target system.

Once it has loaded the linked object code into the target system, PC/STD 88 sets up the PC as a debug console communicating with the monitor on the CPU board. Using the debug monitor, the user can examine and alter registers on the 8088 as well as on the 8087 numeric processor from the PC. Other normal debugger functions let the user set breakpoints, run programs, perform I/O operations, and examine and alter target system memory. When the code has been fully debugged, the monitor PROM can be replaced with a PROM containing the user's routines.

In addition, the ZT 8814 and ZT 8815 single-board computers are based on the 80188 and run at 5 and 8 MHz, respectively. Each provides 5 byte-wide memory sockets that accept memory chips with capacities up to 32-Kbyte RAM or 64-Kbyte ROM. DBUG 88 resides in one memory socket. The same equipment and software can develop software for the 8088 or 80188 board.

The prototype development system, priced at $2800, is available four to six weeks ARO; the ZT 8814 and 8815 are $650 and $695, respectively, and will be available this month. **Ziatech Corp**, 3433 Roberto Ct, San Luis Obispo, CA 93401.

—T.W.

Circle 261

Tape subsystem exhibits full-size performance at low cost

The model 9250 Shamrock group code recording tape drive uses advanced LSI gate array and microprocessor technology to condense its GCR formatter onto two circuit cards. These cards are directly integrated into the tape drive package to support high end performance.

The 50-in./s, start/stop device features vacuum column technology. The brushless, direct drive, pneumatic system is insensitive to changes in voltage, altitude and line frequency, and day-to-day variations in barometric pressure.

Automatic threading, including tip of tape detection and column loading, occurs via one button. This feature minimizes operator tape handling and contamination. Automatic rewind takes only 2 min for 2400-ft reels.

Tape densities start at 6250 bits/in. in GCR and include 1600 bits/in. in phase encoded. Two methods of density selection are available. The host computer can select the density under software control or the operating system or interface allows the operator to select the density. For users with 800-bit/in. nonreturn to zero inverted (NRZI) requirements or large existing NRZI libraries, the drive's tri-density option eliminates the need for additional tape drives.

For applications requiring multiple tape drives, it allows master/slave daisy chain expansion to 1 x 2, 1 x 3, and 1 x 4 systems. Only the master has the embedded formatter, saving the expense of duplicating both the formatter and the interface electronics for each additional tape drive. For flexibility in the field, any master unit can be converted to a slave (or vice versa) by moving the two formatter circuit cards.

Tape drive specs include a tape speed of 50 in./s, a gap size of 0.3 in. in GCR for read and write, 0.6 in. in phase encoded for read and write, and 0.6 in. in NRZI for read and write. GCR access times reach 3 ms for a write and 3.4 ms for a read. Transfer rates are 312.5, 80, and 50 kbits/s for 6250-, 1600-, and 800-bit/in. tape densities, respectively.

Using GCR technology has several advantages. It offers increased data density for significant file compaction over previous industry standard densities. This results in less media to store data, less library space, and reduced handling. System throughput enhancements occur via a high data rate together with automatic error correction circuitry to eliminate rereads.

The 9250 costs $7399 with production deliveries scheduled for October 1984. **Telex Computer Products, Inc**, 6422 E 41st St, Tulsa, OK 74135.

Circle 262 *—M.B.*

Analyzer combines hardware/software tests in one device

Giving designers a single instrument for testing, debugging, and analysis, the HP 1630G supplies three analysis functions for digital development: timing, state, and software performance. With its 65 channels, the analyzer is suitable for applications involving 16-bit microprocessors and multiple bus monitoring.

The unit provides timing-waveform diagrams that simultaneously display up to eight channels, and has user-definable labels to simplify data evaluation. Adjustable parameters include wide magnification range, glitch display, and direct time readout between cursors.

State listings display address, data bus, and status/control-line activity. Selectable display modes include binary, octal, decimal, hex, ASCII, and relocation, as well as user-defined and microprocessor-specific mnemonics. For easy interpretation, the user can display and/or trigger on code in terms of relocatable or absolute address or mnemonics.

Using software performance analysis measurements, users can view selected portions of code and measure time or occurrence distribution. With this technique, the user can spot bottlenecks in operating software, determine best- and worst-case conditions as a function of data variables, and establish benchmarks for modules or an entire program. In addition, graphs of memory activity as a function of occurrence can indicate infinite loops, erroneous jumps, and activity in forbidden areas.

The device contains programmable nonvolatile memory, where the user can store an inverse assembler (disassembler) plus one setup configuration. When turned on, it automatically configures for a particular application. Time tagging measures the time between each stored state in the state analysis mode. It can also measure the time from the trigger point to each state or the number of unstored states between each stored state.

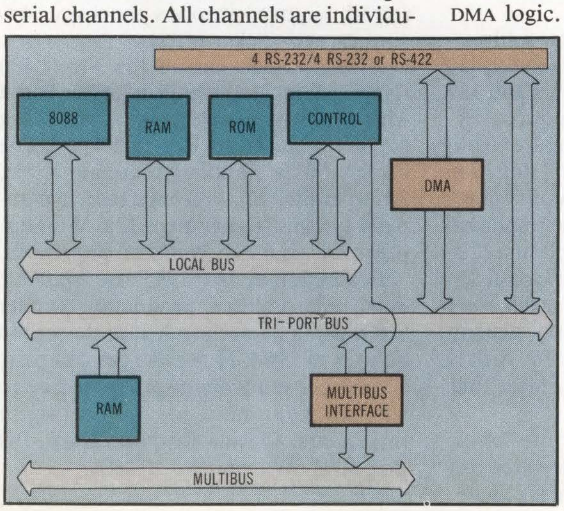
Histograms measure program flow by showing the user where the program spends most of its execution time. It counts either all acquired states or only the instructions in the histogram. This eliminates confusion if the program generates in line code or if memory blocks are interspersed between sections of the program.

The logic analyzer is priced at approximately $12,000. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303. *—M.B.*

Circle 263

Peripheral processor removes communication overhead from host

Providing high speed data communication, the SI08 intelligent processor uses eight serial channels to take over communication responsibilities from the main processor. It is designed for multi-user, multitasking systems such as Unix, RMX-86, and MPM-86. The Multibus-compatible serial communication module features a 16-bit 8088 microprocessor that handles all communications over eight serial channels. All channels are individually programmable and provide asynchronous, bisynchronous, HDLC, and SDLC operation.



A tri-port RAM architecture allows the user to place an onboard 16-Kbyte buffer anywhere in the 20-bit Multibus address space. Once the address is fixed, the tri-port memory can be accessed from any CPU on the Multibus, the processor, or via the serial I/O channels through the DMA logic. Each of the eight input and eight output ports provides a separate DMA channel for continuous operation at a minimum of 9600 baud. Each channel also handles full duplex DMA operation without intervention by the onboard 8088 or the main system microprocessor.

In addition to the 16-Kbyte data buffer, the module contains a 1-Kbyte cache that operates on an internal local bus. The processor manipulates information in local memory using DMA. The 8088 therefore, reads and writes to the local memory together with DMA I/O and can provide no wait states with either memory access. The onboard 16-Kbyte memory is designed around a tri-port interface. The local memory is accessible by any other master on the Multibus as well as by the 8088 and the DMA serial I/O logic. The unit contains full interupt logic for all channels. Baud-rate generation is programmable with standard timer ICs.

Using a coprocessor I/O control-block technique, the host processor places information in the tri-port RAM and requests an I/O operation. The 8088 examines and analyzes the I/O requests and completes the operation without further host intervention. All operations can occur from the local buffer or from the Multibus. Large blocks of information can transfer directly from Multibus main memory, completely bypassing the buffer. An option loads or removes data in the DMA mode from the buffer or from main memory on the Multibus.

The board costs $2800 with immediate delivery. **Distributed Computer Systems,** 330 Bear Hill Rd, Waltham, MA 02154. *—M.B.*

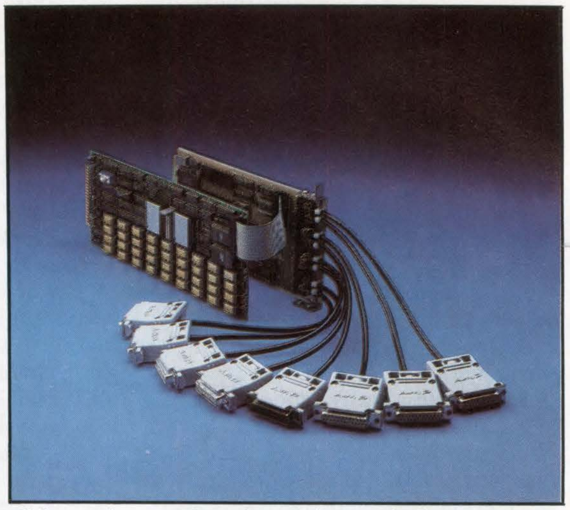
Circle 264

Supermicros run multiple operating systems concurrently

By replacing dedicated CPU boards with a multitasking terminal server, Molecular Computers' series 9 and 36 systems can each share applications running under different operating systems. This intelligent serial multiplexer, called a terminal concentrator processor, gives users access to any available 8- or 16-bit application processor. In turn, the application processors become system resources that can run CP/M-80, MP/M-80, CP/M-86, MP/M-86, or MS-DOS programs.

The multiplexer consists of an Intel 80186-based processor card with its own memory and firmware (photo front) and an 8-port serial I/O card (rear). Freeing users from dependence on a single CPU enables the server to make quick transitions between different applications and access programs written for incompatible operating systems. Moreover, adding a 186 CPU with its own memory significantly speeds up word processing, spreadsheet, and database programs originally written for the 8088.

Previous systems (the Supermicro X series) tied each user to a terminal connected to a Z80 processor card. This card communicated over the backplane bus with other Z80 or 8088 processors via the MP/M operating system. While this approach provides good functionality, it limits users to whatever degree of multitasking the operating system or the Z80 card offers.



Tabletop series 9 has slots for up to 9 application processor cards, 20- or 30-Mbyte hard disk, a 320-Kbyte floppy disk, and an optional streaming tape backup. The series 36 comes in a free-standing enclosure identical to that of the earlier X series, and has a 60-Mbyte, 5¼-in. Winchester disk (with space for two additional drives), a 320-Kbyte floppy disk, and optional tape.

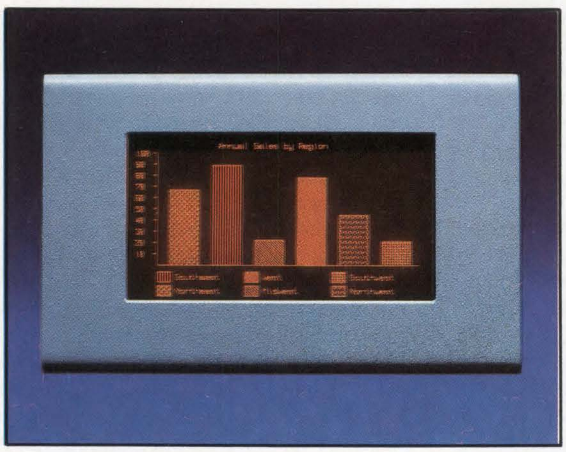
The AP/186 serial I/O card and terminal concentrator processor are fully compatible with earlier systems, and work with the company's proprietary n/Star operating system to let a central file processor handle all disk I/O. Containing 64 to 256 Kbytes of cache RAM, the file processor improves overall disk performance by storing frequently used data "online."

The price of the terminal concentrator processor is quoted under $2000; the AP/186, $1700; and individual Z80 processors, about $1000. Available in May, the series 9 (without application processors) will cost approximately $7995; the bare series 36 (available in June) will be about $18,995. **Molecular Computers, Inc,** 2764 N First St, San Jose, CA 95134.

—S.B.

Circle 265

Hybrid plasma display simplifies driver electronics, cuts cost



Using patented self-scan with memory, the model 120 flat panel combines the inherent memory of ac plasma with the powerful addressing of dc plasma to reduce expensive driver electronics. The result is a full-page display, with 480- x 250-pixel graphics and 80-col x 25-row alphanumerics, that promises to compete pricewise with high quality CRT monitors. Moreover, because the display subsystem is unaffected by magnetic fields and emits no X rays, it can function in industrial environments as well as office and transportable systems.

The all-points addressable, 120,000-pixel display uses only 40 drivers and 137 driver-to-panel interconnections. This compares with 730 X-Y drivers and 730 driver-to-panel interconnections for the same resolution on typical ac plasma displays. Instead of using a driver circuit for each row and each column of pixels as ac plasma panels do, the hybrid display incorporates a dc scan section for X-axis addressing and an ac memory layer that multiplexes Y-axis drivers.

In addition, the 67-pixel/in., 7.2- x 3.75-in. (18.3- x 9.5-cm) display area can be seen from a 150-degree viewing angle. An inherent display storage function eliminates the need for refresh. Once data is entered, the subsystem maintains the image as long as power and an input clock signal are applied to the drive electronics. Otherwise, only the entry of new data will alter the display. Eliminating display refresh removes previous panel size constraints and flicker effects.

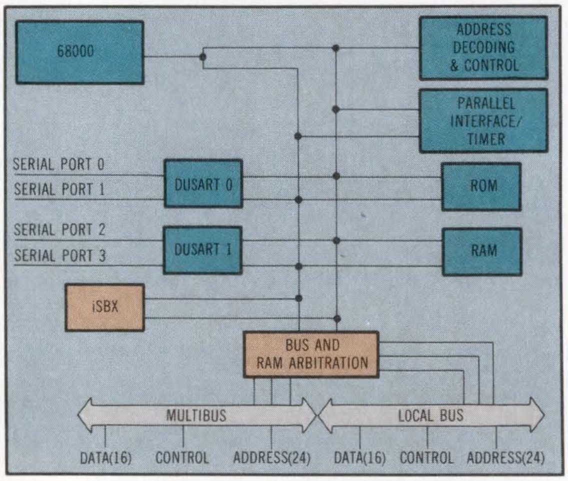
Overall dimensions of the 3-lb (1-kg) flat panel, including built-in driver board with all subsystem electronics, are 11.2 x 6.52 x 1.4 in. (28.4 x 16.56 x 3.6 cm). The display has a standard TTL-compatible, 8-bit parallel data bus interface to computer systems. It consumes 12.5 W in display mode, and 20.5 W in data entry mode.

Evaluation units ($1795) are available now, and volume production (under $1000 per unit) is scheduled for the second quarter of 1984. However, the company expects per-unit volume prices to drop to between $300 and $400 within two or three years. **Plasma Graphics Corp,** PO Box 4093, Warren, NJ 07060.

Circle 266

—D.H.

Single-board computer stores 512 Kbytes with onboard RAM



Standard OB68K/MSBC1 equipment includes 256 Kbytes of triple-ported (CPU, Multibus, and local memory bus) RAM with parity. The zero wait-state RAM uses 128-K x 4-bit single inline package chips. Using these chips allows RAM to expand to 512 Kbytes. The board incorporates the 68000 16/32-bit microprocessor operating at 10 MHz on the Multibus. Optional processors include a 12.5-MHz 68000 and the 68010 virtual memory processor operating at 10 MHz.

When a parity error occurs, a circuit containing a 68230 parallel interface/timer chip identifies the specific RAM bank where the error originated. A 24-bit timer/counter in this chip generates system interrupts. Four JEDEC-style, 28-pin ROM sockets are also provided for monitor, boot, or program PROMs. Total ROM capacity is 128 Kbytes.

The board implements a high speed local memory bus over a P2 connector. This bus is functionally compatible with the Intel iLBX spec. The local bus provides the 68000 with a high speed arbitration-free extension of onboard memory. Total capacity is 16 Mbytes with the addition of four memory boards. The local bus operates in conjunction with Multibus activities without significant effect on global memory or peripheral functions.

Two dual-Universal synchronous asynchronous receiver/transmitter chips provide a four serial port capacity. These chips handle asynchronous protocols, synchronous byte-oriented protocols (IBM Bisync), and synchronous bit-oriented protocols (X.25, high level data-link controls, and synchronous data link control). Two independent baud generators in each chip provide rates of up to 1000 kbaud.

An iSBX expansion connector provides additional I/O. Expansion modules plug in for a wide range of I/O and control options including parallel I/O, serial I/O, floppy disk controller, printer port, IEEE 488 controller, analog I/O fixed/floating point module, or graphics controller.

Seven levels of priority interrupts, one of which is nonmaskable, configure to be bus-vectored or auto-vectored in any combination. All the interrupt sources route to seven inputs in any combination via jumper cables.

The board implements full address and bus arbitration for single- and multiprocessor systems, and is compatible with a range of existing IEEE 796 products. **Omnibyte Corp,** 245 W Roosevelt Rd, West Chicago, IL 60185.

Circle 267 *—M.B.*

Featherweight disk drive protects floppy media in hard shell

The 1-lb, 3½-in. JU-312 floppy disk drive puts a mechanical design that automatically loads or ejects cartridge-style floppies inside a sleek footprint. No lightweight when it comes to memory capacity, however, the low cost drive takes single-sided disks that store 250 Kbytes each; a single-sided, double-track method boosts that capacity to 500 Kbytes. Beyond that, the company has near-term plans for a double-sided, double-track release that will top 1 Mbyte.

Media stow in a hard plastic case featuring button-controlled write protection and a head window shutter that opens when a disk enters the drive. A loading mechanism automatically inserts or ejects disks when activated by a push button on the front panel. This packaging and loading concept makes it easier to store and handle the disks, and gives the vulnerable magnetic media a measure of protection against the environment.

At 32 x 104 x 161 mm (1 x 4 x 6 in.) and 600 g, (1 lb), the JU-312 floppy drive is one-fifth the volume and one-third the weight of typical 5¼-in. disk drives, yet plug-compatible with its bigger brothers. Data transfer rate is 125 kbits/s FM or 250 kbits/s MFM. A three-phase, brushless motor controlled by a single LSI spins the disk at 300 rpm. To economize space, this flat motor mounts directly on the package board.

Together, the direct-drive stepping motor and a steel drive band ensure high reliability, and position the read/write head for 6-ms track-to-track seeks. Maximum settling time is 15 ms, while average positioning time is 58 ms. Estimated deviation is ±1 percent, and variation, ±1.5 percent.

Greatly reduced parts count also improves reliability. In all, three custom LSI chips with minimal support components control the disk drive; the other two LSI circuits manage read/write and control functions. The interface side of the control circuit sends and receives TTL-level signals. In star or daisy chain configuration, up to four drives will attach to the controller.

Gateless drive mechanics consist of a die-cast aluminum base plate that connects to signal ground; mountings protect drive circuits from electrical noise. In quantity, unit price will be about $100; the drives are available now. **Panasonic Industrial Co, Electronic Component Div,** PO Box 1503, Secaucus, NJ 07094.

—D.H.

Circle 268

Take it from someone who comes from a long line of card readers:

"Let me tell your fortune. I see you are searching for something. You have very high standards, very demanding needs. You are looking for a card reader of outstanding quality and reliability.

"Seek no further, stranger. Panasonic has the complete line of Optical and Magnetic Card Readers and systems to satisfy your needs.

"Quality Optical Badge Readers, in both vertical and horizontal versions, with or without automatic card ejection. A uniquely designed Automatic Magnetic Card Reader, built for strength, durability and precise operation. And a choice of budget-priced Manual Magnetic readers/writers, offering precision performance and easy operation in a compact, versatile package.

"The Optical Readers are capable of reading from 20 to 264 bits. And the Magnetic Readers can read up to 119 characters.

"Which one to choose? Let me make it easy for you . . . just consult my chart.

"It is your good fortune that you came to me. Now you will want to know more. To learn about the long line of Panasonic Card Readers, you must contact Computer Products Division, Panasonic Industrial Company, Division of Matsushita Electric Corporation of America, One Panasonic Way, Secaucus, N.J. 07094; call (201) 348-5346 or in Chicago (312) 364-7900 ext. 304.

Model Number	Card Standard
MAGNETIC	
Manual swipe read only	
ZU-1401N or 02N	ISO1 or ISO2*
ZU-1420	ISO1 and ISO2
ZU-1601 or 02	1 or 2
ZU-1601E or 02E	1 or 2
Manual swipe read/write	
ZU-2401N or 02N	1 or 2
Manual insertion read only	
ZU-1801NA or 02NA Partial track	1 or 2
ZU-1851NA or 52NA Full track	1 or 2
Manual insertion read/write	
ZU-2801NA or 02NA Partial track	1 or 2
Motor driven read only	
ZU-1201 or 02	1 or 2
Motor driven read/write	
ZU-2201 or 02	1 or 2
OPTICAL	
Horizontal read	
ZU-XXXHR*	Type II, III
Vertical read	
ZU-XXXVR*	Type II, III, IV, V

*XXX denotes number of bits ranging from 20 to 264 bits.
ISO1 denotes IATA standard
ISO2 denotes ABA standard

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CIRCLE 110

Workstation surpasses PDP-11/23 processing power

The APS.RMS uses a 10-MHz MC68000. Measuring 5.25 in. high, 19 in. wide, and 24 in. long (13.34 x 48 x 61 cm), it contains 256 Kbytes of RAM, expandable to 4 Mbytes. In addition, the unit has 16 to 48 Kbytes of ROM and 5 to 112 Mbytes of formatted high performance, 30-ms disk storage. For disk backup, the workstation offers a choice of 5-Mbyte removable hard disk cartridge or quarter-inch streaming tape with up to 60-Mbyte capacity. Four serial ports and one compatible parallel printer port are included. Regulus and C are also covered in the $9950 base price. **Alcyon Corp,** 8716 Production Ave, San Diego, CA 92121.
Circle 269

Networked personal computer meshes with 3270 users

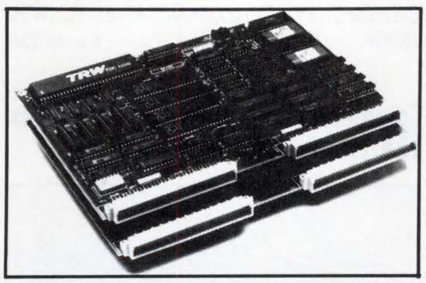
In addition to providing individualized personal computing, the Hero creates an intelligent workstation cluster at the department level. Super 21 interconnects the workstations and other terminals in LANs while Intelligent 3270 tailors the interaction between local and host applications. User-written programs in the terminal systems retrieve data from the host for local processing, store or display data at the terminal, then return it to the mainframe to update the central data base. **Mohawk Data Sciences,** 7 Century Dr, Parsippany, NJ 07054. **Circle 270**

Virtual memory system contains capacity of 32 bits

The Cerebra system is based on the NS16032 micro and runs the Genix system complete with demand-paged virtual memory. The system uses the Multibus for peripheral configurations. Features include 8 Kbytes of 45-ns cache memory, 2 Mbytes of main memory, 84 Mbytes of disk storage, 16 lines of intelligent serial controller, and a backup. A power outage protection system allows 10 to 15 min for shutdown if power fails. Shutdowns and restarts are automatic. Cost is $36,895. **Unidot Systems,** 602 Park Point Dr, Golden, CO 80401.
Circle 271

Mini-array processor competes with rackmounted versions

Fixed point, VMEbus-compatible VAP-64 achieves 10 million operations/s. The processor contains two boards; one houses the array processor and control circuitry, while the other stores 32 Kwords of high speed dual-port RAM. Using 200-ns cycle time RAM enhances system throughput and simplifies system software because each board is independent of the other. This cache memory configuration removes temporary data storage, that in turn eliminates DMA overhead. Price of the array processor board is $2900 and the memory board is $1800. **DSP System Corp,** 1081 N Shepard, M/S-E, Anaheim, CA 92806.



Circle 272

Computer system provides Winchester variety

The system 4000 contains either 160-, 300-, 500-, or 800-Mbyte fixed Winchester and 80-Mbyte magnetic tape drive backup. It offers total emulation of RSTS/E, RSXIIM, VMS, Unix, and TSX and a memory capacity ranging from 256 Kbytes to 8 Mbytes. It is compatible with Micro 11, 11/23 Plus, 11/24/44/73, and VAX. Additional features include a port serial interface for 64 terminals, peripheral bus mapping module, and 18- and 22-bit LSI-11 backplane handling old and new controllers. The system runs DEC diagnostics. **Unitronix Corp,** 197 Meister Ave, Somerville, NJ 08876.
Circle 273

Graphics engine transforms images in real time

Attached to a host processor, WTE 7000 accepts unsorted bicubic patches from the host and returns pixels to any conventional frame buffer. The unit solves the ambigous wireframe image problem by displaying objects as shaded images. The 32-bit floating point chip and tiling chips can process objects composed of 100 bicubic patches and do complete transformation, perspective division, light modeling, and clipping and shading on a 1280 x 1024 color raster station in less than 5 s. In quantities of one to nine, the graphics engine is priced at $70,000. **Weitek,** 301 Mercury Dr, Sunnyvale, CA 94086.
Circle 274

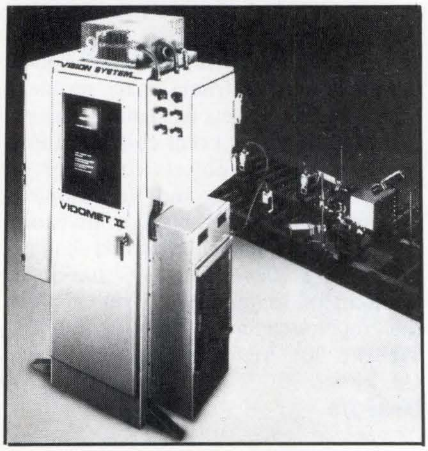
Workstation node integrates floating point unit

The 32-bit DN320 features 1.5 Mbytes of tightly coupled main memory, windows for 25 concurrent processes, and 16 Mbytes of virtual address space per process. A 16-in. monochromatic display offers a 1024 x 800-pixel resolution, bitmapped graphics, and connections to a LAN. In addition to the standard arithmetic functions, the unit performs trig and transcendental functions. Also available are disks featuring Winchester technology. The 70-Mbyte version has a random access seek time of 45 ms and average rotational latency of 8 ms. The DN320 is priced at $23,400 and the disk is $12,800. **Apollo Computer Inc,** 15 Elizabeth Dr, Chelmsford, MA 01824.
Circle 275

Unix-based computer system suited for computation-intensive applications

The Uniqorn uses an enhanced Unix System III and offers PDP-11/44 class performance. It features the LSI-11/73 CPU module with 1-Mbyte main memory (expandable to 4 Mbytes), 4 asynchronous ports, 32 Mbytes of fixed disk, and 10-Mbytes removable cartridge storage. Software for the Uniqorn includes unify relation database/application generator, word processing, virtual memory spreadsheet, and Basic. Prices start at $22,675. **Uniq Computer Corp,** 28 S Water St, Batavia, IL 60510.
Circle 276

Machine vision system performs demanding gray-scale analysis



Featuring a 640 x 485 matrix array, the Vidomet IIE is capable of 256 levels of contrast. Its image processor can operate at the high speed data handling rates necessary for current online inspection tasks. Up to 32 separate cameras, either solid state or Vidicon type, can connect to a single system. Applications include line gauging of dimensional measurements, parts identification, or feature verification at production line speeds. **Penn Video Inc,** 929 Sweitzer Ave, Akron, OH 44311. **Circle 277**

Motion controller applies to dc servo/stepping motors

For two-axis, point-to-point or linear interpolation applications, the Unidex III stores 99 randomly accessible programs. The unit includes a set of motion control commands, four programmable inputs, eight programmable outputs, and five operating modes. Front-panel controls include keyboard, axis-tracking displays, and alphanumeric display. Standard remote interfaces, IEEE 488, RS-232-C, and RS-422 can be daisy chained. Single-quantity price is $2250. **Aerotech, Inc,** 101 Zeta Dr, Pittsburgh, PA 15238. **Circle 278**

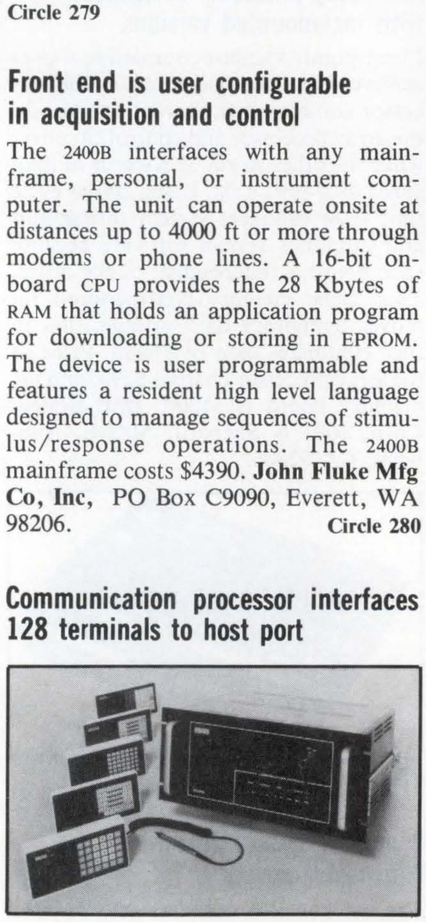
Programmable controller runs with 512 I/O points

The K2E provides sequence instructions such as shift, jump, pulse, and master control for complex process handling. Each controller accepts eight I/O modules, and additional modules control seven KOE controllers or three K2Es. I/O modules have a range of input voltages including 110 Vac, 220 Vac, and 24 Vdc, in increments of 16 and 32. Output voltages are 22 Vac, 24 Vdc, and 48 Vdc, in increments of 16 and 32. Base unit has memory for 2000 program steps and EPROM comes in 2-Kbyte blocks. **Mitsubishi Electric Sales America, Inc, Industrial Products Div,** 3030 E Victoria St, Rancho Dominguez, CA 90221. **Circle 279**

Front end is user configurable in acquisition and control

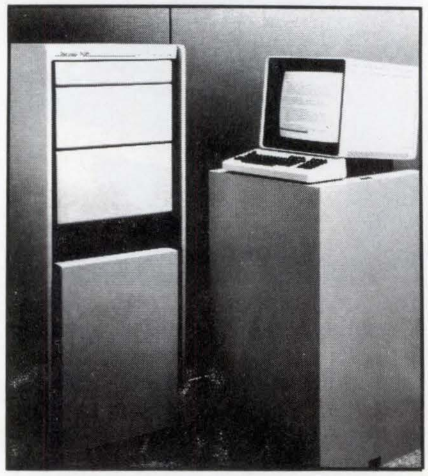
The 2400B interfaces with any mainframe, personal, or instrument computer. The unit can operate onsite at distances up to 4000 ft or more through modems or phone lines. A 16-bit onboard CPU provides the 28 Kbytes of RAM that holds an application program for downloading or storing in EPROM. The device is user programmable and features a resident high level language designed to manage sequences of stimulus/response operations. The 2400B mainframe costs $4390. **John Fluke Mfg Co, Inc,** PO Box C9090, Everett, WA 98206. **Circle 280**

Communication processor interfaces 128 terminals to host port



The TMC900 frontend processor together with Microterminals and associated software compose an integrated data collection system. The processor performs basic factory data collection tasks of terminal polling, local data validation, error recovery, and transaction processing. The host can download definitions for up to 100 transactions, each with 10 prompt/reply editing specifications. Protocol is command/response format with handshaking. Unit price is $7500. **Burr-Brown, Data Acquisition and Control Systems Div,** 3631 E 44th St, Tucson, AZ 85713. **Circle 281**

Modular approach to networking provides test and repair



A multifunction computer resource for factory data collection, the 700 Net workstation is based on a 68010 with 4 Mbytes of memory. The 700 uses standard Ethernet and RS-232 communication lines. Application packages include Factory Observer, Program Manager, Producer2, and Paperless Repair System. Factory Observer collects and analyzes factory data. Program Manager is a test program and retrieval system. Producer2 is an auto-test program generator, while the repair system electronically links testers to the repair station. Average configuration sells for $100,000. **Zehntel,** PO Box 8016, Walnut Creek, CA 94596. **Circle 282**

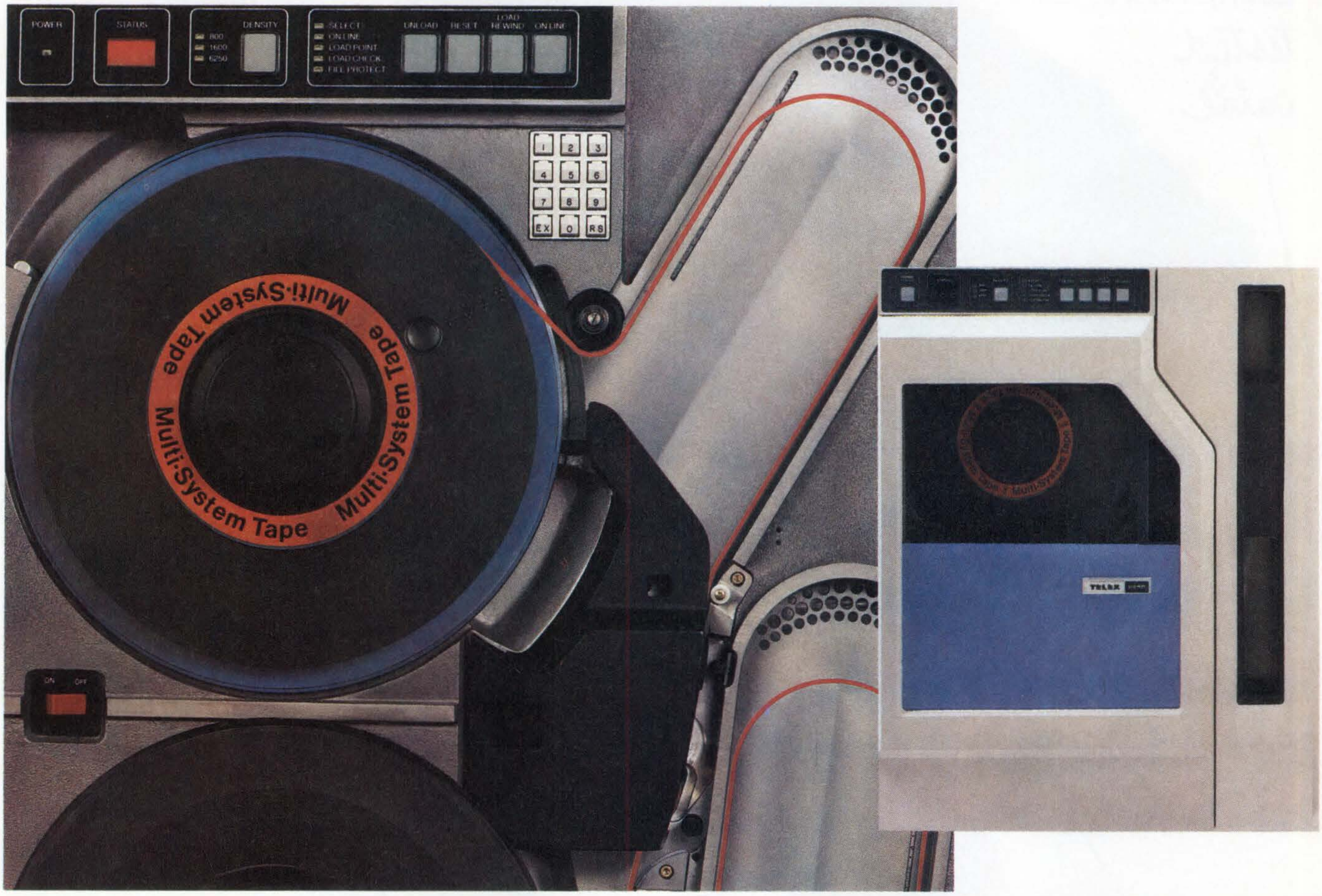
Video image processor uses image recognition

The KR95 system consists of a controller, up to four video cameras, illuminator, and monitor. The system uses an image recognition technique to read and digitize tiny identification numbers on 3-in. or larger silicon wafers in real time. It permits lot tracking and tracing throughout the complete semiconductor processing cycle. Reading is at a 25-char/s rate. Designed around a Z80, memory consists of 16 Kbytes of PROM, 16 to 48 Kbytes of RAM, and 1-Kbyte scratchpad. In single units with one camera, the wafer identification system is priced at $14,654. **Key Image Systems Inc,** 20100 Plummer St, Chatsworth, CA 91311. **Circle 283**

TELEX®

The new Telex 9250 tape subsystem

Finally! Full-Performance GCR Made Affordable. Telex Shamrock



It took Telex to introduce a GCR subsystem with all the performance, all the reliability of larger subsystems — and make it affordable for minicomputer and mid-range mainframe manufacturers.

The Telex 9250 GCR tape drive is the first 50 ips unit to appreciably lower the cost of GCR without sacrificing performance. Advanced LSI gate array technology and vacuum column design offer advantages like low cost, low power and low noise (before offered only on old tension arm systems) — plus all the performance that only vacuum column technology can deliver, including . . .

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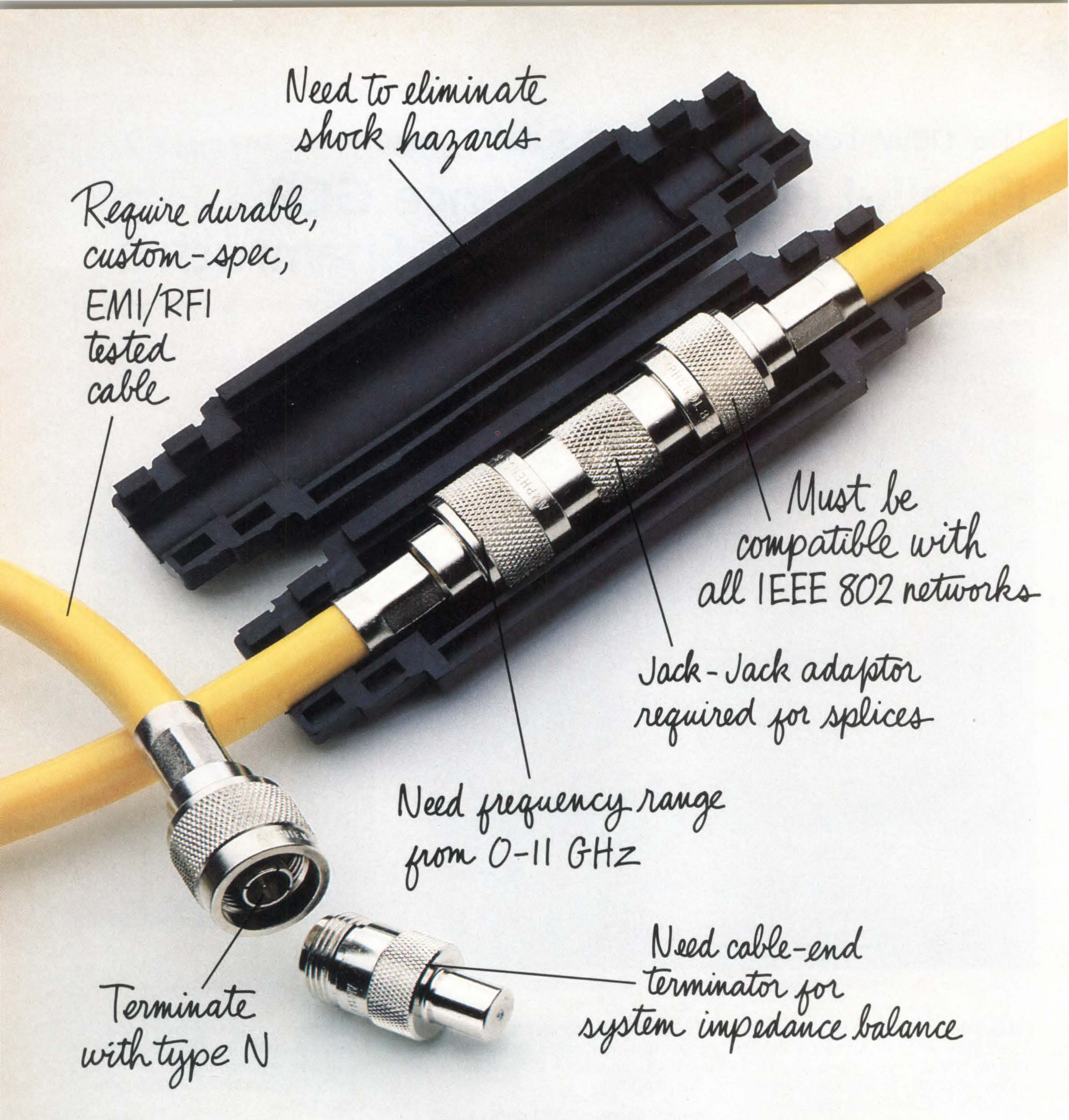
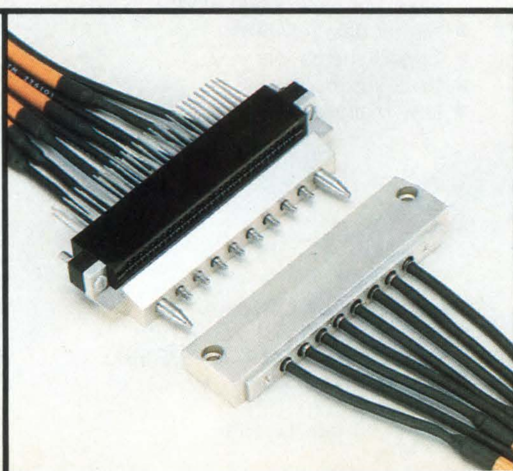
CIRCLE 111

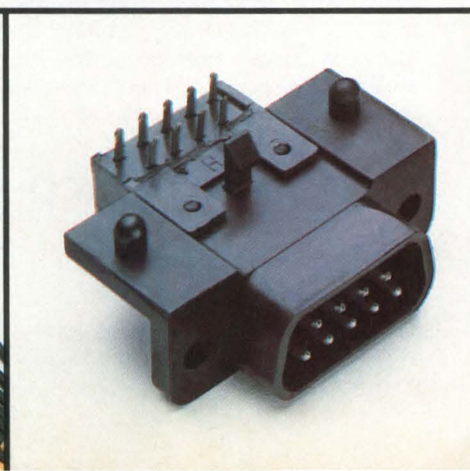


PC Circular Connector

PC Fibre Optic Connector



Plastic D-Subminiature Connector



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When it comes to meeting the rigid interconnection requirements of business equipment, there's hardly anything we won't do. Because at Amphenol, we know that the best design is often a custom design.

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We developed a low-cost, all plastic D-subminiature to meet the need for reliable connections in video games and home computers. The connector, with selectively-plated, pre-aligned and stiffened contacts, snaps easily into a PC board and withstands rugged use.

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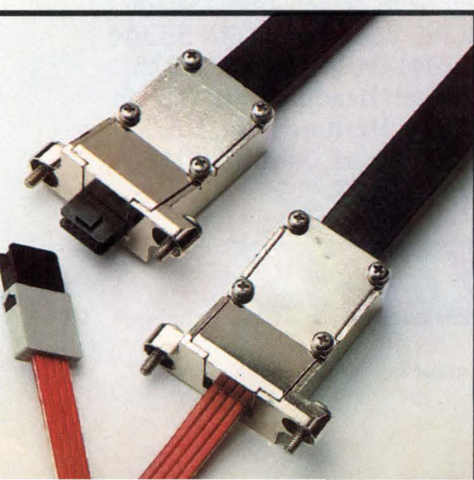
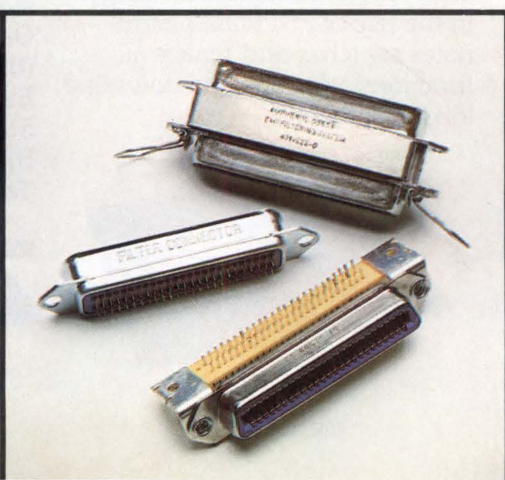
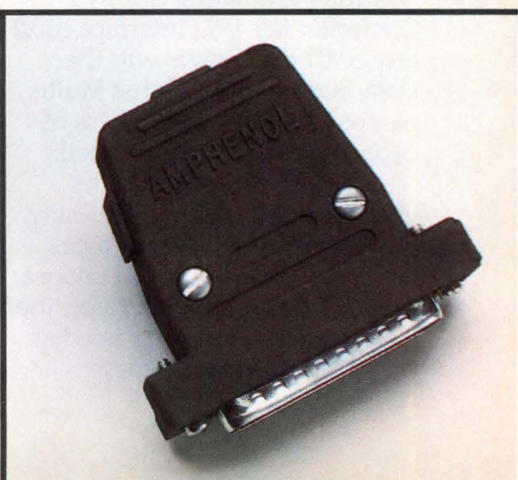


Filtered Ribbon Connectors



Shielded D-Subminiature Connector



Now it's easy for anyone to pick an SMD drive that works with DG's BMC.

Zetaco's new BMX-1 makes over 60 hard disk drives plug-compatible with your Eclipse/MV Series mini.

Our fully emulating BMX-1 Disk Controller lets you interface most any SMD disk drive with the Data General BMC (Burst Multiplexor Channel). Regardless of capacity. Regardless of speed.

No other disk controller gives you that kind of flexibility, that kind of unlimited choice. Only the BMX-1 lets you choose the disk drives that offer you the exact performance you need at the price you want to pay.

Zetaco's BMX-1 offers four disk drive connect ports with software configurable drive characteristics on a port by port basis. Breakthrough technology in the use of E^2-PROMS eliminates switches and makes all functions selectable via downline loaded software.

Like other Zetaco controllers, the BMX-1 offers complete FCC chassis compliance.

Get the complete BMX-1 story from Zetaco, 6850 Shady Oak Rd, Eden Prairie MN 55344. (612)941-9480. Telex 290975. European Headquarters: 9 High St, Tring, Hertfordshire, HP23 5AB, England. 044282 7011. Telex 827557.

ZETACO

Controller Div., Custom Systems Inc.

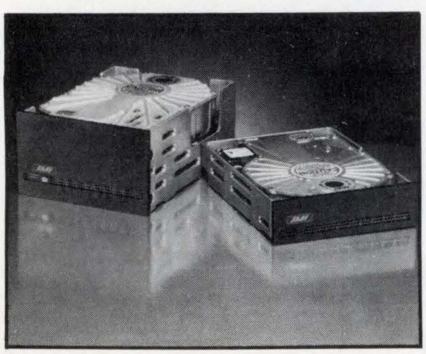
CIRCLE 113

Hard disk system works in development environment

The DataSafe-16 is a Winchester for Intel Intellec series II, III, and MDS-800 micro development systems. It provides 10 Mbytes of formatted storage and three directories. Based on a 5¼-in. drive, the system is compatible with ISIS-II operating system and has 78,336 available blocks. Blocks are allocated in three directories, F0, F1, and F2. Data transfer rate is 625 kbytes/s with an average access time of 85 ms. The Z80A micro-based controller includes 32-bit ECC with transparent 11-bit burst error correction. Cost is $6500. **Winchester Systems Inc,** 14 Laurel Hill, PO Box 545, Winchester, MA 01890.
Circle 284

Half-height Winchesters have access times of 85 ms with settling

The 2306H and 2312H have capacities of 6 and 12 Mbytes, respectively. Access is via a high speed closed loop stepper motor. Two-piece design with a rugged integral mount provides high shock resistance. Bezel-mounted LED shows self-test diagnostic results during power-up, while auto-power sequencing reduces starting currents and system cost in a multidrive system. **International Memories Inc,** 10381 Bandley Dr, Cupertino, CA 95014.



Circle 285

Micro floppy disk drives record at 140 tracks/in.

Using a standard 5¼-in. interface and 3¼-in. media, models 321 and 322 feature single-sided 500-Kbyte and double-sided 1-Mbyte storage capacities. Track-to-track access time is 6 ms and MTBF is 12,000 hours under typical usage. Major components include a direct drive spindle motor and a long life screw head-actuator mechanism. Drives are plug compatible with standard double-sided double-density 96-track/in., 5¼-in. drives. Media are formatted at 80 tracks/side. Model 321 and 322 cost $155 and $190, respectively. **Micro Peripherals, Inc** 9754 Deering Ave, Chatsworth, CA 91311.
Circle 286

Multibus cache memory is processor independent

Offering Multibus and iLBX users a low cost way to add fast memory to their systems, the cache board images the entire Multibus address space (16 Mbytes) through the iLBX extension to the Multibus. The access time on a hit is less than 100 ns. The memory will store the most recent 4 Kbytes of data accessed through the bus and provide a fast response time for subsequent accesses. When a cache miss occurs, the board automatically accesses the Multibus, updates the cache, and provides the data to the host. **Central Data Corp,** 1602 Newton Dr, Champaign, IL 61821.
Circle 287

Bubble memory VMEbus system builds in reliability

The VMI-1 allows VMEbus machines to use solid state mass storage when electromechanical media such as disk and tape are unsuitable. Storage based on nonvolatile magnetic bubble devices are unaffected by dust, smoke, and airborne dirt. In addition, bubbles consume less power than disk systems, eliminate periodic maintenance, and do not require an additional chassis or power supply. This system provides 256 Kbytes of storage on a single PC board that plugs directly into a VMEbus micro. Designed around a Z-80, the controller handles device formatting and control, and soft and hard error detection and correction. The 256-Kbyte version in quantities of 10 sells for $1799. **PC/M, Bubbl-tec Div, Inc,** 6800 Sierra Ct, Dublin, CA 94566.
Circle 288

Storage peripheral designed around bubble technology

The Bubble Drive provides either 256 or 512 Kbytes of non-volatile, high speed mass storage on a single card. It plugs into any I/O slot in the IBM-PC and functions as a floppy disk. The drive will retain all data without battery backup. It is immune to dust and dirt as well as extremes in temperature, humidity, shock, and vibration. The drive can be used in one of these modes: to store programs that are disk intensive, to store critical data, to store programs and data when speed and reliability are essential, and to store operating systems and files when environment precludes the use of mechanical drives. The 256-Kbyte version is $995, the 512-Kbyte version is $1495. **Hicomp,** 5016 148th Ave NE, Redmond, WA 98052.
Circle 289

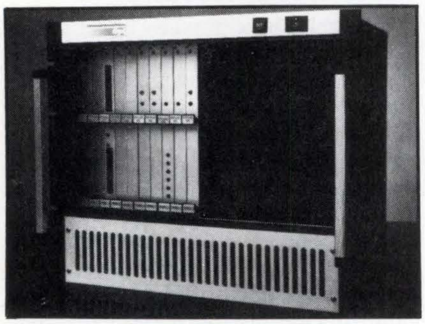
Disk cache accelerates RL02 drive performance

Unlike a RAM disk, the OR-86RLQ is an intelligent board that automatically caches data accessed by programs. The 600-Kbyte device for DEC's RL01/RL02 drives is totally transparent to the user and requires no operating system modification. Unlike caching schemes implemented in the operating systems, the board does not use system memory or CPU resources. It is compatible with any operating system. For data integrity, the board generates and checks parity, and computes and checks a CRC for each transferred data block. Price is $3300. **Origin, Inc,** 9136 Gibson St, Los Angeles, CA 90034.
Circle 290

Winchester subsystem offers 168 Mbytes for the PC

The 8-in. PC-8002-8 has fast data transfer rates and 20-ms average access times for maximum performance in network and file server applications. Available in a stackable PC-style desktop enclosure, the drive formatted with DOS 2.0 drivers, disk controller, integral power supply, and full documentation. It is compatible with Compaq, Victor 9000, Eagle PC, Columbia, and other PC compatibles. Available for immediate delivery, the drive is priced at $9000 in quantity. **National Memory Systems,** 355 Earhary Way, Livermore, CA 94550.
Circle 291

Eurocard modules offer VMEbus links and high performance



Nine modules based on the 233- x 220-mm format include seven VMEbus cards, a 19-in. rackmountable system chassis, and a Unix-based development system. Among the seven cards are two high performance 68000-based cards, a 512-Kbyte dual-port memory card with a 10-MHz refresh port, a universal byte-wide memory card, and a serial and parallel I/O card. In addition, a Z80A-based intelligent disk controller and a bit-mapped color graphics card with 256 Kbytes of memory and a high performance graphics controller are available. Prices range from $1200 to $5000. **Dy-4 Systems Inc,** 888 Lady Ellen Pl, Ottawa, Ontario, Canada K1Z 5M1.
Circle 292

Operating systems processor handles high volume

The single-chip S83 OS processor system has a core Z80 CPU and onchip 64-Kbit ROM. The ROM can be programmed with proprietary code or a standard software version can be purchased. The chip's control, address, and data signals are functionally equivalent to the original Z80 so it is hardware compatible with all Z80 peripheral chips. Additional logic allows the processor to directly connect to 64-Kbit dynamic RAMs. Pricing is approximately $32 in quantities of 100 (plastic packages). **American Microsystems, Inc,** 3800 Homestead Rd, Santa Clara, CA 95051.
Circle 293

Single-chip microcomputer features CMOS and 8 bits

The HD6305Y0 is both software and pin compatible with the HD6305X. The micro features a 7872-byte ROM and a 256-byte RAM. The chip has 32 I/O ports, 7 input ports, 16 output ports, clock-synchronized serial communication interface circuit, and 8-bit timer/counter with 7-bit prescaler. In normal operation at 1 MHz, it consumes 25 mW. In the wait mode, power consumption is reduced to 10 mW, with other modes available to further reduce power consumption. The chip comes in 64-pin packages. Its minimum instruction execution cycle time is 1 μs. **Hitachi America, Ltd,** 1800 Bering Dr, San Jose, CA 95112.
Circle 294

Intel 80188 processor enhances STD-bus capability

The ZT 8814/8815 single-board computers use the 80188 containing two DMA channels, an interrupt controller, timers, clock, peripheral/memory chip select logic, and a wait-state generator. The boards provide 5 byte-wide memory sockets. One socket accepts a debug monitor that can be replaced with a user PROM of up to 32 Kbytes. Other sockets accept byte-wide RAM or ROM devices. Up to 1 Mbyte of memory is directly addressable. The boards also feature an onboard iSBX I/O bus connector that will take any one of approximately 60 plug-in modules. Prices start at $650. **Ziatech Corp,** 3433 Roberto Ct, San Luis Obispo, CA 93401.
Circle 295

Integrated Multibus system housed in desktop cabinet or drawer

The PM200 features a PM68D CPU that has 256 Kbytes of no-wait state memory with a 768-Kbyte extension. CPU includes dual-ported memory, memory management, and mailbox interrupts. It has one or more 20-Mbyte Winchesters, a 1-Mbyte floppy, and an optional 40-Mbyte streaming cartridge tape. Unisoft Unix is part of the system and has full-screen editors, text formatters, electronic mail, and the C language compiler with related 68000 assembler support. **Pacific Microcomputers, Inc,** 119 Aberdeen Dr, Cardiff, CA 92007.
Circle 296

Peripheral computer plugs into existing S-100 computers

The PDP-11-compatible PC11 is designed for S-100-based computer systems. The unit is T11 micro based with 64 Kbytes of onboard memory. It uses host processor and peripherals for I/O. The package includes the RT-11 operating system and an I/O interface program that supports console, printer, and dual disk drives. It will not affect the S-100 computer's normal operation. Software is written in 8080 assembly language and runs CP/M. Price is $795. **Abacus Technology Systems, Inc,** 8343 Carvel, Houston, TX 77036.
Circle 297

Monoboard micro combines virtual memory and memory management

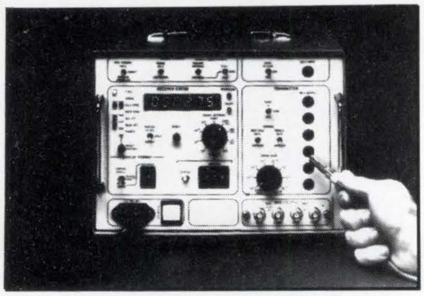
Incorporating an MC68010 MPU and an MC68451 MMU, the VM03 is Versabus compatible. Features include I/O channel interface for configuration of offboard resources, 256 Kbytes of dynamic RAM with parity check, and two 28-pin sockets for ROM/EPROM devices. Dual-port RAM controller provides true shared memory access. Two multiprotocol serial I/O ports with an RS-232-C interface handle modems or terminals. Realtime software supports the board. In quantities of one to five, price is $3900. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.
Circle 298

Powerful 16/32-bit CPU meets MIL-STD-883 Class B

The MKB68000 has a 32-bit architecture with upward migration paths. This makes it suitable for weapons, control, navigation, digital signal processing, and multiuser minicomputer replacement. Features include 32-bit data and address registers with a 16-Mbyte direct-addressing range and high data throughput. In addition, the chip has 14 addressing modes for efficient programming, 56 powerful instruction types, memory-mapped I/O, and support of five basic data types. Data types range from individual bits to longword operation. The 6-MHz device is packaged in a 64-pin cerDIP priced at $97.50 each in 1000s. **Mostek Corp,** 1215 W Crosby Rd, Carrollton, TX 75006.
Circle 299

Talk to the editor
Have you written to the editor lately? We're waiting to hear from you.

Transmission test set contains receiver and transmitter



The portable model 275A tests complete performance of T3 coaxial cable as well as microwave, satellite, and fiber optic transmission systems. A single input jack and six independent bipolar outputs load M34 multiplexers and digital radio equipment. The set permits three test methods: test intervals selectable in bit blocks ranging from 10^8 to 10^{11} bits, time blocks with a timed-test interval ranging from 1 s through 999 min, and continuous count on a nontimed basis. Cost is $5650. **Bowmar/Ali, Inc,** 351 Main St, PO Box 10, Acton, MA 01720.
Circle 300

Local area network assumes general purposes

Flexible LAN comes in either a broadband or baseband version and supports hybrid LANs. Hybrids combine high capacity broadband trunks with lower capacity baseband feeders. The system is also compatible with the Net/One LAN from Ungermann-Bass. Support for data terminal device includes asynchronous and synchronous serial and parallel, 32-bit parallel, and IEEE 488. Providing high speed digital bandwidth at low error rates, in broadband version the LAN accommodates other types of communication. Prices range between $450 and $750 per port. **Codex Corp, sub of Motorola, Inc,** 20 Cabot Blvd, Mansfield, MA 02048.
Circle 301

Improved price/performance are gains in communication processors

The 3690 models A8 to K8 are configured with a minimum of 512 Kbytes of memory, expandable to 4 Mbytes of memory. Up to 512 communication lines and up to 8 channel-attached hosts can be simultaneously supported. The units can be configured for standalone, front-end, or remote communication environments. Software includes system control and two operating system versions. Improved packaging produces greater line and host connectivity and additional logic module space. **NCR Comten, Inc,** 2700 Snelling Ave N, St. Paul, MN 55113.
Circle 302

Modemless networks transmit voice/data simultaneously

Both the DCS-2A and -2B offer a 0- to 9600-bit/s data rate, asynchronous, bit, or serial operation, and a full-duplex operating mode. Station units transmit at 36 kHz space, 40 kHz mark, and receive at 72 kHz space, 80 kHz mark. Dedicated data links can be established from a centralized data processing facility to any terminal equipment. Terminal types can be mixed, operated at different data rates, and located at most any telephone location within 5000 cable ft of switching equipment. **Teletone Corp,** 10801 120th Ave NE, PO Box 657, Kirkland, WA 98033.
Circle 303

Digital encryption system operates at up to 3.152 Mbits/s

Model CD5800A uses the data encryption standard. It features an electronic keyloader, separate master and working keys, battery backup for key retention, up to 16 standby keys, and automatic key change. Alarm reporting circuits allow access to 11 status alarm outputs. Self diagnostics, system and local loop test modes, and bypass operation assist maintenance. **California Microwave, Inc,** 990 Almanor Ave, Sunnyvale, CA 94086.
Circle 304

Auto-dialing modem uses two custom CMOS ICs

Popcom model X100 is a 1200-bit/s modem with AT&T 212 compatible operation. A switchable 20-pole filter provides tone sensing of dial tone, busy tone, remote ring, and voice. The modem can sense when the local telephone handset is lifted so it switches between voice and data operation on the same call. The integral smart RS-232 interface senses the transmit signal on pin 2 or 3 and switches the necessary connections. Price is $475. **Prentice Corp,** 266 Caspian Dr, PO Box 3544, Sunnyvale, CA 94088.
Circle 305

Full-duplex modem is microprocessor based

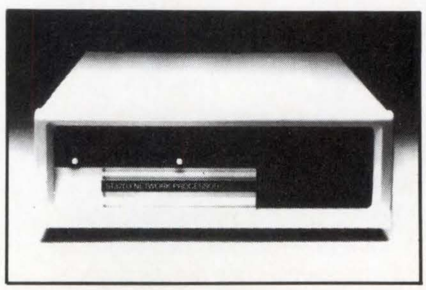
The R2424 operates over the DDD network or two-wire private lines. The modem operates synchronously or character asynchronously at speeds of 2400 or 1200 bits/s. It can perform tests like analog and digital loopback, remote digital loopback, local self-test, and end-to-end self-test. Eleven front-panel LEDs monitor the EIA interface status, test status, error detection, and incoming calls. **Rixon Inc,** 2120 Industrial Pkwy, Silver Spring, MD 20904.
Circle 306

Communication processor emulates IBM systems

The MC-80/602 converts a general KSR device or asynchronous ASCII host into a full-function terminal. The terminals, in turn, communicate with the IBM host using the EBCDIC binary synchronous communication protocol. The processor performs full-screen mapping; data displayed on the KSR terminals will be the same as the 3277/78 display station, with virtual screen sizes of 480, 960, and 1920 chars. The standalone unit has 16 Kbytes of ROM, 16 Kbytes of RAM, and one serial communication port. Price is $1650. **Innovative Electronics, Inc,** 4714 NW 165th St, Miami, FL 33014.
Circle 307

Dynamic gateway improves intercomputer communications

The ST3703 network processor uses SNA, including link-level efficiency, multi-host networks, and IBM network management. Up to 12 devices can be channeled through the unit to save line charges. The protocol processor acts as an SNA gateway, not a device specific emulator. It offers full architectural implementation of SNA for a physical unit type 2, coupled with a host support program and downline multifunction capability. **Office of the Australian Trade Commissioner,** 636 Fifth Ave, New York, NY 10111.



Circle 308

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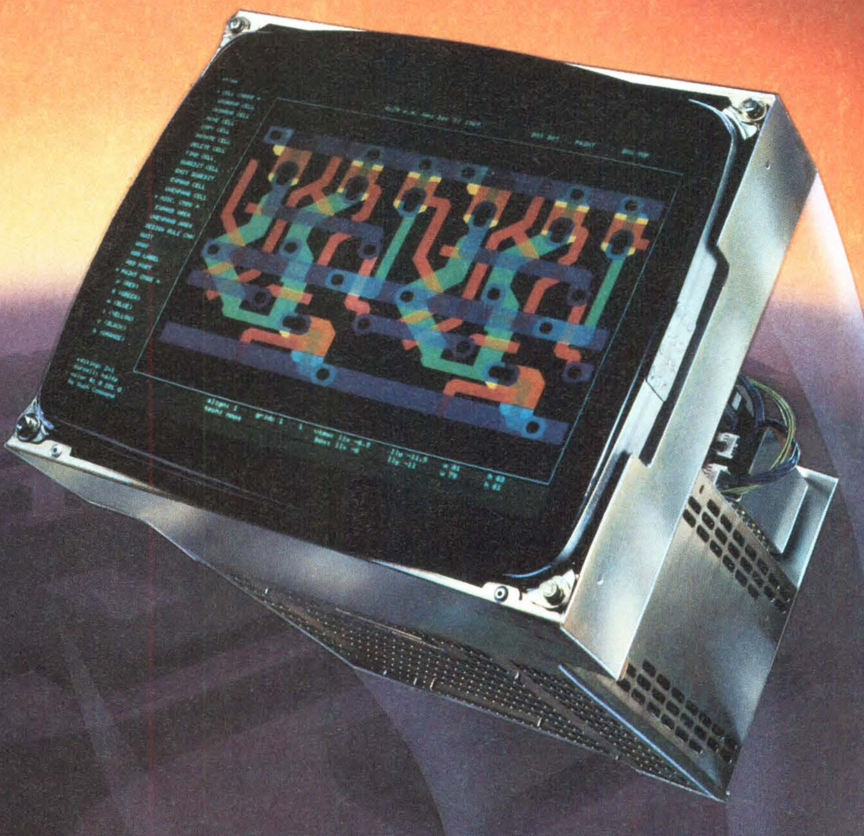

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The HM-4619 delivers flicker-free images with 1280 × 1024 resolution at 60 Hz. Hitachi tube technology leadership has created a new in-line gun delivering high brightness with sharper focus. All of this is enhanced by our Digital Dynamic Convergence™ of 0.1/0.3 mm.

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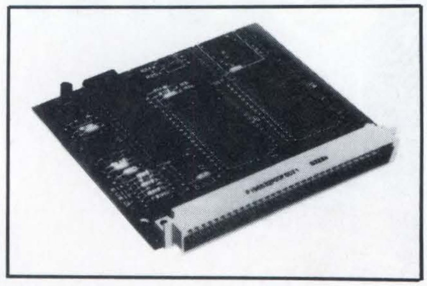
CIRCLE 115

Communication device links personal computers

Microprocessor-based, the Mini-Exchange enables DEC's small computers to transfer information in file or document format. The device also allows sharing of I/O devices such as printers, modems, or multiplexers. It features a 128-Kbyte read/write data memory, power up and self-test diagnostics, and external loop back test. Up to eight personal computers and I/O devices link through ports that are compliant with EIA RS-232/432 standards. Speeds range from 300 to 19,200 bits/s. Price is $895. **Digital Equipment Corp,** 10 Main St, Maynard, MA 01754.
Circle 309

Modem cards are based on proprietary VLSI three-chip sets



The R2424 supports full-duplex communications at 2400 bits/s and meets CITT V.22 bis and V.22 A, B, C standards. The R1212 transfers data at up to 1200 bits/s and meets the same standards. Both cards use a micro bus interface and an RS-232 interface. Auto-answer and automatic pulse-dialing functions are available. The boards fit Eurocard racks and associated 64-pin DIN connectors. They operate from 5- and 12-V supplies and consume 3 W. Prices, in 1000 piece quantities, are $123 for the 1212 and $166 for the 2424. **Rockwell International Corp, Semiconductor Products Div,** 4311 Jamboree Rd, PO Box C, Newport Beach, CA 92660.
Circle 310

Two-chip set provides both modem and filter

Used in Bell 103/113 frequency shift keying applications, the STC9472C and 82C are modem and filter chips, respectively. The modem chip includes both half- and full-duplex modes, built in self test, and TTL-compatible interface. It runs at 300 baud. The filter is a switched capacitance type, handling both the transmit and receive modes. It includes an adjustable limiter, adjustable hysteresis, and adjustable transmit and receive gain. Price for the two-part set is $16 in quantities of 100. **S MOS Systems, Inc,** 50 W Brokaw Rd, San Jose, CA 95110.
Circle 311

June Previews
Watch for two special articles—local area networks on June 1, system testing on June 15

 CIRCLE 116

Communication processor has applications in switching

The CP9000 series II uses a multiprocessor architecture, capable of supporting several thousand communication lines. It features 1-for-N redundancy of its components for fault-tolerant operation and security options to ensure data and user access integrity. Software includes a complete X.25 packet switching network encompassing routing, statistics, billing, and extensive network management and control features. **M/A-COM DCC, Inc**, 11717 Exploration Ln, Germantown, MD 20874.
Circle 312

Satellite communication connects to HP computers

Operating with the HP 3000 minicomputer, the Vitalink system functions between a satellite and an earth station located on the customer's property. Applications are for geographically dispersed organizations that quickly transfer files and information for decentralized inventory control, financial management, and CAD/CAM. A distributed system network approach lets the earth station connect directly to the computer's I/O and run HP software. Transmission rates range from 4.8 to 56 kbits/s. Equipment and installation is $120,000 with a monthly charge of $1800. **Vitalink Communications Corp**, 1350 Charleston Rd, Mountain View, CA 94043.
Circle 313

Protocol converter allows emulation of 3270 devices

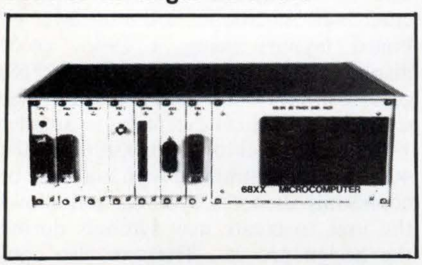
Combining protocol conversion, line concentration, and terminal emulation, the 362 gives ASCII terminals and small computers 3270 emulation capability. The unit features emulation of IBM 3274 controller operating with SNA/SDLC protocol, 19.2-kbit host and terminal support, split speed RS-232-C or RS-422 interfaces, and table-driven configuration control. The standard configuration contains one host port and 16 terminal ports. The price is $9800. **ICOT Corp**, 830 Maude Ave, PO Box 7248, Mountain View, CA 94039.
Circle 314

Expansion module puts voice channels on system

Designed for use with the Link/1 facilities management system, the voice digitizing option allows analog voice input to be multiplexed as part of a data stream. It passes over a 1.544-Mbit/s link and uses a form of continuously variable slope delta modulation at 32 kbits/s. The voice option is offered in multiples of four channels on a board that occupies one slot in the Link/1 backplane. Multiplexed channels of digital voice appear to the PBXs as ordinary wire tie lines. Cost is $3550 for the first unit. **Timeplex, Inc**, 400 Chestnut Ridge Rd, Woodcliff Lake, NJ 07675.
Circle 315

TEST & DEVELOPMENT

Modular development system doubles as target hardware



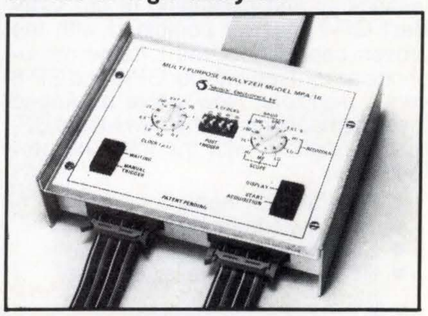
Based on 3U Eurocards, the MC6809 features a 2-MHz 68B09 processor with extended addressing to 1 Mbyte. Memory includes 56 Kbytes of static CMOS battery-backed memory with 2764 EPROM capability. A 5/8-in. single, double-sided disk controller has digital phase-locked loop data separator and individual read/write precompensation. The twin double sided (80 tracks/side), 3-ms stepping disk drive offers 725 kbytes of formatted storage/drive. A complete software library comes with the system. **Windrush Micro Systems Ltd**, Worstead Laboratories, North Walsham, Norfolk, England.
Circle 316

Advanced graphics system boards designed for PC and compatibles

The multiported memory design of the Revolution graphics boards supplements the NEC 7220 16-bit graphics coprocessor. The display is memory mapped into the PC's address space so the 8088 can access display memory at all times. Two modes are available; the pixel mode for modification of a single pixel color value across 8-bit planes of RAM and plane mode for updating 8 pixels at a time in 1-bit plane. With a single card, a display resolution of 512 x 512 can be obtained with 256 simultaneous colors selected from a palette of over 16 million colors. Prices start at $945. **Number Nine**, 691 Concord Ave, Cambridge, MA 02138.
Circle 317

Let's hear from you
We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

Troubleshooting system converts devices to logic analyzers



The MPA-16 allows scopes, graphics recorders, or microcomputers to function as logic analyzers. It displays up to 16 digital input channels simultaneously on a scope without flicker, produces hard copy on a recorder, and transfers logic information to a micro. Memory is 1024 x 16 bits with a 55-ns time. Unit can also provide remote diagnostics via telephone. An internal clock carries asynchronous operation up to 20 MHz. Price is $990. **Sensor Electronics Inc**, 105 Fairway Terrace, Mt Laurel, NJ 08504.
Circle 318

Measurement and control system features fast processing

The 2452 combines an instrument controller and an intelligent computer front end. The 16-bit, micro-based controller has a touch-sensitive CRT and dot addressable graphics. With a 16-bit onboard CPU the front end controls measurement and I/O cards. It takes care of digital and analog measurements, signal conditioning, output controlling, and decision making. The controller provides computing power, mass storage via floppy disk, and advanced graphics. Software allows 10-channel data acquisition functions. Base system is $15,000 with a typical configuration averaging $20,000. **John Fluke Mfg Co, Inc**, PO Box C9090, Everett, WA 98206.

Circle 319

Solid modeling computer hardware removes hidden lines

Hardware compatibility allows Syntha-Vision to run on existing CADAM hardware—including IBM 3250 graphics terminals—with no additional hardware. Output lets users automatically create any view desired, including planar or nonplanar cross sections from any angle. Interface enables the output to be passed to the CADAM, which in turn processes the data as if originally produced by CADAM. **Mathematical Applications Group, Inc**, 3 Westchester Plaza, Elmsford, NY 10523. **Circle 320**

Color graphics system meets CAD/CAM applications

The G-6200 color raster system uses the Genco operating system for graphics control. The basic configuration provides a 1536 x 1024 bit-mapped refresh memory for the selection of 16 colors from a palette of over 16 million hues. With optional memory cards, total color selections are 4096 with additional overlays for graphics and imaging. The operating system permits a multilevel display list with 32-bit precision to be stored locally and manipulated with full 3-D modeling transforms. Single unit price is $23,950. **Genisco Computers Corp,** 3545 Cadillac Ave, Costa Mesa, CA 92626.

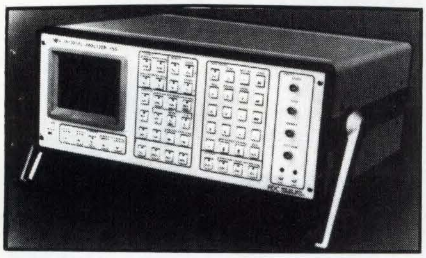
Circle 321

Schematic capture and layout stations use IBM PC XT

The CAD 2000 system allows designers to enter logic schematics and multilayer PC board layouts using a 19-in. color display. High resolution (1024 x 768) color graphics is a standard feature. The CAD 1000 is identical except for its smaller 13-in. screen and lower resolution (640 x 400). Editor is supplied with a library of commonly used TTL symbols and allows the user to create new symbols during the design process. The 2000 also contains a netlist extractor for interface to tools such as simulators. The 1000 costs $13,500; the 2000 is $23,500. **Chancellor Computer Corp,** 1731 Embarcadero Rd, Palo Alto, CA 94303.

Circle 322

Analyzer helps integrate drives with controllers and hosts



The time interval analyzer, model 150, works like a passive bus analyzer to capture bit-shift jitter, reduce it in hardware, and display it in histogram form. First-generation histograms are displayed, or test data may be further reduced in two levels. The analyzer connects directly to the drive under test. The device can be used in evaluation of any kind of high speed data stream, regardless of encoding method. It combines functions of a precision (±1 ns) time interval counter, event counter, high speed RAM, and proprietary software. Price is $15,000. **Applied Data Communications,** 14272 Chambers Rd, Tustin, CA 92680.
Circle 323

Test diskette comes in format for 3¼-in. drives

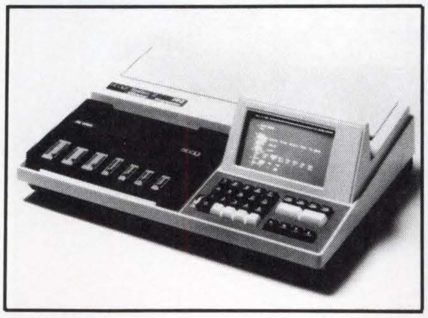
The analog alignment diskette (AAD) is a standard diskette with cat's eye for radial alignment. It allows checking of index timing, head read resolution, and skew error of the head positioning mechanism. Currently, only a one-sided version is available, but the company plans to make the 140 track/in. diskette available in two-sided format. The diskette is available directly from the company at a cost of $25 in single unit quantities. **Dysan Corp,** 5201 Patrick Henry Dr, Santa Clara, CA 95050.
Circle 324

Hardware/software converts PC to gate array design terminal

In addition to design software, the Unicad-1 includes the ISO 3/5 library of macrocells, a high resolution printer, and a graphics driver board. It also has a mouse, terminal emulation and communication package, and operating manuals. With the system, a user can develop a logic design, capture it, and convert it to a network listing. The listing can then be transmitted via modem links to a VAX system. After simulations, the net list is entered back into the system where macrocells are automatically placed and interconnected, rules checked, and test program development is completed. Package costs $7000. **Universal Semiconductor Inc,** 1925 Zanker Rd, San Jose, CA 95112.
Circle 325

Universal programmer senses each pin under variable loads

The PPZ system uses low cost plug-in modules that accommodate high level editing for logic device parameter programming and testing, Boolean entry, and memory mapping. The system's enhanced video facilities feature 80-col x 20-row alphanumeric display with reverse and flashing attributes. It can also measure small current flow to locate a poor contact before programming. The system is priced at $3975. **Stag Microsystems Inc,** 528-5 Weddell Dr, Sunnyvale, CA 94086.



Circle 326

Computer aided engineering design system integrates simulator

The addition of HILO-2 high speed universal design simulator to Metheus' CAE system provides hierarchical design simulation. The ability to analyze and verify designs at each development stage reduces the number of design iterations and improves reliability. HILO-2's concurrent hardware description language supports a set of gate-level primitive elements for various technologies. This capability also allows event creation and logic circuit analysis for full simulation of VLSI devices. **Metheus Corp,** PO Box 1049, Hillsboro, OR 97123.
Circle 327

Color graphics workstation has resident 5¼-in. Winchester and floppy

The Colorware System 11/10 includes a color terminal, a keyboard, color monitor, and an LSI-11 CPU. Model 1024 terminal offers a 1024 x 768 viewable resolution. The keyboard detaches VT-100 style. The CPU comes with memory management. The graphics processor is compatible with Tektronix Plot 10 software. Operating systems include RT-11 and RSX-11M as well as Venix. Graphic input devices include an optical mouse and an 11- x 11-in. data tablet. Single-quantity price is $25,995. **Advanced Electronic Design, Inc,** 440 Potrero Ave, Sunnyvale, CA 94086.
Circle 328

Universal programmer is slave expandable for gang programming

The Z-1000B handles PROM/LOGIC/CPU programs, NMOS and CMOS EPROMS, EEPROMS, bipolar PROMS, logic devices, and Intel's 87XX micros. The unit is software controlled, eliminating pinout adapters; all devices are keystroke selected. The device features an expandable RAM, and a 16-char alphanumeric display with fast programming algorithms for EPROMS. When programming slaves, each will generate three sets of four different programs simultaneously. Cost is $5500. **Sunrise Electronics, Inc,** 524 S Vermont Ave, Glendora, CA 91740. **Circle 329**

Data acquisition and control system displays test data

As a high speed front end or standalone, the model 10K8 is compatible with any RS-232 or IEEE 488 computer. The system offers signal conditioning for any transducer or signal source. Parallel microprocessing scans up to 1000 channels of measured or calculated data at a 2500-channel/s rate. A-D resolution is 16 bits (0.0015 percent of full scale) and overall accuracy is 0.02 percent. Features include a 12-in. color CRT that uses up to 100 EPROM-stored format pages, high-low limit monitoring on a per-channel basis, and formattable hardcopy output. **Daytronic Corp,** 2589 Corporate Pl, Miamisburg, OH 45342. **Circle 330**

Workstation designs, analyzes, and simulates digital circuits

Using TEGAStation a designer can quickly analyze complex circuitry with high speed and accuracy. Powered by the 32-bit Apollo Domain computer, the system brings CAE software to the design engineer. Software includes an application and file management program, graphics editor, interactive waveform display processor, and logic and design verification. An integrated communication link allows high speed data transfer between the workstation and a VAX. Prices start at $50,800. **Calma Co,** 2901 Tasman Dr, Santa Clara, CA 95050.
Circle 331

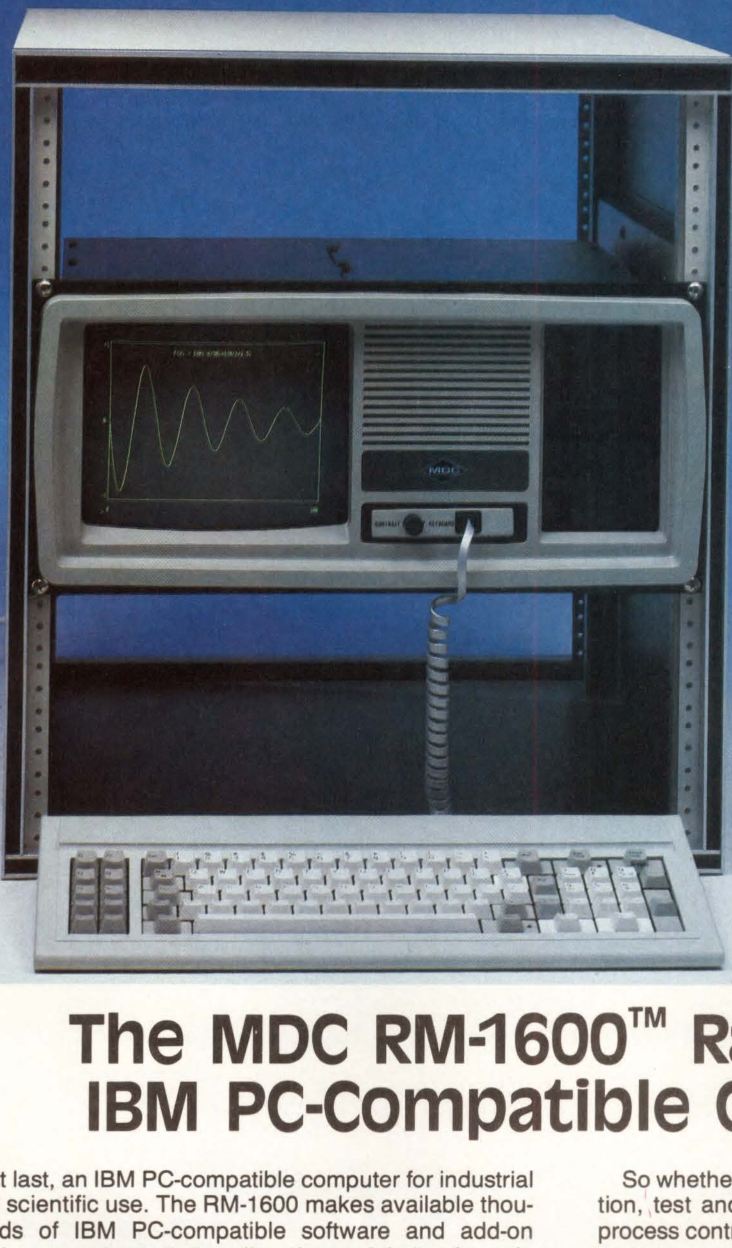
Voice processing system uses proprietary compression

Unix and Multibus compatible, SDC-2000 VoiceServer reduces voice messages to standard microcomputer data rates. It offers its own voice mail software to record, store, retrieve, and transmit digitized voice messages. The system integrates into existing systems, attaches to LANs, and serves standalong applications. Voice compression occurs from 64 kbits/s to as low as 8 kbits/s. The architecture allows interfacing with 2 to 16 external voice ports. Prices range from $13,000 to $45,000. **Digital Sound Corp,** 2030 Alameda Padre Serra, Santa Barbara, CA 93103.
Circle 332

Let's hear from you

We welcome your comments about this issue. Just jot them on the Reader Inquiry Card.

You won't find this PC in an office.



Compatibility:
IBM® PC

RAM on main board:
256 KB standard
512 KB optional

Storage:
Two 320 KB floppies
Optional 10 MB Winchester
RAM-disk built in

Ports:
1 parallel, 1 serial

Expandability:
4 available slots
110 W power supply

Display:
High-contrast, non-glare
16x13 character font
640x325 graphics built in

Software:
MS™-DOS, GW-BASIC™,
assembler

The MDC RM-1600™ Rackmount IBM PC-Compatible Computer

At last, an IBM PC-compatible computer for industrial and scientific use. The RM-1600 makes available thousands of IBM PC-compatible software and add-on hardware products. It also offers the modularity of a rackmount housing.

And the RM-1600 provides four available expansion slots and a high capacity 110 W power supply that let you really mix and match all those add-ons.

For additional storage and speed, an optional 10 MB Winchester replaces a diskette drive. Or for speed enhancement alone, try the built-in RAM disk, using the 512 KB on-board RAM capacity. In numerical applications, you can add an 8087 co-processor for greater speed.

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CIRCLE 123

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Introducing The Ridge 32. Mainframe Performance For Under $43,000.

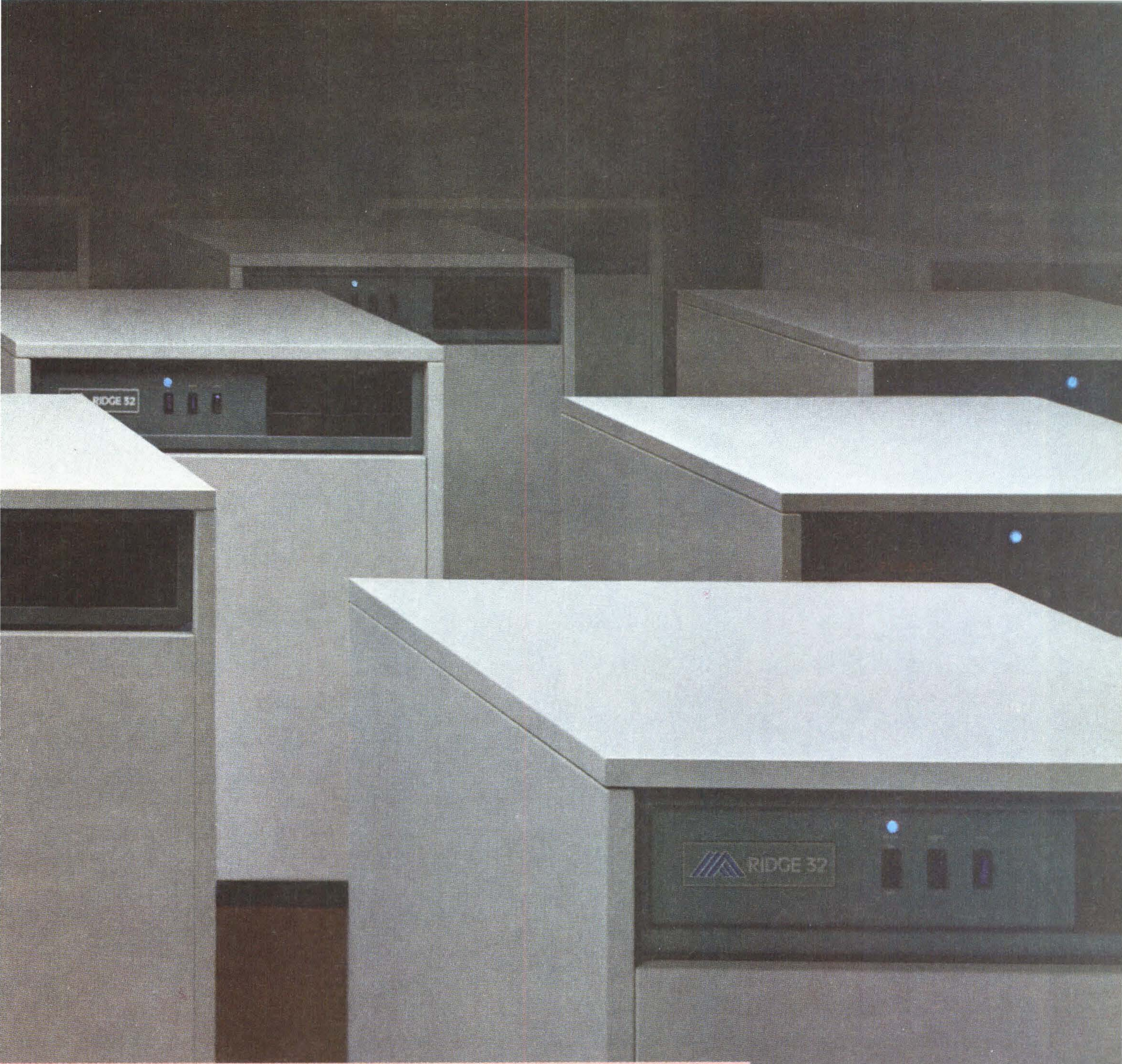
A mainframe computer for under $43,000 is economical. A mainframe computer that networks, distributes resources and talks to the world is logical.

The Ridge 32 is both.

Everything you demand from the most expensive mainframes. Without the headaches. And at one-fifth the cost.

The Ridge 32 is a full 32-bit, UNIX™ System V based computer. A computer powerful enough for the simultaneous operation of as many as four high-resolution graphics terminals. But for under $43,000, it's practical for single users too. And you can expand, one Ridge 32 at a time, as your needs grow.

The Ridge 32 comes in a logical new package that gives you enormous computational power without the frustrations of timesharing. Or the costs of an air-conditioned room.


RIDGE 32

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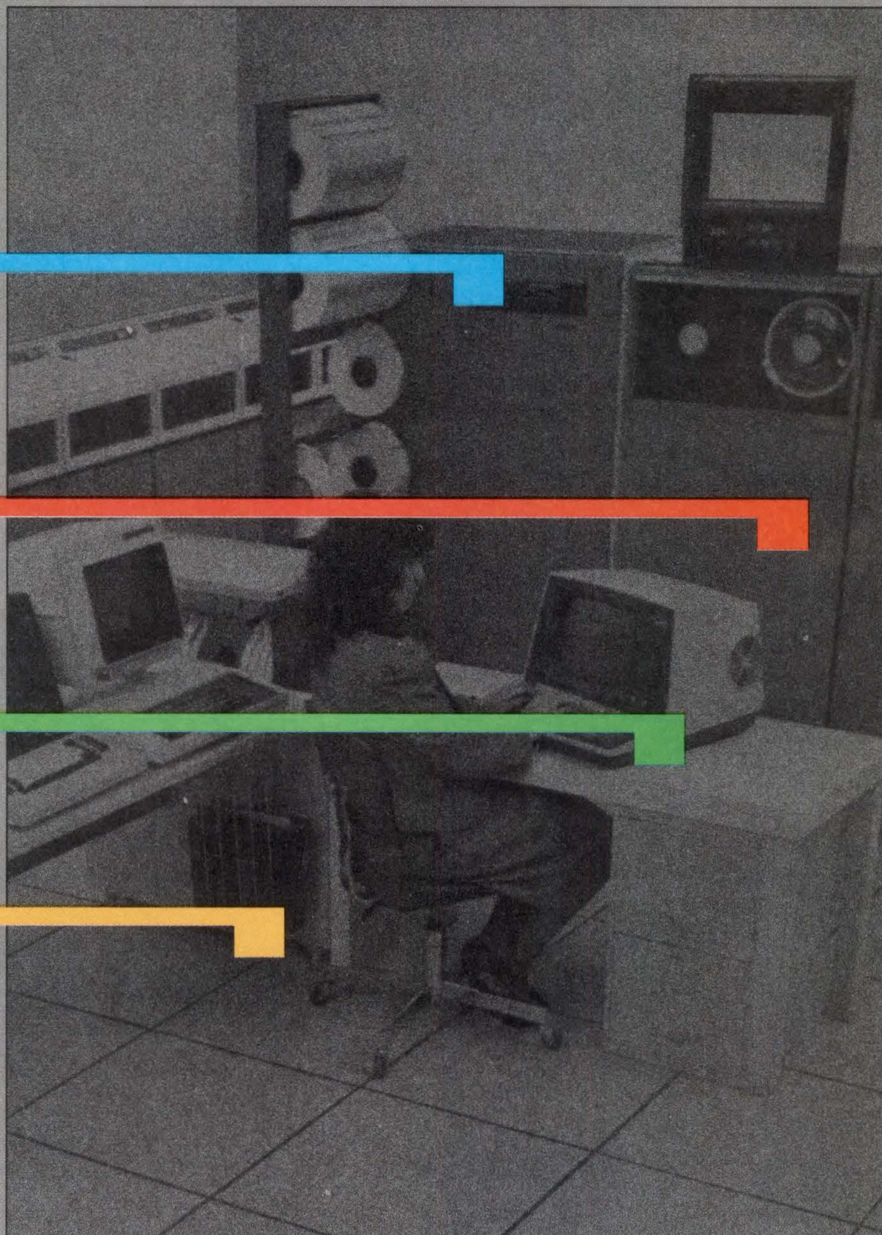

Data Cable — Rely on **Alpha** as a single, quality source for a complete line of data transmission cable and accessories for computer and information systems interfaces. Products include 50 to 100-Ohm coaxial, triaxial, data, individually and/or overall shielded multi-pair cables and molded cable assemblies for RS-232C and IEEE-488 applications.

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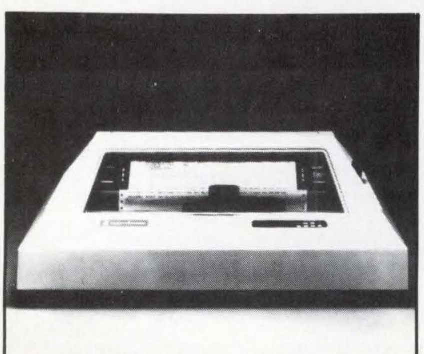
CIRCLE 125

Intelligent terminals cope with industrial environment

Both the model 8300 and 8400 offer a shielded 12-in. CRT that provides 80 col x 24 line display and a 160 x 72 semigraphics capability. Both expand to 44 Kbytes of RAM and 48 Kbytes of user EPROM. The 8300 has a sealed keyboard with characters arranged in alphabetical order. In addition, it contains 12 programmable function buttons with LED active displays and cursor and screen controls. The 8400 has a QWERTY keyboard for data entry input. The models have all metal nonventilated enclosures. **Eagle-Picher Industries, Inc, Akron Standard Div**, PO Box 1869, Akron, OH 44309.
Circle 333

Versatile printer juggles multiple colors and modes

Featuring IBM compatibility, the DP-9725B color/scribe printer produces both text and graphics in a variety of colors. Software handles high resolution screen dumps. Color printing is accomplished by multiple passes and four-color ribbon. Moreover, the printer can change colors at any point in a printed line. Graphics resolution is either 144 dots/in. or 72 dots/in. The four printing modes are enhanced, correspondence, data processing, and graphics. Cost is $1625. **Anadex Inc**, 1001 Flynn Rd, Camarillo, CA 93010.

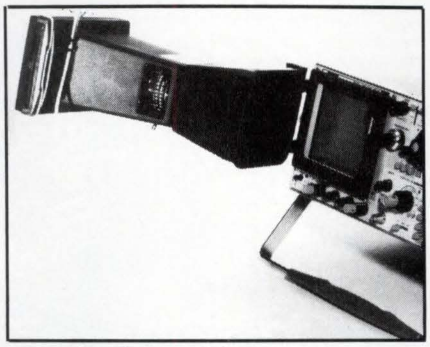


Circle 334

High speed band printer produces hard copy at 1200 lines/min

Designed for the series 3200, the LP1200 is a 132-col, solid-character font peripheral that produces printouts on single or multiple pages. The printer uses a steel band for character sets. The band consists of repeating character sets in an endless loop. Band motion is automatically initiated when data is sent to the printer, minimizing noise. Touch-sensitive control panel includes a self-test unit and features switch-selectable 80- or 132-col printing. Price is $29,990. **Perkin-Elmer Corp, Data Systems Group**, 2 Crescent Pl, Oceanport, NJ 07757. **Circle 335**

Camera works with oscilloscopes and video display tubes



The Primeline model 7000 can be either handheld or bezel mounted. A large selection of prefitted hoods and bezel adapters is provided. The camera accepts Polaroid 3¼- x 4¼-in. film in color or black and white. Variable aperture control from f3.5 to f32, variable shutter control from 1 s to 1/125 s, and B (bulb) combine to provide sharp, clear photos using a wide range of ASA film speeds. The camera matches any one of over 60 CRT bezels. It can swing to either side or be completely removed, allowing the operator an unobstructed view of the display. Prices start at $397 including hood. **Soltec Distribution**, PO Box 818, Sun Valley, CA 91353.
Circle 336

Color graphics terminals offer higher performance

Features of the GTC314 include bit-mapped display, 4000-color palette, polygon-fill in color or pattern, and programmable character sets. Using a 4027-compatible protocol, the 512 x 480 resolution display allows arcs, circles, pies, vectors, bars, and polygons. A 4010 emulation mode permits the use of existing software. Three character sets are available: one fixed and two programmable. The standard character set yields a 48-line display of 85 chars/line; programmable sets define font and cell size up to 256 x 128 pixels. Price is $2895. **Psitech**, 16902 Von Karman, Irvine, CA 92714.
Circle 337

Smart terminal features low cost and emulation capabilities

The 1021 features a 12-in. screen, ergonomic design, 32 graphics characters, and editing functions. The terminal comes in two versions. The first emulates the Hazeltine 1500, ADM 3, DEC's VT-52, and the ADDS Viewport. Any of these emulations can be chosen through soft setup and stored permanently in RAM. The second version supports the ANSI X3.64 standard. Both versions offer a 91-key low profile keyboard and a display with 24 lines by 80 chars. Two communication ports are standard. Cost is $399. **Zentec Corp**, 2400 Walsh Ave, Santa Clara, CA 95050.
Circle 338

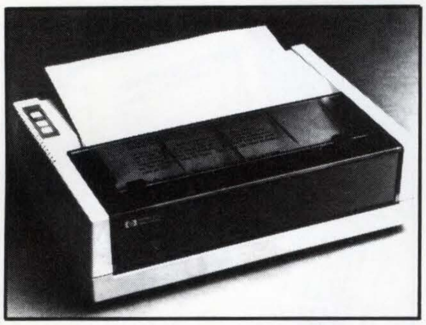
Thermal transfer printer works on various surfaces

The 16-dot TTP16 produces near-letter quality on a variety of papers, even vinyl. The thermal head provides high resolution 1/120 x 1/120 in. in a single pass. A precision positioning feature ensures alignment at 45 chars/s. Operation is silent as the printhead never strikes the printing surface; all moving parts are driven by stepping motors. Other features include vertical and horizontal tabs, sensor for paper out and ribbon end, and multiple color printing. The cost is $470. **Fujitsu America, Inc**, 3075 Oakmead Village Dr, Santa Clara, CA 95051. **Circle 339**

Graphics display terminal is compatible with Plot 10

The NJC-M1401 II consists of a high resolution green or amber monitor, graphics processor, communication section, and separate keyboard. Features include a 14-in. nonglare CRT, 1032- x 780-dot resolution, and selective erase. The terminal also provides DEC VT-100 emulation and an optional graphics package. In single quantity, cost is $2995. **Japan Computer Corp**, Naito Bldg, Nihonbashi Hamacho 2-25-1, Chuo-ku, Tokyo, Japan.
Circle 340

Lightweight ink-jet printer operates quickly and quietly



The HP 2225 may be used with portable or desktop computers from a variety of manufacturers. It combines the printhead with the ink reservoir in one disposable unit. Key specs include: 150-char/s print speed, 11 x 12 dot-matrix chars, less than 50 dB of noise, and multiple print sizes. Interfaces are Centronics, HP-IB, and HP-IL and any paper can be used. Dimensions are 11.5 x 8.1 x 3.5 in. weight at 5.5 to 6 lb. Price is less than $600. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 341

Dual-format terminal displays data-translation capability

Twist provides 80 col x 72 line or 80 col x 24 line formats. Rotating the CRT screen 90 degrees to an alternate orientation enables the dual-format function. All data is retained during the rotation and the characters automatically reorient themselves in less than 1 s. Standard terminal features include 16 user-definable function keys, bidirectional pass-through printer port, five video attributes, and an editing keypad. Cost is $1895. **Micro-Term, Inc,** 512 Rudder Rd, Fenton, MS 63026.
Circle 342

Impact line printer changes to three different speeds

Operating at 3600, 3000, or 2200 lines/min, the 4248's printing speeds are controlled at the unit's operator panel. A microprocessor allows the printer to detect the diagnose potential problems to minimize service requirements. The unit prints by striking hammers against individual alphanumeric characters that are etched into a rotating steel band. These characters strike an inked ribbon to transfer each impression to paper. The basic model 1 printer is $99,000. **IBM Corp, Information Systems Group,** 900 King St, Rye Brook, NY 10573.
Circle 343

Character-recognition terminal provides graphics capabilities

Incorporating the functions of dynamic handwritten character and mark/sense recognition, the Inforite features a 2-line x 32-char LCD that identifies the field and data as written. Error messages are also provided. Based on a 4-MHz Z80, the terminal operates independently of a host and contains 64 Kbytes of RAM, 56 Kbytes of ROM, and 48 Kbytes of CMOS battery backed RAM. The terminal operates with a ball-point pen and can accommodate three-part forms. Price ranges from $1250 to $2000, depending on quantity. **Inforite Corp,** 1670 S Amphlett Blvd, San Mateo, CA 94402.
Circle 344

Smart graphics terminal emulates Tektronix

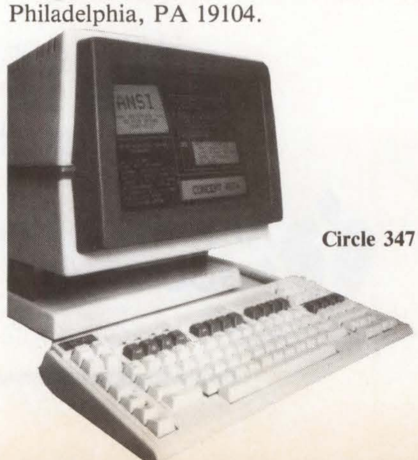
The GX-100 is a dual-alphanumeric and 4010/4014-compatible terminal. In the alphanumeric mode, it emulates the DEC VT52, VT100, and ADM-3A. It provides two independent text planes as well as two full 768 x 585 graphics planes with independent alphanumeric overlay. Standard features include a 15-in. high resolution CRT with green P-39 phosphor, detachable keyboard with graphics function keys, and four types of vectors. The terminal supports Plot 10 software. **Modgraph, Inc**, 1393 Main St, Waltham, MA 02154.
Circle 345

High resolution graphics terminal includes controller

The Cadmus 2200 has an intelligent controller with its own 16/32-bit processor—a 10-MHz 68000. Directly connected to a Cadmus 9200, it links to the graphic monitor with a 10-m coaxial cable. The controller contains a 256-Kbyte memory for programs and picture synthesis and interface for hookup to a serial keyboard or mouse. A pixel processor permits high speed graphic creation. Direct coupling to the system bus allows graphic images to load directly from disk to memory. **PSC GmbH**, Pfaelzer-Wald-Strabe 36, 8000 Munchen 90, West Germany.
Circle 346

Terminals meet ANSI standard and DEC software requirements

The concept AVT+ series provides 80/132-col capability, eight pages of memory, 46 programmable function keys, windowing, and multiple computer connections. The 101-key keyboard offers function key labeling, adjustable tilt, full touch area keytops, four programmable LEDs, and a VT100-style numeric pad. The programmable keys can transmit data and/or execute terminal commands. The display memory eliminates unnecessary printouts and provides an application tool for multiple formats of large volumes of text. With a standard four-page memory, the terminal is priced at $1295. **Human Designed Systems**, 3440 Market St, Philadelphia, PA 19104.



Circle 347

Networking software supports two protocols

Fusion Version 2.0 implements the ARPA Internet as well as the X protocols. The high performance networking software runs on the Ethernet LAN. It offers flexibility linking 6800, VAX PDP-11 and IBM-PC processors; Unix, MS-DOS, and VMS operating systems; and network hardware from most LAN vendors. The software supports the TCP, IP, UDP, and ICMP internet protocols. Completion XNS implementation includes datagram, echo, error, routing, packet exchange, and sequenced packet protocols. **Network Research Corp,** 1964 Westwood Blvd, Los Angeles, CA 90025.
Circle 348

Communication package puts IBM mainframes in touch with others

Using a blocked asynchronous transmission and sliding window protocol, a software release achieves throughput, efficiency, and error immunity. It uses an SDLC-like full-duplex CRC protocol. Binary or text files are transmitted as 8-bit wide data with each block checked for 100-percent data integrity. Software operates over standard dial-up phone lines with any asynchronous modem, at any modem speed, or over direct connections at speeds to 19.2 kbits/s. Prices range from $250 to $2495. **Communications Research Group, Inc,** 8939 Jefferson Hwy, Baton Rouge, LA 70809.
Circle 349

File management systems enhance performance

Btrieve 3.0 and N 3.0 have improved file characteristics, sorting capability, more efficient use of disk space, and high speed file handling options. Designed for the IBM PC, PC-XT, and compatibles, the software also runs on other micros. Keys can be defined as having multiple segments for multilevel sorts built into a file. A utility builds an external index for an existing file. Btrieve is based on the b-tree file index, an optimum file handling structure. Prices range from $245 to $595. **SoftCraft Inc,** PO Box 9802, Austin, TX 78766.
Circle 350

Floating point libraries process via IEEE formats

The 68000 FPAC/DPAC is written in optimized source assembly language for tailoring to specific applications. In addition to the standard arithmetic operations and integer to floating point routines, the library includes sine, cosine, tangent, arc tangent, square root, log, and exponents. ASCII to floating point and floating point to ASCII conversions are also part of the library. Maximum-code space for single-precision routines is under 3500 bytes. Prices range from $750 to $1250. **U.S. Software,** 5470 NW Innisbrook Pl, Portland, OR 97229. **Circle 351**

June Previews
Watch for two special articles—local area networks on June 1, system testing on June 15

Enclosures for your ideas

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PAC-139

Pascal and Fortran 77 for Unix are written in Pascal

Current Unix versions target the NS16000 and NS32000 microprocessors and generate directly executable optimized object code. Both compilers are implemented in Pascal and are rehostable and retargetable to any architecture. Fortran is consistent with the ANSI standard (X3.9-1978) for full Fortran 77. Pascal compiler is a large superset of the ANSI/IEEE standard 770 X3.97-1983. Major extensions include separate compilation, external procedures, initial values, and string processing. **Advanced Computer Techniques Corp,** 16 E 32nd St, New York, NY 10016.
Circle 352

Computer aided design package runs on personal computers

Electronic Design Automation software turns a general purpose computer into a specialized electronic design workstation. It integrates the engineering and layout portions of PC board design. An integrated intelligent data base keeps track of electrical and logical connections, device attributes, and other data. The same data base can be used for schematic design, PC board design, and IC floor plans. PC-CAPS is a schematic capture system for development at the logic level. PC-CARDS is a layout package. PC-LOGS is a logic simulator. **Personal CAD Systems, Inc,** 981 University Ave, Bldg B, Los Gatos, CA 95030.
Circle 353

Database management system styled for mainframes

With built-in calculation, stats, and graphics, Aladin can exchange data with a variety of existing word processing and spreadsheet programs. An integrated set of modules standardizes menu options and commands. Modules include data, report, query, and calculation. The system allows up to 2 million records per data base with variable-length records (automatic data compression on all fields) and allows 50 percent more data to be stored on disk. Prices range from $595 to $795. **Advanced Data Institute America,** 1215 Howe Ave, Sacramento, CA 95825.
Circle 354

Software integrates transaction processing with development

The Primeway transaction development and management system aims for increased productivity. Cobol 74 provides a highly structured, yet flexible interactive development environment to accelerate and standardize the commercial application development process. The control system has administrative facilities for operational control, security enforcement, and full transaction management. An automated application and document library frees the developer from source and documentation maintenance. Prices range from $9600 to $55,000. **Prime Computer, Inc,** Prime Park, Natick, MA 01760.
Circle 355

INTERFACE

Graphics display controller produces 16-color display

The dual-width IV-1651 has a 600 x 800 resolution display (16 colors) or a 4-color display with 1024 x 1024 or 1280 x 768 resolution. The card features a hardware pixel processor capable of plotting vectors and arcs at 800 ns per pixel, integer zoom, and DMA port for rapid screen updates. The unit is priced at $1995 with 128 Kbytes of display memory; $2295 with 256 Kbytes of display memory. The 16-color option (analog RGB) is $250. **Ironics Inc,** Eastern Heights Dr, PO Box 356, Ithaca, NY 14850. **Circle 356**

Magnetic-tape controllers interface with Multibus-based computers

The TFC 505A operates with the Storage Technology 125-in./s drive 1953/35 and the 505B operates with the 50-in./s 2920. The half-in. tape controllers for start/stop drives use GCR technology. A modular data FIFO, expandable from 4 to 32 Kbytes, is built with high speed static RAMs. The RAMs together with dedicated hardware for bus control achieve high bus data rate of 2.5 million transfers/s. Optimizations are achieved via three programmable controls: prefetch, burst size, and dead slot. Price for the basic TFC 505 is $2950. **Aviv Corp,** 26 Cummings Park, Woburn, MA 01801.
Circle 357

Graphics controller supports software and STD bus

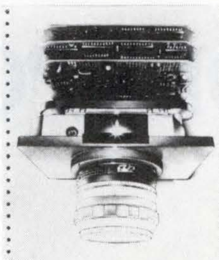
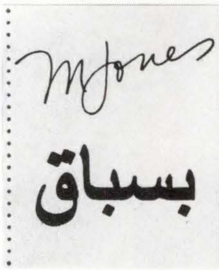
As a 64-Kbyte video memory board that generates a 640- x 480-pixel display, the ST4505 provides the user with selectable wirewrap options. They include TTL-compatible or composite video and sync selection, external clock input, and combination of external video and sync from other video display products. Memory-mapped design keeps memory overhead to a minimum. The unit appears to the host as a series of individually accessible 2-Kbyte banks, each enabled or disabled by a software programmable I/O latch. In 50s, the price is $450. **Applied Micro Technology, Inc,** PO Box 3042, Tucson, AZ 85702.
Circle 358

Intelligent digital input module handles 48 inputs

Designed to enhance system performance through onboard intelligence, the EP-8965 module can operate as a system slave via the 48 opto-isolated inputs. The inputs are monitored by an 8088. Data and commands are passed through 4 Kbytes of dual-ported RAM for decreased system overhead. Supplied with preprocessing firmware, the inputs may be configured as pulse accumulators, pulse duration, or pulse period inputs. Each input is hardware debounced and rolled off to 100 Hz, and meets IEEE 472-1973 surge specs. **Symbicon Associates, Inc,** 89 Rte 101A, Amherst, NH 03031.
Circle 359

WE COULD GIVE YOU A LOT OF TALK ABOUT IMAGE PROCESSING. OR A LOT OF PROOF.



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The Eye of the Computer™

Mainframe windows on IBM PCs available through add-on interface

An interface lets PCs function as 3270s. The Attachmate-3270 works with up to seven different programs and displays each in a separate screen window. Mainframe access security is controlled with a lock and key. The interface also allows PCs to coax-connect to all 3270 control units instead of via Bisync and SNA networks. No PC memory is used and 256 Kbytes are optionally included onboard. The standard interface is available for $910. **Attachmate Corp**, 3241 118th SE, Bellevue, WA 98005.
Circle 360

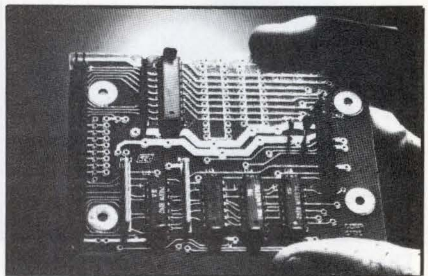
Dual-port I/O board switches transmission rates

Designed for IEEE 696/S-100 bus systems, 8800GF provides two independently addressable RS-232-C or 20-mA ports. An onboard 5.0688-MHz crystal oscillator permits switch-selectable data transmission rates from 50 to 19.2k bits/s. The serial interface employs type 1602 universal asynchronous receiver transmitters for parallel-to-serial/serial-to-parallel conversion, error detection, and serial-data formatting. There are provisions for adding capacitors on output driver lines to limit slew rate with very short cable lengths. **Vector Electronic Co, Inc**, 12460 Gladstone Ave, Sylmar, CA 91342.
Circle 361

Eight-channel conversion board configures for current/voltage mode

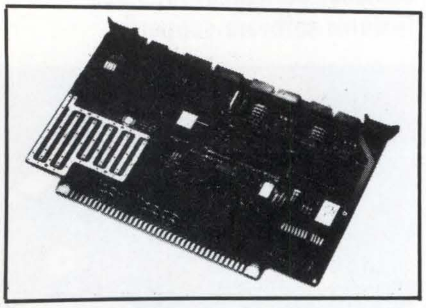
The DSSE8DA12 12-bit D-A board has a conversion time of 3 μs and accuracy to $\pm 1/2$ LSB. Maximum nonlinearity is ± 1 LSB and both gain and offset errors are adjustable to zero. Eight software selectable operating channels are latched. Input modes are jumper selectable and include bipolar, unipolar, and 20-mA current loop. The board takes two consecutive memory locations and requires power of 5 V at 1.5 A. Price is $1875. **Data-Sud Systems/U.S., Inc**, 2219 S 48th St, Tempe, AZ 85282.
Circle 362

Compact peripheral interface features software support



The SASI-100 board converts an 8255 parallel port to the SASI/SCSI standard for interfacing to intelligent peripheral controllers. Primary use will be interconnection to a hard disk controller board. The manual gives four programs for bringing up a hard disk. The format command formats an uninitialized hard disk. HBIOS is a complete BIOS for use with CP/M. PUTSYS will put CP/M and HBIOS on the hard disk system tracks, and HBOOT brings in CP/M. Price is $95. **Miller Technology Inc**, 647 N Santa Cruz Ave, Los Gatos, CA 95030.
Circle 363

Module controls four floppies and digital input/output



The GMS6519B manages four 5¼-in. drives and provides two full RS-232-C ports with modem control functions. The ports control terminals or modems and other serial I/O devices. The parallel port allows control of a Centronics-type printer. The controller can format/control drives in single-sided/single-density (FM) or double-sided/double-density (MFM) modes. It also offers programmable sector lengths, motor on, and a choice of step rates or extra fast step rates for existing and future fast drives. In 100s prices are $295. **General Micro Systems Inc**, 1320 Chaffey Ct, Ontario, CA 91762.
Circle 364

Analog system accommodates 32 input channels through an amp

Q-bus compatible, model 123 runs at 250 kHz in channel scanning mode using DMA. It accommodates up to 32 single-ended input channels through an over-voltage-protected multiplexer/differential amp. A sample/hold allows signal acquisition and a 12-bit A-D converter digitizes the information in 2.5 μs. A buffer register holds the A-D result for transfer directly to the CPU or memory. Pricing in quantities of one to nine is $2495. **Grant Technology Systems Corp**, 11 Summer St, Chelmsford, MA 01824.
Circle 407

Multitasking controller manages micro and mini disk systems

Connecting to the host via the SCSI bus, the Saber-AP is an ST506 Winchester disk controller. The device works in combination with other SCSI compatible peripheral controllers, providing users with a full multitasking I/O bus. Configured on a single 5¼-in. form factor card, it supports two Winchesters and high capacity disk drives having up to 16 heads. Standard features include SCSI bus parity and error recovery messages for accuracy on all bus transactions. Parity is also provided on the board's internal 1-Kbyte data buffer. ECC corrects up to 8 bits. In quantities over 500, cost is $408. **Adaptive Data & Energy Systems,** 2627 Pomona Blvd, Pomona, CA 91768.
Circle 366

Converter guarantees no missing codes over temperature range

The monolithic AD9000 is a 6-bit device that dissipates maximum power of 0.82 W. It guarantees maximum differential nonlinearity of ± 0.4 lsb when encoding at 75 MHz for S grade and 50 MHz for J grade. The chip does not require a track and hold amplifier to digitize fast slewing signals. The internal data latches go into a hold mode when encode input goes high, retaining the last state of the comparators. The converter has a 10-ns maximum transient response time for full-scale step change. Pricing in 100s is $46 to $78. **Analog Devices,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062. **Circle 367**

CIRCLE 135

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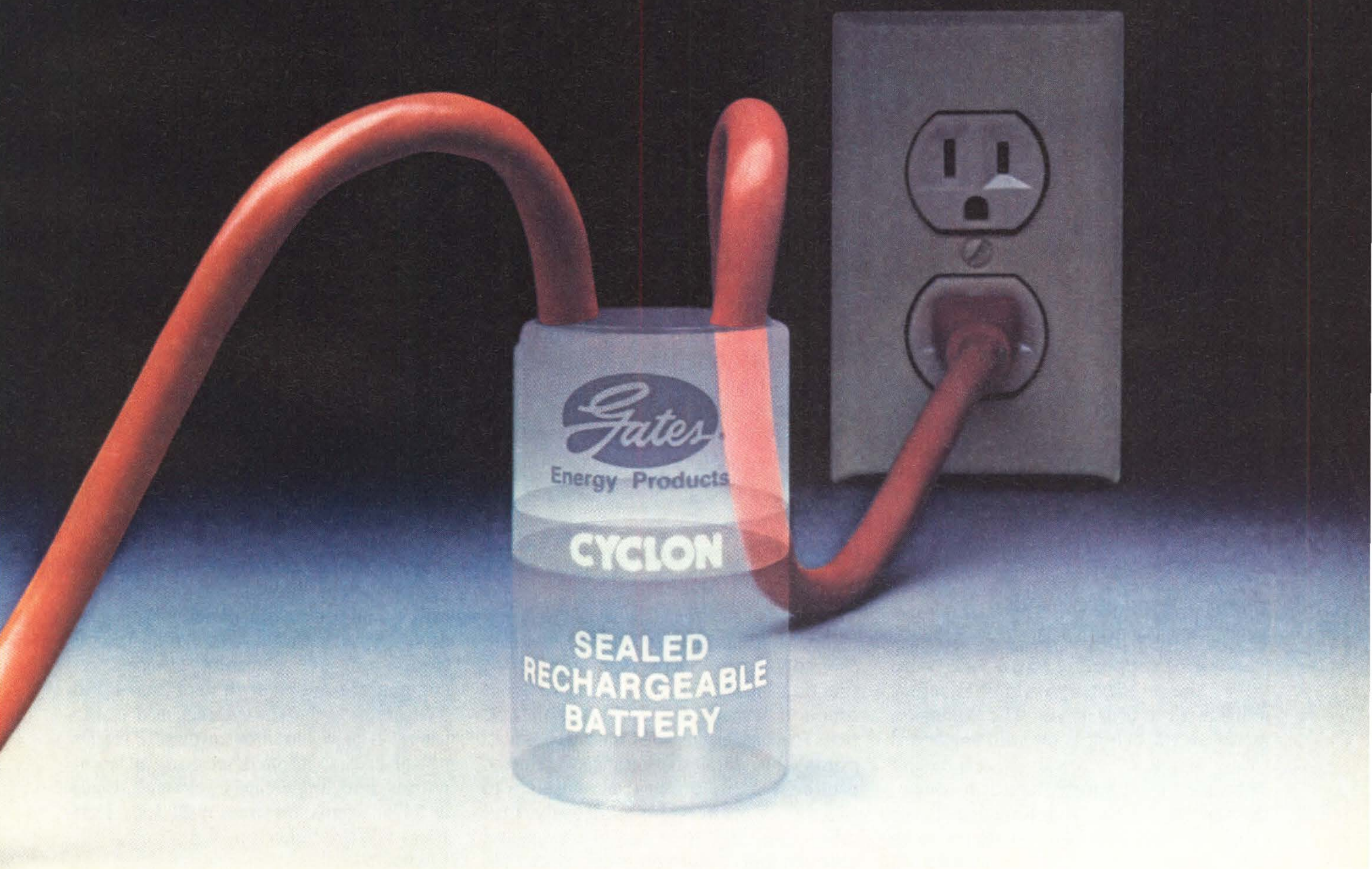
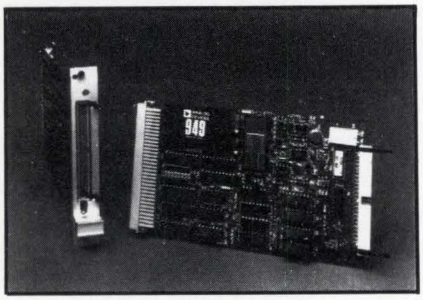


CIRCLE 136

Analog interface boards bring low cost I/O to VME micros



Available in single Eurocard format, the RTI-600 and RTE-602 meet factory automation and process control requirements. The 600 offers 16 single-ended or 8 differential input channels and is expandable to 32 single-ended channels. An onboard instrumentation amp with user-selectable gains from 1 to 1000 permits direct connection of low level signals. The 12-bit A-D converter offers ± 0.01 percent accuracy. The 602 offers 4 analog output channels, each with 12-bit resolution. The board contains an option for two 4- to 20-mA current outputs. In 25-piece lots, the boards are priced between $411 and $535. **Analog Devices, Inc,** 2 Technology Way, Norwood, MA 02062.
Circle 368

Parallel digital I/O board plugs into IBM PC/XT

The PIO-12 provides 24 TTL/DTL compatible lines, along with interrupt input and enable. External connections are to the PC's 5-, 12-, −5-, and −12-V bus power on a half-slot board via a 37-pin D connector. A three-state driver with a separate enable takes care of interrupt handling. It may be configured to interrupt levels 2 to 7 on the PC bus by a plug-type jumper on the board. Three programming modes permit standard, strobed, and bidirectional I/O. In single quantities, cost is $89. **MetraByte Corp,** 254 Tosca Dr, Stoughton, MA 02072.
Circle 369

Floppy controller expands mass storage interface

Capable of supporting any 8- or 5¼-in. drive, the BLX-218 can simultaneously manage up to four drives. The expansion module is fully compatible with any board using the BLX onboard I/O expansion interface. It supports IBM 3740 single-density, IBM system 34 double-density, or other formats with sector lengths up to 8192 bytes. The controller operates in either single or multiple sectors and has onboard data separation logic for encoding and decoding. It also performs in either DMA or non-DMA environments. In quantities of one to nine, the device costs $493. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 370

System lets CP/M software run on HP computer

The HP Bridge allows HP 3000 users to access from any terminal the library of CP/M software. The complete system comprises a coprocessor board, software utilities for translating and transferring data, and a license to CP/M. Microcomputer files are stored on the host minicomputer's mass storage device. Then they are dated, labeled, and backed up by the host operating system. Users of the virtual microcomputer gain access to the high speed central peripherals, thus minimizing hardware costs and allowing maximum microcomputer speed. **Virtual Microsystems, Inc,** 2150 Shattuck Ave, Berkeley, CA 94704.
Circle 371

Data bus adapter controls signals from IEEE 488 bus

Compact model DBA-488 adapts TTL-compatible equipment to the IEEE 488 bus for computer-controlled applications. The self-contained, preprogrammed logic interface unit meets requirements of the IEEE 488-1975 GPIB standard. Operation of the adapter is micro controlled according to programs stored in ROM. The interface controller mediates data transfer to and from the bus. There are 32 identical I/O lines at the instrument interface that are independently programmable. Price is $1162. **ILC Data Device Corp,** 105 Wilbur Pl, Bohemia, NY 11716.
Circle 372

Printer buffer contains 64 Kbytes of memory

The model 500 features a Centronics-compatible parallel interface, memory expandable to 256 Kbytes, multiple copy function up to 255 copies, and pause function to temporarily halt data output. The buffer has four modes. Manual prints the data to manually selected printer. Double prints the same data to two sets of printers simultaneously. Free prints the data to a not-in-use printer automatically, and command prints the data and/or copy to the printer selected by printer software command. Price is $325. **Taxan Corp,** 18005 Cortney Ct, City of Industry, CA 91748.
Circle 373

Single-board interface connects to IBM multiplexers

All circuitry required for complete interface is on the model 8300 and no additional user hardware assembly is necessary to connect to the IBM channel. The board operates under control of its own onboard processor and can emulate any one of several control units. Data transfers occur at rates to 500 kbytes/s. Other features include an onboard RAM buffer with 16 Kbytes. The unit comes with diagnostic software, technical documentation, and custom programming services. **Auscom, Inc,** 2007 Kramer Ln, Austin, TX 78758.
Circle 374

Controller for Winchesters supports 22-bit addressing

The WDC11-H interfaces to the MicroMagnum family of removable cartridge Winchester drives. With the 5/5 version, the controller emulates two RL01 units per drive (one removable, one fixed) for a 10.5-Mbyte storage capacity/drive. The dual-width card contains an onboard bootstrap ROM. Transfer rates are 625 kbytes/s peak, 164 kbytes/s average. The card uses write pre-compensation and a true VCO data separator for data reliability. Quantity 50 price is $1312. **Andromeda Systems Inc,** 9000 Eton Ave, Canoga Pk, CA 91304.
Circle 375

Controller board interfaces to four Winchester drives

The WDC-501 STD bus controller has all necessary buffers and receiver/drivers for direct communication. Communication is via nine I/O ports and the onboard sector buffers allow data transfer to the host computer independent of the drive's transfer rate. Other features include built-in separator, write pre-compensation logic with data rates up to 5 Mbits/s, and 1024-cylinder addressing range. It also provides automatic retries on all errors, implied seek on all commands, and single-card packaging. Price is $495. **Jonos International, Inc,** 1835 Dawns Way, Fullerton, CA 92631.
Circle 376

Surge generator tests low voltage ac circuits

Model 587 follows ANSI/IEEE C62.41-1983 requirements. It allows super imposing any of three waveforms on active ac power lines. The three signals are a damped 100-kHz oscillatory waveform of 6000 V peak, with greater than 500-A peak current; an exponential 6000 V into high impedance; and an exponential 3000-A waveform into short circuit. Surges trigger manually or electrically; surge signal phase is adjusted with respect to the ac sine wave. Basic price is $11,500. **Velonex,** 560 Robert Ave, Santa Clara, CA 95050.

Circle 377

Hazard protection is automatic for computers

System II automatically protects computers from 14 environmental, power line, and security threats. It monitors and reacts to overheating, transients, multiple power interrupts, and brownouts. The control console is equipped with LED status indicators and audible alarms. A remote status module (a slave unit to the control console) allows a remote station to respond to fault conditions. The controller handles 75 A per phase at 120 to 208 Vac, 50 to 60 Hz. Prices start at $13,600. **Sentec Inc,** 1265 N Dutton Ave, Santa Rosa, CA 95401.

Circle 378

Enclosure matches packaging for STD-bus/non-STD-bus components

The Naked 701 allows users to house non-STD-bus parts in packaging identical to that of STD-bus-based system units. It can package other standard buses, on-off circuitry, or other components required to adapt STD-bus systems to a particular application. The enclosure includes fan, two auxiliary power outlets, fuse protection, an on-off switch, and rfi filtering. Six threaded inserts on the inside surface allow customizing, and removable front and rear panels permit installation of user-chosen connectors and controls. Price is $750. **Pro-Log Corp,** 2411 Garden Rd, Monterey, CA 93940.

Circle 379

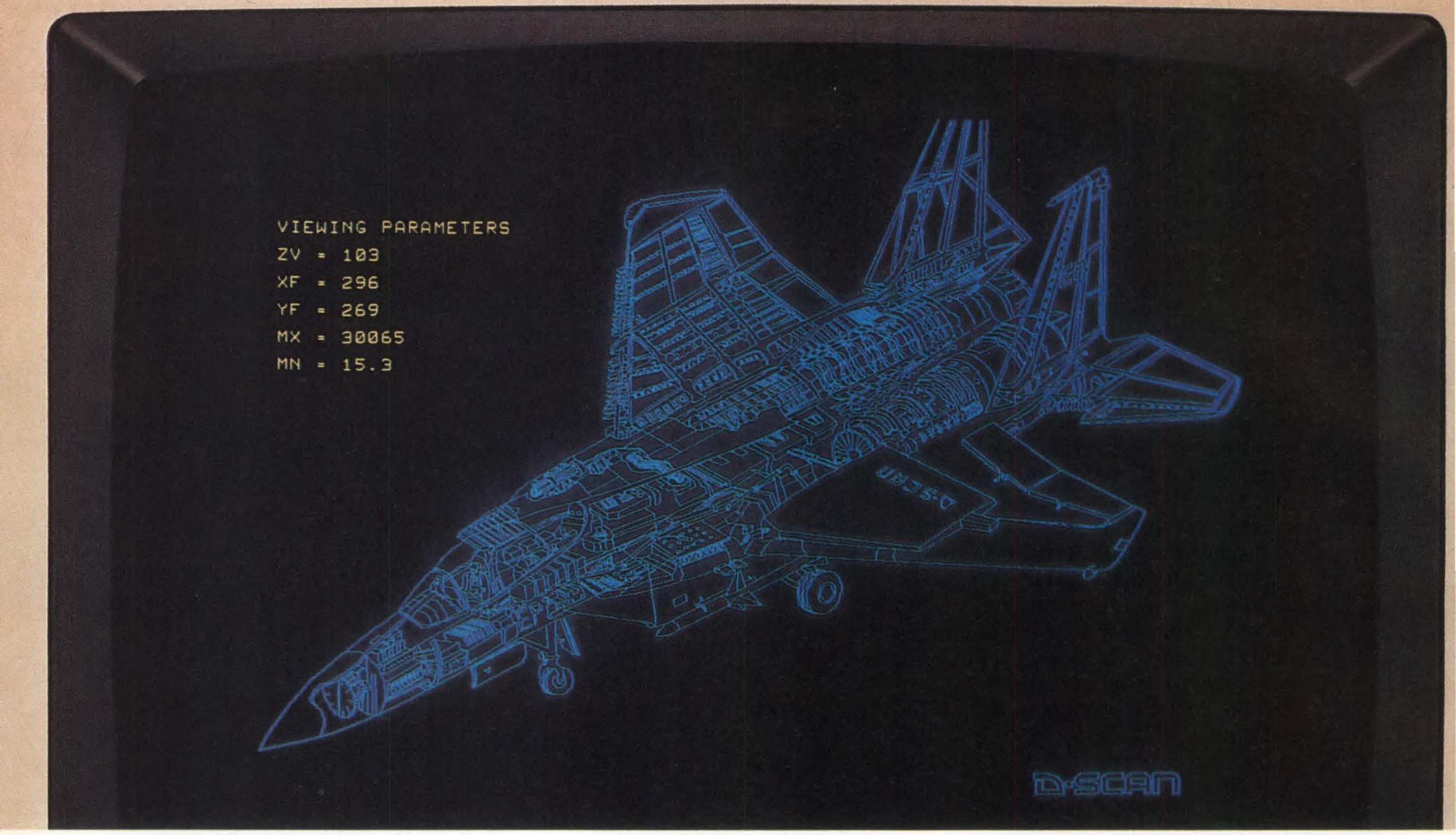
Talk to the editor

Have you written to the editor lately? We're waiting to hear from you.

Power semiconductor switches with high input impedance

Suitable for medium current, high voltage, low frequency applications, the GEMFET has an internal on-resistance that is approximately 10 times lower than comparable MOSFETs. The line consists of four 20-A devices; two have a VDDS of 450 V, the others have a VDDS of 500 V. Specs include a low on-resistance of 0.27 Ω maximum, turn-on time of 60 ns, fall time of 4.5 μs, and forward transconductance of 3.0 mhos. In quantities of 100 to 999, prices range from $6.50 to $8. **Motorola Semiconductor Products Inc,** PO Box 20912, Phoenix, AZ 85036.

Circle 380



High Speed Craft.

No, not the fighter. The craft we're talking about is yours. Because with the D-SCAN GR-2414, you'll experience something you've probably never felt before. High speed response.

Gone are the days when you had to sit around waiting for the host computer to answer your commands.

Quickly, here's the story. Speed. Efficiency. Power. Extraordinary visual acuity. And local control!

We're not done yet, either. You can display up to 1024 colors (not the usual 256). Read them flawlessly on our 1280 x 1024 display (with 60Hz non-interlaced refresh rate!). And expand the 4 bit planes to 10.

The 2414 also gives you display list storage that's simply unmatched in its price class. Starting with 256K and field-expandable to over 1Mbyte! That's two, three, sometimes even four times more storage than you can find in so-called competitive terminals.

Then, to make sure you get the picture you want, the 2414 gives you local picture manipulation. Local transformations. And local graphics tablet support. Which means you'll have true local interactive support. You won't get bogged down while the host spews out accounting reports. And you get instant visual response every time you need it.

There's more to those pictures, too. More complexity. More detail. More information on the 20" screen at any one time. Plus, the handy ability to manipulate the image in more ways. And display alphanumerics with beautiful precision.

A very pretty picture indeed. What's more, you get easy interface to our color hardcopier. Programmable function keys. A user-definable look-up table. And user-definable hardware anti-aliasing.

But hardware technology notwithstanding, you also get a powerful software story with the 2414. For instance, it's compatible with the TEK 401X instruction set and Plot 10 package. So you can save a lot of time and aggravation implementing graphics software. Upgrade quite painlessly. And eliminate costly re-learning curves.

There's something heavyweight to remember, too. Our service. We design, build, sell and service all of our equipment. So you never have to wander around wondering who to call for help. And waits are lifted because you get direct service from 13 offices across the U.S.

So call today to learn more about the GR-2414. We'll get back to you with utmost speed. Just call your local Seiko Instruments sales person, or us at (408) 943-9100. Write 1623 Buckeye Drive, Milpitas, CA 95035.

You'll find there's a new high speed craft that's drawing a lot of attention. Yours.

SEIKO
INSTRUMENTS

Sockets designed for J-11 CMOS microprocessors

Part of the 700 series, the 60-pin socket includes a disposable aluminum carrier supporting precision machined contact assemblies. Socket pins are inserted along with the carrier into a PC board. This configuration maximizes air flow for cooling and eliminates heat entrapment associated with insulation material. Inner contacts are seamless and maintain a symmetrical four-finger configuration to ensure uniform mechanical contact. Price is $3.76 each in lots of 100. **Augat Inc, Interconnection Components Div,** 33 Perry Ave, PO Box 779, Attleboro, MA 02703.
Circle 381

Tell us what you like
Did you remember to rate the articles in this issue of Computer Design? A special editorial score box is provided on the Reader Inquiry Card.

Silver-plated copper shielding meets military specs for emi/rfi

A composite gasketing material, Multi-Point VI-SPC consists of silicone elastomer containing a homogeneous dispersement of silver-plated copper particles. This provides a tight environmental seal as well as shielding performance over 75 dB through a frequency range of 14 kHz to 10 GHz. It is produced in silicone elastomer of 35, 60, 70, and 80 durometer; in fluorosilicone of 60 to 80 durometer; and in reinforced silicone of 80 durometer. **Conductive Systems, Inc,** Dorine Industrial Park, Merry Lane, East Hanover, NJ 07936.
Circle 382

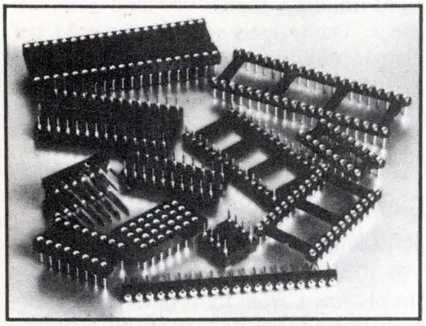
Power switcher delivers 2.5 W of output/cubic inch

The DP-7000 series are available in seven voltage/current output combinations ranging from 2 V at 150 A to 28 V at 26 A. The fully enclosed, fan-cooled units have a maximum continuous output power of 750 W. Because the supplies are modular and can be wired in parallel, additional output currents are easy and inexpensive to obtain. Output polarities can be either negative or positive modes to ground. Internal rfi/emi noise emissions filtering meets FCC and VDE 0841 specs. The models sell for under $1 per watt in quantity. **Datapower, Inc,** 3328 W First St, Santa Ana, CA 92703.
Circle 383

Direct current supply has self-contained HP-IB

The 1000-W HP 6032A auto-ranging power supply has a friendly programming format. It produces 50 A at output voltages up to 20 V and develops no fewer than 1000 W through its 20- to 60-V output range. The supply meets VDE 0871/6.78 level B for both conducted and radiated emissions. The micro-based architecture provides automatic and HP-IB invocable self-test and signature-analysis stimulus. With the unit, a programmer can read back and confirm all programmed functions and values, as well as output voltage, current, and power supply status. Price is $3100. **Hewlett-Packard Co,** 1820 Embarcadero Rd, Palo Alto, CA 94303.
Circle 384

Sockets insert with low force for faster production

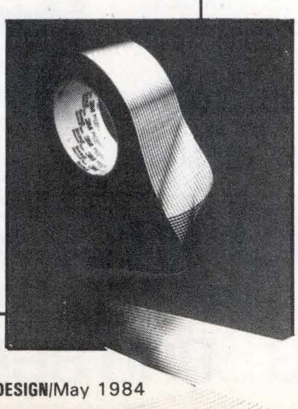


Requiring only 3.5-oz. average force per pin, sockets come in open- or closed-frame configurations with 8 through 64 pins, as well as 20-position single-in-line break away socket strips. Terminal styles include a choice of solder tail, super low profile, and two- or three-level wire-wrap. Plating combinations of tin/tin, tin/gold, and gold/gold are standard. They feature four-finger contacts for reliability, 100 percent anti-wicking of solder, and tapered entry. **Advanced Interconnections,** 5 Division St, Warwick, RI 02818.

Circle 385

Electrical tape makes low current interconnections

As an adhesive tape based connector system, Scotchlink Connector Tape has a dielectric backing that consists of 0.001-in. (0.250-mm) polyester film. Overall thickness with conductors and conductive adhesive is approximately 0.003 in. (0.075 mm). The system can replace conventional flexible circuits, elastomeric connectors, and flat ribbon cables tying into components such as LCDs and membrane keyboards. Two spacings are currently offered: Scotchlink H-254 with conductors on 0.100-in. (2.540-mm) centers and H-200 with conductors on 0.079-in. (2.000-mm) centers. **3M, Electro-Products Div,** PO Box 33600, St Paul, MN 55133.



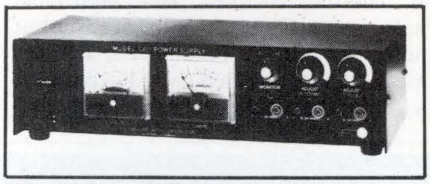
Circle 386

Switching power supply features 75 percent efficiency

In its most common configuration, model 4032 delivers 5 Vdc at 60 A, over an operating temperature of 0 to 71 °C with forced air cooling. Other output configurations are available from 2 Vdc at 70 A to 48 Vdc at 6.5 A. The standard input voltage is 115 ±15 percent, 47 to 440 Hz. With internal jumpers, 230 V ±15 percent is also an option. Input frequency is 47 to 440 Hz. Noise, ripple, and spikes are less than 100 mV peak to peak. Features include remote sensing capability, over voltage, and over current. **Ceag Electric Corp, Power Supply Div,** 1324 Motor Pkwy, Hauppauge, NY 11788.

Circle 387

Power supply offers three isolated floating parts



The triple model 1301 consists of a fixed 5-Vdc supply at 1 A and two 0.5-A, 5- to 18-Vdc, continuously adjustable supplies. The three outputs can operate independently or connect in series or parallel to provide up to 18 Vdc at 1 A or up to 41 Vdc at 0.5 A. Features include a front-panel ammeter (1 A full scale) and voltmeter (20 Vdc full scale). Current limiting protects against short circuits and overloads. **Global Specialties Corp,** 70 Fulton Terr, PO Box 1942, New Haven, CT 06509.

Circle 388

Multiple-output switchers use heat sinking approach

Multiple output P90s are 90-W switched mode supplies built to industry standard 8.25- x 4.25- x 2-in. packaging. Model 401 provides ±5 V and ±12 V, with the 12-V output surge rated for Winchester disk or tape drives. Model 402 has 5, 24, and ±12 V, with the 24-V surge rated for Winchesters and the 12-V tightly regulated with low noise for power CRTs. Model 403 has 5, 12, 12, and −12 V. One 12-V output is surge rated, while the other is designed for flicker-free CRT operation. Prices range from $68 to $116 each in 1000s. **Conver Corp,** 10629 Bandley Dr, Cupertino, CA 95014.

Circle 389

SYSTEM ELEMENTS

Motor features 400 steps per revolution on 4 in.

The motor produces twice the number of steps per revolution as standard hybrid permanent-magnet stepping motors. Full step angle is reduced from 1.8 to 0.9 degrees. The unit uses a high efficiency laminated and bonded rotor. Step-angle tolerance is ±3 percent, noncumulative. The two-phase/8-lead unit is compatible with standard unipolar and bipolar drivers. Torque ratings are comparable to equivalent-sized, 200-step motors. The design is also available as a synchronous motor, which produces 36 rpm at a 60-Hz line frequency. **Sigma Instruments, Inc,** 170 Pearl St, Braintree, MA 02184.

Circle 390

BiFET op amp lowers cost of high precision circuit design

The AD611KH delivers maximum offset voltage and offset voltage drift of 0.5 mV and 10 μV/°C, respectively. Guaranteed maximum input bias of current is 50 pA. Specs include minimum slew rate of 8 V/μs, typical gain bandwidth of 2 MHz, and settling to 0.01 percent in 3 μs. Performance ensures wide bandwidth and 12-bit accuracy in high speed buffer circuits. Other specs include typical voltage noise of 2 μV peak to peak (0.1 to 10 Hz), 0.0025 percent harmonic distortion, and minimum open-loop gain of 94 and 90 dB for the K and J grades. Prices are as low as $1 in 100s. **Analog Devices, Inc,** Rte 1 Industrial Park, PO Box 280, Norwood, MA 02062.

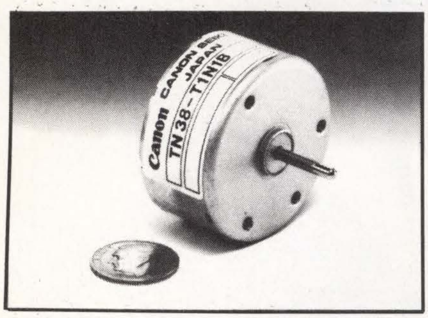
Circle 391

Crystal clock oscillators span wide frequency range

The DS-C308 series offer frequencies as low as 0.5 Hz and as high as 16 MHz. Four types are available with the A and B models offering a frequency range of 0.5 to 64 Hz but differing in tolerance, stability, and operating temperature range. The A and B operate from a 5-Vdc supply and require 10 mA maximum input current. Output voltages are 4.2 Vdc minimum for a logic one and 0.2 Vdc maximum for logic zero. Rise and fall times equal 1 μs maximum with 50 pF of load capacitance. **Seiko Instruments USA,** 2990 W Lomita Blvd, Torrance, CA 90505.

Circle 392

Slimline motor saves space without sacrificing function



The TN38 dc motor measures 19 x 38 mm but provides high power and smooth rotation with low cogging. Typical applications are in VTRs, portable VTRs, computer peripherals, and other places where space is a factor. Rated voltage is 12 V, rated torque is 30 g-cm, rated speed is 3800 rpm, and rated current is 170 mA. No-load speed is 4350 rpm and no-load current is 60 mA. Starting torque is 225 g-cm. The unit weighs 65 g. **Canon USA, Inc, Electronic Components Div,** 1 Canon Plaza, Lake Success, NY 11042.
Circle 393

Monitor's display format is vertical or horizontal

Designed for high density display of up to 6000 characters, the HD series offers 15- and 17-in. screens. They are capable of either standard video for bright characters on a dark background, or inverted video for dark characters on a light background. Features include clear corner resolution, resulting from dynamic and static focusing coupled with an improved CRT and yoke combination. Line rates are from 26 to 36 kHz. **Ball Corp, Electronic Systems Div,** PO Box 43376, St Paul, MN 55164.
Circle 394

Solderless mounted reed relays switch multiple circuits

The series 100/50 are 50- and 100-pole reed relays for high speed multiple circuit transfer. They offer switching of up to 100 poles simultaneously. Each reed switch mounts in a solderless contact mounting on the PC board for quick replacement. High test voltage capabilities are up to 500 Vdc and carry of up to 1 A. Applications include automatic test equipment, telecommunications, peripherals, and data processing. **Interconnect Devices, Inc, Relay Components Div,** 204 N 6th St, Kansas City, KS 66101.
Circle 395

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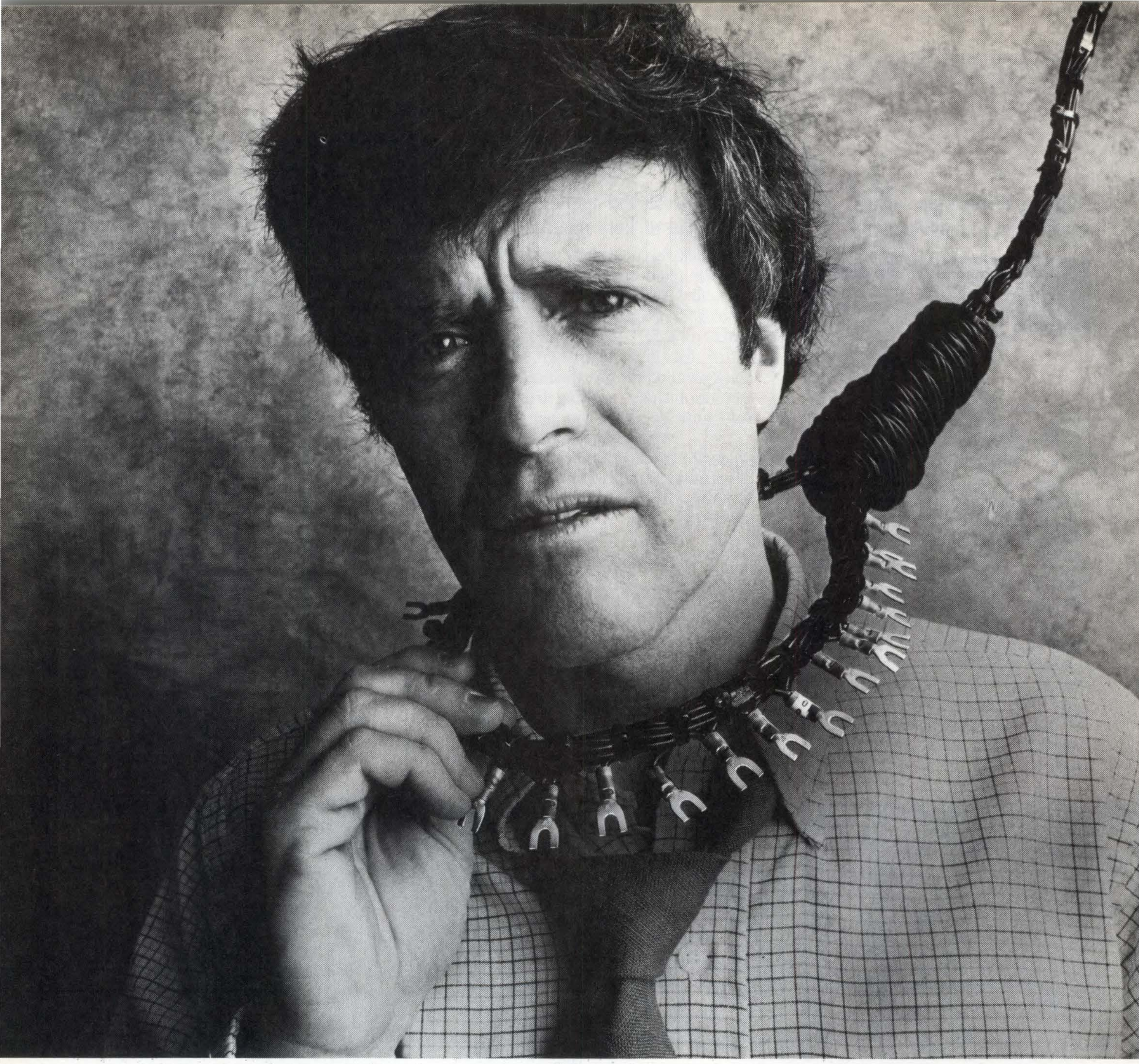

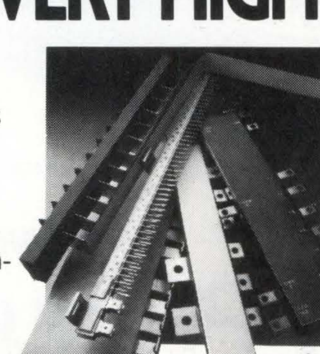

Analog CMOS/DMOS switches have ±10-V output range

The CDG308 and 309 combine high speed CMOS with lateral DMOS to handle signals from dc through video frequencies. The switching devices have at least 10 dB better cross talk and isolation than existing ICs. Specifications include glitch-free operation, cross-coupling rejection ratio of 70 dB at 10 MHz, and off-isolation rejection ratio of 80 dB at 10 MHz. In 100s, cost is $3.90. **Semi Processes, Inc,** 1971 N Capitol Ave, San Jose, CA 95132.
Circle 396

High speed programmable arrays offer 4-ns propagation delays

The bipolar ECL family is programmed on standard PROM equipment. Logic functions are customized by blowing fusible links to configure AND and OR gates. The PLA transfer function is sum of products with a single array of fusible links. It provides variable I/O pin ratio and registers with feedback on future parts. The first member of the family (DMPAL16P8) offers 16 inputs, programmable outputs, and 64 product terms. **National Semiconductor Corp,** 2900 Semiconductor Dr, Santa Clara, CA 95051.
Circle 397

Programmable op amp designed for high gain application

The OP-32 offers precision performance for high gain applications. A single external resistor sets supply current to any value from 1 μA to 2 mA. This allows each amp to be set for minimum power consumption. At a 1-mA supply current, gain bandwidth is 10 MHz. Features include low input offsets, high gain, and high common mode rejection ratio (>100 dB). The chip is fully specified and characterized for operation from a supply voltage of 3 to 30 V. In 100-piece quantities, the military version is priced from $7 and the industrial version from $2.25. **Precision Monolithics Inc,** 1500 Space Park Dr, Santa Clara, CA 95050.
Circle 398

Quad-CMOS version bit-slice processor expands IC line

Power dissipation for the IMI 4X2901B is 175 mW, less than one-tenth that for a single bipolar four-bit slice. Fully TTL compatible on both inputs and outputs, the chip consists of a 16- x 16-bit; two-port RAM, a 16-bit high speed ALU, a 16-bit Q register, and associated circuitry. In addition, the bit slice includes a 2902 lookahead and carry circuit onchip. The cascadable device has three-state outputs and various status flag outputs for the ALU. **International Microcircuits, Inc,** 3350 Scott Blvd, Santa Clara, CA 95051.
Circle 399

Floating point chip set benchmarks 8 MFLOPS

Designed for use in high speed floating point processors, the WTL 1032-8 multiplier and the 1033-8 ALU are IEEE 754 compatible. The full-function chip set features add, subtract, multiply, and absolute value capabilities, as well as conversion to and from 24-bit fixed-point arithmetic. The chips can operate in either pipeline or flow-through modes. Data I/Os transfer at twice the pipeline rate so two 16-bit inputs and one output operation occurs every 60 ns. Circuits are individually priced at $442 each or $884 per set in 100s. **Weitek Corp,** 501 Mercury Dr, Sunnyvale, CA 94086.
Circle 400

Uncommitted logic array mixes precision with performance

The TMG6004 converter is a silicon-gate CMOS semicustom array. The architecture supports both A-D and D-A conversion. Specs in the precision analog range are op amp offset voltage of 2 to 5 mV, op amp noise of 10 μV, op amp bandwidth of 5 MHz, and buried Zener of 7 V. Components include 22 low noise op amp comparators, 4 Zener diodes, 52 switches, 512 capacitors, and 40 flipflops. The device is TTL compatible, operates from a 2- to 10-V power supply, and has 62 I/O pads. **Telmos Inc,** 740 Kifer Rd, Sunnyvale, CA 94086.
Circle 401

GaAs shift register with onchip decoder clocks 1.4 GHz

Based on GaAs technology, the HMD-11141-1 performs shift right, shift left, serial/parallel I/O, and hold operations using an onchip decoder. Inputs and outputs are matched for use with 50-Ω impedance systems (35 to 65 Ω). Both the shift register and divider come individually housed in hermetic, metal-glass flatpacks. The register contains four clocked D flipflops with individual I/Os for parallel operation. Prices in 100s are $393 each. **Harris Microwave Semiconductor,** 1530 McCarthy Blvd, Milpitas, CA 95035.
Circle 402

Dynamic RAM controllers access 16, 64, and 256 Kbits

Designated SN74S408/408-2/409/409-2, the 48-pin controllers feature 160- and 130-ns access times. The 408 controllers have eight address outputs and can directly drive and address all 16- and 64-Kbit DRAMs. The 409s have 9 address outputs and drive 256-Kbit versions, addressing up to 1 Mwords. The chips consist of two address latches, refresh counter, and necessary control logic and drive functions. The 408 has three access modes, one refresh mode, and two setup modes. The 409 contains two additional refresh modes. Controllers range in price from $26.07 to $32.78 each in 100s. **Monolithic Memories, Inc,** 2175 Mission College Blvd, Santa Clara, CA 95050.
Circle 403

Dual-port memory unit contains registers for access control

The 8-bit RAM MC68HC34 enables two processors operating on separate buses to easily exchange data. Registers are available to allow each processor to interrupt the other. The chip contains six read/write semaphore registers that control access to the RAM. Each register arbitrates simultaneous accesses with no ambiguities. Simultaneous reads result in proper data going to both processors. In quantities of 1000, prices are $25. **Motorola Inc, MOS Microprocessor Div,** 3501 Ed Bluestein Blvd, Austin, TX 78721.
Circle 404

Core microcontroller is standard cell for custom designs

The 80C49 core is part of the ZyP standard-cell library for customizing Intel microcontrollers. The 8-bit 8049 family is used in industrial control, keyboards, robotics, and peripherals. The custom designed unit will be attractive to customers who use more than 20,000 standard versions of the microcontroller per year. With the Zyp system, users can design custom VLSI circuits without an extensive knowledge of circuit design. **ZyMOS Corp,** 477 N Mathilda Ave, Sunnyvale, CA 94088.
Circle 405

Family of EEPROMs comes with high density serial device

The 64- x 16-bit 59308 uses a single 5-V power supply for all modes of operation. An onchip voltage generator enables programming without external high voltage supplies. Standby power consumption is 25 mW. The chip supports four instructions—read, write, word erase, and block erase. The erase and write operations are self-timed with a ready/busy indication through the data output pin. Other characteristics include a 500-kHz clock rate, complete TTL compatibility, and 8-pin packaging. In 100s, price is $7.50 each. **NCR Microelectronics Div,** 8181 Byers Rd, Miamisburg, OH 45342.
Circle 406

June will be a two-issue month—*watch for Special Reports on Microprocessors and Microcomputers—Part 1 on June 1, Part 2 on June 15*

Announcing the WY-75.

Our new WY-75, VT-100 software-compatible terminal has a style that's truly impressive.

It offers a combination of features you can't find in any other VT-100 software-compatible terminal. Like a compact, ergonomic design. A sculpted, low-profile keyboard. And a swivel and tilt non-glare 14" screen, tailored with an 80/132 column format.

Priced in a class by itself, the WY-75 lists for only $795.

Contact Wyse Technology for more information. And discover a great new outfit.

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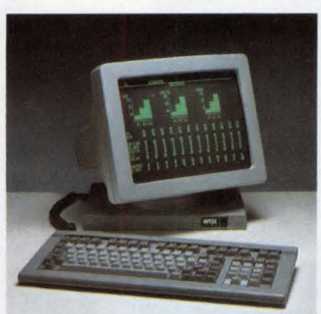

WYSE

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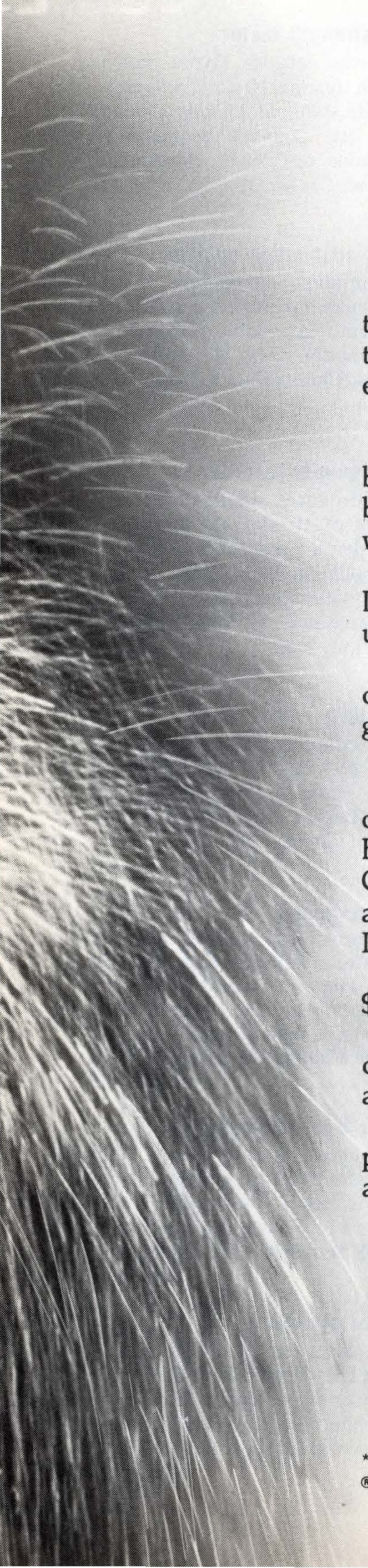
Our UNIX Micro
GE's Industrial

Systems Fine-Tune DC Motors.



We're Dual Systems.

And when the people at GE needed a microsystem as an engineering design tool for industrial DC motor applications, they turned to us.

After all, our high speed microsystems have performed in the clutch for Boeing and Sony and Ford and United Press International, just to name a few.

And for three years we've been delivering 68000-based systems, full UNIX* Version 7 with Berkeley enhancements, and IEEE-696/S-100 bus conformance. That's longer than anyone else.

Which brings us to our newest high-performance micro, the 83/80. Featuring the full UNIX capabilities of Version 7 or System III, the 83/80 can handle up to twelve users and provides a standard 512 KB of dynamic RAM with parity that's expandable to 3.25 MB.

And we've backed it with a full one-year warranty.

Our 83/80 incorporates a high-throughput SMD controller and an 80 megabyte Winchester disk drive with 20-25 milliseconds average seek time. And our backup memory is well worth remembering — it consists of an 8" floppy disk with 1 MB of storage.

In addition, you'll find our 83/80 delivers increased performance through its Dual ported full-track disk buffer and proprietary controller circuiting. More users can access with better response time.

It's also very well-educated. Our 83/80 can read or write up to an entire track of data in a single disk rotation, regardless of where the disk-head settles on a given track.

That's smart.

The C programming language comes standard with UNIX, of course. Other optional languages include FORTRAN-77, PASCAL, RM/COBOL®, LISP and BASIC. And that's just for starters.

Optional software includes data base and administrative packages like INGRES and UNIFY.

And the sticker price? Quantity 10 at $14,693.

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We'll be glad to tell you about one powerful microsystem that's revved up and ready-to-go.

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CIRCLE 145

Comprehensive CMOS data

CMOS reference contains data sheets for over 395 items, including 250 microCMOS products; organized into 16 sections, the data book includes section and alphanumeric indexes. **National Semiconductor Corp,** Santa Clara, Calif.
Circle 410

Software products

A 200-page directory offers more than 2000 software products for microprocessors and systems; two cross-referenced sections contain alphabetical listings of companies with product and service details. **Intel Corp,** Santa Clara, Calif.
Circle 411

Approved ANSI standards

Catalog lists approximately 8000 ANSI-approved standards in sections categorized by title and designation. Price is $10 for nonmembers; free to members. **American National Standards Institute, Inc, Communications Dept,** 1430 Broadway, New York, NY 10018.

Standards and engineering

Over 600 different standards and publications for electronic components and equipment developed by over 250 standing committees are contained in catalog; prices and detailed ordering information for all EIA documents listed are included. Catalog is free to EIA members and $5 for nonmembers. **EIA Standards Sales Supervisor, Electronic Industries Assoc,** 2001 Eye St NW, Washington, DC 20006.

Standard stepper motors

Catalog profiles units appropriate for such applications as floppy and rigid disk drives, printers, and plotters; typical step angles of 0.9, 1.8, 3.6, and 3.75 degrees, and frame sizes of 17 (39 mm) and 23 (57 mm), are featured. **Shinano Kenshi Co, Ltd,** North Hollywood, Calif.
Circle 412

Interference control

Forty-page booklet lists protective devices for microcomputer equipment; products include isolators, ac power line filter/suppressors, line voltage regulators, ac power interrupters, and modem protectors. **Electronic Specialists, Inc,** Natick, Mass.
Circle 413

Dot-matrix printers

Data sheets describe Durawriter and Formwriter series 80- and 132-col dot-matrix printers; features include simple design and high performance components. **Digital Matrix Corp,** Bloomfield, Conn.
Circle 414

Electronic test equipment

Catalog contains information on newest advanced electronic test equipment, such as oscilloscopes, logic analyzers, and counter/timers; pictures and diagrams accompany text. **Philips Test & Measuring Instruments, Inc,** Mahwah, NJ.
Circle 415

Bilingual chart

English and French chart lists types of equipment and system suppliers for electrical installations; alphabetical listings of members in the French Electrical Equipment Assoc and Industrial Electronics Manufacturers Assoc include full addresses and are tabulated by 30 product divisions. **Gimelec,** Paris, France.
Circle 416

Capacitor engineering

Application chart and engineering guide list full specs for devices rated from 0.001 to 500 mF, 50 to 200 kVdc, in a range of film types; typical uses include power supplies, energy storage, motor drives, laser and plasma power, and high frequency applications. **Film Capacitor, Inc,** Passaic, NJ.
Circle 417

Dielectric strength tester

Brochure gives data on Hypot model 4040A, which features 0 to 3 kV continuously adjustable at 25 mA, ground continuity test, auto-test sequencing, and detachable test leads. **Associated Research, Inc,** Skokie, Ill.
Circle 418

Video data acquisition system

Four-page product selection/designer's guide introduces the fully programmable PC-EYE System 1000, capable of digitizing video information from EIA RS-170 or NTSC sources. **Chorus Data Systems, Inc,** Hollis, NH.
Circle 419

Sequential events recorder

Brochure introduces standard features and options of Betalog 128 sequential events recorder, a 128-point capacity unit that has touchpad front plate for inquiries on system status as well as keyboard for programming. **Beta Products, Inc,** Carrollton, Tex.
Circle 420

Electronic disk

Color folder describes and specifies a 368-Kbyte capacity memory board that emulates an IBM PC or XT floppy disk drive. **Distributed Logic Corp, Dilog PC Products,** Garden Grove, Calif.
Circle 421

Digital force gauge

Four-page brochure describes features and applications of model DFG for electronic measurement of tension and compression forces; specs cite 10- and 100-lb capacity units, as well as companion 2-lb model. **John Chatillon & Sons Inc,** Kew Gardens, NY. **Circle 422**

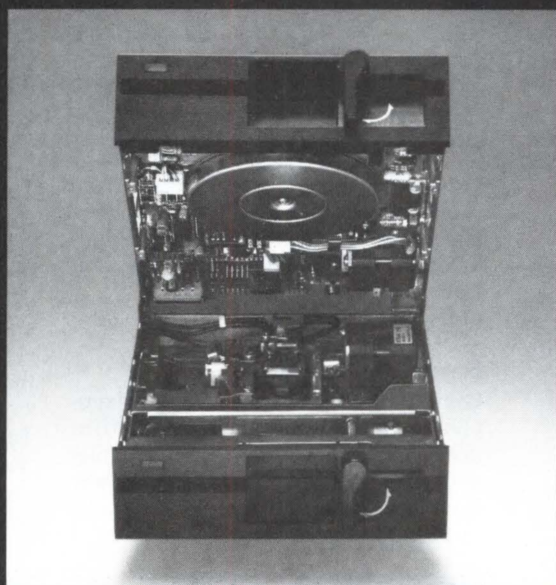
Winchester 8-in. technology

Color brochure highlights 11- to 47-Mbyte series D6011/D6023/D6047 and 48- to 84-Mbyte series D6048/D6084 high-performance 8-in. Winchester disk drives. **Thorn EMI Datatech Ltd,** Middlesex, England. **Circle 423**

Chip carrier sockets

Brochure describes 61 designs of 3M/Textool chip carrier sockets for test and burn-in; improved design features increased latching area, compliant pressure pad, and built-in lid stop. **3M,** St Paul, Minn. **Circle 424**

TAKE ONE FOR A TEST DRIVE.



Introducing the 1984 TEACS.

A full line of 5¼ inch half-high flexible disk drives. Available in single/double sided, 48 tracks per inch/96 tracks per inch, single/double density.

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CIRCLE 146

Fiber optic sensing
Twenty-six page technical brochure outlines general principles and definitions of incandescent and infrared photoelectric controls and fiber optic theory; application notes, glossary of terms, and speed calculation chart accompany text. **Dolan-Jenner Industries, Inc,** Woburn, Mass.
Circle 425

Modular terminal blocks
Six-page folder tabulates series 5000 dimensions, wire capacities, and electrical ratings for a broad selection of standard rail mounting terminals in capacities to 00 AWG; series fits DIN 1, DIN 3, and CENELEC rails interchangeably. **Entrelec, div of Cogenel, Inc,** Spring Valley, NY.
Circle 426

Iris updates
Newsletter written by and for Iris users includes a write-in forum, people and software information, product overviews, and Iris updates. **Point 4 Data Corp,** Irvine, Calif.
Circle 427

Thin-film recording heads
Two-page data sheet for Cyber 100 series of thin-film recording heads describes units for sub-5-through-8-in. Winchester disk drives that operate on thin-film or oxide-coated media; drawings and photos are included. **Cybernex Corp,** San Jose, Calif.
Circle 428

Test instruments
Full-color catalog of high performance instrumentation is divided into six categories: oscillographic recorders, image recorders, signal-conditioning units, magnetic tape systems, industrial systems, and special products; each product is described and illustrated. **Honeywell Inc, Test Instruments Div,** Denver, Colo.
Circle 429

Step/repeat alignment system
Illustrated brochure describes the SRA-100 step-and-repeat alignment system, which throughputs 45 to 60, 100-mm wafers/hour; features include high resolution, overlay accuracy, and productivity. **Perkin-Elmer Corp,** Wilton, Conn.
Circle 430

Data interface cables


Expanded catalog details data interface cables and additional accessories; power line protection ranging from surge eliminators to UPSs is summarized. **Data Set Cable Co,** Ridgefield, Conn.
Circle 431

Engineering handbook
Over 700 linear and switching power supplies and dc/dc converters are specified in engineering handbook; selection tables and glossary are included. **Power Products Group,** Pompano, Fla.
Circle 432

Signal-conditioning system
System 616, a 16-channel programmable electronic filter system with 5-bit resolution, is profiled through graphics, filter specs and feature descriptions. **Precision Filters, Inc,** Ithaca, NY.
Circle 433

Series interface units
Publications covering series Q-1000 and Q-3000 series interface units illustrate and detail functions of various models in each line; general specs and operational schematics are included. **Quasitronics, Inc,** Houston, Pa.
Circle 434

Catalog of computer books
Publisher's guide to over 50 computer science books and software. Covers system analysis and management, as well as language-specific programming references. **Little, Brown and Co,** Boston, Mass.
Circle 435

Design products for PC boards
Twenty-page illustrated brochure highlights latest advances in state-of-the-art PC board design and drafting products; dual-inline, subminiature, silkscreen component, and multi-trace patterns are included. **Bishop Graphics, Inc,** Westlake Village, Calif. **Circle 436**

Advanced Lisp computer
Brochure details LMI Lambda, which configures with Lisp and Unix coprocessors along with extended Zetalisp software; the computer's features include integral Multibus and optional Ethernet II interface. **LISP Machine, Inc,** Los Angeles, Calif. **Circle 437**

Technology references
Brochure details 59 books and journals covering a wide range of subjects, including software technology, data communications, graphics, system design, automated manufacturing, robotics, and electronics. **North-Holland,** Amsterdam, the Netherlands. **Circle 438**

Technical and design data
Two pages of technical and design data focus on medium resolution in a very small optical encoder; options accommodating different mechanical and electrical interfaces and two outline drawings are provided. **Itek, Measurement Systems Div,** Newton, Mass. **Circle 439**

Test accessories
Electronic test accessories reference features specs and photos of 817 products, including order and price information. **ITT Pomona Electronics Div,** Pomona, Calif. **Circle 440**

Heat sinks
Catalog on heat sinks and accessories covers products designed to plug-in, slide on, fasten or glue to semiconductor devices. **AAVID Engineering,** Laconia, NH. **Circle 441**

Microcircuit packages
Catalog features all-metal, flat microcircuit packages in one-piece construction and gold-plated per MIL-G-45204; variety of package sizes measures 0.375 x 0.500 in. to 1.600 x 1.600 in. **Airpax Corp,** Cheshire, Conn. **Circle 442**

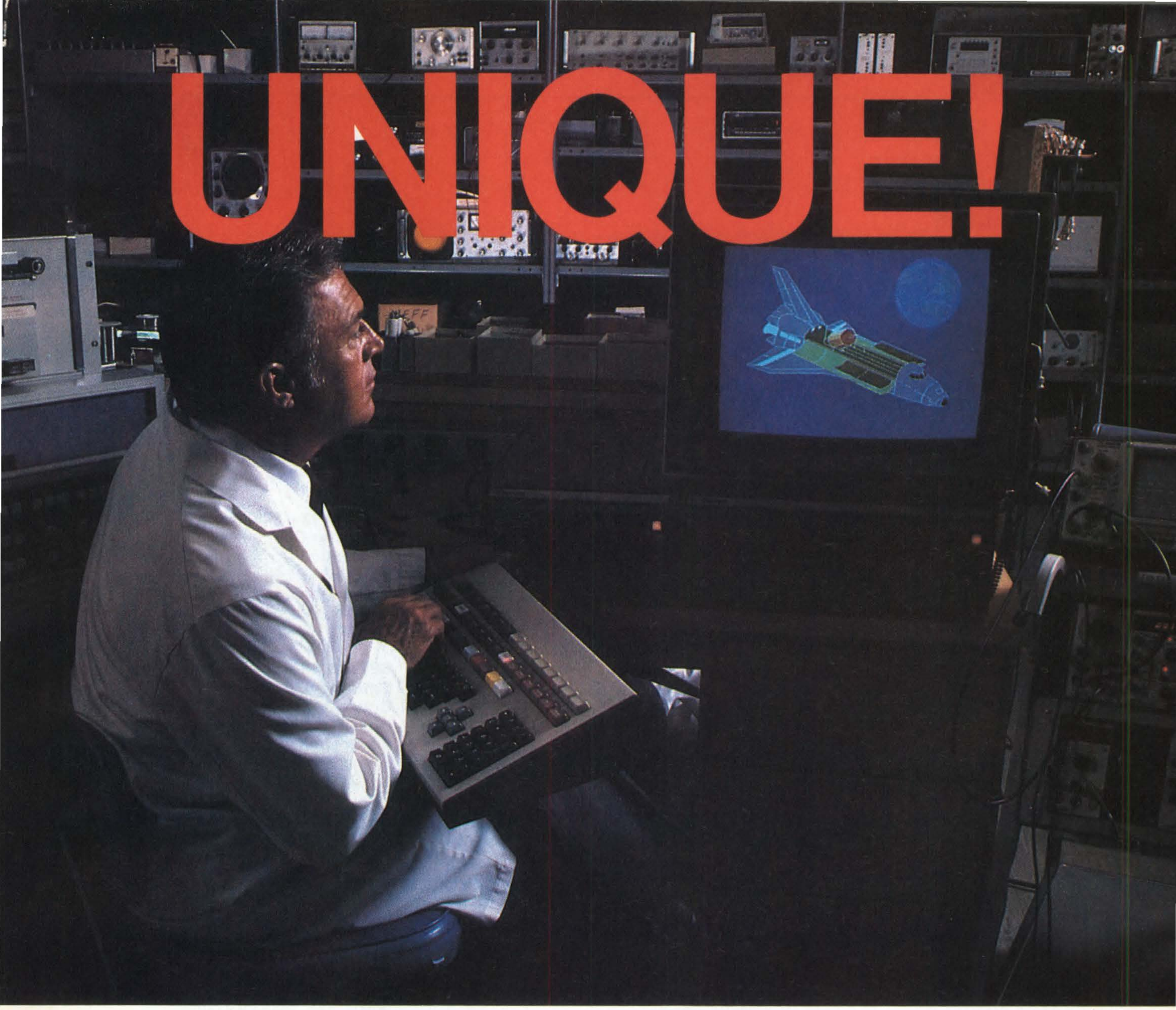

Photo courtesy Chromatics, Inc.

CONFERENCES

JUNE 4-7—Robots 8 Conf and Expo, Cobo Hall, Detroit, Mich. INFORMATION: Patricia Van Doren, Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121. Tel: 313/271-1500

JUNE 4-8—SID (Society for Information Display Internat'l Symposium), San Francisco Hilton, San Francisco, Calif. INFORMATION: Lewis Winner, 301 Almeria Ave, Coral Gables, FL 33134. Tel: 305/446-8193

JUNE 5-7—Internat'l Symposium on Computer Architecture, Rackham Building, Ann Arbor, Mich. INFORMATION: Keki Irani, ECE Dept, Univ of Michigan, Ann Arbor, MI 48109. Tel: 313/764-8517

JUNE 5-7—Symposium on Mass Storage Systems, Marriott Mark Resort, Vail, Colo. INFORMATION: Bernard O'Lear, NCAR, PO Box 3000, Boulder, CO 80307.Tel: 303/494-5151

JUNE 6-8—American Control Conf, Hyatt Islandia, San Diego, Calif. INFORMATION: Herb Rauch, Lockheed 52-56/205, Palo Alto Research Lab, 3251 Hanover St, Palo Alto, CA 94304. Tel: 415/493-4411 X5677

JUNE 6-8—Communications Architectures and Protocols, Montreal, Canada. INFORMATION: Rebecca Hutchings, Honeywell/FSD, 7900 Westpark Dr, McLean, VA 22102. Tel: 703/827-3982

JUNE 19-22—Internat'l Symposium on Fault Tolerant Computing, Hyatt Orlando, Orlando, Fla. INFORMATION: Richard Sedmak, Sperry Univac, PO Box 500, MS C1SW12, Blue Bell, PA 19404. Tel: 215/542-3638

JUNE 20-22—Internat'l Conf on Computers and Applications, Fragrant Hill Hotel, Beijing (Peking), China. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JUNE 21-22—VLSI Multilevel Interconnection (V-MIC) Conf, Hotel Intercontinental, New Orleans, La. INFORMATION: Thomas Wade, Microelectronics Research Lab, Electrical Engineering Dept, PO Drawer EE, Mississippi State, MS 39762. Tel: 601/325-3721

JUNE 24-27—Design Automation Conf, Albuquerque Convention Ctr, Albuquerque, NM. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 9-12—NCC (National Computer Conf), Las Vegas Convention Ctr, Las Vegas, Nev. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

JULY 23-25—Computer Simulation Conf, Copley Plaza Hotel, Boston, Mass. INFORMATION: Society for Computer Simulation, PO Box 2228, La Jolla, CA 92038. Tel: 800/225-7654

JULY 23-27—SIGGRAPH Conf on Computer Graphics and Interactive Techniques, Minneapolis, Minn. INFORMATION: Lynn Valastyan, 111 E Wacker Dr, Chicago, IL 60601. Tel: 312/644-6610

JULY 30-AUG 2—Internat'l Pattern Recognition Conf, Montreal, Canada. INFORMATION: ICPR Secretariat, 3450 University St, Montreal, Quebec, Canada H3A 2A7. Tel: 514/392-6744

AUG 12-15—Computers in Engineering Conf and Exhibit, Las Vegas Hilton, Las Vegas, Nev. INFORMATION: Mary Benedict, American Society of Mechanical Engineers, 345 E 47th St, Suite 13M, New York, NY 10017. Tel: 212/705-7100

AUG 19-24—Technical Symposium on Optics and Electro-Optics and Instrument Display, Town & Country Hotel, San Diego, Calif. INFORMATION: Rich Donnelly, Information Services, SPIE, PO Box 10, Bellingham, WA 98225. Tel: 206/676-3290

AUG 21-24—Conf on Parallel Processing, Hilton Shanty Creek, Bellaire, Mich. INFORMATION: Tse-yun Feng, 1604 Stormy Ct, Xenia, OH 45385. Tel: 614/422-1408

AUG 30-SEPT 1—Conf on Solid State Devices and Materials, Kobe, Hyogo, Japan. INFORMATION: Susumu Namba, Osaka Univ, Faculty of Engineering Science, Toyonaka, Osaka, Japan 560.

SEPT 5-8—Conf on Digital Signal Processing, Florence, Italy. INFORMATION: A. G. Constantinides, Dept of Electrical Engineering, Imperial College of Science & Technology, Exhibition Rd, London SW7 2BT, England. Tel: 01/5895111

SEPT 10-13—Advanced Control Conf, Purdue Univ, West Lafayette, Ind. INFORMATION: Edward Kompass, Editor, *Control Engineering* magazine, 1301 S Grove Ave, PO Box 1030, Barrington, IL 60010. Tel: 312/381-1840

SEPT 11-13—Electronic Imaging, Westin Hotel, Boston, Mass. INFORMATION: Morgan-Grampian Expositions Group, 2 Park Ave, New York, NY 10016. Tel: 212/340-9780

SEPT 11-13—Midcon Electronics Exhibition and Convention, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Mini/Micro-Southwest Computer Conf and Exhibition, Dallas Convention Ctr, Dallas, Tex. INFORMATION: Kent Keller, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

SEPT 11-13—Voice Input/Output System Applications Conf, Marriott Crystal Gateway Hotel, Arlington, Va. INFORMATION: Robert Burgess, Public Information Office, Lockheed Missiles & Space Co, Inc, Sunnyvale, CA 94086. Tel: 408/742-6688

SEPT 11-14—Unix Systems Expo, Los Angeles Convention Ctr, Los Angeles, Calif. INFORMATION: David Sudkin, Computer Faire, Inc, 181 Wells Ave, Newton, MA 02159. Tel: 617/965-8350

SEPT 16-20—Compcon Fall, Hyatt Regency Crystal City, Arlington, Va. INFORMATION: IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

SHORT COURSES

MAY 31-JUNE 1—Microelectronic Systems Interconnection and Packaging, George Washington Univ, Washington, DC. INFORMATION: Continuing Engineering Education, George Washington Univ, Washington, DC 20052. Tel: 202/676-6106

JUNE 6-8 and JUNE 27-29—Introduction to Design of Fault Tolerant Microcomputer Systems, San Francisco, Calif and Boston, Mass (respectively). INFORMATION: William Dries, Univ of Wisconsin-Extension, Engineering and Applied Science, 432 N Lake St, Madison, WI 53706. Tel: 800/362-3020

SEPT 6-8—Personal Computer and STD Computer Interfacing for Scientific Instrument Automation, Washington, DC. INFORMATION: Linda Leffel, C.E.C., Virginia Polytechnic Institute and State Univ, Blacksburg, VA 24061. Tel: 703/961-4848

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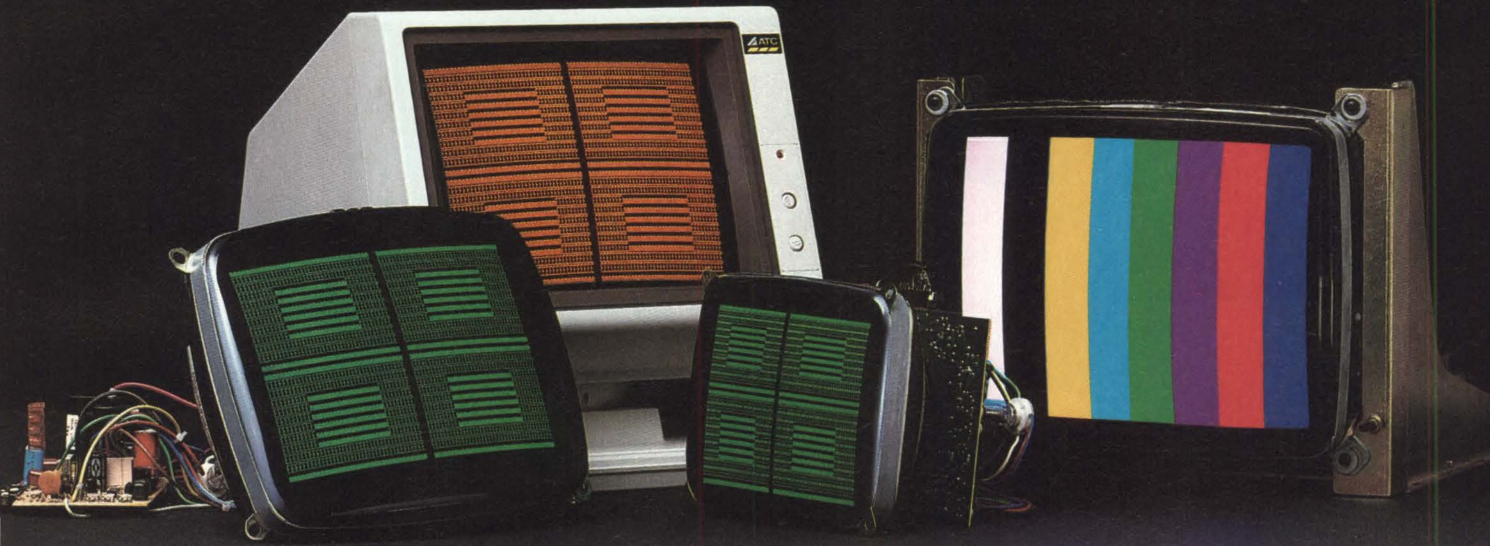

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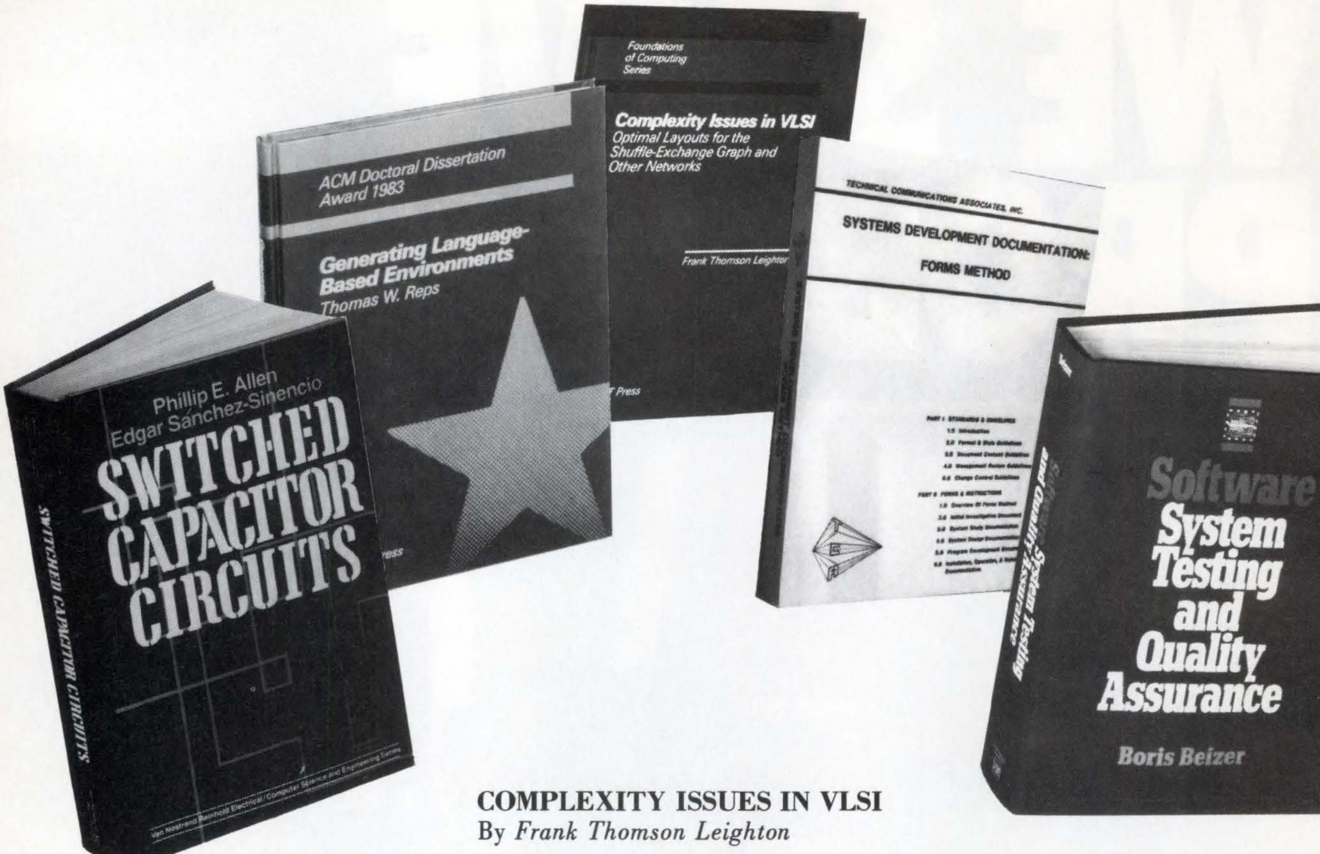

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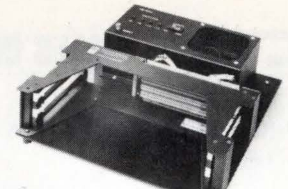

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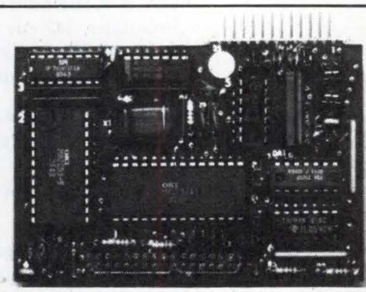

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6809
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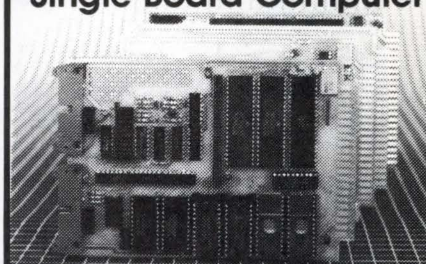

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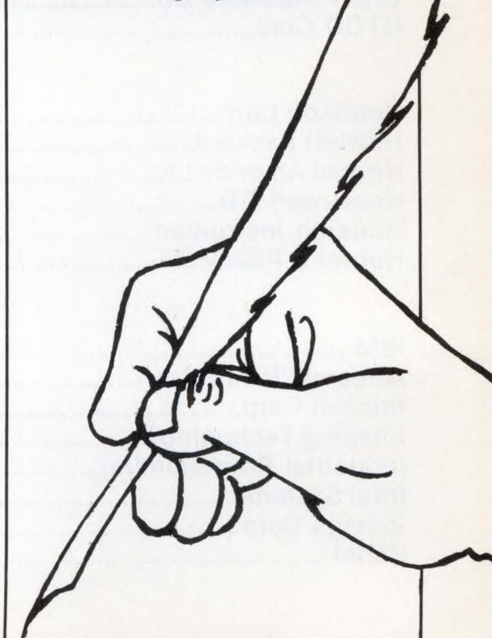

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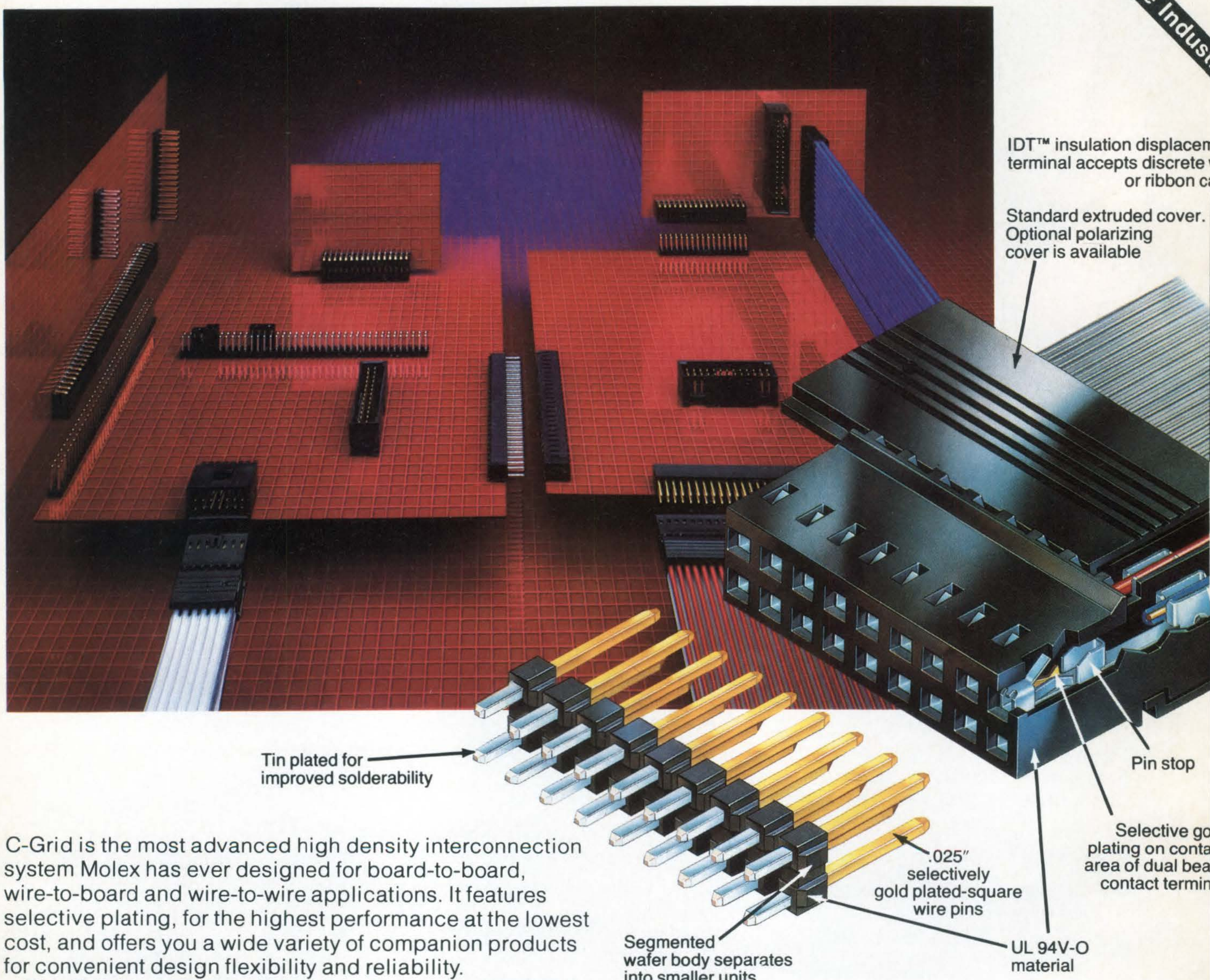

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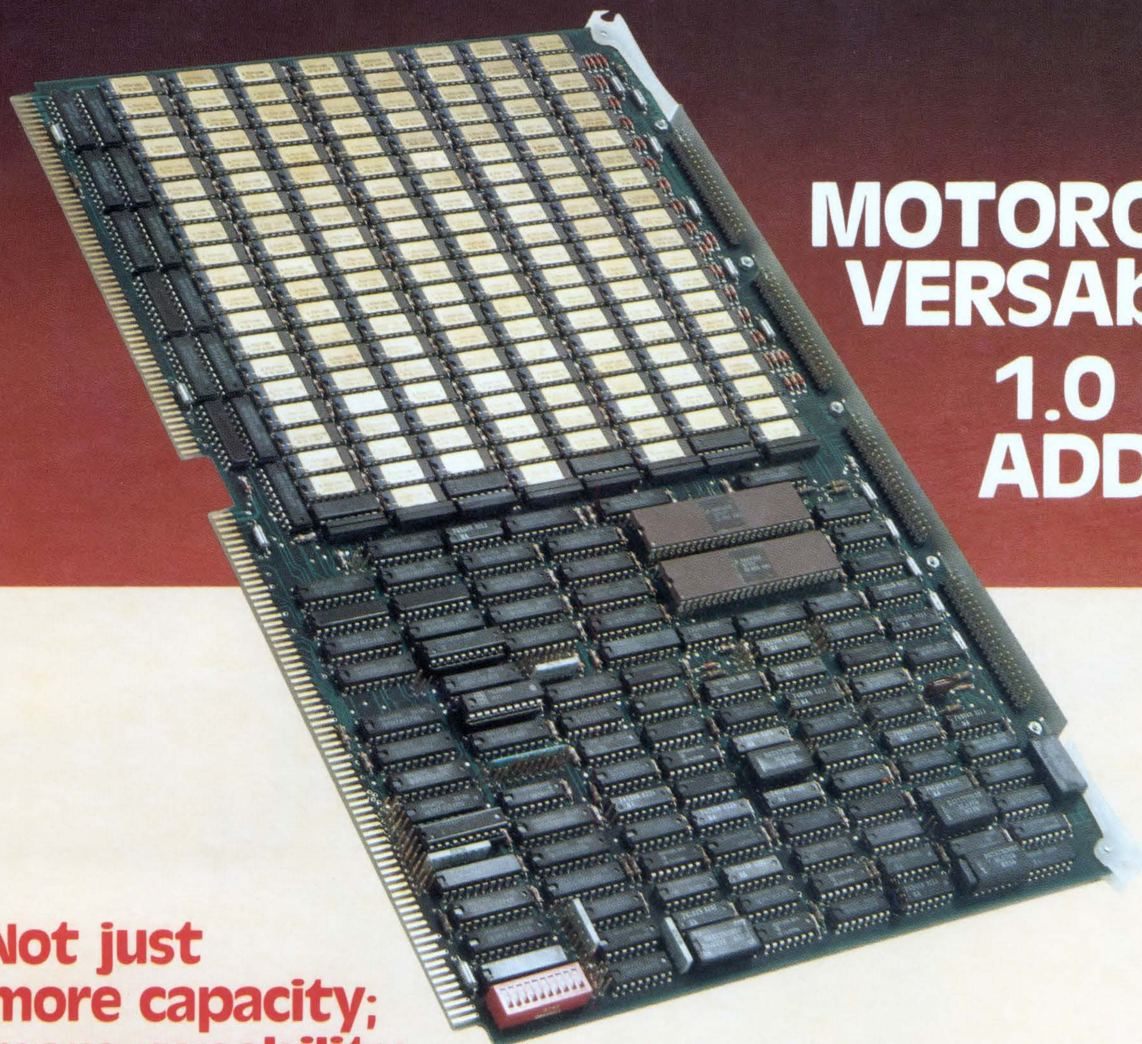

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