

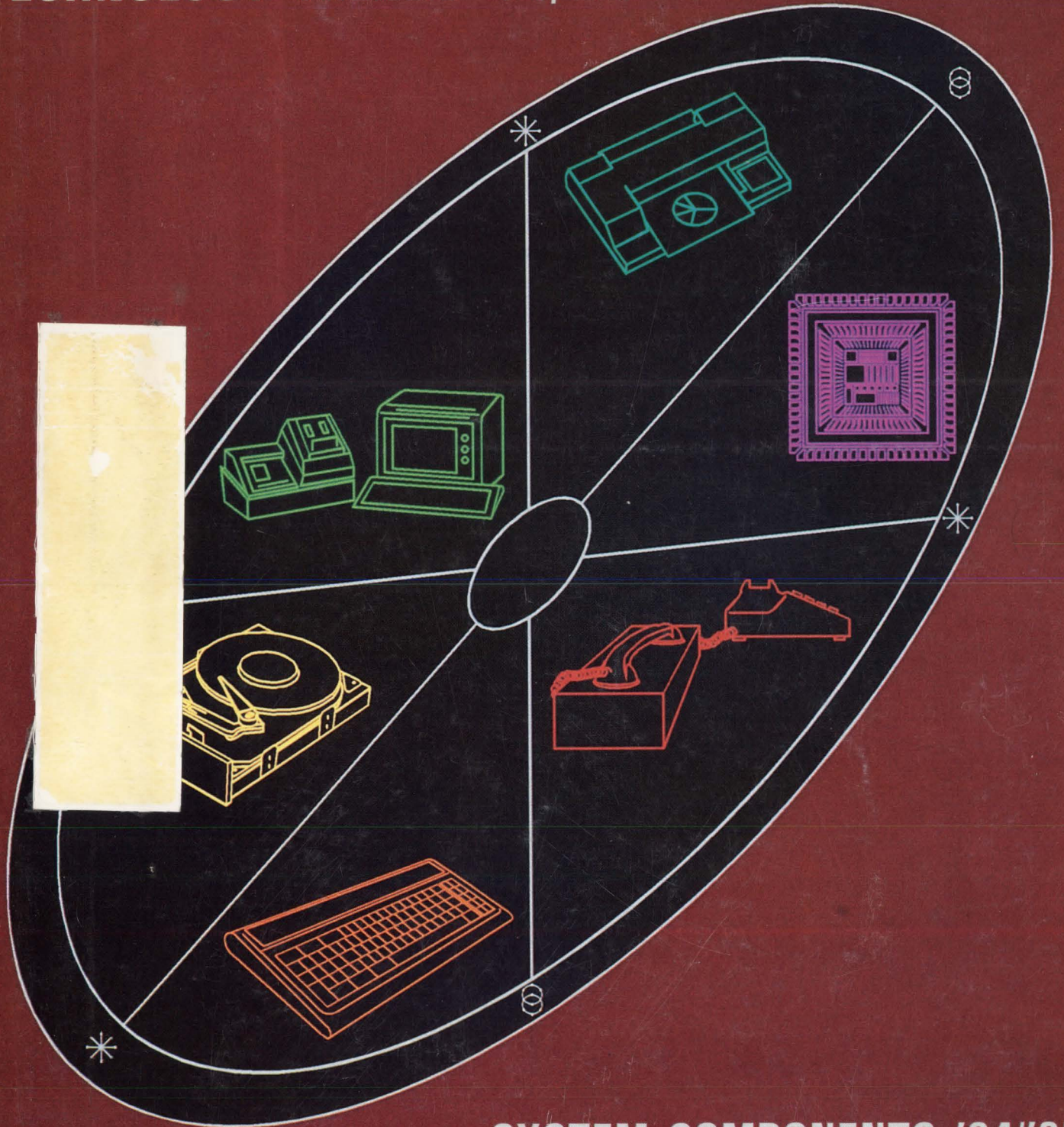
A PennWell Publication

DECEMBER 1984

# COMPUTER DESIGN

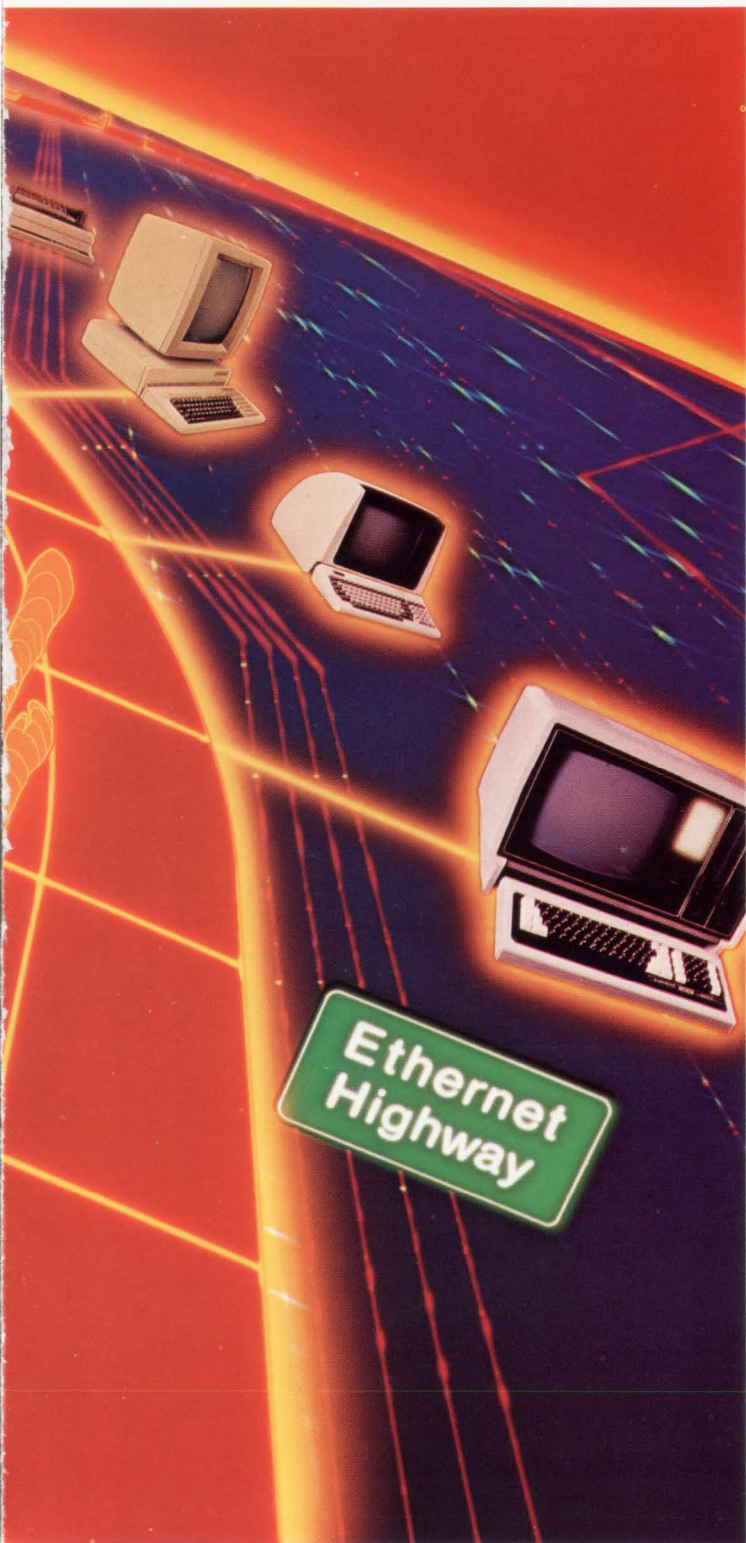
THE MAGAZINE OF COMPUTER BASED SYSTEMS

## TECHNOLOGY TRENDS '84/'85



## SYSTEM COMPONENTS '84/'85

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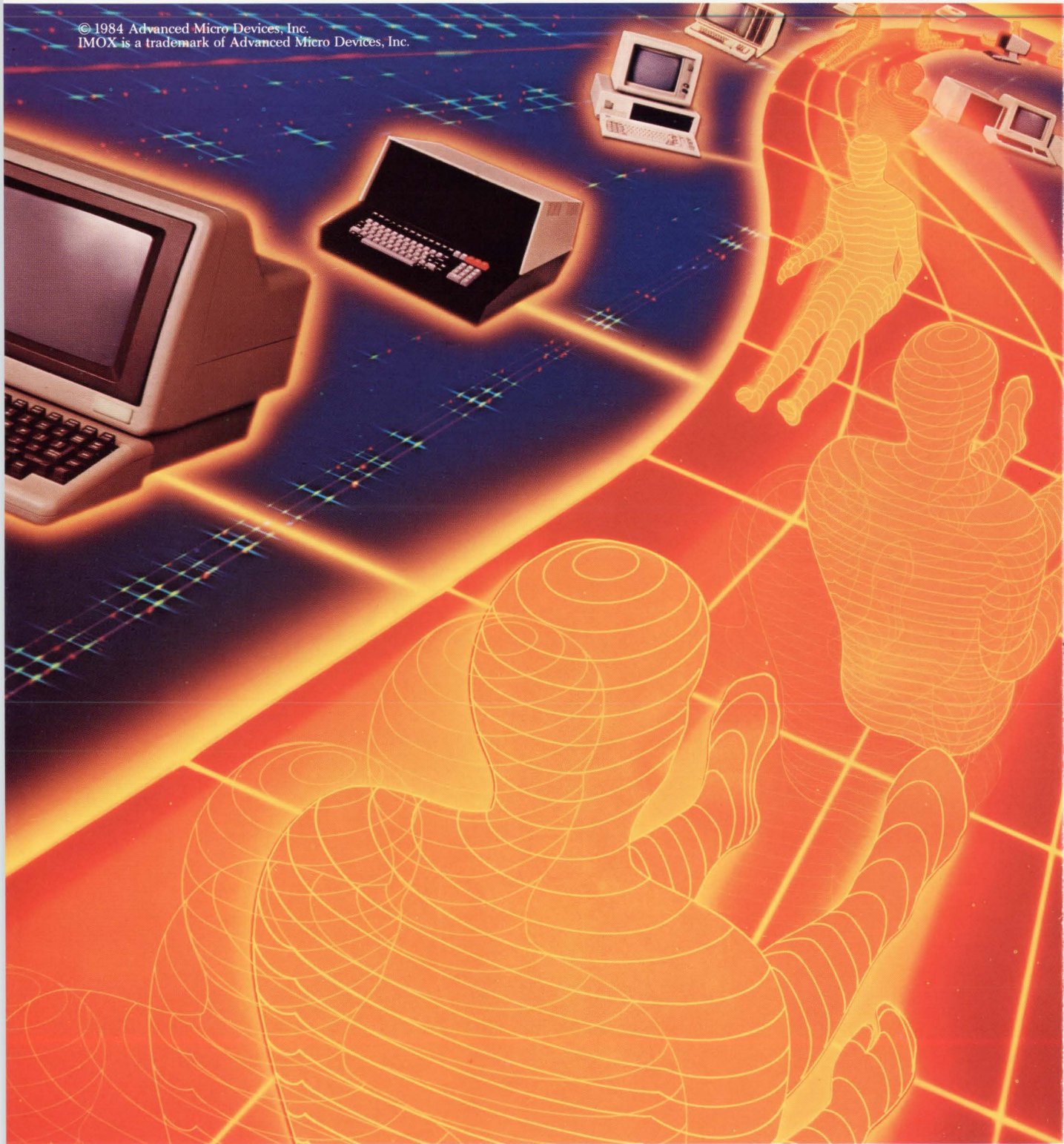
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CIRCLE 1

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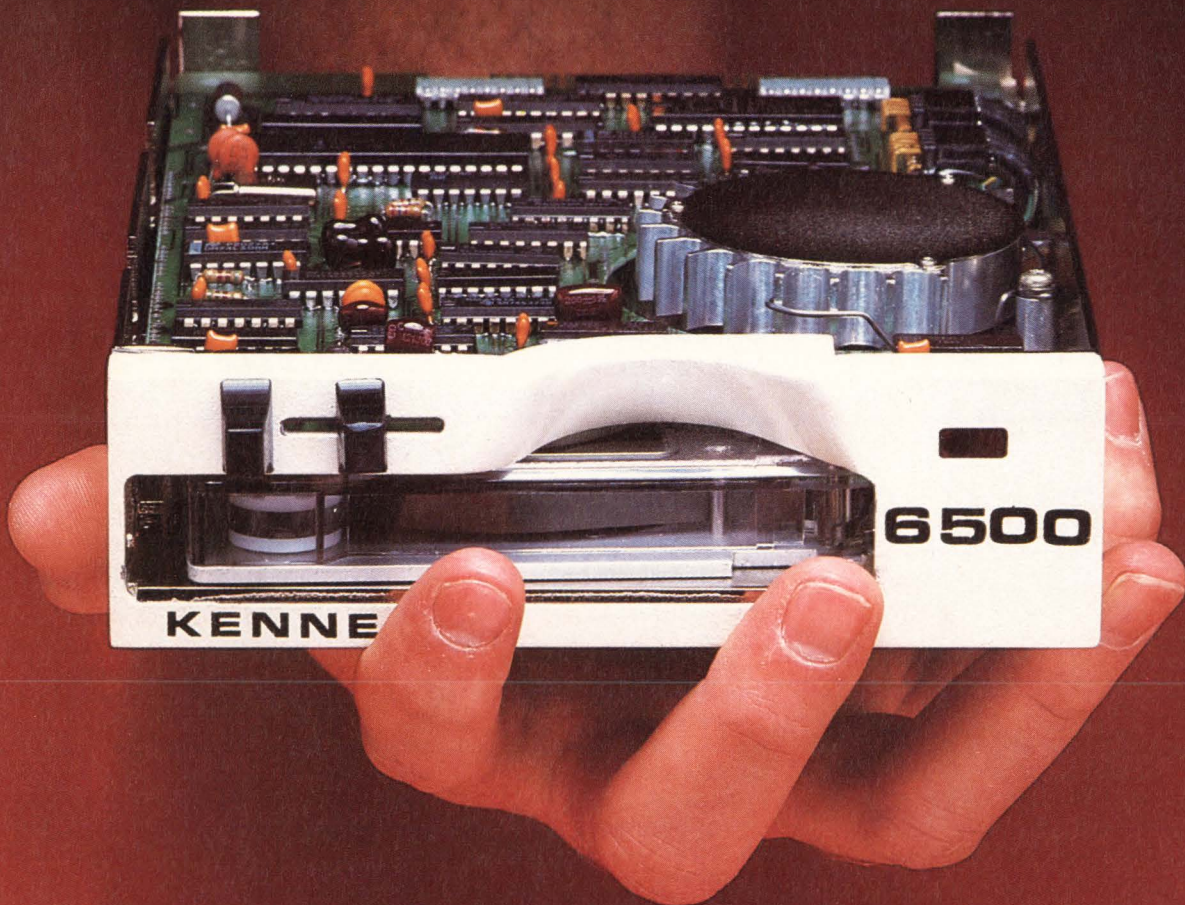




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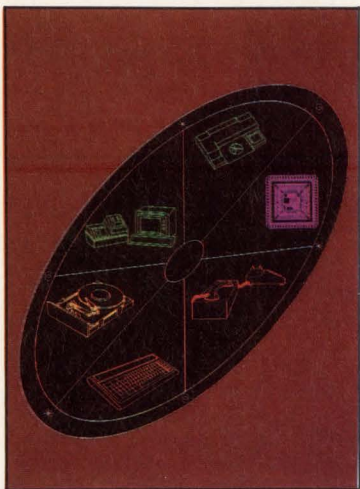
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CIRCLE 2

# COMPUTER DESIGN<sup>®</sup>



This month's cover was illustrated by Tom McCullough at Coddbarrett Associates, Inc using a DICOMED D-38 design station and a D-48 high resolution film recorder.

## TECHNOLOGY TRENDS '84/'85

**81** When the year's major developments are examined one by one, it isn't always easy to see how individual achievements in technology and products join to define a new direction. It's equally hard to see how they will affect the futures of engineers, the products they're designing, or their companies. In this issue, the editors of *Computer Design* look back at the technology and products of 1984, highlighting significant trends and assessing their impact in 1985—and beyond.

### COMPUTERS/MASS MEMORY

#### **83 Multiple CPUs and more memory define next generation**

*by Peg Killmon, Senior Editor*

**92** Superminis renew battle for top ranking... Fault-tolerant systems deal with increased loads... Personal computer benefits from 80286, networking, and software... Notebook-sized unit is an all-CMOS system... RAM/CPU combination produces potent single-board system... Full computer packed on a board... Array processor executes algorithms at 5 MFLOPS... Subset of VAX architecture serves low end of 32-bit market... Unix systems provide long-term solutions with upgradeability... Laser-based optical disk drive stores 1 billion bytes... Tape drives enhance high performance of GCR with cache technology... Winchester drive merges controller electronics on single board... Cache RAM accelerates Winchester disk transfers... Memory bubbles packaged to ride high on the Multibus... Tape subsystem exhibits full-size performance at low cost... Featherweight floppy disk drive stores 500 Kbytes.

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*by Nicolas Mokhoff, Senior Editor*

**126** Speech system designed for text-to-speech conversion... Interactive CAD digitizer enters the third dimension... Interactive three-dimensional graphics more than a pipe dream... Graphics system functionality swells with million addressable points... Workstation graphics architecture lightens programming load... Printwheel technology ups speed, adds intelligence... A single-user solution to CAE/CAD/CAM... Color and monochrome terminals race with megapixel speed... VDT offers low cost programmable features... Low cost plotter combines graphics command set and offline operation... Sophisticated graphics controller draws fast response time.

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#### **145 CMOS sets pace for chip development**

*by John Bond, Senior Editor*

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**DATA COMMUNICATIONS****169 Data comm networks finally come of age**

*by Tom Williams, West Coast Managing Editor  
and Richard Goering, Field Editor*

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**TEST & DEVELOPMENT****197 CAE, scope makers jockey for position**

*by Bill Furlow, Senior Editor*

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**SOFTWARE****217 Software industry strives for a standard solution**

*by Harvey J. Hindin, Special Features Editor*

- 227** Multitasking Unix look-alike supports 11 IBM XT users... Mainframe-style tools move down to personal computers... Multistage compilers go from mainframes to micros... Big Blue makes a major push to link computers... Lisp/APL merger supports functional programming concepts... Local area networks flourish while standards lag... Structured analysis eases project specification... Window worlds open to independent programmers... AI language programs expert systems under VAX/VMS... Graphics software makes dynamic data stream display possible.

**SYSTEM COMPONENTS '84/'85****243 Component advances keep step with system designs**

*by Malinda Banash, Senior Associate Editor  
and Jack Vaughan, Associate Editor*

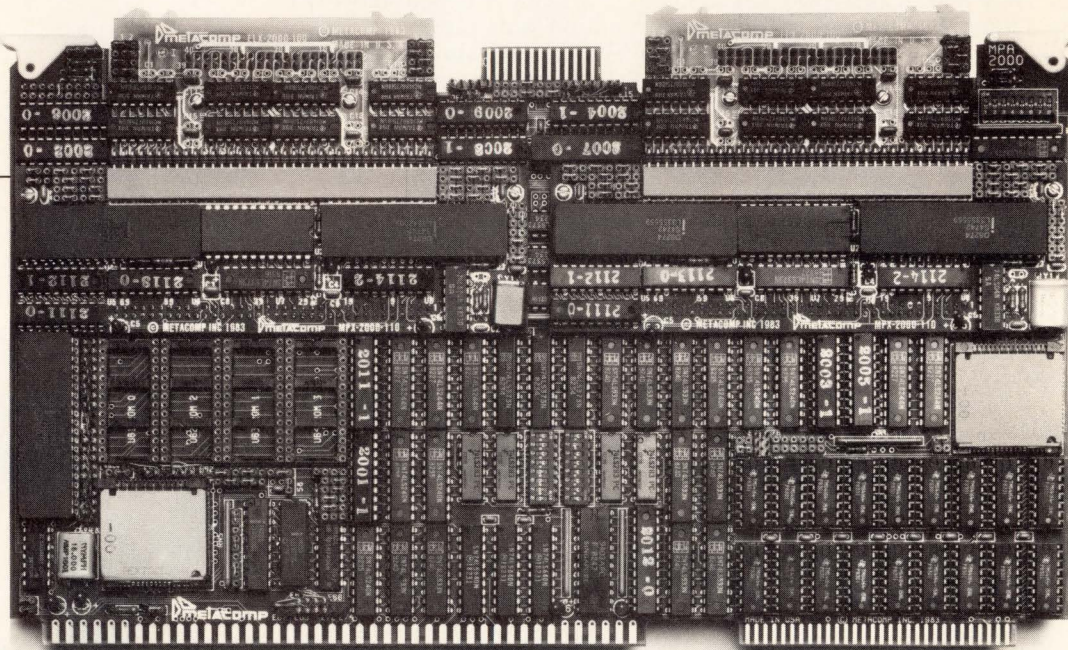
- 251** Flat panels approach monochrome CRT specifications... Technologies vie to displace CRT in terminals... Hybrid plasma display simplifies driver electronics, cuts cost... Power supply handles parallel operation... IBM packs in high density circuits.

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# Chairman of the boards



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## THE MULTIBUS BREAKTHROUGH PEOPLE



# UP FRONT

## Copyright law for ICs will help sustain industry growth

On Nov 10, President Reagan signed a bill protecting semiconductor chip manufacturers from pirates. Those who steal designs of copyrighted chips are now liable for fines as high as \$250,000. Proponents of the bill, including the Semiconductor Industry Association in San Jose, Calif, have long argued that the high cost of designing chips and the probability that the designs will be stolen dampen industry R&D. In a statement released upon his signing of the bill, the President cited industry contentions that a single chip may cost \$100 million to develop, but less than \$50,000 to copy. Therefore, pirates can effectively steal a developer's profits, as well as the chip design itself. He further noted that "not only does the semiconductor industry ship about \$14 billion worth of semiconductors, it also employs about 200,000 people." Manufacturers were generally delighted at the new protection. Said Ben Anixter, Advanced Micro Devices vice president of corporate marketing, "This law will encourage continued high levels of investment in new product development." The law, effective immediately, protects chips designed after July 1, 1983 for a period of 10 years. Other copyrightable works are protected for up to 75 years. In keeping with the unique category of law that protects them, protected chips will bear either the symbol \*M\* or an M within a circle, both of which stand for "Mask Work," rather than the traditional copyright symbol.—*W.S.*

## AC plasma display sports 1024-pixel resolution

Thomson-CSF (Paris, France) has produced a 1024- x 1024-pixel display using ac plasma as the medium. Available in the second quarter of 1985, the display uses fully integrated high voltage driver circuits to produce a small dot spacing. When viewed from 50 cm, the display's spatial resolution corresponds to the resolving power of the human eye. The display's active area is 307 x 307 mm, with a pixel pitch of 0.3 mm. TTL interfaces via a multiplexed bus. The device's electrodes are activated in groups of 32 using single ICs with CMOS-compatible inputs.—*N.M.*

## New entry promises to broaden graphics standards

The Virtual Device Interface standard in addition to vector graphics operations may soon expand to include raster graphics operations, with the help of a new product shown at Comdex by Digital Research (Pacific Grove, Calif). The Graphics Environment Manager, which brings a Macintosh-like user interface to MS-DOS computers, combines an IBM-compatible VDI with raster graphics capability. Digital Research sees the package as an end-user environment that can be transported easily to any MS-DOS compatible computer. Says Bill Higgs, product line manager for GEM, "The user interface is critical for opening up the market to users who are not computer users." Because of that, adds Tom Byers, product marketing manager, "GEM is a strategic product for Digital Research." The company is active in the American National Standards Institute X3H3 committee, which is preparing the VDI specification and recently spawned a subcommittee on raster graphics operations. Digital Research would like GEM to form the nucleus of a new standard.—*R.G.*

## UP FRONT

### Optical disk manufacturers hope to use ESDI

At November's Comdex in Las Vegas, magnetic disk and tape manufacturers responsible for mounting the campaign to install Enhanced Small Device Interface as an industry standard met with potential manufacturers of optical disk memory devices. Their aim was to extend the ESDI to support write-once, read-mostly optical memories in the 1-Gbyte range. Among the companies represented were Optical Storage International (Santa Clara, Calif), Optimem (Sunnyvale, Calif), and Alcatel Thomson Gigadisc (Redondo Beach, Calif). Also present were representatives of Scientific Micro Systems (Mountain View, Calif) and Maxtor, the San Jose originators of ESDI. According to a Maxtor spokesman, ESDI was developed beginning in Nov, 1982 as a standard interface for disk systems with a 5¼-in. form factor. At present, existing and proposed optical memory devices exceed the 5¼-in. form factor. But the real difficulty in tying in the optical devices appears to be their relatively slow access and transfer rates. While ESDI covers devices with transfer rates up to 10 Mbits/s, typical transfer rates for optical devices are below 5 Mbits/s.—*P.K.*

### Megaflop-per-second performance touted by coprocessor chip set

In January, Weitek Corp (Sunnyvale, Calif) will announce a two-chip coprocessor that breaks the 1000-ns barrier for coprocessor floating point multiplication. While conceding the inherent difficulties in devising benchmarks for floating point operations, Weitek's Craig Hansen, director of systems and software design, boasts that the WTL1164/WTL1165 chip set will provide performance "10 times faster than existing single-chip coprocessors." He bases his assertion on the chip set's latency—the total time from operand input to output results. Typical execution times for the chip set are a single-add in 360 ns, a double-add in 540 ns, a double-multiply in 660 ns, and a double-divide in 3780 ns. The set is composed of an ALU and a separate multiplier chip. For array processing, the multiplier chip's execution times will be below 180 ns for a single-precision multiply and less than 300 ns for a double-precision multiply. The ALU chip has flow-through times under 180 ns for both single- and double-precision functions. The set uses a full 32-bit data bus operating at 16.67 MHz to sustain performance exceeding 1 million floating point operations per second. Weitek will ship samples in March and promises production quantities by late April.—*S.F.S.*

### Storage Module Drive interface upgraded

As of November, efforts are under way to modify the industry standard SMD interface, long the standby of high end disk manufacturers. The aim is to support data transfer rates in the 2.4-Mbyte/s range to accommodate recently introduced 8- and 10½-in. Winchester drives that store upwards of 500 Mbytes. Discussing the proposed change in the ANSI standard at Comdex, industry representatives noted that all existing devices supporting the standard are already capable of the higher transfer rate. They seek to change the standard's specification to conform with industry practice.—*P.K.*

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# DATARAM

### Siemens and Philips sign second-source agreement

Two key telecommunication chips designed by Siemens (Munich, West Germany) are now available from the Elcoma Division of Philips (Eindhoven, the Netherlands). They are the 2050 peripheral board controller and the 2060 signal processing codec filter chips. The peripheral board controller contains a powerful HDLC controller that is programmable for pulse-code modulation at speeds of 1.5, 2.3, and 4 Mbits/s. This chip is implemented once for every 16 subscribers and functions as a local area network gateway support IC. Available immediately, the NMOS chip dissipates 0.4 W. The codec/filter chip casts digital filtering in CMOS, a first for such circuit complexity. Available in the first quarter of 1985, the codec chip consumes 150 mW of power. Both Philips and Siemens say they are gearing up to produce more telecomm ICs that need no modification to accommodate the standards of various telecomm authorities throughout the world. Texas Instruments announced a similar effort about two years ago. —*N.M.*


### Validation suite for Unix System V may emerge

Look for a validation package for Unix System V to come from Unisoft Systems, a Unix vendor in Berkeley, Calif. The company refuses to discuss specifics, but company vice president of sales and marketing Robert Ackerman, Jr couldn't suppress a knowing smile after being asked when such a package would be available. "A validation suite is very much needed," was all he would say about it. Ackerman had come to discuss the benefits of Signetics Corp's Memory Access Controller chip, which he claims enables Unisoft to incorporate some nifty features into their System V implementation on the Motorola 68000. He and Bob Rowe, who recently signed on as marketing manager for the MOS Microprocessor Division of Signetics, were extolling the intercorporate cooperation enabling their companies to announce the MAC chip and a version of Unix to support it almost simultaneously. Hardware and software must arrive at the same time, Rowe said, "from the designer's standpoint, that's the key."

But cooperation among corporations is far from universal. AT&T, for one, has been lax about giving the industry either a clear standard version of Unix or a means of verifying it. Hinting that Unisoft might be impatient with this nonstandard state of affairs, Ackerman noted, "Unisoft views the success of System V as necessary to the success of our business. And we don't plan to rely on outside vendors to guarantee it." Still, cooperation is a relative term. "I feel a lot more comfortable picking up AT&T's System V," said Ackerman, "than trying to pick up something IBM has done and make a business out of that." —*W.S.*

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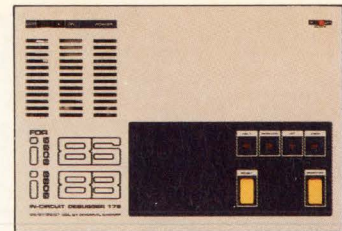
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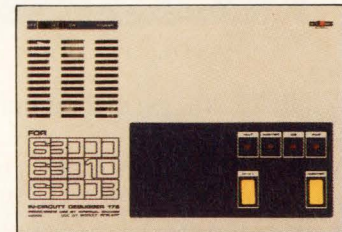
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**i8086/88**

i8086  
i8087  
i8088

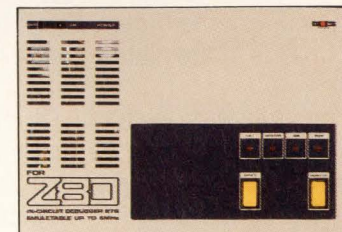
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**68000**

68000  
68010  
68008

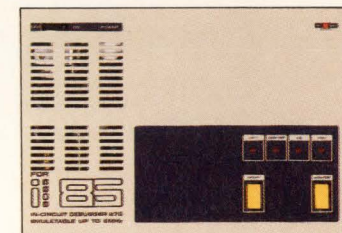
Emulates 68000, 68008 and 68010 in one unit to 10 MHz. Features; 128K of emulation memory - expandable to 256K, 4K deep x 48 bits wide realtime trace buffer, 30 different debugger commands.



**Z80**

Z80  
Z80B  
Z80H

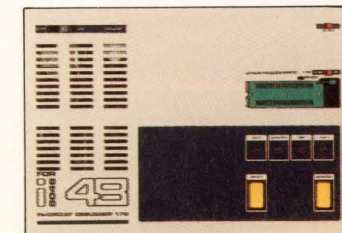
Emulates Z80B microprocessors to 6 MHz and Z80H to 8 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



**i8085**

i8085A  
i8085A-1  
i8085A-2

Emulates 8085 processors up to 6 MHz. Features; 64K byte user emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands.



**i8048**

i8048  
i8049  
i8050  
i8748  
i8749  
i8039  
i8035  
i8040

Emulates entire 8048 family in one unit to 11 MHz. Features; 4K emulation memory, 2K deep x 32 bits wide realtime trace buffer, 29 different debugger commands. 8748 and 8749 units feature a built-in EPROM programmer.

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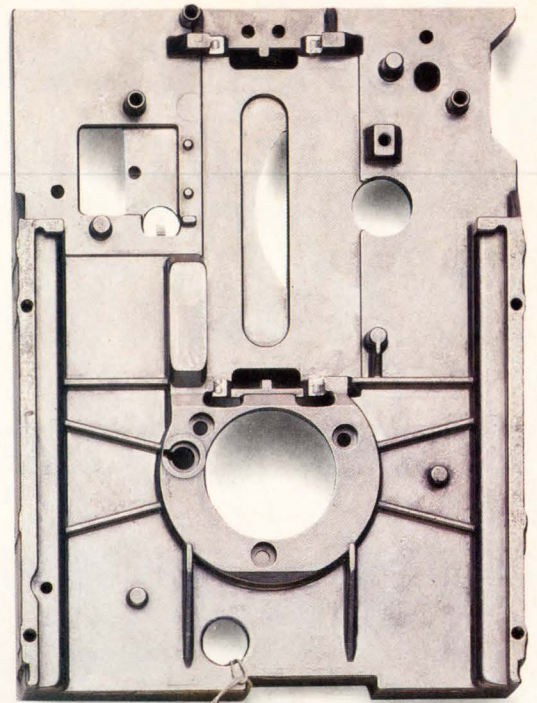
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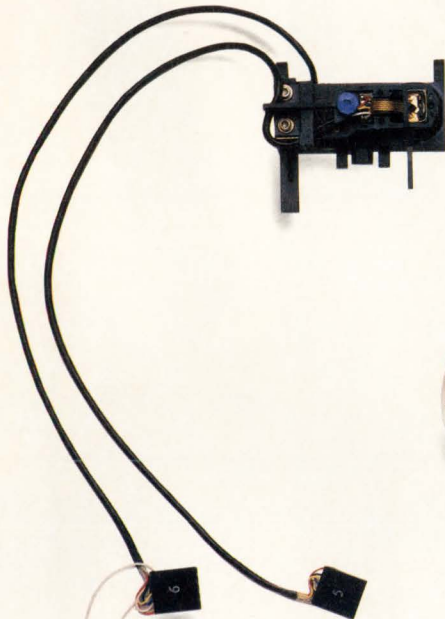
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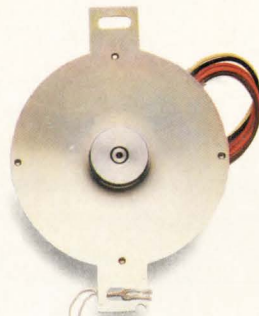
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# WHO IS WHO AND WHO IS NOT

This month I would like to talk about an event I did not attend. As a protest against one of the awards, I refused to attend the Who's Who in America Achievement Awards ceremony held in New York City in September. The specific award I was protesting was that to Lee Iacocca, Chairman of the Board, Chrysler Corporation, for Entrepreneurship.

Before listing my objections to the Iacocca award, however, I should first apologize to Claude E. Shannon—who received the award for technology, mathematics, and physical sciences at the same ceremony. It was certainly not my intention to rain on Professor Shannon's parade. For the record, I believe his information theory had such an enormous impact on computer science, communications, and such seemingly unrelated fields as biology and psychology, that he deserves much more recognition than he has so far achieved outside the scientific community.

Iacocca, I feel, falls far short of being a great entrepreneur because real entrepreneurs don't get federal loan guarantees. Instead, they persuade individual investors or investment bankers to advance capital based on the merits of the business plan and the track record of the management teams. Usually, they put a big chunk of their own cash on the line. Never do they ask unwilling taxpayers to finance their schemes. Within the computer industry alone, I can think of about 100 candidates more deserving than Lee Iacocca. One name that comes quickly to mind is Alan F. Shugart, a founder of Shugart Associates and Seagate Technology. Though Shugart went unrecognized in the Who's Who affair, he accepted Entrepreneur of the Year awards this year for Seagate from both the Harvard Business School Association of Northern California and the Peninsula Chapter of the Stanford University Business School Alumni Association.

Perhaps my assessment of Iacocca's business track record has been negatively influenced by firsthand experiences with products from companies he happened to be running. During Iacocca's tenure at Ford, I bought a Pinto; more recently, my wife bought a Dodge Colt. I would not hesitate to call both these cars "lemons" except that the word suggests an isolated bad car rather than a typical product in the line.

The Pinto itself was recalled twice—once to fix the gas tank which tended to explode if the car was bumped in the rear, and once to fix the steering mechanism, which tended to lock without warning. Also the Firestone 500 tires were recalled. Yet another problem was that Ford decided to cut costs by not drilling a set of holes intended to allow upper cylinder lubrication. The result of this cost cutting was early piston slap, which on my car, rapidly worsened after a water hose fell off and the engine

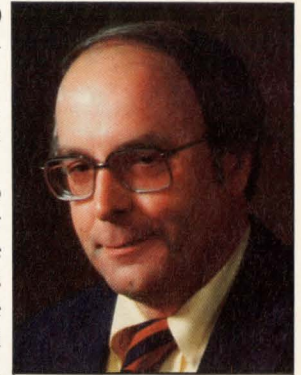
overheated. Even before 1000 miles, the bearings on the pollution control air pump collapsed. The crowning glory, however, occurred when the hatchback door fell off.

My wife's new Colt got off to a fast start in the race for "Lemon of the Year from the Entrepreneur of the Year." As she drove it home from the dealer, it bucked and sputtered like a high mileage used car.

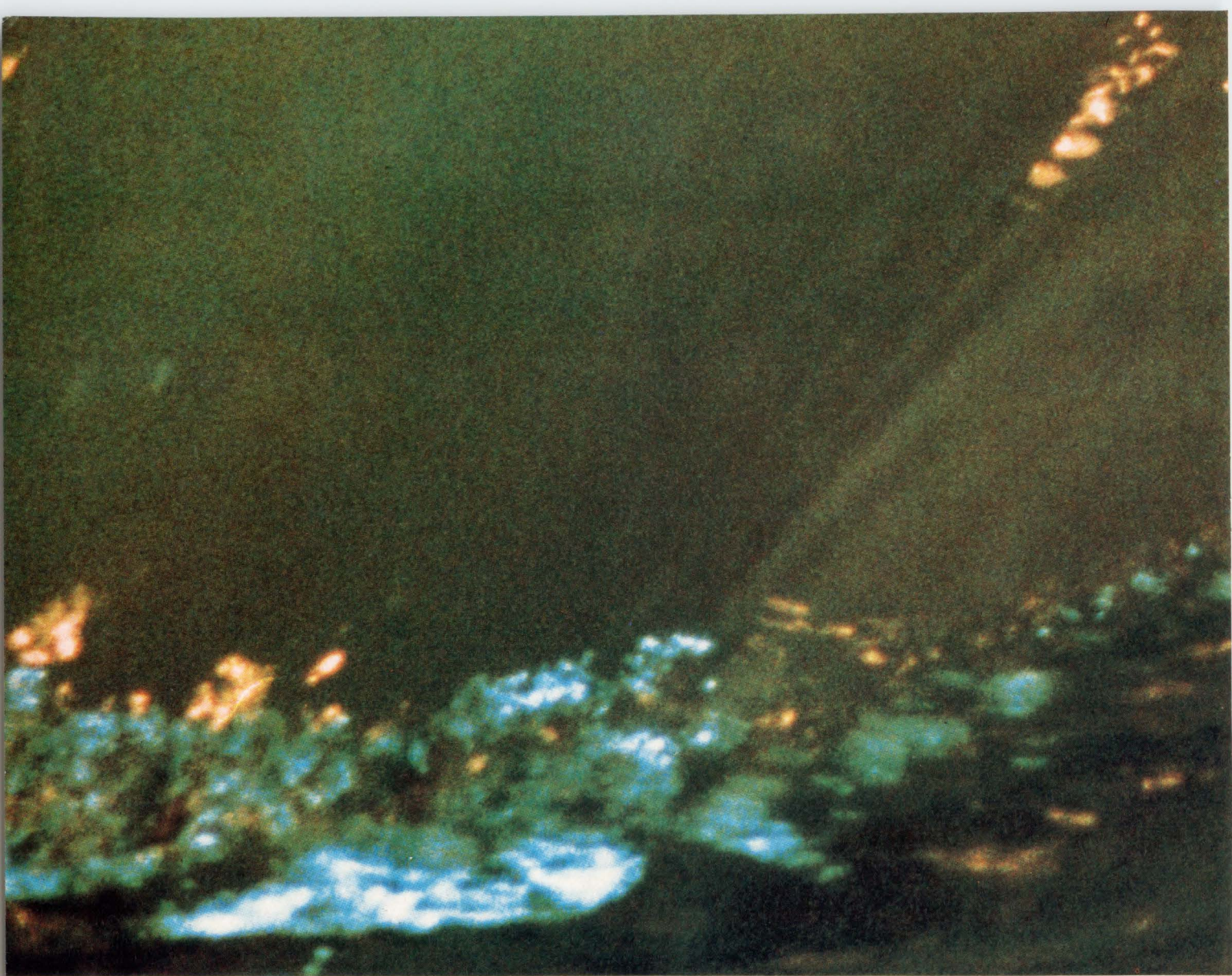
Fortunately, she had refused to sign the acceptance form because she noticed that a mirror and some light bulbs were missing. After about three trips back to the dealer, she got the missing parts replaced plus a new carburetor and a paint job. Now she complains that every time she uses the turn indicator or the light switch, the knobs fall off.

The automobile industry can learn a lot about good design and quality control from the computer industry. Unfortunately for Mr Iacocca, the car buying public is not so gullible as the people who give out Who's Who awards. An organization called CompuSearch (a division of Management Recruiters International, Inc, of Cleveland, Ohio) asked: Have American auto manufacturers improved the quality of their products a lot, a little, or not at all in the past two years? A large majority (66.2 percent) said that they have improved a little or not at all. Far fewer (28.2 percent) said they had improved a lot, while the rest (5.6 percent) were undecided.

Finally, I should substantiate my criticism of Marquis Who's Who, Inc, the organization that sponsored the award to Iacocca. Several years ago, I received a letter from that organization advising me that I was being considered for inclusion in Who's Who of American Women. A quick glance at the receding hairline in the photograph above should convince anyone that I certainly did not qualify. Apparently, a computer with a feminist bias had spotted my initials (MS) and wrongly concluded that I was of the female gender. Therefore, if I ever need to know "who's who" or "what's what," I shall not be consulting any Marquis publications.



Michael S. Elphick  
Editor in Chief



# INMOS has natural answers

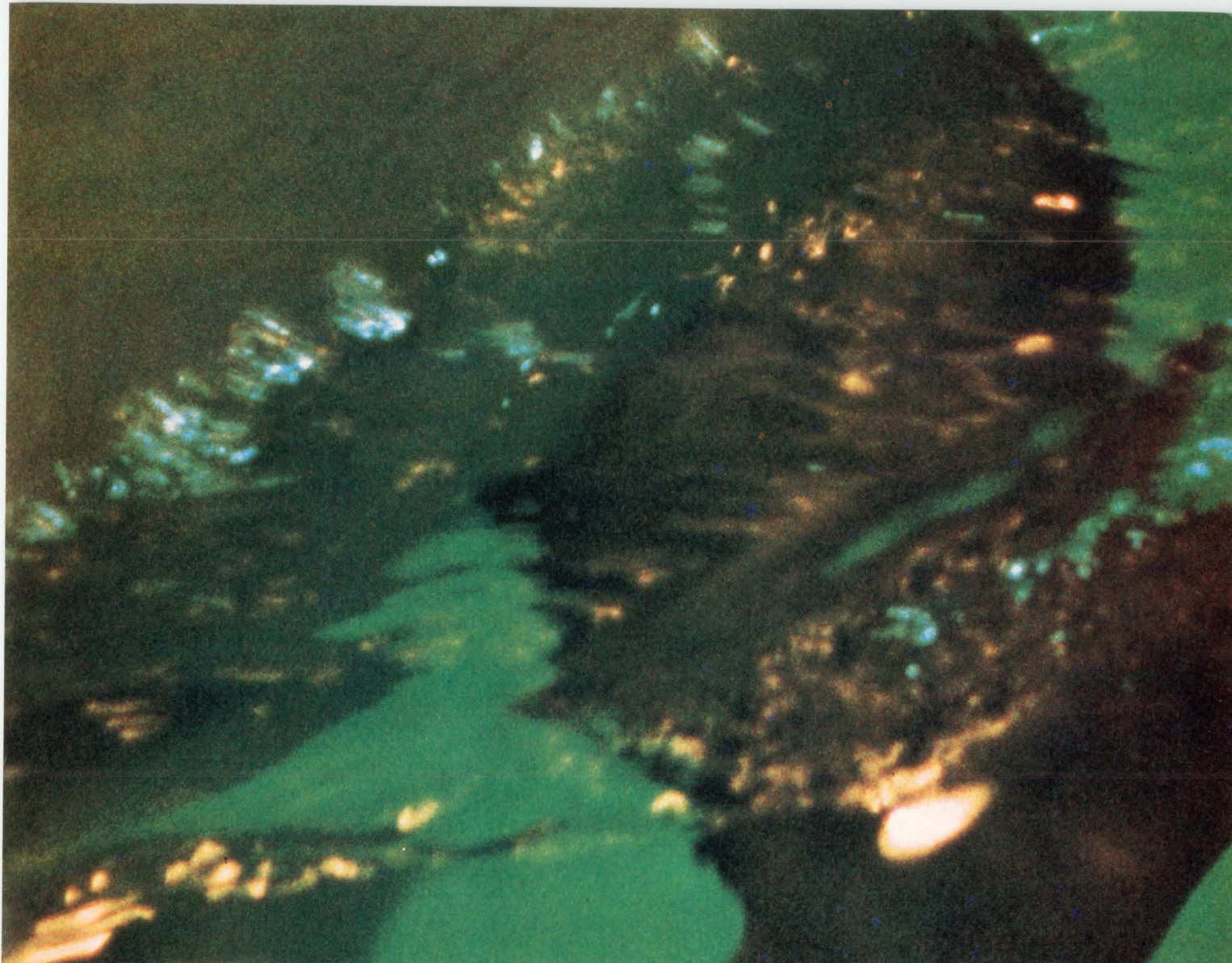
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CIRCLE 8

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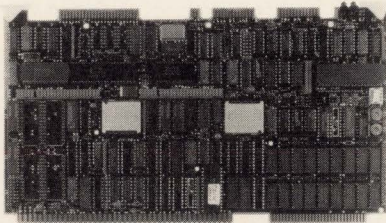
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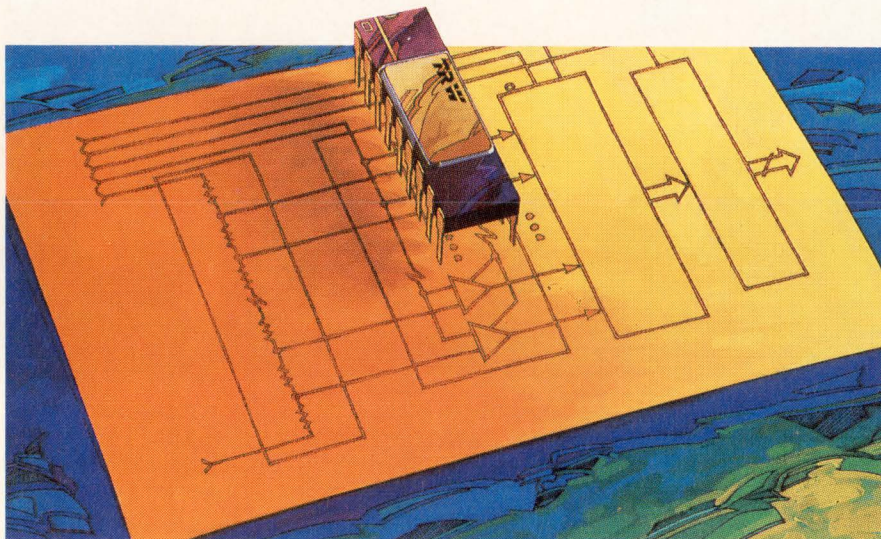
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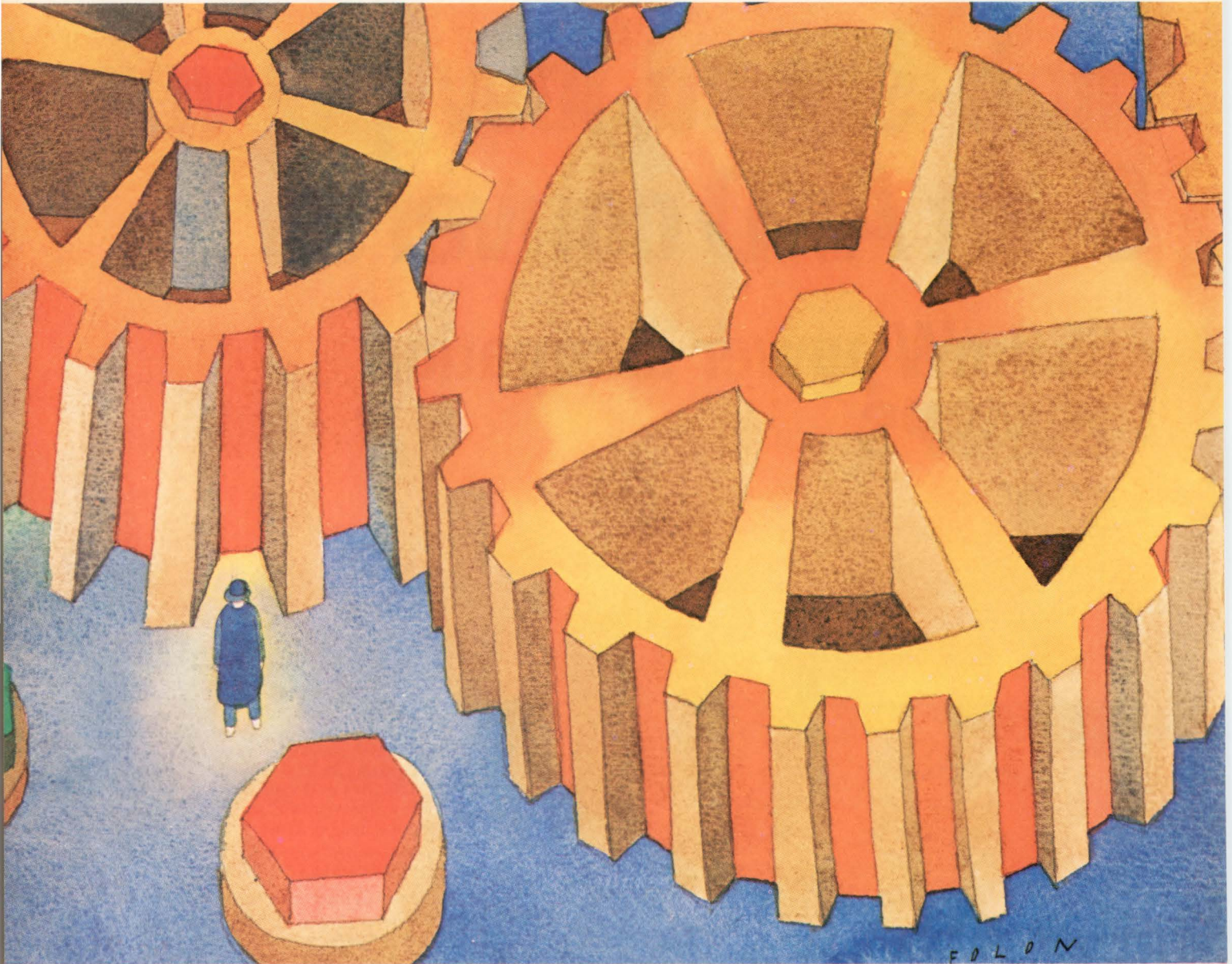
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## TURNING YOUR PC INTO A FASTER TOOL FOR MODERN TIMES.

This is the 3rd in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.

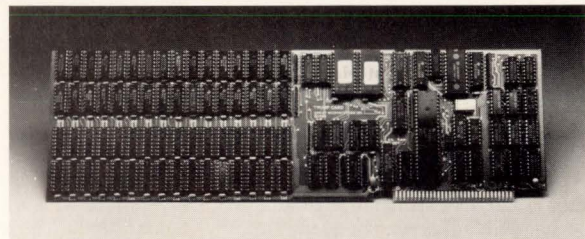


IBM® and other compatible PC computers are fast enough for general home and office use. But, for hardware and software development applications, the gears turn slowly.

What you need is a faster "gear" to co-process with the Intel 8088 inside IBM's PC. Like Zilog's Z8001® CPU. Now, there's a way to increase throughput for the IBM PC—as well as test the performance of the Z8001 CPU for your high-performance applications with a Z8001 CPU-based board called the "Trump Card" from Sweet Microsystems. And it proves dramatically how powerful Zilog's 16-bit CPU really is.

The new device is a peripheral board that plugs into any expansion slot on an IBM PC or compatible PC computer. Trump Card is addressed as an I/O device that communicates through the expansion bus. It is powered by Zilog's Z8001 CPU.

The Trump Card increases the computational power of the IBM PC, and provides maximum performance with a minimum of board space.



The Trump Card, shown from the front. The left side of the board contains 512 K-bytes of type-4164 dynamic RAM; the right side contains the Zilog Z8001 and an interface to the IBM PC I/O-expansion bus.

## Z8001 COMPILER BASIC IS 80 TIMES FASTER THAN IBM INTERPRETIVE BASIC.

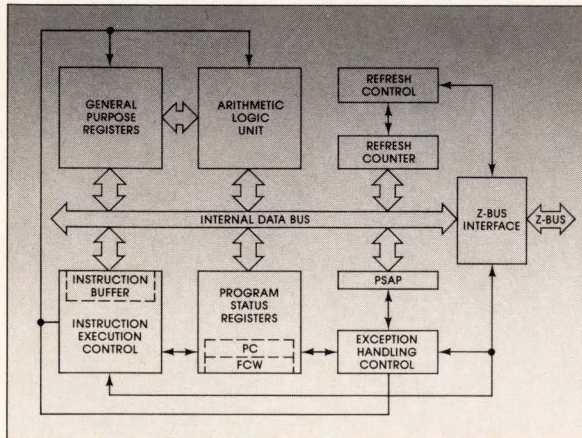
Essentially a monolithic minicomputer central processing unit, the Z8001 CPU is characterized by an instruction set more powerful than many minicomputers. As the programmer sees it, the Z8001 contains sixteen 16-bit general-purpose registers (for addresses or data) that may also be used in groups to form as many as eight 32-bit registers or four 64-bit registers. The low-order halves of the registers may be used for byte operations, thus the Z8001 CPU is able to manipulate data in 8-, 16-, 32-, and 64-bit pieces.

The Z8001 CPU, running at 10 MHz, can execute the same programs 4 to 10 times faster than the Intel 8088. What's more, the Z8001 CPU, with its large 8-megabyte memory range, makes the Trump Card's 512K bytes of memory easy to design with. (To use this memory in the card, you simply load a BASIC, CP/M-80, or C program from PC-DOS and type "RUN.")

Apple II	Apple III	TRS-80 Model II	IBM PC	IBM PC (with Trump Card)
224	222	189	190	2.4

A comparison of execution times (in seconds). Running on IBM's interpretive BASIC, a Sieve program takes 190 seconds to execute. Running the same program under TBASIC on the Trump Card Compiler takes only 2.4 seconds.

The eight addressing modes are register, indirect-register, direct-address, indexed, immediate, base-address, base-indexed, and relative-address. The instruction set utilizes data types ranging from single bits to a 32-bit long word. What's more, the processor executes 110 distinct instruction types that, when permuted by all the addressing modes and data types, create a set of more than 400 instructions.



A Z8000 CPU functional block diagram of the internal structure of the Zilog Z8000 family of high-performance microprocessors.

## ALL THE PROPER SUPPORT FOR 512K BYTES OF MEMORY.

The wide range of software written for the Z8001 CPU is proven by all the programs you can run on the Trump Card. With the Z8001-based Trump Card, you can run the following software on your IBM or other compatible PC:

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**C-Compiler**—The industry standard version of C is available.

**Debugger**—Intended to aid in program development, you can examine and change memory and register contents and more.

**Screen-editor**—Has many word processing features, including ASCII text file development.

**Multilevel Language Compiler**—Allows Pascal-like control and data types, arithmetic expressions with automatic or specified allocations of registers, and more.

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## COPROCESSING IS JUST PART OF THE STORY.

The Z8001-based Trump Card is just one example of a successful application design for the Z8001 CPU. But there's far more to the Z8000 family than this.

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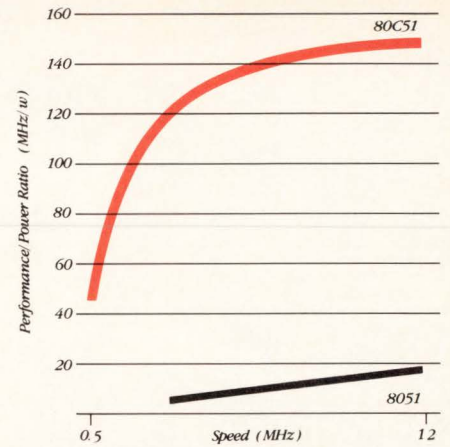
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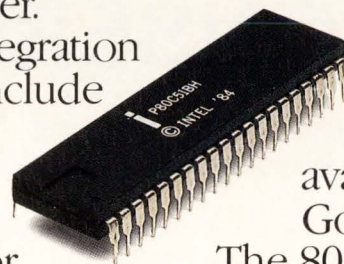
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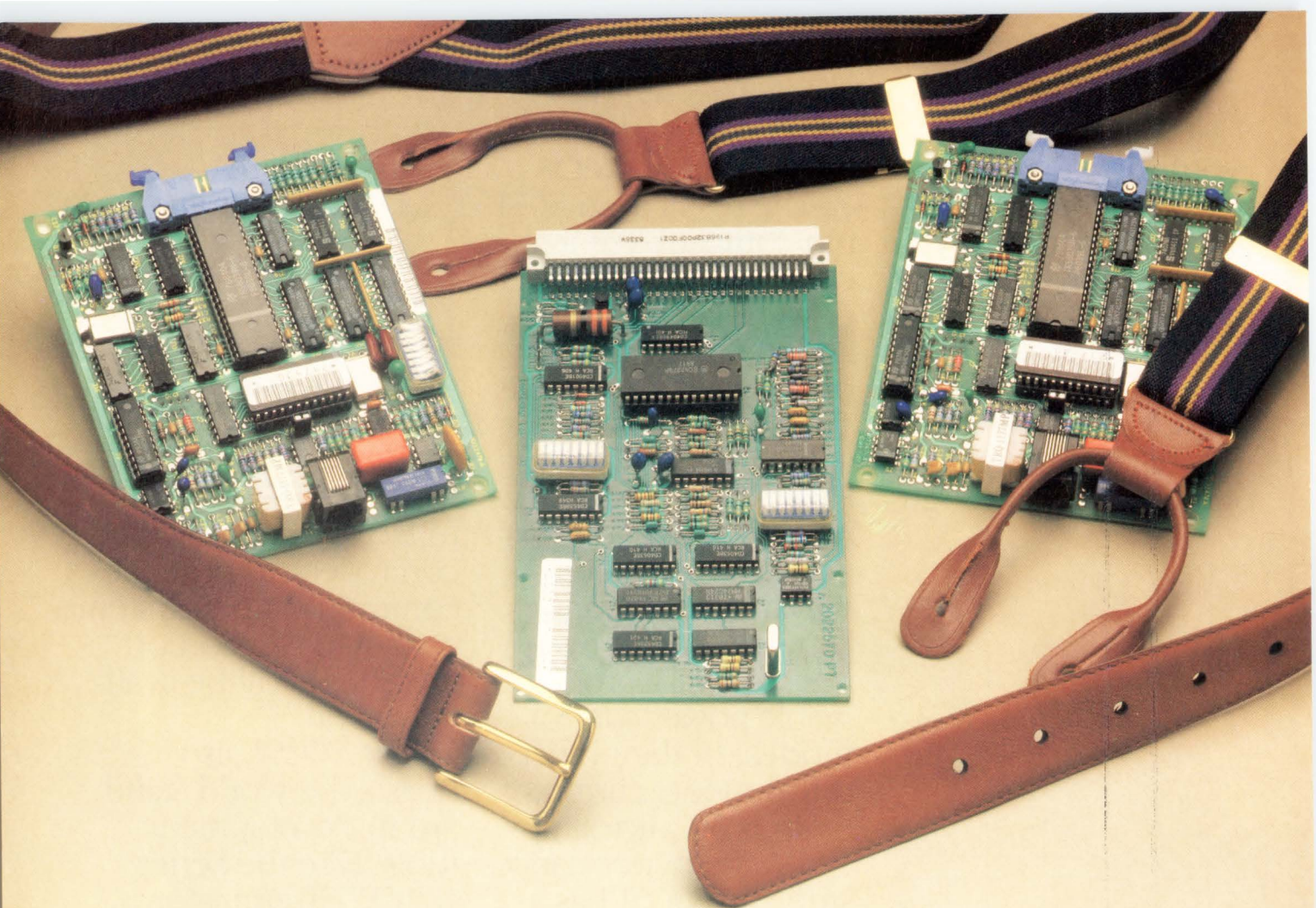
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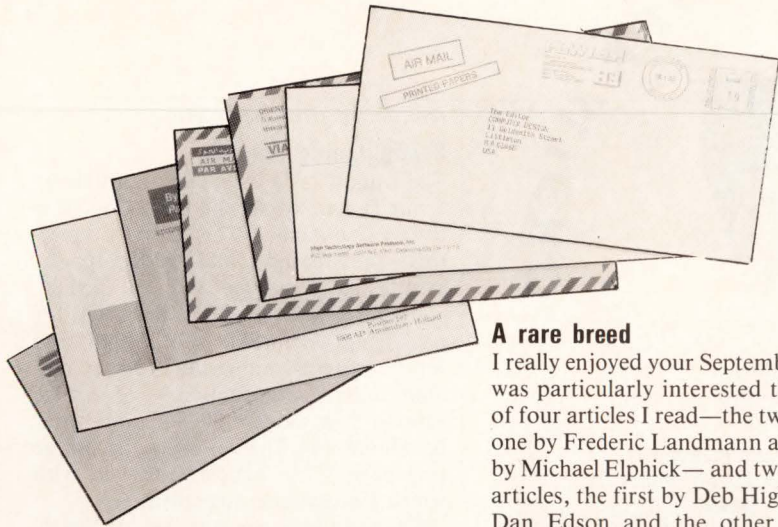


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## LETTERS TO THE EDITOR



### Short on jobs, not engineers

The September 1984 issue contained two items that require a strong rebuttal. When there is a genuine shortage of oil, or tungsten, or corn, the constant-dollar cost of these commodities rises. When there is a genuine shortage of physicians, the constant-dollar cost of their services rises. Yet, the salaries of engineers, measured in constant dollars, have remained the same (or decreased slightly) since 1969! How can this indicate a shortage of engineers?

Contrary to the view expressed by Frederic Landmann in his "Publisher's Perspective" on p 13, there is no "dearth of computer design engineers in the United States." There may, however, be a dearth of experienced American computer design engineers willing to work for \$30,000 a year. While Landmann worries that the United States produces fewer engineers per capita than either Japan or the Soviet Union, he ignores the fact that, per capita, we produce 2.7 times the number of engineers as West Germany.

Corporate presidents such as Ray Stata have a clearly defined fiduciary responsibility to reduce all costs, including engineering salaries. Stata's views (p 92) are old stuff to those of us who are familiar with his "big lie" technique. The fact is that, at the same time Stata was calling for a massive increase in the number of engineers, he had imposed a hiring and salary freeze within Analog Devices.

Stata claims, "We simply cannot afford the risk of having too few engineers." Those of us who remember the cyclical massive layoffs of engineers counter with, "We simply cannot afford the risk of having too few jobs."

Irwin Feerst  
Committee of Concerned EEs  
PO Box 19  
Massapequa Park, NY 11762

### A rare breed

I really enjoyed your September issue and was particularly interested that the first of four articles I read—the two editorials, one by Frederic Landmann and the other by Michael Elphick—and two of the lead articles, the first by Deb Highberger and Dan Edson and the other by Harvey Hindin—all seemed to be addressing the same issue, although from admittedly different viewpoints. All were asking the same question: "Where do we get the people to do all this?"

We will require at least two types of people to accomplish all that is outlined by the authors—design engineers and "frontier pushers." Pushers are people who must provide the information and facts to be crunched by the computers of the 1990s. The design engineers have the task of providing the computers.

Of the two, I guess the frontier pushers will be the easiest to provide. Already our graduate schools and research laboratories are training this type of person. The design engineer may be another story. Our colleges just may not be properly equipped to train design engineers, especially computer designers.

Most of what the computer design engineer needs to know is hidden in either the electrical engineering or computer science programs. Few colleges have gone to a computer engineering program, but often it's part of the electrical engineering program in the same way that computer science is often tied to the math departments. A student is exposed to a wide range of topics, among which are com-

puters and digital design—maybe. Unless students go on to graduate school, most enter industry with a broad (but shallow) background, learning what is required for their job, on the job. I have no problem with that—provided that industry picks up the ball at this point and sees to it that the necessary training is provided.

The electrical engineer and the computer scientist leave the university with a large gap separating them and when they arrive in industry, the gap is widened. We hear of software people and hardware people instead of computer people. To be an effective computer designer, the person has to have a strong background in both software and hardware. Computer design will no longer be software design and hardware design as separate elements but hardware and software design as a single coherent entity.

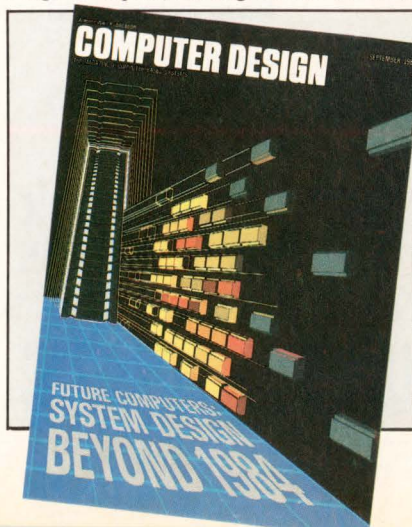
The time has come when computer engineering must stand on its own. To be sure, it must draw upon the existing facilities of both computer science and electrical engineering. These computer engineering graduates may not know energy conversion or theory of languages, but they will be able to appreciate the role each plays in the design of a new computer system.

These computer engineering departments will need the right kind of faculty because most of the existing faculty members are not designers. The emphasis on "basic research" within the academic community has discouraged design in favor of research. What design does go on is often one-of-a-kind design and ignores many of the practical aspects of design so necessary in an industry-based design. We need to get designers into the classrooms and project labs of the universities, not necessarily as teachers, but as referees, as guides, as consultants, whatever.

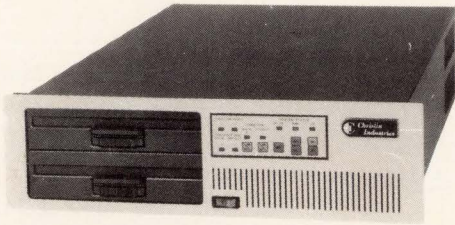
"Who are the students and how do we get them into the classes?" Unfortunately most of the answer is money. Here is my suggestion: whenever industry hires a graduate from a university, let it contribute the tuition, room, and board as a full year scholarship for some future student. In this way we would ensure that universities have the funds to attract good students. These students will ultimately fill industry's needs.

David B. Young  
Harris Corp  
PO Box 883  
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(continued on page 24)



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**LETTERS TO THE EDITOR**

(continued from page 23)

**Straightening the rule**

The August 1984 issue had an article by Frank Drzymkowski and Dave Goodman of ITT Cannon on p 77 entitled "Connectors—the Missing Link in EMI Suppression." This was an excellent article, containing much useful information for packaging engineers who design and retrofit systems to meet the Federal Communications Commission rules of part 15, subpart J (as docket 20780 should now be referenced). There is one point on the first page of the article, however, with which I must take exception.

The authors state that "As of Oct 1, 1983, any equipment under the jurisdiction of this docket that does not meet the requirements cannot be offered for sale. If already sold, the equipment must cease operation until brought into compliance." This statement is not correct. The FCC ruling did not require existing equipment in the field to shut down and be brought into compliance with the new rules. To do so would have been next to impossible, unfair to existing users, and totally uneconomical. Imagine trying to track down all the existing Radio Shack TRS-80 Model 1 computers to bring them into compliance.

In addition, the FCC set Oct 1, 1983 as the date after which all devices/systems manufactured—not sold—must comply with the limits on radiated and conducted emissions. New designs first produced after Oct 1, 1983 had to meet the requirements before they could be offered for sale. The FCC did not require retrofitting equipment/systems already in the field, except in cases where that equipment/system was shown to be causing harmful interference to a communication service.

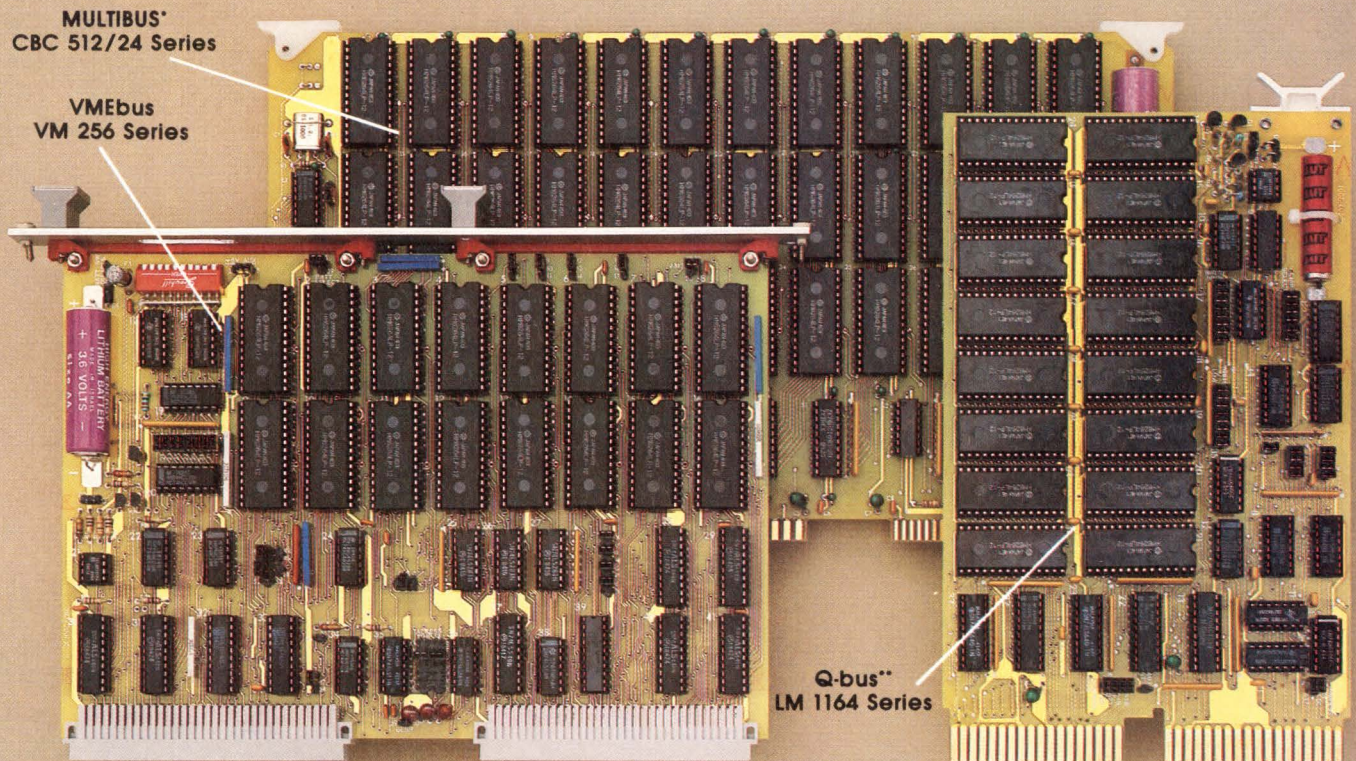
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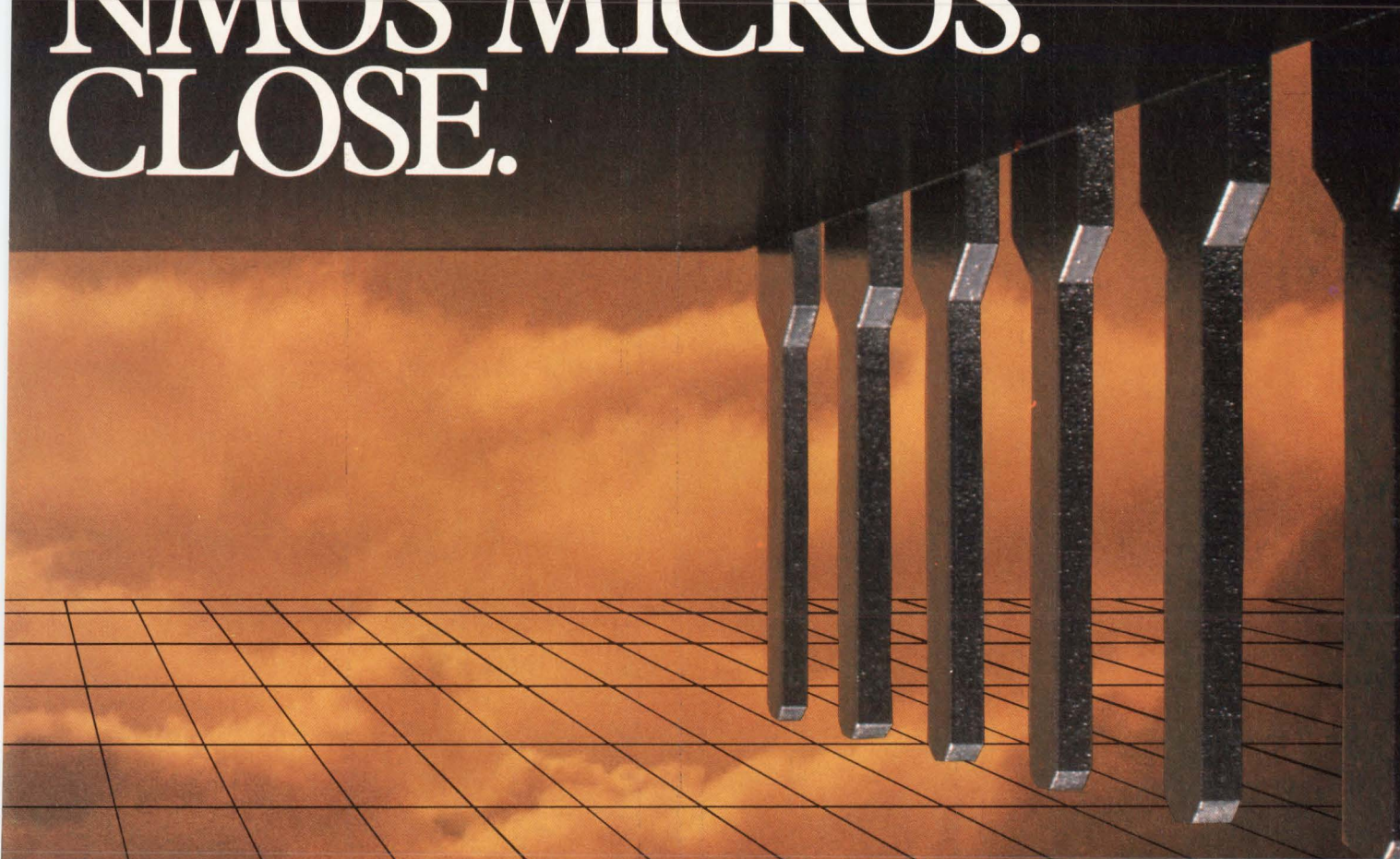
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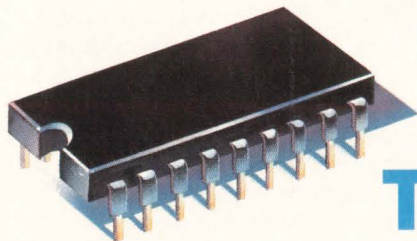
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TMP80C49	CMOS	2K	128	6MHz	10mA	10µA
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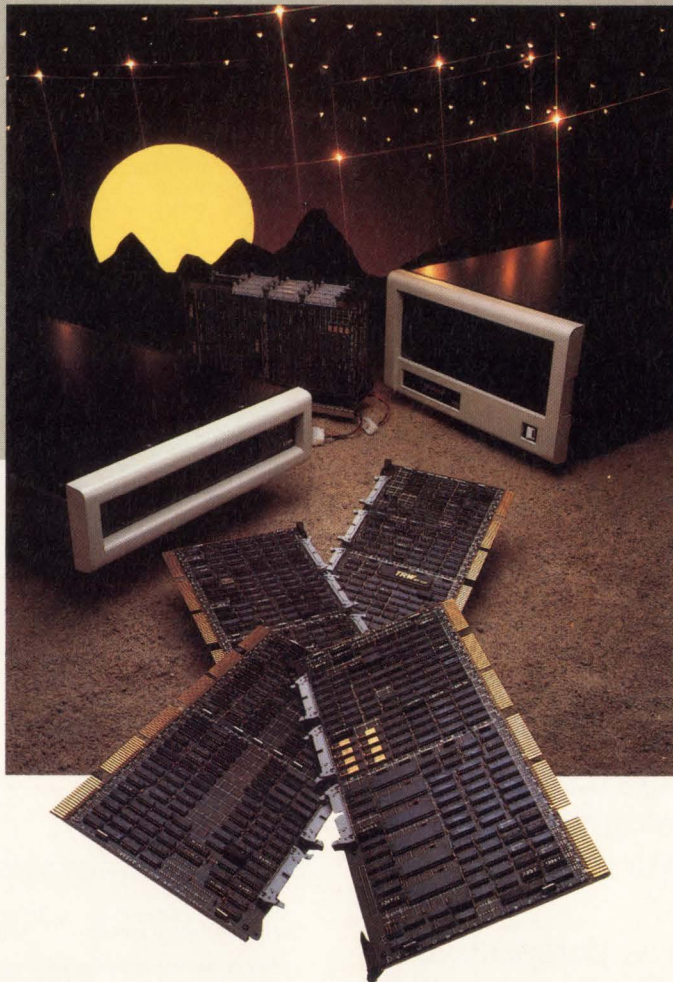
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## Do-it-yourself development tools speed AI applications

Expert system development kits are among the hottest products in the rapidly emerging artificial intelligence marketplace. Now offered by at least a dozen companies, with more new offerings on the way, these software packages are essentially "shells" that allow non-AI programmers to build expert systems. Normally, a development kit provides an inference engine and a variety of programming and graphics tools for building a knowledge base. It provides a simplified user interface for users without AI expertise, saving what may be years of development time.

To build a knowledge base, the user typically specifies a sequence of If-Then rules, gives examples of decisions, or provides lists of items and their characteristics. Graphic aids such as windows and mice (initially developed by AI researchers) are provided by most vendors. Many kits will diagram a chain of reasoning or explain why the system has reached a given conclusion. In addition to the software, most vendors provide training and extensive support for the development kits.

Although many of the development kits look similar at first glance, there are important distinctions between these products. Users need to ask what hardware the package runs on; whether the kit allows (or generally requires) programming in Lisp, or some other conventional language; what applications the kit is designed to solve; and how complete an expert system it can build.

The internal workings of the kit also make a difference. For example, a kit that uses rule-based reasoning requires a different type of input—and offers different advantages—from a kit that uses frame-based representation. Rule-based reasoning represents knowledge in the form of If-Then rules, while frame-based representation classifies objects and their attributes in a semantic network. Some kits combine rule-based reason-

ing and frame-based representation. But, as with any other product, trade-offs always exist.

Now you can buy a kit and build an expert system on an IBM PC or Texas Instruments' Professional Computer, but it will be a very small system or a prototype for a full-scale application. Frame-based representation can be very efficient, but users often find it easier to work with rules. A kit originally designed for business or financial applications may not be of much use for building an industrial process control system.

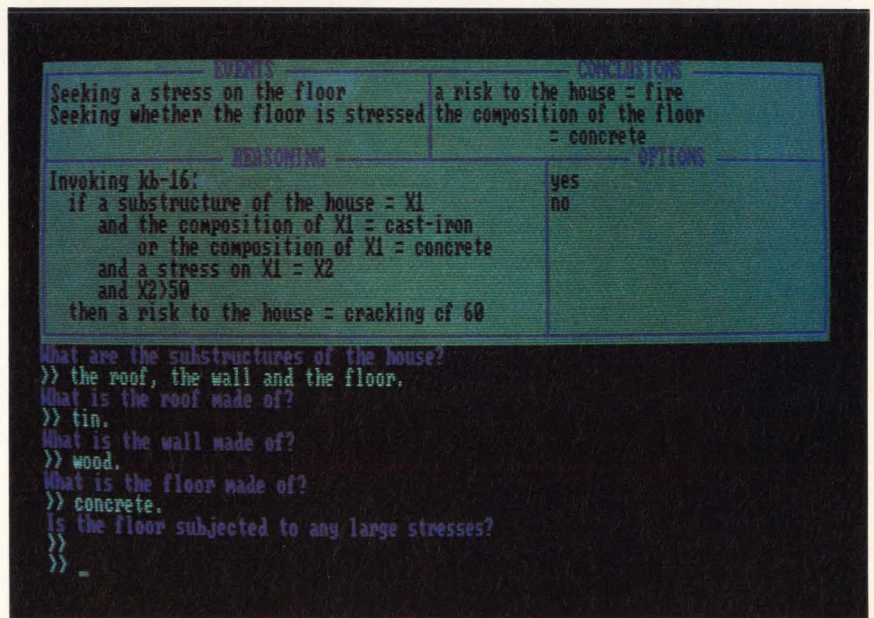
### How useful are they?

Users must determine whether or not a complete application can be built from a kit. According to Bradley Berg, manager of software systems for Smart Systems, "Most people selling expert system tools are only solving 10 percent of an application. In a typical expert system application, about 10 percent is really AI and 90

percent is just general-purpose computer programming." Thus, Berg says, "Shells are nice for building prototypes, but they're not vehicles for building complete applications."

In early 1985, Smart Systems will market Arby, an expert system shell specifically for electrical equipment diagnosis. "We're solving 10 percent of the problem," Berg acknowledges. Other vendors claim a complete application can be built from their kits. Several, however, say that a competitor's product requires extensive programming in Lisp to build a complete application. Whatever merits these claims and counterclaims hold, most suppliers are careful to include some connection to a programming language.

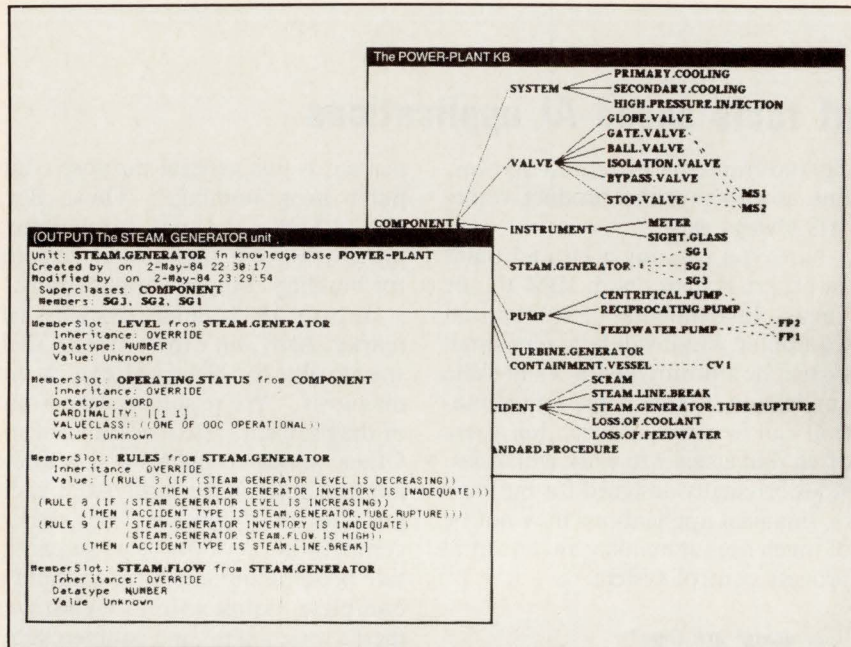
Some development kits were originally designed around a specific application. "If your problem fits the problem they were designed to solve, you're home free," says Peter Wong, *(continued on page 30)*



Teknowledge's M.1 system runs on an IBM PC. In this expert system, the upper half of the screen is devoted to windows that display the system's reasoning, while the lower half shows the consultation as a user of the completed knowledge system would see it. The knowledge base concerns potential risks of physical damage and deterioration in a building.

## Do-it-yourself tools

(continued from page 29)



Several expert system kits, including KEE from Intellicorp, allow frame-based and rule-based representation. Here, a unit called STEAM.GENERATOR is given slots called LEVEL, OPERATING.STATUS, RULES, and STEAM.FLOW. The Rules slot consists of If-Then rules. The window at the right shows the semantic network created by frame-based representation.

director of applications development at Infotym. "If not, it won't be as useful. You've got to look at it and see how it's constructed, and make sure it will solve your problem."

According to the Wong, a predeveloped inference engine can be constraining because the application itself determines how a problem should be solved. "An inference engine is really a strategy for searching through rules," Wong says. "How you do the searching is problem-dependent." Despite this attitude, Infotym encountered resistance this fall when it introduced a development tool called Reveal without an inference engine. A new release will include an inference engine, but will also allow users to write their own.

One feature making the kits attractive is the extensive training and support provided by vendors. For example, of the \$60,000 price tag for Intellicorp's Knowledge Engineering Environment (KEE) development kit, half is earmarked for training and support. This includes three days of onsite training, during which users build a prototype; 10 days of onsite

consulting; and ongoing support provided by Intellicorp's staff of knowledge engineers.

In some cases, results from development kits can be impressive. Ford Aerospace struggled for a year and a half to develop its own expert system for satellite diagnosis. It then bought KEE software, and had a usable prototype running in less than one month. Other vendors of expert system kits tell similar success stories.

### The hybrid approach

Kits that solve the broadest range of problems seem to combine a mix of reasoning and decision-making strategies. KEE, a general-purpose tool, uses both frame-based representation and rule-based reasoning to build its knowledge base. The inference engine uses both forward and backward chaining. (Backward chaining concludes a possible hypothesis and then works backward to verify the facts that will substantiate it; forward chaining starts with the facts and draws a conclusion.)

A new version of KEE, revision 2.0, supports logic-based program-

ming, strengthens semantic checking, and permits the development of graphic end-user interfaces. KEE runs on Xerox series 1100 machines, the Symbolics 3600, LISP Machines Inc's own Lisp units, and the Texas Instruments' Explorer.

Like many expert system kits, KEE uses object-oriented programming, an approach pioneered in Xerox's Smalltalk. An object is an entity representing a collection of information. Objects are organized into hierarchical "classes," and each object is associated with characteristics called "attributes." A new object can inherit attributes from another object—which means the system can infer characteristics without user input.

Object-oriented programming allows frame-based representation. In KEE, objects called "units" have attributes called "slots." For example, a STEAM.GENERATOR unit within the Component class might have slots called LEVEL, OPERATING.STATUS, and RULES. Production rules, therefore, can be used as part of a frame-based structure.

Frame-based representation saves redundant entries because attributes from one object can be inherited by another. It can also reduce substantially the number of rules a system needs to store. In a pure rule-based system, all relationships between objects have to be specified by rules. However, many people find it harder to work with frames than rules. Rules are simple and direct, and they best codify the procedural knowledge of a domain.

Xerox's Palo Alto Research Center offers an object-oriented language called Loops that has many of the same features as KEE. It costs a fraction of what KEE costs—but comes without support. Since Loops runs on the Xerox 1100 workstation, users who buy that machine can start out with Loops, and then move up to a package such as KEE when support is needed to develop an application.

Other kits that combine rule-based and frame-based strategies include SRL+ from the Carnegie Group and the Knowledge Engineering System (KES) from Software Architecture

### Expert System Development Packages

Company	Product	Machine	Cost	Comments
Carnegie Group (Pittsburgh, Pa)	SRL +	C.G. workstations, VAX/VMS/Unix, Symbolics 3600	\$70,000	General-purpose expert system development tool.
	Plume	Same as SRL + except Unix	\$35,000	Natural language interface tool.
IBM (Armonk, NY)	Lisp/VM	IBM System 370	\$6000	Programming language with support.
Inference Corp (Los Angeles, Calif)	ART	Symbolics 3600, VAX/VMS-Lisp, LMI Lisp Machines	\$60,000 to \$100,000	General-purpose expert system development tool.
Infotym (Cupertino, Calif)	Reveal	IBM VM/CMS, VAX/VMS, IBM	\$35,000 to \$50,000	Pascal-type language with support tools.
Intellicorp (Menlo Park, Calif)	KEE	Xerox 1100, LMI Lisp machines, TI Explorer, Symbolics 3600	\$60,000	General-purpose expert system development tool.
Jeffrey Perrone and Assoc (San Francisco, Calif)	Expert-Ease	IBM PC with 128-Kbyte RAM	\$2000	For small expert systems. Induces rules.
LISP Machines, Inc (Los Angeles, Calif)	Picon	LMI Lambda/Plus	—	Shell for realtime process control. Available June 1985.
Radian Corp (Austin, Tex)	Rulemaster	Any Unix 4.2 IBM PC/XT	\$50,000	Induces rules from decisions.
Smart Systems (McLean, Va)	Duck	Any machine running Lisp	\$6000	Logic-based programming language.
	Arby	Any machine running Lisp	\$9000	Shell for electrical equipment diagnosis. Available early 1985.
Software Architecture and Engineering (Arlington, Va)	KES	VAX/Unix/VMS, Apollo, Symbolics, IBM PC, others	\$23,500 or \$4000 per node	General-purpose expert system development tool.
Teknowledge (Palo Alto, Calif)	M.1	IBM PC with 128-Kbyte RAM	\$12,500	Small expert systems or prototypes.
	S.1	Xerox 1100, VAX/VMS	\$50,000 to \$80,000	General-purpose expert system development tool.
Texas Instruments (Austin, Tex)	Personal Consultant	TI PC with 512-Kbyte RAM	\$3000	Small expert systems, or prototypes.
Xerox PARC (Palo Alto, Calif)	Loops	Xerox 1100	\$300	Object-oriented programming language. No support provided.

*(continued on page 32)*

## Do-it-yourself tools

(continued from page 31)

and Engineering. SRL + runs on the Carnegie Group's own line of workstations, as well as VAX/VMS, VAX/Unix, and the Symbolics 3600. KES runs on VAX/VMS or VAX/Unix, and a number of smaller machines, including Apollo workstations and the IBM PC.

## Exploring hypothetical worlds

The most sophisticated and most expensive development tool available today is the Automated Reasoning Tool (ART) from Inference Corp. Just as KEE and SRL +, ART combines rule-based, frame-based, and object-oriented approaches. Unlike other tools, ART has a built-in mechanism to process and represent a large number of possible alternatives simultaneously. "This is the first language that has the semantics for parallelism," says Inference marketing specialist Abraham Gutman.

ART uses a blackboard mechanism to process "viewpoints." These are views that rules have of the knowledge. Viewpoints allow ART to chart alternative courses of action called "hypothetical worlds." This means ART can consider potentially conflicting alternatives, or explore many aspects of one problem. "We look at What-If rules as well as If-Then rules," says Gutman.

Viewpoints also permit a technique called "time modeling," which allows ART to evaluate a situation that changes over time. ART can assign "confidence values" that give a qualitative estimate of a viewpoint's accuracy. Ultimately, ART selects one viewpoint and promotes it as the desired solution. By processing viewpoints simultaneously, ART runs much faster than systems that have to process sequentially all options.

Part of ART's efficiency is based on its ability to find "patterns" in data, and draw inferences. For example, a pattern might show that "the expected logical value at point X is V, the measured logical value at point X is W, and V is not the same as W." ART can infer that the logical value at point X is incorrect. ART can also combine forward and backward chaining in a single application.

## Workstations provide for new applications

Cognitive scientists in the computer research lab at Tektronix explored the use of expert systems during their evaluation of the company's new artificial intelligence terminal. As a feasibility study of using the new 4404 as an expert system, cognitive scientists James Alexander and Michael Freiling chose to implement the AI terminal in repair depot applications supporting service technicians. They chose one particular piece of equipment (Tektronix FG-502 function generator) to represent the task at hand. About 12 work weeks were spent interviewing troubleshooters at the company's repair depots around the U.S. determining their needs, their methods of work, inputting technical data and writing the prototype program.

Alexander said he decided to work in Smalltalk-80, one of three AI languages offered on the 4404. Smalltalk-80 (offered under license from Xerox PARC) was selected because the language's graphics capabilities particularly suited the solutions Alexander wanted.

Initially, the repair technicians felt graphics could help by providing waveform representations at particular test points. Because the graphics are available in Smalltalk-80, the researchers included virtually every drawing and schematic available for the FG-502. During a typical troubleshooting session, the technician may see several diagrams on the screen at the same time. A portion of a schematic diagram, a drawing of the printed circuit board area, a list of components, and the correct voltage readings and waveforms at the indicated component terminals can appear onscreen simultaneously.

Alexander also pointed out he was not an experienced Smalltalk user when he began the program. Although he said his knowledge of the language could be described best as "slightly past beginner," he now considers Smalltalk the preferred language for expert systems. The 4404 can also use Lisp or Prolog.

The 4404 is built around the 32-bit Motorola 68010 microprocessor and borrows heavily from Tektronix existing terminal technology. It is available for less than \$15,000.

—B.F.

Backward chaining can be used to focus a set of forward chaining rules on a particular goal, or forward chaining can be used to rate the likelihood that the facts will satisfy alternative subgoals.

ART is available on the Symbolics 3600, LMI Lisp machines, and VAX/VMS-Lisp. Prices range up to \$100,000, depending on the amount of training provided. Digital Equipment Corp (Maynard, Mass) has a semi-exclusive license to market ART on the VAX. Among other applications, ART has been used to build the Navics console control system at NASA's Johnson Space Center.

## A multilevel approach

Teknowledge is entering the AI marketplace by offering three different products—a tutorial package called T.1, a prototyping tool called M.1, and a full-scale expert system

development kit called S.1. The T.1 and M.1 packages run on an IBM PC, while S.1 requires a Xerox 1100 series machine or a VAX/VMS.

Unlike most expert system kits, M.1 is built in Prolog. It is a backward-chaining, rule-based kit that can build a small expert system (about 200 rules) or a prototype. Oriented to programmers without AI experience, M.1 features a multiwindow display, interactive debugging, and automatic question generation. The M.1 \$12,500 price tag includes a training course in addition to a year of maintenance.

M.1 addresses a similar marketplace as the TI Personal Consultant. Designed to run on the TI Professional Computer, this package can create an expert system with up to 400 rules. Personal Consultant is based on the EMYCIN system pioneered at

(continued on page 37)



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- TI's single-chip, high-performance TMS32010 digital signal processor (DSP) assures highest quality telephone transmission (Page 2).
- TMS320 DSPs from TI support high-speed and numeric-intensive applications from communications to seismic processing (Page 3).
- Complete development support for TI digital signal processors includes hardware, software, documentation, and application workshops (Page 4). ▶

# TI digital distortion

When you're depending on the telephone to get your message through, you don't need "singing" on the line. A standard two-wire circuit "sings" when signals traveling in opposite directions are insufficiently isolated in a repeater. To eliminate this problem, Lear Siegler, Inc., manufacturer of repeaters used worldwide, relies on the Texas Instruments TMS32010 digital signal processor (DSP). And cuts setup time for each repeater from hours to minutes.

In the unique VFR-7608 repeater, TI's TMS32010 performs all the functions of analog equalizers, filters, and amplifiers (see diagram opposite). It compensates automatically for line impedance 8,000 times per second. Completely isolates the opposing signal streams. Puts an end to "singing."

## TMS32010 eliminates reflections "by the numbers"

The standard solution to "singing" is an analog network designed to cancel out reflected signals on the line. But even with expensive "precision" hybrids, the best solution is a compromise that limits usable bandwidth and gain.

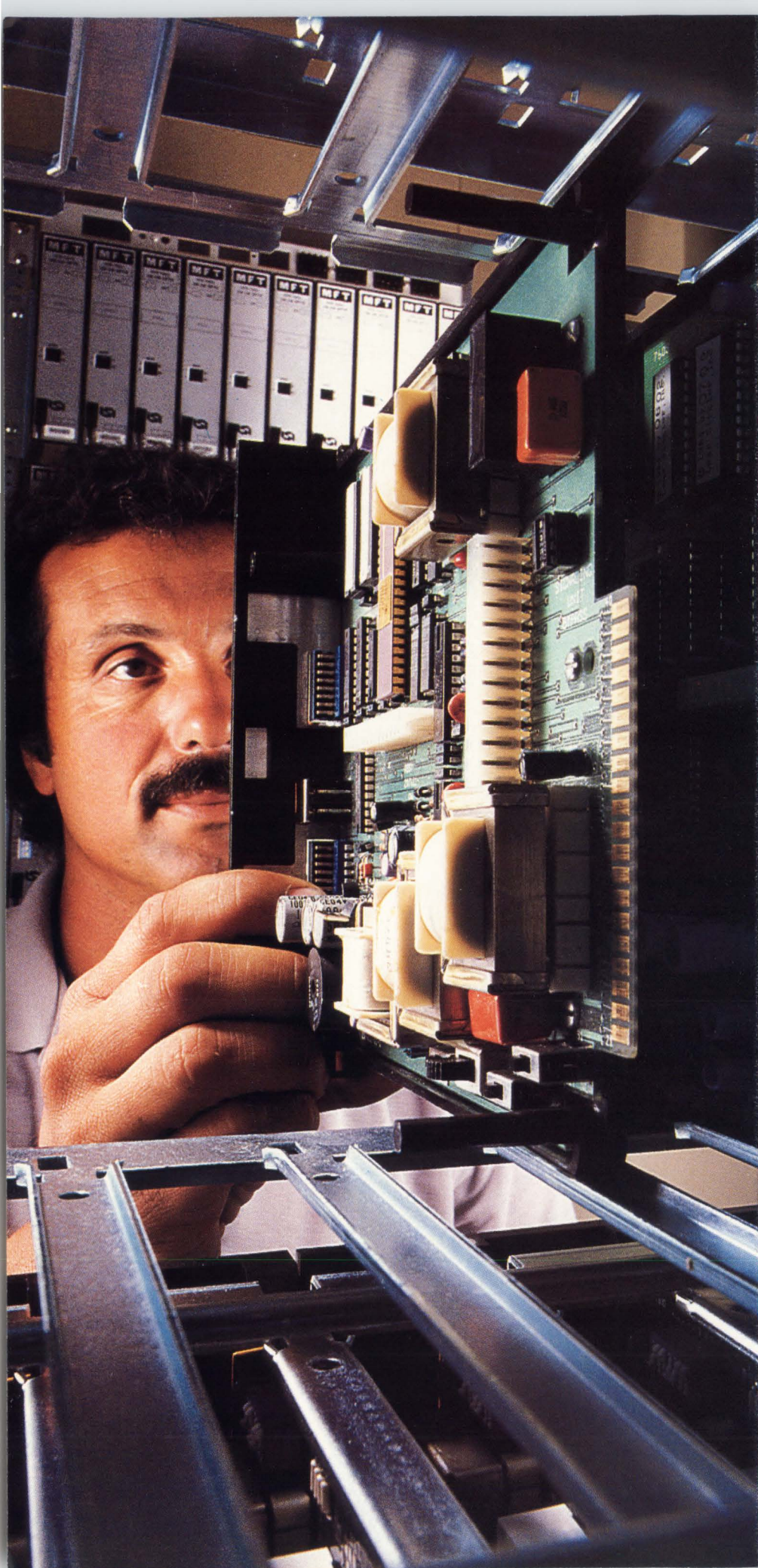
Digital signal processing with the TMS32010 balances the circuit across the entire frequency band every 125  $\mu$ s. Because the repeater adapts continuously, the circuit *cannot* "sing" at any frequency, and its gain can be fully utilized.

## DSP cuts setup time to minutes

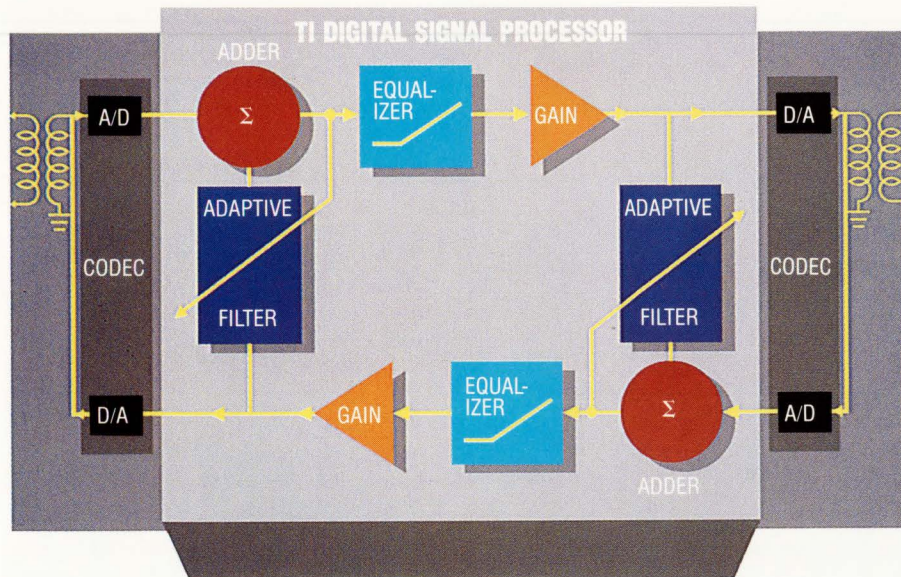
Tuning each analog repeater is an hours-long, trial-and-error procedure for a highly skilled technician. Using a comprehensive history of each circuit, he must set 68 switches in an analog repeater. TI's TMS32010 in Lear Siegler's new digital repeater eliminates 65 of those switches. Ends the need to keep detailed circuit histories. And the small, affordable plug-in unit is interchangeable with older repeaters.

So your message can always come through—loud and clear.

◀ **Setup is as simple as 1-2-3** with Lear Siegler's adaptive telephone repeater using TI's TMS32010 DSP. Whereas manual adjustment of an analog repeater can take many hours, only three simple switch settings are required to assure rock-stable, "sing"-free performance from the digital repeater.



# signal processor squelches in unique adaptive repeater.



Heart of the adaptive repeater is TI's single-chip, 16/32-bit TMS32010 digital signal processor. All the functions shown are achieved in real time through software operating on signals digitized by conventional single-chip codecs.

The TMS320 family, with its extensive development support (see page 4), can handle all the signal processing for spectrum analysis: Autocorrelation, windowing, fast Fourier transforms—performing a 64-complex-point FFT in only 550  $\mu$ s. And for seismic processing involving very low frequencies which only a digital system can implement.

Image enhancement, pattern recognition, and data compression are all possible with TMS320 processors. They can extract features and perform template comparisons for optical character recognition.

## A one-chip alternative to bit-slice processing

TI's 16/32-bit TMS320 DSPs offer an inexpensive alternative to multichip bit-slice processors. They combine the flexibility of a high-speed controller with the numerical capability of an array processor—on a single chip, in one 40-pin DIP.

Highly pipelined architecture and a comprehensive instruction set give the TMS320 the speed to execute five million instructions per second with 32-bit precision: More than fast enough, for example, to handle the 40 additions and 40 multiplications necessary for realtime voice-frequency processing within the 125- $\mu$ s sampling interval. A conventional microprocessor, operating at 8 MHz, would require 900  $\mu$ s, and quickly become bogged down in the signal stream.

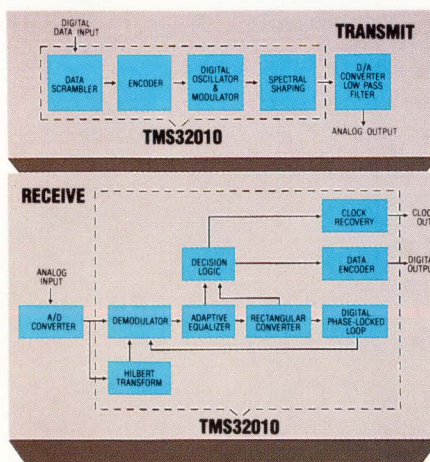
## The TMS320 family from Texas Instruments: "Workhorse of digital signal processing."

The TMS32010, first member of the TMS320 DSP family, is TI's trailblazing contribution to an important new technology. A Lear Siegler engineer who has been following the progress of digital signal processing from its inception says, "The TMS32010 is the first device that can reliably do what we need. It's a real workhorse: The '8080' of DSP."

### TI's TMS320 DSPs excel at high-speed, numeric-intensive applications

High-performance TMS320-family DSPs from Texas Instruments will find widespread use in many fields where large volumes of high-speed computation are required. In telecommunications, they can also be used to build high-speed modems with data-transmission rates up to 9,600 baud. They can make speech recognition, analysis, and synthesis practical. Speed image processing and pattern recognition. Facilitate high-speed process control and instrumentation. Process radar, sonar, and seismic signals. And furnish the multiple functions often required for a single application.

For example, a TMS320 DSP could enable an industrial robot to synthesize and recognize speech, sense objects and their orientation, and perform mechanical operations through digital servo-loop computations.



High-speed modem functions are effectively performed by TI's TMS32010, as well as such expanded functions as auto-dial/answer, dial-tone verification, busy-signal detection, and self-test routines.

### Now in three versions

The TMS32010 microprocessor has 288 bytes of on-chip data RAM, and can address up to 8K bytes of off-chip memory at full speed.

The TMS320M10 microcomputer is identical to the TMS32010, but it also includes 3K bytes of on-chip mask-programmed ROM.

The military version, SMJ32010JDS, is processed to the extended temperature range requirements of MIL-STD-883B.

To learn more about the many applications and available development support for TMS320-family DSPs, return the coupon on the following page.

See back page for more information.





In-depth support for the TMS320 family of TI DSPs includes a host-independent development system, an evaluation module, emulator and analog interface board, as well as assembler/linkers and simulators that can run on a variety of host computers and PCs. Documentation is extensive and thorough.

# Develop your own DSP applications with comprehensive support from TI.

Texas Instruments has assembled an extensive group of development-support packages for the TMS320 family of VLSI digital signal processors (see table). Included are all the hardware, software, and documentation you need to utilize the power and speed of TMS320 DSPs in your designs. A rapidly growing volume of third-party support is also available.

## Use your own PC as a TMS320 development station

The latest addition to TI's development-support software is the TMS32010 Digital Filter Design Package developed by Atlanta Signal Processors Inc. It makes your Texas Instruments Professional Computer or IBM PC a cost-effective, easy-to-use, digital-filter design

### TMS32010 Software and Hardware Support

Host Computer	Operating System	Part Number
<b>Macro Assembler/Linkers</b>		
TI990	DX10	TMDS3240120-08
DEC VAX	VMS	TMDS3240210-08
DEC VAX	Berkeley UNIX 4.1	TMDS3240220-08
DEC VAX	Berkeley UNIX 4.2	TMDS3240230-08
IBM	MVS	TMDS3240310-08
IBM	CMS	TMDS3240320-08
TI/IBM PC	MS-DOS	TMDS3240810-02
<b>Simulators</b>		
DEC VAX	VMS	TMDS3240211-08
TI/IBM PC	MS-DOS	TMDS3240811-02
<b>Hardware</b>		
Evaluation Module (EVM)		RTC/EVM320A-03
Analog Interface Board (AIB)		RTC/EVM320B-06
Emulator		TMDS3262210

station. With it you can produce the TMS32010 source module. Then you can assemble the code and simulate it in software on the PC. Later you can download the code into the hardware-development system for realtime emulation.

Two versions are now available: **DFDP-TI001** for the Texas Instruments Professional Computer, and **DFDP-IBM001** for the IBM PC.

## Learn in TI workshops

Texas Instruments supplies comprehensive documentation with each device. A growing library of application reports will also assist you in the design of digital signal processing circuits using TI's TMS320 DSPs.

Three-day DSP workshops, including extensive hands-on experience, are conducted periodically at Texas Instruments Regional Technology Centers. For registration information, call the Regional Technology Center nearest you: Atlanta, (404) 452-4686; Boston, (617) 890-4271; Chicago, (312) 228-6008; Dallas, (214) 680-5096; Northern California, (408) 980-0305; Southern California, (714) 660-8164.

Texas Instruments Incorporated P.O. Box 809066  
Dallas, Texas 75380-9066

SPR0630S400C

Please send me information about:

- PR 22  TI's TMS320 family of Digital Signal Processors.  
PR 24  Third-party support for the TMS320 family.

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## Do-it-yourself tools

(continued on page 32)

Stanford University. Although the \$3000 cost is substantially lower than M.I, training classes and onsite support are optional.

S.1 is a backward-chaining, rule-based system that includes frame-based representation. Although users primarily enter If-Then rules, S.1 can store frames that describe objects and their relationships. According to Teknowledge, S.1 has fewer functions than KEE or ART, but is easier to use. S.1 is designed for applications that require "structured selection." This is loosely defined as problems with definable solutions. Thus, S.1 would be appropriate for applications such as diagnosis or consultation, but not for design. General Motors is currently using S.1 to build a car diagnosis system.

## Using fuzzy logic

Infotym's Reveal is a Pascal-type language with a set of development tools for building expert systems. Tailored for the corporate environment, Reveal combines expert system development with a decision support modeling tool. Reveal is a rule-based

system best suited for applications with a few hundred rules. Although Reveal was introduced in the United States this fall, it has been available in the United Kingdom for a year, where it has been used to write expert systems for insurance underwriters and commodity brokers.

Reveal is a complete programming language that can be used for general-purpose programming as well as AI applications. It can also be used to build a customized inference engine—although a pre-built, backward-chaining inference engine will be available with a revised Reveal in the future. Infotym representatives claim that building an inference engine with Reveal does not require AI expertise. "This product will demythologize the building of expert systems to a wider community," says Infotym's Wong.

The language makes use of fuzzy logic, a principle pioneered by University of California at Berkeley mathematician Lofti Zadeh. Fuzzy logic allows degrees of truth to be assigned to statements. A fuzzy set is a set that does not have a crisply defined membership, but allows objects

to have grades of membership, or truth values between 0 and 1.

Such user-defined linguistic variables as "large," "small," or "high" are allowed in Reveal. To evaluate those variables, truth values are scaled numerically from 0 to 1. Reveal will then provide answers to problems with numerical confidence factors. This "approximate reasoning" capability allows Reveal to evaluate imprecise information. While kits such as S.1 allow numeric "certainty factors," Reveal provides the linguistics for approximate reasoning.

## Inducing rules from decisions

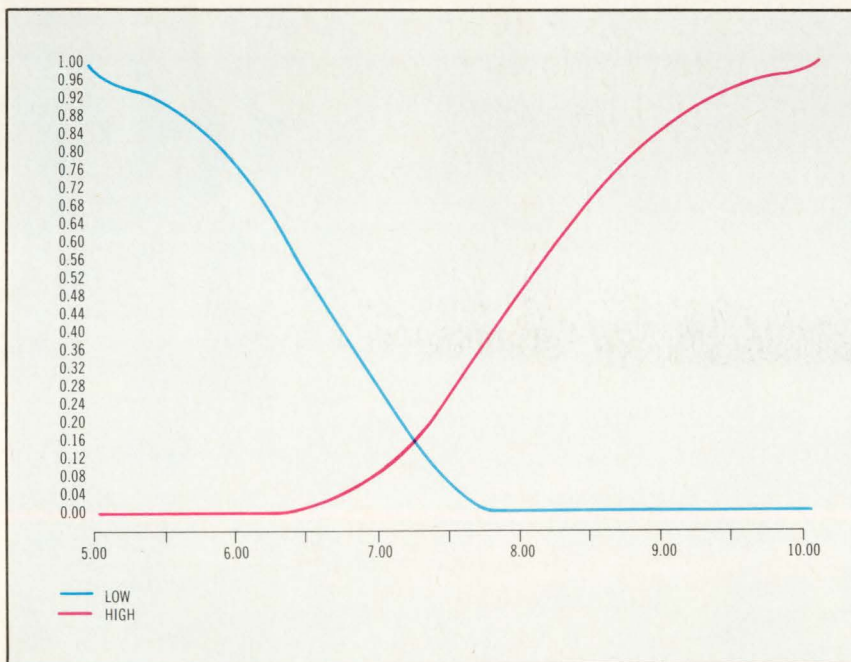
Although most expert system kits require the user to enter rules, two kits induce rules from examples of decisions. These kits are based on the work of University of Edinburgh professor Donald Michie, who has identified the difficulty of articulating rules as a major bottleneck in expert systems development. From examples of previous decisions, these kits can build decision trees and generate rules to solve specific problems.

Suppliers of these systems say it is easier to give examples than dictate rules. Often, they say, a knowledge engineer is required to extract those rules. Competitors point out that one would have to give a lot of examples to cover even a limited application. For the user, the bottom line may be personal preference—whether one finds it easier to use frames, rules, or examples of decisions.

Radian Corp's Rulemaster package includes RuleMaker, an inductive generator of decision trees, and Radial, a Pascal-type language for expressing and executing rules. Thus, the user can enter explicit rules as well as examples, and Radial can explain a line of reasoning. Like Reveal, Radial uses fuzzy set theory to evaluate such variables as "high" or "low." Written in C for Unix-based systems, Radial also permits an interface to Fortran, Pascal, Lisp, or C.

Jeffrey Perrone and Associates offers a low end system for IBM PCs that induces rules from examples. Called Expert-Ease, this package

(continued on page 39)



A fuzzy set allows variables such as "low" and "high" to be defined by truth values between 0 and 1. The chart indicates that a value of 5 will always be considered low, while a value of 6 is "mostly" low. A value of 7 is equally high and low. Reveal and Radial are two languages allowing this type of representation.

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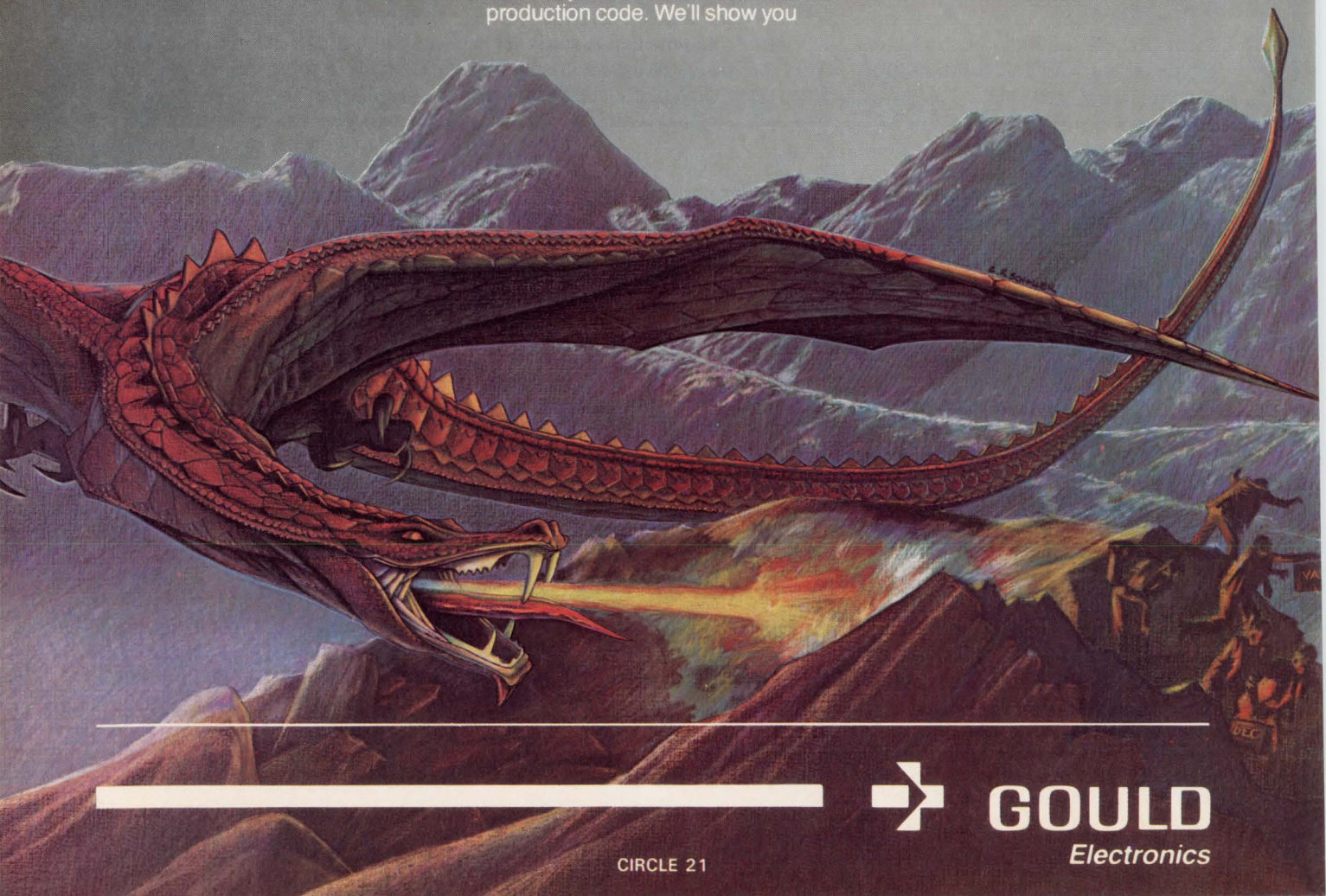
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## Do-it-yourself tools

(continued from page 37)

provides capabilities similar to Rule-Maker. It does not have a language like Radial and cannot explain a line of reasoning. However, Expert-Ease's low cost, easy-to-use interface, and high speed decision-making capabilities have made it a popular package. It has an installed base of more than 200, found mainly in business and academic environments.

## Logic-based programming

Logic-based programming languages—those that are based on predicate calculus—can be used to build expert systems. While such procedural languages as Pascal or Lisp describe how to compute a result, logic-based languages specify what result is desired. As previously mentioned, KEE revision 2.0 allows logic-based programming. Smart Systems sells Duck, a logic-based language that provides an inference engine with support tools. The Arby expert system shell will be written in Duck.

Duck provides the capability to update its reasoning strategy. It can reason with assumptions or incomplete information by assigning default values for variables. If the assumption was false, Duck can go through the knowledge base and update all related data. Duck is now implemented on the Symbolics 3600, on FranzLisp running on a VAX, or TI Lisp on Apollo workstations. It can also be ported to other machines that run Lisp.

Prolog is a logic-based language also, and is the major AI language in Europe. Because it is a higher level language than Lisp, Prolog may not require the simplified user interface and the array of development tools offered by Lisp-based kits. Although Lisp has been the language of choice in the American market, Prolog is now making inroads. Logicware (Toronto, Ontario) is marketing MProlog, a refined, programmer-friendly version with support tools. In November, Quintas Computer Systems (Palo Alto, Calif) introduced Quintas Prolog, a development package that runs on VAX/ Unix, VAX/ VMS, and the Sun Microsystems workstations.

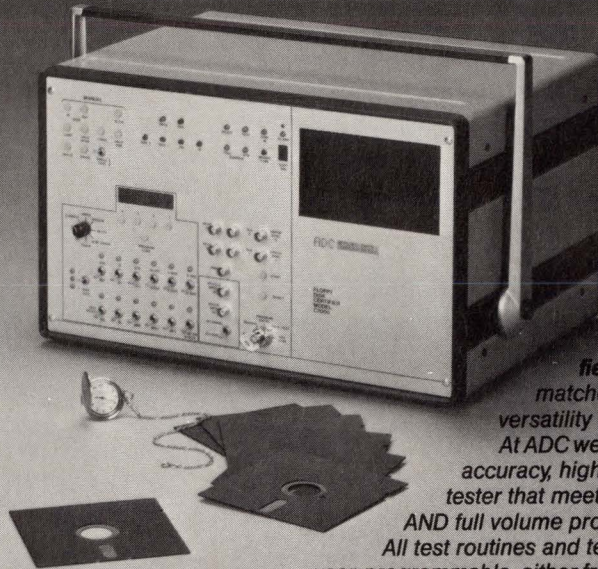
Users who want to build expert systems have many options other than sophisticated development kits. There are many versions of Lisp available, including IBM's new Lisp/VM, which comes with a set of development tools. The Tektronix 4404 workstation runs Smalltalk-80, FranzLisp,

and Prolog. A wide range of tools ensures that expert systems can be built using many approaches, on many different machines, with almost any desired level of support.

—Richard Goering, Field Editor

**SYSTEM TECHNOLOGY**  
(continued on page 46)

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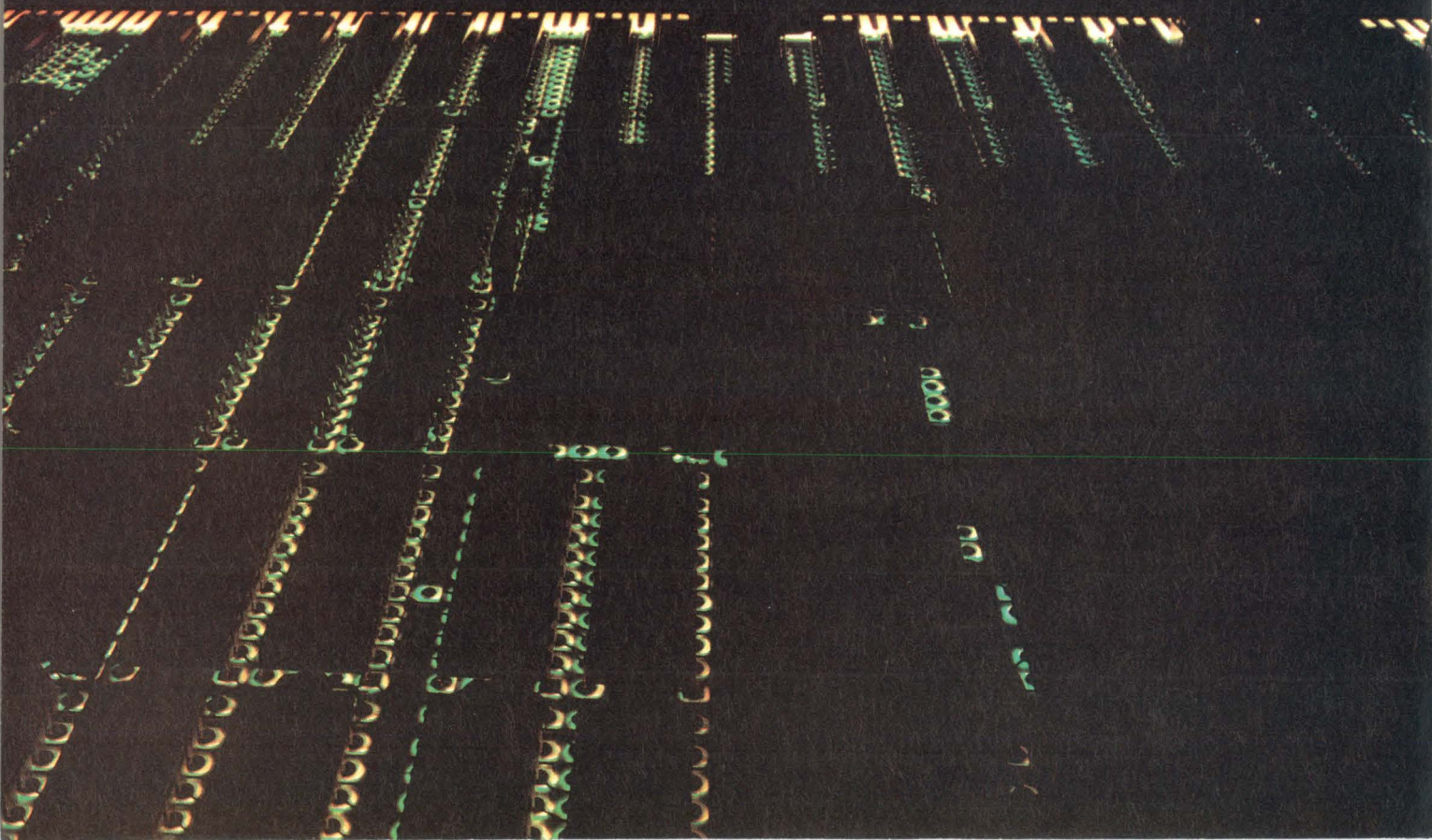
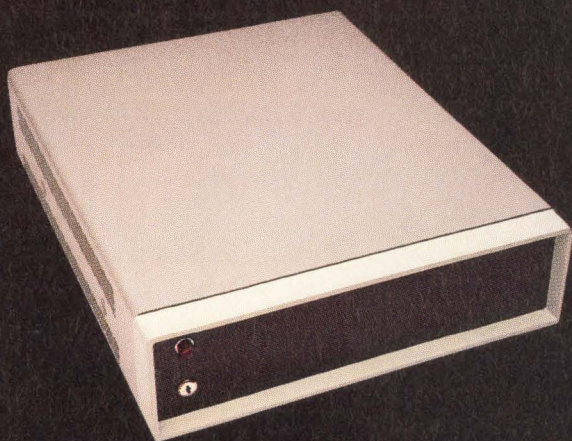
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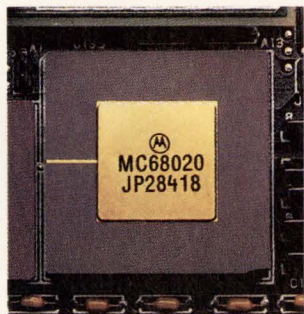
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To help you quickly evaluate the MC68020, the Benchmark 20™ system package uses the 020bug™ Debug/Monitor firmware package to allow you to do benchmarking and to debug code. The 020bug resident package permits quick execution of system and user-developed programs running on the

Benchmark 20 system package. Its powerful software and system debug command set allows access to all I/O, control, and memory facilities plus the full 4-gigabyte direct address range of the VERSAbus™ system bus.

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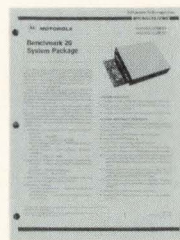


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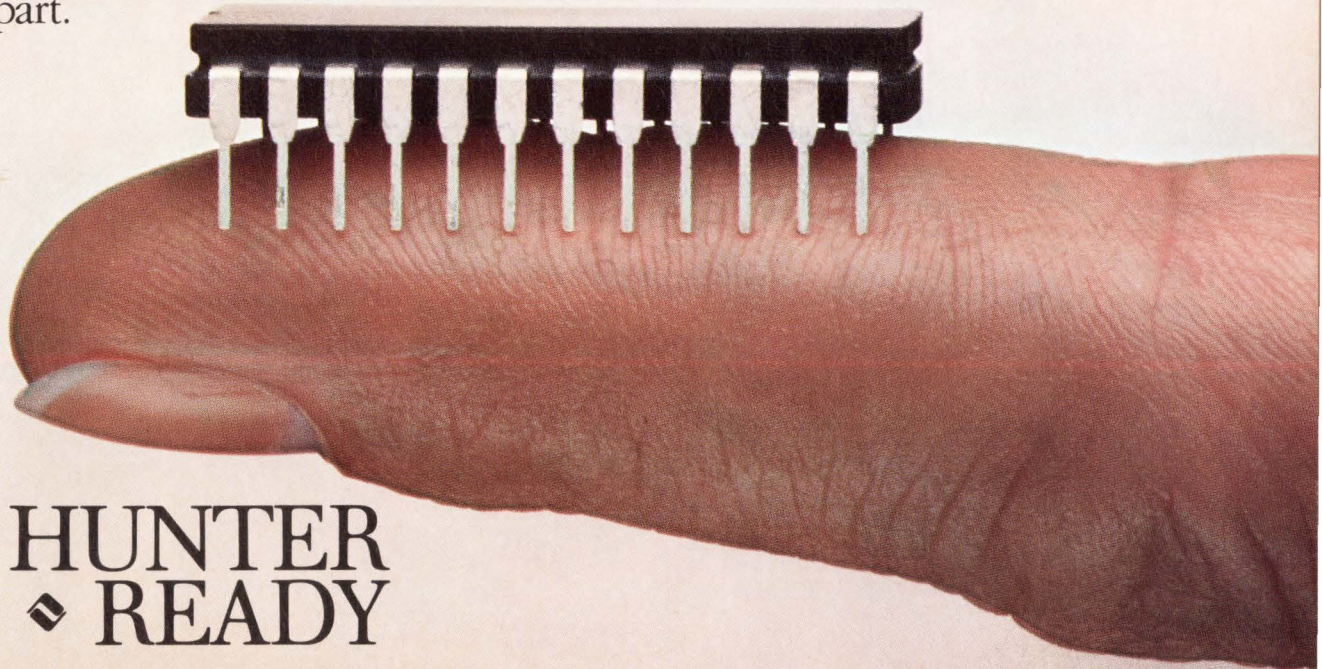
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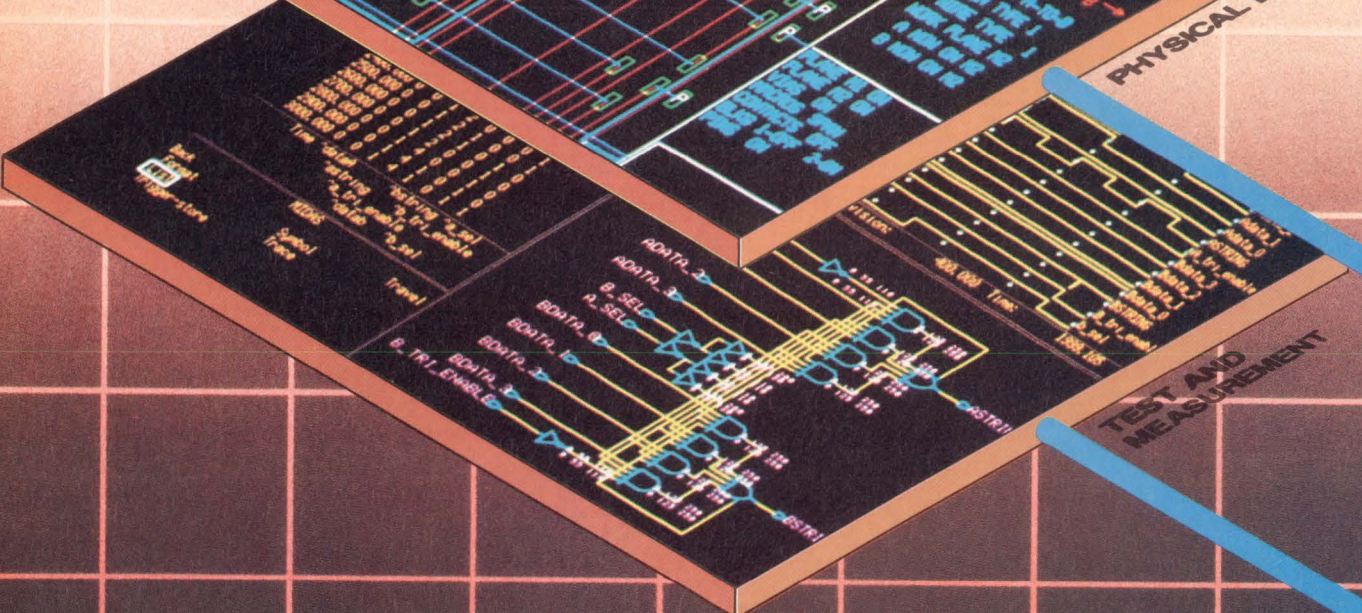
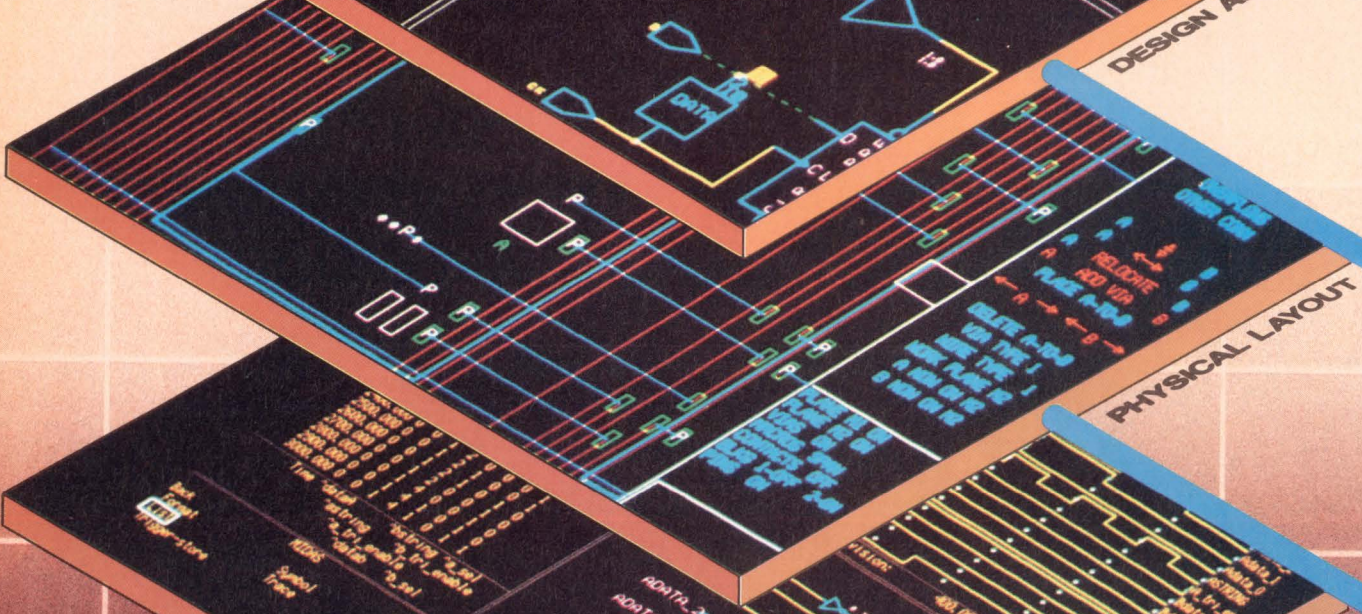
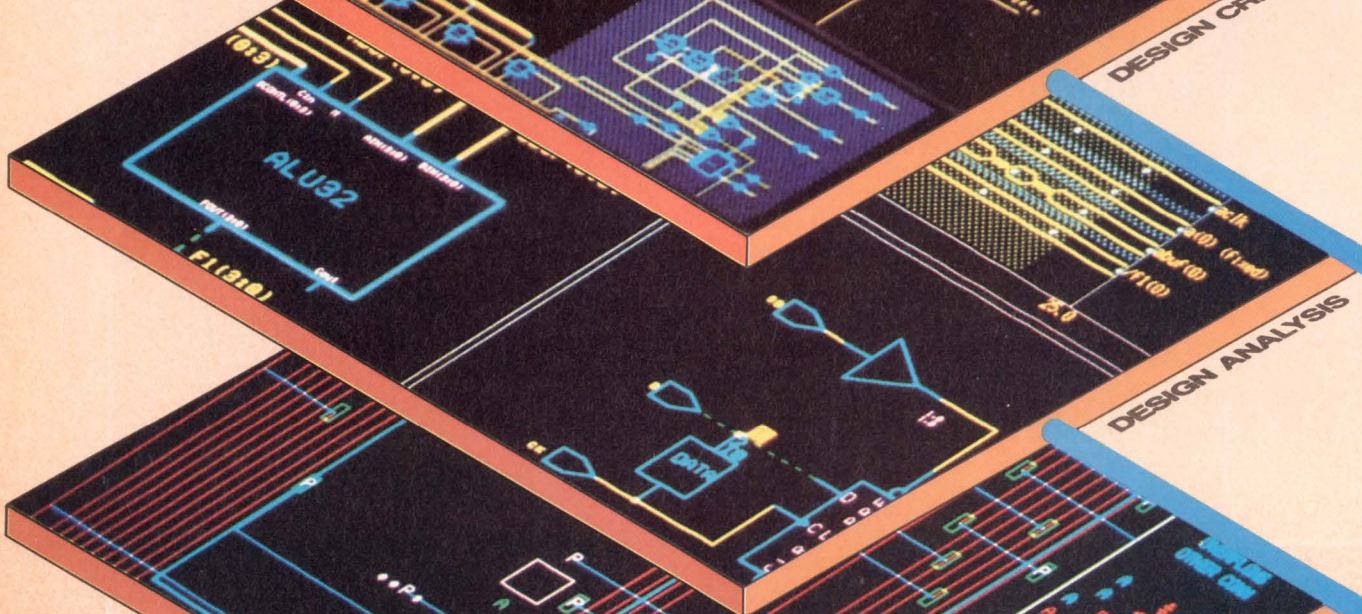
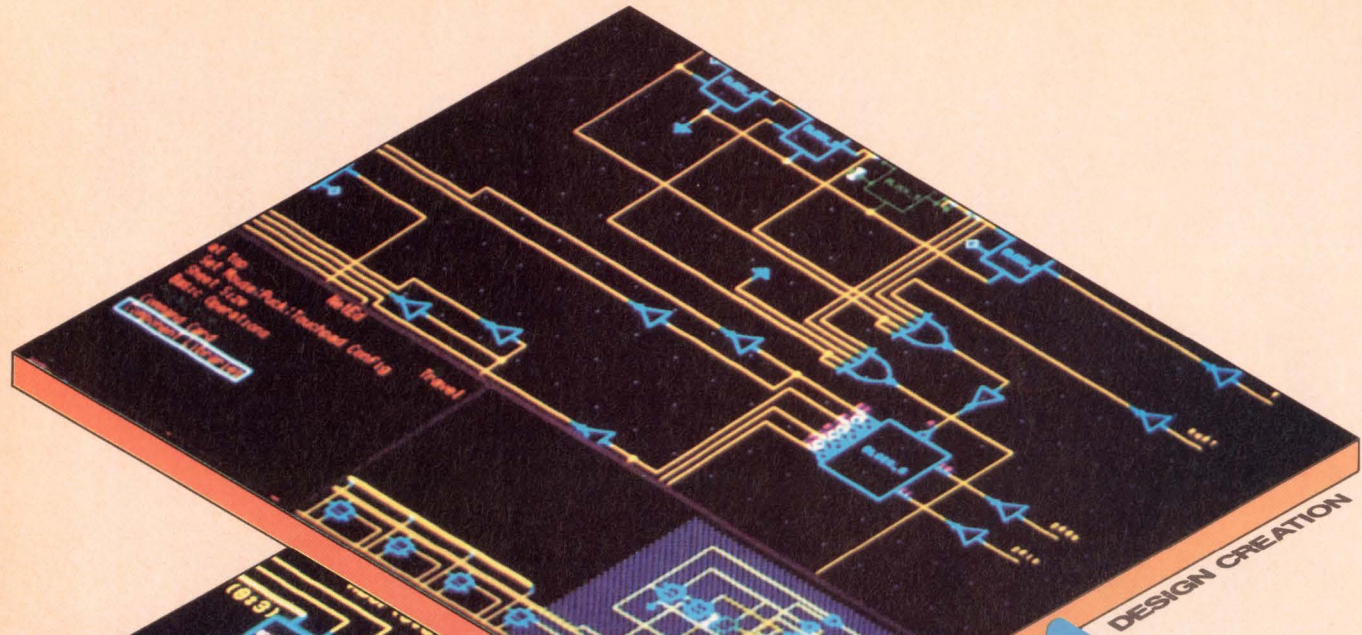
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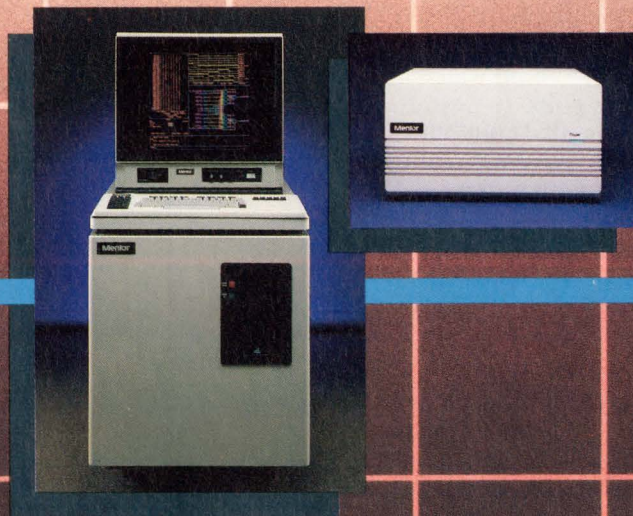
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## Bipolar building blocks well-suited for fast, flexible 32-bit CPUs

In between the realms of general-purpose MOS microprocessors and full-custom CPUs built from gate arrays (and full-custom VLSI), a place exists for a range of high performance CPUs. Advanced Micro Devices filled this niche in the past with its redoubtable 2900 and 29116 bipolar bit-slice families. Those bit-slice parts divided CPU functions vertically and allowed the designer to build processors of almost any data width.

Given the growing popularity of 32-bit architectures, AMD (Sunnyvale, Calif) believes a 32-bit data path will be chosen for many systems far into the future. At the same time, according to Lyle Pittroff, AMD's director of strategic marketing for its bipolar division, "There is still a need for high performance CPUs that can be tailored to the specific needs of the systems into which they are being designed."

With this in mind, AMD has drawn certain conclusions about the design philosophy of its next generation of bipolar processor parts. Rather than the same vertical bit-slice partitioning used in the 2900 family, AMD has functionally divided up the CPU functions based on a fixed 32-bit data path. Thus, instead of vertically partitioned bit-slice functions, the recently announced Am29300 family has horizontally partitioned building blocks. The initial chips in the 29300 family consist of a 32-bit ALU, a 64- x 18-bit register file, a 16-bit wide sequencer, a floating point processor, and a 32- x 32-bit parallel multiplier.

### Trade-offs in ALU design

The trade-offs in horizontal versus vertical partitioning become apparent in the design of the ALU. In bit-slice parts the register file is incorporated into the ALU, but in the Am29300 family the register file is kept as a separate part. The Am29334 is a 64-word, 18-bit file. Two of these can combine to make a file of sixty-four 32-bit registers, plus 4 bits of parity. On the other hand, functions that are difficult to incorporate into bit-slice

ALUs are built into the Am29332 ALU. These include the mask generator, the 64-bit funnel shifter, and the priority encoder.

The system architecture attains its optimum level of performance when the component architectures do not interfere—"when they stay out of the way," according to Pittroff. A key objective of the project is to allow designers to work with a machine having instructions that execute in a single cycle.

Thus, multiple I/O ports exist throughout the Am29300 family. For instance, both the Am29332 ALU and the Am29325 floating point processor have two input buses and one output bus to avoid the problem associated with switching a bidirectional bus halfway through the cycle. I/O registers can be used for pipelining, but nothing in the Am29300 family's architecture requires it.

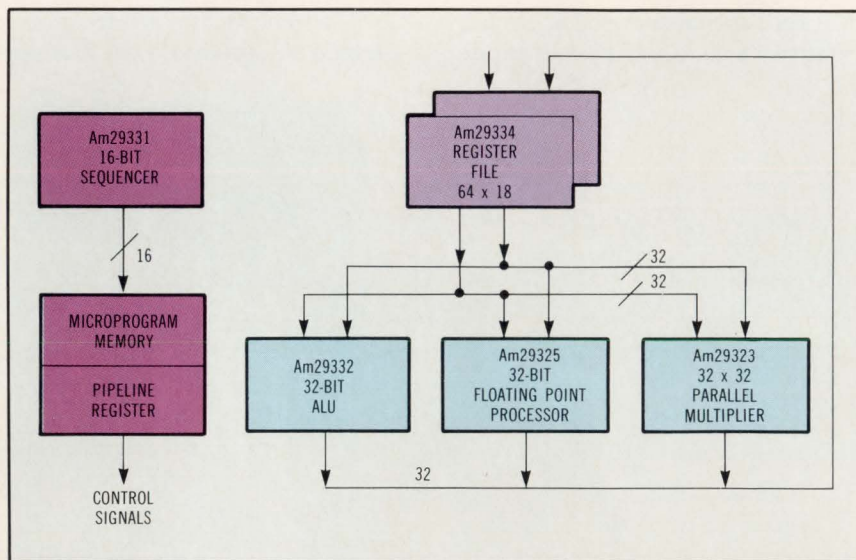
The simplest form of CPU can be built using the Am29332 ALU and two Am29334 register files with the Am29331 sequencer. This would produce a 32-bit CPU with up to 64,000 words of control store and sixty-four 32-bit registers with parity. Registers of any depth, "accelerators," the

Am29325 floating point processor, and the Am29323 multiplier can be added to this basic design.

The ALU chip includes a 32-bit wide ALU with full carry lookahead and a three-port structure—two input ports, one output port, and a mask input that is used on every cycle. The mask supports byte-aligned and field-logical operations on variable-position, variable-length fields. It can control the width of an operation on each instruction without any cycle time penalty. It also contains a 64-bit funnel shifter that can do an n-bit shift or rotate in conjunction with an ALU operation in the same cycle. A 32-bit status register and a priority encoder are also incorporated. All these functions would be hard to include in a bit-slice type ALU because different bit ranges would require different code to control them.

The Am29331 sequencer incorporates 16 bits of address, realtime interrupt, and a 33-level stack. The instruction set can handle sequential execution, branches, subroutines, and loops. Its interrupt feature allows it to handle traps at the microinstruction level. Such traps can be triggered

*(continued on page 48)*



In the Am29300 family, all data paths among the processors are 32 bits wide with 4 parity bits. The register files can be stacked to any desired depth.

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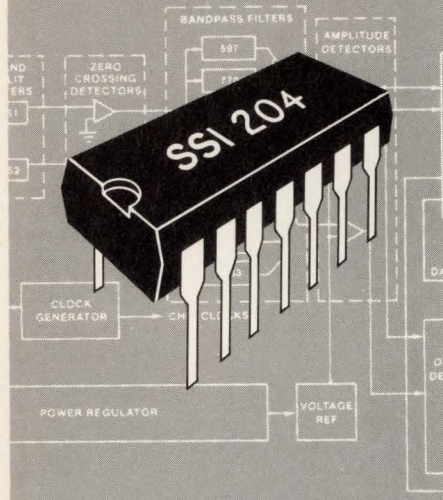
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CIRCLE 27

## MICROPROCESSORS/MICROCOMPUTERS

### Bipolar building blocks (continued from page 46)

by specific system events, such as parity error on the ALU bus. For multitasking operations, the sequencer has a hold pin to let designers use multiple sequencers with only one active sequencer at a given time. Multiple sequencers address the same microcode memory, allowing fast context switching at the microcode level.

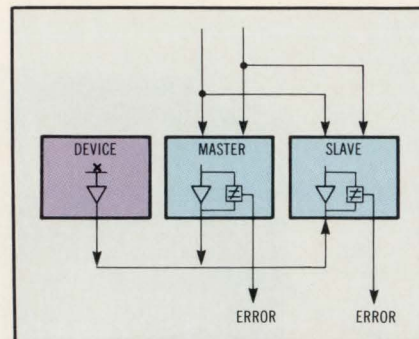
As is the case with the ALU and floating point processor, the sequencer has two separate branch address inputs—both of which can be used to load the counter. The D port can load or unload the stack while the A port is inputting a branch or map address. Using more ports allows more parallelism. In this manner, the sequencer avoids the overhead of a tri-state bus.

The two accelerators that are to be announced with the family are aimed at accomplishing their tasks with single-cycle instructions. The floating point processor executes floating point operations plus format conversions in a single cycle. It can convert between floating point and integer, and between IEEE and DEC floating point formats. As with the other family members, the floating point processor has two input buses and one output bus and no internal pipelining. Pipelining can be done with the I/O registers, but they can also be made transparent.

The Am29323 multiplier can perform a complete 32- x 32-bit clocked multiplication in a single cycle. Both input ports have 32-bit registers. The output port can select from among a 67-bit product register, a 32-bit temporary register, or the 32 x 32-bit array directly. Pipelining is available for multiprecision operations, if needed. If one uses the I/O registers for pipelining, it is possible to overlap 64- x 64-bit operations and obtain a 128-bit product every 4 cycles.

### Fault detection

The Am29300 family supports two levels of fault detection: data path parity and master/slave detection. Parity is not carried through the internal logic of the devices, but is checked on input and generated on output in order to check it at the next



**In master/slave error checking, the slave performs all computations in parallel with the master. If there is a discrepancy, a microinstruction interrupt can be generated.**

input. This parity checking is built in and, therefore, is essentially free.

The master/slave mode provides closer monitoring of the internal logic. These two devices operate in parallel—one does the actual computation and the other performs the same operations for comparison. The slave is able to check the results on a cycle-by-cycle, bit-by-bit basis. Any discrepancy will trigger a microinstruction interrupt.

AMD is also announcing a set of software development tools to provide support for microcode software development support. A definition program allows the user to set up a file that describes each microinstruction, field-by-field, and to define the name and length of each microinstruction. A microcode assembler is then used to generate output that can be relocated. A linker can then relocate and link code modules to be loaded into writable control store or burned into PROM.

The Am29300 family is made using AMD's high speed bipolar process called IMOX. The internal circuits are ECL, but all I/O circuits provide TTL levels to facilitate interfacing. Samples of the Am29325 floating point processor will be available at the beginning of 1985, with the other members of the family appearing in sample quantities about mid-year.

—Tom Williams,  
West Coast Managing Editor

SYSTEM TECHNOLOGY  
(continued on page 50)

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## Artificial intelligence key to computer integrated manufacturing

Despite some system manufacturers' claims to the contrary, computer integrated manufacturing is not yet a reality. Available systems are affordable only to large companies such as General Electric, General Motors, and Westinghouse. Smaller companies—even the mid-sized ones—cannot pay the bill. But of even greater importance is the lack of adequate artificial intelligence. Without artificial intelligence, none of the CIM systems can be practical.

### Hedging the bet

Most experts predict that CIM will not come of age for at least 5 or 10 years. Many others are even more pessimistic; they believe a minimum of 15 years is probable. William H. Slautterback, director of manufacturing systems at Koppers Co in Baltimore, Md, for example, thinks the year 2000 is a likely target. "Manufacturing will change more in the next 15 years than it has in the last 75," says Slautterback. "It is not a matter of if we will implement [the necessary] technologies, but when." All depends on whether or not the expected equipment and technological developments take place.

Larry Goshorn, the president and founder of International Robomation/Intelligence in Carlsbad, Calif, is also pessimistic about the timing—but is optimistic about CIM's future. He believes CIM will be realized only after artificial intelligence becomes practical. Goshorn emphasizes two approaches to CIM: the evolutionary and the revolutionary. The first fits into the plans for the next 5 years, while the second is probably as far as 10 years away.

Evolutionary CIM is based on the technology of the last 100 years. It uses existing machines and existing factories, but includes the addition of artificial intelligence technology. This does not mean the concept is necessarily wrong, however. For now, many companies have no

choice but to follow this path. They just cannot afford to experiment with unproven technologies.

In evolutionary CIM, current types of machines are regrouped into some form of cooperative order "to build the mentality of flexible manufacturing," according to Goshorn. Inspection, material handling, and machine tool operations, for example, are tied to a local area network for an electronically programmable, flexible manufacturing operation.

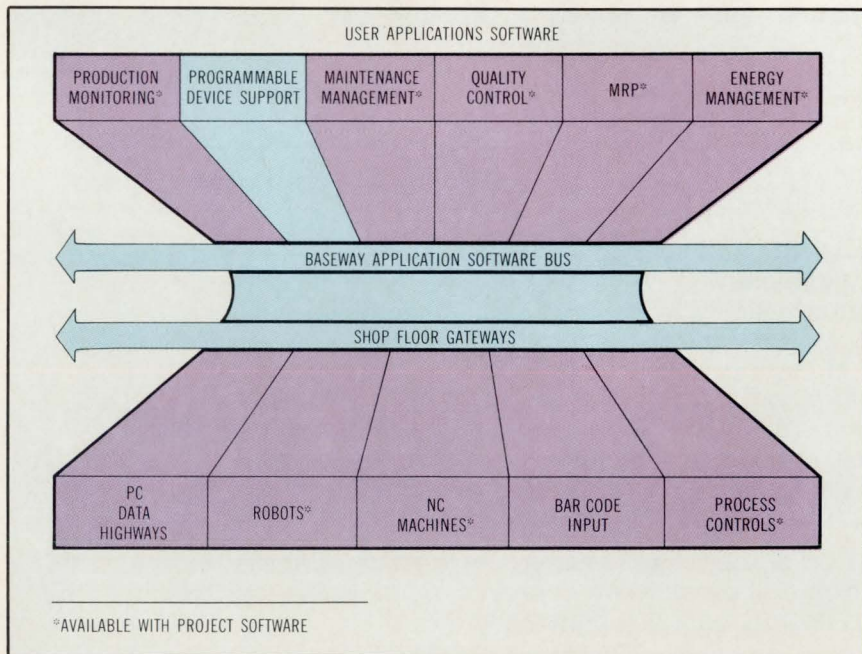
The revolutionary concept, however, involves major changes. It means dramatic new differences in the thinking of company management—as well as in that of system designers. According to this concept, machines will no longer be designed for humans to operate. "Humans will be designed into the machines," says Goshorn. AI periph-

erals will be joined by another important peripheral: expert knowledge or expert systems.

Operations on the factory floor today are based on machine specialization. In many cases the machine operator functions almost as an automaton for loading and unloading a machine. The "expert machinist" still exists and performs important tasks, however. That person looks at a print and then develops "an algorithm" of how to build the device shown on the print. Then the machinist, using several machines, builds the part shown on the diagram. The "algorithm," however, is based upon the human's "expert knowledge," not the machine's.

In the revolutionary era, single machine tools will perform all of what are now specialized functions.

*(continued on page 56)*



**Baseway application software, shop floor gateways, and programmable device support provide necessary communications between the industrial controllers and user applications software in DEC's CIM-like system. The programmable device support package uploads and downloads ladder logic programs between the host computer and the programmable logic controllers. Shop floor gateways poll the industrial controllers to collect information.**

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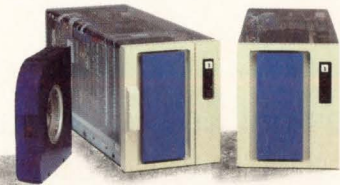
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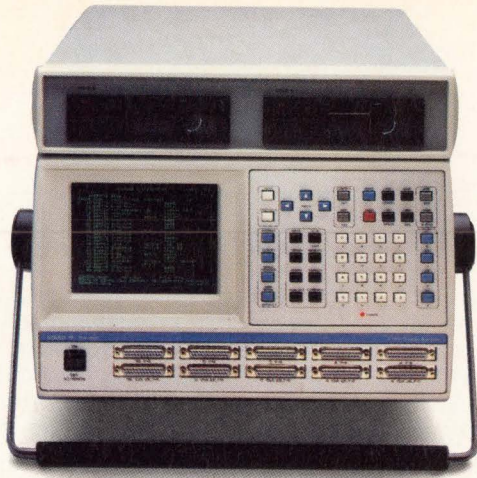
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## AI key to CIM

(continued from page 50)

Each machine will be expert at something. The operator will simply "plug in a drawing" and get out the intended product. AI or artificial peripherals in the form of expert systems will have provided the knowledge and capability.

Only a few people in the world are now working on revolutionary CIM. But Goshorn points out that all long range planners "have to know that the transistor is coming"—that the revolutionary approach is necessary for long-term success.

## Today's versions of CIM

While estimates vary on when CIM will be fully realized, several companies have introduced at least "quasi-CIM" systems. Understandably, the large system manufacturers—which are also the recognized computer system suppliers—are in the forefront.

General Electric, for example, is building an automated facility in Lynn, Mass for making helicopter engines. "Manned" by robots, the plant will operate 24 hours a day, 7 days a week, according to the Research Institute of America, a group based in New York City. Although output will be doubled, the plant will use only 100 workers, instead of 300, working 12-hour daily shifts.

GE's steam turbine-generator small parts manufacturing shop in Schenectady, NY provides still another example. That plant annually produces about 325,000 parts in thousands of different configurations. These facilities, as well as several others at companies such as General Motors and Westinghouse, come closest to true CIM. Such plants, however, are dependent on the availability of subsystems from many other manufacturers.

One recent introduction to the quasi-CIM field is the CIM/mechanical engineering system from Sperry Corp of Blue Bell, Pa. The company claims its CIM/ME system is the most highly integrated system available today in the computer aided design/computer aided manufacturing marketplace. But limiting it to CAD/CAM seems to be a confusion of terms. CAD/CAM is and will be

## AI will rule electronics systems of the future



All electronic systems designers—not just those involved with computer integrated manufacturing—must accept the importance of artificial intelligence for their systems of the future. Larry Goshorn, president and founder of International Robomation/Intelligence of Carlsbad, Calif, believes that AI is fundamental to any truly automated system. Yet he feels that most company planners do not understand or accept that.

Goshorn—a 25-year veteran of the computer automation battle—says that despite his experience even he nearly missed the importance of artificial intelligence. That error is evident in the name of his company. It should have been International Intelligence/Robomation—or even Artificial Intelligence/Robomation, he now believes.

"Most people," says Goshorn, "made the mistake that robotics would lead the way into the factory of the future. But time has shown that this is not the case." Goshorn said he has found in the last 4 years that companies can be in the AI business without being in robotics, but they cannot be in the robotics business without being in AI. "It is impossible to be in the robotics business alone."

[Perhaps that is one reason that a recent study by International Data Corp of Framingham, Mass shows projections for the robotics market to be far below those anticipated earlier by market analysts. Peter A. Cohen says in IDC's *Robotics* report that "the robotics market, with 1983 revenues of \$164 million, will grow to \$700 million by 1989." Predictions of only 3 years ago placed the 1990 market for robotics in the U.S. alone at \$1 billion.]

But this lack of understanding is not limited to just manufacturers of robots. In a recent sectional meeting of a chapter of the American Electronics Association, Goshorn found that "chief executive officers of most companies represented there had absolutely zero understanding of AI and its potential impact on their businesses." He accepts that this lack of knowledge could exist in 1977-78—but not in 1984. "Today there can be no question about the potential impact of AI products on the electronics industry. This is true not just for manufacturers of computers and integrators of factory automation systems."

Evident or not, computers—or at least electronically programmable devices—are now built into just about every piece of electrical equipment. Soon, AI concepts also will have to be designed into just about all equipment intended for future factory operations. This will be true whether in robotic applications or in the automated factories of tomorrow—or even of "later today."

Goshorn points out, however, that all AI components will act as peripherals to the central unit. And all AI peripherals will be dramatically different from peripherals as we now conceive of them. They will not just be printers, plotters, and such. Instead, they will be human-like sensors and they will perform human-like activities: eyes for sight, fingers for touch, and more. But the design concept will remain as it is today. The central unit will need to be developed first—with provision for the artificial peripherals. Then those peripherals will be added.

a subsystem of CIM, not the reverse. Although the CIM/ME is not a true CIM system, it comes closer than some of the others now available. The company boast that its CIM/ME this system is "the product other companies only promise."

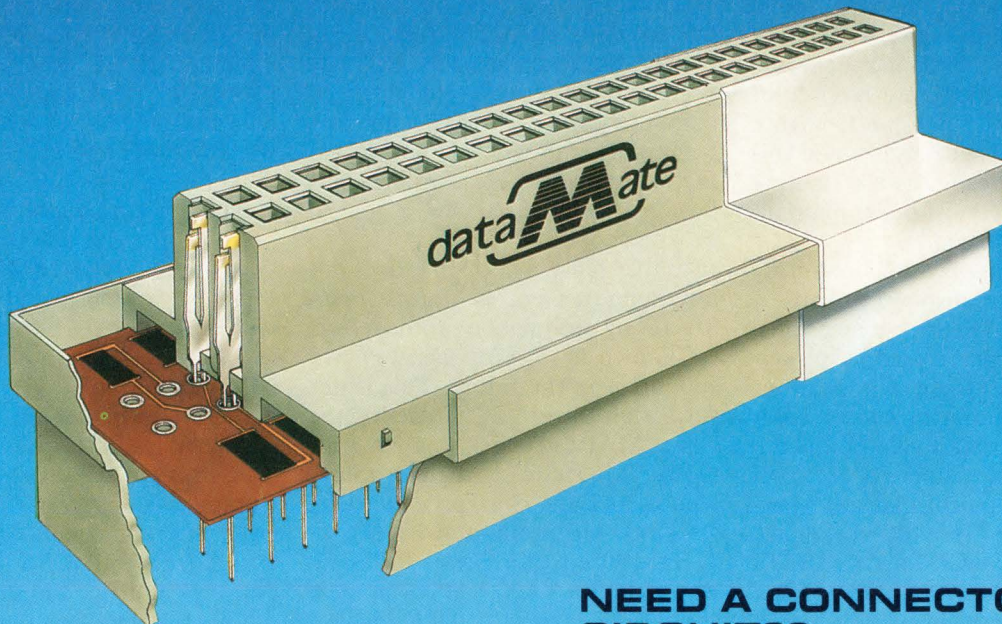
Sperry's system consists of four major modules: design, engineering

analysis, drafting, and numerical control. A Sperry series 1100 mainframe computer can handle up to 20 workstations. In turn, each workstation includes a minicomputer, a graphics display terminal, and local mass storage. Most of the system interactive operations are performed by

(continued on page 58)

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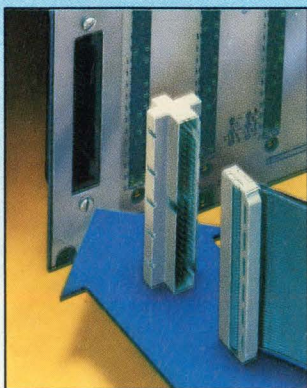
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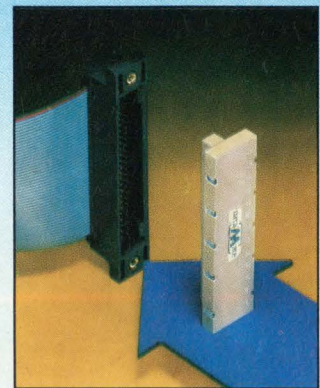
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CIRCLE 30

## AI key to CIM

(continued from page 56)

the workstations. This frees the mainframe to support other tasks.

Basic workstations are from Apollo Computer's Domain line. They range from the low level monochrome DN300 to the moderate level color DN550, to the high performance DN660. The 32-bit processor in this last unit includes hardware floating point rated at almost one million instructions per second.

For special applications requiring dynamic vector displays, Evans & Sutherland PS 330 three-dimensional workstations can be used in the system. Each of these workstations offers either monochrome or color representations; and an Apollo controller/processor supports both.

Digital Equipment Corp of Marlboro, Mass also recently introduced an entry into the CIM arena. DEC's Baseway software, according to Peter Smith, vice president of the company's CAD/CAM group, is "the

manufacturing industry's first software product from a major supplier designed to integrate industrial controllers with manufacturing operations." Smith claims that Baseway "serves as the core of a computerized manufacturing environment and as a framework or base for automated factory growth." He considers this product to be "part of a logical progress to CIM."

In that sense, although it does not now support General Motors' manufacturing automation protocol (better known as MAP), Baseway will support it in the future. This is not surprising since DEC is part of the basic MAP network, along with Gould/Modicon, Allen-Bradley, Concord Data Systems, Hewlett-Packard, Motorola, and IBM.

Hardware requirements for Baseway include a VAX/VMS computer, shop floor gateway, DECnet link support, and a DZ-11 interface. A

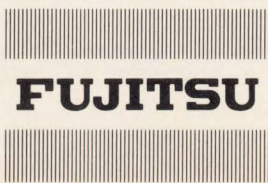
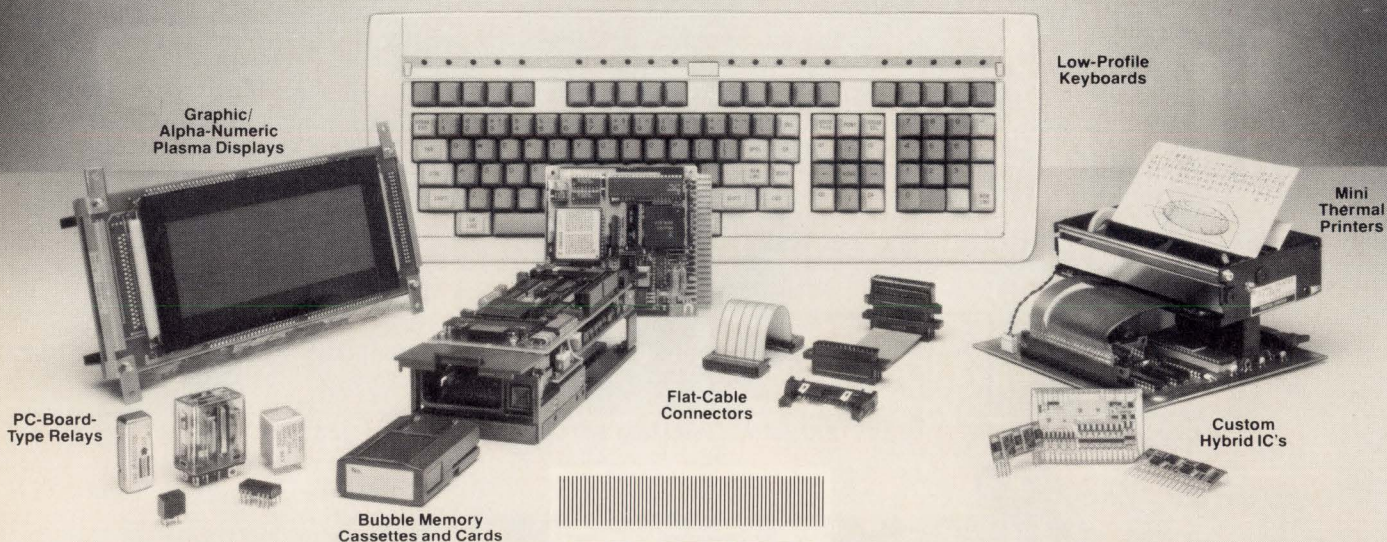
minimum computer would be a VAX-11/750 with 2 to 4 Mbytes of memory. The shop floor gateway would consist of a PDP-11 processor and a minimum of 512 Mbytes of memory. Proposed systems are based on use of either Gould/Modicon or Allen-Bradley programmable controllers.

## CAD/CAM: a key element in CIM

Far more evident today than CIM systems are CAD/CAM subsystems. Most can be considered truly stand-alone systems. Yet they still function as subsystems within the overall CIM picture.

Important moves are underway in this area also, according to H. F. (Bud) Enright, Jr, president of Prime Computer's CAD/CAM business group in Framingham, Mass. Enright emphasizes that "CAD/CAM in the 80s, is what office automation was in the 70s, and banking/retailing was in the 60s. Potential early users have

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unique requirements and specialized companies go after those users. But then as the applications become more generic and more accepted, system suppliers can offer better and broader solutions." The specific application suppliers fall out.

Enright sees the same thing happening in CAD/CAM. For at least the past year, some system integrators have been taking strategy steps so they will appear to be system suppliers first, and integrators second. He says that customers want more than just engineering solutions: they want development tools, communications, and other applications capabilities that are not specifically CAD/CAM. The "system supplier" will provide all of these and make certain that they work together.

A major reason for this shift to the system approach is the lowered component cost. As computer technology becomes more affordable, the system

market develops to encompass multiple application environments. All major computer manufacturers in the CAD/CAM arena recognize this and plan accordingly.

Participation in future CIM applications will be easier for large companies, according to Enright. "Investment costs will be high and only those larger companies will have the necessary resources. CAD was first developed at General Motors in the 1960s, for example, because GM was one of the few companies that could afford the cost. Now, although the costs of computer systems and of graphics have gone down, sophistication of applications has continued to be very high."

Enright believes that widespread acceptance of true CIM is at least five years away. In fact, he says, the industry would do well to reach even that target. Industry reports that he uses for his planning indicate that the CAD

area itself is only 25 percent penetrated right now. Therefore, he feels, a lot of room still exists for advancement before CIM becomes a reality.

Whether or not small industries can afford the expense, CIM will come into being. Perhaps it will be in the form of "mere" factory automation for the immediate future. But certainly CIM will exist by early in the 21st century.

—Sydney F. Shapiro,  
Managing Editor

**SYSTEM TECHNOLOGY**  
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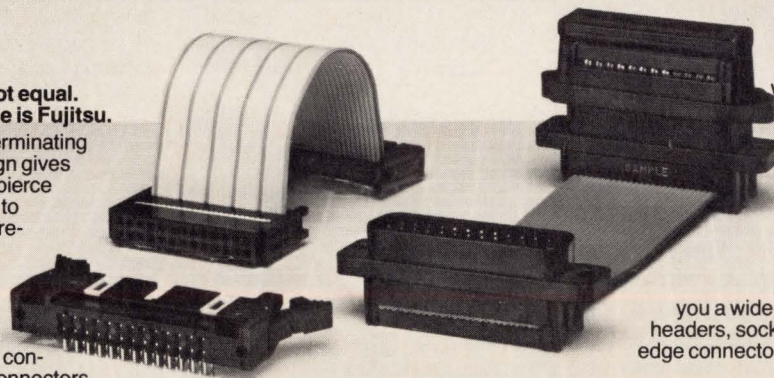
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## Thin-film hybrid tops single wafer package

Rekindled interest in wafer scale integration has made this technology a contender for high performance IC development. While wafer scale integration is particularly attractive for implementing large, high performance digital systems, some recent research indicates that alternative packaging techniques may offer similar benefits without the attendant risks.

Citing results from a study performed at General Electric's Corp Research and Development Lab in Schenectady, NY, C.A. Neugebauer (manager of the semiconductor packaging program) asserts that conventional thin-film interconnections hold a particular advantage over the wafer scale approach. This is the case despite the overall advantages of wafer scale integration, he says. The study compared wafer scale integration to other VLSI packaging methods on the basis of performance, size or weight, and cost.

### Advantages of wafer scale integration

In wafer scale integration, large amounts of microcircuitry are fabricated on a wafer that is mounted, intact, in a single package. This allows for system designs that are larger and have higher speeds than those implemented with conventional VLSI. In addition, much of the capacitance associated with packages, board layouts, and backplanes of conventional designs is eliminated, leading to higher performance.

Higher performance results from the relative absence of line delays associated with ordinary printed wiring boards or conventional hybrid packaging approaches. These delays derive from bonding pads, wires, and package conductor rims, and from conductor rims between packages. Similarly, the much lower output capacitances reduce power dissipation. There capacitances also require smaller output buffers.

These factors make wafer scale integration suitable where computational complexity requires more than 100,000 gates that have custom archi-

Assumptions for VLSI Packaging Comparisons	
VLSI chip (or circuit) size	0.3 × 0.3 in.
Number of output buffers	30 per chip
Number of input buffers	60 per chip
Capacitance of output driver gate, $C_g$	3.0 pF for $R_o \leq 50 \Omega$ 1.0 pF for $R_o = 150 \Omega$ 0.3 pF for $R_o = 450 \Omega$
Input capacitance	1 pF
Output buffer delay, O.B.	3 $\mu$ s for $R_o \leq 50 \Omega$ 2 $\mu$ s for $R_o = 150 \Omega$ 1 $\mu$ s for $R_o = 450 \Omega$
VLSI chip pin count	132
Voltage swing, volts	5 V
Internal chip power (exclusive of buffers)	0.5 W

ecture and very high speeds. For the most part, wafer scale integration is applied in specific vertical applications and in areas where such repeated circuit patterns as memory cells lend themselves to easy redundant replication. Thus, it offers a cost-effective, all-encompassing package.

To determine how alternative packaging approaches compare with wafer scale integration, Neugebauer used a relatively simple case of iden-

tical 64-kbit memory circuits diffused in a silicon wafer, in which he assumed certain contents and densities. Package delay, power requirements at 100 MHz, and size or weight were estimated. Figures of merit were calculated for devices based on printed wiring board that uses discrete packages, thick-film multilayer hybrid ceramic, ceramic multilayer hybrid, thin-film multilayer hybrid with chips  
*(continued on page 62)*

Comparison of Package Figures of Merit				
Packaging approach	Power delay (normalized)	Size or weight (normalized)	Cost (normalized)	Overall figure of merit
Printed wiring board	1.00	1.00	1.00	1.00
Thick-film multilayer on ceramic	1.08	0.42	1.02	0.46
Ceramic multilayer hybrid	0.34	0.20	0.65	0.044
Thin-film multilayer hybrid on various substrates, populated on one side	0.19	0.14	0.60	0.016
Wafer scale integration	0.10	0.09	0.46	0.0041
Thin-film multilayer hybrid on various substrates, populated on both sides	0.08	0.07	0.44	0.0025



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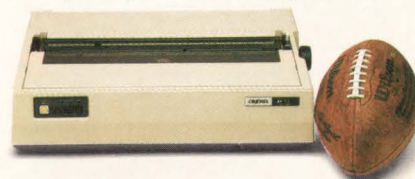
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## Thin-film hybrid

(continued from page 60)

### Restructured VLSI to form wafer scale integration

One wafer scale integration technique that may ensure a higher yield of "good" working circuits is an approach called restructured VLSI. Using this approach, the wafer is partitioned into an array of cells. The smallest replaceable unit, partitioned into each cell, is surrounded by a matrix of interconnect wiring. This wiring matrix comprises a number of wafer length tracks that occupy channels between cells on both first- and second-level metal layers.

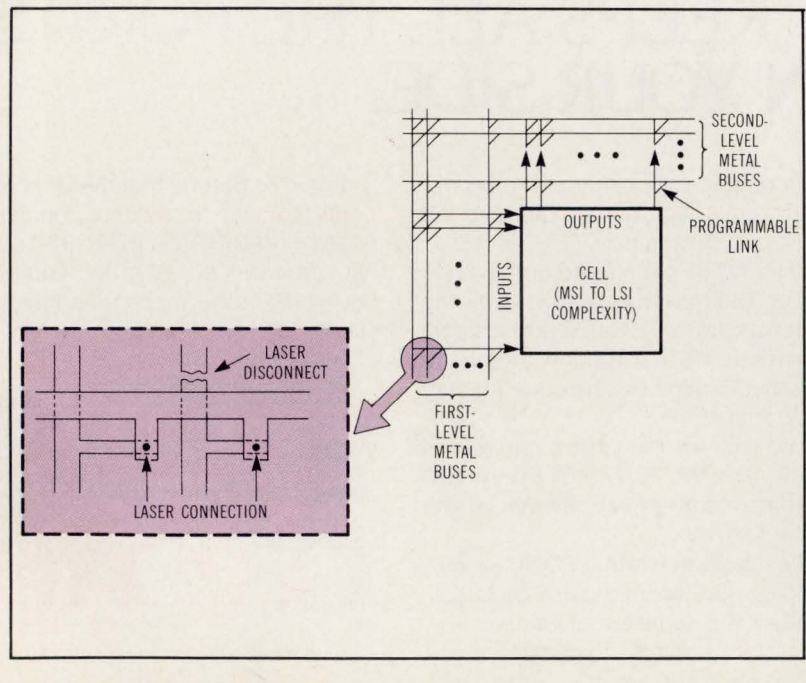
Using a low power constant wave argon laser, wire lines can be linked by forming a vertical weld between two normally insulated metal layers. The laser also cuts the lines when required. Cell inputs and outputs are provided with pads, allowing the cells to be tested at the wafer probe level as though the wafer were to be separated into individual dies.

With the VLSI approach, researchers at the Massachusetts Institute of Technology's Lincoln Labs in Lexington, Mass have fabricated a digital integrator that has 256, 10-bit counters for performing signal averaging. Specifically designed for use in a pocket radio system, developers say the device is also applicable in systems requiring noise reduction through digital integration.

The system is partitioned into 64 cells, each containing four counters. Eight 25-MHz counter enable signals are derived from a single 200-MHz bit stream by an offchip serial-to-parallel converter. A conservative 5- $\mu$ m CMOS process was used to fabricate active devices and a 3:1 redundancy was provided to minimize processing problems. That researchers could test the wafer in increments as the cells were connected played a crucial role in the results summarized in the accompanying table.

As the researchers expected, the track yield on the 20-cm<sup>2</sup> chip is in the range of 95 percent, and input and output amplifiers are almost perfect. Eighty-one cells were operational on this wafer, giving a 42 percent yield. Only 33.3 percent was required. The operational wafer was packaged in a 180-pin hybrid package.

Currently in fabrication at Lincoln Labs is a monolithic 16-point fast Fourier transform, and a system performing dynamic time warping for speech recognition. Both wafers contain 300,000 transistors. Future projects call for larger wafers to house circuits of a 10<sup>7</sup>-gate complexity.



on one side, and the same hybrid with chips on both sides.

The three most important parameters to minimize for any given packaging approach are the performance (power x delay), size or weight, and cost, according to Neugebauer. When normalized values are compared (using one for the printed wiring board), the power x delay product of various approaches ranges over a set of values that differ by a factor of 12. In size or weight, the values span a factor of 14, and the costs differ by a factor of 2. Overall, parameters for the various approaches differ by a factor of almost 400 when the figures of merit are multiplied.

Using this data, Neugebauer bases his claim that considerable room is left for improvement in conventional packaging techniques. "By applying an advanced packaging approach, conventional densities, performance, and costs compare favorably with those achievable using wafer scale integration," he says.

Three principal factors cause thin-film interconnect techniques to achieve particularly favorable figures of merit, according to Neugebauer. First, thin-film interconnections can have a width comparable to that used on the chip itself, producing the highest density and minimum capacitance. Second, the number of interconnection layers between VLSI chips can be as low as two due to the very high line density thin-film technology can achieve. And last, many of the materials and processes developed for IC fabrication are useful here in thin-film interconnections, including implementation of such technologies as aluminum/polyimide multilayering and use of silicon as a substrate.

Beyond this, conventional techniques have a big advantage over wafer scale integration because risk is much less, Neugebauer claims. In essence, this risk is limited to such packaging issues as chip testing, replacement, and substrate rewiring.

—Nicolas Mokhoff, Senior Editor

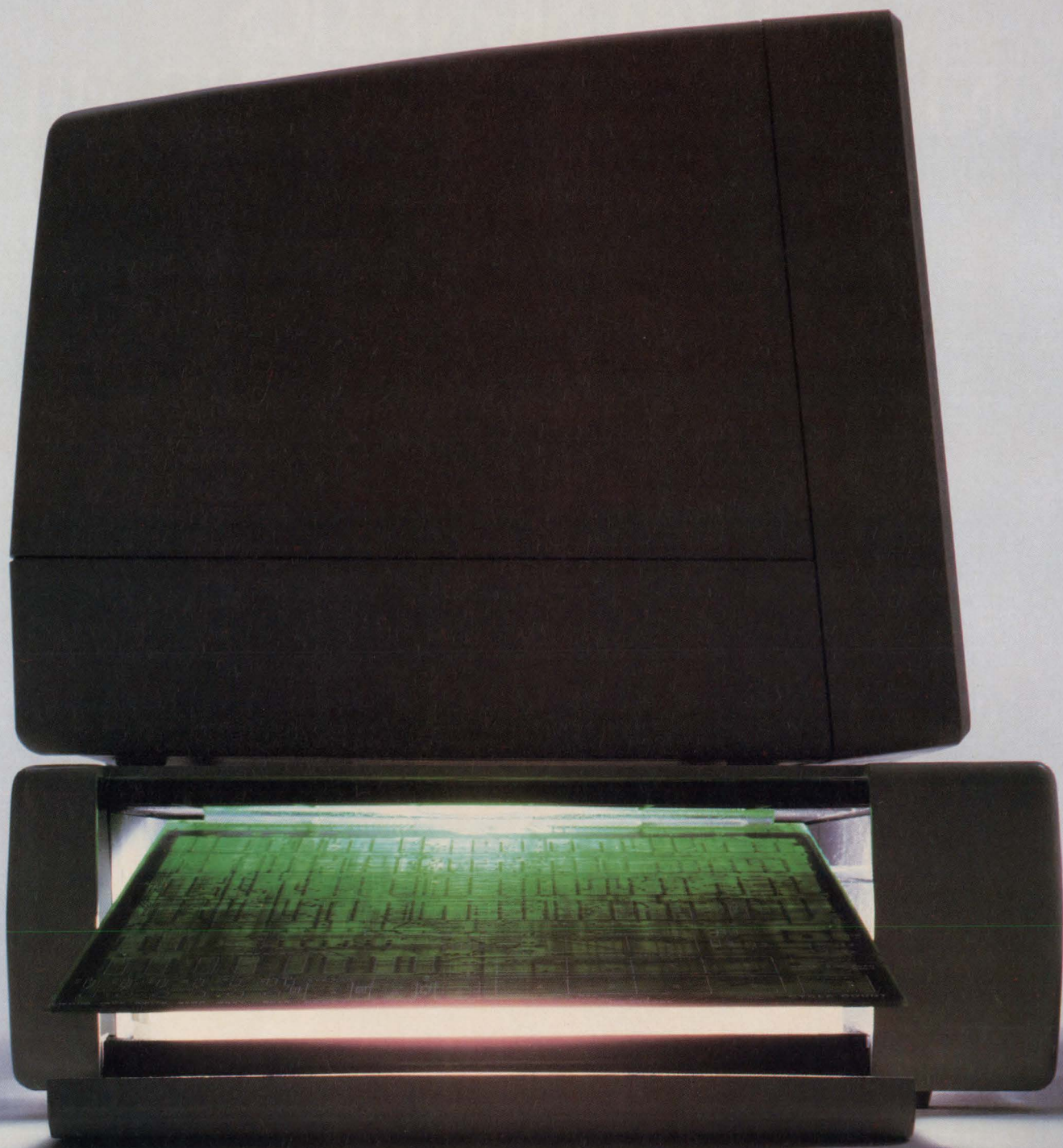
SYSTEM TECHNOLOGY  
(continued on page 70)



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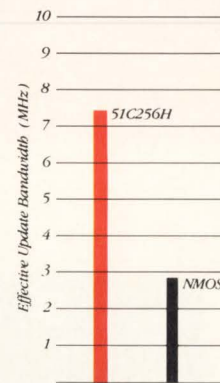
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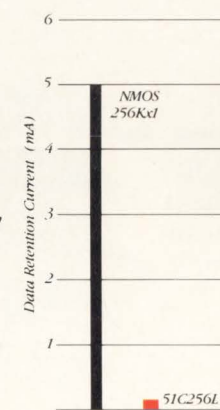
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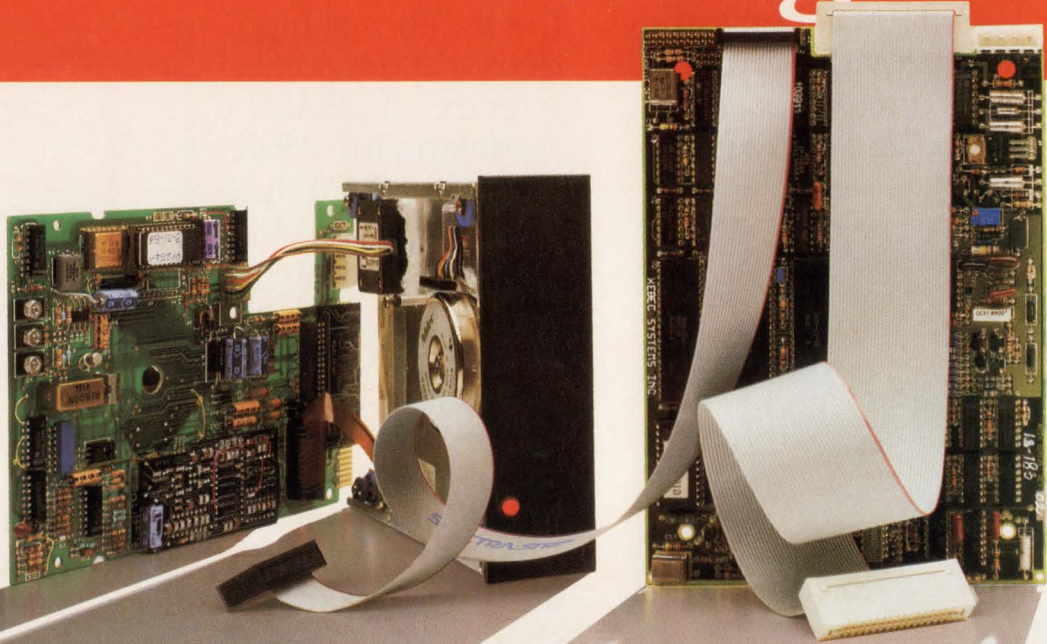


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On the surface, the Owl might look like other 10-megabyte, 5¼" half-high Winchester. Underneath, however, it's an example of superior technology. The integration of controller logic and drive electronics on a single board means not just one less PCB, but the elimination of expensive connectors and cabling, low power consumption (15 watts typical) and enhanced data integrity.

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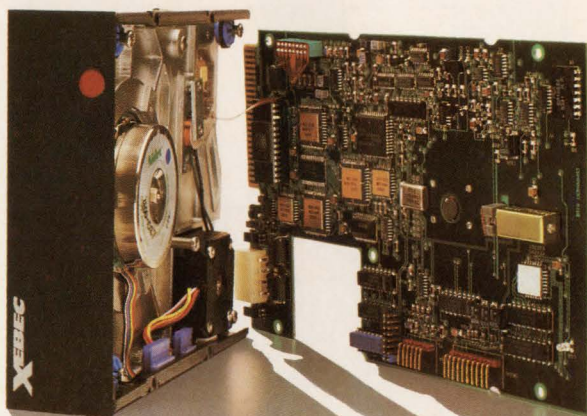
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## Chip solves PC to AT conversion problem

In a move to counter the introduction of the IBM PC AT, manufacturers are racing to develop 80286 upgrades to the PC and compatibles. However, these manufacturers face a tough hardware compatibility problem. While the 80286 runs programs two to four times faster than the 8088, it cannot use existing 8-bit peripherals.

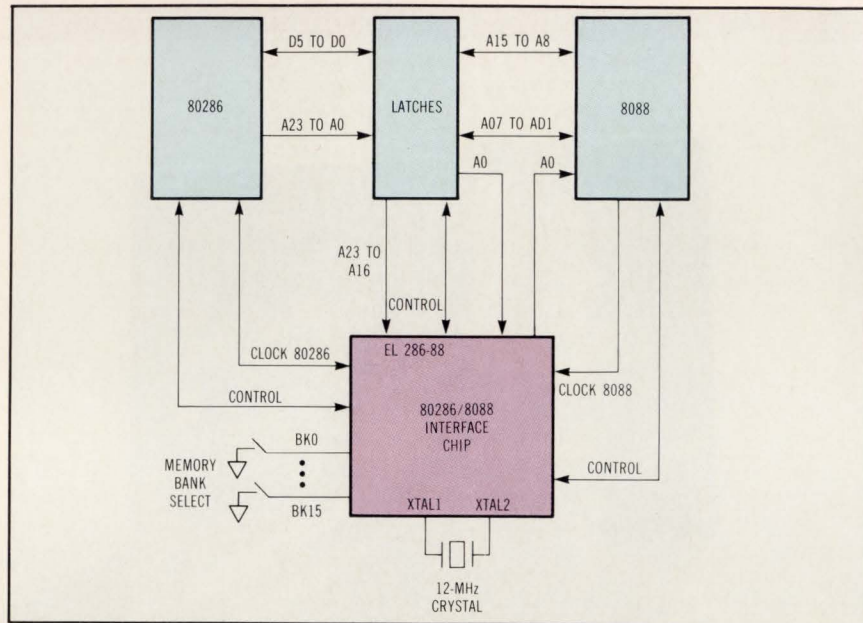
IBM solved the problem with a converter that changes the 16-bit transfers of the 80286 into 8-bit transfers. This conversion, however, is not so simple for manufacturers of compatible computers and expansion boards. It requires a lengthy design cycle and results in circuitry having as many as 50 TTL parts.

A chip developed by Edsun Labs, Inc (Wayland, Mass) solves the conversion problem. The EL 286-88 processor converter is a CMOS gate array available in the same package as the 80286, a leadless 68-pin chip carrier. By translating bus width, control signals, and timing from the 80286 to the 8088, this chip solves a major design problem for developers of PC AT compatible computers.

To the 80286, the converter appears as a 16-bit memory or peripheral operating at the 80286 clock rate. To an 8-bit device or memory, the converter looks like an 8088 running at a different clock rate.

The EL 286-88 allows the two processor clocks to be asynchronous. For example, the 80286 could run at a full 8 MHz, which is faster than the PC AT, while addressing peripherals designed for the 4.77-MHz IBM PC. Control inputs on the device select those memory addresses and I/O devices to be serviced through the converter or by the 80286.

The chip is particularly useful for expansion boards that upgrade the PC to a PC AT configuration because it saves so much board space. The 80286 expansion board can be plugged into the 8088 socket (via a ribbon cable) and translation will be completely transparent to the software. However, this approach may require moving the original 8088 to



**The processor converter chip solves the incompatibility problem between the 80286 and 8088 processors for developers of PC AT compatibles.**

the expansion board to prevent problems with timing-sensitive programs. The EL 286-88 has control circuits that allow hardware or software switch selection of either processor.

Edsun Labs is a development organization only. Manufacturing of the EL 286-88 will be accomplished by Universal Semiconductor (San Jose, Calif) and Siliconix (Santa Clara, Calif).

### Making chips in suburbia

Since 1980, Edsun Labs has been designing and marketing advanced digital circuits in the United States and Japan. The company typifies a new kind of entrepreneurial engineering organization, although it has origins in home-based consulting and independent software design. Edsun Labs does engineering and marketing by using a network of independent entrepreneurs.

The trend for IC designers to work without traditional large company support results from development of silicon foundries, silicon compilers, and regional design centers. These centers allow the self-employed

designer to get the support needed to translate system ideas to the chip level.

Steve Edelson, the owner of Edsun Labs, represents the new breed of designers. He is not an IC designer at all but a designer of hardware and software systems that he has implemented at the chip level.

Another independent designer, Thomas Durgavich, of Duralogic in San Jose, Calif collaborated in the design of the EL 286-88 and functions as a second source. Edelson's company stays small and solvent by striking deals with other independent technologists who might also work in their homes. For example, besides Durgavich, two independent programmers work for Edsun Labs.

According to Edelson, small companies like his survive and prosper because of their flexibility. "It is essentially a hit-and-run business," he says. "If the demand becomes large enough, a major company will produce a standard market niche." But this is not true for many of his customers. They must run to stay ahead of I.M.," he adds.

—John Bond, Senior Editor



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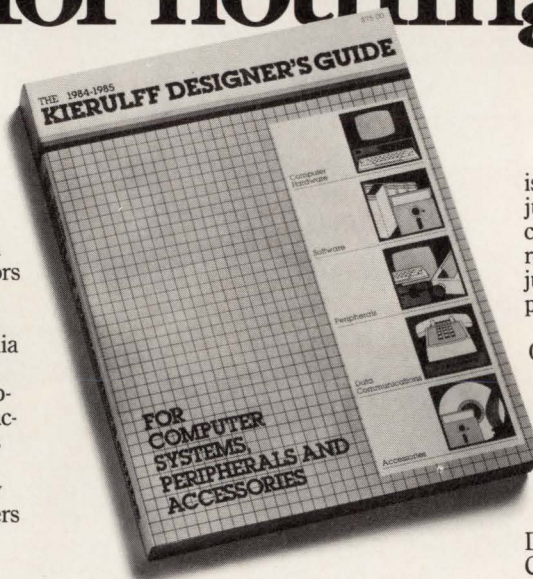
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While not limited to M68000-based systems, the VMEbus and I/O Channel are ideal complements for any application employing the high performance MC68000 MPU. A complete line of M68000 family-based VMEmodules is already available and an aggressive program for rapid expansion is in place with a full 32-bit MC68020 processor board soon to be available.

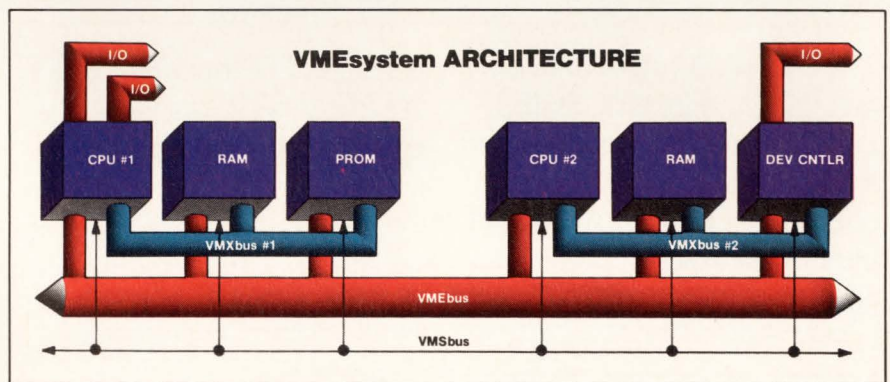
VMEmodules are high performance building blocks, ideal for expanding and customizing Motorola's VME/10 OEM Micro-computer System.

Add system software, such as our VERSAdos™ Operating System, and you have a totally compatible environment for controlling multiple tasks in real time with minimal design and programming.

## VMEbus: graceful growth and Motorola expertise.

VMEbus clearly offers a graceful growth path to 32-bit systems while it can be used just as readily on today's 8- and 16-bit systems. Add Motorola's expertise, proven products, training and service support, and you can have the right choice today and for your future in VMEmodules.

Write Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036.



# MOTOROLA

TO: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036

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Title \_\_\_\_\_

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# FIND THE TAPE MAKE A CON



If you need tape controllers and couplers for VAX, Unibus and QBus systems, you've come to the right ad. Emulex offers one of the industry's most complete selections.

#### **FOR VAX SYSTEMS.**

Our new TC7000 is a good example of the kind of performance you get with Emulex. This single-board controller lets you move up to the higher densities and transfer rates of state-of-the-art GCR transports. One TC7000 can handle up to four STC-type transports or eight reel-to-reel units with Pertec-type interfaces. And you can choose from three tape

densities: 800-bpi NRZI, 1600-bpi PE or 6250-bpi GCR.

#### **FOR UNIBUS SYSTEMS.**

Our TC11 emulates the basic DEC TM11 controller. It works with up to four industry-standard tape drives with densities to 1600 bpi and speeds up to 125 ips.

Unibus users will also appreciate the TC12. This single-board TS11-compatible coupler handles industry-standard formatted Pertec-type  $\frac{1}{2}$ " tape transport, including conventional NRZI/PE start/stop and 800/1600/3200-bpi streaming tape drives.

The new TC15 is another

TS11-compatible tape coupler that allows you to interface the CDC Sentinel  $\frac{1}{4}$ " streaming tape drive. And it features software transparency and standard operating system support on your Unibus system.

Last, but not least, is the TC13. This universal tape coupler works across the Unibus of PDP-11 and VAX-11 CPUs. It handles industry-standard  $\frac{1}{2}$ " tape transports, including conventional start/stop, streaming, and the new generation of GCR units.

#### **FOR QBUS SYSTEMS.**

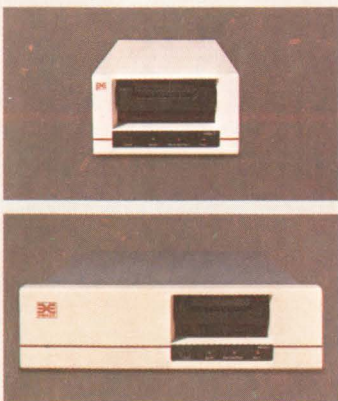
The TC02 has long been an Emulex favorite. This TS11-

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compatible tape coupler works with all 800/1600/3200-bpi formatters at speeds from 12.5 to 125 ips.

Another TS11-compatible coupler is our new TC05. It allows you to interface CDC Sentinel 1/4" streaming tape



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And don't overlook the TC01. TU10/TM11-compatible, it handles as many as four dual-density 800/1600-bpi 1/2" transports at up to 75 ips.

### NEW PACKAGED SUBSYSTEMS.

Also available for QBus and Unibus users are two packaged subsystems.

Vault™ is a 1/4" streaming tape that gives you up to 70 MBytes of storage.

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**The genuine alternative.**

# THE BIRTH OF THE ARRAY PROCESSOR AGE



Until now, array processors have filled an important, but restricted, niche in the computing world. Analogic's AP500 has changed that. Because of its unique combination of flexibility, performance, and reasonable cost, the AP500 opens a vast number of computationally-intensive problems to array-processing power.

## THE ORIGIN OF THE SPECIES

As array processors have evolved, they have proven their worth in specialized, dedicated operations. In fact, Analogic's involvement with these devices started with such an application—a key subsystem in our invention of the first CAT-scan instant-image processor.

Building on this foundation, our engineers then developed the AP400 Array Processor, whose patented architecture set new standards for cost-efficient computing performance. The enthusiastic acceptance of the AP400 has resulted in one of the largest installed bases of any array processor—and continues today.

Now, the AP500 is here. It does not replace the AP400, rather it offers the user a new range of performance options for tackling increasingly complex problems in computer modelling, imaging, and design. With the AP500, state-of-the-art means more than computing speed. In continuing the tradition of cost-effective computing performance and innovative design, our engineers have even given the AP500 standalone capability.

## THE NATURAL SELECTION

The AP500 meets or exceeds the performance characteristics of comparable array processors at 25% to 50% of their cost. It performs a 1024 pt. complex FFT in 4.68 ms, and a 50 X 50 matrix inversion in only 72 ms. Its other performance specs are equally impressive.

With 4 Mbyte of data memory, 384 kbyte of program memory, and high-speed bidirectional I/O capability, the AP500 can form the heart of a high-power computing work station. Its on-board co-processor means that it can even operate independently of a host computer for remote operations or applications which demand complex communication procedures, such as adding data block identifiers or handling packet protocols with incoming data.

We want to tell you more about using the AP500 to solve your problems. Just call Analogic's Computing Systems Group at

1-800-237-1011

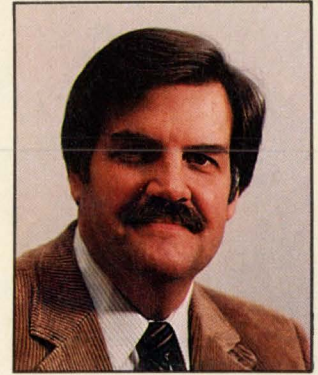
Find out why the AP500 is ...

## THE NATURAL SELECTION

**ANALOGIC** ■  
COMPUTING SYSTEMS PRODUCTS GROUP  
Analogic Corporation, Audubon Rd., Wakefield, MA 01880, (617) 246-0300



# TECHNOLOGY TRENDS '84/'85



This past year in computers, peripherals, ICs, data communications, or whatever aspect of computer systems you may be interested in was just about the same as past years—there was significant activity just about everywhere. In the heady realm of mainframes, IBM broke some price/performance records coming out with a system aimed at the 32-bit scientific market that provides a MIPS for about \$200,000. Moving a step down in size, minicomputers held their own against the onslaught of microcomputers and even took on some mainframe class machines. That's happening because mini designers are using VLSI technology to boost speed and cut costs. Those same advances in VLSI have resulted in the emergence of multiple processor systems and fault-tolerant machines.

Powerful computers demand lots of memory and micro floppy drives reached the storage capacities typical for 8-in. drives only recently. But, perhaps the biggest news in mass storage was that optical storage systems finally became a commercial reality. Exotic technologies are also having an impact in other computer peripheral areas. In printers, for example, several ion deposition units entered competition with laser printers. More ink-jet units appeared as competition for conventional and magnetographic printers. Along with all this printer technology, more companies developed controllers and interfaces that can customize printer systems for specific applications. One benefit of this "modular" approach is that printers can be made to act as high quality test-and-graphics printers.

More powerful minicomputers, smaller microcomputers, and custom printers are only some of the fallout from continuing development in VLSI technology. The first full 32-bit micros were introduced by National Semiconductor, NCR, and Motorola. Further increases in density for dynamic RAMs with 256-Kbit parts, special-purpose memories for high performance video RAMs, EPROMs edging up to half-megabyte levels, and EEPROMs

reaching 64 kbits also made headlines. In addition, this year unquestionably put CMOS in the mainstream of microprocessor, memory, and semicustom IC technologies.

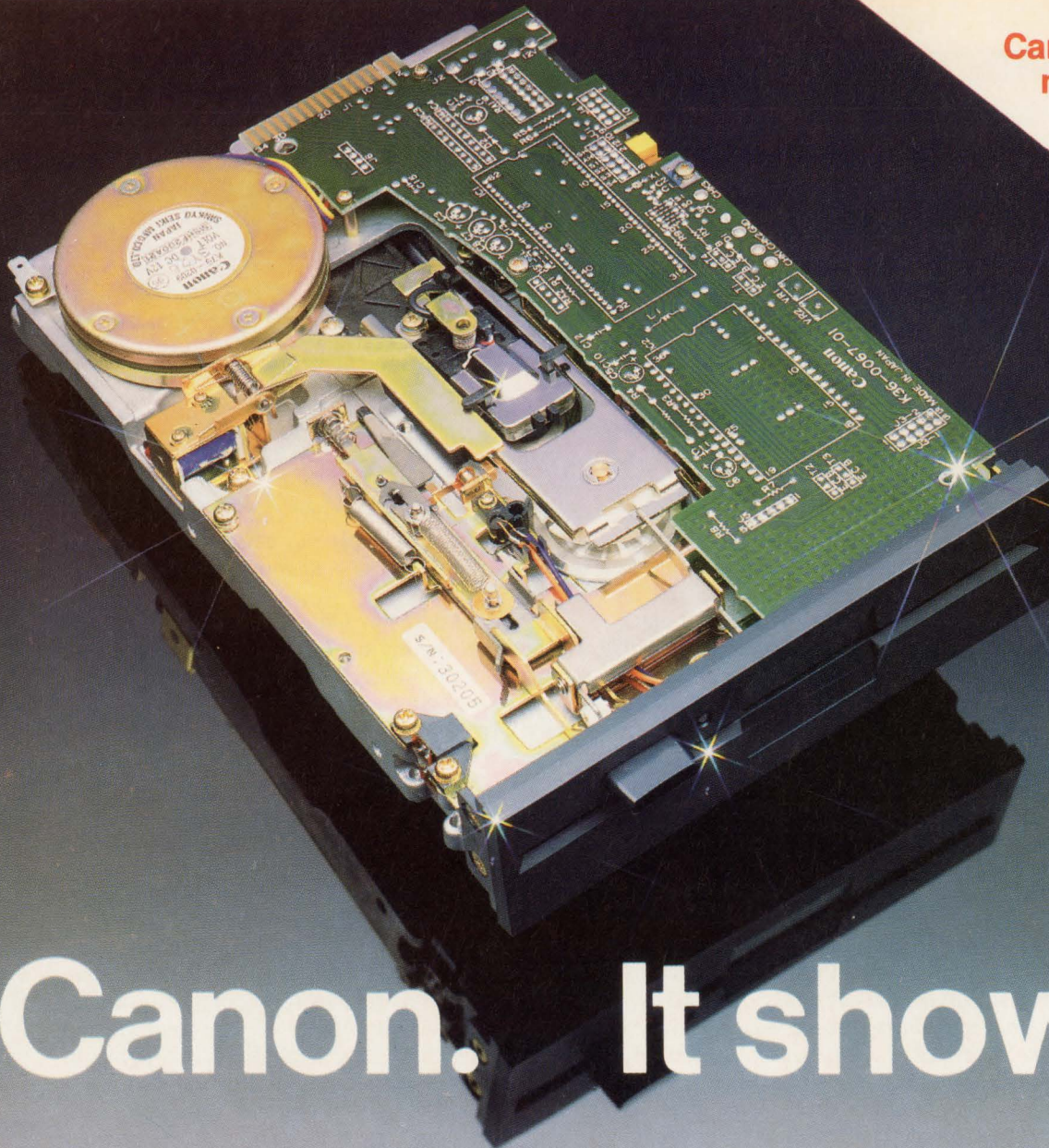
Settling the data link issue for local area networks was perhaps the major development in data communications. It was generally agreed that specific data links are better suited to some applications than others. For example, the Ethernet baseband works best for office environments, and token passing is best for factory environments. Part of the settling down is clearly attributed to the corporate giants, IBM and AT&T, backing LAN schemes. Though the data link level issues are being resolved, much remains to be done at the higher levels of the ISO model. In short, a "protocol wars" seems to be brewing.

In addition to the stability developing in data communication standards, other software standards are sorting themselves out. In the computer graphics industry some rough outlines of the standards and their functions have been established although considerable differences of opinion still exist. NAPLPS and IGES are the official national standards, with others, including GKS and VDM, under development. In the area of operating systems, AT&T launched a major campaign to establish Unix System V as a *de facto* standard and the IEEE has written a standard operating interface that allows application programs to communicate with diverse operating systems. But, with the minimal rules established by the standard and the number of operating systems in place, how effective this standard will be is anybody's guess.

A handwritten signature in cursive script that reads "John Miklosz".

John Miklosz  
Executive Editor

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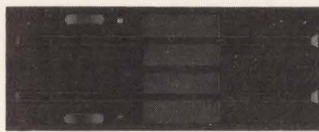
Our drives are available with the bezels shown — or with no bezel at all, so that you can determine your own packaging design.



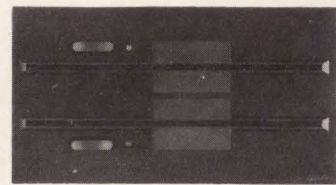
33.5 mm bezel



Standard half-height bezel



Dual drive:  
Standard 2/3 height (57.5 mm) bezel



Dual drive:  
Standard full height bezel

**Canon**

CIRCLE 39

\* Recognized under the Component Program of Underwriters Laboratories Inc.

# MULTIPLE CPUs AND MORE MEMORY DEFINE NEXT GENERATION

**With more than one processor, systems can make substantial gains in computational power. But the extra power and the extra data handled call for higher capacity mass storage.**

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by **Peg Killmon,**  
Senior Editor

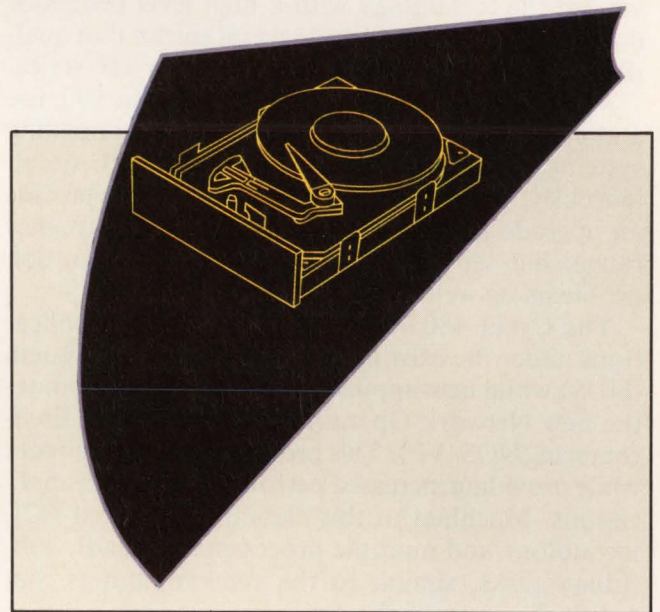
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Multiple processor systems are leading the way to the next generation of computers. In fault-tolerant systems, multiple processors ensure that valuable data will not be compromised when a system component fails. In general-purpose machines, such processors provide the raw power to plow through problem after problem.

The computational power of these machines creates volumes of data. To keep up with expanding needs, storage systems use optical recording techniques. Mass storage systems that are based on these principles fit into the memory hierarchy between tapes and disks.

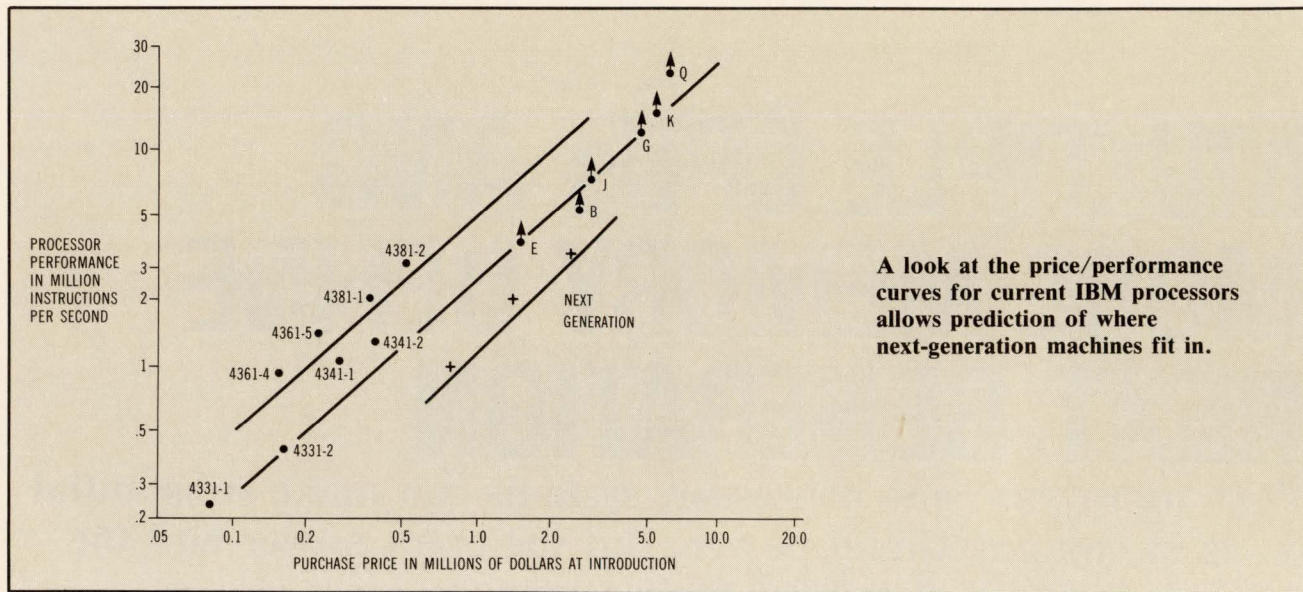
Supercomputers head the pack as the fastest and biggest computers. These behemoths attack complex scientific problems involving enormous arrays of data and incredibly complex calculations. Found mostly at government installations or laboratories doing government work—few others can foot the bill—their failings are well known. Such demands have spawned cooperative efforts to develop fifth-generation computers. As these efforts stimulate interest in artificial intelligence and knowledge-based systems, they pave the way to the future.

At the supercomputer level, the Japanese are mounting a severe challenge to U.S. domination. Both Hitachi and Fujitsu have already invaded the U.S. market, under the aegis of Amdahl (Sunnyvale,



Calif) and National Advanced Systems (Mountain View, Calif), respectively. Cray Research (Mendota Heights, Minn), trying to protect its leading position in the field, hopes to fend off the invasion with its Cray-2, a super-class machine still under development. In the interim, design changes to its X-MP now include dual-processor CPUs with 2 or 4 million words of main memory that are half as big and half as power hungry as their predecessors. A four-processor system that offers performance rated at 10 times that of the Cray-1, the X-MP/48 handles 8 million words of main memory.

Control Data Corp (Minneapolis, Minn), ceding supercomputer development efforts to a subsidiary, has formed ETA Systems (St Paul, Minn) to exert a concerted effort on its high end Cyber series



machines. Recent Cyber series machines have advanced the technology with a high level processor on the mainframe level and several entries that qualify as superminicomputers in the Cyber 180 series.

Machines in this series, headed up by the 990, use a multistate architecture. By allowing two operating systems to run in the same memory and CPU simultaneously, Cyber 180 series machines not only provide an upgrade path over a 1 to 60 times performance range, but seemingly conquer software migration problems as well.

The Cyber 180 system can run existing applications under the existing Network Operating System (NOS) while new applications are developed under the new Network Operating System/Virtual Environment (NOS/VE). This provides a migration path, while providing increased performance for old applications. Machines of this class use advanced ECL technology and multiple processors to handle subsidiary tasks, similar to the supercomputers that typify the state of the art.

### Breaking price/performance barriers

Announced in late 1983, two processors in IBM's 4300 series are exerting a tremendous influence on computers of all kinds. This impact is one of performance and price. The 4381 takes on mainframe manufacturers with its 2- to 3-million instructions per second (MIPS) performance levels. This machine has up to 4 MIPS expected in scientific applications and is priced in the \$500,000 to \$600,000 range. The 4361 is targeted directly at those dominating the 32-bit scientific market, and runs under MVS to provide performance levels close to 1 MIPS. It prices out at between \$150,000 and \$275,000.

With a price/performance ratio at about \$200,000/MIPS for these machines, IBM has broken new bar-

riers. The significance of this price/performance ratio can be appreciated by comparing it to the 4300 series machines introduced at \$400,000/MIPS. In addition, IBM's next series may well be introduced at a \$100,000/MIPS price/performance level.

While last year's prognosticators would have buried the minicomputers, these machines have instead shown remarkable resilience and tenacity, holding their own against the onslaught on microcomputers. Recent entries in this performance and cost class are not only holding the line, but offer serious competition for some mainframe class machines. What has occurred, and what will occur, on the minicomputer level in essence takes two different directions.

To build speed and cut costs, minicomputer designers are turning to increased use of VLSI. New machines display a greater number of functions built into gate arrays. With more functions supplied by each board, higher reliability is attained, and costs are kept down.

High level integration techniques have provided us with high level machines such as Harris Corp's (Melbourne, Fla) H1000 as well as Data General's (Westboro, Mass) MV/10000. On the other end of the performance spectrum, integration has been used to cut the costs in machines such as Data General's MV/4000 and Harris Corp's H60.

A totally different direction may be forming with research reportedly underway on Reduced Instruction Set Computer (RISC) machines. Brought to public attention in Pyramid Technology's (Mountain View, Calif) 90X, this concept may lead to high performance systems at dramatically decreased costs. Two projects rumored to be underway at DEC—code named Titan and Nautilus—would put high end computer performance on a single chip using RISC

technology. Other entrants in the field that serve as pointers to the future are machines designed specifically to run artificial intelligence languages.

Latest in this area is a desktop system from Texas Instruments (Austin, Tex) called Explorer. The 32-bit processor used to handle symbolic structures in this machine is designed with 16-K, 56-bit words of writable control store, microprogrammed for Lisp processing. The 32-bit NuBus with 37.5-Mbyte/s bandwidth and a 32-bit local bus provide rapid exchange of information among processors and memory.

LISP Machines, Inc's (Culver City, Calif) Lambda systems can be configured with up to four coprocessors (two Lisp and one 68010/Unix or four Lisp) on a multiprocessor bus. With the Unix processor, intelligence can be added to a Unix package placed under supervision of a Lisp program, or data acquisition and numeric processing can be handled.

Symbolics, Inc (Cambridge, Mass) in its second-generation Symbolic 3670 and 3640 workstations has cut the cost of symbolic processing. The 3670 incorporates a tagged memory architecture and a stacked-oriented architecture with demand-paged virtual memory in a fully expandable symbolic processing system. The 3640, a dedicated single-user workstation, uses the same processor as the 3670 but supplies less disk and main memory capability. In a standard configuration with a 2-Mbyte RAM and 140-Mbyte disk, the 3640 is priced at \$69,000.

### Multiprocessor micros take on minicomputers

With the power of current 16-bit microprocessors, multiple processor machines are making a dent in the traditional minicomputer niche. With the 32-bit microprocessors finally becoming available, multiple processor machines will cut an even wider swath.

Among the multiple microcomputer systems new to the market, Logical MicroComputer Co's (Chicago, Ill) MegaMicros offer a challenge to traditional superminicomputers. These systems are based on National Semiconductor's (Santa Clara, Calif) NS16032 microprocessor and use demand-paged virtual memory in hardware. They can also use hardware to perform 64-bit double precision floating point arithmetic.

Another new arrival in the multiple microprocessor arena is the model 1124 from Areté Systems Corp (San Jose, Calif). Based on dual 68000 processors tightly coupled by a proprietary multithread architecture, Areté Systems claims performance levels 30 percent higher than the VAX-11/780. Four separate buses within the system optimize memory access, interprocessor communications, and data transfers. Up to four 12.5-MHz 68000 processors, each with a 4-Kbyte cache and a memory manage-

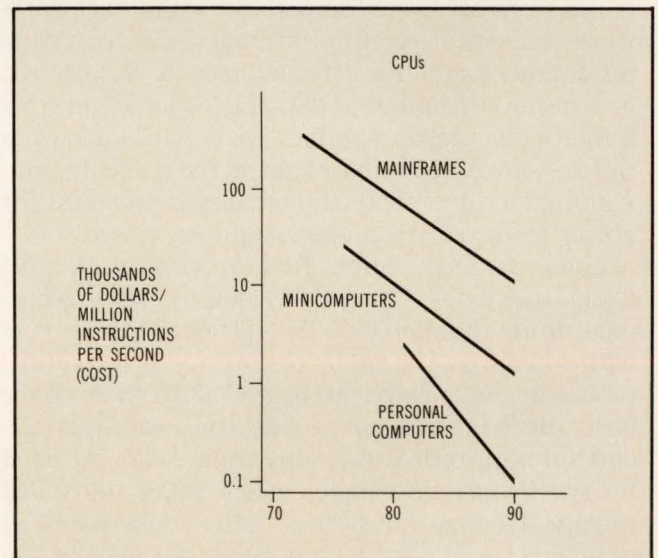
ment unit provide the processing power. As many as 12 processors act as I/O control processors, providing the potential to process data at rates up to 2.8 MIPS.

Joining the ranks of low cost but powerful processors, the Balance 8000 from Sequent Computer Systems, (Portland, Ore) puts from 2 to 12 microprocessors to work to deliver a performance of up to 5 MIPS. Based on NCR's (Dayton, Ohio) 32-bit NS32032 microprocessor, the system dynamically balances the load, and assigns tasks to run on any idle processor. Although all processors access a single global memory, each processor has its own cache to minimize bus traffic. A global synchronous bus interconnects all processors to all resources.

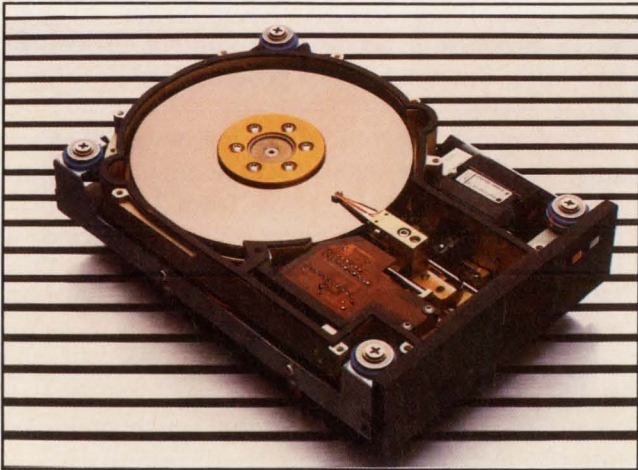
The power evidenced by microprocessors has taken yet another route—that of fault-tolerant machines. Here, the microprocessor has made these systems available to a much wider variety of applications simply by providing a source of processing power at a price low enough to allow duplication.

Dominated by mainframes, with superminicomputers holding about 9 percent of the fault-tolerant market, potential buyers respond to the lower prices of micro-based machines. But these machines must also provide high performance and high capacity, as well as expandability. Systems filling these needs rely on redundant architectures—and are costly. An added detriment is the high overhead incurred because of the software required and the limitation that this places on performance.

Enmasse Computer Corp (Acton, Mass) plans to counteract these penalties with a 32-bit micro-based design currently under development. This system, targeted for introduction in the first quarter of 1985,



Plotting the course of price reductions on mainframes, minicomputers, and microcomputers shows rapidly declining costs during the 1980s.



The half-height 5¼-in. Winchester disk drive model HH-725 from Microscience International stores 20 Mbytes on plated media.

is planned to price out at under \$50,000 in basic configurations. Basic to the system is the Link architecture. This architecture forms a high speed network of file processors and application processors. The original hardware can be expanded to support 32 to 768 user terminals without degraded processing speed.

Sequoia Systems, Inc. (Marlboro, Mass) uses a combination of architectural and operating system features in its machines to supply a high level of fault tolerance with a processing capability that ranges from 2.5 to over 50 MIPS. The tightly coupled architecture interconnects up to 64 processor elements and up to 128 memory and I/O elements through dual 80-Mbyte/s system buses. These self-checking elements can be added or taken out of service without interrupting operations.

Continuous operation and data integrity are attained from hardware comparators within each hardware element. Detecting internal faults or errors instantaneously, the affected task is suspended, preventing corruption of data. Detection of an error initiates diagnostic routines that determine what failed, and isolate that element from the system. Automated load balancing eliminates the need for a user to distribute processes among processors.

Going beyond simple fault tolerance, Parallel Computers (Santa Cruz, Calif) aims at fault management in its Parallel 300. The difference is the ease with which repairs can be made. A pair of parallel processing units based on the MC68010 serves as the basis for the redundant architecture. All tasks execute on both processors. Any failures are detected by synchronization logic, which takes the failed processor out of the system. After replacement of the failed component is completed, synchronization is regained automatically.

August Systems, Inc. (Tigard, Ore) has cut the number of internal components in its CS330 to

reduce costs and improve performance. Aimed at industrial process control, the fault-tolerant machine uses something called triple modular redundancy to achieve reliability. This technique employs three identical computers to perform all functions simultaneously. Inputs, computations, and outputs are automatically read, validated, and voted on by the three processors. If one fails, the two remaining provide continuous correct operation.

Each control computer board includes an 8086-2 microprocessor, and 8087-2 coprocessor with up to 1 Mbyte of RAM. Incoming signals are triplicated and sent to each of the three computer boards through a separate bus. Each computer processes the signal, then reads and compares the data obtained with that of the other two. If one disagrees, the other two remove its output from the system.

The power of microprocessors has also brought about the possibility of a complete system at the board level. A prime example is Intel's (Santa Clara, Calif) iSBC 186/03 series that puts processor, memory, memory management, terminal controllers, and storage peripheral controllers on the same board. Based on the 16-bit 80186, the board replaces several conventional boards while offering faster processing speeds, lower costs, and reduced power requirements. By incorporating the 80130 operating system firmware, the board provides the power of a real-time executive as well as timers and programmable interrupt control.

### Matching data storage needs

Storage devices became the center of attention a few years ago as they started to decline in size. They are now part of the proliferating microcomputer systems sitting on individual desks. Over the past several years, every known storage peripheral has gone through the same downscaling process. All of this has occurred while keeping capacities in the same general range. Now a 3½-in. floppy disk drive stores as much data as the 8-in. floppy that was widely used not too long ago. These units are matched by scaled down Winchesters in the 3½-in. form factor that packs in up to 25 Mbytes of data. These sizes are matched by oncoming tape drives that will take care of the archival or backup functions in the 40-Mbyte range. The growing number of arrivals in the tape drive area has been propelled by the growing awareness that a single, totally enclosed disk does not supply adequate protection from data loss.

Meanwhile, optical techniques have finally reached the commercial stage. Optical storage media have long been heralded as a replacement for magnetic tape in archival storage. They will probably find a niche in the storage hierarchy alongside both magnetic tape and magnetic disk devices instead.

**BY THE TIME THE INDUSTRY  
MATCHES THE PERFORMANCE  
OF OUR 330MB 8" DRIVE, WE'LL  
BE DELIVERING A 660MB.**



**THE NEW MV330 MV660 WINCHESTER.**

No other 8-inch winchester combines this much performance with 330 megabytes of capacity.

We've shaved every superfluous gram from the head assembly, and we've used powerful rare-earth magnets in the actuator.

The result is an average access time under 18 milliseconds.

We've added SMD or SCSI interfaces. And we've

packed it into a sturdy, all-aluminum package that slides easily into a standard 8-inch envelope. Our MV330 is available today.

But we're not stopping here.

We're well into development of the world's first 660MB 8-inch drive, also with an 18 ms access time.

We'll deliver evaluation units of the MV660 in the second quarter of 1985.

We apply only proven technologies to our products, so our production schedules are predictable.

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At present, these optical storage devices come in two forms—read only and write once/read mostly. Developed as a follow-on to read only video disks introduced in the late 1970s, documentation storage devices based on read only technology can maintain 10,000 pages of information on 12-in. disks and access it in a half-second. Based on digital recording techniques derived from audio recording using pulse code modulation concepts, read only devices are also becoming common. Prerecorded 4.7-in. disks for use in these devices supply storage for 550 Mbytes and allow access within a second. Called CD-ROMs, devices such as these will probably find ready application as software distribution devices and for infrequently updated but widely dispersed data bases.

With this technique, optical memories come more in line with typical online data storage needs. The ability to write online makes these units amenable to database applications that require updating. Alcatel-Thomson's Optical Disc Div (El Segundo, Calif) aims to supplement magnetic devices with its Gigadisc GD1001. With data recorded on an 11-in. diameter laser sensitive optical disk, 1 Gbyte of formatted data can be stored on a single recording surface. Each surface of the disk is preformatted into 40,000 tracks with 25 sectors per track, to allow rapid random access of data. Shugart Corp's Optimem Div (Sunnyvale, Calif) supplies a storage system based on a 12-in. optical disk written on one surface. A similar unit from Optical Storage International (Santa Clara, Calif) matches this capacity. Both hope to gain acceptance in computer systems by supplying a Small Computer System Interface (SCSI).

Low cost optical disk-based document filing systems coming online include Reference Technology's (Boulder, Colo) CLASIX. This unit is based on prerecorded optical disks called DataPlates. These disks are loaded into a DataDrive series 2000 to be read. Designed specifically for use as a computer peripheral, the unit uses the SCSI interface and provides an average access time of 151 ns. LaserData (Cambridge, Mass) based its system on a standard video disk player to provide lower cost. It trades off cost, however, for both capacity (800 Mbytes/side) and access time (1.5 to 3 s).

A jukebox system, FileNet Corp's (Costa Mesa, Calif) OSAR consists of one to four optical storage drives, a robot picker arm, and up to 64 optical disks. Average access time for data on an already mounted disk is 200 ms. If the disk must first be mounted, access time increases to 8 s.

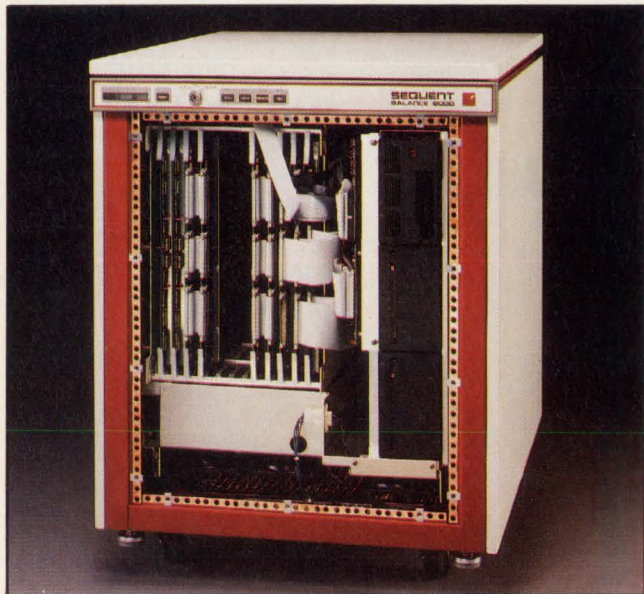
R&D efforts continue on the erasable optical media that have become critical to widespread acceptance in mainstream recording applications. Just when they will become available is still up in the air. The irreversible nature of the optical media currently

available, however, makes the technology particularly valuable where assurance is needed that data has not been falsified. Despite their potential for storing masses of data, optical recording devices remain several steps away from filling most online data storage requirements. There are lots of alternatives, however, as magnetic recording devices push to close the gap between the theoretical and practical limits of their technology.

### Magnetic storage moves ahead

Floppy disk drives, the old standby for all small systems, witnessed numerous half-height entrants in the 5¼-in. form factor. Designed into the majority of small systems, these units are moving up from their previous 520-Kbyte limitations to a new standard at 1.2 Mbytes. Hot on the heels of these units are increasing numbers of 3½-in. single-sided floppy drives storing 0.5 Mbytes. The size and packaging issues that clouded the future of these sub 4-in. drives seem to have been resolved by the major design wins achieved by Sony Corp (Park Ridge, NJ) and its hardshelled 3½-in. media and drive. The challenge of reliably recording on both sides of the media to bring capacity up to the promised 1 Mbyte remains unresolved, however.

Winchester drives in the 5¼-in. form factor have remained in the 5- to 180-Mbyte capacity range, while incremental increases appeared in 8-in. units to bring them up to the 380-Mbyte range. Boosted by the increasing complexity of software available for desktop computer systems, units storing 20



**Balance 8000** was designed by Sequent Computer Systems to dynamically and automatically balance the processing load among from 2 to 12 NS32000 processors. All processors share a single Unix copy that can be executed by all processors simultaneously.





**Harris 60 uses VLSI/LSI circuits and custom gate arrays that have over 8000 gates each. These, along with 256-Kbit RAMs used in the memory system, decrease bulk and cut costs.**

Mbytes in a half-height 5¼-in. form factor account for most entrants in the field. These came from Microscience International (Mountain View, Calif) and Cogito Systems (San Jose, Calif), among others. At present, 3½-in. Winchester drives hold the spotlight with units coming in with 5- and 10-Mbyte capacities. Designers should have 20 to 30 units of this kind to choose from within the year.

### **Tape cartridges also get involved**

This frenzy of activity in disk-based storage devices is complemented by similar action in tape. While reel-to-reel drives remain the mainstays of backup systems dedicated to large mainframe and minicomputer systems, IBM's half-inch tape cartridge is bound to cause some defections.

Serving as backup devices for 5¼-in. disk drives, quarter-inch streaming cartridge tape drives benefit from the increased involvement of MIS directors in the specification of desktop computer systems. These devices, supplied by Archive Corp (Costa Mesa, Calif), Data Electronics, Inc (San Diego, Calif), and Tandon Corp (Chatsworth, Calif) among many others, offer the low cost necessary for use with systems such as these. To win further acceptance for these drives, Cipher Data (San Diego) and Tandon Corp et al have provided a floppy-like interface. By taking advantage of the already existing disk controller, this interface is helping to keep costs down.

Supplying the backup needs of more capacious disk drives used with larger multi-user systems, half-inch tape cartridges from Rosscomp (Cerritos, Calif) and MegaTape (Duarte, Calif) store from 200 to 500 Mbytes on a single reel. Design differences have limited their acceptance, however. With standardization, cartridges can make a major impact on reel-to-reel tape drives.

Considerable new life was breathed into magnetic tape with IBM's introduction of the 3480 cartridge tape drive. While not the first to be devised, this unit should force a standard in the tape industry. And, although it can currently store 200 Mbytes on a single 4- x 5-in. reel of half-inch tape, it does not seriously strain the limits of tape technology. Contact recording with thin-film heads on chromium dioxide-coated tape should have theoretical limits in the 120,000 flux reversal per inch range. In fact, the drive as introduced records a modest 38,000 bits/in.

Equally important is the high level of intelligence and the large buffer that the unit provides. The provision for intelligence also guarantees continuous streaming, bringing the debate over streaming versus start/stop recording techniques to a screeching halt.

The provision of intelligence within the drive itself is also a debatable issue. The trend toward higher and higher densities in smaller and smaller packages has created the need to manage many disk functions within the drive itself. Another factor is the growing desire to offload disk handling functions from the CPU to gain optimum performance.

As increasing densities outgrow the capabilities of standard oxide media, plated or sputtered media will come into wider use. These media have an inherently greater defect rate that is intensified by the increased bit density that they provide. This exponentially expands the problem of defect mapping and the overhead required.

For these reasons, drive manufacturers and system designers agree that more intelligence should be placed at the drive level. Proponents of this theory include Shugart Corp (Sunnyvale, Calif) with its series 700S; Seagate Technology (Scotts Valley, Calif), which supplies its 8100 with an integrated controller; and Xebec Corp (Sunnyvale, Calif), which integrates the controller with the drive in its Owl series.

Another trend based on the same forces that are driving manufacturers to integrate controllers and drives is the increase in the number of traditional controller and drive manufacturers entering the sub-system business. Having reached what may be saturation levels in the disk drive industry, skeptics look for the shakeout. But more optimistic industry watchers note that for every contestant that goes belly up in the field, two more enter the fray.

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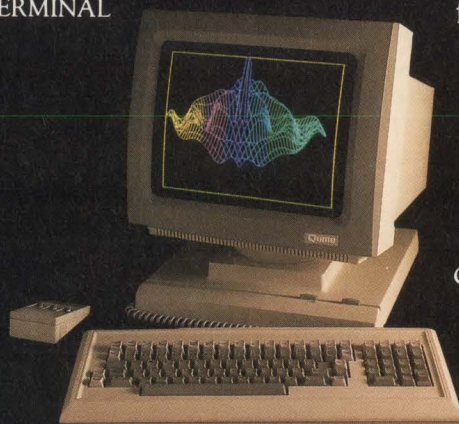
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## Superminis renew battle for top ranking

The flurry of recently released 32-bit minicomputers dampens rumors that micros have taken over the minicomputer world. Some say this renewed vitality stems from recognition of the need for an intermediary in the micro-to-mainframe link. Others maintain that minicomputers have always occupied a special niche because of their superior price/performance ratios, as well as their interactive natures.

Heading for top ranking in the supermini field, Gould extends its Concept 32 family with the addition of the 32/97xx, and Digital Equipment Corp puts together a machine that supplies more raw power than

the familiar VAX-11/780. Meanwhile, Harris Corp extends its 48-bit line with the entry level H60, and Modular Computer Systems Inc joins the 32-bit ranks with its Classic 32/85. In addition, AT&T launches its long-awaited line of mini and supermini machines.

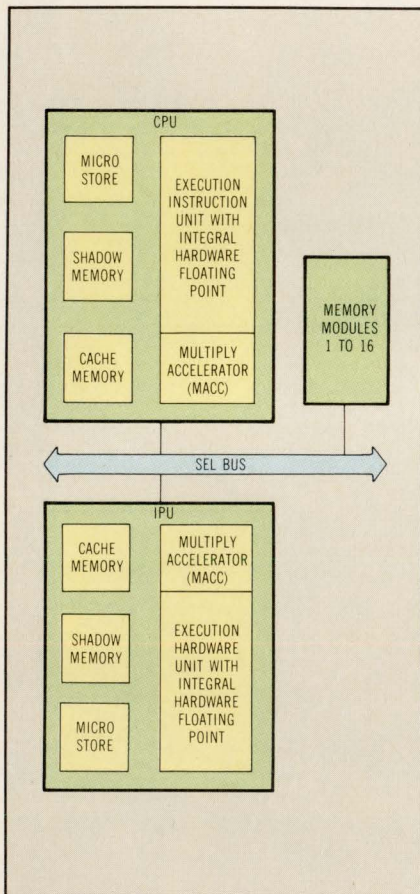
Harris Corp's H60 has a 48-bit CPU, which is contained on only two boards. The 256-Kbit RAM allows 6 Mbytes of memory to reside on a single board, while retaining all standard error detection, error correction, and diagnostic features. The optional single board integrated scientific arithmetic unit (ISAU) hardware processor supplies a 50 percent increase in floating point performance over equivalent software routines. The ISAU contains 900 fewer ICs than the previous 5-board implementation, a reduction achieved through heavy use of VLSI and custom gate arrays containing more than 8000 gates.

Aiming for a similar sized box, Gould fielded the PowerNode 6000 series. Composed initially of PowerNode 6030, 6050, and 6080, the series' performance is rated from 1.5 to 3 times that of the 11/780.

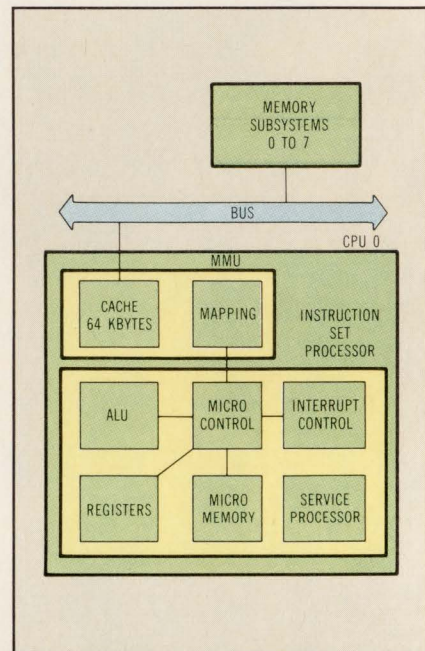
The supermini architecture of the high speed TTL CPU accommodates a 32-Kbyte, 2-way set associative cache memory. This memory provides 150-ns effective access time. Virtual addressing for up to 16 Mbytes, in conjunction with demand-paged hardware memory management, allows handling of large programs.

The Classic 32/85 marks Modular Computer's first venture into the high performance 32-bit world. With the CPU's effective cycle time of 100 ns and extended microinstruction word length that allows parallel internal operation, Modcomp leaves its traditional 16-bit realm. Aimed at answering needs for realtime response, this machine provides rapid movement between priority-based tasks with extremely fast context switching.

Gould's high end contribution to superminicomputer class machines



Functional units within the central and internal processing units that form the Concept 32/9780 are connected by internal buses that have 75-ns cycle times. During each 75-ns cycle, 4 macroinstructions are in various phases of execution, increasing the effective throughput of the system.



The CPU in Modcomp's 32/85 executes two instruction sets; one compatible with the 16-bit Classic II/75, the other providing 32-bit addressability. The instruction set processor is a complete ALU consisting of a functional microprogrammable processor with hardware multiply and floating point arithmetic. Microinstructions are contained in a writable control store.

supplies all the performance of previous Concept 32 systems, plus 16-Mbyte task addressing capability and modular performance enhancements. Moreover, in its basic configuration (with CPU, 4 Mbytes of main memory, and 32 Kbytes of cache memory), the 32/9705 provides performance rated at up to 4.67 million instructions per second (MIPS).

The long-awaited arrival of AT&T's promised contributions to the superminicomputer world lets established vendors breathe a sigh of relief. While extensions to the family promise significantly increased performance, the three mini level systems, the 3B20S, the 3B20A, and the 3B20D use readily available technology.

These systems use bit-slice bipolar technology and 64-Kbit RAM. The 3B20S architecture relies on programmable micro store with capacity for

8 Kbytes of 64-bit long instructions as well as cache memory, to attain speeds of 1 MIPS. With 8 Kbytes of cache enabled, the CPU can access its maximum 12-Mbyte memory in a 400-ns effective access time. The single processor 3B20S machine that supports up to 100 users and performs at a rate of roughly 1 MIPS grows into a 3B20A attached processor system that nearly doubles performance. Rated at 1.8 MIPS, the 3B20A uses parallel processing, with both processors performing operating system calls independently. The unit supports 50 to 180 users and costs only 30 percent more than the 3B20S system.

The 3B20D is a dual processor unit that provides fault-tolerant performance. To supply high reliability (minimum downtime), one processor acts as a hot standby for use only

when the other malfunctions. This unit runs the Unix realtime reliable (RTR) operating system to provide its fault-tolerant features within a real-time environment.

To stay competitive, DEC has introduced a new VAX, not the anticipated "Venus," but an adequate extension to the line. Along with this extension come promises that further additions will be made later this year. The new VAX-11/785 provides performance 50 to 70 percent greater than the 11/780, bringing it up to the 1.7-MIPS range. Improved circuit technology and internal performance enhancements in the traditional VAX architecture provide increased power. Improvements include implementation of the CPU from high speed advanced Schottky circuits, larger cache memory, new floating point accelerators,

and writable control store for micro-program instructions.

In spite of all this activity, the performance improvements displayed by these machines are marked more by evolution than revolution, and may disappoint those looking for great strides forward. However, recognizing that these incremental achievements were enabled through simple circuit tweaking makes speculation about future advances even more exciting. **Harris Corp, Computer Systems Division**, 2101 W Cypress Creek Rd, Fort Lauderdale, FL 33309; **Gould, Computer Systems Division**, 6901 W Sunrise Blvd, Fort Lauderdale, FL 33313; **Modcomp**, 1650 W McNab Rd, Fort Lauderdale, FL 33310.

Harris—Circle 260

Gould—Circle 261

Modcomp—Circle 262

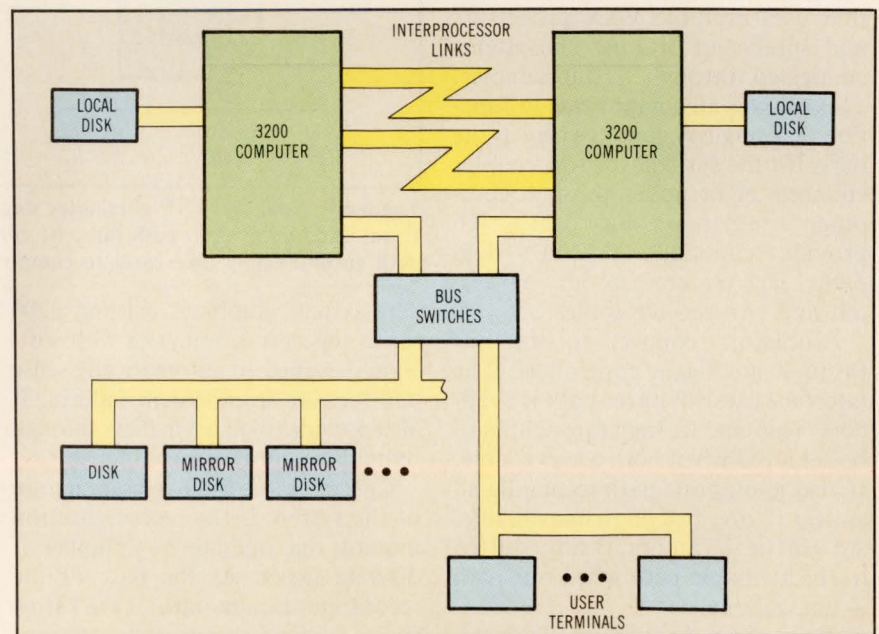
## Fault-tolerant systems deal with increased loads

Moving away from batch processing central computer systems, the transaction processing market has grown by leaps and bounds. To ensure continued operation of both the systems and the links, fault-tolerant systems came into being.

Tandem Computers was not only the first to recognize these needs—and supply a method of preventing a single failure from stopping the system—but the fastest in responding to increased demands. Tandem's recent upgrade, the NonStop TXP, builds on 32-bit minicomputer technology to overcome the limitations of systems based on 16-bit processors. Tandem's architecture depends on total redundancy. Multiple processors, dual-bus communications, dual-ported controllers, and multiple power supplies are inherent.

All processors independently process different applications, instructions, and I/O operations in parallel.

*(continued on page 94)*



**Perkin-Elmer's Resilient system combines redundant hardware components with reconfiguration monitor software. In addition, it allows independent operation of processors while providing either with the capability to take total control.**

**Fault-tolerant systems***(continued from page 93)*

However, if a module or data path fails, its counterpart automatically takes over to complete work in progress. The faulty part can be replaced or repaired without shutting down the system.

Each processor module is a 32-bit computer with a 32-bit native addressing mode and a 64-bit path to main memory. Each processor has its own 64-Kbyte hardware cache memory, and each can address 1 Gbyte of virtual memory.

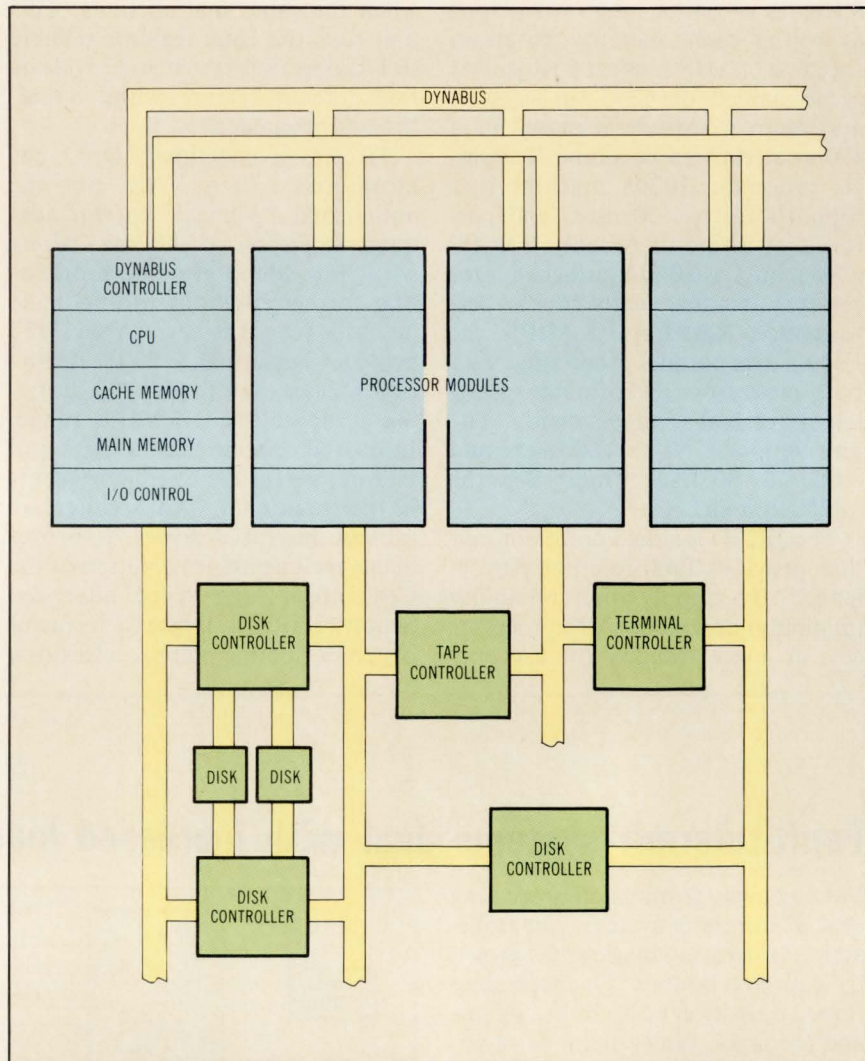
From 2 to 16 processors are accommodated in a single system. From 2 to 14 systems are linked through a 4-Mbyte/s fault-tolerant fiber optic interface to form a local network. Geographic dispersion is handled through networking software.

The system's 64/32/dual 16-bit design allows application programs written for any NonStop system to run on the TXP. Transfer requires no changes in code and results in two to three times greater throughput.

Traditional minicomputer vendors have also recognized the potential to expand into this market. Digital Equipment Corp offers a VAXcluster that uses multiple VAX processors and intelligent storage subsystems connected through a star coupler. This enables all components to function as a single system. Serving as the basis for the system, the star coupler connects eight nodes through computer interconnect bus cables. To provide redundant 70-Mbit/s data paths, each bus consists of two transmit and two receive cables.

Processors connect to the bus through intelligent controllers. The interface uses whatever path is available. This enables high throughput to be achieved when both are available. It also allows one path to handle all traffic if one becomes unavailable. All traffic is automatically shifted to the available path when one path is unavailable.

Attempting to outgun Tandem, Perkin-Elmer's Data System's group has put its 3200 series machines together with database software to form what it calls the Resilient system.



**Tandem's NonStop TXP eliminates single points of failure through total duality. If any module or data path fails, its corresponding device or alternative data path automatically takes over to complete the function.**

The system combines existing 3200 series superminicomputers with software designed to automatically sense and recover from system failures. It also provides high availability through redundant hardware components.

Central to the fault-tolerant nature of the system is the reconfiguration monitor that operates as a number of discrete tasks. At the base of the reconfiguration monitor is the kernel task, which monitors current machine configuration and communicates with the other processor.

These systems have eliminated the necessity for maintaining a "hot

standby" to protect transactions. By allowing each processor to handle tasks independently, throughput remains high until a problem develops. Meanwhile, these systems offer assurance that all transactions can be completed and that the integrity of the data base will be maintained should a component within the system fail.

**Tandem Computers**, 19191 Vallco Pkwy, Cupertino, CA 95014; **Perkin-Elmer, Computer Systems Division**, 2 Crescent Pl, Oceanport, NJ 07757.

**Tandem Computers—Circle 263**  
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## Personal computer benefits from 80286, networking, and software



Compatible with most IBM PC hardware and software, the 80286-based PC AT is available in two versions. The base model provides 256 Kbytes of memory, flexible disk drive, fixed-disk and drive adapter, and seven I/O expansion slots. The enhanced version has 512 Kbytes of memory, flexible disk drive, 20-Mbyte fixed-disk drive, fixed-disk and diskette adapter, serial/parallel adapter, and six I/O expansion slots. The AT requires a video display adapter and display output device.

The system unit holds the 80286 and provides a 6.0-MHz clock speed with 24-bit address and 16-bit data path. The internal 64-Kbyte ROM has 150-ns access time and 355-ns cycle time. The keyboard has 84 keys, along with the thoughtful addition of caps lock, number lock, and scroll lock indicators.

The diskette drive is a half-height 5¼-in. double-sided drive with 1.2 Mbytes of storage capacity. Standard in both AT models, a second drive of this type can be installed in the system unit. Both drives use the same fixed-disk and diskette drive adapter. The high capacity drive can read disks in 160/180-Kbyte, 320/360-Kbyte, and 1.2-Mbyte mode.

In the base model, the 20-Mbyte fixed-disk drive can be the first or second fixed-drive; in the enhanced

model it is the second drive. It is customer installable. With 20 Mbytes, storage has a 40-ms average access time with 512 bytes/sector, 17 sectors/track, and turns at 3573 rpm. Transfer rate is 5 Mbits/s.

Memory options for the AT range from 256- to 512-Kbyte increment expansions. The 256-Kbyte memory module kit allows the base model user to upgrade base memory from 256 to 512 Kbytes. It consists of 18 dynamic RAM modules that plug into existing sockets on the system board. The DRAMs are organized as 128-K x 1-bit, with 16-bit data paths.

With the 128-Kbyte memory expansion option, the base memory of both models expands from 512 to 640 Kbytes. For users requiring support for the 512- to 640-Kbyte address space, the AT is compatible with PCs,XTs, and IBM portables. Performance characteristics are identical to the 256-Kbyte memory module kit.

The 512-Kbyte expansion option allows for 512-Kbyte increment additions to expand above 1 Mbyte of base memory. Expansion slots hold up to five cards for a total of 3 Mbytes of primary storage.

Available operating systems include DOS 3.0, DOS 3.1, and Xenix. The DOS 3.0 configures itself to support six international keyboard versions and provides an enhanced

screen dump utility program. A virtual disk feature allows the use of extended memory (above 1 Mbyte). The operating system uses approximately 36 Kbytes of RAM. The DOS 3.1 version provides all DOS 3.0 functions, plus enhancements that support IBM PC Network hardware and software.

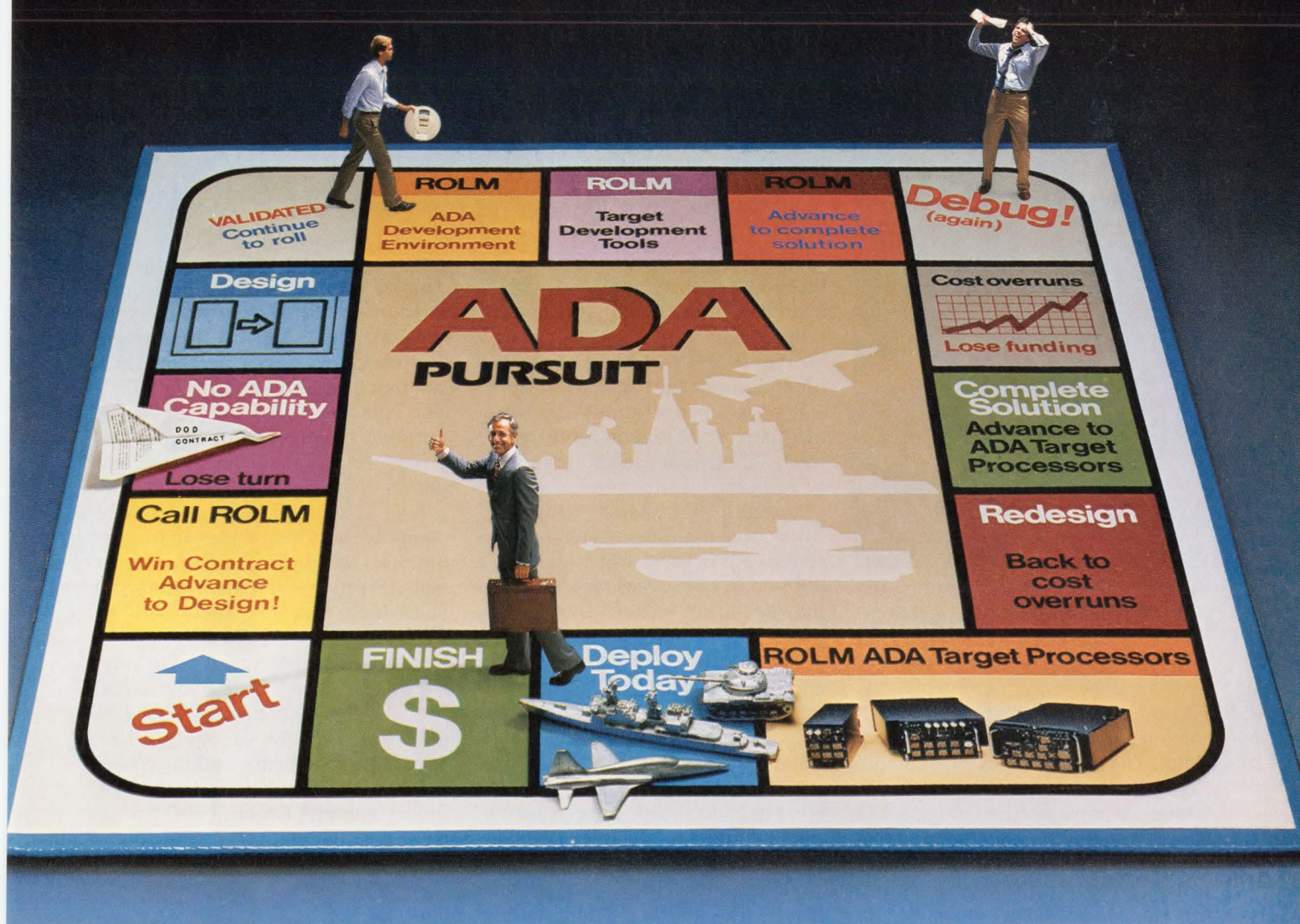
The company also offers Xenix (by Microsoft), which is derived from Unix. It supports single- and multi-user configurations and can run several programs at one time. It supports large memories up to 3 Mbytes via the 80286. Device support includes CPUs, three drives, CRTs, and printers. Optional features include a software development package and a text formatting system.

Topview software is also available. With Topview users can operate several different programs concurrently, switch from one task to another, or view data from several programs using windows—all on a single display screen. A Toolkit includes information on accessing functions from application programs, supporting mouse devices, and creating and using windows.

The low cost broadband PC Network uses standard 75-Ω CATV coaxial and connection hardware. The 2-Mbit carrier sense multiple access/collision detection (CSMA/CD) network consists of an adapter, a translation unit, and cabling hardware. The network adapter is a cord that connects the PC, XT, AT, and portables to the IBM PC network. The translator unit provides broadband frequency translation, from the return channel to the forward channel, for a passive network.

Price for the base model is \$3995 and the enhanced model is \$5795. Hardware options range in price from \$350 to \$1595, with network hardware from \$59 to \$695. In software, DOS 3.0 costs \$65, DOS 3.1 is \$65, Xenix is \$395, and Topview software is priced at \$149. **IBM Corp., Entry Systems Division, PO Box 1328, Boca Raton, FL 33432.**  
Circle 265

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CIRCLE 43

## Notebook-sized unit is an all CMOS system



With all the hoopla surrounding the issue of portability in personal computers, design engineers should find professional satisfaction in the fact that an experienced company has introduced the first notebook-sized computer containing more than empty pages. The Hewlett-Packard Personal Computer Group has designed an all-CMOS computer. It features 272 Kbytes of CMOS RAM; the MS-DOS operating system and two popular software programs (Lotus 1-2-3 and the HP MemoMaker) embedded in

CMOS RAMs; a 300-baud modem; and a 16-line x 80-char LCD screen—all in a package weighing less than 9 lb (4.08 kg) and costing \$2995.

In addition, an 80C86 16-bit processor lets the HP 110 portable run at twice the processing speed of that in the IBM PC. With the Lotus 1-2-3 business software package, which includes a financial spreadsheet, graphics, and file management embedded in ROM, business users can obtain an instant response to financial program operations. To top it off, battery life is good for up to two weeks of normal use before needing a recharge. Data preservation is guaranteed by the battery backup circuitry and monitoring system. This system alerts users when the charge is down to 20 percent, and locks out the keyboard when the battery reaches the 5 percent charge level.

The IBM PC can act as a dumb terminal to the Hewlett-Packard portable. It can dump programs into any IBM PC peripheral via the HP-IL cable and a 5¼-in. disk-based program called HP LINK. Although the HP 110 lacks a disk drive, a peripheral 3½-in. disk drive can be purchased for \$795. This drive provides an additional 710 Kbytes of data space on double-sided, double-

density disks. The HP 9114 disk drive also operates off rechargeable batteries for an average of eight hours. Again, its size is no bigger than a three-ring binder (8 x 11½ x 3 in. or 20 x 29 x 8 cm).

Rounding out the peripheral units for the portable is the company's ThinkJet printer, a quiet ink-jet unit introduced last March, which is the same size as the disk drive, weighs 5½ lb and costs \$495. In effect, users can purchase a full system for \$4285. This compares favorably with the HP portable's nearest competitors.

To meet the challenge of the company's definition of PC portability—a fully functional, battery-operated computer weighing under 10 lb—the unit uses the Harris 80C86 processor and HP's own RAMs and ROMs, all in CMOS. Coupling these with an LCD that can yield 128 x 480 pixels, bit-mapped graphics, and using long-lived lead-acid D-cell batteries, brought the overall weight to 9 lb (4.08 kg), kept the size at 13 x 10 x 3 in. (33 x 25 x 8 cm), and the power below 1 W. **Hewlett-Packard, Personal Computer Group**, 19447 Pruneridge Ave, Cupertino, CA 95014.

Circle 266

## RAM/CPU combination produces potent single-board system

Standard OB68K/MSBC1 equipment includes 256 Kbytes of triple-ported (CPU, Multibus, and local memory bus) RAM with parity. The zero wait-state RAM uses 128-K x 4-bit single inline package chips. Using these chips allows RAM to expand to 512 Kbytes. In addition, the board incorporates the 68000 16/32-bit microprocessor operating at 10 MHz on the Multibus. Optional processors include a 12.5-MHz 68000 and the 68010 virtual memory processor operating at 10 MHz.

When a parity error occurs, a circuit containing a 68230 parallel interface/timer chip identifies the specific RAM bank where the error originated. A 24-bit timer/counter in this chip generates system interrupts. Four JEDEC-style, 28-pin ROM sockets are also provided for monitor, boot, or program PROMs. Total ROM capacity is 128 Kbytes.

The board implements a high speed local memory bus over a P2 connector. This bus is functionally compatible with the Intel iLBX spec. The

local bus provides the 68000 with a high speed arbitration-free extension of onboard memory. Total capacity is 16 Mbytes with the addition of four memory boards. The local bus operates in conjunction with Multibus activities and without a significant effect on global memory or peripheral functions.

Two dual-universal synchronous asynchronous receiver/transmitter chips provide a four serial port capacity. These chips handle asynchronous protocols, synchronous byte-oriented

protocols (IBM Bisync), and synchronous bit-oriented protocols (X.25, high level data link control, and synchronous data link control). Two independent baud generators in each chip provide rates of up to 1000 kbaud.

An iSBX expansion connector provides additional I/O. Expansion modules plug in for a wide range of

I/O and control options including parallel I/O, serial I/O, floppy disk controller, printer port, IEEE 488 controller, analog I/O fixed/floating point module, or graphics controller.

Seven levels of priority interrupts, one of which is nonmaskable, configure to be bus-vectored or auto-vectored in any combination. All interrupt sources route to seven

inputs (also in any combination) via jumper cables.

The board implements full address and bus arbitration for single- and multiprocessor systems, and is compatible with a range of IEEE 796 products. **Omnibyte Corp.**, 245 W Roosevelt Rd, West Chicago, IL 60185.

Circle 267

## Full computer packed on a board

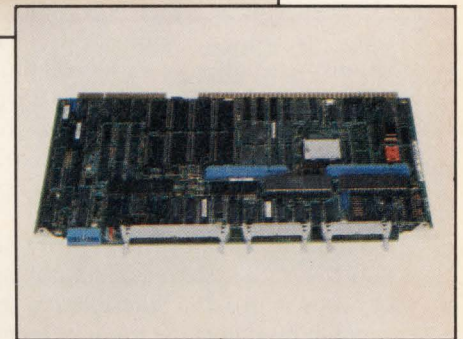
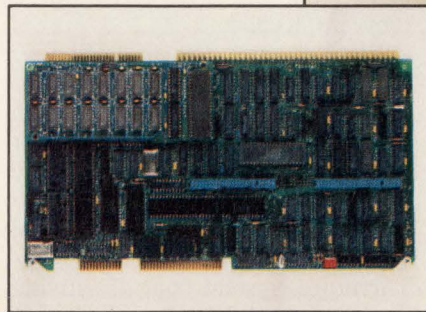
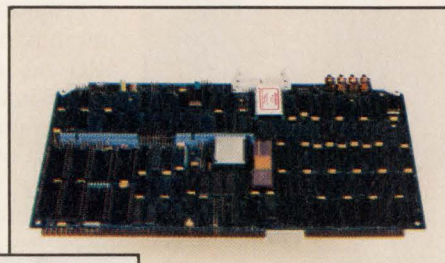
Three board-level computers, based on iAPX 186 and 86 microprocessors, provide such full-system capabilities as CPU, operating system functions, peripheral device interfaces, memory, and industry standard software. The iSBC 186/03, 186/78, and 86/35 combine these functions on single 6.75- x 12-in. Multibus PC boards. All run under the latest version of iRMX 86 operating system software.

Based on a 6-MHz, 16-bit CPU (the 80186), the iSBC 186/03 has eight (expandable to 12) 28-pin JEDEC universal memory sites, two I/O expansion connectors, interface for high speed memory expansion, and two programmable serial interfaces (one RS-232-C, the other RS-232-C or RS-422 compatible). It also has 24 programmable I/O lines, configurable as an ANSI small computer interface intelligent peripheral interconnect, as a Centronics parallel printer interface, or for general-purpose I/O. This board contains six programmable timers and 27 levels of vectored interrupt control.

The second computer, the 86/35, is based on an 8086-2 CPU (16-bit with 5- or 8-MHz clock rate). It contains 512 Kbytes of dual-ported read/write memory (expandable to 1 Mbyte with the iSBC 314, 512-Kbyte memory expansion Multimodule board), sockets for up to 128 Kbytes of JEDEC

24/28-pin standard memory devices, and two iSBX system expansion connectors. An optional iAPX numeric data processor is also available. This computer also has 24 programmable I/O lines and three programmable 16-bit BCD or binary timers/event counters. Its nine levels of vectored interrupt control are expandable off-board to 65. A programmable synchronous/asynchronous RS-232-C compatible serial interface offers software-selectable baud rates.

Video graphics subsystem 186/78, the third computer board, is also based on an 80186 CPU with 6-MHz clock. It includes an 82720 bit-mapped graphics display controller, and has a programmable 50- or 60-Hz frame rate. Resolution is 1024 x 800 x 1 interlaced or 512 x 512 x 4 noninterlaced; drawing rate is 150,000 pixels/s. Up to 16 colors can be displayed from a 4096-color palette.

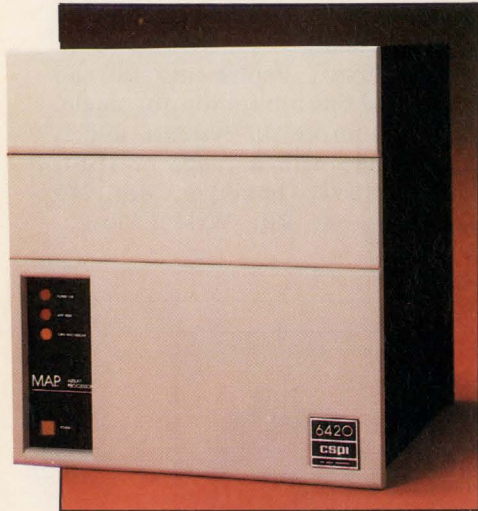


One available graphics software interpreter, the iPLP 720, implements the NAPLPS standard; a second, the iVDI 720, is based on the ANSI proposal for virtual device interface. PROM capabilities of both interpreters provide standard graphics support for the iSBC 186/78, or for an iSBX 275 Multimodule board. The system interfaces to either monochrome or color raster-scan display monitors, has eight universal memory sites for local RAM or ROM store, and provides full RS-343 or RS-170 support.

Production units of both the iSBC 186/03 and 86/35 are now available at \$1650 and \$3495, respectively; engineering samples of the 186/78 sell for \$3000. **Intel Corp.**, 3065 Bowers Ave, Santa Clara, CA 95051.

Circle 268

## Array processor executes algorithms at 5 MFLOPS



When interfaced to a host, the MAP-6420 provides a programmable peripheral that can offload, from the host, numerical algorithms—executing them several times faster than the host. Software development is Fortran based with highly efficient compiler-generated code and full integration into the host Fortran environment.

An independent control processor and separate system and data memory buses provide internal control capabilities that cause no interference with the processor's numerical computations. Data memory is expandable to 64 Mbytes, and for additional storage, disk subsystems can be used. Address space reaches 1 Gbyte for future memory configurations.

As the computational engine of the 6420, the arithmetic processor (AP) performs algorithms at speeds of up to 5 MFLOPS. The AP is made up

of a 32-bit integer/addressing processor unit (IPU) and a 64-bit floating point processor (APU) operating in parallel. To generate addresses fast enough to keep the APU near peak capacity, the IPU was designed as the fastest unit with both an integer adder and multiplier. The IPU also has powerful indirect addressing for efficient handling of sparse matrices and other complex data structures.

Programs for the AP reside in the internal program memories of the IPU and APU. Memory capacity is approximately 2000 lines of Fortran. Larger programs can be split into smaller overlays stored in system memory. These overlays are then loaded into the AP program memories from the array processor as they are needed.

Parallel execution of arithmetic, I/O, and system control through the use of multiple processors and memory systems allows efficient concurrent operation and high performance. The memory system consists of two independent memory buses, a 32-bit system bus, and a 64-bit data bus. Therefore, system control activities on the system bus do not degrade concurrent numerical computations on the data bus. In addition, the memories are not interleaved. Therefore, memory access time is consistently fast and not dependent on address patterns.

The system bus has anywhere from 256 Kbytes to 2 Mbytes of system memory, which stores the SNAP-III operating system, control information, and large user programs. This

bus is also used for all interprocessor communication. The data bus contains 4 to 64 Mbytes of data memory for storing arrays, variables, and constants associated with an application program.

Central to the development software on the processor is the MAP Fortran compiler that supports the user's development application libraries. Working together, the machine's architecture and the compiler provide fast, efficient execution of Fortran programs. Parallel units perform integer operations, memory references, and floating point operations in the program while both components optimize their concurrent operation. This approach is in contrast to other array processors whose pipelined architecture handles vector operations and exhibits poor performance unless the program is specifically optimized for the compiler.

All I/O, control, or communication between the host Fortran program and the 6420 is done with commands, declarations, statements, and calls—all familiar to the Fortran programmer. This software system, integrated into the host environment, allows development or conversion of scientific programs and packages to exploit both processor and host power.

The basic configuration includes 4 Mbytes of data memory in a 21-in. rackmountable chassis and is priced at \$100,000. The first host interface available was for VAX computers running VMS. **CSP, Inc.**, 40 Linnell Cir, Billerica, MA 01821.

Circle 269

## Subset of VAX architecture serves low end of 32-bit market

MicroVAX I extends the VAX product line with CPU performance that averages 35 percent of the VAX 11/780's. The two-board microcomputer implements a subset of the VAX architecture, and retains all the key family elements. These include virtual memory management with address capability of more than 4

Gbytes, sixteen 32-bit general registers, and 32 hardware and software interrupt priority levels.

In addition, all native-mode instructions are provided for byte, word, long-word, quad-word, and single- and double-precision floating point data types. Full memory management performs virtual to

physical address translation as well as page protection. The system supports emulation for the entire VAX instruction set, excluding the PDP-11 compatibility mode.

Some instructions that are hardware assisted in other VAX systems are implemented in software. They include both D and H floating point

instructions, decimal strings, some character strings, and compatibility mode instructions. The central processor resides on two quad-height modules occupying adjacent slots in the Q22 backplane. One module contains a 32-bit data path, a microsequencer, and control store. The second module contains both memory management and cache. It also provides the interface logic for the Q-bus connection to the internal VAX architecture. The system uses standard Q-bus memory modules and performs all data transfers in block mode.

Storage options include a 5¼-in., 10-Mbyte RD51 Winchester disk subsystem, and the RX50 dual-floppy diskette drive with a total storage of 800 Kbytes. A 28-Mbyte Winchester disk is also available. The system uses the same compact enclosure as the Micro/PDP-11 computer.

Software packages offer VAX compatibility in development and production environments. VAXELN software, a compatible subsystem to

the VMS operating system, allows application development for realtime control and distributed computing. Applications are written in an optimizing native-mode version of Pascal, which can be downline-loaded across network (local or wide area) links, or transferred to target systems by disk or by tape.

The MicroVMS operating system is a VMS system version for the MicroVAX. It comes specially packaged. The MicroVMS still provides the same runtime environment as larger VAX computers. In modular form it allows support for configurations with small secondary storage capacity and reduces the overall system cost.

ULTRIX is based on the Berkeley VM Unix system, which takes advantage of the VAX virtual memory architecture. It offers vendor inde-



pendence and portability. Prices for the MicroVAX I begin at about \$9995 for a diskless, rackmountable unit with 512 Kbytes of memory. With RX50 diskette and RD51 Winchester disk drives in a floor-standing unit, the price is approximately \$13,880. **Digital Equipment Corp.**, 10 Main St, Maynard, MA 01754. **Circle 270**

## Unix systems provide long-term solutions with upgradeability

A family of 68000-based systems for 1 to 16 users, the very intelligent Unix system (VIX) offers a 9-slot Multibus card cage (optionally upgradable to 16 slots). Model I has two 5¼-in. dual-sided, dual-density disk drives with 1.4-Mbyte capacity combined with 5¼-in., 20-Mbyte Winchester drive. Model II has 640-Mbyte disk storage capacity and 20-Mbyte streaming tape drive.

Both models feature UniPlus, a Unix System III operating system derivative with Berkeley enhancements. The enhancements provide a general-purpose Unix system for standalone computing, distributed data processing, and communication. The supported languages include C, Fortran 77, Pascal, Basic Plus, SMC Basic, Macro assembler, and simple assembler.

Using the 8-MHz 16/32 68000 micro with memory protection, the systems have 256 Kbytes of RAM on board (expandable to 1024 Kbytes), interrupt select logic, and an MMU. The Multibus card cage holds the CPU/main memory, main peripheral, RAM, I/O system boards, and mass storage modules.

As a companion to the CPU/memory board, the main peripheral module contains two serial programmable RS-232 interfaces, up to 64 Kbytes of EPROM, and an internal timer. Processor options are accessible via DIP switches.

The RAM memory module offers 512 Kbytes of RAM with error correction, while the mass storage module is a multifunction controller supporting dual-floppy and Winchester disk drives and streamer.

Also available is a series of very intelligent systems combining universal terminal emulation, 8- and 16-bit processing capabilities, as well as CP/M-80 or MS-DOS operating systems. The 8200 VIS series uses the company's intelligent terminals. Both terminals and systems support emulations for IBM 3275/71/77, DEC VT 100/200, and Data General's 410/460. Additional features include an 8- or 10-MHz 68000 with 1024 Kbytes of RAM, 128 Kbytes of EPROM, and 2 Kbytes of EAROM.

Prices range in moderate volume quantities from \$10,000 for Model I to \$23,000 for the Model II, not including terminals. A VIS, in a typical configuration, is \$4350 in moderate volume quantities. **Megadata Corp.**, 35 Orville Dr, Bohemia, NY 11716. **Circle 272**

## Laser-based optical disk drive stores 1 billion bytes

Based on a solid state diode laser, Digital Gigadisc GD 1001 provides a 210-Mbit/in.<sup>2</sup> (33-Mbit/cm<sup>2</sup>) recording density and a 4.1-Mbit/s data transfer rate. With three access methods, which are known as random, optimized random, and sequential, the drive allows direct access to any sector in the read or write mode. The drive also allows 3-ms access times within a band.

The unit subassemblies include an optical unit, optical head, linear motor, rotation motor, and a set of logic boards. The optical unit consists of a semiconductor laser module and a photo detector, while the optical head is actuated for both radial and vertical positioning of the laser beam (fine access). The linear motor provides the coarse access by moving the optical head and focusing it on the target track area. The rotation motor, on its axis, includes a disk seating and clamping device. Finally,

the logic boards control servomechanisms and disk accesses.

A 12-in. (305-mm) diameter cartridge encased disk eases all handling, storage, loading, and unloading operations. Each disk is preformatted in tracks and sectors. A sector can be directly accessed by its logical address. A spiral track organization allows continuous writing and reading of information streams. Once recorded, a physicochemical process (plastic copies) can entirely replicate a disk in one step.

The powerful automatic error detection and correction feature guarantees effective disk capacity. In addition, it maintains records at the quality level required in data processing environments, even after numerous years in archival storage.



Data-handling software is kept simple since each record is physically located at a programmer-defined address. This eliminates the need to check physical copies of the disk. The user is kept informed on the level of difficulty that the error correction process has met each time a record is read back. This lets the user check file integrity. **Thomson-CSF Communications**, 360 N Sepulveda Blvd, El Segundo, CA 90245.

Circle 273

## Tape drives enhance high performance of GCR with cache technology

The GCR CacheTape line is a family of compact, high performance, group code recording tape drives. The initial member of the family is the model M990, which offers the high performance of GCR coupled with cache technology; the M991 is a higher end version offering these same benefits.

Cache technology is the key element in the drive's design. The high speed solid-state cache memory replaces more costly and less reliable vacuum column and compliance-arm GCR mechanics. Though two-track error correction is usually possible in GCR drives, cache memory allows four-track correction. This results from a bidirectional (forward and reverse) correction scheme. The cache also provides start/stop software compatibility.

Model M990 features a 128-Kbyte cache size and a 450-kbyte/s maxi-



mum transfer rate. Maximum block size is 32 Kbytes. Model M991 has a 256-Kbyte cache and a 790-kbyte/s maximum transfer rate. Maximum block size is 64 Kbytes. This model also features downstream erase to eliminate tape repositioning on write error retries.

Both models use the standard Cipher half-inch tape interface for hardware integration. The outboard

error (defect) management relieves the host system of performance-limiting tasks including the handling of media defects.

The 6250-bit/in. drives provide up to 180 Mbytes of data storage on a single tape reel—nearly four times the storage capacity of conventional 46-Mbyte phase encoded drives. This lets the M990 support the backup of a 500-Mbyte Winchester disk drive with less than three reels of tape.

The low profile half-inch tape drive measures 14 in., an advantage when space is at a premium. In addition, user-friendly features include a patented front-loading and threading design with understandable, front-panel word displays and service maintenance messages. **Cipher Data Products, Inc.**, 10225 Willow Creek Rd, PO Box 85170, San Diego, CA 92138.

Circle 274



# NO GUTS, NO GLORY.

Parallel port included. Standard interface for popular printers.

Five full-length expansion slots for IBM PC/XT compatible option cards. Hard disk machine with 640K, real time clock, three I/O ports and display has two slots free.

Small overall dimensions, sturdy metal case, designed inside and out with horizontal or vertical operation in mind.

ROM BIOS AND MONITOR by ITT: Interrupt compatible with IBM PC/XT and more. Ever-ready menu-driven, diagnostic monitor debugger. Test hardware device by device and channel by channel. Examine registers, alter or dump memory, read or write tracks and sectors. Even set drive timing.

256K byte, parity-checked RAM on planar board. Combo board with one, two and three banks of 128K bytes each. Real time clock and parallel port also available to give 640K RAM total with only one slot used.

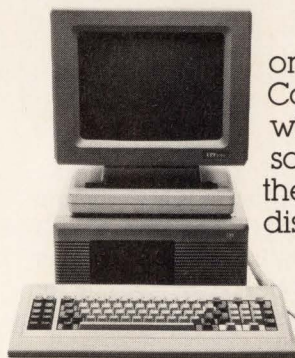
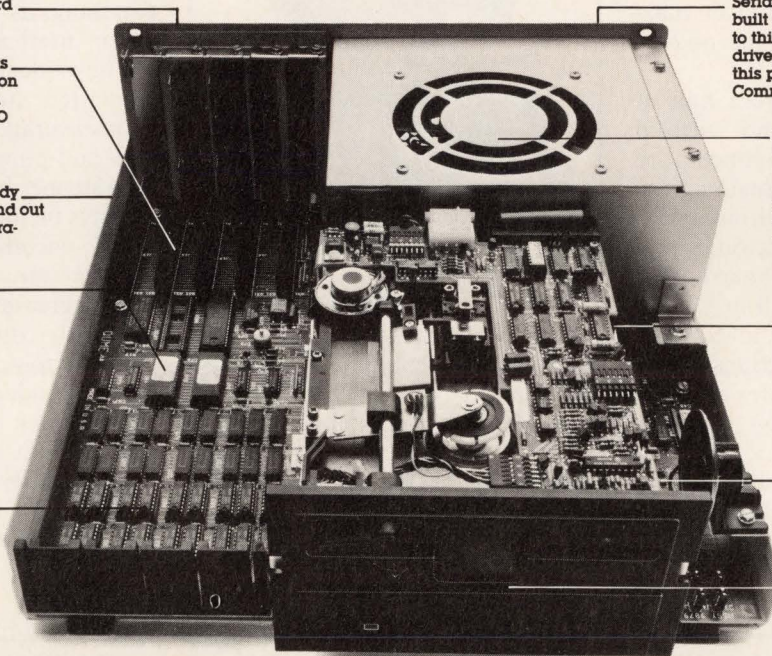
Serial (RS-232) communications port built in. Console I/O may be redirected to this port by switch setting. Menu-driven DOS utility (set up) to configure this port or redirect printer I/O to it. Communications program included.

ITT's own heavy duty, high efficiency switching power supply (115 watts continuous service) saves weight without compromising support for fully-equipped machines. 95 to 132 volts or 180 to 240 volts.

Switch controls allow console I/O redirection to serial port - use whatever ASCII terminal you want. Enable/disable power-on memory test for faster starts on large machines. Enable/disable screen-saving blanking when left idle.

Floppy disk controller on planar. Saves a slot.

Space-saving half-height disk drives.



Monitor conveniently tilts and swivels. Green, amber or color. Three-position keyboard. Our very own, fully-supported ITT Mouse.

Pop the rugged metal case on the new ITT XTRA™ Personal Computer and you'll find what thousands of our personal computer users across the country have already discovered.

The beauty of the ITT XTRA Personal Computer is definitely more than skin deep.

In fact, it runs all the way down to the very last power supply winding.

This is one of the most cleanly designed, most extraordinarily simple machines to come along in quite awhile.

We modestly consider it the finest personal computer compatible on the market.

An example. Where IBM has BIOS support routines for its BASIC, we have a ROM monitor and diagnostics utility that's always available, provides direct disk access and isolates problems right down to the chip level.

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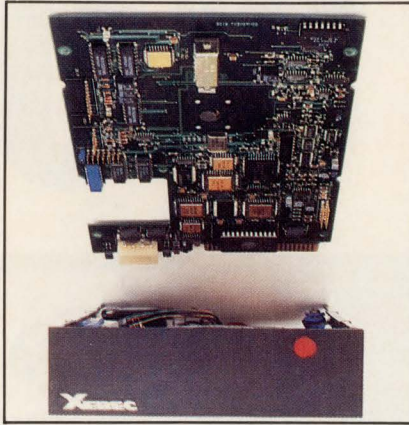
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## Winchester drive merges controller electronics on single board

The Owl 10-Mbyte Winchester disk drive incorporates a S1410A disk controller on the drive electronics board. Previously, one board contained the controller and the other board held the drive electronically. The intelligent half-high 5¼-in. device is suited for single-user micro-based systems, as a built-in mass storage device, or as an add-on storage subsystem.

Board components are a mix of both standard LSI and custom devices. All of these components are surface mounted, thus enabling the combination of two traditional 5¼-x 8-in. boards (disk electronics and controller). The actual board footprint is 1.63 x 5.75 x 8.0 in.

Using custom circuits, all S1410A disk drive controller functions can be implemented with fewer devices. One chip combines serialization, deserialization, and error detection/correction functions with a digital data separator. The built-in data separator is optimized for increased read and write performance. Ground-loop noise and induced errors are reduced



via the closeness of the data separator to the drive. The LSI components include DMA, a Z80, a programmed I/O chip for the Z80, and the SASI interface component.

Providing the high level interface between the disk drive and host, the controller interface is made up of a generic command set plus an 8-bit parallel data bus for communication. This high level command set reduces host system overhead and is compatible with all Xebec SASI systems. A system integrator needs only to de-

sign an SASI host adapter onto the host to accommodate the Owl drive.

The built-in controller provides automatic seek and position verification and automatic command retry when an error occurs. Other features include multisector data transfer with automatic cylinder and head switching, as well as programmable sector interleave.

The oxide media drive's 10-Mbyte formatted storage capacity has a 99-ms average access time. It uses a rack and pinion actuator and open-loop stepper head positioning. Other features include head shipping zone, MFM encoding, and a 5-Mbit/s transfer rate.

To increase reliability further, the matched components share one power supply, lowering induced error rates. In addition, traditional disk drive cabling is eliminated, reducing transmission line effects.

In quantity, the drive/controller combination is priced under \$500. **Xebec**, 432 Lakeside Dr, Sunnyvale, CA 94088.

Circle 275

## Cache RAM accelerates Winchester disk transfers

The 10- or 20-Mbyte DisCache subsystem includes a 5¼-in. hard disk, a RAM cache (up to 256 Kbytes), a specialized microcomputer, and an incremental backup system. It improves microcomputer performance levels by making some programs and/or data on the Winchester immediately available from RAM rather than disk.

Optimized for typical micro database programs, the system returns around 75 percent of all sector access requests from RAM instead of disk. Maximum access time for a sector from RAM is only 100  $\mu$ s, compared with a typical maximum of 200  $\mu$ s

from a Winchester. An independent processor makes these fast access times possible. DisCache constantly monitors the sectors requested from the disk, and automatically keeps frequently used sectors in the RAM "cache" for immediate access. The caching algorithm continually optimizes the contents of the cache.

Part of the cache is reserved for anticipatory buffering. The requested sector as well as 31 neighboring sectors load into the cache. Statistically, these additional sectors will probably be requested next by the host computer. Speed is also improved when writing a sector to disk. The proces-

sor immediately accepts a sector and stores it in RAM. This allows a user's program to continue running without a disk access delay. After pausing for additional sectors from the same track, the processor subsequently transfers the new sector to the disk.

A print spooling facility accepts virtually unlimited printer output at a high data transfer rate. This permits the microcomputer to continue running as though the print operation is complete. Data transfers from the spool are then considered a background task by the processor. Many print jobs queue off the system. An

*(continued on page 108)*

**INTRODUCING  
THE IBEX MAINSTREAMER®**



## THE LEAN MACHINE

The IBEX MAINSTREAMER is a revolutionary new IBM format compatible 1/2-inch tri-density streaming tape drive that slims and trims your space and budget requirements in one easy installation.

At less than 40 lbs., this mighty mite weighs over 60% less, costs 25% less and occupies 25% less space than any other 9-track tape drive available.

The MAINSTREAMER is IBM and ANSI compatible. It can accommodate standard 1/2-inch, 9-track tape reels from 7 to 10-1/2 inches in diameter, yet it fits into dual 8-inch Winchester or floppy drive footprint.

There's more. Much more. The IBEX PCT-1000 MAINSTREAMER gives you:

- Storage of up to 136M bytes per reel
- Transfer rates of 20K to 160K bytes/second
- 800 bpi NRZI, 1600 and 3200 bpi PE format operation
- Plug compatible with standard Cipher/Pertec interface
- Internal diagnostics
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No matter what your application — disk backup, data interchange, or access to archives — the MAINSTREAMER is your most cost-effective, load-lightening answer.

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**CIRCLE 45**

**Cache RAM***(continued from page 106)*

optional second printer port allows separate spools for two printers, which can run simultaneously.

For security backup, the processor keeps track of which sectors on the disk are being updated. The option remains with the user to write only updated sectors to a security backup on the floppy disk system, or to make complete copies. The updated copy typically takes 30 s, eliminating the need for backup devices.

The complete option minimizes the required number of diskettes and relieves the need to supervise the process. Software manages the pro-

cess to ensure that all data is backed up. It also validates each diskette and checks for the correct sequence in the Winchester restoration process. Another feature of the daily backup facility restores the disk to its earlier state, thereby undoing corruptions and erroneous deletions.

Cache-Net acts as an enhancement to the system. It permits up to 21 personal computers (NEC, IBM PC, Apple II) and operating systems to share access in any combination. At a basic line speed of 1 Mbyte/s (similar to Ethernet), Cache-Net allows data transfers at the full DMA speeds

of the computers themselves. Average sustained rate is 250 kbytes/s.

Since DisCache's internal processor handles the polling of users, it eliminates the need for an additional multiplexer box, or master or supervisory computer. Each additional machine daisy chains to the previous one via a cable. The expandable chain accepts different types of computers at any point. **Eicon Research, Inc.**, 2157 Park Blvd, PO Box 60456, Palo Alto, CA 94306.

Circle 276

## Memory bubbles packaged to ride high on the Multibus

Offering built-in 1-Mbit bubble devices, the FBC504M4M series provides four different memory capacities—128, 256, 384, and 512 Kbytes. The card operates as memory-mapped I/O requiring only a 64-byte memory space. Advantages include a single 5-V power source, an internal power fail protection circuit, and data retention even without power.

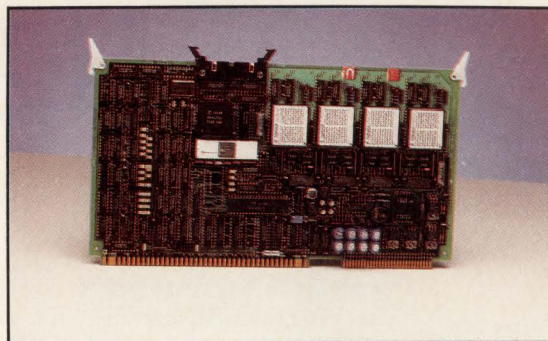
All bubble memory operations are controlled by commands that are set by 5 separate bits in the command register. Several registers act as the interface between the host and the bubble device. A 4-byte FIFO data output register holds data that is read from the bubble. When a data read command is set in the command register, data transfers from the bubble memory to the data output register at a 80- $\mu$ s/byte rate.

Page changes increase this transfer time by 0.3 to 1.5 ms. As the data transfer begins, the number of pages (as specified by the host system) goes to the data output register at the same 80- $\mu$ s rate. Also a 4-byte FIFO register, the data input register functions in the same manner when the data write command is in the command register.

Other registers include a status register, which indicates the card's condition via flags. An error status register lists error contents; a page address register holds the starting address of a page; and a page count register keeps track of the number of pages that will be transferred. In addition, a DMA band select, write only register is accessed for DMA transfers.

The bubble device operates in various software-controlled modes. The read/write command sets the interface registers to execute the read/write operation. It begins by sending the start page from the host to the page address register and the number of pages to be transferred to the page count register. The command register is then set with a command, thereby allowing a sequence of operations to execute.

First, bad loop data is automatically read from a boot loop. An error occurs if the bad loop data is invalid or if the data cannot be read. Next, the page indicated in the page address register is searched. Data is then writ-



ten to the bubble via the data input register or read from the bubble via the data output register.

During the transfer process, the controller continuously refers to the bad loop data storage so bad loops are skipped. When all the pages indicated by the page count register transfer without errors, a status register bit is set.

Other memory card features include a 12.5-ms average access time, subpage read/write commands, and error correction.

Prices for the series range from \$620 to \$1410 in 100s. **Fujitsu America, Inc., Component Division**, 918 Sherwood Dr, Lake Bluff, IL 60044.

Circle 277

# ASC 525

UNIX™ † ACCELERATOR

† Or any other system.

**SUPER** Accelerate your system's disc performance with the **ASC-525™** cached disc controller with 320K bytes of fast access ram. This is not a ram-disc that robs the CPU of processing power. It is a full SCSI controller doing true background mode algorithm execution with overlapped cache search and data transfer.

The **ASC-525** speeds the disjoint block transfer of **UNIX\*** by keeping 40 tracks of winchester data current in the under 1 ms access cache - thus shrinking the disc access time penalty.

**INTELLIGENT** management of disc data - so necessary in today's high performance multi-user environment - is standard with us.

- Full SCSI implementation
  - Arbitration
  - Disconnect/Reconnect
  - Reserve/Release
- Large **320 K** byte cache
  - 1K element size
  - Under 1 ms access time
  - Statistical LRU algorithm
- 5¼ form factor
- Multiple concurrent operations
- 8088 microprocessor (6.7 MHZ)
- Controls two large ST-506 discs

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9660 Hillcroft  
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\*UNIX is a trademark of Bell Laboratories.

## Tape subsystem exhibits full-size performance at low cost

The model 9250 Shamrock group code recording tape drive uses advanced LSI gate array and microprocessor technology to condense its GCR formatter onto two circuit cards. These cards are directly integrated into the tape drive package to support high end performance.

The 50-in./s, start/stop device features vacuum column technology. The brushless, direct drive, pneumatic system is insensitive to changes in voltage, amplitude and line frequency, and day-to-day variations in barometric pressure.

Automatic threading, including tip of tape detection and column loading, occurs via one button. This feature minimizes operator tape handling and contamination. Automatic rewind takes only 2 min for 2400-ft reels.

Tape densities start at 6250 bits/in. in GCR and include 1600 bits/in. in phase encoded. Two methods of density selection are available. The host computer can select the density under software control or the operating system or interface can allow the oper-



ator to select the density. For users with 800-bit/in. nonreturn to zero inverted (NRZI) requirements or large existing NRZI libraries, the drive's tri-density option eliminates the need for additional tape drives.

For applications requiring multiple tape drives, it allows master/slave daisy chain expansion to 1 x 2, 1 x 3, and 1 x 4 systems. Only the master has the embedded formatter, saving the expense of duplicating both the formatter and the interface elec-

tronics for each additional tape drive. For flexibility in the field, any master unit can be converted to a slave (or vice versa) by moving the two formatter circuit cards.

Tape drive specs include a tape speed of 50 in./s, a gap size of 0.3 in. in GCR for read and write, 0.6 in. in phase encoded for read and write, and 0.6 in. in NRZI for read and write. GCR access times reach 3 ms for a write and 3.4 ms for a read. Transfer rates are 312.5, 80, and 50 kbits/s for 6250-, 1600-, and 800-bit/in. tape densities, respectively.

Using GCR technology has several advantages. It offers increased data density for significant file compaction over previous industry standard densities. This results in less media to store data, less library space, and reduced handling. System throughput enhancements occur via a high data rate together with automatic error correction circuitry to eliminate rereads. The 9250 costs \$7399. **Telex Computer Products, Inc.**, 6422 E 41st St, Tulsa, OK 74135.

Circle 278

## Featherweight floppy disk drive stores 500 Kbytes



Measuring 32 x 104 x 161 mm (1 x 4 x 6 in.) and weighing 600 g (1 lb), the JU-312 floppy drive is one-fifth the volume and one-third the weight of typical 5¼-in. disk drives, yet plug-compatible with its bigger brothers. The low cost drive takes single-sided disks that store 250 Kbytes each; a single-sided, double-track method boosts that capacity to 500 Kbytes. Beyond that, the company has near-

term plans for a double-sided, double-track release that will top 1 Mbyte. Data transfer rate is 125 kbits/s FM or 250 kbits MFM. Controlled by a single LSI chip, a three-phase, brushless motor spins the disk at 300 rpm. This flat motor mounts directly on the package board, to use available space best.

Together, the direct-drive stepping motor and a steel drive band ensure high reliability, and position the read/write head for 6-ms track-to-track seeks. Maximum settling time is 15 ms, while average positioning time is 58 ms. The estimated deviation is  $\pm 1$  percent, and the variation is  $\pm 1.5$  percent.

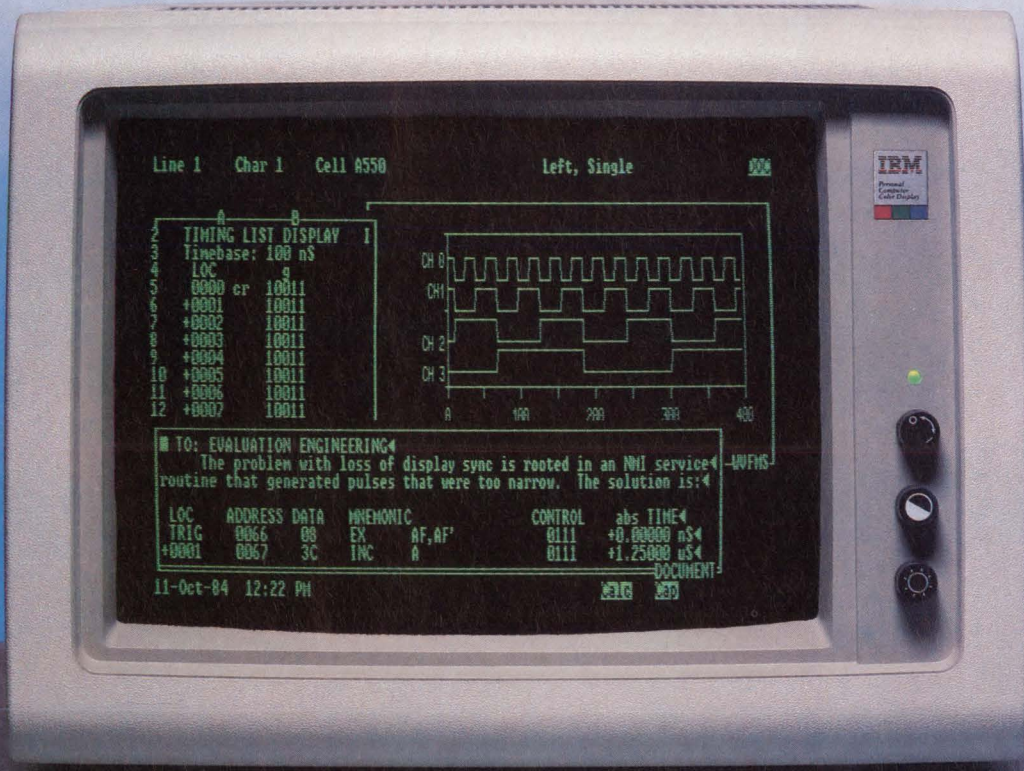
Greatly reduced parts count also improves reliability. In all, three custom LSI chips with minimal support components control the disk drive; the other two LSI circuits manage read/write and control functions. The interface side of the control circuit sends

and receives TTL-level signals. In star or daisy chain configuration, up to four drives will attach to the controller. Gateless drive mechanics consist of a die-cast aluminum base plate that connects to signal ground; mountings protect drive circuits from electrical noise. In quantity, unit price will be about \$100.

Media stow in a hard plastic case featuring button-controlled write protection and a head window shutter that opens when a disk enters the drive. A loading mechanism automatically inserts or ejects disks when activated by a push button on the front panel. This packaging and loading concept makes it easier to store and handle the disks, and gives the vulnerable magnetic media a measure of protection against the environment. **Panasonic Industrial Co, Electronic Component Division**, PO Box 1503, Secaucus, NJ 07094.

Circle 279

# Only our Logic Analysis Workstation can pass this screen test.



Why? Because it's the first system that combines logic analysis with an integrated software package on the new IBM PC AT\*, PC XT\* or IBM PC\*. The  $\mu$ Analyst LAW from Northwest Instrument Systems.

And what a logic analyzer! The  $\mu$ Analyst brings you the industry's most powerful analyzer for under \$10,000. Up to 80 channels of state acquisition with 15 trigger levels. 16 channels of 100 MHz timing acquisition, both conventional and transitional. Correlated state and timing displays. 8, 16, and 32-bit disassembly.

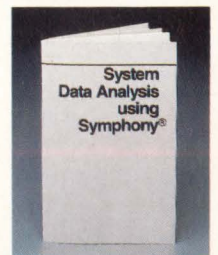
But that's only the beginning. Once you've acquired your data, the personal computer can go to work on it.

Using our Lotus-Link™ software, data can be loaded into Lotus Symphony™. Once there, use the resident graphics



and database functions for filtering, analysis and custom graphing. Or create co-resident programs for special applications. You can even place important data right into engineering documentation and send it to other computers using the integral word processor and communications packages.

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"For logic analysis, you can't beat the LAW"

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What if you could build a VLSI logic device in just a few hours? Instead of months.

And control every step of the process? Instead of relying on outside vendors.

Or change your design for just a few dollars? Instead of a fortune.

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Instead of a gate array.

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It's easy to use. And it's fast.

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The instant alternative to gate arrays.

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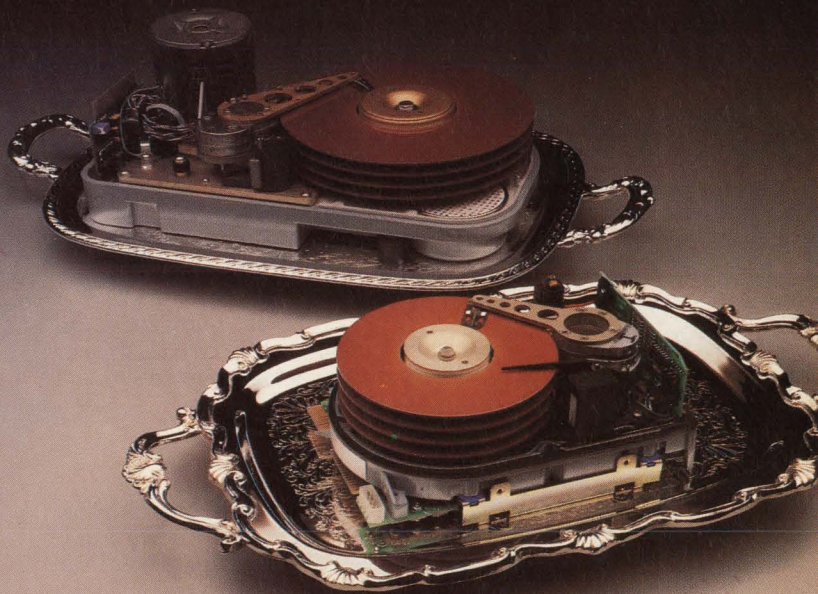
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CIRCLE 49

# TeleVideo corrects the VT220 key mistakes.

The new TeleVideo® 922 shares but one feature with the VT220®: DEC®-compatibility. The similarity ends there.

**1.** Take our keyboard, for example. The RETURN key is within direct, easy reach. But VT220 users must stretch over an additional key to hit RETURN. Or have the hands of a concert pianist.



DEC VT220

**2.** Our ESCAPE key is located above the TAB key, right where you'd expect to find it.

Theirs isn't.

In fact, you have to go hunt for the VT220 ESCAPE key halfway across the row of function keys.

**3.** Take a look below at the 922 keyboard.

That's a true accounting keypad, complete with a Clear Entry, Double Zero and a TAB key. Not merely the numeric keys you get with the VT220.

**4.** Our SHIFT key is exactly where it should be, so it does exactly what it should do—shift. Their SHIFT key is shoved over by the < and > key to create lots of < and > on the CRT. Of course with a little practice, you could re-learn their keyboard. But why, now that you've seen our 922?

Moving The Shift Key Is A Mistake.

922 Display Screen.

<oving <he <hift Key <s A <istake.

VT220 Display Screen.

**5.** And after we built a better keyboard, we built a better terminal. With exceptional reliability. Quality. Advanced ergonomics. Everything you'd expect from the industry ANSI leader.

The new 922 is available now and priced to move now. And it's backed by a worldwide sales and support network.

**6.** Here are 5 more advantages to the 922.

	TeleVideo 922	DEC VT220
Programmable Function Keys	15 (30 with shift)	15 (shifted only)
True Accountant Keypad	YES	NO
Plug-in Graphics Upgrade Option	YES	NO
Full Tilt & Swivel	YES	NO
Enhanced ANSI Mode	YES	NO

DEC VT220 is a registered trademark of Digital Equipment Corporation.

800-538-8725.

In California, call 408-745-7760.



The TeleVideo® 922  
TeleVideo Systems, Inc.

# PERIPHERALS GET SMARTER AS COSTS MOVE DOWNWARD

Local processors, modular designs, and custom approaches are reducing system costs and turning computer peripherals into intelligent workhorses.

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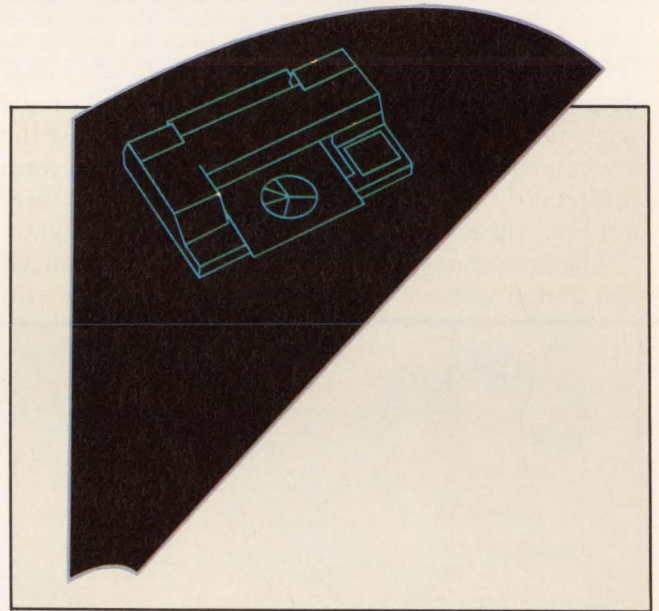
by **Nicolas Mokhoff,**  
Senior Editor

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Hardcopy computer peripherals are increasing in performance while coming down in price. This was most evident this year in the case of nonimpact printers. With laser page printers priced at less than \$4000 (Hewlett-Packard's Laser Jet costs \$3495) and more ink-jet, ion-deposition, and magnetographic printers coming to the market to accommodate a full range of mainframe and microcomputers, non-impact printers are bound to become more prominent in the computer peripheral arena next year.

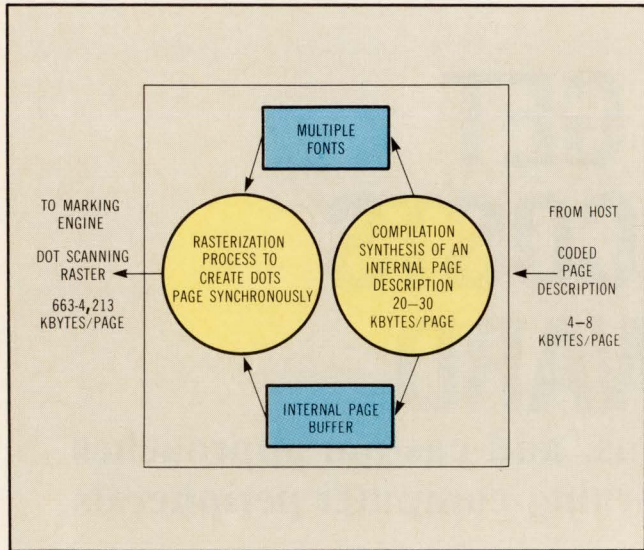
Several technological breakthroughs have made this possible. More companies are developing controllers and interfaces that customize printer systems for individual applications. This allows an OEM to buy any printer "engine" and attach the appropriate frontend image printing processor for its application. Another breakthrough is the availability of reasonably priced printers that use such relatively new technologies as ion deposition and magnetography. Both technologies have a potential price/performance edge over laser printers, but still are far from matching the price/performance of ink jets.

The manufacturing trend to provide separate engines and image processors stems from the inherent advantages of a modularized printer system. The downward pressure on the price of nonimpact printers has created a new industry that is dedicated



to the development of frontend image processors that may or may not be device independent. When integrated with the nonimpact printers, the processors enable the printers to act as high quality text and graphics printers. The primary objective of the rapidly expanding industry is to provide aesthetically appealing output.

Imagen's 5/480 is one such printing system. This Mountain View, Calif company separates its marking engine from the image processor. Thus, a number of host processors can be attached via different interfaces. In effect, the image processor is a specialized computer that generates images electronically and controls printer system functions. In operation,



The image processor from Imagen epitomizes other image processors that serve as frontend processors between the host computer and the marking engine. A specialized computer in its own right, the image processor accepts page description information from the host computer and synthesizes the raster needed to operate its marking engine.

page descriptions come from the host processor as characters and dots. The image processor takes page descriptions and synthesizes the dots to print on the page using a raster scanning technique. Because the image processor allows the user to print on several printers of different speeds and resolutions, it does not limit the user to one particular marking engine.

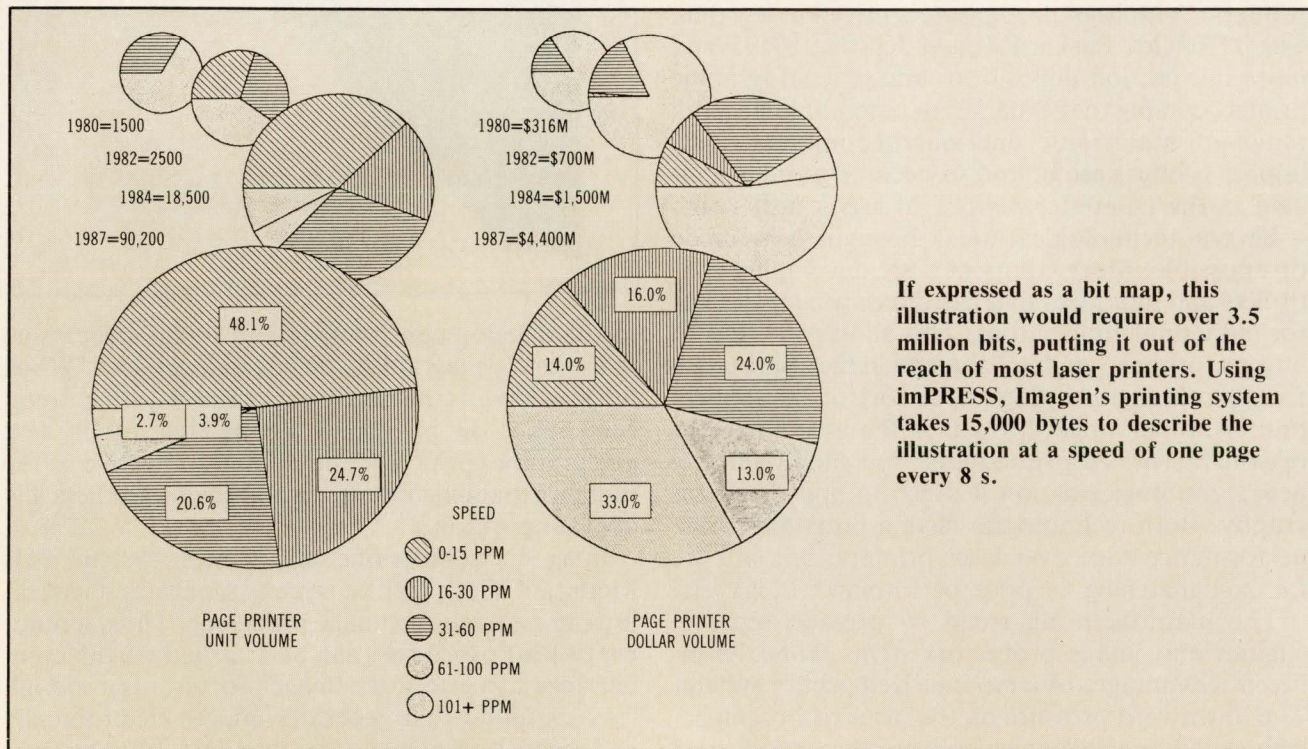
The printer engine used in the 5/480 prints mixed text and graphics at 480 dots/in. using a laser with

a liquid toner at a nominal speed of 5 pages/min. The engine can accommodate fourteen paper sizes and multiple fonts. The image processor consists of a 68000 with a 512-Kbit RAM that can be expanded to 2.25 Mbits. In addition to the usual RS-232-C serial and Centronics parallel interfaces, the image processor can also accommodate Ethernet and IBM 2780/3780 connections.

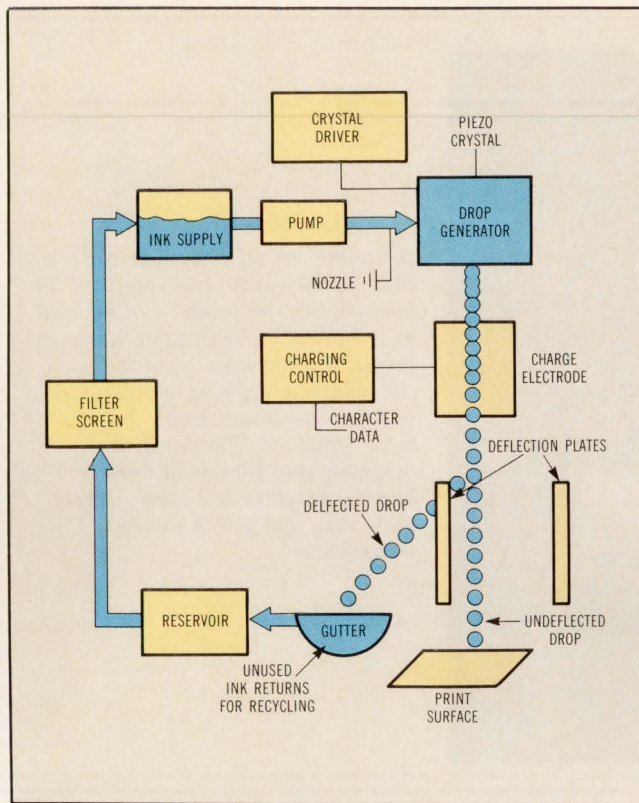
### A sophisticated processing approach

Imagen's proprietary image processing system uses an intermediate language, imPRESS, to create a concise page description that radically reduces the transmission time between the host computer and the image processor. The imPRESS language also allows a page description to be stored in a very compact format. This significantly reduces the amount of RAM needed in the image processor. Alternative approaches to sophisticated image processing that combine high quality text and graphics require a bit map to assemble the information. These schemes increase the RAM requirements and subsequently increase their cost.

For instance, a typical 8½- x 14-in. page at 300 dots/in. resolution would require approximately 1.4 Mbytes of memory using a bit-mapped design scheme. The total memory requirement in Imagen's processor for describing the document is between 20 and 30 Kbytes. This is due to the algorithm that describes a page by optimizing the data structure of that page. A page description may consist of text, graphic primitives, and bit maps. Using the graphic



If expressed as a bit map, this illustration would require over 3.5 million bits, putting it out of the reach of most laser printers. Using imPRESS, Imagen's printing system takes 15,000 bytes to describe the illustration at a speed of one page every 8 s.



In the continuous flow ink-jet printer, Diconix forces the ink under pressure through the orifice while the ink chamber is stimulated at a particular frequency by a piezoelectric crystal. The stimulated ink breaks into drops which pass through the electric charge zone and are separated into charged and uncharged drops. Charged drops get collected while uncharged ones print.

primitives, a 4-in. square with a circle, enclosed and cross-hatched, requires only 25 Kbytes of memory versus 180 Kbytes with the bit-mapping technique.

Imagen has geared the 5/480 for three distinct applications: typesetting, graphics, and office automation. For typesetting applications Imagen's software packages include popular composition systems including Scribe, Di-tro, Troff, and TEX. TEX is a composition program designed by Dr Donald E. Knuth of Stanford University that allows the author complete freedom in page design through a simple user interface. Imagen supports all capabilities of TEX including mathematical functions with fonts that are resident either in the printer or that can be downloaded from the host computer. For the host computer, Imagen provides over 400 different font magnifications of over 90 different basic fonts.

The 5/480 lists for \$19,950. A newer model, the 60/240, prints at 60 pages/min with 240 dots/in. and lists for \$75,000. The rapidly growing list of companies developing processors to be incorporated with the nonimpact printing engines includes Adobe Systems, Inc (Palo Alto, Calif), Interleaf, Inc (Cambridge, Mass), Burroughs Corp (Detroit, Mich),

Xerox Corp (El Segundo, Calif), and Concept Technologies, (Portland, Ore).

Within the last year at least three companies have introduced printers with exotic technologies that will compete with laser printers. Using an ion-deposition process, Delphax Systems' (Westwood, Mass) 60-page/min printer consumes about 5 percent of the power of laser printers. The \$6000 printer with a resolution of 240 x 240 dots/in. is designed for large volume printing tasks requiring 1 to 1.5 million copies or more a month. This printing system integrates the company's 2460 engine with the intelligent capabilities of Digital Equipment Corp's LSI-11 that has specially designed image generation electronics to reproduce standard line printing formats on plain letter-size paper.

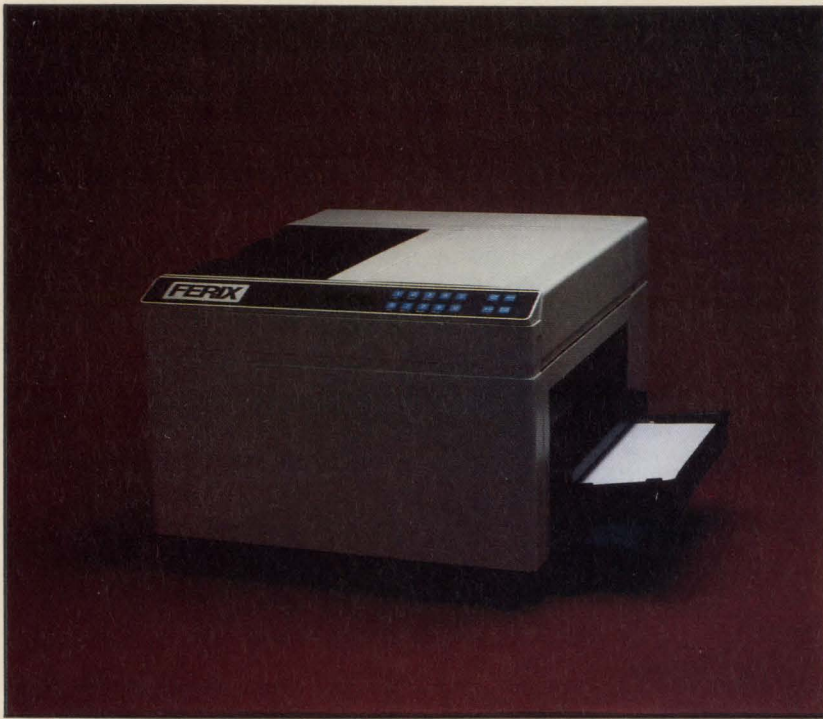
Ion printing uses an ion cartridge to project an array of charged particles on a dielectric drum. Printing occurs through a cold pressure fusing process. Using a single-component toner produces a toner transfer rate of 99.8 percent compared to laser xerography's 80 percent transfer rate, according to a Delphax spokesperson.

Ink-jet printers made an even greater influx this year than in the past. On the low end Hewlett-Packard (Palo Alto, Calif) introduced its 2225 Thinkjet that can print 11 x 12 dot-matrix characters at a speed of 150 chars/s. The \$600 printer accommodates multiple print sizes and supports 11 foreign languages. In addition, with interfaces to the IBM, Hewlett-Packard, Apple, Compaq, Texas Instruments, and other popular personal computers, the system is squarely aimed at personal computer applications.

### Multiple array technology

Arming its ink-jet product with more sophistication, Diconix, Inc (Dayton, Ohio) recently introduced a printer that uses a binary charge, continuous, multiple array technology which allows printing on both sides of the plain paper. Text and graphs can be accommodated at 300 dots/in. resolution and a speed of 18 pages/min. Diconix' multiple array technology is a form of continuous flow ink-jet printing, one of two major methods used today. The other, called drop-on-demand, applies ink drops as needed. While the latter method eliminates this need to recycle ink, drop generation is slow and results in reduced printing speed (see *Computer Design*, Sept 1983, p 147).

Diconix' Dijit 1 supports the needs of host computers and features 128 Kbytes of internal buffered RAM, a resident multipurpose font set, Centronics interface, and Xerox 2700 emulation. Its unique design for duplexing (two-sided printing) turns the paper over for second-side printing. Both sides



A nonimpact office printer for less than \$3000 operates at speeds of 10 pages/min. The printer can be used as a duplicator by printing a master image that has been recorded on the magnetic drum at speeds of 14 pages/min without data retransmission. The patented magnetic thin film head ensures higher reliability and lower supply costs than competing printer technologies.

require the paper to travel as much as 12 ft. The printer sells for \$6000 and will be available in the first quarter of 1985.

Another printer with a fairly new technology sells for half that amount. Ferix' Model 800 magnetic page printer uses a patented, thin film magnetic recording head that prints 10 pages/min. The printer uses an array of magnetic head elements mounted on a flexible substrate to generate concentrated dot images at a resolution of 57,600 dot/sq in. on a magnetically coated drum. As the drum rotates a dry toner adheres to the latent magnetic images which are then transferred to ordinary paper and heat fused to produce the characters (see *Computer Design*, Oct 1 1984, p 44). A unique feature of the printer is its ability to store images on the magnetic drum. Once an image has been created it can be used indefinitely as a magnetic master image in duplicator mode to print at speeds of 14 pages/min without data retransmission.

In the world of plotters, Versatec (Santa Clara, Calif) has developed an electrostatic color printer costing \$98,000 that can output an E-size drawing in 8 min. It can generate 40-in. wide color images of arbitrary complexity on a special print medium which is cycled through the plotter five times to produce a four-color print at a resolution of 200 dots/in. Computer aided design applications are requiring greater plot complexity. Currently plots are generated containing from 8 to 20 million elements—soon to be 40 million elements. An electrostatic

plotter is the only reasonable choice. If such a plotter could draw at 400 dots/in. for half the cost of the Versatec model, it would be ideal. So far Versatec has developed a monochrome plotter that draws 400 dots/in. Its 7435 sells for \$44,000.

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*An electrostatic printer can generate four-color plots with 8 to 20 million elements—soon to be 40 million.*

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In the vector plotter arena—the other major plotter technology—Hewlett-Packard recently introduced an intelligent roll feed unit that can provide drawings up to 12 ft in length. Controlled by a 16-bit microprocessor, the HP 7586B produces precision drawings at 60 cm/s from sizes A to E with a drawing precision of 0.1 percent for any size. Another Hewlett-Packard plotter that is of interest to the design community is the desktop 7550A which can generate up to 99 copies of a plot unattended at a speed of 31.5 instructions/s. With interfaces such as the IEEE 488 and RS-232-C and selling at a price of \$3900, this plotter is a strong contender as a workstation peripheral.

The demand for color printers and plotters brings a need for terminals that can show much detail in color. This, of course, requires that terminals contain as many processing capabilities as feasible



# Where will your network be after the fault?



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The ATTACH network can be configured for complete redundancy. Should one ATTACH subsystem or module fail, users can be detoured around the failed component. On-board battery backup sustains configuration assignments in memory for up to one month.

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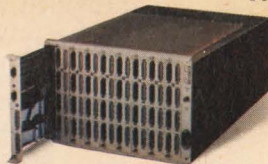
## **ATTACH HELPS MAXIMIZE RESOURCES**

In an ordinary multi-host environment, if one host computer goes down, lots of users could be left sitting idle. The ATTACH network system eliminates user down time, by allowing users to switch to a working CPU, maximizing

human and computer resources.

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CIRCLE 51

without becoming self-contained workstations. Thus, manufacturers are providing local processing power on terminals so that today one can find terminals that feature a high resolution flicker-free display, 60-Hz refresh rates, local intelligence, advanced multiprocessor architecture, numerous local graphics commands, and integrated debugging tools. Depending on the industry that these manufacturers are trying to reach are the amount of functional capability and the type of functions that the terminals contain.

For the engineering community self-contained workstations are becoming common. Such manufacturers as Sun, Saber, Apollo, Hewlett-Packard, and Jupiter Systems have all introduced workstations based on 32-bit microprocessors and some derivative of the Unix operating system. Simple generic terminals are popping up one-a-day just as dot-matrix printers do with a variety for every taste. As such, TeleVideo, the leader in terminals sold through distributors—the most common commerce point for such devices—has recently introduced its model 922 terminal. The Sunnyvale, Calif company pitted its new terminal against DEC's VT200 product line. While code-compatible with the VT220 and the VT100, the \$995 TeleVideo 922 is underselling the two DEC terminals by \$300.

Another type of terminal that is quickly becoming more intelligent is the teleterminal. As the result of the broadening field of telecommunications teleterminals are proving their staying power in three major areas of the communications industry: the Telex/TWX, electronic mail, and data terminal access markets. Their low cost is helping these terminals establish a place in the communications market.



The IBM PC offers a variety of high performance graphics I/O devices. One of these is the Professional Graphics Controller and Display. It can draw up to 256 colors concurrently from a palette of 4096 colors.

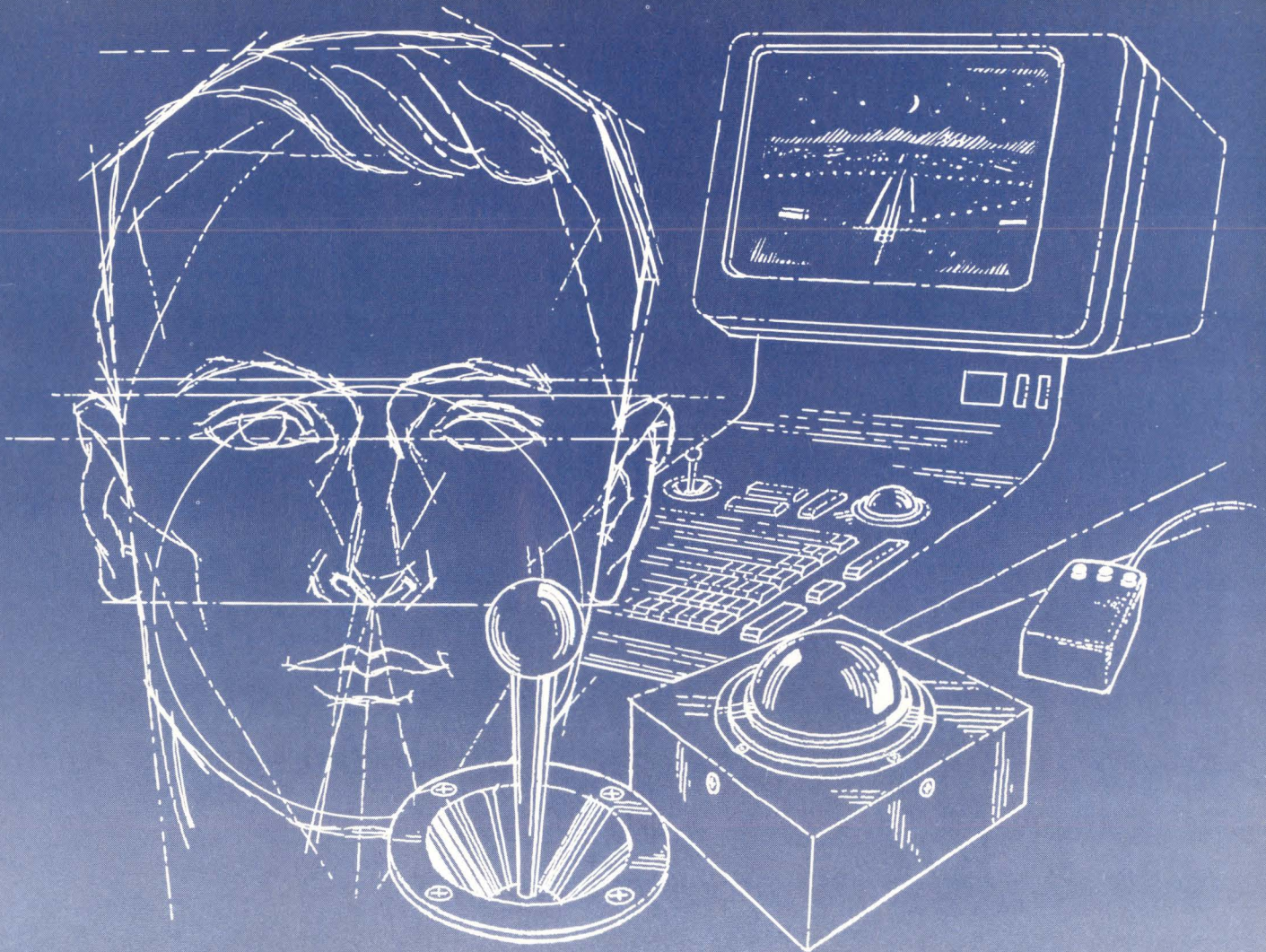
The initial investment is only \$1300 and the operating expenses are low. The offline editing capabilities of teleterminals equipped with intelligent keyboards save online expenses. The user types the message into the unit's memory and edits it before accessing the telephone line. The message may then be directly transmitted or held on the line until more favorable rates apply. Compatibility between terminals is also growing in importance.

One teleterminal—the Whisper Writer from 3M (St Paul, Minn)—can interface to the dedicated TWX or Telex networks providing communications to over 1 million terminals on the worldwide TWX/Telex network. An optional model 1441 Automatic Line Selector interfaces Whisper Writers to both the dedicated TWX network and the public switched telephone network. In addition, the Whisper Writers can communicate point-to-point with each other, as well as access mainframe computers. However, teleterminals lack many of the benefits of a personal computer. For example, the IBM PC has many options that enhance its ability to communicate as a teleterminal.

#### Graphics options for the IBM PC

Recently IBM added two optional graphics boards that make the PC start rivaling some of the more expansive graphics workstations. A Professional Graphics Controller and Display for the XT and AT let the user draw 256 colors simultaneously from a palette of 4096 colors. The display's resolution allows addressing 640 horizontal x 480 vertical pixels. The package costs \$4300. For the less discriminating user the company offers an enhanced color display and controller for \$1370. This card lets users draw 16 colors simultaneously from a palette of 64 colors and can be used on the IBM PC, XT, and AT.

For high performance graphics applications many manufacturers are offering terminal emulators that adhere to the Virtual Device Interface (VDI) standard (see *Computer Design*, May 1984, p 167). IBM has also developed software that makes the IBM PC look like another terminal to be used with mainframes. With the IBM Graphics Terminal Emulator, the PC user gains the attributes of the most popular terminal facilities: the Tektronix 401X and the Lear Siegler ADM-3A terminals. The graphics terminal emulator lists for \$295. Thus, the IBM PC user is provided with access to a variety of graphics I/O devices. While not many companies have implemented VDI or the North American Presentation Level Protocol Syntax, which is the standard for transmitting graphics between terminals (see *Computer Design*, Apr 1984, p 53), IBM's lead into this field should ensure a committed following.



# What kind of operator do you design for your terminals?

When you design a work station, you naturally look for positioning and tracking controls that will permit optimum efficiency, speed and accuracy. Yet, sometimes the most critical link in the entire system is neglected.

The operator.

No matter how good positioning and tracking controls may be, their effectiveness is diminished in proportion to the difficulty in using them. Obvious? Yes. Disregarded? Often.

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We're a leading designer and manufacturer of joysticks, trackballs and control grips. From our beginnings a quarter of a century ago, we've recognized the importance of the human element in successful equipment design. We've spent substantial time and money researching the interaction of man and machine. We've become experts in the human factors in control design.

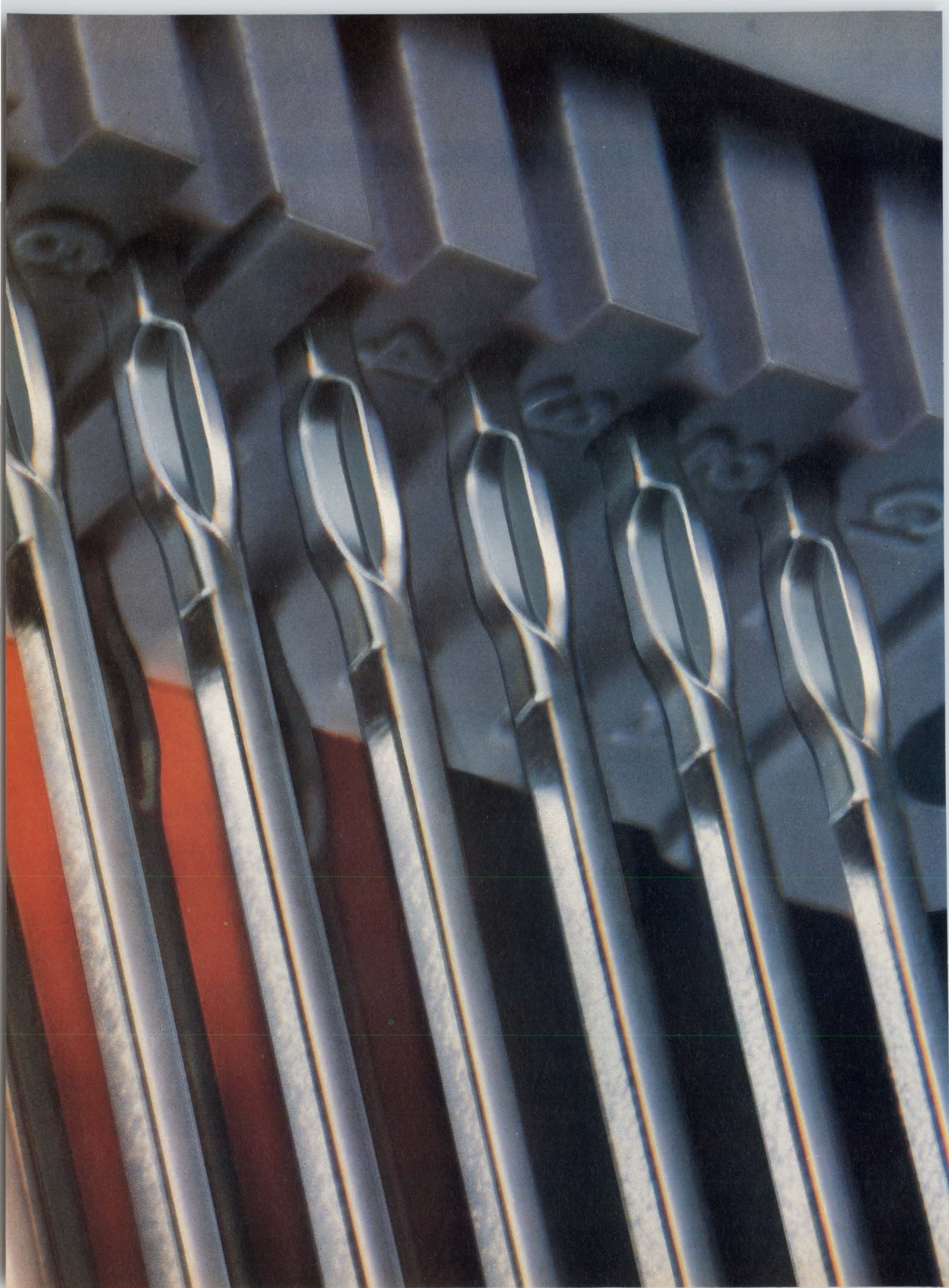
We've put our extensive knowledge to good use. For example, a joystick that's perfect for one type of application is often totally unsuitable for another. So we offer joysticks in numerous sizes and models, each with features suitable for the special requirements of dissimilar applications.

Versatile as they are, if our standard models don't meet your needs, we'll work closely with you to design one that does. If you're designing a system, we'll assist you. Whether your design requires point-to-point positioning, tracking, mapping, processing or something more exotic, we can help.

Nor does it matter to us if you're a Fortune 500 company or a considerably more modest enterprise. You can count on us to respond to your needs with the same enthusiasm and thorough professionalism.

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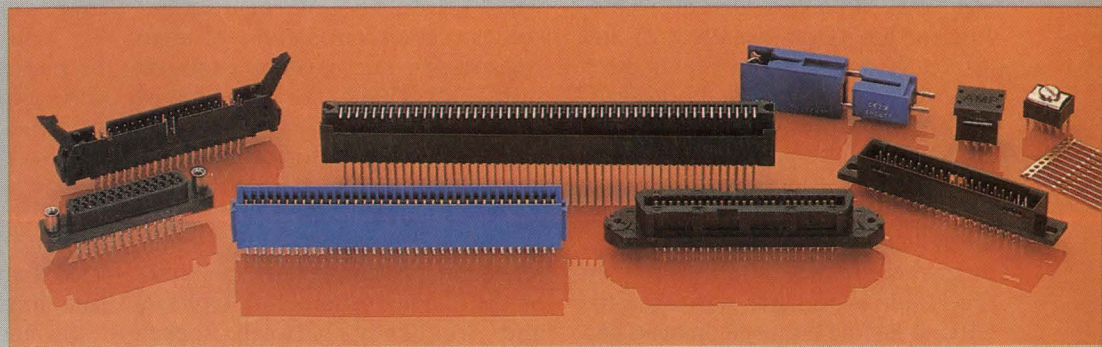
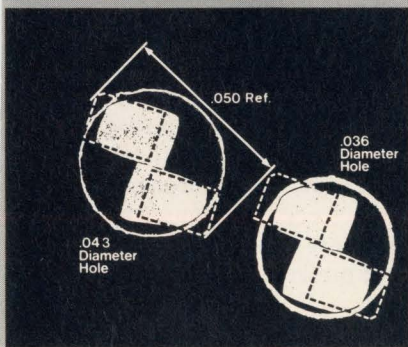
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CIRCLE  
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# AMP means productivity.



Available in a broad range of connector styles, ACTION PIN contacts allow relaxed hole-size tolerances for more economical boards.

## Speech system designed for text-to-speech conversion

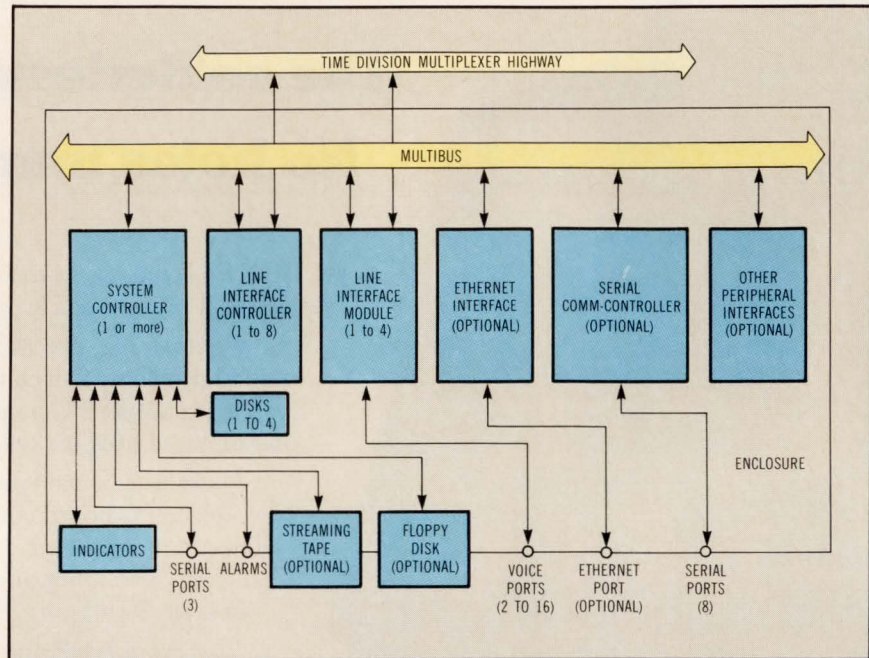
Digital Sound Corp moves closer to integrated voice/text messaging with its DSC-2000 Voiceserver 1 store and forward system. Presently, it is configured to handle voice only, although its 68000-based general-purpose processor and dual Texas Instruments' TMS320 digital signal coprocessors can be programmed to handle text to speech conversion or text alone. Future plans call for incorporating limited speech recognition capabilities for commands and user access, as well as Unix support for any private branch exchange (PBX) based networks.

Such high level integration is beyond the capabilities of current message store and forward systems. Typically, separate systems are needed for voice store and forward and for electronic mail. Common user interfaces tie the two together at the application level. For example, take Digital Equipment Corp's DEC-talk II text to speech system and combine it with a voice messaging system from Voice Mail International.

Less ambitious efforts from Centigram Corp have more in common with their mainframe counterparts than does the Digital Sound system. Their designs focus solely on voice store and forward. These designs also make no provision for text to speech, speech recognition, or general-purpose processing.

Yet, by employing such 16-bit microprocessors and single 5¼-in. rigid disk drives as Digital Sound, Voicemail (from Centigram) and Aspen (from Octel) systems keep costs down to about half those of mainframe implementations offering the same functions. Dedicated voice processing logic and telephone interfaces free the microprocessor to handle system management. In contrast, mainframe implementations rely on the 32-bit processing power of the CPU to handle both system tasks and voice processing. Further complications arise from the need to treat voice information differently from conventional data types.

Still, microprocessor-based voice messaging systems tax the limits of



**The DSC-2000 Voiceserver implements a conventional Multibus system backplane for conventional data transfers and easy expansion, as well as a 32-channel time division multiplexing highway for voice processing.**

speech technology. A problem develops because of contradictory goals. Low overall costs can be achieved only if microprocessors handle the same functions as mainframes. On the other hand, there must be significant digital signal processing to bring sample rates down to 16 kbits/s or less. This will allow microprocessors to process voice information as just another data type.

Unfortunately, there are no easy solutions. Mathematical models, which serve as the voice digitization/reconstruction foundation, fall apart when sample rates go outside their set thresholds. Due to the more general approximation of sampled speech, voice quality deteriorates as noise components are introduced.

Delta modulation, the model most favored by voice messaging systems, relies on high sample rates. It focuses on the changes in amplitude (voltage) and frequency between speech samples (1 bit/s roughly represents one sample). In concept, this method is equal to estimating the shape of a complex curve by taking its first differential (ie, the slope at one point). Distortion increases as fewer samples

are taken (ie, fewer points on the curve). This is due to each sample either over- or undershooting the actual curve. As a result, systems employing this scheme with sample rates that fall below 24 kbits/s, will suffer noticeable degradation in voice quality.

The principal alternative to the delta modulation model is the predictive coding technique. Based on a mathematical model of the human vocal tract and ear, the scheme uses lower sample rates to digitize speech. To achieve this, it fills the gaps between samples with an interpolated curve tying those points together. The principal drawback comes during playback when the reconstructed voice comes out sounding "mechanical." This effect occurs because the inflections that are a part of normal speech are not preserved at the lower sampling rate.

In uncharted territory, vendors must rely on dedicated signal processors (such as the TMS320) for extensive number crunching, or on proprietary algorithms that compensate for deficiencies in mathematical models. At the heart of both

approaches is the fact that the human ear can extrapolate the reconstructed speech and smooth over any gaps. Two examples are the ability to interpret the speech of someone with a heavy accent, and the ability to decipher conversation coming over a bad telephone line.

Based on heuristic (trial and error) algorithms gleaned from research involving thousands of hours of speech samples encompassing gender, age, and accents, both Centigram and Digital Sound have developed proprietary speech algorithms that help the ear smooth over glitches generated by delta modulation techniques.

Centigram reduces voice digitization to 15 kbits/s using only discrete logic components. Meanwhile, by using dual TMS320 digital signal processors, the DSC-2000 Voice-server reduces sample rates even fur-

ther to 9.6 kbits/s. This reduced rate allows voice to be transmitted over conventional data links. Octel's Aspen relies solely on pause suppression to achieve a digitization rate of only 24 kbits/s.

Low sample rates make it easier to use off-the-shelf microprocessors and system backplanes. Centigram dedicates an 8088 to handle system processing, while separate line interface cards handle voice processing and interfacing to an external PBX system. All reside on an IBM PC-compatible backplane.

Digital Sound follows a similar scheme with dual microprocessors: a 68000 to run application programs, and an 80186 to handle supervision of the dual TMS320 signal processors. Both processors, as well as line interface cards, reside on a Multibus backplane. In addition, a separate

time division multiplex highway carries 32 separate channels of voice at 64 kbits/s. It runs between the line interface module, which physically connects to loop trunks or T1 digital carrier lines, and the line interface cards, which actually process the voice. This limits traffic across this Multibus to conventional data transfers. It also bypasses a potential bottleneck, since both voice processing and application processing can also occur concurrently. **Centigram Corp.**, 1362 Borregos Ave, Sunnyvale, CA 94089; **Octel Communications Corp.**, 1841 Zanker Ave, San Jose, CA 95112; **Digital Sound Corp.**, 2030 Alameda Padre Serra, Santa Barbara, CA 93103.

Centigram—Circle 280

Octel—Circle 281

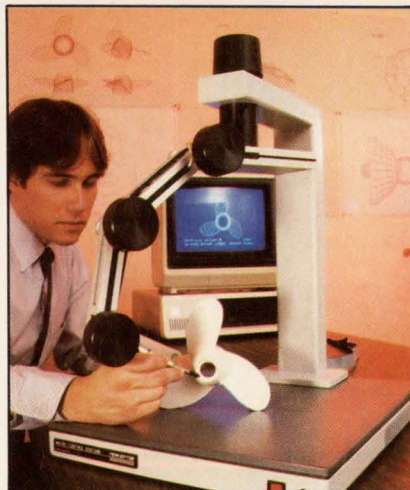
Digital Sound—Circle 282

## Interactive CAD digitizer enters the third dimension

Dubbed an intelligent CAD peripheral that takes advantage of existing software, the Perceptor creates computer models of 3-D objects. Because its handheld pointer moves about the area to be digitized, an engineer can directly convey X, Y, and Z input coordinates—however irregular the physical reference.

Typical CAD workstations conform to 2-D design conventions and contain parts information in a special data base. For instance, X-Y coordinates are input using cursors, light pens, or mice, and a digitizer tablet. Afterward, the Z coordinate is entered through the keyboard or constructed by software.

As an interactive, relatively low cost peripheral, the Perceptor can simplify desktop computer graphics and engineering tasks. Prospective applications include CAD, for creating and modifying 3-D designs under software control. Other applications include analyzing contours, tracing



nested patterns, and modeling complex user-defined surfaces. Moreover, the unit maps fields when sensors for sound, temperature, and radiation replace the standard pointer tip.

Mounted on a ground aluminum reference plate, the digitizing arm captures up to nine X, Y, and Z coordinates per second at 9600 baud. The

arm has five standard joints; a sixth comes with an optional rotational platform. Embedded pots inside each joint convey the electrical information the system needs to calculate rotation angles. Maximum arm reach is about 42 cm.

A Z80A microprocessor board inside the 41- x 46- x 61-cm platform controls electrical data acquisition and converts analog readings from the pots. In turn, the digital signals can be sent over RS-232 interface to any computer that accepts serial input. The processor board also controls digitization modes and rates, baud rates, and calibration. Digitization modes are point, stream, delta distance, and delta time; baud rates are switch and/or software selectable at 300, 600, 1200, 2300, 4800, and 9600. Resolution is 0.018 to 0.025 cm. Price is under \$7000. **Micro Control Systems, Inc.**, 143 Tunnel Rd, Vernon, CT 06066.

Circle 283

## Interactive three-dimensional graphics more than a pipe dream

A workstation now brings the imaginary to reality. Cadtrak's DS-1 architectural design is organized around a bit-addressable pixel memory. This memory holds images with different numbers of colors and presents them to the video monitor via a microcoded frame instruction set resident in the memory itself. This unique design allows smooth virtual panning and zooming at the 60-Hz video refresh rate.

Unlike the conventional double-frame buffering technique used on current raster graphics systems, DS-1 uses a closely coupled multiprocessor architecture that implements parallel data transfers to achieve a design that is totally independent of vector density. The multiple bus structure allows a high degree of asynchronous operation, and a hardware implemented state-machine decodes instruction on how to compose a video frame.

Closely linked to this tightly coupled hardware configuration is

the company's GOS software graphics standard. (For a discussion of graphics standards, see *Computer Design*, May 1984, p 167.) The result is that the user can manipulate a three-dimensional object in a complex model at interactive speeds.

Development of this workstation began in 1981 when company founder Joseph Sukonick sought an application for his technique. "We wanted to find an application that would use smooth panning for easy viewing, and where multiple 3-D images could be simultaneously manipulated in 1/60th of a second," says Dr Charles H. Wells, vice president of business development. "Piping system design was the perfect choice."

The architectural design born of this patented technology is the DS-1, whose 64-bit wide pixel bus transfers information between the parallel processors and the pixel memory at 8 MHz. The video board pulls data from the pixel memory, computes the value of the RGB addresses in the

color map, then outputs RGB signal levels during the video scan.

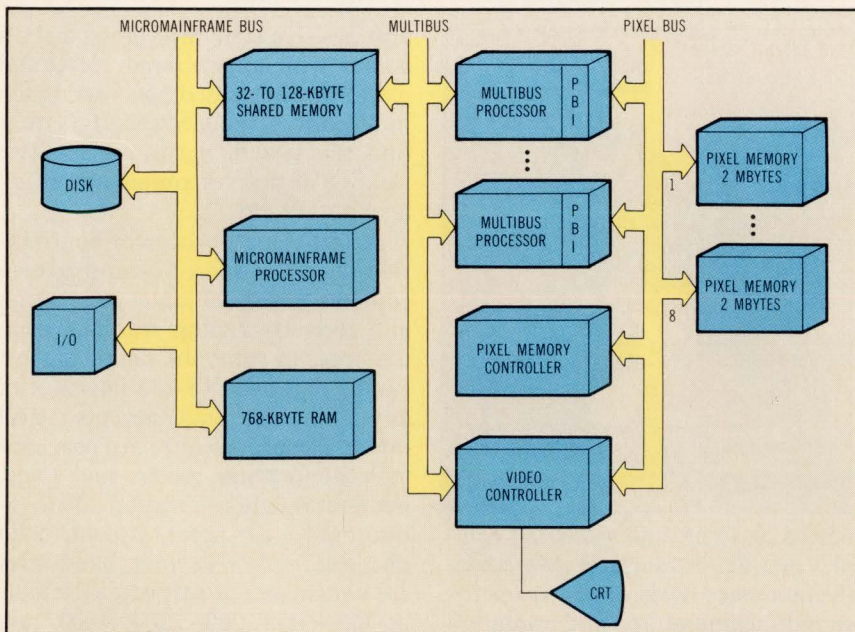
The Multibus provides a means to support parallel processors and possible future enhancements such as array processors. Since the pixel address field is 32 bits wide, a total of 4 Gbits of pixel memory can be addressed. A hardware auto-incrementing address feature eliminates loading the higher word during sequential memory accesses. This allows each processor to move data to pixel memory at 400 Kbytes/s, and to clear memory at 1.6 Mbytes/s.

Each pixel board stores 2 Mbytes of RAM, and up to eight boards can be installed in the station's backplane. This provides 16 Mbytes of pixel storage using 64-Kbit DRAMs. This is equivalent to 13 raster images per board, each holding 660 x 480 x 4 pixels. The pixel memory controller contains a PROM, whose microcoded state-machine performs basic logic operations on pixel memory such as read, write, XOR, OR, and AND.

The pivotal hardware that allows accurate video frame composition is the video board, which converts pixel memory data into RGB signal levels for the color monitor. Composed of random logic devices, the video board implements hardware features that allow multiple viewport displays, over/underlaid grids, alternate grid colors when coincident with data, variable bit/pixel images, variable factor pixel replication, zooming replication blanking, smooth panning, and up to 256 colors.

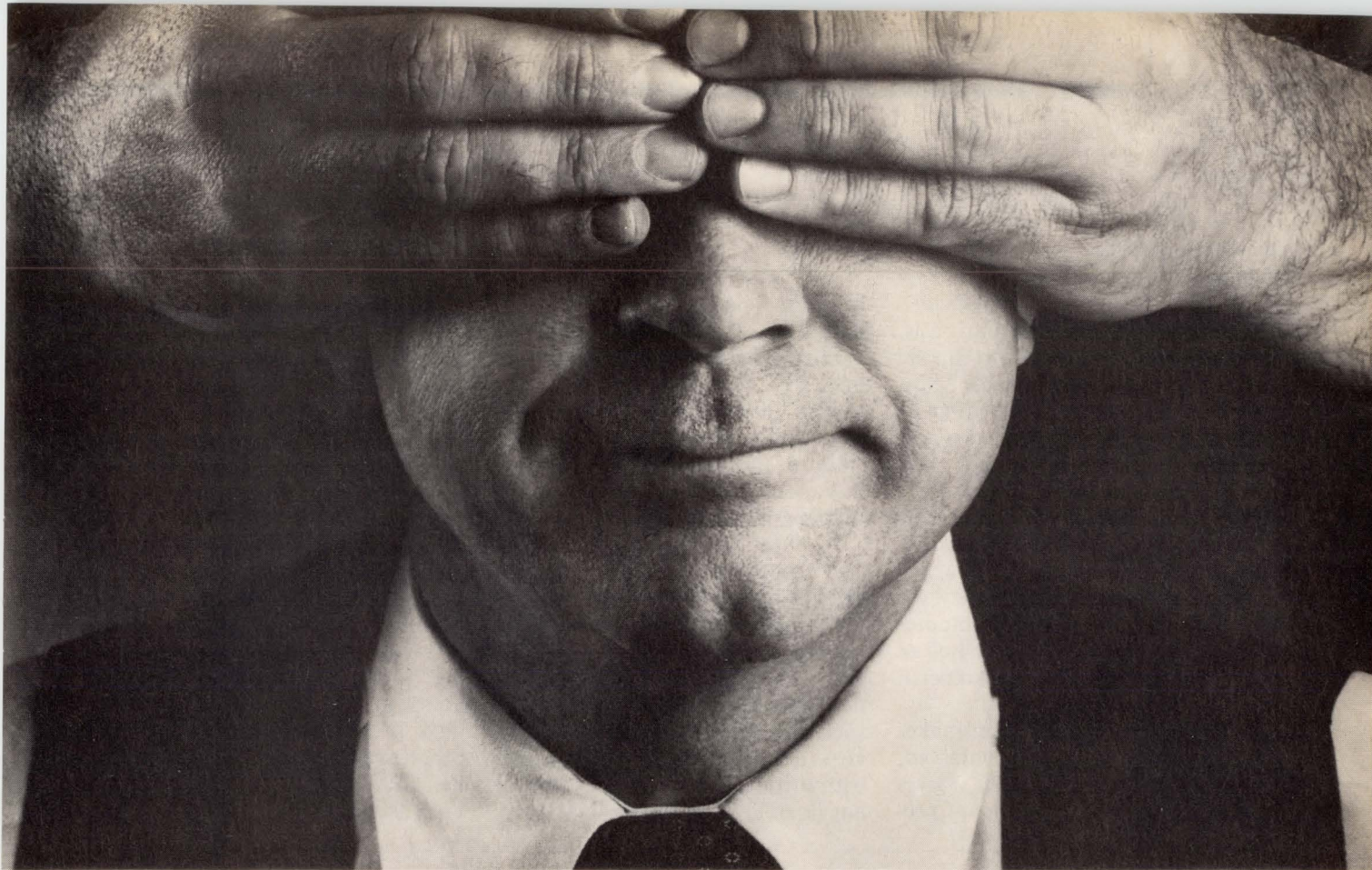
This flexibility is built into the architecture via the microcoded instructions that describe the construction of each video frame. Because each frame (1/60th of a second) is described by a separate table of instructions written by any of the Multibus processors, smooth panning can be accomplished by merely rewriting the instructions for the next frame.

Blocks of pixel information representing instructions or pixel data are  
(continued on page 130)



The workstation performs pipelining operations beginning in the micromainframe processor and continuing in the Multibus processors. Any of the Multibus processors can read/write pixel data or control information into pixel memory. The video controller converts pixel memory information into RGB intensities.





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**CIRCLE 53**

**Interactive graphics***(continued from page 128)*

contiguously transferred to the video board on a first in, first out basis. This enables each viewport to contain differently structured images. Thus, one viewport can have a 1-bit/pixel image, while an adjacent viewport can have a 4-bit/pixel image.

The DS-1 was introduced in early 1983, and Prime Computer Inc (Natick, Mass) was quick to incorporate the hardware and piping application software into its own three-dimensional plant computer aided design (CAD) system. Before DS-1, Prime's system lacked an efficient graphics front end.

The DS-1 software design makes the workstation a self-contained, intelligent graphics computer. It gives the user an arbitrary number of pre-

computed backdrop images of the data base. These images are generated on a host computer and downloaded to the workstation. With their hidden lines removed, they are used as orientation aids, and to provide status of the host resident data base. Enhanced Pascal software supports realtime multitasking.

Applications that require user interaction with a small number of objects in a data base at any one time are mapping, VLSI layout, and space management. Hitachi is interested in DS-1 to help it investigate three-dimensional layout of VLSI chips. In such an application, at least two views are required to provide the user with sufficient visual cues to identify any point in three-dimensional space.

A key aspect in displaying multiple views is a 4 x 4 view definition matrix of floating point real numbers. This matrix describes the transformation for the three-dimensional space to a planar coordinate system, and is sufficient to project the image onto a backdrop view that is generated at any scale factor, position, or window. Typically, a three-dimensional application designer uses multiple views to position objects in space. For interactive piping applications, a four-view plan with the top representing North, elevation views looking South and West, and an isometric view is sufficient to visualize the problem in real time. **Cadtrak**, 823 Kifer Rd, Sunnyvale, CA 94086.

Circle 284

## Graphics system functionality swells with million addressable points

Designed for a wide-range of engineering and scientific work, the 5080 graphics system produces precise, highly detailed displays. The compact system has a display, a graphics processor, a channel controller, and auxiliary software and peripherals.

The 5085 graphics processor performs a variety of graphics operations. These include high speed vector-to-raster conversion, polygonal area fill, circle generation, and two- and three-dimensional scaling transformations (scaling, clipping, rotating, and translating). A user can replace display images instantaneously with no screen blanking between images—an ideal feature for animation. An option allows a user to switch quickly between graphics mode and 3270 mode for network and database access.

Model 5081 display can simultaneously show up to 256 shades of gray. A color model displays up to 256 colors from a 4096-color palette. The noninterlaced raster unit refreshes the 1024 x 1024 addressable points on the screen 50 times per second. This rate results in a steady,

bright, and clear image. To help reduce distortion, the tube face is cylindrically shaped with contrast-improving, antiglare treated glass. For the user's comfort, the model 5081 display can tilt 5 degrees forward and 15 degrees backward.

Shared between host channel and 5085 and/or 3255 control units, the high speed 5088 channel controller attaches to a System/370, 43XX, or 30XX channel. Speeds range up to 2.5 Mbytes/s in data streaming mode, and up to 1 Mbyte/s in conventional channel mode.

The primary device for system interaction is the 5083 tablet. With either its mouse-like cursor control device or a stylus, the tablet digitizes drawings or emulates the operation of a light pen. The thin, flat-surface unit weighs 6.5 lbs and features a palm rest and height adjustment.

The graphics access method/system product release 2 (GAM/SPR2) supports current 3250 functions and



a full range of advanced functions under VM/SP, MVS, and MVS/XA. Other software allows users to examine surfaces in detail, highlight changes in color, and display designs for structural analysis.

Peripherals include an alphanumeric keyboard, a lighted program function keyboard, a tablet with either stylus or cursor control device, and a dial unit. All devices attach to the processor through connections in the display's base. **IBM Corp, Information Systems Group**, 900 King St, Rye Brook, NY 10573.

Circle 285



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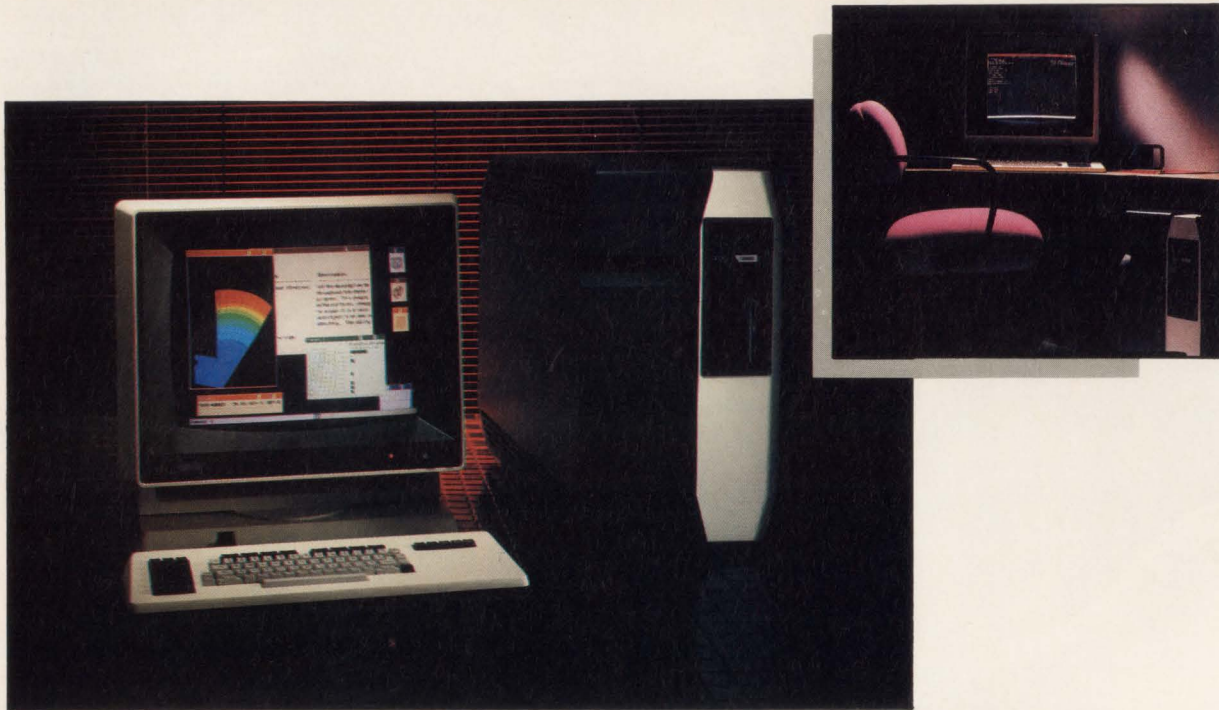
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## Workstation graphics architecture lightens programming load

Compatible with Apollo's entire family of workstations and software, the DN550 color graphics workstation is 68010 based. The unit features a dedicated bit-slice graphics processor, a 1024 x 800 resolution color monitor, and a low profile detachable keyboard. Touch pad and/or mouse are available as options. The system offers up to 3 Mbytes of main memory and up to 2 Mbytes of double-buffered display memory that boasts 256 simultaneous colors.

The Graphics Metafile Resource (GMR) is a graphics architecture for the entire Domain workstation family. It combines graphics capabilities with high graphics throughput and accommodates emerging standards such as the Graphical Kernel System (GKS), the Programmer's Hierarchical Interactive Graphics Standard (PHIGS), and the Virtual Device Metafile (VDM). GMR integrates a graphics data base with advance display routines in one package.

At the heart of the GMR architecture is the graphics metafile—a tree-structured data base that can be edited. This architecture stores graphic entities in the metafile, allowing information to be shared among applications and viewed on any workstation in the LAN. Built for speed, the virtual file stores up to 256 Mbytes of data directly in world coordinates, while the package uses

its graphics hardware to increase throughput whenever possible.

Data in the metafile is displayed in multiple viewports within a given window, with the GMR handling scaling, translating, windowing, and clipping. Changes are reflected in all viewports at the same time. Attributes can be associated with viewports or instances to control a range of display parameters including color, line style, and fill pattern. The creation of a printable bit-map of a metafile simplifies hardcopy generation.

The segmented data base supports nesting and instantiation. Nesting allows segments to contain other segments. Instancing reduces storage requirements for repetitive data. Segments can store nongraphics data or reference data in other files.

Designed with a full 32-bit internal architecture, the unit's dedicated bit-slice graphics processor, together with extensive microcode, provides fast 2-D operations and more than a 10,000-transformed clipped vector/s throughput. In addition, the unit offers more than 1-million pixel/s vector draws and 25- to 35- million pixel/s area fill and bit-block transfers. The system provides circle, arc, and spline generation with user-definable area fills and vector patterns.

With flicker-free color graphics and a multiwindow, multitasking environment, the unit allows up to 24

concurrent processes with 16 Mbytes of virtual address space/process, as well as an integral interface to the 12-Mbit/s Domain LAN. More communication support comes in the form of IBM 3270 emulation, HASP, X.25, and an Ethernet gateway. Ergonomic features of the 19-in. display include tilt/swivel a nonglare filter.

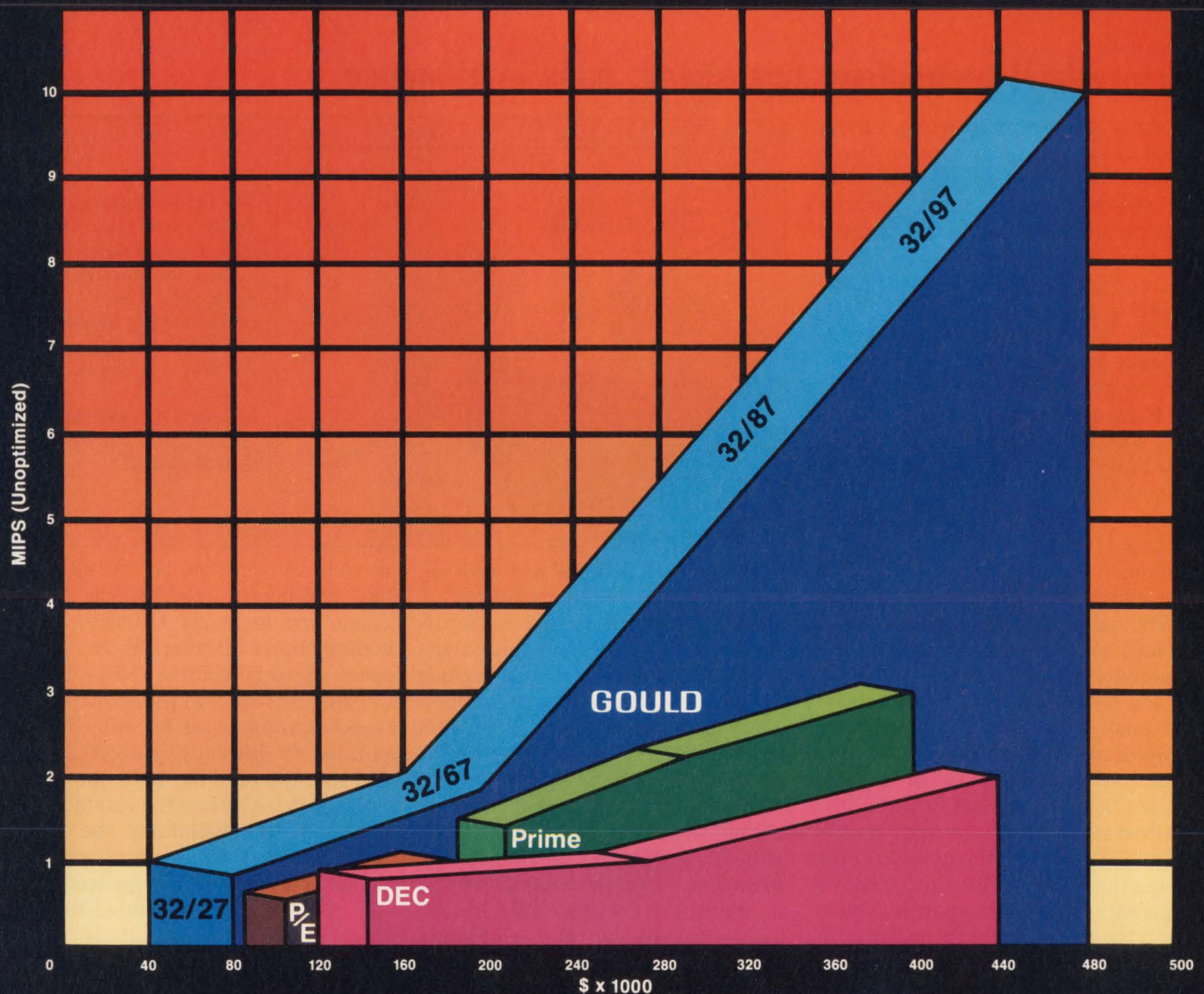
Other software includes D3M, which is a distributed database management system, SIGGRAPH Core nongraphics package, Fortran 77, ISO Pascal, C, and Lisp programming languages, as well as professional support packages. A package for the software engineering environment increases productivity in development, maintenance, and administration of software projects. In addition, terminal emulators, a font editor, and a high level debugger are available.

Options include a 50-Mbyte, 5 1/4-in. Winchester, a 45-Mbyte, quarter-inch cartridge tape unit, a four-slot Multibus peripheral adapter, and a floating point hardware accelerator. Configured with the Aegis operating system, the DN550, with 1 Mbyte of main memory, 4 planes of color, monitor, keyboard, and Domain LAN interface is priced at \$31,500; \$40,000 with a 50-Mbyte Winchester. **Apollo Computer Inc**, 330 Billerica Rd, Chelmsford, MA 01824.

Circle 286

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## Printwheel technology ups speed, adds intelligence

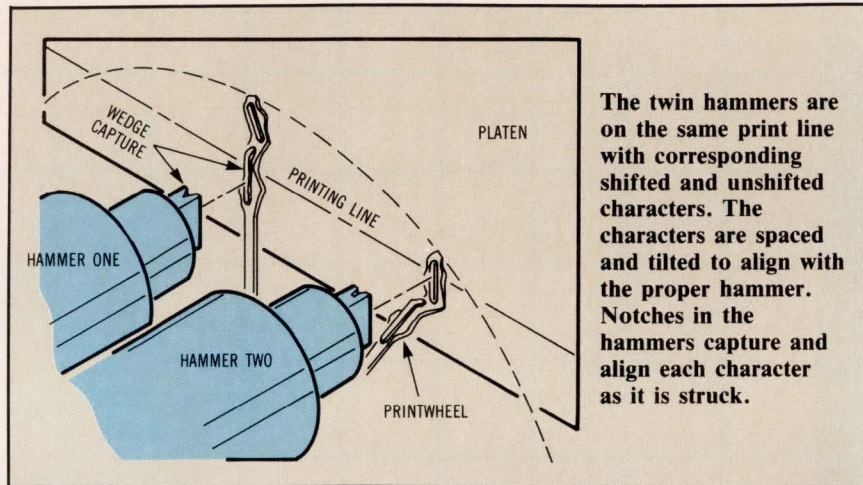
A daisy wheel printing technology by Diablo Systems greatly reduces parts count, yet preserves the ability to print a 200-char extended character set on a single printwheel without shifting the carriage. In addition, the technology packages the plastic printwheel in a snap-in cartridge. This cartridge is encoded to let the printing system recognize the currently inserted printwheel.

Extended character set (ECS) printing without physical shifting is done by using a dual-hammer technique. One hammer is used to print characters on the printwheel's outer circumference, while the second hammer strikes only those found in the inner circumference. The hammers themselves are aligned with the print line, but the characters have a unique arrangement.

For example, the unshifted version of each character is located nine spokes ahead of its shifted counterpart on the wheel. When a given spoke is in the vertical position, the shifted character (in the inner ring) is aligned with the first hammer. At the same time, its unshifted (eg, italic or alternate font) counterpart is aligned with the second hammer on the print line, but ahead of the first hammer's position on the paper.

The characters on the outer ring are tilted with respect to the line of the spoke. This ensures that they are upright on the print line when aligned with the second hammer. A firmware algorithm examines the line buffer in the printer to determine if a given character is to be printed by the first or second hammer.

Since the entire line is buffered before it is printed, characters can be arranged in the order that they will actually be struck as the printing mechanism moves across the platen. They do so with notation as to whether they will be struck by hammer one or two. As a result, some characters may be struck as far as nine print positions ahead of a pre-



The twin hammers are on the same print line with corresponding shifted and unshifted characters. The characters are spaced and tilted to align with the proper hammer. Notches in the hammers capture and align each character as it is struck.

vious character. But, all such gaps are filled in as the line is completed.

The printing technique incorporates several methods of improving speed and accuracy. These include position encoders and a closed-loop stepper motor for the printwheel mechanism, and wedge capture for the hammers and spokes. Wedge capture uses small wedge-shaped pieces behind the characters on the wheel, with corresponding notches on the hammers. When the hammer strikes, it captures the wedge. This ensures exact positioning and eliminates minute position variations caused by the settling of the wheel's motion, or by vibration.

The use of a closed-loop stepper motor for the printwheel mechanism allows a more precise calculation of wheel position (from information provided by the encoders), as well as a calculation of acceleration and deceleration energies. In addition, the combination of dual-hammer technology, wedge capture, and the closed-loop stepper can greatly increase throughput by printing on-the-fly. As the printwheel mechanism moves across the platen, information from its position encoders is used with that from the printwheel to fire the hammers.

Since there is no physical up and down shifting of the printwheel

mechanism, motion can be smooth and continuous. Mechanical parts count and mass are reduced. This combination of factors allows a print speed up to 80 chars/s (55 typical).

Estimates are that the basic printwheel technology can be easily incorporated in low cost printers with end-user prices in the \$500 range. In order to demonstrate the technique's full range of possibilities, the company has built it into a new printer designed for networking applications. The 80IF printer is intended to run largely unattended and is thus equipped with various automatic and communication features.

The 80IF has a dual-bin sheet feeder with an envelope feeder, and a long-life ribbon. It can be equipped with multiple buffers or a 64-k optional spooler. Moreover, its communication capabilities let a remote user query the printer's status and select options to the same extent they could be selected onsite by using the front panel. Integral to this is the encoding present on the printwheel. The encoding enables users to see what they have, to send an operator alert to change the printwheel, or to handle malfunctions not easily resolved from a remote site. **Diablo Systems**, 901 Page Rd, PO Box 5030 Fremont, CA 94537.

Circle 287

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## A single-user solution for CAE/CAD/CAM

The CDS 3000 series of intelligent 32-bit workstations handles schematic capture, two-dimensional drafting and dimensioning, and technical publications—all in a single-user, desktop package. The nongraphics applications include spreadsheet generation, word processing, and electronic mail.

Based on the 68010, the 3000 employs virtual memory Unix enhanced for CAE/CAD/CAM applications. Supported programming languages include Fortran 77, C, and Pascal, as well as standard utilities.

All series workstations incorporate CADDs Access, enabling a user to log on to an existing CDS 4000 or 5000 series system. Connections are point to point, or via a modem. This connection permits access, display, and manipulation of CADDs 4X commands, files, and data bases. CADDs 4X, the latest version of the company's multi-user, multitasking

software, provides the basis for an integrated graphics data base. Processing, retrieval, and storage take place on the host system, ensuring file and database integrity.

The systems communicate with each other, with other CDS systems, and with mainframes through industry standard protocols. With a shared resource manager and Ethernet software, the workstations can be clustered in multi-user networks and linked to central peripherals.

All workstation configurations include as standard the 68010 with 2 Mbytes of main memory, Unix, a Multibus chassis, and graphics unit. The graphics unit provides a high resolution (900 x 1152 pixels), 19-in. monochrome display and controller, low profile keyboard, and mouse. Optional features include additional memory, an FPU, peripheral units, and communication links. Several application packages are available to



complement current CAE/CAD/CAM capabilities now on the system. Schematic Capture/ 3000 produces logical block diagrams and electrical schematics, as well as permitting on-line design rule checking. An optional logic design simulation package is also available.

The Drafting/3000 software gives high productivity in layout design, detailing, and dimensioning. It uses dual English and metric dimensioning, standard parts libraries, and a graphics programming language.

Prices for the workstations range from \$35,000 to \$52,000. **Computer-vision Corp.**, 100 Crosby Dr, Bedford, MA 01730.

Circle 288

## Color and monochrome terminals draw with megapixel speed

HiScan Graphics terminals apply high speed CMOS to low cost graphics displays. Based on dual-processor architecture, the terminals include a proprietary graphics coprocessor, and HiScan Graphics technology. This technology provides a faster graphing speed and more industry standard terminal emulations than comparably priced terminals. The 4210 is based on DEC's VR201 monitor and a VT200 keyboard; the VR241 color monitor and the same keyboard make up the 4205 terminal. All are compatible with DEC and other peripherals.

Image quality considerations are fundamental to terminals. In both terminals, image quality is increased with a high line rate noninterlaced display that is nonsmearing and flicker free. To further enhance image quality, the monochrome display offers an 800- x 600-pixel resolution—the color monitor provides 800 x 300 pixels. The terminals support 80- and 132-col formats with characters formed on a 10 x 20 cell.

By incorporating multiple bit-mapped memory planes, the monochrome terminals offer a four-level gray scale (using two memory planes). With four memory planes, the color terminals can simultaneously display 16 colors out of a 64-color palette.

Integrated architecture uses the bit map to display both text and graphics. The text features include a plain language setup menu displayed in

English, French, or German, downloadable character fonts, and 15 programmable function keys. Support is provided for TEK 4027 or 4105 and DEC ReGIS protocols, as well as standard DEC VT220 text and TEK 4010/4014 graphics functionalities.

To achieve graphing speeds of 1 million pixels/s, the terminals use a specially designed graphics coprocessor that works with a Z8002 16-bit microprocessor. The coprocessor handles all graphics processing tasks while general-purpose calculations are delegated to the Z8002.

The graphics processor consists of three main elements—one for graphics processing, one for read-modify-write, and a CRT controller. These elements, together with the Z8002 in a pipeline architecture, are responsible for the megapixel rate. The monochrome terminals are costs \$2195 each; while the color terminals are \$2995 each. **Digital Engineering, Inc.**, 630 Bercut Dr, Sacramento, CA 95814.

Circle 289





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\*Cost comparison (250 ft extended distance data cable)

#### Data Cable

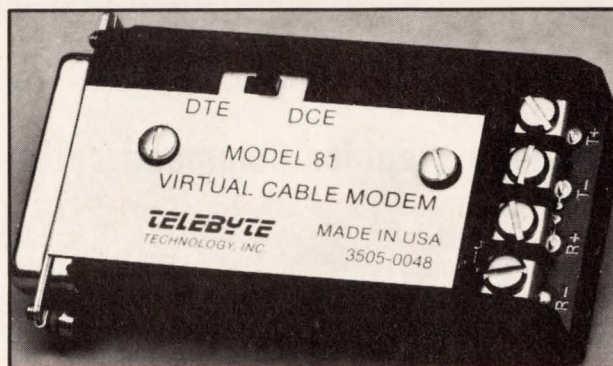
Cable cost = \$ 20 + .80/ft  
(250 × .80) + 20 = \$ 220

Maximum baud rate = 9600

#### Model 81

Modem cost = \$ 77  
Twisted pair (2) @ 500ft = \$ 30  
(2 × 77) + 30 = \$184

Maximum baud rate = 19,200



**TELEBYTE**  
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Halesite, New York 11743  
(516) 423-3232  
TWX 510-226-0449  
A Public Company

## VDT offers low cost programmable features



The Freedom 200 offers a long list of features in one package. Consisting of a 12-in. display and a detachable keyboard, the terminal's points of interest range from a nonglare screen to setup modes and programmable functions keys.

The CRT uses a 24 x 80 display format. The 25th line is user accessible for status or other information. A full tilt (+ 15 degrees, - 5 degrees)

and a full swivel (70 degrees) console houses the etched green phosphor display screen.

In native mode, display memory is one page with the second page optional. In emulation mode, memory reaches two pages with additional pages optional. The unit emulates both the TeleVideo 950 and the Lear Siegler ADM 31 terminals.

Advanced video features include non-embedded character attributes. In visual mode these are normal, reverse, half intensity, underline,

blink, and blank. In data entry mode they include protected, alphanumeric, alpha only, numeric only, and extended numeric.

Jump or smooth scroll is available. Smooth scroll is programmable with rates of 2.5, 5, and 10 lines/s. The user can scroll certain parts of the screen by defining a scrolling region.

Four communication modes are provided: block, conversation, moni-

tor, and local. Block can be immediate or deferred and sent from command. Conversation mode transmits half and full duplex. Monitor mode displays control codes in programming applications, while local mode operates standalone.

The detached, low profile keyboard clusters 106 sculptured keys into functional groups. Twenty programmable function keys (using the shift) produce up to 256 Kbytes of code sequences. These keys can also send 20 preprogrammed default sequences. The 11 cursor control keys assume an inverted "T" format. In addition, there are nine editing keys and 12 functional command keys.

Handshaking protocol is X-on/X-off with programmable characters and DTR. Fifteen transmission rate selections range from 50 to 19.2 kbaud. Parity choices are even, odd, or none, with word structure at 7 or 8 data bits with 1 or 2 stop bits.

Interface is via EIA RS-232-C. **Liberty Electronics**, 625 Third St, San Francisco, CA 94107.

Circle 290

## Low cost plotter combines graphics command set and offline operation

To meet the demand for multiple color, low cost graphics plotting, Enter Computer is producing a six-pen plotter at an end user price of \$1095. The Sweet-P 600, or "Six-Shooter," can store six fiber-tip, Rapidograph-type, or ball-point pens in a rotating carousel for six online colors. Additionally, these carousels can be switched to provide several palettes for writing on either paper or acetate sheets.

The Sweet-P 600 takes either 8½- x 11-in. or 11- x 17-in. paper. The pen moves along a single axis, the X-axis, while the paper is moved back and

forth on the Y-axis by gripping rollers. The smallest addressable increment is 0.004 in., and maximum plotting speed is 14 in./s. Repetition accuracy for any given pen is the minimum step size of 0.004 in., while repetition accuracy from pen to pen is two step sizes, or 0.008 in.

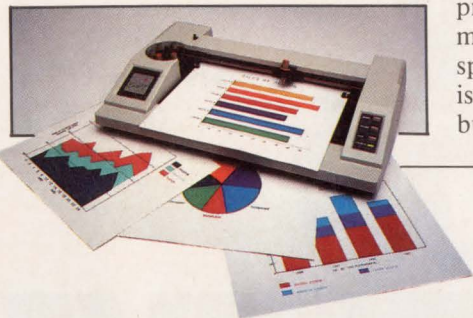
Among the techniques that have enabled this degree of accuracy at a low cost is the use of stepper motors controlled by a microprocessor using ROM-based microstepping routines. The 600 also contains 19 internal character sets, including katakana, and a Sweet-P graphics language

(SP/GL) command set. The command set includes line, curve, and point drawing; axis and tick drawing; and routines for drawing and filling rectangles and wedges.

The Sweet-P 600 is also compatible with the Hewlett-Packard graphics language (HPGL) so that software written for the HP 7400 series plotters can also run the 600. In fact, a considerably large body of software packages from over 25 independent software vendors to run the Six-Shooter on a variety of computer systems including Texas Instruments, IBM, Digital Equipment Corp,

Wang, Apple, and a variety of MS-DOS and CP/M systems.

The Six-Shooter has both RS-232 serial and Centronics-compatible



parallel interfaces and can be used in an "eavesdropping" mode for a multi-user environment. There, it is placed between a microcomputer and printer or between a terminal and a mainframe, and performs tasks when specifically instructed to do so. This is made possible by the 2-Kbyte buffer supplied or by using the

optional 8-Kbyte buffer to download tasks. Even in a single-user microcomputer environment, the plotter can operate without tying up the computer resources, except to receive additional downloaded tasks. **Enter Computer, Inc.**, 6867 Nancy Ridge Dr, San Diego, CA 92121.

Circle 291

## Sophisticated graphics controller draws fast response time

Model One/80 outfits general purpose 32-bit computer systems with the electronics to develop sophisticated graphics applications. At an attractive cost/performance ratio, the controller's prime applications span from computer aided design/engineering, architectural drafting, and computer animation to land resource analysis. Prices for a basic configuration, including monitor and keyboard, start at about \$20,000.

To the host computer, the controller looks like a high speed peripheral. It supports 1280 x 1024 resolution with 8-bit planes of image memory, furnishing 256 colors from a palette of 16.7 million. Moreover, 60-Hz noninterlaced refresh and pixel updates as fast as 8.7 ns/pixel combine with other features to provide interactive three-dimensional modeling and simulation.

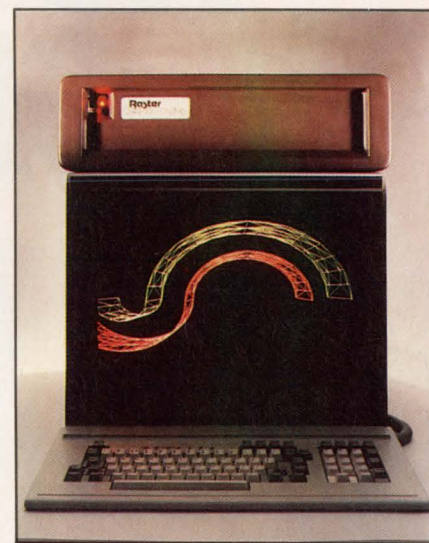
The system draws up to 70,000 one-centimeter random vectors/s. Onscreen, a local programmable window clips vectors at the full draw rate. In double-buffered mode, the bipolar processor has total access to image memory, thereby allowing a vector draw rate that approaches 115 million pixels/s.

Bipolar processor and proprietary VLSI hardware accelerators directly execute most common graphics functions—such as move, draw, fill/unfill area, and transfer pixel image—with minimal host intervention. Vector-defined text can be generated in vertical and horizontal formats. Both formats rotate in one-degree increments and scale from 8 to 256 pixels independently in X and Y.

An 8-MHz, 16-bit microprocessor controls serial I/O and local programming facilities. This tightly coupled unit comes with 96-Kbyte PROM and 32-Kbyte RAM for instruction set, local macro programming, and interactive debugging. A resident command interpreter tests and executes graphics sequences without a host.

Integrated DMA interface conforms to industry-standard specifications for fast image and command transfers to DEC's PDP-11 and VAX families, as well as systems from Data General, Perkin-Elmer, Prime, IBM, and Gould/SEL. Four serial ports at up to 38.4 kbaud are standard.

With an I/O subsystem that accepts data at up to 6 Mbytes/s, the Model One/80 can be closely coupled to a



host for I/O-intensive applications. System commands include CORE and GKS functions, as well as standard primitives; application software is compatible across the entire Model One family. All controller electronics come in a 5.25- x 17- x 21-in. (13.34- x 43- x 53-cm) rackmount box that weighs 50 lb (23 kg). **Raster Technologies, Inc.**, 9 Executive Pk Dr, North Billerica, MA 01862.

Circle 292

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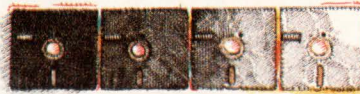
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ENVIRONMENTS MEAN  
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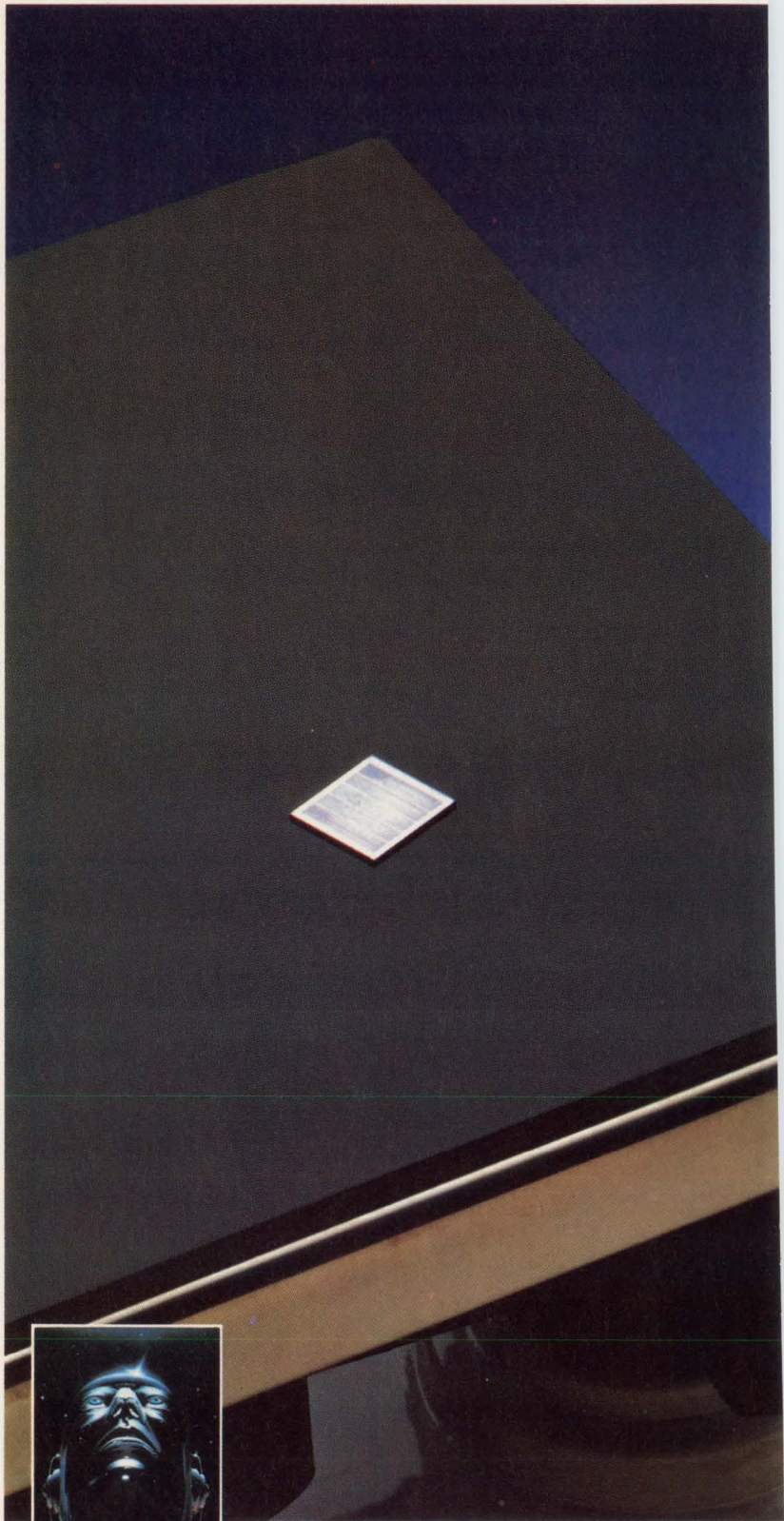
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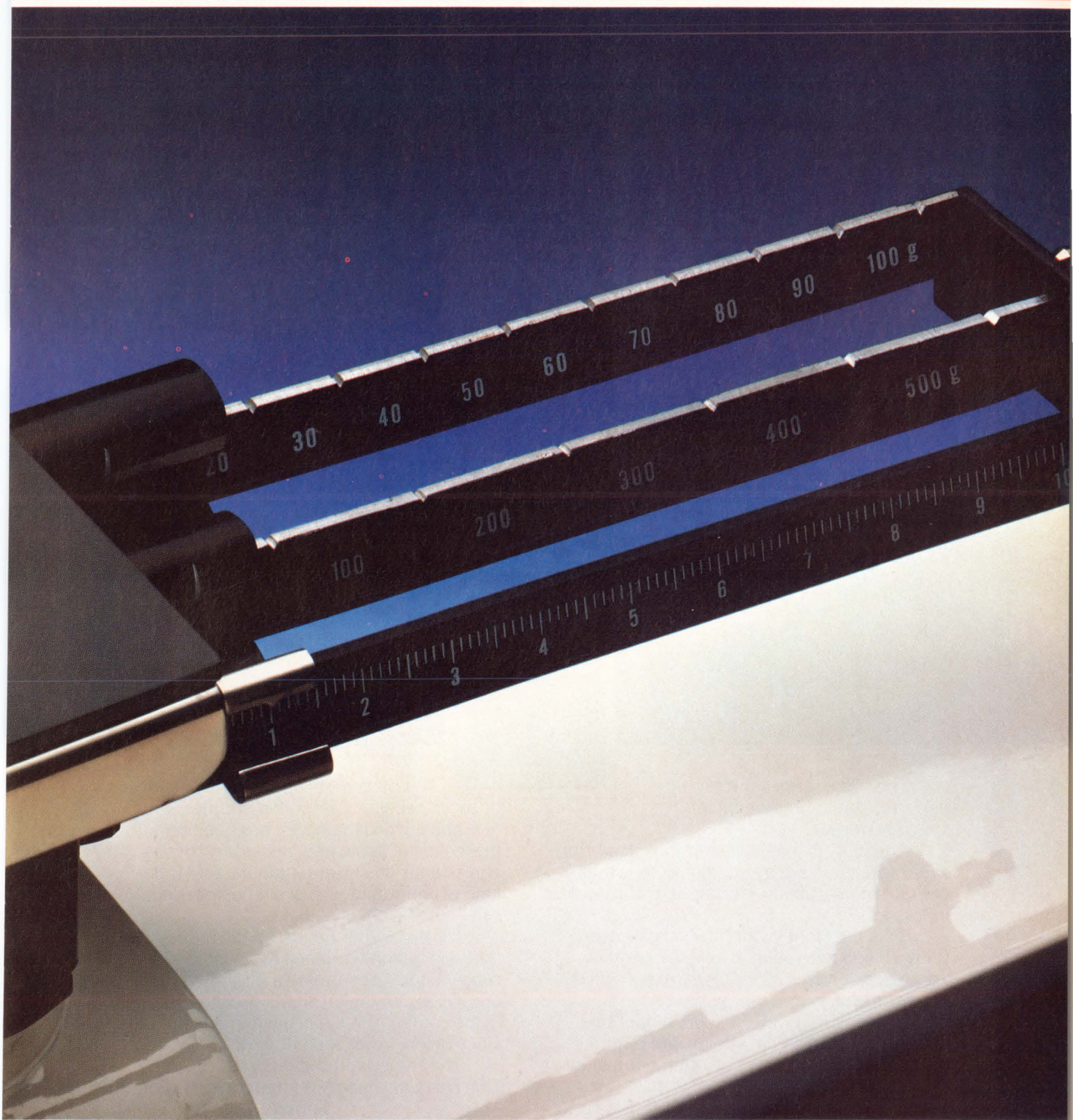
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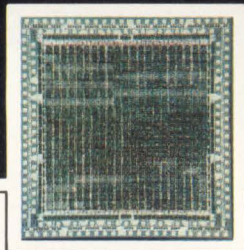
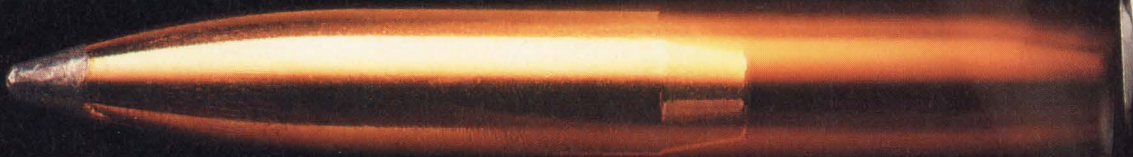


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# CMOS SETS PACE FOR CHIP DEVELOPMENT

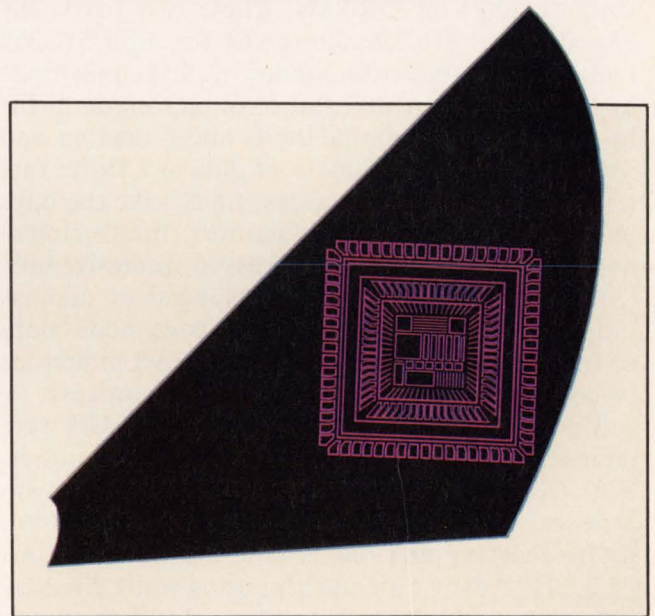
The leading edge of technology for VLSI ICs is now CMOS. Next-generation memories, micros, and application-specific ICs will use the technology extensively.

by John Bond,  
Senior Editor

During 1984, the direction of semiconductor technology became clear. CMOS took its place as the mainstream high density process for memories, microprocessors, and application-specific ICs. Digital gallium arsenide technology began to look like a winner for very high speed applications, but it is only at the beginning of a long growth period. On the other hand, CMOS is rapidly maturing into the major silicon technology. As CMOS is scaled down in size, not only does circuit density increase but the chips run faster—outpacing NMOS and even many bipolar circuits. As a result, every major semiconductor manufacturer has its latest designs or its plans for the next generation in CMOS.

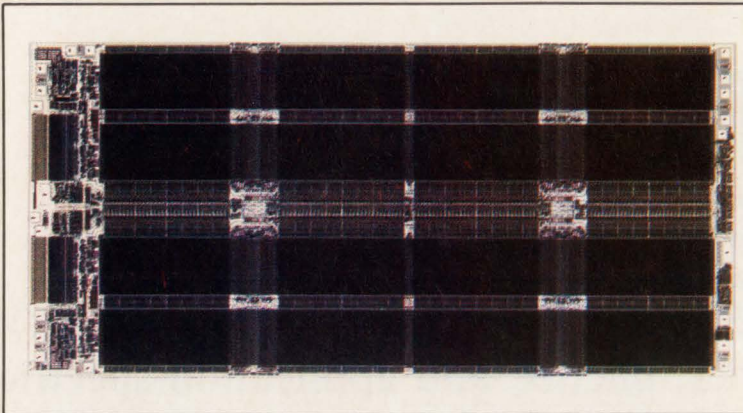
## Mass market ICs

Although there has been major growth in application-specific ICs, it is the growth in memories, microprocessors, and other high volume ICs that fuels the merchant market IC producers. This year was pivotal in the development of memory technology and this is a gauge of each company's process sophistication. The 256-Kbit dynamic RAM (often in CMOS) appeared on the market and descriptions of 1-Mbit designs (always in CMOS) began to show



up at technical conferences. Perhaps an even more important development, spurred by the 256-Kbit DRAM and started with 64-Kbit DRAMs, is the trend toward alternate organizations. Consequently, byte-wide and 4-bit wide chips may turn out to be as common as the by-one organization. Even "by-nine" schemes to allow a parity bit are beginning to appear, in recognition of the way computer memory systems are often designed.

DRAMs remain at the leading edge of semiconductor technology (in process, not circuit complexity). As a result, a semiconductor company may spend



The Intel 51C256, 256-Kbit DRAM is built in the company's CHMOS process and uses ripplemode for faster access time.

\$100 million to develop and manufacture a product that soon becomes a commodity, with all the cut-throat price competition that entails. To offset this, many companies have staked out memory market niches or added unusual features to standard dynamic or static RAMs while maintaining industry compatibility.

Intel (Santa Clara, Calif) took the latter approach with its 256-Kbit DRAMs. These two parts, the 256-K x 1-bit 51C256 and the 64-K x 4-bit 51C259 feature high bandwidth modes. Called ripplemode in the by-one part and static column mode in the by-four device, these methods allow reading and writing of successive blocks of data at a faster rate than the normal per-bit access time. Like the page mode used by other manufacturers, Intel's ripplemode provides continuous access to successive bits. Unlike page mode, it uses lookahead or address pipelining that makes it faster than page mode. Both of Intel's high speed access modes are serendipitous by-products of the high speed CMOS process.

Many of the NMOS circuits on a DRAM were designed with dynamic circuitry to conserve power. With CMOS these circuits can now be designed with a faster static circuitry. The static design requires no precharging and reduces the overall cycle time of the DRAM. Consequently, using static circuitry for column address decoders provides fast column address access and cycle times to permit ripplemode or static column mode.

### Special-purpose memories

Examples of special-purpose niche memories are those useful for high performance video systems such as the Synertek (Santa Clara, Calif) SY2131 dual-port RAM and the Texas Instruments (Dallas, Tex) TMS4161 multiport video RAM. The TI part is particularly interesting because it can be mated to a video system controller (VSC) chip that allows unified text and graphics under one bit-mapped ap-

proach. Besides functioning as a raster-video controller, it generates the special shift-register loading and updating control signals required by TMS4161-based systems.

The VSC permits the host computer to access video memory 95 percent of the time by performing screen refresh while simultaneously updating data in video memory. Although the VCS will control conventional 64-Kbit and 256-Kbit DRAMs, its design extracts the maximum performance from the TMS4161. This combination effectively doubles the system by eliminating half of the memory cycles usually required to refresh the display. The TMS4161 incorporates one port for random access. It contains four cascaded 64-bit internal shift registers that output at 25 MHz via a fast serial port. Data can be written into the RAM from the random access port while it is shifted out of the serial port.

Other specialized RAMs include such oddities as a resettable static RAM, the Am9150, from Advanced Micro Devices (Sunnyvale, Calif). This 25-ns device can clear and reset an entire memory array in two cycle times. It is suitable for cache, high speed buffer memory, and video imaging among other things. Another AMD part, the Am9151 SRAM, can monitor internal state information and can shift the information out via the serial data path to be observed.

Crossing the dividing line between RAM and non-volatile memory are several unusual memories from NCR (Miamisburg, Ohio) and Hughes (Newport Beach, Calif). These devices consist of a RAM array with a duplicate electrically erasable PROM array for backup. They include the 1-Kbit (128 x 8) NCR52001, the 2-Kbit (256 x 8) NCR52002, and the 256-bit (64 x 4) Hughes H3500. Such shadow RAMs were pioneered by Xicor, a Milpitas, Calif-based company that has just pushed the state of the art to 4 Kbits (512 x 8) with its newest NOVRAM, the X2004. Access times for all these are in the neighborhood of 300 ns.

A unique approach to nonvolatility is found in the MK48Z02 2-K x 8-bit SRAM from Mostek (Carrollton, Tex). In most respects, this part is a conventional CMOS SRAM with 150-ns cycle time. Onchip power-failure detection circuitry, however, deselected the SRAM when  $V_{CC}$  drops below 4.5 V. At that point, standby power is maintained by two lithium-carbon monofluoride cells that are housed in a separate "tophat" soldered to the DRAM. Data can be maintained without power for ten years. The lithium batteries have proven so reliable that a single cell tophat version, the MK48Z02A, has been designed for cost savings.

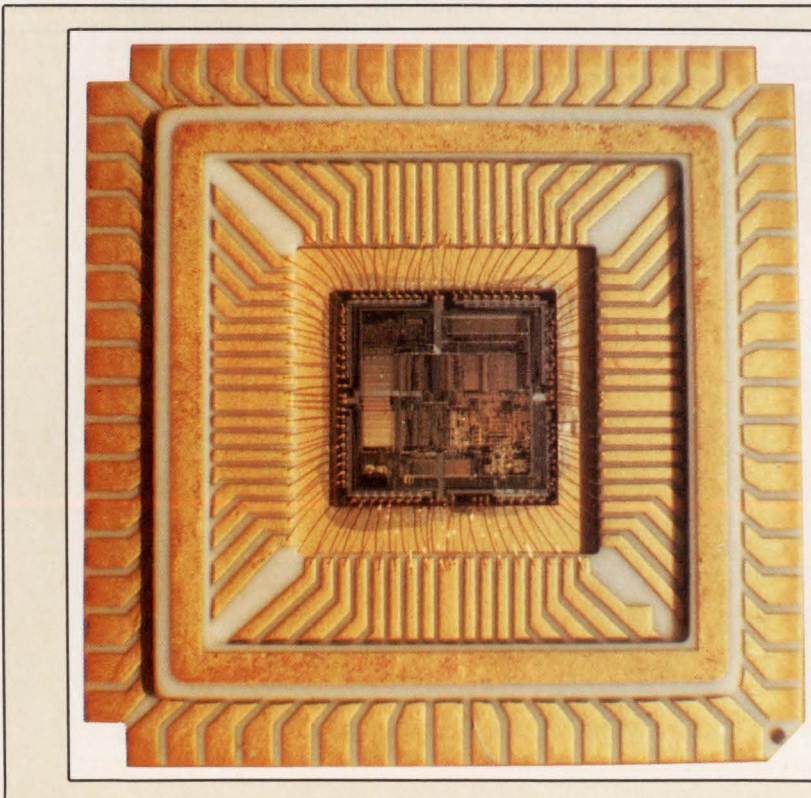
### Mainstream nonvolatility

Despite the advances in unusual mixed technology nonvolatile memories, mainstream nonvolatile memories—ROMs, PROMs, EPROM, and EEPROMs—continue to make advances in speed and density that keep them firmly in the lead. For example, Solid State Scientific (Willow Grove, Pa) introduced a line of 256-K CMOS ROMs with 75-ns access times. Many such new designs are moving to CMOS, although NMOS ROMs are still widespread. The move to 1-Mbit and denser devices should prompt more transition to CMOS. Such dense circuits, however, may increase the risk of code obsolescence and drive designers to alternate technologies, despite the obvious advantages of higher density and lower cost offered by ROM.

High speed (10 to 70 ns, depending on technology and size) continues to be the province of TTL (and ECL) fuse PROMs, but the most complex devices yet fabricated only have a density of 64 Kbits. There are, however, other uses for PROMs than the traditional fast instruction storage applications. They are finding increasing application as they take their place next to programmable logic arrays (PLAs) and Monolithic Memories, Inc's PALs.

PLAs permit programming of both AND or OR arrays while PALs only have programmable AND arrays. PROMs, on the other hand, have a programmable OR array and a fixed AND array. Thus, PROMs are a perfect complement to PALs. Where the PAL has many input terms, the PROM is rich in product terms and can be used to implement functions that cannot be accomplished in a PLA or a PAL. In addition to such logic functions in non-registered PROMs, registered PROMs are useful for state machines and pipelining. Nonetheless, the main use for PROMs is still memory applications where speed is important.

As ROMs have reached the 1-Mbit level, the major competition for these devices—the EPROM—edges to the 512-Kbit level with at least two manufacturers delivering such parts: AMD and Intel. NMOS continues to be the process technology of choice for EPROMs, but both Seeq and Toshiba have built 256-Kbit CMOS chips. The importance of the 512-Kbit EPROM is underscored by the fact that an



The NCR/32 VLSI processor is designed to emulate existing mainframes through the use of external microcode.

entire operating system such as MS-DOS or CP/M-86 can be stored on one chip, with room left over. Performance is also impressive for EPROMs. AMD's Am27512 is organized as 64-K x 8-bit and has a 250-ns access time. Meanwhile, the 1-Mbit EPROM may be only a year away.

After a long gestation period, EEPROMs have evolved rapidly, reaching 64-Kbit density this year. With the advent of the 64-Kbit device, manufacturers finally agreed on the incompatible function and pin assignments. As manufacturers find ways to speed up the write times, avoid false storage cycles, and increase density, EEPROMs may eventually broaden their design niche which sits squarely between EPROMs and RAMs. A great deal of design activity is directed toward improving these devices. But, there is little consensus yet about the right way to build them.

#### Microprocessor headlines

The big story in microprocessors was the introduction of sophisticated 32-bit chips. First out of the gate were the offerings from NCR and National Semiconductor (Santa Clara, Calif) with the long-awaited Motorola (Austin, Tex) chip arriving about midsummer. Other major 32-bit microprocessors, such as those from Intel and Zilog, will be seen the first half of 1985.

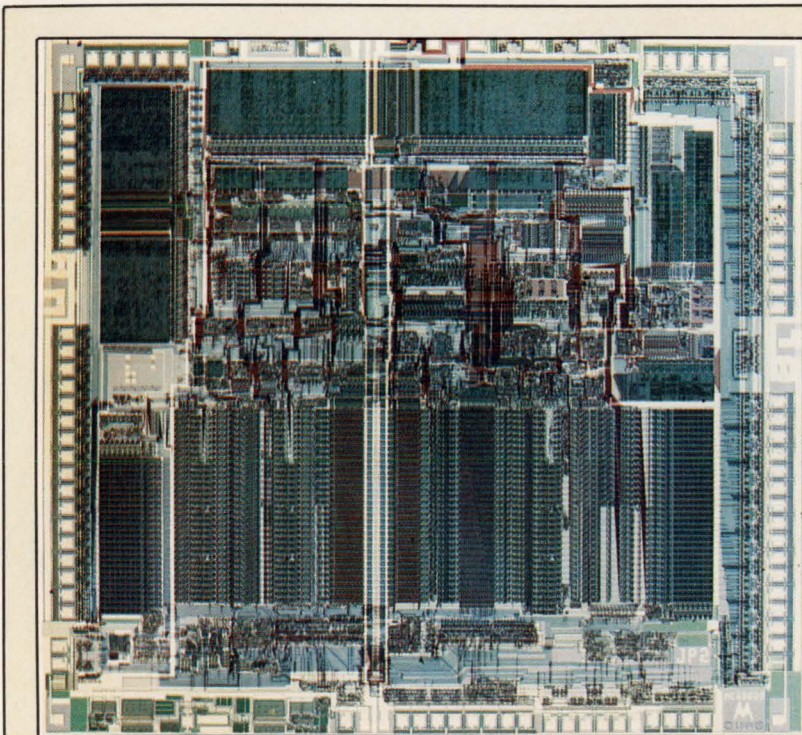
The NCR/32 is a unique microprocessor. It consists of a set of four VLSI chips and two LSI chips that form a powerful CPU. Its unique use of exter-

nally programmable microcode enables the NCR/32 to emulate other computers. The chip set contains a 32-bit central processor, an address translation chip for memory management, an extended arithmetic chip for floating point arithmetic, and a system interface controller for slow speed peripheral I/O and system interface transmitter and receiver chips.

*With the 512-Kbit EPROM, an entire operating system can be stored on one chip, with room left over.*

A 128-Kbyte instruction storage unit (ISU) contains the external microinstructions that tailor the system to the user's needs. The processor has a set of 179 primitive instructions onchip while the external ISU contains the instructions of the computer that is to be emulated. Although any machine can be emulated, the system is optimized for the IBM 370 instruction set and supports IBM floating point. Consequently, the NCR/32 will run IBM MVS at about the same speed as an IBM 4331.

The NS32032 from National Semiconductor was the first 32-bit microprocessor from a major semiconductor manufacturer. The company beat other manufacturers to market by being conservative from a process standpoint. Using a 3.5-micron NMOS



**The Motorola MC68020 CMOS microprocessor integrates 192,000 transistors on a single chip and is capable of 2 to 3 MIPS sustained instruction rates.**

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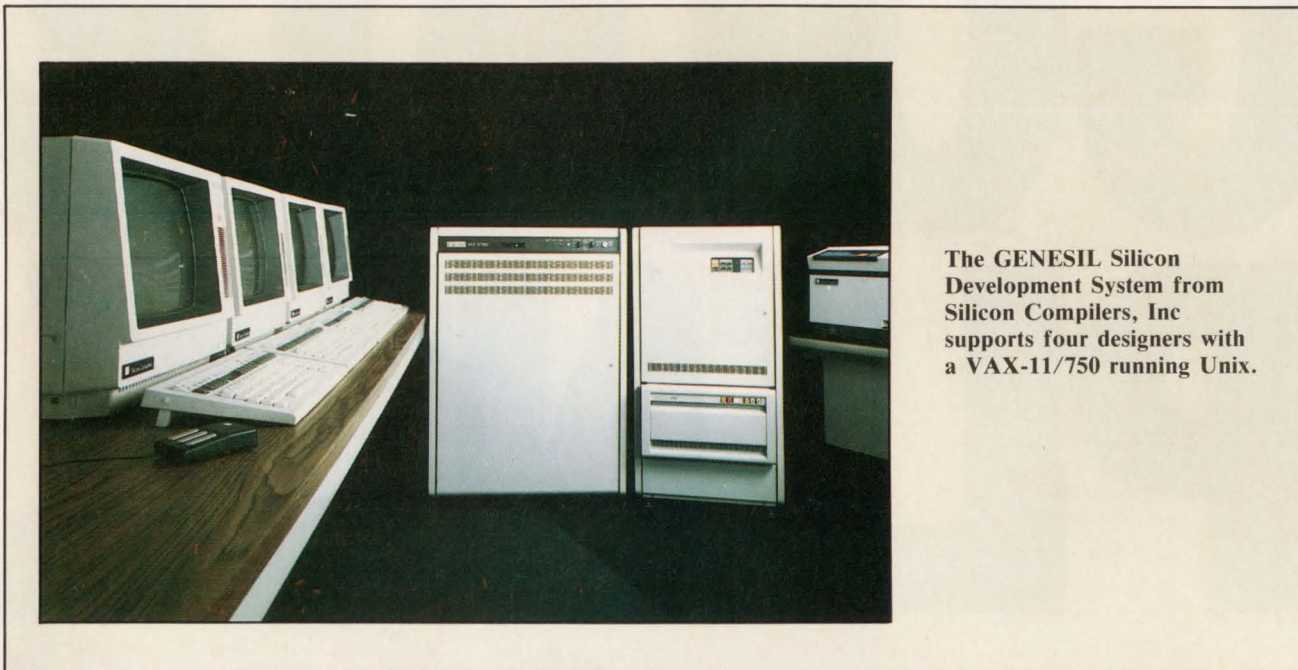
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	100ns	120ns	150ns	Page Mode	TRAC/TCAC	CAS before RAS refresh
FUJITSU	yes	yes	yes	yes	2:1	yes
TI	no	no	yes	yes	1.66:1	no
INMOS	yes	yes	yes	no	1.66:1	yes

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**The GENESIL Silicon Development System from Silicon Compilers, Inc supports four designers with a VAX-11/750 running Unix.**

process enabled the designers to concentrate on a sophisticated VAX-like architecture that provides excellent high level language support.

Along with the full 32-bit implementation of the chip, National also offers 8- and 16-bit external data path versions that contain the same 32-bit processor. The product line is rounded out with slave processors for floating point and memory management. Future versions of the NS32032 will be built in CMOS. As the technology permits, the slave processors will be brought onchip. Future versions of the chip will also use a bus protocol designed to support a high speed external cache.

The VAX influence is most apparent in the instruction set and addressing modes that provide high level language support. Along with standard addressing modes there are five additional addressing modes, specifically designed to support high level languages. For example, support of stack-based addressing simplifies the use of reentrant code and is useful for block structured languages.

As a result of the architectural features that National included on this chip, there has been a great deal of interest from system designers. The company, despite several attempts, however, has not been a major force in microprocessors. Understandably, some designers had qualms about committing to this new micro—especially without a second source. When Texas Instruments committed itself as a full-blown second source, it removed a major impediment to the success of the NS32032 and gained a share of a business in which it has had limited luck.

The smart moves of National Semiconductor and TI came none too soon because they were followed

by Motorola's big guns. With the introduction of the long-awaited MC68020 in midsummer, Motorola hopes to gain the next generation follow-on business to the immensely popular MC68000 and MC68010. The new microprocessor will be a formidable rival that makes full use of the latest technology.

The MC68020 will execute instructions at 2 to 3 million instructions per second (MIPS) with bursts to 8 MIPS. The 2-micron CMOS chip packs in 192,000 transistors while dissipating only 1.5 W and operating at a clock frequency of 16.67 MHz. The address bus, data bus, internal data, and address registers, as well as the three ALUs, are all 32 bits. Up to 4 Gbytes of nonsegmented linear memory space can be addressed over the 32-bit address bus. Despite this emphasis on 32 bits, 8- and 16-bit peripheral subsystems can be easily accommodated. Dynamic bus sizing allows the data bus width to accommodate 8-, 16-, or 32-bit words on a cycle by cycle basis. An onchip instruction cache of 256 bytes holds recently used instruction sequences.

At the time of introduction, the MC68881 floating point processor was not yet ready but was due to arrive by year end along with a gate array version of the memory management unit. The MC68851 MMU, implemented in CMOS, will not be available until mid-1985. How well Motorola adheres to its delivery schedule will be important to the acceptance of the MC68020, considering that the lack of such coprocessors was the one noticeable flaw in the success of the MC68000.

Semiconductor manufacturers must build VLSI circuits that appeal to a large market. These include memories, microprocessors, peripheral controllers,

# Microprocessor programming made simple.

"Keep it simple" was the principle of the 14th Century English philosopher William of Occam and it has even more validity today. Faced with the problems of sophisticated computer systems, designers have found that ever more complex programming languages are further complicating their tasks. Until now.

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When we started designing our new VLSI family of 10-MIP transputers, we built on William's simple philosophy. To take advantage of the possibilities opened up by the transputer, we needed to create a language capable of properly addressing parallelism and multi-processor systems.

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But occam is not limited to our

transputer family. It provides an efficient, responsive implementation language for systems built on today's microprocessors. It also opens up future possibilities with its performance-enhancing multiprocessor capabilities. And INMOS now offers a product to let you exploit occam's total capability in your system.

## **Simplify your job with the Occam Programming System.**

The Occam Programming System (OPS) gives you the tools for complete VAX/VMS software development. This package includes an integrated editor/checker, an optimizing VAX compiler and full documentation. This gives you a supportive environment for the development of occam programs

for execution on the VAX. Cross-compilers for 68000 and 8086-based systems will also be available.

What's more, the occam programs developed and proven on the OPS will give you a head start for work with the INMOS transputer. Extensions to the OPS will be available which will allow occam programs to run on the transputer.

And if you have a requirement to program the transputer in other popular high-level languages, other extensions will include compilers for C, Fortran, and Pascal.

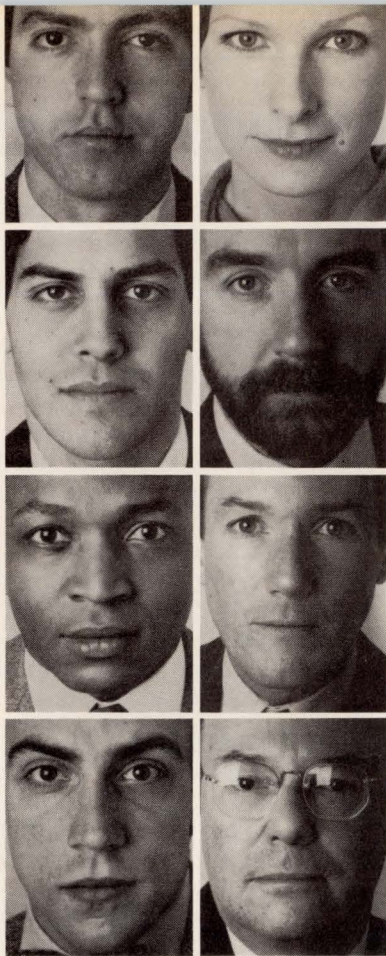
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FOCUSING ON THE OEM

## INTEGRATED CIRCUITS

and special-purpose variants on these themes. The system designer, however, is faced with the need to construct unique systems that have special benefits. The requirement to put such unique systems into VLSI circuits has led to a rapid growth in application-specific ICs.

### Application-specific ICs

There was rapid growth in ASICs during the year, and that such circuits may account for a third of the total IC market by the end of 1985. Gate arrays and standard cells account for a considerable portion of this growth. Nonetheless, it is not possible to get the same silicon efficiency from gate arrays as standard ICs. Even standard cells, although much better than gate arrays in circuit density and efficient use of silicon, lag behind fully custom designs. Until recently, there seemed no way out of this bind. This year, however, silicon compilation finally began to look practical with the introduction of silicon compilers from Silicon Compilers, Inc (Los Gatos, Calif) and Metalogic, Inc (Cambridge, Mass).

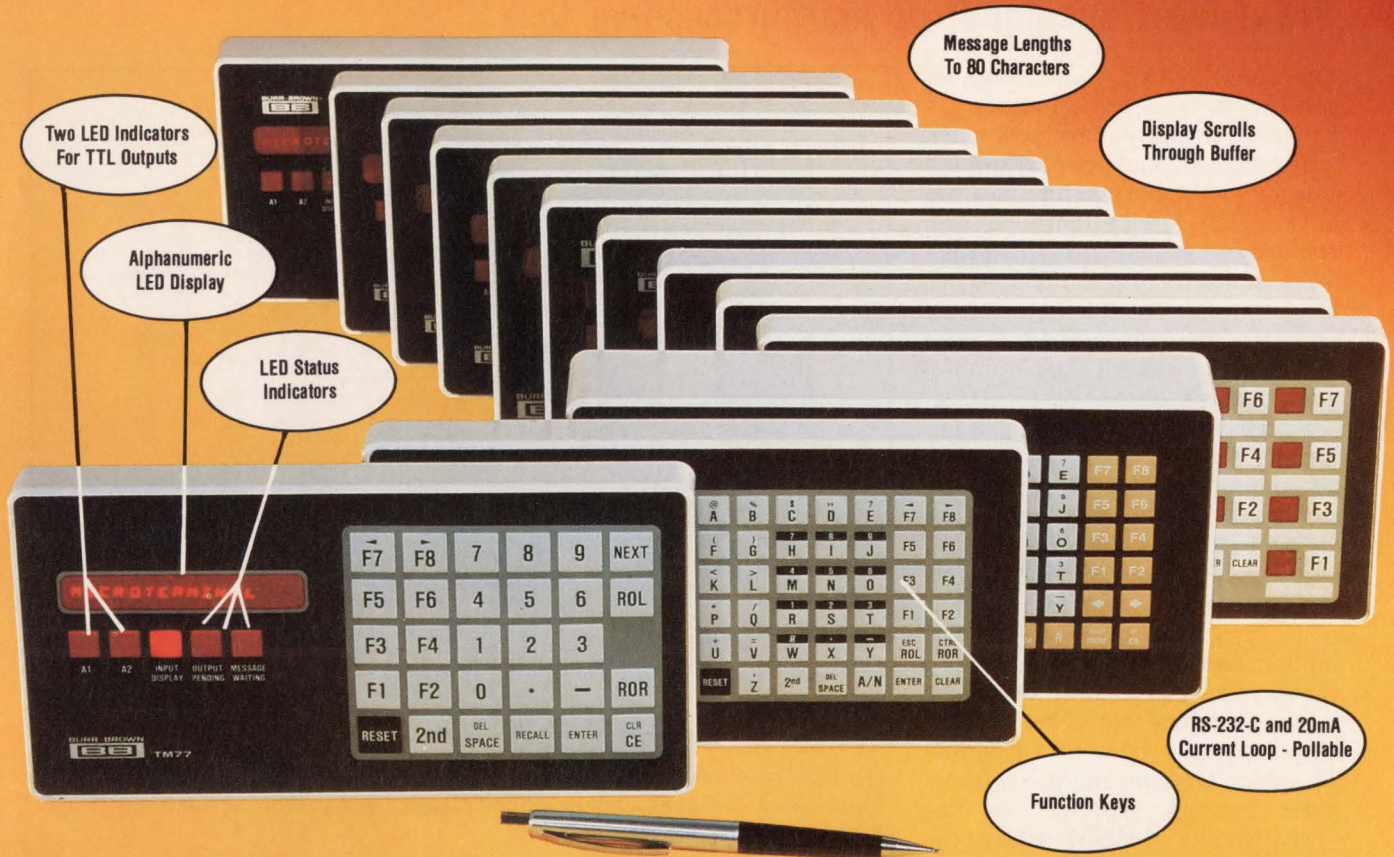
Efficient full custom designs with fast turnaround may now be possible. Gate arrays, standard cells, and even PLAs will continue to serve for circuits of moderate complexity. But, to take full advantage of the high levels of integration of CMOS requires custom circuits. Designers will only be able to get this fast turnaround using efficient silicon compilers. Furthermore, silicon compilation will enable system designers to design their own ICs. That is a key consideration because there are only several thousand IC designers in the country.

It became apparent this year that the high speed functions dominated by bipolar technologies such as Schottky and ECL could eventually be taken over by GaAs digital circuits. Gigabit Logic, Inc (Newbury Park, Calif) and Harris Microwave Semiconductor, Inc (Milpitas, Calif) both introduced GaAs digital logic. Tektronix (Beaverton, Ore) announced the formation of a GaAs foundry. Both Harris and Tektronix designed GaAs gate arrays. Many of the fabrication problems have been solved but transistor design for these circuits is still evolving.

The most common GaAs circuits employ depletion mode metal gate Schottky field effect transistors. Within a year or two enhancement mode devices may take their place as fabrication techniques improve. That advance should bring lower power consumption and operating temperatures. Circuits containing both type devices have been built. GaAs will not replace silicon but it will, in the long run, have a much larger share of the market. This year that finally seemed possible.



# 13 Small, Smart Solutions For Data Entry & Display



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TM71	16	110-19200	320 <sup>(1)</sup>	Alpha	14	Full feature	+5VDC
TM77	16	110-19200	320 <sup>(1)</sup>	Numeric	14	Larger keys	+5VDC
TM71-I/O	16	110-19200	320 <sup>(1)</sup>	Alpha	14	TTL I/O	+5VDC
TM77-I/O	16	110-19200	320 <sup>(1)</sup>	Numeric	14	Larger keys	+5VDC
TM71B TM71MS	16	110-19200	320 <sup>(1)</sup> 5 x 50 <sup>(2)</sup>	Alpha	16	Bar Code Wand	+24VAC/ DC
TM77B TM77MS	16	110-19200	320 <sup>(1)</sup> 5 x 50 <sup>(2)</sup>	Numeric	16	Mag Stripe Reader	+24VAC/ DC
TM71M	16	110-9600	320	Alpha	14	Military	+5VDC
TM70	12	300 & 1200	36	Alpha	8	Low cost	+5VDC
TM76	12	300 & 1200	36	Numeric	8	Larger keys	+5VDC
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CIRCLE 63

## Transputer designed for multiprocessing tasks

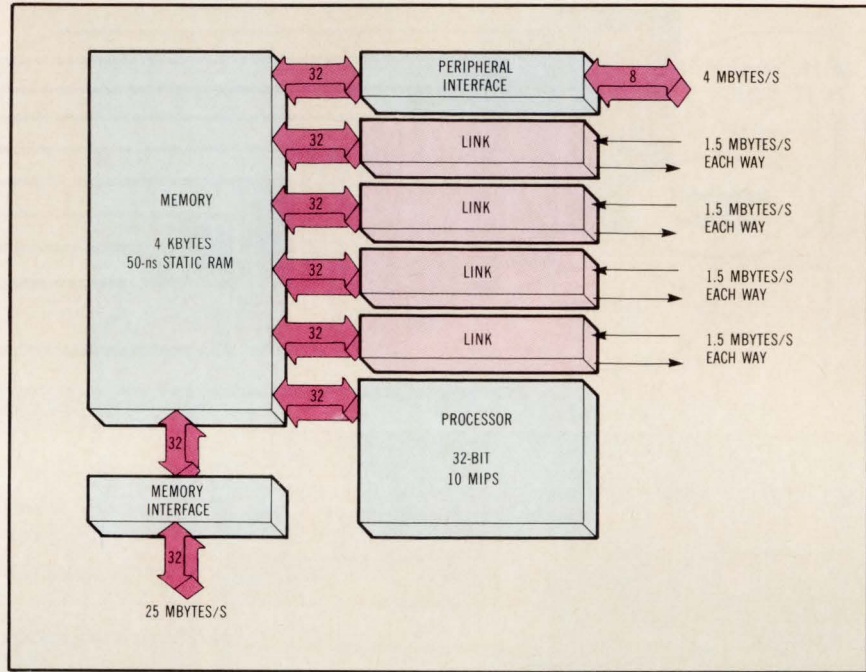
The 10-MIPS IMS T424 transputer consists of a small processor, 4 Kbytes of memory, interfaces to external memory and peripherals, and four high speed communication links. The 32-bit transputer can respond to external interrupts within 600 ns and support simultaneous block transfers between the peripheral interface, the four standard links, and memory without significant degradation in processor performance.

System architecture is optimized to execute Occam, a concurrent programming language. This software sees the system as a collection of concurrent processes that communicate with each other and with peripherals through channels. Programs are built from three primitives: assignment, input, and output. Assignment changes the value of a variable, input receives a value from a channel, and output sends a value to a channel. The same Occam program a transputer network executes can run unchanged by a smaller network or a single transputer.

The three processes combine to form sequential, parallel, or alternative constructs. A construct is also a process, and can act as a component for another construct. Conventional sequential programs translate into Occam via variables and assignments, which then combine to form sequential constructs.

Concurrent programs translate to Occam by combining channels, inputs, and outputs to form parallel and alternative constructs. Each channel provides a one-way connection between two concurrent processes that communicate when both are ready. An alternative process may be ready for input from any channel, so that input is taken from the first channel to be used for output by another process.

Besides Occam, the transputer processor can be programmed in industry standard high level languages, such as C or Pascal. The processor executes programs sequentially—it implements parallel processes by



**The IMS T424 Transputer includes a 32-bit processor, 4 Kbytes of memory, 4 high speed communication links, and memory and peripheral interfaces. It is optimized for multiprocessing.**

sharing its time between the process sets that are active at any instant. For example, a currently running process continues to execute until it requires I/O communication. At that point, the processor temporarily abandons the running process in favor of the next process on the active queue. When the processor communicates with a ready channel, the message passes to the waiting process, which then goes to the end of the active queue.

Supporting two priority levels—0 for high and 1 for low—the processor maintains a queue of active processes for each level. When there are no active priority 0 processes, the latency is typically 600 ns, maximum 2600 ns. (Latency is defined as the time from the instant an external channel is ready to the start of the first instruction of the relevant waiting priority 0 process). If a priority 0 process is already executing, the waiting process links to the end of the priority 0 queue.

Four high speed links provide communication and a variety of network configurations. Each link has two Occam channels: an output and an input to carry data and link control information. Links operate independently and provide block transfers between transputers. The sending transputer transmits messages as a sequence of bytes, then awaits an acknowledgment. This signifies that the receiving transputer is ready to accept another byte.

Transmission is continuous because the receiving transputer acknowledges as soon as it starts to receive a data byte. Moreover, this asynchronous protocol guarantees reliable transmission despite sending or receiving delays. During transmission, both processes are set inactive and will link to the end of their respective active queues only after final byte acknowledgment.

Software sets data rates on each link using the LinkSet configuration channel. Highest frequency is 20

Mbits/s for a maximum data rate of 1.8 Mbytes/s on a channel.

Separating the peripheral interface from the memory interface optimizes each one for its principal function. The memory interface supports mixed memory systems that generate signals for both nonmultiplexed and multiplexed memory. Memory timing is selected by a program or externally controlled by a wait signal. The 32-bit multiplexed data and address bus interface extends the internal address

capability to 4 Gbytes in a single linear address space. Nonmultiplexed cycles provide timing signals to drive industry standard RAMs and ROMs, while the multiplexed cycle provides RAS and CAS control signals for external address multiplexers.

The peripheral interface accesses industry standard devices such as controllers, memories, and microprocessors. Its 8-bit bidirectional bus inputs or outputs byte sequences. Two control lines address external

devices, and an Event input provides interrupt capability. Accessed via four standard output and input channels, the interface allows all eight channels to use the same 8-bit data path. The processor initiates transfers via handshaking. Transfers are synchronized to a separate external clock; asynchronous operation is also permitted, but at a lower speed. **Inmos**, PO Box 16000, Colorado Springs, CO 80935.

Circle 293

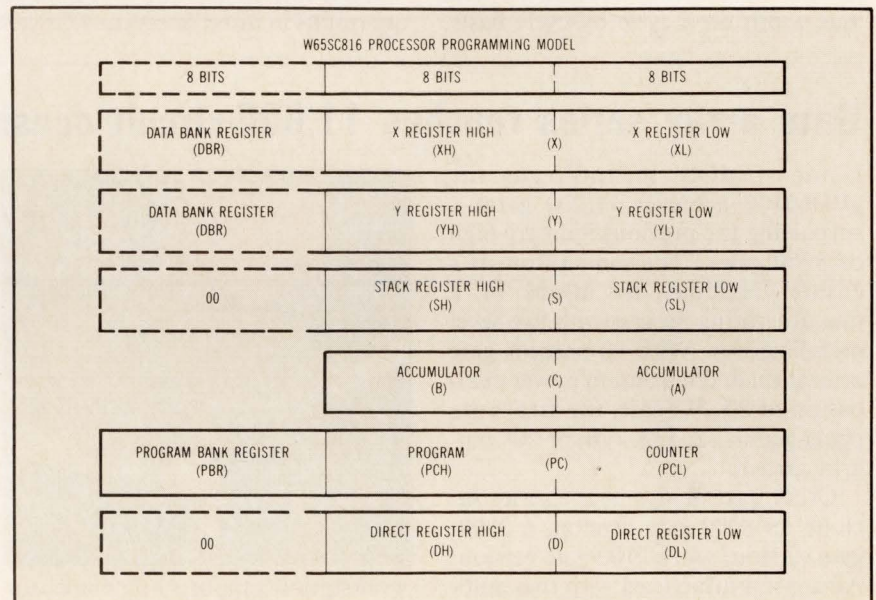
## Family of 16-bit CMOS processors extends 6500 capabilities

Pin compatible with NMOS and CMOS versions of the 6500, W65SC8XX and W65SC9XX chips have a 24-bit addressing range. Despite enhanced features, the family retains software compatibility with existing 6500 code.

Made using the proprietary OXI-CMOS technique, the processors will appear in 1-, 2-, 3-, and 4-MHz versions. The W65SC802 is pin compatible with 8-bit 6502 devices, while the W65SC816 extends the address range to 16 Mbytes. A software switch puts the processor either in 8-bit emulation mode to run existing software or in 16-bit mode to use the 16-bit internal registers and address the full 24 Mbytes of memory.

Internally, the accumulator, ALU, X, and Y index registers, and stack pointer have been extended to 16 bits. The new processors also contain a 16-bit direct page register to augment the direct page addressing mode. Separate program bank and data bank registers extend the X and Y and program counter registers to address 24 bits of address space. Besides the thirteen 6502 addressing modes, the family provides 11 new modes, including stack relative addressing, block move addressing, and absolute indexed direct addressing.

On the W65SC816, four additional signals create a range of options for



With its 24-bit addressing, the W65SC816 CMOS microprocessor extends the range of 6500 code, while retaining software compatibility.

system configuration. The abort input signal can interrupt a currently executing instruction without affecting the internal registers. Two outputs enable the designer to create dual-cache memory by telling the system whether a valid data segment or a valid program segment has been addressed. Vector pull output can be monitored to tell whether to modify a vector. The latter signal goes low

during the two cycles when a vector address is being pulled, as well as for all interrupt vector pulls.

While the W65SC8XX and W65SC9XX family chips are implemented in 3- $\mu$ m silicon gate CMOS, a 1.5- $\mu$ m version will be developed in the near future. **Western Design Center, Inc.**, 2166 E Brown Rd, Mesa, AZ 85203.

Circle 294

## Thirty-two bit microprocessor performs 2 to 3 MIPS

Integrating 192,000 transistors on a single chip, the MC68020 includes nonmultiplexed, 32-bit, internal and external data and address paths. The chip is built using a 2-micron HCMOS process to produce the 375 x 350 mil die. It is packaged in a 114-lead pin grid array that dissipates less than 1.5 W. Functioning at 16.67-MHz clock frequency, the chip operates at burst rates exceeding 8 MIPS and sustains instruction rates of 2 to 3 MIPS.

In the MC68020, all registers, program counters, stack pointers, and arithmetic and logic units are 32 bits wide. The 32-bit design eliminates instruction timing differences for 8-, 16-, and 32-bit operations. The bus interface dynamically adjusts the data bus width on a cycle by cycle basis,

to accommodate 8-, 16-, or 32-bit devices. Consequently, existing 8- and 16-bit peripheral subsystems can be used with the 32-bit microprocessor.

Although it is object-code compatible with earlier 68000 family members, the MC68020 adds addressing modes and instructions that help develop high level language compilers and graphics applications. Existing 68000 instructions have 32-bit extensions in the 68020. Addressing modes include 32-bit displacements, memory indirection, and scaled indexing. New instructions include bit-field operators, double-ended bounds checking, BCD data compression and expansion, module support, and enhanced system calling functions.

Hardware support of virtual memory results in direct access to 4 Gbytes

of logical memory. Like the 68010, the new processor can also process page faults by suspending instruction execution until the physical memory can be updated with the requested information from disk.

A coprocessor interface is provided as a means of extending the instruction set with offchip devices. Two important coprocessors that will be introduced for the 68020 are the long-awaited FPP and the MMU needed for efficient support of demand-paged virtual memory. A full-blown HCMOS chip—the MC68851—will be available in the middle of 1985. **Motorola Semiconductor Products, Inc.**, 3501 Ed Bluestein Blvd, Austin, TX 78721.

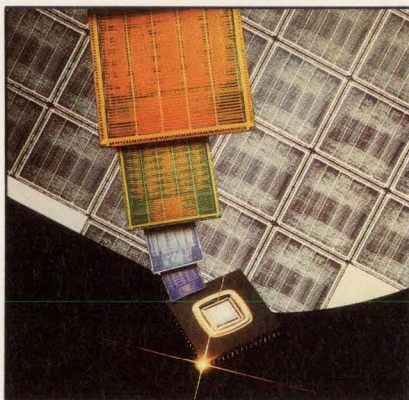
Circle 295

## Gate array series reaches 11,000-circuit density

Using CMOS technology, the  $\mu$ PD65100 achieves 11,000 gates—surpassing the previous industry high of 8000 gates. The semicustom ICs ensure flexibility by means of a manufacturing process with two-level metallization. With 90 percent gate utilization and maximum power dissipation of 20  $\mu$ W/gate, the arrays are packaged in 72, 132, 176, or 208 pin-grid arrays.

Other gate arrays in the series include an 8000-gate version, a 3300-gate version, and a 2100-gate version. All are manufactured with two millimeter channel lengths. Processing speed is 2 ns/gate with three fan outs using 3-mm wiring.

The gate array development process is structured so that users will not be restricted to one interface type. The simplest interface requires a circuit diagram and test patterns. The company then takes on the rest of the development process. Other available interfaces range from providing a net list and test pattern in NEC-compatible format to graphics PC-generated data, where information is generated via the PC9800 workstation. This



workstation supports schematic capture and limited design rule checking.

In this gate array series, the entire development process begins with design rule checking. Parameters such as cell usage, power dissipation, and fan-out loading are determined and checked. Then, all coding errors and data conversion errors are checked and eliminated. Prior to automatic placement and routing, a delay time simulation provides an expected circuit delay analysis. At this point, placement and routing software allows up to 95 percent cell utilization without resorting to manual routing.

Further in the development process, a final delay time simulation occurs. Actual wire lengths are taken into account for accurate circuit analysis. If all previous steps are successful, the design enters production, followed by testing of all wafers. Wafers are divided into individual chips that are die bonded onto customer-specified packages. Each chip is wire bonded and sealed with dc parameters and its logic functions are checked by a final test.

An ECL type gate array with 3000 gates, a delay time of less than 1 ns/gate and power dissipation of 1.1 mW/g is also available. Two other ECL gate arrays with subnanosecond delay times, and one TTL with a 2-ns/gate delay time round out the gate array offerings. Pricing varies according to package type, but an approximate figure is \$200 per unit in 5000-piece quantities plus an \$80,000 nonrecurring engineering option. Delivery is approximately 10 to 12 weeks after initial simulation and verification. **NEC Electronics, Inc.**, 401 Ellis St, Mountain View, CA 94043.

Circle 296

## Chip finds degree of similarity between strings

Adaptive pattern recognition systems deal with information based on inexact, inaccurate, or incomplete data. One problem has been determining the degree of similarity between strings. That function—computing similarity—has now been placed on a silicon chip called the Proximity Filter PF474 microcircuit.

The PF474 performs extremely fast serial string comparisons and computes a degree of similarity for each. This comparison is expressed as a 32-bit binary fraction. Two totally dissimilar strings will yield a zero, while two exactly matching strings will produce a one. In computing the

degree of similarity, the PF474 uses a set of parameters that are stored in onchip RAM. The 16 best matches are then stored in the ranker section of the chip, which also contains flags to locate the 16 next best matches, and so on. The Proximity computer section and the ranker operate in a pipelined mode so that neither need slow down the other in order to complete an operation.

Software comparison algorithms have yielded computation times that are proportional to the square of the number of characters in the string. With the PF474, however, the comparison time is linear with the length

of the string, provided data is supplied at the chip's full input rate. Since the PF474 is mapped into memory address space and has a DMA capability of up to 2 Mbytes/s, 8-char (byte) strings can be compared at a rate of 49,600 comparisons/s, while 127-byte strings run at 3870 comparisons/s.

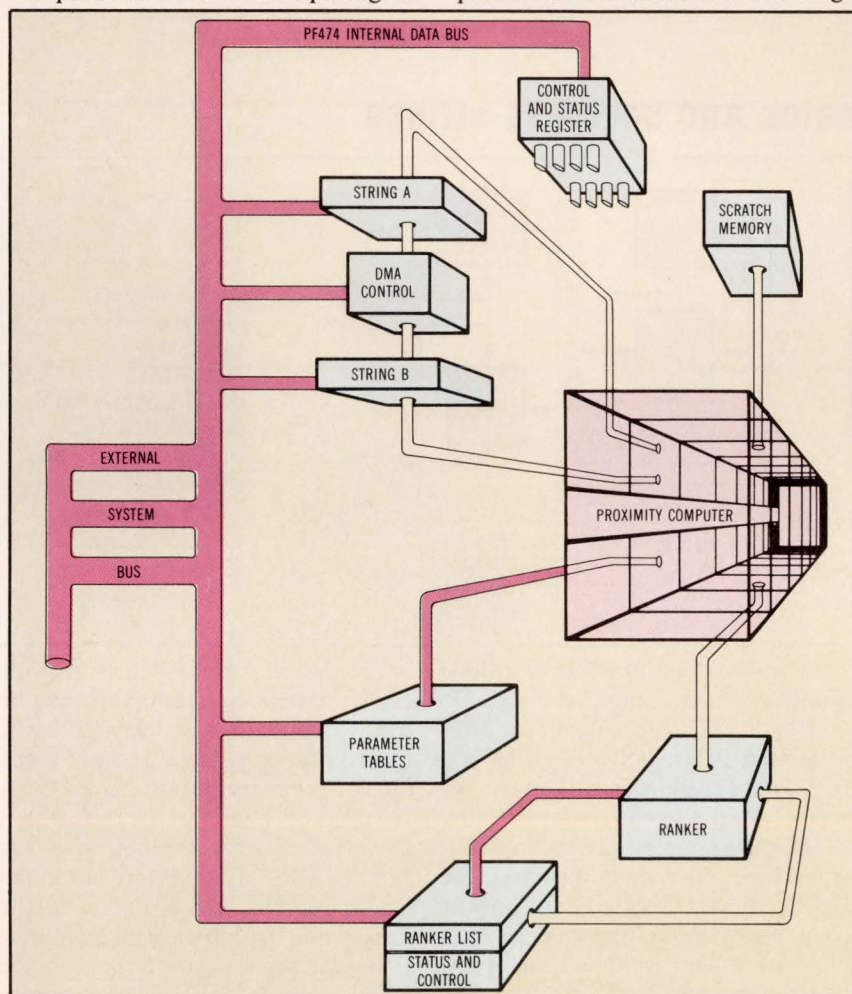
The PF474 normally operates by taking a query string, for which parameters of similarity have been loaded into its parameter RAM, and rapidly searching through a long list of comparison strings in a data base. It is thereby possible to perform an exhaustive search in an acceptable time frame without limiting the search space and risk missing some similar strings.

To the system, the PF474 looks like a 1024-byte address range that is partitioned into four 256-byte sections: control, parameter, string, and ranker. The chip also contains the special purpose Proximity computer core which calculates the comparisons. The string section is further divided into two 128-byte sections to hold the query string and the string currently being compared to it. Since a string must be terminated by a null character, strings of up to 127 bytes in length can be processed.

The three parameters stored in each byte are weight, compensation, and bias. Weight is a direct reflection of the importance of a character in the string, and can vary in value from 0 to 7 (3 bits). For example, in comparing English words, less weight would be assigned to vowels than to consonants and different consonants might have different weights according to the similarity or difference of the sounds they make. A weight of 0 would be almost ignored, but it would affect the similarity since it occupies a position in the string.

The bias parameter tells if a character is more important near the beginning or near the end of the string. Bias can range from a value of  $-2$  to  $+1$ . For instance, if all characters had a negative bias, the computer would assign more importance to

*(continued on page 158)*



In the PF474 architecture, four major blocks—string space, control, parameter tables, and ranker—appear to the system as memory address ranges and can be directly addressed. The Proximity computer generates 32-bit binary fractions that are used by the ranker to establish the list of 16 best matches.

**Chip finds similarity**

*(continued from page 157)*

similarity near the beginning of the word than near the end.

Compensation considers the dissimilarity between two characters and whether a word contains a given character or not, or whether a given character is in the same position in both words. The compensation value of unmatched characters is cumulative in a comparison. Setting a high compensation parameter will make the comparison more tolerant of dropped characters. This type of pattern recognition thus necessitates two

main operations: determining what the parameters for computing similarity shall be, and performing the actual comparison and ranking the results. The PF474 was designed to do the latter at a very high speed while leaving the user to determine the parameters. The PF474 microcircuits also maintain a ranked list of the best matches.

The ranker consists of a control section and a section which contains (for each entry) the result of the proximity computation and an internal

record number (IRN) of the string matched. It does not store the actual strings, but rather the IRNs that typically correspond to database record numbers. If a longer list of ranked near-matches is desired, the application program can copy the contents of the ranker registers to some other location in system memory and keep track of the order of such lists. **Proximity Devices Corp**, 3511 NE 22nd Ave, Fort Lauderdale, FL 33308.

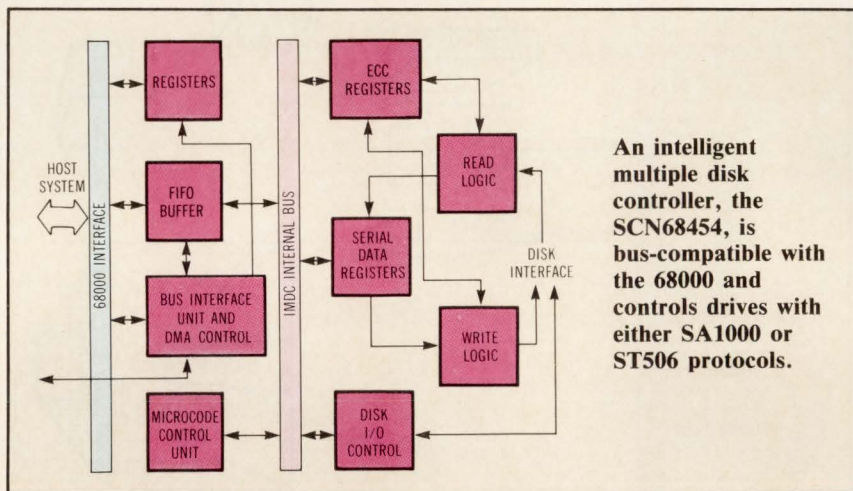
Circle 297

**Smart disk controller locates and searches strings**

The general trend in chip building is to put progressively more intelligence on silicon, and offload control functions from the host CPU. The Intelligent Multiple Disk Controller (IMDC) SCN68454 does just that by offering the system designer a versatile programmable disk controller. In addition, this controller provides a sophisticated string matching function that can be used to create a disk-based database system.

Bus compatible with the Motorola 68000 microprocessor, the chip supports vectored interrupts, a 31-bit address counter, and either 8- or 16-bit data transfers. It supports up to four floppy or hard disks, and uses either SA1000 or ST506 protocols to control the drives.

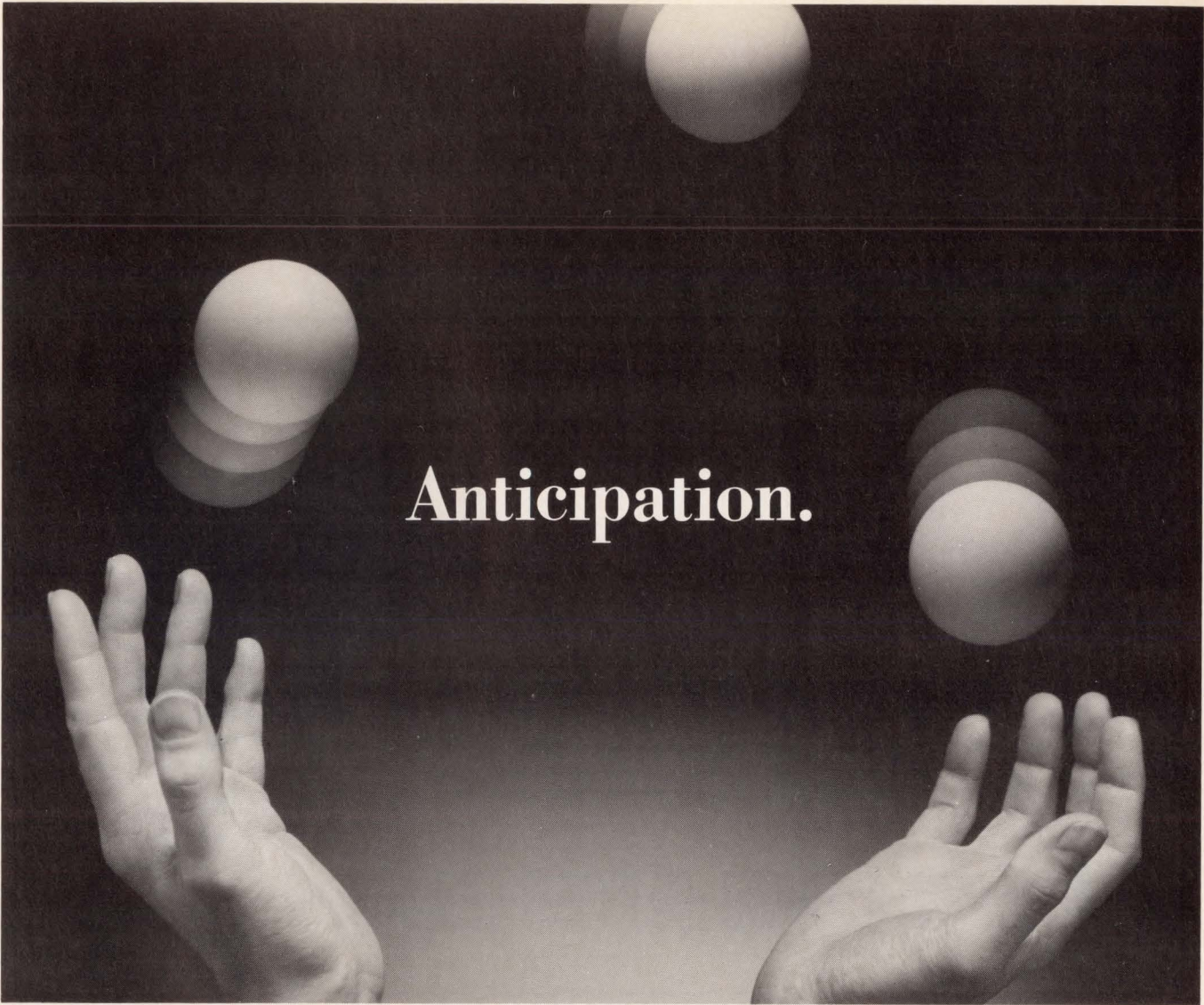
Capable of handling serial data rates up to 10 Mbits/s, the IMDC has a range of commands that allow the programmer to specify disk parameters, and to read soft or hard sectored disks, as well as standard IBM floppy formats. The chip has a DMA controller and a 128-char FIFO buffer onboard. It handles bus arbitration automatically and uses tables resident in the host's memory to get and send status and control information to and from the host.



Error-handling functions include automatic bad sector handling, 32- and 40-bit ECC, and support for host-generated ECC. It handles FM and MFM data encoding, and can read or write multiple sectors automatically.

Using parameters supplied in a control block in system memory, the IMDC locates a specified string of characters within any logical data block on the recording media. It can then retrieve and store the contents of the block, use a pointer value to access data within the block, or locate all data blocks that contain a string that matches a given search string.

Fixed- and variable-length records can be searched, and pointers can be used to search for key fields within the record. In fixed-length records, the index is an integral number of bytes from the beginning of the record, but in variable-length records, it is the "nth" field. To support variable-length records, the IMDC lets the programmer specify a field delimiter. Using the separator as a marker, the IMDC counts fields, and retrieves the proper one for key processing. **Signetics Corp**, 811 E Arques Ave, PO Box 409, Sunnyvale, CA 94086. Circle 298



# Anticipation.

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By selecting the data most likely to be needed at the CPU, the new IBM 3880 Model 23 Storage Control Unit can allow DASD subsystems to perform at electronic speeds. A microprocessor dynamically identifies the most active data and keeps it available in high-speed cache storage.

So when the CPU issues a disk read command, many of the responses may actually come from cache. When that happens, mechanical motion is completely eliminated as a factor in DASD response time.

IBM has combined its proven cache storage techniques with high-performance IBM 3380 DASD. This makes the Model 23 the preferred

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Using the Model 23, you may see one or more of these performance gains: Increased transaction volumes. Higher CPU utilization. Faster response to end users. Shortened batch run times. Or reduced contention for "shared" DASD.

And you may be able to lengthen DASD strings without affecting performance.

This new control unit has 8, 16 or 32 megabytes of cache, using IBM's powerful 256K-bit chip. It offers more speed, lower cost and better reliability.

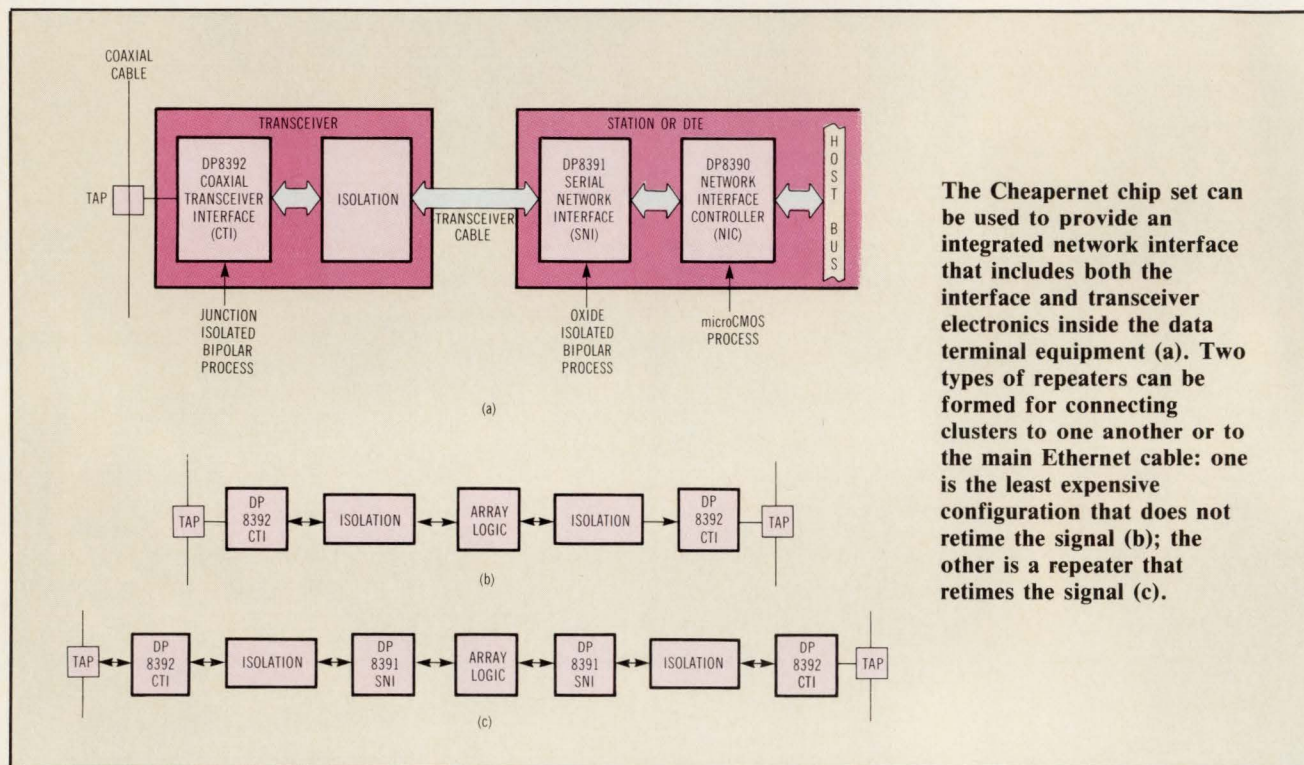
The Model 23 follows the Model 13 in IBM's family of cache storage devices.

For a free brochure to help you anticipate better IBM DASD performance, just call 1 800 IBM-2468, Ext. 562, or return the coupon. Or call your IBM marketing representative.



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## Chip set points to lower costs in Ethernet cabling



The Cheapernet chip set can be used to provide an integrated network interface that includes both the interface and transceiver electronics inside the data terminal equipment (a). Two types of repeaters can be formed for connecting clusters to one another or to the main Ethernet cable: one is the least expensive configuration that does not retime the signal (b); the other is a repeater that retimes the signal (c).

An Ethernet (IEEE 802.3) chip set cuts the cost of the interface electronics, cabling, and installation. Dubbed "Cheapernet," the chip set eliminates the extra drop cable by placing the transceiver electronics in the data terminal equipment (DTE) along with the interface electronics. Connection to the actual Ethernet cable is made with a repeater that can be built up from the chip set. Additional DTEs can be connected to the same repeater in clusters via inexpensive RG58 coaxial cable that connects to the equipment by means of BNCs.

This cabling technique places certain limits on the Cheapernet version that do not apply to the traditional Ethernet configurations. In Cheapernet, the network connection allows a cluster of up to 30 units (versus 100 units for Ethernet) to be assembled per segment with a maximum cable length of 200 m (versus the 500 m for Ethernet).

The components comprising the Cheapernet interface include the

DP8390 network interface controller, the DP8391 serial network interface, and the DP8392 coaxial transceiver interface. These components use the same IEEE 802.3 protocol as Ethernet except for the cabling technique previously explained.

The DP8390 network interface controller is a CMOS device that provides all the data link layer functions required to transmit and receive Ethernet/Cheapernet packets. It includes dual 16-bit DMA channels, which configure the buffer memory as dual-port memory. This dual-port memory then decouples network bus activity from the host. All bus arbitration logic and memory support are contained onchip. The network interface controller is able to filter physical, multicast, and broadcast addresses. It also has a three-level loopback for node diagnosis.

The serial network interface connects the network interface controller to the transceiver cable. It performs the Manchester encoding and decod-

ing of packets, generates carrier sense, and decodes the collision signal. This transceiver cable performs the same function as Ethernet drop cable except it is connected to the transceiver built around the coaxial transceiver interface contained within the terminal equipment.

The coaxial transceiver interface integrates all needed transceiver electronics, save the signal and power isolation. It directly drives the transceiver cable through isolation transformers. On the other side, it connects directly to 50-Ω coaxial cable.

The DP8392 has an onchip timer that can disable the coaxial transceiver interface driver if a data packet is longer than legal length. It also contains a collision detector and generates the collision signal to the DTE. **National Semiconductor Corp**, 2900 Semiconductor Dr, Santa Clara, Calif 95051.

Circle 299

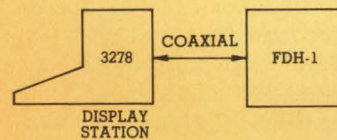


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- Plug compatible with IBM series 3250, 3270A, and 3270B equipment.
- Replaces coaxial cable with fiber optic cable.
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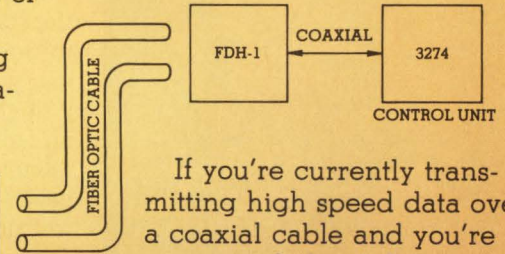
Versitron's FDH-1 (fiber optic digital hybrid) was designed to replace the coaxial transmission path in systems equipped with the IBM 3250 or 3270 series equipment. The simple installation of a fiber optic link provides two very important benefits to the user. First of all, the security level of the transmission link is greatly improved since fiber optic cables are inherently im-

mune to conventional wire-tapping techniques. Secondly, the system operating capability will be enhanced since fiber optic cables are impervious to virtually all types of electromagnetic interference. This includes, of course, interference from heavy duty manufacturing equipment and noisy adjacent cables.

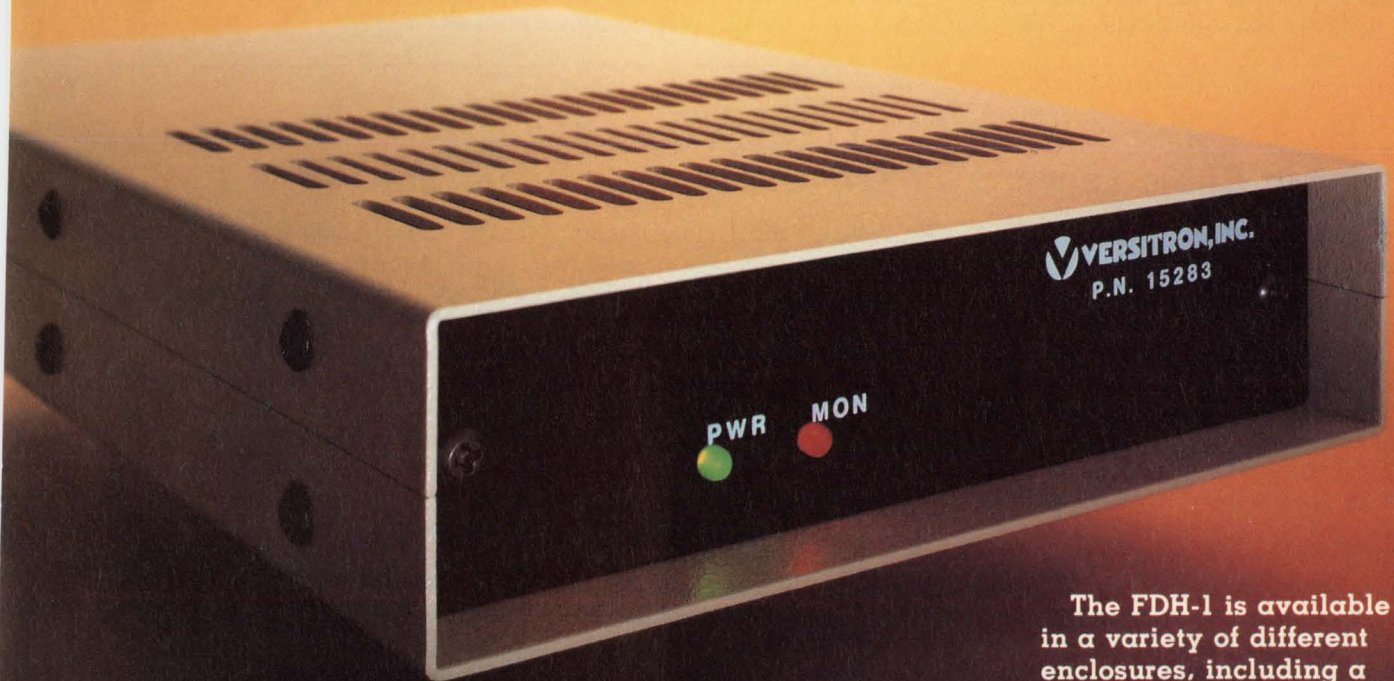


Versitron's FDH-1 combines the high speed capabilities of a coaxial cable with the inherent advantages of a fiber optic cable. By in-

terfacing directly to the coaxial cable, the FDH-1 appears totally transparent to the rest of the system; thus eliminating any operating restrictions.



If you're currently transmitting high speed data over a coaxial cable and you're concerned about data security, give us a call at (202) 882-8464 and get all of the details on how our FDH-1 will not only protect your data; but may also actually increase the operating efficiency of your entire system.



The FDH-1 is available in a variety of different enclosures, including a sealed unit specifically designed for EMI/RFI suppressed applications.

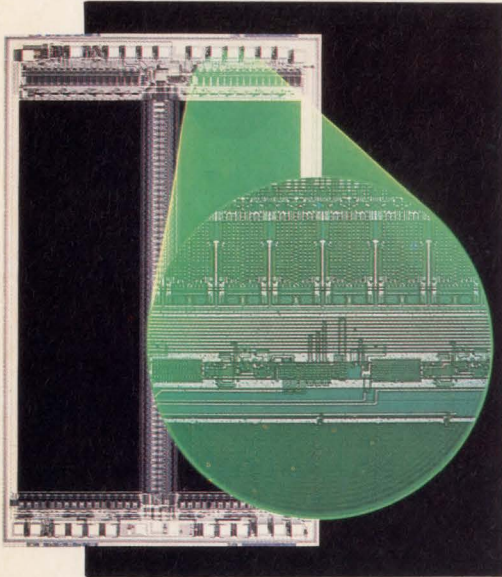
 **VERSITRON, INC.**

6310 Chillum Place, N.W., Washington, D.C. 20011, TEL: (202) 882-8464

CIRCLE 65

TWX: 710-822-1179

## Fast half-megabit EPROMs store software on silicon



The next rung on the erasable PROM density ladder comes in the form of the 512-Kbit Am27512. This chip closely follows the company's previous 256-Kbit EPROM distinguished by its 170-ns access time. The 512-Kbit

chip features many of the same characteristics, but unlike the 256-Kbit version (which used only row redundancy) the 512-Kbit model uses both row and column redundancy.

Organized as 65,536 words x 8 bits, the UV EPROM has a solid capacity to store such microprocessor operating systems as CP/M or MS-DOS on a single device. Putting the software directly onchip allows quick and reliable data access. In addition, the device can store microprocessor control programs for minicomputers.

An auto-select mode automatically reads the EPROM's binary code containing device manufacturer and type. This enables programming equipment to mate the device with its programming algorithm. Using an interactive programming algorithm, the chip requires as little as 6 min for programming. This algorithm uses 1-ms pulses that give each address only the number needed to reliably program data. A 12.5-V program-

ming voltage puts the Am27512 into programming mode. Bit locations can be programmed singly, in blocks, or at random.

Dissipating 132 mW standby and 525 mW active, the device reduces overall power requirements. It operates on a single 5-V supply and is packaged in a 28-pin JEDEC approved pinout. The EPROM is pin-compatible with the Am2764, Am27128, and Am27256 EPROMs, and the Am92256 256-Kbit ROM.

Output and chip enable eliminate bus contention in multibus processor systems. The chip enable is the power control and is used for device selection. Output enable accomplishes output control and is used to gate data to the output pins, independent of device selection. Available access times include 250 and 300 ns (commercial) and 450 ns (military). **Advanced Micro Devices Inc**, 901 Thompson Pl, Sunnyvale, CA 94086. **Circle 300**

## Dynamic RAMs deliver 256-Kbit power using CMOS process

The next-generation design cycle looms near as 256-Kbit dynamic RAMs arrive. Billed as the industry's first CHMOS 256-Kbit DRAMs, the chips represent a memory increase that could redraw the boundaries of graphics, portables, and several other applications.

Using its proprietary CHMOS technology, Intel employs dry etching and wafer stepping techniques to achieve NMOS performance with CMOS low power. These three 256-Kbit families were introduced three months after Intel's 64-Kbit CHMOS DRAM. Basic chip versions are the 51C256H, which is aimed at high bandwidth applications; the 51C256L, a low power chip; and the 51C256HL, which strives to combine the low power/high performance attributes of its siblings. All three versions use a 256-Kbit x 1 organization.

These high density chips are pin-compatible with the 64-Kbit HMOS 2164A and with the recent CHMOS 64-Kbit DRAM ranks. Thus, a four-fold increase in memory is accomplished without major changes in software or system design.

Effective bandwidth on the 51C256H and 51C256HL is enhanced by fast access ripplemode operation. In one access, ripplemode allows random read/write of up to 512 bits within a single row (see article, "CMOS 256-Kbit RAMs Are Fast and Use Less Power," *Computer Design*, Aug 1984, p 133 ). This contrasts with the 4-bit, "nibble" operation. Graphics displays are pegged as an immediate application requiring the bandwidth offered by the 51C256H and 51C256HL. The 51C256H has a 120-ns access time and a 65-ns ripplemode cycle time.

The choice of CHMOS over NMOS offers the benefits of reduced power requirements. The low power 51C256L needs only 230  $\mu$ A for data retention. This is about 1/20 the current required by comparable NMOS devices. CHMOS allows use of internal static circuits for improved addressability, as in the ripplemode, without the power penalty that NMOS would incur.

These devices are currently available. Another 256-Kbit CHMOS DRAM—the 51C259, which features a static column address mode with 64-Kbit x 4 organization—is available for sampling. Quantity-100 prices start at \$115.45 for the 51C256H, \$141.10 for the 51C256L, and \$160.30 for the 51C256HL. **Intel Corp**, 3065 Bowers Ave, Santa Clara, CA 95051.

**Circle 301**

# Welcome the newest member of the Panasonic non-impact printer family.

Meet the EUY-3T, the new Panasonic Non-Impact Printer that's minimal in size but not in capability. It prints 40 alphanumeric characters on 80mm paper. Offers thermal printer performance with dot addressable graphics capability. And low power requirements (just 5V/2.5A) make it very economical to operate.

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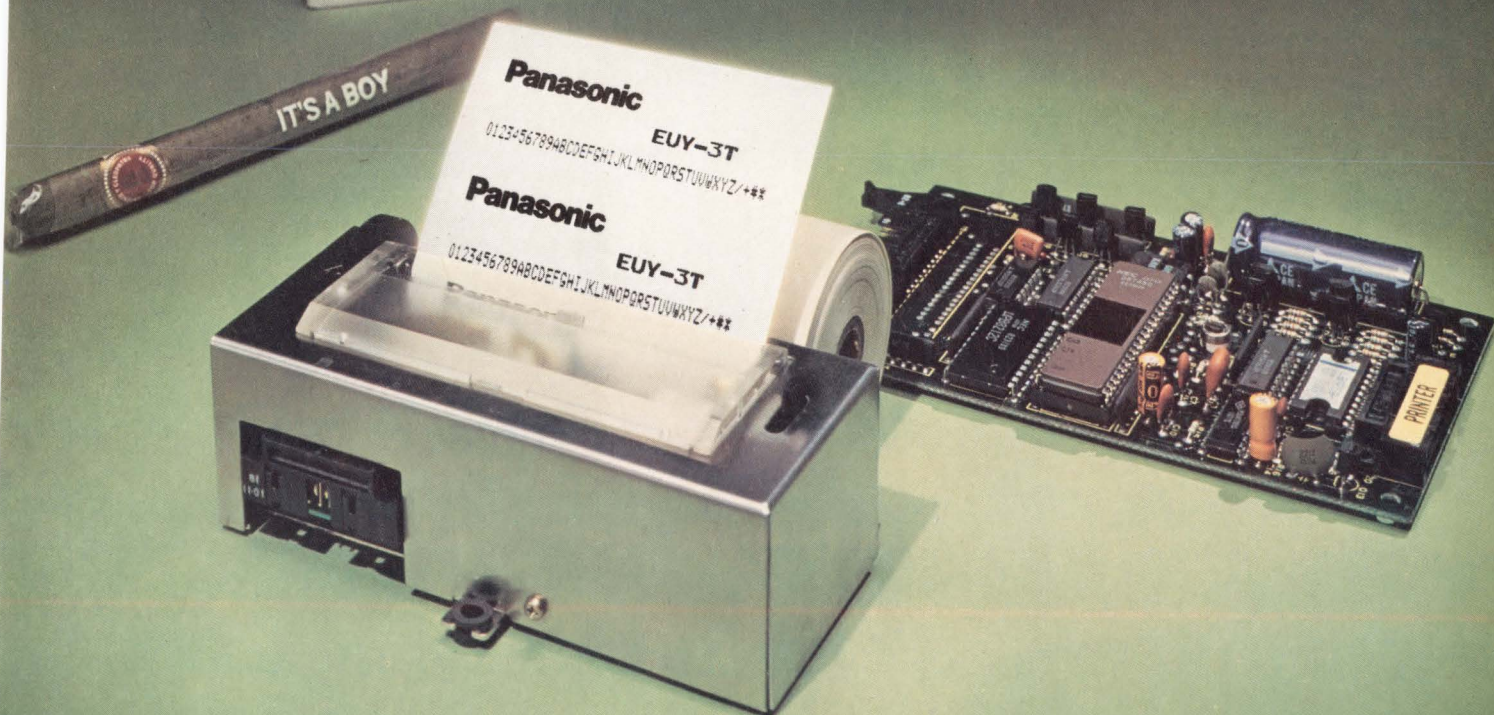
All Panasonic Non-Impact Printers have low all-DC power requirements. And our microprocessor interface modules accept 8-bit Parallel or byte Serial data input (model 3T is also Centronics-compatible). So they're perfect for ATE, printing calculators or other designs requiring low-cost hard copy.

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EUY-10	15, 21, 32, 40	60mm	90.4 x 42.4 x 110 mm
EUY-5	32, 40, 64, 80	127mm	195 x 65 x 70.1 mm

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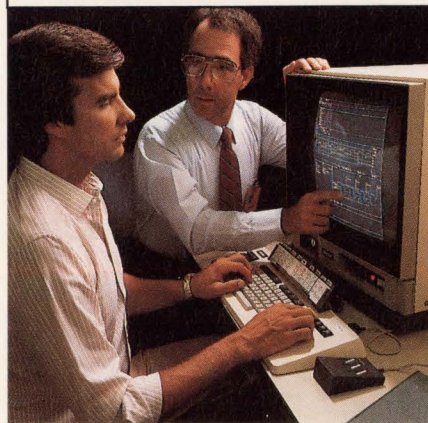
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## Benchmark Study

	Execution Time ( $\mu$ s)		Code Efficiency	
	63B01	8051/ 80C51	63B01	8051/ 80C51
$\chi$ TAL (MHz)	8	12	8	12
Instruction Cycle Time ( $\mu$ s)	0.5	1	0.5	1
<b>TASK</b>				
Binary Multiply	39	42	37	43
Bit Manipulation	6.5	6	8	8
Logical Operations (AND/OR)	7	3	11	6
Nibble Comparison	11	12	29	29
Interrupt Processing	11.5	21	1	19
<b>TOTALS</b>	<b>75</b>	<b>84</b>	<b>86</b>	<b>105</b>

Execution time for the 6301 ranges from 0.5  $\mu$ s (2 MHz) to 1  $\mu$ s (1 MHz) depending on the model, at a wide range of operation:  $V_{CC} = 3V$  to 6V. And an error-detecting function prevents illegal op-code and illegal addresses.

Other enhancements of the 6300 Family include upward source and object code compatibility with the HD6800 and bus compatibility with the MC6800 Family.

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Hitachi's comprehensive development support includes evaluation kits, emulators, prototyping devices, and cross-software packages running under

CP/M on personal computers and under ISIS-II on Intel development systems.

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The 6301 has been in mass production for more than two years. Five million units are now the brains behind hand-held terminals, briefcase computers, printers, digital switches, phones, modems, and automotive spark control computers.

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HD63P01	Piggyback EPROM

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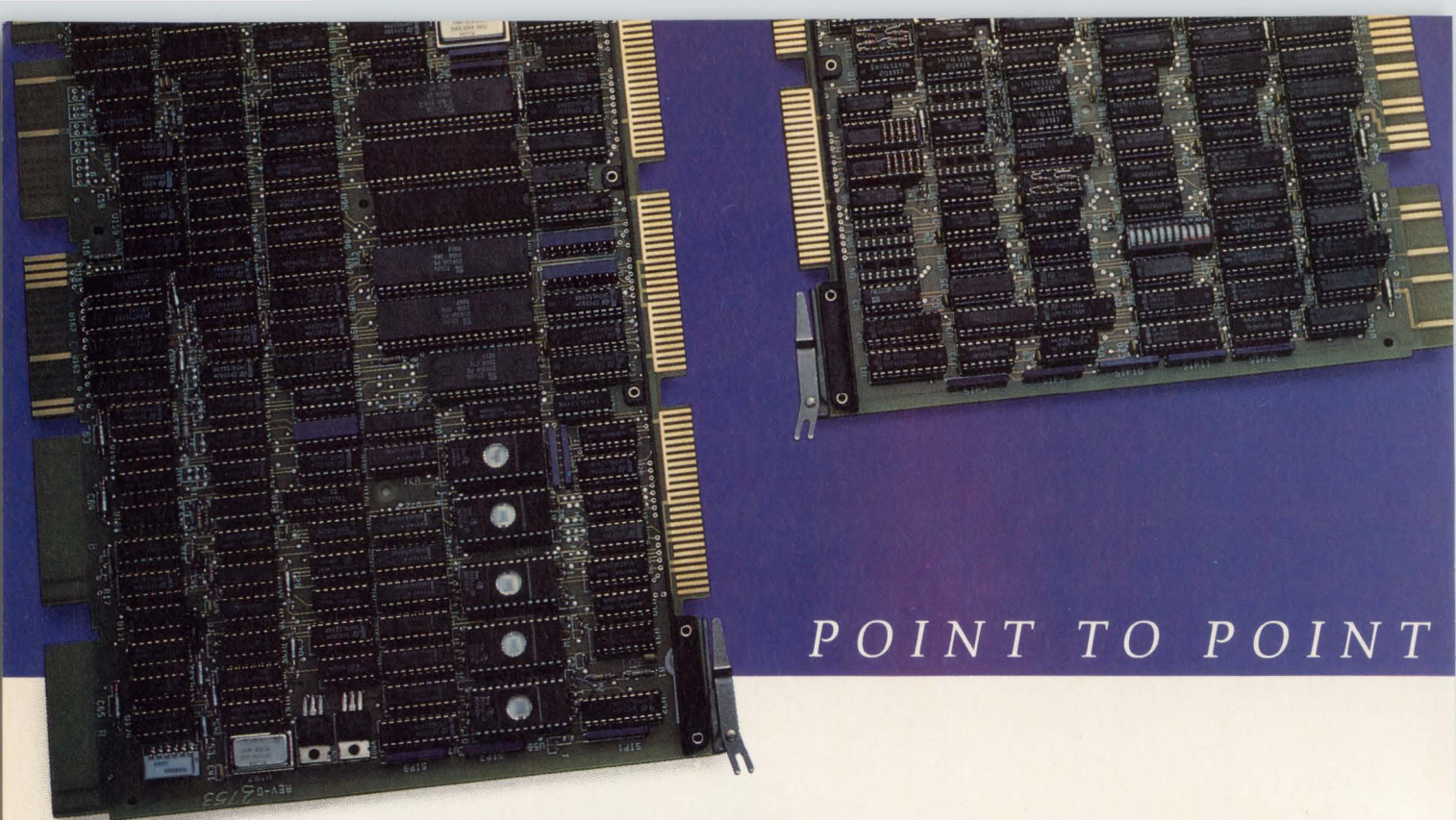
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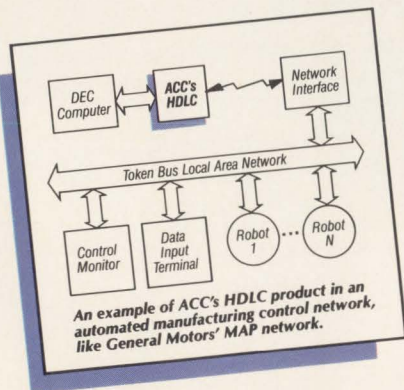
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# DATA COMM NETWORKS FINALLY COME OF AGE

The data link issue seems to have settled down with the realization that some links are better suited to some applications than others.

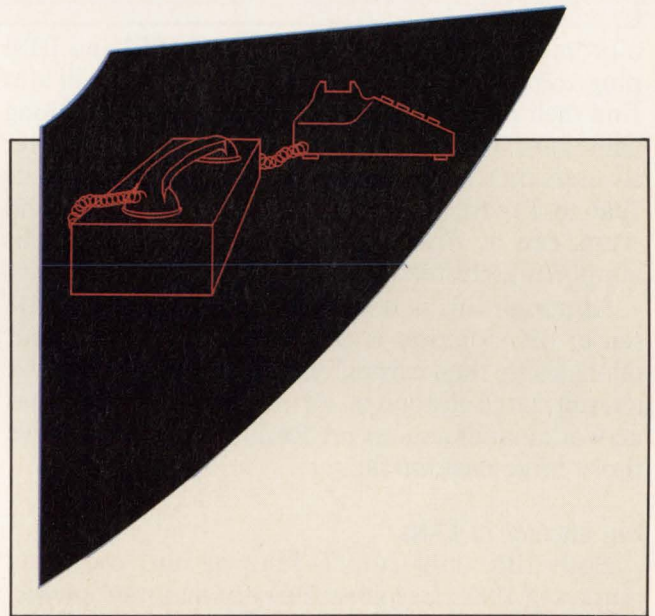
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by Tom Williams, West Coast Managing Editor  
and Richard Goering, Field Editor

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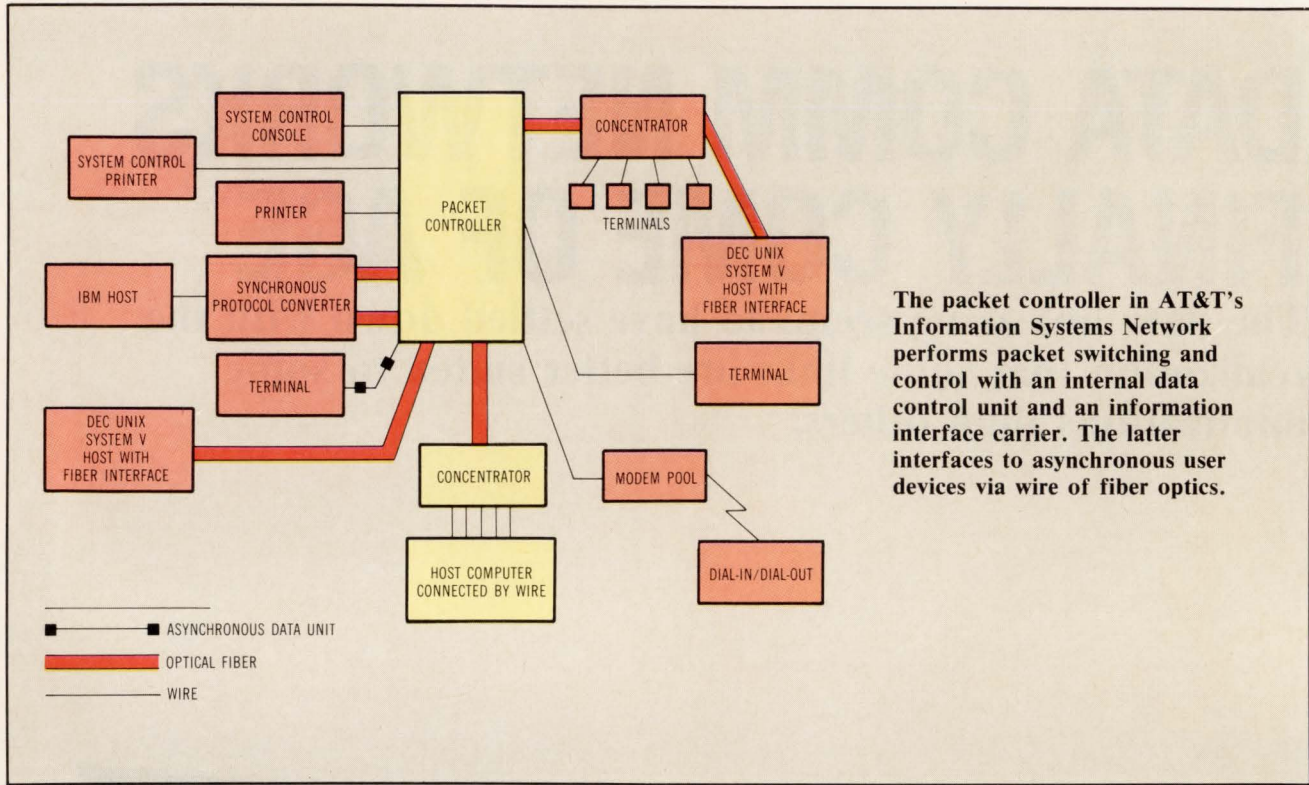
The past year has witnessed a major maturation in data communications—particularly in local area networks. The issue of the data link layer of the International Standards Organization model appears almost settled. It is taking the form of a hierarchy of standards specific to certain application areas. In addition, IBM has played a major card in announcing its token-ring system. This was not only a big psychological step—the blessing of Big Blue—but it will have a profound influence on the market and manufacturing decisions of many companies waiting for the word. As if that were not enough, AT&T has also made some major announcements in both the Ethernet and packet switching network areas.

Even before IBM's announcement, however, some large U.S. corporations had made the decision to commit to major network installations. The installation of what can be termed "production networks" has resulted from settling the data link issue (the second ISO layer). This has also provided a strong impetus for future *de facto* agreements—and quite probably standards—on the higher layers. Other major issues concerning data communications in general include software and standards, gateways



between networks, and the microcomputer-to-mainframe connection.

The data link issue in LANs seems to have settled down to general agreement that specific data links are better suited to some applications than others. Ethernet baseband, for example, appears to be conquering the office environment. At the same time, new controllers, chips, and clustering schemes are making the connection of a workstation to the net an inexpensive and straightforward process. Token-bus arrangements are on the increase in the factory environment, while IBM's token ring will assume



The packet controller in AT&T's Information Systems Network performs packet switching and control with an internal data control unit and an information interface carrier. The latter interfaces to asynchronous user devices via wire of fiber optics.

a prominent position in the arena of IBM and IBM plug-compatible machines. Broadband nets will also find their place in large environments requiring long cable runs, or where a company may want to cluster its users on a private branch exchange and interface that to Ethernet. As an alternative, a broadband trunk can be fitted with lower cost baseband ribs supporting clusters.

Although this is not standardization in the true sense, the situation is certainly more orderly and manageable than existed only a year or two ago. As a result, large customers are installing networks, and network manufacturers are forming alliances to serve those large customers.

**Big movers in LANs**

Both IBM and AT&T jumped into the LAN market in 1984. Despite a flurry of announcements, only one IBM LAN is currently available—the IBM cluster Kit, a baseband carrier sense multiple access/collision detection network for the PC, XT, AT, and PCjr. The long-awaited token-passing ring announced by IBM has been delayed until 1986 or 1987.

In the meantime, users will have to be content with the PC network, an adaptation of the Sytek (Mountain View, Calif) CSMA/CD broadband network. PC Network software, including the DOS 3.1 operating system, will be available in early 1985. Also slated for 1985 are the Industrial Network, a broadband token-passing bus, and the 3270-PC communi-

cation system that allows 3270-PCs to communicate with an IBM 3270 display controller.

The PC Network was a surprise to many users, partly because of its CSMA/CD broadband technology. One rationale for broadband is that it can support many channels at once, including voice, video, and data. But the PC Network only uses two channels, and its 2 Mbits/s speed is far below the capacity of the cable. IBM argues that it is trying to keep things simple by limiting channels and that 2 Mbits/s should be adequate for any likely use of the network.

IBM denies that the PC Network is a stopgap for the token-passing ring, but skepticism remains. IBM's own advertising portrays the token-passing ring as the company's major LAN offering. Although the PC Network can be extended to support 1000 users, IBM only provides a version that supports 72 users; those who want to install more modes will have to talk to Sytek or some other third-party vendor. Unlike the token-passing ring, the PC Network will hook up only with IBM products. Such restrictions as these have led some observers to conclude that the PC Network was intentionally "crippled" to protect the token-passing ring.

Nevertheless, the PC Network is competitively priced, and will provide a tough challenge for other companies in the PC networking business. Such companies as Dataquest (San Jose, Calif), Corvus (San Jose, Calif), and 3Com (Mountain View, Calif) will be feeling the heat—despite their claims of

optimism. When the PC Network was announced, virtually all would-be competitors said the same thing: IBM's announcement will open the market for LANs. That may be true; but how much room is left for competitors is another question.

The PC Network has been heralded as the first "cost-effective" broadband network for small LANs. Whether or not the claim is valid, the PC Network's real contribution may be the software. The lack of adequate software is still a big stumbling block for LANs. As a result, what IBM does with its PC Network software, scheduled for introduction in early 1985, will set a *de facto* standard for multi-user software in the PC environment. The real value of such networking will be realized when such applications as Lotus and dBase III run in a DOS 3.1 environment.

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*Wherever IBM goes, it seems to leave standards in its wake; the area of data communications is no exception.*

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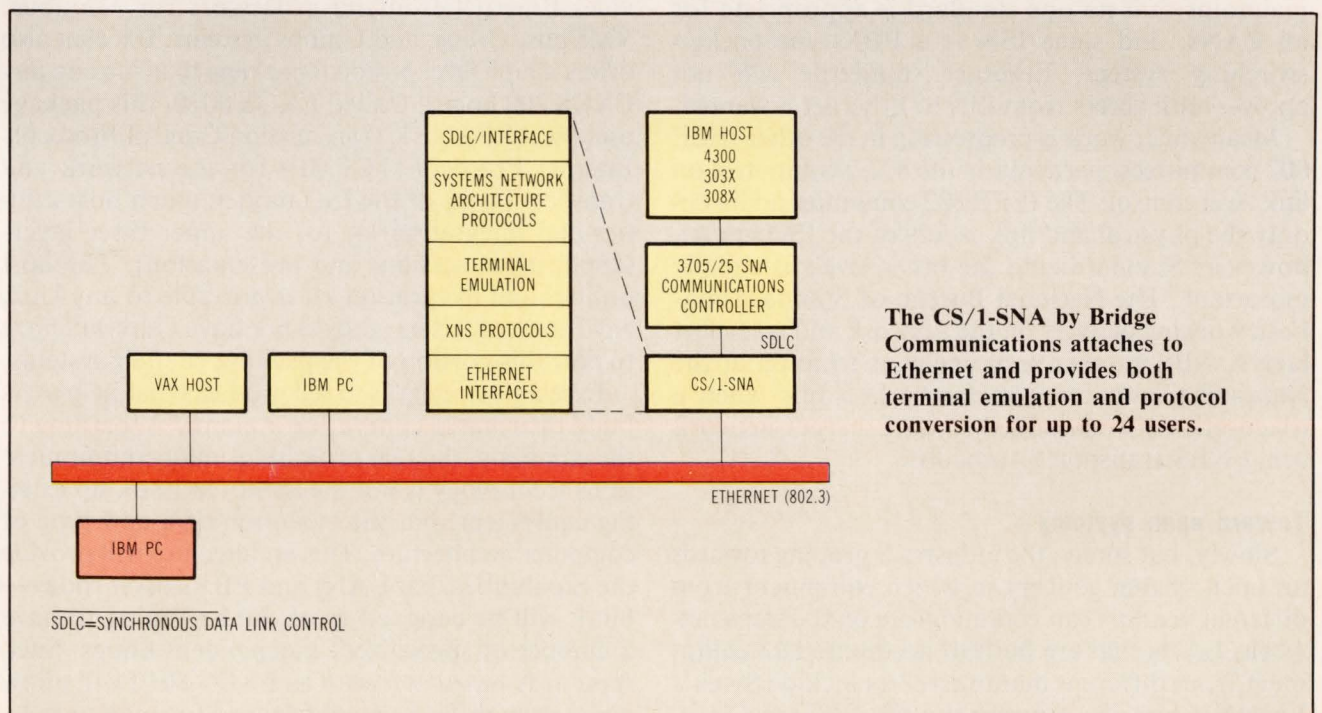
While the industry waits for PC Network software, AT&T's 3BNet is already up and running. This Unix-based, CSMA/CD Ethernet network accommodates non-AT&T computers with an ordinary Ethernet interface. Vendors of non-AT&T Unix systems must write their own Unix drivers, a fairly routine task that does not require knowledge of AT&T computer architecture. AT&T provides an interface for its own 3B series of computers.

AT&T's second entry into the data communications market, the Information Systems Network (ISN), is a general-purpose LAN based on the Datakit private branch exchange switch. ISN uses twisted-pair copper wire and optical fiber, and provides a bandwidth of 8.64 Mbits/s. The access method, which uses a centralized bus, is said to be totally free of packet collisions. ISN will be available next month.

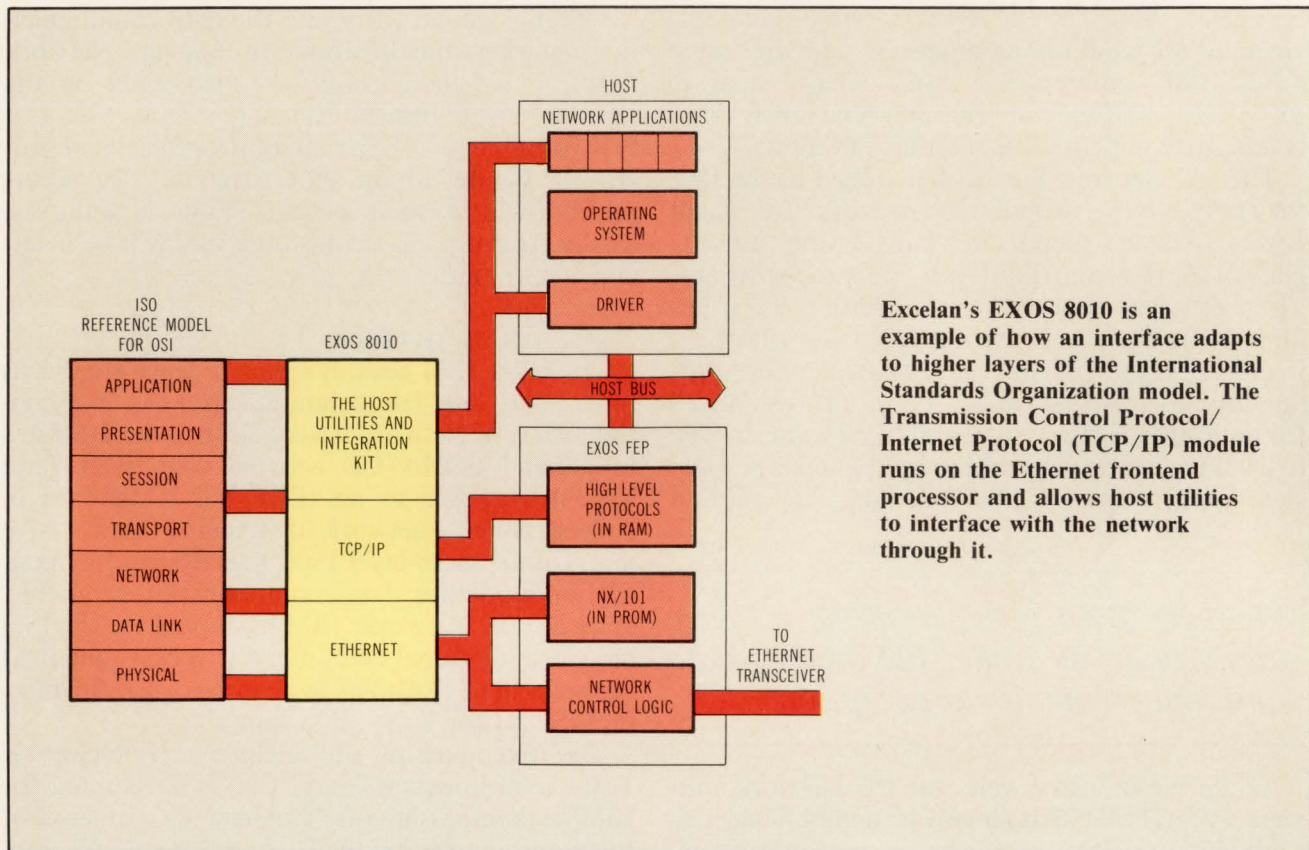
### The search for standards

Wherever IBM goes, it seems to leave standards in its wake, and data communications is no exception. The PC Network is very close to the 2-Mbit/s broadband CSMA/CD network that Sytek (and others) proposed as an IEEE 802.3 standard in August. Sytek's network implements the first five layers of the seven-layer ISO Open System Interconnection model for data communication protocols. With the PC Network, IBM has opted for the ISO model for personal computer networks—but IBM is not about to give up its Systems Network Architecture (SNA) for large scale computers.

The token-passing ring adapter, a five-chip set Texas Instruments (Dallas, Tex) is developing for IBM's token-passing ring, implements a superset of functions adapted by the IEEE 802.5 committee in August. However, the delay in introducing the token-passing ring is also holding up development of standards. This has led to charges that IBM is backpedaling in the 802.5 committee, after exerting considerable influence there. Moreover, the industry is still guessing which protocols IBM will use for its



**The CS/1-SNA by Bridge Communications attaches to Ethernet and provides both terminal emulation and protocol conversion for up to 24 users.**



Excelan's EXOS 8010 is an example of how an interface adapts to higher layers of the International Standards Organization model. The Transmission Control Protocol/Internet Protocol (TCP/IP) module runs on the Ethernet frontend processor and allows host utilities to interface with the network through it.

token-passing ring, and how the ring will interface with SNA. AT&T's 3BNet conforms to the IEEE 802.3 Ethernet standard. AT&T intends to adapt the upper level ISO protocols as they become available. However, ISN's independence from IEEE data communications standards raised some eyebrows. AT&T maintains that no one standard is appropriate for all LANs, and since ISN is a PBX-type packet-switching system, Ethernet standards will not apply—until access from ISN to Ethernet is wanted.

Meanwhile, work is progressing in the other IEEE 802 committees, particularly the 802.2 committee on link level control. The IEEE 802 committee addresses only the physical and link layers of the ISO model, however. Standardizing the other levels is equally important. The National Bureau of Standards has been working actively on the network and transport layers. NBS enjoyed a moment of triumph at the National Computer Conference last July when a token-bus network talked to an Ethernet network using NBS transport protocols.

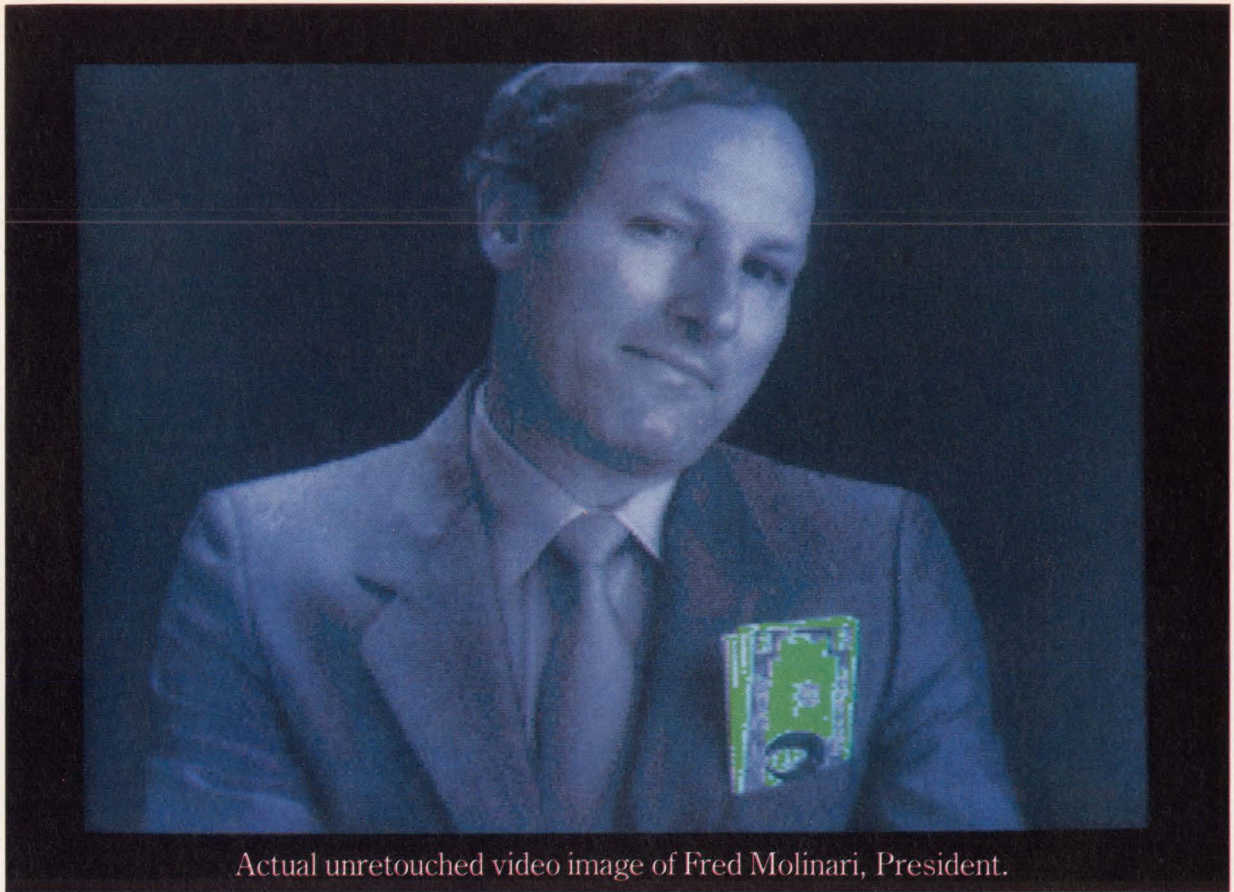
### Toward open systems

Slowly, but surely, the industry is groping towards an open system concept in which equipment from different vendors can communicate on the same network. LANs that are built to accommodate equipment from different manufacturers include Sytek's LocalNet and the Ungermann-Bass (Santa Clara,

Calif) NetOne package, now available in baseband and broadband, using both optical fiber and coaxial cable media.

A number of products have been introduced to help users build integrated systems. For example, the Excelan (San Jose, Calif) EXOS 200 series provides Ethernet frontend processors for Multibus, VMEbus, Q-bus, and Unibus systems. Excelan also offers a high level protocol package that runs on any EXOS 200 board. Called EXOS 8010, this package uses the ARPANET Transmission Control Protocol/Internet Protocol (TCP/IP) for the network and transport layers of the ISO model, and a host utilities and integration kit for the upper three layers (application, session, and presentation). The host utilities and integration kit is portable to any Unix environment. Users who do not have Unix will have to port this portion of the package to their systems.

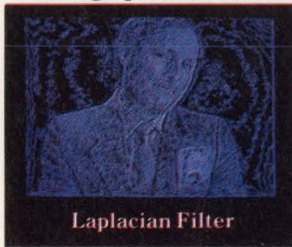
Excelan's strategy is to sell products that help users build distributed computing systems. According to the company, the real promise of data communications technology is not the ability to hook up existing equipment, but the evolution of a new type of computer architecture. This architecture will provide the capabilities that LANs and PBXs offer today—but it will be designed from the beginning to have a number of specialized, independent nodes. Such standards-based software as EXOS 8010 will allow nodes from different manufacturers to communicate.



Actual unretouched video image of Fred Molinari, President.

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CIRCLE 70

There seems little doubt that the network will be the means for connecting personal computers to corporate mainframes. The only question is where the terminal emulation is to take place. One solution, of course, is to use the power of the personal computer to provide users with a terminal just like the one required by their mainframe. Systems of this type are available from Direct (Sunnyvale, Calif). Direct produces an IBM PC look-alike that requires a terminal-specific plug-in card to emulate IBM or Hewlett-Packard terminals.

The other approach uses a more or less central controller attached to the network to perform emulations. The advantage here is that one controller, such as the CS/1-SNA made by Bridge Communications (Mountain View, Calif), can run many different terminal emulations that are available to up to 24 users. It also allows the user to switch between different mainframes on the same network without worrying about which terminal to emulate or what mainframe-specific protocols to run. In addition, if the user's personal computer supports windows, it is possible to have different terminal emulations running simultaneously on the same screen.

### Protocol wars

At this point, networks seem to be moving closer to compatibility at the cable level—taking into account the limits just outlined. But that still does not mean they can talk to each other. Much work remains at the higher levels of the ISO model.

The next area of tacit agreement on applications-specific standards will be, most probably, the next higher level of the ISO. This will usher in what could

be termed "protocol wars." In addition to the transport layer standards under review by such standards organizations as the NBS and the European Computer Manufacturers Association, some manufacturers could not wait and their protocols are finding wide acceptance. These include the XNS protocol by Xerox used in its Star system. XNS will probably become more widely used as the basic Star system makes inroads in the marketplace in the form of a Xerox Star-based computer aided engineering workstation system by Versatec (Sunnyvale, Calif).

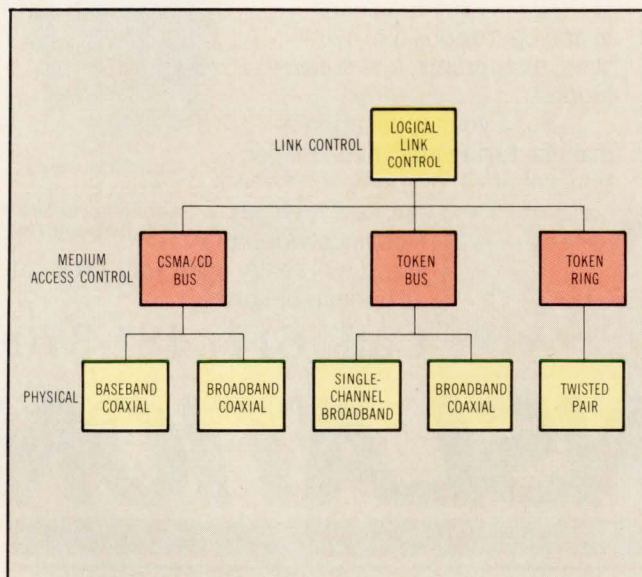
The most widespread protocol among CAE workstations, however, is TCP/IP, and is also the one the U.S. Department of Defense has specified. One reason for TCP/IP's popularity is that it comes as a part of Berkeley Unix—the operating system of choice of the engineering workstation industry. It is, therefore, free and easy to install. The Berkeley package also comes with Multibus drivers already written, and it is natural to use it to communicate over Ethernet.

Yet another protocol that seems firmly entrenched is Digital Equipment Corp's DECnet. This is the Ethernet protocol used by all DEC equipment and, of course, by all equipment built to run in the DEC environment. All these protocols are similar enough to coexist on the same cable, but are too dissimilar to talk to each other.

Given this state of affairs, a replay of what happened recently at the data link level is likely to occur on the transport level. The only protocol standard that has a chance of achieving dominance is the ISO standard itself. By the time dominance is established, however, a heavy investment in other protocols will have taken place. These protocols will always have their own markets, and probably will always be standard in their niches.

Such equipment manufacturers as 3Com, Bridge Communications, and Interlan are not as concerned about standards—they are more interested in having the issues settled so they can gear up for production. Now, they have to support all the popular protocols. Bill Carrico, president of Bridge Communications, believes alliances between companies will help settle some of the issues at the transport layer and beyond. His company and 3Com both support the XNS transport layer protocol, as well as the other three protocols, and have reached an agreement on how to do the next level—the session layer.

There seems to be some disagreement in the industry about how much data communication, especially LANs, will actually take place via digital PBX telephone-type systems. A great deal of activity exists in this area, however. National Semiconductor and Motorola, for example, are producing chip sets for PBX data switching; and manufacturers such as



The IEEE 802 committee's efforts are devoted to a variety of access control and physical media standards. These do not cover packet switching protocols, however.

Rolm Corp (Santa Clara, Calif) and Ztel (Wilmington, Mass) are producing highly intelligent PBX-based systems. IBM's recent purchase of Rolm would lead one to suspect that PBX has a definite future.

PBX makes sense because its wiring is usually in place and because the system is easily expandable. At the same time, however, fundamental questions exist about the feasibility of using PBX on a large scale. It is unclear at what point the volume of data traffic dictates more bandwidth than is economically possible with telephone switching equipment, and it has yet to be determined how to connect the PBX-type network into wider networks.

### Network competition

The first issue concerns clustering—competition will exist between the PBXs and less expensive coaxial systems such as National Semiconductor's CheaperNet. The second issue concerns gateways between networks. Many types of point-to-point gateways exist, including dedicated T-1 telephone cables and microwave links. Even such terminal emulator/protocol translators as Bridge Communication's CS/1-SNA can be considered a gateway. In providing the emulation, it gives users access to the IBM SNA world as well as the DEC VAX world.

A true PBX-to-LAN gateway could be in the offing from the IBM-Rolm merger. A smooth link, having the necessary bandwidth, is needed between the telephone switching environment and the coaxial realm of Ethernet. Such a link must be transparent to both the Ethernet and packet switching user.

Such circuit-switched networks as the Datakit by Western Electric (upon which AT&T's ISN is based) and the Elite One by Doelz Networks (Irvine, Calif) approach this problem by attaching their own control and routing information to the packets of user messages. This encapsulates the protocols that are used at the terminal interface or at the interface to another network.

This implies the need for extensive network management that can be centralized in a star configuration (as in the Datakit), or distributed among nodes in the system, with nodes reporting to a master node (as in the Elite One system). All these present different problems than those existing in an Ethernet type of environment.

It appears as though the world will be treated to both, and standards will have to be worked out for packet switched systems, Ethernet systems, and the bridges between them. Nevertheless, long before the committees end their deliberations the giants that have already made a commitment to all phases of data communications will have set the course for the future.

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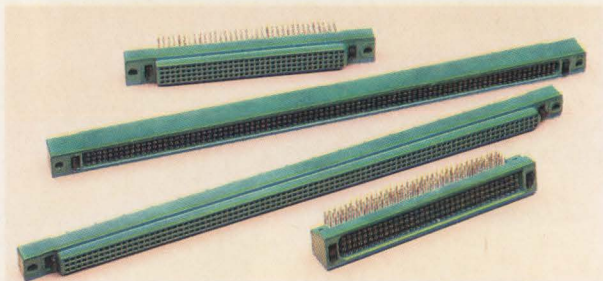
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## Simpler clusters emerge as local area network alternatives

Monolithic local area networks may give way to a cluster concept. Based on multiple clusters, each operating within narrow geographical and organizational boundaries, the concept simplifies peripheral sharing and cuts connect costs. Simplicity results from tying fewer terminals together. The cost per connection is reduced because less data travels shorter distances at slower speeds.

This cost reduction is the goal of vendors such as AST Research with PCNet, Network Development Corp with its Device Network Architecture, and IBM with its PC Cluster. These offerings serve fewer users (typically no more than 32) and run shorter distances than high speed networks such as Ethernet. However, they guarantee access to network resources with lower system overhead.

Meanwhile, a related development focuses on cheaper implementations of the IEEE 802.3 baseband (read: Ethernet) specifications. National Semiconductor hopes that its upcoming network controller chip set will find its way into "Cheapernet" systems using inexpensive RG58AU coaxial cable rather than the more costly RG50AU cable.

Clustering reduces the amount of traffic over high speed networks. Network traffic consists only of requests to central data bases and access to peripherals too expensive to dedicate to one cluster (eg, laser printers and SNA gateways).

Many local networks encourage contention among users since all users must contend for a single resource—the bus. Fairly inexpensive resources (eg, dot-matrix printers, 5¼-in. rigid disk drives) are connected to the same link as the expensive resources. As a result, it takes as much time to submit a print job to a \$600 printer as it would to a \$60,000 one.

Clusters promote efficiency by attacking connection costs that approach \$1000 per node for typical network implementations. Factors affecting these costs include the number of nodes on the network, network

topology, access control method, overall distances that the network must cover, and the transmission speeds needed to support many nodes over extended distances. Faster speeds are needed to shorten delay times between nodes.

Of these considerations, distance and the number of nodes have the most impact. Long distances require extensive transmission medium shielding so that spurious noise from the environment does not disrupt transmission.

This is the major reason that the RG50AU cable used for Ethernet is much more expensive than the RG58AU cable used in Cheapernet. The more expensive version allows packets to be sent as far as 5000 cable-ft. RG58AU, however, limits transmissions to 2000 cable-ft maximum. The less expensive cable cannot be used in noisy environments, such as wiring conduits and ventilation shafts.

Total distance also has an impact on the number of nodes supported because a minimum gap between nodes (eg, the 36 in. required in Ethernet) is needed for sufficient delay between transmissions. Dis-

tance affects transmission speeds in a similar manner by determining the amount of delay incurred in sending a message from one node to the other. Higher transmission speeds (such as the 10 Mbits/s dictated by Ethernet) are needed to support a large number of nodes in geographically dispersed locations.

Network controllers must be more sophisticated (and hence more expensive) when many nodes are interconnected. This is because the probability of collisions rises. Access control surfaces as an issue with more nodes contending for overtaxed bus bandwidth. Prevalent schemes used to handle this challenge—collision detection and token passing—incur significant overhead that may be bypassed if there is a decrease in the number of nodes.

Instead of relying on probabilistic schemes that determine access by generating random numbers (eg, Ethernet back-off), some Cheapernet vendors allocate predefined time slots to each user. The most popular schemes use the carrier sense multiple access (CSMA) method popularized by Ethernet. But they also

*(continued on page 180)*

Comparison of Clustered Networks

	Cheapernet	PCNet II	PC Cluster	Device Network Architecture
Transmit speed	10 Mbits/s	800 kbits/s	375 kbits/s	800 kbits/s
Topology	bus	bus	bus	bus
Access method	CSMA/CD*	CSMA/CA**	CSMA/CA**	polling
Transmission medium	coaxial cable	twisted-pair wire	coaxial cable	coaxial cable
Maximum no. of connections	512	160	64	64

\*Carrier sense multiple access/collision detection  
\*\*Carrier sense multiple access/collision avoidance

**Simpler clusters***(continued from page 179)*

employ collision avoidance techniques rather than collision detection.

With collision detection, more than one user can transmit a message concurrently. Errors are detected when collisions create a large voltage on the bus. Collision avoidance schemes, on the other hand, require that a user transmit a message request before actually sending the message.

National Semiconductor claims that collision avoidance schemes incur an overhead penalty not justified by traffic conditions. Design Manager R.V. Balakrishnan says that collision avoidance schemes work best in networks where transmissions tend to be "bursty" rather than sustained, and where peripheral services are seldom required. He notes that servicing mul-

iple requests on collision avoidance networks requires that the peripheral wait for its turn, as determined by the priority scheme. Here, collision detection networks are better suited since requests can be serviced as often as each peripheral can transmit a message. **National Semiconductor**, 2900 Semiconductor Dr, Santa Clara, CA 95051. **Circle 302**

**Protocol analyzer identifies data communication problems**

Fully compatible with family members 4955A and 4951A, the HP 4953A protocol analyzer has full remote control capability. The analyzer monitors data transmission and simulates network components. Moreover, it monitors bit-oriented protocols at speeds up to 256 kbits/s and provides complete simulation at speeds of 72 kbits/s without loss of triggering capability.

The analyzer displays X.25, X.75, DDCMP, BSC, HDLC, SDLC, and user-definable, character-asynchronous, and character-synchronous protocols. High speed protocol analysis needs include the ISDN's 144 kbits/s and computer-to-computer links at speeds to 250 kbits/s. Data codes are ASCII, EBCDIC, Baudot, EBCD, and Transcode. The user can define other data codes and store these codes on tape.

An intelligent 64-Kbyte buffer memory stores data, timing information, and lead status. A standard mass storage tape provides space for 512 Kbytes of data for later analysis. Actual data storage is greater because the analyzer can eliminate line delays without sacrificing timing information. With 63 triggers available simultaneously at full speed, the user can trap characters in real time or post process the data.

The soft keys let a new user work through setup and test menus easily. The keys present only appropriate choices at each decision point in a menu.

Multiple display formats include viewing and data interpretation in frame, packet, frame and packet,

data, and state—all with 2x display, among others. The display handles timing measurements directly, using cursor timing.

Cartridges store data, timing information, interface and lead status, menu configurations, custom data codes, and application programs. The entire contents of the buffer memory can be stored on a single data cartridge.

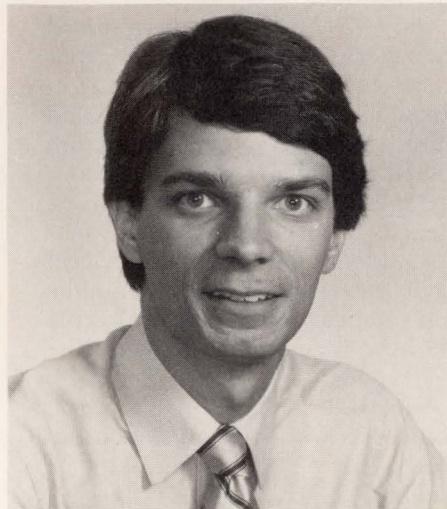
The display is a high resolution, 9-in. device, featuring 25 lines x 80 chars. Double size characters are selectable. A full ASCII keyboard pivots and locks at any angle for

pivots and locks at any angle for desk, bench, rack, or floor standing operation. Separate from the interface port is the RS-232-C/V.24 interface for instrument control. Direct hardcopy output of all normal size displays to an HP 2671G or HP 2673A printer is standard.

The HP 4953A is priced at \$12,000. Option 001 extended memory is \$1000. Interface pods (RS-232-C/V.24, RS-449, MIE188C, RS-422) are \$950 each. Option 003 Katakana keyboard is \$250. **Hewlett-Packard Co**, 1820 Embarcadero Rd, Palo Alto, CA 94303. **Circle 303**



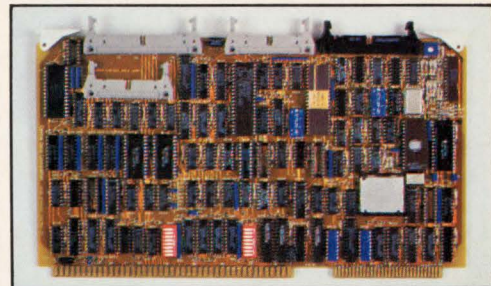
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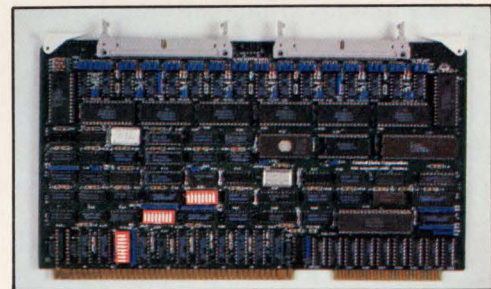
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The new **High Performance Terminal Controller** can operate at 9600 baud-full duplex to all eight channels without loss of input characters. Each channel can be programmed for baud rates to 19.2Kb. The powerful Intel 8088 processor handles all I/O interrupts, freeing time for the host processor. 64K of dual-port RAM is used as buffers for data in and out, with bus lock and parity error detection supported on both ports. Bus-vectored and non-bus-vectored interrupt modes are supported. And for maximum convenience and reliability, the board comes complete with two 60-pin locking right angle headers. The **B1031** is available in 100 up pricing at \$705.



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## Frontend processor mixes VAX and packet-switched domains

Local and remote terminal users move freely between Digital Equipment Corp's VAX-11 computers and packet-switched networks with a frontend communication processor from Advanced Computer Communications. The IF-11/X.25 Plus handles any necessary packet assembly and disassembly that is called for in the X.25 specification, as well as in necessary terminal protocols, without host intervention.

Such transparency results from the ability to emulate a terminal multiplexer, such as the DH-11. Few modifications to existing software drivers are needed. Furthermore, the host computer cannot distinguish between attached and remote terminals.

Remote terminal access is the most straightforward of the two modes, since the 32 data ports dedicated on the host computer handle just incoming calls. Local terminals require additional hardware support since they can initiate X.25 conversations as well as converse with the host system. As a result, the IF-11/X.25 Plus allocates one of the 32 channels for each attached terminal, with the re-

maining channels free to support remote terminals.

Under either hardware configuration, remote users initiate a terminal session by placing a call to the desired network node. Packet switched networks typically use dial-up lines for these incoming calls, with RS-232 serial communications used as the physical link. Messages are transmitted across the network at 56 kbits/s. Incoming calls can either choose a specific port address (1 to 32) or allow the controller to assign the lowest port address available.

In addition to routing incoming calls to the appropriate port address, the controller handles packet assembly and disassembly (PAD) functions. The data link established at layer 2 is divided into 32 logical channels. These channels identify individual user conversations that have been combined for transmission over a single trunk line within the packet network.

Packets also contain session and presentation-dependent information such as baud rate and terminal characteristics (ISO layers 5 and 6). Moreover, the IF-11/X.25 Plus trans-

lates these parameters (set forth in the X.3 and X.28 specifications) into specific terminal protocols (eg, VT100). If necessary, users can reconfigure a remote network node with parameters defined in the X.29 specification.

Only when the user enters a special character sequence does the controller come into play. The user, in effect, disconnects from the host and further terminal communications are routed to the controller for action. Special PAD commands are then used to connect an X.25 data network, as well as to move back to local mode for further interaction with the host computer. Users need not log off the host system at all to enter the PAD mode.

The IF-11/X.25 Plus occupies a double hex-width Unibus slot on any PDP-11 or VAX-11 minicomputer running RSX-11, VMS, or Unix operating systems. **Advanced Computer Communications**, 720 Santa Barbara St., Santa Barbara, CA, 93101.

Circle 304

## Circuit-switched networks connect like telephones

Data transmissions as simple as dialing a telephone could be possible with circuit-switched networks. By specifying the destination address prior to actual transmission, these networks establish virtual circuits. As can be seen, this operation is similar to dialing a telephone number before actually talking on the phone.

When compared to packet-switched networks (eg, X.25), this approach has lower overhead and higher potential throughput. Packet sizes are smaller during transmission since the destination address is already specified. Thus, throughput increases because the packet need not be disassembled and reassembled at each node. Treating packets as bit streams

also frees these networks from user protocols and transmission speeds.

According to Frank Conners of Doelz Networks, fragmentation occurs as designers attempt to connect disparate local area networks (LANs) with wide area networks (WANs) and other means of data distribution. In Band-Aid fashion, bridges connect separate LANs with gateways providing similar services when networks use incompatible protocols and transmission speeds (eg, Ethernet to X.25).

Such measures are necessary because present networks entangle message formats and transmission schemes with the data. These formats and schemes must be translated when moving data from one network to

another. Furthermore, physical medium and transmission speed greatly influence both the format and transmission scheme of each network implementation. For example, the carrier sense multiple access (CSMA) scheme used in Ethernet networks could not work in the noisy environment of voice-grade telephone lines. Likewise, a token-ring scheme would be inappropriate for the high throughput required in a public data network such as Tymnet.

Such tedious deliberations are akin to worrying about whether the mailman's truck uses gasoline or diesel, according to Conners. They should have no direct bearing on the physical act of moving bits from one point to

another. Circuit switching takes a different approach by treating data as a continuous byte stream rather than as a distinct object (or message), as current networks do.

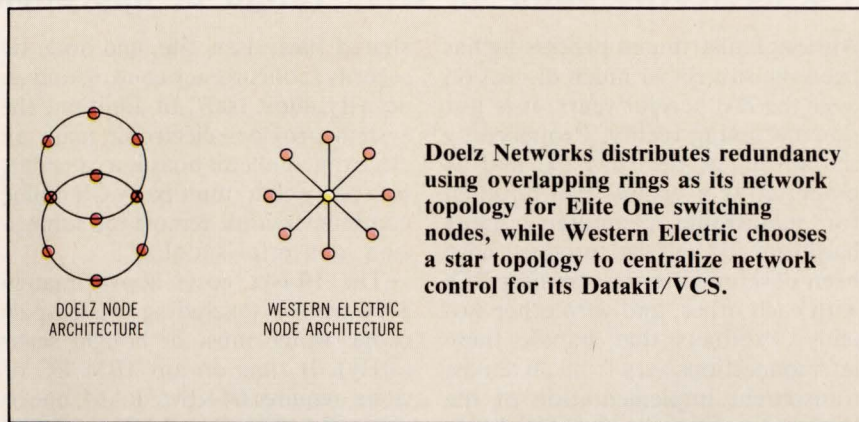
In fact, both Datakit/visually coupled system (VCS) from Western Electric and Elite One from Doelz Networks make no effort to obtain control and routing information from user messages. Rather, they append their own control blocks to the messages and transmit these transparent to user-defined protocols, transmission rates, and physical media. Only at the terminal interface is the bit stream transformed back into messages that contain such information.

Network packets are kept small to maintain fast network response, but are big enough to avoid excessive overhead for control and addressing. Under the Datakit scheme, data is formatted in 9-bit bytes (with one bit used for control), with as many as 16 such bytes tied together to yield longer packets.

On the other hand, Doelz uses normal 8-bit bytes for its 24-byte packet. Of this total, 19 bytes are reserved for data with the remaining 5 bytes containing cyclic redundancy check codes and control and address information. As many as 16 such packets can be linked for longer transmissions.

Datakit and Elite One also differ in the number of channels supported. In the first case, a single channel (as in Ethernet) is the physical link where terminals compete for access. Elite One has two data links, each with four logical channels transmitted end-to-end. Contention resolution is the primary means to determine network access in Datakit. Meanwhile, the Elite One supports four user-defined priority levels.

Specifically, Datakit uses address comparison rather than a CSMA scheme implemented in Ethernet. Two contending terminals have their respective interface modules transmit a binary address to the switch control module, where it is altered. Comparing the two transformed addresses bit-by-bit eventually eliminates one



**Doelz Networks distributes redundancy using overlapping rings as its network topology for Elite One switching nodes, while Western Electric chooses a star topology to centralize network control for its Datakit/VCS.**

terminal, thereby giving the other terminal access to the switch.

Similarly, the Doelz approach leaves network access in the hands of the Elite One switching concentrator, with some help from the user. Each packet has a user-assigned priority level attached to it. This is checked as the packet is passed from node to node. It can be placed on a queue in the node processor if a packet already in the queue has a higher priority. In that case, the node processor then transmits the packet with the higher priority. A watchdog timer on the node processor can also cause a packet to be placed on the queue if another packet has waited a long time.

Another difference between the Doelz and Western Electric approach focuses on network topology. Western Electric implements a star-cluster configuration with network administration handled by a single node. On the other hand, Doelz places its nodes in overlapping rings, with one node also handling network administration. At issue is the ability of the network to recover from breaks in the link, or the elimination of nodes.

In a ring configuration, dual paths are available to each node starting at any point on the ring and moving either clockwise or counterclockwise. If a node or link is broken, an alternate path is always available to reach the other nodes on the ring. Overlapping each ring also provides two separate paths across individual networks through different nodes. Redundancy is an integral part of the design.

On the other hand, a star cluster provides point-to-point connections between nodes through a single point. The loss of a link or the central node cannot be as easily bypassed. Redundancy must be consciously planned in the duplication of the physical links as well as elements of the central node to provide the same level of reliability found in the ring topology. A key advantage of the star cluster is centralized control, according to James Hahn, one of the architects of Datakit/VCS. Ring topologies typically required distributed control necessitating more software implementation.

As far as physical implementations go, a typical Datakit network consists of synchronous and asynchronous terminals (with host computers) connected to dedicated interface modules. These modules reside in a single cabinet (the VCS) node with the trunk interface, switch, switch control, and timing modules. Dual 8 Mbits/s provide a measure of redundancy in case of component failure. Transmission rates range from 9.6 to 56 Kbits/s.

A typical network using Elite One packet-switching concentrators consists of multiple 6800 and 68000 microprocessors on a single card with dual buses providing the interconnect. Transmission rates will range from 56 to 1.544 Mbits/s. **Doelz Networks**, 18581 Teller Ave, Irvine, CA 92715; **Western Electric**, 222 Broadway, New York, NY 10038.

**Doelz Networks—Circle 305**  
**Western Electric—Circle 306**

## PC networks build on wide range of approaches

Although distributed processing has been the subject of much discussion over the last several years, it is just now becoming reality. Propelled by the advent of the IBM PC and its potential as a genius-level terminal for mainframe computers, many hardware and software products have been developed to interconnect PCs with each other, and with other systems. Products that handle these interconnections vary from an almost transparent implementation of the Ethernet protocol on twisted-pair lines, to a standalone program that communicates via a modem.

Using the Seeq Technology Ethernet protocol chip on a plug-in peripheral board for the PC bus, 10-Net from Fox Research implements Level 2 of the IEEE 802.3 standard. The protocol uses a carrier sense multiple access/collision avoidance (CSMA/CA) scheme to pass packet data at up to 1 Mbit/s over twisted-pair wires.

Connection to the net is simple. An electrical connection is made to the twisted pair, and the bottom cover is replaced on the box. Then, the lead-in cable is plugged into a socket, the card is plugged into the PC, a configuration program is run, and a log-in program is executed.

The supplied software is a generic modification of MS-DOS 2.0. At log-in time, and each time a net access is made to a "new" (not recently accessed) node, the system queries the net to determine which nodes are active. It then builds a table of node names. In effect, the file system of each PC or clone becomes a node in a shared root directory.

Each node is given a name (eg, "Fred" or "Accounting") at configuration time. This name is used by other nodes to access its files or devices over the network. Any node can access any hardware device on any node in the net, and no dedicated print, file, or communication server is needed.

A full complement of network management facilities is provided, including insertion and deletion in

shared files; user, file, and node ID security; concurrency control; and an activity audit trail. In addition, the system provides electronic mail, an electronic bulletin board, a calendar, two-party chat, multiparty CB online communications, remote job submission, and print spooling.

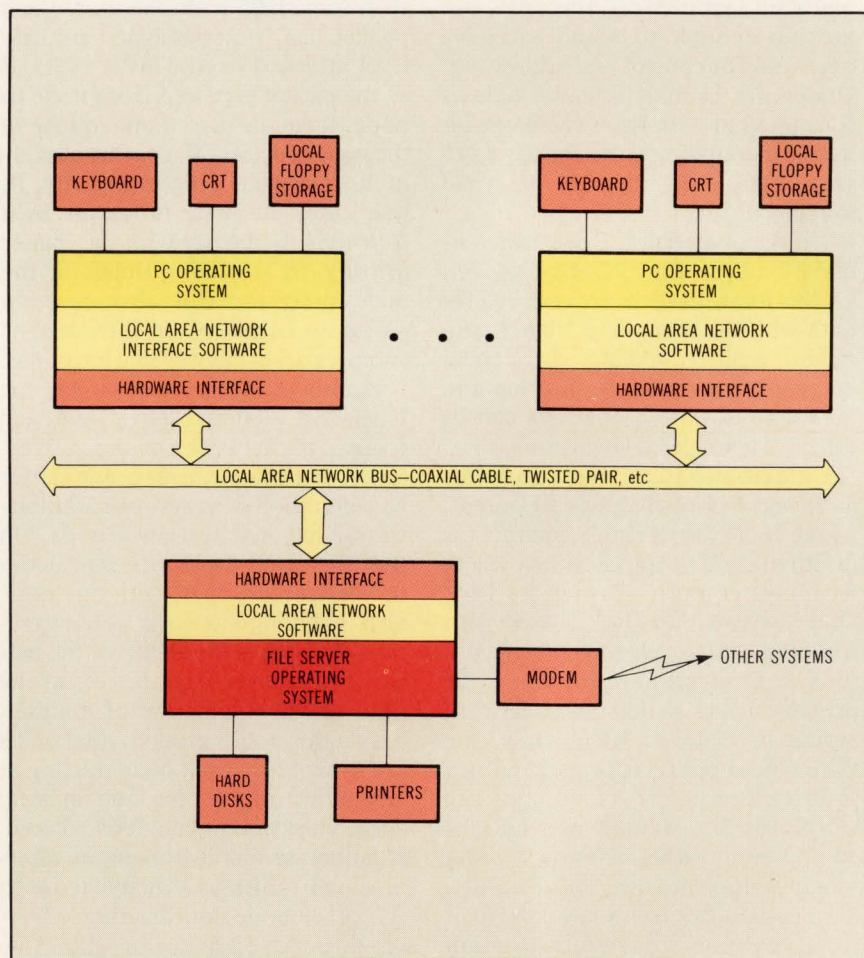
The 10-Net costs approximately \$700 per PC (excluding twisted-pair cable, which must be bought separately). It runs on any IBM PC or clone, requires 64-Kbyte RAM, one or more disk drives, and MS-DOS 2.0.

At a slightly less transparent level, NetWare/OS, from Novell, Inc, replaces the file-handling apparatus of the PC with a sophisticated file server. Tailored to support varieties

of PC-DOS, MS-DOS, CP/M-80, CP/M-86, and the UCSD p-System, it uses any of a number of network hardware systems. One of these is manufactured by the company to share files between PCs.

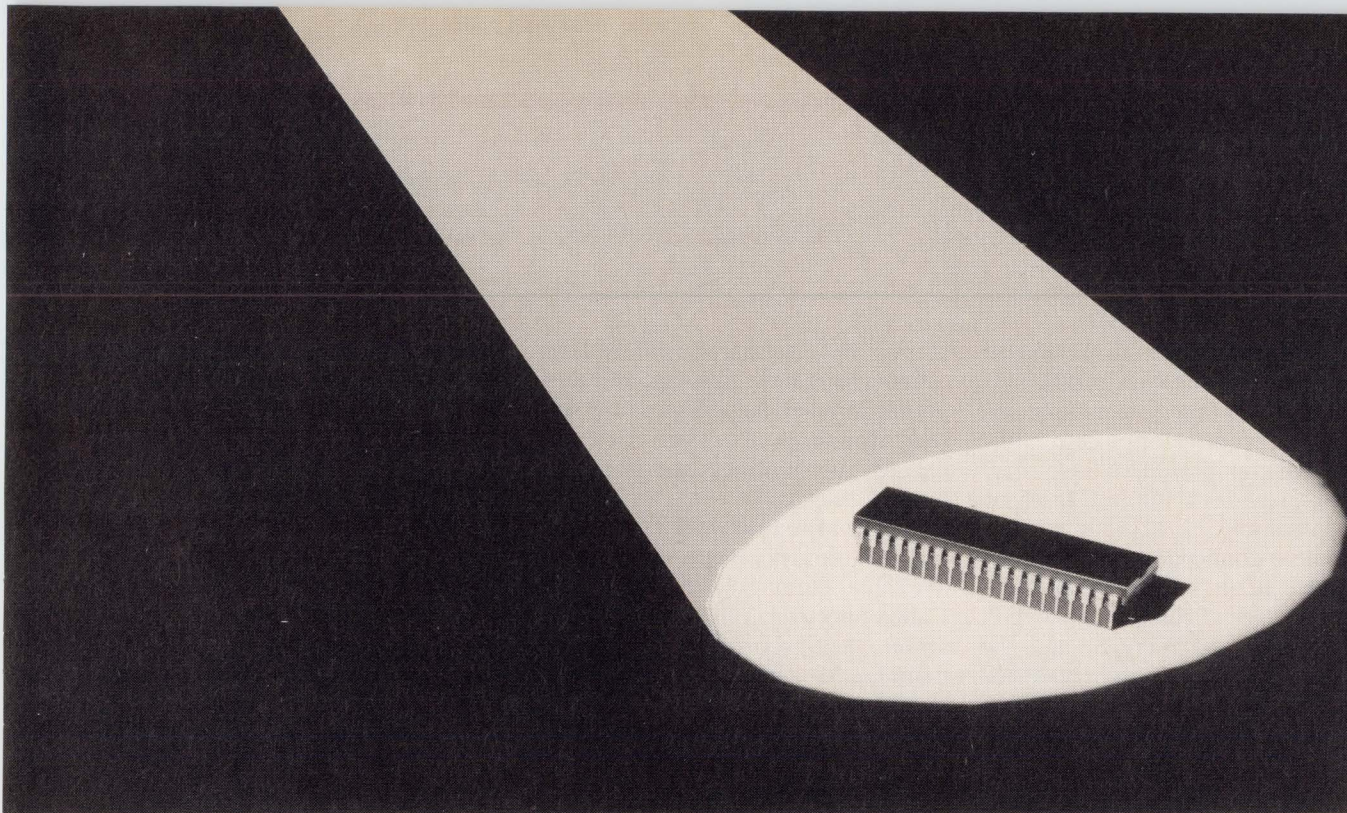
Based on what the company calls its Universal File Server, the operating system features ease of use through simple function utilities and extensive help files. One of these utilities allows disk storage on any PC to be segmented in various ways. Areas on disk can be allocated to different users or different operating systems, and still remain transparent to all users on the system, within limits. A log-on password lets a user have

*(continued on page 186)*



**In a general bus-oriented net, such as 10-Net or NetWare, individual PCs transfer files over a bus via a combination of hardware and software. One or more stations can serve as file or print servers.**





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**PC networks***(continued from page 184)*

access to specified files in the shared portions of the network's disk systems. The operating system maintains duplicate file directories and utilities to recover erased or lost files, and to provide a modest level of fault-tolerance.

Physical connections to Corvus's Omninet, 3Com's EtherLink, Gateways's G-Net, Proteon's proNET, Novell's own NetWare/S; and the ARCnet of Nestar, are provided through peripheral cards that plug into an expansion slot on the PC. Generally, one PC on the network acts as the central file and print server, handling requests from other nodes. Along with special hardware arrangements (usually a PROM on the peripheral card), this allows most of the PCs in the network to operate without local storage (their own disk drives), lowering the system cost.

Novell's NetWare/S is a self-contained computer with a Motorola 68000 CPU. It connects with the various PCs via twisted-pair cables, and manages up to 300 Mbytes of mass

storage and five shared printers. Disk caching, directory hashing, and seek optimization all help to speed file system throughput. Price varies according to the number and kind of options selected.

A specialized network server with application-generating software is available from Science Dynamics. Called Spectrum 700/Magix, the file server (the Spectrum 700 part of the name) is Multibus-based, and communicates with the PC workstations via either an Ethernet-type link or RS-232/422.

The server is built from standard Intel single-board computers and Multibus peripheral boards. A wide range of disk, tape, and printer interfaces is available from numerous vendors. Since the file server handles all file requests, the PC workstations can operate without disk drives.

The system is relatively expensive and has a high capacity. Without the Magix software (database and application generators), as well as an MS-DOS support gateway, it would

qualify as a separate computer system, rather than as a PC enhancement. The basic philosophy of the system is closer to traditional mainframe and minicomputer systems than it is to common PC applications.

The Magix software consists of several parts. These are: a database compiler written in C, a format definer to create or change the way reports are presented, and a database server to create, maintain, and update the data bases on the system.

Since it is an 8086-based system, the Spectrum 700 can load a copy of MS-DOS, and run generic application programs. This facility is useful and supplements a system that has been created to appeal to vendors of turnkey vertical applications. **Fox Research**, 7005 Corporate Way, Dayton, OH 45459; **Novell, Inc.**, 1170 N Industrial Park Dr, Orem, UT 84057; **Science Dynamics**, 2140 W 190th St, Torrance, CA 90504.

**Fox Research—Circle 307**  
**Novell, Inc—Circle 308**  
**Science Dynamics—Circle 309**

## Peripheral processor removes communication overhead from host

Providing high speed data communication, the SI08 intelligent processor uses eight serial channels to take over communication responsibilities from the main processor. It is designed for multi-user, multitasking systems such as Unix, RMX-86, and MPM-86. The Multibus-compatible serial communication module features a 16-bit 8088 microprocessor that handles all communications over eight serial channels. All channels are individually programmable and provide asynchronous, bisynchronous, HDLC, and SDLC operation.

A tri-port RAM architecture allows the user to place an onboard 16-Kbyte buffer anywhere in the 20-bit Multibus address space. Once the address is fixed, the tri-port memory can be accessed from any CPU on the Multi-

bus, the processor, or via the serial I/O channels through the DMA logic. Each of the eight input and eight output ports provides a separate DMA channel for continuous operation at a minimum of 9.6 kbaud. Each channel also handles full-duplex DMA operation without intervention by the onboard 8088 or the main system microprocessor.

In addition to the 16-Kbyte data buffer, the module contains a 1-Kbyte cache that operates on an internal local bus. The processor manipulates information in local memory using DMA. The 8088, therefore, reads and writes to the local memory together with DMA I/O and can provide no wait states with either memory access. The onboard 16-Kbyte memory is designed around a

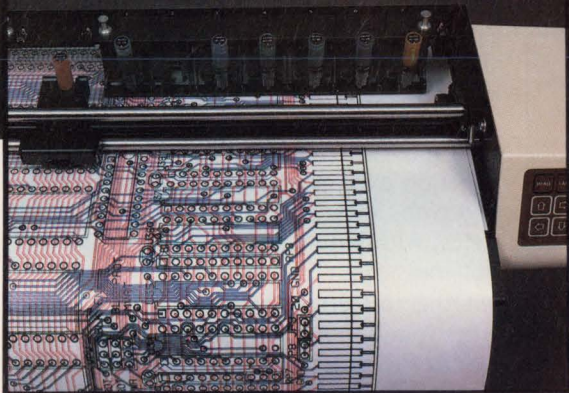
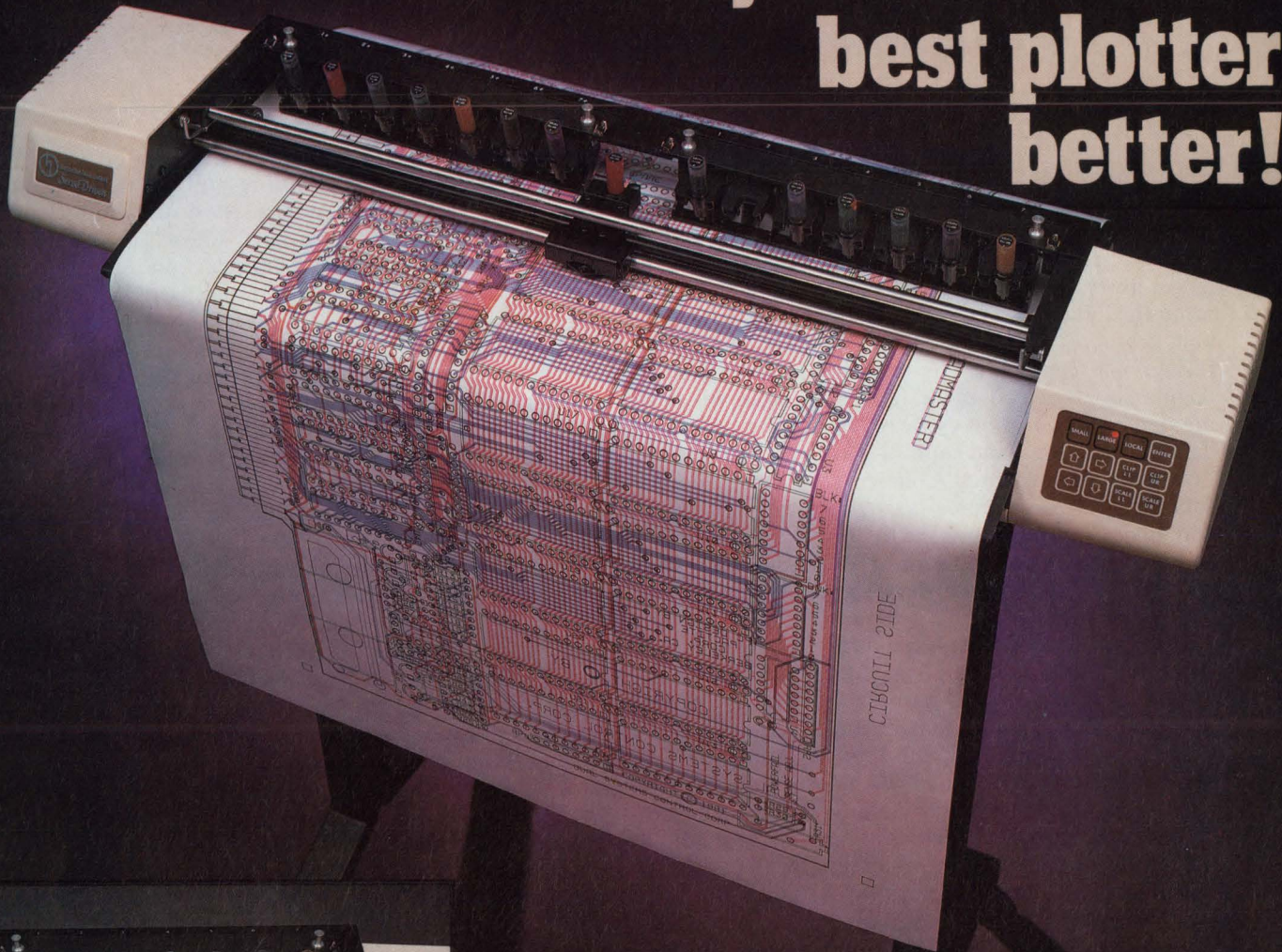
tri-port interface. Using a coprocessor I/O control-block technique, the host processor places information in the tri-port RAM and requests an I/O operation. The 8088 examines and analyzes the I/O requests and completes the operation without further host intervention. All operations can occur from the local buffer or from the Multibus.

Large blocks of information can transfer directly from Multibus main memory, completely bypassing the buffer. An option loads or removes data in the DMA mode from the buffer or from main memory on the Multibus.

The board costs \$2800 with immediate delivery. **Distributed Computer Systems**, 330 Bear Hill Rd, Waltham, MA 02154. **Circle 310**

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## Flexible modem protocols declare war on errors

Enhanced modem protocols promise error-free communication links between personal computers as well as between personal computers and larger hosts. These schemes provide more flexibility than currently available protocols (eg, XMODEM), offering such capabilities as message framing error detection and retransmission based on 16-bit cyclic redundancy check codes, and sophisticated flow-control procedures. Competing for industry acceptance are two announced specifications: the Microcom networking protocols, or MNP, and the X.PC specification developed by Tymnet, Inc.

However, a price must be paid for such functionality. Error detection and retransmission adds significant overhead to the actual data being transferred. In addition, both specifications rely on the host CPU within the personal computer for communication processing. In single-tasking operating systems, this forces other related application programs (eg, spreadsheets and word processing) to

be suspended until all data transmission comes to a halt.

The MNP specification supports data transfers as either byte streams or files. Framing techniques mark the beginning and end of each data unit. Likewise, the X.PC specification implements the data packet format called for in the International Consultative Committee for Telephone and Telegraph (CCITT) X.25 specifications for public networks. A file-transfer mechanism is not defined within X.PC, but the protocol does implement the required multiple data streams of the X.25 specification.

The same three-step procedure establishes links in both versions. First, the sender issues a link request to the receiving node. The receiver acknowledges the request by issuing its own link request, and the circuit is finally established when the caller issues a link acknowledgment. The link will not be established if a "not-acknowledge" is received anytime during this procedure. Once the link is established, the X.PC and MNP

specifications call for byte-oriented data transmission of each message. The formats follow the same basic two-part construction using a header and an optional user data portion. The header typically contains packet function type (eg, user data and link establish), message sequence numbers, and a 16-bit cyclic redundancy check (CRC) code.

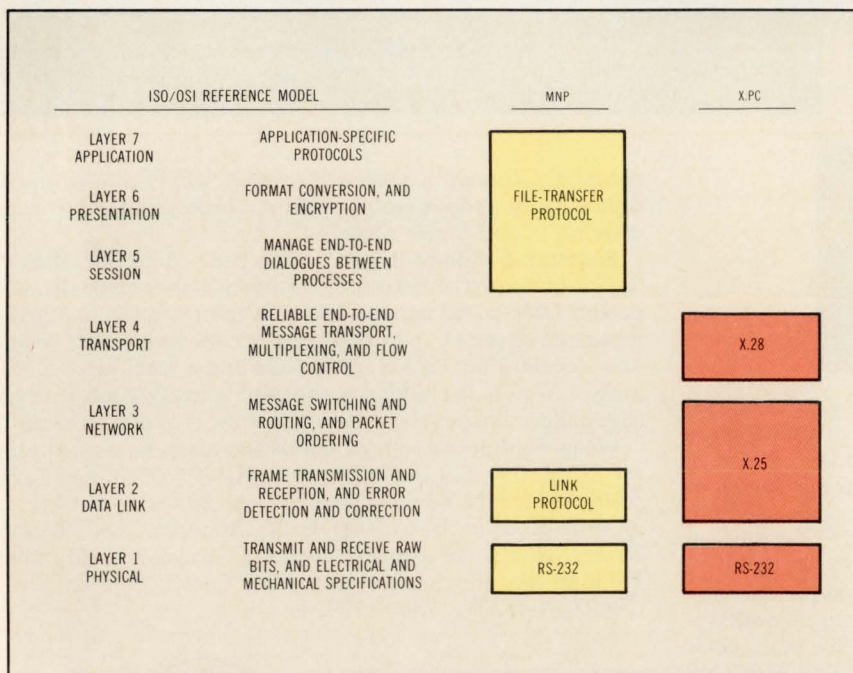
Subsequent messages also follow the same acknowledge/not-acknowledge scheme used for the initial link setup. The link can be broken if several not-acknowledge messages that cause retransmission are received. This typically occurs after the CRC uncovers any corrupted data.

Here, similarities between the two protocols end. The header used in the X.PC specification is fixed so that the overhead for a 256-byte (maximum) message remains the same as the minimum message size—8 bytes. On the other hand, the MNP specification calls for a header consisting of a variable-sized segment in addition to a fixed-size segment. The fixed portion contains such information as the length of the total header and packet-function type, while the variable portion contains parameter information that affects packet-function execution. Overhead for a 256-byte message approaches 14 bytes, with byte stuffing used to fill out messages.

Other differences center on features found in one specification, but not in the other. Perhaps the most significant is the inclusion of a file-transfer protocol in the MNP specification. The X.PC protocol, on the other hand, relies on the file transfer facilities already implemented as Tymnet value-added services (X.25, SNA/SDLC, SNA/BSC).

The file-transfer protocol is implemented at layers 5 through 7 (session, presentation, and application, respectively) of the International Standards Organization/Open System Interconnection (ISO/OSI) model. At the session level, corresponding computers

*(continued on page 190)*



**Tymnet X.PC and Microcom MNP protocols implement network services at different layers of the ISO/OSI model. However, they both use dumb asynchronous modems as the physical link.**

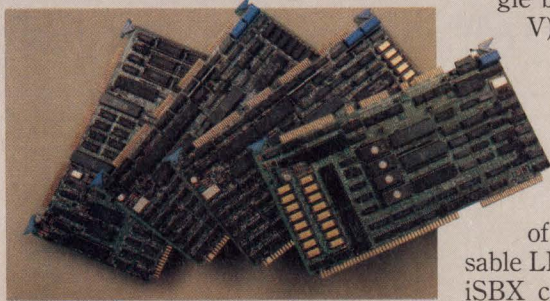
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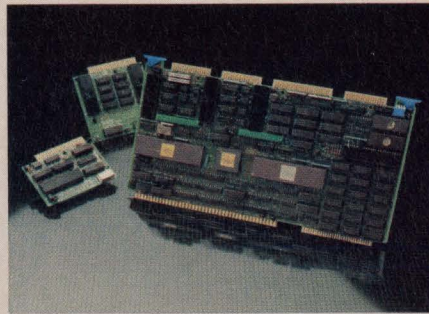


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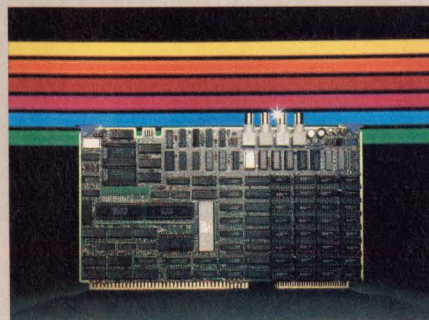
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**Flexible modem protocols**  
(continued from page 188)

exchange information including device type, operating system file type, and application identification, as well as source and destination addresses. Once this information has

been exchanged, corresponding computers can issue open and close file commands and transfer data between files. A virtual file format is used as the intermediary between the two file

systems by appending attributes such as file names, passwords, file types, and record lengths to the actual information.

Meanwhile, Tymnet has chosen X.PC for implementation of the multiplexed data channel feature already found in the X.25 specification. Built into the packet header is logical channel identification that allows users to initiate up to 15 simultaneous data sessions over the same physical link.

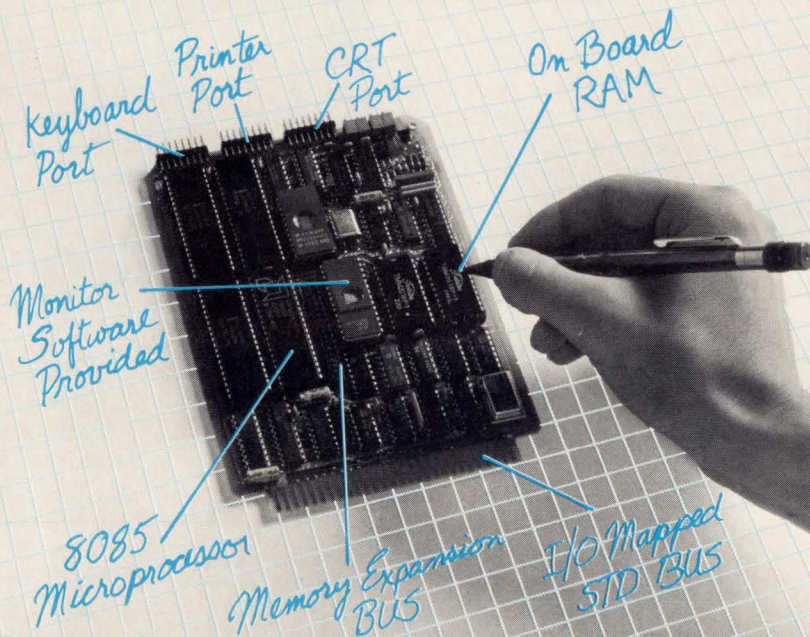
Packet assembly and disassembly software for X.PC executes in the CPU within the IBM PC, while both link management and file transfers are the responsibility of the personal computer in the MNP scheme. In both protocols, processing moves into the host CPU so that cheaper asynchronous modems can be used to implement either protocol.

Such communication overhead may overwhelm the available I/O bandwidth of the personal computer itself. The overhead needed to process messages sent at 1200 bits/s will eat up most of the 25-kbyte/s bandwidth found on many personal computers. Overhead includes taking the message off the serial port, calculating CRC checks, and transferring data to disk.

Additional processing needed for file-format conversion or the demultiplexing of data channels may require a frontend communication processor as that found on some public data networks such as Tymnet. Intelligent modems, such as the ETC100 from Computer Development, Inc or the Era 2 from Microcom, with dedicated microprocessors and memory, represent such frontend processors. Handling the necessary communication overhead in parallel with the application processing done on the personal computer may be the only way that the enhanced capabilities of these protocols can be optimized. **Microcom**, 1400A Providence Hwy, Norwood, MA 02062; **Tymnet, Inc**, 2710 Orchard Pkwy, San Jose, CA 95134.

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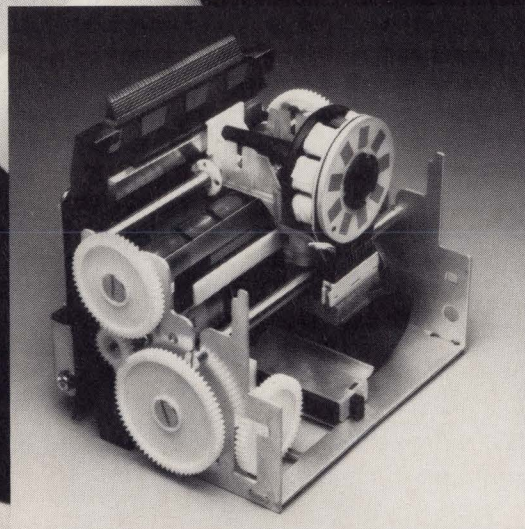
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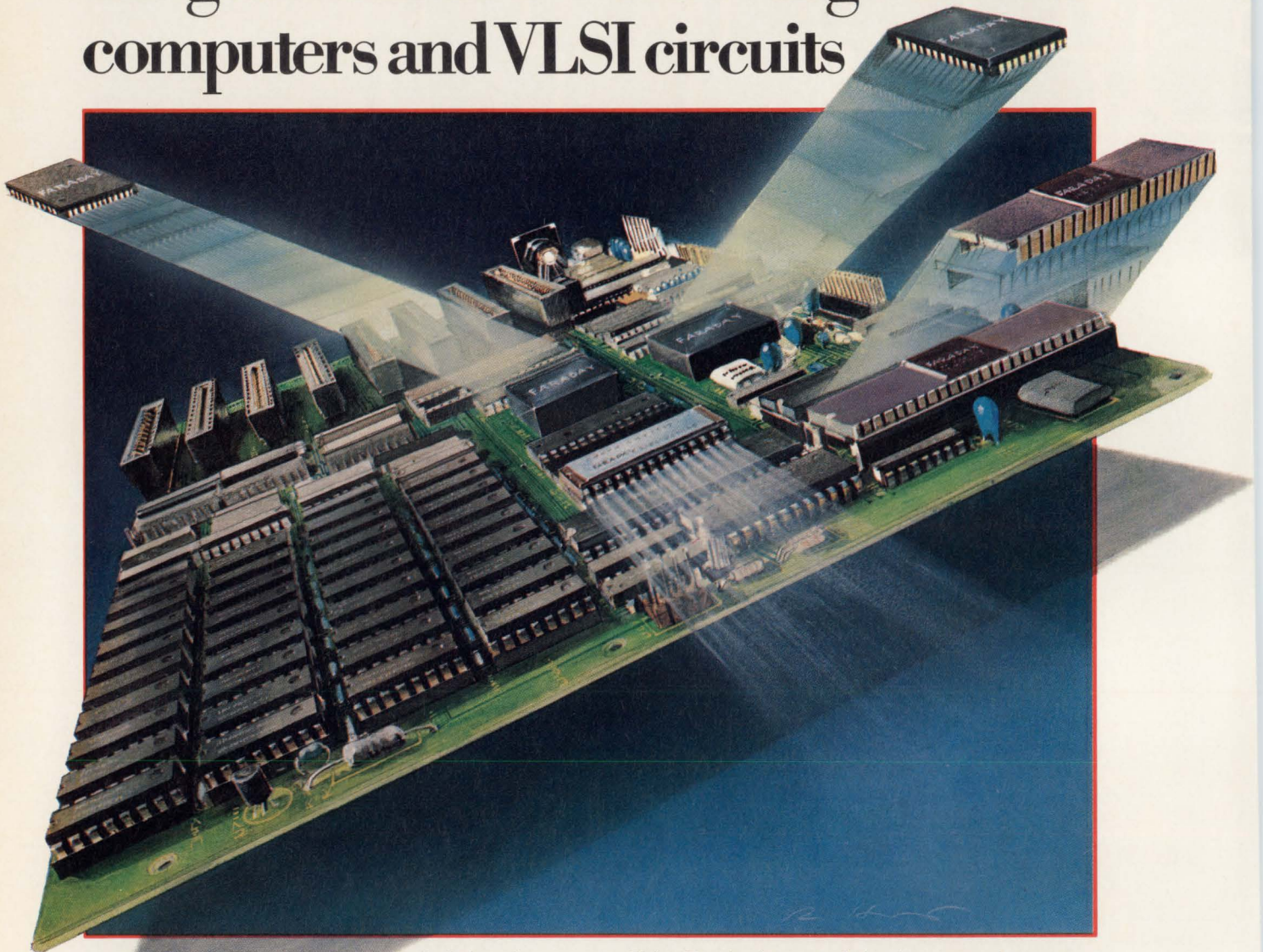
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# CAE, SCOPE MAKERS JOCKEY FOR POSITION

Engineering workstation manufacturers vie for sales with increased performance at lower prices. Meanwhile, the digital versus analog scope battle heats up for high end instruments.

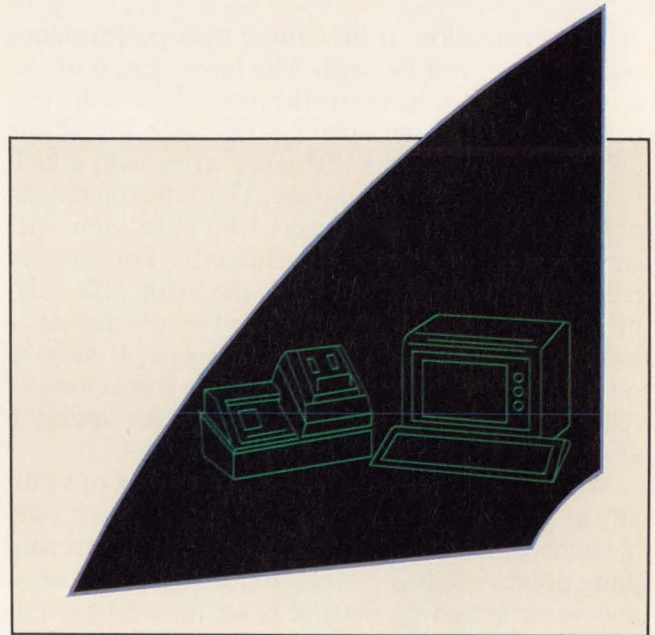
by Bill Furlow,  
Senior Editor

While most experts considered 1984 to be a year of financial recovery, test equipment manufacturers slugged it out as if the economy were in recession. Several key categories of test equipment continued to make significant improvements in price/performance ratios. And, in areas where test equipment gains expanded, advances in computer-assisted engineering for the designer were staggering. The special niches carved from computer aided engineering and test equipment development for use with the IBM and other personal computers were impressive.

The rapid gains have altered the computer aided engineering market substantially from what existed a year ago. And designers' expectations are changing, too. Engineers no longer need to be sold on the value of design workstations—now, the workstation's increased productivity is well documented. Demand for new test equipment is also high. Two factors have contributed to this situation. First, spending cuts from several years ago forced many engineers to postpone purchases; and now, newly designed equipment is starting to outstrip the capabilities of the test equipment that is on hand.

## Scope wars

The battle between suppliers of lab oscilloscopes heated up this year. New activity is most noticeable at the top of the performance scale where the two leading U.S. makers vie for the engineering dollar.



For the last five years Tektronix (Beaverton, Ore) has had little competition in super-high performance oscilloscopes. At 1-GHz bandwidth, and with a screen bright enough to allow direct viewing of traces at that speed, the 7104 was the undisputed speed king of oscilloscopes. Because so few other scopes have come close to this achievement, Tektronix seemed to feel secure enough to keep the same the performance figures for the 7103—a rackmount derivation of the 1-GHz 7104 introduced earlier this year. Whether Tektronix will maintain its edge through 1985 depends upon how well Hewlett-Packard's (Colorado Springs, Colo) newly introduced 54100 scopes sell during the next few months.

The differences between the Tektronix and Hewlett-Packard models are great enough to require



Hewlett-Packard and Tektronix announcements of new computer workstation families may have been too late to slow the rush of personal computer-based tools. However, engineers will continue to look to these large manufacturers.

careful evaluation of how these high performance oscilloscopes will be used. The basic design of the scopes themselves presents the most obvious distinction. The 7104 is an analog scope with a realtime display; the 54100 is a digitizing scope with a brilliant, but digitally stored trace. The 7104, therefore, offers an edge to the engineer who must view one-shot or nonrepetitive events directly. For viewing recurring waveforms, however, the 54100 offers significant enhancements. Since the 54100's display is a digital simulation of a storage scope, it may be set to retain and display information for as long as required; or its persistence may be set for updating as often as desired.

While the 54100's scheme allows viewing of virtually as many pretrigger events as necessary, it does have some drawbacks. The information between sampling points is missing on nonrepetitive waveforms, and when screen persistence is set to short periods of time. This has importance in one of the major applications of this class of oscilloscopes—the study of high speed, single-occurrence phenomena.

Many designers of high speed logic have opted for the precision of the 7104 over other instruments for viewing critical signal waveforms. Logic analyzers, for example, have almost replaced oscilloscopes for debugging microprocessor-based logic circuits which typically run at less than 10 MHz. Since logic analyzers present waveforms at only two voltage levels (actually "1-bit resolution"), a high speed scope can reveal a great deal more information than most logic analyzers. Instability, overshoot, undershoot, and precise timing are shown much more clearly on a scope. This can help designers find causes of many timing problems that typically do not show up on other test instruments. In this area,

engineers will have much difficulty deciding between the digital 54100 and the analog 7104.

Since most logic signals are repetitive, the digital approach becomes far more useful. In the end, the choice may boil down to asking how often an engineer needs to detect and view nonrepetitive waveforms, and whether that need is frequent enough to justify the additional cost of the analog Tektronix scope.

Another important step in oscilloscope evolution took place this year when multicolor displays became available for lab scopes. Although Tektronix introduced its color shutter technology in the lower cost 5000 series lab scopes (with the 5116 and its companion 5D10 digitizer), there is no reason to expect color to stay in the lower performance categories. The nonengineers using lower cost scopes may have greater need for color enhancement. But the displays on engineering scopes are becoming cluttered. High resolution, multicolor displays offer a viable solution to the problem.

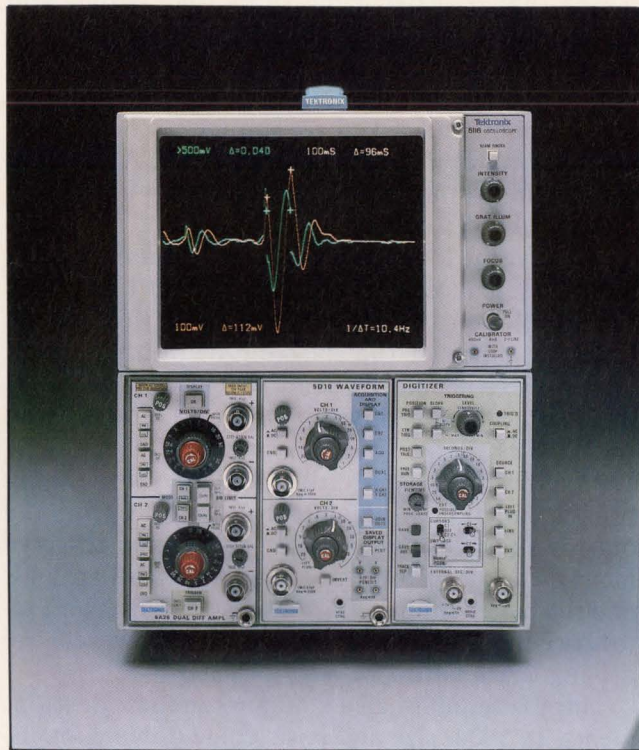
### Analyzer gains

Although some high performance oscilloscopes retain part of their esteem in the design lab, the logic analyzer invasion begun a decade ago is not about to subside. Continuing to build on its successes with the 1630 family of logic analyzers, Hewlett-Packard this year introduced the newest member, the 1630G. The new "G" model is an attempt to broaden the logic analyzer's use. For the hardware designer, the 1630G offers 65 channels of state analysis, of which eight lines can be used for timing analysis at up to 100 MHz.

The capabilities capturing the most attention, however, are the software-performance evaluation



DATA I/O's new ABEL is one of several PROM and PLA programming systems tied to the IBM PC. Providing high level programming, ABEL speeds software development and makes a direct link to programming devices.



The Tektronix 5110 with color display is seen as the forerunner of other oscilloscopes. The added dimension provided by multicolor waveforms gives the instrument a decided edge over other models.

tools provided with the 1630G. New modes of operation include program flow, time position, and linkage measurement. The first monitors the program based on opcode accesses, in addition to making histograms by addresses (introduced on the earlier 1630s). This added feature can be especially useful when ROM and RAM are intermixed through the address ranges or when self-modifying code may confuse the results of a histogram. Time-positional measurements can detect the number of occurrences of any chosen event within any chosen unit of time, thereby providing a close monitor of the precise functioning of the system. The linkage measurement feature also monitors the relative frequency of activity between software modules. In the trend toward storage of data for later recall, the 1630G can be interfaced to Hewlett-Packard's 9121 3½-in. floppy disk drives.

Nicolet Paratronics of San Jose, Calif also features floppy disk storage in its 800 series logic analyzers. Featuring dual floppies and a programming keyboard in a portable computer-like package, the Nicolet analyzer offers up to 200-MHz timing, 1000 words of data collection, and linkage analysis.

Following some of the same trends as Hewlett-Packard and Nicolet, while setting some of its own, Dolch Logic Instruments (San Jose, Calif) this year added floppy disk storage of setup and measured

data to its Colt plug-in logic analyzer. The Colt features mechanical reconfiguration through a selection of plug-in modules that allow the user to choose timing modules up to 300 MHz, state analyzers up to 48 channels, in-circuit emulation, or erasable PROM programming. Whether or not designers will find this level of interchangeability desirable will depend upon how well Dolch reads engineering departments' cost consciousness. It will also depend on the success of the company's decision to put integrated intelligence above general-purpose computer control of simpler instruments.

Another important step upward for logic analyzers came this year when Tektronix announced its DAS 9100. The 91DW DesignLink package ties the DAS to a Digital Equipment Corp VAX computer for VLSI. This package capitalizes on a combination of DAS internal stimulus generation and VAX computation ability to provide its high power answer to the wave of "personal instrumentation." It uses the computer for test pattern generation and downloads to the DAS for testing, then uploads results to the VAX for analysis. Apparently, Tektronix has chosen this method to stem the oncoming tide of PC-based analyzers; it highlights the shortcomings of personal computers in comparison to the power of the VAX.

### Creating development systems

Microprocessor development systems comprised yet another extremely active area in 1984. One enterprising young company of note, Language Resources of Boulder, Colo, has staked out a unique niche. LR is hoping to attract some of the huge interest designers have shown in Motorola's 68000 microprocessor. In an attempt to tap into the tremendous capital investment many labs have already made in purchasing Intel's (Santa Clara, Calif) Intellec series development systems, LR has introduced a hardware/software package that allows the Intellec to support 68000 program development. Its 6800 CPU board plugs into Intel's Multibus chassis directly, and the assembler, linker, and debugger are supplied on Intel compatible disks. LR also plans to supply Pascal, C and PL/M-68K compilers for the system.

In 1984 Hewlett-Packard announced support for both the 68000 and the 68010, as well as several of Intel's newer microprocessors (including the 80186 and 80188), on its 64000 universal development systems. At about the same time, the 68010 became the thirty-sixth microprocessor Tektronix supports on the 8560 series universal development system. Motorola also made its development system for its latest in the family—the 68020—available in 1984. The completeness of this year's effort has appealed to designers. This latest model has cross-development packages for the Motorola Unix-like V/68, and

support packages including Benchmark 20 evaluation software for programmers.

Several higher level languages were introduced in 1984 for use in programming PROMs and programmable logic arrays. Assisted Technology Inc (San Jose, Calif) claims its CUPL is a language "for hardware designers by hardware designers." It is aimed at providing logic design support that will allow a designer to shrink design sizes by replacing TTL with programmable logic. Designs can be expressed in either Boolean equations or truth tables, and designers can generate a fuse pattern that is downloaded to the device programmer. Wavetek-Digelec (Sunnyvale, Calif) incorporated CUPL into its UP 803 device programming system. Design and simulation is done under CUPL on a VAX or a IBM PC, and downloaded into the 803 for programming, testing, and verification.

A direct competitor for CUPL is ABEL, a high level programmer's language also introduced this year for use with Data I/O Corp's (Redmond, Wash) device programmers. ABEL boasts many of the same features as CUPL—ABEL can also be used to generate programming information on a PC.

### Revolution in design

A decade ago, computer aided design was slipping into many engineering companies. Back then, CAD

meant that a department supported design and manufacturing by automating the translation from engineering drawings to printed circuit board layouts. To many engineers, CAD was just a group in the company that asked for copies of their drawings every once in a while. To others, CAD was so self-contained that it actually became a bottleneck in the flow of work.

Whatever it looked like from the outside, however, the engineers in that department knew they were revolutionizing the design process. It mattered little that much of the checking of printed circuit layouts was still done by hand, just in case the resulting board came out unworkably large. Today, even the smallest design departments can offer CAD. Within most companies, the trend is toward taking printed circuit board manufacturing back from the outside specialists who have proliferated to serve many different customers. The speed of turnaround, and the better security of new designs, are two factors driving this change. Economics, however, are driving CAD harder.

This year established a landmark in these developments. In 1984, size and costs came down enough, and performance efficiency came up enough to justify printed circuit board CAD systems for virtually any company. Driven by such systems as those from Cadnetix (Boulder, Colo), Telesis Systems

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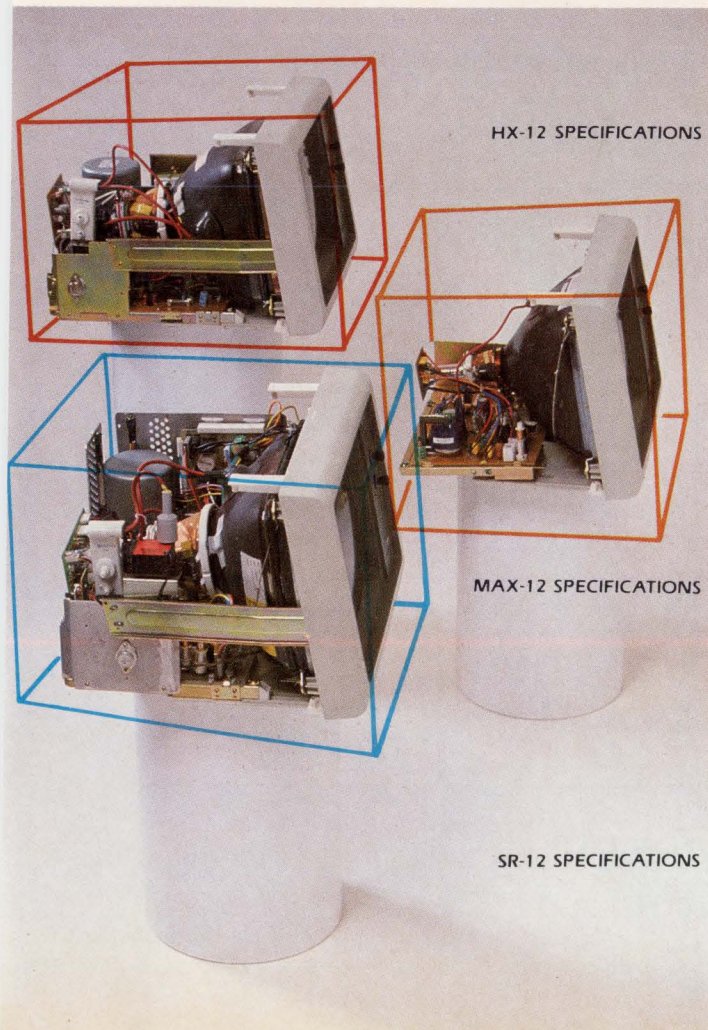
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<b>Scan Frequencies</b>	Horizontal: 15.75 KHz Vertical: 60 Hz
<b>Display Size</b>	215mm x 160mm
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<b>Misconvergence</b>	Center: .6mm max Corner: 1.1mm max
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<b>Characters</b>	2000 characters (80 characters x 25 rows—8x8 dots)
<b>Input Connector</b>	9 Pin (DB9)—cable supplied to plug directly to IBM PC
<b>CRT</b>	12" Diagonal, 90 Degree, non-glare surface (P 34 Phosphor)
<b>Input Signals</b>	Video signal, Horz Sync, Intensity—positive TTL levels, Vertical Sync—negative TTL levels
<b>Video bandwidth</b>	18 MHz
<b>Scan frequencies</b>	Horizontal: 18.432 KHz Vertical: 50 Hz
<b>Display size</b>	204mm x 135mm
<b>Resolution</b>	Horizontal: 900 dots Vertical: 350 lines
<b>Input Connector</b>	9 Pin (DB9)—cable supplied to plug directly to IBM PC
<b>CRT</b>	12" Diagonal, 90 Degree, In-Line Gun, .31mm dot pitch black matrix, non-glare surface
<b>Input Signals</b>	R, G, B channels, Horz Sync, Vert Sync, Intensity—all positive TTL levels
<b>Video bandwidth</b>	25 MHz
<b>Scan frequencies</b>	Horizontal: 31.5 KHz Vertical: 60 Hz
<b>Display size</b>	215mm x 160mm
<b>Resolution</b>	Horizontal: 690 dots Vertical: 480 lines (non-interlaced)
<b>Misconvergence</b>	Center: .5mm max Corner: 1.0mm max
<b>Display colors</b>	16 colors (black, blue, green, cyan, red, magenta, yellow, white, each with 2 intensity levels)
<b>Characters</b>	2000 characters (80 characters x 25 rows)
<b>Input Connector</b>	9 Pin (DB9)—cable supplied

Corp (Chelmsford, Mass), Xerox Versatec (Santa Clara, Calif), and old standby Calma (Santa Clara, Calif), printed circuit board design and manufacturing is not only moving into smaller companies but is being tied to the common design data bases generated from new computer aided engineering workstations.

Features a designer can expect to find in these systems today include automatic schematic capture from the CAE workstation, automatic or assisted component placement, and automatic routing of multilayer conductors. As a minimum output, they can expect artwork generation, numerical control drilling tapes, and auto-insertion tapes.

**Workstations attain legitimacy**

Engineering managers have observed that workstations are the third-most frequently mentioned concern of engineers. After years of insufficient investment support—during which engineers saw technicians receive \$50,000 to \$60,000 worth of test equipment while the average design engineer got less than \$15,000 in equipment—the process is being revised. This year engineers saw the CAE workstation attain legitimate status as a productivity tool that was really on their side. While sales have climbed steadily since the concept first came to general attention several years ago, critical mass was achieved in

1984. Such companies as Daisy (Harrisburg, Pa), Computervision (Bedford, Mass), Metheus (Hillsboro, Ore), Mentor Graphics (Beaverton, Ore), and Apollo (Chelmsford, Mass) have grown to respectable size by serving this growing market, but the opportunity for successful launching of another Sun Microsystems (Mountain View, Calif) or Valid Logic Systems (Mountain View, Calif) may be over. In the last year, such giants as Hewlett-Packard, Tektronix, and Hitachi (Woodbury, NY) entered the CAE workstation fray.

Even so, other viable CAD and CAE systems makers do exist, including Zycad of St Paul, Minn; Masscomp of Westford, Mass. Phoenix of Data Systems of Albany, NY; EAS of Middletown, Conn; and Kontron of Redwood City, Calif. They range in computing power from PC size, through mini-computers, to very large mainframes. They allow true top-down design, and make the engineer's pencil and drawing board obsolete—just as the scientific calculator replaced the traditional slide rule. What is more, they encourage simulation during design, not after the prototype has been built.

Engineers will find their designs and turnaround times so improved by CAE, that nothing will reverse the trend. Designers themselves estimate that CAE improves their productivity by 50 percent. Some even feel that 50 percent is a conservative guess.

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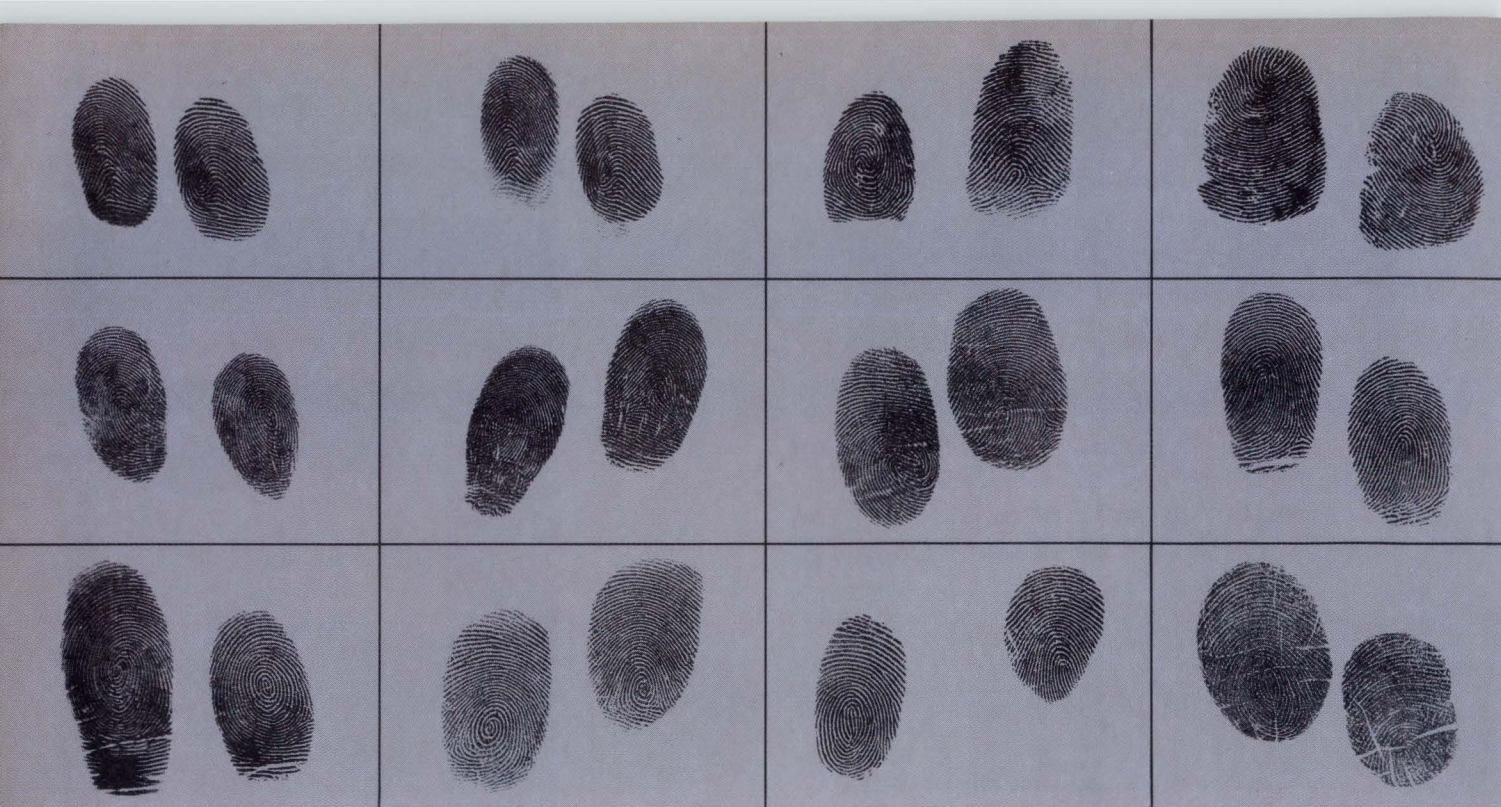


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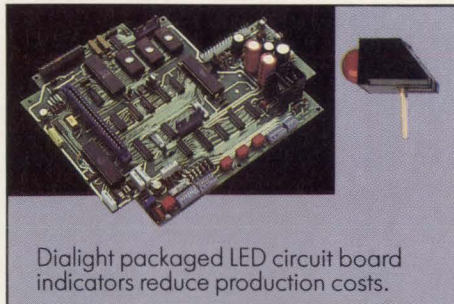
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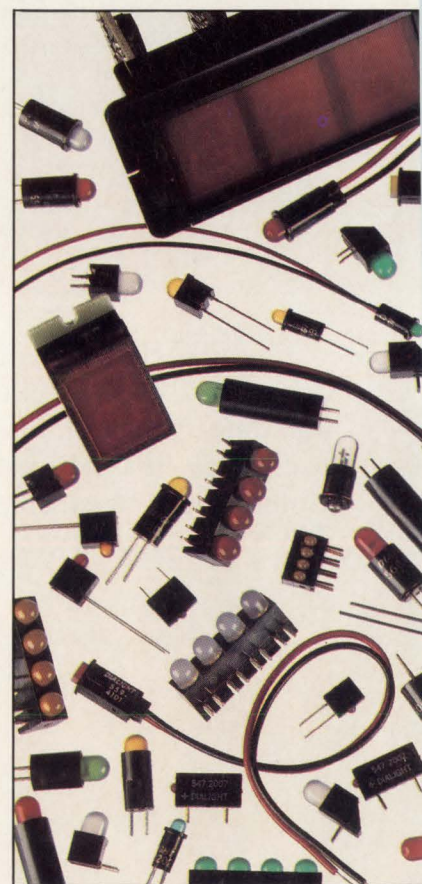
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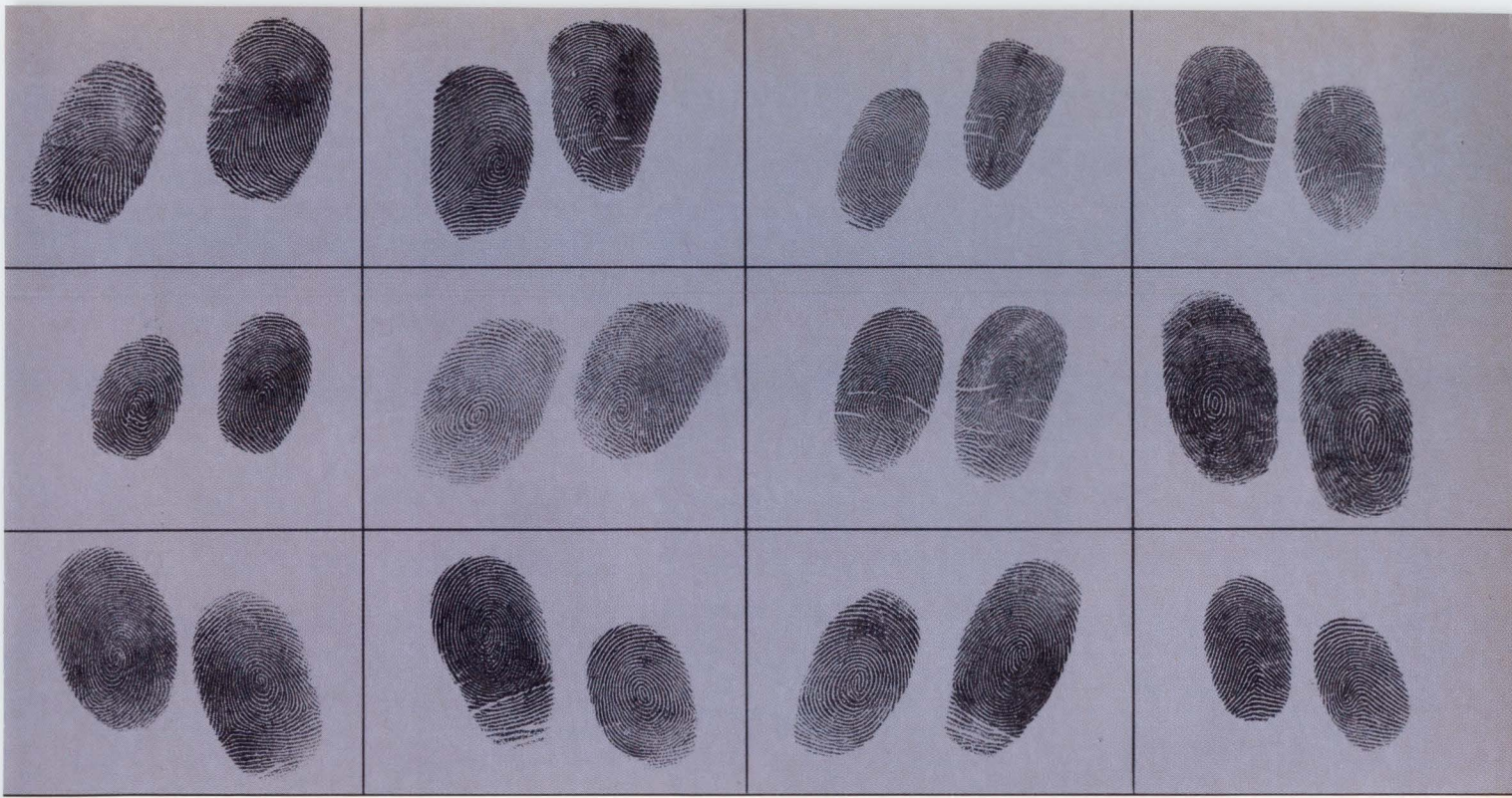


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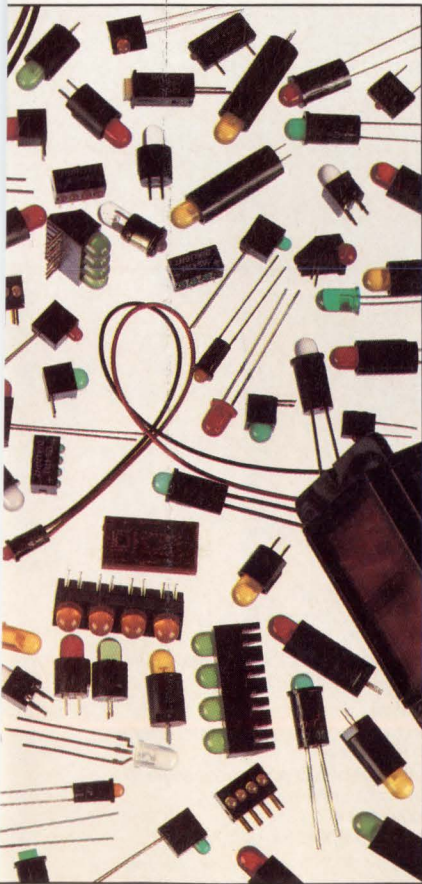


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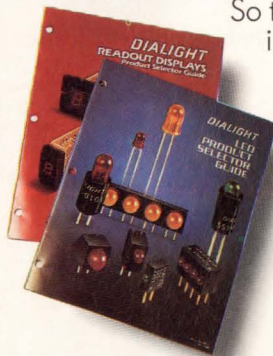
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CIRCLE 88

## CAD packages convert micros into engineering workstations

Personal computers outfitted with the necessary design tools (eg, schematic editing and logic simulation) can be bought for less than \$15,000, according to Roy Prasad, product manager for Personal CAD, Inc. He admits that the software packages designed for personal computers are less powerful than similar tools on larger computers. These packages support fewer nodes in simulation and handle smaller data bases for schematic entry. On the other hand, he points out that engineers rarely use the full capabilities of the large systems.

In fact, some tasks are more suitable for personal computers than multi-user hosts. For example, the highly interactive nature of schematic editing makes it difficult to use computer aided design packages (eg, SCICARDS) that run on larger machines through time-sharing. Editing packages such as CAD 2000, from Chancellor Computer Corp; Design Automation, from Dasoft Design Systems; DASH-1, from FutureNet; and PC-CAPS, from Personal CAD support hierarchical structuring of logic design so that large projects can be effectively partitioned into as many as 50 different levels of detail (99 levels for DASH-1). Net lists and component values can be extracted for use as input to logic and circuit simulators, such as Tegas and Spice, or sent to larger CAD systems,

Simulators for Personal Computers			
	Personal Computers	Type of Simulation	No. of Nodes
Blume Engineering PSpice	IBM PC	analog circuits	120 MOS or 140 bipolar transistors
E/Z CAD Logicorp	IBM PC any CP/M machine	logic	3000 (9-state)
Personal CAD PC-Logs	IBM PC	logic	5000 (12-state)
Spectrum Software MicroCAP	Apple II IBM PC	circuit	40
Spectrum Software MicroLogic	Apple II IBM PC	logic	1750 (5-state)

such as Applicon and Gerber, for generation of artwork or circuit layout.

In addition to schematic editing, Chancellor Computer, Dasoft Design Systems, and Personal CAD also support manual routing of printed circuit boards as well as the generation of finished artwork. However, disagreements arise concerning the minimum graphics resolution needed to route complex circuit boards.

On one hand, Chancellor Computer provides the high resolution found on more expensive CAD systems (1024 x 768 pixels on the CAD 2000) as well as the 640- x 400-pixel resolution found on many IBM PCs. Likewise, FutureNet uses the 640-

x 400-pixel resolution for its schematic editor. Terry Smith, product manager with Chancellor Computer, feels this is the minimum resolution for accurately placing pad and drill masters, trace layers, ground and power planes, and final silk screens.

However, higher resolution exacts a higher price. For example, Chancellor Computer's high resolution system costs \$10,000 more than its 640- x 400-pixel version, or about \$23,500. The higher price is due to the special graphics card with its own dedicated graphics processor.

Many potential users cannot afford that premium and do not need to pay it anyway, Prasad says. He notes that the PC-CAPS routing package requires only a 320- x 200-pixel resolution (the standard resolution on IBM PC systems), but has the potential to handle printed circuit boards that approach 60 x 60 in. (25 mil grid size). Similarly, the Dasoft routing package needs no special graphics terminal, but uses any 80-col x 24-row cursor terminal for graphics editing. Line-drawing primitives on such terminals provide finer onscreen editing.

Without the pretty pictures, both systems provide the necessary ability to generate the artwork because the

(continued on page 208)

Schematic Editors			
	Personal Computers Supported	Graphics Resolution Required	Circuit Routing
Chancellor Computer Corp	IBM PC	1024 x 768 pixels 640 x 400 pixels	yes
Dasoft Design Automation	Apple II Kaypro North Star Advantage	80 x 24 cols	yes
FutureNet DASH-1	IBM PC	640 x 400 pixels	maybe (simple circuits)
Personal CAD PC-CAPS	IBM PC	320 x 200 pixels	yes

**CAD packages***(continued from page 207)*

graphics resolution of the screen has little to do with the resolution of the hard copy generated on a plotter. Prasad notes that lines and curves displayed on a raster screen are still made up of distinct points, no matter how fine the graphics resolution. On the other hand, plotters generate solid lines and curves. In fact, all graphics packages must eventually convert the bit maps used in graphics editing to vector endpoints understood by plotters.

Beyond graphics editing, personal computers can make a more significant contribution to an engineer's productivity through logic and circuit simulation. According to several knowledgeable sources, fewer than 10 percent of circuit and logic designers currently use simulation tools. Prior to the advent of personal computer-based tools, simulators (eg, Tegas and Spice) were the province of large mainframe and minicomputers with associated costs easily exceeding \$150,000. Those who had access to such systems often encountered "loopback" times (the amount of

time spent waiting for the final computations) exceeding several hours.

Although the processing power of personal computers is a fraction of that found on larger machines, they do supply users with a response right after the completion of computations. Thus, computations for integer-based digital simulation or floating point analog simulations can take several minutes on personal computers and still offer response times superior to those offered by mainframe or minicomputers.

However, maximum physical memory sizes (eg, 768 Kbytes on the IBM PC) limit the size of net that can be simulated, with logic simulation much simpler to implement than circuit simulation. For example, Logipro from E/Z CAD, Inc supports nine-state logic simulation for 3000 nodes on CP/M systems with 64 Kbytes of RAM. On the other hand, the MicroCAPS circuit simulator from Spectrum Software supports just 40 nodes. The smaller net sizes for circuit simulation result from the larger number of parameters involved

in comparison to logic simulation, says Andrew Thompson, president of Spectrum Software.

The smaller net size does not necessarily mean that such tools are less powerful than their mainframe counterparts. Thompson points out that designers often break down large logic designs or circuits into smaller partitions in order to analyze the results. Thompson estimates that the typical engineer breaks up circuit simulations to around 40 nodes, while logic simulations are best managed at about 2000 nodes. Accuracy does not suffer because logic and digital circuit simulations use integer data bases, easily handled by personal computers such as the Apple II or IBM PC. **Chancellor Computer Corp**, 1731 Embarcadero Rd, Palo Alto, CA 94303; **E/Z CAD, Inc**, 5589 Starcrest Dr, San Jose, CA 95123; **Personal CAD Systems, Inc**, 981 University Ave, Bldg B, Los Gatos, CA 95030.

**Chancellor Computer Corp—Circle 313**

**E/Z CAD, Inc—Circle 314**

**Personal CAD Systems, Inc—Circle 315**

## Software developer based on IBM PC puts 8088/80188 on STD bus

To strengthen STD bus applications, Ziotech is introducing a software development package for 8088/80188 processors along with a line of STD bus based single-board computers using the 80188. Extended capability for the 8-bit bus will be particularly useful in controller architectures, where STD systems address a wide variety of applications.

The series 8800 prototype development system, which runs on an IBM PC or compatible, consists of an 8088-STD target system in an eight-slot card cage, a power supply, software, and documentation. Offering a 16-bit internal capability, the ZT 8812 processor board is specially designed to work in the STD bus

development process. It contains the 8088 processor with a socket for an optional 8087 floating point processor. An 80130-6 interrupt processor with counters and timers provides Intel's iRMX-86 operating system kernel. In addition, the DEBUG 88 PROM monitor resides on the CPU board.

Software forms the major portion of the prototype development system. It consists of the DEBUG 88 monitor and a disk-based development package, PC/STD 88, which runs on the PC. The user can prepare object code for the development system, using



PC-compatible assemblers or compilers, as well as any convenient editor. The PC/STD 88 package then structures the object file for use on the target system. It lets the user specify memory address positions, links modules for use with other programs, and formats the files for loading into



the target system. Once it has loaded the linked object code into the target system, PC/STD 88 sets up the PC as a debug console communicating with the monitor on the CPU board.

Using the debug monitor, the user can examine and alter registers on the 8088 as well as on the 8087 numeric processor from the PC. Other normal debugger functions let the user set breakpoints, run programs, perform the I/O operations, and examine and

alter the target system memory. When the code has been fully debugged, the monitor PROM can be replaced with a PROM containing the user's routines.

In addition, the ZT 8814 and ZT 8815 single-board computers are based on the 80188 and run at 5 and 8 MHz, respectively. Each provides 5 byte-wide memory sockets that accept memory chips with capacities up to 32-Kbyte RAM or 64-Kbyte ROM.

DEBUG 88 resides in one memory socket. The same equipment and software can develop software for the 8088 or 80188 board.

The prototype development system, priced at \$2800, is available four to six weeks ARO; the ZT 8814 and 8815 are \$650 and \$695, respectively. **Ziatech Corp.**, 3433 Roberto Ct, San Luis Obispo, CA 93401.

Circle 316

## Silicon compilation cuts costs of custom VLSI

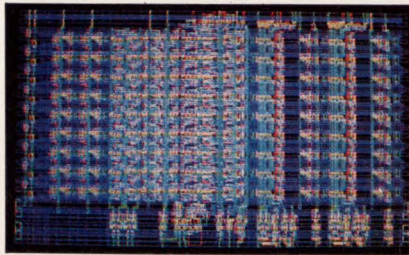
The Genesil silicon compilation system supports four designers from first concept through silicon layout in a hierarchical system design. In addition, it checks each design step for correctness. This makes it practically impossible to design a bug into the system because each step is checked for its impact on other parts of the system. As pictured here, the system can graphically plot sections of the chip's geometric layout.

During layout, a complete set of design rules for the specific process and IC manufacturer is used. Violation of the design rules is not allowed. Up to four processes can be verified simultaneously, allowing the designer to check between them to see which system allows the smallest die size.

The Genesil system is not restricted to designing one IC at a time. Designers can begin with the complete system, regardless of the number of chips required for a full implementation. In the event that more than one chip is required for the system, designers are able to continue interactive design of the entire chip set. Thus, system partitioning (interconnections between the chips and other optimizations) can be done during the early design phase and monitored or changed at any point in the design cycle.

Genesil is aimed at all system designers (not specifically IC designers) and has a Digital VAX-11/750 with a 1600-bit/in. tape drive, 450 Mbytes of disk storage, up to four color graphics stations (1025- x 768-pixel

resolution), and design automation software packages. These packages include IC definition, functional simulator, timing analyzer, place and route, testout, and tapeout.



Currently, the software package only supports NMOS chip designs. In the first quarter of next year, a CMOS function set that will be directly interactive with the NMOS function set, is expected. This will permit conversion of NMOS designs into CMOS circuits. IC design functions for both systems fall into six categories: memory, complex logic, data path, random logic, pads, and test. Memory functions offer blocks including RAM, ROM, first in, first out buffers, and stacks. Complex logic functions include PLAs, decoders, and encoders, while data path functions allow parallel data paths from 4 to 32 bits wide.

Compared to previous approaches, Genesil is a more hierarchical design environment. Designers can start at any design level. Logic and timing can be verified at any stage through more and more detailed iterations. A system architecture can be developed during the design process.

Random logic functions allow the user to compose lower level functions such as NAND and NOR gates or flipflops for simple signal inversions, gate buffering, or control signals. This provides direct access to the design's gate level, which is normally hidden in the other Genesil functions' block level design.

The Pad function is used to construct the pad blocks that provide off-chip connections. Test functions allow designers to include test blocks within the IC design. Two separate functions are provided—level-sensitive scan device (LSSD) and Interblock Scan Path. In LSSD, users create a test strategy that converts sequential circuits into combinatorial circuits by setting all of the sequential nodes so that test vector generation can be used. The Interblock Scan Path improves the controllability and observability of the internal paths. This yields a built-in test strategy in which the interblock registers are configured as linear feedback shift registers.

Designers are not apt to rush out and buy a Genesil system without some serious consideration. It costs \$545,000. This is almost 50 percent higher than other workstations on the market. However, the capabilities and labor savings are also higher than other workstations intended for gate-array or standard-cell VLSI design. **Silicon Compilers, Inc.**, 2045 Hamilton Ave, San Jose, CA 95125.

Circle 317

## Analyzer combines hardware/software tests in one unit

Giving designers a single instrument for testing, debugging, and analysis, the HP 1630G supplies three analysis functions for digital development: timing, state, and software performance. With its 65 channels, the analyzer is suitable for applications involving 16-bit microprocessors and multiple bus monitoring.

The unit provides timing-waveform diagrams that simultaneously display up to eight channels, and has user-definable labels to simplify data evaluation. Adjustable parameters include wide magnification range, glitch display, and direct time readout between cursors.

State listings display address, data bus, and status/control-line activity. Selectable display modes include binary, octal, decimal, hex, ASCII, and relocation, as well as user-defined and microprocessor-specific mnemonics. For easy interpretation, the user can display and/or trigger on

code in terms of relocatable or absolute address or mnemonics.

Using software performance analysis measurements, users can view selected portions of code and measure time or occurrence distribution. With this technique, the user can spot bottlenecks in operating software, determine best- and worst-case conditions as a function of data variables, and establish benchmarks for modules or an entire program. In addition, graphs of memory activity as a function of occurrence can indicate infinite loops, erroneous jumps, and activity in forbidden areas.

The device contains programmable nonvolatile memory, where the user can store an inverse assembler (disassembler) plus one setup configuration. When turned on, it automatically configures for a particular application. Time tagging measures the time between each stored state in the state analysis mode. It can also measure



the time from the trigger point to each state or the number of unstored states between each stored state.

Histograms measure program flow by showing the user where the program spends most of its execution time. It counts either all acquired states or only the instructions in the histogram. This eliminates confusion if the program generates in line code or if memory blocks are interspersed between sections of the program.

**Hewlett-Packard Co.**, 1820 Embarcadero Rd, Palo Alto, CA 94303.

Circle 318

## Workstations unite 32-bit processing with graphics

The 6000 family consists of two software compatible groups—the 6100 and 6200 workstation series. Both use National Semiconductor's NS32000 micros. These devices feature a main-frame-like architecture and an instruction set that is designed for efficient execution of high level language programs.

Members of the 6100 series employ the NS32016, a 32-bit processor with an external 16-bit bus. Three basic products are included in the series—the 6110 instrument controller, and the 6120 and 6130 graphics workstations. The 6110 instrument controller runs a realtime operating system (RTOS) and can execute object code programs generated in Basic, C, Fortran, or Pascal. It has a GPIB port with pass control and optional DMA. Standard equipment on the 6110 includes 256 Kbytes of memory, dual RS-232 ports, and a 360-Kbyte flexible disk.

The 6120 workstation uses the proposed ANSI Basic providing graphics functions, extended I/O, and interactive editing. The workstation comes with a keyboard and mouse, 1 Mbyte of memory, an FPP, a 360-Kbyte 5¼-in. flexible disk, and a 10-Mbyte Winchester.

Designed for data analysis, software development, and CAE applications, the 6130 is similar to the 6120, but also includes an enhanced version of Unix. A 20-Mbyte, 5¼-in. Winchester disk, a 360-Kbyte flexible disk, 1 Mbyte of memory, and an FPP are all standard.

The 6200 series is based on the NS32032 with a 32-bit data bus. It is expandable through the Global bus: a standardized, high speed (40-Mbyte/s) interface that connects the computing systems. The two basic products in this series are the 6210 and 6212 graphics workstations. The 6210 is suitable for custom VLSI and gate

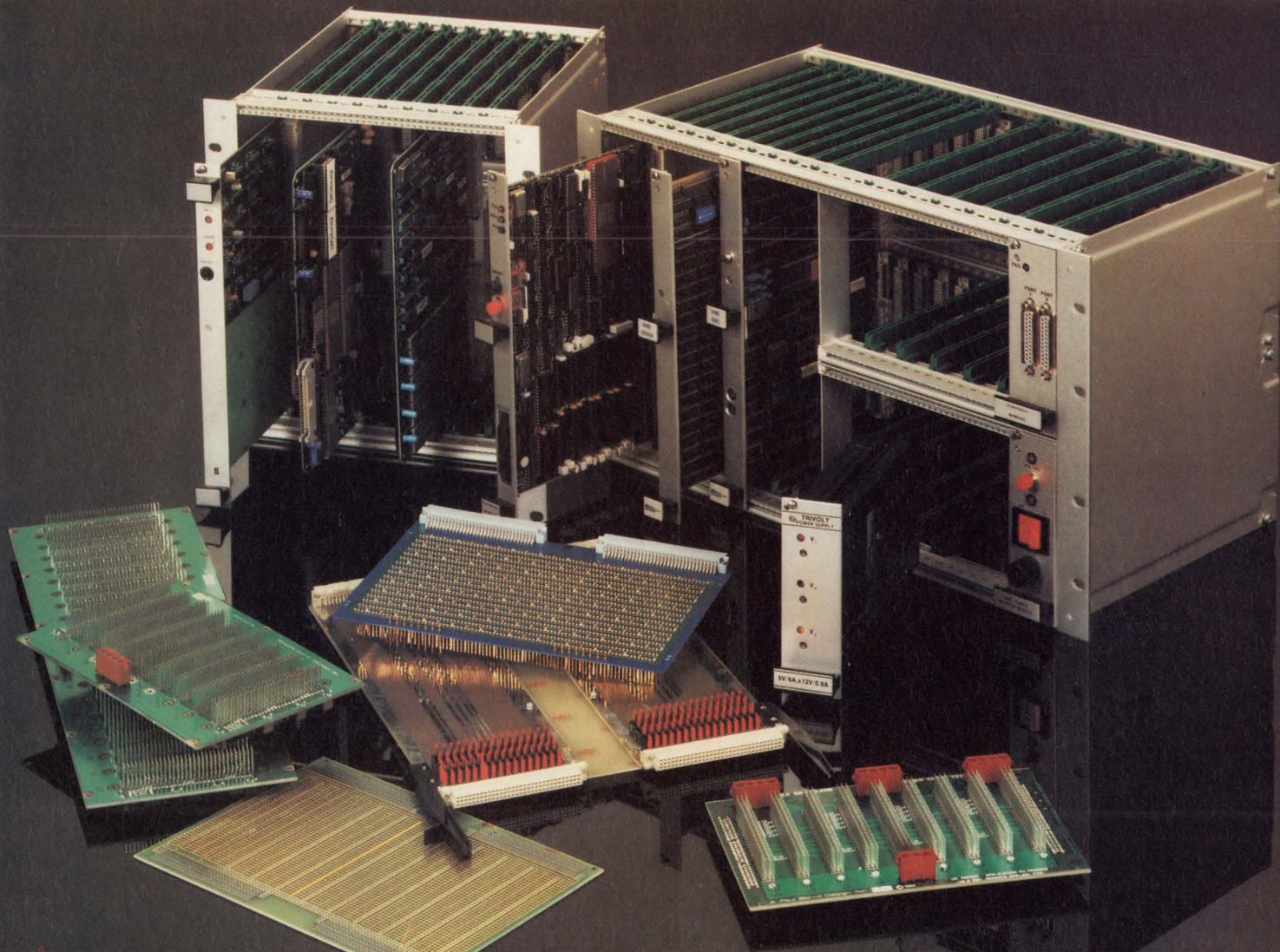
array design. It can also be configured as a file and a peripheral server for workstations on a local area network.

The 6212 workstation has dual 32-bit application processors, and large disk and memory. It is optimized for concurrent execution of compute- and interactive-intensive tasks such as editing designs and circuit simulation.

For configuration flexibility, the family provides industry standard interfacing options. These include RS-232, RS-422, IEEE 802.3 Ethernet, Centronics, Multibus, SCSI, and IEEE 488 interfaces. The 6110 controller is priced at \$4995.

The graphics workstations range in price from \$7995 to \$35,950. **Tektronix, Inc.**, PO Box 1000, Wilsonville, OR 97077.

Circle 319



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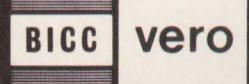
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CIRCLE 89

## Development system turns any microcomputer into a workstation

Using a personal computer as its control console, the Universal Development Laboratory integrates an analyzer, an emulator, a programmer, and an input stimulus generator in a single pod-sized box. A control program running on the host coordinates system resources. When emulating a target ROM, the laboratory becomes a development system for any target processor.

The 48-channel bus state analyzer is triggered if a program goes outside its normal address range. In addition, the trace buffer stores 170 bus cycles that can be used for debugging. Trigger setups and traces of good systems can be saved on disk, then automatically compared to later test traces. A filtered trace allows only writes to a particular memory location together with a following cycle (which contains the next instruction). Four-step sequential triggering specifies up to three events that must occur before triggering becomes possible.

To search for the trigger, the system uses high speed RAM truth

tables instead of comparator circuits. This allows any 8-bit function to be specified on each of the 6 input bytes.

Universal at both ends, the system interfaces to the host through an RS-232 port and to the target system through a standard ROM socket.

Because the bus state analyzer can debug any processor, target processor emulation is unnecessary. Most target bus signals connect at the ROM socket, so a complete view of bus operation takes only about 12 additional analyzer inputs. The signals connect by plugging probe wires into a 40-pin DIP clip on the target processor.

Since the target processor stays in its socket, operation is transparent. Moreover, maximum 195-ns access time makes ROM emulation fast enough for full-speed operation with next generation processors. A single wire connects both the analyzer and



the emulator to target system signals, thereby minimizing loading.

The ROM emulator and EPROM programmer share the same memory, so EPROMs can be burned directly from the target program image used for emulation. This target program can be loaded several ways: read from hex or binary disk files, received serially in hex format, or from a ROM in the programming socket. **Orion Instruments**, 172 Otis Ave, Woodside, CA 94062.

Circle 320

## Standard APL development station front-ends array processor

By using an IBM PC as its workstation, Analogic's APL Machine brings the low cost, flexibility, and responsiveness of a desktop microcomputer to high speed array processing. Through this interface, the system

begins to overcome previous drawbacks to developing high speed array processing applications, such as inflexibility and difficult programming. Previous APL/array processing development was confined mostly to large, computation-intensive installations because conventional linear computer architecture is not hardware efficient for processing arrays. Conversely, array processing hardware is generally infeasible for the execution of high level programming languages.

As an interface to the APL Machine, the PC

becomes an APL programmer's workstation; alternately, it functions in native mode. Whereas array processors typically execute libraries of assembly language or Fortran subroutines, the APL Machine's array processor directly executes ISO-validated APL programs written on its own or external hardware. Moreover, Unix-like shells incorporating non-APL code accommodate applications using compiled or assembled code.

The Unix-derived operating system creates a multi-user, multitasking environment with virtual memory. Three processing units make up the system architecture: a 12.5-MHz 16/32-bit control processor, pipelined ALU, and address generator. APL



primitives and operators reside in pipeline microcode. This architecture supports several levels of overlapped and parallel processing; a memory manager coordinates nested applications and shared code among concurrent processes.

Though the array processor has been benchmarked in specific applications between 2 and 10 MFLOPS,

the company claims that hardware design efficiencies sometimes push those figures into the 15-MFLOPS ballpark.

The workstation's InSight operating environment lets each user display up to 10 concurrently running tasks on overlapping and sliding windows; 10 function keys on the workstation keyboard correspond to active windows. Keycaps are labeled with

both APL and ASCII characters. A typical system configuration includes the IBM PC, 4-Mbyte AP500 array processor, 124-Mbyte hard disk, dual-mode tape drive, and I/O processor supporting 8 to 16 terminals. **Analogic Corp.**, Audubon Rd, Wakefield, MA 01880.

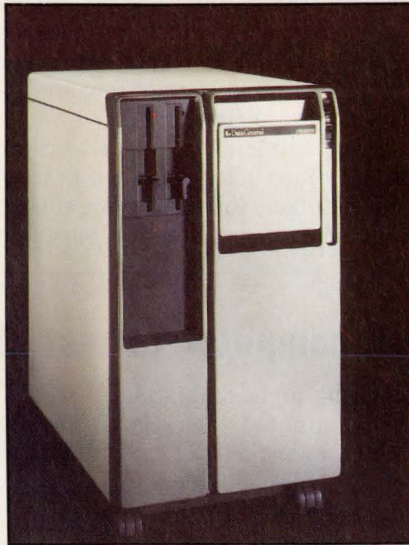
Circle 321

## Video DRAM adds graphics power to workstations

Two engineering workstations offer a choice of high resolution monochrome or color graphics. The 4000 and 4200 incorporate Texas Instruments' multiport video DRAM and can stand alone or be used as a node in a distributed system environment. Contained in a housing that fits under a desk, the workstations feature up to two 5¼-in., 38.6-Mbyte Winchester disks, up to two 5¼-in. floppy disks—each with a 737-Kbyte capacity, and built-in Ethernet LAN.

The system's graphics architecture takes a raster buffer, closely coupled with CPU and system memories, and combines it with a set of assembly level graphics instructions. The raster buffer houses the 64-Kbit video chips. These devices have a fast on-chip shift register that supports dot rates in excess of 150 MHz. The workstations require support for an interlaced 1024 x 1024 display with dot rates around 50 MHz. This chip also provides display refresh through a separate serial port, allowing the CPU greater random data port access. The result is a graphics memory that sits directly on the high speed memory bus, simplifying control hardware.

Designed to run on all 32-bit workstations having bit-mapped graphics, the graphics instruction set (GIS) is considered a Data General standard. It provides the basis for window management with a firmware concept



called a form. All GISs define pixel coordinates relative to this form. The forms, in turn, are building blocks for windows. Operating within forms, GIS clips all primitives to the form boundary, defines pixel coordinates relative to user coordinates specific to each form, and manipulates colors independently for each form. With this process, several independent windows are displayed and written simultaneously, with minimal system and user overhead.

Six boards make up the system hardware. The two-board CPU is based on the Eclipse MV4000 and consists of a control unit and a processor unit. Built-in reliability features include memory error detection

and correction, memory sniffing, and power-up tests.

The I/O board is a microEclipse-based controller. It provides interfaces to three asynchronous ports, a Winchester controller, a floppy controller, a cartridge tape unit, a keyboard, and a LAN.

Other boards include a color graphics board and monitor supporting 1024 x 1024 x 4 bit-mapped raster display. Sixteen simultaneous colors are available from a palette of 4096. Memory boards provide 1-, 2-, or 4-Mbyte capacities.

Running AOS/VS software and a native Berkeley Unix operating system, workstations support languages including Fortran 77, C, PL/1, and Basic. Systems cost between \$35,500 and \$59,500. **Data General Corp., Technical Products Div**, 4400 Computer Dr, Westboro, MA 01580.

Circle 322

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## Test and measurement merges with CAE in design workstation

With a complete logic analysis system and tools from the Idea 1000, the Midas 7000 supports the entire digital hardware design cycle. The system covers not only schematic capture, simulation, and physical layout, but handles verification and test of the final hardware as well.

Data acquisition and clock probes connect the 7000 to the hardware under test. Realtime acquisition results go to the workstation's main memory. Once there, a disk drive on the network stores the data, or the workstation can process it.

To analyze software performance, a user-written program (anywhere on the network) acquires and processes realtime software execution. In histogram form, the CRT displays subroutine call frequencies that are automatically sorted. Through the use of command macro files and programmable keys, only a single keystroke will accomplish the software analysis. A triggering system is the basis for state acquisition. Its



60-word recognizers trace software data flow. The recognizers organize into 15 states for either triggering or data qualification. A programmed trigger sequence can jump between states, branch to other states, or branch within a state to trace recursive software flow.

The sample clock uses five clock lines defined in terms of logic or transition edge, then they are ORed together for synthesis of bus-cycle

clocks for microcomputer systems. Two hold clocks demultiplex buses without double probing.

To make the most of its 4-Kbyte/channel data storage memory, the timing analyzer uses several acquisition modes to increase the time window for acquiring data. The transition mode stores data only when a transition occurs on one of the acquisition channels. A counter provides realtime representation of timing activity on the display. The counter keeps track of the number of samples between transitions.

A multitrigger mode breaks data acquisition up into subgroups of 16 samples. The same user-specified trigger event is at the center of each subgroup. During acquisition, an additional subgroup is stored for each trigger event. In this way, up to 32 stored subgroups can give the user a record of triggering occurrences. **Mentor Graphics Corp**, 10200 SW Nimbus Ave, Portland, OR 97223. **Circle 323**

## Logic analyzer teams with computer to test chips

Engineers presently using VLSI design automation tools available on VAX computers can now test chip designs on the Tektronix DAS 9100 logic analysis system. The 91DVV VLSI verification software package from Tektronix creates a close relationship between the VAX host and logic analyzer. This combination implements chip testing more easily and at much lower cost than production testers.

Instrument cards in the DAS perform the tests, while the system interfaces to VAX running Unix. Within the DAS, a pattern generator card supplies the input stimuli. A data acquisition card captures the response outputs, which are then uploaded to the VAX and compared to reference data. Reference data can come from a simulation program, a good device, or the user. Comparison results can be formatted to graphically highlight discrepancies. Test pattern vectors

used by logic simulation programs (eg, Berkeley RNL or Sandia SALOGS) can be down-loaded to the DAS 9100 for use as a stimulation program.

A program reformats the simulator test program to take advantage of the system's algorithmic pattern generation, and allows long sequential test patterns to fit into pattern generator memory. Interactive operation permits stimulus control and acquisition setups, tri-state control, and pattern to pin mapping.

The system runs under Unix 4.1 BSD, with the software composed of several modules that act as Unix shell commands. Test vectors and setup information are pipelined through the modules to conduct the test. The 91DVV software modules convert the



test vectors into the DAS format and download them to the DAS pattern generators. The software exercises the device, collects responses, uploads to the VAX, compares responses to response predictions, and outputs the results. A typical DAS 9100 for this application is about \$40,000. **Tektronix, Inc**, PO Box 1700, Beaverton, OR 97077. **Circle 324**

## Support package allows benchmarking and debugging

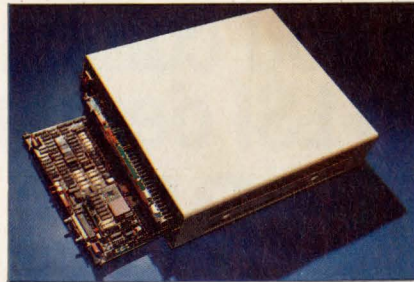
First-time users of the MC68020 MPU can evaluate the chip and start code development with the Benchmark 20 system package. This 32-bit development package includes hardware and firmware for benchmark testing, debugging, and paged memory management. The Benchmark 20 is VERSAmodule-based, and can be configured with existing VERSAmodule boards to provide user target systems. A VME/IO or EXORmacs host system can assemble, compile, and download software for executing the Benchmark 20.

The Benchmark 20 includes two VERSAbus compatible boards: the VM04 32-bit monoboard microcomputer and the VM13 1-Mbyte memory board. Also included is a four-slot VERSAmodule chassis with a power supply, and an EPROM-resident debug monitor named 020bug. The boards and 020bug can be purchased separately.

The VM04 uses the MC68020 at a fixed clock rate of 16.67 MHz. It provides a socket for optional use of the MC68881 floating point coprocessor, which improves speed in arithmetic operations. The VM04 also has an onboard cache, memory management, dual multiprotocol serial I/O ports, and comes with a high speed RAMbus interface.

Designed for use with VERSAbus and RAMbus, the VM13 is a dual-ported, 1-Mbyte dynamic RAM board with parity. The RAMbus interface is specifically designed to enhance VM04 performance, and it allows concurrent DMA transfers on VERSAbus, with RAMbus transfers between the VM04 and VM13. The VM13 has parity generation and error detection circuitry that works with control and status registers for error detection and memory diagnostics. The VM13 uses high density 64-K x 1-bit DRAM devices.

In the Benchmark 20 system, 020bug is resident on the VM04. It allows the user to access any MC68020 internal register, VM04 status/con-



trol bits, timer for benchmarking applications, and any memory-mapped VERSAbus or RAMbus resource. Additional features include two types of power-up, self-test diagnostics, and software drivers to accommodate both serial ports, an operating system bootstrap command, and breakpointing and tracing capabilities.

A cross macro assembler for 020 code, a C language cross compiler,

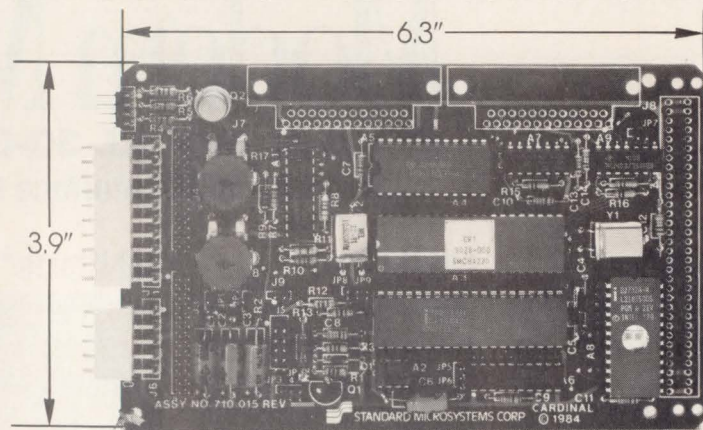
and a cross linker are now under development. An MC68020 cross macro assembler is available. As a single unit, the Benchmark 20 system is priced at \$14,995. The VM04 can be obtained separately for \$6855 and the VM13 for \$4200. The 020bug package can be purchased for installation on the VM04 for \$500. **Motrola Microsystems**, PO Box 20912, Phoenix, AZ 85036.

Circle 325

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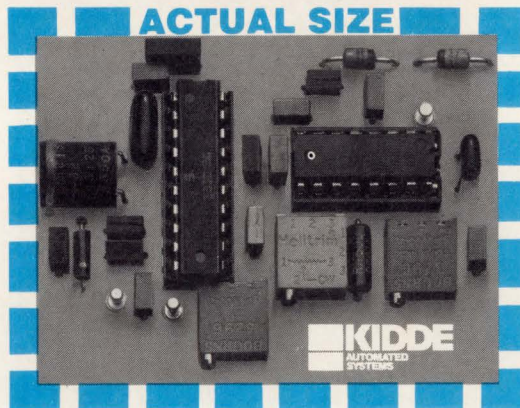
operation and a menu-driven setup mode stored in a non-volatile memory. In fact, the Cardinal is so advanced, you only have to add a power supply, keyboard and video monitor to build a complete video display terminal. To find out more, contact Standard Microsystems Corporation, 35 Marcus Blvd., Hauppauge, NY 11788. (516) 273-3100.

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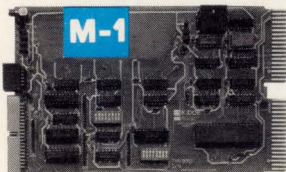
Rate (Mbps/s)	Carrier freq. (MHz)	PG-39 (ft.)	PG-11 (ft.)	J14412A (ft.)	J14730A (ft.)	T41000A (ft.)
1.0	3	5K	12K	20K	32K	50K
2.0	5	4.2K	9.5K	15K	25K	37.5K

\*\*Quantities of 5000.

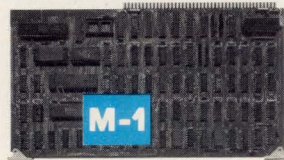
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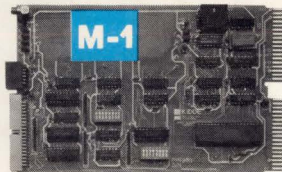
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# SOFTWARE INDUSTRY STRIVES FOR A STANDARD SOLUTION

Corporations, consortiums, and national/international standards bodies work together to define standards that minimize software babble. The result is more versatile systems, without inhibiting proprietary product development.

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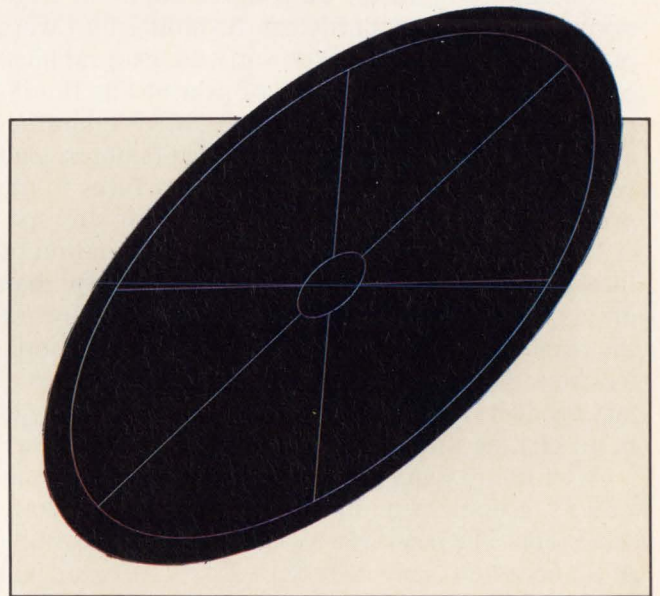
by **Harvey J. Hindin,**  
Special Features Editor

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When it comes to software, the computer designer has a full menu, making choices all the more difficult. A host of groups, both public and private, have worked together in 1984 to organize a software plate. The goal is simple—help the designer in the search for a reproducible, reliable, portable, and flexible standard code for a wide range of applications such as graphics and computer communications.

Microcomputer and minicomputer operating systems do not enjoy the benefits of national or international standardization except in the attempts by individual firms to “declare” standards. But, this year these firms have moved toward more functional operating environments and toward defining operating system interfaces.

While all this has been going on, proprietary products have been developed in operating systems, languages, and almost every kind of software. Some are unique; others are the same old thing. Some address conventional needs such as better compilers. A few look to the fourth, or even the fifth generation of computer technology. In all, many software standardization developments and proprietary products have come forth. The clear promise for 1985



is that the computer system designer and integrator, software developer, and end user will see more of the same.

## What's going on

Private firms, industry consortiums, research organizations, and national and international standards groups are working to provide a common denominator for software standards. Such standards will be based on operating systems, high level languages, communications software, protocol specification languages, graphics software, and compilers and interpreters. Other efforts are aimed at software

for the fifth-generation computer, the current fourth-generation computers, and the artificial intelligence field. These goals allow the designer a choice with market viability.

Developing software standards is no easy chore. Few oppose them, yet each company would like its own software to become the standard without further ado. Since a committee (with all the conflicting interests of its members) does the initial work, the generated documents tend to be minimal standards. Higher level implementation for specific applications is left up to individuals. Nevertheless, standards of sorts are set forth and provide a rallying point for computer designers in today's multivendor environment.

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### *Two graphics standards, NAPLPS and IGES, are already official national standards.*

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A computer industry using agreed-upon international software standards can (excluding hardware problems) enjoy a market with no geographical boundaries. Since each piece of gear has its fundamental software behavior well specified, manufacturers can concentrate on value-added features. End users also have standard software interfaces to the products they use and are less locked into any specific product vendor. Because of a combination of factors, some standards will be more successful than others. Some of these factors include the clout of the firms on the committees, how long the committees have taken to do their work, how many proprietary products already exist, and how difficult it would be to change them to conform to some standard.

After many years of effort by some dozen organizations, graphics standards are finally sorting themselves out. The result is a logical structure consisting of an accepted body of code. All this software will ensure that applications, data bases, and graphics devices can communicate in both low and high end products, regardless of who produces them.

Standards do not inhibit individual innovation or a value-added contribution. Graphics standards are no exception. Standards provide an accepted base for extra features to be built on, and facilitate portability. Proprietary software will still exist, driven by market forces for applications that must have dedicated code to do the job most efficiently.

Each segment of the computer graphics industry has an opinion about what should be standardized, how it should be done, and what functions a standard should supply. While this has held up progress,

the rough outlines of the standards and their functions have been established. Groups such as the American National Standards Institute (ANSI), the Association for Computing Machinery (ACM), and the International Standards Organization (ISO), have all been involved.

The different standards serve different sections of the computer design community. For example, the Graphical Kernel System (GKS) helps the software developer interface to graphics software utilities and tools. Descriptions are given of the graphics objects to be displayed and used by the application software (*Computer Design*, May 1984, p 167). The Core software standard performs similar functions but can handle three dimensions. The GKS is limited to two dimensions, but a three-dimensional version is coming. Another difference lies in the GKS emphasis on the ability to distinguish pictures; Core concentrates on user control.

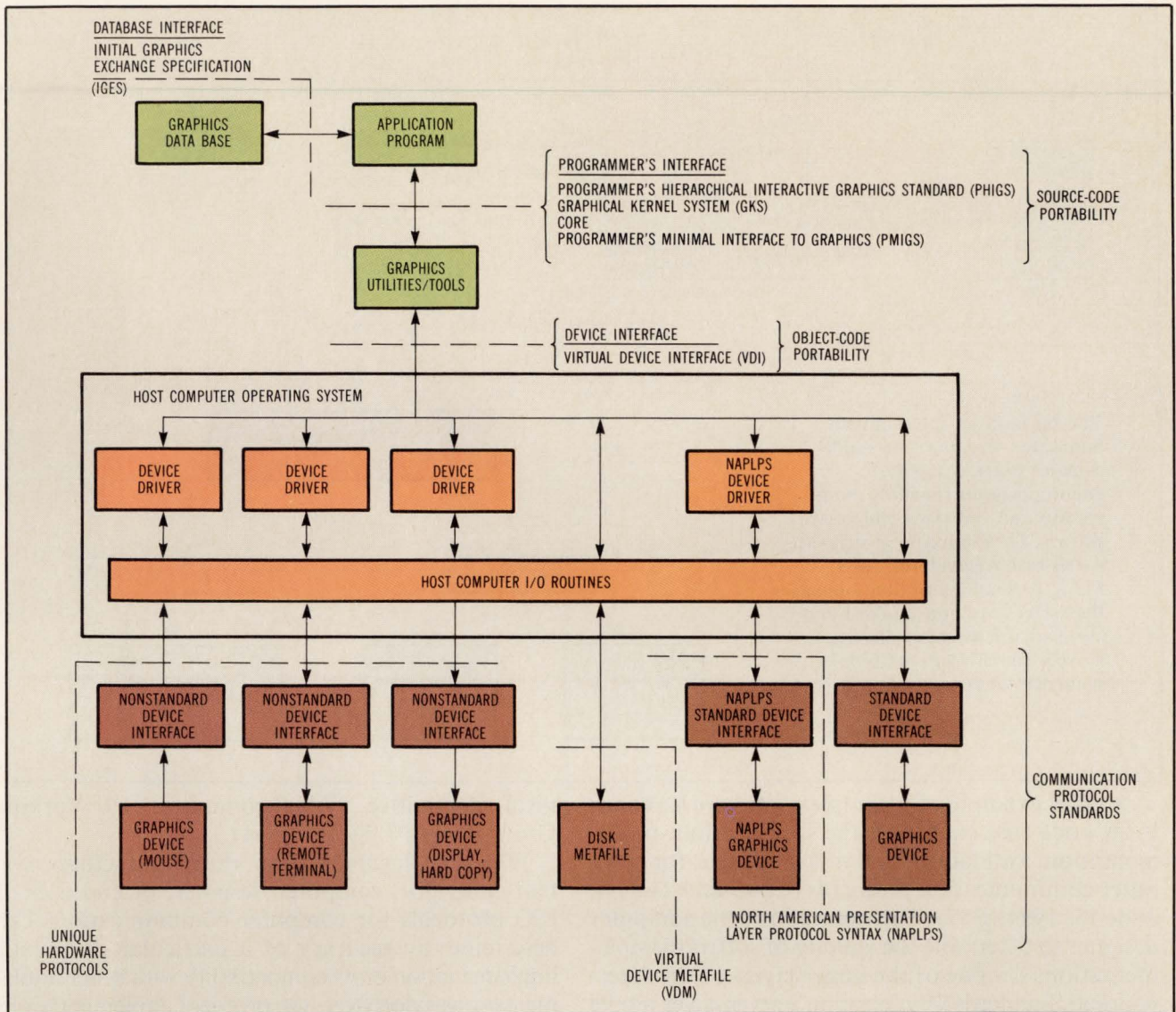
High and low end versions of both standards are also available. The Programmer's Hierarchical Interactive Graphics Standard (PHIGS) is an extended version of Core for computer modeling and simulation applications. The Programmer's Minimal Interface to Graphics (PMIGS) is a minimal GKS subset for business graphics/graphics arts applications.

Many application programs for computer aided design and computer aided manufacturing chores need to call on design and database information. Different database file structures require the software developer to write different interfaces. And, designs built on one computer cannot be implemented on another of a different manufacturer or, often, even from the same manufacturer.

### **Object code portability**

The Core, GKS, PHIGS, and PMIGS software standards concern themselves with source-code portability. In contrast, the Virtual Device Interface (VDI) addresses object-code portability to different host computer operating systems. The VDI is the interface between device-independent code and device-dependent code. It supports as many graphics I/O devices as possible, with as many graphics functions as possible. It may or may not require standard or specific device drivers—or no drivers at all. As market niches become clear, these software drivers or interfaces will appear as VLSI chip implementations.

The key problem for VDI designers is VDI placement in the device driver hierarchy. If it is placed too high, or contains too many functions, device drivers are large and hard to write. On the other hand, if it is placed low or has minimal functionality, device drivers will not be able to use unique or advanced device features. A single VDI standard is still difficult for a standards committee to devise.



Proposed or already accepted graphics standards take care of the interfaces between software developers, computer hardware devices, data bases, and computer communications. Relationships are indicated in the diagram, but no hierarchy is implied.

Several other graphics software standards have been developed for specific needs. One is the Virtual Device Metafile (VDM). Another is the North American Presentation Layer Protocol Syntax (NAPLPS). The former is a file format standard for storing and transmitting pictures. Like the VDI standard, the VDM is a compromise. Devices interfaced through it cannot be used to full potential without additional software. NAPLPS is a software interface between a videotex device driver and a display.

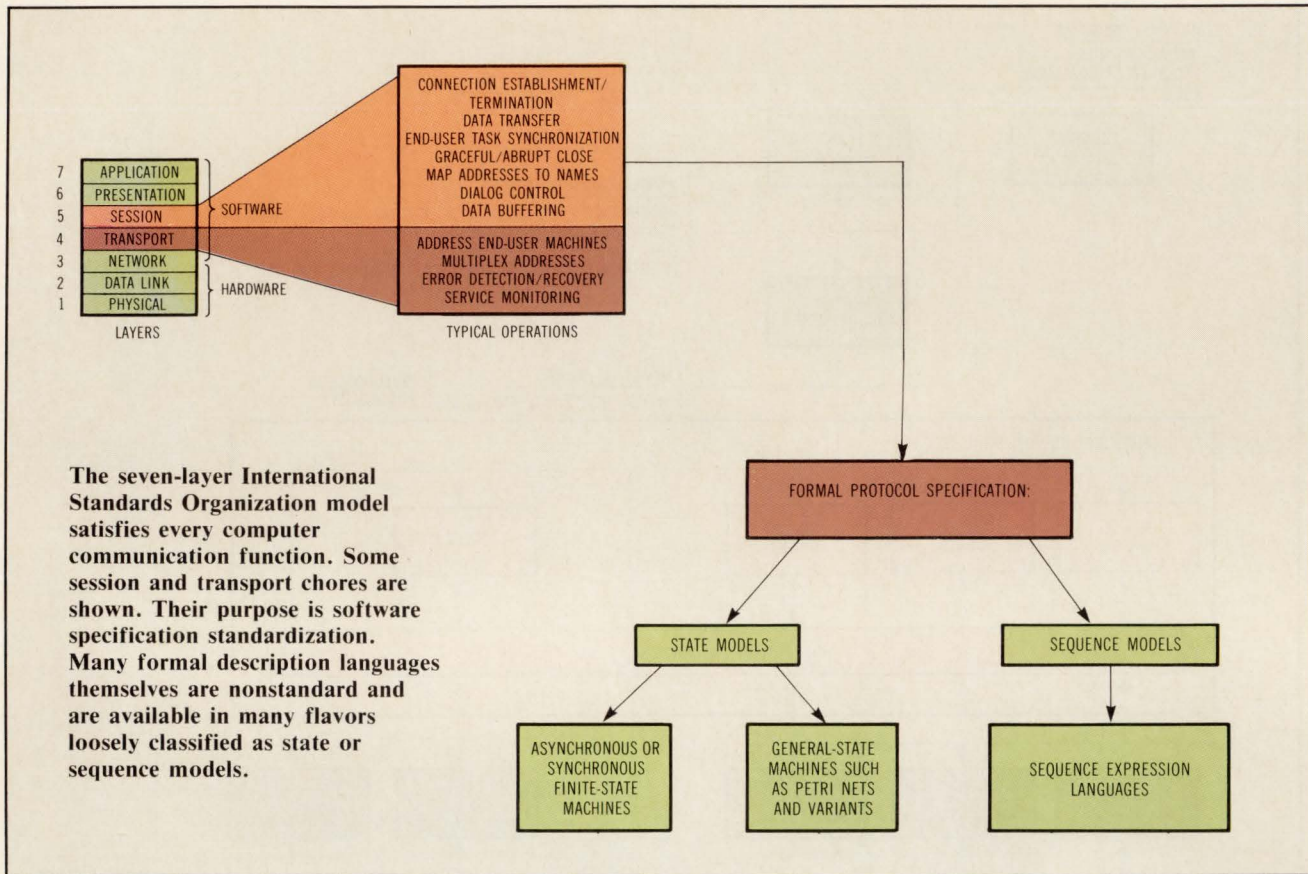
Two graphics standards, NAPLPS and the Initial Graphics Exchange Specification (IGES), are already official national standards. PMIGS, GKS, and VDM are under review. Others still under development are PHIGS and VDI. The GKS is the most advanced of those still being reviewed. Several firms, however, have jumped the gun and have already offered vari-

ous GKS implementations. Some firms offer the less developed VDI.

For years, a variety of Core versions (each a "standard") has been available. In addition, many firms continue to set forth their own proprietary graphics software. Other firms take such software and develop it further. Then they often present standard graphics software such as GKS as an option on their graphics hardware.

### Define that protocol

The process of devising graphics standards will ultimately eliminate many proprietary graphics programs. There is no way around this because of the complex issues that graphics standards software addresses. The graphics standards themselves, however, represent a rather large set of programs.



A good example of a complex software standard is the code that comprises the specification, implementation, validation, and test languages for computer communication protocols (*Computer Design*, June 15, 1984, p 57). This code allows the computer designer to determine the validity of software implementations for one of the upper layers of the International Standards Organization's seven-layer model for computer communications (the Open Systems Interconnection or OSI model).

Besides requiring many thousands of code lines, this software represents a very complex set of standards regardless of the particular implementation. This is so even though ISO just defines the layer's functions and the interfaces between layers; the user must write the code. But, if the standards are followed, and the functions and interfaces are clearly defined (the purpose of formal specification), disparate computers can communicate over very long links (meters or thousands of kilometers in length). These computers can do this even if there are many different software implementations for a particular layer.

In 1984, work has proceeded at a brisk pace on the final versions of formal protocol specification languages for the ISO upper layers. A key upcoming event is the February 1985 presentation of a machine readable, formal description of the transport layer (layer 4), and session layer (layer 5) to ISO's Tech-

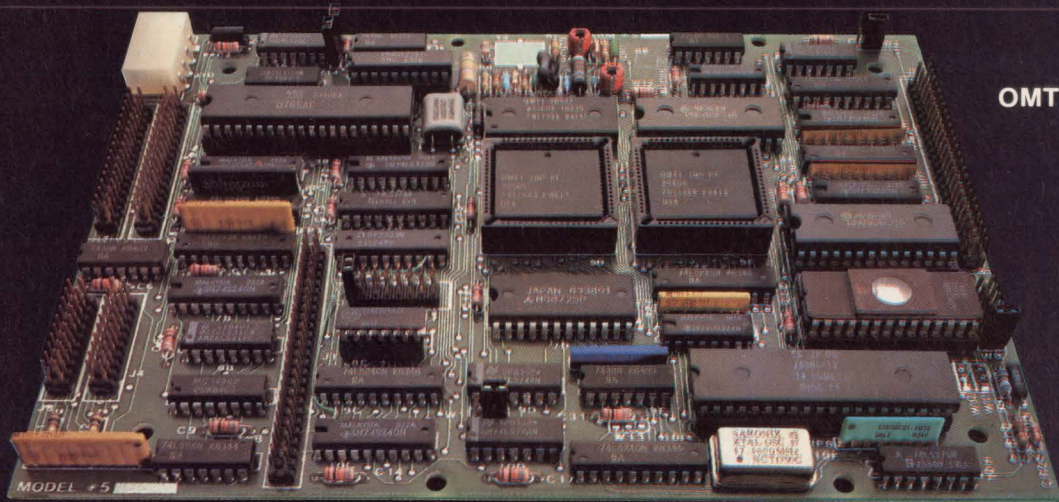
nical Committee 97/Subcommittee 16/Working Group 1 (TC97/SC16/WG1).

With such documentation, the manufacturer, system integrator, computer designer, or end user of ISO protocols for computer communications can determine the accuracy of a particular protocol's implementation or its compatibility with other implementations. Moreover, the protocol implementations can be properly specified, verified, and tested. ISO will eventually specify all seven layers.

A protocol engineering system provides one practical way for computer designers to design, debug, and test protocol software. With the protocol design expressed in a formal, machine-executable specification, its specification can be fed into a compiler. Such a compiler automatically generates a module of software that becomes part of a final software product. The system also derives design and analysis tools and test sequences from the specification.

Work on protocol standards is going on worldwide. Private firms (most notably IBM in Raleigh, NC) research organizations (the National Bureau of Standards, Washington, DC), and national and international standards bodies (the International Consultative Committee for Telephony and Telegraph) are all taking part. Indeed, the CCITT is quite active and has its own formal description language. But, most important of all is the work being done on the

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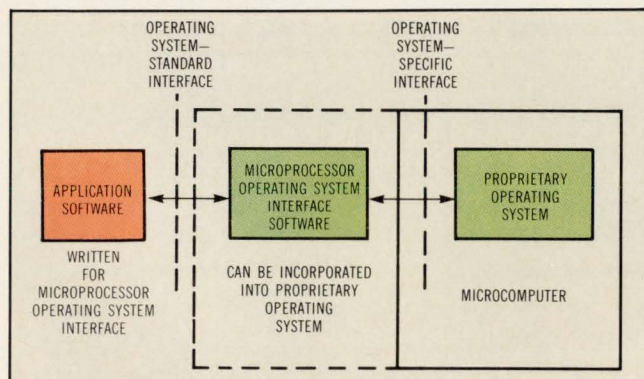
ISO protocol description language. If successful, it is assured of worldwide acceptance. ISO's TC97/SC16/WG1 efforts are divided into parallel efforts by three subcommittees.

The first subcommittee is working on computer architecture specifications that serve as the basis for formal description languages, regardless of type. The second subcommittee is dealing with a finite state machine-based language; the third group is looking into a language based on sequence expression. The second subcommittee is considered to be more mature and less research-oriented. Its language, Estelle, will be used as the basis for the specifications to be presented to the ISO's TC97/SC16/WG1 in February 1985. The formal language specification issue is a difficult one. To attain the best representation, it may turn out that different ISO layers will require different languages. But, ISO committees have begun looking into the possibility of one language for each layer.

### The protocols themselves

The upper-level ISO protocols, which guarantee that computer designers can link computers to access applications and resources, do have competition. This competition comes in the form of IBM's Systems Network Architecture, Xerox's own Xerox Network System (XNS) protocols, and the Department of Defense's Transport Control Protocol/Internet Protocol (TCP/IP) protocols.

None of these protocols will disappear because of their market acceptance or the backer's clout. Still, only ISO can establish international standards. Many firms announced in 1984 that they would opt for ISO on a gradual basis or support ISO concepts. These companies include Digital Equipment Corp, Data General, Burroughs, Honeywell, Hewlett-Packard, Tektronix, Xerox, Intel, Advanced Computer Communications, and Interlan.



The microprocessor operating system interface translates system calls and functions. It will ultimately standardize memory management, file formats, time management, and exception handling.

While the vendor attraction expected for ISO upper layer protocols in 1984 did not materialize, the demand should rise in 1985 as more ISO protocols are made ready. The presentation layer and parts of the application layer should become draft international standards. This is the last step before acceptance as a full-fledged international standard.

Presentation layer chores covered will include transfer syntax for character sets, text strings, file organization, and data types. Application layer tasks include common application services, file transfer, access, and management. How much will be accomplished depends on how fast the committees move and the industry comments they receive. Even DoD is looking to ISO as long as its protocols can deal with survivable network concepts. ISO layers one and two (hardware-based) are well accepted. They have been further implemented in 1984 with a variety of carrier sense multiple access/collision detection (CSMA/CD), and token-passing ring and token-bus networks.

IBM opted for one novel implementation of CSMA/CD this year in a broadband, radio frequency modem-based local network (from Sytek, Inc of Mountain View, Calif). The network works with Big Blue's new AT multi-user personal computer (*Computer Design*, Oct 1, 1984, p 27). On the other hand, IBM announced that its token-passing-based local network for future office applications will not be available for three years.

### Instant standards

While graphics and computer communications standards take years to develop, some software standards are established by single organizations with market clout. IBM's AT software is a good example. Overnight, the Xenix operating system from Microsoft, Inc (Bellevue, Wash) was established as the *de facto* operating system standard for the two- to four-user small business system environment. And, IBM, which established Microsoft's MS-DOS 1.1 and 2.0 operating systems as the operating system standard for 16-bit single-user personal computers, also ensured that MS-DOS 3.0 for the multi-user standalone AT, and MS-DOS 3.1 for the networked AT will be *de facto* standards.

AT&T has also engaged in a massive campaign during the year to convince everyone that Unix System V is a *de facto* standard. It probably will become a *bona fide* standard, given the extent of the campaign, and the lack of viable alternatives. The popular Berkeley 4.1 and 4.2 Unix versions, for example, do not enjoy either promotion or product support by the University of California, Berkeley team that developed them.

### Software Development Trends

	(1984) Greater Production of:	(1985) Greater Production of:
Software Architecture	Portability (layers, modules), object-orientation	Parallel processing, function distribution, fault tolerance
Software Specification	Formal languages such as Estelle (ESTL)	Further development from ISO and CCITT
Software Design	Expert systems, top-down, bottom-up	Software workstations, AI workstations
Software Languages	Fourth-generation work, functional programming, Ada compilers	Fifth-generation work increases, data and demand-driven applications, Ada applications
Software Testing	Simulators, development systems	Test generators

There are a number of other Unix versions (either licensed from AT&T or developed independently and including some from IBM). But, they are mostly offered by smaller firms not equipped for major development. For example, AT&T is going along with the porting of System V to the full 32-bit microprocessors. Such microprocessors will be

offered by Intel, National, Motorola, and Zilog—ensuring AT&T's place in future microcomputers, supermicros, and minis.

Many other operating systems for both microcomputers (*Computer Design*, July 1984, p 155) and minicomputers (*Computer Design*, August 1984, p 165) have been introduced this year. According

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to industry sources, new introductions will be made in 1985. None of them will impact the market share of MS-DOS for microcomputers or Unix for minicomputers. Unix dominates the minicomputer operating system market. It is enjoying the addition of fault tolerance and realtime features. And, although it is portable, it has competition only in the form of nonportable, machine specific, proprietary operating systems from minicomputer vendors.

Early operating systems were monitor programs that simply ran hardware. While most microcomputer and minicomputer operating systems are not becoming standards, they are much more useful to the computer designer than mere monitor programs. For this reason, they are often called operating environments.

The latest operating systems offer a rich set of services. They allow application programs to interact with graphics, graphics standards, light pens, touch screens, and other multiple application programs. In addition, multiple file formats, fault detection, multitasking, multiprogramming, I/O control, communications with multiple protocols, and more are possible with these systems.

This embarrassment of riches makes the choice of an operating system difficult. Adding to the problem are application programs that will run on only one operating system. Thus far, the various schemes proposed to solve this problem have been unsuccessful. The Softech p-System (San Diego, Calif) for example, achieves object-code portability by having applications written only once for a hypothetical p-machine emulator for each microcomputer of interest. The application talks to the p-machine emulator and the emulator talks to the target microcomputer. Perhaps because the approach is promoted by just one firm—and is looked upon as yet another operating system (which it is)—the p-System is not very popular.

### No moss on MOSI

The IEEE's Microprocessor Operating System Interface (MOSI) Task Force 855 has written a standard operating system interface allowing application programs to communicate with diverse operating systems. In operation, the interface allows application software to be written for its standard interface "side." This interface converts the application software so it can communicate with the particular operating system connected to the interface's other "side."

Because the interests of the MOSI committee are so diverse, the standard has four parts, each accommodating a different viewpoint. Like most standards, only minimal rules are set up in order to achieve consensus. The question of how to deal with

file systems has been addressed and will be included in the standard in its 1985 presentation to the IEEE.

Given the number and advanced state of microcomputer operating systems, no one knows if MOSI will have any real effect. In any case, there are two design options. Application software can be written for a specific MOSI interface to interpret such software for a particular operating system. Or, designers of new operating systems will conform to the MOSI interface and application software with a MOSI interface that can run directly.

Other operating system standards efforts include various industry and user groups working to standardize Unix. Unfortunately, they work in the shadow of AT&T and IBM. While AT&T announced that it will upgrade system V to include many Berkeley-like and other features, the pace and order of implementation are unknown. IBM already offers a single-user Unix on its XT personal computer, the licensed version of Unix known as Xenix on its multi-user AT, and various licensed Unix versions on its mainframes and minicomputers (*Computer Design*, Aug 1984, p 44). It is also capable of coming out with its own version of Unix.

Many other products introduced this year are specific to particular problems, such as multipass compilers to produce tight code and interpreters. Still others are related to different standards problems, such as windowing programs. Each product claims to be the *de facto* standard for window-using application programs.

All such claims are blown out of the water by IBM's announcement of its own brand of windowing software. To show how serious it is about its Topview, IBM has taken the unprecedented step of giving it away free to selected software developers. There is no standard windows package for microcomputer software developers yet, but Topview has a good chance because of IBM's market domination.

Even proprietary products developed this year have tried to minimize software babble problems. For example, Pyramid Technology Corp (Mountain View, Calif) ported Unix System V and Berkeley 4.2 onto one operating system of its own design to run on its own superminicomputer. Apparently, this is an attempt to keep the users of both operating systems happy.

### Fourth generation

There has been much talk about software for the so-called fifth-generation computer (*Computer Design*, Sept 1984, p 150). But, the fifth generation is not due until the 1990s. For the time being, users of the 1980s' computers will make do with the fourth generation whose features are a little clearer and more amenable to implementation.



Some of these features have begun to appear in the 1984 products while others are still in the research stage. In any case, the software developer, computer system designer, and computer system integrator pushing for fourth-generation languages or procedures have a massive inertia problem to overcome. The installed software base is so large that it is not economically viable to change over.

*A standard operating system interface allows application programs to communicate with diverse operating systems.*

The question of new languages is a good example of this problem. Most software is written in languages that have been around for many years. Yet newly developed languages offer distinct advantages. Nial, a language developed by Kingston, Ontario, Canada's Nial Systems Ltd, supports functional programming by combining the properties of Lisp and APL (see *Computer Design*, Apr 1984, p 29). Designed as an interactive and extensible, fifth-generation language, Nial can be used in the 1980s to offer software developers the full benefits of

both structured and functional programming (see *Computer Design*, Sept 1984, p 150) for expert systems, logic programming, computer aided design, and data bases.

**Tracking the AI effort**

Expert systems are part of the artificial intelligence effort that has been so much a part of worldwide software development efforts this year. Even Unix and its associated language C got into the AI act with an object-oriented version developed for AI applications (see *Computer Design*, Apr 1984, p 47). The important AI languages, however, remain Smalltalk, Lisp, Prolog, and OPS-5. Many firms have offered them on dedicated AI workstations or more traditional mainframes and minicomputers (and even micros).

For example, Tektronix, Inc (Beaverton, Ore) introduced an AI workstation based on the object-oriented Smalltalk environment from Palo Alto, Calif's Xerox, Inc. And, Texas Instruments, Inc (Dallas, Tex) introduced a dedicated AI workstation running Lisp. Finally, some of this year's software work has been partly spurred by the lure of parallel processing architectures. And, efforts continue on language environments for dealing with time, as well as with the various control-, data-, and demand-driven languages.

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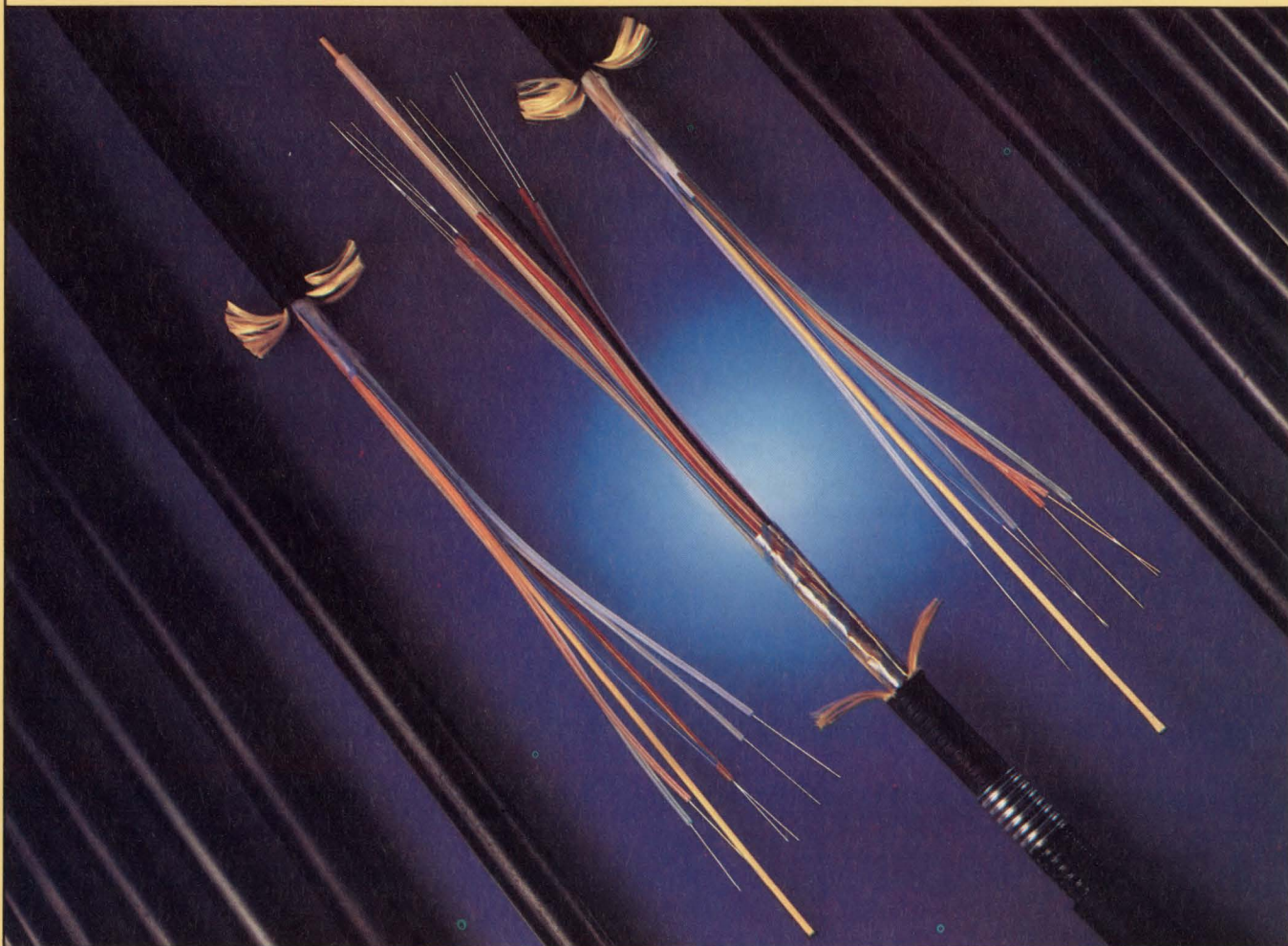
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## Multitasking Unix look-alike supports 11 IBM XT users

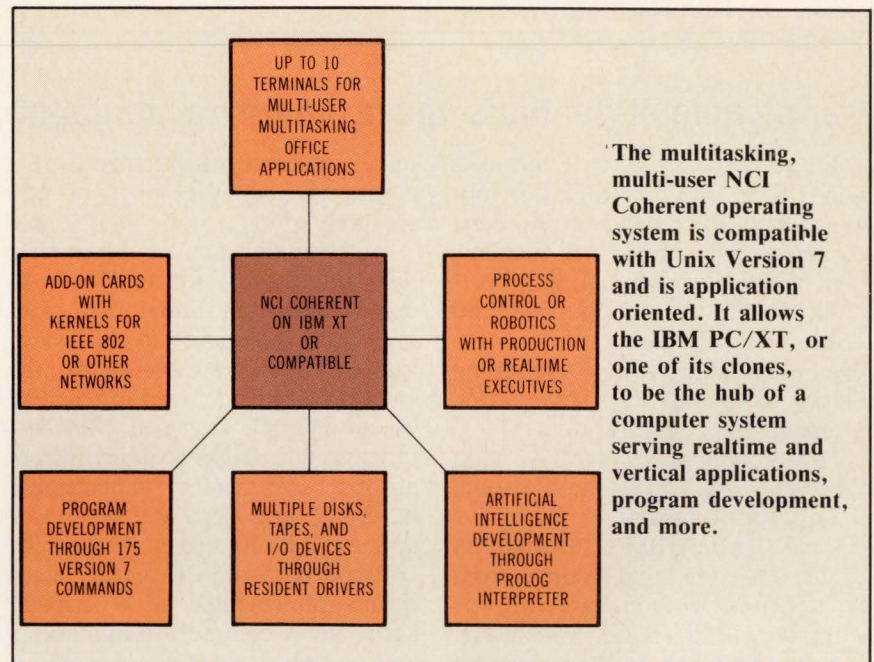
Many computer designers believe that the last thing they need is yet another Unix look-alike to add to the bewildering array of similar operating systems. However, an alternative now exists that makes a multi-user Unix available on the IBM PC/XT and its clones. This look-alike also offers runtime or production operating system versions at a greatly reduced price and furnishes the tools for easy program development of multitasking, multi-user Unix Version 7 compatible software.

Network Consulting, Inc has taken the Coherent operating system, a two- to three-user multitasking Unix look-alike and adapted it to a multi-user environment on the industry standard PC/XT. Using the Unix Version 7—which is compatible with the NCI Coherent—and hardware added to the IBM PC/XT, up to 11 users can simultaneously operate the PC/XT. The system can handle many vertical applications, including order entry, record keeping, and other office activities.

To design its operating system, NCI, under license, made major changes in the Mark Williams Co's (Chicago, Ill) two- to three-user Coherent operating system. Coherent, itself, was developed independently from the original AT&T Bell Labs Unix Version 7, but was designed to be a look-alike. In particular, parts of the original Coherent kernel have been rewritten for faster multitasking operations. For example, new serial line drivers, disk driver DMA interrupts, and schedulers all result from the NCI design.

A variety of other modifications are implemented with the goals of making the NCI operating system Unix-compatible and optimizing the system for designers and software developers. For example, the 165 to 175 Unix Version 7 commands are geared toward allowing software developers to create Unix-compatible applications to run with either a runtime or production operating system version.

In order to ensure faster execution of Unix Version 7, NCI rewrote the Coherent mathematics library in assembler and reworked some features of the kernel code, including the



The multitasking, multi-user NCI Coherent operating system is compatible with Unix Version 7 and is application oriented. It allows the IBM PC/XT, or one of its clones, to be the hub of a computer system serving realtime and vertical applications, program development, and more.

scheduler and the C library. NCI Coherent also incorporated such Unix system memory routines as memcopy, memchr, memcmp, memcpy, and memset, which ensure memory locks and shared memory. These make Unix System V compatible with the multitasking NCI Coherent kernels written for various IBM XT add-on cards, such as an ARCnet card and the 8088-based Persyst smart serial interface card. Computer designers opting for this hardware can enjoy, for example, RS-232-C based networking with hardware handshaking and flow control. By design, realtime interrupts go from the Persyst card by message passing to the XT's operating system kernel.

All these features have been incorporated with an eye toward designing an application-oriented operating system that presents more than just an elaborate monitor program. For example, the PC/XT can be used as a database-oriented machine such as a data multiplexer. It has such built-in networking features as log-in, password, encryption, and file protection. The XT can also serve as a protocol converter, allowing up to 50 different kinds of terminals on a multi-user system to communicate using the Berkeley termcap data base. Finally, it can monitor a private branch exchange and log telephone calls.

The NCI operating system uses 2.5 Mbytes compared to 5 Mbytes for the Interactive Systems' single-user, multitasking licensed Unix for the PC/XT (and about 8 Mbytes for Unix itself). This is because the TROFF utility program, the Unix dictionary, and some macros are not included. Space is saved because NCI Coherent is not the same as Unix and, therefore, has been written differently. Use of even shorter run time or smaller production kernels—which NCI will help develop for computer system designers—further minimizes the code size.

The NCI Coherent operating system allows a computer network system to be IBM PC/XT-based with up to 10 remote terminals at a price competitive with that of a dedicated multi-user Unix system. Depending on the hardware configuration used, the NCI Coherent operating system could be more cost effective than multi-user Unix systems.

The PC/XT with NCI Coherent is 1/50 the cost of the DEC VAX traditionally used for Unix-compatible package development, has about 1/10 the power, and needs no support. **Network Consulting, Inc**, Discovery Pk, Suite 110, 3700 Gilmore, Burnaby, BC, Canada V5G 4M1.

Circle 326

## Mainframe-style tools move down to personal computers

Unix ports to the IBM PC promise mainframe-style software development support at a relatively low cost. Programs and utilities, such as source code debugging (sdb) and lint (portability analysis), previously found only on larger machines, ease the task of high level language programming on personal computers. Multitasking is added in as an extra treat.

Unix comes in various flavors on the IBM PC. Both the Personal Computer Interactive Executive (PC/IX), from IBM's Information Systems Group; and Xenix, from Santa Cruz Operation, base their versions on AT&T's Unix System III. VenturCom bases its Venix/86 port on the earlier Version 7 release. These ports have been enhanced with utilities taken from other Unix versions (eg, Berkeley 4.2) as well as modifications (eg, file and record locking) not found in Unix itself. Such variety may diminish as these vendors move toward the System V specification favored by AT&T.

There is, however, no completely efficient way of moving Unix to the micro world. Users of PC-based versions must sacrifice some performance in exchange for the power provided by the utilities and multitasking capability. Computation-bound or disk-bound operations will execute more slowly on personal computers than when executed on larger multi-user hosts. On the other

hand, interactive tasks such as text editing have better response on a personal computer.

Its beginning as a minicomputer operating system makes Unix oriented toward machines that offer multitasking support in hardware, rather than microprocessors like the Intel 8088 that are most efficient at executing single programs. Most visibly absent in 8088/8086 processors are extensive memory management hardware and separate supervisor and user address spaces. As a result, Unix ports to the PC modify algorithms implemented in the original kernel to overcome the limitations and optimize performance.

Beyond the lack of memory management hardware is the lack of a nonprivileged mode that separates user operations from supervisor operations handled by the kernel. This is typically handled through different logical address spaces. As a result, any user process can alter its base registers and perform operations anywhere within main memory.

Bypassing this obstacle, PC/IX calls for programs to be written in a "small" mode, whereby the program never modifies all segment registers. This limits program size to 64 Kbytes, but allows these registers to separate user processes from kernel operations.

Both Venix/86 and Xenix approach the problem differently to

take advantage of segment manipulation. Both implement a "middle" programming model that allows user processes to dynamically modify the code segment register. This allows code segments to exceed 64 Kbytes.

To implement memory management within this scheme, Venix/86 breaks a large code segment into smaller pages. This facilitates code swapping, and a mapping table is always resident in memory. In contrast, both PC/IX and Xenix implement no such scheme for code swapping. All three ports limit user data and text spaces to 64 Kbytes each.

Similar modification schemes in the porting process do not necessarily mean that the kernel is the same size for all versions. On the contrary, kernel size ranges from 50 Kbytes for Venix/86 to over 128 Kbytes for Xenix. Each vendor has also made individual choices on which enhancements it wishes to make to the original Unix version.

Santa Cruz Operation (SCO) has chosen to enhance its System III version with capabilities not found in the original AT&T specification. File protection and error recovery procedures are most notable. Since Xenix is intended as a multi-user operating system, file and record locks are provided to prevent one user process from corrupting the data of another. File recovery procedures are also provided in case of disk crashes.

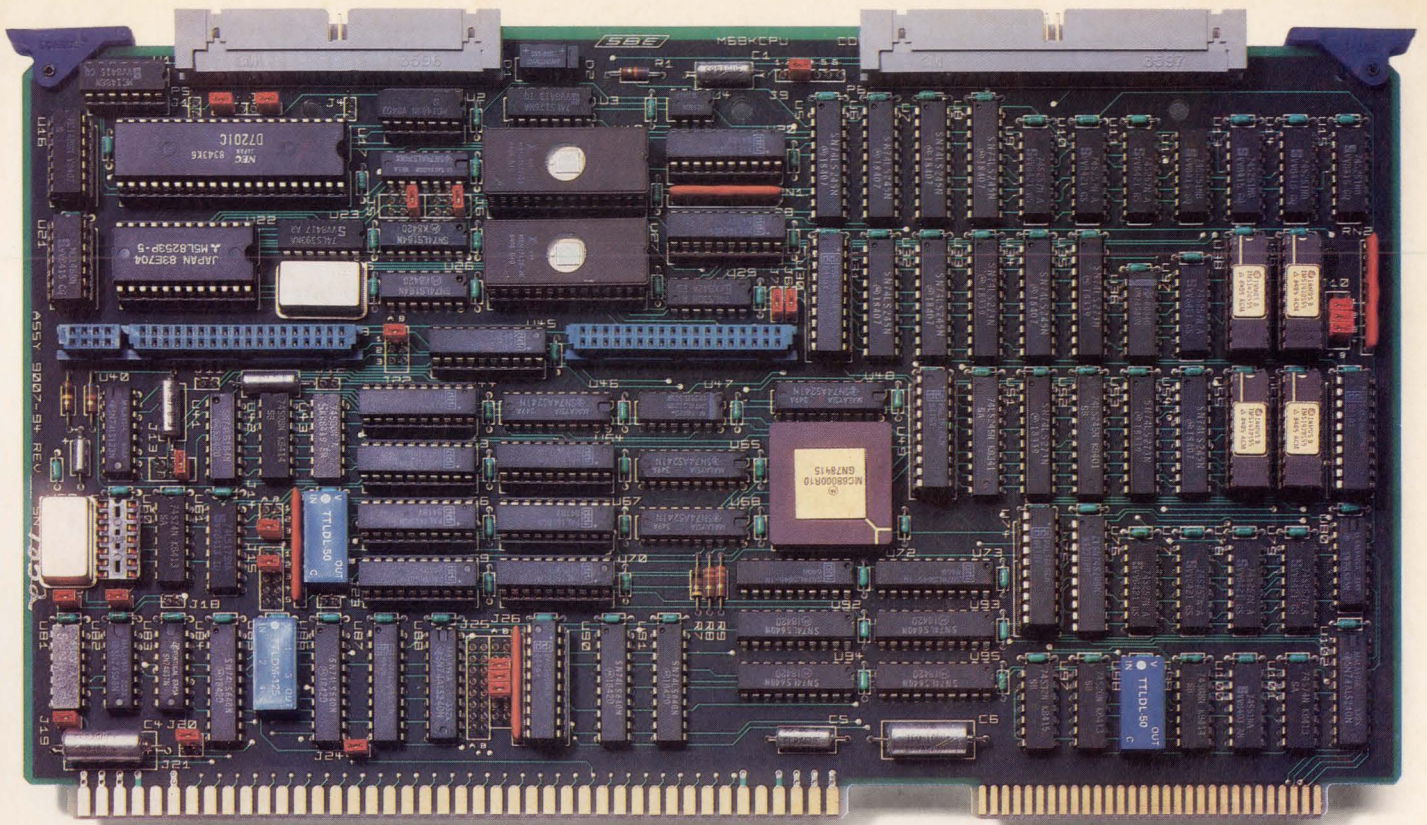
In contrast, both Venix/86 and PC/IX make no provision for memory protection. Vendors for both systems contend that the probability of file corruption is so small that it does not justify the extra code needed to implement file protection. Furthermore, file protection might hinder software development (the primary application area for both systems) because programmers desire free access to physical resources.

Enhancements to the kernel, such as file protection and floating point support, affect memory requirements

*(continued on page 230)*

Comparisons of Unix Ports to the IBM PC

	IBM PC/IX	SCO Xenix	VenturCom Venix/86
Unix-licensed versions	System III single-user	System III multi-user	Version 7 single- or multi-user
Suggested memory requirements	512-Kbyte RAM, two 10-Mbyte rigid drives	384-Kbyte RAM, one 10-Mbyte rigid drive	256-Kbyte RAM, one 10-Mbyte rigid drive
Suggested no. of users	1	2 to 3	2 to 3
Memory protection	none	File/record locks	none



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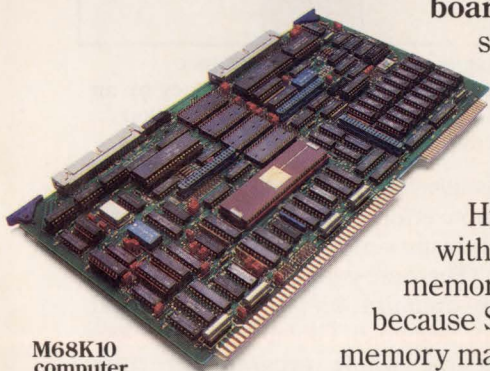
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### Mainframe style tools

(continued from page 228)

as well as the number of users able to log on to the system. Desired sizes for main memory run from as little as 256 Kbytes for Venix/86 to as much as 512 Kbytes for PC/IX. All three versions work best with one 10-Mbyte rigid disk drive acting as auxiliary storage. A second 10-Mbyte rigid drive with the IBM version is suggested for additional storage.

Within its 256-Kbyte memory, Venix/86 will support as many as three users. Xenix recommends 384 Kbytes for the same number of users. On the other hand, PC/IX supports a single user with its suggested 512-Kbyte configuration.

Program utilities and software tools take a big bite of the memory not reserved for the kernel (always resident in main memory). The command shells can easily occupy 50 Kbytes, with compilers and editors each grabbing as much as 60 Kbytes. A full Unix system with utilities and shells can take up as much as 6 Mbytes without taking application programs into account.

Furthermore, both PC/IX and Venix/86 allow MS-DOS programs to coexist on the same rigid disk. For example, PC/IX can occupy 7 Mbytes of a 10-Mbyte rigid disk, with the remaining 3 Mbytes reserved for MS-

DOS applications. Utilities are provided for file transfers between the two systems. IBM suggests a second rigid disk drive to allow both faster access to programs and data, and to handle larger programs running under each operating system. **Santa Cruz Operation, Inc.**, 500 Chestnut St, Santa Cruz, CA 95060; **IBM Corp, Information Systems Group**, 900 King St, Rye Brook, NY 10573; **VenturCom**, 215 First St, Cambridge, MA 02142.

Santa Cruz Operation, Inc—Circle 327

IBM Corp—Circle 328

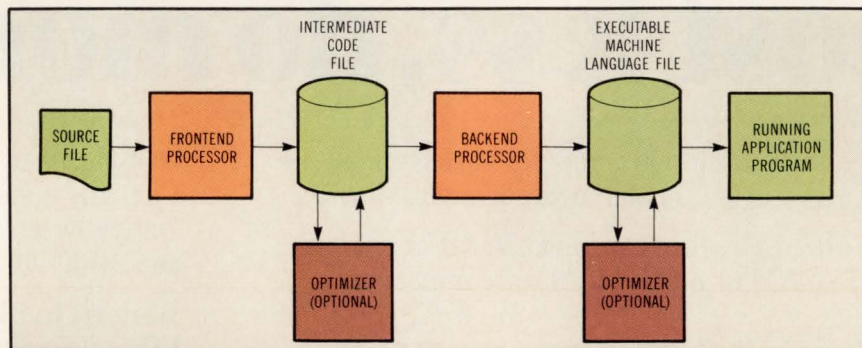
Venturcom—Circle 329

## Multistage compilers go from mainframes to micros

Although multistage optimizing compilers have been available on mainframe computers for a number of years, they have only recently become available for micros. Announcements from Language Processors, Inc, TeleSoft, and Digital Research, Inc illustrate this trend.

There are several advantages to multistage compilers. A multipass compiler creates intermediate code files, which describe the program as written for a simple abstract machine, rather than going directly to machine code for a particular microprocessor. This additional step allows the compiler writer to optimize the program's logic and storage use. Common intermediate code files also let the programmer "mix and match" routines from different languages to produce a given program. An example given by Language Processors includes writing the main logic of a program in Pascal, and including a Cobol routine for handling files.

Writing compilers for many languages also becomes easier. The architecture of the abstract machine, though simple, can be made powerful enough to handle all high level language constructs while still mapping



**Multistage compilers first process source-language (text) files to produce intermediate code files. These files can be further processed for efficiency by an optimizer. The intermediate code file is then processed by a "back end" that generates and (optionally) optimizes executable machine code files.**

easily onto a given microprocessor's instruction set. Furthermore, for a given microprocessor (eg, the 68000), only one machine language-generating "back end" needs to be written.

Single-stage compilers generally handle functions including processing the source-code file, optimizing code, and generating machine code. Including these and other functions makes compilers large, complex, and difficult to program and debug. A multistage approach breaks the various functions into separate programs, making the programming effort much more manageable. Such modules are

smaller and easier to understand, and more effort can be devoted to making them powerful and efficient.

There are two different approaches to optimization—global and local, (or peephole). Global optimizers look at the whole program structure, identify and eliminate sections of code that will never be executed, optimize register usage, and generally streamline the logic. Peephole optimizers, on the other hand, generally look at only a few instructions at a time. These optimizers move constant expressions out of loops and find more efficient machine instructions

to perform a given function. In general, global optimizers are more suitable for processing intermediate code files, while peephole optimizers polish and accelerate machine language implementation.

As with any technique, there are trade-offs in optimizing. The optimizer can be designed to produce fast code (reducing run time) or compact code (decreasing storage requirements). A balance point exists between the two, and choosing depends on the experience and judgment of the compiler writer or designer. There are trade-offs in the degree of optimization too—the more detailed and thorough the optimization, the more time that compilation will take. Alternately, a fast compiler with an unsophisticated optimizer will produce less than optimal code.

Language Processors, Inc has compilers that run on 68000-based Unix

systems for Cobol, RPG-II, Pascal, and C, with PL/1 and Basic to follow. All use what the company calls its "component architecture," a modular architecture with five standard subsystems: a front end, an optimizer, a code (machine language) generator, a runtime library, and a high level debugger. The programs all use the same indexed sequential access method (ISAM) to handle data files. Thus, programs written in one language can address and use files written in another.

The compilers are being offered to hardware manufacturers at \$50,000 plus royalties, based on the size of the system on which they are used. Single copies with runtime distribution licenses are also available.

TeleSoft has made multistage compilers part of its Ada development effort from the start. Since Ada is such a large and complex language, the

sheer magnitude involved in developing a compiler for it almost mandates a stage by stage approach.

Building on experience gained with the UCSD p-System, the company developed a proprietary operating system, called ROS. It has since moved on to produce compilers that run under Unix, IBM mainframe operating systems, on the VAX, as well as on the IBM PC and its clones.

Digital Research, Inc has announced its adherence to the philosophy of multistage compilers. In fact, the company has announced that all of its languages will henceforth have multistage compilers, and be able to exchange object modules. **Language Processors, Inc**, 400-1 Totten Pond Rd, Waltham, MA 02154; **TeleSoft**, 10639 Roselle St, San Diego, CA 92121.

**Language Processors, Inc—Circle 330**

**TeleSoft—Circle 331**

## Big Blue makes a major push to link computers

Code-named VM/IX, this IBM licensed version of AT&T's Unix operating system clarifies the line of march that IBM is taking toward networking workstations, terminals, microcomputers, minicomputers, and mainframes. Operating as tasks under IBM's interactive VM mainframe operating system, the VM/IX operating systems serve as IBM's next step on the way to accomplishing its networking goals.

The VM/IX operating system and specific machine-tailored versions will eventually operate on IBM mainframes that run VM, as well as minicomputers such as the 43XX series, Series/1 machines, the XT/370, and the IBM XT itself. In short, computer system designers will be able to link such machines in Unix-controlled communication networks while the machine's native operating system is handling the specific computing chores.

VM/IX is the result of IBM's work with Interactive Systems Corp. Inter-

active developed the single-user Unix for the XT that became IBM's PC-IX operating system. VM/IX is right in line with IBM's long-term goals. Currently, IBM dominates the mainframe market. Thus, the first goal is to make sure that other computers/workstations that are directly connected to an IBM mainframe remain IBM machines running IBM operating systems. The VM/IX will help ensure that this goal is met.

The second goal is to ensure that IBM minicomputers grow in market share (Digital Equipment Corp dominates the minicomputer market), and that IBM micros continue to be best-sellers. IBM feels that improving the product, cutting the price, and allowing networking through the use of VM/IX builds the strategy for achieving this goal.

The Unix operating system was chosen for this application because it can run on almost any machine. It is portable because of its design and its C-code, which has minimal hardware

dependencies. (C is a language midway between assembler and a high level language.)

In addition to its utilities and program development tools, Unix is the only portable operating system with so much experience and exposure. Thus, while most operating systems are proprietary, Unix can run on any manufacturer's minicomputer. Moreover, it allows system designers to link, not only IBM minis, but products from other companies such as DEC, Data General, Hewlett-Packard, and Gould. As a bonus, the system designer can link IBM's Motorola 68000-based 9000 Series scientific minicomputer/workstation. Because it already runs on Microsoft Corp's Unix-licensed Xenix operating system, conversion would be reasonably straightforward.

This common VM-based operating system can serve as the basis for network communication either using a peer-to-peer or master-slave variation

*(continued on page 232)*

## Big Blue makes a move

(continued from page 231)

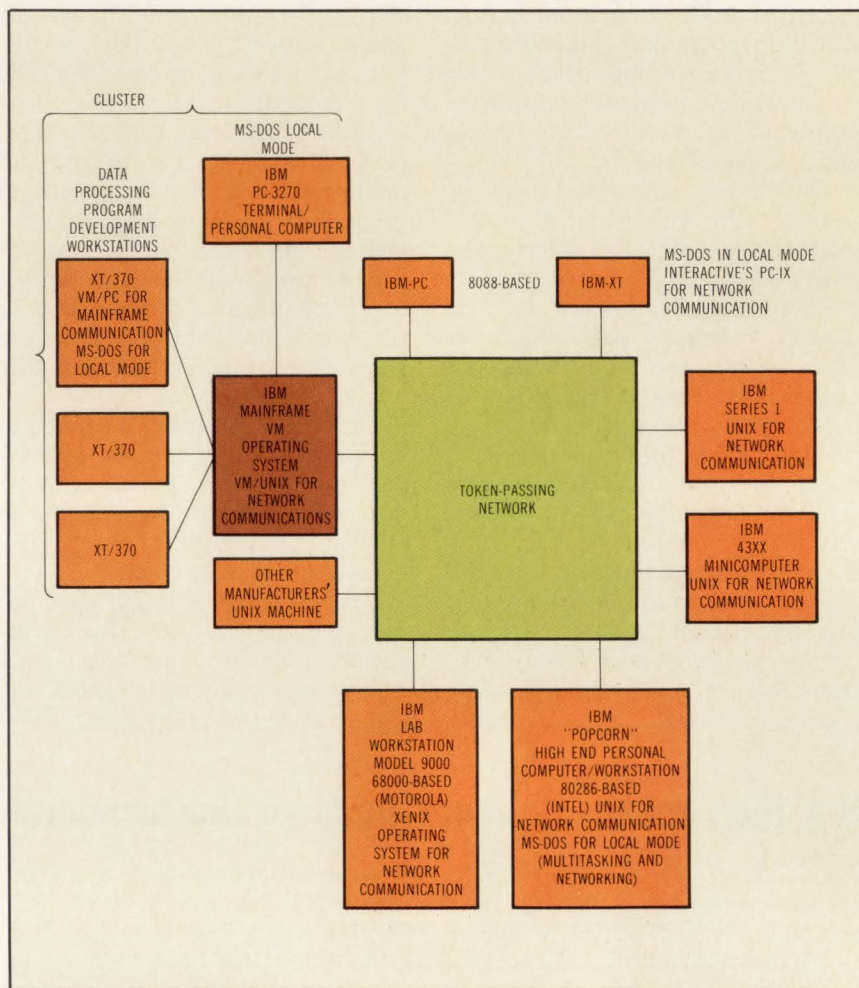
of IBM's Systems Network Architecture (SNA) or the Internal Standards Organization (ISO) seven-layer model for computer communications. In some cases, the software that takes care of these protocol functions will run on the operating system in the computer. In other cases, for the sake of low overhead, it will run on a frontend processor. And, for those just needing a personal computer/workstation and a mainframe link for program development, there is IBM's VM/CMS approach, which will be network-linkable through the mainframe.

VM/CMS links the program development/personal computer XT/370 to a mainframe through a common operating system. This is done without using Unix, whose capabilities are not needed for this application. The XT/370 was introduced mainly for local development of mainframe programs under VM. But, it also allows the use of MS-DOS-based personal productivity software in a local mode.

IBM moved portions of its VM/CMS operating system to the XT/370 so it could become the micro part of a micro-to-mainframe link's common operating system. This link, specifically designed for professional program developers of mainframe and minicomputer software, is geared to the mainframe/XT/370 subnetwork (cluster).

In part, IBM introduced the VM/CMS operating system because it already exists on mainframes. The existence of the same operating system on both sides of a micro-to-mainframe link facilitates file access, information transfer, and program execution across the connection. Moreover, a cluster of XT/370s operates as a standalone or communicates with networked computers through a mainframe.

VM/CMS offers advantages on the mainframe side of the link also. Here, it is used for data processing, software program development, and many management information system departments in major firms



The communications link hooking all the departments in the corporate environment will feature a Unix-based communication system that links IBM and other vendor's machines regardless of type. Both local and remote machine operation will be possible. Each machine will be able to access data or programs from the others and will perform either general purpose or dedicated functions.

already know it. This saves learning time as well.

VM/CMS will run in standalone mode on the 4301 and 4311 machines—tying IBM's computer network world together even more tightly. These high end, desktop superminis allow all the functions of such machines for computer designers. Designers must also realize that upcoming engineering and scientific applications (eg, on the 43XX series) will cut into workstation applications heretofore dominated by firms like DEC and Data General.

IBM is not the only company using VM/CMS. Several manufacturers of

micro-to-mainframe links are porting their software to work under this operating system. Once data is downloaded from the mainframe to the XT/370, it can be directly transferred from the VM operating system to the PC-DOSs application. The XT/370, by design, can look for and read mainframe directories and access files, downloading them to the PC-DOS operating system. **IBM Corp., Information Systems Group, 900 King St, Rye Brook, NY 10573.**

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CIRCLE 97

## Lisp/APL merger supports functional programming concepts

Nial is a very high level, fifth-generation programming language with features that can prove highly beneficial even to the most skeptical software person. Synthesizing ideas from APL, Lisp, and structured and functional programming, interactive Nial (a mnemonic for nested interactive array language) is a functional language. Like Lisp, it allows creation of new operations and transformers, and can treat programs as data. Like APL, Nial is terse, and based on data objects that are treated as arrays. But, unlike any other language—even array-handling ones—Nial carries the array-as-data-object concept further. It can easily work with nested arrays or even with arrays of arrays.

Nial applications include expert systems, computer aided design, and data bases. Thus, it has already been used to do chores in logic programming, prototyping, VLSI programmed logic array generation, forms management, and data system design. Designed to operate with such operating systems as AT&T's Unix and IBM's DOS and VM/CMS, Nial has unique debugging tools. It can display the contents of its array-based data structures even as calculations are in progress.

Perhaps most important for the designer using Nial as a thinking tool is that the language is extensible. Like Lisp, its software mechanisms allow newly created operations to be used in exactly the same ways as predefined ones. The new operations are created incrementally either in successive interactions or by reading a script file containing definitions.

In Nial, an operation can be applied to any kind of data. Thus, it is ideal for experimenting with problem solving. Programmers can try a possible command and learn immediately if it is correct. Interpreted Nial, like APL and Lisp, executes each of its input commands immediately. In short, programmers can see how the data is transformed by the operation they are defining.

```
# GETFILE - Make a list of lines of characters from a text file.
Each line of the file is made an item of the list. Parameter
required is the file name you wish to read from.
```

```
getfile IS OPERATION Fname {
  A := open ( Fname "r" );
  IF ??~ = type A THEN
    Lines := vacate'' ;
    Line := readfile A ;
    WHILE Line ~ = ??eof DO
      Lines := Lines append Line ;
      Line := readfile A ;
    ENDWHILE ;
    close A ;
    Lines
  ELSE
    A
  ENDF
}
```

**Nial provides library scripts for use within the system. These are documented in its help facility and can be accessed using the "library" operation. The sample shown is designed for file handling.**

The advantage of this language design is immediacy. When all the statements required to solve a problem have been proven, the log of the programming session can be edited. Only those commands that worked are edited into the final program.

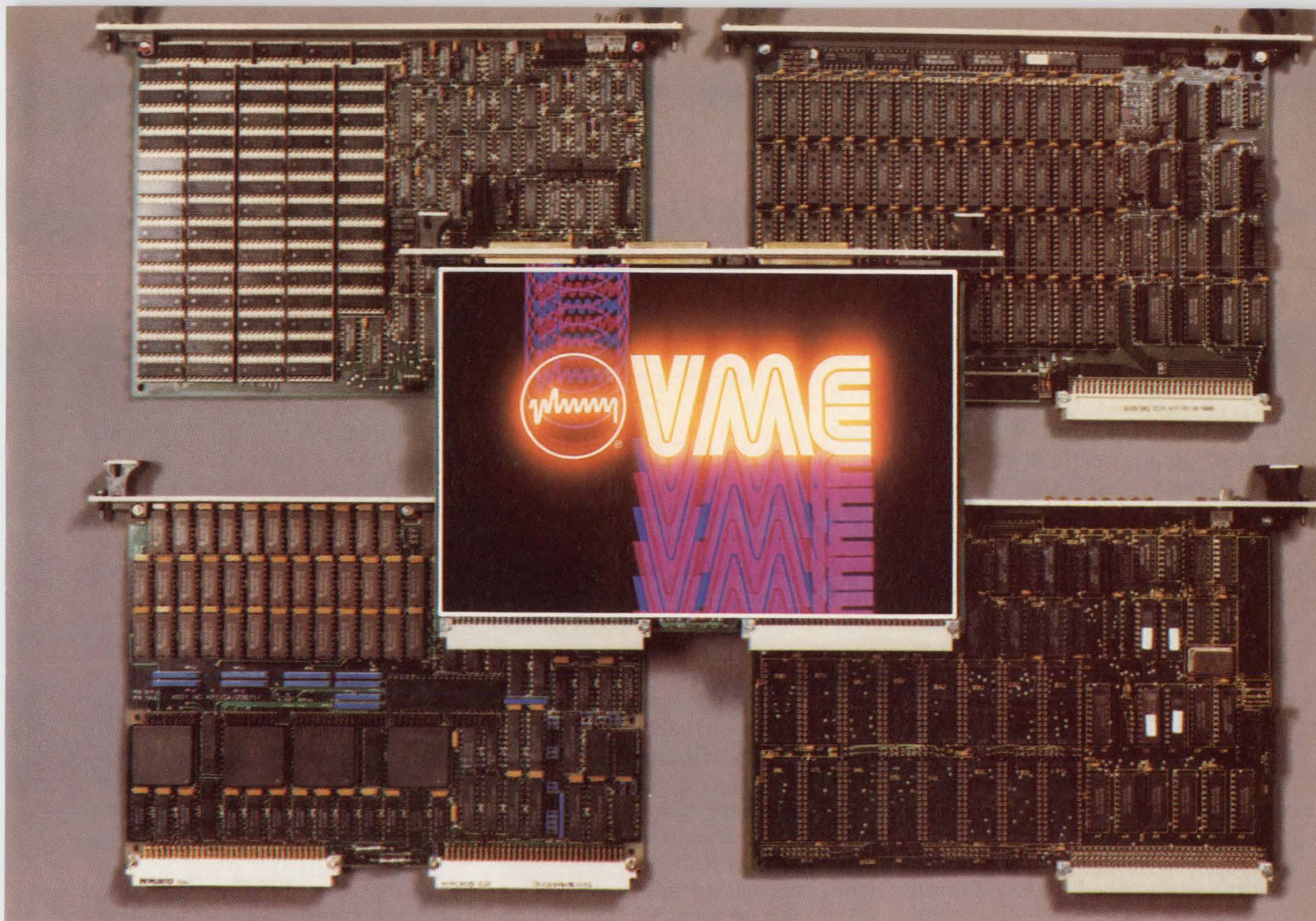
Nial's portable implementation, known as Q'Nial (developed at Queen's University in Kingston, Ontario) uses standard Unix files, an editor of the programmer's choice (including the Berkeley Unix VI), and Unix commands from within Q'Nial.

The Q'Nial interpreter is written in C and, as might be expected, parameterizes machine dependencies to allow simple host operating system interfaces. Originally developed on a Digital Equipment Corp VAX under the University of California at Berkeley Unix 4.1 BSD operating system, it will be ported to seven other systems. These range from the low end IBM PC to the large scale IBM 4341 system. Q'Nial interfaces with Unix for file management, text editing,

and command processing. Moreover, it is possible to call any Unix utility and have it create or modify a Q'Nial-accessible file. This open design means that Nial also works with software written in other languages. Its user can pick and choose the appropriate language and program for the problem at hand.

A binary object code license for the VAX version of Q'Nial ranges in price from \$1600 to \$8000, depending on the number of system terminals supported. Clearly, Q'Nial is not a casual purchase and this fact is recognized by an evaluation license being available at a lower cost. Prices range from \$400 to \$10,000 for other binary object code Nial versions that run on the Xenix, Unity, PC-DOS, Tops 20, and VM/CMS operating systems. Finally, \$25,000 buys the source code. **Nial Systems, Ltd**, 20 Hattcher St, Kingston, Ontario, Canada K7M 2L5.

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## Local area networks flourish while standards lag

Since VLSI devices and interfaces to support them have appeared, local area networks (LANs) have been multiplying like rabbits. The advantages of connecting relatively cheap workstations to expensive file servers and graphics peripherals are obvious, as is the need to connect to mainframes with superior computing power and database structures.

The problem, however, is that individual hardware and software vendors have gone haring off in separate directions. Each provides relatively easy interconnection between users of their particular products, but no simple way of transferring data or programs to other systems.

The resulting incompatibilities, like the chaos of floppy disk formats, are a disservice to the industry and the consumer. The real and pressing need, at all levels of the computer industry, is for a free flow of data and information among all levels of machines and users.

Purely commercial concerns—locking users into a particular hardware/software combination—will prove counterproductive in the long run. Telecommunication managers are already beginning to see that a 10-Mbyte/s Ethernet link, with expensive cables, interface hardware, and installation, is not much good if the machines at either end of the link find themselves unable to understand one another.

Creating a local network interface is a fairly straightforward technical problem that can usually be solved relatively quickly. Standards, on the other hand, are a political problem involving a large number of people and the reconciliation of conflicting points of view. Technology, as usual, is outrunning the political process.

To help solve such problems, DR Soft/Net, from Digital Research, Inc, implements the session and transport layers of the International Standards Organization (ISO) interconnect standard. It is basically a distributed file-serving mechanism that allows various machines running Digital Research

operating systems to share data files and use remote peripherals.

Its strength is in its modularity. Each function is a self-contained routine that other functions access via strictly defined interfaces. Data and service requests are passed between modules in a standard and easily understood way. Therefore, details are effectively hidden and design effort can be concentrated on the job at hand.

By putting all hardware interfaces into one module [Basic I/O System (BIOS)], file handling in another [Basic Disk Operating System (BDOS)], and a simplified user interface, [console command processor (CCP)] in another, Digital Research has created a flexible operating system. This system has made writing relatively inexpensive application programs feasible and quick.

Soft/Net continues the tradition of modularity, and was designed to make it easy for manufacturers to configure for particular hardware. The strictly logical component, Network Disk Operating System (NDOS) is provided in both 8-bit (8080/Z80) and 16-bit (8086) versions. Hardware connections Network I/O System (NIOS) are presently available for Ethernet and ARCnet, with documentation available for adapting to other transmission media.

File sharing, password protection, record and file locking, and remote peripheral use are all supported by Soft/Net. The first release of Soft/Net will be as part of Concurrent CP/M-80. This package will allow remote operations to go on in the background, while other programs are running.

Distributed processing, using the most widespread, commercially available desktop microcomputer, is the goal of an Ethernet-based Unix network recently announced by Plexus Computers, Inc (Santa Clara, Calif) and LanTech Systems. The network lets users of the IBM PC take advantage of Unix files, utilities, and multi-user capabilities.

LanTech's uNETix, a single-user Unix-compatible operating system for the PC, includes software interfaces to Plexus' Network Operating System (NOS). Together with a standard Ethernet interface board, the system turns the PC into a very intelligent distributed workstation with access to the resources of a super-microcomputer. It is available 90 days ARO for \$250 from LanTech.

The uNETix-Ethernet combination competes directly for board and disk space with IBM's recent PC/3270 (for communications) and PC/370 (for executing mainframe software in the PC) products. Neither system makes provision for communicating with the other—except, perhaps, by writing data to the PC disk, and rebooting with the other operating system to read it. This is, however, an inherently slow and clumsy process. In the absence of formal standards and user demands for compatibility, manufacturers will continue to create technical solutions that cause intercommunication problems.

Billing it as "The standard in network software," SofTech Microsystems has introduced Liaison, a networking implementation of the UCSD p-System. Liaison includes a limited multiprocessing operating system, a disk server to manage files for remote users, a print server, and a tool kit that will help develop the Liaison systems.

The system is presently available for the Apple IIe, IBM PC, TI Professional, and Corvus Concept computers. It communicates via the Corvus Omninet LAN. Implementations for other computer systems and other LANs are slated to become available soon. **Digital Research**, PO Box 579, Pacific Grove, CA 93050; **SofTech Microsystems**, 9294 Black Mountain Rd, San Diego, CA 92136; **LanTech**, 9635 Weddell Rd, Dallas, TX, 75243.

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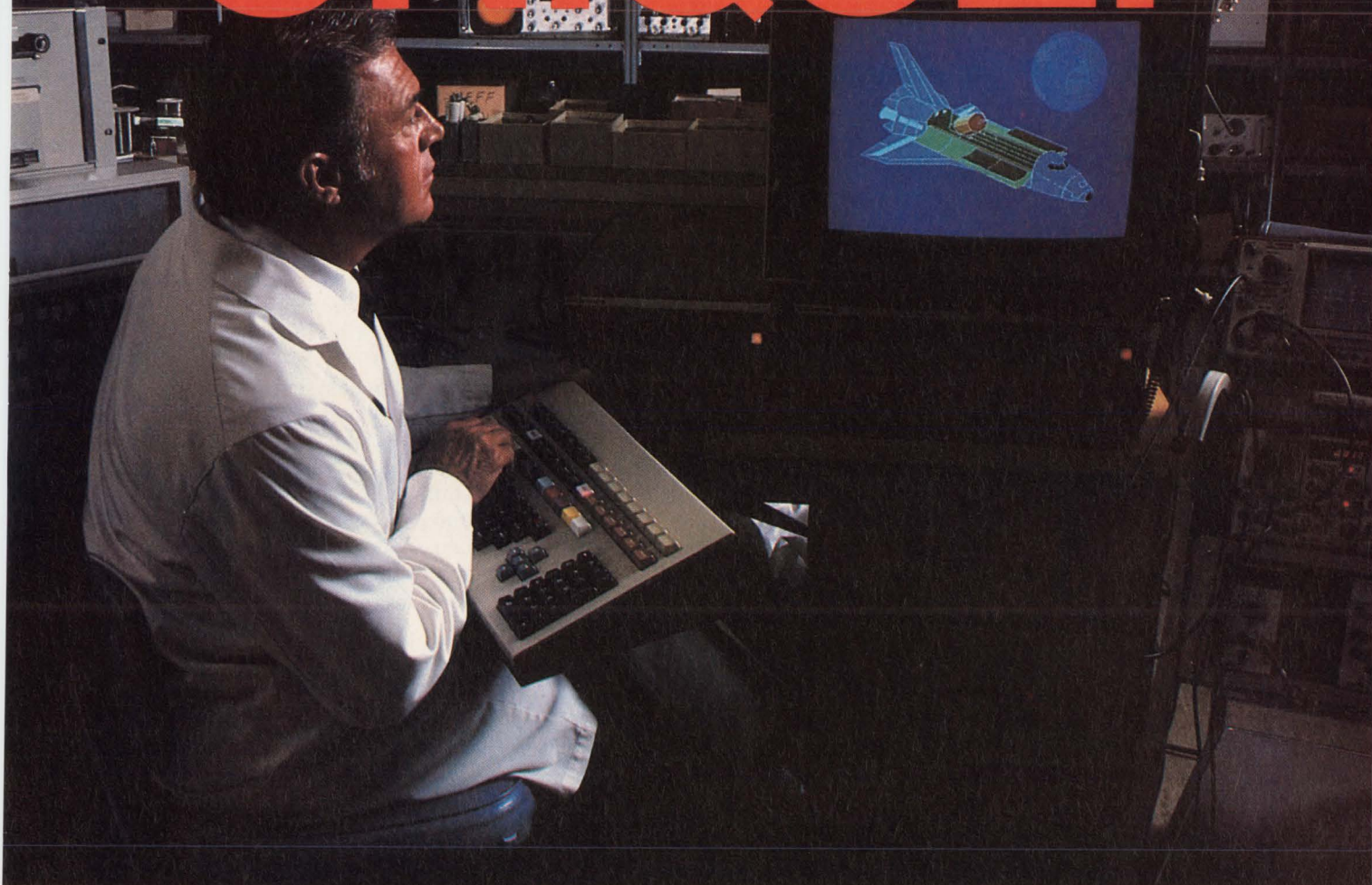


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## Structured analysis eases project specification



Techniques of structured analysis developed in data processing are used in a set of software tools tailored to meet the needs of software project specification. The tools are designed to define system and software problems at the beginning of the design cycle, before the code is written.

These Structured Analysis (SA) tools cover four main areas. These include graphics diagram editing, internal consistency checking, error

correcting, and formatting the analysis for output on printers or graphics peripherals.

To achieve system specification, a color graphics terminal displays data flow paths, processes that modify data, and data storage elements. Data flow diagrams are arranged in the computer hierarchically, enabling users to access each branch of the tree-like structure. At the bottom of the hierarchy is the mini-specification—a brief, English-like description of a data-modification process. Also included is a data dictionary that defines the items in the flow diagram and in the mini-specifications. The system's main function is to track activity and notify designers of any loose ends.

The SA graphics editing tools run on various Tektronix color graphics terminals. The system's internal consistency tools keep track of the processes and data paths that the user enters. These routines automatically check for errors in data flow diagrams, mini-specifications, and the data dictionary. They also search out inaccuracies in syntax, conflicts in the data flow hierarchy, and other problems. Currently, SA tools run on the Tektronix 8560 microcomputer development system and on the DEC VAX. Versions for VAX-Unix environments and for VAX-VMS are also under development. Hardcopy output compatible with Tektronix printers and plotters, and with the 4695 color copier, is available. **Tektronix, Inc.**, PO Box 1700, Beaverton, OR 97077. **Circle 337**

## Window worlds open to independent programmers

The open applications environment and the desktop metaphor are common concepts among the newer 16-bit operating system user interfaces. Notable among these are the Macintosh and Lisa by Apple Computer, the Windows system by Microsoft, and VisiOn by VisiCorp. The desktop metaphor uses windows, icons, menus, and a mouse to select actions and is obviously meant to make the systems appealing to those who are not totally familiar with computers. The open application environment, however, has two purposes: to allow the user to select and run applications from different software vendors, and to encourage independent software vendors (ISVs) to write applications for the window environments.

To this end, Apple Computer, Microsoft, and VisiCorp have come up with ISV programming aids and support. They have also specifically designed their operating environments to make it easy to adapt independently produced application programs to their computers. Such

ISV support has appeared in the form of "tool kits" for adapting to the world of windows and as porting aids for adapting existing programs to the new environment.

Porting existing software from other systems can be done in two ways. In some cases, programs can be recompiled and adapted to a subset of the window environment. In other cases, an application must run in a window which simply emulates a standard alphanumeric terminal. The programmer may later have the option of rewriting routines in the ported application to make it work more closely with the world of windows, but at least the existing software investment is preserved in the new environment.

The Apple Lisa system has a tool called QuickPort, which enables applications written in Basic-Plus, Cobol, or Pascal to be quickly moved to the Lisa Desktop. Such applications readily make use of complementing screen features. They will have their own menu, window, icon,

and stationery pad, as well as be able to utilize Lisa's scrolling and printing interfaces. Thus, although the Lisa uses an object-oriented programming approach, nonobject-oriented programs can be written for it. These can interact with the user in a Lisa-like manner.

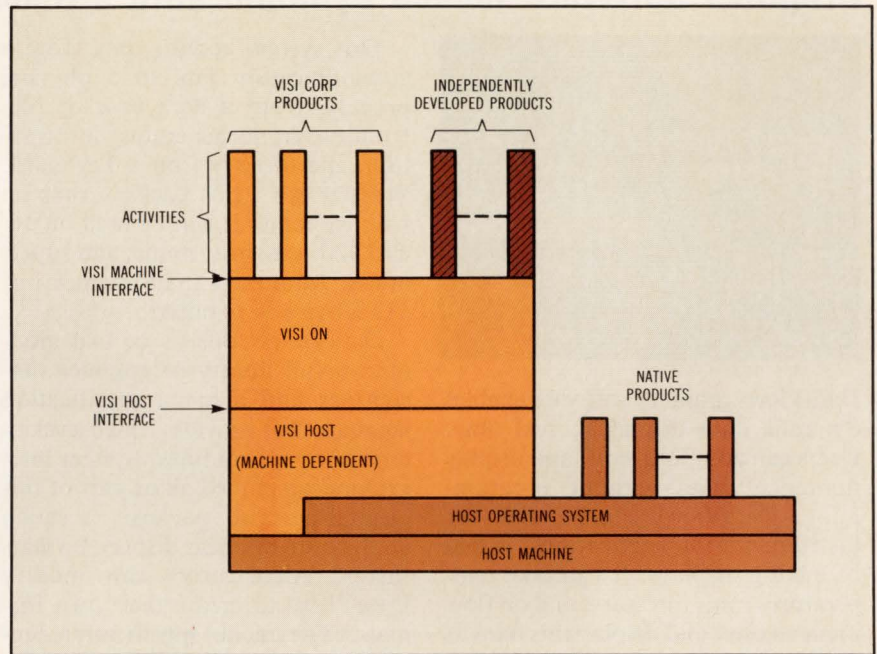
One main difference exists between the Lisa world and the window systems offered by VisiCorp and Microsoft. Lisa is a hardware environment with its own operating system, while the latter two represent extensions to existing operating systems. Microsoft's Windows is an extension of its own MS-DOS operating system. VisiCorp's VisiOn interfaces to other 16-bit operating systems via a machine-dependent VisiHost/operating system interface.

Microsoft does provide the ability for a window to emulate a VT-52 type terminal for straight alphanumeric I/O. But, applications that write directly to hardware, bypassing MS-DOS, will not run in a window. Here, the portability issue involves

porting the program to the MS-DOS environment rather than to a hardware system (in contrast to Lisa). Unix-only programs would not run under MS-DOS. On the other hand, Microsoft provides language bindings to six languages that give them access to the standard Windows features when compiled under MS-DOS.

In all three approaches, applications can take full advantage of user-interface features when they are written specifically for that environment; all three companies provide tools for the ISV to do that. Each has a somewhat different focus, however. Apple is primarily a hardware manufacturer with its own operating system. Microsoft has concentrated on the MS-DOS running on a wide variety of machines. VisiCorp has focused on consistent application software that runs in a number of operating systems. The three companies are aware that they cannot service the full demand for applications, hence the importance of the ISV.

One effect of open applications may be a standard for the human interface. By not withholding interface tools from ISVs, major companies are not only encouraging vendors to write software for their systems, but



The machine-dependent interface, VisiHost, connects the VisiOn environment to the host operating system. Applications written by VisiCorp, as well as those by ISVs, run consistently in the VisiOn world sharing user interface and data.

are also encouraging the use of ready-made tools. These tools will give users a familiar way to interact with the new applications. **Apple Computer**, 20525 Mariani Ave, Cupertino, CA 95014; **Microsoft**, 10700 Northup

Way, Bellevue, WA 98004, **VisiCorp**, 2895 Zanker Rd, San Jose, CA 95134.

**Apple Computer**—Circle 338

**Microsoft**—Circle 339

**VisiCorp**—Circle 340

## AI language programs expert systems under VAX/VMS

Expert system design requires the use of an artificial intelligence language. OPS5, based on Carnegie-Mellon University's original AI language, takes advantage of the VAX/VMS system architecture by offering additional capabilities.

To let the language be fully involved in the expert system design process, it is separated into individual parts. A changing model represents expert knowledge using rules in an if...then format. This dynamic "knowledge base" is also used to build and maintain the model. The third part of the AI language, the inference engine, has the responsibility

of deciding which rules to execute for any given situation. Unlike AI languages that are Lisp based, OPS5 requires no garbage collection and will execute in real time. It is reimplemented in native mode on the VAX, yielding a program running 5 to 20 times faster than Lisp machines.

OPS5 applications can call and be called by software in any language supporting the VAX calling standard. For example, a data collection routine written in another language can be called from OPS5, and the information incorporated into the AI model.

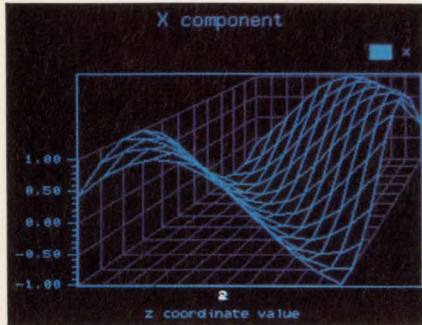
Targeted for companies with in-house AI departments and program-

mers with AI experience, the forward-chaining, rule-based language handles large production systems. Forward-chaining combines inputs from previous rule-based decisions and forms another version of the present model. Two different conflict resolution strategies are provided, so users can choose one that best meets their application.

Available through DEC's External Application Software Library, approximate price is \$5000, with right to copy licenses at \$3000. **Digital Equipment Corp**, 10 Main St, Maynard, MA 01754.

Circle 341

## Graphics software makes dynamic data stream display possible



DataViews graphics software enables dynamic data display in real time. Users can compose, edit, and display numerical data without programming. DataViews can be used for instrumentation applications, in lieu of analog displays. It can take temperature, rpms, pressure, and oil flow in an engine, and display this data as a simulated instrument panel on a color monitor.

This system accepts data from a communication link to a physical process, from a data base or file, from programs generating information, and directly from a keyboard. Written in C, this package runs on Unix systems. It can be used on 16- and 32-bit micros, minis, and super-minis. Minimum main memory of 512 Kbytes is required.

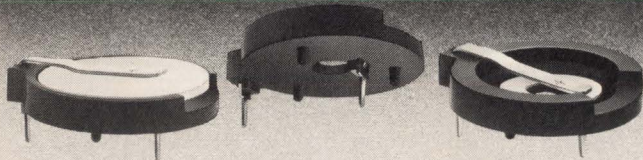
DataViews consists of two modules: a full library of graphics subroutines and a menu specification language that provides a high level interface to subroutines. System integrators can embed all or part of this general-purpose package, creating application-specific display formats faster. Also, users can modify DataViews to create their own formats. The menu specification language module allows alteration of existing menus.

Subroutines offer over 40 display formats including line graphs, dials, bar charts, surface plots, and flow fields. Multiple screens can be constructed with a variety of viewports and formats. In an aerospace application, for example, windows show each dimension of net velocity as data is generated on a display of simulated vector fields. (A network of supercomputers, minis, and color graphics workstations was used in the 3-D simulation pictured here.)

Instrumentation, automatic test equipment and process controls, as well as engineering, science, and simulation are among DataViews uses. In quantities over 25, the product is priced at \$1000 for a one- or two-user system. **Visual Intelligence Corp.**, 160 Old Farm Rd, Amherst, MA 01002.

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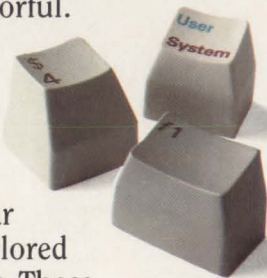
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# COMPONENT ADVANCES KEEP STEP WITH SYSTEM DESIGNS

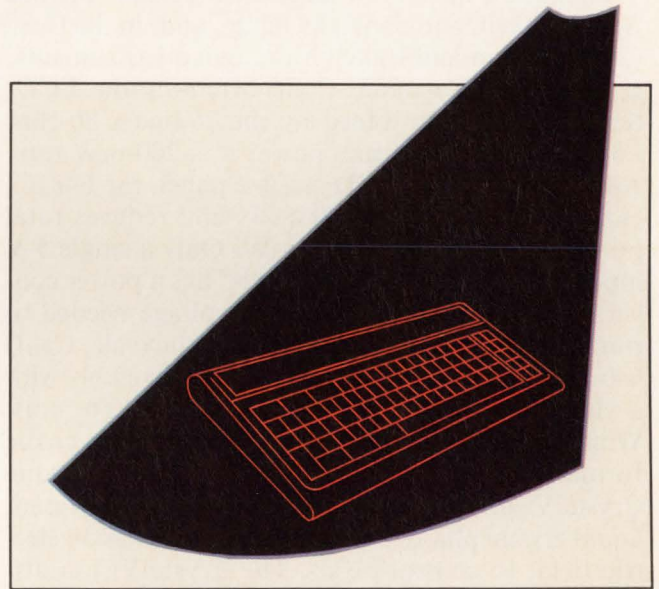
The screen world gets flatter and ergonomics gain momentum as system elements reflect the drive to portability and user friendliness.

by Malinda Banash, Senior Associate Editor  
and Jack Vaughan, Associate Editor

Smaller system elements, previously taken for granted, are exhibiting the same levels of technological advancement that larger systems are achieving. As developments in optic electronics and ICs trickle down, components such as displays, power supplies, and input devices are taking on a luster once reserved for their bigger brothers.

Much of this year's display activity revolved around flat-screen technology. Although it is unlikely that flat screens will displace the CRT in high resolution applications, they are posed to make serious low end inroads. Nurtured in specialized industrial and military applications, flat screens become more prevalent as the notebook computer format evolves into the 25-line, briefcase portable. The appearance of flat screens on portables from Grid, Hewlett-Packard, and Data General has signaled designers that replacements are here for the CRT that has steadfastly held out against solid state alternatives. Active matrix LCDs from Panelvision, plasma displays from IBM and Plasma Graphics, and electroluminescent screens from Sharp and the Finnish Lojha Corp have also garnered special attention.

The 1984 debut of Hewlett-Packard's (Cupertino, Calif) portable—the HP 110—was a harbinger of



more capable and smaller computers. This machine features a 16-line x 80-char LCD in a package weighing less than 9 lb (4.08 kg). Contrast is adjustable via keyboard commands and the screen can tilt almost 180 degrees to adjust to light conditions.

In September, Data General (Westboro, Mass) greatly upped the line and character count stakes with its Data General/One personal system. This unit sports the industry's first full-size, 25-line LCD screen. It also claims 640- x 256-pixel resolution, compared to the HP 110's 480 x 128 presentation. The One's bit-mapped display supports characters



The electroluminescent flat-panel screen on the Grid Compass has shown the remarkable clarity EL technology can achieve. Available this year in a 512-Kbyte RAM version, the Compass features a readout window from Panelgraphic that enhances the display with a neutral gray filter that makes character resolution more vivid.

in a 2:1 ratio for good legibility. This display also generates various shades of gray, allowing use with color graphics software packages.

### The bigger picture

Important makers of large LCD screens include Seiko, Sharp, and Sanyo in Japan, and, in the U.S., CrystalVision and Panelvision. Seiko Instruments, U.S.A., Inc. (Torrance, Calif) offers various LCDs that were recently joined by the 25-line x 80-char F641D, which consumes power at a 200-mW rate. Another new Seiko LCD graphic panel, the F481C, can display 16 lines of 80 chars and reduces total power consumption to 180 mW. Only a single 5-V input is necessary, since the F481C has a power conversion circuit that supplies the voltage needed to run the panel. CrystalVision Inc's (Sunnyvale, Calif) 640- x 250-pixel unit is a panel/driver assembly with a viewing area of 5 x 6.4 in. (127 x 162.56 mm). While the large Japanese LCDs use a twisted nematic format (dependent on two polarizers), the unique CrystalVision product manipulates several different liquid crystal phases and uses heat, as well as an electric field, to control pixels. The CrystalVision display boasts an extraordinary contrast of about 10:1. Power needs, however, about match those of CRTs.

Panelvision Corp (Pittsburgh, Pa) approaches the contrast problem with active matrix addressing. In this system, thin-film transistors at each pixel act as switches. Improved clarity and a better viewing angle result. Dubbed the MiniGraphic, the Panelvision display has an 8:1 reflective contrast ratio.

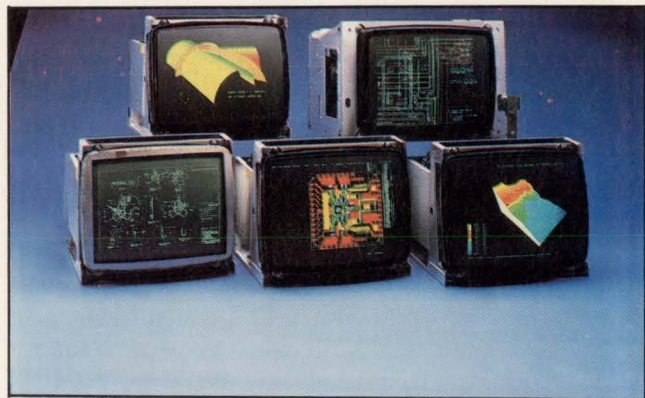
The early dominance of the LCD is being challenged by electroluminescent (EL) technology, notably represented by Sharp Electronics Corp (Paramus, NJ) and Lohja Corp (Lohja, Finland). Sharp's EL screen appears in the Compass portable

from Grid Systems (Mountain View, Calif). The 25-line x 80-char display on the Compass uses a neutral gray, 0.030 polycarbonate display window from Panelgraphic Corp of West Caldwell, NJ. The neutral gray filter provides contrast enhancement, so that the amber pixels stand out more vividly. The display produces a 240 x 320 distortion-free image. Refresh rate is 66 Hz.

From Finlux, Inc (a subsidiary of Lohja) comes the MDM 512.256.11 panel. It has 512 x 256 resolution and measures 140 x 260 x 9.5 mm. This 25-line x 80-char unit includes a monolithic 64-channel driver from Sunnyvale's Supertex, Inc and features a proprietary atomic layer epitaxy thin-film process. There are still only a few players using the EL approach, which relies on the activation of phosphors. EL allows manufacture of lightweight units, its advocates claim, with extremely sharp images. However, it does make greater demands for power. The Grid machine's power requirement hits 60 W. Next year will see significant progress in EL technology, and perhaps price cuts.

Gas plasma flat panels from IBM and Plasma Graphics (Warren, NJ) gained attention in 1984. The ac-dc plasma hybrid from Plasma Graphics marked a high performance 480- x 250-pixel device with the 25-row x 80-col alphanumeric format that is quickly becoming *de rigueur*. Easily viewable, even under bright lights, it uses 12.5 W in display mode and 20.5 W in data entry mode.

Flat-panel technology is not likely to stagnate at the monochrome application level. Next year may mark the introduction of an eight-color LCD from Seiko. Reports indicate that unit will have 64- x 160-pixel resolution. In the realm of EL color, Planar Systems, Inc (Beaverton, Ore) hopes to market multicolor EL panels in the future. Planar recently demonstrated strontium sulphide-based



GMA raster displays from Tektronix incorporate graphics features including 60-Hz noninterlaced refresh, dynamic controlled convergence correction, and digitally controlled dynamic focusing. Addressable resolution of the GMA201 model is rated at 2048 x 1536 pixels.



High voltage ICs were announced this year by GE. The firm has developed a proprietary process for fabricating monolithic junction-isolated chips rated at up to 500 V. Power supplies represent a prime application area.

thin-film units with brightness representing a two orders of magnitude increase over previous thin-film, blue EL phosphors.

### Beyond 1024 x 1024

Still the domain of the CRT, high resolution can make major strides in the coming year. Though graphics software and controllers seem to be driving high resolution display development, there are rumblings at the 1024- x 1024-pixel resolution limit. Computer aided design station vendors, such as Megatek Corp, Raster Technologies, Inc, and Lexidata Corp, have incorporated assorted techniques and bypassed that limit. For example, Lexidata's (Billerica, Mass) LEX 90/35 model 2 dual-resolution graphics system allows simultaneous display of both a 640- x 512-pixel x 8 deep image and a 1280- x 1024-pixel x 4 deep overlay on one screen.

Just on the horizon, the GMA201 monochrome monitor from Tektronix (Beaverton, Ore) melds high image quality with low power consumption. This intriguing unit features an addressable resolution of 2048 x 1536 pixels, and it combats flicker with a 60-Hz noninterlaced refresh rate. A low capacitance CRT gun diminishes power consumption requirements. Also near release is the GMA303 raster display. It has 1280- x 1024-pixel resolution with 60-Hz noninterlaced refresh rates.

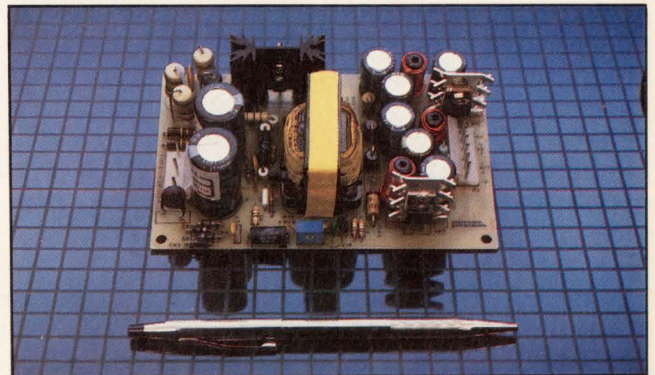
Other monitors are making new waves. RCA Laboratories' researchers are working on a power-saving deflection yoke that mounts inside the vacuum glass envelope. Toshiba Corp has described a color display that achieves high performance luminance.

And, display manufacturers like Hitachi America Ltd and Saber Technology Corp offer here-and-now RGB color displays with 1280 x 1024 resolution. In the coming year, we can perhaps expect the high resolution CRT log-jam to break, thereby provoking an interest similar to that received by flat screens in 1984.

### The scepter of power

Portability, the concept behind most flat-panel developments, is at work in the power sector also. Small power ICs stand foremost when considering this past year's power developments, but they do more than miniaturize. Power ICs are likely to redefine component and system design. (See "Power and Logic Devices Are Merging on the Same Chip," *Computer Design*, Aug 1984, p 29.) These devices are finding niches in power supplies, disk drives, and in flat-panel display drivers such as the Supertex chip used in the Finlux display. An intelligent power chip, such as the HV03/04 set from Supertex, cuts system complexity and reduces operating temperatures while making simpler system power supplies possible.

New power ICs handle greater control voltages while exhibiting low power dissipation. "Smart-power" chips from Motorola Semiconductor Products, Inc (Phoenix, Ariz), as well as power ICs from Unitrode Corp, Siliconix, Inc, General Electric Corp, and others, represent an ongoing technological breakthrough. For example, high voltage ICs under development at GE (Albany, NY) produce 500-V isolation. They merge the functions now performed by discrete devices, logic circuitry, and relays. Designed in biMOS, the devices can deliver up to a 2-A peak, and drive bipolar and MOSFET power devices. GE anticipates a variety of uses (eg, plasma display drivers and switching power supplies). Motorola's parts, with breakdown output power surpassing 100 V, can dissipate 250 W and control switched loads exceeding 2 kW.



Triple output 30-W power supplies from Power General are marked by an ultraminiature form factor. These compact units operate with low output noise and feature 4000-Vac I/O isolation.



Addressing the problems of reliability in elastomer switching technology, the Ergokey series of keyboards from Advanced Input Devices tests at over 100 million cycles. This improvement may bring elastomer to the forefront of switching technologies for keyboards.

As with so many components, the power supply is getting smaller. Sola, Boschert, Inc, Power Products, and Power General are just a few of the firms offering standard power supplies for small systems. A mighty mite, the 3030-1 from Power General (Canton, Mass) is a 30-W, triple output switching power supply. Its board is only 3 x 5 x 1.8 in. (7.62 x 127 x 45.7 mm). It weighs 0.5 lb (0.226 kg). Units in this ultraminiature supply series feature 4000-Vac I/O isolation, as well as user-selectable voltage ranges of 90 to 130 Vac and 180 to 250 Vac. Sola (Elk Grove, Ill) now offers a miniature series that includes 15-, 30-, and 50-W models with 5-Vdc single output, plus 40-, 50-, 65-, and 90-W models in triple and quad outputs covering standard output combinations of -12, -5, 5, and 12 Vdc.

### Ergonomic factors drive the keyboard

Ergonomics and human factors engineering hold the interest of designers, perhaps even more than advances in technology. This becomes particularly apparent in input devices—the human to machine interface. Successful efforts include Hewlett-Packard's HP 150 personal computer with its touch screen and Apple's use of the mouse with the Macintosh. Not quite as successful was the IBM PCjr keyboard. It not only wanted to be cordless, but to supply friendliness through overlays for application programs. The most recent attempt to help the PCjr keyboard gives it a more familiar key shape but keeps the sometimes unreliable infrared technology.

This concern for user friendliness and ergonomic standards is perhaps the most significant trend in today's input device technology. Keyboards are seen

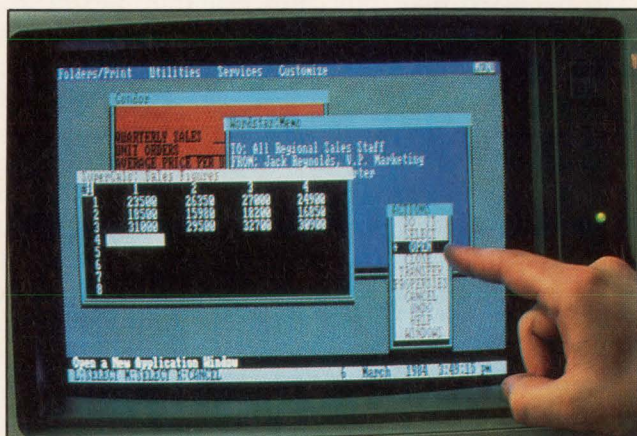
as the primary input devices with mice, touch screens, trackballs—among others—acting as enhancements to the keyboard. Some feel that as voice technology matures it may replace the keyboard.

Generally, input and input devices can be placed in three classes: conceptual, indirect, and direct. The conceptual approach encompasses the traditional keyboard. With the indirect method, the user works with a model of the screen; for instance, with a mouse and keypad. Direct input devices allow the user to actually work with the display itself. Touch screens are examples of this approach. Often, direct and indirect devices lend themselves to user friendliness as menu-driven systems. The path that input devices are taking combines the primary input device (keyboards) with devices that are better adapted to easily move and manage data.

### Designed for user comfort

With companies firmly entrenched in their specific technologies, the future of keyboards lies in the ergonomics of the design. While the traditional engineering factors of cost and reliability are still important, the keyboard designer tends to pay more attention to human factors. Deutsches Institute für Normung (DIN) standards call for a 30-mm limit on keyboard height from tabletop to home row and specify several other factors including slant spacing and even a tactile feel. More and more users are asking for tactile feel and manufacturers are even using electronically controlled volume for those that prefer a silent touch.

Various keyboard switching technologies are available and range from mechanical to capacitive to elastomer. Although the oldest switching technology—mechanical switching—has many critics, it has many followers as well. Hi Tek's

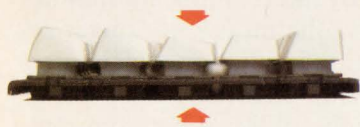


The Point-1 Color Kit from MicroTouch brings touch technology to both IBM and DEC systems. Used in this case with window-oriented software, the kit provides an alternative input device that incorporates user-friendly features.

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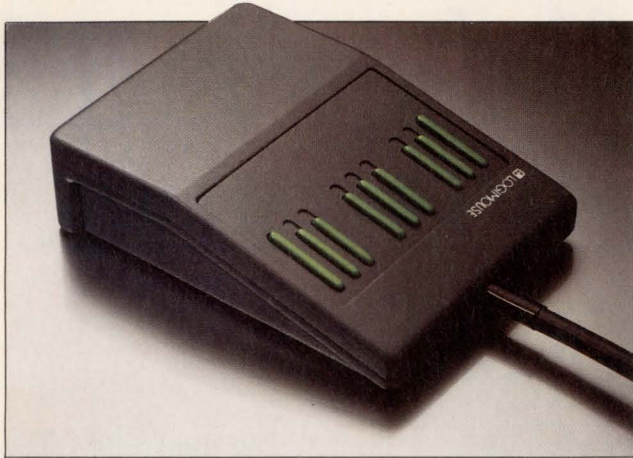
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The Logimouse from Logitech incorporates opto mechanical technology. The unit can accommodate serial or parallel interfaces and provides a choice of two or three button designs.

(Garden Grove, Calif) dominant technology is full travel mechanical switching. The company's PC 83 and PC 84 keyboard designs attempt to eliminate many mechanical switching criticisms. Traditionally, this technology could not provide for N-key rollover that comes standard with the popular capacitive technologies. But, by using diodes under each key, mechanical devices can now offer the choice of N-key or multikey rollover.

Reliability was another problem for mechanical switching devices. Previously they were good for 20 million (or less) cycles. Now, testing shows 100 million cycles—a value that rivals the reliable capacitive technologies. Mechanicals compete even in the cost arena with production improvements.

Hi Tek employs a passive approach that lets contacts relax and automatically move toward each other when the keyswitch is depressed. This helps alleviate the bounce problem associated with mechanical switching keyboards and customary active contacts. Encoded keyboards can also efficiently control bounce by using advanced microprocessor technology.

Another technology that has made advances is the elastomer keyswitch. In the past, elastomer switches had relatively short life spans that limited their popularity. But the Ergokey Series from Advanced Input Devices (Coeur d'Alene, Idaho) employs a long life switch that has been tested at 100 million cycles. By providing the advantages of cost-effectiveness and easily incorporated ergonomics, such as tactile feel, elastomer promises to be a dominant keyboard technology.

The mouse is probably the most popular keyboard enhancement, slowly becoming a legitimate part of a system's design. But, application software for these devices is often unavailable, especially for optical

mice. They can sense small rotations, a useful ability that is not often incorporated into applications software. Mice also use mechanical technology. This approach provides higher resolution and, unlike the optical mouse which requires a keypad, it can work on any surface.

#### Mouse without a tail

Until recently, these were the only technologies used in mice. Now Logitech, Inc (Redwood City, Calif) has implemented an infrared, cordless design for Metaphor Computer Systems information retrieval and analysis system. This design solves several problems. Lighter batteries answer power-up problems. The unit becomes lighter and can be left on longer without the battery dying.

Another problem, similar to the one that plagued the PCjr keyboard, is that the infrared keyboard has to line up with the system unit for valid command entry. Logitech gives the mouse a large angle in which to work, as well as interference protection from neighboring mice. By intertwining ergonomics with infrared technology, the mouse no longer requires the cables that emitted radiation which interfered with the system. While the widespread use of infrared mice depends on the ability of both the computer and the mouse to understand what the other is doing, this technology offers great potential as more and more of the design problems are met.

As with keyboards, human factors are important in other input devices. Direct input methods such as touch screens have become increasingly popular—notably demonstrated by the HP 150 personal computer. The 150 uses LEDs that run across the bottom and right, while the detectors run along the top and left. This results in beams that cross in a 40 x 23 matrix. The beams are far enough from the screen, so actually touching the screen is not required. The HP touch screen offers a comfortable reaching distance. Moreover, the touch screen is ideal in applications where the user is not familiar with the system or does not use it constantly.

It is not necessary to have an HP 150 to use a touch screen. Other companies offer packages that can transform a regular screen into a touch activated one. MicroTouch Systems, Inc (Woburn, Mass) provides touch screen kits for both the IBM PC and DEC personal computers and terminals. The Point-1 Color Kit includes a 13-in. diagonal touch screen, an intelligent controller, and an RS-232-C serial interface. It is supported by a complete set of software development tools and is fully programmable. In addition, the Point-1 Color Kit offers a resolution of 1024 x 1024 touch points, and software that averages the areas of contact makes moving even a single letter possible.



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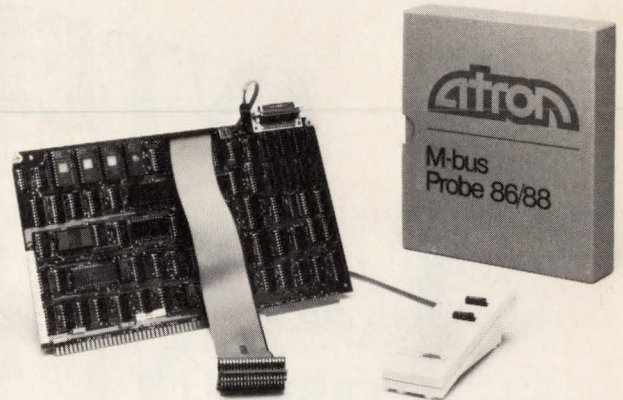
Breakpoint encountered at 0624:01C2:..MEMORY_TESTER#100
OP
ADDR CODE OPERAND(S)
-----
0637B JMP $+0082 :..MEMORY_TESTER#99
..MEMORY_TESTER#99:
063FD ADD WORD PTR [F5B2],0040 :..MEMADDR+0002
19202 READ - DS - 00
19203 READ - DS - 10
19202 WRITE - DS - 40
19203 WRITE - DS - 10
* LOCAL VARIABLES ON THE STACK
BUFFER = 09C5:0000 BUFFERLENGTH = 001F
BUFFER CONTENTS
09C5:0000 54 45 53 54 4D 45 4D 4F 52 59 20 50 4F 49 4E 54 *TESTMEMORY POINT*
09C5:0010 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 00 *.....*
AX=00A5 CS=0624 SS=09C5 DS=09C5 ES=1000
BX=03FF IP=01C2 SP=F5B0 SI=F5B0 DI=09C5
CX=0006 BP=F5B0
DX=0000 FL=00 00 11 T0 S0 Z0 A0 P0 C0

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Assemble BP Byte Compare Console Delete DMA Echo EMacro Eval Fill Flag
Go IF INit Interrupt List Load LOGic LOOP Macro MEmu MODule MOVe MORE
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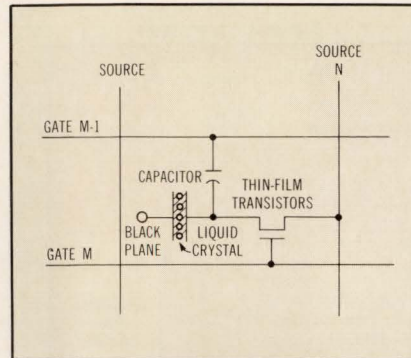
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## Flat panels approach monochrome CRT specifications

A flat-panel display incorporating thin-film transistors (TFTs) with a liquid crystal medium has been announced by Panelvision Corp. Although Panelvision designers chose liquid crystal media, the TFT active matrix approach lends itself to all forms of display media currently used.

The real breakthrough of active matrix technology lies not so much in the display material as in its ability to address and drive a large number of display elements. With LCDs, each pixel can operate at 100 percent duty cycle, thus achieving a very sharp contrast and viewing angle in comparison to time division multiplexed LCDs. The TFT approach also lends itself to eventual incorporation of gray scales.

The unit announced by Panelvision features an active area of about 4 x 3 in. (10 x 8 cm) and displays 512 chars using a 5- x 7-pixel matrix. The pixels total 24,576. Panelvision is also



**The actual transistor takes up a small part of the pixel area in this one-pixel elementary cell for the active matrix display. Vacuum-deposited on glass, the cell can be replicated according to size limits of the vacuum equipment.**

currently engineering an 80-char, 25-line display that will be a 400-line resolution bit-mapped matrix. As the displayed information approaches that of a standard 24- x 80-char CRT, the number of pixels that

must be directly addressed approaches 250,000.

Panelvision has solved this by creating what is, in effect, a 5¼- x 4-in. (13- x 10-cm) IC. The TFTs are vacuum-deposited on a glass substrate that takes up an arbitrarily large area dependent only upon the size of the vacuum equipment. The LCD material is injected and the panel sealed. The same kind of TFTs can be used to produce row and column drivers and shift registers, thus integrating peripheral circuitry onto the display panel. This reduces the number of connections needed for external circuitry to about 10.

The entire matrix is analogous to a large, fully decoded RAM. Since the full duty cycle is available at each pixel, there is room to introduce levels of gray scale in later products. **Panelvision Corp.**, 265 Kappa Dr, Pittsburgh, PA 15238.

Circle 343

## Technologies vie to displace CRT in terminals

The IBM 581 Plasma Display claims a 1000-char capacity. Its 960 vertical lines and 768 horizontal lines at a 71.4-line/in. resolution yield a pixel count of 74,000 that can be drawn on an approximately 1 ft<sup>2</sup> viewing area of the panel. It takes 200 ms to fill a screen. To achieve this large pixel count, IBM researchers minimized the panel process defect densities by using projection printing and low temperature glass materials. They also found an effective way to repair open lines.

On the 581, the vertical lines are brought out half on the top and half on the bottom of the panel as even and odd lines. The horizontal lines are handled in a similar fashion on the right and left sides of the panel. This is done to reduce the density of the interconnections to the panel and affects the architecture of the interface. The 581 interface consists of 10

data-addressing lines, five functions, and two lines with signals sent to the using system.

IBM does not expect the plasma display to dislodge the CRT in all computer applications since the production costs of ac plasma panels are not competitive with those of CRTs. But, for generating flicker-free, high quality images on a flat panel, the ac plasma panel can be a practical alternative.

While liquid crystal flat panels have usually been restricted to small applications, CrystalVision Inc has recently developed an LCD that has 250 rows x 640 cols, and can typically be used in a 25-line x 80-char format. Although the current writing speed is roughly 2000 chars/s, special cases where the information is repetitive (eg, displaying the grid for a graph or erasing the screen), can approach a writing speed of 1000 chars/s.

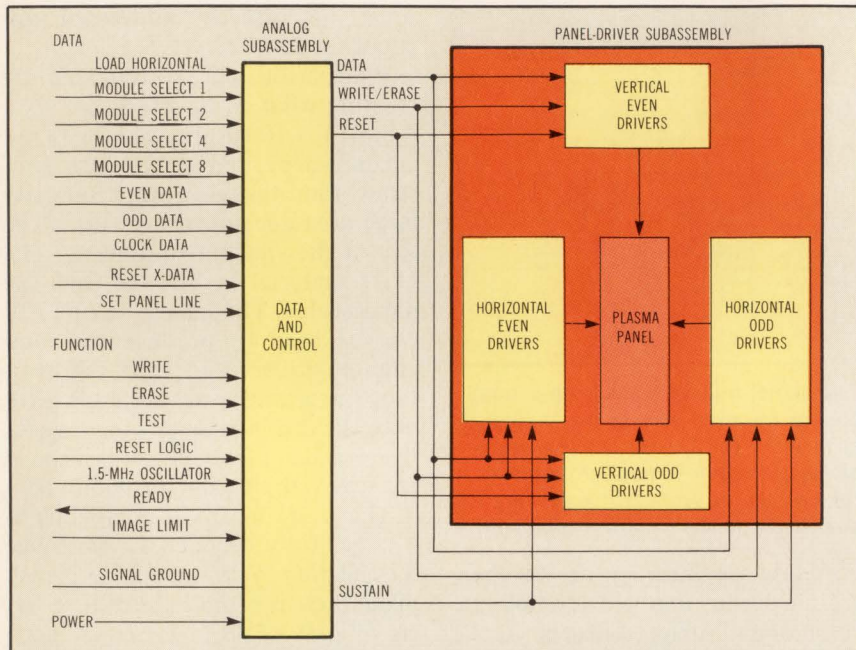
Basically, the display consists of two parallel glass plates separated by approximately 165 μm, which contains a smectic liquid crystal and dye mixture. The front glass has transparent indium tin oxide column traces running vertically. The back glass has textured, mirror-finish metallic row heating traces running horizontally. A pixel is created at the intersection of each of the 640 cols and 250 rows, for a total of 16,000 pixels. A wide border column on each side and six border rows add another 4352 controllable pixels, allowing the user to dynamically control the border area.

Low level display functions are performed on the panel driver board microprocessor. These functions include general display control and timing, ac waveform generation, pixel row addressing, and thermal

*(continued on page 252)*

## Technologies vie

(continued from page 251)



The 10,000-char capacity of IBM's ac plasma panel display implements a subassembly to accommodate all computer interfaces. Ten data-address lines are complemented with five function lines that allow a maximum of 960 pixels in the X direction and 16 pixels in the Y direction at any one time.

management. For users who may not want to generate the serial data stream required by the low level control board, CrystalVision has designed an optional high level control board that accepts both ASCII characters and graphics bit patterns. Users can communicate via a serial or a parallel port.

In alphanumeric mode, the high level controller accepts standard ASCII codes from the user and performs font generation. In graphics mode, the high level control board sends received data to the display module without performing font generation. In this mode, users have control over every pixel in the display by specifying the bit pattern and the row address where writing is desired. Rows can also be written in any sequence. **IBM**, Neighborhood Rd, Kingston, NY 12401; **CrystalVision Inc**, 1313 Geneva Ave, Sunnyvale, CA 94089.

IBM—Circle 344

CrystalVision—Circle 345

## Hybrid plasma display simplifies driver electronics, cuts cost

Using patented self-scan with memory, the model 120 flat panel combines the inherent memory of ac plasma with the powerful addressing of dc plasma to reduce expensive driver electronics. The result is a full-page display, with 480- x 250-pixel graphics and 80-col x 25-row alphanumeric, that promises to compete price-wise with high quality CRT monitors. Moreover, because the display subsystem is unaffected by magnetic fields and emits no X rays, it can function in industrial environments as well as in office and transportable systems.

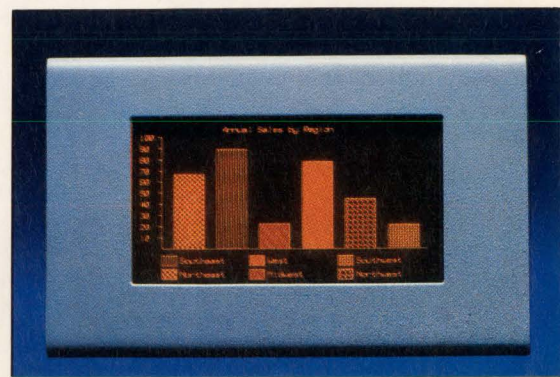
The all-points addressable, 120,000-pixel display uses only 40 drivers and 137 driver-to-panel interconnections. This compares with 730 X-Y drivers and 730 driver-to-panel interconnections for the same resolution on typical ac plasma displays. Instead of using a driver cir-

cuit for each row and each column of pixels as ac plasma panels do, the hybrid display incorporates a dc scan section for X-axis addressing and an ac memory layer that multiplexes Y-axis drivers.

In addition, the 67-pixel/in., 7.2- x 3.75-in. (18.3- x 9.5-cm) display area can be seen from a 150-degree viewing angle.

An inherent display storage function eliminates the need for refresh. Once data is entered, the subsystem maintains the image as long as power and an input clock signal are applied to the drive electronics.

Otherwise, only the entry of new data will alter the display. Eliminating display refresh removes the previous panel size constraints as well as any flicker effects.



Overall dimensions of the 3-lb (1-kg) flat panel, including built-in driver board with all subsystem electronics, are 11.2 x 6.52 x 1.4 in. (28.4 x 16.56 x 3.6 cm). The display has a standard TTL-compatible, 8-bit parallel data bus interface to computer systems. **Plasma Graphics Corp**, PO Box 4093, Warren, NJ 07060.

Circle 346

## Power supply handles parallel operation

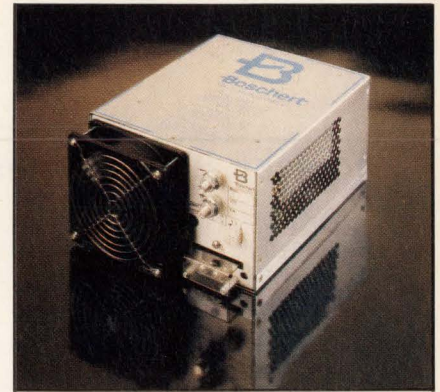
A single output switcher, the 1000-W HL1000 fits the standard 5- x 8- x 11-in. format. A nine-pin connector provides outputs for advance thermal warning, power fail detect, remote sense output status, supply paralleling, and remote inhibit.

Supplies are constructed from ac input, output, and control modules. The input module includes an rfi filter, ac line rectifier and filter, 24-V housekeeping supply, power fail detect, and drive and power switching circuitry. The output module contains the power output transformer, rectifier, and filter. The control module is a 4.25- x 4.5-in. PC card containing control and supervisory circuitry together with an external control interface.

When the supply operates in parallel, the difference between output currents of parallel units is less than

10 percent of the full load value. In a redundant configuration, parallel outputs deviate less than 2 percent as a result of inhibit, shutdown, or failure of a parallel supply. Some control features pertain to the parallel supply configuration. The parallel signal controls current sharing in the main modules. Current sharing is insensitive to output voltages, resulting in a value to within 10 percent of the total current. A slave triggering signal ensures simultaneous triggering of all main crowbar protection circuits when one is activated.

The current mode features a built-in voltage proportional to the current. Placing the units in parallel results in an average voltage. Current mode switching reduces the need to compensate for changes in load, lessening the supply's dependence on the input voltage.

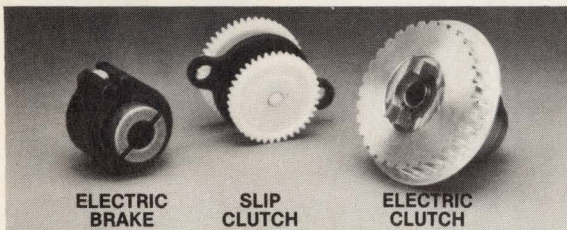


Both the current mode and the proportional drive reduce parts count and power dissipation of control and drive circuitry. This increases efficiency and reliability. Output sharing is also available using a single control wire between units. The total power varies between 600 and 1000 W, depending on the selection of output and control modules.

Other features include overvoltage and overcurrent protection. Supply is priced at \$775 in quantity. **Boschert Inc.**, 384 Santa Trinita Ave, Sunnyvale, CA 94086.

Circle 347

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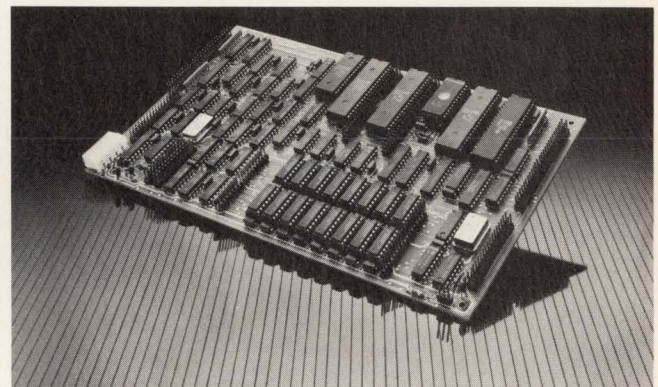
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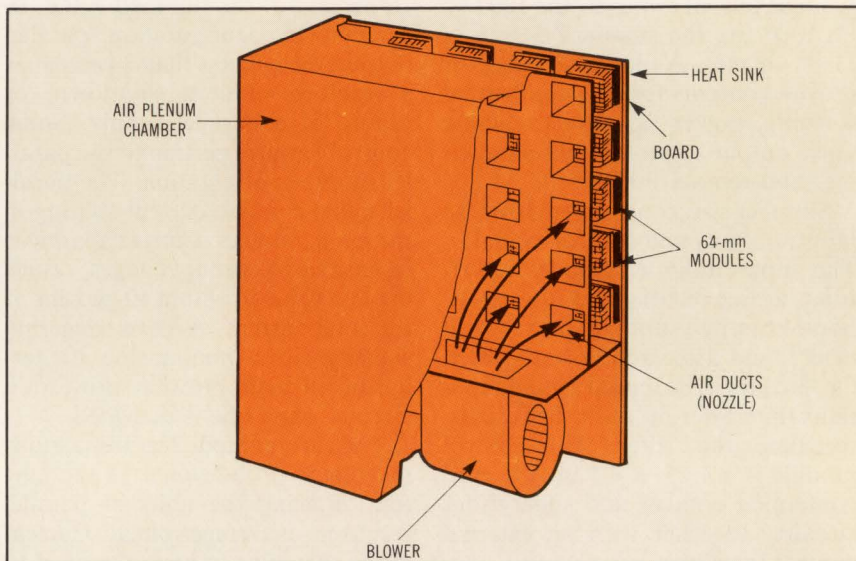
COMPUTER DESIGN/December 1984

253

## IBM packs in high density circuits

Packaging plays a critical role in the computational performance of IBM's mid-range 4381 processor. As a result, the new computer provides up to three times the performance of its predecessor—the IBM 4341—while not requiring air conditioning for cooling. The company uses an air-impingement cooling technique that yields twice the million instructions per second (MIPS) per kilowatt of power that was obtained from the 4341 machine. As a result, the individual power densities at the component level increased fivefold.

The densely packed circuits eliminated the need for an entire level of packaging. As opposed to the chip-on-module-on-card-on-board hierarchy used in the 4341, the 4381 has the chip mounted in modules. These modules are in turn stacked on a single board, thereby eliminating the



Cooling this compact mass is an air impingement mechanism with a blower that directs air simultaneously through nozzles. The air hits the circuit board in a perpendicular direction.

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card entirely. To top it off, the 4381 has twice the number of circuits in each module that the 4341 had on a card. More than 200,000 circuits are interconnected in 22 air-cooled modules. Three major components make up each module: a cooling assembly, the substrate chip carrier, and up to 36 chips holding about 700 circuits.

To cool these circuits, a blower supplies room air to a plenum chamber and directs the air simultaneously through nozzles (arranged in parallel rows) to all the modules plugged on the circuit board. Air impinges on the modules in a direction perpendicular to the circuit board at velocities over 10 m/s. It then exits near the base of each heat sink at the low velocity of 1.5 m/s into channels that lead to the periphery of the computer console. There are two primary advantages that parallel impingement has over

serial cooling, according to IBM engineers. First, each module receives fresh air without having been heated by adjacent modules. Second, no air conditioning is required.

Specially designed heat sinks further enhance the external cooling of the modules. In turn, chips in each module are cooled again in parallel with direct heat pads provided by the thermal paste placed between each chip and the module cap. The 4381 module can accommodate up to 36 chips in a 6 x 6 arrangement on a 64-mm ceramic substrate. High powered chips are judiciously placed on the substrate based on thermal considerations. It is then solder-sealed against a ceramic cap that is fitted with an aluminum heat sink.

In the 4381, some chips are qualified to 90°C, others to 85°C, and all are specified not to operate below

25°C. For this type of configuration, high powered chips are designed for placement on the module's periphery to take advantage of the proximity to the cap walls. These walls provide additional cooling paths to the heat sink. In the same manner, chips are allocated according to computed specifications to minimize temperature differences between them. This also reduces electrical noise.

The thermal model was verified against measurements made on actual modules. It can predict beginning-of-life and end-of-life operating temperatures and it compensates for appropriate thermal parameters as determined by diverse test modules. **IBM, Information Systems Group**, 900 King St, Rye Brook, NY 10573.

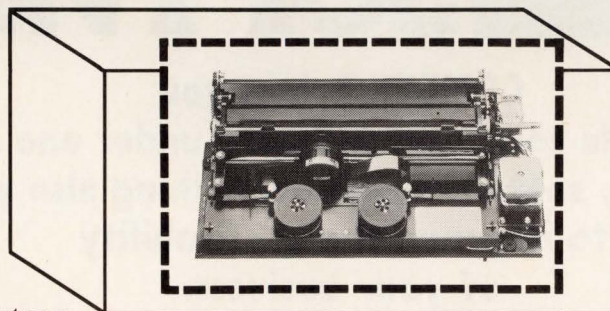
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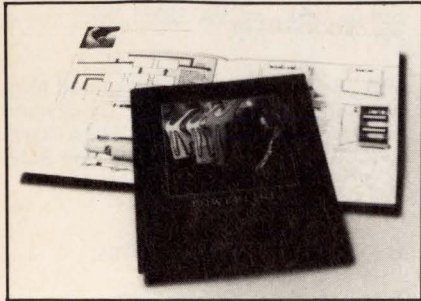


## LITERATURE

### Annual book of standards

The 1985 ASTM catalog describes the 66 volumes of the *Annual Book of ASTM Standards*. Also listed are several hundred other technical publications from the group, which strives to achieve voluntary consensus standards for materials, systems and services. **ASTM**, Philadelphia, Pa.  
Circle 410

### Uninterruptible power



Power products compose a 12-page color brochure. Rotary systems are highlighted in power ranges from 5 kVA to 1000 kVA. This line features optional sound attenuating enclosures and full digital instrumentation. **Computer Power Products**, Gardena, Calif.  
Circle 411

### Custom design

This four-page item outlines ACT capabilities in custom design, engineering, and development services for electronic assemblies and systems. Circuit design, software development, microprocessor applications, as well as product design and development, receive full treatment. **Advanced Control Technology, Inc.**, Ivyland, Pa.  
Circle 412

### Instrument and control systems

A 12-page booklet outlines the EIS-110 realtime operating system for microprocessor-based instrument and control configurations. **Electronic Information Systems, Inc.**, Stamford, Conn.  
Circle 413

### STD bus product line

A full line of STD bus equipment is described in a 40-page folder. Memory systems, development systems, networking, and power supplies are just a few of the topics covered. **Datricon Corp.**, Lake Oswego, Ore.  
Circle 414

### Printed circuit assembly

Packaging and interconnect design, as well as assembly and testing, highlight a brochure from Interconics. Printed circuit assembly turnkey services also get full treatment. **Interconics**, St Paul, Minn.  
Circle 415

### Digital stimulus/response testing

Brochures detailing digital stimulus/response testing via series RS-4000 pattern generator/analyzers and the RS-660 digital word generator are available. **Interface Technology**, San Dimas, Calif.  
Circle 416

### Chip capacitor methods

A 25-page booklet depicts multilayer ceramic capacitor chips. Coverage of electrical properties and electrical parameter testing is aimed at reaping better understanding of the chip capacitor. **Johanson Dielectrics, Inc.**, Burbank, Calif.  
Circle 417

### Control catalog

Positioning and tracking controls are illustrated in a 24-page catalog of input devices. Joysticks, forcesticks, control grips, trackballs, and mouse controls are among the items covered. **Measurement Systems, Inc.**, Norwalk, Conn.  
Circle 418

### Peripheral switching

An 88-page catalog outlines peripheral switching and data communication products. Catalog covers equipment for use with Burroughs, Data General, Texas Instruments, Wang, and other computers. **Digital Controls**, Dayton, Ohio.  
Circle 419

### Software for DEC hardware

Over 100 programs, including recent releases like InfoCen by 3CI and IMON from Bear Computer Systems, are described in a catalog devoted to DEC-compatible software. **Midcom Corp.**, Orange, Calif.  
Circle 420

### Supply catalog bears a famous name

Perkin-Elmer enters the catalog-based supply and accessory field with a 40-page, full-color catalog. This *P/E Prompt* catalog features a range of selected products, including modems, terminals, disk packs, and printer supplies. **Perkin-Elmer**, Oceanport, NJ.  
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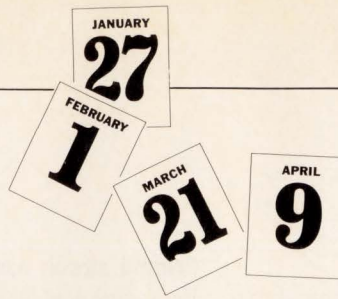
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## CONFERENCES

**JAN 8-10—CAD/CAM International**, National Exhibition Center, Birmingham, England. INFORMATION: EMAP Int'l Exhibitions Ltd, 8 Herbal Hill, London EC1R 5JR. Tel: 01-837-3699

**JAN 8** (Irvine, Tex), **JAN 29** (Houston, Tex), **JAN 31** (Dallas, Tex)—**The Invitational Computer Conf**, INFORMATION: Susan Fitzgerald, B. J. Johnson & Assoc, Inc, 3151 Airway Ave, C-2, Costa Mesa, CA 92626. Tel: 714/957-0171

**JAN 14-16—S.M.A.R.T (Surface mount and reflow technology) Seminar**, Sheraton Hotel, New Orleans, La. INFORMATION: Components Group, Electronics Industries Assn, 2001 Eye St NW, Washington, DC 20006. Tel: 202/457-4930

**JAN 24-26—Modeling and Simulation on Microcomputers**, Bahia Hotel, San Diego, Calif. INFORMATION: Ray Swartz, Berkeley Decisions/Systems Inc, 730 Park Ct, Santa Clara, CA 95050. Tel: 408/984-6397

**FEB 5-7—Mini/Micro West Computer Conf and Exhibit**, Anaheim Hilton Hotel, Anaheim Calif. INFORMATION: Nancy Hogan, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**FEB 13-15—Int'l Solid State Circuits Conf**, New York Hilton, New York, NY. INFORMATION: Lewis Winner, Almeria, Coral Gables, FL 33134. Tel: 305/446-8193/4

**FEB 25-28—Compcon Spring**, Cathedral Hill Hotel, San Francisco, Calif. INFORMATION: Harry Hayman, PO Box 639, Silver Spring, MD 20901. Tel: 301/589-8142

**FEB 26-28—Automated Design & Engineering for Electronics**, Anaheim Hilton & Towers, Anaheim, Calif. INFORMATION: Cahners Expo Group, Cahners Plaza, PO Box 5060, Des Plaines, IL 60018. Tel: 312/299-9311

**MAR 5-7—Southcon & Mini/Micro Southeast**, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Dale Litherland, Electronic Conventions, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

**MAR 7-8—Int'l Conf in Industrial Automation**, Hong Kong. INFORMATION: Conf Secretary, Autotech Hong Kong, Hong Kong Productivity Center, 12/F, World Commerce Center, 11 Canton Rd, Tsimshatsui, Hong Kong. Tel: 3-723-5656

**MAR 11-14—National Design Engineering Show**, McCormick Place, Chicago, Ill. INFORMATION: Cahners Expo Group, PO Box 3833, Stamford, CT 06905. Tel: 203/964-0000

**MAR 13-15—Picosecond Electronics and Optoelectronics**, Hyatt Lake Tahoe, Incline Village, Nev. INFORMATION: Optical Society of America, 1816 Jefferson Pl, NW, Washington, DC 20036. Tel: 202/223-0920

**MAR 13-15—Simulation Symposium**, Tampa, Fla. INFORMATION: Alexander Kran, IBM Corp, East Fishkill Facility, Hopewell Junction, NY 12533. Tel: 914/894-7142

**MAR 20-22—Phoenix Conf on Computers & Communications**, Hyatt Regency Hotel, Tampa, Fla. INFORMATION: Doug Powell, Motorola, Inc, PO Box 2953, Phoenix, AZ 85062. Tel: 602/244-3965

**MAR 25-28—Applied Machine Vision Conf**, Cobo Hall, Detroit, Mich. INFORMATION: Robotics Industry Assoc, PO Box 1366, Dearborn, MI 48121. Tel: 313/271-7800

**MAR 25-28—IEEE Infocom 85**, Washington, DC. INFORMATION: Celia L. Desmond, Rm 1855, 160 Elgin St, Ottawa, Ontario, Canada K1G 3J4. Tel: 613/239-4510

**MAR 25-29—IEEE Int'l Conf on Robotics and Automation**, Marriott's Pavilion Hotel, St Louis, Mo. INFORMATION: Dr K. S. Fu, Dept of Elec Engin, Purdue Univ, West Lafayette, IN 47907. Tel: 317/494-3433

**MAR 31-APR 3—Softcon**, Georgia World Congress Center, Atlanta, Ga. INFORMATION: Northeast Expo, 822 Boylston St, Chestnut Hill, MA 02167. Tel: 617/739-2000

**APR 14-18—Computer Graphics Conf**, Dallas Conv Center, Dallas, Tex. INFORMATION: National Computer Graphics Assoc, 8401 Arlington Blvd, Ste 601, Fairfax, VA 22031. Tel: 703/698-9600

**APR 16-18—Computer Integrated Mfg and Communications Conf**, Disneyland Hotel, Anaheim, Calif. INFORMATION: CASA/SME Public Relations, One SME Dr, PO Box 930, Dearborn, MI 48121. Tel: 313/271-0777

**APR 17-24—Hannover Fair '85**, Hannover, West Germany. INFORMATION: Hannover Fairs Information Center, PO Box 338, Whitehouse, NJ 08888. Tel: 201/534-9044

**APR 23-25—Electro and Mini/Micro Northeast**, Coliseum and Sheraton Center, New York, NY. INFORMATION: Dale Litherland, Electronic Conventions, Inc, 8110 Airport Blvd, Los Angeles, CA 90045. Tel: 213/772-2965

## SHORT COURSES

**JAN 7-11—Introduction to Command, Control, and Communications Systems**, The George Washington Univ, Washington, DC. INFORMATION: Merril A. Ferber, The George Washington Univ, School of Engineering and Applied Science, Washington, DC 20052. Tel: 202/676-8522

**JAN 8-9** (San Francisco, Calif), **FEB 13-14** (New York, NY)—**Integrating Multivendor Voice & Data Networks**. INFORMATION: The DMW Group, Inc, Seminar Div, 2020 Hogback Rd, Ann Arbor, MI 48104. Tel: 313/971-5234

**JAN, FEB, MAR** (Anaheim, San Diego, and Palo Alto, Calif; Boston, Mass; Washington, DC; Baltimore, Md)—**Data Communications Courses**. INFORMATION: Ruth Dordick, Integrated Computer Systems, 6305 Arizona Pl, PO Box 45405, Los Angeles, CA 90045. Tel: 213/417-8888



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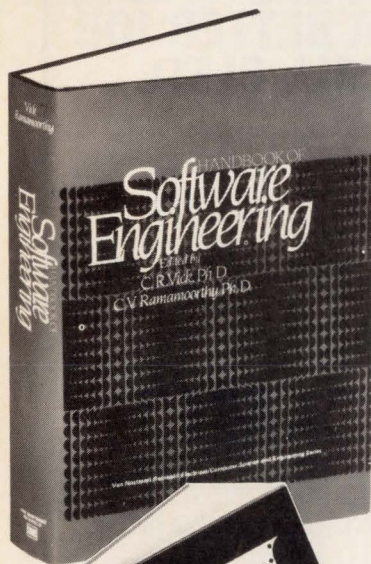
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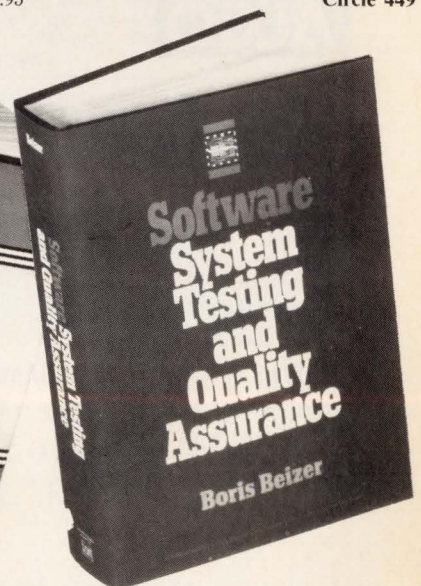
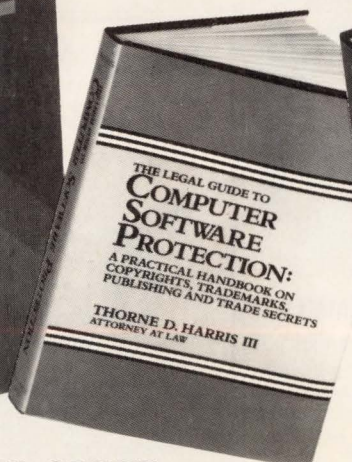
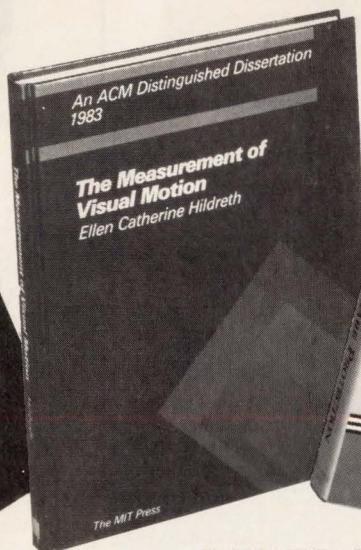
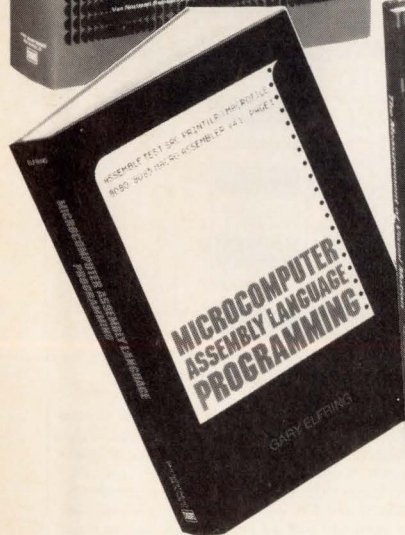
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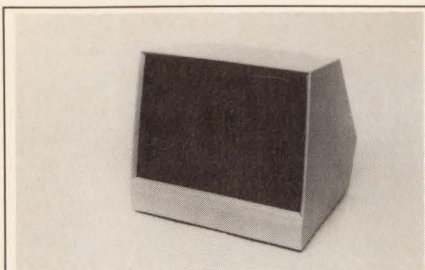
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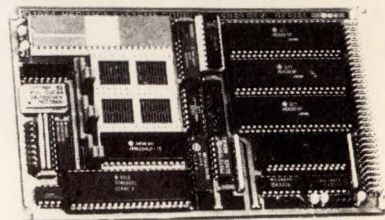
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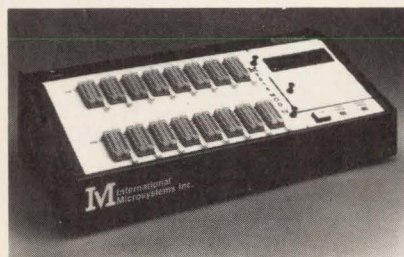
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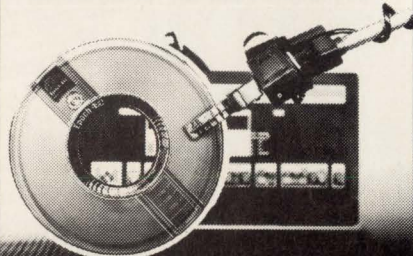


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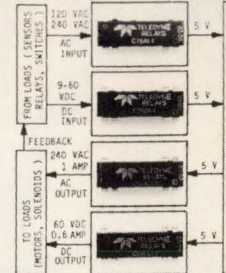
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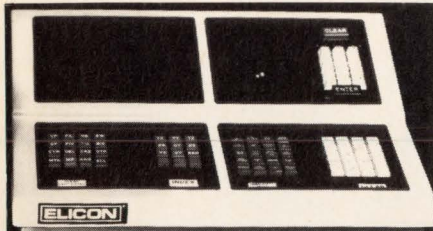
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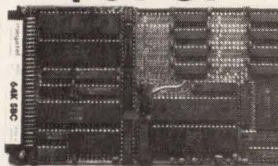
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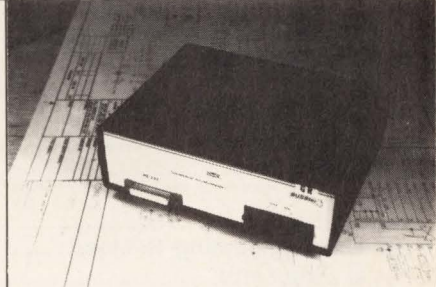


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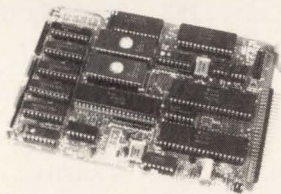
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