

G. Dan Hutcheson on
Mixed-signal
technology

A PENNWELL PUBLICATION

MAY 1, 1991

COMPUTER DESIGN

*Technology
and Design
Directions*

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS

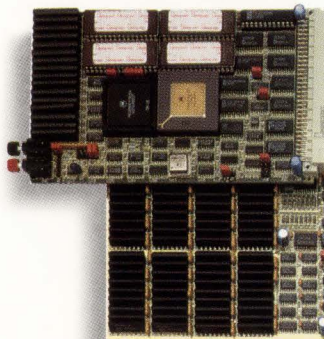
**Will monolithic or multichip processors
win the performance race?**



**ASIC complexity fuels
drive to HDL design**

**Object-oriented tools
expand the repertoire
of real-time developers**

Only GESPAC Has It All!



16 & 32-bit Single Board Computers

68000 8088
 68020 80186
 68030 80286
 68040* 80386
 T405, T805 Transputers

Static & Dynamic Memories

512K to 32 Mbytes Dynamic RAM
 Universal EPROM/RAM
 Memory Boards



Software

OS-9[®], VxWorks[®], Cross Code C[®]
 MS-DOS[®], QNX[®]
 Drivers and Tools
 All PC Software & OS's

Mass Storage

3.5" & 5.25" Floppy
 Controllers and Drives
 IDE Controller and Drives (500 Mb+)
 Intelligent SCSI Controller (up to 1+ Gb)
 Tape Streamer

Input/Output Interfaces

RS-232/422/485 SIOs
 Parallel TTL I/O, 10, 12 & 16-bit A/D & D/A
 Thermocouple, RTD Opto Isolated I/O
 Mechanical and Solid State Relays

Color Graphics

EGA and VGA Controllers
 ACRTC Based 750 x 520 x 256 Colors
 GDP Based 1280 x 1024 x 256 Colors

Motion Control

DC Servo Controller
 Stepper Motor Controller
 Resolver & Shaft Encoder

Call Toll Free 1-800-4-GESPAC
 or call (602) 962-5559.



Service

Support Hotlines
 Application Notes
 Integration Services
 Custom Design

Vision Subsystems

256 to 2048 Element Linear CCD Cameras
 Matrix CCD Camera Interface
 Real-Time Image Processing Hardware

Networking & Communications

10 Mb/s Ethernet[®], 10 Mb/s X.25
 2 Mb/s Arcnet[®], 1 Mb/s MIL 1553B
 1 Mb/s IEEE 488, 375 Kb/s Filbus[®]/Bitbus[®]
 Universal 68302 Based Controller

Accessories

Predecoded Prototyping Boards
 Terminal Strip Adapters
 Power Supply, Bus Extenders
 4-20 Slot Backplanes & Card Cages

Systems

Industrial PC AT Systems
 Turn-Key OS-9 Workstations

Only GESPAC offers over 200 state-of-the-art microcomputer boards

that are designed to work together, available from under a single roof and backed by a team dedicated to your success. With GESPAC, you can buy all the boards and software you'll ever need or you can get turn-key microsystems designed to meet your unique specifications. Move ahead of the pack and call today to receive the industry's most comprehensive catalog of microsystem solutions. See how GESPAC can help you build the system that best meets your unique specifications, in the shortest amount of time!



USA - CANADA
 50 West Hoover Ave.
 Mesa, Arizona
 85210 USA
 Tel. (602) 962-5559
 Fax. (602) 962-5750

EUROPE
 Z.I. les Playes
 83500 La Seyne
 France
 Tel. 94 30 34 34
 Fax. 94 87 35 52

INTERNATIONAL
 18, Chemin des Aulx
 CH-1228 Geneva
 Switzerland
 Tel. (022) 794 3400
 Fax. (022) 794 6477

* Available Q3 1991 TM/Companies: OS-9/Microware, QNX/Quantum, VxWorks/Wind River Systems, Ethernet/Xerox, Arcnet/Corvus, Bitbus/Intel, Filbus/GESPAC, CrossCode C/Software Development.

OMEGA

New

Easy Access = Maximum Accessibility

Quick access saves time in assembly, test, and maintenance. Loosen two captive fasteners and the front, top, and sides slide off for maximum access to all of the internal components. Each internal component comes out with two screws, or remove five hex nuts and the entire system lifts out of the bottom tray to provide a free-standing, fully functional development platform!

Peripherals Just Slide In

Up to eight half-height 5 1/4" peripherals simply slide into their mounting brackets.

The Quietest Backplane Available

Plug your VME system into the quietest backplane ever! Our new 10-LAYER VME backplanes handle the fastest VME signals with the absolute minimum distortion, crosstalk, and noise.

Engineered Cooling

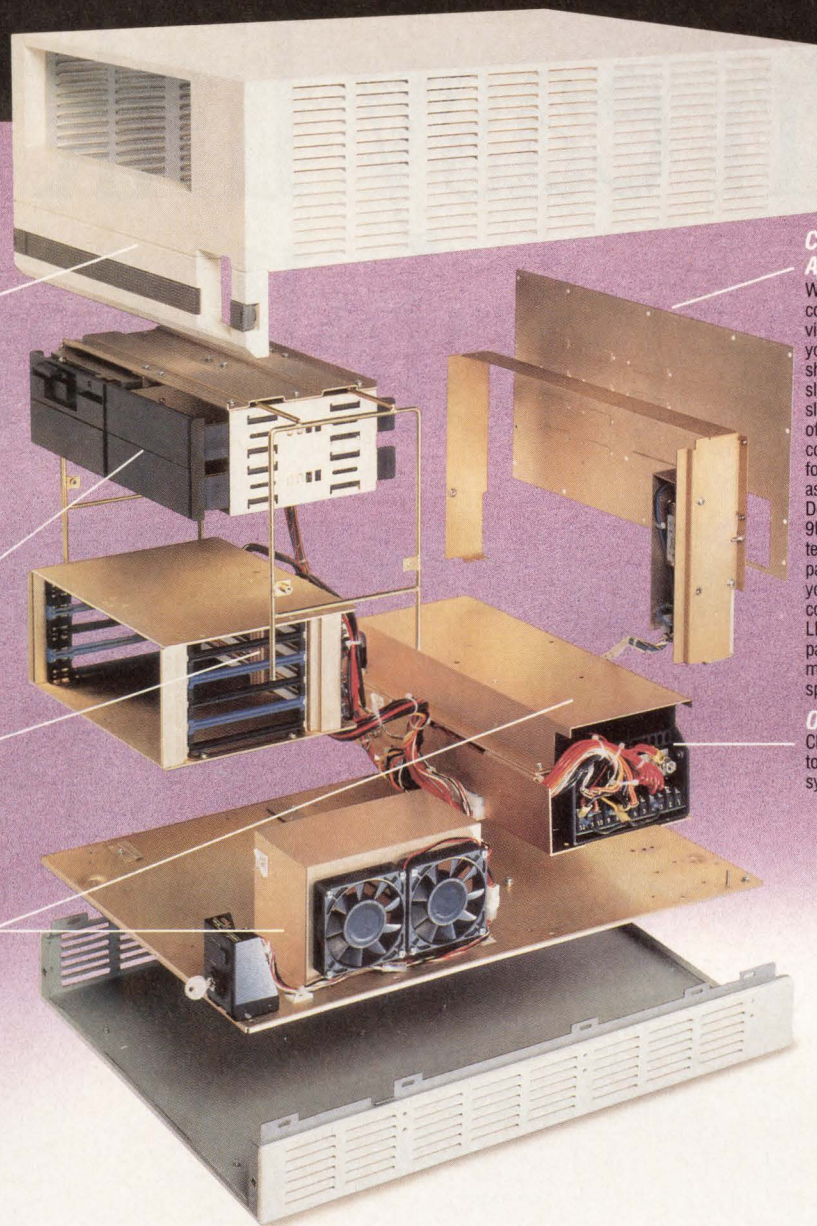
Airflow is directed over the components that need cooling — the power supply and your boards. Separate chambers maximize cooling by channeling airflow and restricting recirculation.

Configured for Your Application

With over 2000 standard configurations you can virtually design the enclosure yourself — and still get it off the shelf. Choose from 3 to 14 slots for VME or 4 to 18 slots for Multibus. Loads of peripheral options and configurations are available for rack and tabletop models as well as floor-standing DeskMate™ versions that accept 9U x 400mm cards. Or let our team of engineers provide a packaging solution tailored to your specifications — from configuring the front panel LEDs to customizing the rear panel. Designing enclosures to meet your specific needs is our specialty.

Optimum Power Output

Choose from 175 to 1000 Watts to satisfy the demands of your system.



The Last Word in System Packaging

Now you can benefit from 12 years of design experience and innovation that has made Electronic Solutions the industry leader in system packaging. The Omega™ Enclosures will give your VME or Multibus system the attractive exterior your image demands with a rugged, well-designed interior to withstand the most demanding environments. And besides the Electronic Solutions' full 3-Year warranty, the Omega bears FCC approvals and is UL, CSA, and TUV

listed to get your system to an international market in the shortest time possible.



Call Electronic Solutions for the latest information about the best choice for your system package. It's the last system enclosure you'll need to see.

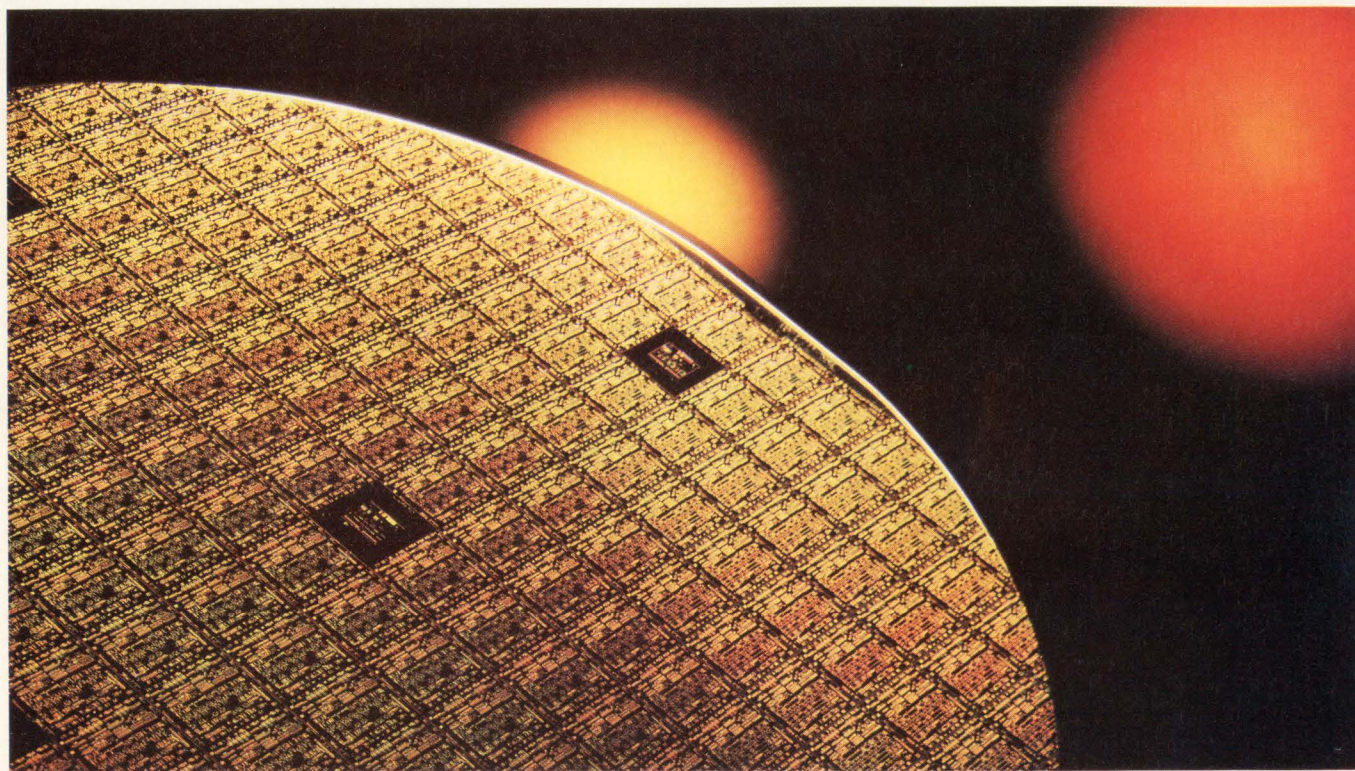


6790 Flanders Drive, San Diego, CA 92121
(619) 452-9333 FAX: 619-452-9464
Call **TOLL FREE (800) 854-7086**
in Calif. **(800) 772-7086**

CIRCLE NO. 2

Synchronous Communications

An easy link to higher intelligence.



To a PC, workstation or communications card, it seems like just another asynchronous UART. But to the intelligent, synchronous universe of high-speed data communications it looks and functions like the world's first virtual communications packet controller.

"It" is our exclusive new M650 Serial Packet Controller. In a single-chip CMOS package you now can add high-speed (14,400+ bits/sec) modems to your PC peripheral bus or integrate with most high-speed synchronous

communications networks.

The M650's dual-port mode architecture accomplishes in hardware what you can't do as well in software. Even after you've linked up multiple UARTs and messed with glue logic.

So the M650 can take the heat off your CPU and function comfortably as a communications sub-processor. And, in power-down mode, be sensitive to the low power demands of your laptop and notebook PC designs.

Clearly, it's the intelligent asynch/synchronous communications link your

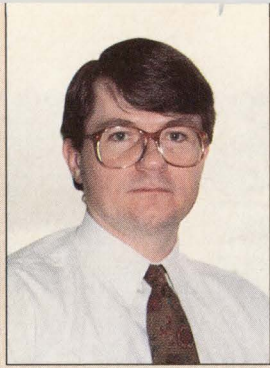
next-generation product designs are waiting for. To find out more, call us for literature package **CPD-10**. We'll connect you with your nearest Silicon Systems representative and update you on our latest developments.

1-800-624-8999, ext. 151.

Silicon Systems, Inc.
14351 Myford Road, Tustin, CA 92680
Ph (714) 731-7110 Fax (714) 731-6925

silicon systems[®]
A TDK Group Company

Circle No. 3 for Product Info
Circle No. 19 for Career Info

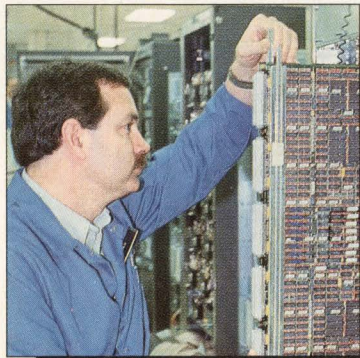


G. Dan Hutcheson on Mixed-signal technology Page 23

COMPUTER DESIGN

Technology and Design Directions

FOR ELECTRONIC ENGINEERS & ENGINEERING MANAGERS



Page 50

TECHNOLOGY UPDATES

Integrated Circuits

Are secondary caches for the 486 worth the money?28

Transputer performance boosted to 10x that of its predecessor36

80-MHz RISC processor screams through floating-point40

Interconnect key to speed of new programmable ASICs46

Computers and Subsystems

Supercomputer maker embraces standards50

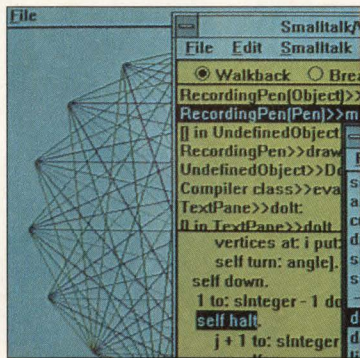
Single-chip DSPs invade SBus56

Design and Development Tools

Analysis tools help digital designers avoid analog speed traps62

Software

RISC instruction benchmarks spark performance debate69



Page 89

TECHNOLOGY AND DESIGN FEATURES

ASIC complexity fuels drive to HDL design

Spiralling gate counts and time-to-market pressures are making HDLs mandatory.....77

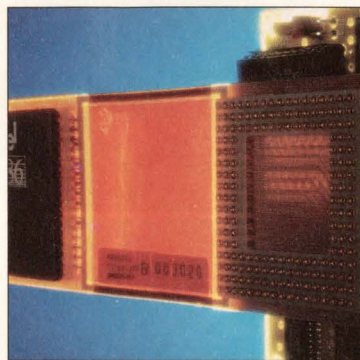
Object-oriented tools expand the repertoire of real-time developers

Object-oriented programming eases problems caused by program size and complexity, and its benefits are coming to real-time applications.....89

COVER STORY

Will monolithic or multichip processors win the performance race?

The era of the million-transistor microprocessor is upon us. "Megachip" blockbusters—some executing 100 Mips or more—are becoming available in both RISC and CISC designs.....100



Page 123

NEW PRODUCT HIGHLIGHTS

PRODUCT FOCUS

32-bit emulators struggle with processor complexities123

Design and Development Tools

Simulation tool simplifies top-down analog design129

Hardware modelers meet needs of both small and large design teams.....131

Integrated Circuits

Single-chip decoder PLDs give users freedom of choice133

High-speed CMOS gate arrays integrate 150,000 gates.....134

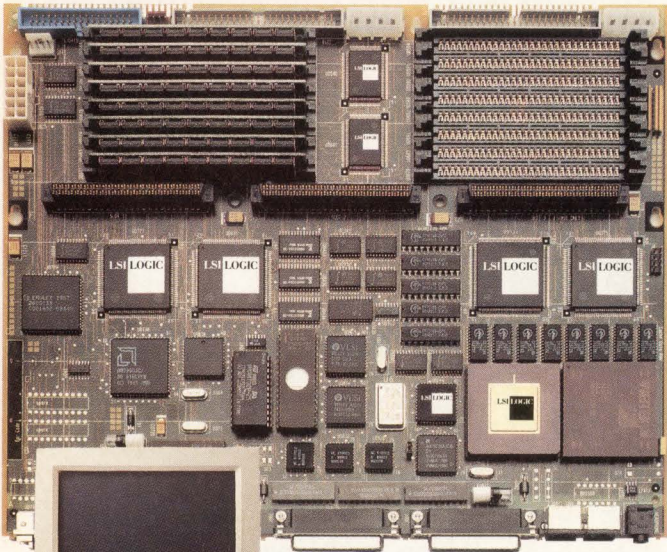
Computers and Subsystems

Controller moves PC architecture into embedded arena136

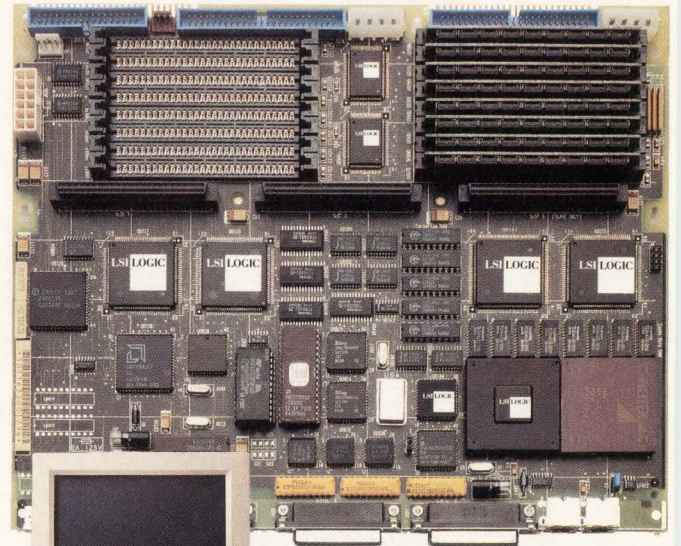
Versatile I/O processor races at 100 Mips.....138

DEPARTMENTS

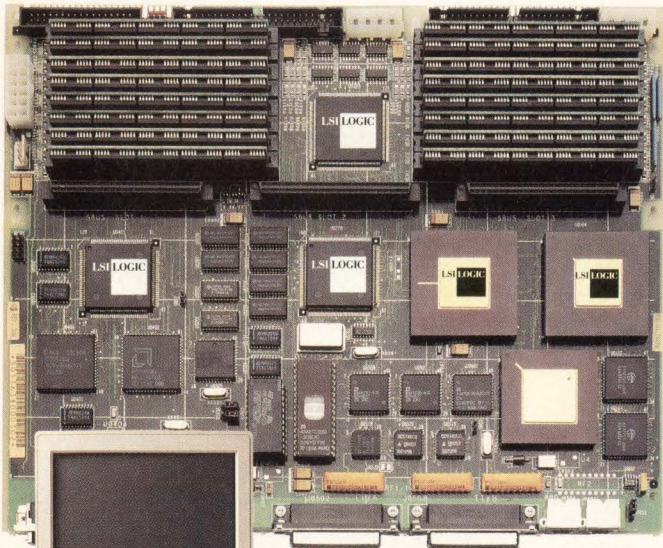
News Briefs	8
Editorial	14
Calendar	20
Advertisers Index	151



**April '89
SPARCstation 1**



**May '90
SPARCstation 1 +**

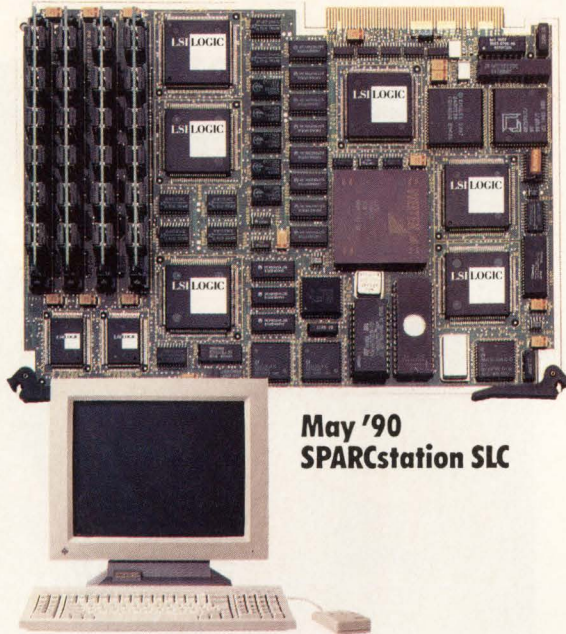


**November '90
SPARCstation 2**

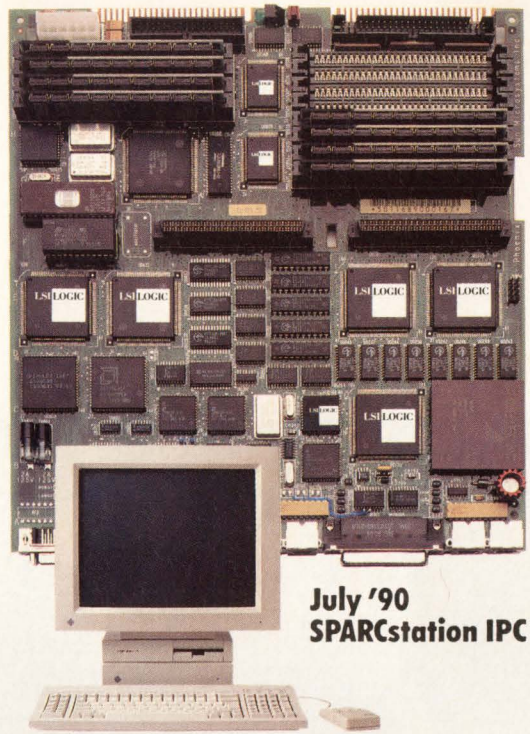


LSI HAS ANOTHER

© LSI Logic Corporation 1990. Sun Microsystems is a registered trademark of Sun Microsystems, Inc. SPARC is a registered trademark of SPARC International, Inc., and SPARCstation is used under license therefrom. UNIX is a registered trademark of AT&T Bell Labs.



May '90
SPARCstation SLC



July '90
SPARCstation IPC

S JUST MADE ER SUN SHINE.

Since introducing SPARCstation 1 in April '89, Sun has utilized LSI Logic's RISC and ASIC technology and design methodology to pack more processing power into smaller footprints.

This strategic partnership has enabled Sun to compress time to market to an unbelievable four months between new product announcements and has reduced their time to volume. Forever altering the rules on time to market. And capturing the dominant position in the workstation market in the process.

Sun's latest creation, SPARCstation 2, is a shining example. This powerful new workstation was brought to market just four months after the introduction of the

SPARCstation IPC. By leveraging the power of LSI Logic's RISC and ASIC technology, Sun has quickly introduced a whole new level of price/performance in UNIX workstations.

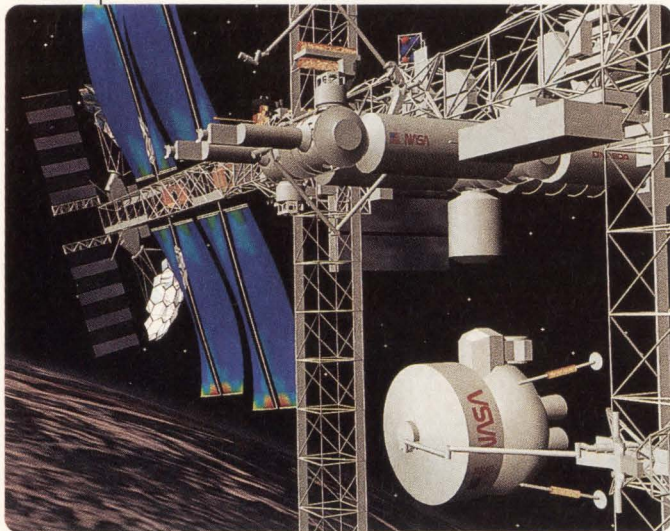
If you have some brilliant new product concepts on your horizon, with windows of opportunity opening as often as every four months, call us at 1-800-451-2742, or write to LSI Logic, 1551 McCarthy Blvd, MS D102, Milpitas, CA 95035.

We'd like to show you how quickly your new product can see the light of day.



ACROSS THE BOARD

CIRCLE NO. 4



CASE and AI solutions include HP's SoftBench; Interactive Development Environments; Intellicorp; Inference; and Neuron Data.



Mechanical CAD solutions include SDRC; HP ME 10 and 30; McDonnell Douglas; Parametric Technology; and PDA.

Move up the launch

Whether you're launching a new car, a new chip, or a new magazine, you'll get it to market faster with a new HP Apollo RISC workstation.

And that speed won't cost you, either. Those 76 MIPS come for less than \$20K for gray-scale; \$27K for color. And, if 57 MIPS will launch you fast

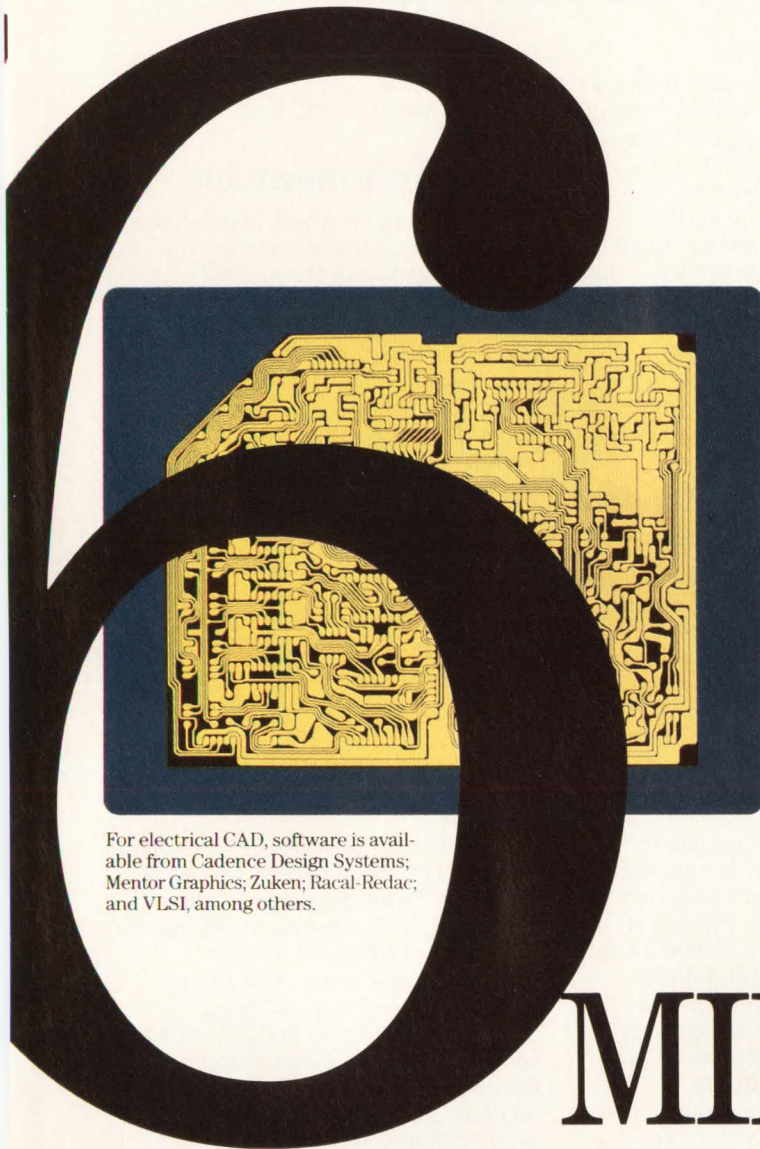
enough, you can get that for under \$12K.

Of course, you'll go nowhere fast unless your applications run on our workstations.

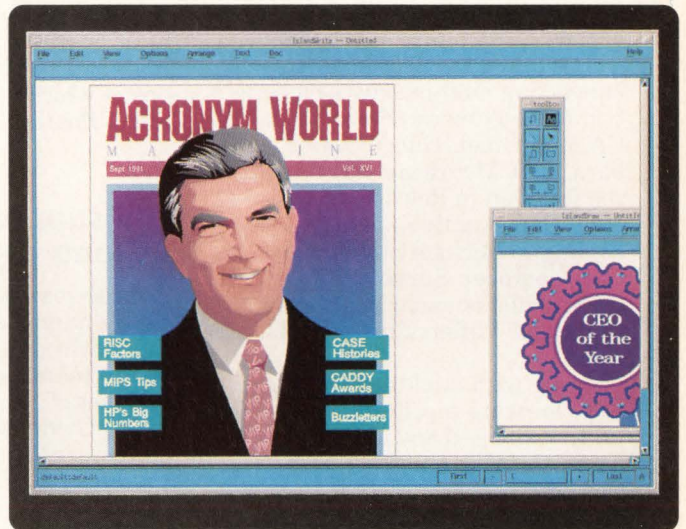
Chances are very good that they do. The top programs are already ported. And more than 3,600 applications are now available on PA-RISC.

HP's open design allows for an easy fit into your multivendor network. As well as for easy upgrades when you're ready to grow.

The sooner you get your hands on a new HP Apollo RISC workstation, the sooner you'll be launching new products. So



For electrical CAD, software is available from Cadence Design Systems; Mentor Graphics; Zuken; Racal-Redac; and VLSI, among others.



For Electronic Publishing, Desktop Productivity and Database, available software includes Informix; Oracle; ASK/Ingres; Interleaf; and Island Graphics.

MIPS!

dates.

call 1-800-637-7740, Ext. 2049 for more information. It could help your business really take off.



© 1991 Hewlett-Packard Company CPWG016

CIRCLE NO. 5

860 compilers on the way

Dual-instruction mode is one of the more-powerful features of the 860 chip from Intel, but only now have compiler vendors begun to support this mode. Without compiler support, which allows integer and floating-point calculations to be issued in parallel, much of the power of the 860 remains untapped.

The first compiler vendors supporting dual-instruction operation are Metaware (Santa Cruz, CA) and Green-Hills (Santa Barbara, CA). Metaware will support the function in Release 2.4 of its High C, currently in beta test, according to Michael Stebbins, systems engineer. Support from Green-Hills is under development, said Steve Lafferty, director of OEM sales.

Along with dual-mode instruction, software pipelining is another under-exploited 860 feature. Useful for performing repetitive operations that are independent of the results of previous operations (in applications such as vector processing), software pipelining will also be included in High C, Release 2.4. Again, it's under development at Green-Hills. With these new compiler optimizations and more, Metaware claims that the 860 chip will benchmark at over 86,000 Dhrystones/s, a 41 percent improvement over the earlier release.

Unfortunately, compiler support for the on-chip 3-D graphics engine won't be forthcoming in the short term. Despite the lack of compiler support, the 860 is the 3-D graphics engine of choice in the workstation world.

—Dave Wilson

860 bugs kept under cover

Designers integrating 860 RISC boards into their AT or VME systems shouldn't expect their board vendors to supply a current bug list for the processor—they may not be allowed to. At least one board vendor has been required to sign a non-disclosure agreement with Intel (Santa Clara, CA) prohibiting the discussion of the bugs with customers. All of that vendor's customers have been asked to refer

their questions to Intel.

"You can try to get this information from Intel, but it's the kind of stuff they really just guard the [expletive deleted] out of. They just don't want anyone to know. This is extremely aggravating for us because the customers want to know what these problems are too," one board vendor reported. Apparently, after nearly two years in the market, the 860 still has five bugs, one of which is said to significantly affect floating-point performance.

—Dave Wilson

"I'll support any standard as long as it's mine"

A large-scale lobbying effort by the newly named Advanced Computing Environment consortium has begun to sell software developers on a set of standards based on MIPS Computer Systems' RISC architecture. The standards embrace systems including laptops, PCs, workstations, and supercomputers. Among the major players in the 21-member group are Compaq Computer, MIPS, Digital Equipment Corp, Microsoft, and The Santa Cruz Operation. The group's efforts appear to focus primarily on the yet-to-be-available R4000 processor. The consortium has agreed on a variety of features that will provide both binary and source-code compatibility.

These efforts have groups of industry leaders poised for yet another clash over standards issues. "I'll support any standard as long as it's mine," commented one industry leader.

Groups supporting the Sparc and MIPS processors are amassing ammunition. The escalation in competitive maneuvering may explain why Sun Microsystems recently let some of its techies out of the laboratory to tour the country with studies pushing Sparc as the instruction set architecture with the brightest future (see "RISC instruction benchmarks spark performance debate," p 69). Sun is certainly at the top of archrival MIPS' hit list and is no friend of the new consortium. Sun president Scott MacNeally was credited with

commenting, "Those who can't compete, consort."

—Warren Andrews and Tom Williams

Mac clones inevitable

By delivering an Apple Macintosh-compatible operating system on disk and in ROM, three ASICs that replicate the logic of the Mac, and user interface software based on OSF's Motif, Nutek (Cupertino, CA) will enable OEMs to start designing Apple Mac clones. To get around legal wranglings, the Nutek operating system was written from the ground up and required more than a quarter million lines of code. The chip set has been prototyped and is currently going through simulation and validation. Shippable parts should be ready by the end of the year, according to Benjamin Chou, Nutek's president.

—Dave Wilson

Mentor's Falcon makes slow ascent

Mentor Graphics (Wilsonville, OR) has started shipping the first elements of its long-awaited Concurrent Design Environment, Release 8.0. Phase I of the Falcon Framework software, the Board Station printed circuit board design and analysis tool, as well as thermal-analysis and on-line documentation tools, will run only on older HP/Apollo Domain 400 workstations. Mentor hopes to have these tools up and running on Sun workstations by the end of the second quarter, with third-quarter releases running on the new HP 700 workstations.

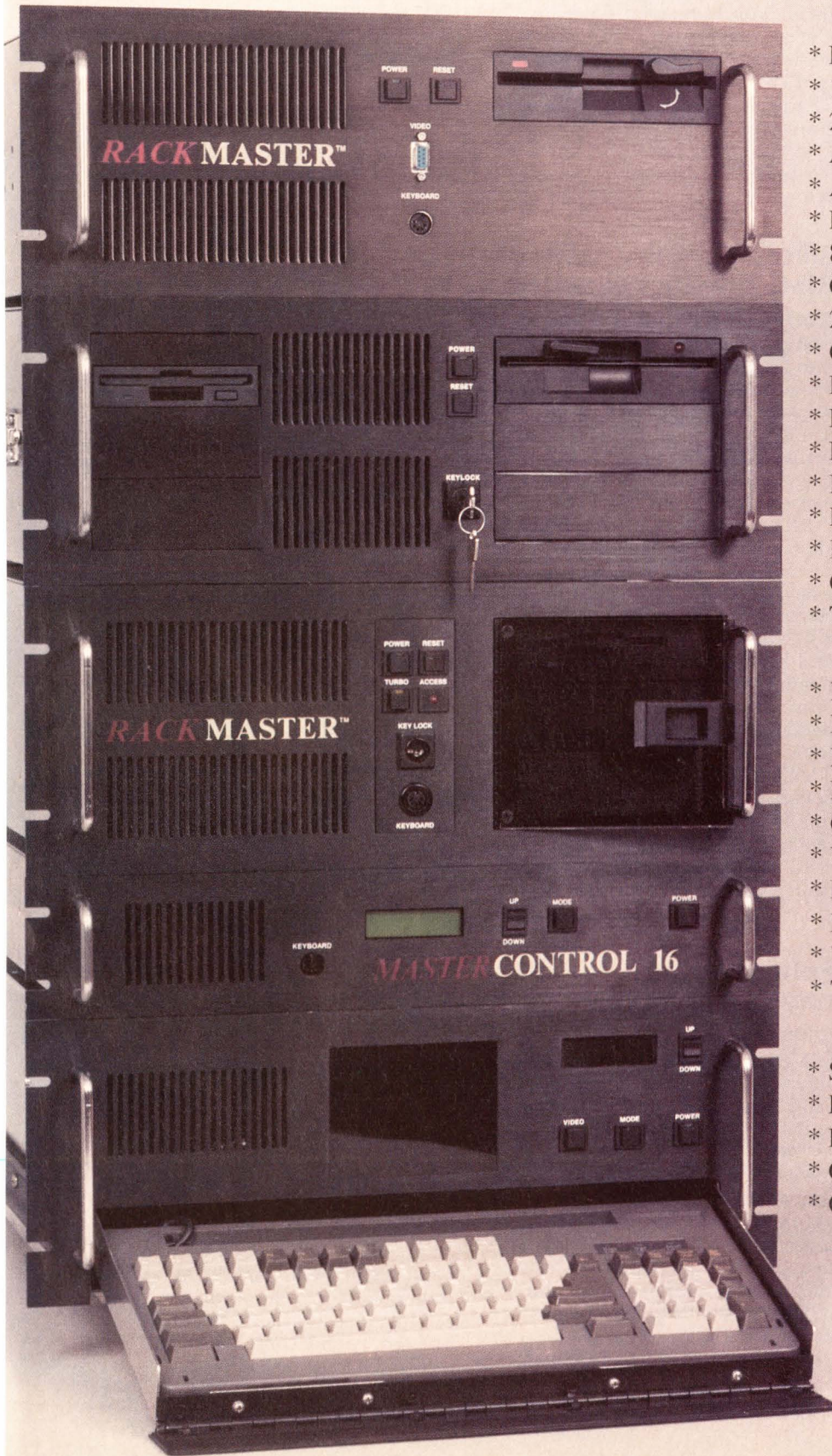
The Phase II release will include tools for the design of hybrids, multichip modules and ICs. Phase III will include QuickSim II, Design Architect, System-1076, and VHDL synthesis. Some analysts are downplaying the importance of the Phase I tools because they target only printed circuit board design, which accounts for 15 to 20 percent of Mentor's revenues. Until more front-end tools are released, it's doubtful that Phase I will have much of an impact.

—Mike Donlin

Continued on page 10

RACK MASTER™

Our Systems Stack Up To Be The BEST!



SYSTEM FACTS

- * Rugged, Reliable 19" Rackmount
- * 18 inches deep with 3 drive bays
- * 24 inches deep with 6 drive bays
- * Accepts Motherboards
- * Accepts Passive Backplanes
- * EISA and ISA bus architectures
- * 8, 12 or 16 -slot configurations
- * Cortex Split Backplanes
- * 200W to 350W power supplies
- * Custom Power Supplies available
- * Front mounted keyboard socket
- * Rackmount monitors
- * Rackmount keyboard drawer
- * MS-DOS, OS/2, Unix, Xenix
- * Dual card cage cooling fans
- * Master Control 16 controller
- * Quick disconnect extending slides
- * Tilting and extending slides

SYSTEM USAGE

- * Network File Server / Duplexing
- * Data Acquisition
- * Factory Automation
- * Motion Control / Robotics
- * Communication Networks
- * Voice Mail / Message Systems
- * Broadcast Communications
- * Military / Defense Systems
- * Video Editing Studios
- * Test System Controllers

ENGINEERING

- * Steel Enclosure
- * EMI/RFI Plating
- * Hard Coat Anodized Face Plate
- * Custom Configurations
- * Custom Engineering / Design

Cortex Corporation
1-800-888-RACK

12274 Nicollet Ave. S
Burnsville, MN 55337
(612)894-3354 Fax (2414)

Continued from page 8

Another record-breaking SBC for Moto?

When Motorola rolled out a new CPU board at the most recent Buscon (January 1991), many in the audience expected the company to also announce the follow-up version of its MVME147. Instead, it introduced the next version of its 88000 RISC-based board, the MVME187. The MVME167, as the 68040-based board was expected to be called, remained elusive.

The 68030-based MVME147 set new price/performance standards for single-board computers when it was introduced. At a list price of \$4,995 with very deep quantity discounts, the board was the most successful single-board computer ever offered. It's reasonable to assume that the 040-based 167 board and 88000-based 187 will share many of the same features, ASICs and design as the 147. Word has it that the two boards were designed concurrently and that software problems held up the 167.

With sampling expected to start sometime in July, Motorola expects the 167 to top sales of the 147. According to reports, the board is a "screamer" and, although the list price is rumored to be significantly below that of the 147, there's no hint the company will tighten up on its discounting policy. —Warren Andrews

DAC hears pleas of EDA attendees

After much pressure from groups such as the Electronic Design Automation Companies, the Design Automation Conference (DAC) has announced plans to attract more EDA users and managers to this year's conference. The 28th annual gathering, slated to take place in San Francisco from June 17 to 21, will feature free first day passes for exhibits, as well as two panel sessions aimed at EDA users and managers.

Many vendors claimed that the return on their investments in the conference was unsatisfactory.

Rather than face the possibility of a rival show targeted to users and management, DAC officials formed an Industrial Program Committee to sponsor presentations from corporate presidents and CEOs of vendor companies. The lineup includes Tom Bruggere from Mentor Graphics, Wilfred Corrigan from LSI Logic and Joe Costello from Cadence Design Systems. —Mike Donlin

Silicon Graphics hands off RISC, graphics expertise

A strategic agreement between Compaq Computer (Houston, TX) and Silicon Graphics (Mountain View, CA) is expected to pave the way for technology exchange and the joint technical development of future products. The plan includes Compaq's purchase of a 13 percent equity stake in Silicon Graphics.

Silicon Graphics has agreed to share its Iris graphics library and its expertise in designing RISC-based systems, while Compaq will contribute its expertise in the EISA bus standard, VLSI design and high-volume manufacturing techniques. Using the newly acquired technology, Compaq is expected to build low-cost RISC-based systems with leading-edge graphics. The agreement benefits Silicon Graphics by further promoting its graphics technology. The Iris library is already licensed to IBM for use in its RS/6000 RISC workstations. —Jeffrey Child

Futurebus spec one step closer

With its March meeting, the IEEE 896 working group took another step toward completing the Futurebus+ specification. Negative ballots from the sponsor ballot phase of 896.1 (the logical layer) have been resolved, and the draft is out for another 30-day spin around the block. The physical layer and profiles are already out to the committee for its sponsor ballot phase. Ballot review and negative ballot resolution is expected for the next session.

IEEE Project Authorization Re-

quests have been granted for additional profiles: "T" for telecom/high-availability systems; "M" for military modules; and "D" for the desktop profile. These have been upgraded from study-group status. Profile "C" for cable interconnect has been granted study group status to look at the benefits and methodologies for interconnecting Futurebus+ systems with a cache-coherent cable media.

Finally, the long-awaited P896.3 Systems Recommended Practices (the "How to do it" document) is in the final stretch, and submission for final ballot is expected this month. If the name and "P" number don't seem to match, it's because the Systems Configuration Guide has become Systems Recommended Practices. —Warren Andrews

Synthesis a hot topic at ASIC conference

Hundreds of Idea'91 conference-goers left standing room only last month at the technical sessions on low-level logic synthesis. If the number of attendees at the sessions was any indication of how the technology is catching on, synthesis should be a mainstream design methodology before long.

At one session, Howard Landman, senior CAD engineer for logic synthesis at Sun Microsystems (Mountain View, CA), presented a user's perspective. He told attendees that synthesis tools are not pushbutton, and that they leave many options for designers to explore. Designers should stop asking whether logic synthesis tools are better than human designers, Landman said, and instead ask whether a designer with synthesis tools is better than one without them. —Barbara Tuck

Committee zeros in on FB+ military connector style

In an effort to standardize on an open architecture for future military/avionics applications, a committee comprising the IEEE and several subcontractors has selected a specific connector style



DY 4 VME

When you must win!

For your "must-win" defense and aerospace programs, put the world's leading supplier of MIL-SPEC VMEbus systems on your team. Ready-to-run VMEbus systems from DY 4 are selected overwhelmingly by system integrators for aerospace and defense programs worldwide.

DY 4 provides performance, reliability and cost-effectiveness through integration of a full range of open-system VMEbus products and services to military, rugged and commercial standards.

DY 4's system solutions incorporate non-developmental item (NDI) products from the broadest product line in

the business – CPUs... memories... communications controllers... analog I/O... high-performance graphics engines... chassis... Ada* foundation software and built-in-test (BIT) diagnostics.

DY 4 provides a comprehensive quality program to MIL-Q-9858A and fully compliant configuration management to MIL-STD-483; design procedures conform to MIL-STD-1521 with manufacturing according to MIL-I-45608 (quality control) and soldering to MIL-STD-2000 in an ESD-controlled environment.



**Customer First,
Quality Always**

DY 4 Systems Inc.

Campbell, CA
Tel: (408) 377-9824
Fax: (408) 377-4725

Nashua, NH
Tel: (603) 595-2400
Fax: (603) 595-4343

21 Fitzgerald Road, Nepean, Ontario K2H 9J4 Tel: (613) 596-9911 Fax: (613) 596-0574

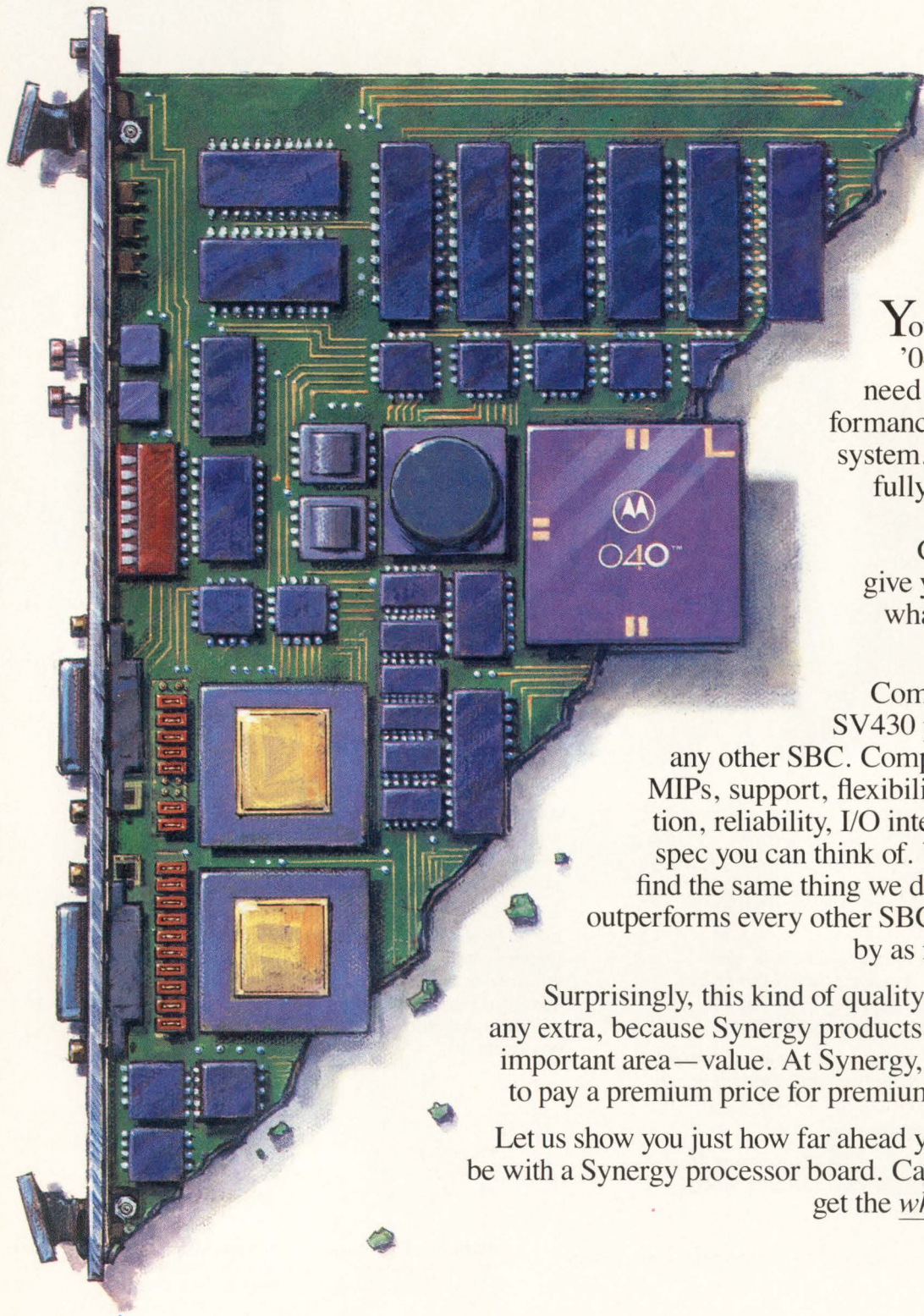
Hammel, Denmark
Tel: +45-86-963624
Fax: +45-86-962575

Pennant Hills, Australia
Tel: +61-2-484-6314
Fax: +61-2-875-1665

*Ada is a trademark of the United States Department of Defense

CIRCLE NO. 7

Why Settle for 1/2



You've chosen the '040 because you need maximum performance in your VME system. But look carefully, because other Single Board Computers may give you only half of what you expected from the '040.

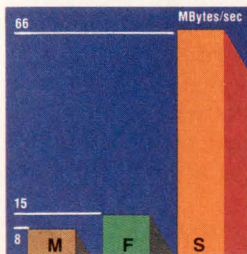
Compare Synergy's SV430 performance to any other SBC. Compare bus speed, MIPS, support, flexibility, documentation, reliability, I/O intelligence or any spec you can think of. We think you'll find the same thing we did—the SV430 outperforms every other SBC on the market by as much as 150%.

Surprisingly, this kind of quality won't cost you any extra, because Synergy products lead in another important area—value. At Synergy, you don't have to pay a premium price for premium performance.

Let us show you just how far ahead your system can be with a Synergy processor board. Call us today, and get the whole '040 story.

an '040 Board?

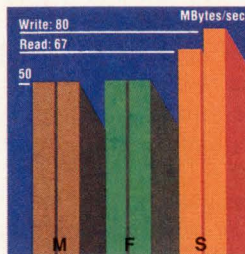
Compare our specs.
Synergy is superior across the board!



VME Transfers

VME64 doubles bus performance to 66 MB/s—and the SV430 is the only '040 board that has it. But we don't need VME64 to win this comparison.

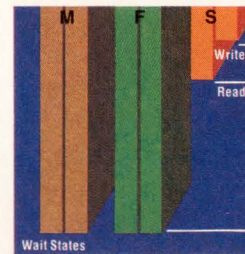
Even normal 32-bit transfers race at 33 MB/s. That's 200% faster than Force or Motorola.



DRAM Burst Rates

A 25 MHz '040 is capable of accessing memory at 80 MB/s. The closer you are to this maximum, the more '040 perform-

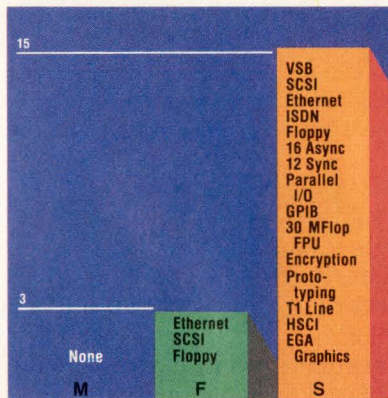
ance you're gaining. SV430 bursts are 26% faster than Force and Motorola.



DRAM Random Accesses

Non-burst '040 performance is measured in wait states. Fewer wait states mean higher performance. The SV430 is not only 66%

faster than Force or Motorola, it supports twice the on-board memory—32 MB.

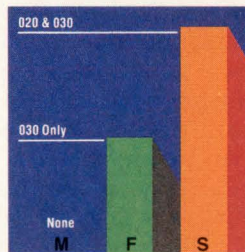


I/O Modules

Synergy's EZ-Bus modules are compatible with our entire line of SBCs. This means Synergy's current line of 12 intelligent I/O modules are immediately available for the SV430—today. No other vendor comes close for selection, functionality or availability.

Data from Motorola MVME165 data sheet dated 2/90, and Force CPU-40 data sheet A1 Rev. 1. DRAM measurements shown are with parity. VMEbus transfers are to a 60ns slave.

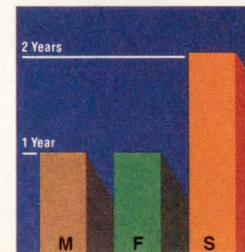
VME64 is a trademark of Performance Technologies, Inc.



'020/'030 Compatibility

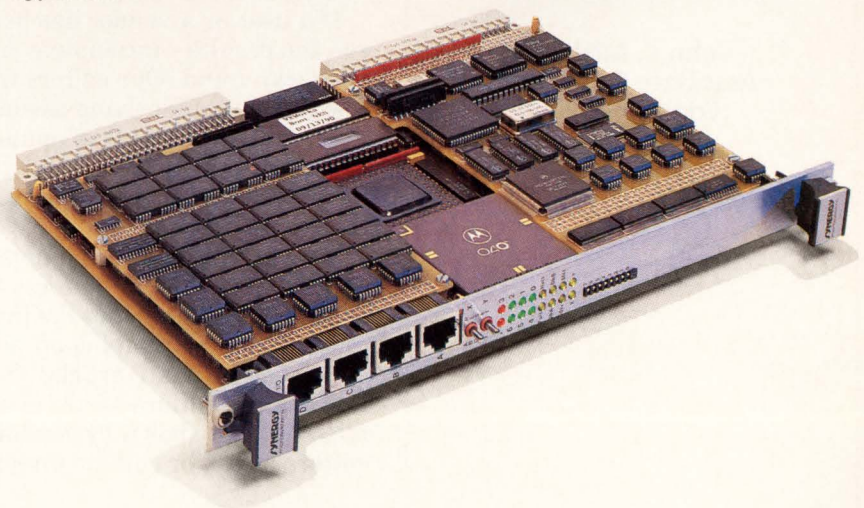
Software compatibility between Synergy SBCs means users have simple upgrades to the SV430 from our '020 and

'030 SBCs. Force offers compatibility only from the '030 level, and Motorola offers "upward migration"—a polite phrase that means rewriting your code.



Product Warranty

Synergy backs the reliability of its SBCs with a two year standard warranty. Force and Motorola only offer you one.



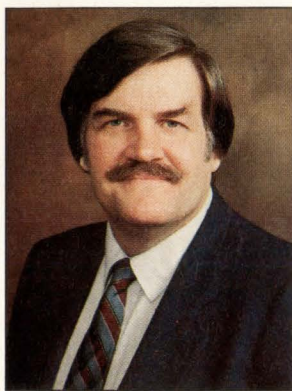
Synergy Microsystems, Inc.
179 Calle Magdalena
Encinitas, CA 92024
(619) 753-2191
FAX: 619-753-0903



CIRCLE NO. 8

Hard data isn't so hard to come by

If a user or vendor has benchmark data, we think you should see the results.



John C. Miklosz
Associate Publisher/
Editor-in-Chief

One characteristic of *Computer Design's* editorial approach—we even like to think it's unique—is that we try to go beyond the product specs, features and implementation-level details that are the stock and trade of most publications serving the electronics/computer design community. All of our senior technical editors have the mandate to provide perspective, analysis and comparative data on the technology and products they write about. Our goal is to make it a little easier for you to make decisions about your options and the trade-offs you have to make when choosing an ASIC implementation, a microprocessor or any other IC, a bus architecture, a CPU board, a CAE/CAD package, an operating system—the list goes on and on.

A key element in making any choice is having the data. In the electronics/computer world, that means benchmarks. Unfortunately, getting objective benchmarks is extremely difficult. While potential users of a particular product—a printed circuit board layout tool, for example—might benchmark several prospective candidates, that data might not be comprehensive and would usually remain within the company. Vendors, on the other hand, routinely benchmark their own and competitive products and make the results public. But the objectivity of these benchmarks is always open to question.

Because user benchmarks may not be comprehensive and vendor benchmarks may be tainted by self interest, the electronics/computer publications you receive—*Computer Design* included—have been loathe to use them. There's also the fear of offending present or potential advertisers if they don't do well in a benchmark. We think that's a mistake.

If a user or a vendor has benchmark data, we think you should see the results—incomplete or not, biased or not—and make up your own mind. Our editors will probe the benchmark data to uncover any underlying assumptions, discrepancies, biases or legitimate differences of opinion and point those out to you. Two of our editors, Tom Williams and Dave Wilson, have done just that in the Technology Updates section of this issue. And we're going to do more.

Whenever possible and appropriate, we will publish any and all benchmark data our editors can lay their hands on. Editors will work relevant benchmarks into our feature articles and use benchmark data as a jumping-off point for our shorter, news-oriented Technology Update articles. You can help us in this effort by making our editors aware of any benchmark results you've compiled or been shown by vendors or colleagues. Give any one of our editors a call, or call me directly.

RADISYS GIVES VME THE INSIDE ADVANTAGE

Integrating a PC with your VME system is a smart move. The "PC advantage" provides a superior human interface and access to the PC's huge base of system, application and development software.

The PC Advantage belongs inside your VME system. Not attached to it. By embedding a PC inside your VME card cage, instead of attaching it externally, you break through the inherent communications bottleneck that constricts system performance. You also eliminate the superfluous hardware and software needed to attach two system architectures.

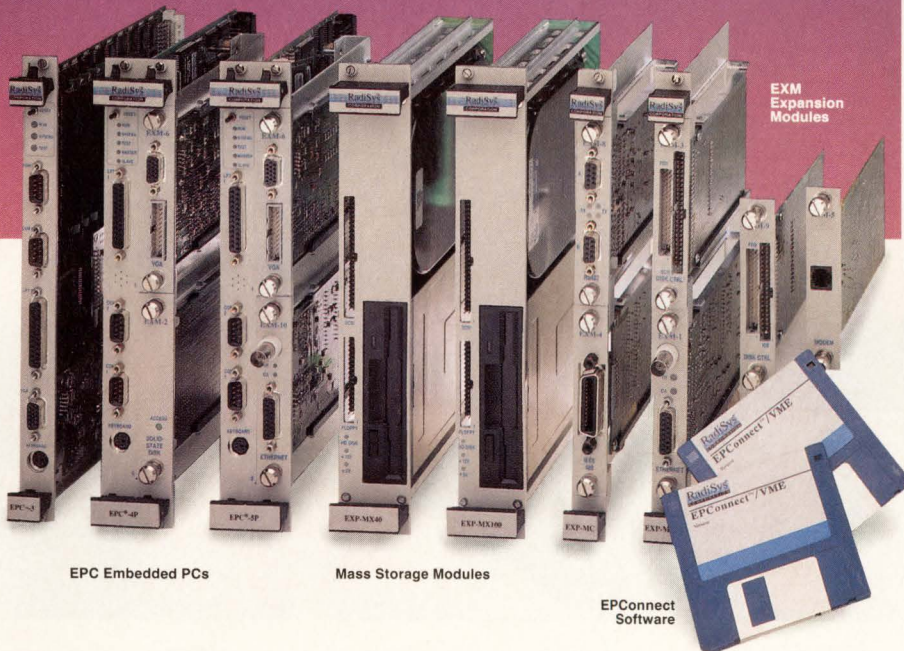
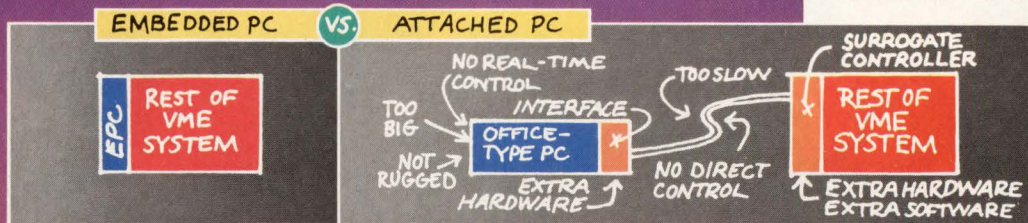
Only RadiSys EPC® Embedded PCs completely integrate the strengths of PC and VME. An EPC, with its exclusive EPConnect™ Software, is the only 386- or

486-based, PC-compatible computer with software that integrates the VMEbus into the DOS, Windows, UNIX and OS/2 environments. EPCs give your VME systems:

- **Highest system performance** from the real-time responsiveness of the direct 32-bit interface between the 386 or 486 and the VMEbus.
- **Improved system packaging** in 1/10th the volume, with integral VME ruggedness, and no bus link baggage.

And EPCs cost you less. EPC-based systems avoid the costly pitfalls of attached PC systems. No extra interfaces, cables, surrogate controllers, or the software to make them work.

Give your VME systems the EPC advantage. Call (800) 950-0044. We'll send all the details. No strings attached.



EPC Embedded PCs

Mass Storage Modules

EPConnect Software

EPC MODEL	EPC-1 (shipping since Aug '88)	EPC-3 (shipping since Aug '89)	EPC-4 (shipping since Mar '90)	EPC-5 (shipping since Oct '90)
Processor Modules:				
CPU	80386	80386SX	80386	80486
CPU Clock	16 or 20MHz	16MHz	25 MHz	25 or 33 MHz
DRAM	1 or 4 MBytes	1, 2 or 4 MBytes	4, 8 or 16MBytes	4, 8 or 16 MBytes
Graphics	EGA (640 x 350)	VGA (800 x 600)	VGA (800 x 600)	VGA (800 x 600)
Mass Storage Modules:				
Hard Disk Capacity	40 MBytes		40, 100 or 200 MBytes	
Floppy Drive Size/Cap.	3.5" / 1.44 MBytes		3.5" / 1.44 MBytes	
Expansion Capabilities:				
PC Add-in Cards	Yes		Yes	
EXMbus Expansion	N/A	EXM Expansion Modules:		
		EXM-1 Ethernet	EXM-5 Modem	EXM-9 IDE/Floppy Ctrl.
		EXM-2 Solid State Disk	EXM-6 VGA Graphics	EXM-10 Ethernet
		EXM-3 SCSI/Floppy Ctrl.	EXM-7 RS232 Serial I/O	EXM-11 Timer/Counter
		EXM-4 IEEE 488	EXM-8 RS422 Serial I/O	EXM-12 Prototyping Card
Software Support:	EPConnect development, run-time, and multiprocessing software package for DOS, Windows, UNIX, and OS/2			



THE INSIDE ADVANTAGE

RadiSys Corporation
19545 NW Von Neumann Dr.
Beaverton, OR 97006 USA
(800) 950-0044
(503) 690-1229
Fax (503) 690-1228

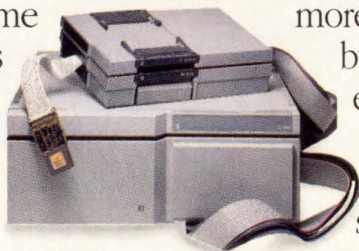
Copyright © 1989 RadiSys Corporation. All rights reserved. RadiSys and EPC are registered trademarks and EPConnect is a trademark of RadiSys Corporation. 386 and 486 are trademarks of Intel Corporation, OS/2 is a trademark of International Business Machines Corporation, UNIX is a trademark of American Telephone and Telegraph.

So would you like the number



Yes, it's true some design teams see us as the emergency number of development systems providers.

Many more, however, use Applied Microsystems



more productively by calling us in earlier—at the start of their embedded systems project.

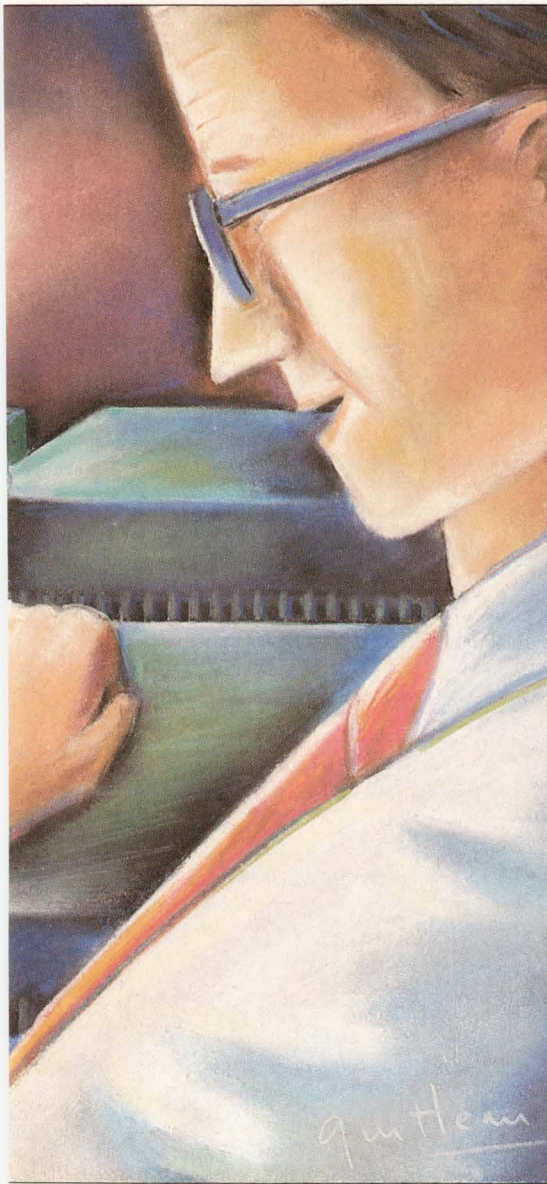
Out of our experience comes tools and support to help your design team work like a team.

Long before the sirens ever begin to sound.

Development systems for today's embedded systems.

It's getting much more complicated in there. Like, several megabytes of code

for Applied Microsystems?



in a 32-bit design. Which means more engineers to write it, often within very different, even mismatched environments.

Our modular development system architecture helps bring your design

together by integrating your computer environment with our high performance emulators, debuggers, simulators and compilers.

We even offer a networked system for Sun® setups. And a common interface for all our systems for easier 16- or 32-bit development.

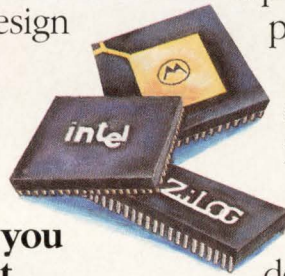
All so your design team can begin working like a real team.

We work with the processors you work with most.

Megahertz for megahertz, our tools run with the best, such as the powerful 68020/030 or i960™CA microprocessors.

In fact, we have alliances with Motorola®, Intel® and others. This enables us to deliver fully tested, compatible development systems sooner to support your processor's unique features.

Moreover, supporting your development efforts is our only business. So unlike others who just dabble in development, we have to be better at it.



Which may explain why companies have called upon us to set up over 15,000 development systems worldwide.

Call before your development days are numbered.

It's never too early to talk with us about your upcoming design projects.

In fact, you can start now by calling for our brochure on what you should expect from a development systems company (and can't afford not to get).

Just call 1-800-343-3659 (in Washington, 206-882-2000).

And of course, we'll be happy to take your emergency calls, too.



**Applied
Microsystems
Corporation**

Where it all comes together.

CIRCLE NO. 10

ASSOCIATE PUBLISHER/EDITOR-IN-CHIEF
John C. Miklosz (508) 392-2114

SENIOR EDITORS

Warren Andrews, *Computers and Subsystems*
(508) 283-2102
Barbara Tuck, *ASICs and ASIC Design Tools*
(516) 744-2984
Michael G. Donlin, *CAE/CAD Tools*
(508) 392-2123
Tom Williams, *Software and Development Tools*
(408) 335-5514
Dave Wilson, *Integrated Circuits*
(508) 392-2176

SECTION EDITOR

Jeffrey Child, *New Product Highlights*
(508) 392-2126

MANAGING EDITOR: John Donovan
(508) 392-2115

ASSISTANT MANAGING EDITOR:
Barbara-Ann Scofidio
(508) 392-2121

ASSISTANT EDITOR: Sue Cavallaro

PRESENTATION MANAGER: Richard D. Sarno

ASSISTANT PRESENTATION MANAGER:
Claire Coupal

EDITORIAL ASSISTANTS: Claire Ellis,
Terrie Robertson

ART DIRECTOR: Jan Horner

ILLUSTRATORS: Fred Lomas, Manuel King

COVER ART: Steve Fuller

AD TRAFFIC MANAGER: Betsy Anderson

CIRCULATION DIRECTOR: Robert P. Dromgoole

CIRCULATION MANAGER: George Andrew

PUBLISHER

David L. Allen (508) 392-2111

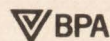
ASSOCIATE PUBLISHER/NATIONAL SALES MANAGER:

Tim L. Tobeck (516) 883-8815

PennWell
PUBLISHING COMPANY

Advanced Technology Group
L. John Ford, Senior Vice-President
Leslie P. Cypret, Vice-President, Administration
One Technology Park Drive
P.O. Box 990
Westford, MA 01886
Tel: (508) 692-0700
Fax: (508) 692-0525

Postmaster: Send change of address form 3579
to COMPUTER DESIGN Circulation Department,
Box 3466, Tulsa, OK 74101



LAN Magnetics and Filters

Solutions to the High Cost of Real Estate

ETHERNET 10Base-T and Token Ring 16 Mbps

- Miniaturization saves 40% on real estate
- Lowers production costs
- Designed to meet IEEE 802 performance standards
- Thru-hole and surface mount
- Discrete or integrated modules

Quality On The Leading Edge

4787 Cardin St., San Diego, CA 92111-1416
Tel: (619) 569-6577 • Fax: (619) 569-6073



CIRCLE NO. 11

SCSI INSTRUMENTS



ANCOT's SCSI instruments are powerful, easier to use, and cost less. Proven in use worldwide, Ancot's portable equipment travels from bench to field and back again without ever slowing down. They are time and labor saving instruments, for design, manufacturing, repairing, and inspection applications.

Call today for product data sheets, demo disc, or to make arrangements for a free evaluation unit in your facility.



[415] 322-5322

115 Constitution Drive
Menlo Park, CA 94025
Fax # 415 322-0455

CIRCLE NO. 12

REFLECTIONS OF QUALITY...

1.65 GB in a 5.25-inch Form Factor Available Now Is the New Hitachi DK516C-16 Winchester.

To back-up the famous Hitachi quality, the DK516 series drives are offered with a 150,000 hour MTBF and a 5-year warranty.

Edge-to-Edge Performance

The DK516C-16 uses Hitachi's advanced proprietary technology to deliver 1.65 GB of capacity and a fast 13.5 ms average access time.

Its SCSI interface provides a maximum data transfer rate of 5.0 Mbytes/sec (synchronous), with a 256 Kbyte data buffer and read look-ahead cache.

Or, if you have an ESDI application, look into Hitachi's new 1.54 GB DK516-15 with a 14 ms average seek time and a 2.75 MB/sec data transfer rate.

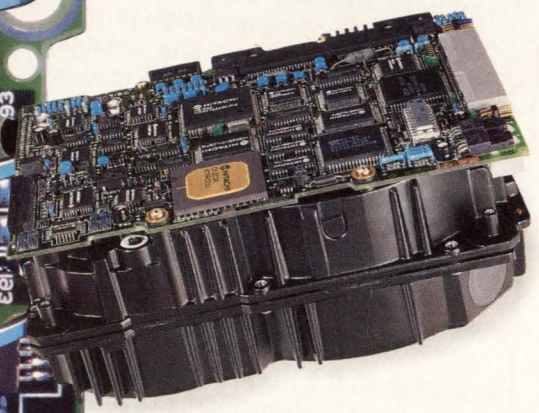
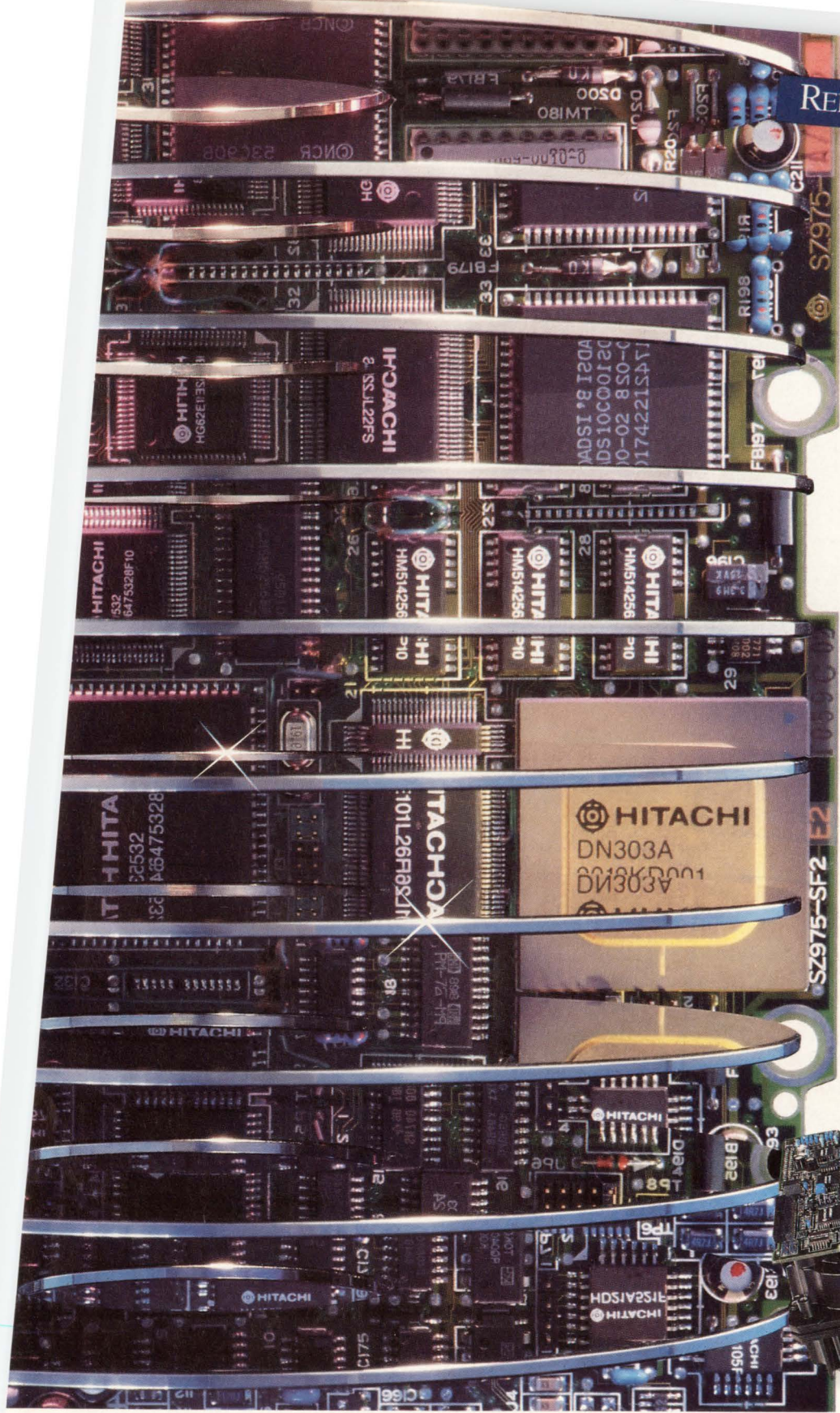
Edge-to-Edge Quality

Choose the DK516 and you get a drive backed by the quality and reliability of Hitachi—a \$44 billion company. Unlike other drive manufacturers, we design, build, and test all key components in-house.

If your new system design is leading the edge, then there's only one disk drive choice: the new DK516, from Hitachi.

For more information about the DK516, or any Hitachi disk drive, call 1-800-HITACHI.

Hitachi America, Ltd.
Computer Division, MS500
Hitachi Plaza
2000 Sierra Point Parkway
Brisbane, CA 94005-1819



The Leading Edge of Capacity

CONSAN 612-949-0053
(IA, IL, IN, KS, KY, MI, MN, MO, ND, NE, OH, Pittsburgh, PA, SD, WI)

GENTRY ASSOCIATES
800-877-2225 (AL, D.C., FL, GA, LA, MD, MS, NC, SC, TN, VA)

R SQUARED 800-777-3478
(AZ, CA, CO, NM, OR, UT, WA, WY)

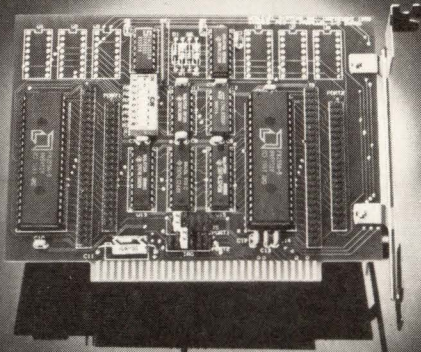
SIGNAL 800-228-8781
(CT, MA, ME, NH, RI, VT)

Authorized Distributors:

SPECIALIZED SYSTEMS
TECHNOLOGY 800-688-8993
(AR, LA, OK, TX)

CIRCLE NO. 13

PIO-48



- 48 DIGITAL I/O LINES FOR PC
- TWO PROGRAMMABLE 8255 I/O PORTS
- INTERFACE TWO 24 MODULE RELAY RACKS
- DRIVER SOFTWARE PROVIDED
- OTHER I/O PRODUCTS AVAILABLE
- DELIVERY FROM STOCK
- MADE IN USA



SEALEVEL SYSTEMS INC.
PO BOX 1808
EASLEY, SC 29641
[803] 855-1581

CIRCLE NO. 15

Sorry OrCAD Sorry Tango

The NEW **SCHEMA III 3.3** introduces an incremental compiling, unlimited size design processor, full network compatibility, auto parts creation, and much more, again keeping SCHEMA a step ahead in function and speed.

OrCAD introduced its "framework" in 1991. SCHEMA had it in 1987! Tango introduced wildcard library browse in 1991. SCHEMA had it in 1988!

SCHEMA III 3.3 leads the pack in features and performance, but not in price! Still only \$495 including the "framework" and FREE 1-800 support! Why wait for them? Call today for your free demo disk and see why SCHEMA is the professionals' choice.



(800) 553-9119

FAX (214) 783-9072

CIRCLE NO. 16

CALENDAR

CONFERENCES

May 12-15 CICC

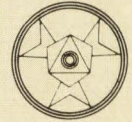
Town & Country Hotel, San Diego, CA. Global communications is the theme of the 13th annual Custom Integrated Circuits Conference. The show will offer education, technical and new product sessions, as well as exhibits from semiconductor manufacturers, software tool vendors and design houses. Information: Roberta Kaspar, Technical Program Coordinator, 1597 Ridge Rd W, Suite 101C, Rochester, NY 14615, (716) 865-7164.

Circle 366

May 20-23 Spring

Georgia World Congress Center, Atlanta, GA. Spring is a new event that includes Comdex and the debut of Windows World, featuring products, support and education on Windows computing. Spring's exhibits and conferences will focus on networked computing and multimedia. Information: The Interface Group, 300 First Ave, Needham, MA 02194-2722, (617) 449-6600, fax (617) 449-6953.

Circle 367



May 20-23 Midwest Electronics Expo/PCB Expo

Minneapolis Convention Center, Minneapolis, MN. The Midwest Electronics Expo and the PCB Expo will conduct a joint conference program this year. The show will feature 30 conference sessions and tutorials, with 10 devoted solely to printed circuit board issues. Information: Miller Freeman Expositions, 1050 Commonwealth Ave, Boston, MA 02215-1135, (800) 223-7126, fax (617) 232-0854.

Circle 368



June 10-13 Nepcon/East '91

Bayside Exposition Center, Boston, MA. This conference and exhibition will feature products and technologies for the design, fabrication, assembly, packaging, inspection, and test of printed circuits and electronic assemblies. The expected 16,000 attendees will find 375 exhibitors, 17 technical sessions, 7 workshops, and 9 professional advancement courses. Information: Cahners Exposition Group, Cahners Plaza, 1350 E Touhy Ave, PO Box 5060, Des Plaines, IL 60017-5060, (708) 299-9311, fax (708) 635-1571.

Circle 369



June 17-21 DAC

Moscone Center, San Francisco, CA. The 28th annual Design Automation Conference, geared toward electrical engineers, computer scientists and management, will offer technical programs, tutorials and vendor exhibits. Two new panels, "Global Strategies for Electronic Design" and "Implementing the Vision: Electronic Design in the 1990s," will target high-level management and project and group managers, respectively. Information: 28th Design Automation Conference, 7490 Clubhouse Rd, Suite 102, Boulder, CO 80301, (303) 530-4333, fax (303) 530-4334.

Circle 370



See Ya Later, OSCILLATOR!



*The ICS1394...the low cost,
space saving alternative to
multiple crystal oscillators!*

*Imagine...a single ICS1394
replaces every video crystal
oscillator on your board.*

*Consider...one ICS1394
costs about the same as just
one crystal oscillator*

*Then rely on the
ICS1394... the proven video
dot clock generator that has
become the industry
standard.*

Whether you use the extra space to put more new features on board or pass the dramatic cost savings on to your customers, the ICS1394 gives you a competitive edge in the marketplace.

The ICS1394 Dot Clock Generator was developed by ICS for high performance video display systems. Since it's capable of generating up to 32 frequencies, it can easily replace the 3 to 8 crystal oscillators usually found on most video boards—and it has standard frequency patterns for most popular VGA chipsets. The ICS1394 is available in a 20 pin DIP or an S.O. surface mount package.

The best part is, the ICS1394 **works** and has been working reliably in high performance video systems of leading manufacturers around the world. Now you have a choice! Control cost and space with the ICS1394 alternative.

For technical literature, samples, or a sales rep nearest you, contact ICS today, toll free 1-800-220-3366.



Integrated Circuit Systems, Inc.
Where ASIC experience sets new standards

2626 Van Buren Avenue, P. O. Box 968 • Valley Forge, PA 19482-0968
Tel: (215) 666-1900 • FAX: (215) 666-1099

CIRCLE NO. 17

Fast Things Fast.

- 15 ns 256K SRAMs.
- 20 ns 1MEG SRAMs.
- 20 ns 4MEG SRAMs.

Right parts. Right speeds. Right now.



San Jose, California. And watch for our Processor Specific Memories to support Intel 486, MIPS R4000 and SPARC architectures—coming soon.

Discover the service designed to eliminate wait-states—for you and your processor. Call Paradigm's Express Chip hotline today.

To get your next design off to a fast start, get the fast parts you need through Paradigm's exclusive Express Chip service. Every SRAM is fabricated in our own facility in



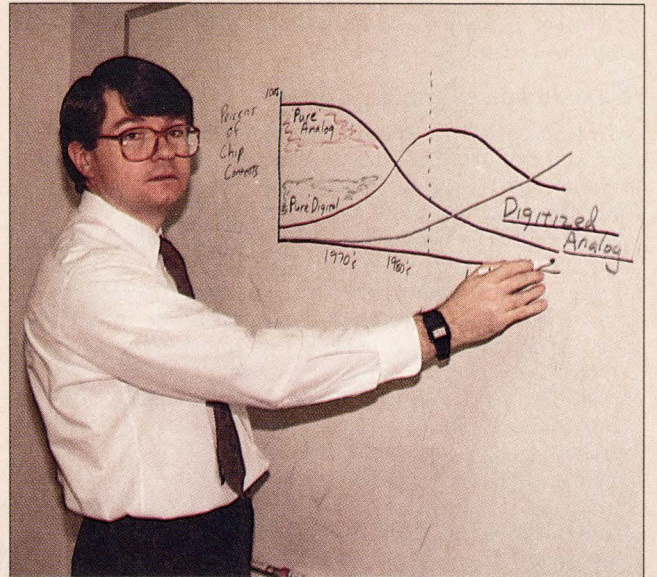
256K Family	
PDM 41256	32K x 8-28 lead DIP, SOJ, Cerpack, LCC
PDM 41258	64K x 4-24 lead DIP, SOJ, LCC
PDM 41298	64K x 4 with OE-28 lead DIP, SOJ
PDM 41251/2	64K x 4 with sep I/O-28 lead DIP, SOJ, LCC
PDM 41257	256K x 1-24 lead DIP, SOJ, LCC
1 MEG Family	
PDM 41024	128K x 8-32 lead DIPs, SOJ, Cerpack, 450 x 550 LCC
PDM 41028	256K x 4-28 lead DIP, SOJ, LCC
PDM 41022	256K x 4 with sep I/O-32 lead DIP, SOJ, LCC
PDM 41027	1024K x 1-28 lead DIP, SOJ, LCC
4 MEG Family	
PDM 4M096	512K x 8-32 lead DIP, Module



Catch the Expresssm 1-800-767-4530

PARADIGM TECHNOLOGY, INC. 71 Vista Montana, San Jose, California 95134 (408) 954-0500 FAX (408) 954-8913

G. Dan Hutcheson on: Mixed-signal technology



The mixed-signal IC is an emerging new technology that's easy to overlook because on the surface it appears to be no more than a niche application. If the current trends hold true, however, mixed-signal ICs will be as important to computer designers in the '90s as ASICs were in the '80s. But like any new technology generation, mixed-signal requires an entirely new way of thinking.

One reason why it's easy to overlook mixed-signal solutions is that in the '80s the technology earned a reputation for being difficult to design. Adding analog, which is also difficult to work with, only made design more tedious and complex. But by bringing the power of digital VLSI to analog, it has been possible to introduce mixed-signal devices with integration scales and complexities that were only dreamed about a few short years ago. They offer digital's ease of use with analog's functionality. This new wave of devices is breathing life into new, unique designs that have until now been impossible for all but the most costly design targets.

Mixed-signal ICs follow a pattern in semiconductor technology. Every decade a new technology emerges that dramatically alters how systems are designed. In the 1960s, SSI/MSI IC logic blocks were the foundation for mainframe computers. Then in the 1970s, LSI microprocessors and memories brought forth the first powerful minicomputers, electronic calculators and video games. In the 1980s, VLSI ASICs let designers glue large blocks of processors, logic and memory together to bring mainframe computing power to desktops and laptops. ASIC design methods also allowed chips to give workstations, personal computers and video games powerful graphics capability.

Each of these technology generations had several common characteristics. They typically gained momentum in the beginning of the decade; they had a new semiconductor technology as their key driver; they made use of the latest scale of integration; they integrated previously separate functions; and they let computer designers differentiate their products in new ways. Mixed-signal is the only technology avail-

able today that follows this pattern. Also, mixed-signal is difficult to clone, which protects developers of value-added systems.

Automation brought to bear

Prior to the '80s, chip and board designs were laid out by hand. Designers were faced with the difficult task of keeping both the electrical design and its physical layout in order. There was a natural split between the two industries.

With the development of ASICs, designers had to integrate the printed circuit design layer with the silicon design layer. A design could no longer be conceptualized as a collection of catalog chips soldered to a board. What had previously been a board of chips became merged into functional logic blocks that were glued together in silicon. The barrier between what was on the board and what was on silicon became fuzzy. The design task would have been virtually impossible had EDA tools not been developed. And not only did EDA tools make it possible to manage these large designs, they also made it possible to build a business in ASICs.

In the early '80s it was easy to think of both EDA and ASICs as separate trends in technology. ASICs were semiconductors, which were historically a commodity product. So semiconductor companies could focus on chip manufacturing and ignore how ASIC methodologies would affect design—and ultimately the market.

Also, circuit design and chip design had been separated between the systems level and the silicon level. So chip companies could confuse, or ignore, what was going on at the silicon level with the end objective, which was to obtain a working design. Many of the early leaders, such as Interdesign, made the error of believing that the responsibility for system design would continue to rest with the systems houses and unwittingly placed the burden of silicon design on the systems designer. Those that recognized the link between ASICs and EDA tools embraced both methods early on to simplify the systems designer's task. Virtually every leader in ASICs today attributes

its early success to making EDA software a strategic component of its business.

■ Evolution of mixed-signal

Mixed-signal faces challenges today much like ASICs did last decade. The conventional view of many market researchers is one of those challenges. According to this viewpoint, future mixed-signal devices will have an ever-increasing analog content. Current analog content rates are typically estimated at 5 to 10 percent, and some industry experts project a cross-over into the 50 percent region during the mid-1990s (see "Conventional Wisdom," on facing page).

There are many reasons why this view is not practical. The first is a lack of good mixed-signal simulation tools. Without strong simulation tools, designs with high analog-to-digital content ratios need significant amounts of hand crafting and the intuitive knowledge of an experienced analog designer. Testing mixed-signal devices with high analog-to-digital contents is another area of difficulty. Consequently, designing mixed-signal devices with a high analog and digital content is both expensive and time-consuming.

Second, the pool of analog designers has been shrinking over the years, since analog has not been a popular area in which to work. Additionally, the long market life of most analog parts has meant that relatively few designers have been needed to service this market. The few designers that have remained in analog are the pioneers, and many of them are nearing retirement.

The conventional view that future mixed-signal devices will have ever-increasing analog content has its roots in the earliest announcements of digital applications where microcontrollers were being designed with analog I/O; however, this trend hasn't continued. In contrast, analog circuits have had increasing digital content. Analog Devices has reported that a 12-bit digital-to-analog converter of the early '80s had 58 percent analog content with a mere 475 components. A state-of-the-art Delta Sigma A-D converter today has a 2 percent analog content with a total of 100,000 components. Consequently, the cross-over point for analog and digital actually occurred in the mid-1980s (see "The Facts," on facing page).

Additionally, mixed-signal ICs already account for 8.5 percent of the total IC market. Sales of mixed-signal ICs amounted to \$4.4 billion in 1990. This included \$0.9 billion in communications circuits, \$0.7 billion in converters, \$1.1 billion in interface circuits, \$0.8 billion in integrated signal-processing circuits, and \$0.9 million in other mixed-signal circuits. Another indicator of this technology's importance is that the market leaders in mixed-signal are all significant overall players in the semiconductor market. They include National Semiconductor, Texas Instruments, Analog Devices, Motorola, and Harris Semiconductor.

■ Emergence of digitized analog

A problem with the conventional view is that it is grounded in the physical attributes of the silicon, rather

than the object: the signal. In silicon, according to this view, analog is analog and digital is digital. So mixed-signal must be the simple placement of the two on silicon.

The fact is that this is not the case. Thanks to the digital VLSI revolution of the '80s, it is now relatively easy to design and simulate digital circuits with hundreds of thousands gates and to implement analog functions in digital circuits. These circuits are a paradox because they're not analog, but they're also not digital in a pure sense. Pure digital is a control function, where analog is an information-bearing signal.

Consequently, a definition is needed to describe this newly emerging circuit. Much of the ambiguity in mixed-signal has occurred because it is so immensely tedious and complex. Some mixed-signal applications can't logically be called digital. One example is digital signal processing. The central element of DSP consists of totally digital microcontrollers and multipliers. Still, they are digital elements that are designed for exclusive use in analog applications. Another example is LAN transceivers and subscriber line interface circuits. These circuits are highly digital, but are used for analog applications.

VLSI Research has coined the term "digitized analog" to define these circuits. They are ICs whose function is to aid in the mapping of analog system activities into digital system activities and vice versa. This includes transformations of digital signals into other digital signals when the end objective is to achieve a digitized analog function whose inverse mapping into an analog function will eventually occur.

■ Digitized analog is unique

It's easy to think of digitized analog as merely converted analog with DSP; however, it is much more. These are just the transmission and engine of a totally new technology. Together, they result in totally new activities that employ digital circuits instead of analog. Digitized analog is the representation of analog signals in digital form. They can be filtered, analyzed and changed with software. Moreover, this can be done on the fly. This enables new functions which couldn't have existed alone in either domain.

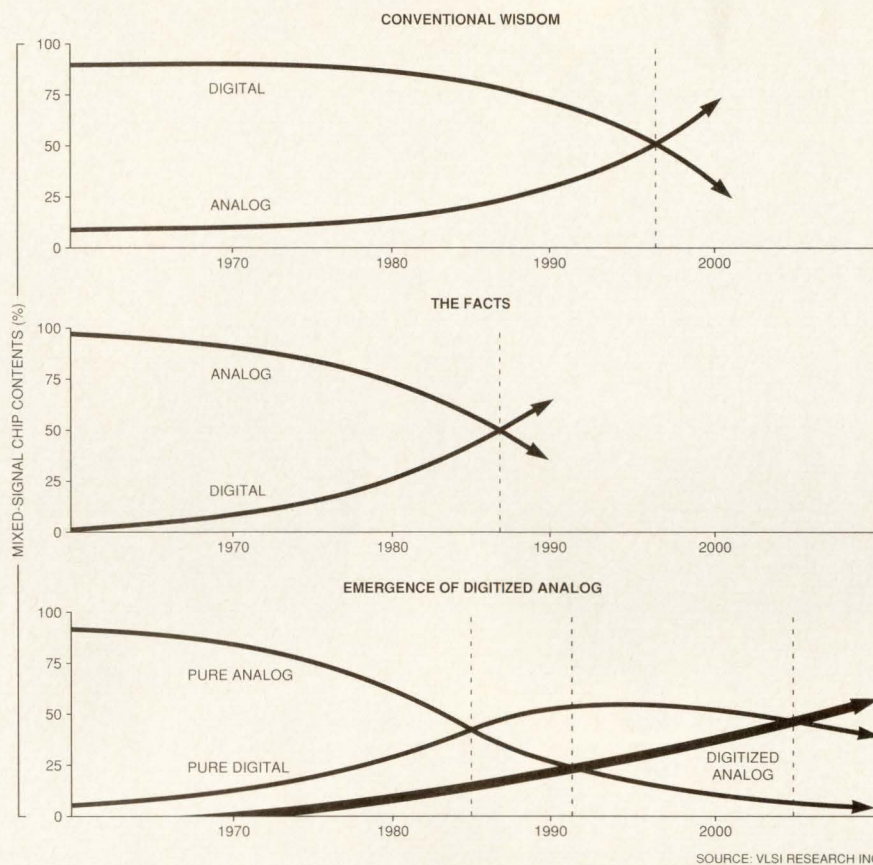
Some examples of digitized analog implementations in systems include the Patriot missile system, compact disk players, digital audio tape, laser printers, copiers, and ISDN. Examples of assemblies include signal generators, automatic braking systems and fuel injection. At the component level, examples range from a simple phase-locked loop to delta-sigma converters, image-compression circuits and image-transmission circuits.

These new types of circuits are evidence that mixed-signal is allowing designs that previously were not possible. Digitized analog nullifies the key criticism made against mixed-signal: that it is too difficult to design. Analog circuits can be designed with digital functional blocks. This eliminates the many parameters that must be tracked for each cell in a pure analog

A new generation of mixed-signal devices have emerged with integration scales and complexities that were only dreamed about a few short years ago.



PATTERNS OF CHANGE IN MIXED-SIGNAL ICs



While conventional wisdom has it that the crossover point for analog and digital will occur in the mid-1990s (top), some industry experts feel that it actually already occurred in the mid-1980s (middle). The resulting technology is digitized analog (bottom), or ICs that aid in the mapping of analog system activities into digital system activities and vice versa. According to some experts, digitized analog is the next wave in semiconductor technology.

circuit and, in turn, makes analog design simpler.

Analysis of the interaction of the analog cells on the circuit is also simplified. Digitized analog circuits are a mathematical representation of what is normally represented with materials properties in pure analog. Consequently, they can be designed at the signal level without any concern about the enormous complexities of materials properties at the silicon level.

As a result, many other design barriers are broken down. Existing design tools can be used since the design is digital. Moreover, they can be developed in an evolutionary manner to meet the needs of digitized analog design. After all, Spice will be around for a long time for the purely analog portion. It won't be necessary to wait for the next-generation mixed-signal design tool. And the same will hold true for testing. Also, the aging pool of analog designers will give way to new breed of designers building new digitized circuits.

■ Transparency a benefit

Digitized analog won't merely push converters out to the periphery of the circuit; it will find its place right in the heart of the chip. In that way, it will be a mapping technique, rather than a conversion technique. The mapping ability of mixed-signal can make

computers transparent to the user. In many cases with mixed-signal, users never need know that they are operating computers.

Take the modern auto, for example, with ABS braking, electronic fuel injection and engine control. Some cars already have several Mips of computing power. In the future, automobiles will also include smart power, noise cancellation and suspension control. All of this is transparent to users. Mixed-signal also has found its way into color pixelation, image synthesis, disk drives, loud speakers, and displays, to name a few technologies.

This will have significant ramifications for the system designer because modern mixed-signal system development is heavily steeped in converters, DSP, software, and standards development. But while mixed-signal simplifies the design problem, it does not eliminate it; design and simulation tools will still have to evolve.

Mixed-signal offers myriad new benefits and frees designers to think in completely new ways. The challenge, as with any new technology, will be in learning how to master it.

G. Dan Hutcheson is president of VLSI Research (San Jose, CA).



H4C
SERIES

The Best of Two Worlds in One New System Solution.

Motorola's H4C Series™ combines unprecedented speed/power and density with unique system-level design implementation in one CMOS Array.

If you want the density advantages of cell-based architectures plus the economy and cycle time of high-performance custom gate arrays, you've just found the best of two worlds in one system solution. It's Motorola's new generation state-of-the-art CMOS ASIC technology, the H4C Series™ of Customer-Defined Arrays.™

The new fabrication process of the H4C Series provides 180 picosecond performance in densities typically ranging from 19,000 up to 222,000 usable gates, and supports the speed requirements of 60 MHz processors with a power dissipation of only 3μW/Gate/MHz.

System-Level Design

One of the H4C Series' system-level design features is the Customer Defined Architecture. CDA enables versatile, efficient system-level design in which large, fully-diffused architectural blocks like RAM, and in the future, microprocessors and arithmetic functions, are embedded in the Array. High-speed, user-configurable RAMs are structured to easily integrate with user-defined BIST circuitry. Optimized SRAM is available in several hundred thousand single and dual port configurations of up to 256K bits.

Additionally, Motorola's proprietary digital PLL clock skew control

macros facilitate high-speed inter-chip synchronous communication. And, a variety of design-for-test features, including JTAG in the I/O periphery and ESSD/LSSD scan macros, is included.

System Solutions

- Tight Process Distribution
- Digital PLL Clock-Skew Mgt.
- Design-For-Test Scan Macros
- JTAG (IEEE 1149.1) Boundary Scan
- Embedded Megafunction Blocks
- Clock Tree Synthesis
- User-Defined Memorist™ SRAM Compiler

The H4C Series meets the challenges of the most demanding applications by combining advanced sub-micron technology with Motorola's unique battery of system-level design solutions. It's the best of two worlds in one system solution. And it's available only from Motorola.

Array	Available Gates	Usable Gates (70%)	I/O Wirebond / Tab
H4C027	27,000	19,000	160/188
H4C035	35,000	24,500	176/208
H4C057*	57,368	40,000	216/256
H4C086	86,000	60,000	260/304
H4C123*	123,136	86,000	340/360
H4C161	161,000	113,000	344/404
H4C195*	195,452	136,800	376/444
H4C318	318,000	222,500	464/556

*Now available. Other Series devices planned for future announcement.

H4C SERIES

What brings all these system design features to your fingertips is our work-station based Open Architecture CAD System™ which creates an environment where leading edge design tools work together in harmony.



MOTOROLA

MOTOROLA and are registered trademarks of Motorola Inc.

To: Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036
Please send me a copy of the Motorola Semiconductor Technical Data Booklet on the H4C Series CMOS Arrays and the CDA Architecture

#89CD050091



Name _____
Title _____
Company _____
Address _____
City _____
State _____ Zip _____
Call me (_____) _____

INTEGRATED CIRCUITS

Are secondary caches for the 486 worth the money?

Dave Wilson, Senior Editor

If the 386 needed a second-level cache controller, does that necessarily mean the 486 will? Some say yes, some say no.

The 486 chip from Intel (Santa Clara, CA) has 8 kbytes of on-chip cache. If that isn't enough, designers can choose from a host of peripheral cache controllers, both write-through and write-back, that will let them build second-level caches to improve cache hit rates. But some question whether the peripheral cache controllers are worth the money.

With each new member of the 486 processor family, they say, Intel adds yet another price/performance point to its PC processor family that makes it less likely that designers would add much extra value to their products through secondary caching techniques. "Intel's pricing on 486 processors is coming down quickly. Clearly, the 25-MHz 486 is priced to replace the 33-MHz 386, moving the 486 into the commodity market where motherboard cost is the most-important factor," says Patrick Lee, vice-president of marketing and product engineering at Pioneer Computer (Fremont, CA), a manufacturer of 486 PC motherboards.

Performance a moot point

Derivatives of the 486, such as the 486SX, will help. By Intel's reckoning, the 20-MHz 486SX hits a performance point between the 33-MHz 386DX and the 33-MHz 486DX (see figure, above right). Hence, what advantage may have been gained in the past by accelerating the performance of the 33-MHz 386DX through caching may now be moot. Buying a 20-MHz 486SX without cache would appear to be a more cost-effective solution. According to Intel, the 486SX at 20 MHz will outperform a 33-MHz 386 even when the 386 has a second-level cache.

Looking at cache performance alone clearly is not the answer, especially for EISA-based systems that may support second-level caches in addition to other EISA bus

masters that may also access DRAM memory. "Boosting the performance of the cache isn't the only way to enhance system performance," says Jack Lii, vice-president of engineering at Cache Computers (Fremont, CA), a manufacturer of 486 PC motherboards. "You have to look at how to balance system performance as well."

Intel's 486 architecture is the key to its performance gains over the 386, as demonstrated by the ability of an uncached, 20-MHz 486 system to outperform a cached, 33-MHz 386 system on integer benchmarks.

20-MHz UNIX PERFORMANCE	33-MHz 386 DX	20-MHz 486 SX
SPEC INTEGER	7.7	10.2
DHRYSTONES V1.1 (VAX MIPS)	11.4	16.5
DHRYSTONES V1.1	19.9K	28.9K
DHRYSTONES V2.1	18.7K	26.2K
STANFORD INTEGER SUITE (VAX MIPS)	7.9	11.6

Because the 8-kbyte cache already on the 486 chip uses a write-through technique, the number of write bus cycles on the 486 bus increases dramatically. Both Intel and Mosel (Sunnyvale, CA) have contrasted the bus cycle mix for an application running on the 386DX with the same application running on the 486 and found that the number of reads is dramatically lower because most reads are already well cached. It appears, then, that optimizing the memory subsystem for consecutive write cycles is the way to go.

The crucial issue might instead be how well write cycle memory optimization can be performed. Perhaps

one way to find out would be to build a processor module with an added 256-kbyte, 32-byte line, 1-line/sector write-back cache, and to measure the bus traffic on the DRAM side of the module. In that case, the read/write prefetch mix might end up as shown in the bottom figure. Here, of the total cycles performed by the processor, the majority of the bus traffic external to the module is spent doing prefetch, and bus cycle time is clearly reduced.

Assuming that Intel's mix is right, write cycle optimization appears to be key. And write-back caching, rather than write-through caching,

would appear to be the best route to take with high-end 486 motherboard designs.

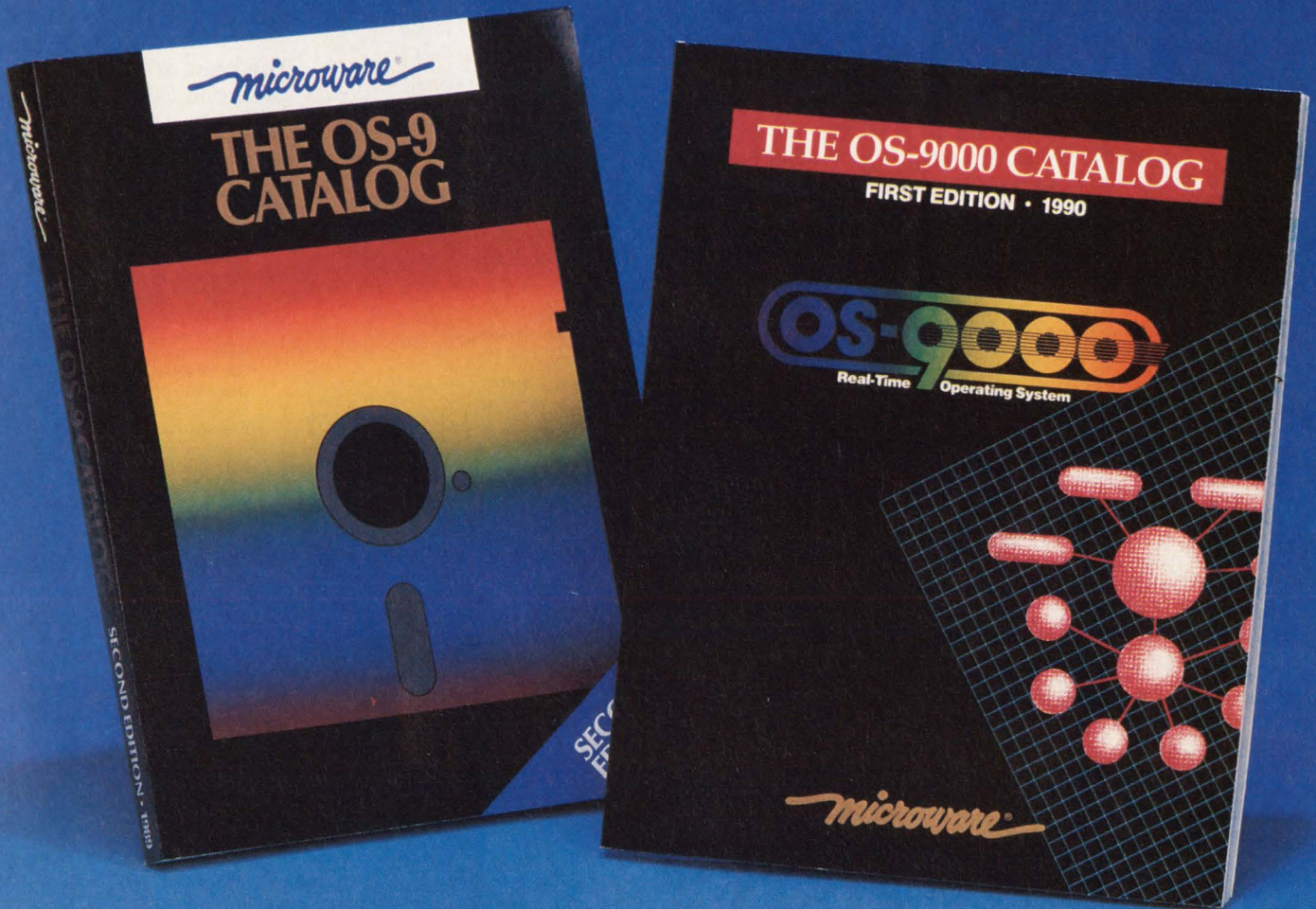
Along those lines, Mosel has recently introduced its single-chip write-back cache controller, the MS441. When accompanied by the company's own MS443 dual-port burst memory, the controller can be used as a 64-kbyte two-way set-associative second-level cache subsystem in either 386 or 486 systems. The chip design uses dual concurrent 386/486 bus controllers to manage the data path from the CPU to the cache and from the cache to the system.

When a write hit occurs, the cache

OS	READS	WRITES	PREFETCH	SECOND-LEVEL CACHE HIT RATE
UNIX (avg)	25%	14%	61%	97%
DOS (avg)	29%	18%	53%	99%

Estimates provided by industry sources of the performance achieved by a 486 with a 256-kbyte, 32-byte line, 1-line/sector write-back cache show that write bus cycle mix can be reduced significantly.

We wrote the books on real-time.



When it comes to real-time system software, Microware Systems Corporation leads the way. Now, we offer two books that provide you with complete real-time solutions — the OS-9 and OS-9000 Catalogs.

Microware offers the broadest range of real-time solutions in the industry. Data sheets and flyers just weren't enough to tell our story, so we wrote these books to tell you about our real-time operating systems. These catalogs are chock-full of more than 330 pages of useful information about our operating systems including networking, graphics, language compilers and productivity tools.

OS-9 is the world's leading real-time operating system for 680X0-based systems. OS-9 has been designed into thousands of embedded applications from industrial automation to consumer electronics.

OS-9000 is a portable real-time operating system written in C for advanced CISC and RISC processors. The ability to port OS-9000 to various hardware platforms "future-proofs" your real-time software investment through the 1990s.

Put the world's real-time leader to work for you today.

For Your Free Catalogs, Call
1-800-475-9000
In California, call (408) 980-0201

microware[®]

MICROWARE SYSTEMS CORPORATION

1900 N.W. 114th Street • Des Moines, Iowa 50322
Phone: (515) 224-1929 • Fax: (515) 224-1352

Microware is a registered trademark of Microware Systems Corporation. OS-9 and OS-9000 are trademarks of Microware Systems Corporation. All other brand or product names are trademarks or registered trademarks of their respective holders.

MORE CHOICES • MORE OPTIONS • TOTAL SUPPORT

CIRCLE NO. 20

INTEGRATED CIRCUITS

data array is simply updated, without initiating any system cycles. On a read or write miss, it gets more complex. Either a read or write miss will generate a system fetch that brings new data into the cache, replacing older data in the cache. However, the data that's replaced may be dirty, having been updated in cache since it was loaded from memory. This would require a write-back cycle to system memory to update its version of the data. In traditional single-ported write-back caches, this causes a penalty since the system read to fill the cache with new data must wait until the write-back cycle is completed. In the 443, however, hidden write-back cycles permit a background write back while read and write cache hits continue uninterrupted.

A custom design

Perhaps the most impressive point about the chip, according to Lii, is that the dual concurrent bus controller will support the 486 dual-port burst cache memory. On the other hand, he says, the Mosel dual-port SRAM is a single-source solution

and only works with that company's cache controller. He also believes that the 64 kbytes of external cache provided by the Mosel chip is not enough for the 486. As a result, Lii has elected to design his own ASIC cache controller for the company's latest project, a 486-based EISA motherboard. He feels that he can gain more in performance by implementing his own algorithm. "And it will cost less than an off-the-shelf part," he adds.

In the custom design, Lii plans to combine a write-back cache controller with a write buffer as well as a dual-port DRAM controller—all in a single chip. "Our goal is to break through the cache memory bottleneck and at the same time break through the DRAM bottleneck in the EISA system arbitration," says Lii.

Normally, in an EISA system, if the 486 wants to access DRAM and the DRAM is not dual-ported, the processor must go through EISA bus arbitration to obtain DRAM ownership before accessing the DRAM. Lii feels that by implementing a dual-port DRAM cache controller he can reduce that bus arbitration cycle

The best address for Siemens Semiconductors:

- (A) **Wien**
Tel. (02 22) 71711-5661
- (AUS) **Melbourne, Vic. 3121**
Tel. (03) 420 7111
- (B) **Bruxelles**
Tel. (02) 536-2111
- (BR) **São Paulo-SP**
Tel. (011) 833-2211
- (CAN) **Mississauga L5T1P2**
Tel. (416) 564-1995
- (CH) **Zürich**
Tel. (01) 495-3111
- (D) **Berlin 10**
Tel. (030) 3993-0
- Düsseldorf 1**
Tel. (0211) 399-0
- Frankfurt 1**
Tel. (069) 797-0
- Hamburg 1**
Tel. (040) 2889-0
- Hannover 81**
Tel. (0511) 877-0
- München 80**
Tel. (089) 9221-4391/4138
- Nürnberg 1**
Tel. (0911) 654-0
- Stuttgart 1**
Tel. (0711) 2076-0
- (DK) **Ballerup**
Tel. (44) 7744 77
- (E) **Madrid**
Tel. (01) 555 4062
- (F) **Paris**
Tel. (1) 4922-3810
- (GB) **Sunbury on Thames**
Tel. (0932) 752615
- (GR) **Amaroussio/Athen**
Tel. (01) 6864-111
- (HK) **Hongkong**
Tel. 5-8330222
- (I) **Milano**
Tel. (02) 6766-4241
- (IND) **Bombay 400018**
Tel. 4938786
- (IRL) **Dublin**
Tel. (01) 302855
- (J) **Tokyo 100**
Tel. (03) 201-2401
- (N) **Oslo 5**
Tel. (02) 633000
- (NL) **Den Haag**
Tel. (070) 3333333
- (P) **Alfragide**
Tel. (01) 4183311
- (RA) **Buenos Aires**
Tel. (01) 300411
- (RC) **Taipei**
Tel. (02) 5234700
- (RO) **Seoul**
Tel. (02) 275-6111
- (S) **Kista**
Tel. (08) 7033500
- (SF) **Helsinki**
Tel. (9) 051051
- (SJP) **Singapore 0513**
Tel. 7760044
- (TR) **Istanbul**
Tel. (01) 1510900
- (USA) **Iselin**
Tel. (201) 906-4300 (Discrete)
- Santa Clara**
Tel. (408) 980-4500 (ICs)
- Cupertino**
Tel. (408) 725-7910 (Opto)
- (ZA) **Johannesburg**
Tel. (011) 407-4111

Our Lists Are No Good (Unless You Use Them!)

In direct mail marketing, testing is the name of the game. PennWell's Computer Design list is worth a test. Use a sampling of our list for as little as \$475. It's a small price to pay when thousands of dollars are at stake.

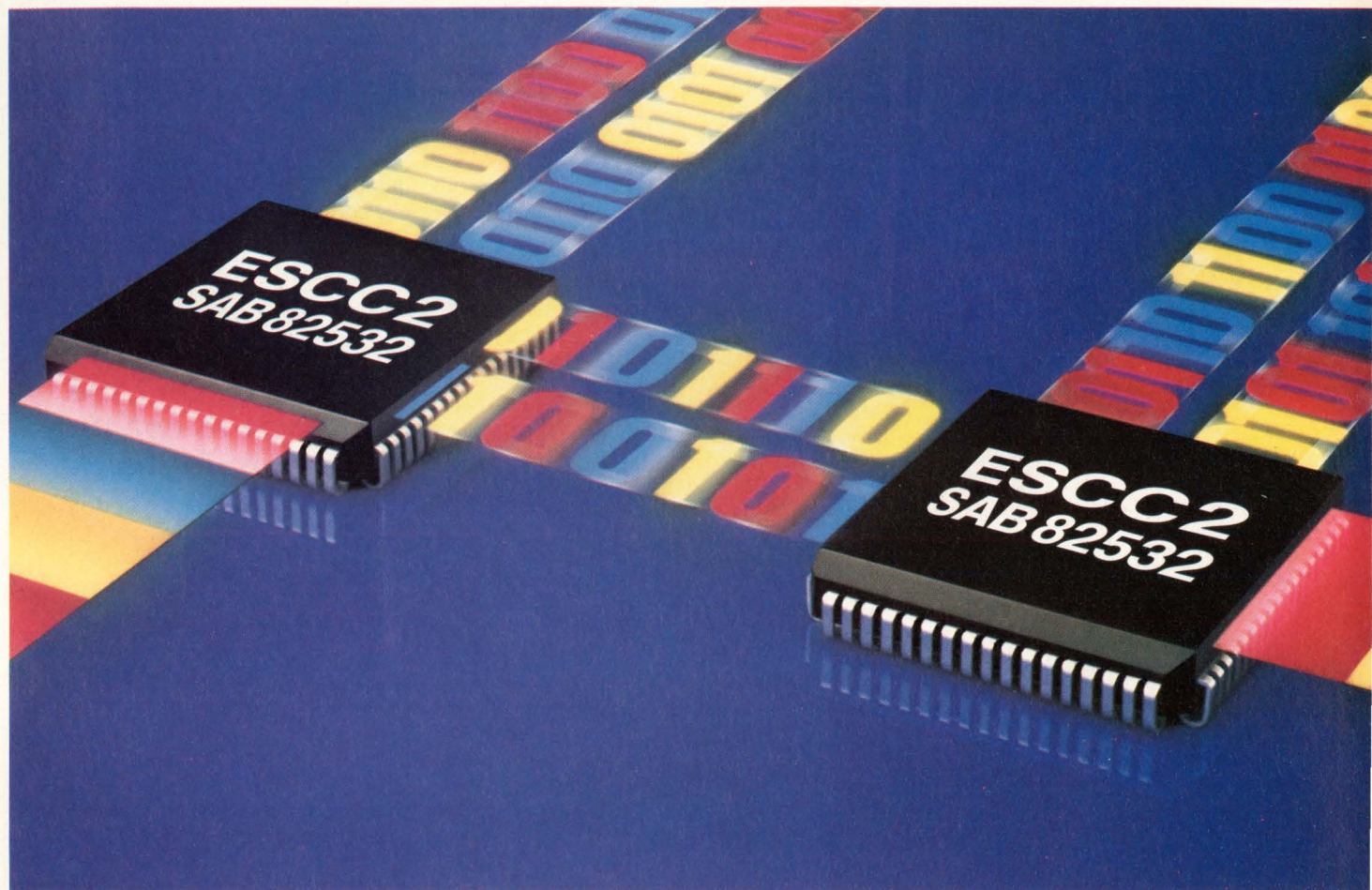
PennWell
Lists | ADVANCED
TECHNOLOGY
GROUP

Names you can count on.

Call 1-800-962-4669

Ask Deanna Rebro for good names
1421 South Sheridan • Tulsa, Oklahoma 74112

SIEMENS

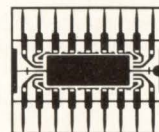


Communications Genius

With the development of the new Enhanced Serial Communication Controller (ESCC2), Siemens has demonstrated a new genius in high-speed multi-protocolling. The ESCC2 (SAB 82532) offers an extraordinary range of protocol options at a high-speed transfer rate of up to 10 Mbit/sec in synchronous mode. Supporting X.25 LAPB, ISDN, LAPD, HDLC, SDLC, and both ASYNC and BISYNC, the ESCC2 offers outstanding capabilities for a wide variety of applications. And it is as adaptable as it is powerful. The ESCC2's flexible 8/16-bit bus interface allows it to easily adapt to either Intel or Motorola microprocessors. Plus, it provides direct 8/16-bit accessi-

bility to all registers, as well as DMA and both vectored and non-vectored interrupt modes. This ensures efficient data transfer to and from host system memory, for fast, accurate and reliable multi-protocolling. For superior performance and flexibility, the ESCC2 features clock recovery up to 4 Mbit/sec, storage capability of 64 bytes in each of its four on-chip FIFOs and four encoding schemes: NRZ, NRZI, FMx and Manchester. In addition, it offers user-programmable features such as 16/32-bit CRC, time slot assignment, and an 8-bit parallel port. The result is an excellent CMOS device with only 40 mW power consumption for all kinds of multi-protocol applications.

For more information on the ESCC2, or to find out how you can receive your inexpensive PC-based evaluation kit (EASY 532), call 800-456-9229, or write:
Siemens Components, Inc.
2191 Laurelwood Road
Santa Clara, CA 95054-1514
And put the communications genius of Siemens to work for you.



**Siemens
World Wide
Market Smart**

CIRCLE NO. 21

INTEGRATED CIRCUITS

time, specified at 8 ms.

For its initial foray into the 486 ISA market, Cache Computers had chosen a second-level write-back cache controller chip from UMC (Santa Clara, CA). "Using the UMC chip we found that less than 2 per-

cent of the time the processor was going out onto the bus to write to the DRAM," says Lii. Read hit rate on the board, he claims, is running nearly 99 percent. For a write hit, it's around 96 percent.

Mylex (Fremont, CA) is another

vendor that, like Cache Computer, believes the Mosel chip was a less-than-adequate solution: in its own EISA 33-MHz 486 motherboard, Mylex has elected to use 128 kbytes of write-back cache. Pioneer's Lee says he would consider the Mosel part as a contender for his next-generation design, along with another controller from Opti (Santa Clara, CA). The Opti chip is part of a two-chip set that includes a bus controller peripheral chip. It integrates not only the cache controller but a memory controller and it can support up to 512 kbytes of write-back cache.

MultiVendor in MicroSeconds

Real-Time Microsecond Response from Multivendor Computer Environments

Are fast, real-time computations between multiple vendors' computers unrealistic? No. Through replicated shared-memory, the SCRAMNet™ Network from SYSTRAN allows high-speed transfer of data between multivendor computers in real-time — without communication software.

SCRAMNet's ring configuration achieves microsecond application-to-application performance with zero software overhead. Revolutionary features include data-filtering to reduce network traffic, byte swapping for automatic reformatting of variables, interrupt passing for synchronization, and a dual fiber optic link that handles 150 Mbit/sec line transmission rates for distances up to 300 meters.

Call SYSTRAN at 1-800-252-5601 for more information on the only communications network for stringent, real-time demands: SCRAMNet.

SYSTRAN CORP.

The Problem Solving Company

4126 Linden Avenue • Dayton, OH, USA 45432-3068
(800) 252-5601 • FAX (513) 258-2729

CIRCLE NO. 22

"Boosting the performance of the cache isn't the only way to enhance system performance."

—Jack Lii, Cache Computers



Faced with a plethora of newer 486 Intel derivations that will cover an expanding spectrum of clock speeds, potential users of off-the-shelf cache solutions have split into two camps: one group that resorts to custom ASICs when their volumes get high enough and another group that doesn't believe in the benefits of cache techniques. Cache controller vendors may find themselves selling products to a very select customer base at the highest end of the performance range. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Cache Computers	
(415) 226-9922	Circle 244
Intel	
(800) 548-4725	Circle 245
Mosel	
(408) 733-4556	Circle 246
Mylex	
(415) 683-4600	Circle 247
Opti	
(408) 980-8176	Circle 248
Pioneer Computer	
(415) 623-0808	Circle 249
UMC	
(408) 727-9339	Circle 250

It Takes One To Know 1 μm .

And, Mitsubishi is the only one who reduced $1\mu\text{m}$ gate width to a size that's small enough to provide a low, $5\mu\text{W}$ power dissipation (the lowest you can get), lower operating temperature and small die size. Plus, we're the only supplier to give you performance as fast as 370 picoseconds and four speed/power options: x1, x2, x3, and x4. So, you can optimize your circuit for both fast speed and low power. By taking advantage of Mitsubishi's smaller cell sizes, you achieve low operating temperature, more-cost effective silicon use

**We're The Only One
With $5\mu\text{W}$ And Four
Speed/Power Options.**

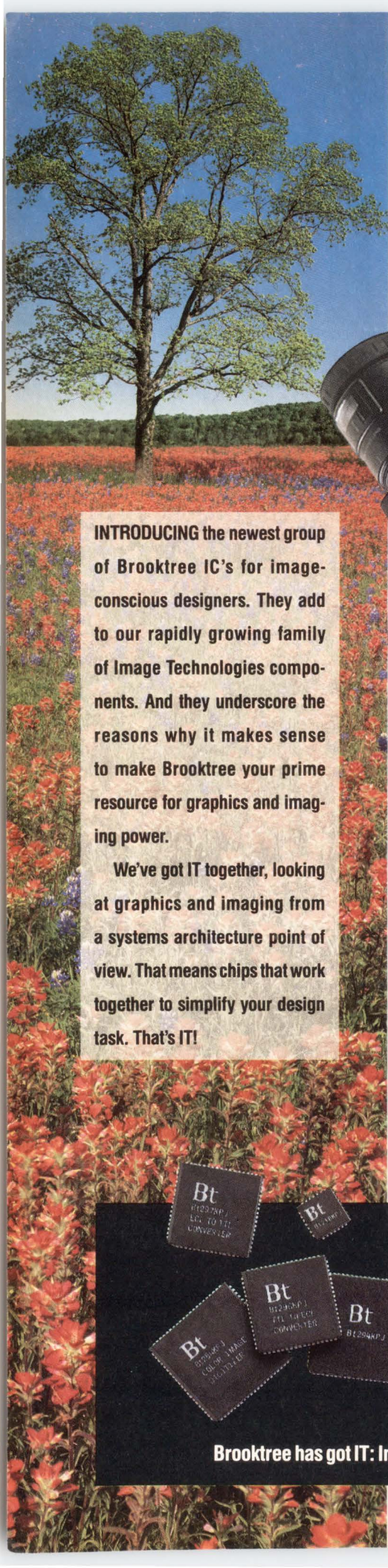
and smaller die size. And, all this means we can help you put your designs in smaller, lower-cost plastic packages and achieve higher reliability. Plus, our selectable output buffer drive and slew rate control help reduce noise and electromagnetic radiation. Mitsubishi offers 70,000 gates (50% utilization); patented* gate isolation structure for faster performance, and extensive packaging options, including plastic QFPs, very-fine-pitch QFPs (VQFPs), PLCCs and APGAs (adaptable pin-grid-arrays). And, of course, we give you 100% burn-in, 100% AC and DC testing, a library of more than 500 cells and design kits for the industry's leading-edge CAE design tools. It takes one solid, proven semiconductor supplier to know $1\mu\text{m}$. We're one of the top ten worldwide semiconductor manufacturers, and the world's fifth largest

MOS memory manufacturer. We've been producing gate arrays since 1976 and offer production capacities surpassed by none. So, we'll get you through $1\mu\text{m}$ design, prototype and production fast and right the first time. Also, keep in mind, a good $1\mu\text{m}$ will get you to a great $0.8\mu\text{m}$! Call the one it takes to know $1\mu\text{m}$ today at 1-800-624-8999 #178.

*U.S. Patent No. 4,562,453

 **MITSUBISHI**
ELECTRONIC DEVICE GROUP

CIRCLE NO. 23



INTRODUCING the newest group of Brooktree IC's for image-conscious designers. They add to our rapidly growing family of Image Technologies components. And they underscore the reasons why it makes sense to make Brooktree your prime resource for graphics and imaging power.

We've got IT together, looking at graphics and imaging from a systems architecture point of view. That means chips that work together to simplify your design task. That's IT!

IMAGE ACQUISITION. We've got chip sets that bring image capture to your system with an added dimension: Image quality, made possible by three new 30 MSPS devices that support higher resolutions.

The Bt252 Gray-Scale Image Digitizer, with its onboard lookup table, is perfect for machine vision applications.

The Bt254 Color Image Digitizer's triple Flash A/D's digitize your analog RGB for low noise, high quality multimedia applications.

And our new Bt218 30 MSPS single channel CMOS Flash A/D provides another basic building block for image acquisition.

Team any of the three with our Bt261 30 MHz line lock controller and one of our true-color RAMDACs for a complete image acquisition system on a board.

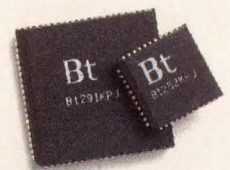


Convert and optimize its color space in real time,



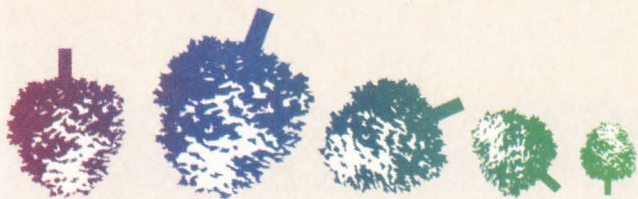
Capture an image and digitize it,

IMAGE RECEPTION. We've got chip sets to send and receive true-color digital video using an 8-bit interface. Our Bt294 CCIR 601/SMPTE RP 125 Decoder works with our upcoming Bt297 ECL-TTL Translator for a complete solution to 4:2:2 digital component video.



WHAT

Brooktree has got IT: Image Technologies. It's our system-smart approach to packing image acquisition, manipulation,



send it and receive it as live color video then display it in high resolution true-color



IMAGE TRANSMISSION. We did say complete solution, didn't we? The Bt291 CCIR 601/SMPTE RP 125 Encoder teams with the upcoming Bt296 TTL-ECL Translator to provide cost effective 4:2:2 digital component video transmission without adjustments or support circuitry. In combination with the Bt294/297 reception devices, they make it easy and economical to add point-to-point video transmission to your multimedia system.

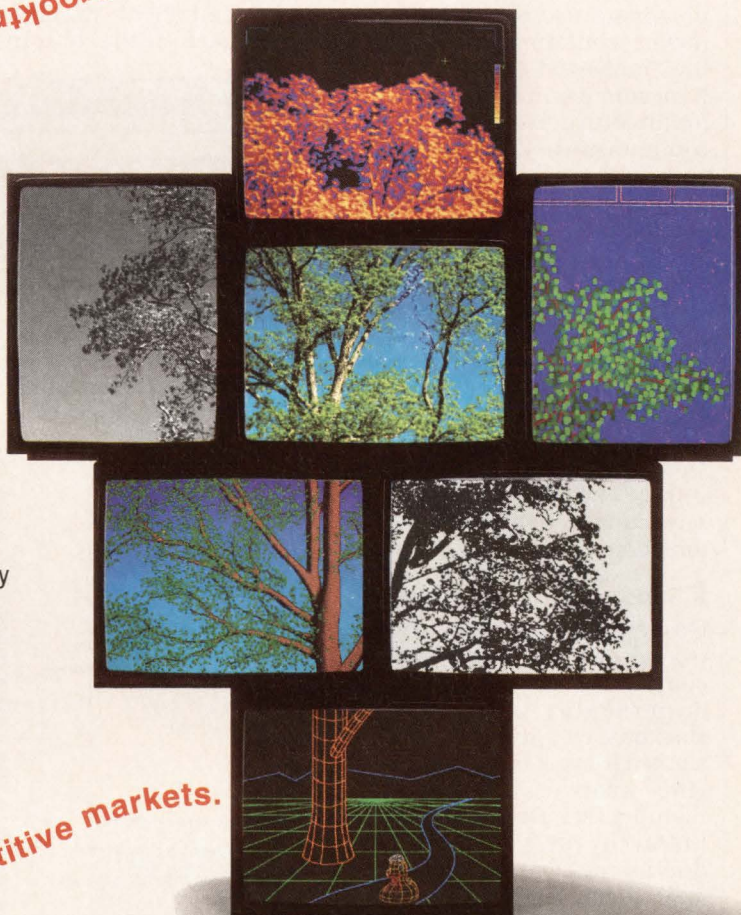
and do it all with Brooktree's Image Technologies. They make it easy to give your PC or WS design a visual edge in today's competitive markets.

IMAGE PRESENTATION. When it comes to display technology, we're where IT's at: We revolutionized RAMDACs. Now we're setting a new performance standard for super VGA, high-end XGA, 8514/A, TIGA compatible and x. terminal applications. It's the Bt484 true-color RAMDAC.

Its programmable pixel depth means you can run at 4 bits/pixel with 8:1 multiplex, 8 bits/pixel with a 4:1 MUX, 16 bits/pixel at 2:1 MUX or even 32 bits/pixel for 24-bit true color and 8-bit VGA. And its 32x32x2 three-color, user-definable cursor is absolutely awesome.

GET IT NOW.

Get with IT with Brooktree. Make us your source for Image Technologies products and information. We've assembled especially useful packets of technical information, geared to your special interest. To get yours, call **1-800-VIDEO IC**. Or write Brooktree Corporation, 9950 Barnes Canyon Rd., San Diego, CA 92121. **(619) 452-7580**. FAX **(619) 452-7294**.



© 1991 Brooktree Corporation.

IT IS.

transmission and presentation into highly-integrated, tightly-linked chip sets.

Brooktree®

Transputer performance boosted to 10x that of its predecessor

Tom Williams, Senior Editor

The first member of a new family of transputers has been introduced by the Inmos division of SGS-Thomson (Colorado Springs, CO). The transputer, code named H1, boasts an order of magnitude increase in all performance parameters, except power consumption. Performance has improved thanks to enhancements in the processor architecture as well as in the communications section of the chip, both of which now occupy approximately equal areas of silicon.

The H1 peaks at 200 Mips and offers 60-Mips sustained throughput with 25-MFlops peak and 10-MFlops sustained floating-point performance. Overall performance improvements include enhanced communications via the processor's four serial links. Each bidirectional link now runs at 10 Mbits/s in each direction.

Superscalar architecture

Gains in processing performance of the transputer come from a new pipelined superscalar architecture that passes multiple instructions per cycle down the pipeline, from a hierarchical memory scheme with cache hierarchy and from the reduction of cycle count for instructions. Most instructions now take between two and five cycles. In addition, fast CMOS process lets the part run at 50 MHz. Even with the enhancements and additions to the instruction set, the H1 maintains compatibility with the T805 transputer.

The H1's superscalar architecture supports multiple instruction units (IUs) that can execute in parallel for a sustained instruction rate of 4 instructions/cycle. The architecture is supported by an in-

telligent pipeline that automatically routes instructions to the proper execution unit without the need for a sophisticated optimizing compiler. The pipeline also has access to a 32-word workspace cache, which stores the most recently used local variables. The workspace cache eliminates in many

cases the need to go to the on-chip cache for data.

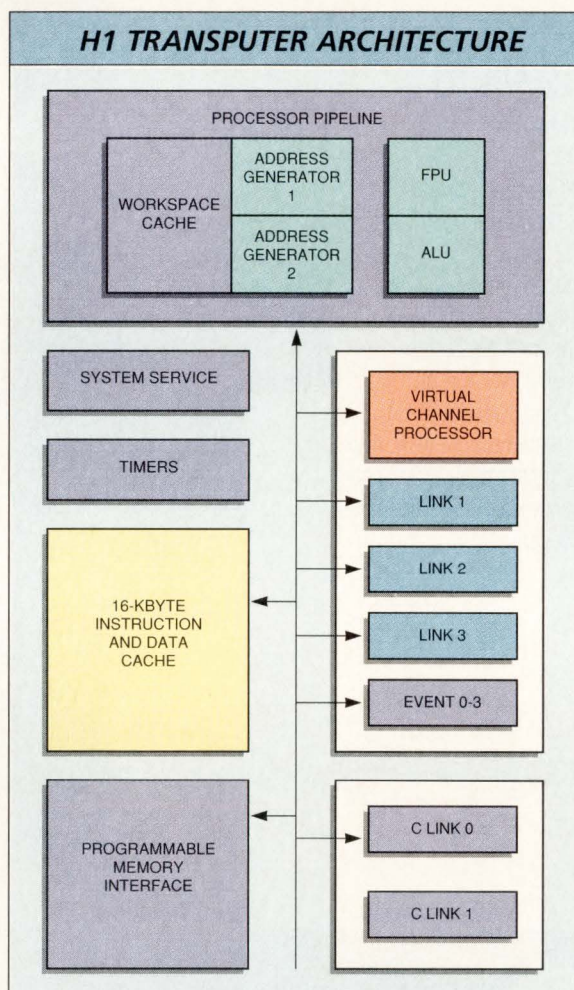
Instructions are fetched in groups of four 8-bit instructions, that is, one 32-bit word. Operands for some instructions must, of course, be fetched on subsequent cycles, which introduces gaps between some instructions in parallel paths in the pipeline. But the hardware itself is able to avoid pipeline stalls. When a group of instructions is fetched, a hardware "grouper" scans them and decides which type of instructions they are and to which IU they should be routed. The grouper then

re-sorts them onto the proper paths in the pipeline, which includes stages of instruction fetch, grouping, local cache access, address generation, memory read, execution, and memory write.

With this superscalar architecture, not every instruction will perform every function possible along the pipeline, and, as noted above, there will be times when not all instruction units are busy. The traditional way to handle such an architecture is to have an optimizing compiler analyze the code and schedule instructions to optimize the use of parallel execution units.

This involves inserting No-Ops into the code to avoid pipeline stalls when an IU will be idle. Instruction scheduling in hardware avoids padding the code with No-Ops, instead throwing them in at the last minute when the idle IU needs them. This avoids bloating the code with unneeded instructions (which is especially bad for embedded applications, because they seek to occupy minimal space). It also eliminates the processor overhead involved with fetching and processing No-Ops.

The workspace cache is also an important element in avoiding pipeline stalls. "You can think of it as internal to the pipeline," says Raul Diaz, senior field application engineer at Inmos. "So the pipeline, when it's fetch-

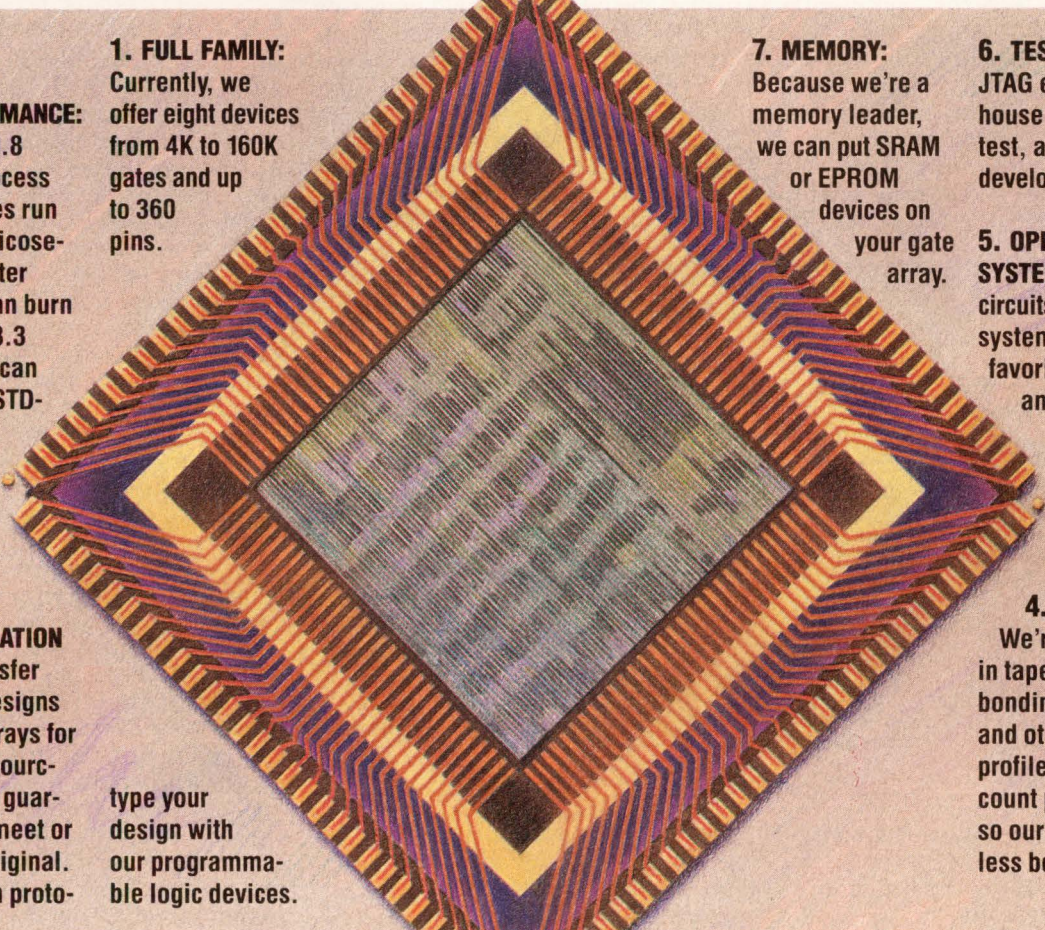


The architecture of the H1 transputer from Inmos features a multiple-path intelligent pipeline that uses grouping hardware to schedule instructions for four multiple execution units and four bidirectional serial links. A hardware virtual channel processor can multiplex large numbers of interprocess messages over the four physical links. The on-chip cache can be configured as either cache memory or program RAM for embedded applications.

ATMEL GATE ARRAYS OPEN TO THE PUBLIC

Atmel engineers have been successfully making gate arrays for some of the world's biggest computer makers for more than a decade. That's some 650 different personalizations. Now we are offering our latest generation to the public.

Here are seven reasons why you should pick Atmel for your next gate array.



1. FULL FAMILY: Currently, we offer eight devices from 4K to 160K gates and up to 360 pins.

2. PERFORMANCE: We use a 0.8 micron process so our gates run fast (260 picosecond inverter delays), can burn less fuel (3.3 Volts) and can meet MIL-STD-883C.

3. TRANSLATION EASE: Transfer existing designs into our arrays for alternate sourcing. Atmel guarantees to meet or beat the original. Or, you can prototype your design with our programmable logic devices.

4. PACKAGES: We're a leader in tape automated bonding (TAB) and other low-profile, high-pin-count packages, so our arrays use less board room.

5. OPEN DESIGN SYSTEM: We make circuits, not design systems. Use your favorite hardware and software.

6. TEST PROOF: JTAG eases in-house system test, and cuts test development time.

7. MEMORY: Because we're a memory leader, we can put SRAM or EPROM devices on your gate array.

So, if you're looking for an old hand at gate arrays, look to Atmel; we've been making great arrays for almost as long as they've been around. Call, write or FAX us to get our latest gate array literature.

ATMEL CORPORATION
2125 O'Neil Drive
San Jose, CA 95131



The people who make the difference.

Tel. 1-800-292-8635
Tel. (408) 441-0311
FAX (408) 436-4200

INTEGRATED CIRCUITS

ing local variables, doesn't ever have to go to the on-chip cache because it has its own registers inside where it keeps the latest parameters." The workspace cache allows two reads and one write on every cycle, so statistically there's little chance of a stall during the cache access stage of the pipeline.

The on-chip cache itself is a fully unified set-associative 16-kbyte cache. It can store both instructions and data and allows 4 accesses/cycle. But the cache is also configurable. It can be set up as a 16-kbyte system RAM for use with compact embedded applications, for example, as an 8-kbyte RAM and an 8-kbyte cache, or as a full 16-kbyte cache. For those who wish to use a communications scheme other than the serial links

manager David Dornblaser.

Another problem arises when there are more "channels"—software virtual links for communications between processes on separate transputers—than there are physical links. The solution on the T805 and earlier transputer models has been to write special multiplexing software, for which Inmos has developed libraries.

The H1, however, uses a hardware communications processor called the virtual channel processor (VCP) that can multiplex up to 16,000 virtual links onto one physical link. The VCP packetizes communications in 32-byte message packets, each of which it gives a distinct header and end-of-packet (or end-of-message) field. The VCP automatically decodes the headers

Inmos, to tell which packet headers are to be routed to which physical links. As a packet comes in, its header is decoded, and the routing switches automatically create a temporary circuit for the data. As the end-of-packet "tail" passes through, the channel is closed, like dirt collapsing behind a burrowing earthworm. This is done with a latency of less than 1 μ s. A single C104 can handle up to 32 physical links.

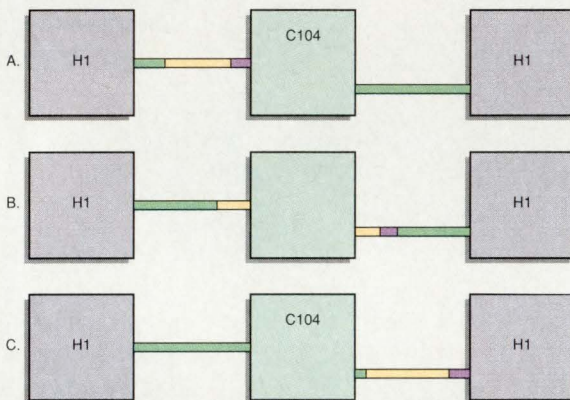
Real-time enhancements

In addition to its four serial communication links, the H1 also has four hardware interrupt lines that could be thought of as "bit links." They let a transputer either receive or generate interrupts. Error handling, which was a global function on the T805, now lets errors be handled locally on a per-process basis. A trap handler can be assigned to most processes to manage errors. For catastrophic errors—errors that have no assigned handling—a message can be sent to the system control process over an additional link, the control link. The control link is used exclusively to propagate an error message over an entire network of transputers.

Also new is a protected mode. Normal processes, called P-processes, run in user mode and are protected against other "untrusted" processes. They aren't allowed to access systems-level instructions, which are reserved for "trusted" or operating systems-level processes.

Inmos is porting real-time kernels and operating systems to the H1. One of these is the Chorus operating system by Chorus Systems, which includes a Unix-compatible programming interface. Real-time kernels include VRTX by Ready Systems and C Executive by JMI Software Consultants. According to Diaz, Inmos already has in place a suite of development tools including a C compiler and network configuration tools.

C104 'WORMHOLE ROUTING'



The C104 dynamic routing switch automatically reads message packet headers to make its routing decisions (A). If the output link is free, a temporary circuit is created to send the packet from input to output with no buffering (B). As the end-of-packet tail token is pulled through, the circuit vanishes (C).

provided by the transputer architecture, there are instructions for support of shared memory and DMA-based coprocessors.

Enhanced communications

Current transputer technology allows interprocess communication via memory on the same transputer and via four serial links between processes residing on different transputers. But the complexity of a network can make applications development difficult—and may make porting applications to new systems even more so. "Portable software demands that the details of the network be relatively transparent," says Inmos technical marketing

of arriving packets to determine the destination virtual link. For every packet sent out on a link, an acknowledgment packet, consisting of header and end-of-packet token, is sent back to the originating VCP. This method works for point-to-point communication adjacent transputers; for nonadjacent chips, Inmos has created a dynamic routing switch.

The C104 dynamic packet routing device had to solve the problem of routing messages without incurring any overhead from store-and-forward buffering. The solution is what Inmos calls "wormhole routing." The C104 is loaded with a table, generated by tools developed by

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

SGS-Thomson (719) 630-4000 Circle 215

THE MEGABIT E² WITH OPTIONS

Now you can choose the exact megabit E²PROM to meet your system needs. You don't have to design around your suppliers' shortcomings ever again. Our new megabit family can satisfy every system requirement. Call it the megabit E² with options. Look:

OPTION 1

ORGANIZATIONS

- 128K by 8**
AT28C010
- 64K by 16**
AT28C1024

OPTION 2

PACKAGES

- DIP**
- LCC**
- Flatpack**
- TAB**

OPTION 3

ENVIRONMENTS

- Industrial**
- Commercial**
- Military**
- Space**

No matter what options you need, our megabit E²PROMs run as fast as 120 nano-seconds, have 300 microamp standby power, up to 100,000 write cycle endurance, individual byte programmability and on-chip error detection and correction. And, as with everything we make, they are available processed to MIL STD 883C.

So, if you want the megabit E²PROM designed for your system, in volume now, call Atmel.



ATMEL CORPORATION
2125 O'Nel Drive
San Jose, CA 95131

The people who make the difference.

Tel. 1-800-292-8635
Tel. (408) 441-0311
FAX (408) 436-4200

CIRCLE NO. 63

INTEGRATED CIRCUITS

80-MHz RISC processor screams through floating-point

Dave Wilson, Senior Editor

Companies introducing new RISC processors into today's crowded market must be either crazy or extremely optimistic that they can bring something new to the processor party. Betting on the latter scenario, Micron Technology (Boise, ID), better known for memory technology than processor architecture, will roll out a new processor dubbed FRISC in the third quarter.

The objective of the FRISC project was to develop a 64-bit processor with fast context-switching time and high floating-point performance. By targeting embedded-control and signal-processing applications, Micron hopes to avoid direct competition with the likes of Intel and Motorola. Despite that fact, a comparison with the 860 from Intel (Santa, Clara, CA) will be inevitable.

The FRISC chip consists of seven functional units: the bus unit (BUSU); a program control unit/vector interrupt unit (PCU); an instruction fetch unit (IFU); a register file (RF); a block-transfer register scoreboard unit (BTRSU); a data load store unit (DLSU); and an execution unit (EXU) consisting of a parallel floating-/fixed-point multiplier and a floating-/fixed-point adder/subtractor unit. The processor executes in a five-stage pipeline and can handle background block-transfer load/store operations, in addition to instruction buffer loading.

Banked, fully mapped system

The FRISC virtual memory system differs from the hierarchical memory caching technique supported by the Intel 860 design and is best described as a banked, fully mapped system. The 32-way, byte-addressable, interleaved memory supports a 12.5-ns cycle time both in the chip and to the Interleaved Memory Buffer (IMB) registers, a 20- to 30-ns DRAM page-mode cycle time and an 80- to 110-ns DRAM row/column cycle time.

A direct-mapped cache in the IMB MMU maps the virtual row address

bits to the physical row address bits. This banked fully mapped virtual-memory scheme implies that the DRAM column addresses are both physical and virtual memory addresses. The IMB operates in a write-back manner with a page-mode write-back to the current DRAM page being performed only if there was a write to one of the eight 64-bit double words of that bank's line.

"Such a memory architecture implies that the chip will be well-suited to data that is heavily vector-oriented," says Scott Israel, director of marketing at Alacron (Nashua, NH), a manufacturer of 860 accelerator boards for the PC bus and VMEbus.

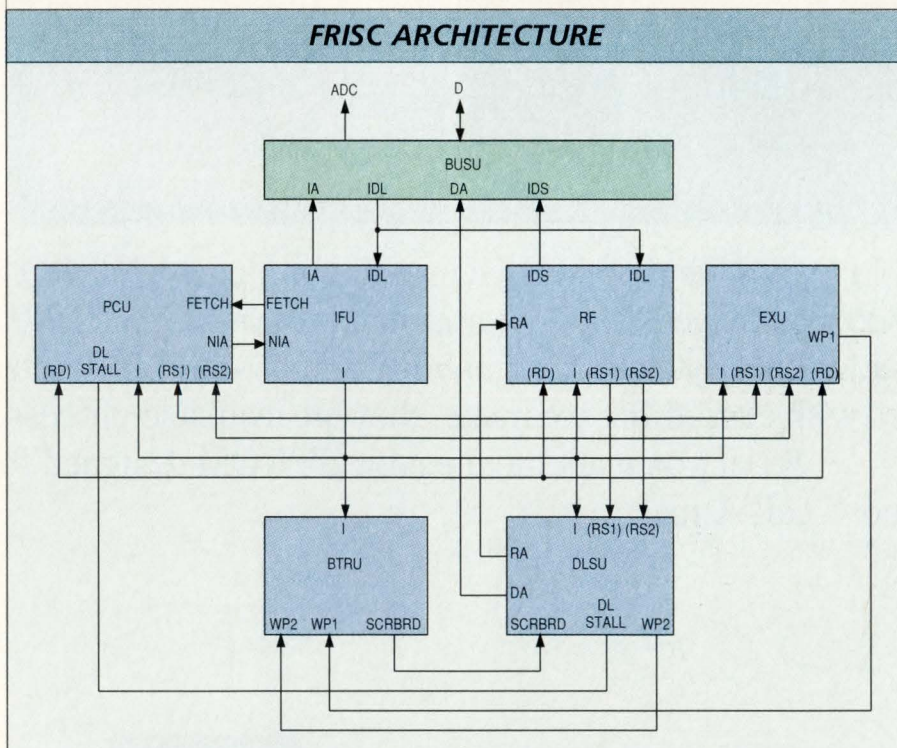
FRISC vs. 860

The 860 takes a more conventional hierarchical memory approach than FRISC. Designers can cache instruc-

tion, data and address translation information directly on chip.

There are other differences between the FRISC and the 860 in the way interrupts are handled and context switches are performed. On the FRISC, the PCU is responsible for generating the next instruction addresses that are directed to the IFU. The vector interrupt unit prioritizes one of 16 interrupts and sends the interrupt service address of the vector table to the IFU. Both preemptable and non-preemptable interrupts can be serviced by the unique design of the interrupt system. The interrupt latency can be as short as two machine cycles (24 ns) if a non-preemptable routine is not in progress. Since the entire set of pipeline registers are duplicated, a low-overhead real-time interrupt service routine could load or store data or refresh the DRAM and return to the current process in four machine cycles. The vector interrupt sub-unit and the block-transfer sub-units support message-passing communication in large-scale parallel applications, as in Mach.

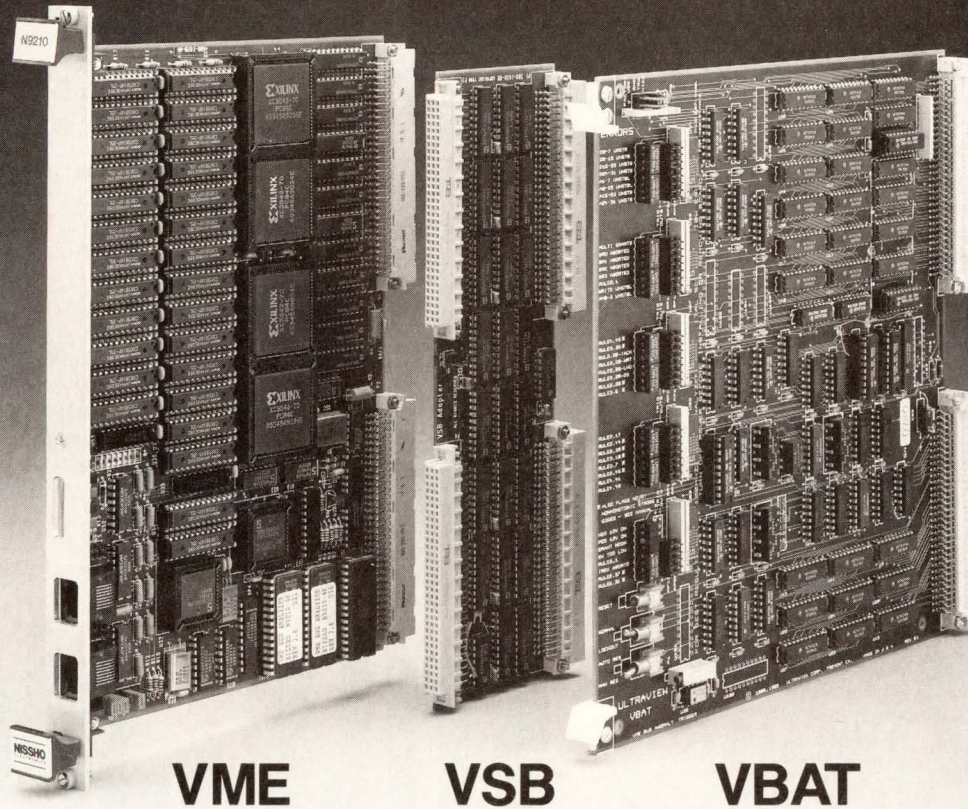
The 860, on the other hand, is



The FRISC architecture provides hardware support for real-time multiprocessing. Capable of handling load/store operations as a background task, the FRISC chip can support concurrent real-time and background operating systems.

BOTHERED BY BUS BUGS?

NOW YOU CAN SEE THE WHOLE PICTURE.



VME

- Captures up to 64K VMEbus events
- Stores 96 VME signals with a time tag during each event
- 50MHz VME Timing Analysis
- Bus Master Capability
- Printer/Passthru port for connection to Printer and Host Computer

VSB

- VSB State Analysis
- Switches analysis between VME and VSB buses
- Synchronous sampling of VME/VSB events up to 25MHz
- Slot number identification command

VBAT

- VMEbus Anomaly Trigger
- Screens 98 lines for 28 classes of violation
- Fully automatic with 104 preset triggers
- 37 individual LED's and trigger outputs
- Detects extra transitions on strobe line

A NISSHO ANALYZER is indispensable for ENGINEERS and DESIGNERS who are involved in:

- Hardware system design, analysis and debugging
- Hardware production testing and quality assurance
- Industrial instrumentation and control system integration
- Software development
- Field service

For your copy of "ANALYZER APPLICATIONS" and a FREE 30 DAY EVALUATION, call:
800-233-1837; in California 714-261-8811

NISSHO
ELECTRONICS

17320 Red Hill Avenue, Suite 200 Irvine, CA 92714 FAX: (714) 261-0934 TLX: 181-308

CIRCLE NO. 27

INTEGRATED CIRCUITS

Pushing back the limits of floating-point performance

While today's fastest microprocessors run the double-precision Linpack at 14 MFlops at best, the FRISC achieves a 340-MFlops double-precision Linpack (65-MFlops single-precision), using a bank-interleaved DRAM main memory. Micron Technology claims that this performance is relatively independent of vector size.

The FRISC CPU has a peak floating-point performance of 160 MFlops single precision and 80 MFlops double precision. A unique fully scoreboarded block-transfer unit supports double buffering of the 64-word five-port register file so that background load/store operations can occur in parallel while current data is being processed by the execution units.

Unlike the Intel 860's dedicated units for integer and floating-point calculations, the FRISC's floating-/fixed-point arithmetic sub-unit performs all 32- and 64-bit integer, signed, and single- and double-precision IEEE 754 floating-point instructions, as well as maximum, minimum and subtract/compute condition code instructions for each data type. Full support for IEEE 754 rounding and exception handling is provided. A new instruction can be issued every clock cycle. A floating-/fixed-point multiplier sub-unit performs all fixed- and floating-point multiplications, and a full-precision divide and square root.

All single-precision operations, mixed-precision operations and fixed-point operations can be issued every clock cycle. Double-precision operations can be issued every other machine cycle. Full support for IEEE 754 rounding and exception handling is also supported. Chained operations are directly supported for single-, double- and mixed-precision floating-point operations.

more software-intensive. It handles interrupts through the use of traps. Traps cause interruption of normal program flow to execute a trap handler program. Vectored interrupts must be implemented with vector interrupt controllers and software. Full hardware mechanisms to save and restore the machine state were considered unnecessary in the 860, and are performed in software.

The FRISC PCU also contains the master clock control circuitry to control the pipeline interlocks due to instruction buffer misses or block-transfer scoreboard hits, as well as the vector interrupt processing. Hardware control of pipeline interlocks reduces the burden on the compiler and is critical to achieving a tightly coupled processor and DRAM- and IMB-based memory system.

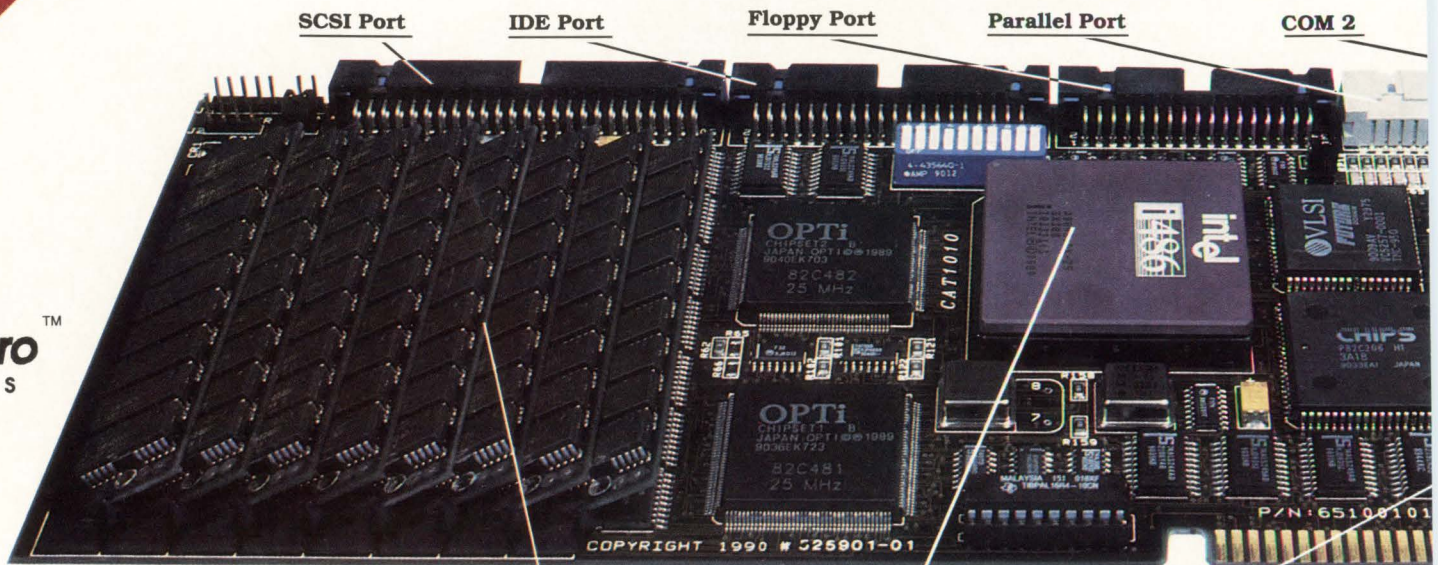
The IFU contains eight fully associative instruction buffers that are constrained to load using a least re-

Inquire about price reductions on DTI's Single Board Computers.



STILL..MORE

About The DTI 25/33MHz '486'TM



Up to 32M RAM On-board

High Performance Intel 80486 33MHz

Industry Standard Custom BIOS

Product names are trademarks or registered trademarks of their respective companies. 486 & 486 are trademarks of Intel Corp. Slotpro is a trademark of Diversified Technology

INTEGRATED CIRCUITS

cently used replacement strategy. In addition, a valid buffer permits the buffer loading operation to occur in the background, with the first instruction issue occurring once the first valid instruction is loaded into a buffer.

The DLSU performs all single and block-transfer load/stores to the five-port RF. Since all single or block-transfer pending loads are scoreboarded by the BTRSU, the RF can be made to operate as a double-buffered memory with a background load of new data, or to store processed data occurring in parallel with execution unit processing. The five-port RF allocates two read ports and one write port to the EXUs and one read port and one write port to the DLSU.

The BUSU arbitrates between the IFU and DLSU bus requests and generates all memory selection and timing. On-chip configuration regis-

ters permit the entire memory address definition and timing to be easily modified to suit a given application. Direct support of the write-back mechanism for the IMB MMU is transparent to the DLSU and further improves the performance of the system's average memory access time.

A board-level demonstration supercomputer using the FRISC processor will be produced in 256-Mbyte and 1-Gbyte configurations. The FRISC CPU and the eight IMB MMUS are each housed in 164-pin LCC packages and are mounted in a 4x4-in. mechanical assembly that utilizes a mainframe-grade AMP interposer interconnect system. The entire mechanical assembly will be thermoelectrically cooled so that the chip temperature is maintained at a constant 25°C. The board can operate in two configurations, either connected to a Sun host running Unix via a host interface unit and

controlled with a remote procedure call mechanism, or operated in a stand-alone mode.

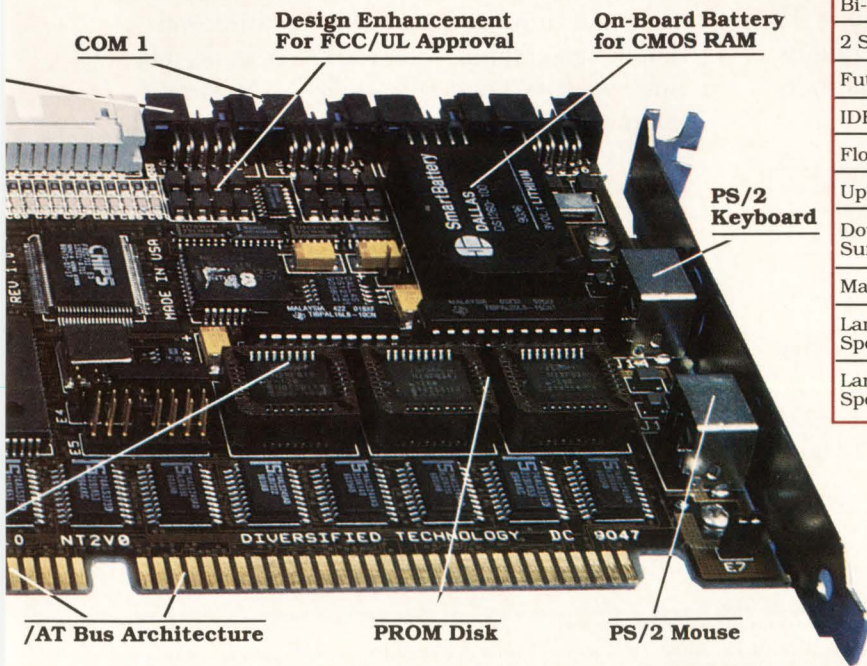
Although Micron is still in the early stages of software development, the company has examined the applicability of both VxWorks from Wind River Systems and the Lynx OS from Lynx Real-Time Systems. On the multiprocessing side the company is leaning toward supporting the Mach operating system, since hardware hooks for multiprocessing are provided on-chip. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Alacron		
(603) 891-2750	236
Intel		
(800) 548-4725	237
Micron Technology		
(208) 368-4000	238

REAL FACTS!

Single Board Computer



COMPARE FUNCTION	DTI CAT1010 486	Competitor 1 486	Competitor 2 486
25, 33MHz CPU- Shipping Now!	✓		25MHz Only 7-8 Wks Del.
Up to 32M RAM Onboard	✓		
Noise Reduction Circuitry For FCC Class B	✓		
PS/2 Mouse Support	✓		
PS/2 Keyboard Support	✓		
On-Board Battery Real Time Clock	✓		✓
Bi-directional PS/2 Printer Port	✓		
2 Serial Ports - Up to 115K Baud	✓		
Future Domain SCSI	✓		
IDE Interface	✓		
Floppy Interface	✓		
Up to 512Kb User PROM Disk	✓		
Double Sided Surface Mount Technology	✓		
Manufactured In-House(U.S.A.)	✓		
Landmark V1.14 Speed at 25MHz	114.1		84
Landmark V1.14 Speed at 33MHz	150.9		

NOT AVAILABLE

Call us toll free for orders and information.

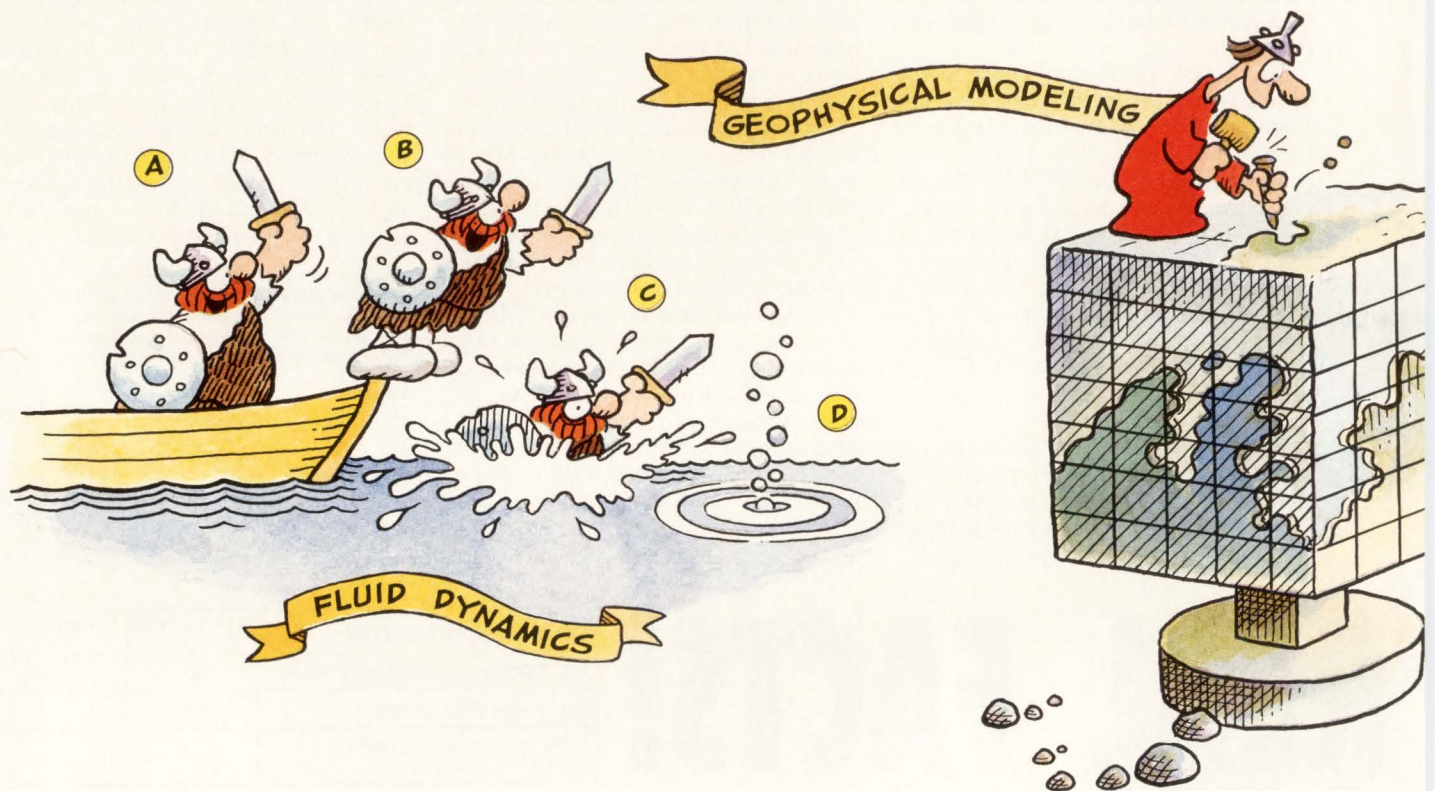
1-800-443-2667

Diversified Technology
An Ergon Co.

U.S.A. - (601) 856-4121 Fax (601) 856-2888
Outside U.S.A. - (201) 891-8718 Fax (201) 891-9629

CIRCLE NO. 28

The IBM RISC System/ The power you've been seeking



It's a never-ending quest for power seekers. You're always looking for ways to run your favorite applications faster. Well, search no more. The RISC System/6000™ family of POWERstations and POWERservers gives you power that soars as high as 23 MFLOPS.

	MFLOPS	MIPS	SPECmark™
POWERstation 320	8.5	29.5	24.6
DECstation 5000-200	3.7	24.2	18.5

When it comes to porting, your ship has come in. Of course, all the speed in the world wouldn't mean much without the applications you need. So the RISC System/6000 family

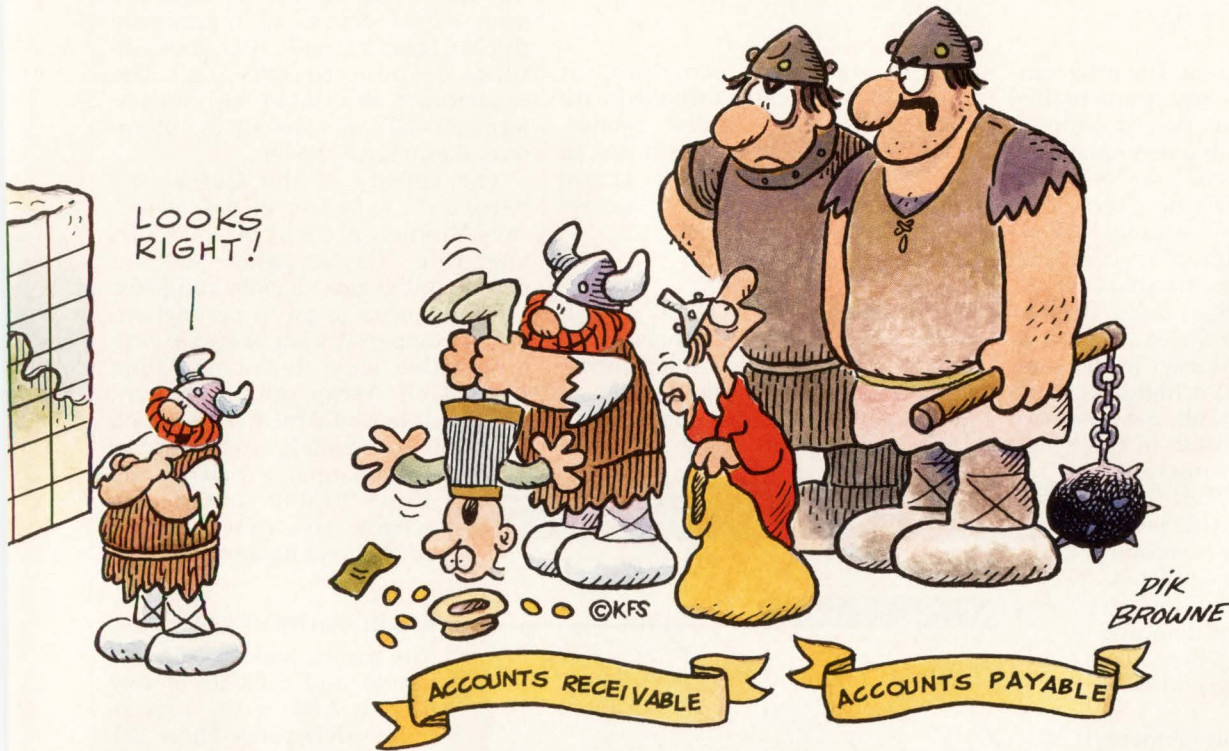
already has more than 2,500 of the most popular technical and commercial applications up, running and running fast. And if you think you know a good thing when you see it, so do software vendors. That's why you'll also be seeing more and more applications coming on board the RISC System/6000 platform all the time. And if you like to build your own solutions, there's a full arsenal of enablers and relational data bases from leading vendors, as well as CASE tools and a host of popular programming languages.

A smorgasbord of solutions. Applications already announced include the IBM engineering design packages CADAM™, CAEDS™, CBDS™,

MFLOPS are the results of the double-precision, all FORTRAN Linpack test 100x100 array suite. The Dhrystone Version 1.1 test results are used to compute RISC System/6000 Integer MIPS value where 1,757 Dhrystones/second is 1 MIPS (Vax 11/780). SPECmark is a geometric mean of ten benchmark tests. All performance data are based on published benchmark information.

IBM is a registered trademark, and RISC System/6000 and CAEDS are trademarks of International Business Machines Corporation. SPECmark is a trademark of Standard Performance Evaluation Corporation. UNIX is a registered trademark of UNIX System Laboratories, Inc. CADAM is a trademark of CADAM INC. CATIA is a trademark of Dassault Systemes. CBDS is a trademark of Bell Northern Research Corporation. DECstation is a trademark of Digital Equipment Corporation. HAGAR THE HORRIBLE Character(s) © 1990 King Features Syndicate, Inc. © IBM Corp. 1991, all rights reserved.

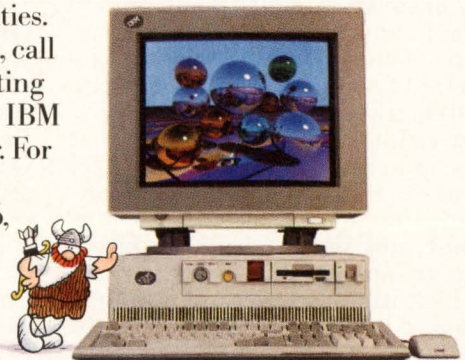
6000 family. for all your applications.



CATIA™ and AES. Also available are a broad spectrum of solutions from vendors like Valid Logic, MacNeal Schwendler, Swanson Analysis, SAS Institute, SPSS, Wavefront, Alias, Polygen, Cadence, Fluid Dynamics International, Western Atlas, ECL Petro and create.X. Scientific and technical applications are available in areas like physics, structural analysis, chemistry, securities trading, mathematics, earth resources, operations research, visualization, graphics, technical publishing and more. There's also accounting software like FourGen and support for leading UNIX®-based office automation packages. And there are key industry applications for businesses in medical groups, retail stores, newspapers, pharmacies and many more.

Command enormous processing clout.

The RISC System/6000 family is built to boost the performance of the software power seekers use most. It's got the best floating point processor in the business for numerically intensive applications, plus a new superscalar processor and incredible 3D graphics capabilities. To find out more, call your IBM marketing representative or IBM Business Partner. For literature, call 1 800 IBM-6676, ext. 990.



For the Power Seeker.

CIRCLE NO. 29

Interconnect key to speed of new programmable ASICs

Barbara Tuck, Senior Editor

The bottom line in the programmable device market is to give designers the fastest time-to-market with the highest-speed device. The founders of Peer Research, now QuickLogic (Santa Clara, CA), having invented the original PAL devices at Monolithic Memories, can claim a familiarity with that market. QuickLogic principal John Birkner and his peers, convinced that a low-impedance interconnect is the solution, have created a highly conductive path, or ViaLink, between two metal layers of CMOS in their just-announced programmable ASICs (pASICs). VLSI Technology (San Jose, CA) is using a standard high-volume 1.2- μm CMOS logic process, jointly developed by the two companies, to manufacture the pASIC 1 family, expected to be in volume production by midyear.

For the ViaLink element in its pASICs, QuickLogic uses a high-resistance amorphous silicon, similar in electrical characteristics to the silicon dioxide that insulates the vias, or vertical openings, connecting one metal line to another. The application of 10 V to a via containing a specially deposited layer of amorphous silicon triggers a flow of programming current that permanently changes the structure of the silicon. The result is a metal-to-metal connection with a resistance of less than 200 Ω . Key to QuickLogic technology is the plasma-enhanced chemical vapor deposition equipment needed to deposit the amorphous silicon, equipment that wasn't available until a few years ago.

Essentially an antifuse structure created in a programmable via, the ViaLink interconnect emulates that of gate arrays by hooking logic gates together with real wires. Competitive devices, according to Birkner, simulate real wires with memory-

type floating-gate structures or transistor pass gates switched with RAM cells. These active connections, with effective resistances in the range of 2,000 to 3,000 Ω and high-parasitic capacitance, can severely limit device speed.

Programmable wires

QuickLogic claims the pASICs' hard-wired physical link and regular interconnect structure will let the devices maintain raw speeds even in fast pipelined designs. Speed-compatible with 80386, 80486 and RISC

1,000 Ω . "Actel goes down to the substrate and does its magic in the active area of the circuit," says Birkner. The QuickLogic via in which the link is formed is more than one and a half orders of magnitude thicker than an Actel dielectric antifuse, according to QuickLogic. The capacitance associated with an unformed ViaLink element is, therefore, many times lower.

The density of the QuickLogic pASICs "is a matter of definition," says Birkner. A count of what Birkner calls "honest gates" yields a 500- to 4,000-gate density range for the first parts to go to production. When compared with erasable programmable logic device or Xilinx Logic Cell Array gates, though, those counts would have to be upped to 1,500 to 12,000, according to

QuickLogic, which claims that 20,000 gates are within the reach of the pASIC technology.

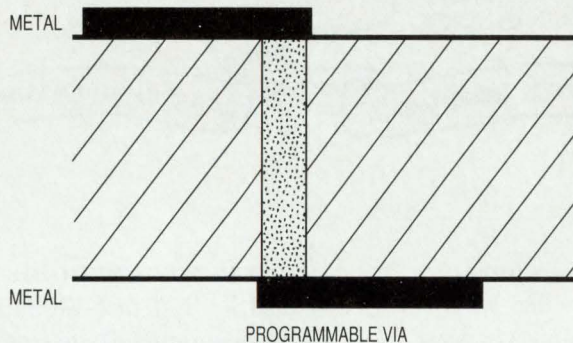
Granularity of pASICs

The pASIC logic cell has 23 inputs and consists of two 6-input AND gates, four 2-input AND gates, three 2:1 multiplexers, and a flip-flop. Each cell can accommodate logic functions up to 14 inputs in width. All 200 gate array-like library macros have built-in scan cells. Flip-flops can be configured as a D, JK, T, or RS function, and toggle rates are over 130 MHz for a simple D flip-flop and over 110 MHz for a JK.

Each pASIC device consists of a matrix of logic cells between rows and columns of interconnecting metal. The densest member of the family at initial introduction, the QL16 \times 24, contains 384 logic cells in a 16 \times 24 array. According to QuickLogic, approximately a dozen equivalent gates out of each logic cell would be used in a typical application.

QuickLogic supports its devices with a Microsoft Windows 3.0-based environment (initial release will not support multitasking) on the personal computer. A database software architecture permits users to combine general-purpose third-party

VIALINK PROGRAMMABLE INTERCONNECT



QuickLogic's ViaLink interconnect in its new programmable ASIC devices is antifuse-based but forms a metal-to-metal connection. ViaLink programs at 10 V and has a resistance of less than 200 Ω and a capacitance less than 1 ff.

processors, pASICs have input-to-output combinatorial function delays of less than 15 ns and a quiescent current of just 2 mA typical. David Laws, president and CEO of QuickLogic, says a complex 32-bit counter operates at 90 MHz and draws just 100 mA max. from the supply.

The obvious comparison for ViaLink is the dielectric antifuse approach taken by Actel (Sunnyvale, CA). Though a programming current applied to Actel's dielectric antifuse-based FPGAs also creates a hard-wired interconnection, the interconnect resistance is still about

Introducing Canon's Wide-Body Jet



The P-670 Bubble Jet. A High-Quality, Low-Cost, Wide-Format Printer Engine for OEMs.

Now you can offer your customers the performance of large-format laser printers and electrostatic plotters...at a fraction of the cost.

The P-670 Bubble Jet printer engine delivers crisp, laser-quality output at 360 dpi on plain paper up to 17" wide (C-size). Able to handle cut sheets and fanfold paper, envelopes and transparencies, it's the most versatile personal printer/plotter for CAD/CAM, business graphics, spreadsheets, desktop publishing and poster printing.

The P-670's patented, 64-nozzle print head delivers 300 cps, or 6.7 letter

size pages per minute* with whisper-quiet, non-impact printing (less than 45 dbA)...and Canon's proven reliability. All of which assures you first-class, non-stop performance.

Canon offers OEM printer technologies for today's needs and tomorrow's growth. Find out how Canon's leadership and innovation can work for your company.

**Call 1-800-323-0766 for an
OEM information kit.**

Canon[®]
OEM Operations/Printer Division

CIRCLE NO. 30

*High Speed Mode
©1991 Canon U.S.A., Inc. Canon is a registered trademark of Canon, Inc. Illustration printed on the P-670 in High-Quality Mode. For information write Canon U.S.A., Inc., OEM Operations, Printer Division, One Canon Plaza, Lake Success, NY 11042.



INTEGRATED CIRCUITS

An old argument: Can amorphous silicon conduct?

More than two decades ago, Stanford Ovshinsky began theorizing that amorphous silicon could match and exceed the semiconducting performance of expensive, carefully grown silicon crystals. The scientific community ridiculed Ovshinsky for his belief that an amorphous material, with atoms scattered randomly, could conduct electricity, and difficulty in manufacturing Ovshinsky's "glass transistors" did little to lend credibility to his claims.

Ovshinsky did not let his detractors discourage him. The amorphous silicon-based, electricity-generating solar cells he makes at Energy Conversion Devices (Troy, MI) are attracting worldwide interest. The thin-film technique used to make the solar cells could be adapted to produce ICs, Ovshinsky says.

He has at least been recognized in the dictionary; the "Ovonics" entry credits the first two letters of the word to Ovshinsky's name. Ovonics is defined in *Webster's Ninth New Collegiate Dictionary* as "a branch of electronics that deals with applications of the change from an electrically nonconducting state to a semiconducting state shown by glasses of special composition upon application of a certain minimum voltage."

tools with architecture-specific tools. Initially, the pASIC toolkit contains the CAD/CAM Group's Engineering Capture System for schematic capture, and Silicon Automation Systems' X-SIM simulator, as well as QuickLogic's own Seamless pASIC Design Environment (SPDE, pronounced Speedy).

Simulated annealing

The SPDE tools include automatic place and route, modeling, and automatic test vector generation. Placing and routing a pASIC can be done at the rate of 1,000 gates/15 min, according to Birkner, who says that the software is based on simulated annealing technology out of the University of California at Berkeley. At present, QuickLogic provides its own device programmer. QuickLogic communicates with third-party tools through a proprietary ASCII interface description, the QuickLogic Data Interchange Format, rather than through the EDIF (Electronic Data Interchange Format).

As QuickLogic releases information on its long-awaited pASICs, competitive device makers are doing

anything but resting on their laurels. Altera (San Jose, CA), for instance, is just now revealing architecture details of its 0.8- μ m CMOS MAX 7000 EPLD family. Parts with 10,000 and 4,000 gates will be introduced in the fourth quarter and the remaining members next year. High-end density is 20,000 gates, and in-system speeds have been boosted to 70 MHz from 50 MHz for MAX 5000 parts.

The MAX 7000 Programmable Interconnect Array has been enhanced to minimize additive delays associated with earlier devices. The improved interconnect introduces less than 2 ns of signal skew, compared with about 13 ns for

MAX 5000 parts. By removing EPROM elements from the direct signal path, Altera has reduced across-the-chip logic delays to 15 ns.

MAX 7000 devices have five dedicated product terms per macrocell (up from four in the MAX 5000). Additional product terms can be borrowed from adjacent macrocells through the use of *parallel* logic expanders, new with MAX 7000 devices. The incremental-delay penalty for using parallel expanders is 2 ns/macrocell, down from the MAX 5000 6- to 12-ns penalty for shared expanders, also available on MAX 7000 devices with a fixed 6-ns incremental delay. A programmable speed/power trade-off option for the MAX 7000 parts involves a 10-ns speed penalty for quarter-power operation. The devices are register-configurable as D, T, RS, or JK flip-flops.

The Windows 3.0-based MAXPlus II toolset that supports MAX 7000 designs includes a multitasking capability. According to Altera, a 5,000-gate design typically can be compiled in 10 minutes or less with

the new software. MAXPlus II also supports EDIF.

National Semiconductor (Santa Clara, CA) just recently announced a new electrically erasable CMOS PLD architecture that features a paged configuration, similar to that used in memories. The paged architecture of the 1,000- to 4,000-gate Multiple Array Programmable Logic (MAPL) family is aimed at sequential designs and consists of multiple PLAs interconnected via programmable macrostate registers and a global input bus. The macrostate register outputs have fixed feedback paths to the global input bus to determine which PLA "page" is enabled. Only necessary product terms are active and consume power, thus reducing current draw to 140 mA max.

The company guarantees a worst-case system speed of 45 MHz (with feedback) across the family of MAPL products. Programmable output macrocells can be configured to act as either DE-, JK-, RS-, or T-type flip-flops. National supports its MAPL architecture with its own Open Programmable Architecture Language software package.

Steadily mounting competition among complex PLD and FPGA vendors is making one-upmanship the order of the day. But architectural details and spec sheets aren't enough to popularize a particular family. That comes only after designs have been completed successfully, and the resulting silicon matches design specs. Hopefully, the newer architectures and more-sophisticated tools will let users design parts that perform as well as they look on paper. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Actel (408) 739-1010	Circle 239
Altera (408) 984-2800	Circle 240
National Semiconductor (408) 721-5000	Circle 241
QuickLogic (408) 987-2000	Circle 242
VLSI Technology (408) 434-3000	Circle 243



If you're tired of pouring on SRAM to
get 128Kbyte cache performance,

Take a load off.



Introducing an amazing new cache chip that gives crowded motherboards a new lease on life.

It's called 386™ Smart Cache, a family of chips that integrate a cache controller with up to 16Kbytes of SRAM onto a single, one-million-transistor chip. The result is a 16Kbyte chip that really cleans up, equalling the performance of 128Kbyte caches.

Intel's 386 and 386SX Smart Cache are one-chip solutions that give you extra space on your motherboards for other applications.

©1990 Intel Corporation. 386 is a trademark of Intel Corporation.

And when you stack them up against other caching solutions, you'll find their innovative architecture costs substantially less.

Give your motherboard a lift. Send in the attached card today for a free copy of our unique 386 Smart Cache video, performance report and documentation. Or if the card's been ripped off, call 1-800-548-4725, dept. HA47.

Because the reasons to look into 386 Smart Cache are really starting to pile up.

intel®

CIRCLE NO. 31

Supercomputer maker embraces standards

Warren Andrews, Senior Editor

Supercomputer maker FPS Computing (Beaverton, OR), formerly Floating Point Systems, has just announced its first supercomputer family that embraces a variety of industry standards from the Sparc processors to Hippi (high-performance peripheral interface) and VMEbus. And on the software side, the machine is fully Unix compatible. The supercomputer performance—533 Mips, 13.4 GFlops—is achieved using a combination of scalar, vector and matrix processors in the company's own massively parallel computer architecture.

And while much of the system incorporates standard architectures, the main processor bus handling the multiple processors, memory and I/O retains its proprietary identity. Unlike conventional backplane buses, the FPS 500 family of supercomputers uses what marketing vice-president Steve Campbell describes as a scalable interconnect architecture. The architecture is implemented in what he refers to as a "centerplane." The physical configuration is one in which the various processor, memory and I/O boards radiate off the centerplane much like spokes off a wheel. This also includes the memory system—a large hierarchical memory—and address translation and virtual caches.

Three types of processors share the centerplane: scalar, vector and matrix processors. Each processor is actually a group of parallel processors whose number is dependent on the application. The processors get their data from the main memory system and communicate to each other through the main memory.

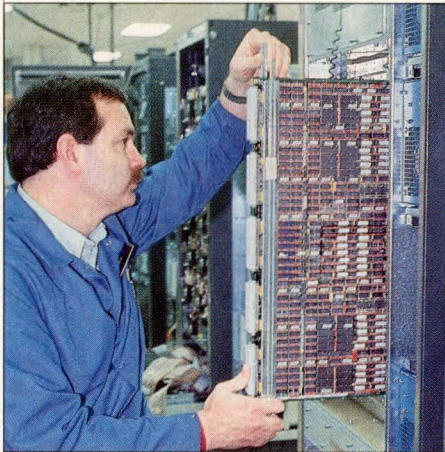
According to Campbell, the centerplane comprises four buses with an aggregate data transfer rate of better than 1 Gbyte/s. The centerplane handles the dual role of minimizing distances—and therefore propagation delays—between boards, and reducing the length of the backplane and therefore the linear dimension of the machine.

Campbell emphasizes that FPS'

500 series will provide supercomputer users GFlops performance with the support of key industry standards. And, he points out, the prime element in providing the type of performance required is the ability to match—through the correct combination of processor quantity and type—the processing power to the customer's needs.

■ Coprocessing allows scaling

Campbell defines FPS' multiprocessing approach as a coprocessor approach, rather than an integrated approach such as that used by Cray



The FPS 500 series can be configured with multiple scalar, vector and matrix processors to meet application requirements. By using a modular architecture, fielded systems are easily upgraded simply by swapping boards.

Research in its supercomputer. In Cray's approach, the scalar and vector processors are tied closely together, and to increase the number of CPUs, both vector and scalar CPUs must be incremented equally.

In FPS' coprocessor approach, the vector processor is treated as a coprocessor, so if more scalar processing power is required, only scalar processors are added. Similarly, if only vector processing is needed, additional vector processors can be added without disturbing the scalar

function. The coprocessor works like a shared memory-management-type connection where the scalar processor passes jobs across to the vector processor, freeing the scalar processor to do other functions and handle other parts of the application.

The system configuration—how many scalar, how many vector and how many matrix processors are included—in any given machine is determined by the particular application. In a scientific application, for example, says Campbell, more vector processors will be needed compared with a database management application, which would call for a higher component of scalar and matrix processors.

One key to operating in this coprocessing/parallel processing environment is that the operating system must know exactly how many of each processor are in the system. "The Unix operating system has full knowledge of the configuration of the machine, including how many and what kind of processor as well as the amount and type of memory," says Campbell. The Fortran and C compilers used in the system automatically generate vector code when the application calls for it.

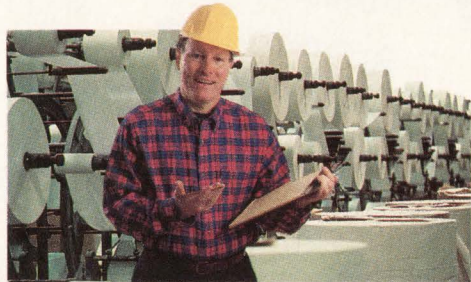
And while Campbell touts the efficiency of the compilers, he admits that in some intense applications it's possible for a programmer to boost efficiency even more by writing code such that it is best suited for the mix of processors. "In most cases, the machine configuration should be transparent to the programmer," says Campbell. "Programmers need simply to write standard Fortran or C code."

■ I/O plugs into standards

The I/O subsystem on the FPS 500 series is a memory-mapped I/O with various flavors of I/O types ranging from processors handling VME to the latest high-performance approach such as Hippi. "VME is pretty much the I/O standard in the industry for large computer systems to interface disks, tapes and standard peripherals of various technology," says Campbell. Hippi is targeted at 800-plus Mb/s (100-plus Mbytes/s) and is currently being considered as an ANSI standard.

In operation, the memory-mapped I/O is relatively simple.

LINE SCAN PROCESSOR CUTS INSPECTION COSTS IN HALF



"Our DT2856 is the only processor board designed exclusively for EG&G Reticon, Loral Fairchild, and other line scan cameras."

--Fred Molinari, President

Complete camera interface for PC AT

- Complete camera controls on boards
- 20kHz to 20 MHz sample rate
- Up to 8K pixels per line
- Works with single or dual channel cameras

Real-time processing

- Template matching for web inspection
- Run length encoding for fast measurement
- Binary compression
- Double buffered memory for fast data transfer
- 10 MHz DT-Connect™ interface to auxiliary processors

Compensates for lighting and sensor irregularities

- Gain & offset correction on pixel-by-pixel basis

FREE software

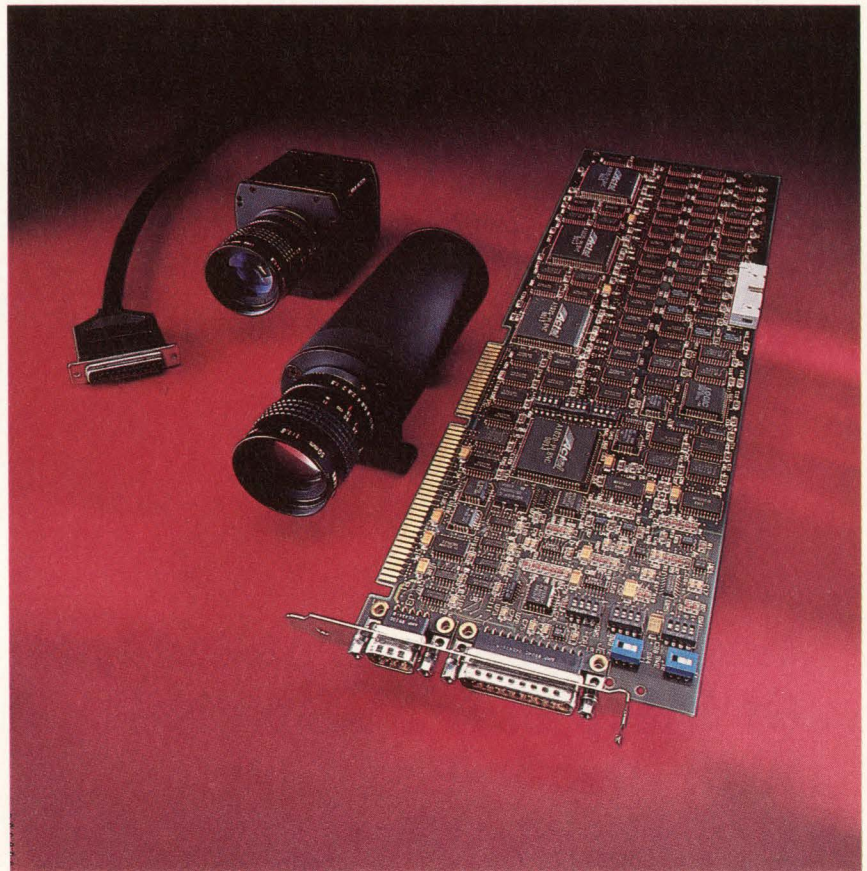
- Setup/calibration utility
- Driver and library

Quantity pricing available

Fast 5-day delivery

Call for FREE Catalog
(508) 481-3700

In Canada, call (800) 268-0427



Applications

- Inspection
 - Paper, Metals, Forest Products
 - Film, Textiles
- Document processing

DATA TRANSLATION®

World Headquarters: Data Translation, Inc., 100 Locke Drive, Marlboro, MA 01752-1192 USA, (508) 481-3700, Fax (508) 481-8620, Tlx 951646

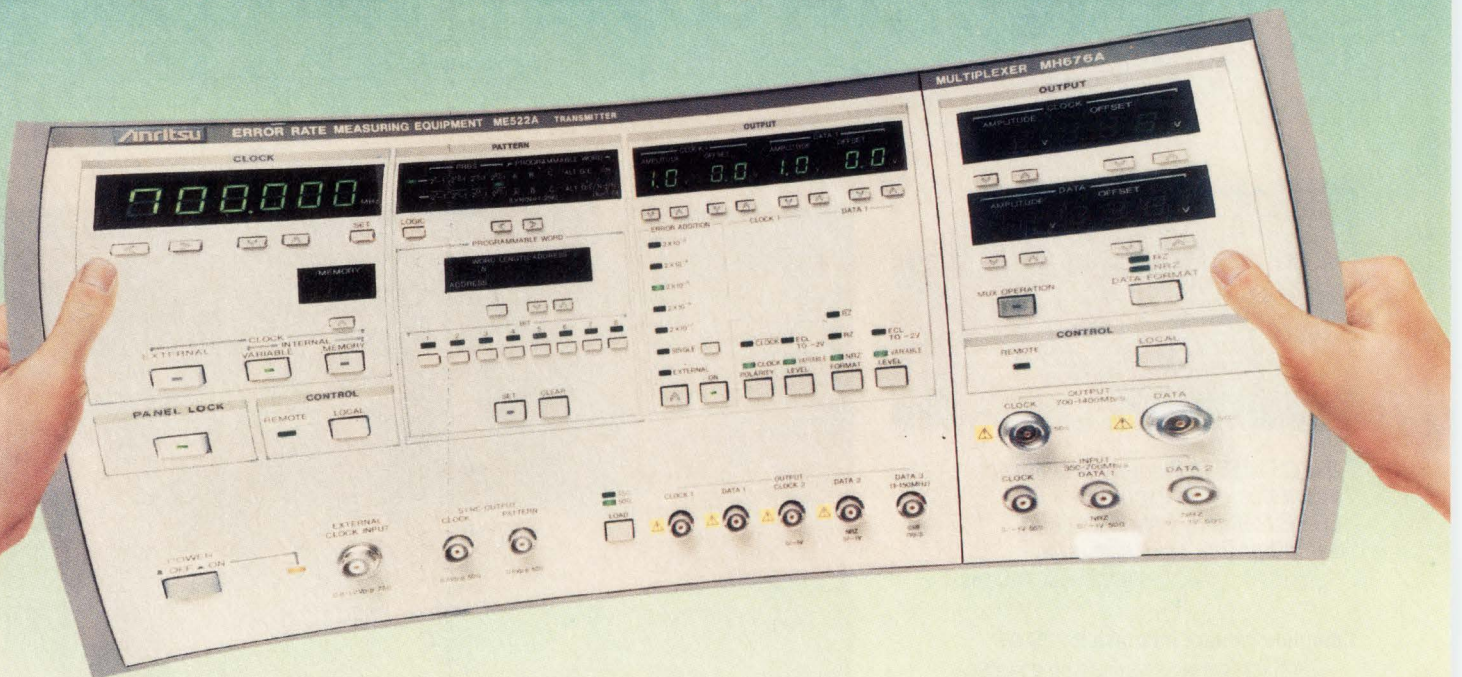
United Kingdom Headquarters: Data Translation Ltd., The Mulberry Business Park, Wokingham, Berkshire RG11 2QJ, U.K., (734) 793838, Fax (734) 776670, Tlx 94011914

Germany Headquarters: Data Translation GmbH, Im Weileren 10, 7120 Bietigheim-Bissingen, Germany 7142-54025, Fax 7142-64042

International Sales Offices: Australia (2) 699-8300; Belgium (2) 466-8199; Brazil 11 240-0598; Canada (416) 625-1907; China (1) 513-7766 x1222; Denmark 2 274511; Finland (0) 3511800; France (1) 69077802; Greece (1) 361-4300; Hong Kong (5) 448963; India (22) 23-1040; Israel 52-545685; Italy (2) 82470.1; Japan (3) 502-5550, (3) 5379-1971; Korea (2) 718-9521; Netherlands (70) 399-6360; New Zealand (9) 415-8362; Norway (2) 53 12 50; Poland (22) 580701; Portugal 1-7934834; Singapore 338-1300; South Africa (12) 803-7680; Spain (1) 555-8112; Sweden (8) 761 78 20; Switzerland (1) 723-1410; Taiwan (2) 3039836

DT-Connect is a trademark and Data Translation is a registered trademark of Data Translation, Inc. All other trademarks and registered trademarks are the property of their respective holders.

STRETCH YOUR BERT



Meet Changing Requirements Of Every BER Application With Plug-In Flexibility

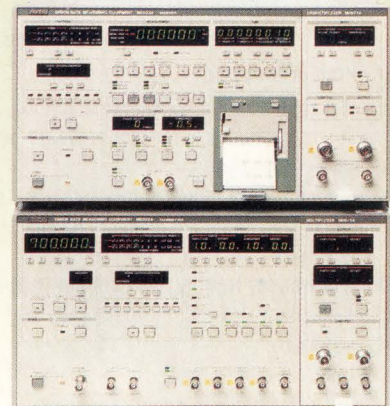
- 1 MHz to 1.4 GHz
- Synthesized Clock
- Multiple Patterns
- Multiple I/O Interfaces

The ME522A Error Rate Measurement Equipment covers a frequency range of 1 MHz to 700 MHz, and up to 1.4 GHz with plug-in MUX/DEMUX units. It provides abundant pattern generation capability and measurement functions, including PRBS to $2^{23}-1$, three words up to 2048 bits in length, mark ratio

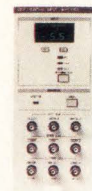
variable patterns, alternate patterns, and isolated patterns.

The ME522A is the most flexible solution to your BER measurement requirements, from component test to systems analysis and from low frequency rates to the optical requirements of SONET.

For a demo, application assistance or literature, contact Anritsu America, Inc., 15 Thornton Road, Oakland, NJ 07436. Call 800-255-7234 or (in NJ) 201-337-1111. FAX 201-337-1033.



DE-MUX



MUX



O/E



DIFFERENTIAL OUTPUT



DIFFERENTIAL INPUT



E/O

Anritsu

CIRCLE NO. 33

ANRITSU CORP., JAPAN

COMPUTERS AND SUBSYSTEMS

Basically the application program requests I/O, and the operating system posts a request for an I/O device to handle the operation. The operating system tells the I/O controller to perform the requested task and in-

FPS takes a RISC

FPS Computing (Beaverton, OR) is using the 64-bit ECL version of the Sparc chip made by Bipolar Integrated Technology (BIT). "We've worked closely with BIT for some time," says marketing vice-president Steve Campbell. "They currently manufacture our proprietary RISC chip, and we've worked with them on the Sparc implementation. The part we're using is the fastest Sparc chip on the market today.

"We selected Sparc for a number of reasons," he says. "We looked at Motorola, Intel, MIPS, and Sparc as primary candidates for RISC chips. Motorola and Intel fell by the wayside very early. On the surface it looked like MIPS might have had some early technology advantage. But when we looked at Sparc with the same detail, we found that Sparc and MIPS essentially became a wash in terms of technology.

"What really made the difference was the number of applications, systems software and tools readily available and in the market already for the Sparc architecture," he says. "Quite frankly these are not available for MIPS. While there are some major vendors of MIPS machines such as Silicon Graphics and Digital Equipment Corp, there's no compatibility at the software level between those vendors. On Sparc, there's a clear ABI (application binary interface) compatibility between multiple vendors so it truly is possible to get access to a broad library of software."

terrupt the application when the I/O transaction has taken place. "This results in a very high-performance asynchronous I/O capability," says Campbell.

"On VME—including VME64—we're capable of increasing performance through such techniques as using disk arrays, where data can be written (read) to multiple disks over multiple controllers," he says. "In this way it's possible to gang together multiple VME controllers re-

sulting in an aggregate throughput greater than would be possible with a single device."

Even with these techniques, however, it's not always possible to achieve the types of data rates needed for many applications. "We have to go beyond that and look at things such as Hippi," Campbell says. "In addition to conventional peripheral interface, Hippi is being developed for a variety of other applications. For example, it can be used for high-speed communication from one computer to another, or as a high-performance interface for disk arrays.

"We have a strategic relationship with Maximum Strategies, which is building a Hippi-based disk array that supplies some 30-plus Gbytes of storage at something like a 120-Mbyte/s data rate," he says. "This will be interfaced to the FPS 500 through a built-in Hippi connection.

"There's a lot of 'rational' speculation that more and more high-end systems will be interfaced to Hippi as a means to get access to high-performance data and share data between systems. Further, work with vendors such as Network Systems Corp developing Hippi switches is making it possible for a single machine to talk to a high-performance switching system and have access to a variety of devices whether they be disk drives, computers, graphic frame buffers, or whatever."

With its advanced I/O capability coupled with a flexible massively parallel compute engine, the FPS 500 series is at the leading edge of high-performance computers and servers currently available. Its strong advocacy of industry standards make it an attractive alternative to strictly proprietary solutions. Futurebus+ based solutions, however, are expected to be announced as early as later this year boasting the same type of performance, only with a standard processor/memory bus substituted for FPS' centerplane. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

FPS Computing
(503) 641-3151 Circle 219

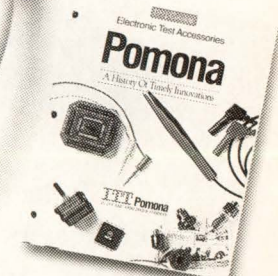
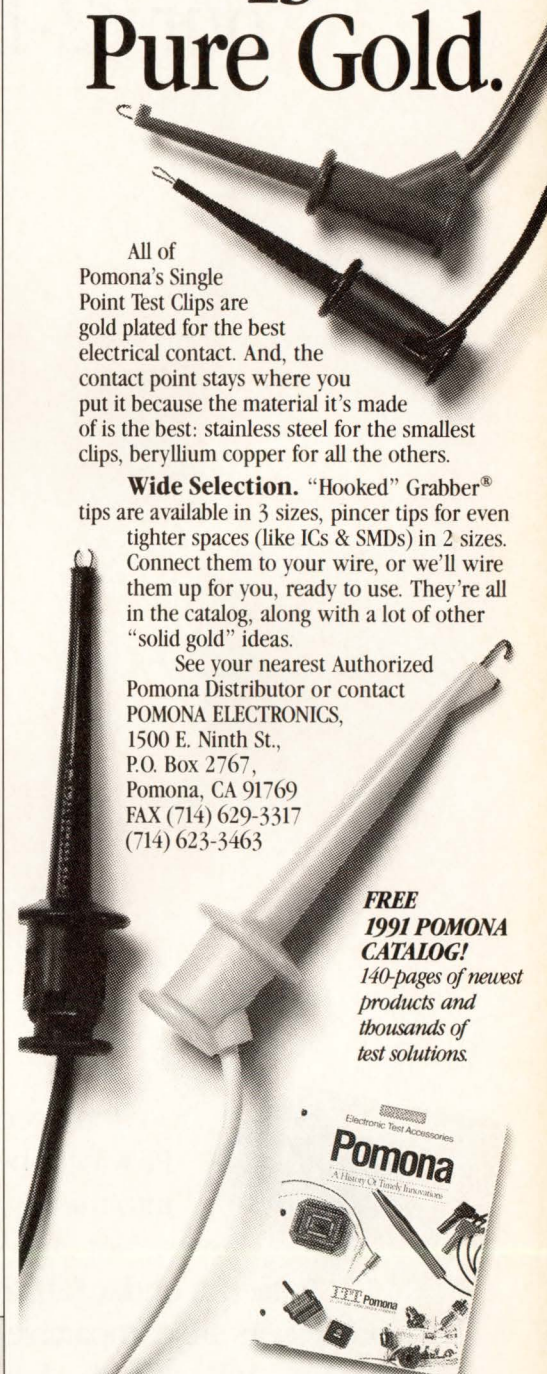
The Point We're Making Is Pure Gold.

All of Pomona's Single Point Test Clips are gold plated for the best electrical contact. And, the contact point stays where you put it because the material it's made of is the best: stainless steel for the smallest clips, beryllium copper for all the others.

Wide Selection. "Hooked" Grabber® tips are available in 3 sizes, pincer tips for even tighter spaces (like ICs & SMDs) in 2 sizes. Connect them to your wire, or we'll wire them up for you, ready to use. They're all in the catalog, along with a lot of other "solid gold" ideas.

See your nearest Authorized Pomona Distributor or contact POMONA ELECTRONICS, 1500 E. Ninth St., P.O. Box 2767, Pomona, CA 91769 FAX (714) 629-3317 (714) 623-3463

FREE 1991 POMONA CATALOG!
140-pages of newest products and thousands of test solutions.



CIRCLE NO. 34

ITT Pomona
AN ITT EMC WORLDWIDE COMPANY
Discover our strengths.

Surprisingly, it doesn't
cost much to move into
our 32-bit architecture.



You don't need a French
Provincial budget to move
into the i960™ SA/SB proces-
sors. Not even close.

In fact, at under \$20, the i960 SA/SB
processors are comparable in cost to a 16-bit
system. And yet, with a full 32-bit internal
architecture and a 16-bit data bus, they give
you five to six times the performance of any
other 16-bit embedded processors.

Or in other words, for almost nothing
down you can own an impressive new home.
With an architecture that's perfect for today's
more demanding applications, such as entry-
level page printers, I/O controllers, and com-
munication products.

Naturally, when you move up to a 32-bit
architecture, you want to be sure it's a place
where you can stay and grow. Which is why
you'll be happy to know that the i960 SA/SB



processors are part of a close-knit neighborhood of Intel SuperScalar i960 microprocessors. So you get software compatibility across the board as well as an easy performance path up to 100 MIPS.

And while great price performance and compatibility are important, they're not the only reasons some very important companies have already moved into the i960 line. They were also impressed with the compre-

hensive array of development tools and the outstanding technical support that made them feel right at home with the technology.

So when you are ready to move into the i960 SA/SB line, call 800-548-4725 and ask for the 960 Welcome Guide. We'll not only make the move less expensive, we'll even help you set up.

intel[®]

CIRCLE NO. 35

Single-chip DSPs invade SBus

Warren Andrews, Senior Editor

SBus is rapidly becoming host to a variety of digital signal processing chips and data acquisition functions despite the limited board area (about 3x5 in.) and low-power budget allotted to the normally space-consuming, power-hungry functions. Ariel (Highland Park, NJ) offers two fixed-point boards based on Motorola's 56000 24-bit chip and one based on AT&T's DSP32C 32-bit floating-point chip. In addition, Vigra offers a 56000-

TMS320C30 in the near future and, not too far down the road, squeeze the 96000 into an SBus form factor." And Sonitech's sales and marketing manager, John Collins, reports active plans under way to plant TI's next-generation DSP chip, the TMS320C40, on an SBus platform as soon as it's available.

But the integration of such complex floating-point functions on a tiny card requires a lot of design and manufacturing magic. The main

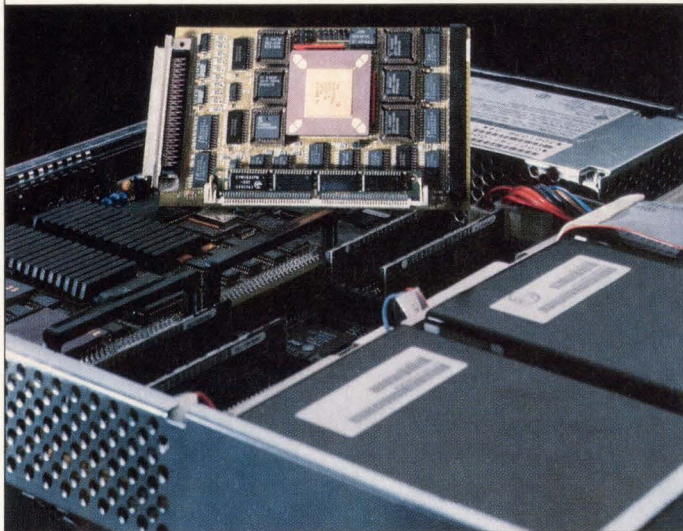
Sales estimates of SBus boards for 1991 range from a high of about \$9 million to a low of a little over \$3 million. But interpreting these numbers as an indication of option card design activity requires some understanding. The market for SBus boards is different from that of other standard-bus boards because it's exclusively an I/O board market. In looking at other buses such as VMEbus, STD Bus or Multibus, the total market figures usually include the value of all hardware and software, including backplanes, cardcages, power supplies, and standard, real-time or DOS operating systems. In addition, the traditional buses offer CPU boards as well as I/O. For SBus, the figures include only the I/O boards. All other functions, including CPU boards and other system components, are considered part of the "host" computer.

Still other factors have an impact on total market figures. SBus, for example, is relatively new to the market and still near the top of its cost/volume learning curve. And SBus poses technical challenges, some of which will be overcome over time. SBus option board manufacturers are not yet supported by readily available ICs that integrate critical functions; only a single DMA controller chip, for example, is currently offered for SBus boards. And the postcard-sized board so limits available real estate that many ASICs will have to be developed to make option boards functional. All this means that early boards are expected to be relatively costly at introduction but to slide quickly down the learning curve.

DSP board makers hope to cash in on some of the business as Sparcstations are used in increasingly more scientific and industrial applications. Some caution, however, that the performance advantage currently enjoyed by the Sparcstation may be eroded by products such as the new EISA-based machine from Hewlett-Packard.

On and off the board

"When you're talking about something with the processing power of the 320C30, one of the critical factors is being able to keep feeding the DSP data," says Sonitech's Collins. All the DSP boards offer some provi-



Sonitech's SBus DSP board is designed to take only a single slot. In many cases, as illustrated, two of the three standard Sparcstation slots are taken by double-width SBus boards such as the frame buffer shown.

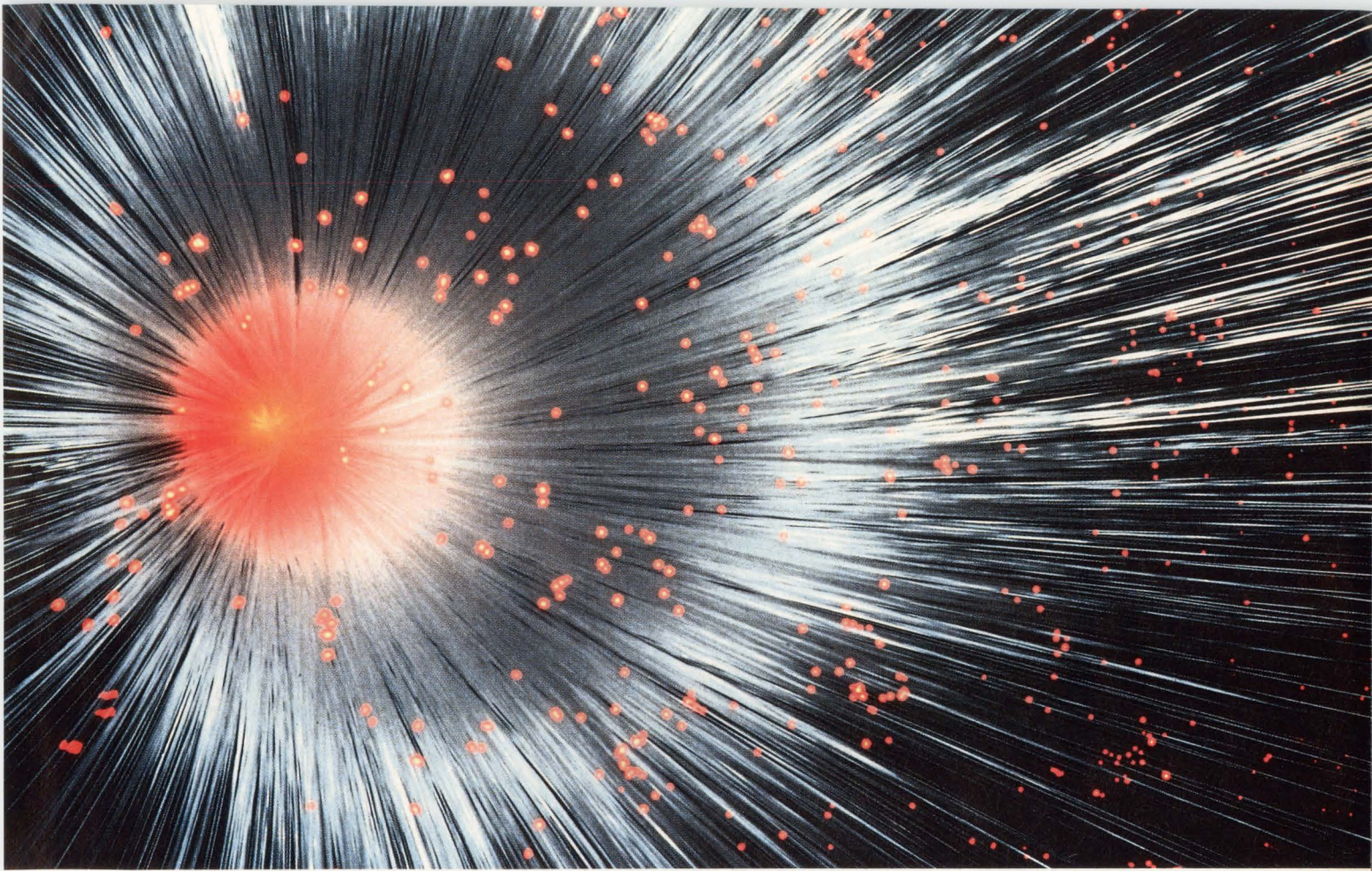
based board with data acquisition circuitry on-board intended for hi-fi audio interface applications. Lockboro has announced an SBus card based on Texas Instruments' 320C31, a scaled-down version of its 320C30. And most recently, Sonitech International (Wellesley, MA) introduced a high-performance SBus card based on TI's 320C30.

But that's just the beginning. Almost every manufacturer represented has plans to expand its SBus DSP offering soon. And undoubtedly some newcomers are ramping up for entry into the field. Sky Computers, for example, has already introduced an i860/i960 coprocessor board and will undoubtedly migrate some of its other DSP technology to SBus. Ariel's director of marketing, Les Listwa, says, "We plan to put together an SBus board based on the

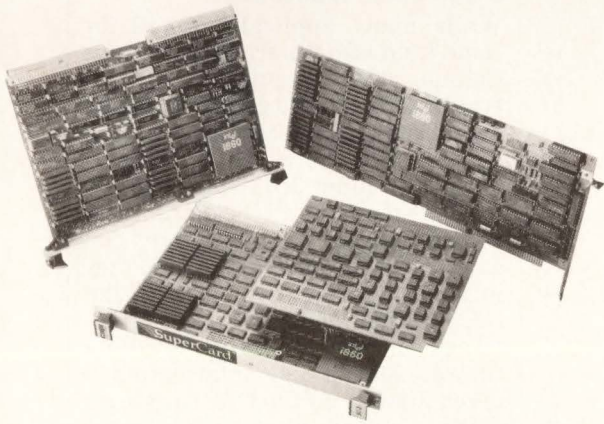
DSP chip, connectors and memory take up almost 90 percent of the board area, leaving precious little real estate left for bus interface and boot functions. In fact, to bring memory up to the requisite megabyte, Sonitech had to resort to a plug-in memory module positioned over other components.

An I/O board market

"We've seen a tremendous response to our SBus board, particularly in applications where customers need to work with real-time data on a Sparcstation platform," says Collins. Ariel's Listwa shares Collins' enthusiasm but observes, "We've seen a lot of interest and inquiries, but sales are just now starting to ramp up." But even early results indicate that SBus will be a winner in both commercial and industrial markets.



Speed + Performance . . . *The SuperCard™ Family of i860 Vector Processors*



The second generation of i860-based SuperCards™ is here... vector processors with GigaFLOPS system capability, concurrent I/O via secondary buses, large math libraries, FORTRAN and C development software... and, best of all, the *best price* on the market. The SuperCard family is compatible with VMEbus, ATbus, EISAbus and TURBOchannel platforms for hosts like Sun, HP, Motorola, Compaq, and DEC... here's what you get:

- 1024 complex FFT in 0.8 msec.
- 80 MFLOPS to 1.5 GFLOPS
- 160 MB/sec I/O
- Large memories
- pSOS+ Multiprocessing
- CASE Tools

CSPI

To find out how SuperCard can work for you, call: 1-800-325-3110 or 617-272-6020, (Fax 508-663-0150) or write CSPI, 40 Linnell Circle, Billerica, MA 01821.

SuperCard is a trademark of CSP Inc., i860 is a trademark of Intel Corp.
TURBOchannel is a trademark of Digital Equipment Corp.
pSOS+ is a trademark of Software Components Group, Inc.

CIRCLE NO. 36

COMPUTERS AND SUBSYSTEMS

sion in addition to the computer bus to get data on and off the board. Ariel uses what it calls its DSP Port, which a number of DSP companies using the 56000 have standardized. It essentially brings out the data pins of the processor, letting it rap-

idly take and output data.

Sonitech provides a similar port using one of the TMS320C30 parallel ports to get data on and off the board. In addition, the serial ports of the DSP chip are brought out to the same connector. "We're in the

process of designing an external SCSI interface—and perhaps other interfaces—to let users simply stream data off the DSP board," says Collins. "First, we need to do this externally because we can't really be sure of having another SBus slot available to tie SBus cards together internally. Many of the applications we've seen use a double-width SBus frame buffer or other function card leaving only a single SBus slot for additional adapters."

The need for getting on and off the board is driven primarily by the broad variety of applications in which DSP boards are used. Many applications call for some kind of spectrum analysis, which requires digitizing an analog signal and processing the resulting data. Sonitech, Ariel and other companies offer a stand-alone digital-to-analog/analog-to-digital converter to handle the job. "The product we offer is a 16-bit data acquisition box, which interfaces directly with our SBus card," says Collins.

But the reason for keeping the data acquisition section separate from the workstation and the DSP board involves more than simply the number of slots available. With 16 bits of resolution—approximately 1 part in 65,000—the noise within the workstation's enclosure, and coming in through its power supply, tends to greatly reduce the available resolution, says Collins.

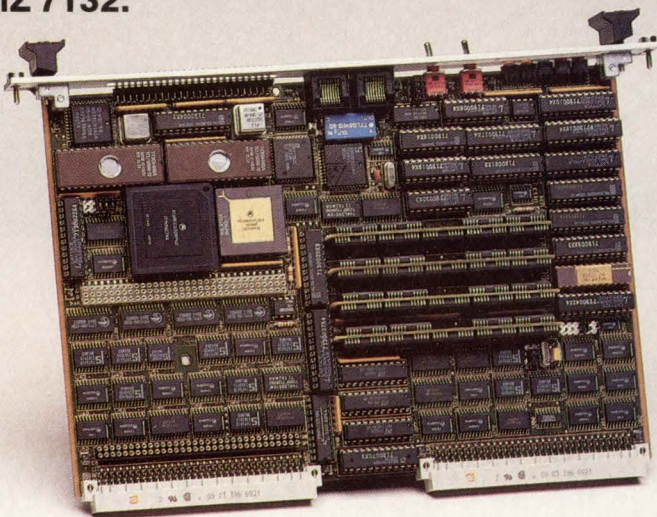
Still other applications

While many applications call for some kind of data acquisition, says Collins, others require a different type of I/O capability. "For example, one of our customers uses our DSP board to perform vibration analysis of an oil-welling drill head to eliminate the need to pull the cutter head up for frequent examination," he says. "In addition to the 'go-no go' information on the drill head, all the information is logged and maintained as part of the well-drilling record." In this case, information is taken directly off the DSP card to an SCSI adapter where it's permanently logged on disk.

In still other areas, says Ariel's Listwa, DSP boards are used as accelerating coprocessors for the workstation. The data being processed can be anything from speech analy-

Super Cache

Bring your entire application aboard Mizar's MZ 7132.



If your application requires not only superior 68030 performance, but plenty of on-board memory, Mizar's MZ 7132 is the answer. An economical, yet powerful, VMEbus single board computer, the MZ 7132 provides 16 Mbytes of dual-ported memory as well as a 16 Kbyte cache. Now, you can implement your memory-intensive applications more efficiently by avoiding the performance degradation of off-board memory. And, if you need more than 16 Mbytes, treat the on-board memory as a large cache and use the MZ 7132's optional VSB interface to access an additional memory pool.

The fully-featured MZ 7132 includes a 68EC030 or 68030 CPU with on-board SCSI, serial I/O, and optional Ethernet. OS-9™ and VxWorks™ support is also available. For more information on the MZ 7132 and other Mizar products, call today: 1-800-635-0200.

MIZAR

1419 Dunn Drive/Carrollton, Texas 75006/214-446-2664/FAX 214-242-5997

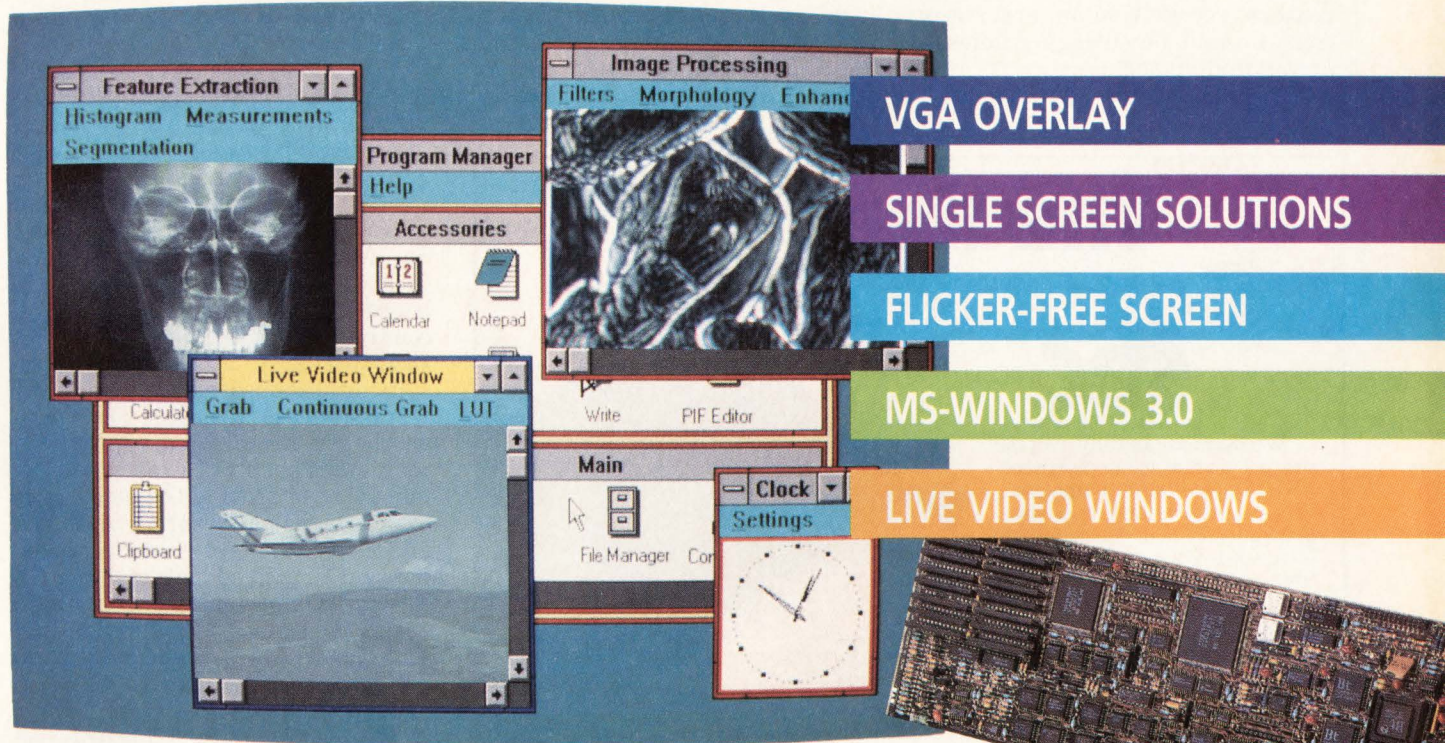
© 1991 Mizar, Inc.

Mizar is a registered trademark of Mizar Digital Systems, Inc. Other names are trademarks of their respective manufacturers or developers.

CIRCLE NO. 37

IP-8

THE NEW LOOK IN IMAGING



Matrox brings a new look to imaging applications with IP-8, a flexible low cost frame grabber and display controller for PC AT based systems.

IP-8 delivers this new look with features like VGA overlay, display resolutions up to 1024 x 768, flicker-free screen, and MS-Windows 3.0 or custom user interfaces running in the VGA overlay. In addition, IP-8 accepts up to four RS-170 or CCIR input sources, and multiple memory access modes accelerate imaging algorithms.

IP-8 is the cost effective solution for OEMs and end users. With extensive software tools and 3rd party packages, you'll cut development time and implement the new look in image analysis, scientific imaging, inspection and medical applications...fast.

The new look will change your view.

**1-800-361-4903
or (514) 685-2630**

Matrox is a trademark of Matrox Electronic Systems Ltd., MS-Windows is a trademark of Microsoft Corporation. AT is a trademark of International Business Machines Corporation.

matrox

PRODUCTIVITY, PERFORMANCE . . . VISIBLE SOLUTIONS

CIRCLE NO. 38

IP-CD/0191

COMPUTERS AND SUBSYSTEMS

sis to specialized math processing. Still other applications are just opening up, including image and pattern recognition in everything from human physiology studies to automated inspection.

"Still many of our applications lie

in audio," says Listwa, "and we're in the process of developing a 16-bit A-D, 20-bit D-A SBus card just for such applications." Though he anticipates that some of the noise from the computer system may compromise the final resolution, he says the

company offers a personal computer-based product that provides about 90 dB signal to noise. He expects the SBus card to do as well.

Not just for desktops anymore

Though SBus DSP boards are starting to ramp up in volume, they're just touching the edge of the emerging market. According to Peter Palm, product line manager for Sun board/embedded systems products at Sun Microsystems (Mountain View, CA), Sun is doing a brisk business in board-level Sparcstations and will continue to ramp up as companies such as Foxboro begin to use Sparcstations as embedded computers.

A number of dedicated SBus add-on chassis are also emerging from companies such as Texas Microsystems. These provide the electronics to interface to an existing SBus slot and three—or more—additional expansion slots to add adapter boards. The major limitation to that approach is that the memory is mapped to only the original slot, and, depending on the expansion option card(s), memory space could be restricted.

Sun also offers its 1E board—essentially a Sparcstation on 6U VME that's second-sourced by Force Computers (Campbell, CA). Force will also be developing a 2E Sparcstation II equivalent board to be released soon. Both of these single-board computers will work with a two-board SBus/VME adapter board introduced by Sun at Buscon '91/West.


With Sparcstations starting to invade the industrial marketplace, there will undoubtedly be a growing need for all varieties of I/O cards, from multiple serial channels to parallel I/O and from low-resolution data acquisition to all varieties of frame grabbers right through and beyond many of the DSP functions just emerging. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

- Ariel (201) 249-2900 Circle 251
- Force Computers (408) 370-6300 Circle 252
- Sonitech International (617) 235-6824 Circle 253
- Sun Microsystems (415) 960-1300 Circle 254

NEW FOR VME

The Next Generation SBC



We listened carefully over the past 12 years as we've pioneered VME Single Board Computers. We now present the V36, a new generation of higher-performance, lower-cost SBCs designed for real-time applications.

The V36 Features:

- 68030 MPU at up to 40 MHz
- SCSI Interface with a 32K Buffer
- 8 Channels of Serial I/O
- Ethernet™ with local dual-ported, battery-backed SRAM
- 2 or 8MB of two-way interleaved DRAM with burst access
- Up to 2MB of EPROM
- Battery-backed Real-Time Clock
- Optional 68882 Coprocessor
- Pin Compatibility with Motorola MVME147
- 68040 Version Available

Priced Under
\$1800 in
OEM Quantities

Triple Local Buses for High-Performance

Through the use of buffers and component level DMA, the CPU, Ethernet and SCSI can operate simultaneously and independently for maximum performance and collision-free operation.

Expandable

Additional features can be added to the V36 via a local expansion bus, allowing system designers the flexibility to include proprietary features in an off-the-shelf computer, further reducing design costs.


Designed for Design-In

The V36 was designed for use in enclosed systems. All I/O on the board is routed through the P2 connector, which means no cable hassles during board swaps and upgrades. Additionally, the V36 makes extensive use of CMOS components, guaranteeing low overall power use (7W typ.) and the absence of "hot spots". The V36 can be used without a cooling fan in most applications.

Software Support

Software support is available for all major real-time operating systems, including VxWorks, OS-9, PDOS AND PSOS+.

Call today to learn more about the V36 SBC, and our complete line of VME CPUs, I/O and memory boards.

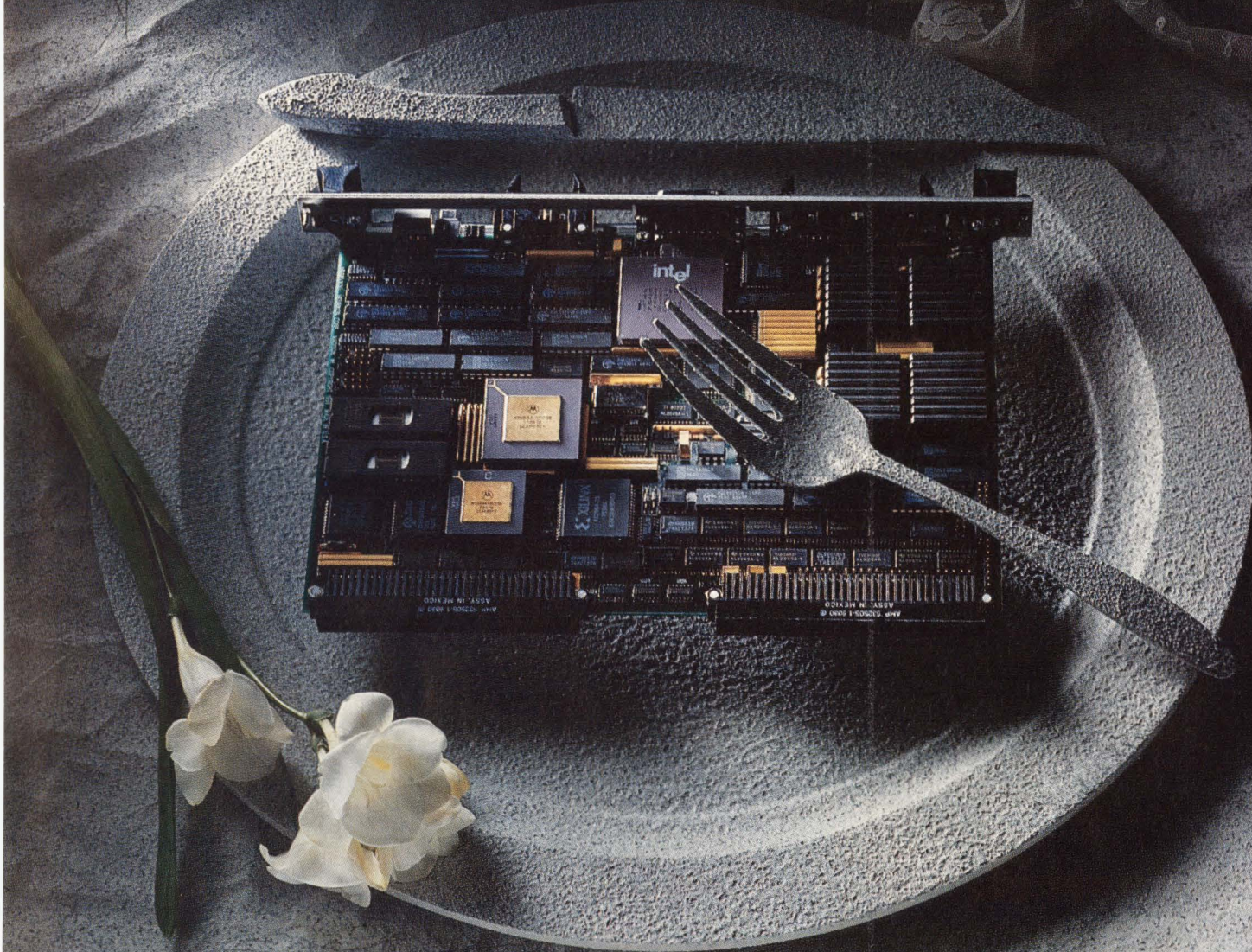


GENERAL MICRO SYSTEMS INC.

4740 Brooks St., Montclair, CA 91763 (714) 625-5475 FAX (714) 621-4400

VME ala Card

\$1795



VME performance at a price you can sink your teeth into! Heurikon's HK68/V3D offers VME standardization and design flexibility with a 33 MHz Motorola 68EC030 and 2 Mbytes of memory for only \$1795 (less in quantity). That makes the V3D a cost efficient entry point into VME single-board computers. As a complement to our main course, you can add more memory, SCSI or Ethernet. VxWorks and OS-9 are also available.

While our price indicates good value, it's our service which makes that value great. Our VME boards, real-time operating systems and software development environments are backed by superior technical support before and after the sale. The Heurikon V3D is the first in a series of new 680X0 value priced entrees. If you're hungry for more information, give us a call. **1-800-356-9602**. Bon Appétit.

Partners in Real-Time
HEURIKON
CORP.

Outside the U.S., call 608-831-0900 or FAX 608-831-4249. VxWorks is a trademark of Wind River Systems. OS-9 is a trademark of Microware Systems.

CIRCLE NO. 40

DESIGN AND DEVELOPMENT TOOLS

Analysis tools help digital designers avoid analog speed traps

Mike Donlin, Senior Editor

As microprocessor clock speeds climb beyond the 20-MHz mark, electrical connections no longer behave as simple pathways that conduct signals from one device to another; instead they're complex transmission lines subject to a range of faults—namely crosstalk, ringing, time delays, parasitics, and impedance mismatches.

Because transmission line effects are getting worse and experienced analog designers are rare, sophisticated analysis tools are emerging that can simulate analog effects on digital circuits so that engineers can place components, connectors and cables for optimum performance. The Greenfield tool suite from Quantic Laboratories (Winnipeg, Manitoba), for instance, predicts faults by simulating the electrical effects of high-speed transmission lines on a variety of applications including printed circuit boards, hybrids and integrated circuits, as well as cables, connectors and other interconnect media.

The newest addition to the tool suite, BoardScan, is a circuit simulation tool that screens printed circuit board layout data and determines critical nets where crosstalk and signal integrity problems are likely to occur. The software calculates worst-case crosstalk, time delays and signal integrity parameters for critical nets. Results are then listed in a comprehensive net report. BoardScan makes these analyses by applying electromagnetic field principles to the traces, wires and interconnect media to determine their behavior. According to Quantic, this method is much more accurate than some analysis tools that rely on topographically rule-based violations.

"Many tools use heuristics as a rule of thumb and execute simple formulas to deduce where a circuit might run into trouble," says Quantic president Al Wexler. "We think that such estimates are a dangerous proposition. Our tool looks at a cross section of the circuit and calculates

the electromagnetic characteristics of that circuit. By analyzing those characteristics and calculating the fields, we can judge the mutual inductance and capacitance of a circuit."

Once BoardScan has identified the critical nets, they can be analyzed in further detail with the Greenfield simulator, which also includes a schematic and graphics editor that lets designers correct the offending circuitry and then resimulate. The latest version of the simulator, Greenfield 3.0, accepts Spice transistor-based models. In addition, Quantic's library of drivers and receivers now includes behavioral models for Fast, ALS, CMOS, Bi-CMOS, and ECL devices.

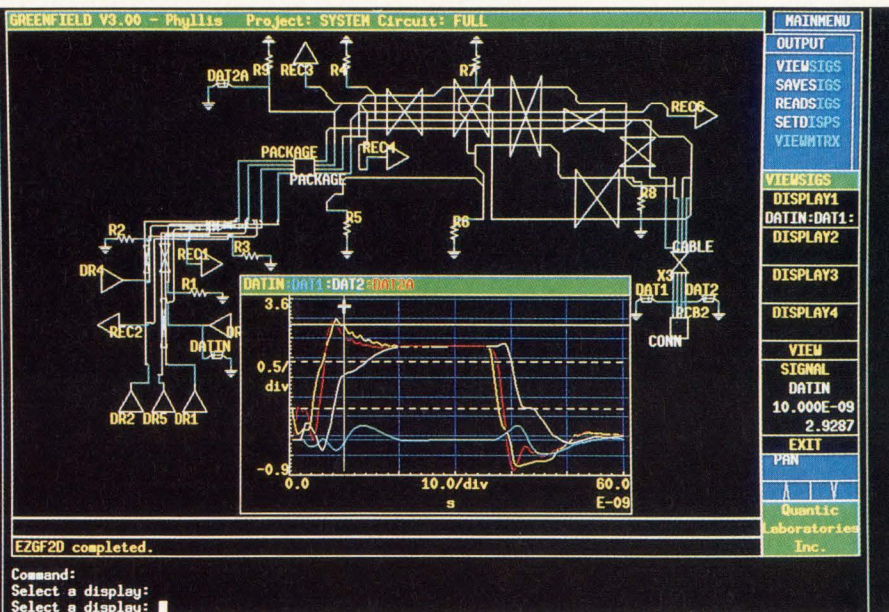
Details take time

A drawback to such detailed analysis, of course, is that it takes more time than a broad-brushed, topologi-

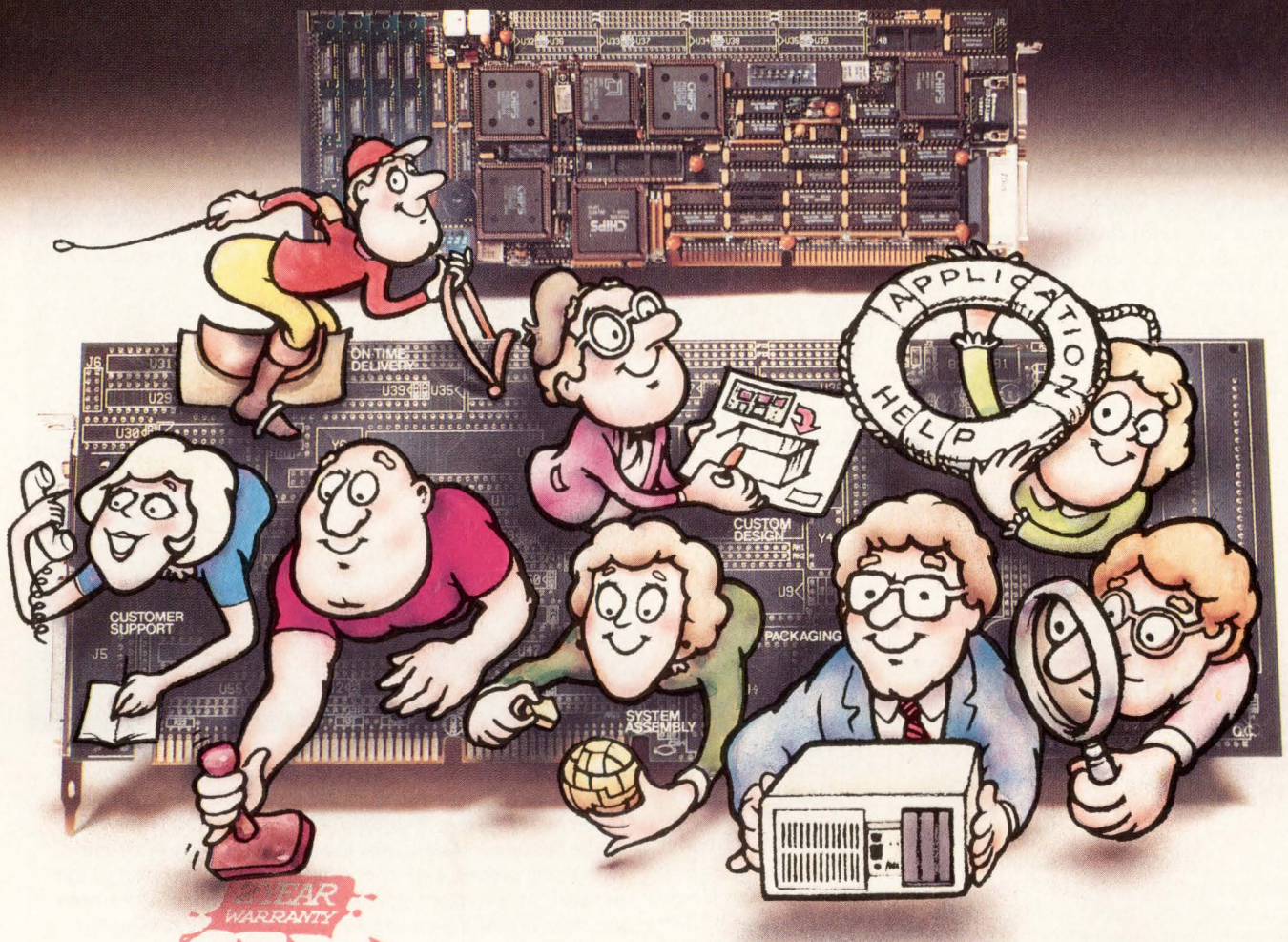
cal approach. "A field calculation does take time," says Wexler. "When you first run our tool, it's slower than less-sophisticated analysis tools. But it quickly builds a library when it finds identical or similar circuit configurations and, by referring to this database, gets speedier as the number of references increase. This way we don't sacrifice accuracy for speed. We think it's better to err on the pessimistic side for a more-extensive analysis."

In addition to building up libraries to increase calculation speed, there are other ways to increase a transmission line analysis tool's performance. The XTK Crosstalk Tool Kit from Quad Design (Camarillo, CA) uses enhanced calculation algorithms as well as stored libraries to improve performance.

"We've put a lot of work into our algorithms so that we can provide accurate circuit behavior predictions without undue time penalties," says Chuck White, vice-president of engineering at Quad Design. "The conformal mapping we do is similar to a Smith chart, which maps an infinite plane into a finite-sized plane. In essence, we warp space to do a finite computation. This means that we



Predicting the behavior of signals and crosstalk on complex circuits can help designers avoid costly rework of prototypes. In this example, Quantic Laboratories' Greenfield simulator models the propagation of a signal generated within a multichip module package passing through the leads of its ceramic package, across part of a printed circuit board, through a connector, and through a ribbon cable, and being received at another connector.



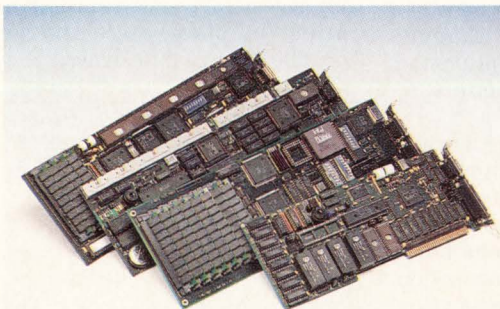
Take a Close Look at What's Behind Your PC CPU Board!

I-Bus has a lot more to offer the OEM and System Integrator than a family of CPUs with great price/performance. The I-Bus T.O.P.S.™ (Total OEM Program Support) Plan is designed specifically for OEMs and System Integrators:

- Engineering and Manufacturing Services
- Program and Project Management
- Peripheral Sourcing
- OEM Developers Program
- Life Cycle Support Program
- Unprecedented 2 Year Warranty

But that's only the beginning. We'll completely assemble and test your system (our boards and/or yours), modify or custom design an enclosure, and take it all the way to drop shipment to your customer.

We're 100% dedicated to the OEM and System Integrator, utilizing PC technologies in their application and products. Call today about the I-Bus OEM Developer's Program — a total support program that saves you time and cost in the design phase, and continuous support over the life of your system.



CPUs for the OEM and System Integrator

A286	8/12/16 MHz 80286 4 MB on-board DRAM Solid State Disk Option
J386SX	16 MHz 80386SX 4 MB on-board DRAM Floppy/IDE Hard Disk Controller
J386	16/20/25 MHz 80386 16 MB on-board DRAM
N88	10 MHz 8088 1 MB on-board DRAM Solid State Disk Option

I-BUS
PC Technologies

Call toll free
800-382-4229
Ask for our
new catalog!



I-Bus, 9596 Chesapeake Drive, San Diego, CA 92123 (619) 569-0646 FAX: 619-268-7863

CIRCLE NO. 41

DESIGN AND DEVELOPMENT TOOLS

don't have to specify boundary conditions or boundary sizes because we're effectively considering an infinite space in our analysis. Not having to take these boundary conditions into consideration makes a more efficient algorithm."

XTK uses the Crosstalk Field Extractor, which takes the designer's conductor geometry data to calculate signal line characteristics for all the traces in a given configuration. It also determines the degree of crosstalk and other distortions that will affect each set of parallel traces in a circuit network. Quad Design's

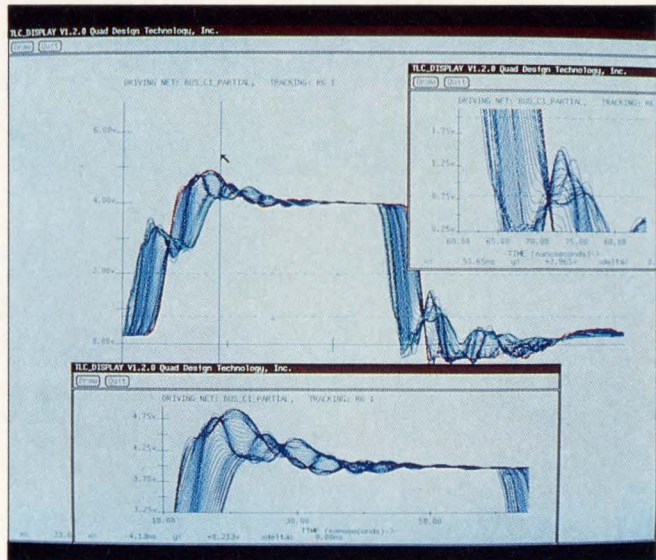
Transmission Line Calculator tool accepts postroute data as well as network topology information entered manually. It then analyzes all the nets in a design using the same database from which the design will be built.

The tool then calculates the effects of loading and circuit topology on system timing and determines resulting signal quality. Signal waveforms are displayed so the designer can analyze the expected behavior of the circuit. The signal information generated by these tools during component placement and routing can then be back-annotated into Quad's Modular Timing Verifier for comprehensive timing analysis at the system level. "Of course the watchword here is accuracy," White says. "So we actually represent detail inside the pixel so the finite elements displayed aren't simplistic representations."

Low-end tools available

Of course not everyone can afford the comprehensive analysis tools such as those from Quantic Laboratories and Quad Design. But even smaller design houses with lower-speed products can benefit from some sort of transmission line simulator. Personal computer-based tools are available, such as the LineSim from HyperLynx (Redmond, WA), that give preroute simulation information to assist designers in component placement.

The LineSim software is an interactive tool that predicts circuit response and calculates board trace impedance. The circuit to be simulated is specified in a schematic where users can select transmission lines, resistors and capacitors via a mouse. The simulation itself is dis-



Quad Design's Transmission Line Calculator simulates transmission line effects for a single circuit net or a complete digital system. This example shows the simulation of a printed circuit board system, including a backplane. The waveform in the background simulates the image of an oscilloscope with many probes, each connected to a different part of the network. In the upper right and at the bottom of the screen are close-ups of the waveform, which can be examined in detail. The tool also generates a report that summarizes error conditions.

Problems increase with speed

Engineers who design high-speed circuits are faced with a dilemma: if a circuit is designed too conservatively—that is, if traces are placed far enough apart to avoid transmission line effects—then the layout will be large and inefficient, and performance will suffer. If traces are close enough to ensure high-speed performance, then these effects can cause a circuit to malfunction. Therefore, the more information a designer can get about transmission line effects before committing a project to prototype, the less likely that expensive rework will be necessary.

Though these transmission line effects have always existed to some degree, they generally didn't cause too many problems in the larger, slower circuits of the last 20 years. And because these effects were easy to ignore, the analog design expertise that's needed today to combat them is hard to come by.

"Remember, not too long ago the computer industry decided that the world was made of ones and zeros," says Al Wexler, president of Quantic Laboratories (Winnipeg, Manitoba). "And there was a wholesale decimation of analog engineering courses in the universities. Then as processor speeds increased, analog effects started showing up in digital designs, and we started seeing the consequences of the lack of experienced analog engineers. As speeds increase and geometries decrease, these problems will only get worse."

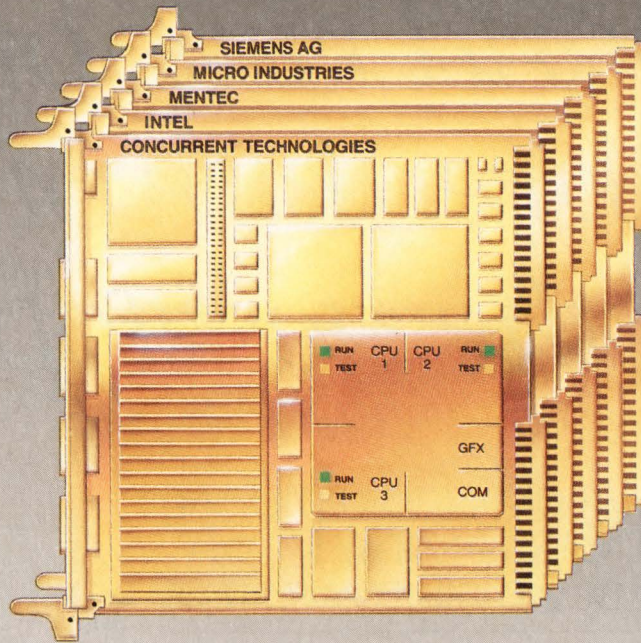
played in an oscilloscope format. To resimulate after a parameter change, the user modifies the schematic and replots. No recompilation or netlist step is required. The tool supports a library of digital devices that are modeled for device nonlinearities such as dynamic driver impedance and diode clamping. In addition, LineSim models printed circuit board trace geometries including microstrip, buried microstrip, stripline, and asymmetric stripline.

Though these tools offer varying degrees of accuracy and performance, they all have one thing in common—they give designers vital information during the place, route and simulation phase of circuit design. ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

- HyperLynx (206) 869-2320 Circle 216
- Quad Design (805) 988-8250 Circle 217
- Quantic Laboratories (800) 665-0235 Circle 218

Live Long.



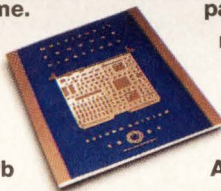
And Prosper.

MULTIBUS II

It is logical to choose the bus architecture that will deliver the greatest return on your development investment, for the longest possible time.

■ Today's Multibus II not only gets you to market quickly, with higher performance and superior reliability. But of all available buses, only Multibus II provides the performance headroom to effectively absorb silicon advances through the 1990s, to protect your investment long into the future.

■ During the past year Multibus II has grown faster than any other open architecture. One third more



vendors have expanded the range of available Multibus II boards, systems, software and packaging products by nearly 40 percent!

■ You can explore the world of Multibus II with your free copy of the new 1991 *Multibus II Product Directory*. Just send your business card to the MMG.

And, contact the enterprising manufacturers listed below for complete information on Multibus II products that will transport you into the future. ■ Discover Multibus II. Your application will live long. And you will prosper.

CONCURRENT TECHNOLOGIES

Jerry Hoffman 217-356-7004 FAX 217-356-6238
NEW! i486 CPU Board/Communications Controller

INTEL

Call 800-548-4725
NEW! High integration 33 MHz i486 CPU board

MENTEC

Ralph Shaw 800-446-6762 FAX 614-548-6184
NEW! i860-based SBC running UNIX System V Rel. 4



MULTIBUS MANUFACTURERS GROUP

MICRO INDUSTRIES

Bill Jackson 800-446-6762 FAX 614-548-6184
NEW! i960-based RISC development board

SIEMENS AG

Dr. Klaus P. Killian, Germany 089 4144 5737 FAX 089 4144 5841
NEW! Scalar CPU board with Hard-Realtime Unix

© COPYRIGHT 1991 MULTIBUS MANUFACTURERS GROUP

P.O. BOX 6208, ALOHA, OREGON 97007, 503-696-7155

“The world runs on infor silicon breakthroughs to right to the desktop.”

HOW NATIONAL SEMICONDUCTOR IS HELPING YOU MEET THE CHALLENGES OF TODAY'S — AND TOMORROW'S — DATACOM AND TELECOM SYSTEMS.

John Jorgensen, National's Director, Advanced Communications Business Group, talks about applying advanced VLSI technology to next-generation communications systems.

Setting the stage for connectivity.

“National has a definitive strategy for providing voice- and data-communications solutions in silicon.

“We have solutions for Ethernet, FDDI, and integrated-digital networks. And we're working on next-generation solutions for ultra-high-speed network applications.

“The key to building devices this sophisticated is our experience with advanced analog+ digital

integration. We have all the enabling technologies. BiCMOS, CMOS, and ECL processes. Powerful design tools. Experienced analog + digital designers.

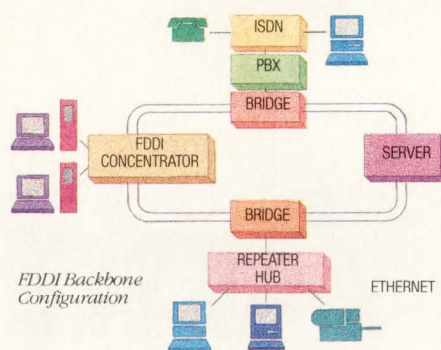
“It isn't easy. But we're doing it.”

Linking LANs with FDDI.

“Our FDDI chipset provides the backbone that links Ethernet LANs at the workgroup level with integrated-digital networks, such as ISDN and SONET— and it provides the high-speed datapipe that links workstations directly.

“We're the first manufacturer to introduce a fully-integrated FDDI solution. It offers more network management features and consumes less power than any other solution.

“Our latest device, called the BSI, provides the system interface between our core FDDI chips and the host-system bus, such as VME,



AT, Microchannel, or EISA. It gives you the maximum available system bandwidth, with burst-mode transfers of 800Mbits/second through a 32-bit-wide data interface — without the need for an external processor.

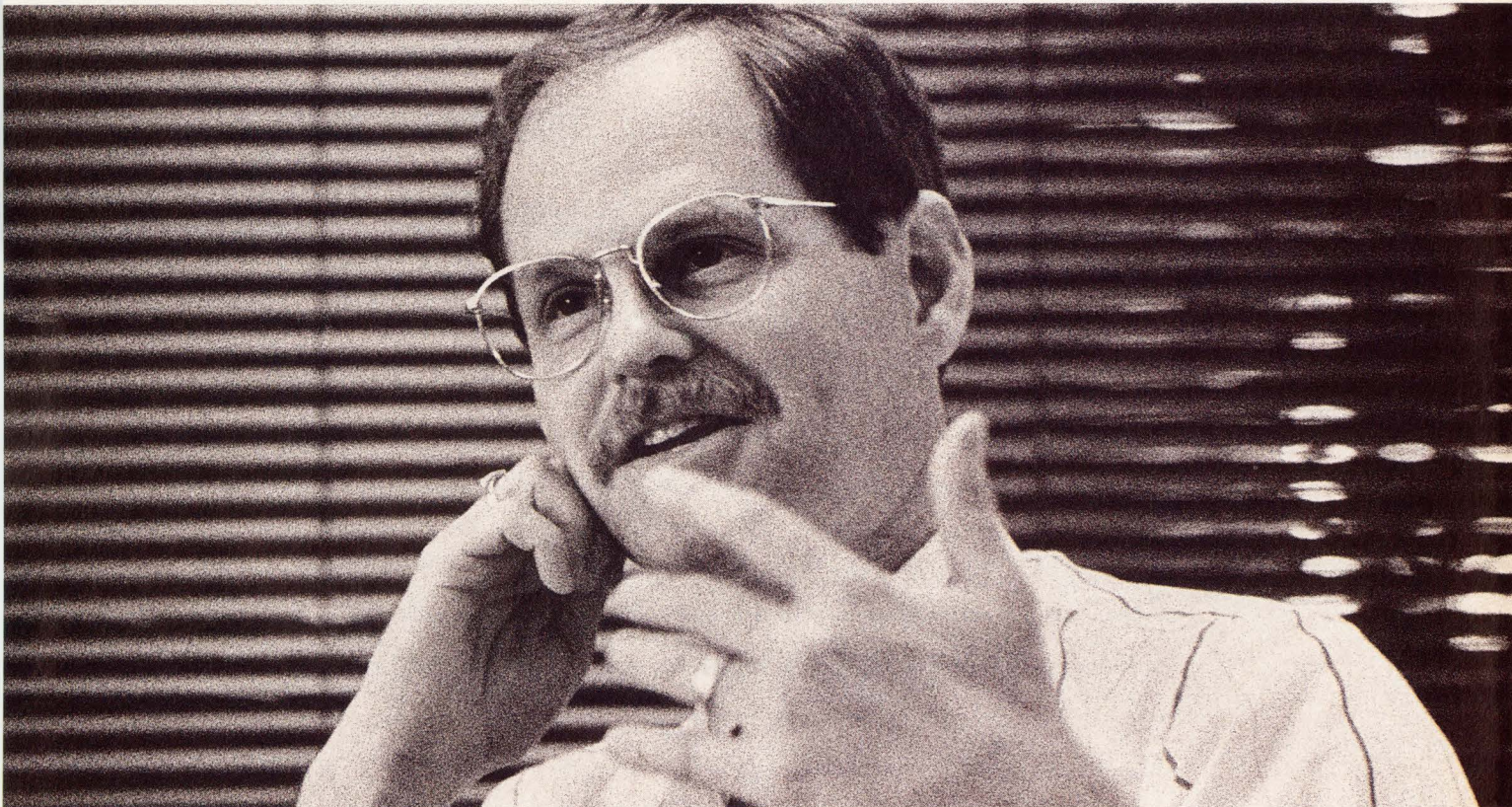
“So now you can develop products for highly-integrated FDDI networks, such as bridges, routers, and concentrators, or you can develop adapter cards for high-performance workstations and PCs — all from one supplier. National.”

Linking the workgroup with Ethernet.

“Our SONIC — Systems Oriented Network Interface Controller — integrates, for the first time, a digital controller with a 10Mbit/second analog encoder/decoder.



*mation, and we're making
bring that information*



"It supports all IEEE 802.3 functionality in a single chip that goes right on the motherboard in 16- and 32-bit systems, providing full network management functions in hardware.

"And with a transfer rate of 50 Mbytes/second, it's 20 times faster than most other solutions, and cuts bus occupancy by up to 80%.

"The workgroup is linking itself with Ethernet. And we're making it happen faster, smaller, and more cost effectively. That's the standard, and we're setting it."

Linking voice and data with ISDN.

"Our U interface breaks the ISDN logjam. It allows the simultaneous transmission of voice and high-speed data over the existing twisted-pair telephone network, providing the missing link between the subscriber and the central office.

"It may be the most technically complex mixed analog+ digital device ever designed. The receiving front-end is analog, but the back-end signal processing is all VLSI digital. And this had never been done before. Until we did it."

Putting it all to work for you.

"The communications revolution is accelerating. As a datacom or telecom systems designer, I'd feel the need for advanced solutions to tomorrow's problems *today*. That's why I'd call National. Because we have those solutions. Today."

1-800-NAT-SEMI, Ext. 115

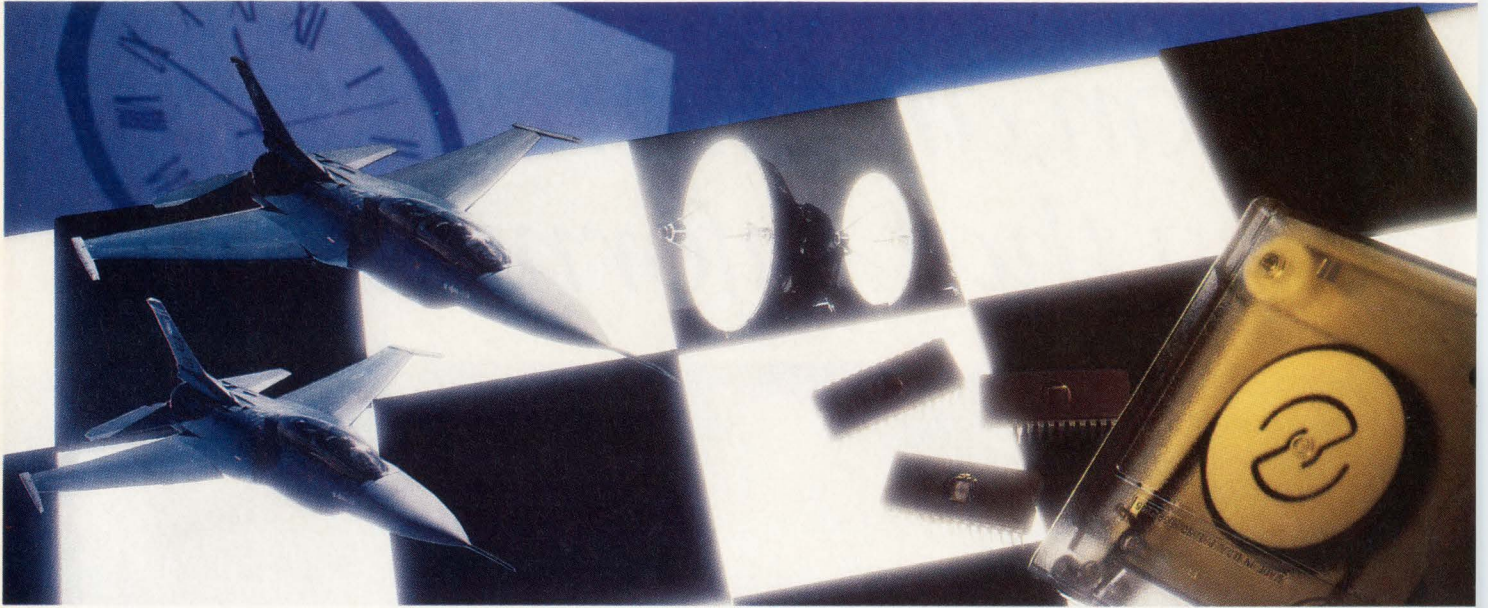


BSI, BMAC, CDD, CRD, PLAYER and SONIC are trademarks of National Semiconductor Corporation.

VME is a trademark of Motorola, Inc. AT and Microchannel are trademarks of International Business Machines, Inc.

© 1991 National Semiconductor Corporation

REAL-TIME STRATEGY



For Critical Minds and Systems

Your product is only as reliable as your embedded software. Which explains why real-time experts like you at over two thousand companies have made the strategic move to Software Components Group's real-time software and development tools.

Smart choice, since we offer you so many critical advantages. First, there's the famous quality and performance of our pSOS⁺ operating system, complete with superior multiprocessing and UNIX-friendly network support. Plus the best, most integrated development and debugging environment for your C or Ada application. And it's all available for the widest range of hosts – Sun, PC, VAX, HP, HP Apollo. And for all the popular processor families – M68K, M88K, i86, i386 and i960.

Best of all, when you're on the critical path, our service is just as friendly, reliable and complete as our software. We support you from seven U.S. offices and thirteen countries.

So whether your software is life-critical, mission-critical or just plain time-critical, call us at 1-800-458-pSOS for the winning real-time strategy. Or write to us at 1731 Technology Drive, San Jose, CA 95110. Fax: (408) 437-0711.



SOFTWARE COMPONENTS GROUP

SOFTWARE

RISC instruction benchmarks spark performance debate

Tom Williams, Senior Editor

Another salvo of benchmarks has been fired in the often-heated debate over the advantages and disadvantages of certain RISC architectures. A recent study conducted by Sun Microsystems (Mountain View, CA) has analyzed the Sparc and MIPS instruction sets using the widely accepted Spec benchmarks.

The analysis showed a small difference between the two processors in terms of the performance provided by their instruction set architectures. But after isolating architectural differences, the study concluded that the combined effects of the strengths and weaknesses of the compilers and library routines used on both processors failed to give either a clear advantage. MIPS Computer Systems (Sunnyvale, CA) has countered that analyzing instruction usage doesn't necessarily reveal anything about performance.

One of the authors of the study, Sun engineer David Ditzel, claims that it is not about performance, but only a look at efficiency of instruction set usage. Somehow, the issue of real-world performance seems to come up anyway.

Multiple performance factors

The analysis started from the premise that differences in instruction set utilization could only come from three sources: differences in instruction set architecture; differences in the compilers; and differences in the library routines, which may have been hand-coded and, hence, used different algorithms. One of the points conceded by the study is that even if a benchmark analysis is divorced from timing and system architecture influences, such as cache and memory organization, a raw instruction count doesn't necessarily reflect true performance. The study further concedes that to be fair one must include functions that cause delays similar to executing instructions. But using factors other than actual instructions to normalize the comparison of instruction usage

gives MIPS an opening to claim that many other factors must be considered in evaluating the two processors.

On both MIPS and Sparc processors, for example, a load instruction is often unable to return its data before the cycle immediately following the load. MIPS requires a no-op instruction in the intervening time,

delayed by the hardware interlock even though an instruction is not executed. Factoring out differences such as this produces a closer overall instruction count between the two processors. But it also opens the question, "Why not also count cache access and multiplexing and other elements of the processor that can cause delays?"

Benchmarks and architectures

The Spec benchmarks consist of 10 programs (six floating-point and four integer) written in C and Fortran. The benchmarks include compilation timing, PLA optimiza-

BENCHMARK	MIPS INSTRUCTIONS	SPARC INSTRUCTIONS	MIPS/SPARC
SPICE2G6	21,569,202,673	22,878,017,309	0.94
DODUC	1,613,227,089	1,303,276,485	1.24
NASA7	9,256,812,144	6,614,656,686	1.4
MATRIX300	2,775,967,947	1,693,589,255	1.64
FPPPP	2,316,200,144	1,443,008,199	1.61
TOMCATV	1,812,691,974	1,626,342,454	1.11
FLOATING-POINT GEOMETRIC MEAN			1.3
GCCL.35	1,110,816,041	1,155,986,011	0.96
ESPRESSO	2,828,804,443	2,930,860,108	0.97
LI	6,022,855,076	4,661,320,853	1.29
EQNTOTT	1,243,469,361	1,321,536,444	0.94
INTEGER GEOMETRIC MEAN			1.03
OVERALL GEOMETRIC MEAN			1.18

Among the overall dynamic instruction counts from running the 10 Spec benchmarks, the overall mean ratio (bottom right) shows MIPS executing 18 percent more instructions than Sparc.

while Sparc has implemented a hardware interlock function that operates if the data is not going to be ready for the following instruction. The effect of both techniques is to impose a delay in terms of cycles. The Sparc approach yields a lower total instruction count, while the MIPS approach yields a lower cycles-per-instruction ratio. However, judging performance on instruction count alone would appear to give Sparc an advantage that is not warranted because throughput is

tion, circuit simulation, chemical, thermodynamic engineering problems, matrix and Boolean equations. Different benchmarks were able to highlight some aspects of the architectural differences between the Sparc and MIPS. According to the study, the most significant architectural differences are that MIPS has only single-precision floating-point loads and stores while Sparc has both single- and double-precision floating-point loads and stores, giving Sparc an advantage in the float-

SOFTWARE

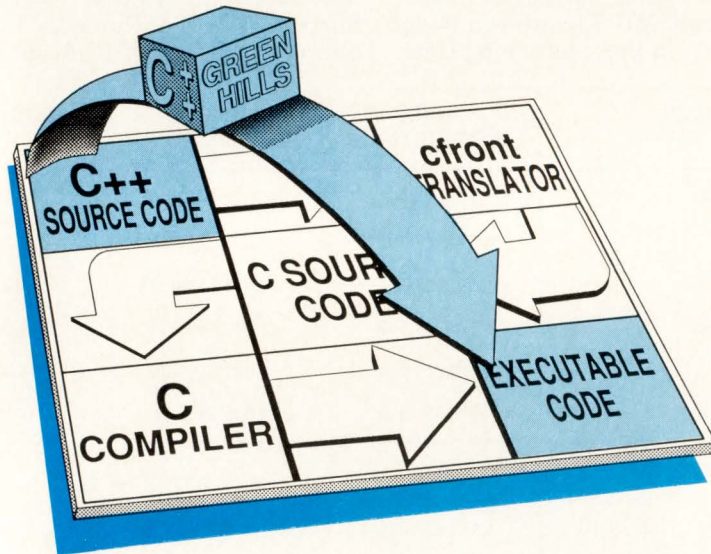
ing-point benchmarks. However, MIPS has a single compare and branch instruction, while Sparc uses one instruction to set condition codes and another to branch. This gives MIPS an advantage in the integer benchmarks.

Some differences relate to the importance the architects of the chips placed on the trade-offs in implementing operations in silicon as opposed to library routines. The MIPS processor, for example, has multiply and divide/remainder instructions,

while the Sparc chip does not. As a result Sparc incurs a penalty on these operations, averaging 19.8 instructions/call for integer multiply and 35 instructions/call for divide/remainder. Sparc, on the other hand, has a floating-point square root instruction while MIPS does not. MIPS, in turn, pays a penalty averaging 62 instructions/call for floating-point square root. Fortunately for both processors, the Spec benchmarks are not heavy with these calls. The worst-case benchmark for Sparc uses 1.47 percent of the instructions for integer multiply and 2.20 percent for divide/remainder. Conversely, the highest percentage of floating-point square root instructions required of the MIPS chip is 2 percent.

According to the study, the com-

NO TRANSLATION REQUIRED



GREEN HILLS C++ IS A TRUE COMPILER

Unlike a C++ translator, Green Hills C++ goes direct from source to executable code in one step. With over 50 advanced optimizations, Green Hills C++ produces far faster code than cfront pre-processors.

THREE COMPILERS IN ONE!! C++, ANSIC, KERNIGHAN & RITCHE C

Simplify your development environment with one compiler for your C++ and C sources. Green Hills C++ supports multiple inheritance, operator overloading and data abstraction.

CIRCLE NO. 43



One Cranberry Hill • Lexington, MA 02173
Tomorrow's Solutions, Today

DEVELOP EMBEDDED OR NATIVE APPLICATIONS

Reduce the cost of complex cross/embedded applications by using object oriented technology. Green Hills C++ supports 680x0™, 88000™, and i860™ targets.

THE CHOICE IS YOURS

Available on over 15 hosts: Native and cross: Sun-3, Apollo, 386 UNIX, Apple Mac II (A/UX), Motorola, NeXT, DG AViiON, Sony NEWS and 88open certified hosts; Cross only: Sun-4, DEC VAX (VMS & Ultrix), DECstations, Apollo, IBM RS/6000. More ports in process, call for details.

We're fluent in C++
Call (617)862-2002
or FAX (617)863-CODE (2633)

i860 is a trademark of Intel Corporation. All other trademarks are acknowledged to their respective companies.

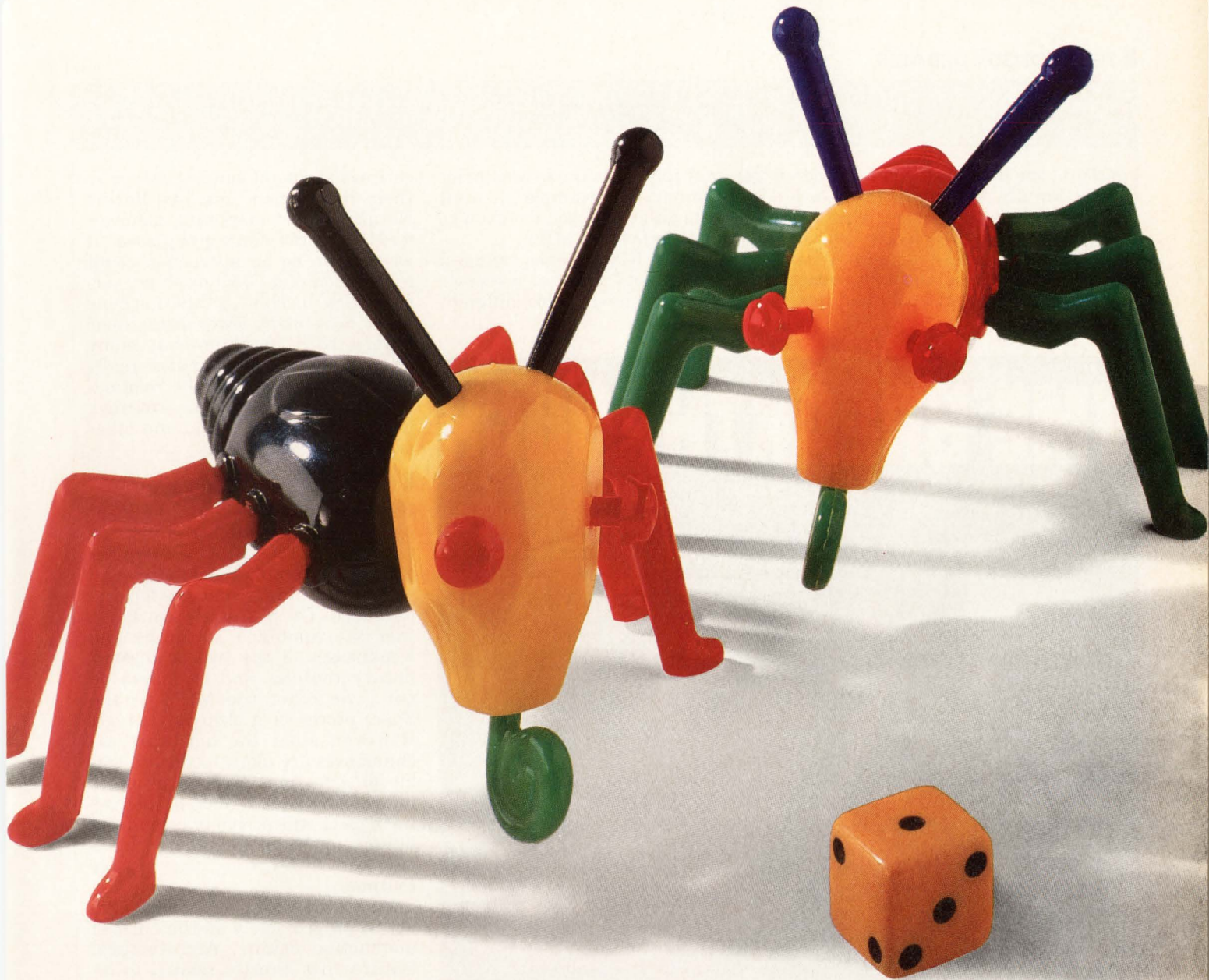
BENCH-MARK RATIOS	MIPS/SPARC RATIO		
	FLOATING-POINT	INTEGER	ALL
TOTAL	1.3	1.03	1.18
TOTAL+	1.25	0.88	1.09
TOTAL++	0.86	0.97	0.97

Three ratios measure instruction set usage between MIPS and Sparc using the Spec benchmarks. "Total" indicates raw counts of user-level instructions. "Total+" shows the ratio considering other delay factors, such as trap handling and load-use interlocks. "Total++" shows the estimated effect of adding hypothetical instructions to both architectures to even out differences in instructions.

compilers and the library routines affect performance. But again, most of the differences measured are the result of conscious trade-offs, and the net results on overall performance tend to cancel out.

Performance gap narrows

The raw instruction data gathered using the Spec benchmarks showed the MIPS processor executing 18 percent more user instructions than the Sparc. However, when Sparc's non-instruction events, such as load-use interlocks, are brought into the



You Don't Have To Take Chances With Bugs.

THE LOWEST-COST XDB ROM MONITOR DEBUGGER FOR MOTOROLA 68000, 68020, 68030, 68302, 68332 AND 68340 MICROPROCESSORS.

Every embedded microprocessor application starts off with a few bugs. But you can eliminate them without missing a beat — or a deadline. Because with InterTools XDB ROM Monitor Debuggers, you start and finish debugging sooner in actual prototype environments. XDB's powerful user-friendly interface and "smart" ROM Monitor make it the most productive debugger available. And, starting at just \$2,495, it's also the lowest priced. Call now for more information, or to order.

With InterTools, you don't have to take chances with bugs. **1-800-356-3594**
617-661-0072.



Intermetrics

Microsystems Software, Inc.

Make Every Bit Count



Price is for IBM PC and compatible version; call for pricing for other platforms.

733 Concord Ave., Cambridge, MA 02138

CIRCLE NO. 44

SOFTWARE

picture, the difference drops to 9 percent. Finally, the study team estimated the effects of adding hypothetical instructions to each chip to factor out all architectural differences. What if MIPS had a floating-point square root instruction and Sparc had inte-

ger multiply and divide/remainder instructions, for example? In that case, the difference would narrow to 3 percent in favor of MIPS.

But since RISC means "reduced instruction set," the two processor architectures have made different

choices in terms of limiting the size of their instruction sets. As Robert Novak, product marketing manager for MIPS' performance group, says, "If we were to do an instruction count comparison of a CISC machine, versus a RISC machine, a CISC machine would have many fewer instructions than a RISC machine—but many more cycles." So performance really can't be divorced from the relationship between instructions executed, the cycles per instruction and other architectural overhead.

Neither has significant edge

Because RISC relies on intelligent use of a smaller number of instructions than CISC, RISC is more dependent on compiler technology and on efficient library routines for performance. The Sun study concluded that the combined strengths and weaknesses of the two processors' library routines and compilers do not give either the MIPS or the Sparc processor a clear advantage. However, since the hardware architectures are likely to remain stable for some time, practical progress in reducing the number of instructions used will probably come from improvements in compiler technology and fine-tuning the library routines.

Pure processor performance cannot be judged solely on the basis of instruction counts. Architectural features not directly related to instructions can also affect performance. According to MIPS' Novak, the MIPS processor can, for example, simultaneously access data and instruction caches, while Sparc cannot—an element that must surely affect performance. If Sun is going to concede that there are some factors other than instructions executed that affect performance, it must admit to all of them. And if the results of Sun's own study were so close, designers must look at factors beyond instruction utilization to draw their own conclusions. ■

VME BREAKTHROUGH



Announcing VMIC's New VME to VME Links Breakthrough

VMIC's new VME-to-VME Links:

- VMIVME 5610L - High Speed Direct Memory Access Link with 32-Bit VME-to-VME Data Transfers at 13 Mbytes/s
- VMIVME 5530L - Fiber Optic Repeater Link for Remote VMEbus System Linkage
- VMIVME 5550 - Multidrop Reflective Memory with Interrupts and broadcast capability.

VMIC's line of VME-to-VME links gives you a wide variety of options which support the interconnection of all mainframes and minicomputers designed with a VMEbus based front end. These links may be used with Sun Workstations, Concurrent, Encore 91 Series, Silicon Graphics, Motorola Delta Series, Alliant, DEC, Harris and more.

VMIC VME
1-800-322-3616

VMIC offers over 75 VMEbus products with a two year warranty ready for immediate delivery. VMIC further supports our customers with 24 hour technical support.

VME Microsystems International Corporation
12090 South Memorial Parkway
Huntsville, AL 35803-3308
(205)880-0444 FAX (205)882-0859

VMIC products are internationally represented by distributors throughout the world. Call or FAX VMIC for complete information.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

MIPS Computer Systems (408) 720-1700	268
Sun Microsystems (415) 960-1300	269

68000

STOP WASTING TIME & MONEY

BSO/TASKING'S new toolkit for developing software for the 68000 family, called **TASKTOOLS™**, beats all others on the market today. Check out these features and benefits.

C COMPILER

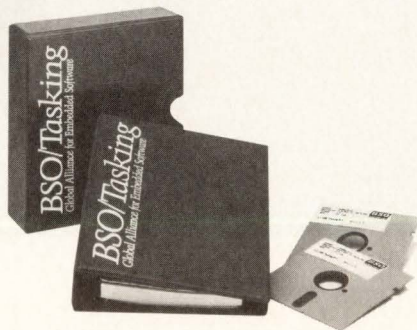
- ANSI C
- Highly optimized code
- Reentrant code
- Direct control of I/O
- Interrupt handlers may be written in C
- Floating point support
- 68040 and 68332 support

CROSS VIEW™ DEBUGGER

- All major emulators supported
- Multi-window interface
- Code & data breakpoints
- Source level tracing
- Stack tracing
- I/O simulation

ASSEMBLER & LINKER

- Motorola compatible
- FPU & MMU support
- Fully featured



TaskTools and CrossView are trademarks of BSO/TASKING.

TASKTOOLS™

The most
powerful set of
68000 software
development
tools available!

BENEFITS

TASKTOOLS™ offers you the following benefits:

- Reduced code size
- Increased productivity
- Great documentation
- Hot line support
- For PC, Sun, Vax, HP, Apollo, IBM & DEC RISC
- Multi object formats

OTHER PROCESSORS WITH SIMILAR SUPPORT

- Motorola 68HC11
- Intel 80X86
- Intel 8051 & derivatives
- TMS 320C25
- Siemens 80C166

CALL US

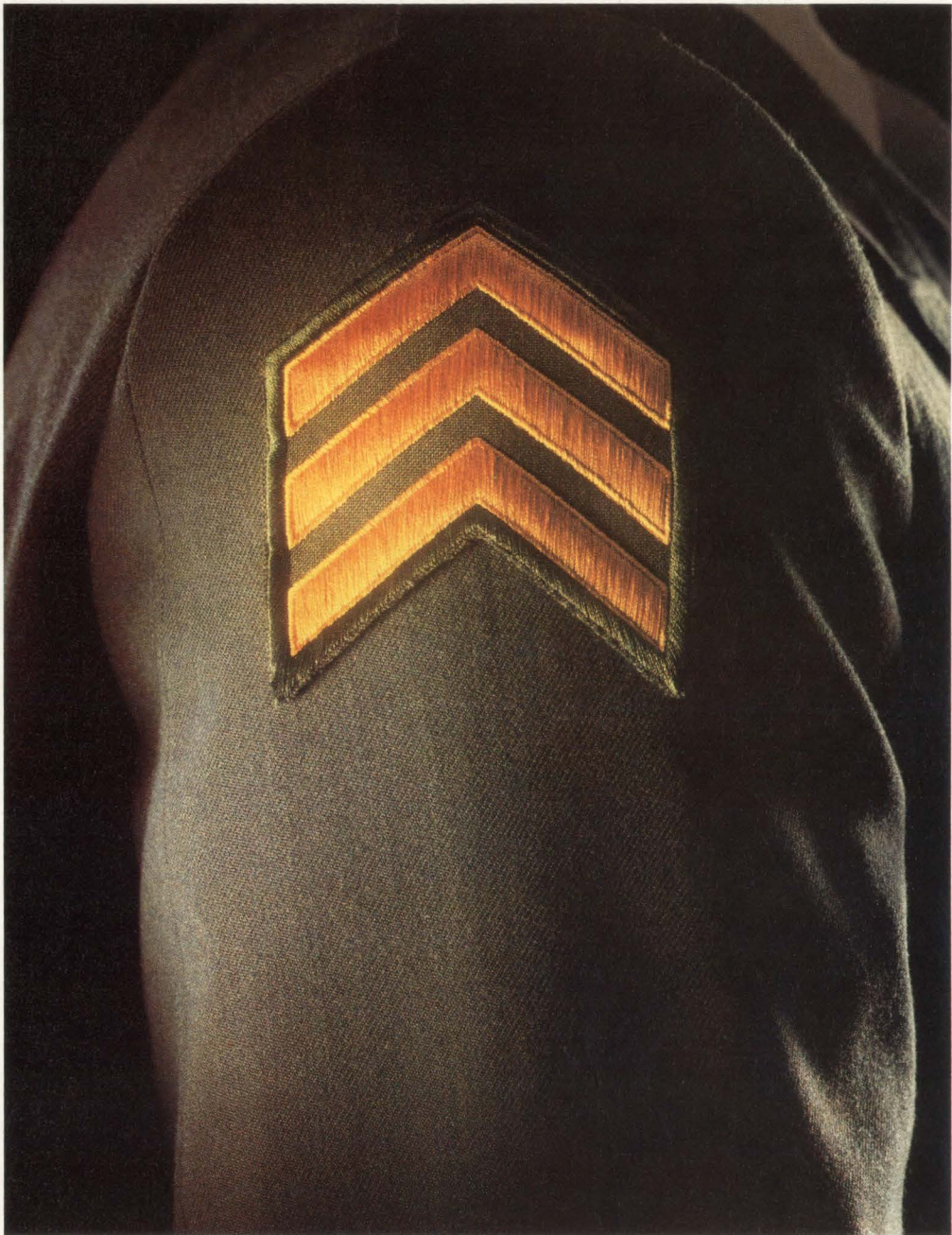
1-800-458-8276.

Outside U.S.A. 617-894-7800.

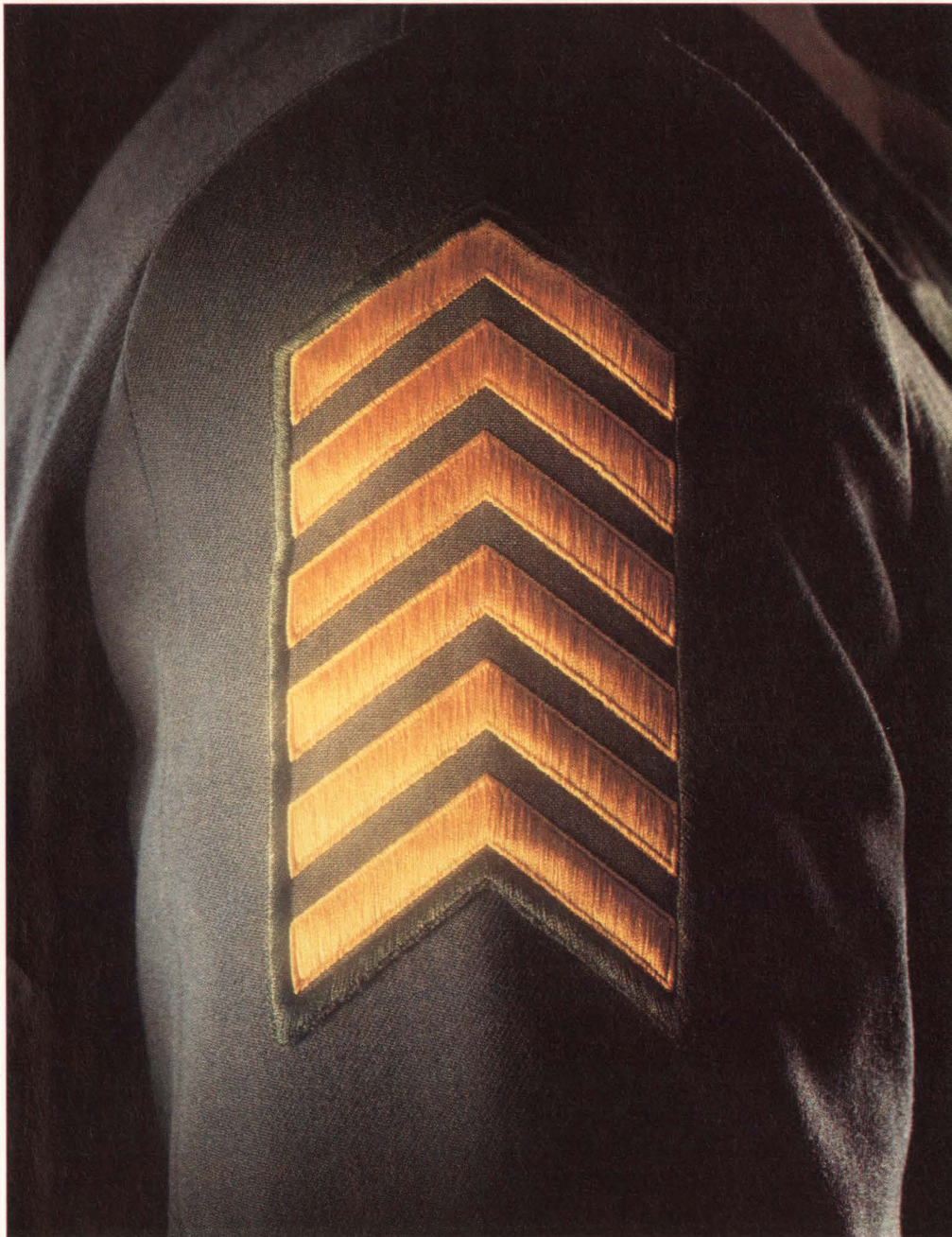
Fax 617-894-0551.



**BSO
TASKING**

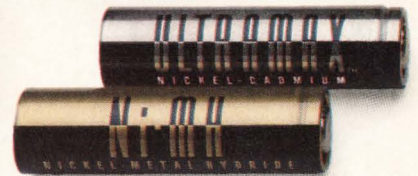


© 1991 Gates Energy Products, Inc.



Now, up to twice the power of a standard battery.

Introducing two new rechargeables from Gates that are commanding everyone's attention: Nickel-Metal Hydride and ULTRAMAX™ Nickel-Cadmium batteries.



Ni-MH offers up to 100% more capacity than a standard Ni-Cd battery, while our ULTRAMAX line offers up to 70% more capacity.

And, with this increase in power comes unequalled design flexibility, such as longer run time, additional features, or downsizing without sacrificing performance. To contact a sales engineer near you, give us a call at 1-800-67-POWER. And see why no battery ranks higher.

Gates

Energy Products

The power of great ideas.

CIRCLE NO. 47

When is it safe to synthesize?



Ask Sun.

Synthesis is one of the reasons the SPARC® systems get to market so fast. Sun's Chris Malachowsky says, "I can now design 30,000 gates in the time it would take to design 2,000 gates the old way. Synthesis gets me to simulation and verification faster and more accurately." Synopsys tools have become the synthesis standard, compatible with all major ASIC libraries, hardware platforms, and other design software. Chris is convinced: "Logic synthesis is the *safest* way to design complex, gate-intensive chips—and to meet impossible deadlines."

synopsys®

DAC Booth #2218

Synopsys Inc., 700 East Middlefield Road, Mountain View, CA 94043-4033 FAX: 415-965-8637 TEL: 800-388-9125

© 1991 Synopsys Inc. SPARC is a registered trademark of SPARC International, Inc. Products bearing the SPARC trademark are based on an architecture developed by Sun Microsystems, Inc.

CIRCLE NO. 48

ASIC complexity fuels drive to HDL design

Spiralling gate counts and time-to-market pressures are making HDLs mandatory. Designers must choose the right HDL and integrate it into their design environment.

Mike Donlin
Senior Editor

As design tasks get more complex and ASICs routinely surpass the 20,000-gate level, it's impossible for an engineer to visualize a design without using a high-level description. In addition to this "can't see the ASIC for the gates" problem, time-to-market pressures will require simulation at the architectural level as time-consuming iterations of a design become unacceptable.

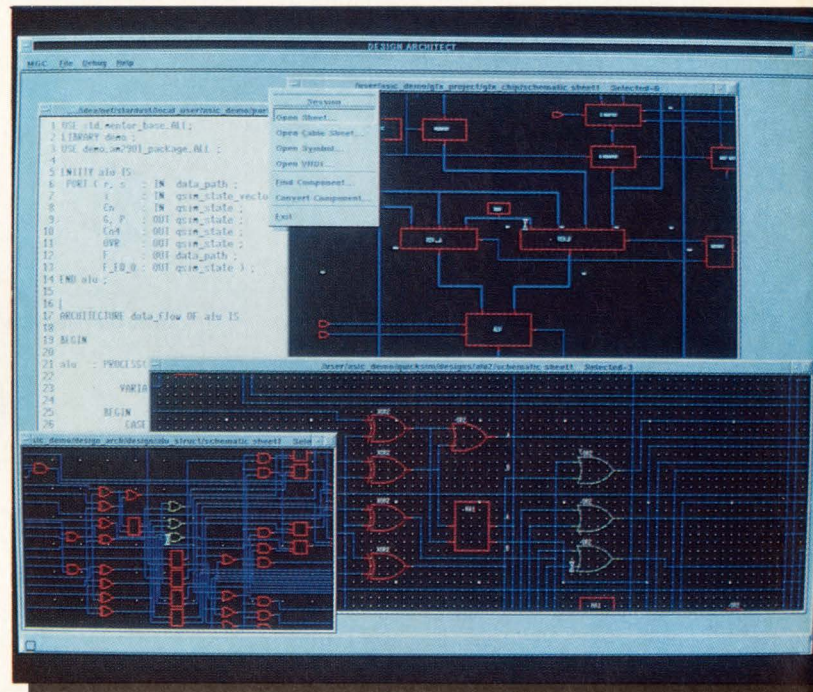
High-level languages in general and hardware description languages (HDLs) in particular will do for hardware designers what C, Pascal and Ada did for software developers—free them from thinking about the minutiae of a design and let them optimize its behavior.

Quite simply, the HDL revolution addresses two increasingly important issues: circuit complexity and designer productivity. "Companies just don't have a choice anymore," says Patrick Beauvillard, technical marketing manager at Cadence Design Systems (San Jose, CA). "Even if it were possible to design a complex ASIC at the gate level, statistics show that about half the time it won't work when interfaced to the rest of the system. It's imperative to simulate performance at a high level of abstraction. You need an HDL to do this."

More-productive designers

"Another critical benefit of HDLs is designer productivity," adds Venkatesh Shukla, the open Verilog program manager at Cadence. "With traditional methods an engineer might be able to design 30 to 50 gates a day. With an HDL, productivity is more in the neighborhood of 200 gates a day. Does this mean a company will need fewer logic designers? I don't think so. There are plenty of other tasks, like exploring design efficiency and real estate requirements before implementation, that need to be addressed."

In addition to increasing productivity, HDLs also decrease the costly portions of the design cycle, namely the test and debug of complex circuits.



Mentor Graphics' design environment lets users specify designs graphically or textually. The upper right window displays a high-level block diagram for a graphics processing design. The upper left window contains the VHDL description of the ALU block. The lower two schematic windows display the gate level logic synthesized from the VHDL description.

■ HDLs

"What you have is a shift in how engineers use their time," says David Coelho, executive vice-president of strategic planning and business development at Vantage Analysis Systems (Fremont, CA). "In a typical bottom-up approach, a designer might spend 10 percent of his time doing high-level architectural planning, 40 percent on gate-level design and 50 percent on test and debug. In a top-down approach, that shifts to maybe 30 to 40 percent for design description, but only 30 to 40 percent in logic design and only 20 to 30 percent in test and debug. By simulating at the front end, you don't have as many penalties at the back end."

HDLs also give engineers an opportunity to generate test vectors at an early stage in the design cycle. Products such as Test Compiler from Synopsys and Test Design Expert from ExperTest (Mountain View, CA) generate test programs from VHDL descriptions. "We find that if an HDL description is being written for synthesis, it's very close to what we need for test generation," says Charlie Miller, vice-president of sales and marketing at ExperTest. "We can tweak a description like that in a day or so. If the code has been written for simulation purposes, however, it might take a little longer because there are structures in there that have nothing to do with the physical implementation of the device and which don't translate into test parameters."

■ Thinking in code

Even though the debate over whether to use an HDL is subsiding, there are other issues, such as which HDL to use and how to implement it into a company's design philosophy, that are just beginning. The real question that fuels these debates is simple—how does a company get design engineers who are used to thinking in graphical or schematic terms to think of a design as lines of code?

The transition to an HDL methodology is usually not as much of a problem for engineers who have recently graduated from schools where software is part of the curriculum as it can be for designers who simply haven't had to work with or think about software. The push to adopt HDLs is real, however, and even experienced engineers are being forced to learn new ways. The transition is not always easy.

"I guess you could say that at the

outset, some people aren't wildly enthusiastic," says Terry Coston, director of systems development at Harris Semiconductor (Melbourne, FL). "But if you look at the history of EDA, it's full of the same kind of painful transitions. In the '60s and '70s engineers were forced to use

computers to verify circuits. They weren't wild about that at first, either. In the '70s the real EDA tools started coming out, and engineers had to start working on workstations. The same thing will happen with HDLs. It will be a slow transition, but it will happen."

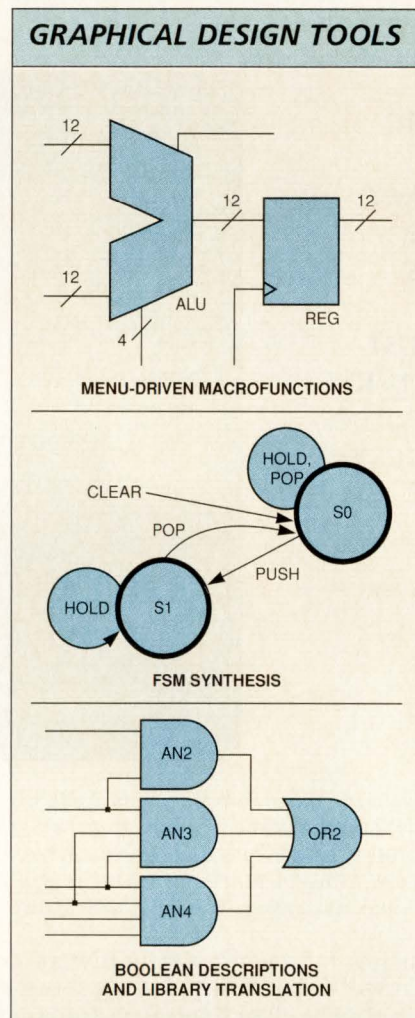
Harris conducts in-house seminars to teach its engineers VHDL, a language the company uses primarily for building cell libraries for synthesis. "The trick is not to just push people through a two-week course," Coston points out, "but to get an engineer working on a project using an HDL as soon as possible. Of course the time it takes someone to master a language varies, but within a few months just about anyone can become proficient."

■ Designing at a higher level

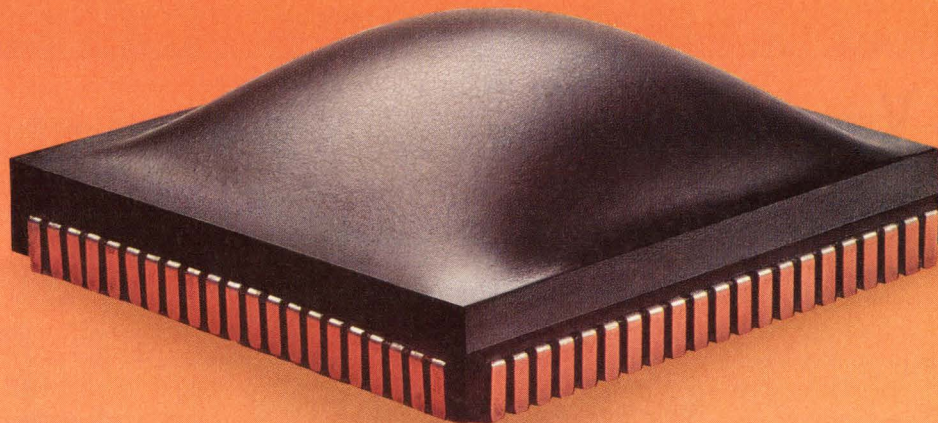
Traditional design methodologies force designers to focus on wiring up gates. The HDL approach permits designers to work at a higher level, where the function and behavior of a device is considered before committing the design to a specific architecture.

Considering a device's functions and behavior first has its advantages. "Take, for instance, someone who's designing an adder," says Cadence's Beauvillard. "If the device has been designed with a schematic editor and it's not fast enough, there aren't a lot of options for improving its performance. A designer might optimize the place and route and get a 10 to 15 percent speed improvement, but if that's not enough, either the design has to be thrown out or the slower speed has to be designed around. With an HDL, however, a designer can evaluate the architecture and choose the best one before committing it to gates."

Some engineers are approaching HDL design methodology by adopting traditional software methods. In his VHDL training seminars, Bill Billowich, president and CEO of the VHDL Consulting Group (Allentown, PA), encourages this approach, especially for students unfamiliar with software design. "Anytime you tell a hardware engineer to take a design and start coding, he's probably going to be intimidated," says Billowich. "So I think the best method is to train someone how to approach the job. If a hardware designer asked a software engineer how to approach a 10,000-line piece of software, he'd get some



Graphical tools give designers a familiar way to conceptualize portions of a circuit at a high-level of abstraction. These tools are emerging as an entry point for designers who aren't familiar with thinking of a project in terms of lines of code. Shown here are some examples of the form that such tools might take. The top diagram shows how menu-driven macrofunctions can be drawn to represent commonly used devices such as ALUs and registers. The diagrams can represent structural elements as well as data paths and can replace many lines of VHDL. Familiar representations such as bubble diagrams (middle diagram) and Boolean descriptions (bottom diagram) are used to represent finite state machines and PLD circuits.



Pack more logic into every FPGA.

NEW ABEL-FPGA helps you get the most out of the latest FPGAs. If you want to take advantage of the sophisticated capabilities of today's FPGAs, only Data I/O's new ABEL-FPGA™ Design Software has the power to pack in maximum logic. It combines the industry-standard ABEL Hardware Description Language (ABEL-HDL™) with our new intelligent FPGA Device Fitter™

technology. So, you can create more complex designs with less effort—ABEL-FPGA does the hard work for you!

ABEL-FPGA's powerful Device Fitters automatically optimize your circuits for minimum area or maximum speed. Fitters are available for all the leading architectures, including Actel, Altera, AMD, Atmel, ICT, National, Plus Logic, and Xilinx. And with built-in knowledge of its target architecture, each fitter masters the complex features of its device automa-

tically, intelligently.

Practical, detailed documentation, complete with FPGA design examples, also helps to ensure that you get the most from each architecture. And for added design power and flexibility, ABEL-FPGA lets you specify place-and-route constraints directly in your circuit description, so you can easily migrate the same design between multiple FPGA vendors.

Pack more logic into your next FPGA design, with the single solution to all your FPGA behavioral entry needs: ABEL-FPGA. Call today to find out more about NEW ABEL-FPGA.

1-800-247-5700

ABEL-FPGA
Design Software

NEW ABEL-FPGA
with FPGA
Device Fitters!

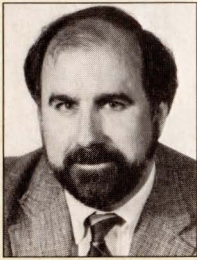
Data I/O Corporation 10525 Willows Road N.E., P.O. Box 97046, Redmond, WA 98073-9746, U.S.A. (206) 881-6444/1-800-247-5700
Data I/O Canada 6725 Airport Road, Suite 302, Mississauga, Ontario L4V 1V2 (416) 678-0761
Data I/O Europe World Trade Center, Strawinskylaan 537, 1017 XX Amsterdam, The Netherlands +31 (0)20-6622866
Data I/O Instrument Electronic Systems Vertriebs GmbH Lochhamer Schlag 5A, 8032 Graefelfing, W. Germany, +49 (0)89-858580
Data I/O Japan Sumitomosaimi Higashi-Shinbashi Bldg., 8F, 2-1-7, Higashi-Shinbashi, Minato-Ku, Tokyo 105, Japan
011-81-3-3432-6991/Telex 2622685 DATAIO J

© 1991 Data I/O Corporation

The Personal Silicon Experts

DATA I/O
Corporation

VHDL, Verilog and UDL/I: An example-driven comparison



VHDL, the IEEE- and ANSI-standard hardware description language, is increasingly used in the defense and commercial sectors of the electronics industry for digital design.

Verilog, a proprietary HDL recently placed in the public domain, is widely used in North America and Europe. UDL/I is the emerging Japanese standard HDL. Why are there three commonly used HDLs? What do they look like? What are the differences between them? When should the use of one language be favored over another?

To compare these three HDLs, we can look at an example worked in all three languages. The model is a clocked, serial-input, parallel-output, 8-bit shift register with asynchronous, active-low clear. To more easily understand the examples, the language keywords used in each model are in bold type.

The VHDL model shown is built around the draft IEEE-standard multivalued logic model. VHDL allows signals of arbitrary scalar or composite type; we'll use the IEEE's proposed nine-state model, which comprises two main elements: the entity interface and the architecture body.

The entity interface, beginning with "entity ShiftRegister" and ending with "end ShiftRegister," describes the model's interface to the universe. Here, the ports, or signals that pass information across this interface, are listed. Each port has a mode, or direction of data flow, and a type. Type "Bit" is a single bit defined by VHDL that indicates the port's mode. "Std_logic" and "std_logic_vector" are the nine-state scalar and vector types, respectively, of the IEEE logic model.

There's also an assertion statement in the interface to check that the shift register is not simultaneously strobed (a rising edge on clock while shift is high) and cleared (clear low).

The architecture body, beginning with "architecture Functional" and ending with "end Functional," describes the

A VHDL example

```

use IEEE.Logic_System.all;
entity ShiftRegister is
  port (Clr: inBit;— asynchronous
clear
  Clk: inBit;— shift clock
  Sh: inBit;— shift enable
  LR: inBit;— shift direction
  S1, S2: inBit;— shift control
  Q: instd_logic;— serial input
  Output: outstd_logic_vector (1 to
8));— parallel output
  begin
    assert not (Clr = '0' and Clk = '1'
and Clk'event and Sh = '1')
    report "Shift register simulta-
neously strobed and cleared"
    severity Warning;
  end ShiftRegister;

```

```

architecture Functional of Shift-
Register is
  signal v: std_logic_vector (1 to 8)
register; — register's internal storage
  begin

```

```

  Output <= v 30 nS;

```

```

  AsyncClear:
    block (Clr = '0')
    begin
      v <= guarded (others => '0') after
12 nS;
    end block AsyncClear;

```

```

  Shifter:
    block (Clk = '1' and Clk'event and
Sh = '1')
    subtype three_bit is Bit_Vector (1
to 3);
    begin
      with three_bit(LR & S1 & S2)
    select
      v <= guarded
      Q & v(1 to 7) when "000",
      '0' & v(1 to 7) when "001",
      '1' & v(1 to 7) when "010",
      v(8) & v(1 to 7) when "011",
      v(2 to 8) & Q when "100",
      v(2 to 8) & '0' when "101",
      v(2 to 8) & '1' when "110",
      v(2 to 8) & v(1) when "111";
    end block Shifter;
  end Functional;

```

structure or behavior of the model.

Models may have multiple architecture bodies per entity interface. In this way, a collection of architectures may represent different organizations or different design abstractions of a model.

The functionality of this shift register is described with three concurrent statements. The first (immediately after the "begin" in the architecture) drives the outputs as a function of the internal state, "v." The second clears the internal state whenever clear is low, and the final statement implements the shift logic.

If both the second and third statements are simultaneously active, then "v" will have conflicting drives applied to it. The IEEE logic model specifies a resolution function to handle such cases; "v" will be set to all "X"s in this case. Note that both of these statements are simultaneously active precisely when the assertion condition is violated.

Together, an entity interface and one of its architecture bodies compose a complete model.

Verilog version

The Verilog version of this model uses the built-in data type for signals—Verilog does not give you the choice of using your own—and is organized in much the same way as the VHDL version. But since Verilog doesn't separate the interface and body of a model, this model is built as a single **module**.

Moreover, Verilog has only relative (or scaled), and not absolute, delays. Hence, we specify that the delay scale factor chosen for this model is 1 ns per unit at the top of the model. Finally, Verilog's built-in resolution mechanism handles the case where both the final two always block drive "v" at the same time.

Like Verilog, the UDL/I version allows the use of only its built-in, four-valued data type for signals. Also, the bits are numbered from zero to seven, and not from one to eight as in the other two examples, because UDL/I requires bits be numbered from zero. Other than this difference, the UDL/I model is very similar to the Verilog model.

As illustrated by these examples, the

Paul J. Menchini, MSEE: Computer Engineering, Corporate Strategic Staff, CAD Language Systems Inc

A Verilog example

```
'timescale 1ns/100ps

module ShiftRegister (Clr, Clk, Sh, LR,
S1, S2, Q, Output);

  input  Clr, // asynchronous clear
         Clk, // shift clock
         Sh, // shift enable
         LR, // shift direction
         S1, S2, // shift control
         Q; // serial input
  output [1:8] Output; // parallel output

  reg [1:8] v; // register's internal storage

  always @(posedge Clk)

    if (Clr == 0 && Clk == 1 && Sh ==
1) $display ("Shift register simul-
taneously strobed and cleared");

    assign #30 Output = v;

  always @(Clr)

    if (!Clr)
      #12 assign v = 0;
    else
      #12 deassign v;

  always @(posedge Clk)

  begin
    if (Clk == 1 && Sh == 1)

      case ({LR, S1, S2})
3'b000:v = { Q, v[1:7]};
3'b001:v = { 1'b0, v[1:7]};
3'b010:v = { 1'b1, v[1:7]};
3'b011:v = {v[8], v[1:7]};
3'b100:v = {v[2:8], Q};
3'b101:v = {v[2:8], 1'b0};
3'b110:v = {v[2:8], 1'b1};
3'b111:v = {v[2:8], v[1]};
      endcase

    end
  endmodule
```

three HDLs have large areas of overlap. Each, however, has features that distinguish it from the others and that may make it especially suited for a particular application.

■ Selecting a language

VHDL contains the most features for design abstraction, especially data-type abstraction. It's especially suited for design-space exploration and for life-cycle management of designs. VHDL has features (configuration declarations—not used in the VHDL example) for the management of design configurations. In addition, VHDL was a well-specified, public standard from the start. Accordingly, many tools from many different vendors are now or soon to be available, giving users the widest choice in EDA tools.

On the other hand, VHDL is the most complex of the three HDLs. If you don't need any of the extras that VHDL provides, then Verilog or UDL/I may let you start designing more quickly. Verilog also has the most-mature suite of tools available, although currently only a small number of vendors support Verilog. That number may soon grow because Verilog has recently become a public standard.

But you have to be careful when using Verilog models as input to synthesis. Verilog contains some nonhardware-oriented constructs; moreover, some constructs are ambiguous. UDL/I, in contrast, was designed to drive register-transfer-level synthesis tools. No constructs are included that cannot be synthesized by such tools, which may limit your ability to describe complex behaviors. Another problem you'll face when attempting to use UDL/I is that there are currently no tools commercially available, although this situation will soon change.

With these examples in mind, designers should carefully consider their needs and goals when choosing an HDL for a particular task.

A UDL example

```
IDENT: Registers;
NAME:SHIFT_REGISTER;
LEVEL:CELL;
INPUTS: SH,"shift enable"
        LR,"shift direction"
        S1,S2,"shift control"
        Q;"serial input"
OUTPUTS:OUT<0:7>;"parallel output"
RESET_PIN:CLR;"asynchronous clear"
CLOCK:CLK;"shift clock"

ASSERTION_SECTION:

ASSERT (^CLR) & RISE(CLK) & SH
ELSE PRINT ('Shift register simul-
taneously strobed and cleared')
END_ASSERT;
END_SECTION;

BEHAVIOR_SECTION:

REGISTER:V<0:7> DELAY 12NS;

OUT := V DELAY 30NS;

IF ^CLR THEN
  RESET(V);
END_IF;

V := IF .SH THEN
  AT .CLK DO
    CASE LR !! S1 !! S2 OF
#3o0Q!! V:6
#3o10!! V:6
#3o21!! V:6
#3o3V<7>!! V:6
#3o4V<1:7>!! Q
#3o5V<1:7>!! 0
#3o6V<1:7>!! 1
#3o7V<1:7>!! V
    END_CASE
  END_DO
  END_IF;
  END_SECTION;

END;
```


HDLs

valuable advice. The issues are the same for both hardware and software engineers, namely ones of modularity, commentary, partitioning, and defining interfaces up front."

Thinking in pictures

Because some engineers are reluctant to change their methods of thinking and because portions of a design may be best left to a graphical methodology, some EDA vendors

charts. Using these graphical descriptions, Express VHDL can simulate the performance of a system and generate VHDL code that can be synthesized into schematics.

At first blush, this ability to graphically depict system behavior and have a tool translate the resulting diagrams into VHDL might seem like the best of both worlds, but some engineers are skeptical about such an approach. Critics point out that code translated from

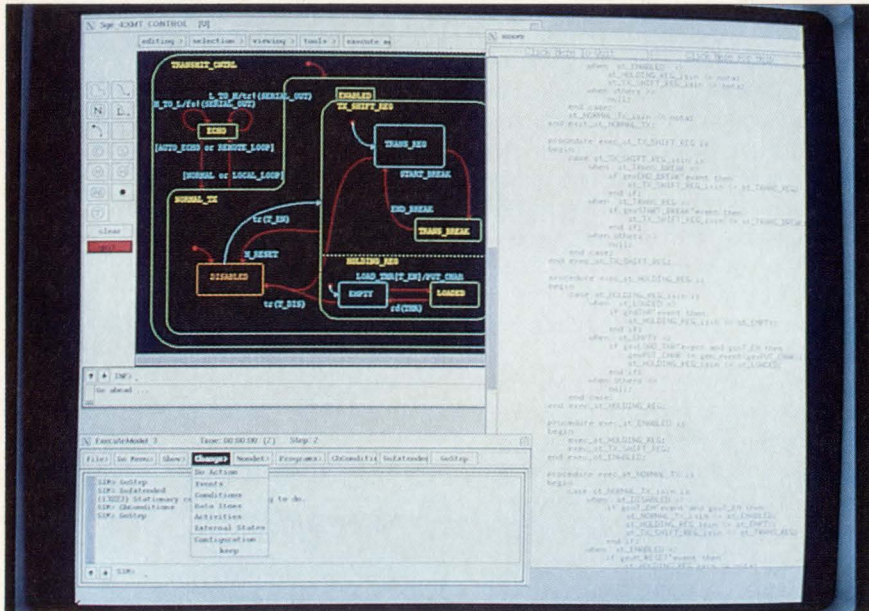
such tools available. Mentor Graphics (Wilsonville, OR), for instance, acquired high-level graphical description tools when it purchased Silicon Compiler Systems (SCS). According to Mentor, the AutoLogic and LogicLib tools from SCS let ASIC designers raise the level of their design specifications from gates and improve the efficiency of those designs without having to learn new design practices. With these tools, designers can express functions with building blocks. These blocks can represent over 50 synthesizable logic functions including adders, ALUs, comparators, counters, multipliers, tally blocks, and Wallace trees. Custom functions can also be developed by users. The synthesis side of the tool accepts these blocks as input, as well as NETED schematics, netlists, Boolean descriptions, PLA tables, and finite state machines.

The goals of HDLs

Regardless of how a design is entered, it's only useful if it can be simulated, synthesized down to an actual product and accurately documented. Interestingly enough, the three main HDLs in use today, Verilog HDL, VHDL and UDL/I (Unified Design Language for Integrated Circuits), were all designed with one of these capabilities in mind.

Verilog HDL from Cadence was developed as a high-level language for use with the Verilog-XL simulator by Gateway Design Automation, a company that was acquired by Cadence in 1989. The Verilog family caught on with a number of ASIC vendors because of its excellent simulation capabilities. According to Cadence, Verilog HDL is currently the most widely used HDL in the industry with over 10,000 users. In addition to its high-level description and simulation capabilities, Verilog HDL is also supported as a synthesis language. Although highly regarded, Verilog carries neither the DOD stamp of approval nor IEEE standardization (VHDL has both). In a move designed to keep Verilog HDL alive as a competing force against VHDL, Cadence opened the language as public domain software in May of 1990.

VHDL was designed for the U.S. government by Intermetrics (Cambridge, MA) to provide a standard way to document designs. Because VHDL provides a standard simula-



Express VHDL, a graphical entry tool from i-Logix, lets engineers validate a behavioral model of a device before any code is written. The tool then generates VHDL code that can be synthesized into schematics. In this example, the transmitting function of a dual asynchronous receiver/transmitter is described graphically in the upper left window. Resulting VHDL code is printed to the right.

are coming out with products that let designers use a combination of block diagrams and HDLs. A tool called Express VHDL from i-Logix (Burlington, MA) lets users create a visual model of system specifications through Activity-Charts, which show data and control flows hierarchically, along with the system's processing capabilities. These Activity-Charts translate into Statecharts, which describe the dynamics of a system and show the control aspects of the system's functions.

The charts identify all possible states and the transitions between them, while labels on the transitions indicate when and under what conditions each transition will take place. The tool uses Module-Charts to describe the hardware and software components of a system and their relationship to the elements identified in the previous two

such high-level descriptions will not be as efficient as software written by a good designer. In addition, some people think a large design can't be conceptualized at a graphical level.

"It's hard to picture a state machine bubble diagram stretching beyond two pages," says the VHDL Consulting Group's Billowich. "It's difficult to think of a large project that way because after a while you have to think of a design as a classic enumeration of states. By the time you get to page five or six of a graphical representation of a design, you don't know where you are or what connects to what. This isn't to say that a graphical entry for VHDL is a bad thing—you just have to be careful how you design it."

Still, because engineers are accustomed to using graphical representations for design definition, EDA vendors are pursuing ways to make

NETWORKING SOLUTIONS

FDDI, TOKEN-RING AND ETHERNET COMMUNICATIONS

The need to network has never been greater. Diverse processing platforms, distributed architectures, client-server, departmental and workgroup environments all contribute to increased demands on the network. System and network designers need a proven source of technology solutions for the wide range of networking and communication application problems they face. Interphase delivers those solutions.

FDDI, TOKEN-RING AND ETHERNET SOLUTIONS

Interphase has long led the industry in high-performance VMEbus peripheral controllers, and that same leadership is now evident in networking node controllers. Interphase has FDDI, Token-Ring and Ethernet solutions for virtually any VMEbus system application challenge.

PROVEN FDDI SPEED AND INTELLIGENCE

Interphase's FDDI 100 Mb/s offerings are a logical choice for the industry. The V/FDDI 3211 Falcon received *UnixWorld* magazine's Product of the Year designation and was the industry's first 6U VMEbus FDDI solution. Interphase's newest FDDI product is the V/FDDI 4211 Peregrine, a RISC-based high-performance node controller capable of link level operation or on-board protocol processing. The Peregrine provides single or dual attach configurations, with SMT (Station Management Software) running on-board, all in one 6U VME slot.

TOKEN-RING RESULTS

The V/Token-Ring 4212 Owl is an ultrafast Token-Ring node controller based on the partitioned architecture of Interphase's proven Eagle class of controllers. The Owl facilitates connectivity of UNIX® systems, workstations, supercomputers or any other VMEbus system into an IBM® environment using IEEE 802.5 Token-Ring. This multiple processor design provides an elegant queued interface to the system supporting IEEE 802.2 LLC, and a flexible 4 or 16 Mbit interface to the Token-Ring network.

ETHERNET CHOICES

Interphase also offers two Ethernet design options. The V/Ethernet 4207 Eagle 32-bit protocol platform is the high-performance standard for the industry, and offers on-board TCP/IP support. The V/Ethernet 3207 Hawk is designed specifically for cost-sensitive VMEbus applications.

GET YOUR NET WORKING NOW

No matter what your networking need – FDDI, Token-Ring or Ethernet – Interphase is ready to provide the solution. For more information call today:

(214) 919-9000



OPEN SYSTEMS CONTROLLERS™

Disk • Tape • Networking

13800 Senlac • Dallas, Texas 75234 • (214) 919-9000 • FAX: (214) 919-9200 • NASDAQ-NMS:INPH

Interphase International
Astral House, Granville Way • Bicester, Oxon OX6 0JT • (01144) 869-321222 • FAX: (01144) 869-247720

© 1990 Interphase Corporation. Interphase is a registered trademark of Interphase Corporation. Open Systems Controllers is a trademark of Interphase Corporation. Specifications subject to change without notice. UNIX is a registered trademark of AT&T in the United States and other countries. IBM is a registered trademark of International Business Machines.

CIRCLE NO. 50

HDLs

tion input language, it's supported by most major CAE vendors' simulators. Several companies, among them Synopsys, Racal-Redac (Westford, MA) and Viewlogic, support VHDL as a synthesis language. The fast-growing acceptance of VHDL, however, probably stems more from DOD support and the IEEE endorsement rather than its ease of use or popularity. Many users feel that because VHDL has so many features and capabilities, it's difficult to use.

"VHDL was developed by software designers," says James Velenga, manager of design representation at Racal-Redac. "I remember in the '80s looking at some of the original proposals for VHDL and thinking that it wasn't being designed for hardware designers; it was being written for software designers who didn't understand the issues of synthesis and implementation. Restricting it would make it more usable. People don't want 47 different ways of expressing something—it confuses them."

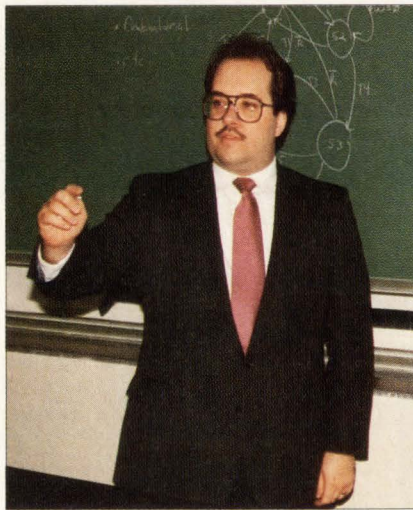
The most recent contender in the HDL arena, UDL/I, is being developed by the Software Development Committee, an organization of Japanese electronics firms and the Japan Electronic Industry Development Association. Based on Nippon Telephone and Telegraph's internal HDL, UDL/I is primarily targeted to drive register transfer level (RTL) synthesis tools. Though the fact that it's being designed to support synthesis is attractive, the large market share of Verilog HDL and the standardization efforts behind VHDL are causing most EDA vendors to take a wait-and-see attitude about UDL/I.

HDLs for programmable logic

Most companies that support VHDL and Verilog view these languages as a way to design large ASICs and even larger systems. But there are other HDLs that are targeted to programmable devices such as PALs, PLDs and field-programmable gate arrays (FPGAs), and these are often an entry point for engineers who are just starting to use language-based designs. Companies such as Data I/O (Redmond, WA) and Minc (Colorado Springs, CO) offer HDLs that support the development of programmable devices. Because these languages aren't intended for large system designs, they're simpler to use and don't need the complicated

simulation and synthesis constructs of other HDLs because their target devices can be programmed, tested and reworked in a matter of minutes.

"Our Abel language is designed to work at the behavioral level," says David Kohlmeier, division engineering manager for the design software business unit at Data I/O. "We don't get into structural issues such as data paths. We can go from a description to a device, whereas VHDL and Verilog produce generic netlists and then need synthesis to get to a



"Basically two types of people deal with VHDL," says Bill Billowich, president of the VHDL Consulting Group. "A minority are model developers who support the CAE functions of a company. They will produce a model of a multiplexer that the design team might need. The second group, digital designers, use VHDL to describe what these models do."

particular part."

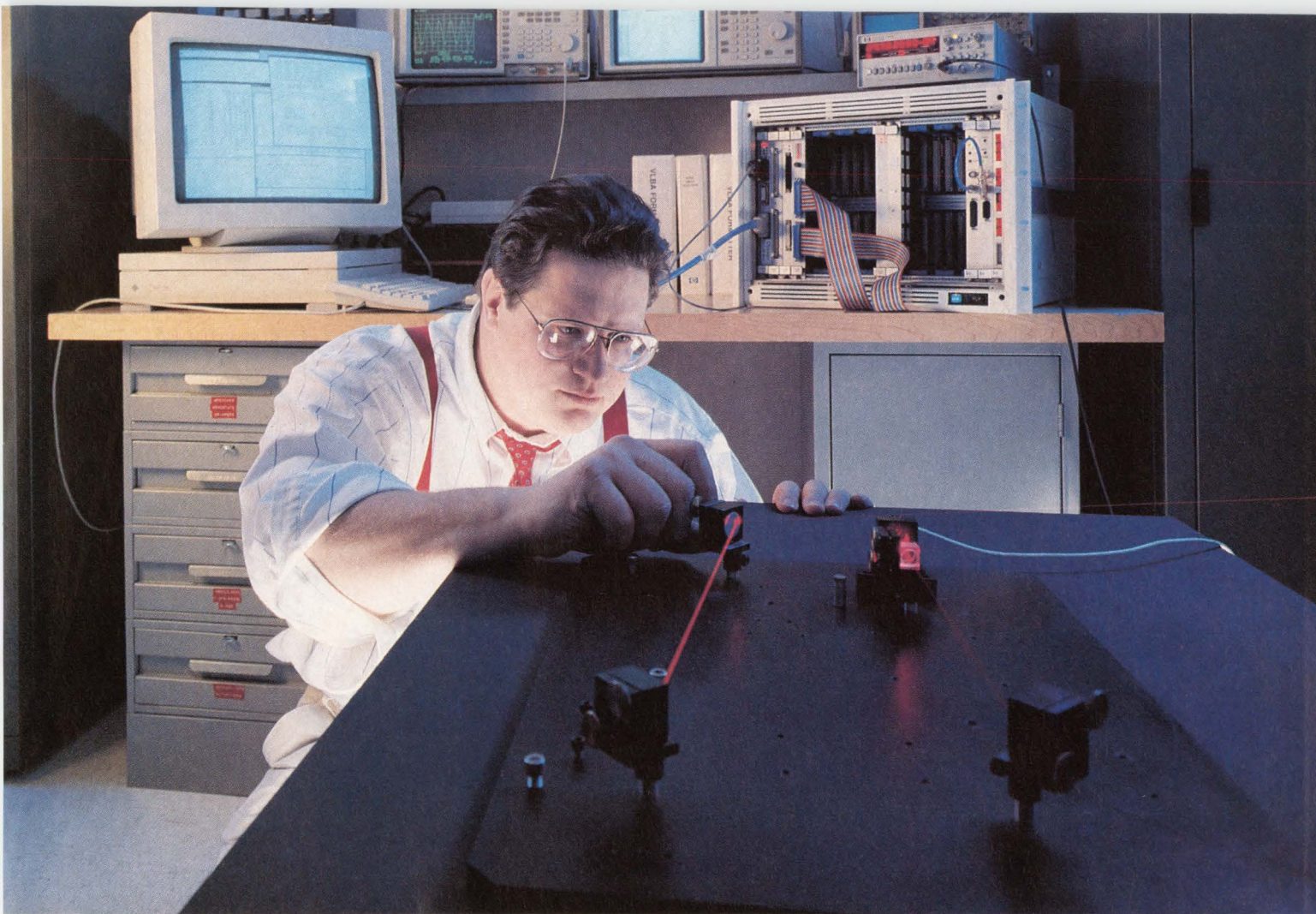
Even though these programmable logic languages provide a migration path for engineers to move from traditional methods of design entry to HDLs for ASIC design, most vendors of these tools and languages agree that they will someday move into VHDL either as a subset or by providing hooks for file input and output. In fact, Viewlogic's VHDL synthesis translates from RTL descriptions to FPGA part formats. According to Minc vice-president Kevin Bush, "In the long term, we'll end up with some form of VHDL in our tools. When you have companies like Mentor and Valid incorporating VHDL into the suite of tools of which you're a part, it's pretty hard to stay on the sidelines."

Analog designs are one of the last frontiers that need an HDL standard. Work on an analog HDL (AHSL) standard is in its infancy, with the IEEE SCC30 committee looking into it as a language or as an extension of VHDL. One of the proposals the IEEE committee is considering is the Mast AHDL from Analogy (Beaverton, OR). Designed for use with Analogy's Saber simulator, Mast can be used to write models for circuit-level devices, such as transistors and diodes, up to system-level boxes, such as control functions and differential equations. Saber can then simulate these analog parts, as well as ASICs, digital components, lasers, motors, and control systems.

HDLs, whether graphical, textual or some combination of the two, will undoubtedly be a primary force in the designs of the '90s. "Let's face it," says Dick Albright, director of marketing for CAE products at Valid Logic Systems (San Jose, CA). "If you can keep a designer working at a high level, you're going to increase productivity. If I have a language, a simulator and a synthesis tool, I don't want my engineers wasting their time laying gates out on a schematic. To be competitive you simply have to move to a higher level of abstraction." ■

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Analogy	
(503) 626-9700	Circle 220
CAD Language Systems Inc	
(301) 963-5200	Circle 221
Cadence Design Systems	
(408) 943-1234	Circle 222
Data I/O	
(206) 881-6444	Circle 223
ExperTest	
(415) 965-2000	Circle 224
Harris Semiconductor	
(800) 4-HARRIS, ext. 1030	Circle 226
i-Logix	
(617) 272-8090	Circle 227
Intermetrics	
(617) 661-1840	Circle 228
Mentor Graphics	
(503) 685-7000	Circle 229
Minc	
(719) 590-1155	Circle 230
Racal-Redac	
(508) 692-4900	Circle 231
Valid Logic Systems	
(408) 432-9400	Circle 232
Vantage Analysis Systems	
(415) 659-0901	Circle 233
VHDL Consulting Group	
(215) 266-9791	Circle 234



At Interferometrics Laboratories Todd Brackett, Control System Group Leader on NRL's Big Optical Array Project, adjusts the optics on a laser interferometer.

Opening a New Eye on the Cosmos

The Naval Research Laboratory needed a better way of seeing the Universe. They came to Interferometrics for help.

When Interferometrics needed computers to control NRL's revolutionary Imaging Optical Interferometer they came to Themis Computer.

The NRL Big Optical Array imaging interferometer requires a perfectly synchronized dance of mirrors to eliminate the delay and distortion of starlight passing through turbulence cells in the atmosphere. These mirrors require an intricate network of motors, sensors and actuators, linked through Ethernet, working together, to counter the earth's motion and distorting effects of the atmosphere. Themis Computer's broad, fully-compatible family of VMEbus CPU, I/O and Communication boards provides real-time control for this stellar project.

The result will be a new generation of optical telescope capable of imaging star systems to an angular resolution 1,000 times greater than conventional ground-based optical telescopes, and 200 times greater than the Hubble Space Telescope. Significantly, this will be accomplished at a cost of only \$10 million, 1/200th of the Hubble's cost.

This remarkable project will result in more accurate mapping and measurement of the stars and improve our understanding of phenomena such as black holes, binary stars, and quasars.

We at Themis are proud of our involvement in this endeavor.

Whether your application is on the factory floor or out of this world, Themis has the hardware and software to put it all together.

Call (415) 734-0870, fax: (415) 734-0873, or in Europe, 33.1.69.86.15.25, fax: 33.1.64.46.45.50.

At Themis, we're making the open systems promise a reality.



Americas: 6681 Owens Drive, Pleasanton, CA 94588
Europe: 29, Av. de la Baltique, 91953 Les Ulis Cedex-France

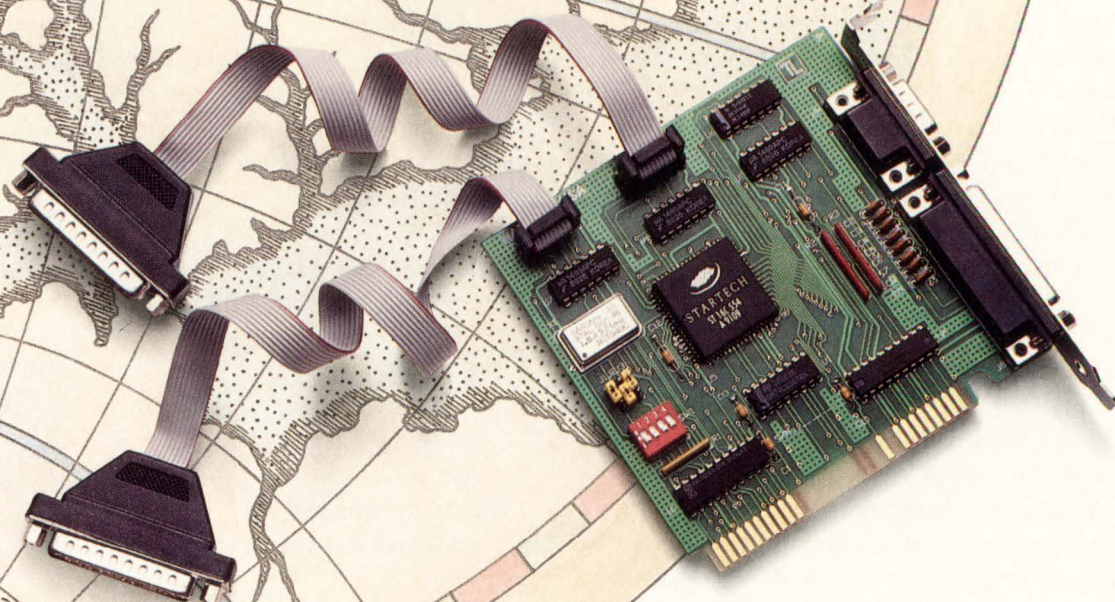
CIRCLE NO. 53

Now There's a 68 Pin Qua



ST16C554

If you're looking to reduce costs and pin counts, the ST16C554 quad UART with FIFO from STARTECH can make a world of difference. This PC-compatible quad UART offers FIFO, modem control signals and an internal programmable baud rate generator. And it's fabricated in CMOS for low power drain and high speed performance. Best of all, its evaluation board is available now.



quad UART for Both Worlds.



ST68C554

Now you can squeeze more out of your board for less with the VME-compatible ST68C554 quad UART with FIFO from STARTECH. Available at a lower price than the competition, the ST68C554 brings you world class performance. And unlike the competition, it provides a complete modem interface.

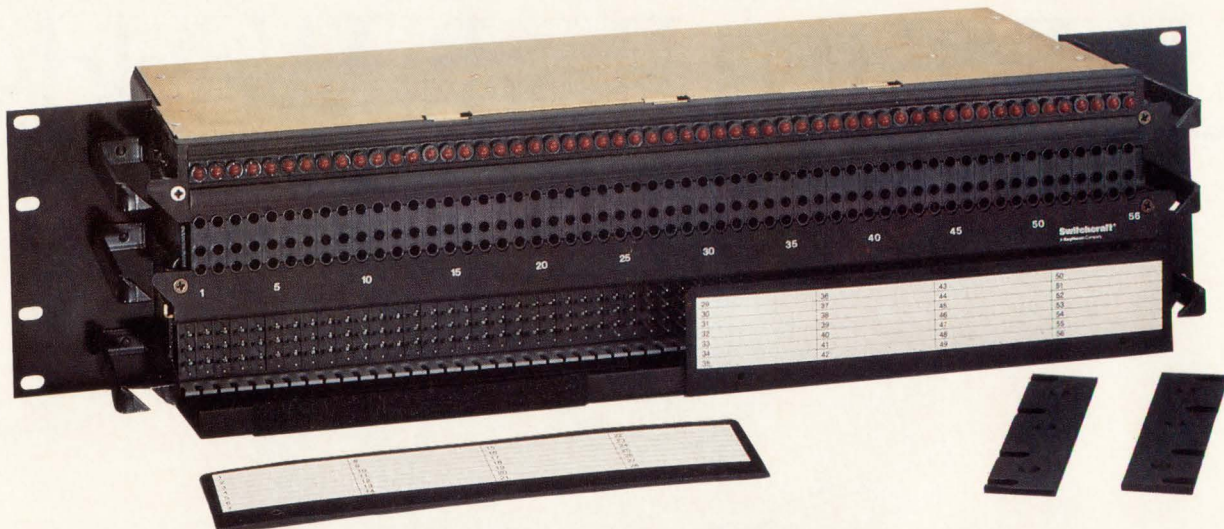
PRODUCT NUMBER	DESCRIPTION	PACKAGE
ST16C550	UART with FIFO	40 PDIP/44 PLCC
ST16C552	2 UARTS with FIFO + printer	68 PLCC
ST16C2550	2 UARTS with FIFO	40 PDIP/44 PLCC
ST16C554	4 UARTS with FIFO	68 PLCC
ST16C450	UART	40 PDIP/44 PLCC
ST16C452	2 UARTS with printer	68 PLCC
ST16C2450	2 UARTS	40 PDIP/44 PLCC
ST68C554	4 UARTS with FIFO for VME-BUS	68 PLCC

Whatever your application, whatever your operating system, we've got the perfect quad UART. For more information on our complete family of products and quad UART samples, call STARTECH: 1 (800) 245-6781 or (408) 247-8781. FAX (408) 247-0292.


STARTECH
SEMICONDUCTOR, INC.

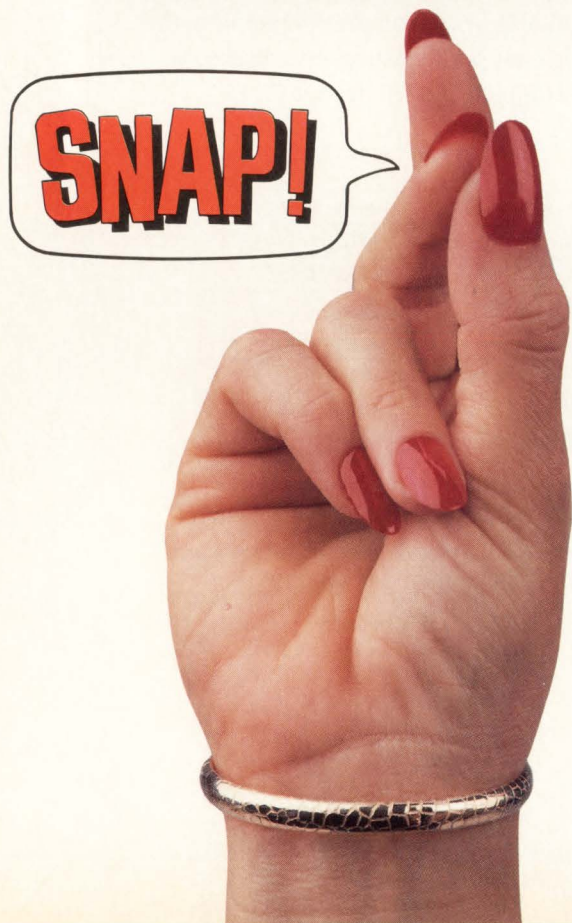
1101 S. Winchester Blvd., Bldg. A101, San Jose, CA 95128

CIRCLE NO. 54



IT'S TIME TO MAKE THE **SNAP DECISION!**

**SWITCHCRAFT'S
NEW SNAP-56 . . .
IT'S ONE OF THE
SMARTEST DECISIONS
YOU'LL EVER MAKE!**



Making the right business decision always takes time. But choose the new **SNAP-56** and you'll discover a whole new way thinking. The **SNAP-56**, with full UL approval, now features universal 19 and 23 inch mounting flanges. These separate flanges make fast mounting in either size configuration a snap.!

FEATURE BY FEATURE, THE SNAP-56 WILL HELP YOU MAKE A TIMELY DECISION:

- Switchcraft . . . 1st with total modularity, front cross-connects, jacks, and monitor LED's are removable from front of panel.
- Total flexibility, wiring of all cross-connects can be made or changed from front of panel; jacks and circuit cards can be used at any location.
- High performance patching circuits for connecting, monitoring and re-routing facility digital signals.
- High density, 56 circuits in 19 inch panels.
- Total in-service maintainability, all individual circuit elements (jack, circuit board, LED) can be changed, replaced or modified without disrupting other channels.

PLUS MANY MORE FEATURES!

When you add on-time deliveries, responsive customer service and competitive pricing, you'll come to one of the best business decisions you've ever made . . . in a snap!

The SNAP-56 Jackfield, only from Switchcraft!

For more information and specifications call Richard Neidl at (312) 792-2700, Ext. 232. or FAX your request to (312) 792-2129.

Switchcraft

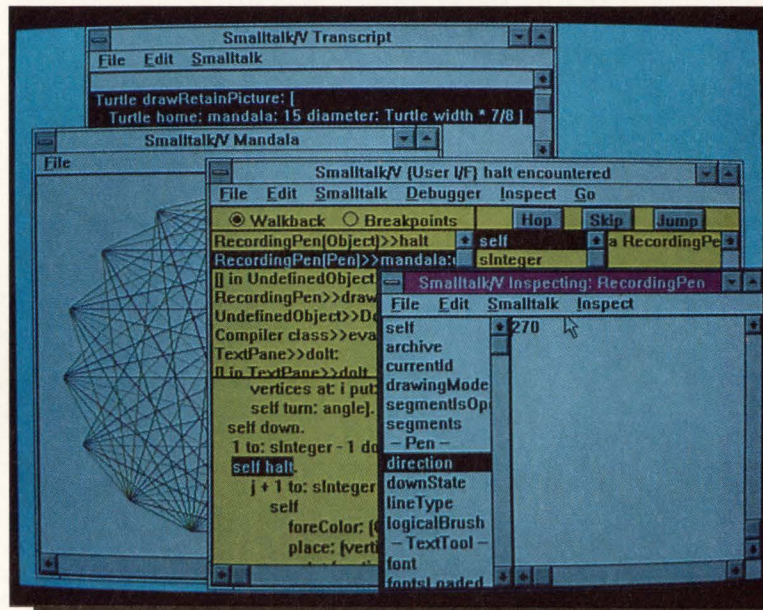
A **Raytheon** Company

5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
FAX: (312) 792-2129

Object-oriented tools expand the repertoire of real-time developers

Object-oriented programming eases problems caused by program size and complexity, and its benefits are coming to real-time applications.

Tom Williams
Senior Editor



Object-oriented software technology has become one of the major concerns of the computer industry for the '90s. The hoped-for benefits of object orientation have spawned a huge amount of activity in the design of object-oriented languages, database systems, programming environments, and third-party support products. It has also raised a number of "cultural" issues that revolve around the way programmers do their work and how they must adapt to an object-oriented discipline.

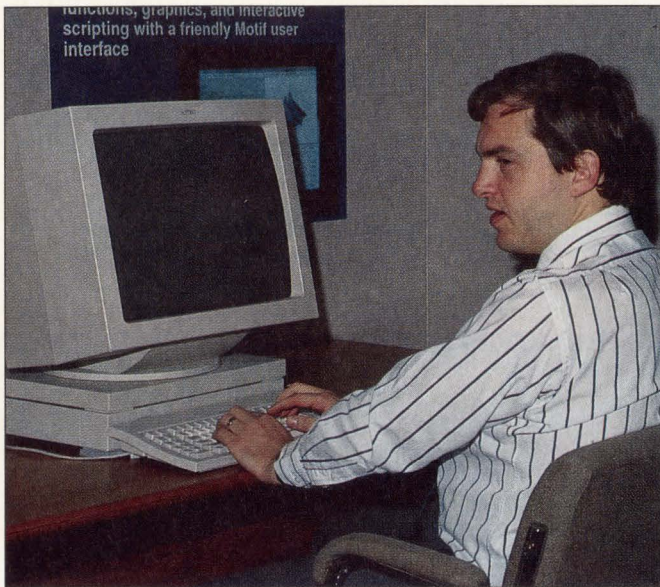
The advantages offered by products and technology available today are causing many organizations to make a commitment to object orientation. Among these benefits are reusability of code, the ability to manage increasingly complex applications, and the ability to more easily extend and modify existing software products. And the benefits appear to apply to all ranges of applications. "The techniques really apply to any type of application that you're creating and are almost independent of the language you're using," says Zack Urlocker, Turbo Pascal product manager for Borland International (Scotts Valley, CA).

David Hoffman, president of TeamOne Systems (Sunnyvale, CA), makers of the TeamNet product, which comprises software for development project management in CASE, CAD/CAM and CAE disciplines, says that object-oriented technology is especially appropriate for the engineering field because "one is dealing with objects such as circuits, ICs, software modules, and the like. And one needs to deal with these objects in a way that's manageable." He says that rather than having the behavior of objects known to the entire monolithic system, it's easier to partition their behavior within the objects themselves, "because then you can reuse components more easily and the system is more scalable. You can evolve the system more easily."

These observations touch on just some of the more formally defined characteristics that make object-oriented technology attractive. First, the idea of objects with attributes is not new. Integrated Systems (Santa Clara,

Smalltalk usually comes with an integrated development environment. Modifications have been made recently to adapt Smalltalk for embedded applications that can run in ROM without having to include all the tools of the programming environment.

OBJECT-ORIENTED PROGRAMMING



Michel Floyd of Integrated Systems says his company's investment in reworking its entire product line in C++ is necessary because "we had such a large product in so many pieces that we needed a lot of people to work on it, yet it was impossible to manage that effectively."

CA), a vendor of control engineering design software, developed a product called SystemBuild with which the user puts together control blocks in a hierarchy of functions and assigns behavior to design control systems. But it was possible to represent such an environment without using object-oriented programming internally. Michel Floyd, manager, CAE product development, at Integrated Systems, notes that the complexity of the product and customer demands for enhancements are forcing the company to make the "internal representation of its products object-oriented."

The move to object-oriented representation in the internals is seen as critical to both the development of new applications and the maintenance of existing products. "We found we just couldn't deliver what the customers were asking for in a timely manner," Floyd says. "We were constrained by the framework we had built for ourselves."

Languages and tools

Perhaps the most striking difference between modern structured languages and object-oriented programming is in the approach to constructing code. In languages such as Pascal and C, there's a relatively small list of reserved words and syntax rules out of which the programmer can construct enormously elaborate programs. In pure object-oriented programming, these words and syntax rules are encapsulated within a large number of "classes" of objects. A class describes a set of objects with similar characteristics.

An object is an "instance" of a class with an actual state (data) that can be acted on by the methods of that class. Programmers construct code by browsing the class library and selecting those objects that will do what the programmers want. Encapsulation also means the programmer can try out the objects' behavior on the spot to see if they are what the programmer really wants before including them in the program.

The two currently most popular

languages for object-oriented programming, Smalltalk and C++, reflect this different approach to programming. Smalltalk is more than a language; it's a programming system. The user is forced to work within the object-oriented framework of browsing the class library, selecting objects, trying them out, and building them into the program.

In C++, the programmer could choose to program entirely in standard C if desired, or to select only those objects the programmer wished to build into the code. While arguments can be made for the sink-or-swim method of Smalltalk, C++ is the most widely used language simply because of the vast number of trained C programmers in the world.

Objects in real time

For object-oriented development of embedded and real-time systems, C++ is clearly in the lead because it's compiled completely to object code. Smalltalk, on the other hand, uses a byte-code interpreter and until recently only came in versions that were integrated with the rest of the programming environment, such as browser, editor and debugger. The interpreted nature of Smalltalk has led to the conclusion that it must be slow, and in traditional computer architectures that has been the case.

Advantages of objects

The advantages of objects can be largely described by three words: encapsulation, inheritance and polymorphism. Encapsulation means that an object contains both a state and the operations that can be performed on that state. Actions on an object's state, called methods, are initiated by messages sent to the object. With encapsulation the user really need not worry about how an object performs its function but simply what it can and cannot do. Users can be confident that adding an object to existing code will not cause unpredictable things to happen to other parts of the program.

Inheritance is the ability to associate characteristics common to all members of a class of objects; lead, gold and iron, for example, all have the characteristics of metal. In object-oriented programming, subclasses of objects can inherit characteristics of the class they belong to. Drawing a square or a triangle uses methods inherited from the method of drawing a polygon. Different types of triangles in turn inherit characteristics from the general class of triangle, such as having three sides.

Polymorphism means that an operation to be performed on an object is determined by the type of object it addresses. The same command to edit the drawing of an IC, for example, would act differently when applied to the drawing of a printed circuit board because the characteristics of the two objects are different as are the internal methods that act on them. But the programmer, as well as the user, need only deal with the concept of "edit." The ability to generalize behavior over many types of objects allows a higher degree of abstraction in software design since the programmer only has to think about specifying actions rather than the details of how to implement them.



First, we're delivering 040 VME single board computers today. In quantity. So you can get started while the rest of the world waits for a delivery date from other suppliers.

Second, our new CPU-40 board is setting performance standards nobody else can touch. Like 30,000 dhrystones sustained at 25 MHz*. And DMA transfers at a screaming 50 Mbytes per second sustained (3 microseconds on the VMEbus).

So it might just be the last 040 board you'll ever need.

That's because we've fully optimized the on-board architecture. Thanks to our 281-pin gate array, DMA operations can be handled between on-board RAM, the VMEbus and on-board I/O devices. Or through our FLXi interface to other I/O drivers.

All of which means the CPU is free

over 75% of the time to run your application.

Of course, we provide comprehensive support with the industry's best-rated documentation**, complete systems integration support and technical assistance.

CPU-40 PERFORMANCE CHARACTERISTICS

Data from	CPU	CPU	CPU	CPU	VMEbus	SCSI*	Floppy Disk*	Ethernet*	Shared RAM*	VMEbus*
Transfer to	Shared RAM	EPROM	Serial I/O Timers	SCSI, Ethernet Controller, Floppy Disk	Shared RAM	Shared RAM	Buffered RAM	Dual-port RAM	VMEbus	VMEbus
Transfer Speed	53.7 MB/sec	16 MB/sec	2 MB/sec	2 MB/sec	5 MB/sec	4 MB/sec	500 Kbit/sec	10 Mbit/sec	15 MB/sec	15 MB/sec
Local 68040 CPU Operation	100%	100%	100%	100%	70%	80%	100%	100%	75%	100%

*DMA x FPS

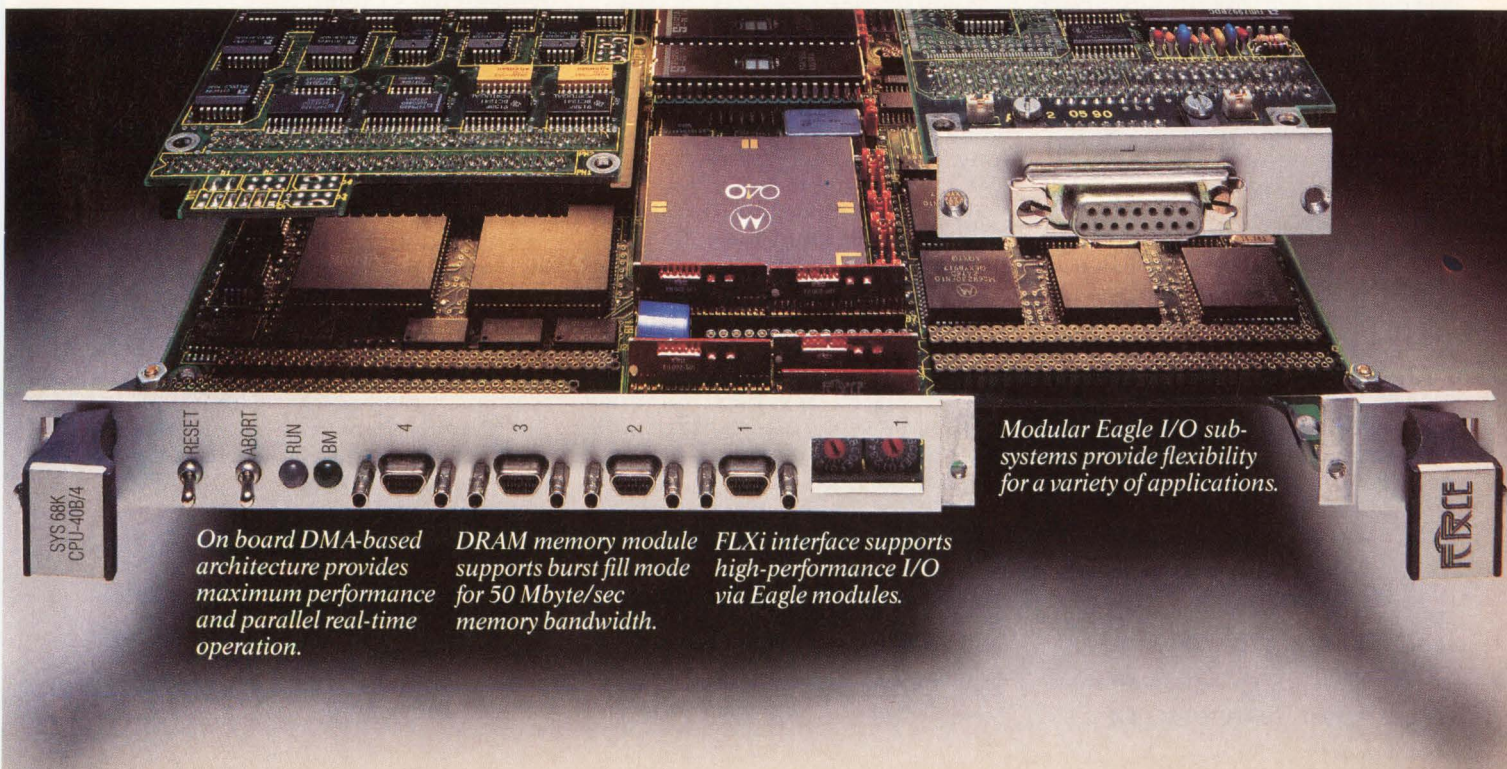
So be the first in your company to turn 040. Call 1-800-BEST-VME, ext. 40, for more information or fax a request to (408) 374-1146 for an immediate response. It'll be to your lasting advantage.



FORCE Computers, Inc. 3165 Winchester Blvd. Campbell, CA 95008-6557
 *Actual dhrystone results may vary depending on compiler used. **Computer Design News, March 12, 1990. All brands or products are trademarks of their respective holders. © 1991 FORCE Computers, Inc.

CIRCLE NO. 56

WHY THE FIRST 040 VME MIGHT AS WELL BE THE LAST.



Modular Eagle I/O sub-systems provide flexibility for a variety of applications.

On board DMA-based architecture provides maximum performance and parallel real-time operation.

DRAM memory module supports burst fill mode for 50 Mbyte/sec memory bandwidth.

FLXi interface supports high-performance I/O via Eagle modules.

OBJECT-ORIENTED PROGRAMMING

On a modern RISC processor such as the Motorola MC88000, however, the entire byte-code interpreter and the Smalltalk virtual machine, which consists of about 100 byte codes or Smalltalk instructions, can run out of the on-chip cache.

Running the interpreter in the cache means that fetches from memory are a relatively small number of high-level instructions that generate greater numbers of machine code instructions out of the cache. That machine code runs much faster when it emanates directly from the cache than if it had been fetched from memory as normal compiled

Recently, however, Object Technology International (Ottawa, Ontario) has modified Smalltalk/V in a licensing agreement with Digitalk for embedded applications. Embedded Smalltalk/V is available for the Motorola MC680X0 family of processors and also in versions that will run on top of commercial real-time executives such as VRTX by Ready Systems and VxWorks by Wind River Systems. Object Technology International (OTI) also provides a configuration control environment called Envy/Developer that has, among other things, a packaging facility, which can separate the execu-

garbage collection techniques are not up to hard real-time yet ... where it's a predictable, schedulable action. Currently we don't have one of those, but it's a high priority for us." Still, a great deal can be done in embedded control that does not need submicrosecond response times.

Factory control systems

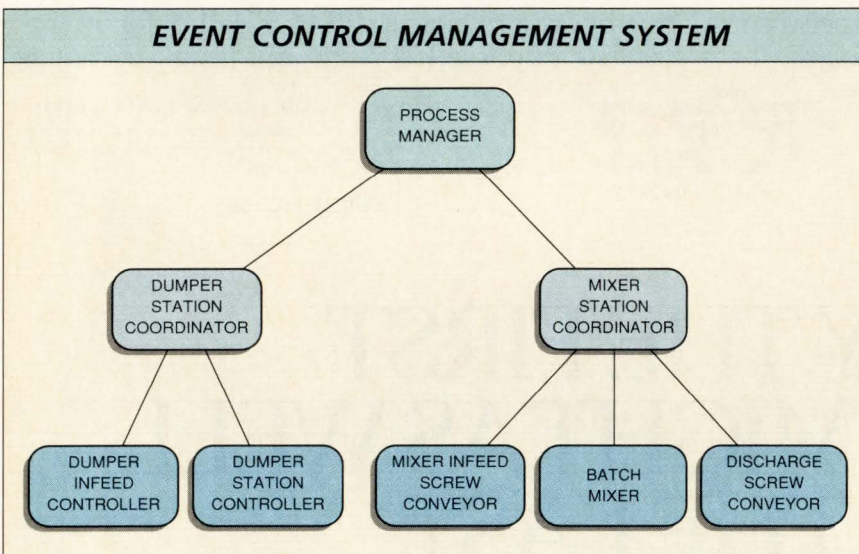
A system for constructing modular factory control systems built on the object-oriented concept is the Event Control Management System (ECMS) by Forth (Manhattan Beach, CA). ECMS is based on software objects called processes and receptors. A control system can be constructed by assembling processes and receptors into a hierarchy in which a process receives input from a subordinate process, acts on that input and sends messages back down to its subordinate and/or reports its new state to its supervisory process.

A process can be thought of as a state engine that contains a state (data) and one or more actions (methods, in object-oriented terminology) that it can perform on that state. The actions it performs internally can cause its state to change to one or more different defined states. A receptor is an object that is generally used for communication between processes and between processes and I/O. Receptors provide a means of bringing an event—such as the change in state of a digital point—to a process. Each higher level in the hierarchy allows a greater degree of abstraction in describing the system.

Interestingly, the lowest levels in the ECMS hierarchy, starting with the I/O level, have the highest priority. This means that in terms of levels of priority, the lower-level processes are handled before the higher-level ones. The entire hierarchy of processes is coordinated by an executive task running under Forth's pF/x real-time operating system.

Databases aid design systems

Complex data structures that don't lend themselves to the traditional relational database tools are typically found in applications such as engineering design and CASE, says Ian Schmidt, director of product marketing at Object Design (Burlington, MA), which produces ObjectStore, an object-oriented database system. One way design applications differ from general business applications is that they use



In an application based on Forth's Event Control Management System—here a materials mixing system—discrete process objects are arranged in a hierarchy such that each subordinate process reports conditions upward to its supervisor process and receives events from its subordinates. It can also send messages down to subordinates to cause them to change to a desired state. The highest priority is assigned to the lowest level of the hierarchy, the I/O.

code would be. "That's going to make us rethink some previous assumptions about interpreted languages and speed," says Dan Goldman, vice-president general manager of marketing and advertising at Digitalk (Los Angeles, CA), publishers of the leading version of Smalltalk.

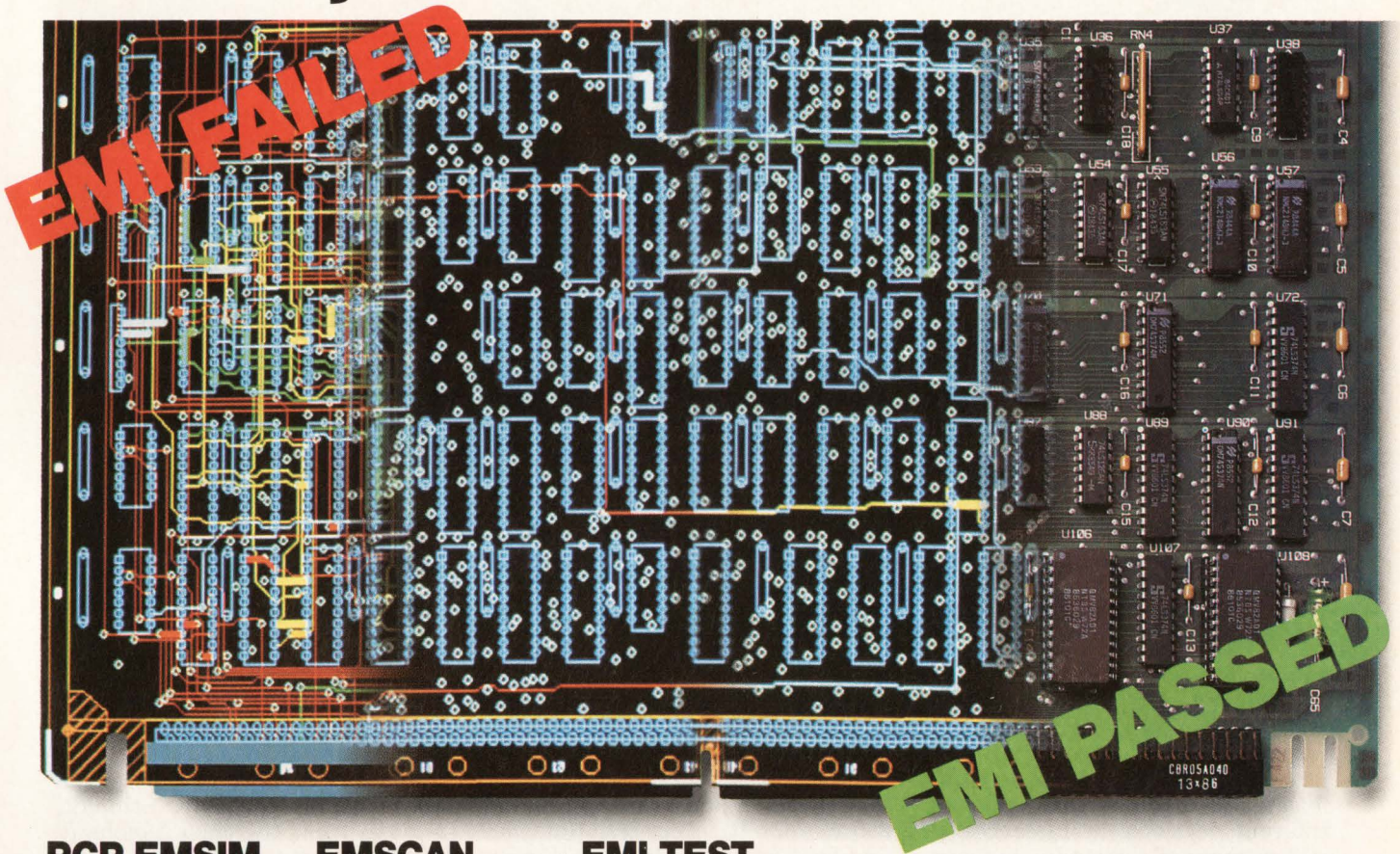
But speed isn't the only requirement for real time; preemptability and predictability are also essential. One characteristic of Smalltalk that has inhibited its acceptance for such applications is its automatic garbage collection facility. The danger is that the program might be garbage collecting—searching memory for program or data segments that are no longer active and reclaiming the unused memory blocks—when a critical interrupt could occur.

table part of a Smalltalk application from the rest of the programming environment and produce a ROMable run-time module.

Currently, embedded Smalltalk/V is preemptable but not fully deterministic. When running with a real-time executive, for instance, interrupts are caught by the real-time executive and forwarded to the virtual machine, which has a fixed response time. The garbage collection facility, however, is not yet fully predictable. John Duimovich, manager of embedded systems at OTI, says the garbage collector has been built to "average out the pain of garbage collection on a workstation." The scavenger routine interrupts for about 0.001 seconds every 10 seconds. "However," he notes, "the best

Minimize EMI During PCB layout before you build it!

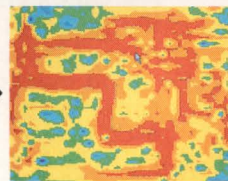
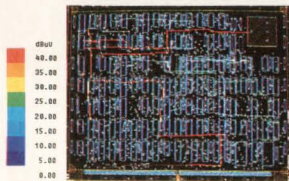
Get your product to market fast and save time and money in the process! Now you can optimize your circuit boards early in the design cycle before hardware prototyping with a simulation tool developed by Bell-Northern Research for Northern Telecom. As a complement to the circuit board design system CBDS, PCP EMSIM allows designers to select, position and route components for minimum EMI emissions, decreasing the risk of failing government regulations, such as FCC, CISPR and VCCI.



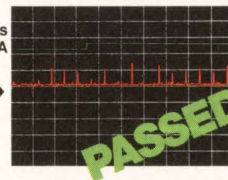
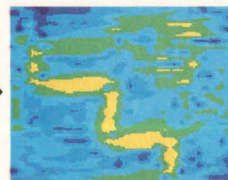
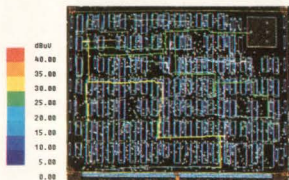
PCP EMSIM

EMSCAN

EMI TEST



Hot traces (shown in red) identified early at the layout stage with PCP EMSIM indicate that this board design will likely fail EMI radiated emission tests. As shown here, subsequent board testing on the EMSCAN hardware scanner and open field tests confirm the PCP EMSIM results.



Optimizing component selection, placement, and routing using PCP EMSIM enables you to reduce EMI before costly hardware prototyping. Scanning the revised prototype board on EMSCAN confirms the reduction in EMI, which is again verified by open field tests.

Marubeni
INTERNATIONAL ELECTRONICS CORPORATION

For complete technical details, call or fax us today.

20 William Street
Wellesley, MA 02181
Tel. (617) 237-2115
Fax (617) 237-1046

Come and see
PCP EMSIM &
EMSCAN at
Booth

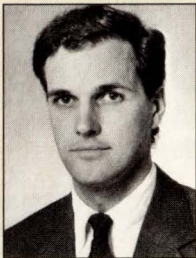
1361



PCP EMSIM, EMSCAN and CBDS are trademarks of Northern Telecom Limited.

CIRCLE NO. 57

Industry group working toward standards for object-oriented programming



To bring object technology into the mainstream, the industry must agree to cooperate. The Object Management Group (OMG) was founded in

April 1989 to establish a framework for object technology supported by detailed and widely available interface specification. From just 9 initial members, the group has grown to more than 110 members representing over 80 percent of the companies pursuing object technology development. A nonprofit corporation, the OMG is headquartered in Framingham, MA with marketing offices in Boulder, CO. The OMG welcomes participation by both users and developers of object technology.

The Object Management Architecture (OMA) Guide, released in October 1990, was the first product of the

group's efforts. The OMA Guide contains the architecture for an object-oriented environment along with a glossary of terms to standardize the terminology used to describe object technology. The architecture forms the foundation for the OMG's work. From this the group will adopt interface specifications that will let developers build products that fit into an integrated environment constructed from products offered by many vendors.

The architecture gives a framework for an object-oriented environment. The key elements are applications, shared facilities, common services, and the object request broker. Currently the OMG is working to adopt interface specifications that will support the passing of messages across an object-oriented environment. After the architecture, the most important element was deemed to be the ability to establish communications among the objects in an object-oriented environment.

The OMG's work plan extends over

the next two years. In that time the group will adopt interface specifications, based upon commercially available products, for applications interfaces, database interfaces and other specifications to support the adopted reference architecture. The group has recently issued a Request for Information for an object model, which is a formal description of the allowable behavior and visible characteristics of objects within an object environment. Once completed, the object model will act as a bridge for the many proprietary object models being developed.

In order for object technology to be widely and quickly adopted, it must adhere to a nonproprietary architecture with widely available interface specifications. This will create a market condition where both users and developers can buy and build products, confident in the ability of those products to communicate.

Chris Stone, president, Object Management Group

the concept of things being derived from other things. One creates something and then modifies it—but may wish to save the original version. Or, one takes an existing object and modifies that, creating different versions, or instances. A vast number of objects in engineering are represented as aggregations of parts or levels of detail or a combination of both. And the inheritance and encapsulation characteristics of object-oriented software technology fit such a means of representation naturally.

Schmidt also notes a particularly good fit between object-oriented languages and the kinds of entities that are stored in an object-oriented database, and that there are very few sophisticated applications that have a CAD or design flavor to them that aren't being written in C++.

"C++ is attractive because it almost has the capability within it for people to design their own language," he says.

Users design their own classes and types starting with some basic given classes and then making modifications. Thanks to the property of inheritance, new instances of an ob-

ject that a user creates can reuse the code of that class; the user changes or adds only those attributes that make the new object unique. "The beauty of this," says Schmidt, "is that there's a long start-up time to define your base classes. But you find that as you're defining classes

***With encapsulation
the user need not worry
about how an object
performs its function
but simply what it
can and cannot do.***



for your application, you keep borrowing from stuff that already exists, and before long, you're writing less and less code."

Not only do new classes inherit the characteristics of previously defined classes, but it's also possible to build in the characteristic behavior (methods) of the data objects. Because the behavior is built into the

object, the user need not worry about the details of handling any given object since that object knows how to respond to messages it receives. "C++ gives you an incredible data modeling tool," says Schmidt. "You can treat the class 'elephant' the same as the class 'integer' (for example, store, delete, edit) because the language knows about all the things 'elephant' can do and how."

And this is where the object-oriented language begins to overlap with the object-oriented database. Since both work with objects, and since objects are the same thing in both language and database—namely data and the methods to operate on that data—one can refer to objects in the database the same as if they were parts of the language. This is an essential feature for those who wish to use object-oriented databases in large design environments.

■ A user's move to objects

Valid Logic Systems (San Jose, CA) has incorporated an object-oriented database in its newest product, called Design Manager. Design Manager fits into Valid's Framework

NEW

For All Your Embedded AT/VME Requirements

LOWEST COST

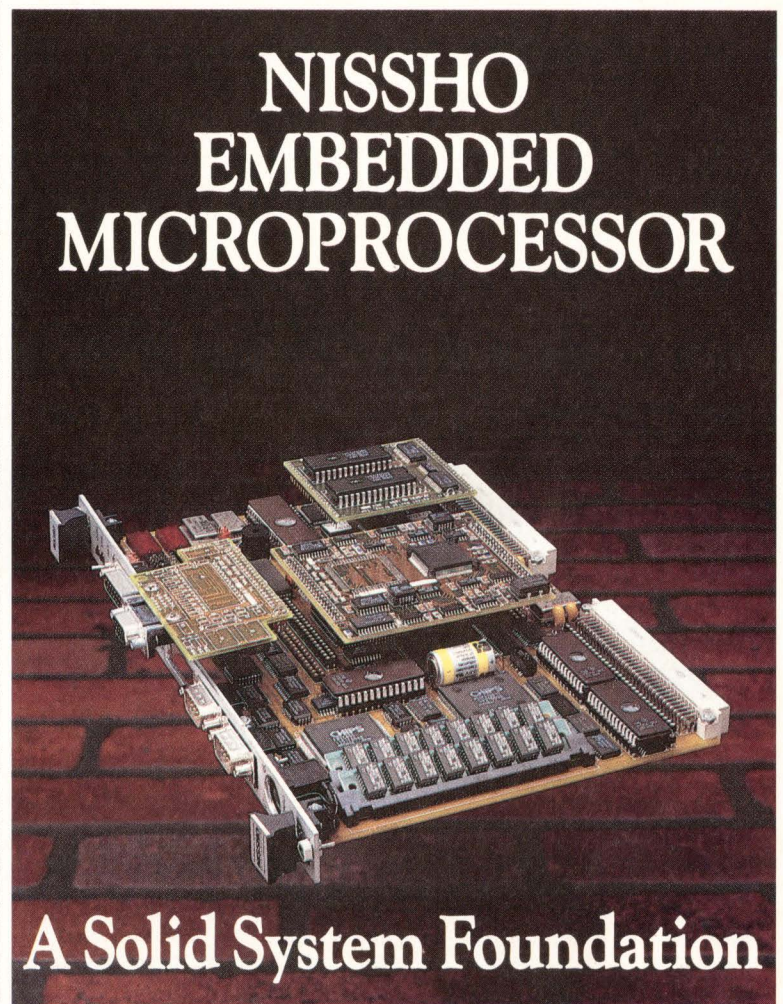
N5280 (Models 22 to 54)

- 80286 or 80386SX CPUs
- 20MHz, 25MHz, or 33MHz
- PC/AT Compatible
- VMEbus Master or Slave
- 1 to 8 MB DRAM
- 64KB to 512KB Dual Ported SRAM
- IDE Hard Disk Controller
- 5 Video Options
- Single 6U Size Board

HIGHEST PERFORMANCE

N5280 (Models 63 to 84)

- 80386DX or 80486 CPU
- 25MHz or 33MHz
- PC/AT Compatible
- VMEbus Master or Slave
- 2 to 32 MB DRAM
- 1 MB Dual-Ported SRAM
- SCSI Host Adapter
- 5 Video Options
- Single 6U Size Board



SINGLE BOARD SOLUTION

The NISSHO N5280 is the only complete 486 AT/VME Embedded Microprocessor built on a single 6U size VMEbus board.

SOFTWARE

The N5280 comes with extensive software support including configuration and driver utilities with source code for ease of

installation. Typical Operating Systems include MS/DOS 4.01 and 3.3 from Microsoft, VENIX/386 from VenturCom, and OS-9000 version V1.0.1 from Microware.

ADD-ONS

The N5280 has an ATbus extension for accommodating 1/2 and 3/4 length AT cards as well as a SCSI Host Adapter for built in or external disk and tape drives.

FOR A FREE 28-PAGE HANDBOOK, CALL (800) 233-1837 — in California (714) 261-8811

TIME TO MARKET IS THE KEY TO YOUR SUCCESS.

NISSHO
E L E C T R O N I C S

17320 Red Hill Avenue, Suite 200 • Irvine, CA 92714 • FAX: (714) 261-0934

CIRCLE NO. 58

OBJECT-ORIENTED PROGRAMMING

design environment and is a universal storage mechanism for managing data and the output of Valid tools. "You want to combine an object-oriented programming language with an object-oriented database and see how well you can map C++ classes into the database," says product manager Larry Rice.

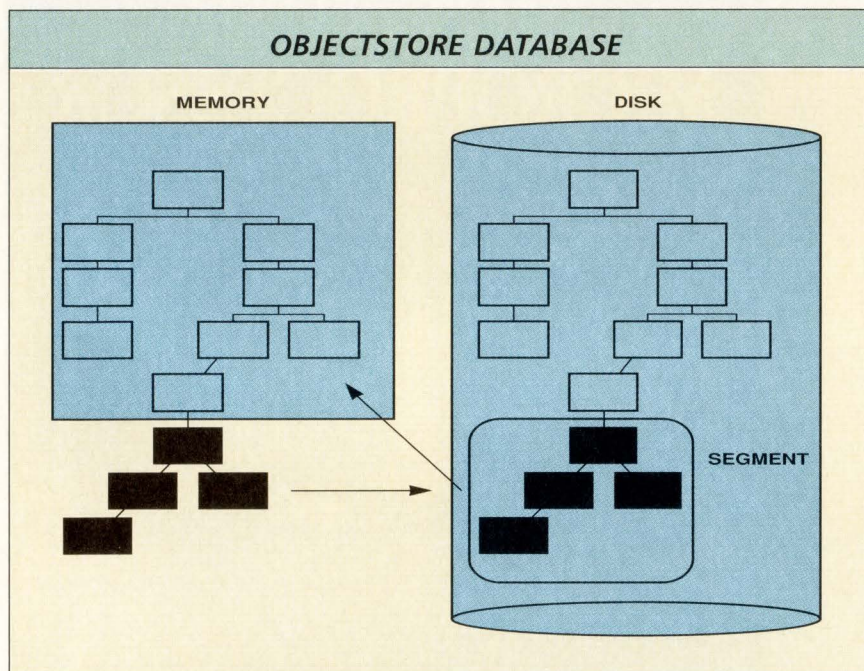
The idea is that one can model all the types of data one wants to store

representations of those parts. "So instead of just having gate-level representation, we're having VHDL and physical representation and who knows what else," he says. Now, he adds, the whole EDA marketplace is moving to editors that can deal with such different representations as logic, behavior and physical attributes all at once, and that's possible thanks to the fact that an object-ori-

fundamental approach to programming isn't changed as well," says McKenna. "It's a lot of effort; there's a learning curve that takes about six months." But he cautions that while making the change isn't worth the trouble from the point of view of individual productivity, "it's worth it from the point of view of the reuse of software in the long term." So as an organization moves into an object-oriented mode, it will create objects tailored to its application needs that can be reused and shared among other members of the organization. Eventually, it will amass an inventory of commercially acquired and custom-designed—or derived—software components.

Increasingly, the programmer's job will entail finding the right component (object) for the job by browsing class libraries—much like hardware engineers perusing their Texas Instruments or Motorola data books. McKenna says that software engineering is going to have to change to where programmers are told, "What you read is more important than what you write." Finding the right objects and figuring out how to use them to build solutions will be the major activity.

But the cultural burden is not just on programmers. "Managers are rewarding programmers for writing code, so it's not in the programmer's interest to find an object that he can use because it doesn't add to his line count," says McKenna. So there has to be a way to reward programmers for delivering solutions to problems rather than grinding out and debugging code. ■



Object Design's ObjectStore database uses a virtual memory mapping architecture that can preserve the inheritance relationship of data objects. If an object is not in physical program memory, it's brought in from disk. This gives developers a "single-level store" of objects.

in the system, and the database can accept them just the way they were modeled by the programming language. With a relational database, the programmer almost has to unravel the structure to deal with it and store it. As Object Design's Schmidt puts it, "That's almost like taking your car apart at night before you put it in the garage." ObjectStore, on the other hand, maintains the class hierarchy of stored objects. The database is retrieved in virtual memory, so that if a desired object is not in physical memory, a page fault will fetch it off the disk, maintaining all its links within the schema so the user can easily move up and down the hierarchy.

But hierarchical organization of data is not all one gets from object-oriented data storage. It allows storing the models of electronic parts, but not just electronic parts, says Rice. It can also provide different

ented programming language such as C++ maps so well to the database.

Making the move mentally

"Some people believe it (object-orientation) is the same old thing in new packaging," says Jeff McKenna, founder of McKenna Consulting Group (Portland, OR). "I don't happen to believe that. It's a fundamentally new way of thinking about software." Adopting an object-oriented programming discipline means changing some basic ways of thinking for an individual, and so it can entail some wrenching changes for an organization. And it must be remembered: in today's industry, programming is not an individual activity; it's an organizational activity that requires planning, coordination, communication, and management.

"Shifting to an object-oriented environment isn't worth it if the user's

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Borland International (408) 438-8400	Circle 201
Digitalk (213) 645-1082	Circle 202
Forth (213) 372-8493	Circle 203
Integrated Systems (408) 980-1500	Circle 204
McKenna Consulting Group (503) 694-2357	Circle 205
Object Design (617) 270-9797	Circle 206
Object Management Group (508) 820-4300	Circle 207
Object Technology International (613) 228-3535	Circle 208
TeamOne Systems (408) 986-9191	Circle 209
Valid Logic Systems (408) 432-9400	Circle 210

For all of these microprocessors, you need only one name on your emulator.

	MICROPROCESSOR									
	68000	68302	68020	68030	80C186	286	386	SX	486	
HEWLETT PACKARD	👍	👍	👍	👍	👍	👍				
MOTOROLA	👍		👍							
INTEL					👍	👍	👍	👍	👍	
TEKTRONIX	👍		👍							
APPLIED	👍	👍	👍	👍	👍	👍				
MICROTEK	👍	👍	👍	👍	👍	👍	👍	👍	👍	👍

Learn one, learn 'em all

When you put a Microtek emulator to work, comfort comes with the territory.

All of our emulators make you feel right at home with windowed user interfaces and on-line help. And, our hyperSOURCE™ high level language debugger integrates the best of source level support with the hardware features you look for in an emulator.

With hyperSOURCE™, you no longer need to lower your expecta-

tions when you combine source debug with emulation.

Super support

Integrating software and hardware is never challenge-free, even



with all the right tools. Talk to our support engineers directly for quick answers to your applications problems. *With over 26,000 systems in the field, these folks are hard to stump.*

"Real" real-time

Our emulators don't add wait states, they don't slow your target, and they don't give you any surprises later.

Your final product will perform the same in front of your customer as it did with your emulator.

The Bottom Line

The choice is easy. Microtek doesn't leave any gaps in the development path. For "real" real-time emulation, easy to use features, high level language debug and a technical support system envied by our competition, we're the one.

When you add it all up, there's only one name that should be on your next emulator...

MICROTEK

The Leader In Development Systems Technology™

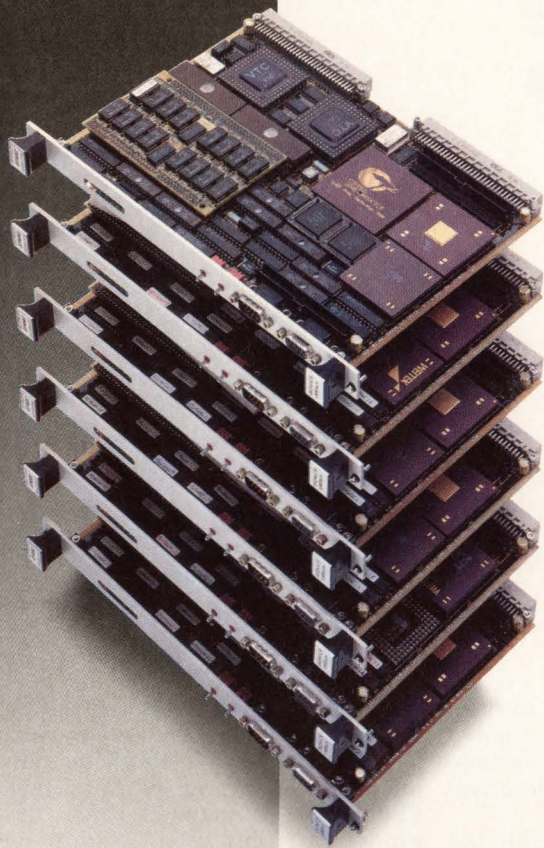
For sales or leasing information, call 503-645-7333 ext. 1

MICROTEK INTERNATIONAL, INC. - Development Systems Division
3300 N.W. 211th Terrace, Hillsboro, OR 97124 • (503) 645-7333 • Fax (503) 629-8460

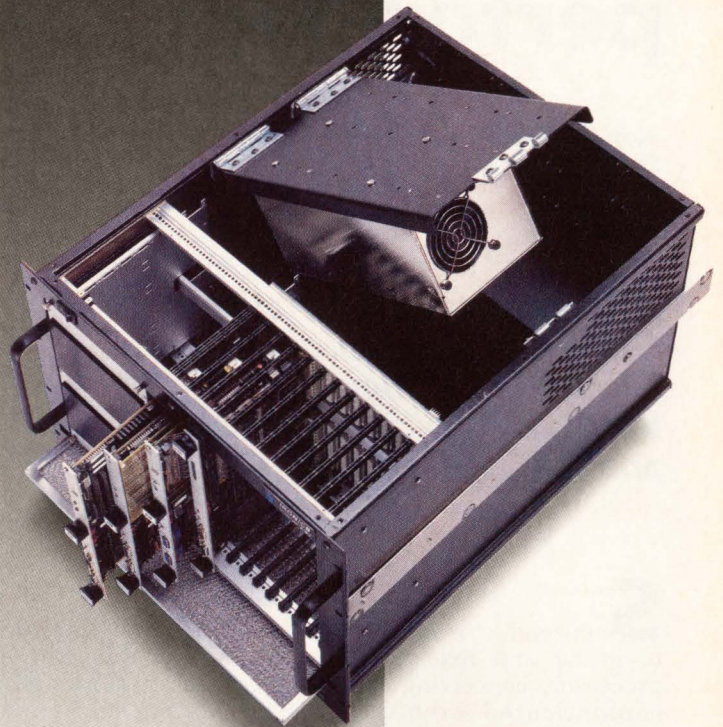
Australia: 61-3-7202399, Austria: 43-1-6271953, Belgium: 32-2-2523680, Denmark: 45-42-804200, France: 33-1-39611414, Germany: 49-89-8570000, Israel: 972-3-5447475
Italy: 39-11-503427, Hong Kong: 852-3-7443516-9, Japan: 81-3-7955171, Korea: 82-2-679-1161, Netherlands: 31-3403-91234, Norway: 47-2-289490, Singapore: 65-7468182
South Africa: 27-11-7863710, Sweden: 46-8-930000, Switzerland: 41-1-2010711, Taiwan: 886-2-7576939, Thailand: 66-2-2217040, U.K.: 44-276-685005

CIRCLE NO. 59

NOW



Multi-Processing
Real-Time SPARCs™



ICEBOX™ VMEbus
System Enclosure

it all together.

Our goal is to provide all the pieces for the best VMEbus System solutions. To this end, we have just added a full spectrum of cost effective Imaging and Graphics boards and systems.

At Ironics, we care about real world solutions. Our quest for more reliable and maintainable systems has even taken us into the realm of VMEbus enclosure design.

And now Ironics' new Systems Integration Group can help you put it all together. Call Ironics' VMEbus hotline today (800-334-4812) and ask for further information or a demonstration.

Real-Time, On Time, All the Time!

IRONICS

IRONICS Incorporated
798 Cascadilla Street
Ithaca, New York 14850 USA

607.277.4060
Fax 607.272.5787
Telex 705742

CIRCLE NO. 60

Will monolithic or multichip processors win the performance race?

Alex Mendelsohn
Contributing Editor

The era of the million-transistor microprocessor is upon us. "Megachip" blockbusters—some executing 100 Mips or more—are becoming available in both RISC and CISC designs.

Semiconductor makers continue to refine and redefine the microprocessor, conceiving increasingly sophisticated architectures on multimillion-transistor chips. Other processor architects are opting for the increased design flexibility and higher manufacturing yields of multichip processor designs. Which camp is right? More important, can either stake a clear claim to the high end of the performance spectrum? Will the fastest processors be megatransistor monoliths or multichip devices?

One key for processor architects in the monolithic camp has been the ability to keep faster transistors productively used in VLSI. Transistor-rich logic blocks now let processors schedule multiple activities per clock cycle, creating parallelism at the chip level. And optimizing compilers, able to extract parallelism from source code, are getting better.

At the same time, the clock speed of processors is increasing. Even 8- and 16-bit single-chip microcomputers of conventional architecture now routinely run with 25- and 30-MHz clocks. Speeds over 25 MHz mean that system designers must be especially wary of potential performance penalties due to physical layout. While this would seem to favor integrating all critical functions on

a single chip to minimize physical separation, the need to eventually access things off-chip keeps system layout effects a major consideration for monolithic architects.

IC makers are touting highly integrated CISC and RISC ICs and compilers. The recent superscalar, superpipelined debate has seen vendors announcing a spectrum of hardware/software architectures.

■ Partitioning is key

In the face of multiple unique architectures, partitioning is emerging as an issue. IC vendors extol VLSI—even ULSI—chips that integrate many systems-level features. But there's growing evidence that some of the largest, most-integrated silicon devices eventually may be constrained by packaging limitations and wind up in some sort of "micro-card cage" module. Texas Instruments, for example, is now experimenting with silicon "backplanes" and "plug-in" dice.

Some argue that well-partitioned silicon will become essential as the integration revolution continues. Many of the arguments in the partitioning camp make good engineering sense, especially from a cost-versus-performance point of view.

"The partitioning controversy is based on arguments between people

who relate to instruction set architecture development in silicon versus those who have to write compilers and operating systems," says Phil Hester, director of IBM's Engineering Center for Advanced Workstations (Austin, TX). "It's a delicate balancing act.

■ Silicon or software?

"The compiler folks ask what silicon does at execution time versus what a compiler does at compile time," he says. "With today's multiple execution unit designs, some people believe it's efficient to move things such as handling responsibility away from silicon and into a compiler. Others feel it's better to add such functions to the hardware.

"Silicon is very precious to semiconductor makers, especially merchant market vendors," he says. "They want to reduce die size. So, they move functions to a compiler for things such as interlocking multiple execution units."

IBM's RS/6000 multichip design embraces the hardware approach, thanks to excellent compilers and well-developed and available fabrication processes. "We don't rely on software," Hester says. "We keep interlock handling on-chip because with our fab process we pay a minimum penalty in terms of silicon area

and cycle time/clock rates. And we build a set of efficient compilers for a number of languages without having to tie specific implementation details to the compiler.

"It's true that the simpler you make a chip, the easier it is to prove that it works correctly. The more special cases a chip has to handle, the more design validation you have to perform, especially simulating gate level descriptions to convince yourself it'll work as designed."

A critical capability for IBM resides in its IC validation technology. "If you have hardware simulation engines that let you run a few hundred million simulation cycles per week, you'll come to different conclusions about partitioning issues than if you have to let simulations run for months," Hester says. "Testability is at issue too. If you have sophisticated validation tools, time-to-release-to-manufacturing penalties for IC makers are reduced."

■ Partitioning choices

Nathan Brookwood, marketing director for Intergraph (Palo Alto, CA), acknowledges IBM's leadership. "The fastest machine today, the IBM RS/6000, using a multichip CPU design, proves there really are multiple schools of thought about architecture and partitioning," he



FAST PROCESSORS

says. "We eschew the semiconductor macho mentality in our Clipper chip set to get the highest possible performance consistent with reasonable cost."

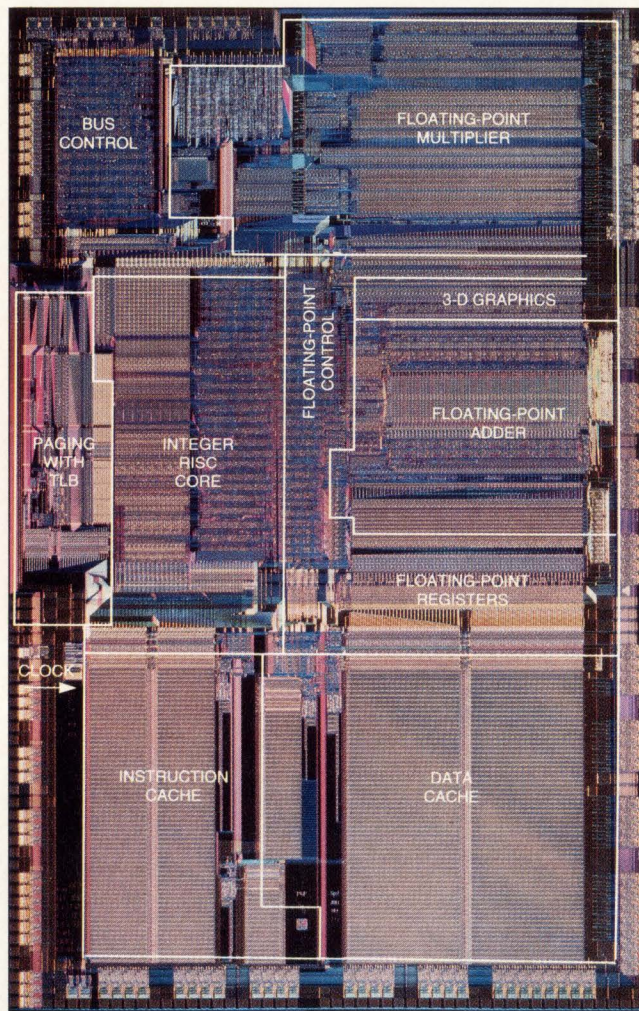
Intergraph's Advanced Processor Division's latest Clipper (there have been three Clipper "compute engines" since 1985) is enjoying popularity in the company's RISC-based CAE products. The system makes use of minimal cache and offers moderately powerful floating-point ability.

Intergraph's approach relies on efficient partitioning, low-voltage logic, advanced packaging, and multichip modules (MCMs). The company's reason for using MCMs is multifaceted. Its chip set designers dropped logic operating voltage to 1 V instead of the more typical 5-V TTL or even 3.3- or 3.6-V levels. Of course, there were compromises. The Clipper chips require two voltages—5 V for internal logic, along with a reference signal, and 1 V for I/O signals. "But, as we lowered logic levels, we got away from using conventional or multilayer circuit boards and got onto a better surface in MCMs," says Brookwood. "Raw dice are bonded directly to chips rather than having packages placed on a board. MCMs give us control over parasitic capacitance and inductance."

Hybrid-like packages, eliminating long conductors between dice and packages, let Intergraph realize 1- or 2-ns off-chip delays. "It's almost as good as the on-chip prop delays people tout," Brookwood says. "With low-voltage logic and MCMs, you don't have to drive nearly as much capacitance."

Intergraph says wire-bonding techniques have dramatically improved over the past few years. Assembly yields and reliability are exceptional. "We don't sacrifice anything," Brookwood says.

MCM performance data from Texas Instruments (Dallas, TX) supports Intergraph's findings. TI's customized MCMs, based on molded modules using ceramic substrates,



The first 64-bit RISC CPU chip, Intel's i860 architecture emphasizes balanced integer, floating-point and graphics performance. Its floating-point and graphics performance have made it more successful as a graphics and math accelerator than as a CPU.

typically result in cost reductions from 2 times to as much as 10 times at the systems level.

TI found that stress, moisture and thermal sensitivity fell by 3 to 8 times with MCMs. Lead length reductions of 6 times resulted in inductance reductions of 60 times, with load capacitance lowered by 6 times. Critical path delays with MCMs were typically reduced by a factor of three, say TI engineers.

"The argument for large-scale integration is it eliminates interchip propagation delays like you have with multichip designs," says Intergraph's Brookwood. "But, megachips fundamentally constrain the hardware you can use in a system. Megachip vendors force architectural compromise. They want to put more and more on a single chip. If they leave things off, they create

opportunities for competitors to provide functionality. They would rather not do that.

"And, when it comes to testing, with off-chip cache it's easy for a logic analyzer to trace program execution. With on-chip cache, you can't do that. The more highly integrated, the more difficult it is to know what's going on within the chip unless you want to pay a penalty in silicon real estate for diagnostics."

Transistor-bound caches

Another problem for monolithic processor architects is transistor cost of caches. "Many highly integrated chips typically have only 1-, 2- or 4-kbyte caches, which prove not nearly large enough," says Brookwood. "People will discover that they'll really need much bigger caches of 16 or even 64 kbytes."

IBM's Hester agrees. "If I had future submicron technology, I'd allocate more of the multimillion device budget on much larger caches to get the off-chip bandwidth requirements down. Then you'd see dramatically better single-chip RISC than single-chip CISC."

"Regardless of RISC or CISC, with single-chip technology, you're bandwidth limited getting in and out of

a chip to main memory because of cache size limitations," Hester says. "That's why IBM chose multichips. We simply can't put enough devices on one chip today. We have separate chips for instruction and data caches. And separate ICs for the execution units for fixed point, floating point and branching."

Like Intergraph, IBM defined its own interchip logic for its fastest platforms. The highest-performance IBM RS/6000, the 41-MHz Model 550, with 0.5- μ m effective gate length ICs, uses 3.6-V logic.

The big win: chip costs

Multichip proponents point to economics as a big factor. Wafer yields are key. Getting a big chip to yield acceptably, from an economic viewpoint, has always been recognized as difficult. In fact, most semiconduc-

The SPARCs are going to fly.



We put SoftBench on Sun. So you can put your CASE on autopilot.

SoftBench automates all those tedious, repetitive tasks in the software development process. This gives your developers more time to think and speeds up the project life cycle, while reducing errors and rework. And now it runs on



Sun SPARCstations, as well as HP and Apollo workstations.

A tool integration platform, with its own set of tools, SoftBench provides distributed computing services, tool communication, and a common user interface that's easy to learn and use. Add Encapsulator, and you can integrate your favorite CASE tools. Now and in the future. Without even having to change source code.



SoftBench will make your software development process far more efficient, cost-effective and accurate than ever before. It will protect your present and future hardware and software investments, too.

Call **1-800-637-7740, Ext. 2195** for complete product information. And get the best CASE environment under the Sun.



CIRCLE NO. 61

The economics of megachips

Intergraph's Clipper microprocessor uses superscalar dispatch and deep floating-point pipelines. Several moderately sized dice ensure worthwhile production yields and low program risk. In a paper delivered at Compcon recently, Intergraph's Howard Sachs, vice-president and general manager of the Advanced Processor Division, and Harlan McGhan, manager of analysis and application, make a case for multiple-chip microprocessors.

In their presentation, Sachs and McGhan note that a "pure" superpipelined microprocessor, able to operate in CMOS at speeds in excess of 100 MHz, would require an exotic and expensive memory subsystem. The other alternative is to implement large on-chip caches that require large die areas and consequently carry severe economic penalties.

The largest die feasible today typically supports only a relatively small cache (perhaps 8 kbytes or so). This means it's still necessary to construct off-chip secondary cache. The resulting multiple paths to and from memory for multiple load/store pipes become expensive and I/O-pin intensive. Required elaborate decode circuitry also tends to slow down overall processing.

4.5-million-transistor caches

The superfast Clipper microprocessor therefore relies on unpackaged die mounted in multichip modules. Purely on the grounds of cost-effectiveness, say the authors, it makes sense to implement microprocessors as a set of two or more moderately sized chips.

They cite the IBM RS/6000 as an example. It partitions 7 million transistors over nine chips. Of these, 4.5 million are expended just for cache. The accompanying graph illustrates a possible cost-versus-performance trade-off.

Given information about defect density ratios taken from a learning curve

(see graph), it's possible to calculate Y , the effective yield.

$$Y = e^{-AD}$$

where A = area in cm^2 and D = defect density (number of defects/ cm^2).

Applying this formula to the column for 2- cm^2 die, the large area die generates just 70 candidates on a 6-in. wafer versus 146 on a 1- cm^2 die. Assume the first year of production that the defect ratio is the typical maximum for a new process of 1.5 defects/ cm^2 . Then, on average, just 3 of the 70 candidates will be good.

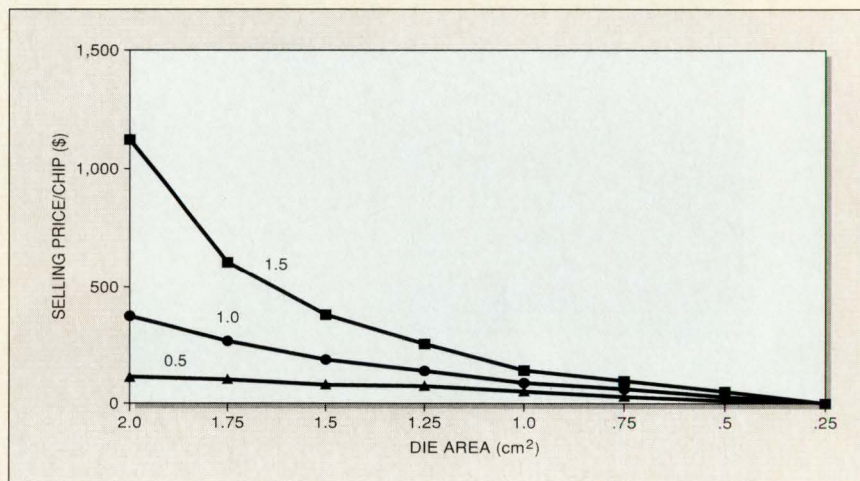
As the defect ratio drops in time, the number of good dice rises accordingly.

good chip is nearly \$1,200. This drops to \$389, and ultimately to \$135.

Assume one of these "super" chips would be used in a system, and 100,000 systems a year would be sold over a period of three years. Total silicon costs would add up to \$169 million.

Compare that with \$42 million for the same period, but using two 1- cm^2 die with exactly the same silicon area. There's a real savings of \$127 million. It's four times as expensive to implement a microprocessor as a single megachip than as two smaller chips.

Of course, this simple "level sales" model can be accused of exaggerating



During the second year of production, at a ratio of 1 defect/ cm^2 , yield triples to 9 good die. During the third year and beyond, when the defect ratio bottoms out at 0.5, yield nearly triples again to around 26 good die.

From this analysis a calculation of the cost of working silicon can be derived. Assume that a 6-in. wafer must bring \$3,500 in revenue (including packaging). In the first year of making 2- cm^2 die, when the defect ratio hovers around 1.5, the actual cost to produce a

the problem. Sales are likely to be smallest during the first year, when the cost differential is greatest, and largest in years three and on, when the differential is lowest. Even so, a substantial difference remains. If 10,000 systems are sold the first year, 50,000 the second, and 100,000 the third, the cost of using a single large die will drop to \$45 million. The cost of a two-die implementation over the same period, however, will be only \$17 million, 2.7 times lower.

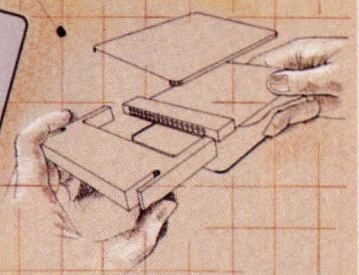
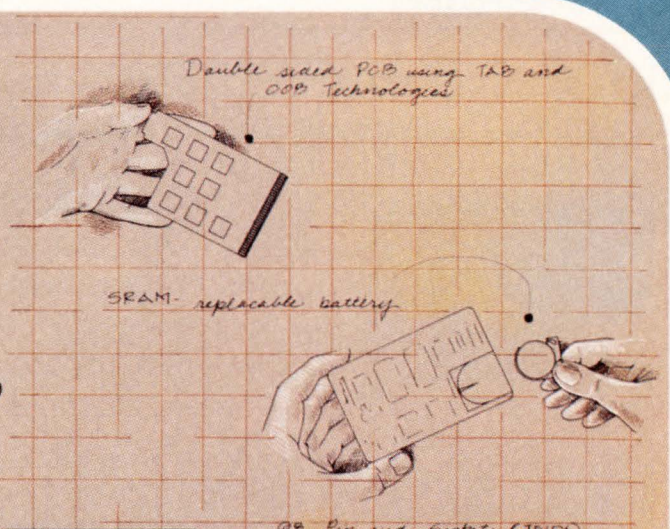
tor vendors, when asked, are reluctant to talk about the subject, and are even more hesitant to provide metrics. "Things like megachips often happen more because they're possible than because they're sensible," says Howard Sachs, vice-president and general manager of Intergraph's Advanced Processor Division.

Intergraph's numbers show that monolithic designs with everything squeezed onto one chip push the practical limits of chip size. "Off-the-shelf processing equipment won't let you deal with chips larger than 2 cm^2 ," says Brookwood. "Mask repair and reticle size limitations pose manufacturing limits. We deal with world-class foundries, but the bigger

the chip, the lower the yield. Regardless of vendor, yield goes down exponentially with area. From an economic standpoint, it makes a lot of sense to use multiple smaller ICs."

Intergraph's analyses point to the use of two small dice instead of one large one with equivalent area (see "The economics of megachips," above).

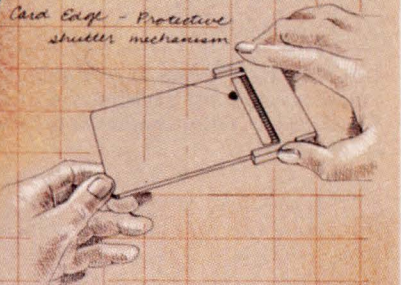
EPSON® IC MEMORY CARDS



JEIDA/PCMCIA

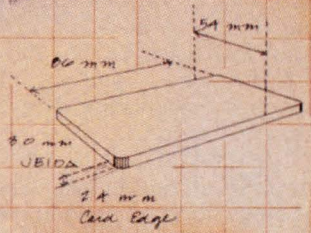
Storage and Software

SRAM	64kB to 2M
OTP EPROM	64kB to 2M
Flash EEPROM	64kB to 1M
Mask ROM	256kB to 8M
EEPROM	16kB to 32kB

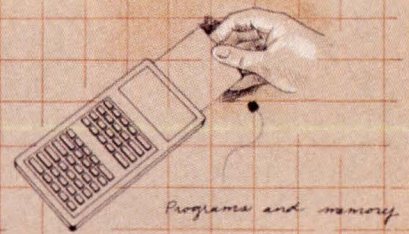
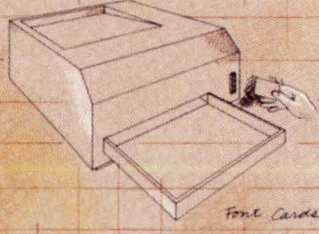
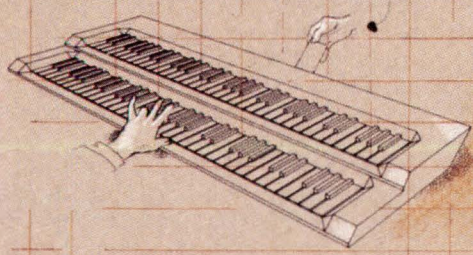


CARD EDGE

SRAM	8kB to 1M
OTP EPROM	32kB to 1M
Flash EEPROM	128kB to 1M
Mask ROM	128kB to 4M
EEPROM	8kB to 32kB



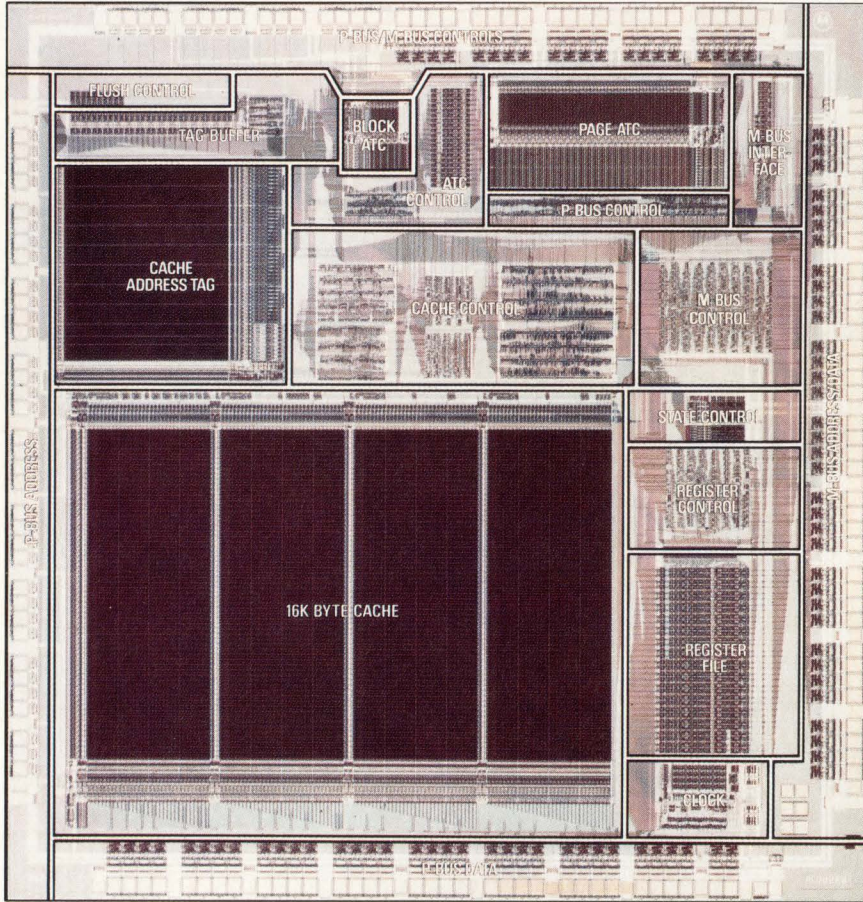
Musical Sound Cards



EPSON EPSON AMERICA, INC.
Component Sales Department • Telephone: 213/787-5300
EPSON Sales Representatives: AL-GA-TN-NC Concord Components 205/772-8883 AZ-NM Fred Board Assoc. 602/994-9388 CA-No. Costar 408/446-9339
CA-Sa. Bagper Electronics 714/957-3357 CO-UT Wn. Region Mktg. 303/428-8088 FL Dyme-A-Mark 305/771-6501 IL-WI LTD Technologies 708/773-2900
IN-KY C. C. Electro 317/921-5000 KS-MO-IA Microtronics 913/262-1444 MA-NH-CT Rosen Assoc. 617/449-4700 MD-VA Tech Sales Assoc. 301/461-7802
MN Electro Mark 612/944-5850 NJ JMR Sales 201/525-8000 NY Elcom Sales 716/385-1400 METRO-NY Niktronix 516/929-4671 OH-MI J.D. Babb Assoc. 216/934-4454 OR-WA Matrex 503/245-8080 PA Omega Sales 215/244-4000 TX-OK Component Tech. 214/783-8831

Call your sales rep today.

FAST PROCESSORS



This photomicrograph of Motorola's existing 88200 RISC cache memory management chip illustrates vast expenditures of silicon real estate consumed by relatively small SRAM caches. Future higher-density devices will obviate the need to go off-chip for larger caches.

"Single-chip designers recognize the need for on-chip cache located near integer units (IUs)," says Brookwood, "but fast cache is tough to design. In a 33-MHz MIPS Computer Systems R3000, you need a 66-MHz cache. If you put it on-chip, how does the floating-point unit act with the cache?"

"Caches and FPUs are very consumptive of real estate. There's no middle ground where you can easily marry an IU and cache and still have a separate FPU. You can do it, but you lose performance." Not all RISC vendors agree. "Fast IEEE FPUs are something that RISCs have over CISC designs," says Martin Booth, senior product marketing engineer for RISC processor products at Fujitsu Microelectronics (San Jose, CA). "It's a function not only of the FPU definition but also of the interface between the IU and the FPU. A lot of design is moving toward integrating both on the same chip die. We do both with about 255,000 transistors."

Still, Brookwood contends that partitioning is better, emphasizing that interchip delays are not a problem at 1991 real-world silicon clock rates. "Our 50-MHz pipelined architecture requires an extra stage in the pipeline, but once the pipeline is filled, prop delay is not significant to throughput," he says.

■ Beyond 50 MHz

Will prop delays be more critical when ICs roll out of fab with transistors toggling at 100 MHz? "They might be," Brookwood says, "but calculations show that a single-chip 100-MHz design would only give a 10 percent better performance spec than a multichip design that would run at 90 MHz because of the interconnects. If you save 35 or 40 percent in cost, the 10 percent performance sacrifice figure isn't that significant. At 50 MHz, there's no trade-off."

But what about merchant market superfast products? It's one thing to be a captive supplier like Inter-

graph, and quite another if your silicon is fueling the vast commercial marketplace.

"We're driven by the need to deliver between a quarter and a half million 68040s in 1991. There's no right or wrong philosophy about partitioning," says Jim Reinhart, manager, M68000 marketing and applications at Motorola (Austin, TX). "It depends on what you're driven by."

Megachip technologies and partitioning are recognized as interrelated at Motorola. "Both factors play a strong role in one's thinking about the future," says Reinhart.

■ Cultural preference

"Motorola has a goal—call it a requirement—for future generations, including the 68040," Reinhart says. "It's to focus on single-chip designs. Everything has to be on one chip, from where you process the simplest integer instructions to where you get your main memory interface."

"Driven by the market, we believe customers must have such devices to help them build cost-effective systems. They must deliver competitive performance without having to resort to large external caches or other things that tend to dramatically increase systems cost and reduce performance by going off-chip. The fastest transistors and buses must be on-chip. Mainstream performance levels must be achieved with low-cost DRAM. Sixteen-way interleaving or large external static caches don't play into this definition."

"Sophisticated memory controllers are key, not just the size of caches. Memory controllers are measured by how well you handle cache hit-and-miss cases, as well as how well a processor handles a very complex set of memory events."

"Although much progress has been made with MCMs, I'd be surprised if you could come anywhere near the volume, cost and quality of what we're doing. MCMs do provide excellent results, but they're really much more suitable for lower-volume applications."

"Testability is also a mixed bag," Reinhart says. "We don't find MCMs more testable than monolithics. In fact, we have military customers who use MCMs; we sell them dice. For them, a big problem is final testing. We can do a much more thorough job when a chip is packaged than at die probe. We can test at a higher frequency. Wafer probes won't let us drive a 68040 die at 25 MHz under

Whatever your destination on the open bus highway ...



Newbridge Microsystems can help you get there.

Newbridge Microsystems offers the industry's most complete and flexible open bus silicon product line.

Leading the way with our 32-bit VME chipset that supplies a full high performance VMEbus interface, we provide a pin-for-pin compatible migration path to VME64. Our product direction extends beyond VME to devices and VHDL models for emerging Futurebus+ protocols.

The CA91C014 and CA91C015 VME chipset provides:

- IEEE 1014/VMEbus Rev C compliance
- Full VMEbus interface implementation
- High performance VMEbus decoupling with on-chip DMA functionality
- Bus Isolation mode for system diagnostics and fault isolation

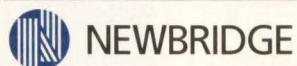
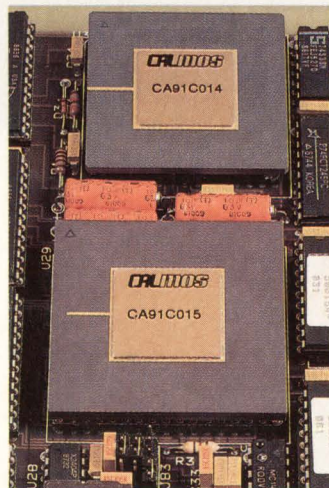
For those applications demanding even higher performance, the CA91C064 VME64 device will offer users of our 32-bit chipset a pin-for-pin compatible upgrade to VME64.

Newbridge Microsystems is also developing a highly flexible solution for entering the Futurebus+ market quickly. The CA91C896 and CA91C897 Futurebus+ chipset will feature:

- Generic local bus and decoupled Futurebus+ interfaces to support split transactions for multiprocessing and burst transfers for higher performance
- Support for scalable external performance enhancements for use across a spectrum of applications
- Portable VHDL models to minimize design effort — and your time to market

Our second generation Futurebus+ products will include processor specific single chip devices, such as the CA91C880 for the Motorola 88K RISC processor family.

Backed by the worldwide Newbridge group of companies and an international sales and distribution network, Newbridge Microsystems is laying out an open bus route to the future.



**NEWBRIDGE
MICROSYSTEMS**

Newbridge Microsystems • A Division of Newbridge Networks Corporation.

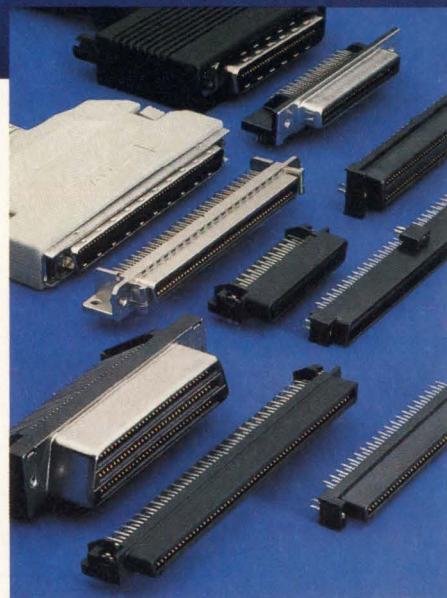
603 March Road, Kanata, Ontario, Canada K2K 2M5

Tel: (613) 592-0714 • 1-800-267-7231 • Fax: (613) 592-1320

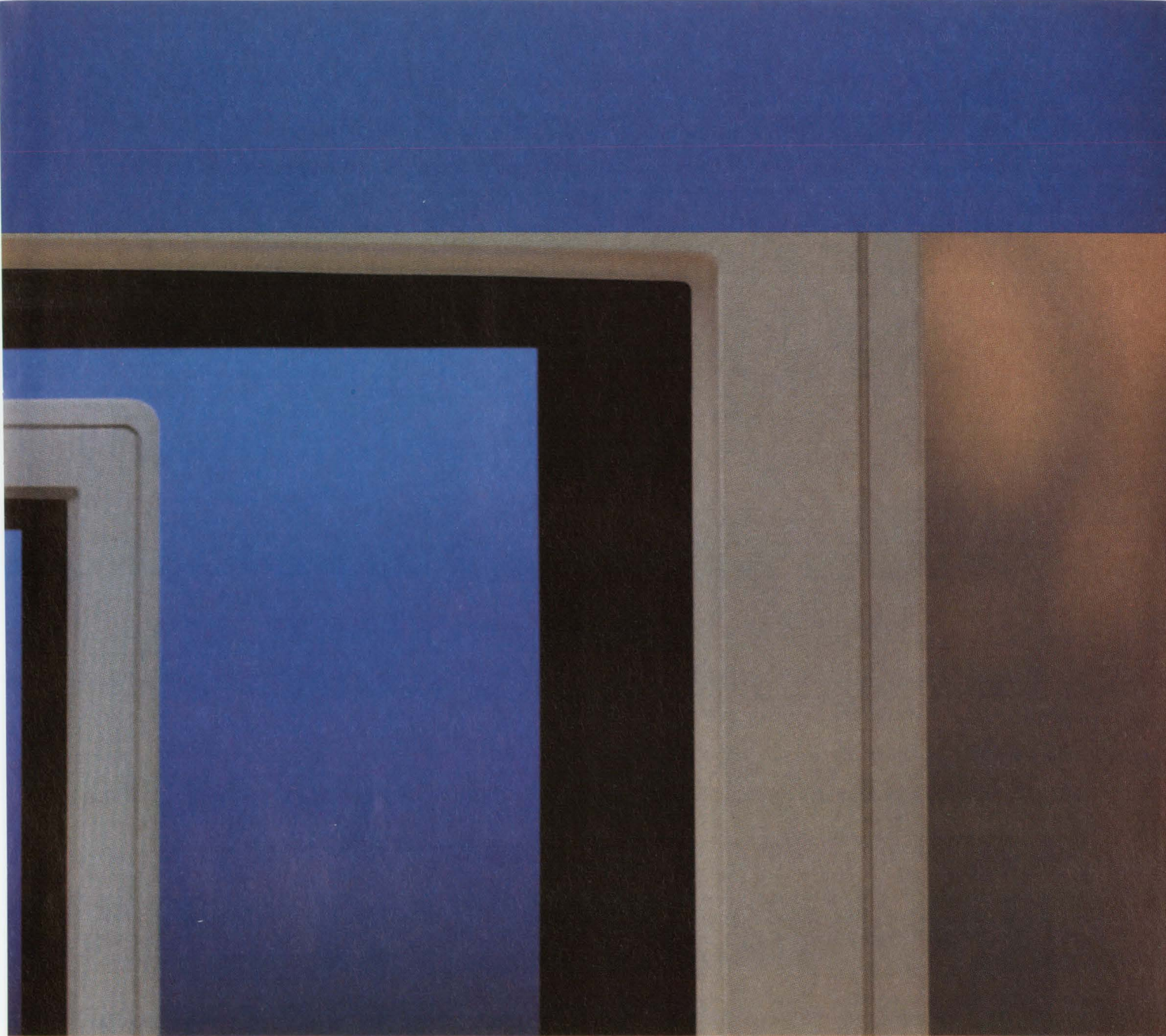
*Keeping reliability up
as form factors go down.*



THIS IS AMP TODAY.



.050 CL, leaf-contact design



In today's tight-corner designs, reliability all too often depends on precise (and costly) manufacturing practices. Our CHAMP .050 connectors weigh in on your side with economic simplicity, and inherently tolerant contacts.

Overview: 0.050" centers, trapezoidal interface, dual-row leaf-contact design. Small, friendly, and forgiving.

Board-to-board: our proprietary compliant-receptacle, fixed-plug contact system tolerates wide mat-

ing depth variations that come with pcb warp—happy news for high-line-count designs—and offers superior performance in assembly, especially in blind-mate applications. Parallel, perpendicular, and in-line styles, 30-200 positions.

Shielded I/O: here, compliant plug and receptacle contacts take full advantage of the controlled header-to-plug interface to meet emerging global intermateability standards. Shielded receptacles and

plugs provide EMI protection. Mass IDC termination and fast braid crimp keep production rates up; AMP tooling covers your volume requirements. 14-100 positions.

The CHAMP .050 high-density line: think of it as a very big factor in small-form design. For details, call our Product Information Center toll-free at 1-800-522-6752 (fax 717-561-6110). In Canada call 416-475-6222. AMP Incorporated, Harrisburg, PA 17105-3608.

AMP
CIRCLE NO. 64

FAST PROCESSORS

thermal and electrical stress. There's too much inductance in probe fixtures."

But, systems flexibility still means multichip designs, some argue. For that reason, Hewlett-Packard (Cupertino, CA) used partitioned silicon rather than monolithic megachips in its Precision Architecture (PA) RISC. Forthcoming PA machines include 90-MHz CMOS five-stage pipelined CPUs that HP engineers anticipate will vie with

puter family from SGS-Thomson (Colorado Springs, CO), for example, has always used partitioning as a route to scalability. Transputer users describe the bounds of a system in software, and then implement it in just enough hardware to do the job.

Newest Inmos H1 chips are highly integrated CMOS VLSI devices. Individual H1 transputers are expected to execute more than 150 Mips peak (60 Mips sustained) and deliver greater than 20-MFlops. H1

ring data at up to 80 Mbits/s. This contributes to a 10 times performance increase over predecessors.

Regardless of demonstrated cost-versus-performance advantages of well-partitioned, smaller-die-size chip sets, single-chip designs are stealing the limelight. First- and second-pass functionality of multimillion-transistor chips, clock rates pushing 50 MHz and beyond, relatively short 3- to 4-year development times, and the concurrent development of optimizing compilers are fueling the monolithic fires.

Complex architectures are now the rule. Some CISC processors are taking on RISC features. And RISC ICs, requiring less silicon real estate to begin with, are integrating previously separate peripherals on-chip.

Memory subsystems

Main memory limitations continue to impose complex cache and memory subsystem designs on users. Unique and varied secondary cache controller schemes are migrating on-chip. The trend is to integrate a first level of cache and resort to sub-25-ns SRAMs off-chip in secondary caches addressed over high-speed memory buses. But bandwidth is recognized as a bottleneck. Wider buses to secondary memory are needed.

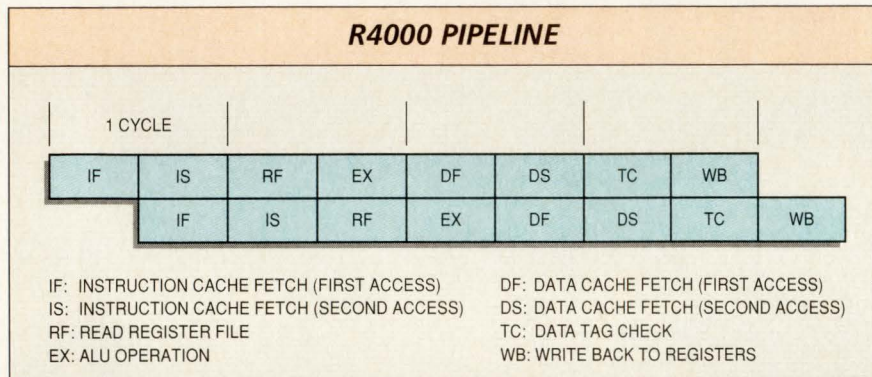
MIPS Computer Systems (Sunnyvale, CA) has a new CMOS R4000 RISC architecture that uses a 64-bit external address bus. The chip handles addressing via a built-in 64-bit virtual address MMU, and includes internal 64-bit registers, buses and multiple execution units.

The R4000 design avoids problems surrounding multiple execution data dependencies. Unlike competitive RISCs such as Motorola's 88000, R4000s don't rely on mainframe-like scoreboarding techniques to keep track of which instructions have been executed. Bypass circuits keep pipelines filled, and the chip's compiler handles the overhead.

Unlike R3000 predecessors that use five-stage pipelines (the latency of individual pipe stages equaled one clock period), 100 native MIPS R4000 chips implement a finer-grained pipeline. They issue two instructions simultaneously (the R3000 issues one).

The R4000 is noteworthy for its 100-MHz internal circuits, with the execution pipeline running 2 times as fast as instruction fetch logic.

R4000 PIPELINE



By implementing a fine-grained pipeline, MIPS Computer Systems' R4000 "super-pipelined" chip issues two instructions simultaneously.

competitive ECL implementations.

PA RISCs compete in both workstation and commercial marketplaces based on adaptability. HP says its approach to superfast processing encompasses unanticipated demands. HP claims performance can be more readily scaled with cost by varying clock speed and cache parameters, which is made easier by partitioning.

Based largely on standard-cell control blocks, library-based data paths and PLAs, HP's fully static design avoids large on-chip caches. Claiming large caches display unacceptably high miss ratios when running the large benchmarks simulating multiuser workloads, PA relies on instruction store buffers that act like small associative caches.

Off-chip propagation delays between PA chips are shortened by low-voltage (3.3 V) drivers and controlled impedance signal buses plus low inductance power and ground lines. Machine cycle times are closely matched to typical SRAM cycle times, with unused cache cycles used to write specially buffered data to off-chip SRAM caches.

Partitioning for transputers

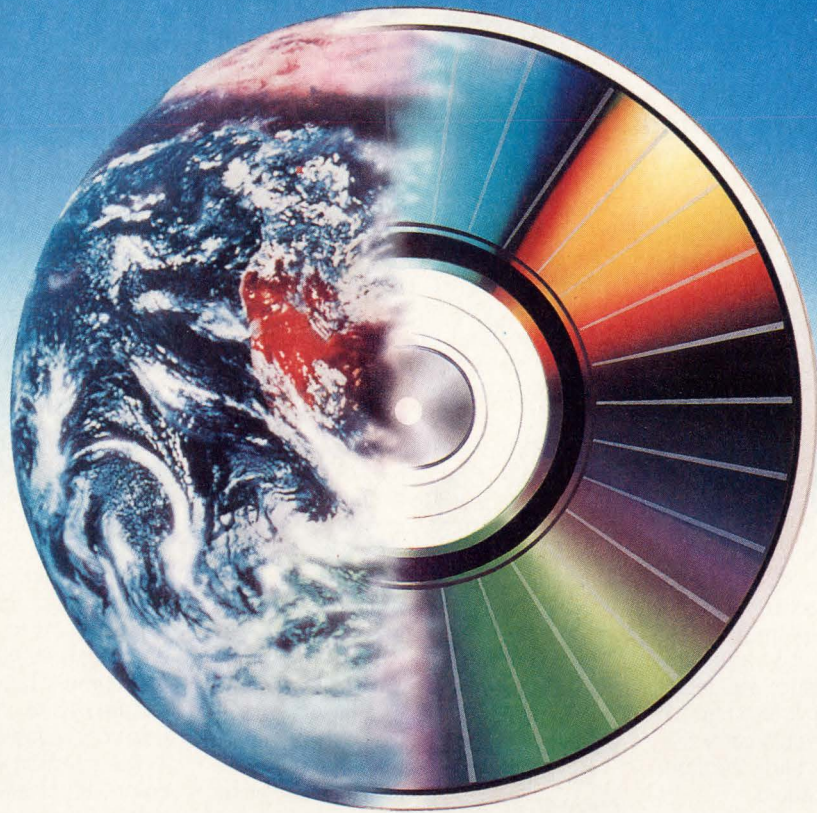
Different vendors use different partitioning approaches to extract benefits from VLSI. The Inmos trans-

puter family from SGS-Thomson (Colorado Springs, CO), for example, has always used partitioning as a route to scalability. Transputer users describe the bounds of a system in software, and then implement it in just enough hardware to do the job.

As pipelined superscalar devices simultaneously dispatching several instructions from cache, H1 transputers pack CPUs, scalar FPUs, 64-bit external data buses, and rather large 16-kbyte on-chip memories, which can be programmed to act as 8 kbytes each of instruction and data cache. Also included are programmable external memory interfaces. The transputer sidesteps external glue logic, supporting board-level designs using up to 16-Mbytes of off-chip DRAM.

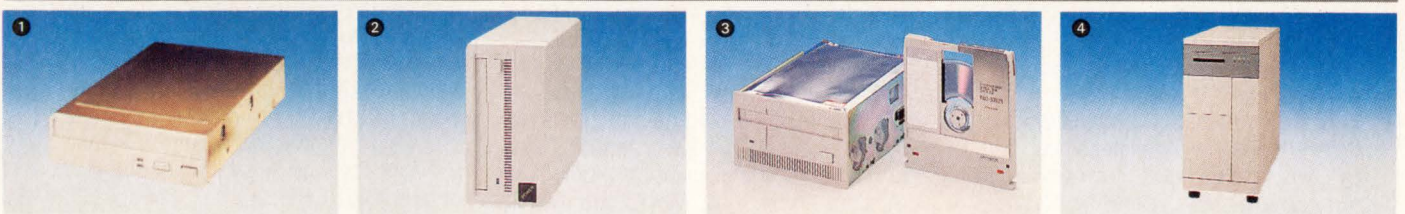
But the real key is the transputer's interprocessor communication scheme, supported by Inmos' Occam language compiler. The ease in which users can create scalable concurrent processing arrays may be the transputer's trump card. Arrays of transputer chips communicate over serial message-passing links.

The latest H1 chips, however, targeted at higher-performance real-time and fault-tolerant concurrent systems, stick with the message-passing approach but with enhancements. The newest H1s have elaborate multiple 4-wire serial interfaces that are capable of transfer-



A World of Choice

When it comes to mass storage needs, your choice is clear: Ricoh optical disc drives. From WORM and rewritable to bare drive and entire library units or subsystems, Ricoh offers a world of choice. Each drive boasts quality you can trust to safeguard vital information. The kind of quality that comes from over 50 years of know-how in optics and image processing, in such products as cameras, copiers, facsimiles, telepress, laserprinters and scanners. Now you know why Ricoh is the world's leading supplier of 5-1/4" optical disc drives. For more information, call 1 (800) 955-FILE.



- 1 RH5500/5-1/4" REMOVABLE CARTRIDGE HARD DISK DRIVE
- 2 RS-9100H/5-1/4" HALF-HEIGHT WORM SUBSYSTEM
- 3 RO-5030EII/REWRITABLE OPTICAL DISK DRIVE
- 4 RJ-5330E/MAGNETO-OPTICAL DISK LIBRARY UNIT

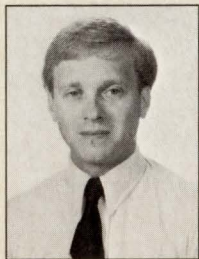
**BEST FOR QUALITY.
UNMATCHED FOR SERVICE.**

RICOH

RICOH CORPORATION (File Products Division) 5150 El Camino Real, M/S D-20, Los Altos, Ca 94022 U.S.A Phone: 415-962-0443 Fax: 415-962-0441
RICOH CORPORATION (Eastern Region Office) 59 Stiles Road, Suite 102, Salem, NH 03079 Phone: 603-893-0547 Fax: 603-893-4162

CIRCLE NO. 65

Design decisions and technology that were keys to success of RISC System/6000



From the outset of the America project in 1985, we knew we needed to achieve significant advances over previous RISC architectures and the earlier IBM RT PC, IBM's first RISC-based Unix workstation. In 1986, we defined a second-generation RISC architecture that would come to be known as the Performance Optimization With Enhanced RISC (Power) architecture. Of primary concern was that the Power architecture and chip set needed to offer both scientific and commercial users the lowest price and highest performance possible. It also had to be extensible, so that it would carry the RISC System/6000 product line through several technology generations.

Building upon earlier work by John Cocke at IBM's Yorktown Heights Research facility (Yorktown Heights, NY), we determined that an architecture that permitted overlap of each basic function—branch processing, integer instruction execution and floating-point execution—would best meet this goal and achieve equivalent integer and floating-point performance.

We believed it was necessary for the Power architecture to provide instruction-level parallelism that could execute up to 5 instructions/cycle: one branch instruction, one fixed-point instruction, one condition register instruction, and one floating-point multiply-add instruction, which would be counted as two floating-point instructions.

Behind every architecture lies a series of decisions that build one upon the other; the Power architecture was no different. For me, four decisions, plus the software technology embodied in our compilers and operating systems, stand out in particular.

Starting from scratch

The RT PC had been introduced only months before we set out to define the Power architecture and chip set. Thus, the first decision we faced was whether to build upon the RT's architecture or to start from scratch. At first, we thought it might be possible to graft a superscalar architecture and other key design concepts onto the existing RT architec-

ture, but we soon realized that would be extremely difficult. For one thing, the RT architecture wouldn't allow the exploitation of instruction-level parallelism we wanted to achieve in the Power chip set, and without that, we couldn't achieve our performance goals.

Even if we could extend the RT architecture to support superscalar implementations, we were certain it wouldn't scale much beyond that. A key design criterion for the Power chip set was that it would be extensible through several successive technology generations. We wanted the chip set to process at least 4 instructions/cycle in its first generation.

We worked closely with our compiler teams to generate code that could exploit the architecture to its fullest.



The RT had other limitations as well. It had only 16 general-purpose registers, for instance, while our design called for 32. We found that, with 16 registers, we kept running out of fixed-point registers, particularly in floating-point codes. This would severely limit our floating-point performance.

We had determined that the Power microprocessor unit would have three separate processors—branch, fixed and floating-point. In the RT architecture, the fixed-point and the branch processors were the same. Separating these two processors would be difficult.

Finally, the RT processor required a co-processor interface to floating-point extensions. In the end, we realized the RT architecture simply had too many limitations to meet our design goals. Of course, we were keenly aware that customers had already made significant investments in RTs, and that independent software vendors (ISVs) were porting their applications to the RT. At first, we thought that any new RISC CPU design should incorporate binary compatibility with the existing RT, to help preserve customer and ISV investments.

Maintaining binary compatibility, how-

ever, carried substantial performance penalties. Since this was to be an optimized architecture, we knew we had to avoid that. In the Unix market, source code compatibility was the norm and would give us an important performance advantage. So we opted for that.

Selecting a floating point

From the beginning, the Power architecture was designed to deliver the best price/performance possible for both commercial and scientific applications. Therefore, we sought to optimize the Power architecture for both integer and floating-point operations, respectively. Our goal was to execute floating-point operations at the same speed as integer operations. That meant the Power architecture had to complete one floating-point operation every clock cycle.

The question was, which floating point—370 hexadecimal or IEEE floating point? Standards drive the Unix market, and the IEEE floating point ranks as such a standard, especially among many mathematicians and scientific users. IEEE floating point was standard on the RT, for instance.

There was significant debate about whether we would give up too much performance implementing the IEEE standard. After drawing heavily on research at IBM's Yorktown laboratory, we were able to select an IEEE-compatible floating-point implementation with no significant performance penalties.

Partitioning chips

The next decision we faced was how best to partition the chip. We had three priorities: to optimize performance, to create a scalable architecture that would expand for low-end and high-end products, and to provide an implementation that would require minimal changes through several technology generations.

In the end, we determined that six unique chip designs would offer the best chance for successful scaling and a long life for the implementation. Those six include a branch processor, fixed-point processor, floating-point processor, MMU, the Micro Channel Architecture bus interface unit, and a data cache unit, implemented in combinations of two or four chips.

We also decided that the initial design point of the Power chip set would

Randy Groves, MSEE, senior engineer/manager of Advanced Products Development, Advanced Workstations Division, IBM

perform at 25 MHz. That would give us an excellent lead in integer and floating-point performance for the first RISC System/6000 products, yet also let us devise faster clock cycles in successive generations. In fact, at the initial announcement we introduced a 30-MHz system as well as two 20-MHz systems. We also knew that chip-to-chip crossings wouldn't drag down performance beyond 25 MHz, and that the memory interface could scale for additional low- and high-end systems.

With these two criteria defined, we designed the six chips, then optimized the chip-to-chip interconnects. In this way, we would be able to increase the clock frequencies without having to rework the entire chip set.

The proof of the success of our efforts was the announcement of RISC System/6000 Model 550 Powerstation/Powerserver in October 1990. The 550 implements a 41-MHz design of the Power CPU in IBM's latest CMOS technology.

■ Verification tools

The scope of the Power chip set, with six unique chip designs, was considerably more complex than the three-chip RT design. We realized early on that traditional design verification and simulation tools—such as those used for the RT processor—would be inadequate for the task.

Moreover, time-to-market was crucial. We had to find a way to verify the new design as quickly as possible. Using tools such as those for the RT would have taken longer.

We turned to IBM's mainframe designers for software simulation tools. Those tools let us run automated simulations overnight and randomly generate complex instruction sequences. With many of our traditional tools, we would have had to generate simulation codes manually, which would have limited the code our verification team could test.

IBM's compiler and operating system technology played a crucial role in the success of the RISC System/6000. We couldn't have achieved our ambitious performance goals for the Power architecture without the close cooperation of IBM's compiler technology laboratory in Toronto, Ontario.

When we built the Power chip set, we implemented one of the first—if not

the first—true superscalar RISC architectures. But the hardware's ability to process multiple instructions in parallel would have been useless without compiler technology to exploit that. We worked closely with our compiler teams to generate code that could exploit the architecture to its fullest. They, in turn, provided us with insight into how we could best implement architectural elements to improve compiler performance even further.

In addition, earlier work on operating system technologies proved invaluable to providing the high reliability users achieve in the RISC System/6000 family's AIX operating system—IBM's implementation of Unix. IBM's 801 project had developed its own operating system, called Control Program-Research (CPR). But, early in RT development process, the design team realized Unix had become a standard, especially for technical computing.

Therefore, it was decided that AIX would be the operating system for the RT and successive RISC-based products such as the RISC System/6000. Still, key technologies of CPR could be stitched into the AIX kernel on the RT and, later, the RISC System/6000. CPR technology improved AIX's file system reliability and provided preemptable kernel routines, program management, dynamic binding, and other features. All of this remains transparent to the user, who sees a standard Unix interface on a system that is inherently more reliable.

■ Foundation for the future

The Power architecture of today provides a solid and extensible foundation for future technology generations.

At the low-end, the original architecture will let us use fewer chips, which, in turn, will lower the cost of entry while maintaining performance. At the high-end, the Powerstation/Powerserver 550 is only the beginning. We plan to offer increased performance in a number of ways: through faster clock rates, by exploring clustering and multiprocessor (MP) technologies, and by exploiting fiberoptic link technology.

We also plan to extend the original superscalar concepts on which the Power architecture was based. Future iterations of the Power chip set will process even more instructions in a single clock cycle.

Using 64-bit data paths to cache and main memory as well as a 64-bit floating-point ALU, these very dense chips rely on a superpipelined architecture and this double-speed internal clocking to provide performance gains. MIPS' approach includes hefty on-chip instruction and data caches (8-kbytes each) for its multiple execution units.

VLSI R4000s include FPUs, IUs and control logic for cache-coherent systems, as well as optional secondary cache interfaces. The design is compatible with 32-bit forerunners and peripheral products and lets designers "tune" off-chip I/O for optimal cost/performance trade-offs using special selection circuits.

While MIPS indicates that lab version R4000 chips have been tested at 50 MHz, other vendors are announcing processors running even faster (although none so far sport 64-bit-wide address buses).

One high-speed single-chip design played center stage at this year's ISSCC conference. Intel (Folsom, CA) reported development of a 0.8-mm, triple-metal CMOS implementation of the 80486 operating at 100 MHz.

Such a 486, if commercialized and properly supported with superfast packaging, peripherals and memory devices, would certainly boost the performance of applications software in the world's largest installed applications software base—MS-DOS.

Intel's racer, having seen silicon, integrates 1.2 million transistors in a fabrication process optimized for on-chip phase-locked loop timing circuits that slash setup, hold and output valid times. Intel says its vehicle is based on markedly reduced wire lengths, planar dielectrics, salicided gates and source drains, and tungsten-filled vias and contacts. These are factors that will play important roles in Intel's much-closer-to-market 50-MHz 486.

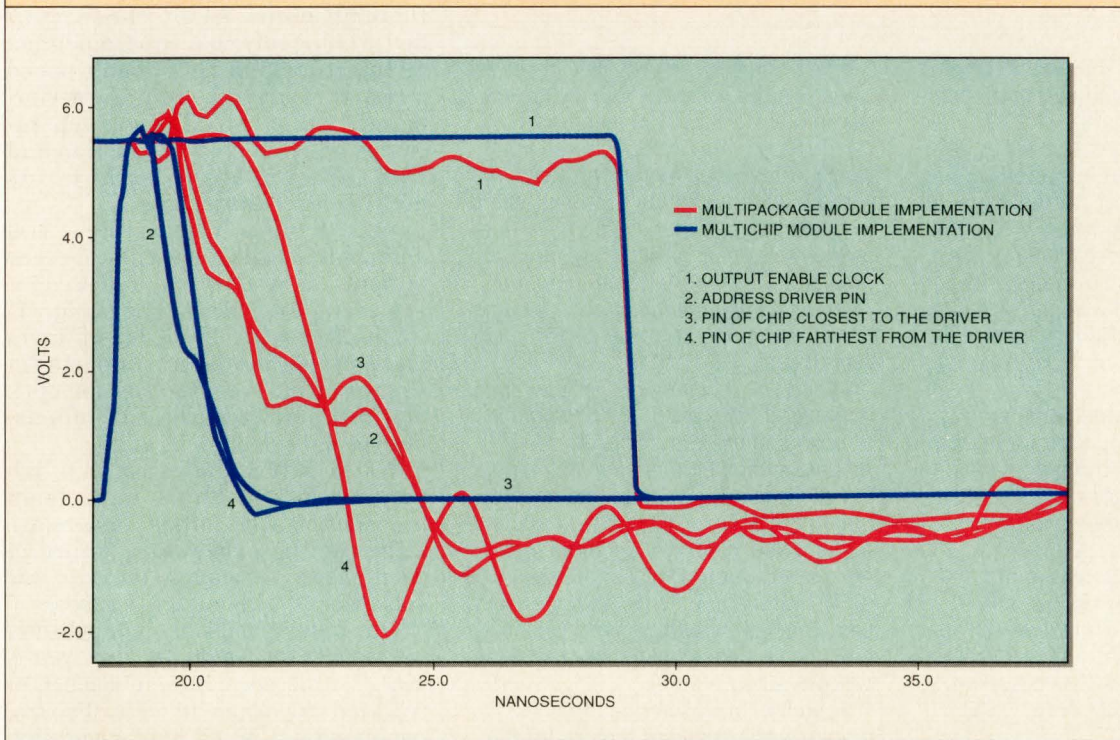
■ Embedded applications abound

"The newest technology and the fastest processors tend to debut in computer systems and workstations," says Fujitsu's Booth, "but, their impact in the embedded controller arena is equally significant."

The 1-million transistor superscalar core from National Semiconductor (Santa Clara, CA) is a case in point. Tailored for on-chip digital signal processing, National's high-throughput chip is aimed squarely at embedded applications.

Code-named "Swordfish," Nation-

486 I/O PERFORMANCE AT 100 MHz



Simulation results based on Intel's 100-MHz 486 processor illustrate how multipackage modules (MPMs) and multichip modules (MCMs) perform as devices get faster. A typical MPM might include a processor and an SRAM cache. An MCM would also include control circuitry, possibly mounted on a silicon substrate. The curves depict performance for pins both close and far from on-chip driver stages.

al's 100-Mips Type 32SF640 engine includes not one but two independent integer units, each with a four-stage pipeline. The dual execution units effectively execute two instructions per clock cycle.

But the parallelism doesn't stop there. Parallel execution of integer and DSP functions is handled by separate on-chip hardware. Execution of multiply/addition routines for DSP algorithms and floating-point calculations overlap with integer processing. On-chip instruction and data caches feed all four processing sub-blocks (any two of which can be simultaneously active).

Although National's latest creation includes a system interface at the data bus that is 64 bits wide, it uses a conventional 32-bit address bus. It's limited, therefore, to addressing a 4-Gbyte uniform address space. The Swordfish's data bus also dynamically supports 8-, 16- and 32-bit peripheral ICs. To minimize embedded cost, National expects Swordfish users will choose an optional clocking scheme that lets an external system bus operate at half the frequency of the chip's internal clock. The Swordfish design will read/write to relatively slow DRAMs and EPROMs—devices that are relatively inexpensive and readily available. Pipelined and wide-band-

width interleaved memory are also supported.

As impressive as the CMOS Swordfish is, its primary caches are still relatively small. This is suitable, however, because a lot of embedded code—especially time-critical inner-looping routines—execute over and over and are generally less than 400 bytes. A 1-kbyte two-way set-associative data cache and a 4-kbyte decoded instruction cache is provided on-chip. Both are equipped with a locking mechanism to prevent replacement of data deemed performance-critical (National also uses bus snooping logic to ensure coherency between data cache and main memory).

National's preliminary data sheets discuss three versions of the Swordfish, running at either 33 MHz, 20 and 40 MHz, or 25 and 50 MHz. These clock speeds, when combined with the device's superscalar architecture, result in one very fast controller. If it proves economically reproducible, it should find wide favor in commercial embedded graphics applications. A lot of sockets are waiting for 100-Mips processing in scanners, laser printers and fax machines, among others.

Raw clock speed, plus the ability to put more elaborate structures in silicon, drives the embedded control-

ler effort at Advanced Micro Devices (Sunnyvale, CA) too. The company's new 29050 RISC embedded controller now packs 428,000 transistors—nearly a quarter million more than the widely used 29000 predecessors.

The small feature size CMOS 29050 clocks as high as 40 MHz. At this rate, a 29050, which includes an on-chip pipelined IEEE floating-point processor, can perform 34 sustained MFlops, peaking at 40 integer Mips and 80 MFlops (based on 4x4 and 1x4 graphics transforms).

Low- vs. high-density MOS

CMOS processes such as those of the 100-MHz Intel 486, National's Swordfish and AMD's 29050 dominate superfast single-chip news. CMOS density enables things such as multiple execution units and cache. But BiCMOS and bipolar ECL are gaining favor for high-speed, low-density logic used in superpipelined RISC approaches. BiCMOS and ECL designs offer better control over clock skewing in high-speed circuits, both partitioned and single-chip designs.

As for ECL, some experts predict a move away from the power-hungry logic, regardless of its obvious speed advantages. Motorola, for one, has dropped its plans to collaborate with Data General on a 100-Mips ECL

We're giving away our management secrets.



More project managers are turning to Microsoft® Project for Windows™, the number one management package*.

Probably because Microsoft Project for Windows wouldn't be any different if you'd planned it yourself.

Work with data easily. Create customized filters, tables, even output.

Manipulate PERT and Gantt charts by clicking and dragging.

See for yourself. Just give us a call at (800) 541-1261, Dept. P95, and we'll send you a free working model.

Microsoft®
Making it all make sense™

*Project for Windows has been given top honors in PC World, InfoWorld, Software Digest and PC Magazine. Offer good until June 30, 1991 or while supplies last. The first working model is free, not including shipping and handling; additional models are \$9.95 plus applicable sales tax and shipping and handling. Offer good only in the 50 United States. In the U.S., call (800) 541-1261, Dept. P95. For information only: In Canada, call (416) 568-3503; outside the U.S. and Canada, call (206) 936-8661. © 1991 Microsoft Corporation. All rights reserved. Microsoft and the Microsoft logo are registered trademarks and Windows and Making it all make sense are trademarks of Microsoft Corporation.

How high-end embedded processors are changing



The embedded processor market is changing. The traditional constraints of high performance and low system cost are no longer the only considerations. Designers of

fax machines, laser beam printers, speech compression equipment, and image compression equipment are now demanding that embedded processors be customized for specific low-cost applications. This customization reduces the user's time-to-market and results in a better cost/performance ratio.

While customization is receiving a new level of emphasis, the user's need for performance is continuing to grow. It's no longer sufficient for a processor to excel in a few specific benchmarks. A typical multifunction imaging application, such as a combination laser printer/fax machine, requires digital signal processing for the modem function, fast handling of floating-point operations for the Postscript interpreter, and integer arithmetic for image compression and system control. And the bus interface of such a processor must operate with low-cost memory arrays yet still deliver high performance. External caches are too expensive, so an innovative design approach is needed to achieve high system performance with DRAM arrays.

The design goals for the embedded processor core now called Swordfish were driven by these demands. The design's dual pipelines, high-performance floating-point unit and DSP capabilities formed the basis of the architecture. The addition of on-chip instruction and data caches and the design of the processor's bus interface were key to the ability to provide high levels of system performance with low-cost memory arrays. And on-chip peripherals were added to reduce the system board size.

An embedded architecture

We knew that by early 1991 we could produce a device that would have more than 1 million transistors and operate reliably at 50 MHz. The problem was where to allocate the transistors. We had to choose among larger caches, more execution pipelines, improved FPU

performance, and a faster multiplier. We also faced the challenge of building a RISC processor while still maintaining compatibility with other members of National's Series 32000 embedded processor family.

We could have chosen to define a more complex logic for issuing instructions, using out-of-order execution. Instead, because an optimizing compiler can reorder the code and yield about the same performance, we decided to allocate the transistors to modules that would have a greater impact on the total performance. The logic for issuing instructions, together with the instruction cache and the instruction loader, are key contributors to performance, so the greatest effort was concentrated on optimizing this path.

More high-end processors will include on-chip system modules, reducing the costs of systems.



for two interleaved memory banks by providing two sets of control signals. Furthermore, the unit can be programmed to operate at half the internal execution frequency. As a result, execution is fast, even with slow memory arrays.

Finally, we put a lot of effort into on-chip debug features. The most important feature is support of in-system emulation (ISE), with a special serial link from ISE equipment to the Swordfish processor.

Interdisciplinary cooperation

The design process of a complex processor requires the expertise and cooperation of many disciplines. The Swordfish design team comprised architects, chip designers, compiler experts, system designers, and a logic verification group, working together to define the architecture specification of Swordfish.

During initial definition of the processor's architecture, we focused our attention primarily on the number of execution pipelines, the cache structure and the system interface. The architecture group built a performance simulator,

and the compiler experts built a prototype compiler. Together both groups simulated different pipeline models with different instruction sets. At the same time, chip designers evaluated the feasibility of implementing the different models. By defining the compiler at the same time as the architecture, we were able to choose whether a function would be implemented in hardware or in the compiler. Next, we defined the caches and the system interface.

The bus was defined primarily by system designers. At this stage, we considered supporting half-frequency bus operation and interleaved memory configurations. We also integrated a system interface module into our performance simulator, enabling simulations of off-chip caches, DRAM arrays with in-page support and other memory configurations.

The result of this design effort was a RISC CPU core optimized for compute-intensive embedded applications. Its dual integer units, each with a four-stage pipeline, and its on-chip FPU with an array multiplier, and caches for instructions and data, allow a high degree of parallel execution of instructions. Combined with clock rates up to 50 MHz, the architecture provides execution speeds up to 100 Mips. This super-scalar RISC processor core is the first in a new generation of high-performance processors that will form the computational heart of embedded processors customized for specific applications.

The changes in the embedded processor market will continue to drive integration. More high-end processors will include on-chip system modules, reducing the costs of systems by providing greater functional integration. The common goal of embedded processor designers and users is ultimately to have a single-chip solution for a given application, requiring that a specific CPU core be integrated with a different set of on-chip modules for each application.

The main obstacle to high performance in the embedded control market is limited memory speed. Future processors will solve this problem using larger caches and wider buses. They will also provide on-chip support for interleaved DRAM arrays to narrow the gap between processor speed and memory speed.

Gideon Intrater, MSEE, chief Swordfish architect, engineering manager, National Semiconductor design center

16 lines, No waiting.

Your application is first in line with the MVC 16-line Async Commux. It's got processing capacity to spare, thanks to a 16 MIPS RISC, so system power goes to your users — not I/O.

Character processing and buffering is managed on-board by our RISC, so driver calls and host overhead are kept to a minimum. All 16 lines can operate at 38.4 KBaud. That's over 61,000 characters per second throughput, double the rate of other VMEbus async controllers.

The MVC's advanced features benefit both the integrator and programmer. Port and VMEbus parameters are soft-configured and set line-by-line. Modem control is standard. Full software support is also included,

along with diagnostics and a Streams driver.

Advanced memory architecture and high-speed buffering eliminate overruns and port domination. Memory is expandable from 128KB to 1MB, so the MVC handles today's requirements and future application needs.

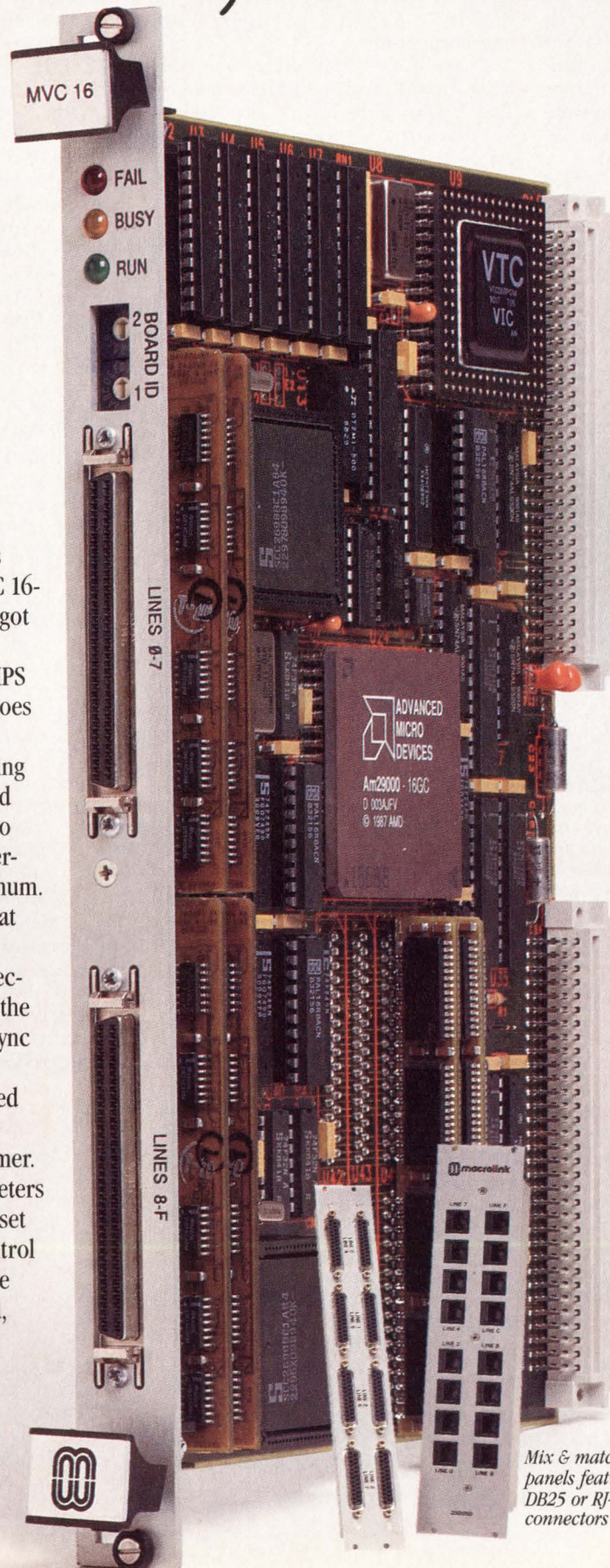
With over 11 years experience producing advanced storage, communications and memory products, Macrolink delivers the powerful and flexible MVC in 8 and 16 line configurations. Call us today. We won't keep you waiting.

Macrolink Inc.,
1500 North Kellogg Drive,
Anaheim, California 92807.
Phone (714) 777-8800,
FAX (714) 777-8807.

 macrolink® inc.

CIRCLE NO. 66

Mix & match I/O panels feature DB25 or RJ-45 connectors



FAST PROCESSORS

88000 spin-off. But not everyone agrees ECL's days are numbered.

MIPS Computer Systems' new systems-level server products, for example, built in conjunction with Prime Computer and Control Data Corp, are based on ECL microengines. NEC, MIPS' foundry partner, is expected to start shipping volume production quantities of MIPS' three-chip ECL RISC chip set.

And, it's only been a short while since Bipolar Integrated Technology (Beaverton, OR) introduced an ECL FPU chip—the IEEE-compatible B3130.

"There are no fundamental manufacturing limitations facing ECL makers," says Jim Peterson, vice-president of engineering at Bipolar Integrated Technology (BIT). "And, the inclusion of CMOS memory into ECL processes may actually accelerate ECL density and performance curves. Moreover, ECL processes are able to deliver the required clock frequencies to support superpipelining."

Significantly, BIT's bipolar process competes with CMOS for density. It trims power dissipation from bipolar's typical 2 or 3 mW/gate to a few hundred mW/gate.

For now, the highly pipelined B3130 device is set to provide sustained performance at 200 MFlops. Sporting a 64-bit I/O bus, the B3130 incurs only 20-ns latency for ALU and multiply operations, resulting in 100 MFlops for random scalar operations and up to 100-Mips scalar performance. The chip concurrently executes ALU, multiplier and divide/square root operations.

BIT is already enjoying design wins for the B3130 and acceptance of the company's bipolar technology. HP/Apollo has signed up to use the new chip, FPS Computing's supercomputer is using BIT's ECL-based Sparc RISC, and BIT has been selected by MIPS Computer Systems as the foundry for MIPS' fastest R6000 32-bit processor in its RC6280 RISCComputer server.

BiCMOS gains favor

BiCMOS is gaining momentum too. Motorola is discussing its next-generation 88000 RISC product, the sym-

metric superscalar 88110. The chip is fabbed in triple-level metal 0.8- μ m CMOS, but Motorola seems likely to use BiCMOS in a post-88110 family of highly parallel superscalar microprocessors.

These ICs will probably have very wide buses and 100-MHz speeds. The BiCMOS 88110 is intended to be object-code compatible with the original 88000, but it will feature multiple independent pipelined execution units.



"There are no fundamental manufacturing limitations facing ECL makers," says Jim Peterson, vice-president of engineering at Bipolar Integrated Technology. "And, the inclusion of CMOS memory into ECL processes may actually accelerate ECL density and performance curves."

ECL 88110s will likely have on-chip FPU, special graphics units for 3-D number crunching, demand paged MMUs and on-chip caches. Motorola says these RISCs will have less than 1.5 million transistors.

What do IC giants such as Motorola and Intel see in the future for fab technologies where 1.5 million device chips are considered sleek? In recent statements to the industry, Motorola discussed its dual-pronged BiCMOS RISC and CMOS CISC strategy. The company identified process technologies to achieve 4 times performance improvements on each generation of 88000 RISC throughout the decade.

Motorola predicts improvements in transistor density and speed thanks to BiCMOS. The company predicts over 100 million devices on a chip, clocking at over 300 MHz. Single-chip microprocessors will de-

liver 4 billion instructions/s performance by the year 2000, Motorola engineers forecast.

Intel also plans for 50- to 100-million transistor CPUs. Its Micro 2000 architecture includes ICs capable of 2 billion instructions/s, maintaining binary compatibility with the 386 family and MS-DOS/OS-2/Unix architectures.

Of course, such efforts will be incredibly costly. As performance competition heats up in CISC and RISC camps, processor makers must adopt new and increasingly expensive fabrication and test systems. Intel recently announced a \$1 billion spending plan for an 8-in. wafer fab this year.

Pushing the limits?

With industry leaders such as Intergraph, SGS-Thomson and others capitalizing on small-die multichip systems and advanced packaging, one wonders whether megachips represent a viable course for future generations. Some industry analysts say no. They contend today's fab technologies are rapidly approaching practical limits to feature size reduction. Conventional steppers and wet and even dry plasma etching cannot meet the submicron challenge necessary to make ICs such as BIT's and National Semiconductor's feasible in the marketplace, they say. Particle control

and clean-up techniques may not be adequate either. Moreover, many systems designers suspect on- and off-chip packaging and interconnect constraints will put a damper on further reductions in feature sizes, too.

Others disagree. "We've just opened a fab line with sub-0.5 μ m optical technology," says Bob Rowe, RISC marketing manager at Integrated Device Technology (Santa Clara, CA). That company builds products based on MIPS Computer Systems' RISC instruction set and architecture. "Remember, only a few years ago folks said the limit for CMOS was 1 μ m, but that proved not to be the case."

Rowe says there's no reason why the trend shouldn't continue. "Submicron fab makes 30-MHz clock speeds routinely possible. Look at



GO

START OVER
Imported board
has no tech support

GO BACK 1 SPACE
Discount board
has compatibility
problems



Cheap boards
forces Bankruptcy

NOBODY WILL VISIT YOU HERE



START
HERE

Are you playing board games?

GO BACK 3 SPACES

Cheap board fails in
UNIX system

Imported board
proves unreliable

GO BACK 1 SPACE

Choosing a board is serious business. The quality of the motherboard will determine the performance and reliability of your machine, and the success of your company.

ISA SOLUTIONS

If EISA is not required, the AMI 486 ISA boards are the answer. Operating at 33 MHz and possessing the fastest video speeds in the industry, they provide the perfect platform for graphic intensive applications.

FINISH AHEAD OF THE GAME

Select dependable AMI
Motherboards

Use AMI for
reliable network
file server

MOVE AHEAD 2 SPACES

That is why more OEMs and Integrators are using American Megatrends, Inc. for their motherboard needs. Already the industry leader in 386 and 486 BIOS, AMI has now established the standard for EISA and ISA boards.

THE AMI DIFFERENCE

Unlike any other motherboard, AMI boards provide total BIOS compatibility; this ensures the highest levels of performance and reliability.

Call today and see how the team at AMI will put you ahead of the game.

LOSE TURN

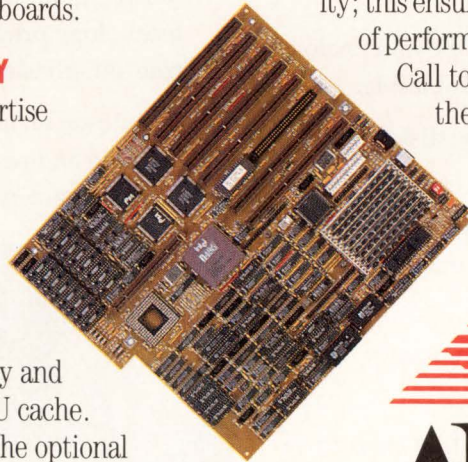
Imports ship late

Cheap board
ruins reputation

GO BACK 3 SPACES

EISA TECHNOLOGY

AMI has the expertise to provide you with premium 486 EISA boards. These 33 MHz systems can support up to 96 meg of memory and up to 256K of CPU cache. Used along with the optional SCSI Host Adapter, it creates a terrific high performance network server or UNIX hub.

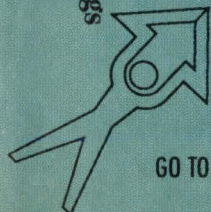


SINGLE SOURCE TECHNOLOGY

AMERICAN MEGATRENDS, INC.
800-U-BUY-AMI or 800-828-9264, 404-263-8181, fax 404-263-9381

CIRCLE NO. 67

Discount
boards not
worth the savings



GO TO BANKRUPTCY

Discount boards have
high failure rate

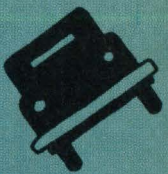
GO BACK 3 SPACES

Discount board has
slow video speed

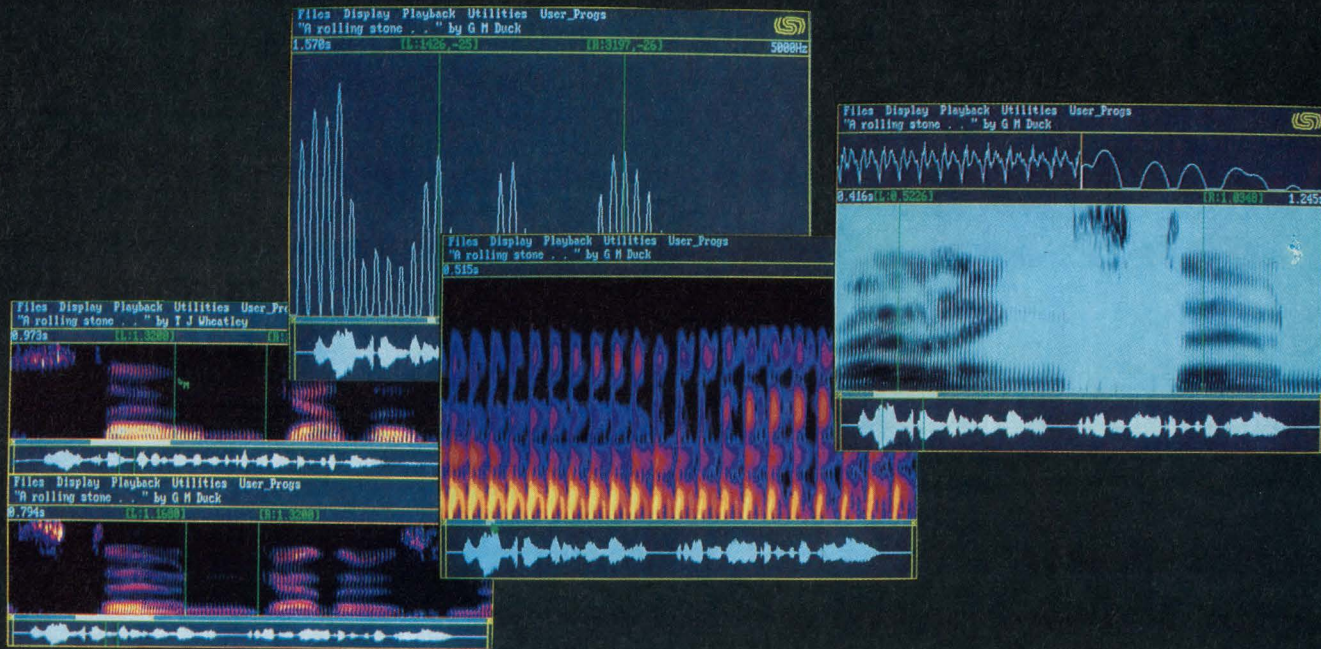
LOSE TURN

Use highly compatible
AMI motherboards

PROFITABLE PARKING



No sooner said than done...



LSI Speech Workstation Spectrograms in seconds—Performance second to none

- Sold and proven in Europe, now available in the US and Canada.
- Package includes sophisticated DSP and analog plug-in cards for a fast PC AT compatible.
- Twin analog input channels allow disk capture from microphone or line input.
- Display types include spectrograms, time waveforms, spectral slices, energy and pitch contours.
- Split-screen mode allows time/frequency comparisons of two signals.
- Add your own custom functions that execute on the PC or on the DSP board.
- Signal editing includes cut, copy and paste facilities.
- Two 16 bit A/D converters allow simultaneous sampling up to 100 kHz. Latest Sigma Delta technology provides 64 times oversampling and true anti-aliasing.
- Pull-down menus and mouse operations for quick learning and easy use. Moveable markers allow precise quantitative analysis.



Loughborough Sound Images Ltd
The Technology Centre
Epinal Way Loughborough
Leics LE11 0QE England
Tel: (0509) 231843
Fax: (0509) 262433

- **USA** – **Spectrum Signal Processing Inc**
Tel: 800 323 1842 (East US)
Tel: 800 663 8986 (West US & Canada)
- **France** – **LSI France SARL**
Tel: 1 43 94 99 86
Fax: 1 43 94 99 89

FAST PROCESSORS

our latest R3000 devices—40-MHz ICs are coming off the lines in economically feasible production quantities.”

Motorola's Reinhart agrees. "At the present time the 68040 is 580x609 mils with 1.2 million transistors. It's cost-effective, yet if you asked two years ago we would have said it wouldn't have been."

Today's defect-reduction and yield-enhancement techniques enable manufacturability. "Our goal has been to consistently double performance," Reinhart says. "We presently build 68040s in two-layer metal, 0.8- μ m drawn feature size (0.7 L-effective) dimensions. We've also built a few 68040s with 0.65- μ m features, and we're qualifying this process for use later in the year. This will give a smaller die cost reduction and make possible 40 MHz."

Submicron 68050s are coming

Notably, 0.65- μ m is also the starting point for Motorola's next-generation superfast CISC—the 68050. "To double the 040's performance, we have to set a clear path to 0.5- μ m CMOS," says Reinhart. "We've already invested in a fabrication line for 8-in. wafers, with process capability for microprocessors with very fast SRAM."

Regardless of the confidence semi-

conductor manufacturers express for optical lithography, resource-rich firms such as Motorola are also investing in X-ray lithography. Motorola is doing so in conjunction with IBM, Sematech and others.

"It's a tremendously scary technology, though," says Reinhart. "It costs millions just to build a re-

quired particle accelerator. One wants to be generating a lot of revenue to justify that."

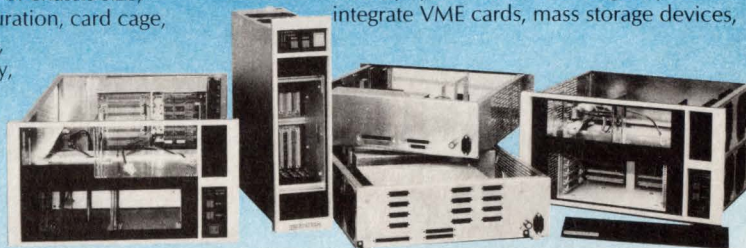
Reinhart says optical lithography will live on, even where it has recently been predicted to fall apart. "There's no way to avoid X-ray in the future," he says, "but is it at 0.5, 0.25 or less than 0.1 μ m? We don't know." ■

A COMPLETE FAMILY OF VME SYSTEM PACKAGES

FINALLY YOU CAN SELECT EXACTLY WHAT YOU NEED!

Thousands of Different Systems from Standard Modular Parts

You can choose the most appropriate combination of chassis size, basic configuration, card cage, mass storage, power supply, I/O panels, cooling and enclosure. Zoltech's modular chassis concept allows your VME system to be optimized for specific applications and environments.



Zoltech Delivers

We will provide you with anything from an empty metal shell to a complete turnkey system. And, we will gladly integrate VME cards, mass storage devices,

I/O cables, peripherals and system software.

Low Prices and Fast Delivery

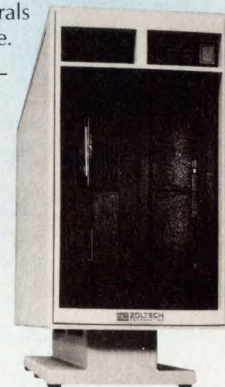
The use of our off-the-shelf components allows your special system package to be delivered quickly and at a standard system price.

Long-Term Reliability

A low-cost package really isn't low-cost if it fails in the field. Zoltech's unique positive-pressure, filtered air cooling system insures that your machine will run clean and cool. The EMI shielding integrity of the fully-enclosed chassis is preserved regardless of the number of cards installed in the card cage.

A typical complete system:

VLV-11/Model 30 chassis, twelve 6Ux160 slots, 68020 CPU, 5MB memory, 18 serial channels, floppy, cartridge tape, dual Winchester, 400W power supply, eight fans, in tower enclosure.



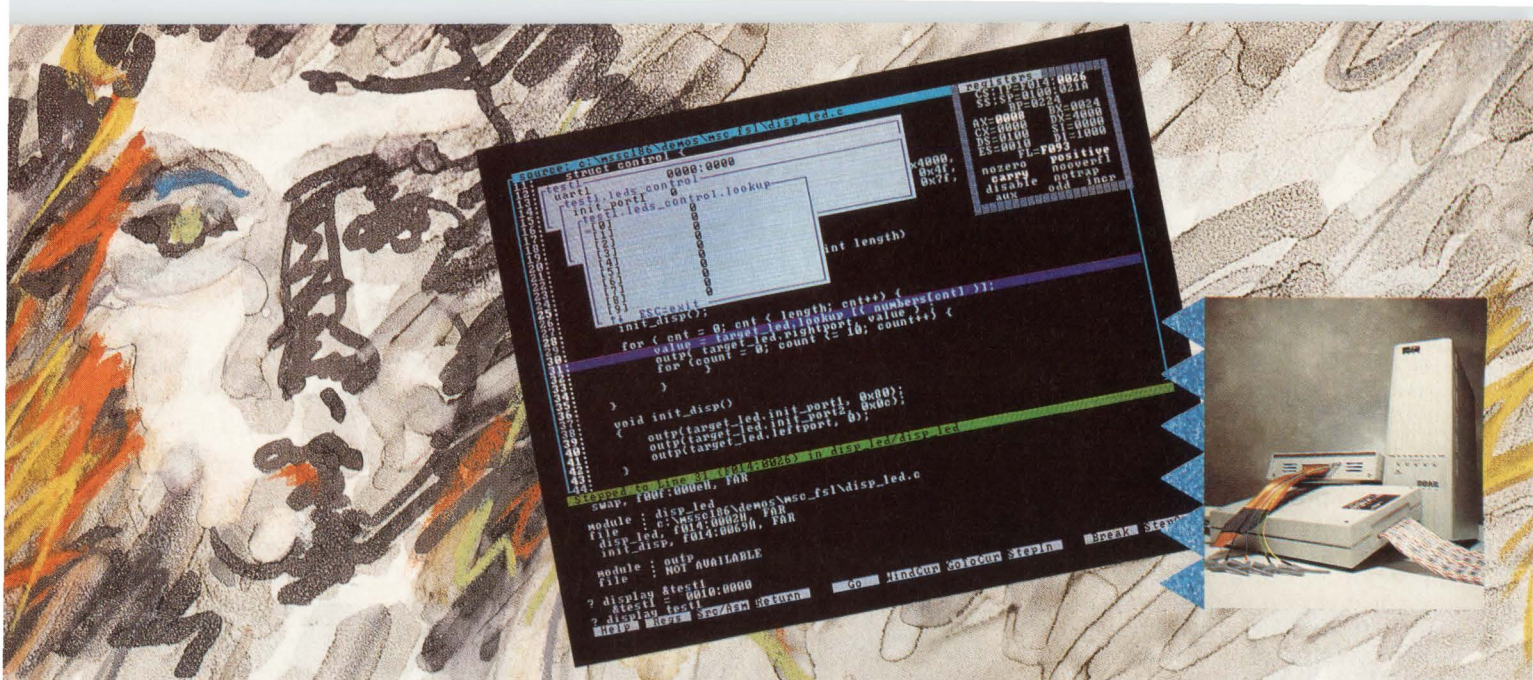
ZOLTECH CORPORATION

7023 Valjean Avenue, Van Nuys, California 91406 USA
(818) 780-1800 FAX (818) 780-1978
Representative and dealer inquiries are invited.

For more information about the technologies, products or companies mentioned in this article, call or circle the appropriate number on the Reader Inquiry Card.

Advanced Micro Devices	
(408) 732-2400	Circle 255
Bipolar Integrated Technology	
(503) 629-5490	Circle 256
Fujitsu Microelectronics	
(408) 922-9000	Circle 257
Hewlett-Packard	
(800) 752-0900	Circle 258
IBM	
(800) 426-3333	Circle 259
Integrated Device Technology	
(408) 727-6116	Circle 260
Intel	
(800) 548-4725	Circle 261
Intergraph	
(415) 494-8800	Circle 262
MIPS Computer	
(408) 720-1700	Circle 263
Motorola Semiconductor	
(512) 891-2839	Circle 264
National Semiconductor	
(408) 721-5000	Circle 265
SGS-Thomson	
(719) 630-4000	Circle 266
Texas Instruments	
(800) 336-5236, ext. 700	Circle 267

Call or write for complete specifications and prices



Power Debugging ... for Real-Time Targets

SOPHIA EMULATORS SUPPORT

INTEL

80C86/88	10 MHz
80C186/C188	20 MHz
80286	25 MHz
80386	25 MHz
80386SX	16 MHz

MOTOROLA

68000/10/12	16 MHz
68020	20 MHz

NEC

V20/V30	16 MHz
V40/V50	10 MHz
V25	16 MHz
V33	16 MHz
V53	16 MHz
86/V	16 MHz

... plus processors from
AMD, Hitachi, Mitsubishi,
Rockwell, Zilog.

Do you need to debug a real-time embedded system? Do you use C along with assembly language?

Our emulation systems can help you complete your project faster.

Real-Time Target Control

- Emulate without stealing target resources or adding wait states.
- Step through your actual source code, comments and all.
- Choose from many popular compilers.
- View code, registers, data, and commands all at once with our windowed interface.
- Capture precise information using our powerful trace capabilities, including sequential triggers, all in real time.

- Use full symbolic debugging capabilities, including high-level trace.

Real-Time Technical Support

- Experienced software and hardware engineers.
- Step-by-step troubleshooting assistance.
- 24-hour Bulletin Board for users. Upload problem software, questions. Download code fragments, new releases, examples.

Sophia Systems' emulators give you the *power* to debug your target in your environment. And we're continuing to expand our capabilities to match your processor and debugging needs.

Call and tell us about **your** target.

Sophia
systems
and Technology

1-800-824-9294

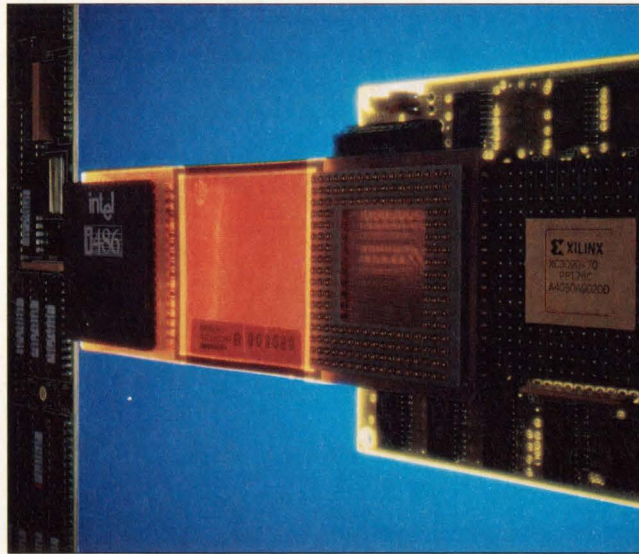
Sophia Systems and Technology, 777 California Ave., Palo Alto, CA 94304, TEL: (415) 493-6700 FAX: (415) 493-4648
 Sophia Computer Systems, Ltd., Alpha House, London Road, Bracknell, Berkshire RG12 2TJ England, TEL: 0344-862404 FAX: 0344-861374
 Sophia Systems Co., Ltd., Shinjuku NS Bldg. 8F, 2-4-1 Nishishinjuku, Shinjuku-ku, Tokyo 163, Japan, TEL: (03) 3348-7000 FAX: (03) 3348-2446

©1991 Sophia Systems and Technology

DESIGN AND DEVELOPMENT TOOLS

32-bit emulators struggle with processor complexities

Jeffrey Child, Associate Editor



The Mice-V emulator for the i486 from Microtek International features an isolation mode that lets users remove the processor from the probe tip and still do emulation. The emulator doesn't need functional hardware to begin emulating—all that's required is a working clock signal.

With budgets tighter than ever, designers of 32-bit microprocessor-based systems may welcome any alternative to buying an emulator. Most admit, however, that there's no real substitute for a full-blown in-circuit emulator for debugging systems in real time. And as processor speeds reach 33 MHz and above, many are starting to question the feasibility of building emulators at a reasonable price.

The challenge for emulator manufacturers is to create emulators with the control capabilities needed to debug complex programs and to integrate complex systems. But accomplishing this for 32-bit devices is not an easy task, especially with the combinations of high speed and complex architectures found in today's high-end microprocessors.

As microprocessors have become more complex, so has the task of debugging and development. Faster devices can process more instructions, leading to larger applications, leading to more software. While around 80 percent of that software in a design needs to talk only to other parts of the software, there's still that important remaining part of the code that must interface with the hardware directly. Developing this 10 to 20 percent of code is the job of the emulator.

■ Network support

As a result of growing size of code, the ratio of software designers to hardware designers involved on projects has gone from 1:1 to around

10:1. This new design environment requires development tools that fit a team-oriented concurrent engineering methodology. Recognizing this, an increasing number of emulator vendors are including network support in their products so that emulators can pass code to other systems.

"A problem that comes up with 32-bit designs is that the scale of projects has changed, and all the managers and designers working on the project should recognize that," says Richard Jensen, vice-president of new business development at Applied Microsystems (Redmond, WA). "Tools are needed to support that different scale."

Design projects for 32-bit emulators are more complex, creating emulation problems for designers and cost problems for emulator manufacturers. "The first scale of problems is linear—wider addressing and data capability. That means more signals, more pins and more problems," says Jensen. "So from the number of added signals all the way to the amount of memory that's required, the tool is going to cost more to build."

Speed requirements also contribute to cost. The generally accepted rule is \$1,000/MHz, which holds up reasonably well for most of the full-featured emulators (see chart, p 124).

Applied Microsystems' latest offering, the EL3200, is a development environment for the Intel i960CA microprocessor. The system includes a 33-MHz emulator and a software development package. The emulator

is designed to offer real-time transparent emulation to full i960 speeds with no wait-states. Special features of the i960 are supported by the EL3200, including pipelining, burst modes and the different bus widths. The emulator's trace-and-event system allows tracking and isolation of complex, real-time interactions between hardware and software. Full networking capability is provided for Sun Sparc workstations and personal computer-compatibles.

■ Complex architectures

Another hurdle manufacturers of 32-bit emulators face is the sophisticated architecture of the latest processors. "It used to be that the logical execution flow and the physical execution matched. By observing the execution on the bus you could determine what was going on inside the chip," says John P. Romano, manager of research and development at Hewlett-Packard's Logic Systems Division (Colorado Springs, CO).

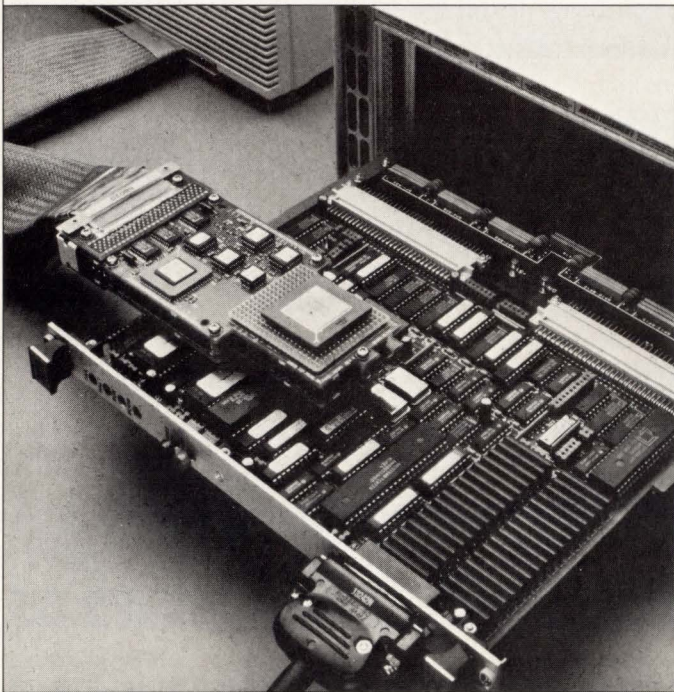
In 32-bit processors that's no longer the case. Internal pipelines, multiple execution units for floating point and memory management, and on-chip caches all confound an emulator's ability to observe the internal workings of a chip. This complexity also inhibits the ability to correlate activity on the system bus with the high-level instruction the user expects to see. "You basically have to replicate the logic of the processor," says Romano. "Accomplishing this is becoming prohibitively expensive."

PRODUCT FOCUS/32-bit Emulators

Model	Speed (MHz)	Processor(s) supported	Overlay memory (bytes)	Number of hardware breakpoints	Number of breakpoint levels	Trace buffer depth (bits)	Performance analysis	Price	Comments
Applied Microsystems 5020 148th Ave NE, PO Box 97002, Redmond, WA 98073-9702 (206) 882-2000 Circle 301									
EL3200	33	i960CA	4 M	53	4	8 k×139	Y	\$30,000	zero wait-state 20-MHz read and zero wait-state 30-MHz write; fully networked; Sun or PC hosts
EL3200	33	68020, 68030	2 M	53	4	8 k×139	Y	\$30,000	same as above
ES1800	25	68020	2 M	32	4	2 k×10	Y	\$16,000	Sun network operation; SCSI communications; Sun, PC or VAX hosts
Cadre Technologies 19545 NW Von Neumann Dr, Beaverton, OR 97006 (503) 690-1300 Circle 302									
SmartProbe/386	25	80386	2 M	4	4	2 k×88	Y	\$19,450	source-level debug for C and Ada real-time source trace; Sun, PC or VAX host
SmartProbe/020	25	68020	512 k	8	4	2 k×96	Y	\$12,450	same as above
SmartProbe/030	25	68030	512 k	8	4	2 k×96	Y	\$16,450	same as above
Embedded Performance 2840 San Tomas, #100, Santa Clara, CA 95051 (408) 980-8833 Circle 303									
SYS29K	25	AM 29000, AM 29005, AM 29050	256 k-4 M	50	16	2 k	Y	\$14,995-\$32,370	interfaces to assembly and C debuggers; supports 7 host systems
SYS29K-TURBO	33	AM29000, AM29005, AM29050	256 k-4 M	50	16	8 k	Y	\$24,995-\$66,870	Ethernet interface; supports 7 host systems; low-capacitance probe head
SYS-R3000	33	MIPS R3000, R3000A, R3001	256 k-4 M	50	16	8 k	Y	\$27,500-\$69,870	Ethernet interface; supports 5 host systems; cross-development software
Hewlett-Packard PO Box 617, Colorado Springs, CO 80901-0617 (800) 447-3282 Circle 304									
HP64774	25	AM29000, AM29005	1 M	8	8	1 k×80	Y	\$24,445	supports big- and little-endian byte ordering; supports several file formats
HP64772G	30	NS32532, NS32GX32, NS32GX320	512 k-4 M	8	8	1 k×80	Y	\$24,294-\$30,554	precise dequeuing and analysis of code running in cache
HP64778G	30	68040	512 k-4 M	8	8	1 k×80	Y	\$39,960	active probe; extensive help; software dequeuing; custom memory mapper
HP64420SB	20	80386DX	512 k	16	16	2 k×80	Y	\$28,475	software dequeuing; full 80386 debug register support
HP64773A/L	50	AT&T DSP32C	64 k	8	8	1 k×64	Y	\$28,503	interfaces on the PC and HP4000 series 300/400 workstations
HP64760	25	i960KA/KB, i960MC	4 M	8	8	1 k×108	Y	\$25,000	real-time transparent access to target memory; supports several file formats
HP64748	33	68020, 68ECO20	2 M	8	8	1 k×80	Y	\$19,300	download speeds exceed 1 Mbyte/min; cable adapters allow probing of PGA and PQFP packages
HP64430/31	33	68030, 68ECO30	1-2 M	16	16	2 k×80	Y	\$41,500	active probe; custom memory mapper; zero wait-state to target memory
Huntsville Microsystems PO Box 12415, 4040 S Memorial Pky, Huntsville, AL 35802 (205) 881-6005 Circle 305									
HMI-200-68020	16, 25, 33	68020, 68ECO20	256 k-4 M	8	4	two 4 k×104	Y	\$12,000-\$21,000	integrated with window-driven debugger; real-time performance analysis operates transparent to system
HMI-200-68030	16, 25, 33	68030, 68ECO20	256 k-4 M	8	4	two 4 k×104	Y	\$15,000-\$23,000	same as above
HMI-200-68300	16, 20	68331/2, 68340, 68330	256 k-4 M	8	4	two 4 k×104	Y	\$16,000	same as above

Model	Speed (MHz)	Processor(s) supported	Overlay memory (bytes)	Number of hardware breakpoints	Number of breakpoint levels	Trace buffer depth (bits)	Performance analysis	Price	Comments
Intel 3065 Walsh Ave, Santa Clara, CA 95051 (408) 765-8080									Circle 306
ICE386DX	25, 33	80386DX	128 k-2 M	12	4	4 k×96	optional	\$22,500	windowed-interface; trace filtering
ICE486/33	33	i486	2 M	12	4	8 k×96	N	\$38,000	execution trace instructions; sequential break points on events that occur from cache; trace filtering
ICE960-R3.0	16, 25	i960KA/KB i960/SA/SB	2 M	10	8	1 k×240	N	\$16,495	module selection for symbol table improves download time; trace filtering
Microtek DSD 3300 NW 211th Ter, Hillsboro, OR 97124-7136 (503) 645-7333									Circle 307
Mice-III	25	68020	1 M	7	8	8 k×96	Y	\$16,500	code coverage option identifies code that is or isn't used
Mice-III	25	68030	1 M	7	8	8 k×96	Y	\$18,000	same as above
Mice-V	33	80386	512 k	12	4	8 k×144	N	\$25,000	—
Mice-V	20	80386SX	512 k	12	4	8 k×144	N	\$18,250	—
Mice-V	33	i486	—	12	4	8 k×144	N	\$32,000	can isolate the i486 chip from the emulator pod; permits debugging of nonfunctional hardware
Motorola PO Box 3600, Austin, TX 78764 (512) 891-3759									Circle 308
CDS32	25	68331/2	1 M	4	4	8 k×136	N	\$7,950	runs on PC-compatible or PS/2 hosts; 16 software breakpoints
Softaid 8930 Rt 108, Columbia, MD 21045 (301) 964-8455									Circle 309
CodeStalker 386	33	386	512 k	4	1	4 k×48	N	\$9,995	fiberoptic link provides fast downloads (250,000 bytes/s)
CodeStalker 386SX	16	386SX	512 k	4	1	4 k×48	N	\$9,995	same as above
Step Engineering 661 E Arques Ave, Sunnyvale, CA 94086 (408) 733-7837									Circle 310
Adapt II Plus	33	AM29000, AM29005, AM29050	1 M	1	0	4 k×160	N	—	logic analyzer interface; zero wait-state overlay memory
Excel 930	40	Fujitsu SparcLite MB86930	0	5	0	8 k×160	N	—	Ethernet interface; 32 external bits; cache reconstruction
ExpressPlus 960CA	33	i960CA	0	9	0	8 k×160	N	—	Ethernet interface; cache reconstruction
Adapt II	25	AM29000, AM29005, AM29050	1 M	1	0	4 k×160	N	—	logic analyzer interface; 32 external bits; zero wait-state overlay memory
Zax 2572 White Rd, Irvine, CA 92714 (714) 474-1170									Circle 311
ERX-68030/20 HS	25, 33	68020/30, 68881/2	256 k-2 M	1,000,000	4	8 k×88	optional	\$23,150	256-k×4-channel memory scheme allows over 1 million hardware breakpoints
ERX-68030	20	68030, 68881/2	256 k-2 M	1,000,000	4	8 k×88	optional	\$16,840	same as above
ERX-68020	20	68020, 68881/2	256 k	1,000,000	—	8 k×88	optional	\$14,730	same as above
ERX-80386	16	80386, 80387	256 k-2 M	1,000,000	4	8 k×88	optional	\$16,840	same as above

DESIGN AND DEVELOPMENT TOOLS

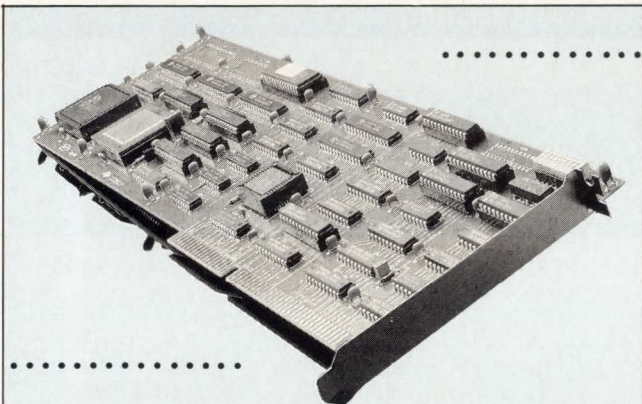


Designed to deal with the complexities of 32-bit microprocessor-based design, Hewlett-Packard's HP64440 emulation/analysis subsystem for the 68020 processor provides real-time, no-wait-state operation up to 33-MHz in target memory. The emulator uses an active-probe technology that provides maximum electrical and functional transparency.

HP's 64000 series of emulators offers a feature called prestore, which is particularly important in larger applications. The emulator can be set up so that the trace buffer captures only write to this data area. If the prestore is on, it captures not only the write cycle but also the previous state; in other words, it identifies where the write came from. If a pointer value is misused in C, for example, prestore can capture information showing which piece of code uses that pointer and where the pointer received the wrong value.

Cache problems

On-chip caches provide advantages to aid system performance. They not only boost speed but also let instructions be executed inside the chip, freeing up the bus for other devices in the system to use. Cache can be a nightmare for in-circuit emulators as they try to match in-



**Universal
Compression Processor**

- Compatible with all major imaging boards (AT bus).
- Image compression with proposed JPEG standards.
- Offers both lossless and selectable quality.
- Processes TIFF 5.0, PCX and GIF image files.
- Two optional processors to accelerate time-sensitive operations.
- A compression processor from a reputable imaging supplier.

AT is a registered trademark of International Business Machines Corporation.



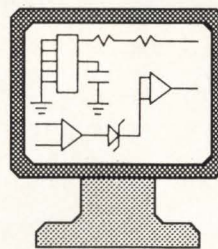
EXCELLENCE IN MACHINES THAT SEE

Tel.: (514) 333-1301 • 1-800-361-4914 (USA) • Fax: (514) 333-1388

CIRCLE NO. 69

**PCB MANUFACTURING
DESIGN AND ARTWORK !**

ALL YOUR CIRCUIT BOARD NEEDS UNDER ONE ROOF



PCB MANUFACTURING

- 2 Day turn on multi-layers
- Prototype and production
- One tooling charge for both
- Turn-key assembled boards

PCB DESIGN

- Backplanes
- Impedance control
- Analog and ECL
- Surface mount

TECHNICAL ASSISTANCE

- PCB design tips
- Mfg cost cutting tips
- Testing guidelines
- We accept gerber data via modem (714) 970-5015

CALL FOR A QUOTE !

A MANUFACTURING, PCB DESIGN AND SUPPORT CENTER



4761 E. HUNTER AVE. ANAHEIM, CA. 92807

TEL: (714) 970-2430 FAX: (714) 970-2406

CIRCLE NO. 71

DESIGN AND DEVELOPMENT TOOLS

structions executed with corresponding bus cycles. Keeping track of instructions executed from main memory is straightforward, but when instructions are executed from inside the cache, no bus cycles are involved.

The 8-kbyte cache in the Intel 486, for example, complicates the job of an emulator. Some emulator vendors provide the option to turn off the cache while emulating, but by doing so the system is no longer running in real time. Other solutions involve using algorithms to estimate which instructions are in the cache. Intel, which also makes emulators, has an obvious advantage because it can tap into proprietary signals on the chip. Using these signals, Intel can identify exactly which instructions are being executed from in the cache. The 486 also contains debug registers that aren't proprietary.

"The i386 and i486 were designed for debugging from the start," says Tovey Barron, senior technical marketing engineer at Intel (Hillsboro, OR). "They both have debug registers that provide the capability to control events that occur in the chip, as a first step in that direction. As the caches get bigger, and the functions on the chip get more and more sophisticated, the debug capability built into the chip will have to become equally sophisticated, because the emulator vendor will not be able to see into a chip through its pins."

■ On-chip support for RISC

Solving emulation problems of faster-speed RISC processors may also require on-chip circuitry that supports emulation. In fact, the lack of such on-chip support is a possible reason behind the lack of emulators available for RISC processors. When it comes to building an emulator for a Sparc or MIPS RISC processor, speed isn't the fundamental problem. "RISC chips are easier to emulate," says Applied's Jensen. "The cache is outside, the MMU is outside, and there are no half instructions or byte-wide instructions. It's all pretty balanced. The problem is that RISC processor designers have put very little in the chip that lets us get control of the processor."

Despite the many concerns expressed about the feasibility of building emulators for tomorrow's faster processors, some views are optimis-

tic. "The market has proclaimed the end of emulators since about 1984, when everyone was saying that it will be impossible to emulate the next generation of processors," says Rick Leatherman, vice-president of marketing at Microtek International's Design Systems Division (Hillsboro, OR). "Emulators can be built for almost any processor out there, as long as the speeds are within TTL limits. However, the price to support the faster speeds goes up exponentially."

Even some of the high-end 32-bit emulators are not all that they could be. According to Leatherman, even sophisticated emulators require that a board be at least 75 percent functional before it could be of any use. To address this issue, Microtek's Mice-V emulator for the 486 features an isolation mode with which a user can actually remove the processor from the probe tip. When the emulator is initialized and realizes that the

processor is missing, it allows the user to stimulate the target system. Thus, the emulator doesn't need functional hardware to begin emulating; all that's required is a working clock signal. The key to this is a cable technology, where the chip is mounted on a small printed-circuit board at the end of the cable.

Full in-circuit emulation alternatives that offer some view into the internal workings of a processor are appearing. Texas Instrument's scan-based emulation and Applied Microsystems' CodeTap are two examples. But neither of these offer true substitutes for full in-circuit emulation. "If you could come up with an instrument or a methodology," says Jensen, "that lets you control the execution of the processor, provide visibility into the execution of that processor (even with interrupts coming in), and do it in real-time, then you've got a substitute for an emulator." ■

ALL ABOARD!

The Engine with Everything You Need
To Get There On Time

ZT 8901
Single Board V53
(80286) Computer

STD 32

Call For
Free On-site
Demonstration
Or Technical Data
805-541-0488
FAX: 805-541-5088

- STD 32 and STD-80 compatible
- 16 MHz V53 (80286) processor
- 1 Mbyte RAM (Static), 1 Mbyte ROM
- Numeric data processor socket
- Flash EPROM Support
- Three serial ports (RS-232/485)
- One interrupt controller (8259)
- Three 16-bit counter/timers (8254)
- STD 32 Multiple Bus-master Operation
- Three DMA channels (8237)
- 8-bit or 16-bit SBX with DMA
- Real-time clock
- 48 parallel I/O lines (Opto 22-compatible)
- AC/DC power fail detection
- DOS, VRTX, STD ROM and STD LADDER software support
- Watchdog timer
- 20-year MTBF (175K hours)
- -40° to +85° C Option
- Dynamic 8- and 16-bit bus sizing
- Low power CMOS with sleep mode
- Two-year warranty, and more.

ZIATECH CORPORATION

CIRCLE NO. 72

If you can see it, we can print it.



No matter what application you're using, no matter what monitor you're viewing it on, the CH5500 video color printer can produce a hard copy. It supports over 350 video sources—more than any other printer.

Moreover, since the CH5500 doesn't use software, it captures your image fast—so you can get back to work. And it offers outstanding 300 dpi quality in both A and B sizes.

To find out more, give us a call at 1-800-873-4561, Dept. SI-A4.

After all, we pioneered video color printing. And we still do it best. Anybody can see that.

SII 
Seiko Instruments

DESIGN AND DEVELOPMENT TOOLS

Simulation tool simplifies top-down analog design

One of the problems in migrating analog simulation into a top-down design environment has been the reluctance of analog engineers to work in software languages to describe analog behavior. In addition to this reluctance, there's no IEEE-sanctioned analog hardware description language (AHDL) for even the most willing engineer to embrace. Valid Logic Systems' Profile and Analog Workbench II may be the answer to this dilemma.

Profile lets analog designers describe blocks or entire circuits at the behavioral level by using a combination of graphics and text. The resulting models can be simulated in Workbench II, a mixed-behavioral and structural-level design environment. With this combination, engineers can adopt a top-down or bottom-up strategy, which is useful for large, hierarchical designs that must be partitioned across multiple design teams.

Strong models

Profile's graphical interface lets users create and simulate an architecture without having to resort to a language-based behavioral modeling technique. The Profile models also support user-specified error and warning messages, allowing in-process circuit diagnostics.

"Analog behavioral models are key elements of a good architectural design," says Eric Filseth, Valid's product marketing manager for analog CAE. "After all, if your specification is wrong, most probably the product won't work. But getting accurate analog models has been a real problem, especially for parts that aren't entirely electrical, like motors and sensors. The characteristics of such an electromechanical device have a definite impact on the

circuit that drives them. So if you want to design a good circuit, you need a good model." A purely language-based approach, he adds, is not going to work until an AHDL standard is defined.

With Profile, Valid focused on ease of use: engineers aren't required to use the templates or compilation methods that are common

and basic arithmetic. In addition to providing electromechanical device models for motors, solenoids and sensors, Profile can build mixed analog-digital models for components such as data converters and phase-locked loops.

Multilevel simulation

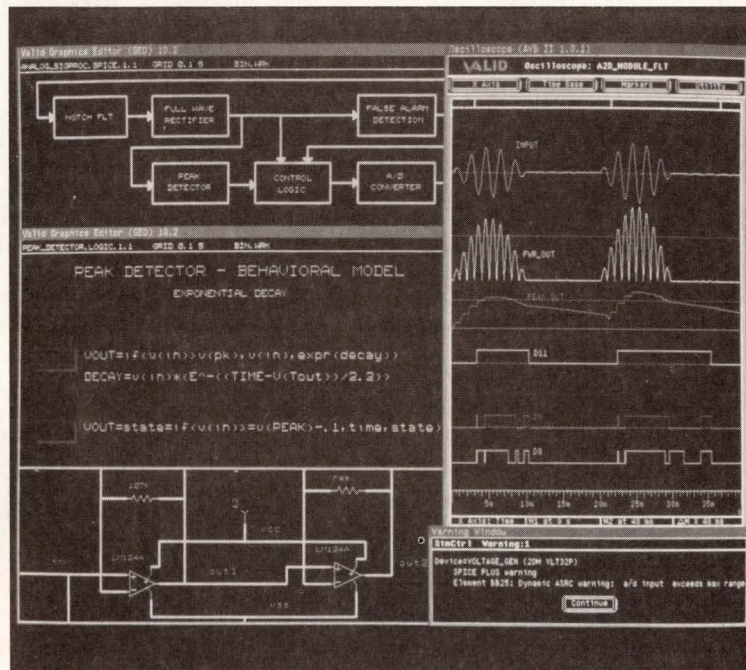
Once analog designers have developed Profile models, they can simulate and analyze their designs in Analog Workbench II. Multilevel simulations containing both high-

level behavioral descriptions and transistor-level circuitry operate in the simulation environment. It's also possible to simulate systems in which some, but not all, of the blocks have been fully designed at the circuit level. This allows users to begin manufacturability, quality and reliability analyses at early stages in the design.

Profile models are fully compatible with all Analog Workbench II analysis tools including sensitivity analysis, pole/zero analysis, stress analysis, and parameter analysis. For specific needs, Valid also provides a User-Coded Models feature, which lets engineers write analog models in C or Fortran and simulate them in Valid's version of Spice, Spice Plus, along with conventional devices.

Profile is available now as an option to Analog Workbench II for \$15,000. Analog Workbench II, including user interface, basic analysis tools and Spice Plus, is available on Sun, Digital and IBM RISC System/6000 workstations. Prices start at \$12,000.

—Mike Donlin



In this example of Profile at work, top-down design begins with a system diagram (top left). Profile models of one or more blocks can then be created (center left) while a detailed circuit-level implementation of this block can reside in the design hierarchy. After simulation, the system response is shown in the oscilloscope output window (top right), and a model-generated diagnostic message appears (bottom right).

with language-based tools. Profile models can incorporate effects not supported by macromodeling such as hysteresis, memory, state variables and conditional branching. This lets users construct complex models including pulse-width modulators, multiplexers and sample-and-holds. For even higher-speed analyses, piece-wise linear models can be created in Profile. Analog designers can also write flexible descriptions of a range of user-programmable blocks, including differential equations, Laplace domain-transfer functions

Valid Logic Systems

2820 Orchard Pky
San Jose, CA 95134
(408) 432-9400

Circle 351

Design system option generates DSP code from block diagrams

Two new options for Comdisco Systems' Signal Processing Worksystem (SPW), a CAD system for digital signal processing, let designers automatically generate program code from the same graphical description that can be used for the system architecture. These features give designers greater flexibility in partitioning their designs between hardware and software and in applying multiple processors to a system design.

The two new software generation modules, called MultiProx (MPX) and DSP ProCoder (DPC), fit into the SPW environment, which includes a graphical block diagram editor and a signal display editor that lets designers describe a DSP system in terms of signal flow blocks. SPW already can output VHDL and netlist descriptions for the design of ASICs and printed circuit boards.

Simple and automatic

MPX lets DSP designers partition a system block diagram into various functional regions to be executed by

separate processors. The system then generates C code for each processor. DPC targets specific fixed-point DSP chips and automatically generates assembly language code from the signal flow block diagram.

MPX supports all the SPW application libraries, which include some 500 DSP signal blocks, from filter designs and encoder/decoder functions to math blocks. Users simply assemble the blocks with the SPW block diagram editor and then draw boxes around those portions of the diagram that they wish to run on separate processors.

The system not only generates the C code to run on the different processors, but automatically handles the details of interprocessor communication via shared memory. The links between modules can use either data flow designs or control flow designs. Users have the option to substitute their own interprocessor communication protocols.

The C code can then be compiled

for any general-purpose processor or specialized DSP processor for which a C compiler exists. This allows designers to do a good amount of their design verification in an execution environment other than the final target system. It also lets them experiment with load balancing and identify possible bottlenecks among multiple processors. Decisions can also be made about possible hardware implementation of all or part of the design in ASICs.

Comdisco has initially targeted MPX at Texas Instruments' TMS 320C40 and Motorola's M96002 DSP chips on chip-specific PC-based hardware and software development systems. In the future, Comdisco will target MPX and additional chips at different system buses, such as VMEbus and VXibus; it also plans to add its own multiprocessing performance diagnostic tools.

More-specific option

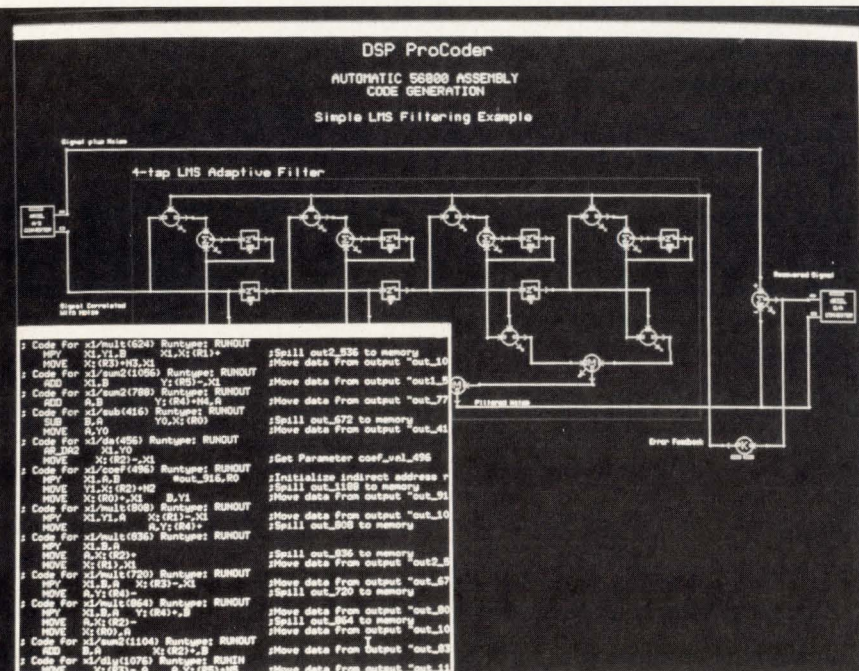
DPC, like MPX, generates code from graphical signal flow diagrams. However, DPC is aimed at the efficient generation of assembly code and is therefore tailored for specific DSP chip architectures and instruction sets. The initial target processor will be Motorola's DSP56001, followed by Texas Instruments' TMS 320C50.

Initially DPC will support fixed-point DSP chips where optimization is essential; later, it will be moved to support floating-point DSP processors. Currently it supports a library of 60 functional blocks and can generate one to three lines of assembly per kernel block.

Both MPX and DPC are based on an open architecture in which designers can add their own blocks or segments of code. Both code generator systems run on the same environments as the SPW—Sun, Hewlett-Packard/Apollo and Digital Equipment Corp workstations.

Both software modules are scheduled for shipment in the fourth quarter. MPX will cost \$10,000; DPC will cost \$15,000.

—Mike Donlin



A DSP ProCoder screen shows a signal flow block diagram created with the Signal Processing Worksystem's block diagram editor. In the accompanying window is 56001 assembler code that has been automatically generated directly from the block diagram.

Comdisco Systems

919 E Hillsdale Blvd
Foster City, CA 94404
(415) 574-5800

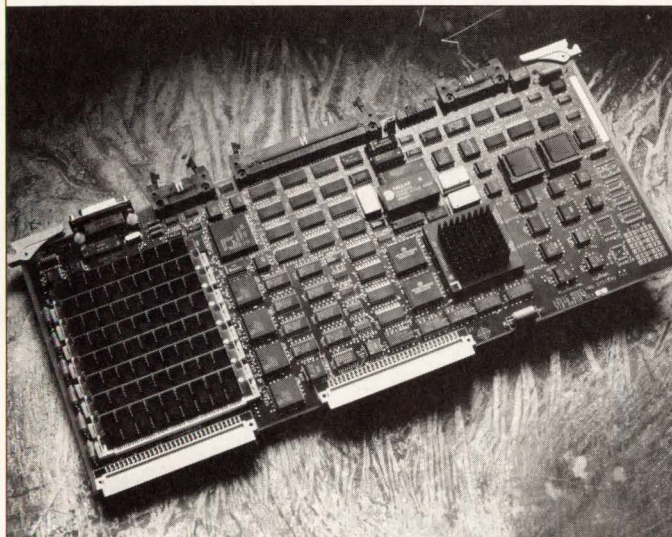
Circle 354

Hardware modelers meet needs of small and large design teams

A typical circuit board today consists of a complex microprocessor and coprocessor, as well as a conglomeration of ASICs, standard parts, I/O, memory and glue logic. For such an

the 486, 68040, R3000A, and 29050.

In a nod to the needs of smaller design teams who might not be able to afford the horsepower of the LM-1200, Logic Modeling has also rolled



At the heart of the performance of Logic Modeling's LM-1200 hardware modeler lies this 12-layer, surface-mount board based on a 33-MHz 68040, with up to 8 Mbytes of memory and a 64-kbyte cache.

out the LM-500. It supports devices as large as 160 pins, including the 80386, 68030 and 29000. The LM-500 supports more than 95 percent of the hardware models currently offered by Logic Modeling.

To support existing users, Logic Modeling also is offering an upgrade kit for the LM-1000. The kit, which will bring the performance of the LM-1000 up to that of the LM-1200, consists of a CPU board and software. Although the LM-1000 will be phased out of production by the end of June 1991, Logic Modeling plans to support existing systems.

The LM-1200, the LM-500 and the upgrade kit will all be available by mid-June. Prices for the LM-1200 start at \$87,000. The LM-500 starts at \$35,000. The upgrade kit costs \$19,000.

—Mike Donlin

Logic Modeling Systems

1520 McCandless Dr
Milpitas, CA 95035
(408) 957-9181

Circle 352

arrangement to work, reliable models must be incorporated into a simulation environment to accurately predict prototype behavior. As clock speeds and device complexity increase, modeling technology must keep pace—a need that Logic Modeling Systems has addressed with the introduction of its latest hardware modelers, the LM-1200 and LM-500.

The LM-1200 achieves up to six times higher performance than Logic Modeling Systems' first hardware modeler, the LM-1000, which was introduced in 1989. To do so, it uses a much faster CPU (the 25-MHz 68040), an improved network server and enhanced hardware-modeling algorithms. The system also hosts 8 Mbytes of memory (expandable to 32 Mbytes), which increases its fault simulation capacity by as much as a factor of 10.

Higher processing speeds let the LM-1200 support multiple design teams, all working concurrently with a variety of complex models. As many as 2,560 signal pins can be modeled on the Logic Modeling system, and support is provided for complex standard devices, including

SUPER SOLUTIONS

ALACRON provides expandable i860 based Super Solutions for your application

- AT or VME Bus
- Multiple i860 daughter cards providing up to 240 MFLOPs on a single card
- Megapixel High Speed True Color Graphics
- DT Connect and SCSI I/O
- Up to 64 MBytes of 0 wait state local memory
- The best i860 software including DOS and UNIX interfaces, C and Fortran compilers, multitasking/multiprocessing kernels, and scientific subroutine library

71 Spitbrook Road, Suite 204 • Nashua, NH 03060
Telephone: (603)891-2750 • Fax: (603) 891-2745

Trademarks are property of their respective holders.

Marketing OEM Computer Graphics?

**AMONG ICC ATTENDEES,
COMPUTER DESIGN IS #1**

During 1989/90, Dataquest/ICC asked their engineering graphics series attendees to name the publications they read.

**AMONG
ENGINEERING GRAPHICS
SERIES ATTENDEES
THE #1 CHOICE
IS COMPUTER DESIGN.**

But that shouldn't be a surprise. After all, COMPUTER DESIGN is 100% design & development qualified, 70% engineering management and has more than 70,000 engineering managers. Plus we reach buyers and specifiers of graphics/imaging products in a big way:

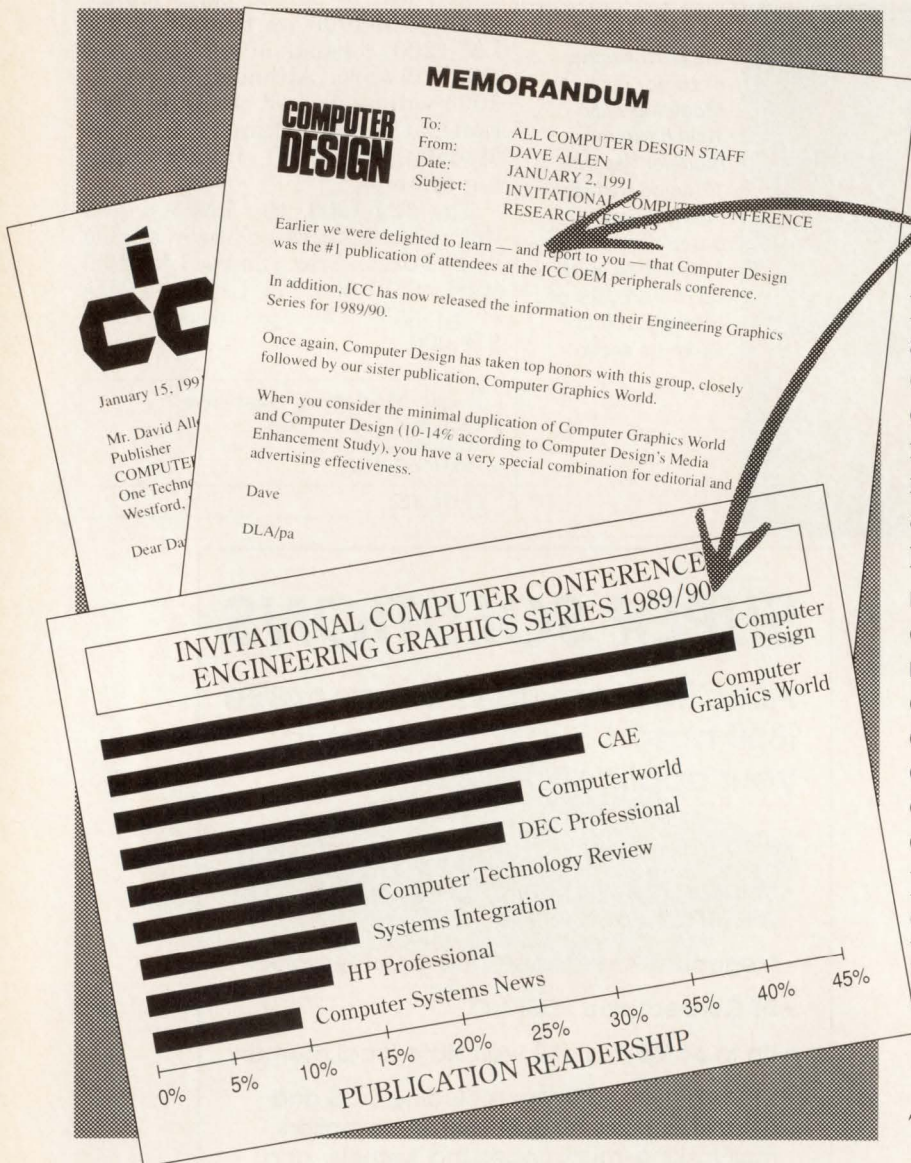
PRODUCT	# SUBSCRIBERS
Graphics/Display Controllers	42,681
Image Processing Boards	23,053
Graphics ICs	24,792
CAE/CAD/CAM Workstations	44,210
Graphics/Imaging	40,804
Graphic Display Terminals	47,325
Graphic Input Devices	30,579

Plus more than 45,000 specifiers of CAE/CAD/CAM software.

If you're marketing graphics products to OEM specifiers, we should be your #1 advertising buy.

Call any of us for more information.

Thanks, and good selling.



* June, 1990 BPA
Publisher's Statement

Delivering Today's Electronics OEM

PENNWELL PUBLISHING COMPANY • ONE TECHNOLOGY PARK DRIVE • WESTFORD, MA 01886 • 508-692-0700

For more information, contact any of us ...

PUBLISHER: David L. Allen, 508-392-2111 • ASSOCIATE PUBLISHER: Tim L. Tobeck, 516-883-8815 • SALES OFFICES: PORT WASHINGTON, NY, Eleanor Hobbs, 516-883-8815 • WESTFORD, MA, Tim Pritchard, 508-392-2217 • MATTESON, IL, George Mannion, 708-748-7565 • SPRING, TX, Eric Jeter, 713-353-0309 • SANTA ANA, CA, Tom Boris, Greg Cruse, Phil Cook, 714-756-0681 • PALO ALTO, CA, John Sly, Bill Cooper, 415-965-4334 • SURREY, ENGLAND, David Round, 81-686-7655 • PARIS, FRANCE, Daniel R. Bernard, 1-43-54-55-35 • MUNICH, GERMANY, Johann Bylek, 089-903-88-06 • MILAN, ITALY, Luigi Rancati, 02-7531445 • TOKYO, JAPAN, Sumio Oka, 03-502-0656 • SINGAPORE, REPUBLIC OF SINGAPORE, Anne Goh-Taylor, 734-9790 • SEOUL, KOREA, Jay G. Seo, 776-2096

CIRCLE NO. 68

COMPUTER DESIGN

A PennWell Publication

Single-chip decoder PLDs give users freedom of choice

Fast enough for systems with clock rates of up to 50 MHz, the 12-input, 8-output CY7B336, CY7B337, CY7B338, and CY7B339 BiCMOS programmable logic devices from Cypress Semiconductor let users tailor the products' benefits to their needs. With the PLDs, designers can either use 40-MHz-or-faster processors, or specify slower, less-expensive SRAMs for designs that use 33-MHz processors.

The 336 and 337 have registered inputs that make them compatible with RISC processors such as the MIPS R3000, the AMD 29000 and some Sparc implementations, all of which assert addresses for a short period around clock edges. The 338 and 339 have output latches to accommodate CISC processors such as the 80486, which does not issue an address with every clock and which removes addresses and data before the end of clock cycles. Users can also select the 6-ns 336 and 338, in which product terms are limited to two per output for speed, or the 7-ns 337 and 339, which have four prod-

uct terms per output for implementing an addressing scheme with bank select and/or byte write control. The 338 is faster than, but similar in architecture to, Intel's CMOS 85C508 single-chip decoder.

Users pick the benefit

Designers can use the new parts either to significantly reduce system memory cost, or to use faster processors with faster memory, according to Cypress senior product marketing engineer, Robert Moore. "The fast decoders allow designers to make that trade-off between dollars and speed."

Cypress accomplishes that speed by actually implementing ECL circuitry, says Moore. The fuse-programmable BiCMOS features an ECL speed path, BiCMOS-level conversion circuitry and CMOS for control. Cypress uses the same BiCMOS to manufacture its 7.5-ns PAL22V10C-7.

The dozen input registers of the 6-ns 336 and dozen inputs of the 6-ns 338 capture data at the rising

edge of the clock signal and forward information to a 24x16 programmable array. Processed data from the array is available to external logic via the eight output pins. One of the two product terms sums products from the array while the other controls tristate output buffers. All outputs of the 7-ns 337 and 339, which have 24x32 programmable arrays, can be tristated. Each of the four parts has an asynchronous output enable, power-on-reset and more than 2,001-V input protection from electrostatic discharge.

Packages for the Cypress decoders include 28-pin, 300-mil plastic and ceramic DIPs, SOJs, LCCs, and PLCCs. The 336 and 338 cost \$16.35 (100s) and the 337 and 339 cost \$14.30 (100s). Production quantities of the 338 and 339 are available now; samples of the 336 and 337 are available now, with production quantities expected next quarter.

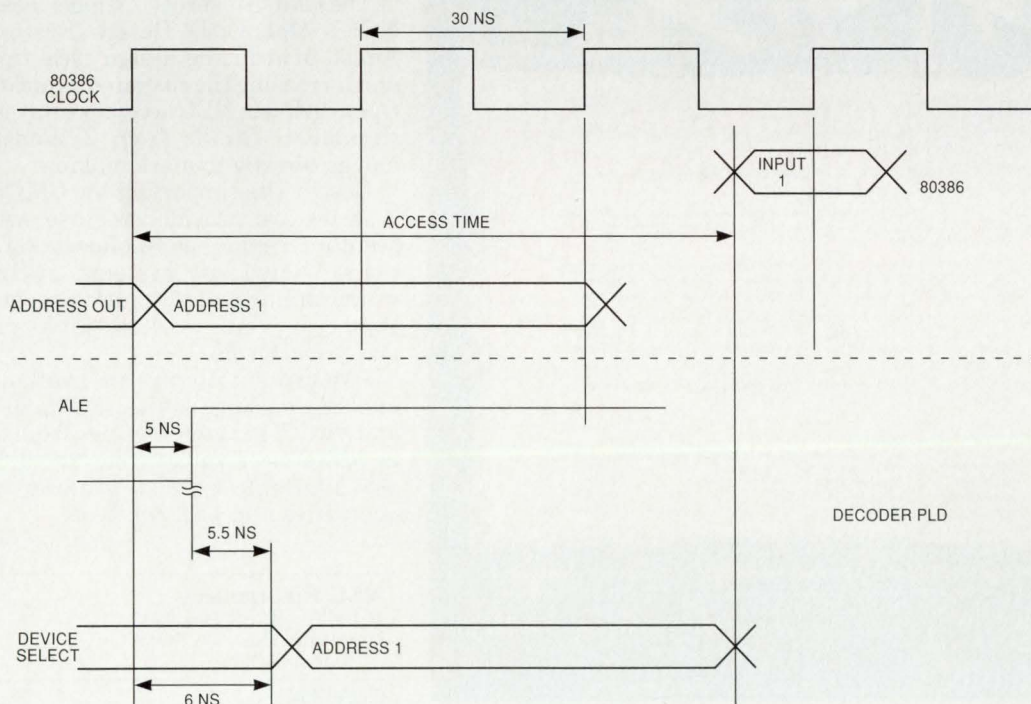
—Barbara Tuck

Cypress Semiconductor

3901 N First St
San Jose, CA 95134-1599
(408) 943-2600

Circle 355

33-MHZ PIPELINED ADDRESSING WITH DECODER PLDs



Output latches in the 6-ns Cypress CY7B338 enable it to decode addresses in a CISC-based system, such as this 33-MHz 80386. The programmable logic device decodes the address data and maintains it on the bus until the next data screen. The effect is to allow cache design based on 45-ns SRAMs, instead of the more-expensive 35-ns devices required without the decoder PLD.

INTEGRATED CIRCUITS

High-speed CMOS gate arrays integrate 150,000 gates

The CMOS-7 series of CMOS gate arrays from NEC Electronics offers up to 150,000 usable gates. At 0.3 ns for a power NAND gate, the devices also push the envelope of ASIC

speeds. The CMOS-7's mix of density and performance is targeted to meet the integration and speed requirements of ASIC implementations in superminicomputers, high-end work-

stations, telecommunications systems, and instrumentation.

The devices feature a sea-of-gates architecture that provides gate complexities from 60,500 to 250,000 equivalent gates using four master-slice options. Power dissipation of the devices is 6.5-mW/gate. The parts have I/O pin counts from 220 to 488.

The CMOS-7 devices use the same cell library as NEC's previous generation ASICs, simplifying migration from the older 1.0- μ m CMOS-6 series. More than 300 macrocells are available, including ROM and RAM macroblocks with built-in self-test circuitry.

Built with NEC's 0.8- μ m channel-less architecture, CMOS-7 products use a self-aligned twin-well technology. The gate array chips are divided into I/O and internal cell areas. To isolate the internal cells from high-energy input signals, the I/O cell area contains input and output buffers. The internal cell area is an array of basic cells, each composed of two p-channel MOS transistors and two n-channel MOS transistors, as well as four additional n-channel MOS transistors for compact RAM design. These transistors are sized to provide an optimum ratio of speed to silicon area.

The CMOS-7 series is supported by NEC's OpenCAD Design System. Aimed at reducing design cycle time and increasing the customer's control, OpenCAD lets NEC accept postlayout simulation results from customers and go directly to mask making.

Design kits supporting the CMOS-7 series are provided for use with Mentor Graphics on Apollo workstations; Valid Logic Systems on Sun workstations and PC platforms; and Dazix on Sun workstations and Daisy platforms.

CMOS-7 gate arrays are available in three package styles: PGA, QFP and PLCC. Pin counts range from 68 to 528. Prices range from 2¢ to 5¢ per available gate depending on quantities and package type.

—Jeffrey Child

THE PERFECT STRATEGY FOR ANALOG & DIGITAL PCB DESIGN



- ☐ YOU want powerful, automated analog design features
- ☐ YOU use power planes
- ☐ YOU want lots of other automated features
- ☐ YOU want an affordable upgrade path
- ☐ And don't forget schematic capture...
- ☐ YOU want to find out more
- ☐ ULTIboard's new Version 4.1 let's you use curved or any angle traces. Also, you specify automatic fill patterns for copper areas of any shape. Polygons are assigned to nets while traces of other nets are automatically ploughed through filled areas.
- ☐ With ULTIboard, power and ground planes with thermal relief pads are created automatically.
- ☐ Real-time DRC, trace shove, reroute-while-move, round tracing and board outlines, .DXF output, automatic component renumbering, and more are standard in all ULTIboard systems.
- ☐ ULTIboard's got a smooth upgrade path with a system in every price range, running under DOS or extended memory. Choose a system to design a small board of 50 equivalent IC's, up to our 32-bit 386 version with unlimited design capabilities.
- ☐ ULTIcap schematic capture featuring automatic guided wiring, automatic junctions, auto rewire after block moves, and on-line symbol creation are just some of ULTIcap's easy-to-use automated features. Or, use your own schematic package with ULTIboard's backannotation.
- ☐ Call ULTIimate Technology today for a free demo disk, and the name of the dealer nearest you.

ULTIboard Professional 386 is a true 32 bit Design System: approx. 2x faster than 16 bit versions.

Select your ULTIboard system from this table:

Model	Price	Nr. of 16 pins equiv. IC's	Memory required
Entry Level	\$ 995	35 - 50	640 K
Advanced Level	\$ 2,475	140 - 200	640 K + 1 Mb
Professional 286	\$ 5,950	unlimited	640 K + 2 Mb ¹
Professional 386	\$ 7,900	unlimited	640 K + 2 Mb ¹

USA/Canada Headquarters
ULTIimate Technology Corp.
269 Mt. Hermon Road,
Suite 105
Scotts Valley, CA 95066
Tel. (408) 439-8944
Fax (408) 439-8966

UK/Ireland Sales Office
ULTIimate Technology Ltd.
1 Mars House Gallewa Park
Aldermaston
Berkshire RG7 4QW
Tel. (0734) 812030
Tel. (0734) 815323

Germany Sales Office
ULTIimate Technology
Vaihinger Straße 12
D-7032 Sindelfingen
Tel. (07031) 876028
Fax (07031) 85915

Europe Intl. Headquarters
ULTIimate Technology bv
Energijstraat 36
1411 AT Naarden, Netherlands
Tel. (+31) 2159-44424
Fax (+31) 2159-43345
Telex. 73415

NEC Electronics
401 Ellis St, PO Box 7241
Mountain View, CA 94039
(415) 960-6000

Circle 356

OEM PRODUCT UPDATE

Canon Laser Beam Printer Family

The Canon family of OEM Laser Beam Printer Engines comprises the largest installed base in the laser printer market. This success has been built on Canon's well-documented reputation for reliability and low maintenance, innovation and high quality images.

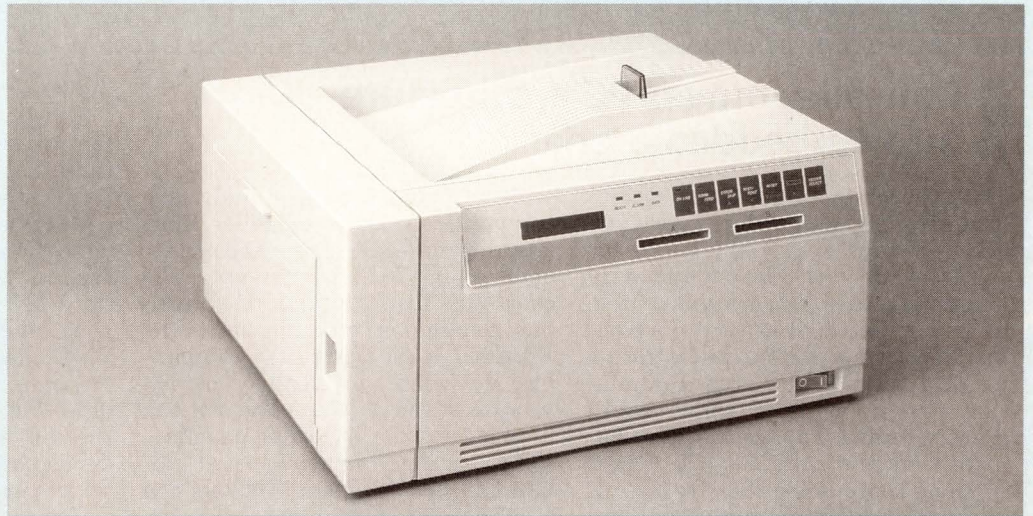
There's a Canon engine for every OEM application. Personal printers. Desktop publishing and printing. Spreadsheets. Engineering. Graphics production. CAD/CAM. A unique feature of Canon's table top models is the patented EP cartridge system. Housing virtually all consumables, the EP cartridge makes user maintenance simple.

As an OEM associated with Canon, you'll work with a leader in laser technology and engine reliability. You'll get the product and technical support you need to serve existing customers and respond to emerging market opportunities.

For more information, call **1-800-323-0766**. Or write to Canon USA, Inc., OEM Operations, Printer Division, One Canon Plaza, Lake Success, NY 11042-1113.

Product specifications subject to change without notice.

Canon[®]
OEM Operations
Printer Division
CIRCLE NO. 77



LBP-LX Laser Beam Printer Engine

A compact, affordable printer engine ideal for desktop applications. Utilizes the disposable EP-L cartridge. Available in both Video (external OEM controller) and PCB (internal OEM controller) models.

Monthly prints: 750
 Resolution: 300/400 dpi
 Print Speed (PPM): 4
 Dimensions: 16.7"W x 14.1"D x 7.6"H

LBP-SX



The most popular laser beam printer in the world. Clamshell top cover permits easy access to paper path and disposable EP-S image cartridge. Available in Video and PCB models.

Monthly prints: 5000
 Resolution: 300/400 dpi
 Print speed (PPM): 8
 Dimensions: 18"W x 19.5"D x 9.1"H

LBP-TX and LBP-RX



Hard-working laser beam printers featuring expanded paper handling. The RX model offers duplex capability. Dual cassettes hold up to 400 sheets and two types of paper. EP-S cartridge in all versions. Available in Video and PCB models.

Monthly prints: 5000
 Resolution: 300/400 dpi
 Print speed (PPM):
 TX Simplex 8
 RX Duplex 7 (impressions)
 Dimensions: TX 18"W x 19.5"D x 12.5"H
 RX 18"W x 25.0"D x 12.5"H

LBP-20



A heavy-duty laser beam printer for large-format printing. Modular design allows multiple product configurations.

Monthly prints: 30,000
 Resolution: 300/400/480 dpi
 Print speed (PPM):
 Simplex: Letter 20
 11" x 17" 10
 Duplex: Letter 14 (impressions)
 11" x 17" 8 (impressions)
 Dimensions: 29"W x 24"D x 20"H

LBP-DX



Our largest-format laser beam printer. Outputs high-quality photographs, halftones and line art prints on vellum or paper. Ideal for engineering and graphics production. Handles 500-foot rolls of 24" wide paper or cut sheet sizes up to D (24" x 36").

Monthly prints: 5000
 Resolution: 400/508 dpi
 Print speed (PPM):
 D size (24" x 36") 3
 C size (18" x 24") 5
 Dimensions: 30"W x 39"D x 46"H

Controller moves PC architecture into embedded arena

The PC architecture is evolving into a control computer for embedded and real-time systems, not just for the Intel 80286 or 80386 found at its heart. As a result, users will be able to do a great deal of code development on standard PC-type platforms without the need for cross-compilation and debugging, which could greatly reduce application development time and cost.

Along these lines, Radisys has introduced a PC-compatible VMEbus controller, called the EPC-6, which can be used as a stand-alone control processor. The EPC-6 contains a 20-MHz 80386SX processor, an optional 387SX math coprocessor, up to 4 Mbytes of dual-ported DRAM, and 8 kbytes of battery-backed SRAM for storing critical data. It uses the ROMed version of Microsoft MS-DOS and includes a 16-kbyte instruction and data cache to increase performance for high-speed control functions. Radisys has taken advantage of the highly integrated, low-power core logic ICs that have been developed for laptop and notebook PCs to implement the architecture on a single VME card.

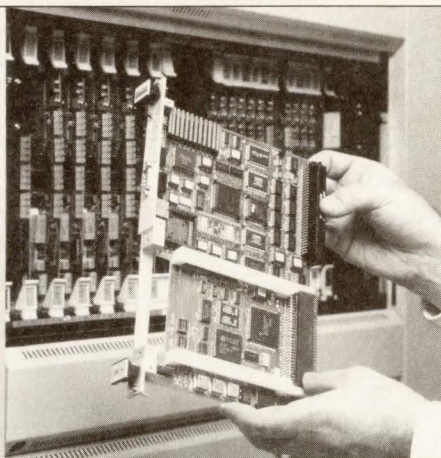
Flash memory the key

The EPC-6's 512 kbytes of flash memory for program storage, which is treated by the system as a solid-state disk drive, is key to its use in embedded applications. The drive can be formatted and downloaded with DOS-compatible files.

Most PC-based compilers generate code as relocatable .EXE files, and the disk format of the flash memory allows them to be stored and run in that format. Systems based on Intel CPUs, which use EPROMs for program storage, must first convert the code to a hex format with absolute addresses before it can be loaded into the EPROM and used by the system. The flash memory not only eliminates the need for this step, it makes it easier to dynamically download control programs and/or program changes directly from an attached PC or over a network.

The EPC-6 is implemented on a single-slot VME card. The VME in-

terface includes master and slave capabilities, slot-1 controller functionality, and generation and receipt of all seven VMEbus interrupts. The controller also contains one EXMbus expansion module slot. (The EXMbus is an electrically compatible, but more physically compact, version of the AT bus.) The slot can be used for an Ethernet interface, VGA graphics support, extra RS-232 I/O, or a modem; VMEbus can



The EPC-6 embedded controller contains a full PC-compatible architecture, including DOS in ROM, with access to VMEbus functionality.

then be used for high-speed I/O and communication with other real-time controllers.

Tailored to VME

In an embedded application, programs would normally communicate with the EXMbus via DOS and BIOS calls, as would a normal PC. For VMEbus communications, Radisys supplies a library of software tools and modules, called EPControl, to allow system configuration, debug and communication via the VME backplane. Control applications communicate with the VMEbus either directly using the run-time library communication modules or via a real-time multitasking executive that can be loaded in memory. DOS does not participate in the real-time functionality of the EPC-6; it merely loads control programs and inter-

faces with ECM modules.

EPControl programs include configuration and set-up routines to establish I/O ports and format the flash solid-state disk. Debug software consists of a command line diagnostic program, called BusProbe, that allows the EPC-6 to manipulate the VME interface. It can read and write single addresses or blocks of VME memory, and manipulate interrupts and error signals. A standard DOS debugger gives access to the EPC-6 memory and I/O. The debug software can be invoked via a serial port or over the backplane.

The run-time software libraries can handle VMEbus interrupts, manage a VME window in local EPC-6 address space and do data transfers over the VMEbus. The libraries also support remote procedure calls (RPCs) to allow the EPC-6 to communicate in a multiprocessor environment. RPCs can take place over the VMEbus or serial I/O ports, or via Ethernet if an Ethernet card is installed in the bus slot.

The EPC-6 does not have a keyboard interface or on-board graphics display hardware. Application software development can take place in a number of ways. If the EPC-6 is being used in an environment that requires an embedded human interface, the computer supporting that interface can be used to emulate EPC-6 functions before the final code is downloaded to the EPC-6. Alternatively, a desktop PC can be used for software development up to the stage where it must be linked with the VME run-time library routines. It would then be transferred either by disk or Ethernet to an embedded PC with a human interface for final debugging and testing. The final system, however, will often contain only the EPC-6 and other VME cards that communicate via the EPControl software. Human access to such a system could then occur via serial ports or Ethernet, when needed.

The EPC-6 costs \$1,995 in single quantities and \$1,495 in OEM quantities. — Tom Williams

Radisys

19545 Von Neuman Dr
Beaverton, OR 97006
(503) 690-1229

Circle 353

COMPUTER DESIGN Card Deck Circulation Increased to 100,000 AT NO EXTRA COST

COMPUTER DESIGN has increased the distribution of its Direct Action Card Decks by 10,000 — at no extra cost to you. This totals over 100,000 design and development qualified engineers and engineering manager subscribers from COMPUTER DESIGN Magazine's newly expanded U.S. and Canadian circulation base.

**Circulation — 100,000 Design and Development Qualified Including:
71,000 Engineering Managers
29,000 Design Engineers**

Now, More Engineering Managers Than Any Other Deck!

COMPUTER DESIGN Direct Action Cards have always been top-performers for new product introductions, catalogs, literature, mailing list compilation, and lead generation. Now, with extra reach, COMPUTER DESIGN Direct Action Cards are even better. And best of all, these 10,000 new prospects are free!

1991 Direct Action Cards Schedule

Mailing Date	Insertion Order	Materials
January 1	December 3	December 4
March 1	February 1	February 4
April 1*	March 1	March 4
Surface Mount Devices Specifier Deck		
May 1	April 1	April 4
June 3*	May 1	May 3
Design & Development Tools Specifier Deck		
July 1	June 3	June 4
September 2	August 1	August 5
October 1*	September 2	September 4
Test & Measurement Tools Specifier Deck		
November 1	October 1	October 4

*Special Marketing Directed Decks with special pricing.

1991 Rates:

1x \$2,080
2x \$1,945
4x \$1,650
6x \$1,445
2nd Color:
Std add \$200
PMS add \$300

**Call for information on
1990 Rate protection
and multiple Cards Per
Pack discount.**

**For more information, production assistance,
or to place an order, call Sue Nawoichik
at 800-225-0556 or 508-392-2194
or FAX us at 508-692-0525.**

COMPUTERS AND SUBSYSTEMS

Versatile I/O processor races at 10 Mips

Recognizing the need for fast I/O processing in systems using military interconnected buses, such as the Naval Tactical Data System and the MIL-STD-1553 Multi-

plexed Avionics Bus, Antares has developed a second-generation intelligent I/O processor for VMEbus environments. Based on a bit-sliced architecture, the board executes I/O

operations at a 10-Mips rate. It can be tailored to service different I/O protocols simply by changing a piggy-back board containing bus-specific circuitry and PROMs with microinstructions set for the specific I/O protocol.

Capable of performing a variety of I/O-to-VMEbus transactions as either a VMEbus slave or master, the board makes virtually all VMEbus resources available to Antares' microengine, which is at the heart of the board. Complete microcode drivers are provided on the board to simplify integration.

If users require a MIL-STD-1553 interface, for example, the microcode driver needed to handle that protocol is already resident. They merely have to install the proper piggy-back board and to provide the board with message-passing information.

Microengine heart of board

The Antares microengine, which is built around WaferScale Integration's 2901 bit-slice processor, is made up of a 32-bit 2901 ALU, together with the 2910 microsequencer chip and microcode PROMs. The 32-bit ALU operates at a 10-MHz clock rate, resulting in the 10-Mips processing rate. A 32-bit 100-kHz real-time clock allows timing of I/O events with a 10-ms granularity. Combined with the fast PROMs, the design offers a highly programmable I/O interface path with the VMEbus interface.

All operations are controlled by microinstructions stored in 2 kbytes of fast, 64-bit-wide PROM. Each 64-bit word contains data, op-code and address information. Microinstruction pipelining is implemented to provide an additional speed boost. By always having the next instruction available, a PROM fetch cycle is eliminated.

Available now, the Antares I/O processor is offered on a single-slot 6U card. Prices start at \$3,525.

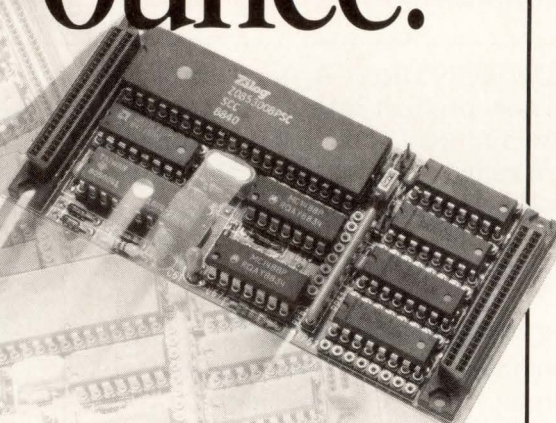
—Jeffrey Child

Antares

4025 Hancock St
San Diego, CA 92110
(619) 223-4311

Circle 358

More bounce per ounce.



Customize your I/O with IndustryPacks™ from GreenSpring

Each credit-card sized IndustryPack performs a related group of Input/Output functions. IP's snap onto carrier boards containing host bus interface and cable connections. Choose from Digital I/O, 12- and 16-bit A/D and D/A Converters, Relay, 12-bit Servo, Timers, RAM and many others, or create your own using our Design Kit.

Flexible I/O for your PC/AT, VMEbus or Mac II

Mount up to four different IP's on one VMEbus or ATbus, or up to two on one Mac II carrier board. IP's support I/O, Memory, Interrupts, DMA and battery backup with transfer rates up to 8

MB/sec. Customizing your I/O allows you to save slots and money!

The new industry standard

Take advantage of the new open industry standard to select the precise I/O you need. More than 100,000 single-slot solutions give more bounce to your VME, AT, or Macintosh system.



1204 O'Brien Drive
Menlo Park, CA 94025
(415) 327-1200 FAX (415) 327-3808

CIRCLE NO. 81

28th ACM/IEEE DESIGN AUTOMATION CONFERENCE[®] and EXHIBITION FROM GATE ARRAYS TO THE GOLDEN GATE

- Over 125 exhibitors of CAD hardware and software products.
- Over 60 exhibitor technical presentations Monday, June 17, 1991, many announcing new products.
- *Monday Exhibits Only Passes.* Free invitations available from participating companies or call toll free, 1-800-321-4573



- DA Professionals world-wide attend DAC to keep current with advancements in Design Automation.
- Seven full day tutorials Friday, June 21, 1991.
- Over 140 papers, tutorials and panel presentations.

sponsored by:



ADVANCE REGISTRATION ENDS MAY 17, 1991.

In cooperation with:



MOSCONE CENTER
June 17- 21, 1991
San Francisco, California

**ATTEND THE WORLD'S
LARGEST DESIGN AUTOMATION EVENT**

This year's conference starts Monday, June 17, 1991 !!

HOTEL RESERVATION FORM
28th Design Automation Conference
June 17 - 21, 1991

Hotel reservations will be handled by the San Francisco Convention and Visitors Bureau, on a first-come, first-served basis. The following hotels are available:

HOTEL	SINGLE	DOUBLE
— Holiday Inn Union Sq.	\$ 85.00	\$ 85.00
— King George	85.00	85.00
— Le Meridien	115.00	115.00
— Mark Hopkins	115.00	145.00
— Nikko	115.00	115.00
— Parc Fifty Five	115.00	115.00
— Ritz - Carlton	115.00	145.00
— S. F. Hilton	115.00	125.00
— S. F. Marriott	115.00	125.00
— Sheraton Palace	115.00	115.00
— Sir Frances Drake	105.00	115.00
— The Handlery	85.00	95.00
— The Raphael	83.00	96.00

Above rates honored only if your reservation is made by May 16, 1991.

Complete the form below and send to:

DAC HOUSING BUREAU
P.O. Box 5612
San Francisco, CA 94101
Fax (415) 227 - 2602

CAUTION:
Hotel reservations sent to the DAC office will be discarded!

Name _____ (first) _____ (last)
 Company _____ Mail Stop _____
 Mailing Address _____
 City _____ State _____ Zip _____
 Country _____ Telephone (____) _____
 Arrival Date _____ Time _____ AM _____ PM _____
 Departure Date _____ Time _____ AM _____ PM _____

Reservations will be confirmed by the DAC Housing Bureau and the hotel to which you are assigned. A one night deposit, payable to the appropriate hotel will be requested at that time.

VISA MASTERCARD AMERICAN EXPRESS

Number _____ Expiration Date _____

Signature _____

ADVANCE REGISTRATION FORM
28th Design Automation Conference
June 17 - 21, 1991

To register, mail your payment with this form or a copy to:

28th Design Automation Conference
c/o DAC REGISTRATION DESK
7490 Clubhouse Rd. #102
Boulder, CO 80301

For Information Only, Call (303) 530-4333 or e-mail DACINFO@DAC.COM

NO TELEPHONE REGISTRATIONS OR CREDIT CARDS ACCEPTED!

IMPORTANT - Registration Instructions

1. Full payment in U.S. Dollars MUST accompany registration. Any registration without payment WILL be discarded.
2. Advance registrations must be postmarked no later than **May 17, 1991**.
3. Register one person per form (copy this form as needed).
4. **Refund Policy:** Written requests for refunds must be received in the DAC office no later than **May 17, 1991**. Refunds are subject to a \$15.00 processing fee.
5. Make checks payable to: **28th Design Automation Conference.**

PLEASE TYPE OR PRINT CLEARLY

CAUTION:

This information will be used to print your ID badge!

Name _____ (first) _____ (last)

Company _____

Street Address _____

Mail Stop _____

City _____ State _____ Zip _____

Country _____ Telephone (____) _____

*MEMBER NO. ACM/IEEE _____

CONFERENCE REGISTRATION FEES

	Conference Only	Conference and Tutorial
Advance Registration (postmarked by May 17, 1991)		
Member IEEE/ACM	\$130.00	\$230.00
Non-Member	\$160.00	\$310.00

	Conference Only	Conference and Tutorial
At Conference Registration (after May 17, 1991)		
Member IEEE/ACM	\$160.00	\$260.00
Non-Member	\$200.00	\$350.00

Students and One-day-only registrations will be accepted AT CONFERENCE only!

*This is for individual members only. This does not apply to company memberships. If this membership number is not included, non-member fees will be charged.

Computer Design, in cooperation with Sun Microsystems, presents **A MAJOR EDIT SECTION ON S**

SPECIAL
S-BUS
ADVERTISING
SECTION

**COMPUTER
DESIGN**

Staff Written S-bus Keynote Feature

Warren Andrews
Senior Editor

**VMEbus and Multibus II
link up with Futurebus+
bringing new architectural
dimensions to the open-
bus playground.**

Whenever the term "bridging the bus" comes up, it's usually in connection with the VMEbus and Multibus II. In fact, it's a term that's used to describe the relationship between these two buses. First, because they're both open buses, where the concept of a bus is a plane of communication. Second, because they're both open buses, where the concept of a bus is a plane of communication. Third, because they're both open buses, where the concept of a bus is a plane of communication. Fourth, because they're both open buses, where the concept of a bus is a plane of communication. Fifth, because they're both open buses, where the concept of a bus is a plane of communication. Sixth, because they're both open buses, where the concept of a bus is a plane of communication. Seventh, because they're both open buses, where the concept of a bus is a plane of communication. Eighth, because they're both open buses, where the concept of a bus is a plane of communication. Ninth, because they're both open buses, where the concept of a bus is a plane of communication. Tenth, because they're both open buses, where the concept of a bus is a plane of communication.

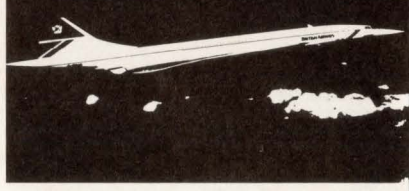


The Argument for and against, S-Bus

Perhaps a good way to view the differences between American and Japanese business strategies is to consider the games of chess and go. In chess, the object is to capture individual pieces and corner the king. In go, the object is to occupy strategic positions to control territory. The acquisition of MCA by Matsushita serves as an example of the devastating effects of a go strategy in a chess world, and today it is for the future. The first reactions in the press were that the U.S. culture was no longer that of the games probably would not block the release of films like "Drunks" or "The Untouchables." This is the judgment of a player who thinks he has just lost a rook when in fact he has lost half of his maneuvering area. The MCA acquisition, along with the earlier acquisition by Sony of CBS Records, is really about digital audio tape and high-definition TV—and even more ominous issues beyond those. The situation leaves the impression that the U.S. government and business elite is a confederation of fools—fools who treat employees like the enemy, who measure success in three...

There are several viable mezzanine buses for VME...

Imagine it's transporting data and you'll understand our new VME board.



Introducing a 68030 VME board that makes your applications take off.

When it comes to transporting a payload of people or data, there's nothing better than a 68030.

Introducing a 68030 VME board that makes your applications take off.

Introducing a 68030 VME board that makes your applications take off.

Introducing a 68030 VME board that makes your applications take off.

Introducing a 68030 VME board that makes your applications take off.

11, 1981 COMPUTER DESIGN



While the programming changes have to control the interface functions, it's also the idea behind CPU. In the lowest member of our VMEbus family, transporting thousands of data at maximum speed. Providing throughput like you've never seen in a 68030 based board. All thanks to CPU. Its unique architecture starting with a full complement of non-pipelined dual port SRAM. It's designed to provide maximum performance during dual port access. Which makes your real time applications fly.

THIS SPECIAL SECTION WILL FEATURE:

- ITS OWN COVER AND IDENTITY, IN A LIFT-OUT FORMAT
- MULTIPLE PAGES OF EDITORIAL OVERVIEW IN COOPERATION WITH SUN MICROSYSTEMS
- FULL-PAGE ADS WITH ACCOMPANYING FULL-PAGE EDITORIAL POSITIONING

EDITORIAL/ADVERTISING -BUS IN JUNE

ABOUT S-BUS

S-Bus is on its way to becoming the standard mezzanine bus for Futurebus+. Motorola has already endorsed it for its Futurebus+ products and VITA is considering it as a standard mezzanine bus for Futurebus+.

The competition is intense. There are over 130 manufacturers of S-Bus boards vying for business from the rapidly growing list of vendors building S-Bus-based systems. This translates into 400,000 S-Bus slots currently in the market and 20,000 to 30,000 new slots being added every month.

ABOUT THE S-BUS ADVERTISING SUPPLEMENT

This supplement will open with a major editorial overview that discusses the opportunities and options S-Bus provides to today's technical decision makers.

Each participant will provide **COMPUTER DESIGN** with a full-page ad and editorial copy of approximately 900 words. This copy can detail whatever opportunities, benefits and predictions you choose. A black & white photo of the author (preferably your company's President, CEO or other high-ranking individual) will be included in the piece. Participants should also provide 40 words of copy for the July/August Showcase S-Bus forum.

The advertiser's editorial copy will face its ad and provide a strong positioning statement.

- In total, a participant in the S-Bus advertising supplement receives a spread consisting of a full-page ad and an editorial positioning statement plus a 1/9th-page ad in the July-August S-Bus Showcase forums
- Reservations deadline is May 1, 1991
- Editorial and ad material by May 6, 1991
- Positioning of advertising will be at the discretion of **COMPUTER DESIGN**, with priority given to early commitments
- The back cover (in 4/C) will be available to a participant for an additional \$5,000

ABOUT COMPUTER DESIGN

- Covers today's microprocessor/computer-based electronics OEM
- Provides design directions, options and choices...with exclusive "Why-to" editorial
- Serves 100,000 Design and Development Engineers and Engineering Managers—all 100% design and development qualified
- Reaches 71,000 Engineering Managers—more than any other electronics publication
- *And it's the fastest growing publication in the market!*

COMPUTER DESIGN reaches subscribers involved in:*

• Super Microcomputers/ Workstations	41,583
• System Boards	84,066
• Integrated Circuits	77,922
• Design and Development Equipment including CAE/CAD/CAM Workstations	85,312
• Software including CAE/CAD/CAM and Embedded Systems	88,949

* JUNE, 1990 BPA

Each advertiser will appear with its own full-page ad and full-page positioning editorial.

Plus:

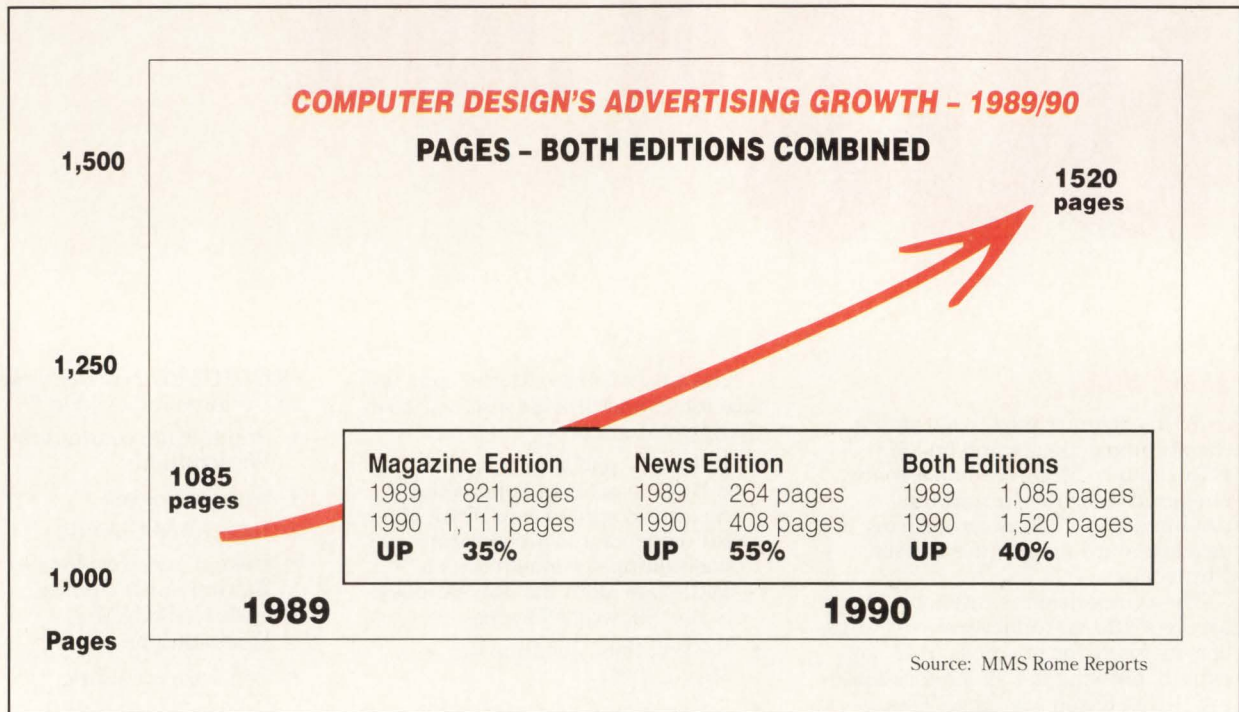
- Two free S-Bus forum showcase ads—one in July and one in August
- All 4-color
- Free copy editing and layout of positioning editorial

A total value of more than \$18,000. **All at a single inclusive price of \$8,000.**

COMPUTER DESIGN *Technology and Design Directions*

More and more...

Advertisers are investing in Computer Design's unique readership



Our Magazine Edition's 70% engineering management, 100% design & development qualified circulation combined with our News Edition's 100% Time-To-Market management circulation is causing more and more advertisers to take a new look at where electronics OEM marketers are placing their ad dollars. In these leaner, tougher times, they are turning to COMPUTER DESIGN to deliver their message, promote their products and boost their sales to today's computer/microprocessor-based OEMs.

Delivering Today's Electronics OEM

PENNWELL PUBLISHING COMPANY • ONE TECHNOLOGY PARK DRIVE • PO BOX 990 • WESTFORD, MA 01886 • 508-692-0700
For more information, contact any of us ...

PUBLISHER: David L. Allen, 508-392-2111 • ASSOCIATE PUBLISHER: Tim L. Tobeck, 516-883-8815 • SALES OFFICES: PORT WASHINGTON, NY, Eleanor Hobbs, 516-883-8815 • WESTFORD, MA, Tim Pritchard, 508-392-2217 • MATTESON, IL, George Mannion, 708-748-7565 • SPRING, TX, Eric Jeter, 713-353-0309 • SANTA ANA, CA, Tom Boris, Greg Cruse, Phil Cook, 714-756-0681 • PALO ALTO, CA, John Sly, Bill Cooper, 415-965-4334 • SURREY, ENGLAND, David Round, 81-686-7655 • PARIS, FRANCE, Daniel R. Bernard, 1-43-54-55-35 • MUNICH, GERMANY, Johann Bylek, 089-903-88-06 • MILAN, ITALY, Luigi Rancati, 02-7531445 • TOKYO, JAPAN, Sumio Oka, 03-502-0656 • SINGAPORE, REPUBLIC OF SINGAPORE, Anne Goh-Taylor, 734-9790 • SEOUL, KOREA, Jay G. Seo, 776-2096

COMPUTER DESIGN

A PennWell Publication

CIRCLE NO. 83

EMPLOYMENT OPPORTUNITIES, OUTPLACEMENT AND POSITIONS WANTED

Recruitment Advertising Managers

Eastern U.S.

Sue Nawoichik (508) 392-2194

Western U.S.

Tom Murphy (213) 372-2744

CAREER CONNECTIONS

Closing Dates for upcoming magazine issues

Issue	Closing dates
June	May 3
July	June 3
August	July 3

POSITIONS WANTED

POSITIONS WANTED ADS

Free 1" ad to subscribers seeking full-time employment. Just include 50 words of copy and your subscription label. We'll run your ad in 2 consecutive issues.

Available to non-subscribers or consultants/companies at \$125 per column inch. Mail your position wanted ad to:

COMPUTER DESIGN

Positions Wanted
One Technology Park Dr
PO Box 990
Westford, MA 01886

LEADER IN TRANSFER OF PRODUCTS FROM ENGINEERING TO MANUFACTURING. Successful background for 10 years in Manufacturing technologies for electro-mechanical products in commercial and military markets. Job responsibilities have included Senior Engineer, Production Manager, New Product Transition Manager, Manufacturing Engineering Manager. Willing to relocate. Call Connie at (714) 525-9220 or write to 211 S. State College St. #278, Anaheim, CA 92806.

Project Manager/MIS Management: 15+ years MIS/Software (Mfg) implementation and management experience. Desires progressive company offering new challenges and growth opportunities. IBM and HP hardware/software. P.O. Box 870775, New Orleans, LA 70187 (504) 649-0485.

Project or R&D Engineer, 30 years experience from initial concept to product support for electro-mechanical and electro-optical systems. Aircraft instruments, air data computers and flight data recorders. Specializing in transducers for the above systems. Charles A. Liucci (201) 569-8641.

EMBEDDED SOFTWARE DEVELOPMENT - Can provide software (assembler, C), simulator, programmer, and design assistance for 68XXX series. 16 years software development including real-time, diagnostics, and embedded systems, mainframe and language variety. Nick Werle, 86 Saddle Mt. Rd, Co. Springs, CO 80919 (719) 550-4253

SALES MGMT/TECHNICAL MARKETING: Over 20 years experience in high tech electronics specializing in selling components, sub-assemblies, and sub-systems to OEM Computer, Peripheral, Data Communications, LAN, Process Control and Telecommunications industries including Military, Industrial, and Commercial manufacturers. Experience includes carrying a bag, Key Accounts Manager, Regional Manager, and Marketing Manager working with direct inside/outside sales and Mgr Reps. With Engineering degrees, MBA and proven track record, focused on people, planning, and results while exceeding customer expectations. Would like to run or open your NE office as Regional or East Cost Mgr. If you are ready to grow contact: Bill Elswick (603) 926-8044.

ADP/MIS/PROJECT MANAGER. Extensive mainframe computer software development, operations managerial experience in business and technical environments. Results-oriented. Effective leadership, team-building, communicative, and problem solving skills. Maintains excellent ADP staff-client relationships. MA/BS/AAS ADP degrees. Professionally certified. Security clearance. Relocatable. For resume, send requirements to: Mgr/CD; 5464 Alteza Drive; Colorado Springs, CO 80917

PURCHASING MANAGER, 15+ years in purchasing for electrical/electronic manufacturing environments. Specializing in R&D, design support, and troubleshooting. Main thrust is efficiency, and profitability, and inventory management. Also has capability for consulting and off site procurement. Northwest Chicago and suburban area. Call (708) 541-4164 eve. and (312) 539-3373 days. Resume on request.

HARDWARE ENGINEER, 7 years experience as a field, test, integration and, for the last 3 years, design engineer on digital devices, boards and systems. Design experience with ASICs and gate arrays in addition to VLSI and MSI on parallel processing architectures. Familiar with most CAD tools on market, Mentor, Orcad, etc. I'm a motivated team player who needs a challenge. Resume on request and willing to relocate except the southwest. Call Frank at (301) 730-1590.

HARDWARE/SOFTWARE SYSTEMS ENGINEER; BSEE +29 years broad experience -DC to RF, Analog, Digital, Microprocessors, EO, ATE, design & test, specification writing/BASIC, ATLAS, FORTRAN & C; MIL-STD-2167A; 1750A, VAX/VMS, HP1000 & HP9000. Commercial, military & aerospace products. West/East coasts. H. Thomas; 5133 Laurette Street, Torrance, CA 90503. (213) 316-5322.

Software/Hardware Design Engineer. Six years of software/firmware design experience in assembly and C using Intel, Motorola, and Zilog processors. 8 years of hardware design experience, including Programmable logic design. Considerable amount of real-time systems experience - both hardware and software/firmware. Relocation acceptable. Contact: Jody Weber, 2048 S. 327th Lane #FF104, Federal Way, WA 98003. (206) 874-5948.

MANAGER, DIRECTOR OR VP OF ENGINEERING. 19 years of experience in electro-mechanical products and machine design and development. Management, Development, Design and hands on experience with machine, inspection, fabrication, plastic and woodworking shop equipment, fixtures, tools, molds, etc. Plus plant startup. Will relocate. Call Dan (708) 584-8555.

SALES ENGINEER or SALES MANAGER - demonstrated success with high-tech components, equipment, systems, datacom/telecom, networks, services. Distribution and direct sales experience in 15 Southeastern states, calling on management, engineering, specifiers, purchasing. BS-degree. Strong "hands-on" technical training/experience. Peter Alexander, P.O. Box 957111, Duluth, GA 30136. or call (404) 945-6950 (Atlanta).

SENIOR QA/TEST ENGINEER with over 20 years in the computer industry is seeking position that would benefit from over 6 years of excellent experience in all aspects of QA/Testing. Mil-Std 2167A/2168 and all related DID's and related documentation development. Wish to stay in the St. Louis area. Please call and leave message for resume (314) 921-8066.

POSITIONS WANTED

Documentation: editing/writing, inter-area ms-to-bound book liaison, productivity/QC inroads maven and implementation; walk on eggs and get things done. Remove documentation-details aggravation and side-tracking delays from higher-salaried programmers and system analysts responsibility. Thoroughly grounded (25 yr) in hard sciences publications practices and procedures. Supportive. Paul T. Johnson, (212) 925-6983, (914) 647-7016.

CONTRACT MANAGEMENT/ACQUISITION MANAGEMENT/LOGISTICS Professional with 20 years experience as US Government contracting Officer and senior logistician. B.S. and J.D. Degrees. Technical/Military training. Familiar with Aerospace, Defense, and Telecommunications industries. Seeks challenging position. Will relocate. Major Charles W. Hughes, 10072 Roselee Drive, Garden Grove, CA 92640 (714) 537-8961.

SENIOR HARDWARE/SOFTWARE ENGINEER/SCIENTIST, PhDEE, MSEE, BSM +25 years experience in R&D and Design, D&A circuits, Microprocessor, DSP, A/D, D/A, Parallel Processing, Control, Communications, Radar, Ultrasonic, Voice, Image. Has new great product idea for PC market. Looking for R&D challenging position or investors. W. Klimkiewicz, 360 McBath St., State College, PA 16801, Call Voitek: (814) 237-1118/234-1149.

SR. SOFTWARE ENGINEER, BS/Comp. Sci., 14 years experience. Full life cycle development. Diagnostics, networks, multi-processors, systems, applications, User interface. C, C++, Assembler, PASCAL, and several others. Intel & Motorola families familiarity. UNIX, Macintosh, IBM, DEC. I. Rabinowitz, POB 1379, L.G., CA, 95031-1379. Please call (408) 354-9991.

HARDWARE/SOFTWARE DESIGN ENGINEER. 10+ years experience. Digital/Analog/RF circuit design. Have worked on projects involving micros, electro-optical, communications, robotics, device drivers, and data collection systems. Software: assembler, Pascal, "C", Fort, PostScript, Occam and others. Lots of IBM PCs and DOS experience. Tom (313) 665-7366.

AVIONIC SYSTEMS INTEGRATION. Hands on Senior Engineer 9+ years experience. FLIR/TV, Digital/Analog, DSP, Control Systems/Tracker, Optics and Microprocessor Circuit design and test. M68000 assembly, MS-DOS, UNIX, Most high level languages. RS232, RS422, RS170, IEEE488 and MIL-STD-1553B. BSEE. Will travel/relocate. Chris, 2981 Black Horse Dr, Ontario, CA 91761 (714) 947-0463.

Mfg. Engr. Surface Mount Assm. Desire N. Cal. but will consider offer. Dave Hughes (408) 266-2823 early A.M.

Hardware/Software Engineer: Experienced with analog and digital hardware, as well as software (assembly for many uPs, BASIC, and C under UNIX and MSDOS). Very proficient in documenting HW/SW projects using a variety of packages, including "troff". Self-taught hobbyist with degree to back it up, management experience, and strong interpersonal skills. Prefers NY Metro area. Call Gene at (718) 894-9139

HELP WANTED

SOFTWARE CONSULTANT - Consulting with faculty on the use of hardware (IBM 3090, VAX 8650), operating systems (CMS, VMS), and software (programming languages and statistical packages); electronic mail system (office vision); conduct special studies and investigations pertaining to development of new information systems to meet current and projected needs; Providing support for remote communications of PC's with the central facility, including data uploads and downloads.

37 1/2 hours per week, 8:30 a.m. to 5:00 p.m. with 1 hr. breaks, \$22,500 annual salary. No overtime. BBA-major; Computer Information Systems. 6 months experience as a programmer. Job Service of Florida, 701 S.W. 27th Ave., Room 15, Miami, FL 33135 Job Order #FL0415873.

Generate cost-effective sales leads with Computer Design's Showcase Advertising

For as little as \$840 for each 1/9 page ad, your advertising message reaches over 100,000 computer systems designers, and developers —each a key decision maker responsible for purchasing your products.

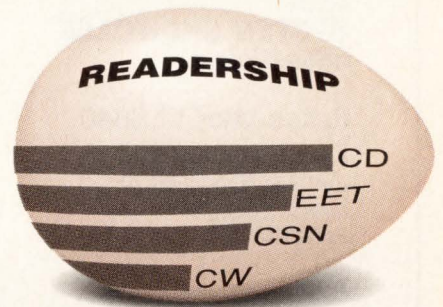
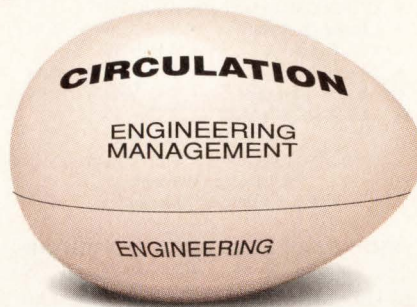
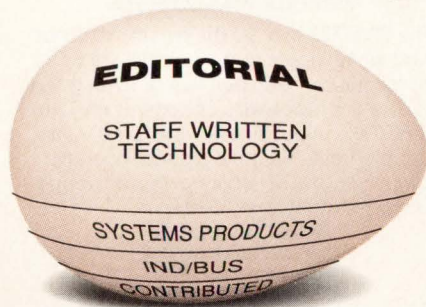
Just send a glossy photo and approximately 60 words of copy. We'll do the rest...with no production charges. If no photo, 100 words of copy accepted. Two and four color available at nominal charge. Closing date: First day of previous month.

For more information or to reserve space: **Call Sue Nawoichik at 800-225-0556
or in Massachusetts at 508-392-2194**

COMPUTER DESIGN
One Technology Park Drive
P O Box 990
Westford, MA 01886

COMPUTER DESIGN

We believe the eggs come first.



Delivering value to our advertisers begins with editorial, circulation and readership.

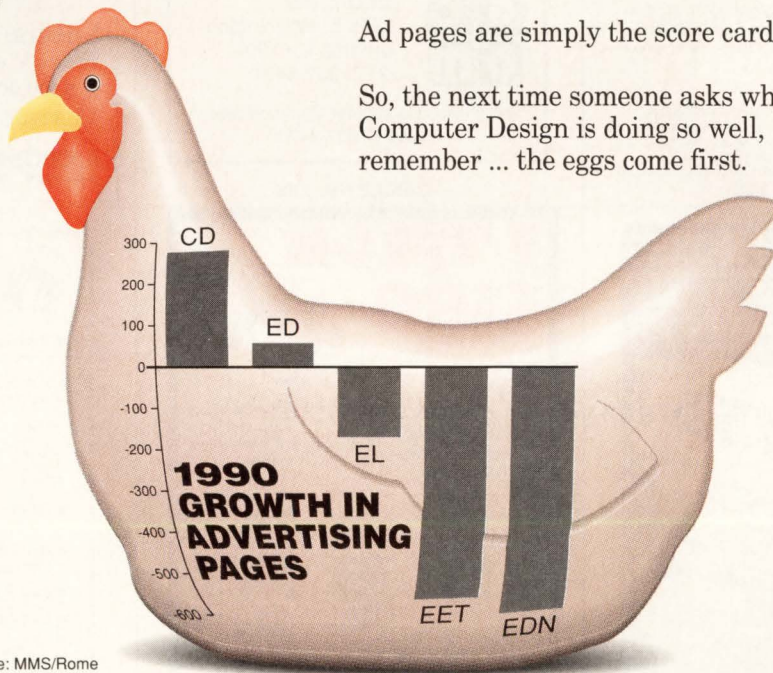
“Why-to” editorial — strong, technology editorial. 65% of our editorial is technology driven. Design choices, options and directions, staff written, multi-vendor, multi-product driven — essential! Essential, to our 71% Engineering Management circulation — “why-to” editorial is exactly what’s needed by Design & Development Engineering Managers

making the tough decisions on design tradeoffs and directions.

Readership — That’s why Computer Design wins readership among such important audiences as those senior technical trend setters attending meetings like the Invitational Computer Conferences. Among all attendees registering at all 1989 ICC conferences Computer Design was #1.

Ad pages are simply the score card.

So, the next time someone asks why Computer Design is doing so well, remember ... the eggs come first.



Ad pages source: MMS/Rome

PENNWELL PUBLISHING COMPANY • ONE TECHNOLOGY PARK DRIVE, WESTFORD, MA, 01886 • (508) 692-0700

CIRCLE NO. 84

**COMPUTER
DESIGN**

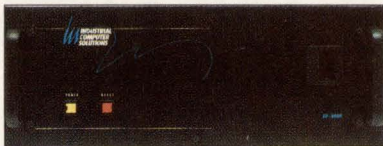
A PennWell Publication

SYSTEM SHOWCASE

Reach over 100,000 qualified engineers and engineering managers with **SYSTEM SHOWCASE** advertising.

Rates start at \$840

For more information call Sue Nawoichik at 800-225-0556 or 508-392-2194



Industrial 386sx

\$3200.00

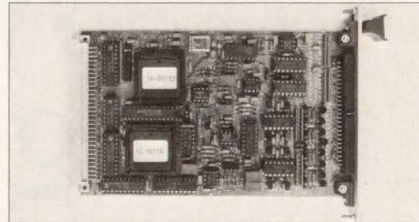
- 19" Rack Mountable
- Passive Backplane
- VGA Graphics
- 1.44Mb Floppy
- 2 Serial/1 Parallel
- Intel 80386sx-16MHz
- 1Mb RAM
- 14 Expansion Slots
- 44Mb HD
- 270w Power Supply
- One-Year Warranty

Custom Cases/Graphics Other Systems Available
Distributors Welcome
Call For Complete Information

Industrial Computer Solutions

236 Bergen Blvd., West Patterson, NJ 07424 (201) 256-7272 Fax (201) 256-1126

CIRCLE NO. 166



VMEbus ANALOG I/O.

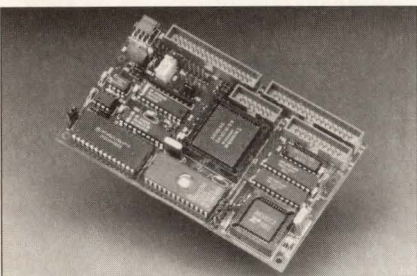
The RVE788 is a 3U (halfwidth) VMEbus card w/ 16 inputs and 8 outputs, all w/ 12 bit resolution. Replace two or even three of our competitors' cards with one RVE788. Input filters, res. prog. gain, sample-hold, variable speed operation, low power CMOS, optional current loops. Throughput rates to 33 kHz.

ROBOTROL CORP.

925 W. San Martin Ave.
San Martin CA 95046
(408) 683-2000

CIRCLE NO. 167

A 3"x5" Single Board Computer with FREE C Source Utilities!



30-Day Money-Back Guarantee!

- 8051 type architecture
- Siemens 80C535
- 40 digital I/O lines
- 2 RS232 ports and 1 RS485 port
- 8-Bit A/D converter with 8 multiplexed inputs
- Power supervisory circuits
- 8KB or 32KB RAM/32KB or 64KB EPROM
- 5x4 keypad encoder
- On board +5V regulation
- Optional real time clock
- Over 40 FR EE C source utilities

TRI-L.DATASYSTEMS, INC.
94-871 Farrington Hwy, 2nd Fl
Waipahu, Hawaii USA 96797
Phone: (808) 671-5133
Call Toll Free: 1-800-245-8745

CIRCLE NO. 168

X.25 SDLC
QLLC HDLC
ADCCP PAD

- C source code
- ROM-able
- Full porting provided
- No OS required



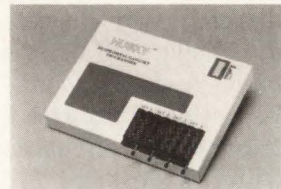
GCOM, Inc.
1776 E. Washington
Urbana, IL 61801
(217) 337-4471

Specialists in Computer Communications
FAX 217-337-4470

CIRCLE NO. 169

Program Your Chips

In Sets of 4 for \$495.00



Special offer Now Includes:
Free UV eraser, CUPL starter Kit and a \$300.00 Rebate with the PDT-1 Universal Programmer System\Kit.

LOGICAL DEVICES, INC. 1-800-331-7766
CIRCLE NO. 170

COAX SWITCH BOXES

A new series of modular low-frequency manual switches for voice, video and data applications. Non-constant impedance switches designed for use at frequencies up to 15 MHz. Switch action is "break-before-make" with an extremely low contact resistance. Case is fabricated of heavy gauge steel with a blue enameled finish and accented by white imprinting.



- Choice of Toggle or Rotary
- Isolated or Grounded Shields
- Optional Built-In Terminators
- One, 2 or 4 Pole, 2, 3, or 4 Pos.
- Custom Switch Boxes Considered
- Data Transfer Switches DC to 15MHz
- BNC, TNC, "F" or Twinax Connectors
- Compact Cases, Rack Panels Available

AGENTS WANTED

LCOM® 1755 Osgood St., N. Andover, MA 01845
Inquiries 508 682-6936 FAX 508 689-9484
Toll Free Ordering 800 343-1455

CIRCLE NO. 171

E/EPROM \$180

Buy your E/EPROM programmer from a company with over 12 years experience in providing both hardware and software tools.

Order today, call 800-448-8500

AVOCET SYSTEMS, INC.

120 Union St., Rockport, ME 04856
Outside US 207-236-9055 • FAX 207-236-6713

CIRCLE NO. 172

- Expert technical support
- HEX file utilities included
- Supports EPROM and EEPROMs to 32 pins
- NMOS and CMOS devices to 1 MBit
- 4, 8, and 16 socket models available
- IBM PC/XT/AT/386 compatible
- 1 year warranty



CROSS-32 V2.0 META ASSEMBLER

- Table based absolute macro cross-assembler using manufacturer's assembly mnemonics.
- Includes manual and MS-DOS assembler disk with tables for ALL of the following processors:

16C5X	64180	6801	8048	H8/300	Z8
37700	6502	6805	8051	H8/500	Z80
50740	65816	6809	8085	TMS320	Z180
78C10	COP400	6811	8086	TMS340	Z280
SUPER8	COP800	68000	8096	TMS370	MORE...

- Users can create tables for other processors or ask us, we have many more!
- Generates listing, symbol table and binary, Intel, and Motorola hexcode.
- Free worldwide airmail shipping & handling.
- Canadian residents please add 7% GST

US \$199.00 CN \$239.00

UNIVERSAL CROSS-ASSEMBLERS
P.O. Box 6158, Saint John, N.B., E2L 4R6
Canada Voice/Fax: (506) 847-0681



CIRCLE NO. 173

Multibus II Parallel System Bus Analyzer

PSBA-100 A productivity enhancement tool for the system integrator, field service engineer, software, and hardware engineer.

- Stand-alone, single board computer
- 6U form factor, installs in a single slot
- Built-in, terminal-based user interface
- Supports all four address spaces
- Data capture based on Multibus II protocol
- Fully programmable filter logic uses templates based on Multibus II protocol
- Filter logic supports 16 trigger levels

Multibus II is a trademark of Intel Corp.

PRC

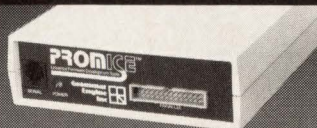
PRC Inc.
1410 Wall Street
Bellevue, NE 68005

For more information and free Demo Disk, Call **(402) 293-3900**

New Features!

CIRCLE NO. 174

A STEP BEYOND.



PROMICE takes ROM emulation a step beyond. It's an affordable, multi-operational development tool with:

- on board intelligence
- modular design
- source level debugging
- future expandability

PROMICE. The Firmware Development System of Tomorrow...

Grammar Engine Inc

3014 Morse Road
Columbus, Ohio 43231
614/471-1113
FAX 614/475-6671
101 Cherry Street
San Carlos, California 94070
415/595-2252

CIRCLE NO. 175

For METALWORKING FLUIDS, QUENCHANTS, PLATING BATHS, etc.

The DYNATROL™ System is designed for measurement and/or control of density, specific gravity, percent solids, and percent concentration of METALWORKING FLUIDS,

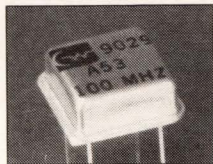


QUENCHANTS, PLATING BATHS, ACIDS, CAUSTICS, SLURRIES, etc. Response is immediate and continuous. Rugged, accurate, and easy-to-install on-line sensing cell has no moving parts and maintains long term stability. For more information, request Bulletin J-67DA.

AUTOMATION PRODUCTS, INC.

3030 Max Roy Street Houston, TX 77008 USA
Toll Free (800) 231-2062 Fax: (713) 869-7332

CIRCLE NO. 176



Reduced size 100 MHz Clock Oscillator

Connor-Winfield Corp. announces literature on a new line of High Speed 8-pin DIP oscillators. The

A53 Series line of CMOS logic clock oscillators covers the high frequency range of 50-120 MHz. Literature for a 14-pin version (ACS3) with frequencies to 200 MHz is also available. The A53, 8-pin model will soon be available in a .48" square ceramic surface mount package. Contact Barney 111 for details. Additional specifications listed below:

Model : A53
Package : 8-pin DIP
Duty Cycle: 50/50 +/- 2%
R/F Times : 2-3 nS typical

Connor-Winfield Corporation
1865 Selmarten Road
Aurora, IL 60505
PH: (708) 851-4722 FAX: (708) 851-5040
CIRCLE NO. 177



For memory protection: two fierce competitors!

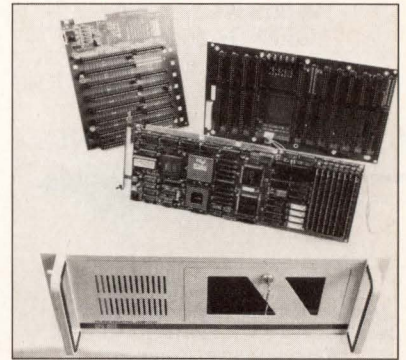
For memory protection, NiCd rechargeables and lithium primary cells go head-to-head. Varta's unique mass-plate NiCd cell construction provides the longest time between charges, can be trickle charged continuously and lasts 500-1,000 full-charge cycles over 4 or more years. Varta CR lithium cells offer the highest capacity available and 10-year life. So whichever your application requires, Varta has the best solution. Contact Varta Batteries, 1-800-431-2504, Ext. 270. FAX: 914-592-2667.

VARTA

CIRCLE NO. 178

80386DX/80486 25/33MHz INDUSTRIAL Single-Board PC/AT Computer

For Passive Backplane System
2 YEAR WARRANTY
45-Day money-back guarantee



80486-25/33MHz

- Intel 80486-25/33 CPU
 - 8K Internal CACHE
 - 256K Secondary CACHE Memory
 - IDE Hard-Disk Interface
 - 2 Serial & 1 Parallel Ports
 - Up to 32MB of DRAM
 - Floppy Interface
- \$895.00** (Without CPU or Memory)
\$2245.00 (With 25MHz CPU & 4MB)

25/33MHz 386 PASSIVE BACKPLANE CPU BOARDS

- 80386DX 25MHz with 2MB **\$875.00**
- 80386DX 33MHz with 128K Cache & 4MB **\$1295.00**

CMOS 386SX BOARD (From \$395.00)
4.75" x 10", 2S, 1P, FDD, IDE, 16MB DRAM,
512KBytes EPROM/SRAM

OEM, Distributors & Dealers **DISCOUNT** available.
Call or FAX for complete information.

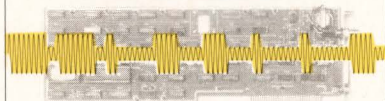
Designed & Manufactured by:

Toronto MicroElectronics Inc.
1848 Bonhill Rd. #1S Mississauga, Ont. L5T-1C4, CANADA
Tel: 416-564-4833 Fax: 416-564-4768

CIRCLE NO. 182

Precision Time Plug-ins

by **TRUETIME**



VME · Multibus · PC

TIME CODE

Time in various formats is furnished to the host computer over its particular bus. Time resolution to 1 microsecond is available.

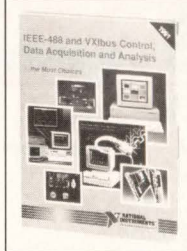
SYNCHRONIZED CLOCKS

Available in a number of sizes and configurations, these boards provide 1 millisecond time synchronization referenced to UTC.

3243 Santa Rosa Avenue • Santa Rosa, CA 95407
(707) 528-1230 • FAX 707-527-6640 • TELEX 176687



CIRCLE NO. 180



Instrument Control and Data Acquisition

Free 1991 color catalog of instrumentation products for personal computers and workstations—application software with graphical user interfaces acquires data from RS-232, GPIB, or VXI instruments and PC data acquisition boards, and analyzes and presents data. Includes data acquisition, GPIB, and VMEbus controller boards, and signal conditioning.

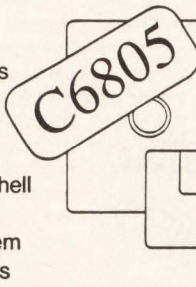
National Instruments
6504 Bridge Point Parkway, Austin, TX 78730
(512) 794-0100 (800) 433-3488

CIRCLE NO. 181

SYSTEM SHOWCASE

C6805 Code Development System

- First 6805 C compiler
- Built-in cross assembler
- Includes integrated shell
- Expert system optimizations



Call today! 519-888-6911

BYTE CRAFT LIMITED
421 King St., N.
Waterloo, ONT. N2J 4E4

CIRCLE NO. 183

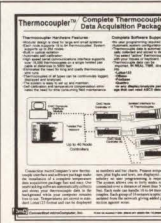


RUGGED AND HIGH PERFORMANCE COMPUTER SYSTEMS WITH FOLD DOWN KEYBOARD AND VGA MONITOR FOR RACK, BENCH OR PORTABLE APPLICATIONS. Standard features include:

- * 12 slot passive back plane
 - * 80386 CPU card at 20/25/33 MHz, up to 8MB of zero wait state RAM
 - * Sony Trinitron tube, high resolution VGA (640x480) monitor and card
 - * Room to mount three half height drives
 - * 2 serial, 1 parallel port, MS DOS/GW basic
- Also available with 80486 or 80286 CPU cards in various configurations, for further details contact:

IBI SYSTEMS INC.
6842 NW 20 Ave., Ft. Lauderdale, FL 33309
(305) 978-9225 Fax: (305) 978-9226 Telex: 529482 IBI SYSTEMS

CIRCLE NO. 184



Complete, Low cost, Distributed Thermocouple Temperature Measurement Package.

Literature on new "Thermocoupler" temperature measurement systems is now available. The Thermocoupler is a complete system providing precise thermocouple measurement for as little as \$30 a channel. No external signal conditioning is required. The Thermocoupler returns real data in Fahrenheit, Celsius or microvolts. Cold Junction Compensation and linearization built in. The system supports hundreds of thermocouples, located up to 5000 feet from the host computer, using a single twisted pair cable. Long, expensive, thermocouple wire runs are eliminated. Thermocoupler software collects data in the background, allowing the use of CmC or any other software package for display or analysis of real time data. Data logging.



(800) 426-2872 (203) 354-9395
Connecticut microComputer, Inc.
568 Danbury Rd. New Milford, CT 06776

CIRCLE NO. 185

STD BUS PRODUCTS

8 & 16 Bit CPU's
Peripherals & Card Cages
Custom Design
Worldwide Service
OEM Discounts
Guaranteed Delivery

ZWICK SYSTEMS INC.



17 Fitzgerald Rd., Suite 104
Nepean, Ontario, Canada, K2H 9G1
Tel (613) 726-1377, Fax (613) 726-1902
Representatives Required!

CIRCLE NO. 186



ELECTROMAGNET RADIATION

Analyze DC and AC Electromagnet Field Radiation from the gamma range (1 gamma =

0.000001 gauss) to 200 kgauss from DC to 100KHz. Earth's field is typically 0.5 gauss DC.

Typical Applications:

- ELF field measurement of power lines, transformers, motors, lamp ballasts, etc.
- CRT/VDT field measurement
- Electromagnetic clean room environment analysis
- Determine magnetic shielding effectiveness

Walker Scientific Inc.
Rockdale Street
Worcester, MA 01606 U.S.A.
Toll Free: (800) 962-4638
FAX: (508) 856-9931

CIRCLE NO. 187

C for the 8051 Compare:

NEW PROFESSIONAL EDITION

Small Benchmarks from BYTE (1/83), 10 iterations. Small memory model.
Whetstones/second from Single Precision Whetstone Benchmark Program (A001)
Dhrystones/second from C/1.1 Program from Reinhold P. Weicker, CACM Vol. 27

Programs validated 10/90 on a 25MHz/386 AT	FRANKLIN PROFESSIONAL C-51 v3.0	BSO/ TASKING CCS1 V1.0.3	IAR/Archimedes ICC8051 v4.01B
Total Execution Time (large model)	6.744 sec 8.287 sec	8.753 10.98	8.388 17.295
Module Code Size (large model)	188 bytes 188 bytes	266 303	238 343
dynamic Data Size	41 bytes	126	96
Total Code Size (large model)	1223 bytes 1292 bytes	1936 3467	1626 2088
Whetstones/Second	13	Float not yet supported	3
Dhrystones/Second	203	163	90



888 Saratoga Ave. #2 • San Jose, CA 95129
(408) 296-8051 • FAX (408) 296-8061

CIRCLE NO. 188

1991 UPCOMING ISSUES Computer Design Magazine Edition

MONTH	SPECIAL REPORT	TECHNOLOGY FOCUS	PRODUCT FOCUS
June 1 DAC	Design synthesis Barbara Tuck	Mil-Spec standard buses — Warren Andrews Disk controller ICs	Op amps Jeff Child
July 1	CASE for real-time programming Tom Williams	Mezzanine buses — Warren Andrews Device modeling — Mike Donlin	Multibus CPU boards Jeff Child
August 1* Siggraph	Mixed-signal ASICs Barbara Tuck	Display controller ICs Software-management tools — Tom Williams	DRAMs Jeff Child
September 2 Buscon-E ESC	Enhanced-performance standard buses Warren Andrews	CAD frameworks — Mike Donlin RISC in real-time — Tom Williams	Device programmers Jeff Child

*Starch Readership Study Issue

PennWell Publishing Company • One Technology Park Drive • Westford, MA 01886 • 508-692-0700



CIRCLE NO. 190



357 MHz 14-Pin Clock Oscillator

Connor-Winfield Corp. announces literature on a new line of high frequency ECL Logic clock oscillators. The ECLB Series oscillator covers the high frequency range of 8 MHz-360 MHz. AVAILABLE NOW IN A 14-PIN DIP. Literature for a double DIP version with frequencies to 500 MHz is also available. Frequencies to 90 MHz are now available with Voltage Control function (model EV53 series). Contact Barney III for details.

Additional specifications listed below:

Model : ECLB
 Package : 14-pin DIP
 Frequency: 8 MHz to 360 MHz
 Supply : -5.2 or -4.5 Vdc

Connor-Winfield Corporation
 1865 Selmarten Road
 Aurora, IL 60505
 PH: (708) 851-4722 FAX: (708) 851-5040
 CIRCLE NO. 192

Passive Backplane CPUs

80386SX 16 MHz & 20 MHz,
 512K through 16M DRAM

80386DX 25 MHz & 33 MHz,
 1M through 32M DRAM,
 128K cache optional

80486 25 MHz & 33 MHz,
 1M through 32M DRAM,
 256K cache optional

Call, write, or FAX for complete specifications and OEM terms.

Retail, OEM, and Private Label available

Designed, Manufactured, Sold and Serviced by:

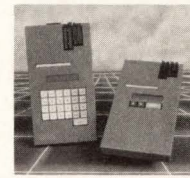


Voice . . . (612) 345-4555
 FAX . . . (612) 345-5514
 Modem . . (612) 345-4656

907 N. 6th St., Lake City, MN 55041

CIRCLE NO. 193

(E)PROM/PLD PROGRAMMERS



Low Cost, High Performance solutions for users of programmable ICs. BYTEK offers logic & memory programmers for

Design, Production, Field Service & Engineering Labs. Stand-alone units offer RS232 & Parallel Port for quick data transfer. 3.5" Disk Drive for easy updates. **FREE** Warranty & Updates for 1 yr. Models from \$495. (US)

Call for Catalog: 800-523-1565.

BYTEK Corporation

543 NW 77th St., Boca Raton, FL 33487
 (407)994-3520 FAX: (407)994-3615

CIRCLE NO. 194

EPROM PROGRAMMER



\$750 8 ZIFs
 20 Key Keypad 20x4 LCD

- Quick pulse pgms. eight 1 Mbit EPROMs in 40 sec.
- Stand-alone or PC-driven
- RS-232, parallel in & out ports
- Binary, Intel hex, & Motorola S formats
- 100 user-definable macros
- Information, call (916) 924-8037
- 1 Megabit of DRAM
- Made in U.S.A.
- A9 Identifier
- 2 year warranty
- Single pgmr. \$550

NEEDHAM'S ELECTRONICS
 4539 Orange Grove Ave. • Sacramento, CA 95841
 (M-F, 8-5 PST)

CIRCLE NO. 195

"Tango-PLD is the price/performance leader in logic design tools."

"I regularly put this program through its paces. It's inexpensive and works great. I'm telling as many friends as I can that Tango-PLD is the best value in programmable logic design."



Tango

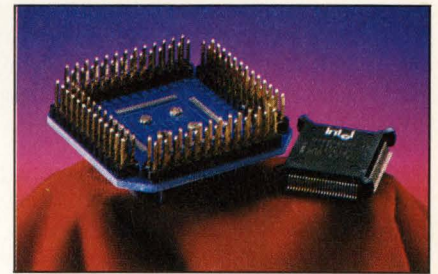
See for yourself. Call today to order your free PLD design evaluation package.

800 488-0680
 619 554-1000 • FAX: 619 554-1019

ACCEL Technologies, Inc.
 6825 Flanders Drive • San Diego, CA • 92121 • USA
 Contact us for the representative nearest you



CIRCLE NO. 196



Quality Debugging Accessories

- Protect your ICs from damage. Insert and extract LCC, PLCC, PGA, and PQFP packages with the right tool.
- Use receptacle boards to build test fixtures, and mount your test equipment, in half the time.
- Get the right production sockets, burn-in sockets, test leads, and test clips for SMT, SOIC, or PLCC circuits.
- Quick turnaround on custom engineering services, if needed. For a free catalog, contact:

Emulation Technology, Inc.
 2344 Walsh Ave. Santa Clara, CA 95051
 Phone: 408-982-0660 FAX: 408-982-0664



CIRCLE NO. 197

TARGET COMPUTER DESIGN SUBSCRIBERS BY MAIL

COMPUTER DESIGN subscriber list available for rent. 100,000 direct mail responsive engineers and engineering managers. Key decision makers, by name, at business addresses. Target by job function, company type, design management, product design, purchase influence or geographic areas. Proven winner for books, subscriptions, technical reports, seminars, conferences, tools, components, catalogs, hardware, software, testing instruments and many other offers.

For more information call
 Deanna Rebro at PennWell Lists,
 Advanced Technology Group:
 800-982-4669 or 918-831-9551

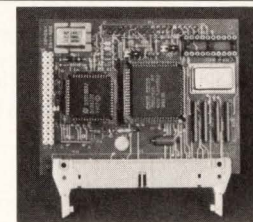
The only company who didn't need to make better EDA tools just did.

OrCAD introduces Release IV of our entire line of PC-based design automation software. All products, from programmable logic and schematic design through simulation to printed circuit board layout now work seamlessly within the new ESP framework. Try it for yourself.

OrCAD
 Call (503) 690-9881 today
 for a FREE demonstration disk.



CIRCLE NO. 199



ZBX-380 SCSI/Floppy Host Adapter

Powerful SCSI host adapter with floppy drive controller on single-wide iSBX-compatible (Intel)

module featuring single-ended operation using NCR's 53C90 SCSI processor. ZBX-380 supports high-speed data transfer—4MB/sec. synchronous and 1.5MB/sec. asynchronous. DMA operations from host iSBX-compatible boards are supported (Zendex MBI master/slave SBC with 486, 386, 286, or 186 CPU), as are interrupt service operations. SCSI implementation conforms to ANSI X3T9.2 specifications. The ZBX-380 is an ideal SCSI host adapter for virtually all Multibus I/II, VME, PC-AT/ and SBus systems. Drivers are available for Intel's RMX I/II and Microsoft's MS-DOS operating systems. Zendex Corporation, 6780A Sierra Court, Dublin, CA 94568-2623. (415) 828-3000. FAX (415) 828-1574.

CIRCLE NO. 200

As design engineers and managers you know that the higher speeds and greater complexity of electronic systems are making your jobs more challenging. As clock speeds climb to 50MHz and beyond, analog characteristics become major considerations for digital designs. In addition, demands for mixed-signal technology have increased in the consumer, automotive, and telecom markets. According to Technology Resource group, 40% of all ASICs will be mixed analog and digital by 1994.

*Analog and mixed-signal design issues are the most challenging area of design engineering.
Until now you've been on your own...*

Announcing the First Annual

ANALOG & MIXED-SIGNAL DESIGN CONFERENCE

Finally, there's a source for objective and up-to-date information on analog and mixed-signal design. This technical conference, sponsored by **COMPUTER DESIGN Magazine**, features over 45 lectures and workshops dedicated 100% to your needs as an analog designer. Nowhere else will you find so much information, so much technology and so much expertise all under one roof.

High-Quality Workshops

Respected engineers will offer high-quality information that you can immediately use to help you complete your design projects more quickly, creatively, and elegantly. You'll learn about analog and mixed-signal simulators, different design techniques, analog implications of high-speed systems, and much more in workshops such as:

Transmission-Line Effects in High-Speed Design • Mixed Analog/Digital Design, Modeling, Simulation, and Test • Designing with Worst Case and Monte Carlo Analysis Techniques • Solving Convergence Problems in SPICE • Modeling Device Performance Over Temperature • And much, much more.

Practical, Hands-on Instruction

For years you've been subjected to oral press releases from vendors under the guise of objective panel discussions. The ANALOG & MIXED SIGNAL DESIGN CONFERENCE is different. You'll find in-depth, practical and real-world information from well-known practitioners—experts who will give you knowledge you can bring to the workstation tomorrow!

Who Should Attend?

The Analog & Mixed-Signal Design Conference is dedicated to the unique needs of mixed-signal design. If you're an analog design engineer, a digital designer who must address the analog implications of high speed design, or an engineering manager, you should attend this conference.

Question Authority

The Analog & Mixed Signal Design Conference Vendor Products Exhibition features booths crammed with the latest in analog and mixed-signal design tools. As questions arise about different products or problems, you can go directly to the vendor authorities on the exhibit floor for answers. They will be on hand to let you try out and compare products, give you a clear grasp of the practical tools available, and tell you where to look for new avenues of information exchange. And the convenient Silicon Valley location gives you access to the best and the brightest in the design community.

As an attendee at the Analog & Mixed-Signal Design Conference you'll learn how to improve your design skills, how to increase your productivity, and where to turn in order to ensure design success. All in three days, all under one roof.

Join your colleagues this October in Santa Clara. Launched with your needs in mind, this in-depth, technical conference promises to be one of the most significant industry events of the year!

ANALOG & MIXED-SIGNAL

Santa Clara Marriott

10101001010010100100010011
0001110010010101011101001
100010011001010100101010
010001010100100101010111
0100010101001010101010101
1100110001010001001100010
01100010100110010110001101

Santa Clara, California

DESIGN CONFERENCE

October 30 - November 1, 1991

For more information call:
Angela Hoyte at (415) 905-2354
or FAX at (415) 905-2630

Sponsored by: **COMPUTER DESIGN Magazine**
Produced by **Miller Freeman, Inc.**
P.O. Box 7843, San Francisco, CA 94120-7843.

PLEASE SEND ME COMPLETE INFORMATION ON THE
FIRST ANNUAL ANALOG & MIXED-SIGNAL CONFERENCE.

I'M INTERESTED IN ATTENDING EXHIBITING

NAME _____

TITLE _____

COMPANY _____

STREET _____

CITY, STATE, ZIP _____

PHONE/FAX _____

Analog & Mixed-Signal Design Conference, P.O. 7843, San Francisco, CA 94120-7843

CD5/91

ADVERTISERS INDEX

ADVERTISER	PAGE NO.	CIRCLE NO.	ADVERTISER	PAGE NO.	CIRCLE NO.
A					
Accel Technologies	149	196	Logical Devices Inc.	146	170
Alacron	131	76	Loughborough Sound Images	120	74
American Megatrends	119	67	LSI Logic	4,5	4
AMP	108,109	64	M		
Ancot	18	12	Macrolink	117	66
Anritsu	52	33	Maroloni	93	57
Applied Microsystems	16,17	10	Matrox	59	38
Atmel	105	62	Microsoft	115	—
Atmel	107	63	Microtek	97	59
Automation Products Inc.	147	176	Microware Systems	29	20
Avocet Systems Inc.	146	172	Mitsubishi	33	23
B					
Brooktree	34,35	24	Mizar	58	37
BSO/Tasking	73	46	* Motorola Semiconductor	26,27	—
Bytecraft	148	183	Multibus Mfg Group	65	—
Bytek Corporation	149	194	Murrieta Circuits	126	71
C					
Canon USA	47	30	N		
Canon USA	135	77	National Instruments	147	181
Chrislin Industries	152	88	National Semiconductor	66,67	—
Connecticut Microcomputer	148	185	Needham's Electronics	149	195
Connor-Winfield	147	177	Newbridge	39	26
Connor-Winfield	149	192	Nissho	41	27
Coreco	126	69	Nissho	95	58
Cortex	9	6	O		
CSPI	57	36	Oasys	70	43
Cypress	Cover 4	—	Omation	20	16
D					
Data I/O	79	49	ORCAD	149	199
Data Translation	51	32	P		
Design Automation Conference	139	80	Paradigm Technology	22	18
Diversified Technology	42,43	28	PC Tech	149	193
DY 4 Systems	11	7	PRC	147	174
E					
Electronic Solutions	1	2	R		
Emulation Technology	149	197	Radisy	15	9
Epson	37	25	Ricoh	111	65
F					
FEE Technologies	18	11	Robotrol	146	167
Force Computers	91	56	S		
Franklin Software	148	188	SBE	Cover 3	89
G					
Gates Energy Products	74,75	47	Sealevel Systems	20	15
GCOM	146	169	Seiko Instruments	128	—
General Micro Systems	60	39	Siemens	19	14
Gespac	Cover 2	1	Siemens	31	21
Grammar Engine	147	175	Silicon Systems, Inc.	2	3,19
Green Springs Computers	138	81	Software Components	68	42
H					
Heurikon	61	40	Sophia Systems	122	—
Hewlett-Packard Workstations	6,7	5	Spectrum Signal Processing	120	74
Hewlett-Packard EAG	103	61	Startech Semiconductor	86,87	54
* Hitachi Peripherals	19	13	Switchcraft	88	55
I					
I-BUS	63	41	Synergy	12,13	8
IBI	148	184	Synopsys	76	48
IBM	44,45	29	Systran	32	22
Industrial Computer Solutions	146	166	T		
Integrated Circuits Systems	21	17	Tadpole Technology	80A	97
Intel MicroComputer	49	31	Themis	85	53
Intel Embedded Controllers	54,55	35	Todd Products	112A	95
Intel	151	87	Toronto Microelectronics	147	182
Intermetrics	71	44	Tri-L Data Systems	146	168
Interphase	83	50	U		
Ironics	98,99	60	Ultimate Technology	134	78
ITT Pomona	53	34	Universal Cross Assemblers	146	173
K					
Kinometrics	147	180	V		
L					
L-COM	146	171	VMIC	72	45
			Varta Batteries	147	178
			W		
			Walker Scientific	148	187
			Z		
			Zendex	149	200
			Ziatech	127	72
			Zoltech	121	51
			Zwick Systems	148	186

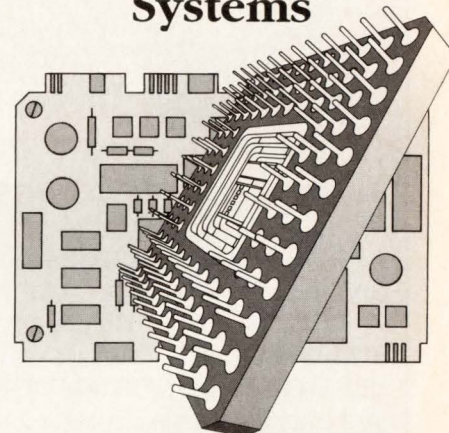
* Domestic only
† International only

The Advertisers Index is published as a service. The publisher does not assume liability for errors or omissions.

intel®

Access in Europe

Microelectronics Components Boards Systems



EUROPEAN SALES OFFICES

FINLAND

Intel
Ruosilantie 2
00390 Helsinki
Tel.: (358) 0 544 644
Fax: (358) 0 54 40 30
Telex: 1 23 332

FRANCE

Intel
1, rue Edison - BP 303
78054 St. Quentin-
en-Yvelines Cedex
Tel.: (33) (1) 30 57 70 00
Fax: (33) (1) 30 64 60 32
Telex: 6 99 016

UNITED KINGDOM

Intel
Pipers Way
Swindon, Wilts SN3 1RJ
Tel.: (44) (0793) 69 60 00
Fax: (44) (0793) 64 14 40
Telex: 4 44 447/8

NETHERLANDS

Intel
Postbus 84130
3099 CC Rotterdam
Tel.: (31) 10.407.11.11
Fax: (31) 10.455.46.88
Telex: 2 22 283

ISRAEL

Intel
Atidim Industrial Park-
Neve Sharef
P.O. Box 43202
Tel-Aviv 61430
Tel.: (972) 03-498080
Fax: (972) 03-491870
Telex: 3 71 215

ITALY

Intel
Milanofiori Palazzo E
20090 Assago Milano
Tel.: (39) (02) 89 20 09 50
Fax: (39) (02) 349 84 64
Telex: 3 41 286

SPAIN

Intel
Zurbaran, 28
28010 Madrid
Tel.: (34)-1-308.25.52
Fax: (34)-1-410.75.70
Telex: 46880

SWEDEN

Intel
Dalvägen 24
171 36 Solna
Tel.: (46) 8 734 01 00
Fax: (46) 8 27 80 85
Telex: 12261

SWITZERLAND

Intel
Zürichstrasse
8185 Winkel-Rueti bei Zürich
Tel.: (41) 01/860 62 62
Fax: (41) 01/860 02 01
Telex: 8 25 977

GERMANY

Intel
Dornacher Strasse 1
8016 Feldkirchen
Tel.: (49) 089/9 09 92-0
Fax: (49) 089/9 04 39 48
Telex: 5-23177

Intel
Abraham Lincoln
Strasse 16-18
6200 Wiesbaden
Tel.: (49) 06 11/72 87-05-0
Fax: (49) 06 11/71 86 15
Telex: 4-186 183

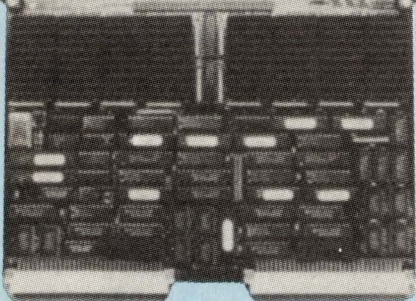
Intel
Zettaching 10 A
7000 Stuttgart 80
Tel.: (49) 07 11/72 87-280
Fax: (49) 07 11/72 80 137
Telex: 7-254 826

DOWN ADVERTISING

CIRCLE NO. 87

40 + MB/SEC DUAL-PORT VME/VS HIGH - DENSITY MEMORY

from
Chrislin Industries, Inc.
Your
TOP QUALITY Memory Supplier
for
OVER 15 YEARS



THE CI-VME40 FEATURES

FAST ACCESS TIMES

* 20NS READ/WRITE in BLOCK CYCLE

FAST CYCLE TIMES

* 83/62NS READ/WRITE in BLOCK CYCLE

VERSATILE CONFIGURATIONS

* 4MB, 8MB, 16MB, 32MB or 64MB in one

VMEbus/VS 6U option slot

VERSATILE ADDRESSING

* Addressable in 24 or 32 bit through

4 Gigabytes

* Memory start and end addresses

selectable on 256kb boundaries

* VMEbus/VS configured independently

RELIABLE

* Byte Parity Error Detection

* LIFETIME WARRANTY

OTHER QUALITY VMEbus MEMORIES AVAILABLE ARE:

THE CI-VMEemory

LOW-COST VMEbus BYTE PARITY
MEMORY with 4,8,16,32, or 64MB
in one 6U VMEbus slot

THE CI-VSB EDC

Dual-port VMEbus/VS memory
with Error Detection and Correction,
single-bit error detection/correction,
double-bit error detection, 4MB up
to 64MB in one VMEbus/VS slot

Chrislin Industries, Inc.

31312 Via Colinas, Suite 108
Westlake Village, CA 91362

TEL: (818) 991-2254 FAX: (818) 991-3490

CALL TOLL FREE: (800) 468-0736

CIRCLE NO. 88

COMPUTER DESIGN

Technology
and Design
Directions

Executive Office: One Technology Park Dr, PO Box 990, Westford, MA 01886

(508) 692-0700 Fax: (508) 692-0525 Telex: 883436

Publisher: David L. Allen (508) 392-2111

Associate Publisher/Editor-in-Chief: John C. Miklosz (508) 392-2114

Associate Publisher/National Sales Manager: Tim L. Tobeck (516) 883-8815

Marketing Communications Assistant/Research: Annette Petagna (508) 392-2209

Administrative Assistant: Peg Alexander (508) 392-2112

Ad Traffic Manager: Betsy Anderson (508) 392-2198

Recruitment Advertising: Sue Nawoichik (508) 392-2194, Eastern U.S.

Tom Murphy (213) 372-2744, Western U.S.

Postcards/System Showcase/Bulletin Board: Sue Nawoichik (508) 392-2194

Circulation Director: Bob Dromgoole (918) 832-9213

Circulation Manager: George Andrew (918) 831-9443

List Rental: Deanna Rebro (918) 831-9551

SALES OFFICES

Associate Publisher

Tim L. Tobeck

Mid Atlantic

Eleanor D. Hobbs
14 Vanderventer Ave, Suite 1
Port Washington, NY 11050
Tel: (516) 883-8815
Fax: (516) 883-6268

New England/New York State/ Eastern Canada

Tim Pritchard
One Technology Park Dr
PO Box 990
Westford, MA 01886
Tel: (508) 392-2217
Fax: (508) 692-0525
Telex: 883436

Upper Midwest

George Mannion
21517 Locust
Matteson, IL 60443
Tel: (708) 748-7565
Fax: (708) 748-7695

South Central/Southeast

Eric Jeter
19627 I-45 N, Suite 220
Spring, TX 77388
Tel: (713) 353-0309
Fax: (713) 288-8350

Southern California/Southwest

Tom Boris, Greg Cruse, Phil Cook
2232 SE Bristol, Suite 109
Santa Ana Heights, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

Northern California/ Nevada/Western Canada

John Sly, Bill Cooper
1000 Elwell Ct, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

Oregon

Tom Boris
2232 SE Bristol, Suite 109
Santa Ana Heights, CA 92707
Tel: (714) 756-0681
Fax: (714) 756-0621

Washington

Bill Cooper
1000 Elwell Ct, Suite 234
Palo Alto, CA 94303
Tel: (415) 965-4334
Fax: (415) 965-0255

U.K./Scandinavia

David Round
69 Imperial Way
Croydon, Surrey CRO 4RR
England
Tel: 81-686-7655
Fax: 81-688-2134

France/Belgium/ Southern Switzerland/ Spain/Netherlands

Daniel R. Bernard
10, rue Michelet - B.P. 279
78502 Sartrouville Cedex, France
Tel: 01-39-14-67-80
Fax: 01-39-14-70-14

Germany/Austria/Northern Switzerland/Eastern Europe

Johann Bylek
Verlagsbuero Johann Bylek
Stockaekerring 63
D-8011 Kirchheim/Muenchen
Federal Republic of Germany
Tel: 89-903-88-06
Fax: 89-904-35-26

Italy

Luigi Rancati
Rancati Advertising
Milano San Felice Torre 5
20090 Segrate, Italy
Tel: 02-70300088
Telex: 328601 RANCAD I
Fax: 02-7532354

Japan

Toshio Egusa
PubliNetwork
C407, 2-22-6
Tsukuda Chuo-ku
Tokyo 104, Japan
Tel: 03-3536-5404
Fax: 03-3536-5490

Southeast Asia

**Taiwan/Hong Kong/Korea/
China/Thailand/Philippines/
India/Pakistan/Singapore/
Malaysia/Indonesia/Australia/
New Zealand**

Tom Gorman
CCI Asia-Pacific, Ltd
Suite 905, Guardian House
32 Oi Kwan Rd, Happy Valley
Hong Kong
Tel: 833-2181
Fax: 834-5620

COMPUTER DESIGN (ISSN-0010-4566) is published monthly by PennWell Publishing Company, 1421 S Sheridan, Tulsa, OK 74112. Second-class postage paid at Tulsa, OK 74112 and additional mailing offices. Editorial offices are located at One Technology Park Dr, PO Box 990, Westford, MA 01886. Annual subscription price: \$88 in the U.S.A., \$139 in Canada, \$148 for Europe via air, and \$192 other foreign via air. Call (918) 832-9263 for subscription information. Microfilm copies of COMPUTER DESIGN may be purchased from University Microfilms, a Xerox Company, 300 N Zeeb Rd, Ann Arbor, MI 48106. POSTMASTER: Send change of address form to COMPUTER DESIGN, Circulation Department, PO Box 3466, Tulsa, OK 74101. ©1991 COMPUTER DESIGN by PennWell Publishing Company. All rights reserved. No material may be reprinted without permission from the publisher. Officers of PennWell Publishing Company: Philip C. Lauinger, Jr., Chairman and Chief Executive; Joseph A. Wolkling, President; John Ford, Senior Vice-President; Carl J. Lawrence, Senior Vice-President; Joe T. Bessette, Senior Vice-President; John Maney, Vice-President/Finance; Steve Zimmerman, Vice-President/Corporate Services.



*No Matter
What the
Application,
SBE Fits.*

Matching your high-speed data communications requirements with a quality supplier has never been easier. Whether you're a manufacturer of mini/superminicomputers, workstations or high-performance data communications products, *only* SBE provides a perfect fit.

Only SBE offers a complete line of intelligent high-performance communications controllers for all major interface technologies: FDDI, Token Ring, Ethernet and High Speed Serial. Only SBE adds premium features, without a premium cost, for the best price/performance in the industry.

Add integrated hardware/software solutions; availability in VMEbus, Multibus and SBus; plus legendary development assistance and continuing product support.

Discover how SBE's intelligent high-performance controllers can meet your LAN and WAN interface requirements. Turn to SBE today.



For fast action, call: 1-800-347-COMM

Germany: 0130-810588

United Kingdom: 0800-378-234

SBE, Inc., 2400 Bisso Lane, Concord, CA 94520

CIRCLE NO. 89

SBE
Communications &
Real-time Solutions

TURN A FEW DOLLARS INTO A COOL 18 MILLION.



*SPARC
Embedded RISC.
18 MIPS.*

Embedded control challenge of the 90s:
Applications are increasingly burdened with the overhead of friendliness. Even so, users expect everything to happen immediately, if not sooner.

As a result, applications with embedded microprocessors need more computing power than ever. Our CY7C611 SPARC® RISC controller gives you the power to create, at a price that fits your application.

It performs. At 25 MHz, our CY7C611 delivers 18 sustained MIPS.

It handles interrupts brilliantly. Asynchronous and synchronous traps let you jump to trap routines with 200 ns worst case response. 16 prioritized interrupt levels let you tailor your application. You get 136 32-bit registers that you can divide into register banks for fast context switching.

It has hooks. Connect our CY7C602 concurrent floating point unit for 5 MFLOPS. Use our CY7C157 Cache SRAM for a zero wait state memory system.

Use our CY7C289 512K PROM for glueless, virtually waitless program storage.

It is extendable. You get a large address space, and support for multitasking and multiprocessing.

It is affordable. We're talking a few dollars per MIPS.

And it is SPARC. You can choose from a multitude of SPARC platforms to operate as native development platforms. You work with the world's most popular RISC architecture. You can expect faster evolutions, to keep your design current well after it is designed.

The whole story – from data sheet to User's Guide – is yours for a fast, free phone call.

**Free SPARC RISC User's Guide.
Hotline: 1-800-952-6300*
Ask for Dept.C11K.**



**CYPRESS
SEMICONDUCTOR**

*1(800) 387-7599 in Canada. (32) 2-652-0270 in Europe. ©1991 Cypress Semiconductor, 3901 North First Street, San Jose, CA 95134. Phone: (408) 943-2600. Telex: 821032 CYPRESS SNJ UD, TWX: 910-997-0753. SPARC is a registered trademark of SPARC International, Inc. Products bearing the SPARC trademark are based on an architecture developed by Sun Microsystems, Inc.