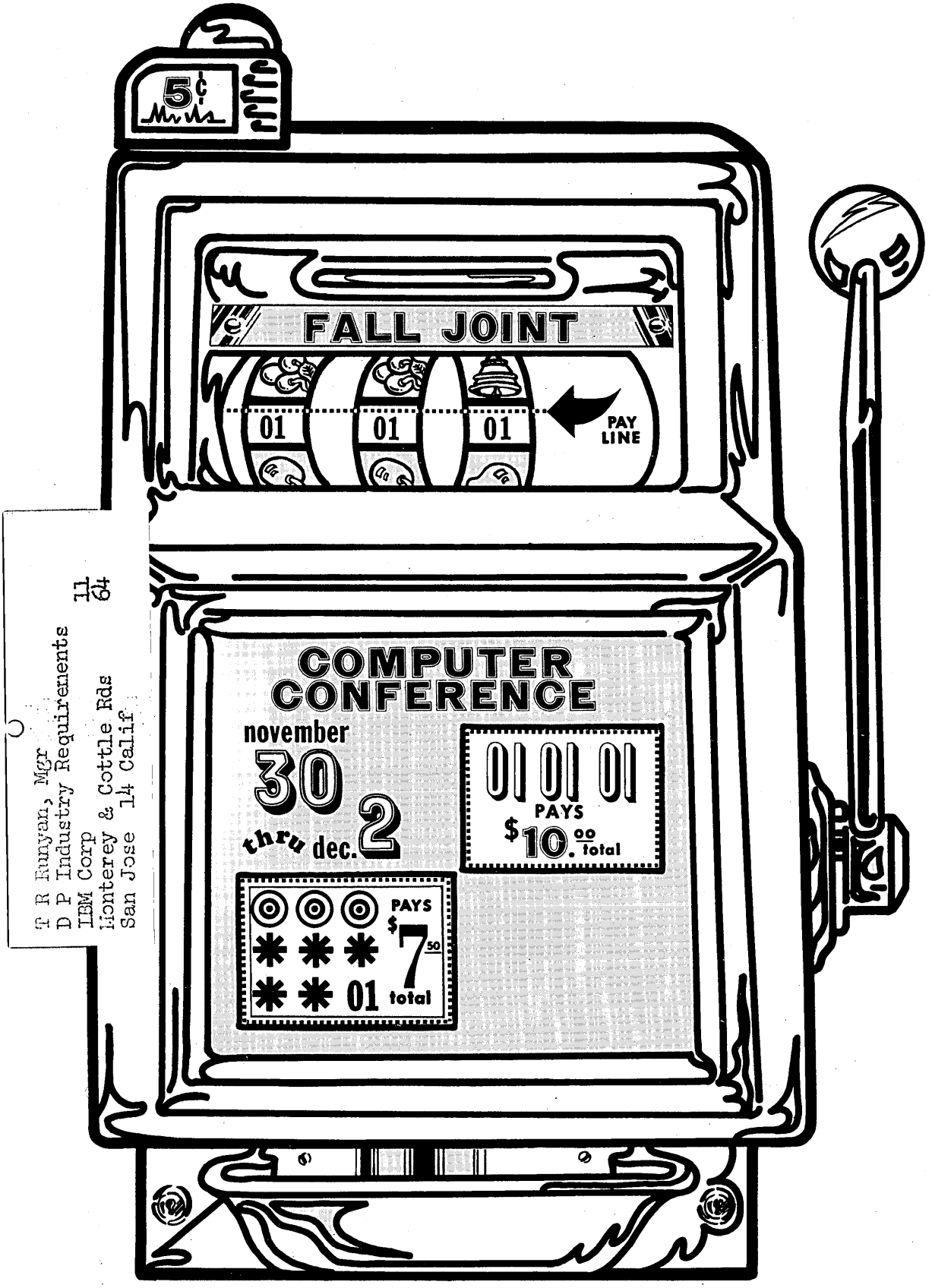
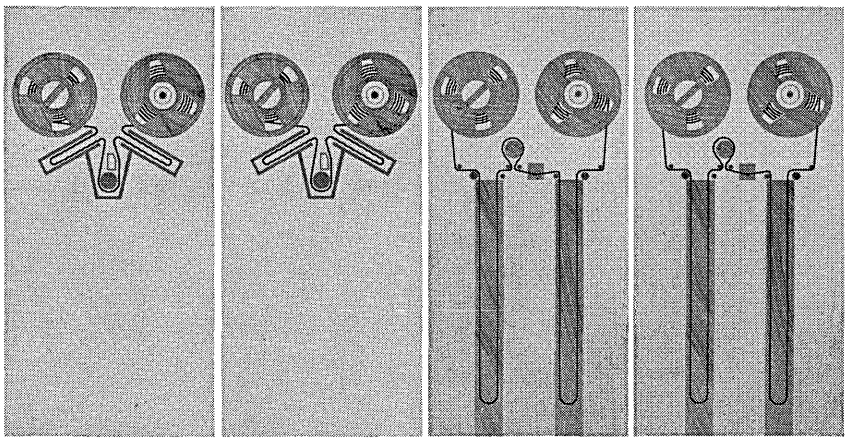
DATAMATION 65®

November



Only Ampex gives you a complete family of interface interchangeable single-capstan tape transports.



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Ampex Corporation,
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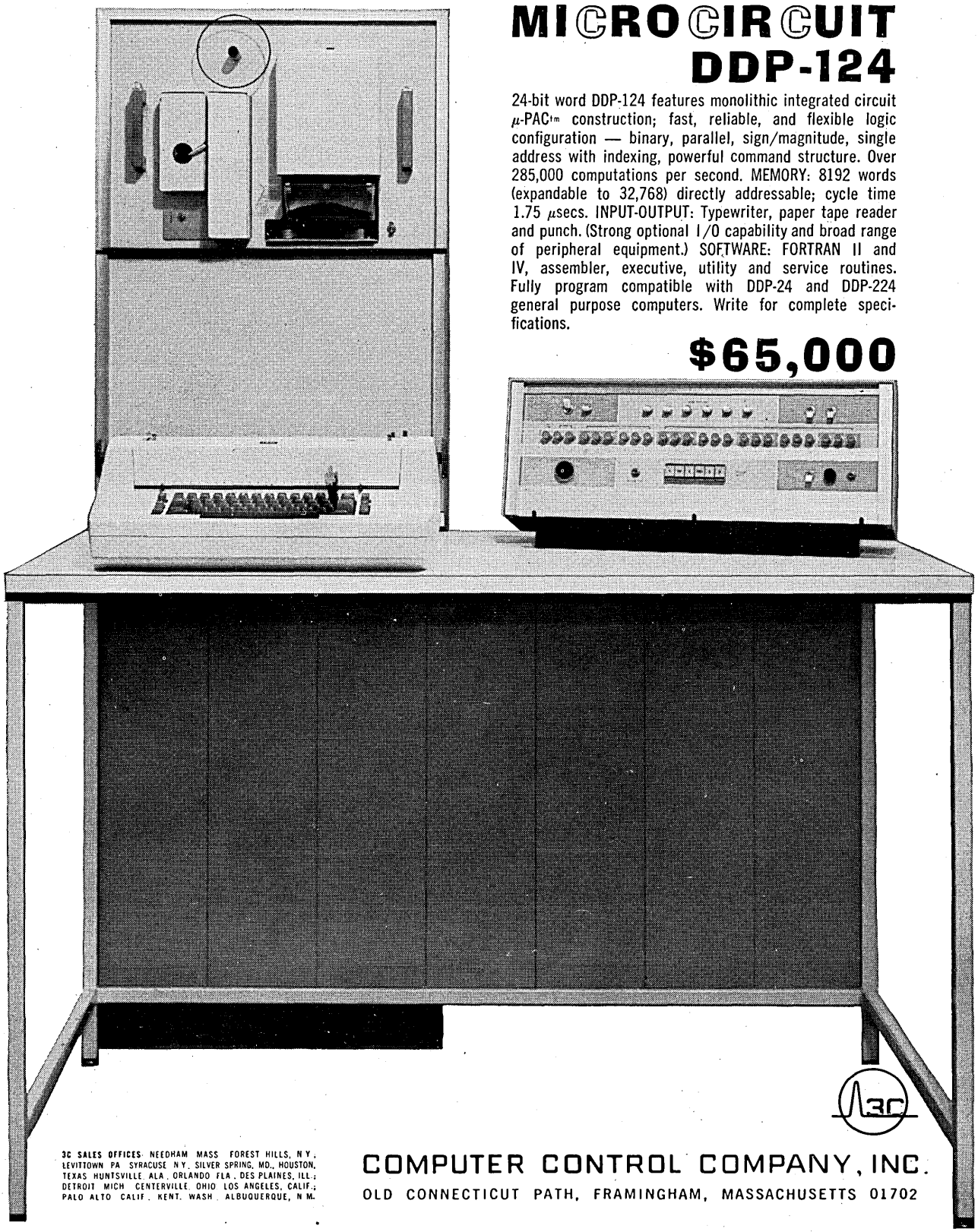
AMPEX

CIRCLE 1 ON READER CARD



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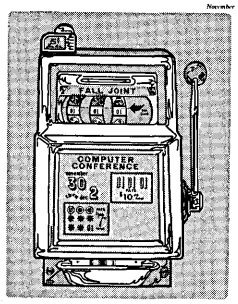

november
1965
volume 11 number 11

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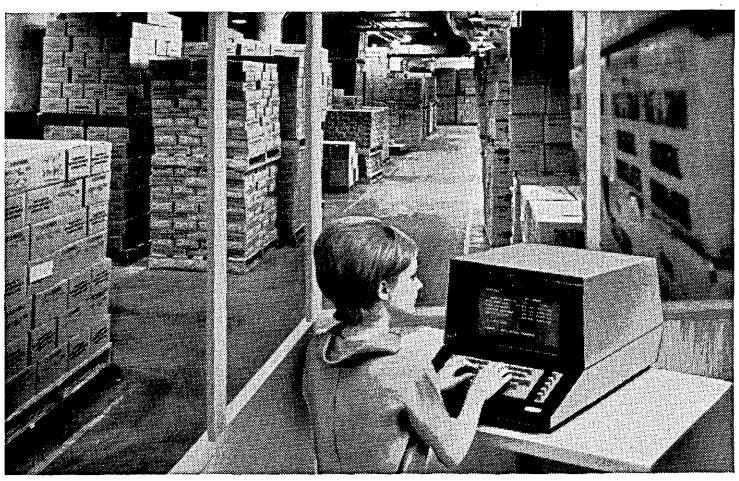
THIS ISSUE 60,202 COPIES

New from Raytheon... the first self-contained remote display console available at an economical price...$6000*



It's no longer necessary to buy — or rent — expensive multi-display control units to serve locations that only need 1 or 2 remote display stations.

The Raytheon Display Console, model 402, is the only low-cost equipment with its own control unit combined into the *same* package. And, because the 402 connects directly to a telephone dataset, there's no need for a separate interfacing console. Character generator, buffer memory, keyboard, telephone interface and power supply are all combined in one desk-top sized package which can be remotely connected to any general purpose digital computer.

The 402 can be easily moved from one location to another. Connect, and it's ready for quick-response, on-line communication with regional offices, warehouses, or ticket offices. Ideally suited for remote computer time sharing applications.

If your problem is one of providing real-time access to computer-stored information from remote locations, send today for information about the new model 402 Display Console and other units in Raytheon's DIDS (Digital Information Display System) family. Write: *Manager of Industrial Sales, Dept. D 115, Raytheon Company, Wayland, Massachusetts 01778. Or phone: (617) 358-2721 ext. 2911.*

*Rental prices available on request

RAYTHEON

CIRCLE 9 ON READER CARD

AN OFF-BIT HISTORY OF MAGNETIC TAPE... #9 of a series by Computape*

There were mutterings at the Round Table that Merlin the Magician was growing absent minded, not to say daft. The Knight of the Silver Spoon was sure of it. And the Knight of the Iguana agreed.

"Absent minded am I? Ready for Medicare am I?" cackled Merlin. "I'll show them!"

And so he collared the noble Galahad. "Watch this, Gal old boy!" he crowed.

And without so much as an abracadabra — lo! The two were suddenly in a strange room, where a damsel pecked absently at a typewriter and musicians played Greensleeves from the balcony.

"And what do you think those are?" Merlin whispered to Galahad, pointing a warty finger at a bank of computers that had suddenly materialized along the far wall.

"Computers," Galahad replied promptly. "As for the tape, it's heavy duty Computape. Magnetic. 556, or 800, or 1000 bits per inch with no dropout, if I recall."

Merlin sighed. "Then I've shown you this before?"

"At least 25 times," said Galahad. "But fear not, Merlin. None shall ever be the wiser."

And none ever was. After all, would you have the heart to tell on a poor old man?

Galahadn't either.

One of a series of documentaries made possible by COMPUTRON INC., a company even more interested in making history than fracturing it. Our Computape is so carefully made that it delivers 556, 800 or 1,000 bits per inch — with no dropout. Available with 7, 8, 9, 10, 16 channel or full-width certification to meet your systems requirements.

Now — if Computape can write that kind of computer tape history — shouldn't you be using it?

*Reg. T.M. Computron Inc.

COMPUTRON INC.
MEMBER OF THE BASF GROUP
122 CALVARY STREET, WALTHAM, MASSACHUSETTS

COMPUTAPE — product of the first company to manufacture magnetic tape for computers and instrumentation, exclusively.

CIRCLE 10 ON READER CARD

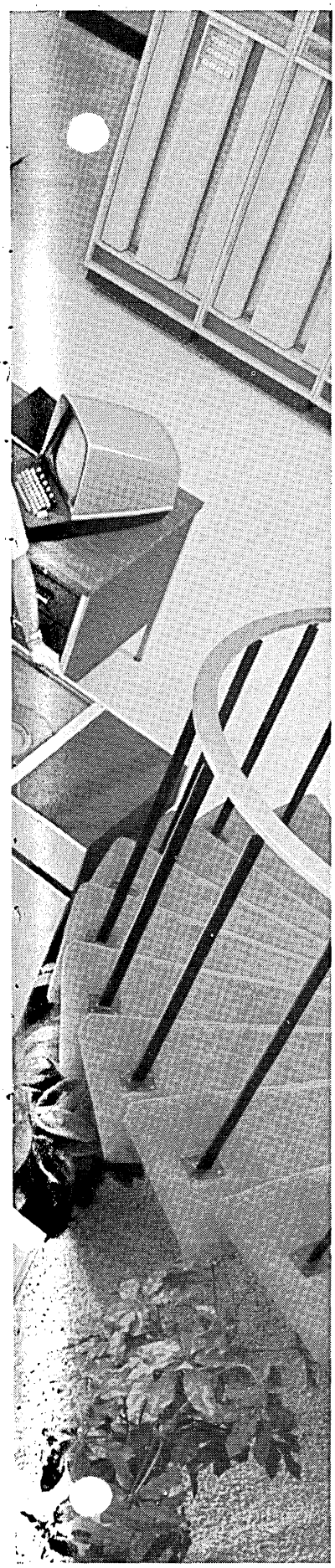
DATAMATION 65®

november 1965

volume 11 number 11

automatic information processing for business industry & science

CONTROL DATA 3300 Time Sharing System shown here includes the following peripheral devices:
915 Page Reader, 405 Card Reader, 415 Card Punch, 852 Disk Storage Drive, 210 Entry and Display Station, and Tape Transports



what say?

"X = ZY + 12 COS (CM-3)"

"FISCAL BUDGET 1962...$3,765,574.32"

"SALES A3646...$12,000...6-10-65"

"SHIPPED 5-5-65...9 GROSS"

"E = MC²"

"INVENTORY J-67443-A...12 UNITS"

tell it to the new CONTROL DATA® 3300/3500 time-sharing systems for business/scientific computing

CONTROL DATA 3300/3500 Computer Systems introduce time-sharing tailored to your individual data processing or computational requirements, with new flexibility ideal for a whole spectrum of medium to high performance needs. Here is power to make business more scientific — scientific problem-solving more businesslike. And with the comprehensive range of Control Data peripherals available to you (many of them shown here) information can be input and output in any preferred format, from widely separated locations. 3300/3500 Systems talk the language of research—production control—engineering—accounting—business management—you name it. And, talk the language of ordinary individuals, through people-oriented peripherals, newest breed of Control Data I/O devices that permit scores of people to use 3300/3500 Computer power simultaneously as if the system were totally dedicated to each user. 3300/3500 Computers offer a choice of several power configurations . . . automatic program relocation features . . . main core memory of over one million characters . . . 1.25 or 0.8 microsecond central memory cycle . . . new and powerful commercial data processing instructions . . . improved performance from existing software library . . . new time-sharing software systems. We can provide complete documentation, hardware and software demonstration, and practically immediate delivery!

and talk about price/performance

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The biggest computers for the biggest installations come from

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Visit our Exhibit at the Fall Joint Computer Conference, Las Vegas, Nov. 30 - Dec. 2

CIRCLE 11 ON READER CARD

DATAMATION calendar

● The fall symposium of the Digital Equipment Computer Users Society will be held Nov. 29, Tresidder Union Hall, Stanford Univ., Stanford, Calif.

● American Univ. is sponsoring the following courses: "The Computer Impact on the Law," Nov. 30-Dec. 3, Twin Bridges Marriott Motor Hotel, Washington, D.C.; "Managerial Implications of Electronics in Publishing," Jan. 17-20, International Inn, Washington, D.C.; "The Challenge of Cybernetics to Education," Jan. 26-28, Twin Bridges Marriott. Fees: $150-175.

● Brandon Applied Systems, Inc. offers the following courses: "Computer Selection," Nov. 30, N.Y.; "Computer Systems Analysis Techniques," Dec. 1, 2, N.Y.; "Management Standards for Data Processing," Dec. 6, 7; "Appreciation Course in Data Processing," Dec. 8, 9; "Computer Selection," Dec. 10, London.

● Scientific Data Systems Users Group meeting will be Dec. 3-4, Dunes Hotel, Las Vegas, Nev.

● C-E-I-R is sponsoring a seminar, "Programming Languages," Dec. 6-8, Hotel del Coronado, San Diego, Calif. Fee: $175.

● Seminars will be held at the Diebold Group's Management Science Training Institute, New York: "Problems of Mounting a Computer Utility Business," Dec. 9, "Software—Purchase or In-House," Dec. 14.

● Lecture series, "Computers and the World of the Future," is being offered by California State Polytechnic Institute, Theater Building, Pomona, Jan. 13, April 21.

● ARINC Research Corp. will present an Integral Electronics course, Jan. 17-21, Airport-Marina Hotel, Los Angeles, Calif. Fee: $450.

● "Methods of Operations Research" is being offered by the Univ. of Miami, Fla., Jan 31—Feb. 4. Fee: $175.

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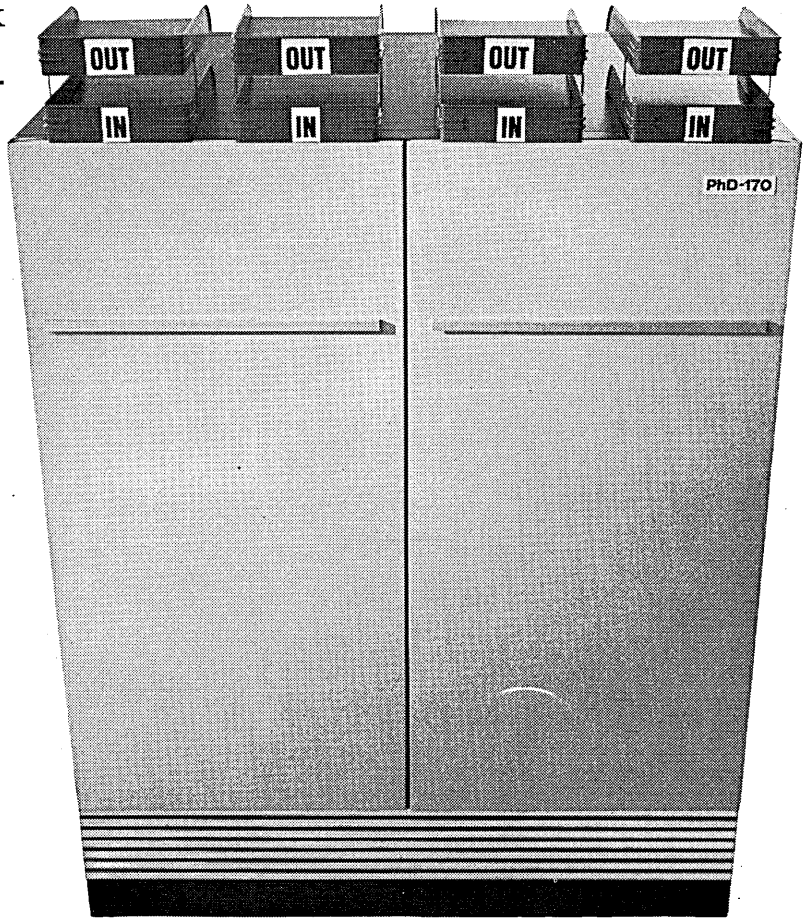

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CIRCLE 13 ON READER CARD

letters

data transmission

Sir:

Justin Perlman's "Centralization vs. Decentralization" in your September issue (p. 24) is an excellent article. You have performed a valuable service by presenting this current perspective on a dynamic subject of continuing importance.

I think, however, that Mr. Perlman unduly complicates the question by equating centralization with standardization and decentralization with destandardization. With the current capability of medium and large-scale computers to control and execute multi-batch type programs in a real-time environment, this need not be the choice. It is entirely possible (technically) to furnish high-speed terminal devices to branch or divisional personnel (communicating with a remote central site computer) which can be used by those personnel as though they did, in fact, have their own computer. The implication is inescapable that they can also do their own systems work and programming with a minimum of concern for those areas of interface with corporate system requirements.

This does not mean, on the other hand, that there is a lessened need for explicit corporate systems objectives and corporate organization and staffing to gain these objectives. But it does mean that the operating divisions can continue to master their own fate. Divisional or branch management is usually best qualified to define and solve their own problems and can do so in a free-handed way using a central computer facility without the rigours of standard operating, reporting, and control procedures levied on them by a corporate systems staff.

Special staffing at the central computer site is required to make it possible for the remote user to operate independently. Some functions of this staff would be to define facilities available to each user under various conditions, to establish some standards of use, to furnish specially skilled consultants to the user for advanced languages such as FORTRAN and COBOL, operations research, communications, and operating systems. In addition, many companies will want to supplement divisional systems and programming personnel with skilled men who are thoroughly familiar with the total central computer hardware and software specifications.

Usage of this type, it seems to me, offers an additional alternative to those presented by Mr. Perlman—i.e., centralize the computer function and standardize those systems where the divisions feed data to corporate reporting, but give decentralized usage to the branch or division through high-speed terminals and let them destandardize their systems and procedures as their own unique requirements dictate.

All the advantages claimed for centralization by Mr. Perlman are still valid and most of the disadvantages are dissolved.

H. GLEN HANEY
Univac Division,
Sperry Rand Corporation
Hartford, Connecticut

Author replies: There is indeed a place for remote independent operation of a central computer, and it is an important place. It is not a panacea, however.

One of the prime points made in the article is that centralization vs. decentralization is not a simple question and typically requires a unique solution for each user. The type of hardware solution Mr. Haney proposes is very attractive and *will* work where the conditions are right. Where distances involved are short and/or input-output (transmission) volume is low the hardware economics may be quite favorable. Where I/O volume is high and distances are long, the economic analysis may look substantially different. A number of hardware operational questions exist too—e.g., if tape master files are utilized, where and how will they be located and how will they be operated?

The aspects of centralization vs. decentralization not directly connected with the hardware (and particularly the non-economic aspects) are somewhat more difficult to analyze in the *general* case. In many situations they are more important than the hardware economics and the technical feasibility of the hardware operating plan. It would require a number of pages to do this justice here. As a brief statement, I think it is well to reflect on the sizable number of efforts in a variety of companies to achieve the type of information-handling operation Mr. Haney describes. Most often these efforts have not been successful. I will concede, of course, that higher-capability data transmission and multi-processing hardware are becoming available, but this is not solely a hardware-oriented question.

As stated in the article, "overall management of the company can be centralized, information-handling management can be centralized, computer hardware can be centralized, and no one of the possibilities *necessarily* dictates the others." Read decentralization in place of centralization and the statement is

equally true. The proper mix for a specific situation is a custom solution.

marketing in u.k.

Sir:

The World Report in September (p. 75) refers to relationships between IBM United Kingdom Ltd. and a new organization known as Centre-File Ltd. Your report states that the two organizations "are understood to have reached some verbal agreement about situations where they are competing."

This statement is wholly without foundation; no arrangements whatsoever have been made with this or any other competitive organization relative to current or future marketing practices or plans, or other competitive situations.

D. J. SCHERER
IBM World Trade Corporation
New York, New York

australian communication

Sir:

In Dr. G. N. Lance's paper "Australian Computing Network" (March, p. 33), he says:

"Data transmission has been considered, but rejected for the time being. In Australia, the Postmaster-General's communication network is not developed to quite such a high standard as in some other countries, and the use of ordinary telephone cables for phase modulated transmission is not currently possible. Coaxial cables and/or microwave links are available but it is too costly to use them over the distances involved."

I feel this does not present a complete picture of the data transmission capabilities of the Post Office telecommunication system and may therefore be misleading.

The P. M. G. Research Laboratories have carried out quite extensive data transmission trials on the Australian telecommunications network. These trials have revealed error rate figures comparable to those published for North American, European, Japanese and other networks, indicating a similar standard of performance. This is not surprising since the Australian communications network is planned and executed to the international standards of C.C.I.T.T. (International Consultative Committee for Telegraphy and Telephony).

In the data transmission field the Post Office is at present providing data channels for phase-modulated data transmission over thousands of miles. Some of these facilities are linked to the outside world via the Pacific Ocean telephone cables. The

global circuits thus provided, of which the Australian portion is very significant, are carrying phase-modulated data signals at 1200 bauds. Some of the circuits are now being phase and amplitude equalised for four-level phase-modulated data transmission at 2400 bits per second, again on a global basis. I feel thus obliged to correct any impression that "the use of ordinary telephone cables for phase-modulated transmission is not currently possible."

Dr. Lance also comments that data transmission facilities over coaxial cables and/or microwave links are too costly over the distances involved. I would like to point out that the department naturally chooses the most economical transmission media in each case, and that its charges to its customers are not directly related to the transmission media used in specific cases. In the case of long distance data circuits different types of transmission media would normally be encountered over different sections of the circuit, but the amount of coaxial cable and/or microwave equipment used would not be reflected into the charges to the customer.

P. R. BRETT
Research Laboratories
Postmaster-General's Department
Commonwealth of Australia/Melbourne

we goofed

Sir:

Under "Rumors and Raw Random Data" (August, p. 19), you stated that Control Data Corp. was "shipping out the 3600 from its Los Angeles service bureau and phasing out the 1604 there." Please let me correct this information.

Control Data's 3600 has been and still is located in Goleta/Santa Barbara, Calif. The only machine that was removed from the L.A. Data Center was a 1604A. As you may know, we also have a 6600 in our L.A. Data Center.

A. T. BASSETT, JR.
Control Data Corporation
Data Centers Division
Los Angeles, California

rehabilitating mag tape

Sir:

The article on tape rehabilitation (August, p. 51) was both informative and thought provoking. It showed that Mr. DeJianne, while showing a grasp of the basic principles involved, is remarkably inaccurate when comparing costs of in-house vs. outside service.

He estimates that cost of outside service for 3,000 reels of tape would be $31,500-43,500. In actual fact, these figures are at least $10,000 overstated. (Prices of $7-9 are now readily obtainable).

Then figuring to his in-house costs, he generously admits to not considering tape drive rental, which runs around $10,000/annum.

On the other hand, no mention is made of other costs such as floor space, utilities, employee overhead, supervision, operating supplies, etc. . . . The truth is that outside service costs are generally very close to in-house costs, and most managers are willing to pay the small difference (if any) to have the job done by specialists.

DON DESBOROUGH
Tape Certifiers Inc.
Gardena, California

time-sharing hysteria

Sir:

I am amazed at the way in which the edp community has overwhelmingly and almost irreversibly committed itself emotionally and professionally to time-sharing. Many normally hard-nosed manufacturers, programmers, engineers, salesmen, analysts, scientists, users, educators, and stock market traders seem not at all to be concerned, as they are for other proposals, with whether the promoter-scientists of time-sharing are systematically, scientifically, and economically exploring it; or whether the probable outcome will be worth the investment; or whether time-sharing is good or bad and for what purposes. All they seem to be concerned with is, which kind to design, build, or buy.

It would be illuminating to obtain some understanding of the causes of this mob behavior. Is it the prestige of MIT and Project MAC? Had Licklider at ARPA not funded Project MAC at MIT but at some other place, would we not now have this irrational, bandwagon behavior? This is a socio-psychological phenomenon that should be studied by specialists in group behavior.

Only at one other period in my professional career did I observe equally puzzling mob behavior. In 1950, the electronics community overwhelmingly committed itself emotionally and professionally to transistors as a replacement for vacuum tubes on no more substantial grounds than that the Bell Telephone Laboratories had developed some three-terminal

solid-state devices that could amplify electrical signals. Normally hard-nosed manufacturers, engineers, salesmen, scientists, users, educators, and stock market traders were not at all concerned with whether reliable transistors could be manufactured in quantity with desirable characteristics. All they seemed to care about was which kind of those available would replace their tubes. In fact, for several years after this widespread commitment and conviction, transistors were largely worthless. Yet so great was the determination that Uncle Sam poured tens of millions of dollars into the effort to make good transistors. And it was so! The enormous expenditure turned out to be worth it; the faithful were redeemed.

But surely the electronics community did not know, when they joined the mob, that the taxpayers would bail them out if they were wrong; nor could they know that to bail them out would be technically feasible, however much money was expended. Why, then, did the electronics community go overboard on transistors, so prematurely? There was no compelling national emergency that would force them to disregard their normal rules of conduct. I used to think that it was the prestige of the Bell Telephone Laboratories and their Nobel Prize winners that represented the Temple and its Clergy to these true believers.

I suppose that the transistor story provides defenders of the time-sharing faith with "evidence" and hope that they too will be redeemed; that the edp community and especially Uncle Sam will continue to pour whatever time, energy, resources, and money it takes to make it so. But I would like to remind the faithful of an ancient Jewish dictum: For example is no proof!

Perhaps the behavioral scientists undertaking to study the present time-sharing syndrome could learn something about the matter by also studying the transistor syndrome of the fifties.

Louis Fein
Palo Alto, California

P. S. I wish to emphasize that I am not disparaging either the interest or the work of those seriously engaged in the important field of time-sharing, as I did not disparage those in the 50's seriously engaged in the important field of transistors. These men have my admiration and respect as do other men working seriously in other fields. What I do disparage and do not understand are premature commitments made by normally sophisticated and cautious communities.

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CIRCLE 18 ON READER CARD

BUSINESS & SCIENCE

WILL SERVICE BUREAUS
OF THE WORLD UNITE?

If a service bureau wants to get in on CEIR's franchise plan, one requirement is that its prospective growth rate be greater than that of the service bureau industry -- 100% every five years. CEIR unfolded more of its program to about 40 independents in a meeting last month, but major questions that have to be left to individual talks include fees and "potential hardware discounts." Though interested centers were dismayed that there may be more than one franchise to a territory, the company emphasizes that they won't be competitive, since specialties differ. An economic model has given CEIR 92 market (application and/or geographic) areas to shoot for with their program during the first 18 months.

Elsewhere, in the service center world, ITT is reported girding for growth of its dp center operation by forming a wholly owned subsidiary devoted to it. One center will open soon on Wall Street, with a 1460 on-line to the Paramus complex, and another for L.A. is on the books.

THE WONDERFUL
WORLD OF PL/I

At the recent SHARE-Jug conference, IBM announced that it has defined a JOSS-like -- not Quiktran-like -- subset of PL/I with appropriate terminal extensions, is looking at terminal control facilities with PL/I for implementation on extensions to Operating System 360, and is investigating list processing and graphic facilities for the language. More, PL/I will be used to produce major parts of normally released IBM processors starting in '67, and it's expected that the PL/I "H" compiler, to be delivered 3rd quarter '66, will be written and compiled by itself.

THE JAMES
GENERAL PURPOSE COMPUTER

The cheap terminal that will permit everyone to use a computer has been under our very noses, says Peter James of Photo Magnetic Systems, Inc. Just take a touchtone phone, put a PMS decal overlay (one per application) on it, maybe add some low-cost PMS peripherals, like a tape printer and crt display, dial the right number, and we're told you'll be able to do everything from remote payroll and inventory accounting, teaching, keypunching, and graphic plotting to controlling building heating systems, and robots. PMS, a small R & D firm for the last 10 years, now has 60 men developing and patenting I/O devices and applications packages, looking for the first 5,000 subscribers in the D.C. area, leasing telephone lines in volume, and setting up manufacturing facilities and their first data center

I'm satisfied w

How about you

My name is Gary Andersen, B.E.E., U. After graduation, I went to work for a puter manufacturer. It was interesting a work, and I gained experience in circuit ation, and production computers in gene

After three years, I took a serious look a growth and wasn't happy with what I sa

Growth careers no

Development Engineer – Memory Syst
B.S.E.E., M.S.E.E., 1-3 years experience in c of position that started Gary Andersen on hi

Development Engineer – Mass Memor
B.S.E.E., M.S.E.E., 3-5 years of digital circu perienced engineer to contribute to the late

Development Engineer – Integrated C
B.S.E.E., M.S.E.E., 2-3 years of circuit and memory systems preferred. An excellent ch

Senior Development Engineer – High
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Research Scientist – R & D
M.S. or Ph.D. in physics or physical electro electromagnetic and magneto-optic propertie film memories.

If you're not satisfied with your pres are waiting for an earthquake to sta ladder of recognition and advanceme to John A. Mitchell, Fabri-Tek Incorp sior Blvd., Hopkins, Minnesota 55343 our climb to success? If you fit any of there could be a reserved seat waitin

in Silver Spring, Md. -- all at the same time.

SYSTEM/360 DELIVERIES DELAYED

With about 300 System/360's now delivered, IBM has notified some customers they will have to wait a while. Production rates for the rest of this year and next will be "85 to 90%" of target goals, which will mean delays for some users of two to four months. The delivery slowdown will apparently affect models pretty much across the line, with blame for the bottleneck being put on the difficulties of producing large enough quantities of circuitry and components.

PROFITABLE TOGETHERNESS

A software house which refuses to play the game according to the stodgy rules of the leaders is making headway anyway. It's Advanced Computer Techniques, NYC, which decides if a prospective employee is a "nice guy" -- compatible with other employees -- before worrying about his technical skill.

In the process of gathering a group of friendly programmers, ACT president Charles Lecht has never had an employee resign or ask for a raise, has fired only one. More important: he's rarely missed a deadline, never exceeded his bid price, and surprised one client by beating the deadline and turning back money. To emphasize proposal content and not the trappings, Lecht has been known to ride up to a bidders' conference on a motorcycle alongside competitors wearing Homburgs and driving Cadillacs. He turns down more business than he seeks and has a proposal success rate of better than 98%.

The result of all this nonconformity: ACT has grown since '62 from a one-man shop to a firm with 50 full-time professionals located at New York and Washington offices and in France, Italy, and Kwajelein in the S. Pacific. And the company, privately held, is making dough. Who says nice guys finish last?

RUMORS AND RAW RANDOM DATA

Eastern Airlines and IBM are developing an airborne computer which will record and analyze in-flight engine performance, predict component failure. Though this particular system will record on punched cards, airline visionaries see the day when malfunctions will be directly communicated to ground stations via satellite... Reportedly, the next Keydata system will be an 1108 instead of a 494... At a recent ADAPSO meeting, Computer Systems Institute of Pittsburgh reported that eight students have completed its programmer-training course for the blind. Most already have jobs, are said to be doing as well or better than their colleagues. Braille devices have been developed specially for the purpose ... A profitable flurry of activity at Burroughs in the last few weeks has seen the order for a B 8500 by U.S. Steel confirmed, a D 830 (about the same thing but with different configurations) for TWA about to come in, and five more orders for the B 5500... B 2000 announcement is not expected until next year... Look for Digitek to go public shortly after the first of the year...

For Digital Computers . . . A NEW MEMO PAD

The GRAFACON* MODEL 1010 is the first commercially available low-cost, two-dimensional digital graphical input system that lets you communicate with a digital computer directly in the natural graphical language of the problem at hand. Write on the MODEL 1010 horizontal tablet as naturally as you would write or sketch in a notebook... to update, compare, transform, revise, review, preview or annotate graphical information stored in the system, or monitor, filter, guide and assist the semi-automatic processing of graphical information.

The 10" x 10" horizontal writing surface (printed-circuit tablet with capacitive coupled encoding) contains one million points, each of which can communicate unambiguously with the computer in the formulation of graphical input statements. The MODEL 1010 has excellent linearity and 100 lines/inch resolution in both x and y.

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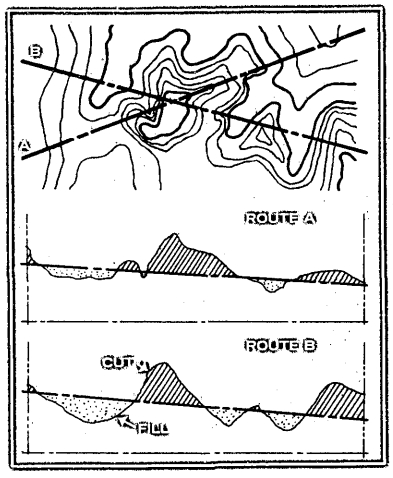

To Illustrate . . . An application for highway route location problems.

Tracings of the ground elevation contours and the tentative routes provide graphic input to a computer for CRT display of profiles and calculation of cut and fill volumes. The planner can evaluate alternatives directly, working in his graphic language.

This unique input system permits greater freedom of expression in direct man-machine communication than heretofore possible. It finds a large spectrum of applications in digital computer installations ON-LINE and OFF-LINE in conjunction with magnetic tape, paper tape and punched card systems.

FJCC ATTENDEES: See the GRAFACON MODEL 1010 ON-LINE in our Booth 502-503. You will also be able to see and use TELEPUTER†, BBN's new remote I/O system with CRT display, which provides a multiple station time shared system using low-bandwidth data links.

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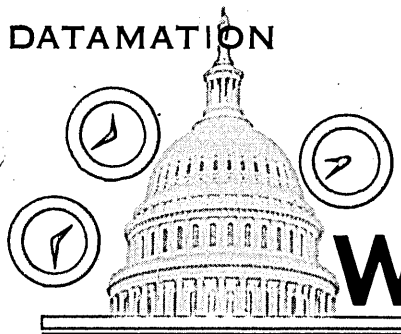
CIRCLE 20 ON READER CARD



WASHINGTON REPORT

BROOKS BILL PASSES SENATE IN SURPRISE MOVE

The Brooks Bill, H.R. 4845, which would centralize most government dp procurements within the General Services Administration, passed the Senate at 9:30 p.m. on the last day of the 1965 Congressional session. By voice vote, the Senators agreed unanimously to adopt, without amendment, the House bill, which in the previous Congress had failed to make it past the Senate Government Operations Committee. This time, an unnamed but "high" source prevailed upon committee members -- by a last-minute individual poll, not in a formal meeting -- to report the bill out to the Senate floor. Chances of a Presidential veto are considered to be -- ahem -- minimal. (For a more complete report, see p. 45.)

MORE CASH FOR COLLEGE COMPUTER KITTY

Thanks to the bounty of the 89th Congress, the National Science Foundation has jingling in its pockets $9 million with which, in fiscal 1966, it expects to fund 27 computer procurements by the nation's universities and colleges. This almost doubles its $5 million appropriation for these grants in both '65 and '64. (The NSF also received a little over a million dollars, about the same as last year, with which to sponsor research projects in computer science.) NSF awards have been a prime means of getting computers onto the nation's campuses for use by faculties and students. Counting this year, over a hundred edp facilities grants will have been made by the foundation since 1958.

Not that the academics have been overly venturesome in their proposals. An NSF program administrator noted, "We've been somewhat surprised by the conservative approach to equipment selection taken by many schools. Frankly we had hoped they'd be more willing to experiment. That, after all, is one of the purposes of our program." Another semi-gripe by NSF: reluctance of some manufacturers to grant meaningful educational discounts. Computer demand, meanwhile, continues to outrace supply. A comprehensive report on "Digital Computer Needs in Universities and Colleges," prepared for NSF by a National Academy of Science committee headed by the Univ. of Michigan's Dr. J. Barkley Rosser, is due for early release. It's expected the report will set forth the case for heightened federal, local and private support of university computing facilities, from the 1964 level of $120 million to as much as $240 million in '68.

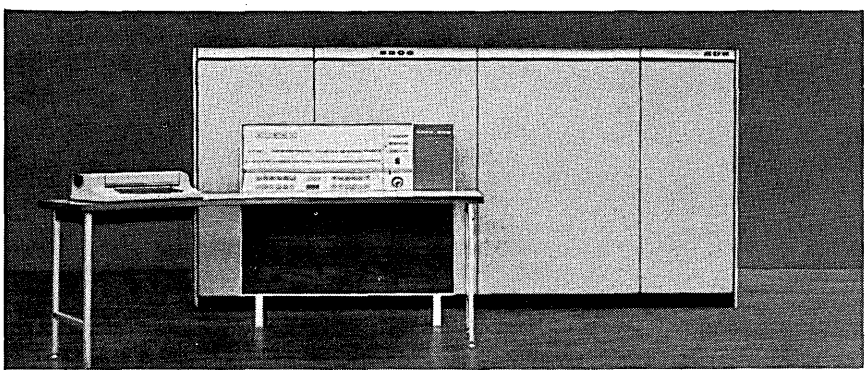
COMPUTER PROGRAMS COVERED IN COPYRIGHT LAW REVISION

The copyright law revision now making its way slowly through Congress establishes that computer programs are to be considered "literary works." While this phrase will gratify programming aesthetes, it may

(Continued on page 133)

Now you can buy 6,800,000 multiply-adds per second for only $545,000

and get this valuable SDS 9300 computer absolutely free!



Unless you're doing digital correlation and filtering, you may not appreciate this amazing bargain offer.

But if you are, you probably know that to get over 6 million multiply-adds per second out of a general purpose computer would cost you about 5 million dollars.

Up to now.

Now an SDS Correlation and Filtering Unit (CFE-1) hooked to an SDS 9300 computer can achieve multiply-add times of 146 nanoseconds (6,800,000 multiply-adds per second).

This will cost you around $545,000 ($145,000 for the CFE-1 with 12 multiply-add units, and $400,000 or so for the 9300 with assorted peripherals).

If you don't need all that capacity you can spend less, get fewer multiply-add units and a smaller computer. The basic CFE-1 consists of a control unit and one multiply-add unit and costs $35,000. Additional multiply-add units (up to a total of 12) cost $10,000 each. Besides the 9300, the CFE-1 works with the smaller SDS 930 and 925.

The basic CFE-1 performs a multiply-add operation in one computer memory cycle — 12 times as fast as the computer could do it alone. With 12 multiply-add units it makes the computer 144 times as fast.

The CFE-1 works automatically and independently, with its own direct path to memory. This leaves the CPU free to do other work simultaneously.

So if you're analyzing and interpreting sample data, involving auto-correlation, cross-correlation and filtering, you can buy ample capacity to do your job at about 1/10th what it would have cost you up to now.

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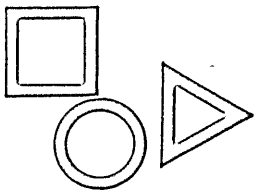


EDITOR'S READOUT

GOTHIC COMPUTER ARCHITECTURE: A GUEST EDITORIAL

Two decades of stored program electronic computing. One-and-a-half decades of serious computer marketing efforts. One decade of quantity installations of computers. It's a new and booming business by any standard. Year by year, performance per dollar and equipment dependability have steadily improved. Some users have become computer sophisticates, while other users have been provided aids that permit them to remain unsophisticated.

But what about the computer itself? It has managed to remain relatively unchanged in an organization or "architecture" sense; the Princeton-class computer (von Neumann, et al) has survived with modest embellishments.

The big changes have been in memory and circuit components, and in features like fully buffered I/O channels and interrupts. Time-sharing and multiprocessing have had early achievements with relatively minor hardware concessions. It's the age of the user and the software designer, the age of a "let's learn to use what we have" philosophy.

Throughout the brief history of computers there has been a steady flow of achievement and optimism from the research laboratories. Occasional developments such as transistors and magnetic core memories have had tremendous impact on computers, if not computer architecture. Some other highly publicized developments such as cryogenics, tunnel diodes and thin magnetic films, have matured slowly or have failed to become fully competitive. Now monolithic integrated circuits are here, probably maturing at a rate much faster than that predicted. Other microelectronic techniques which support their use are also evolving rapidly.

The potential implications of the use of monolithic integrated circuits in computers are widespread. At an equivalent component level, an order of magnitude improvement in cost, volume and reliability is in the offing. This is not to say that a computer at one-tenth the cost, one-tenth the volume, and ten times the reliability of present-day computers should be the objective of the use of monolithics. For example, cost improvements per equivalent circuit component can greatly exceed an order of magnitude if complex functional circuits are placed on one circuit chip. Circuit redundancy can also be utilized, permitting the design of super-reliable computers.

Since integrated circuit technology is well suited to memory functions as well as to register and control logic functions, the conceptual relationship of memory and processor should be reconsidered, perhaps along the lines of processor array structures.

But there has been a serious lag in the experimentation with new computer organization techniques and design tradeoffs which would utilize advanced monolithic integrated circuits to their best advantage. Computer architects appear to be in a Gothic period similar to that of the Middle Ages for mortar and stone, said to be the consequence of a period of security and complacency. Today's serious computer design efforts appear to be largely directed to the incorporation of stained glass and flying buttresses, rather than a fundamental review of design concepts.

—LOWELL AMDAHL

AUTOMATED SECONDARY STORAGE MANAGEMENT

by F. B. MacKENZIE

During the past several years, the idea has been advanced that the management of secondary storage should be handled automatically by the computing system. Basic trends in computing system design dictate that automatic management *must* be provided if the design objectives are to be practically realized. These trends are well noted elsewhere.[1]

The use of the term "computing system" here refers to an operational coupling of hardware and a higher-level-language programming system. The application programmer should view his entire computing system as a *machine*. As such, it has gross properties with which he should become familiar. The structure of the hardware-language programs is implied by his higher-level language usage. That he should achieve the necessary familiarity becomes more evident as these programs come ever closer to:

(1) exceeding the physical memory capacity of his "machine's" hardware component, or
(2) being economically unfeasible because of excessive running times.

the single level store

Many names have been applied to suggest the concept of automatic secondary store management, especially the term "single level store." The use of such names implies that secondary memory stores exist and are used *by the computing system* as back-up to its primary memory store. Program segments and internal data are moved about, as necessary, between the primary and secondary stores on demand—as these demands are detected by the computing system. The application programmer need think only in terms of the logical space requirements of the programs and their data. He does not explicitly direct movements between the different memory levels. Computing system action to use the backing store is automatically invoked if an execution situation arises in which logical space requirements cannot be satisfied in the primary store alone.

Automatic secondary store management is provided by the Burroughs B 5500 computing system. This article explains the operation of the basic control mechanism employed in the computing system to invoke the store management process, and reports observations which demonstrate its effectiveness.

The disc-based programming systems for the B 5500 operate in a hardware memory complex with from:

4 to 8 modules of 4K words each of core memory,
1 to 100 modules of 1.2 million words each of disc file storage (20 ms average access), and
0 to 2 drums of 32K words each (8.3 ms average access).

The modular availability of the (primary) core memory is sensed automatically as the system is initialized. The backing store size is specified as an installation-controlled parameter as the system is loaded. If drums are present, they may also be consigned to backing store use. The single level store, then, includes all of core storage, and part of the secondary memory. A program and user file library is also maintained on the disc file and managed by the programming system.

language levels

All programming for this computing system is done in one of its three higher language levels. Applicational programs are written in B 5500 Extended ALGOL, COBOL, or FORTRAN. The programming system components themselves are written entirely at the Extended ALGOL level. The

[1] *"Design of a Scientific Computing Facility,"* Wagner and Granholm, *Proceedings of IFIP Congress 65*, page 288: ". . . The requirements of general purpose executives and multicomputer, multistore Continuous Flow Systems, together with the great growth in higher level languages, all will bring powerful pressures to bear on this problem. . ."

Mr. MacKenzie is manager, Programming Systems Development, ElectroData Div., Burroughs in Pasadena, Calif., responsible for the design and production of program systems for the B5500 and B300 on-line teller system. He was formerly dp manager at ElectroData and computing group leader at the Southern California Cooperative Wind Tunnel of Cal Tech. He received his BS in Mathematical Statistics from the Univ. of Washington.

Disc File Master Control Program (MCP) is written in ESPOL—a special-purpose variant of Extended ALGOL which was defined to permit the expression of control algorithms and other important miscellany necessary for the construction of this operating system and the intrinsic functions of its compilers.

All the remaining programming system components are written in Extended ALGOL—the same language available to application programmers. With respect to this explanation of the employment of the single-level store concept, the following should be remembered: this computing system's compilers are but Extended ALGOL programs. The action described is the same, be it for a compiler or an application program.

segmentation

Segmentation of programs is implied by the programmer. The Extended ALGOL compiler automatically segments at the language's block level, the COBOL compiler at the paragraph level. The compilers do *not* allocate storage for their generated code, which is placed in the disc file library either temporarily or permanently, depending on the contents of the job call control card. Instead, storage is dynamically allocated by the MCP at run time. Core storage for program segments or arrays is not actually allocated until some execution reference is attempted. Program segments which are not referenced do not have core storage allocated for them. Similarly, even though an array is declared in a program, storage is allocated for it only on a row-at-a-time basis as the first reference to an element is attempted in the execution. The operating principle is simple. Incremental core storage is bound to a given program only as dynamically required. Program or data space is allocated to the program only as it is actually needed, and is returned when the need no longer exists.

storage allocation and the prt

Now, this conservative means of storage allocation employed by the MCP is not accomplished without considerable assistance derived from the organizational features of the hardware's processors. Each program in execution has associated with it a Program Reference Table (PRT). The MCP arbitrarily allocates core space for this one-dimensional PRT array, and constructs the array as the program's first segment is initially loaded from the disc file library. The MCP programmatically sets a processor register to point to the basic core address of the PRT. One may visualize the PRT as a part of the interface between a specified program, the MCP, and the processor.

Each program segment and array of the program is represented by a word entry, called a descriptor, in the PRT. A certain bit position in each descriptor is called the presence bit. The MCP sets this bit on or off, depending on whether the represented entity is or is not present in core memory. If the presence bit is on, then the MCP also will have set another field in the descriptor to point to the base core address of the entity or an address where further descriptive information begins. (For example, in the case of a multidimensional array, the field is set to point to the base address of an array of descriptor-like words).

All hardware language references to program segments or arrays are made relative to the register in the processor which points to the base address of the PRT. If the presence bit of the encountered descriptor is on, then the linkage to another core address is permitted by the processor. If not, a processor interrupt occurs which causes all of the program's state variables, including the contents of the PRT base register, to be automatically stored.

more mcp action

It falls to the MCP, then, to make the necessary entity —program segment or array—present in core memory. The MCP attempts to allocate storage for the entity from the list it maintains of available core storage. If the allocation cannot be made because the necessary amount of space is not directly available, then the MCP appropriates a sufficient amount from among that core storage previously allocated to other entities. Of course, in so doing, the MCP does all necessary presence bit bookkeeping for the entities from which the storage was taken—no matter to which program the entities belong.

If the appropriated space previously was allocated to a program segment, then the core copy of the program segment is simply "abandoned" since the copy was originally taken from *somewhere* in the disc file library and never subsequently altered. If the appropriated space previously was allocated to an array row, then this array row must first be transferred by the MCP to *somewhere* in the backup memory complex since the integrity of this informa-

tion must be maintained.

With space now available, the MCP either:

(1) brings in the required program segment from *somewhere* in its library, or
(2) brings in the required array row from *somewhere* in its backup memory complex, or
(3) for the first attempted reference, simply initializes core space for the required array row.

Parts of other programs may have been executed by the processor during the elapsed time span of this presence bit operation while the storage movements were being conducted. A very suitable control of concurrent processing operations is maintained by the MCP to utilize such available periods. When the interrupted program is subsequently reinitiated by the MCP, all state variables are automatically put back into their proper places in the appropriate hardware registers. The presence bit in the descriptor which originally caused the interrupt has now been set "on." The processor permits the required linkage through the PRT to be completed, and processing commences again from the interrupt point.

It can now be readily deduced that all the *somewheres,* anywhere in the total memory complex, are determined by the MCP. The need to make the determinations dynamically is signaled by hardware interrupts.

It should also be apparent that the hardware organization, which so helpfully assists the process, does extract core memory accesses as the price for its assistance. However, overall throughput objectives, which properly consider programming costs, are well served by the PRT concept. Many other processor features exist which, coincidentally, temper the effect of memory accesses for the PRT interface. For example, the program strings are represented in syllables, packed four to a word. A built-in stack in memory is topped by the two registers between which binary arithmetic operations are defined.

release of restraints

What does all this mean in this context? Simply stated, it means that two things are made possible. First, very large programs can be executed without any explicit control of the secondary stores being expressed. "Very large" refers to situations in which the logical space requirements of a program either marginally or grossly exceed the amount of core memory available. Second, the performance level—i.e., program running times—may be varied, perhaps substantially, as core memory modules are added to, or removed from, the operating memory configuration within the limits mentioned previously.

The flexibility of operation, which may be obtained without any programmatic change, is truly a bonus factor. With conventional computing system organizations, additions to the core memory configuration become usable, in the applicational processes, only as new programs are prepared to use the additional memory or as existing programs are modified—if modification is deemed practical at all. With the B 5500 computing system, the benefit of more available core memory may be realized *immediately* for existing programs without any reprogramming—if that additional memory space can be effectively used by the programs. Furthermore (and perish the thought), operations may be conducted, although perhaps at reduced performance levels, even though failure reduces the number of available core memory modules below that number normally present in the configuration.

An effective single-level store implementation offers much of value which can be realized by intelligent use. It promises to reduce the cost of preparing programs which, without it, might be constructed to explicitly move program segments and data about between different memory levels. It promises to make less restricted, in applicational scope, large programs for which primary memory requirements are very much data-dependent. Furthermore—although the situation may not seem obvious—it promises to make much less restricted the conditions under which a mix of programs may be processed concurrently.

first observation

Observations on two sets of programs are presented, in the following paragraphs, which demonstrate the effectiveness of the single level store implementation produced in the B 5500 computing system. The first set of two programs was run three times; only the operating conditions were varied on the successive runs. Specifically:

(1) The programs were run serially, using a single processor and 16K of core memory.
(2) The programs were again run serially, using a single processor and 24K of core.
(3) Finally, the programs were run concurrently using two processors and 24K of core memory. (A second processor may be employed if it is present in the hardware configuration. In that event, both processors share the same common memory complex. The two processors are never assigned to work exclusively on distinct programs. Programs are "mixed" and processors are assigned by the MCP to do a bit of this, a bit of that, and so on).

The program running times were observed for each of the three operating conditions. A brief qualification of the total observation is made, however, before the running times are presented. The backing store was made up of 450,000 words of disc storage and two magnetic drums. Either of the two programs runs nearly processor-bound in the serial operating conditions.

One program was the ESPOL compiler, which was called upon to compile an experimental version of the MCP. The ESPOL compiler itself occupies about 6,100 words of storage in the same disc file library used for the storage of applicational programs and files. The data to the compiler was the symbolic MCP—about 12,000 card images.

The other program in this first set was the Extended ALGOL compiler, which was called upon to compile an experimental version of itself. The Extended ALGOL compiler occupies about 8,000 words of storage in the disc file library. The data to this compiler for the run comprised about 9,000 card images.

Many thousands of words of internal data were generated during the execution of each of the two programs. In summary, the total primary storage demands were thus quite substantial for each program.

The observed running times for these two programs are presented in Fig. 1. Note that, for the serial operating conditions, only slightly less total time (681 vs. 703 seconds) was recorded for the 24K core memory case than that recorded for the 16K. This fact supports the conclusion that either of the programs, by itself, would run "comfortably" in a 16K configuration. (Although the times are not shown, it has been observed that three to five times longer is required to process very similar data when these compilers are run in a 12K core memory).

Recorded on the third line of Fig. 1 is the total elapsed time which was required to run the two programs concurrently employing two processors and a 24K core memory. The elapsed times observed for each program are given within parentheses, since in this operating condition they are not expected to add up to the total time. The total time to execute both programs was only about 6% greater than the time observed for the longest of the two programs run serially in a 16K core memory.

As noted above, either program runs nearly processor-bound. Only a slight reduction, perhaps 10% in total time, might be anticipated if the two programs were run concurrently employing a single processor and 24K core memory. Of course, a substantial reduction of total time should be anticipated when two processors are employed, if enough core memory is available. Thus the primary signi-

Fig. 1

Operating Condition	TIME IN SECONDS Compile ALGOL	Compile MCP	Total Time
1. 16K Serial	269	434	703
2. 24K Serial	261	420	681
3. 24K Mix	(296)	(458)	458

Fig. 2

```
PROCEDURE ACCUMMATRIXMULT (A, B, C, I, J, K, P);
  VALUE I, J, K, P; INTEGER I, J, K, P;
  ARRAY A, B, C[0,0];
  COMMENT    THE MATRIX OPERATION  C := A × B + C   IS
             PERFORMED AS DEFINED FOR SIZE DECLARATIONS
                A[0:I,0:J], B[0:J,0:K], C[0:I,0:K]

             THE PARAMETER P SPECIFIES THE NUMBER OF ROWS
             OF B TO TAKE AS A PARTITION AS THE ROWS OF A
             AND C ARE PASSED (ALTERNATELY TOP-TO-BOTTOM
             THEN BOTTOM-TO-TOP) AGAINST SUCCESSIVE PAR-
             TITIONS OF B, WHILE ACCUMULATIONS ARE BUILT
             UP IN C.  LAST PARTITION BY P (AN INTEGER IN
             THE ZERO-ORIGIN SET) IS ADJUSTED TO FIT DE-
             CLARED UPPER BOUNDS IF NECESSARY;

BEGIN INTEGER DL, DR, P1, P2, P3, TA, TB, TC; REAL SPOT;
  P1 := 0; P2 := 1; P3 := I;
  FOR DL := 0 STEP (P+1) UNTIL J DO
      BEGIN
        DR := DL + P; IF DR > J THEN DR := J;
        FOR TA := P1 STEP P2 UNTIL P3 DO
            FOR TC := 0 STEP 1 UNTIL K DO
                BEGIN
                  SPOT := C[TA,TC];
                  FOR TB := DL STEP 1 UNTIL DR DO
                      SPOT := A[TA,TB]×B[TB,TC] + SPOT;
                  C[TA,TC] := SPOT
                END;
        IF P1 = 0 THEN BEGIN P1:=I; P2:=-1; P3:=0 END
                  ELSE BEGIN P1:=0; P2:= 1; P3:=I END
      END
END ACCUMMATRIXMULT;
```

ficance of this first set of observations is not the substantial time reduction recorded. It lies, rather, in the fact that the reduction was realized when only 8K of additional core memory was made available.

second observation

The impact of this first observation on the set of two programs will be reinforced, if one can gain a better insight of the computing system action required for the primary and secondary store manipulations. As a reinforcement, the second observation provides an illustration of the single-level store action on a simple program, in a case where the data storage requirements grossly exceeded the amount of available core memory.

The program performs a logically simple operation with matrices ($C := A \times B + C$). Better algorithms undoubtedly exist which should be used were the intent literally one of demonstrating matrix operations. The illustration uses this readily understood matrix operation, as a device, to expose a required data-manipulation situation not uncommonly encountered in much more complex programs.

The heart of this illustrative program is the procedure of Fig. 2. In constructing this procedure, advantage was taken of two very simple properties of the computing system.

(1) A simple variable can be accessed more rapidly than a subscripted variable. Hence, the local simple variable SPOT was used to overall advantage, even though a trade-off of extra inner-loop operations was required.

(2) Array overlays are made on a row basis. The procedure can be used with matrices for which the data space requirements exceed core memory size. Hence, use was made of what might otherwise seem to be a peculiar partitioning scheme.

This program was run and timed with varying core memory configurations while using a disc-only backing store of 450,000 words. The operation on the matrices was performed several times during each run by making a programmatic variation of the matrix sizes. A set of logical data space requirements was created which ranged from within to significantly beyond each core memory configuration. Thus, times were obtained for this set for each core memory configuration.

A set of base times was obtained for comparison purposes—one base time for each logical space requirement. The base times were defined to be those lower limit times predictable if an assumption could hold. The assumption was that somehow the core memory configuration could be extended sufficiently beyond the 32K physical limit to a size such that all logical data space requirements could be statically accommodated in core memory (i.e., no backing store action required). The effect of pretending that sufficient core memory was available was created by "dummying" the procedure to hold all logical data references at parametric values. The "dummy" program was run and the set of base times was observed. A comparison then was made between the times actually observed and the appropriate base times, as explained below.

Two devices were used to simplify the analysis of the comparison of the observations and to conserve the hardware time required to make the total observation.

(1) Calls on the procedure were always made using square matrices. The dimension of the square was varied from 59 in steps of 30 through 179, thereby creating logical data space requirements of 10,800, 24,300, 43,200, 67,500, and 97,200 words, respectively.

(2) Zero-value matrix elements were always used. Prior to making the call on the procedure, all elements of the matrices A, B, and C were always initialized to zero—thereby leaving the rows of the various matrices lying *somewhere* in core or the backing store memory.

The reasoning which led to the choice of the second device requires explanation. The hardware multiply time is minimal for the special case where either the multiplier or multiplicand is zero. The choice of zero-value multipliers not only allowed an expedient reduction of the sum of all multiply times, but also provided a conservative basis from which to state the comparisons. That is, the incremental differences, of the actual times observed over the base times, are invariant as to hardware multiply times, and will be stated as a percentage of the base which includes these multiply times. Thus the percentage increases will be larger—hence a more conserva-

tive basis—than would have been observed were representative (non-zero) multipliers employed.

The percentage time increases for the observations are given in Fig. 3. For example, an increase of 16.9% over the base time resulted as the 97,200 data word case was run on 32K hardware. For all observations, the actual parameter ENTIER (J/4) was furnished for the formal parameter P. The procedural action, therefore, was to partition into four pieces. (When base times were obtained, however, the integer 200 was furnished as the actual parameter).

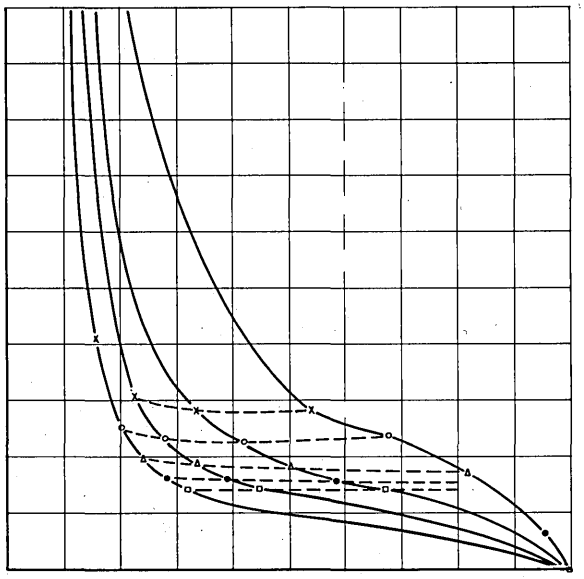
On an absolute basis alone, the observations provide a very substantial demonstration of the effectiveness of the computing system action on this particular illustrative

Fig. 3

Matrix Size	Data Space	CORE MEMORY SIZE 16K	20K	24K	28K	32K
0:179	97,200	44.4	28.0	22.3	18.7	16.9
0:149	67,500	34.2	26.2	22.3	19.2	17.5
0:119	43,200	32.6	26.8	22.2	19.6	18.5
0:89	24,300	34.8	30.0	22.9	11.5	4.3
0:59	10,800	13.5	6.2	6.2	6.2	6.2

PERCENTAGE TIME INCREASES
(above base times)

Fig. 4



problem. Certainly, smaller percentage increases would have been noted for any discrete observations, had special programs been tailor-made to minimize increases at non-trivial points in the Fig. 3 array. The matrices could have been set up as temporary files in the disc file library. For any point minimization, use could have been made of the disc READ, WRITE and SEEK statements available in B 5500 Extended ALGOL. The effect of such usage would have been to buffer most of the required data movements back and forth between the disc file library and core memory.

Given the observations, certain important properties of the computing system action on this particular problem become apparent with a bit of manipulation and analysis. The percentage increases are due to two factors. Obviously, the substantial part of each was due to the extra computing system time used to perform the storage allocation and data overlay necessary because of the sizes of the matrices. A lesser factor of each increase was due to the extra processor time required by the loop mechanics of the partitioning scheme.

Fig. 4 is a graphical presentation of the observations, made subject to the following manipulation. First, the percentage time increases reported in Fig. 3 were adjusted to a new base, which included the extra processor time required by the partitioning scheme (the adjustments were made in a manner very similar to the method of establishing base times previously explained). Then the adjusted percentage time increases were plotted against yet another percentage base. This latter base was constructed by calculating the ratio of core memory available, as each observation was made, to the amount of space logically required for the matrices, the program string, and those few parts of the MCP always fixed in core memory.

In Fig. 4, curves have been faired through the plotted points, for each constant logical space requirement, observed as the program was run with the various core memory sizes. One indication of an important property should be noted: a relatively broad threshold exists for each specific core memory configuration. These thresholds range from about 25% to perhaps 75% or 80% on the horizontal axis and are indicated by broken lines. On these thresholds, the percentage increases remain relatively constant for the various logical space requirements. For example, about a 15% time increase was observed above their respective base times for each of the 43,200, 67,500, and 97,200 word cases when these were observed running with 32K of core memory. On these thresholds, then, the computing system "overhead" time, for the single level store action, is a constant multiplier of the appropriate base time and is *independent* of the percentage relationships the actual core memory configurations bear to the logical space requirements.

This is indeed an interesting and important property. Even though the simple program was prepared for illustrative purposes, it seems likely that the illustration at least typifies some significant characteristics of a broad class of problems.

In a different way, each of the two sets of observed programs demonstrate the effectiveness of the B 5500 single-level store implementation. The observations on the first set, reported in Fig. 1, are probably the more significant from a practical viewpoint. The observations on the second set reinforced the demonstration of effectiveness and, hopefully, did it in an illuminating manner.

epilogue

If the reported observations have merit to the extent implied, then sobering, thoughtful review of established trends should be made by computing system designers. The time *is not* past when attempts to innovate basically new processor organizations can bear fruitful results. The trend to place bigger and bigger, more expensive primary memories on computing systems *need not* be anywhere near so pronounced. "Big" programs may need a million words of logical space. The computing system needed to execute their processes effectively, however, need not have anywhere near that much primary memory capacity. Furthermore, the programs themselves need not be as costly to produce, nor constrained by the implications of the static memory allocation processes currently employed.■

INTEGRATED CIRCUITS FOR COMMERCIAL COMPUTERS

monolithic vs hybrid

by WILLIAM H. RICHMOND

Only a little more than a year ago monolithic integrated circuits moved out of the stratosphere of high-priced military systems and into the commercial computer cost range. Today their use in large-scale business and industrial computers is common design practice.

Competition and technological breakthroughs in production techniques have overcome the cost barrier. Integrated circuits meeting rigid military specifications are now available over the full military temperature range at lower prices than many large-volume silicon transistors were two or three years ago.

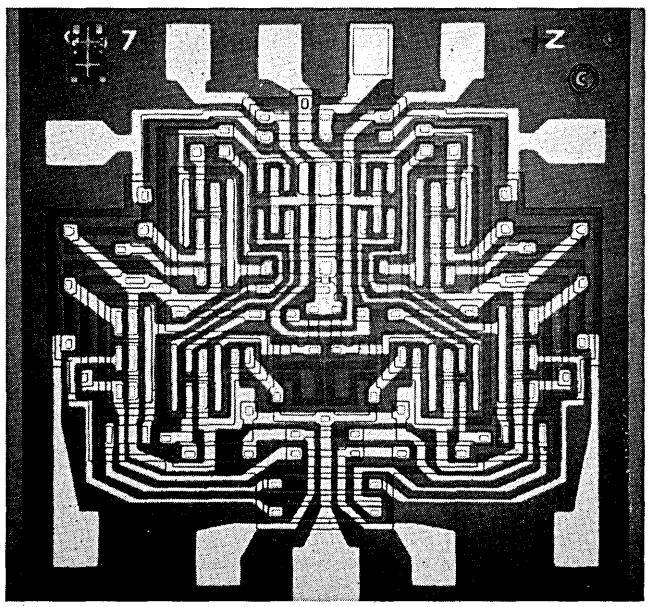
At present there are two distinct approaches to the manufacture of integrated circuits, the monolithic and the hybrid integrated circuit.

the monolithic integrated circuit

In this approach, a silicon wafer 1.5″ in diameter is exposed to a series of diffusions through masks of appropriate pattern to form 200 to 1,000 circuits per wafer, depending on the size of the circuit. The components of each circuit are intraconnected on the surface by aluminum metalizing brought out to relatively large "bonding pads" at the edges of the circuit for easy attachment of wire connections to the ouside world (see Fig. 1).

After each circuit has been tested to rigid electrical specifications, a diamond scribe scores between the circuits, which are then separated into uniform square dice. Each acceptable die is mounted on a gold-plated header (see Fig. 2) using a gold alloy preform. Fine gold-wire leads are attached to make electrical connection to the outside world by ultrasonic bonding, and each lead is spot-welded to a header post. A final visual inspection takes place at this time to be sure the circuit has not been damaged during the die-attach process. If it passes inspection, it is cleaned and hermetically sealed by welding a protective cap to the header.

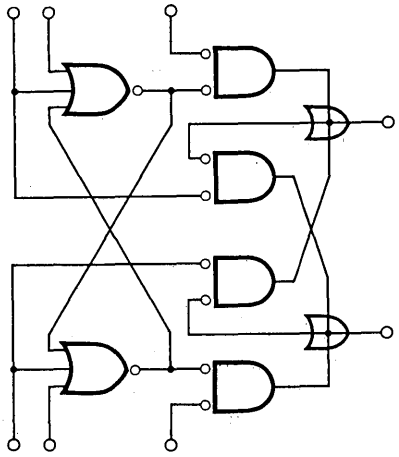
Fig. 1 Fairchild CTμL957 Dual-rank flip-flop die. White areas are aluminum metalizing.



The packaging procedure described above applies specifically to the TO-5 package (Fig. 3). For extremely high-density military applications the flatpack (Figs. 4 and 5) is used, and for commercial computer use the rugged dual inline package (Fig. 6) was developed at Fairchild.

After sealing, the integrated circuits are subjected to a series of rigorous environment tests, including hermeticity tests, temperature cycling and centrifuge acceleration tests. Each circuit is then given a final electrical classification test, and any deviations from specification (fallout) are removed at this time.

Fig. 1-b Logic diagram of CTμL957 dual-rank flip-flop.



Both "off the shelf" and "custom" circuits (i.e., circuits designed specifically for one customer) are available. Unlike "off the shelf" circuits, which are usually available on request, custom circuits require 6 to 12 weeks for circuit design, breadboard, masking, diffusion, etc., before delivery of the first prototypes.

the hybrid integrated circuit

In this approach, discrete transistor and diode dice are mounted on a ceramic or glass substrate metalized to form interconnecting paths for the circuit similar to a

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printed circuit board, and resistors are deposited by thin-film techniques. Additional inter-die connections are made by lead bonds, and leads are spot welded to header posts in the manner described above for monolithic integrated circuits.

comparison of monolithics and hybrids

Monolithic integrated circuits are inherently low in cost because of the batch processing and the amount of circuitry that can be put on one die. Furthermore, in high-speed logic circuits the performance available with today's monolithic circuits is equal to that obtainable in either discrete-component circuits or hybrids.

Fig. 2 TO-5 header minus the protective cap. Integrated circuit die in center of header. Fine wires can be seen connecting die to posts.

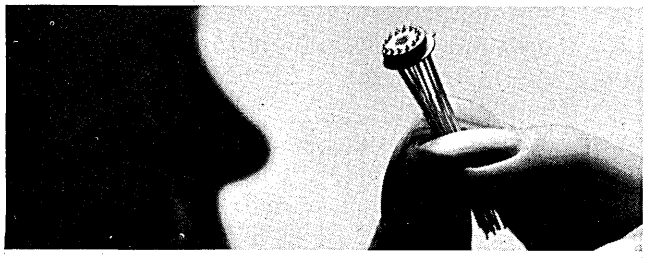


Fig. 3 TO-5 can

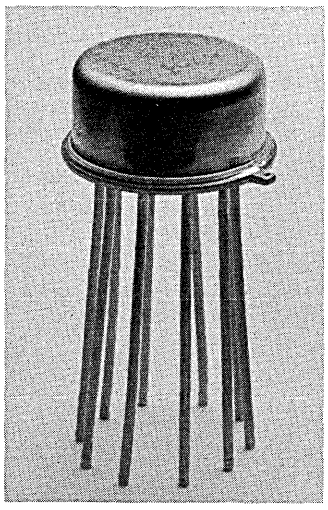


Fig. 4 Flatpack

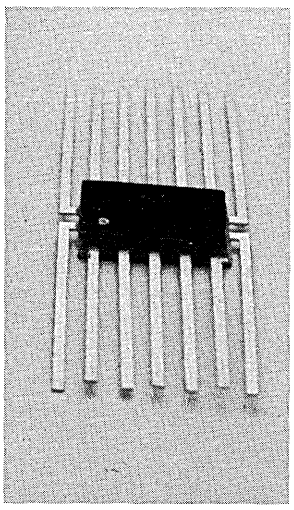
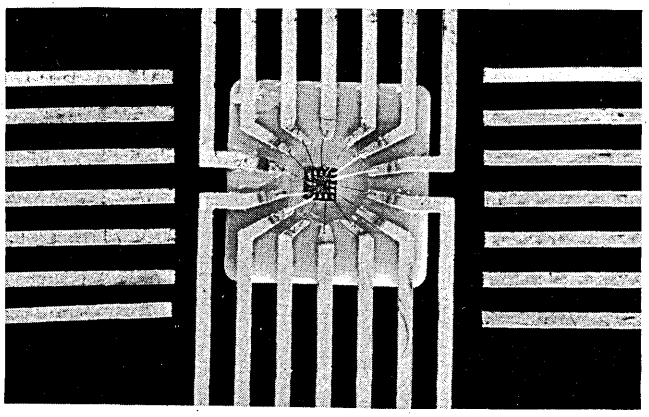


Fig. 5 Fairchild ceramic flatpack, Cerpak, minus upper half of ceramic sandwich. Shows integrated circuit die and connecting wires.



Despite these marked advantages of monolithic integrated circuits, however, there are certain applications in which hybrid circuits are preferable. For example:

(1) Circuits that do not exist as "off the shelf" monolithics and are not required in sufficient volume to justify the tooling costs and long delivery schedules of the custom monolithic circuit. A custom hybrid circuit can be brought from the initial circuit design stage to prototype parts in a much shorter time.

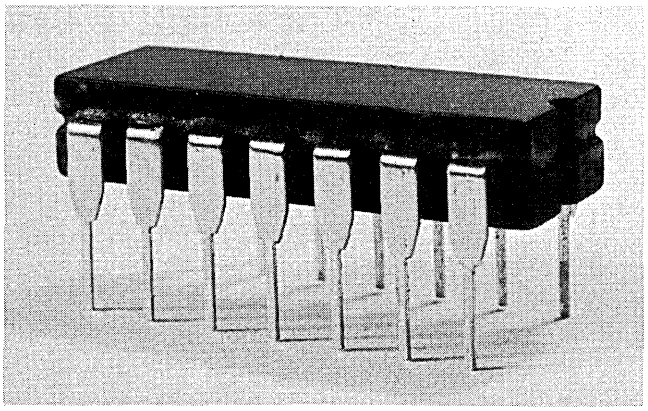
(2) Circuits with voltage and current requirements exceeding those presently available in monolithic integrated circuits—memory drivers would be one example. In such cases hybrid circuits offer a very definite advantage.

The biggest disadvantages of the hybrid are in cost and yield. Since each transistor and diode must be physically attached to the substrate, and each lead bond made individually, there is a great deal of hand labor involved in making a hybrid circuit. The cost per circuit function may therefore be considerably higher than in either a conventional discrete component or a monolithic integrated circuit. The problem of yield enters the picture in that the more separate dice and lead bonds used the greater the risk of a serious flaw in the final circuit.

history

Impetus for the development of the integrated circuit came originally from the desire to lower semiconductor prices. The monolithic circuit was a natural outgrowth of the Fairchild-patented planar process, by which hundreds of transistors were diffused into a single wafer and then separated for subsequent reconnection into discrete-component circuits. It was believed that the cost per transistor could be greatly reduced by diffusing and interconnecting several transistors into a circuit within a single die. This approach seemed particularly promising since die sizes smaller than about 0.030″ square could not be handled economically at that time (1959), yet the active area (i.e., the transistor) was much smaller. The active area for a switching device, for example, was approximately 0.009″ in diameter.

Fig. 6 Fairchild Dual inline package



Several severe problems arose, however, in attempting to fabricate circuits monolithically, and many entire wafers were processed with zero yield. Typical of the problems were those associated with scribing. Common practice in transistor production was to scribe from the back of the wafer. Although this method worked nicely for transistors, when it was tried with integrated circuits it was found to cause severe scratches in the aluminum interconnections, resulting in open circuits at final test. The answer to this specific problem was topside scribing with the addition of more in-process visual inspection steps.

The scribing problem was just one of many that had to be resolved before the economic advantage of integrated circuits could be realized. It is estimated that at least 50% of the development dollars spent by major semiconductor companies active in integrated-circuit manufacture were pumped into solving these problems. Today they have all been resolved, thanks to a series of technological breakthroughs combined with the rigid quality control now extended to each step of wafer processing and assembly.

Even after costs were substantially reduced, however, they were still too high for the commercial computer market. Furthermore, since the military—the major integrated-circuit market—in general preferred low power to high speed, the performance of integrated circuits, by commercial standards, was not adequate. Technology had progressed from masking tolerances permitting line widths of 1.0 mil to a new level of 0.5 mil, making possible more complex elements for the same die size, but diffusion schedules (temperature, pressures, and times) were similar to those now used for low-speed logic transistors, and testing was archaic by today's standards. Common test equipment consisted of small functional black boxes which could perform only a severely limited number and type of tests. The accepted packages for the industry were the standard TO-5, 8- and 10-lead cans, and, for ultraminiaturization, the flatpack, neither of which met commercial requirements for rapid automatic assembly, ease of handling, and low thermal resistance.

Progress continued from 0.5-mil to the 0.25-mil technology in use today in production circuits, and improvements in diffusion were made. Today's factory diffusion schedules for integrated circuits are similar to those of the highest speed silicon transistors. With these technological advances, the industry arrived at the point where it was ready for the commercial computer market. However, it arrived at this point without being fully aware of the fact, and without an adequate product for the market.

present industry status

Announcement in May 1964 of low-cost integrated-circuit gates for $2.55 and a flip-flop for $6.50 heralded the entry of integrated-circuit manufacturers into the commercial computer market. Subsequent investigation into the needs of this market resulted in a product specifically designed to meet these needs. A series of mutually compatible high-speed elements—the Fairchild CTμL family —was introduced in a rugged low-cost package (the dual inline shown in Fig. 6), which can be easily handled and automatically inserted if necessary. Thermal resistance of the package is low enough to handle the high power drain of high-speed commercial circuits.

Other circuits presently being designed include both advanced factory technologies and future R & D technologies. The integrated-circuit industry is devoting a very large portion of its effort to commercial computer devices.

The general trend in this new generation of computers is not only a change from discrete components to integrated circuits, but to the design of computer systems with higher access and processing speeds as well. This means that not only must integrated circuits be competitive in cost with former designs; they must also offer higher performance. In addition, the buying trend has been toward a 50% split of "custom" to "off the shelf" circuits.

New techniques in production processing and testing are constantly being implemented for still further cost reduction. Typical is the improvement in test equipment. Whereas the early test boxes could test 100 units per hour, today's equipment tests 20 times that volume in the same time.

According to Fairchild's market research, the actual number of integrated circuits that will be purchased this year by the commercial computing industry is a small portion of the total sales. By 1970, however, this volume will be nearly 200 million dollars. Out of a forecast total of 900 million dollars for the entire semiconductor industry, this figure is impressive indeed.

cost factors in using integrated circuits

Integrated-circuit costs are governed by three factors: die sort yield; classification yield; volume; and circuit complexity.

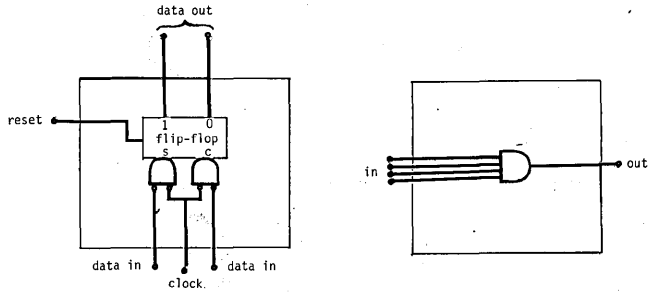
In die sort, a complete electrical test is performed on each die before scribing and separation. Dice that do not meet the electrical criteria are marked and discarded after separation. The yield at this point depends on die size and the electrical specifications. Large dice tend to produce lower yields as well as fewer dice per wafer since imperfections in the wafer that occur in the active areas cause that die to be a reject. Electrical specifications that limit acceptable devices to those whose characteristic values fall within a very narrow range also account for yield loss at die sort. For example, if devices with a range of current gain from 40 to 120 are normally produced, specifying a minimum value of 80 would severely limit the die sort yields.

Classification is the final test prior to shipping. In general, the fallout to class is quite small compared to that at die sort, since most of the yield loss has been absorbed at the die-sort stage.

The fallout at classification is generally due to open circuits, rejects for insufficient hermeticity of package sealing, and other small yield losses due to electrical specifications. In some cases, however, a specification may be tight in an area that cannot be tested at die sort. When this happens, a large fallout may occur at classification. This is undesirable since by this stage the total material and labor costs have been incurred and devices are completed and packaged.

Semiconductor operations tend to have a very high fixed overhead compared to that of the equipment manufacturer. By amortizing this overhead over a large quantity of units, the total cost can be reduced. Another factor which applies to volume is the standard learning curve. This applies especially to difficult circuits. History has

Fig. 7 J-K flip-flop 4-input gate



shown that many circuits that seemed difficult at the outset of a program have become high-yield items thanks to technological improvements in device characteristics as well as development of new, lower cost manufacturing techniques. For these reasons large-volume, long-term procurement programs are very desirable for both supplier and customer. This statement may seem academic, but it is especially true of integrated circuits where low cost is a prime consideration.

Circuit complexity is another important cost factor. The size of the die, to a degree, controls the complexity of any given circuit. With present technology, the most eco-

nomical die size is 45 to 50 mils square. (This is a general statement, which, as we shall see later, is not always true.) A 45-mil-square die can be as simple as a 4-input gate or as complex as a full J-K Flip-flop (see Fig. 7). However, with a simple gate there will be much wasted space on the die, since the limit in die size is dictated by the bonding pads rather than by the actual circuitry. On the other hand, a circuit such as a J-K Flip-flop with five times the complexity of the simple gate would, with proper layout, require the same die size. Economically it is desirable to put as much function as possible on a single die.

memory elements

A relatively new area in which integrated circuits are finding application is memory. High-speed, scratch-pad, control and buffer memories of 256 to 1000 words using integrated circuits are now practical. Fairchild is presently working on and has delivered prototype quantities of several different memory cells.

Basically these cells range from 6 to 16 bits per chip with various organizations to suit the specific customer requirements. In most of these cells the decode circuitry is external to the die. The main reason for not incorporating the decade circuitry is flexibility and economy, since more bits can be incorporated in the same size die.

Integrated-circuit memory cells are an example that violates the basic economic rule of small size die. The elements that have been produced to date, using existing factory 0.25 mil technology, range in size from 70 to 95 mils square. The 95-mil-square die is presently the limit of existing production camera lenses. Die sizes beyond 95 mils tend to produce fuzziness or poor mask resolution at the edge of the die.

The die size rule can be violated with memory elements because:

(1) They are relatively simple circuits. Although they require precise layout, they are merely latches (flip-flops) and generally do not have complex electrical specifications that cause fallout. The time required for the flip-flop to change state (latch time) is inherent in the process and hence batch controlled.

(2) Most of the active circuitry (transistors, diodes, etc.) is in the center portion of the die with aluminum interconnections running around the periphery of the die. Under these conditions, die-sort yields tend to be high since the true active area is on the order of only 50 mils square.

The significant advantages these memory elements offer are nondestructive readout, output signal levels compatible with the processor logic, high speed (typical write times are 25 to 40 nsec with equal read times), and low cost. The cost per bit in production quantity ranges from $1.00 to as low as $0.40. This is more expensive than core and less than present thin-film price, but neither of these can approach the performance of integrated-circuit memory elements. Bit costs of $0.20 in large quantities are forecast by 1967.

future integrated-circuit technologies

The circuits for the fourth-generation computers (which can be expected in 1970) will be very complex functional arrays. While today's practical logic circuit has as many as three 3-input gates or a single J-K flip-flop function on a die, future circuits may have up to 500 gates. Practical complexity will range from 50 to 500 gates per die as a function of switching time requirements. Because of power dissipation, the higher speed circuits will be limited to fewer functions than will slower, hence lower power circuits. However, this will not be a direct trade-off as we understand the relationship today, because capacities associated with today's circuitry (i.e., P. C. line capacities, load capacities, etc.) will be reduced. There will be more interconnections on each die, and, with smaller transistors, the load and line capacitance will be reduced. (The required power level for an output device that drives other logic segments on the same die is substantially less than for one that drives logic elements on other dice.) High-speed circuits in the one-nsec range are obtainable with much less driving power than we presently work with in laboratory devices.

Circuits with complexities of 36- to 72-bit shift registers are within the grasp of future technology. The basic masking technology for this complexity level is 0.1 mil mask tolerance and multilayer interconnections. The 0.1 mil mask tolerance makes possible a practical 2–3:1 reduction in overall device size.

One of the major limitations in today's technology is inter-chip component connection. Present technology limits intraconnections to phosphorous cross-unders (diffused) and aluminum crossovers (intraconnections) across the top of the oxide, which in turn limits the amount of circuitry on a single die.

Multilayer intraconnections are analogous to multilayer P.C. boards. The first aluminum intraconnections would be made over the original oxide as is done today. A dielectric material is then deposited over the complete wafer, including the first layer of metal. On top of this dielectric the next level of intraconnections would be made with appropriate etching through the dialectric to make the necessary connections between circuit elements.

The technology to manufacture these more complex circuits is not just a concept—it is a reality, presently being refined in R & D. To use these more complex integrated circuits to their full advantage will require careful consideration on the part of the commercial computer manufacturer. Some changes in machine concept must be considered. Certainly, testing will be tricky, to say the least. With most of the circuitry on the die, circuit-design errors cannot be corrected with yellow wire. Replacement, if not considered in its proper perspective, could be troublesome, since it is conceivable that the entire central processor could be contained in 10 to 20 P.C. boards.

The circuitry for a keyboard input terminal could conceivably be put on one die. There are many obvious advantages to this approach, but the most significant is reduced system cost. Although these complex circuits will cost several times more than present integrated circuits, the cost per function will be much lower. In addition, these new elements will eliminate large quantities of wire, connectors, P.C. boards, and, most important, assembly labor.

The organization of today's computer may not be ideal for these complex elements. As an example, the 16-bit memory element of today might be expanded to 64 bits. With the read-write times previously noted, it would be worthwhile to consider memory distributed throughout the processor rather than having to go out to memory as is the case today.

The lowest cost approach will be for the semiconductor industry to supply standard elements to make up the arithmetic section, buffers, accumulators, adders, etc. The I.O. control circuits could then be either custom or less complex standard circuits at the computer manufacturer's discretion.

The computer industry will benefit significantly from this new technology, and the determining factor appears to be the speed with which computer manufacturers begin to demand the next generation of integrated circuits. ■

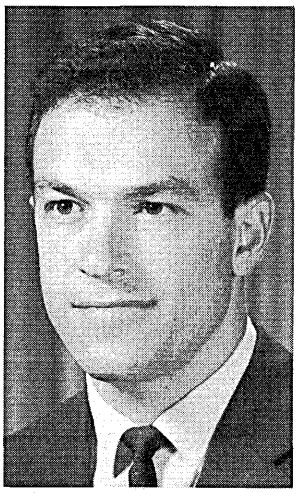
THE TWO SIDES OF TIME-SHARING

by MARTIN GREENBERGER

There is more than one way to bisect the new subject of time-sharing into contrasting aspects. For example, we could view the *good* and the *bad* of it, a dichotomy that is guaranteed to provoke lively discussions. But these discussions, although healthy, are permature. They are a little like the Harvard sweatshirts we see on some three-year-olds. They focus attention on important issues and goals, but come too early in the developmental process to be very meaningful.

My bisection is not going to be into the *good* and the *bad*, but rather into the *system* and the *user*, both of whom we consider good for now. The distinction between system and user is reflected in the double-edged acronym of MIT's Project MAC: *Multi-Access Computer* refers to the physical tool or system, whereas *Machine-Aided Cognition* expresses the hopes of the user. The distinction is also present in the phrase on-line real-time. Real-time depicts the performance of the processor, while on-line describes the status of the user. The distinction may even

Based on material presented to the IFIP Congress 65. Work reported herein was supported (in part) by Project MAC, an MIT research program sponsored by the Advanced Research Projects Agency, Department of Defense, under Office of Naval Research Contract Number Nonr-4102(01). Development of the OPS system was a cooperative undertaking with Anthony Gorry, Malcolm Jones, James Morris, David Ness, Mayer Wantman, and Stephen Whitelaw. Publication by the MIT Press of a manual on the system is scheduled for next month.



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be found within the scheduling algorithm of an on-line operation.[1]

The two-sided characteristic of computing is not new, and it did not begin with on-line systems. In a conventional computer center the operations manager strives for greater equipment efficiency through batch processing and a closed shop, while the programmer longs for faster response time and closer touch with his problem. This state of affairs has led to conflict, and this conflict has been the single most important motive for the development of time-sharing. Time-sharing is definitely a concession to the user and a recognition of his point of view.

By time-sharing we mean the matching of a large computer system with a community of concurrent users dispersed at remote terminals. The match is made by giving each user a small amount of the computer's time (which may or may not be adequate for his request), then passing down the line to successive users, one after another, and returning to users who still need more time. The purpose of the game is to present the appearance to each user of a private computer with instant turnaround for small requests and constant access to a vast store of programming and data. This type of time-sharing benefits the user by enabling him to bring the computer up into the formulative and cognitive phases of his research or problem-solving process. It stands in contrast to the time-sharing of a processor by multiple programs for the primary purpose of achieving higher machine efficiency and more balanced utilization of computer components.

time-sharing supervisors

The first order of business in making time-sharing work on a meaningful scale was to solve the technical problems occasioned by this new mode of operation. Supervisors were built to:

a. Accept input continuously from the remote terminals of a number of simultaneous users,
b. Parcel out successive pieces of the computer's time to users equitably,
c. Schedule this time so that the computer seemed immediately responsive to most requests,
d. Protect the programs of each user from damage by an errant neighbor,
e. Manage input-output and queues of interrupts,
f. Transfer programs flexibly between primary and secondary storage,
g. Maintain data files,
h. Provide error detection and security from unauthorized use, and
i. Allow batch processing to continue in the background, concurrently with operation of the remote terminals in the foreground.

Programming the supervisors to solve these technical problems was a major undertaking, partly because the job had not been done before, and partly because the computers available at the time were not designed to do the job. Emphasis was placed on the system side of the operation—getting the processor to time-share.

A few time-sharing supervisors with limited horizons, like Quiktran and JOSS did cross over to the user's side,[2,3] while the bigger and broader supervisors at MIT and SDC provided a framework and the means for others to do so.[4,5] CTSS, the time-sharing supervisor at Project MAC, is structured as a modular set of subroutines that encourages further evolution.[6] Users may add to CTSS by writing and compiling programs in a variety of languages, including FORTRAN, MAD, ALGOL, and FAP. There are flexible facilities for editing. From this base, systems can be hand-tailored for particular applications, such as engineering design,[7] stress analysis,[8] and symbol manipulation.[9] Each of these systems is in a sense a fulfillment of CTSS in a special user's domain.

The development of time-sharing supervisors has been an approach to man-machine operation from the system's side of the operation. In contrast, the work of Culler and Fried, Hellerman, and Sutherland has approached from the user's side.[10,11,12] They designed their systems to facilitate man-machine interaction in a specific problem context. Sharing time among users was not a prerequisite or initial concern, although it makes good sense as an afterthought, and some of these systems have since moved in that direction. Sketchpad, for example, which is one of the earliest and most vivid of the interactive user systems, is being implemented in an extended three-dimensional form on the Project MAC computer.

The full power of an on-line system is attained when the user is able to shift flexibly and naturally between activities like programming, execution, model building, and statistical analysis without incurring high set-up costs or requiring awkward adjustments. The raw computer can do a wondrous variety of things, as we all know, but this versatility does not benefit most users unless it is placed at their fingertips. The average user should not have to carry water to the faucet in his own buckets, one at a time. The system should provide a continuous supply for him, with the hot, cold, and lemonade taps all within easy reach.

Specifically, it should be convenient for the on-line user to regulate echo checking, make calculations, display intermediate results, obtain helpful guidelines, and view key variables. He should have the ability to move easily between program modification and execution without the need for recompilation. He should be able to execute a subroutine by simply referring to it symbolically, alter its arguments without fuss, compound it with other subroutines, and treat the compound as he treats the parts. These features are important to him whether he is solving a mathematical problem, building a simulation model, designing a man-machine decision procedure, constructing

---

[1]Greenberger, M., "The Priority Problem," Technical Report MAC-TR-21, MIT, 1965.

[2]Morrisey, J. J., "The Quiktran System," *Datamation*, Nov. 1964.

[3]Shaw, J. D., "The JOSS System," *Datamation*, Nov. 1964.

[4]Corbato, F. J. et al, "The Compatible Time-Sharing System," MIT Press, Cambridge, 1963.

[5]Schwartz, J., "A General-Purpose Time-Sharing System," *AFIPS Proceedings 25*, 1964.

[6]Corbato, F. J. and Glaser, E., "Introduction to Time-Sharing," *Datamation*, Nov. 1964.

[7]Ross, T. D. and Feldman, C. G., "Verbal and Graphical Language for the AED System," *Technical Report MAC-TR-4*, MIT, 1964.

[8]Biggs, J. M. and Logcher, R. D., "STRESS: A Problem-Oriented Language for Structural Engineering," *Technical Report MAC-TR-6*, MIT, 1964.

[9]Weizenbaum, J., "OPL-1: An Open-Ended Programming System Within CTSS," *Technical Report MAC-TR-7*, MIT, 1964.

[10]Culler, G. J. and Fried, B. D., "The STL On-Line Computer," TRW/Space Technology Laboratories, Redondo Beach, Calif., 1964.

[11]Hellerman, H., "Experimental Personalized Array Translator System," *Comm. of the ACM*, July 1964.

[12]Sutherland, I. E., "Sketchpad: A Man-Machine Graphical Communication System," *Technical Report 296*, Lincoln Laboratory, Jan. 30, 1963.

a real-time operation, or simply doing some data analysis. And if he is ping-ponging among several such activities, the value of these features, when provided by a single system, is multiplied.

The OPS system at Project MAC was developed to provide these features.[13,14,15] It is an on-line system that is multi-purpose to the individual user, just as CTSS is multi-purpose to the community of users. The OPS system uses CTSS and is a natural extension of it.

an illustration

Suppose we have the following problem to solve: our single processor time shares n terminals, using a round-robin scheduling procedure with a quantum of one second; we want to know how long a one-second request has to wait, on the average, for values of n ranging from 1 to 50; we also want to know how much batch processing can be accomplished in the background during periods when none of the n terminals is requesting service.

For n equal to the number of terminals currently connected, we can answer these questions by making the time-sharing operation introspective—that is, by having it gather statistics about itself. But we cannot use this device in general, unless we are willing to change n repeatedly. Even the most callous administrator would hesitate before subjecting his customers to that series of disruptions.

Simulation is a more feasible tack, as any good student of the art will hasten to tell us. Changing n in a simulation does not disturb the clientele, and can be accomplished with great dispatch.

A still more elegant solution to the problem is to develop a queueing model with n as parameter. By virtue of suitable simplifying assumptions, the model becomes a set of difference equations. A compact algorithm can be programmed to solve the equations recursively.

The benefits and drawbacks of empirical data gathering vs. simulation vs. mathematical analysis are well documented. What we would really like to be able to do is a little of all three, back and forth, until our gradually increasing comprehension of the problem becomes the desired solution.[14]

This iterative process can expand into a series of runs over several weeks or even months in a traditional production-oriented batch setting. Consider the debugging sequence required to program the algorithm; add to this the statistical analyses necessary for estimating relationships and reducing data to classical probability distributions; combine all that with repeated complications of the simulation and contemplation of its results; and you see how this process can be very costly in time. In addition, the process requires a flexible simulation system (like SIMSCRIPT), good statistical routines (like Chi-Square and multiple regression), debugging aids (like traces and dumps), a desk calculator, graphical displays, and so on.

In a time-sharing environment, we can hope for a better match of computer with the creative or problem-solving process. Indeed, this has been one of the main motivations in the development of time-sharing. We can hope for an on-line system that provides us with the variety of facilities we need, and allows us to switch back and forth between debugging, calculating, modeling, simulating, modifying, displays, and analysis, with minimal effort and expense.

The OPS system has these features, and brings us closer to the day when the total process that we have been describing might occupy an able researcher no longer than one interesting afternoon at his terminal.

the ops system

The OPS system is multi-purpose. Its executive gives an on-line user the ability to compound precompiled subroutines, called operators, into programs that can be run interpretively and modified easily without the need for recompilation. The operators may be of the user's own design, or they may be selected from a standard assortment that comes with the system. Standard operators include on-line facilities for: symbolic matrix, vector, and polynomial calculations; statistical analyses such as multiple regressions and classical tests; FORTRAN and MAD type programming with instant execution; incremental modeling of computer simulations; and symbolic manipulation of stacks and tables. The degree of man-machine interaction is variable, and is governed by programmed switches for suppressing and tracing that may be turned on or off at any time. Alternating between separate facilities of the system is generally no more difficult than repeated use of a single facility. Subroutines are added or subtracted with ease, allowing the system to be adapted to a broad spectrum of different applications. Diagnostics and information about the system are available on-line.

The OPS system is a publicly available command at Project MAC. In giving the command, the user can specify operators stored in his personal file, and these will be loaded with the standard operators of the OPS system. Operators either may be loaded at load time, or dynamically any time thereafter.

By means of the OPS system, the user can:

1. Call operators by name from the console;
2. Compound operators into MAD or FORTRAN type programs that may themselves be called like operators;
3. Execute (or test) while compounding;
4. Compound (or remember) while executing;
5. Edit compound operators and their parameters either from the console or from a compound operator;
6. Refer symbolically to common storage by cell or array name;
7. Dynamically modify the mapping and contents of common storage at execution time;
8. Add operators without limit and bring them into core as needed;
9. Intensify or reduce the level of user interaction by means of switch settings.

standard operators

Among the standard operators that come with the system are:

1. SET, which is like the general assignment (=) statement of FORTRAN and MAD, except that its symbols can denote complete matrices and vectors, as well as elements. Thus, executing the operator

```
SET D=A + B * LOG. (C)
```

may cause a 20 x 20 matrix A to be added to the product of a constant B with a second scalar (which is equal to the log of the constant C). The scalar matrix need not be stored explicitly. SET also provides general matrix multiplication, transposition of matrices, and several logical operations. Elements of matrices are referred to by the customary parenthesis notation. Subscripts may be symbolic, as in the following example:

```
SET D(I,J)=A(I,C)/SQRT. (B(C,J))
```

[13]Greenberger, M., "The OPS-1 Manual," Technical Report MAC-TR-8, MIT, 1964.

[14]Greenberger, M., "A New Methodology for Computer Simulation," *Technical Report MAC-TR-13*, MIT, 1964.

[15]Greenberger, M.; Jones, M. M.; Morris, J. H., Jr.; and Ness, D. N., "On-Line Computation and Simulation; The OPS-3 System," MIT Press, 1965.

2. IF and IFB (pronounced IF-B), which are similar to the MAD conditional statement, and cause a branch depending upon the truth value of a Boolean proposition.

3. REPEAT, INDEX, and GOTO, which allow for looping, indexing, and unconditional transfers.

4. READ and PRINT, which permit symbolic entry or printout of information with format control.

5. SAVEC and LOADC, (pronounced SAVE-C and LOAD-C), which save and retrieve information between common storage and disc.

6. SAVES, LOADS, ENTERS, ERASES, RESETS, NORMD, PRINTS (pronounced SAVE-S etc.), which save, retrieve, modify, and print the symbol table.

7. SAVEK, LOADK, EDITK, PRINTK, BEGINK, ERASEK, NAMEK, RESEQ, CALLK, RETRNK, and LOCAL, which save, retrieve, edit, print, delete, initiate, name, rename, resequence, execute, and terminate compound operators, and distribute their parameters.

8. TEXT, which prints out prespecified textual information during execution.

9. FIT, which performs a multiple linear regression of a dependent variable on a set of independent variables. For example

FIT Y TO X1 X2 X3

fits the observations stored in the vector Y to those stored in vectors X1, X2, and X3. A vector of weights may be specified, and a vector containing the residuals of fit may be created.

10. SCHED, RSCHED, DELAY, CANCEL, LOCAL, CALLAK, CALLBK, and RETRNA, which form a package of simulation operators for on-line modeling using an agenda that schedules actions and events.

11. FORMAT, INPUT, and OUTPUT, which make possible arbitrarily formatted reading and printing in the sense of FORTRAN.

12. VIEW, which gives a snapshot of key system variables for error checking.

13. ERROR, which provides diagnostic information on common user mistakes.

14. CTSS, which allows execution of any CTSS command from within the OPS system.

15. GUIDE, which provides descriptive information on the OPS system.

16. DRAW and SEED, which furnish a random draw from the exponential, normal, or rectangular probability distribution, and initialize the generator.

17. RESETQ, STACKQ, GETOLD, POPOLD, GETNEW, and POPNEW, which bring elements or vectors into or out of a single or multi-dimensional queue (or stack) according to either a FIFO or LIFO discipline.

18. COUNT, which assembles into one vector counts of the elements of a second vector that fall into class intervals specified by a third vector.

19. POLY, PSET, and CPSET, which operate on real and complex polynomials analogously to the way that SET operates on vectors and matrices.

20. MADKOP, which translates a compound operator into a MAD subroutine for conventional compilation.

21. RANK, which orders elements of one vector into a second vector, and will store the mapping into a third vector if desired.

22. LOADO, which loads operators at any time.

23. ROOT, which finds the root of a polynomial equation with arbitrary coefficients.

24. A wide assortment of statistical operators for performing classical tests.

the future

Future time-sharing supervisors will run on computer systems having many processors, and many active memory modules, flexibly interconnected. These systems will correct a number of current technical deficiencies in time-sharing operation. They will provide for the dynamic allocation of space between primary and secondary storage, so that a user will not have to specify or load all his programming and data requirements when he begins to interact with the computer. This is a feature of the OPS system, but it had to be programmed. Future systems will furnish it through hardware. They will also permit the sharing by different users, not only of processors and storage, but also program packages assembled as pure procedures in symbolically identified segments of memory.

These advances are on the system's side of the operation. There is still much work to be done there, and it will benefit the user directly. Progress will also come on the user's side in the form of more natural languages, a much wider range of terminal equipment, improvements in graphical and audio input-output facilities, and bigger and better OPS-type systems.

The situation today in computation is about what it was after the turn of the century in the distribution of electricity.[16] The first electric service in New York City illuminated the early Edison light bulbs, and did little else, except run an occasional elevator, toaster, or iron. There was plenty of skepticism about the benefits of distributing electricity in those days. Each electric light installation was required by law to be accompanied by a gas light alongside to cover what was at first considered to be the very substantial likelihood of failure. As it turned out, very few of the gas lights ever had to be used.

Much progress has been made in the design of distribution lines and turbines since then, but the system developments are dwarfed by what has happened on the user's side—household appliances, radio, television, hi-fi, communications, heating systems, air conditioning . . . and computers.

Today there is great intellectual challenge in designing better computer system configurations, as well as the programming concepts and software required to make the systems work as intended (and, historically, even better than intended). Many of the finest minds in the computer field are dedicated to the task. At Project MAC, system programming receives top priority, and the twofold MAC objective is temporarily dominated by a concerted effort to foster and implement the utility concept.

> The broad system goal of Project MAC may be regarded as the development and operation of a community utility that is capable of supplying computer power to each customer where, when, and in the amount needed.[17]

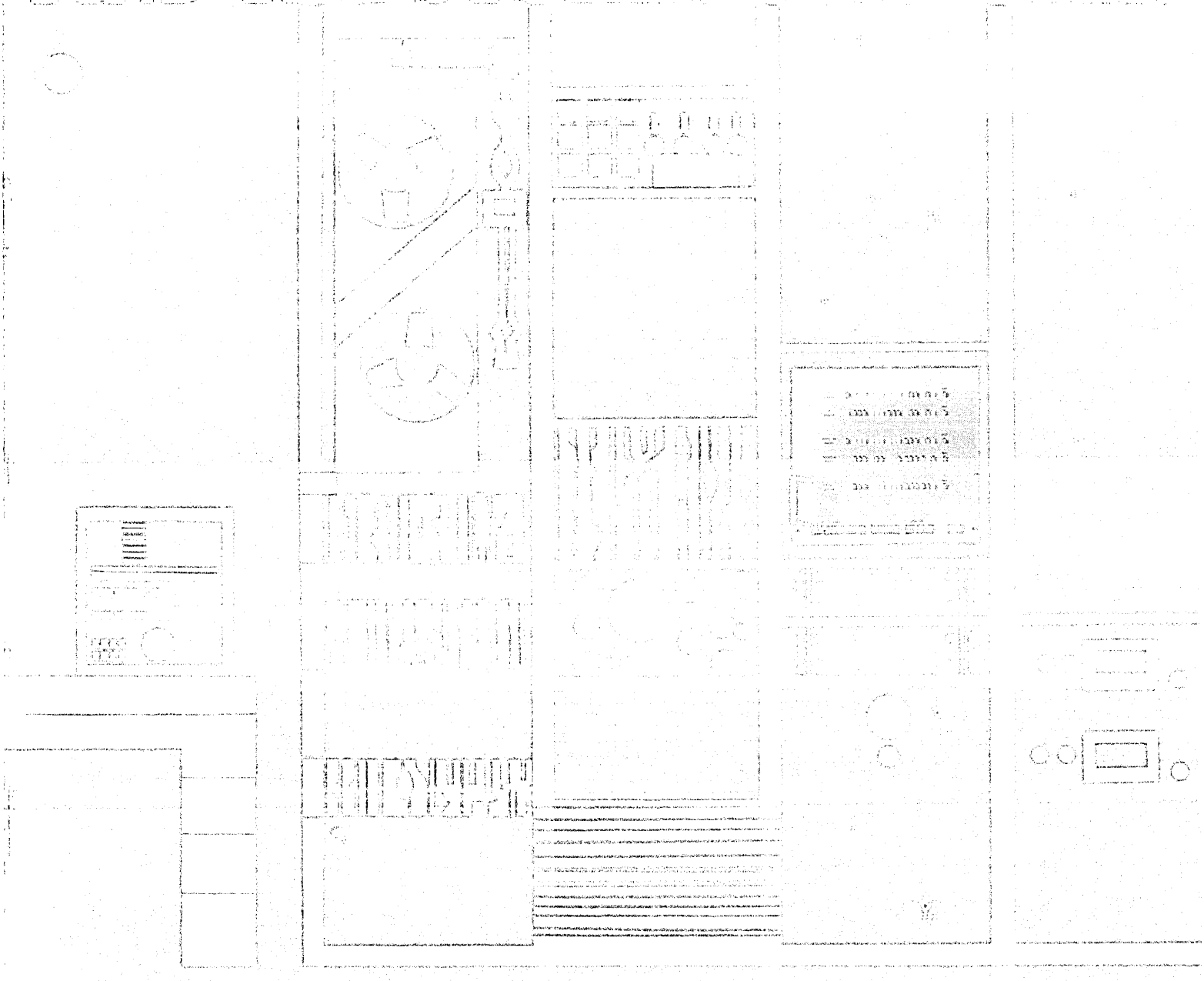
Work also is in progress at Project MAC on the user's side, and OPS is only one of a large number of examples. In coming years we may expect facilities for users to expand dramatically in magnitude and importance, just as applications of electricity have expanded during the past several decades. More and more scientific brainpower and creative energy will shift in this direction.

The shift has just begun. After it is underway for a few years we shall want to sit down and talk about the *good* and the *bad* of time-sharing, although, by then, the contest may be over. ■

[16] Greenberger, M., "The Computers of Tomorrow," *The Atlantic Monthly*, May 1964.

[17] Fano, R. M., "The MAC System: A Report," *IEEE Spectrum*, Jan. 1965.

FIND THE SYSTEM COMPUTER



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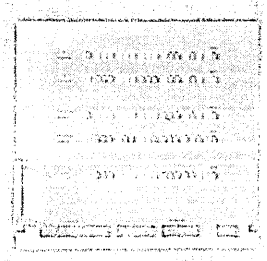

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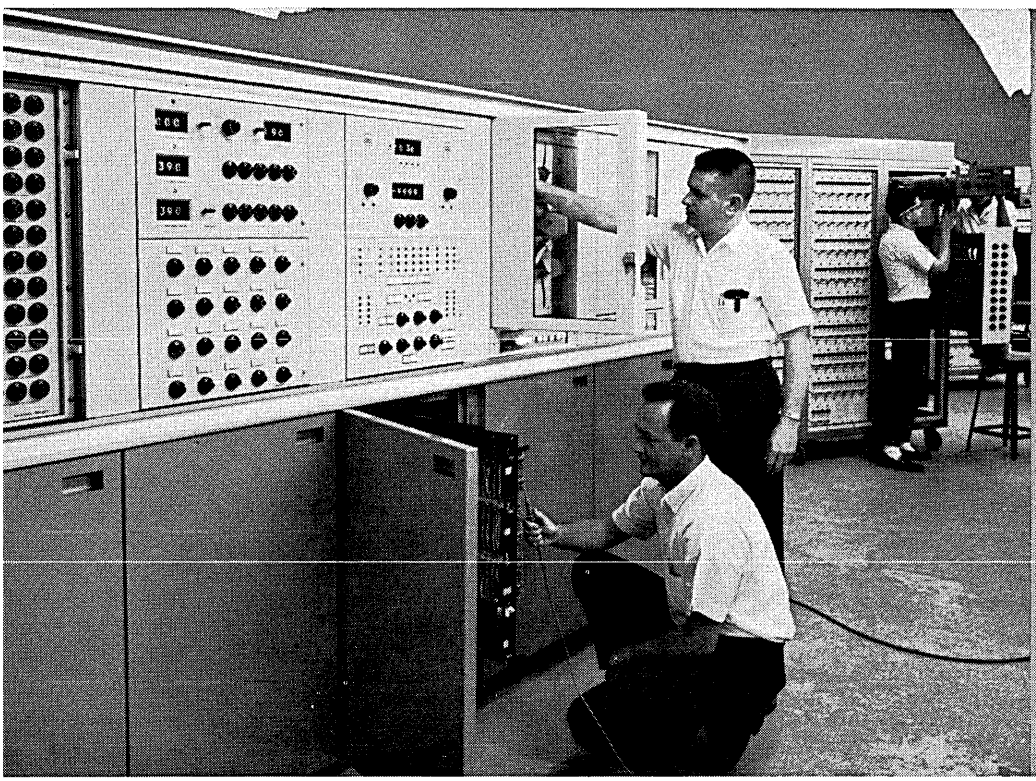

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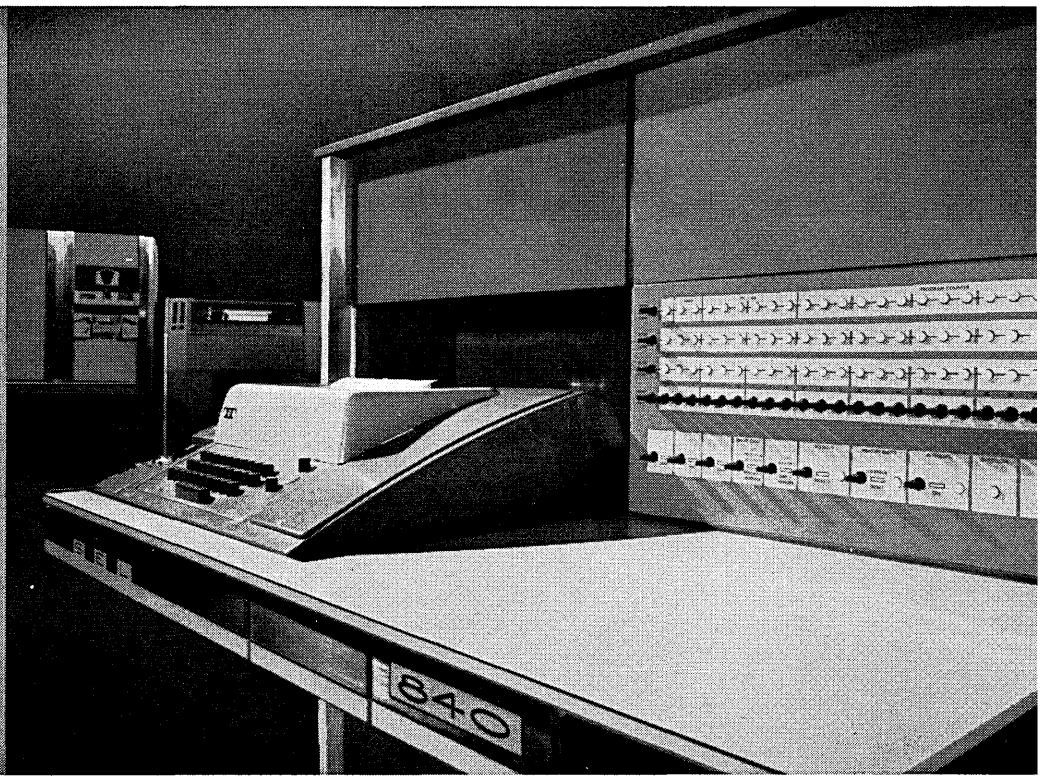

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CIRCLE 23 ON READER CARD

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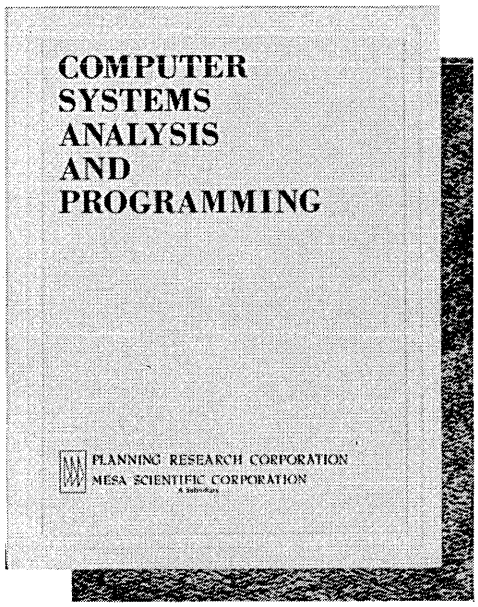

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CIRCLE 24 ON READER CARD

DATA BASE SYMPOSIUM

A blue-ribbon audience of some 200 top software professionals and important users, the latter mostly military, filed into the Santa Monica, Calif., Civic Auditorium on September 21 for a two-day symposium on computer-centered data base systems. After remarks by representatives of the three sponsoring organizations (System Development Corp., the DOD's Advanced Research Projects Agency, and the USAF Electronic Systems Div.), and a state-of-the-art summary by Guy Dobbs, the participants disassembled to spend several hours in concurrent work groups, coming together again for a presentation of four solutions to a data base problem posed by Dick Canning and worked out in advance by MITRE Corp., Informatics, NCR, and Bolt, Beranek & Newman. (GE also provided a solution, but for some reason didn't manage to get on the program).

The welcoming speakers placed emphasis on the importance of facilitating the user's ability to communicate with and manipulate his data base. SDC's Don Drukey, the symposium chairman, distinguished between canned or static and empirical uses of data, a distinction echoed by Dobbs, who asserted that one often doesn't know—*a priori*—how data should be organized. Bob Taylor of ARPA questioned whether there should be acceptance of system design solutions that bar the "naive" unprofessional user from interacting with his data base and affirmed that ARPA, for one, doesn't think so. Colonel Paul Galentine of the Electronic Systems Div. chided the programming community for its "artisan approach" and urged a "software industrial revolution" while agreeing with his co-hosts that ways and means must be found for the user to participate in the design and updating of his data base.

Dobbs can perhaps be excused for neglecting in his state-of-the-art commentary to indicate just what a data base is. After all, presumably the rest of us showed up to help to do that. He did suggest that the objective of any data base should be to: 1) aid executive decision-making, 2) reduce programming and conversion costs, 3) decrease problem definition costs, and 4) facilitate user control over the system.

It was also pointed out by Dobbs that data base research has already opened up a rich new vein of OK words, in what is perhaps the richest single strike since the great time-sharing goldrush of 1963. Files are henceforth to be called "sets" or "volumes" or, if you must be so gauche as to cling to passé terms, at least remember that there are now two classes of files—data files and executable files —and that, moreover, these files may be "self-defining" if not "partially inverted." And they now contain within them not records or fields but, depending on one's choice of barbarisms, "entries," "elements," "lines," or "pages."

It doesn't take a very perceptive observer to begin to wonder at this point how the alleged beneficiary of data base systems, i.e., the hapless user, will be able to manipulate his data base with maximum freedom and minimum training while at the same time avoiding not only these brambles of jargon but, more important, the theoretical and conceptual ferment that they represent. Perhaps our field has begun to develop two distinct kinds of people—the loutish but affluent user whose information needs are fulfilled by a small cadre of clever meta-data base designers.

Anyone harboring such disturbing thoughts could find little solace in the symposium's work group on the theory of data base problem definition. Here, the user types discovered that John, a professional programmer, knew Mary, another professional programmer, and that Mary knew Bob, etc., and off we all went on a merry, albeit somewhat recursive, discussion of warmed-over set theory and information algebra. Interestingly, the user representatives, though sullen and downtrodden, doggedly stayed with the group to the end. (Included was one Air Force officer who stayed on with the objective of finding out how "metal" languages might affect the large system for which he had responsibility).

Other work groups considered criteria for going on-line, entry and query language design, file organization, file protection, evaluation of data management systems, and recording for analysis, costing, and control. If these deliberations fell short of being conclusive, the work groups did seem to provide a stimulus to most everyone's thinking and, after all, this was only the *second* symposium. Several attendees were in favor of a third.

The solutions to the data base problem were interesting though somewhat uneven, both in the elegance of the solutions and in the quality of the presentations. The problem, a deceptively simple one having to do with the maintenance of personnel records, evoked solutions utilizing MITRE Corp.'s COLINGO system, Informatic's Mark III, BB&N's Massachusetts General Hospital System, NCR's BEST, and GE's Integrated Data Store. Perhaps more significant than the details of any of these solutions was the fact that each of the generalized data base systems not only solved the problem, but according to Canning's reckoning, did so in far less problem-solving time than an assembly-language solution would have taken.

Is it possible that users, led by the military, will surrender to these data base systems without a shot being fired in anger? —ROBERT V. HEAD

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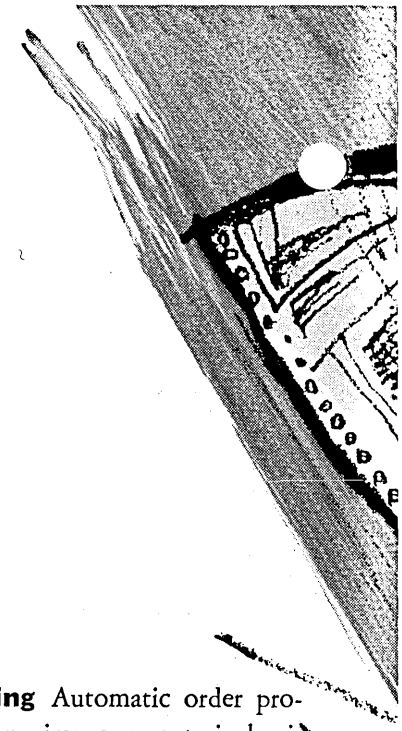

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Automates Order Processing Automatic order processing is only one of the many improvements in business communications provided by Teletype equipment. As an order is typed on a Teletype machine, the details are transmitted to accounting, production, and shipping departments. These departments can receive the information on their own specific forms—thus production, shipping, and billing forms are completed at the same time with maximum accuracy. This instant communication keeps inventories at a profitable minimum.

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That's Why They Want It These important business applications explain why Teletype Models 33 and 35 are used by the Bell System and others who require reliable communications at the lowest possible cost. To learn more about these uses of Teletype sets, write to: Teletype Corporation, Dept. 81L, 5555 Touhy Ave., Skokie, Illinois 60078.

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CIRCLE 25 ON READER CARD

BROOKS BILL BECOMES LAW

new federal edp program

The edp industry's best customer has appointed a new purchasing agent. It happened last month when Congress, just before adjourning, enacted the Brooks Bill (HR 4845). Along with that change, the new legislation makes several others. Added together, they are likely to have a profound effect on Uncle Sam's edp equipment needs. How long this metamorphosis will take is one of the many questions industry observers are asking themselves at the moment.

Basically, HR 4845 sets up an administrator in the GSA whose prime job is to coordinate and standardize the purchase, utilization, and disposal of all edp equipment owned or leased by the federal government. The Bureau of the Budget has responsibility for framing the basic policies under which the administrator operates.

The administrator, rather than the using agencies, will negotiate the purchase and lease of edp equipment required by the federal government. The money the users have been receiving from Congress to buy hardware and software on their own will go into a revolving fund, and this fund will finance the administrator's operation.

Ownership of already purchased equipment will be transferred to GSA so that the administrator can bring about optimum utilization. The bill gives him authority to do this in a number of ways. He can fill an agency's request for new equipment by providing unused time on already available hardware. He can move dp units from one agency to another, or to a third location, if it saves money. He can also buy new equipment and use it to set up pools or dp centers.

There are three main limitations on the administrator's authority:

1. Contractor-owned or leased equipment is outside his jurisdiction.
2. He cannot "impair or interfere with the determination by agencies of their individual automatic data processing requirements, including the development of specifications . . . and the selection of types and configurations of equipment needed."
3. He can't "interfere with or . . . control in any way, the use made of adp equipment or components . . . by any agency."

It will take a "whole team of Philadelphia lawyers" to define these last two limitations, says one observer of the proceedings. A GSA spokesman, however, believes the new program can be organized in about 18 months. In the meantime, the administrator's responsibilities will be "delegated" to the using agencies—i.e., existing procurement, utilization, and disposal policies will remain in effect.

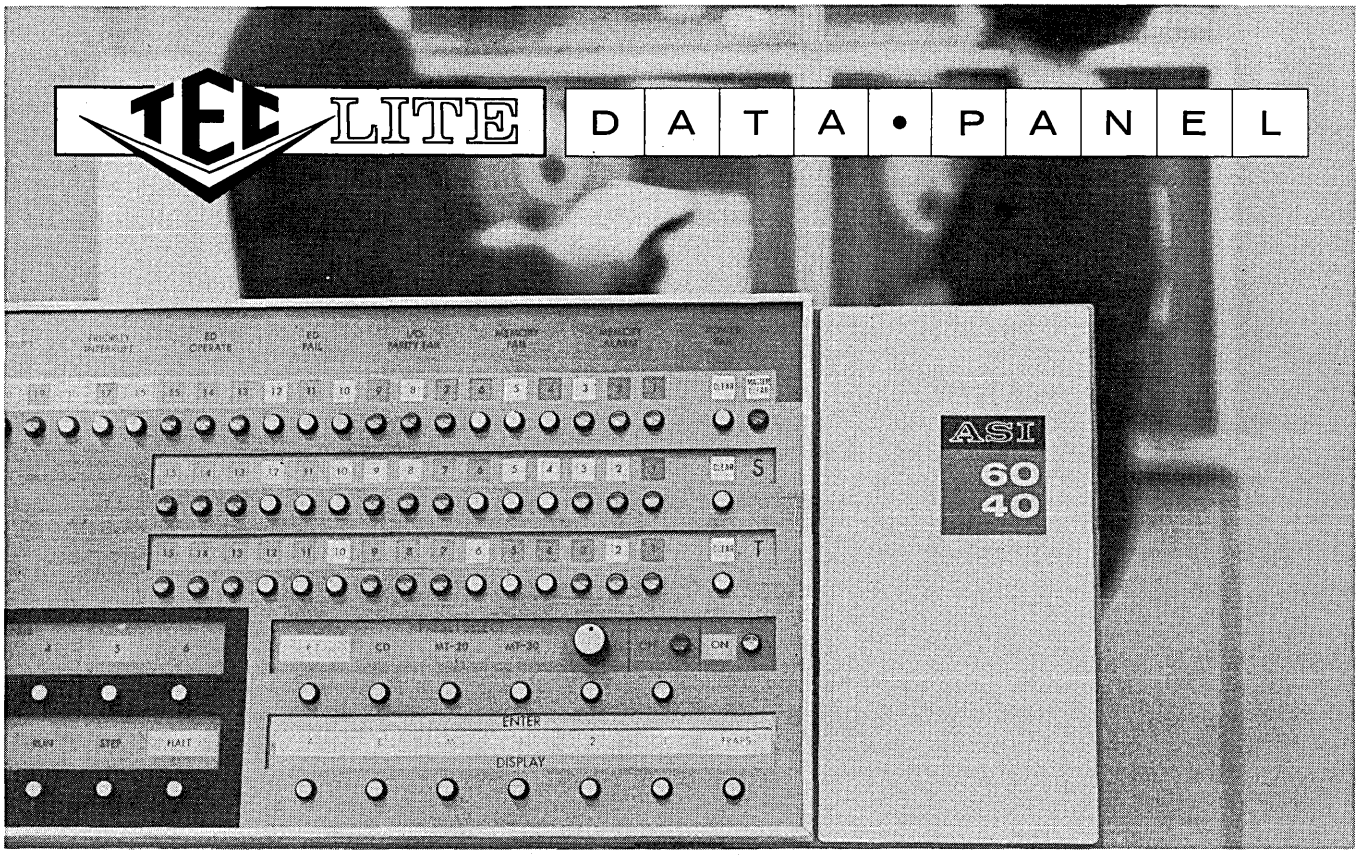
GSA and BOB have quite a job on their hands. They must hire staff, gather the information needed to frame the administrative regulations, decide how far these regulations can go without violating the restrictions written into the act, and resolve the inevitable objections from the using agencies. According to industry overseers, this process could well take longer than 18 months.

A systems expert, sympathetic to the legislation's basic objectives, fears what he calls "the dead hand of federal accountancy." He agrees that more coordination is required but contends that "it's ridiculous to assume that accountants can evaluate the adp requirements of applications at the outer most reaches of every major branch of science and engineering. There can be no greater difference between two research applications using identical hardware and software than between either of them and, say, an adp system used to make up a payroll. An accountant can see that the latter difference affects purchase, utilization, and disposal policies, but he isn't likely to appreciate that these same policies are going to be affected as much or more by differences in research environment."

Earlier this year, GSA and the National Bureau of Standards launched a number of studies designed to improve utilization of federal edp equipment. These activities are an outgrowth of BOB's circular A-71, and an accompanying report, issued last month. How quickly the Brooks Bill is implemented depends partly on how quickly these studies progress.

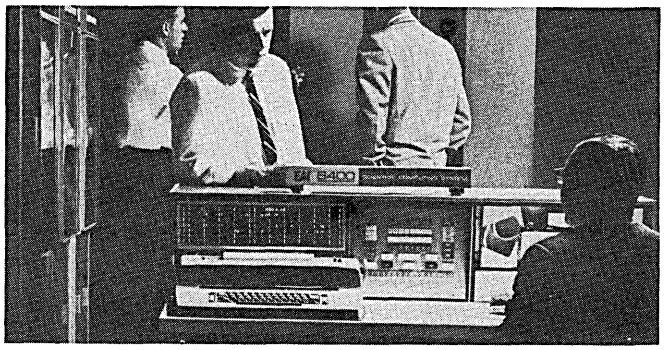
GSA plans to implement circular A-71 partly by setting up additional equipment-sharing exchanges and expanding the rudimentary federal service center and time-sharing facilities now in operation. Guidelines designed to help using agencies choose the best hardware and software, the most reliable suppliers, the break-even equipment utilization point, and the merits of purchase or lease, given a particular application, are being developed, along with regulations to insure effective utilization of excess equipment and machine time. GSA also intends to further standardize adp equipment specs, and speed up publication of its price lists. The latter will come about partly through pressure on suppliers to submit their bids earlier.

The National Bureau of Standards has reorganized its entire dp research and advisory operation; Norman J.

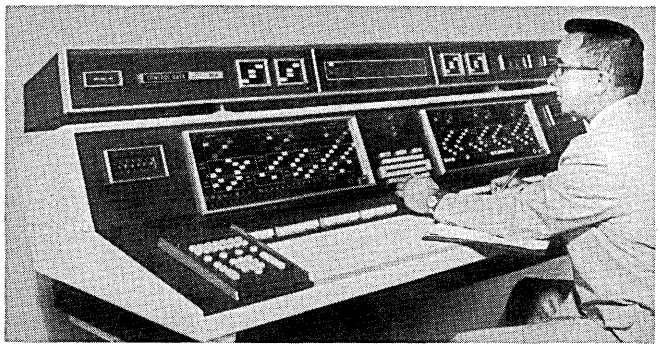


Advanced Scientific Instruments uses DATA·PANEL for complete display and control console of their new ASI ADVANCE Series 6040 Computer.

NEW CONCEPT OF INFORMATION DISPLAY AS DRAMATIC AS TODAY'S COMPUTER DESIGN!



DATA·PANEL indications are visible only when illuminated in EAI 8400 Scientific Computing System by Electronic Associates, Inc. ▲



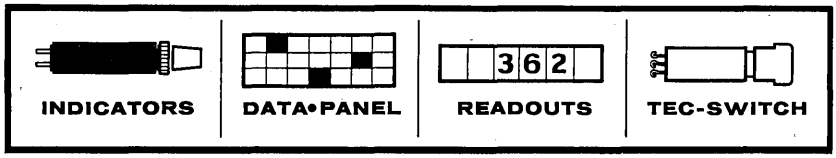
▲ Two computers are operated from this Control Data Corporation Console which uses six DATA·PANEL Information Displays.

Leading designers of modern computers specify TEC-LITE DATA·PANEL for its dramatic new appearance in operator consoles and maintenance panels. DATA·PANEL offers a new concept of display versatility and visual impact, in addition to greatly increasing operator accuracy.

Extremely flexible visual and mechanical parameters of DATA·PANEL give designers display freedom never before available. There are no restrictions, within practical limits, to the shape, color, size or arrangements of the information displayed. Indications and digital readouts stand out emphatically in color behind smooth planes of glare-free black glass. When "off", legends and indications can be totally invisible until illuminated. For control, complete range of switch actions can be an integral part of DATA·PANEL design.

Write for full-color brochure, specifications and ordering information.

TEC LITE
INDICATING DEVICES



Transistor Electronics Corporation

Box 6191 Minneapolis, Minnesota 55424 Phone (612) 941-1100

See TEC-LITE Indicating Devices — FJCC Booth #119

CIRCLE 27 ON READER CARD

BROOKS BILL . . .

Ream, Lockheed's director of Systems Planning, has been brought in to take a top job: he'll become director of a computer science and technology center NBS is setting up. The agency has developed nearly 60 separate projects related to the federal adp program. It's designed, basically, to improve existing technical advisory services, promote the adoption of equipment and programming standards, and resolve technical questions connected with system design, purchase, utilization, and disposal of federally-acquired dp equipment.

It will be a long time before much of this work bears fruit. For example, the BOB report stressed the use of service centers as one way of using equipment more efficiently. But GSA doesn't plan to open any more new service centers until: a) an evaluation of the experimental center now operating in Washington is completed, and b) NBS has made a detailed study of the kinds of applications, hardware and software best suited to service centers. According to many observers, it will be 1968 or '69 before an appreciable number of centers is operating. They feel the same way about the plans to add a time-sharing capability to the Federal Telecommunications System, and the effort to standardize programming symbols. The directives and guidelines required to carry out the bulk of the BOB recommendations will also germinate slowly. Says one official: "BOB needs a year just to decide how it's going to study a problem."

Despite these delays, some progress is likely next year. In January or February, DOD probably will implement one of the BOB recommendations; a department spokesman says that a long-discussed amendment to Armed Forces Procurement Regulations—limiting contractors' adp lease payments to no more than the purchase price of the equipment—should be published then. DOD already has ordered that contractors' technical personnel be replaced by civil service or military people "wherever necessary or desirable." This decision grew out of a study conducted by the Civil Service Commission that was roughly simultaneous with the BOB inquiry.

Also, a subcommittee of the Inter-Agency Committee for adp is now putting the final touches on a proposal to classify government systems according to use. This work is an attempt to carry out a recommendation in Chapter One of the BOB report. It could be vitally important because the classification system ultimately accepted will be used in the development of adp purchase, utilization, and disposal policies.

The basic purpose of A-71 and accompanying report was to remove the sting from charges of sloppy edp management made by the General Accounting Office. Backers of the Brooks Bill say the legislation has stilled this criticism. The using agencies aren't so sure. A typical comment is that: "GAO is just biding its time. It will start squawking again as soon as GSA and BOB sit down to start drafting the legislation."

Up to last March, when A-71 appeared, GAO had announced 90 cases of alleged mismanagement. These were the major complaints: inadequacy of pre-installation planning and preparation; uneconomical and ineffective equipment utilization; overpayments due to poor record-keeping and failure to take advantage of favorable contract provisions; uneconomical procurement; waste from un-coordinated determination of needs. Remedying these defects, said Comptroller General Joseph Campbell, who retired recently, would produce savings of about $100 million a year.

BOB and the using agencies haven't questioned GAO's figures. But they have contended that the GAO's proposed solution would create more problems than it would solve.

The most current statement of what GAO wants is embodied in S 1584, a bill drafted by the GAO at the request of Sen. Paul Douglas of Illinois, who introduced it early in the last session. Hearings weren't held on S 1584 because the committee wanted to consider it and the Brooks Bill concurrently. When Brooks got his bill passed on the Senate floor, just before adjournment, he neatly killed the Douglas legislation.

"It is the sense of Congress," says the Douglas bill, "that adp equipment or systems shall be purchased rather than leased." There is no similar language in HR 4845. S 1584 also covers contractors, who are excluded from GSA management control under the Brooks Bill. It seems likely that before the new regulations are adopted, GAO will try, once more, to get these two points considered.

A good opportunity will be provided when GSA submits to the Senate Appropriations Committee a report on the relative advantages of purchasing vs. leasing adp equipment. This evaluation was requested by the Senate just before it approved HR 4845. The report probably will be sent over next year. GAO, judging by the way such matters have been handled in the past, will be asked to evaluate it. ■

—PHIL HIRSCH

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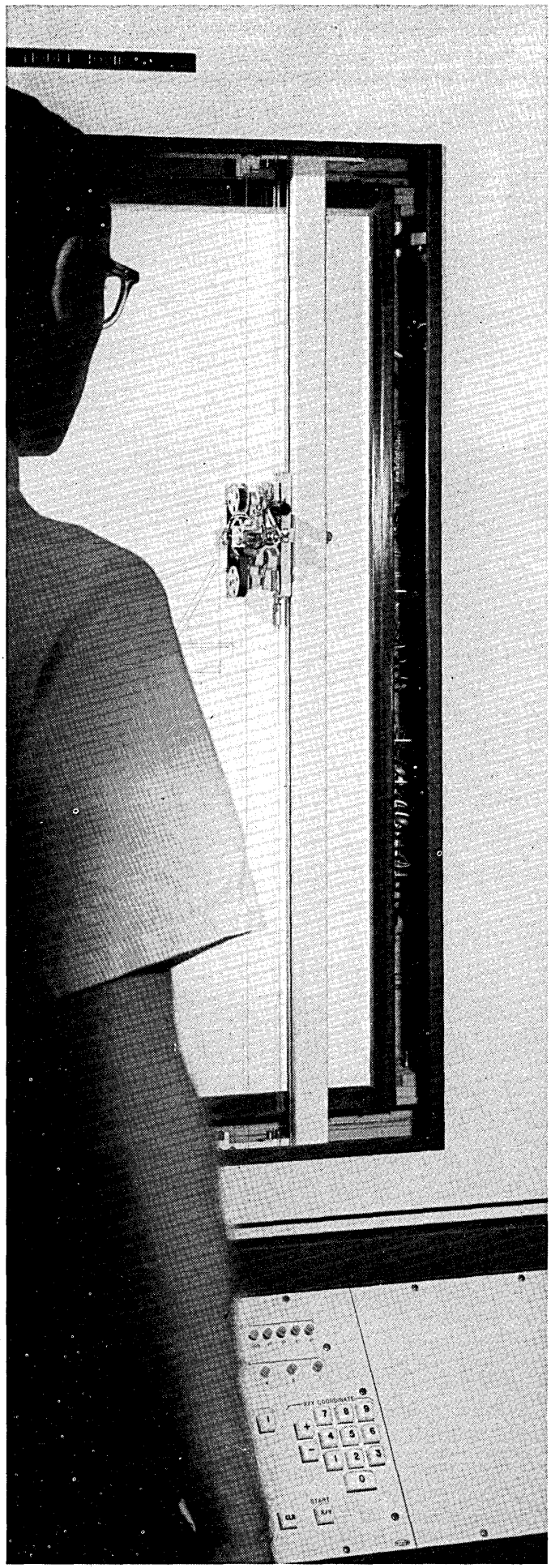
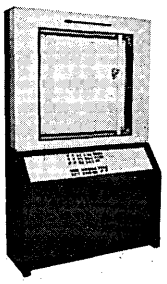


See how much more your data display dollar will buy...



Compare Milgo's new 30"x30" Vertical - plotting X-Y Recorder feature for feature.

Compare it for speed. Repeatability. Accuracy. Reliability. Plot visibility. Add-on flexibility. Versatility. Quality. Floor space. Delivery time.

The Milgo solid-state 4021D X-Y Recorder accepts on-line digital inputs from any digital computer; off-line inputs from magnetic tape, punched paper tape, punched cards, a manual keyboard or an analog source. The pen/printer draws lines, curves and point-plots; it symbol prints with a 50 character symbol printer. Pen and symbol printer interchange electronically in milliseconds. The pen/printer has a slew of 30 ips, with a continuous writing speed of 20 ips. The pen/printer point-plots in either pen or symbol mode at 500 ppm. It prints a random selection alpha-numeric character at 300 per minute. The plotting surface is evenly back-lighted by a variable powerstat control. Plots are clearly visible for 10 feet or more. The complete unit only occupies a 50 by 18 inch floor space.

The 4021D was developed and is produced to military standards of quality and reliability. It is rugged and of modular construction. Installed and operating, it has the lowest feature-for-feature price tag of any 30 by 30 inch plotter available to industrial and commercial users.

Take a cold, hard look, for instance, at the symbol printer and its integral pen and inking system.* The complete unit is ⅓ to ¼ smaller than competitive units. It has no dangling umbilical cord. Pens are low-mass, solenoid actuated. Capillary action prevents spilling at any slew speed or acceleration, and the ink reserve can be filled without disassembly. Ink supply is indicated visually. The arm, only 1¼ inches wide, is servo-motor driven at both top and bottom. It is ball-bearing mounted on stainless steel rails, precision ground to within 0.004 inch. It allows accelerations of 400 ips² in both X and Y; provides static accuracy within ±0.05% of full scale, and repeatability of ±0.02%.

Milgo offers analog and/or digital recorders in vertical or horizontal models with plotting surfaces up to 45 x 60 inches. If you need to know what your "data-display dollar" can buy, call Tom Thorsen, Marketing Department.

*U.S. Patent No. 3,120,214.

milgo

Milgo Electronic Corporation
7620 N.W. 36th Avenue, Miami, Florida 33147.
Phone: 305 691-1220. TWX: 305 696-4489.

FROM PROGRAMMED INSTRUCTION: A PROGRAMMED TEXT

by T. D. C. KUCH, Applied Data Research, Inc.

Page 1

Chapter I

Programmed Instruction is a new, useful method of learning. A new, useful method of learning is _____ _____.

Page 2

Programmed Instruction

If your answer was correct, go on to Page 3. If not, forget the answer above (*Programmed Instruction*) and go back to Page 1.

Page 3

The key concepts of Programmed Instruction, that new, useful method of learning, are repetition, blank-filling, and page-turning. Based on this information, do you think that Programmed Instruction is really worth while? Decide on an answer, then turn to page 4.

Page 4

If you answered yes, go to page 5. If you answered no, go to hell.

Page 5

This is the end of Chapter 1. Turn the book upside-down and inside-out, and you will find the next chapter, which is Chapter II. Begin Chapter II.

Page 6

Chapter II

One of the revolutionary techniques of Programmed Instruction is to insure that the correct answers to the questions can be immediately determined from information already given the student. This is called "rote". This is called "_____".

Page 7

Rote

If your answer was correct, go to Page 8. If your answer was some synonym of rote, go to Page 8, but watch it in the future; next time we will make you go back. If you salivated, you may skip the rest of this book. If none of the above, go back to Page 6. If all of the above, go back to Page 1.

Page 8

Note is reinforced through repetition. Note is reinforced through repetition. Note—reinforced through repetition.

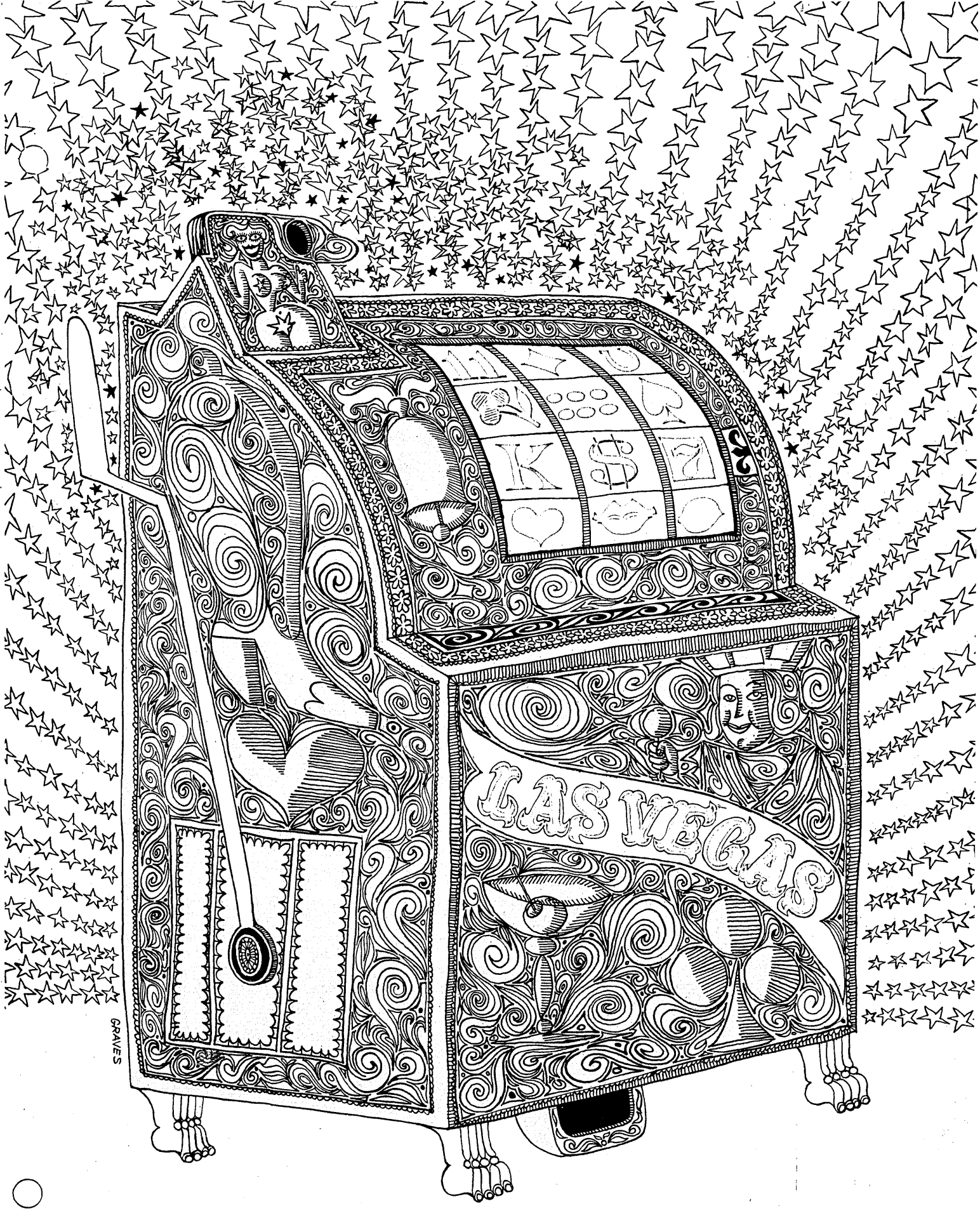
Page 9

is

If your answer is is, go to Page 10. If your answer is is not, go to hell. If your answer is not is, go back to Page 8. If your answer is not is not, go go to to Page Page 10 10.

Page 10

This is the end of Chapter II. Perform a spatial inversion with respect to this book and you will find Chapter III. Begin Chapter III.



Fall Joint Computer Conference

Dr. Robert W. Rector

THE CHAIRMAN'S WELCOME

by DR. ROBERT W. RECTOR

Statistics are O.K. They can even make a conference sound great. For example, the Fall Joint Computer Conference has to be the largest and best one in 1965. Since it is the only AFIPS-sponsored conference of the year, it will set records for sure. With IFIP preempting the spring meeting dates, FJCC 1965 becomes the AFIPS showcase for equipment and the related programming advances. The conference has already sold the largest amount of exhibit space and received the largest number of papers for its technical program. The Conference Committee recognizes that these are shallow claims; the test will be how well FJCC 1965 presents significant material to the professional community.

A great deal of thought has gone into the preparation of the program, and the conference presents three major innovations. The most distinctive feature is five "discuss-only" sessions—two in software and three in hardware. Pre-prints of these sessions, made available for study before the conference, make it possible to dedicate entire sessions to a searching examination of specified material. The method has been successful in smaller conferences, and we are confident that this will permit us to bring timely, thoughtful discussions to the floor of a major national conference. Pre-prints of the "discuss-only" sessions were available a month before the conference. The fee for the pre-prints is applicable to subsequent registration, so there is no additional cost to the conference participants.

conference participants

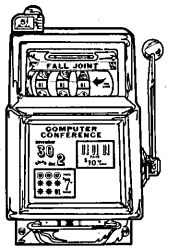
Recognizing the increasing degree of specialization in the hardware and software fields, the Technical Program Committee has added a third information channel to the conference to focus attention on management and applications. The sessions and the related discussions speak to questions of marketing and economics as well as applications in the scientific and humanistic fields. This approach should provide interest for the generalist and the ever-increasing number of dedicated computer people no longer in the middle of research and development activities.

Finally, FJCC 1965 has made a major revision in its format. There is no keynote speaker, but rather a series of distinguished specialists from allied disciplines to delineate the real influence of the computer on their fields. This complete and comprehensive series of presentations on the last day of the conference, without the distraction of parallel sessions, is a serious attempt to place the influence of computers on the American society into proper perspective.

We have tried to add interest in other ways: a special program for educators and a display of computers assisting in the learning process; a concert of computer-generated music; an exhibit of computer-generated art; and an on-line press room.

While we welcome records in attendance and the like, the goal for the committee chairmen for the 1965 Fall Joint Computer Conference is to make this the most stimulating and informative conference ever held. They are also providing for your comfort and convenience. It is my pleasure to commend the results of their work to you and to invite you to participate in the conference. ■

CONFERENCE PARTICULARS



Innovation. That's got to be the word for this year's Fall Joint Computer Conference, on Nov. 30 through Dec. 2. "Crammed" might be another, for there are 35 technical sessions scheduled for the first two days . . . and nights. But this crowded schedule is an attempt to offer something for everyone, and is a recognition of the computer's effects on an ever-widening segment of the social and physical sciences.

Perhaps more striking, however, is the format to be followed this year at the Las Vegas Convention Center. With formal and parallel (up to five at a time) technical sessions out of the way, the third day (Thursday) will be devoted to an all-conference session. In serial fashion, the impact of the computer on such fields as urban transportation, world trade, medicine and the consumer will be assessed by people working in those areas. There will be no other sessions to detract from this. At least not in the Convention Center.

The presentations: Simon Ramo, The Computer and Our Changing Society . . . Ralph W. Gerard, Computers and the Future of Education . . . James V. Maloney Jr., The Future Impact of Computers on Medicine . . . C. Robert McBrier, The Computer and the Consumer . . . William I. Merkin, The Application of Computers to World Trade . . . William H. Pickering, The Role of Computers in Space Exploration . . . James A. Ward, The Impact of Computers on Government . . . Paul Baran, Communications, Computers and People . . . Kenneth J. Schlager, The Impact of Computers on Urban Transportation.

As has already been widely publicized, there are also five discuss-only sessions, which are heavily dependent on the ability of attendees to study pre-prints of the papers and to fire questions at their authors. There'll be no word-for-word reading by authors of material already in the Conference Proceedings.

A copy of the Proceedings goes to each registrant. Fees are $10 for members of sponsoring organizations, $20 for non-members. Sponsoring societies, all members of the American Federation of Information Processing Societies (AFIPS), are the Assn. for Computing Machinery, the IEEE Computer Group, American Documentation Institute, Simulation Councils Inc., and the Assn. for Machine Translation & Computational Linguistics.

Of course, this fee also gets you into the exhibit area, which this year will feature some 90 exhibitors. There may be some new, small computers on the floor, but chances are most mainframe manufacturers will have only Teletype terminals affixed to the ends of phone lines.

On-line coding is all right, but for the more esthetic, there will be a Computer Music Concert on Tuesday from noon to 1:15. Presented by Dr. John R. Pierce of Bell Telephone Labs, the program will cover computer-composed music, computer-aided musical composition, and computer-produced musical and vocal sounds. Recorded examples will be played. Another special event, again on Tuesday, is a re-enactment of the mock trial, "The Computer in Court: Are Computer Records Legal Evidence?" Described briefly in the May issue of DATAMATION (p. 142), it is produced and directed by Roy Freed.

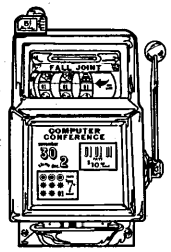
Other conference features include a luncheon address by Mrs. Ida Rhodes of the National Bureau of Standards. Always to be recommended, this "call 'em as I see 'em" lecturer will speak on "The Might of the Man-Computer Team." Two other industry pace-setters will receive the Harry Goode Memorial Award for 1965. They are George Stibitz and Konrad Zuse, both credited with the design of the first operating program-controlled computer. Independently, the two also proposed the use of the binary system and floating-point arithmetic.

During the exhibit hours, experimental but operating educational and training devices will be shown in Meeting Room 17. Included will be on-line consoles used as teaching machines, small analog and digital computers designed for classroom use, and programmed instruction in FORTRAN.

Again this year, educators from the nation's Southwest will be invited for an orientation on the computer technology, and will sit in on the Thursday general session.

Although this FJCC may be daring in format and remunerative in revenue, the question to be asked is, was it an effective technical conference? This will be the function of an epilog session on Thursday, when a preselected board of observers will convene in public session. More than a critique, this assembly will attempt to chart trends drawn from the three-day meeting and to cite areas of research deserving more attention. Sometimes astute conclusions are more valuable than a bound volume of technical papers. ■

exhibit area
convention center



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TO TECHNICAL SESSIONS
TO REGISTRATION

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DATAMATION

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LOUNGE

TO TECHNICAL SESSIONS

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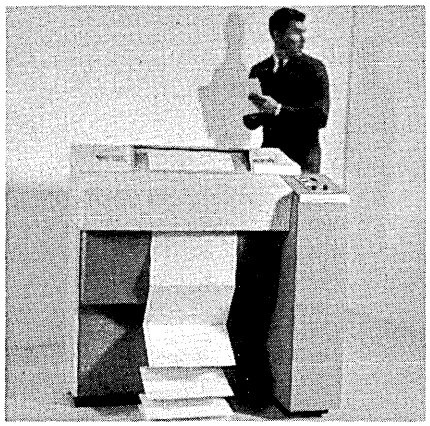
THE EXHIBITORS

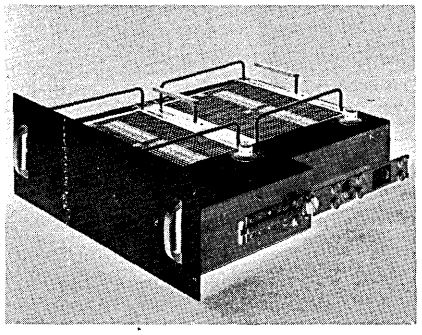
FJCC
PRODUCT PREVIEW

ANELEX CORP.
Boston, Massachusetts
Booth No. 433, 434, 509, 510
A line printer with DataPhone interface capability, and operating at 300



lpm, is being shown. It prints single or multiple copies in a variety of widths and lengths, and uses the rotating drum impact method.
CIRCLE 130 ON READER CARD

APPLIED DYNAMICS INC.
Ann Arbor, Michigan
Booth No. 438, 439
Newly introduced is an arbitrary diode function generator for analog computers. A removable pre-patchpanel facilitates setup and storage, enabling changeover of functions by simply changing patchpanels. The panel reportedly can be patched in same time

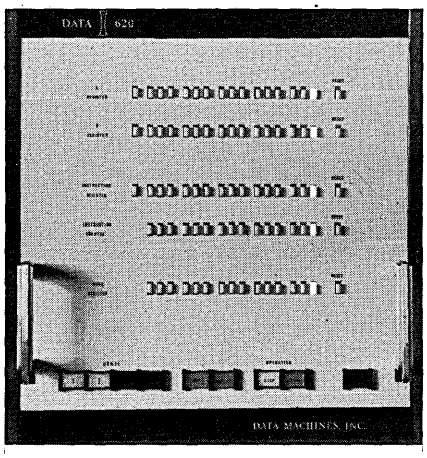


as conventional manual units. Breakpoints, slopes and parallax values are patched by inserting jumper plugs. Breakpoints are terminated in BCD to allow direct, open-loop setup to the nearest 0.5 volt with 0.02-volt precision. Slopes are selected with 14 bits to provide 0.01% resolution.
CIRCLE 131 ON READER CARD

BRYANT COMPUTER PRODUCTS
Walled Lake, Michigan
Booth No. 146, 200
Being introduced and demonstrated is the PhD-340 Random Access Storage Drum. The unit features simultaneous read-write access to 340 million bits stored on 5,504 tracks. Up to four channels provide programming flexibility and the ability to serve multiprocessor configurations.
CIRCLE 132 ON READER CARD

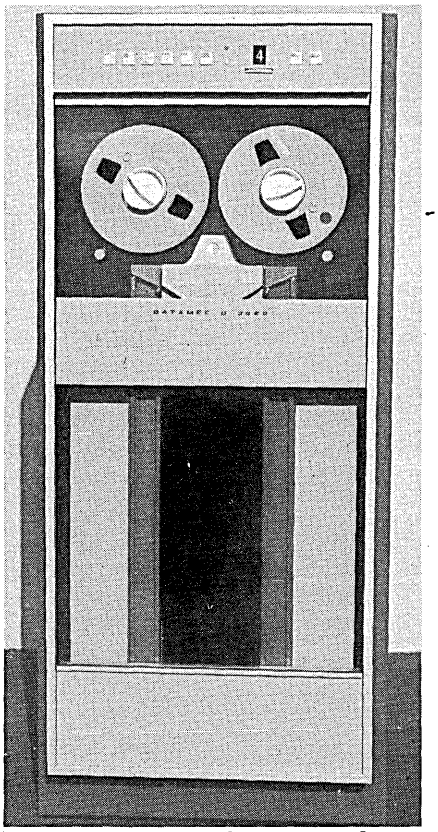
CALMA COMPANY
Los Gatos, California
Booth No. 130, 131
Getting its first public showing is the model 302 digitizer, an upgraded version of the Mod 300. The new unit has a maximum tracing speed of 125 inches/minute, output recorder packing density of 556 bpi, and output recorder speed of 500 cps. For each inch of analog trace digitized, 0.2 inch of mag tape is required.
CIRCLE 133 ON READER CARD

DATA MACHINES INC.
Newport Beach, California
Booth No. 526, 527, 528
The DATA 620 System Computer receives its first public demonstration. Requiring 21 inches of standard rack space, the 620 is designed for use at a telemetry station, or data reduction or process control installation. It has 4-32K (16 to 24-bit) words, cycle time of 1.8 usec, and a repertoire of 107 basic machine commands—plus microprogramming capability. Up to 28 optional application-oriented in-



structions are also available. A "party-line" I/O channel permits up to 18 devices to be connected by a single plug-in bus.
CIRCLE 134 ON READER CARD

DATAMEC DIV., HEWLETT-PACKARD CO.
Mountain View, California
Booth No. 506, 507
New at this show is the D 3029 tape transport which is directly interchangeable with the IBM 729-II and -V tape drives. Performance characteristics,



data rates, electrical inputs and outputs, and even the plug connector match the above units. But price is said to be lower.
CIRCLE 135 ON READER CARD

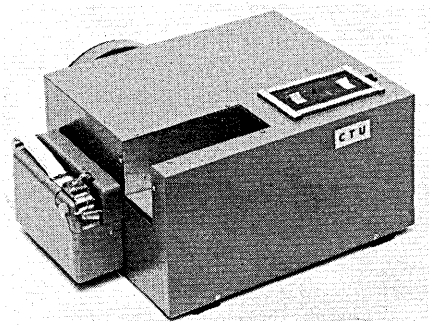
DECISION CONTROL INC.
Newport Beach, California
Booth No. 526, 527, 528
First showing of the recently-announced VersaSTORE integrated circuit core memory systems is scheduled. The units operate at speeds of 2 usec full or half cycle, and have capacities of 128 to 4K words of up to 24 bits.

Signal input and output levels range from 3 to 12 volts with both PNP and NPN interfaces available, and the front panel of the rack-mounted units have continuous incandescent-lamp display of all registers.

CIRCLE 136 ON READER CARD

DIGITAL ELECTRONIC MACHINES INC.
Kansas City, Missouri
Booth No. 140

Two media converters being shown are the CTU card-to-tape converter, operating at 800 characters/minute, and the TPU-28, a 28-bank keyboard to tape (or card) unit. In the latter, one or two entry columns can be used to set up supervision circuits so that



preprogrammed fields must be filled with data before punching will occur. The card-tape unit has as options an external keyboard, non-standard tape coding, alphanumeric printer, and automatic control of peripherals (typewriter, printer, etc.).

CIRCLE 137 ON READER CARD

DIGITAL EQUIPMENT CORP.
Maynard, Massachusetts
Booth No. 233, 244, 309, 310

The Model 338, being introduced, is a CRT display system incorporating a 4K PDP-8 computer as a buffer. An off-line, self-contained display unit, it can operate a variety of peripheral devices or act as an interface to an external computer through a direct or phone-line connection. The PDP-8 allows it to simultaneously control the interface to the external data source, respond to light-pen requests from the display, and respond to keyboard messages from the operator. The display shows a 0.15-inch spot at any of 1,024 x 1,024-points in a 9⅜ x 9⅜-inch square. Random points can be plotted in 35 usec in the point mode; in the increment mode, up to 15,000 flicker-free points can be plotted at 1.5-usec/point.

CIRCLE 138 ON READER CARD

ELECTRONIC MEMORIES INC.
Hawthorne, California
Booth No. 431, 432

Two core memory systems and a stack are being introduced. The NANO-MEMORY 700 system has a cycle time of 700 nanoseconds, access time of 350 nsec, and a capacity of up to 16K (8 to 84-bit) words. It is said to have a 2½-dimensional organization, combining the decoding advantages of a 3-D with the reduced array assembly costs of a 2-D organization. The second system is a lightweight, ruggedized unit with an access time of 750 nsec and a capacity of 4K (32-bit) words. The new stack is also ruggedized, said to have a third greater packing density. A typical 4K, 30-mil stack has 12 bits/inch.

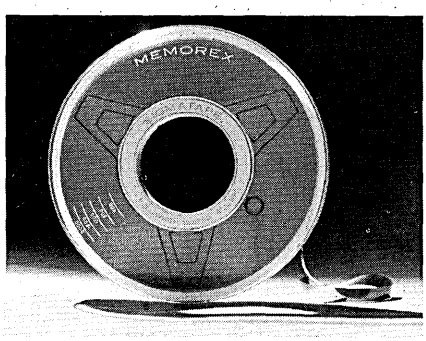
CIRCLE 139 ON READER CARD

GENERAL PRECISION LIBRASCOPE GROUP
Glendale, California
Booth No. 422, 423, 424

In addition to the regular line of disc memories and other products, being shown is one of the discs and a retractable head plate from the recently-announced LIBRAFILE 4800 mass memory. The disc is 48 inches in diameter, combines with five others to store 400 million bits that are accessible in an average of 35 msec.

MEMOREX CORP.
Santa Clara, California
Booth No. 120, 121

The newly-announced Sigmatape, which reportedly is a high-reliability



mag tape, is being shown. It is said to enhance the performance of tape drives.

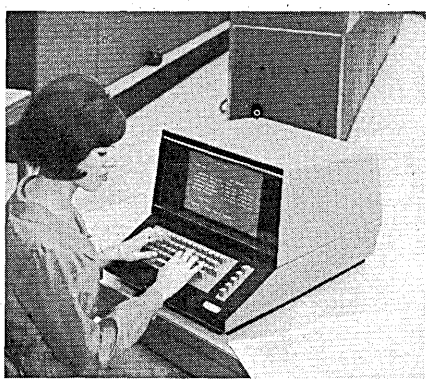
MIDWESTERN INSTRUMENTS INC.
Tulsa, Oklahoma
Booth No. 219, 220, 221

The M4000 series tape transports are compatible with 7- or 9-track formats. Available for single or multiple speed operation from 25 to 150 ips, and with densities to 800 bpi, they have transfer rates to 120KC. Tape movement is by pneumatic pressure. Options include multiple transport control, address select, select echo, manual density set, programmable control toggles for read/write, other specialized functions.

CIRCLE 140 ON READER CARD

RAYTHEON EQUIPMENT DIV.
Wayland, Massachusetts
Booth No. 540, 541

Not newly-announced but getting its first showing is the DIDS-400 display system. This table-model I/O unit has an alphanumeric keyboard and a 6 x



9-inch display area with a capacity of 1,040 characters. Self-contained, it consists of a display console, control unit, and optional hardcopy printer. Interfaces enable linkage with a computer or a telephone line.

RAYTHEON COMPUTER
Santa Ana, California
Booth No. 235, 236, 307, 308

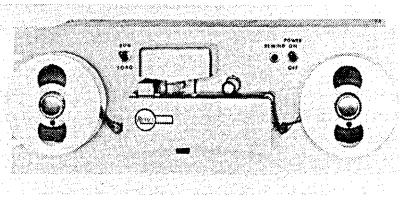
New memory to be displayed is the EAROS, Electrically-Alterable Read Only Store, which is part of the firm's MICROBIAX series. It reads out at 3 to 5 MC rates, and has a capacity of up to 4,000 words with lengths up to 120 bits. Lowered costs of this non-destructive readout memory are reportedly achieved by use of two-wire arrays and new type diodes in the read-

write circuitry. Operating range is 0° to 50°C.

CIRCLE 141 ON READER CARD

RHEEM ELECTRONICS
Hawthorne, California
Booth No. 518

A paper-tape reader/spooler to be introduced operates with a photocell at speeds up to 300 cps with push but-

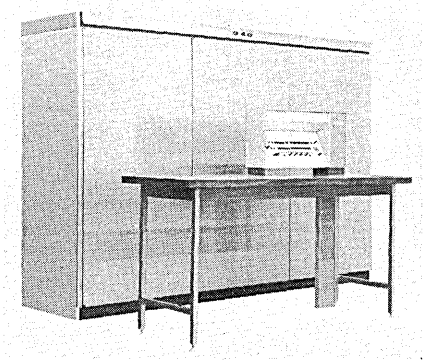


ton or remote control rewind of 40 inches/second. Reels of 5¼-inch diameter are available with storage capacity of up to 500 feet of tape. Model designation is the RRS-302D.

CIRCLE 142 ON READER CARD

SCIENTIFIC DATA SYSTEMS
Santa Monica, California
Booth No. 226, 227, 316, 317

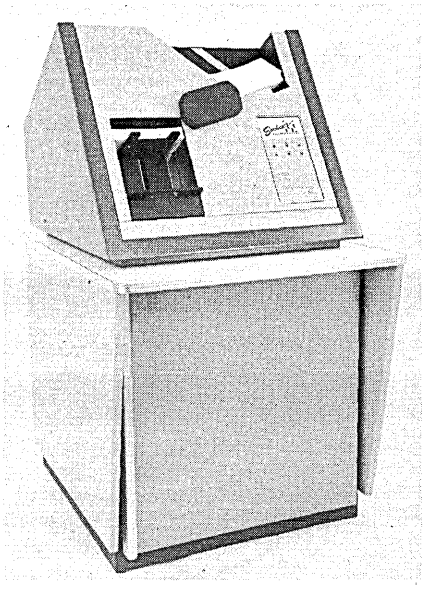
Receiving its first public showing is the SDS 940, the time-sharing version of the 930. Actually, visitors will see only two Teletype units hooked to a 940 at Cal-Berkeley, 500 miles away. Also being debuted is a new line of



mag tape units, already announced, and a 21-inch CRT display with light pen. There's also a new line of logic modules featuring integrated circuits and module boards 50% smaller than current units.

SOROBAN ENGINEERING INC.
Melbourne, Florida
Booth No. 211, 212

New peripherals being introduced are a compact, floor-model card punch and a reader. Features in common are vacuum-assist card picker with pneumatic throat and 1,000-card hopper. Punching, in four-column increments, is at 150 cpm. Used is the firm's EP-4 end feed punch head. The

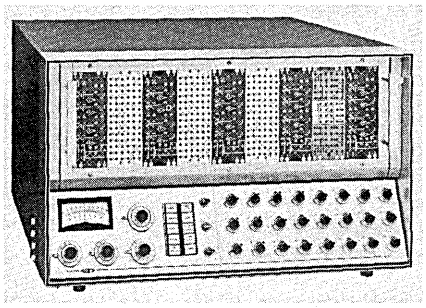


reading unit operates at up to 1,000 cpm, has a "wide-strobe" logic and solid-state read station. Both consoles have self-contained control, logic and interface circuitry, off-line self test facilities.

CIRCLE 143 ON READER CARD

SYSTRON DONNER CORP.
Concord, California
Booth No. 132, 133

Weighing 100 pounds, the SD 10/20 is a portable analog computer being introduced. With a ±100-volt operating range, it features a removable problem board with visual computer



circuits, patchable electronic mode control and patchable integrator time scales. It has a capacity of 20 amplifiers, 16 integrators, eight multipliers, four comparators, 24 pots and four variable diode function generators.

CIRCLE 144 ON READER CARD

TALLY CORP.
Seattle, Washington
Booth No. 500, 501

The System 311 being unveiled is a paper-tape data communications system. Operating at 120 cps (1,200 wpm), the system has an error detect/retransmit feature. Each character is checked after it has been punched; if an error is punched, the 311 will detect it and punch a "flag" character which turns the punch off. The transmitter is then told to back up and retransmit that portion of the tape in which the error was received. The unit is used with the Bell 202C-2 data set.

CIRCLE 145 ON READER CARD

TECH MET INC.
Sunnyvale, California
Booth No. 525

The MAGNEDISC is a removable cobalt-nickel disc that can be used with either flying or contact heads. With a packing-density of more than 5,000 bpi, the capacity of a 12-inch disc is 3.5-million bits. Other diameters are from eight to 24 inches, and service life is said to exceed 10,000 hours. Frequency response is from 10 cycles to 3.8 megacycles.

CIRCLE 146 ON READER CARD

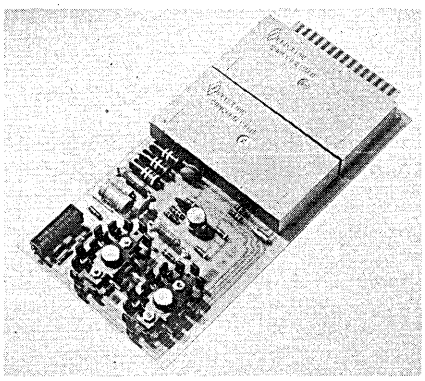
WEST ELEVEN INC.
Los Angeles, California
Booth No. 117

Two analog computers of Japanese origin are the Hitachi 303 (first showing in the U.S.) and the Hitachi 505 (first exhibition anywhere). The 303 is a desk-top unit for gp educational use, and can be expanded from a four- to a 24-amplifier system. Computing voltage is ±50 volts, accuracy of computing components is ±0.5%, and drift is 10 millivolts/hour at unity gain. The 505 is a 40-amplifier, ±100-volt unit with 18 integrator networks, 54 potentiometers, six multiplier networks, and six variable function generator nets.

CIRCLE 147 ON READER CARD

ZELTEX INC.
Concord, California
Booth No. 127, 128

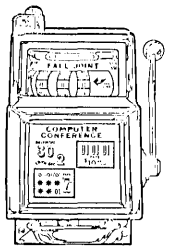
Being introduced is the model 140-B solid-state operational amplifier with a ±100-volt swing at 20 mA for analog



computers and instrumentation. A field-effect transistor chopper circuit with internal drives gives 3 uV/°C maximum drift, and zero offset voltage adjustment is built-in.

CIRCLE 148 ON READER CARD

AT NIGHT



According to the local news bureau, Las Vegas features, among other attractions, 1,031,000 light bulbs and 40 miles of neon tubing in its signs—which cost $5 million to build, use 7,827,000 watts per month and generate an electric bill of $53,500. Behind these signs are the gambling parlors, shows, food, and girls. Gambling is covered elsewhere in this issue. The girls, we understand, are not covered at all. So this section offers some hints on the shows and food.

The shows at the big hotels are included in the price of dinner, which ranges from about $6 to $10 a head. For the late shows, there's usually a two-drink minimum. For this you get to see casts of 50 people 50 and stage efforts that in the recent past have included earthquakes, rainstorms (of special interest to visitors from the New York area), tigers, trapeze acts, skating rinks, disappearing swimming pools, and sinking ships. Here is a list of the shows that are supposed to be on during the days of the convention. Phone numbers are included, because reservations are usually necessary and because this is being written some time in advance when schedules are incomplete and possibly subject to change.

RIVIERA (735-8533). The main attraction here is Eddie Fisher in the Versailles Room. Performers for the Starlight Lounge have not yet been announced.

SAHARA (735-4242). The management announces that Judy Garland will appear in the Congo Room until Dec. 14, when the place will be closed down for alterations.

SANDS (735-3464). Danny Thomas stars in the Copa Room, while the Copa Lounge offers an assortment including Phil Foster, January Jones, and Red Norvo.

STARDUST (735-2545). The Cafe Continental has the 6th All New Edition of Le Lido de Paris Revue. Continuous entertainment by half a dozen groups in the Stardust Lounge.

THUNDERBIRD (735-4111). C'est La Femme, Denise Darcel in the Continental Theatre.

TROPICANA (736-4949). In the Theatre Restaurant is the All New 1965 Folies Bergere. The Blue Room has Vaughn Monroe, the Smart Set, and Gene Baylos. The Gloria Tracy Trio is in the La Fontaine Lounge.

DESERT INN (735-1122). Hello America in the Crystal Room and a series of entertainers in the Lady Luck Lounge.

FLAMINGO (735-5646). The Flamingo Room has Trini Lopez and Totie Fields, with Della Reese appearing in the Driftwood Lounge.

HACIENDA (736-2933). No definite word yet, but may still have the Wonderful World of Burlesque at the Jewel Box Lounge.

DUNES (734-4110). The Casino de Paris, starring Line Renaud, is in the room of the same name. Persian Room offers Vive Les Girls.

For eaters, the big bargains are to be had at the buffets. Times vary for these, but several hotels have both dinners and breakfasts, each running for several hours. Some also add lunch. Prices are in the agreeable range of under $3 for dinner, $1.50 to $2 for breakfast or lunch.

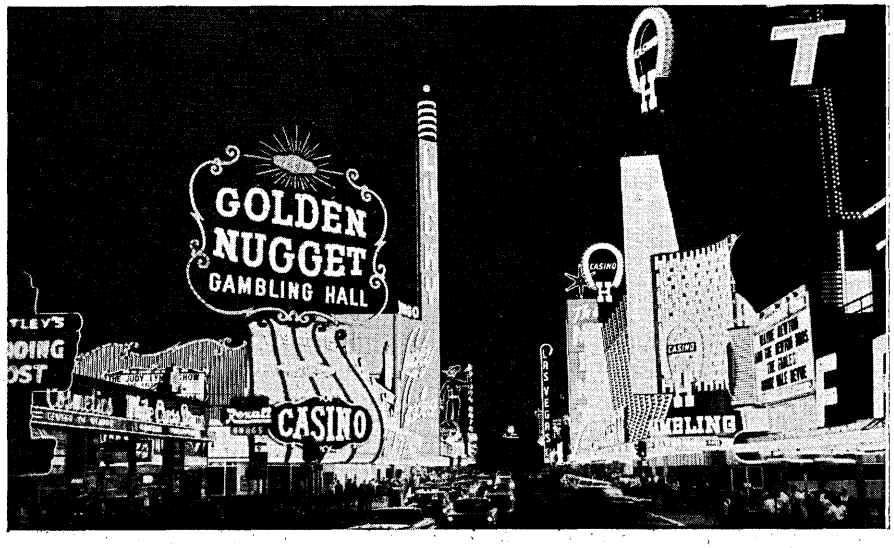
Some 250 other restaurants are available, in addition to those in the hotels and clubs. But you won't go hungry staying close to home.

The Sahara offers Olde English fare at the House of Lords. French cooking can be had at the Dunes' Sultan's Table and the Tropicana's Gourmet Room. Steaks are the feature at the Riviera's Hickory Room. The Polynesian bit is done at the Aku-Aku of the Stardust and the Sahara's Don the Beachcomber. Seafood fans have Joe's Oyster Bar at the Thunderbird and the Dome of the Sea Restaurant.

German/Hungarian types include the Black Forest Inn, the Alpine Inn, and The Danube and, for Mexican food, there's El Cholo, near the strip, and The Macayo in the business district.

The Villa D'Este, next to the convention center, is good for dinner and the Desert Inn has a famous breakfast, featuring fresh berries.

Let's have an eat-only session. ■



CASINOS, CARDS AND COMPUTERS

by DR. ALLAN N. WILSON

There is an empirical formula due to Wilson which expresses the probability of finding a person in a casino, as a function of intelligence Q and time t:
$P(Q,t) = k\,[e^{-(Q-Q)^2} + O(Q) + C(t)]$. The resonance shaped distribution of the first term implies that if one's Q is too low, he can't afford casino life; conversely, the person with too high a Q regards the games as either dull or economically unattractive. O(Q) is a complicated "obstinacy function" which denotes that there are some nonconformists like the author who think they can "beat the game." Finally there is the "computer conference function," which indicates that adroitly arranged but nonetheless bona fide professional activity may occasionally bring one in tempting proximity to the halls of chance.

Those readers who find themselves in the latter fix undoubtedly would like the latest scientific information, to aid them in at least minimizing their losses, and hopefully in maximizing their gains. So we present a table summarizing the player's mathematical "expectation" at each of the popular Las Vegas games, followed by brief comments on the more interesting topics.

Table 1

Game	*Player Expectation (%)*
Keno	—20
Chuck-a-luck	— 8
Slot Machines	— 5 to —25 typical
Roulette	— 5.3
Baccarat	— 1.1[a]
Craps	— 0.8 to —11
Blackjack ("21")	+ 0.1 to + 2 typical[b]

Notes:
[a]There used to be a side bet at baccarat which, like "insurance" at blackjack, was usually an unfavorable bet, but which could occasionally be very favorable. This bet is no longer offered.
[b]This assumes the game is dealt "fair and square"—i.e., there is no manipulation of the cards to vitiate the random deal model used in computer calculations.

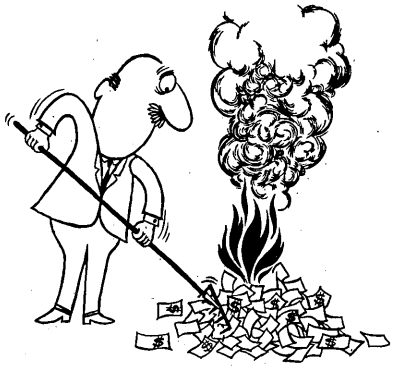
(1) *Keno:* The atrocious house percentage is presumably "justified" on the basis of some potential high payoffs—e.g., maximum 25,000-1 payoff (chance of winning this: 1in8,900,000).

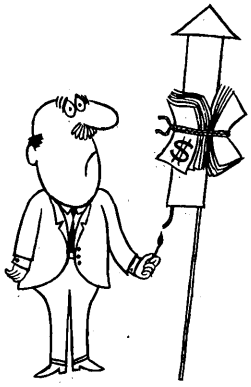
(2) *Chuck-a-luck:* The most common wager appears to the casual observer (unschooled in probability theory) to be better than a 50-50 proposition, but it actually works out to be 7.9% in favor of the house.

(3) *Slot Machines:* Since operation of the machines to capitalize on resonance effects, or other mechanical phenomena, is strongly discouraged by our casino owners

KENO


CHUCK-A-LUCK


BACCARAT

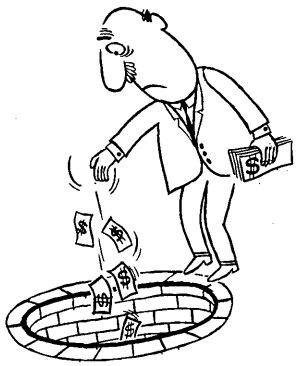

CRAPS

Accustomed to the casino environment, Dr. Wilson is presently associated with General Dynamics/Convair in San Diego, Calif., where he is leader of the analysis group in the analog computer lab. He taught physics for five years at San Diego State and is chairman of the western division of Simulation Councils, Inc. He was educated in New York and California and received his PhD in nuclear physics from the Univ. of California, Berkeley.

(witness their rejection of the Australian experts*), the unfavorable configurations of lemons, bells, etc. result in a generally unpublished but overwhelming house margin.

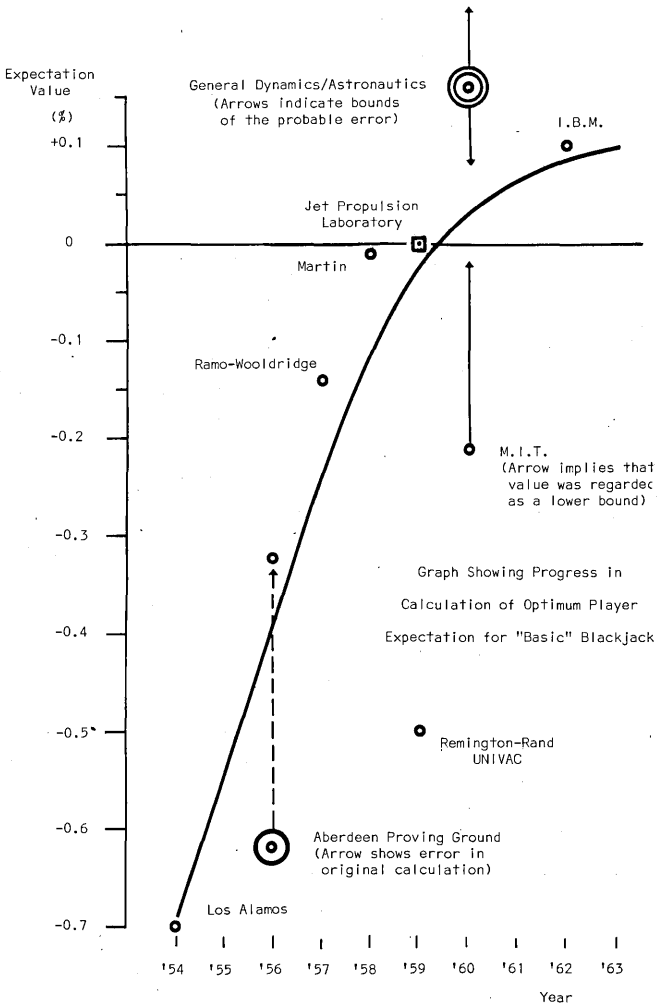
(4) *Roulette:* Statistical prediction, applied either to the physical variations of the wheel or to repetitive aspects of the croupier's manner of spinning the ball and wheel, offers intriguing possibilities of overcoming the nominal 5.3% edge. However, the duration and unobtrusiveness of sampling required probably preclude any such operation during off hours at FJCC.

SLOT MACHINES



ROULETTE

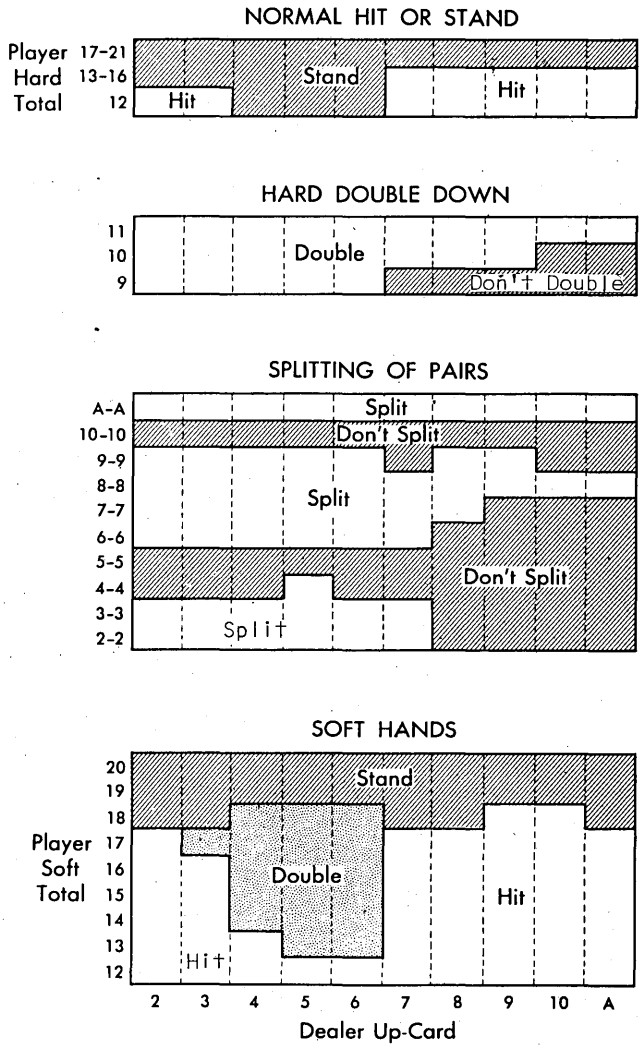
(5) *Baccarat:* This exotic card game yields −1.23% for the player who bets with the "player" hand, and −1.06% for the player who bets with the "banker" hand. The minimum wager is frequently $5, and for a place at the table one must often compete with exhibitionists displaying huge piles of "the green."



(6) *Craps:* By taking, or laying, the odds "on the back line," the crap-shooter may effect an almost 50% reduction of the usual 1.4% margin (in the house's favor) on the pass or don't pass lines. But unless he can exert physical control on the throwing of the dice, that is the irreducible minimum.

(7) *Blackjack:* Unlike the preceding six games, this is a game of *skill* as well as chance, by virtue of the player decisions and the options involved. It was not set up originally with any particular percentage for the house, for until the advent of fast computers, the multiplicity of the card combinations precluded accurate calculation of the odds. Through ignorance of anything close to an optimum strategy, many players give the house an advantage of several percent. But an enlightened player can, at worst, break even in the long run, and with serious effort he can score an overall 1 or 2%, or even better.

Table 2



This remarkable state of affairs is due largely to an understanding of the game gained from computer studies. Indeed, high speed digital computers have been used for blackjack analysis for more than 10 years, a fact which may surprise quite a few readers. Numerous prestigious government, industrial, and academic laboratories have participated (sometimes willy-nilly) in this endeavor. Some of the early investigations were conducted almost secretly,

*These experts found that they could beat the machines in Australia, apparently by pulling down violently on the handle. An attempt to try it in the U.S. resulted in their expulsion from the casino by the manager.

but there was a more pertinent reason for the apparent slow spread of results: early models of the game just happened to err on the pessimistic side, and a number of researchers were discouraged from further pursuit.

The graph shows the history of attempts to compute the player's expectation, for what is called the "basic" game, with fixed bet size and no card memory. The most recent simulations are seen to converge upon a seemingly unbelievable conclusion: the casinos are banking an essentially even game. The price of admission to this rarity is to commit to memory the matrix given in Table 2. The four sections of the matrix are given in decreasing order of importance, and indeed for the beginner the last section on doubling down of "soft" hands (containing an ace counted as 11) can almost be passed over, such a small increment does it add.

The player who is *really* willing to exert himself can do better than break even. Just how much better depends on his proficiency at card memory, and his knowledge of the changing odds. An important point to grasp, however, is that it does not require either a "photographic memory" or a staggering intellect to play superior blackjack. But it does require practice.

As cards are dealt from the deck in successive hands, the probabilities vary. Hence the skilled player regards the preceding matrix, which was derived for *average* probabilities, as just a starting point. The first step in superior play is to place a larger than normal wager when there is an excess of "good" cards (such as aces or 10's) left to be dealt, and hence the player expectation is positive. Conversely, one

should bet less than normal when there is an excess of "poor" cards (such as 5's and 6's) left.

counting cards at blackjack

Various parameters have been devised by various researchers as a measure of the "richness" or "poorness" of the remaining deck. There are simple additive point count methods, and there are more taxing ratio methods. In general, the more demanding a technique is, the greater is its information content, and the higher its payoff. Such a parameter may be used to indicate when to bet more or less than usual, by identifying situations in which the player expectation has shifted from zero to as much as +10% or −10%.

Point counting can also enable a player to effect a second step in superior play, namely to adjust his hitting strategy as a function of his parameter. The original matrix (Table 2) is a binary matrix in the sense that each element is a little box which says yes you should, or no you shouldn't, take a certain action in each given situation. Thus the *average* value of the parameter is such as to favor one action or the other. As the cards are dealt, however, the parameter may increase or decrease. Hence, strictly speaking, the elements of the matrix should be a set of "threshold" values of the parameter, and if the momentary parameter value has shifted away from average and across the threshold, then the usual strategy should be reversed.

As an example, consider the use of the "10's ratio" method, where the parameter used is the ratio of the number of remaining non-10's divided by the number of remaining 10's. (Remember that 10, jack, queen, king each count as 10 in this game). The normal ratio count is $3\frac{6}{16} = 2.25$. Now take the case of a player with 6-5 versus a dealer 10. Normal strategy tells the player to double down on his two card total of 11. But if as cards are dealt out, you reach a point where the ratio count exceeds 2.8, then you should simply hit this 11, and not double down. The depletion of 10's at this point is such that the double down no longer produces the higher expectation.

To do justice to the various point count methods currently in vogue would take many pages. Accordingly the interested reader is referred to two outstanding references, which in the author's opinion are the only books now in print with adequate scientific coverage of the subject: (1) the author's 300-page *Casino Gambler's Guide* (Harper & Row), about half of which is devoted to blackjack, and (2) Ed Thorp's *Beat the Dealer* (Random House), a 225-page book on blackjack alone. Other important aspects of the game covered in these books are (a) the reduction in player expectation when two or more decks are used in-

stead of the standard single deck, (b) the normally *very unfavorable* (−6%) "insurance" bet, which however does become favorable when more than one-third of the remaining cards are 10 value cards, and (c) the various harassments, both legal and illegal, to which the skilled and high betting player may be subjected, even in the large and wealthy casinos on the Las Vegas strip.

Two final items of interest: (1) Some readers may be under the impression that the rules of the game have been changed because of the inroads made by the count players. Actually what happened was that in April 1964 in Las Vegas only, with much publicity, some of the options were removed, thereby lowering the basic expectation to around −1%. However, the reaction among regular casino patrons (mostly regular losers) was so severe that within a few weeks, and with very little attending publicity, the rules changes were rescinded. To the writer's knowledge, as this article is being written, all of the old options are still in effect.

(2) Recently there have appeared slot machines which play blackjack! Each round of cards is dealt "electronically" from a fresh deck, and lighted registers display the cards in play. There are usually 3 or 4 playing positions available on the one deal. Certain of the customary options (such as pair splitting) which would complicate the hardware too much are not offered. So the player suffers a loss of around 1%. However, *some* of these machines pay 2-1 on blackjack, in contrast to the usual 1½-1, and this adds a compensating 2¼%. Thus, provided that the deal is truly random, such machines may well give a net 1% expectation to the astute player who masters the basic matrix!

So what to play? The nervous dilettante is advised to park at a blackjack machine. Card-count play at the tables is strictly for the strong at heart. Although any average bridge player can easily master blackjack point-count theory, successful execution may be another matter. Often it takes a certain dead-pan, lightning-mental-calculator type to make

a go of it amid jibes, distractions, alarming fluctuations, and fast action play. Still, to whatever proficiency one can attain, it pays to try the game with the best odds! A dead even game at the least is an exhilarating place to start.

computer simulations

Let us now return to the specific topic of computers. Although digital computers have been used in the laboratory to furnish a wealth of detail about proper blackjack strategy, the use of such aids "on-line" in the casino is strictly taboo. During the November 1963 Fall Joint Computer Conference in Las Vegas, an LGP-21 from Los Angeles was trundled in to the Tropicana Hotel, and used to assist a blackjack-playing programmer to make his decisions on whether to hit or stand. After an hour, with no bet in excess of $50, and usually much less, he was several hundred dollars ahead. The casino operators were convinced, and that was that! No more hardware tie-ins. Furthermore, it is likely that attempts to subvert this policy via miniaturized consoles and surreptitious communication links will meet with strong disapproval by Nevada gambling authorities. Lots of luck.

Digital computers have been of considerable help as a simulation tool for study of various gambling "systems." A system is a predetermined pattern for varying your bet sizes so that in a sequence of play there is a large chance of winding up with a small win, and a small chance of suffering a large loss; you then hope the latter does not happen. With a number of such successful sequences, it appears that you have overcome the basic odds against you, and defied the omnipotent "law of averages." Now every reader of this magazine has sufficient mathematical savvy to know that, in the long run, this will fail in any game in which the player's expectation is negative on each individual play. You just can't add up a set of minuses and get a plus. For the simpler systems, this can be proved mathematically by direct analysis. But for many of the more intricate systems which have been proposed, direct analysis gets hopelessly involved.

Computers to the rescue. Random number generation techniques may be employed to economically simulate thousands of sequences, and to provide a fully adequate statistical test of the system. This writer was once approached by a crap system player who had consistently won $100-150 on dozens of weekend trips to Nevada over several years. Each of his sequences was intended to yield exactly $1 profit. He wanted to know the probability that his intricate betting arrangement would reach the house limit of $500, at which point the method would have to be aborted.

A run of about a quarter of a million sequences on an IBM 709 took a half hour (a month's play on the crap table)! There were 66 fiascos, for a net loss on paper of $584,000 out of $40,000,000 total wagered. This implied 1.46% for the house, very close to the theoretical 1.41% on the pass line. It was a beautiful exposition of the fact that the percentage expectation in a long, complicated marathon is exactly the same as for an individual bet!

All betting systems will be found to be fallacious when applied to games in which the basic expectation is negative. But when the expectation can be positive, as in blackjack, computer simulation may be extremely helpful in evaluating a system. It can be argued heuristically, for example, that a simple double-up (Martingale) has merit when you play alone through the deck against the dealer, employing correct basic strategy (but not necessarily counting cards for strategy variations). There is a slightly greater than normal chance of winning after a loss, and vice versa. Successive hands through the deck are not independent, or uncorrelated, in contrast with successive tosses of the dice at craps.

This winds up our stochastic briefing for the prospective attendee at FJCC. It will be interesting to see what gaming displays the vendors put on at the exhibits, and whether the casino pit bosses give their usual ha-ha reception to the onslaught of the computer specialists. If you take a fling, here's to a strong positive fluctuation! ■

Nissim

Steel

THE TECHNICAL PROGRAM

by S. NISSIM and T. B. STEEL, JR.

The Technical Program for the 1965 FJCC is introducing in this year's conference several experiments in format in an attempt to better serve the needs of the information processing community. These departures from tradition are not radical but are, we believe, significant in their direction.

Most striking in its variance from past practice is the presentation of a set of five "discuss-only" sessions. Two of these sessions pertain to software subjects and three to hardware fields. The objective of these sessions is the stimulation of *informed discussion.* Preprints of the formal papers were made available a month before the conference so that essentially the entire session can be devoted to an interchange between the audience and the authors.

Effective discussion has been difficult to achieve in past conferences. It can be obtained, however, through this "discuss-only" procedure provided every attendee undertakes to prepare himself in advance. That such sessions can be productive was demonstrated at the IEEE Computer Group conference on "The Impact of Batch-Fabrication on Future Computers." It will succeed at the 1965 FJCC through the active participation, after preparation, of all attendees.

An additional departure from the norm is the absence of a keynote speaker and general session on the initial day of the conference. What has been done instead is the introduction of a special session, which might be called a "keynote session," on the final day of the conference. Rather than a single speech, we plan a series of papers by prominent authors, all relating to the impact of information processing technology on various aspects of modern society. These subjects will range from commerce through government and education to science, and the papers will serve as a focal point for extracting from all the sessions answers to the three questions: "Where are we now?" "Where are we going?" and "How will we affect the world around us?"

Following the papers just mentioned and closing the conference will be an epilogue session, consisting of a panel of distinguished representatives from the information processing community. This panel will undertake the task of articulating the virtues and failings of the conference and attempting to summarize and focus the themes emergent from previous conference activities.

In addition to the sessions noted above, there will be the usual collection of technical sessions, panel discussions and tutorial sessions. The technical program has not been diluted to create innovations; rather, it has been supplemented by them. A casual perusal may leave the reader overwhelmed by the large number of parallel sessions as well as by the intensive schedule. The aim is to create an environment conducive to interdisciplinary exchange of knowledge and experience. Towards this end, less time has been allowed for individual wandering around halls and lobbies talking privately to old cronies and colleagues.

Sessions are two hours in length to permit wider coverage of the technical areas. While some overlapping of topics does occur in order to allow coherent presentation, the sessions and schedules have been organized in a manner tending to minimize conflict. We sincerely *urge* participants *not* to join in the last-day early exodus back home, but rather to stay with us through the epilogue session, experiencing the emergent coherence that only the conference itself, with the individual attendee as an active participant, can create. Special arrangements are being made with the airline companies to facilitate convenient departure after the conclusion of the epilogue session.

We feel that the virtues of past programs have been retained and that the additions and modifications complement tradition. We are looking forward to a rewarding experience in this conference, and urge all readers to join us for it. ■

THE TECHNICAL PROGRAM

Tuesday, 9:30-11:45
Auditorium

Programming Languages

Chairman:
C. H. Davidson
Univ. of Wisconsin
Madison, Wisconsin

In this session will be presented two surveys and three applications papers. Walter Burkhardt's lead-off paper presents a brief survey of universal programming languages, proposes a new method of classification of these languages, shows how many of the existing efforts fit into this classification, and suggests some directions and goals. Second, the large associated area of digital simulation languages receives a critical survey by John Clancy and Mark Fineberg, and characteristics important to both the user and designer, such as format, structure, implementation, and required features, are discussed.

Following the two general papers, three specific applications papers will report on some new developments in language implementation. B. J. Karafin describes a new block diagram compiler for simulation of sampled-data systems, R. G. Tobey reports for his FORMAC group on the FORMAC algorithm for automatic simplification of algebraic expressions, and Melvin Klerer and Jack May describe an ingenious method for implementing the input of graphical symbols which may extend over several lines of coding, called "Two-Dimensional Programming."

Universal Programming Languages and Processors: A Brief Summary and New Concepts, WALTER H. BURKHARDT.

Digital Simulation Languages: A Critique and a Guide, JOHN J. CLANCY and MARK S. FINEBERG.

Automatic Simplification of Mathematical Expressions—the Formac Algorithm, R. G. TOBEY, R. J. BOBROW and S. N. ZILLES.

The New Block Diagram Compiler for Simulation of Sampled Data Systems, B. J. KARAFIN.

Two-Dimensional Programming, MELVIN KLERER and JACK MAY.

Tuesday, 9:30-11:45
Gold Room

Advances in Computer Organization

Chairman:
Arthur J. Critchlow
IBM-ASDD Div.
Los Gatos, California

This session has evolved, almost accidentally, into an exposition of novel control methods in computer organization. These methods, each a marked success in its own sphere, have as a common goal improvement in the cost/performance ratio of the computer system.

Despite the increased emphasis on general purpose computers and compatibility between computers, it is apparent that there is a need for computers with specialized capabilities. This paradox may be explained by noting that a specialized computer may well have general purpose capabilities and yet be exceptionally powerful in a particular application.

New computer applications have arisen in weather analysis and prediction, solution of magneto-hydrodynamics equations in nuclear physics, and pattern recognition in complex situations. In addition, computers are being widely used in specialized control applications as well as in conventional data processing. Furthermore, powerful small computers are beginning to replace mechanical desk-top calculators. In today's competitive world a slight advantage in cost/performance can open a new market large enough to justify some specialization.

W. C. McGee and H. E. Petersen give a fairly detailed account of a possible microprogram controller for a nuclear bubble chamber film scanning system, with some comments on potential controller performance. With this controller, experimental apparatus is automatically operated, not by conventional wired logic, but by a microprogram controlling a very general register configuration and a single logic element.

B. E. Briley describes a control technique which resembles microprogramming in that the instructions correspond to locations in a control memory and are easily changed. Picoprogramming differs in that an instruction is in only one location. A MYRA magnetic memory element at the location identified by the instruction directly produces all the necessary logic level gating pulse trains necessary to execute the corresponding instructions. The PUPP, a prototype computer which uses picoprogramming to provide several advantages in computer operation, is discussed.

The paper by S. Frankel and J. Hernandez describes a valuable method for improving performance while reducing cost in a small delay-line computer. A "silent" period is introduced into the operation of the delay line memory to simplify addressing and synchronization problems. A precession pattern in the memory divorces the rate of information handling from the bit transmission rate of the delay line. The paper includes descriptions of alternative methods of delay-line control and reasons for selecting the present method.

R. H. Fuller and R. M. Bird describe a processor which, in addition to the comparison logic normally provided at each memory word cell in associative memories, provides sufficient logic to make possible multi-write operations.

D. N. Senzig and R. V. Smith describe VAMP (vector arithmetic multi-processor), a powerful computer organization approach aimed at solving such problems as global weather prediction. VAMP operates on a vector. A vector, in the sense used here, is a linear sequence of numbers, possibly a row or column from a matrix. The multiple arithmetic units of VAMP can simultaneously operate on two vectors to obtain a vector result.

Microprogramming for Data Acquisition and Control, W. C. MCGEE and H. E. PETERSEN.

Picoprogramming: A New Approach to Internal Computer Control, B. E. BRILEY.

A Precession Pattern in a Delay Line Memory, S. P. FRANKEL and J. HERNANDEZ.

An Associative Parallel Processor With Application to Picture Processing, R. M. BIRD and R. H. FULLER.

Computer Organization for Array Processing, D. N. SENZIG and R. V. SMITH.

Tuesday, 9:30-11:45
Room 15

Efficiency and Management of Computer Installations

Chairman:
M. H. Halstead
Lockheed Missiles & Space Corp.
Sunnyvale, California

The session on "Efficiency and Management of Computer Installations" presents a group of excellent speakers which includes both "Doers" and "Thinkers" in this field. Corpo-

Halstead *Davidson* *Critchlow*



rate officers, directors and managers will describe problems and solutions as seen from their own positions, consultants and experts will cover some fascinating middle ground, and their academic colleagues will present some penetrating analyses.

Efficiency and Management of University Computing Systems, H. D. HUSKEY.

Management Problems of Aerospace Computer Centers, G. A. GARRETT

The Multi-Discipline Approach: A Marketing Application, B. G. MENDELSON.

Organizational Philosophy and the Computer Center, M. H. GOTTERER and A. W. STALNAKER.

Planning for Generalized Business Systems, ROBERT V. HEAD.

Computer Systems Design and Analysis Through Simulation, G. K. HUTCHINSON and J. N. MAGUIRE.

Basic Concepts for Planning an Electronic Data Processing System, A. F. MORAVEC.

Tuesday, 9:30-11:45
Room 14

The Computer Industry in the Buyer's Market
A Panel Discussion

Chairman:
Joseph A. Ricca
Raytheon Computer
Santa Ana, California

The computer industry appears now to have entered a "buyer's market." By definition, a buyer's market is one where the user has a wide variety of choices at attractive prices. These requirements would seem to imply that engineering innovation will be stifled in the conformity required by technical standardization. Does this mean that research and development will now take a secondary position to marketing and manufacturing? Will highly automated production lines reduce costs dramatically but also hold back product improvements because of financial inertia? Will the business manager take over from the scientist in the management of our industry? Our panel will examine these issues and other important aspects of the computer industry during this period of change resulting in the buyer's market.

Tuesday, 9:30-11:45
Room 3

Future Hardware Technologies
A Tutorial Session

Session A: William H. Hartwig, Univ. of Texas
Session B: Linder C. Hobbs, Hobbs Associates

A: TECHNOLOGIES FOR FUTURE COMPUTERS

Hitherto unexploited physical phenomena will become the technological basis for computer components in the distant future. Developments to be anticipated on a shorter time scale are already evident in research on superconducting and magnetic thin film logic and memory planes. Existing technologies may have reached saturation in efforts to increase component density, reduce cycle times, and limit energy density. Future efforts will yield greater gains in reliability and economy of fabrication. Design of read-in, read-out, logic, memory, and auxiliary function circuitry will also influence the technology of computer fabrication.

B: ADVANCED STORAGE TECHNIQUES AND THEIR IMPACT ON FUTURE COMPUTERS

The well proved magnetic core still remains the basic element of most computer memories. However, numerous basic avenues are being pursued to obtain a new generation of digital memories. These include cylindrical and thin magnetic films, ferro-acoustic techniques, cryogenic and semiconductor technologies. To date almost all research and development work undertaken in these technologies has come to grips with the problem of yield. The session is devoted to a tutorial type review and evaluation of new approaches and a close examination of their potential impact on future computer system design.

Tuesday, 1:30-3:30
Auditorium

A New Remote Accessed Man-Machine System

Chairman:
Edward L. Glaser
MIT Project MAC
Cambridge, Massachusetts

It is sad to report that the computer field is as fickle as the field of ladies fashions: both can be swept by fads on almost a yearly basis. We periodically hear those around us say that the computer field is truly reaching maturity. Unfortunately, often this only means that the fads take two years to sweep the field. Because of this environment it is often difficult to determine whether a new view of computation is truly a catchword, another fad, or in reality a major change in the direction of computation.

By the time of the IFIP conference in New York, there was little question of the fact that this year's favorite buzz word was "time-sharing." All kinds of companies and organizations claim: "We have time-sharing!" This definition of time-sharing can mean anything from an airlines reservation system, a true on-line general purpose time-sharing system, to a multiprogrammed batch processing environment.

One of several installations where general purpose time-sharing experience has been gained over the last several years is Project MAC at MIT. A project of the Advanced Research Projects Agency, the Department of Defense, MAC was established to investigate the various problems of establishing a true general purpose time-sharing computation system. In 1964, it was decided that a new and more advanced form of time-sharing system was required. At this time it was determined also that two other organiza-

tions, the Bell Telephone Laboratories and the Computer Dept. of the General Electric Co., were interested in similar goals. As a result of this mutual interest, a joint cooperative venture was begun to produce what has now come to be known as the MULTICS system. MULTICS is an acronym for multiplexed information and computing service. This system is not yet operational, and therefore it is the purpose of this session to describe what the system is and why it is being structured the way it has been.

Introduction and Overview of the Multics System, F. J. CORBATO and V. A. VYSSOTSKY.

System Design of the GE 645 Computer for Time-Sharing Application, E. L. GLASER, J. F. COULEUR and G. A. OLIVER.

Structure of the Multics Supervisor for the GE 645, V. A. VYSSOTSKY, F. J. CORBATO and R. M. GRAHAM.

A General Purpose File System for Secondary Storage, R. C. DALEY and P. G. NEUMANN.

Communications and Input-Output Switching in a Multiplex Computer System, S. D. DUNTEN, L. MIKUS and J. F. OSSANNA.

Some Thoughts About the Social Implications of Accessible Computing, E. E. DAVID, JR. and R. M. FANO.

Tuesday, 1:30-3:30
Gold Room

Applications of Simulation

Chairman:
Paul Brock
The RAND Corporation
Santa Monica, California

The technological revolution into which our generation has been catapulted by the development of electronic computation and data processing equipment is expanding at an unprecedented rate. We, the faithful, believe that its ultimate effect will be a boon to humanity once the accompanying sociological problems are solved and the normal social lag is absorbed. So, on with the revolution!

Advances have been and will be achieved through a bilateral process. Equipment is designed and developed, then it is applied and its applications are extended. Dually, as applications are found and the subject technology extended, new requirements and specifications are created—to be reflected in new equipment designs.

Foremost in the advance of application tools is the technique of computer simulation. The computer with its inbuilt decision making and computational capability and with extensive high-speed storage has been able to emulate real processes analytically and empirically.

Dr. E. Levine will discuss the impact of simulation on military science. Dr. T. W. Murphy represents the medical field with a discussion of the simulation of respiration. Dr. A. J. Rowe applies simulation to problems of corporate management, and Dr. E. A. Bowles considers simulation as a tool that has advanced research in the humanities. Dr. L. Fein, as anchor man, will discuss simulation for information processing, a newly evolving academic discipline in its own right.

Structure and Dynamics of Military Simulations, E. LEVINE.

Analogue-Digital Data Processing of Respiratory Parameters, T. W. MURPHY.

Computer Simulation: A Solution Technique for Management Problems, A. J. ROWE.

The Role of the Computer in Humanistic Scholarship, E. A. BOWLES.

The Structure and Character of Useful Information Processing Simulations, L. FEIN.

Tuesday, 1:30-3:30
Room 15

Natural Language Processing

Chairman:
David Hays
The RAND Corporation
Santa Monica, California

After a decade of slow development—centered around machine translation and automatic storage and retrieval of scientific information—computational linguistics seems ready to expand rapidly. Courses are appearing in many college catalogs, college and research libraries are automating catalog production, computer aids in the publication process (from typing of the initial manuscript through final typesetting) is expanding, automatic parsers for natural languages and programming languages are fairly well understood, a magnetic tape format for text storage is being adopted as a standard, and research projects are spreading from more elaborate retrieval systems to deeper involvement with semantics.

This session, one of four in and around FJCC on computational linguistics and closely related subjects, has space for only a few of these topics; but taken together with papers and discussions in other sessions, they contribute to a general view of the newest and best work in the field.

Catalogs: A Flexible Data Structure for Magnetic Tape, MARTIN KAY and THEODORE ZIEHE.

Information Search Optimization and Iterative Retrieval Techniques, J. J. ROCCHIO and G. SALTON.

An Economical Program for Limited Parsing of English, D. C. CLARKE and R. E. WALL.

The MITRE Syntactic Analysis Procedure for Transformational Grammars, ARNOLD M. ZWICKY, JOYCE FRIEDMAN, BARBARA C. HALL and DONALD E. WALKER.

Tuesday, 1:30-3:30
Room 14

Cellular Techniques for Logic, Memory and Systems

Robert C. Minnick
Stanford Research Institute
Menlo Park, California

Possibly the most important present trend in the field of digital circuits is the rapid emergence of practical, reliable and economical *batch-fabricated* components. The best known example of these fast-growing technologies is the monolithic integrated circuit; other important examples are cryogenics and highly miniature vacuum devices.

While logical designers and systems designers have dealt with individual components, such as transistors, diodes, and so on, the rapid development of these new technologies will soon give these designers a large quantity of interconnected components on a single substrate. Therefore, a burden is placed on them to reformulate their procedures to be more compatible with the new methods of manufacture.

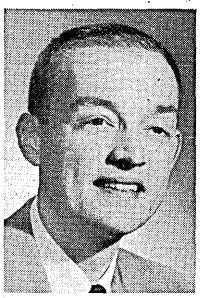
The purpose of this session is to investigate an important approach to the solution of this problem—an approach that uses *cellular techniques*. While the variety of cellular techniques is quite large, they all rely on the use of large arrays of interconnected *cells*. The cells are the fundamental logical building blocks, and they may be as simple as a majority gate or as complex as an entire computer.

A core memory plane is a cellular array, as is a matrix-organized diode array. Recent research, however, including that of the speakers at this session, has shown that much more efficient and generally useful cellular arrays can be designed.

An attempt will be made at the session to discuss whether modern cellular techniques, when they are used in connection with the emerging batch fabrication technology, make practical sense.

In the first paper, I discuss a cobweb cellular array, a two-dimensional array of single-output digital cells that are disposed on a square grid. Associated with each cell is a horizontal and a vertical buss as well as three inputs from nearby cells. The logical functions produced by each cell are the same logically complete set of six functions previously reported in connection with cutpoint cellular arrays. It is shown that the use of cobweb arrays allows the logical designer more design flexibility than he has when using cutpoint arrays.

Hayes *Glaser* *Bobrow*



A study, reported on by Rudd H. Canaday, has been made of two-dimensional arrays of three-input one-output gates, or elements, each element realizing the "majority" function ($f(A,B,C) = AB + AC + BC$). Two methods are developed for synthesizing any given Boolean function in an array. The first method results in an array whose size depends on the particular function being realized. The second method results in an array whose size depends only on the number of variables in the function being realized.

Robert A. Short discusses two-rail cellular cascades. An important synthesis problem in the design of cellular logic arrays is the development of techniques for the realization of arbitrary switching functions within a given array—i.e., the design of general-function arrays. A useful technique for such realizations has been to compose the required functions by "collecting" the contributions of an appropriate set of subfunctions that are individually formed in the columns of the array.

B. T. McKeever discusses the Associative Structure Computer, a cellular array of subarrays establishing a uniform but flexible interconnection scheme. ASC has a hierarchy of distributed stored logic, flexible so that two functional modules in uniformly wired stacks may be used for a variety of machines, but circumventing the usual limiting of system speed by control memory read rate and avoiding either extreme of monolithic centralized or diffuse localized control. ASC has a hierarchy of languages ranging from the small set of primitive information manipulations built into the hardware to interpretive subroutines for user selected and modifiable languages.

Cobweb Cellular Arrays, R. C. MINNICK.
Two-Dimensional Iterative Logic, R. H. CANADAY.
Two-Rail Cellular Cascades, R. A. SHORT.
Associative Memory Structure, B. T. MCKEEVER.

Tuesday, 1:30-3:30
Room 3

Time-Sharing in the Real World
A Tutorial Session

Ed Bryan, The RAND Corporation
Richard E. Kaylor, Informatics Inc.
Arthur Rosenberg, Scientific Data Systems

The seemingly magic term, "time-sharing," is the subject of a great deal of popular interest, controversy, and confusion. It stimulates some members of the computing community to become prophets, others to become defensive. It attracts the attention of the "outsiders," the real-world users. Above all, it provides another step forward in the practical utilization of computers.

This session is tutorial in nature for those persons in a position to contribute to the successful exploitation of time-sharing. Such people range in computer involvement from hardware design through corporate management.

The session covers three aspects of time-sharing systems:

The real significance and impact of multi-usage interactive computer utilization is presented as a fundamental key to the future of time-sharing.

A discussion of hardware and software considerations is used to describe the fundamental operations and implementation needs of such systems.

Finally, the significant role of communication facilities in conjunction with computer processing is evaluated in the light of current developments.

Tuesday, 3:45-5:45
Auditorium

On-Line Interactive Software Systems
A Discuss-Only Session

Chairman:
Daniel Bobrow
Bolt, Beranek & Newman
Cambridge, Massachusetts

On-line operation of computers has long been popular with programmers working with small machines. On these machines, intimate man-computer interaction is economically feasible, even though the central processor may sit idle much of the time. With time-sharing, large and expensive computing facilities have been used to provide economical responsive service for programmers. However, the use of on-line systems is being extended far beyond the limits of the programming community, to military planners and businessmen, to engineers and mathematicians. In this session, we are concerned with some software developments which allow a number of different classes of users to interact on-line with responsive systems.

Machine language programming is simplified by the IMP system, which allows integrated program writing, editing, compiling, debugging and patching. During debugging, done in symbolic, changes made in the binary program can be automatically incorporated into the symbolic listing. Macros are available for editing as well as for assembly, and all input for both assembling and debugging goes through the same processor.

A paradigm for the construction of higher level language on-line systems is illustrated by an on-line incremental compiler and debugger for ALGOL programs. The basic unit of an ALGOL program is the "statement," and a programmer using this on-line system can control the execution, debugging, and modification of his program in terms of this basic unit in the higher level language.

A civil engineer using an on-line system wants to talk about bridge structures and highway foundations, not about subroutines and calling sequences. He needs to have available a number of tools to deal with various engineering problems which arise. ICES provides a hierarchical, integrated system for civil-engineering design, accessed through a well-designed interaction language.

Despite a popular misconception, mathematicians rarely

deal with numbers. MATHLAB is a start toward providing aid in symbolic manipulation. Substitution, symbolic differentiation and integration are available in this system.

Computers are gradually becoming more adept at the storage, and retrieval of large quantities of information. AESOP is an experimental on-line information control system with very flexible input and output. A novice is led through operations step by step, but a sophisticated user can immediately specify a complete sequence of operations.

Finally, business has started to recognize the advantages of on-line data processing: timeliness, cost reduction and control. These advantages and possible facilities are illustrated in the description of the KEYDATA system.

Tuesday, 3:45-5:45
Gold Room

The Revolution in Written Communication

Margaret T. Fischer, Time Inc.
W. B. Kehl, Univ. of Pittsburgh

This is the first time there has been a session on this topic. It deals with the potential contribution of computers in the total creative process of communication through the written word. If this sounds like biting off too big a piece of cake, it is meant to be. For what is involved is not the automation of the printing industry, nor the mechanization of a library file. But it implies fundamental changes in every phase of authorship.

In the two papers presented, new developments to make this possible are described. They include the author-machine interaction at a computer visual display, editing and manipulating his "draft." They include new equipment (and ideas for new equipment) for not only this but also for high-speed typesetting.

The two papers in the session are devoted to advanced developments which have never been presented before. The first is a project at Bell Laboratories which emphasizes some new technological developments. The second describes research at the Univ. of Pittsburgh under Defense Dept. support of new software systems.

Computer Editing, Typesetting and Image Generation, M. V. MATHEWS and JOAN E. MILLER.

The Left Hand of Scholarship: Computer Experiments with Recorded Text as a Communication Medium, GLENN E. ROUDABUSH, CHARLES R. T. BACON, R. BRUCE BRIGGS, JAMES A. FIERST, DALE W. ISNER and HIROSHI A. NOGUNI.

Tuesday, 3:45-5:45
Room 15

High Speed Computer Logic Circuits

Chairman:
D. Ackley
Texas Instruments Inc.
Dallas, Texas

This session deals with the logic circuits used in high speed computers. Some of the system considerations which govern the choice and design of logic circuits are outlined. The various trade-offs used in logic arrays, the various packaging schemes and speed vs power are considered. Reflection and cross-talk considerations in interconnecting the high speed logic circuits are discussed.

Circuit Implementation of High Speed Pipeline Systems, LEONARD W. COTTON.

High Speed Logic Circuit Considerations, W. H. HOWE.

Crosstalk and Reflections in High Speed Digital Systems, A. FELLER, H. R. KAUPP and J. J. DIGIACOMO.

TECHNICAL PROGRAM...

Tuesday, 3:45-5:45
Room 14

Computers in the Biological and Social Sciences

Chairman:
Ward Sangren
Computer Applications, Inc.
San Diego, California

Every facet of our society is feeling the impact of digital computers. The applications are becoming extensive not only in the accepted fields of engineering and business, but also in such fields as biomedical research and in the behavioral and social sciences. Five technical papers are presented on these latter topics in this session: three on biomedical applications, one on social sciences, and one on behavioral science.

The paper by Hiltz on *Computer Correlation Analysis of Intracellular Neuronal Responses* notes that the full potential of digital computers in the biomedical disciplines is not even in sight. The biomedical investigator need no longer spend a large amount of his time and effort manually reducing raw data, but may now utilize the automatic techniques of computers.

Mitchell *Fischer* *Dennis*

Mr. Steinborn in his paper on *Nonlinear Regression Models in Biology* is more abstractly concerned with the isomorphism that exists between biological processes and the real number system. The mathematical-biological models expressing this isomorphism have as a purpose the gaining of insight into biological phenomena and the ability to predict a response for a given set of input.

The third biomedical paper is concerned with the use of chemical agents in the treatment of cancer. A discussion is given of the statistical center in Buffalo which is responsible for the implementation, control and follow up of these chemotherapy studies. The computer system for handling this diverse and extensive data is also outlined.

The paper by Ball, dealing with data analysis in the social sciences, is similar to the other papers in the session in that much reference is made to statistical methods and to the eventual use of a digital computer. The author's prime objective is to outline a body of computer oriented techniques called "cluster seeking" which may take the place of present statistical techniques.

The remaining paper deals with the implication of the computer for the behavioral scientist. The paper indicates that the computer is affecting the research efforts of the behavioral scientist by: (1) providing a more powerful tool for the statistical analysis of his data, (2) providing a means of simulating a system of complex interacting variables, and (3) requiring new data on the effects of automation in the changing economic environment.

Integrating Computers Into Behavioral Science Research, HAROLD BORKO.

Data Analysis in the Social Sciences, GEOFFREY H. BALL.

Nonlinear Regression Models in Biology, JOSEPH A. STEINBORN.

Computer Correlation of Intracellular Neuronal Responses, FREDERICK F. HILTZ.

Information Processing of Cancer Chemotherapy Data, ALICE HOLMES and ROBERT K. AUSMAN.

Tuesday, 8-10 p.m.
Gold Room

Extra-Sensory Perception and Man-Machine Communications
A Panel Discussion

Chairman:
J. B. Rhine
Duke University
Durham, North Carolina

With all advanced computer organizations, the direct coupling between the user and the computer still remains the weakest link in a digital system.

Parapsychology deals with psi communication, a mode of extra-sensorimotor exchange between a person and his environment. This means of communication is not only independent of the sense organs and muscles, but equally so of any known energetic basis. Accordingly, since it is measurably effective, even though as yet with a very low order of controllability and efficiency, it can only be accounted for by some nonphysical influence or energetic principle in nature.

Tuesday, 8-10 p.m.
Room 15

Block Oriented Random Access Memory Techniques
A Panel Discussion

Chairman:
D. Haratz
U.S. Army Electronics Command
Ft. Monmouth, New Jersey

The concept of an all-electronic block oriented random access memory (BORAM) for use as a computer secondary memory has been introduced. The concept exists in the form of a set of performance requirements rather than a specific hardware implementation. The performance requirements are derived from the intended usage as a generalized secondary memory for all computer applications.

The purpose of this panel is to discuss a number of possible implementations, which are in various stages of development, and to attempt to discover the assets and liabilities of these techniques to implement the BORAM concept.

Tuesday, 8-10 p.m.
Room 14

The Future of Electro-Mechanical Mass Storage
A Panel Discussion

Chairman:
William A. Farrand
Autonetics
Anaheim, California

Subjects that will be discussed include file efficiency factors in terms of peak data rate, data latency time, average data rate, and necessary housekeeping and bookkeeping associated with the files. Efficiency factors at present computing installations will serve as background for estimating future work loads and desired future file properties. Factors, such as independent arm access, content addressing, extended I/O multiplicity, self-contained file management, hierarchical file structure, use of files as autonomous peripherals, and other potential future characteristics of electromechanical stores will be discussed.

Wednesday, 9:30-11:30
Auditorium

Time-Shared Computer Systems A Discuss-Only Session

Chairman:
Jack Dennis
MIT Project MAC
Cambridge, Massachusetts

The past two years have witnessed a substantial influence on central processing hardware by improved understanding of the design problems of multiprogramming software for time-shared computer systems. Paging, segmenting, and protection mechanisms have been designed that are far more sophisticated than past practice would consider expedient.

These hardware developments have been motivated by the practical difficulties of main memory allocation, shared access to data and procedure segments, and the protection of information against unauthorized access. In turn, the provision of more powerful addressing mechanisms has made possible the creation of a new generation of time-sharing executive programs that greatly facilitate shared use of procedures and data by a community of users.

The papers in this session will describe the hardware/software approaches taken by several independent group efforts in time-shared system design. After the presentation a panel will contrast the approaches and discuss their influence on the character of future data processing systems. Panelists are David C. Evans, Univ. of California; James W. Forgie, MIT Lincoln Laboratory; Kermith W. Speierman, Burroughs-Paoli; and Watts S. Humphrey Jr., IBM.

In order to provide facility for experimentation in man-machine interaction, a time-sharing system providing fast response for a limited number of users has been developed. The system, described by Lichtenberger and Pirtle, provides each user with a variety of services ranging from machine language to sophisticated sub-systems and higher level languages. The system utilizes a memory paging technique and high-speed drum to derive a capability for both memory sharing and memory swapping.

An experimental operation-oriented system for the on-line analysis of data is being developed for the TX-2 computer at the MIT Lincoln Laboratory. Forgie describes the executive program that has been designed to satisfy the needs of that system, as well as the needs of the other activities currently employing the computational energies of TX-2. These various needs are developed into a set of requirements for a fast-response, time-sharing system. The requirements, in turn, lead to a series of design decisions that involve hardware, software, and the interaction between them. The design takes the form of a complex of apparent computers, one for each console, which share time, memory, and programs in the real computer (TX-2).

McCullough, Speierman, and Zurcher describe the Burroughs B8500 system design, predicated on a multiprogramming-multiprocessing mode of operation where all user programs are in a uniform structure, with emphasis placed upon program and data segmentation. The functional operation of the hardware was strongly influenced by requirements for relative addressing, reference to independently allocated data and program segments via descriptors, memory protection, and shared use of program and data segments.

Recognizing the potential significance of time-sharing as a way of operating a computing system, IBM has developed a special machine within System/360—the Model 67—and a special programming support package, the objective of which is to provide a user at a console with effectively fingertip control over the system in the solution

of his computing problem. Comfort's paper discusses some major system characteristics and hardware features.

Wednesday, 9:30-11:30
Gold Room

Scratchpad Memories
A Discuss-Only Session

Chairman:
Gordon Mitchell
Director, NSA
Ft. George G. Meade, Maryland

Some form of scratchpad memory can be found in most computer systems. They range from simple flip-flop registers up to 256-word ferrite core or magnetic thin film memories. They are used for a multiplicity of functions, such as index registers, I/O channel control registers, arithmetic registers, and other central processor registers. The increasing popularity of scratchpad memories is due to:

(1) Improved technology and decreased cost in the high-speed memory area, and

(2) Increased complexity in computer systems.

The six papers in this session are concerned with hardware approaches to, and systems utilization of, scratchpad memories. Three papers describe how the Burroughs B8500, the RCA Spectra 70, and the Honeywell computer systems use scratchpad memories, and how these memories enhance the performance of the systems. The other three papers describe the design and operation of fast scratchpad memories which use tunnel diodes, integrated circuit latches, and magnetic thin films as the storage elements.

Wednesday, 9:30-11:30
Room 15

Arithmetic Techniques and Systems

Chairman:
Lowell D. Amdahl
COMPATA
Tarzana, California

To the computer designer, the arithmetic section is a major part of the battlefield where the price/performance war is fought. Improved weapons are brought into use to maintain established positions, and totally new weapons are devised for daring assaults. These weapons range from improved circuits and carry bypass techniques, to algorithms which are more parallel or which employ new representations for numbers.

This year's call for papers produced good descriptions of new weaponry. For improved carry handling, Kruy describes a circuit technique for carry bypassing which employs tunnel diodes in conjunction with monolithic integrated circuits. Average logic propagation delays of a fraction of a nanosecond per stage are reported.

Katell describes a carry improvement resulting from recoding operands into a redundant ternary form. He suggests that such representations might even be employed with advantage for general internal use in a computer.

Checking of errors introduced by faulty arithmetic components is discussed in the paper by Davis. Error detection properties of residue check codes and binary logarithms are analyzed. The logarithmic check would be an order-of-magnitude verification of results.

Lee, Lehman and Senzig examine the tradeoffs associated with byte-serial processing. More complex techniques for multiplication such as adder-array structures are discussed, showing them to be fast and relatively inexpensive.

In all, this session provides a good cross section of research and development efforts in arithmetic methods.

A Bounded Carry Inspection Adder for Fast Parallel Arithmetic, EMANUEL KATELL.

A Fast Conditional Sum Adder Using Carry Bypass Logic, JOSEPH F. KRUY.

A Checking Arithmetic Unit, RICHARD A. DAVIS.

Serial Arithmetic Techniques, M. LEHMAN, D. SENZIG and J. LEE.

Wednesday, 9:30-11:30
Room 14

The Overseas Computer Market
A Panel Discussion

Chairman:
Daniel L. Goldy
Department of Commerce
Washington, D.C.

Industry and governmental officials familiar with many of the challenges and opportunities for marketing American computers and systems abroad will focus on four key areas. These are: the American company's relations with foreign governments; the prospect for increased trade with the Soviet bloc; building a market for computers in the less developed countries; and that of providing sound, fully competitive export financing for American computers in the emerging nations.

Wednesday, 9:30-11:30
Room 3

Two-Wire Extended Core Memories & Computer Organizations
A Panel Discussion

Chairman:
M. Rosenberg
Electronic Memories Inc.
Hawthorne, California

The development of high speed, low cost extended core memory techniques is having an impact on the system organization of new computer designs. For most applications, the desirable configuration would be to have one hierarchy of memory. Of course, mundane items such as cost and technical feasibility prohibit this approach.

The extended core memory technique (mass memory) is thought of as an additional hierarchy of memory. To date, the boundary line between the upper end of existing high speed core and the lower end of the extended core is thought of as somewhere between one and ten megabits. It is submitted that this is a very temporary artificial boundary and that cost and technical breakthroughs will make this boundary highly flexible within the next few years. The upper end of the extended core is now considered to be 10^8 bits.

The session will explore the following areas: a. General organization of extended core memories for maximum through-put; b. Speed range vs. size of extended core memories; c. Will there be two hierarchies of core—if so, how long? d. Assuming two hierarchies, what is the boundary between them in size, speed and cost?

Wednesday, 1:30-3:30
Auditorium

Simulation of Human Behavior

Chairman:
Kenneth Kolence
Control Data Corp.
Palo Alto, California

The history of scientific thought has as one of its main

themes the development and testing of theories. A secondary theme, which in some sense is highlighted in this session, is the development of techniques and devices for obtaining the data necessary to the formulation and testing of these theories. The three papers in this session discuss efforts to develop computer programs into such a technique or device in the realm of behavioral sciences.

The first paper, by Carl E. Helm, discusses an investigation into the methods used by psychologists to evaluate an individual's performance on a battery of personality and aptitude tests. Typically, these tests are inter-related in such a manner as to require an interpretation of the overall results. It was a goal of these researches to develop a sufficiently explicit theory of how this is done by an individual to permit computer generation of similar material. In the process of this work, a special problem-oriented language was developed for the 7094 to facilitate the expression of alternate theories as computer programs.

The second paper, by Nicholas V. Findler, goes into this possibility even more deeply, albeit with different subject matter. The paper describes a series of experiments in which students were placed in a situation which required them to optimize a process being simulated on a small computer. They were permitted to vary certain input values which resulted in new output values for the process. The strategies they adopted to find the optimum input values were determined by having them verbalize their thoughts and recording these statements on tape.

The third paper in the session, by Gene R. Bussey, differs from the others in that it does not use actual situations as the base from which theoretical development occurs. It is similar to the second paper in two important respects: the use of two programs running in the same machine to describe an interaction between two "individuals," and its concern with the problems of developing a strategy of response appropriate to a situation. It is closer conceptually to the problems of artificial intelligence than the other papers. Essentially, it describes experiments wherein one program (PUPIL) attempts to adapt positively to a limited environment on the basis of reinforcement information provided by a second program (TUTOR). Considerations representing novelty, organization improvement, and rewards or usefulness measures are built into PUPIL, which uses the values for these to determine its actions within the environment. The paper describes in detail both the considerations that have gone into the programs and the results obtained to date.

Simulation Models for Psychometric Theories, C. E. HELM.

Human Decision Making Under Uncertainty and Risk: Computer-Based Experiments and a Heuristic Simulation Program, N. V. FINDLER.

Computer Experiments in Motor Learning, G. R. BUSSEY.

Wednesday, 1:30-3:30
Gold Room

High-Speed Read Only Memories
A Discuss-Only Session

Chairman:
J. Reese Brown
ElectroData Div., Burroughs
Pasadena, California

New computer systems are more and more using read-only memories in their internal structure. These memories range in size from a few hundred to a few thousand words and are used to store logic and control functions which are never or rarely altered. The major emphasis in most systems is on very high speed and low cost.

Organized to try to present a comprehensive look at the present and future of the hardware aspects of high speed read-only memories, the session will present four formal published papers. These are followed by three panelists who will discuss several other read-only memory techniques.

The session starts with a survey paper which will take a general look at the whole field. The read-only memory

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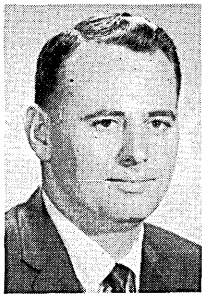


Kolence

is considered as a matrix in which the information is stored as a pattern of coupling elements at the cross points of the matrix. The coupling elements can be linear devices, such as resistors, capacitors or transformers, or can be non-linear devices such as diodes, transistors or non-linear magnetic elements. The paper will discuss the characteristics and fabrication of the different forms and will make some comparisons between them.

The other three published papers describe three techniques in which a magnetic device forms the coupling element.

The first one is made of a woven matrix in which copper wires are woven with permaloy plated wires. The storage is contained in the weaving pattern. The matrix is driven on the copper wires and sensed on the plated wires. The paper reviews the magnetic characteristics of the plated thin film element and the overall electrical characteristics of the array. A system using the array is described.

The next paper describes a memory in which a linear transformer is used as the coupling element to store information. The memory is made of a group of ferrite E cores, one for each bit of the storage word. The center leg of each core has a sense winding on it. The primary of the transformers is formed by laying a series of word wires in one or the other of the apertures to store a "1" or a "0." Each wire will link all cores, thus storing one word. A set of matching E cores is used to complete the magnetic circuit. The paper discusses the general principles of the memory array and gives typical electrical and performance characteristics. The organization of a system is described and the characteristics of a 1,024-word, 24-bit system is given.

The last paper describes a memory technique which might have some application to read-only memories in the future. Described is a technique in which thin permaloy films are non-destructively sensed using microwaves. The system utilizes the ferro-magnetic resonance characteristics of thin permaloy films. The basic phenomenon and its application to memories is described. A description of a 32-word, 24-bit memory is given. Its operating characteristics are given and a few comments are made on the problems encountered in the program.

The authors of the formal papers will not read them in their entirety but will give a short five minute summary of the key points of the papers. They will be followed by three panelists who will give brief summaries of the characteristics of other types of read-only memories.

Wednesday, 1:30-3:30
Room 15

Input/Output Equipment for Closer Man-Machine Interface

Chairman:
J. S. Craver
Hobbs Associates
Corona Del Mar, California

Off-line use of computers has allowed the user time to convert problems into machine language. On-line use requires a faster exchange of information and demands input/output systems that can accept data without conversion into machine language. This session is devoted to input/output devices and techniques which can function on-line with a computer system and accept or generate data in a form that is directly understandable by the operator. The papers presented describe equipment suitable for on-line input/output of graphical data and remote output of computer composed voice messages. Attention is given to the design, control and application of equipment, and to its probable impact on future systems design.

MAGIC: A Machine for Automatic Graphics Interface to a Computer, D. E. RIPPY, D. E. HUMPHRIES and J. A. CUNNINGHAM.

A Magnetic Device for Computer Graphic Input, M. H. LEWIN.

GRAPHIC 1—A Remote Graphical Display Console System, W. H. NINKE.

The Beam Pen: A Novel High Speed, Input/Output Device for Cathode-Ray-Tube Display Systems, D. R. HARING.

Voice Output from IBM System/360, A. B. URQUHART.

Wednesday, 1:30-3:30
Room 14

Industrial Applications

Chairman:
I. Whiteman
Computer Applications, Inc.
Los Angeles, California

Four papers and a panel discussion make up this session. Kicking off, for the line-up, is Walter Kock of IBM who will discuss a corrugation plant operating system. Applications include a chain of computer functions which begin with order entry, scheduling, inventory management and production control, and end with maintenance of files. All of this takes place on an IBM 1620 with 40K memory, 1311 disc, and 1443 printer.

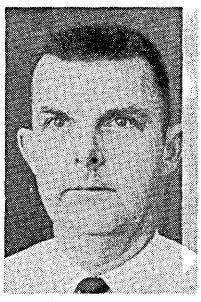
Real-time programming and Athena support at White Sands will be covered by William G. Davidson. The real-time program at the missile range, while not as large as SABRE or SAGE, does employ most of the accepted real-time monitoring and multiprocessing techniques currently in use. Topics discussed include: monitoring philosophy, the actual organization, implementation of the programming system, and problems facing the real-time programmer.

According to Art Daush of Hughes, the role of quality assurance in defining and monitoring edp has not kept pace with other technological developments. He provides a consistent methodology for including quality control in edp. The returns from such an approach are technically and economically rewarding, but they do need a dedicated program, carefully staffed and supported by management, if they are to be successful.

Since it will be many years before man's general decision making powers can be channeled into computers, we must provide him with an optimal remedial problem solving

capability, says S. H. Chasen of Lockheed-Georgia. In discussing "man-computer graphics in the aerospace industry," he shows how with a visual display and the ability to interact with the computer through geometric representations, it is possible to perceive and absorb significant information (such as shape, area, proximity, density, and intersections) to a degree that may obviate the requirements for special purpose, complex and cumbersome computations.

Brown *Whiteman* *Bolles*



As an added bit of frosting, I will moderate a panel discussion on "The Role Of The Computer In Quality Control." The panel consists of Charles Dedo, Aerospace; Karl Frederiksen, Douglas; Walter Kuzmin, Hughes; William Wingstedt, *Quality Assurance* magazine, and Cdr. Robert Smiley, Polaris Missile Facility.

Corrugator Plant Operating System, WALTER J. KOCH and RICHARD H. STRANFORD.

Real-Time Programming and Athena Support at White Sands Missile Range, WILLIAM G. DAVIDSON.

Quality Evaluation of Test Operation Via Electronic Data Processing, A. A. DAUSH.

Introduction of Man-Computer Graphics Into the Aerospace Industry, S. H. CHASEN.

Wednesday, 1:30-3:30
Room 3

Hybrid Computers for Future Systems

Chairman:
E. E. Bolles
The Bunker-Ramo Corporation
Canoga Park, California

The broad field of computation and control systems normally has been divided into two general areas of technology: analog computing, and discrete, or digital, computing. Each of these two approaches has distinct advantages in problem solution or system implementation; but each also has its limitations. Analog systems use continuously variable signals to represent problem parameters and specific elements for each segment or function of the problem. Since all segments of a problem are processed simultaneously, very fast response times are achieved. However, the inherent limitations of precision components confines analog devices to an overall accuracy of about one part in several thousand. Digital devices represent parameters by discrete signals and can therefore have as high a precision as desired. But since most digital equipments solve each segment of a problem sequentially, they therefore have an inherent limit on solution or response time.

Hybrid computer systems capitalize on the best features of both technologies: analog speed and digital precision. Just as there are many variations within either the analog or digital computer field, there are many variations of what constitutes a hybrid computer.

One general class of hybrid systems are those that *combine* a digital and an analog computer via analog-digital and digital-analog conversion equipment. In these

systems each computer preserves its identify but can freely talk and exchange data with the other. A good example of this approach is shown in the paper by Arthur Burns of Grumman Aircraft Engineering Co. This paper describes the use of such a system for design studies of the Lunar Excursion Module (LEM). Here, the dynamics of the vehicle are simulated by the analog computer to achieve real-time response, while the digital computer is used to simulate the precision environmental and orbital factors.

Another form of hybrid system is one in which the computing functions performed are analog, but are *implemented* by digital techniques—such as by digital differential analyzers (DDA). Two papers discuss this approach: Roger Burt of Motorola Inc. describes the design and error analysis of digital integrators for discrete system simulation; M. Goldman of The Martin Co. presents a logical structure and its implementation to achieve a very high-speed DDA.

Probably the most promising of hybrid systems is the *integrated* analog/digital computer. A single computer that uses digital techniques for memory and control, and analog techniques for the arithmetic element is the topic of a paper by H. Schmid of General Electric.

The combined hybrid systems have their greatest promise in simulation and training areas; integrated hybrids show their power in solving real-time problems involving weapons and process control. Although the integrated hybrid will be only about 10% more complex than its digital cousin, it will be 10 times more powerful. Future systems employing hybrid computers, and especially those employing integrated machines, are certain to revolutionize our approach to control and instrumentation.

Hybrid Computation for Lunar Excursion Module Studies, ARTHUR BURNS.

Optimum Design and Error Analysis of Digital Integrators for Discrete System Simulation, ROGER W. BURT and ANDREW P. SAGE.

Sequential Analog-Digital Computer (SADC), HERMAN SCHMID.

Design of a High Speed DDA, M. W. GOLDMAN.

Wednesday, 3:45-5:45
Auditorium

Computer Dimensions in Learning

Gloria Silvern
North American Aviation Inc.
Downey, California

Since the dawn of formal education, only a few of man's inventions have been powerful enough to produce major changes in existing methods of instruction. What was formal instruction like *before* the textbook? . . . *before* the blackboard? These devices not only influenced instructional techniques, but did so in practically *all* subject-matter areas.

With the invention of the computer and its growing acceptance in business, industry and government, together with shorter feedback loops from real-life to the formal learning situation, we are on the threshhold of yet another revolution in education and training. How will the computer liberate and change a curriculum? First, as expected, special and *separate* courses are created in the field of computing technology. These appeal to certain groups of learners, particularly in the sciences, mathematics, engineering and management. However, as computers are more

widely used in the real world, and as new applications are discovered and invented, we begin to see an *integration* of computing *within* an existing course. This integration tends to alter the original course . . . in some instances modifying it so completely that it no longer is the same. In addition, we find *innovation* or the creating of completely new courses or parts of courses which could not have materialized without the computer.

Major Marsland describes the use of computers to increase insight and improve understanding in existing undergraduate university courses in algebra, trigonometry, analytic geometry, calculus and introductory modern analysis.

Professor Staudhammer goes a step further and suggests that the use of the computer in engineering and engineering mathematics courses will eliminate many time-consuming calculations during class. This will lead to reevaluation and restructuring of the conventional engineering curriculum. He contends that a number of standard computing techniques in industry have not yet reached the university campus. Furthermore, many engineering educators are preoccupied with methods for solving specific problems rather than emphasizing mathematical problem formulation and problem evaluation. Staudhammer is proposing that the traditional emphasis in engineering education be shifted from problem solution to problem formulation.

Professor Meyer reinforces the Staudhammer viewpoint when he calls for a major change in the way a course in statistics is conventionally taught. Not only will computing relieve the undergraduate from the tedium of routine calculations, it should give him a facility for looking at larger, more realistic problems. By using a program library tied to a standard textbook, an interacting instructor-student-text-computer library relationship is established.

The infiltration of the computer in learning environments—as a training aid to be used by an instructor for demonstrations and as a learning aid to be used by trainees in a simulated work environment—is the message communicated by Raspanti. He describes training—not education—and was able to synthesize a curriculum to develop and shape new occupational behaviors in preparation for the introduction of a stored-program electronic telephone switching system developed by Bell Telephone Laboratories.

The final paper involves a completely different aspect of learning—in the research domain. Professor Baker develops a three-level model of human memory and proceeds to perform a computer simulation of the model.

Engineering Mathematics Via Computers, JOHN STAUDHAMMER.

Use of Computers in Basic Mathematics Courses, WILLIAM D. MARSLAND, JR.

The Computer: Tutor and Research Assistant, ROBERT J. MEYER.

WOSP: A Word-Organized Stored-Program Training Aid, M. RASPANTI.

CASE: A Program for Simulation of Concept Learning, FRANK B. BAKER.

Wednesday, 3:45-5:45
Gold Room

Memories for Future Computers
A Discuss-Only Session

Chairman:
Donald A. Meier
NCR Electronics Div.

TECHNICAL PROGRAM . . .

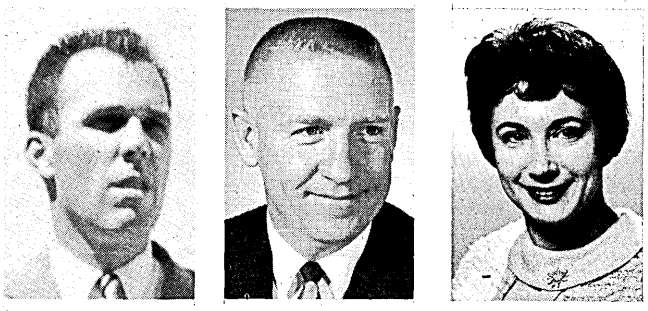
Hawthorne, California

Is there a limit in the requirements for higher speeds and larger capacity in future main memories? Certainly not, at least not in the foreseeable future. Present logical rates are orders of magnitude faster than access times of the fastest main memories, so there is room for much improvement in memory speeds. Future capacity requirements will stagger our imagination and most probably our pocketbooks. Because the combination of speed and capacity required today is not practical in a single main memory, hierarchy techniques such as scratch pads and paging are necessary in the efficient utilization of these systems. However, even with hierarchy techniques, future systems can be made to work better with larger and/or faster main memories, so there is a continuing need for their development.

With present main memory capacity increasing to millions of elements per system, and submicrosecond cycle time systems becoming more common, the rate of main memory developments has by no means stood still. These systems in the past have been dominated for nearly 10 years by a single element being used for nearly all of the total main memory capacity produced during this period. The discrete ferrite toroidal core has been the industry standard during this time, and only recently has it been seriously challenged for this dominating position. Magnetic metal film structures in both planar and cylindrical shapes are appearing or being announced for new main memory systems. This is not to say that advances are not continuing to be made with the ferrite core systems. On the contrary, improvements in ferrite materials, their fabrication and system organization, are being made to such an extent that the main memory race is probably still one sided. The discrete core is still the industry standard to which all other elements must be compared in cost and performance; this also includes systems with cycle times of only a few hundred nanoseconds.

This session will explore some of the newer techniques in main memory developments, as well as the latest developments in discrete core systems. Batch fabrication of memory arrays using either ferrite or metal film materials is becoming very attractive, due to the simple repetitive structure of a memory array. A memory system, of course, is not complete with storage elements alone; the circuits contained within a complete memory system share a good percentage of the total system cost. The impact of batch-fabricated semiconductor circuits is creating as much stir as is new memory element configurations. Not only is the integrated semiconductor technology being felt in the circuit area, but it is also trying to challenge magnetics as a high-speed main memory storage element.

Cellar *Meier* *Silvern*



There will be a total of seven papers in this session. Two papers will describe the latest developments in core tech-

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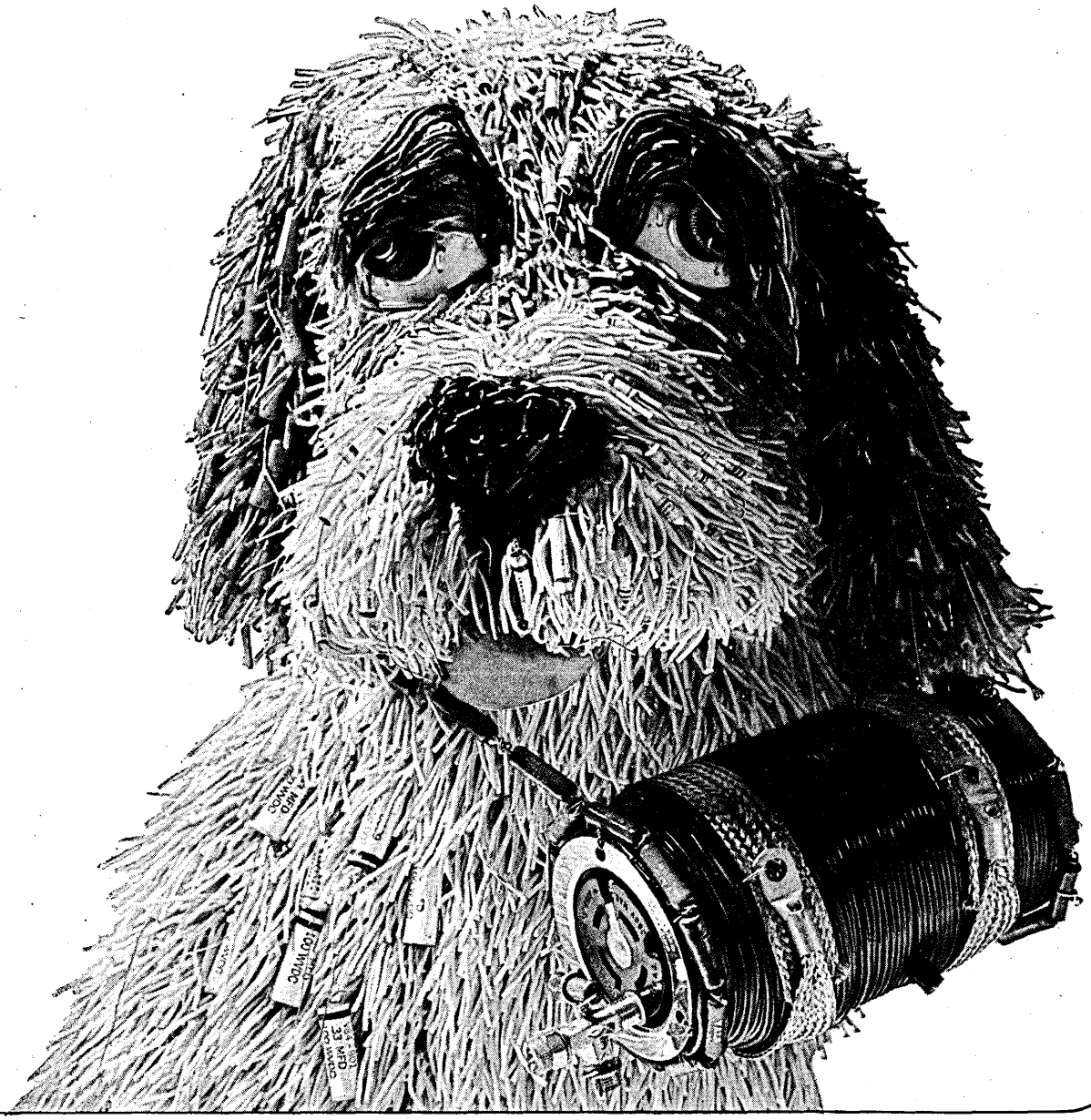

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Can't keep enough things going at the same time.

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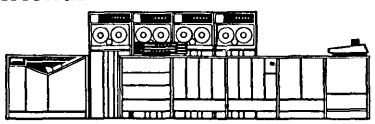


Honeywell

ELECTRONIC DATA PROCESSING

CIRCLE 40 ON READER CARD

nology, and five will explore and describe different facets of batch techniques of fabricating ferrites, metal films and semiconductor storage elements and circuits.

Wednesday, 3:45-5:45
Room 15

Computer-Aided Design & Maintenance

Chairman:
John W. Cellar
Automation Systems
Encino, California

Many companies are now in second and third generation design automation systems. Historically, most have followed similar patterns. The initial use of computers to aid in the design function was aimed for the most part at problem solving. That is, specific design problems were solved with little thought of a system approach to program design. The aerospace and military computer developers spent considerable efforts in implementing logic aids and simulation programs. These were hardware-dependent and unsuitable for later designs. Commercial computer manufacturers spent much of their time in developing wiring, file maintenance, and diagnostic programs. These, too, turned out to be usable only for these specific projects.

Unfortunately, many of the same problems exist today, making proper planning for an integrated design automation system a necessity.

There has been a recent splurge of activity in this application area. This has for the most part been fostered through current technological advancements in hardware and software. Developments of high-resolution automatic drafting machines, increasing uses of visual displays and other graphic input/output media are helping pave the way. Perhaps the greatest boon to automated design of computers is the integrated circuit. It provides the designer with an ability to achieve much greater packing densities with much fewer system connections. However, packing efficiency gains demand more highly skilled printed circuit designers. Design automation is able to move profitably into this picture. The integrated circuit manufacturers, being automation conscious themselves, have brought considerable geometric uniformity and standardization to printed circuit board design. This of course benefits design automation.

A panel will be assembled to discuss the system implications of computer aided design. Representatives from integrated circuit manufacturers, packaging, and programming will give their interpretations of what the future holds for automated design in their areas of specialty.

There will be four papers on computer aided design and maintenance. Two are concerned with the maintenance problem. One will explore fault analysis and describe in detail a system designed to be self-diagnosable. The second describes diagnostics on a large time-sharing computer. Here, diagnostics and marginal tests are run in a time-sharing mode with the normal computer load, thus eliminating the need for a preventive maintenance period. The other two talks are on the design aspect. One discusses a multi-sided circuit board design system, the second automation of various areas in logic design.

Strobes-Shared Time Repair of Big Electronic Systems, J. T. QUATSE.

A Self-Diagnosable Computer, R. E. FORBES, D. H. RUTHERFORD, C. B. STIEGLITZ and L. H. TUNG.

An Automated Interconnect Design System, W. E. PICKRELL.

Systematic Design of Automata, J. P. ROTH.

Wednesday, 3:45-5:45
Room 14

Promising Avenues for Computer Research
A Panel Discussion

Chairman:
Rex Rice
Fairchild Semiconductor
Palo Alto, California

By 1970, fabrication of monolithic circuit elements will approach pennies per element thus providing very low-cost powerful computers. The era of near zero cost hardware circuit elements permits new freedom in the organization and use of computers. The concept of a "personal" stand-alone system as well as shared use of on-line on demand personal computation assistance for all is explored.

In Part I of this session, the panel members will present their views of data processing by 1970. They will postulate a set of software and hardware components to implement their preferred system combinations. This approach will focus attention on present research and the required new research and development. Part II of the session is for active audience participation. Agreement, disagreement and controversial views on these subjects are invited.

Wednesday, 3:45-5:45
Room 3

The Impact of Federal Policy on Computer Usage
A Panel Discussion

Carl W. Clewlow
Arthur Young & Co.
Washington, D.C.

Government expenditure for computer acquisition and operation, both direct and indirect, exceeds two billion dollars annually. It is to be expected, therefore, that various policy decisions inside the federal government have a significant impact on others interested in, or associated with, computer usage.

A panel composed of representatives of a hard goods manufacturer, a major user in government and a governmental policy agency, will discuss the impact of federal policies on computer usage. This discussion will use as its foundation the recently issued Senate document #15, and Report of House and Senate Committees on proposed and/or existing legislation concerning computers.

Wednesday, 8-10 p.m.
Gold Room

The Computer As a Factor in Cultural Evolution
A Panel Discussion

Paul Armer, The RAND Corporation, Co-Chairman
William D. Orr, SF Associates, Co-Chairman

Computer specialists, behavioral scientists and social philosophers seem agreed that the computer ought to be ranked in importance with such pivotal cultural innovations as the alphabet, the wheel, movable type and the internal combustion engine. This session, co-sponsored by FJCC 65 and the AFIPS Committee on Social Implications, will attempt to define a broad conceptual framework for future interdisciplinary research on the topic, some specifics of which appear to be these:

The Influence of Computers on Language. How will the widespread use of computers affect the language we communicate in and think in and solve our problems in?

The Computer and the Civilized Record. How will the "Revolution in Written Communication" (session 11) affect the quality and viability of the civilized record?

The Computer and Learning. What effect will addition of the "Computer Dimension in Learning" (session 28) have on society's ability to cope with its pressing problems—including those raised by the computer itself?

The Computer and Individual Personality. What effect will the computer have on the mental discipline, innovativeness, perceptions and conceptions of individual personalities who are placed in sustained intimate contact with them?

Wednesday, 8-10 p.m.
Room 15

Computer Memories, Fact and Fiction
A Panel Discussion

Chairman:
Robert L. Koppel
Autonetics
Anaheim, California

Optimism has plagued workers active in the memory field. Those influential in shaping future planning for advanced memory development have been perplexed, puzzled and disturbed with the wide gamut of claims made. Of primary concern has been the need for improved performance accompanied by reduced costs.

Improved performance is sought in terms of faster cycle time and increased storage capacity. Military applications require, in addition, lower system power, radiation hardness, and non-destructive readout. Also, new organizations have been suggested among which are content addressable (CAM) and serial (static) memories (BORAM).

Batch fabricated memory structures have been proposed by some as a universal solution but such systems have been slow in "arriving." Others feel that new concepts in device characteristics are called for (e.g. flux gain at the bit level to provide compatible storage, detection, and driving functions in the same memory device).

The purpose of this session is to delve deeply into these controversial topics. Conference attendees are encouraged to come prepared with their own facts and fictions, and attempt to arrive at some meaningful and factual conclusions.

Wednesday, 8-10 p.m.
Room 14

Implications of Information Storage and Retrieval in the Human Brain
A Panel Discussion

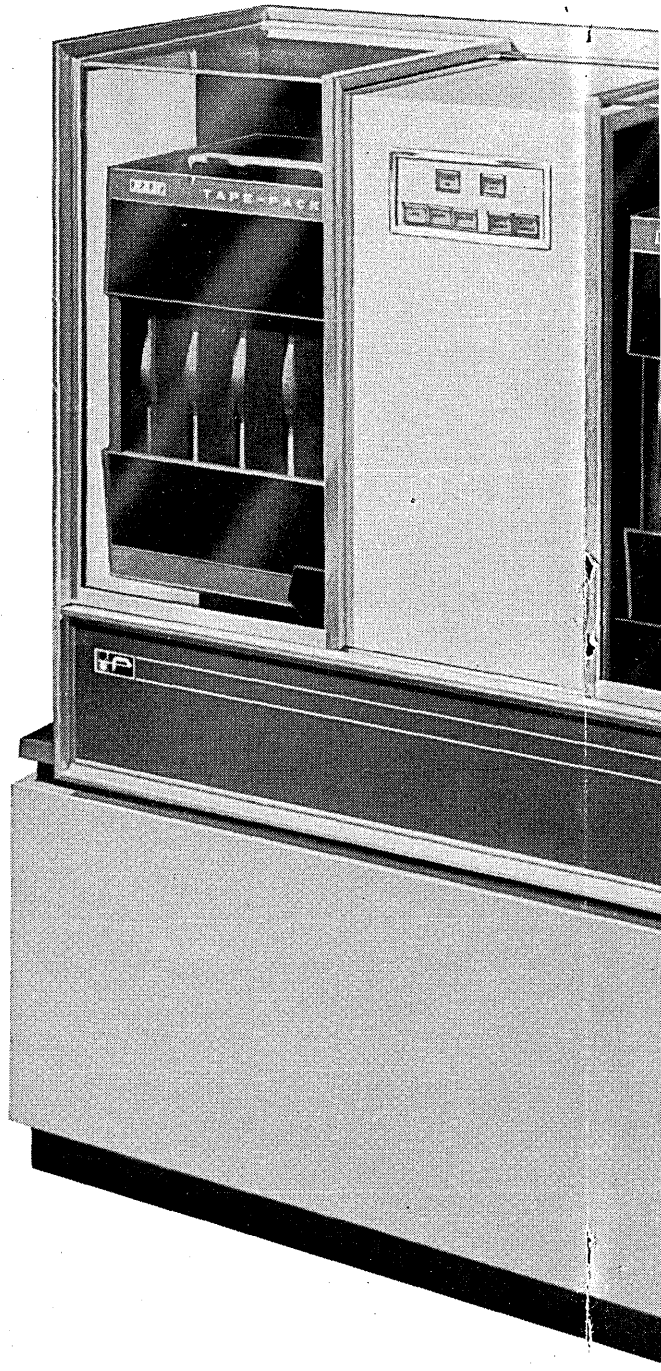
Chairman:
W. S. McCulloch
MIT
Cambridge, Massachusetts

Given devices for storage and retrieval much of what is ordinarily regarded as computation can be done in such a memory. It appears that the art of building such a memory may have to wait for the development of nets having simultaneous access over a sufficient number of channels and for the development of what is commonly called associative memory. The development of such circuits is not thoroughly understood in theory, because we do not know how to create such complexities by simple rules which require changes characteristic of evolution and of learning.

Numerous avenues of research and development are being pursued; however, the organization of such a memory remains the crucial problem. Storage and retrieval in biological mechanisms, such as the human brain, appear to offer promising approaches to mechanize such a memory oriented computation. The session aims at exploring the implications of such an approach. ■

There's a new random access n
it's MAGNETIC TAPE.....

Unless your thoughts on storage mediums are rigid and easily shocked (like old fashioned disc storage systems). . . . you'll want to know these facts about THE WORLD'S FIRST random access memory to successfully use magnetic tape storage—now in commercial operation. The familiar, flexible, reliable medium, MAGNETIC TAPE, has made the breakthrough. Problems of WEAR, COST and RELIABILITY have been solved.



RELIABILITY of the new system is assured because the magnetic tape touches nothing but air during read or write operation. There is no friction between tape and moving parts and no wear or damage to the oxide surface.

SHOCKPROOF characteristics of tape assure no permanent damage will result from shock to the tape itself or to the system. Unlike rigid mediums which are susceptible to permanent distortion from shock, tape resumes its normal shape.

NO TOLERANCE PROBLEM – The new system does not demand precision gap spacing between head and recording surface as does the old disc system. Free-moving, flexible magnetic tape flows past the head on a cushion of air. It maintains precise distance despite shock and other adverse environmental conditions.

POTTER® IN

ss memory storage medium...in use .....in POTTER's *RAM*®

Potter Instrument Company's ***RAM*** uses two cartridges each containing eight magnetic tape loops on which information is recorded serially. Partial or entire data can be transferred between one cartridge and another. Loading and unloading are automatic.

Air cushion tape transport assures full protection against wear and loss of recorded information. If you are interested in a random access memory that outperforms anything else now in use, check these features:

- 30 per cent faster than any old-fashioned system
- Over 50-million bits on-line capacity
- 600 KC transfer rate
- Less than 90 milliseconds average access time
- Rugged, shockproof operation
- Check-read-after-write capability
- Full protection against harmful tape wear

For computer programming and sub-routines, and real time data processing in applications such as geophysical research systems, shipboard and trailer installations . . . and anywhere else that rugged, dependable access to an economically stored volume of information is needed.

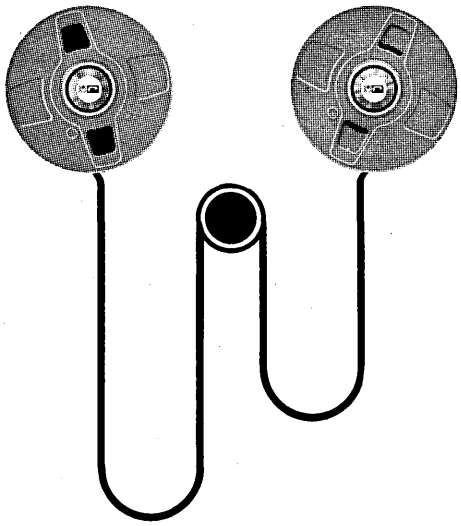
Write, phone or wire for full information. (or see us at booths 537-539 at FJCC)

CIRCLE 43 ON READER CARD

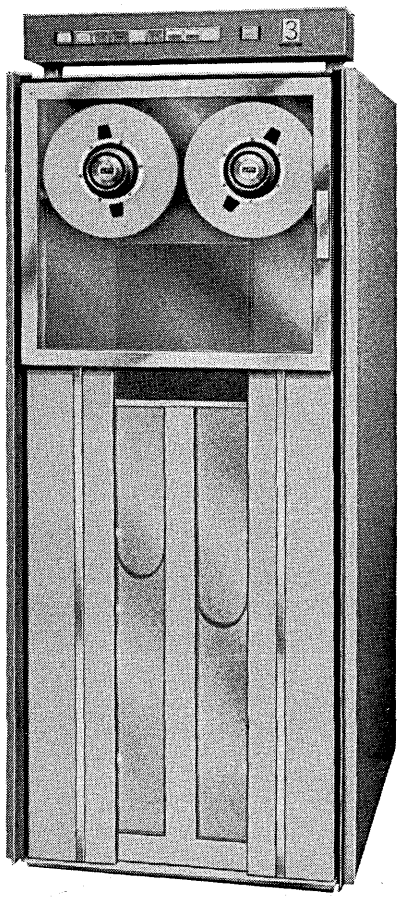
R® INSTRUMENT CO., INC. *151 Sunnyside Blvd. • Plainview, N.Y. 11803 • 516 OV 1-3200 • TWX (516) 433-9320 • Cable-PICO*

How simple can

This simple!



in POTTER®'s new single capstan



POTTER'S ALL-NEW SINGLE CAPSTAN PRINCIPLE greatly increases tape life because nothing touches the oxide surface of the tape except the read/write head. In addition, for the high-speed SC-1150 the head retracts during rewind. Tape path control is maintained by a precision trough guide system with constant vacuum for uniform tape pressure on the reels.

POTTER'S ALL-NEW SINGLE CAPSTAN PRINCIPLE cuts tape handling time drastically because there are no complicated tape threading problems. For example, with the SC-1150 the operator simply clicks the supply reel in place, puts the tape end on the takeup reel and pushes the start button.

POTTER'S ALL-NEW SINGLE CAPSTAN PRINCIPLE means no adjustments—fewer parts. Maintenance time is reduced—reliability is increased.

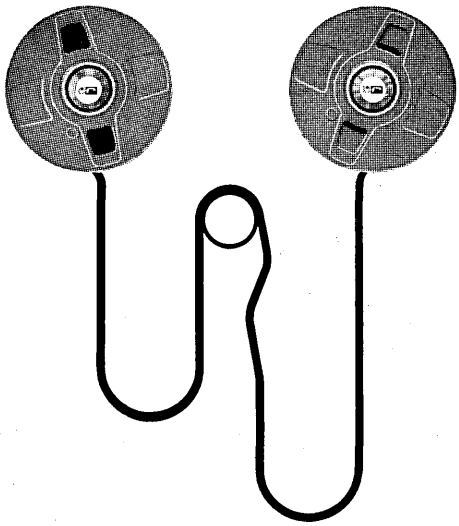
HIGH SPEED SC-1150

POTTER®

PI 105

a tape path be?

or this simple!



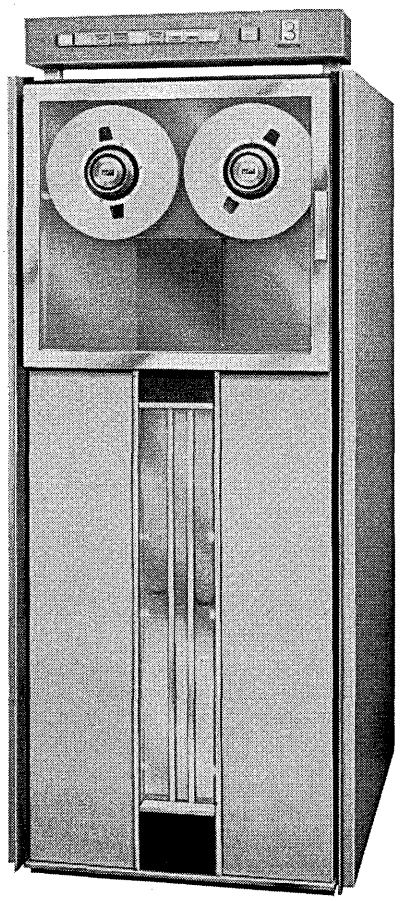
transports...the world's most advanced design

THE SC-1150 AND SC-1060 FEATURES

- Tape speeds to 150 ips (for the high-speed SC-1150)
- Tape speeds to 120 ips (for the medium-speed SC-1060)
- Fully automatic loading
- Compatibility with System 360
  (Including 1600 bpi phase modulated recording)
- Solid state controls
- No program restrictions

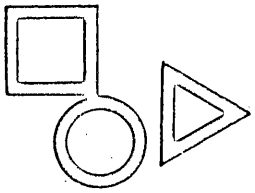
For full details on the SC-1150 and the SC-1060, write call or wire.
(or see us at Booths 537-539 at FJCC)

CIRCLE 44 ON READER CARD



MEDIUM SPEED SC-1060

INSTRUMENT CO., INC. *151 Sunnyside Blvd. • Plainview, N.Y. 11803 • 516 OV 1-3200 • TWX (516) 433-9320 • Cable-PICO*



WORLD REPORT

THE AUSTRALIAN COMPUTER SCENE

The average purchase price of computers in Australia fell during the past fiscal year, ending June 30, to $225K, from $300K the previous year, according to the Dept. of Labour and National Service. The smaller figure is partly attributed to the installation of more small-scale machines. The report shows that the number of digital and analog computers installed and on order rose by more than 40%, from 371 to 527. There were 356 machines installed, compared with 280. Of the 527, 50 cost over $500K, 282 under $200K.

CHEAP TAPE DRIVES DUE FROM BELGIUM

After 18 months in the development doldrums with earlier announced magnetic tape peripherals, Bell Telephone Manufacturing, Amsterdam, (an ITT Belgium subsidiary) has a new set of devices under field test prior to release in early '66. First is a cheap, low-speed unit for seven or nine tracks, 800 bpi, and full IBM compatibility. Standard tape speeds are 28.125 and 56.25 inches/second. Complete with electronics, the price is $10,000 ex-factory Antwerp. A second tape unit will sell at $18,000. IBM compatibility will be provided again on seven and nine tracks. Tape speeds are 75, 90 and 112.5 ips with options for 120 and 150 ips. Tape capacity may be doubled by using 14-inch reels with NARTB hubs.

ALL'S QUIET WITH ANGLO-FRENCH CO-OP

No development seems imminent in the earlier reports of proposed Anglo-French collaboration between ICT and France's CITEC. In spite of this, the digital computer systems division of CITEC, a company called Cie Europeenne d'Automatisme Electronique, is making inroads with machine designs under license from Scientific Data Systems. CAE labels them series 90, models 10, 40 and 80. Recent orders have been from such large research groups as CERN, Contraves and Shell.

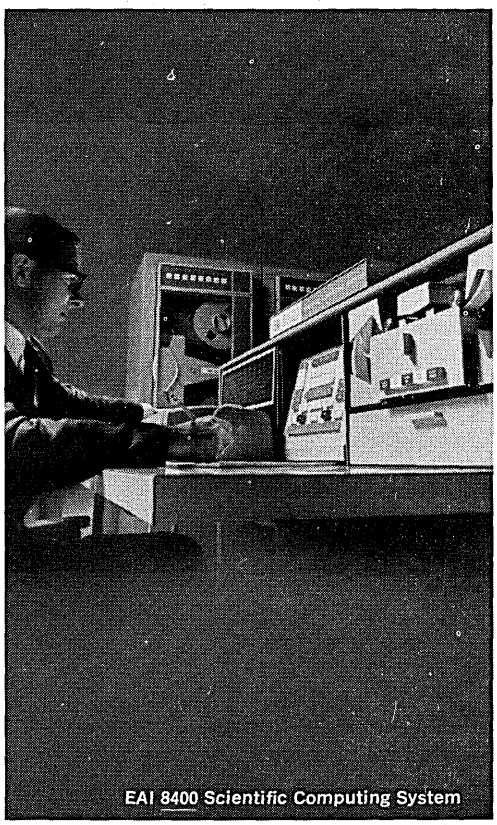
COMPUTER TIME BROKER APPEARS IN LONDON

The service bureau business in the U.K. is in a very whacky state. IBM moved a 1401 out from one bureau in West London that was more than $50,000 in arrears on rental, with every prospect of getting further into the red. Regarded as one of the most specialized and successful operations, International Shipping Information Services has made drastic cuts and reorganized remaining staff. With special packages developed for the ship-broking community, ISIS had been regarded as a sound bet.

CEIR Ltd., on the other hand, is hardly able to contain its expansion. Recent near-acquisition was an established bureau called Independent Computer Services, Edinburgh. With a National-Elliott 803, the Scots service centre is apparently willing to sell. Negotiations have broken down on the price. Expansion into Scotland by CEIR would mean closer location to plants of existing big accounts. Recently CEIR opened an office in Wales that took them into the steel belt where they have big customers.

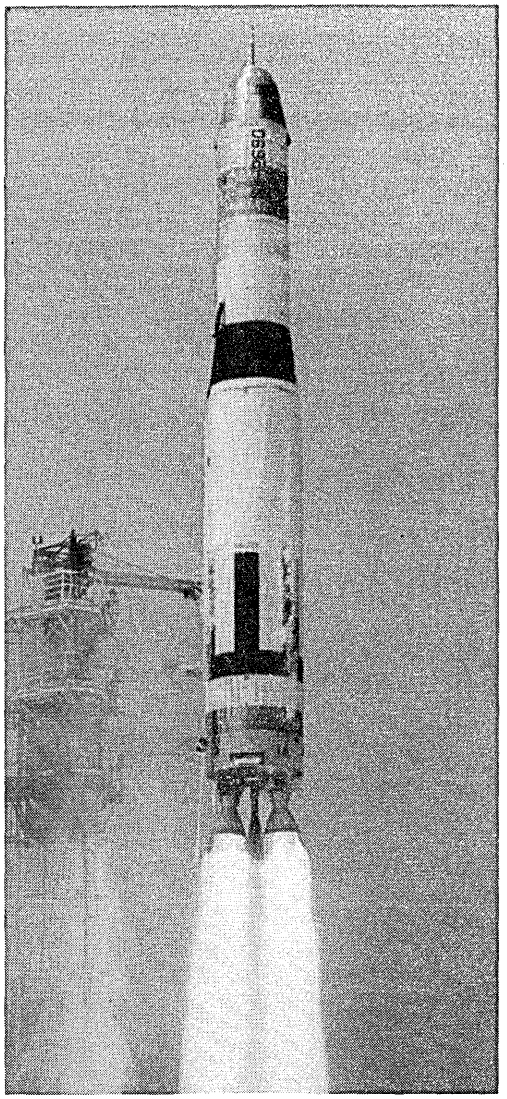
(Continued on page 127)

EAI® software is the difference



EAI 8400 Scientific Computing System

The development of a software system for simulation is among the most challenging tasks presented to the computer industry. Not only must it include conventional scientific software, but it must be capable of performing under on-line, real-time constraints. With a heritage of over 15 years as both a supplier and user of scientific computing systems, EAI has produced the EAI 8400 operating system—the first software system to meet the demands of today's simulation laboratories.



The EAI 8400 operating system delivers a new high level of man/machine communication throughout all phases of program preparation, debug and program execution. Its time-sharing mode offers efficient throughput, by permitting a background of batch-processing to continue during man/machine communication or on-line dead-time.
Error-free recovery from real-time, multi-level interrupts is provided during any phase of system operation—and the entire operating system—from monitor, through language processors, debug, and run time controllers, is operational over the spectrum of EAI 8400 expansion and peripheral configurations starting with the basic system.
EAI is setting the software standard in the field of simulation. How about your field... does a real-time, on-line system with batch processing capability sound interesting? If so, write for details.

EAI®
ELECTRONIC ASSOCIATES, INC., *West Long Branch, New Jersey*

CIRCLE 45 ON READER CARD

Contemporary Electronics is one of the largest producers of computer pulse transformers in the U.S.

SO?

So, maybe you're missing a bet if you haven't checked Contemporary Electronics for *quality, service* and *price.*

Contemporary Electronics *specializes* in pulse transformers. It's not a sideline, but a principal part of our business. Well over 100,000 pulse transformers are produced each month in 75 different designs.

Advantages? Here are some.

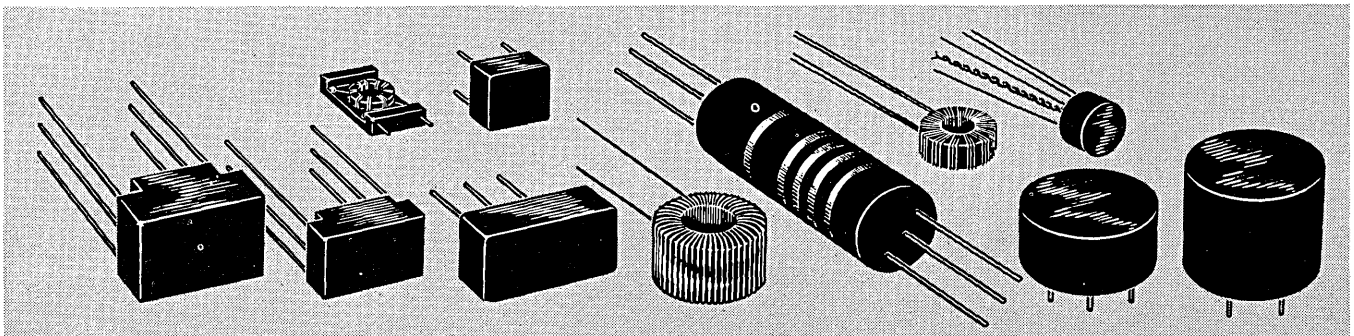
Technical Capability. Contemporary Electronics engineering staff knows computers and can design any special product for any application.

High Quality. Most transformers have special high quality design features. All pulse transformers are 100% inspected as many as three times before shipment. QC system meets MIL-Q-9858, and has been approved for use on the Apollo program.

Fast Sample Service. Samples, small production lots and specials are normally shipped 24 to 72 hours after receipt of request.

Interested in what can be done in terms of performance, size, delivery, or MIL-specs? Get to us—we've got lots more to tell.

WRITE, OR CALL COLLECT AND WE'LL HAVE THE FULL STORY TO YOU WITHIN 48 HOURS



Here are commonly used packages for which tooling is available. Other configurations are always possible.

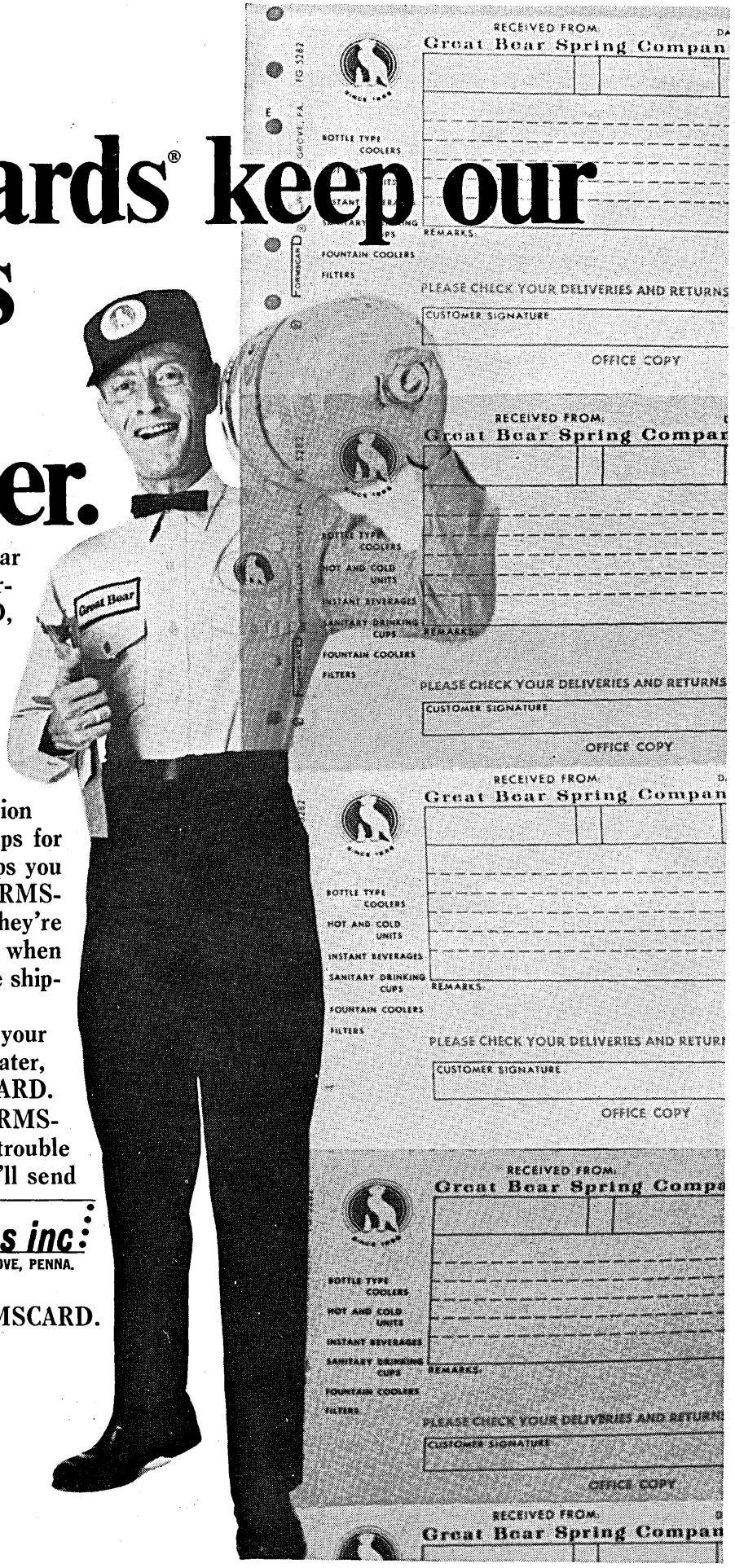
CONTEMPORARY ELECTRONICS

128 North Jackson, Hopkins, Minn. 55343 Telephone 935-8481—Area Code 612

EXTRA SERVICE TO THE DATA PROCESSING INDUSTRY

CIRCLE 46 ON READER CARD

Formscards® keep our business flowing like water.



What's the secret behind Great Bear Spring Company's fast flowing operation? No secret. It's FORMSCARD, the continuous tabulating card system that speeds up delivery and service . . . keeps billing and bookkeeping efficient and orderly.

FORMSCARD means business! And it takes care of business smoothly, without wasting time, motion or money. Take medial waste strips for example, those annoying little strips you find between so many tab cards. FORMSCARD will have no part of them. They're a waste! And they cost you plenty when you've got thousands of cards to be shipped, stored and burst apart.

Take a tip from Great Bear and your business operations will flow like water, with the fast, waste-free FORMSCARD.

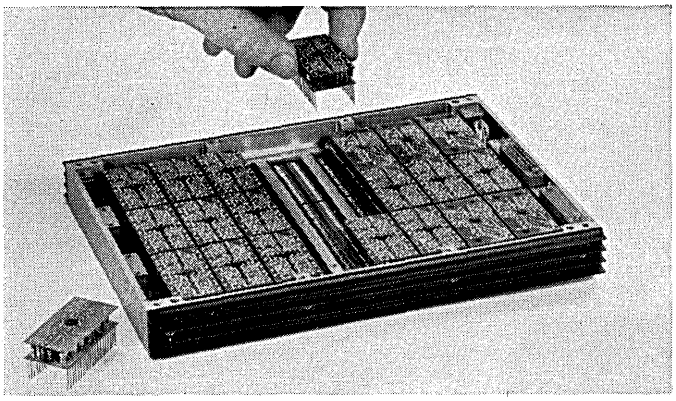
For the full story on how a FORMSCARD system can save you time, trouble and money, drop us a line and we'll send you a copy of our brochure. Or, even better, call us at OLdfield 9-4000 (Area Code 215).

We love to talk about FORMSCARD.

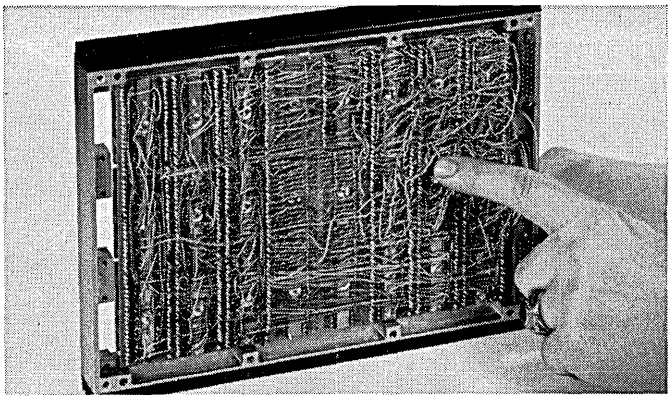
Forms inc
WILLOW GROVE, PENNA.

NATIONAL BUSINESS FORMS ASSOCIATION
FROM COAST TO COAST
MANUFACTURER-MEMBER

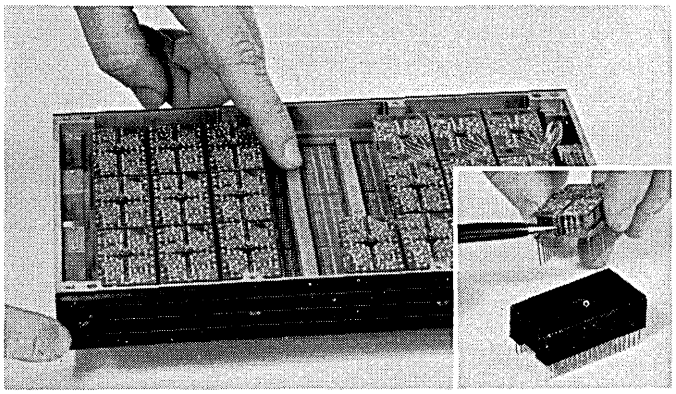
CIRCLE 47 ON READER CARD



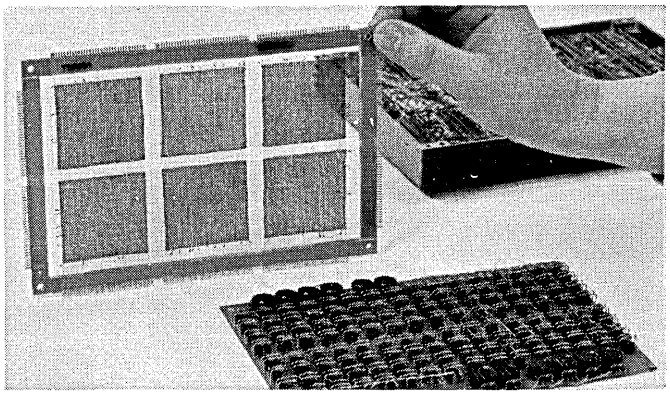
Economical circuit modules, mated directly through a parent-board assembly can be potted with light-closed cell foam if desired.



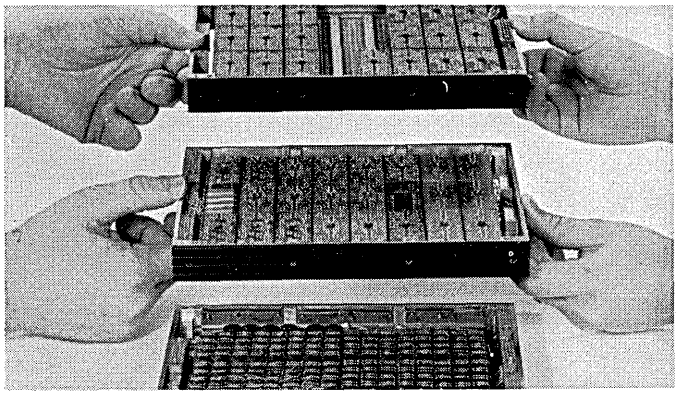
Wrapped wiring of circuit module terminations eliminates connectors, increases reliability, and yet retains easy replacement features.



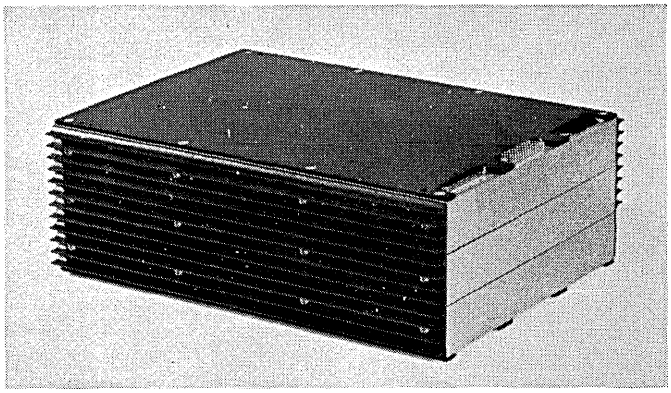
All heat-producing components mount directly to heat sinks. Inset shows how circuit modules each contain individual heat conductors.



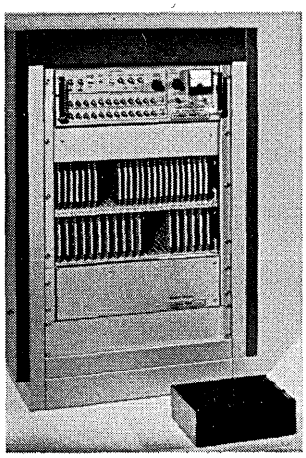
Memory stack consists of 64 x 64 core arrays mounted on rugged, laminated frames. Wide temperature cores are used. Planes can be potted.



System is composed of stacked modules. Number of modules depends upon memory capacity. This typical system has 3 modules and a capacity of 4,096 x 12.



This typical Series MC memory is 7.25″ x 9.375″ and weighs approximately 8 pounds. Max. power dissipation is less than 48 watts. Operating temperature range is —55° to 71°C.



Two Fabri-Tek 4,096 x 12 memories. The larger one is the 1 usec. Series MF. Dwarfed is the 4 usec. Series MC compact memory. Of course, the big one has integral power supply, self-test, and many other features.

A COMPACT, RUGGEDIZED MEMORY FOR SPECIAL-PURPOSE APPLICATIONS

This Fabri-Tek memory incorporates high-reliability packaging techniques intended to extend the MTBF to from 7,000 to 10,000 hours. Typical applications for this memory are: use in industrial atmospheres, geophysical van-mounted systems, special-purpose aircraft, and military applications. Fabri-Tek has used MIL-E-16400 and MIL-E-5400 as development criteria. Ask for information about the Series MC memory system. Write: Fabri-Tek Incorporated, Amery, Wisconsin. Call: 715-268-7155. TWX: 510-376-1710.

FABRI-TEK INCORPORATED

CIRCLE 48 ON READER CARD

NEWS BRIEFS

IBM SWITCHES SIGNALS WITH PURCHASE-OPTION PLAN

IBM has a new purchase option plan, effective Oct. 1, changing the rules for buying rented equipment.

Main point is that the new policy allows a discount only for the first year of leasing—from 40 to 60% of prime shift rental, depending on the specific unit in the system. The plan also eliminates the 1% deposit formerly required and juggles maintenance rates. It doesn't change the price at which a customer may buy rented machines installed before Oct. 1, but that price will not decline any further.

Consensus of reaction so far: it will take a while to see what the effect is. Some users say it's all right with them; they still have a year to try out a new machine, including the software—an attraction with the larger 360's.

Most likely to suffer are the leasing firms. Although the effect will be delayed while there is still plenty of older gear in use, it will be much less profitable in the future for them to move in on a user with equipment leased from IBM, offering to buy it and lease it back at a lower cost.

Much of the industry guessing so far has to do with IBM's motives in making the change. There will be a stronger incentive to buy the new line, but not the old. Selling more 360's quick would bring in lots more cash. But—IBM needs dollars?

The new plan also suggests that IBM would just as soon get all those 1401's back, raising the possibility that a push might be on later with the World Trade Corp. to offer them at competitive prices abroad.

TIME-SHARING DISCUSSION RAISES MANY QUESTIONS; OFFERS FEW ANSWERS

Members of the L.A. chapter of the ACM got a realistic look at time-sharing through the eyes of three advocates of the latest edp fad at their October meeting.

Clark Weissman (SDC), Al Irvine (UCLA), and Jim Babcock (Allen-Babock Computing), took turns answering questions about time-sharing raised by moderator Robert L. Patrick. Among these questions raised by Patrick: What are the classes of jobs which can stand the lowered transfer rate and increased overhead imposed by the necessary directories, primary and secondary storage allocation, and calling of programs and files by name? What is the status of file security? What progress is being made to reduce T-S overhead of scheduling and swapping?

Other toughies: Are there any *facts* about comparative evaluation of time-sharing systems and batch processing? How do we train people to use time-sharing systems well, and how do we measure the results? What is being done to allow reasonable recovery from minor faults? What is being done to cope with the difficult problems of debugging? How will costs be allocated?

The speakers agreed the questions were good—and tough—ones. Plenty of work is being done to answer them, it seems. But few, if any, final answers exist. One panelist reminded the audience that time-sharing is still an infant, experimental technique. From the floor, Guy Dobbs of SDC asked how well the same questions were being answered in traditional, non-time-sharing processing.

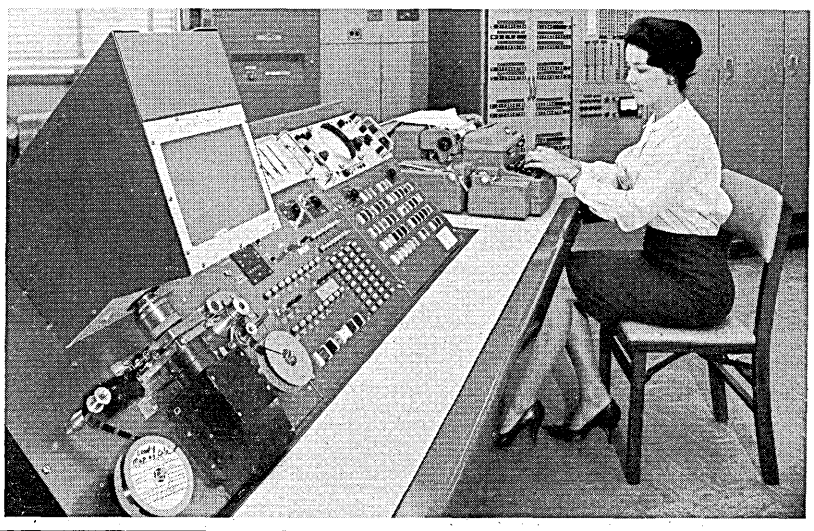
In an extended summary that attempted to compare the status of the

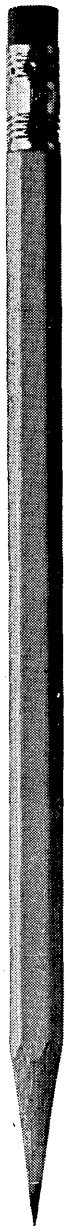
ACCESS SYSTEM ACCEPTS DIRECT MICROFILM INPUT

The National Bureau of Standards Institute of Applied Technology has developed a data gathering and processing system that handles both digital and pictorial data.

Now in use by the Office of Emergency Planning, ACCESS (for Automatic Computer Controlled Electronic Scanning System) will accept input directly from microfilm records and hand-marked documents and digital data from other machines or a keyboard. Specially prepared maps and charts are being read experimentally, the information processed, and graphic results produced by plotter.

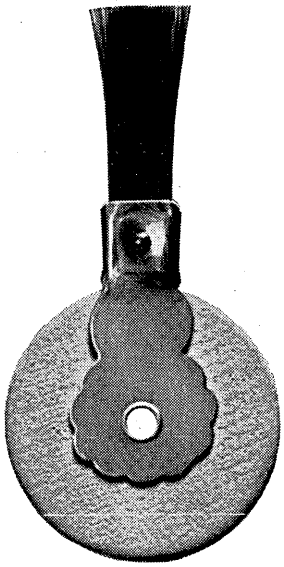
An optical sensing subsystem called FOSDIC is used; it was developed jointly by NBS and the Bureau of the Census. The processor controls the scanner, communications facilities, plotters, and storage units. The scanning unit will selectively read specified areas of a film image. In map reading, a line-following program searches for a point on a line, analyzes eight surrounding points on a fine grid to determine line direction to establish the line for transfer to memory.



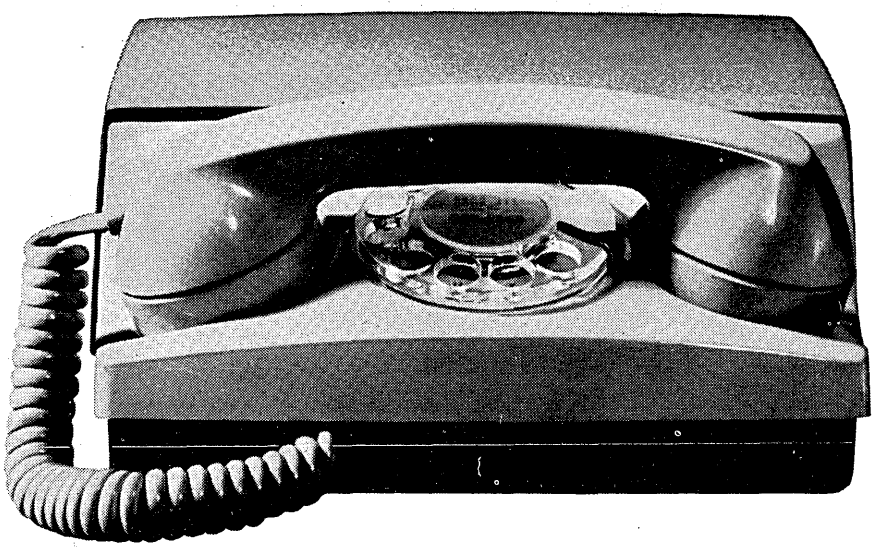


"Guess who saved $75,000 for a customer of Atlas Stationers?"

"Well, who?"



"I did."



"Actually, I shouldn't take all the credit. I'm just part of the Atlas Order-Mation* system, which is saving money for a lot of customers."

When an Atlas customer needs office supplies, it's just a matter of feeding punched cards through a card reader connected to a Bell System Data-Phone** data set.

The order flashes over telephone lines from distant locations to Atlas headquarters in Los Angeles. The cards are automatically duplicated and processed so that Atlas can start filling the order within minutes.

Because of the fast, automatic reordering operations, Atlas customers are able to reduce clerical details, paperwork, and inventories. A chain of department stores saved approximately $75,000. An electrical company saved $28,000. An astronautics firm saves $5000 yearly.

If you're interested in keeping customers buying from you, consider what Data-Phone service could do for your customers and your business. We can show you how.

Just call your Bell Telephone Business Office and ask for the services of our Communications Consultant.

*Trademark of Atlas Stationers **Trademark of the Bell System

Visit the Bell System data exhibit at the Joint Computer Show in Las Vegas, November 30-December 2.

Bell System
American Telephone and Telegraph and Associated Companies

CIRCLE 49 ON READER CARD

two methods, it became apparent that present methods *also* fail to provide adequate solutions to all problems.

PROGRAM FOR POLITICAL REAPPORTIONMENT

A program to help resolve the problems faced by states in reapportioning political districts is now available from C-E-I-R.

It was originally developed for the state of Illinois by Stuart S. Nagel, professor of political science at the Univ. of Illinois, and "has built-in implicit values in favor of the notion that the recent Supreme Court decision on reapportionment should be complied with." Political judgment, compromises, and general horse-trading are not replaced by the program. Instead, it offers a means to juggle several factors and quickly produce the alternative set-ups resulting from the changes.

Eight redistricting conditions can be adjusted, such as number of current districts, number of districts to be formed, and percentage by which a district may deviate from the average district population. The results of weighting these factors include an indication of the influence of any proposed redistricting on the political balance of power.

COMPUTER USAGE COMPANY FORMS TWO SUBSIDIARIES

Computer Usage has set up two new operating subsidiaries, Computer Usage Development Corporation and Computer Usage Education.

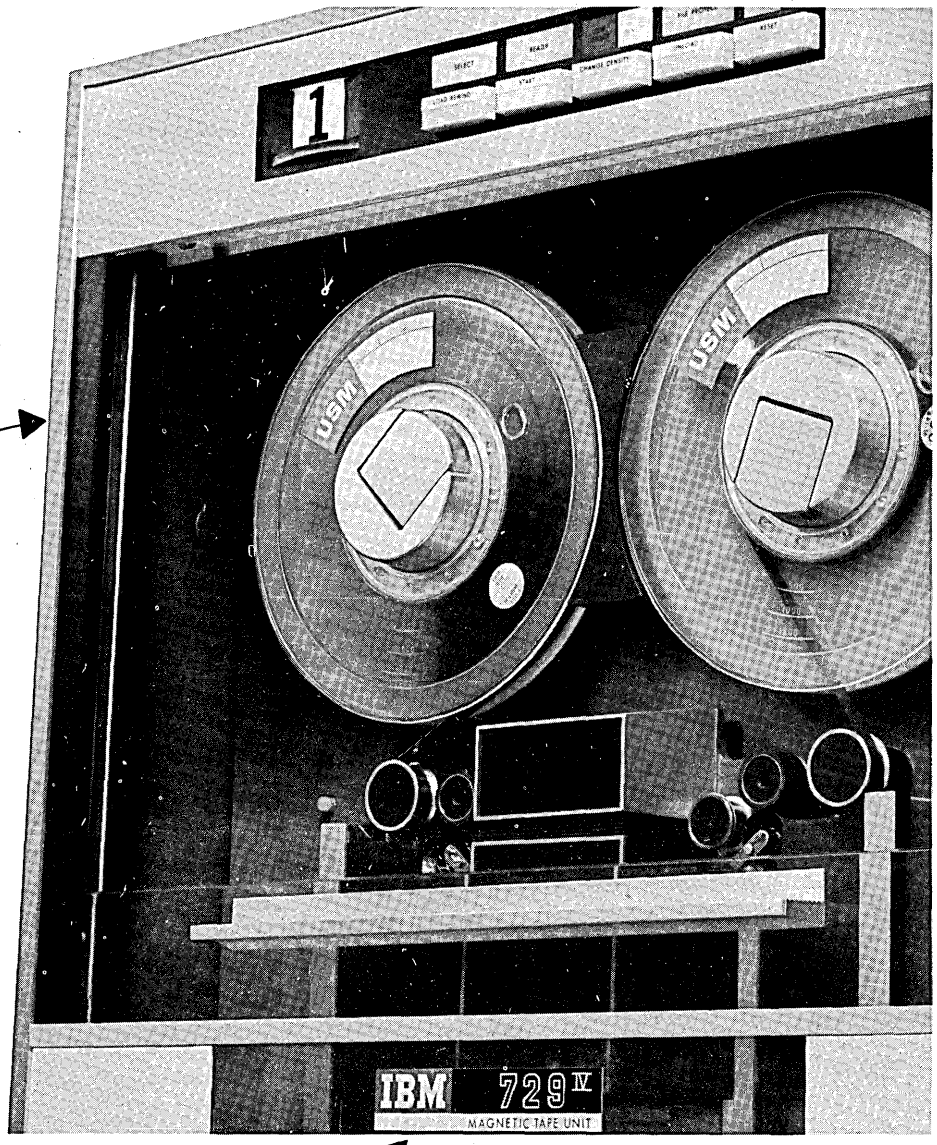
CUDC, to be headed by Walter B. Nelson, will supply analysis and programming services. CUE will offer educational services, including classes and traveling seminars. Ascher Opler will be executive director but will also continue to take part in the design and planning of software projects.

The company has now completed ten years in the computer services field.

NATIONAL BUREAU OF STANDARDS CENTER OPENS

The Commerce Department has announced formation of the Center for Computer Sciences and Technology, National Bureau of Standards, headed by Norman J. Ream, formerly director of systems planning for Lockheed Aircraft.

Main purpose of the center is to aid government agencies in selecting, acquiring, and using computer equipment. In addition, it is charged with



DOES THIS MAKE SENSE ?

INDEED IT DOES! U. S. Tape performs superbly on IBM's 729. It's also the best digital tape you can buy for compatible systems produced by Burroughs, CDC, GE, Honeywell, NCR, RCA, and Univac (solid state). U. S. Tape performance is supported by **the longest, strongest guarantee in the industry.** See for yourself how this outstanding tape lasts longer, assures more profitable computer operation. Write for our test-it-yourself folder.

US TAPE

U. S. MAGNETIC TAPE COMPANY

HUNTLEY, ILLINOIS 60142 / *A Subsidiary of Wabash Magnetics, Inc.*

CIRCLE 52 ON READER CARD

providing advisory and consulting services to the government in developing systems, conducting research in computer sciences and information systems design, guiding an executive branch program for developing standards, and recommending standards for equipment, techniques, and languages.

The NBS center combines the information technology division of the Institute for Applied Technology with the computation section of the Applied Mathematics Division, NBS Institute for Basic Standards.

NIH FACILITIES TO GET TIME-SHARED SYSTEM

A three-stage program leading to a large time-shared IBM system has been announced by the National Institutes of Health for their Bethesda, Md., facilities.

Under a $1.8 million contract, the institutes will work up from a 360 Model 40 in January to a Model 65 in August, eventually to be expanded to a 67. To get started, NIH is establishing a new division of computer research and technology. NIH operations involve nine research institutes, four service divisions, and a 500-bed hospital, all devoted solely to medical research. First of the terminals linking the research institutes to the computer will be installed late next year.

SOUTHERN PACIFIC CHOOSES VIDEOFILE

First commercial firm to place an order for the Ampex Videofile is the Southern Pacific Company, where it will be used for information storage and retrieval covering waybills and related documents.

The system uses videotape techniques for data storage, retrieval stations with CRT displays and facsimile printers plus a switching network and video storage buffers. The Southern Pacific configuration will have a capacity of over 20 million documents and take up 1000 square feet of space, about one-eighth former filing requirements. Updating will average 400K insertions and corrections per month, activity about 56,000 requests monthly.

Six file/retrieve consoles will be used with eight videotape storage units, each packing 36 8½ x 11 documents per foot of tape.

First Videofile ordered will be delivered to NASA's Marshall center early next year; this one is scheduled for early '67.

● A central computer facility for hospitals in the Indianapolis area is being planned by the Indianapolis Hospital Development Association, Inc. Intention is to record all patient activities, from admittance through discharge, in an eight-county area. A six-month study is now under way by Information Sciences Associates to recommend management methods and determine costs. Preliminary estimates indicate three to five years will be required to carry out plans. A $1.5 million grant from Public Health Service has been applied for, citing the usefulness of the proposed system as a demonstration project.

● A general purpose digital computer operable under extreme environmental conditions has been developed by the Westinghouse Defense and Space Center. The DPS-2402 has been designed for such uses as communications switching, weapon control and guidance, navigation, and air-traffic control; the first will be installed on the Royal Canadian Navy's anti-submarine hydrofoil. It is a parallel,

NEWS BRIEFS

binary, single address machine with a capacity per module of 4-32K (24-bit) words, memory overlap capabilities, and a two usec reasonse time. Options on I/O signal levels and control signals make it compatible with all peripheral equipment designed for the Navy Tactical Data System and with most commercial peripherals. Software includes FORTRAN and NELIAC.

● Many students who are granted loans and scholarships to Pennsylvania colleges can give some thanks to an IBM 1460 at the Service Bureau Corp. The state's Higher Education Assistance Agency, in cooperation with SBC, has developed a computer program to evaluate its applications, which are expected to reach 15,000 this year. The system, put into operation last July, determines the applicant's needs based on 190 variables; for example, allowances are made for retirement savings of parents after a certain age. Each run takes seven seconds, compared to 40-50 minutes for an evaluator. The computer's decisions, noted to be "free of politics," are reviewed by the agency; most have been upheld.

● To handle stock record inquiries and stock transfer operations on any of 1.5 million accounts, Chemical Bank New York Trust Co. is developing a 56-terminal on-line system. Five IBM 1050's are now tied into a 1440-1401 system with two 1311 disc files (four megacharacter capacity); the rest of the terminals and another configuration of 1440 and 1401 with disc storage will be phased in by 1967. The 18,000 certificates transferred daily at Chemical will be processed, checked, and typed out by the system, which has a 500 msec response time. A mag tape on daily transactions will be produced and transferred to the history record on the bank's 7074, which also performs demand-deposit accounting, professional and rental billing services, and other functions.

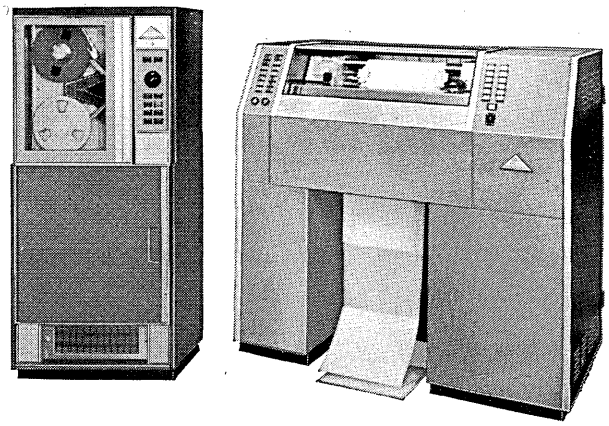
● Link Group of General Precision, Inc. has ordered four DDP-224 computers from Computer Control Co., Inc. for use in Lunar Excursion Module (LEM) Mission Simulators, simulating a manned lunar landing. Each LEM Simulator employs two DDP-224 digital computers to drive equipment simulating the lunar orbit and individual steps anticipated during the approach, landing, and launch from the moon. The $1.8 million contract includes installations at NASA's Manned Spacecraft Center, Houston, and Kennedy Space Center.

● System Development Corporation has a two-year grant of $90,980 from the National Science Foundation to develop a computer-based system designed to improve the teaching of statistics training of research workers. SDC will add $47,487 of its own money to further the project. The system will involve a time-sharing computer, natural-language user/machine communication, and programmed instruction. After initial design, the equipment will be installed at the Univ. of California at Los Angeles for student participation. A feature will be diagnostic routines that will branch the student to remedial material when necessary.

● Munitype, Inc., a New York computer center, is offering a central on-line time-sharing computer for the use of municipal bond underwriters and dealers. The $350,000 system includes a GE-215, 5-megacharacter disc storage, and a Datanet-30 communications processor for automatic relaying of messages. This service will enable the subscribers to call the central computer and obtain immediate answers to complex bid calculations.

● The 1966 presentation of National Electronics Week will be held in San Francisco, May 20-June 5. New regulations restrict exhibit areas to eligible individuals and companies who must buy products from 5% or more of the exhibiting companies for resale without further manufacturing. Service dealers, purchasing agents, and others who do not buy directly from exhibitors will be able to attend only on Sunday, June 5.

● With an initial capital and debt structure that will permit it to acquire up to $40 million worth of computer equipment, a new company, North American Computer Corp., has joined the computer leasing field. NAC boasts highly experienced management, substantial capitalization, and planned specialization in leasing the latest equipment. A major innovation introduced by NAC is the short-term lease under which the computer is rented only for a period tailored to suit the customer's requirements. President and chief executive officer of the company is John M. Randolph; John G. Arbour is executive vice president.



Increases output

A new Anelex Print Station System is the low cost way to greater hard copy output

Anelex Print Station Systems work on-line or off-line with IBM 1400 and 7000 computers. Designed to operate from magnetic tape, these print stations provide fast, reliable, economical printout. You gain new efficiency in computer usage.

Choose from four different print station configurations: a complete off-line system including an Anelex tape transport and high speed printer; an off-line system with high speed printer interfaced to a 729 II, IV, V or VI tape transport; a high speed printer functioning on-line in place of a 729 tape transport; or an on-line or off-line system interfacing the high speed printer either to the computer or an Anelex tape transport.

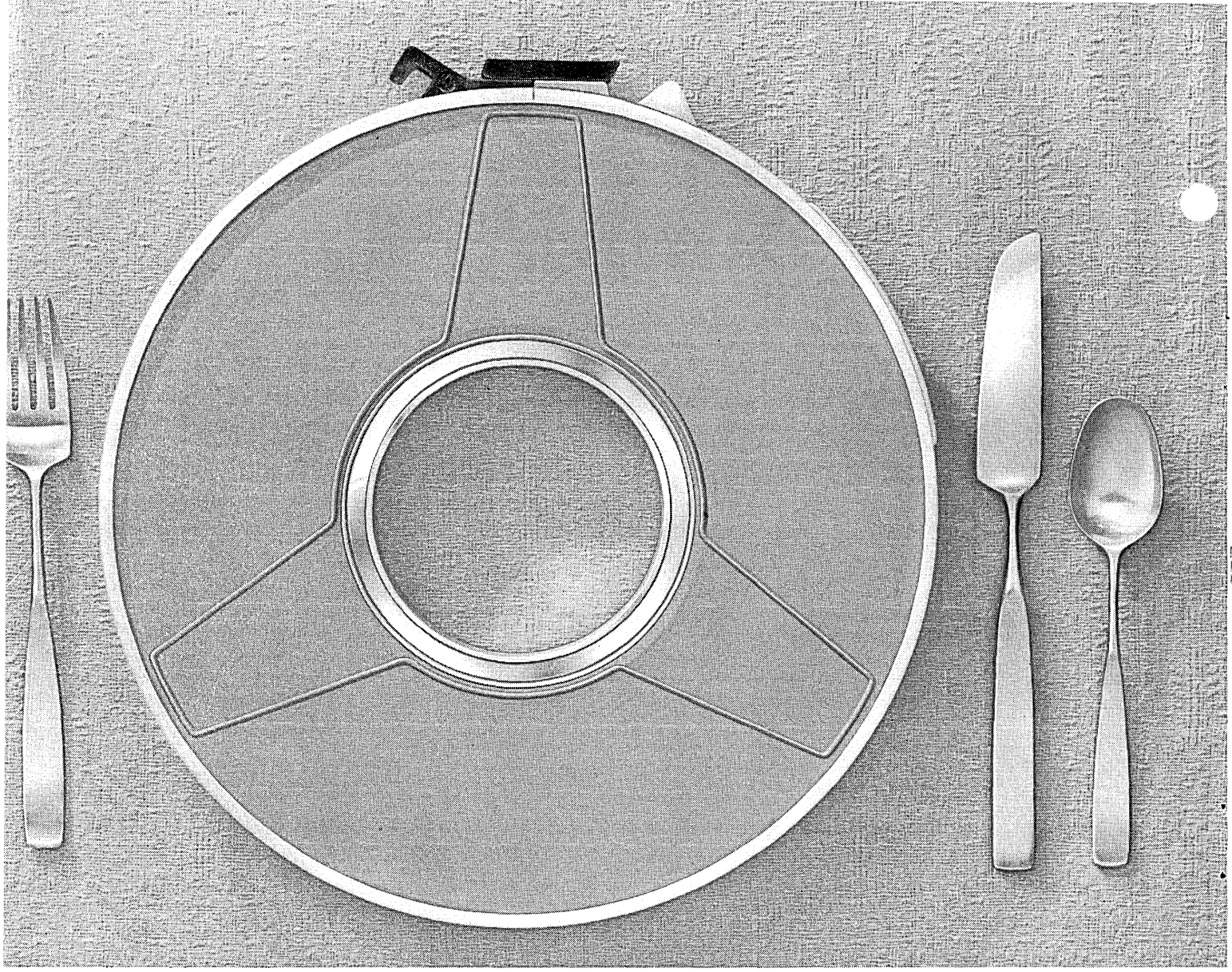
See how an Anelex Print Station can handle your printing overload quickly and at reduced cost. Visit the Anelex Booth, Nos. 434, 433, 509, 510 at the FJCC in Las Vegas — or, get the complete story from Anelex Corporation, Department D-11, 150 Causeway St., Boston, Massachusetts 02114.

ANELEX

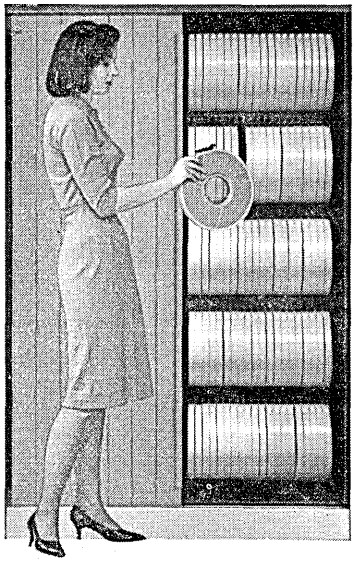
SYMBOL OF QUALITY

ANELEX CORPORATION

CIRCLE 55 ON READER CARD



THE TAPE-SEAL™ SYSTEM TRIMS OVERSTUFFED TAPE STORAGE AREAS BY 50%. HOW'S THAT FOR A CRASH DIET?



Is your tape storage bulging at the seams? Wright Line offers you the new Tape-Seal computer tape storage system* that slashes the fat away. Specifically, this system lets you store 200 tapes in the floor space formerly taken up by 96 tapes. Our patented Tape-Seal Belt helps a lot. It saves space, cost and handling time. Because it hangs from a unique hook-and-latch, no wire supports are required. And retrieval is quick and easy. If you'd like to put your tape storage on a diet, contact us for complete details about Tape-Seal. Our story is so good we think you'll eat it up.

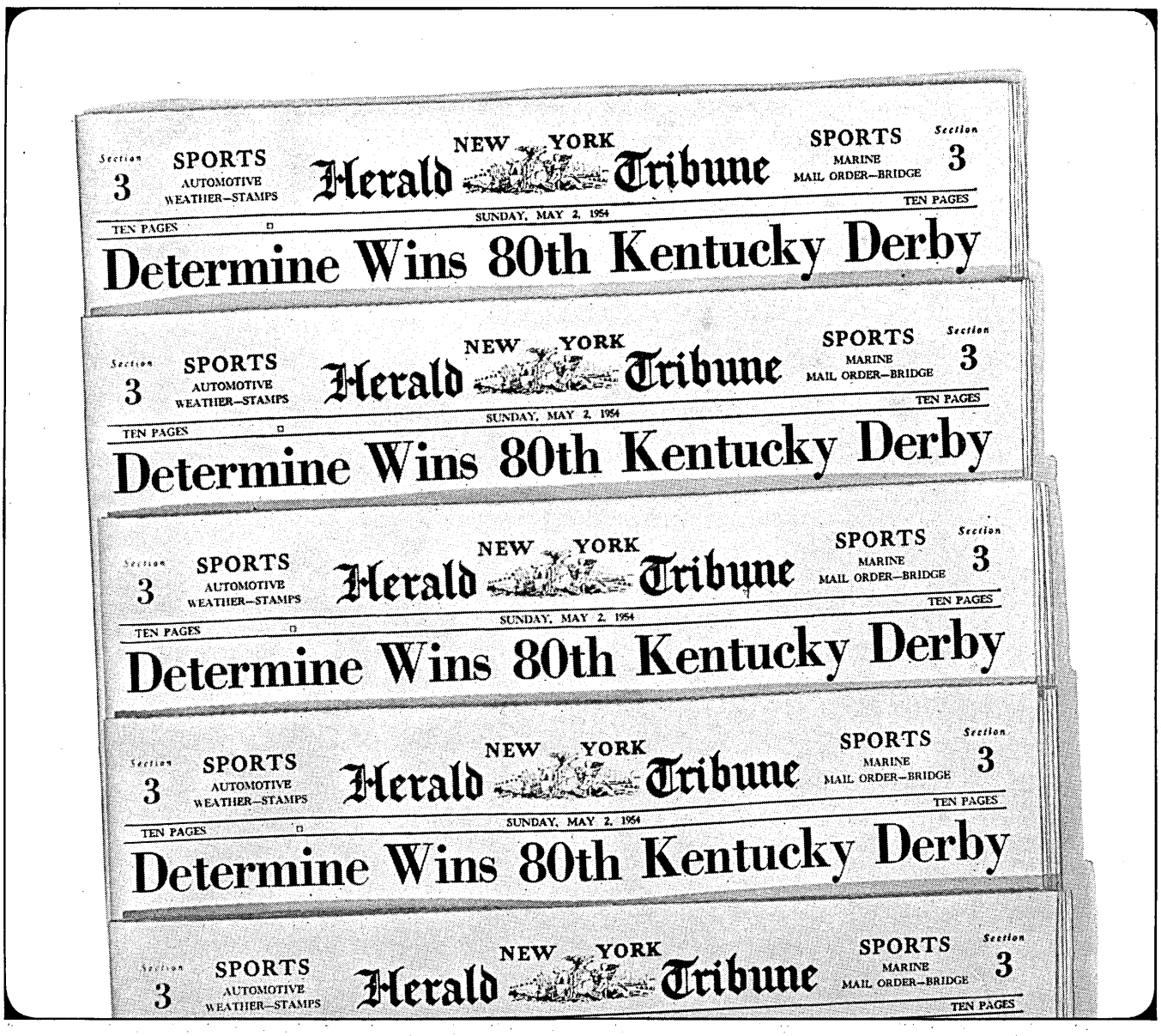
(When you order new tape, insist that they be shipped without canisters. Buy Tape-Seal Belts and save.)

*Patents Pending

Wright LINE DATA PROCESSING ACCESSORIES

170 GOLD STAR BOULEVARD, WORCESTER, MASS. 01606 A division of Barry Wright Corporation BW

CIRCLE 56 ON READER CARD



When this headline was current news... digital recording tapes had a packing rate of 200 bpi.

Today, 800 bpi is standard; improvement in tape and base is the reason.

In analyzing the sensational development of EDP over the past decade, most of us naturally talk in terms of improvement of hardware. But when you stop to examine them, the contributions made by tape manufacturers have been quite remarkable.

The tape of today *looks* like the tape of 1954 . . . but think of the differences: improved oxide coatings to increase total capacity, reduce fluctuations in performance; much stronger binders to reduce dropouts and flaking, lengthen tape life; smoother surfaces to give longer, error-free wear; thinner coatings and better production controls to guarantee reel-to-reel uniformity.

Working hand in hand with the tape manufacturers during this time has been Du Pont. Improvements in the uniformity, stability and overall reliability of the base of MYLAR* have played a vital role in making possible the sophisticated tape in use today. Continuing cooperation of research and development facilites assures continuing improvements in the future. Your guarantee of the most advanced tape is the manufacturer's brand and a base of MYLAR polyester film.

*Du Pont's registered trademark for its polyester film.

DU PONT

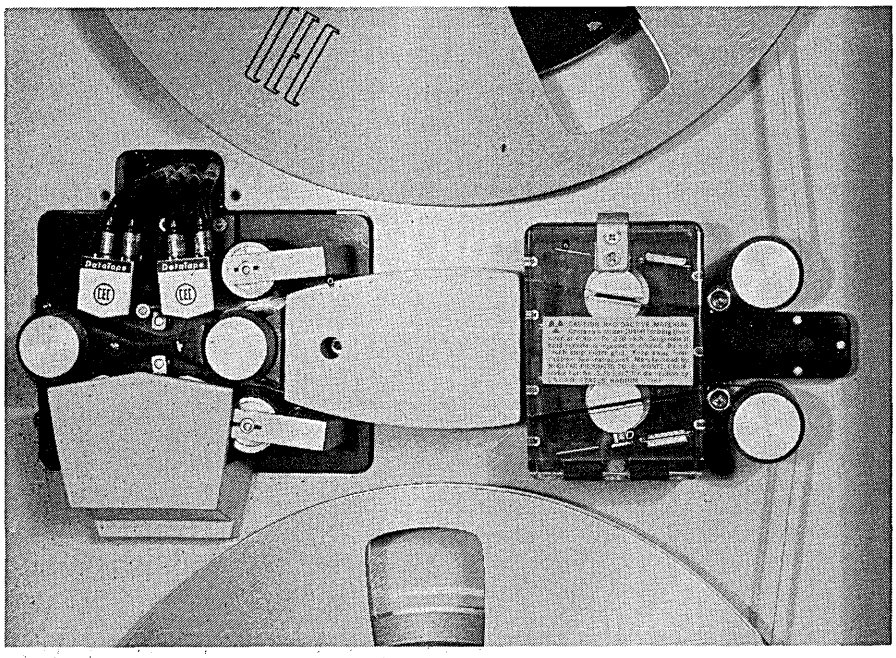
only DU PONT makes MYLAR® POLYESTER FILM

Better Things for Better Living ... *through Chemistry*

At the base of all tape improvements: Mylar®

CIRCLE 57 ON READER CARD

CEC's VR-3600 establishes new record for head life



It is not news that the VR-3600 is the most advanced of all magnetic tape recorder/reproducers. This has been proved in countless telemetry and laboratory applications. But what *is* news, is the remarkable durability of the instrument's recording heads.

All reports have shown that CEC's head life guarantee of 1000 hours is not only realistic but very conservative, since in virtually every case the new recording heads have surpassed this figure with little sign of wear. Compare the 1000 hour achievement with the performance of the VR-3600's closest competitor, and the savings to the user become significant indeed.

Reason behind the performance: these CEC recording heads are of a unique material and solid metal pole-tip design which completely eliminates the weaknesses of conventional head lamination or other solid-tip designs.

Result: a head that both provides superior performance at frequencies to 1.5 mc and reduces head wear and cleaning to a minimum.

Other advantages of the VR-3600 include...

1 **Bandwidth switchability.** With a mere flick of a switch, the operator may instantly change from wideband to narrow band, and back again—thus *doubling* the unit's capability with *no change* of components required. (On special order.)

2 **Constant flux recording** for assured machine-to-machine compatibility at all frequencies and tape speeds (with IRIG standards).

3 **Six speed switchable video FM**—d-c to 500 kc.

4 **Single source responsibility.** All components are designed and manufactured by CEC...including the video FM!

Important features:

◙ Pushbutton selection of *six* transport speeds along with associated electronics.

◙ Each of the VR-3600's 7 or 14 record/reproduce channels can be used for data storage in the 400 cps to 1.5 mc or d-c to 500 kc frequency range.

◙ Automatic end-of-reel sensing stops tape without leaders; transfer switch provides start command for nearby recorder and 30 second overlap of recorded data between machines—at no extra cost.

◙ IRIG or 18.24 kc AM servo system or time expansion/contraction servo system using common assemblies mean low cost for any version or combination of servo systems.

◙ Tape is constantly cleaned by optional vacuum/ionization; tension controlled, in all modes, by closed-loop servo control.

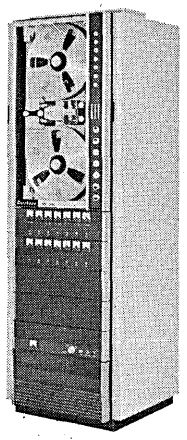
◙ Individual plug-in equalizers (6 per amplifier) meet all specifications simultaneously. Buy only those required, then set and forget.

◙ Record and reproduce amplifiers are solid state; the direct system fully amplitude- and phase-equalized.

◙ Tape transport skew is less than 0.5 μsec; complete cumulative flutter less than 0.30% p-p at 120 ips.

◙ The system may be supplied in single or dual rack configurations, with or without a dolly.

For *all* the facts about the VR-3600, call CEC or write for Bulletin 3600-X22.



CEC

Data Recorders Division

CONSOLIDATED ELECTRODYNAMICS

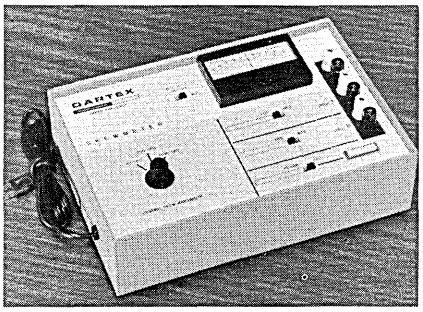
A SUBSIDIARY OF BELL & HOWELL/PASADENA, CALIF. 91109
INTERNATIONAL SUBSIDIARIES: WOKING, SURREY, ENGLAND AND FRIEDBERG (HESSEN), W. GERMANY

CIRCLE 65 ON READER CARD

NEW PRODUCTS

tape skew meter

The SKEWMETER is used to detect skew errors in mag tape transports before the magnitude causes loss of data, and to establish a reference standard to pinpoint responsibility for data losses due to skew error when tapes are interchanged between transports. The latter situation arises, for example, when data collection tapes are transferred to run on faster tape drives.



Requiring no mechanical connection to the transport, the unit uses a master tape to automatically measure skew and give a meter reading of static and low-frequency skew in microinches, independent of tape speed. Ouput connections are provided for a scope display of both static skew and the full frequency range of dynamic skew, if desired. The portable unit can also be mounted for on-line measurement. DARTEX INC., Santa Ana, Calif. For information:

CIRCLE 150 ON READER CARD

small analog computer

The desk-top, portable SD 10/20 is a ±100V machine featuring a removble problem board and ±.01% component accuracy. The removable problem board has visual computer circuits that enable new operators and students to learn programming directly from textbook diagrams. The unit is expandable to 20 amplifiers. SYSTRON-DONNER CORP., Concord, Calif. For information:

CIRCLE 151 ON READER CARD

ruggedized tape drive

The FT-150 FIELD-TAPE operates on 12 volts DC. Designed for digital geophysical field recording, it is also said to be applicable as aircraft recorder, for mobile equipment and shipboard applications. Using IBM-type reels, it operates in 7- and 9-channel formats with densities to 800 bpi. Three speeds range from 15 to 150 ips, and transfer rate is up to 120KC. POTTER INSTRUMENT CO. INC., Plainview, N.Y. For information:

CIRCLE 152 ON READER CARD

optical reader

The 420-2, an upgraded 420-1, reads 52 lines per second, 32 characters/line, for a maximum 1,664 characters/second. It reads NCR's optical font from the firm's cash registers and accounting machines. Internally programmable, it features automatic tape editing, 10-second tape change, selective line output, and four programs for variable output formats. With an automatic back-up feature, an unreadable line is scanned up to seven times before it is rejected. Three provisions are made for unread material: manual keyboard entry by operator, automatic replacement of unreadable character with a special symbol, and automatic printing of unread line on back of the tape. NATIONAL CASH REGISTER CO., Dayton, Ohio. For information:

CIRCLE 153 ON READER CARD

data transmission system

For transmission of punched card data using the 202C Dataphone, this sys-

PRODUCT OF THE MONTH

A display console with its own processor and the ability to project fixed images on a dynamic display is the BR-90. The built-in computer is used to perform all console functions; each control key calls up a subroutine, or group of subroutines, which is executed between refresh cycles of the display. Thus, the display system operation and functions can be changed without modifying the hardware.

The CRT, with an active area of 13.2 x 13.2 inches, has a capacity of 2,816 characters, and can also generate symbols, circles (16 sizes), vectors and points. In addition to an alphanumeric keyboard, a variable function keyboard with 30 keys can provide up to 3,840 discrete key messages for computer program control by the use of removable plastic overlays.

Optional accessories include light gun, cursor control, and film projector. The projection system automatically selects and projects standard 70mm color or black & white slides in 100-slide capacity magazines. Selection can be by operator or computer. The operator may select any of nine overlapping quadrants (¼th of the slide area) for 2X magnification of both background and electronic data. BUNKER-RAMO CORP., Canoga Park, Calif. For information:

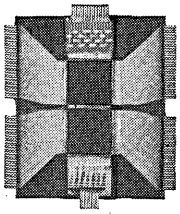
CIRCLE 154 ON READER CARD

A totally new memory technology from RCA

NEW BATCH-FABRICATED HIGH-SPEED MONOLITHIC FERRITES

Each monolithic array contains 4096 "virtual cores" with an effective diameter of only 5 mils within a single, solid, sintered ferrite wafer only 1 in. by 1 in. by 0.005 in.

RCA monolithic ferrites offer all the proved advantages of ferrite technology plus:



□ **Potentially much lower cost** than wired core-memory planes because RCA monolithic ferrites can be mass-produced with standard ceramic processing techniques.

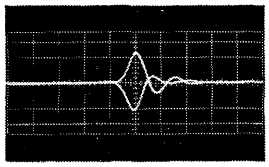
□ **High-density packaging.** Type MF 2100 unit, as shown, is complete with two monolithic memory wafers, and an integral diode matrix assembly. It requires only 3.75" x 4.5" for a memory capacity of 4096 bits in two -"core"- per bit linear-select operation.

□ **Very high speed.** Full cycle time (read, delay, write), as low as 0.2 usec for 64 x 64 array.

□ **Low drive current requirement.** Less than present small-core memories: only 400 ma read, 120 ma write for 45 mv output and 35 nsec switching time.

See RCA Monolithic Ferrites in Operation at FJCC. Booths 202-203

□ **High output voltage.** Equal to conventional cores. Trace indicates over 50 mv each for differential 1 and 0 output. Compare this with other bulk-fabricated systems having output voltages of only 1 or 2 mv.



. . . . . and no stringing

TYPICAL PERFORMANCE IN 64 x 64 ARRAYS								
READ CURRENT			WRITE CURRENT		DIGITS		TYPICAL OUTPUTS	T_s
I ma	T_d (50%) ns	T_r T_f ns	I ma	T_d (50%) ns	I ma	T_d (50%) ns	1 & 0 mv	nsec
400	110	45	100	120	30	200	35	60
400	80	30	120	100	30	200	45	35
400	60	30	150	30	30	100	30	35

Available now in developmental 4096-bit arrays for testing and evaluation. Call your local RCA Sales Office or write today for information to: RCA Electronic Components & Devices, Memory Products Operation, 64 "A" Street, Needham Heights, Mass. (617) HI 4-7200.

CIRCLE 59 ON READER CARD

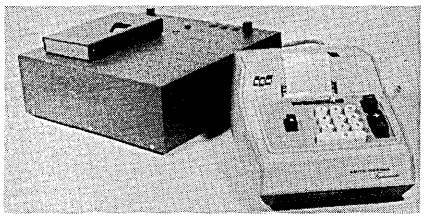
The Most Trusted Name in Electronics

tem consists of a model 2020 transmitter operating at 75 cpm. The model 2120 receiver converts the information to IBM-compatible mag tape, using the 1420 incremental recorder. The receiver may also be used off-line as a card to tape converter with an optional card reader. DIGIDATA CORP., Bladensburg, Md. For information:

CIRCLE 155 ON READER CARD

incremental recorder

The model 351 records 16 data inputs at a packing density of 16 characters to the inch on an endless loop of quarter-inch mag tape—in a cartridge. It incorporates read after write



to insure errorless recording at speeds up to 50 characters per second. In the photo, the unit is linked to an adding machine. ELECTRIC INFORMATION CO., Riverton, Wyoming. For information:

CIRCLE 156 ON READER CARD

disc memories

Five new systems include the 6607 and 6608 large-capacity units for use with the CDC 6000 series computers, and the 852, 853, and 854 removable-pack systems. The first two have respective capacities of 168 and 84 million (6-bit) characters, and 72 and 36 discs. Minimum access time is 34 msec, maximum is 100 msec. The latter three have a 6-disc, 10-recording-surface removable cartridge, and capacities of 9.6, 4.8, and 2.9 million characters, respectively. Maximum access time is 145 msec. CONTROL DATA CORP., Minneapolis, Minn. For information:

CIRCLE 157 ON READER CARD

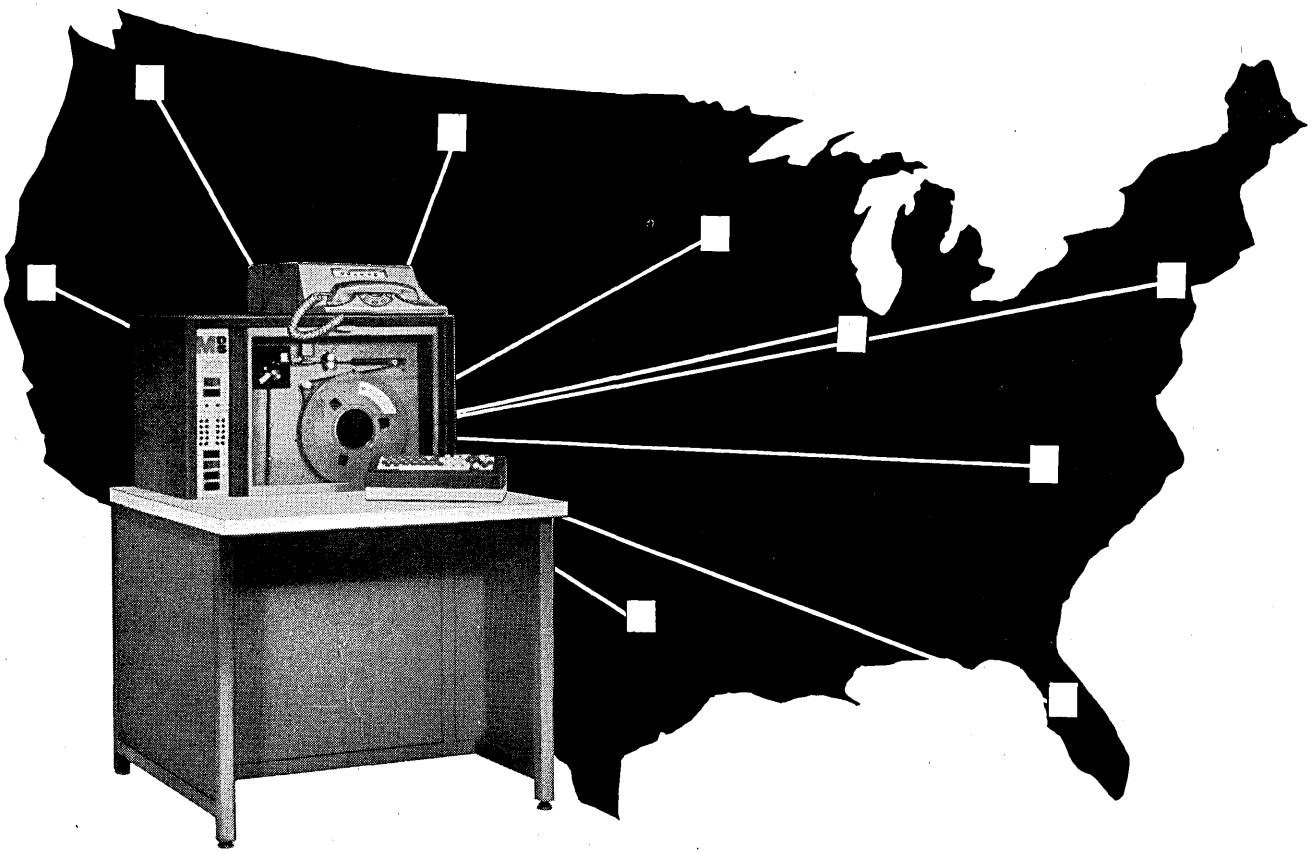
analytical processor

A computer-based system which automatically processes electrical signals generated by groups of analytical instruments, and provides a typewritten report of the data analyzed is PACE (Precision Analytical Computing Equipment). A basic system will automatically service up to five gas chromatographs simultaneously, and is expandable to service up to 40. Expanded system will also service such analytical instruments as mass spectrometers; spectrophotometers, including infrared, ultraviolet and visual; nuclear magnetic resonance spectrometers; and physical testing machines. In a demonstration run, linked to three prerecorded gas chromatograph signals it produced a complete report within one minute without operator intervention. ELECTRONIC ASSOCIATES INC., West Long Branch, N.J. For information:

CIRCLE 158 ON READER CARD

control computer

The GE/PAC 4020 can be rack- or desk-mounted, uses monolithic integrated circuits. Software-compatible with the GE-PAC series, it has 2 to 32K (24-bit) words of core, read/write cycle time of 1.6 usec, add time of 3.2 usec, and average multiply time of 10 usec. It has seven index registers, up to 128 interrupts, and a repertoire of 22 basic instructions. Software includes a process assembler, FORTRAN II (for process work) and IV, plus an executive which allows batch opera-



COMPUTER MAGNETIC TAPE DATA-COMMUNICATION:

You originate, verify, transmit and receive data at $195 rental per terminal

Are you tied to less efficient data transmission media because cost of magnetic tape communications terminals is too high?

Are the slow transmission and high line costs, inherent in non-magnetic tape terminals, restricting your wider use of data communications?

There's a good chance you'll find the solution to these problems in the new MDS 1103 Long Distance Communications DATA-RECORDER.

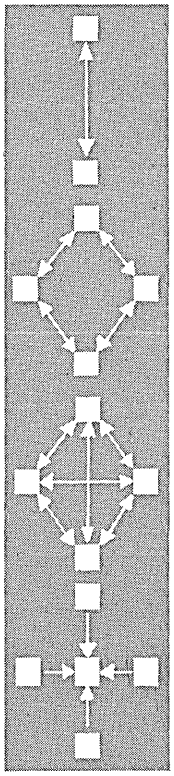
Data processing installations operate most efficiently when both input and output are on magnetic tape. *The 1103 originates, sends and receives... all on magnetic tape... and is designed for use with standard modems and transmission systems. At a cost of $195 per month... we invite your comparison of the 1103 with other magnetic tape terminal equipment on a cost/performance basis.*

The 1103 can record, verify, transmit or receive data as your schedule requires. It obsoletes the single-use terminal.

Recording and verifying can be performed during the day, with transmission at night under low time rates. The high speed of the 1103 minimizes communication facilities charges and other costs.

The 1103 meets the following specifications: (1) Uses standard modems (Bell System 202C or equivalent; (2) Asynchronous operation at speeds up to 1200 bits per second on standard commercial circuits; (3) Uses ½" computer magnetic tape NRZ recording.

You'll be surprised and pleased at the versatility of the 1103... and how much it can do for you at a drastically lower cost. Write or phone us.



1103 LDC

DATA-RECORDER

FOR LONG DISTANCE COMMUNICATION

MDS

MOHAWK DATA SCIENCES CORPORATION • HARTER STREET, HERKIMER, NEW YORK 13350

CIRCLE 61 ON READER CARD

tion during lulls in control functions. It also has a memory protect feature. GENERAL ELECTRIC PROCESS COMPUTER SECTION, Phoenix, Ariz. For information:

CIRCLE 159 ON READER CARD

control computer

The 1700 is an 18-bit machine with a 1.1-usec memory; it is capable of stand-alone scientific computing. It has two index registers, multi-level indirect addressing, and a 16-level (internal and external) interrupt system. Memory capacity is 4 to 32K words, and arithmetic speeds, in usec, are 2.2 for add, 7.0 multiply, and 10.0 for division, all fixed point. Data channels are of two types: interrupt channels with 100KC rate and buffered channels up to 900KC. Software includes executive, industrial control package, and FORTRAN IV. Shipments begin second quarter of '66. CONTROL DATA CORP., Minneapolis, Minn. For information:

CIRCLE 160 ON READER CARD

tape drives

Model 95461 has densities of 200/556 bpi and transfer rates of 15/41.7KC and the 95462 has 200/556/800 bpi densities and transfer rates of 15/41.7/60 KC. Both are IBM (7-track) compatible and feature single-capstan drive, full-length vacuum columns, and air-bearing tape guides. Tape reel loading/unloading is also said to be simplified. Tape speed is 75 ips and start/stop time is 5 msec. SCIENTIFIC DATA SYSTEMS, Santa Monica, Calif. For information:

CIRCLE 161 ON READER CARD

analog computer

Designed for use in such fields as aerospace, process control, and biomedical research, the CP 10/50 is a desk-top analog computer with a 10-volt reference and up to 50 amplifiers. It may be linked with any general-purpose digital computer for hybrid computation, having such features as an auxiliary patch panel for control of individual integrators and a crystal-controlled master and auxiliary timer for high-speed repetitive and interative operations. Amplifiers can be used over a small-signal 350-kc bandwidth; dynamic amplitude error is 0.1% at 10 volts; multiplier accuracy is ±0.1% at full scale. The three-mode electronic mode control is independently controllable from 0.1 msec to 0.99 sec. COMPUTER PRODUCTS, INC., Braintree, Mass. For information:

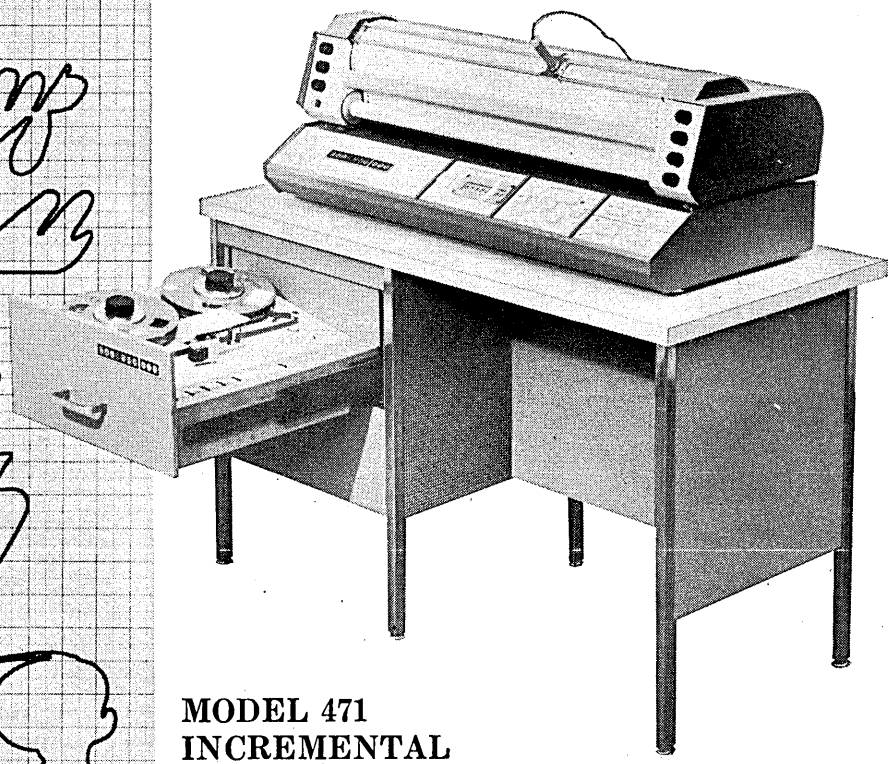
CIRCLE 162 ON READER CARD

NOW PATTERNS CAN BE REPEATED AUTOMATICALLY WITH DIGITAL ACCURACY

CalComp's new Model 471 Incremental Curve Follower permits you to trace any silhouette pattern and record it digitally on magnetic tape.

Process the tracer tape by digital computer and you can reproduce the pattern off-line on any CalComp Magnetic Tape Plotting System.

The same CalComp plotter used to record the pattern on tape can be used to return it to graphic form. Just replace the pen assembly with a Model 471 photocell tracer head to trace and record the pattern, then restore the pen assembly to draw the pattern automatically and accurately—in any quantity and any scale



MODEL 471 INCREMENTAL CURVE FOLLOWER

- Automatic tracing and digital recording of graphic data
- IBM 729 tape format
- Compatible with both character and word oriented computers
- Resolution .01 inch, lineal speed up to 45 inches-per-minute

CALCOMP

Write "Marketing" for additional features and specifications

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CALIFORNIA COMPUTER PRODUCTS, INC.

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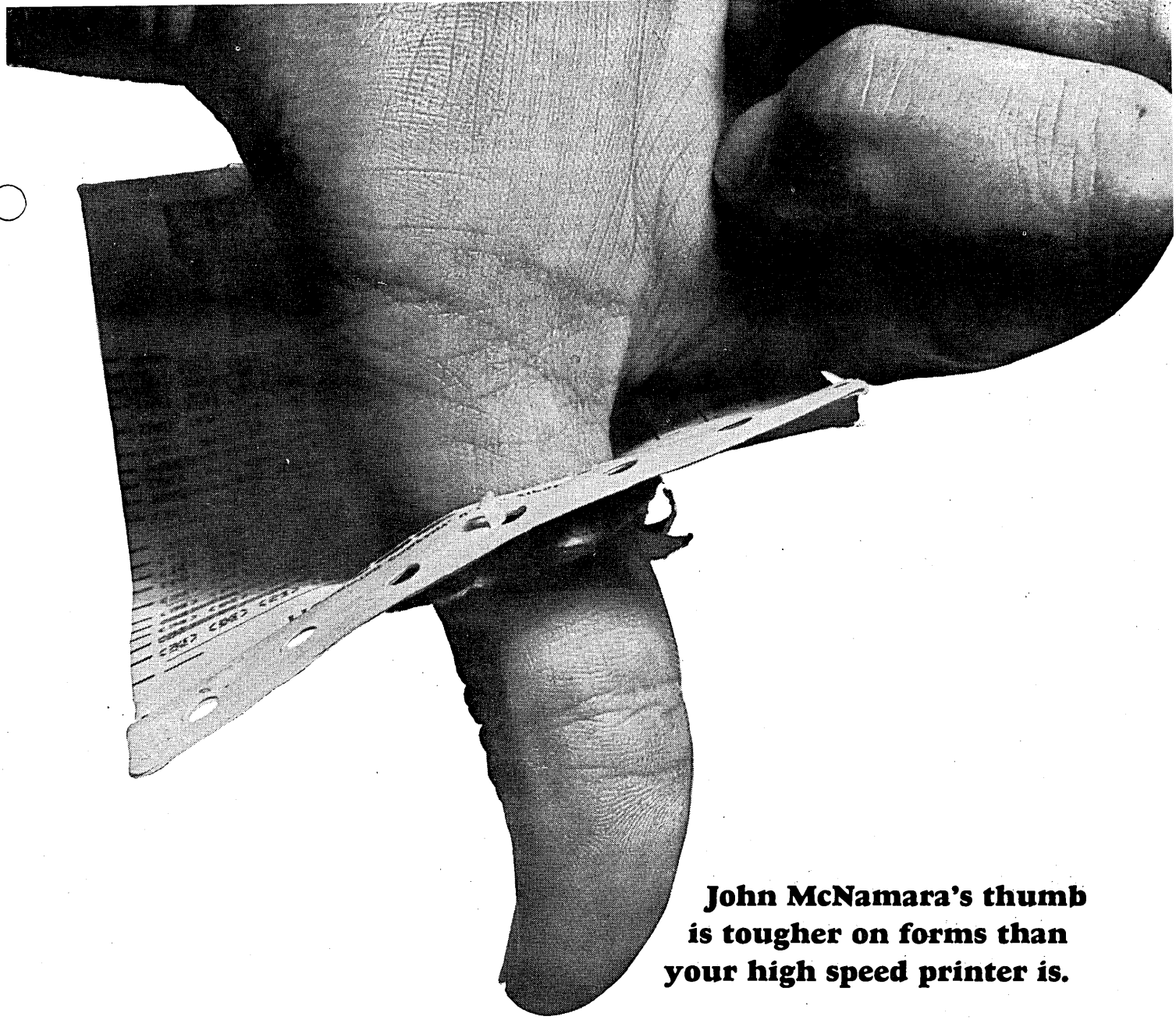


John McNamara's thumb is tougher on forms than your high speed printer is.

Any high speed printer is tough on
forms. But not as tough as John McNamara's thumb.
His job is to make sure our Machine Mated forms are made
right. And if they fail to meet specifications?
It's thumbs down and throw them out.
The specifications are tough and precise. They're
based on getting the most out of your printer.
We work with the people who make the printer. And with you.
So we can develop accurate, exacting standards for a whole
range of forms to meet your needs. Standards for
papers, sizes, plies, carbons, punching,
alignment, copy, feeding, handling, and fastenings.
High standards and a tough taskmaster like John produce a better form.
And that means uninterrupted runs. With no downtime.
Why not see our representative? Or write us at
Standard Register, Dayton, Ohio 45401.
Now you know about McNamara's thumb. And where to
put your finger on Machine Mated forms.

MACHINE MATED™ FORMS BY STANDARD REGISTER

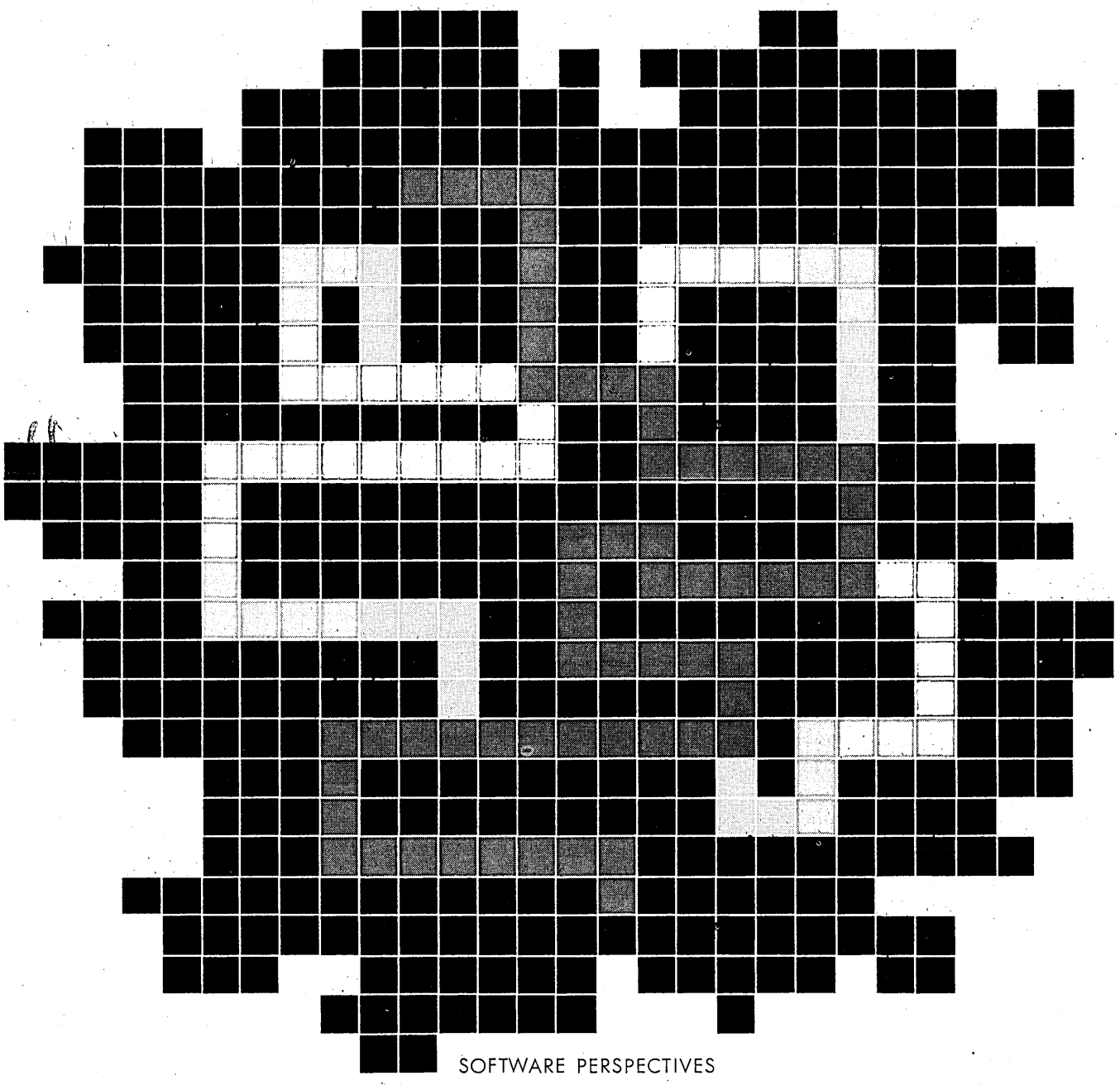
CIRCLE 64 ON READER CARD

HUNG UP BY AUTOMATIC PROGRAMMING?

You say all your senior programmers just joined the Peace Corps? You blew $50K on an automatic programming wizard who flowcharted his way out the side door and got run down by a truck coming to deliver that time-sharing computer you're not ready for anyway? Your OR group got their simulator scrambled up with payroll and EDP sacked all the corporate Veepees and gave the janitor a $25,000 bonus? And now your best prospect just phoned to say you'd better have PL/I working by next Friday even though you're still trying to debug FORTRAN? Sure, it's a rotten streak of luck. But no reason to get your overhead in an uproar as long as there's IDC. Who's IDC? Well, let's put it this way:

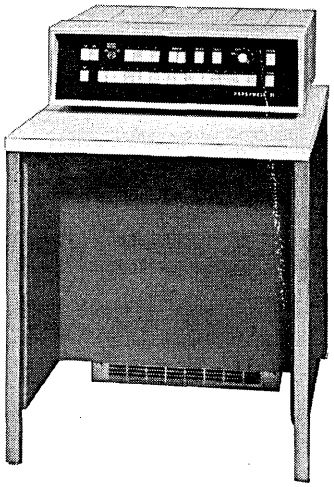
■ IDC is the kind of company that competitors would like to buy, and that the best software specialists are trying to join, and that computer manufacturers and computer users alike are calling on for software results. ■ IDC is the kind of company that if you asked for the man who has developed 20 compilers, they've got him; along with other top professional talent for executive routines, monitors, assemblers, report generators, simulators, hybrid, on-line, realtime, and management information systems. ■ IDC is the kind of company that routinely beats out the giants; like when one company needed a compiler in a hurry, IDC delivered one of the most efficient systems ever written in *less than four months*. That's IDC... fast growing, dynamic, capable, personalized, thoroughly experienced in every phase of systems programming. Sound like a company that could help you? For an improved perspective on your software management problem, contact IDC now. 1621 East 17th Street, Santa Ana, California. Phone: (714) 547-8861

INFORMATION DEVELOPMENT COMPANY



SOFTWARE PERSPECTIVES

CIRCLE 58 ON READER CARD



if you can find a better main frame for the price . . . get it!

We're talking about the H21 – central processor for the new Honeywell 20 Digital Control System. The main frame price, starting at $21,000* is one of many features which make it an attractive component for real-time systems.

Some other features are:

Word Length: 18 bits plus parity and memory guard bits. Single word instructions provide 8192 directly addressable core locations.

Priority Interrupts: Up to 16 hardware levels.

Memory: Magnetic core, random access; 2,048 to 16,384 words capacity; prewired for field expansion; non-volatile on power failure.

Memory Guard: Gives "padlocked" protection against accidental modification of guarded core locations.

Direct Memory Access: Independent path to memory for external I/O operations on a fully buffered, cycle-steal basis.

Silicon Hybrid Circuits with low active component count insure reliable system operation from 32 to 120° F.

Indexing may be combined with indirect addressing.

Three-Address Register Commands allow three-address arithmetic and/or logical operations with single word, one cycle instructions.

Double Length Accumulator facilitates 36-bit arithmetic.

Parallel I/O Channels — designed to provide efficient and convenient interface with user's system equipment.

Typical Operating Speeds (in microseconds, including accessing and indexing): register arithmetic/logical operations, 6.0; load/store, 12.0; multiply, 54.0.

Options: Auxiliary drum memory, magnetic tape unit, high speed paper tape punch and tape reader, priority interrupts, DMA.

Software—An extensive software package includes CONTRAN, the new compiler-level programming system for real-time control; FORTRAN IV with linkage capability to executive programs; and CAP assembly system plus arithmetic, utility, and diagnostic programs.

The H22 central processor with a cycle time of 1.75 microseconds is available at a slightly higher price.

For additional information
call or write A. L. Rogers, Systems Sales Manager
Philadelphia Division, Fort Washington, Pa. 19034
Telephone: 215-643-1300

*Basic price of $21,000 includes H21 central processor with 2K core and input/output typewriter with integral tape punch and reader.

Honeywell

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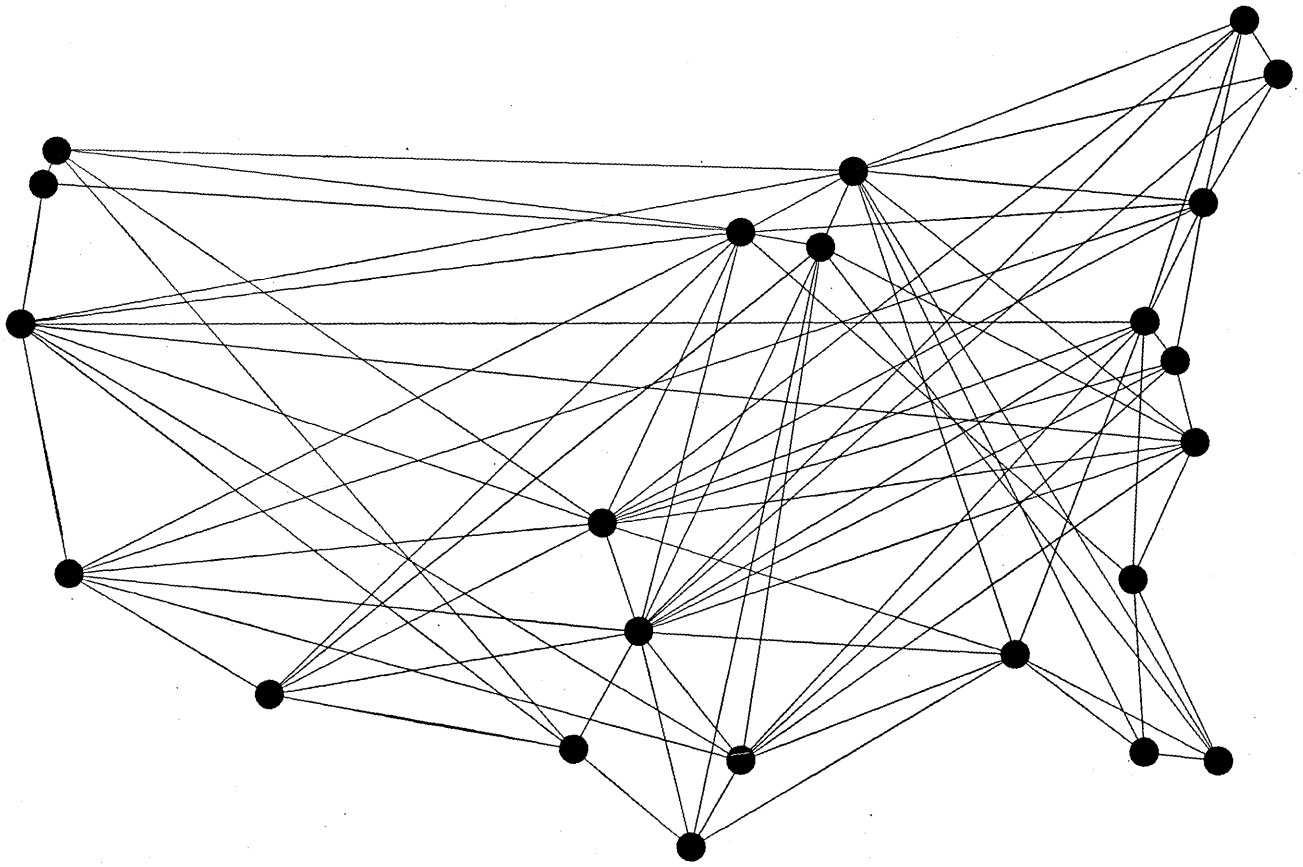

Your decentralized company

Your decentralized company with a Univac
Total Management Information System.

Your total organization is tied together by a total communications system that continuously receives, up-dates and relays management information. Centralized control of decentralized operations becomes a reality. And distance, as a factor in management, becomes irrelevant.

There are three distinct Total Management Information Systems graded for businesses of varying size and complexity and known collectively as The Univac® Modular 490 Real-Time Systems.

For information about them, get in touch with the **Univac Division of Sperry Rand Corporation.**

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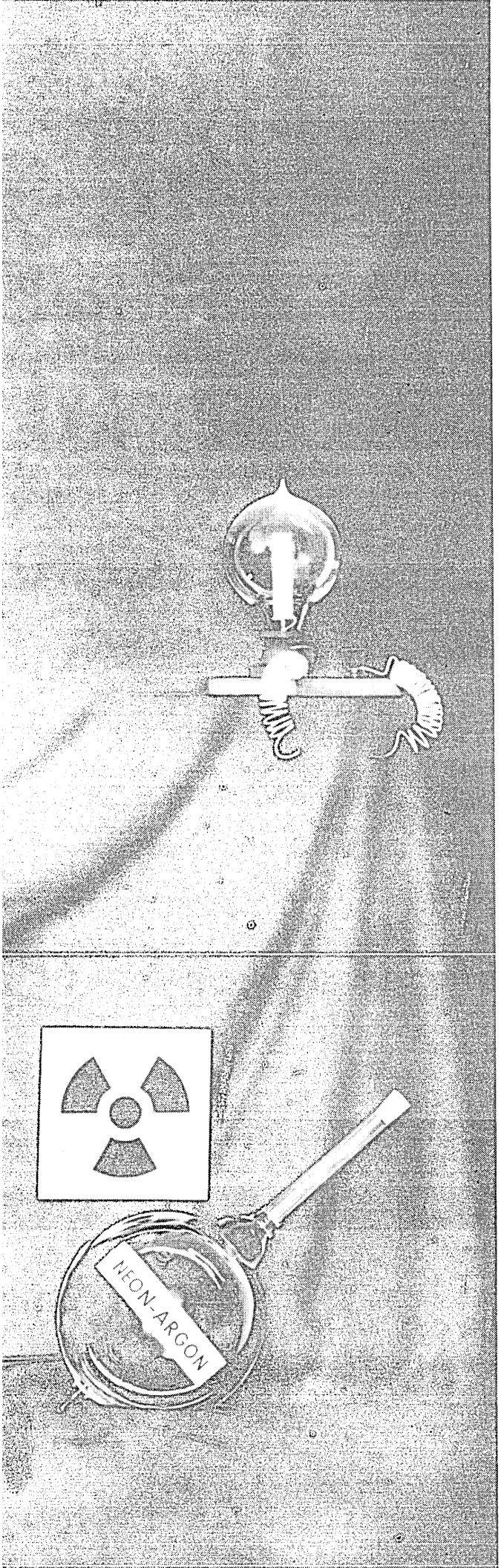


A Noble Approach to an Old Problem

Edison was first.

He converted heat to electricity in a vacuum tube back in '83. But there was a barrier. We're knocking it down.

In a gas-filled thermionic tube, electrons can be boiled off of an emitter and directed to a collector, giving current flow. But only briefly. Then a cloud of electrons forms in the path . . . a space charge inhibiting further flow.

One way to get rid of this barrier is to neutralize it with positive ions, charged atoms of some gas. Many experimenters use vaporized cesium. But its atoms impede electron flow, requiring close interelectrode spacing. So GM Research physicists chose some of the noble gases argon, neon, and xenon. They offer less impedance.

Our experimental emitter is a mixture of fissionable material and good electron-emitting material. Exposed to a neutron barrage in a reactor, the emitter gets hot from its own nuclear fission, sending electrons toward the collector. This same fission produces fragments that bombard the noble gas, generating ions to counteract the space charge.

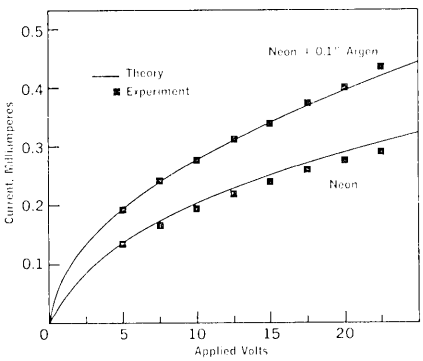
We have developed a theory to predict the ion generation rate and have experimental data that backs it up. We think we understand why and how things happen.

General Motors is in the energy conversion business. The direct conversion of heat to electricity, with a device having no moving parts, interests us.

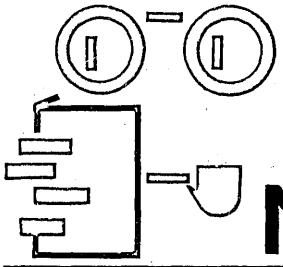
CIRCLE 68 ON READER CARD

General Motors Research Laboratories

Warren, Michigan



Characteristics of tubes filled with gases ionized by fission fragments. Resulting current is a function of ion generation rate, which is increased greatly (from 1.8 to 2.6 x 10^{16} ions per cm^3 per sec) by small addition of argon.



NEW LITERATURE

DIGITAL LOGIC SYSTEM: Eight-page bulletin details features of DES-30 which can be linked to the TR-48, other small analog computers and general purpose analog or digital computers. System can be used in advanced problem solving, including simulation of discrete systems, statistical calculations, Fourier analysis, transport delay simulation and incremental and iterative computations. ELECTRONIC ASSOCIATES INC., West Long Branch, N.J. For copy:
CIRCLE 165 ON READER CARD

EVALUATING THE EFFECTIVENESS OF IR SYSTEMS: 86-page book suggests using model based on Bayesian statistical theory. This model relates effectiveness of a retrieval system to the statistical characteristics of the retrieval process and the value structure of the requestor. Order no. AD 618 311N, CLEARINGHOUSE, U. S. DEPARTMENT OF COMMERCE, Springfield, Va.

INTRODUCTION TO SHARE ALGOL 60 TRANSLATOR: 166-page book describes system as well as each phase of translator which operates under FORTRAN II version II monitor system on the IBM 709/7090/7094. It consists of a supervisor and six phases, each of which performs a specific function in the translation process. Order no. K-1614N. Price: $5. CLEARINGHOUSE FOR FEDERAL SCIENTIFIC AND TECHNICAL INFORMATION, U.S. DEPARTMENT OF COMMERCE, Springfield, Va.

TIME-SHARING COMPUTER: 16-page brochure describes system 940 which can give up to 32 users simultaneous access to the central processor. Definition and characteristics of time-sharing, computer utilization, hardware features, specifications and a working example are given. SCIENTIFIC DATA SYSTEMS, Santa Monica, Calif. For copy:
CIRCLE 166 ON READER CARD

FORMS HANDLING EQUIPMENT: Six-page bulletin discusses forms problems, input and collection, mobility and storage of forms. SYSTEMS SALES CO., Binghamton, N.Y. For copy:
CIRCLE 167 ON READER CARD

MULTI-WEB DECOLLATOR: Four-page brochure illustrates features of Model 284, which removes one or both margins and all carbons from continuous forms in one operation. Specifications, add-on units, forms sizes and electrical and mechanical details of the

We don't claim that Royal Paper Tape equipment is more reliable.

Our customers do.

And you can get their names from our representative.

What we do is tailor 50 CPS and 75 CPS punches and readers to their specifications and help integrate them into their system (rack mounted, desk mounted or custom-designed units). Give a meaningful warranty we stand behind. Guarantee fast service. And provide these new design features for greater efficiency and reliability:

☐ Efficient electromagnets and off-center springs insure smooth, trouble-free punching.

☐ Reluctance type pickup for timing eliminates contacts and cams, reduces systems noise.

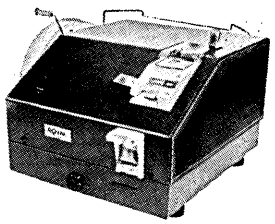
☐ Bi-directional reader operates with high reliability at low noise level through action of sensing pins on wire contacts and strobe-like interrogate pin.

☐ Sealed read station protects mechanism . . . saves maintenance.

☐ Semiautomatic feed allows fast tape loading (operator merely places tape in head assembly throat).

All at no extra cost. Evaluate them for yourself before you go a step further on *any* system requiring a punch or reader mechanism. There is a Royal Series 500 (50 CPS) and a Royal Series 700 (75 CPS) unit for every punched tape requirement. Including, most specifically, *yours*. Write for specifications. Industrial Products, Royal Typewriter Company, A Division of Litton Industries, Dept. 33JV, 150 New Park Avenue, Hartford, Conn.

Series 500 and 700 Integrated Punch Stations can operate as a complete tape punching facility when cable connected to appropriate signal generating equipment. This configuration includes a standard 8" tape supply reel in a drawer mounted at the base of the unit. The tape feeds through the punching head and a tape guide (located at the rear) to a side mounted take up reel. Take up reels in either 7½" or 8½" diameters are available. The oversize chad container can accommodate chad from approximately 1000 feet of punched tape. Overall dimensions are 13½" wide x 15" deep x 9½" high. Weight is approximately 23½ lbs.



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machine are included. MOORE BUSINESS FORMS INC., Niagara Falls, N. Y. For copy:

CIRCLE 168 ON READER CARD

DESK TOP CALCULATOR: Booklet offers description and specifications for the Friden 130 which measures 13x21x 10-inches, weighs 44 pounds, and can be used to solve business and scientific problems. FRIDEN INC., Los Angeles, Calif. For copy:

CIRCLE 169 ON READER CARD

DISPLAY SYSTEMS: Brochure covers variety of advanced-design display systems and related devices, including types of crt display consoles. PHILCO CORP., Willow Grove, Pa. For copy:

CIRCLE 170 ON READER CARD

HIGH SPEED IMPRINTER: Bulletin outlines use of the MICAR II for E-13B encoding of continuous form checks at speeds up to 40,000 impressions/hour. Includes details of stop-and-go paper travel, image transfer, and variable positioning of numbers. HELLER ROBERTS INSTRUMENTS CORP., Brooklyn, N.Y. For copy:

CIRCLE 171 ON READER CARD

MILITRAN SIMULATION LANGUAGE: 16-page brochure summarizes technical features of MILITRAN. Sample problem and complete list of statement forms included. SYSTEMS RESEARCH GROUP, INC., Mineola, N.Y. For copy:

CIRCLE 172 ON READER CARD

MULTIANALYZER: Four-page brochure describes control and analysis systems for mass spectrometry, three-circle x-ray diffraction and neutron diffraction analyses. DIGITAL EQUIPMENT CORP., Maynard, Mass. For copy:

CIRCLE 173 ON READER CARD

DRAFTING AID: Cross-reference catalog lists standard printed circuit drafting shapes, and includes illustrated instructions on how to use tape with centerless pads and shapes on release liner paper for printed circuit drafting. BY-BUK CO., Los Angeles, Calif. For copy:

CIRCLE 174 ON READER CARD

EDUCATIONAL TEXTBOOKS: Two-volume technical operations manual for Bi-Tran Six digital trainer is available both for teachers and (at lower rate) for students. Cost: $29.95, free with trainer. FABRI-TEK INC., Hopkins, Minn.

OPTICAL PRINTER: MC 4000 is designed for printing telemetry data, monitoring in-process control systems with a printing rate of 6000 lpm. Booklet gives specifications, dimensions, circuit diagram, warranty and prices. LITTON INDUSTRIES, MONROE DATA/LOG DIV., San Francisco, Calif. For copy:

CIRCLE 175 ON READER CARD

FORMAT CONTROL BUFFER: Catalog includes product descriptions, I/O specifications, block diagrams, and detailed coverage of related equipment as well as ordering information. ELECTRONIC ENGINEERING CO. OF CALIFORNIA, Santa Ana, Calif. For copy:

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We've just added more speed, software and peripherals to the Raytheon 520...your next real-time systems computer.

1. ONE MICROSECOND MAIN MEMORY New high-speed working storage improves the already impressive operation times of the 520. Data acquisition/reduction systems will gain from increased throughput and availability of this high-speed main memory for buffering of real-time input/output.

2. KEYBOARD-DISPLAY STATION This new low-cost keyboard CRT display allows *high-speed* output of test data, system status information, reference tables or text, program lists, register or memory contents, etc. Up to 1040 characters may be displayed on the 6½" x 8½" viewing surface of the cathode ray tube. Instant erasure by character, line, or message is possible. On-line program debugging can be faster and easier. Use of the keyboard-display station for test direction and quick-look or remote inquiry/display is suggested.

3. DISK PACK Fast random access mass storage for bulk data or program storage. Capacity approximately 3 million characters; transfer rate 74,500 characters per second. This new drive reads and writes on IBM-compatible disk packs.

4. ANALOG INTERFACE UNITS Real-time analog data acquisition with standard, low-cost expandable interface. Analog units include the Multiverter®, with up to 96 channels of integrated circuit multiplexing, a sample-and-hold amplifier and an A-D converter in a 5¼" drawer. Typical over-all accuracy of 0.02%, 50 nanosecond aperture time and conversion rates from 30 KC (15 bits) to 50 KC (12 bits) are standard. Digital-to-analog conversion at high precision and speed are also available.

5. TEN-KEY STATION A small, 10-key keyboard provides convenient, fast, fingertip data entry as well as control of computer operations. Offered as control panel accessory.

6. REAL-TIME FORTRAN IV Raytheon 520 FORTRAN is the ASA standard FORTRAN with real-time capability. Programmers and system engineers are provided direct access to 520 interrupt facilities and the real-time environment the computer controls without loss of compatibility at the FORTRAN IV language level.

These improvements reflect our continuing program to increase the 520's real-time system capabilities. They are available to users of currently-installed and future 520's. Write for details. Ask for Data File C-117J.

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2700 South Fairview St.
Santa Ana, Calif 92704

RAYTHEON

WATCH 520 HARDWARE AND SOFTWARE PERFORM AT FJCC

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"TESTING...ZERO, ONE...ZERO, ONE...ZERO, ONE...ZERO, ONE..."

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Systems Analysts
and
Senior Programmers
FOR LOS ANGELES

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If you feel stymied in your current position and are interested in a future with an aggressive, diversified organization, this could be your opportunity.

This is a working assignment for qualified applicants who must have strong experience with FORTRAN IV and machine level programming in both scientific and commercial applications on large and small computers. B. S. Degree in Mathematics or Engineering preferred.

Please submit resume, complete with salary requirements to: Personnel Dept. B172.

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Computer Scientists,
Programmers
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C-E-I-R, Inc., internationally famed applied research and computer services company, is accelerating its growth in Washington, D. C., New York, Boston, Los Angeles, San Francisco and other locations. Exciting and stimulating new projects await computer-oriented professionals ready to step into C-E-I-R's Applied Research and Management Sciences Division as:

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Requirements vary, but in general we are looking for creative achievers with degrees (preferably advanced) in the physical sciences, mathematics, statistics or engineering, plus at least one year of computer programming experience. Professional experience will be considered in lieu of formal education.

Initial assignments will involve one or more of these varied problem areas:

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Salaries and benefits are attractive, and the personal and professional growth potential is outstanding. Learn more by arranging a confidential interview. Submit your resume to: Dr. Jack Moshman, Vice President, Applied Research and Management Sciences Division, C-E-I-R, INC., 12th floor, 1 Farragut Square, South, Washington, D. C. 20006.

C-E-I-R will recruit at the Fall Joint Computer Conference in Las Vegas.

An equal opportunity employer

CIRCLE 207 ON READER CARD

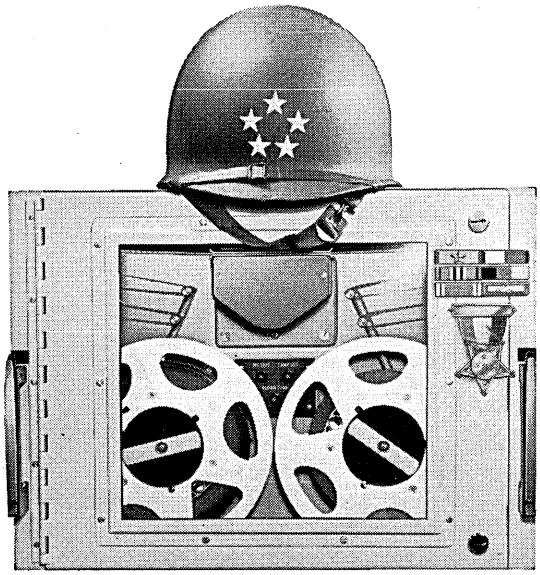
Photocircuits' fully-militarized

500 RM TAPE READER

is the only reader to pass the tests for:

HEAT, COLD, VIBRATION, EXPLOSION, SHOCK, ALTITUDE, RFI, SALT, SAND AND DUST!

(as required by MIL-E-16400 Class 3 and MIL-T-21200 Class 2)



Still...the top military performer

Users of the 500 RM fully-militarized Tape Reader will not be surprised that it passed successfully a complete "campaign" of military environmental tests. Its speed, accuracy and reliability provide a performance that meets all the worst case conditions of the above MIL specs.

Specifically designed as a military unit, the 500 RM is a high-speed photoelectric reader providing speeds to 1,000 char/sec. — with 8″ reels to give you maximum data-storage. Its smooth power comes from a unique printed-motor, direct-capstan drive. This means that all tape-reading modes are electronically controlled. The 500 RM has none of the clutch, pulley, brake or pinch-roller problems inherent in conventional or hybrid tape readers, since all of this high-maintenance hardware has been eliminated.

If your department or agency requirements demand top performance with MIL spec reliability — find out about the 500 RM Tape Reader today. Simply write or phone: Photocircuits Corporation, Tape Reader Division, Glen Cove, New York. Telephone: (516) ORiole 6-8000.

Photocircuits
CORPORATION
TAPE READER DIVISION
GLEN COVE, NEW YORK

CIRCLE 74 ON READER CARD

The next time somebody asks you why the talent is moving to the Independent Software Houses, quote him Bauer's Second Law.

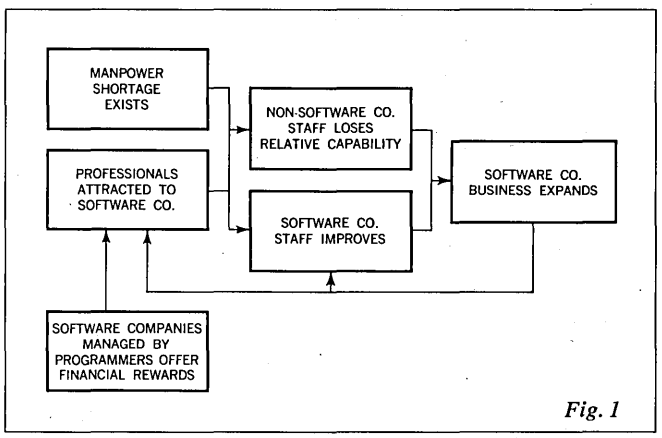


Fig. 1

Fig. 2: Dr. Bauer

Bauer's Second Law: Talent migrates from areas of well defined and stratified responsibility to areas of expanding activity at a rate proportional to the rate of expansion. Or, stated more simply: *talent goes where the action is.*

COROLLARY

Independent software companies, those not associated with a manufacturer or user group, are attracting an increasing percentage of available programming talent.

MANPOWER SHORTAGE EXISTS

Our basic premise is that talent, especially top talent, is in limited supply in any field. In the software industry the demand for top-rated specialists exceeds the supply. Consequently, software experts have a choice as to where they work. At present, and with increasing frequency, they choose to work for independent software companies. This is not to say that you can't find very talented people employed by computer manufacturers or user organizations. You certainly can. But more and more of them concentrate in independent companies.

SOFTWARE COMPANIES, MANAGED BY PROGRAMMERS, OFFER FINANCIAL REWARDS

It is true that part of the attraction is financial. Independent software companies depend on talent for their livelihood and consequently are willing to pay for it in several ways. Empiricists please call.

PROFESSIONALS ATTRACTED TO SOFTWARE COMPANY

But specialists are attracted to the independent company by more than money. A professional, given his choice, would rather work among his fellows. It is always best to work where your contribution is essential to the success of the enterprise, a place where you feel yourself in the mainstream of the business. Furthermore, when a man and his management are of the same discipline his needs are understood, his accomplishments rewarded, and his individual worth appreciated. Finally, working among top talent, a man can improve his own skills. This is especially true where people who have relatively narrow specialties within the basic discipline have a chance to exchange ideas and to learn from one another.

SOFTWARE COMPANY STAFF IMPROVES

For these reasons the staff of the independent software company improves, both in quality and in quantity. Since the talent pool is limited, it follows that the increased capability of the independents results in a decrease in the relative capability of non-independent software groups.

SOFTWARE COMPANY BUSINESS EXPANDS

This increase in capability brings more business to the independents. This in turn, makes it possible for the software company to offer more challenging work, more responsibility and more rewards. All this attracts still more talent. Thus the whole process repeats itself and becomes self-propagating.

IS THE INDEPENDENTS' GROWTH GOOD FOR YOU?

In five short years the independent software industry has grown from a meager $5,000,000 annual business, to $70,000,000 last year. And this year the figure is expected to double. Such growth must have sound economic reasons. There must be something the independents have to offer. There is. Stated in the simplest terms, the independent software firm can offer a pool of specialized talent which few users could afford to maintain for themselves. You can buy all this expert know-how, and use it for just as long as you need it to solve a given problem. And you will pay less than if you tried to solve the problem yourself. Furthermore, you will get the results on time.

HOW DOES INFORMATICS FIT IN?

Within our own organization (you knew the commercial was coming, didn't you?) we can call upon systems specialists, language specialists, experts in artificial intelligence, in data retrieval, in PERT, and many more. Without even leaving the building. Now, this kind of talent doesn't come cheap. (Look at our payroll and at our salary incentive plan, unique in the software industry.) We're always busy working on the latest problems. Right now, about 80% of our work is in the new field of on-line computing systems. We sponsored the first national symposium on the subject together with U.C.L.A. (We'll be happy to send you some of the papers presented in return for the coupon, below.)

THE MORAL:

If you have read this far, you might be interested in talking to us further about our services, capabilities, and opportunities. Simply call (213) 872-1220 and ask for me, for Frank Wagner, for Bob Rector or for anyone else on our staff. If more convenient call Werner Frank at our Washington office (301) 654-9190.

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Sherman Oaks, California

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☐ On-line CRT Displays: User Technology and Software

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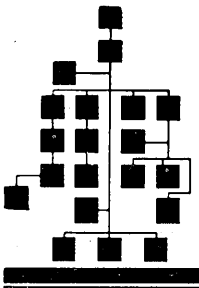
An Equal Opportunity Employer.

P.S. IN CASE YOU'RE WONDERING, BAUER'S FIRST LAW IS: IF THE PROGRAM HAS A BUG, THE COMPUTER WILL FIND IT.

CIRCLE 75 ON READER CARD



people IN DATAMATION

■ George Stibitz and Konrad Zuse have been named joint recipients of the Harry Goode Memorial Award for 1965. The award has been established by the American Federation of Information Processing Societies to honor outstanding contribution to the information processing arts.

■ Dr. John W. Mauchly, co-inventor of the first digital computer, has moved up to board chairman, Mauchly Associates Inc., Fort Washington, Pa. Robert K. Stern has been appointed president.

■ Ned W. Buoymaster has been elected president of Ferroxcube Corp. of America, N.Y. He will also serve on the board of directors and holds responsibility of marketing.

■ Prof. Edward A. Feigenbaum has been named director, Stanford Computation Center, Stanford Univ. He replaces Prof. George E. Forsythe who is head of Stanford's Computer Science Dept.

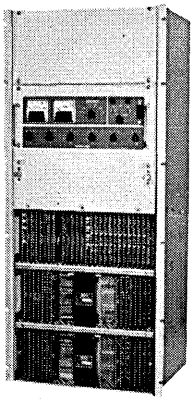
■ Peter Z. Ingerman has been chosen manager, language systems standards and research, RCA EDP. Previously he was associated with Westinghouse Defense and Space Center.

■ James R. Bradburn has been appointed division vp, RCA EDP, Cherry Hill, N.J. He was formerly vp for engineering and manufacturing, Burroughs Corp., Detroit.

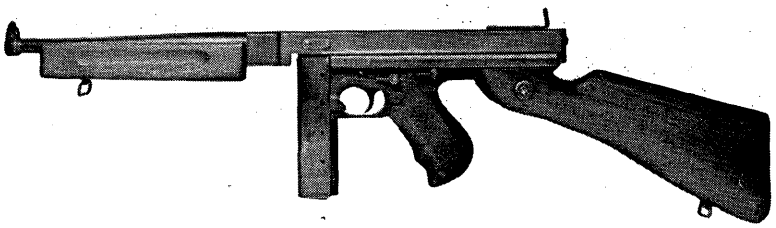
■ Lowell Amdahl is president and Ed Boutwell vp of a new firm, COMPATA, Inc. specializing in system design and analysis applications, Tarzana, Calif.

■ Robert L. Patrick, editorial adviser and frequent contributor to *Datamation*, has been named to the L. A. Traffic Commission.

■ Robert R. Kley is president and James C. Kellogg vp of a new company, Technology Planning Center, Ann Arbor, Mich. Krey and Kellogg are former defense and space system analysts.



What does it take to put a Lockheed memory system out of action ... this?



Just about. Because we've done the most thorough job of "worst-case design" you'll find in any high-speed memory system available. Whether uninterrupted computer time is simply profitable, or vital to you, you need Lockheed's CC-100 (1 μsec) or CC-200 (1.75 μsec) memory systems. They are totally designed for reliability and flexibility.

For instance, to drive 74 bits, many other memory systems require a minimum of two core driver circuits. Lockheed Electronics Company's unique design approach makes one circuit do the job. With power to spare. Result: fewer circuits, greater reliability, lower cost.

Lockheed's exclusive three-way "1-0" signal discrimination in the sense amplifier circuit is another example. No signal can pass until it has faced time discrimination, threshold discrimination, and width discrimination. Result: a new order of accuracy and reliability.

Unique "plug-in" memory stacks add flexibility as well as dependability. A low-capacity Lockheed system can be economically enlarged later to 74 bits and 32,768 words... or more. A 1.75 μsec Lockheed memory can be quickly converted to 1 μsec, or vice-versa.

Here's another reason why Lockheed memory systems enjoy a reputation for unusual dependability: total quality control because Lockheed is the only manufacturer producing complete systems – including cores, planes, and printed circuits—under one roof.

More facts on Lockheed memories: operating temperature range 0° to 50°C. • All-silicon semiconductors • Commercial or military specs • Standard rack or special mounting • Numerous operational and equipment options • *Write for full technical data now.*

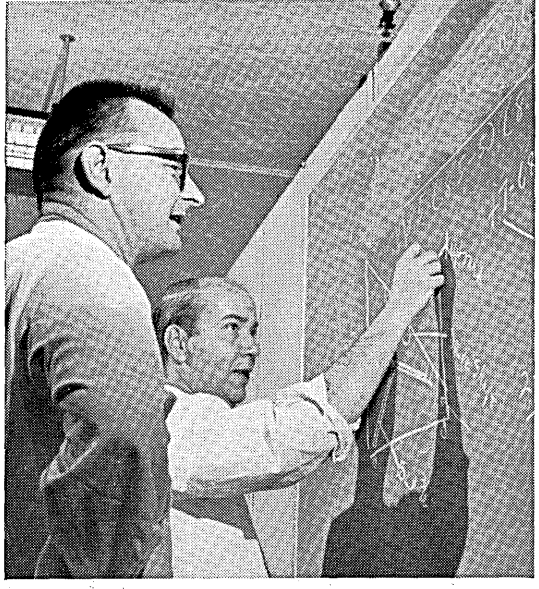
Lockheed
Electronics Company

6201 E. Randolph St., Los Angeles, California 90022 • A Division of Lockheed Aircraft Corporation

See us at FJCC, Las Vegas. Booth 108-110. Bring your own machine gun.

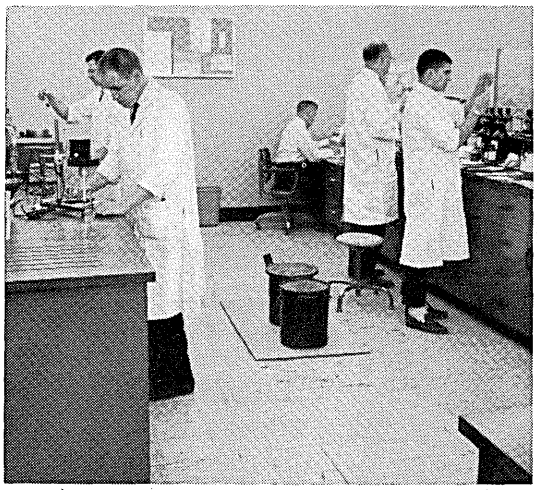
CIRCLE 77 ON READER CARD

Moore Research gives you 'built-in' quality

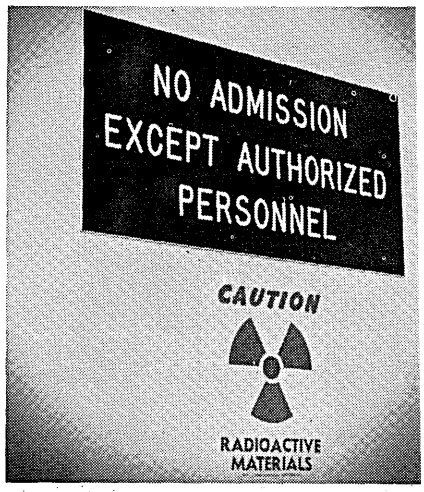


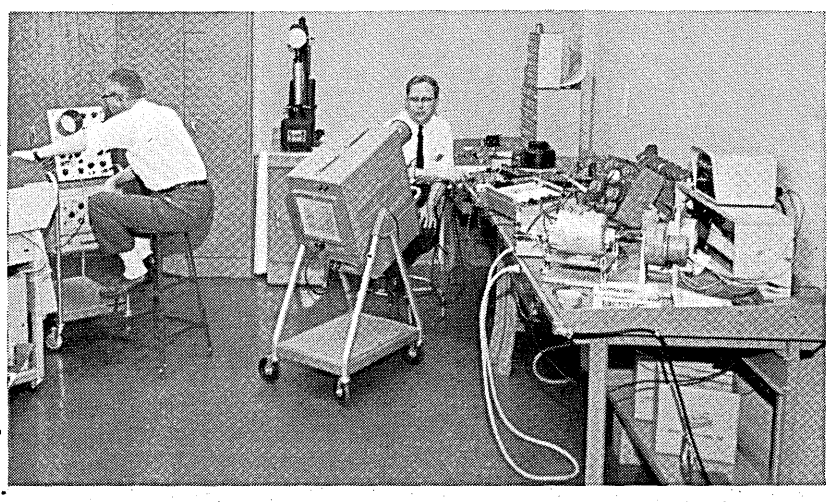
Moore Research is an 'extra value' you get in every Moore product you use. The largest, most varied in the industry, Moore Research is your assurance that maximum quality and superior performance are built into every product. Using the most advanced research techniques and facilities, Moore Research develops new products and quality that are superior in every detail—in raw materials, in production, in final results for you. From start to finish, you are assured of maximum performance, no matter what your forms or forms-handling need. Moore Research means built-in dependability in every Moore product —new or old—that you buy. If you work with forms, we can show you how to make forms work for you.

CHEMICAL RESEARCH—Intensive activity brings improved quality, new specifications in papers, inks, carbons.



NUCLEAR RESEARCH, like that used to produce better carbons, helps set industry quality levels.





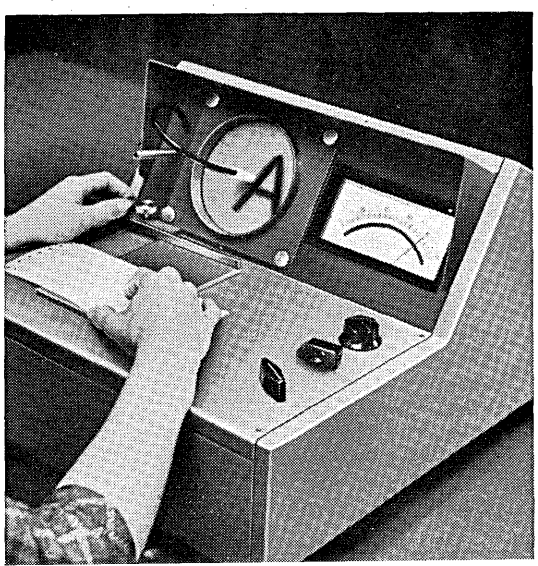
MACHINE RESEARCH—New electronic discoveries are incorporated in Moore forms-handling equipment to give you faster, precise production.

MOORE BUSINESS FORMS, INC

'The right business form for every form of business' • Niagara Falls, New York • Park Ridge, Illinois • Denton, Tex. • Emeryville, Calif. • Over 500 offices and factories in North America

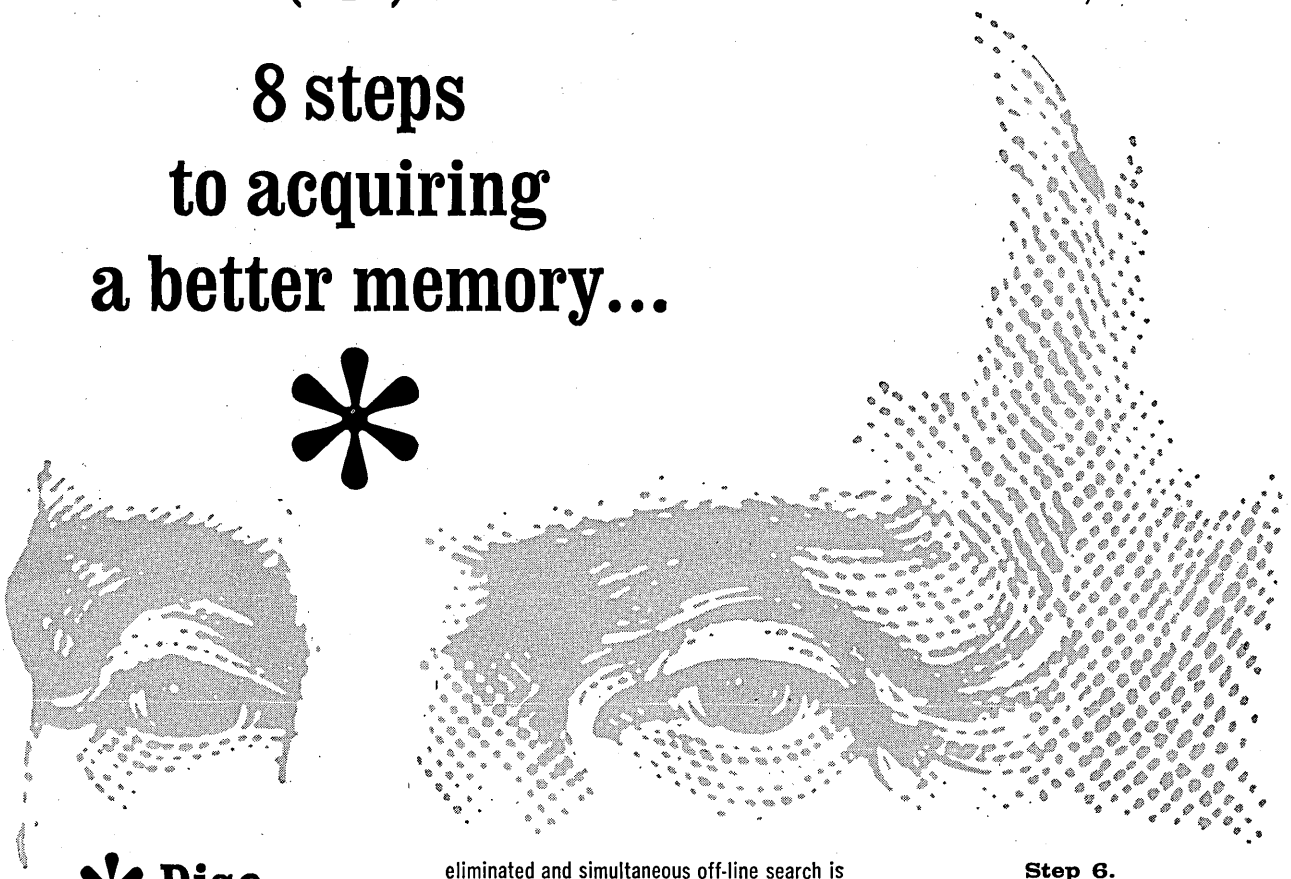
CIRCLE 78 ON READER CARD

FORMS RESEARCH promotes precision printing (OCR, MICR), new production equipment, and new forms constructions.



VISIT OUR BOOTH (422-4) AT THE FALL JOINT COMPUTER CONFERENCE, LAS VEGAS

8 steps to acquiring a better memory...



* Disc mass memory, that is.

For "time-sharing" and other applications where various computer systems must draw upon one large-capacity, central memory file designed for continuous and virtually instantaneous information processing, the LIBRAFILE 4800 mass memory produced by Librascope Group of General Precision, Inc., offers many remarkable new features. Consider the following before you buy or specify:

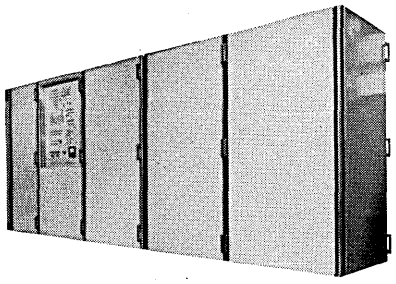
Step 1. Consider Capacity:
Where an extremely large amount of data must be stored, the memory element of the LIBRAFILE 4800 has an initial capacity of 400 million bits of information with expansion capability to 6.4 billion bits on a single trunk line.

Step 2. Inquire About Access and "Time Sharing":
The technique of information retrieval used by the random-access 4800 is either fixed-address or record-content search, depending on the master-control electronics used. Average access time is 35 milliseconds. Search by record-content is an exclusive technique that permits any desired field to be used as the access key so that where the data is stored need not be known; only what information is needed. Costly flagging and table look-up are eliminated and simultaneous off-line search is permitted. The 4800 can be easily incorporated into time-sharing computer networks.

Step 3. Consider Flexibility:
The LIBRAFILE 4800 mass memory can be used with any data processing system, whether already in use or scheduled to be installed in the future to provide faster, more accurate, more reliable operation with greater storage capacity.

Step 4. Inquire About High Transfer Rates:
The Series 4800 disc files can be organized to transfer data at rates from 1 million up to 160 million bits per second. This is accomplished through multiple-head read/write operations. (The 4800 discs have one head for every data track.) Through adaptation of special electronics, data rates approaching 1 billion bits per second are possible for special applications.

Step 5. Ask About The Manufacturer's Experience:
Behind the LIBRAFILE 4800 mass memory is the extensive background and 28-year history of Librascope Group of General Precision, Inc., in computer equipment and components.



Step 6. Check The Equipment's Performance Record:
LIBRAFILE 4800 mass memories are a key part of a General Precision/Librascope data processing system in Headquarters USAF's 473L command-and-control system in the Air Force Command Post at the Pentagon. More than a million headbar hours have been logged without a single head-bar failure. And, a scheduled installation for a scientific laboratory will provide a common data base for eight powerful computers, enabling many scientists and engineers to "share" the system on virtually a simultaneous basis. The 4800, in this instance, will help replace magnetic-tape equipment twelve times more costly and which must now be manually monitored to provide the data base.

Step 7. Request Detailed Information:
Write today for our brochure showing applications, typical configurations, and complete specifications.

Step 8. Call or Write Us:
The quickest and surest way to acquire a better memory (a LIBRAFILE 4800 mass memory) is to contact our Marketing Department. The address is shown below.

SYSTEMS DIVISION
GENERAL PRECISION INC.
LIBRASCOPE GROUP
808 Western Ave Glendale 1, Calif.
Phone: (213) 245-8711

CIRCLE 79 ON READER CARD

(Continued from page 88)

Against this background of bureau activity, a new company has emerged with another slant on the business. Called the Computer Office, London, it intends to act as the broker for any machine user with spare capacity available for sale on competitive terms. From an initial survey of users, Max Lipman, a former ICT salesman and head of Computer Office, says that 150 users in the U.K. have indicated they have a total of 3,700 hours a week surplus capacity they are willing to sell. Lipman has recruited systems and programming staff, but his main job is to organize the matching of bureau customers with available machine facilities and to plan the handling of data being transferred across the country. If successful, Lipman may severely undercut the prices of the full-time bureaus by negotiating reasonable prices for second and third shifts with spare machine-capacity vendors.

SWEDISH MANUFACTURERS SHARE A GE 635

A GE 635 delivered to Swedish electrical combine ASEA is to be made available to other industrial users. The machine has been installed on the premises of a data processing user association called Industridata, which includes SAAB and Facit as members. SAAB makes its own range of systems. Facit intends to drop its slow-moving main frame line and concentrate on its expanding peripheral business.

ICT BEATS OUT IBM; THAT'S POLITICS

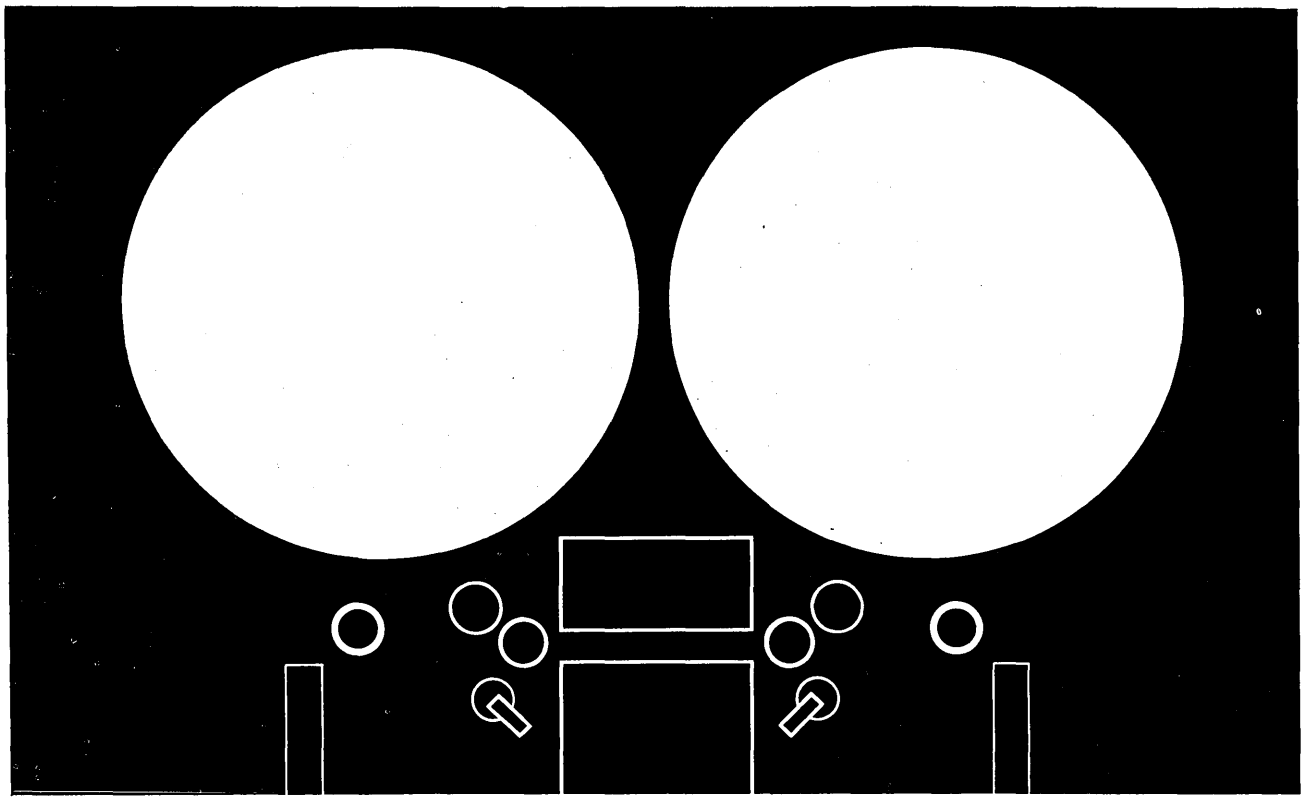
ICT stole a march on IBM last month in the fight for the U.K. local government market, worth some $60 million in prospective business. The big surprise came with a plum IBM user, West Sussex County Council, changing from a 1401 with 360 intent to a $600,000 ICT 1904. West Sussex had developed many special packages for jobs such as health control and has been regarded as a pioneer in local government dp techniques in Britain. The bouquet came for ICT because top priority was for software. But the real importance is that local authorities in Britain have their own self-generated "exchange-of-information" club in dp. Close watch is kept on each others' activities in buying matters.

LARGE FRENCH USERS ARE UNIVAC TARGETS

With a comparatively small division in France, Univac is pitching at large-scale users who are prospects for either a big one-off system or a data communications hook-up. The 1107 at Paris Univ. is to be updated to an 1108 next year. Also, SCNF (French railroads) will add a 418 to its twin 1108's next year. The 418 will handle message switching for jobs such as wagon location and scheduling. While Univac leaves the small machine side of the French market alone, ICT is making inroads with card and tape versions of the 1004 (licensed from Univac) and its own 1900 series.

ODDS & ENDS

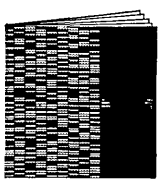
Number of service bureaus in Germany has grown from 50 in 1960 to 80 today, according to Tobias Schuler, head of a chain in Europe. There were 32 in France in '60, 85 today; in Switzerland they've grown from 10 to 25; Austria, eight to 17; Belgium, eight to 10 ...According to latest reports, Japan's output of edp gear rose in value from $5-million in '60 to $70 million last year...The Netherlands' computerized postal checking system, Giro, is handling 1.6 million transactions daily.



Buy your computer from a computer specialist

Buy your tape from the tape specialist.

General Motors, Monsanto, New York Central System, International Latex, Continental Insurance, Curtis Publishing, A.T.&T., Pennsylvania Blue Shield, Xerox Corp., Firestone Tire & Rubber, Prudential Insurance, Humble Oil, Continental Can—in fact, 16 of the top 25 companies in the United States—buy computer tape from Audio Devices. Isn't it time you consulted a specialist?

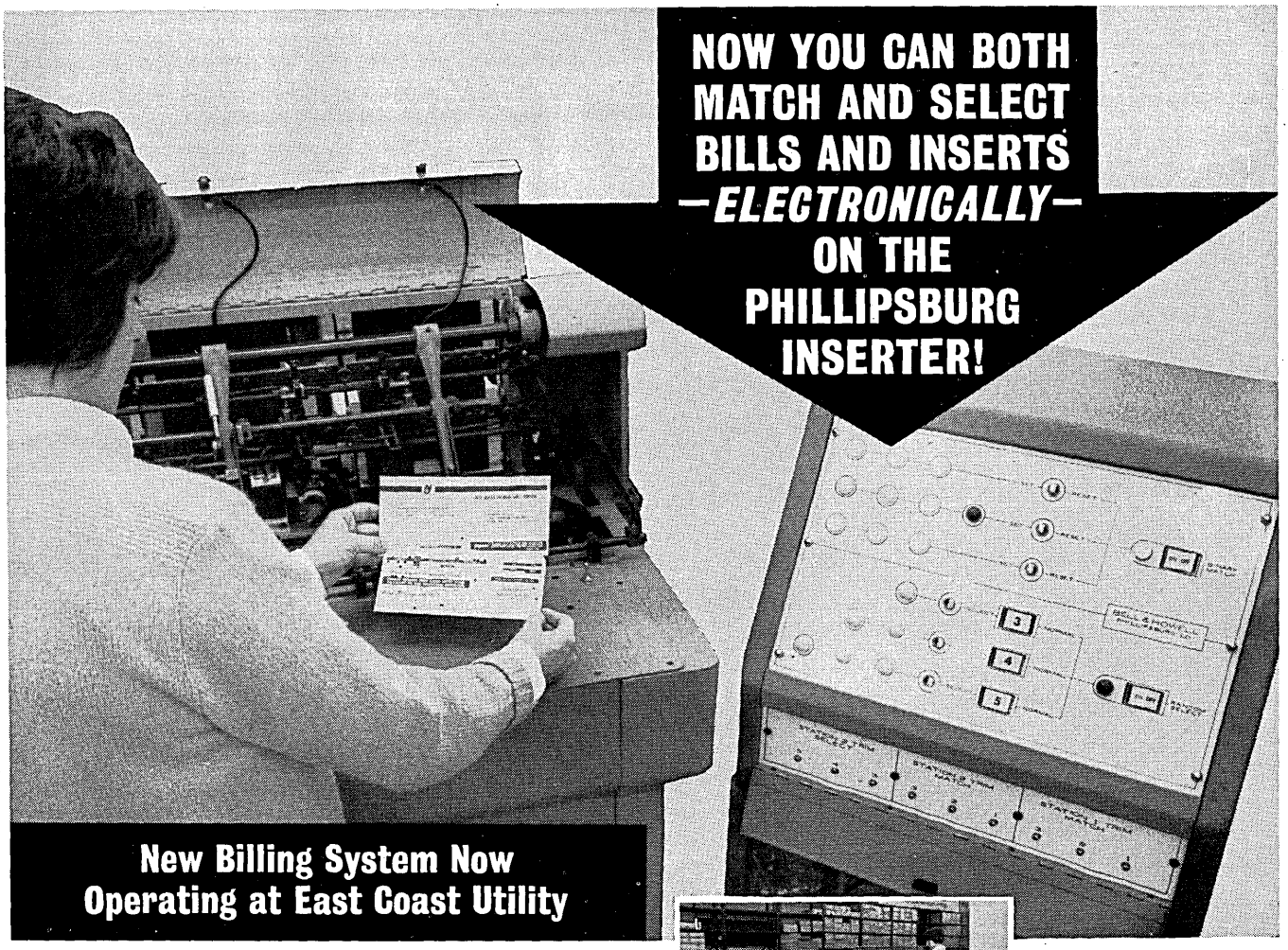


AUDIO DEVICES Inc.
INSTRUMENTATION TAPE
COMPUTER TAPE
AUDIOTAPE

The Memory Business contains useful information about modern magnetic recording tape. Write for your copy to Dept. DP-5, Audio Devices, Inc., 235 E. 42nd St., New York 10017. Offices in Chicago, Los Angeles and Washington, D.C.

CIRCLE 80 ON READER CARD

NOW YOU CAN BOTH MATCH AND SELECT BILLS AND INSERTS —*ELECTRONICALLY*— ON THE PHILLIPSBURG INSERTER!



New Billing System Now Operating at East Coast Utility

THE PHILLIPSBURG INSERTER ELECTRONICALLY—

- **MATCHES code-punched cards with their correspondingly coded printed bills.**
- **SELECTS past-due notices, resident and business advertising, product literature, renewal notices, special subscription offers, etc.**

A new electronic breakthrough enables the Phillipsburg Inserter to accomplish two of the most important jobs in a billing operation: matching and selection of inserts. Imagine a volume billing operation in which it is possible to—

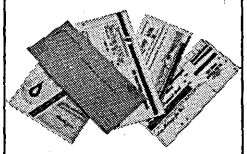
1. Guarantee that two mailing enclosures, such as a utility bill and cash card, are inserted in the same envelope,

and, *at the same time*—

2. Automatically select one or more additional enclosures, such as an overdue notice, only for those recipients for whom it is appropriate. Contents of mailings can thus be varied, as required—and all without human intervention!

The system has extra dividends built in, too. Advertising material can be piggy-backed into the same mailing, at no increase in postage. There is no costly hand-sorting when payments are returned. The savings add up quickly. This is just the newest development in Phillipsburg's electronic-oriented program of research. There's always room for improvement—even in the Phillipsburg Inserter, the world's finest, most versatile inserting machine!

Operator holds matching inserts. Console for matching and selection is at right.



SEND FOR INFORMATIVE CASE HISTORY

We've wrapped up the entire matching-selection story in an actual case history of the New Jersey Natural Gas Co. Just mail the coupon for your copy.

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☐ Send me the Case History Report on Electronic Matching and Selection.

☐ Send me your brochure, "A New Advance in Mail Inserting Through Electronic Sensing."

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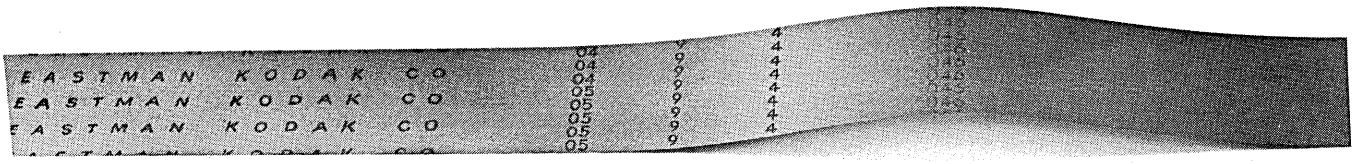
CIRCLE 81 ON READER CARD

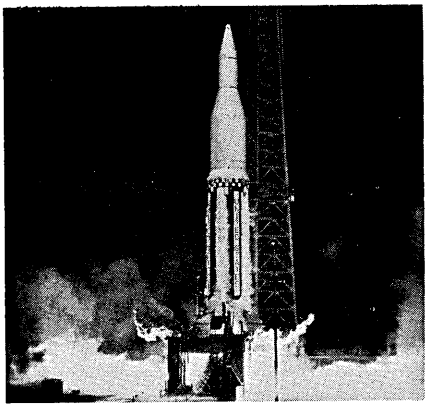
Traceability now assures positive data identification



With the new CEC "Traceable" Magnetic Tape, created and produced by Eastman Kodak, any specific run of tape may be quickly located and identified.

This breakthrough has eliminated one of the major problems in data tape recording. For no longer can important projects be hindered or delayed due to a mixup in reels. The possibility of misplaced data is now virtually a thing of the past.

Reason: an exclusive *numbering* process. All CEC tape is numbered—color-coded on the box, can, reel; even digitally numbered on the back of the *tape* itself for instant identification.



For example, on every 15 inches of tape there appears an internal Kodak reference number which immediately identifies the tape by type; and every 30 inches there is a numbered tape signature which provides an index to the coating and test records for that particular production block. So efficient is this coding method, it is possible—through the numbers on the tape, reel, can, or box—to trace any roll of tape all the way back to the master web from which it came.

However, digital coding is only one of the significant reasons why CEC Magnetic Tape is rapidly changing the state-of-the-art.

CEC tapes are divided into *four* specific categories. Collectively, they meet the most advanced requirements of *every* data recorder. Yet each tape records at the highest applicable resolution and sensitivity—with the greatest uniformity and lowest tape and head wear obtainable today.

In addition...

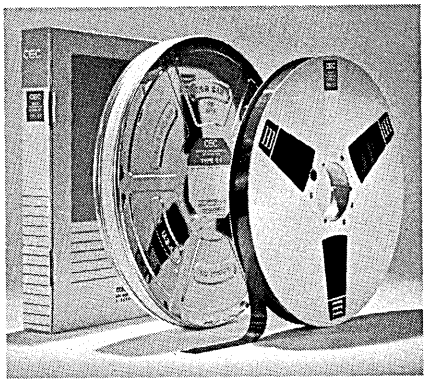
▣ Only CEC tapes provide a standard nomenclature for simplified identification and ordering: S-1 standard, 100 kc; SX-1 standard extended, 300 kc; M-1 medium band, 600 kc; W-1 wide band, 1.5 mc.

▣ Only CEC tapes are so precisely differentiated that users are no longer subjected to the time-consuming burden of performance evaluation.

▣ Only CEC tapes come shielded in metal containers—packed in cardboard filing boxes covered with protective plastic sleeves.

▣ Only CEC tapes are protected from shipping and storage damage by means of a plastic waffle hub, thus preventing tape serration and flange deformation.

However, with all these advantages, CEC Instrumentation Tape costs *no more* than the tape you are now using.



If you have not already done so, write now for your free CEC INSTRUMENTATION TAPE CHART. This special chart lists CEC tape categories, applications, and models of recorders for which each tape is recommended. Ask for CEC Chart DM-47-X19.

CEC

Technical Supplies Department

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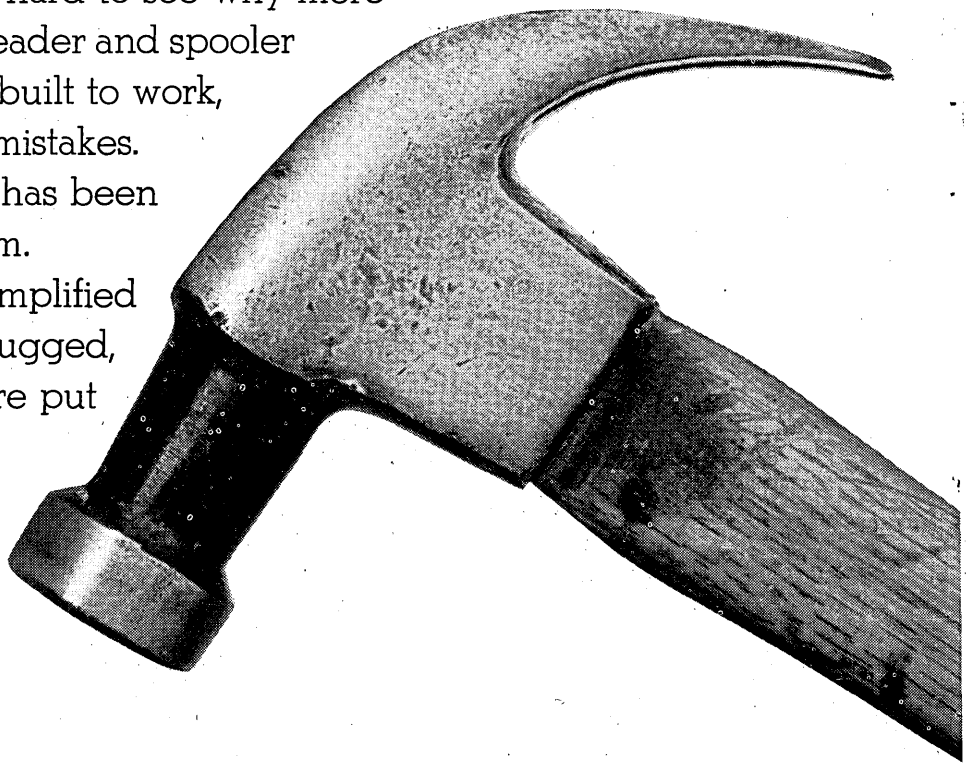
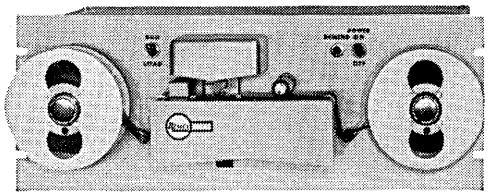
CIRCLE 82 ON READER CARD

If you ever get tired of waiting for a Remex tape reader to break down, you can always try hitting it with a hammer. It's not hard to see why more companies buy Remex tape reader and spooler units than any other. They're built to work, work, work. Without making mistakes. The number of moving parts has been kept to an absolute minimum. The solid state circuit has a simplified design. And then there's the rugged, yet precise way these units are put together. You may find yourself looking for a bigger hammer. For details, phone 213 772-5321, or write us at 5250 West El Segundo Blvd., Hawthorne, Calif. 90251





REMEX

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a division of
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CIRCLE 54 ON READER CARD

(Continued from page 21)

not provide the total copyright protection sought by software creators. "The big difficulty is trying to accommodate basic copyright concepts to wide-ranging technological developments still in a process of evolution," said a Copyright Office official.

Congress has shown itself reluctant to "freeze" precise, detailed language into a law that may well apply for the next 50 years. A recent report by the House Judiciary Committee noted that "it would be a mistake for the statute, in trying to deal with such a new and evolving field as computer technology, to include an explicit provision that could later turn out to be too broad or too narrow..." While the report made it clear that the revised copyright law would apply to computer inputs and outputs in their present formats (i.e., punched cards, mag tapes, standard printout), it noted that "in many cases in the future the end product of a computer process will not be tangible printout but will be a visual image or sometimes even a performance."

FCC LAUNCHES STUDY ON 'COMPUTER UTILITIES'

A Federal Communications Commission taskforce has begun an intense study of the public "information utility" based on third-generation computing equipment and what its significance may be vis-a-vis the regulatory responsibilities of the commission. Since the likely candidates to organize and operate such public information utilities include present computer service companies, computer manufacturers and large-scale user companies as well as the large common carriers, AT&T and Western Union, the FCC is uncertain of its regulatory responsibilities.

According to Bernard Strassberg, chief of the Commission's Common Carrier Bureau, the study will attempt to answer three basic questions: 1) What aspects of computer utilities will involve activities subject to present FCC regulation, 2) What aspects of computer utilities not subject to present regulation should be made so via revision of the Communications Act of 1934, and 3) What are the effects upon the growth and efficiency of computer utilities, and what need is there to change existing tariff regulations and practices of the common carriers.

Noted Strassberg in a recent speech: "AT&T's tariff regulations ... specifically prohibit its private line customers from using the leased channel for any purpose for which a payment (apart from cost sharing) is received, or for the collection, transmission or delivery of any communications for others. To the extent therefore that computer enterprises may seek to employ common carrier channels for the rendition of a package of services taking on the character of data processing and communication, questions are presented as to the status of such services both under the Communications Act and the tariff regulations..." There's another edge to the sword, duly noted by Mr. Strassberg. "As (computer) time-sharing increases, the economies of scale could so reduce the cost of computer use that the major cost component of the data service could be the charges for communications channels and circuits. Conceivably this might induce some large firms with the financial capability to establish their own nationwide private microwave networks."

WHO READS DATAMATION?

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Tell it in

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DATAMATION

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The quoted price is for the combination unit. The Reader and Spooler are also available as separate units. For complete specifications contact . . .

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CIRCLE 86 ON READER CARD

PROGRAMMERS & SYSTEMS ANALYSTS

IMMEDIATE OPENINGS

GERMANY	412L System — various locations throughout West Germany providing maintenance programming on command and control systems.
PHILADELPHIA	Suburban location, Willow Grove, Pa. Development of overseas AUTODIN programs. Later assignment available throughout Europe, etc.
BOSTON	Several positions, Lexington, Mass. in scientific programming and systems analysis for command and control air defense, missile re-entry, etc.
OKLAHOMA CITY	Development and maintenance of programs involving communications switching for air weather information.

In general, we are seeking persons with 2-3 years' applicable experience. Degree is desirable and in several instances, mandatory. Some qualifying experience areas are:

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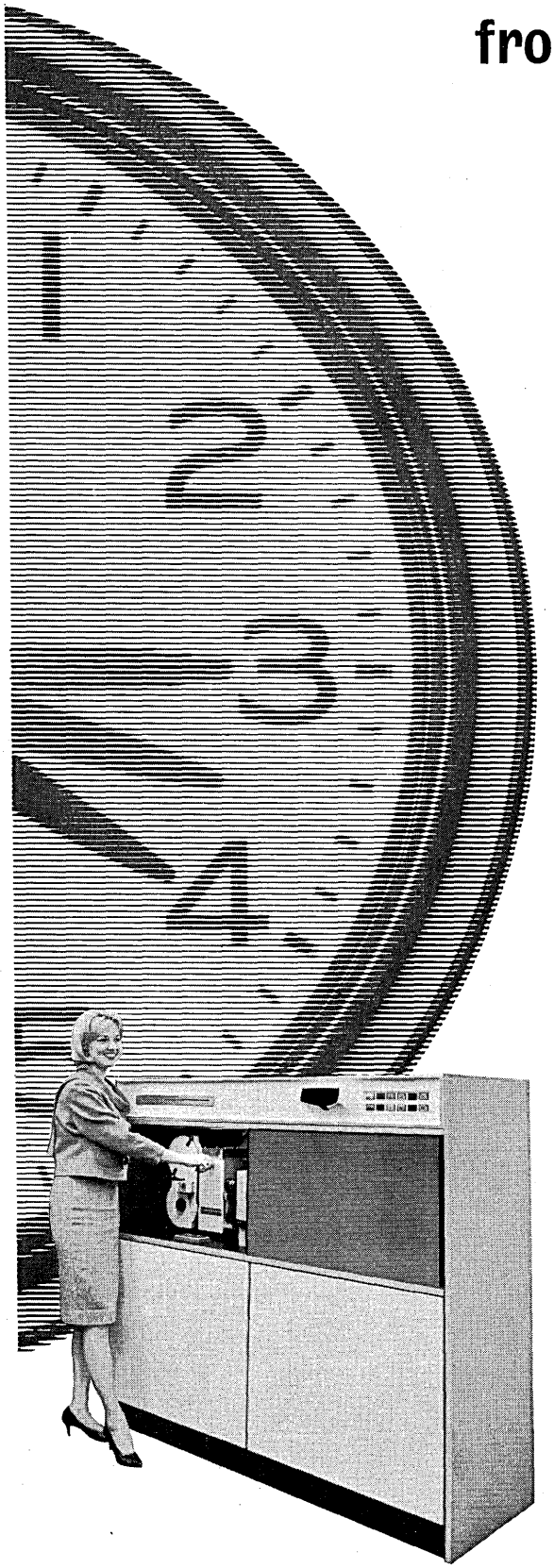
CIRCLE 105 ON READER CARD

The S-C 4400 document recorder has to work only one hour per day to cut $3,000 a month from computer printing costs!



If you now operate two mechanical computer printers, the S-C 4400 can save you thousands of dollars a month. At the same time it speeds output, increases retrieval rates and reduces data storage problems by recording all or part of your data on microfilm. The S-C 4400 can do all of this by operating as little as one hour per day.

For the second printer you pay approximately $200 per day or more. An S-C 4400 can do the same job in less than an hour, making a million line entries every sixty minutes. The cost? Approximately $182.00 based on one hour per day usage; the actual hourly rate will of course decrease with increased usage. Besides cutting printer costs by $400.00 per month, the S-C 4400 can usually replace one operator per shift as well as eliminate several thousand dollars a month or more in business forms inventory. The total result is a conservative $3,000 a month savings.

The S-C 4400 simplifies mass data processing by taking information from a computer and recording it directly on 16mm or 35mm microfilm. Today's automatic microfilm systems permit finding one document out of a million in 15 seconds.

Operation—In the S-C 4400, computer data is displayed on the face of a CHARACTRON® Shaped Beam Tube and then photographed automatically. It saves time and money by eliminating the costly step of producing paper output before microfilming. The S-C 4400 can operate on-line with a computer or off-line from magnetic tape. Magnetic tapes and paper need not be manually transported to other machines to get microfilm output. When you desire selected paper copies, they can be produced easily on a microfilm reader/printer.

No Forms Needed—Large inventories of pre-printed business forms are no longer necessary. Instead, forms are photographed on slides and inserted in the S-C 4400 projector. As needed, forms are projected by program control directly to the microfilm for recording with the computed data. One company estimates the S-C 4400 system can save more than $25,000 per month in business forms alone.

Codes Film—Film coding for retrieval systems is accomplished automatically by the S-C 4400. Line indexing marks, image count blips and MIRACODE retrieval codes can be imprinted on the film at electronic speeds.

Typical Applications—S-C 4400 can simplify data processing by recording customer histories; account, payroll and personnel records; route and rate information; credit figures; stock transfers; transaction journals; inventory reports; configuration management reports, etc. on easy to use and easy to store microfilm.

If you are interested in obtaining additional information on how to reduce your computer output costs and at the same time expand the capabilities of your computer operation, write Stromberg-Carlson Corporation, Data Products—San Diego, Department F-46, P. O. Box 2449, San Diego, California 92112.

STROMBERG-CARLSON
CORPORATION
DATA PRODUCTS-SAN DIEGO

CIRCLE 42 ON READER CARD

Air Traffic Control

People needed in MITRE's Washington, D. C. office to provide system engineering assistance to the Federal Aviation Agency. Work areas include broad level system design, computer program operational specification, configuration management, system integration and system test planning.

Communications

We need people who can help conceive new communications systems, recommend development programs to achieve these, and analyze special communications requirements generated by new systems concepts. Work areas include systems planning, analysis, simulation and design for command and control systems, missile and space systems and test range and weapons support systems, engineering of communication networks, range instrumentation, tactical air control, and survivable communications.

Sensor Systems

People needed to support theoretical and experimental programs on advanced radar and optical detection and tracking systems; feasibility and technique analysis, systems synthesis and performance evaluation.

Telemetry

Engineers are needed to work with telemetry and instrumentation. Particular work areas include telemetry standards, systems, and techniques for both airborne and ground applications. Experience should include design or analysis of telemetry systems as well as modulation theory, RF techniques and receiving and transmitting antenna systems.

Range Data Transmission

Engineers are needed to work on range data transmission. Particular work areas include digital data transmission systems analysis and testing. Experience with switching systems, modulation and information theory, and coding is desired.

Systems engineers needed for work in these vital areas!

MITRE works on the basic design and general system engineering of complex information, control, sensor, and communications systems of national importance. An important part of its mission is the development of new techniques in these areas and advancement of the general technology. If you have three or more years' experience and a degree in electronics, mathematics or physics, write in confidence to Vice President — Technical Operations, The MITRE Corporation, Box 208AU, Bedford, Mass.

Pioneer in the design and development of command and control systems, MITRE was chartered in 1958 to serve only the United States Government. An independent nonprofit corporation, MITRE is technical advisor and systems engineer for the Electronic Systems Division of the Air Force Systems Command, and also serves the Department of Defense, and the Federal Aviation Agency.

THE MITRE CORPORATION

An Equal Opportunity Employer

CIRCLE 95 ON READER CARD

What is it about a growth environment that brings out the best in a programmer?

To a programmer or systems analyst, a growth company means excitement—more stimulating problems, greater opportunities for advancement and greater personal rewards. The growth environment brings out the best of his talents and abilities. Because, in a proven growth company like IBM, he must work constantly toward greater technical achievement.

Today at IBM there are *more career openings than ever before* for programmers and systems analysts—more opportunities to achieve distinction, recognition and personal advancement.

We would be pleased to give you more detailed information about the available positions that can make the most of your talents and professional goals. The positions listed below represent only a few of the many immediate openings at IBM.

Junior Programmers: Will be assigned to a programming team after three to six months of formal programming education. Will contribute to the analysis and solution of programming problems and will eventually acquire an understanding of technical programming documentation, IBM programming systems, testing methods and analyzing test results. Will also make modifications to established programs. At least one year's programming experience is required.

Systems Programmers: Evaluate performance of programming systems and develop technical specifications in the areas of compiler design, control programs and IOCS. This work also involves technical liaison to assure satisfactory performance and adherence to specifications of IBM programming systems. Three to six years' systems programming experience is required.

Programming Systems Testing: Develop new techniques for testing systems, evaluating performance and coordinating systems development. Work involves systems generation, editing and related test activity.

Formula Manipulation Systems: Develop systems to perform algebraic manipulations of mathematical expressions. Work involves use of PL/I in the development of advanced programming languages, compilers, mathematical techniques and algorithms.

Advanced Conversational Programming Systems: Design and implementation of systems which permit more effective interaction between men and machines. Concepts such as Time-Sharing, conversational techniques, input/output, graphics, formula manipulations, PL/I and microprogramming will be explored in depth.

Programming Engineering: Work on problems in the boundary areas between programming and computer design, particularly microprogramming.

Programming Applications of Linguistics: Application of linguistics to the solution of problems in programming language development and the creation of practical systems which permit restricted English as input to a computer.

Please write, outlining your qualifications and interests, to:
D. Neyer, Dept. 701-L
IBM Corporation
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Poughkeepsie, New York
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IBM®

The popularity of our new 600 Series carries a price.

High-level staff additions.

Call it the price of success. Of course, we're happy with the number of orders coming in for our new G.E. complex of computers . . . and what really pleases us is that orders are coming from some of the most knowledgeable, technically sophisticated users in the world. Does anything confirm the superiority of the line better than winning out in today's hard, nose-to-nose competition?

But this means heavy demands are being made on our senior group of computer systems development engineers to extend the capability of the 600 series beyond the fringes of present knowledge . . . in the fields of business, scientific, real time, and time-sharing applications.

And in addition we are right now starting on a whole new "line", and numerous company-funded development programs are underway.

All this means that a wide number of openings are now available in many areas. And the men we're looking for must be equal in stature to the calibre of the present staff. Preferably they should have a strong academic background in Math, ME, EE, or Physics. This group is part of the headquarters complex in Phoenix, Arizona.

Programming (BS or MS degree with 3-5 years experience preferred) • **Business Systems Applications** • **Scientific Programming** • **Software Package Development** • **Systems Programming** • **Data Center Services** (customer-oriented programming in time sharing applications, BS/MS Math is highly desirable)

Mechanical Engineering, BS or MS required with extensive experience in packaging or high speed small mechanisms design.

Systems Engineering, BSEE or MSEE required with 5 or more years experience in large scale digital computer or related systems.

Logic Design & Circuit Design Engineering, BSEE or MSEE, with 3-5 years circuit and/or logic design experience with computers or related digital hardware.

Custom Engineering, Maintainability and Continuation Engineering, a number of key spots for engineers with interest in these areas and a background in basic computer hardware design.

If you want a chance to better your own past performance, and have experience in any of the areas mentioned above, we invite your further inquiry. There are many other openings, too, in the General Electric Computer effort in Phoenix and other major cities throughout the U.S. If you have a solid academic background and computer-related experience in design, applications, sales, service or administration, you are invited to explore these opportunities. Please write to Stephen K. Stewart, Administrator — Professional Placement, Room 42-L, General Electric Co., Computer Department, P. O. Box 270, Phoenix, Arizona.

COMPUTER DEPARTMENT

GENERAL ELECTRIC

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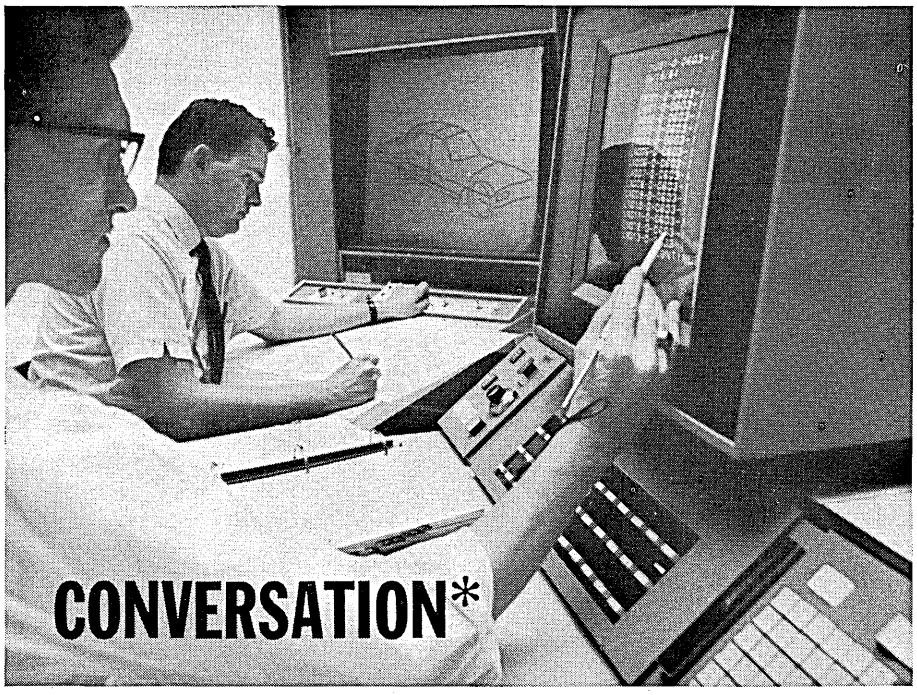
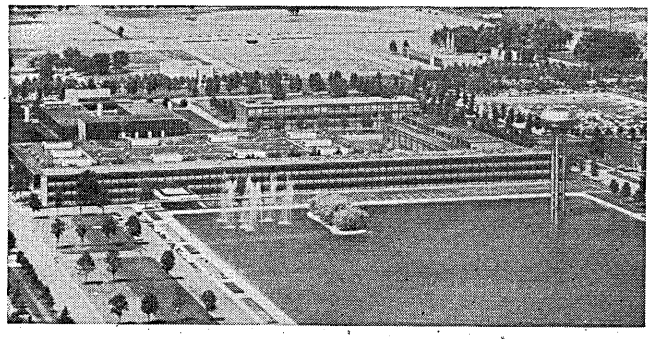
CIRCLE 97 ON READER CARD

OPPORTUNITIES AT THE OUTER EDGE OF COMPUTER TECHNOLOGY . . .



***CONVERSATION.** *Here's one approach to developing the time-sharing systems of tomorrow. First, build your own man-machine communication laboratory from the ground up. Including every bit of the software. Then invite in people doing real-world problems, really real-world. Test out their ideas. Test out your ideas. Test and test again. (Shown is real-time conversation at the graphic console of the GM DAC-1 system, Design Augmented by Computers. DAC-1 was described as "A Laboratory for the Study of Graphical Man-Machine Communication" in one of our 1964 AFIPS papers.)*



Home of the General Motors Research Laboratories consists of these eight buildings making up part of the 330-acre GM Technical Center. This model campus of technology is located in suburban Warren, 13 miles north of downtown Detroit and within easy driving distance of top Michigan and Canadian recreational areas.

As conversational computing enters the shakedown world of reality . . . as time-sharing approaches the big scale . . . the pace of advancement in computer technology will be set by the person creating new "tools" for man-machine communication.

This is the **SYSTEMS PROGRAMMER,** the **SYSTEMS ANALYST** or the **APPLIED MATHEMATICIAN** who can design, build and evaluate the wide variety of software necessary to any man-machine problem-solving system.

This is also the person who will want to join in the pioneering work of our Computer Technology staff . . . where facilities for man-machine communication are fully operational . . . where ideas can be tested on-line . . . where future man-machine systems involving a multiplicity of different consoles are now under development.

Most likely this person will have a master's or doctor's degree in mathematics, physics, or engineering, some 7090/94 experience and academic courses in the information sciences: compiler construction, symbol manipulation, queuing theory, numerical methods, etc.

INTERVIEWS AT FALL JOINT COMPUTER CONFERENCE, LAS VEGAS

In Las Vegas, call 734-4110 at the Dunes Hotel on Tues., Wed., Thurs., November 30, December 1 and 2, and ask for Mr. D. E. Hart, Head, GMR Computer Technology Department . . . or, if you prefer, send your résumé today to:

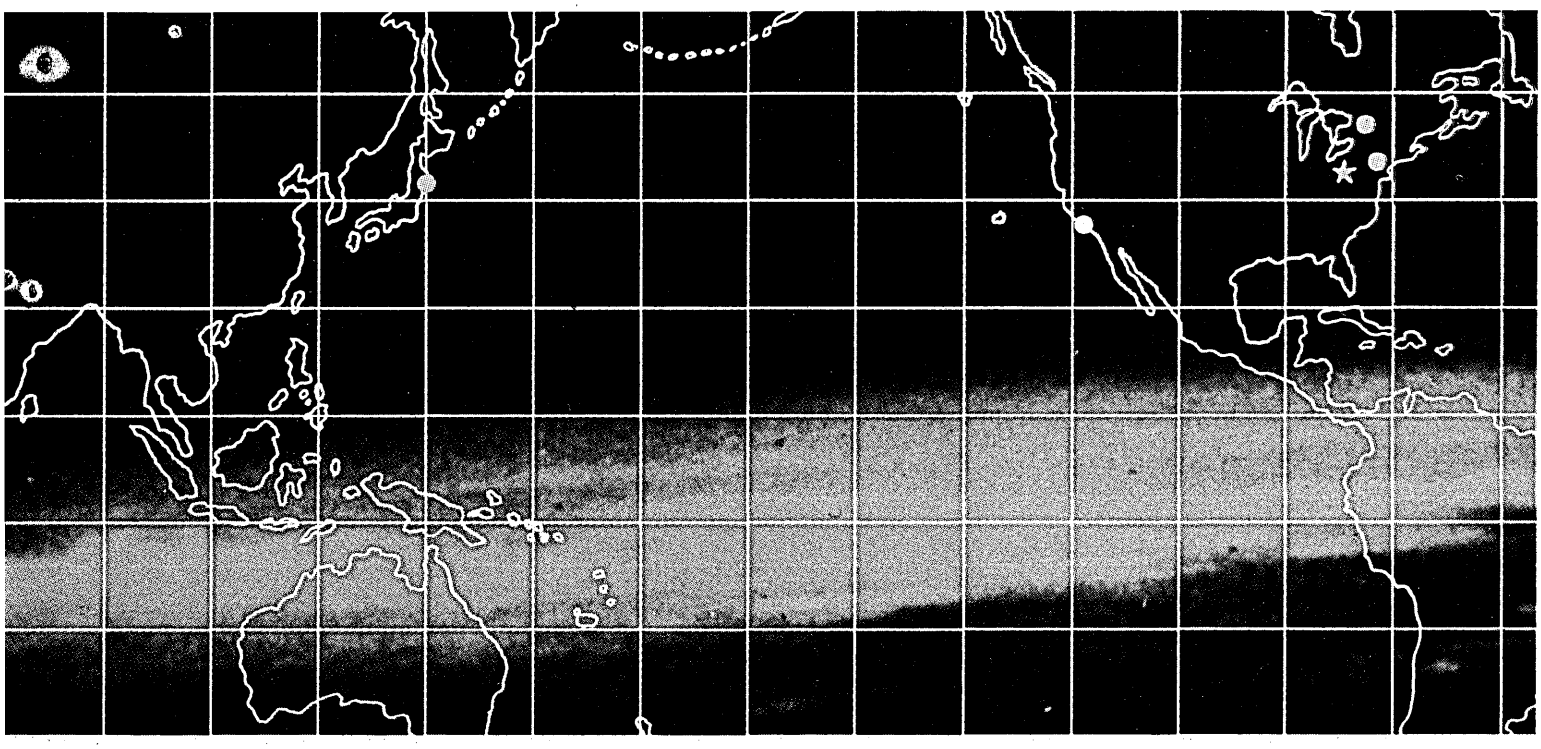
Mr. J. B. Sparhawk, Personnel Staff

General Motors Research Laboratories

Warren, Michigan 48090 **An equal opportunity employer**

CIRCLE 98 ON READER CARD

NCR is moving fast in worldwide business automation.



How about you?

Does your future in digital systems look distant or uncertain? At NCR Electronics Division in Los Angeles—one of 12 major NCR facilities throughout the world—the Computer Era is a reality *now*. NCR sales of advanced EDP hardware in more than 120 countries tell you that this Division is as successful as it is creative. Join the men who developed CRAM, the NCR 315 RMC Rod Memory Computer and the 420 Optical Journal Reader—and share in their next success. Your future can start *today* at NCR.

ADVANCED PRODUCT PLANNING SPECIALISTS

To work in advanced product planning group responsible for determining and analyzing requirements of new product markets, recommending product development programs needed to promote new ideas, formulating and specifying new products based on state-of-the-art and beyond-the-state-of-the-art hardware, software, and application concepts.

Ability to deal with "total systems" concept in a business data processing environment is essential. Specific experience in such areas as time sharing systems, multi-processing, data transmission technique, programming language design, list processing, and information retrieval is desirable.

Requires a broad background in business data processing systems with a minimum of eight years of hardware and software systems design experience. Advanced engineering or science degree desirable.

ADVANCED MECHANISMS SPECIALIST

For analysis and design of complex computer mechanisms. Must have knowledge of applied mechanics and high-level mathematical ability. PhD required.

MAGNETIC RECORDING SPECIALISTS

Senior and intermediate positions for men with experience in advanced magnetic recording techniques. Knowledge of media, circuitry and magnetic head design necessary. Requires BS in engineering or physics.

ADVANCED MEMORY-RESEARCH SPECIALISTS

Positions require MS in EE or physics and previous experience with nanosecond pulse technique and high-speed applications of magnetic cores or thin films to memories with computer systems logic and hardware.

ADVANCED SYSTEMS SPECIALISTS

Senior-level positions in advanced logic, circuitry, and memory development and preliminary design of beyond-the-state-of-the-art data processing equipment. Considerable experience required in the over-all system design and integration of commercial computing equipment. BSEE required with advanced degree highly desirable.

ELECTRONIC PRODUCT ENGINEERING

Positions require a BSEE degree with experience in designing digital computer equipment and in maintaining liaison with manufacturing.

PACKAGING

Positions entail layout and design of packaging for computer systems. Applicants must have previous experience with electronic computers or electro-mechanical devices. Background in miniaturization utilizing thin films and integrated circuits is desirable. BSEE required.

SOFTWARE PROGRAMMING

Positions entail development of software for various computer input/output routines, operating systems and monitors. Applicants must have previous programming experience with machine language on a large file computer.

DESIGN AUTOMATION PROGRAMMING

Positions require previous experience in programming for design automation, good understanding of engineering and hardware problems, and BS degree in math, engineering or related field.

CIRCLE 99 ON READER CARD

LANGUAGE IN THE SIXTIES

PL/I is not all things to all people, and existing major languages aren't on their way out right now, it was generally agreed at the SHARE-JUG conference in Philadelphia Oct. 7-9. But – few denied that PL/I is here to stay, and PL/2, 3, . . . n will come.

This mammoth new language effort by IBM, which M. D. McIlroy of Bell Labs stated "can't be ignored" and "really is good," was the real focus of the cooperative workshop on the "Programming Language Objectives of the Late 1960's." The intent of the meeting, attended by about 100, was to provide a forum for manufacturers and users to discuss these objectives, how present languages meet them, and how these objectives and languages may change to meet future requirements.

During three days of sessions, a multitude of points—economic and technical—were stated and debated. A programming language should be easy to use; emphasis should be placed on facilitating man-machine interaction; the language should make programs easily transferable from one installation to another and from an old to a new system; it should accommodate the peculiarities of various hardware complexes, including I/O, core, random access files; it should facilitate production of efficient code; it should decrease the cost of building compilers and documenting; it should be easy to teach, to expand, to modify. Further, standardization should help provide some of these objectives.

A panel of manufacturers, represented by SDS, IBM, RCA, Univac, Burroughs, and CDC, was concerned with the programming language objective of providing tools which would keep users happy (in a broader range of applications) and with keeping themselves competitive. But, financial and manpower resources are being exhausted by the multiplicity of programming languages today.

IBM, said William McClelland, does not see "any need for any other major new procedure-oriented language development which is not a direct and essentially compatible extension of the existing languages." Too, the development of "another language at the same level would not be worth the effort." The ideal, he proffered, one IBM is working on, would be that "manufacturers provide not compilers for languages themselves as a principal product, but a metalanguage compiler and expressions of standard forms of the appropriate language in that metalanguage users would then be able to tailor the language to their individual needs.

What about existing languages? Standards on two, FORTRAN and ALGOL, are (at time of writing) being voted upon at the ISO meeting in Japan. Will manufacturers support these standards? Attitudes, though positive, varied slightly. IBM gave an unequivocal yes for FORTRAN and COBOL standards, while Univac noted that it would be "guided by the needs" of its users.

Throughout the meeting PL/I was compared with other major procedure-oriented languages, and examined in the light of some of the objectives laid down by the attendees. Repeatedly hammered home was the gigantic user investment in programs. A GSA spokesman on PL/I was quoted by a panelist as saying the "government would have to protect its investment in COBOL and FORTRAN." (Elsewhere it was referenced that the 1964 inventory of government edp equipment lists 5885 applications, 19% using FORTRAN as the primary language, 3%—COBOL, and 1.8%—ALGOL).

E. F. Cooley of Prudential Insurance Co. questioned whether PL/I meets the commercial users' needs as well as COBOL, and, since these users put the most money into equipment rentals, their needs should receive "high priority." Another panelist, with the tale of the still existing schism between FORTRAN II and IV as a backdrop, noted that PL/I stands the best chance of replacing COBOL and FORTRAN at a point when we are changing hardware and PL/I is the only language offered. Too, some felt that if PL/I doesn't replace "two or more" languages, it shouldn't exist.

What's a PL/I? In the "great debate" on the language, Joseph Smith of RAND Corp., representing a vehement anti-PL/I position, protested the "Swiss Army knife" approach, because it is going to cost the user much money to have this "unbelievably intrusive general purpose thing there intruding on your specific applications."

McIlroy, "pro" panelist, defended, with some user support from the floor, the concept of bringing in all users, all aspects of standard languages under one tent. PL/I accomplishes its attempts to be "powerful, natural, and well-balanced," he thought, and commended IBM for public-spirited cooperation by "listening to all comers"

in developing it. "Its dependence upon the 360 has practically vanished."

On the other hand, Tom Steel of SDC argued that the designers of PL/I had used the "wrong model of the world." It fails, he said, to recognize "an express train bearing down on us by the name of on-line," to cater to the non-programming user, to understand the concept of elegance: generality, parsimony, extendability. It does have some generality, he said, but it's artificial. "You don't want the '1000' data types" PL/I is said to have, "but one or two that are sufficiently general that they can encompass all the things that these 1000 ad hoc devices do." If you have this, he stated, you have parsimony.

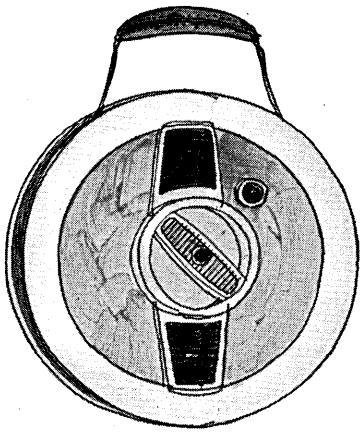
Steel went on to say that the conversion problem is not only one of programs but also of people, and teachability hasn't been proven, at least not by the 170-page manual. "Much could be done still, but probably won't because we're already in orbit . . . When the point reaches the vitals, the length of the shaft is not important."

During his excellent summary of the meeting, Charles Adams of C. W. Adams Associates labeled the oft-repeated desires for such concepts as extendability, modifiability, teachability, and self-applicability as important, but secondary objectives. Further, he felt that the conference had ignored important topics like documentation and modularity (not total nesting but pieces configured to the requirements of the user).

Among general criticisms leveled at the workshop were that nothing concrete came of it and that not enough users in the audience were heard from. If the intent of the gathering was to get a group like this to start talking to each other it was accomplished. More discussion of this kind, particularly on PL/I, is needed, many felt.

R. Zemlin of CDC suggested, but it was little discussed, that a nonprofit institute of people interested in the development of programming languages be formed. The group would meet on a continuing basis to discuss the fundamental objectives—"what are we trying to achieve, how are we going to get there, and with respect to particular language features, what does this contribute to the total objective and what price do we have to pay to get this particular feature." Perhaps it would conflict with other agencies, perhaps there are other drawbacks to such an institute, but it seemed to deserve more than a cursory glance. —ANGELINE PANTAGES

Why should programmers consider us?



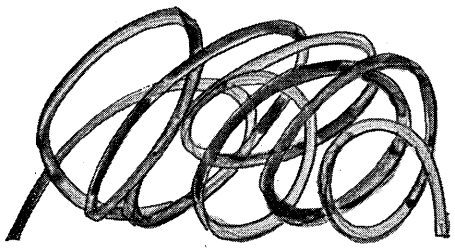
FOR BUSINESS REASONS—

There are positions currently open for all levels of programmers and EDP project planners with one or more years' experience, preferably utilizing IBM 1401 or 1410 equipment, although experience with other computers will be considered.

Xerox's 7010s are completely random access oriented utilizing 2302s and are being used to implement our total systems concept. This will require the systems programmer to be familiar with systems and procedures, production planning, inventory control, accounting and other related functions. Real time and operating systems experience helpful. Bachelor's degree required.

Moving Logic.

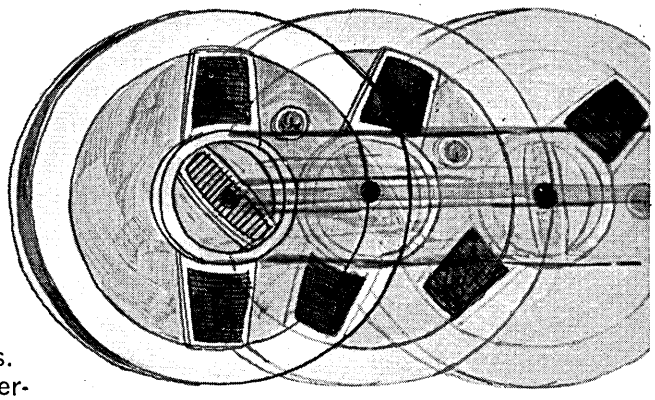
—because we're now installing a total management information system... and because we're growing rapidly in graphic communications, a direction with formidable implications all its own. New and possibly revolutionary information/imaging systems for business and industry are under study. No wonder programming has become more and more important to **us**... for business as well as technical reasons. Let us tell you more after we hear from you. Local interviews can be arranged.



FOR TECHNICAL REASONS—

Xerox's Scientific Computing Center has recently installed an IBM 7040 system. Opportunities exist for personnel desiring to develop Fundamental and Applied Research applications. Additional openings exist for personnel experienced in systems programming, PERT, operations research, and information storage and retrieval.

B.S. degree in Mathematics, Physics, or a technical discipline required. M.S. degree preferred. Must have a minimum of two years' experience in scientific or engineering applications programming. This should include at least one year's experience utilizing FORTRAN IV. Experience in symbolic programming highly desirable.



These positions are in Rochester, New York. Please forward resumes in confidence to Mr. David E. Chambers, Dept. DA-11, Xerox Corporation, P.O. Box 1540, Rochester, New York 14603.

XEROX

An Equal Opportunity Employer

Digital Computer Systems Designers, Analysts, Programmers:

Apply your experience to complex problems in the Navy's worldwide, multi-computer command and control network

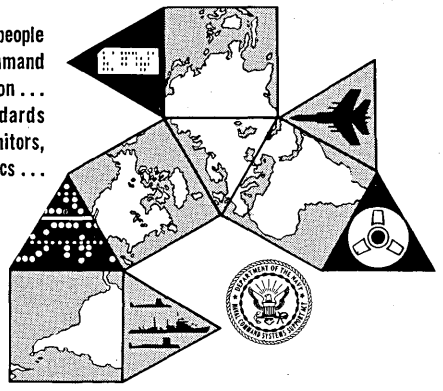
OPERATING DIRECTLY under the Chief of Naval Operations (and in support of the Secretary of Defense, Secretary of the Navy, Joint Chiefs of Staff, and other Major Commands), NAVCOSSACT—the Naval Command Systems Support Activity—has one of the most important and far-ranging missions ever assigned to any technological organization: **to design, develop and implement data processing systems for the Navy's worldwide multi-computer command and control network.**

WITH SEVERAL MAJOR ADP systems operating in Hawaii, Norfolk, and Washington, D. C., (and others underway or planned for San Francisco and London), the Department of Defense Computer Institute (DODCI) and the Navy Information Center (NAVIC)—both in different locations in the Nation's Capital—NAVCOSSACT applies systems analysis and advanced ADP technology to the solution of complex command and control problems.

NAVCOSSACT is now seeking experienced people for all its offices who can contribute to command and control progress in System Integration... Source Data Automation... ADP Standards Development... Operating Systems, Monitors, Executive & Utility Programs... Logistics... Operations... Intelligence... Simulation... Communications... Sea-Surveillance... Data Base Development.

CURRENT STARTING SALARIES are in the $10,000 to $13,000 range, with regular increases, and all the benefits of Career Civil Service. This is an excellent time to join NAVCOSSACT. Although a young (since 1961) organization, it has established its pre-eminence in the worldwide implementation of command and control systems. With the shakedown phase behind it, NAVCOSSACT knows where it is going in the years ahead... with the right kind of talent.

Interested candidates should forward resumes to: Technical Director (Code 44A), Naval Command Systems Support Activity, Washington Navy Yard, Washington, D. C., 20390... an Equal Opportunity Employer. You must be a U. S. citizen.



NAVCOSSACT

Naval Command Systems Support Activity
Navy Yard Annex
Washington, D. C., 20390

CIRCLE 104 ON READER CARD

COMPUTER ANALYSTS-PROGRAMMERS

Opportunities with growth potential exist in the following areas of application:

Design Automation

Management Information Systems

Engineering Data Systems

Reliability Information Systems

Generalized File Information Systems

Mechanized Technical Library Systems

Flight Mechanics

Thermo/Nuclear Dynamics

Trajectory and Orbit Simulation

New challenges await qualified applicants as the planned conversion from IBM 7094 to System 360 hardware begins.

Please send resume to
Mr. A. N. MacDonald

DOUGLAS

MISSILE & SPACE SYSTEMS DIVISION
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CIRCLE 208 ON READER CARD

GROWTH OPPORTUNITIES FOR COMPUTER-ORIENTED SPECIALISTS

WITH TRW SYSTEMS
in Los Angeles and Houston

GROWTH has been the by-word of TRW Systems (formerly TRW Space Technology Laboratories — STL) since its founding over a decade ago. Having established standards of TECHNICAL EXCELLENCE in aerospace and related fields, TRW has new and important OPPORTUNITIES for computer-oriented specialists.

AT TRW Systems in Redondo Beach, California and in Houston, Texas, specialists in scientific and business programing are invited to join our staff in advancing the application of computer technology to underwater defense systems, Gemini and Apollo mission planning and analysis, advanced ballistic missile studies, advanced space probes, Mars studies and space communications systems.

Vitally involved in the nation's major space programs, TRW Systems provides its personnel in scientific and business programing with two IBM 7094 systems. Installation of an advanced GE 635 system is scheduled for 1966.

We urge you to investigate these ground-floor opportunities NOW!

Computer Software Project Engineers

Background should include technical or business degree, scientific or information systems programing, leadership experience, and ability to direct the development of complex software projects.

Computer Programing Engineers

Requires technical degree and experience in analysis, programing and debugging of computer solutions of advanced engineering problems encountered in space and undersea research.

Scientific Programers

Experience in programing high speed digital computers. Will assist in solution of problems arising in missile and space vehicle engineering, with responsibility for analysis, programing and debugging of computer solutions. Requires BS or MS in Math, Physics or Engineering.

Test Evaluation Programers

BS or advanced degree in Math or the Physical Sciences, with programing experience on high speed digital computers, and experience with scientific test data. Responsibilities will include mathematical and computational aspects of physical problems, and the formulation and programing of test evaluation computer problems, employing data obtained from various test facilities and systems, including flight test telemetry.

Real-Time Programers

Software development for small or medium-size digital computers on real-time or near real-time applications. Prefer experience with real-time for handling instrumentation or telemetry data. BS in Engineering or Math preferred.

Systems Programers

Experienced in development and/or modification of control programs, i.e., supervisors, monitors, loaders, etc., for large-scale computing systems. Background in multiprocessors and multiprograming very desirable but not required.

Data Management Systems Programers

Design, develop and implement computer-supported management information/data processing systems for engineering data management, computer center administration, aerospace project management and government. BS/BA degree and two years' experience on large-scale computers required.

•

Please submit resume to G. O. Deshler, TRW Professional Placement, Dept. D-11, One Space Park, Redondo Beach, California 90278. TRW is an equal opportunity employer.

TRW SYSTEMS

ONE SPACE PARK, REDONDO BEACH, CALIFORNIA

Formerly TRW Space Technology Laboratories – STL

CIRCLE 106 ON READER CARD

OPPORTUNITIES FOR PROGRAMMERS in San Diego, California

Engineering and Scientific Programmers

Positions are available for engineering and scientific programmers with a minimum of a BS Degree and two years' experience in symbolic programming for large-scale digital computers. Assignments will involve engineering and scientific programming applications. In addition, programmers are needed to program a real-time tracking and navigation problem for the Apollo Instrumentation Ships project. The tasks include real-time program organization, multichannel input/output for peripheral equipment, utility and diagnostic routines, data simulation, and programs for analysis and synthesis of the tracking and navigation data. Equipment utilized is an IBM 7094-44 directly coupled system.

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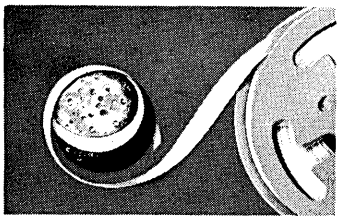

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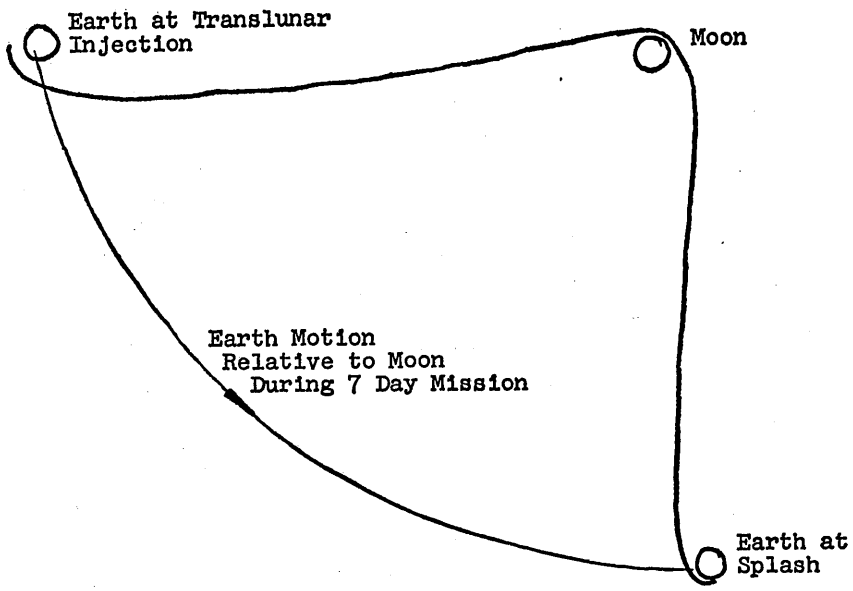

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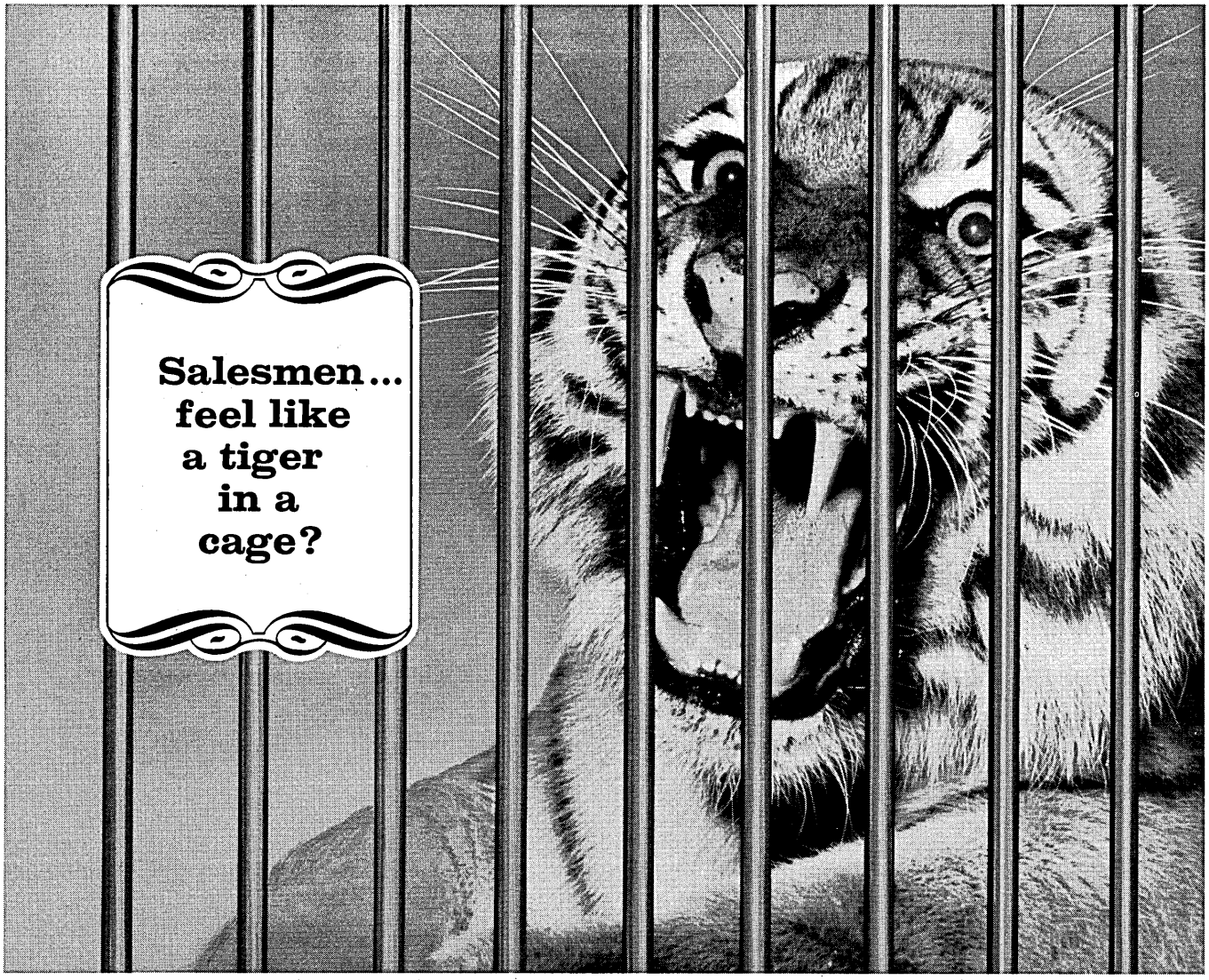

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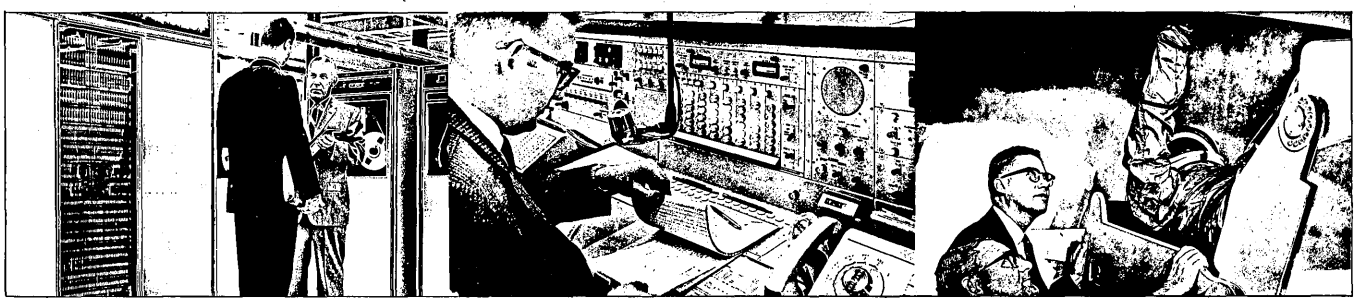

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BOOKS

Computers and Thought, edited by Edward A. Feigenbaum and Julian Feldman, McGraw-Hill, 1963.

Artificial intelligence and the simulation of human cognitive processes are the subjects for this stimulating collection of papers. The theme is set by the first sentence of the preface: "These research reports and discussions are concerned with the information processing activity that underlies intelligent behavior in human beings and computers." Both the introductions to Part 1, on artificial intelligence, and to Part 2, on the simulation of cognitive processes, emphasize that computers can do a great deal more than compute. Certain kinds of behavior are intelligent, the editors maintain, whether it is a man or a machine that is behaving. Artificial intelligence is the study of means to increase the range of intelligent behavior in machines; simulation of cognitive processes is the use of machines to help understand intelligent behavior in man. At least for the present, I believe it an act of faith to assert that a single set of principles will suffice for both purposes. It is also an act of faith to assert that a single set will not suffice, however, for the dividing line between artificial intelligence and simulation of cognitive processes is extremely hard to draw—as any reader of this anthology will see.

Leading off the collection is Turing's paper on "Computing Machinery and Intelligence." In it is introduced the imitation game. Either a computer and a woman or a man and a woman must answer questions put by an interrogator in another room. The interrogator must decide which is which (or who or what). Rather than ask, "Can machines think?" Turing asks whether a computer can be built and programmed to fool the interrogator as often as the man does. The new question helps make sense of the statement that machines can think, as well as the milder statement that some machine behavior can be called intelligent. I prefer not to talk that way myself, but Armer makes a telling point in his later chapter on attitudes toward intelligent machines: "To prove that machines *today* do *not* exhibit intelligence, it is only necessary to define a lower bound . . . which is above the behavior exhibited by the machines and then say that behavior above that bound is intelligent and below it is not intelligent. . . . Many who use this gambit have been redefining the lower bound so that it is continuously above what machines can do today" (pg. 396, author's italics).

Seventeen chapters separate the arguments by Turing and Armer. These, too, contribute their share of thought provoking material, but it is obvious that an additional selection criterion was to show what is done rather than said in the field. Game-playing programs are represented by Newell, Shaw, and Simon on chess and by Arthur Samuel on checkers. Theorem proving includes articles on the Newell-Shaw-Simon logic theory machine and Gelernter's geometry-theorem proving machine. Tonge's heuristic line balancing procedure and Slagle's heuristic program to solve integration problems in the elementary calculus show some applications of artificial intelligence methods. Question answering by machine is treated by Green and others with a chapter on baseball and by Lindsay with a chapter on parsing and understanding the meaning of English sentences that express kinship relations. Descriptions of the Selfridge-Neisser and Uhr-Vossler techniques for pattern recognition by machine close Part 1. The second part of the book maintains the strong empirical flavor. Newell and Simon discuss their general problem solver and compare its behavior with that of a human subject. Verbal learning is covered by Feigenbaum's EPAM (elementary perceiver and memorizer) program. Hunt and Hovland describe a computer model

for human concept formulation. Two chapters are devoted to decision making under uncertainty: Feldman's paradigm comes from the psychology laboratory and Clarkson's from the world of banking. Part 2 closes with a chapter by the Gullahorns, who describe a technique for simulating the social behavior of man.

Continuity of thought is maintained from one empirical chapter to the next despite the apparent diversity in subjects treated. Some of that continuity is brought about through carefully constructed introductions to each major part and section. Some of it is due to the similarity of presentation in the articles selected. Thus, all these chapters deal with real programs that have been constructed and run on real machines. All of them discuss the theoretical background for the problem treated, and all of them present specific techniques for interpreting the theory in a computer program. Most of them also describe the actual outputs obtained from running the programs. There is another basis for continuity, however, arising in a certain connectedness of concept and method. Although workers in the field may disagree violently on the answers, there is wide agreement as to what are the fundamental questions. These questions are treated thoroughly in the final expository chapter of the book. Minsky's "Steps Toward Artificial Intelligence" remains the outstanding summary and critique of the field, and it serves as a capstone for the material preceding it.

Probably no one is satisfied with the specific selections that find their way into a particular anthology. In this case, I believe the book falls short of being a self-contained introduction to the field because of a single omission—Hao Wang's 1960 paper on mechanical mathematics in the *IBM Journal of Research and Development*. It is cited often enough in the papers that are included that no careful reader should be satisfied without firsthand exposure to Wang's presentation. Any other lacks are compensated for by the inclusion of an updated version of Minsky's descriptor-indexed bibliography, an invaluable guide to the literature on artificial intelligence and closely related areas. In scanning that bibliography for other omissions, it becomes clear that the editors have succeeded remarkably well in sampling the work from a young and vigorous experimental discipline.

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By DICK CALDWELL
Minneapolis Star Staff Writer

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ELECTRONIC NEWS

Control Data Buying Howard

MINNEAPOLIS.—Control Data Corp. here has reached an agreement to acquire assets and business of Howard Research Corp., Arlington, Va., electronic systems engineering company.

The acquisition, subject to approval of Howard's stockholders, will be in exchange for shares of Control Data common stock, the amount was not disclosed.

Howard Research, which specializes in underwater systems, missile systems and information systems, will become a part of Control Data's Government Systems division, headquartered in Minneapolis. Howard will remain in Arlington.

William C. Norris, president of Control Data, said his firm's acquisition of Howard will further expand Control Data's total systems capabilities in electronic military and weapons systems programs.

Howard Research will continue to be operated under that name as a part of the Control Data's Government Systems division. James H. Howard, president of Howard Research, will join Control Data in a position not yet disclosed.

BUSINESS WEEK

Computers speed up

Control Data's 6800 model is the largest, swiftest electronic brain yet

Living up to expectations, Control Data Corp. has wrested back from International Business Machines Corp. the title for the biggest, fastest, most powerful computer.

This week, the Minneapolis company announced it has added the 6800 model to the top of its line. The 6800 operates at speeds four times those of the company's 6600, which held the title for size before IBM expanded its System 360 line with the model 92 last August. Control Data also came out with a model 6400. As the numbering suggests, this is smaller than the 6600.

WALL STREET JOURNAL

Control Data Unveils Two 'Super' Computers For High-Speed Service

One Model Will Execute 1 Million Instructions in a Second, and The Other, 12 Million a Second

By a Wall Street Journal Staff Reporter

MINNEAPOLIS—Control Data Corp. has strengthened the heavy end of its computer line with the introduction of two "super-scale" machines—the 6400 and the 6800 models.

The 6000 series, including the previously announced 6600 computer, gives Control Data one of the most extensive lines of super computers of any company in the electronics industry.

Last August, International Business Ma... chines Corp. introduced the model 92 to its ... to Control Data's 6600 com... the fastest

FORBES

Control Data: Big Success,

Brilliant engineering and managerial boldn... Control Data to the third spot in com... second spot in profits. But Bill Norris ca...

...ARDLY THREE YEARS ago the ...nancial pages were awash with ...entific-sounding names of brand-...w little companies. In most cases ...y consisted of little more than a ... Ph.D.s working in rented loft ...e on a bit of a Pentagon subcon-... It didn't matter. Investors bid ...heir prices. But since the collapse ...e new-issue boom in early 1962, ...s have gone out of business and ... was only four years old, and in name hardly distinguishable from scores of other new science companies.

Control Data, however, was the one in a thousand that had what it takes. It was founded in 1957 by Chairman and President William C. Norris, who had recently quit as general manager of Sperry Rand's Univac division. Norris' whole staff consisted of a half-dozen fellow Univac refugees. To... later became part of Univac. ... in their late thirties and early forties, this team is among the most experienced in the young computer field.

But Norris is oversimplifying when he attributes CD's success entirely to "brains." Control's technical people produce fine equipment. But so do the top technical people of rival companies. What has made a good deal ... of differ...

Good news travels fast... Find out how you can join the Control Data Success Team that's making the news

There's a lot of good news going around about Control Data – new products and systems making headlines, sales increasing year after year, and *GROWTH* born of bold management, frequent technological advances, and effective selling. Along with this growth we've created excellent opportunities for the kind of people that have made Control Data the most dynamic force in the computer field.

If you'd like to be a member of one of industry's fastest growing teams and have a share in its success, get the details on positions that are now available. Check the opportunities listed here, then contact us for more information on these and other positions.

PRODUCT MANAGEMENT: Openings in advanced planning require a technical degree and a minimum of two years experience in technical market requirements, programming systems design, systems organization, management information systems, or time sharing systems. Keen interest in computer advances and management communication ability desirable. St. Paul location.

SYSTEMS AND PROCEDURES ANALYSTS: Rapid internal acceleration of data processing techniques requires the need for imaginative, random-access-oriented data processing personnel. A degree and two years' experience are necessary. Engineering, mathematical or manufacturing background is required. Minneapolis location.

SOFTWARE DOCUMENTATION: Assist in the development of reference manuals, sales aids and other forms of documentation on programming systems. Should have three years' programming experience and working knowledge of time-sharing systems, monitors, assemblers, NPL, FORTRAN, COBOL and/or ALGOL. Must have a strong interest in writing and editing. Minneapolis, Los Angeles locations.

SYSTEMS PROGRAMMER ANALYSTS: New application areas for high-speed digital computers and programming systems. Positions require varied backgrounds in command and control, real time, monitor systems and knowledge of scientific programming languages. A degree in math, physics or engineering and a minimum of three years' experience are required. Los Angeles location.

PROGRAMMER ANALYSTS – INDUSTRIAL: Responsibilities include analysis, synthesis, and implementation of real-time communications systems. Experience is desired in assembly language programming, software development, real-time applications, and systems programming in the communications area. Other positions exist in on-line data collection, terminal recordings, and message and data switching. Minneapolis location.

PROGRAMMER ANALYSTS: Analyze Data Center Customer problems for customer's computer applications. Responsibilities also entail work in sales support and the preparation of programming proposals. Experience on large-scale machines in either commercial or scientific programming is necessary. Commercial applications background should include payroll, A/R, A/P, inventory control, school scheduling, etc. Los Angeles, Palo Alto, Washington, D. C., Minneapolis, Houston, Long Island locations.

At the Fall Joint Computer Conference in Las Vegas November 30-December 2, call M. E. Hawkins, (702) 735-1122 for information on other opportunities.

Rush resume now for West Coast or Las Vegas Interviews.

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CIRCLE 204 ON READER CARD

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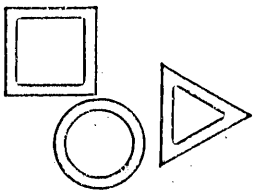


THE FORUM

Starting with this issue, the editors are presenting a new feature, The Forum. Its purpose is to offer timely and perhaps controversial discussions of current concepts, techniques, and events related to information processing. As with standard articles, manuscripts will be selected on the basis of "having something to say," rather than by experience or reputation. Your contributions are invited.

YES, GENERAL, THERE IS A MAX PALEVSKY

PL/1 versus COBOL. FORTRAN versus ALGOL. GECOS versus IBSYS. Liberator versus 1401. IBM versus National Physics Laboratories. The present swirl of controversy and confusion over software in general and programming languages in particular evokes the thought from Matthew Arnold that "we are here as on a darkling plain, swept with confused alarms of struggle and flight." Where programming systems clash by night.

About the only thing that most people concerned with software care to prognosticate with much confidence these days is that we'll all probably have to endure a great deal more of it before we're through. RCA's David Sarnoff, in his Tower of Babel address to last year's fall joint, noted with understandable dismay that "there are, by conservative count, more than 1,000 programming languages. And there are languages within languages — in one instance, 26 dialects, and in another, 35 dialects."[1] 'Tis indeed confusing, sir, if not downright infuriating. And beyond a consensus that there needs to be much greater emphasis on standards, which was the burden of General Sarnoff's polemic, there have been few cogent — or even uncogent — proposals for extricating the industry from this self-created quagmire.

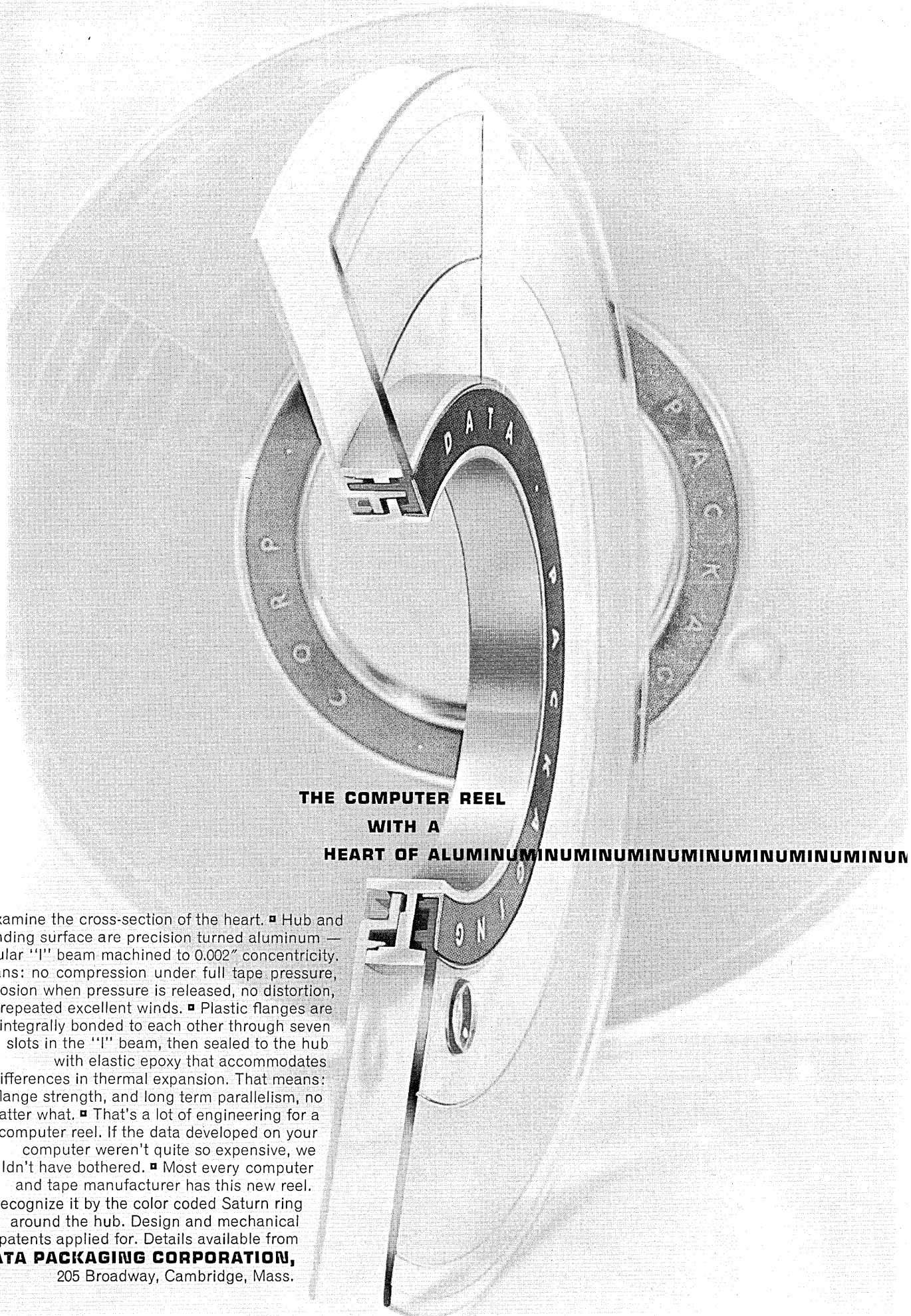
Until just recently. When along came Max. Max Palevsky, that is, who in a speech before a TIMS-ORSA joint meeting inferentially indicated an exciting new possibility for coping with the software proliferation: ignore it.[2] Mr. Palevsky talked of many things in his little-publicized discourse, but his most stimulating commentary had to do with the trend toward ever-decreasing costs in the engineering and manufacturing of computers. In reflecting upon this trend, Mr. Palevsky conjured up a future vision of machines so low in cost that they could be custom tailored to the requirements of a particular user. Special purpose computers, I suppose you'd have to call them. And although the president of Scientific Data Systems didn't come right out and say so, maybe these special purpose machines won't need to house a stored program at all. Or, failing in the attempt to rid ourselves of programs entirely, we can at least relegate many of their functions to the hardware.

I don't know whether Max Palevsky happens to know Howard Aiken but, if not, somebody should introduce them, as they offer some fascinatingly complementary ideas. One of the pursuits with which Dr. Aiken has been occupying his time since retiring from Harvard's computation center is in doing programming research for the Air Force. He and his research team colleagues came up not long ago with something they call the Theta language which, besides raising General Sarnoff's count beyond 1,001, suggests some interesting new dimensions for programming methodology.[3]

The Theta language, or ideal digital language (IDL) as it is also called, endeavors to be "precise, succinct, universal, minimal, expansible, deductive, and logically consistent." And as if all that weren't enough, it also strives to be machine independent; however, *machine design should depend upon the language* [italics supplied]. Thus, presumably one should be able to take Dr. Aiken's Theta language and get Scientific Data Systems to build a computer that would accept it directly without benefit of compilers, interpreters, simulators or other software encumbrances. And if Mr. Palevsky is able to do *that*, then maybe he can produce other machines to handle a goodly number of the remaining languages that General Sarnoff and the rest of us are so concerned about.

—ROBERT V. HEAD

[1] David Sarnoff, "The Promise and Challenge of the Computer," address to the Fall Joint Computer Conference, San Francisco, October 27, 1964.
[2] Max Palevsky, "Tomorrow's Data Processing and Computers: The Expected and the Unexpected," address to the Joint Western Regional Meeting of TIMS/ORSA, Los Angeles, April 30, 1965.
[3] "A New Approach to Computer Command Structures," Technical Documentary Report No. RADC-TDR-63-135, Rome Air Development Center, May 1964.



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