A MORGAN-GRAMPIAN PUBLICATION

# DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

APRIL 1985

## PROGRAMMABLE LOGIC TAKES EXPANDING APPLICATION-SPECIFIC IC ROLE







- ARTIFICIAL INTELLIGENCE AND THE FIFTH GENERATION
- EFFECTIVE COMMUNICATION ELUDES DESIGN ENVIRONMENT NETWORKS
- DEC COMPATIBILITY
- PLOTTERS
- SOLID MODELING

# We run with a great crowd.

## Complete hardware/software compatibility.

Talk about easy interfacing. You can take a ZETA 824 or ZETA 836 plotter and plug it into virtually any computer made.

What's more, you'll be ready to run because our plotters understand a variety of computer protocols. Select the model for your application then just plug in and plot.

In fact, we're a plug compatible replacement for many plotters from HP, CalComp and Tektronix. Some models of our plotter can even run directly from your IBM cluster controller. Now that's easy interfacing.

When it comes to your favorite application packages, you'll be on safe ground too. Packages such as CADAM, TechniCAD, Euclid, P-CAD, AutoCAD and many more.

### *The most productive plotter for the money.*

You'll be getting the highest output plotters for the money with our new ZETA 824CS and ZETA 836CS. More finished plots. More productivity. Plus, these "D" and "E" format plotters let you run either single sheet or roll media.

IBM
PRIME
SAS
digital™
Tektronix
ISSCO GRAPHICS
p-cad
Precision Visuals
hp


### *Easy-to-use touch controls.*

Your time is valuable. So we've made our touch controls simple – yet powerful. Set speed, pen pressure, liquid ink parameters, electronic limit sensing, windowing, scaling – all at the touch of a finger. Self-test and diagnostic plots too. Let us show you dozens of other time-saving operations in a brief demonstration.

### *Plotter specialists.*

We've been designing hardware interfaces, plotting language emulators and high performance pen plotters for over 14 years. Nicolet also provides you with worldwide sales and service support.

Give us a call. See how easy it is to join the crowd.

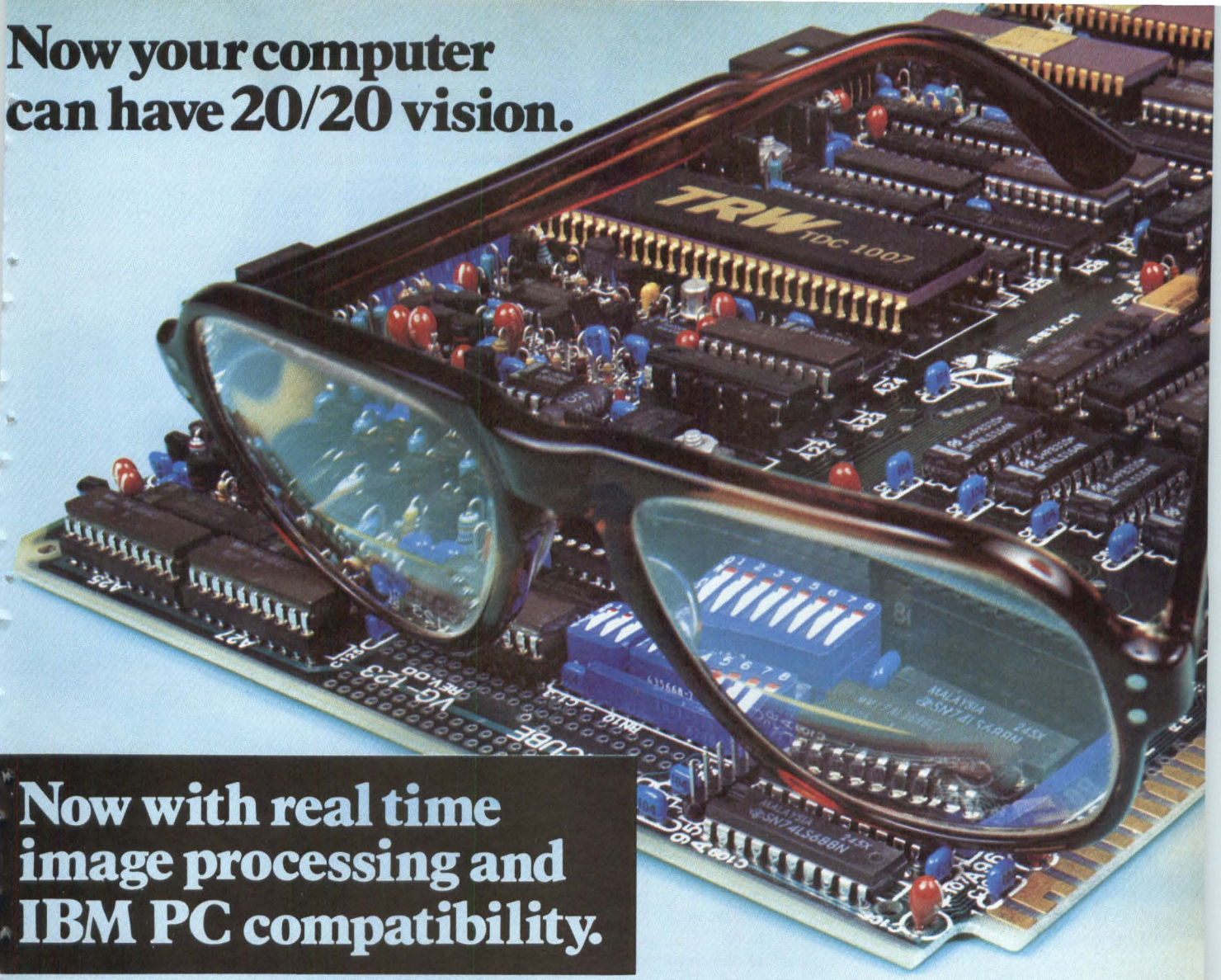
*Call (415) 372-7568.*
*Nicolet Computer Graphics Division, 777 Arnold Drive, Martinez, CA 94553*
*TWX 910-481-5951*

**Circle 23 on Reader Inquiry Card**

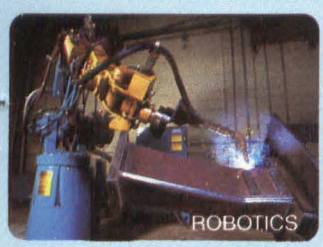
**Nicolet**
*Computer Graphics Division*

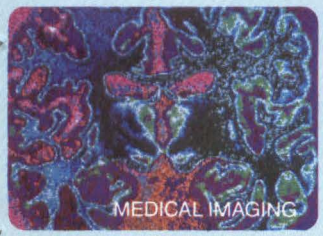
CADAM is a trademark of CADAM, Inc.
TechniCAD is a trademark of Tektronix, Inc.
Euclid is a trademark of MATRA DATAVISION, Inc.
P-CAD is a trademark of Personal CAD Systems.
AutoCAD is a trademark of Autodesk, Inc.

# Now your computer can have 20/20 vision.




## Now with real time image processing and IBM PC compatibility.





Datacube continues to be the single source leader in image processing and graphics for your Multibus, Q-Bus, and now IBM PC's. Solutions are available from single boards to fully integrated systems.

Resolutions range from 320H x 240V to 1400H x 1100V with pixel depths from 1 to 24 bits.

The new SP-123 offers advanced signal processing of high resolution black & white or full color images at the rate of 14 megapixels per second.

The new IVG-128 is a complete video acquisition and display module on a single IBM PC compatible card. It features input & output look up tables, an 8-bit digitizer, and RGB 8-bit outputs.

The new DC-1000 and DC-1500 systems are complete workstations capable of video acquisition and image processing.

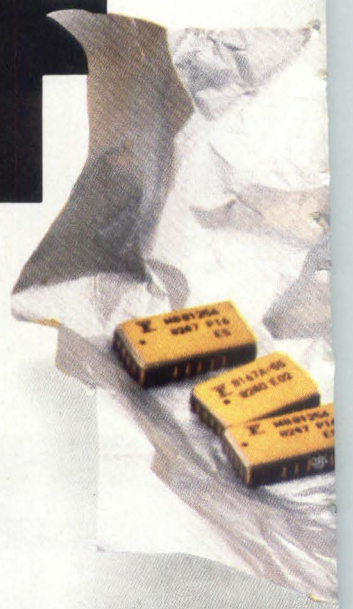
Datacube products provide reliable vision and real time image processing for robotics, medical imaging, surveillance, inspection, teleconferencing, animation, etc. And at surprisingly low prices.

Call or write for our new Product Guide of Multibus, Q-Bus, and IBM PC compatible boards and systems. Datacube Incorporated,
4 Dearborn Road,
Peabody, MA 01960,
Telephone: (617) 535-6644.
Western Sales Office:
Telephone: (408) 737-9978.

**Datacube**

Circle 4 on Reader Inquiry Card

# CHOCK FULL OF CHIPS.



We've long been recognized for our tasty technology. But not many know us for our tempting selection.

Fact is, no one offers a more complete line of integrated circuits than Fujitsu: memories, microprocessors, microcontrollers, floppy disk controllers, LAN chip sets, codecs, flash converters, application specific ICs and more.

And while others make promises, we deliver. Now. In production quantities.

**DRAMs.** In MOS memories, we were the first to consistently ship production quantities of 16K, 64K and 256K DRAMs. With features that make your mouth water. Like our MB81256/MB81257 256K with both the smallest die size in the industry and the fastest address access time: 100 ns.

**High-speed bipolar memories.** We serve up PROMs in sizes from 256 to 64K bits. All made according to our unique DEAP™ recipe for high reliability.

**ECL RAMs.** Fully compatible with the industry-standard 10K and 100K series families. In densities from 1K bits at 7 ns to 16K bits at 15 ns. All available now. With a 16K at 10 ns version later this year.

**Static RAMs.** All the industry-standard high- and low-speed parts – from 35 ns to 150 ns address access times. In your choice of organizations and densities, from 4K to 64K bits.

**EPROMs.** We'll more than satisfy your appetite, from 64K to 256K. And 512K coming soon. In a choice of two flavors: CMOS and NMOS.

**Microprocessors.** We serve up a mouth-watering selection. Starting with our proprietary 4-bit microcontrollers offering the best value by function. And continuing with a complete line of Intel-compatible (second source licensed) 8- and 16-bit microcontrollers, microprocessors and their peripherals.

Complemented by a choice of many Fujitsu-designed VLSI circuits. Including the industry's first Ethernet™ chip set, high-performance digital signal processor, disk and video/graphics controllers, and later this year – MBL80186 and MBL80286 microprocessors.

**Gate Arrays.** We supply more of the world's gate array requirements than any other manufacturer. With CMOS arrays in densities from 440 to 8000 gates. And bipolar arrays from 240 to 2000 gates. All supported by one of today's most sophisticated and prolific design systems, with well over 3000 designs already produced.

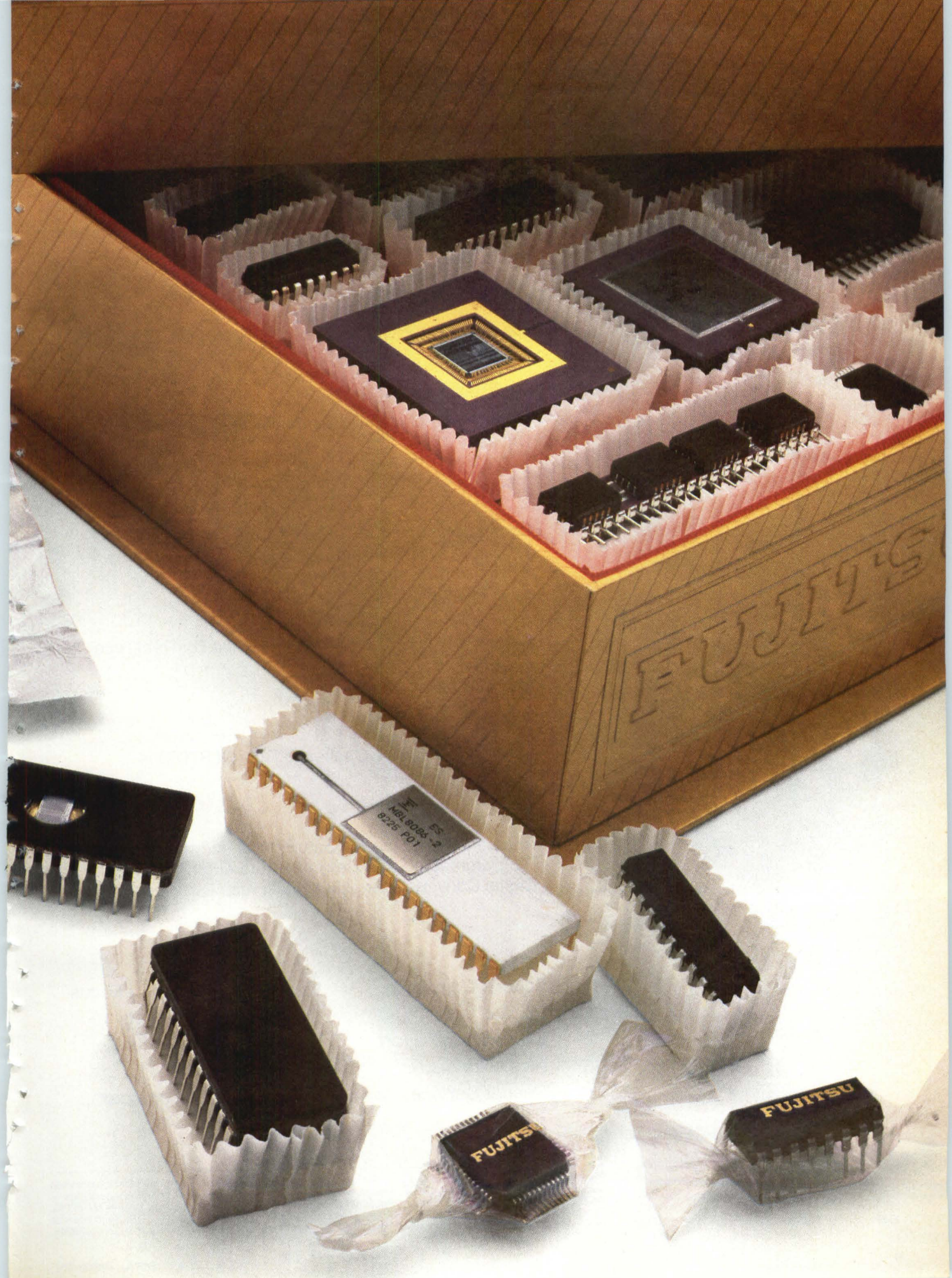
**Packaging.** Wrap it up any way you want. We offer the most comprehensive selection. From standard plastic DIP to LCC. PLCC to Cerdip. SIP to flat pack. And skinny DIP to high-pin-count grid arrays.

That's why, the next time you hunger for a part – any part – call Fujitsu first.

We'll satisfy your appetite.

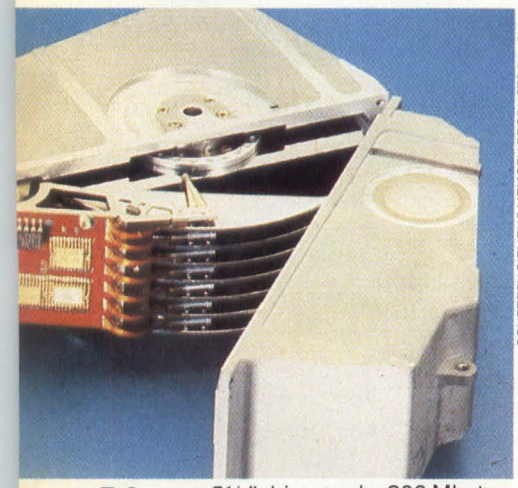
**FUJITSU**
**MICROELECTRONICS, INC.**

**Integrated Circuits Division**
3320 Scott Boulevard
Santa Clara, CA 95054-3197
(408) 727-1700


FUJITSU
FUJITSU
FUJITSU

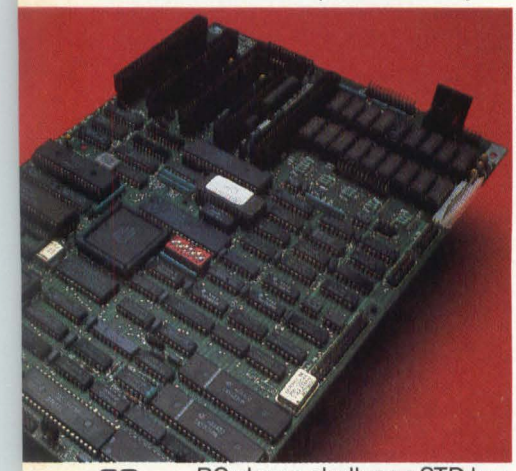
# DIGITAL DESIGN

APRIL 1985 □ VOL. 15 NO. 4

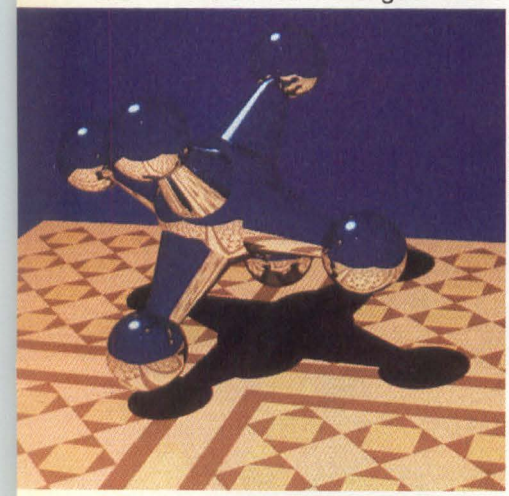
COURTESY SIEMENS MEMORY PRODUCTS DIVISION

**24** 5¼" drive packs 306 Mbytes



COURTESY MOSTRON

**30** PC clones challenge STD bus



COURTESY GRAY LORIG AND RPI

**56** Advances in solid modeling

## TECHNOLOGY TRENDS



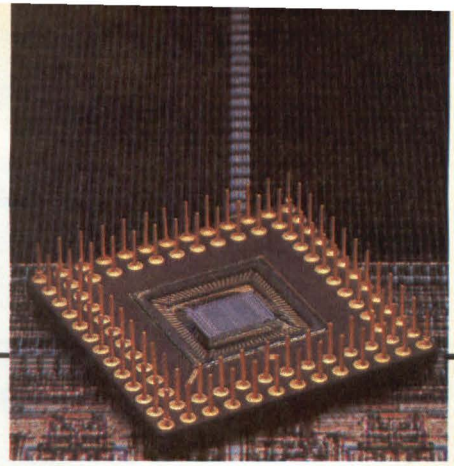

Published monthly thirteen times a year with two issues in November. Subscription rates for non-qualified subscribers (US and Canada) — $40/yr; foreign — surface mail — $50/yr; airmail — $85/yr. Single copies — $4.



Second class postage paid at Boston, MA and at additional mailing offices. POSTMASTER: Send address changes to Morgan-Grampian Publishing Company, Berkshire Common, Pittsfield, MA 01201 ISSN 0147-9245.

# TABLE OF CONTENTS

**42**
**Advances in programmable logic** and development tools combine to provide designers with a viable alternative to gate arrays.



COURTESY MONOLITHIC MEMORIES

## FEATURES



## ON THE COVER

Recent advances in programmable logic, including programmable macrocells, CMOS, and non-destructive programming, are breathing new life into this ten year old technology. Chips such as Advanced Micro Devices' AmPAL22V10, shown on this month's front cover, represent the trend toward increased functionality and higher speeds. In addition, new development tools for programmable logic permit designers to use schematic capture tools as opposed to Boolean equations to program the logic. Photo courtesy AMD.

# FORCE COMPUTERS
# System 68000 VMEbus

## Single board solutions for 16/32 bit "open systems" in industrial, business, and scientific environments

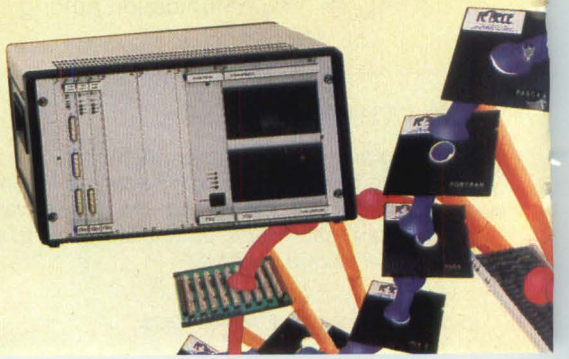
If your application requires advanced technology available in production quantities if quality, reliability, and price/performance ratio are the major criteria for supplier selection – then compare our product portfolio with other alternatives.

- Three CPU's for most applications from intelligent I/O controllers to multiuser/ multitasking environments with powerful UNIX* or real time operating software PDOS* and up to 1M byte of on-board memory: CPU-1B, CPU-2, CPU-3.
- Two DRAM Boards: 512KB and 2MB; two SRAM Boards: 128KB and 512KB. RAM/ROM Board: 512KB (max.); DRAM-1, DRAM-2, SRAM-1/2, RR-1/S/E
- Mass memory interface boards with either direct control of up to seven drives (WFC-1) or intelligent VMEbus interface to SASIbus with DMAC (SASI-1).
- Six-channel serial I/O board with Multi-Protocol-Communications-Controller (SIO-1).
- 32-channel parallel I/O boards either optically isolated (1000V) with DMAC (OPIO-1) or TTL-level with 64 mA drive capability signals (PIO-1).
- Intelligent high resolution graphics subsystem (master/slave) with resolution of 1024 x 1024 pixels and up to 12 bits of pixel depth. Powerful graphics operation through local 68000 MPU in parallel with 7220 graphics controller(s) GDC-1M/1S.
- Winchester/Floppy drive modules with up to 80 M bytes: WFMOD-20/80.
- Auxiliaries: Backplanes, chassis, power supplies.
- A variety of Software Products, e. g.:
  PDOS* – Real-Time, Multi-Tasking, with Basic interpreter, Pascal, Fortran 77, and C Compilers.
  COHERENT* – UNIX* V.7 compatible with C Compiler, Pascal and Fortran 77 in preparation.
- UNIX* – System V, Multi-User, Multi-Tasking.
- In development: memory boards with byte parity and 32 bit addressing; dedicated LAN-Controller; high performance communication I/O.

Supported by a worldwide network of distributors and representatives, FORCE Computers is recognized by its customers (and competitors) as the leading supplier of 68000/VMEbus board products.

*PDOS is a trademark of Eyring Research, COHERENT is a trademark of Mark Williams Co., UNIX is a trademark of AT&T.

**Consider, compare, and contact:** FORCE COMPUTERS, INC.




FORCE COMPUTERS®

FORCE COMPUTERS INC.
2041 Mission College Blvd.
Santa Clara, CA 95054
Phone (408) 988-8686
Tlx 172465
Telefax 408 980 93 31

FORCE COMPUTERS GmbH
Daimlerstraße 9
D-8012 Ottobrunn/München
Tel. (089) 609 20 33
Tlx 524 190 forc-d
Telefax (089) 609 77 93

**Circle 58 on Reader Inquiry Card**

## TELL US YOUR THOUGHTS

***Digital Design* is your forum—your inputs help keep the magazine interesting and vital to the design community.** So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design*, the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design*. Have your say in *your* magazine! Send letters and comments to: Editor, *Digital Design*, 1050 Commonwealth Ave., Boston, MA 02215.


# DIGITAL DESIGN

| | |
|---|---|
| **Publisher** | James R. DiFilippo |
| **Editor in Chief** | John Bond |
| **Executive Editor** | Dave Wilson |
| **Managing Editor** | Debra A. Lambert |
| **Senior Editor** | Julie Pingry |
| **Senior Technical Editor** | Ronald E. Collett |
| **West Coast Technical Editor (408) 356-0405** | Gregory MacNicol |
| **West Coast Technical Editor (408) 356-0405** | Joe Aseo |
| **Technical Editor** | Brita Meng |
| **Copy Editors** | Sherri Mack<br>Winnie Jenkins Rubino |
| **New Products Editor** | Terri Lamneck |
| **Washington Correspondent** | Anne Armstrong |
| **Production Director** | Paul Dadarria |
| **Art Director** | Maureen Bernardini |
| **Senior Designer** | Joyce Croker |
| **Advertising Production Manager** | Martha Watjen |
| **Graphics: Supervisor** | William Manning Jr. |
| **Sr. Technician** | Don Schaaf |
| **Jr. Technician** | Paul Christo |
| **Marketing Director** | Charlotte King |
| **Promotion Manager** | Elaine Bull |
| **Marketing Assistant** | Sharon Lembo |
| **Research** | Carolyn Wulfsberg, Peter Micheli |
| **Circulation Director** | Hugh J. Dowling |
| **Circulation Supervisor** | Maggie Hayes-Miville |
| **Circulation Staff** | Miriam Hlister, Betty Papa |
| **Reader Service (413) 499-2550** | Rose Wetherell |
| **Direct Mail** | Deborah Goldstein |
| **Executive Administrator** | Suzanne Levecque |
| **General Administration** | Nancy Deveau<br>Deanna Richardson<br>Debra James<br>Karen Bowman |

**President**
Ronald W. Evans


## Advertising Sales


**Northeast:** Terry L. Willins (In MA) **(617) 232-5470,** (Outside MA) **(800) 223-7126,** 1050 Commonwealth Avenue, Boston, MA 02215

**Middle Atlantic/Southeast:** Jane Archbold (In MA) **(617) 232-5470,** (Outside MA) **800-223-7126,** 1050 Commonwealth Avenue, Boston, MA 02215.

**Midwest, South Central:** Hank Bean, Rob Robinson **(312) 794-1515,** Edens East Office Center, 6200 N. Hiawatha, Suite 215, Chicago, IL 60646

**Northwest:** Carole Sacino, **(408) 356-0405,** 15951 Los Gatos Blvd., Suite 7, Los Gatos, CA 95030

**Southwest:** Mike Prewitt, **(714) 851-8550,** 2041 Business Center Dr., Suite 206, Irvine, CA 92715

**National Postcard Sales:** Jon Binder **(617) 232-5470,** 1050 Commonwealth Avenue, Boston, MA 02215

# Sell someone a Genicom 3000, and it may be some time before you hear from them again.

## Genicom 3000 printer reliability can keep a customer happy for years.

From offices to factories across the country—hour after hour, day after day—Genicom 3000 printers have been proving their quality and reliability under even the toughest conditions for years.

The result has been a large number of very satisfied customers, which means a large number of satisfied OEM's. But durability is only part of the Genicom 3000 printer advantage.

The Genicom 3000 family of printers offers multi-model flexibility combined with single design simplicity to give OEM's real dollar savings with price/performance matching for every customer. Parts commonality. Easier servicing. Single source supply. Plus you can select speeds from 180-500 cps draft/EDP, 45-100 cps NLQ, single or multi-mode printing, automatic sheet feeders, document inserters, multi-color printing and graphics, plus more. There's such a diversity of models, features and options, you can choose just the right printer and you don't have to pay for things you don't need.

See how long you can keep your customers satisfied...with the long lasting, field proven printers that have earned the respect of OEM's nationwide—the Genicom 3000 family.

GENICOM™

**The New Printer Company.**

**Genicom Corporation,** One General Electric Drive, Waynesboro, VA 22980 In Virginia, call 1-703-949-1170

For the solution to your printing needs call

TOLL FREE 1-800-437-7468

**Circle 57 on Reader Inquiry Card**

**DIGITAL DESIGN**
SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

**EDITORIAL AND SALES OFFICES**
DIGITAL DESIGN, 1050 Commonwealth Avenue, Boston, MA 02215, Telephone: (617) 232-5470

MORGAN-GRAMPIAN

**CORPORATE HEADQUARTERS**

Morgan-Grampian Publishing Company, 1050 Commonwealth Avenue, Boston, MA 02215, (617) 232-5470. Brian Rowbotham, Chairman; Ronald W. Evans, President; Charles Benz, Vice President.

**EXPOSITIONS GROUP**

Morgan-Grampian Expositions Group, 1050 Commonwealth Avenue, Boston, MA 02215 (617) 232-EXPO.
The following is a list of conferences produced by the Expositions Group:

ATE West
CADCON West
ATE Northwest
ATE East
CADCON East
ATE Central
CADCON Central

In addition to DIGITAL DESIGN, Morgan-Grampian publishes the following in the United States: Circuits Manufacturing • Electronic Imaging • Electronics Test • Computer & Electronics Marketing

Morgan-Grampian also publishes the following in the United Kingdom: Electronic Engineering • Control & Instrumentation • Electronics Times • What's New in Electronics • What's New in Computing • Business Computing and Communications • Communications Systems Worldwide.

DIGITAL DESIGN serves the manufacturers of computer-related OEM products. This includes primary computer and systems manufacturers, systems integrators, components and peripheral manufacturers, integrating OEM's and commercial end users. These companies manufacture products used to control machinery, equipment and information in manufacturing, material processing, machine tools, packaging, health care, defense, data processing, communications, instrumentation, and scientific and business operations.

ABP BPA

**SUBSCRIPTION POLICY**

DIGITAL DESIGN is circulated only to qualified research, development and design engineers and engineering managers primarily responsible for computer products and systems in OEM plants. To obtain a complimentary subscription, request (on company letterhead) a qualification card from Circulation Director. For change of address, attach old address label from recent issue to new company letterhead or note. Send this plus request for new qualification card to:

Circulation Department, **DIGITAL DESIGN**, Berkshire Common, Pittsfield, MA 01201

**Subscription rates:** non-qualified subscribers (US and Canada) — $40/yr; foreign — surface mail — $50; air mail — $85. Single copies — $4.




DIGITAL DESIGN solicits editorial material and articles from engineers and scientists. Contributors should submit duplicate manuscripts typed with two spaces between lines. All illustrations should be clear; components on all schematics and line drawings should be labeled. The editors assume no responsibility for the safety or return of any unsolicited manuscripts.

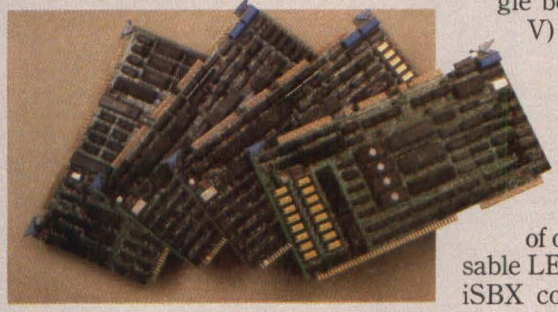
# FOR THE MICROCOMPUTER OEM OR END-USER HEURIKON IS THE CHOICE

Make Heurikon your choice for Multibus™ microcomputers and system components.

For 12 years, Heurikon has supplied thousands of computers to help its customers find economical solutions for their microcomputer applications.

## 8-BIT MICROCOMPUTERS

**MLZ-90A** single board microcomputer with nine byte-wide memory sockets for use with RAM or ROM (AM9511 and floppy disk drive controller optional).

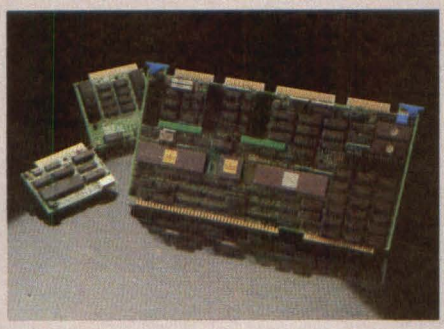


**MLZ-91A** single board CP/M™ system with on-card floppy disk drive controller, winchester interface, optional AM9511, streamer tape interface, two serial ports, one parallel port, 64K or 128K bytes RAM with parity, two EPROM sockets, and GPIB CONTROLLER.

**MLZ-92A** single board CP/M™ system with four serial ports on-card, floppy disk drive controller, winchester interface, optional AM9511, Centronics printer interface, 64K or 128K bytes of RAM with parity, and two EPROM sockets.

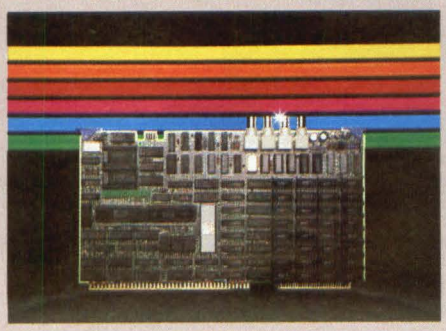
**MLZ-93A** single board CP/M™ system with 128K bytes of dual ported RAM, four EPROM sockets, floppy disk drive controller, optional AM9511 and powerful serial port features including SDLC and HDLC protocol support and modem controls.

## 16-BIT MICROCOMPUTERS



**HK68™** powerful and versatile single board UNIX™ (System III or V) or CP/M-68K™ system with 68000/68010 CPU (8Mhz or 10Mhz), MMU, quad channel DMA, four serial ports, 128K, 256K, 512K or 1M bytes of on-board RAM with parity, up to 128K bytes of on-board EPROM, user accessable LEDs and dip switches, and two iSBX connectors for I/O expansion. Heurikon can also supply a full line of iSBX I/O expansion modules including quad channel serial port module, floppy disk controller, A/D converter, bubble memory and many more.

## GRAPHICS CONTROLLERS



**MLZ-VDC** intelligent 640 x 480 x 4 color graphics controller based on the NEC 7220 controller chip with on-board Z-80 CPU, DMA controller, and user definable FIFO interface to Multibus™. Users may display up to 16 colors from a 4K palette. Up to 1024 x 1024 x 3 interlaced also available.

## MICROCOMPUTER SYSTEMS


MINIBOX

Heurikon also provides completely integrated UNIX™ development systems with UNIX™ System III or System V including Berkeley enhancements. CP/M-68K™, PolyFORTH™, Regulus™, and VRTX™ (real time operating system kernel) are also available.

Heurikon UNIX™ systems are available in four, six, and fourteen slot enclosures with 30MB, 65MB, 140MB or 280MB of winchester storage, a megabyte floppy, and optional *interactive* on-line streamer tape drive supporting 1-16 users.

HEURIKON CORP

Microcomputers For Industry

3201 Latham Dr.
Madison, WI 53713
Telex 469532

Z-80 is a trademark of Zilog Corp. Multibus and iSBX are trademarks of Intel Corp. UNIX is a trademark of Bell Lab. CP/M 68000 and CP/M-80 are trademarks of Digital Research. HK68 is a trademark of Heurikon Corp. Regulus is a trademark of Alcyon. VRTX is a trademark of Hunter & Ready. PolyFORTH is a trademark of FORTH, Inc.

Call Heurikon Direct

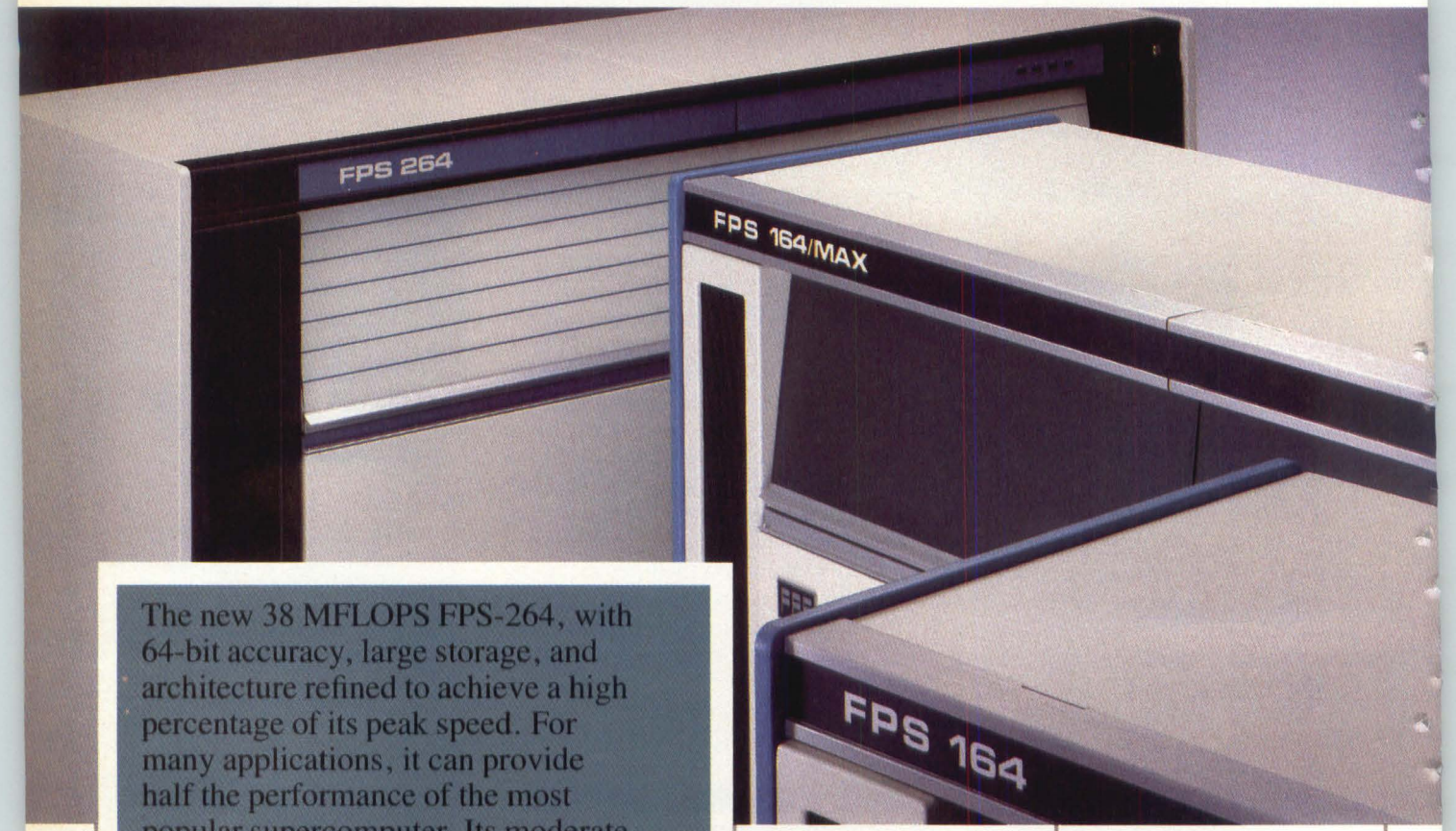
**1 800 356•9602**

In Wisconsin 1 608 271•8700

See Us at MINI MICRO N.E. Booth 208-210

**Circle 3 on Reader Inquiry Card**

# THE FPS 64-BIT FAMILY: CONSIDER WHY THE MOST ACCESSIBLE SUPERCOMPUTERS MAY BE THE FASTEST WAY TO DO YOUR JOB.



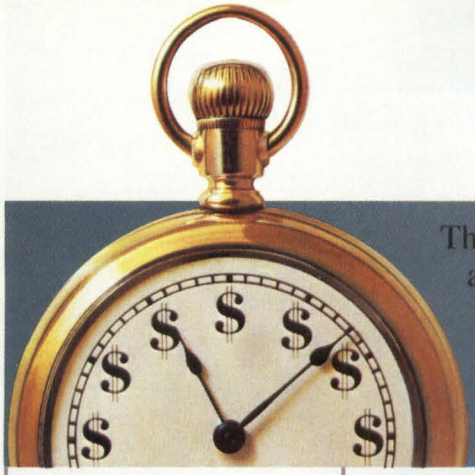

The new 38 MFLOPS FPS-264, with 64-bit accuracy, large storage, and architecture refined to achieve a high percentage of its peak speed. For many applications, it can provide half the performance of the most popular supercomputer. Its moderate price and exceptional support liberates supercomputing from the realm of major corporate investment and puts it within practical reach of departments and teams.

**How fast can you get a supercomputer up and running is as important as how fast it runs.** When you look beyond peak computing speeds to the practical realities of compute-intensive analysis and simulation, odds are that nothing else can take your job from start to finish as fast as the FPS 64-bit supercomputer family. Here's why:

**1. FPS protects and utilizes your existing software resources.** FPS offers you an exceptional, proven software tool set. If your investment in FORTRAN is typical, the FPS Compiler will alone be a compelling advantage.

**2. More applications software than for any other comparable computer.** Compare quantity and quality of compatible third party software packages—for structural analysis, circuit design, reservoir simulation, fluid flow analysis, chemistry and much more—and the FPS advantage widens.

**3. The FPS 64-bit family makes supercomputing speeds affordable at the department level.** Even teams with remote access to Crays® and Cybers™ are



The FPS optimizing FORTRAN-77 Compiler lets you easily adapt code to FPS' pipelined architecture in a form that is nearly as efficient as hand-coded assembly language. With extensions for asynchronous I/O and for enhancing compatibility with other compilers, it is one of most comprehensive tools of its kind.

likely to find that the advantage of immediate, local access is well worth the sacrifice of standing in line for the "fastest" machines.

System prices start at $300,000 (U.S.) for the 11 MFLOPS FPS-164. The new 38 MFLOPS FPS-264, starting at $640,000, achieves 4-5 times the speed of the FPS-164 on many applications programs. The multiple parallel processing units and peak 341 MFLOPS of the FPS 164/MAX can run many matrix computations faster than supercomputers, for less than one-tenth the price.

## Family Specifications

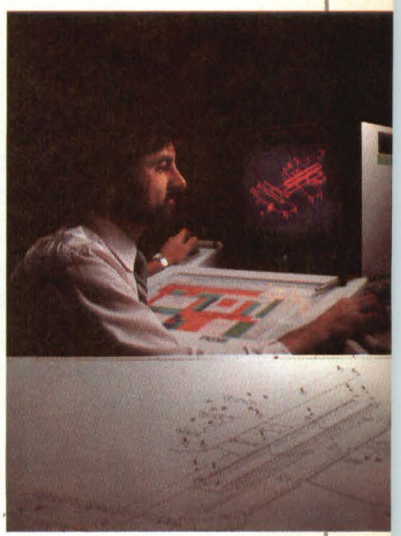
| | FPS-264 | FPS-164/MAX | FPS-164 |
|---|---|---|---|
| **Peak speed, MFLOPS** | 38 | 33-341 | 11 |
| **Dynamic range** | $2.8 \times 10^{-309}$ to $9.0 \times 10^{+307}$ | $2.8 \times 10^{-309}$ to $9.0 \times 10^{+307}$ | $2.8 \times 10^{-309}$ to $9.0 \times 10^{+307}$ |
| **Logic format** | 64 bits | 64 bits | 64 bits |
| **Main memory capacity** | 4.5 MWords | 15 MWords | 7.25 MWords |
| **Maximum disk storage capacity** | 16 Gbytes | 3 Gbytes | 3 Gbytes |
| **Precision** | 15 decimal digits | 15 decimal digits | 15 decimal digits |
| **Vector registers** | 4 x 2K | 124 x 2K (max.) | 4 x 2K |
| **Scalar registers** | 64 | 184 (max.) | 64 |
| **Host interfaces** | IBM, DEC | IBM, DEC, Sperry, Apollo | |
| **Program Development Software** | FORTRAN Compiler, Overlay Linker, Assembler, Object Librarian, Interactive Debugger. | | |

## Family Performance Measures

| | FPS-264 | FPS-164/MAX | | FPS-164 |
|---|---|---|---|---|
| | | 15 accelerators | 1 accelerator | |
| **Peak MFLOPS** | 38 | 341 | 33 | 11 |
| **Peak MOPS** | 190 | 1705 | 165 | 55 |
| **Peak MIPS (Multi-instruction partcels)** | 19 | 5.5 | 5.5 | 5.5 |
| **Typical MFLOPS, LINPACK Benchmark** | 9.9 | 20.0 | 6.0 | 2.6 |
| **Whetstones (64-bit)** | 20,100 | 5800 | 5800 | 5800 |
| **1000x1000 matrix multiply, seconds** | 53 | 10 | 66 | 189 |
| **$K/MFLOPS (system price/peak speed)** | $16.8K | $2.5K | $12.3K | $27.1K |


**4. The FPS family is expandable. Proven dependable. Well-supported. In other words, a safe, farsighted investment.** You can upgrade your existing FPS computer, or evolve from one level of performance to another, with minimal disruption. And you can bank on a record of reliability that begins with exhaustive manufacturing testing and extends to our 21 field office service facilities worldwide.

**Ask your local Floating Point sales representative to help you develop your own strategy for accessible supercomputing.** Contact Floating Point Systems, Box 23489, Portland, OR 97223. Telex 360470 FLOATPOIN BEAV. Sales offices worldwide. Call (800) 635-0938.



## THE PROVEN POWER IN ACCESSIBLE HIGH-SPEED COMPUTATION.

FPS® FLOATING POINT SYSTEMS

# Good News and Bad News

First the bad news: Our sister publication, *Electronic Imaging,* will no longer be published as a separate entity after this month. Now the good news: *Electronic Imaging*'s editorial coverage and editors will be integrated into *Digital Design*. This merger of the two magazines is possible because considerable overlap exists in technology coverage. The move will strengthen *Digital Design* and, increase our coverage of graphics and image processing. We will still devote as many pages to those technology areas that you have come to expect– from ICs to supercomputers –but graphics and imaging coverage will be expanded starting with the May issue.

In the meantime, the April issue holds several surprises for the readers. Up front, our new Technology Trends section presents in-depth technology news. The New Products section has been redesigned to include New Product Focus reports. These half-page to one-page summaries highlight important new products. In addition the type size has been increased to make the entire New Products section more readable. These changes are just a few steps in *Digital Design*'s continuing evolution toward a more readable and useful magazine. The May issue will be more of a revolution as we merge the editorial approach and graphic design elements of the two magazines.

So pay attention. You'll like the new *Digital Design*.

**John Bond, Editor in Chief**

# The most people-oriented interface ever designed.

Photo courtesy of American Stock Exchange

**The Fluke 1780A InfoTouch® Display**

What does the American Stock Exchange have to do with designing sophisticated manufacturing systems? Nothing, and everything.

If the Fluke 1780A InfoTouch Display can calm the chaos in a frenzied environment where a transaction is made every 36 seconds, just think of the benefits it can provide when designed into an OEM system for controlling an industrial manufacturing environment.

The fact is, the 1780A was specifically designed for industrial environments where a computerized system is run by people. And it is so simple to use even semi-skilled personnel can operate complex systems at the touch of a finger. To control weighing systems. Run refineries. Operate assembly line robots. Manufacture semiconductor wafers. And for dozens of other applications where man and machine work together.

Touch-sensitive displays are not new to Fluke. We pioneered one of the first truly touch-sensitive overlays back in 1979. Since that time we've improved and refined the technology, making the 1780A one of the most inexpensive and reliable systems on the market; and one that is backed by a multinational corporation and worldwide service organization.

To find out how you can incorporate the 1780A into your next design, call **1-800-426-0361;** or contact your local Fluke Sales Engineer or Representative. We think you'll agree with Amex, it's a good investment.

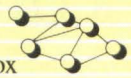
FLUKE®

IN THE U.S. AND NON-EUROPEAN COUNTRIES: John Fluke Mfg. Co., Inc., P.O. Box C9090, M/S 250C, Everett, WA 98206, Sales: (206) 356-5400, Other: (206) 347-6100.
EUROPEAN HEADQUARTERS: Fluke (Holland) B.V., P.O. Box 2269, 5600 CG Eindhoven, The Netherlands, (040) 458045, TLX: 51846.


**Circle 17 on Reader Inquiry Card**

# UPDATE

## XNS Implementors Group Formed



Representatives from about 30 organizations using Xerox Network Systems (XNS) communications protocols have formed the Xerox Network Systems Implementors Group (XNSIG). The group was established to exchange information and ideas regarding XNS developments and applications, encourage compatible operation among various vendors' implementations and promote XNS as an open system communications architecture standard.

## TI Produces 256K DRAM

Texas Instruments has begun producing two versions of its 256K × 1 DRAM devices, the TMS4256 page-mode and the TMS4257 nibble-mode. The 256K DRAMs use the same refresh scheme used in its 64K DRAM and are directly upward compatible, allowing an immediate quadrupling of system memory capacity without redesign or additional hardware. They are fabricated with 2-micron N-channel double-level polysilicon gate single-level metal technology.

## Erasable Optical-Disk Media

3M released performance details of its first erasable optical-disk product. Although the 5¼" disk has the capability to store up to 500 Mbytes, the average range is 250- 450 Mbytes. It also has the capability to record a high data rate (75 Mbps) but 3M cautions it will be some time before that is fully utilized.

## 32-Bit SBC Developed For Multibus II

Microbar Systems Inc. developed a single-board computer (SBC) that combines the 68020 32-bit microprocessor with the open-systems architecture of Multibus II. Included on the DBC II/68020 SBC are a cache memory and a memory management scheme. Microbar will port UNIX System V to the DBC II/68020 computer.

## Rockwell Purchases Allen-Brady

Rockwell International Corp. purchased all of the outstanding common stock from Allen-Brady Co., a manufacturer of electronic systems and equipment for industrial automation markets, for $1.65 billion. Rockwell expects the acquisition to fit into their long-range strategtic objectives concerning the growth of factory automation.

## Silicon-On-Sapphire Circuits On 4" Wafers

Asea Hafo Inc. claims it is the first company to produce silicon-on-sapphire (SOS) custom integrated circuits on 4" wafers. The isolating sapphire substrate of SOS circuits makes them immune to latch-up problems and more tolerant of transient radiation than bulk silicon.

## Micom Expands LAN Activities

Micom Systems Inc. acquired Interlan Inc., a privately owned firm supplying Ethernet LAN products, for 1,750,000 shares of its common stock. Through the acquisition, Micom expects to offer a local network approach which integrates data PABX and cable-based LAN technology in a single local network system. Interlan will operate as a wholly-owned subsidiary with the sales organization of both companies combining forces.

## LinCMOS Technology

A silicon-gate CMOS process for analog and interface applications has been developed by Texas Instruments. The LinCMOS technology combines the low power, low voltage and high input impedance of CMOS integrated circuits with single supply operation and bipolar-like speeds. The result is linear ICs with low 210 mV input-offset voltages. The TLC271 series of general-purpose op amps has a low input-offset voltage that typically varies only 0.1 $\mu$V per month and 0.7 $\mu$V per degree Celsius. Using the offset null pins provided, voltage can be reduced further.

The LinCMOS process also produces ICs with bandwidths that are two to three times greater than metal-gate CMOS components and the self-aligned gate of the transistors results in a gate-drain capacitance that is about one-seventh of metal-gate CMOS ICs.

TI has added recent devices to the LinCMOS family. Two comparators, the TLC372 and TLC372, operate at twice the speed and half the power of the industry-standard bipolar LM393.

## Fault Tolerant Graphics

Stratus Computer Inc. and Data Research and Applications (DRA) are offering device-independent graphics software packages. The DI-3000 and GK-2000 developed by Precision Visuals are designed to run on the family of Stratus/32 Continuous Processing computer systems.

## ICs With 1 Nsec Switching Time

Siliconix redesigned its SD210 series FETs and SD5000 series analog switch ICs using an oxide-isolated silicon gate DMOS process. Combining low drain-to-source on-resistance with low input capacitance, these products provide 1 nsec switching time. Designed to switch signals in the range of 5V to 10V, the series has a maximum drain current of 50$\mu$amps and typical drain-to-source on resistance is 50 Ω.

## ICs For Multibus II

Under an agreement with Intel, Toshiba Corp. will manufacture, market and sell Multibus II bus interface ICs. The ICs, the Bus Arbiter/Controller and the Message Interrupt Controller, will act as the general interface to the Parallel System Bus (iPSB) of Multibus II. The Bus Arbiter/Controller oversees use of the bus in a multiprocessor system, manages bus control lines and checks for errors. The message interrupt controller provides the interrupt message generation and receiving function for modules such as host processors or peripheral controllers.

## IEC Issues Standard

The International Electrotechnical Commission issued an international standard on electromagnetic compatibility for industrial-process measurement and equipment control. The standard establishes a common reference for evaluating the performance of industrial-process measurement and control equipment when subjected to electromagnetic fields that will generate continuous wave radiated electromagnetic energy. The standard sets forth a test procedure and recommends severity levels.

# Because You need to run FORTRAN programs 10X to 100X faster...

Mini-MAP makes it practical to apply array processing to general-purpose scientific and engineering computing.

**Practical in terms of use:** Mini-MAP's compiler allows you to program the array processor directly in FORTRAN. An assembler, a linker, and a debugger are also part of the package. Plus you can use our library of over 250 highly optimized scientific subroutines.

**Practical in terms of throughput:** Because it is an array processor, Mini-MAP increases the computing speed of a mini or supermini computer as much as 10 to 100 times. Where it takes a typical minicomputer minutes to perform tasks such as image rotation, Mini-MAP reduces interactive response times to seconds. Your computer may require hours to perform each step of a trial-and-error-process such as simulation, but Mini-MAP, can zip through in mere minutes.

DEC, PDP-11, LSI-11, and VAX-11 are trademarks of Digital Equipment Corp.
Mini-MAP is a trademark of CSPI.

## We built Mini-MAP.™

**Practical in terms of cost:** Mini-MAP is available as an economical, four-board set or as a packaged system. Now, with Mini-MAP, OEMs can offer their customers a better product at lower costs. Mini-MAP's low power demands, small size, and high reliability make the package extremely attractive. And end users will find our FORTRAN compiler and other software tools minimize program development costs.

**Some practical things to know about Mini-MAP:** 32-bit DEC™ floating point format ☐ Interfaces to DEC PDP-11, LSI-11, and VAX-11 series ☐ Up to 16 MBytes of data memory ☐ 1024 x 1024 2-D FFT in 8.8 seconds ☐ Extensive software tools plus dedicated applications assistance including training, convenient parts depots, and field service staff support our worldwide installations.
To find out how Mini-MAP can work for you, **call toll free 1 800 325-3110.**

cspi
THE ARRAY PROCESSORS

40 Linnell Circle, Billerica, Massachusetts 01821 • 617/272-6020 • TWX: 710-347-0176

**Circle 60 on Reader Inquiry Card**

# WASHINGTON REPORT

by Anne A. Armstrong

## OMB And GSA Quarrel Over Contract

In a colossal public airing of family grievances, the Office of Management and Budget announced it was abruptly stopping the procurement process for a multibillion dollar long-distance telephone system for the federal government. Only days before, the General Services Administration had briefed more than 70 companies that were interested in bidding on some or all of the 10-year contract for voice, data and video traffic.

David Stockman, OMB director, said in a letter to GSA that no further action on the procurement was to be taken until a broad executive branch review of the policy has been completed. Stockman also said that technological questions—should the service carry data as well as voice—and policy issues, such as who would be required to use the network and under what conditions, have yet to be resolved.

Under GSA's original timetable, the contract would have been awarded in 1987, but service was not scheduled to begin until 1989. Neither OMB nor GSA would venture a guess about how long the review would take.

GSA officials appeared to be caught off guard by the stop order and said that OMB had been briefed on the plan and had not indicated there were any objections.

The latest move delays chances of AT&T competitors gaining a bigger share of the government telecommunications business, according to industry observers. Currently, AT&T provides more than 85% of the government's long distance service. The Department of Defense, in particular, has expressed concern in years past about the effect on service of awarding contracts to discount long-distance services.

## Commerce And State End Turf Squabble

Another long-running intragovernmental feud over who should control international telecommunications policy has apparently ended as the Departments of State and Commerce reached a new agreement outlining each other's area of responsibility. Under the new arrangement, Commerce will formulate policy and act on behalf of the Executive, and State will cover all relations with foreign governments and intergovernment organizations. In other words, Commerce will provide technical expertise and domestic views and State will handle foreign policy support.

State is also in charge of US delegations to international meetings—which includes staffing, instructions and submitting any treaties to Congress. Earlier attempts to settle jurisdictional questions lead to disputes over who was in charge of such areas as international satellite systems.

## Retailer Opens All-Tempest Store

MBI, the computer retailer that holds the contract for the government's computer store, has opened a branch that specializes in Tempest products. The new store carries more than 50 products that are designed with special shielding to protect them against electromagnetic interference.

MBI officials believe that by offering government buyers the chance to compare different systems side-by-side and to put all the components on a single purchase order, they will attract business that would have gone through other channels. In addition, the store will offer training at any of nine Washington area stores. If the Tempest store is a success, other specialty market stores may be opened in other areas, say store executives.

## Bill Pulls Copyright Protection From Japanese Software

In a move designed to send a message to Japan's Ministry of International Trade and Industry (MITI), Sen. Frank R. Lautenburg (D-NJ) introduced a bill in the Senate that would remove copyright protection for software originating in countries that do not offer protection to US software. Aimed specifically at Japan, the bill is intended to add pressure to the US efforts to stop that government from changing its copyright protection for software from the current 50 years to a proposed 15 years.

Several US organizations, including The Association of Data Processing Service Organizations, are trying to derail the copyright revision effort in Japan. Last year, US industry groups did succeed in bumping the proposal from consideration; however MITI has continued to develop and push the legislation for consideration this year by the Japanese legislature.

Lautenberg's bill says that if a country gives less than 25 years of copyright protection for software, the US will not give any protection to software first published in that country or by its citizens.

## FCC Considers New Regulations For Japanese Products

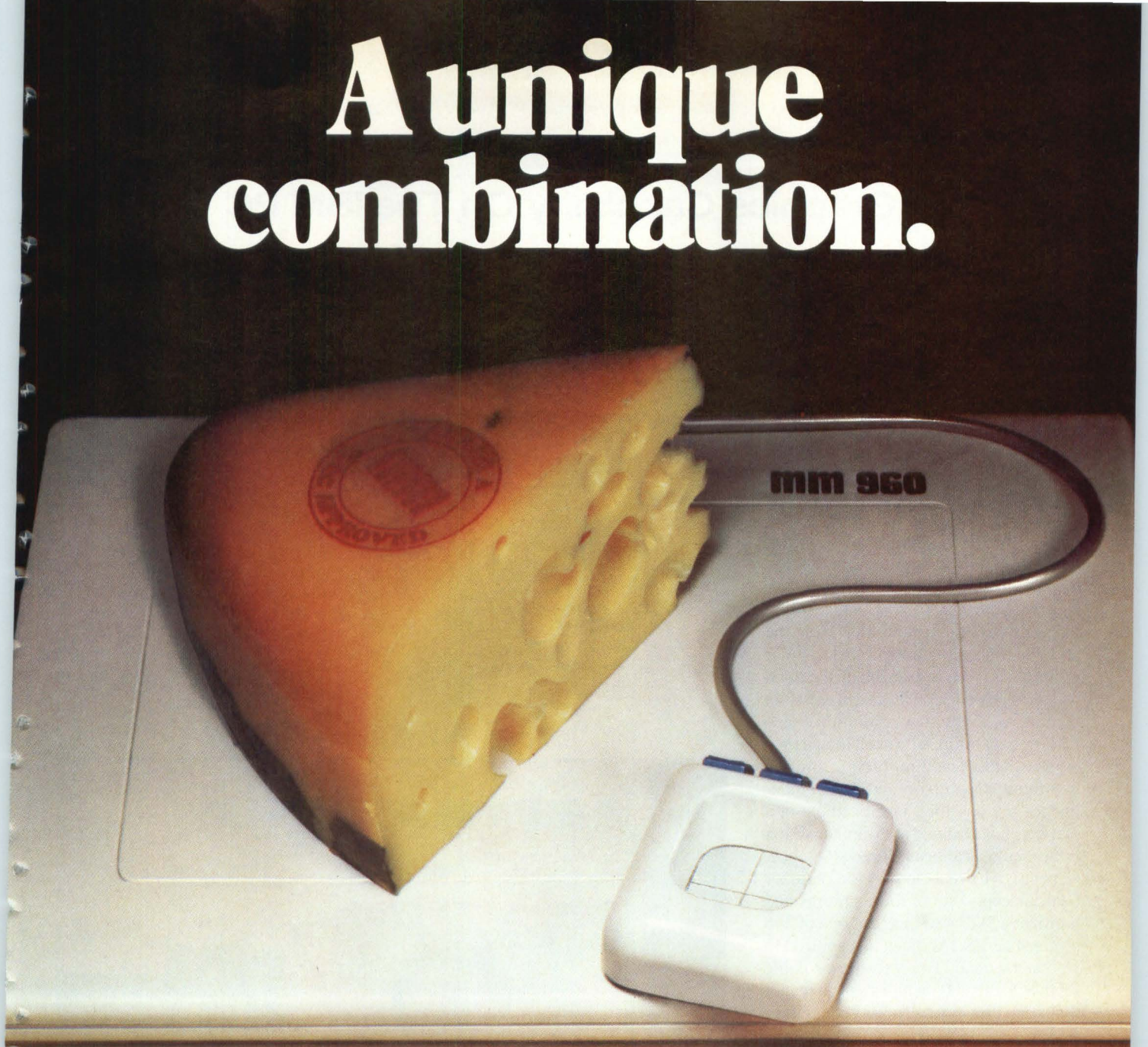
Years of complaining that Japanese import regulations effectively act as a restraint on trade may have paid off for telecommunications manufacturers. FCC chairman Mark Fowler said he is considering whether the US should institute retaliatory trade restrictions here that would make Japanese goods as difficult to import into the US as US firms say it is to get into Japan. American companies point to sales figures, such as Japanese phone equipment sold to the US last year was more than $2 billion, while US equipment sold to Japan amounted to only $194 million.

## EDS Gets INS Contract

Electronic Data Systems, now a General Motors subsidiary, has succeeded in winning most of a contract it originally lost to IBM. The $99.5 million contract for equipment to monitor the entry and departure of more than 50 million visitors to the US was in dispute when EDS sued to stop the award charging IBM representatives with an illegal meeting with INS officials. EDS claimed that as a result of the meeting IBM was able to adjust its bid so it was slightly lower than the competing EDS bid.

All parties have apparently been negotiating a settlement for several months. The final agreement called for EDS to drop its federal court suit and, in return, to receive $91.5 million of the contract. However, EDS also agreed to buy all the hardware for the contract from IBM. The settlement was reached before GAO, which was investigating, had announced any conclusions.

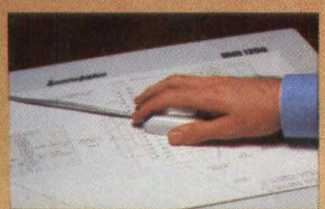
# A unique combination.




## Introducing a digitizer with a built-in mouse.

A unique combination unmatched by any digitizer on the market today, the MM™ Series can perform all your cursor steering, menu picking and graphics digitizing tasks. The MM outputs both absolute coordinate data like a digitizer and delta coordinate data like a mouse.

The MM Series was designed to offer builders of today's lower-cost terminals, graphic workstations and personal computers Maximum performance at Minimum cost. Maximum performance because you'll get all the features you need from a high resolution, remotely-controlled digitizer plus the versatility of a cursor steering mouse in one compact package. And Minimum cost because MM was designed, right from the start, to be inexpensive to purchase, integrate and maintain.



MM digitizers are available with either cursor or pen-like stylus.

Advanced packaging combining light weight, small overall size, and slim profile with built-in tilt mechanism make the MM Series an ideal addition to your user-friendly system.

Every MM Series digitizer is backed by Summagraphics, the leader in digitizers, and the emerging leader in graphics input devices.

Call or write Summagraphics Corporation, 35 Brentwood Avenue, P.O. Box 781, Fairfield, CT 06430. Telephone (203) 384-1344. Telex 96-4348.

Summagraphics® CORPORATION

Circle 41 on Reader Inquiry Card

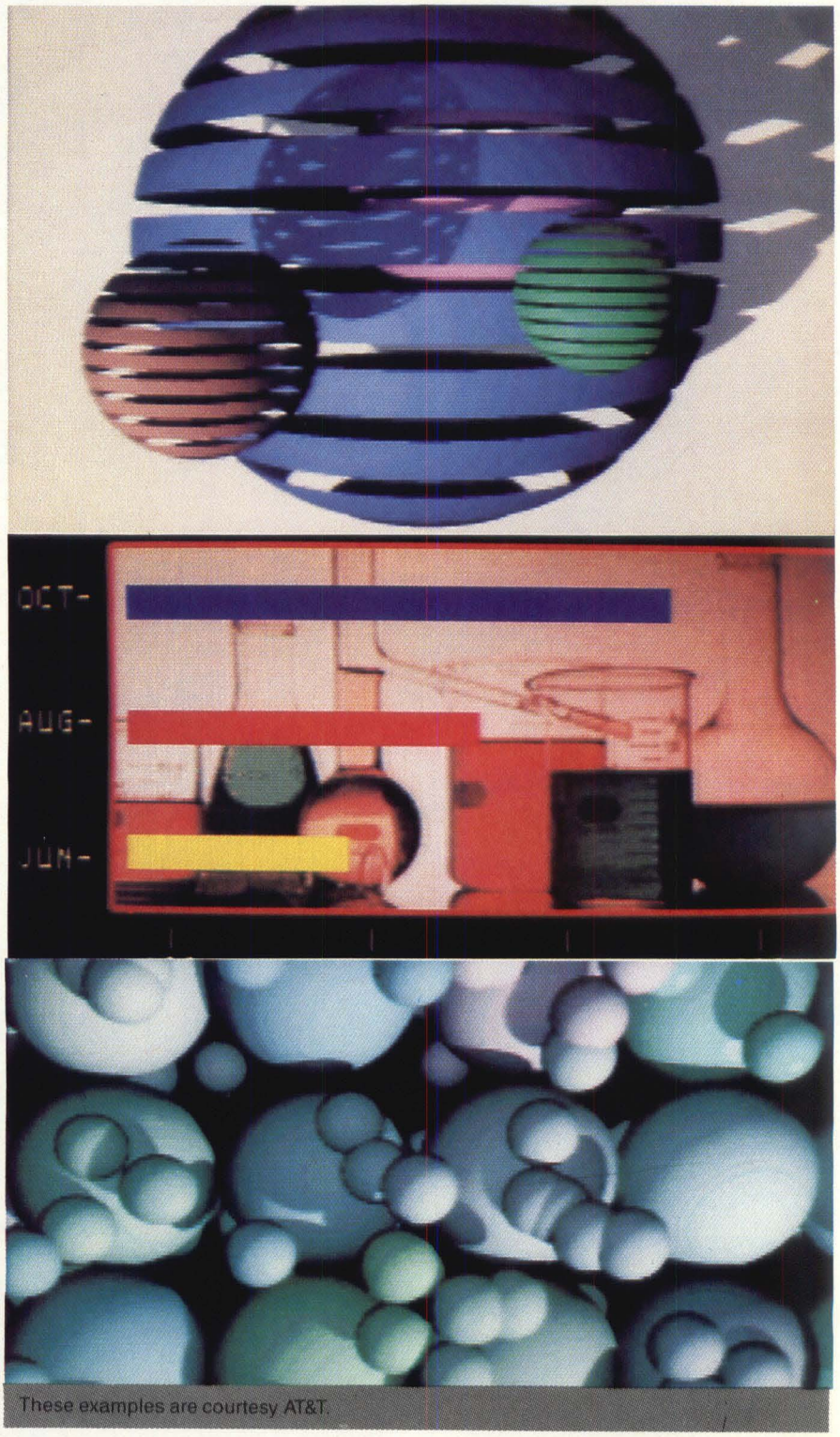
# High-End Graphics Capability On The IBM PC

With the proliferation of IBM PCs, look-alikes and peripherals, engineers will inevitably take advantage of this popularity and use these for creating high-end equipment. The basis for this popularity is partly due to the acceptance of the IBM 16-bit bus. In fact, several manufacturers are in the process of offering the PC on a peripheral-size card, enabling system integrators to add other boards with specialized functions. Designers in the past were oriented toward integrated systems; now they view the architecture as functional blocks.

Graphics is one area in which the trend of dedicated power on the board exists. In contrast to simple, low resolution chart-making capability, advanced image processing, video capture, high resolution with hundreds of colors and greater intelligence are possible. One example of a graphics board aimed at computer vision is the Oculus 100 from Coreco (Quebec, Canada). The real-time image digitizer board accepts one of four cameras and digitizes a 512×480 image at one of 256 levels. The RS-170 image is captured in 1/30 of a second. The software available for the Oculus 100 includes a page reader that converts typewritten letters into ASCII.

The Oculus 200 is a real-time gray level digitizer board that displays 512×480 pixels × 7 bits (128 gray levels). The board includes external sync inputs and output to a video monitor. Full color is possible with the use of three boards. A teleconference program that allows fixed frame teleconferencing and an industrial inspection program for sorting, comparing or quality control are two optional software packages. Source code is included with the software.

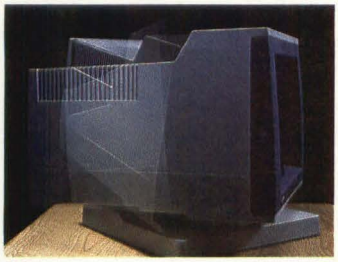
Aiming for 8-bit depth, the Epix (Chicago, IL) Silicon Video board can grab 1-752 pixels per line and 1-480 lines per frame in real time. The programmability of the horizontal and vertical image is excellent for machine vision applications. Memory can be extended from 256K to 1 Mbyte for image storage. The




These examples are courtesy AT&T.

# GOOD LOOKS RUN IN THE FAMILY.

## LEXIDATA'S LEX 90 FAMILY OF HIGH-PERFORMANCE DISPLAY PROCESSORS.



Lexidata's monitor enclosure design features a unique tilt and swivel movement with smooth and easy operation. All monitor connections and peripheral power supplies are located in the enclosure's base.

LOOKING GOOD. The LEX 90™ family is a good family to know. It's as advanced in a business sense as it is technologically. And what it has, compared to what it costs, makes it look very good indeed. For example:

Its software architecture is compatible both within the family and with our popular Series 3000 line. So performance upgrades are easy and economical. And software investments are well protected.

Every LEX 90 model has the same basic components which use the latest bit-slice technology for rapid execution of complex calculations and set-up times.

The family's flexibility allows you to buy only the functionality you need now, and gives you the ability to add on later as required.

Exclusive SimulRes functionality allows simultaneous display of 640x512 and 1280x1024 images on the same screen. A True Color configuration offers two buffers of 640x512x24 with an 8-bit color lookup table for each color. And where you're looking for high performance with high resolution, there's a LEX 90 model that can support up to 24 planes of 1280x1024 display memory at 60Hz non-interlaced refresh.

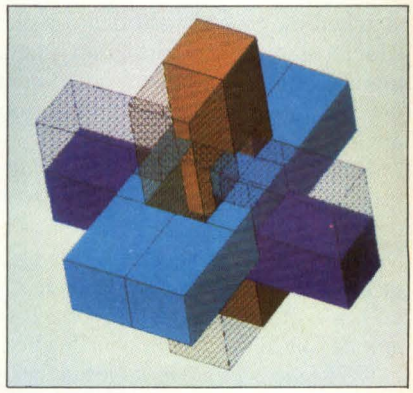
LEX 90's SimulRes enables the designer to mix theory with reality by allowing the simultaneous display of a wire-frame model with the real-life product. (Courtesy of PDA Engineering)

A tiger shows off its "true colors" with the LEX 90 True Color display system from Lexidata.

The extraordinary solid modeling display capability of our patented SOLIDVIEW™ technology is available in a 640x512 version. And for petrochemical applications, there's GEOVIEW,™ a three-dimensional geological interpretation package.

On-board diagnostics, based on a 6801 microprocessor, help maximize uptime. And the unique tilt-and-swivel movement of our monitor allows smooth and easy operation of your display.

Of course, the entire family is compatible with a variety of leading application software packages and minicomputers. Which makes everyone look even better.



SOLIDVIEW, Lexidata's patented technology for the display of solid models, is available as an option on selected LEX 90 display processors. Its translucent shading pattern allows you to see inside your solid model.

For a good look at the LEX 90 family and its expanding capabilities, call us at 1-800-472-4747. In Massachusetts, call (617) 663-8550. Or write: Lexidata™ Corporation, 755 Middlesex Turnpike, Billerica, Massachusetts USA 01865. TWX: 710-347-1574. In UNITED KINGDOM call: Lexidata Ltd., Hook (025672) 3411. In FRANCE call: Lexidata SARL, Rungis (1) 686-56-71. In JAPAN call: Lexidata Technical Center, Tokyo 486-0670.

LEXIDATA®
LOOKING GOOD.

board also accepts genlock and provides output to an RGB or B&W monitor. Genlock allows an external synch signal to drive the graphics horizontal and vertical synch. Video timing on the board is selectable, and the 14.318 MHz oscillator or the PC clock oscillator can be chosen for the master timing of the RS-170 video signal. Sync timing is available for driving cameras or monitors that do not accept composite video. Besides standard diagnostics and demos, such additional software as histogram generators, Huffman encoding for image compression and multiple display functions are available.

AT&T (Parsippany, NY) is offering a graphics board that is different from those with merely high resolution. The Video Display Adapter (VDA) is a plug-in board with 256×256 pixels at 256 colors from a palette of over 32000 colors. The high resolution mode allows 512×257×16 colors. The large number of colors allows continuous tone and television-like quality on analog RGB and composite monitors. Input signals for signal pass through can be either NTSC or analog RGB. Software included with the VDA runs under MS-DOS and includes drivers written in C, reading and writing to the display, bit area manipulation, geometrics, fonts, image compression/decompression and several images. This board matches with the Image Capture Board which takes an image at the VDA's resolution from a video source such as a camera or VCR. Adding to the family of graphics products from the Consumer Products Division is a NAPLPS decoder which enables users to receive and display frames made from one VDA to another. NAPLPS, North American Presentation Level Protocol Syntax, is a graphics standard for the transmission of graphics images. Because of its ability to transmit images in different resolutions with different computers, it is gaining popularity. The quality of the VDA system with the NAPLPS decoder is the same as AT&T's Sceptre videotex system.

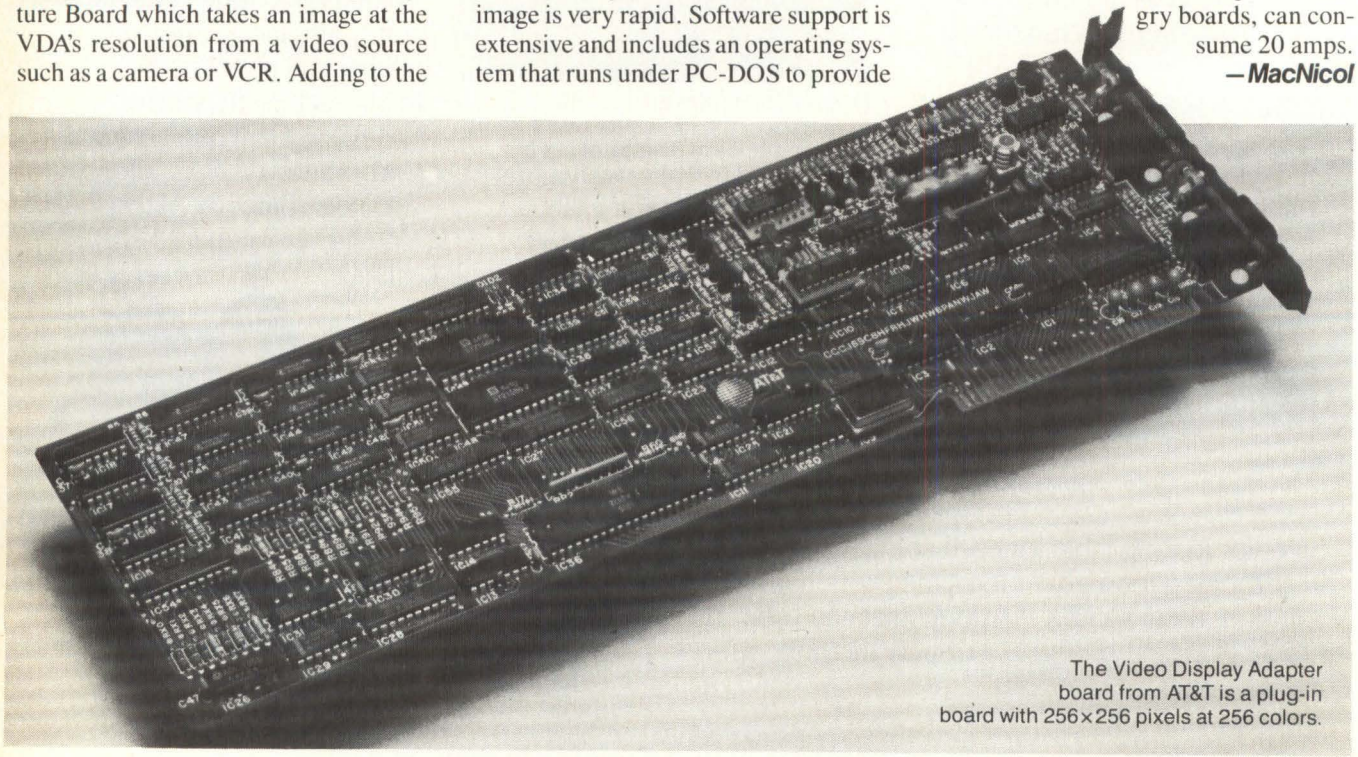
Data Translation (Marlboro, MA) also offers a 256×256×8 bit frame grabber. The DT2803 has a dual-port-frame store memory and eight 64×8 input look-up tables with four 256×12 output look-up tables. The color RGB output is 64 colors at 64 intensities for a total of 4096 attributes. Image capture is real time, one video frame in 1/30 of a second. Videolab, the optional software package, has a large set of callable routines from Basic, C, Pascal and Fortran. The software package provides an interactive tutorial program and an advanced package for experienced programmers. This board, combined with Sky Computer's (Lowell, MA) SKY320 array processor board, permits image processing via high speed external data paths. Using TI's TMS320 signal processing chip, FFTs, IFFTs, matrix multiplies and convolution of an image is very rapid. Software support is extensive and includes an operating system that runs under PC-DOS to provide a set of user callable routines to control the SKY320. A C compiler, a macro preprocessor, assembler and a library of signal and image processing algorithms are provided.

For higher resolution, the PC-EYE from Chorus Data Systems (Merrimack, NH) is available. It is a 480×512×1-, 2-, 4-, 6-, or 8-bits deep video capture system. The system is versatile. It has a four-channel selectable camera input and several auxiliary components for support. The Colorverter board accepts NTSC and converts the signal to RGB for digitization. The PC-EYE can then use the Tecmar, Hercules, Scion, Digigraphics, Mylex or Number Nine board for display. Software is available from Chorus, and support is available for other graphics packages such as Halo and Dr. Halo.

PCVISION from Imaging Technology (Woburn, MA) is another frame grabber for the PC. Resolution is 512×512 pixels × 8 bits deep, providing 256 gray levels or pseudocolors. The PCVISION digitizes RS-170 signal at 30 frames per second which is intended for applications in robotic vision, teleconferencing, medical imaging and factory inspection.

A systems integrator should consider the power supply in applications that use multiple boards. Full color Oculus boards, for example, use 4 amps at 5 volts each. This, combined with a hard disk and other power hungry boards, can consume 20 amps.

***—MacNicol***



The Video Display Adapter board from AT&T is a plug-in board with 256×256 pixels at 256 colors.


# Only Triad makes Bypass Static Switch a standard on all Powerstar™ UPS units.

You could call it a switch in time, because Triad's automatic Bypass Static Switch—a better-than-standard feature on all Powerstar uninterruptible power supply (true UPS) units—transfers and regulates incoming power automatically and instantaneously.

Powerstar true UPS units provide instantaneous power upon AC line power failure...preventing potential damage and memory loss and protecting equipment from an overload inrush of current without shutting it down.

The Bypass Static Switch is a vital feature on any true UPS unit. But only Triad's Powerstar offers it as a standard feature at no extra cost.

Powerstar is at work constantly, providing a continuous, regulated line voltage flow to equipment..freeing any power line of electrical interference and glitches...and protecting equipment against damage and losses due to line voltage surges, failures and irregularities.

Powerstar units ensure complete isolation from the power line...and provide up to an hour of battery back-up time to prevent loss of entries. When power fails, Powerstar saves the day...and the day's work.

## Another powerful incentive is its energy efficiency.

Powerstar units are 90 percent energy-efficient or better; it runs up to 20° C cooler than most other UPS units.

With output ratings from 250 to 2500VA ...and an output load capability that's unsurpassed in the industry...there's a Powerstar UPS unit designed and competitively priced right for small or large computers, point-of-sale terminals, word processors and virtually any microprocessor-based industrial control.

Triad also makes a full line of Linestar™ portable and hard wire constant voltage regulators (CVRs) to protect equipment and operations from low voltages, power surges and transients...with the added feature of both common and transverse mode noise attenuation...and with output ratings ranging from 70 to 30,000 VA.

Powerstar and Linestar...two powerful ways to stop line voltage irregularities before they stop equipment.

For unsurpassed quality, competitive prices and fast delivery, contact your nearest Triad-Utrad distributor, or write: Triad-Utrad, Standard Products, 1124 E. Franklin St., Huntington, IN 46750, 219-356-6500, TWX 810-333-1532.

Triad Winds Up The Best

TRIAD®-UTRAD
A Division of MagneTek, Inc.

Circle 35 on Reader Inquiry Card

# Megafile Leapfrogs Capacity Of Current 5¼" Drives

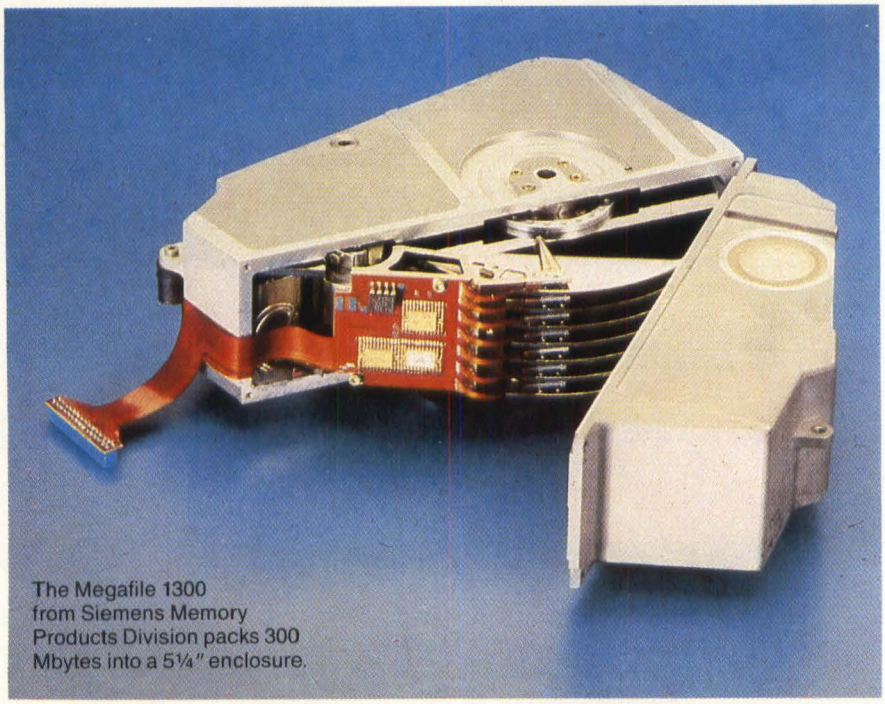
Providing capacity previously available only on larger disk drives, the Megafile 1300 from Siemens Memory Products Division (Westlake Village, CA) packs 306 Mbytes (254 Mbytes formatted) into a 5¼" enclosure. Currently being sampled, it leapfrogs over available 5¼" drives offering only one-third to one-half the capacity.

The highest-capacity drives currently shipped consist of a 143 Mbyte drive from Maxtor Corp. (San Jose, CA) and a 102 Mbyte drive from Advanced Storage Technology (San Jose, CA). The only other high-capacity drives being shipped are limited to 85 Mbytes. Vendors in this latter class include Control Data Corp. Magnetic Peripherals division (Oklahoma City, OK), Micropolis (Chatsworth, CA) and Priam Corp. (San Jose, CA).

The factor limiting most 5¼" disk drives to 85 Mbytes is the current ST506 interface. Accepted as the *de facto* industry standard, its 5 Mbit/sec data tranfer rate effectively limits the bit density to about 10,000 bits/in. In addition, track density cannot be increased since the interface specifies a maximum of 1024 cylinders that can be addressed per disk surface. Finally, the brute force method of increasing capacity by increasing the number of disks is thwarted by a limitation of a maximum of eight heads or eight disk surfaces.

In contrast, the Siemens drive takes advantage of the increased flexibility found with the Enhanced Small Disk Interface (*Digital Design*, January 1985, p. 44). It takes full advantage of the specification's increased data rate (10 Mbits/sec) to boost the bit density to 19077 bpi as well as increase the number of cylinders to 1224. Its increased capacity is also partly due to the greater number of data surfaces, now 12. The ESDI specification allows as many as 16.

Vendors seeking to maintain compatibility with the ST506 standard have a less straightforward path to increased capacity. For example, Priam proposes increasing the bit density 50% by moving from Modified Frequency Code Modulation data encoding to run-length limited coding. However, a measure of compatibility is lost since this would require modifications to existing ST506 controllers. Maxtor increases capacity of its XT-1000 family by adding platters and addressing the extra surfaces with an additional head select line undefined in the standard ST506 interface. As with the approach of Priam, this can cause havoc with existing controllers that may recognize this additional signal.



The Megafile 1300 from Siemens Memory Products Division packs 300 Mbytes into a 5¼" enclosure.

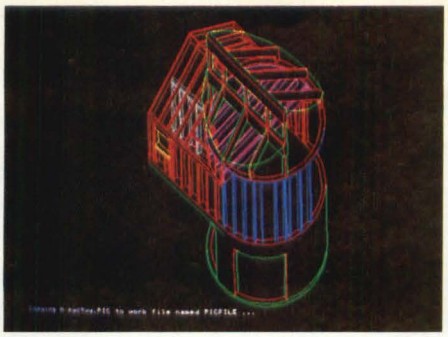
Although the ESDI interface provides adequate room for growth, vendors still face a formidable task in finding the right combination of heads and media to provide reliable storage. Of the three vendors supplying ESDI drives, only Control Data's Magnetic Peripherals division chooses to stick with ferrite heads and oxide media. Gene Milligan, Manager of Product Planning, thinks this conventional combination has yet to reach its upper limits. In fact, the current Wren-II drive has a storage capacity of 86 Mbytes, but exemplifies conservative design with its bit density held to just 9230 bpi and track density to 960 tpi.

Both Advanced Storage Technology and Siemens have opted for thin-film heads and media as the preferred path for increased capacity. Despite earlier problems with satisfactory yields, both companies believe the increased recording densities possible with this combination (30,000 bpi with run-length limited coding) make their use worthwhile. They also employ dedicated servo surfaces to better align the heads during read/write operations. Siemens has gone one step further by including embedded servos for closer track following.

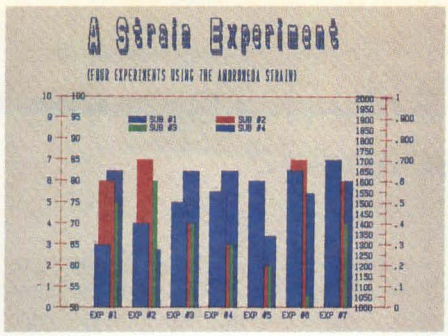
Advanced Storage Technology pursues a different design tack than Siemens by emphasizing area density, rather than the number of platters, as the principal means of expanding storage capability. Vice President Dan Klang foresees future versions of the existing 62 Mbyte and 102 Mbyte drives using the present two to three platter configuration. But these versions will increase the track density from 960 tpi to 1200 tpi and go to run-length limited coding to increase the bit density to 30,000 bpi from the present 20,000 bpi.

As a result, systems architects can soon expect to see 5¼" disk drives approach 500 Mbytes in capacity as more vendors implement high-performance interfaces like ESDI to gain the maximum benefits of thin-film technology.

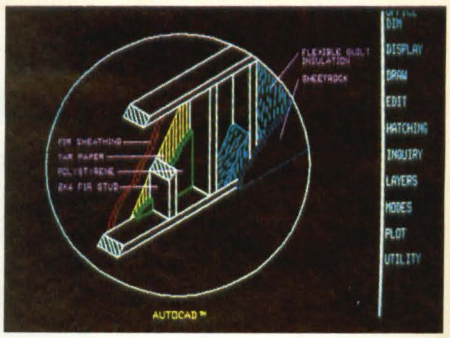
***—Aseo***



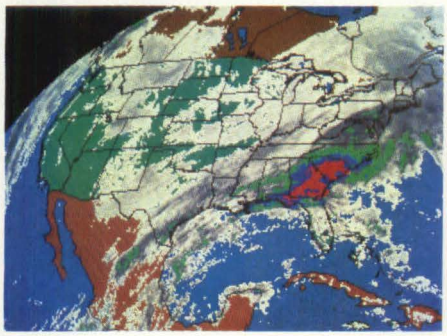
1. High Speed (MicroCAD Software)



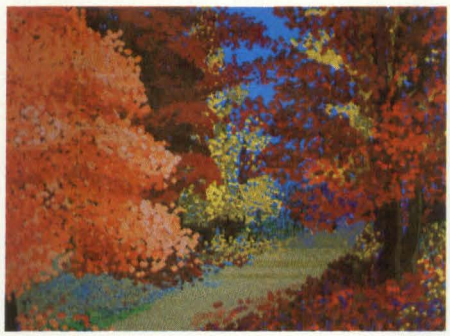

2. Dual Display Modes (Energraphics Software)



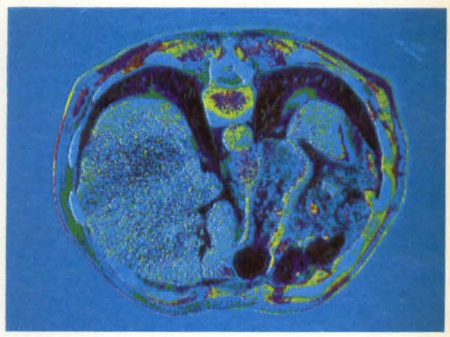

3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



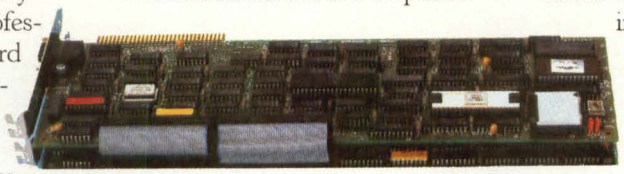
6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

# Six reasons why professionals continue to choose Vectrix for quality IBM XT/PC graphics.

Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit microprocessor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.



What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see. For more information, contact Vectrix Corporation, 2606 Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.

Vectrix
THE COMPUTER GRAPHICS COMPANY

Distributor inquiries welcome.



**Circle 55 on Reader Inquiry Card**

**See Us at NCGA Booth 360**

# Seven-Layer LAN Scheme Spawns Products For A Standard Backbone

While the International Standards dards Organization (ISO) slowly progresses toward networking protocols that fit into all seven layers of their Open Systems Interconnection (OSI) model, users are demanding systems with local area networking. The IBM PC Network (*Digital Design*, February 1985) will surely become a *de facto* standard for DOS-based micros. Microsoft (Bellevue, WA) Networks protocols, developed jointly with IBM (Boca Raton, FL) and Intel (Santa Clara, CA), round out the PC Network with upper protocol layers. Intel's benefit from this project is now clear: Their new OpenNET scheme uses these protocols on top of existing and new Ethernet and iNA 960 network products.

OpenNET is attractive for OEMs because the vendor is a known quantity and the scheme is IBM PC compatible. Further, nonproprietary protocol software is used at every level and all are offered from one vendor. End users have been able to get a complete network from turnkey vendors, but with proprietary protocols or for only one type of computer.

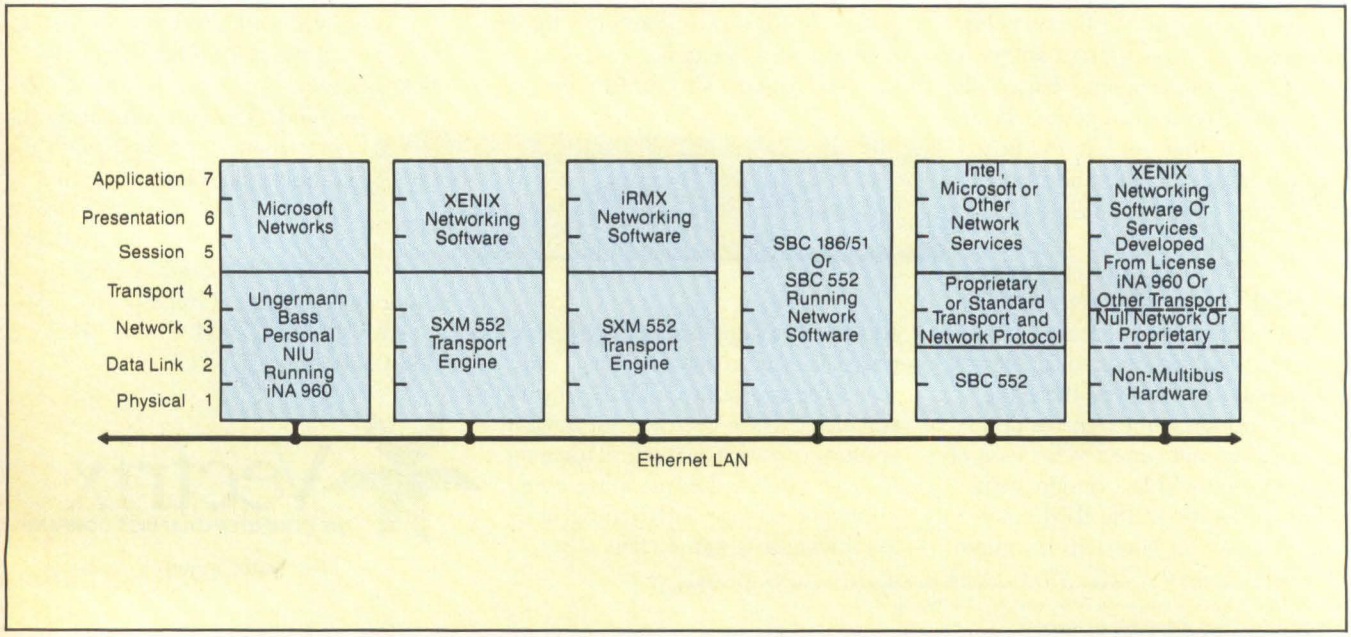
OEMs, on the other hand, can buy boards or boxes from several sources, but most only include layers one through four. Although current international standards also stop at the Transport (fourth) layer, networking only through this level allows connectivity but not communication. Above layer four, several sets of protocols have been popular (*Digital Design*, January 1985). Some firms have written their own, but commonly for only one operating system.

File transfer software licenses for application communication and data sharing between different computers has been available through only a handful of software vendors. A good deal of interface and design work was generally needed, and neither software nor hardware vendors are commonly well equipped to help.

With most networks, file transfer means an entire file must be transported through the network before work can begin. Disk servers divide a shared hard disk into logical volumes for each network node, and to use a file, it must be transferred to the user's partition. This may result in wasted disk access time and the possibility of differing versions of the same file. Even multiuser packages need to be in a special version for use on a network. For an application to use files on a station using a different OS, code must be written to accomplish file format transformation.

Upper-layer protocols for OpenNET will be in the public domain. Network services at layers five through seven allow transparent remote file access, so applications work with remote and local files identically. For intervendor operability, OpenNET network services support iRMX operating systems for real time and Xenix for UNIX multiuser systems. Using Microsoft Networks, DOS machines can also communicate on OpenNET. Multiuser applications need no modification for the network, and with transparent file access in place, other network services like mail and print can be built without too much effort.

As an OEM network, OpenNET is designed with hooks for other physical network equipment. By layering the protocols, writing software under other operating systems should be relatively straightforward, as well. Intel's Xenix package is written in C for portability, so their server can be used. For DOS systems, the Microsoft server software can be applied. Microsoft encourages OEMs to write their own server, and since theirs




Initial OpenNET product offerings allow DOS, Xenix and RMX-based computers to access each other's files. Hooks are built into the protocols to allow development for non-Ethernet networks and computers with other operating systems.

# The lean, mean plotting machine from Houston Instrument

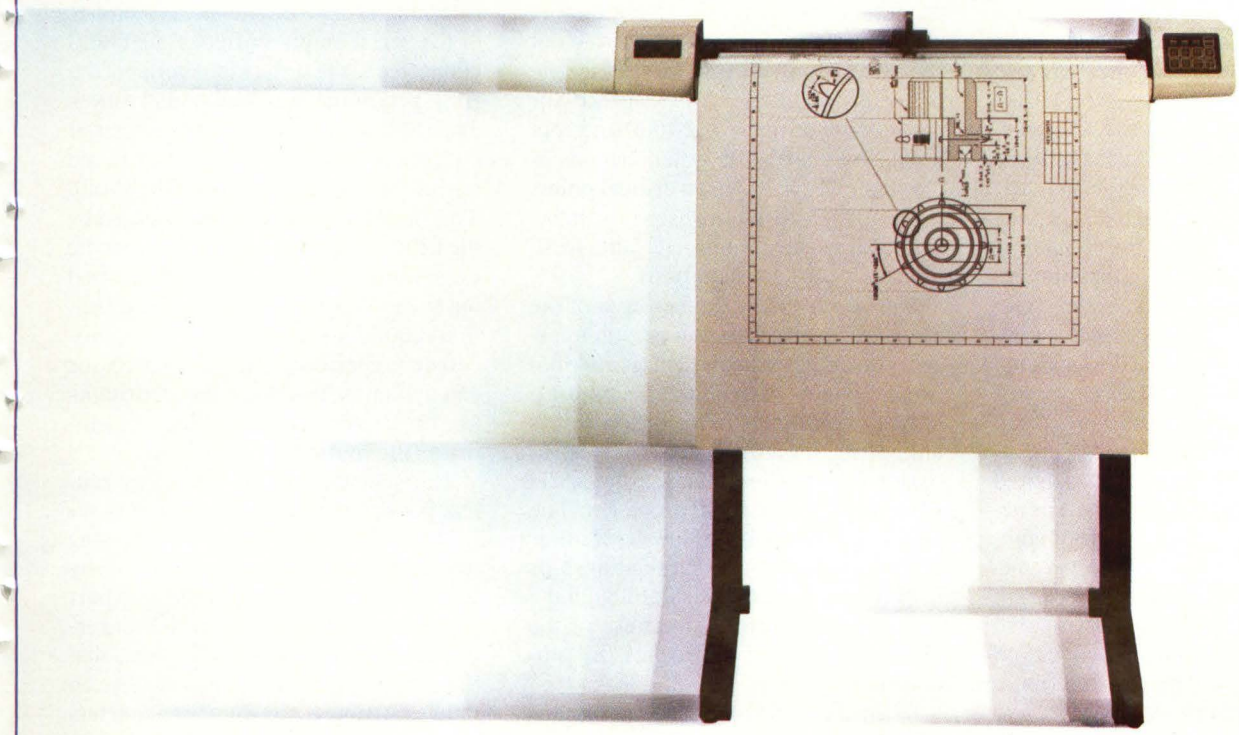
Houston Instrument's brand new servo driven DMP-51 is the fastest drum plotter we've designed to date. This superb plotter offers a pen speed of up to 22 inches/second; programmable accelerations, and a pen-on-paper resolution of 1/1000 of an inch! That means you'll turn out quality 17″ x 22″ and 22″x 34″ drawings a lot faster, increasing your firm's productivity and profitability.

Now, for more good news. The DMP-51, priced at $4,495*, is as fast as other plotters costing three times more. At that price, you can afford to put a DMP-51 at individual drafting work stations.

This is the professional plotter that meets the needs—and the budgets—of all companies, large or small.

The DMP-51 is intelligent, too. The DMP-51 can execute complex graphics operations from the simplest commands. A mechanical/architectural version, the DMP-52, with its 18″ x 24″ and 24″ x 36″ paper size, is available for the same price from Houston Instrument.

So, watch our new plotter in action . . . it won't take much time to realize it's the best buy for your money. For the name, address and phone number of your nearest dealer or distributor, write Houston Instrument, 8500 Cameron Rd., Austin, Texas, 78753. You can also call 1-800-531-5205 or 1-512-835-0900 (Texas residents). In Europe, contact Houston Instrument Belgium NV, Rochesterlaan 6, 8240 Gistel, Belgium. Tel: 059-27-74-45. Tlx: 846-81399.



*Suggested U.S. retail price

houston instrument

Visit Us at NCGA Booth 852

Write 36 on Reader Inquiry Card

is different from the Sytek/IBM version, this may not adversely impact compatibility.

In addition to the networking software for intervendor communication, initial OpenNET offerings include products Intel has offered for some time, such as iNA 960 ISO-standard transport software (with null Network implementation, layer three, until the next release) and the iSBC 186/51 Ethernet COMMputer module. For further OEM flexibility, new products are unbundled Multibus modules (**Figure 1**). The iSXM 552 transport engine is a box or board with transport protocols, RAM and cable included; the iSBC 552 COMMengine is only IEEE 802.3 hardware to level three with no RAM. By agreement with Ungermann-Bass (Santa Clara, CA), their Personal NIU controller boards will permit PC nodes to communicate on OpenNET.

The first OpenNET products constitute a backbone network, according to Intel. Other network clusters, like an IBM PC Network or GM's MAP for the factory, can be connected through a gateway to the backbone or devices can be directly attached. Ethernet's 10 Mbit/sec line speed was chosen partly to support Intel's multiuser systems like the 86/310, 286/310 and 286/380. Application throughput speed is about 200 Kbits to 250 Kbits/sec on Xenix and RMX nodes and 120 Kbits to 150 Kbits/sec on DOS nodes.

OpenNET products are available this month; the basic iSBC 552 board is $1,500 and the iSXM board (with RAM and iNA 960 protocols through layer four) is $1,800. Software costs $9,500 for either the RMX package or the Xenix OEM license. OpenNET is based on those standards currently set and IBM's choice of upper layers, an indication that VLSI and hardware development will follow. Intel also proclaims they will provide training and hand-holding services to allow designers to add network capability at minimal risk.

***—Pingry***

## TECHNOLOGY TRENDS/Software

# Expert System Gives Advice For Real-Time Control

By automating many of the functions handled by human operators, the Real-Time Intelligent Machine Interface (RTIME) software package from Lisp Machines Inc. (Los Angeles, CA) can expedite the management of such real-time applications as oil refineries and nuclear power plants. Using this package, the 68010 coprocessor in the the company's Lambda computer screens incoming information on a real-time basis thus freeing the dedicated LISP processor to concentrate on high-level decision making.

Working in parallel, the coprocessor communicates with the LISP processor via a software serial stream or by updating data values stored as arrays in shared memory. It handles such tasks as data acquisition, executing process-related algorithms and acting upon low-level events. Furthermore, the LISP processor can dynamically reprogram the coprocessor to watch for expected events or to focus on areas of the process where it needs more information to make a decision.

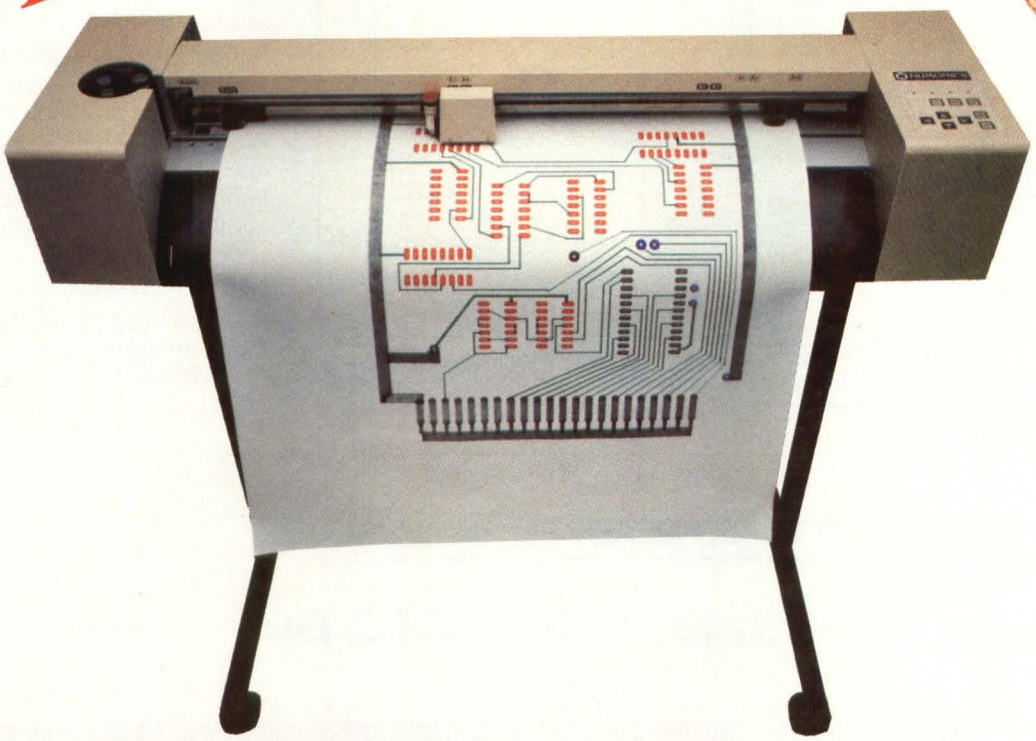
In effect, the organization of RTIME puts an expert system on top of a distributed control system. The 68010 acts as a programmable controller that monitors all input from sensors and carries out specific actions in response to specific stimulus conditions. This coprocessor can monitor as many as 20,000 different points in a distributed system but places the status of the 200 most critical points in the arrays stored in shared memory. These points are monitored by the LISP processor on a constant basis.

The coprocessor watches each of the remaining sensors within certain tolerances and time intervals. This is done between updates determined by the user. Should one or more of the these sensors fall outside their tolerances, the coprocessor then places a flag on the serial stream to alert the LISP processor. The 68010 is also capable of low-level inferences that provide if-then relationships between groups of sensors although the determination of the root cause of the observed behavior is left to the LISP processor.

Using a polling scheme, which scans this stream once every 250 msec, the LISP processor is free from physical interrupts, but still can respond in a reasonable amount of time. This stream consists of the serial output buffer of the 68010 connected to the serial input buffer of the LISP processor. Another stream moves data (128 bytes at a time) from the serial output buffer of the LISP buffer to the corresponding input buffer of the 68010. This output stream is the means used by the LISP processor to initiate the specific exception handling routine to be carried out by the coprocessor. Should the exception require an action not in the coprocessor's repertoire, the LISP processor can dynamically change the algorithms used and automatically reallocate memory as the routine is recompiled.

This scheme of focusing only on critical portions of the system not only relieves the LISP processor of processing information in real time, but also closely follows the manner in which expert human operators work. Carl Knickerbocker, architect of RTIME, notes that human operators can keep a close eye on only a portion of the gauges and meters before them and scan other meters briefly for wide variations in readings. In a sense, RTIME seeks to act as a high-

# CASCADE GRAPHICS, take note.



## AND ATTRIBASE, VERSATEC, ICS, PRIME COMPUTER

Einstein himself would find a plotter with this quality, speed and accuracy ingenious. Frankly, you will too. Using the newest technology to produce the most complex plots, the low-cost Numonics #5600 series plotters reduces the cost of your work stations by thousands of dollars, and you don't sacrifice speed, accuracy or flexibility.

It's fast. The #5600 plots at speeds up to 250 mm per second. The grit-roller transport system produces a smooth, accurate, controlled plot on cut sheet paper or mylar. A new synchro-belt drive is used for quiet, accurate, maintenance-free pen position control.

It's flexible. Accepts paper sizes from C to D and under HOST control automatically selects any of four self-capping, magazine loaded pens of any choice.

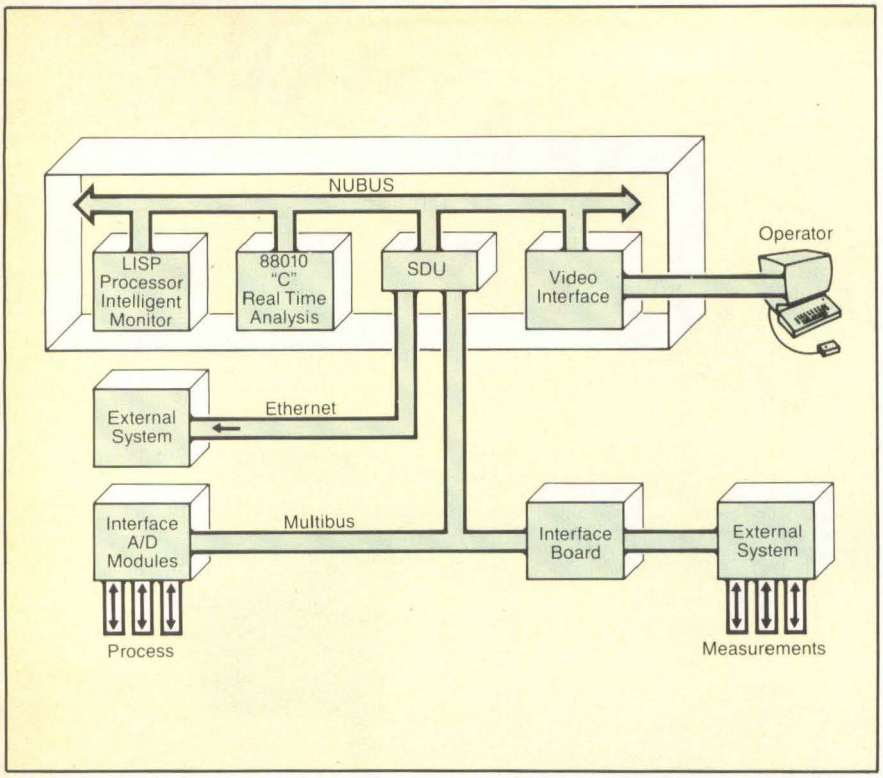
It has available one of the widest selections of command functions on the market today or, if you have existing software, use our HPGL emulators.

We're reliable. Our reliability based on manufacturing control and inspection, a comprehensive documentation system and complete traceability, all of which ensures a zero-defect product. It means superior construction and customer support. Take note and call us today.

NUMONICS

418 Pierce Street, Lansdale, Pa. 19446
Tel: (215) 362-2766; TWX: 510-661-6585

Circle 5 on Reader Inquiry Card




RTIME uses the NuBus to provide a high-speed communications link between the LISP processor and the 68010 real-time processor. Links to the outside world occur through peripheral boards on the Multibus chassis, or via Ethernet to other distributed systems.

speed filter for these operators so they can concentrate on making decisions rather than merely reacting.

To aid in this process, RTIME provides a series of menus so human operators can specify the rules of thumb that they use to come to their decisions. The knowledge base used by the LISP processor consists of a decision tree formed by the if-then relationships described by the human operators. Based on the inputs provided by the 68010 coprocessor, the LISP processor can form the same logical relationships and make the same logical inferences as its human counterpart. As a result, response time can be measured in milliseconds rather than in minutes.

Although this system represents a breakthrough in the application of expert systems, Knickerbocker cautions that the era of self-adaptive systems is still far off. He notes that existing systems work best in situations where the nature of the problem is well characterized and predictable. Expert systems are still incapable of anticipating possible consequences based on existing conditions; such intuition is best left to the human mind.

***—Aseo***

## TECHNOLOGY TRENDS/Boards

# PC Clones Challenge Role Of STD Bus

Low cost bus structures, such as the STD, have a new competitor—the integrated IBM PC-compatible motherboard. Already, three firms have announced products whose price and performance make them an extremely attractive alternative to the traditional board level approach exemplified by the STD bus.

The first board, from Mostron (Milpitas, CA), integrates a monochrome video controller, an Intel 8088 CPU, two RS-232 serial communications channels, a PC-compatible keyboard and a Centronics-printer interface (**Figure 1**). The board, the SBM-88 PC, also includes up to 256 Kbytes of RAM, with expansion capability of up to 640 Kbytes. Five I/O expansion slots are provided to allow the OEM to support a variety of available peripheral controllers. In addition, a floppy disk controller can support up to four 5¼" drives.

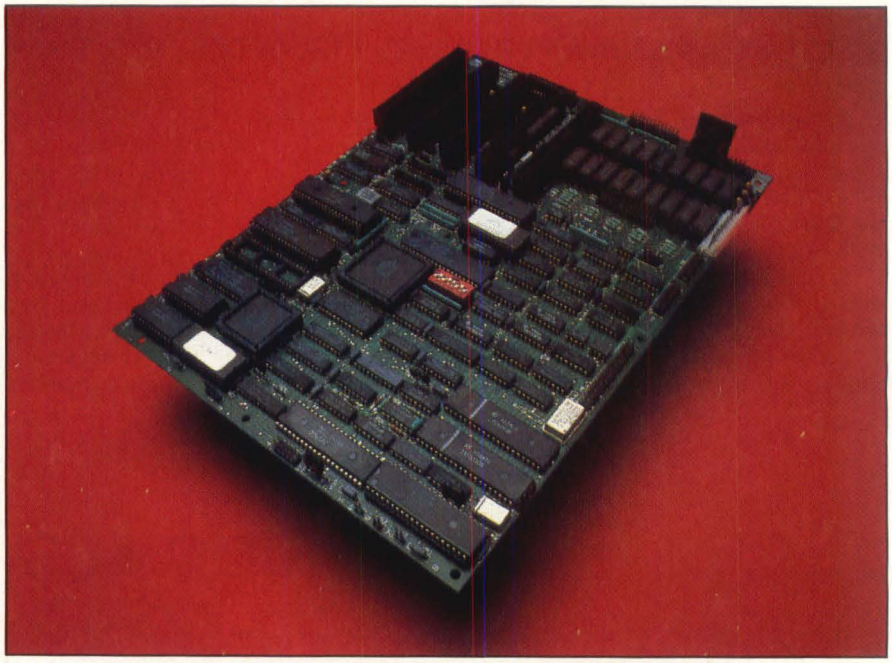
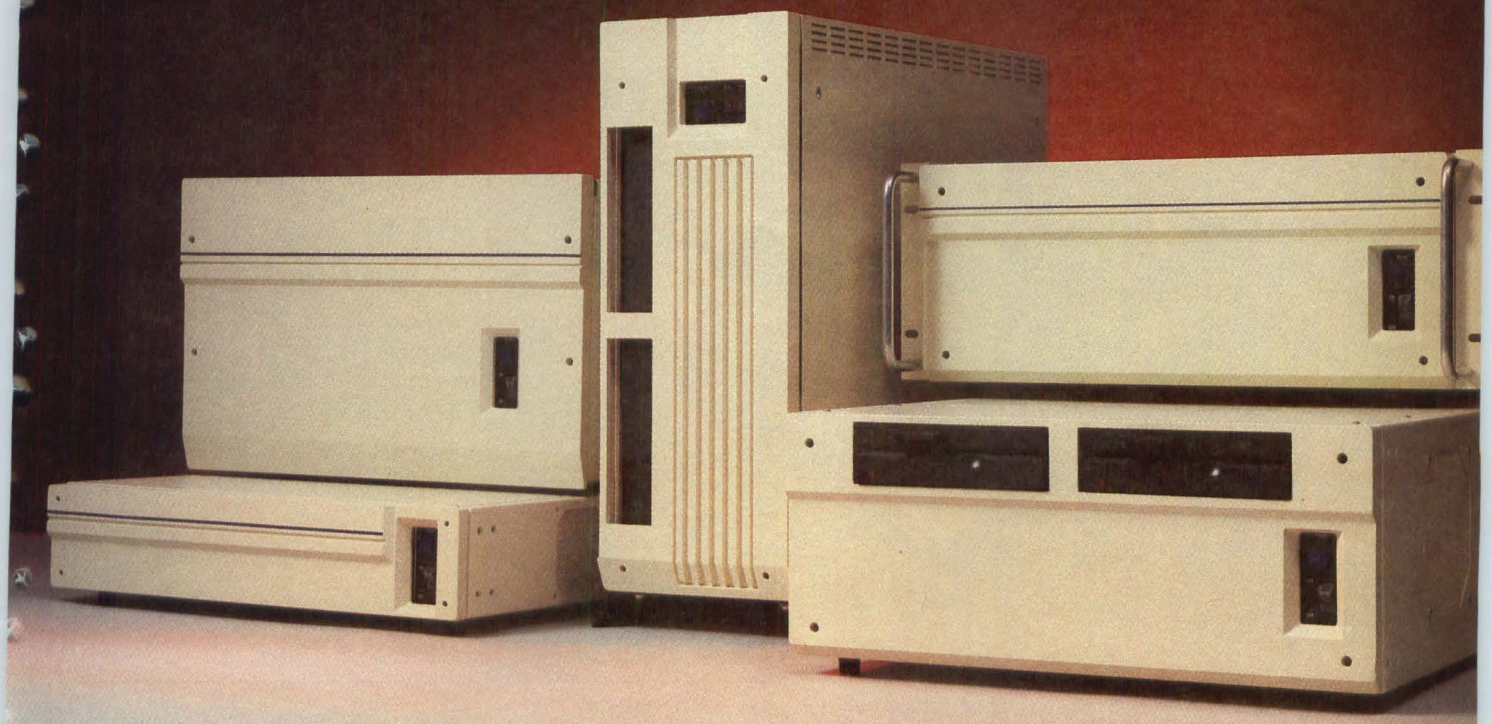


Figure 1: The Mostron PC motherboard includes up to 256 Kbytes of RAM.

# Multibus/VMEbus

# PACKAGING THAT MAKES THE DIFFERENCE



Now there's a complete, integrated line of Multibus™ and VMEbus system enclosures that lets you match your system needs today — with the flexibility to expand or reduce your requirements in the future.

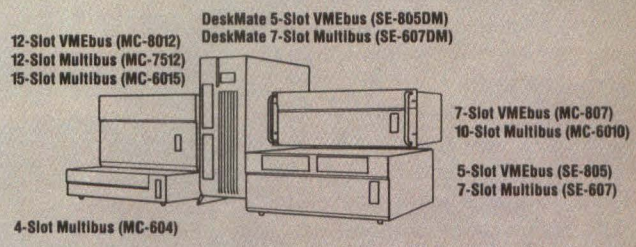
For Multibus, choose from visually-compatible 4, 7, 10, 12, and 15-slot enclosures with Multi-Cage® card cages and backplanes, all designed to meet FCC class A EMI/RFI requirements with typical systems installed. The 7-slot upright DeskMate™ and the 7-slot tabletop models have room for two half-height 5¼" peripherals, plus an additional 5¼" full height Winchester drive. All but the DeskMate are available for rack mounting.

For VMEbus, there are 5, 7 and 12-slot models, with peripherals available on the DeskMate, rack mount and tabletop 5-slot versions. All use Electronic Solutions' VMEasy™ card cage and backplane design for rugged, reliable card mounting and easy servicing. If you're into Multibus now, you can even convert your enclosures later for VME.

Talk to us about your unique requirements. Build upon the industry's most comprehensive system of Multibus and VMEbus enclosures, and reduce your lead time to market. We'll provide front or rear card loading, or special slot spacing, special power supplies, or I/O connections. See how our custom design gives you an entire enclosure line instead of a single box.

Electronic Solutions' entire line is backed by our three year limited warranty—your assurance of built-in reliability.

Call us today, and find out how Electronic Solutions can make the difference in *your* system packaging.



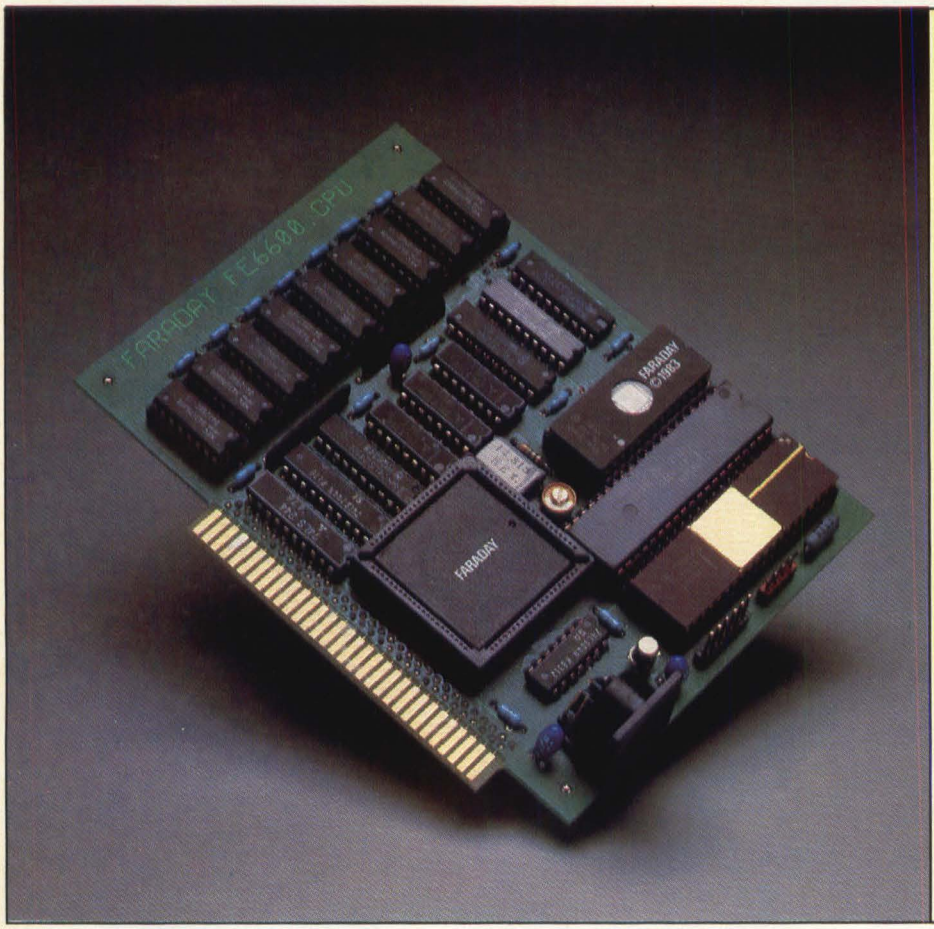

**Electronic Solutions**

9255 Chesapeake Drive, San Diego, CA 92123 • (619) 292-0242 Telex II (TWX): 910-335-1169

**Call Toll Free: (800) 854-7086** In Calif: **(800) 772-7086**

See Us At Mini Micro Northeast Booth 316-318

Circle 15 on Reader Inquiry Card




| Part | Quantity |
|---|---|
| 8288 | 1 |
| 8259A | 1 |
| 8284A | 1 |
| 8237-5 | 1 |
| 8253-5 | 1 |
| 8255 | 1 |
| Delay Line | 2 |
| 74LS280 | 1 |
| 74LS373 | 1 |
| 74LS245 | 2 |
| 74LS175 | 2 |
| 74LS138 | 5 |
| 74LS244 | 3 |
| 74LS670 | 1 |
| 74LS322 | 1 |
| 74LS125 | 1 |
| 74LS10 | 1 |
| 74LS20 | 1 |
| 74LS04 | 2 |
| 74LS02 | 2 |
| 74LS74 | 3 |
| 74LS30 | 1 |
| 74LS00 | 2 |
| 74LS08 | 2 |

Figure 2: Faraday's Micro PC: 39 LSI and MSI parts have been integrated into a gate array.

The second, from Advanced Computer Solutions International (Dallas, TX), includes 1 Mbyte of RAM and can support up to four floppy drives and a SASI hard disk interface. Six expansion slots are provided.

Creating a third alternative, Faraday Electronics (Sunnyvale, CA) has taken the level of integration of the IBM PC motherboard to its limit by using a 6000-gate array. The array has allowed no fewer than 39 conventional packages to be integrated onto a single device (**Figure 2**). Hence, Faraday's board product, the micro PC board, contains only 23 active devices, including the gate array, 8088, 8087 64 Kbytes EPROM for the BIOS, 256 Kbytes of RAM and some buffers.

While the majority of STD manufacturers have not seen much competition from these products, it is likely that they will in the future. Most, however, point to the ungainly form factor of the PC add-in boards as a deterrent to some OEMs in the industrial and process control fields.

Obviously, the STD market is not likely to disappear overnight. In fact, the

**CMOS BUS COMPARISON**

| BUS | CMOS STD | CIM BUS | C-44 |
|---|---|---|---|
| Processor Supported | 80C85-A<br>Z80C<br>80C88<br>NSC800 | NSC-800 | NSC-800<br>80C85 |
| Data Width | 8-bit<br>(16-bit being defined) | 8-bit | 8-bit |
| Address | 20-bit | 20-bit | 8-bit |
| Supporting Manufacturer | >160 | <10 | <5 |
| Card Size (Inches) | 4.5×6.5 | 3.9×6.3 | 4.5×4.733 |
| Temperature Range | −40 to +85°C | −40 to +85°C | −40 to +85°C |
| Connector Type | Edge card or optional pin and socket | Inverse DIN 41612 | Edge Card |
| NMOS/TTL Equivalent cards | Yes | No | No |
| Signals buffered onto the bus | Yes | Yes | No |
| Pins on the Bus | 56 | 64 | 44 |

Table 1: A comparison of CMOS bus structures.

advent of the STD CMOS standard is creating a unique market for the bus. Although such bus structures as National Semiconductor's CIM bus (Santa Clara, CA) and the C-44 from Onset Computer (Falmouth, MA) have offered solutions for some time, the marketshare of these buses is relatively small compared with that of the STD. A comparison of the three bus structures is shown in **Table 1**.

Several vendors currently offer CMOS STD cards. Prolog (Monterey, CA) has a minimum of nine in their catalog. Win Systems (Arlington, TX) offers no less than 16 cards. Analog Devices (Norwood, MA) plans to introduce four new STD I/O cards using both analog and digital CMOS parts. The family consists of the RTI-1280, a 12-bit analog input card; the 1281, a 12-bit combination analog I/O card; the 1282, a 12-bit 4- or 8- channel analog input card; and the RTI-1287, a digital CMOS input/output card. Many of the CMOS CPU vendors, including Win, Prolog and Microcomputer Systems (Baton Rouge, LA), have used the 80C88 processor from Harris in their CPU designs, allowing the OEM to develop software for their designs on the IBM PC.

One criticism about the STD bus is that it does not conform to a standard Eurocard connector. To address this issue, the STD Manufacturers' Group has recommended the AMPMODU Interconnection System as a standard practice. This design methodology means that the systems integrator is not required to pay the excess cost of pin and socket connectors for every board if the application does not justify it. Since the AMPMODU connectors are soldered to the existing card edge connectors, the system integrator only buys what he needs and the compatibility of all STD cards are retained.

Another criticism of the STD bus is that it is unsuited to support the latest generation of 16-bit devices since it was originally designed for 8-bit processor support. This has left a gap in the marketplace for a board-level product with a small Eurocard format which can support both 8- and 16-bit products.

Gespac (Mesa, AZ) hopes to fill that niche with its G-64 range of cards. At the present time, the company offers over 85 boards to the marketplace and is currently negotiating second source agreements with two large US corporations. Recently, Gespac extended the capabilities of its G-64 bus by using a 96-pin DIN connector instead of the original 64-pin connector. This improved version of the bus, dubbed the G-96, is backwards compatible with all the existing G-64 products. The additional 32 lines to the original bus have been implemented to improve the bus' direct addressing capability, to increase the total number of interrupts and to provide a simple multiprocessing arbitration scheme.

As the price of board-level products continues to fall, they become an even more attractive solution to the industrial OEM. This is especially true at the low end of the market which may change structurally over the next few years due to the competition from IBM PC clones.

***—Wilson***

第五代

The transliteration of these three Japanese characters (or kanji) is dai go dai, this translates as "the fifth generation."

# Artificial Intelligence And The Fifth Generation

**by Gregory MacNicol, West Coast Technical Editor**

In laboratories worldwide, a new generation of computers is under development. Researchers are moving beyond conventional Artificial Intelligence (AI) software development to computer architectures specifically designed for AI applications. In the short term this will result in improved natural language processing, speech and image recognition and expert systems. In the long run it may result in true machine intelligence.

The research that started in US universities gained momentum with the announcement of Japanese efforts to produce fifth generation computers. AI research and product development has spread to American companies and European laboratories. But the Japanese remain the ones to watch, as they pursue their goals with the most focused program in the world. Their goal is to develop computers with human-like intelligence that will be able to understand speech and pictures. Japan's fifth generation group plans computers that can learn, associate, make inferences and make decisions. Parallel fifth generation computer developments incorporate new IC technology that includes fabrication of submicron architecture and three-dimensional chips.

Motivation for developing the next generation of computers is in part driven by a feeling among computer scientists that von Neumann structure, dominant in computer architecture for 40 years, is approaching the limits of its usefulness. Von Neumann architecture requires a large amount of software development time and effort, and the machines require humans to adapt to the computer rather than vice versa.

The basic ingredients for a new architecture are available. They have been researched and published but not integrated. Similarities in logical structure are apparent in several separate disciplines of computing technology: AI, relational database architecture and dataflow machines. New theories in linguistics

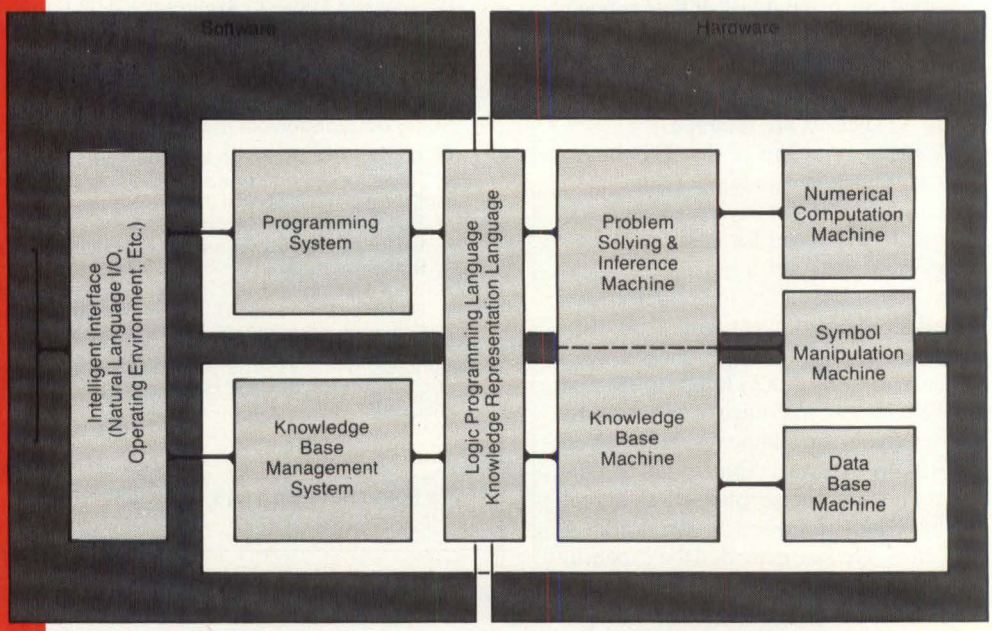



Figure 1: In this diagram of a knowledge-based system of the fifth generation, segregation between software and hardware is shown. The system is to be organized as a continuation of a relational database machine and a parallel processing machine for relational algebraic computation.

# CAD without CACHE™ is like life without water.

Now CACHE brings the CAD design process to life with the information you need. No more long dry spells while you wait for your CAD Library to be created. CACHE offers the design engineer a comprehensive component library of standard and semi-custom IC's that support logic design and physical layouts for engineering workstations and turnkey CAD systems. With the information from CACHE at your fingertips, you can shorten your design path, reduce design costs and improve productivity. So learn how to breathe new life into CAD with CACHE. Call us or send in the attached form today.

**Tell me more about how CACHE can add life to my CAD system.**

Name _____

Title _____

Company _____

Address _____

City _____ State _____ Zip _____

Send to: **INACOM International, 4380 South Syracuse Street, Denver, Colorado 80237**

Call: **1-800-443-INFO**
**303/694-4200 (Within Colorado)**

INACOM International

COMPUTER AIDED ACCESS™
We go right to the source.

**Circle 19 on Reader Inquiry Card**

suggest similarities between the logical structure of language and those three fields as well. The fifth generation project plan is to synthesize these technologies into one concept.

## The Japanese Strategy

The Japanese Ministry of International Trade and Industry (MITI) incited great interest in the next generation with their 1982 announcement and formation of ICOT, the Institute for New Generation Computer Technology. Armed with $450 million seed money over a 10 year period and ambitious plans, ICOT is coordinating AI development with major Japanese firms.

Japan's strategy rests on a desire to be more self-sufficient. Despite a shortage of land and natural resources, Japan intends to use their largest asset – people – to cultivate information as a new resource comparable to food and energy.

The project was conceived by a group of scientists led by Kazohiro Fuchi, a prominent Japanese computer scientist. Fuchi was the principal designer of the fifth generation architecture and was a key force behind adoption of the program.

Japan's fifth generation computer project should not be confused with their supercomputer project. Supercomputers use new architectures for performing fast numerical operations, whereas the fifth generation project will develop high performance logical engines utilizing AI to augment human intelligence. In other words, supercomputers are optimized to deal with data in contrast to symbols.

The list of those involved in the fifth generation program includes Fujitsu, Hitachi, Nippon Electric Company, Toshiba, Mitsubishi and most leading Japanese academic, government and industrial institutions. IBM intended to join, but later withdrew.

A standing requirement for participation is sharing the results of research among members. The Japanese have required similar sharing of technologies on projects in the past. However, companies that made discoveries sometimes kept the information secret from the other participants. This could potentially happen again in the fifth generation project.

Although most coverage of Japan's fifth generation project has focused on the use of AI in the future system, it is only one component of the project. The other primary components are relational database architecture and dataflow or parallel processing. Much of the research in these areas has already been done. IBM, in fact, pioneered relational database architecture but abandoned it in favor of extending the 370 line.

When defining the project, the Japanese task force realized that they needed to research several technologies before creating a new architecture:

- The basic mechanism of inference, association and learning.
- Preparation of AI software.
- Hardware and software control of the database.
- Maximizing the man-machine relationship.
- Software tools that enhance development.

In addition, peripheral subjects such as knowledge representation, inference operations, knowledge acquisition and dataflow hardware must be understood.

The core of Japan's fifth generation project is an inference machine. The initial milestone in the plan is a single-user workstation capable of performing one million logical inferences per second (LIPS). One LIPS is roughly equal to between 100 and 1000 instructions per second. The 1M LIPS prototype workstation is targeted for completion this year. This is an intermediate step toward the goal of a machine to perform at one billion LIPS, which will require a departure from von Neumann architecture.

An integral part of the prototype workstation, the Personal Sequential Inference engine (PSI) will provide researchers with a programming development system. Kernel Language Zero (KL0) will replace the Prolog language used cur-

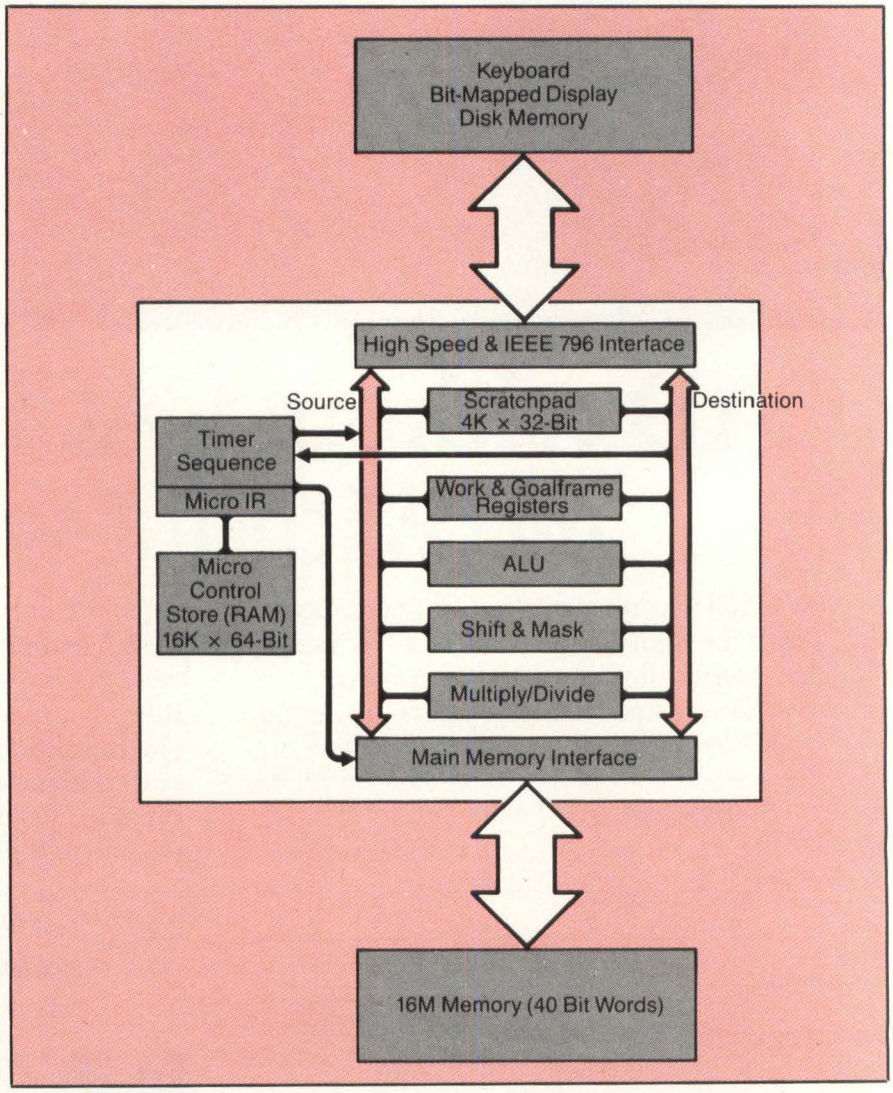
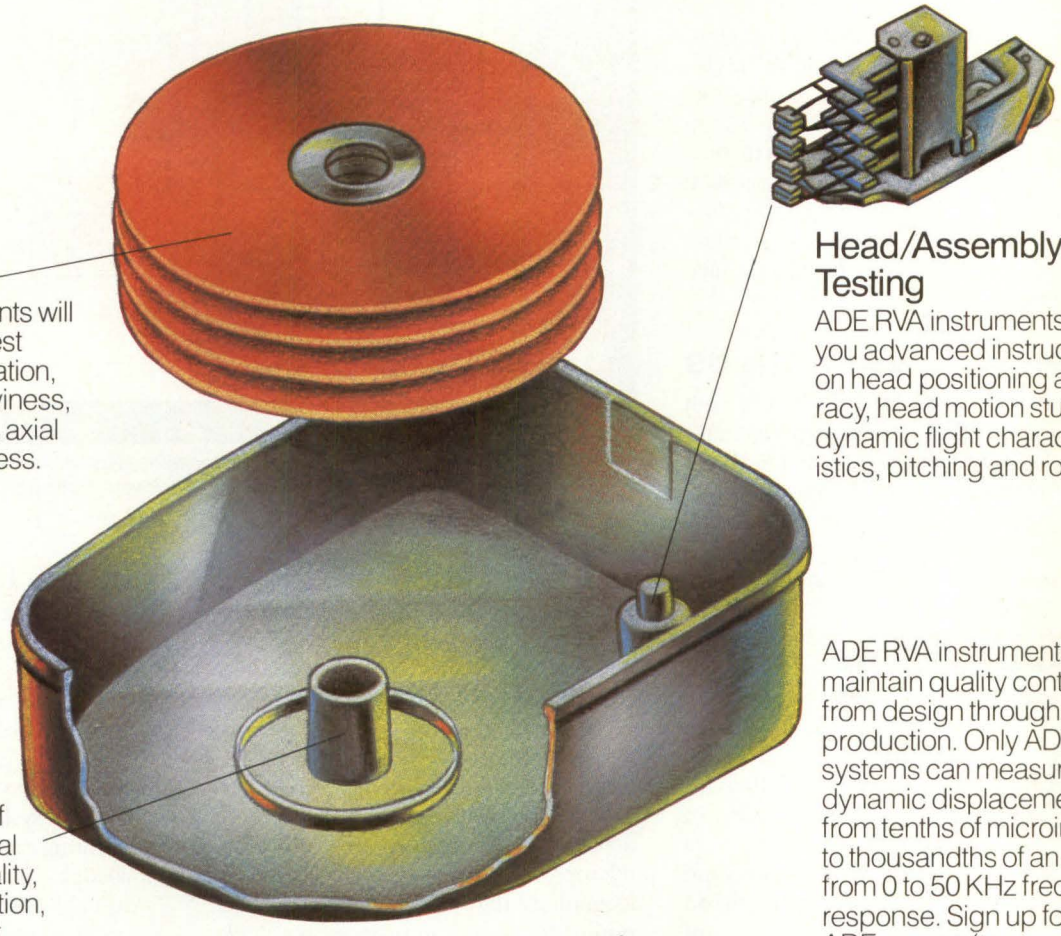



Figure 2: The first version of a Parallel Inference Engine uses depth-first or breadth-first strategies depending on the problem.

# A CRASH COURSE IN DISK AND DRIVE TESTING:





## Disk Testing

ADE RVA instruments will show you how to test excessive acceleration, flatness, radial waviness, datum positioning, axial run-out and thickness.

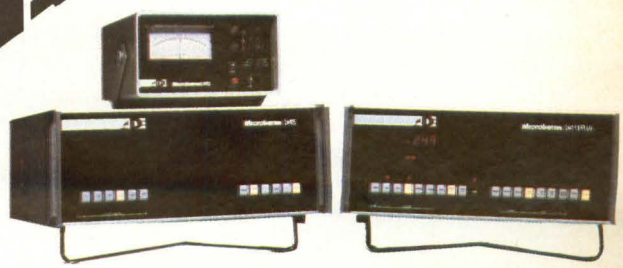
## Head/Assembly Testing

ADE RVA instruments give you advanced instruction on head positioning accuracy, head motion studies, dynamic flight characteristics, pitching and rolling.

## Spindle Testing

Learn the nuances of testing axial and radial runouts, bearing quality, axial/radial acceleration, non-repetitive runout, radial resonance, wobble, and high frequency vibration.

ADE RVA instruments maintain quality control from design through production. Only ADE systems can measure dynamic displacements from tenths of microinches to thousandths of an inch from 0 to 50 KHz frequency response. Sign up for the ADE course (every major manufacturer of disks and drives already has).




**ADE Corporation**
77 Rowe Street
Newton, MA 02166
Telephone: (617) 969-0600
Telex: 922415


**Circle 29 on Reader Inquiry Card**

rently. Execution time is 200 nsec per instruction, using 40-bit words. A word consists of 32 data bits, with the remaining 8 bits for garbage collection, tags and defining several data types.

Studies on parallel simulation have been conducted, specifically in the area of structured data sharing. Conventional computers were used to evaluate the process. The hardware, which is a parallel processing system called Paralog, has been designed and tested. The language specifications are based on pure Prolog statements and are executed in a breadth-first manner as opposed to depth first. The results indicate that execution time increases linearly with the number of processing modules.

The next major task is the parallel inference engine (PIE). While the architecture is well defined, there are some issues to resolve. The fetch operation may be too slow in conjunction with time losses due to marking and decomposition of information for unification and reduction. There is also a potential problem of reduced efficiency due to garbage collection.

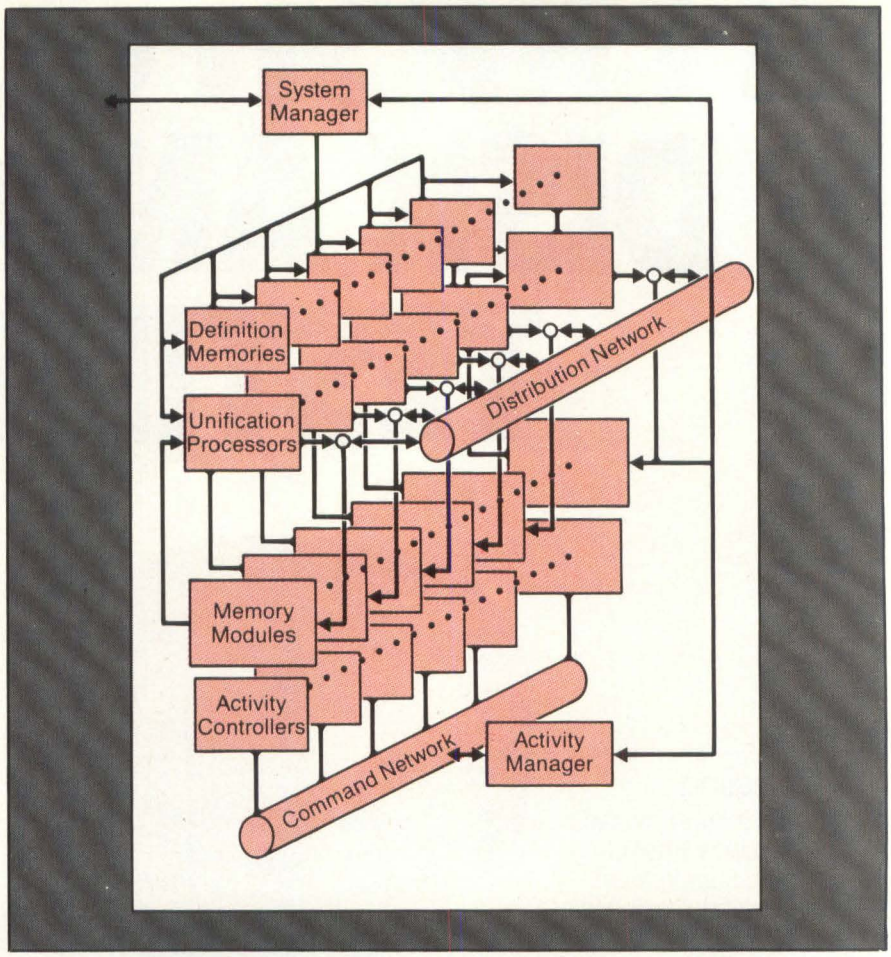



Figure 3: The Personal Sequented Inference machine is intended to provide researchers with a programming environment for the development of software. It can process 16 million 40-bit words.

## The Players—AI In The US

A major force in the US effort in fifth generation machines is the government. The National Science Foundation (NSF) is requesting $500 million over a three year period to provide basic academic research computing facilities. The NSF would like to see at least 10 supercomputers devoted exclusively to AI research. Furthermore, the Navy and the Air Force have committed themselves to working on all levels of AI.

DARPA (Defense Advance Research Projects Agency) has the most ambitious fifth generation effort in the US. The Strategic Computing program of DARPA requested $600 million over a five year period. The program's overall goal is to provide the US with a broad range of machine intelligence that will greatly increase national security and economic power. The investment for 1984 was $50 million, which constituted 20% of the Department of Defense's total commitment in science and technology for that year.

The program calls for a cooperative effort of industry, the government and universities. It has three goals: the creation of autonomous two-ton vehicles with machine vision, large scale battle management systems and a pilot's assistant device that aids aircraft control. Sponsors hope such applications will stimulate progress in expert systems, speech recognition, natural language understanding and machine vision.

Supporting research is in such areas as GaAs technology, packaging, CAD/CAM and quick prototyping. DARPA has awarded Texas Instruments (Dallas, TX) a $6 million contract to develop a Lisp microprocessor chip. Using sub 2-micron technology, the chip will have over half a million transistors and operate at a clock rate of 40 MHz.

Work being done at Stanford Research Institute (SRI) (Menlo Park, CA) is another major effort in the US. With over 40 people directed by Nils Nilsson, a leading AI researcher, SRI is focusing primarily on three issues: natural language, perception and representation of reasoning.

While natural language is an important and obvious issue for the man-machine interface, perception is an extension of the human process of comprehension. An important quality of perception is the ability to extract intrinsic information from an image such as surface and texture. Representation and reasoning are the problems encountered in expert systems where associations and relationships are used to solve problems. Developing expert systems has been easier than representing common sense or common knowledge.

Although SRI is not involved in specialized hardware for testing AI concepts, they will use a robot created with goal planning, natural language processing, reasoning, expert tasking and machine vision. All of this is to be designed around multiple 68000s and other available hardware.

There is considerable cooperation between industry and universities in the US. SRI, for example, keeps close ties with Stanford University. In 1983 Stanford established the Center for the Study of Language and Information (CSLI),

# New PC Enhancer "Message Centers" now available in up to 4-line, 96 characters

**F. A. Amendola**
Cherry Electrical Products Corp.
Waukegan, IL

## New Cherry units provide space for messages from 24 to 96 characters. Diagnostic and operator prompting for programmable controller in understandable English.

The programmable controller in your plant may be able to signal when a problem is occuring or is about to occur. However, that signal, in the form of complicated codes is understandable only to a technician who is familiar with and has access to that code.

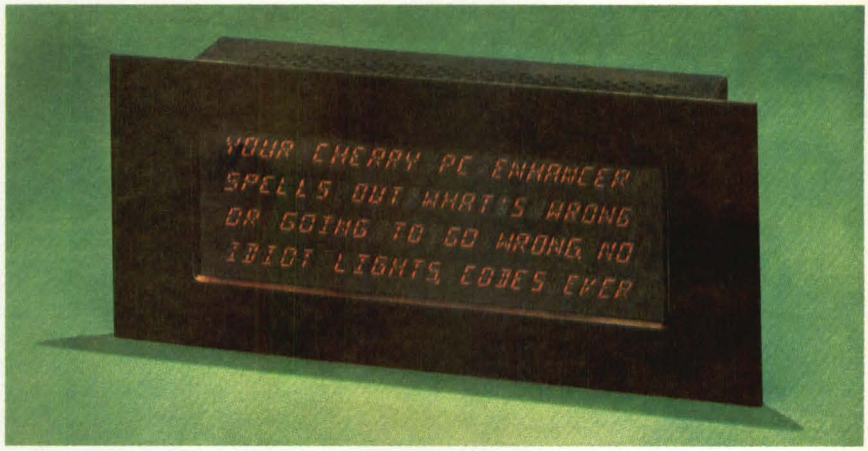
The new line of Cherry PC Enhancers—"The Message Centers"—can change that situation into one in which anyone can read a diagnostic or operator prompt message and act upon it. The result is immediate action and less down time.

## Bigger Display panel... longer messages

For systems where more detailed messages are desired, the W424-4040 is a 4-line, by 24 character—96 character total—alphanumeric gas discharge display system. It has the ability to display any of the 256 messages—up to 32 characters each—that have been stored in a non-volatile, battery powered CMOS RAM. Because the messages can begin at any frame, longer messages can be created by butting sequential messages end to end.

The display itself is in large .5 inch, 14 segment characters. The bright orange neon is readable even in direct sunlight. For different lighting situations, five levels of variable brightness are provided via ASCII control codes.

Messages may be loaded into the display system through the parallel or serial port, either from an optional ASCII keyboard (Cherry Model No. V1NV-0112) or downloaded from a host computer or terminal. Real-time variable data can be displayed along with the stored messages and updated continuously.




**Keyboard Input Instructions** for Cherry W424-4040, 4-line, 96 character Message Center with full alphanumeric capabilities. **To enter program (message):**

| **KEYBOARD ENTRY (ASCII)** | |
|---|---|
| **Control Y** | **(Learn)** |
| **HEX 1 4 5** | **145 (Message Number 145)** |
| (Readout Line 1) | SAFETY GUARD OPEN. |
| (Readout Line 2) | TO RESTART MACHINE |
| (Readout Line 3) | CLOSE SAFETY GUARD. |
| (Readout Line 4) | PUSH RESET BUTTON. |
| **Control Y** | |
| **Carriage Return** | |

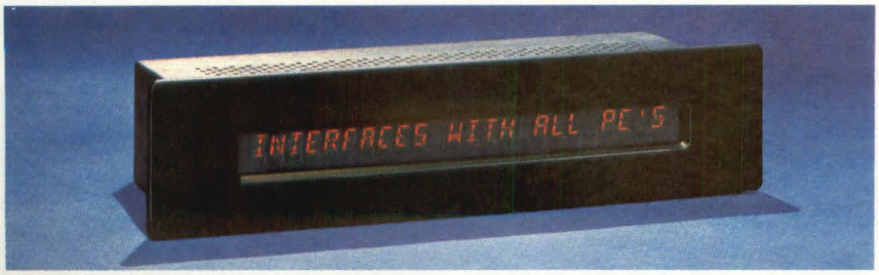
The W424-4040 is a self-contained PC Enhancer. It comes in a front mountable metal enclosure with a sealed, diecast bezel that is compatible with NEMA 12 specifications. For easy access when programming or updating, all signal and power connections are screw terminals on the back. The W424-4040 will operate with a 115/230 VAC power source.

## Single Line Message Centers Complete the Lineup

Not all systems require a Message Center with a 96 character display. Therefore two single line display Message Centers have been developed. Each one is self-contained in front mountable metal enclosures with sealed diecast bezels compatible with NEMA 12 specifications.

The W424-105B is a 24 character display system that has been designed to be interfaced with programmable controllers and other devices that provide an ASCII output.

The W424-105D is a more sophisticated model with the ability to store up to 256 messages. Each message can be up to 32 characters in length, with messages longer than 24 characters being scrolled. Virtually all of the features available in the 4-line display.




**Cherry W424-105D can store 8,000 characters in memory for operator prompting.**

See Us At ELECTRO/NY, April 23-25, 1985, CHERRY BOOTHS 2036-2042

## Write for complete specs.

Instructions and application information are available from Cherry now.

CHERRY

**CHERRY ELECTRICAL PRODUCTS CORP.**
3631 Sunset Avenue
Waukegan, Illinois 60087
312/578-3500

**Circle 9 on Reader Inquiry Card**

where people from SRI work part time. Symbolics (Cambridge, MA) has close ties with MIT.

Common Lisp is the result of cooperation between corporations such as DEC (Maynard, MA), TI, Symbolics, Lisp Machines Inc. (Los Angeles, CA) and universities including MIT, Yale and Carnegie-Mellon. ARPANET has been used for communications, and many of the discussions and proposals occurred through this medium. As a result of this dialog, Common Lisp's capabilities have grown and it is used on computers from the IBM PC to the VAX.

US joint efforts for R&D were cleared on May 1, 1984 when the House of Representatives approved the Joint Research and Development Act (HR 5041). The bill is designed to clarify issues surrounding antitrust legislation and relieve obstacles to the formation of joint research efforts. As a result of the bill, firms participating in the Microelectronics and Computer Technology Corporation (MCC) (Austin, TX) can pool resources and technology without threat of breaking antitrust laws.

## The European Effort

It would be inaccurate to say that European fifth generation projects began after the Japanese announcement. The ICOT project in Japan has certainly been a catalyst for governmental awareness, but AI efforts have been under way for years in Europe. The language Prolog, for example, was invented in France and refined in England.

The British fifth generation program is very impressive but takes a different approach than other programs. Central to their plan is the integration of one million devices on a single silicon chip by 1989, using only native technlogy. The development of five semiconductor fabrication technologies that can be used to implement submicron architecture will involve 15 companies, 24 universities and other laboratories. Fifteen processes will be used, such as dry etching and microlithography.

Like Japan's fifth generation project, Britain has a prominent scientist setting the strategy. John Alvey, Technical Director of British Telecom, was instrumental in creating a £350 million plan for the next generation of computers. The program will cover software engineering, knowledge-based systems, man-machine interfaces and VLSI. Roughly one-third of the development costs will be used for VLSI.

France is active in fifth generation work; however, there is no grand cooperative plan unifying the efforts. Several French programs sponsor and structure fifth generation research: the National Projects (PN), the Joint Research Projects (PRC), the National Center for Scientific Research (CNRS and GRECO) and the Thematic Research Program.

The PN is involved in initiating projects such as VLSI and CAD tools, software engineering, automatic translation, display hardware and the basic components for AI products. PRC is essentially a technology transfer program to bring together the various small, scattered research groups dealing with fifth generation issues. Some of its focus is on topics such as concurrency, cooperation and communication, fifth generation database management and man-machine communication. Some groups, whose members sponsor projects of their own, mainly enhance the transfer of information between laboratories working in similar fields. Research groups include a speech group, a symbolic manipulation group and an advanced robotics group.

With funding of $9 million in the first year of operation, France's World Center for Information Technology has encountered problems. Recommendations for hardware included acquisition of American-made VAX and Lisp computers that seem unlikely to be purchased since they are built outside of France. Major disputes have hindered operations and many researchers (including Seymour Papert from MIT) have quit.

Efforts of the French government have been less successful than those of companies such as Schlumberger and Elf Aquitaine, who continue to make major strides in applications using AI. Schlumberger, owner of Schlumberger-Doll (Ridgefield, CT), and Fairchild (Palo Alto, CA), use the technology for oil drilling and exploration. Elf Aquitaine also works with American companies developing expert systems.

With the current interest in fifth generation computers, Germany is also starting to make plans. In March 1984, the federal research minister presented a report stating that the development of future computing systems is essential for Germany to be competitive with the rest of the world. Of the three primary strategic areas, one is focused on AI. The most important subjects are knowledge engineering, pattern recognition, expert systems for technical service and support and knowledge-based man-machine communication.

Concern over the possibility that they may lag behind in the technology of the next decade has led the Europeans to form ESPRIT (European Strategic Programme for Research and Development in Information Technology). The overall objective of ESPRIT is to provide the basic technologies by fostering "precompetitive" technological research. However, ESPRIT funds industry proposals by a maximum of only 50%. This is in contrast to a well-thought-out and financed plan by MITI in Japan and DARPA in the US. Major objectives of ESPRIT include standardization and unification of software efforts.

## Fifth Generation Status

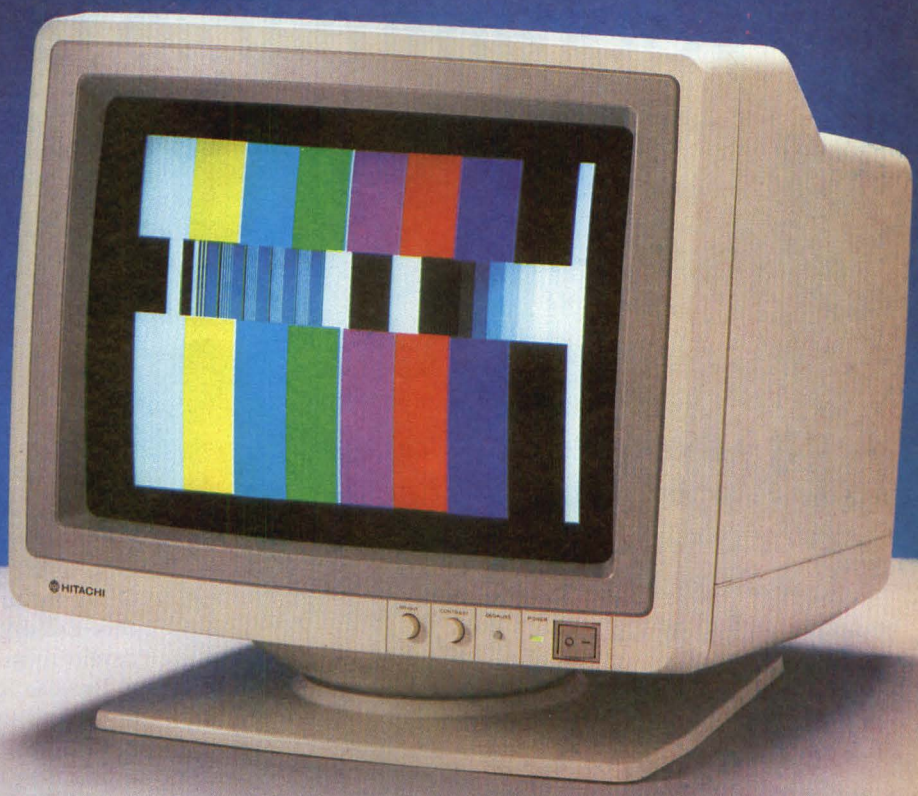
Some clear successes have resulted from the first phase of the Japanese fifth generation research. The design of the PSI is finalized and prototyping is in progress. The remaining architecture offers good support for a logic programming environment.

Momentum is beginning to build in artificial intelligence and next generation research projects in other parts of the world as well. With cooperation between universities, industry, government and military in the US and Europe as well as in Japan, advances may be expected on all sides.

One of the most remarkable features of the proposed fifth generation architectures is that they are building on existing technology. Developments are focused on AI, relational databases and architectural innovations like dataflow and parallel processing, as well as semiconductor technologies to support advanced processing. If the goal of focusing and unifying these technologies into a singular concept is achieved, the projects will be a success. DD

# HITACHI'S NEW BREAKTHROUGH IN 1280 x 1024 19″ COLOR MONITORS:

# THE BEAUTY IS MORE THAN SKIN DEEP.




Now there's an ultra high resolution monitor that combines state-of-the-art technology, ergonomic cabinetry and decisive clear cut price advantages. It makes sense to switch!

Hitachi's new 19″ color monitor gives you high-speed horizontal scanning (both 64 KHz *and* 32 KHz), flickerless vertical scanning (60 KHz non-interlaced), wide band video circuitry (100 MHz @ 3dB down), .3mm misconvergence specs, plus a newly developed large diameter lens, precision gun and dynamic focus circuit for the sharpest, brightest picture in the business.

It's part of a full line of color and monochrome monitors from one of the largest, most highly automated manufacturers on earth. And along with size comes a level of R&D resources that have made Hitachi a world leader in technology to reduce glare, sharpen picture clarity and improve color registration — all at very competitive prices.

Call NSA for complete details.

## HITACHI: THE DECIDING FACTOR.

NSA

NISSEI SANGYO AMERICA, LTD.

Boston: 40 Washington Street, Wellesley Hills, MA 02181, (617) 237-9643
San Francisco: 460 E. Middlefield Road, Mountain View, CA 94043, (415) 969-1100

Circle 18 on Reader Inquiry Card

# Programmable Logic Soars Into New Dimensions

by Ronald Collett, Sr. Technical Editor

**By the end of the decade, application-specific integrated circuits (ASIC) will be the primary building blocks of printed circuit board design.**

Pre-configured off-the-shelf chips will no longer satisfy the performance, functionality and tight space requirements of tomorrow's systems. Until now, gate arrays received the most attention in the ASIC arena, with programmable logic devices (PLD) taking a backseat. However, this is rapidly changing as new technologies and architectures are setting the stage for PLDs to rival gate arrays.

In-house programmability is the primary advantage PLDs have over gate arrays. An uncommitted array that can be transformed into an ASIC in the lab provides the designer with his own silicon foundry. In contrast, gate array designs require the designer to depend on the gate array vendor throughout the design cycle.

PLDs have, however, continuously drawn strong criticism in several areas. First, their basic AND-OR array structure is too confining for many designs, even though any Boolean functon can be represented as a sum-of-products (SOP). Early PLDs had neither registered outputs nor feedback, which are required for state machine design. Even with these features, many new PLDs force the user to adapt to the device's rigid structure.

Programmable logic has also been inadequate for constructing arithmetic logic operations (i.e., add, subtract, divide) since most PLDs do not have the many XOR operators typically required. Some devices include XOR gates, but often too few to implement complex arithmetic logic.

Since PLDs have been confined to bipolar technology, another criticism has been the tradeoff between speed and functionality. Higher performance and increased functionality (i.e., more logic) both demand additional power. As a result, PLD die size and packaging dictate the tradeoff. Manufacturers have been reluctant to expand the package sizes of these devices because traditional 20-, 24-, and 28-pin packages provide an advantage over the large packages of many other high-functionality ASICs.

The third attack made on PLDs was their silicon inefficiency. Because PLDs are programmed by blowing fuses, wasted gates are inherent. A fourth criticism is that the chips cannot be fully tested after fabrication. The only way to check whether all gates are functional is to burn the fuses and exercise the logic. However, full testing is not possible because once the fuses are blown, the device is committed. In some cases, three to five percent of all devices shipped to a customer are flawed. And finally, development software to program PLDs confined the designer to Boolean equations.

Even though designers can maintain full control over the design cycle, these deficiencies have allowed other ASICs to overshadow PLDs. Realizing the user's reluctance to use programmable logic, manufacturers and software vendors are providing solutions to many PLD shortcomings.

## Architectural Considerations: Then And Now

Since any Boolean function can be implemented as SOP, PLDs are composed of an AND array whose outputs feed an OR array.

PHOTO COURTESY DATA I/O

# Suddenly, everyone's headed for MARS.

**The MARS-432 32-bit, programmable, floating point array processor.**

*And with good reason. Because the MARS-432 has opened up a new world of speed, power and ease-of-use that's hard for anyone to resist.*

*The MARS-432 already interfaces with some of this world's leading computers — DEC, Apollo, Elxsi — to provide users with a new level of computational power. Interfaces for other leaders such as IBM, Perkin-Elmer, and Gould/SEL are scheduled to arrive soon.*

*Simply put, we're setting the direction in state-of-the-art array processors with features such as:*

## Programming Ease

*All of the computational power of an array processor doesn't mean much if accessing that power requires days of tedious programming, debugging and reprogramming. That's why we engineered the MARS-432 with an architecture specifically designed to support a FORTRAN compiler and a screen-oriented debugging system that make accessing and utilizing its raw power a very civilized process.*

*The MARS-432 also provides:*

- ☐ *A Microcode Development System for off-line program development.*
- ☐ *An AP Run Time Executive Support Package (AREX) for simplified processor initialization, I/O operations, and array function executions.*
- ☐ *Applications Libraries for math, signal processing, and image processing.*

## Speed

- ☐ *Add and multiply times of 100ns.*
- ☐ *Computational power of 30 megaflops.*
- ☐ *Computes a 1024-point complex FFT in 1.7ms.*
- ☐ *DMA transfers at I/O bus rates of 20 megabytes/sec.*
- ☐ *Data memory write or two reads in 100ns.*
- ☐ *Memory paging for uninterrupted processing during I/O transactions.*

## Impressive Memory

*Program memory contains a physical address space of 4K words and a virtual address space of 64K words via a cache configuration. Data memory contains a physical address space of 16 million words.*

*The MARS-432 from Numerix: a journey to faster, more affordable array processing power. With programming ease that sets it worlds apart.*

*Going our way?*

PERKIN ELMER

GOULD/SEL

VAX

MICRO VAX

APOLLO

ELXSI

*For additional information on the MARS Family of High Speed Array Processors, write or call:*

**NUMERIX**

maximum power / minimum effort

*Numerix Corp. 320 Needham Street, Newton, MA 02164-1594 Tel. 617-964-2500.*

**Circle 53 on Reader Inquiry Card**

# SHORT CIRCUIT YOUR STATE MACHINE DESIGN.

Electrifying news for anyone designing logic control systems. Signetics can help you build a powerful state machine in a matter of hours. Using a single circuit.

This is the only efficient way to make a state machine. All you need is one of our Field Programmable Logic Sequencers (FPLS). Write a simple equation, blow its fuses in a programmer, and you have a complete controller on one chip.

You cut down board space and inventory. While increasing the capabilities of your system.

## Short Circuits put you in control.

Our Logic Sequencers are part of Signetics' industry-leading Integrated Fuse Logic (IFL)—informally known as Short Circuits, because of our shockingly simple approach to programming.

In addition to our five FPLS circuits (with more to come), our unique IFL family includes logic arrays and gate arrays.

All of them help you build more quality into your system. For one thing, you reduce your part count dramatically. So you have fewer connections to cause problems. And IFL uses our proven reliable PROM technology. All of which contributes to lower cost of ownership.

With all its advantages, it's not surprising to see our features turning up in other companies' programmable logic. Things like programmable ORs and output polarity, preset/reset flip-flops and preloaded registers for testing.

Of course, these are all part of our original architecture, instead of add-ons. So you don't have to take chances on designs that haven't proved themselves.

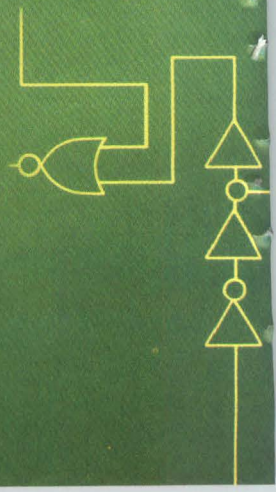
**If the Logic Sequencer fits, use it.**

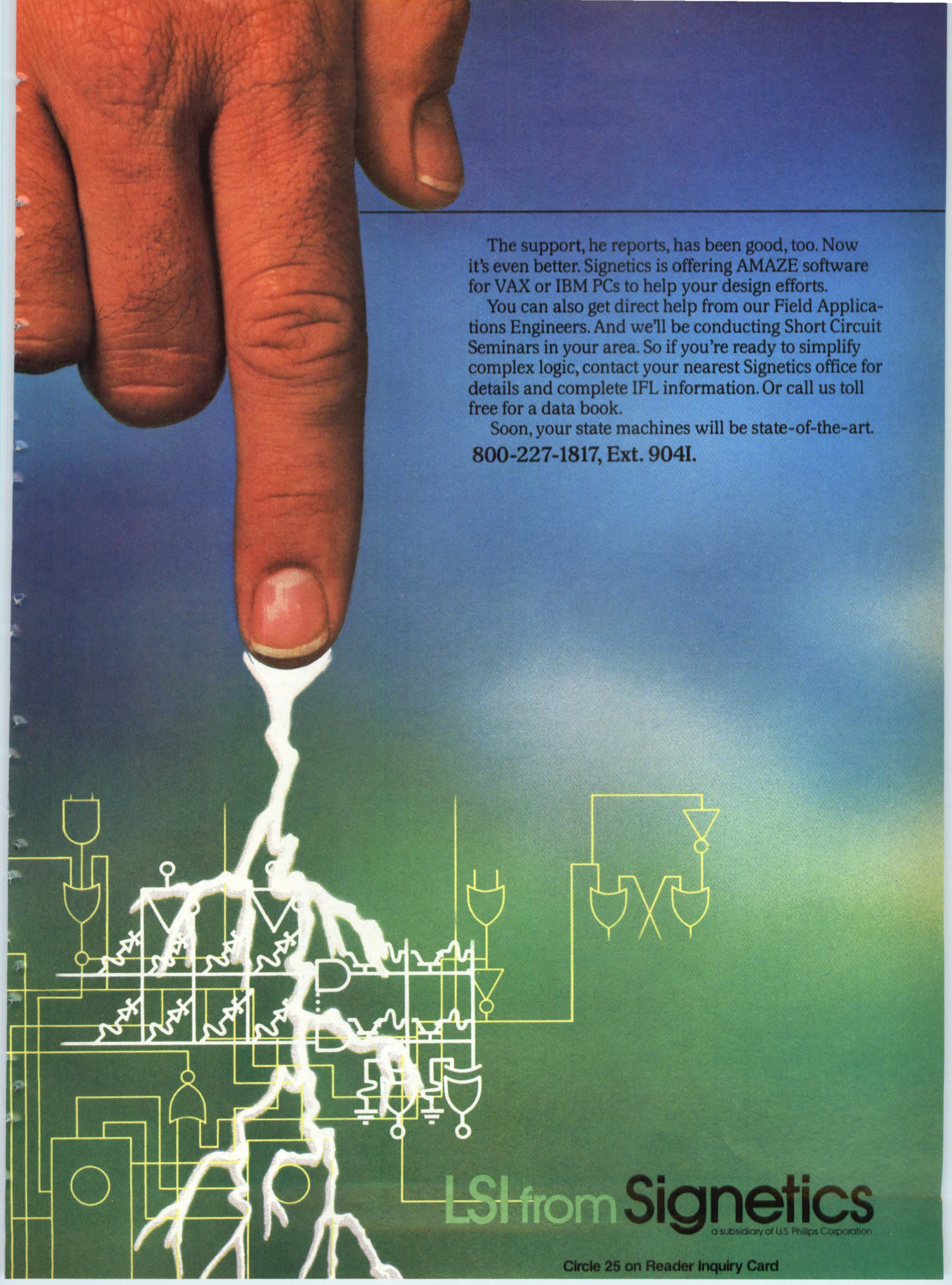
| | |
|---|---|
| 82S105 | 16 input/8 output/48 term with 6-bit state register and 8 output registers. 28-pin package. |
| 82S167 | 14 input/6 output/48 term with 8-bit state register and 6 output registers. 24-pin package. |
| 82S159 | 16 input/12 output/45 term with 8 state registers and 8 output registers. 20-pin package. |
| 82S155 | 16 input/12 output/45 term with 4 state and output registers. |
| 82S157 | 16 input/12 output/45 term with 6 state and output registers. |

## "There's just no competition."

That's the opinion of Art Sobel, Project Manager and Senior Design Engineer at Data Technology. His company makes a whole line of controllers for hard discs and floppies. And he's sold on Short Circuits.

"When you're using the IFL Logic Sequencers to design state machines, it takes about 1/10th the time compared with other programmable logic. Typically, one hour versus two days. And it's easy to change codes with IFL. With other devices, good luck!"





The support, he reports, has been good, too. Now it's even better. Signetics is offering AMAZE software for VAX or IBM PCs to help your design efforts.

You can also get direct help from our Field Applications Engineers. And we'll be conducting Short Circuit Seminars in your area. So if you're ready to simplify complex logic, contact your nearest Signetics office for details and complete IFL information. Or call us toll free for a data book.

Soon, your state machines will be state-of-the-art.

**800-227-1817, Ext. 904I.**

LSI from Signetics

a subsidiary of U.S. Philips Corporation

Circle 25 on Reader Inquiry Card

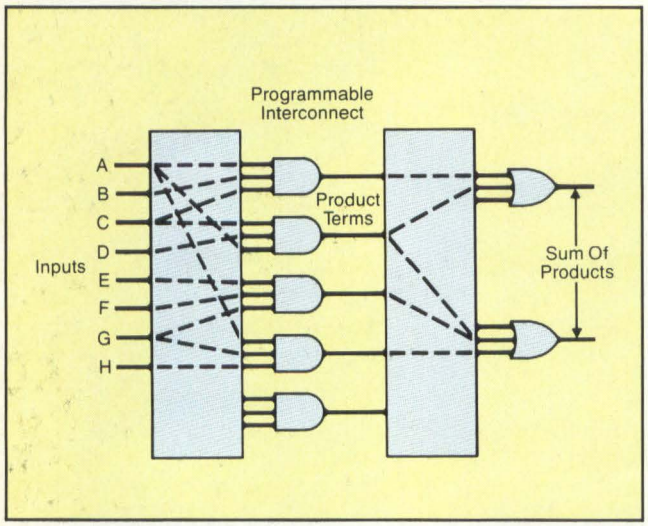



Figure 1: After PROMs were introduced in the early 1970s, field programmable logic arrays (FPLAs) were the first user-programmable ASICs. Both the AND array and OR array are fuse programmable and thus offer product sharing among all outputs.

Early field programmable logic arrays (FPLA), first offered in the mid 1970s by Signetics (Sunnyvale, CA), included both a programmable AND plane and a programmable OR plane, (**Figure 1**). The programmable OR plane allows true product sharing, so any product term can be routed to any OR gate. Having both arrays programmable made these parts very flexible, but far more complex to program. Moreover, the FPLA is slower than other PLDs because signals must propagate through two fuse arrays.

Shortly after Signetics introduced the FPLA, Monolithic Memories (Santa Clara, CA) introduced programmable array logic (PAL). With PALs, the OR array is not programmable (**Figure 2**). Although this limits the device's product-sharing

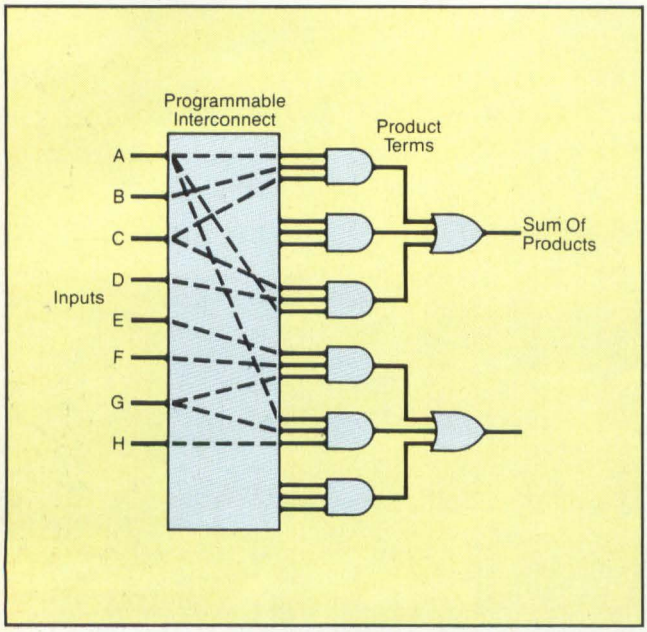



Figure 2: Programmable array logic (PAL) was introduced by Monolithic Memories shortly after FPLAs. Since the AND plane is hardwired to the OR array, device programming is simplified.

flexibility, designers have found PALs far easier to program. These devices are also faster than FPLAs because input signals propagate only through one fuse array. When the PAL was introduced, it included registered outputs together with feedback circuitry, allowing sequencers to be constructed.

Since most PLDs reside in 20- to 28-pin packages, designers are often constrained by the limited I/O. Tri-state outputs, another feature of many PLDs, permit each pin to be used as either an input or an output. Each programmable I/O pin is controlled by a product term, while the remaining terms are summed. In addition, the summation can be fed back to the AND array (**Figure 3**). This allows a single pin to be used as an output when the tri-state output is enabled. The I/O pin can be used as an input to the array when the tri-state output is disabled. Moreover, in registered devices, the OR-gate summation can be simultaneously used as an output and fed back to the AND array input. This allows the device to execute functions including count up, count down, skip, shift and branch.

As mentioned earlier, some PLDs include XOR gates for arithmetic functions such as addition, subtraction and comparisons (**Figure 4a**). The XOR feeding the D-type flip-flop permits data from the previous operation to be carried over and XORed with two variable sums generated by the PLD array (a

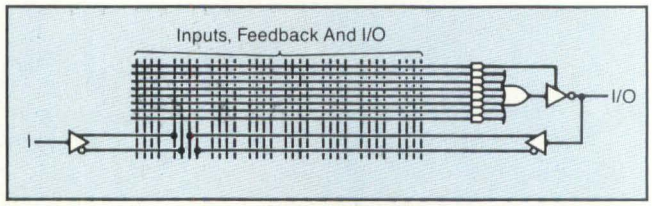



Figure 3: Programmable I/O permits a pin to be used as both an input and output. One product term is used to enable and disable the tri-state buffer. This is useful for allocating available pins for I/O functions or to provide bidirectional output pins for shifting and rotating data.

PAL in this example). The flip-flop output is then fed back to be gated with input terms (B). This gated feedback provides any one of the 16 Boolean combinations shown in **Figure 4b**; the figure also illustrates how the PAL array can be programmed to perform these operations.

Some manufacturers, such as Signetics and, more recently, Monolithic Memories, incorporate a fuse programmable 2 input XOR gate at the output (**Figure 5**) for configuring output polarities as either active high or active low. The output polarity fuse is represented by a grounded XOR input. When the fuse is blown, that input is in a permanent high state, making the output an active high. An active low output is achieved by leaving the fuse intact.

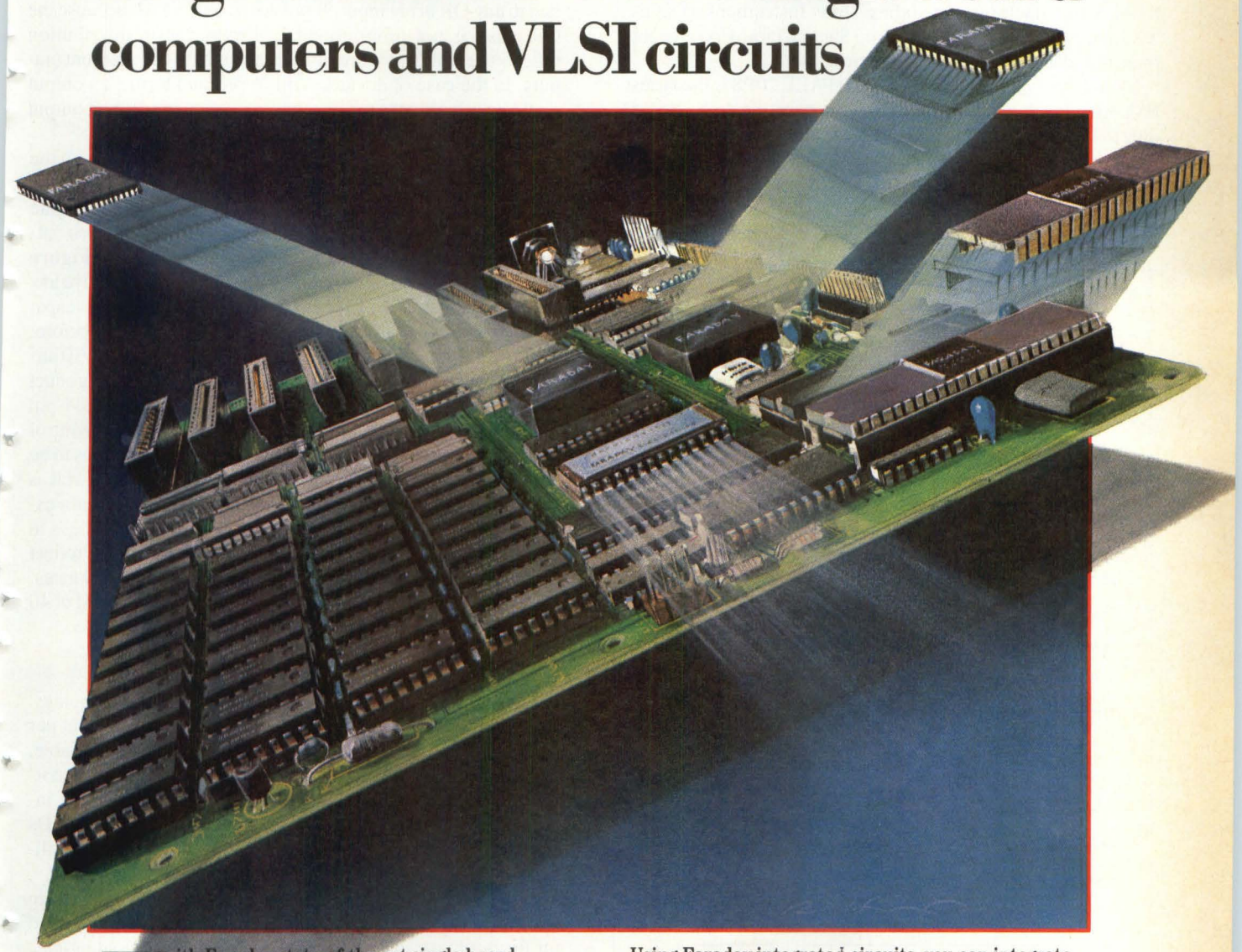
In the last few years, basic PLD architecture has remained unchanged; focus has shifted from functionality to speed. Propagation delay (Tpd) is the parameter most often cited when comparing PLD performance. In PLDs, this is the time it takes for a signal to propagate through both the AND plane and the OR plane. Tpd does not include the time consumed if the PLD has registered outputs. Set-up (Tsu) and clock-to-output (Tco) are frequently noted when determining sequential logic performance. In newer devices, Tsu and Tco times typically range from 10 nsec to 15 nsec.

Early devices had a Tpd of 50 nsec. The most common devices today, the A-Series, have propagation delays of 25 nsec.

# Anyone can be compatible.

# Only FARADAY

## gives you packaging flexibility with integrated IBM® PC BUS single board computers and VLSI circuits



With Faraday state-of-the-art single board computers and CMOS VLSI circuits, you can implement PC-DOS compatibility in various system configurations. At lower cost. And with a shorter time to market.

Faraday single board computers are available with various combinations of integrated disk, video display and CPU controller functions. These and other functions are also available on Faraday adapter cards.

The single board computers include the Faraday BIOS in EPROM and support Faraday PC-DOS (enhanced MS™-DOS). Faraday provides MS-DOS and GW™-BASIC under license from Microsoft.

Using Faraday integrated circuits, you can integrate disk, monochrome display and CPU controller functions. These devices replace more than 75 integrated circuits.

To take advantage of the powerful cost, packaging and time advantages you'll get with this and future levels of integration, simply contact Ron Mazza, Vice President Marketing, Faraday Electronics, 743 Pastoria Avenue, Sunnyvale, California 94086, (408) 749-1900, TLX 706738.

MS and GW are trademarks of Microsoft Corporation.
IBM is a registered trademark of International Business Machines.

FARADAY

**The OEM PC Compatible Company.**

Circle 28 on Reader Inquiry Card

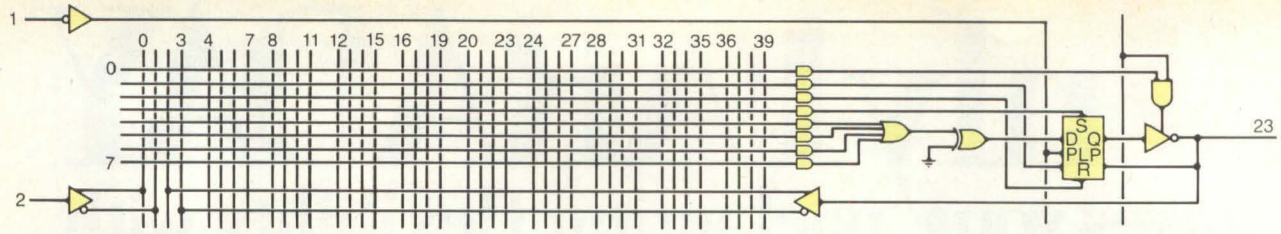



Figure 5: The fuse programmable XOR-gate shown feeding a D-type flip-flop is used to configure the PAL's outputs to be either active high or active low.

Several manufacturers, including Texas Instruments (Dallas, TX) and National Semiconductor (Santa Clara, CA), recently introduced a new 15 nsec B-Series.

Monolithic Memories Inc.'s (MMI) PALE 20P8 is the fastest PAL available, with a reported 6 nsec propagation delay. According to MMI (Santa Clara, CA), the new ECL part also includes programmable output polarity and product term sharing. However, product term distribution might be a better definition; true product term sharing, in which any AND array output can be tied to any OR array input, is not possible in a PAL because the OR array is not programmable. Product term distribution reflects the ability to share product terms between adjacent outputs. In the case of devices with 16 product terms, an output could have from zero to sixteen terms, with an adjacent output handling the balance of unused terms.

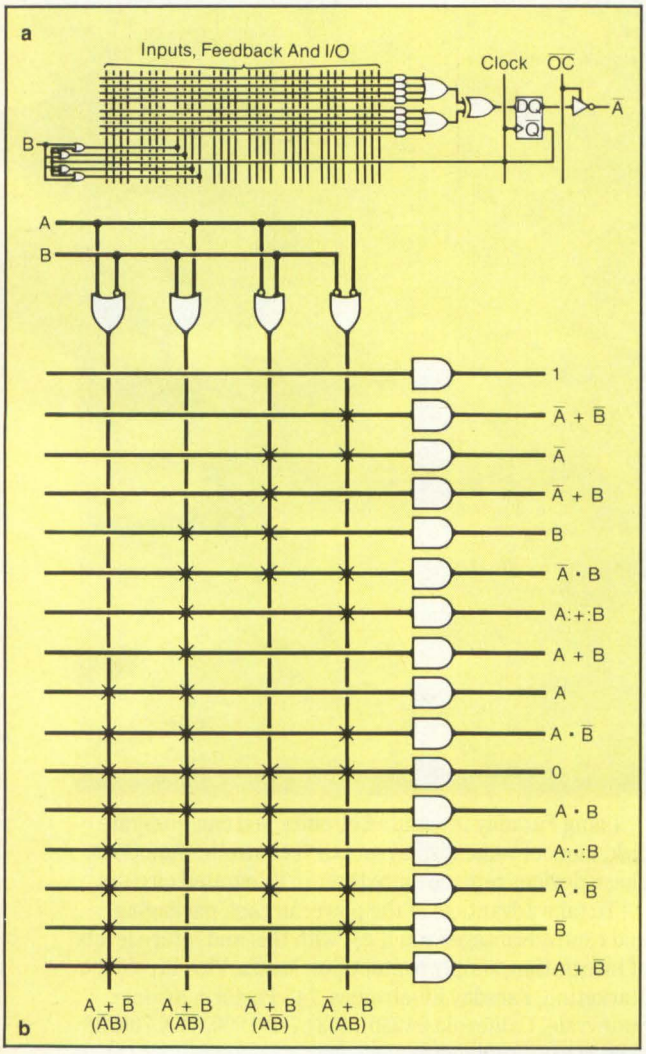



Figure 4: (a) By including an XOR gate at the input to the D-register, carries from previous operations can be XORed with two variable sums generated by the PAL array. This architecture allows the user to implement arithmetic operations. (b) When the PAL architecture of (a) is programmed as shown, the circuit provides the corresponding 16 Boolean combinations.

PAL technology took a major step forward in 1984 with the introduction of the 800-gate AmPAL22V10 from Advanced Micro Devices (Sunnyvale, CA) (**Figure 6**) and the 5000-gate MegaPAL from MMI. Both parts have macrocells at each output that can be individually defined and programmed (**Figure 7**). Every output can be programmed as active high or active low and for either registered or combinatorial operation. This capability provides designers with more flexibility than ever before.

From a functional standpoint, the AMD AmPAL 22V10 has up to 22 inputs (programmable I/O), 10 outputs and 132 product terms (AND gates), or 132 44-input AND gates. The 84-pin MMI PAL64R32 MegaPAL (**Figure 8**) has a preload control line on each output register. Preload allows the flip-flops to be put into a known state when the PLD is powered-up, as well as making the chip more testable. Product term distribution extends the flexibility of the 64R32 by permitting the devices's 16 product terms to be shared between a given output pair. Product terms are formed from the chip's sixteen 128-input AND gates. As far as speed is concerned, the MegaPAL offers a Tpd of 40 nsec, and the AmPAL22V10's Tpd is specified at 35 nsec.

## CMOS And EPROM PLDs

Until recently, PLDs were available only in bipolar technology. The common A-Series PALs consume 180 mA of current per device; half-power devices using only 90 mA are also available, but the Tpd rises to 35 nsec. If many of these chips are incorporated on a single board, power consumption can be intolerable. The solution, of course, is to use new CMOS PLDs that operate at lower temperatures and thus increase reliability and simplify packaging problems.

Erasable programmable logic represents a second twist in PLD technology. Simply stated, EPROM cells are substituted for fuses as a means to program the device. The floating-gate transistor traditionally found in EPROMs allows PLD customization via a nonvolatile charge transfer mechanism. EPROM cells are programmed by injecting charge on the floating gate, which permanently turns the transistor off.

Since 1978 when it became feasible to fabricate CMOS EPROMs, this technology has been viewed as the strongest contender to replace fusible links. EPROM cell programming elements yield good price per storage bit because of their relatively small size. A state-of-the-art fusible link consumes 513 square microns, while a state-of-the-art EPROM bit takes only 36 square microns. This difference will allow tremendous growth in PLD gate densities.

Some companies are also developing EEPROM PLDs which

# VICOM.

# The image processor for those who deserve to get more than they thought they paid for.


**Innovation has always been a VICOM hallmark.**
From its beginning, Vicom Systems has built its business by delivering systems that exceed the performance expectations of the most critical scientists and engineers. It is against this background of unequivocal performance that Vicom Systems builds your specific image processor.

**Configure the specific system you need.**
The VICOM image processor is highly modular. By selecting the right combination of circuits our team of specialists can quickly and cost-effectively create the task-oriented image processor you need.

**Long term relationships**
At Vicom Systems our objective is to build a working relationship. The initial sale is only the beginning. System upgrades, responsive service, training, special software routines, we have them in place ready to implement at your call.


**Vicom Systems, Inc. The image processing professionals.**
Our business strategy is simple. We build-in quality. More than you thought you paid for. We help you get your system running, faster. We respond positively when you need us. The results: Productivity, not promises. Performance with lasting reliability.

We're Vicom Systems. Call us at 408-946-5660 or 800-538-3905. Or write us at 2520 Junction Avenue, San Jose, CA 95134. Telex 171603 VICOM SYS.

VICOM SYSTEMS INC.

**For Immediate Interest, Circle 12**
**For Information Only, Circle 22**

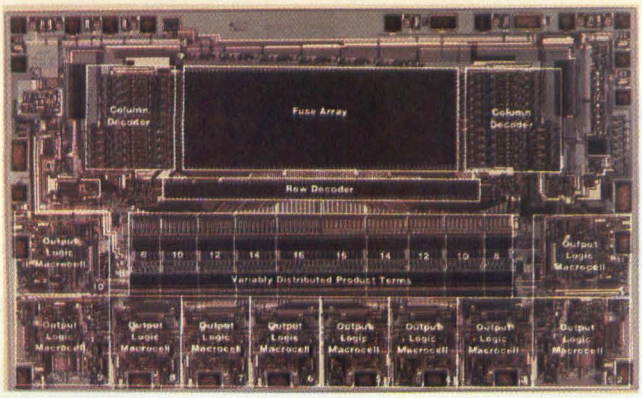



Figure 6: A die photograph of AMD's AmPAL22V10 illustrates the various sections of the device.

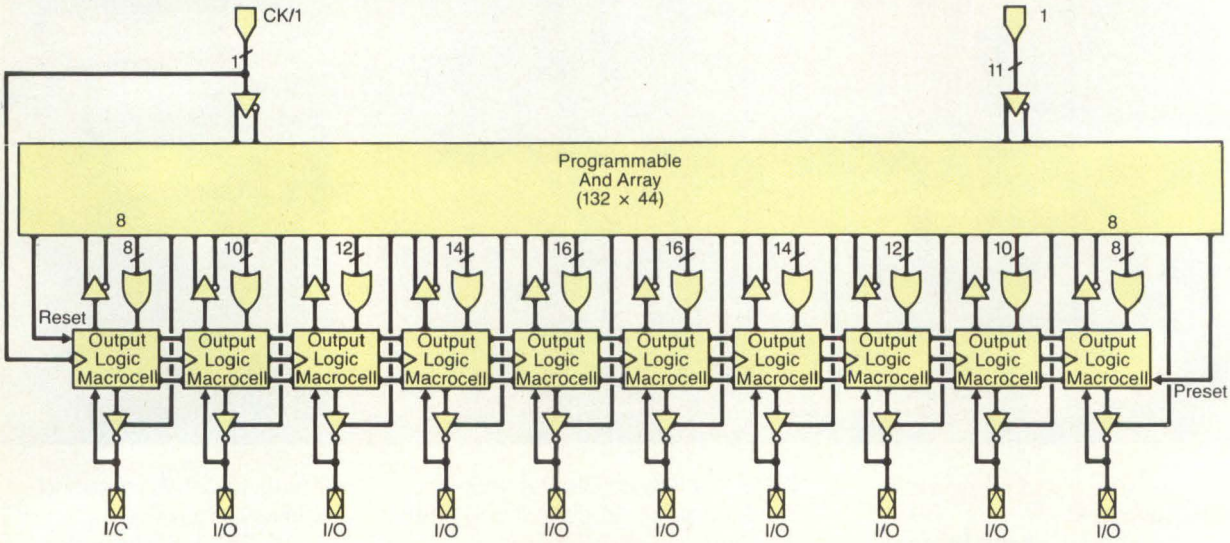
could be reconfigured without being removed from the socket. With this technology, a new era in system design is on the horizon: the dynamically reconfigurable ASIC. Lattice Semiconductor (Portland, OR), Exel Microelectronics (San Jose, CA) and Semi Processes (Santa Clara, CA) are expected to be among the first vendors to introduce this kind of PLD.

According to Lattice, their new PLD architecture allows one generic design to be configurable for virtually any 20-pin PAL architecture. The GAL-16V8 is a 20-pin device with 18 input/feedback paths and 8 output logic macrocells. With its unique architecture matrix, the chip can function identically as either a medium or a small PAL device. The GAL-16V8 is reportedly compatible with the following devices: 10L8, 10H8, 10P8, 12L6, 12H6, 12P6, 14L4, 14H4, 14P4, 16L2, 16H2, 16P2, 16L8, 16H8, 16P8, 16R4, 16R6, 16R8, 16RP8, 16RP6 and 16RP4.

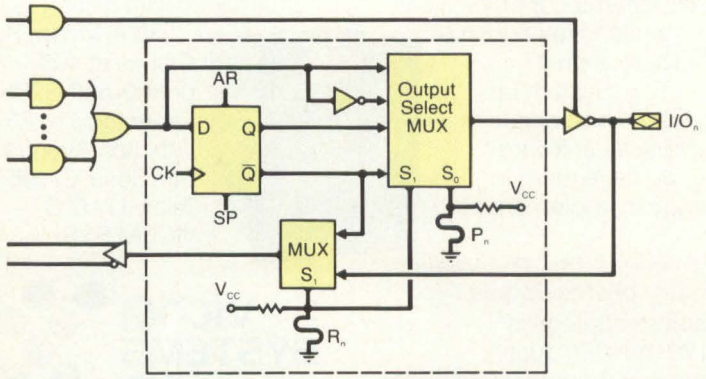
Improving CMOS technology has been continuously stalking the bipolar PLD. Thus far, manufacturers announcing CMOS EPROM PLDs include Altera Corp., VLSI (VTI) and Cypress Semiconductor, all based in San Jose, CA, and Panatech Semiconductor/Ricoh (Santa Clara, CA). Monolithic Memories and Harris Semiconductor (Melbourne, FL) introduced CMOS PLDs, but the parts use fuse-link technology. National Semiconductor and AMD are also poised to usher in CMOS PLDs.

In the past, the penalty incurred when using CMOS was low performance. Although this is true in some instances, many CMOS PLD vendors are claiming performance parity with their bipolar counterparts. Vendors such as National Semiconductor and MMI are also quick to point out that their devices will have negligible standby power – as low as 100 $\mu$A. According to National Semiconductor, their CMOS PLDs will have an operating range of 5-10 mA/MHz.

Cypress Semiconductor claims to have achieved 35 nsec propagation delays while holding current consumption to 90 mA using their 1.2 micron technology. One criticism of EPROM PLD technology is that signals incur longer propagation delays traveling through EPROM cells than through fuses. Cypress claims to have beaten the problem by using a two-transistor EPROM cell. One transistor is optimized for reliable




Output Logic Macrocell Diagram




| $S_1$ | $S_0$ | Output Configuration |
|---|---|---|
| 0 | 0 | Registered/Active Low |
| 0 | 1 | Registered/Active High |
| 1 | 0 | Combinatorial/Active Low |
| 1 | 1 | Combinatorial/Active High |

0 = Unblown Fuse
1 = Blown Fuse

Figure 7: AMD expanded the basic PAL architecture by including programmable macrocells on each output of the firm's 22V10. Also adding to the device's flexibility are the varying number of product terms found at the ten outputs.

# ONLY EIKONIX®

## DOES SO MUCH IN HIGH PERFORMANCE DIGITAL IMAGING CAMERAS.


EIKONIX® high-performance digital imaging cameras offer unique capabilities that clearly distinguish them from all others.

### CCD or Photodiode Technology

Only EIKONIX offers a choice of high-resolution cameras employing either linear CCD (charge-coupled device) or photodiode technology. In fact, EIKONIX offers the highest-resolution CCD camera available anywhere, with up to 20 million pixels per image (4096 x 5200). You can choose the economy and low-light capabilities of a CCD camera, or the greater dynamic range of a photodiode camera, *without sacrificing high resolution.*

### Color or Monochrome

Only EIKONIX has a family of high-resolution cameras available for either monochrome (256 gray-scale levels) or color (a palette of 16 million colors) applications.

### More User Control

Only EIKONIX cameras use a precision stepping-motor/lead-screw/ball-slide stage mechanism, which provides precise positioning of the array and eliminates one-dimensional smearing. In addition, this mechanism allows asynchronous operation, so the user can control both scan speed and data collection rate. This eliminates the need for a separate "frame grabber" or dedicated processor, and frees the host computer for multi-tasking.

### Buy Just What You Need

Only EIKONIX' broad product line lets OEMs and end users match needs precisely. Configurations range from bare-bones digital camera heads through complete image acquisition subsystems, including cameras, light sources, control electronics, imaging software, and interfaces for many widely used computers (including most DEC and Multibus-based systems).

### More Applications

Only EIKONIX offers the performance and flexibility to handle the broadest range of the most demanding applications, including mapping, engineering drawing digitizing, graphic arts, CAD/CAM input, office automation, X-ray storage and analysis, textile pattern design, geological imaging, communications, animation and microscopy.

### EIKONIX Know-How

Only EIKONIX digital imaging products are backed by our 17 years of experience in matching advanced electro-optical technology to a widening world of applications.

To find out what we can do to support your digital imaging applications, contact EIKONIX, 23 Crosby Drive, Bedford, MA 01730, (617) 275-5070.

EIKONIX®

**Circle 56 on Reader Inquiry Card**

programming, and the other is optimized for high speed. Cypress also introduced their A-Series which has a 25 nsec Tpd and consumes 155 mA of current.

VLSI Technology recently unveiled their PACC cells, which exhibit propagation delays of 55 nsec and consume 20 mA to 40 mA of current. The default state of the basic PACC cell (**Figure 9**) assumes that only the primary four-term product group is ORed; the combinatorial output with the active low state is also a default state. If more than four product terms are required, the secondary product term group can be selected. Between the two groups, eight product terms are available at the output. Like the AMD AmPAL22V10, VTI's PACCs permit users to program the output macrocells for either registered or combinatorial operation. One difference between the two is that the AMD chip has a wide variation in the number of product terms per output.

Altera's CMOS EPROM PLD products, the EP300, EP600, EP900, EP1200 and EP1800, range from 300 to 1800 gates. Like VTI and AMD devices, a programmable macrocell is the dominant factor behind Altera's arrays. The EP300 includes eight of the macrocells shown in **Figure 10a**. Connections are made by programming selected EPROM cells (**Figure 10b**). The internal structure of the architectural control shows that output and feedback selectors, programmable cells, provide 12 operating configurations for each sum term. The output selector permits programming the registered and combinatorial outputs to be either inverted or noninverted. And with the feedback selector, users have a choice of tapping signals from three distinct nodes.

Performance for the Altera line of PLDs ranges from 35 nsec Tpd in the EP300 and EP600 to 60 nsec in the EP1800. At the same time, active power consumption ranges from 125mW in the EP300 to 480 mW in the EP1800. Standby power for the EP300 is 125 mW, but this figure drops to 15mW for all other family members.

## EPROM And EEPROM: Advantages And Disadvantages

Programming a fusible link device is a destructive process.

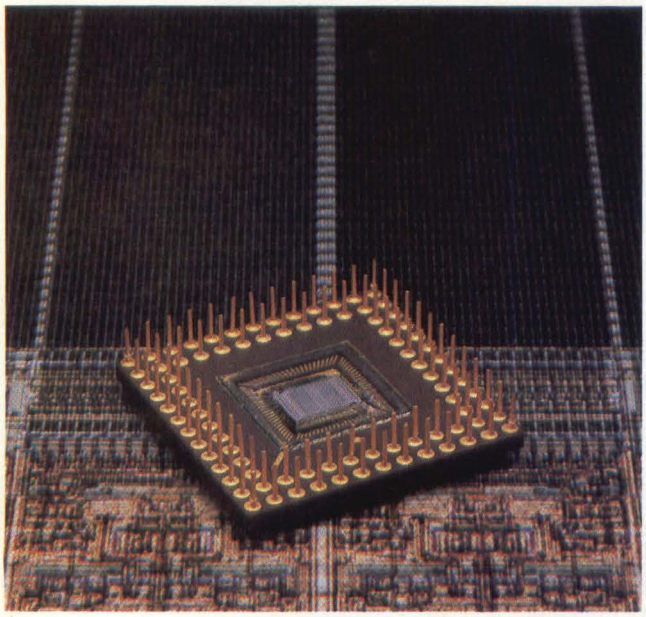


Figure 8: Monolithic Memories claims the 64R32 MegaPAL is equivalent to 5000 gates. The accuracy of this number has been the subject of recent debate among PLD competitors throughout the industry.

Consequently, PLDs have been virtually impossible to test before programming. In many cases, vendors incorporate redundant circuits to test the programming circuitry. Additional test circuitry is included to facilitate functional testing both before and after programming. Even with these schemes, however, many faulty devices are shipped to customers who must also perform functional testing on the PLD after programming.

In contrast, erasable and reprogrammable EPROM and EEPROM PLDs can be 100% tested before leaving the factory. The manufacturer will program devices the number of times necessary to assure every logic gate, each programmable link and all datapaths are operating correctly. In addition, manufacturers will be able to perform full AC parametric testing on the entire device.

Unlike most manufacturers, AMD claims their bipolar fuse-link devices are fully tested before leaving the factory. The firm guarantees that only 0.05% of all parts shipped to the customer will fail. According to AMD, additional test circuitry, test rows and test columns are added to each device. By putting Zener voltages on certain pins of the chip, the test circuitry is accessed during wafer sort and final testing, so each device is checked for stuck at 1 and stuck at 0 faults. Complete functional testing

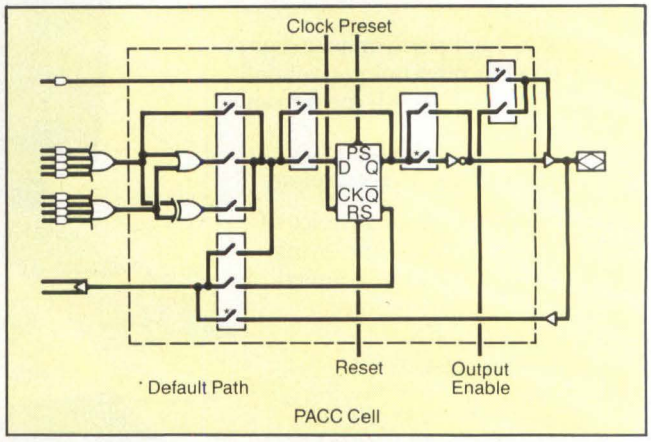



Figure 9: VLSI Technology, known best for their cell compilers, recently expanded their presence in the ASIC arena with the introduction of PACC cells. The new family of devices is based on CMOS tecnology and uses EPROM cells instead of fuses.

is done on the device's AND-OR array, registers, I/O buffers and feedback circuits. And finally, AMD maintains that the device undergoes full parametric testing.

Comparing EPROM PLDs to their EEPROM counterparts, each has advantages and disadvantages. For instance, EEPROM cells are about four times as large as their EPROM equivalents. EPROMs are also easier to fabricate. And perhaps even more significant, EPROM technology is more mature than EEPROM and has proven to be quite reliable.

EPROMs, on the other hand, may have to be packaged in plastic to be cost-competitive with other PLDs. Unless they have windows, they are no more testable than fused technology parts. Even with windows, they will be costly to test since it usually takes ten to fifteen minutes to erase a UV EPROM. In constrast, an EEPROM device is typically deprogrammed in 10 msec.

Whether a PLD is based on EPROM or EEPROM technology, the ability to erase and reprogram the device permits the designer to correct any mistakes or incorporate upgrades

# A clear difference in real-time Image Processing

Whether you need a turn-key system or a peripheral to connect to your computer, the **TRAPIX™ 5500** Image Processors have been carefully designed to meet your specific needs. They're compact and rugged enough to withstand most hostile environments, yet they carry a commercial price tag and are backed by a full year factory warranty — the best in the industry. They don't require special power or air conditioning and they use standard programming languages and operating systems — features designed to make them easy to own and use.

It's both flexible and expandable. Even the smallest **TRAPIX™ 5500** is a full-function, image processor that can grow to meet your future requirements. Its modular design and Q-bus/Unibus architecture let you develop cost-effective solutions for any image processing application. To tailor your own solution, simply select any subset of the following capabilities:

**Image Acquisition**
- Monochrome, binocular, color or multispectral input
- Camera, CCD, infrared or video tape
- Line scan or array to 2048 x 2048
- Analog or digital to 12.5 MHz
- 8-, 10- or 12-bit digitization

**Image Storage/Retrieval**
- Up to 16 mbytes of dual ported image memory
- From one to 32 bits per pixel
- Images to 4096 x 4096 pixels
- Real time disk storage up to 6800 images

**Image Processing/Analysis**
- Real-time logical, arithmetic processing
- Convolution, warping, and FFT
- Morphological, machine vision processing
- Continuous interpolated magnification/minification
- High-speed vector generation
- User-programmable 32-bit signal processor (TMS-320)
- Real-time histogram generator

**Computing/Networking**
- Standalone with internal LSI-11 or MicroVAX
- Bus-connected to any Q-Bus or Unibus computer
- Easily interfaced to non-DEC computers
- Ethernet, DECnet, IEEE 488

**Software**
- Proven library of ready-to-use image processing and analysis functions
- Turn-key and custom software availability
- Support for Fortran, C, Pascal and assembly language
- RT-11, TSX-Plus, RSX-11M, VAX/VMS, UNIX

As you can see, the **TRAPIX™ 5500** offers a clear solution to your image processing requirements. For more information or applications assistance, call or write RCI.



RCI RECOGNITION CONCEPTS, INC.
924 Incline Way, P. O. Box 8510, Incline Village, Nevada 89450 (702) 831-0473 Telex: 753168

INNOVATORS IN IMAGE PROCESSING©

Circle 2 on Reader Inquiry Card

**See us at NCGA booth #146**

without having to use a new part. This is a significant advantage over fuse programmable devices.

## Tools Tackling The Technology

Forget EPROM- and EEPROM-based CMOS PLDs. Without the sophisticated tools to program these ASICs, the chips are useless. Deficiencies in development software contribute heavily to designers' reluctance to use PLDs. However, recent introductions are changing the development software outlook.

PALASM set the standard for PLD development software in the late 1970s. The program was intended to provide designers with a tool to translate equations into PAL fuse plots. Simulation and fault grading were added, making PALASM a more sophisticated program. However, to keep pace with rapidly expanding PLD technologies and architectures, MMI is developing a second version of the program, PALASM2.

According to MMI, the new software is a language specification used for describing hardware design in terms of logic equations representing combinatorial and registered circuits, equations representing state machines, states, inputs and outputs. For simulations, PALASM2 allows the functional description of a design to be put in a high level syntax. The program is designed to reduce the size of the circuit specification without losing design clarity. Additional features such as indexed variables, equation compaction, product term compaction and string substitution are aimed at reducing the amount of time spent entering a design into the computer.

Several third party vendors are also capitalizing on PLD's recent growth. Assisted Technology (San Jose, CA), for example, offers CUPL, which supports PLDs from several different IC suppliers. The product accepts designs represented by Boolean equations. Logic expressions are then reduced by the software, which also establishes whether the target PLD can accommodate the design. CUPL includes CSIM, a simulator that permits design verification prior to programming. When the designer is satisfied with the circuit, CUPL generates a JEDEC format code for input to various PAL programmers. Presently, CUPL runs under both VMS and PC-DOS.

Representing a future trend in PLD programming, Data I/O (Redmond, WA) offers ABEL, which allows designers to specify a circuit via schematics, state diagrams, Boolean equations or truth tables. All of these programming techniques are supported on Futurenet's (Canoga Park, CA) DASH IBM PC-based workstation. ABEL 1.1 supports over 95 PLDs and runs under PC DOS, VMS and UNIX. Schematic capture, however, is only possible using Futurenet software. ABEL maximizes efficiency with an algorithm that reduces the number of product terms. In addition, an automatic De Morgan conversion algorithm permits the designer to specify any signal polarity. Design-debugging aids include a simulator with trace and breakpoints, diagnostic error messages and debugging list files. Thus, new logic configurations can be tested and debugged before programming the device.

Like Abel, Altera's A+PLUS allows the user to enter PLD designs via schematic capture, a netlist, Boolean equations or a state machine representation. The program runs on Personal CAD (Los Gatos, CA) IBM PC workstations. A unique facet of the system is Netmap, a schematic capture interface for netlist specified designs. Once the design is entered, mapping the equations onto Altera's EP family of EPLDs (erasable programmable logic devices) requires no designer interaction.

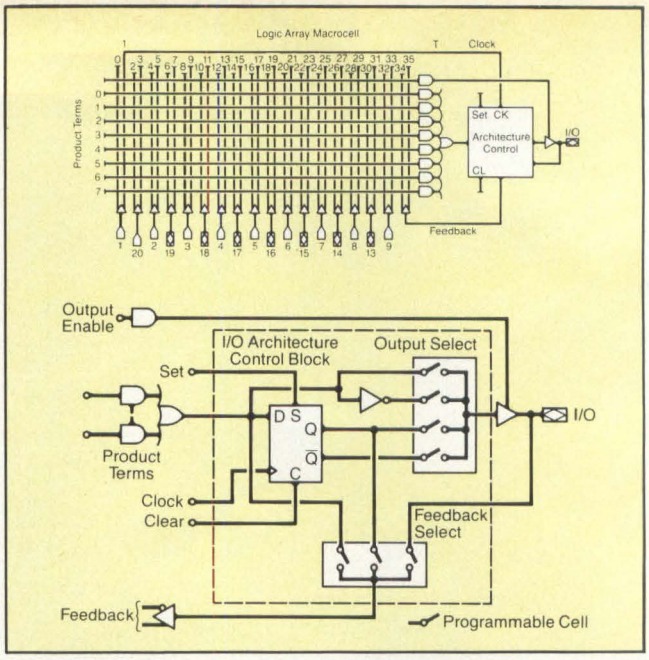



Figure 10: (a) Altera's EP300, which is based on CMOS technology and uses EPROM cells as opposed to fuses, incorporates eight of these macrocells in a single device. (b) The internal structure of Altera's architectural control section shows the output and feedback selectors that provide 12 operating configurations for each sum term. Both registered and asynchronous outputs can be configured to be inverted or noninverted by programming the output select multiplier.

## 1985: The Year Of The PLD?

1985 marks the year PLDs begin to rival gate arrays. Until now, PLDs possessed neither the speed nor functionality necessary for many designs. Moreover, new EPLDs are expected to be introduced by more than a dozen vendors by the end of the year. The deluge of newcomers offering these devices will surely result in price wars among vendors. This may curb fuse-link supporters' speculation that EPLDs will not be cost-competitive with bipolar devices.

Bipolar PLDs will not disappear, for new parts based on ECL technology are expected to offer propagation delays below 10 nsec. CMOS fabrication processes would have to be drastically upgraded to reach speeds even close to ECL performance. Like the CMOS gate array, however, CMOS PLDs are finding use in a wide range of compact systems demanding low power consumption.

Analogous to the CAD/CAE tools used for semicustom design, development tools hold the key to the PLD's growth. Software divorcing engineers from low level PLD design chores are on the way. Logic designers reluctant to transform schematics into Boolean expressions will appreciate new PLD schematic entry tools. And finally, by the close of 1985, several manufacturers including National Semiconductor and Assisted Technology are expected to introduce automatic test generation software for PLDs. DD

**How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.**

Very Useful . . . . . 613
Useful . . . . . 614
Somewhat Useful . . . . . 615


# "Our DT2750 graphics processing board puts on the whole show."

Here's a new breakthrough that'll be music to your ears.

Data Translation™ introduces the DT2750. It's intelligent graphics for your Q-Bus™ that bands together *everything* for your complete graphics processing needs.

It has dual memory capabilities, working in a shuttle mode, for continuous motion sequences and instant screen update.

There's an on-board processor that gives you both graphics and text.

It performs graphics in color, with as many as 8 colors from a palette of 512 available for display at any one time.

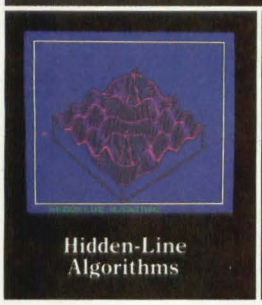
You can even generate a superimposed cursor to focus on various parts of the screen.

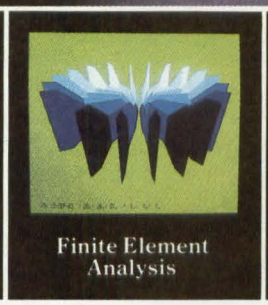
And there's lots of software included: a graphics subroutine package for DEC's RT-11™ and RSX-11M™, command utilities and diagnostics. There's also an optional high level CORE package for more advanced graphics capabilities.

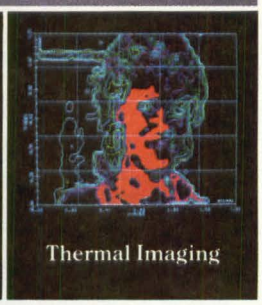
And the price? Unbeatable. You get all these features for less than $2,000.

Can you blame us for blowing our own horn?

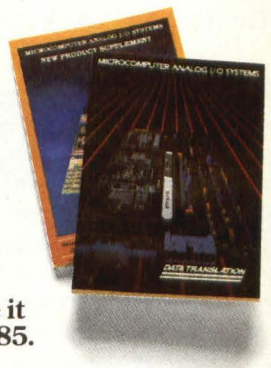
## Call (617) 481-3700


Hidden-Line Algorithms


Finite Element Analysis


Thermal Imaging

FIVE DAY 5 DELIVERY




**Call for our new 576 pg. catalog/ handbook or see it in Gold Book 1985.**

# DATA TRANSLATION

**World Headquarters:** Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.
**European Headquarters:** Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG112QZ, England Tlx: 851849862 (#D)
**International Sales Offices:** Australia (61) 663-5289; Belgium (32) 2-7352135; Canada (416) 625-1907; Chile (56) 2-253689; China (408) 727-8222; Denmark (45) 2451822; England 0734-793838; Finland 358-0-372-144; France (33) 6306839; Greece (30) 031-527039, (30) 01-3614-300; Hong Kong (852) 3-312607; India 231880; Israel (972) 3-324198; Italy (39) 2349751; Japan (81) 343-7571, (81) 348-8301, (81) 335-5111; Korea (82) 753-3101; Netherlands (31) 70996360; Norway (02) 567140; Portugal (351) 19545313; South Africa (27) 12118161782; Singapore (65) 2729412; Spain (34) 12502577; Sweden (46) 8289425; Switzerland (41) 17231410; Taiwan (86) 721-7864, (86) 531-2434; West Germany (49) 89806061.



**Circle 52 on Reader Inquiry Card**

# Solid Modeling

# A Maturing Technology

Solid Modeling does more than paint a pretty picture — It is an essential component to present CAD systems.

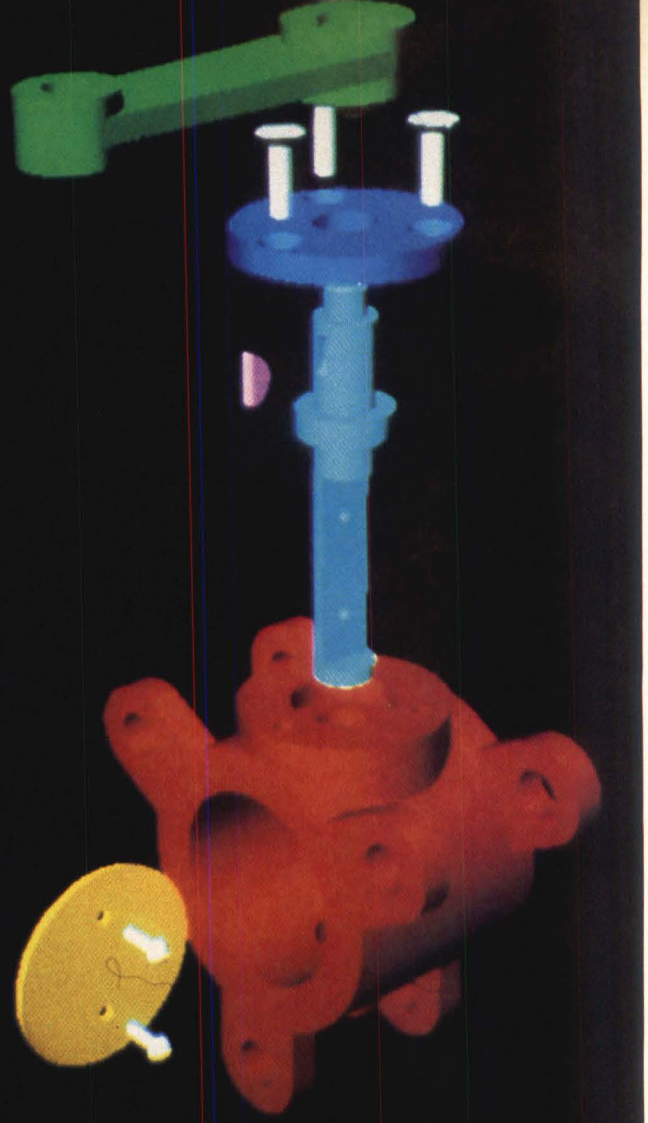


PHOTO COURTESY MCDONNELL DOUGLAS

**by Gregory MacNicol, West Coast Technical Editor**

In the early '60s when solid modeling was just beginning, only lines and arcs were available to create two-dimensional drawings to be used for drafting. Now, advanced solid modeling systems can depict objects never before seen in 3D, using multiple light sources with photograph-like detail. The object may be rotated, moved, exploded, seen with a wide angle view, and most importantly, changed. Relying on an object's database, the object may be modified to meet exact specifications and displayed again.

Solid modeling uses a mathematical description of an object to generate a visual image that is mathematically correct. Non-solid modeling systems can also describe and render an object but lack the mathematical accuracy needed for engineering purposes. In addition, these systems based on wire frame models create ambiguous representations. Wire frame models lack the ability to remove hidden lines, offer interference and clearance information and provide mass property calculations. A complete solid modeling system is well integrated into a CAD/CAM system for the creation of layouts, multiaxis numerical control instructions and finished rendering. The system must be mathematically complete, geometrically accurate, highly interactive and versatile. For engineering purposes, the real utility of solid modeling is much more important than a final result that is a visually pleasing rendering of an object.

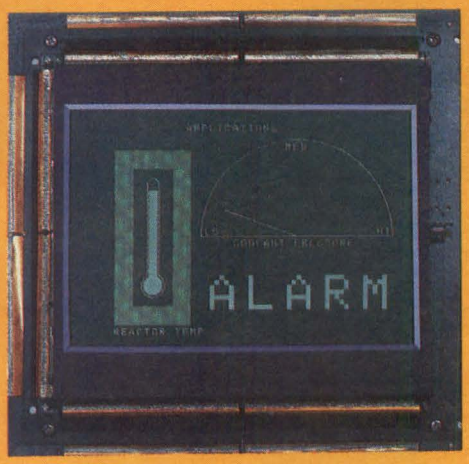
The results of a comprehensive solid modeling system allow users to create, store and manipulate complete and unambiguous models of solid objects. A requirement for the object is that it must be finite, homogenously three dimensional and not questionable, such as an object that has an internal void or a non-manifold edge. The result of having an object's complete description is improved automation, integration for use with other models, use in multiple applications and the ability to upgrade a system with future applications.

A complete modeling system should provide several useful functions for an engineer, such as tolerance analysis, sectioning, stacking, automatic mass property calculations and Boolean operations. Sectioning allows an engineer to view the interior of an object. The program must be able to calculate the various properties — area, perimeter, center of gravity and moment of inertia — as each part of an object is sliced away. Stacking uses several parts within one complete object; it must incorporate the variations from temperature and machining. Automatic

# NEW EL and VF DISPLAY MODULES

## GRAPHICS MODULES


Electroluminescent Graphics Module with powerful drawing processor using GCI (VDI) industry standard syntax. 512 x 256 pixels.

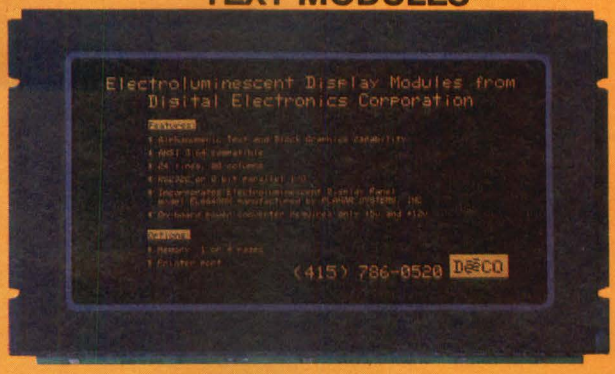



Vacuum Fluorescent Graphics Module. Controller has dual processor pipelined architecture for fast speed. 320 x 240 pixels.

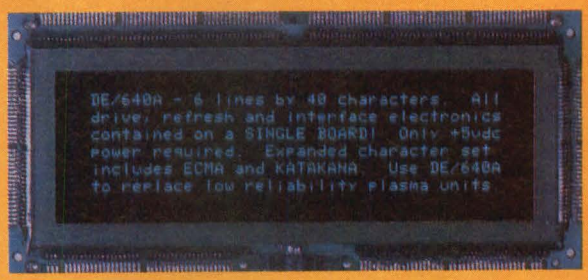
Vacuum Fluorescent Video Module accepts NTSC standard RS170 signals, has 16 gray levels, 3.75" x 5.00" screen size.


Vacuum Fluorescent Module, super fast bit mapped display. 256 x 64 pixels.

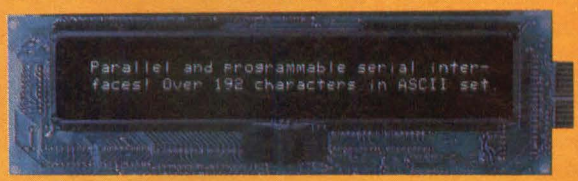
## TEXT MODULES




Electroluminescent Text Module allows 24 lines by 80 characters, double wide, double high characters, many other features.




Vacuum Fluorescent Text Module allows up to 240 ASCII, ECMA and KATAKANA characters, parallel or serial input.




Vacuum Fluorescent Text Module allows 2 lines by 40 characters, same features as above. Only +5 vdc power needed.


Vacuum Fluorescent Text Module, 40 characters. Above three modules available in high brightness and extended temperature range versions also.

Vacuum Fluorescent Text Module, 2 lines by 20 characters, loaded with features!

**+ MANY MORE! Over 25 standard models available!**

WORLDWIDE DISTRIBUTION

*THE DISPLAY INNOVATORS*

DeeCO T.M.

**DIGITAL ELECTRONICS CORPORATION**

26142 Eden Landing Road • Hayward, CA 94545 • (415) 786-0520

Telex: 172073 DIGELEC HYWD • Facsimile: (415) 786-1040

**Circle 62 on Reader Inquiry Card**

mass property calculations enable an engineer to gain such useful information as surface area, mass center of gravity and volume. Boolean operations, including intersection and difference, allow an engineer to experiment interactively with a model, testing for the best solution.

The documentation process is automatic in solid modeling systems. In the past, designers had to draw various orthographic views of an object and had no time for additional views which allow better and more immediate interpretation.

## Solid Elements

With all the interest and activity in solid modeling, there is the misconception that there are now simple definitions and concepts which can be used today. However, not only do applications dictate the best software route to use, but basic methods and concepts are still in debate. As new methods are introduced, some basic agreements and similarities in methodology remain.

There are several schemes for representing solid models, each very different from the others. Two of these schemes dominate: the constructive solid geometry (CSG) and the Boundary representation (B-reps) modelers. The CSG relies on graphic primitives such as blocks, cones, spheres and cylinders as the primary means of model definition. These basic elements are used to build a model and allow the creation of superprimitives such as linearly swept solids (slabs) or rotationally swept solids. The primitives are built with binary trees of Boolean operations such as union, interaction and subtraction.

Boundary representation modelers, in contrast, define solids by faces, edges and vertices. Faceted boundary representation approximates surfaces by planar facets or tiles, with curves which are actually strings of line segments. The advantages of faceted representation is the ease of adding new surface types, ease of hidden-line execution and the small amount of geometric code. The disadvantages are implicit; because there are no circular arcs, it is difficult for drafting and the creation of numerical control instructions. Additionally, there are very large quantities of data. Each solid modeling scheme requires a different

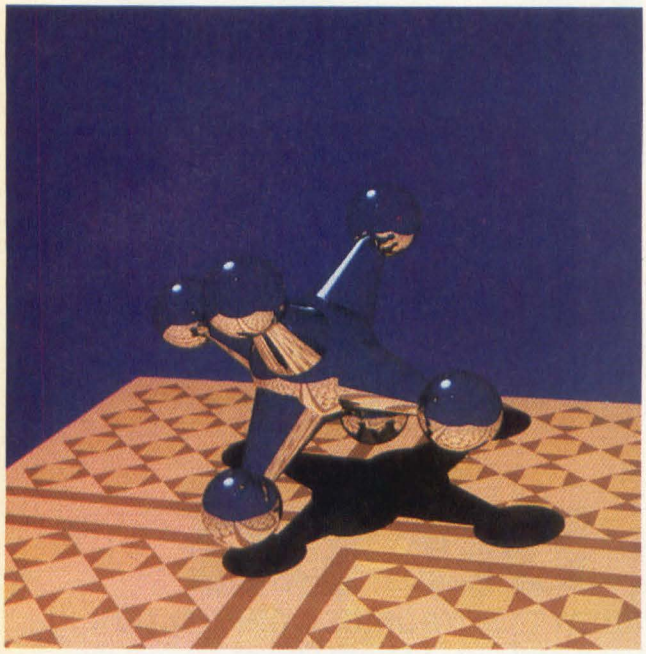


Figure 1: Rendering in solid modeling includes accurate shading of the model. (Photo courtesy Gray Lorig and RPI)

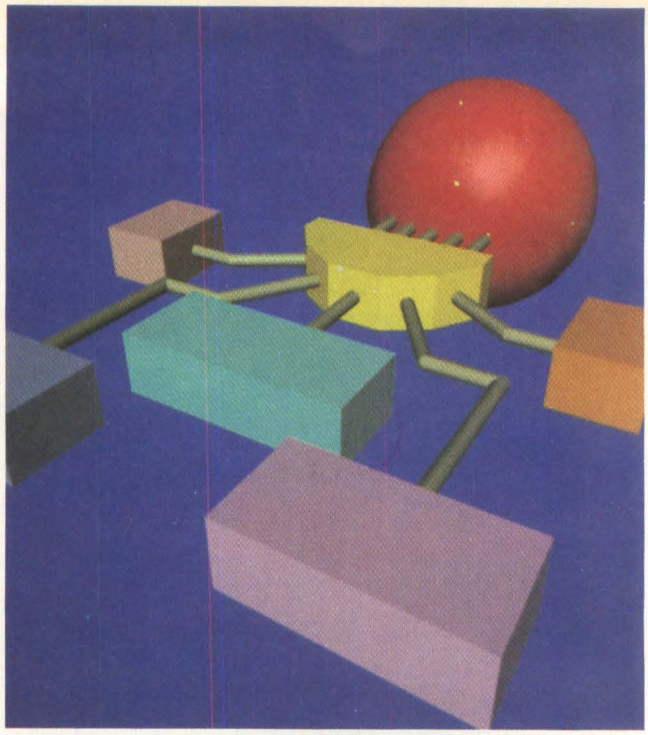


Figure 2: Modern day solid modeling systems use a combination of B-rep and CSG for describing objects to be displayed. (Photo courtesy Olin Lathrop and Raster Technologies)

form of database and allows for different methods of clipping, hidden object elimination, prespective control and special effects such as translucency.

There are newer choices for solid modeling to overcome the limitations of the basic methods. One method, spatial enumeration, takes a description of an object and breaks it down into quadtree data structures. The resultant algorithm looks like a tree depending on whether the node is partially filled, empty, or filled. A uniform grid could describe the object but would suffer from redundant and unused data.

A hybrid approach combines the best features of CSG and B-rep. Thus, Boolean operations may break down into primitives that are boundary represented. Hybrids include such leading turnkey modeling packages as Unisolids from McAuto (St. Louis, MO), Euclid from Matra Datavision (Burlington, MA), Solids Modeling II from Applicon (Burlington, MA) and ICM GMS from Auto-Trol (Denver, CO). Several other unbundled packages are offered by Cadam (Burbank, CA), Hewlett-Packard (Santa Clara, CA), Data General (Westboro, MA), Perkin-Elmer (Oceanport, NJ), and Digital Equipment Corp. (Marlboro, MA).

A major function of model creation is the editing process. Some editing functions in advanced solid modeling packages include Boolean operations, primitive instancing, sweeping and lofting, tweaking and automated filleting and chamfering. The origins of the terminology are from a mixture of graphics, drafting, and machining. Translational sweeping of a planar surface, for example, is the process of taking a two-dimensional surface description and adding thickness to it. A string of curves can also be swept rotationally; this is similar to taking half an outline of a screw and rotating it 360°. Lofting or skinning is the process of defining a curved outline so that the computer can calculate a finished and smooth object. Boolean operations also

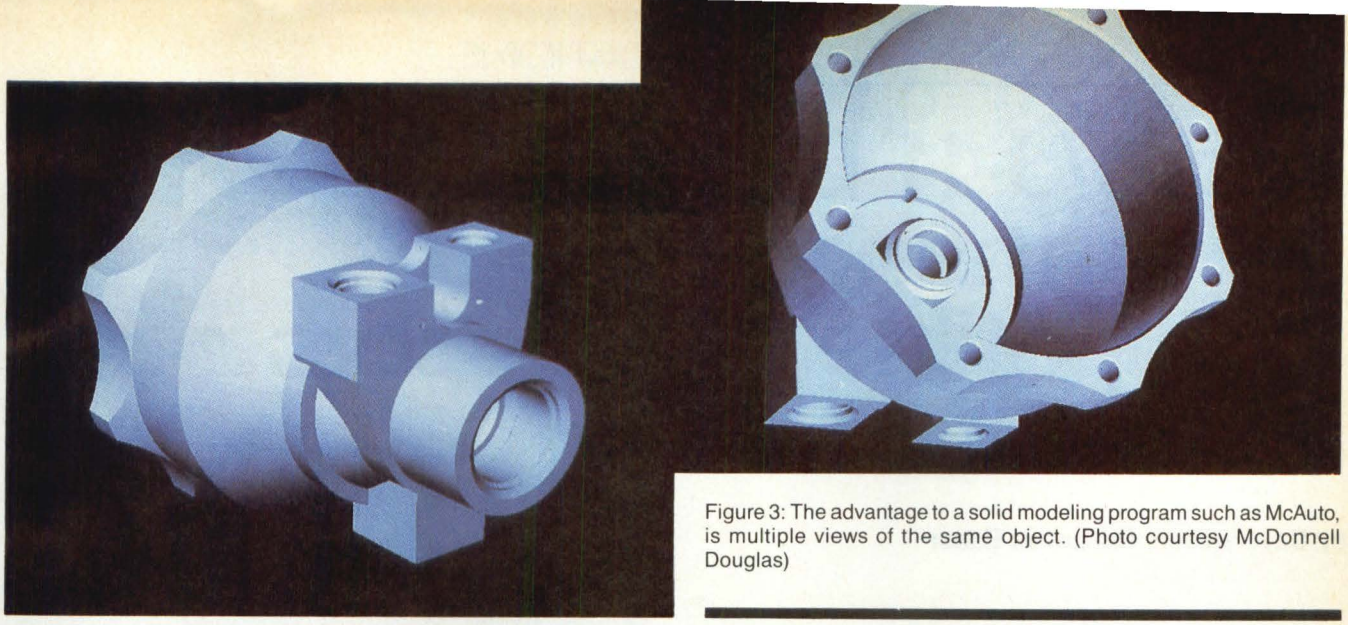


Figure 3: The advantage to a solid modeling program such as McAuto, is multiple views of the same object. (Photo courtesy McDonnell Douglas)

have simple analogies. Union operations are similar to gluing or welding, and the difference operation is similar to milling or drilling. Tweaking is the process of adding or subtracting a particular segment. A good editor should do tweaking interactively so the operator can see the process as it is occurring.

Problems, ambiguity and complex issues often arise during the editing process. One problem with editors that occur is limitations that are difficult to resolve. Sometimes the limitations are very basic, similar to the restrictions of Boolean operations. Because Boolean operations can play two different roles, storing and editing the geometry, there can be ambiguity in the desired operation. Other limitations may relate to subjects that do not overlap, have coincident or tangent surfaces or must be made in a particular order. There will always be limitations to a solid modeling program, such as filleting multiple unions, so it is important to evaluate what is necessary and what is extra.

## Support From Hardware

Although the focus on the creation of a solid model is on software, major advances in hardware are responsible for the high activity now in solid modeling. The Raster Technologies' (North Billerica, MA) Model One series is an example of graphics display processors aimed at the functions the host is responsible for: acquisition and control of an object's database into a display list of graphics instructions. Because a major bottleneck in the solid modeling process is graphics display, the graphics display processor's responsibility is to rapidly execute graphics functions. All shading, hidden object calculations, perspective and graphics display functions are executed on the graphics processor. Several other vendors make high performance display processors for solid modeling purposes such as Lexidata (Billerica, MA), Metheus (Hillsboro, OR) and IGC (Hauppauge, NY).

Support for solid modeling on the chip level is becoming commonplace. Three companies have focused on specific aspects of display problems and offer distinct solutions. Xtar (Elk Grove, IL) makes a graphics chip set for rapid display. The Graphics Microprocessor (GMP), with the Video Shift Register set, can display 160 million pixels per second; the host is required to calculate shading and hidden objects. Silicon Graphics (Mountain View, CA) manufactures a complete graphics workstation based around several "geometry engines." IRIS, a UNIX-based workstation, can transform, clip, and scale 65,000 coordinates per second. Weitek (Sunnyvale, CA) has chosen to focus on specific aspects of graphics display. The Solid Modeling Engine is designed similar to a set of chips that is also available on a Multibus-based three-board set. After the host has transformed the database into a display list, the resultant bicubic patches are sent to the Solid Modeling Engine where they are transformed, clipped, rendered and shaded. This process can take a polygon model and display it in seconds. Despite the board's high price, several CAD manufacturers use the set in their systems because of its speed and power.

## The Future

Solid Modeling has come a long way. But due to a more sophisticated user base that is goal oriented, many changes are in order. The most obvious is the total integration in a CAD system where many functions can take advantage of the model. Numerical control is a problem. Given a model's data, will the tool's motions correctly produce the desired part. Another problem is the generation of robotic simulation and the simulation of tool cutting motion. Integration towards finite element analysis is an additional CAD utility that is gaining importance in integration.

A major issue common in the computer industry is the user interface. Presently the user interface for solid modeling systems is poor. An informal inquiry of *Digital Design* indicated that the learning curve for 2D systems was a minimum of six weeks, 3D was three to four months and solid modeling took over six months for full proficiency. For technology developing as rapidly as graphics, electronics and solid modeling, this is too long.

Without any doubt, solid modeling systems are changing the way objects are being engineered. Turn-around time is lessening, while user involvement and productivity is increasing. The picture-perfect images created from solid modeling systems are doing more than painting a pretty picture. DD

**How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.**

| | |
|---|---|
| Very Useful | 607 |
| Useful | 608 |
| Somewhat Useful | 609 |

# Micro/J-11 Boosts Performance Of DEC-Compatible Processors

by Dave Wilson, Executive Editor

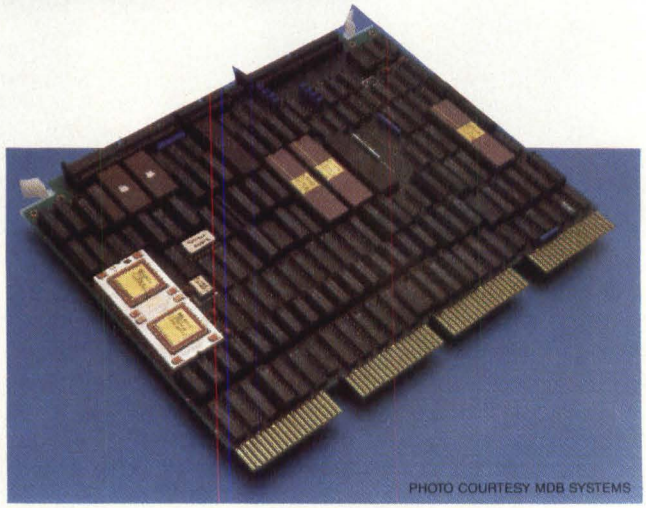


PHOTO COURTESY MDB SYSTEMS

Since its introduction, the Micro/J-11 microprocessor has offered the design engineer the potential for designing a wide variety of DEC-compatible equipment. Outside DEC, however, the processor has seen few designs when compared to other offerings such as the 68000 or iAPX families. There are a number of reasons why this is so. First, DEC does not consider itself primarily a components vendor, preferring to emphasize the systems side of the business. Second, design engineers using the device may design products which compete directly with products from DEC, obviously an undesired situation. Since DEC is the only vendor of the processor, they can either ration or simply cut off the number of devices to the OEM depending on whether they see the end product competing with their own.

Clearly, the lack of second sourcing has made many vendors wary of using the device at all; a fact verified by the number of J-11-based products in the marketplace. Those vendors that do offer J-11-based products have sought market niches that DEC has not entered. Usually working in conjunction with DEC, their product lines augment rather than compete directly with the DEC line.

In the OEM board business, DEC's Q-Bus has lost substantial marketshare to the Multibus, and this trend is likely to continue. Recent activity surrounding the Multibus shows an even greater push to maximize the functionality of a given board. Some vendors have even gone so far as to incorporate surface mount and SIP devices. This work is clearly lacking in the DEC-compatible marketplace. Furthermore, those vendors of more specialized products, such as disk and tape controllers, may have to conform to a given set of DEC protocols and diagnostic software; Multibus vendors do not have these constraints, leaving room for more innovative design on the boards. Of course, the long-awaited VBI bus with its Eurocard format may alleviate DEC's problem of marketing what is now perceived to be an older bus structure. Unfortunately, neither the specification nor any products on the new bus were available when *Digital Design* went to press. Clearly, DEC has lost some ground here too, considering that VME products and Multibus II products are available today.

Vendors of products on these bus structures tout the availability of silicon to support their products. Motorola, Mostek and Signetics, for example, have a great number of VLSI devices to support their VME bus (*Digital Design*, December 1984, pg. 44). For their part, Intel has signed an agreement with Toshiba to manufacture two Multibus II chips—the Bus Arbiter/Controller and the Message Interrupt Controller. Microbar (Sunnyvale, CA) has already announced they will manufacture a 68020-based Multibus II board. When DEC does announce their new bus structure, they should foresee that this sort of support is key to convincing the marketplace of the viability of their product.

Even without a new DEC bus structure, some smaller vendors have chosen to port DEC's J-11 microprocessor to existing high performance bus structures, such as the Multibus II and the VME bus. Over the past two years, the VME bus and associated products have provided a low cost alternative to DEC's PDP-11 machine family. However, the problem with using the VME versus the DEC product is mainly one of software—the user may have several man-years of investment in the DEC product but neither the time nor the money to port it to a 68000-based machine.

To enable a smoother transition from DEC to VME, one manufacturer, Logical Design Group (Raleigh, NC), has designed a VME board based on the J-11 microprocessor (**Figure 1**). The four serial input/output devices offered are DEC DL compatible so that standard software routines can run on them. A multiple function I/O device, the Zilog 8536 CIO, provides sixteen parallel I/O lines, four multimode handshake lines and three general-purpose counter/timers. The parallel I/O lines are capable of bit programmable input or output and can be used to interface with remote parallel devices, such as printers or controllers via the P2 connector.

Due to the design of the J-11 chip, the potential for data misalignment exists in applications where the board is used in a multiprocessor system with a MC68000. The 68000 on EVEN byte transfers exchanges data on the upper (DO8 through D15) data lines of the VME bus, whereas the J-11, on EVEN byte transfers, exchanges data on the lower (D0 through D7) data lines. Similarly, the 68000 on ODD byte transfers exchanges data on the lower VME bus data lines, whereas the J-11 on ODD byte transfers exchanges data on the upper VME bus data lines.

# Microbar. Your future system is our current project.

At Microbar, we're working today on the Multibus™ single-board computer (SBC) you'll need tomorrow. We specialize in developing SBCs that put OEMs and system integrators in front of the competitive pack—in technology, in time-to-market, and in cost. Doing that means maintaining a clear focus on the future and anticipating your needs—maybe even before you do.

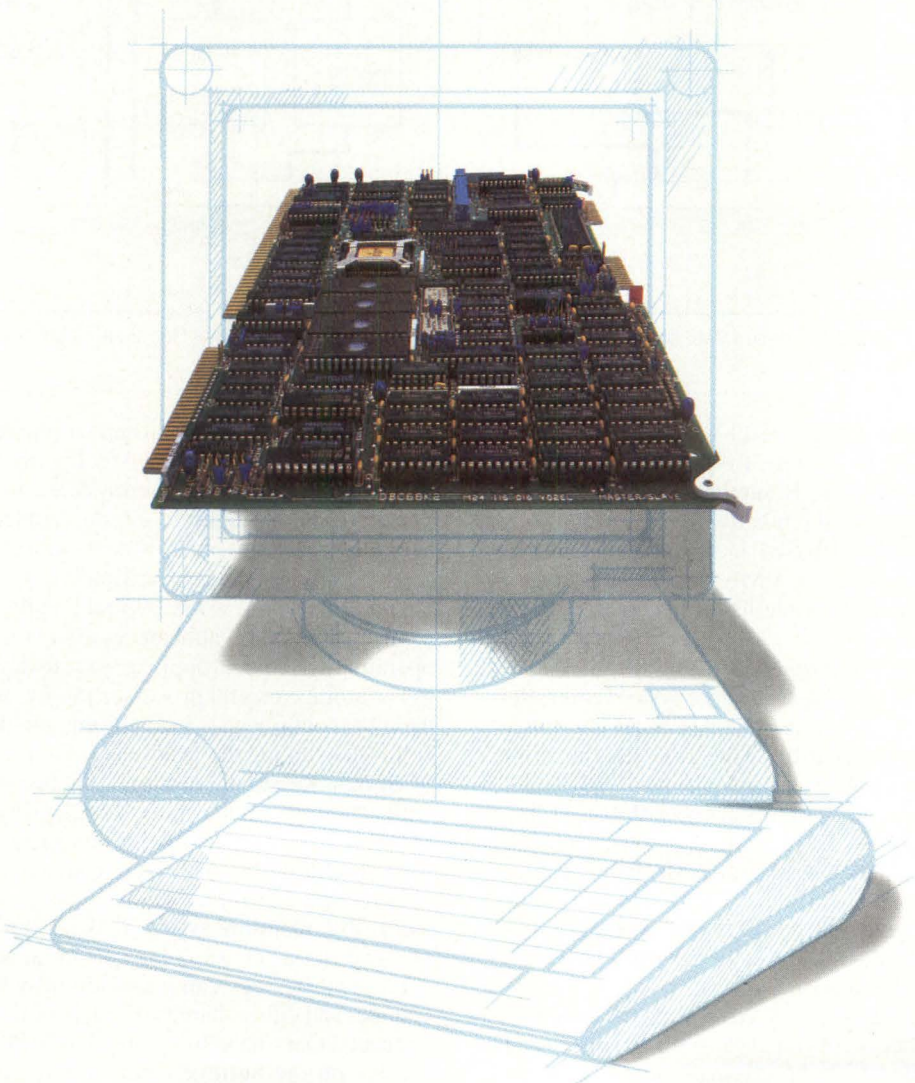
Keeping you ahead means we've got to stay flexible. We refuse to lock in to particular CPUs and technologies. Because we're independent, we continuously—and objectively—evaluate the newest microprocessors, busses and operating systems. So you can count on getting the best fully-integrated SBC solution for your application. And on getting it early enough to make that critical difference.

Today, we're exacting maximum performance from the leading 16- and 32-bit microprocessors implemented with the industry-standard Multibus. We do it by applying systems engineering concepts to board-level design. And through special architectures leading to speed and efficiency far beyond typical Multibus capabilities.

One thing we don't—and won't—do is compete with *you*. Our business is high-performance CPU boards, not systems. So our resources are 100% committed to developing and producing SBCs that make *your* systems successful, that give you a real edge in the market.

Microbar. We're working on your next system—today.

**MICROBAR SYSTEMS, INC.**
*785 Lucerne Drive, Sunnyvale, CA 94086*



**Circle 24 on Reader Inquiry Card**

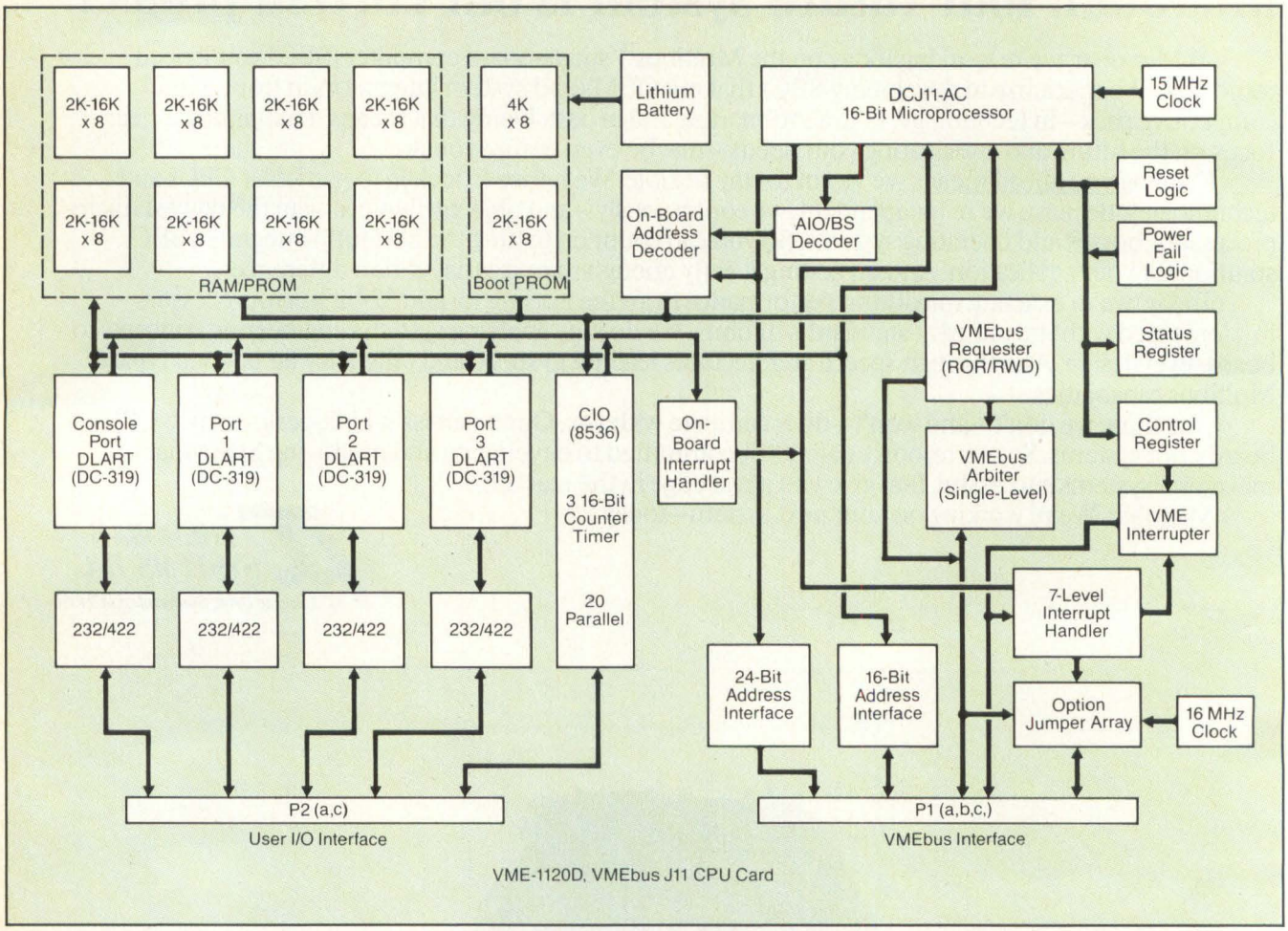



Figure 1: Logical Design Group's J-11-based VME board incorporates a full VME Bus Data Transfer Bus Requester, VME Arbiter and a seven-level interrupt handler.

As shown in **Figure 1**, a single-level VME bus arbiter has been implemented to handle requests from the J-11 SBC or any other master on the VME bus. If another card supplies this function, as is often the case, the function may be disabled by jumpering. The design of the J-11 SBC incorporates a full VME bus Data Transfer Bus Requester, VME Arbiter, a seven level interrupt handler, a selectable single-level Interrupt Requester and a set of utility signals.

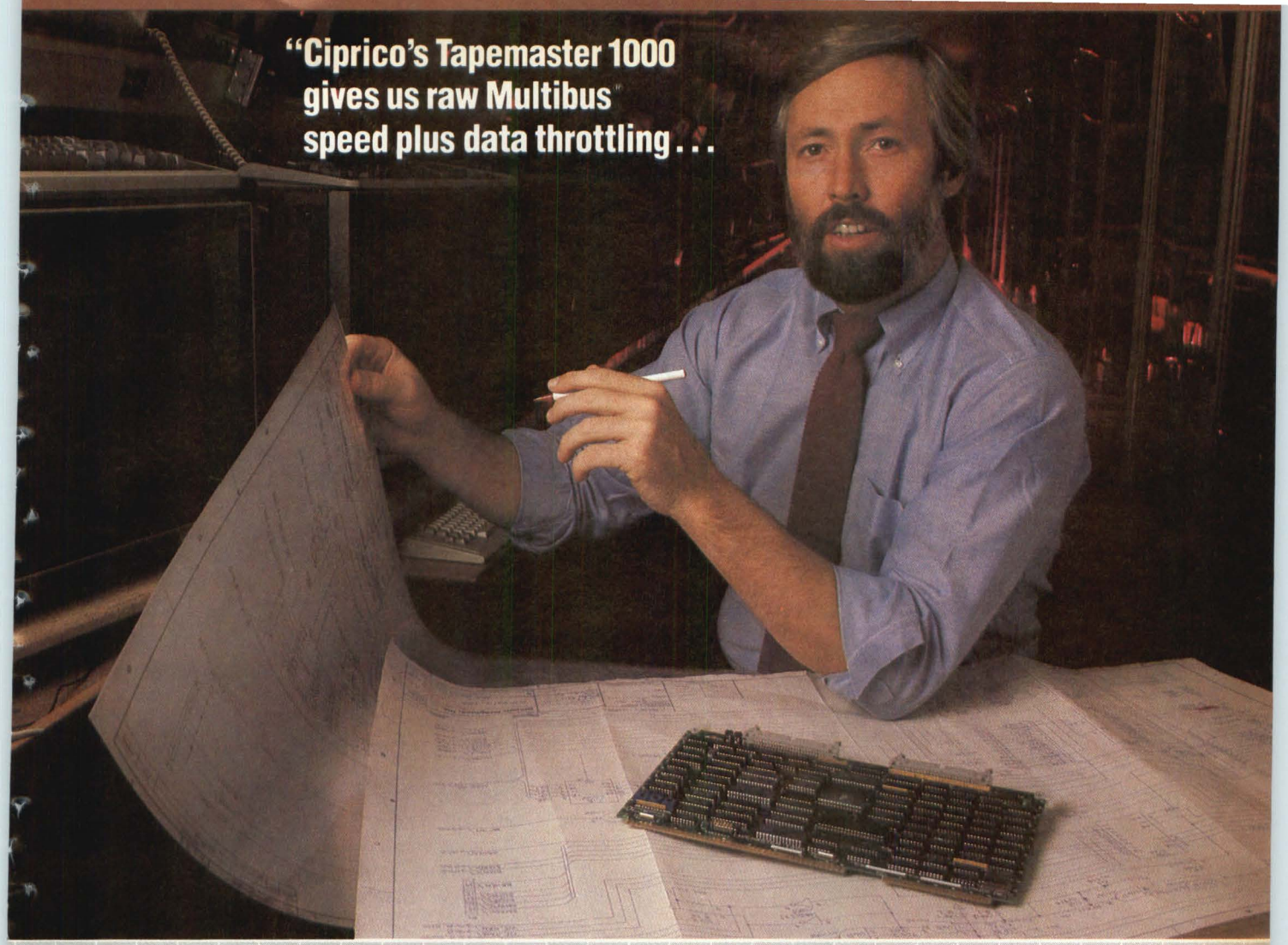
Two features have been incorporated to allow the SBC to be used in systems that do not have a separate system controller module. The first is a 16 MHz free-running crystal-controlled clock which may be jumpered to drive the SYSCLK line of the VME bus. The second feature is the VME bus SYSRESET signal line which may be driven from the on-board RESET line.

An array of eight 28-pin sockets can accept a variety of byte-wide memory devices, including static RAMs, EPROMs and EEPROMs. The entire on-board memory is local to the J-11 processor and is not accessible from the VME bus. A pair of 24-pin sockets, each configured for a 2K × 8 EPROM, enables the installation of a bootstrap loader.

The Multibus II from Intel is the VME bus' closest contender in the 32-bit marketplace. Intel's recent announcement of products for the bus included a 286-based single-board computer, several cache-based memory boards, a central service module and software support (*Digital Design*, February 1985, p. 24). But even before Intel's formal announcement of products for the Multibus II, one company, Argonne Systems (Santa Clara, CA), built a Multibus II-based system around the J-11 chip set. The design allows multiple, closely coupled central processors to run their own operating system within the same enclosure. A set of I/O controllers on the Multibus II services multiple central processors and creates a "virtual" PDP-11 hardware environment, enabling the central processors to run unmodified PDP-11 operating system and application software.

The storage central processor (SCP), an example of one of these I/O controllers, is an intelligent, multiported disk and tape controller linking the Multibus II Parallel System Bus to the SCSI bus. Key to the design of the board is its emulation of Digital Storage Architecture's MSCP protocol that uses logical requests for disk accesses. This is quite a task and has proven to be a big hurdle for many DEC-compatible companies to overcome (*Digital Design*, October 1984, p. 67). Under this protocol, the operating system disk server need not know the physical characteristics of the device attached to the system.

Physical devices can be subdivided into various logical volumes and either shared among several central processors or dedicated to a single processor. The MSCP disk class server, located on the Storage Control Processor, communicates logically with the host server running out of the central processor's memory.




Chase Bailey Design Engineer, Silicon Graphics, Inc., Mountain View, Calif.

. . . to maximize bus efficiency in our engineering workstations".

Silicon Graphics designs engineering workstations with high level graphics capabilities. Controller boards that Chase Bailey designs into his systems must pass rigid performance criteria, Ciprico's® Tapemaster® 1000 Multibus ½-inch tape drive controller included.

Bailey wanted to maximize bus efficiency, thereby increasing system response time. Two design criteria would accomplish this—high transfer speed and data throttling. The Tapemaster 1000 offered bus transfer rates up to 4 Mbytes/second. The tape drive transfer capability up to 1.5 Mbytes/second insures that the board works with the newer, faster GCR drives. Onboard data throttling provides precise control over data traffic and is programmable by either byte count or time in microseconds.

Tapemaster 1000 offers system designers like Chase Bailey total flexibility plus a host of support features.

Ciprico written, fully documented and supported software drivers are compatible with most major operating systems including UNIX® 4.2, UNIX Systems III & V, and RMX-86.® Tapemaster 1000 can be counted on to get your total system up and running from the moment it is plugged in.

Extensive diagnostic support is offered, from an onboard self-check at power up to a separate diagnostic board for customers' incoming inspection.

Systems designers who choose Ciprico, know they are getting the support of a dedicated team offering same-day call-back on service requests, 48-hour repair turnaround, and the availability of field application engineers.

Ciprico offers a complete line of high performance disk and tape controllers. As good listeners, we work with customers early in the design process and follow through with a highly personal level of customer support. Experience the Ciprico spirit and maximize the efficiency of your Multibus system by calling us: 612/559-2034.



**Ciprico Inc.**

2955 Xenium Lane
Plymouth, MN 55441
612/559-2034

European Office:

United Kingdom
Phone (0276) 682-149
Telex: 858306

CIPRICO

. . . where people listen—and respond.

Circle 27 on Reader Inquiry Card

At the lower end of the board marketplace, no vendor currently offers J-11-based products for either the Multibus or STD bus. Many Multibus vendors feel it would hardly be cost effective for them to compete with DEC by producing such a board; instead, most are concentrating on building next generation products around the 68020 or 32032 processor families.

Gespac's (Mesa, AZ) G-64 bus is not a direct competitor to the VME but rather a complement to it. The bus is similar to the VME; it uses the same form factor and DIN connector. The difference is that the VME is based on the double-height Eurocard and uses a 96-pin C type connector; whereas, the G-64 is based on the smaller single-height card and uses the 64-pin B type connector.

The G-64 is a much simpler bus than VME and, to some extent, has a lower performance because it does not support multiprocessing capabilities and has reduced addressing space.

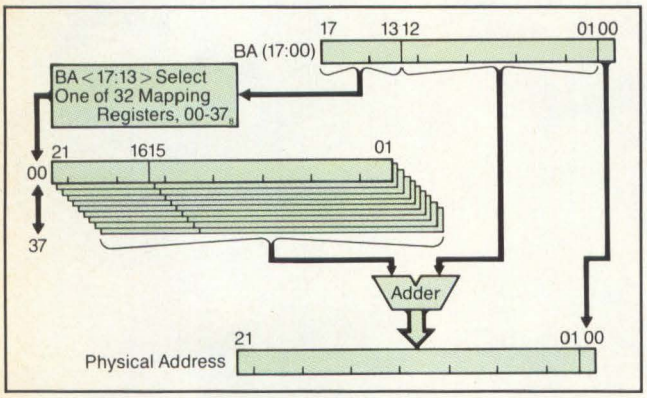



Figure 2: Construction of the physical address on the N1100 Unibus board is achieved through a set of mapping registers.

However, because of its low price and processor independence (8- or 16-bit machines can be supported), Gespac is targeting their G-64 line as a natural replacement for STD bus systems.

So far, Gespac is the only vendor in the low end of the marketplace to offer a J-11 CPU card. Their GESMPU-11 module includes an asynchronous RS-232-C/V24 compatible serial communication interface that can be selected to provide either a modem or a terminal connection. Like Logical Design Group's VME product, Gespac has based their serial I/O interface on the DC319 DLART chip for direct compatibility with standard DEC software. The DLART has an internal baud rate generator from 300 to 38.4K baud which can be selected either by software or by jumper. The board also contains a triple 16-bit timer/counter.

A relative newcomer to the US market, the company has been well-established in Europe for a number of years. However, at the present time, no second sourcing for the bus exists, although the company is currently investigating the possibilities. The G-64's direct competition comes mainly from the STE Bus. Most of the vendors for STE products are currently small and overseas (mainly UK). Hence, the STE has not established a strong foothold in the US to date.

Other recent designs based on the J-11 have been implemented on the existing DEC bus structures—the Unibus and the Q-Bus. They provide either an upgrade or add coprocessing power to existing DEC machines. For example, the N1100 from Nissho Electronics (Torrance, CA) is designed to enhance the performance of all the PDP-11/04/24/34 series of computers.

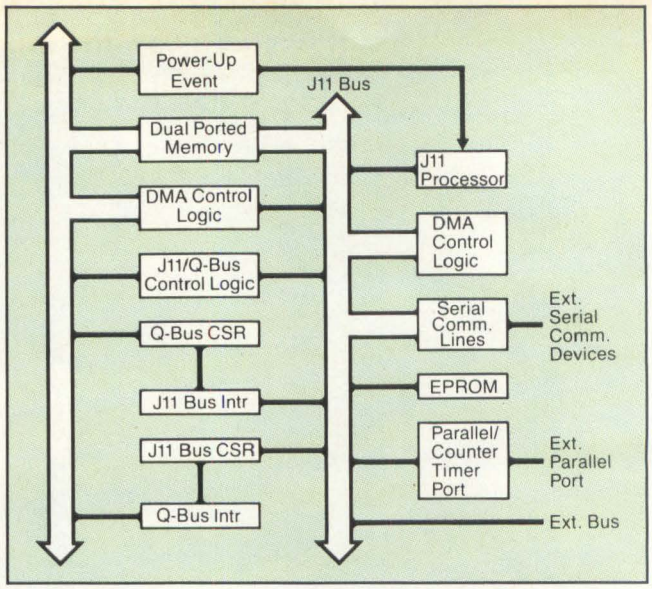



Figure 3: The dual bus architecture of the MDB front-end processor supports two bus structures—the Q-Bus and the J-11 bus.

Included on the standard HEX size Unibus board are the J-11 microprocessor, 2 Mbytes of DRAM memory, 2 asynchronous serial I/O parts and power up self-diagnostics.

The processor operates on the 18-bit backplane and provides Unibus mapping for the memory, located on its own independent 22-bit bus. Relocation expands the 18-bit Unibus address to the 22-bit main memory address, allowing the Unibus to access any location in main memory. This relocation or mapping of address is done by adding the contents of one of a set of mapping registers to incoming bits of the Unibus address (**Figure 2**).

When an address is taken from the Unibus, the mapping register is automatically selected and the contents read out. The 22-bit base address contained in the selected map register is added to the 12-bit offset in the Unibus address from the physical address. The program controls this process by selecting the contents of the mapping register and by enabling and disabling the Unibus map relocation function. Since the Unibus map registers may be accessed directly from the Unibus, a DMA device can also manipulate them. Nissho is currently targeting the product towards process control or CAD/CAM systems which may presently be restricted to 256 Kbytes of memory.

The offloading of time-consuming processing from the main processor to free it for other functions has long been the rationale behind the design of coprocessor boards. MDB's front-end

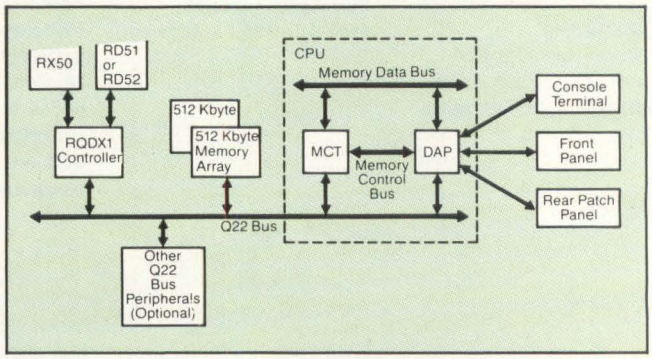



Figure 4: Early limitations of the MicroVAX-1 included a low-performance disk controller and lack of tape support.

Q-Bus processor, for example, performs data manipulation prior to the main processor intervention. One specific application is to perform protocol handshaking requirements so that only the necessary data, in its simplest form, is presented to the main processor. Dual-ported memory enhances this function by putting the data directly into memory without taking up Q-Bus bandwidth. The board, the JFEP11, consists of a J-11 processor chip, 22-bit/512 Kbytes dual-ported memory, 2 high speed DMA serial communication lines and a parallel counter/timer. The module supports two bus structures – the Q-Bus and the J-11 bus (**Figure 3**).

The J-11 may be programmed to initiate DMA transfers on the Q-Bus to or from the dual-ported memory on the module or any Q-Bus memory. The J-11 sets up and starts the transfers. Once the DMA transfer is in process, the J-11 is free to handle other functions; only the Q-Bus is pre-empted during the DMA transfers.

An external bus connector is also available to interface other devices directly to the board interfacing to the J-11 bus. Those devices may utilize the DMA feature with either the dual-ported memory or the I/O and interrupt feature interfacing with the J-11 processor. Since the devices connecting to the external bus cannot interface directly to the Q-Bus, the external connector requires a special cable to interface with an external device. And because the device is oriented around specific applications, all software for the module must be user generated, including the diagnostics.

The reason for this recent activity in product design around the J-11 stems from a customer base with a large investment in PDP-11 computers and software. To further protect that investment, DEC has ensured that their VAX line will accept, with minimal conversion, most types of PDP-11 programs. Naturally, there are some restrictions, but in may cases, PDP-11 programs require only simple recompilation to be ported to the VAX. The VAX even has a compatibility mode at the hardware level so that many PDP-11 programs can run on it unchanged.

The VAX is an expensive upgrade solution. Although the MicroVAX-1 (**Figure 4**) is DEC's least expensive VAX, it does not offer a compatibility mode with the PDP-11. Worse yet, the low performance of DEC's RQDX1 controller and the limitations of the Q-Bus have not helped the rapid acceptance of the MicroVAX-1. It also lacks a tape drive, and disk storage is limited to 31 Mbytes. This has restricted the application areas of the product.

Nevertheless, the future for the low-end VAX line of products looks far from bleak. DEC is working on a high speed 32-bit Eurocard bus structure that will support parallel VAX processors. Possibly making use of the 32-bit chip set described at the 1984 ISSCC, it may be that the new CPU cards will support the compatibility mode with the PDP-11. If this is so, many current PDP-11 users will find the next generation MicroVAXes a more expedient upgrade solution. DD

**How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.**

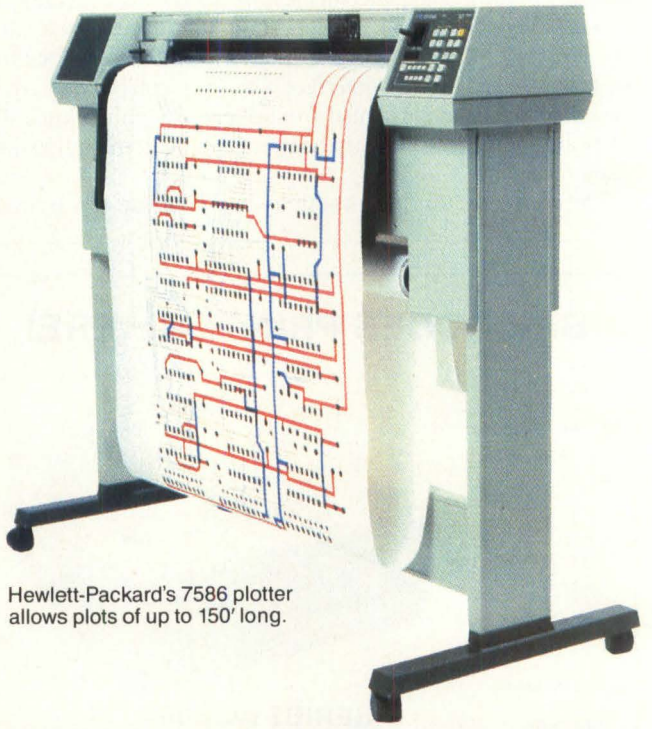
Very Useful . . . . . 610
Useful . . . . . 611
Somewhat Useful . . . . . 612

# VDI Spells Portability For Graphic Plotters

**by Joe Aseo, West Coast Technical Editor**

The need for graphic programs to explicitly specify plotter configurations may soon fade. This is the promise of the proposed Virtual Device Interface (VDI) now before the American National Standards Institute. Rather than binding the application program with specific drivers for input/output, VDI promotes device independence by providing a logical interface similar to that used in operating systems. Through common system calls rather than device-specific commands, application programs can be compatible with a wide variety of plotters.

This approach is no panacea for those programmers and end users who must maintain existing graphic programs. Older device drivers could require extensive modifications to work with VDI system calls. Furthermore, performance may suffer since application programs cannot directly control the plotter's actions. As a result, systems architects must carefully balance the needs for portability and performance.



Hewlett-Packard's 7586 plotter allows plots of up to 150' long.

## Graphics Tried And True

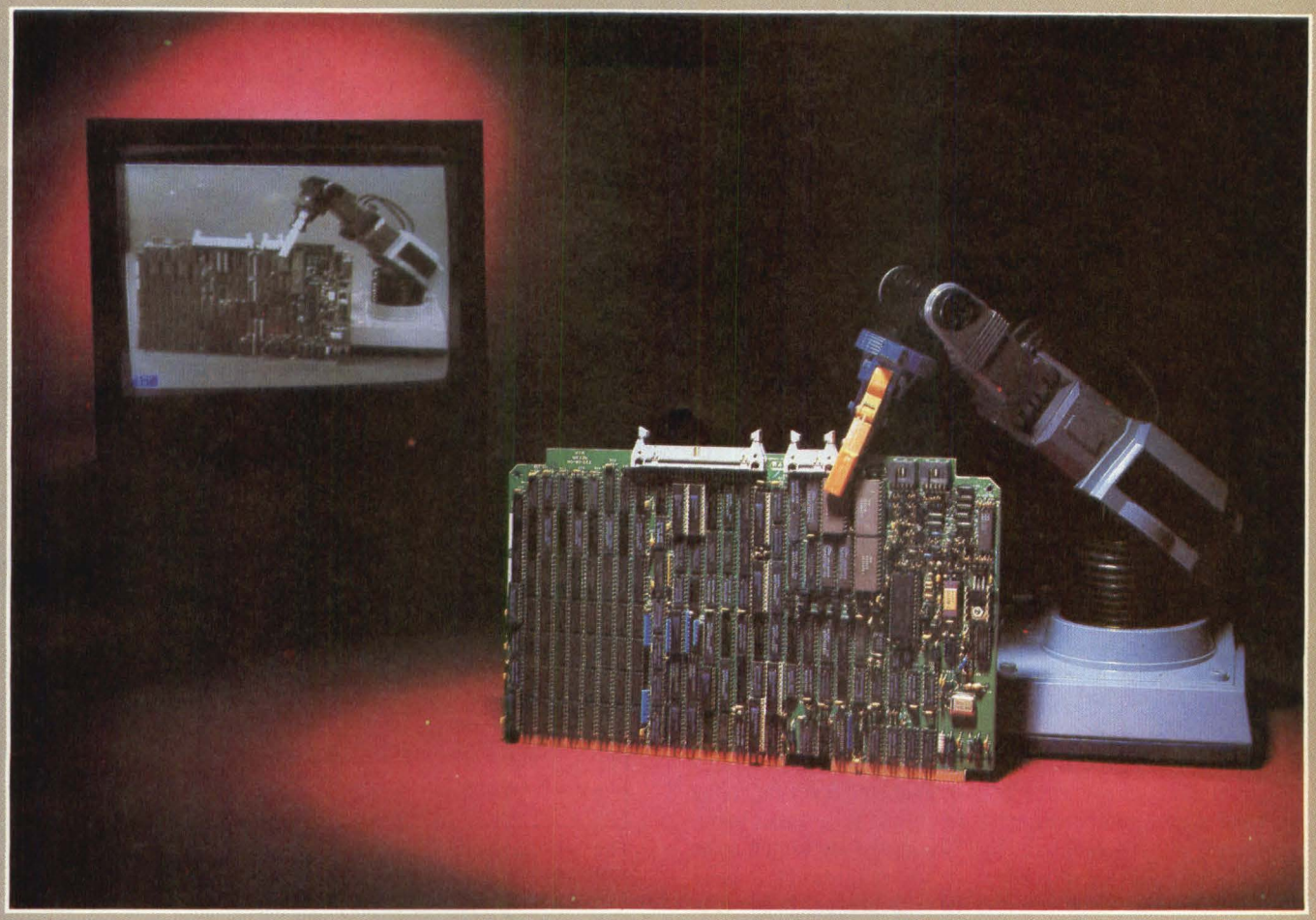
Until now, graphic applications have, by necessity, closely coupled application programs with device-specific routines for optimum performance (**Figure 1**). Prior to the development of dedicated graphics controllers, the host CPU was responsible for both generating the images for the display and plotter as well as running the applications programs (both CPU-intensive tasks). To maintain optimum performance, these input/output routines were typically written in assembly language and accessed as subroutine calls from Fortran application programs.

This approach works best when there is a limited number of choices of input and output. For example, hard copy output was, for many years, largely limited to pen plotters, so application programs contained routines that controlled specific plotters such as the CalComp 907 or Hewlett-Packard 7580. With a similar approach, pen plotters emulated the commands of storage tube display terminals (such as the Tektronix 4010), taking advantage of graphic utilities like PLOT 10.

Because of the tremendous software investment in existing graphics applications, vendors of unsupported plotters must provide some form of upward compatibility so that existing programs can also control their plotters. Typically, this takes the form of "call" or "command" compatibility where the plotter is able to interpret the device-specific instructions issued by the application and execute corresponding instructions that it understands.

However, the use of "de facto" industry standards has its limitations. Most application programs with embedded device drivers cannot easily be transferred to other hard copy devices such as electrostatic or laser plotters. Commands to draw such graphic primitives as lines and arcs may differ. Likewise, data must often be converted from display lists composed of vector endpoints (used in pen plotters and storage tube displays) to bit maps used to address individual points (used in electrostatic plotters and CRT terminals).

# REAL-TIME IMAGE PROCESSOR — $2,995



## MIP-512 - The Single Board Multibus Machine Vision System

- **512 x 512 resolution**
- **8 bits/pixel up to 24 bits/pixel**
- **4:3 or 1:1 aspect ratio**
- **16.7 million color LUT**
- **Hardware pan, scroll and zoom**
- **Dual ported video RAM for true DMA**
- **IEEE-796 (Multibus) compatible**
- **8 bit frame grabber**
- **90nsec/pixel video ALU**
- **IP software library (C, Fortran)**
- **Image processing functions:**
  - **addition & subtraction**
  - **averaging**
  - **convolution (N x M)**

Image processing technology need not cost an arm and a leg. With the Matrox MIP-512 you can get full 8 bit data acquisition, 8 bit image storage and 90nsec/pixel image processing **all on one Multibus board and for only $2,995 in singles.**

**REAL-TIME IMAGE ACQUISITION**
An 8 bit flash A/D converter is used for digitizing an external video signal. External sync genlock or internal sync generation are software selectable. On-board programmable offset and gain controls and input look-up tables are provided for real-time pre-processing of raw video data.

**IMAGE STORAGE AND DISPLAY**
The MIP-512 contains 256K Bytes of dual ported video RAM for storing a 512 x 512 x 8 image. Images can be loaded or unloaded from Multibus to video memory under DMA control in just a fraction of a second.

MULTIBUS - TM INTEL

The MIP-512 supports instantaneous pixel by pixel panning and scrolling of images, and zooming by a factor of x2 or x4. Up to 256 colors or shades of gray can be displayed from the 16.7 million color LUT.

**REAL-TIME IMAGE PROCESSING**
A 90nsec/pixel video ALU is provided for performing real-time arithmetic and logical operations on image data. The MIP-512 supports several standard image processing functions including frame addition and subtraction, exponentially weighted frame averaging, low and high pass filtering and convolution with an N x M kernal. All computations are performed at high speed by the MIP-512 without burdening the host CPU.

In addition to state-of-the-art graphics and imaging boards, Matrox also supplies monitors, cardcages, CPU cards, memory boards and communication controllers for complete OEM display system requirements.

*Call now for a complete documentation package.*

**matrox**
**electronic systems ltd.**

**1055 St-Régis Blvd**
**Dorval, Québec**
**H9P 2T4**
**Tel.: (514) 685-2630**
**Telex: 05-822798**

Circle 51 on Reader Inquiry Card

Another drawback is that existing applications cannot use a new plotter's unique features unless the device drivers are rewritten. For example, graphic programs that call for pen-plotter output cannot take advantage of an electrostatic plotter's ability to do shading, toning or pattern filling. In a sense, the current approach freezes an application into minimal functionality as plotter technology advances.

## Planned Portability

Promising a more orderly growth path for graphics programs, VDI separates device-independent code (application programs) from device-dependent drivers. If implemented, application programs would substitute a set of logical system calls to execute a common set of graphic primitives rather than embedded routines of device-specific commands (**Figure 2**).

This scheme is much like that used in operating systems to isolate application programs and the device drivers that control such peripherals as disk drives and printers. In fact, current implementations of the proposed VDI standard – the Graphic System Extension from Digital Research and GSS-Drivers from Graphic Software Systems – look very much like operating systems with command interpreters and device-level drivers (**Figure 3**).

As a result, systems architects no longer need to consider the target hardware that their application programs will support. Using VDI commands, graphic primitives and attributes assures that the desired action will be carried out. Even if a specific plotter is unable to execute or emulate the function, a flag is set and the program continues execution. On the other hand, unsupported commands in a closely coupled implementation could cause fatal errors that suspend the execution of that same program. In addition, device-specific attributes can be handled blindly using a feature called "bundled attributes," or the application program can query the device driver before taking any action.

Bundled attributes makes the plotter, rather than the application program, responsible for specific actions such as drawing circles and area filling. Contained within the driver are the routines required to carry out the desired VDI command. For example, a VDI command to fill a polygon might be carried out as a solid color by a pen plotter or as a pattern fill by a laser plotter. In this way, VDI can easily accommodate various levels of capabilities within each device.

If it is necessary for application programs to know specific device attributes, VDI provides a query capability so the program can interrogate the device driver to determine such capabilities as resolution, pattern fill, area fill and polygons. These options give the systems architect the option of knowing as little or as much about the target hardware as the application dictates.

As with the closely coupled approach, there are limitations to VDI. Since there is a logical interface imposed between the application program and the physical device, there will be a significant amount of CPU overhead associated with the translation of system-level calls to the actual device-level commands. This performance penalty may be small if the plotter's firmware is sophisticated enough to handle system calls with a single command. On the other hand, if the plotter does not directly support a given graphic primitive, e.g., area fill, then the emulation required to carry out the request may burden the host CPU with additional overhead.

It is difficult (if not impossible) to provide a set of commands and graphic primitives that take advantage of specific features offered by each of a wide variety of plotters. This is especially true for raster-oriented devices such as electrostatic, thermal and laser plotters. The primitives employed in VDI emphasize line-oriented display lists rather than bit maps that describe individual points. As a result, these vectors must be converted to individual points comprising the line before it can be plotted on raster devices.

Likewise, pen plotters cannot readily execute graphic primitives such as shading, toning and gray scales handled by bit-addressable raster devices. Such compromises can limit the usefulness of VDI for those users seeking to take advantage of special features not directly supported.

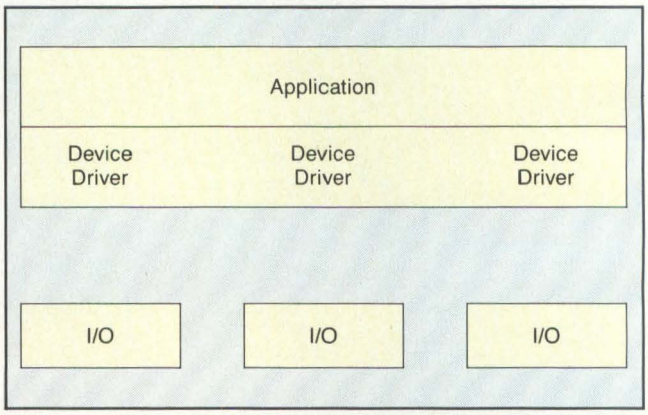



Figure 1: Conventional graphics programs are a monolithic piece of code with device drivers embedded with the object code. This is typically done for optimum performance, but hinders portability.

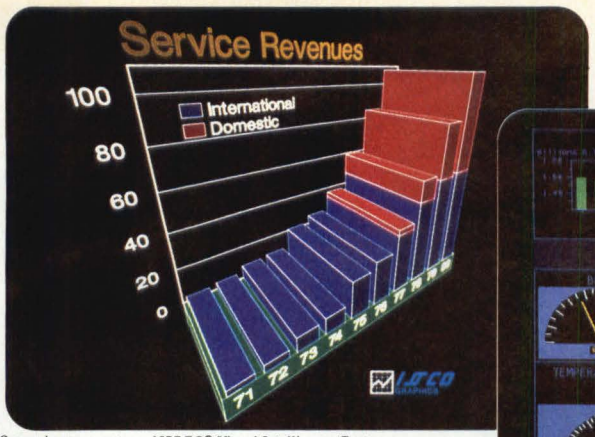
## Design Considerations

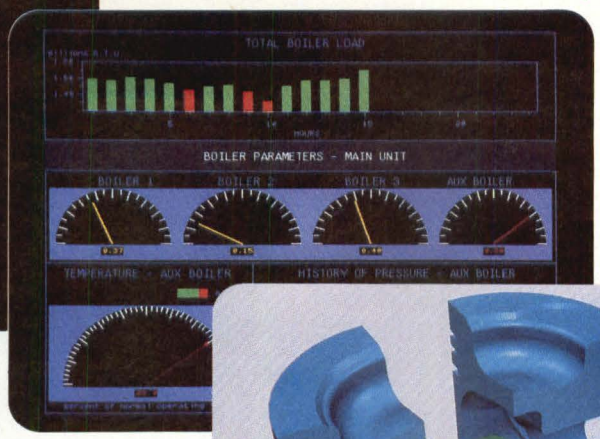
Both *de facto* standards and the Virtual Device Interface have their place when establishing the proper software interface between plotters and host computers, but their benefits must be contrasted with their drawbacks. The advantage of optimum performance comes at a price of limited support for a wide variety of devices. Portability often calls for compromises in performance. Systems architects should carefully look at the requirements of their application before selecting either approach.

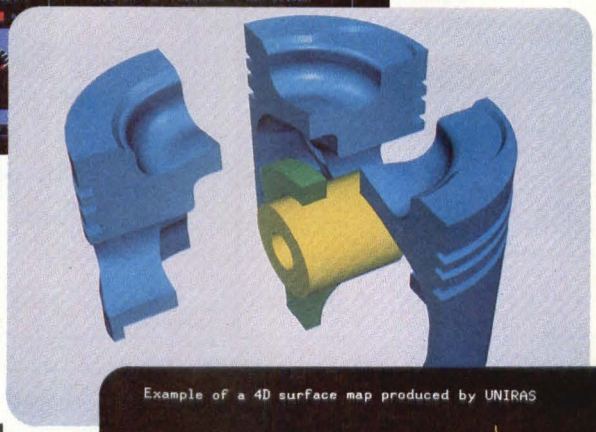
In general, those applications best suited to implement VDI demand that a wide variety of plotters be supported. New applications being developed for the personal computer marketplace is one such example. Software developers are often unsure of what the output device and its graphics capability will be. The ability to either query a specific device to determine its graphic attributes or to utilize bundled attributes to carry out common graphics primitives allows the developer to be ignorant of the target environment.

Portability may also be a concern, even when the plotter devices are well characterized. The desired application could involve a large CAD system that must support the output of working diagrams at one stage of a project's life, but also support final artwork for actual production. As a result, an electrostatic plotter may be selected for working diagrams because

See us in Booth #1828 at NCGA



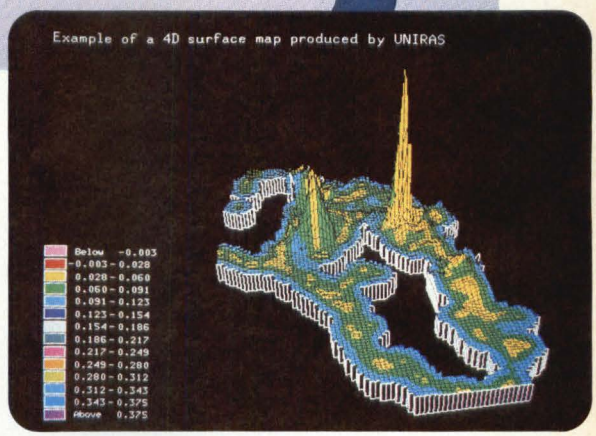



*Screen images courtesy of ISSCO® Visual Intelligence Corp., PDA Engineering, and UNIRAS®, Inc.*

# Raster's Model One/10.

## High performance has rarely looked so good. Or cost so little.




Our high performance Model One/10 graphics terminal lets you run today's most popular engineering, technical and business presentation graphics software.

Programs like PATRAN, ANSYS, TEMPLATE, DI-3000, UNIRAS, DataViews, and TELL-A-GRAF, to name but a few.

What's more, Raster Technologies' Model One/10 is VT-100 compatible and emulates the Tektronix 4014.

And you don't have to pay a high price to get all its high performance features. Like a vector writing rate of over one million pixels/second. Support for 256 colors from a palette of 16.7 million with two additional overlay planes. Total image memory of 1024 x 512. 640 x 480 resolution on a 60 Hz flicker-free, non-interlaced 14″ screen. Fully programmable look-up tables and more.

Just as important, you also get the application development tools made famous by the Model One family. With over 150 graphics commands, including local debugger, command interpreter, alphanumeric emulation and powerful local display list.

So call today. And watch your favorite programs for less.

**Raster Technologies**

**The benchmark of computer graphics.**

Nine Executive Park Drive
North Billerica, MA 01862
(617) 667-8900 TWX 710-347-0202
1-800-4RASTER

**Circle 20 on Reader Inquiry Card**

*PATRAN is a trademark of PDA Engineering. TEMPLATE is a trademark of MEGATEK Corp. UNIRAS is a trademark of UNIRAS® Inc. DataViews is a trademark of Visual Intelligence Corp. TELL-A-GRAF is a trademark of ISSCO. ANSYS is a trademark of SWANSON Analysis Corp. DI-3000 is a trademark of Precision Visuals, Inc.*

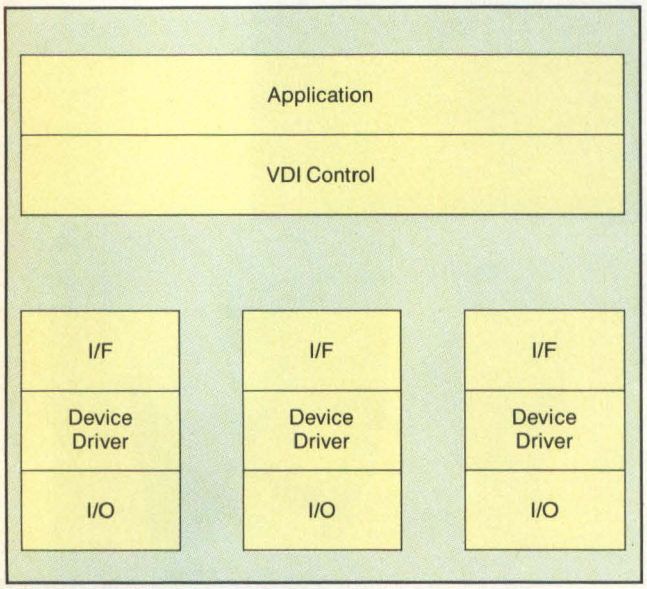
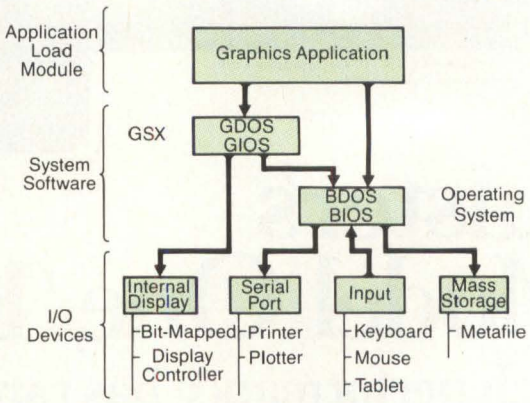



Figure 2: The Virtual Device Interface (VDI) separates device independent code (application programs) from the routines that drive specific plotters (device drivers). The VDI interface then translates system calls to physical commands.

Figure 3: The Graphic System Extension (GSX) from Digital Research implements the Virtual Device Interface in much the same manner as an operating system with the Graphic Device Operating System (GDOS) handling logical system calls and the Graphic Input/Output System managing the physical device drivers.






of its high throughput, but a photoplotter may be used for the high resolution of the finished drawings.

On the other hand, *de facto* standards – either the PLOT 10 library from Tektronix, Hewlett-Packard's Graphics Language or utilities developed for the CalComp 907 plotter – work best in situations where the choice of plotters has narrowed. Existing graphics applications with embedded drivers form the largest category. Software maintenance costs would rise inexorably should these programs be rewritten to implement VDI. If the developers of such programs wish to move to other plotter types (e.g., pen to electrostatic), many vendors provide some level of call compatibility so that software need not be rewritten.

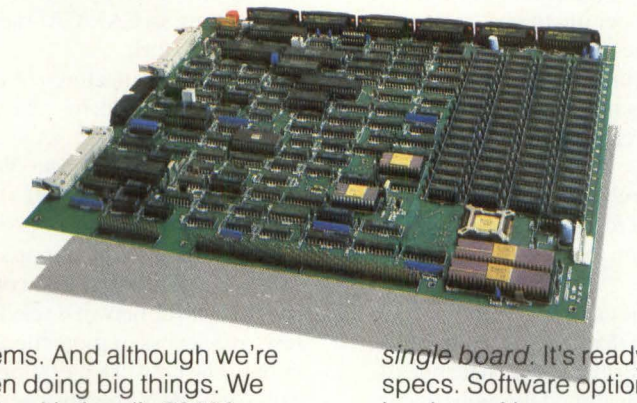
Furthermore, there are applications that can best utilize only one type of plotter. Image processing, for example, is best suited to raster-oriented devices since the emphasis is on addressing individual bits rather than dealing with more abstract objects such as lines or circles. In fact, such applications may want to take advantage of specific attributes of a specific plotter type such as shading, toning and gray scale imaging, not supported in the broadly based VDI specification.

As a result, *de facto* standards will not disappear as VDI gains acceptance. In fact, system architects now have an expanded list of options and should no longer feel locked into the status quo. DD

**How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.**

Very Useful . . . . . 604
Useful . . . . . 605
Somewhat Useful . . . . . 606

# 32 BIT TECHNOLOGY FROM A 2 BIT START-UP?



## ABSOLUTELY!

We're Goodspeed Systems. And although we're new on the scene, we've been doing big things. We took an exciting new chip set — National's 32000 Series — and created a 32-bit single board computer. The GS-32 delivers true ***32/32*** performance — plus some big advantages no one else can match:

**The Time Advantage:** We can shorten your time to market with our tested, proven boards. The GS-32 is available now; there's no wait for the 32-bit power you need today.

**The Design Advantage:** Our flexible, fully socketed design offers 32-bit processing, up to 2 MB memory, I/O and mass storage interfacing, *all on a single board*. It's ready to plug in or expand to your specs. Software options scaled to your application level, too. Now you can have 32-bit performance without a workstation or even card cage.

**The Price Advantage:** The GS-32 delivers full 32-bit performance at a fraction of the cost of bussed systems. Our price-to-power ratio is unmatched. And that means it can slash *your* overall system costs for that competitive edge.

The GS-32 from Goodspeed Systems. The little company with the big board. If you're ready for 32-bit technology, call for the name of your representative:

**1-800-243-8160**

**GOODSPEED**
*SYSTEMS*

*23 Main Street, P.O. Box 29, East Haddam, CT 06423*

**See us at Mini-Micro Booth 226.**

**Circle 8 on Reader Inquiry Card**

# Efficient Communication Eludes Design Networks

by Julie Pingry, Senior Editor

Workstations can provide an engineer with local computing power, but members of a design team must cooperate closely. Vendors of standalone CAE and CAD systems generally offer local area network communications to allow users to share data and resources, touting a complete design environment. Despite optimistic claims, these networks do not allow all stages of the design cycle to interact smoothly. Either the equipment vendor or the user generally must write some network application and translation software to allow communication of data between engineering, design and test tools.

CAE/CAD networking schemes range from proprietary tightly coupled systems for connecting one brand of workstation to using industry-standard hardware and protocols adaptable to a variety of machines. Proprietary networking systems limit meaningful communication to machines from one vendor. Network standards are emerging, but do not address actual application-level format compatibility. Application software for either type of network is generally specific to one company.

With several of one vendor's engineering and design stations networked, the combined resources are available to each individual user. CAE/CAD applications running on these micro- and supermicro-based workstations ease parts of the PC board and IC design cycle such as schematic capture, simulation and timing verification. However, their relatively limited processing power generally makes layout and routing too time-consuming to be practical, so communication to and from larger systems is desirable.

Though a standard network scheme can connect into various computers, it is important to realize that the way information is transmitted is not the same as the format in which it appears. No matter how efficiently data is transmitted through a cable, if the data arrives in a format the receiving machine cannot use, no meaningful communication can take place.

## Workstations' Domains

Engineering and design automation has been largely in the form of tools to address localized problems. Standalone workstations may be adequate for schematic and netlist generation as well as simulation and timing verification of small circuits. To accommodate larger designs divided into simultaneous tasks, workstation vendors allow transparent connection of their products. This set-up allows engineers and designers working as a team to share files and expensive resources like disk space and laser printers.

As a manfacturer of computing engines sold to OEMs adding CAE and CAD software, Apollo Computers (Chelmsford, MA) built networking into all of their products and the proprietary AEGIS operating system under which they run. Connected in the "Domain" environment, a user at any Apollo workstation can directly access all files and resources as though they were local, no matter where they physically reside in the network. In effect, the network in this distributed system acts as an extended backplane.

In the Apollo architecture, directories, files, interprocess mailboxes, executable modules, bit maps and other system entities are all stored in the same object format. Networking features such as demand paging (as opposed to transfer of a complete file), virtual memory, concurrency control and standard object naming structures allow distributed applications. These are characteristics of the AEGIS OS, not separate network protocols demanding their own processing time and power.

With the advantages of Domain networking and architecture, Apollo equipment is a popular base for a variety of design and engineering workstations. The Apollo DN series includes models at different performance specs all based on the same architecture, so CAE/CAD application tools can communicate over the network.

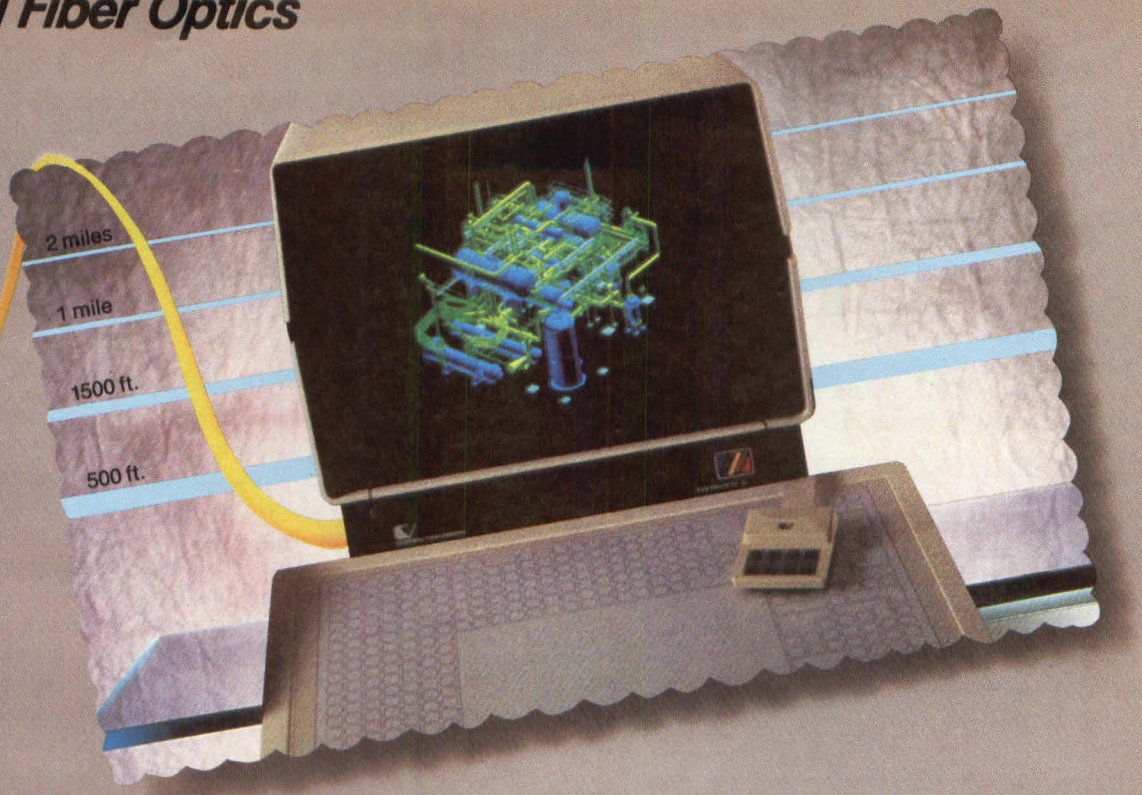
A larger manufacturer of engines often used as a base for design and engineering stations is Digital Equipment Corp. (Hudson, MA). Their VAX computers cover a wide range of performance. From the VAXstation (MicroVAX-I with graphics) through the 8600, all VAX machines run under VMS and the DECnet network protocols.

DECnet Phase IV supports LAN-style Ethernet cabling, as well as X.25, point-to-point or multidrop connnection (**Figure 1**). High-level network services on DECnet include remote resource access, remote file and record access and virtual terminal. The network will support other Digital computers, but using only VAX systems operating under VMS, the file structures are identical and all services are available.

Though both Apollo and Digital have developed fully configured networks, the approaches differ. DECnet is effective, but not built into the VMS operating system. Networking was a design premise at the conception of the Apollo line, so their communication is streamlined. On the other hand, DECnet is not machine-specific since it is not part of VMS. In fact, the spec is published, and Technology Concepts (Sudbury, MA) has developed Portable DECnet to allow other types of computer to run the DECnet protocols.

Vendors of engineering and design workstations based on other hardware have realized the importance of networking as well. Many use *de facto* standards that exist only at the lowest level of system and communication software, namely UNIX and published protocols. The Department of Defense Internet Protocol/Transmission Control Protocol (IP/TCP) networking software is popular and developed around UNIX.

# Artel Fiber Optics




# Put your Computervision Instaview anywhere you want it.

*Artel fiber optic systems transmit high resolution graphics video and data up to 2 miles without signal degradation, a feat impossible with coaxial cable.*

If you're using Computervision Instaview color or monochrome CAD/CAM workstations, you know the problem. Coaxial cable limits the distance workstations can be placed from your graphics processor.

Artel's compact CV100 Series fiber optic systems change all that. They can reliably transmit video images and data up to two miles. You can even run the cable outdoors.

Artel's products are plug-compatible to the Computervision system. They give you reliable, noise-free high resolution graphics transmission, communications security, intrinsic safety, lightning immunity, and freedom from ground faults.

Fiber optic cable is small, lightweight, and only a fraction the size of coaxial cable. You can run it right next to power lines, between buildings, or alongside electrical equipment without using special conduits or shielding. It's easily installed inside a new or existing office building or throughout an industrial complex.

We've installed CAD/CAM fiber optic communication systems in aerospace, automotive, and many other manufacturing companies. These companies have had our systems operating continuously for years. We're also a prime vendor to the U.S. government.

If you're anxious to go the distance, call or write Harold Milton, Artel Communications Corporation, P.O. Box 100, West Side Station, Worcester, MA 01602, (617) 752-5690.

ARTEL

*Computervision and Instaview are registered trademarks of Computervision Corporation, Bedford, MA. Photo courtesy of Computervision.*

***Light years ahead in communications.***

**Circle 7 on Reader Inquiry Card**

**See Us at COMPUTER GRAPHICS 85 in Dallas, Booth 145-147**

One firm producing general-purpose workstation engines and promoting standards is Sun Microsystems (Mountain View, CA). They use UNIX on a 68000 base and have a program to encourage third-party software vendors to offer their communication products on Sun hardware. Not all of the packages are IP/TCP protocols. For example, Network Research (Santa Monica, CA) Fusion 3.0 uses Xerox XNS protocols to connect to 8086/7, 8088, VAX and PDP hardware as well as 68000s. Access to IBM mainframes is supported by Spartacus (Bedford, MA) and FlexComm (Seattle, WA).

The DOD network protocols are attractive, however. In addition to being designed for UNIX systems, IP/TCP protocols include several session and presentation level services on which

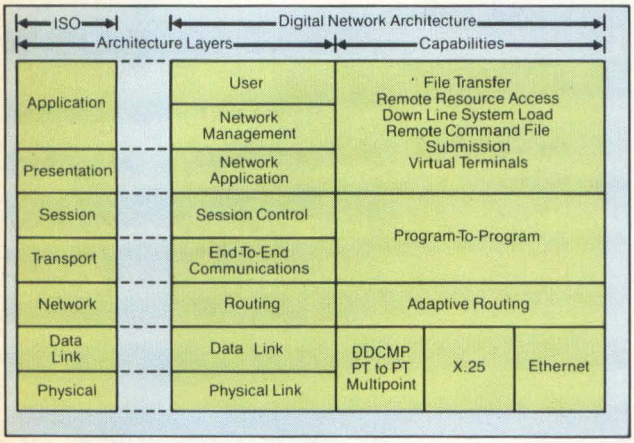



Figure 1: DECnet covers all seven levels of the standard networking Open System Interconnect (OSI) model and provides a variety of network services to Digital computers.

applications are easily built. Among other workstation suppliers, Tektronix (Wilsonville, OR) uses IP/TCP and Ethernet. For computers not equipped with IP/TCP protocols, many use the Wollongong Group's (Palo Alto, CA) package for computers running under VMS, UNIX V or BSD 4.2. Their IP/TCP services include remote logon to a host, file transfer that automatically resolves format differences and electronic mail.

Companies that offer boards with network protocol layers one through four often provide standard IP/TCP as well. For example, Communication Machinery (Santa Barbara, CA) has protocol software to run under VMS, UNIX and VERSAdos, while Excelan (San Jose, CA) offers upper level software under UNIX, VMS and RSX-11M.

Using standard network protocols has advantages in industry compatibility, but may entail more system overhead than protocols designed for one operating system. They also solve only part of the problem: devices on the network still must use the same formats at the unstandardized application level for transparent communication to be accomplished.

Sun offers source code for their Network File System (NFS) and underlying Remote Procedure Call (RPC) at the upper network levels to the public in hopes that the protocols will become intervendor standards. Designed to skirt explicit file transfer commands, NFS allows transparent access to all files on the network. As in Apollo's system, only one copy of each file exists, so a user does not need to know where a file resides and define a location and pathname. The single copy of a file is a feature that also ensures consistent data for all network users. With NFS, application and file access can be extended across a network of multiple vendor computers if the user is willing to write executable code compatible with the published protocol.

Until recently, networking was not standard with all workstations and some users chose turnkey network systems custom-designed for their hardware, but not necessarily for design applications. Though networking is now a standard workstation feature, upper level protocols are only designed for applications from that vendor. Since few people like to be tied into one company for all of their equipment, design departments may still have a problem communicating.

## Connecting Design Stages

With all of the talk of networking, it is easy to forget that the problem to be solved is how to computerize the design cycle (**Figure 2**). Workstations were initially promoted as not only a more efficient way to perform engineering tasks like schematic capture, but, with a network, as a way to coherently automate an entire engineering and design team. In reality, various stages of the design cycle require different compute, graphics and disk performance. So just as applications for each stage may be separate packages, they may run on different machines.

IBM PCs have invaded many environments, and several firms provide packages for the IBM PC to act as an engineering front end. Since the PC does not have the memory or processing speed to adequately run all engineering applications, companies who have developed PC-based CAD applications like Futurenet (Canoga Park, CA) and Personal CAD (Los Gatos, CA) offer translation interfaces to other tools. Though many network schemes have been developed for connecting IBM PCs, most cannot link both larger systems and PCs. Standard schemes could provide low-level network connections, but applications would still need translations.

Despite these variable processing power needs, supermicro

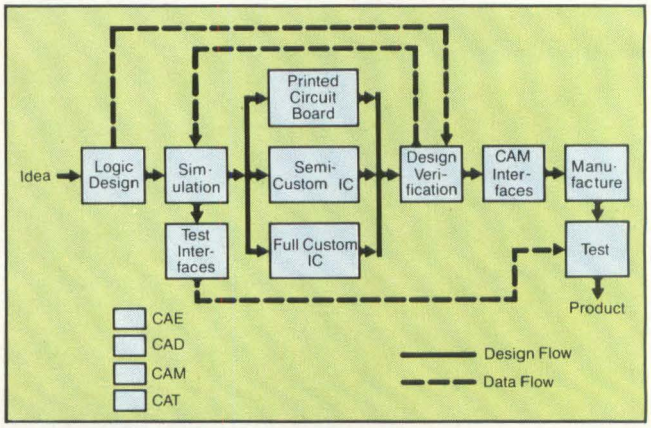
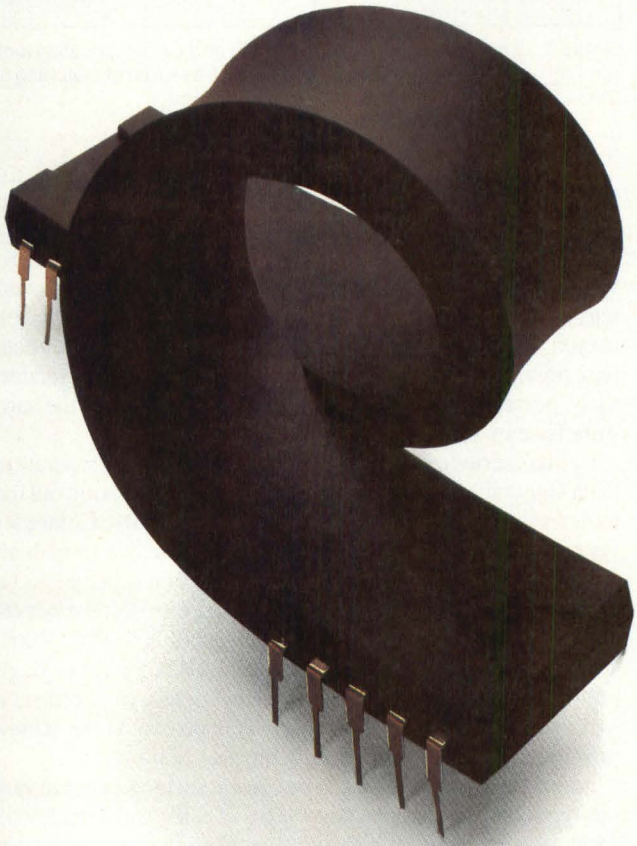



Figure 2: From initial idea through manufacture and test, data must flow from one application to the next and, often, back again. What this Calma diagram does not show is that current tools are often not well integrated and communication may not be possible between various vendors' computers and applications.

workstations in a network have been promoted as a way for many design departments to computerize without buying a mainframe. Advantages of a network of micros over a mainframe include lower initial investment and adding CPU power with each user. On the negative side, large tasks and programs execute much more slowly. Use of CPU power for large tasks is more effective with a mainframe; partitioning a task manually for load sharing across a network is difficult, if possible at all.

# DON'T LET SPEED SLOW YOU DOWN.



**The Mostek BiPort FIFO takes your processor out of the loop.**

Until now, buffering two devices with different data rates meant one of two things. Either extra hardware design effort. Or software loops to slow your processor down while it's waiting for a peripheral or a coprocessor to be available.

But now there's a better way. The BiPort™ FIFO from Mostek. You can do away with the need for extra hardware design and software loops, and let your processor operate at its optimal performance level.

Our MK4501 is a 12.5 MHz CMOS device with access times as fast as 65 ns. It can handle asynchronous and simultaneous reads and writes from each respective port. And its 512 x 9 architecture is fully expandable by word width or depth. It even has a retransmit capability.

There's nothing quite like it. Except our MK4511. The MK4511 is similar, but has the added advantage of being a true dual-port RAM that's randomly-accessible for bi-directional applications.

So put a speedy end to your interface problems. Call or write Mostek for more details. Mostek Corp., 1215 W. Crosby Road, MS1051, Carrollton, Texas 75006, 214/466-7479. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5.681.157-9.

BiPort is a trademark of Mostek Corp.

UNITED TECHNOLOGIES MOSTEK

See us at Electro and Mini Micro N.E.

Circle 16 on Reader Inquiry Card

Moreover, with micro- or supermicro-based workstations, applications are often limited to initial schematic and netlist generation. At the next stages of the cycle, simulation and layout, a larger engine is preferable for all but small ICs and boards. CAE/CAD firms now offer translation packages to VAX and IBM computers that convert workstation output into a format usable as input for the larger system.

Perhaps the biggest pitfall in the translation packages provided by workstation vendors is that most can only upload from an early stage tool on the workstation to the larger machine for the next design phase, but can not download new data from simulation and layout back to the engineer for iterations. Users of both Valid (Mountain View, CA) and Daisy (Sunnyvale, CA) workstations, pleased with the automation these tools provide engineers, have been slowed down greatly by the lack of easy back annotation.

A netlist compiled on a workstation may be transformed and uploaded, for example, to a large computer running GenRad's (Santa Clara, CA) HILO or Calma's (Austin, TX) TEGAS for circuit simulation and timing verification. Small circuits or portions of circuits may be simulated on the workstation.

No matter what system is used for simulation, gate array designs are generally laid out by the semicustom vendor. To get actual delay data on the basis of the layout for resimulation, either the IC vendor must output to the user's simulator format or the user must pay for CPU time at the semicustom house. This outside compute-time cost defeats one of the justifications for in-house workstations.

For PC board layout, a common interface is to a VAX running Scientific Calculations' (Fisher, NY) Scicards. Translation packages allow schematics captured on various workstations to be used as input for Scicards. But again, the engineer cannot download timing delay data based on actual wire lengths or information on IC swaps performed during layout back into the workstation for simulation. If timing problems are found after layout, designers must either work at the VAX and manually annotate at the workstation for a matching file or begin from scratch at the workstation and upload a changed file.

Even if those compute-intensive tasks are not performed in-house, the storage and the compute power of a workstation, initially adequate, may soon be outgrown as board and chip densities increase. Archiving for expanding engineering and design efforts may create huge databases as well. Most users want the option of a supermini or mainframe in their design environment and current translator links may not be adequate.

## Sharing The Database

Running applications that interface smoothly at each stage on a variety of hardware bases does not necessarily mean using one vendor's workstations and limited-function translation packages. Some CAE/CAD firms provide software for a variety of hardware systems; these companies need communication between various computer systems. To compete with workstations, they must provide networks; the point-to-point translation links in many workstation environments are inadequate for integrated design.

One approach to communication between various hardware tools is to provide a shared database around which design stage applications are built; the applications may reside on several types of equipment. Design systems cooperate this way in the CIEE environment from Racal-Redac (Westford, MA). Applications for IBM PC, VAX and, soon, Apollo hardware are all built around a common database (**Figure 3**) to ensure accuracy in going from one design state to the next.

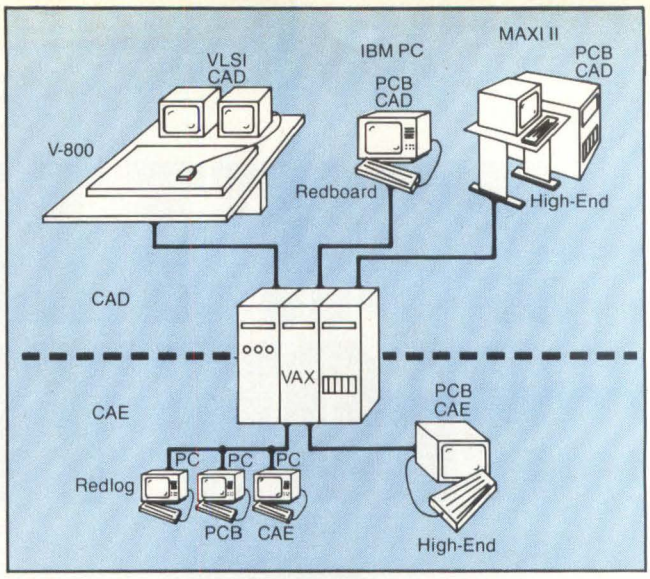



Figure 3: Using one central database, CAE and CAD application tools running on various types of hardware can be assured of matching information in the Racal-Redac CIEE environment.

The charter of CAE Systems (Sunnyvale, CA) is also to provide software tools to run on a variety of hardware bases, including Apollo, Sun, DEC and, with their recent acquisition by Tektronix, Tek's 6000 line. Their open architecture integrated database provides the hooks for building interfaces to other vendors' tools, presenting the same user interface regardless of the hardware base or software application being used.

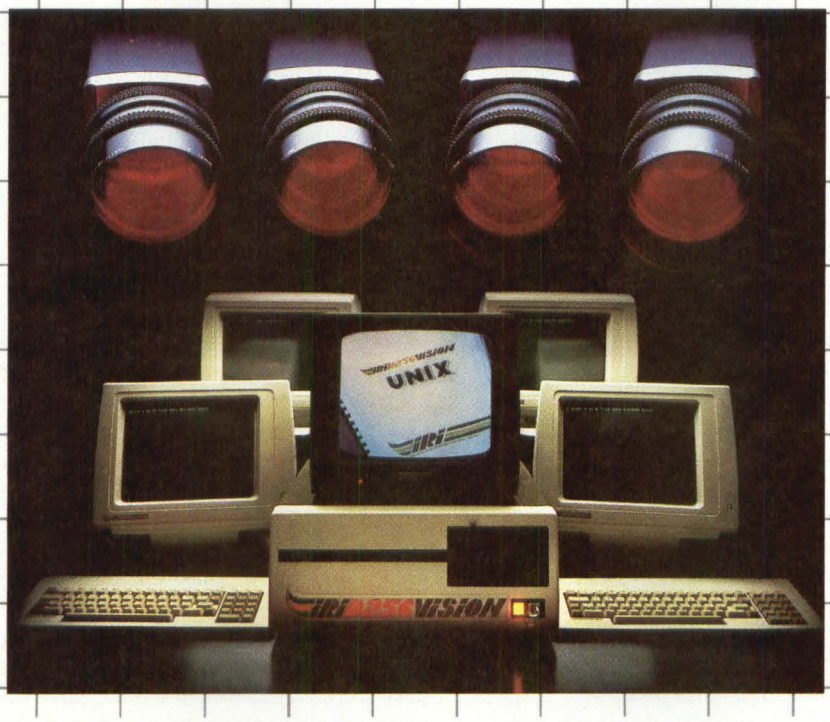
Calma's series of engineering and design packages operate on Data General, Apollo and VAX computers. They point out that tools from large, longer-established companies like Computervision (Bedford, MA), Intergraph (Huntsville, AL) and themselves tend to rate better on integration between applications but not as well on speed compared to smaller companies' products. The TNET link Calma provides between their Apollo-based TEGAStation and the VAX operates over RS-232 for throughput of 300 bytes, or RS-422 for 2 Kbytes/sec. In contrast, 10 Mbit/sec Ethernet systems with IP/TCP protocols can achieve throughput of several hundred Kbits/sec or more.

Any time information must be communicated between various types of hardware, the advantages of using native binary file format are out of reach. Operating systems may define sequential, direct access and indexed sequential file formats of either variable or fixed length for particular types of files as well as ASCII and EBCDIC. The number of possible file formats and the specifics of length and structure vary greatly from one OS to another. Transferring binary files to a computer under a different OS takes considerable translation effort.

More complex network operations than file transfer create larger problems. Remote logon and terminal emulation services require packages to make one type of computer look like another company's terminal. To execute an application on another machine, the network software must be able to execute the OS commands of the remote computer. These applications may be written between two tools, but for a heterogeneous network, it may never become practical to send anything but ASCII files.

Nearly all transmissions between unlike hardware are in ASCII format. Nontext information may be safely interpreted

# HOW TO DEVELOP YOUR VISION.




## INTRODUCING THE D 256 VISION DEVELOPMENT SYSTEM.

Name your vision application need: Quality Assurance. Process Control. OCR Applications. Classification and Sorting. Machine Monitoring and Safety. Material Handling. PCB Inspection. Image Processing. Keyboard Inspection. Robot Guidance. Or, Educational Applications.

Now you can develop the vision programs you need with The D 256 Vision Development System from IRI. The D 256 is a stand-alone system based upon the new world standard multi-user program development environment: UNIX, and IRI's unique Iconic Kernel System(IKS™). The IKS is a software package that provides a comprehensive set of over 300 software modules which can be used as vision software "building-blocks," for your application development. This means that now you can develop programs on the D 256 which can operate on the D 256 or on any IRI P 256 Target System—the vision price/performance leader for inspection and other industrial applications.

If you're considering developing computer vision systems for your applications, look to the D 256 Vision Development System from IRI. And, our worthwhile line of options including color input and output.

The IRI D 256 user-friendly programming systems are now operating at major corporate research labs in the U.S., Europe and Japan. Get in touch. We'll be happy to show you ways to develop your vision. For a demonstration, more information, or a direct quote, call: Richard Carroll, V.P. Sales (619) 438-4424.
International Robomation/Intelligence
2281 Las Palmas Drive, Carlsbad, CA 92008

IRI

**THE BEST VISION INDUSTRY HAS EVER SEEN.**

**See Us At NEPCON SE / Orlando, Booth 326, April 23-25**
**See Us At QUALITY EXPO / Chicago, Booth 2207, April 16-18**

**Circle 63 on Reader Inquiry Card**

once in the standard format, but ASCII translation at each end of a link slows the process considerably. The very 8-bit format of ASCII is cumbersome compared to a machine's native binary file formats. That is currently the trade-off between intercommunication and performance.

## Vanilla Formats

At the heart of shared databases is a data and file format usable by the entire design team from their equipment. This task has been taken on by only a few relatively large software tool companies. An aid to lower-level uniform formats would be a common operating system. The popularity of UNIX for engineering and development work suggests this route may be available for mixed-equipment networks.

Berkeley version 4.2 addresses networking with several new features. Virtual memory support uses a global page-replacement algorithm to manage large programs' storage space. File access speed, notoriously poor with earlier UNIX systems, has improved with data blocks that are larger and located more closely to each other on the disk. A network protocol subsystem built on external low-level networking protocols provides the base for interprocess communication via either one-way datagram service or reliable stream bidirectional virtual circuit connections.

From Cadnetix (Boulder, CO) to Apollo to DEC, proprietary operating systems are being supplemented with UNIX. Some modifications to the AEGIS OS are moving it closer to UNIX, according to Apollo. Digital has recently announced the VAX Shell for interface into UNIX environments. The differences between versions of UNIX, popular "UNIX-based" OSs and even implementations of one versions can be large. But assuming close adherence to specs, the BSD 4.2 enhancements to allow distributed applications on a network diminish the advantages of proprietary systems over UNIX.

In addition to UNIX software compatibility and individual companies that support various hardware types, there is some movement to standardize design data formats across the industry. In the future, users may prevail on vendors to create design files in a format common to many companies' tools.

A formal standard from the National Bureau of Standards is IGES (Initial Graphics Exchange Specification). As a graphics standard, IGES had to be expanded to cover electronic CAD. It is now the only standard for specifying printed circuit boards, schematics, cabling and ICs, but does not include an exchange language nor a hardware definition language.

EDIF (Engineering Data Interchange Format), developed by Tektronix, Daisy, Mentor Graphics (Beaverton, OR), Texas Instruments (Austin, TX), National Semiconductor (Santa Clara, CA) and Motorola (Phoenix, AZ), is more complete and designed to expand. Design data in EDIF are presented in a common symbolic format, regardless of the system on which the data were generated (*Digital Design*, August 1984).

Some aspects of TI's TIDAL hardware description language, Daisy's GAIL for gate array layout specification, Motorola and Mentor's TDF and UC Berkeley's CDIF interchange formats are included in the current version of EDIF. It is not a programming language or a database system, but a format for engineering data transfer. The syntax is similar to the Lisp programming language and designed to be expandable, like Lisp, to accommodate technology, methodology and parts changes.

Unlike many existing format and interchange systems, EDIF is not limited to a particular type of information. Netlists, logic models, layout abstractions, schematic symbols and documentation would all use EDIF for interchange. Technology data from an IC vendor could also be expressed under EDIF. This system of a common vanilla format would greatly facilitate meaningful communication among various types of hardware.

Though EDIF is not coming from a standards group, the base of industry support is growing. Firms offering software for only part of the design cycle or for limited performance machines, like Futurenet with design software for PCs, find standard formats worth supporting. The EDIF steering committee approved Version 1 in January. Copies of the document are available at $10.15 each for postage and handling from: ProPrint Services, 568 Widdell Dr., Suite #3, Sunnyvale, CA 94089.

A published document does not mean the work is finished. Version 1 focuses mainly on static descriptive formats, and procedural information (like a test method) is important to the design cycle. EDIF subcommittees are now working on devising procedural language and on issues of modeling and simulation, test, technology for design and electrical rules and adding terminology and features for printed circuit board design.

Though the most complete solution available, EDIF is based on proprietary schemes of the companies promoting it. Those with greatly different systems may be slow to join the movement. As is evident in many aspects of design systems, a majority of vendors are not yet convinced that open intervendor communication of engineering data is desirable.

## Filling The Gaps

Automating the electronics design cycle is still relatively novel; integrating the various stages is both important and difficult. Networking promises sharing of information and expensive resources like computing power, laser printers and high-capacity disk drives. Workstation networks may operate with shared files and databases, but they generally limit the user's network access to their own systems. Open network standards are emerging, and in the technical environment, Ethernet and IP/TCP are popular but provide only connection. The highest software layers, now proprietary to each vendor, are still needed for useful communication.

Since a design goes through many phases and iterations, it is crucial that the output of one stage can be used as input in the next. Though this function is available between certain equipment and applications on a point-to-point basis, it is far from standard. Companies using a common database have the right idea, but still manage to lock users into their system and about three types of hardware.

Format, interchange and network standards could release designers from single-company dependence. Those will undoubtedly be several years in coming. In the interim, new designs must be created as efficiently as possible. The range of applications and computers already (and in the plans to be) part of each firm's design environment must be the basis of CAD/CAE choices. If you require workstations to communicate freely with several other types of computer, plan on spending some time and effort at interconnecting them. DD

# Are you getting the color quality you expect?


# We can tell you in seconds

High technology instrumentation for spectroradiometry, photometry and colorimetry:
Pritchard® spectral and spatial scanning SpectraRadiometer™ systems.
SpectraScan™ fast spectral scanning SpectraRadiometer systems.

## PHOTO RESEARCH

The Light Measurement People
Division of Kollmorgen Corporation
3000 No. Hollywood Way, Burbank, CA 91505 Telephone (818) 843-6100 - Telex 69-1427

**AUSTRALIA** ETP PTY LTD., Ph: 858-5122, 858-5200 • **CANADA** OPTIKON CORPORATION, Ph: 519-885-2551 • **FRANCE** MICRO GISCO, Ph: 670-1158 • **WEST GERMANY** ROHDE & SCHWARZ, Ph: 02203-491 • **JAPAN** KYOKKO TRADING COMPANY, Ph: 03-586-5251 • **U.K.** MILLECRON INSTRUMENTS LTD., Ph: 207-4844 • **INDIA** PHOTONICS INTERNATIONAL, Ph: 366665 • **ISRAEL** DELTA FILM LTD., Ph: 052-557222 • **SWEDEN** SAVEN AB, Ph: 315-80 • **EUROPEAN HEADQUARTERS** LUZERN, SWITZERLAND, PHOTO RESEARCH, Ph: 041-3690-89

**Circle 59 on Reader Inquiry Card**

# PRODUCT INDEX

To help you find the products that you need, we've compiled a subject index of the ads and new products that appear in this issue. Organized by general product area, the listings include the name of the manufacturer, the page on which the product appears and a circle number for additional information on that product. Bold type indicates advertised products.

# *Shape The Future*
# *Share The Pride*

Pioneering has been our business since 1891. Today, we're in the midst of a technological revolution...still leading the way toward shaping the future of modern telecommunications. Digitalized switching and transmission systems, advanced integrated circuits utilizing state-of-the-art Bipolar and CMOS technologies, new dimensions in fiber optics, innovative products and processes...all assimilated to shape the direction of tomorrow by the professionals at GTE.

If you have a background and experience in Electrical Engineering, Computer Science, Computer Engineering, Physics or Chemical Engineering, we invite you to share the pride with GTE by becoming part of tomorrow's telecommunication task force today! Please send your resume or letter of qualifications. An Equal Opportunity Employer. m/f/h/v.

**GTE COMMUNICATION SYSTEMS**
**Human Resources Dept. 5885**
**2500 W. Utopia Road**
**Phoenix, AZ 85027**

GTE **Communication Systems**

Working Together To Be The Best

# Gate Equivalency For Programmable Logic Devices

by Joseph Vithayathil, Strategic Marketing Manager, Bipolar/LSI, National Semiconductor, Santa Clara, CA

Programmable logic devices constitute one of the fastest growing areas in semiconductor technology, with more designers becoming aware of the benefits they offer. The basic programmable logic structure is an AND-OR array that can be implemented in a Sum-Of-Products (SOP) form. The compact SOP logic structure is implemented through fuse-linked arrays. An issue frequently raised by system designers is the definition of gate densities or gate equivalency of programmable logic devices (PLDs).

This question is important because the density of some other semicustom alternatives, particularly gate arrays, is measured in terms of equivalent basic gates. The basic gate can vary from one gate array to another, but the 2-input NAND gate is most common. Estimating gate density of a gate array is relatively easy because the silicon consists of actual gates that can be interconnected to implement logic in an arbitrary fashion. In contrast, the fuse-linked array silicon of PLDs does not contain a collection of basic gates, making measurement of gate density difficult.

Furthermore, PLDs appear to be used less efficiently than gate arrays. The term efficiency, however, must be applied in the context of the particular application-specific IC technology. The 2-input equivalent gate count used in gate arrays and standard cells can be applied to PLDs, but certain other factors must be included in the gate equivalency analysis to put the PLD in perspective. Because a PLD by nature has very wide programmable gates, it does not immediately lend itself to a 2-input gate equivalent analysis. For many reasons, the efficiency with which PLDs are used varies considerably.

A major source of variability is the complete array connectivity of these devices, the feature that makes them so flexible. Designers have the option of connecting every input of a programmable array to every output gate of the array. Most devices have TRUE/COMPLEMENT input signal lines in the AND array, and therefore half of the array inputs will never be used. The resulting wide gates are needed for flexibility since the manufacturer does not know which input variables or complements will be necessary for a particular application.

Since most designs do not use a major portion of the logically valid connections, it appears the wide gates are used inefficiently. Any attempt to increase the efficiency of usage would entail a decrease in the overall connectivity options of the array (i.e., remove all complement lines, reduce the number of fuse links). This, in turn, would decrease the structure's flexibility.

In many cases PLDs are used to reduce chip count, system size and cost of an existing product. Because of the nature of some existing designs, it may not be possible to use the programmable logic device efficiently. In I/O intensive applications, the wide gates of these devices tend to be underutilized.

Further disparity in usage efficiency is due to users' lack of experience with this approach to logic design. Most designers choose standard SSI/MSI devices from the TTL Data Book for needed functions.

| GATE BEING REPLACED | REQUIRED NUMBER OF BASIC GATES |
|---|---|
| 16-INPUT NAND | 15 2-INPUT NAND GATES |
| 16-INPUT NAND | 5 4-INPUT NAND GATES |
| 12-INPUT NAND | 11 2-INPUT NAND GATES |
| 12-INPUT NAND | 3¾* 4-INPUT NAND GATES |
| 8-INPUT OR | 7 2-INPUT OR GATES |
| 8-INPUT OR | 2½ 4-INPUT OR GATES |

*A fraction of the basic gate results when available inputs are not used; ¾ indicates that one input in a 4-input gate is not being used.

Table 1: Number of basic gates required to replace NAND and OR gates of different widths.

| PAL DEVICE | 2-INPUT TMFE | GATE EQUIVALENCY RANGE | |
|---|---|---|---|
| | | 5% TMFE | ≈25% TMFE |
| 16L8 | 1020 | 50 | 250 |
| 16R8 | 1077 | 50 | 270 |
| 16R6 | 1063 | 50 | 260 |
| 16R4 | 1025 | 50 | 260 |
| 20L8 | 1430 | 70 | 360 |
| 20R8 | 1487 | 70 | 370 |
| 20R6 | 1473 | 70 | 370 |
| 20R4 | 1459 | 70 | 360 |

Table 2: Two-input basic gate Theoretical Maximum Functional Equivalency and usable gate equivalency range for popular PAL devices at 5% and 25% of the TMFE.

# THE ELECTRONIC IMAGING WORLD IS GOING DRY

## With 3M's improved Dry Silver Papers and Films

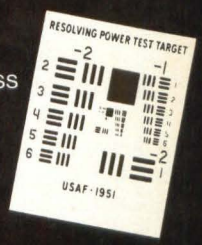
In the past 20 years, we've helped a lot of people — from all areas of electro-optical imaging — go dry. We've simply convinced them, with 3M Dry Silver Papers and Films, that dry is definitely better. That it's faster, cleaner and more economical than conventional wet-processed materials.

Working with OEM's, our product improvements have helped the imaging industry make giant strides in hardcopy system design, with fresh ideas and new solutions to problems. For a wide range of imaging applications requiring photographic quality with dry instant processing, 3M Dry Silver continues to be the answer.

So it's no wonder the electronic imaging world is going dry. And now there are more reasons why you should, too: 3M's new generation of high performance Dry Silver Papers and Films. You'll get fast, permanent hardcopies of your data that are sharper, cleaner and easier to process than before. Here's why:

**Spectral sensitivity from UV to IR**
The 3M Dry Silver process uses photo-sensitive compounds which can now be tailored to obtain desired spectral sensitivity, from roomlight handling ultraviolet sensitive materials to infrared sensitive materials suitable for use with IR semiconductor lasers.

**Photographic resolution and quality**
3M Dry Silver Papers and Films offer photographic quality similar to wet-process materials. Plus they're faster and more economical. Resolution in excess of 150 line pairs/mm is possible with our papers and 300 line pairs/mm for films.




**Increased sensitivity**
Significant increases in sensitivity over our previous materials are now a reality. If faster writing rates or low energy light sources are problems, this improvement may be your answer.


**Faster, totally dry processing**
New processing techniques and systems have increased the quality and access time associated with dry processing. We now offer our processing know-how, OEM sub-assemblies and finished units to OEM's and end-users interested in going dry.

Don't be content to watch your world go dry around you. Find out how you can too. Contact us today!

**Imaging Products**
**Imaging Systems Division/3M**
223-2SW, 3M Center
St. Paul, MN 55144

**3M hears you...**

3M

Circle 65 on Reader Inquiry Card

Becoming reasonably proficient with SOP and Boolean calculations to get complex functions in a PLD may take a substantial amount of time. The advent of software design aids like minimization, logic partitioning and state machine synthesis will help the user apply PLDs more effectively and efficiently than in the past.

With the current wide variability in the efficiency with which these devices are used, it may not be meaningful to derive a fixed gate-density number for PLDs. However, a means of establishing a usable gate density range is important. Before outlining the algorithm for determining this range, two definitions are in order.

First, the Theoretical Maximum Functional Equivalency (TMFE) is defined as the maximum number of basic gates needed to functionally replicate the virgin programmable logic device. Second, the efficiency at which a PLD is used is defined as the ratio of the number of basic gates it would take to perform the desired logic function to the TMFE.

The approach taken here for estimating gate density consists of three steps. First, establish a TMFE number for each PLD. Then, examine the possible applications to determine a range within which the number of basic gates needed to implement them falls. At that point, a usable range of efficiency or gate equivalency, within which programmable logic device applications fall, can be established.

Calculating the TMFE involves several steps. To begin, the basic gate must be chosen. The most common basic gate is the 2-input NAND gate; other possibilities are 2-input OR, 2-input NOR, 2-input AND, 3-input NAND and 4-input NAND. Next, establish conversion factors to describe digital logic elements in terms of basic gates. Two-input gate equivalencies for common digital elements found in popular PAL devices include one-half gate equivalency for both inverting buffers and tri-state buffers and six gate equivalency for a D flip-flop.

The final step in establishing TMFE is to examine the AND-OR array and calculate the minimum number of basic gates that would be required to implement the same logic function. **Figure 2** shows that the AND-OR structure can be logically represented as a NAND-NAND array. With this in mind, AND gates and OR gates can be individually replaced by the number of basic gates required to achieve functional equivalence. For example, using a 2-input OR basic gate, an 8-input OR requires seven 2-input OR gates. **Table 1** shows the number of basic gates required to replace AND and OR gates of different widths. (See "Example of TMFE Calculation" for a step-by-step example.)

One question that could be raised at this point, is what is the use of a lengthy and precise computation of a theoretical gate count when only a portion of the gates counted will ever be utilized? The reason for this approach is to establish the baseline from which to derive a usable range. The alternative to proceeding in this objective manner is to use totally subjective conversions.

Now that a method of calculating the TMFE for PLDs is in place, a usable range must be established that will cover most applications. This is a range of ratios of basic gates needed for an application to the device's TMFE. From an empirical examination of various applications, National Semiconductor determined that a usable range for PLDs such as PALs is from 25% to 5% of TMFE.

The value of providing such a range based on an objective TMFE computation is that the user can, based on the application and Boolean equations, determine exactly where a design falls within the usable range. This provides an accurate

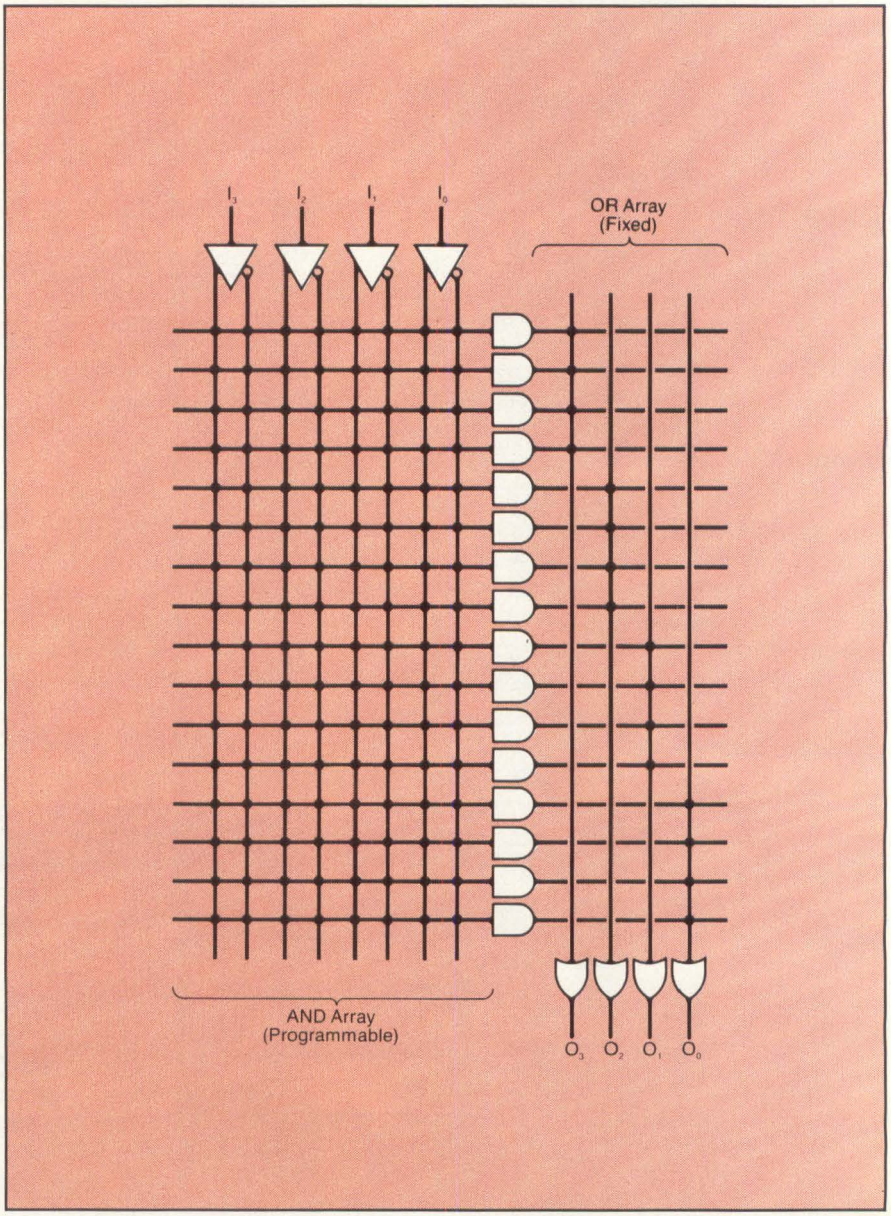
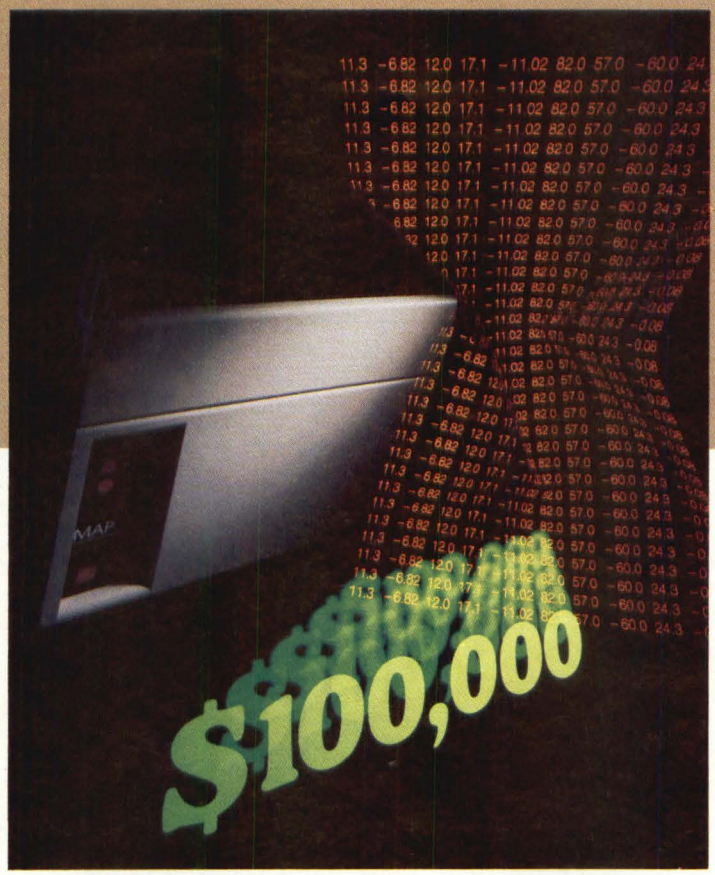



Figure 1: Set up of a PAL having four inputs, four outputs and 16 products.

# A Supercomputer you can REALLY Afford.




## At $100,000,* 64-bit Scientific Number Crunching is NOW Accessible.

Supercomputer number crunching power in a compact package—that's the new MAP-6420. First CSPI set the goal of making 64-bit double-precision computation truly accessible to scientific and engineering users in laboratory environments. Then we enhanced computation and condensed array processor size and cost to produce the MAP-6420. Small in size—up to 16 megabytes of memory will fit in a 21-inch rack-mountable chassis. Small in price—our 4 megabyte unit starts at a low $100,000. And packed with computational muscle—MAP-6420 speeds up your VAX by a factor of 5 to 15, and at the same time, frees it for other tasks, so the overall response time for every VAX user is improved.

The MAP-6420 has the configurational range to handle your large scale applications. Its low component count yields high reliability and offers the benefits of low power, low cooling, and minimal space requirements.

For users who can program in FORTRAN, high performance is virtually assured. We planned MAP's hardware around its FORTRAN compiler so the programs the user writes will deliver the performance paid for. Parallel units process algorithms efficiently, even if they're not vector-oriented. In addition, we offer a Scientific Subroutine Library of 120 optimized math functions. Uniform, versatile performance delivered from FORTRAN—that's MAP-6420!

Discover how you can benefit from MAP-6420 number crunching. **Call toll free 1 800 325-3110.**

*USA price

VAX is a U.S. trademark of Digital Equipment Corporation

MAP-6420 is a U.S. trademark of CSPI

CSPI
THE ARRAY PROCESSORS

40 Linnell Circle, Billerica, Massachusetts 01821 • 617/272-6020 • TWX: 710-347-0176

**Circle 70 on Reader Inquiry Card**

## Example Of TMFE Calculation

The 16R8 is a 16-input, 8-output AND-OR registered array in a 20-pin package. In terms of traditional logic, its schematic consists of the following functional logic elements:

– 64 AND gates with 16 inputs each. (Note that even though the schematic would show the AND gates with 32 inputs each, from a functional viewpoint, it has only 16 inputs because the TRUE and COMPLEMENT of a variable will always hold the output low. Assuming more than 16 inputs implies such a condition.);

– 8 OR gates with 8 inputs each;

– 8 D flip-flops;

– 25 inverting buffers.

To obtain the array's 2-input TMFE, these elements must be converted with the following procedure.

For the 16-input AND gates, functional duplication of each gate with 2-input basic gates requires 15 gates. Therefore, the TMFE for this element would be 64 × 15 = 960 gates. Similarly, for the 8-input OR gates, it would take seven 2-input OR gates to functionally duplicate each element. The TMFE is 8 × 7 = 56 gates. The gate equivalency for each of the 8 D flip-flops is 6, so the TMFE is 8 × 6 = 48 gates. Each inverting buffer is one-half gate equivalent, for a TMFE of 25 × ½ = 12.5 gates. The result of this is a 2-input TMFE for the PAL16R8 of 960 + 56 + 48 + 12.5 = 1076.5 gates.

The 2-input TMFE for other popular PAL devices can be calculated in the same fashion. This objective functional equivalency, established in terms of a basic 2-input gate, is the first step in establishing a usable gate count range.

measure of how efficiently the designer has used the PLD. **Table 2** shows the TMFE and usable range for popular PALs, in terms of 2-input gate density. The relatively wide range is indicative of the variability in the way these devices are used.

An example of a PAL device application is the DP84412 Dynamic RAM Controller Interface Circuit for the Series 32000 CPU. This design uses the PAL 16R6. Calculating on the basis of **Table 1**, this application requires 165 2-input gates. According to **Table 2**, the 16R6 2-input TMFE is 1063; the 165 gate equivalency of this application works out to an efficiency of 15%. Within the usable range established earlier (5% to 25%), this device has been used at an efficiency of 60%. **Figure 3** shows the Boolean equations and number of equivalent 2-input gates for the circuit.

The PAL user can reference **Table 1** to estimate a device's 2-input gate density; from this estimate, the designer can compare an application for overall efficiency in PALs with other semicustom technologies. Gate density is not the only consideration in choosing technology. Cost, flexibility for making changes and expediency in prototyping are also important. In addition, there is no rule that a 2-input gate is the only basic gate to be used. A similar analysis can be carried out using a 3-input or a 4-input basic gate.

A direct one-to-one correlation cannot be drawn between basic gate equivalency analysis and silicon area. To relate this to

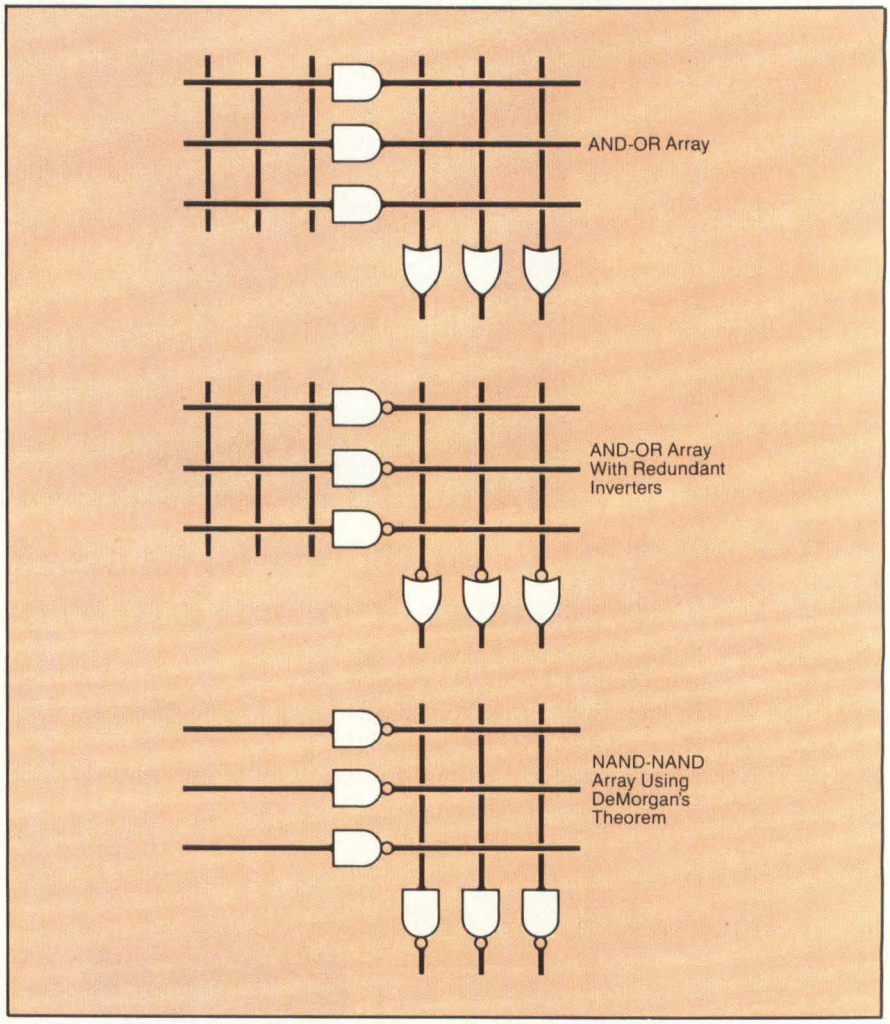


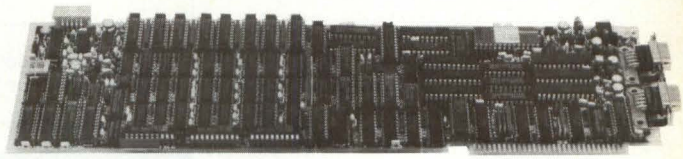

Figure 2: The AND-OR array at top can be represented with redundant inverters (center) and, using De Morgan's theorem, as a NAND-NAND array.

# Now your IBM PC can see like a hawk!

## Datacube's real-time frame grabber matched for CCD cameras.

Datacube's new IVG-128 is the perfect match for QC inspection and medical imaging applications on the IBM PC.

- Real-time video acquisition with 384H × 512V resolution and 256 grey levels or pseudo-color output (256 colors out of 16 million configurable palette).
- CCD & CID cameras map directly and efficiently in the memory space. These cameras include Sony, Fairchild, Panasonic, Hitachi, NEC and GE.
- Single, low-power board is cascadable for 24-bit true color processing.
- Dual phase-locked loop for excellent display stability and locking to external video tape input.
- Language-independent image processing and pattern recognition software routines.



See how easy it is to make your computer see like a hawk. Call or write Datacube Incorporated, 4 Dearborn Road, Peabody, MA 01960, Telephone: (617) 535-6644.

Datacube

Circle 66 on Reader Inquiry Card

```
PAL16R6A      ;FAST PAL
NEW PAL FOR THE NATIONAL SEMICONDUCTOR NS32016, 32008, 32032
NATIONAL SEMICONDUCTOR (WORKS UP 10 MHz)

FCLK TSO RFIO ADS DDIN WAITWR CTTL CS WAITRD GND
OE CWAIT 4DLY 3DLY 2DLY MODE RASIN CYCLED INCY VCC
```

**7χ**

```
RASIN := INCY*CYCLED*MODE*CTTL*DDIN+          ;Start RASIN fast during
                                              ; *READ* cycle
         INCY*MODE*2DLY
```

**27χ**

```
CYCLED := MODE*2DLY*WAITWR*DDIN*CTTL +        ;No WAITS inserted
          MODE*2DLY*WAITRD*DDIN*CTTL +        ;No WAITS inserted
          MODE*2DLY*4DLY*WAITRD*DDIN*CTTL*    ;WAIT in READ cycle
          MODE*2DLY*4DLY*WAITWR*DDIN*CTTL +   ;WAIT in WRITE cycle
          CYCLED*TSO*MODE +
          CYCLED*MODE*CTTL
```

**9χ**

```
MODE := RFIO*INCY*2DLY*CTTL +                 ;forced refresh during idle
                                              ;states, in long cycles,
        MODE*3DLY +                           ;or at the end of a cycle
        MODE*4DLY +
        MODE*CTTL
```

**26χ**

```
2DLY := MODE*4DLY*CTTL +
        2DLY*CTTL+
        INCY*CYCLED*MODE*3DLY*4DLY*CTTL +
        CS*DDIN*WAITRD*INCY*MODE*2DLY*3DLY*4DLY +   ;extend 2DLY if
        CS*DDIN*WAITWR*INCY*MODE*2DLY*3DLY*4DLY     ;WAIT states
                                                    ; are wanted
```

**4χ**

```
3DLY := 2DLY*4DLY*CTTL +
        3DLY*CTTL
```

**10χ**

```
4DLY := 3DLY*CTTL +
        4DLY*CTTL+
        INCY*MODE*CTTL +
        INCY*MODE*2DLY*CTTL
```

**11½χ**

```
IF (VCC) INCY = ADS*MODE +
          CS*TSO*CYCLED*MODE*2DLY*4DLY+     ;Start INCY for CS
          INCY*CYCLED +                     ;access after forced
          INCY*2DLY                         ;refresh
```

**26½χ**

```
IF (CS) CWAIT = CS*TSO*CYCLED*MODE*2DLY*4DLY+     ;for Access during
                                                  ;forced refresh
    CS*TSO*MODE+
    CS*INCY*CYCLED*DDIN*WAITRD*MODE*2DLY*3DLY*4DLY+
                                                  ; CS READ cycle with
                                                  ; WAIT states
CS*INCY*CYCLED*DDIN*WAITWR*MODE*2DLY*3DLY*4DLY
                                                  ; CS WRITE cycle with
                                                  ; WAIT states
```

Additional necessary logic: 6 registers = 36χ
16 inverters = 8χ

Total Gate Count = 165 2-input gates

*NOTE: χ = one 2-input gate*

Figure 3: These Boolean equations and number of 2-input equivalent gates for each section of the DP84412 demonstrate how the 165-gate figure is reached.

silicon would require an investigation of the amount of die area consumed by the AND and OR arrays as well as the registers and any other logic elements on the PLD. The silicon area used for a particular application would then be divided by the total area consumed by the entire AND-OR array.

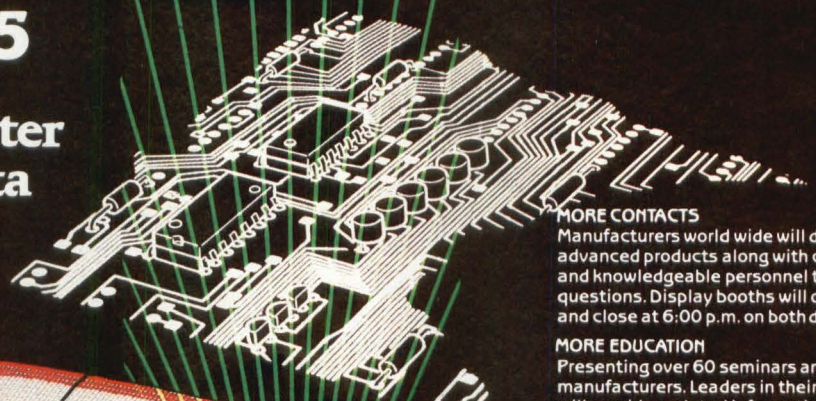
Programmable logic devices continue to gain popularity as a semicustom design option, but comparison of gate density with other technologies has been difficult. The intent of this proposal is not to suggest that every user and manufacturer tediously compute gate equivalency for every application, but more to provide an objective framework in which gate densities for such devices can be estimated.

# 2nd Annual
# Midwest Electronics Exposition

"It's all here–Components, Process and Production, Protective Packing, Purchasing and Management, Quality and Test."

## May 8, 9, 1985

## St. Paul Civic Center
## St. Paul Minnesota



**MORE CONTACTS**
Manufacturers world wide will display their most advanced products along with current information and knowledgeable personnel to answer your questions. Display booths will open at 10:00 a.m. and close at 6:00 p.m. on both days.

**MORE EDUCATION**
Presenting over 60 seminars and 1000 manufacturers. Leaders in their respective fields will provide updated information regarding the very latest technology in a series of ongoing seminars from 8:30 a.m. to 3:15 p.m. each day.

**NEW THIS YEAR**
Surface Mount Assembly Line.

ENDORSED BY: • ERA • IEEE • ISHM • Governors Office of Science & Technology • REPNA • Minnesota High Tech Council • Women in Electronics

Sponsored by Circuits Manufacturing & Digital Design

**ADVANCE REGISTRATION FORM**
**MIDWEST ELECTRONICS EXPO – MAY 8, 9, 1985**

PLEASE PRINT

NAME

COMPANY

ADDRESS

CITY _____ STATE ZIP

PHONE ( ) - MAIL STATION

Check Principle Job Function

- ☐ Electrical/Electronic Engineering
- ☐ Mechanical Product Engineering
- ☐ Test Engineering
- ☐ Production/Manufacturing Engineering
- ☐ Engineering Services
- ☐ Purchasing
- ☐ Sales/Marketing
- ☐ Manufacturer's Representative
- ☐ Management
- ☐ Student/Educator
- ☐ Other

Please send me _____ additional registration forms for my co-workers.

**Return form to: LST OF MINNEAPOLIS, INC. 7900 W. 78th Street Suite # 105 Edina, MN 55435 Tel (612) 944 3639**

DD485

**PLEASE REGISTER ME FOR:**

registrations received by

**Plan A** – Exhibits only _____ April 26, 1985 – no charge

**Plan B** – One day technical sessions _____ $10.00 at the door

_____ $20.00

**Plan C** – Two day technical sessions _____ $35.00 at the door

_____ $30.00

$50.00 at the door

**Seminar Tracks** – Please check track of interest*

- ☐ Process and Production (Automation, PCB Assembly, Soldering, Cleaning, Surface Mounted Devices, Electro Static Devices)
- ☐ Purchasing and Management
- ☐ Semiconductor, Hybrid and Vacuum
- ☐ Basic Electronics
- ☐ Design and Components
- ☐ Protective Packaging
- ☐ Quality, Test and Environmental

* Note: This is not a commitment to this track, but will help us in providing appropriate room space.

Enclosed is a check or money order # _____

Bill me: P.O. # _____ (payable next 30 days)

Visa or Master Card #

Expiration Date _____ Signature _____

# Autoranging Analog-To-Digital Converter Simplifies Multimeter Design

by Wes Freeman, Teledyne Semiconductor, Mountain View, CA

Single-chip analog-to-digital (A/D) converters with on-board drivers for an LCD display have simplified the design of hand-held digital multimeters (DMMs). Such DMMs typically measure voltage, resistance and current over several ranges and require only a 9V battery for operation. Since the A/D converter is a single CMOS chip, low instrument cost and long battery life are easy to attain.

The DMM still requires an extensive network of mechanical switches, however, to select range and function. This switch matrix accounts for a significant portion of the cost of a DMM.

A new IC from Teledyne Semiconductor, the TSC805, replaces the DMM's mechanical switches with internal CMOS switches. In addition, logic on the chip automatically selects the proper voltage or resistance range to ensure maximum resolution without operator intervention. Logic inputs are also available to place the TSC805 in its manual-range mode with push-button range stepping.

Bringing the range switches on chip and adding autoranging logic significantly reduces the cost and size of a DMM. To further reduce system cost, added features of the TSC805 permit continuity measurements with high-current drive for a piezoelectric transducer, operation in memory mode, AC-to-DC conversion, low-power resistance measurements and low battery-voltage detection. Physical size can be reduced because the entire A/D converter is contained in a 60-pin surface mount package. This 0.5″ square quad-leaded package is much smaller than the 40-pin DIP of previous A/D converters.

Functionally, the TSC805 (**Figure 1**) can be divided into three sections: (1) input conditioning circuits and autoranging switches, (2) a 3½ digit A/D converter with on-chip voltage reference and drivers for a liquid crystal display and (3) logic circuits which set the function and range and drive the annunciators and the buzzer.

The input conditioning circuits include

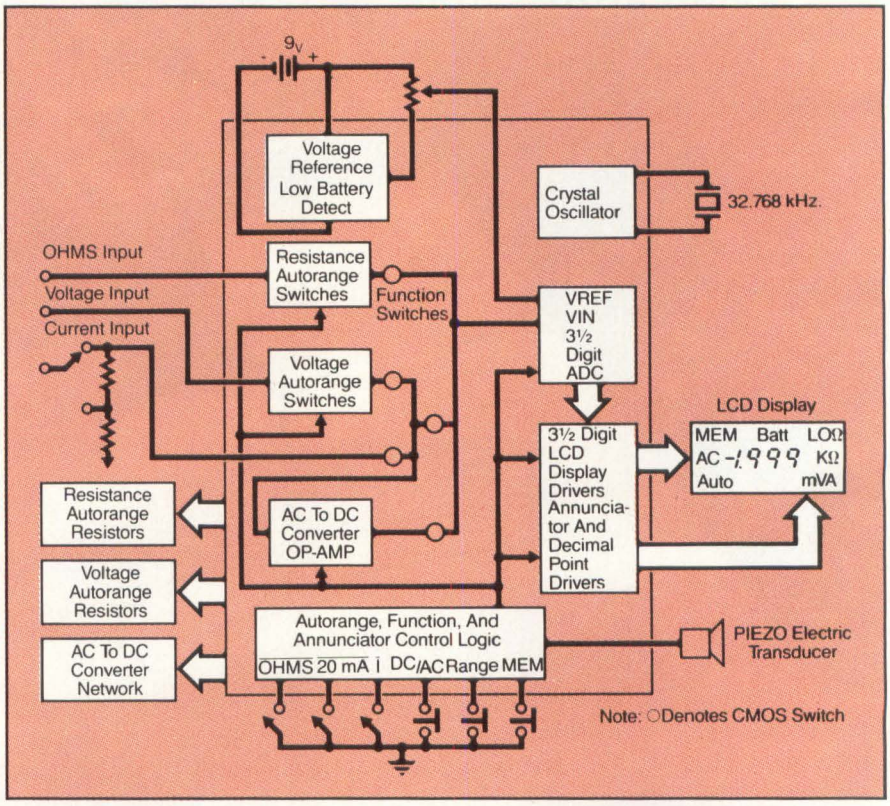



Figure 1: A simplified block diagram of the TSC805 identifies the main components of the input conditioning, 3½ digit A/D converter and control logic subsystems.

two banks of CMOS switches that provide voltage and resistance range switching. An op-amp that can be configured as an AC-to-DC converter is also provided, permitting AC voltage and current measurements. Finally, CMOS switches connect the resistance, current and voltage inputs to the A/D converter.

The TSC805's A/D converter is a dual-slope, autozeroed, integrating type which combines good resolution with low power operation. Since the A/D converter integrates noise over time, accurate measurements can still be made in the presence of, for example, 60 Hz line interference. The A/D converter has a resolution of 2000 counts (3½ digits) in the autoranging mode. In the manual-range mode, however, resolution is extended to 3000 counts. Extended-range operation also occurs automatically in the highest voltage and resistance ranges, permitting measurements up to 2999 KΩ and 2999V.

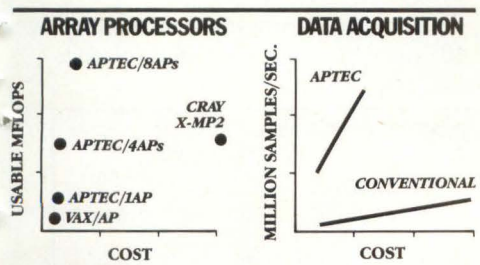
Logic circuits control the measurement modes, autoranging and options. Three logic inputs to the TSC805 select the desired measurement mode. Three other inputs select manual-range operation and step from one range to the next, select between AC and DC or high and low power ohms, and enable or disable the memory option.

A typical application for the TSC805 is a 3½ digit DMM. The schematic for such a meter, shown in **Figure 2**, reveals that only one simple multipole switch and five SPST switches are required to provide five DMM functions with 18 operating ranges. A low-power ohms mode, which reduces probe voltage to permit measure-

# THE MOST SIGNIFICANT BREAKTHROUGH IN VAX SYSTEM PERFORMANCE SINCE THE ARRAY PROCESSOR.


Introducing the Aptec 2400 I/O Computer – a new *class* of computer that can increase the throughput of VAX-based systems as much as 40X. Simply. And economically.

By eliminating the I/O bottlenecks that limit performance, the Aptec I/O Computer makes your peripherals work faster and more efficiently. Including disks and tapes, APs, graphics/image processors, and special purpose devices.




*The Aptec I/O Computer will unleash the performance potential of your VAX.*

It lets you achieve true supercomputer performance with any VAX by allowing efficient integration of multiple array processors.

And, the Aptec I/O Computer permits dramatic new levels of performance in real-time data acquisition and analysis.

Not since the array processor has any development done so much to boost the performance of minicomputer systems.

Here's how it works: The Aptec I/O Computer creates an independent, 24 MB/sec, FILES-11 I/O environment that allows VAX-shared peripherals to transfer data at full speed, free from VAX bandwidth limitations.

From 1 to 200 MB of high speed memory is directly accessible by your attached peripherals and VAX.

And, the Aptec I/O Computer provides the intelligence to control peripherals, data transfers and peripheral computations – with minimal involvement of the VAX CPU, the VMS operating system or the Unibus.

Peripheral operations become more efficient. Attached processors work at peak efficiency. And your VAX is free to provide better service to your on-line users.

Learn how the Aptec 2400 I/O Computer can unleash the performance potential of your VAX system. For the complete story on this exciting new class of computer, write or call Aptec today.

APTEC SYSTEMS®

Aptec Computer Systems, Inc.
10180 S.W. Nimbus Ave.
Portland, OR 97223
(503) 620-9840
Telex 467167



Circle 69 on Reader Inquiry Card

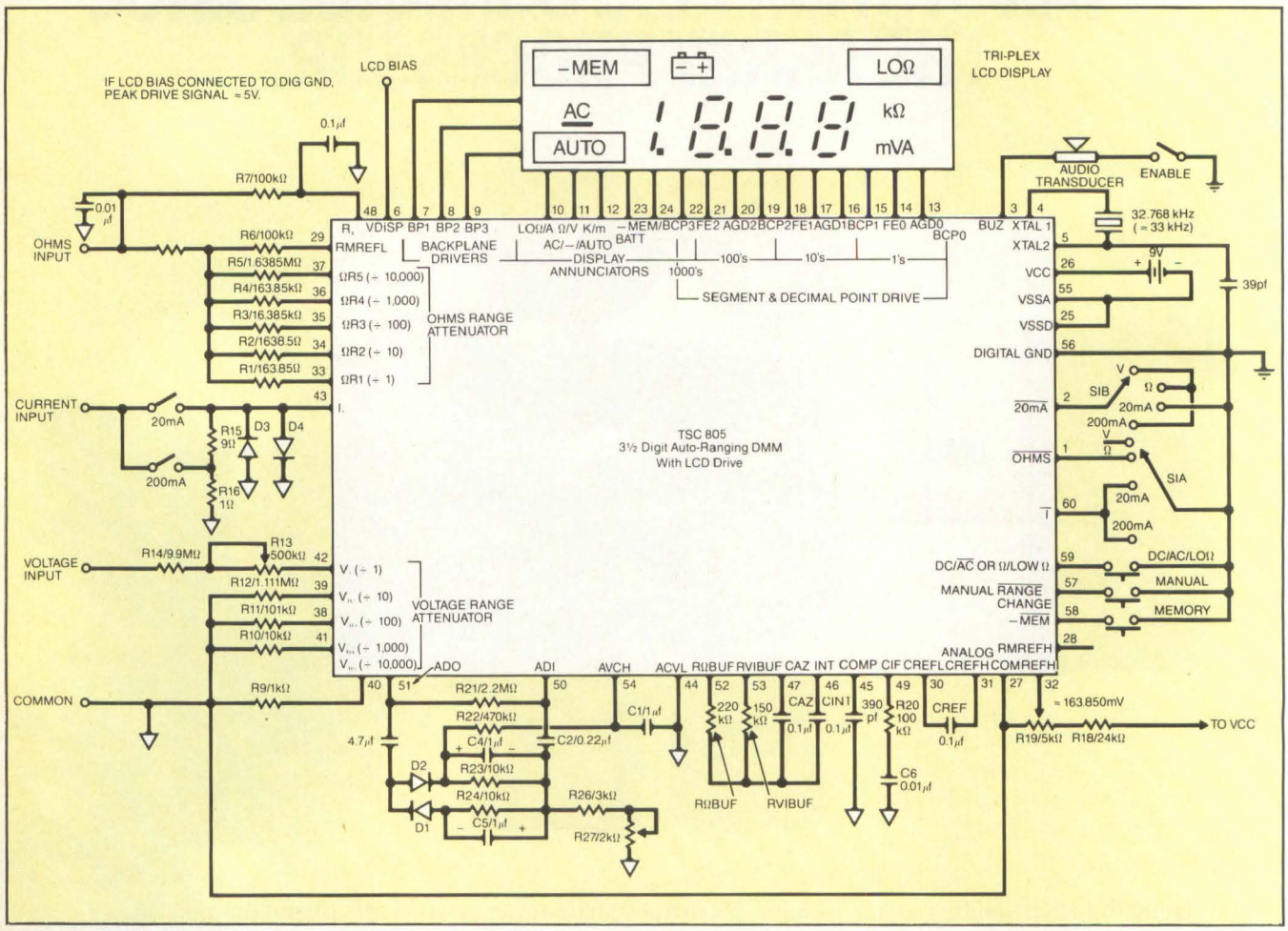



Figure 2: The TSC805 is the only active component in this five function, 22 measurement-range digital multimeter.

ments without turning on semiconductor junctions, can also be selected (**Table 1**).

Autoranging operation is provided for resistance and voltage measurements. External resistors combine with internal CMOS switches to form a programmable attenuator, controlled by autoranging logic. The logic adjusts the attenuator ratio to constantly maintain a 200 mV full scale input to the A/D converter. If the converter is overranged, the switches are changed to select the next higher range. If the conversion result is less than 9% of full scale, the next lower range is selected.

Range changes are signaled to the operator by a short beep on the buzzer. A continuity indication is also provided, by turning on the buzzer when a resistance reading is less than 1% of full scale.

Measurements of current are not autoranged. The unknown current is simply passed through a 1.0Ω or 10Ω resistance, to produce 100 mA and 20 mA ranges, respectively.

For AC measurements, two diodes and a resistor-capacitor (RC) network are attached to the ADO and ADI pins. This network combines with the internal op-amp to form a full wave rectifier. The rectified output is then returned to the A/D converter via the ACVH and ACVL inputs. If more accurate AC results are required, the diode-RC network can be replaced with a true-RMS converter.

For a voltage reference, the circuit utilizes the TSC805's Analog Common output. This pin is a current sink input whose voltage is maintained at about 2.6V below Vcc, with a temperature coefficient of 50 ppm/°C. Analog Common also serves as a common mode bias point for the A/D converter, permitting bipolar measurements when powered from one 9V battery.

The circuit also makes use of the TSC-805's multiplexed LCD drivers to produce

| FUNCTION | RANGES AVAILABLE | | | | |
|---|---|---|---|---|---|
| DC Voltage | 200mV | 2V | 20V | 200V | 2000V |
| AC Voltage | | 2V | 20V | 200V | 2000V |
| High Power Ohms | 200Ω | 2KΩ | 20KΩ | 200KΩ | 2MΩ |
| Low Power Ohms | | 2KΩ | 20KΩ | 200KΩ | 2MΩ |
| DC Current | | | 20mA | 200mA | |
| AC Current | | | 20mA | 200mA | |

Table 1: Without complex switches, the TSC805-based DMM provides 22 measurement ranges.

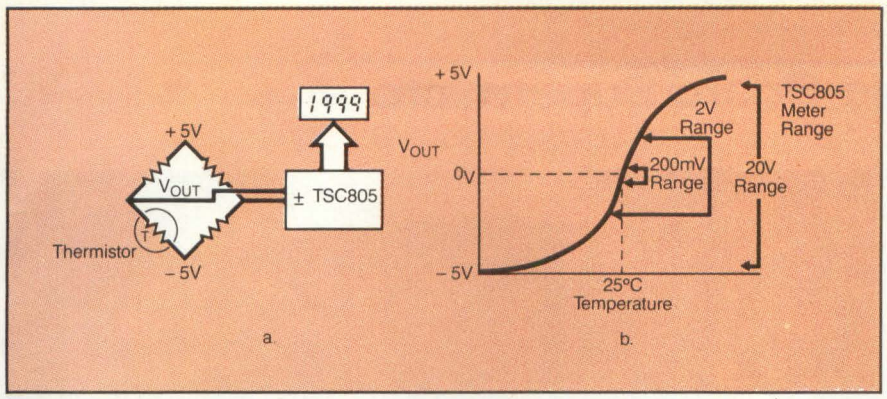



Figure 3: The autoranging meter combines high resolution for the narrow linear portion of this thermistor's output with wide range for determining magnitude and trend during overrange.

a variety of annunciators on the display. Annunciators for displaying function, decimal point and detection of low battery complement the information content of the normal 3½ digit numerical display.

Depressing the circuit's MEMORY pushbutton switch activates the TSC805 memory mode. This mode stores a constant, up to 99 counts, in internal memory. The constant is then subtracted from succeeding readings, easing such tasks as relative voltage measurements and resistor matching.

Duplicating these DMM features with a nonautoranging A/D converter is difficult. Manual range selection adds about 20 mechanical switch sections, while autoranging requires several ICs. An AC-to-DC converter, continuity buzzer and display annunciators require an op-amp, discrete transistors and one or more ICs, respectively. Some functions, such as extended range and memory option, are difficult to add at all.

Another application for which the TSC805 is well suited is in instrumentation for monitoring inputs that have a large dynamic range. For example, a 3½ digit meter for a 0-40V laboratory power supply can only provide 10 mV resolution without a cumbersome and expensive range switch. The autoranging meter, on the other hand, can provide resolution down to 100 $\mu$V for low output voltages while maintaining the ability to measure higher voltage levels. In fact, the simplicity of the TSC805 circuit could permit upgrading the power supply's meter to a full-function DMM by adding an ohms-range attenuator resistor divider.

Some process control circuits, such as thermistor bridges, can also benefit from an autoranging meter. The thermistor bridge of **Figure 3**, for example, provides an output of about 100 mV/°C at 25°C. The TSC805 can provide the resolution for a thermistor's ±2°C scale, thus yielding an extremely sensitive thermometer. However, a meter with 200 mV full scale could only measure ±2°C before overrange occurred. The bridge output is actually about ±4.95V, from -55°C to +125°C. By autoranging when the bridge output exceeds ±200 mV, the meter will continue to monitor temperature, at reduced resolution and accuracy, over a wide temperature range.

Although the full range output is nonlinear, the magnitude, polarity and trend information could still be useful to an operator. In addition, the buzzer output that occurs at each automatic range change could be used to inform the operator of an overrange condition.

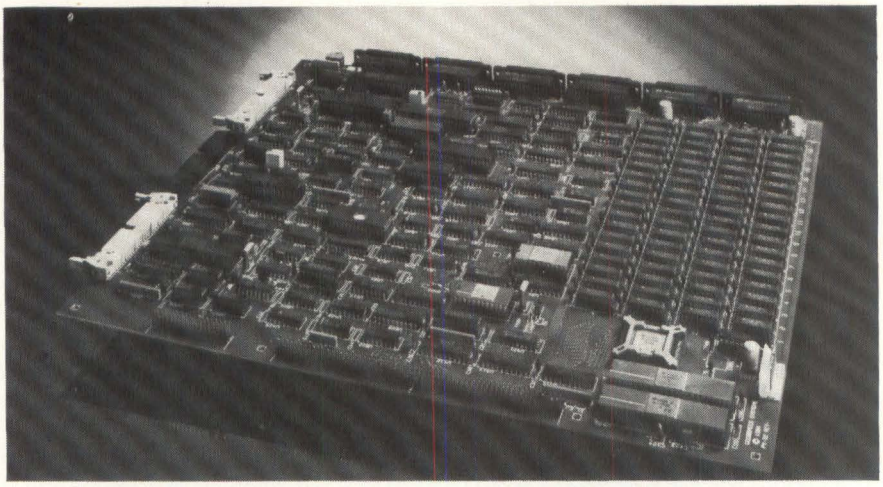
The autoranging feature of the TSC805 provides application flexibility while reducing system costs. The metal-gate CMOS process produces both low-noise analog components and complex digital functions. Simple 9V battery operation is maintained, and power consumption is actually reduced from the previous generation of display A/D converters.

**Circle 235**

## BOARDS

# 32032-Based Single-Board Supermicro

A dual-processor, 32-bit single-board computer aimed at the industrial/scientific marketplace has been announced by Goodspeed Systems (East Haddam, CT). The GS-32 is based on National Semiconductor's 32000 series of processors and is configured to accept either the 32016 or the 32032. Included on the board is an NS32082 MMU, an NS32081 FPU and the NS32021 TCU. All I/O operations are handled by a separate Z80B processor that has 8 Kbytes of static RAM and 16K of nonvolatile control storage. The Z80B directly controls a DMA device for block transfers between I/O devices and the NS32032 main memory. All I/O devices are interrupt/vector driven with a flexible prioritization scheme. The GS-32 bus structure and form factor are proprietary, but Goodspeed is providing an optional plug-in module for an expansion connector



which would adapt the CPU core to the Multibus. There are 512 Kbytes of parity protected dynamic RAM on-board, expandable to 2 Mbytes. In addition to the GS-32 SBC, Goodspeed is manufacturing a development system aimed primarily at OEMs designing in the single-board computer.

*—Wilson*
**Circle 233**

## SYSTEMS

# DEC Workstation Supports CAE Software

Complementing its previously announced VAXstation 1 system, DEC's latest addition to its family of workstations, the VAXstation 500, is based on the MicroVAX-1 and incorporates the Tektronix 4125 color video terminal. Using Digital's MicroVMS operating system, the VAXstation 500 can be linked to other VAX and PDP-11 computers via DECnet/Ethernet LANs. The base configuration for the VAXstation 500 consists of a MicroVAX-1 processor with 1 Mbyte of main memory, a dual 400 Kbyte floppy disk drive, a 31 Mbyte mini Winchester hard disk and a graphics subsystem. The graphics subsystem consists of a 19″ color monitor, a 80286/287 graphics processor, 256 Kbytes of display list memory, a 16-million-color pallette and a keyboard.

In addition to the hardware announcement, Digital Equipment (Maynard, MA) jointly announced with Silvar-Lisco (Menlo Park, CA) the availability of computer-aided engineering software that runs from workstations to host systems. The availability of the new software enables both VAXstation 1 and 500 systems to be fully integrated as CAE workstations into a network of VAX systems using DEC's DECnet/Ethernet products. Under Digital's Cooperative Marketing Program (CMP) agreement, Digital and Silvar-Lisco have engaged in cooperative marketing activities for CAE and CAD for the electronics industry since 1982.

Silvar-Lisco's Structured Design System (SDS) consists of a collection of CAE tools that enable designers to input design data, to create netlist information used as input to simulators and layout tools and to produce hard copy plots. SDS modules are available for design entry, partitioning, and checking and expansion.

The front-end program allows schematic component and wiring information to be entered in the SDS Design Database. This information is entered through a graphical schematic capture program called CASS (Computer-Aided Schematic System). After entering a schematic diagram with CASS, a compiler program called NLE (netlist extractor) is used to check the schematic data for wiring and naming violations. A similar program, SDLOAD, is used to load netlist entry (SDL) into the design database. The schematics entered into the design database are hierarchical, meaning that the symbols on a top-level schematic can contain underlying schematics that can also be viewed or edited. A program called HIDEX allows hierarchical schematics to be expanded so that components or levels of hierarchy are removed and replaced by their logic descriptions. This expansion is then saved as a separate netlist. Symbols, instances of symbols or entire levels can be saved.

The price of Silvar-Lisco's Design Capture System on a VAXstation is approximately $10,000 each. *—Wilson*

*Digital Equipment Corp.* **Circle 231**
*Silvar-Lisco* **Circle 232**

# Can you picture a single-board PC graphics controller with 32-bit planes?

© Image courtesy of Artronics/3M by Scott Lewczak.

## The New REVOLUTION™ 512 x 32.

We built a combination of advanced capabilities into the latest Revolution board... like our unique megabyte of multi-ported display memory, 16 million colors with overlay capabilities, hardware zoom and optional video broadcast compatibility. The kind of architecture you'd like to specify for your system needs.

Our single-board design won't tie up the PC's expansion slots and power supply. And you can update the screen with uninterrupted bus access to our memory-mapped display buffer. A feature that gives you speed and programming versatility with a minimum of effort.

Compare our specs and prices and you'll see why Revolution graphics controllers are a part of the most advanced and competitively-priced PC design systems available today. Not tomorrow. Not someday.

Get the whole picture by calling (617) 492-0999. Or write: Number Nine Computer Corporation, Dept. G2, 691 Concord Avenue, Cambridge, MA 02138.

**Specifications:**

**System:** IBM PC, XT, AT and compatibles.
**Requirements:** 2.6 amps, one expansion slot.
**Memory:** 1 Megabyte on-board video RAM.
**Resolution:** 512 x 512 pixels.
**Bit Planes:** 32 bit planes (8 bits per gun, two 4-bit overlays).
**Color Specs:** 16.8 million colors selectable, 256K colors simultaneously viewable. Three 4K x 8 read/write look-up tables.
**Display Buffer Access:** Multi-ported access by both host processor and on-board graphics processor.
**Display Buffer R/W Modes:** Pixel mode, RGB-gun mode, concurrent mode.
**Hardware features:** 1–16X zoom, pan, scroll and split screen.
**Optional Output:** RS-170A Genlock.

# It's here.

number nine
Computer Corporation

See us at Booth 109.
NCGA

Revolution is a trademark of Number Nine Computer Corporation. IBM is a registered trademark of International Business Machines, Inc.

Circle 64 on Reader Inquiry Card

# Enhanced Drives, Controllers Expand 3380 Line

Four new 3380 drives and larger cache memories for 3880 model 21 and 23 controllers have extended the range and capabilities of IBM's 3380 14" Winchester line. AD4 and BD4 single capacity (same capacity as existing 3380s) and AE4 and BE4 double capacity drives provide up to a 15% increase in performance, but can still use 3880 controllers.

IBM says the new AD4 and BD4 units will have average access times of 15 msec, and the double capacity AE4 and BE4 models will average 17 msec. Though track organization of 3380 models AD4 and BD4 is identical to that of the current 3380 Standard models, the double capacity drives have twice that track density. AE4 and BE4 units provide 5.04 Gbytes of storage per unit unformatted; the single capacity models hold 2.52 Gbyte, as do current 3380s.

New 3880 H21 and H23 controllers have up to 48 Mbytes cache and J21 and J23 models have 64 Mbytes, up from 32 Mbytes maximum. The increase is achieved by using IBM's 256K (actually 288K) RAM chips.

Either the 3880 model 23 or the model 3 controller can interface the enhanced capability 3380 drives to a System 370 computer. These "storage directors" can handle 32 actuators; with four actuators (two for each of the two HDAs) per drive, this permits strings of four. With the maximum number of double capacity drives in one string, the controller sees a single 20 Gbyte unit.

A Device Level Selection (DLS) function of the extended capability drive models enables concurrent data transfer from any two actuators within a string; this includes those of the same head-disk assembly (HDA). The new drive models are also supported by Dynamic Path Selection (DPS), which allows reconnections to be established along any available path. A performance improvement in the Dynamic Path Reconnection algorithm has further reduced the time needed for reconnection. Using DPS in the extended architecture (XA) mode provides systems the 15% improvement quoted, while using the new drives in equal data/equal device comparisons under System/370 mode improves performance by about 5%.

The Data Facility software support programs for Multiple Virtual Storage (MVS) systems have been enhanced to accommodate the new controllers and drives, as well.

The new single capacity drives are the same price as current 3380 models, $88,780 for the AD4 and $64,440 for the BD4; they became available in March. Double capacity AE4 and BE4 drives are to be available 4th quarter and will cost $134,740 and $110,400 respectively. At that time, upgrades from single to double capacity will cost $45,960. Minimum monthly maintenance charges have been reduced 10% for new models. New 3880 controllers will be available sometime this quarter at $349,975 for the 48 Mbyte model and $429,975 for the 64 Mbyte model.

*—Pingry*

**Circle 234**



# Mixed Memory Models In C Compiler Enhance 16-Bit Performance

Whitesmiths Ltd. (Concord, MA) has announced an enhanced version of its C compiler for the 8086 computer family. Version 3.0 features the ability to support all 8086 memory models, in addition to mixed models formerly only available to assembly language programmers. Other enhancements include compiler and assembler source listings enabling the programmer to view high level source code, assembler source and generated code on one listing and source level interactive debugging with breakpointing and variable display.

The compiler adheres more closely to the emerging ANSI C standard, allowing long identifiers, enumerations and struct assignment. Arguments can now be declared to a function for coercion and type checking. A full ISO Level 1 implementation of Pascal, in addition to several popular Pascal extensions, is available for Version 3.0. These extensions include a string data type, the ability to open files by name and an "else" clause for case statements.

The variety of memory models available with the Version 3.0 C compiler enables the programmer to mix the models selectively within applications. In several applications, the results are 16-bit C programs which perform as if running on a 32-bit machine or written in assembly language. The usual global memory models, from "small" to "large," can be specified for an entire program at compilation.

Whitesmiths' C address space modifiers permit the programmer to control the use of segment override prefixes for each function and data object. They also allow the specification of I/O data ports for generating such instructions in-line.

Two models, the 8080 and the small 8086, allow efficient addressing since the 16-bit address for both is sufficient to address any function or object. All memory references are relative to segment registers and, therefore, fully relocatable. However, the use of small pointers restricts the entire program to one or two 64 Kbytes of memory. The large 8086 memory model allows the programmer to access more memory at the expense of execution speed. Data reference pointers of 32 bits may cause a program to double in size and to run half as fast. In addition, longer times for function entry and exit and greater demand on the run time stack space result.

With mixed models, the manipulation of a few large data objects need not penalize an entire program which may consist primarily of small data objects. A linker constructs an executable image from multiple program segments; each segment has internal functions and data which are accessible through small pointers. The Whitesmiths' linker is able to load multiple copies of the same library functions for each segment, eliminating time and space penalities incurred by the use of a large model library.

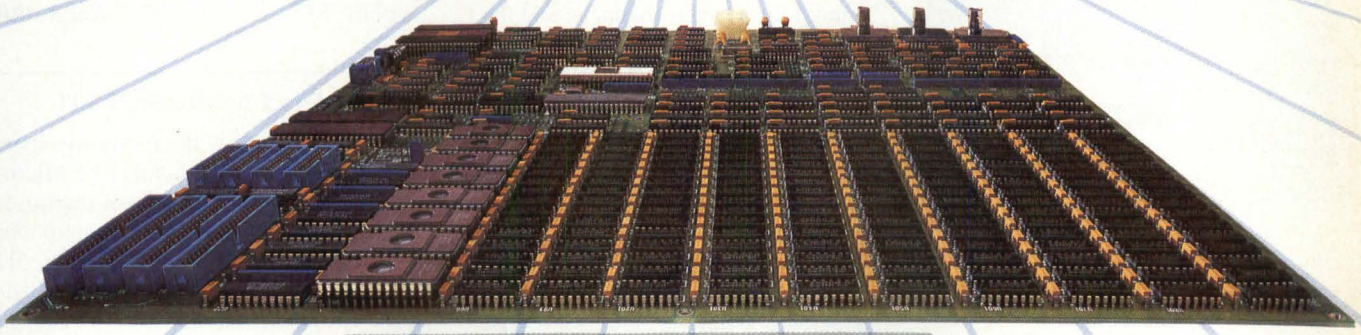
*—Meng*

**Circle 230**

# OMNI 1000 GDC™

**MEANS**

# FREEDOM




**FREEDOM** to interface the bus independent OMNI 1000 GDC to your host via DMA, Parallel I/O or Serial RS-232C with off-the-shelf hardware available for most bus architectures.

**FREEDOM** to reduce software development cost. Use the OMNI 1000 GDC together with OMNILIB host interface library (FORTRAN or C) for full GKS compatible functionality.

**FREEDOM** to reap the benefits of the OMNI 1000 GDC multiple processor design. Overall system performance is enhanced by local scale, rotate, translate, polyfill, drag, clip, highlight, rubberband, etc. provided by the display list processor.

**FREEDOM** to choose the OMNI 1000 GDC configuration which fits your needs; circuit board only, rack-mount/tabletop enclosure or complete graphics terminal.

The OMNI 1000 GDC is a single board graphics controller with display resolution of 1024 x 1024 x 8 planes. High performance graphics, segmented architecture, bus independence and an extraordinary high level of field proven reliability are hallmarks of the OMNI 1000 GDC.

Circle 67 on
Reader Inquiry Card

**Omnicomp™**
**Graphics Corporation**

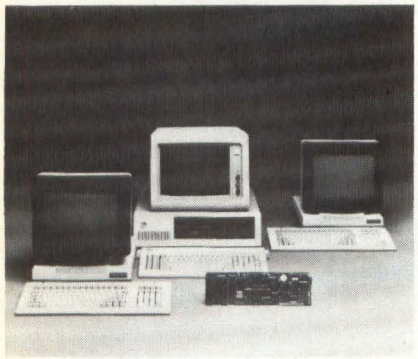
*Optimizing Computer Graphics . . . by Design.*

See us at
Booth 2432
NCGA '85
April 14-18
in Dallas

1734 West Belt North, Houston, Texas 77043 • 713/464-2990 • Telex 285801 OMNICO UR

## COMPUTERS/SYSTEMS

### Applications Processor



The AM-170 applications processor, also called the AMOS/PC Upgrade Package, includes a 68000 $\mu$P and the AMOS multiuser, multitasking operating system. Allowing an IBM PC with a hard disk to be converted into a one to three terminal multiuser system, the AM-170 can be combined with AlphaMate's software program; PCs will function as terminals linked to an IBM PC containing an AM-170. Memory on the system's hard disk can be partitioned between AMOS and MS-DOS, and AMOS and MS-DOS files can be transferred between the two operating systems. Price (with AMOS) is $2,800. **Alpha Micro**, Irvine, CA **Circle 192**

### Concurrent Computer

The iSPC family of concurrent computers combines a multiple instruction multiple data (MIMD) parallel-processing architecture and commercially available VLSI components in a system composed of computational nodes. These nodes, each a small computer with its own local memory, perform tasks concurrently. The initial product line consists of the iPSC/d5: 32 computational nodes and 16 Mbytes of distributed memory; iPSC/d6: 64 computational nodes and 32 Mbytes memory; iSPC/d7: 128 computational nodes and 64 Mbytes memory. Each node includes one 80286 CPU, an 80287 numeric processor and 512 Kbytes memory. The iSPC products have a performance range of 2.5 MFLOPs to 10 MFLOPs, with prices from $150,,000 to $520,000. **Intel,** Beaverton, OR **Circle 184**

### Dedicated Benchtop Logic Analyzer

Providing state analysis, timing analysis and digitizing oscilliscope functions, the HP 1631A/D logic analyzer is a follow-on product to the HP 1630A/D/G line of standalone benchtop logic analyzers. While the HP 1631A has 27 state channels and eight timing channels, the D model has 27 state channels and 16 timing channels, or 35 state and eight timing. Additionally, the HP 1631A can be configured for 43 state channels, and the D model can be configured for 43 state channels. Two analog channels are available with 200M sample/sec digitizing rate. Single-shot time-interval measurements can be made with an accuracy of up to $\pm$1.5 nsec. Price is $11,000 (1631A) and $13,000 (1631D). **Hewlett-Packard**, Palo Alto, CA **Circle 191**

### Word Image Processing System

Based on flat-bed scanner technology, the Model 700 Word Image Processing System interfaces with most IBM PC word processing and database management software. Operating with the IBM PC XT or AT as a front-end peripheral, the system contains the Model 210 Image Scanner, the Model 111 Imaging Interface, WIPS software and interconnect cable. With illumination built into the system, resolution of the scanned image is 200 dpi across the horizontal scan line; users can select either 200, 150 or 100 lines/inch in the vertical dimension. Price is around $4,000. **Datacopy**, Mountain View, CA **Circle 195**

### Improved Mid-Range Systems

With 16 Mbytes of memory expandable up to 128 Mbytes, the Cyber 180 models 840, 850 and 860 systems make up an enhanced series of mid-range processors. The Network Operating System (NOS) operates with 6-bit character/60-bit words, and the new Network Operating System/Virtual Environment (NOS/VE) operates with 8-bit character/64-bit words. Featuring a microcoded central processor with cache memory that is capable of suporting up to 16,777K 64-bit words, all three models use subnsec ECL circuits and LSI arrays. The Model 860 can have one or two central processors and each is independent with its own cache memory; they share only central memory. Models 840, 850 and 860 have a memory transfer rate of one word every 64 nsec (max). **Control Data**, Minneapolis, MN **Circle 188**

### Low-End MicroPDP-11

Fully compatible with existing members of the MicroPDP-11 family, the MicroPDP-11/SV is an entry-level multiuser system. The system supports up to four users and includes the F-11 CPU, 512 Kbytes of main memory, RDS, 10 Mbyte Winchester disk drive, 400 Kbyte RX50 diskette, with a 2SLU 4-slot backplane. The new MicroPDP-11/SV will run Digital's A-to-Z Integrated System, integrating graphics, word processing and spreadsheets with customized business applications. Available with an optional 31 Mbyte disk, the MicroPDP-11/SV is priced at $5,995. **Digital Equipment Corp.** Maynard, MA **Circle 198**

### Enhanced Desktop IBM PC-Compatible PCs

Similar to Corona's earlier line of IBM PC-compatibles, the PC400 Series of desktop PCs offers 640 $\times$ 400 resolution and a larger 14" swivel monitor. Screen resolution is software selectable so users can run in IBM's medium and high 200-line resolution modes and in Corona's 400-line mode without an adapter card. The 16-bit 8088-based PC 400 Series is available in several configurations: 360 Kbytes half-high floppy drives and standard memory of 256K; 256K RAM and two half-height floppy drives; and a single half-height floppy drive, a 10 Mbyte hard disk and 256K RAM. Prices range from $2,650 to $4,395. **Corona**, Thousand Oaks, CA **Circle 196**

## Fault Tolerant Computer

With eight dual application processors, the Reliant II fault tolerant computer can be tailored to the individually required level of dual processor redundancy needed. The dual application processors are connected via dual data buses to a mirrored file system of dual file processors, dual disk controllers and dual hard disks. Powered by dual power supplies and dual power buses, the system is also backed up by duplicated internal UPS battery packs. Cost of an entry level Reliant II with one fault tolerant processor pair is less than $30,000. With 140 Mbytes files fully mirrored on a pair of hard disks with any combination of dual processors, using 16 Intel 8086s each with 256K RAM, the cost is under $85,000. **NoHalt Computers,** Farmingdale, NY **Circle 185**

## High-End Supermini

Supporting up to 254 terminals in an interactive environment of up to 255 processes, the 9955 superminicomputer uses the PRIMOS operating system. Hardware and software compatible with the firm's 50 series systems, the 9955 includes a 32-bit CPU featuring ECL circuitry and pipelined architecture, up to 16 Mbytes of error correcting MOS memory, burst-mode I/O, hardware instruction assists, 64 Kbytes cache memory (with a 40 nsec access time) and a diagnostic processor. Upgrades from the Prime 9950 cost $45,000 and (for all other systems) $177,000 to $327,000. **Prime Computer**, Natick, MA **Circle 189**

## 200 Pixel/Inch Image Scanner

The MS-200 desktop image scanner accepts documents up to 8½″ × 24″, digitizes the image at 200 pixels/inch resolution and transfers the image to host computer memory. Switch selectable scanning modes include text, picture and mixed. In mixed mode, up to four picture windows are allowed. The MS-200 features stationery optics assembly to aid in misalignment problems. Performing Group 3 1-D CCITT data compression at a 10 to 1 ratio for text and comparable compression ratio for graphics, the MS-200 uses a sensor array and a real-time algorithm that compensates for the nonuniformity of the CCD image array. Price is $1,700. **Microtek Lab**, Gardena, CA **Circle 190**

## PERIPHERALS

### Desktop Tape Storage

Holding up to 900′ of magnetic tape, this 9-track reel-to-reel storage system (Reel-Core 7) stores up to 33 Mbytes of information on its 7″ reel. Recording at 1600 and 3200 bpi, the Reel-Core 7 has tape speeds of 25 and 50 inches/sec, and can copy data at a maximum rate of 80,000 cps. It also has built-in diagnostics for self-testing and comes with its own PC-compatible board and software. Price is $4,495. **Lancore Technologies** Westlake, CA **Circle 174**

### Coax Protocol Converter

Attaching non-IBM output devices to IBM 3270 cluster controllers, the Series II+ 3287/Coax Protocol Converter emulates the functionality of an IBM 3287 Model 1 or 2 printer, allowing the ASCII printer to appear to the host as a 3287. The Series II+ 3287/Coax supports RS-232-C, Dataproducts, Centronics, as well as the firm's Graphic Controllers. Depending on the application program and local controller, the 3287/Coax accepts SNA LU1 (SCS), SNA LU3 (DSC) or BSC data streams. Price is $1,995. **KMW**, Austin, TX **Circle 167**

### Complete Mass Storage For IBM PC, AT, XT

Integrating five separate devices in a single half-height box (2½″ high), the Masterflight storage system is designed for the IBM PC, AT and XT. The system contains a half-height 10, 20 or 33 Mbyte hard disk, a backup system (half-height 20, 40 or 60 Mbyte streamer tape), five power direction switches (computer monitor, printer and two auxiliary switches), a locking security key and a surge protector. Price is $3,795. **Kamerman Labs**, Beaverton, OR **Circle 163**

### Interface Pod

Designed for testing and troubleshooting 8051-family microprocessors, the 8051 Intelligent Interface Pod is the interface between the Unit Under Test (UUT) and a Fluke 9000 Series Troubleshooter. It has its own μP on-board and eight configuration switches which are set to match the specific UUT configuration. The Pod is connected to the UUT directly through the μP, performing a variety of tests, including Bus, RAM, Short, ROM, I/O, RAM Long and Auto Test. Price is $1,995. **John Fluke Manufacturing**, Everett, WA **Circle 165**

### Color Display Terminal

Designed for use with the firm's 932 Supermicro family, as well as with other UNIX-based systems, this color display terminal, the ColorScan 90, allows simultaneous display of up to eight active tasks, each with vertical and horizontal scrolling. Eight background and eight foreground colors display data in 64 combinations. The 12″ nonglare screen presents characters and images in 80- or 132-columns. Price is $1,995. **Datamedia**, Nashua, NH **Circle 170**

### 20-Mbyte Tape Drives

With formatted capacity in excess of 20 Mbytes and a data transfer rate of 500,000 bps, the Model 125 drive has a 5¼″ half-high form factor and the Model 225 drive has a 3½″ half-high form factor. Designed for IBM PCs and compatibles, the drives are sized to slip into the same size cavities as floppy drives. They operate in streaming mode or in file-by-file mode and use the 3M DC 1000 tape cartridge. With MTBF of 12,000 hours, the drives employ closed-loop servo head positioning technology. In quantities of 1,000, the drives are priced at $330. **Irwin Magnetics**, Ann Arbor, MI **Circle 175**

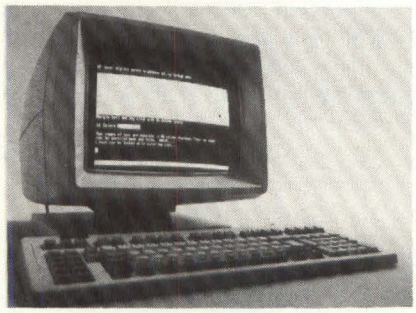
### Photoplotter

Installed on a standard working table, the DP-1504R photoplotter can be operated directly via an RS-232-C link or by a peripheral data station using mag tape or floppy disks. Printed circuit artwork is produced on film or photographic glass plate. The true flatbed construction with vacuum hold-down accepts any type of photographic material of any thickness with dimensions up to 19.0″ × 27.5″. The built-in microprocessor controls the operating parameters, such as light beam intensity or plot speed. An optional dual penhead can be mounted in place of the photohead for check plots and artwork on paper. Two pen stations accept either ink pens or ballpoint pens. Price is $29,000. **Glaser**, Volketswil, Switzerland **Circle 180**

### IBM 3270 BSC/SNA Protocol Conversion

Allowing up to 24 async ASCII devices to communicate with an IBM or equivalent host computer using either SNA/SDLC or BSC protocols, the MC800 appears to the host as an IBM 3274 or 3276 communications controller with 3278/3279 terminals attached. The MC800 comes in port configurations of 5, 7, 8, 9, 12, 16, 20 and 24 ASCII ports. User configurable to support all standard async baud rates up to 19.2 Kbaud, the MC800 allows any mixture of CRTs and printers to be attached with automatic baud rate detection for CRTs at all speeds. Price starts at $3,600 for the 5-port unit. **Innovative Electronics**, Miami, FL **Circle 173**

### Color Graphics Terminal



A lower-priced version of the earlier PST100 terminal, the PT200 "Performer" terminal offers four display formats, amber, green or b/w screens and a keyboard in one of nine different language versions. The 14″ diagonal, nonglare bezelled screen (and choice of three phosphors) provides 80- or 132-column display and folded-page support for 160 columns. Screen resolution is 720 × 300. The detached keyboard features 26 character-attribute and editing function keys, along with 26 application-function keys. Price is $995 or $1,695 with optional color monitor. **Prime Computer**, Natick, MA **Circle 171**

### 300 DPI Laser Printer

Based on the Canon LBP-CX laser xerographic engine, the LaserWriter prints eight pages/minute at 300 dpi output. The LaserWriter has the AppleTalk Personal Network built in, as well as an RS-232 port to connect it to devices outside AppleTalk. Controller hardware contains a 12 MHz 68000, ½ Mbyte of ROM and 1½ Mbytes of RAM. Supporting the Postscript programming language, the LaserWriter stores fonts as mathematical formulas, rather than as a bit map for every size and style of a typeface. Price is $6,995. **Apple Computer**, Cupertino, CA **Circle 181**

### Thermal/Dot Matrix Printers

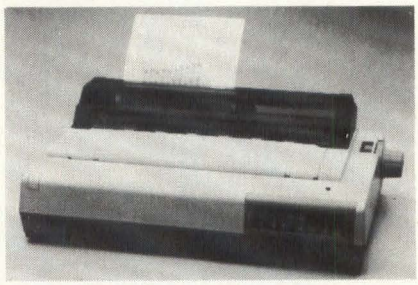
An expansion to the company's line of printers and sheet feeders, the T1000 Thermal Printer features a 24-element print head and an IBM PC-compatible command set and offers nlq print speed of 40 cps and 80 cps draft. The T90 Thermal "Message" Printer plugs into a standard telephone jack and performs as a hard copy answering machine. With a 7 × 5 matrix, the T90 is a 40-column, 40 cps unit that can be equipped with RS-232 and modem interfaces. The 8510S/SC multimode serial matrix printers are enhanced with nlq capabilities. Prices are $350 (T1000), $150 (T90) and $795 (8510S2), $895 (8510SC2). **C. Itoh**, Los Angeles, CA **Circle 178**

### Host-Independent Communications Network

An enhancement to the PIX/PIXNET product line, the PIXNET-XL communications system is designed for high speed data transmission in the IBM environment. PIXNET-XL extends the block or byte multiplexer channel of IBM mainframes to connect high speed devices at any location, to any CPU in the network. The PIXNET-XL distributes communications intelligence to key controllers in the network by using HDLC communica-

tions protocol with data compression and by allowing devices attached to PIXNET-XL to appear as local channel attached peripherals to the host CPU. Price per link ranges from $95,000 to $125,000. **Paradyne**, Largo, FL **Circle 164**

## Letter-Quality Matrix Printer



A multifunctional, serial matrix printer combining letter-quality text and color graphics, the Model 750 prints letter quality at 100 cps, has data processing speed of 200 cps and prints graphics at 10 ips. Character resolution for letter quality is 180 × 360, 180 × 180 for draft and graphics. The 750 features standard courier 10 LQ/DQ, letter gothic 12 LQ/DQ and gothic 17.1 DQ fonts. For downloadable fonts or transfer buffer, RAM is expandable to 72K. With standard friction feed, and optional tractor feed and automatic sheet feeders, the 750 provides multiple part forms printing up to four parts. Price is $1,990. **JDL**, Westlake Village, CA **Circle 166**

## IBM Series/1 Streaming Tape Storage

An expansion to the firm's family of peripherals for the IBM Series/1 minicomputer, this ¼" streaming tape system (certainty 810) provides up to 60 Mbytes of formatted disk backup data storage using DC 600A or equivalent ¼" tape cartridges. The storage system includes the streaming tape drive, an attachment controller that plugs into the Series/1 processor and software utility programs. The Certainty 810 System operates in either full disk or selective data save/restore modes. Price ranges from $3,500 to $5,000. **Control Data**, Minneapolis, MN **Circle 177**

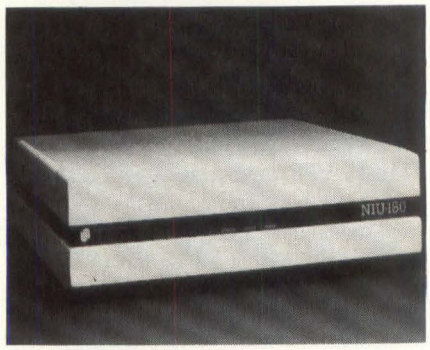
## Distribution Terminal

A full-featured emulation of the Wyse 50 terminal, the Fame 50 features a 14" green screen with the capability for 80- and 132-columns. The terminal also includes 16 programmable function keys with extended storage of 256 characters, as well as programmable editing keys. Also included is a buffered bidirectional printer port with two independent baud rate settings. Compatible with TeleVideo's 925, 920 and 910, and Lear Siegler's ADM-31 terminals, the Fame 50 features a 7 × 9 dot matrix in a 9 × 12 cell for sharper character definition. Price is $595. **Falco**, Sunnyvale, CA **Circle 172**

## Program Option Package

The Program Option Package, or POP-PAC, looks like an 8-track tape cartridge and plugs into the basic 81X Communications Processor, Openline. A number of POP-PACs are available for the 81X Openline: an async/bisync protocol converter, single-link stat mux, dual-link networking mux, dual-link networking switch mux and a single-link X.25 pad. With the appropriate POP-PACs, units can be concentrated to form 16- or 24-port configurations or can be used to build nine node networks with up to 72 channels. **Case Rixon Communications**, Silver Spring, MD **Circle 179**

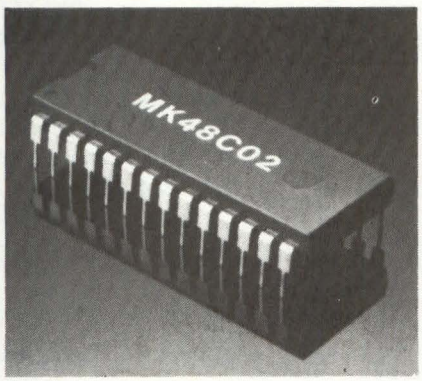
## Network Interface Unit




Based on the 801896 μP, the NIU-180 network interface unit connects eight user devices to the firm's Net/One LAN system. Net/One software running on the NIU-180 now allows each of the 8 ports to be configured with an individual password. The parameters of each NIU-180 port can be reconfigured from the Net/One Network Management Console (NMC), without affecting any other ports on the same NIU. Other services available with the NIU-180 include idle circuit time-out and automatic baud rate detection. The NIU-180 operates at 8 MHz and supports up to eight ports simultaneously running at 96 Kbaud, with data rates up to 19.2 Kbaud also supported. Price is $2,950. **Ungermann-Bass**, Santa Clara, CA **Circle 168**

## COMPONENTS

### 16K CMOS Static RAM




Eliminating the need for external fail detection and battery switching circuitry, the MK48C02 CMOS SRAM uses an external battery pin and features write protection circuitry. As $V_{cc}$ falls below 4.75V, read and write circuits disconnect $V_{cc}$ and substitute $V_{bat}$. Internal memory is isolated from all address and R/W activity until $V_{cc}$ rises above 4.75V. In addition, the MK48CO2 provides a power fail detect output that disables other devices sensitive to low $V_{cc}$. It is available in two versions: with data retention $I_{Bat}$ less than 50 $\mu$A at 70°C (50 nA typical at 23°C) or less than 1 $\mu$A at 7°C (1 nA typical at 23°C). Both versions offer 150, 200 and 250 nsec access times and prices are $16-$18, $12-$14 and $12-$13, respectively. **Mostek**, Carrollton, TX **Circle 141**

### 64-Kbit HMOS DRAM

An enhanced version of the MCM6665A, this 64-Kbit HMOS DRAM, the MCM-4164BP15, features a smaller die size and laser redundancy. Incorporating a 100 nsec access time with a power dissipation of 302.5 mW in the active mode and 22 mW standby, the MCM4164BP15 is fully TTL compatible. Maintaining upward pin compatibility from the 16K MCM-4116 RAM and MCM4517 RAM, it has a 128-cycle 2 msec refresh and a 155 nsec page mode cycle time. Packaged in a 16-pin plastic DIP and operating from a single +5V power supply, the MCM-4164BP15 is priced from $5.18 to $5.74, depending on quantity. **Motorola**, Austin, TX **Circle 135**

### 12-Bit A/D Converter

This 12-bit A/D converter, the ADC 574A, offers selection of 8-, 12-, or 16-bit $\mu$P bus interface. With a 25 $\mu$sec max conversion time and 150 nsec bus access time, the ADC574A contains a +10V reference, internal clock, digital interface for $\mu$P control and TTL-compatible three-state parallel format output. There are no missing codes over 0°C to +75°C and -55°C to +125°C. The ADC574A operates from +5V and ± 12V or ± 15V supplies. The reference circuit, containing a buried zener, is laser-trimmed, and the clock oscillator is current-controlled. Packaged in a hermetic 28-pin side-brazed ceramic DIP, price in 100s ranges from $31-$124. **Burr-Brown**, Tucson, AZ **Circle 132**

### P-Channel COMFET

Complementing RCA's N-channel COMFET, this new P-channel COMFET has the same chip area as the N-channel and, therefore, the same input capacitance. The P-channel COMFET has a DC on-resistance at forward blocking voltages between 200 and 400V—0.35 ohms at 20A in a 3 mm × 3 mm pellet. The COMFET overcomes a conventional MOSFET's limitations as a power switching element above 200V by increasing the conductivity of its epitaxial drain region through the injection of minority carriers. **RCA**, Somerville, NJ

### Number Controlled Oscillator

With 8-bit resolution sine and cosine outputs, the ST-1172 number controlled oscillator (NCO) provides a clock frequency of up to 12 MHz. It is microprocessor bus-compatible and provides 28 bits of programming resolution. Consuming less than 100 mW power ($f_c$ ff 200 kHz), the ST-1172 has a DC to 6 MHz output frequency range. In all digital applications, the NCO can generate precision, real-time, sine and cosine functions. **Stanford Telecommunications**, Santa Clara, CA **Circle 146**

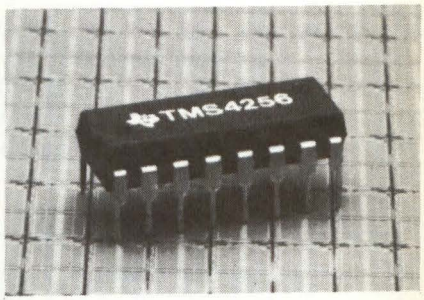
### CMOS Cell Library

An addition to the CMOS 80C86 microprocessor library, these LSI peripherals include a DMA controller, UART and interval timer, each above the 2000-gate level. Powered from a 5V supply, the library provides circuit densities of up to 7000 2-input NAND gate equivalents. Also featuring I/O cells that offer 10 nsec into pF load, the library has drawn channel lengths of 2.5 microns. This standard cell library is supported by the Teledesign design automation system. Software includes schematic capture, logic simulation, auto place, auto route, electrical and design rule verification. **Harris**, Melbourne, FL **Circle 142**

### Nonvolatile RAM

When used with 8-bit microcontrollers and multiplexed microprocessors, the 2001 NVRAM eliminates the need for interface circuitry by transmitting address and data information on the same lines. On-chip data protection circuitry detects when the power supply drops below 4V, and the internal erase and write circuitry shuts off. The 2001's 128 × 8 bit architecture allows designers to design in only one chip to achieve parameter storage in 1 Kbit of byte-wide nonvolatile memory. Price is $11.20 in quantities of 10,000. **Intel**, Santa Clara, CA **Circle 133**

### 256K DRAMS




Available in page-mode device (TMS4256) and nibble-mode device (TMS4257), these 256K DRAMs are packaged in 16-pin plastic DIPs; pin-out and package dimensions meet the JEDEC standards. Using the same refresh scheme as the firm's 64K DRAMs, they are upward compatible, allowing quadrupling of system memory capacity without redesign or additional hardware. Alternatively, the 256K DRAM may be used to reduce physical system size while maintaining memory capacity. Available in 150 nsec and 200 nsec row address access times, column address access times are 75 nsec and 100 nsec, respectively. Typical power dissipation is 300 mW operating and 12.5 mW standby. The TMS4256's page-mode capacity allows access of up to 64 bits of data and the TMS4257's nibble-mode capability provides serial access of up to 4 bits of data. Fabricated with 2-micon N-channel double-level polysilicon gate single-level metal technology, the 256K DRAMs sell for $27.20 (150 nsec) and $24 (200 nsec), in quantities of 100. **Texas Instruments**, Houston, TX **Circle 214**

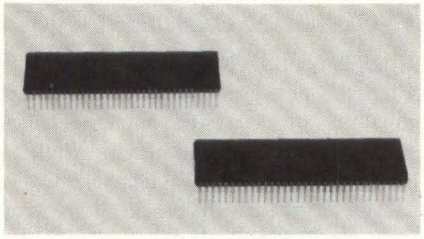
## Monolithic Voltage-To-Current Converter/Transmitter

Housed in a 16-pin DIP, the XTR110 precision voltage-to-current converter/transmitter has 0.01% max nonlinearity (12 bits). It converts 0V to +5V and 0V to +10V inputs into 4 mA to 20 mA, or 5 mA to 25 mA outputs. A precision +10V reference output on the chip drives loads up to 10 mA. An external transistor can be added for more current; e.g., 33 mA for 300 ohm bridges. With a supply range of 13.5V to 40V and 30 ppm/°C drift, the XTR110 has a settling time of 15 μsec to 0.1% of span and operate over a -55°C to +125°C range. Price in 100s is $10.95 **Burr-Brown**, Tucson, AZ **Circle 137**

## Data Acquisition Macrocomponent

Designed for use with the MA2000 family of macrocomponents or any microprocessor system, the MA2400 data acquisition macrocomponent delivers 14 single-ended input channels with 12-bit plus sign resolution. The internal variable gain amplifier handles signal levels from ±40 mV to ±5V full scale. A software-controlled low power standby mode is available as well as software selectable gains of ±1 to +128 in binary steps. With internal power consumption of 1.25W active and 55 mW standby, the MA2400 features accuracy over a -25°C to +85°C temperature range. Price in 100s is $400. **National Semiconductor**, Santa Clara, CA **Circle 129**

## 8-Bit CMOS CPU

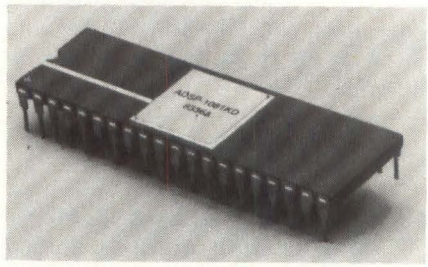


Designed to support CP/M and MSX operating systems, the HD64180 8-bit CMOS CPU incorporates an on-chip MMU and two-channel DMAC. The microcomputer's 6 MHz clock rate and expanded instruction set achieve 16-bit performance while compatible with existing CPU families. The device also features an on-chip wait state generator, DRAM refresh, two-channel ASCI, clocked serial communication interface, two-channel, 16-bit programmable reload timer, 12-source interrupt controller and a dual bus interface. In quantities of 1,000, the HD64180 sells for $15. **Hitachi**, San Jose, CA **Circle 127**

## CMOS Switched Capacitor Filter

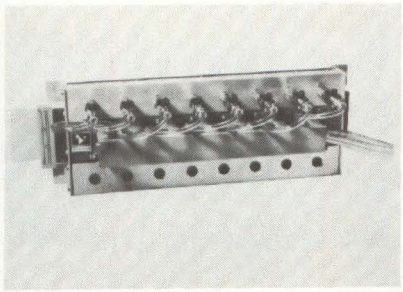
Operating from 4.75V to 7.0V and consuming 50 mW (typically), this CMOS switched capacitor filter (MSM6912) contains two filters in the same package. Providing external gain adjustment for both the transmit and receive filters, the MSM6912 can also be used as an impedance-transforming buffer. The filter's response can be shifted in frequency by adjusting the rate of the switching clock. Packaged in a 16-pin ceramic DIP, the MSM6912 sells for $5.80 in quantities of 100. **Oki Semiconductor**, Sunnyvale, CA **Circle 143**

## 8 × 8-Bit CMOS Digital Multiplier



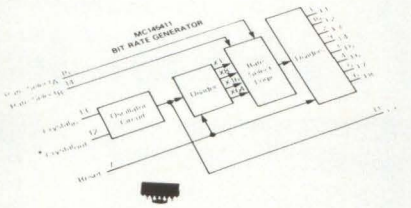
As a pin and function-compatible alternative to TRW's MPY-8HUJ, the ADSP-1081 8 × 8-bit CMOS digital multiplier provides maximum 85 nsec multiply time and 100 mW power dissipation. Maximum cycle times are guaranteed over each grade's temperature range: J and K grades are specified at 100 and 85 nsec, respectively, at +25°C and at 115 and 100 nsec from 0 to +70°C; S and T grades are guaranteed at 100 and 85 nsec at +25°C and at 130 and 115 nsec from -55°C to +125°C. Packaged in a 40-pin hermetically sealed ceramic DIP, the ADSP-1081 operates with a single +5V supply and is TTL compatible. Price in 100s starts at $31 and $45 for J and K models. **Analog Devices**, Norwood, MA **Circle 128**

## Direct Pneumatic Interface



The Models 6955, 6956 and 6957 Pneumatic Termination Panels directly interface pneumatic field signals to digital-based data acquisition and control equipment. These termination/conversion panels handle standard pressure inputs and convert them to equivalent mV signals. The 6955 accepts 0 to 15 psi, 0 to 1.05 kg/cm$^2$, or 0 to 206.8 kPa inputs; the 6957 accepts 0 to 100 psi, 0 to 7.04 kg/cm$^2$, or 0 to 689.5 kPa. Available with 8 or 16 input channels, the standard panels have 1/8″ NPT female connectors for direct pneumatic connection. **Acromag**, Wixom, MI **Circle 139**

## Bit Rate Generator



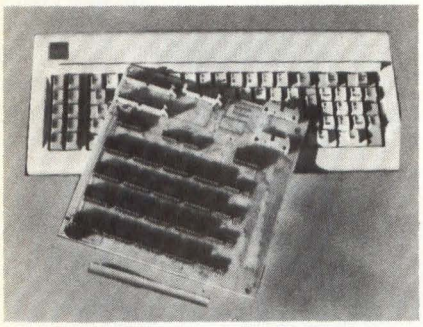

The newest member of the 24-pin MC14411 Bit Generator family, the 16-pin MC145411, has 21 possible bit rates and nine different bit rate output pins. With an on-board oscillator crystal controlled for stability (to 4 MHz) with TTL compatible buffered clock outputs, a 50% duty cycle and programmable time bases for one of four multiple output rates, the MC145411 offers a power dissipation of 30 mW. Noise immunity for the device = 45% of $V_{DD}$ typical. In 100s, packaged in a 16-pin DIP, the MC145411 sells for $3.32 (plastic) and $4.42 (ceramic). **Motorola**, Austin, TX **Circle 136**

## A/D Converter Family

Available in three input configurations, the A/D/A/M-826 family of 16-bit A/D converters, features true 16-bit accuracy. The A/D/A/M-826-1 provides a S/H amplifier (better than ±0.0015% in less than 800 nsec for a full 20V step) producing a complete acquisition and conversion in 2.3 μsec. The A/D/A/M-826-2 features a 100M ohm input impedance buffer amplifier with full-scale settling in 400 nsec, yielding an overall conversion rate of 500 kHz. The A/D/A/M-826-3 is an unbuffered ADC with a 1.5 μsec conversion time. Code differential nonlinearity of ± ¼ lsb is typical in all configurations and differential linearity is stable over temperature, with a temperature coefficient of better than ±1 ppm/°C. All are guaranteed to have no missing codes. Power dissipation ranges from 3.25W (max) for the A/D/A/M-826-3 to 4.5W (max) for the A/D/A/M-826-1. **Analogic**, Peabody, MA **Circle 148**

## BOARDS

### Counter/Totalizer Interface

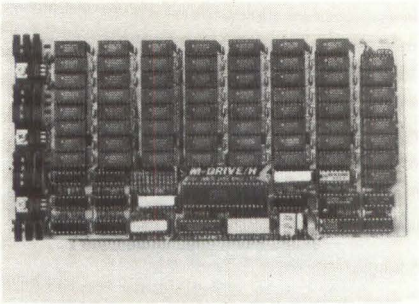


The PC-800/16 Counters Board contains 16 independent CMOS counters with 5-digit capacity each (99999 events) that can be staged to achieve 128 input channels. Counting speed is up to 0.5 MHz and communication with the computer is via parallel communication port and BCD bus of the PC-800/16 card. Requiring +5V power, the counter board also needs 14 communication lines plus two for power and ground between itself and the computer. CMOS counters have input transistor stage (2N3904) and pulse shaping gate (4081) to protect CMOS counters (4534) from overvolatge damage. Input information can be in the form of transistor closure to ground or TTL pulses. Input impedance is 50K ohms. The PC-800/16 is available as a fully populated board with 8 or 16 counters or in an aluminum cabinet. **Columbus Instruments**, Columbus, OH **Circle 152**

### Multibus Probe

This Multibus-based in-circuit emulator, the MBus Probe 86/88, is compatible with the RMX 86 real-time operating system. It plugs into the Multibus and has an umbilical cable which plugs into the CPU sockets of Multibus CPU boards. Loading the program to be debugged can be done remotely or from a local disk under RMX 86 control. Providing real-time trace of program execution, symbolic debugging, hardware breakpoints and memory mapping, the Probe also has a performance analyzer mode showing where to start tuning the program. Price is $3,495. **Atron**, Saratoga, CA **Circle 162**

### 2 Mbyte Disk Drive Emulator



With an expanded memory capacity up to 2 Mbytes, the MDrive/H solid state disk drive emulator operates at RAM speed rather than disk speed, eliminating disk waits. The MDrive/H board systems can consist of one to eight boards, providing users of this firm's IEEE 696/S-100 bus-compatible System 816 Microcomputers with up to 16 Mbytes of storage. The company's standard operating systems, including Concurrent DOS-8-16, CP/M 2.2, CP/M-68K, CP/M 8-16 and MP/M 8-16 contain built-in support for the board. Price is $3,995. **CompuPro**, Hayward, CA **Circle 158**

# WE'VE BROUGHT THE INNOVATORS IN COMPUTER GRAPHICS TECHNOLOGY TO YOU!

## NEW YORK, JULY 10-12, 1985

The east coast has the largest concentration of users and potential users—and as yet no dedicated show. We've changed that! World Computer Graphics '85 will be an annual exhibition and conference staged in New York.

You will see computer graphics hardware, software systems and services for use in CAD/CAM, CIM, CAE, architecture, business management, film and TV, communications, medicine and many other applications. Exhibits, displays, demonstrations and technical advisors will be on hand at the New York Coliseum to make your visit a rewarding and informative graphics experience.

WORLD COMPUTER GRAPHICS '85 NEW YORK
10-12 July 1985
New York Coliseum

**MAIL TO:**
8300 Greensboro Drive, Suite 690
McLean, VA 22102
703/893-4545

## I WOULD LIKE TO ATTEND THE "STATE-OF-THE-ART" CONFERENCE FEATURING 75 SESSIONS FROM LEADING EXPERTS IN THE COMPUTER GRAPHICS FIELDS

I'm interested in receiving the full conference prospectus. Please send detailed information on the following subjects:

- ☐ Graphics technology for factories of the future
- ☐ CAD/CAM for the engineer
- ☐ CIM and CAE for the manufacturing executive
- ☐ CAD/CAM for the architect

Computer graphics applications for:

- ☐ business
- ☐ management
- ☐ communications
- ☐ advertising
- ☐ printing and publishing

- ☐ Film, video, TV, animation and digital effects
- ☐ Graphics technology for medical applications

Please enclose _____ registration forms for me to pass on to other interested members of our company.

Name _____

Company _____ Title _____

Address _____

State _____ Zip _____ Telephone _____

☐ I need _____ complimentary ticket(s) to visit the show

☐ We would like to exhibit if suitable space is still available and may require a _____ x _____ foot booth. Please have the exhibit manager call me.

DD485

*A member of the* Andry Montgomery *Organization*

# 512 MEGA-BYTE

# THE SAM SYSTEM

**High Performance Multi-Port Mass Memory**

# 320 MB/SEC

## FOR INTENSE I/O PROCESSING:

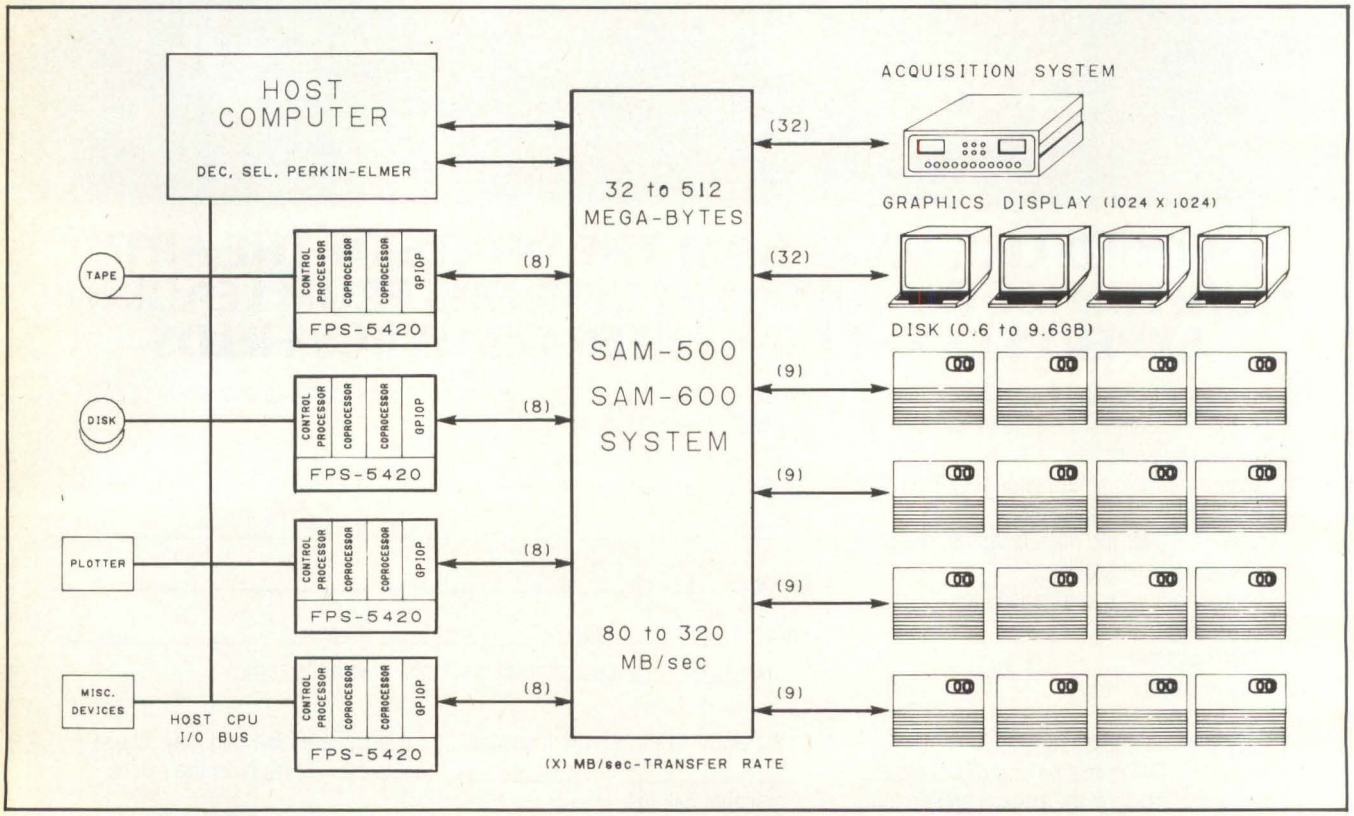
**ON:**
**FLOATING POINT SYSTEMS**
**DIGITAL EQUIPMENT CORP.**
**PERKIN-ELMER**
**GOULD-S.E.L.**

**FOR:**
**REAL-TIME SIMULATION**
**DATA ACQUISITION**
**COLOR GRAPHICS**
**ARRAY PROCESSING**

- LARGE MEMORY CAPACITY
- MEMORY HIERARCHY CAPABILITY
- FIVE SAM ACCESS MODES
- SIMPLE INSTALLATION
- FAST DATA TRANSFER RATES
- MULTI-PORT ACCESSIBILITY
- SEPERATE HIGH SPEED BUSES
- LOW COST ($2K per MB)

Very large capacity SHARED ATTACHED MEMORY (SAM) systems are available for custom installation into your computer system. With this multi-port mass memory system, your computer can more effectively manage extremely large data arrays during intense I/O processing. The SAM-500 chassis holds 96MB (12 I/O ports) and the SAM-600 chassis holds 128MB (8 I/O ports). Each chassis can support an 80MB/sec data transfer rate. Four chassis may be daisy chained together for a capacity of 512MB at 320MB/sec. Also, SAM storage modules can be directly attached to provide an additional storage capacity of 9,600 MB at a 36MB/sec. rate. With a wide range of configurations possible, the SAM system is flexible, expandable, adaptable, and affordable.

NEED INFO: GIVE US A CALL OR GIVE US A VISIT AT SIGGRAPH '85.



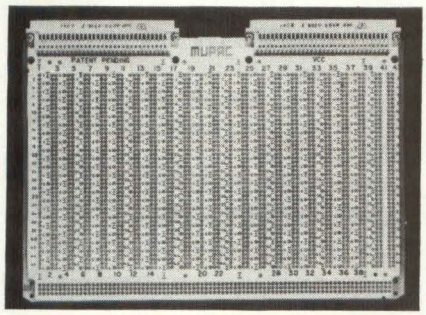

**Texas Memory Systems, Inc.**
9888 Bissonnet #470, Houston, Texas 77036
(713) 771-8200 TLX-792449

Circle 50 on Reader Inquiry Card

## Motion Controller

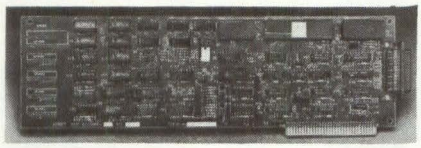
A complete motion controller that plugs into the IBM PC and compatibles, the PC21 Indexer provides direct control of microstepping motor/drives and may also operate DC Servo amplifiers with full closed loop control. Providing its own 8085-based intelligent interface, the PC21 unburdens the IBM's $\mu$P. The PC21 Indexer assembles and stores up to 300 commands. Supporting motor positioning in absolute or incremental distance units, the PC21 will report the motor/drive's position on command in terms of motor steps or encoder steps. IBM PC-compatible software is supplied. Price is $795. **Compumotor**, Petaluma, CA **Circle 213**

## VME Wire Wrappable Panel



This VME Universal Panel has a 6U × 160 mm deep wire wrappable panel layout and four layer, true multilayer construction. With copper foil around each pin on all layers and plated through holes to equalize current flow throughout the power bus system, the component side $V_{cc}$ plane around each pin allows individual pins to be committed to $V_{cc}$ plane through the use of solder washers. ICs are spaced within a .100″ pitch. Price starts at $495. **Mupac**, Brockton, MA **Circle 157**

## X.25 Data Communications Board



Featuring the CCITT X.25 LAPB protocol, the WD4025 packet switching data communications controller board is designed to be compatible with the IBM PC, XT, AT and compatibles. The board features the WD2511 controller, the Telenet certified X.25 controller chip incorporating on-board data security using Western Digital's WD2001 encryption chip. The WD4025 will link computers at the same site or across the country via dial-up or leased lines or through a packet switching network. It will also provide a gateway connection for LAN. The board also includes automatic on-board buffering of data and flow control. The RS-232-C interface provides full-duplex transmission up to 19.9 Kbps. Price is $395. **Western Digital**, Irvine, CA **Circle 154**

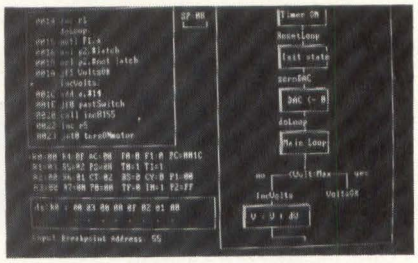
## Multibus-Based Peripheral Controllers

Two new multifunction single-board computers control peripheral storage devices in Multibus-based systems: the iSBC 214 board controls up to two 5¼″ Winchester disk drives compatible with the ST506/412 standard, up to four 5¼″ floppy disk drives, SA 450/460 compatible, and up to four ¼″ streaming tape drives, QIC-02 compatible. The board supports 20-bit or 24-bit addressing, has on-board diagnostics and error correcting circuitry. The iSBC 226 board controls up to two drives, compatible with the enhanced SMD interface, at transfer rates of up to 1.9 Mbytes/sec. It also contains on-board error correcting circuitry and diagnostics and is capable of 1:1 interleave. Price is $1,450 (iSBC 214) and $2,700 (iSBC 226). **Intel**, Santa Clara, CA **Circle 155**

# NEW PRODUCTS

## SOFTWARE

### 8048 Simulator/ Debugger For IBM PC



Designed to execute and debug machine codes for the 8048 family of microcomputers on the IBM PC, the Sim-8048 simulator/debugger displays the source code, register values, flags, I/O pins and program branches in windows. In addition to updating register contents, the flowgraph scrolls through the window as the program executes. Sim-8048 supports the timer-counter and external interrupts and the use of 8155 external RAM. Providing 50 commands consisting of single alphabetic keys or control characters, Sim-8048 displays both the source (symbolic) names and the numeric values. Price is $395. **Cybernetic Micro Systems**, San Gregorio, CA **Circle 201**

### Micro-To-Mainframe Communications Emulator

Emulating an IBM 3270 or RJE terminal in an SNA environment, the AdaptSNA/OEM micro-to-mainframe communications emulator is operating system independent. Written mostly in C language, the emulator is supplied with a Porting Guide. When operating in 3270 mode, AdaptSNA/OEM emulates an IBM 3270 PU Type 2, LU Type 2. The system then functions as an IBM 3274 controller with a 3278/9 terminal. Both the controller and terminal functions are performed by the emulator. Support is also provided for concurrent LU Type 1 and LU Type 3 direct print emulation, functioning as a 3286/7 printer. When operating in RJE mode, the software emulates an IBM 3770 or 8100 workstation, capable of operating in unattended mode. **NSA**, Irvine, CA **Circle 199**

### Design Verification System

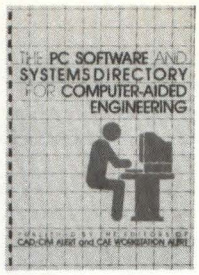
Supporting output to Versatec plotters, the NCA/Design Verification System (NCA/DVS) modular host software system verifies IC design. NCA/DVS includes Electrical Rules Check that checks electrical circuit designs against basic engineering principles, Design Rule Check that detects design rule violations, Networking Consistency Check that compares graphic design with schematic, Mask Data Preparation that translates graphic data to pattern generators and Electrical Parameter Checker that extracts circuit values from a layout. It links to Versatec plotting software for on-line, off-line or remote plotting. **Versatec**, Santa Clara, CA **Circle 200**

### SNA Subsystems

Allowing Prime systems to communicate with IBM hosts within IBM SNA-based networks, Prime/SNA runs on any 50 Series computer. Supporting both interactive and RJE subsystems on a single link, Prime/ SNA operates with Primnet networking software as well as operating concurrently with other Prime communications systems (RJE, DPTX). The package can suspend and recover multiple SNA terminal sessions without disconnecting from the IBM host. Interfacing to host communications network management software and conforming to IBM's network diagnostics and control procedures, Prime/ SNA uses ICS 2 Intelligent Communications Controller Subsystem and Prime Performer terminal (PT 200) to offload a Prime host. Price ranges from $5,500 to $6,000. **Prime Computer**, Natick, MA **Circle 204**

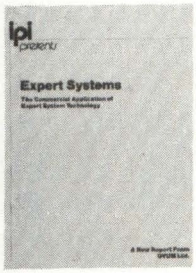
### Enhanced UNIX-Based Operating System

An enhanced version of the firm's UNIX-based operating system, ROS 3.2 includes networking, windows/mouse, graphics and development tools. Also introduced is the Ridge Local Area Networking. The software is derived from Berkeley's 4.2 TCP/IP implementation and includes file transfer capability and network configuration commands. The ROS 3.2 window and mouse manager software aides program development; users can simultaneously create several windows on the company's monochromatic bit-mapped display terminal. Ridge has also implemented the System V graphics package: ROS 3.2 implements System V, Release 2.0's job scheduling (cron) and a terminal information package. **Ridge Computers**, Santa Clara, CA **Circle 208**



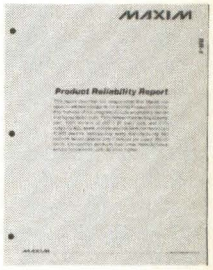

**PC Software and Systems Directory.** This 82-page book from Management Roundtable Inc. is to help design and engineering professionals choose CAD/CAM packages. Provided are listings of suppliers, software packages, applications, compatible hardware and prices. Also included is an analysis of trends and a market forecast.
**Management Roundtable** **Circle 259**

**Test and Instrumentation Products.** This 232-page catalog from Wavetek features its test and instrumentation products and accessories. Descriptions include specifications, prices and ordering information for generator and measurement equipment and components. Indexes and charts are also included.
**Wavetek** **Circle 252**



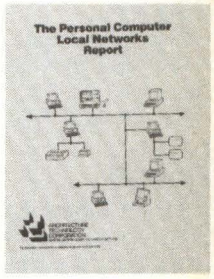

**Expert Systems Report**. This 380-page report from International Planning Information Inc. is a resource for firms producing and integrating computers, microcomputers, workstations and peripherals. Described are 185 expert system projects being carried out at 95 organizations. The report analyzes developments and provides forecasts of the industry.
**IPI** **Circle 260**

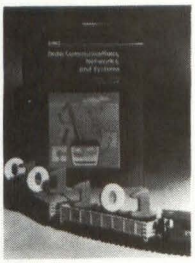
**Product Reliability Report.** This report from Maxim Integrated Products describes the steps that it has taken to set new standards for analog product reliability. Included are features of the program such as proprietary design and layout techniques, 100% temperature testing of parts, 100% burn-in at 150°C of parts and 0.1% outgoing AQL levels. Two appendices with tutorials are also contained.
**Maxim** **Circle 254**




**Fiber-Optic Newsletter.** This quarterly newsletter from Corning Glass Works is for its optical waveguide customers and end-users. It consolidates information on fiber-optic industry trends, application engineering, waveguide installations, business activities and case histories. It also contains efforts with fiber-optic component manufacturers, and describes available literature.
**Corning** **Circle 257**

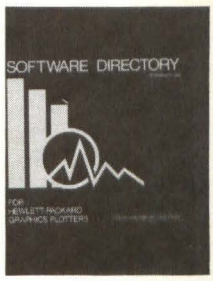
**Personal Computer LAN Report.** This 282-page report from Architecture Technology Corp. explains the ins and outs of PC LANs from wiring to protocols to servers to systems and specifies cautions to observe. Also included are tables of baseband and broadband PC LAN systems, followed by a listing of the vendors' addresses and phone numbers.
**Architecture Technolgy Corp.** **Circle 253**

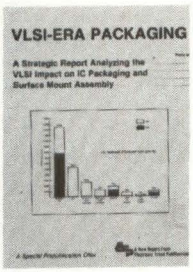


**Data Communications, Networks, and Systems Book.** This 368-page book from Howard W. Sams & Co. presents technical considerations involving contemporary data communications systems. Discussed are advantages and disadvantages of different approaches to LANs. Examined are strategies and techniques for error control, system security measures and forces shaping structure and regulations.
**Howard W. Sams & Co.** **Circle 258**

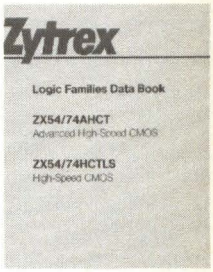
**Software Directory.** This 108-page directory from Hewlett-Packard describes 87 graphics software packages available for graphics plotters on both HP and non-HP computer systems. Products are listed in six application categories by name, vendor, application and computer system. Listings contain product descriptions, prices, operating system and memory requirements, model of supported HP plotter, and information about vendor support.
**Hewlett-Packard** **Circle 250**

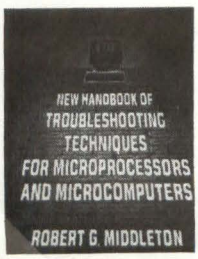



**VLSI Era Packaging Report**. This 200-page report from Electronic Trend Publications analyzes the VLSI impact on IC packaging and surface mount assembly. Covered is the impact of packaging trends and survival strategies for electronic equipment manufacturers. Also supplied are vendor profiles for assembly equipment, I/C package, IC handlers/testers and socket manufacturers.
**Electronic Trend** **Circle 256**

**Logic Families Data Book.** This 408-page manual from Zytrex Corp. provides information on its ZX54/74AHCT advanced high-speed CMOS logic and ZX547HCTLS high-speed CMOS logic families. Details on parameter measurement information, family descriptions, enchancement programs, reliability, ordering information and package dimensions are included as well as 120 data sheets.
**Zytrex** **Circle 251**




**Troubleshooting Techniques for Microprocessors/Microcomputers.** This 293-page book from Prentice-Hall describes microprocessors and microcomputers from the elementary to the sophisticated. Provided are explanations of how to troubleshoot them and to recognize malfunction symptoms in defective equipment. Included are illustrations, block diagrams, charts, troubleshooting flowcharts, circuit arrangements plus projects and experiments.
**Prentice-Hall** **Circle 255**

**Power Semiconductors Databook.** This product guide and specification databook for power semiconductors from International Rectifier Corp. is prefaced with a Jedec Alphanumeric index. Other sections include information on standard/custom assemblies, a brief listing of Hexfet power Mosfets by package type and a product digest of Crydom Division's solid state relays, microprocessor input/output modules and advanced products.
**International Rectifier** **Circle 261**

# CALENDAR

**April 16-18**

**ATE Northwest Conference And Exposition.** San Mateo, CA. Contact: Morgan-Grampian Exposition Group, 1050 Commonwealth Ave., Boston, MA 02215. (617) 232-EXPO.

**April 30-May 3**

**Implementing Local Area Networks.** Washington, DC. (Also in Palo Alto, CA; May 21-24.) Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA 90045. (213) 417-8888.

**May 1-2**

**Artificial Intelligence Conference And Exhibition.** Long Beach, CA. Contact: Tower Conference Management Co., 331 W. Wesley St., Wheaton, IL 60187. (312) 668-8100.

**May 2-3**

**Micro Mainframe Links.** Washington, DC. Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

**May 6-9**

**COMDEX/Spring.** Atlanta, GA. Contact: The Interface Group Inc., 300 First Ave., Needham, MA 02194. (617) 449-6600.

**May 8-9**

**Midwest Electronics Show.** St. Paul, MN. Contact: LST, Inc., 7900 W. 78th St., Suite 105, Edina, MN 55435. (612) 944-3539.

**May 14-15**

**California Computer Show.** Palo Alto, CA. Contact: Norm De Nardi Enterprises, 289 S. San Antonio Rd., #204, Los Altos, CA 94022. (415) 941-8440.

**May 14-17**

**Designing Custom And Gate Array VLSI.** Ottawa, Canada. Contact: Ruth Dordick, Integrated Computer Systems, PO Box 45405, Los Angeles, CA. 90045. (213) 417-8888.

**May 15-17**

**Network Communication Protocols.** Palo Alto, CA. (Also in Boston, MA, May 29-31.) Contact: Center for Advanced Professional Education, 1820 E. Garry St., Suite 110, Santa Ana, CA 92705. (714) 261-0240.

**May 20-21**

**Data Communications And Networking For The IBM PC And Other Personal Computers.** Boston, MA. (Also in Los Angeles, CA, June 13-14.) Contact: Software Institute of America, Inc., 8 Windsor St., Andover, MA 01810. (617) 470-3880.

**May 20-22**

**Custom Integrated Circuits Conference.** Portland, OR. Contact: Conference Chairman, Sperry Computer Systems, PO Box 43525 MS Y11B1, St. Paul, MN 55164-0525. (612) 456-4130.

**May 21-22**

**Utilizing Computer Graphics.** Silver Spring, MD. Contact: Conference Chairman, National Bureau of Standards, c/o IEEE Computer Society, PO Box 639, Silver Spring, MD 20901. (301) 921-2431.

**May 22-24**

**Seminar On Future CAD/CAM Technologies.** Austin, TX. Contact: BJW Marketing Communications, Inc., Suite J-5, 13740 Research Blvd., Austin, TX 78750. (512) 258-9983.

**May 28-31**

**Dexpo South '85.** New Orleans, LA. Contact: Expoconsul International, Inc., 55 Princeton-Hightstown Rd., Princeton Junction, NJ 08550. (609) 799-1661.

**June 10-13**

**ATE East Conference And Exposition.** Contact: Morgan-Grampian Exposition Group, 1050 Commonwealth Ave., Boston, MA 02215. (617) 232-EXPO.

# ADVERTISER INDEX