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DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS DECEMBER 1985

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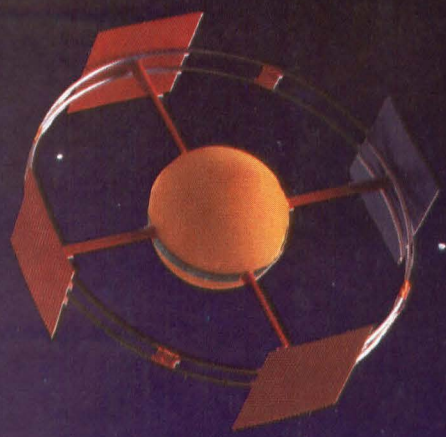
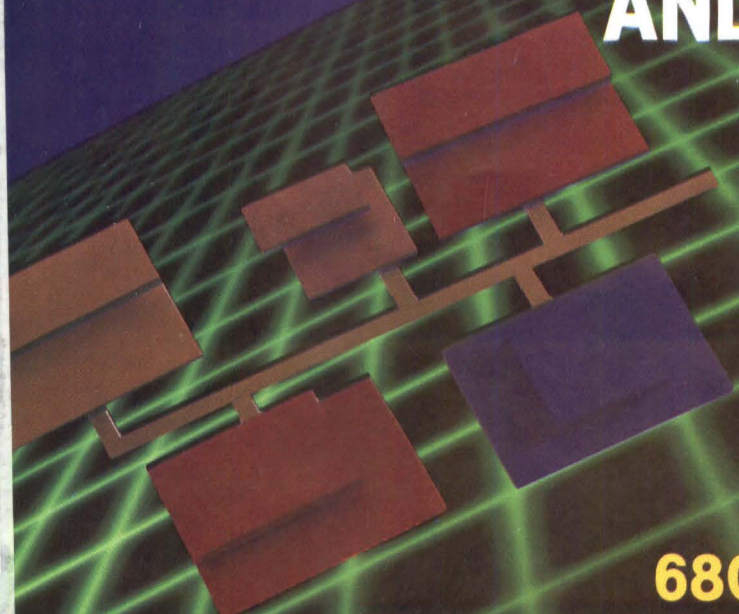


FLAT PANEL FUTURE FADES

COMMUNICATION NETWORKS AND PROTOCOLS



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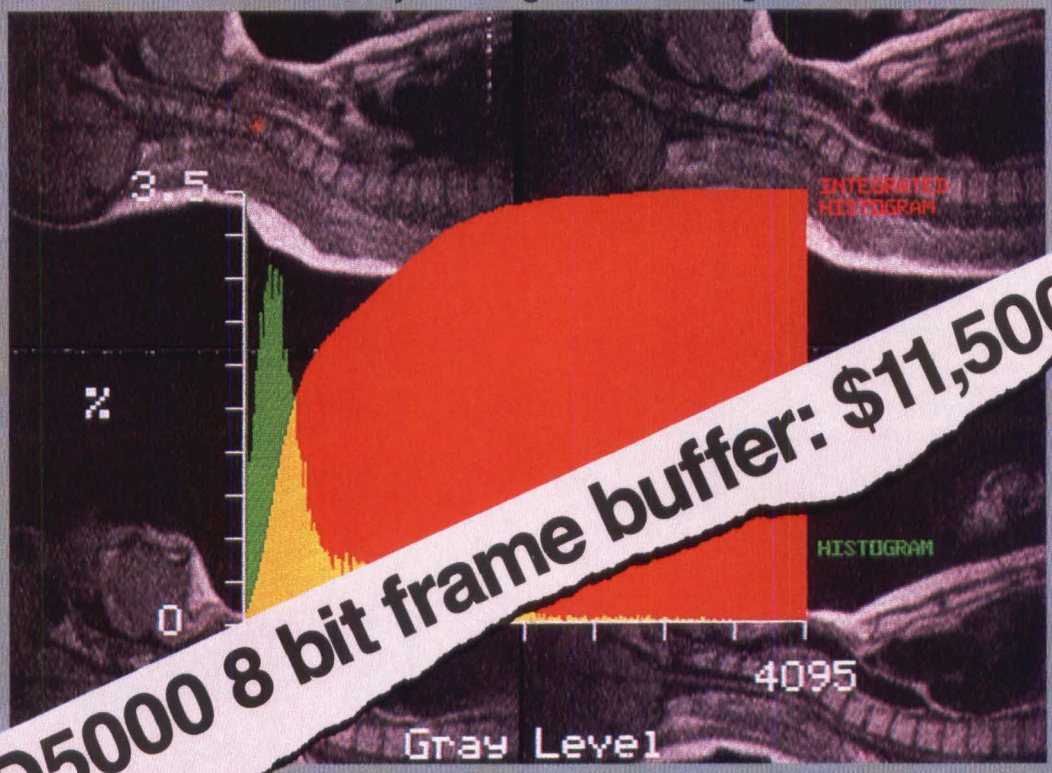

FD5000 8 bit frame buffer: $11,500.

Histogram of 12 bit magnetic resonance medical image with four (4) bit color overlay. Courtesy of Mallinckrodt, Institute of Radiology.

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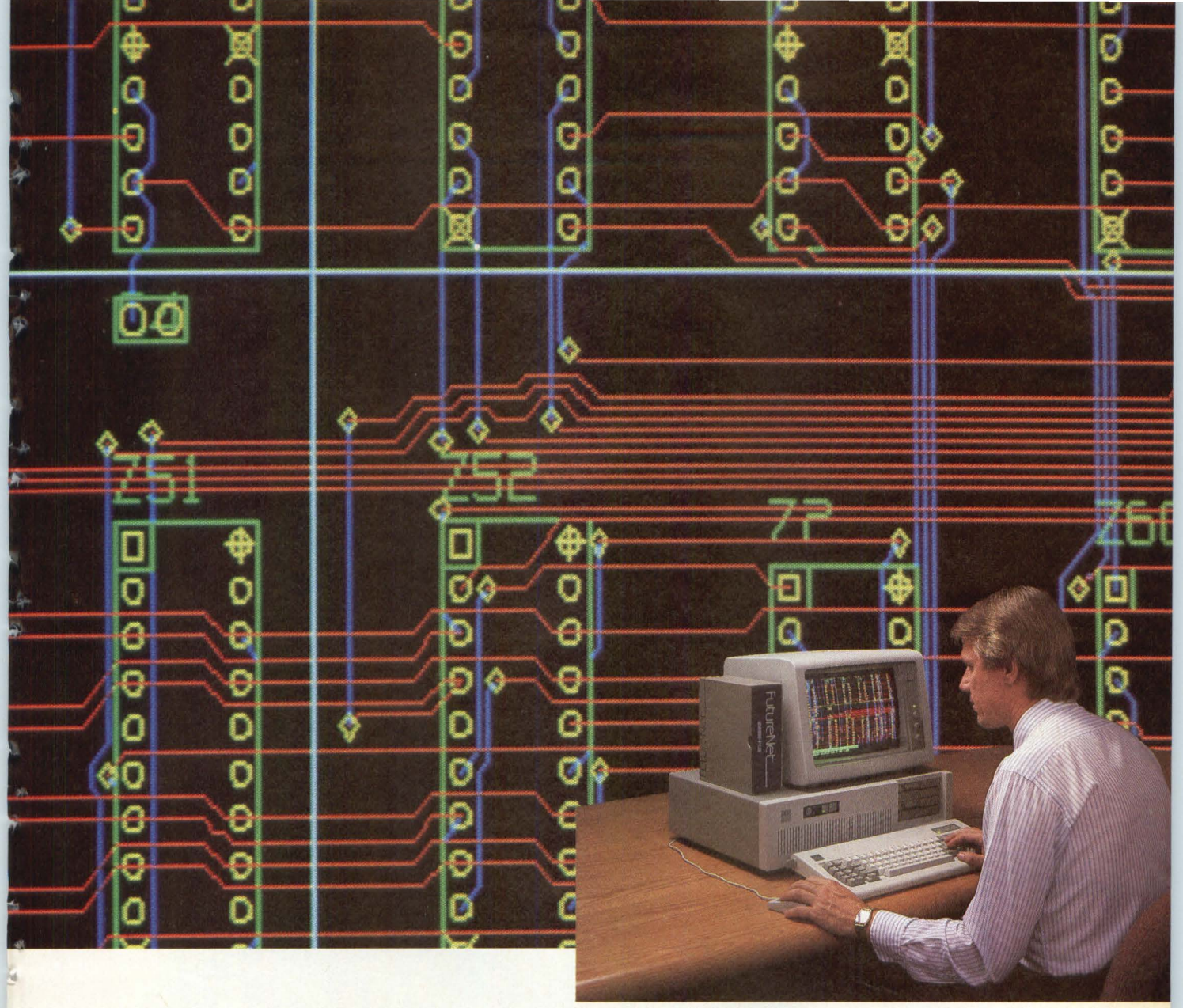

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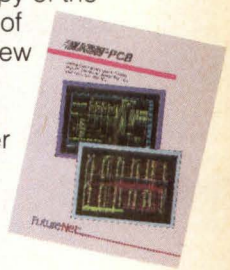

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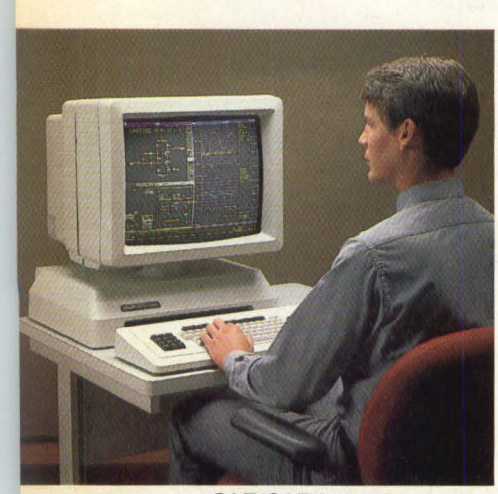

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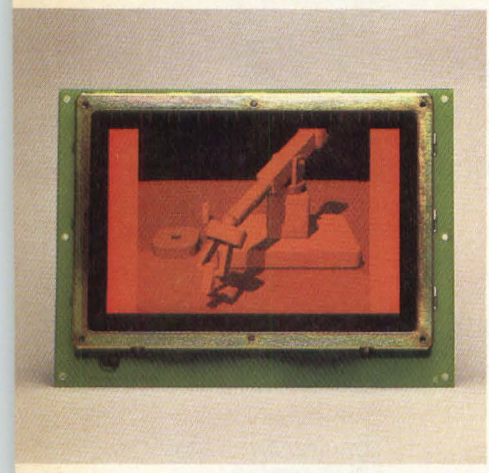

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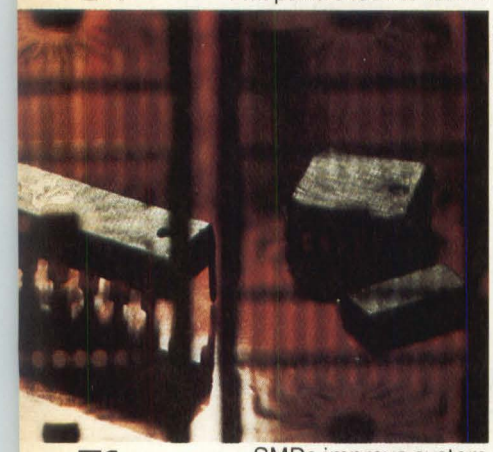

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ON THE COVER

Vendor-independent networking software that interconnects a wide variety of normally incompatible processors, operating systems and network interfaces is the aim of second-generation LANs. Fusion network software from Network Research Corp. provides virtual terminal capabilities, remote command execution, internet routing, high-speed, high-performance file transfer and interprocess communication across processor, operating system and LAN hardware boundaries. Fusion also provides network management support with Ethernet monitoring, network statistics, network and node testing. It offers users a choice of the two widely used LAN protocols — Xerox XNS and/or DARPA TCP/IP. Photo courtesy Network Research Corp.

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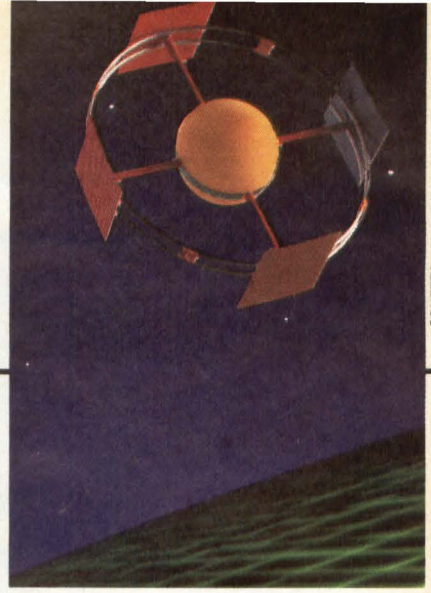
36 **Network Protocols**
The move toward standardization will advance LAN development.



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The hybrid ring can adapt to a variety of applications from backend networks, to a backbone LAN or to a distributed PBX.

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To get the highest system-level performance from advanced bipolar logic, designers should consider not only the device itself, but also the device's packaging.

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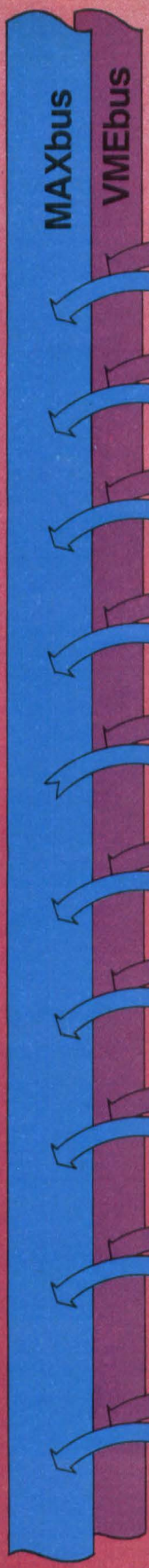

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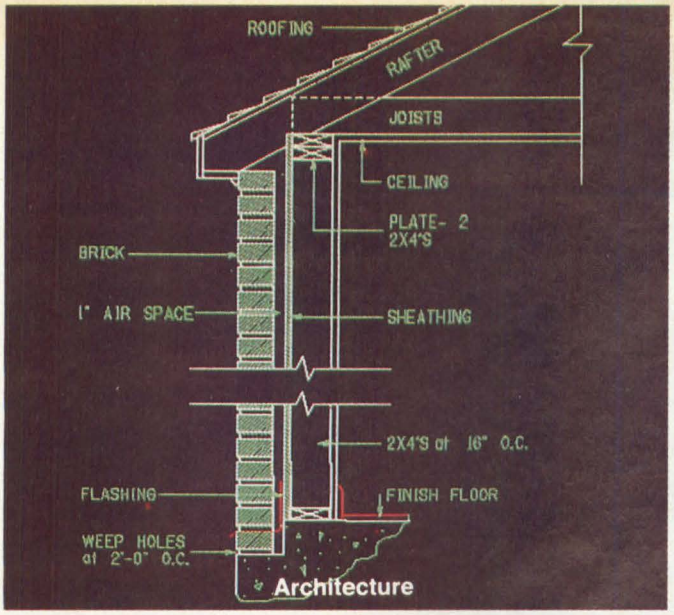

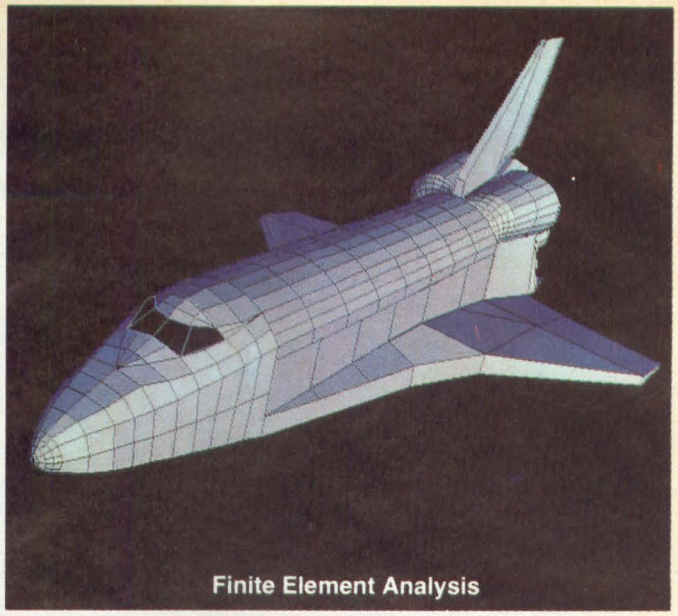

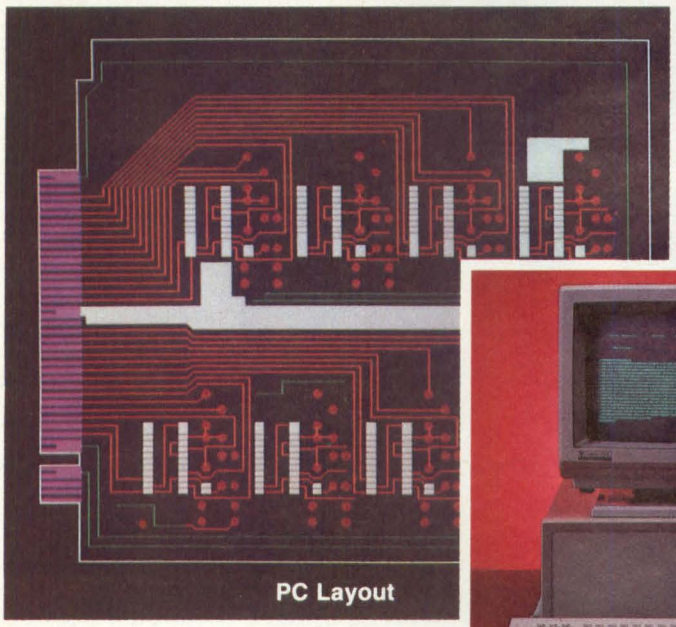

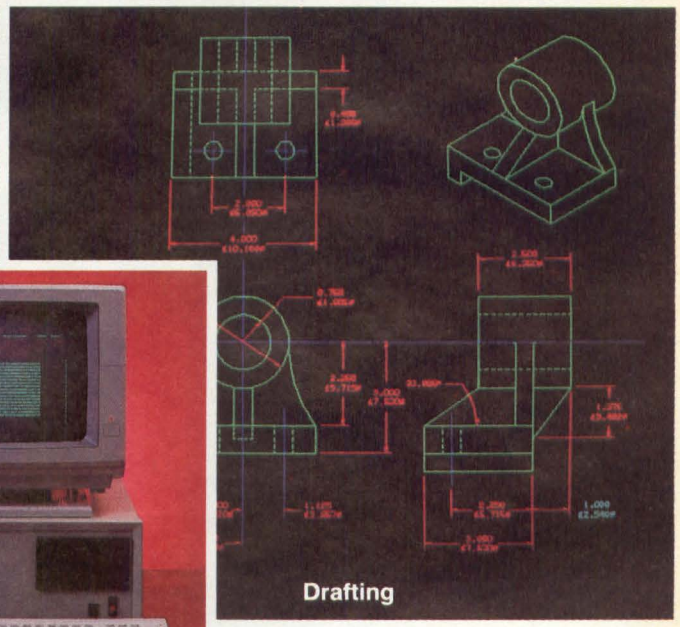

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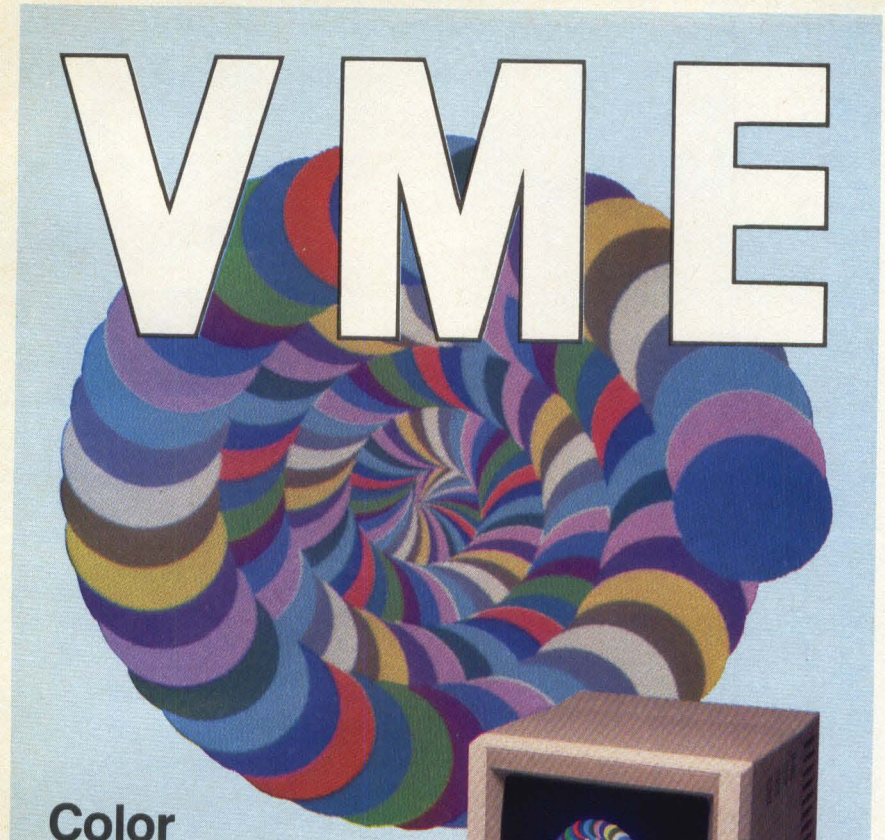

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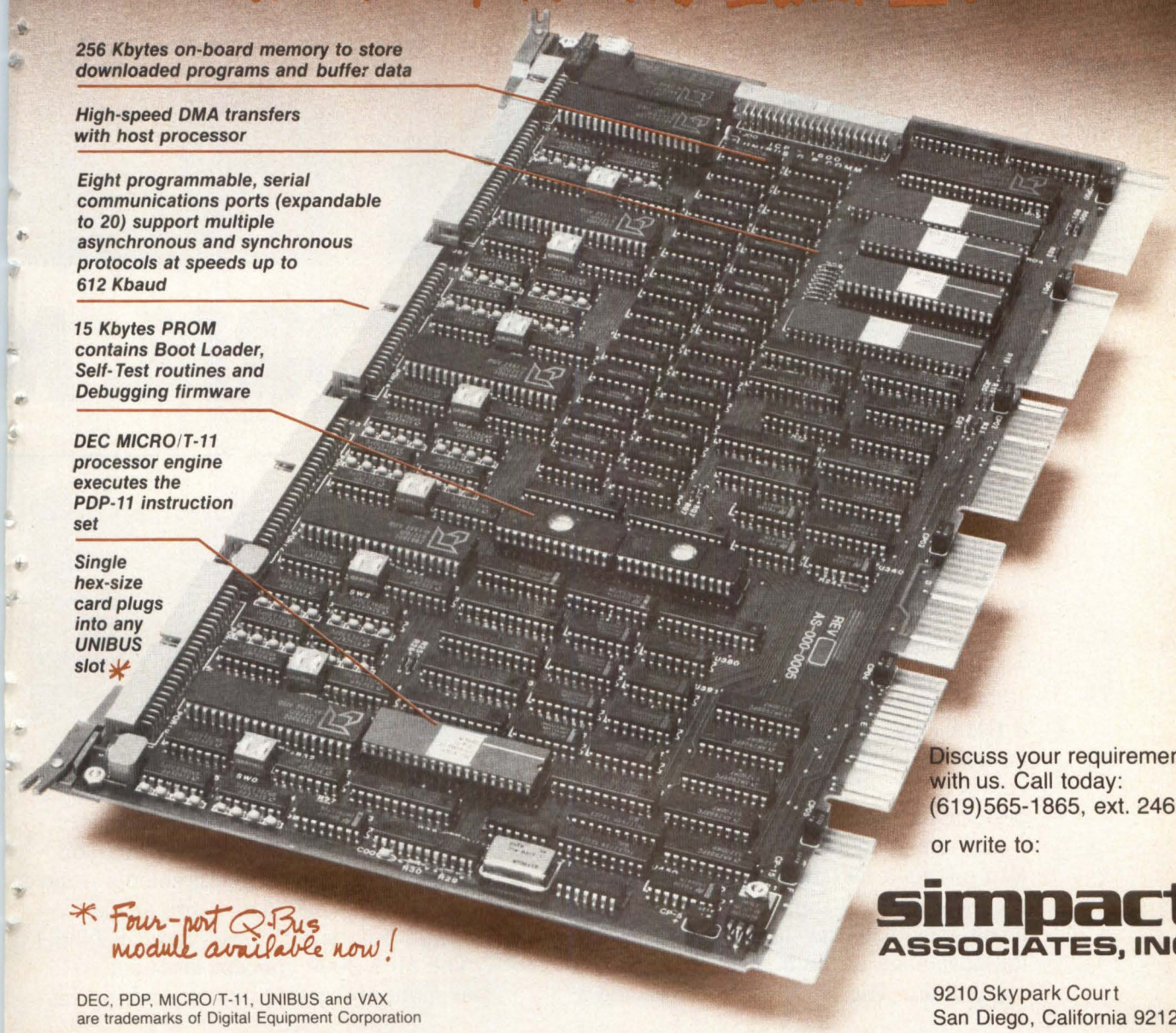

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Circle 32

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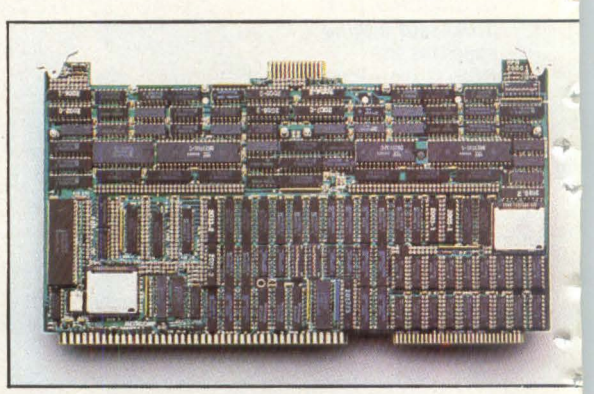
The best ideas are simple. And it simply makes good sense to build one good idea on top of another.

Take, for example, the MPA-2000. We started with this basic idea: Design the best Multibus CPU/Intelligent I/O processor possible. One with an 8 MHz iAPX-186 microprocessor...512 Kbytes of zero wait state dynamic RAM...256 Kbytes EPROM... 8 DMA channels to support I/O...and an optional 8 MHz 8087 numeric coprocessor...plus many other high performance features.

But our good idea didn't end there. We also provided two plug-in module sites on the MPA-2000 to support a family of I/O adapter modules specially designed to take full advantage of the board's superior capabilities. The MPX modules provide a



wide range of data communications, local area networking and disk I/O interfaces. Quite simply, you can choose a solution tailored to your exact requirements — no more tradeoffs associated with single-function boards with restricted capabilities.

The MPA-2000 concept gives you maximum processing power. And it gives

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you significant flexibility in I/O enhancements when you select one or two MPX plug-in modules. Choose for instance...

...**16 channels of full-duplex DMA serial I/O.** With the MPX-2000-160, eight 8530 devices provide ASYNC, BISYNC and BITSYNC protocols.

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There's the MPX-2000-510 **Ethernet I/O adapter module** with the 82586 coprocessor. Put it aboard the MPA-2000 to support LAN communications including the IEEE 802.3 Ethernet standard.

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The superior capabilities of the MPA-2000. The flexibility of its MPX family of plug-in modules. It all adds up to a simple solution. Modular by design.

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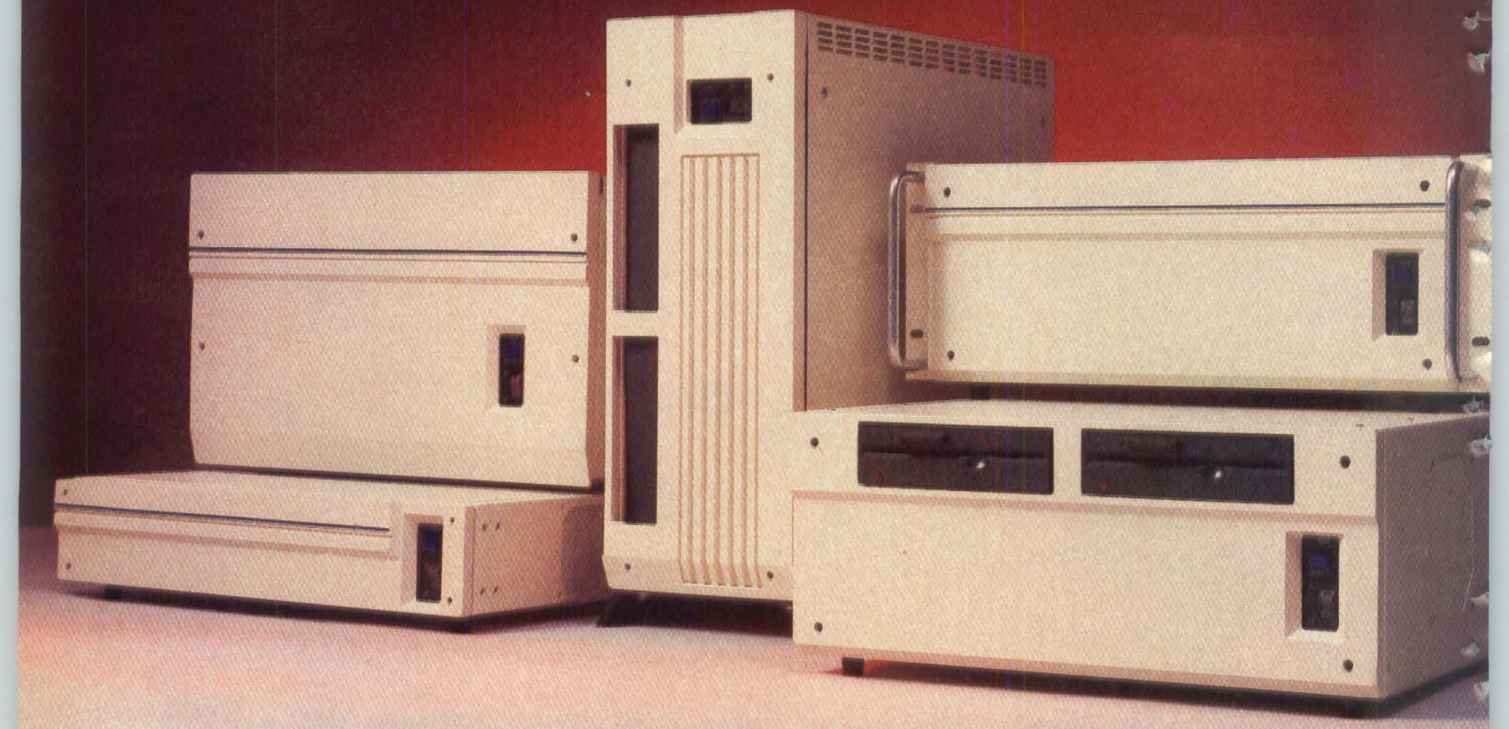

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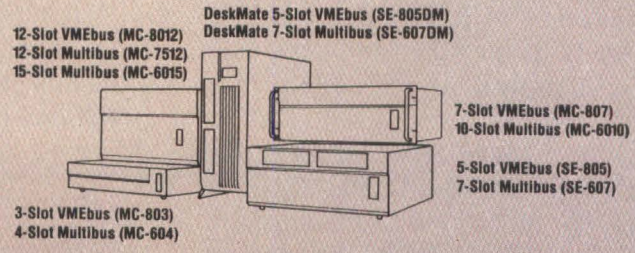

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Circle 20

EDITOR'S COMMENT

Exclusive!

Magazines devoted to the technical enlightenment of design engineers often run so-called exclusive feature articles. These exclusive articles are placed with the agreement that no other information on the subject will appear in print before the article is published. Trade magazine editors run exclusives because they make their magazines appear timely, even though the articles are prepared months in advance by the contributing companies. Editors enjoy this practice as do the firms who get to expound on the wonders of their technology. The audience may even find the article of some use although most could care less where they read it. Was it *ED*, *EDN*, *CD*, *DD* or somewhere else? It only becomes important if you want to go back and clip the article or look up something. So competition for exclusives is in most cases a harmless conceit of trade magazine editors – a bit silly perhaps, but harmless.

Consequently, most magazines have a more or less balanced attitude toward exclusives. We like them but wouldn't kill for them. There is an exception, however. One of the major design magazines (let's call it *Crazy-For-Exclusives Design* or *CFED*) has a policy to continually demand exclusives. *CFED* uses a not-so-subtle threat to restrict coverage of the topic or at least to downgrade its importance if it is not given to them on an exclusive basis.

Such bullying of PR agencies and companies by *CFED* does not serve the needs of either design engineers or industry. It is time that the industry realized that such practices have nothing to do with responsible journalism and refuse to make exclusive deals with any magazine that uses such tactics. Companies such as IBM and DEC learned this lesson years ago and try to keep the wraps on a new product until they are ready to announce it to the whole world.

Some of this tight-lipped approach is generated by fear of violating SEC insider rules if the announcement is expected to materially affect stock prices. More commonly, it is prompted by the desire not to impact the sales of present product lines before the new product is available in volume. In addition, early release of information may expose the company, especially if it is a large and major player, to restraint of trade charges.

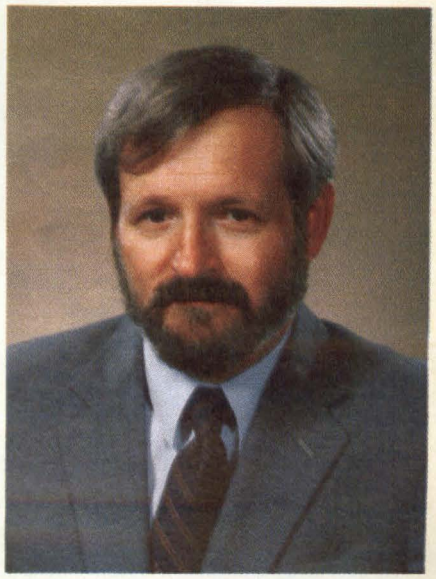
Nonetheless, there are often compelling reasons to write an article exclusively for one magazine. For example, if the product is one that is not expected to generate a great deal of excitement in the press, then an exclusive may be the best deal a company can get. From the reader's viewpoint, that may be the worst type of article. The magazine may accept it only because it is exclusive and not because of technical merit.

On the other hand, an exclusive, in-depth article published after a general press announcement may be best for both the reader and the company. The reader gets to read about the product in broad outline in the weekly industry newspapers and gets the technical details in the article.

In addition to contributed, exclusive feature length articles, there are also news exclusives, written by the magazine staff. These should result from superior reporting – because an editor discovered something before other publications become aware of it. Sometimes this may lead to an exclusive article because the company wants the chance to explain their technology at a time of their own choosing. Unfortunately, exclusive news is often the result of the magazine's editors demanding that the information not be given to any other publication. That's not journalism – it's news manipulation and our old friend *CFED* is at the forefront of such questionable practice.

The company or PR agency that tries to manage their press relations through the use of exclusive announcements certainly has that right. Publications that demand exclusives have no such right and the industry should stand up to them.

– John Bond, Editor in Chief



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Prop. Delay Time (typ) GATE (C_L = 15pF)	8ns	9ns	15ns	125ns
Max. Clock Freq. (typ) J/K F•F (C_L = 15pF)	60MHz	45MHz	20MHz	2MHz
Quiescent Power Diss. (typ) (GATE)	0.01 μW	8mW	0.01 μW	0.01 μW
Noise Margin $V_{IH(min)}/V_{IL(max)}$	3.5V/1.5V	2.0V/0.8V	4.0V/1.0V	3.5V/1.5V
Output Current $I_{IOH}I(min)/I_{OL}$ (min)	4mA/4mA	0.4mA/4mA	0.36mA/ 0.8mA	0.12mA/ 0.36mA
Op. Volt. Range	2-6V	4.75-5.25V	2-8V	3-18V
Op. Temp. Range	–40-85°C	0-70°C	–40-85°C	–40-85°C

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Circle 8

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HOTLINE

CMOS GRAPHICS SYSTEM PROCESSOR—By mid-1986, expect TI (Dallas, TX) to sample a 32-bit, 6-MIPS graphics processor with instruction cache, CRT controller, DRAM, VRAM and host interface. The 1.5-μm CMOS part will hold about 200,000 transistors.

IMAGE PROCESSORS GO ON-CHIP—ISSCC in February will showcase several image processing ICs. Matsushita will unveil a microprogrammable real-time image processor done in bipolar technology, while Siemens will describe a 2D digital video filter. Mitsubishi will announce a processor for decoding composite TV into two DSP ICs—with the DSP chips allowing conversion of composite video into luminance and chrominance (and vice versa). And, Toshiba will show a 20-MHz, 32-bit pipelined CMOS image processor capable of performing a 1024-point complex FFT in 1 msec.

ISSCC TO FOCUS ON DSP—National Semiconductor, Signetics/Philips and NEC will preview single-chip DSPs at ISSCC. The Signetics part contains two 16-bit data buses, executes a 40-bit instruction set and supports up to six concurrent arithmetic and data-move operations in each instruction. The NEC part has a 32-bit floating point multiplier and 55-bit floating point ALU. The 25,000-transistor National part, targeted at motor control, will boast 0.5- to 1.5-μsec instruction cycle time.

TOUCH SCREEN USES SOUND—Surface acoustic wave technology is at the heart of a touch screen system from Zenith (Glenview, IL). Exhibited at WESCON, it offers crosspoints in three dimensions. Fewer parts should mean lower cost versus competing technologies.

BIT-SLICE GaAs—A technology exchange agreement between AMD (Santa Clara, CA) and Vitesse Electronics (Camarillo, CA) will produce GaAs equivalents of the 2900 bit-slice family. First members, which include a 4-bit-slice processor and a look-ahead carry generator—are scheduled for sampling in mid-1986.

PARALLEL PACTS—Vendors of little mainframes, or "Crayettes", are forming alliances with CAE vendors. Alliant Computer Systems (Acton, MA) and Apollo (Chelmsford, MA) inked a pact that will see Alliant's FX/1 and FX/8 perform as servers on the Apollo DOMAIN. Meanwhile, Culler Scientific Systems (Santa Barbara, CA) and Sun Microsystems (Mountain View, CA) have announced a cooperative marketing effort.

PARITY BEGINS AT HOME—Zilog Systems Div. (Cupertino, CA) has bypassed the Z80000 32-bit microprocessor for its upcoming System 8000/32 UNIX-based computers. Citing time-to-market demands, the division has selected the WE32100 chip from AT&T. Meanwhile, the Z80000 is still scheduled for sampling in early '86.

NON-VON NEUMANN DEBUGGING—Sequent Computer Systems (Beaverton, OR) has announced software that bolsters its 32032-based Balance computer family. A notable enhancement is a parallel debugger which lets the programmer stop and examine individual or multiple processes. Known as PDBX, it works with Fortran, C and Pascal.

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LEX 90's exclusive Virtual Windows functionality allows real-time *color* window management of up to eight user-defined windows.

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Every model in the LEX 90 family has the same basic components which use the latest bit-slice technology for rapid execution of complex graphics calculations.

And the family's flexible and compatible hardware/software architectures have been designed to accommodate growth. So you'll never have to sacrifice your initial investment should you decide to enhance your LEX 90 system's performance. And what performance!

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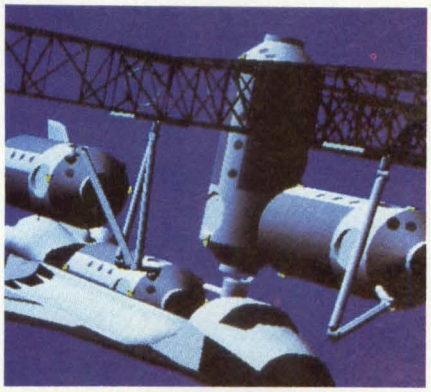
Exclusive SimulRes functionality allows simultaneous display of 640x512 and 1280x1024 images on the same screen. And where you need high performance with high resolution, there's a LEX 90 model that can support up to eight planes of 1280x1024 display memory at 60Hz non-interlaced refresh.

Intelligent List Language functionality enables enhanced local display list management. The extraordinary solid modeling display capability of our patented SOLIDVIEW® technology is available. And for oil applications, there's GEOVIEW,™ a three-dimensional surface modeling package for geological interpretation.



This space station model, courtesy of Martin Marietta, was created with Lexidata's SOLIDVIEW display technology, and GEOMOD™ application software from SDRC.

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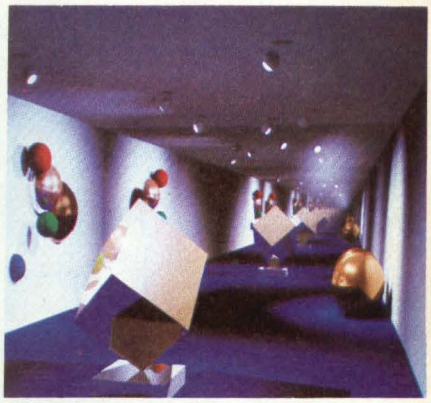

This gallery "exhibits" LEX 90's true color capability and appears courtesy of Cornell University's Program of Computer Graphics.

For a good look at the LEX 90 family and its expanding capabilities, call us at 1-800-472-4747. In Massachusetts, call 617-663-8550. Or write Lexidata Corporation, 755 Middlesex Turnpike, Billerica, Massachusetts USA 01865. TWX: 710-347-1574.

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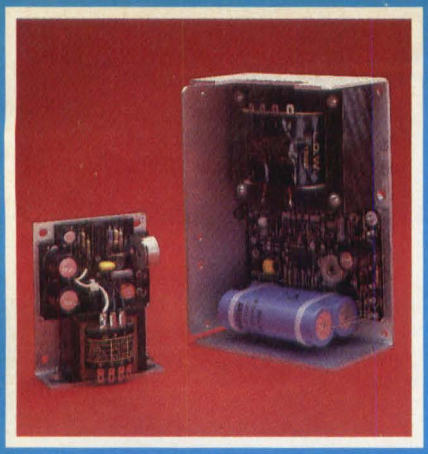

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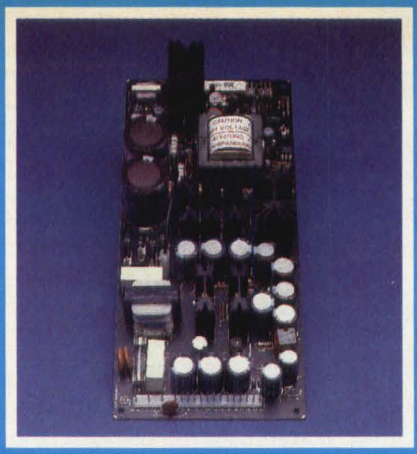

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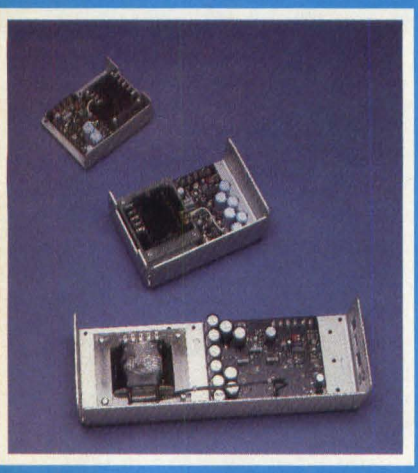

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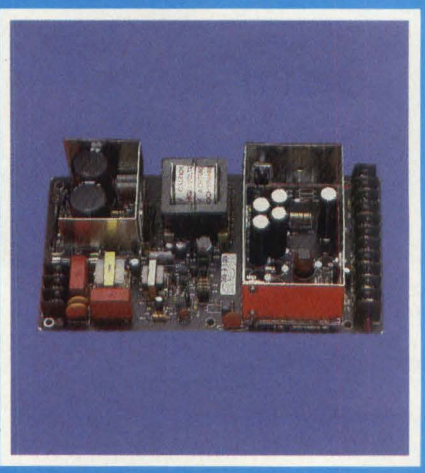

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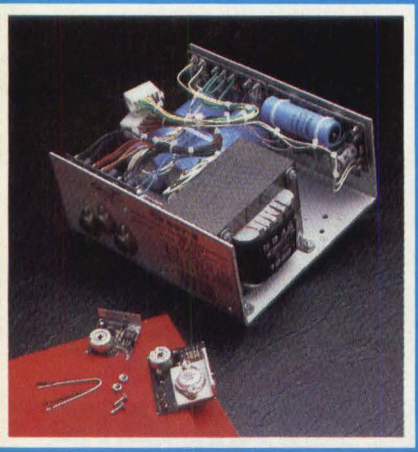

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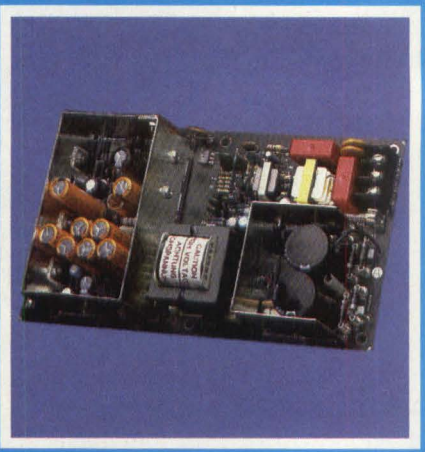

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CAE/CAD Industry Accelerates Toward Maturity

Figure 1: DEC's MicroVAX II is rapidly becoming a workstation standard. Daisy has combined a MicroVAX II workstation with its Logician software and a PC/AT graphics interface. Shown is the resulting Logician VX, available in the first quarter of 1986.

As the CAE/CAD industry matures, many product introductions serve to round out product lines. Although the recent Automated Design and Engineering for Electronics (ADEE) show in Boston held few surprises, the products that were introduced fill some important gaps in vendors' lines. Most noteworthy, however, were announcements of support for DEC's MicroVAX II, which looks like a machine that will significantly impact the CAE/CAD industry.

Until now, standard CAE/CAD workstation platforms came from a variety of vendors such as Apollo (Chelmsford, MA), Sun Microsystems (Mountain View, CA) and IBM. But many companies do not consider such products to be standard machines. Although IBM's personal computer certainly fits the definition, it lacks the horsepower of a full 32-bit computer. Viewed in this light, the CAE/CAD user has been without a standard platform. Because many potential workstation buyers desire a true standard platform, several CAE/CAD vendors are either abandoning or complementing their proprietary machines in favor of the MicroVAX II.

Surprisingly, Daisy Systems (Mountain View, CA) changed its course by announcing a two-year, $50 million OEM MicroVAX II agreement with DEC. Under the agreement, Daisy purchases MicroVAX IIs and equips them with its Logician CAE/CAD software and a PC/AT graphics interface. The resulting Logician VX (**Figure 1**) workstation sells for $90,000 and will be available in the first quarter of 1986. Daisy's shift from proprietary hardware eliminates a primary criticism of the Logician. Others joining Daisy's MicroVAX II strategy include Tektronix/CAE (Santa Clara, CA), Case Technology (Menlo Park, CA), Phoenix Data Systems (Mountain View, CA), FutureNet (Chatsworth, CA) and Valid Logic (San Jose, CA). Since Valid's Scald software already ran on VAX computers, the port to the MicroVAX II is relatively easy.

On the other hand, Cadnetix (Boulder, CO) chose the 68020 (running UNIX) as a platform. The company announced a family of seven 68020-based workstations: three monochrome systems and four color machines. On the monochrome side, the CDX-9100S ($30,500) is a basic schematic capture system whereas the CDX-9150S ($33,500) includes an additional virtual logic analyzer and a special graphics editor for analyzing simulation data. The CDX-9200S ($39,500) is identical to the 9150S except that it includes the Cadat logic simulator from HHB Systems (Mahwah, NJ). In the color domain, the CDX-50000S ($82,900) is a high-performance graphics CAD system supporting both PC board layout and schematic capture.

Another 68020-based workstation from Cadnetix, the CDX-59000S ($96,900), handles schematic capture, logic simulation and PC board layout (**Figure 2**). Rounding out the family is the CDX-9300S ($59,000) and CDX-5900S ($71,400). Both perform schematic capture, logic simulation, logic analysis and custom postprocessing. However, the 5900S also handles automated PC board layout and manufacturing postprocessing.

At a time when proprietary hardware is on the decline, Buck Henry, Cadnetix's vice president of marketing defends the firm's strategy. "Standard platforms are excellent general purpose systems," says Henry, "but they do not deliver the performance found in a dedicated machine." For users, the trade-off is between exceptionally high performance or a more standardized design environment.

Following the recent unveiling of Intel's (Santa Clara, CA) 80386, both Daisy and Valid announced simulation support for the processor on the Physical Modeling Extension and Realchip hardware modeler, respectively. Daisy also introduced MegaFault, a high-performance fault simulator for the firm's Megalogician. MegaFault, priced at $45,000, uses a concurrent fault simulation algorithm and the same simulation models as those in the Megalogician.

Traditional fault simulation algorithms, such as those used by MegaFault, Calma's (Austin, TX) Tegas and GenRad's (Santa Clara, CA) Hilo, fault each node in the circuit and then determine whether the test vectors detect the fault. Faulting each node is a time-consuming task that often demands excessive processing power. However, Caedent (Colorado Springs, CO) takes a different approach to beat the problem. Instead of actually faulting the nodes, the company offers a probabilistic fault grading (PFG)

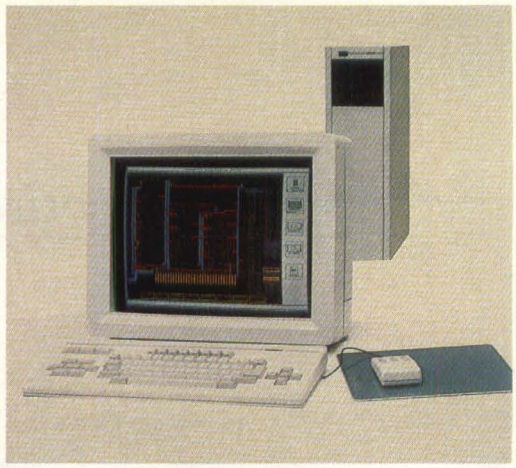

Figure 2: Cadnetix launched several 68020-based UNIX workstations at the recent ADEE show. Shown is the CDX-59000S, a CAE/CAD system handling schematic capture, logic simulation and automatic PC board layout. Also included is a virtual logic analyzer and graphics accelerator.

tool that statistically determines the percentage of faults detected by a set of test vectors. PFG reportedly yields results very close to those of traditional methods without the long run times.

Along a similar vein, Silicon Solutions (Menlo Park, CA) announced the Mach 100, a second hardware accelerator in its family of logic and fault simulation engines. Mach 100 executes 250,000 events per second and has a capacity of 32,000 modeling elements.

High accelerator prices have been a major deterrent to many potential buyers. Until recently, accelerator prices ranged from $200,000 to several million dollars. But both Silicon Solutions' Mach 100 and Zycad's (St. Paul, MN) Sprintor represent systems in the $20,000 to $30,000 range. Sprintor (available only on an OEM basis) offers slightly lower performance and capacity than the Mach 100, but it costs $5,000 less than the Silicon Solutions machine.

At ADEE, Zycad introduced Eventlink, an option for its Logic Evaluator (LE) and Expeditor simulation engines that allows them to interactively exchange event data with other systems. According to Nicholas Van Brunt, leader of the company's R&D group, "Eventlink gives users of the LE and Expeditor the potential to link one of the simulation engines to almost any event-generating CAE tool or peripheral. They can operate concurrently with external physical and behavioral models as well as share a Zycad simulation engine interactively between design teams." Users, however, must write the software to support such an interface.

Both Daisy and Valid have begun to address the analog designer's needs. Daisy's recently-formed Analog Design Automation Division unveiled the ChipSIM MOS simulator, which reportedly runs up to 20 times faster than Spice. ChipSIM was developed under an agreement with Shiva Multisystems (Menlo Park, CA), a firm specializing in analog simulation. In addition, Daisy introduced the Daisy Parameter Extraction Program (DPAX) and the Analog Device Library Builder (ADLiB). DPAX takes actual device parameters from test wafers and feeds the data into the analog simulator's models. This ensures that the simulator uses the most accurate device modeling parameters. ADLiB permits designers to construct their own models for inclusion in the analog simulator's library.

Although Valid and Daisy products compete with each other on most levels, Valid's recent analog offering is more in line with the software from Analog Design Tools (ADT) (Menlo Park, CA). In addition to Spice, Valid's Analog Designer includes a digital voltmeter, an oscilloscope, a network analyzer and a function generator (**Figure 3**). The package is priced at $22,000, not including the Scaldsystem platform. ADT, however, offers the same kind of tools as Valid plus packages that perform spectrum analysis, Monte Carlo analysis and sensitivity analysis.

Figure 3: Expanding its product line to meet the analog designer's needs, Valid has introduced a workstation that includes a digital voltmeter, an oscilloscope, a network analyzer and a function generator.

Hewlett-Packard (Fort Collins, CO) also exhibited at the ADEE and is showing signs of commitment to the CAE/ CAD market. In addition to its own recently-announced CAE/CAD product offerings, the test equipment giant is teaming up with VLSI Technology (VTI) (San Jose, CA), SDA Systems (Santa Clara, CA) and Analog Design Tools. VTI announced that its IC design software product line will run on the HP 9000 Series 300 engineering workstations. HP will also market and distribute the products. Similar agreements were signed with SDA and Analog Design Tools.

VLSI Technology introduced its long-awaited standard cell library. Fabricated in 2-micron CMOS, the library consists of over 250 standard cells and is fully compatible with VTI's Megacells and silicon compilers. (VTI recently repositioned its cell compilers as silicon compilers.) Other newcomers to the standard cell market include Fujitsu (Santa Clara, CA) and Oki Semiconductor (Sunnyvale, CA). Fujitsu's standard cells have been available in Japan for several years, but the firm delayed its US debut. The library is based on the same 1.8-micron, two-layer metal, silicon-gate CMOS technology used in its gate arrays. Oki's standard cells also use this technology, but the firm offers both a 2-micron and 3-micron library.

Most CAE/CAD vendors attending the ADEE reported a leveling-off of sales, which stands in sharp contrast to the record revenues of 1984. Although the semiconductor slump is affecting the CAE/CAD sector, manufacturers are predicting an upturn.

—Collett

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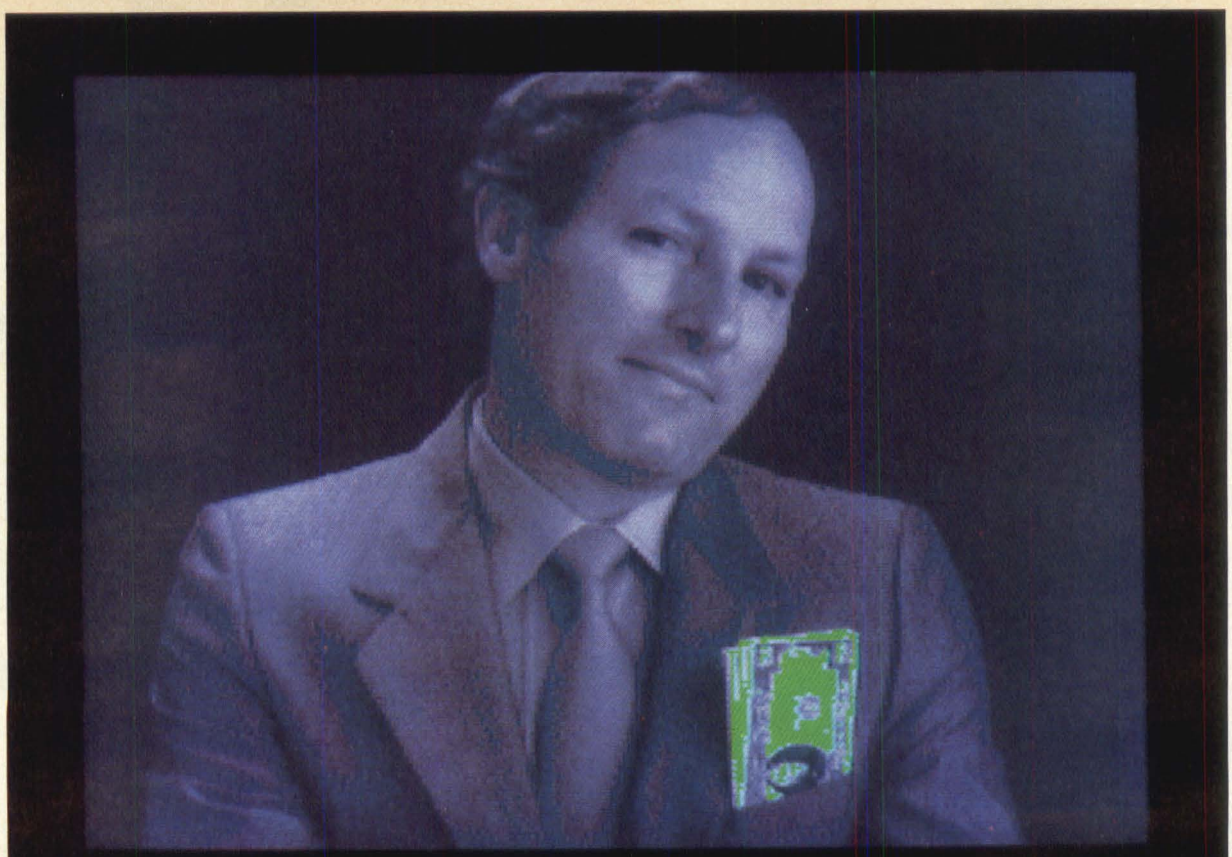

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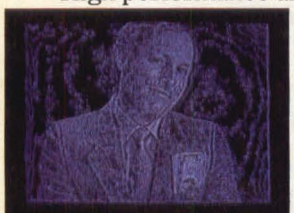

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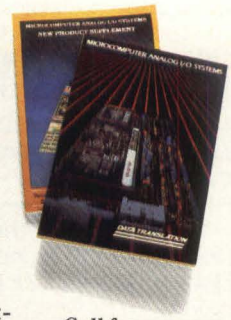

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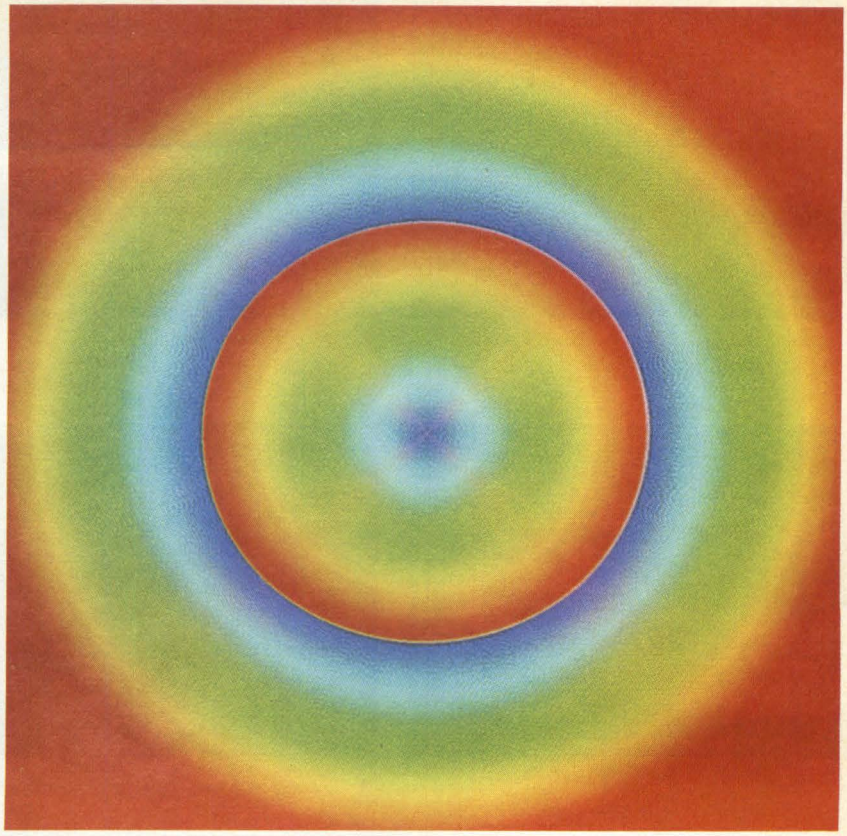
IMAGING

Optics Finds A Niche In Imaging



Combining three 8-bit DACs with 1 Mbyte of on-board memory allows the AGC-1024P graphics controller from Imagraph to simultaneously display 256 colors from a palette of 16.8 million.

Technologies such as fiber optics, optical disks, software and graphics have combined to produce unique electronic imaging products. Emerging from the exhibit halls of the recent Electronic Imaging '85 show in Boston, products were launched by a variety of companies seeking to gain a specific niche within the image processing market.

In CAD/CAM applications, for example, a major problem has been the relatively large expense associated with flatbed scanners (*Digital Design,* June 1985, p. 20). At Galileo Electro-Optics Corp. (Sturbridge, MA), this problem has been overcome with a product called Glasscan, which converts most pen plotters into image digitizers. By replacing the Gurtz pen holder with a fiber-optic sensor, systems integrators can digitize 4-bit-deep images into IBM PC/XT or AT systems. Costing between $3,000 and $4,000, Glasscan transfers images over a fiber-optic cable to a 256 × 1 linear charge coupled device from EG&G Reticon (Sunnyvale, CA) and digitizes the resulting signal across the IBM PC bus.

According to Brian Rhea of Galileo, the PC memory represents the only limitation to image size. The company is actively working with OEMs to develop interfaces for other computer systems including the MicroVAX II from DEC. In 1987, the company plans to announce a color version of Glasscan which will be able to digitize large size color drawings to 8-bits deep.

Image storage has also plagued imaging systems designers. Because of the large amounts of memory associated with image storage, system designers have been forced to consider new technologies such as optical disks. Aquidneck Data Corp. (Middleton, RI) has done much to address these problems with a line of IEEE controllers for the Gigadisc from Alcatel Thomson (Redondo Beach, CA).

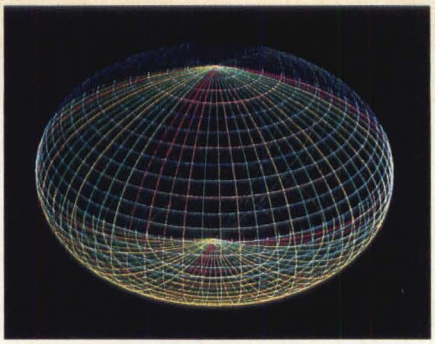
In operation, the optical archiving system that Aquidneck has developed appears to the host as a 9-track 1,600 bit/in. PE tape formatter. Thus, a single 1,000-Mbyte optical disk can hold the contents of 20 or more 2,400'-tapes, depending on the amount of data stored on each. The controller interfaces to any Pertec-type tape controller over two standard I/O cables and accepts all standard tape commands. A 12"-optical disk is employed. This is removable and has a data retention life of over 10 years. As an option, the controller can encrypt data saved to the optical disk to provide information security and access restrictions.

Addressing the imaging software problem is the goal of many of the hardware companies. For example, Data Translation (Marlboro, MA), has announced an agreement with Camtrel Computer Systems (Cambridge, England) to distribute Camtrel's PC Semper in the US. PC Semper, an image processing package for the IBM PC family, has been tailored for use with Data Translation's DT2803 frame grabber. Developed initially at Cambridge University, the software package is written entirely in Fortran-77 code, allowing users equipped with the IBM Fortran compiler to either develop image processing routines using callable routines or to develop novel routines not included in the package. According to Camtrel, the package can support full IEEE floating point representations of images on the PC. Camtrel is also working on an array processor which will speed up imaging functions by up to 180 times. At present, distribution agreements for the AP have not been signed in the US.

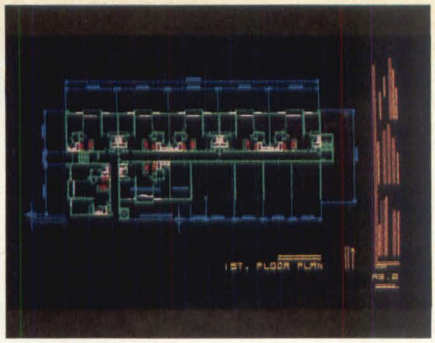
Combined imaging and graphics has become one of the most important goals in the electronic imaging field. As a step in this direction, start-up Imagraph (Woburn, MA) has announced its AGC-1024P advanced color graphics and imaging controller for the IBM PC/XT and AT. Although the board uses the Hitachi ACRTC graphics controller, as is used in many other graphics boards, it also supports 1 Mbyte of on-board memory and three 8-bit DACs. This allows it to display 1024 × 1024 × 8 images producing 256 colors from a palette of 16.8 million. According to Bob Wang, president of Imagraph, two of the most novel features of the design are the ability of the board to perform hardware clipping of images and its speed versus existing 7220 designs.

—A. Wilson

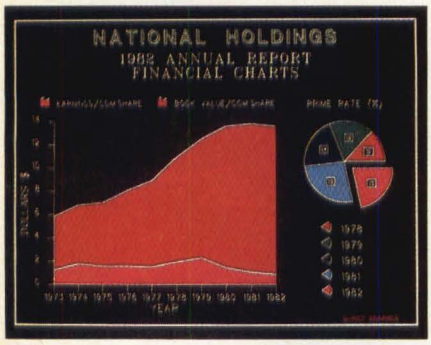
1. String Software™ from Geobased Systems, Inc., Raleigh, North Carolina



2. 3D sphere from Vectrix

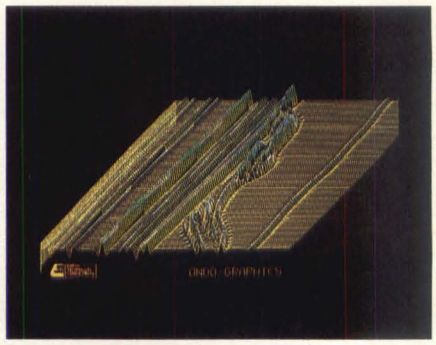


3. Created with VersaCAD™ software from T&W Systems, Inc., Huntington Beach, California



4. Business graphics created with D-PICT/B software from Dataplotting Services, Inc., Don Mills, Ontario, Canada

5. Courtesy of Wave Graphics, Cleveland, Ohio



6. Seismic traces displayed in isometric projection using Ondo-Graphics software from Earth Technology Consultants, Inc., Houston, Texas

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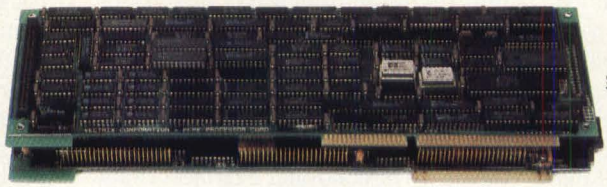

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UNIX And MS-DOS Merge

AT&T Information Systems (Morristown, NJ) will offer Multisystem Merge as OS Merge on its AT lookalike, the 6300 Plus, available in the first quarter of 1986. The ability to run MS-DOS and UNIX programs concurrently may solve the problem of information flow that now exists for PC-based CAE workstations.

The UNIX operating system has achieved the support of the engineering and scientific community, perhaps due to the amount of CAE software written for it. But the emergence of PC-based workstations has led to numerous CAD/CAE software packages for the MS-DOS operating system. Several CAD/CAE vendors have had to split certain aspects of the design process between the two operating systems. Schematic capture may be able to run under MS-DOS; on the other hand, fault simulation, because of its heavier computational requirements, is better accomplished under a multitasking operating system such as UNIX. According to Terry Zimmerman, vice president of marketing at FutureNet (Canoga Park, CA), the integration and free flow of data between systems is the primary problem for PC-based workstations.

Most implementations of multiple operating systems partition the system disk between the operating systems, necessitating file transfer utilities for file access. Will Herman, director of product engineering at Viewlogic (Marlboro, MA), indicates that despite available tools for CAE, the development cycle has been hampered by the need to convert file formats from the MS-DOS-based schematic to UNIX-based simulation.

Connector from Uniforum (Santa Monica, CA) was the first system to allow MS-DOS applications to run as tasks under UNIX. However, George Strong, vice president and chief financial officer of Uniforum, notes that Connector's limitation was in rewriting MS-DOS programs so that they could run in the 80286 protected mode for multitasking systems. As a result, a tradeoff existed between doing substantial software rewrites and limiting UNIX to a single user.

The announcement of Multisystem Merge from Locus Computing Corp. (Santa Monica, CA) enables 80286-based microcomputers to run both MS-DOS and UNIX applications concurrently while maintaining the multitasking features of UNIX. It is a wholly software solution. Since UNIX and MS-DOS share the same CPU, no rebooting of the computer is necessary.

Multisystem Merge divides system resources into low-level resources, such as the disk, CPU and system memory, and high-level resources, which include the file system and application programs. Both levels are transparently sharable between the two operating systems. Record-level sharing of files by MS-DOS and UNIX is provided. As a result, all MS-DOS applications can run as tasks without modification under UNIX on a 80286-based computer. Data files created under MS-DOS can be immediately used by a UNIX application; MS-DOS and UNIX programs can both be used to develop other software.

Nevertheless, the question of performance is still at issue for Multisystem Merge. How well does a 16-bit processor run UNIX? Several UNIX/coprocessor subsystems with on-board UNIX ports and 32-bit processors are currently available. These boards, for example the Opus516 Personal Mainframe from Opus Systems (Los Gatos, CA), still require that the computer be rebooted after an MS-DOS to UNIX file transfer in order to change operating systems.

At Wescon, FutureNet announced the DASH-CADAT Plus, a coprocessor board that includes a 32016 microprocessor to control the two operating systems. A windowing environment buffers the user from having to know either UNIX or MS-DOS commands. The hardware approach to integrating operating systems differs from the software approach because either XT- or AT-compatibles can be configured to run UNIX. Multisystem Merge requires an AT-compatible. This fact may prove important with the large installed base of XT machines in the CAE arena.

—Meng

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ICs

Multiplier/Accumulator Manufacturers Multiply

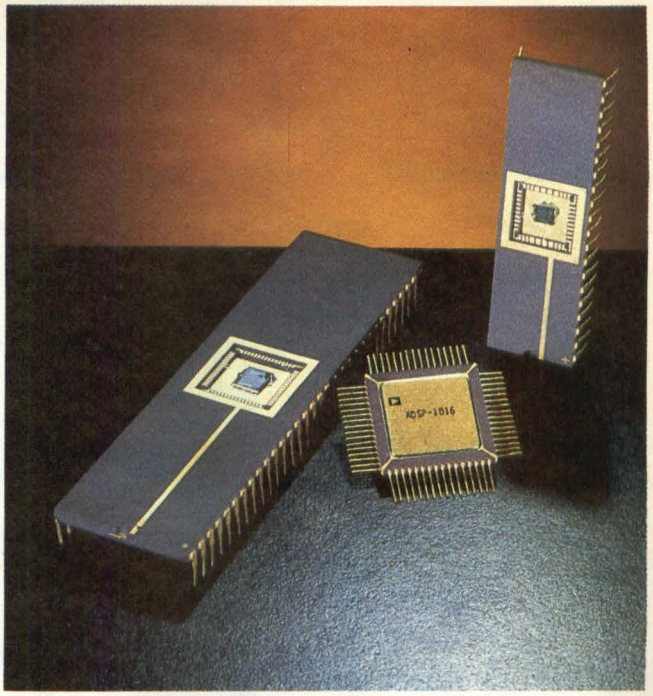

Photo courtesy Analog Devices.

When TRW introduced the TDC1010, it set the standard by which 16 × 16 multiplier/accumulators were measured. Fabricated in TRW's bipolar process, the part offered the capability to specify input data as two's complement or unsigned magnitude, yielding a full-precision 32-bit product. Products could be accumulated to a 35-bit result.

Since then, the company has gone on to offer both bipolar and CMOS pin-compatible versions of the part. Its TDC1043, for example, is compatible with the TDC1010, but does not provide the preload and least significant product output capabilities. However, what the part does offer is almost twice the speed of the 1010 at less than one-third the power dissipation.

Building on the success of the bipolar parts, the company recently disclosed information on its 16 × 16 CMOS multiplier/accumulators. The first, the TMC2010, operates at a 160-nsec cycle time. Compatible with the TDC1010, the part consumes less than one-sixth the power of its bipolar cousin, depending on the multiply-accumulate rate.

By scaling down to a 1-micron CMOS process, TRW (La Jolla, CA) introduced its recent TMC2110 with a 50% increase in speed over the TDC1010. In the past, the company's main competition has been from companies such as IDT, Weitek, Analog Devices and Logic Devices, who all offer multiplier/accumulators in CMOS. But competition has become more fierce with the introduction of important parts from Micropower Systems, VLSI Technology Inc., and most importantly, Texas Instruments (**Table 1**).

The TI part, dubbed the TCHT1010, has sub-100-nsec multiply and accumulate times and worst case power consumption measuring 165 mW. The part has TTL- and CMOS-compatible I/O and, like members of TI's SN54/74HC family, it includes latch-up suppression circuitry and an electrostatic discharge protection network capable of protecting the part from transients of up to 3000V.

Micro Power Systems (Santa Clara, CA), best known for its semicustom, full custom and standard product line since its inception in 1981, also announced a 16 × 16 CMOS multiplier/accumulator last month. The company is one of the few

	IDT	Weitek	Texas Instruments	Micro Power Systems	VTI	Analog Devices	TRW	Logic Devices	Fairchild Semiconductor
Part Number	IDT7210 IDT7243	WTL2010	THCT1010	MP1010	VL2010 VL2044	ADSP1010A	TMC2110	LMA1010	5 AC/74AC1010
Pin Equivalent	TDC1010J TDC1043	TDC1010J AM29510	TDC1010J AM29510	TDC1010 TMC2010 WTL1010	AMD29510 TDC1010J	TDC1010J	TDC1010	TDC1010J AMD29510	TDC1010J
Speed Multiply/ Accumulate	65, 75, 100,165 nsec	2010 (65 nsec) A (60 nsec)	100JD (100 nsec) 170JDE (140 nsec)	75 nsec (typ) 100 nsec (max)	50-65 nsec (typ) 65-90 nsec (max)	70 nsec (max)	100 nsec	standard 120 nsec (max) 1 (90 nsec)	40 nsec
Packaging	64-pin DIP 68-pin LCC	64-pin DIP 68-pin LCA 68-pin LCC	64-pin ceramic 68-pin plastic	64-pin ceramic 68-pin grid array 68-pin LCC	64-pin ceramic	64-pin ceramic 68-pin grid 68-pin LCC	64-pin DIP 68-contact chip carrier 68-pin LCC	64-pin DIP 68-pin plastic 68-pin LCC	64-pin DIP 68-pin plastic 68-pin LCC
Power Dissipation	<250 mW	200 mW	165 mW	125 mW	<200 mW	200 mW (typ)	500 mW	150 mW (max)	500 mW
Pricing	(100x) $123 (100x) $123	(100x) $80	(25x) $65 (25x) $85	(100x)/CD $75 (100x)/MD $300	(25x) $95	(100x) $95	(100x) $98	(100x) $60 (100x) $68	N/A

Table 1: A potent variety of 16 × 16 multiplier/accumulators are vying for position in the competitive DSP marketplace.

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that will offer its part, the MP1010, in die form.

Also entering the field, VLSI Technology (San Jose, CA) announced two parts, the VL2010 and the VL2044. The 2044 is identical to the 2010 except for the elimination of a preload function. According to Henri A. Jarrat, president of VLSI, these components are only the first in a family of products the company plans to introduce in 1986. Both of the new parts feature multiply/accumulate times as low as 50 nsec, while typically consuming less than 200 mW.

Yet another start-up company, Bipolar Integrated Technology (Beaverton, OR) will enter the multiplier/accumulator business next year. This firm will not compete directly with the slew of CMOS vendors, but will target high-speed market niches with its own bipolar semiconductor process. Its first products will form a family of digital signal processing building blocks and will include a 16 × 16 integer multiplier and muliplier/accumulator, a 32/64-bit floating point multiplier and ALU and a multiport register file. The company expects first samples of its 16 × 16 integer multiplier by the first quarter of 1986 and the 16 × 16 multiplier accumulator by the second quarter of 1986. The parts will be offered in both ECL- and TTL-compatible versions. Les Soltesz, product marketing manager for the parts, claims that the ECL version of the integer multiplier will work at under 8 nsec and dissipate less than 4W.

As Analog Devices *et al* have targeted what was once exclusively TRW's market, so Bipolar Integrated Technology is aiming its sights on Advanced Micro Devices. Although AMD has yet to announce any similar parts, they will likely enter the market soon.

Another company with its eyes on both the CMOS and the ECL marketplace is Fairchild Semiconductor (South Portland, ME). No details on their ECL parts are available as yet. However, early next year Fairchild will announce a range of CMOS DSP parts that includes a 16 × 16 multiplier and 16 × 16 multiplier/accumulator. A single-chip DSP ALU will follow. The parts will all be fabricated in Fairchild's Advanced CMOS technology process, which has already produced a range of SSI devices.

Next year should prove a very competitive time in the DSP market. The eager start-ups may meet some formidable competition in the form of Fairchild and Texas Instruments.

—D. Wilson

SIMD Architecture Takes Aim At Image Processing

Digital signal processing, finite element analysis and database searching are operations that require uniformity of computation across large, well-organized data structures. In the past, array processors have met this requirement, but with limited success and at considerable cost.

Future cellular array processors may offer a more cost-effective solution by more closely mapping the organization of the problem to the architecture of the machine, resulting in increased throughput. Although many array processors are currently on the market, only a few cellular array processors have been developed to date—the DAP from the British ICL firm, the Goodyear massively parallel machine and the NCR GAPP chip set. These are single instruction/multiple data (SIMD) machines.

Joining this list is a cellular array processor from ITT's Advanced Technology Center (Shelton, CT). Presently in prototype, the ITT cellular array processor (CAP) could eventually form the basis for a single board that plugs into the IBM PC. According to Steven Morton, the architect of this cellular array, a PC so equipped could achieve one-third or more of the capabilities of a CRAY-1. The basic

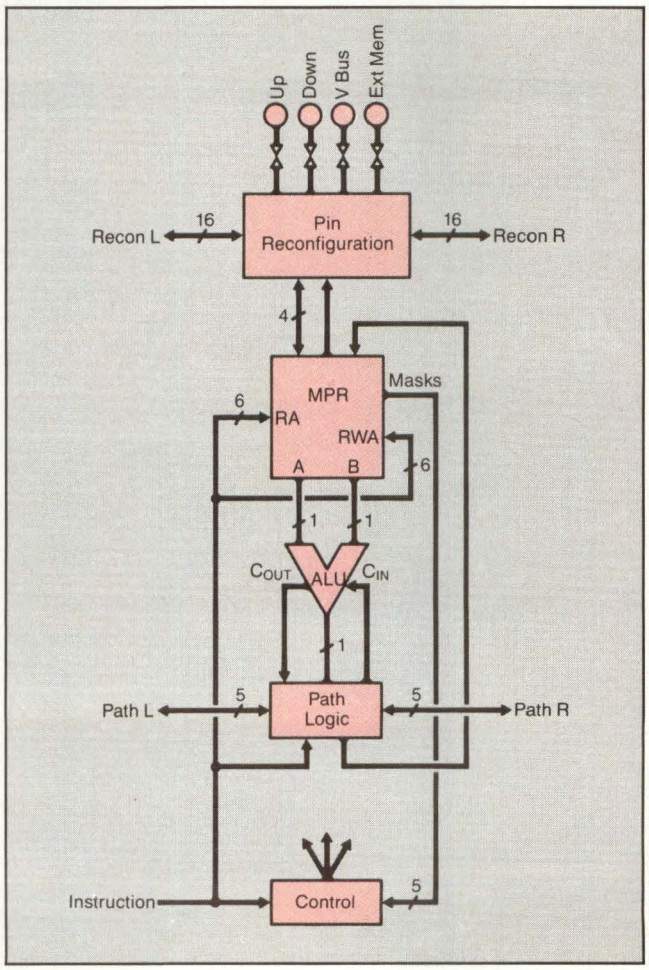

Figure 1: A single chip cell is modeled on the 2903 bit-slice processor from AMD. Using a 1-bit rather than 4-bit slice, ITT has combined 20 of these processing elements on a single prototype chip, to achieve a single instruction/multiple data (SIMD) architecture. In the ITT single-chip cell design, the most- and least-significant slice are stored as locations in multiport RAM.

processing element is analogous to the 2903 bit-slice machine from Advanced Micro Devices (Sunnyvale, CA). Unlike the 2903, however, the ITT design represents a 1-bit slice rather than a 4-bit slice.

As shown in **Figure 1**, two locations are simultaneously read from the multiport RAM, operated on by an ALU and the result fed back to a shifter. Moreover, instead of using pins external to the chip to define the most- and least-significant slice, the ITT design stores these configuration masks as locations in the multiport RAM, offering a wider variety of set-ups.

So far, ITT has successfully combined 20 of these 1-bit processing elements on a single chip. The chance of a defective element ruining a design has been eliminated by a fault-tolerant technique that will switch-out defective elements under software control. The fault-tolerant technique was necessitated by the large die size, which provides the prototype machine's capability to work in both bit-serial and bit-parallel mode, as well as allowing users to define a completely arbitrary word size.

In the ITT cellular array architecture (**Figure 2**), each row of the vector execution unit can be viewed as a 16-bit processor of which their are 16 in the design. The processor array forms the heart of the ITT image processor. Image data is loaded into the video DRAMs through the high-speed I/O port, where it can be accessed concurrently by each of the processing elements. In the prototype, the computation of data and addresses is distinguished by two separate elements. An up/down mechanism allows the rows to communicate with one another.

ITT hopes to integrate the image processor onto a single IBM PC board. Using the IBM PC solely as an operator interface, all image processing will be handled live within the CAP, eliminating the PC bandwidth bottleneck that has plagued other designs. It will be based on a second generation architecture that will be disclosed soon.

—D. Wilson

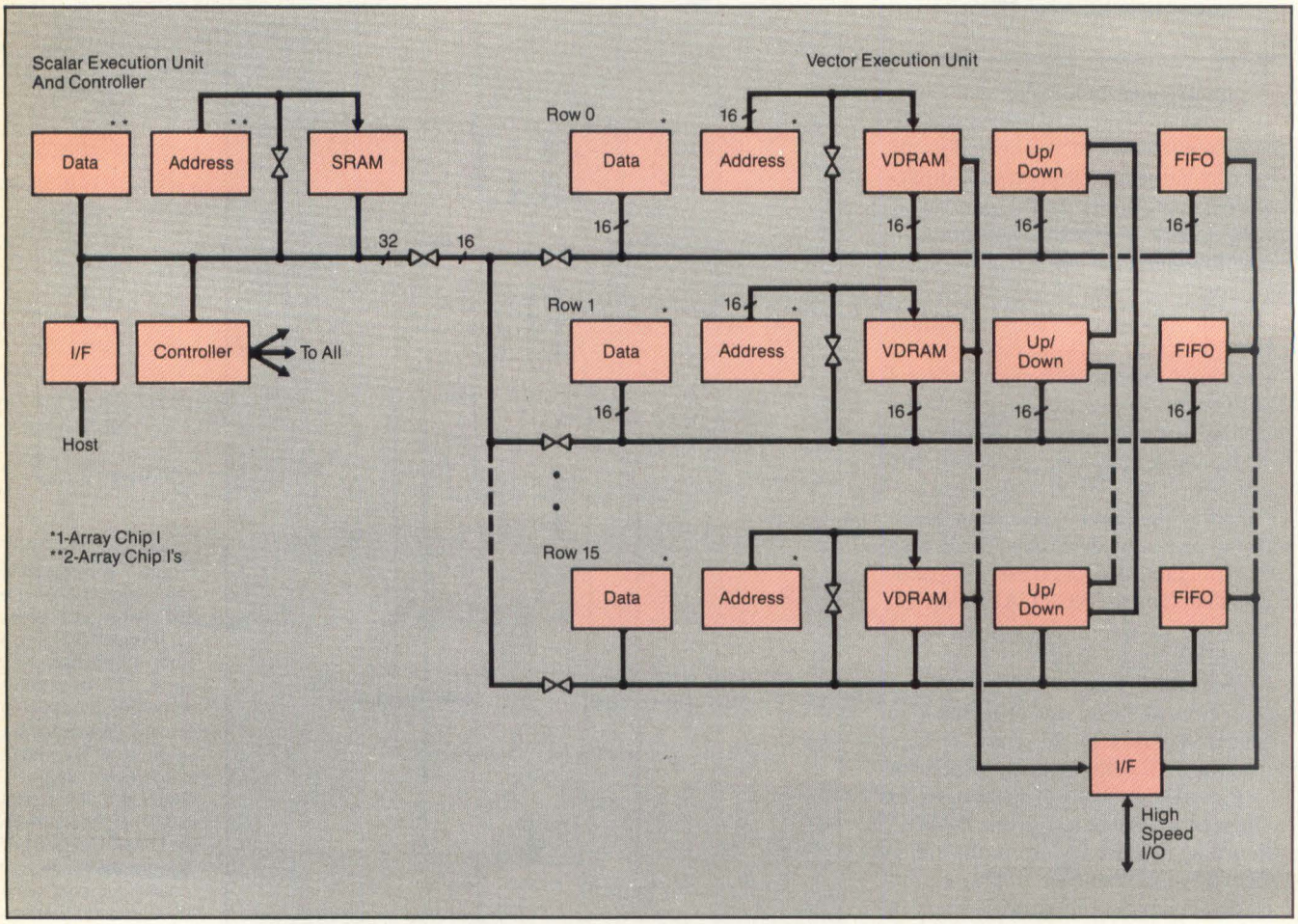

Figure 2: The prototype ITT cellular array processor architecture has both a scalar and a vector execution unit.

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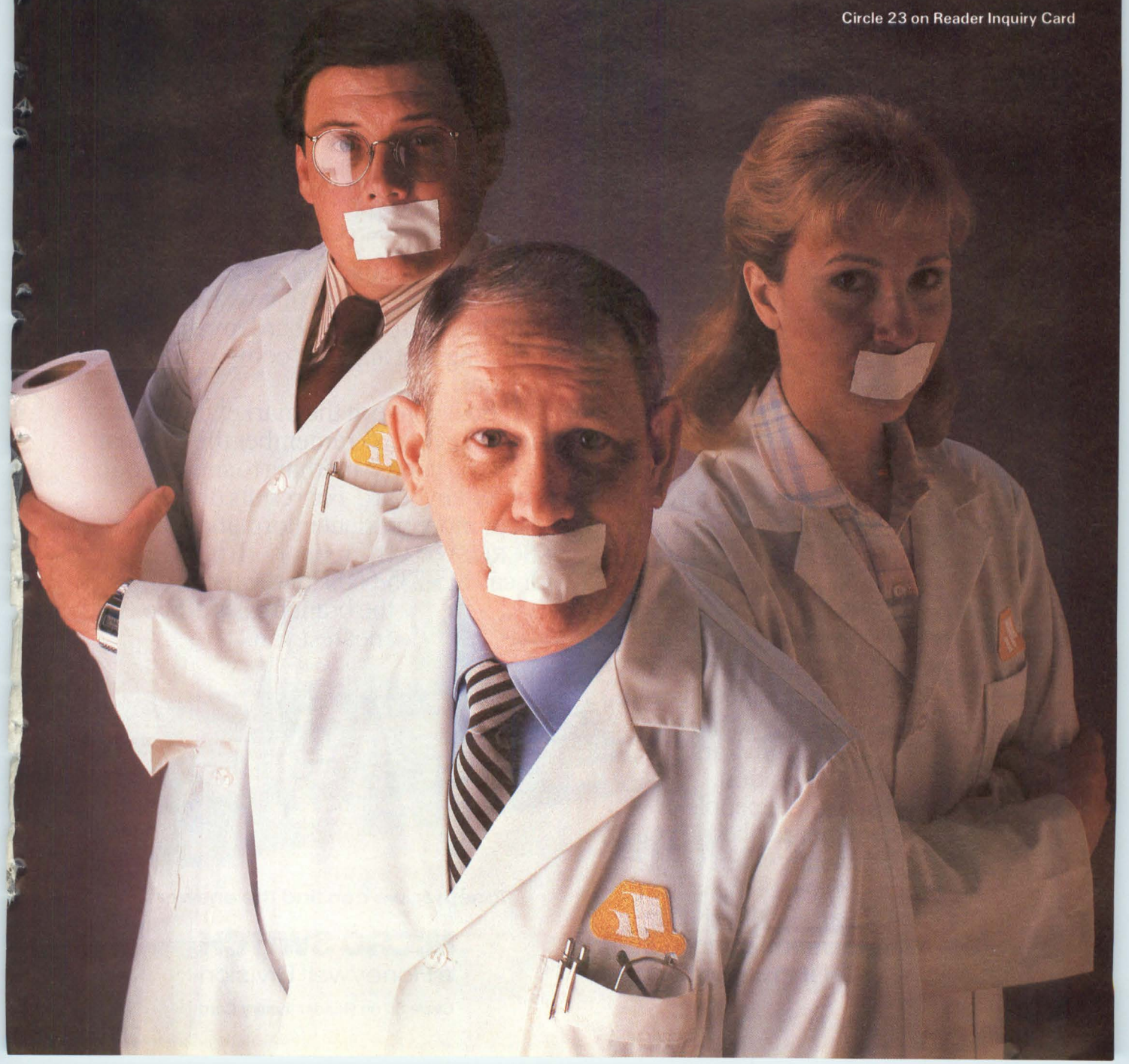

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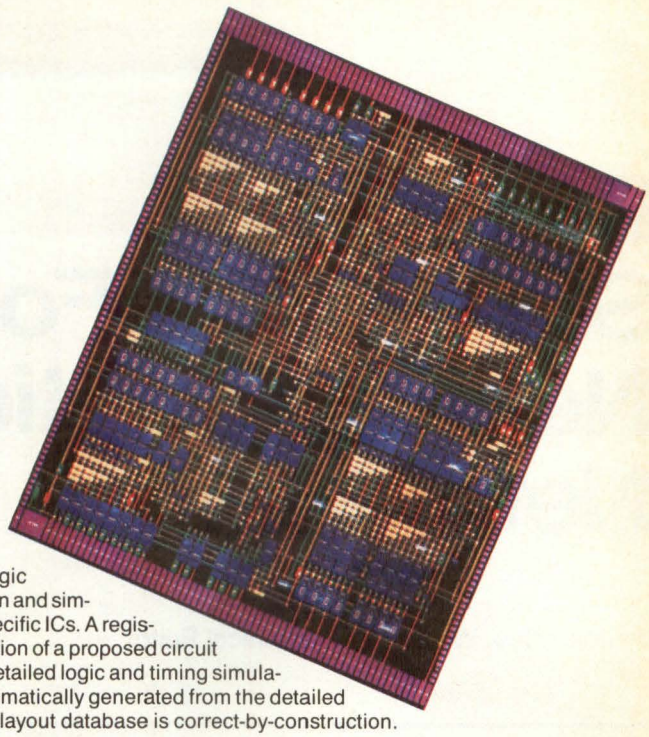
Users Tailor Standard Designs Through Silicon Compilation



Designers at Cirrus Logic focus on functional design and simulation of application-specific ICs. A register-transfer level description of a proposed circuit serves as the basis for detailed logic and timing simulation (shown above). Automatically generated from the detailed design, the subsequent layout database is correct-by-construction.

Combining the advantages of standard products and custom-designed LSI circuits, Cirrus Logic (Milpitas, CA) has brought out a range of application-specific ICs for data communications, graphics, and mass storage applications. These ASICS can be modified to meet user requirements. The company provides detailed concept specifications similar to data sheets provided for off-the-shelf devices like microprocessors and associated peripherals. Within this framework, users have the freedom to add or delete features, specify the operating frequency of the final product and can choose the desired input/output interfaces.

Rather than designing the chip, users choose from the specifier menu which becomes the blueprint for the finished part. Besides providing a detailed design specification, Cirrus also has responsibility for functional specification, physical layout, simulation, mask generation and test program generation. Prototype chips must also perform to specification in the target system, or the company will make the necessary design modifications.

Conventional semicustom approaches (e.g., gate arrays, standard cells and macro cells) typically require that users assume responsibility for many, or all, of the front-end tasks that Cirrus handles. Often in semicuston LSI approaches, system designers must also be trained to use sophisticated CAD tools on engineering workstations. And, their finished designs may not be optimized for chip density or speed due to the limited expertise of the user or limitations imposed by standard cells (fixed function and size) and gate arrays (fixed function, size and location).

Bypassing such limitations, the silicon compiler employed by Cirrus Logic generates circuits said to rival handcrafted designs in terms of size and speed. For example, the company compared a handcrafted DUART for the 68000 microprocessor with a similar design generated with the silicon compiler. Average size per transistor for the compiled design was 1.37 sq. mils compared to 1.85 sq. mils for the handcrafted design. Furthermore, the handcrafted design took 6.5 work-years to complete, whereas the compiled design took only 6 work-months.

The ability to generate packed circuits in a minimum amount of time – estimated to take only 10% of total development time – allows the company's designers to focus on functional design and verification of the final circuit. Working from a preliminary block diagram described in the concept specification, a designer would delete any functions not required by the user as well as add any desired features. The user specifies these features in terms of state machine descriptions, truth tables or Boolean expressions. The detailed implementation is left to the compiler. At the same time, the designer also lays out the circuit by grouping related functions together as well as routing necessary buses and control signals. The gate level logic is then automatically synthesized, a netlist is extracted, and functional simulation follows.

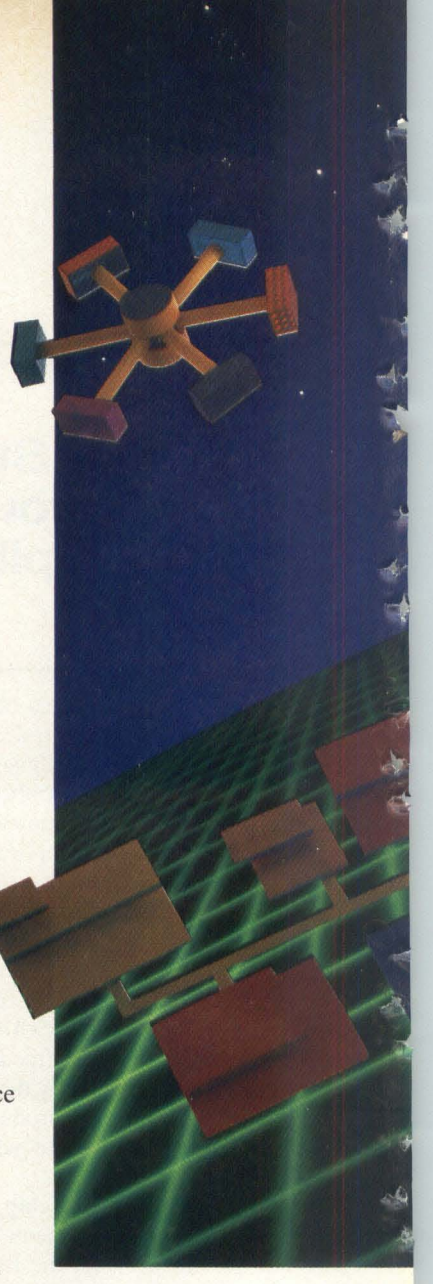
Once functional design and simulation are finished, the "floorplan" (or functional layout) serves as the basis for the detailed implementation. The functional blocks are described in terms of 30 primitive cells ranging in complexity from 2 to 14 gates. These cells have the detailed transistor-level descriptions required for layout, design rule verification and timing simulation. The cells can be implemented in a variety of process technologies (3-micron NMOS as well as 1.6-micron two-metal CMOS and 3-micron CMOS currently) in much the same manner as the alphabet can be implemented in different type fonts.

Should the results of timing simulation require changes in the layout of the circuit, a Cirrus designer can manually modify the physical layout. If the designer goes back to the block level, regeneration is automatic. Minor changes to the control logic can be incorporated at the metal mask level after chip layout.

Cirrus Logic foresees a typical development cycle of six months from detailed specification to prototype. The company has made arrangements with Advanced Micro Devices (Sunnyvale, CA) for mask generation and wafer fabrication, but retains responsibility for final assembly and test.

—Aseo

Protocols Set Course For Next-Generation Networks



by Joe Aseo, West Coast Technical Editor

The second stage of local area network development is well under way. The driving force remains the same as in the first stage: a network should be a common implementation available from multiple vendors.

Xerox's Ethernet system for heterogeneous machine connection has evolved into the IEEE 802.3 standard. ISO and IEEE panels have steadily chipped away at establishing complete, layered models for communications. Clearly, common data transport mechanisms embodied in the range of IEEE 802 proposals will move many users from proprietary implementations like IBM's System Network Architecture (SNA) and Apollo Computers' (Chelmsford, MA) DOMAIN network to common implementations available from many vendors. A de facto standard overnight, the recently released token-ring net from IBM (see box) shows a compatibility path for many vendors who have waited on the local net sidelines. And, gaining rapid acceptance in the factory, the General Motors-backed Manufacturing Automation Protocol (MAP) (IEEE 802.4) seems to meet the criteria for LANs of the '80s. It provides a common set of network services for large numbers of users.

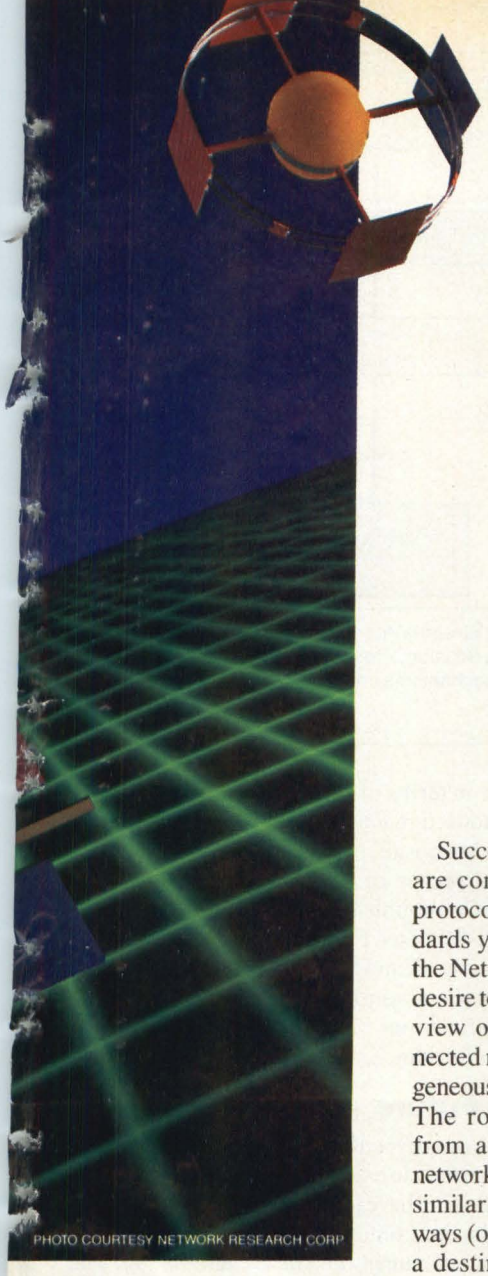
Further marking 1985 as a potentially fruitful year for local nets, 100-Mbit/sec backbone networks like the Fiber Distributed Data Interface (FDDI) will emerge to provide the bandwidth necessary to integrate voice and data switching on the same network.

Despite progress towards standardization, much work remains until higher levels of network protocols are defined and implemented. Controversy over specific physical media and access methods have been largely resolved through the work of the IEEE 802 committees, but standard definitions of the protocols to be implemented on top of these transport mechanisms have yet to be determined. For example, there exists no standard method to route packages between different IEEE 802 networks. There is also little agreement on the specific means to reliably transport messages from one machine to another. Moreover, standards committees have given little thought to desirable services such as file and record locking, network addresses and directory services, as well as remote procedure calls. Until such services have been defined and implemented, users will have little more than the functional equivalent of two tin cans connected by a piece of string.

From The Bottom Up

A quick look at the International Standards Organization's Open Systems Interconnect reference model helps clarify network services and implementations. The model organizes the various services offered by a general communications network into seven layers. Each layer builds upon the services offered by the nearest lower layer. Each succeeding higher layer has an increasingly conceptual (or logical) view of the network since it is unaware of the layers that are not immediately below it. This affords a degree of isolation so that lower-level services can be changed without causing changes at the upper layers.

The Physical layer is the lowest level of the reference model. It supports the electrical and mechanical characteristics of the physical interconnection. Examples of the physical interface include the RS-232 and RS-442 standards for low speed serial communications and the coaxial cable used in Ethernet. The Data Link layer supports the lowest logical link possible on the network. It provides the ability to gain access to the physical interconnection, send data to another node on the network, and subsequently release access of the physical link for use by other nodes. These two layers are the only ones to have reached the final stages of standardization. IEEE committees have defined three network topologies and access methods (Ethernet, token bus and token ring) although there are many variations on these themes (e.g., Cheapernet, AT&T's StarLAN and FDDI).



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In the OSI model, each higher layer becomes more software intensive and host dependent.

Succeeding higher layers are composed of de facto protocols or proposed standards yet to be adopted. At the Network level, there is a desire to provide each user a view of several interconnected networks as a homogeneous collection of nodes. The routing of messages from a node on one local network through bridges (on similar networks) and gateways (on dissimilar ones) to a destination on a remote network should be transparent. At present, only the CCITT X.25/X.75 and ARPANET Internet Protocol (IP) have been widely implemented. The IEEE 802.1 internetworking specification, which is intended to link the IEEE 802 data and physical links, is still being defined.

On top of the routing functions of the Network layer, the Transport layer provides reliable transmission of messages from one user to another. This can take the form of datagram services conceptually similar to letters mailed through the postal system—users attach an address to the message and hope it gets delivered. Should it get lost in transit or the recipient is no longer on the network, the user may (or may not) be notified and allowed to retransmit.

In contrast, a virtual circuit service provides an assured connection between two nodes in much the same manner as a telephone call. As part of this service, conversations are monitored so that a party talking too fast is requested to retransmit portions of the message until the other party catches up. Network protocols providing Transport level services include ARPANET TCP/UDP and NBS Class IV.

Providing dialog management services is the job of the Session layer. On this level, one user process on one host is linked to a user process on another. Services are also provided to con-

The Giant Moves

In October, three years after announcing a joint agreement to produce a token-ring local area network, IBM and Texas Instruments unveiled a communications system destined to become a standard. Participants in the LAN industry segment have long watched for Big Blue to make its big move. IBM's customers, of course, represent a vast installed base that could be the springboard propelling the LAN out of the niche and into the mainstream.

Based on a five-chip set from Texas Instruments (see *Digital Design*, November 1985, p. 97), the IBM network approach has been heavily promoted in standards committees. Interface specifications are said to meet the IEEE 802.5 standard as well as the European Countries Manufacturers Assn (ECMA-89) standard for token-ring baseband LANs. As in its PC program, IBM is opening up the system. Interface components will be offered by TI and interface specs will be publicly available.

The TI TMS380 chip set includes a system interface chip, communications processor, protocol handler, ring interface transceiver and ring interface controller. This chip set offers configurable options that include cycle-steal or programmable-burst mode operation, as well as polled or interrupt operation and list-suspension capability. Data transfers from the TMS380 to the workstation run at up to 40 Mbits/sec. The complete IBM Token-Ring Network Adapter card presently costs $695. Required is a Multistation Access Unit (MAU), at $660, which functions as a concentrator. Each MAU handles eight stations. Probable capacity of the network is 260 nodes. Use of telephone twisted-pair cabling simplifies many applications.

IBM has introduced an application program interface known as the Advanced Program-to-Program Communications for the PC (APPC/PC). Based on the SNA LU 6.2 interface, this application program reportedly forms an environment for development of application programs for peer-to-peer communication between PCs and SNA-based hosts.

How the Token-Ring Network connects to the PCNetwork, IBM's earlier low-end network entry, remains to be seen. Viewed by some as a stop-gap measure to fend-off complaints that IBM was restricting competition by delaying a LAN announcement, the PCNetwork has gained many adherents during the last 12 months. Sytek has said that its PCNetwork server, the 6610, is compatible with the IBM Token-Ring Network and initial reports indicate that the IBM Token-Ring's NETBIOS program can facilitate an interface to the IBM PC network.

SNA connections to IBM's important mainframe and minicomputer bases will likely emerge as APPC/PC software is developed. Plenty of users would like to see such capability today. IBM says that any PC on the network can serve as a gateway to hosts, allowing PCs on the ring to access 3270 applications as well as to upload and download files.

trol data exchange, delimiting and synchronization. Examples of such services include CCITT X.3/X.28/X.29. The Presentation layer is the lowest level that concerns itself with user-specific services. It provides the ability to discern the meaning of the data being exchanged. To this end, it provides services that define data types and their bit representations.

End users of these lower-level services interface via the Application layer. This layer can be viewed as a pool of services that the user accesses without regard to the location of the actual provider. Such services include file transfer, virtual terminal, electronic mail and remote procedure calls. Examples include Courier in Xerox Network Service and ANSI X.400 electronic mail.

Putting Theory Into Practice

Unfortunately, the idealized OSI reference model is difficult to implement from the bottom up. Succeeding higher layers become more software intensive and host dependent. Howard Gordon, chairman of Network Research Corp. (Oxnard, CA), notes that current work on network protocols still fails to deal with the reliable transport of data from one point to another. While applauding the efforts of the standards committees, Gordon asserts that the current bottom-up approach of specifying succeeding higher layers of abstraction delays addressing important issues such as operating system interfaces, remote procedure calls and network management until the end of the specification process. This forces users either to wait until preliminary implementations of the standards are available, or to use de facto protocols until these standards are widely accepted.

Fusion networking software from Network Research Corp. has been implemented to be protocol independent. Generic network services (e.g., virtual terminal and file transfer) are isolated from the implementation-dependent specifics (e.g., Physical and Link layers). As a result, the same package can support standard protocols like XNS and TCP/IP as well as proprietary protocols where existing standards do not exist. Gordon notes that the package can accept the proposed ISO higher-level protocols when defined, but customers will have similar functionality supported until then.

In addition, there seems to be a large degree of redundancy between the Network layer, Transport layer, Session layer and the Presentation layer in terms of error correction, flow control and message acknowledgment. As a result, many networks may implement some, but not all, of the upper layers. For example, Larry Green, director of advanced technology for Advanced Computer Communications (Santa Barbara, CA), speculates that the 100-Mbit/sec FDDI backbone network will have a pass-through Network and Session layer with a minimal Transport and Presentation layer for file transfers. This is due to the redundancy in functions between these layers. It also serves to optimize performance.

	MAP	TOPS	NFS
Application	ISO FTAM	ISO FTAM	File Access
Presentation	Null	Null	xdr
Session	ISO	ISO	rpc
Transport	ISO Class IV	ISO Class IV	ARPANET Diagram
Network	ISO Internet	ISO Internet	ARPANET IP
Data Link	IEEE 802.4	IEEE 802.3	IEEE 802.3
Physical	Coax	Coax	Coax

Table 1: The familiar seven layers of ISO network communications have helped to standardize a once-haphazard industry segment. Individual implementations—such as MAP, TOPS and NFS—vary, but ISO gives structure to LAN design.

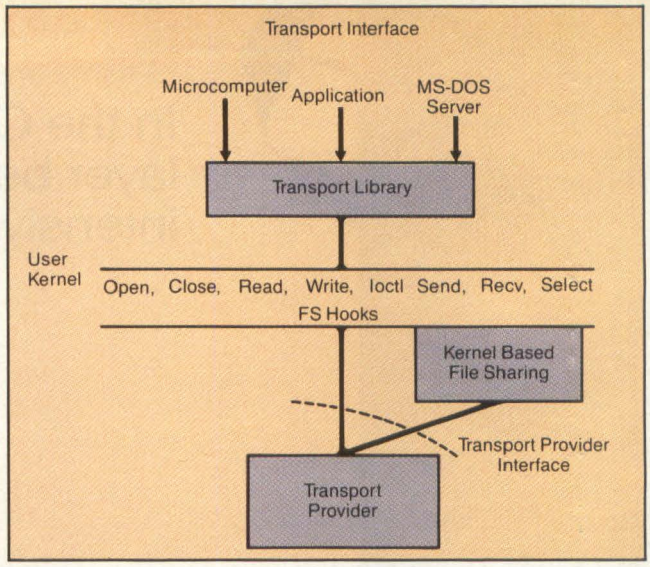

Figure 1: From AT&T, the Streams interface serves as the link between services provided by the Session, Presentation and Application layers and the data transport mechanisms implemented at the Physical, Data Link and Network layers.

MAP For The Future

Efforts are underway to implement common sets of upper-layer services with standards that do exist. Large-scale users such as General Motors and Boeing have joined together to implement these services within the context of industry-specific environments such as manufacturing and office automation. The Manufacturing Automation Protocol (MAP) provides networking between the factory floor and related services (e.g., manufacturing resource planning) for hardware and software offerings from multiple vendors. The IEEE 802.4 token bus serves as the backbone of the factory LAN with the ISO connectionless network service acting as the Network layer. Transport, Session and Application layers are also based on a subset of the ISO proposal for virtual circuit services, session management and file transfer and access (FTAM).

Related developments focus on providing standards in engineering and office applications. The Technical and Office Protocols (TOPS) will utilize the same upper layer protocols (ISO layers 3 through 7) as the MAP project, but will implement these on IEEE 802.3 (a.k.a. Ethernet) networks. Laurie Bride, manager of networking for Boeing Computer Services (Bellevue WA), says that future efforts will include adoption of standard protocols for electronic mail as well as remote procedure calls.

Yet another effort garnering industry support is the Network File System from Sun Microsystems (Mountain View, CA). It provides transparent sharing of file systems on diverse host processors and operating systems, using virtual nodes. Similar to inodes in the UNIX operating system, vnodes act as the interface for users to access local and remote files at the Application

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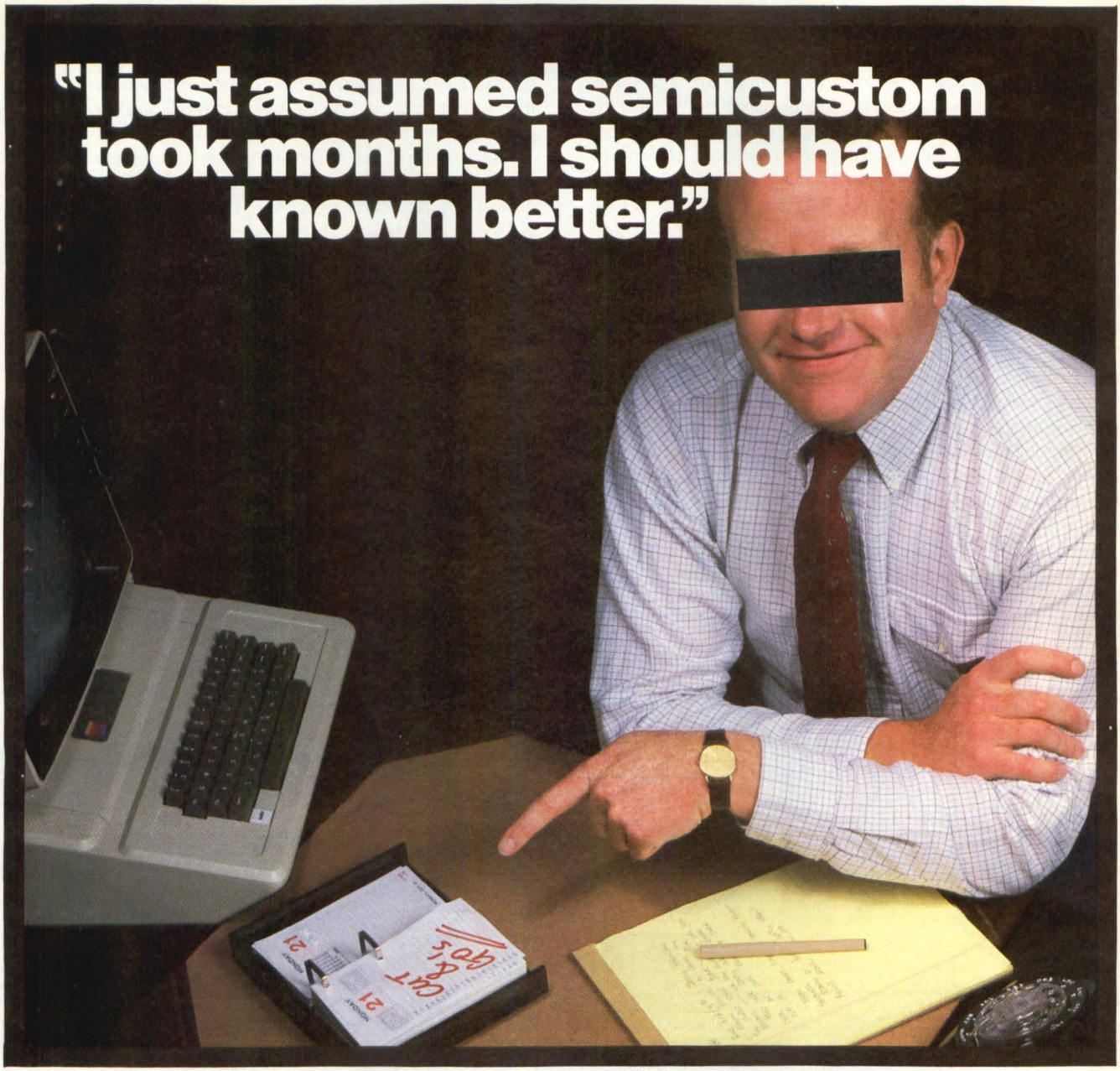

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layer. An external data representation format (xdr) allows file transfer without regard to specific file formats of individual host machines at the Presentation layer, while a remote procedure call (rpc) facility provides a transparent mechanism to service file requests at the Session layer.

Sun also provides a directory service, called the "yellow pages," at the Application layer. This allows sharing of central read-only databases (e.g., passwords) by multiple hosts. Current implementations use the ARPANET Universal Datagram Protocol (UDP) at the Transport level for transfers across Ethernet networks.

A major assumption embedded within the protocols conforming to the OSI model are that lower-level transport and routing services can be isolated from the upper layer services provided by such efforts as MAP, TOPS and NFS. However, the layer providing the cleanest break for portability remains a question. The importance of the distinction lies in the ability to separate the host-dependent portions of code from the network-dependent portions.

Three major efforts have focused on the Transport layer as the interface between higher-level network services and the actual transport mechanisms. AT&T Information Systems (Morris Park, NJ) has plans to implement its Streams interface in its next major release of UNIX System V. Berkeley UNIX versions 4.2 and the upcoming 4.3 incorporate a similar implementation called "Sockets." Likewise, IBM (Armonk, NY) has expanded its SNA to include peer-to-peer communications without host intervention via the Logical Unit (LU) 6.2 and Physical Unit (PU) 2.1 device interfaces.

As currently planned, the Streams interface takes advantage of common datagram or virtual circuit services across several network architectures (ARPANET TCP/IP, SNA, XNS, and NBS Class IV) to provide reliable data transfer facilities. The Streams interface itself consists of a well-defined bidirectional path between higher-level services and the physical transport mechanisms (**Figure 1**). This interface is implemented in the kernel for speed and efficiency with a common set of system calls to establish and close sessions, as well as to send and receive messages.

These operations are independent of the actual network protocols used to provide the services. Examples of higher-level services that will utilize Streams system calls include addressing remote nodes through directory services and remote procedure calls.

An earlier Transport level interface is the Sockets mechanism implemented in Berkeley UNIX versions 4.2 and 4.3. Ideas embodied in this interface have also found their way into the

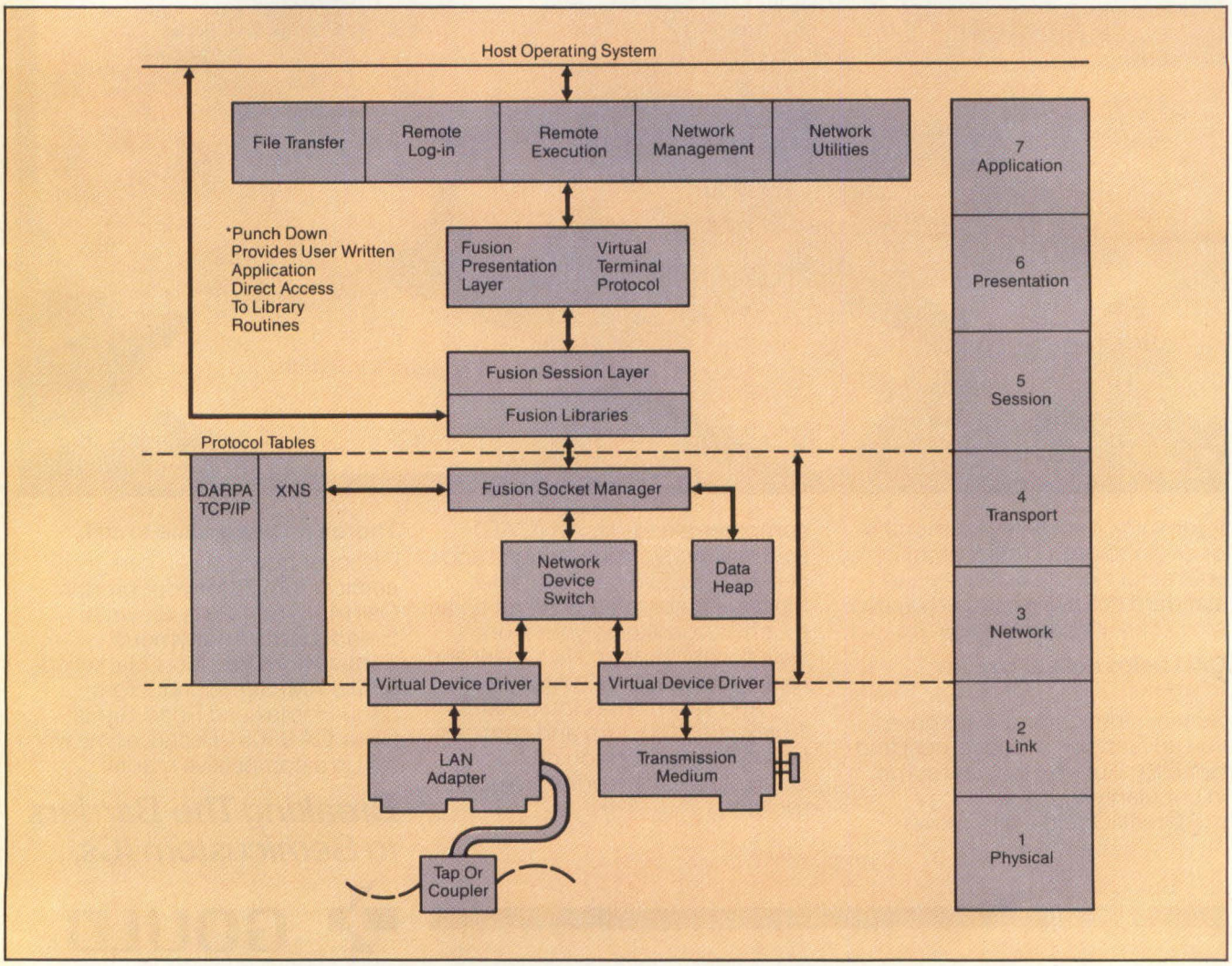

Figure 2: The Socket manager in the Fusion package from Network Research minimizes software overhead by using a common heap space for preparing messages for transmission or transfer to the host computer.

THE BUS ARCHITECTURE CAREER COMPATIBILITY TEST.

Streams implementation. Sockets serves as a switching mechanism between user processes requesting network services (and the network protocols that actually provide them) by providing temporary connections. Since messages are copied only once from the user to the operating system address spaces, messages can be quickly constructed for transmission (or stripped for host transfer) as they pass through each network layer for processing since only pointers to the data are passed rather than actual data. In contrast, other network software packages copy the entire message for each level of protocol that needs to be processed. A similar mechanism is also at the heart of Fusion from Network Research (**Figure 2**).

Providing similar functionality within the IBM networking environment, the LU 6.2 and PU 2.1 device interfaces provide the means for intelligent devices like workstations and personal computers to communicate without using the host computer as an intermediary. The company has also developed protocols for program-to-program communications and document interchange that use the services implemented with these drivers. Plug-compatible vendors note that LU 6.2 and PU 2.1 services also prove valuable as gateways for attaching hardware and software products from other vendors. Companies providing such tools include Communications Solutions (San Jose, CA) and the Orion Group (Berkeley, CA).

Supporting interfaces at the Session and Transport layer is the forerunner of IBM's token ring – the PCNetwork. The company has implemented file and resource sharing protocols in addition to Transport level services like datagrams and virtual circuits within the NETBIOS portion of its network interface card. Microsoft (Bellevue, WA) has announced plans to support a compatible version of the Session layer interface for third-party vendors, but such implementations may differ somewhat at the Network layer and below with the protocols implemented on the IBM PCNetwork card by Sytek (Mountain View, CA).

Gateways And Bridges

Transport and Session level interfaces that support multiple protocols (like Streams and Sockets) can also serve as gateways between transport services residing on different networks. For example, Lawrence Brown, director of UNIX networking services for AT&T Information Systems, notes that initial versions of Streams will support users on different networks running ARPANET TCP/IP on one end and IBM's SNA on the other. Gateways between heterogeneous networks and bridges between networks of the same type must work both at the Network and Session layer to be effective, according to Judith Estrin, executive vice president of research and development for Bridge Communications (Mountain View, CA). She notes that although users will communicate as peers at the Session layer (and above), Network layer gateways will provide the actual routing of messages across local network boundaries.

Estrin predicts that two types of gateways will serve the needs of most users. The large base of IBM mainframe equipment necessitates a direct link into the SNA network in terms of terminal gateways (e.g., IBM 3270) as well as Session layer gateways for file transfer and process-to-process communications. A second gateway based on the ISO protocols should serve the need for other proprietary networks (e.g., DECNET, WangNet and DOMAIN) to connect with each other as well as to those based on IEEE 802 proposals. Digital Equipment Corp. (Maynard, MA), which is altering the proprietary nature of DECNET, has pledged to comply with ISO/OSI standards. The firm recently added the LAN Bridge100 – a device linking multiple Ethernets – to a line that includes significant SNA interconnects.

EXAMPLE: Deleting a File on an Internet	OSI MODEL
FTP > I'd like to delete 'MyFile.'	APPLICATION

FTPServer =
call (program = FileDirectoryService,
procedure = GetRemoteFileServer,
filename = 'MyFile');
SuccessCode =
call (program = FTPServer,
procedure = Delete
filename = 'MyFile',
password = 'MyName');
	PRESENTATION

Gain access to an instance of the remote FTPServer using the password, 'MyName.' Once FTPServer is ready, send the procedure call message and wait for response.	SESSION
Despite a bad connection, repeat the message until the remote end has it exactly.	TRANSPORT
Although it may be impossible to guarantee success, make a 'best effort' to send the message to the appropriate local network on the internet.	NETWORK
Send the message to the appropriate station on the local network and be sure a corrupted message is at least detectable.	DATA LINK
Guarantee that communication cables may be plugged together and that everyone has the same understanding as to what constitutes a "1" and a "0" on the network cable.	PHYSICAL

Table 2: The seven layers of the ISO Open Systems Interconnect reference model can best be understood by following the processing needed to delete a remote file.

Another option is to use LU 6.2/PU 2.1 gateways to access the SNA networks. Paul Rampel, president of Orion Group, claims these interfaces provide similar functionality at the Network and Transport layers to the ISO protocols so users can interconnect their heterogeneous networks with one gateway rather than two. He notes that the IBM peer-to-peer communications protocol provides an arbitration facility to find a common set of services for data transfer between different host computers. As a result, services at the Session, Presentation and Application layers ensure connectivity across network boundaries, according to Rampel.

Standard protocols may never completely supplant de facto protocols for networking applications due to investments in both hardware and software. In the end, the ISO and IEEE specifications may exist as yet another set of protocols that the customer and vendor implement at their own choosing. **DD**

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Useful 602
Somewhat Useful 603

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Geographic Addressing		*X*	
Built-in Self-Test		*X*	
Software Configurability		*X*	

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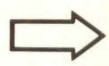

X.25 Software: Transaction Scheduling Keys Efficiency

by David Grothe, Gcom, Inc.

As more data communications users turn to the X.25 standard for packet-switched networks, the need for X.25 software packages and implementation hardware is growing dramatically. A number of options are available to those investigating X.25 implementation. Software packages are offered that can be run alone on a communications processor or be incorporated into the design of OEM products. Alternatively, many users are choosing to develop X.25 software for in-house applications or for inclusion as a value-added option in existing systems and products.

There are many trade-offs to consider when implementing X.25 applications. Key among these is the choice between transaction process scheduling and multiprogramming process scheduling. Transaction process scheduling assures that the design will exhibit high-speed operation, low use of memory space and overall efficiency of transmission.

The Multiprogramming Model

Multiprogramming, also called multitasking, is a process scheduling technique developed to serve the scheduling needs of time sharing operating systems. A multiprogramming system manages processes as if they were objects. Each process has a stack and a state vector. The stack represents an area of memory that contains the process' subroutine calling history. The state vector is an area of memory that contains information about the process (e.g., the location of its stack, its priority and its saved registers when the process is not running). A scheduler determines which process can acquire the processor at any given moment.

While a current process runs in a multiprogramming priority scheduling system (**Figure 1**), an array of "ready queues" waits, with the number of queues corresponding to the number of levels of priority. The state vector for each ready-to-run process waits in a queue corresponding to its priority level until the scheduler cedes the central processor unit. If the process currently running suspends itself, the process has to be "put to sleep" (made inactive). To do this, the system must store information in the state vector of the process for safekeeping. When the process runs again, it will resume at the point where it left off.

Subsequent to this operation, the system calls the central scheduler to determine which process is going to run next. The scheduler looks in the highest priority queue (e.g., priority 0) to see if there is a ready-to-run process. If so, the scheduler will remove the process from the queue and designate it as the new "current process". In order to correctly restart the new current process, the system must restore all of the information from the process' state vector into registers which define the execution environment of that process.

Suppose a program runs for a long time and "hogs" the processor. If the scheduler always runs the highest priority program until it suspends itself, and if the program is in an infinite loop or performing massive computations, the system will come to a complete standstill. This can happen even if the process is running at low priority. Typically, this problem is solved by suspending a process after it is run on the processor for a certain amount of time.

Yet another problem is process starvation. With a standard multiprogramming priority scheduler, there may be several long-running processes that are eligible to run at the first priority level. They will continue to be eligible at that priority level and just trade places on the processor, starving out processes at all other priority levels. Some kind of nonstarvation algorithm must be implemented to ensure that low priority processes get to run after waiting a reasonable length of time, regardless of the presence of higher priority processes. Many multiprogramming systems implement priority preemption in which the current process is halted and put in its ready queue as soon as a higher priority process becomes available. The higher priority

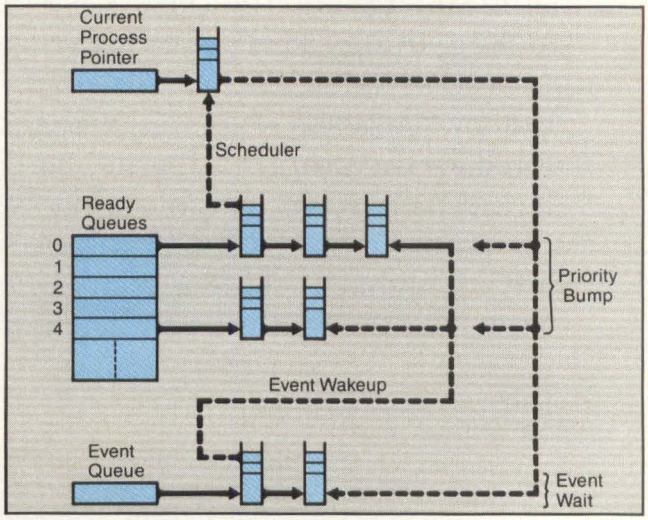

Figure 1: In priority multiprogramming, the scheduler determines which programs can acquire the processor. Multiprogramming system throughput is affected by the processor's scheduling duties and process switching load, which can represent considerable overhead.

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Career Compatibility Test			
Bus Capability	*VME**	*MB II*	*Mark Your Preference*
Power and Ground Pins (PI Connector)	*14*	*30*	
Synchronous Protocol		*X*	
Bus Parity		*X*	

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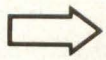

process is then given the processor.

Multiprogramming systems tend to have some or all of the above features in their scheduling mechanisms. In addition, multiprogramming systems usually implement some sort of process synchronization mechanism (e.g., an event-wait system).

In event-wait systems, a process is said to wait on an event when it is suspended until a particular event occurs. When the event is later "caused", all processes waiting on it will be awakened.

Such multiprogramming systems are often called "event driven." This is actually a misnomer, because nothing actually happens when an event is caused – something only happens when a process has waited on one. These are more aptly called program-driven or wait-driven systems. The process has to do something itself in order to be put to sleep. It has to wait on an event.

The process, in the multiprogramming model, has to have its state saved when it is put to sleep. Waiting on an event requires this overhead. When the event is caused, more overhead is required to wake it up – it must be removed from the event's wait queue, put into the ready queue and then the scheduler must be called to determine which process has the highest priority. The scheduler must then remove that process from the ready queue, restore its registers, switch to its stack and return into the program.

In a multiprogramming communications system, time that the processor spends doing process switching and scheduling lowers potential throughput by consuming processor resources that would otherwise have gone to processing messages. What makes this even more costly is the necessity of disabling interrupts during much of this overhead processing. Interrupt routines tend to cause events, which in turn cause the scheduler to run. If the scheduler itself was interrupted, the ready queue and other scheduling structures might be corrupted, so the scheduler must disable interrupts to protect itself.

The result is that the CPU must run for perhaps half a millisecond or, on slower processors, even a full millisecond at a time without being able to respond to real-time interrupts. This can lead to input overruns and the loss of data, so line speeds have to be kept low.

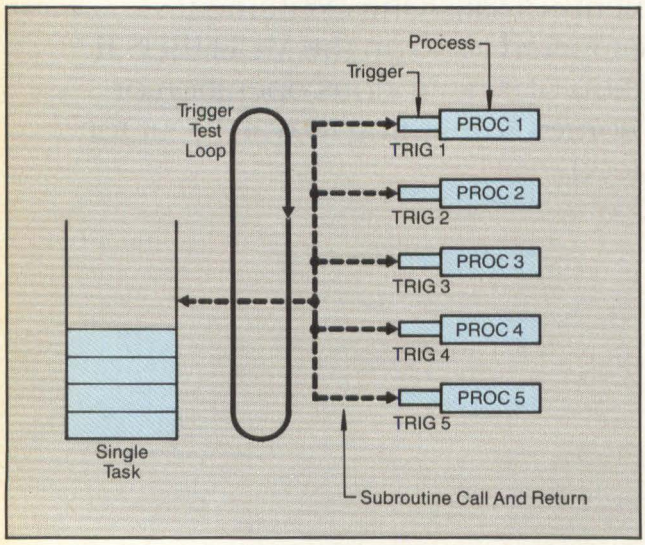

Figure 2: With the Trigger Method of X.25 transaction scheduling, every process has an associated byte, or trigger. Since there is only one stack, no complex priority schemes are needed.

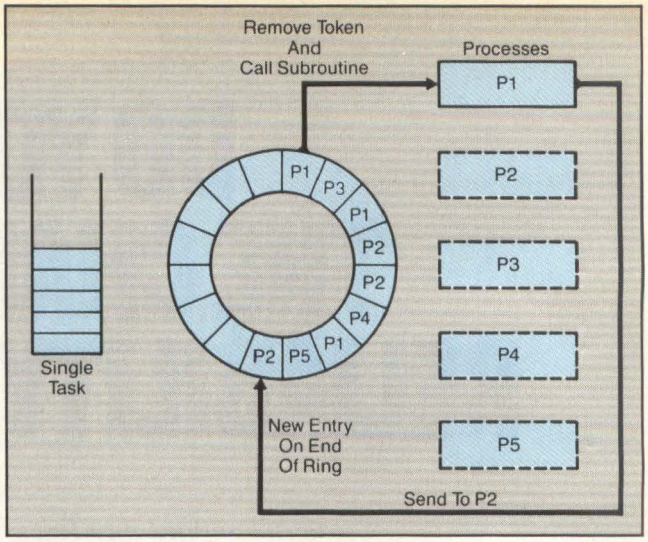

Figure 3: Data communication software implemented using the Ring System centers on a large circular buffer. Each slot in the "ring" buffer can hold a token. A scheduler removes tokens and calls the destination process.

In a data communications system, priorities do not have any real value – the multiprogramming priority scheduling method always runs the highest priority program in the system, whether or not that is what is needed to move data through at a particular time. The processor is so busy doing process scheduling and switching that the overhead of scheduling is often as much as the amount of time spent actually processing the data.

Let The Data Drive The Processing

High overhead and low throughput associated with multiprogramming priority communications systems can be avoided by using transaction scheduling. With this method, an event-wait mechanism is not needed – the data itself drives the processing. The Trigger Method, Ring System and G-System have been implemented by Gcom, Inc. (Urbana, IL). In all three approaches, the process control structure of the program closely models the protocol's data-flow diagram.

With the Trigger Method (**Figure 2**), every process has an associated byte or an integer with it, called its trigger. The trigger scheduler is just an infinite loop of trigger tests. If a trigger tests non-zero, the corresponding process is run. These processes are not independently executing processes such as those in multiprogramming systems. They are really subroutines – the scheduler calls one, it holds the processor as long as it needs it and then it returns. If it is stopped by an interrupt, the registers are quickly saved on the stack. When the interrupt returns, it always returns to the interrupted process. There is only one stack, so there is no complex priority scheme. There is much less overhead involved than with the multiprogramming model's multiple stacks.

Another advantage of the Trigger Method is that since each process is a subroutine, one process cannot interrupt another. Each runs to completion, so no preemption or synchronization problems can occur.

Throughput improves because the code that executes in a Trigger system is almost entirely interruptable, whereas multiprogramming systems require long periods of disabled interrupts. Process switching is also fast – 10 μsec on a 4-MHz Z80. This allows running up to twice as many packets per second as in a multiprogramming communications system. This through-

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Distributed Arbitration		*X*	
Number of Arbitration Levels	*4*	*20*	

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put increase is due to getting back as useful CPU cycles the overhead time associated with scheduling in a multiprogramming system. Since interrupts are almost always enabled, real-time events are handled quickly. Since the triggers are tested in a logical data-flow sequence, even the small overhead of trigger testing is minimized.

Ringing In The Tokens

The Ring System has all the advantages of the Trigger Method—low overhead, interrupts enabled almost all of the time, data driven—but it has a different scheduling algorithm. The Ring System uses a large circular buffer—the ring. Each slot in the buffer can hold a token (**Figure 3**). A token is a small structure with fields containing the identification of the process that sent the token, the identification of the process to which it is sent and parameters.

The ring scheduler maintains an input pointer that points to the next slot into which a token should be inserted, and an output pointer that points to the next slot from which a token should be removed. The scheduler is an infinite loop which removes a token from the slot designated by the output pointer and puts it in a location known to all processes. The scheduler then calls the process to which the token should be sent. That process can look at all of the information in the token and can send as many tokens as it wants by calling a system routine that inserts a token into the next input slot.

Circle 24

The effect is dynamic adaptation to the data flow. With the Trigger Method, the order in which triggers are tested is fixed at compile time. With the Ring System, tokens follow the actual instantaneous data flow as they come out of the scheduler. Thus, the Ring System is better for protocols in which the data flow pattern varies considerably—as the scheduler goes around the token ring, it will actually track the flow. In addition, the token ring generates a transaction history of the last few hundred activities in the system, allowing data flow to be traced for debugging purposes.

G-System Scheduling

A third method of transaction scheduling, the G-System, is an elaboration on the Ring System. A configuration file specifies exactly what processes exist and exactly what their connections will be. Each G-System process has a number of "plugs" or data output paths, and a number of "sockets" or data input paths. In the configuration file, connections between processes are specified in terms of which plugs are connected to which sockets. The configuration file contains an encoded version of a data-flow diagram. This file is compiled into a table with entries for each process. When a process sends a token, instead of making a system call in which the receiving process is specified, it makes a system call that directs the system to send a token to whatever process is connected to a particular plug. Thus, the sending process has no information about the receiving process. When a process makes this system call, the system consults a table to determine which process' socket is connected to the sending process' plug, fills in the token, puts it in the ring and the token is sent.

The major advantage of the G-System is that modules can be coded completely in isolation and specified only in terms of their inputs and outputs. This results in an extremely flexible system that allows "cutting and pasting" to meet current needs. This design sacrifices some efficiency to gain this flexibility—the table must be consulted every time something is sent—but this is a small trade-off for the greater efficiency in coding and developing new systems.

When comparing the merits of different X.25 software packages, designers should be wary of any data communications system that is built on a multiprogramming or multitasking model, especially if the system allows preemptive scheduling. In these systems, any one task can conceivably preempt any other task at any time, so there are often serious bugs which manifest themselves only under particular, difficult-to-reproduce circumstances. For this reason, multiprogramming schedulers may still have serious bugs in them after years of operation. The alternative Trigger Method offers simplicity and efficiency in most applications. When there are a large enough number of triggers to test (30 or more), the Ring System can offer some advantages. It will save time because it allows for better isolation of modules and offers more software reliability. The third alternative for transaction scheduling, the G-System, is appropriate for custom tailoring data communications systems that are built up from modules chosen from a large set of protocol handling modules. This offers easier control over configuration and interrelation of modules benefiting the OEM designing a communications board. DD

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Useful	617
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Synchronous Protocol		*X*	
Spec Options	*Many*	*Few*	

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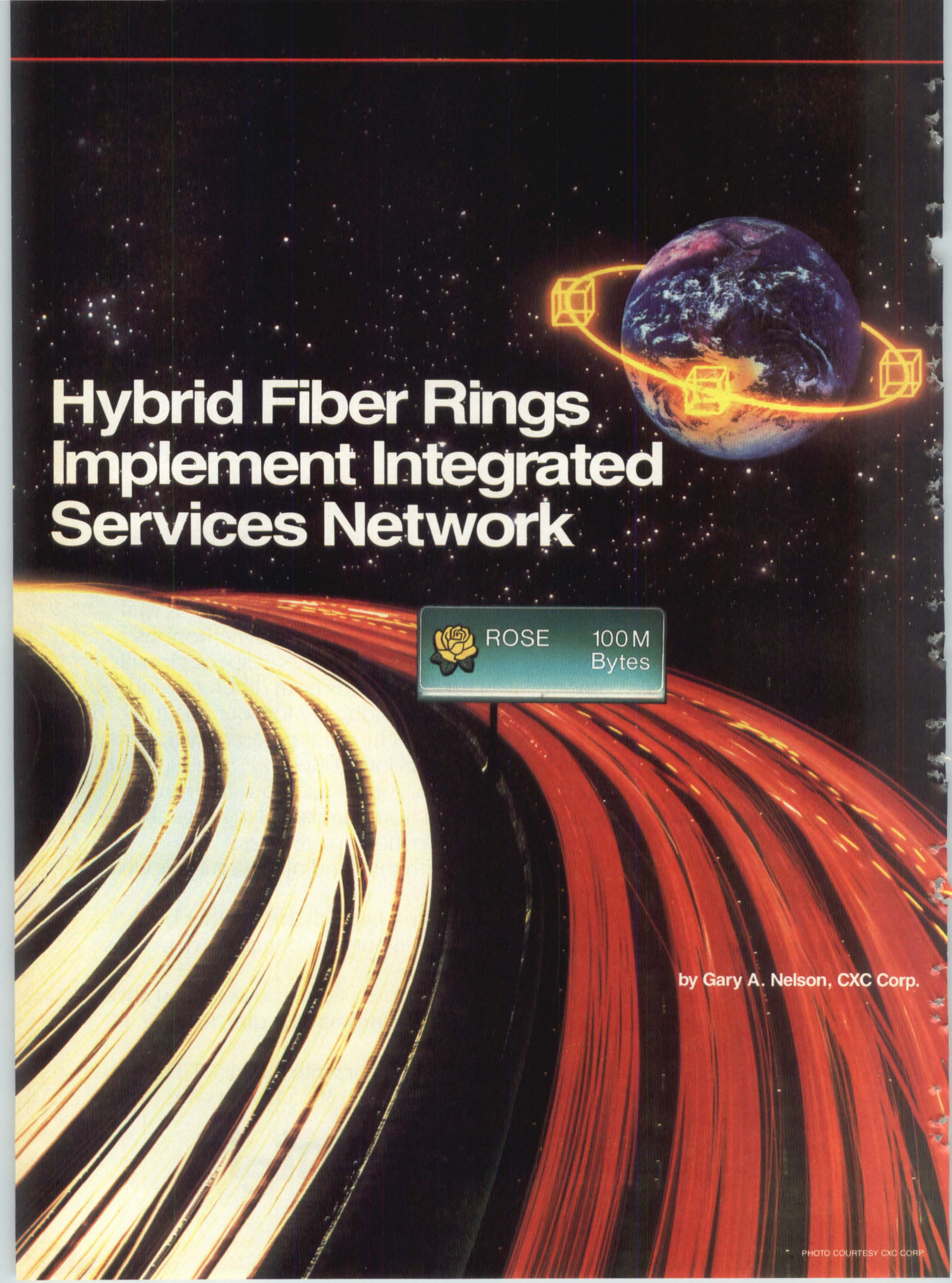

by Gary A. Nelson, CXC Corp.

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Environments such as the office/corporate communications realm pose significant challenges to the vendors of communications equipment. Addressing these challenges, the Integrated Services Local Network (ISLN) represents a new generation of switching machines designed to satisfy requirements for functions that fall between Integrated Services Digital Network (ISDN) primary access, telephony trunk interfaces and desktop station equipment. Eventually, the ISLN will provide a single solution to what are currently separate communication networks: backend networks, backbone networks, local area networks (LANs) and integrated services-private branch exchanges (IS-PBXs).

High-speed LANs such as Hyperchannel, a proprietary network from Network Systems (Minneapolis, MN); Local Data Distribution Interface (LDDI), a 70-Mbit/sec bus; and Fiber Distributed Data Interface (FDDI), a 100-Mbit/sec data-only token ring are examples of backend networks. These networks were designed for mainframe communications.

At present, few backbone ring networks are in production. Proteon's (Natick, MA) 80-Mbit/sec token ring is a notable exception. Also, FDDI promises to serve as an excellent backbone data network when the standard becomes complete and chips become available.

LANs include the familiar Ethernet, the IEEE 802 family, the modest-performance IBM PCNetwork and AT&T Starlan. In a large corporation, departmental LANs can be numerous. For example, an IEEE 802.5 Token Ring can accommodate only 250 stations on one ring. Thus, integrating several 802-type LANs requires a high-speed backbone LAN. Such a LAN must conform to the IEEE 802.2 Logical Link Control interface specification to enable low overhead LAN-to-LAN bridging.

Voice Meets Data

The IS-PBX includes all the various digital voice and data switches. Many PBX vendors now supply proprietary digital station loops that carry both voice and data. In the future, PBXs will handle both proprietary and ISDN telephone equipment. Future standards for the digital station loop will accommodate speeds higher than the present 144 Kbits/sec.

Conventional PBXs are designed around the Time Slot Interchange (TSI), which allows the simple and economical switch-

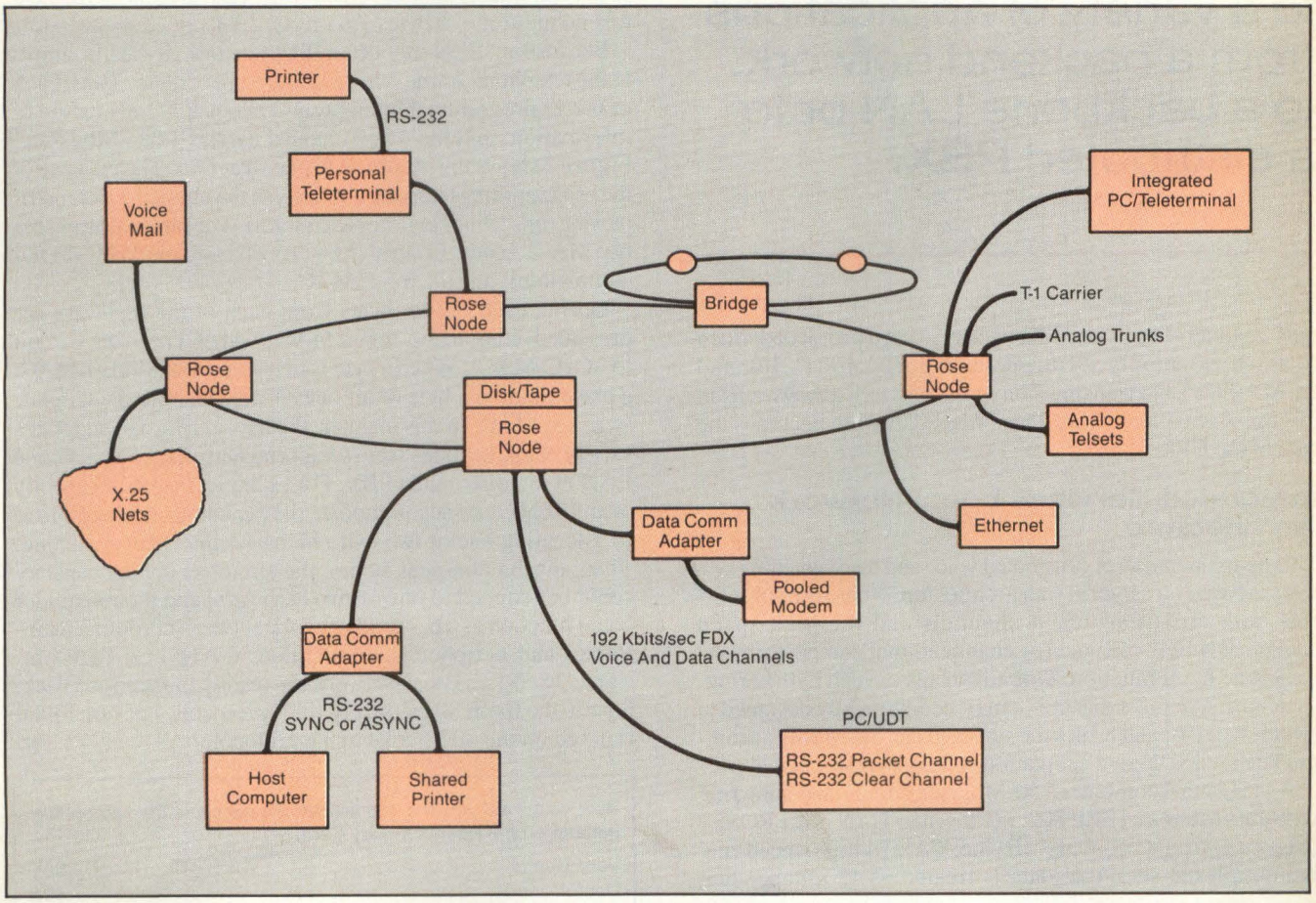

Figure 1: The Integrated Services Local Network utilizes a hybrid ring to provide packet-switching facilities for data communications as well as circuit-switching capabilities for voice communications.

ing of information bytes. However, to accommodate the rates adopted by the new V.110 standards, the TSI switch and existing designs require the use of a full 64-Kbit/sec time slot to carry a 4.8-Kbit/sec communication.

At the present stage of development, ISDN standards define an all-digital network and two access methods. The two access standards are for basic access—the Digital Subscriber Loop (DSL)—having an information capacity of 144 Kbits/sec. Each DSL has both a 16-Kbit/sec packet-switching channel, called the D-channel, and two circuit-switched bearers, or B-channels, each running at 64 Kbits/sec. Basic access defines a four-wire S or T interface operating at 192 Kbits/sec in addition to a two-wire interface. Specifications for the two-wire interface are not yet solidified.

Primary access provides Customer Premises Equipment (CPE) with access to the network at speeds of 1.544 Mbits/sec and 2.048 Mbits/sec. In primary access, the packet-switching D-channel operates at 64 Kbits/sec, and the number of B-channels is 23 or 30. B-channels can carry PCM encoded voice or data. Standard rate data transmissions are carried in a "sub-

The hybrid ring can adapt to a variety of applications from a backend network, to a backbone LAN or to a distributed PBX.

rate" channel of 8, 16, or 32 Kbits/sec, using a protocol defined by three essentially identical standards: I.461, V.110, and ECMA-102. Data transmission in the network always runs in multiples of 64 Kbits/sec. Thus, rate adaptation becomes the task of the CPE.

Integrated Services Local Network Architecture

This new generation of distributed voice and data switching systems is based on a hybrid ring architecture where the ring carries both circuit-switched channels and the high-speed packet-switching channel (or channels) that can perform the backbone LAN function. One advantage of such hybrid ring-switching systems is that they can be economically designed to switch 1-, 2-, 4-, and 8-bit time slots and can thus easily accommodate the ISDN rate adaptation schemes mentioned above.

An ISLN that combines a 50-Mbit/sec circuit-switching ring with a 10-Mbit/sec IEEE 802.3 (Ethernet) LAN is the ROSE* (**Figure 1**) from CXC Corp. (Irvine, CA). Its high-speed ring is multiplexed such that data is treated as 12 independent

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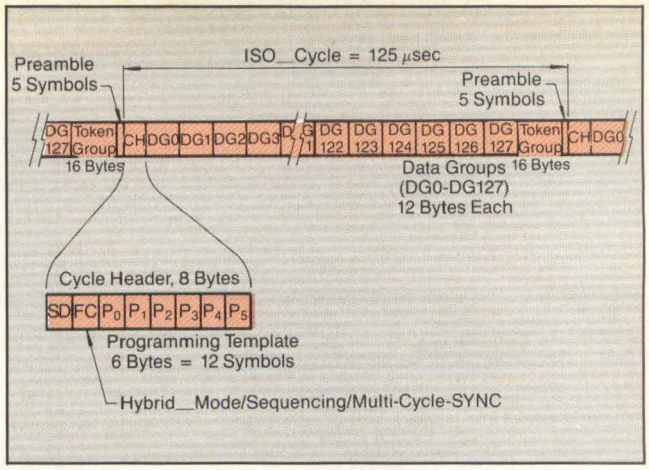

Figure 2: The proposed frame header for the Integrated Services Local Network supports a 125-μsec frame for PBX functions.

highways of 4.096 Mbits/sec each. Eight highways are dedicated to circuit switching while four serve to transport packet ring protocols such as the 4-Mbit/sec, 802.5 token ring.

CXC Corp. has proposed that the ANSI X3T9.5 committee incorporate such a multiplexing scheme in the physical layer of the 100-Mbit/sec FDDI token ring. This proposal has garnered considerable support as a candidate for an ISLN standard. The hybrid version of FDDI maintains the 100-Mbit/sec rate and converts the physical layer to a slotted ring with one of two formats: 12 programmable slots of 1024 bits (128 bytes) each and one permanent token-ring slot of 16 bytes (1.024 Mbits/sec); or 16 programmable slots of 768 bits (96 bytes) and one permanent token-ring slot of 6 bytes (768 Kbits/sec).

Because an ISLN supports a PBX function, it must conform to the telephony frame rate of 125-μsec per frame. Thus, each of the 12 programmable highways carries 8.192 Mbits/sec of information, and the token channel carries 1.024 Mbits/sec. **Figure 2** shows the proposed frame structure. The purpose of the programming template is to refresh the physical layer multiplexing (or sorting) logic for each frame. The physical layer sees two Media Access Control (MAC) ports: a Token MAC (FDDI compatible), and a Circuit MAC.

During each frame, bytes from each of the highways are presented either to the Token MAC (T-MAC) or to the Circuit MAC (C-MAC). When a byte is presented to the Token MAC, a place holding a byte of all ones is presented to the Circuit-switched MAC. In this manner, the hybrid ring can adapt to a variety of applications from a backend network, to a backbone LAN or to a distributed PBX. For example, the voice capacity of an ISLN could accommodate the peak hour voice call load by allocating one or two extra highways to circuit switching. Then, during non-peak hours, the circuit switching capacity could be reduced to one or two highways, and the remainder could function as a backend network between corporate mainframes and peripherals. In addition, the Hybrid FDDI Integrated Services Local Network can readily function as a backbone to the IEEE 802 family of LAN protocols, because FDDI is based on the 802.5 token-ring protocol. DD

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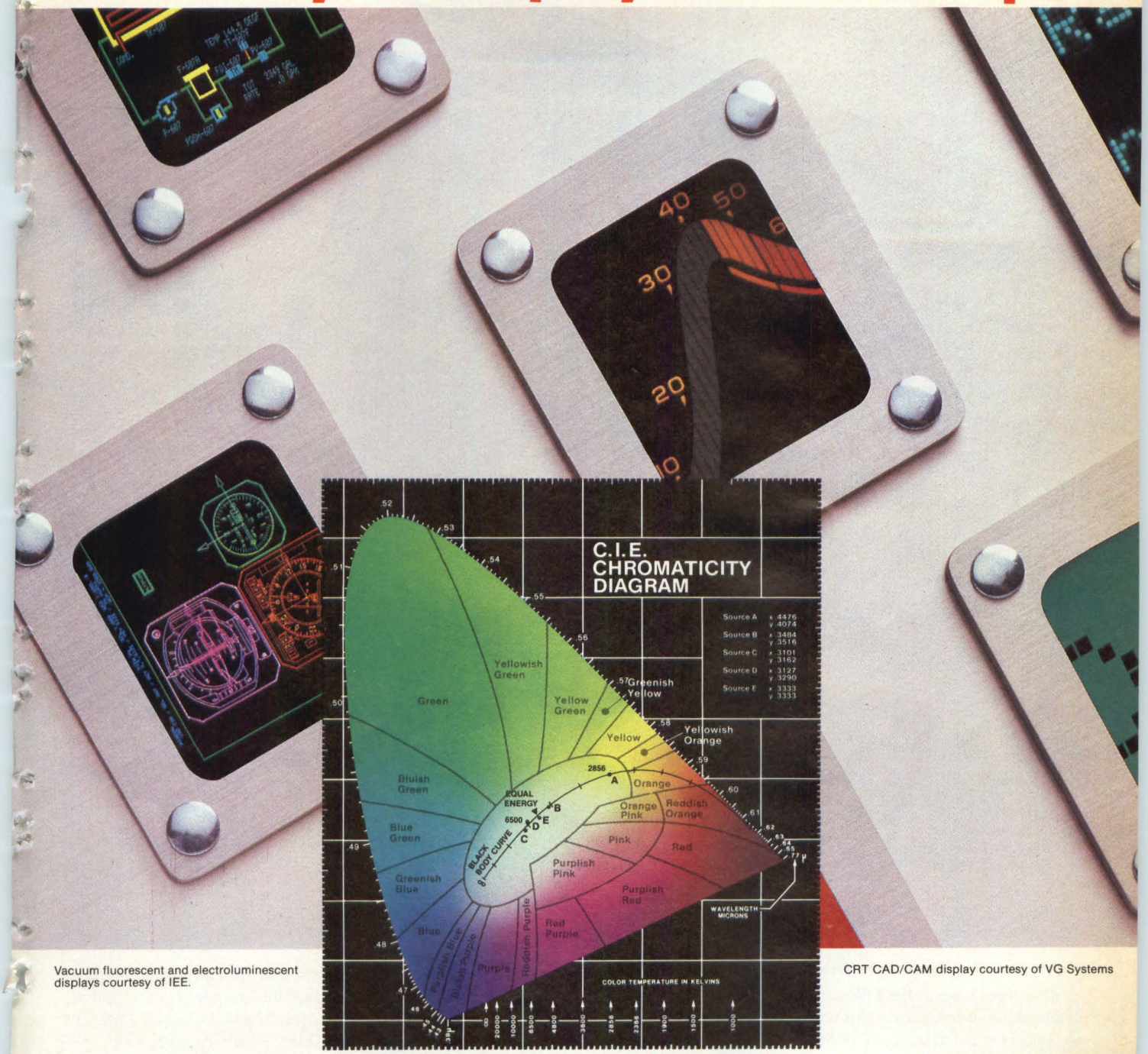

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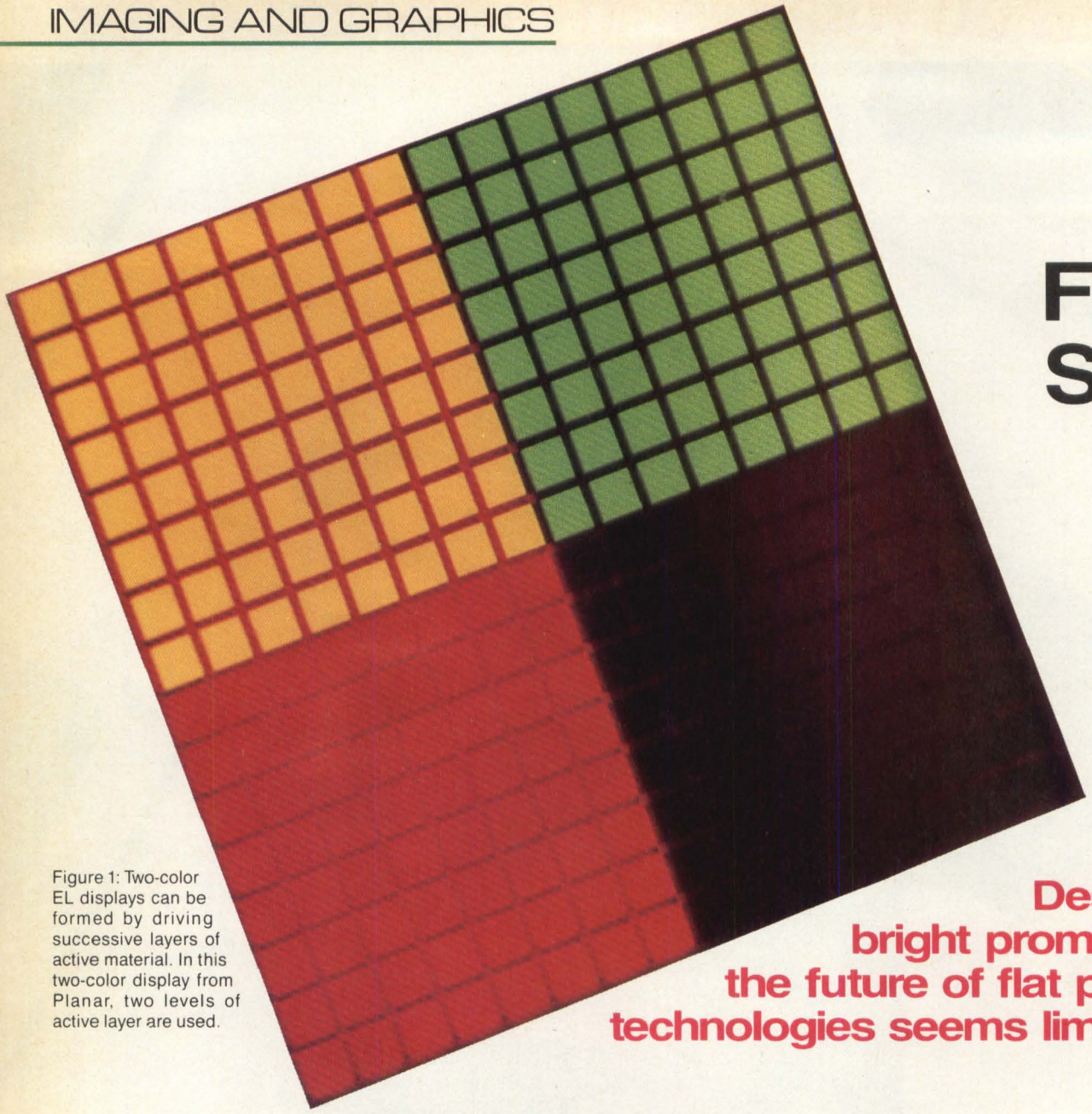

Figure 1: Two-color EL displays can be formed by driving successive layers of active material. In this two-color display from Planar, two levels of active layer are used.

Despite bright promises, the future of flat panel technologies seems limited.

In George Orwell's **1984**, Winston Smith gazed at an oblong metal plaque attached to his wall. Ever since, the futuristic concept of the "telescreen" or flat-panel display has intrigued researchers, manufacturers and consumers with the promise of a low-power, bright, high-resolution replacement for the CRT.

To accomplish this flat-panel goal, technologies such as liquid crystal, vacuum fluorescent, plasma, electroluminescent and even flat CRTs have been put to use with limited success. State-of-the-art CRT technology is a primary reason for the low market share of flat-panel displays. Currently, it is possible for high-resolution monitors to display 2448 × 2048 pixels with 70 Cd/m^2 brightness, 0.15 mm dot pitch and misconvergences as low as 0.1 mm. Flat panels, on the other hand, can only display one quarter of this information, usually at much lower brightness levels, albeit using a fraction of the power of their CRT counterparts.

And, despite the introduction of consumer products such as flat-screen personal computers and portable, battery-operated televisions, flat-panel displays have not emerged as CRT replacements except in areas such as military and automotive applications. In these applications, the low-power consumption, high reliability and medium resolution of the displays present systems integrators with a viable CRT alternative.

Despite their presently limited applications, flat-panel researchers continue to seek the elusive CRT replacement. Although the large scale application of high-resolution flat panels is distant, research points to several ways in which these types of displays can be fabricated.

Rocky Road For Liquid Crystal

Poor brightness, limited viewing angles and slow response times at low temperatures have plagued developers of liquid crystal displays (LCDs). Early LCD designs used twisted-nematic liquid crystals sandwiched between crossed polarizers and an electric field. In the "off" state, the light passes through the first polarizer, is twisted through 90° by the liquid crystal and passes through the second polarizer oriented at 90°. Upon application of an electric field, the rod-like crystals change orientation and no longer twist the light. These types of display

Panel Displays: In The Future

by Andrew Wilson, Senior Technical Editor

suffer from a dull gray look due to the presence of polarizers which are also responsible for the limited viewing angle.

Because of this, many manufacturers are turning to dynamic scattering methods in which the liquid crystal itself is responsible for the passing and blocking of the light. In this method, no polarizers are needed since the application of the electric field is all that is needed to switch the LCs into a random state to block light. The resulting displays have better contrast and viewing angle because no polarizers are used.

Another mode of LC transitions relies on the ability of the liquid to change phase when heat is applied. These displays consist of two glass plates with smectic liquid crystals held between them. Etched to the front glass are vertical, indium tin oxide electrodes while the rear plate has horizontal heating filaments. Each horizontal and vertical crossing represents one pixel. Although this type of display is non-volatile, power requirements are substantial.

Despite the disadvantages of twisted-nematic displays, they are the most widely used LCDs currently available. High-contrast, low-voltage operation and ease of multiplexing in large panel displays are prime twisted-nematic benefits. Indeed, over 10 manufacturers have now introduced twisted-nematic displays with resolutions ranging from 64 × 320 to 200 × 640 displayable pixels.

Using twisted-nematic techniques, work on full color LCDs is under way at several companies. At Citizen Watch (Saitamaken, Japan), a prototype 110 × 340-pixel color LCD has been demonstrated with a dot size of 0.15 × 0.354 mm. In the panel's construction (**Figure 2**), two groups of 55 × 340 pixels were fabricated and joined to form the complete 110 × 320 panel. Switching of the panel is accomplished by IC drivers formed on the glass substrate. According to Citizen, this structure can also be implemented using an active matrix approach in which the liquid crystal would be addressed by a layer of thin film transistors mounted onto a transparent substrate.

At Matsushita (Osaka, Japan) a multi-gap color twisted-nematic LCD has been developed to reduce the effect of rotary light dispersion. In the design, three RGB cell gaps are formed by using different thicknesses of filter. A uniform optical path length for red, green and blue wavelengths is maintained.

While many manufacturers are attacking the problem of video-speed LCDs, others are seeking to replace the CRT in personal computer-type applications. With the introduction of the DG/One, Data General (Westboro, MA) produced the first

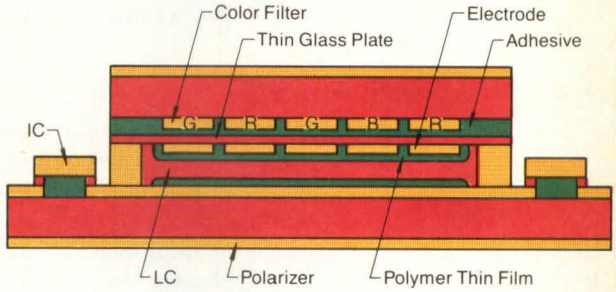

Figure 2: Citizen's color LCD panel, which is shown in cross section, uses two groups of 55 × 340 panels to achieve a total pixel count of 110 × 340 pixels.

portable computer with a full-sized LCD. With displays produced by Matsushita, Hitachi (Chicago, IL) and Epson (Torrence, CA), the PC received a lukewarm market reception. Many felt that the computer's display exhibited low viewing angle and low brightness. Data General will offer the PC with an electroluminescent (EL) display later this year.

Problems with the too-early introduction of the LCD PC have not, however, hindered its development. Two novel designs from Polaroid (Cambridge, MA) and Standard Telecommunications Labs (STL) (Harlow, Essex, UK) increase the brightness and viewing angle of the LCD. Although much of the Polaroid work remains proprietary, the company is offering a flexible plastic LCD 0.015" thick that can be custom produced

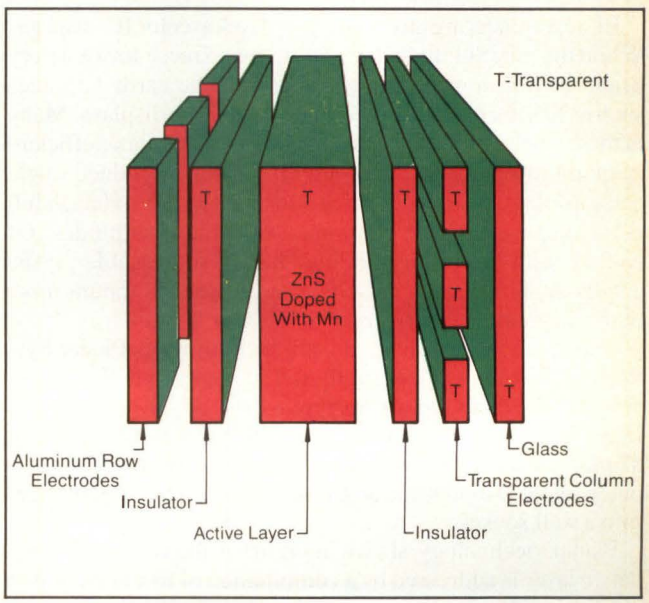

Figure 3: To obtain color from Planar's EL display, the layers would be repeated three times with different active layers which would emit the three primary colors.

up to 16" wide by virtually any length (*Digital Design*, September 1985, p. 13).

At STL, the dynamic scattering effect has been used to produce a 420 × 780 LCD pixel panel with a hemispherical viewing angle and a contrast ratio of greater than 8:1. In the design a custom merged-technology, 30 channel, 350V IC was developed to drive the panel. And although the time for a full page panel write is 0.84 sec, the display consumes just 5W. These types of displays will directly replace the CRT in a number of specialized applications.

Bright Prospects For EL

Electroluminescent effects were first observed some 50 years ago in zinc sulphide. Since then, work in both ac and dc excitation from managanese-doped zinc sulphide thin films has yielded displays of medium resolution with high brightness levels. Unlike liquid crystal displays, the EL display requires high modulation, write and refresh voltages, placing heavy demands on semiconductor driver technology. And, although drivers are becoming available from such companies as Siliconix (Santa Clara, CA) and Texas Instruments (Dallas, TX), driver technology has heretofore held back the progress of large, efficient and bright electroluminescent displays.

Driver technology has held back the progress of flat panel displays.

EL researchers are also striving to develop color EL displays. While the zinc sulphide doped with manganese forms a very bright yellow-orange display, other alkaline earth sulphides such as $SrS:CeF_3$ can be used to produce blue displays. Many of these sulphides, however, cannot offer the luminous efficiency of zinc sulphide and have not been used to produce single color displays. Instead, research has centered on producing full color displays using a combination of these sulphides. Of course, with three times the number of addressable pixels, display manufacturers must find novel ways to mount three times the number of drivers onto the display packages.

One of the leaders in EL display technology is Planar Systems (Beaverton, OR). Recently, the company signed an agreement with Data General to replace the LCD panel in the DG/One personal computer with Planar's 640 × 200 EL display. Data General will now offer two versions of the computer, an LCD model and an EL model which must be plugged into a wall socket.

Planar's technology, shown in **Figure 3**, illustrates how each active layer is addressed by a combination of row and column electrodes. In the structure the patterned transparent front column electrodes are made up of indium tin oxide (ITO), with the phosphor layer sandwiched between two dielectric insulating layers, followed by the intersecting aluminium row electrodes. A typical display formed using the technology is shown in **Figure 4**. With the display, gray level effects can be accomplished using dithering techniques, although "true" gray-scale capability (in which the intensity of the pixels themselves are modulated) cannot be accomplished. Planar is currently studying color and RGB type EL displays for the Army.

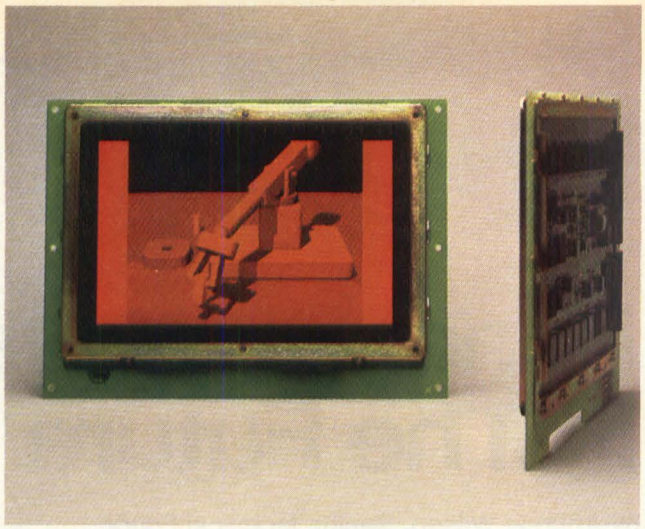

Figure 4: Electroluminescent technology, such as this from Planar, can produce bright displays with dithered gray-scale capability.

In these designs, the construction of **Figure 3** would be duplicated three times, allowing the three alkaline earth sulphides to be switched independently. Convergence in these displays will be almost negligible, since red, green and blue picture elements are colinear. **Figure 1** depicts a two-color version.

Work currently underway at the University of Tottori (Tottori, Japan) has already proven the viability of full-color versions of EL displays. Using thin film deposition techniques, researchers have developed prototypes of displays using the rare-earth doped alkaline earth sulphides CaS (red), SrS (blue) and BaS (yellow/green). Relative brightnesses for the materials used measured about 100, 650 and 350 Cd/m^2, respectively. Luminous efficiency of the materials was also shown to be strongly dependent on the deposition temperature of the films.

Even if full color displays can be fabricated in EL technology, many problems still have to be overcome. Apart from the problems of high-voltage drivers, rare-earth sulphides, sputtering efficiency, gray scale and color, there remains the problem of picture quality. While EL displays are addressed on a by-pixel basis, color CRTs are not. In CRT designs, the electron beam itself is larger than the mask through which it passes to form an image on the CRT phosphor screen.

Because of this, the spot of the CRT beam is somewhat blurred by overlapping pixels, producing a non-spot-like image. In EL displays such as LCD, electroluminescent and plasma displays the image appears dot-like due to the construction of the displays themselves. To overcome this appearance, dot pitch sizes must approach that of CRTs, and antialiasing algorithms must be used to reduce the dot-like appearance of the displays.

Vacuum Fluorescent Displays

As with electroluminescent displays, advances in photolithographic and thick film technologies have resulted in the increased size of vacuum fluorescent displays. Color VFDs have been achieved through the use of novel phosphor elements coated on separate RGB phosphors. Despite these advances,

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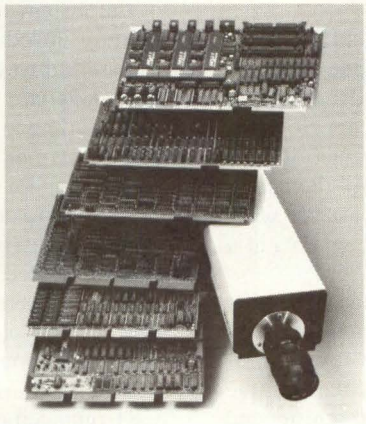

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vacuum fluorescent displays remain perhaps one of the least used technologies in the area of video and graphics. The main reason for this is that it is very difficult to quickly update the VFD. And, many of the pixels "drop out" at these rates causing patchy-looking displays.

One company, Digital Electronics Corp. (Hayward, CA), found VFDs so unreliable that it dropped its line of video VFD panels and retained EL technology as its display medium. According to Bob Christiansen of Digital Electronics, the company is already shipping a 512 × 256 EL panel and will announce a 640 × 200 EL panel in the first quarter of next year.

Surveys of current research efforts indicate a move away from vacuum fluorescent technology. The recent SID symposium, saw only two presentations on VFT. Both were presented by Japanese authors. The first, from Ise Electronics (Ise, Japan), described a 20-character active matrix addressed display. Targeted primarily for cash register and low-information content displays, the VFD from Ise has been designed with 20 ICs mounted on a glass substrate. According to the company, the use of static RAMs in the display elements leads to a highly luminous display which can be switched at relatively low voltages. At Futaba Corp. (Tokyo, Japan), a color graphic VFD panel has been developed with a display resolution of 160 × 120 pixels. Using anode layers coated with red, green and blue phosphors, the display must be driven at voltages ranging from 100V to 200V. Displayable colors of the prototype model were red, green, blue, cyan, magenta, white and black.

Although in a state of relative maturity, research and development efforts still continue in VFD in the areas of matrix addressing. However, as with electroluminescent and plasma displays, high voltage IC drivers need to be developed so that the displays run more efficiently.

Plasma Displays

Over the past decade, neon-based flat-panel plasma displays have been developed to the point where they are finding a variety of applications mainly in the military arena. Perhaps the best known plasma display is the 581 module from IBM (Yorktown Heights, NY).

In its design, IBM used a 960 × 760 pixel panel driven by high-voltage horizontal and vertical line drivers. One of the initial problems with the display was the inability to drive it at fast speeds. Last year, IBM reported that it had developed a 50-frame per sec, non-interlaced 16-MHz interface for the display which could drive a 720 × 350 section of the panel. Now the company has extended this work to allow users to write and erase the panel at twice this speed and accept data at a 40-MHz video rate.

Because of the requirement that panel line updating overlap with loading of video data, the driver modules that were used to accomplish this were SN75553/54 drivers from Texas Instruments (Dallas, TX). Originally designed for EL displays, the drivers have a latch register between the input shift register and the output drivers. These allow overlapped operation. But these drivers were not designed for either the 40V to 90V pulses used in the plasma panels or the panels' load characteristics. Instead, they were used merely to show the panels' video rate potential. Using a CRT controller card developed by Control Systems (Minneapolis, MN), IBM has achieved a 20-msec update of the 750,000-pixel ac plasma panel.

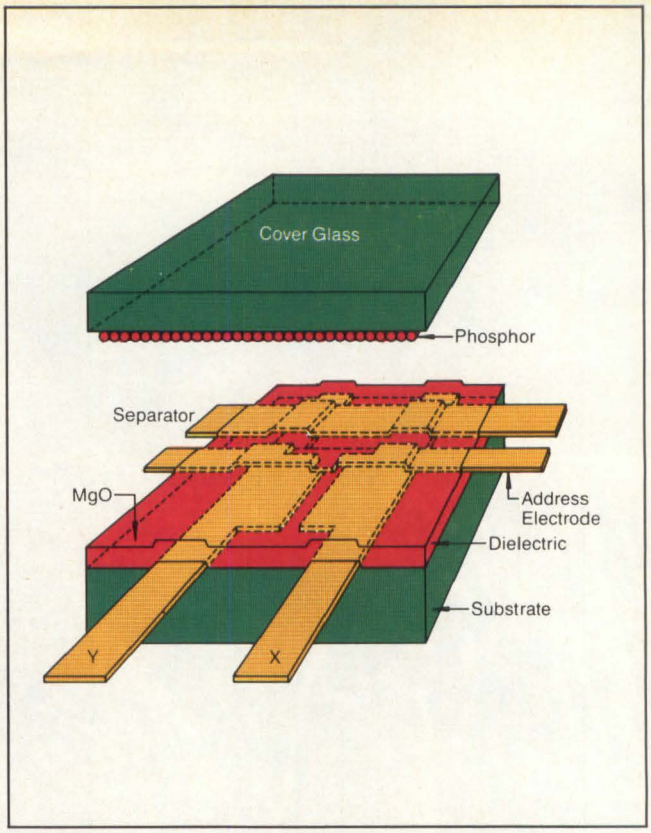

Figure 5: A cross-section of Fujitsu's green surface discharge plasma display shows the panel structure and the electrode pattern.

Other developments in ac plasma technology include the study of new gas mixtures to replace the orange emission associated with Ne-based panels. At United Technologies' Research Center (East Hartford, CT), blue-green Xe_2Cl and green XeO emission has been demonstrated. And at Fujitsu (Akashi, Japan), a neon-xenon mixture has been used to produce a 240 × 80 ac plasma panel. **Figure 5** shows the panel structure and the electrode pattern of the display. In the figure, X and Y are the sustaining electrodes and A and S are an address electrode and a separator. During operation, the panel is driven by the sustain and address drivers. Fujitsu uses a neon-xenon mixture introduced into the display after the cover glass is assembled to the substrate. Zn_2SiO_4:Mn phosphors are deposited onto the cover glass.

According to a recent report from Stanford Resources (San Jose, CA), the flat-panel display market remains at about one-tenth of that for the CRT. And, although different technologies may gain greater acceptance, the market for flat panels will remain at least one-tenth that of that of CRTs for at least the next five years. Because of its low cost per pixel, color attributes, ease of addressability, driver requirements, gray level capability and ease of integration, the CRT will dominate the display market. Although flat-panel displays will find niches in high-reliability, consumer and military markets, the promise of a CRT replacement is still far from a reality. **DD**

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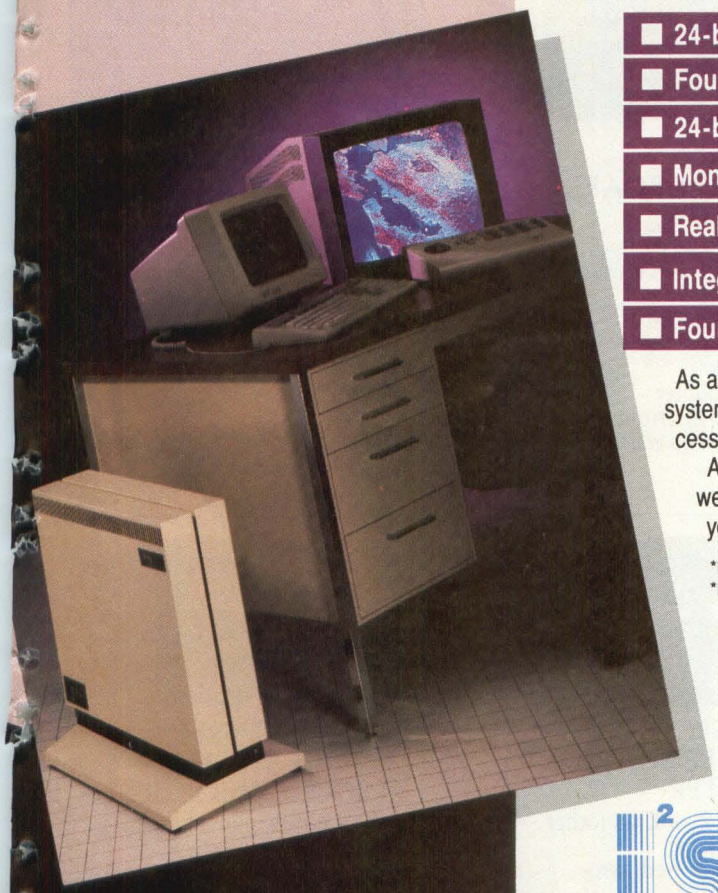

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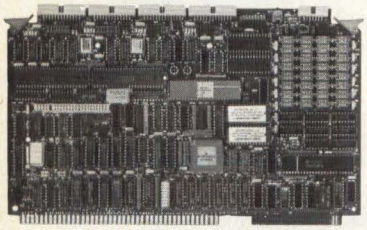

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- (1) iSBX* expansion connector
- (4) 28 pin ROM sockets (up to 256KB)
- Optional memory management
- Omnibyte two year limited warranty

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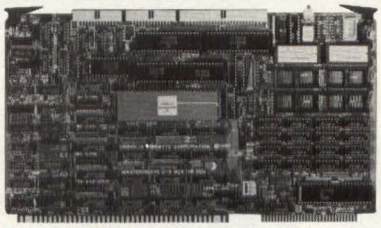

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- A triple 16-bit timer/counter
- (7) prioritized-vectored interrupts
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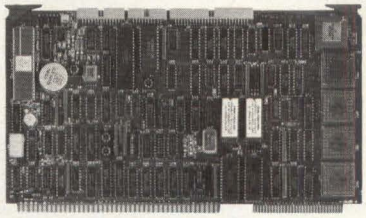

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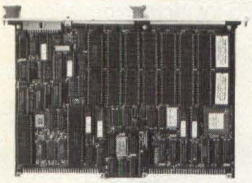

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Floating Point Unit Extends Arithmetic Processing

by Bruce Hoffman and Donald Tietjen, Motorola

In today's marketplace, deciding which floating point coprocessor to use is difficult. But considering a few key points that distinguish coprocessor interface designs can ease coprocessor selection.

First, it must be determined how instructions and operands are passed to the coprocessor. Second, if concurrency exists, main processor and coprocessor timing must be defined. Finally, the designer must be aware of how mid-instruction context switching and coprocessor detected exceptions are handled.

The MC68881 is an arithmetic processor that conforms to the IEEE floating point standards (P754, Draft 10.0). It contains a set of complete transcendental functions. The MC68881 was designed as a 32-bit coprocessor to accompany the MC68020, and includes a 67-bit arithmetic unit, a 0-67 bit barrel shifter and eight 80-bit general purpose data registers. It operates at 16.67 MHz and consumes less than 1W of power. It can also operate as a peripheral processor on an 8-bit, 16-bit or 32-bit data bus, allowing it to serve in systems using the 8-bit MC68008 and the 16-bit MC68000, MC68010 or MC68012.

Communications between the main processor and the MC68881 employ standard M68000 family bus transfers. Since the bus is asynchronous, the MC68881 does not have to run at the same speed as the main processor. The only difference between a coprocessor bus transfer and any other bus transfer is that the MC68020 issues a special function code to indicate CPU SPACE. Using the function code as part of the decode, no memory mapped coprocessor interface registers impinge upon the instruction or data address spaces of the main processor. The coprocessor interface provides a tight coupling between processor and coprocessor. Thus the MC68881 appears to the user as a logical extension of the main processor.

The MC68881 contains a number of coprocessor interface registers that are addressed like memory by the main processor (**Table 1**). The main processor and coprocessor communicate via reads or writes from and to these CPU SPACE registers, in a protocol of bus cycles defined by the M68000 coprocessor interface. For example, the main processor writes a coprocessor instruction to the coprocessor interface command register and then reads the coprocessor interface response register. In this response, the bus interface unit of the coprocessor encodes any additional actions required of the main processor on behalf of the coprocessor. The response may call the main processor to evaluate the effective address, and to transfer "n" bytes of data to or from the coprocessor. Once the processor fulfills all coprocessor requests, it is free to fetch and execute subsequent instructions from memory. This is known as concurrent operation of the main processor and coprocessor. Concurrent instruction execution is limited to those instructions with an on-chip register as a destination.

Following concurrent instruction execution, the response register of the MC68881 can synchronize the main processor by indicating that the coprocessor instruction is not complete. Thus, concurrency is controlled by the MC68881 on an instruction-

A4-A0	D31 D15 D0		
00	Response	R	Informs Processor Of Service Request
02	Control	W	EXC_ACK Or Abort
04	Save	R	Coprocessor ID, # Of Bytes To Be Saved
06	Restore	R/W	Coprocessor ID, # Of Bytes To Restore
08	Reserved		
0A	Command	W	General Instruction Register
0C	Reserved		
0E	Condition	W	Conditional Instruction Register
10	Operand	R/W	Data Reg. Between Coprocessor & Proc.
14	Register Selector	R	Internal Registers To Be Moved
16	Reserved		
18	Instruction Address	R/W	Logical Address Of Instruction
1C	Reserved		

Table 1: The MC68881 contains a number of coprocessor interface registers that are addressed like memory by the main processor.

by-instruction basis and remains transparent to the programmer.

Virtual machine architecture of the MC68020 is supported by the MC68881. If the main processor detects a page fault, or if a task times out, it can force the MC68881 to stop executing and save its complete internal state to memory. The MC68881 minimizes both the average state size and average context switching time of a save command. Three possible state sizes may be saved: reset, idle and busy. If the save instruction is received when the MC68881 is still in the reset state, only one word of state is transferred to memory. The operating system may examine this word to determine that the programmer's model (**Figure 1**) is empty. If the MC68881 is between instructions (in an idle state) when the save instruction is received, 12 words of internal state are transferred to memory. If the MC68881 cannot finish the instruction in less time than saving the busy state size would take, 90 words of internal state are transferred to memory.

The main processor can also force the MC68881 to reload the previously saved state from memory and continue executing the instruction from the point it was interrupted. A restore of the reset state size functions just like the hardware reset pin. Both save and restore commands represent privileged instructions.

Interfacing To The MC68020

The M68000 coprocessor interface allows a simple hardware interface with a well-defined communication protocol between the MC68020 and the MC68881. For systems requiring a reduced bus between the main processor and the coprocessor, the MC68881, in conjunction with the dynamic bus sizing of the MC68020, can operate over an 8-bit, 16-bit or 32-bit data bus.

In the 32-bit connection shown in **Figure 2**, all data lines are used from the processor to the MC68881. The size pin and AO address pin are tied high to configure the MC68881 for operation on a 32-bit bus. In the 16-bit connection, only the 16 most significant bits (MSBs) of the processor's data bus are used. The coprocessor must have D31-D24 to D15-D8 and D23-D16 to D7-D0 strapped to operate on a 16-bit bus and the AO pin must be tied low. An 8-bit connection uses only the 8 MSBs of the processor's data bus. The size pin is tied low and AO address pin is connected to the processor. To operate on an 8-bit data bus, the MC68881 must have D31-D24 to D23-D16 and D31-D24 to D15-D8 and D31-D24 to D7-D0 strapped. The MC68020/MC68881 pair appears to the user as one processor that supports seven floating point and integer data types and has eight integer data registers, eight address registers and eight floating point data registers.

Coprocessor interface overhead is shared between the

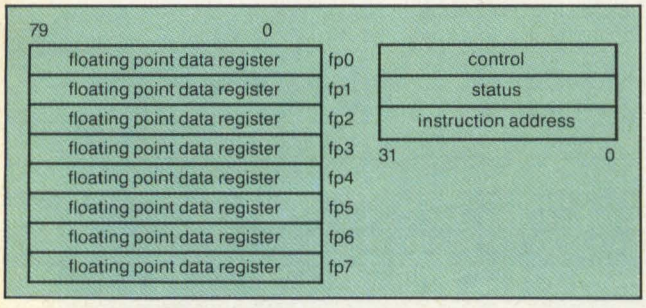

Figure 1: Programmer's model of the MC68881. The virtual machine architecture of the MC68020 is supported by the coprocessor.

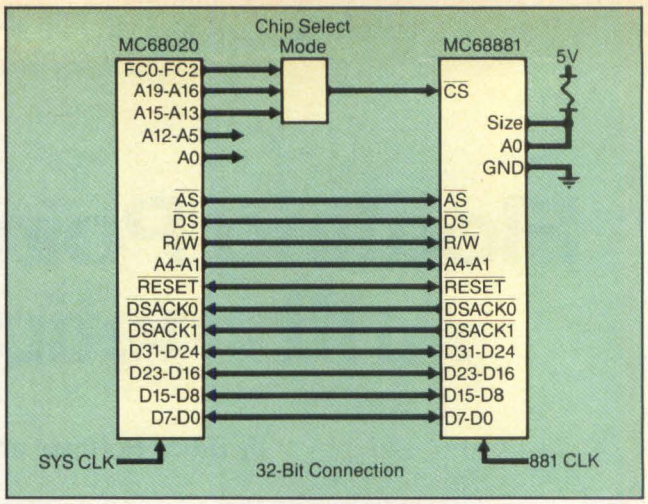

Figure 2: In the 32-bit connection between the MC68020 and the MC68881, the size pin and AO address pin are both tied high.

MC68020 and MC68881. **Figure 3** shows the instruction format for a typical coprocessor instruction. The first word of all MC68020 instructions is the operation word. The MC68020 interprets all F-line instructions as coprocessor instructions. (Instructions with ones in the 4 MSBs of the operation word are known as F-line instructions.) When the MC68020 detects such an instruction, it writes the coprocessor command word to the coprocessor interface command register in CPU space. The function codes of the MC68020 select CPU address space, and address bits A16-A19 specify a coprocessor access in CPU

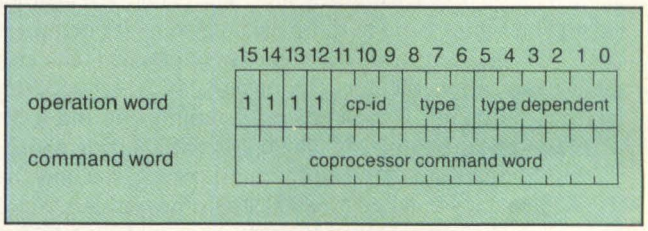

Figure 3: The instruction format for a typical coprocessor instruction. The first word of all 68020 instructions is the operation word.

space. Address bits A13-A15 contain the coprocessor identification extracted from the F-line operation word and A1-A4 distinguish the various coprocessor interface registers of the MC68881. The coprocessor ID field is used to allow up to eight MC68881s in a system.

After the MC68020 writes the coprocessor command to the interface command register, it reads the interface response register. The coprocessor encodes in this response any additional action required from the MC68020 on behalf of the MC68881. The response may request the MC68020 to evaluate the effective address and to fetch an operand from memory. The effective address of the operand is encoded in the operation word and the size of the operand is encoded in the response. After the MC68020 fetches the operand from memory, it writes the operand to the coprocessor interface operand register of the MC68881. Once the operand has been transferred, the MC68020 is free to execute instructions concurrently with the MC68881's instruction execution. If another MC68881 instruction is encountered before the previous instruction has completed, the response encoding instructs the MC68020 to continue polling the response register until the previous instruction completes. The MC68020 is free to sample interrupts while polling the response register.

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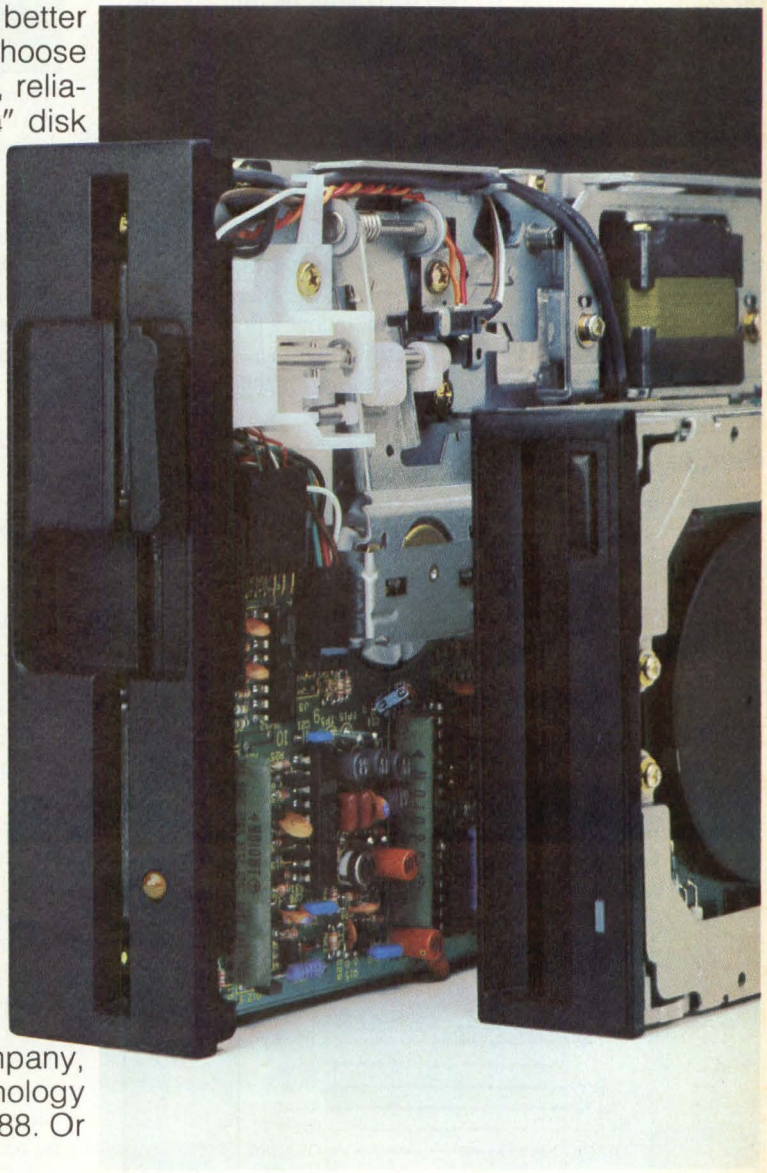

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Runtime Exceptions

Runtime exceptions are unusual conditions arising during the execution of an instruction. An example for the M68000 family of processors is integer divide by zero. When an M68000 processor detects an attempt to divide by zero, normal processing is terminated and exception processing is initiated. This design provides an efficient context switch so that the programmer can handle unusual conditions in an exception trap handler routine.

The MC68881 also detects runtime exceptions such as floating point overflow. The MC68881's control register contains user selectable bits to enable or disable the eight classes of floating point exception traps.

While executing concurrently, the MC68881 may detect an enabled exception. If so, the MC68881 will hold the pending exception until the MC68020 reestablishes communications when it encounters the next coprocessor instruction. The exception is then reported using a response encoding which includes the appropriate vector number. Concurrent instruction execution prevents the exception handling routines from using the MC68020's program counter as a pointer to the offending floating point instruction. The MC68881 maintains a floating point instruction address register for this purpose. Thus, the MC68020 performs exception processing for the MC68881 detected-exceptions.

Emulators

The MC68881 can be used as a peripheral processor in any system using M68000 asynchronous bus transfers. **Figures 4** and **5** show the hardware connections for 8-bit and 16-bit processors. The main processor must emulate the protocol of bus cycles which make up the M68000 coprocessor interface implemented in the MC68020. While software emulation of the coprocessor interface produces some performance degradation, system performance is still higher than with comparable floating point software packages. The MC68881's execution time remains the same once the coprocessor interface emulation delivers instruction and operands. Chip select logic of the MC68881 is system dependent in the peripheral mode because the interface registers must be mapped into a data address space. After selecting the MC68881, the emulator must complete the protocol of reading or writing one of the internal registers of the MC68881.

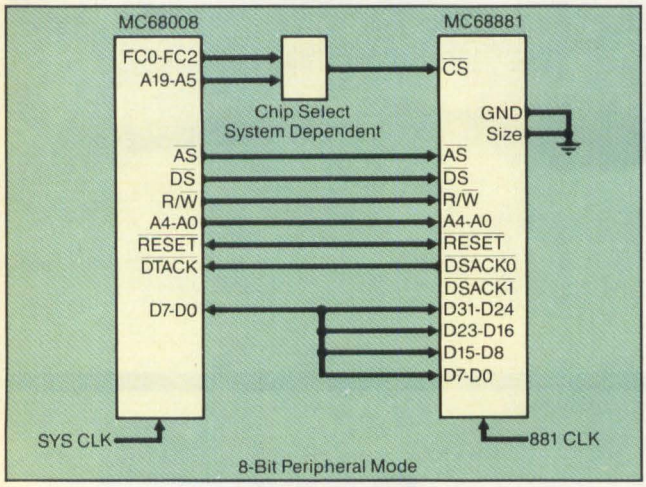

Figure 4: The coprocessor can be used as a peripheral processor in any M68000 system using asynchronous bus transfers. Shown is the hardware connection for an 8-bit machine.

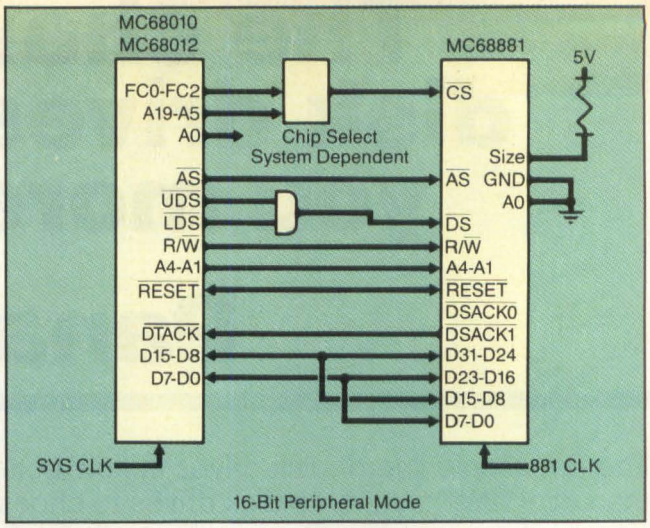

Figure 5: The hardware connection enables the MC68881 to function as a peripheral processor for a 16-bit machine.

In M68000 systems using the MC68881 as a peripheral processor, there are two techniques for emulating the M68000 coprocessor interface in software. These are F-line instruction emulation and in-line code emulation (macros or subroutine calls). These techniques trade-off performance degradation, with upward compatibility of software, when upgrading to an MC68020/MC68881 system.

The 8-bit and 16-bit members of the M68000 family of processors take a unique exception trap when encountering an F-line instruction. F-line instruction emulations of MC68881 instructions are much slower than in-line code emulations. The processor must service the exception, decode the MC68881 instruction format and decode the MC68881's response register encodings. However, this technique provides object code upward compatibility which the in-line code technique cannot provide. Designers who plan to upgrade to the MC68020 processor should use this approach. When the MC68020 detects an F-line instruction, it will not take an exception trap. The MC68020 will utilize the on-chip coprocessor interface to communicate with the MC68881. This significantly increases system performance and no software has to be reassembled or recompiled.

In-line code technique is much faster than F-line instruction emulation. This technique only permits the source code to be upward compatible to the MC68020-based systems. For example, the in-line code for an MC68881 instruction (register-to-register) could be two MOVEs and a branch generated by a macro. Thus, when assembly or compilation expand the macro, the object code will access the MC68881 as a peripheral processor. To port this code to an MC68020-based system, which accesses the MC68881 as a coprocessor, the source code must be reassembled or recompiled with a redefined macro. The redefined macro would then expand to the appropriate F-line instruction recognized by the MC68020 as a coprocessor instruction. DD

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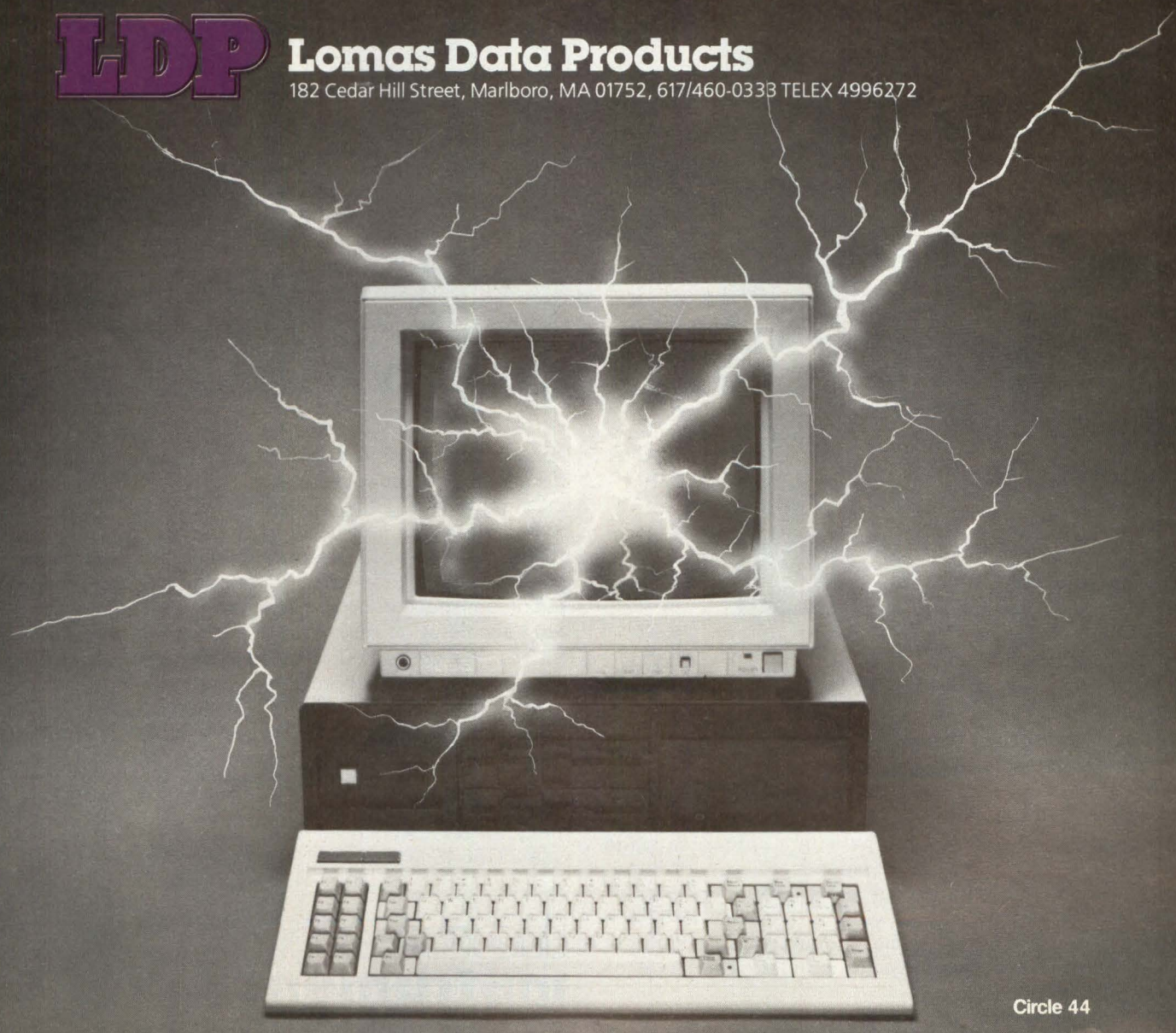

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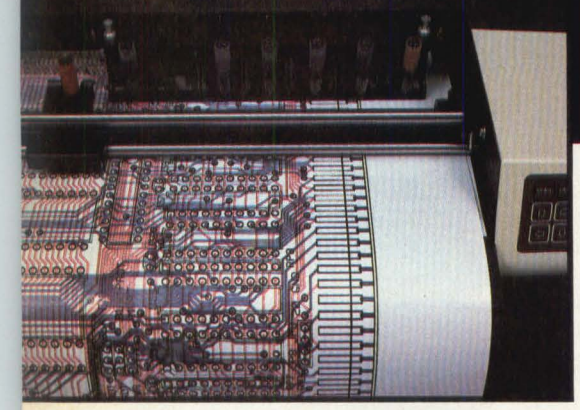

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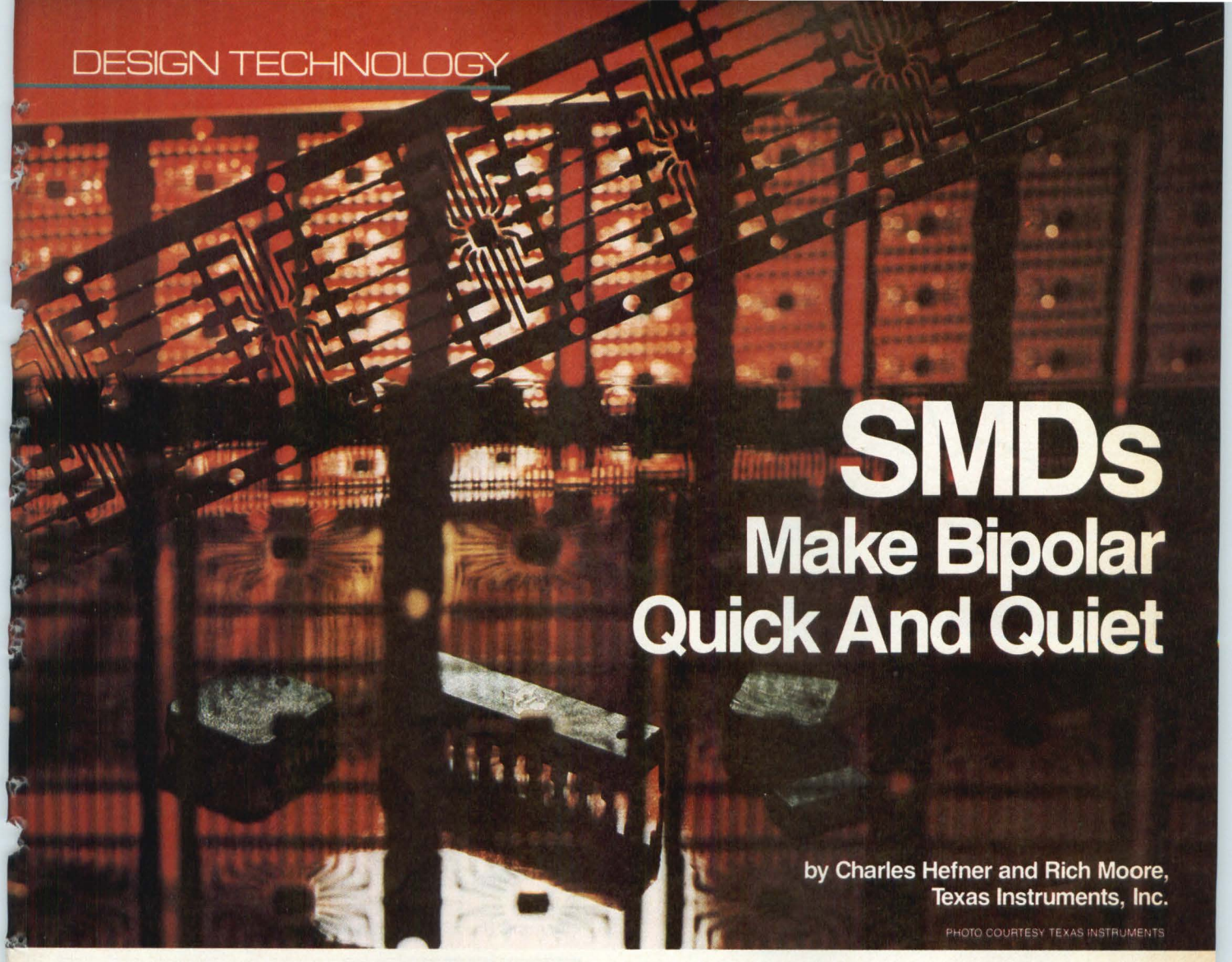

SMDs Make Bipolar Quick And Quiet

by Charles Hefner and Rich Moore,
Texas Instruments, Inc.

PHOTO COURTESY TEXAS INSTRUMENTS

To get the highest system-level performance from advanced bipolar logic, designers should consider not only the device itself, but also the device's packaging. Less than optimum system performance often results from poor package choice.

The original TTL family used the dual-in-line package (DIP). With rise and fall times of approximately 7 nsec or greater for light loads, the TTL family readily lent itself to the standard DIP. Oxide-isolated bipolar processes, however, have spawned development of logic families with rise and fall times as fast as 2.5 nsec for a standard 50 pF load (Advanced Schottky and Advanced Low Power Schottky). Standard DIPs may not satisfy the designer's high-performance needs.

The new generation of surface mount devices (SMDs) includes both small-outline (SO) packages and plastic leaded chip carriers (PLCCs). A comparison of such SMD packages with DIPs shows that DIPs have larger parasitic impedances because of longer leadframe interconnections. Leadframes have finite resistance, inductance and capacitance.

Self-inductance is the major culprit of high-frequency problems, causing ground bounce, V_{CC} noise, pin-to-pin crosstalk and lower noise-margin problems. These effects only become worse as the operating frequency of the device increases. Reducing the parasitic inductance by shrinking the size of the packages can help to avoid the associated complications.

A comparison of DIP leadframes to SO and PLCC packages shows reduced lead length for the smaller packages. Actual measurements (**Figure 1**) verify that the longer leads have more self-inductance. For example, the self-inductance for a 16-pin DIP varies from about 3.5 nH to 11 nH. End pins exhibit the maximum values. This is unfortunate because these terminals are the standardized ground and V_{CC} pins in TTL families.

Any deviation of the chip's ground from a quiescent value of 0V is considered ground movement or ground bounce. Ground movement is the major problem in standard packages of TTL circuits. Although moving the ground and V_{CC} to centrally located pins would result in a reduced inductance and voltage drop, it would also result in a nonstandard pin configuration. Placing the ground pin in a corner of a DIP is too widely accepted a practice for central placement to be considered.

A 16-pin SO package's self-inductance profile is similar to that of a miniature DIP package. The PLCC package has a flatter, more uniform, lead self-inductance plot. The PLCC package has leads on four sides, resulting in a more even inductance distribution than DIPs. Since both the DIP and the SO packages have leads on only two sides, both have similar self-inductance profiles. Size differences make the SO package values proportionally smaller than those of the DIPs.

Interestingly, 14- and 16-pin SO packages have less lead inductance than 20-pin equivalent PLCCs. However, as pin count increases, 28-pin PLCC packages present less lead self-inductance than 24-pin SO packages. This occurs because the SO package leads become longer, similar to those of a DIP.

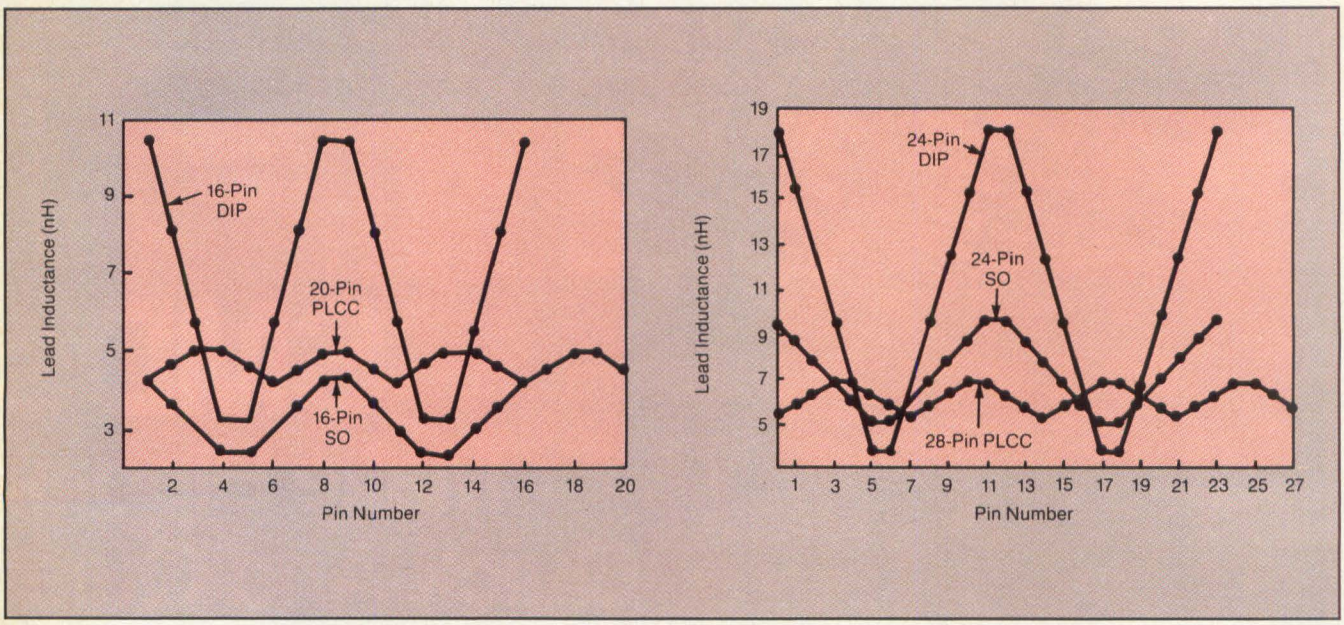

Figure 1: These two plots illustrate the electrical advantages of surface mount technology. Package leadframes have finite resistance, inductance and capacitance and affect circuit performance by inducing ground bounce, V_{CC} noise and pin-to-pin crosstalk and by lowering high-frequency noise margins. Physically smaller packages offer smaller package parasitic impedances.

To illustrate the effects of self-inductance, consider an SN74AS00 with a standard 50 pF load, and an output waveform transition fall time of about 2.6 nsec. Ground movement peaks at 0.374V in an SO package with 3.8 nH parasitic ground pin inductance (**Figure 2**), compared to 0.663V and 10.2 nH in a DIP.

Ground Movement Effects

Ground movement voltage was calculated to a first order approximation from the equations (see box). Simultaneously switching outputs can cause ground movement to become quite large. Factors affecting the magnitude of this voltage include current spiking (caused by totem pole overlaps), rise and fall times of output waveforms, internal circuit design and the package's parasitic inductances. IC designers must consider and adjust these factors to optimize the circuit's simultaneous switching performance. Placing the power pins on the corners of DIPs results in greater ground movement associated with output voltage transitions than in smaller surface mount packages.

In an Advanced Schottky device that uses an SO package, the reduced internal lead self-inductance decreases ground movement and thus enhances high-frequency performance. This conclusion is based on a comparative study of the effects on propagation delay. When only one of four NAND gates in an SN74AS00 is switched, the propagation delay of the SO-packaged device is approximately 12% less than that of a DIP device (**Figure 3a**). When all four gates are switched simultaneously, the difference between the propagation delays of the two types of devices becomes 15% (**Figure 3b**).

In another test, the frequency of the input to an SN74AS00 gate was increased and the output waveform observed. The frequency at which single gates could switch was determined for both the DIP and SO package and plotted (**Figure 4**). This was done without violating the criteria of 2.0V as the lowest logic high voltage and 0.8V as the highest logic low voltage. SO pack-

Equations For Approximating Ground Movement Voltage

$V(t) = L\, di/dt$
$i(t) = C\, dV_O/dt$
$V(t) = LC\, d^2V_O/dt^2$

where

$V(t)$ = voltage across the parasitic inductance
$i(t)$ = current through the parasitic inductance
L = parasitic inductance
C = load capacitance
V_O = output voltage

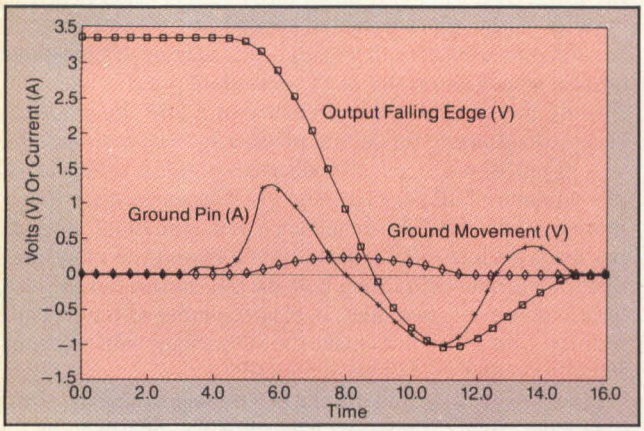

Figure 2: The ground movement and parasitic ground pin inductance for an SO-packaged SN74AS00 are significantly less than those for a similar device packaged as a DIP. Waveform degradation is directly proportional to the amount of ground movement.

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ages exhibited a 20% improvement in frequency operation over that of DIPs.

Similarly, a comparison of two hex NAND gate 48 mA drivers, the SN74AS808BN and the SN74AS1808N, shows the advantages of reducing the ground pin parasitic inductance inside the IC package. Moving the ground pin of the SN74AS808BN, which is at a corner (pin 10) of a 20-pin DIP,

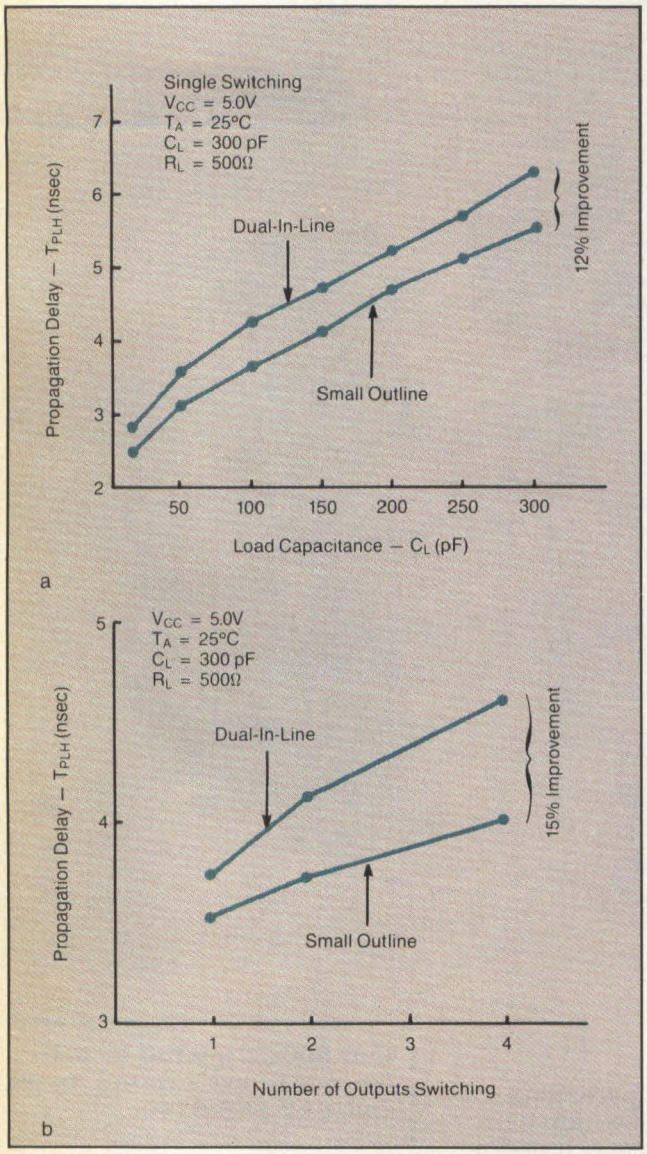

Figure 3: The data indicate a 12% improvement in propagation delay between a DIP and SO package when only one of four NAND gates in a SN74AS00 is switched. This improvement rises to 15% when all four gates are switched.

to a center pin (pin 5), similar to the configuration of the SN74AS1808N, causes a drop from 13.7 nH to 3.4 nH in the parasitic ground lead internal inductance. This difference permits simultaneous switching of all 48 mA outputs while driving large capacitive loads, with less waveform degradation for the SN74AS1808N (**Figure 5a**) than for the SN74AS808BN (**Figure 5b**).

Waveform degradation is the product of the chip's ground

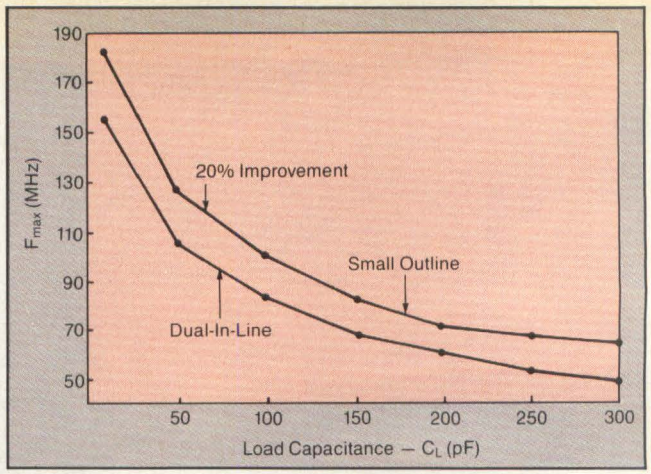

Figure 4: The plot compares the F_{max} performance as a function of load capacitance for the SN74AS00, a quad 2-input NAND, when packaged in a DIP or SO package. F_{max} is defined as the frequency at which the output waveform violates either V_{OHmin} or V_{OLmax}. SO packages typically show a 20% improvement in F_{max} performance for the SN74AS00.

voltage moving to the point where the input voltage appears to be at an opposite logic state with respect to the device's internal threshold. When this occurs, the SN74AS808BN NAND gate's output begins to switch from a high to low state. If the ground voltage starts returning to its quiescent state of 0V, the output waveform recovers. For a given worst case transition, the amount of output waveform degradation is directly proportional to the magnitude and duration of the ground movement.

An often overlooked cause of output waveform degradation is improper decoupling of the device packages. Decoupling a

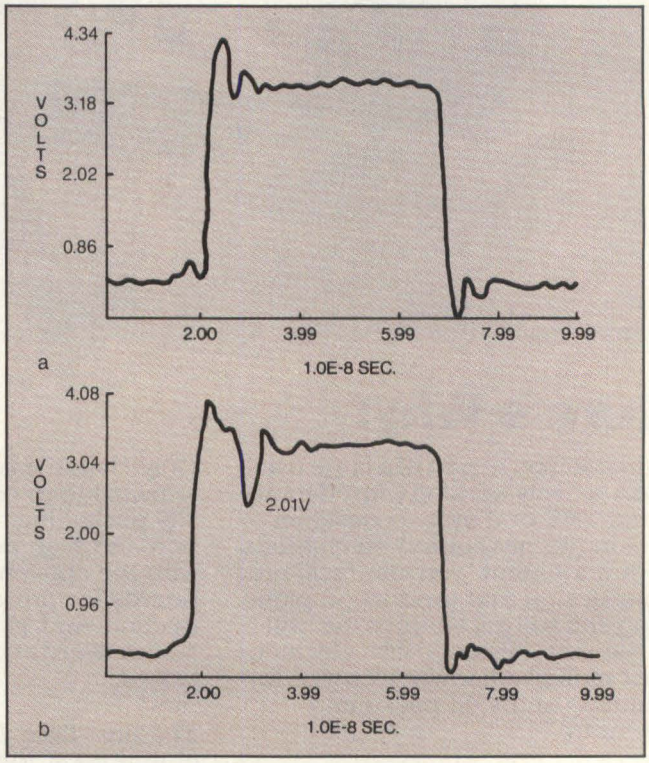

Figure 5: The ground pin of the SN74AS1808N is located at the center of a 20-pin DIP. The SN74AS1808BN is functionally similar to that device; however, the ground pin is located at a corner. Changing the placement of the ground from the corner to the center of the device lowers the parasitic ground lead internal inductance, thus reducing output waveform degradation.

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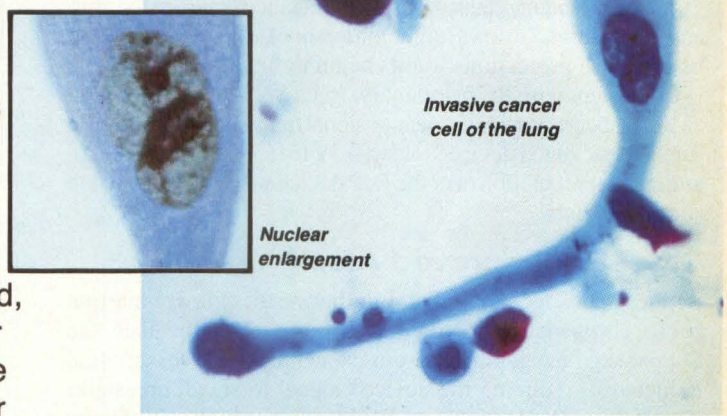

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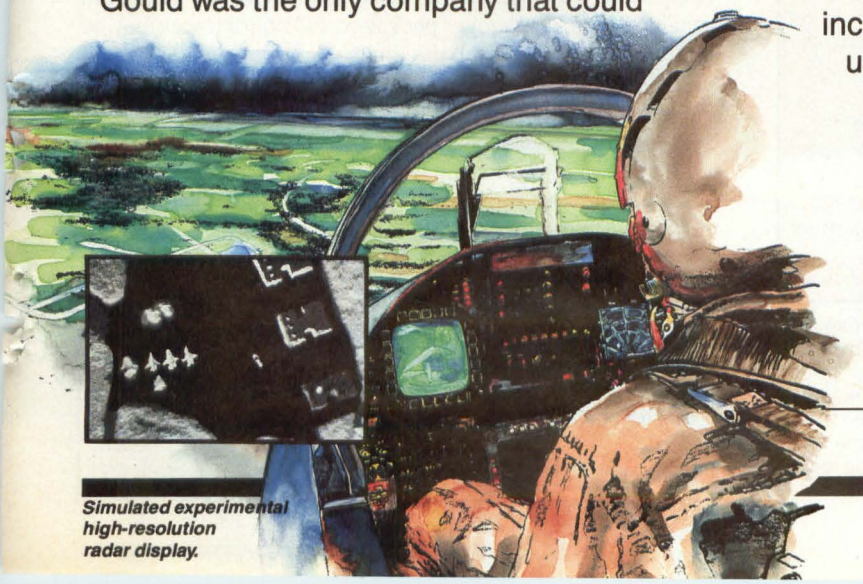

Simulated experimental high-resolution radar display.

GOULD
Electronics

Circle 15

device's V_{CC} pin to ground can greatly reduce degradation caused by V_{CC} noise. The decoupling capacitor reduces the noise generated on a V_{CC} pin due to the pin's inductive effect and the V_{CC} bus. Decoupling every chip on a printed circuit board is recommended even for surface mounted devices.

Reducing Undershoot

Any signal path can be viewed as a transmission line when the path's propagation time is much longer than the signal's rise and fall time. A long path propagation delay results in reflections that cause the effects seen in **Figure 5**: overshoot, undershoot and ringing.

To alleviate signal deterioration, Advanced Schottky TTL devices use input and output clamp diodes to enable operation over long delay paths. Other devices use a 0V clamp circuit to sense attempts by the output to drive below ground. Both circuits track the chip's ground as a reference voltage. In each case, ground movement, caused by self-inductance between the chip and the terminal, allows larger undershoot voltages to develop before these protection circuits begin to function (**Figure 6**).

Consistent with the prior analysis, an SN74AS00 housed in an SO package provides a cleaner signal than a comparable DIP. The SO-packaged device yields a 0.3V to 0.5V improvement in undershoot protection over the DIP device when outputs switch simultaneously.

Crosstalk Improved Also

Reduced package crosstalk is another result of lower internal package impedance. In addition to lower self-inductance, the SO package has less pin-to-pin capacitance and less mutual inductance, reducing the device's signal to signal crosstalk. Crosstalk can be particularly troublesome in high-speed logic systems.

Tests on the SN74AS00 indicate up to 50% better performance for very fast edge speeds when it is packaged in an SO enclosure rather than a DIP. **Figure 7** shows the results of applying a 5V input pulse to pin 1 of the SN74AS00 NAND gate and observing the crosstalk output on pin 2 for different rising edge speeds.

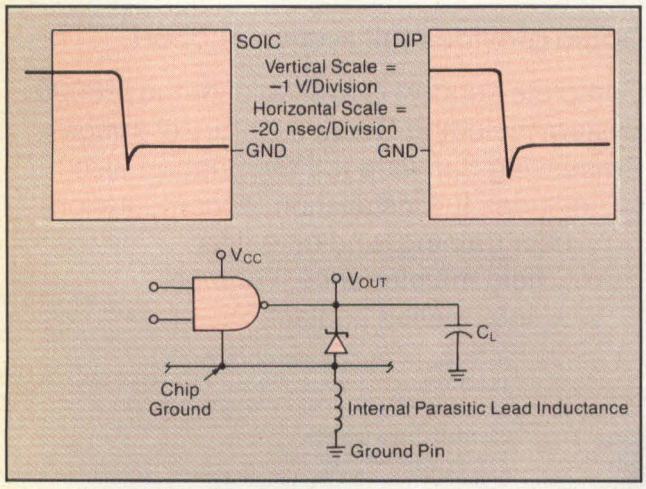

Figure 6: The SO-packaged device improves undershoot protection over that of a DIP. Shown is an undershoot comparison between the DIP version and SO version of the SN74AS00. The circuit illustrates the test condition. Switching outputs results in chip ground movement, which causes the reference voltage of the standard on-chip Advanced Schottky output clamp diode to become more negative. Due to the lower parasitic inductance of the SO package, the reference voltage moves less and thus exhibits less undershoot.

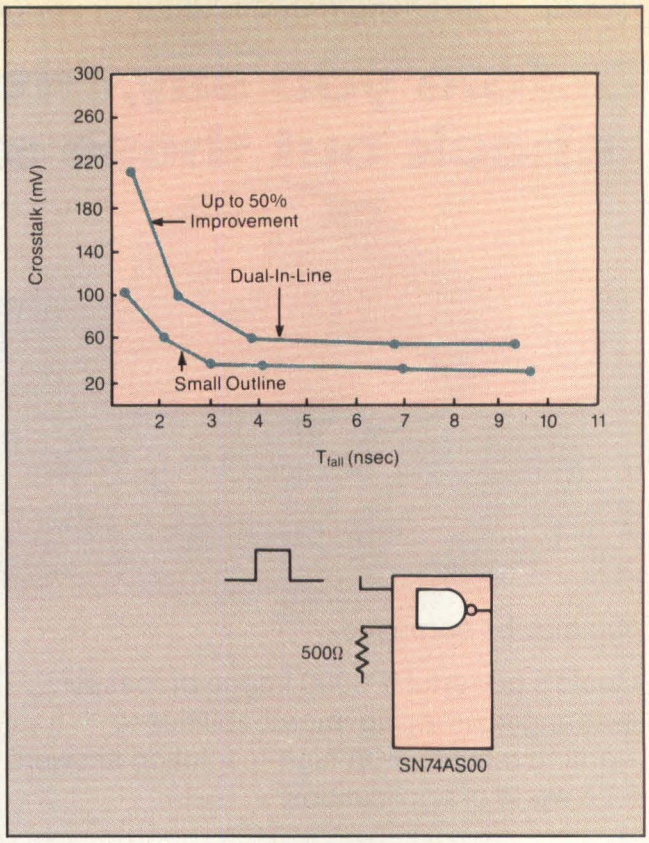

Figure 7: The crosstalk of a 14-pin DIP is much higher than the crosstalk exhibited by a 14-pin SO package because of lower high-frequency noise margins in DIPs. The circuit illustrates the test condition: a 5V pulse was applied to pin 1 of the 14-pin package, and the peak-to-peak crosstalk voltage was measured on pin 2. The results show a 50% reduction in crosstalk.

The improvement is particularly important when both ground movement is present and device outputs are switching. Crosstalk voltages can couple to a static input, causing the device to operate in an unexpected manner. An increased noise margin at high frequencies allows more reliable high-speed designs and fewer problems.

While surface mount packages offer a reduction in crosstalk for the package, designers should also consider the crosstalk component of the PC board. Because of the closer pin-to-pin spacings of surface mount packages, PC board traces may be laid out with very tight spacings. Such layouts can create unwanted crosstalk. Parallel runs, especially for runs on different layers, should be avoided. Running adjacent signal layers perpendicular to each other or using ground and V_{CC} planes to shield the runs on different layers minimizes these problems. A careful layout, coupled with the use of surface-mount Advanced Schottky devices, may allow more reliable high-speed designs and result in fewer troubleshooting problems to solve. **DD**

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Table top or rack mount enclosures are also available for the Model 40.

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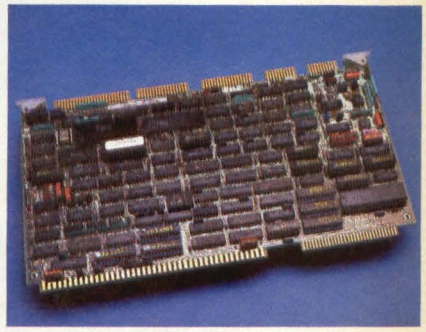

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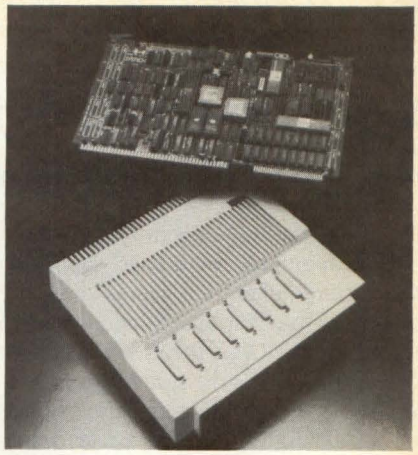


Traditionally, providing asynchronous multiplexing capability for Multibus I or VME systems has required use of a single board providing up to 16 channels that must plug directly into the CPU bus. If more terminal support was required, more boards had to be used. Designers got around this by interfacing the single board to an expandable distributive panel. However, the panels were expensive and often ended up clustered in one or two adjoining computer cabinets.

Now, Systech Corp. (San Diego, CA) has announced a more cost-effective approach to the multiplexing dilemma. Its multiplexers consist of both host adapters and remote cluster controllers that handle terminals in 8- or 16-node increments. The transport mechanism between host and multiple cluster controllers is based on the Arcnet token-passing LAN.

The host adapters—available in Multibus I, Multibus II or VMEbus formats—support up to 128 terminal ports while occupying a single slot in the host backplane. All host adapters in the series include a 10-MHz 68010 CPU, up to 512 Kbytes of zero wait-state memory and a 2.5-Mbit/sec transport interface to the cluster controllers. Host adapters can run the host operating system's TTY manager, or can emulate a block-mode multiplexer with standard TTY drivers.

An option, available for the Multibus I version of the host adapter only, is a 4-Mbit/sec serial interface. This is suitable for synchronous host-to-host communications.

Cluster controllers handle the character-by-character processing for 8- or 16-user terminals. Built around the 68008, they contain 16 Kbytes of RAM, the transport interface and four dual-channel UARTs. Standard DB-25 connectors provide the interface to user terminals. They are packaged in an impact-resistant plastic case suitable for wall-mount or desktop use.

Communication between the host adapter and up to 32 cluster controllers is provided by cabling that may extend 1000' from the host. The controllers are transformer coupled to the cable, insuring that a failing cluster controller will not bring the entire system down.

—D. Wilson

Circle 231

Hot Box Joins Supermini Line

Running at speeds up to 10 MIPS, a new machine from Data General Corp. (Westboro, MA) ups the stakes in the cost-per-MIPS competition. This tightly coupled dual-processor combo, known as the Eclipse MV/20000 Model 2, claims a cost per MIPS of $33,000. The computer is also available as a single-processor cabinet model (the MV/20000 Model 1) and as a rackmount model (the MV/20000 C), both of which report 5.5-MIPS performance.

"The linchpin in this design is the Motorola ECL gate array," says Thomas West, vice president of systems development, "Just three CPU boards comprise the processor, which translates into significant benefits in terms of system cost, reliability and maintainability." The 15 gate arrays per board furnish more than twice the density of the VAX/8600, according to Data General. ECL provides speed needed for critical data paths while low-power, low-cost TTL is used for noncritical data paths. The ECL/TTL gate arrays, together with Fairchild Advanced Schottky Technology (FAST) and advanced Schottky devices deliver mainframe-class performance in a housing measuring 61.4" × 35.1" × 40.4". No special cooling or power is required for the Eclipse MV/20000 systems.

Also, the CPU uses a group of microcode-controlled subsystems for pipelining of instruction fetch, decode and execution operations. Both the instruction processor and the ALU have caches to speed the pipeline. These caches are built using 64K static RAM with access time of 25 nsec.

MV/20000 main memory is configurable to 64 Mbytes. It supports three I/O channels and 25 I/O slots for peripherals. Main memory in the MV/20000 C rackmount model is expandable to 16 Mbytes. The rackmount unit has seven I/O slots and supports up to seven disk controllers. System MV/20000 maximum I/O bandwidth hits 35 Mbytes/sec while aggregate memory bandwidth is set at 47 Mbytes/sec.

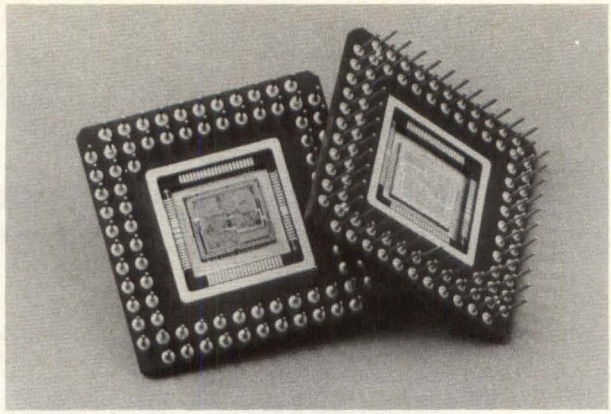
Operating systems offered include AOS/VS and an enhanced distributed version of that system known as AOS/DVS. DG/UX—a Data General system said to support both UNIX Systems V and 4.2—and MV/UX, a hosted version of UNIX are also available. An Ada development package, as well as languages such as ANSI Fortran 77 and ANSI 1974 Basic are supported.

Also announced by the company was the DS/7000 series of engineering workstations, which are based on a single-board implementation of the MV processor architecture, and a low-end 32-bit single-board multiuser system—the MV/2000 DC. MV/20000 Model 1 will be available for delivery 90 days after receipt of order. Model 2 is available for delivery in 180 days.

—Vaughan

Circle 230

Second-Generation 32-Bit Microprocessor Bows



With the first generation of 32-bit microprocessors barely upon us, the second generation seems ready to emerge. From National Semiconductor (Santa Clara, CA), the NS32332 chip boasts three times the system speed of a first-generation computing cluster based on the NS32032 CPU. Clock rate for the 32332 is 15 MHz. The chip features a full 32-bit address register that allows the CPU to address up to 4 Gbytes of memory.

Dynamic bus sizing means the 32332 can be used with 8-, 16- or 32-bit data buses while a burst mode memory addressing capability lets the device process multiple addresses from a single instruction. The 32332 can switch from one buswidth to another on a cycle by cycle basis. Burst mode is available only in instruction fetch cycles and operand read cycles. Other enhancements include bus error and retry support and an advanced slave processor communication protocol.

This part is object-code compatible with its predecessors in the 32000 family. Because there is no architectural difference between the 32332 and the 32032, an AT&T validated UNIX System V/Series 32000 system runs on the 32332. Upgraded versions of 32000 family memory management units and floating point coprocessor units are compatible with the new microprocessor. National's EXEC real-time operating system also runs without revision. As with other processors in the 32000 family, the new chip is said to support high-level language constructs. Performance in the 2.5- to 3-MIPS range is reported.

The 32332 retains the 32032's symmetrical approach. Nine general addressing modes are available for the commonly used operators (move, arithmetic, logical and comparison) and no restrictions are placed on which data types (8, 16, or 32 bit) are allowed. Any of the eight, 32-bit general purpose registers can be used to hold either address or data, regardless of the instructions. Eight dedicated registers handle such functions as program counting, frame pointing, interrupt stack pointing and holding of status codes.

Manufactured using XMOS, a proprietary 2.8-micron NMOS process, the 32332 is packaged in an 84-lead pin-grid array and operates from a single 5V power supply. On-chip are 90,000 transistors. The part can be developed using existent 32000 series design tools. Initial cost of the 32332 is set at $195.

—Vaughan

Circle 232

Two-Chip Set Implements 300/1200-Bit/Sec Modem

Sierra Semiconductor (San Jose, CA) has announced a CMOS 300/1200-bit/sec modem chip and companion controller that together implement a complete Bell 212A or CCITT V.22 smart modem. The chip set also incorporates the Hayes (Norcross, GA) command set, while providing the necessary hardware and software to connect to either a parallel system bus or an RS-232 serial port.

The company notes that competitive single-chip modems do not provide the high level of integration found on the SC11004. Some other modem chips require an external DTMF generator for tone dialing, a separate 300-bit/sec modem chip for the low-speed fallback mode called for in the Bell 212A specification or an external band-split filter. In addition to these functions, the SC11004 modem chip also includes a two-to-four-wire hybrid circuit to simplify interfacing to a Data Access Arrangement (DAA) required by the FCC for connection to the phone lines. Analog loopback and remote digital loopback functions are included for self-testing. Furthermore, the chip also has an energy detector to handle carrier detection and call progress monitoring on the phone line.

The SC11007 controller provides the necessary intelligence to determine the mode of operation, initiate the call to the remote modem using either pulse or tone dialing, set up the handshaking sequence, monitor the call progress tones on the line, and switch into the data mode. The controller includes an 8-bit microprocessor, 8 Kbytes of ROM (2K are user-defined), and 128 bytes of RAM. Simplifying the interface to a parallel system bus, the controller also includes the major functions of an 8250B-type UART.

Intended for standalone modems, the SC11008 version of the controller handles handshaking protocols associated with RS-232 serial communications. The parallel version differs in that the UART is turned around so that serial data from the RS-232 port is converted to parallel data for internal processing. Pins are provided for connection to the familiar switches and indicator lamps found on most standalone modems. However, these are not needed for actual operation since all of the switch settings can be done in software.

Samples of the SC11004/SC11007/SC11008 will be available early in 1986. Prices are quoted at $50 for the SC11004 and $20 for the SC11007/SC11008 in 100-piece quantities.

—Aseo

Circle 300

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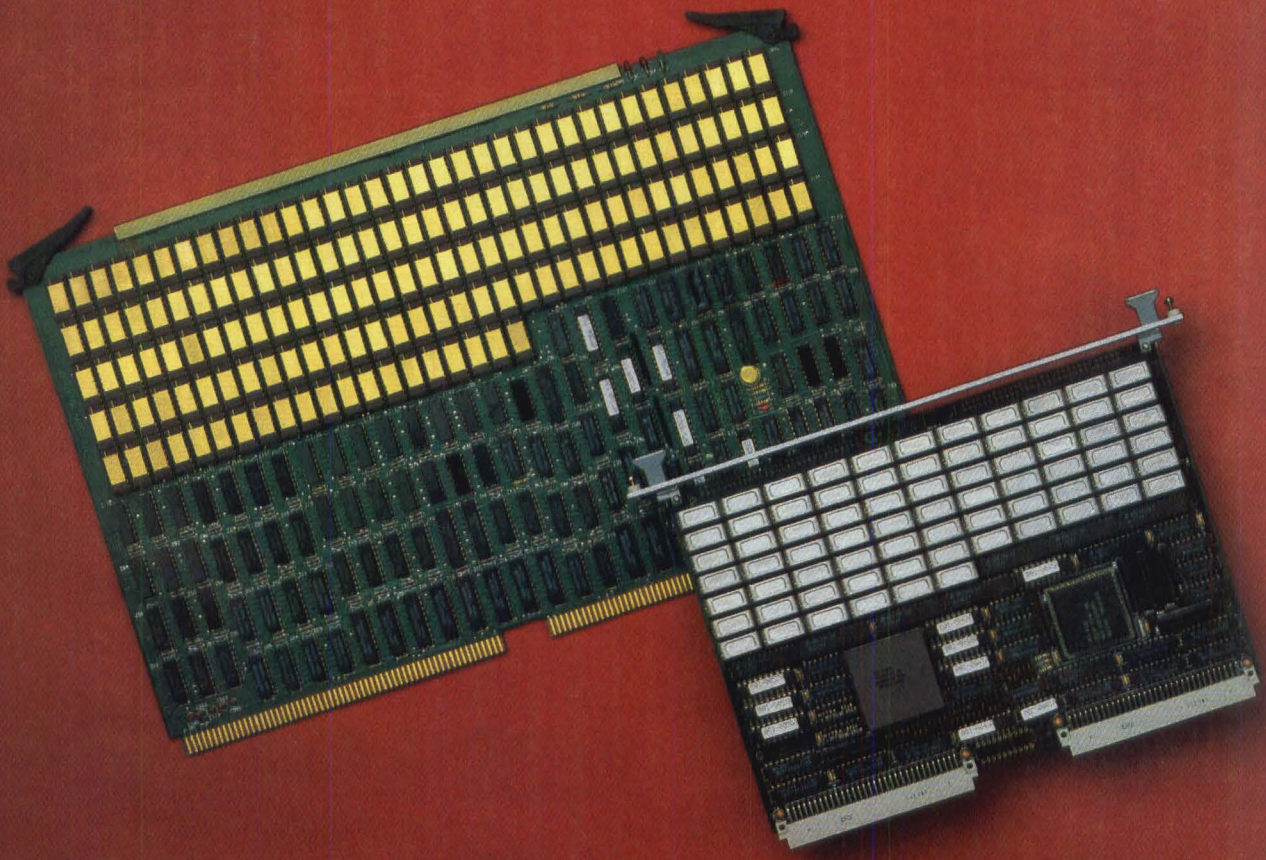
INNOVATORS IN IMAGE PROCESSING©

Circle 72

Clearpoint Defines State-of-the-Art for VME and VERSAbus Memory



Error Detection and Correction with the Price, Performance and Density of Parity Memory

Clearpoint has established a reputation in the DEC marketplace for unparalleled performance, quality and density in memory design. Now available for the VME and VERSAbus, Clearpoint memories set the standard for state-of-the-art capabilities.

Error Detection and Correction
Clearpoint's proprietary technology allows true single bit error correction and double bit error detection. The VMERAM achieves the same high density as parity memory: 2 MB on a dual card and up to 4 MB with a daughter card. The 64 bit cache reduces average access time to as low as 180 ns on reads and 100 ns on writes.

Maximum Versatility for the VME Bus
The VMERAM uses 8, 16 or 32 bit data transfers and 16, 24 or 32 bit addressing. Options include addressing on 64K boundaries, low power refresh, stand-by power backup, and a programmable Control and Status Register.

Unparalleled Performance on the VERSAbus
The V-RAM 68 is still the price/performance leader on the VERSAbus — 4 MB of EDC memory with a 220 ns access time.

5 Year Warranty.
Clearpoint memories are warranted for 5 years, with a 24 hour repair/replacement policy.

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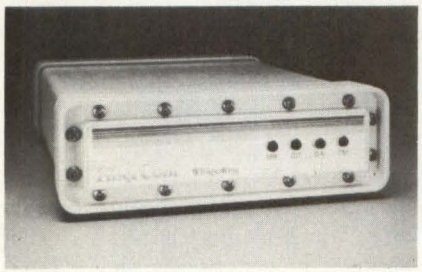
Circle 38

COMPUTER SYSTEMS

Voice/Data Unit Sports EL Panel

An 18-lbs. portable system with an electroluminescent screen integrates voice and data communications. The basic workstation contains a 68000-based microcomputer with integrated word processing, spreadsheet, database, graphics and communications software. It also has an 80c88 processor, 7220 graphics processor, modem, 3½" drive and Ethernet interface. The system provides a multitasking windowing environment that accepts MS-DOS as a guest operating system. A telephone is included that provides two-line capability, tone or pulse dialing, automatic directory dialing and auto-redial. Electronics reside on two easily accessed printed circuit boards. Digital voice storage is via continuously variable slope delta modulation, with recording rate listed at 16 Kbits/sec or 32 Kbits/sec. **Insystec,** Winter Park, FL **Circle 126**

Fiber-Optic Net Extends RS-422 LAN

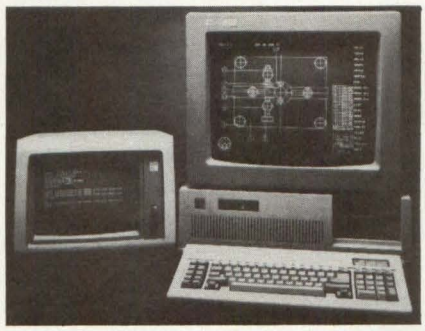


WhisperRing represents a fiber-optic data network capable of extending a high-speed RS-422 twisted-pair LAN as far as 32 km. It employs an active ring topology with automatic optical bypass of a node if a failure occurs. The active nodes convert lightwaves to electricity, then back to lightwaves. The WhisperRing provides half-duplex balanced clock and data transmission up to 2 Mbits/sec. **Fiber-Com**, Roanoke, VA **Circle 127**

Network Management Series Gains Member

The 5100 network management system brings comprehensive diagnostics and control, full-color graphics and management reporting to small and medium-sized network systems. Up to four color workstations are supported by the 5100's central site controller, which is a 32-bit computer. The 5100, which joins the vendor's 5000 product line, manages 30- to 120-line networks while supporting up to 1,500 devices. A relational database is featured, as are a 26-Mbyte hard disk and 640-Kbyte floppy disk. The system runs UNIX and supports both CAE 4000 diagnostic modem and DCX products. **Case Communications,** Silver Spring, MD **Circle 134**

System For CAD Offers High Resolution

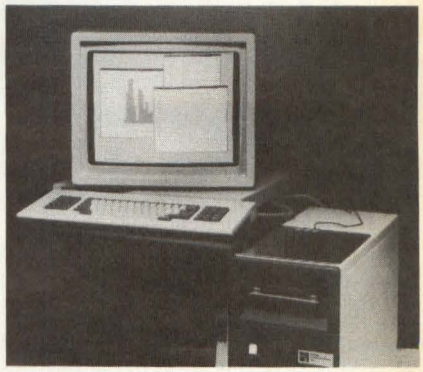


Ergonomically designed, the Micro 1024 features a 19" display with an image store area of 1024 × 2048. Screen resolution equals 1024 × 780 pixels. Non-interlaced refresh rate is 60 Hz. AT compatible, the product is said to use the standard IBM operating system and includes a graphics processor. **Cambridge Computer Graphics**, Oakland, CA **Circle 131**

System Boasts 36-MWhetstone/Sec

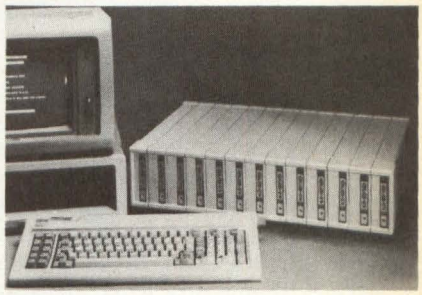
High-performance computers based on an architecture that maximizes parallel execution include the Culler 7, which offers performance ranging from 7 to 36 million Whetstone instructions/sec and from 2 to 16 million LINPACK double-precision floating-point operations/sec. Each Culler 7 sports a user processor that is a proprietary 64-bit unit employing a hierarchical memory subsystem. It runs optimizing Fortran and C compilers. A 32-bit kernel processor with 2-Mbyte private memory runs the CSD operating system and oversees concurrency between the user and kernel processor. Entry level product is a file server for Sun network workstations priced at less than $250,000. **Culler Scientific Systems**, Santa Barbara, CA **Circle 132**

LAN Manager Tells Trends In Graphics



The NCS/1 network control server allows centralized control and monitoring of Ethernet resources. It allows real-time monitoring of critical net parameters and analysis of audit-trail information using graphic displays from which trends can be detected. Based on the Sun 2/120, the network management system runs as an application on UNIX. It has a 71-Mbyte Winchester and is designed for networks of over 100 users. Price is $45,000 plus $5,000 annual software license. **Bridge Communications**, Mountain View, CA **Circle 129**

Modules Link Micros To Analog And Digital

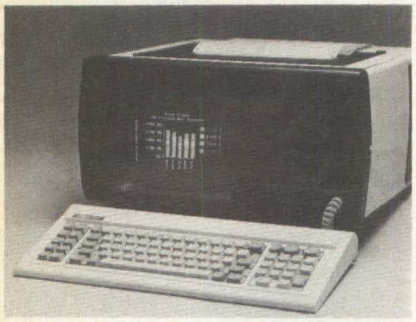


An intelligent microprocessor-based system of I/O modules, the PC-I/O, interfaces microcomputers to an array of analog and digital events. Interfacing via RS-232, RS-422 or IEEE-488 link, the PC-I/O's 8088 relieves the host of many program requirements. The PC-I/O can configure with several module combinations. Each module contains its own personality in ROM. System modules include general purpose discrete/analog I/O combinations, as well as relay output and current output, thermocouple and strain gauge modules. **Analogic,** Peabody, MA **Circle 128**

Parallel Systems In Card Cages

Series 600 and 1200 Flex/32 systems are 21″ x 19″ rackmountable card-cage versions of the Flex/32 Multicomputer. The series 600 model holds as many as four 32-bit superminis, each with its own 16- or 32-bit VMEbus I/O channel and up to 56.5 Mbytes of memory. In the Flex/32 architecture, multiprocessors can execute parts of large programs simultaneously in parallel. High-level ConCurrent C, ConCurrent Fortran and Ada are supported. **Flexible Computer**, Dallas, TX **Circle 130**

Transportables Unbundled



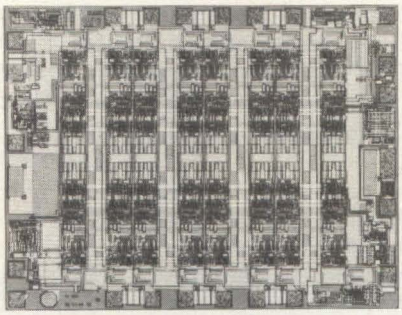
Transportable computers, offered as unbundled systems, include an AT-compatible model. The OTI Model 3 houses an 80286 system board with a maximum system RAM of 1 Mbyte, while a built-in 20-Mbyte hard disk drive and a 1.2-Mbyte floppy disk drive are also available. As an option, the machine includes a built-in 160-char/sec dot-matrix printer. The PC/AT compatible averages $3495. **OEMTEK**, San Jose, CA **Circle 133**

COMPONENTS

A 32-Bit Processor Joins iAPX86 Family

The 80386 32-bit microprocessor touts sustained speeds of 3 MIPS to 4 MIPS. Virtual memory capacity exceeds 64 trillion bytes. Chip architecture supports segmentation and paging plus two complementary memory-management techniques. The part is fully compatible with software written for chips that include the 8086, 8088 and 80286. The 80386 is said to allow simultaneous execution of MS-DOS and UNIX. Data paths support 32-bit addresses and data types, as well as 8- and 16-bit data. In sample volumes, unit price is $299. Production quantities are pegged for the second half of 1986. **Intel**, Santa Clara, CA **Circle 168**

Video Shift At 200 MHz



Dubbed the Am8177, a parallel-to-serial video shift register sports a clock rate of 200 MHz. This video data serializer for bit-mapped graphics systems can accommodate video words in 16-bit increments. Parallel data inputs of the Am8177 are TTL logic types, while the clock and serializer controls are ECL. A set of latches is provided between the parallel data input pins and the shift register, allowing the next word of data from the RAMs to be loaded without affecting the contents of the shift register. The 100-piece price is $20 in 24-pin plastic DIPs. **AMD**, Sunnyvale, CA **Circle 171**

Gate Array Comes In Gallium Arsenide

The 2,000-gate HGG-2020 GaAs array supports clock speeds up to 1 GHz, with typical internal gate delays of 230 psec. Gate feature size is 1-micron. With this part, 56 I/O cells can be configured as I/O for either 5V TTL/CMOS or ECL options. The HGG-2020 is offered in an 88-pin chip carrier package. **Honeywell**, Richardson, TX **Circle 175**

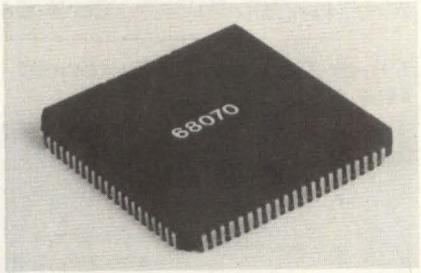
Video DACs Boast 50-MHz Conversion

The Bt106, for medium-resolution graphics systems, drives a doubly-terminated 75-ohm load, allowing easy interface to color and monochrome monitors. It supports screen resolutions exceeding 768 × 576 pixels at a 60-Hz frame rate. The monolithic device uses silicon gate CMOS switches for guaranteed less than ±1 LSB differential and integral linearity errors. Bt106s dissipate only 400 mW of power worst case at full rated clock speed. RS-343-A-compatible output provides video control signals (Blank, Sync and Ref White) to simplify system design. In quantities of 1,000, standard parts are $16 each. **Brooktree**, San Diego, CA **Circle 174**

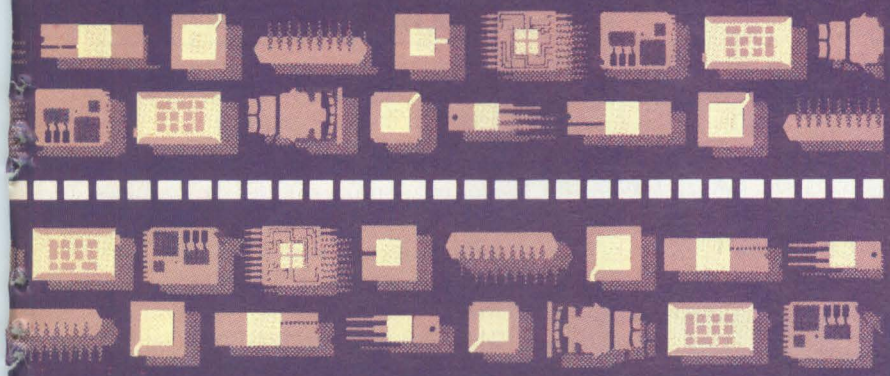
Devices Drive EL Displays

A family of compact Smartpower ICs replace many discrete components for driving EL display panels. The devices are said to combine great drive capability with low power consumption. Built with combined DMOS and CMOS Smartpower technology, the circuits are pin compatible with existing 32-channel driver circuits. Dubbed the Si9551 and Si9552, two parts are 32-channel row drivers that have 32-bit shift registers. They are rated at 225V and 80 mA over the full military temperature range. The 32-channel column drivers—Si9553, Si9554, Si95555 and Si9556—have a 10-MHz 32-bit shift register, 32-bit latch and 32 totem-pole outputs rated at 60V and 90V. Sink-and-source capability ranges up to 15 mA over the entire military temperature range. **Siliconix**, Santa Clara, CA **Circle 173**

Processor Includes Memory Management



The SCC68070 microprocessor in CMOS integrates a CPU with memory management, direct memory access and other peripheral functions. The single chip is packed in an 84-pin plastic leaded chip carrier and takes advantage of surface mounted device assembly techniques. Functionally, the 68070's CPU is identical to the 68000. Like the 68000, the 68070 directly addresses 16 Mbytes of memory and executes instructions at a clock speed of 10 MHz. The programming model is similar to that of the 68000. **Signetics**, Sunnyvale, CA **Circle 172**



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CMOS 256K SRAM Offers Byte-Wide Access

HM62256 is an SRAM chip organized as a 32K × 8 bit, byte wide device. Implemented in advanced 1.3-micron CMOS technology, the part boasts an access time as low as 85 nsec. The HM62256 comes in a 28-pin package. Power dissipation measures 40 mW. With mass production quantities due in January, the 1,000-piece price for the 120-nsec version is $83 each. The low-power version will sell for $91.70 in the same quantity. **Hitachi**, San Jose, CA **Circle 176**

CMOS Circuits Surpass Schottky

A family of advanced CMOS logic circuits exceed performance of standard and advanced low-power Schottky as well as existing HCMOS devices. Called FACT (for Fairchild Advanced CMOS Technology), power consumption is as low as 0.1 mW per gate at a 1-MHz clock frequency, with propagation delays of just 5 nsec. Family devices include 54 and 74 series logic circuits. The Fairchild process produces gate lengths of 1.25 micrometers. Operating temperature range for 54AC devices is -55° to 125°C. **Fairchild**, Mountain View, CA **Circle 169**

DMA Controller Offers 8-MHz Clock

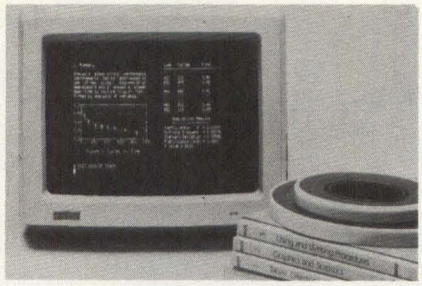
A CMOS device for control of direct memory access sports a maximum clock frequency of 8 MHz, with a typical operating current of 2 mA/MHz. Functionally equivalent to the NMOS 8237A, the chip improves system performance by allowing external I/O devices to directly transfer data to and from system memory at clock rates up to 8 MHz. During high-end DMA operaton, the 8-MHz frequency pushes data transfer at a 4-Mbyte/sec rate. The part is available in 40-pin ceramic or plastic DIPs and 44-pad ceramic LCCs. The plastic-DIP version costs $33.70 each, in quantities of 100. **Harris Semiconductor**, Melbourne, FL **Circle 177**

SOFTWARE

Cross Assembler Runs Under VSM Or UNIX

A versatile cross assembler runs under VSM or UNIX 4.2. It will work with 4-, 8-, 16-, or 32-bit microprocessors. It supports the 8086, 68020, 32032 and other parts, using pseudo-instructions common to all processors. Powerful preprocessor macro functions are touted. The assembler is executable in the 32-bit native mode of VAX-11 systems, as well as the MicroVAX I and II. Support for C, Fortran and Pascal is planned. **Sumitronics**, Sunnyvale, CA **Circle 194**

Enhanced RS/1



Release 2 is an enhanced version of RS/1 software. Table and graph editing, a command line editor, interfacing to other editors and an enhanced set of analytical tools are supported. Spline fits, probability plots, histograms, principal components analysis, general linear models, quadratic response curves and contour plots are also possible. **BBN Software Products**, Cambridge, MA **Circle 191**

TCP/IP Software Support

Support for the DARPA Internet Protocols (TCP/IP) enhances operation of Fusion 3.0 LAN software. Running on the PC and compatibles, it provides virtual terminal and file transfer utilities using TCP/IP between MS-DOS machines and other operating systems, including VAX, VMS and UNIX. The package also provides network test and management. **Network Research**, Oxnard, CA **Circle 192**

Virtual Windows

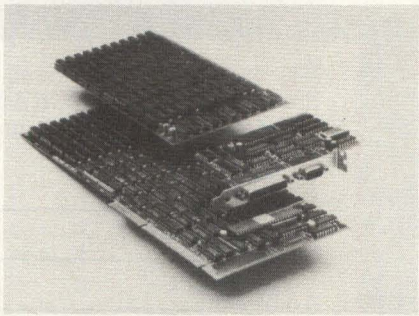
A software system, Virtual Windows, can display solid overlays and support true color images in up to eight active windows. It runs on machines from DEC, Data General, HP and others. Virtual Windows technology is based on LEX 90 processors. With the software, users can divide a bitmap area into a series of 80 × 4 × 4-pixel cells. Functions include split-window text scrolling, dynamic window sizing, panning and scrolling of color and double-buffering of bitmap areas. Users can read and store up to 24 planes in a window. Display is in less than 0.03 sec. As a Lex 90 module, price is $3,000. **Lexidata**, Billerica, MA **Circle 189**

BOARDS

VMEbus Board Family Performs Imaging

MaxVideo family members provide real-time image processing for the VMEbus. Modular architecture allows for easy system configuration and expansion. MaxVideo boards communicate via the MAXbus. One family member, the MAX-SP general purpose signal processor module, performs operations ranging from conventional spatial and temporal filters to exotic "shift and difference" algorithms. The MAX-SP appears as a 16-Kbyte block of VME memory space, with the base address jumper selectable. Selection of inputs (from a variety of MAXbus signals and a control register) to a fast 4K × 16 bit SRAM array is transparently switchable on a pixel-by-pixel basis. Also included in the series are an interpolator, an A/D and D/A module, a framestore and pipelined linear pixel processor. **Datacube**, Peabody, MA **Circle 148**

Expansion Board Offers ECC For AT



An expansion board for the PC AT, the ECCEL, incorporates error correction code. The high-capacity RAM disk utility provides up to 12 Mbytes of storage. The main card has a memory capacity of 1 Mbyte, with 2 Mbytes on the daughtercard. Up to 4 boards per system can be added. A 1-Mbyte capacity board costs $595; each daughtercard costs $145. **Orchid Technology**, Fremont, CA **Circle 150**

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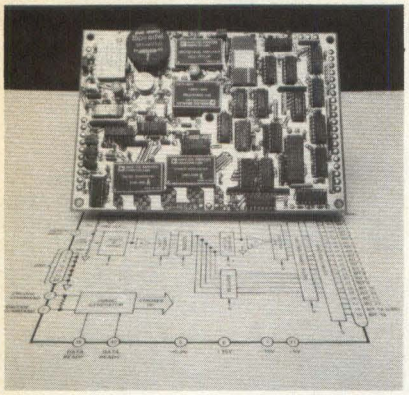
Circle 25

A/D Converter Uses Pipelining



The CAV-1220 utilizes a unique pipelining conversion technique along with fast track-and-hold and subtration amplifiers to achieve 20-MHz throughput. This A/D converter is capable of 12-bit resolution. Total error at dc, including nonlinearity, is 0.0125% of full scale. Typical small signal and large signal bandwidth are 40 MHz and 35 MHz at 3 dB. Applications include digital communications, medical instrumentation and real-time spectrum analysis. Pricing starts at $4,078 in singles. **Analog Devices**, Canton, MA **Circle 151**

AT Voice Recognizer

Allowing users to invoke up to 500 spoken commands, a short-card voice recognition package aims at PC/XT/AT applications. It is a discrete word, speaker-dependent package that combines a menu-driven, keystroke definition program. Called the VocaLink SRB-LC, the package occupies less than 64 Kbytes of PC memory. Included in the package is a microphone. Single-unit price is less than $400. **Interstate Voice Products**, Orange, CA **Circle 152**

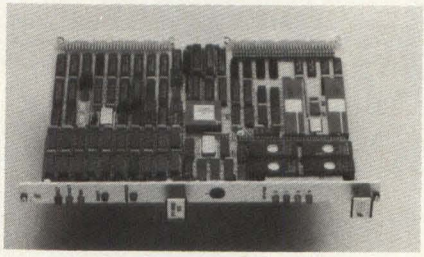
Disk Controller Handles VAX-11/780 Applications

A disk controller—known as the SC7002—handles the VAX-11/750 and 780. Tying directly to the CMI bus, the SC7002 interfaces through the Emulex V-Master and connects to the Synchronous Backplane Interconnect (SBI). The device allows mixing of standard SMD drives with 1.2-Mbyte, 1.8-Mbyte or 2.4-Mbyte transfer rates. A 4-Kbyte RAM buffer in the controller provides 12 sectors of buffering. Operation is transparent to the VMS, UNIX or other VAX operating systems. Price is $8,950. **Emulex**, Costa Mesa, CA **Circle 153**

Array Processor For 6300

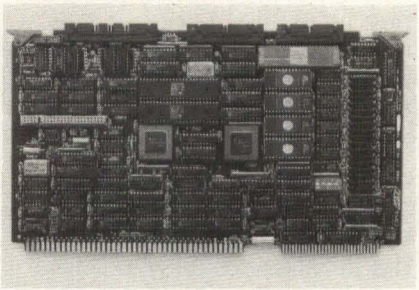
The APB-3024ATT is a single-board array processor plugging directly into any available slot in the AT&T 6300. The unit performs high-speed computations on floating point or integer data. It processes a 1024-point complex integer FFT in 18.2 msec and a 1024-point complex floating point FFT in 73.1 msec. Memory mapping allows users to locate program memory wherever desired within the first Mbyte. Processor runs at 125-nsec cycle time. It performs at an 8-MIPS rate. Floating point speed rates at 1 MFLOP. Price is $3550. **Marinco**, San Diego, CA **Circle 138**

Single-Board Has 2-Mbyte No-Wait-State



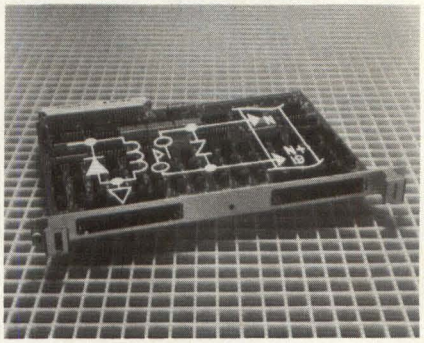
A single-board VME system sports 2-Mbyte zero-wait-state memory and runs a 68010 processor. A 68881 floating point processor and eight serial I/O ports are also touted. On-board memory features full parity checking. Known as the PT-VME102, the board supports up to 256 Kbytes of ROM. Real-time clock with on-board battery back-up is reported. Pricing for the base PT-VME102 single-board computer starts at $2195. **Performance Technologies**, E Rochester, NY **Circle 154**

Multibus Unit Runs 68010 Chip



A communications board has two serial channels that can transmit and receive data at up to 3 Mbytes/sec. Using a 68000 or a 68010 processor, the COM II Multibus board runs without wait states at 10 MHz. The channels can configure to run in asynchronous, byte synchronous or bit synchronous modes. The COM II supports X.25, SNA, SDLC/HDLC and Bi-sync protocols. Interface via RS-232, RS-422 or TTL drivers is supported. In quantities of 100, price is $1,295 each. **SBE**, Concord, CA **Circle 149**

VME Output Control



Up to 32 digital output channels—each handling up to 10W—are controlled by a microcomputer using the MPV902. This VMEbus-compatible relay output board lets micros control voltages and currents exceeding normal TTL levels. MPV902 relay contacts are controlled by the CPU and work as high-voltage and high-current switches. The board appears as a memory location and data written on the bus controls the status of each output. In quantities up to 50, the device costs $780. **Burr-Brown**, Tucson, AZ **Circle 146**

Memory Array Aims For MicroVAX II

Memory array boards with capacities of 2 Mbytes and 4 Mbytes are tailored for the MicroVAX II. Known as the DR-222, the quad-sized board uses 256K × 1 dynamic RAMs. The board interfaces directly with the MicroVAX II and communicates with the CPU via a private memory bus. Price for the 2-Mbyte model is $1,890 while the 4-Mbyte board lists for $2,700. OEM discounts are available. **Dataram**, Cranbury, NJ **Circle 147**

DEVELOPMENT TOOLS

Workstation Built On MicroVAX II

First in a series of MicroVAX II-based workstations, the Logician VX will run Daisy's complete set of software from design entry through verification. The MicroVAX II includes the 787032 floating-point processor, 2 Mbytes of memory, a 70-Mbyte hard disk and a choice of either the VMS or Ultrix oper-

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- *Image Analysis*
- *Image Enhancement*
- *Spatial Filtering*
- *Area Measurement*
- *Digitization, Storage and Retrieval*
- *Image Editing*
- *Half Tone Printing*
- *Report Generation and Annotation*

The heart of the solution is the Image-Pro Software. This software includes:

1. *A stand alone interactive, image processing program.*
2. *An icon-based, image editor.*
3. *A library of powerful image processing subroutines.*
4. *A slide show and batch printing program.*

With Image-Pro, information from documents, photographs, x-rays, satellites, etc., can be electronically captured, processed, analyzed, stored and retrieved for future reference.

Image-Pro Workstation

The Image-Pro Workstation includes: an IBM AT or compatible; precision video camera, image capture board, video display device, high resolution monitors, and a color or black and white printer (including laser printers).

And the Image-Pro software is transportable between Workstations configured with different imaging and graphics components.

Image-Pro Subroutines

Image-Pro subroutines provide software developers and OEMs with all the tools needed to quickly implement customized imaging solutions.

HALO Software Development Environment

With HALO, a complete programming environment is available as a complementary package to Image-Pro. HALO is a powerful toolbox of over 170 graphics primitives that is an established standard for graphics in the IBM PC and compatibles marketplace.

Some of HALO's extensive functions include: point, lines, arc, circle, ellipse, image compression, rubberbanding, polygon fill, animation, windowing, color management, curve fitting, world coordinates, etc.

HALO supports the most popular programming languages, graphics controller cards, and input and output devices and includes LEARNHALO, an interactive, computer-aided tutorial.

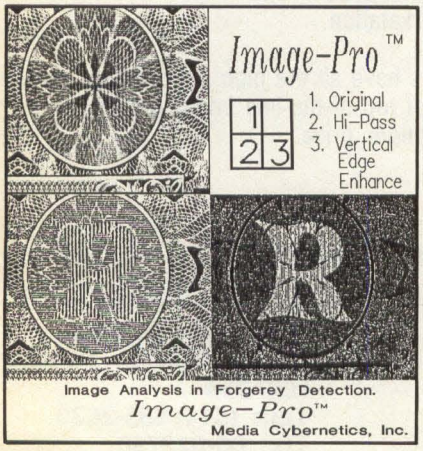

Image Analysis in Forgerey Detection.
Image-Pro™
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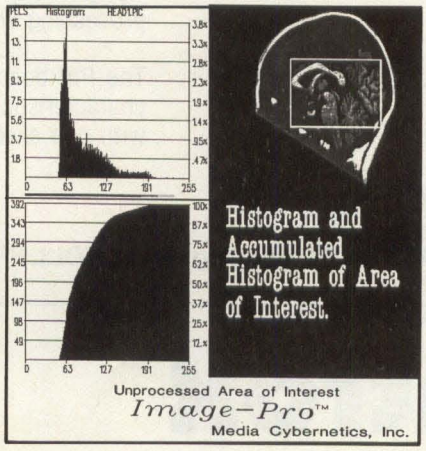

Unprocessed Area of Interest
Image-Pro™
Media Cybernetics, Inc.

Ordering Information

The price for the Image-Pro Software is $1,000.00. HALO costs $250.00 for a single language; additional language bindings cost $150.00.

For price information on the Image-Pro Workstation see GSA Schedule GS00K85AGS6100.

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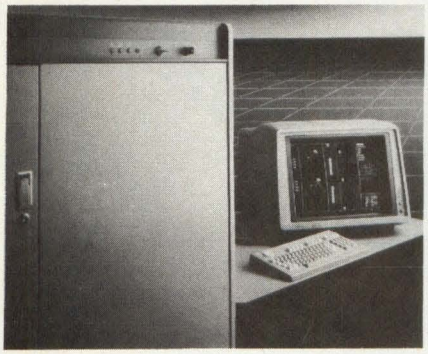
ating systems. A VX node is offered that allows sharing of MicroVAX II resources that can be tailored to individual needs. **Daisy Systems**, Palo Alto, CA **Circle 145**

CAE For The VAX



CAE schematic design software runs under the VMS system due to the CT10000 package. The software also supports high-resolution Tek 4100 graphics. CT10000 incorporates an advanced graphics editor, the SCALD hardware compiler and netlist postprocessor, as well as PC-board layout tools and a logic simulator. The package allows standard DECNet/Ethernet configurations. CT10000 for the VAX starts at $12,500. **Case Technology**, Menlo Park, CA **Circle 140**

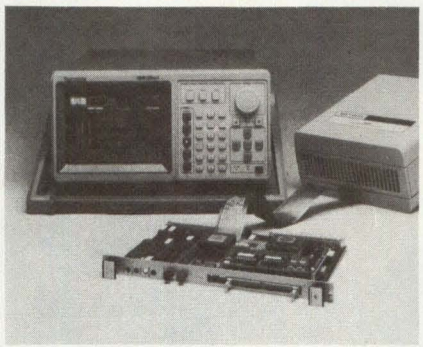
PC-Hosted Erasable Programmable Logic

A development system for programming and testing erasable programmable logic devices (EPLDs) includes a full set of software, programming hardware, an interface for the IBM PC and sample EPLDs. The iPLDS, or Intel Progammable Logic Development System, allows quick development, programming and testing of a logic design. Programs handle design entry, logic optimization, compiling and automatic design fitting. Design software also programs, reads and verifies the EPLD using the system's programming hardware. EPLD designers can use Boolean equation entry, schematic capture packages, state machine entry and interactive netlist entry. Running on the PC/AT, PC/XT or PC-DOS-compatible systems, the EPLD programmer can purchase iPLDS for $1,450. **Intel**, Santa Clara, CA **Circle 156**

Simulation Accelerator At 250K Events/Sec

The Mach 100 Simulation Engine is a hardware accelerator that simulates ICs and PC boards 500 times faster than software running on a VAX 11/780. It operates at 250,000 events/sec and has capacity for 32,000 modeling elements. Designed to perform high-speed logic and fault simulation of electronic designs at the gate and switch levels, the Mach 100 Simulation Engine can accept behavioral-level output from a host workstation. Logic and fault simulations on the high-end Mach 1000 machine run at 500,000 events/sec. Sold as a free-standing tower that can fit under a desk, the Mach 100 has a 20″ × 10″ footprint. It serves as either a dedicated hardware accelerator for a single workstation or PC, or as a shared peripheral accessible over a LAN through a host workstation. Interface is standard IEEE-488. Price is $25,000 for logic simulation and $30,000 for logic and fault simulation. **Silicon Solutions**, Menlo Park, CA **Circle 157**

Analyzers Handle 68020/80286 Devices



The 1200 series of modular logic anlayzers now handles 80286 and 68020 microprocessors. For the 80286, the PM204 personality module provides instruction disassembly of the 80286 and 80287 at clock speeds up to 10 MHz with a flexible single-plug for easy connection. The PM205 module offers support for the 68020 as well as single-point probing. The probe is configured to plug directly into the processor socket of the DUT. The PM205 provides disassembly of bus cycle mnemonics at 16.7 MHz. **Tektronix**, Beaverton, OR **Circle 143**

Digital Storage Scope

Model 4050 digital storage oscilloscopes offer dual 100-MHz A/D converters. Vertical resolution of 8-bits is reported, as is 1K of memory per channel. Five-trace non-volatile RAM storage further enhances this machine. The model 4050 also functions as a dual-channel analog oscilloscope while retaining the ruggedness and convenience of a general pur-

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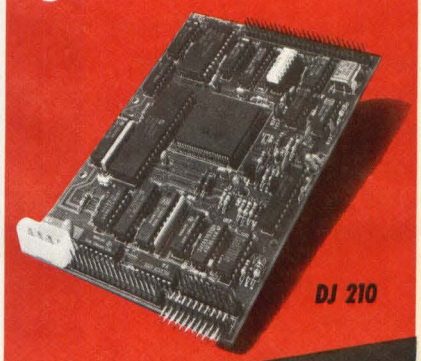

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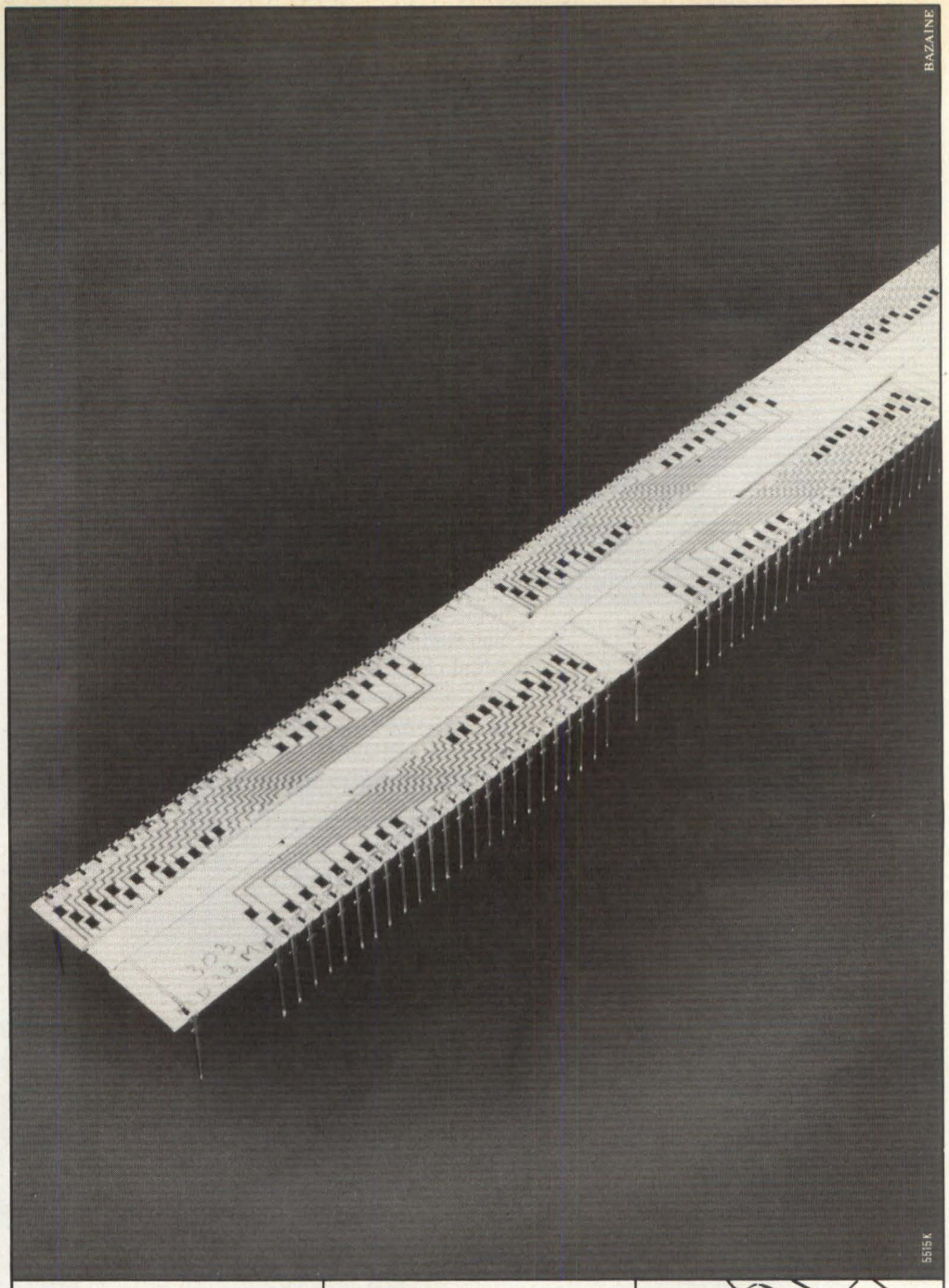

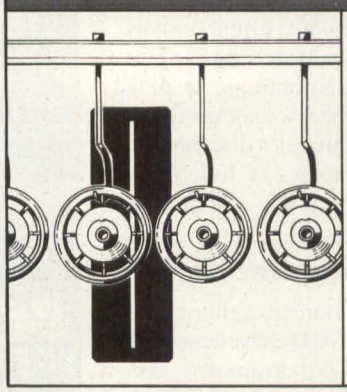

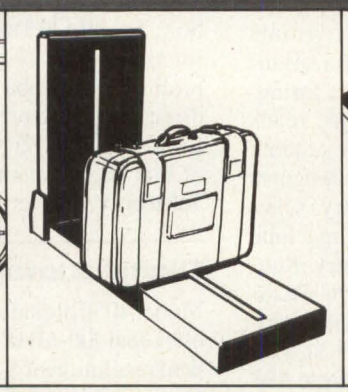

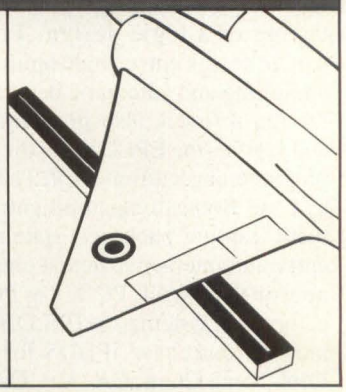

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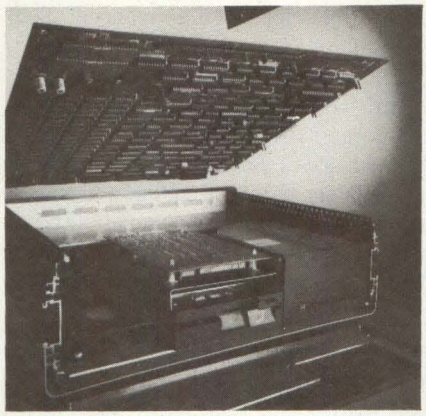
NEW PRODUCTS

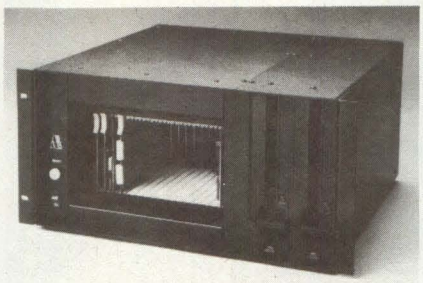
pose real-time scope with bandwidth capability to 35 MHz. The complete 4050 costs $7,950, or $7,290 without optional keypad. **Gould Inc., Recording Systems Div.**, Cleveland, OH
Circle 158

GS-32 Developer



A complete 32-bit multiuser developing system, the GS-3200, is billed as a development tool for the GS-32 from Goodspeed. It also handles other 32032 and 32016 projects. The software environment is the GENIX system, which supports demand-paged virtual memory management, giving each user a full 16-Mbyte virtual address space. Also featured is 2-Mbyte no-wait-state memory. The I/O coprocessor is a Z0B. **Goodspeed Systems**, E Haddam, CT
Circle 144

Development/Target System For Automation



For applications including data acquisition, machine automation and process control, the Racklink development and target system is supported by over 1,000 STD function modules. Based on the 6809, the system comes in 5¼" and 8" versions. The front of the chassis has a removable cover that encloses a 16-slot fully STD bus-compatible motherboard and card cage. A single 100W switching power supply provides dc voltage (5V at 15A, 12V at 1.5A, -12V at 1A and 24V at 4A) for system and disk drive operations. **Matrix**, Raleigh, NC **Circle 141**

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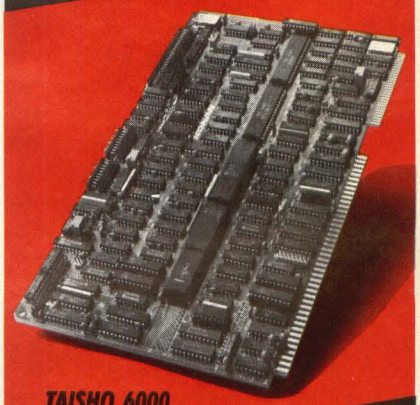

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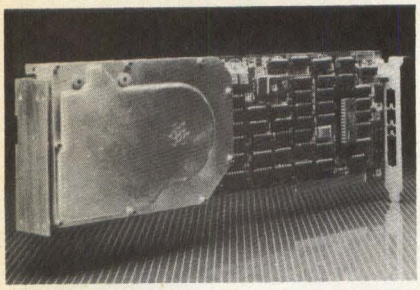
PERIPHERALS

20-Mbyte Winchester Resides On A Board



With 20-Mbyte capacity and an average access time of 45 msec, a 3½" Winchester sits on a single board. Priced at under $1,000 in OEM quantities, the device is known as the HC 2045. It is PC compatible, fitting directly into a standard PC slot and drawing less than 9W from the computer's power supply. Head positioning is controlled by a closed-loop servo system and sputtered-plated media with carbon overcoating used for maximum performance as well as reliability. **AK Associates**, Manhattan Beach, CA **Circle 162**

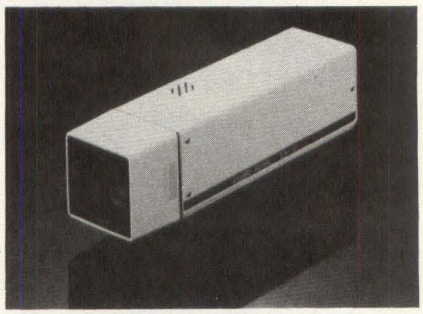
Mass Storage Subsystem Line Expands

A standalone mass storage subsystem, featuring either a 10-, 20- or 33-Mbyte fixed drive and a 10-Mbyte removable cartridge disk drive for IBM PCs and compatibles has been announced. The subsystems are available both in a single configuration with a fixed or removable disk drive or in a dual configuration with any combination of two fixed or removable disk drives. Each subsystem includes a standalone hard disk cabinet and power supply, an IBM PC/XT-compatible controller and interconnect cable. **Sumo Systems**, San Jose, CA **Circle 161**

Medium-Res Terminal Offers 38.4-Kbaud Link

Providing one page of dot addressable screen memory, with three added pages optionally available, the 8820 color graphics terminal features an 80-character, 48-line screen format. Resolution lists at 480 × 384 pixels. The 19" display offers eight foreground and eight background colors. Rapid polygon fill is touted. Communications rates up to 38.4 Kbaud are supported. The 8820's preconverged CRT with auto-degaussing has a screen saver feature. Process symbols or full uppercase characters can be selected locally or from the host. Four character sets are available. Price for the terminal, in quantities of 100, is $2,965. **Intecolor**, Norcross, GA **Circle 233**

MOS Imaging Sensor Means Low Power



A micro-sized MOS imaging sensor combines developments that include auto-aperture lens control, special small lenses, high-precision semiconductors and high-density packaging. The camera

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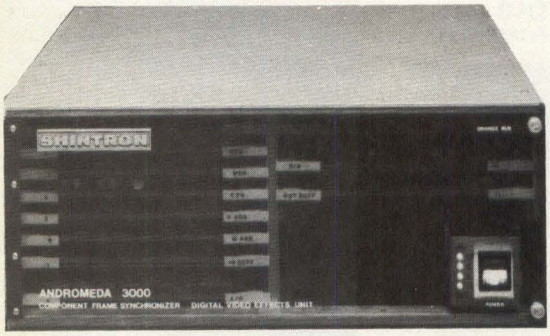

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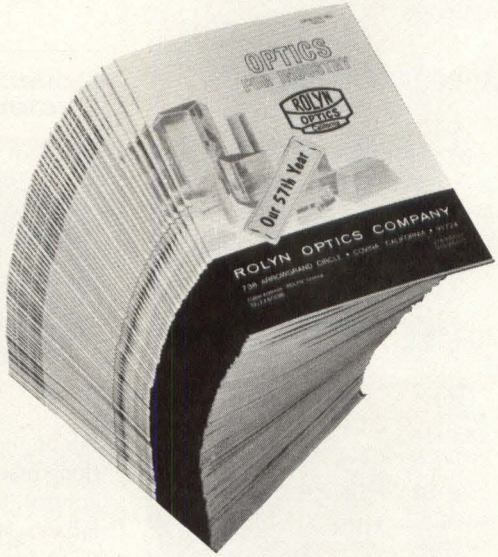

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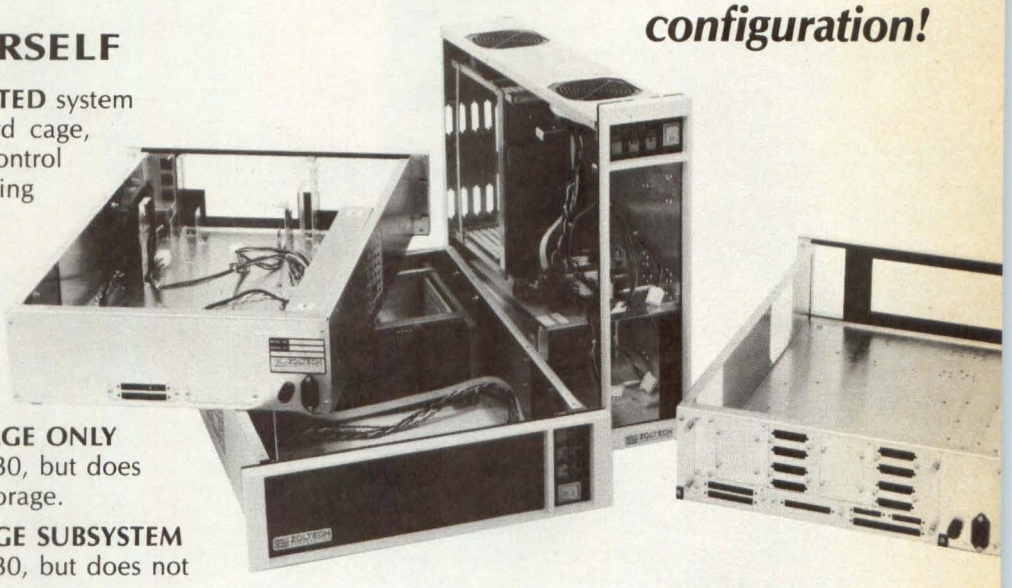

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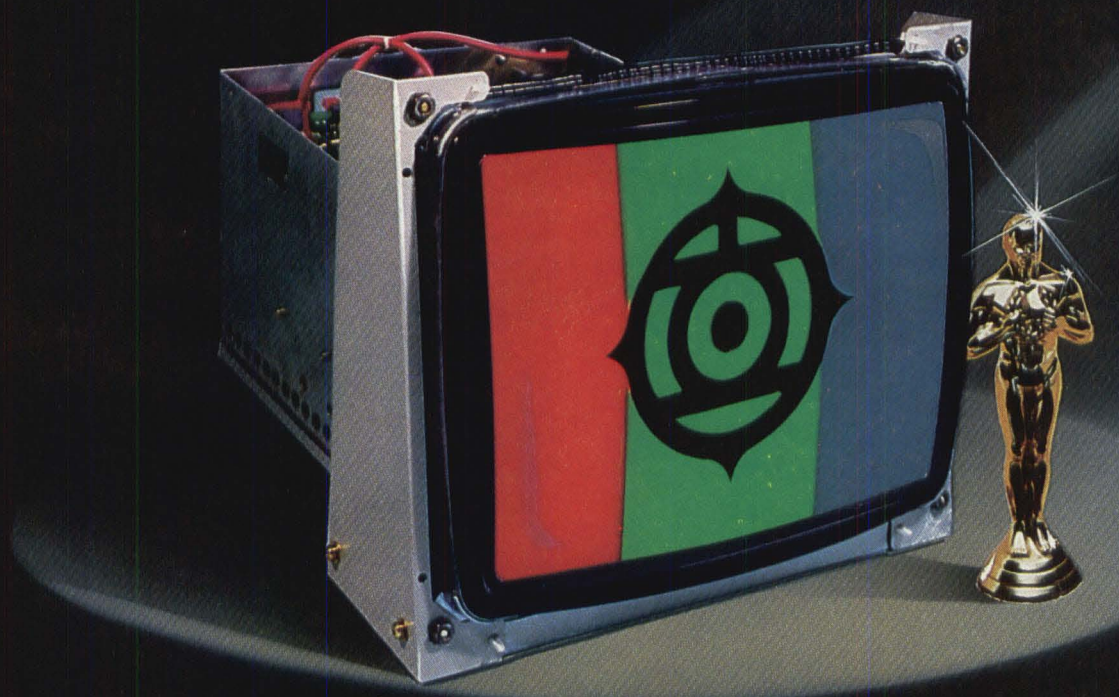

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