

# DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

SEPTEMBER 1984

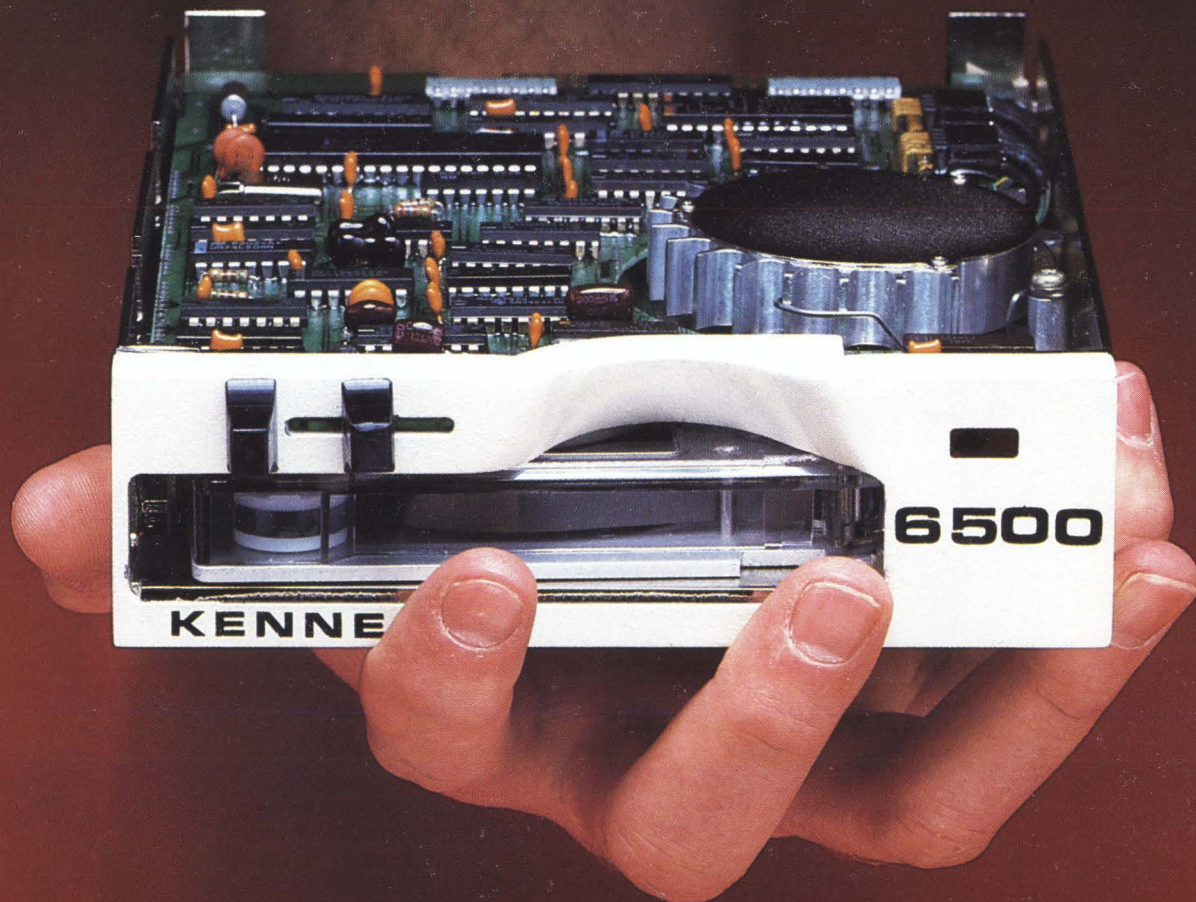


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- STD BUS: DIVERSITY AT THE LOW END
- SILICON SUPPORT FOR SOLID MODELING
- PROCESS CONTROL BRINGS INTELLIGENCE TO THE FACTORY FLOOR
- DEVELOPMENT TOOLS ■ EEPROMs ■ ERGONOMICS ■ DISK CONTROLLERS



# 'the handful'



Kennedy's Model 6500 5 1/4" Cartridge Recorder — it fits in your hand, but it's more than a handful of new and unique features, such as:

- 16 KBYTE Buffer — Model 6500 can transfer data at a burst rate of up to 3 MBYTE/sec., and maintain streaming longer in systems with little buffering.
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- Direct Drive Motor — Assures much higher reliability and lower I.S.V.

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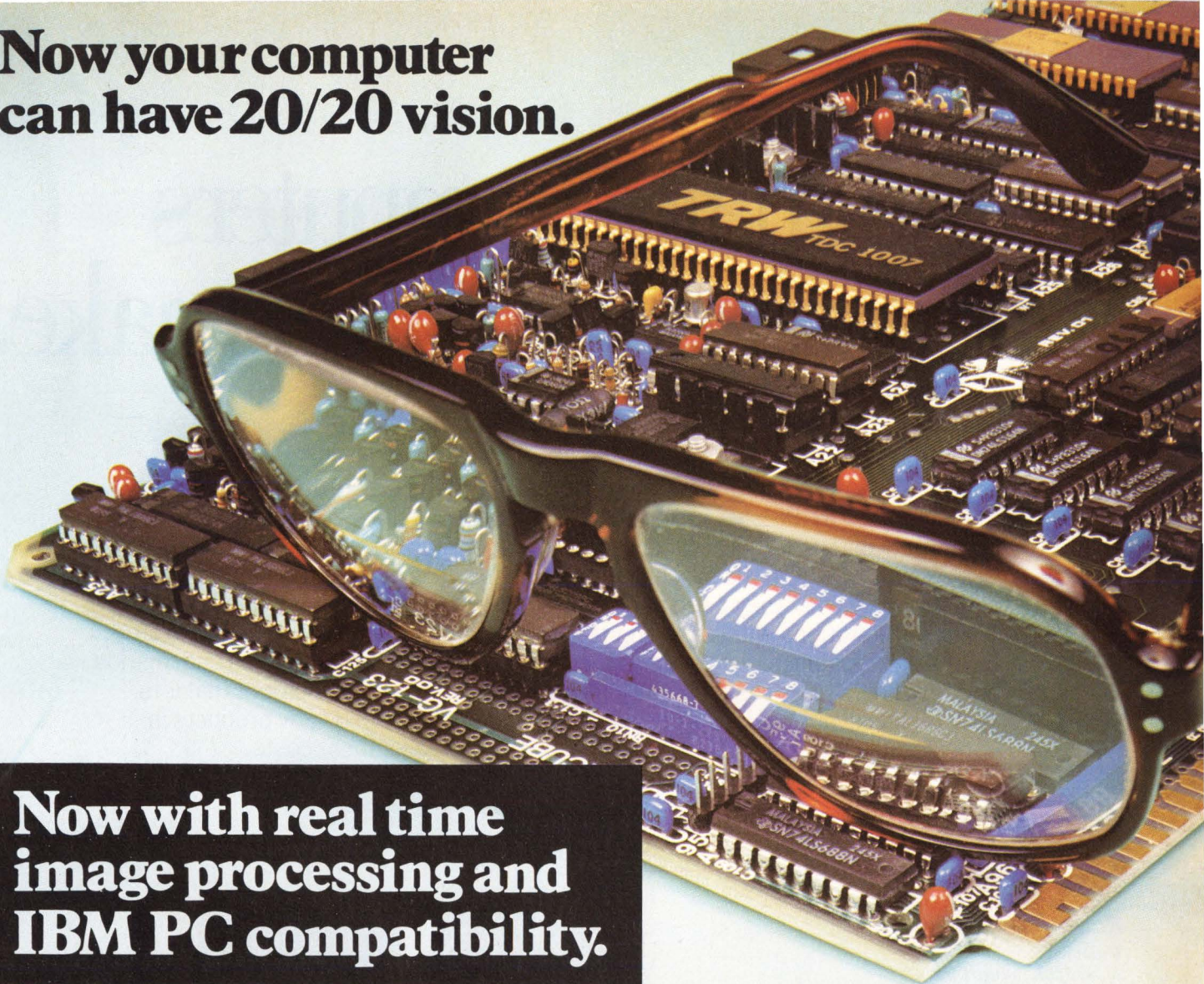
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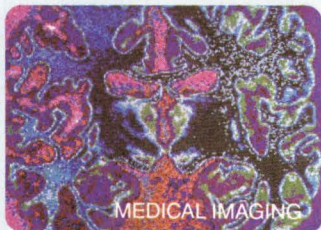
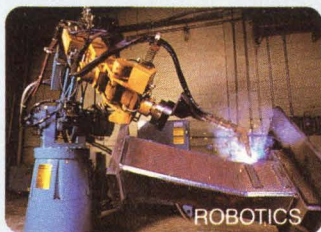
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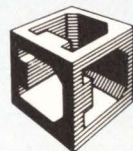
The new SP-123 offers advanced signal processing of high resolution black & white or full color images at the rate of 14 megapixels per second.

The new IVG-128 is a complete video acquisition and display module on a single IBM PC compatible card. It features input & output look up tables, an 8-bit digitizer, and RGB 8-bit outputs.

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## Datacube

We will look for you at Electronic Images 84

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# We make computers that design what you make.

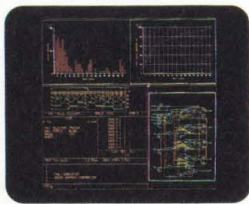
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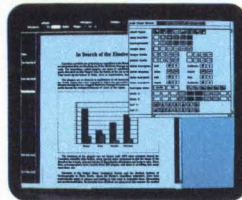
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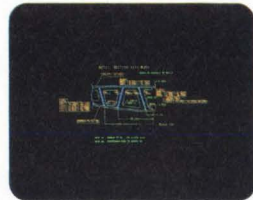
From left to right  
application software from:  
Mentor Graphics Corp.,  
Interleaf,  
Auto-Trol,  
Swanson Analysis  
Systems, Inc.,  
Racal-Redac,  
Automated Impact,  
GE/CAE International,  
ORACLE Corp.  
and GE Calma Co.



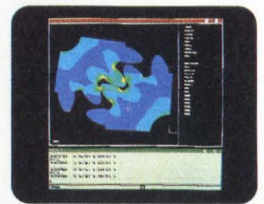
Logic design  
simulation.



Documentation  
with  
integrated  
graphics and  
text.



Design  
drawing of a  
bulkhead.



Finite  
element  
analysis of  
gear cluster.





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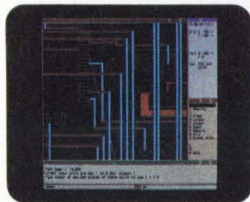
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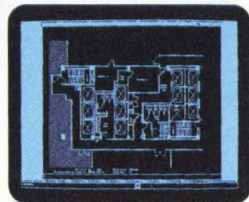
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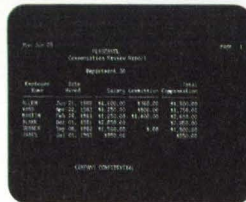
*Printed  
circuit board  
layout.*



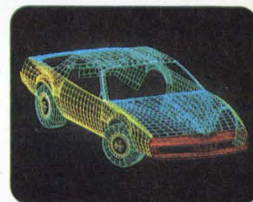
*Space plan  
of a  
facility.*



*Exploded  
solid model  
of an  
automobile.*



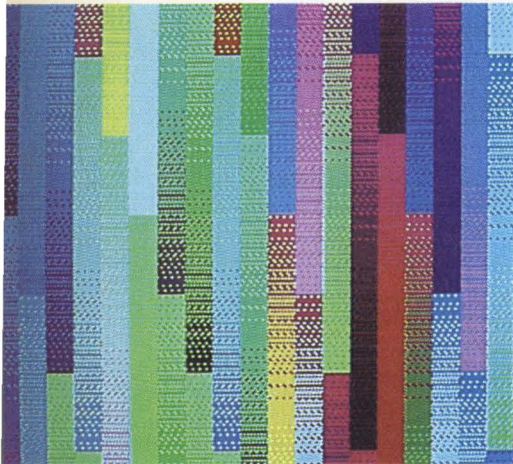
*Relational  
database  
management  
system.*



*3D surface  
model.*

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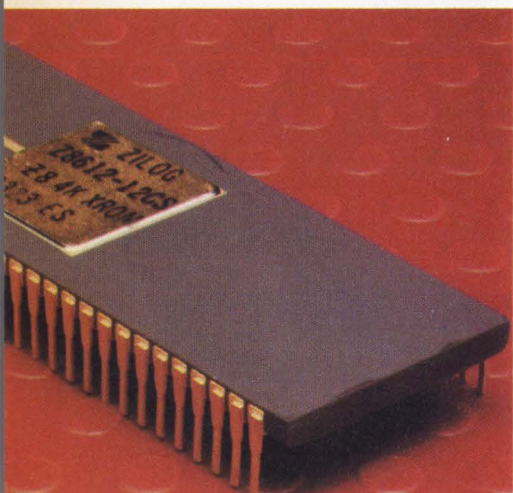
COURTESY XTAR

54 ICs for Solid Modeling



COURTESY FLUKE MANUFACTURING

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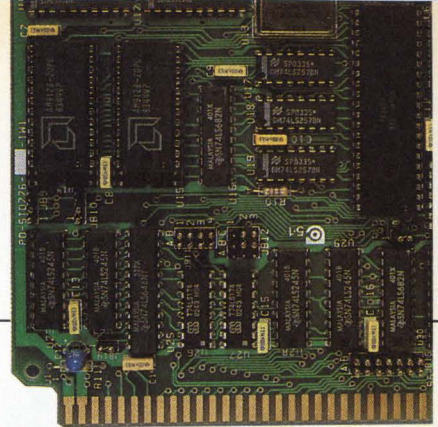
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While advances in memory technology, wide-word architecture, and high-speed bus design have generated higher performance, few advancements have made a greater impact than custom graphics chips.

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The range of applications for STD products, while traditionally very broad, is today continuing to grow, mainly in automation, process control, monitoring and data acquisition areas.

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Computing in the industrial environment has meant inputting data hand-delivered from the factory floor to a control room, but this is changing rapidly with intelligence and undisguised computers moving throughout manufacturing plants.

### **86** **Development Tools Take Aim At 32-Bit Chips**

by Ronald Collett

The prospective user has three main options when purchasing a development system: a dedicated system; a universal system; or an emulator and cross software for a host such as a VAX, PDP-11 or IBM PC.

### **96** **Function Determines Form In Workstation Ergonomic Design**

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Human factors evaluation labs are now a vital segment of the design process at many companies, using models or simulated ergonomic situations to specify variables affecting human behavior and design performance.

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by Stephen Goldman

The primary technical problem to overcome during the design of a caching disk controller is the limitation on cache access time.

### **108** **Designing With EEPROMs**

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Most EEPROM applications today include some type of single-chip microcontroller, so the combination of EEPROM on-board was a predictable step in the evolution of EEPROM.

## ON THE COVER

The STD bus is still one of the most flexible yet low-cost alternatives available to the systems integrator. Impetus from the new CMOS standard and systems that work hand-in-hand with the IBM PC, will retain the bus' foothold in the marketplace. The cover depicts the wide variety of cards currently available from Pro-Log. Photo courtesy Pro-Log Corp.

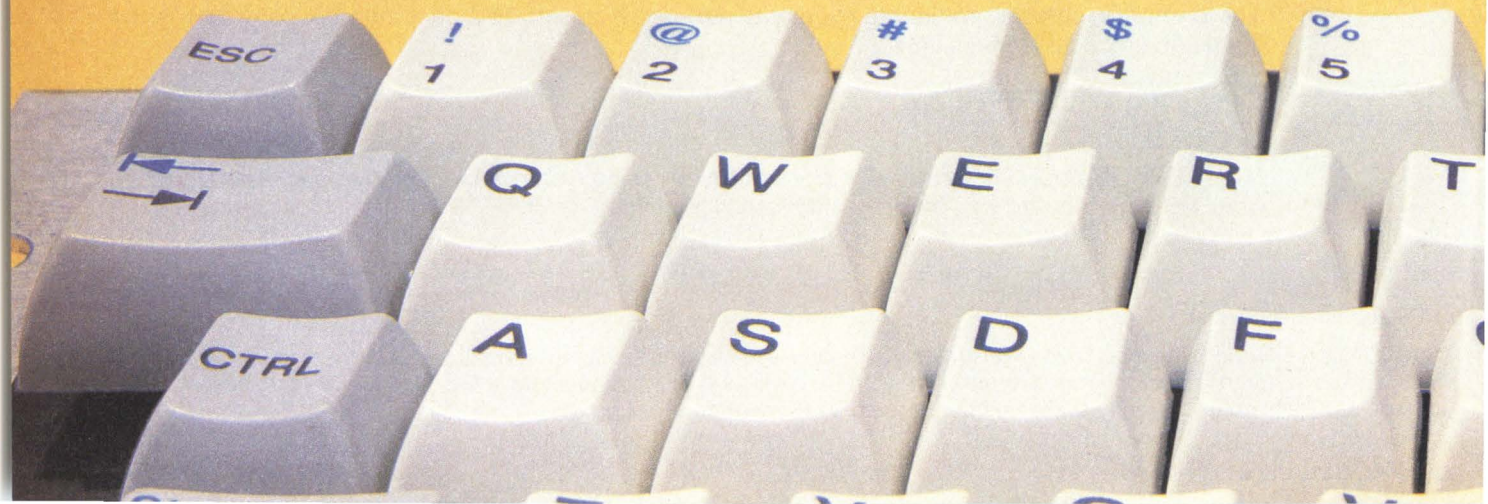


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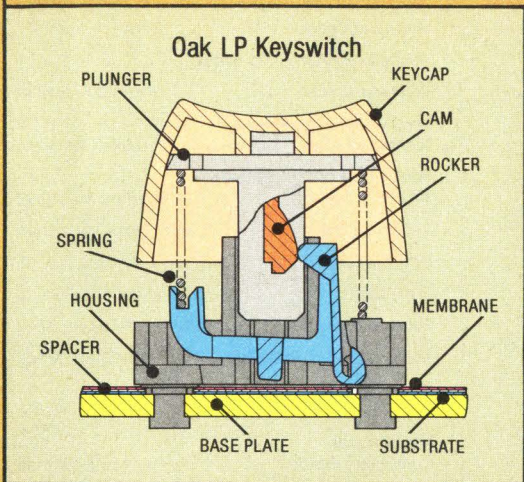
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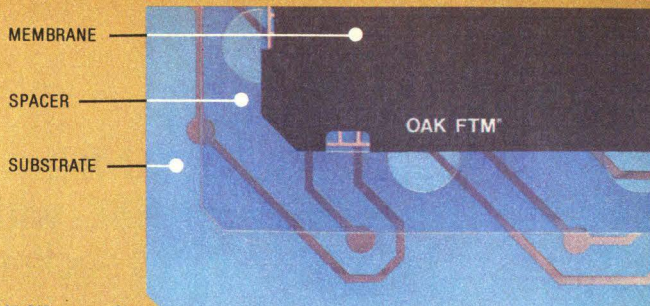
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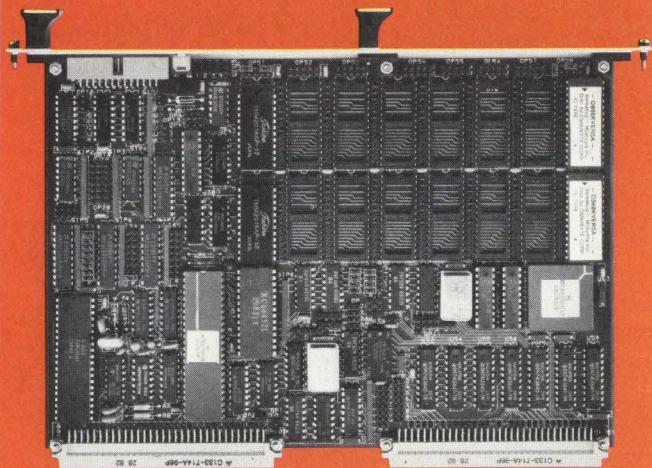


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*Lundy UltraGraf sets 3-dimensional standards.*

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with many other systems. And you have local storage of all control functions for the interactive input devices. This provides maximum input flexibility, with minimum keyboarding.

## **Lundy helps you see more in graphics.**

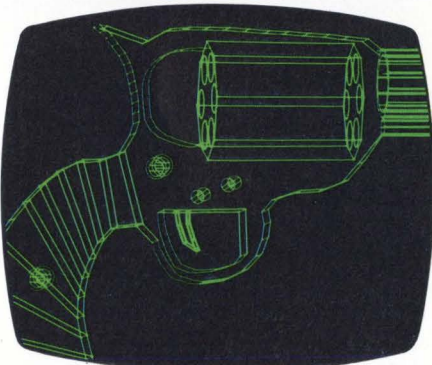
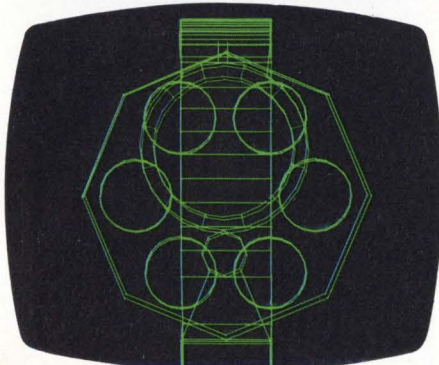
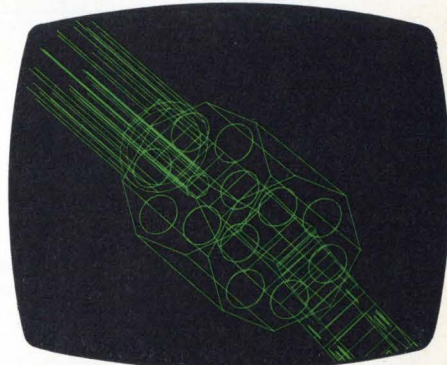
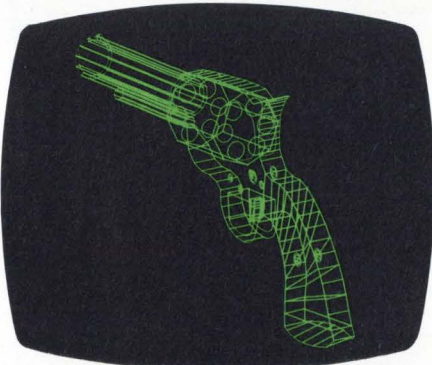
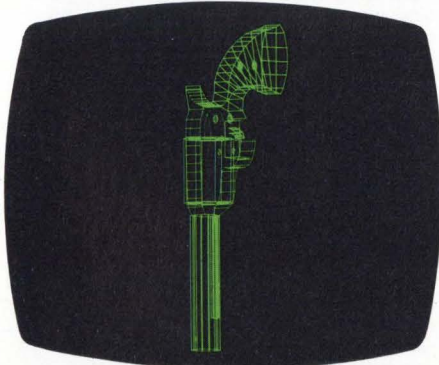
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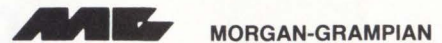


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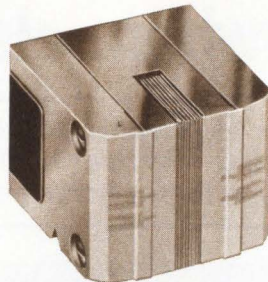
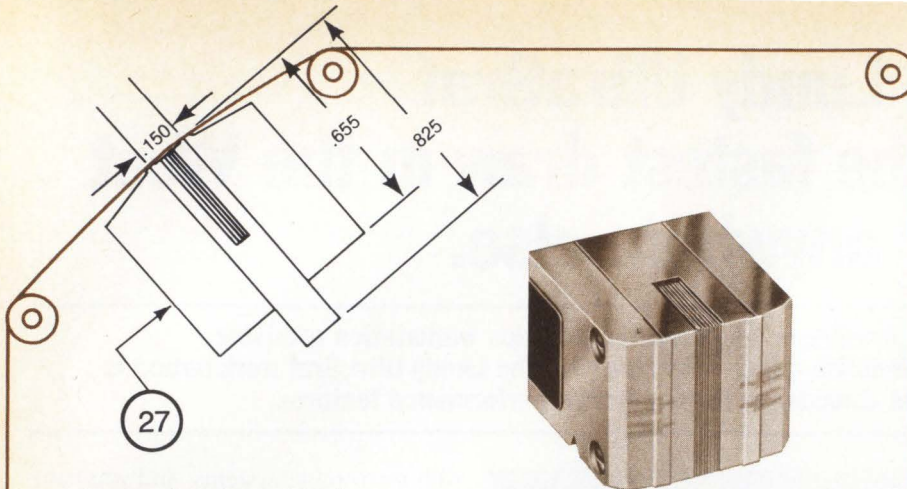
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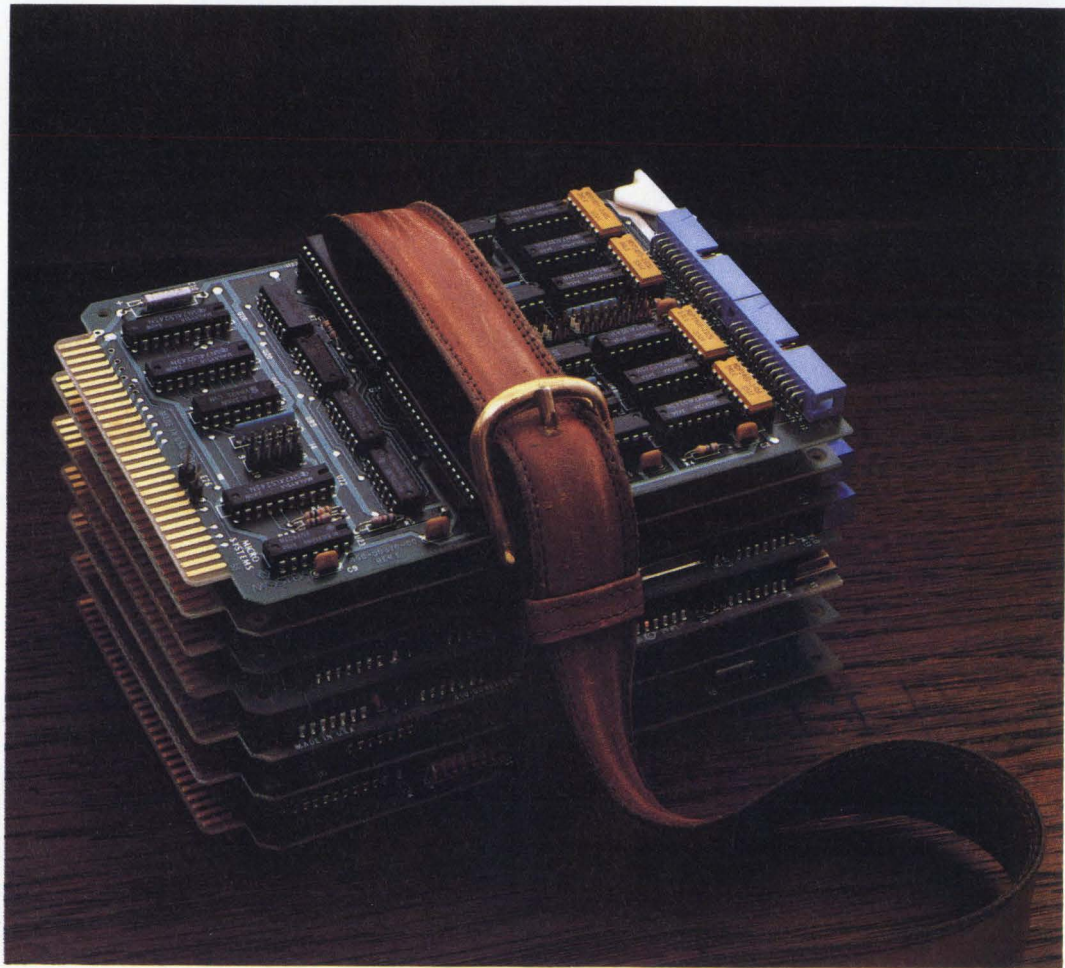
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Take advantage of our learning curve experience with the STD-Z80 BUS. It's a time-proven course that can add a degree of success to your own system designs. For more information, contact Mostek, 1215 W. Crosby Road, MS2205, Carrollton, TX 75006, (214) 466-8816. In Europe, (32) 02/762.18.80. In Japan, 03/496-4221. In the Far East (Hong Kong), 5-681157.

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‘Emerging new technologies and an evaluation of forthcoming approaches to system design almost dictate that the systems architect be a Renaissance Man.’

## EDITOR'S COMMENT

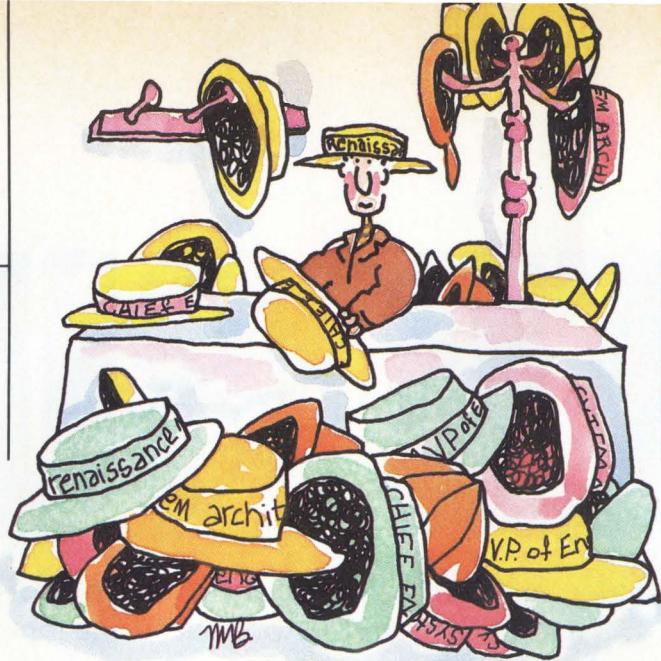
Computer systems design is increasingly becoming a field which dictates an approach involving combined talents from a number of widely varying disciplines. The communication between designers has always been vitally important to the success of any given project. Often, the coordination of these separate efforts is left to the talents of the systems architect who must have a global overview of the project at hand.

Today, the systems architect goes under a variety of guises — Chief Engineer, Project Engineer or Project Manager to name a few. This individual may have gained several years of experience and wisdom in many related design activities. At present, emerging new technologies and an evaluation of forthcoming approaches to system design almost dictate that the systems architect be a ‘Renaissance Man,’ able to take a broad overview of the industry in general, and be knowledgeable in specific technology areas.

Unfortunately, today many design engineers and engineering management have a very myopic view of their environments and are unable to appreciate broader implications of developments outside their particular realm of expertise. Computer design may be likened to a complex jigsaw puzzle where many pieces must interact to produce the whole picture. At the present, the pieces in the puzzle are becoming larger and consequently the systems architect must take one step back to get the full effect. Companies that do not insist on having several of these multi-talented employees will find themselves caught without the necessary insight into the industry and its future trends in order to effectively compete.

Computer architecture, based on the classical Von Neumann approach, has changed very little since the earliest machines. In the future, it will be challenged by alternative architectures, but it is likely that the jump to next generation architectures will be gradual rather than dramatic. The reason that the transition will take place at all, is due to the speed limitations of conventional hardware, programming languages and operating systems.

Over the past few years, the IC houses have been addressing the speed problem by announcing dedicated computational machines, and the system architect should be aware that developments will emerge there first. The newer devices will allow the distribution of processing over a number of system elements. At the IC level, fuse programmable controllers are emerging that will allow the designer to implement complex state machines and controllers by programming the appropriate series of microinstructions. Next year it seems likely that RISC machines will make their debut. First out will be popular versions of existing microcontrollers.



Following closely on the heels of RISC machines will be radical departures from the Von Neumann approach. Two products already in the marketplace are the Harvard architecture of the TMS320 and the NEC data-flow machine, a pipelined image processor, the  $\mu$ PD7281.

It has long been the case in the board business that the systems architect has been able to choose from modular building blocks with very specific functions with which to design his systems. Next generation bus structures offer a “functional partitioning” to maximize system throughput by the minimization of data movement throughout the system. At the system level, newer modular languages will allow for these advanced architectures to optimize program execution with a greater degree of parallelism and concurrency.

In the same way that today's system architects have recognized the potential of the latest generation of 32-bit microprocessors to challenge the role held by existing minicomputer designs, the future will dictate that the system architect not only hold an appreciation of alternative computer architectures but an understanding of how these architectures will be implemented. The important role of the applications specific IC, and in particular semi-custom ICs, will provide yet unheard of opportunity for a smaller start-up to get to market quickly with advanced products based on new architectures and break the dependency of the systems houses on the IC companies.

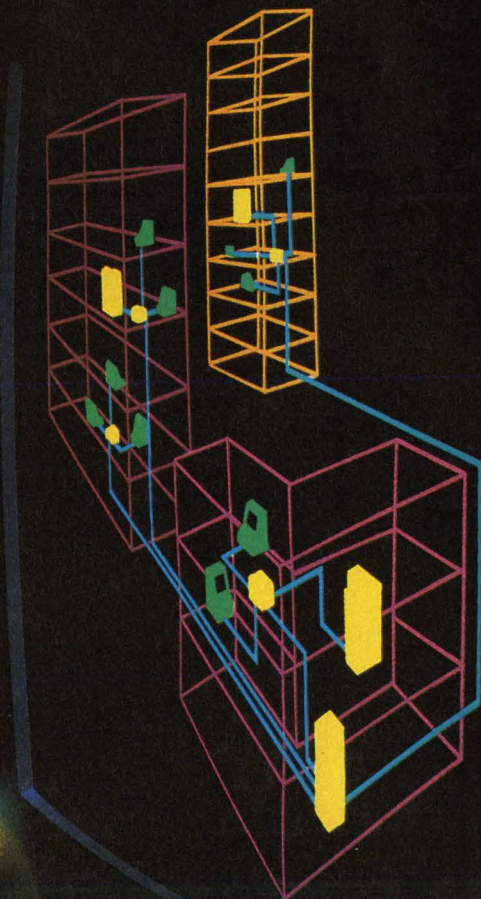
The challenges facing the system architect today may appear less complex, but system design necessitates an understanding of a variety of disciplines, technologies, and integration issues, ranging from ICs, boards, and peripherals to systems, as well as an awareness of the many design tools available to implement a system.

To effectively take advantage of the diverse opportunities that are and will become available, it is mandatory for the system architect to have an appreciation of alternate design options and future computer architectures. Only the system architect will be the individual with enough foresight to implement advanced system architecture in the most effective way using today's technology.

**Dave Wilson, Executive Editor**



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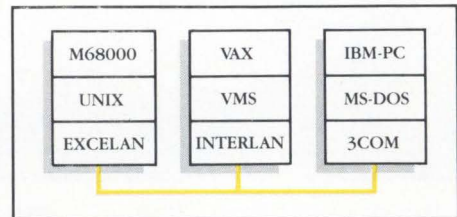
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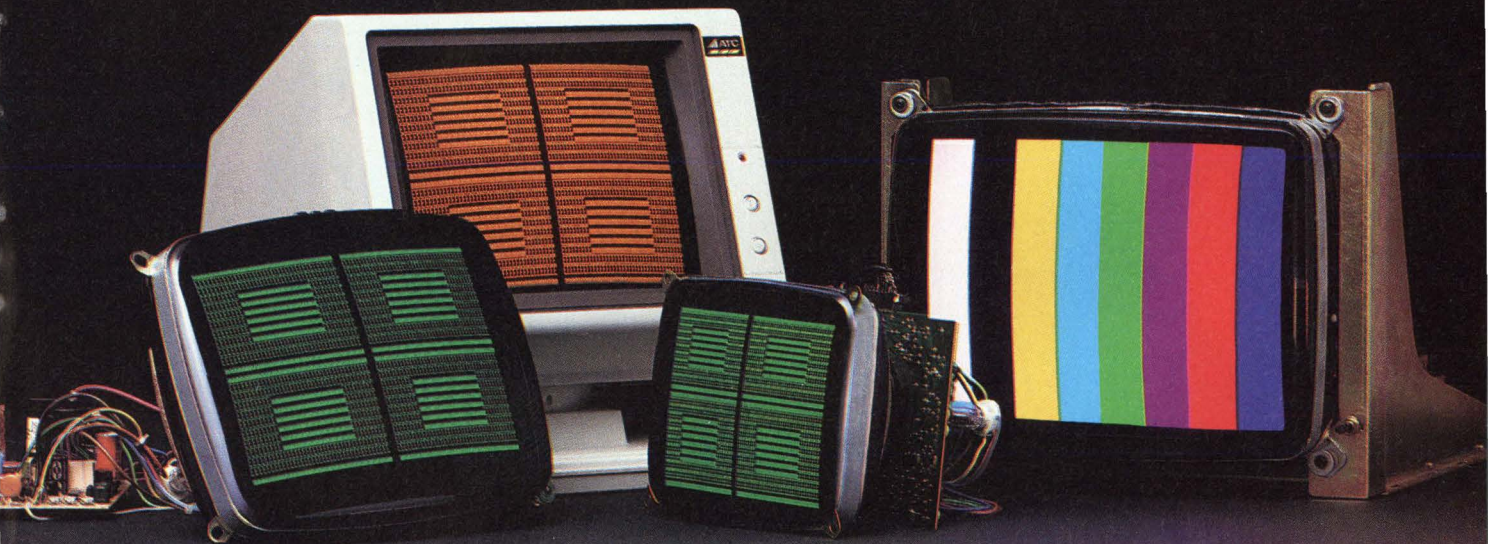
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# DISPELLING THE MYTH ABOUT SINGLE CHIP MICROCOMPUTERS.

This is the first in a series of technical papers from Zilog, designed to give engineers new insights into Zilog microprocessors—what advantages they provide for particular products and why they are the choice among engineers who need optimum performance.



Single chip microcomputers are marvels of advanced electronic technology. Going beyond even the tiny architectures of today's general-purpose microprocessors, they combine the functions of multiple chips to form a single-device solution. Indeed, they are awesome machines.

But after their introduction, myths grew up around MCU's. Designers believed that they were difficult to design with; that there wasn't sufficient hardware and software support for them; that those who selected them would get a Sisyphus Complex. Sisyphus, you remember, is the character in ancient Greek mythology who was condemned forever to push a rock up a hill. Just as the rock reached the top, it escaped Sisyphus and rolled back to the bottom.

Some MCU's, no doubt, deserve the stigma of this myth. But one definitely does not. Zilog's Z8® MCU Family. For there is more than enough evidence to prove that the Z8 chip is not only the fastest MCU around, but it's the easiest to work with, too. In fact, it should be the chip of choice for any dedicated control applications that must get to market

on time—even if you need large quantities of them to fill your needs. Because the Z8 device is available now for off-the-shelf delivery.

But what does ease of design mean to you? What do you look for when you select a chip? What do you need to make your job easier? Whatever it is, you'll find Zilog provides everything you need, and more:

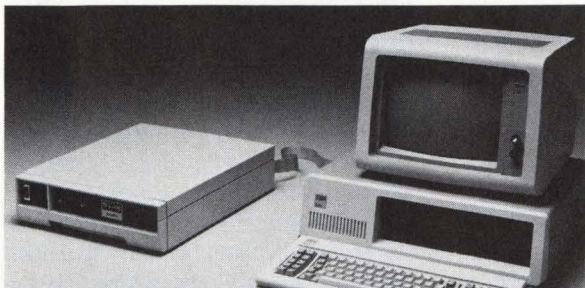
- Hardware and software development tools
- An existing software base
- Factory and field sales support
- Preproduction parts supplies

## Z-SCAN™ 8 PROVIDES REAL-TIME EMULATION CAPABILITIES.

Zilog's Z-SCAN 8 is an in-circuit Emulator with a combination of hardware and sophisticated software that gives you efficient, interactive emulation of the entire family of Z8 microcomputers. By the simple exchange of target devices, the selected Z8 MCU can be emulated in a real-time mode that gives you the ability to inspect and control the



tested environment. It also gives you real-time trace speed up to 12 MHz, two breakpoints, single-step capability and extensive mappable memory. All to ensure that you get an accurate simulation of your Z8 operating environment.



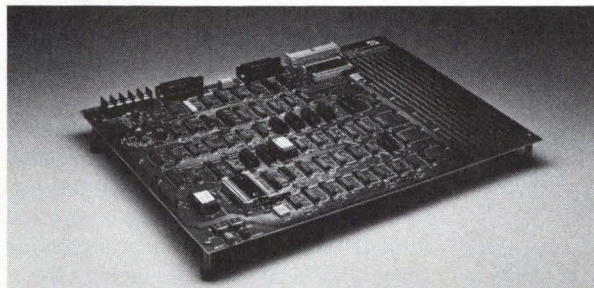
The Z-SCAN 8 Emulator is a combination of hardware and firmware that allows efficient, interactive emulation of the Z8 MCU. When hooked to an IBM PC software host, Z-SCAN 8 provides real-time, in-circuit development system capabilities. The Z-SCAN 8 will connect easily to other PC's making it a highly versatile unit.

The Z-SCAN 8 operates with both Zilog systems and other 8-bit development systems running CP/M® and/or other operating systems. Its standard RS-232 serial link makes it particularly useful with the IBM PC and other CRT terminals. Hardware and software debugging is fast and convenient. Two screens display the status of the Z-SCAN 8 monitor and Z8 MCU target resources. Target memory can be displayed and modified in a scrollable window. Moreover, the Z-SCAN 8 is interactive and easy to use. Commands are selected from menus and command arguments are self-prompting.

The set-up procedure and initialization for the Z-SCAN 8 is done for you—a unique feature in itself. The Z-SCAN 8 is designed to reduce design time. But it's not the only time-saving device Zilog provides for the Z8 MCU.

## THE Z8 MCU DEVELOPMENT MODULE CUTS HARDWARE AND SOFTWARE DEVELOPMENT TIME.

The Z8 Development Module (DM) features two 4K Z8 devices on a single-board microcomputer. It's designed to assist you in the development and evaluation of hardware and software designs based on the Z8 MCU. With it, you can easily build a prototype using the Z8 prototyping device, and then develop code that will eventually be mask-programmed onto the Z8 on-chip ROM.



The Z8 Development Module allows you to build a prototype using the Z8 prototyping device, thereby developing code that will eventually be mask-programmed into the Z8 on-chip ROM. The Module is a single-board microcomputer system designed to develop and evaluate hardware and software designs based on the Z8 family.

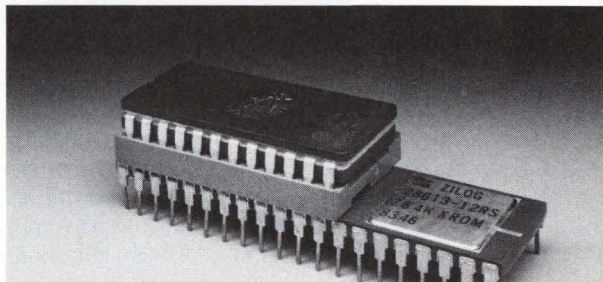
The Development Module connects to the CRT terminal and host system through two on-board RS-232 serial ports. So the DM fits between the CRT and host. A simple command makes the DM transparent in the serial path, which allows software

to be developed on the host-resident assembler without disconnecting the DM from the CRT and host.

The DM has a range of features to make Z8 designs easier than you ever thought possible: • 4096 bytes of static RAM for convenient creation and debugging of user code; • an on-board socket that tests user code in a 2716 or 2732 EPROM; • up to 4096 hardware breakpoints on address compare that can cover the entire internal ROM space; • a wire wrapped area for prototyping; and much more.

## Z8 MCU DEVELOPMENT SOFTWARE SPEEDS UP DESIGN TIME.

Zilog also provides you with a growing library of sample programs and convenient assembler packages to help you get started testing your Z8 MCU designs. In our Subroutine Library, for example, there's our arithmetic subroutine, an I/O subroutine and a general control subroutine. What's more, there are several versions of the Z8 device: a 2K and 4K ROM version; a ROMless version; and a Protopak for prototyping. Each offers different memory addressing structures. Zilog is developing more all the time. Plus, there's an existing software base for all the Z8 MCU's. We can provide you with samples of designs currently in use.



The Z8613 MPE is used for prototype development and preproduction of mask-programmed applications. The Protopak is a ROMless version of the standard Z8611, housed in a pin-compatible 40-pin package.

## SERVICE AND SUPPORT AT EVERY LEVEL FOR YOUR Z8 MCU DESIGNS

From the factory to the field, Zilog provides support at every level. A worldwide field sales network stands ready to help you with both hardware and software support. And you can get all the Z8 MCU's you need right now. Yields for the device are up 40%, and price reductions reflect our new supplies. What's more the upcoming Z8 Super 8™ promises a smooth migration path for today's Z8 MCU family.

Zilog's Z8 single chip microcomputer. Believe the myths. Or get the facts. If bringing your product to market is important to your business, then design with the part that does more for success than any other. The Z8 MCU makes getting over the design hill and into production a lot easier than you might think.

For more on the Z8 MCU, send for our complete overview or call our Literature Hot Line at 800-272-6560. For seminar dates and locations, or information on Zilog training, call (408) 370-8091. Or write: Zilog, Inc., Technical Publications, 1315 Dell Avenue, MS C2-6, Campbell, CA 95008.

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## Daisy Forms Personal Systems Division

Daisy Systems Corp. has formed a new division, responsible for research and development, engineering and marketing of Daisy's Personal LOGICIAN family of products. These new products are part of Daisy's Distributed CAE strategy and are aimed at making systems design teams more productive. The new division has its own research and development, engineering, and marketing groups and will take advantage of Daisy's existing manufacturing, field operations and application software groups.



## Voice/Data Workstation

Cermetek Microelectronics, Inc., announced that it has received a contract from Liberty Electronics for more than \$1.5 million to provide the manufacturer of video display terminals with an intelligent modem. The product is a 1200 or 300 bit-per-second modem module which mounts directly onto a printed circuit board which is inserted into Liberty's new Freedom 212 Remote Information Station, a voice and data communications workstation.

## Vertex To Supply Hewlett-Packard

Vertex Peripherals Inc., manufacturers of a family of 5 1/4" Winchester disk drives, announced it has signed an OEM agreement with two divisions of Hewlett-Packard Company. Product deliveries for an undisclosed number of 31- and 72-Mbyte unformatted drives have already begun. The contract value was not disclosed. HP will incorporate the drives as options in its small business and technical computers, and the company will use the Vertex drives to support up to 10 different product families. HP will begin customer-based shipments of systems OEMed from Vertex in early Fall.



## Xebec Forms Subsidiary

Xebec announced the establishment of Epelo Corp., a majority-owned subsidiary company dedicated to the design and development of disk drives. Frank C. Gibeau, founder and former president of disk drive manufacturer, Atasi Corp., is president of the new subsidiary.

## Harris, Intel Announce New Exchange Agreement

Intel Corp. and Harris Corp. have signed a technology exchange agreement covering the development of microprocessors and telecommunications circuits based on CMOS technology. Under the agreement, Harris will be a second source for Intel's new 29C51 codec/filter combination circuit, a third generation CMOS VLSI product. The bus structure allows telecommunication systems designers to upgrade an analog-only switch to an integrated voice/data switch without the need for major system redesign. In addition, Harris and Intel will collaborate on a CMOS design for a new analog-to-digital voice processing circuit.

## FutureNet Announces Racal-Redac Interface

FutureNet Corp. has developed a new interface translator to transfer the designs created on its DASH-1 Schematic Designer to Racal-Redac's printed circuit development system. The new interface eliminates the task of manually entering, and perhaps translating, design net lists, so designers can now proceed more quickly to board layout.

## PerSci Acquires Cipher's Drive Line

PerSci, an EF Industries company, has acquired all the rights to the cartridge disk drives, drive subsystems and related drive equipment of Cipher Data Products. PerSci will assume responsibility for depot maintenance and warranties on cartridge disk drive products now in use or to be manufactured by Cipher through Sept. 1, 1984. PerSci also acquired the manufacturing rights to the products.

## Alternate Source Agreement For Byte-Wide EEPROM

National Semiconductor Corp. and Synertek, Inc. have signed an agreement under which National will serve as a licensed alternate source for Synertek's 2,048-bit SY2802E EEPROM. National's version of the part will be designated as the NMC9802, and will be available in either a ceramic (J) or molded plastic (N) package. Production quantities are scheduled to be available by the end of 1984.

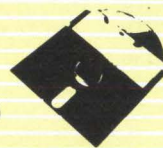


## Monolithic Second Sources Fujitsu

Monolithic Memories, Inc. signed an alternate source agreement with Fujitsu Limited of Japan, covering high-performance, bipolar TTL gate arrays. Fujitsu will supply technical support and information required for Monolithic Memories to develop, manufacture, and market Fujitsu's line of TTL gate arrays. The devices to be transferred will be Fujitsu's B240, B350, B600, B1100, and B2000 gate array products. Estimated availability of the first products from MMI is 1985.

## IBM PCjr To Use Tabor Drives

Xetec, Inc. (Salina, KS) has signed an OEM agreement with Tabor Corp. for micro-floppy disk drives that will be used in Xetec's newest product, a 3 1/4" dual disk package for the IBM PCjr. Xetec is a systems integrator, and supplier of personal computer enhancements to major systems users.



## Printers For Data General

Centronics Data Computer Corp. signed a four-year multi-million dollar contract with Data General Corp. to supply a customized version of its Printstation 350 Series printers to the computer manufacturer. Centronics is a manufacturer of line and dot matrix printers with sales and service worldwide.

## VLSI Technology And Western Digital Agreement

VLSI Technology, Inc. (VTI) and Western Digital have entered a long term agreement that will feature new product co-definition and co-development, immediate second sourcing of specific products, and certain product conversion from NMOS to CMOS technology. Western Digital will grant VTI second source rights on the WD2123 (DUAL UART), WD1933/1935 (SDLC), WD9216 (DATA SEPARATOR) and selected disc controller products. The companies will jointly develop key Megacell building blocks based on WD's product architectures for use in custom IC designs to be built and marketed by both companies.



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**Practical in terms of cost:** Mini-MAP is available as an economical, four-board set or as a packaged system. Now, with Mini-MAP, OEMs can offer their customers a better product at lower costs. Mini-MAP's low power demands, small size, and high reliability make the package extremely attractive. And end users will find our FORTRAN compiler and other software tools minimize program development costs.

## We built Mini-MAP.™

32-bit DEC™ floating point format  Interfaces to DEC PDP-11, LSI-11, and VAX-11 series  Up to 16 MBytes of data memory  1024 x 1024 2-D FFT in 8.8 seconds  Extensive software tools plus dedicated applications assistance including training, convenient parts depots, and field service staff support our worldwide installations. To find out how Mini-MAP can work for you, call toll free 1 800 325-3110.

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## Parallel Computers, Data Phase Sign Agreement

Parallel Computers and Data Phase Corp. announced a \$4 million sales agreement under which Data Phase will purchase approximately 60 Parallel 300 minicomputer systems over the next 18 months. Data Phase, a supplier of library-automation systems, will install its Automated Library Information System (ALIS) software on the fault-tolerant Parallel 300s for resale as integrated turn-key systems to libraries across the country.

## Faraday, NCR Contract

Faraday Electronics signed a contract with NCR Corp. under which NCR will use its PC-DOS compatible CPU products in the NCR 7921 Personal Computer Engine and the PCIV. The contract involves both the sale of standard format micro-CPU's and the design and manufacture of custom form factor boards for NCR.

## Wangtek Contracts for 1/4" Cartridge Tape Streamers

Wangtek, a manufacturer of half-high, 5 1/4" cartridge tape streamers, has signed OEM contracts totaling \$65 million in eight months for its Series 5000E 1/4" cartridge tape drives.

## INMOS Licenses Technology To Japan

INMOS has reached agreement with the NMB/Minebea Company of Japan to license the INMOS 256K Dynamic RAM. The agreement concludes a worldwide search by NMB for VLSI technology to install in their new wafer-fabrication facility currently under construction. In return for a substantial initial payment and continuing royalties, the agreement provides for INMOS to transfer its advanced dynamic RAM CMOS technology to NMB and to license NMB to manufacture INMOS' yet-to-be-announced 256K x 1 Dynamic RAM.



## Lattice And Synertek Cross-License

Lattice Semiconductor Corp. (Portland, OR), has entered an agreement providing Lattice with a portion of the production capacity from Synertek Inc.'s wafer-fabrication facility at Santa Cruz, CA. Synertek now has license to manufacture Lattice's high-performance 64K static RAM design as well as the process technology to produce it. The two companies also agreed to cross license and second source future products designed to the static RAM process.

## Elxsi Signs With Valid

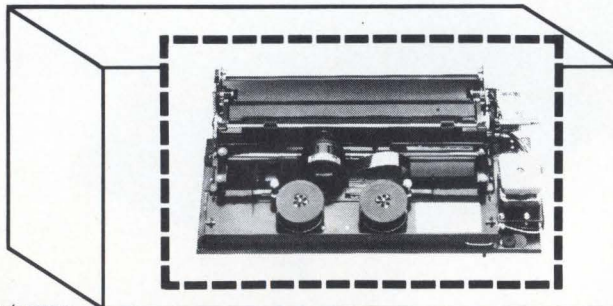
Elxsi has signed a marketing agreement with Valid Logic Systems, Inc. (Mountain View, CA), to market Elxsi's System 6400, an expandable, general-purpose 64-bit multiprocessor computer, with Valid's SCALDsystem workstations. The System 6400 will serve as a host processor to Valid Logic's graphics design station.

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Star Micronics is a leading manufacturer of high quality, high performance, printer mechanisms.

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# Our Family has a New Generation...

Plessey, a leader in the DEC\* compatible marketplace, has once again expanded its family of micro computer systems. In addition to our LSI-11/23\* based 6000 series, Plessey is pleased to announce the higher performance 8000 series based on the NEW DEC LSI-11/73.

Similar to our 6000 series, the 8000 series offers you the most popular peripherals available today. Plessey offers Winchester Disc technology in 10 Mb, 20 Mb, 40 Mb, or 80 Mb capacity to handle your storage needs. Also available is our new 40 Mb drive, [20 Mb fixed, 20 Mb removable].

For all your backup needs, Plessey provides a choice of 1/4" start/stop streaming tape with 70 megabytes of backup storage capacity or our 20 Mb streaming tape. We also offer 1/2" streaming and start/stop drives and RX02 compatible floppies.

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## **Congress Limits Sole-Source Contracts**

In a catch-all bill that is supposed to raise federal revenues and cut the deficit, Congress has included tough new restrictions on sole-source contracting. Long a target of the House Government Operations Committee, sole sourcing is often cited as one reason for the enormous waste in the government procurement system.

Rep. Jack Brooks (D-TX) has indicated that almost two-thirds of the annual federal procurement is done through the non-competitive sole-source contract method. At current budget levels that would total some \$100 billion each year in direct awards. The new legislation requires competitive bids, except in certain limited cases, such as there being only one source for an item, the possibility that national security would be compromised by open bidding, or an unusually urgent need that precludes the normal bidding process.

Also stiffened were the host of government justification procedures for not using competitive bids. The rules about notice and approval which must accompany any sole-source contracting procedure now include informing Congress 30 days before the award is made. Companies that believe they have been unfairly excluded from bidding on a particular contract can appeal to the General Accounting Office, Congress' budget arm, for a hearing.

## **Computer Crime Bills**

The House and Senate have approved, and the President is expected to sign, a bill that authorizes the Small Business Administration (SBA) to set up a computer crime education program for small businessmen. The bill permits the SBA to work with private firms and set up seminars and courses on how the owners of small businesses can protect themselves from various types of computer abuse. The bill also includes a favorite Washington patronage vehicle — the advisory council. In this case, the selected government and private-sector members would advise the SBA on issues relating to computer crime.

Also moving forward, but stalled temporarily in election year recesses, is the Counterfeit Access Device and

Computer Fraud and Abuse Act. Introduced in the House by Rep. William Hughes (D-NJ) and approved by the Judiciary Committee, the bill outlines new laws about credit card fraud. In addition, it establishes a new felony offense for computer crime aimed at computer hackers. Persons trespassing into a government computer, causing damage greater than \$5,000 in one year, or taking more than \$5,000 illegally through a computer scam, could now be prosecuted under federal law.

## **AEA Opens Tokyo Office**

The American Electronics Association, with the help of a \$500,000 grant from the US Department of Commerce, has opened an office in Tokyo, Japan, to improve the access of US firms to Japanese markets. The office will lobby on behalf of US interests, collect and disseminate technical data on Japanese industry, act as a liaison with Japanese industry groups and provide support for association members trading in Japan. Heading the office will be John Stern, a specialist in US-Japanese trade.

## **Australian Government Promises Copyright Law**

Bowing to heavy pressure from the country's computer industry, the Australian Labor government has announced that it will introduce legislation to amend the Australian Copyright Law to include protection for computer software.

Last December, in a suit brought by Apple Computer against a look-alike Wombat computer, Apple charged that Wombat violated its copyright. The Australian Federal Court judge handling the case ruled that Australian copyright rules did not cover computer software. Since that ruling the software industry in general has been confused about what protection is available in Australia for their products. Many copyright attorneys, such as Susan Nycum of Gaston, Snow, Ely, and Bartlett in Palo Alto, CA have advised US companies to avoid business in Australia until the situation is clarified.

Lobbyists from the Australian computer industry claim many companies are following that advice and they face a virtual embargo from overseas software producers. The government is

proceeding with the legislation to provide relief for the industry until the full Federal Court reviews the Apple case.

In the statement announcing the plan to push for copyright protection the government said, "There are real risks of a withdrawal or limitation on the availability of imported software in the absence of copyright protection... The majority of software packages used throughout industry, manufacturing, mining and commerce are imported under license, and limitations on the availability of such packages would be a major setback to productivity and to Australian industries' endeavors to modernize."

## **US Army Evaluates Computer Contracts Series**

The Army's Computer Systems Selection and Acquisitions Agency has a vast range of computer contracts in progress. Competitive bids have been received on a two-year contract to supply field commanders with microcomputers. Although no dollar amount was given for the contract value, it is expected that the two vendors selected would supply large numbers of the machines. The Navy and Air Force recently awarded a joint contract for micros to Zenith Data Systems.

Other projects in the works at the agency include a contract for two large-scale IBM or compatible computers for the Korean Intelligence Support System, point of sale processors for 63 Army commissaries, a replacement system for the Pentagon's Consolidated Telecommunications Center, and a mobile computer system for Army forces in Europe.

## **Postal Regions Select Hardware**

The US Postal Service has prepared a list of qualified vendors for its four regions and will permit each region to select its own hardware system. Among the list of manufacturers who made the list are IBM, Digital Equipment Corp., Data General Corp., NCR Corp., Wang Laboratories, and AT&T. Industry observers say AT&T has the inside track in the Central division to land a multi-million dollar contract to provide its new 3B2 and 3B5 minicomputers to the postal automation project.



# Suddenly, everyone's headed for MARS.

## The MARS-432 32-bit, programmable, floating point array processor.

And with good reason. Because the MARS-432 has opened up a new world of speed, power and ease-of-use that's hard for anyone to resist.

The MARS-432 already interfaces with some of this world's leading computers — DEC, Apollo, Elxsi — to provide users with a new level of computational power. Interfaces for other leaders such as IBM, Perkin-Elmer, and Gould/SEL are scheduled to arrive soon.

Simply put, we're setting the direction in state-of-the-art array processors with features such as:

### Programming Ease

All of the computational power of an array processor doesn't mean much if accessing that power requires days of tedious programming, debugging and reprogramming. That's why we engineered the MARS-432 with an architecture specifically designed to support a FORTRAN compiler and a screen-oriented debugging system that make accessing and utilizing its raw power a very civilized process.

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## Tektronix Launches New Line Of 32-Bit Workstations

Tektronix's (Beaverton, OR) entry into the CAD/CAE arena this month marks a major event in the world of engineering workstations. Attacking the market with full force, the firm unveiled the 6000 Series of four workstations (6120, 6130, 6210, 6212) and an instrument controller (6110). The intelligent graphics workstations can be used as standalone systems, networked together or linked to a mainframe. This product offering will compete with similar products from vendors such as DEC, Apollo, Sun, Daisy, Mentor, Metheus and Valid.

With engineering projects demanding larger design teams, communications between systems has become a primary consideration. Integration of the Tektronix systems into existing CAD environments is achieved through terminal emulation (RS-232) and by connecting workstations together via the IEEE 802.3 standard (Ethernet). Supporting software handles communications services such as the ability to transfer files between workstations and log in to a remote workstation.

Recognizing the trend toward supporting established "standards," the 6000 Series

runs the UNIX operating system, except the 6110 instrument controller which runs the firm's real time operating system RTOS. The 6110, however, will execute object code generated by other family members. In addition, the 6120 and 6130 can be configured to run CP/M-86 and MS-DOS. The Tektronix implementation of UNIX includes the major features of System V and Berkeley 4.2, with local area networking, virtual memory and demand paging. Other standard interfaces that the new line accommodates include: RS-422, Centronics, Multibus, SCSI and IEEE-488.

TEKTRONIX 6000 FAMILY HARDWARE SUMMARY					
	6110	6120	6130	6210	6212
<b>Processors Standard</b>	32016 CPU	32016 CPU 32-bit display processor* 32081 I-P Proc.	32016 CPU 32-bit display processor* 32081 FP Proc. PC Co-Processor	32032 CPU 32016 I/O processor 32-bit and 24-bit slice display processor* 32081 FP Proc.	dual 32032 CPUs 32016 I/O processor 32-bit display 24-bit slice display processor* 32081 FP Proc.
<b>Optional</b>				32032 CPU	32032 CPU
<b>Memory Standard</b>	265K	1MB	1MB	1MB	4MB
<b>Optional/Additional</b>	512K, 1 & 2MB	1 or 2MB	1 or 2MB	9MB	16MB
<b>Storage Standard</b>	360KB diskette	360KB diskette 10MB Winchester	360KB diskette 20MB Winchester	40MB Winchester.	80MB Winchester
<b>Optional</b>	10 or 20 MB Winchester	20,40 or 80MB Winchester (repl) external 40MB cart. tape external Winchester disk	40 or 80MB Winchester (repl) 40MB cart. tape	80MB Winchester 40MB cart. tape 9-track tape 300MB SMD disks (1.2GB max) 360KB diskettes	80MB Winchester 40MB cart. tape 9-track tape 30MB SMD disks (1.2GB max) 360KB diskettes
<b>Interface Ports Standard</b>	RS-232-C (2) GPIB	RS-232-C (2) GPIB LAN	RS-232-C (2) GPIB LAN	RS-232/RS-422 RS-232-C (3) LAN 8-bit parallel	RS-232/RS-422 RS-232-C (3) LAN 8-bit parallel
<b>Optional</b>	High-speed GPIB 24-bit parallel 8-bit parallel Multibus adaptor Addit'l RS-232	High-speed GPIB Hi-speed serial 24-bit parallel 8-bit parallel SCSI Multibus adaptor Addit'l RS-232	High-speed GPIB Hi-speed serial 24-bit parallel 8-bit parallel SCSI Multibus adaptor Addit'l RS-232	High-speed GPIB** Hi-speed serial** 24-bit parallel** SCSI** Multibus adaptor Addit'l RS-232**	High-speed GPIB** Hi-speed serial** 24-bit parallel** SCSI** Multibus adaptor Addit'l RS-232**
<b>Display Systems Standard</b>	15" monochrome, 640x480	13" color, 640x480			
<b>Optional</b>	13" color, 640x480 4010 Series 4100 Series 4110 Series	15" monochrome, 640x480 4010 Series 4100 Series 4110 Series	19" monochrome, 1024x768 19" color, 1024x768 4010 Series 4100 Series 4110 Series	19" monochrome, 1024x768 19" color, 1024x768 4010 Series 4100 Series 4110 Series	
	*display processor comes standard in the 6000 Series display systems				
	**mid 1985 availability				

Figure 1: A brief summary of the hardware and software specifications for the Tektronix 6000 Series.



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Tektronix 6200 Series Intelligent Graphics Workstations use multiple 32-bit CPUs. The 6212 Workstation with a 6000 family display in the foreground is connected to the Tektronix 4115B Display Terminal with 4691 color graphics copier support and to the 4695 color graphics copier. The cabinet at right houses two 300 Mbyte SMD disk drives and a 9-track tape drive.

The 6000 Series is based on National Semiconductor's Series NS32000 microprocessors. At the low end of the 6000 line, the 6110 instrument controller, the 6120 and 6130 workstations are configured around National's 32016 microprocessor (32-bit internal/16-bit external architecture). A summary chart of the hardware and software specifications is shown in **Figure 1**. The 6120 Intelligent Graphics Workstation is aimed at the data analysis market segment for scientific, engineering and instru-

ment control applications. Similar to the 6120, the 6130 includes an enhanced version of UNIX and a 20 Mbyte Winchester disk.

At the high end, the 6200 Series consists of the 6210 and 6212 which are both object- and source-code compatible with the 6100 Series. The 6210 is intended for mechanical engineering design and analysis, printed circuit board design and custom/semi-custom VLSI design. More powerful than the 6210, the 6212 is a pre-

configured version of the 6210. This top of the line system is intended for concurrently executing interactive tasks such as schematic capture and computationally-intensive jobs such as circuit simulation. Since the system uses dual 32-bit processors, schematic editing and simulation can run simultaneously on separate CPUs and on separate windows of the display screen. (The 6210 can be upgraded to the 6212).

For users presently using the Tektronix 4000 Series terminals, the 6000 family was designed to support the 4010, 4100, 4110 and 4115B terminals.

One possible drawback of the new line is that electrical engineering (EE) application software will not be available from Tektronix until mid-1985. With the 1983 purchase of VR Information Systems, (an Austin, TX-based developer of gate array and printed circuit board layout software), Tektronix will undoubtedly offer a wide range of EE software. Tektronix claims that most UNIX-based application programs will run on the 6000 Series; however, this will only be verified by actually porting existing CAD/CAE programs.

For users needing mechanical engineering application software, several vendors including General Electric CAE International Inc., Manufacturing and Consulting Services Inc., MacNeal-Schwendler Corp., PDA Engineering, Precision Visuals Inc. and Swanson Analysis Systems have announced intent to port software programs to the 6000 Family.

Preliminary price ranges for the 6000: Family Model 6100 — \$5,000; Model 6120 — \$12,000 to \$13,000; Model 6130 — \$17,000 to \$19,000; Model 6210 with color display — \$38,500; Model 6212 — \$53,500 to \$58,500.

— Collett  
Write 230

(Figure 1 continued)

TEKTRONIX 6000 FAMILY SOFTWARE SUMMARY					
	6110	6120	6130	6210	6212
<b>Operating Systems Standard</b>	RTOS	BASIC Based on UNIX (subset)	Based on UNIX	Based on UNIX	Based on UNIX
<b>Optional</b>		Based on UNIX (full) PC Co-Proc. Support	PC Co-Proc. Support		
<b>Languages Standard</b>		proposed ANSI BASIC	proposed ANSI BASIC	proposed ANSI BASIC	proposed ANSI BASIC
<b>Optional</b>		enhanced FORTRAN 77 C Pascal	C Pascal enhanced FORTRAN 77	C Pascal enhanced FORTRAN 77	C Pascal enhanced FORTRAN 77

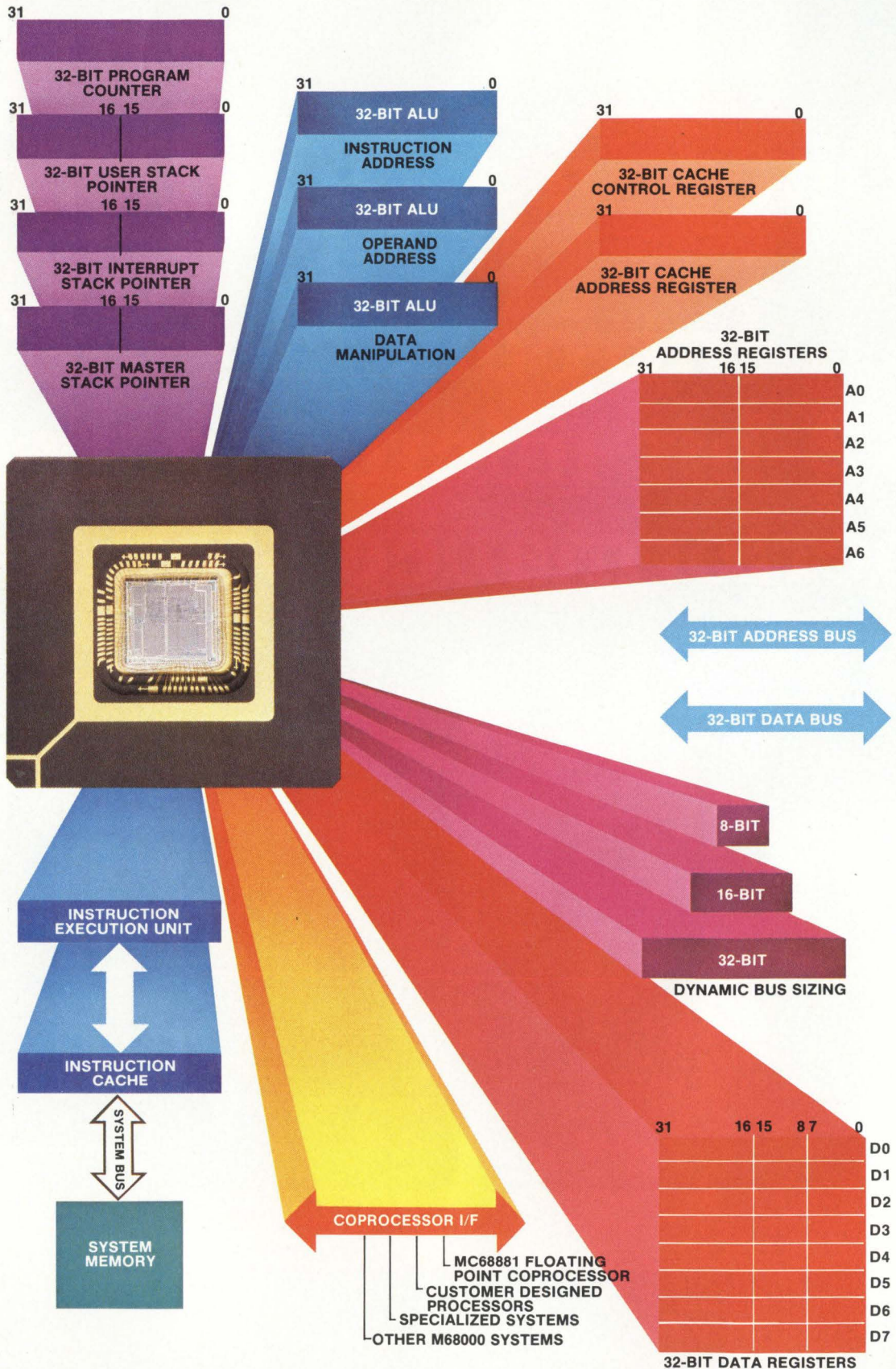


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Motorola's new MC68020 performs at speeds typically 400% of the established standard of comparison, the MC68000. It's up to ten times faster in dedicated 32-bit applications.

No other 32-bit MPU makes this extensive a leap in performance improvement. At 16.67 MHz the MC68020 typically runs at 2.5 MIPS for integer processing. MIPS rates several times typical are achievable in dedicated 32-bit applications.

The advanced two-micron HCMOS manufacturing technology which allows this unparalleled performance also results in very low power dissipation. In fact, the MC68020 consumes less power in a system than the original MC68000.

The MC68020 creates opportunities you've never had before—opportunities to unleash the full potential in your 32-bit MPU-based systems because it sets the standard for 32-bit microprocessors. And, because it's the first complete 32-bit microprocessor available, more than just a 16-bit design on a data bus stretched to 32 bits. A detailed look at the architecture reveals this totality.

## A fully compatible M68000 Family member.

Yes, the MC68020 has features new to the M68000 Family to maximize its true 32-bit capabilities.

Yes, it's an all new design built with advanced, highly manufacturable HCMOS technology.

And, yes, it's a fully-compatible member of the M68000 Family of MPUs and peripherals. All user object code written for previous M68000 Family MPUs executes without revision. In fact, MC68020 enhancements allow it to run more than three times faster.

Family compatibility is further enhanced by dynamic bus sizing, which supports the use of 8-, 16- and 32-bit ports in 68020-based systems. In fact, the MC68020 can be used in existing 8- or 16-bit systems.

## New features enhance 32-bit architecture.

The MC68020 design is new, however its architecture is based on the proven M68000 Family 32-bit register set. And, the MC68020 is highly enhanced.

On-board instruction cache speeds operation and provides increased multiprocessing efficiency. The coprocessor interface allows direct expansion of the architecture off the MC68020 chip to coprocessors or customer-specified processing systems.

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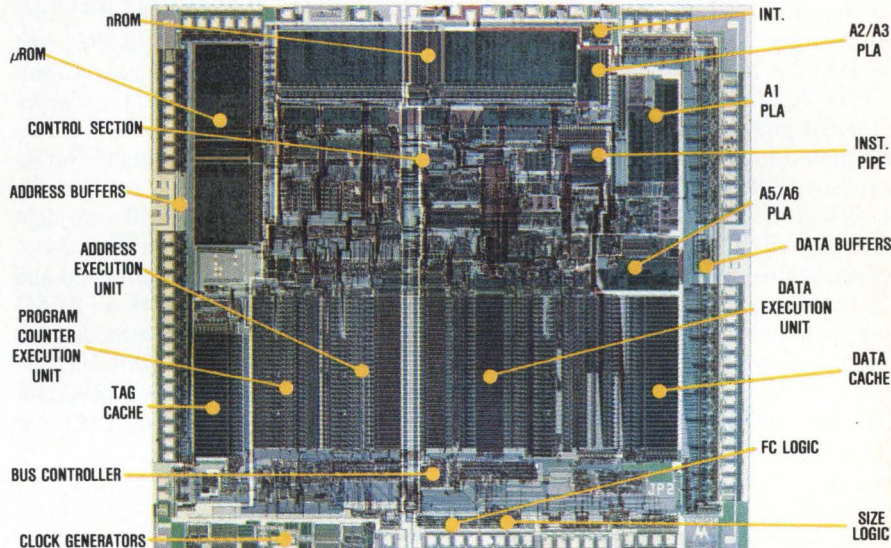
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# New Company Debuts Eight Graphics Workstations

Demand for networked 32-bit graphics workstations for technical applications is so great that Apollo's business is soaring, Tektronix is jumping in, and there is still room for more, at least, Mosaic Technologies (Billerica, MA) hopes so. The company, founded a year and a half ago, brought out a line of eight graphics workstations based on the NSC32032 CPU and the AM29116 bit-slice processor.

The Shared Vision System (SVS) workstations are based on UNIX, C and Core graphics standards, with Multibus and Ethernet interface slots. Fast response time was a main design goal. The full NSC32000 chip set with MMU and floating point co-processor, 16 Kbytes of cache, ECC RAM, and the microcoded bit-slice processor are connected on the proprietary 32-bit System Memory Interconnect (SMI). A "dual rail" bus at 48 Mbytes/sec aggregate bandwidth separates write from read operations (**Figure 1**) for good throughput.

Like Apollo, Mosaic plans to offer hardware and general software to OEMs and high volume end-users. Application software development should be eased by the object-oriented software. At the core of the Mosaix UNIX-based OS is a File System. Surrounding this are layered an Object Storage Manager, and then utilities, including window manager, menu, graphics primitives and an image composition library. Over this, applications and screen management can access either the utilities or the Object Storage Manager directly.

The power of a 32-bit single-user computer provides not only design functions, but also general purpose computing. According to Mosaic and others, only about 30% of a designer's time is spent on design creation; 30% is devoted to detail and documentation and another 30% is spent in communication. Ethernet provides for sharing of a designer's vision and communication, hence the name Shared Vision Systems.

Two series were announced: the SVS100s are desktop systems without Multibus expansion slots and a maximum of 4 Mbytes of error-corrected ECC RAM: 200 series are deskside, with ECC RAM expandable to 8 Mbytes and up to four 85-Mbyte disk drives, as well as



three Multibus slots. All of the workstations include a 1 Mbyte floppy, 45 Mbyte streamer tape, keyboard, 2 RS-232 ports, an Ethernet interface and Mosaix, C, emulation, screen manager and file transfer software.

Displays are all high-resolution 60 Hz non-interlaced, with four monitors for either series. The 110 and 210 use a 1024 x 800 15" B/W monitor; a 19" 1024 x 1280 pixel screen comes with 120 and 220 models. Color monitors are 19" 512 x 640, with four bits/pixel in models 150 and 250 and eight bits/pixel in the 152 and 252. List prices range from \$25,900 for the SVS110 to \$42,900 for the 252 color

system with room for expansion.

First official showings were at Siggraph, but at this writing, only a canned demo was available. The speed and resolution of the B/W system were impressive. Systems are to be commercially available in October. Mosaic plans introductions every three to six months, and likely announcements would be higher resolution color, more network functions for resource-sharing and transparency, added processors, data management facilities and GKS-compatibility.

—Pingry  
Write 232

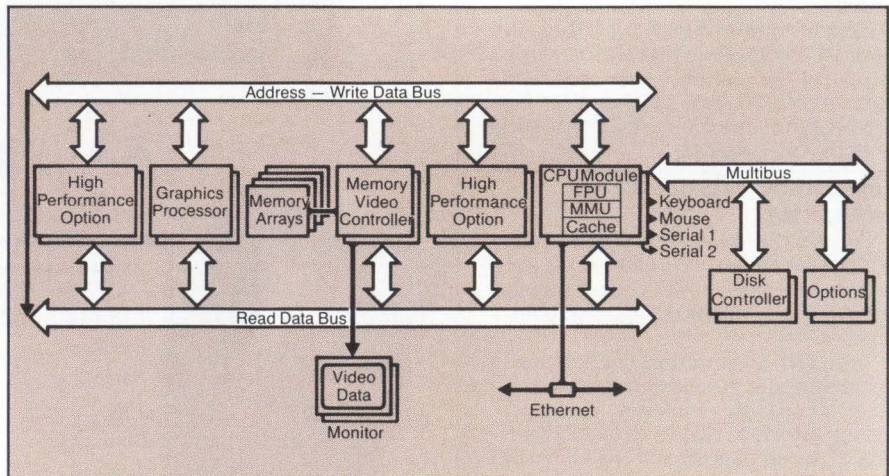


Figure 1: The hardware architecture of Mosaic's Shared Vision System workstations uses write and read buses for improved throughput on the 32-bit system.



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## Controllers Combine Disk And Tape Interfacing With Full Emulation

The recent introduction of six controllers manufactured by Spectra Logic Corp. (Sunnyvale, CA) at this year's National Computer Conference are in keeping with the company's history of product development. Spectra Logic has focused on emulating single and multifunction controllers for the Digital Equipment, Data General, Texas Instruments and Perkin-Elmer markets. A feature of their products has been the combination of disk and tape interfacing with full emulation on one printed circuit board.

The new single-board computers are targeted at three controller markets: Data General (Spectra 17, Spectra 27), Texas Instruments (Spectra 116, Spectra 126) and Digital Equipment Corp. (Spectra 111, Spectra 121).

For DG users, the Spectra 17 is a disk/tape controller for use with the Eclipse and MV series computers. It emulates both the DG 616X series of controllers (when using 80 or 160 Mbyte drives) and the 606X series disk and 6021 and 6125 subsystems.

The controllers cable to disk and tape from the system backplane via the chassis bulkhead. One consideration in this arrangement was that the controller had to be compatibility "hardened" with the chassis, or protected from electromagnetic interference.

The board utilizes a 16-bit 29116 microprocessor which controls the CPU, disk and tape interfaces. To bring data transfer rates to the level of the interfaces, the board has separate buffering for disk and tape, eliminating the problem of errors stemming from late data. Drive mixing and mapping configurations are located in PROM. The Spectra 27 interfaces any combination of four SMD-type disks to the burst multiplexer channel or data channel and eight 1/2" tape drives, including GCR, to the data channel. Transfer rates of 2 Mbytes/sec for disk and 750 Kbyte/sec for tape are supported. A companion model, the Spectra 17, is a single-function disk controller which has all the same hardware as the Spectra 27 related to disk.

For the Texas Instruments 990 and BS 600/800 computer series, Spectra Logic introduced the TILINE compatible Spectra 126. This disk/tape controller emulates TI's CD1400, DS80/300 and WDMT disk and

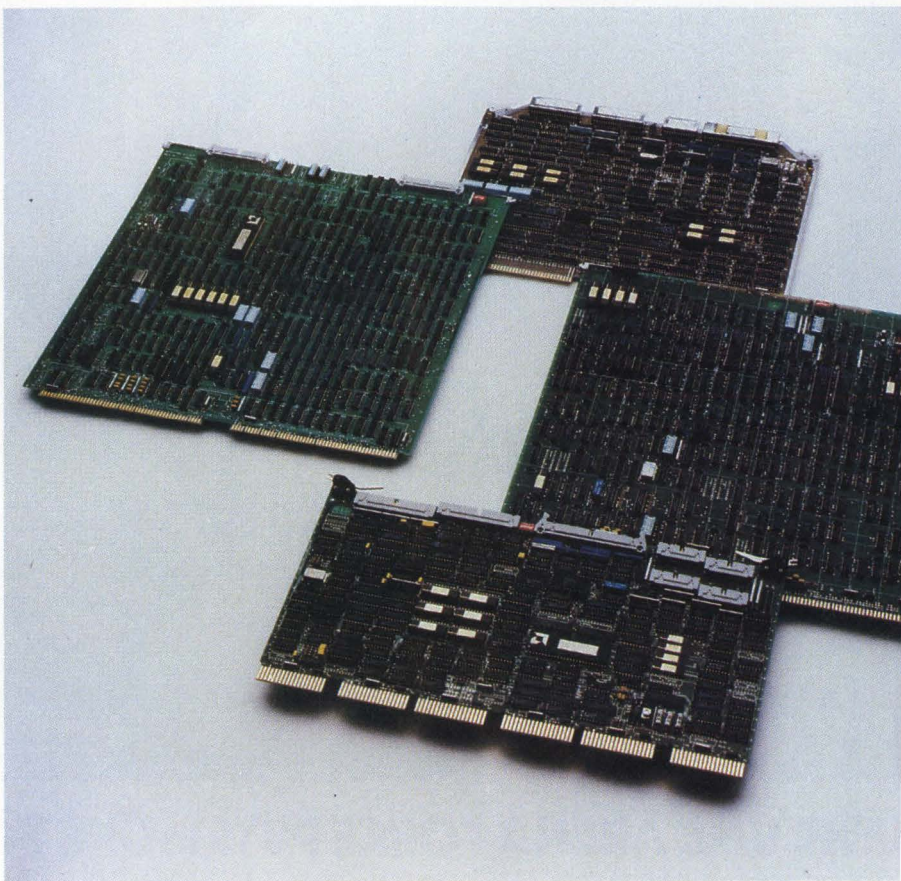


Figure 1: Spectra Logic Corp.'s new single-board, multifunction disk/tape controllers: (clockwise) the Spectra 126, Spectra 120, Spectra 121, and Spectra 27.

979 tape subsystems. Like the DG controller, it supports direct attachment of shielded flat cables to meet FCC requirements for EMI emissions.

The board is similar to the Spectra 27 except for the use of a bipolar microprocessor and that it interfaces to two SMD-type disks and four 1/2" tape drives. It also supports transfer rates of 800 Kbytes/sec tape. A single function model, the Spectra 116 is also available.

The Unibus compatible Spectra 121, which follows the introduction of a Q-bus compatible controller, can be used with DEC's PDP-II and VAX computers. Because the DEC controller market is highly competitive, Spectra Logic is introducing products in each segment of that market, such as Unibus and Q-bus, as they

have done with Data General and Texas Instruments.

The Spectra 121 interfaces combinations of both four SMD-type disks and four 1/2" tape drives. Transfer rates are comparable to the other introductions.

Users can program the on-board EEPROM with menu driven software without removing the controller from the system, facilitating drive mixing and mapping. The Spectra 111 is a single function disk controller with the same features as the 121.

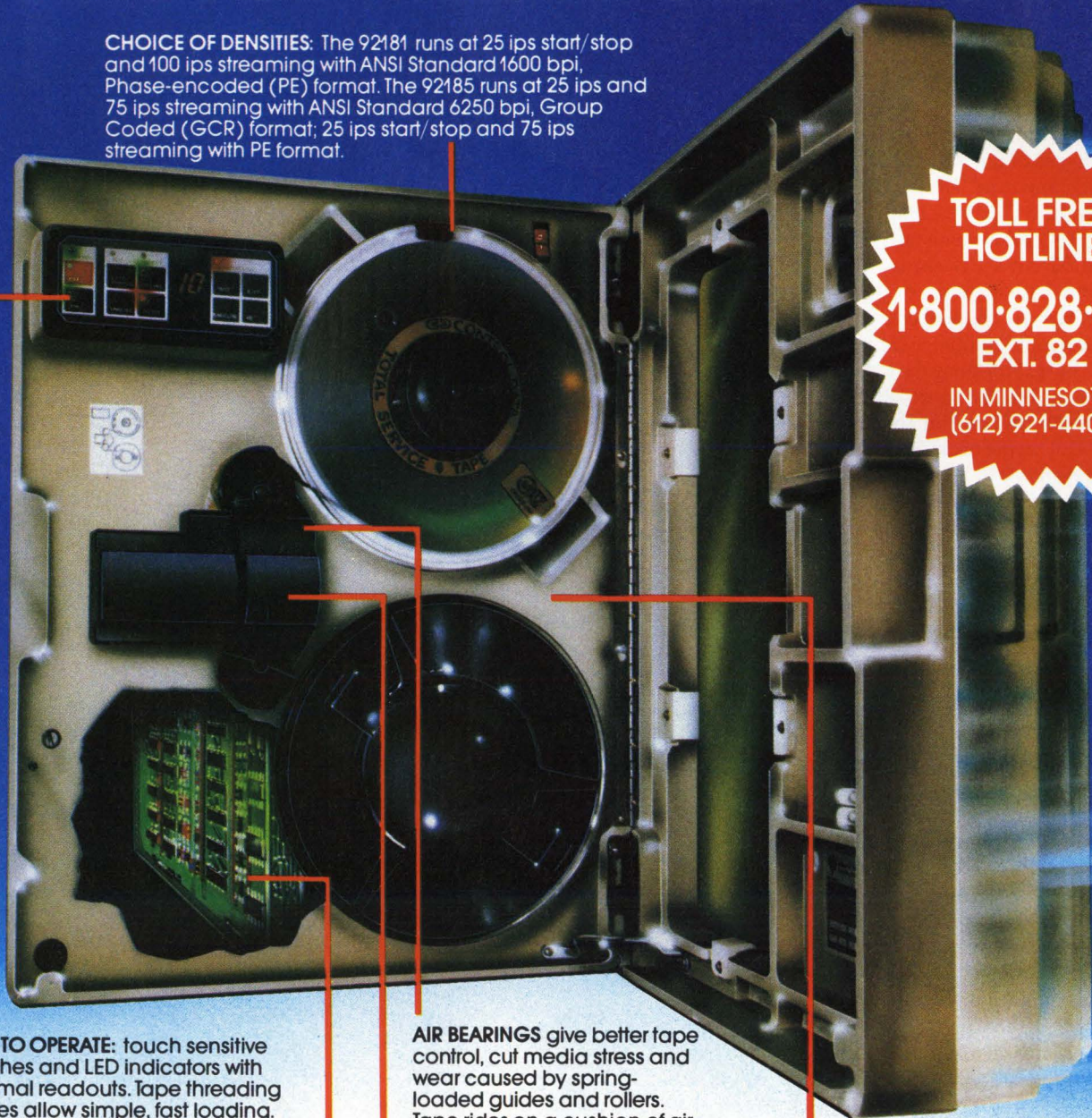
All of the recently introduced controllers allow users to attach removable pack or Winchester SMD drives. The six single board computers add to the company's line of 13 board products.

— Coville  
Write 236



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## Multiple CPU System Provides Concurrency For Real Time Computing

One new system based on the National Semiconductor 32032 goes beyond the improvements of full 32-bit processing to true multicomputing. The Flex/32 Multicomputer from Flexible Computer Corp. (Dallas, TX) allows concurrent use of multiple 32-bit CPU cards, memory cards and I/O systems in a shared-memory, tightly-coupled environment.

Within a multicomputer cabinet, two common buses run along the top of three sets of 10-card racks; vertically, 10 local buses run between the three levels (**Figure 1**). Out the back, VME connections are available to a peripheral control cabinet for I/O based on the Eurocard standard. Memory, processor and I/O building blocks can be combined in an erector set fashion.

Local to common bus interface through common access cards and a common control card allows memory sharing in the multicomputer cabinet. Each common access card contains 128K of common memory as well as interprocessor synchronization circuitry and connects one local bus to the common buses. One common control card is needed per multicomputer cabinet. This card acts as a common access card and also provides the arbitration hardware for common bus access.

The lower two levels of the cabinet may contain CPU or memory modules mixed in any configuration. If concurrency is more critical than memory, up to 20 CPUs can share the 10 buses and use on-board memory as well as the common memory. Flex/32 CPU cards have 1 Mbyte of RAM and 128 Kbytes EPROM, as well as 8-byte instruction cache and 32-page table cache. At the other extreme, one CPU could operate with 19 memory modules. This single-processor machine would need no common access or control cards, with no need for common bus arbitration.

Memory cards come in two configurations. Standard memory cards of 1, 2, 4, or 8 Mbytes, have 150 nsec access times, with double error detection and single error correction. Bus error checking can be either single error correction and double error detection or byte parity on both data and address. High performance 128K to 2 Mbyte memory boards provide 35 nsec

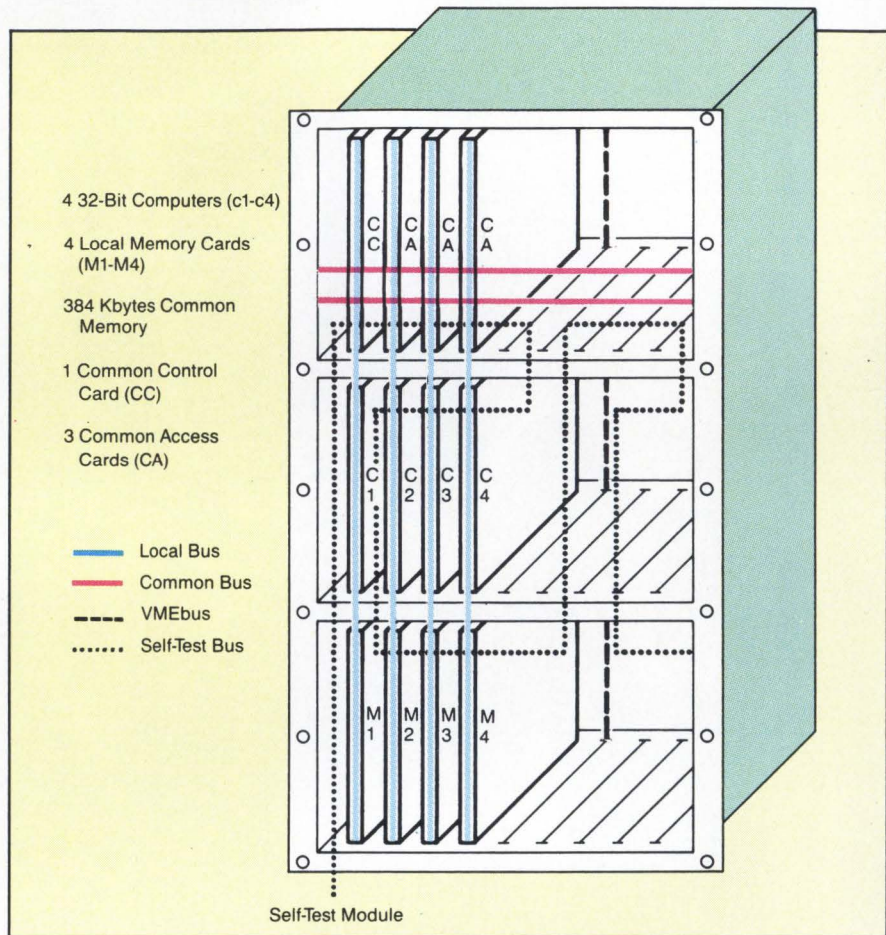


Figure 1: Four Flex/32 computers in a multicomputer cabinet; each local bus connects the CPU to a memory card and common access or control card.

access time.

For each of the 10 local buses in a cabinet there is a separate VMEbus out the back for outside communication. An I/O interface is implemented through VME boards in peripheral control cabinets (**Figure 2**). These cabinets have 10 VME buses with up to nine cards each on double Eurocard standard backplane/card cage, and can be bolted on to multicomputer cabinets. The VMEbus was a logical choice for peripheral control and I/O, as one of the only standard buses that currently supports 32-bit processors.

Software for this multiple processor architecture also consists of building blocks. Common variable modules declare variables common to all software

processes; language modules are written in Fortran 77 (with ISA extensions for real time operation), C, Ratfor or assembly language; concurrent modules are written in ConCurrent C; library modules and interprocessor messaging modules round out the system.

Flex/32 systems use two operating systems: UNIX V for universal software development and ConCurrent C for developing real time concurrent object modules. If a software house decides to support it, Flexible will likely add Ada. Flexible's multicomputing multitasking support utilities, in conjunction with ConCurrent C, helps develop run time real time executive programs.

Redundancy is possible by configuring two common control cards and using



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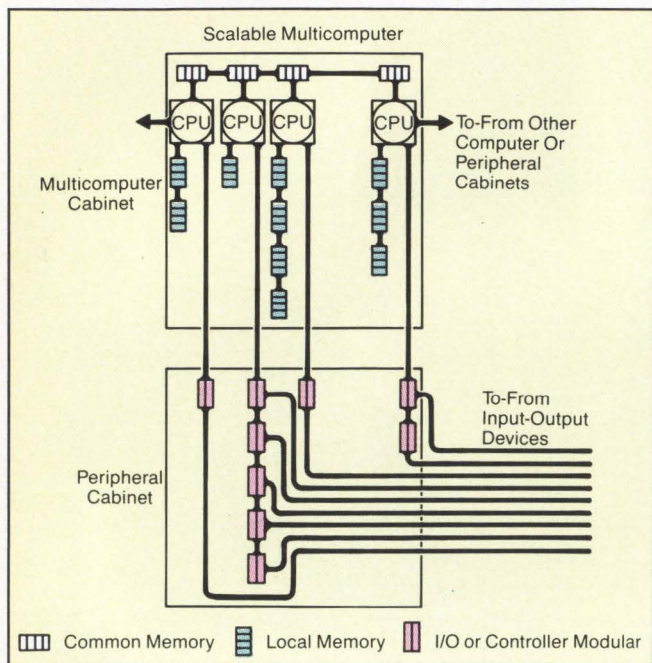


Figure 2: VMEbus-based peripheral control cabinets hook to multicomputer cabinets via VMEbus.

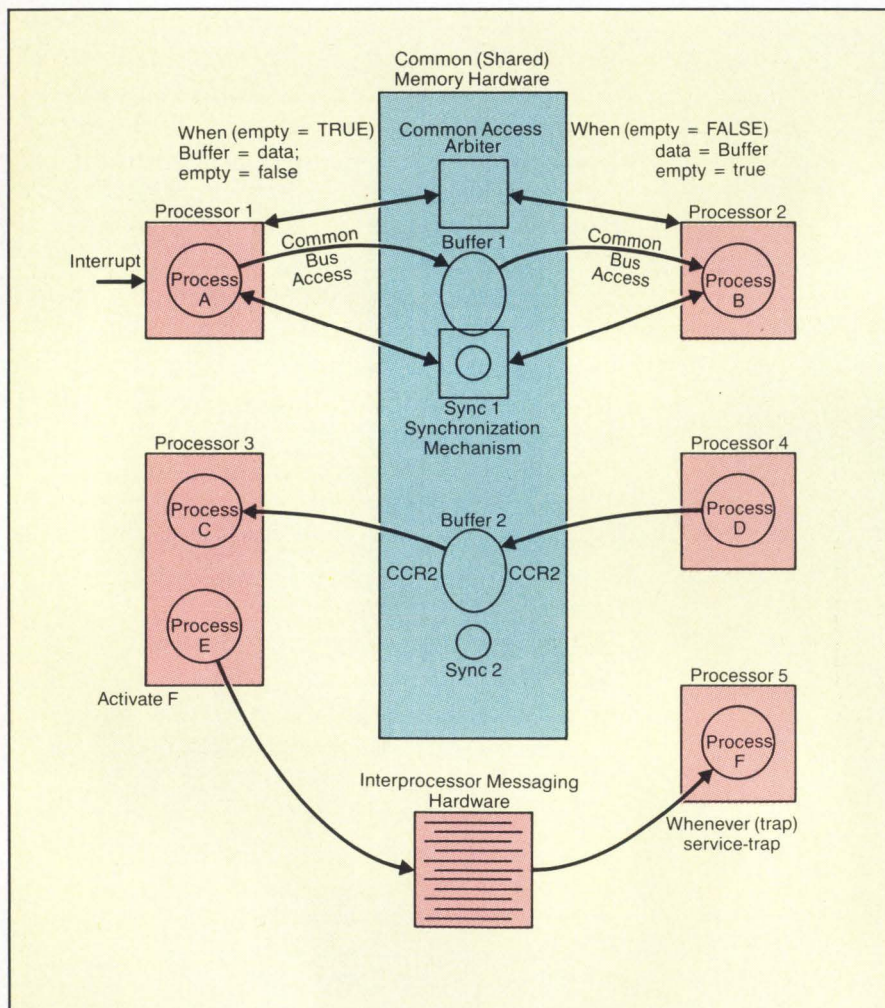


Figure 3: For concurrent use of multiple CPUs, Flexible offers two main types of interprocessor communications: interprocessor messaging and Conditional Critical Region Communications (CCRC).

CPU modules redundantly rather than concurrently on processes. A continuous self-test system built into each card adds further fault tolerance. Dual redundant buses (shown at the bottom in **Figure 1**) interface with the 8-bit self-test microcomputers on each board. This system can perform fault diagnosis and isolation or performance analysis of intercomputer communication.

Mechanisms for interprocessor and interprocess communications are provided with the goal of not dictating implementation. There are two prime methods of synchronized communication between processes on different computers within a multicomputer cabinet: interprocessor messaging or data sending and Conditional Critical Region Communications (CCRC), or using a shared memory mailbox.

Hardware for arbitration of the common memory for CCRC is on the common access and common control cards. In **Figure 3**, processes A, B, C and D are using CCRC with common memory buffers. A and B, by using proprietary synchronizing hardware, only go to the common bus when there is information available for them in buffer 1. They can examine the sync hardware without accessing the common bus, as C and D do using read/modify/write instructions.

Note that process E is also running on processor 3, in a multitasking environment with process C. E is communicating with F by means of interprocessor messaging hardware. In the application shown, E raises an exception in F by issuing an activate statement. Process F responds to the exception with the service trap routine.

The combination of hardware and software building blocks in an architecture of true multiprocessing, with I/O on the international Eurocard standard, allows flexibility for expansion or reconfiguration. Concurrent C software and multiple 32-bit processors make possible real time computing for large and I/O intensive applications.

Flex/32 is a directly programmable multiple instruction stream/multiple data stream computer. CPU cards with 100 nsec cycle time, 4 Gbytes addressing, cache RAM and EPROM, demand paged memory management and floating point processor can communicate three ways with their local bus connections to common bus and memory. Though the boxes are general purpose, initial market thrust is to industrial and government markets, as well as specialized scientific applications.

— Pingry  
Write 233



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## Dedicated Stand-Alone System Is First For Analog Circuit Design

Until recently, there were no stand-alone workstations dedicated specifically to analog circuit design. The Analog Workbench, introduced by Analog Design Tools, Inc. (Menlo Park, CA) is a micro-computer-based workstation developed solely for analog circuit design, providing on-screen simulation of circuits and test instrumentation.

Previously, software packages for analog design have been available which run on mainframe computers, but stand-alone workstations have proven ineffective for the analog designer because of the differences between the design tasks of digital and analog circuitry.

The function of a digital circuit workstation is to create and verify a complex roadmap of thousands of circuit elements. Conversely, an advanced analog circuit may have as few as 30 elements, each of these requiring detailed characterization. For example, 42 parameters must be examined for a single transistor. Whereas a digital workstation simulates one test instrument, a logic analyzer, analog engineers need additional equipment such as oscilloscopes, function generators, frequency sweepers and DC multimeters.

The Analog Workbench simulates all schematics, devices, test instruments and calculations of analog circuit design, eliminating the man hours of assembling breadboard prototypes at a workbench. Hardware for the system is Sun Microsystems, Inc. (Mountain View, CA) Model 2/120 which is based on a 32-bit MC68010 microprocessor. The system runs on UNIX, has a 50 Mbyte 5 1/4" Winchester disk drive, 20 Mbyte 1/4" streaming tape drive, monochrome video display, detachable keyboard and optical mouse.

The Analog Workbench uses a menu-driven software scheme which follows the logical flow of the analog design process. For example, selecting "transistor" on the circuit element menu displays all the specific transistors available for use in that circuit. The mouse is used for menu selection except in cases where circuit names or a definition of element values is required. In these cases the user types numeric values or text on the keyboard.

Once selected, circuit elements appear in a circuit window, a blank space on the

Figure 1: An example of on-screen analog circuit simulation.

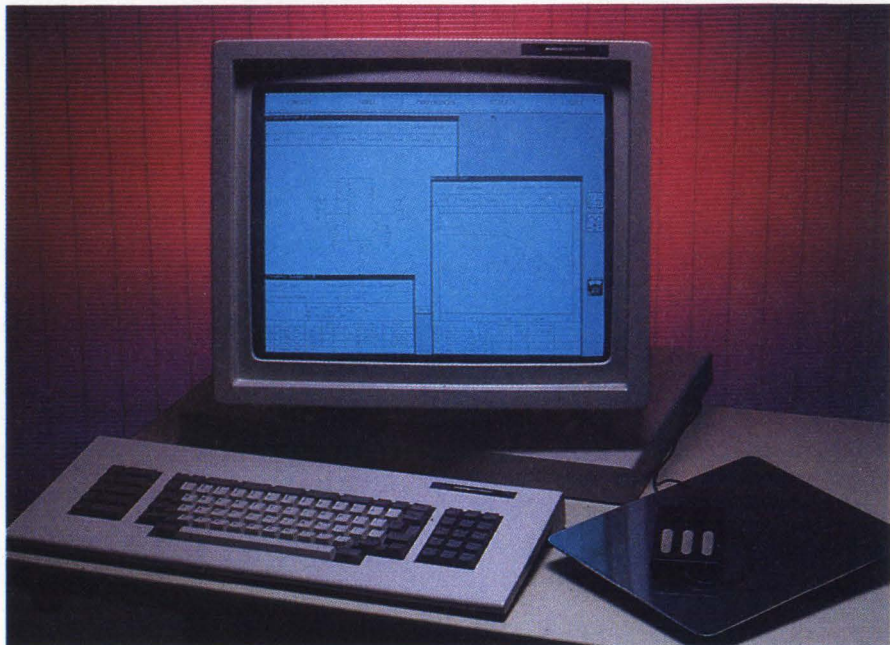
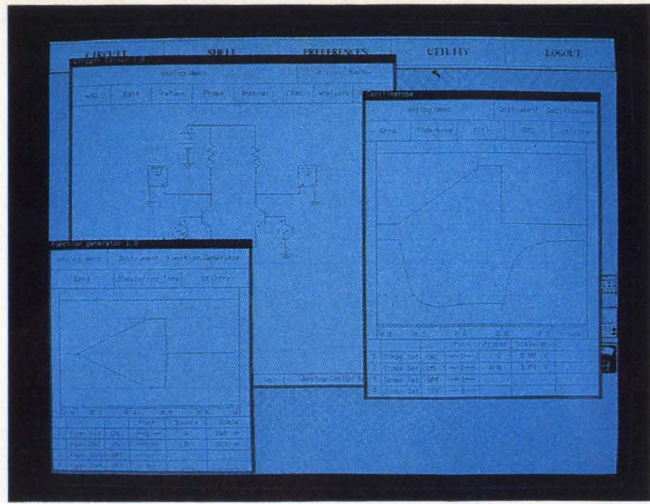


Figure 2: The Analog Workbench is a turnkey stand-alone workstation based on the 32-bit model 2/120 from Sun Microsystems.

screen where the circuit is constructed. The mouse moves elements within this window, flipping or connecting them with other lines.

Three test setups are provided: a time domain setup with generator and oscilloscope; a frequency domain setup with sweeper and network analyzer; and a DC set up which includes a DC multimeter. Probes are then placed on completed circuit designs to connect test instruments, all simulated in software.

After the circuit is drawn and tested, the results are displayed on another window on the screen. The multiwindow display contains one million pixels organized in 900 rows of 1152 columns. The display contains a dedicated processor for raster operations and has 128 Kbytes

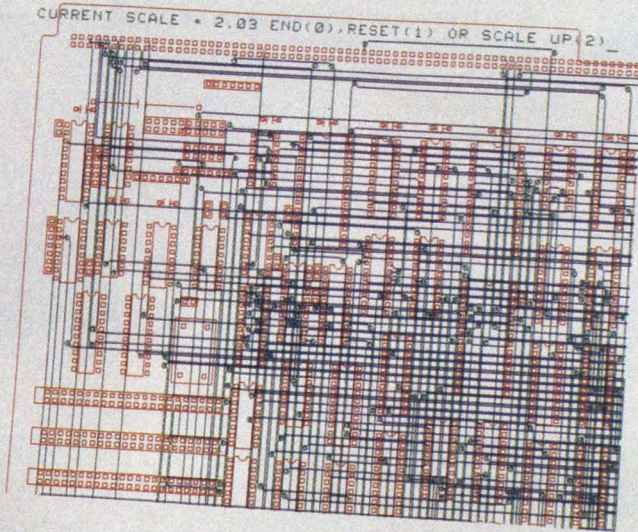
of dual ported frame buffer memory.

The Analog Workbench comes with several circuit libraries, which contain models of bipolar transistors, JFETs, MOSFETs and diodes. Other software includes an editing program for drawing and modifying schematics, simulation programs which emulate test instruments operation, a window manager and a C language compiler.

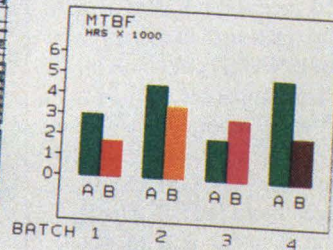
Because the system is UNIX-based, a variety of software from third party vendors is available. The system sells for \$74,800 and includes all workstation hardware and software. An Ethernet interface is optional. Deliveries begin in October.

—Coville  
Write 237





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## Oki Semiconductor Enters Commercial Gate Array Market

Add one more vendor to the growing number of semi-custom IC manufacturers. Oki Semiconductor (Sunnyvale, CA), a subsidiary of Oki Electric Industry Co., Ltd., is known for its achievements in memory, CMOS microprocessors and speech synthesis. They recently introduced family of CMOS gate arrays that range from 380 to 4205 gates.

Oki's MSM60000 and MSM70000 CMOS array series' are three-micron, silicon-gate, dual-layer metal. The firm claims typical propagation delays of three nsecs for two-input NAND gates and inputs and outputs are compatible with TTL and CMOS. Both series reportedly handle voltages from 3V to 6V and operate in a temperature range from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . Available packages include DIP, plastic flat pack, pin grid array and plastic leaded chip carriers.

Oki's functional library includes 77 basic logic blocks and 38 macrocells. After design, masking, prototyping and volume fabrication takes place in Japan where the silicon foundry is located.

According to Ray Houghton, Product Marketing Manager, Oki is manufacturing packages with up to 132 pins, with

Development Commitment of OKI CMOS Gate Array Family					
DESIGN RULES	LINE-UP	1984	1985	1986	1987
3 $\mu\text{m}$	300 GATES	IN PRODUCTION			
	700 GATES	IN PRODUCTION			
	1400 GATES	IN PRODUCTION			
	2000 GATES	IN PRODUCTION			
	4000 GATES	IN PRODUCTION			
	<ul style="list-style-type: none"> <li>- Schmitt Trigger Input</li> <li>- Crystal Oscillator</li> <li>- Pull Up/Down</li> </ul>	SHRINK	D&E	PRODUCT	
2 $\mu\text{m}$	10000 GATES	D&E IN PRODUCTION			
	FAMILY EXTENSION	DESIGN & EVAL.		PRODUCT	
	6000 Gates				
	8000 Gates				
	20000 Gates	DESIGN & EVAL.		PRODUCT	
	- Include Memory/PLA				

280 pin packages currently under development. Oki is also developing two-micron CMOS gate arrays with two nsec propagation delays that will be available later this year.

Concurrent with the introduction of

these high speed arrays will be the opening of design centers in Los Angeles, Dallas, Boston, Minnesota and Poughkeepsie, New York.

— Collett  
Write 231

## New Family Of GaAs ICs

A full family of ultra-high speed, ultra-high frequency GaAs semiconductors, developed by GigaBit Logic (Newbury Park, CA), is targeted for use in products already in the marketplace. GaAs' promises of performance advantages and speed increases by a factor of ten have caught the interest of OEMs and end-users alike.

GigaBit's ICs are based on their patent-pending Capacitor Diode FET Logic (CDFL) circuitry and are manufactured using the company's proprietary FastFet process, a planar technology similar to Si VLSI. In GigaBit's process, no isolation channels are required due to the isolation provided by the semi-insulating GaAs substrate. Multiple localized implants define active device regions. Ion implementation is used exclusively for the introduction of dopants as opposed to high tem-

perature diffusion. One micron widths are obtained by using direct-step-on-wafer photolithography.

Twelve new products in GigaBit's PicoLogic family of their FastGaAs Series were recently introduced, including ultra-high speed logic ICs, counters/prescalers, and diode and transistor arrays.

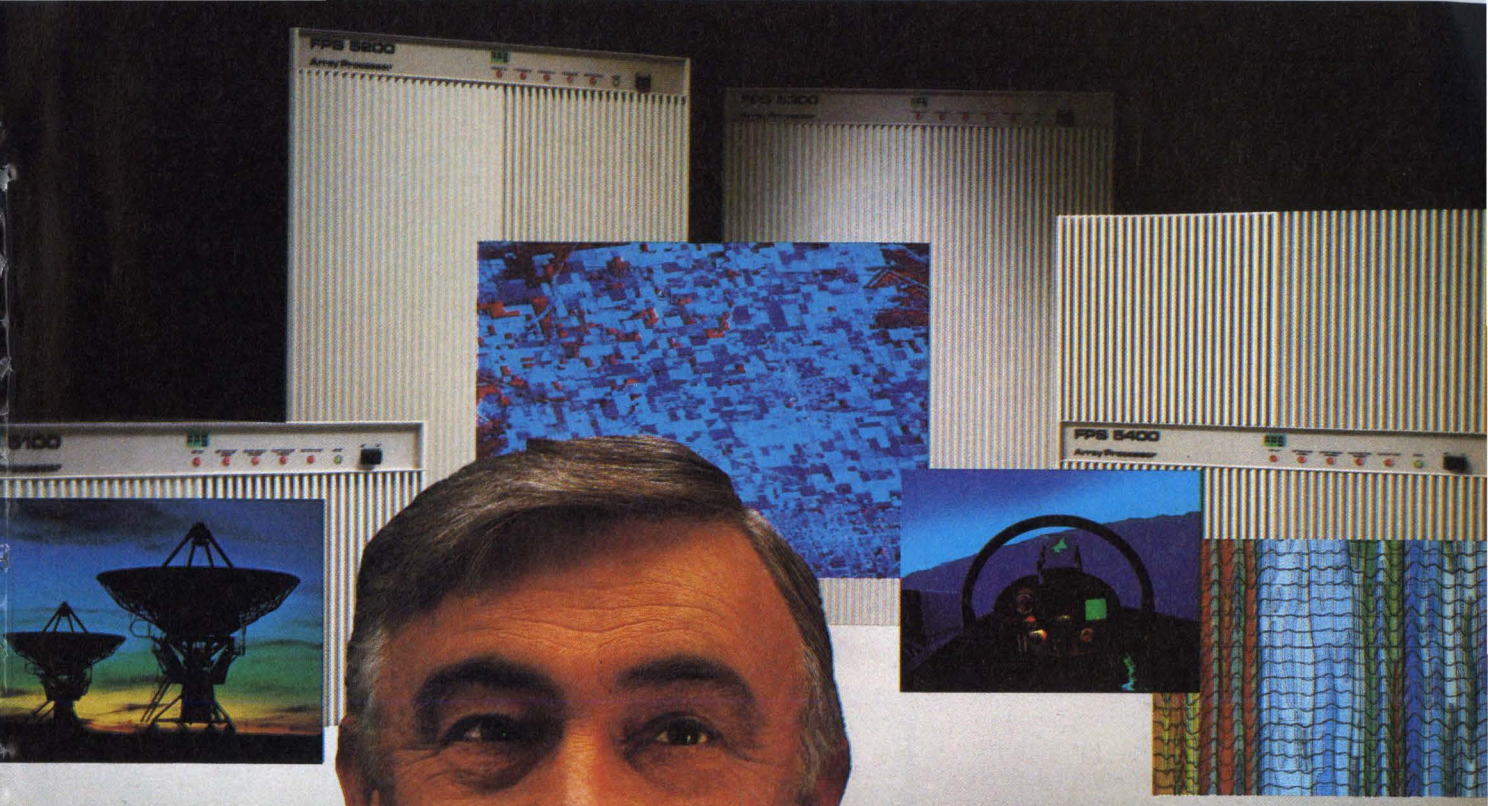
The ultra-high speed logic product line consists of the 10G000, a 75 picosecond Quad three input NOR gate; the 10G011 dual one to four fanout buffer; the 10G021 dual precision D flip-flop; and the 10G012 comparator/complementary driver. Ultra-high frequency ICs in the counter/prescaler line include a 3 GHz two-stage ripple counter, a seven-stage ripple counter with clear, a 4 GHz seven-stage ripple counter, and a variable modulus prescaler. Rounding out the present PicoLogic family are two diode arrays, a

single gate FET array and a dual gate FET array. To aid the user in evaluating GigaBit's new ICs, the company is also providing an evaluation board.

All 12 products are available in dice form, in hermetically sealed leadless chip carriers, or in hermetically sealed flat packages. The 10G models all provide ECL compatibility so they can immediately be used in products presently employing ECL. The 11G566 4 GHz seven-stage ripple counter provides TTL/CMOS interface capability as well.

The ECL compatible inputs and outputs facilitate using the 10G000 input NOR gate in existing high performance systems for improved throughput, reduced signal skew and increased timing margin. The 10G000 can also be driven from and driven to TTL and CMOS gates, providing high speed TTL/CMOS-





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5200	—	5205	—	5210	—	—	—
5300	—	—	—	5310	—	5320	—
5400	—	—	5410	—	5420	—	5430
5500	—	5505	—	5510	—	—	—
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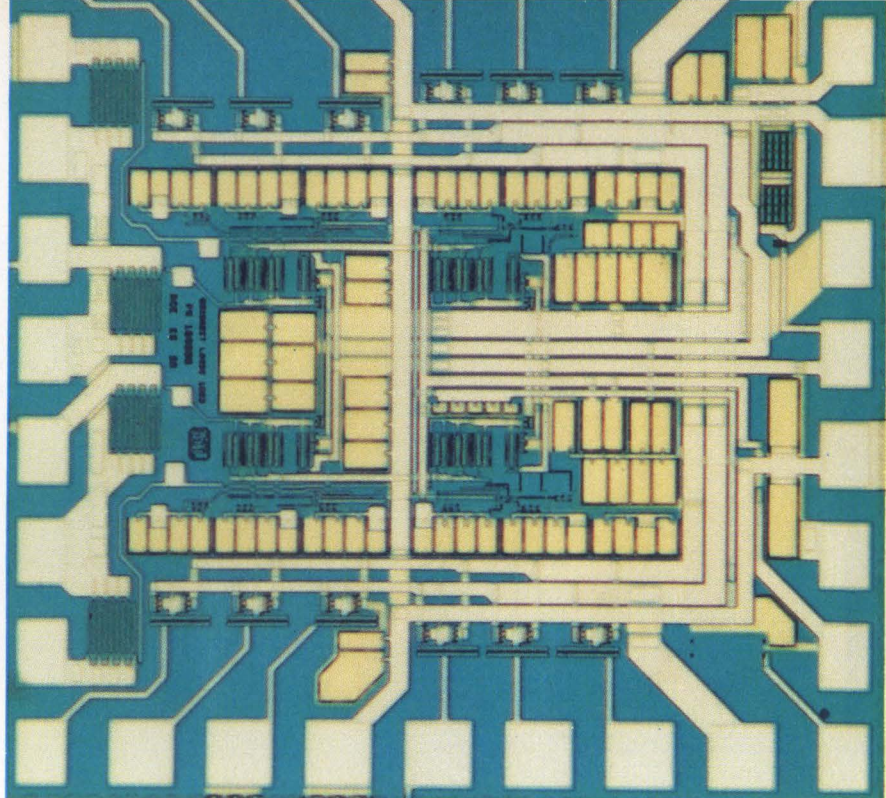


to-10G/ECL and ECL/10G-to-TTL/CMOS translation capability.

Typical applications for the fanout buffer include data buffering and clock distribution. Because the 10G011 is a dual buffer, both true and complementary clock signals can be buffered by one chip, minimizing skew differences between the two clock phase.

The line of ICs cover applications such as high-speed switching circuits, waveform clamps, high frequency mixers or input protection devices. The 16G010 and G011 are Schottky barrier diode arrays consisting of 14 individual diodes plus a full wave rectifier. Both feature low junction capacitance and low series resistance. The G020 contains 11 single gate GaAs depletion MESFETs on a single chip. One pair of MESFETs has a common source for use as a differential pair. The MESFETs are ideal for high frequency applications utilizing relatively small signal levels, in both digital and analog circuits. Eight dual gate GaAs depletion MESFETs are contained on the G021 chip, providing for applications using relatively small signal levels in both digital and analog circuits.

Immediate markets for GigaBit's products include OEM manufacturers of computers that process data at hundreds of



GigaBit Logic 10G000 75 picosecond quad three input NOR gates.

MIPS, fiber optic communication systems that will accommodate as many as 30,000 individual telephone conversations on a single fiber optic pair, instru-

mentation operating in the GHz range, as well as military/aerospace systems.

— Hanrahan  
Write 239

## DEPARTMENTS/Backplane

### Exercising Packaging Options For Electronic Circuits

Connector options can affect the cost, efficiency, flexibility and maintenance difficulties of computer systems. Bus configurations affect packaging options and conversely, packaging decisions may affect the efficiency of the bus.

When selecting a packaging scheme, the most essential consideration is cost. Bus length is also important, since too long a path may produce unacceptable signal delays or distortion, especially as speeds increase. Bus parameters and packaging methods affect adaptability and expandability of a system, as well. The designer may choose either a backplane or a stacking bus structure. Three connector types are available: card edge, two piece, and zero insertion force (ZIF).

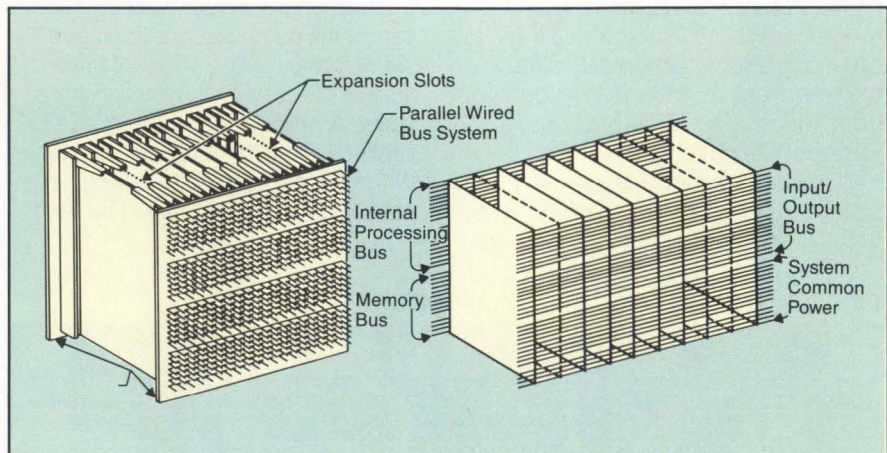


Figure 1: Split backplanes are used for large numbers of lines; ZIF connectors act as both connectors and card guides.



# The lean, mean plotting machine from Houston Instrument

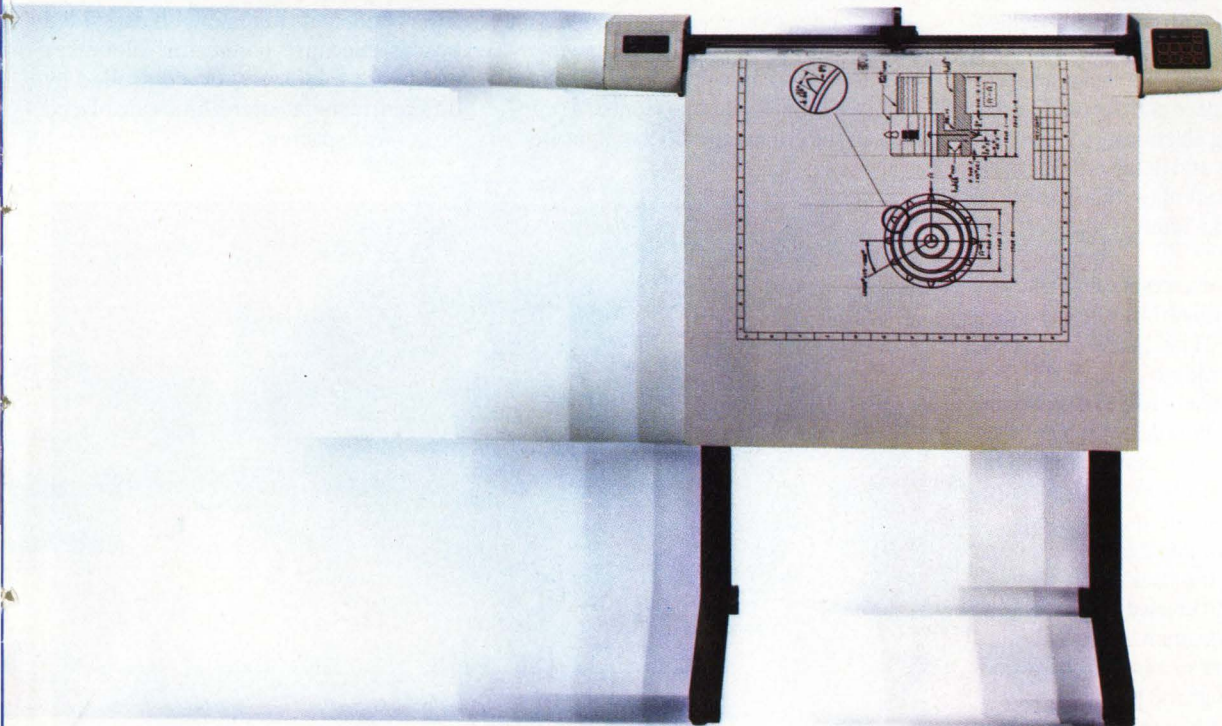
Houston Instrument's brand new servo driven DMP-51 is the fastest drum plotter we've designed to date. This superb plotter offers a pen speed of up to 22 inches/second; programmable accelerations, and a pen-on-paper resolution of 1/1000 of an inch! That means you'll turn out quality 17" x 22" and 22" x 34" drawings a lot faster, increasing your firm's productivity and profitability.

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Write 36 on Reader Inquiry Card





Standard backplane systems use a motherboard bus to provide a signal path between daughterboards. Though the one-motherboard backplane bus traditionally employs one-piece edge connectors, two-piece connectors are being selected for complex circuits.

If the number of signal lines becomes unmanageable, the split backplane bus with two motherboards (**Figure 1**) should be selected to shorten the signal path length between daughterboards. The drawback of a split backplane bus with card-edge connectors is that disassembly is required when replacing a single daughterboard. A side-entry ZIF connector eases that; contacts are camed open so that the daughterboard slides into the connector. Higher connector costs are offset by eliminating the need for card guides and other hardware.

One advantage of the backplane bus is that several standard configurations exist. It is often more cost-effective to specify a standard bus and use off-the-shelf daughterboards than design bus and boards.

Another advantage is flexibility by adding new boards, the system is configured for future needs, and repair means simply swapping boards.

However, expansion capability is limited to the size of the motherboard and the number of connectors it can hold. Unused connectors waste space and money: a 10-slot motherboard with only two daughterboards is clearly inefficient. The long signal paths in a standard backplane may slow the system speed and degrade performance. Designing electronics to overcome signal distortion and delay will increase costs. Still, the backplane bus is versatile and effective and often is the selected standard.

A stacking bus overcomes the disadvantages of the backplane bus by eliminating the motherboard. Here, boards are stacked (**Figure 2**); the tails of each connector extend through one board and plug into the connector on the board below. The bus is carried through the connectors. This scheme allows variety in the size, shape, and thicknesses of the boards used.

Expansion is available from the top and bottom boards of the stack. The minimum system contains no unused connectors and wiring, and the maximum system is limited only by the cabinet size and electrical considerations such as the power supply.

In addition, connectors can be placed anywhere on the board and a split bus is possible. Careful placement of connectors will eliminate or reduce the need for other

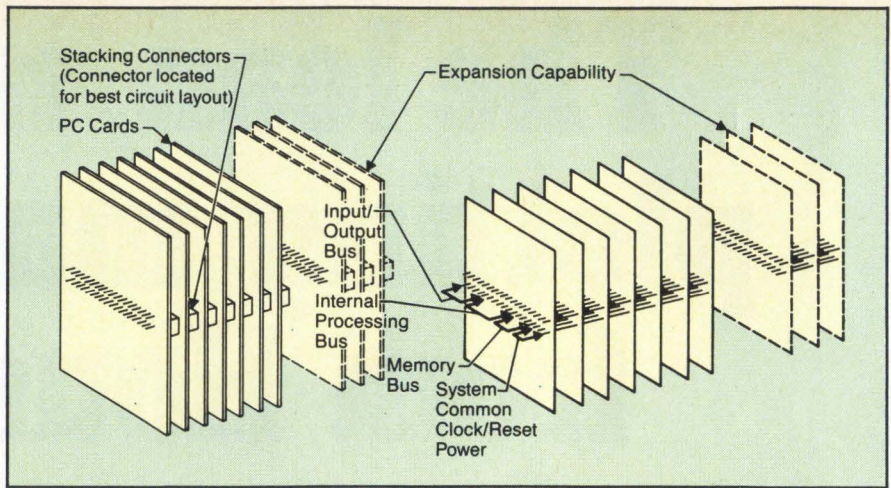


Figure 2: A stacking bus uses only needed connectors and wiring, with cabinet and electrical considerations limiting system size instead of a motherboard.

hardware to support the boards. Signals do not have to be brought to the board edge; edges are then available for special interconnection needs. Signal paths are shortened both on the board and through the connectors from board to board.

One disadvantage is that replacing boards in the middle of the stack requires some disassembly. Many stacking connectors require plated-through holes, which may add complexity. Also, since the stacking bus is less widely used, it is not standardized and off-the-shelf boards are not available.

Card-edge connectors are mounted on the motherboard; pads on the daughterboard plug into the connector. These have disadvantages for a large number of contacts in the connector. To maintain elec-

trical and mechanical continuity over a range of board tolerances, connector contacts must exert relatively strong pressure on the PC pads during mating.

A board nominally 0.062" thick typically has a tolerance range from 0.054" to 0.070". To provide sufficient force on the minimum thickness board and yet not permanently damage the thicker board, mating forces are usually between 8 and 16 oz. per contact, limiting card-edge connectors to 140 positions or less.

Card-edge connectors don't work well with warped or thick multilayer boards. These connectors are restricted to two rows of contacts to mate with two-sided boards. Because connector tolerances and board tolerances are controlled by different manufacturers, limits are placed on contact spacing.

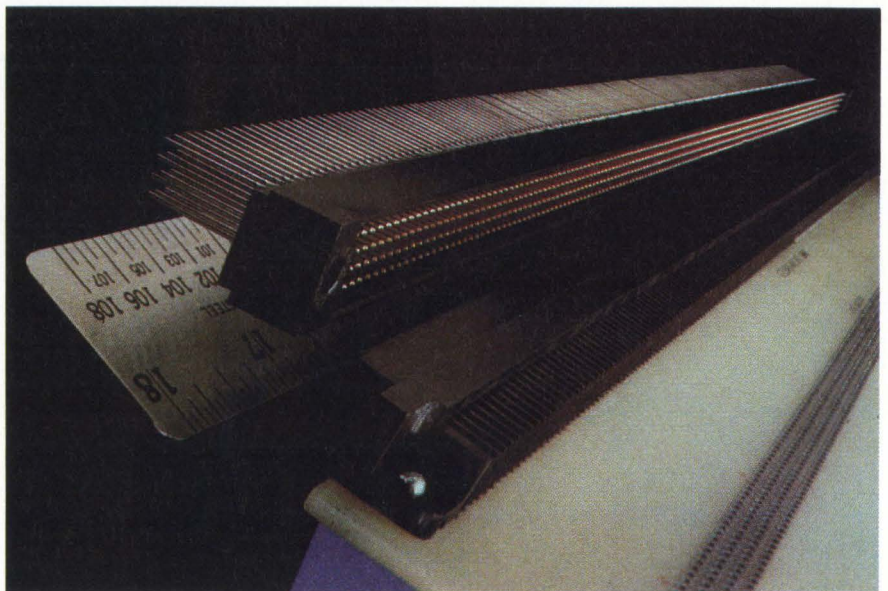


Figure 3: Two-piece connectors generally use a pin and receptacle arrangement.



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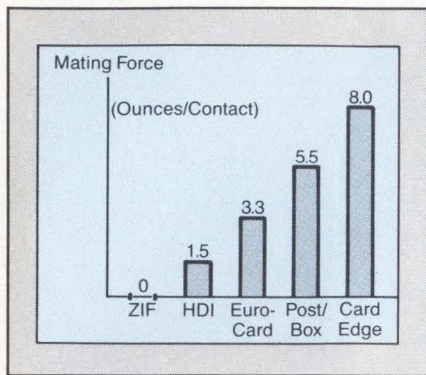


Figure 4: Comparison of mating forces for five connector families from AMP, Inc.

Card-edge ZIF connectors, as used on the split backplane, reduce the mating force to zero when the connector is engaged or disengaged. But the force required to cam the contacts closed limits the number of positions. The connector must still compensate for board tolerances. Nevertheless, it should be considered when a large number of positions are required.

The two-piece connector, **Figure 3**, where one half of the connector is on one board and the other half is on the mother-board, overcomes many of the disadvantages of the card-edge connector. Most versions use a pin and receptacle. This

eliminates the need to mate with both sides of the board, for up to four rows of pins.

A single manufacturer controls and accounts for the tolerances of both mating components of two-piece connectors. As a result, the mating forces for each contact pair are lower to allow as many as 700 contacts per connector. Contacts can be 0.001", 0.075", or 0.050" centers.

**Figure 4** shows the mating force per contact for five connector families from AMP. For the three center families of two-piece connectors the maximum number of positions per connector increases as the mating force drops. The ZIF connector is still limited by the force required to cam the contacts closed.

Two-piece connectors cost more but offer lower in-place and applied costs over card-edge connectors. They reduce the use of gold in both connectors and PC boards. The connector manufacturer can selectively plate connector contacts with gold only in the areas where the contacts mate. Board manufacturers typically allow for board tolerances with large PC pads. The higher mating force of the card-edge connectors usually also requires a thicker plating layer on both connector and board contacts.

Cost savings in board manufacture come from less board preparation — such as chamfered lead-in to aid insertion of the board into a card-edge connector. Two-piece connectors' tolerance of variations in board thickness may mean fewer board rejects.

Two-piece connectors are reliable first because the receptacle contact allows it to mate on both sides of the male contact. This provides redundant electrical continuity. Second, the connector is relatively insensitive to vibration. Because the receptacle contacts can have spring members of different lengths, electrical contact of each member is ensured during extreme vibration. Third, receptacle contacts are in cavities that protect them from stubbing during mating. Special cavities can also be molded into the housing of two-piece connectors to accommodate power, coaxial, or fiber optic contacts.

Both card-edge and two-piece connectors are predominately used with backplanes. The use of bottom- or top-entry receptacles in connectors allows boards to be stacked. A special two-piece stacking ZIF connector is easily adaptable to a stacking bus.

Increasing electronic sophistication, density, and application requires design and packaging engineers to carefully weigh options. The wrong choice can limit the system design or make design of future systems incompatible with existing systems.

As the number of I/O connections per board increases, the need for a flexible, high density bus also increases. The selection of the bus affects the efficiency of the system; similarly, selection of the connector affects the efficiency with which the bus is implemented.

— George Lawrence, Senior Development Engineer, AMP Inc.

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## DEPARTMENTS/CAD/CAM

### A CAD Program From Lucasfilm

From the people who brought you Starwars is a software package for designing electronic circuits boards and semicustom integrated circuits. Appropriately called CADroid, the Lucasfilm schematic capture package runs on a variety of UNIX-based computers such as the Sun workstation, Apple's Lisa, Apollo, and the CADMUS 9790. Priced at \$6000 for first time users, CADroid is aimed at users who want to integrate low cost workstations with affordable electronics CAD.

CADroid is designed to be the front-end of electronics design by allowing a user to create a library of schematic draw-

ings, checking the schematics for errors and generating a netlist. The schematic design module was written in C and provides convenient interfaces to other modules such as simulation, verification placement and layout packages. The editor offers windowing and menus, and uses a mouse and keyboard for data entry. The menu, which has 25 commands and 55 subcommands, allows hierarchical design rules with unlimited levels of hierarchy. Data entry through the drawing facility has drawing tools such as attach, move, jump, erase, flip and unmove. Zoom and pan are also possible where the drawing space can be as large as 650"

× 650".

What makes the package unique is that the software is sold independent of hardware. Typically CAD packages are sold inclusive of hardware. The goal was to create a transportable CAD system on the UNIX operating system. In addition, the package is unique in providing drivers for routing. After a typical CAD system creates a netlist, the user brings the tape to a service bureau for post processing. While there are hooks to interface with a driver, an added charge is made in addition to the routing. The finished result is a printed circuit board (pcb) layout. CADroid differs by including the DIP formats in its library to configure the schematic for a board's physical layout. This simplifies the process in addition to reducing costs.



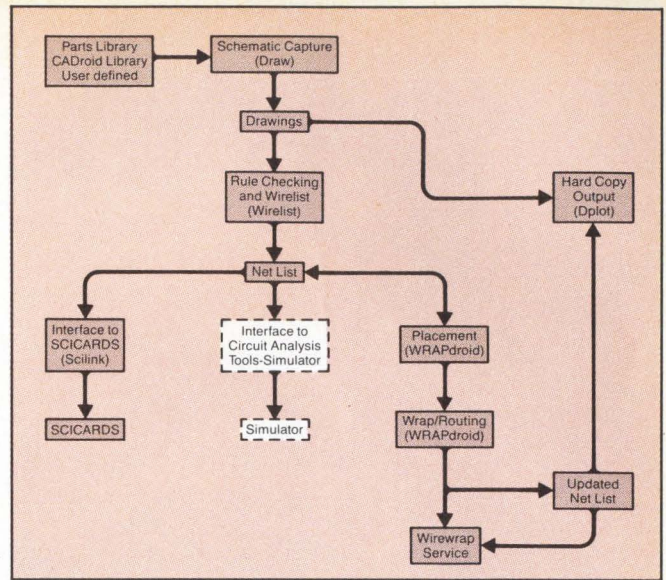
The origins of the CAD package came from SUDS, a Stanford University Design System that ran on a PDP-10 and was written in assembly language. The commercial software group (CSG) at Lucasfilm used many of the basic concepts of SUDS for their own CAD system, wrote transportable code in C, and took advantage of the basic library of parts while adding more components.

Lucasfilm plans to offer additional modules that will enhance the present system. One of these packages, WRAPdroid, optimizes placement and wire routing for wirewrapping boards. WRAPdroid consists of two major programs, an automatic placement program and an optimized routing or wrap program. Optimizing produces shorter physical paths which create better signal conditions, in addition to allowing a higher clock rate.

The advantage to using a wirewrapping process is that complex boards, produced in small quantities, may not justify the costs of creating printed circuits boards. The program uses a process called an annealing optimizer. Conventional optimizers start at a random route and search for a better one while replacing the old route. In an annealing optimizer the searching criteria are relaxed in the beginning and tightened as the process continues. This method searches a larger set of possibilities, creating more optimal conditions. The program starts with the parts "frozen" in place on the board and then searches for the best path for connecting the pins together. The WRAPdroid output can then be converted into a suitable output for use by an automatic wirewrapping service such as Augat Datatex.

One of the features of CADroid is a library of over 1000 building blocks which includes TTL and ECL parts, discrete components and linear devices. User definable functions can also be created. Sets that contain many objects can be created and edited for merging and moving. The sets can then have identifiable values such as extraneous or unconnected points. Later, during checking, these points can be tested and dangling points discovered. Set expressions and variables are possible using C syntax. Some of the tools include loops for repetitious actions, expression evaluators such as "if... then... do," and user definable macros for creating long sequences of commands. The macros may be nested to any level of depth. An unusual feature not found in other CAD systems is an expression parser which

Figure 1: CADroid Overview.



acts as an intelligent macro. While other CAD systems may have a smoother linguistic structure, CADroid has greater power and intelligence and, as a result, requires familiarity in its optimal use. Documentation is excellent and the manual has complete information including installation.

The drawing space can be very large, 65,000 x 65,000 points, where the screen refreshes the image each frame. Users

can choose plot drawing sizes A through E. Printers and plotters are filtered through the UNIX format for Imagen, Versatec, and Benson devices. In addition, there is a direct SCICARDS interface for PCB layout.

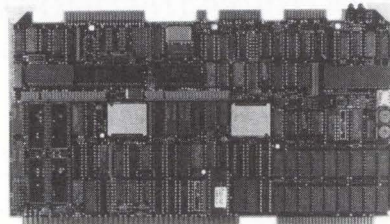
CADroid is a cost effective CAD program because it allows users to configure and upgrade their own CAD system.

—MacNicol  
Write 238

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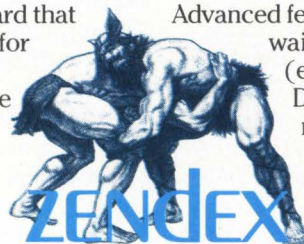
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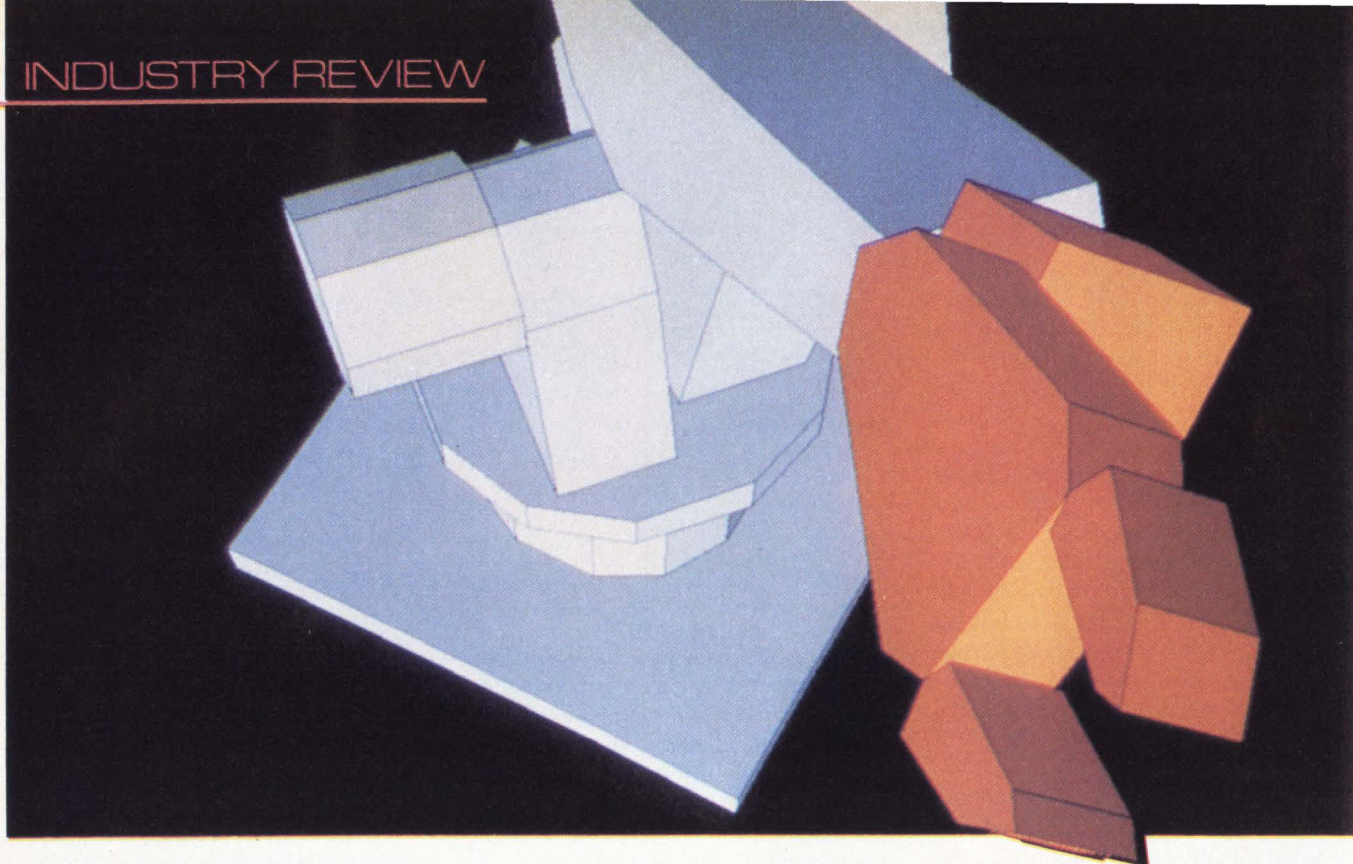
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# Silicon Support For Solid Modeling

*Graphics manufacturers are depending more on application-specific VLSI to perform demanding tasks in solid modeling.*

by Gregory MacNicol,  
West Coast Technical Editor

Striking images of objects never before seen can be generated by computers with solid modeling. The goal is to create images of objects complete with shadows, perspective, color, depth and realism. Some applications for this rapidly changing technology include CAD, molecular modeling, animation, medical imaging, and architecture. Generating these images is a complex task and, as a result, graphics designers have taken many different approaches.

While advances in memory technology, wide-word architecture, and high-speed

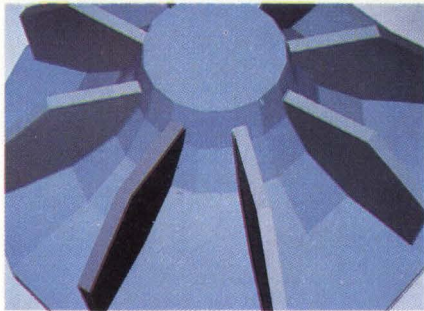
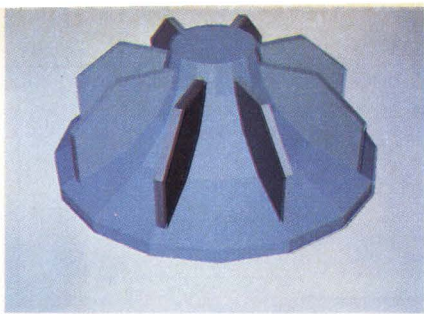
bus design have generated higher performance, few advancements have made a greater impact than custom graphics chips. Most graphics IC manufacturers design chips targeted at the primary markets: CAD, medical and geophysical representation, and modeling. These applications differ from computer graphics functions such as image analysis, where data must be modified after it has been displayed. Many of the latest custom chips, however, are aimed directly at solid modeling.

To attain three-dimensional realism, solid modeling systems transform model's complete spatial data into pixels. An important class of data manipula-

tions, called set operations, allows users to generate models of unlimited complexity. Traditionally there are two families of set operations. Constructive Solid Geometry (CSG) modelers use set operations (very basic graphics primitives) as the primary means of model definition. They represent a solid by a tree of set operations. Boundary Representation modelers, in contrast, define solids by faces, edges and vertices. Each family requires a different kind of database and allows for different methods of clipping, hidden object elimination, perspective control, and special effects such as translucency. Any solid modeling program must be able to translate either database into useful display functions.

The creation of an image on a screen follows a logical path. As a model evolves, the host computer builds and maintains a working representation of the model. This model may take form in polyhedral approximations or be represented in complex parametric cubic surface patches. Each patch, and in many cases each pixel, is given an intensity





Left: Photo courtesy Silicon Graphics. Above: Two more examples of solid models from Silicon Graphics.

value in addition to its color to represent proper shading.

Shading, which takes place after hidden line calculations, is composed of diffuse illumination effects, multiple light sources and transparency. Two methods of shading dominate and are considered standard functions of solid modeling systems. Gouraud shading shades polygons by linearly interpolating between the color values specified at the vertices. The method is simple and quick due to averaging one pixel against another. Its weakness is that it can produce "Mach bands" where lines of darkness or lightness causes unnatural lighting effects. Smaller patches reduce this effect at the cost of longer display creation times. The second method, Phong shading, relies on interpolating normal vectors rather than color values and applying the shading model at each pixel. This method remedies many of the problems of Gouraud shading at the cost of greater computation time.

At this point the data can be sent to the frame buffer. Meanwhile the host computer must deal with I/O overhead, floating point operations, and memory control. Graphics designers have been trying to liberate the host computer from these functions by using dedicated silicon chips.

Three companies are presently offering graphics support in silicon that resolves the problems of producing real time interaction of shaded graphics images. Each company has focused on par-

ticular problems and distinct markets. Xtar (Elk Grove, IL) produces two chips for integration into a board. Weitek (Sunnyvale, CA) has a chip set in addition to the complete set on a Multibus configuration, and Silicon Graphics (Mountain View, CA) offers a complete workstation using their proprietary chip set.

### Solids Modeling Engine

Weitek has created what they call a Solids Modeling Engine. After the host computer has transformed the database into a display list, the resulting bicubic patches in world coordinates are buffered in the display list memory and sent to the Solid Modeling Engine. There, the image is transformed, clipped, shaded and sent to the frame buffer via a 16-bit, high-speed data path. This configuration allows a multi-thousand polygon model to be displayed in seconds. The Solids Modeling Engine consists of a single-based transformation processor and a two-board tiling engine.

The 32-bit transformation processor performs all the computation for transformation and parameter calculations. It transforms and clips 110,000 3-D (x,y,z) coordinates per second. Processing is possible due to Weitek's 32-bit floating point adder, multiplier and register file chips that execute 16 million floating point operations per second (MFLOPS). Communications I/O is a major problem with fast graphics processors, so a 4K × 32-bit local data buffer minimizes potential bottlenecks. Additionally, a 2K by 96-

bit Writable Control Store is available for OEMs to implement custom algorithms for specific applications such as surface intersection.

After the Transformation Processor mathematically modifies (tessellates) the polygons of the polyhedra or the parametric cubic patches into triangles, the Tiling Engine takes the planar triangles or tiles, and applies the Z-buffer algorithm for hidden surface removal. The Tiling Engine is critical to performance and requires two boards, one used only as memory for the Z-buffer and the other for computation. The Z-buffer is an extension of a frame buffer concept where the Z value of the image-space of the object is stored at every raster element as well as intensity. The Z value of any new point is compared with the value of Z already in memory. If the new point is behind, it is discarded. But if the new point is in front, it replaces the old value.

There are several advantages to using a Z-buffer. Hidden surface and intersection of arbitrary surface problems are handled rapidly and easily for images of any complexity. Sorting of complex objects is not necessary, because surfaces can be written into the buffer in any order. The main disadvantage is that the Z-buffer requires so much memory. A 512 × 512 pixel buffer with 8 bits of Z uses 256K 8-bit words. In addition, any algorithm providing anti-aliasing requires that the silhouette of the objects contain the corresponding raster elements and should be some combination of the intensities of the

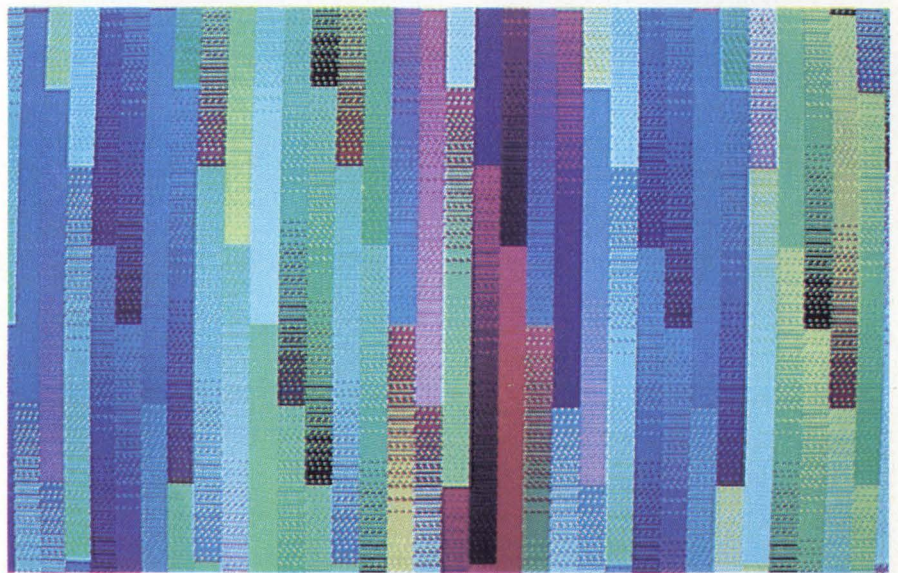


Figure 1: An example of the application of Xtar's Video Shift Register (VSR) dithering feature. This system contains four bits per pixel which allows 16 colors to be displayed on the screen at one time. With four bits per pixel and 16 different patterns over 1800 effective color combinations can be generated on the screen at one time. This allows the user to have a large number of colors on the screen while still keeping the number of bits per pixel in the frame buffer at a minimum.



two objects. If the objects were displayed in random order, then the intensities of the objects, when combined, would produce a local error. For anti-aliasing, then, it may be necessary to sort the objects prior to display time to eliminate the staircase effect.

The Tiling Engine Z-buffer uses 64K RAMs in its 1.31 Mbyte memory plane but can use 256K RAMs when they are available. The spatial resolution is  $512 \times 512$  pixels but images requiring  $1024 \times 1024$  pixels can be handled in four passes (or one pass with 256K RAMs). Each pixel is assigned 24 bits of Z and is user selectable to have 16, 14 or 12 bits of Z leaving 8, 10 or 12 bits for intensity, respectively. Additionally, the user can define the color palette and separate bits into shading values. For example, if a 12-bit intensity field is allocated, six bits might be used for the palette and six for shading. This provides 64 displayable colors, each with 64 intensities. During processing, a shading value is calculated for each pixel by interpolating between vertices, this value is stored together with the base color in the Z-buffer. After tiling, the image is formatted and sent to a frame buffer. If the frame buffer lacks a color look up table, the postprocessor can decompose the 12-bit intensity into R,G,B values through a program supplied transform table.

To properly shade the model, either Constant, Gouraud or Phong shading may be chosen. Normals to the cubic patch are computed at the vertices of the polygons. In the case of Constant shading, they are averaged using a factor derived from the diffuse model, in which light is scattered equally in all directions. With Gouraud

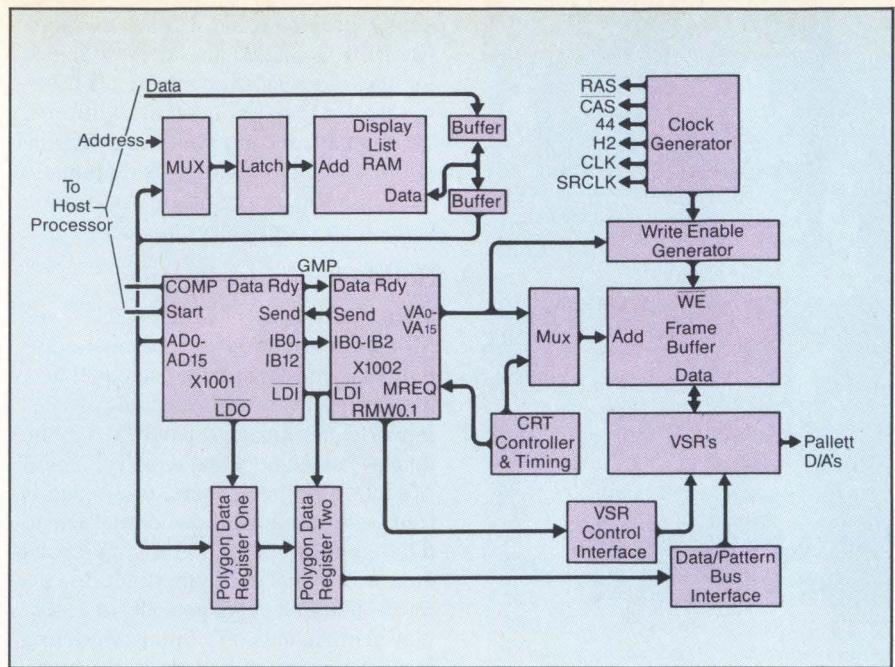


Figure 2: Typical block diagram using Xtar's GMP and VSR.

shading, the diffuse model is applied at each vertex. Phong shading is more realistic but slower to execute. Some situations may require calculation of the surface normal of the object-space surface before perspective transformation because perspective distorts the surface and hence falsifies the intensity. Surface normals are interpolated with the Tiling Engine from 16 control points of each tile.

The concept of the tile has its origins from the cubic patches. A surface may be composed of many patches from the poly-

gon or bicubic solid model data base. Drawing a diagonal line within each one creates a set of triangles. These triangles, or tiles, may then be shaded. One approach to shading is to divide each tile into smaller tiles for a more realistic shading effect. The Tiling Engine, in contrast, determines the color and intensity of each pixel from the Z-buffer, creating better shading and allowing translucency effects (to see through surfaces), edge highlighting, and patterning or texturing of surfaces.

With capabilities like these, the solid modeling engine can display 6000 shaded triangular polygons in six seconds. This translates to between 55,000 and 180,000 3-D vectors per second. Because the boards communicate through the high-speed P2 interface on the Multibus (2.5M pixels/sec) and computations are executed in parallel, a 100 patch, 9000 quadrilateral model can be executed in 1.35 seconds. The I/O ports to the frame buffer will often increase display time however. The I/O port to the frame buffer is either through the Multibus or a 16-bit parallel interface to a VAX, Apollo's DN600 workstation, or Data General's MV series of computers. An optional second DMA port may be configured to provide high speed pixel unloading to a frame buffer.

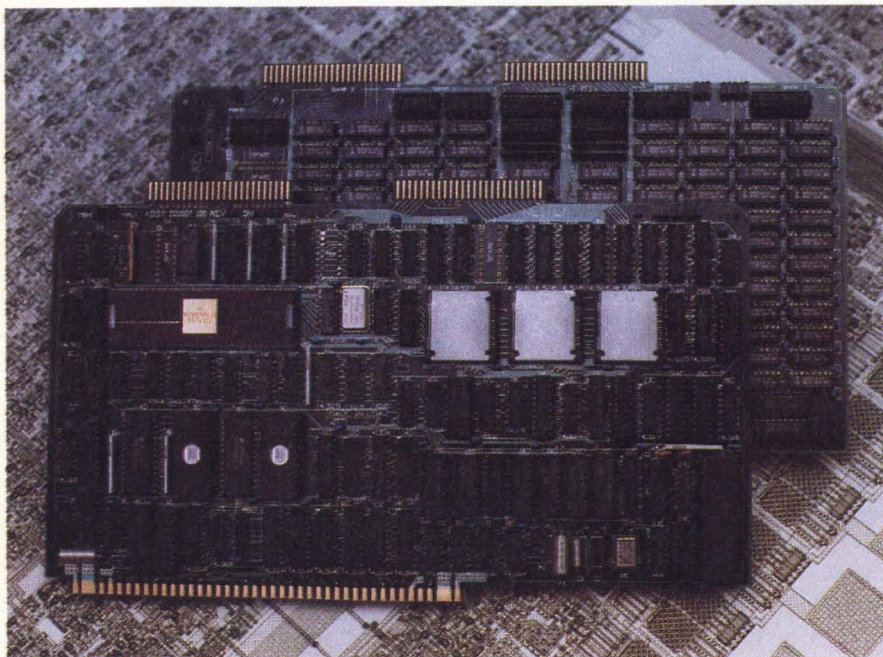


Figure 3: The Weitek tiling engine is built around 2 Multibus boards. One is used only for Zbuffer memory.



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If this isn't fast enough, an optional polygon buffer can maximize output speed by holding one to four pictures in polygon form. Each frame contains a list of control items and control commands which define the picture. As long as the view is not changed, the host is required to transform only changes such as additions and modifications. Minimizing the host's burden of recalculating an image results in throughput improvement of 100 to 200%.

## Graphics Microprocessor

Designing a solid modeling system around a board or chip set has advantages and disadvantages. The lower the level a designer or small systems integrator has to build from, the less support he has in developing a usable product. On the other hand, where cost is a primary concern, and where volume justifies, the system architect has the advantage of designing from specific goals without external constraints. From components to software, the designer can optimize for special applications at reasonable costs.

With an entirely different approach, Xtar (Elk Grove, IL) has its origins in video games. Requiring high speed for animation and scene simulation, VLSI chips were developed for the video arcade market where rates of 30 frames per second are common. Other CRT controller chips such as the NEC 7220 are 10 times faster than a microprocessor working alone, but the display speed is still unsatisfactory for real time simulation.

Xtar offers two IC products for use on board level designs. The Graphics Microprocessor (GMP) is a two chip set that interfaces with any microprocessor. This fast display processor generates points,

lines, filled polygons and polygonally-defined characters for storage in a frame buffer. The other product addresses a problem common to graphics systems designers. After all calculations are completed and the frame buffer is full with the correct display information, the data must be sent to the monitor. This requires parallel to serial conversion, typically through a shift register, which can be a major bottleneck. Xtar makes a Video Shift Register (VSR) that interfaces directly with the GMP for functions that transcend normal shift register operations.

The GMP, which is on two 40-pin DIPs, can display polygons at speeds up to 160 million pixels per second. It typically interfaces a host microprocessor with a frame buffer that displays up to  $2048 \times 2048 \times 32$  bits. Communication with the host is through a display list RAM which may contain up to 64K words. The display list function is used for two reasons; one can interface any microprocessor to the display list, and faster operation is obtained with the read-modify-write capability. The instruction set is specifically designed to draw filled polygons quickly and can update every pixel in the frame buffer at 130 to 300 times per second. As resolution is increased, so is the drawing speed, so the number of screen updates per second is relatively constant.

Typical use of the GMP is illustrated in **Figure 2**. The display list is contained in separate RAM for fast reading and writing. This reduces the I/O overhead on the host CPU. The use of shared memory is essential to Xtar's concept of fast and versatile solid modeling hardware. The 320 nsec cycle time of the DRAM is used on alternate memory cycles, allowing the host

processor to access memory more efficiently. Because the GMP chip set does not generate CRT sync signals or video refresh information, a standard CRT controller must be added.

The graphics primitives used by the GMP are divided into three major categories: points, lines, and polygons. The GMP relieves the host CPU by calculating the different parameters defining lines to be drawn and searching in the frame buffer for polygon edges to do polygon fills. Use of the optional VSRs with the frame buffer increases throughput significantly.

The VSRs are designed specifically for use with the GMP. While the GMP controls the address and Write Enable inputs to the frame buffer, the VSR controls the data bus of the frame buffer. The VSR reads the pixels in parallel from the frame buffer and converts them to a serial stream of values which can be fed to the address inputs of the color palette RAM. It can also read one strip of the frame buffer and hold the data until it can be read by the host processor. The VSR has the capability of ditherizing, or mixing various colored pixels, so the filled polygon can be represented in pseudo-shades of colors. This feature can increase the number of displayable colors without increasing the depth of the frame buffer. As long as memory costs remain high, this is a useful feature.

The VSR takes advantage of the nibble mode of addressing graphics memory. The newer  $16K \times 4$  DRAMs such as the 4416 are designed to benefit graphics designers by providing wide bandwidth and fine granularity. Although still organized as a  $64K \times 1$  chip, the internal structure of a chip with nibble mode is  $16K \times 4$  and allows four bits of data to be accessed for each RAS cycle. Since each VSR is four bits wide, a  $256 \times 256 \times 4$  bits per pixel display with a double buffered frame buffer would require only eight DRAMs, and therefore two VSRs. Bit planes in the frame buffer can be accessed independently, so operations such as AND, OR, and XOR can be performed separately.

Xtar's chips require the host to calculate shading values. The method chosen can be any contemporary algorithm where the host calculates the normal of the vertices and sends the information to the display list. The algorithm can also "cheat" by omitting unnecessary shading or optimizing on simple shading methods when possible.

In many graphics systems, it is necessary for the host processor to read the values of pixels in the frame buffer. Using additional circuitry, the VSR can be used

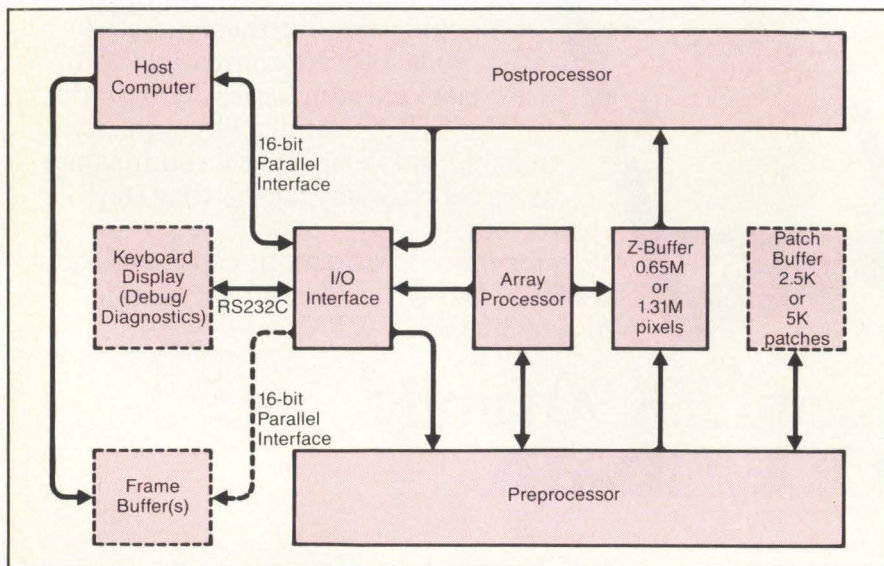
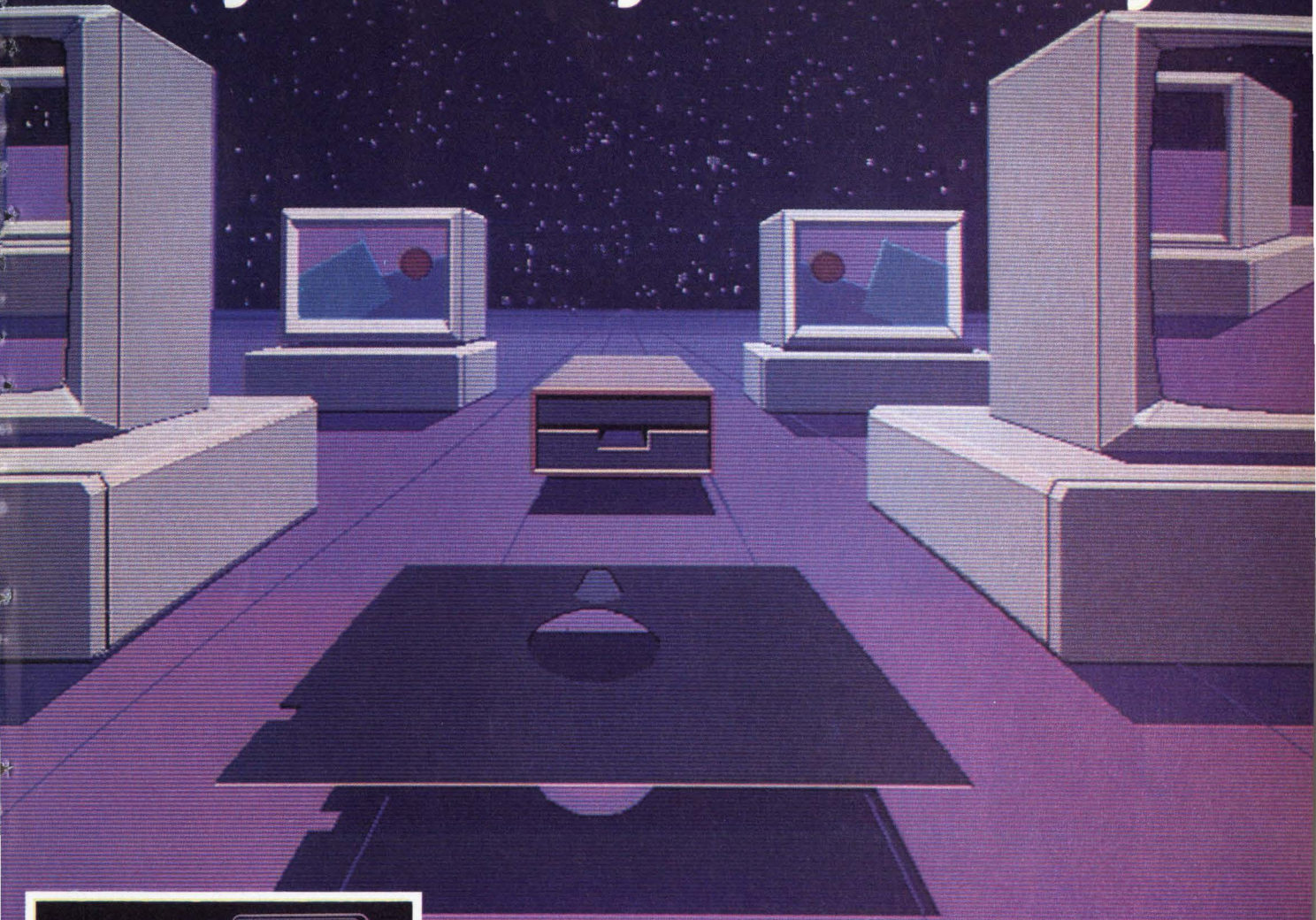


Figure 4: Functional block diagram of Weitek's graphics engine.



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## Geometry Engine

Clearly, the designer who uses the chip approach for creating solid models can take advantage of the latest components for specific applications. Upgrading is easily implemented and material investment is minimized. But Silicon Graphics' (Mountain View, CA) approach is to provide not just the custom chips for solid modeling, but a complete system.

The Geometry Engine (GE) from Silicon Graphics provides the means to execute real time processing for tasks that are common to both 2-D and 3-D applications. After three years of work at Stanford, Dr. James Clark, founder of Silicon Graphics, developed a set of custom chips that are microprocessor implementations of common graphics functions. Twelve ICs constitute the GE, but rather than sell the VLSI chips alone, they are used in a Multi-bus-based system using a 68000 microprocessor.

The Integrated Raster Imaging System (IRIS) uses the capability of these chips to transform, clip and scale 65,000 coordinates per second. Operands can be in 32-bit floating point, or 24-bit integer formats. Polygons can be filled at 44 million pixels per second where viewing is either orthographic or in perspective.

The IRIS workstation can display 4096 of 16 million colors which represent 24-bit values, eight bits each for red, green, and blue. At 1024 x 1024 resolution, even with optional double buffering, the processing demands are great.

The manipulations of solid modeling, such as clipping and scaling, are calculation intensive. They require fast floating point math computations in addition to

iterative matrix multiply and divide operations. This has been a major bottleneck in creating an image quickly because the host processor, already slow at floating point calculations, must do that and all other processing. The GE solves these and other graphics intensive functions using three subsystems on separate flatpacks: the matrix clipping, and scaling engines. Used together, 4 x 4 floating point matrices, matrix multiply operations, clipping and scaling operations, hit testing, and curve generation can be implemented from higher order commands.

The matrix subsystem is a stack of 4 x 4 floating point matrices for 2-D and 3-D coordinate transformations including object rotations, translations, scaling perspective, and orthographic projections. It is the first of the four subsystems in the pipeline. Full floating point transformation of all coordinates is done in this subsystem in 15 msec. using an eight deep, 4 x 4 matrix stack, in addition to the 4 x 4 matrix multiplier. The matrix subsystem also generates cubic and rational cubic curves such as conic curves, where new points in a curve are generated in 10  $\mu$ secs.

The clipping subsystem receives transformed data from the matrix subsystem. A user may use four or six GE ICs depending on the need to clip objects near or far to the clipping boundaries. If there is no need for clipping at these boundaries, two chips may be omitted. A hit-testing mode is included in the clipping subsystem for testing objects for intersection within the viewer's window. This mode omits output of certain extraneous data from the GE.

The last two GE chips which comprise the scaling subsystem, convert data from the pipeline to the output device. The viewport registers control the scale of the win-

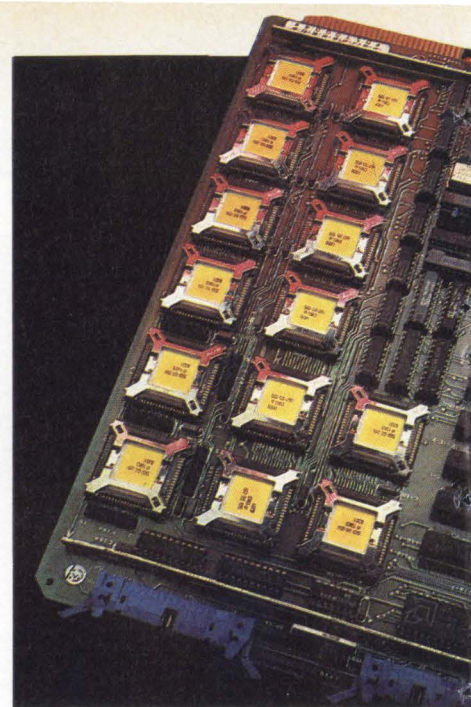


Figure 5: The geometry engine as used in the IRIS workstation from Silicon Graphics.

dow on the user's drawing space and allow up to 24-bit integers. This is where orthographic or perspective projection is calculated for 3-D mapping. The scaling subsystem treats all coordinates of x,y,z the same. Z values are used for intensity depth cueing and perspective depth.

The GE acts as a slave processor and can almost be viewed as a hardware subroutine system. The instruction set has three types of instructions that manipulate graphics data. The drawing instructions, which are followed by four 32-bit floating point numbers, are supplied to the matrix subsystem for transformation. The register manipulation instructions are used for setting up the matrix, matrix stack, or viewport registers. The last set of instructions are miscellaneous commands such as setting or clearing the hit mode. All input data must be in the user's virtual drawing coordinate system (integer or floating point).

## Solid Choices

The decision whether to use any of the available VLSI technologies is difficult, even if the price/performance looks attractive. Weitek, for example, makes a fast display system for creating fully shaded objects but it does not have the capability to read or modify the frame buffer after creating an image. In addition, the board set requires programming, from database interpretation to output drivers. The trade-off, of course, is versatility, the reason many major CAD companies are using the board

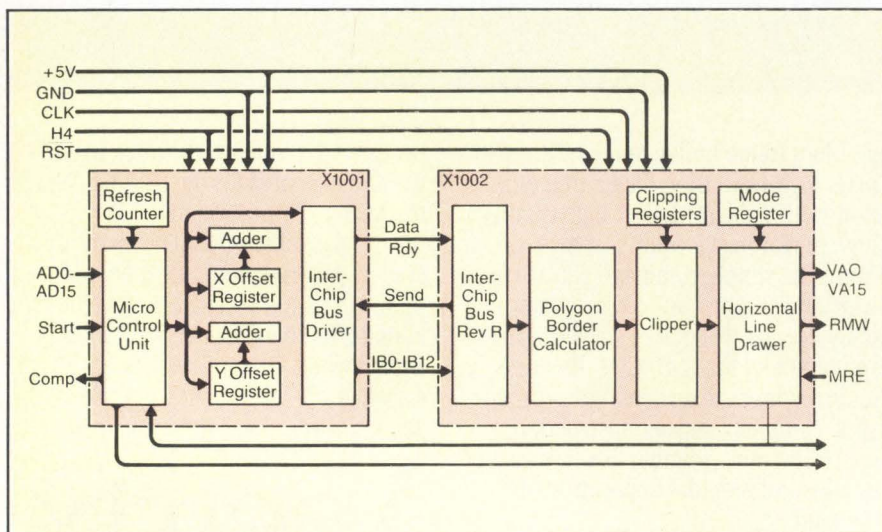


Figure 6: The GMP uses 2 chips for graphics processing.



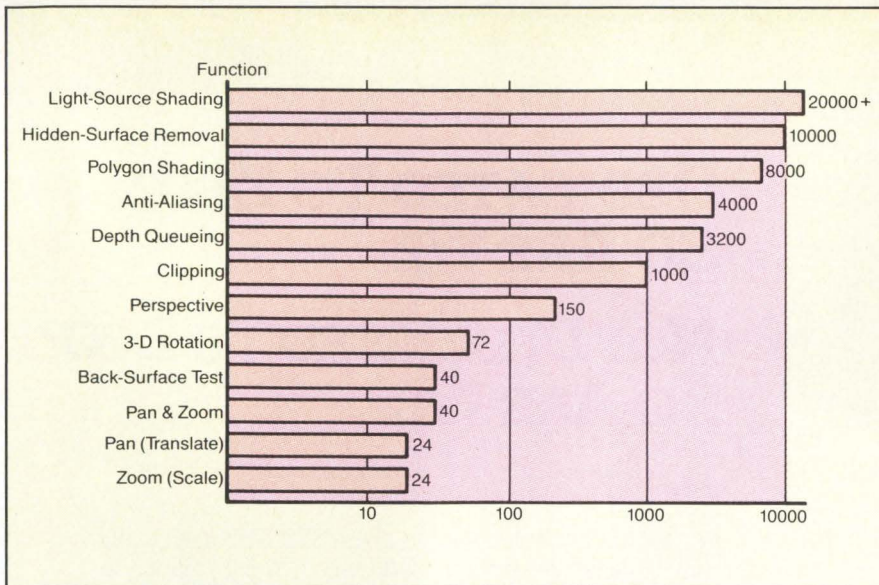


Figure 7: This table represents the time requirements for 3D soliding processes.

set with their existing systems.

A weakness of the IRIS system is that newer algorithms in computer graphics that may benefit from the matrix multiplier cannot easily utilize its internal hardware. The overhead in using the chips is equivalent to using standard code. The resolution is fixed, and in addition, users already committed to a bus approach cannot economically use the system. A typical user is one who wants a complete system, with an operating system, powerful graphics primitives and no hardware compatibility problems.

Manufacturers are responding to sophisticated users' needs. While the IRIS workstation is not really an effective frame buffer, Silicon Graphics is adding hardware and software that makes this function possible. They are also adding a function called block image transfer (otherwise known as bit block transfer), where sections of an image can be moved about easily, such as icons on a menu. Weitek is also adding more math-intensive hardware such as a divide function with a  $32 \times 32$ -bit register for providing faster graphics related calculations.

### Conclusion

The current trend to incorporate solid modeling functions in silicon is just beginning. Work being done at universities such as the University of North Carolina Microelectronics Center is resulting in new products that will soon reach the commercial market. Other developments, still proprietary, are focusing on two primary aspects: pixel output speed and specific graphics

algorithms. The success of solid modeling systems is based on useful interactivity. In terms of hardware, it can be interpreted as execution speed. And as greater rates are reached manufacturers will add

enhanced functionality such as Z-buffers. Ultimately though, a buyer must ask "am I buying hardware specs or real functionality?"

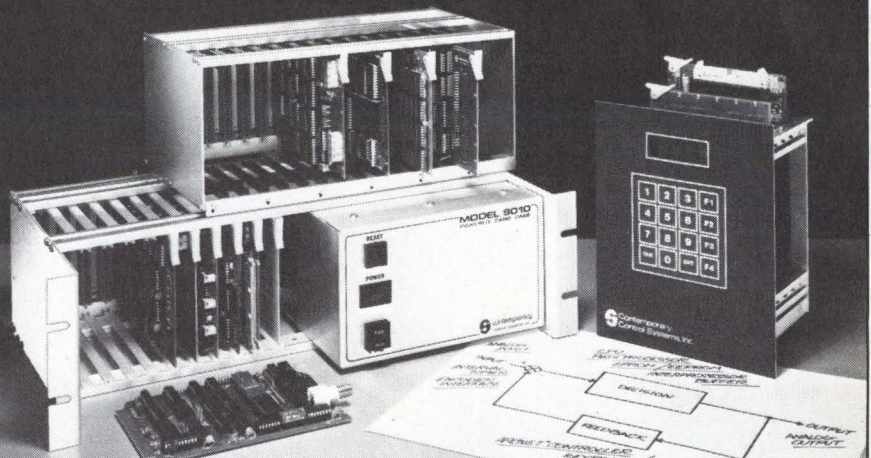
The latest developments in VLSI are not the only reason for the recent availability of these dedicated graphics chips. Memory is still a critical issue and graphics systems are dependent on the current memory marketplace. Were it not for the availability of the  $16K \times 4$  DRAMs, for instance, Xtar would be unable to take advantage of the higher bandwidth that they offer.

The demand for producing higher performance computer graphics is driving manufacturers to mold the best concepts in solid modeling into silicon. Combined with advances in custom VLSI technology, users can expect major advances in the capabilities of new systems. □

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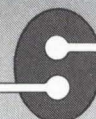
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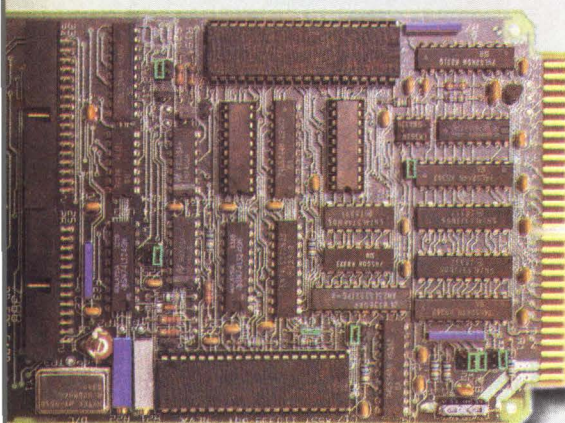
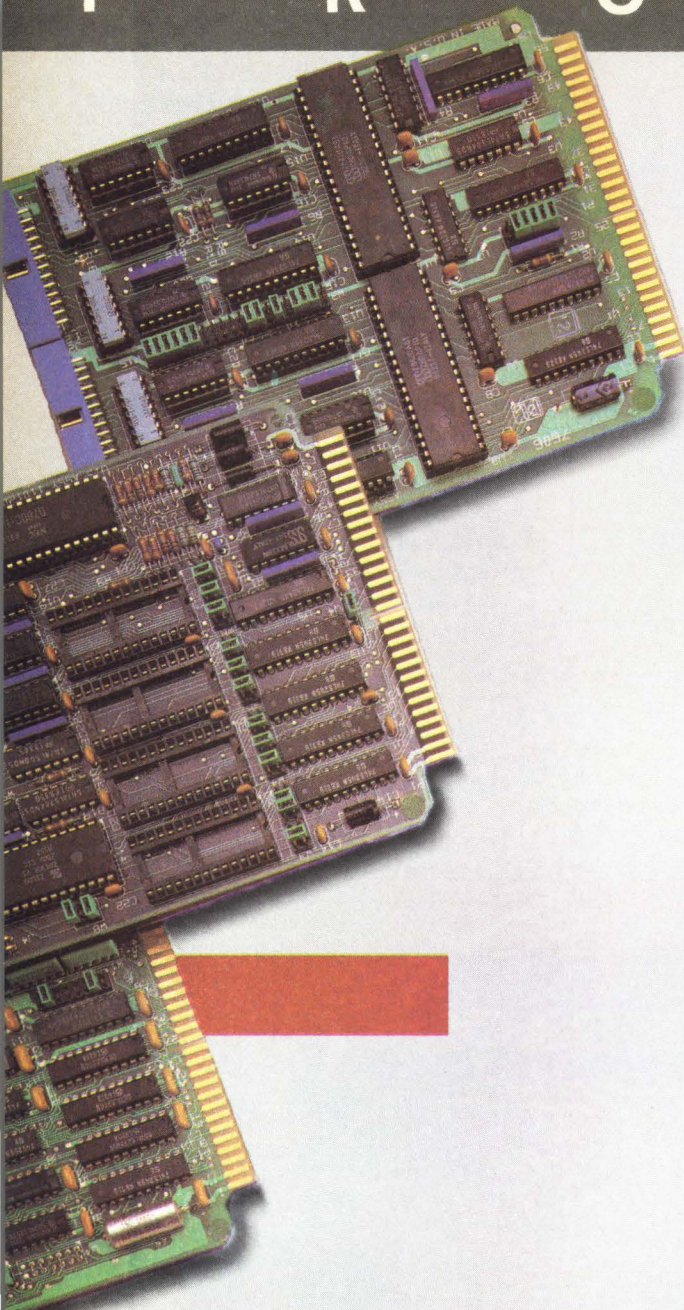
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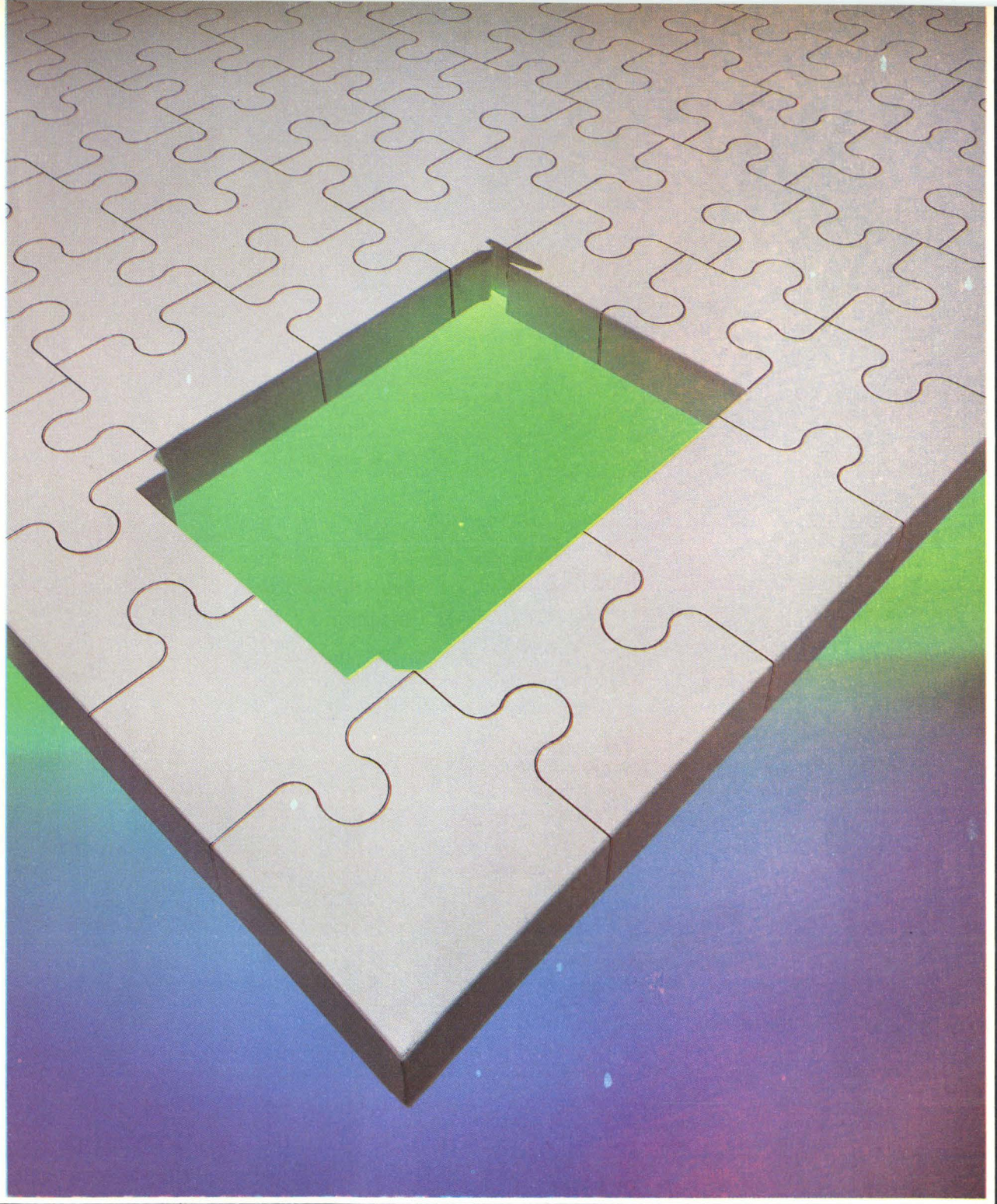
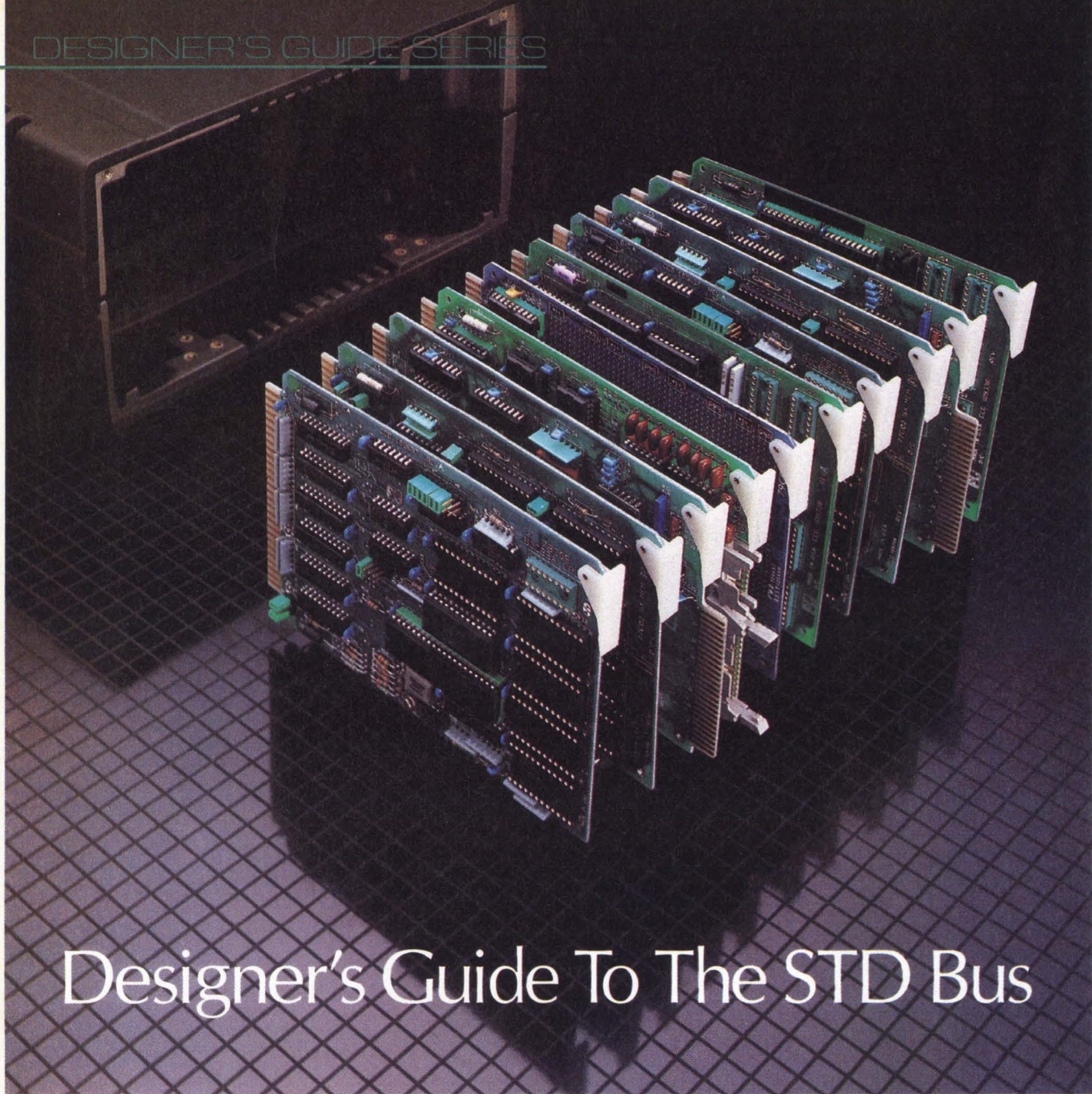


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Designer's Guide Series **STD BUS**





# Designer's Guide To The STD Bus

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*CMOS and the IBM PC breathe  
new life into the STD bus.*

---

by Dave Wilson, Executive Editor

The STD bus, developed by Pro-Log and introduced jointly with Mostek in 1978, defines a card size and interconnection scheme that supports a modular-by-function approach to micro-processor system design. Made available to industry without patent, copyright or trademark restrictions, it has become a recognized standard, supporting a wide variety of processors

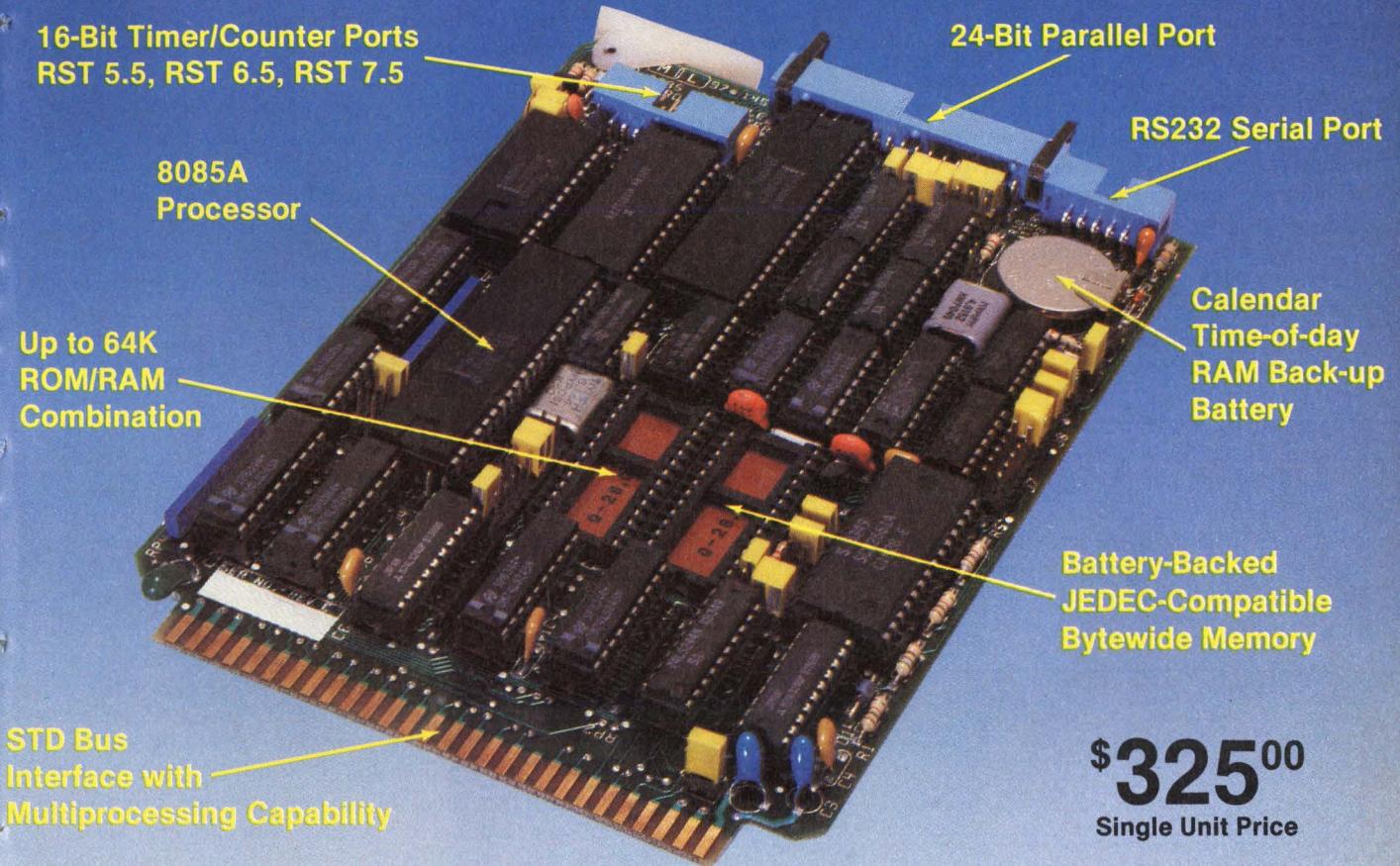
on the market. The range of applications for STD products, while traditionally very broad, is today continuing to grow. The applications are mainly in the automation, process control, monitoring and data acquisition areas, which is not surprising considering that this is the market sector for which the bus was designed.

## Compatibility

The objective of any bus structure is to provide flexibility to the user in configuring a system to fit specific needs without compatibility problems. Each unique processor, however, on the STD bus requires specific timing characteristics to perform properly. Consequently, each CPU has a set of guidelines to assure that many, if not all, products work together. The STD bus specifications serve to define the usage of the bus lines. The timing specifications serve to guide each manufacturer as he designs products for the bus for the unique processor segment



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that he chooses. According to Ray Alderman of the Matrix Corporation (Raleigh, NC), advances in CPU family compatible chips are creating more unique boards that run only with Z-80 or 6809 CPU chips that are destroying some of the compatibility of the bus products.

Although simple functions such as TTL latched I/O and static memory can usually be processor independent, more sophisticated functions often require a higher degree of integration between CPU timing and peripheral card timing. Users should be cautioned to think twice before mixing an STD-Z80 peripheral card with an STD-6809 CPU card. Picking cards from the same basic processor family will assure quicker integration, due to the maturity of the STD specs.

According to Ken Finster of Micro/Sys (Glendale, CA), another compatibility issue relates to the physical location of memory in RAM intensive systems. In such systems, typically using disk operating systems or multiple RAM banks, density requirements most often swing the user toward dynamic RAM technology. One trend seems to be tightly integrating the RAM array with the CPU, and placing both on the same card. At first glance this may appear to provide a size and cost advantage. The designer, however, should proceed carefully if more sophisticated systems are being built. Take, for instance, a multi-channel data comm line monitor application. In addition to the steady-state, predictable CPU memory addresses, the RAM array may also see high duty DMA accesses for serial channel data transfers. RAM refresh and other problems, sometimes quite subtle and evasive, may creep in. The approach Micro/Sys suggests for such systems is to consider the RAM as a globally accessible resource that must stand on its own. As such, Micro/Sys' dynamic RAM cards contain full refresh and timing support for the RAM array. Memory cycles can be initiated through the backplane from a variety of sources, with slightly

different timing characteristics, but the dynamic RAM array always sees the same timing, and unpredictable burst DMA transfers cannot affect RAM refresh.

### 16-Bit Microprocessors

The strong interest in 16-bit processors continues because it offers advanced system performance while still retaining the small STD footprint. New product designs at Dattricon (Lake Oswego, OR), for example, are based on the 68008, 68000, 68010 and 8088. In the case of the 68000 family, Dattricon are employing pin-grid array technology to enable them to pack a lot of functionality on the processor card. A tightly-coupled dual-port memory enables the processor to run at full speed on-board while having the capability to access off-board memory within the limits of the bus bandwidth.

The STD manufacturers' group has published a new specification for the 8088 processor with provision for multiplexing the upper address bits onto the data lines during the early portion of a cycle. In terms of compatibility, there are precautions a user must take for using STD-8088 with older boards. Ziotech (San Luis Obispo, CA) advises its users to select only memory boards that adhere to this extended addressing specification with I/O boards that are I/O mapped as opposed to memory mapped. Ziotech is currently compiling an STD-8088 compatibility guide that will identify all the existing boards that have been tested.

### I/O Cards

The higher levels of integration in both analog and digital circuits will both lower the cost and improve the functionality of STD bus boards. Unlike the S-100 bus, the STD bus is supported by a number of analog houses. In this area, lower hardware costs have led to distributed processing. A local microprocessor handles all data and stores it in local memory. The CPU board only has to read the required memory location to obtain analog data.

Surface mount devices, with their smaller size, will lead to adding more distributed processing and signal conditioning capabilities onto an STD bus system. One example of possible saving of board real estate in analog I/O boards is in the area of D/A converters. It is now possible to purchase four 8-bit voltage-output D/A converters in a single 20-pin package (AD7226). This means that one DIP package can replace up to nine individual components. In higher resolution D/A converters, the evolution to 12-bit monolithic parts has already arrived. Both Analog Devices' AD667 and Burr-Brown's BB811 offer a reference, D/A converter, double-buffered latches and an on-chip op amp. As few as three years ago, the latches, op amps and a reference would have to have been supplied externally, thereby using up limited board real estate. To increase I/O flexibility further, the Intel iSBX bus connector can give the systems integrator a choice of a number of daughter board cards that can be plugged into an STD system. This has been proposed to the STD Bus Manufacturers Group for inclusion in the STD specification.

### Role of CMOS

In the future, it appears that many new products on the STD bus will use primarily CMOS devices. According to John Hilburn, President of Microcomputer Systems (Baton Rouge, LA), the primary application of these cards will probably be in remote installations and dedicated applications that require communications with other computers, such as the IBM PC. The low power and high noise immunity have special benefits for the

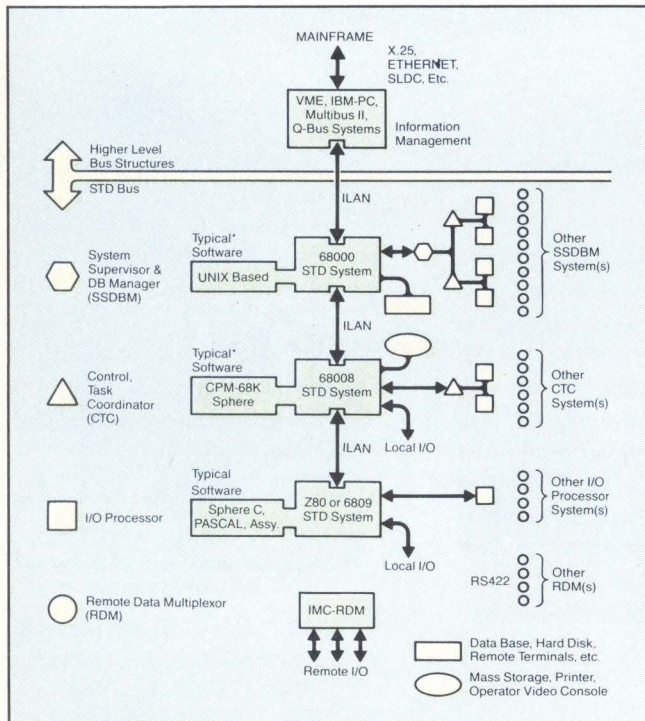
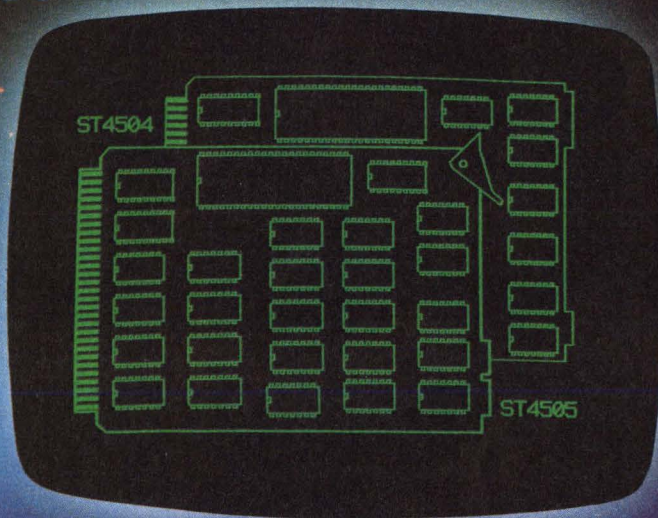
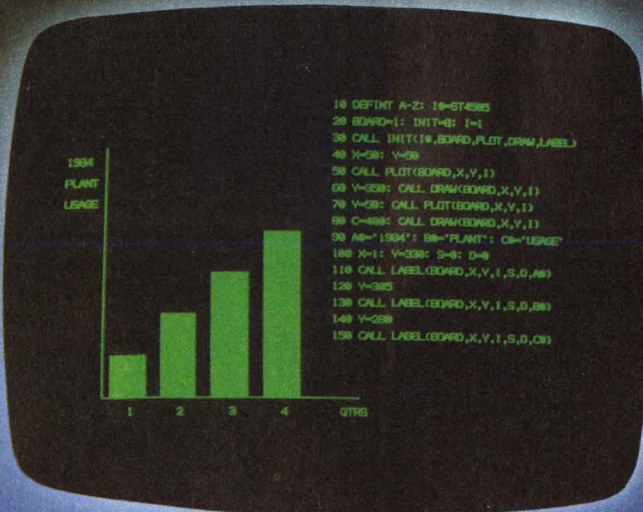


Figure 1: Dattricon's ILAN will use a multidrop RS-422 with up to 32 nodes per network.



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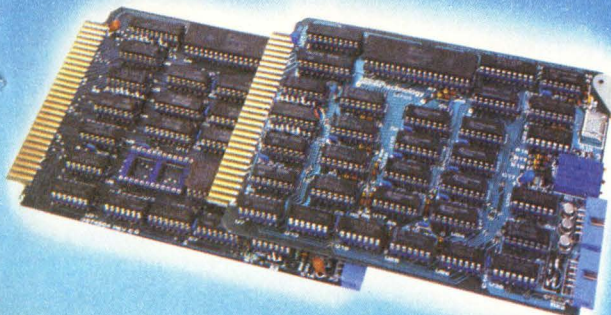
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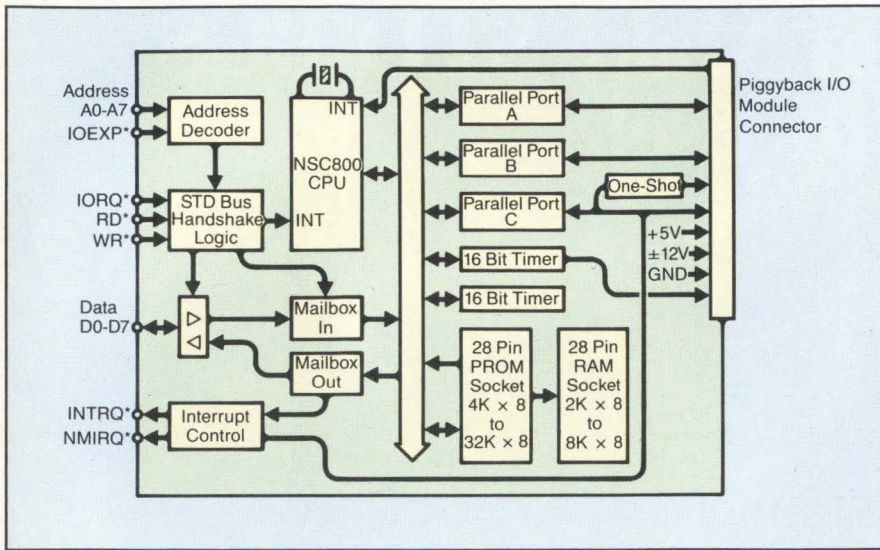


Figure 2: This SB8275 STD bus slave processor from MicroSys executes Z80 machine code, allowing firmware for the SB8275 to be developed on any systems capable of Z80 code development. The board looks like four sequential I/O ports to the host STD bus processor.

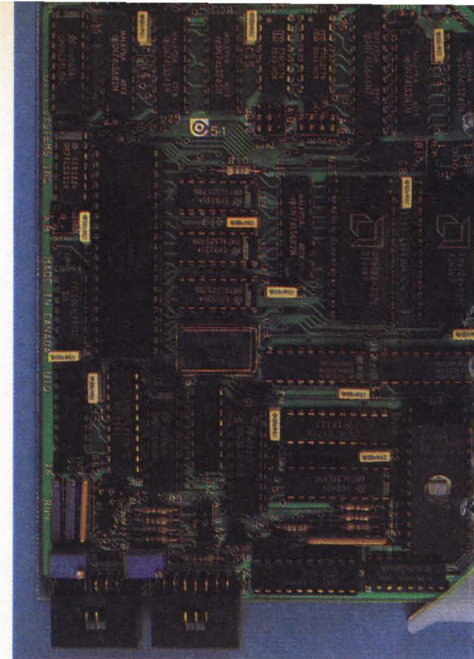


Figure 3: DY-4's color CRT controller for the STD bus can be configured for 8 level color or 16 level monochrome output. Character attributes include blink, intensity, foreground and background colors.

control environment, which complement the inherent advantages of the STD bus card size. Also, the CMOS STD bus may prove a challenge to other low-power buses not currently as well supported – National Semiconductor's (Santa Clara, CA) CIM-bus and Onset Computer's (Falmouth, MA) C-44 bus.

One of the first CMOS cards introduced was the MSI-1800 from Microcomputer Systems. Based on the NSC800, it is the forerunner of a range of products the company hopes to introduce this year – an 80C88 CPU as well as CMOS I/O cards providing both RS-232C and RS-422 communications protocols.

Pro-Log (Monterey, CA) have no less than nine CMOS cards on the market today. Their family includes three CPU cards, two based on the 80C85 and one on the Z80; two memory cards, two I/O cards and one serial communications card.

### Networks

STD bus based systems ideally serve the cost/performance requirements of the lower tiers in pyramidal systems as dedicated slave controllers, process monitors and data loggers. Because of this, Ethernet, X.25 and other proposed LAN standards are incompatible with low-end systems in terms of cost and scope of software implementation.

Perhaps the most popular interconnect method at present is the IEEE-488 Bus. The flexibility of the bus is no longer important solely for the test and measurement engineer, but has found wider applications in networking that will also affect the systems integrator (*Digital Design*, January 1984, p. 54). Both Ziatech and Applied Micro Technology (Tucson, AZ) provide STD to IEEE-488 interface cards.

Other STD vendors (such as Contemporary Control Systems and Dattricon) offer their own solutions. Contemporary (Downers Grove, IL), for example, have implemented the Arcnet on their S871 module providing up to 255 nodes and data rate to 2.5 Mbit. Each S871 module has an eight-position DIP switch which identifies the node address of the module. A 2K on-board

packet buffer provides four pages of packet storage and may double-buffer transmit and receive data as defined by the user. An on-board coax driver directly connects to RG 62/U coaxial cable that interconnects the nodes. According to Contemporary, applications include office automation, process control and remote I/O controllers.

Providing the vehicle to link STD-based systems to higher performance bus structures such as VME, Multibus II, the IBM PC and Q-bus, Dattricon's ILAN (available 4Q84) will use a multidrop RS-422 with up to 32 nodes per network. Twisted pair wiring keeps connection costs reasonable and bit rates up to 180K baud allow networks to cover up to a mile.

The network uses a token-passing collision-avoidance technique and automatically configures on power-up. Individual nodes can power-up or down without affecting the systems which automatically re-initialize themselves.

One other network the system designer may be able to take advantage of is the Intel Bitbus (*Digital Design*, February 1984, p. 72). A serial bus architecture, it was developed to allow the construction of real time distributed control systems. Bitbus modules are available in the iSBX format that may plug directly into STD cards designed to accept them.

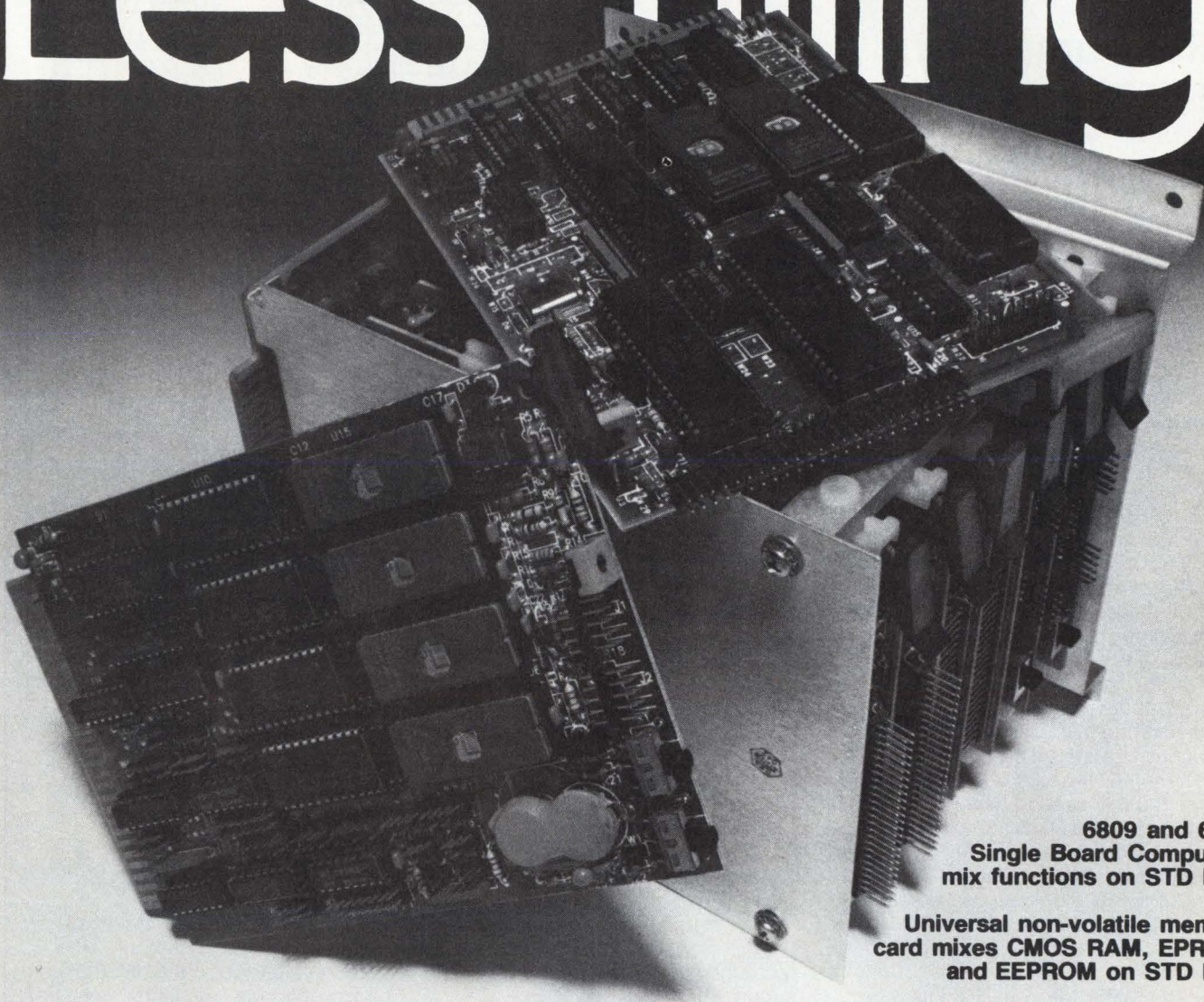
Enhancing the compatibility between the STD and other bus structures may destroy arguments from those who feel that the industrial market will follow the commercial marketplace away from 8-bit to only 16-bit and 32-bit systems.

### IBM PC Threat

One real threat to the future of the STD bus may not be more expensive bus structures, such as the VME, but the IBM PC. The rampant success of the PC in the market has led to its use in a wide variety of environments it was not primarily designed for. Today, so much third party hardware and software is available for the machine that it is possible to configure a PC into applications ranging from image processing and logic analysis to schematic capture. The problem for the PC manufac-



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# Real Time Clock For The STD Bus

A real time clock is a useful addition to any computer system, providing a time stamp for files and interval timing for many applications programs. National Semiconductor Corp. (Santa Clara, CA) has recently introduced a microprocessor compatible real time clock circuit, the MM58167, which is available in a 24-pin dual-in-line (DIP) package. This circuit provides timing functions from thousandths of seconds to months and occupies 32 consecutive I/O or memory locations.

Figure 1 shows an interface for the MM58167 to the STD bus via the Pro-Log (Monterey, CA) 7904 decoded I/O utility card. The 7904 card is a convenient vehicle for putting the MM58167 on the STD bus since it contains the necessary buffer and decoder circuitry, and it has a large breadboard area.

In the circuit, U1 and U2, the 74LS244 bus buffers on the 7904, route the data lines of the MM58167 to the input and output data lines of the STD bus. Circuit U3, the 74LS42 card select decoder on the 7905, is used to decode the base address for the MM58167 and combines this decoded address with the STD IORQ signal to generate CS to select the MM58167. The low order address bits A0-A4 are tied directly to the MM58167, as are the read (RD) and write (WR) lines.

The MM58167 would be a slow peripheral in many systems, so a WAITRQ signal is generated at STD pin 45 by the 7405 open collector buffer. This wait signal is derived from the ready signal which is available at pin four of the MM58167. The additional circuitry in Figure 1 is designed to place the MM58167 in a power-down mode when the +5 V bus power is removed and provide battery back-up of the clock: The nickel-cadmium cells are continually

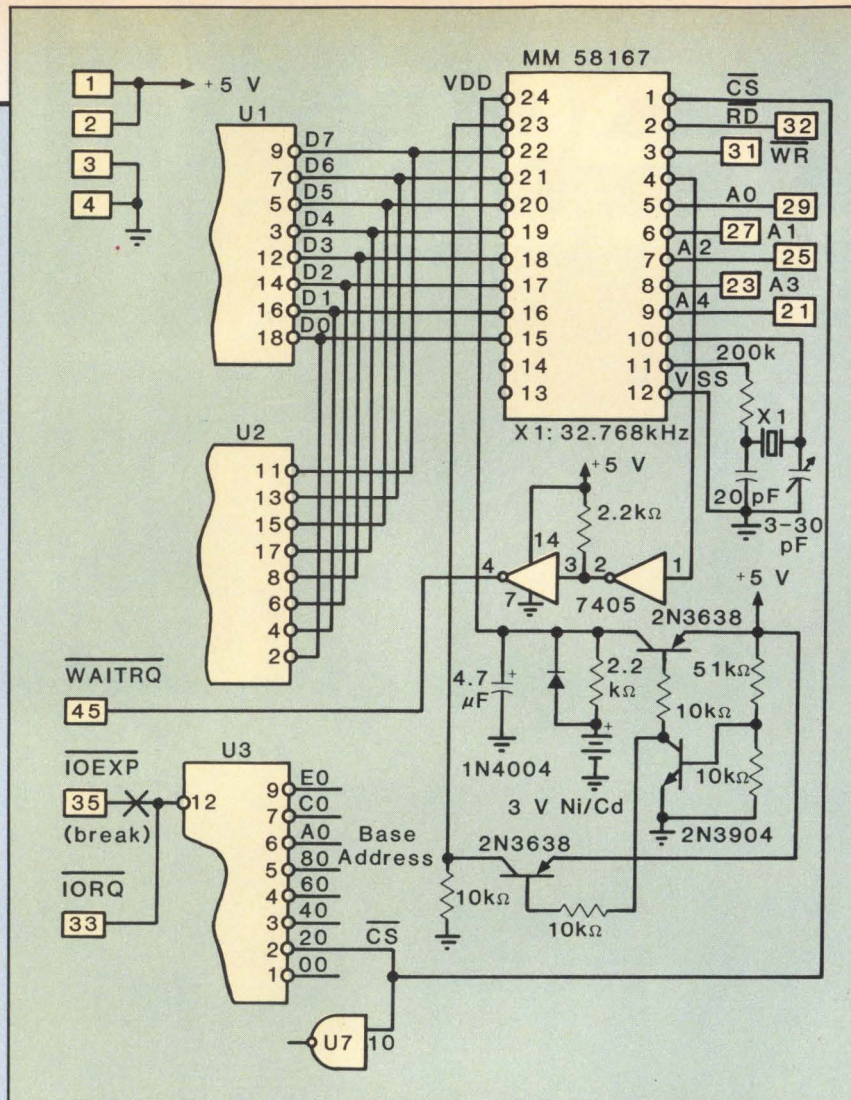


Figure 1: An interface for the MM58167 to the STD bus via the Pro-Log 7904 card.

recharged from the STD bus +5 V supply when the power is on.

Circuits U4-6 on the 7904 (all 74LS42) are not used. The circuitry requires the 7904 jumpers SX, SY, and C to be open, and jumpers A and B to be closed. Furthermore, the connection to STD pin 35 (IOEXP) must be cut, allowing STD pin 13 (IORQ) to be connected to pin 12 of U3 in its place. Pin two of U3 is tied to pin 10 of U7 to enable the bus buffers on read and write when the card is selected.

The programming of the MM58167 can be learned from the data sheets. For testing purposes, however, the registers BASE+2, BASE+3, and BASE+4 contain the data for seconds, minutes, and hours as packed BCD digits. Writing these registers will set the time, and reading from them will get the time.

**Write 300**

*D.M. Gualtieri,  
Allied Corporation*

turers to solve is expandability of their devices via a low-cost bus structure. Recognizing this, several vendors now allow STD bus systems to complement the role of the PC. An STD bus I/O subsystem, for example, can be used to monitor and control industrial interfaces, or collect and preprocess data for communications to the PC. The PC can be used to save, process, display or print data using existing operating and application software.

The PC requires a single RS-232C serial asynchronous

communications port and software to upload or download data files through the serial port. The IBM PC, for example offers an optional RS-232C port and asynchronous communications software. The STD bus requires a CPU card with a serial port, such as the Pro-Log model 7806 and the necessary I/O function cards. The user writes the I/O handling routines for the STD bus CPU including any data preprocessing desired.

Linking the PC to the STD bus via a serial port provides an expensive distributed processing environment with a high



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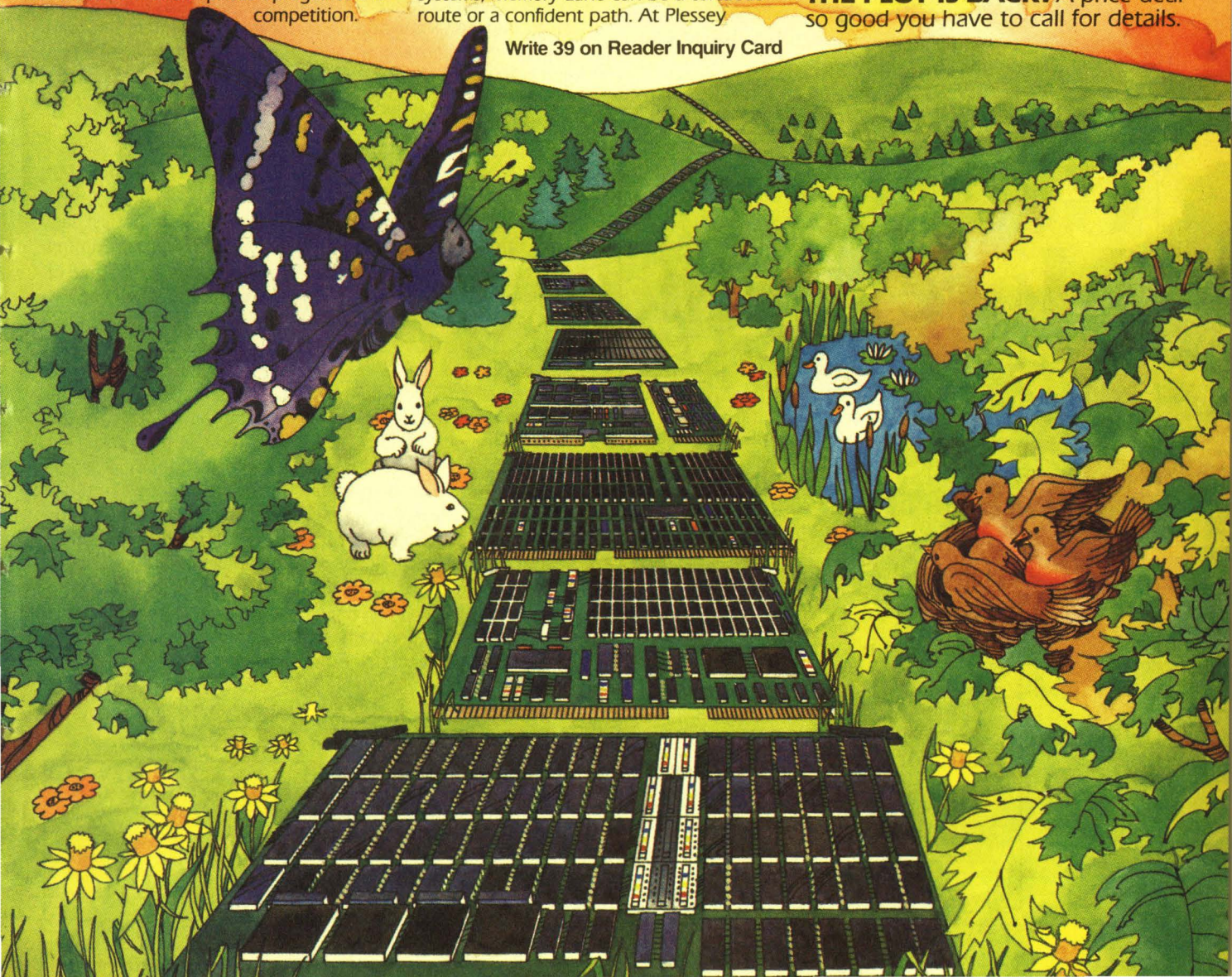
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degree of violation. The PC can be kept on-line for processing while hardware or software changes are being made to the STD bus I/O subsystems. This is facilitated by two Ziatech designed programs: PC/STD 88 and DBUG 88. PC/STD88, residing on the PC, structures the object code file output from the PC language modules for the target STD-8088 system. It handles memory address positioning, links each module to related routines and formats the files for loading. Then, in cooperation with the DBUG 88 program, the code is downloaded for testing. DBUG 88, physically located in PROM on the STD-8088 processor, relays the code into the requested memory space.

The DBUG monitor operates transparently through the PC making it appear that the user is directly connected to the monitor. DBUG 88 can also be operated by connecting a terminal to an STD-8088 serial port. The debugging capabilities of DBUG 88 include examination of the internal registers of the 8088 and optional 8087 co-processor. From the PC keyboard, the user can perform I/O operations, set breakpoints and examine and alter memory in the target system.

IBM PC and XT users can now also link their machines to ProLog's M980 and M910A PROM programmers. All that is required, along with the PC and PC/DOS operating systems and an M980 or M910A with a communications adapter, is an RS-232C cable for asynchronous connection and software to download data in Intel's hex format. Details of the process are available in a Pro-Log application note #139 which may be obtained from the company.

# Get More Data

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## Software Support

Choice of operating system and application software is an important consideration for the systems integrator. Most 8-bit STD applications are implemented without a target operating system due to their single task nature. The 8088, however, is a candidate for a run time operating system. Without one, implementation of complex applications will take longer and the user will run the risk of incurring difficult debugging problems. The application has a direct bearing on the choice of a target operating system. If the system's activity is primarily interrupt driven, requires multiple programs to handle random and possibly overlapping events, or both, a real time operating system will be extremely useful.

Machine control applications are easier to implement with a real time multi-tasking operating system because it provides the ability to develop and schedule independent programs. With the capability of interleaving execution based on priorities (i.e. iRMX86), the user can sense and respond to events in a simplified fashion without inventing his own interrupt control and task suspension routines. On the other hand, interactive processes like digital board test and design graphics are better served with single task operating systems like MS/DOS or CP/M.

The chosen language for the application must fit within the given budgeting constraints for both development and end application. Control applications typically require detailed bit manipulation and speed. Here, low-level languages such as assembly, PLM and C are used. Assemblers are available from both Microsoft and Digital Research.

When the main requirement is computationally intensive, a language such as FORTRAN or Pascal provides simple but powerful numerics, iterating, array handling and data typing. Applications that are continually changing, like simple test data acquisition are well served by BASIC's ease of programming even at the expense of execution speed and code size. Some of the newer compilers, such as those available for the IBM PC tend to be suitable for these areas.

## Conclusion

The use of the STD bus has grown at a rapid rate in terms of new users, new manufacturers and product innovations. Today, there are 900 announced STD bus board products from over 100 manufacturers. When looking for a board supplier, it is advisable to research the track record of the vendor carefully. Smaller businesses can fail and leave the systems integrator without a source. Software support from the vendor is another critical consideration. Some smaller companies without larger resources may simply offer the hardware and leave the whole software/integration procedure to the systems integrator. On the other hand, larger companies may not only offer software but can offer the integrator some assistance through technical marketing and development aids. □

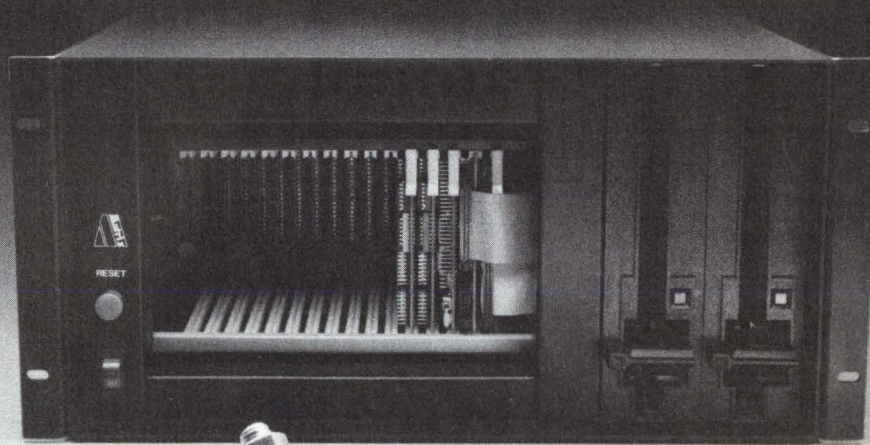
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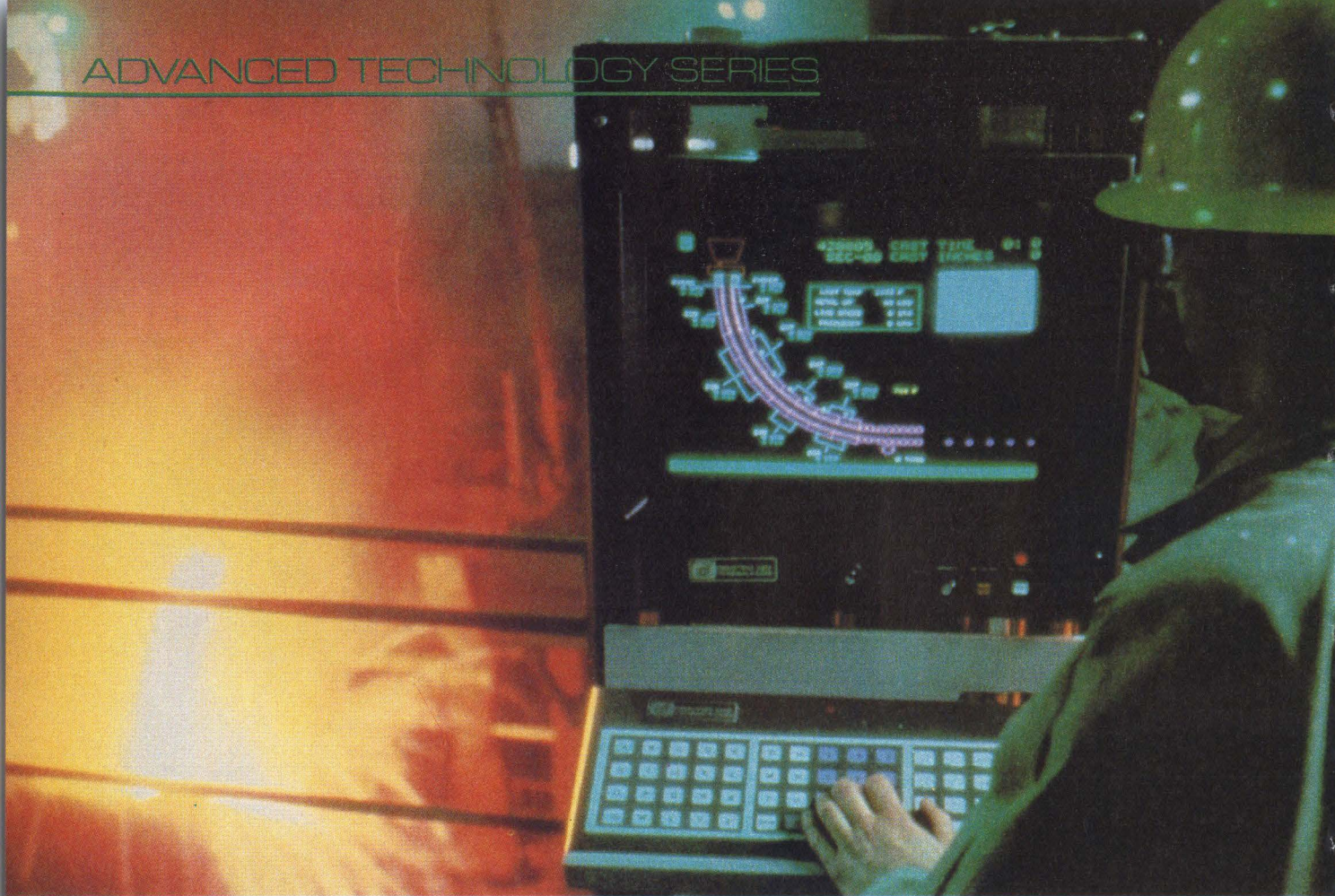


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# Process Control: Intelligence Moves To The Factory Floor

by Julie Pingry, Senior Editor

Computing in the industrial environment has, until fairly recently, meant inputting data hand-delivered from the factory floor to a control room. Programmable controllers for manufacturing automation are highly disguised and not very sophisticated computers. Computer systems at the corporate level have not been closely linked to the factory control room. All that is changing rapidly, with intelligence and undisguised computers moving throughout manufacturing plants.

The impetus: competition for industrial market share has heated up for US companies. To compete with low labor costs and huge production volumes of offshore industries, they are finally looking to digital computing technologies for

help. To optimize operations from the top, corporate computing and process information systems are communicating.

Though this will provide huge new markets for digital equipment manufacturers and systems integrators, entry will not be easy. Not only must devices be protected from harsh environments and untrained users, but the clout of traditional control and instrumentation suppliers must be considered.

One of the big industrial suppliers, Honeywell (Phoenix, AZ), introduced the TDC 3000 process management system last fall. They pointed out that new systems must "enable interchange of data between process control and other previously separate but related plant functions." Such turnkey suppliers will work to maintain their market share by expand-

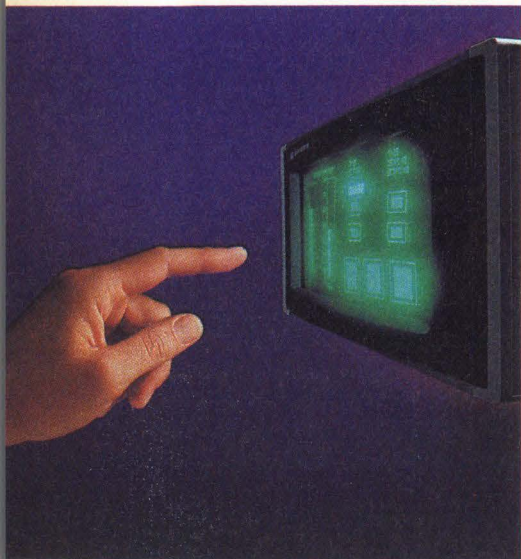
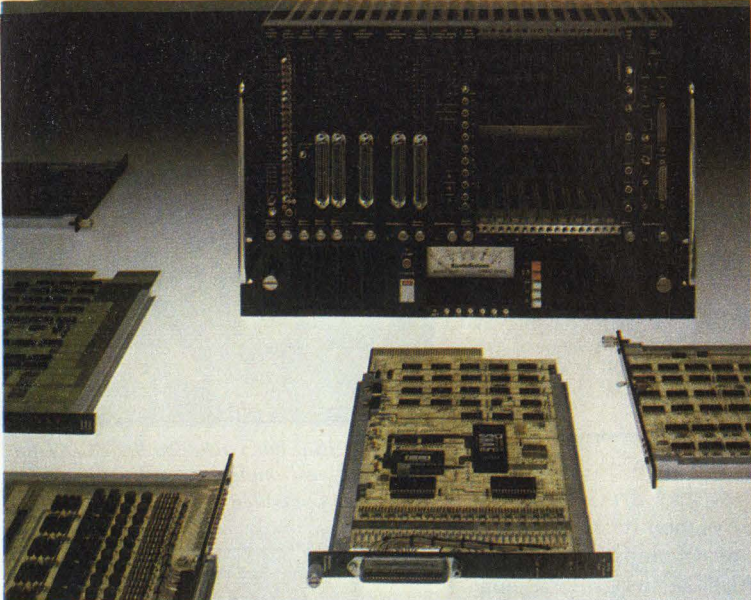


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## Competition for industrial market share has heated up for US companies, and they are finally looking to digital computing technology for help.

ing product lines partly through OEM agreements.

Main points to remember when designing for factory applications are: IBM has already hit the market, and for "area computers", compatibility may be key; environmental hazards include dirt, temperature extremes, vibration, noisy equipment and, not least, the users; interface is to operators often without computer training and, at the other end, to analog monitoring equipment, not other digital systems.

Some of the products that may best address these needs are microcomputers to manage information while programmable controllers control the process; advanced CMOS semiconductor technologies, for powerful computer chips in totally sealed enclosures; interactive color graphics displays for an understandable user interface and token passing local area networks for tying all areas of a shop together. All of these will work in conjunction with traditional process and factory control instruments.

### Microcomputers Move In

One driving force in the distribution of intelligence to the plant is the bottom line figures viewed by the top management. Those with access to corporate computing/MIS are now interested in complete factory operations and management information. As the major supplier of MIS systems, IBM realizes that need; their Industrial Systems Division (Boca Raton, FL) is developing many systems tailored to factory use. At the Programmable Controllers show this spring, they introduced an industrial version of the PC/XT, the 5531 (**Figure 1**), for use in the plant.

Essentially, the 5531 has only different packaging from the PC/XT, providing it complete XT software and hardware compatibility. The IBM 5531 with a keyboard, 128K memory, a single floppy and a 10 Mbyte fixed hard drive and ports for a color graphics monitor, asynchronous

communications and a printer costs \$6,740. Because of their relatively small cost and size, microcomputers will find their way into manufacturing information management.

The 8088 is used to power other industrial terminals as well. Eagle-Picher Akron Standard's (Akron, OH) FacTer 8300 and 8400 terminals are totally sealed, with integral 12" monitors and keyboards (**Figure 2**). ISI International (Sunnyvale, CA) use the 8088 for IBM PC and XT compatibility in their 6160 Industrial Computer. The system is rack-mountable and has a socket for the 8087 math co-processor.

Even GE (Norwalk, CT) has based their Workmaster Programmable Control Information Center on an IBM PC—the portable. This system (**Figure 3**), optimized for size constraints, uses a 9" screen, 3½" hard-case floppy diskettes, and weighs 32 lbs. GE also uses terminals from NemaTron Corp. (Ann Arbor, MI). NTC offer their own industrial terminal, the IWS-100, for flush panel-mounting. With a Z80 processor, 12" screen, flat membrane keyboard and ANSI-compatibility, this system costs \$1,690 list and \$1,175 OEM.

Software for industrial use of the IBM PC has been introduced as well. A hardware/software product called Factory Calc has support from several major programmable controller firms, though the originator, MISA Corp. (Milford, OH), is a start-up. FactoryCalc is a VisiCalc-compatible spreadsheet package with an 8085-based Information Manager to interface to the IBM PC.

Heuristics (Sacramento, CA) has had similar success in working with major control manufacturers on their Onspec personal computer software package. The modular package for the IBM PC, Sage or PC-compatible, communicates with controllers and instrumentation from about a dozen big names. Historical and trend data, as well as alarms, real

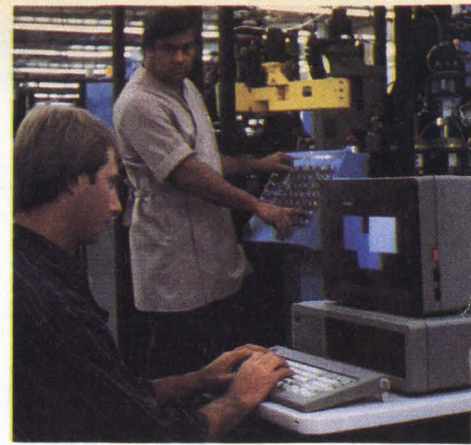


Figure 1: IBM has packaged the PC/XT for industrial environments to make their 5531 Industrial Computer.

time status and output to instrumentation are part of the \$2,450 Onspec program.

A key feature of these systems is that they run without user programming for analysis of the information generated in manufacturing. Another company providing that is Cyborg Corp. (Newton, MA), whose ISAAC (Integrated System for Automated Acquisition and Control) family is based on IBM or Apple personal computers. ISAACs are designed for data acquisition, as their name implies. Cyborg offers several I/O boards for sensitive A/D and D/A needs of laboratory and process control applications.

One traditional feature of control equipment is IEEE-488 GPIB bus compatibility, and National Instruments (Austin, TX) has given that to the IBM PC, too. These packages allow an IBM PC to run control routines. Two versions, one with high-level commands only, is for end-users, and an OEM version can mix those with primitives.

How large a dent such microcomputer process control products will make is a question, however. As MISA President Walter Schoellmann points out, the main role of personal computers in factory automation will not be process control, but management of the information generated by a process. As area computers collecting data from a group of factory instrumentation, the PC will be pervasive.

Industrial managers are interested in utilizing available computing technology to stay competitive. Evidence of this trend is a new consulting company to address strategies for industrial revitalization, Harbor Research (Cambridge, MA). Glen Allmendinger, President of Harbor, succinctly says: personal computers will be the gateway between corporate MIS and factory management.



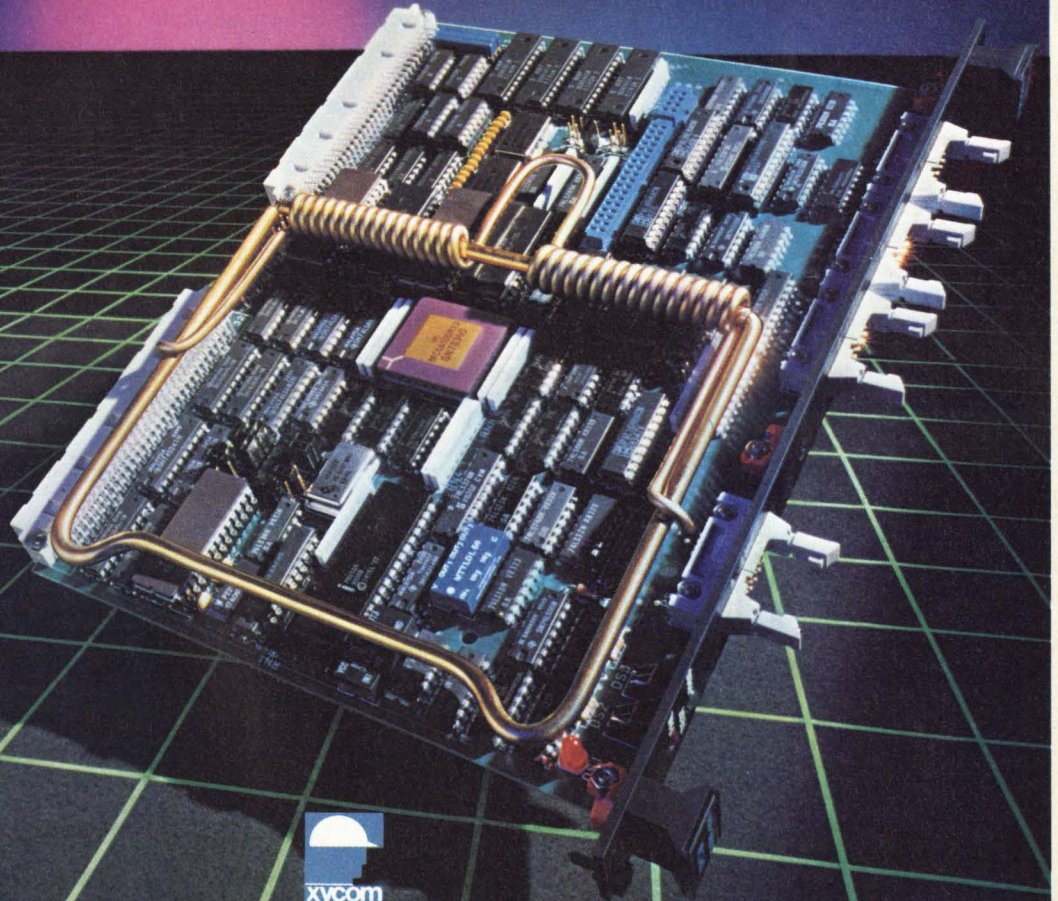
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## Industrial Environment Constraints

One of the most obvious differences between industrial and most other applications is the physical environment. Hazard from dirt, dust, high temperatures, chemicals, vibration or shock may need to be accounted for in equipment design.

Equipment for process control has long been made to NEMA standards to allow operation in factories. Totally sealed enclosures are an advantage for devices that could serve a wide range of industrial markets. Membrane keyboards have taken hold for this reason, as have membrane-based touch panels, like the 1780 (Figure 4) from John Fluke Manufacturing (Everett, WA).

High temperatures and total enclosure are difficulties for magnetic memory peripherals, as well. Some companies are working at widening disk and tape drive operating temperature ranges, but most drives are still not reliable under factory conditions. Industrial Data Terminals (IDT) (Westerville, OH) uses bubble memory to circumvent some of those problems (*Digital Design*, July, 1984). Fluke offers bubble as an option, so for dusty use, floppies are only needed for initial booting. Bubble memory module supplier Targa (Ottawa, Canada) sees industrial computing equipment as a prime market.

The electrical noise generated by manufacturing machinery can be another problem. Cables need good shielding, and enclosures need to be EMI-resistant. Some communication problems in extremely noisy environments can be solved by fiber optic links. Companies like Anaconda-Ericsson (Overland Park, KS), Valtec (West Boylston, MA) and EOTec (West Haven, CT) supply links for such purposes, and the traditional connector/hardware maker Molex (Lisle, IL) has introduced a fiber optic link.

In addition to protection against the physical environment, equipment needs to be shielded from inexperienced computer users. Some of the users of equipment on a factory floor are familiar with operating only knobs and switches. In addition, their hands may be dirtier than the environment at large.

The suppliers of control and industrial equipment have experience in ruggedizing. Studying their packaging could be worthwhile. Another possibility is to OEM to the large firms such as Allen-Bradley, GE, Honeywell, Gould and Sie-

Figure 2: Integral display screen and membrane keyboard with letters in alphabetic order make Eagle-Picher's FacTer terminals well-suited to the industrial environment.



mens and let them package devices as part of their systems. The latter scheme could also lend help to market acceptance of the product.

## VLSI, Bus Choices For The Factory

Ideally, the digital intelligence invading everyday products can be integrated into many instruments and controls on the plant floor. This will require not only very small size devices, but also sealed enclosures with little or no extra room needed for cooling. The heat dissipation of high density computing circuitry has made sealing virtually impossible.

Various IC houses have developed CMOS processes that promise high speed for computing with little enough heat dissipation for sealed, uncooled use. The noise immunity of CMOS ICs is also an advantage for industrial systems. The ad-

vent of dense, low-power VLSI circuitry could revolutionize the factory floor.

Controlling a process, unlike processing data, requires ongoing response to real-world analog signals. To optimize a manufacturing process, data must move rapidly; here, 32-bit processors will be useful. Some 32-bit machines are available, soon at only a small cost premium over 16-bit machines. But they may not storm the market because there are few bus structures that support 32-bit processing.

Currently, the VME bus is gaining ground for high performance. Xycom (Saline, MI) has committed energy to the VME, seeing that it has a small form factor and is easily ruggedized. By using intelligent I/O cards, processing power is distributed.

Traditionally, the STD bus has been popular for industry. Micro-Link (Car-

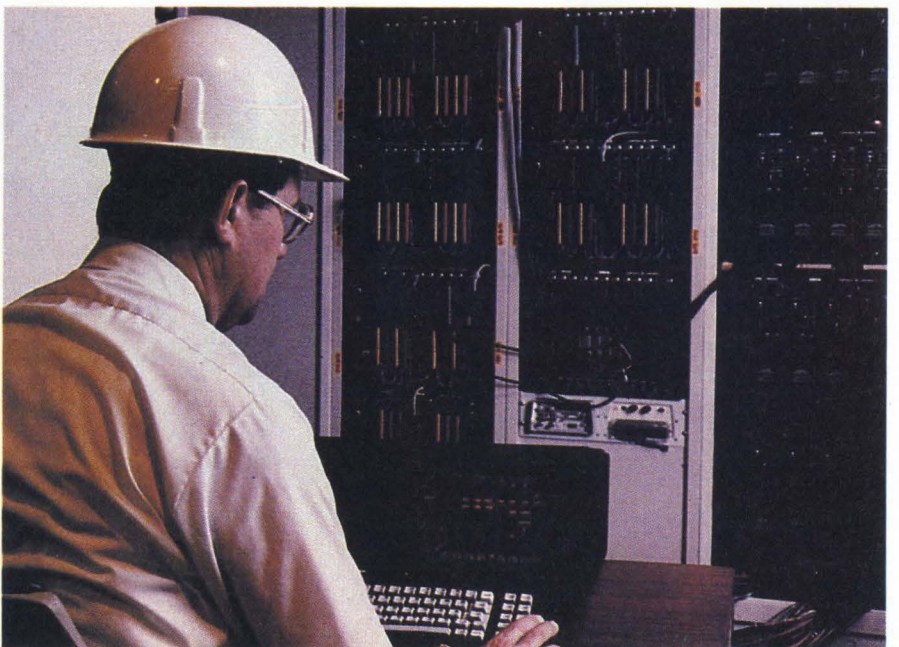


Figure 3: GE (Norwalk, CT) has based their WorkMaster on IBM's portable computer; it uses 3 1/2" diskettes.



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## Simulation Of Automated Factory Allows Optimized Designs

One of the largest deterrents to automating an industrial plant is the capital investment in an untried system. Every control application is different; factories may vary in size and require equipment in unique configurations. One system, from HEI, Inc. (Carol Stream, IL) addresses these factors by simulating industrial equipment, emulating software for the control computers and animating potential scenarios. Designers can show management how the automation of a plant would function before installation.

The HEI product includes software emulation for debugging and simulation of industrial hardware. This simulation includes the movement of materials and operation of instruments and programmable controllers on the factory floor.

The RTCS (Real Time Computer Simulator) takes the place of factory floor equipment and hooks up to a programmable controller and a host computer (Figure 1). The parameters of an automation system, such as placement, timing and functions of equipment, are input to a table in the IBM PC or compatible host. Different equipment designs can be tried by manipulating these parameters. The programmable controller executes software as if it were operating the factory system rather than the RTCS. A color character graphics display



Figure 1: RTCS on the right is testing a control program running on the Allen-Bradley PLC-3 programmable controller.

(Figure 2) shows activity in real time, as it would happen in the plant, as well as the programmable controller inputs and outputs.

The HEI system can act as a diagnostic station after the optimized equipment is installed. The investment in the simulation system can then be absorbed over the lifetime of the plant.

Two configurations of the RTCS are available. The 250-A has two 8086 16-bit processors and 128K model memory and the 250-B uses three processors and 256K model memory. The -B handles processes as fast as 50 msec, and the -A, 100 msec minimum. Both are Multibus-based, with 256K of main system memory and a serial interface to Allen-Bradley and Modicon controllers. They include a color graphics monitor and an operator CRT console. The 250-B also directly interfaces via Opto-22 or Texas Instruments I/O modules.

This system is especially useful in demonstrating possibilities before equipment installation. Simulation packages are available for industrial plants, but inclusion of software emulation and graphics animation allow for fuller analysis of factory operation for system optimization.

Write 301

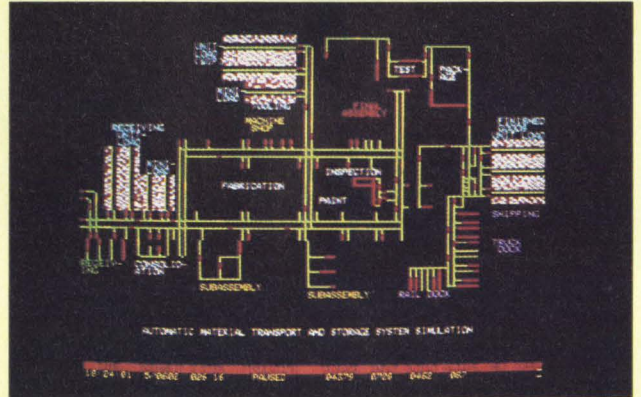


Figure 2: Operation of an integrated manufacturing facility is shown on the color display. The simulation includes automatic storage and retrieval, conveyor and wire-guided vehicles.

mel, IN) and Contemporary Control Systems (Downers Grove, IL) offer a wide range of systems and I/O and control cards to the STD bus form factor. The boards are small, and the bus allows for prioritized interrupts. Both these are bonuses for industrial systems.

Texas Instruments (Johnson City, TN), has their own bus, the TM990. Their own 99000 and 99105 processors for the bus have a communications register unit (CRU) that allows single-bit addressing for I/O. Also critical for control applications is the interrupt-handling of these CPUs; 15 maskable vectored prioritized

hardware interrupts are allowed.

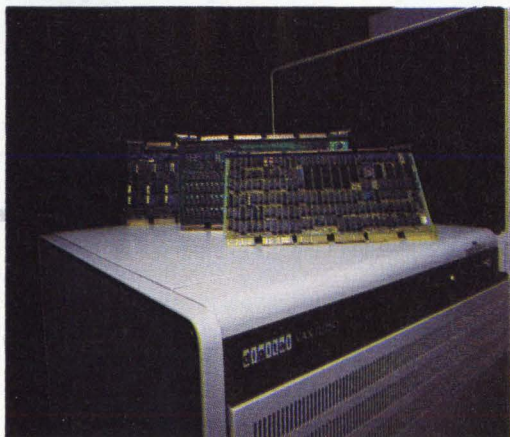
Building around CMOS parts allows sealed-enclosure industrial systems on National Semiconductor's (Santa Clara, CA) CIMbus (CMOS Industrial Microcomputer). A power bus allows power down on everything but clock and memory, for low power consumption during sampling I/O. Like the VME, CIMbus uses the Eurocard form factor with its small card size and corrosion- and vibration-resistant connectors. National says the bus is being expanded to support 16-bit CMOS ICs as well as their 8-bit NSC800 CPU.

Specifically tailored to industrial applications are the GPIB/HPIB and CAMAC buses. These are rarely seen in general purpose computing systems, but are suited to test and control systems. When peripheral I/O, ASCII and teletype connections became inadequate for computer-to-instrumentation connection about 10 years ago, these two standards caught on quickly.

The HPIB (Hewlett-Packard Interface Bus), standardized as the GPIB or IEEE-488, is for relatively simple monitoring and data acquisition. Basic to this scheme are talkers, or devices such as counters



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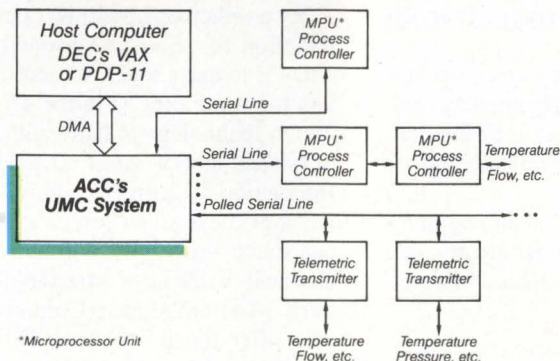
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\*Microprocessor Unit

Typical configuration locates the UMC controller between a DEC computer and process control lines.



**Advanced Computer  
Communications**

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and timers that only transmit on request, and listeners, such as printers and recording devices that simply take input. Other devices on the bus can do both, as talker/listeners and controllers. Simplicity of the bus hardware and the command structure keep costs relatively low for the GPIB.

IEEE-595 CAMAC, the other industrial bus, is for larger installations. Card cages on this bus, called crates, can each hold up to 23 process modules (**Figure 5**). As many as 62 crates are connected by a serial or parallel data highway with redundant paths. KineticSystems (Lockport, IL) has long offered CAMAC crates, modules and crate controllers. Now, they have interfaces for the IBM, DEC Professional and Apple personal computers to act as an interface for I/O to office.

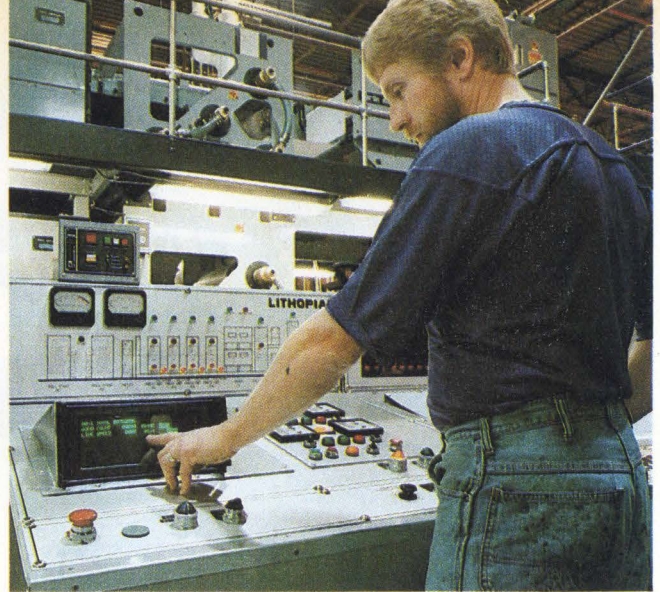
Traditional industrial bus architectures are contending more frequently with powerful commercial bus structures. For any bus on the factory floor, interrupt handling, small form factor and soon, power and speed to accommodate 32-bit processing are critical.

**Interfacing To Process, Operator**

Computers in an industrial environment are connecting to different sources of incoming data and to another sort of user than those in MIS or laboratory situations. A continuous process is often automated to keep it within stricter limits. This means continuous analog feedback from the process and the ability to respond to out of bounds conditions.

Turnkey suppliers of control systems

*Figure 4: John Fluke Manufacturing offers a small touch panel for user interface to their range of industrial controls and instrumentation; the technology for the 1780 has tactile feel and is easily cleaned.*



have long interfaced instrumentation to computers. But for increasingly tight control, a process should be controlled at the site. Along with Burr-Brown (Tucson, AZ), Datel-Intersil (Mansfield, MA) and others, Analog Devices (Norwood, MA) has been a leader in A/D and D/A conversion devices. An 8-bit A/D chip that provides a transducer to microprocessor interface including amplifier-buffering is one of their products. Analog Devices may announce low power analog components soon, as well.

A large contingent in the control industry is making computer front-ends. John Fluke offers the 2400 and Acurex (Mountain View, CA), the Autolink to offload the computer from data acquisition. Factory data collection systems like those from Honeywell (Minneapolis, MN) and hand-held versions like those from Fluke and from Innovative Electronics (Miami, FL) also provide collection functions.

A key element of the interface to the process is multi-tasking and efficient I/O handling. S&H Computer Systems' (Nashville, TN) TSX-Plus for LSI-II systems uses caching for faster I/O access and 18-bit DMA.

At the other end, the factory worker/user may be an even bigger interface challenge. Most of the operators on the floor have no training on a computer, and are somewhat afraid.

Great improvements in an operator's ability to control a process are possible with interactive color graphics, however.

With products such as Industrial Data Terminals' (Westerville, OH) Screenmax, color graphics to show what is happening with a process and setpoints for high and low boundaries (**Figure 6**) are easily developed. Configuring a display to match the actual manufacturing process is critical, since every industrial setup is different and subject to change. USData (Richardson, TX) also makes extensive use of color graphics for the user interface.

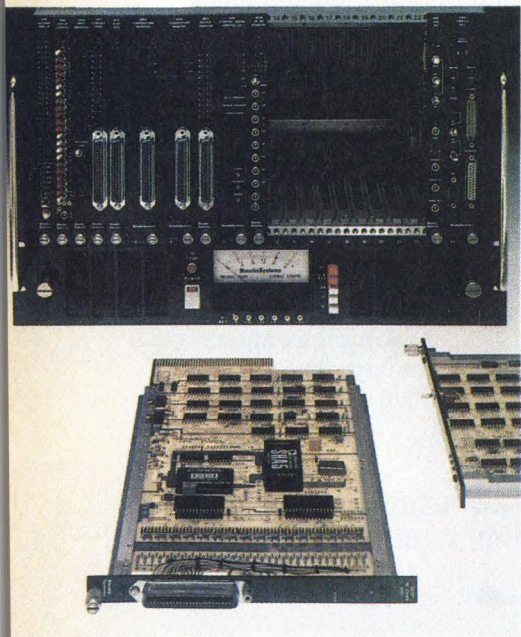
This configurability to fit the application has also extended to the keyboard for USData. The Flexus keyboard kit (**Figure 7**) allows as many as 155 keys to be placed wherever they are logical for a particular operation and operator. Unlike data entry, most control applications only require a few keys to perform necessary input and manipulations.

Most keyboards will not be used for text entry in the factory, and those using the terminal equipment generally are not typists by training. Several manufacturers have introduced products with keys in alphabetical order (**Figure 2**), to make them easier for a non-typist to find.

Yet another way to allow operator interaction for those not trained in data entry is to use a touch screen, as Fluke has for some time (**Figure 4**). Carroll Touch Technology (Champaign, IL) has developed special Industrial Touch Units. Interaction Systems (Newtonville, MA) has a gridless touch screen system that has touch sensitivity without any mechanical workings. Microtouch (Woburn, MA) and Autech (Columbus, OH) also offer touch sensitive display and retrofit products.

Voice input and synthesis may be useful for the factory, too. When an operator needs to move about, freedom from the panel could be an advantage. However,

*Figure 5: 25-slot CAMAC crates and modules such as these from KineticSystems allow large numbers of instruments to be connected for process control and data acquisition.*





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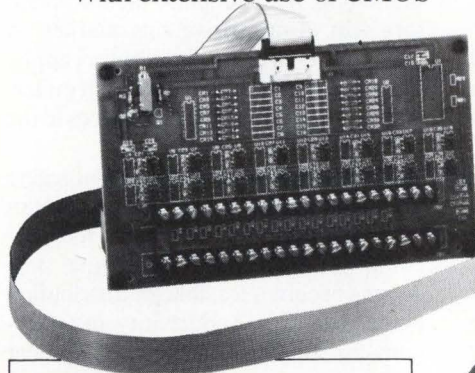
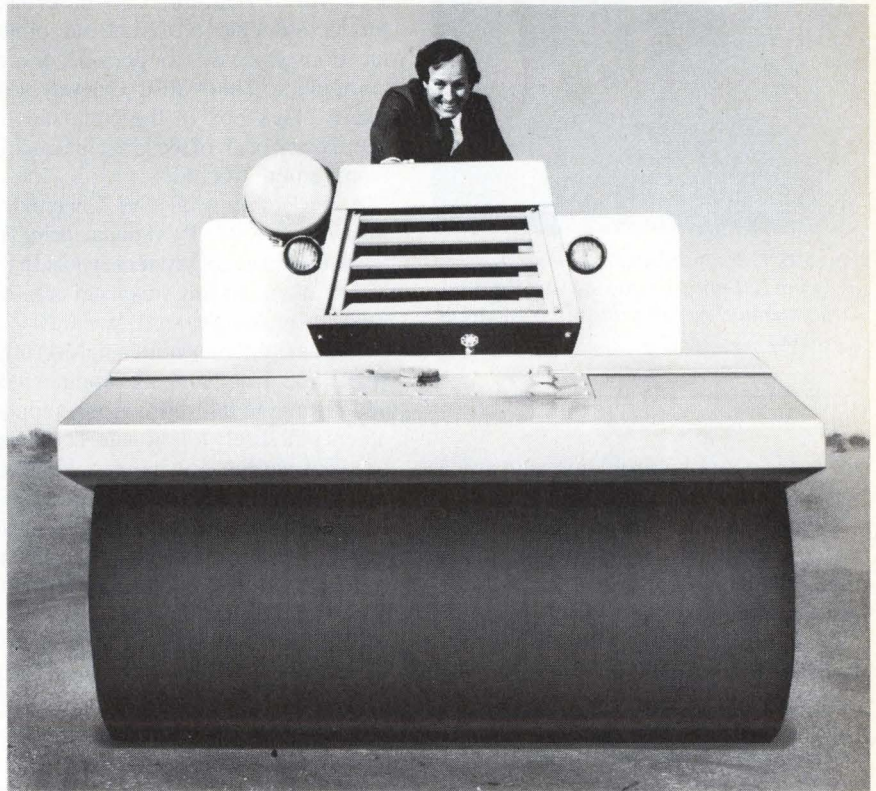
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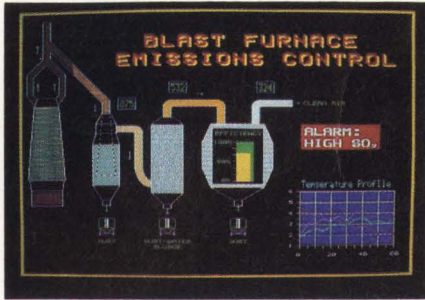


Figure 6: Color graphics displays such as this one from IDT not only provide visual alarms to the operator, they show the whole picture of a process.

there are potential problems with voice interaction.

Besides making an interface that does not intimidate the user, alarm and warning methods are important. In the event of a parameter setpoint being violated, the operator must be alerted in a timely fashion. But in many instances, not the operator, but a supervisor, should have final control. Therefore, some form of access codes or override from another location are desirable.

Providing useful information to the user on the plant floor without intimidation is tricky. Most users are accustomed to seeing dials, gauges and buttons on the control panel of industrial equipment. Some graphics displays simply reproduce that look and allow buttons either on a keyboard or on a touch-sensitive screen to act as mechanical human interfaces.

### Factory Communications

With more powerful equipment in the factory, the need for sophisticated communications has grown. There are many levels of communications needed: between intelligent equipment and the instruments at the process; plant-wide networking; and between the manufacturing facility and the corporate MIS equipment.

For the smaller area, the control equipment manufacturers probably are developing the best solutions. From Honeywell to Texas Instruments to Allen-Bradley, local "data highways" and other links are designed for the application. And new versions of most of these systems are on the way or recently announced.

Since intelligent remote units can process much of the incoming data before sending it to a central control computer, high bandwidth communications may not

be critical. Assured, constant transmission is more important. Companies like ETI Micro (Dublin, CA) have based product strategies on a front-end communications processor for personal or other computers. Their 8691 Gateway looks like a black box to the computer and keeps track of all of the latest information from remote I/O units.

At the facility-wide level, General Motors with their MAP (Manufacturing Automation Protocol) system and its IEEE-802.4 token passing bus local area network are pushing toward standards. Concord Data Systems (Waltham, MA) offers IEEE 802.4 networking products now, and with GM and user group support, others will surely follow suit. The benefit of token passing for industrial applications is the assured access for decisive processes. Access is assured because a logical token, or possibility to transmit, is given in turn to each node; no device must wait because of collisions.

IBM also supports the 802.4 standards for industrial communications. Though the token passing ring is their choice for office LANs, they, like GM, see a bus topology for the factory. The physical bus is a broadband cable, which many facilities already have installed for CCTV monitoring, attendance, surveillance and machine vision. With the backing of such giants, the token passing bus will no doubt be standard for installations in industry needing local area networking.

For interconnection with office networks, gateways can be used. Once higher-level protocols have been standardized for networks, whether to the NBS, TCP/IP or Xerox XNS, various network methodologies and bus access and data format methods will be able to interact easily as one. Gateways to the major control manufacturers' dataways will also be critical.

### Conclusion

System integration for the industrial market has many battles to fight. But at long last, the resistance to automating and to using other than traditional process vendors' equipment is waning. Still, computing equipment will not replace the control devices; designs must accommodate programmable controllers, ladder logic and huge quantities of I/O.

Industrial automation will no longer take place in isolated, separate units. CAD workstations that are not linked to engineering or manufacturing equipment are a familiar example of "islands of auto-



Figure 7: Processes being controlled are generally unique, and this Flexus keyboard kit from USData provides total user configurability of 155 keys; even the legends on the keycaps are chosen or created by the system designer.

mation" that are being linked into a larger picture now. Similarly, remote instrumentation, controllers and area computers will all connect and also be closely linked to corporate computing.

Microcomputers, especially the IBM lines, will invade as intelligent gateways between the office and the factory. PC software tailored to the process environment will be in high demand.

New silicon processes that yield high-performance ICs that generate very little heat could radically change the face of industrial automation. With opportunities to fully enclose intelligence for relatively low costs and almost no space, an increasing number of instruments will incorporate computers.

Harsh environments and non-programming, non-computer-literate operators will always drive this market. A different set of ergonomic factors apply. Creating rugged equipment with understandable, configurable interfaces to the user is of prime importance.

Traditional controllers, dataloggers and instrumentation will continue to populate the factory floor. But as they become more intelligent and digital processing becomes feasible for distribution to these devices, opportunity and problems for suppliers of digital equipment will increase.

In this old field, names and reliability are important; look for control vendors to OEM much of the needed software and hardware to improve their products. Even IBM products are now incorporated into the systems of several major control suppliers. Perhaps the more experienced industrial suppliers can best configure highly application-specific systems for process control. □

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# Development Tools Take Aim At 32-Bit Chips

by Ronald Collett,  
Technical Editor

Although much has been published about the extended capabilities of 32-bit microprocessors, the market still belongs to the 8- and 16-bit chips. For most current applications, 32-bit horsepower is seen as overkill and is not expected to immediately shake up the industry.

The arrival of full 32-bit microprocessors from National Semiconductor and Motorola has set the stage for a deluge of third party support tools. Most vendors, however, are hedging their bets and not committing to support any particular manufacturer. Instead, watchful eyes are fixed on the National Semiconductor NS32032 and the Motorola MC68020 to see which is more dominant in the marketplace. The expected arrival of Intel's 80386 and Zilog's Z80000 has also added to the suspense. Once the four semiconductor vendors are in head-to-head competition and system integrators have a chance to evaluate the offerings, third party vendors will provide development support.

The prospective user has three main options when purchasing a development system: a dedicated system; a universal system; or an emulator and cross software for a host such as a VAX, PDP-11 or IBM PC. Dedicated systems support the development of one manufacturer's microprocessors, whereas a universal system accommodates almost any microprocessor. In most cases, the major difference between the two systems is the emulators that come with the system. New interface tools also enable some emulators to be tied directly to the host. With this, code can be directly downloaded to the emulator from the host. Otherwise the only choice for in-circuit emulation is to purchase a standalone emulator.

Capabilities of development systems from various manufacturers present the potential user with a range of choices. For instance, some systems include logic analysis, emulation and software development while others provide a limited combination of these capabilities. More specifically, some of the tools found in



Figure 1: The COLT 300 from Dolch can function as either a portable or benchtop development system.

new development systems include in-circuit emulators, cross compilers, cross assemblers, state and timing analyzers, simulators, symbolic debuggers and PROM programmers. Available as separate tools for several years, only recently have manufacturers combined many into one package.

Beyond combining many development tools into a single system, manufacturers have been concentrating on improving software aids. Using a development system can be confusing, so manufacturers have aimed at easing the task. In addition, many new systems use common operating systems based on UNIX, CP/M or



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## For software development tasks, system integrators are shying away from traditional universal and dedicated development systems and opting for general purpose computers.

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PC DOS. With a common operating system users can transport development and application programs between different computers that support that operating system.

For software development, using a general purpose computer such as a VAX has evolved into a dominating trend. With this configuration, system integrators have realized the benefit of having a computer system for not only microprocessor development but VLSI design, logic simulation PCB layout and general CAE tasks. The large host can also act as a central node for networking several development stations together. In response to this trend, many universal and dedicated development system manufacturers have created communication links between their systems and the VAX.

### Universal Systems

Recognizing that many users want to draw on the resources of the VAX, Tektronix (Beaverton, OR) adapted their system's language development system (LANDS) to run on the VAX 11/730, 750 and 780. Tektronix's 8500 Series of microprocessor development systems also allow stand-alone use, so system integrators need not own a VAX. After developing programs on the host, object files can be downloaded to the 8540 integration unit to test and debug software. The 8540 also interfaces to the firm's emulators so engineers can perform software/hardware integration for most 8- and 16-bit microprocessors. In addition, the DAS 9100 Digital Analysis System can be interfaced to both the 8540 and 8560/61 so the same symbols can be used for logic analysis, emulation and software development.

Logic analysis, emulation and software development for most 8- and 16-bit microprocessors is also offered by Hewlett-Packard (Palo Alto, CA). The HP64000 development system can be purchased as either a desktop model or transportable unit. The desktop version offers 10 expansion slots and the transportable

model offers 5 slots. Option cards that fit in these slots include state analysis, timing analysis, high speed emulation and additional emulation memory.

Users can develop software with Pascal and HP offers assemblers for most microprocessors. If the assembler is not available, custom assemblers can be created using the HP definable assembler. HP's software performance analyzer option can significantly aid in optimizing software since it aids in locating software throughput bottlenecks which affect overall performance.

Hewlett-Packard has also recognized that system integrators want to develop software on a VAX. They plan to introduce software tools that run under VMS as well as a high speed link to network their 64000 series development systems to a VAX. Originally scheduled for introduction this month, HP postponed the release until late 1984 or early 1985.

Besides offering a standalone microprocessor development system, Kontron (Redwood City, CA) provides the Emu-

lator Bridge as an interface between their own KSE Series of in-circuit emulators and any of DEC's VAX or PDP-11 computers. As a result, software developed on DEC computer systems can be directly downloaded into the emulator via the Bridge.

For full development capabilities, Kontron's KDS microprocessor development system provides software development capabilities, in-circuit emulation and logic analysis. This system has several configurations. The most powerful, the KDS-968, operates under UNIX, uses a 68000-based CPU and a Z-80 coprocessor for controlling in-circuit emulators, logic analyzers or other peripherals. This system simultaneously supports up to three users: one user has access to software development, logic analysis and emulation while the others can perform only software development. Programs can be developed using Pascal, C or assembly language and an optional Ethernet interface allows multiple KDS-968 units to be networked.

Kontron also offers emulators for most 8- and 16-bit microprocessors and the emulators can be daisy-chained to support up to four microprocessors simultaneously. To complete the development system, the firm offers the KSA series of logic analyzers and a PROM programmer. The logic analyzers provide up to 64 channels with both state and timing analysis at speeds to 100 MHz. The PROM programmer supports up to 400 devices including MOS, CMOS and bipolar, and can be integrated into the development



Figure 2: Kontron's Development Adapter enables an IBM Personal Computer to host their slave emulator subsystem.



## ISE/32: NS32032 In-System Emulator

The ISE/32, National Semiconductor's NS32032 In-System Emulator, is designed to support National's own series 32000 family of microprocessors. It is completely different from its current cousins, the NS32016 and the NS32008. When available early next year, the ISE/32 will be the first ISE to truly emulate a full 32-bit microprocessor.

Used with host systems such as National's SYS32, the ISE/32 will emulate a complete 32000 chip set, including the NS32032 (CPU), the NS32082 Memory Management Unit (MMU), and the NS32201 Timing Control Unit (TCU).

Like the ISE/16, the ISE/32 can either enable or disable the MMU. The ISE/32 will allow users to test and debug both hardware and software in their own 32000-based hardware environment. The user could test and debug only the 32000 software program if a 32000-based hardware system is not available. ISE/32 will operate in either emulation mode, when the ISE/32 is actually running the user's program, or monitor mode, when the ISE/32 is communicating with the user via the host system.

ISE/32 will include an internal clock oscillator for speeds of up to 10 MHz and 12 Kbytes of high-speed dedicated ISE memory for real time emulation. All the features needed to stop emulation to examine and modify CPU registers, slave processor registers, and memory space will also be provided.

The ISE/32 package consists of hardware, the monitor firmware program, and RS-232 cables. A host-dependent debugger program (IDBG32, ISE-DeBuGger for the NS32032) will be available as part of the NS32000 cross software support package. The software portion of the ISE/32 consists of the monitor firmware program which will reside in PROMs on the emulator pod and the IDBG32 program which resides in the host system. IDBG32 is a high-level user-friendly debugger program, much like the IDBG16 for the ISE/16. For ISE/32, IDBG32 will support multiprocessing environments, 32-bit processors, 32-bit data paths, and various hardware enhancements.

ISE/32 will have four 76-bit hardware breakpoints. The user can set a break to occur on address (25 bits), data (32 bits), status (11 bits) and/or external (8 bits via the TTL Status Pod)

conditions. Breakpoints can be used either combinationally or sequentially (e.g., A or B, B before C, etc.). As in the ISE/16, the ISE/32 will support a breakrange independent of these breakpoints to allow the user to specify a break to occur if an address falls within a specified range.

The ISE/32 will also have two 32-bit execution timer/counters for measuring time between two events or creating a new event after a predetermined number of events. Thus the user can not only perform time measurements in terms of clock cycles, events, instruction executions, or memory cycles, but also have the timer turned on by one event and off by another. Counting could be resumed whenever the first event reappears, allowing execution timing statistics to be recorded.

ISE/32 will have a 1023x128 entry trace buffer to support either Program Flow (non-sequential instructions or branches) or Bus Analysis Tracing. An entry in the trace buffer will include such information as address, data, and status, among others.

Since the architecture of the NS32032 lends itself to multiprocessing, ISE/32 will also support multiprocessing environments. Care is being taken not to force the user into a multiprocessing environment if the application does not require it. For such applications, then the ISE/32 will provide the most general case of multiprocessing, where a number of processors are operating asynchronously with both private and shared resources.

Processors do not have to be all NS32032 CPUs. Future enhancements to the ISE/32 include interchangeable emulator pods to support other members of the 32000 family and combinations of them. By supporting the most general of multiprocessing configurations, ISE/32 will be able to support all its subsets, including the tightly coupled synchronous dual processing which is a unique feature of the NS32032.

**Write 302**

—Mike McCullough,  
Group Marketing Manager,  
Development Systems,  
National Semiconductor

system or act as a standalone unit. A recent introduction, the Kontron Development Adaptor (KDA), enables an IBM Personal Computer to host their slave emulator subsystem (**Figure 2**). This allows system integrators to develop and debug application programs for 8- and 16-bit processors.

Dolch (San Jose, CA) gives system integrators the option to develop programs on a VAX or PDP-11 and download to the ATLAS 9600 or use it as a standalone development system. A portable version of ATLAS, COLT (**Figure 1**) offers most of the same features and runs the MP/M-II operating system. The 9600 runs CP/M and compatible compilers, assemblers and linkers. A reconfigurable system, the 9600 accepts different mea-

surement modules for tasks including logic analysis, emulation, EPROM and PAL programming, word generation, signature and waveform analysis.

The emulator module supports the Z80, 8085 and 6809; the trace module supports additional processors including the 68000, 6502, NSC800, 1802 and the 8080. There is also a choice between several high and low speed logic analyzer modules. One high speed logic analyzer, the model 96300, provides 16 300 MHz channels (100 MHz synchronous), and 0.5K of source and reference memory.

In addition to software development and emulation capabilities, Emulogic's (Norwood, MA) ECL-3211 microprocessor development system has a unique command file structure that allows the

system to be used for production test. With this feature, diagnostic test programs can be automatically executed on the unit under test (UUT) via the ECL-3211's emulator. Other features of the system include Pascal and C compilers, a symbolic debugger and the Emunet network for linking development systems. In addition, users can interface the system to a VAX or PDP-11. Emulators for the system support most 8- and 16-bit microprocessors from manufacturers including Intel, Motorola, Zilog and National Semiconductor.

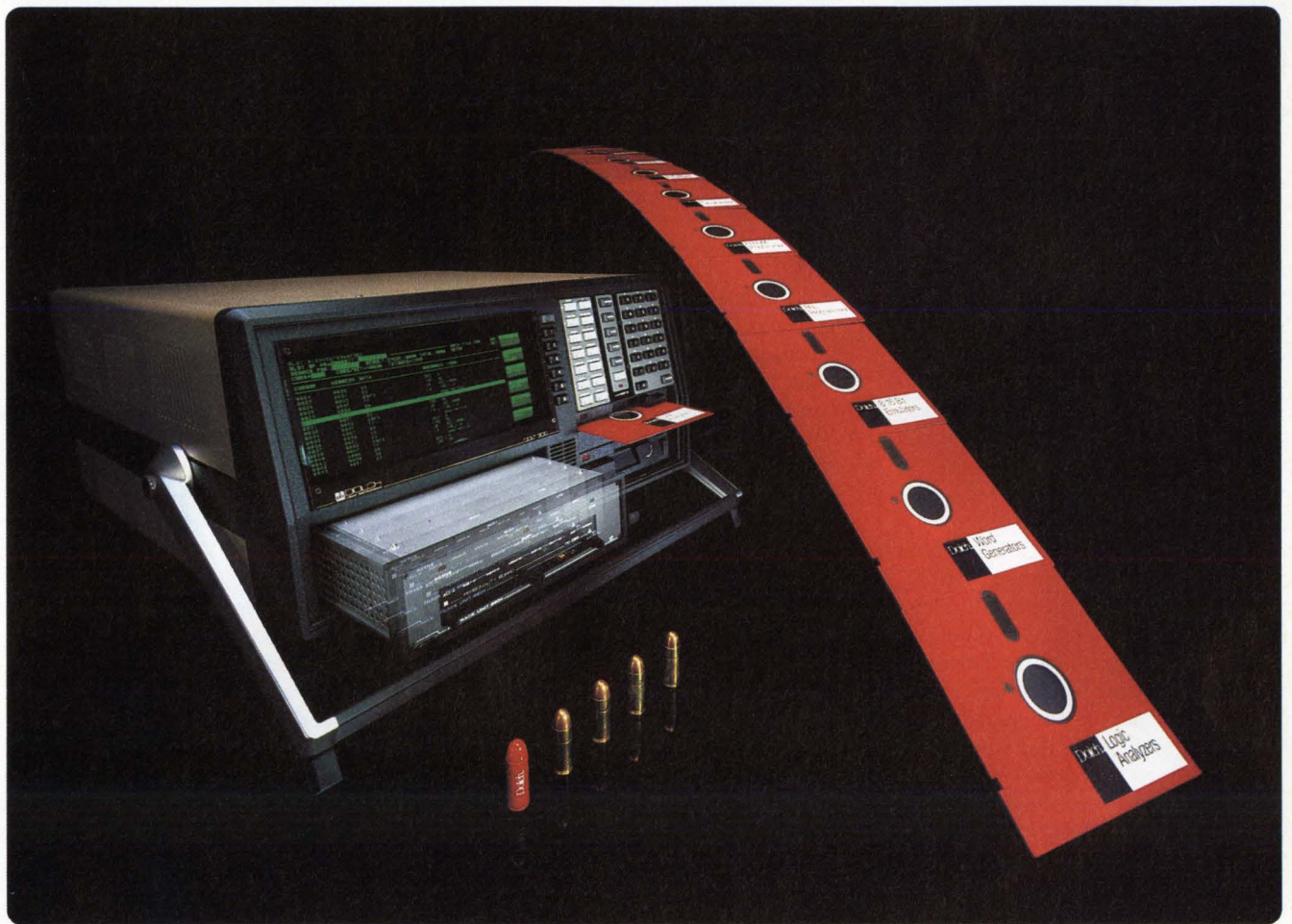
Emulogic also recently introduced a new line of development systems built around DEC's Professional-350 desktop PDP-11 computers, the ECL-3200 line (**Figure 3**). The first of the family built



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LOGIC INSTRUMENTS





Figure 3: Emulogic's new ECL-3200 Series development systems are built around the DEC Professional-350 desktop PDP-11 computers.

around the DEC-350, range in price from just under \$20,000 to \$25,000. Key features include: no wait state emulation, Pascal and C cross-compilers, symbolic debugging and comprehensive breakpoint capabilities. According to Emulogic President Frank Bruns, "Comparable universal development systems can cost as much as \$40,000. But by building on DEC's Professional computers, we are able to offer the industry's first full-function software development and in-circuit emulation system priced under \$20,000."

For a powerful development system under \$7,000, Microtek Labs (Gardena CA) offers their Personal Development System. This system supports microprocessors from manufacturers including Motorola, Intel and Zilog. Based on CP/M, the system supports software development, real time emulation, symbolic debugging, software performance analysis and logic state analysis.

### Dedicated systems

One major advantage to choosing a dedicated microprocessor development system is that when a microprocessor is released from its manufacturer, the emulator from that manufacturer is usually available much earlier than similar emulators from independent vendors. For example, the emulator for NS32032 and 68020 microprocessors will be available earlier than corresponding emulators from independent vendors (see "ISE/32" and "MC68020 Emulator/Analyzer Module").

Committed to maintaining compatibility between its older and new development systems, Intel (Santa Clara, CA) supplies enhancement products so their systems can be upgraded to meet the requirements of new chips. Intel offers three development systems: the Intellec Series and NDS-II for 8-, 16- and 32-bit

microprocessor development, and the less powerful portable iPDS unit for 8-bit processor development.

Completely integrated and based on the 8085, iPDS supports high level software development using PL/M, Fortran, Basic or Pascal and assemblers are available for all Intel 8-bit microprocessors and controllers. Interchangeable modules for emulation and PROM programming fit into the unit's side door and optional modules for bubble memory or an IEEE-488 interface can be purchased separately. When not being used as a development system, the iPDS can act as a personal computer since Intel also offers CP/M as an option.

For development projects that require more horsepower, Intel's Intellec Series IV, supports the iAPX 86/87/186/188/286, the MCS 80/85 and the MCS 48/51 family of microprocessors. Like the iPDS, the Series IV permits software development using PL/M, Pascal, Fortran, C and Basic. The Series II E, III E, IV are software compatible.

To further enhance the Series IV, Intel includes PSCOPE, emulator modules and the I<sup>2</sup>ICE system (Figure 4). PSCOPE, a symbolic debugger program, provides a window into program execution at the high level language source. By using the I<sup>2</sup>ICE system, which supports the entire iAPX 86 family, system integrators can perform high level language debug with in-circuit emulation. Consequently, assembly mnemonics do not have to be matched with high-level language statements. In addition, the I<sup>2</sup>ICE system has the same command syntax as PSCOPE. To complete the system, I<sup>2</sup>ICE has a 16 channel 100 MHz logic timing analyzer option.

Intel also offers their Network Development

System-II (NDS-II) which supports a distributed development environment. At the core of NDS-II is the network resource manager which provides mass storage, a spooled line printer, a protected hierarchical file system and distributed job control to each user. Workstations or standalone Intellec Series II, III or IV development systems can be attached to the network. An asynchronous communication link allows communication between an NDS-II workstation and a mainframe.

Aiming to capture users of Intel development systems, RELMS (San Jose, CA) offers ICEBOX, a software development and real time emulation system that interfaces to any of Intel's Intellec systems (MDS-800, Series II, III, IV) or the iPDS system. ICEBOX also communicates with any CP/M system with an auxiliary serial channel, a VAX running VMS or a PDP-11 running RSX-11M. RELMS supports emulation for the Z80, NSC 800 and 8085 microprocessors.

Motorola (Phoenix, AZ) offers the Exormacs and the VME/10 (Figure 5) dedicated development systems. Exormac, a multi-user system, supports the MC68000 family, contains a 68000 CPU and runs under the VERSAdos-E operating system. Up to eight users can simultaneously perform symbolic debugging and develop software in Pascal or Fortran. The compact VME/10 desktop system can be used for 8-, 16- and 32-bit processor development. Software features include a Pascal compiler, a macro assembler, a linkage editor, a text editor and a symbolic debugger. For hardware development, the HDS-200 or the HDS-400 hardware/software development stations provide for 8- and 16/32-bit support, respectively. In addition, the real

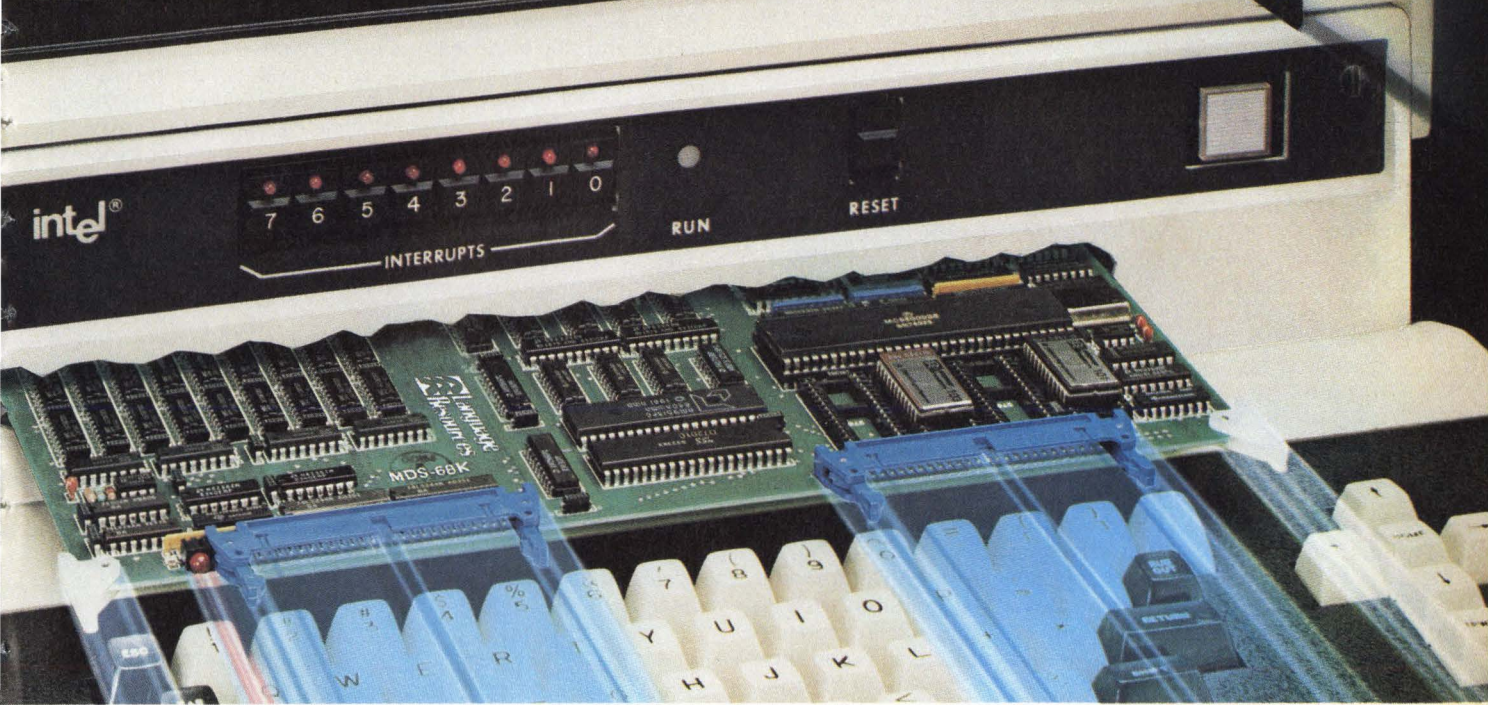


Figure 4: Intel's bond-out technology gives the I<sup>2</sup>ICE system special access to internal processor states that are virtually inaccessible in any other way. The result is a near Intel monopoly on emulators for the 8051 microcontroller and the 80286 microprocessor.



# MDS-68K

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LR's MDS-68K CPU board contains a 68000 CPU, 256K bytes of high speed RAM, proprietary ROM's, 2 serial I/O ports and a memory management subsystem. Plug it into any Multibus master card slot in an MDS system chassis, and run code in a true 68000 environment.

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With MDS-68K, you can extend the range of an Intel MDS to include full 68000 family development support without sacrificing those Intel features you have come to depend on. MDS-68K software and hardware is passive unless you access it through the special software provided in the package. Plus you can use available Intel tools (e.g., CREDIT™, UPM) concurrently with MDS-68K.

The plug-in board provides you with two serial I/O ports for interfacing to one of the several available 68000 hardware emulators. You can develop code for Intel microprocessors while adding 68000 development capability without swapping out boards.

Our MDS-68K base package, including Motorola compatible assembler, linker/locator, symbolic debugger, 68000 CPU board and extensive documentation is \$5995. The optional Pascal compiler (C and PL/M-68K compilers available soon) are \$1995 each.

### Major Benefits

- Provides 68000 family design freedom for your current Intel Intellec MDS
- Meets development support needs for designs using a 68000 family chip and an Intel controller chip (e.g. 8051)
- Saves capital equipment costs by utilizing existing MDS equipment
- Frees you from having to spend time learning a new development system's editor and other support tools
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## MC68020 Emulator/Analyzer Module for the HDS-400

To provide development support for its new 32-bit microprocessor the MC68020, in December, 1984 Motorola will introduce the MC68020 Emulator/ Analyzer Module. This module is an addition to the HDS-400/BSA control station that provides development support for all of the MC68000 16/32-bit microprocessor family.

With a compatible host and appropriate emulation and BSA module, the HDS-400 speeds hardware and software development time by providing real time emulation and real time bus state analysis for the MC68008, MC68000, MC68010 and now the MC68020. The HDS-400 may be hosted by Motorola's EXORmacs or VME/10 running either VERSAdos or, in December, UNIX System V/68 or by the DEC VAX running either VMS or UNIX System V. The control station contains four VERSAmodule boards in a four slot chassis. A VM02 processor board acts as the control module, a Family Interface Module (FIM) provides the interface between the control station and the emulator module. The system includes a Bus State Analyzer (BSA) module as well. 256 Kbytes of emulation RAM can be added with an optional Emulator Memory Module (EMM). Also contained in the control station are a built-in power supply and a five slot VME I/O channel to allow serial communication with host and terminal.

All of the HDS-400 emulators including the MC68020 emulator/analyzer module provide an accurate power-on/ reset sequence, as if the MPU were in its socket. In addition, the user has unrestricted use of the memory map. Emulation and target memory can be loaded, modified, displayed and dumped. Targetless emulation is possible using only emulation memory. Emulation memory can be write protected to allow

testing of ROM-able code and up to 16 breakpoints can be set in target or emulation memory. Set breakpoints will stop emulation before instruction execution; the emulator will not be fooled and stop on an instruction prefetch.

Three triggering modes are accommodated on the BSA: Continuous Trace, Sequential, and Address Window. The Bus State Analyzer can provide performance histogram displays and complex breakpoints with up to seven events (sequence terms) from the 79 qualifier lines of the BSA.

The MC68020 Emulator/Analyzer module has been integrated into one module with one cable to the target system. This allows the BSA to trace emulation memory cycles as well as target memory. The emulator and analyzer may be used independently or simultaneously.

Real time emulation is possible up to 16.67 MHz while the BSA is capable of bus speeds up to 5 MHz, the equivalent of 20 MHz with one wait cycle or 15 MHz with no wait cycles. The real time BSA supports the 83 principal MC68020 pins, 75 at one time. Four additional hardware option lines provided with the BSA allow monitoring of any of the 91 active pins of the MC68020, 79 at one time. Cache operations are supported by the MC68020 emulator/analyzer module. The cache enable can be controlled by both the target and the emulator and breakpoints will remain operative even with the cache enabled.

*Motorola Semiconductor Products*  
**Write 303**

time Bus State Analyzer gives the user logic analysis capability.

Also supporting the 68000, Mostek (Carrollton, TX) offers two development systems. One system, RADIUS (Remote Access Development and Integration  $\mu$ Computer System) is designed for use with a host computer. Software development on the host can be downloaded to RADIUS for hardware/software integration and PROM programming. The second system, MATRIX, stands as a complete system that provides tools for both software development and hardware/software integration. Software tools include an editor, assembler and linker. Hardware tools for both the MATRIX and RADIUS include the firm's AIM series of in-circuit emulators which support the 68000, Z80 and Mostek's 3870 family of microprocessors. A PROM programmer can also be purchased for the MATRIX system.

Taking a less conventional approach, National Semiconductor (NSC) (Santa Clara, CA) offers development tools that support microprocessors from Zilog and Intel. NSC offers two development sys-



*Figure 5: Motorola's VME/10 and HDS-400 development system will host the new MC68020 emulator.*





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tems, STARPLEX II and the multi-user SYS32 for their 32000 microprocessor family. With STARPLEX II, users can develop software using Fortran and Basic (PL/M and Pascal for the 8080/8085, NSC800 and Z80). About the size of a personal computer, STARPLEX II supports the firm's in-system emulator (ISE) packages which include the NSC800, INS8048 family, INS8070 family, INS80CX48, 8080, 8085 and Z80. Emulators are connected to the ISE module where standard features include a symbolic debugger and an in-line assembler/disassembler.

To support their NS32000 family, NSC's SYS32 development system accommodates up to eight users on a time shared basis. With a UNIX-based operating system (GENIX), SYS32 includes a C compiler, NS32000 assembler and linker as well as emulators for the 32000 family.

Zax Corp. (Irvine,CA), offers dedicated development systems and stand-alone emulators for Zilog, Intel and Motorola processors (Z80, 8048, 8049, 8085/86/87/88, 68000). Development systems for these processors include a CP/M microcomputer, editor, assembler, linker, debugger, in-circuit emulator, EPROM/EEPROM programmer, and a CRT. All emulators have an in-line assembler, provide uploading/downloading with Intel's Hex format (via RS-232C) and can display software programs in HEX, ASCII, or disassembled format. In addition, the firm offers software packages for symbolic debugging and uploading/downloading files between Zax emulators and CP/M, UNIX, iRMX and MS DOS based computers.

### Intel Protection Scheme Thwarted

To stifle the development of third party emulators for the 80286 microprocessor and 8051 microcontroller, Intel designed these chips without providing means of access to internal registers and control signals. Without access, building an emulator is extremely difficult, if not impossible. Intel built special versions of these processors, called bond-out chips, that provide added pins and access to the internal registers. However, these emulator-specific chips are only found in Intel's emulators and are not commercially available.

According to Dr. John Adam, Kontron's Director of Marketing, Kontron has solved the 80286 emulator problem by replicating (via hardware and software) the functions that are inaccessible in the chip. Kontron plans to introduce this

emulator at the 1985 Electro Show.

As for the 8051 microcontroller, control signals and contents of the internal ROM memory are not accessible from outside. Given that, there is no way for an emulator to observe the chip's internal registers when running code in the ROM space. However, Hewlett-Packard has surprised Intel by offering an emulator for the 8051. By reverse engineering, HP was able to build their own version of the chip and bring out necessary signals to the pins.

### Conclusion

A major issue surrounding today's development tools is whether to purchase a system that does only microprocessor development tasks or a general purpose computer for all engineering applications. There is little doubt of the power that a dedicated/universal development system offers. However, it is important to consider other aspects of system design. For example, when designing a product that includes a microprocessor, the job entails much more than just writing and debugging code. The circuitry surrounding the processor is of equal importance. Until recently, this peripheral logic was designed primarily with off-the-shelf parts. Semi-custom chips (gate arrays and standard cells) have changed the situation. It is now important to have design tools that can be used for VLSI design and PCB layout as well as software development.

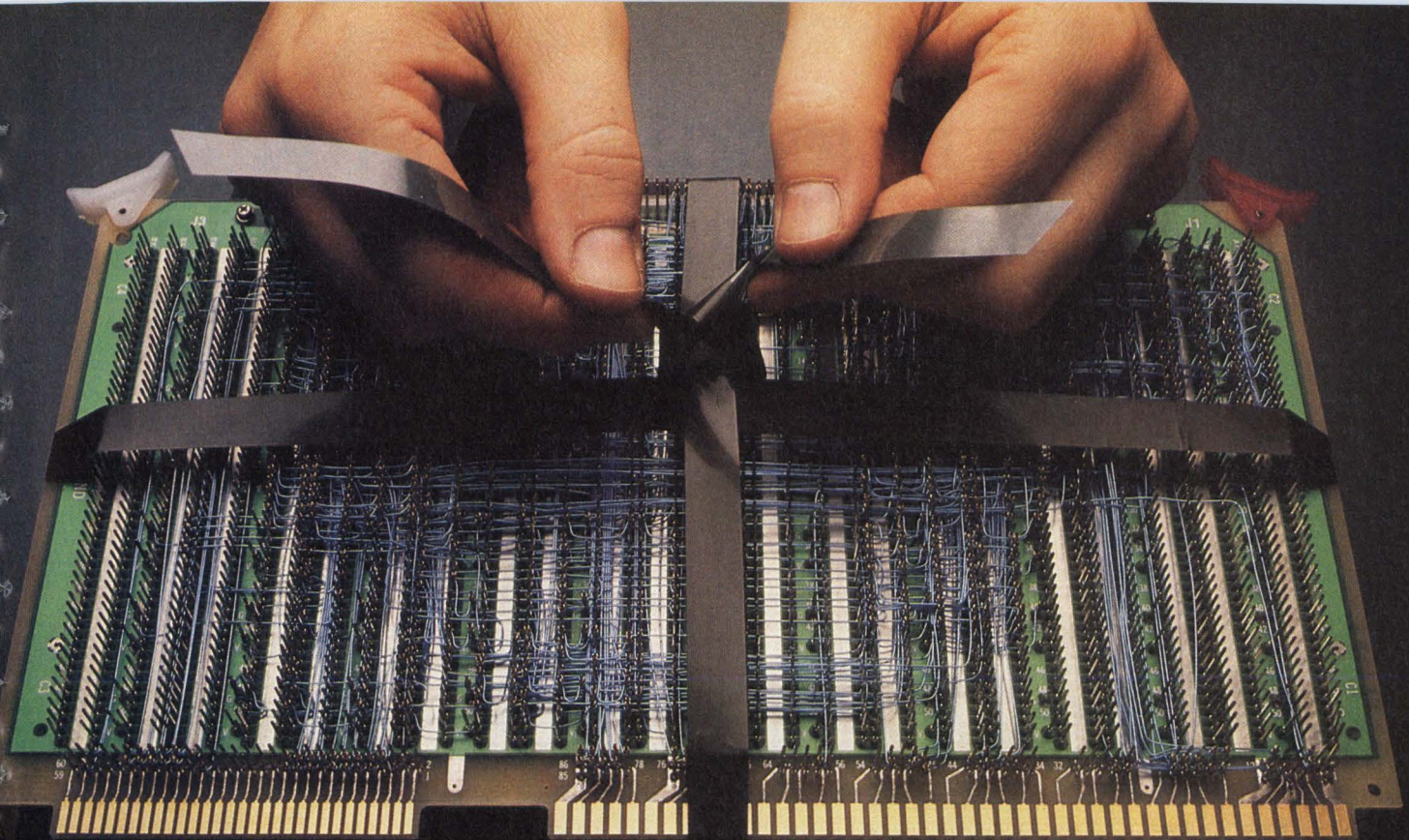
Networking is also becoming a crucial element in the design environment. It has been a topic of discussion for several years, but the advent of 32-bit processors makes networking a necessity rather than a luxury. Writing and debugging code for these complex chips often requires design teams as large as 100 engineers. Without sophisticated networking schemes, coordinating such huge projects is almost impossible. The days of transferring floppy disks between engineers is over.

Along the same vein, managerial software that helps orchestrate large design efforts is also becoming a necessity. Project management tools have long been considered of secondary importance, but as development tasks grow their use becomes unquestionable.

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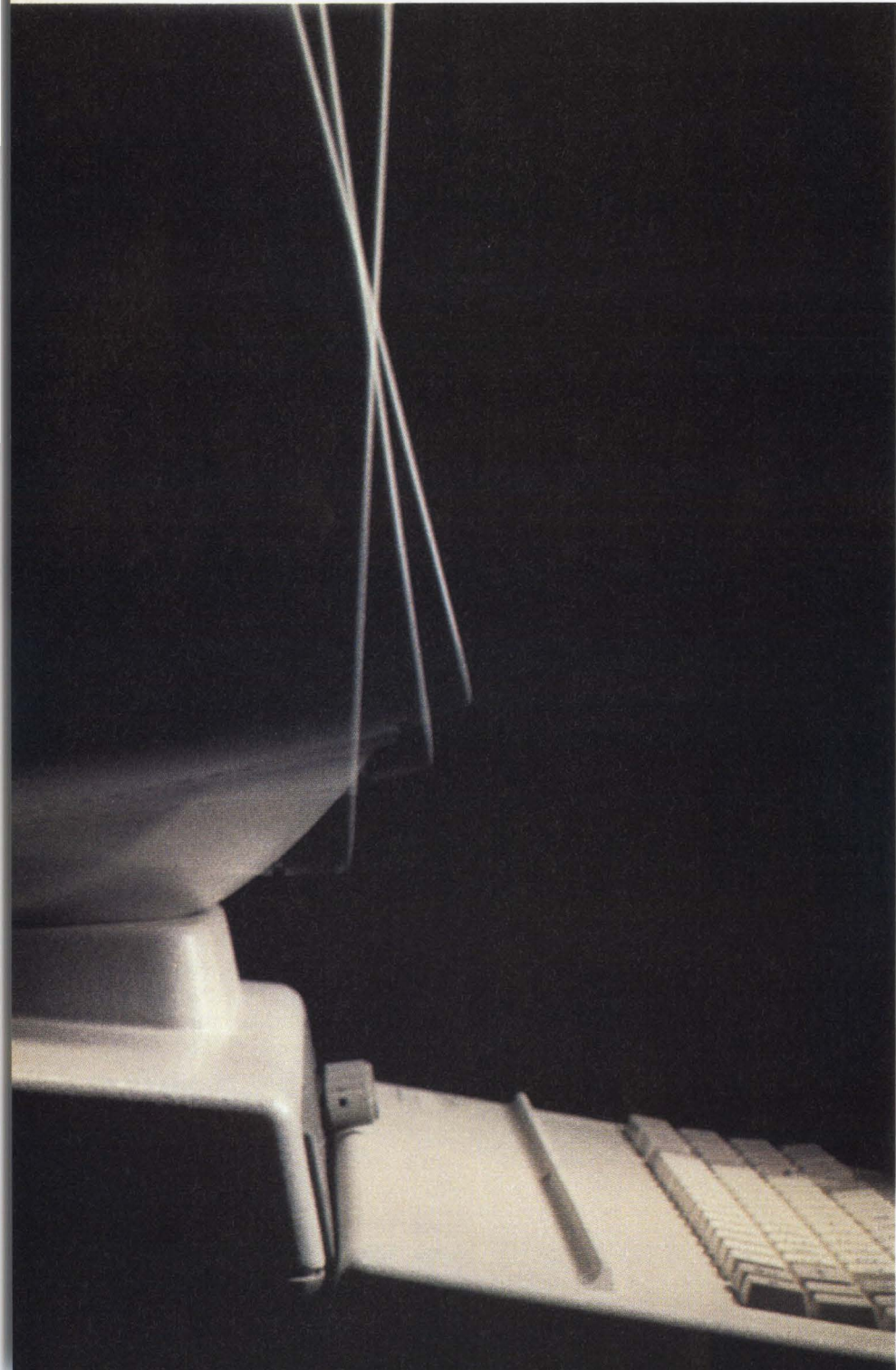
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# Function Determines Form In Workstation Ergonomic Design

by M.R. Hanrahan, Associate Editor



One of the most difficult issues facing workstation ergonomists or human factors engineers, is how to determine an evaluation method for assessing factors affecting human performance. These factors include environment, workstation hardware, applications software, and various psycho-social considerations. The inherent complexity in this task has led many ergonomists to prefer concentrating on single issues—such as VDTs, interactive input devices, or applications software and the hardware that houses it. It is the synthesis, however, of these design considerations that ultimately results in an ergonomically well-designed workstation.

The primary step in ergonomic design is to determine the product requirements, addressing areas such as performance specifications, styling, cost, reliability and safety. The product's size, weight, tolerances and strength are also defined. These requirements are typically then passed on to a manufacturer's engineering group to develop the design solution that satisfies the greatest number of requirements.

Human factors evaluation labs are now a vital segment of the design process at many companies. Quantitative models, or mathematical representations of a problem, can be a very precise way to describe important ergonomic factors. Using models or simulated ergonomic situations in a lab, ergonomists can specify the variables that appear to affect human behavior and design performance.

The Industrial Design Group at Digital Equipment Corp. has determined a process of testing DEC products from the VAX to the Rainbow PC through a series of ergonomic benchmarks conducted in their Human Factors Lab. Users are observed while unpacking and assembling the product, interpreting documentation, and maneuvering input devices. Potential

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The primary step in ergonomic design is to determine the product requirements, addressing areas such as performance specifications, styling, cost, reliability and safety.

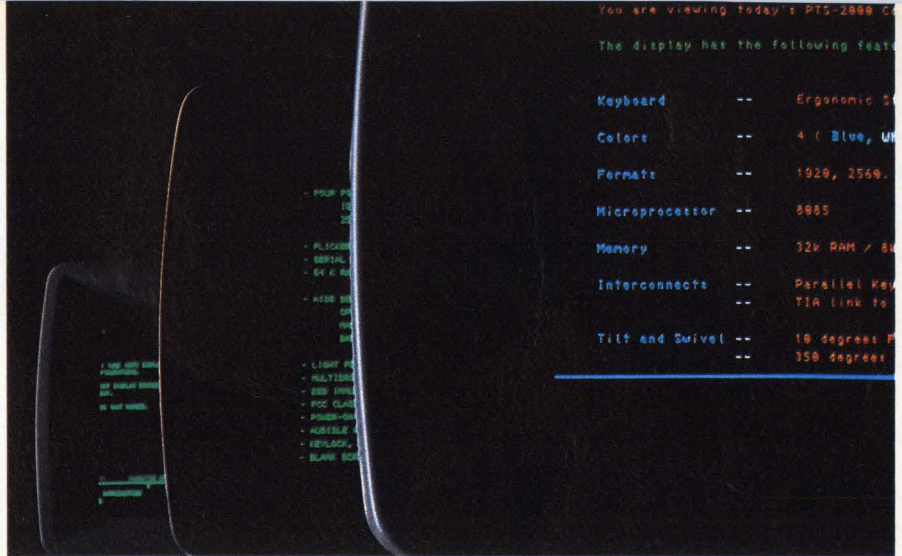


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trouble areas are targeted and alternatives are recommended by designers observing the experiment. Charles Abernethy, Manager of Human Factors at DEC, stresses that a task must be easily executed regardless of the level of expertise of the user. "Added functions must be addressed as to their accessibility—how you access them, and once you get there, how you use it."

### The User Interface

The design functions now inherent in a typical CAD system replace the traditional designer's drafting table with a computer system and interactive graphics terminal. A plethora of input devices and interactive controls characterize the design station. There are various specifications of the user-system interface which assure communication between the designer and the human factors engineer. The user-system interface consists of hardware elements (keyboard, display, input devices, etc.) and their dynamic use, defined as the system operations which are usually implemented in software.

While considerable progress has been made in the design of the hardware, the methods of use of these items is more difficult to specify. An emphasis must be placed on productivity in systems development through efficient user-system interface specifications. Specifications provide a mechanism for control of interface design, while keeping software development costs down, and providing hardware design direction.

When determining interface specifications, the suggested ergonomic design cycle can be divided into three progressive phases: 1) functional design; 2) pre-

liminary design; and 3) detailed design (Figure 1). The functional phase consists of the requirement analysis, definition of functions, and the initial breakdown into subfunctions. The preliminary design phase is the further analysis of the subfunctions and the definition of system elements. Each of the system elements are described in terms of hardware requirements, software requirements, and operator requirements. The last design phase is the detailed analysis of the requirements and the integration of system elements. Lastly, verification of the system design is accomplished.

### Interactive Input

A variety of technologies have been developed that allow a system operator to interact with computer-generated graphical or pictorial data. These include both cursor-movement devices such as keyboards, joysticks, "mice" and direct-access devices such as light pens, light-guns, touch pads, touch screens and graphics tablets.

Touch pads and touch screens can take a number of forms, ranging from capacitance (the form originally used in the 1960s) to infrared and ultrasonic. Results of test applications of touch technology in the past several years suggest that a judicious application of the technology can produce beneficial results. These findings, however, deal with tasks requiring relatively low resolution.

Screen angle and its relationship to the touch input method is critical and is based on user preference. Screen angle from the vertical usually varies from 20°, 30°, to 45°. The majority of users prefer a 45° angle, given a fixed display base height and control of glare sources.

A recent alternative to the touch screen is the touch pad, which resides on the keyboard and eliminates the extra movement required to extend the hand from the keyboard to the screen. Touch pads also reduce the real estate on a desktop which has been traditionally occupied by input devices such as a mouse. Apollo Computer's (Chelmsford, MA) recently intro-

FUNCTIONAL	DESIGN PHASE:	
	PRELIMINARY	DETAILED
<b>Design Activity:</b>	Hardware Mission Analysis—Functions—Subfunctions—System Elements— Software —Integration—Verification Operator	
<b>Specification Methods:</b>	<ul style="list-style-type: none"> <li>• Element Specifications</li> <li>• State, Transition Diagrams</li> <li>• Detail Timelines</li> <li>• Operational Scenarios</li> <li>• Military "B" Level Sub-system Specs (B-1s, B-5s)</li> </ul>	<ul style="list-style-type: none"> <li>• Design Guidelines</li> <li>• Tailored User-System Interface Specification</li> <li>• Timeline Verification</li> <li>• Checklists</li> <li>• Military "C" Level</li> </ul>

Figure 1: The relationship of user-system interface specification methods to system design activity for each of the progressive design stages.



duced N550 Graphics Workstation incorporates a touch pad as a standard feature. The pad is basically a grid of points sensitive to touch, which give back a position value when pressed. Its absolute mode allows the cursor to jump to the point of contact, allowing a mapping between touch pad and screen. The relative mode offers constant contact, allowing the cursor to be dragged across the screen.

## Human Factors Software/Hardware

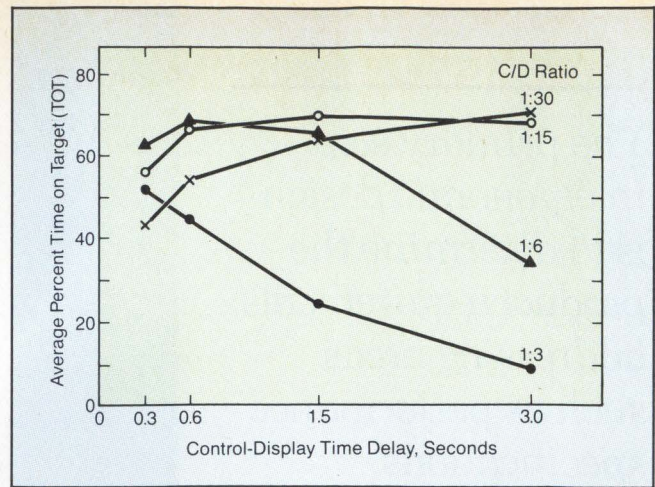
An area of prime importance to workstation vendors is providing the tools with which applications developers can make a particular application approachable. It is imperative that a workstation allow the engineer to concentrate on the application rather than the system itself.

Al Lopez, Apollo Computer's Director of User Environment and Graphic Software, emphasizes "the workstation has to be flexible enough to accommodate different styles of interfacing." Lopez cited two problems that exist when applications developers present more complicated interfaces. The applications developer has to spend more time determining menus, devising icons, and routing the cursor track, etc. And each application developer has perfected a different "style" of memory access and iconic representation. When the objective is a certain amount of consistency across applications, it is necessary to allow some familiarity through common menu directions, common icons, or common control keys for different applications.

The expert user at a sophisticated workstation may not require the same iconic representations and graphic cues as users in an office environment, for example. Designers, however, are striving toward systems which are flexible and extensive allowing the user to migrate from one style to another, or work in a variety of styles depending on the nature of the application. Lopez predicts a situation where "application developers will be working in conjunction with user interface designers where the interface issue will include how images are perceived, how to lay out the screen, and the determination of a set of tools that allow the designer to develop a user interface."

Operator performance is not only related to hardware design parameters, but is also dependent on software. The design of programmed operations and construction of man-machine dialogues can complement the workstation selection process, particularly the selection of display

Figure 2: Machine operation vs. human performance in reaction time.



terminals, or it can degrade operator performance. Factors such as presentation rate, irrelevant information and irregular presentation can also strongly influence how well the system is used.

Deciding how the various subtasks fit together and how the operator reacts to them are important parts of the software engineering process. The continual feedback of information to the operator on his performance can improve that performance, and the lack of it can introduce additional errors. Feedback can be in the negative (performance degrading) as well as positive direction. When feedback is time-delayed, performance suffers, unless the system is designed to compensate for this delay as shown in **Figure 2**.

An important consideration for the feedback cycle is the rate at which information is demanded by the system. The number of operator errors has proven to increase as the load (rate of information transfer required) increases. An optimum point should be targeted where high speed and low errors combine to provide the best performance.

Trade-offs must often be made between various parameters of workstation ergonomics and human factors. For example,

it may be necessary to sacrifice compatibility in order to improve some other aspect of a program or system.

## Displays

The relationship between luminance, contrast, exposure time and visual angle are important elements of a display system and all are related to workstation performance. These factors can also be related to the element of flicker (where the refresh rate is lower than a value that produces a constant brightness). Refresh rates of 35 cycles per second can provide brightness levels (40 foot-lamberts) at which many users do not experience annoyance. When the refresh rate drops below 20 cps, flicker is discernable and user irritation occurs. Since flicker is more noticeable at the higher brightness levels and some individuals are more susceptible to its effects, a rate of 50 cps is required for brightness levels of up to 30 fl and 60 cps for levels up to 180 fl.

Another important display parameter that affects performance is resolution. The importance of resolution is primarily the effect it has on two other factors of performance: legibility and bandwidth. The bandwidth is defined as the amount

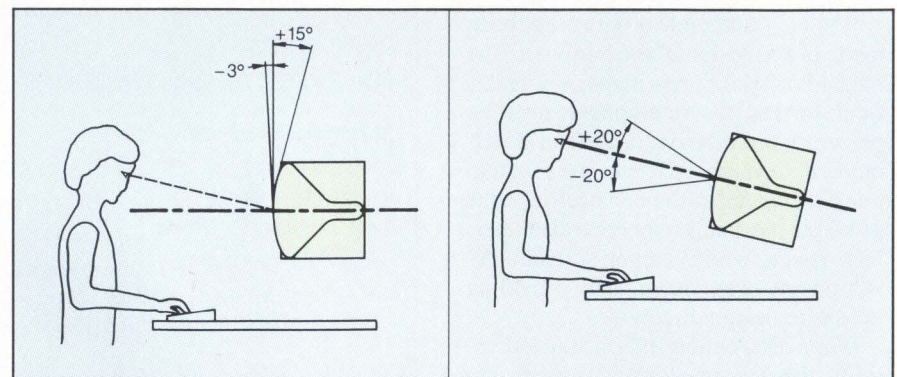
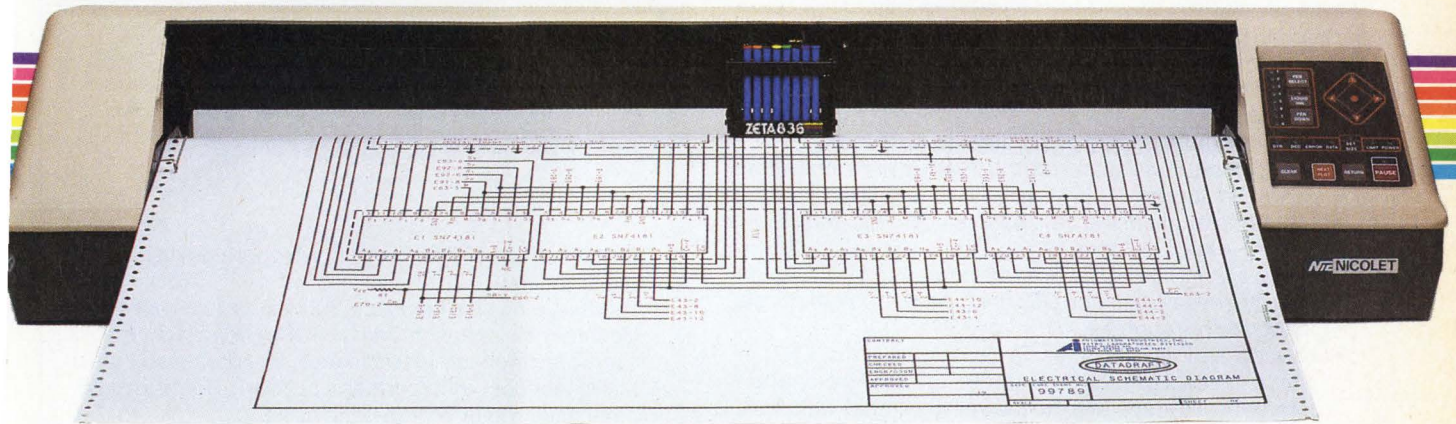


Figure 3: a. ECMA recommended tilt angle for visual displays. b. ECMA recommended viewing angle for visual displays.



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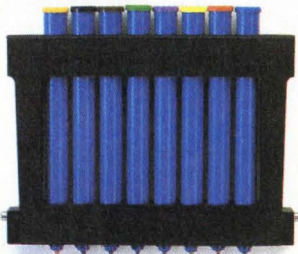


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## Keyboards and DIN Specs

A major influence governing keyboard ergonomics is the DIN specification, dating to 1980. DIN, an abbreviation of the West German electrical standards institute, Deutsche Industrie Normenausschuss, arose from intensive studies of operators performing high-speed data entry, and sought to match the engineering of the keyboard to the natural motions of hands, wrists, and fingers. The goal is to minimize errors and maximize productivity.

DIN makes the following requirements of keyboards:

- The maximum distance from the tabletop to the home row of keys is 30mm.
- Mounting angle of the keyboard is not to exceed 15°.
- Key travel of 3 to 4 mm.

There are a number of important "human comfort" areas which are not specified in the DIN document. Customers are specifying factors such as:

- Keycap and legend color. To complement the CRT, in which the background is generally light and the characters dark, keycaps are molded or imprinted with dark legends on light-colored keycaps.
- Keycap finish. A non-glare finish on keycaps and enclosure aids in minimizing eye fatigue.
- Legend placement. Legends may be located on a quadrant or on the front surface to allow maximum space utilization. Multicolor printing is used to differentiate multiple legends printed on a single keycap.
- Alternative keyboard arrays. One example is the Dvorak system, in which vowel keys are more accessible to the operator's index fingers than the standard QWERTY arrangement.
- "Homing devices." While the keyboards often have "deep-dished" F and J keycaps, an alternative is a raised ridge



*Oak Switch Systems' low-profile, full-travel membrane keyboard.*

on the surface of these keys to aid operators in locating the home row.

- Feedback. Audible feedback, such as a click, verifies key closure to the operator. One type of feedback now receiving more emphasis is tactile feel. The preferred type of tactile feedback incorporates a buildup of force to make-point, followed by a drop-off in force.
- Free-standing keyboards. The emphasis of free-standing keyboards for portability allows interface to the central processing unit by either a coiled cord or infrared link.

The study of keyboard ergonomics continues, especially with major keyboard manufacturers. This will certainly lead to more opportunities for consumers to express preferences and ultimately for home and business operators to become more comfortable using keyboards.

*—Harold Hengesh, Director of Marketing,  
Membrane Products, Oak Switch Systems Inc.*

**Write 305**

of information displayed per unit time. This is measured by the capacity of the display and the rate of information transfer. If the resolution of a system with a given bandwidth is increased, the rate of transfer of a display decreases as well as the response of the display system. If the response rate is slower than the human response time, this will slow the interaction, and in some cases affect the feedback cycle.

The ability of the phosphor to remain illuminated between refresh cycles is known as persistence. Short persistence phosphors lose their luminance level much faster than long-persistence phosphors and will appear to flicker unless refreshed at a higher rate.

The typical CRT screen occupies a large portion of the visual field. When it is used in positive polarity, featuring dark or unilluminated characters on a light or illuminated background, the combination of phosphor persistence and refresh rate must be carefully matched to get

above the expected fusion frequency for fairly large light sources. Positive displays require wider character stroke widths than the equivalent negative polarity displays, which feature light or illuminated characters on a dark or unilluminated background. This is due to the fact that the eye reacts primarily to luminance and emphasizes it through a process called lateral inhibition.

Provided adequate luminosity is achieved, any color within the visible spectrum can be used in displays. It is recommended that deep blue or violet be avoided for fine detail since the acuity of the eye is poor for these colors. For good legibility, display designers should aim for high luminance contrast between a symbol and its background, independent of color. Symbol and background of equal luminosity should be avoided even if they are of different colors in order to maintain good clarity. In multi-color displays, the distance between colors on the chromaticity chart should

be such that they are clearly distinguishable. Lower level luminances, when achieved by using screen backgrounds that reflect the ambient luminance level, have the effect of reducing color separation. If the background is significantly lightened, colors will become pale or pastel and closer in hue to each other, thus reducing color contrast.

The glare factor, another problem when designing displays, has been addressed by a variety of methods. The curved surface of the screen distorts images as would a curved mirror. Glare technically includes reflected light sources, but may also be used to describe any reflected image. The best method of eliminating specular glare has proven to be careful placement of the CRT relative to the windows and light sources. The use of swivel and tilt adjustment on the CRT can help considerably. Other popular techniques include; etched surfaces, optical coatings, micro-mesh filters, polarizers, and hoods.



## Recommendations

The European Computer Manufacturers Association (ECMA) and the Computer and Business Equipment Manufacturers Association (CBEMA) recommend some general principles on designing the components of the workplace to meet the ergonomic needs of those performing tasks for extended periods of time. Their goal is to provide for worker satisfaction by designing to meet the prolonged comfort and productivity needs of a wide range of workers in a wide variety of settings. The three prime elements of the workplace which affect performance are the task, the workstation, and the environment.

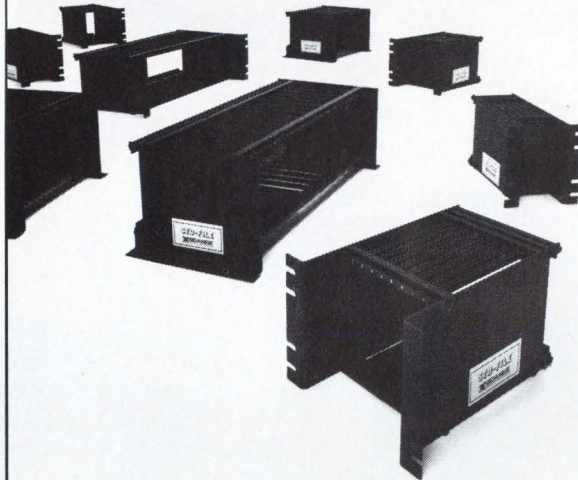
The workstation itself should provide an adequate work surface determined by the dimensions of the required working equipment and by its arrangement. Current workstations include angled and adjustable (up-down) tables. Regardless of whether the table is adjustable or not, a height-adjustable chair is required which dictates such factors as vertical distance between seat pan and keyboard; viewing distance from eye to reading surfaces; relative heights of screen and eye; and table height if non-adjustable. In most cases, keyboards should be separable from the screen. The inclination of the surface of the screen should be adjustable at least between  $-3^\circ$  and  $+15^\circ$  from the vertical perpendicular to the base, to avoid visual disturbances such as reflection. Under some circumstances it may also be desirable to provide height adjustment to control the angle between the line of sight and screen surface. While  $90^\circ$  (normal) is optimal, a variation of  $\pm 20^\circ$  is usually acceptable (Figure 3).

Other recommendations include: a distance between users of not less than 39"; a combination of ambient and task lighting to achieve a 300-500 lux intensity; detachable keyboards; tilt and swivel screens; keyboard slopes between  $5^\circ$  and  $18^\circ$ ; and a  $5 \times 7$  dot matrix for character presentation on displays. Although standards cannot be adequately determined due to the variety of situations surrounding workstation use, ergonomic guidelines for designers allow the human factor to be accommodated in well-designed, comfortable and efficient workplaces. □

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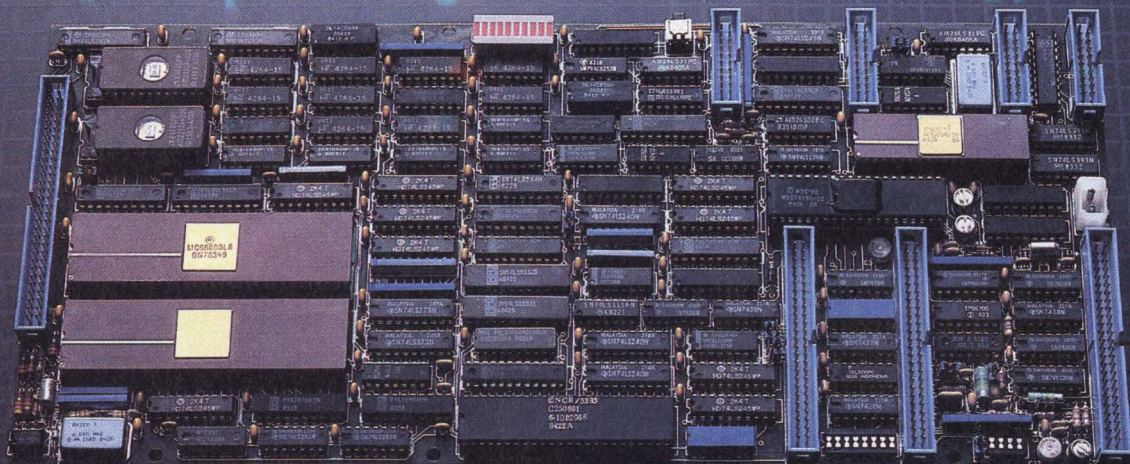


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# Caching Disk Controller Relieves System Bottlenecks

by Stephen Goldman

Processors have become faster, disks have become larger, and data rates have increased, but one bottleneck remains in many small computer systems. Disk rotational speed and thus data access time have not been significantly enhanced and are not likely to be in the near future. This dependence upon a moving part for what is, in most systems, the key memory device, can cause severe performance degradation.

Multi-user or multi-tasking operating systems such as UNIX can aggravate the

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*Stephen Goldman received a BS in Physics from the University of Florida and was a member of the technical staff of Georgia Tech before founding Distributed Processing Technology in 1977.*

problem by requiring data to be simultaneously accessed on widely separated areas of a disk. With average cylinder seek times of around 85msec for a typical rigid disk drive, system throughput can be excessively slow.

A family of caching disk controllers, the PM-3010 series, has been designed to relieve this bottleneck. The combination of fast access time (400  $\mu$ sec. worst case) and high sustained data rate (1.0 Mbyte/sec) along with up to 16 Mbytes of cache, allow disk throughput to be substantially increased. Up to eight rigid and flexible disk drives can be controlled by a single 5 1/4" extended form factor board, using one 5VDC power source. The disk controller family controls a range of drives including Winchester and flexible disks. ST506, SA1000 and SMD compatible Winchester drives with up to 16 heads and

1024 cylinders are supported along with SA460 and SA860 compatible flexible disk drives.

The controllers use the Small Computer System Interface (SCSI) for host communications. The SCSI specification, proposed by the American National Standards Institute (ANSI), defines both hardware and software protocol for device controllers. The primary objective of the SCSI interface is to provide host computers with device independence. Disk drives, tape drives, printers, and communications devices, of different types, can be added to the host computer(s) without modifying the interface hardware and with little or no change in generic system software.

## Standard SCSI Command Set

The PM-3010 supports the standard and



## The primary technical problem to be overcome during the design of a caching disk controller is the limitation on cache access time.

extended SCSI command set. An important objective during its design was to assure that caching operations were transparent to the host computer and did not require modification of existing software. The same basic SCSI commands are used by both the controller and other SCSI compatible disk controllers. The primary difference is in the execution speed of those commands.

The worst case access time for cache resident data with the PM-3010 is 400 $\mu$ sec. Access time is measured starting with receipt of the last byte of the host command and ending with the first byte of the data transfer between controller and host. Without cache, the access time would be limited by the rotational latency and cylinder seek time of the disk drive. For ST506 compatible Winchester drives, the average rotational latency is 8.3msec and the average cylinder seek time is typically 85msec. This means that if the data can be accessed in cache, the PM-3010 will begin its data transfer in 1/200th the time it takes a conventional disk controller to do a random disk access. Even if the disk read/write heads are already positioned at the correct cylinder so that no seek is required, the disk access will still take 20 times longer than the worst case PM-3010 cache access.

Once the data transfer is initiated, it proceeds asynchronously at a rate determined by the host and the controller. The PM-3010 is capable of handling data transfers at up to 1.0 Mbyte/sec. Although some non-caching disk controllers can also transfer data across the host interface at that rate, the data must additionally be transferred between the controller and the disk. Since data transfers to ST506 compatible drives are slower than 1.0 Mbyte/sec, a non-caching disk controller will not be able to maintain a sustained data rate of 1.0 Mbyte/sec.

In theory, the best possible sustained data transfer rate that a disk controller without cache could maintain is limited

by the average data rate for sequential sectors on a disk. Using the example of a controller capable of handling a sector interleave of zero, at 256 bytes/sector, the best average data rate for an ST506 compatible drive is less than 500 Kbytes/sec. Even if no extra time was taken up by the subsequent transfer of data to the host, the PM-3010 would still transfer data at twice the rate of a conventional "high-performance" disk controller.

### Cache Expandable To 16 Mbytes

Since cache accesses are so much more rapid than disk accesses, the key to optimizing performance with a caching disk controller is to maintain the highest possible "hit ratio." Hit ratio is defined as the number of times that data requested by the host is found in cache, divided by the total number of data requests.

Although highly dependent upon the application program, hit ratios as a rule, can be increased by raising the amount of cache memory. The PM-3010 comes with 128 Kbytes of cache memory integrated onto one 5.75" by 12.5" circuit board. Memory expansion boards may be added to increase the size of the cache. With a maximum supported cache size of 16 Mbytes, approximately 64,000 disk sectors of 256 bytes each can simultaneously reside in cache with sector sizes of 128, 512, and 1024 bytes also supported. The ability to expand cache as needed allows the system designer to configure the controller for maximum performance without requiring more cache than needed for his application.

### Sector Vs. Track Caching

The primary technical problem to be overcome during the design of a caching disk controller is the limitation on cache access time. If the access time for cache resident data is too long, a cache system

may, in certain cases, slow down an application rather than speed it up. In order to reduce cache access time, many caching disk controllers resort to track rather than sector caching.

Track caching schemes access all sectors on a track as a group when moving data between cache and disk. Since entire tracks are stored in cache instead of individual sectors, the search algorithms are much simpler. The primary problem with track caching schemes is the additional overhead needed to access and store entire tracks of disk data when only one sector may be needed by the host. Track caching works well when large blocks of physically contiguous data are accessed, but performance may be seriously degraded for random access file structures such as hierarchical or non-contiguous files.

To avoid this the PM-3010 uses sector rather than track caching. Each sector in the cache is handled separately and only the sectors needed by the host are read into cache. However, even with up to 64,000 separate sectors residing in the full 16 Mbytes of cache, worst case cache access time will never exceed 400 $\mu$ sec. When sequential sectors are accessed, throughput can be further increased by addressing multiple sectors with a single command. In this case, the rated access time applies only to the first sector in the group. All additional sectors addressed by the command will be transferred across the host interface without significant delay.

### High Performance Internal Architecture

To search 16 Mbytes of cache in less than 400 $\mu$ sec required development of new caching algorithms executed in firmware by an on-board 68000 microprocessor. The proprietary algorithm organizes the

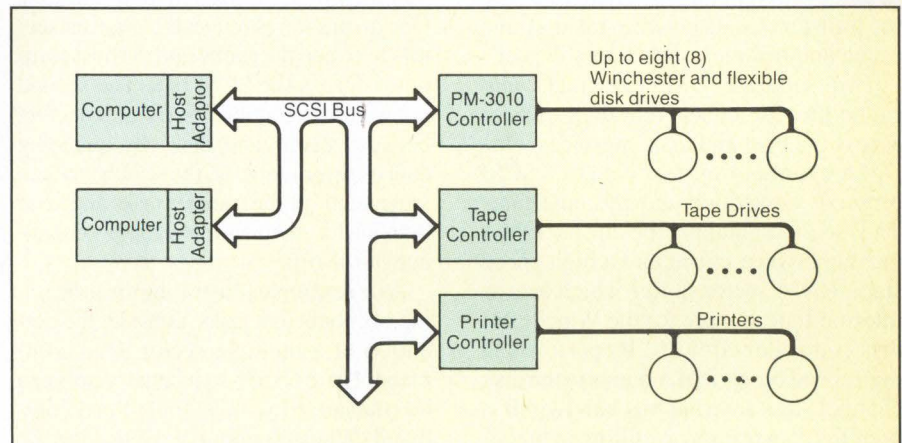


Figure 1: Up to eight devices such as disk or tape controllers, printers, communications devices, and computers can share a single SCSI bus.



COMMAND	DESCRIPTION
INQUIRY	Returns information regarding the Class of Device of the controller and attached drives.
MODE SENSE	Returns drive parameters and media format.
MODE SELECT	Sets drive parameters and media format.
READ CAPACITY	Returns size of usable media or locates areas of contiguous storage.
TEST UNIT READY	Confirms the drive is powered on and ready.
REQUEST SENSE	Returns information regarding command completion including errors and statistical reporting.
READ	Reads data from disk (and cache).
READ EXTENDED	Same as READ but supports larger address space on disk.
WRITE	Writes data to disk (and cache).
WRITE EXTENDED	Same as WRITE but supports larger address space on disk.
WRITE AND VERIFY	Writes data and then verifies CRC (or ECC) or performs byte-by-byte comparison of data.
VERIFY	Verifies CRC (or ECC) or performs byte-by-byte comparison of data with data from host.
*PRE-READ	Pre-fetches data into cache before needed by host.
REZERO UNIT	Recalibrates drive to cylinder zero.
SEEK	Moves head to desired cylinder (not mandatory).
START/STOP UNIT	Controls spindle motor and seeks head landing zone before power-down.
LOCK/UNLOCK MEDIUM	Clears cache and allows media removal.
*LOCK/UNLOCK CACHE	Allows or prevents data from being "paged out" of cache.
RESERVE	Prevents other SCSI initiators from accessing drive.
RELEASE	Allows other SCSI initiators to access drive.
FORMAT UNIT	Writes sector boundaries onto the disk. Optionally maps bad sectors and saves device parameters on media.
REASSIGN BLOCKS	Adds additional bad sectors to defect map after formatting.
SEND DIAGNOSTIC	Directs the controller to perform a self-test.
RECEIVE DIAGNOSTIC	Returns diagnostic results from self-test.

*\*vendor unique command*

Figure 2: The primary objective of the SCSI interface is to provide host computers with device independence. Since the PM-3010 supports the standard and extended SCSI command set, little or no change is required in generic SCSI software drivers in order to be compatible with the PM-3010.

sectors in cache into a tree structure and constantly rearranges the structure to minimize search time. The cache search and cache maintenance tasks run in parallel with other tasks which supervise the transfer of data between the disk and cache and between cache and the host.

Two separate DMA channels into cache provide concurrent data transfer across the host and disk interfaces. One DMA channel transfers data to a SCSI protocol controller and bus interface. The second channel performs DMA bursts between cache and a high speed static RAM sector buffer which acts as intermediate storage for the Winchester disk controller circuitry. By performing high speed block DMA bursts to the disk channel, less internal bus bandwidth is used for data transfer resulting in higher overall execution speed for the on-board 68000 microprocessor.

Two queues are used by the firmware to store requests for the two tasks which transfer sectors in and out of cache. These requests are generated by the task which searches for sectors asked for by the host. One queue stores requests to transfer sectors between the cache and the host computer across the SCSI bus. The second queue stores requests to transfer sectors between cache and disk. By queuing data transfer requests, the search task can "get ahead" of the transfer tasks and keep both DMA channels busy a large percentage of the time.

As an example illustrating the processing of concurrent tasks, consider the execution of a multiple sector Read command. Up to 65,535 sequential sectors can be transferred with a single Read command. When the command is received by the PM-3010, a cache search for the first sector in the request is immediately per-

formed. This will typically take from 100 to 250 $\mu$ sec. If the sector is found in cache, an entry is made in the SCSI Channel Request Queue, requesting the DMA channel to begin the sector transfer across the SCSI bus. As soon as the request has been added to the queue, the 68000 is free to begin the search for the next sequential sector. Since this sector sequentially follows the first sector, the search proceeds faster than the first totally random search.

Typical search times range from 10 to 50 $\mu$ sec. At a SCSI bus transfer rate of 1.0 Mbyte/sec the first sector will take a minimum of 256 $\mu$ sec to complete its transfer to the host, assuming 256 bytes per sector. By the time the transfer is complete, the cache search task will have completed several sector look-ups and will have added more entries to the queue. The next sector transfer can begin without delay.

During execution of the Read command, if one or more sectors are not found in cache, then the missing sectors must be read into cache from disk. The controller uses the second Channel Request Queue to queue up requests to the disk controller circuitry. By using queues to store internally generated requests for data transfers between disk, cache, and the host, the cache search and maintenance routines can execute concurrently with the loading of missing data into cache from disk and the transfer of cache resident data to the host. This results in zero access time for all but the first sector in multiple sector transfers. Since the search routines are faster than the data transfer, the PM-3010 can look ahead to read missing sectors into cache from the disk while cache-resident sectors are still being transferred to the host.

### Vendor Unique Commands Enhance Performance

The SCSI proposed by the ANSI Task Group X3T9.2 defines not only hardware interface standards but in addition a standardized software command set. Within this standard a command may be issued to a device controller such as the PM-3010 by sending a Command Description Block over the SCSI bus. These blocks consist of a one byte command code, followed by the parameters for that command. Although commands are standardized, certain bits have been left available for vendor unique options.

Several of the standard SCSI commands in the PM-3010 command set utilize the defined vendor unique bits to allow the selection of optional command execution modes. These options may be



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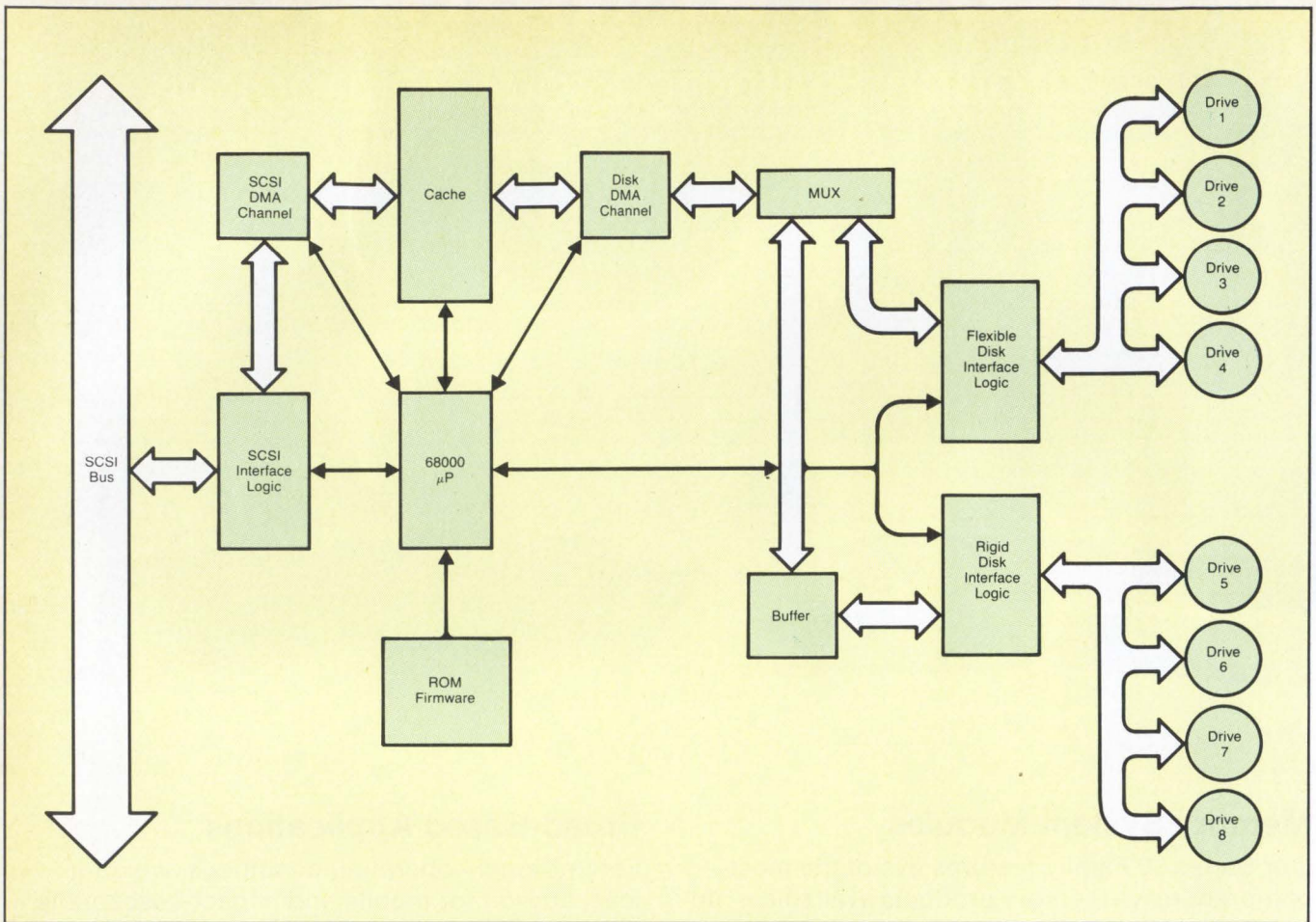


Figure 3: Two separate DMA channels into cache provide concurrent data transfers across host and disk interfaces.

used to fine-tune system performance for specific applications. Since these bits may be set to zero without degrading performance, the PM-3010 may be used with generic software with few or no software modifications required.

A vendor unique bit in the Read and Write commands allows the cache memory to be bypassed for any new sectors accessed which do not already reside in cache. This prevents the "paging out" and removal of sectors which are already cache-resident in order to make room for the new data. This option may be selected for data files which will be accessed infrequently, thereby avoiding unnecessary allocation of cache to store this data.

Another vendor unique bit in the Write command causes the controller to write all data to disk before the Write command is terminated. Normally disk writes are postponed until after command completion status has been returned and the controller has remained idle for one second. The necessary sectors are then copied back to disk starting with the least recently used sector. If another command is

received during the writes to disk, the new command will be immediately executed. When the controller again becomes idle, the writing is resumed. This allows the cache to be used to "spool" data to disk, thereby freeing up the host computer as soon as the data has been transferred into cache.

Since all sectors are immediately cached, the hit ratio for Write commands without the Write Immediate option selected is always 100%. The Write Immediate option may be selected for cases where a data recovery routine must be executed by the host computer if the disk write fails.

In addition to providing vendor unique

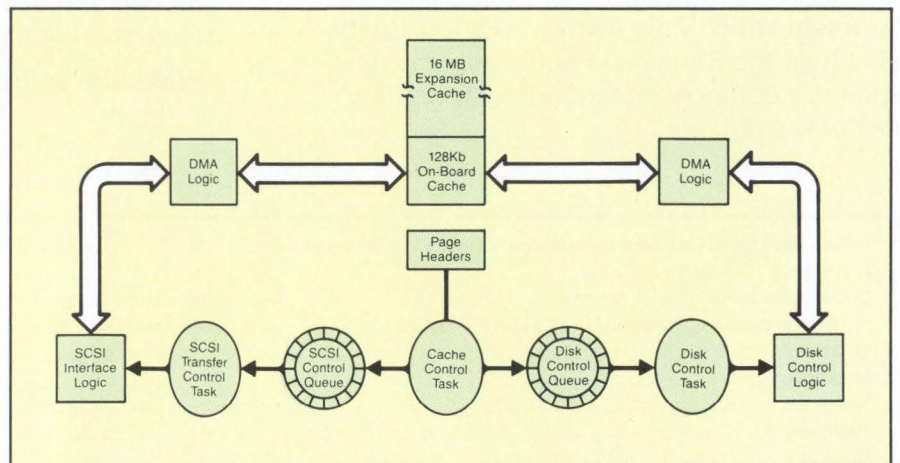


Figure 4: Concurrent execution of cache search and data transfer tasks allow these processes to be overlapped, resulting in zero access time for all but the first sector in multiple sector transfers.



bits within the standard SCSI command definitions, the SCSI specification also allows certain command codes to be used for vendor unique implementations. The vendor unique commands in the PM-3010 command set may be used to optimize controller performance for specific applications. A Lock/Unlock Cache command prevents critical sectors from being "paged out" and removed from cache. A Pre-Read command is also provided to allow data to be "pre-fetched" from the disk and loaded into cache before it is actually needed by the host computer. These commands, although not mandatory, can be used in certain applications to fine-tune system performance.

### Automatic Features Simplify Programming

To simplify software driver design, the SCSI command set uses "logical" rather than "physical" addressing. Physical drive parameters are initially specified by the host computer or in some cases, automatically sensed by the controller. When a disk is formatted, these parameters can be optionally stored in a reserved area of the disk, along with the defective sector map. Drive parameters and defect map

are then automatically loaded by the controller at power-up. Since all physical characteristics of the drive and media are known by the controller, it can assume the burden of translating logical block addresses into cylinder, head, and sector number, plus mapping defective sectors without host intervention.

The controller handles media defect mapping on a sector rather than a track level. Any reference by the host computer to a block which is known to be defective, is automatically mapped to an alternate location on the disk. The mapping is transparent to the host computer and does not require the entire track to be declared defective. The defective sector map may be augmented as additional media defects show up during normal disk utilization.

### Extensive Performance Reporting

The controller utilizes the Return Sense command defined by the SCSI specification to return optional performance statistics to the host upon request. The host has the option of limiting the Return Sense data to error reports only, or to request full performance data at any time. Information provided includes Cache Pages Utilized, Cache Pages Dirty,

Cache Hits, Cache Misses, Background Disk Accesses, Foreground Disk Accesses, Post Completion Disk Accesses, Soft Disk Error Retries, and SCSI Bus Disconnects. This data may be used to assess the results of adding more cache expansion boards to the controller or more devices to the SCSI bus. In addition, the data can be used to evaluate the need to pre-read or lock files into cache.

Diagnostics are embedded in the on-board firmware and are accessible through software command (Send Diagnostic) or by pressing a self-test pushbutton on the controller. Results are returned by software to the host computer or may be read by viewing a bank of on-board LEDs.

Caching operations will become increasingly important as disk controller manufacturers attempt to resolve some of the performance issues of computer systems. □

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# Designing With EEPROMs

*Most EEPROM applications today include some type of single chip microcontroller, so the combination of EEPROM on-board was a predictable step in the evolution of EEPROMs.*

by Dave Wilson, Executive Editor

Over the past few years, EEPROM vendors have incorporated increasing levels of functionality to allow the devices to be used in byte-wide memory sockets without support circuitry. The newest devices at the 16K density level read and write like static RAMs, even though the standard write cycle is 10ms long and only 10,000 write cycles per byte are typically allowed.

Figures 1 and 2 both illustrate the evolution of the EEPROM lineage. Figure 1 traces the development of the Exel (San Jose, CA) XL2816A EEPROM. The device integrates latches and timers, a high-voltage generator and a RAM-like interface onto the chip. Figure 2 shows the X2864A part from Xicor (Milpitas, CA).

In addition to supporting the now mandatory features of 5V operation, latched address, data and write enable inputs, automatic erase-before-write, a self-timed write operation and on-chip Vcc sensing, both page mode and data polling are supported. The Page Mode Write feature in the X2864A allows the user to write 1-16 bytes into the EEPROM on a single 5ms write cycle. The only requirement is that all the bytes reside on the same page in the device and that the bytes in the page are latched within the first 200  $\mu$ sec after the initial Write Enable. Page Mode Write reduces the time required for a complete device rewrite to a total of 2.5 seconds.

Data polling is a method for determining the completion of the internal EEPROM write cycle. Since the memory is self-timed, this is only of benefit in

those applications where time is of the essence in writing to the device. Data polling ensures that any reads to any location in the EEPROM during the 10ms write cycle will yield the complement of the data bit currently being written. Since the X2864A completes the write cycle in less than 5ms, some speed may be gained if the entire part is to be written, but the improvement in the chip write time gained through the automatic page write feature greatly overshadows any improvement that can be gained through the use of data polling.

Page mode is also supported by Exel's XL48C64, an 8K  $\times$  8 CMOS EEPROM. Here, a 32-byte static register is available on chip which is not subject to the normal EEPROM write cycle endurance limitations, yet is written just like a static RAM. The page mode function, which is initiated through a normal microprocessor write cycle, copies all of the data from

this register into non-volatile storage in a worst case 10ms. Since the register may be updated frequently and is written into EEPROM only on command, it can be used to store current vital parameters such as pointers, stack data, and vector information.

The XL48C64 has also solved the problem of inadvertent or false writes during power transient situations. One of the status word registers is used to control operation of the on-chip charge pump, used for boosting the internal programming voltage from 5 to 20V.

During power up, the charge pump enable bits in the status word are initialized in the disabled state so that write operations are not possible. To allow write operations, the status word register must be written with a specific data pattern and to access this register, a specific address must be on the address pins. Hence, virtually all the pins on the device must be set to a specific combination of levels for a false write to affect this register. Although the probability of a false write in systems without protection mechanisms is not great, the status word approach reduces that probability further.

Recently EEPROM has begun to find its way onto microcomputers. The first part to incorporate the technology was the Seeq (San Jose, CA) 72710, but since then others have followed suit. The Motorola MC68HC11A8, for example, contains RAM, ROM and A/D converter, serial and parallel ports as well as 256 bytes of

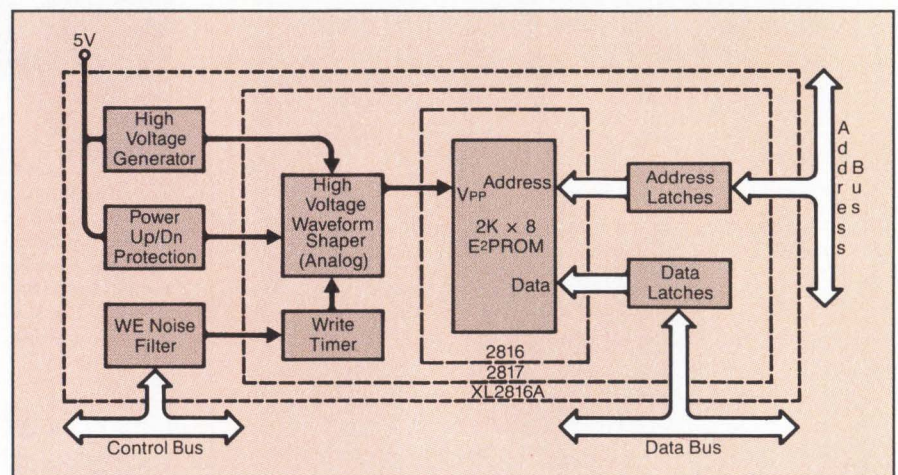


Figure 1: The development of the Exel XL2816A EEPROM.



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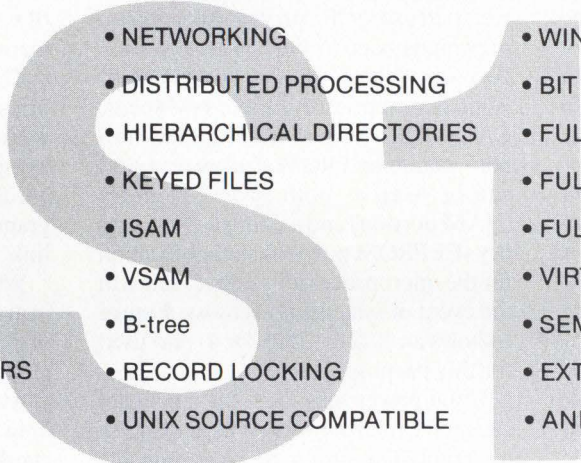
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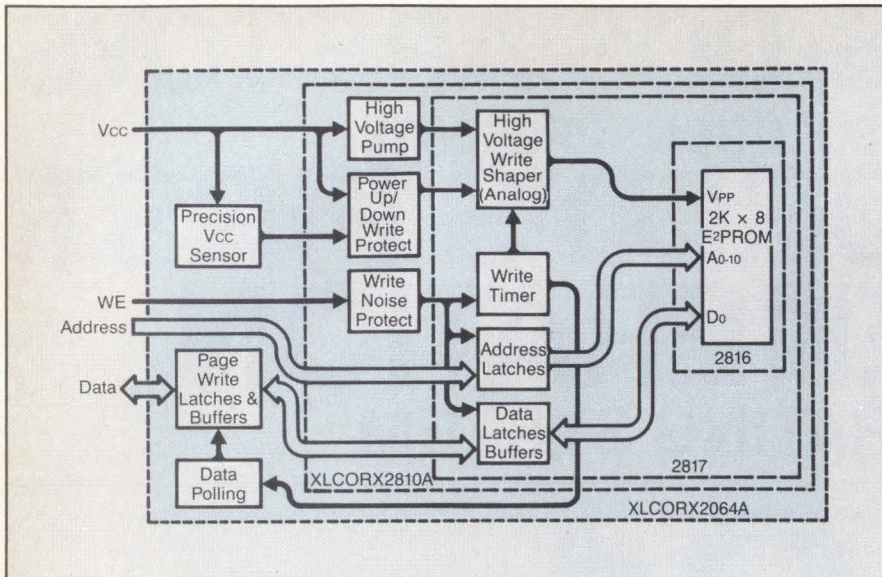


Figure 2: The development of the Xicor X2864A part.

EEPROM memory.

In the Seeq part the  $2K \times 8$  on-board EEPROM can be programmed via the processor itself or under external control as if it were a standard 5V EEPROM. An expansion mode allows the EEPROM to be easily expanded off-chip. A security lock mechanism in the EEPROM memory allows the users' program to inhibit external access to its proprietary program code. Once activated, this lock can be reset only by an external EEPROM block clear operation which erases the entire memory.

Putting UV EPROM on a micro is at present the most often used alternative. Unfortunately, it suffers from the fact that it must be removed for its contents to be altered, unlike the EEPROM approach.

More important, however, is the designers familiarity with the instruction set of the microprocessor. His investment in design and development tools is also a key consideration when selecting a microcomputer. Unfortunately, in many cases the fact that a particular micro may have on-board EEPROM memory may be a secondary or tertiary consideration.

## Applications

One of the most rudimentary applications for the EEPROM is the non-volatile counter which simply counts events and maintains the count with no power applied. Automotive odometers and video game score tables are all currently manufactured using EEPROMs.

In the event of power failure, many industrial controllers must be stopped and restarted at specific program locations to prevent damage to work in process or to the users of the machinery under control. In such an application Xicor's (Milpitas, CA) NOVRAM (a RAM overlaid with a non-volatile EEPROM shadow memory) can be used as both system memory (RAM portion) and a non-volatile memory (EEPROM portion) storage location for the microprocessor program status in the event of systems power loss. **Figure 3** shows an X2212 ( $256K \times 4$ ) part used for this purpose.

Upon power loss, a power fail signal causes the microprocessor to generate an interrupt. The system memory contents and the  $\mu P$  stack, which are both in the RAM portion of NOVRAM, are then stored on the non-volatile EEPROM portion of the NOVRAM. Upon return of power, power on/reset also generates a recall at the NOVRAM. A power-on routine verifies that an interrupt did occur at power loss and a return from interrupt is performed, returning the program to a known function.

EEPROM devices have also found use in applications previously requiring analog design techniques. One, is the basic digitally controlled analog calibrator. Here, functions formerly performed by a potentiometer may be provided by a digital-to-analog converter and fine tuning can be achieved by modifying the corresponding EEPROM data. Through this

means, analog circuit drift is compensated and system mechanical wear can be offset. New calibration constants can be stored in the EEPROM and used in the closed-loop control algorithm. Products which include potentiometer adjustments before delivery may encounter great manufacturing time and expense reductions when converted to high speed digital calibration designs.

## EEPROMs and Microcomputers

Most EEPROM applications today include some type of single-chip microcontroller, so the combination of EEPROM on-board was a predictable step in the evolution of EEPROM. There are several unique features which a microcomputer with its data and/or program memory implemented in EEPROM can provide.

Many systems are evolving today that are able to adjust their own program memory to adapt to environmental changes or to optimize their algorithms for specialized applications. EEPROM program memory allows the creation of adaptive algorithms otherwise not possible with RAM or volatile control memory.

The combination of non-volatile features coupled with CMOS technology will allow microcontroller products to be completely sealed for environmental or security reasons, yet be easily reprogrammed locally over a communications link.

When all program code exists on-chip, instructions do not appear on the I/O pins of the processor. This makes the code externally invisible.

Also, when instruction fetches occur only from on-chip memory, instructions cannot be forced on the processor externally, causing it to dump the contents of the internal registers or memory.

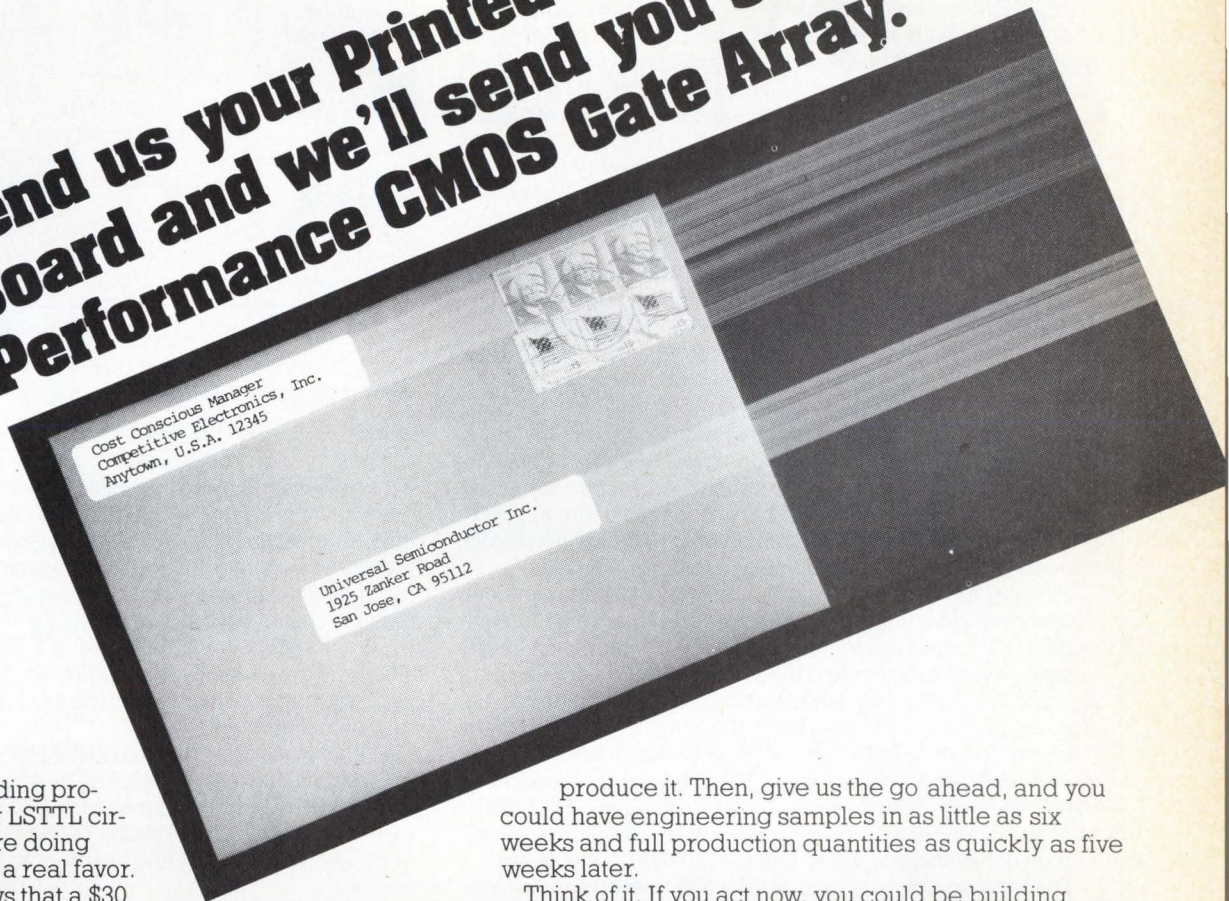
Seeq's 72710, for example, provides for security with an option that will lock the processor in a single-chip mode, preventing external access, but allowing the processor read/write access to all memory including EEPROM.

## Conclusion

Many of the early problems suffered by EEPROMs, such as long write and access times, have been solved by today's newer devices. Despite these, design alternatives exist that have kept the EEPROM out of a number of sockets; CMOS with battery back-up, UV EPROM, bubble memory or cards with



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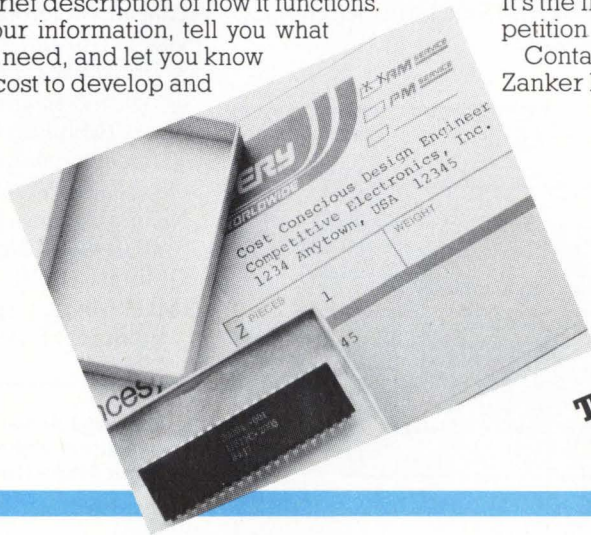
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# Micro Memory Alternatives

UV EPROM is currently the most often used method of putting alterable non-volatile memory on a microprocessor. Although the on-chip EPROM provides program prototyping freedom and can provide data security, it must be removed for its contents to be altered, and it fails to save the microprocessor's status during power down. In addition, it is not self adaptive because UV light must be used to erase memory.

Using non-volatile RAM backs up the microprocessor's internal RAM memory with EEPROM to create non-volatile RAM on the micro. Each time the processor is powered down, the RAM contents are copied into the EEPROM, and each time it is powered up, the RAM contents are restored from EEPROM. This combination allows continuity of CPU status and system initialization constants through power interruptions and provides a limited amount of data logging capability. The major disadvantage of the non-volatile RAM is the high cost per bit, since each bit requires both an EEPROM and a dedicated static RAM cell. The on-chip EEPROM approach is less costly because a one-to-one correspondence of EEPROM to RAM is not necessary. Because of the high per bit cost, non-volatile RAMs in single-chip micros will typically be limited to a few hundred bytes or less.

In very high volume/low cost applications, it makes economic sense to implement only a portion of program memory in EEPROM, with the remainder in ROM. A reduction in device and system flexibility is the price that must be paid. Storage of initialization constants and limited data logging can be accomplished, but if in-circuit or remote reprogrammability is to be implemented, the decisions as to which code is to be stored in ROM and which in EEPROM must be made very carefully. Most of the code security provided by EEPROM is forfeited when ROM is substituted, since ROM data patterns can be determined visually, while EEPROM data cannot.

The most complete approach is to implement the entire program memory of the micro in EEPROM memory. In this case,

Single Chip Microcomputer with:	Prototyping	Power Down Status Save	Self Adaptive Code	Data Logging	Initialization Constants	In Circuit or Remote Reprogrammable	Code Security
EPROM Program Memory	✓						✓
Non-volatile RAM		✓		✓	✓		
ROM/EEPROM Program Memory				✓	✓	Partial	
EEPROM Program Memory	✓		✓	✓	✓	✓	✓

Table 1—Attributes and applications of EEPROM technology compared with alternate methods of implementing non-volatile memory on a single-chip microcomputer.

if the processor is given the ability to write to its EEPROM program memory it gains self-adaptive as well as security capabilities. Any portion of this EEPROM memory that is not used for the storage of program code can be used as slow write/fast read non-volatile data memory for storing initialization or calibration constants or logging data. The major disadvantage of this approach is the higher cost of EEPROM compared to ROM and the relatively slow write time (1-10 ms) of EEPROM vs. RAM memory which limits the amount of data which can be stored if power is lost.

The future will see the cost of EEPROM single-chip micros approaching that of current EPROM-based micros. Expect to see EEPROM write times measured in microseconds, rather than milliseconds, significantly closing the price/performance gap between EEPROM and the other approaches described above.

—Larry Goss, Seeq Technology  
Write 304

magnetic strips. Higher speed, extended durability and faster write times of the EEPROM will be key to the growth of the market in the future.

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From papers delivered at Electro '84.

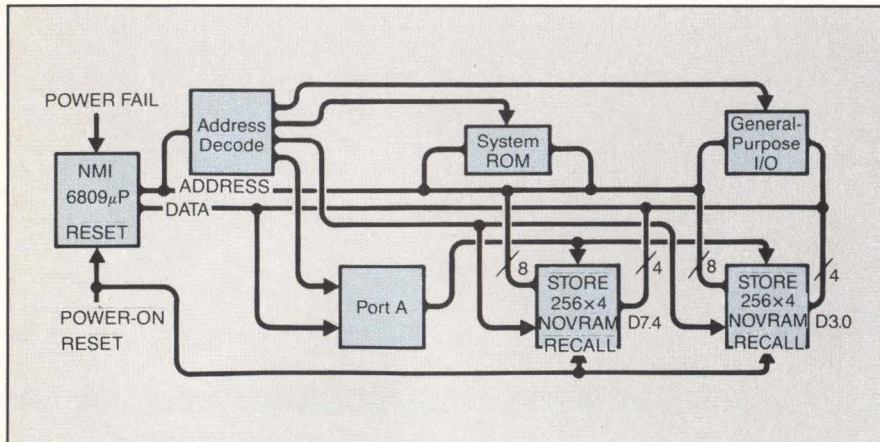


Figure 3: Use of Xicor's NOVDRAM in an industrial application.

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## Build A Cost-Effective EPROM Programmer With The Z8

The first thing mentioned in many design labs is the desire to have quick, easy EPROM programming capability. One of many applications for the Z8 microcomputer is as an EPROM programmer on a small board.

The Z8 has an internal UART and two counter/timers. One counter/timer is used with an external crystal; when a 7.3728 MHz crystal is used, the counter/timers generate any one of the nine lower bit rates from 110 through 19,200.

The Z8 has four 8-bit multifunction ports that can be programmed to change modes during operation. Port 3 has four multifunction inputs and outputs. The four inputs can generate interrupts on signal edges from external devices or act as inputs for the internal counters and perform functions such as counting gates for timers. One input on this port is used as the UART input and output.

One unique feature of the Z8 is that it allows individual interrupts to be enabled and disabled. This comes in handy for application in an EPROM programmer.

### Need For An EPROM Programmer

The original idea for this application was to allow engineers to program EPROMs at home without purchasing a \$3,500 PROM programmer. Commercial programmers also require software to be written for up/down loading to a host. Making use of very few low-cost materials to replace the commercial system, PROM programming hardware and software can be ready in less than a day. This can be done using any system with a C compiler, including the IBM PC, any CP/M system with C and, in this case, the UNIX-based Zilog System 8000.

### Hardware Layout

The first design used a 3870, but was very slow. The 3870 has no serial port, and with multiplexing, the maximum speed was supposed to be 2400 baud. In fact, the best usable speed was 1200 baud. With the Z8 serial capability, a bit rate of 19.2 is easily attained.

As shown in **Figure 3**, the interface between the Z8 and external circuitry is straightforward and simple. There are only four chips and it is almost impossible to assemble them incorrectly.

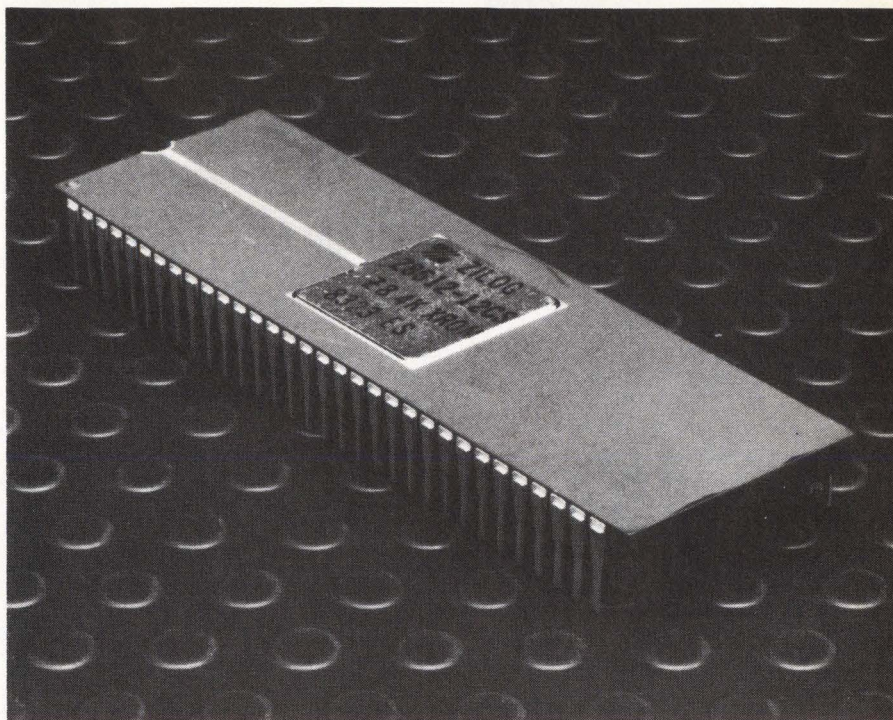


Figure 1: The Z8 4K MCU.

List of Materials and Cost			
Quantity	Description	Price Each	Total
1	28-Pin Zero Insertion Force Socket (ZIF)		\$ 9.00
1	8603 Z8		60.00
1	1488		.70
1	1489		.70
1	2N 2222		.25
1	2N 5227		.25
1	TL 497 (Voltage Reg) ANC	3.25	
1	Single Throw Single Pull (STSP) Switch Pack		.40
5	1K Resistors	.025	.125
1	510 Ohm Resistor		.025
1	4.7 Resistor		.025
1	20K Resistor		.025
1	0.5 Ohm Resistor—1 Watt		.025
1	5K Trimpot		2.00
1	50 MicroHenry Inductor		3.00
1	4" x 8" Vector Board		1.00
2	10 pF Capacitors	.05	.10
1	2.2 mF Capacitor		.50
4	0.1 mF Capacitors	.15	.60
2	10 mF Capacitors—35 Volt Tantalum	1.00	2.00
1	100 pF Capacitor		.05
1	LED—Your Choice		.20
1	Switch Pack—4-Switch On/Off		.85
1	7.3728		3.00
<b>Total</b>			<b>\$88.125</b>

The above parts can be found at Anchor or JDR Microdevices.

Figure 2: List of materials and costs for an EPROM programmer.



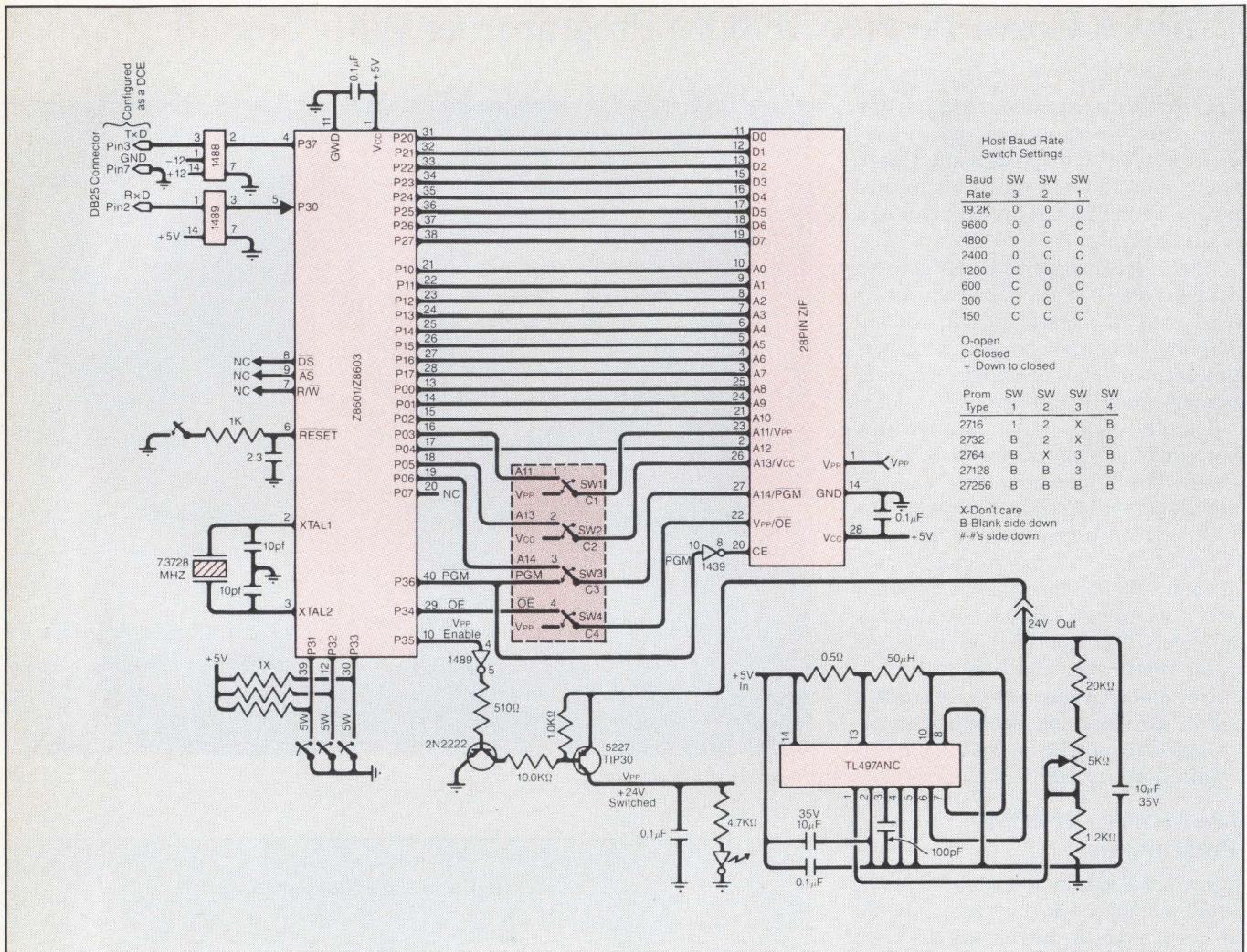


Figure 3: Schematic of board for Z8 EPROM programmer.

## Programming

The only software needed in this system is the Z8 source code to allow actual programming of the EPROM and the C source code to the driver routine, for communication between the host computer and the board.

In the Z8 source code program, the general constants are defined to address the Z8, then the register locations are declared. The interrupt vector entry points are set, and initialization is programmed. Initialization routines are usually short and available in documentation supplied with the software. The baud switches should then be checked and timer 0 is set for the correct bit rate. The actual command interpreter routine then begins.

Next the PROM type is selected and the

send/receive routine takes over if the System 8000 is the host. This could be replaced by the Intel or Tek Hex routine. A PROM blank check is performed; then, the Program PROM, Read PROM or Burn PROM routine is selected. The balance of the code is a series of modules for Delay, Send/Receive Serial Characters, conversion of ASCII-Hex to Binary, and Binary to ASCII. The final section contains messages and tables including the serial bit rates.

Code can also be written in the C source to the driver routine, or any language understood by the host computer. C is a universal language, but a copy of the Basic code is included for those who do not have a C compiler.

The C program is a routine to drive the Qume 102A and the Z8 EPROM programmer. The first modules contain the

command parser for the main menu and the special terminal driver routines possible on the Qume: clear to end of screen, reverse video, blinking, underline, graphics mode vertical and horizontal lines, use of auxiliary port and transparent mode. Next is the EPROM Programmer Utility that displays all instructions on the screen: display modification of memory, copy, selection of PROM type. The user is then instructed to place a blank PROM into the socket and give the command to write.

If the driver is written in C, neither Tek or Intel Hex presents a problem for up/downloading, since communication is handled within the language. There are advantages to either format. In most sources, a format written specifically for each program is used. This usually has a speed advantage over standards.



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## Transmission Protocols

Tektronix Hex format:

```
/ <load address> <byte count>
<checksum1> <data field...>
<checksum2> <cr>
```

Tek Hex requires acknowledgement from the receiving device before the next block can be sent. The three possible acknowledgements are:

0 <cr> - data block was received without error

7 <cr> - block was received with bad

checksums, please retransmit the last block

9 <cr> - bad load address or sector message received, abort process.

Intel Hex format:

```
: <byte count> <load address> <type field>
<data field...> <checksum>
```

Intel Hex does not provide for error retransmission or acknowledgement. A type field of 00 is a data block and the 01 is an End-of-Record field. The byte count contains the total number of bytes trans-

ferred in each record including the SOR: the load address, type field, byte count, data field and the checksum, giving a value of  $(2 * L) + 11$ . Both Intel and Tek Hex send all information as ASCII encoded characters.

## Conclusion

A Z8 and a few added pieces of hardware can be put together in less than a day to create a useful and cost-effective EPROM programmer. The alternative is a rather expensive system for occasional use.

- Dr. T.M. VendenHeede, Zilog, Inc.

Write 234

## Multibus II Parallel System Bus - An Inside Look

The iPSB (Parallel System Bus) of the Multibus II architecture standardizes not only hardware data transfer, but software inter-module communication. It is a synchronous bus, with protocols implemented as state machines. The use of multiplexed signal lines on the iPSB allows the entire 32-bit interface to be contained in a 96-pin connector (Figure 1).

Operations performed by the iPSB are referred to as cycles. Arbitration cycles are used by agents requesting use of the iPSB bus to resolve contention. Transfer cycles are performed by the requesting agent to exchange information with a replying agent or agents. In the event of an error, an exception cycle reports the error and resets the bus for further operation. As shown in Figure 2, the three iPSB cycles are overlapped, maximizing the use of the bus resource.

### Arbitration Cycles

When conducting an arbitration cycle, the agent drives its arbitration ID onto the ARB5\* through ARB0\* signal lines, and signals its request by driving the BREQ\* signal line low. Three bus clocks later, the agent samples the ARB5\* through ARB0\* lines. If the ID on those OR-tied lines matches its ID, that agent has "won" the arbitration and performs transfer cycles on the bus at the next available opportunity.

The bus supports two modes of arbitration: no starvation, and strict priority. These are selected dynamically for each arbitration cycle. In no starvation mode, each agent must wait until all pending requests for the bus are satisfied before starting an arbitration cycle. In strict

Connector Pin Number	Row A	Row B	Row C
1	0 Volts	PROT*	0 Volts
2	+5 Volts	DCLW*	+5 Volts
3	+12 Volts	+5 Battery	+12 Volts
4	Reserved (note 1)	SDA (note 3)	BCLK*
5	TIMOUT*	SDB (note 3)	0 Volts
6	LACHn*(note 2)	Ground	0 CLK*
7	AD00*	AD01*	0 Volts
8	AD02*	0 Volts	AD03*
9	AD04*	AD05*	AD06*
10	AD07*	+5 Volts	PAR0*
11	AD08*	AD09*	AD10*
12	AD11*	+5 Volts	AD12*
13	AD13*	AD14*	AD15*
14	PAR1*	0 Volts	AD16*
15	AD17*	AD18*	AD19*
16	AD20*	0 Volts	AD21*
17	AD22*	AD23*	PAR3*
18	AD24*	0 Volts	AD25*
19	AD26*	AD27*	AD28*
20	AD29*	0 Volts	AD30*
21	AD31*	Reserved	PAR3*
22	+5 Volts	+5 Volts	Reserved
23	BREQ*	RST*	BUSERR*
24	ARB5*	+5 Volts	ARB4*
25	ARB3*	RSTNC*	ARB2*
26	ARB1*	0 Volts	ARB0*
27	SC9*	SC8*	SC7*
28	SC6*	0 Volts	SC5*
29	SC4*	SC3*	SC2*
30	-12 Volts	+5 Battery	-12 Volts
31	+5 Volts	SC1*	+5 Volts
32	0 Volts	SC0*	0 Volts

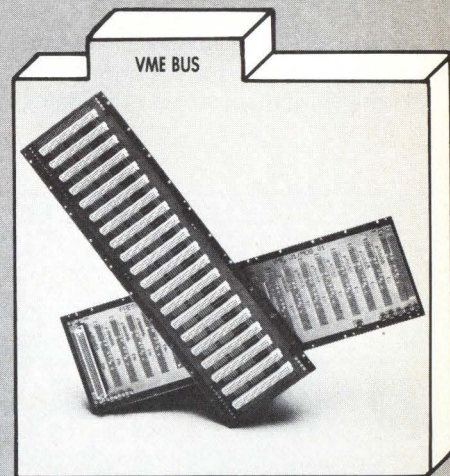
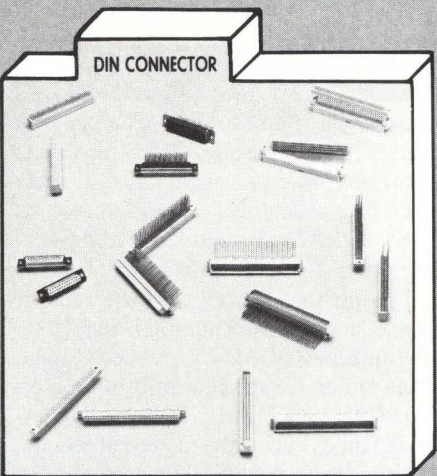
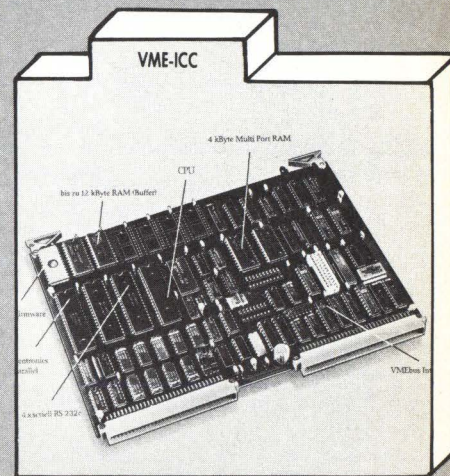
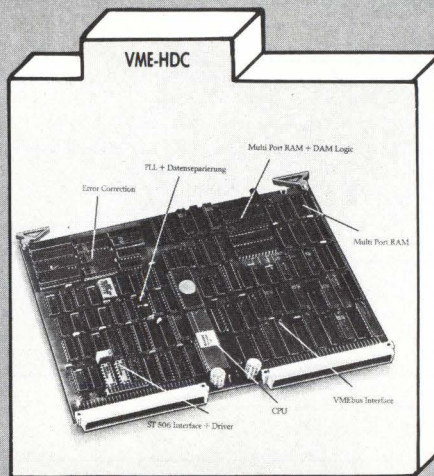
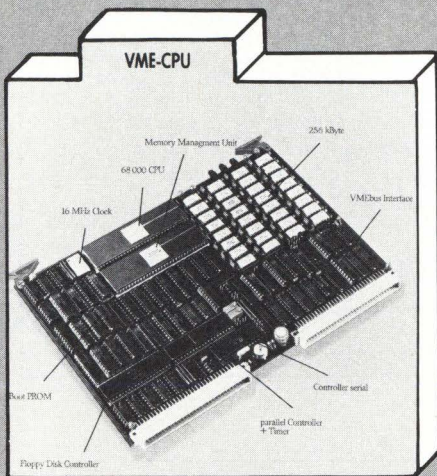
#### Notes:

1. Slot 0: Second BCLK\* driver for systems containing more slots; drives BCLK\* (pin 4C) to left half of backplane. Slot 1-19: 0 volts.
2. Slot 0: Second CCLK\* driver for systems containing more slots; drives CCLK\* (pin 6C) to left half of backplane. Slot 1-19: LACHn\*.
3. Signal lines SDA and SDB are reserved for the Serial System.

Figure 1: Parallel system bus connector pinout.



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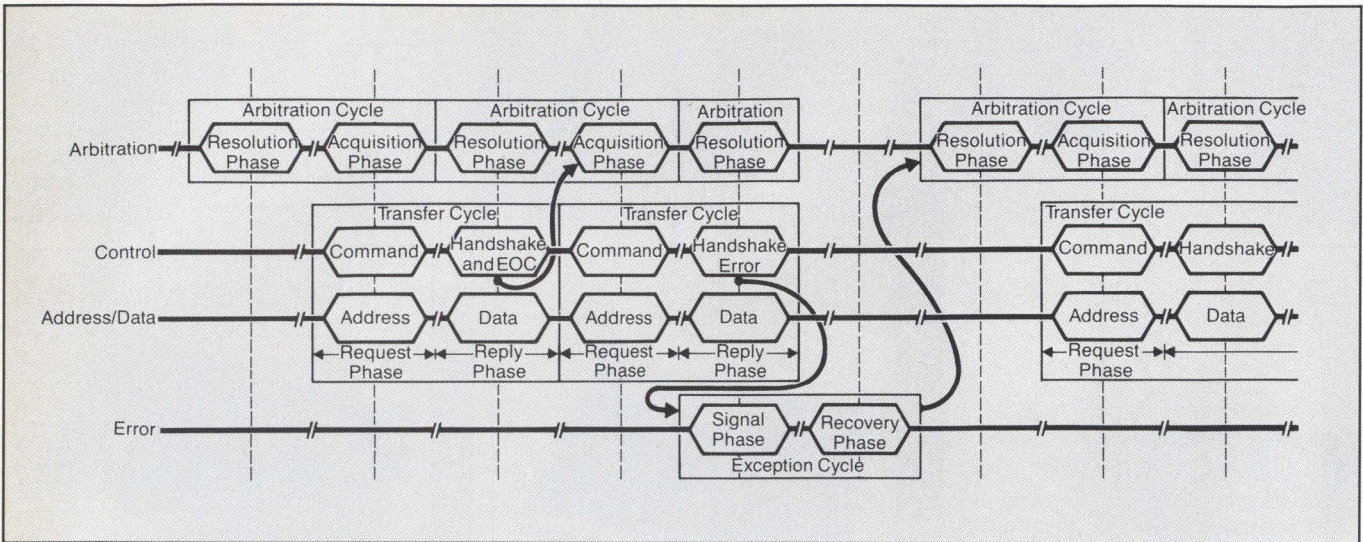


Figure 2: Block diagram of bus cycle operation with errors.

priority mode, an agent starts in the arbitration cycle at the first opportunity. In either mode, if there are no outstanding

requests for the use of the bus, the agent last granted use of it remains the current bus owner.

## Transfer Cycles

Transfer cycles are divided into two phases, the request and the reply. All transfer cycles on the iPSB are parity-protected. Even parity is generated on each byte of address or data, as well as over the SC7\* through SC4\* and SC3\* through SC0\* control signal lines.

During the one clock long request phase, address information is placed on the multiplexed AD31\* - ADO\* signal lines and the command information on the SC9\* - SCO\* lines. There are two encoded fields during the request phase, the transfer width and the address space. The iPSB supports transfer widths of eight, 16, 24 and 32 bits. The bus also accommodates four address spaces: memory, I/O, interconnect and message.

During the reply phase of the transfer cycle, data is transferred on the AD31\* through ADO\* lines at a time mutually agreed upon by the requesting and replying agents. The SC9\* - SCO\* lines are used for handshake or indication that data is valid on the iPSB bus. One or more handshakes may occur during the reply phase. A handshake is indicated by simultaneous assertion of SC4\* by the replying agent and SC3\* by the requesting agent.

The supplier of data, (requesting agent for write operations or the replying agent for read operations) asserts the corresponding handshake signal when data is valid on the bus. The recipient of the data asserts its portion of the handshake when

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ready to accept the data from the bus. The assertion of SC2\* coincident with the handshake event signals the end of the transfer cycle. Broadcast operations are also supported on the iPSB.

Replying agents can signal a number of errors during the reply phase. Error signals can be used by the requesting agent for recovery. These are called agent errors, and force termination of the current transfer cycle without effecting the arbitration cycle in progress.

## Exception Cycles

There are two signals on the iPSB which, when asserted, initiate an exception cycle: BUSERR\* and TIMOUT\*. BUSERR\* is an indication of a detected parity error during a transfer cycle. TIMOUT\* is driven by the CSM to indicate that an agent has taken too long to respond with its portion of the handshake event during the transfer cycle. The iPSB reaction to either type of exception is the same: halt all cycles in progress and restart bus operation after a short delay.

## Architectural Features

Architectural enhancements of the iPSB can be seen in the uses of the four address spaces supported: memory, I/O, interconnect and message. Memory and I/O spaces have much the same function as they do in today's bus structures. This is important for migration from existing environments to the iPSB. These address spaces have been expanded to satisfy the needs of future 32-bit processors, to 32 bits (4 Gbytes) for memory space and 16 bits for I/O.

The use of interconnect space has no precedent in current bus structures. Interconnect space has three purposes: 1) Identify the particular board in the addressed slot, 2) Configure the board from the iPSB, and 3) Provide a standard interface for diagnostic commands.

To accomplish these goals, the interconnect space address consists of a 5-bit slot address and a 9-bit register number. The 5-bit slot address, from 0 to 19 decimal, identifies a single card slot in the iPSB backplane. The register number selects an entry into a defined template. Each bus agent must respond when the interconnect address refers to its slot. Some of the registers in the template identify the

board specifically (e.g. 512 Kbyte RAM board). Additional registers configure the board and communicate with diagnostic firmware resident on the board.

Message space on the iPSB standardizes interprocessor communication. At its simplest, message space provides an interrupt capability equivalent to 65,000 interrupt signal lines. When message space protocols are fully utilized, parametric interrupts and negotiated data movement are supported.

In current system buses, drivers must be written specifically for intelligent controllers used to perform the operation. Therefore, the standard for inter-processor communication is set by the implementation of the controller. In the Multibus II, transportability of system software is insured by the iPSB protocol, even if implementations change. System software may be transported from the iPSB to a low cost serial implementation on the iSSB (Serial System Bus) of the Multibus II or vice versa.

## Physical Bus Characteristics

The connector used for the iPSB is the standard EuroCard DIN 41612 connector. The 233.4 × 220 mm board outline also allows single height versions.

Electrically, the iPSB bus is driven with standard, multiple-sourced TTL components, using both three-state and open collector devices. All state machines can be implemented using available programmable logic. Up to 20 boards may be installed on the iPSB bus. The terminated backplane of the iPSB bus supplies power voltages of +5, -12 and +12 volts.

## Foundation for the Future

Multiple processors in the system pose great difficulties for hardware and software. The iPSB hardware provides high bandwidth in a multiple processor environment. The bus also provides a standard interface on which software can be built to solve multiprocessing problems.

—*Scott Tetrick, Senior Engineer, Bus Architectures, OEM Microcomputer Operation, Intel Corporation*

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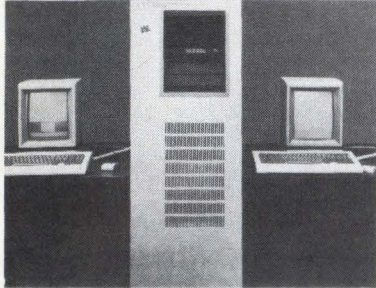
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## THREE PROCESSOR LISP MACHINE



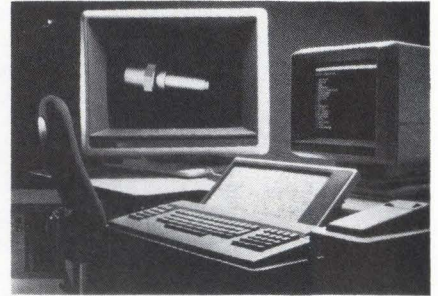
The Lambda 2x2/Plus LISP machine supports the development or execution of LISP, Prolog and UNIX software simultaneously on three

independent, concurrently-executing processors. The machine features two LISP processors and a 68010 processor and is supplied with two displays and AI keyboards, and a 474 Mbyte Winchester disk. Software supplied with the system includes ZETALISP-PLUS for the 68010. Optional 8- and 16-port RS-232 terminal interfaces are available for multi-user UNIX operation. Also included is the Extended-STREAMS Interface, which allows 37.5 Mbyte/sec communication between programs on any or all of the three processors in the 2x2/PLUS during parallel operation. Price is \$140,000. **Lisp Machine, Inc.**, Los Angeles, CA

**Write 219**

11/730 running VMS and is supported by Tektronix 4107, 4190 or 4115 Computer Display Terminals. Price is \$50,000. **VR Information Systems**, Austin, TX **Write 137**

## MODULAR GRAPHICS WORKSTATION



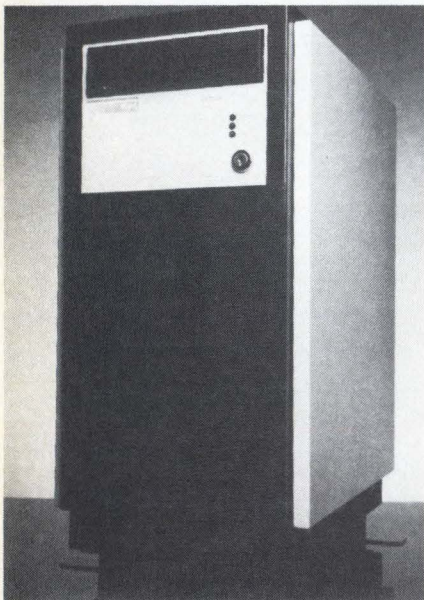
The AGW III is based on the Apollo 32-bit CPU. The processor operates as a true 32-bit unit using bit slice technology and has a floating point processor and cache memory units. Hardware features include a 19" graphics screen, 12" alphanumeric screen, keyboard, and thumbwheel or joystick module. The CPU has 1 to 4 Mbytes of main memory. A 68 or 158 Mbyte Winchester disk drive and 1.2 Mbyte floppy disk drive comes with the system. **Auto-trol Technology Corp.**, Denver, CO

**Write 153**

## ETHERNET SYSTEM

The Ethernet local area network (LAN) System from SGS Semiconductor meets the Ethernet specification of up to a 10-Mbit/sec transfer rate and a 16-bit dedicated CPU, with 128 Kbytes of on-board RAM for message buffering and high-level protocol software. The hardware has 32 variable-length receive buffers chained and up to 60 Kbytes available for packet buffering. **SGS Semiconductor Corp.**, Phoenix, AZ **Write 133**

## UNIX-BASED DEVELOPMENT SYSTEM



The DSM-6816 is a VMEbus development system which runs under the UNIX operating system, providing a multi-user environment. The DSM-6816 uses the 68000 microprocessor with the 68451 MMU. Features include 768 Kbytes of RAM with parity resident on the CPU board, expandable to 3.8 Mbytes; a 20 Mbyte hard disk and a 1.2 Mbyte 8" floppy disk drive. Two serial console channels, a serial printer port, an intelligent disk/printer controller and six spare card slots are also standard. Price is \$16,575. **dy-4 Systems, Inc.**, Ottawa, Ont.

**Write 149**

## IBM PC COMPATIBLE DAS



The ISAAC 41-I and 91-I add extension expansion capabilities to the IBM PC for data acquisition and control applications. The ISAAC 91-I is a general purpose computer/interface system designed for workstation applications, while the ISAAC 41-I is a building-block solution for applications not requiring full 91-I capabilities. Both systems offer I/O capabilities for direct interfacing with thermocouples, pressure transducers and other analytical and industrial instruments. **Cyborg Corp.**, Newton, MA **Write 148**

## VME-BASED 32-BIT SUPERMICRO

The Universe 2203 32-bit supermicro computer and its unbundled central processor, the VCP2000, were designed to run programs developed under UNIX or UNIX compatible operating systems. Both computers use the 12.5 MHz Motorola 68000 microprocessor, and both are built around the VME bus. The Universe 2203 has a 4 Kbyte cache memory, memory allocation and protection, and a 35 Mbyte Winchester disk. Price is \$15,000 to \$20,000. The VCP 2000 is \$4,000. **Charles River Data Systems**, Framingham, MA **Write 136**

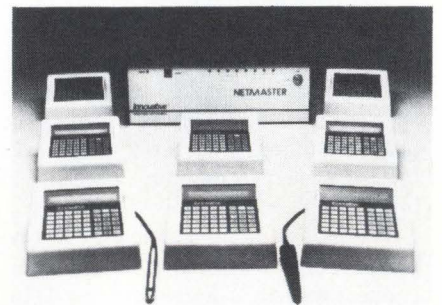
## PCB DESIGN SYSTEM

Merlyn-PCB is a PCB design system that performs hierarchical schematic capture, automatic component placement, automatic circuit routing and interactive editing, and real-time design rule checking in the layout of printed circuit boards. Merlyn-PCB is available for use with the VAX-11/780, -11/750 and

## SUPERCOMPUTER

The AS/91X0 series are five IBM mainframe-compatible supercomputers designed to handle vector-processing applications. The AS/91X0 entry-level supercomputer series can perform typically at 28 Mflops and is field upgradable. The computers include a software tool called VAST which looks for operations it can vectorize, inserting appropriate code to activate the vector-processing hardware. Prices are \$2.1 to \$5 million. **National Advanced Systems**, Mountain View, CA **Write 143**

## DATA COLLECTION SYSTEM



The Innovative Factory Data Collection System is a microcomputer based data acquisition/supervision system. The system operates in two configurations: standalone or with a host computer. Hardware components include the Netmaster CPU, disk drive, terminals and peripherals. The software includes a standard operating system, a data collection subsystem, transactor process routines, and a host communications subsystem. **Innovative Electronics, Inc.**, Miami, FL **Write 147**

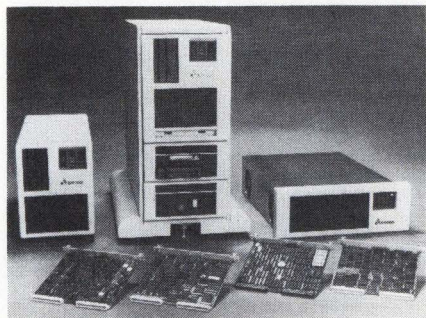
## SIMULATION SOFTWARE

LASAR Version 6.1, an update on Lasar logic simulation software, incorporates new algorithms for signal state and current strength analysis. The simulator propagates ten nodal values made up of



combinations of the four logic states that can physically exist at a node. For evaluation of wired net circuit nodes, minimum and maximum drive currents for logic states 1 and 0 can be specified for each gate. Price is \$10,000 to \$225,000. **Teradyne, Inc.**, Tempe, AZ **Write 138**

## SUPERMICROCOMPUTERS



TARCH is a 32-bit architecture developed by Argonne Systems for the MCP series of supermicrocomputers. The multiple-coupled processor includes 16 Kbytes of cache memory and the Multi-bus II as the main system bus with data transfer rates up to 40 Mbytes/sec. Processors can be coupled in variety of ways: tightly coupled, running a single copy of an operating system; closely coupled, running different operating systems, and loosely coupled, with distributed systems. Prices start at \$11,000. **Argonne Systems, Inc.**, Sugarland, TX **Write 135**

## SCHEMATIC DESIGN SOFTWARE

SDS Version 5 software is designed for Silvar-Lisco's SL-2000 portable CAD/CAE system. The software offers multi-windowing, search features, a symbol editor, automatic schematic scaling, and component dragging. Each window may overlap and display a different schematic drawing, and users can edit schematics within any window currently displayed. Local vector lists provide a listing of component input and output pins and signals. Price is \$14,000 to \$35,000. **Silvar-Lisco**, Menlo Park, CA **Write 140**

## WORKSTATIONS

The Astra 300 series of minicomputers utilize a 10 MHz, NEC 32-bit VLSI microprocessor and have diagnostic capabilities. All have a one Mbyte floppy disk drive. Features include terminal emulators such as 3278, 3780 and 3740 bisynchronous polling capabilities, and X-25 product processing. Color or monochrome workstations are used with the Astra 300 Series, which have 128 Kbyte RAM and 4 Kbyte of ROM. Prices range from \$15,000 to \$20,000. **NEC Information Systems, Inc.**, Boxborough, MA **Write 141**

## POWER CONDITIONER

The Z-Phase Line Tamer power conditioner is designed for three-phase applications for both line-to-line and line-to-neutral loads. The Line Tamers are used primarily for loads from 7.5 kVA through 75 kVA. Line-to-line regulation is  $\pm 5\%$  over a regulating range of +10, -20%, with load unbalances of 30% of the average of the total load. Line-to-line regulation with load unbalances of up to 75% of the average of the total load is +7%. Price ranges from \$3,400 to \$24,000. **Shape Magnetronics, Inc.**, Lombard, IL **Write 215**

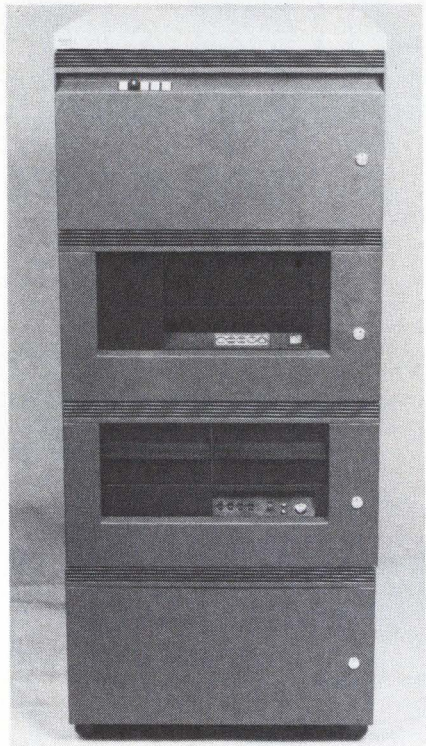
## CAE WORKSTATION

The CDX-9000 CAE Workstation offers HHB Softron's CADAT 12-state logic simulation and fault simulation packages for logic verification and test development. The workstation has 16 transistor models, 95 logic primitives and a library of TTL, CMOS and ECL devices. The CDX-9000 contains a 32-bit CPU, 1 Mbyte of RAM, an 814 Kbyte 5 1/4" floppy disk drive, a 35 Mbyte Winchester disk, 17" monitor, keyboard and mouse. Price is \$36,500. **Cadnetix Corp.**, Boulder, CO **Write 146**

## DATA COMMUNICATIONS SOFTWARE

MacTerminal is a data communications software package that allows the Macintosh personal computer to interact with mainframe and minicomputers as well as commercial electronic information services. It has a visual user interface, integration between applications, a mouse, and the ability to view multiple objects on the screen. A file transfer capability facilitates the transfer of text and graphics to Macintoshes or Lisas in different locations. Price is \$99. **Apple Computer Inc.**, Cupertino, CA **Write 132**

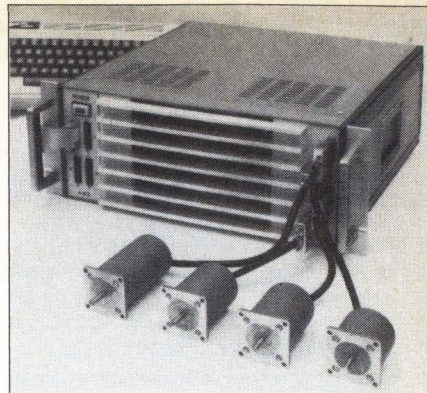
## 32-BIT SUPERMINICOMPUTER



The 8855 Model 10 is a 32-bit superminicomputer which incorporates SNA and concurrence of function. The 8855 Model 10 has a 16032 32-bit main processor chip and coprocessor functionality utilizing a 80186 chip in 16-bit terminal and communications I/O processors. The system allows 64 tasks to operate at the same time including: batch and interactive communications, SNA/SDLC and Bisynchronous protocols and data entry. Price is approximately \$97,500. **Nixdorf Computer**, Waltham, MA **Write 145**

## LASER PRINTER CONTROLLER

The Pixel 300 is an MC68000 microprocessor-based controller designed for use with laser print-



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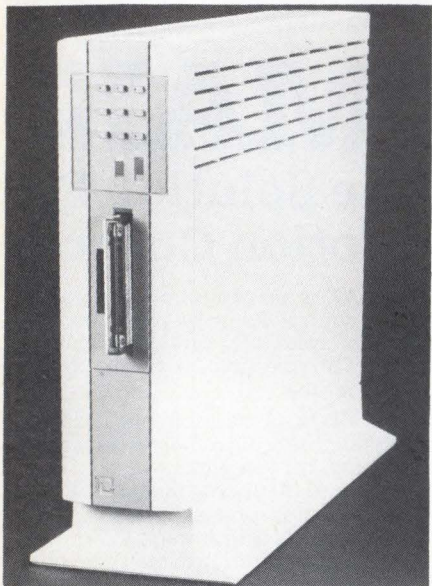
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ers. It can accommodate output speeds ranging from eight to 60 pages-per-minute. Options include bit-map printing. A Z80-A interface board is available which contains four RS-232C serial ports and two Centronics parallel ports. This enables the Pixel 300 to be tied into word processing systems or networked computers. Price is approximately \$3,000 for quantities of 500 or more. **Electronic Machine Corp.**, Los Angeles, CA **Write 151**

## DEC-COMPATIBLE MICROSYSTEM



The MicroVIP computer system is designed for multi-user and database-intensive applications. MicroVIP consists of a DEC Q-Bus central processing unit (such as the MicroVAX, LSI-11/73 or LSI-11/23), memory, communications controllers, a 190 Mbyte Winchester disk drive, a 100 Mbyte cartridge tape transport and intelligent USDC controllers. Price starts at \$15,900. **U.S. Design Corp.**, Lanham, MD **Write 134**

## SCHEMATIC CAPTURE SYSTEM

The Simulog Logic Simulator and the Symgraph Schematics Capture System are CAE applications for a workstation based on the IBM PC. Simulog is a nine-state, event-driven, logic simulator with a set of 20 logic primitives. The engineer can simulate circuits using both TTL and MOS integrated circuits technologies. Simulog is priced at \$2,500 per copy, while Symgraph is part of the graphics subsystem. **Chancellor Computer Corp.**, Albuquerque, NM **Write 130**

## CALCOMP-COMPATIBLE GRAPHICS

Skygraf is a Calcomp-compatible graphics software package for the IBM PC. Written in FORTRAN, the Skygraf subroutines are device independent and provide B&W/color, interactive graphics, 2- and 3-D contour plotting, as well as hard copy output. The subroutines interface to many standard printers. The Skygraf libraries implement two industry graphic standards: ACM SIGGRAPH "core" and the GKS. **Sky Computers, Inc.**, Lowell, MA **Write 131**

## IC LAYOUT SOFTWARE

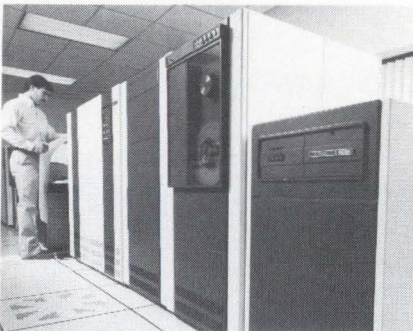
These software products from ECAD are additions to the Dracula IC Verification system. They include

a layout debugger, hierarchical verification and PG/E-beam software. The IC layout debugger locates layout violations from DRC, ERC, LVS and LPE results on a color graphics terminal and interactively edits and reruns checks on data within the display window. The PG/E Beam package drives the most mask generation systems. **Ecad Inc.**, Palo Alto, CA **Write 129**

## DESKTOP CAE WORKSTATION

The SCALDsystem IV is a full-function CAE workstation which can perform schematic capture, timing verification, logic simulation and system documentation. The system is designed to function in a network configuration, consisting of four to 16 workstations connected to a central file server. The SCALDsystem IV has a 68010 16/32-bit processor, demand paged virtual memory, one Mbyte RAM and a 10 Mbyte Winchester disk drive. Price is \$20,000. **Valid Logic Systems, Inc.**, Mountain View, CA **Write 155**

## SUPERMINICOMPUTERS



The Prime 9650 and Prime 9750 are two mid-range superminicomputers which utilize a custom gate array-based processor. The 9750 supports 128 terminals and 255 interactive processes simultaneously and is available for systems and upgrades. The Prime 9650 supports 96 terminals and 255 interactive processes simultaneously. Prices are \$251,500 (9750) and \$146,500 (9650). **Prime Computer, Inc.**, Natick, MA **Write 152**

## SOFTWARE WORKSTATION



The Symbolics 3640 is a dedicated, single-user workstation designed for use in a networked software engineering environment. The standard 3640 configuration provides 2 Mbytes of main memory,

one 140 Mbyte Winchester disk, four backplane expansion slots, a black & white display console (1100 x 900 bit mapped) and keyboard. Pipelined video memory and phase encoded digitized video output allow the console to be located up to 1000 feet from the processor. Price is \$69,000. **Symbolics**, Cambridge, MA **Write 154**

## SYSTEM CONTROLLER

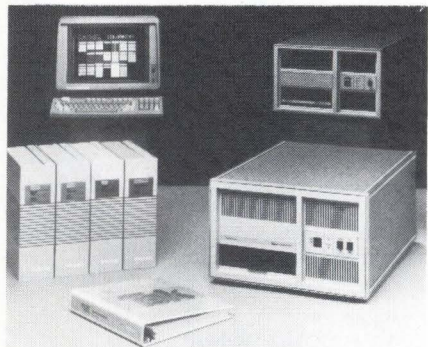


The 8000 series system controller is built around Digital Equipment's KDJ11-based LSI-11/73 processor. Six configurations are available, providing a choice of 20-, 40-, or 80-Mbyte Winchester disks, or 20/20-Mbyte fixed/removable drives. Also available are 1/4" and 1/2" streaming cartridge drives. Price in OEM quantities is \$15,000. **Plessey Peripheral Systems**, Irvine, CA **Write 150**

## INTERACTIVE 3270 CAPABILITY FOR HP 1000 COMPUTERS

Programmatic Mainframe Facility 1000 (HP PMF/1000) gives HP 1000s the ability to emulate IBM 3270 cluster controllers, allowing them to be used as distributed processing systems with links to IBM host applications or data bases. The HP PMF/1000 uses an microprocessor-based interface card, providing a response time of 2 sec. The card handles a bisynchronous communication link to the IBM host over a non-switched line at 9600 baud. Price ranges from \$4,000-\$7,000. **Hewlett-Packard**, Palo Alto, CA **Write 240**

## DEVELOPMENT SYSTEM



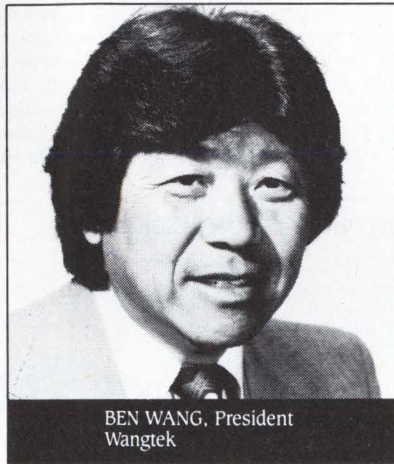
The 8562 software development system supports eight users in a TNIX multi-tasking software development and integration environment. Based on the LSI-11/73 central processor, the 8562 is compatible with other 8500 series systems. The 8562 includes the proprietary TNIX operating system, 11/73 processor, one Mbyte of RAM, a floating point processor, 40 Mbytes of hard disk storage, eight user ports, two line printer ports, and an 8" floppy disk drive. Price is \$36,000. **Tektronix, Inc.**, Beaverton, OR **Write 139**



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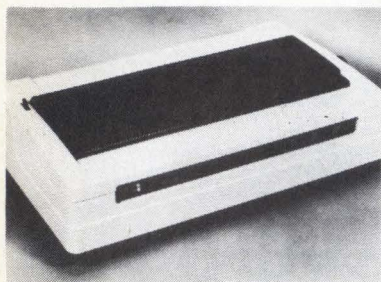
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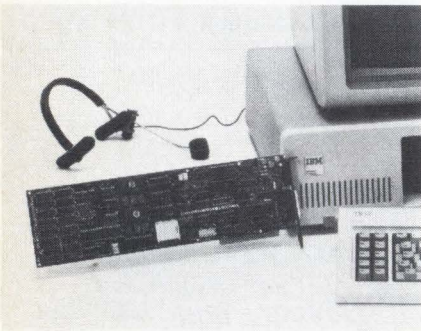


## COLOR DOT MATRIX PRINTER



The model 1570 is a multi-mode, color (four on the ribbon, seven total) dot matrix printer that features a 24-wire print head together with emulation of daisywheel products. The device operates at two speeds: 130 cps for letter quality/business graphics applications, and 180 cps for other printing applications. Resolution in the graphics mode is 360 dpi. The 1570 can print 136 to 233 characters per line and there's a 24 Kbyte buffer to reduce cpu overhead. A variety of interfaces are available. Single-unit prices start at around \$2,000. **C. Itoh Electronics, Inc.**, Los Angeles, CA  
**Write 173**

## SPEECH RECOGNITION PACKAGE



VocaLink is a speech recognition hardware/software package. The unit can process 240 spoken commands and its applications include data entry and CAD/CAM. The device operates in two modes; keystroke simulation, which substitutes user-defined verbal commands for keyboard entries to operate standard PC software; and "PC mode," for customized software. **Interstate Voice Products**, Orange, CA  
**Write 174**

## NON-IMPACT ION PRINTER

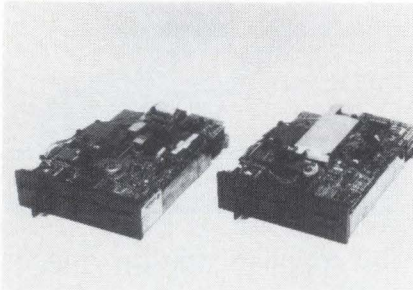
The Series 6000 is a non-impact page printer with a printing capability of 60 pages/min. The S6000 has a resolution of 240 by 240 dpi and prints forms and variable data simultaneously. The S6000 uses a DEC LSI II processor and supplies IBM 3211 and Dataproducts interfaces. The S6000 can be configured to support additional image generator cards such as graphics and variable forms cards. Price is \$60,000. **Delphax Systems**, Mississauga, Ont.,  
**Write 178**

## FLOPPY DISK DRIVE



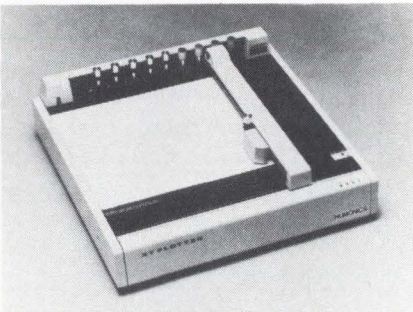
The FD-100 is a single-side, double-density, Apple compatible floppy disk drive. The 5.25" minifloppy disk drive has 164K of formatted storage capacity and uses the GCR recording method. Track density is 48 tpi, and recording density is 5536 bpi. Data transfer rate is 250 Kbytes/sec. Price in quantities of 100, is \$90. **Multitech Industrial Corp.**, Taipei, Taiwan  
**Write 168**

## 5 1/4" HALF-HEIGHT DISK DRIVES



Model TM65-4 is a 96 tpi, double-sided drive that has a 1 Mbyte storage capacity. An on-board microprocessor controls spindle speed, positions the heads, switches the write current for recording quality, and provides a programmable ready signal. Track-to-track access time is 3 ms. Model TM65-2L is a 48 tpi double-sided drive that has 1/2 Mbyte storage capacity and a track-to-track access time of 6 ms. In OEM quantities price ranges from \$125-\$150. **Tandon Corp.**, Chatsworth, CA  
**Write 183**

## 10 PEN FLAT-BED PLOTTER



The Model 6412 flat-bed plotter is equipped with 10 pens and has axial speeds of 18 in/sec. The 6412 plots graphs, bar and pie charts, and diagrams on paper, drafting paper, or transparency film. Command functions include axis, hatching, foreign symbols, ellipses, curve, and curve fittings. It interfaces with RS232C and IEEE. **Numonics**, Lansdale, PA  
**Write 245**

## ISO-STANDARD LAN

This local area network introduced by Charles River Data Systems allows its Universe family of super microcomputers to communicate and exchange data with computers from different manufacturers. UniverseNet is made up of three components; an IEEE 802 network interface, network management software, and application software packages. The network interface consists of a hardware interface, available in either VMEbus or VERSAbus format, and the software necessary to tie a Universe system into an ISO-standard network. Price is \$1,500. **Charles River Data Systems**, Framingham, MA  
**Write 177**

## PARALLEL ACCESS DISK

The MVP212 is an 8" Winchester disk with an unformatted data capacity of 212 Mbytes. The device's eight data surfaces are organized into two groups of four, with four parallel read/write channels, enabling simultaneous read/write on any four surfaces. With an SMD interface and a transfer rate of 9.67 MHz per channel, the aggregate data rate is 38.6 MHz. Quantity prices are approximately \$7,500. **MegaVault**, Woodland Hills, CA  
**Write 176**

## SUB-5.25" REMOVABLE WINCHESTER



The SQ312RD is a removable Winchester cartridge disk drive with 10 Mbytes of formatted storage. Track density of the drive is 740 tpi, cylinder count is 612, and there are 1,224 read/write tracks. The SQ312RD is a single disk system which uses 3.9" thin-film metallic plated disks, which are sputtered with graphite. Price in quantities of 100 is \$750. **SyQuest Technology**, Fremont, CA  
**Write 165**

## COLOR DOT MATRIX PRINTER

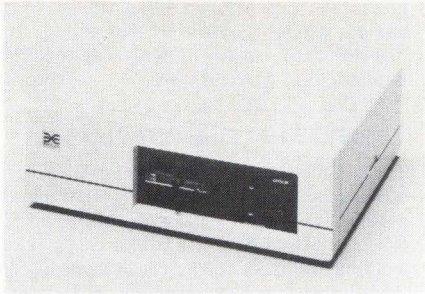
The JX-80 color dot matrix printer can print up to seven colors at speeds of 160 cps. The printer features multiple print modes that range from a 9 x 9 matrix to an 18 x 18-dot double-strike emphasized mode. For graphics output, the JX-80 functions in an eight- or nine-pin bit image mode with densities ranging from 60 to 240 dpi (horizontal) and 72 to 216 dpi (vertical). Standard interface is Centronics eight-bit parallel. Price in quantities of 1000 or more is \$480. **Epson**, Torrance, CA  
**Write 172**

## INTEGRATED SERVICE UNITS

The Integrated Service Units (ISU's) are compatible with AT&T DSU products. Central site control and diagnostics are accomplished by equipping remote ISU's with an optional diagnostic card. Each controller supports 16 lines. Optional dial-backup is available for line speeds of up to 9600 bps. The ISU 500 operates at external switch-selectable speeds of 2400, 4800 or 9600 bps, while the ISU 556 transmits at 56,000 bps. Prices are \$925 (ISU 500) and \$1090 (ISU 556). **Infinet**, Andover, MA  
**Write 171**



## PACKAGED SUBSYSTEM



The Javelin is an SCSI-based desktop mass storage, packaged subsystem. It connects through an independent host adapter to a variety of cpu's, including the DEC QBus and Unibus, the Intel Multibus, and the IBM PC, PC/XT, and compatible processors. The subsystem contains an integral power supply, cooling fan, controller boards, and a choice of two 5.25" storage peripherals. A typical configuration would include an 86 Mbyte, 5.25" Winchester drive and 1/4" streamer. Price is \$7,725. **Emulex Corp.**, Costa Mesa, CA **Write 175**

## MULTIPLEXER

The AJ statistical multiplexer allows four to sixteen remote data terminals to communicate at data ranges of 9600 bps. The multiplexer buffers data prior to transmission, transmits variable length data blocks according to the loading on individual channels, and checks data blocks received on the high speed line and requests retransmission in the event of errors. Price is \$1,850-\$7,200. **Anderson Jacobson**, San Jose, CA **Write 162**

## DAISY WHEEL PRINTER

The DWP5155 daisy wheel printer features a column/status display and a printwheel mechanism that can rotate 90° for printwheel changes. The printer accepts plastic or metal printwheels in 10, 12, 15 pitch and proportional spacing, and comes with 100 font styles. The DWP5155 has a rated MTBF of 3000 hours. **Tempest Technologies**, Reston, VA **Write 182**

## IBM-COMPATIBLE PC WITH LAN



The PCterminal which has a built-in LAN, functions as an intelligent terminal in an IBM PC network. The PCterminal has a monitor, keyboard, an 8088 microprocessor, both serial and parallel interfaces, four expansion slots for peripheral cards and 64K of RAM memory (expandable to 256K). A proprietary network protocol allows the PCterminal to initialize its operating system from the remote floppy disk of an IBM PC or hard disk. Price is \$1,295. **Santa Clara Systems**, San Jose, CA **Write 271**

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## HALF-HEIGHT 5.25" WINCHESTER

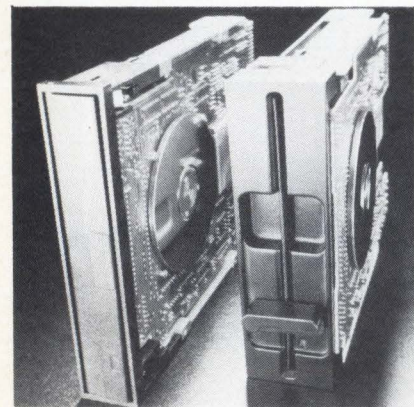


The 3425 half-height Winchester has 25 Mbytes of storage on two disks. Unformatted capacity per drive is 25.5 Mbyte and per track, 10,416 bytes. Formatted capacity for drive and track is 20 Mbyte and 8,192 bytes, respectively. Rotational speed is 3600 rpm and recording density is 10,030 bpi. The 3425 has an average access time of 85 msec and features an IC preamplifier and self-diagnostics. **MiniScribe**, Longmont, CO **Write 164**

## COLOR CRT SCREEN OPTION

The CRT screen option is designed for the Scaldsystem I and Scaldsystem II CAE workstations. The color screen allows engineers to display circuits and buses in various colors and to highlight parts of a design using different colors in different windows. The color option displays 256 colors from a palette of 16 million. Price is under \$20,000. **Valid Logic Systems**, Mountain View, CA **Write 272**

## FLOPPY DISK DRIVES



The GM3000 series of mini-floppy drives include a 48 tpi model and a 96 tpi unit. Both are available in 1/3 high and 1/2 high versions to accommodate the smallest microcomputer configurations. These double-sided drives have unformatted capacities of 500 Kbytes for the 48 TPI version and 1000 Kbytes on the 96 TPI model. The floppy disk drives have a MTBF of 11,000 hours with no duty cycle limitations. **Okidata**, Mt. Laurel, NJ **Write 170**

## 1200 BPS DIAL MODEM

The DialNet 3000 family of 1200 bps modems are designed for full-duplex communications over a dial telephone network. Capable of supporting both asynchronous or synchronous devices, the modems include two dual-speed auto-answer units and another dual-speed modem with directory-driven

autodialer. The four modems are offered as desktop units or card modules. Each has non-volatile memory for up to 20 telephone numbers. Price is \$495-\$795.

**Micom Systems Inc.**, Chatsworth, CA

**Write 181**

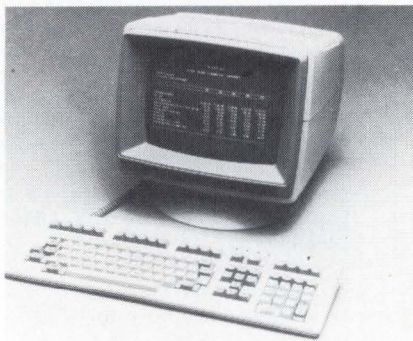
## 85 MBYTE WINCHESTER DISK DRIVE

The V185 is a 85 Mbyte 5.25" Winchester disk drive with a 30msec average access time. The drive uses ST412/ST506 interfaces and a landing zone for data recording. Track density is 1000 tpi. The V185 uses four metallic disks with a sputtered hard carbon protective overcoat and data protection is provided by automatic actuator lock and full shock mounting. The drive is compatible with controllers incorporating RLL encoding. Price in OEM quantities is \$1,695. **Vertex Peripherals**, San Jose, CA **Write 166**

## COLOR PRINTER WITH EMULATION PACKAGE

The Act II Ink Jet Color Printer has an emulation package which allows it to adapt to all Tektronix 4695 applications. The printer produces hardcopy on paper or overhead transparency materials. The printer has a pallet of 125 colors and its applications include CAD/CAE, engineering and research analysis and scientific and medical imaging. **Advanced Color Technology**, Chelmsford, MA **Write 184**

## VIDEO DISPLAY TERMINAL



The ADM 220 is a DEC VT220 compatible video display terminal which is also compatible with all X3.64 ANSI terminals. The terminals have an 80 or 132 column x 24 line display (plus 25th status line), split screen, four visual attributes and full editing capabilities. International capabilities include a non-volatile set-up mode for displaying in English, French or German, a resident multi-national character set, and optional international keyboards. **Lear Siegler, Inc.**, Anaheim, CA **Write 169**

## RUGGED 3.5" WINCHESTER

The Ranger 3521 and 3522 are rugged 3.5" Winchester disk drives that can withstand a shock load of 40G with power off and up to 100G with additional external shock absorbers. A head lifter and arm lock protects the heads and media from damage. The drives have formatted storage capacities of 5 Mbyte (one disk) and 10 Mbyte (two disks). Average access time is 80 msec. **Lapine Technology**, Santa Clara, CA **Write 270**

## ETHERNET TRANSCEIVER

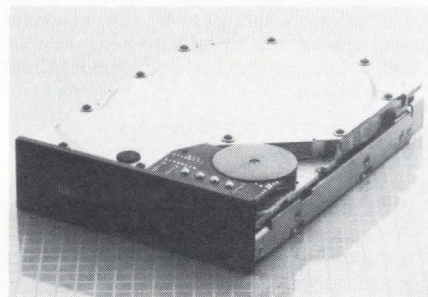
The NT100 Ethernet transceiver is compliant with the IEEE 802.3 LAN standard. The transceiver permits nodes to be attached or removed from an active network without disturbing network communica-

tions. The transceiver can send and receive 10Mbps bit streams, detect the occurrence of collisions, provide electrical isolation between the coax cable and the stations, and protect the network from transceiver and station malfunctions. Price is \$250. **Interlan, Inc.**, Westford, MA **Write 185**

## 1.6 MBYTE HALF-HEIGHT FLOPPY

The X3138 1.6 Mbyte half-height floppy disk drive uses read/write heads at a bit density of 9870 bpi and a track density of 96 tpi. Data transfer rate is 500 Kbyte/sec. The drive uses a diskette clamping system which utilizes a double-clutch clamping cone to ensure dynamic disk registration, diskette interchange, repeatable disk centering for approximately 50,000 insertions. The drive's average positioning time is 90 msec. **Philips Peripherals**, South San Francisco, CA **Write 273**

## HALF-HEIGHT 5.25" DRIVE



The CM3426 is a two-disk, half-height 5.25" Winchester disk drive with 25.52 Mbyte capacity. The drive has closed-loop servo positioning and track density of 690 tpi and contains customized package circuitry for positioning. Average access time is 85 msec, with a track-to-track access of 18 msec. Average latency is 8.3 msec. The drives are interchangeable with industry standard half-height 5.25" floppy disk drives having the same dimensions and power requirements. **Computer Memories**, Chatsworth, CA **Write 180**

## ELECTROSTATIC PLOTTERS



Four plotters have been added to the Versatec 7000 family. Models 7222 and 7422 plot on 22" wide media and the 7224 and 7424 use 24" wide media. Models in the 7200 series plot at 200 point/in and 7400 models plot 400 point/in. The adjustable plot speed ranges from .125 ips to 1.5 ips. Features include diagnostic keypad/display, darkness control/display, line enhancement, mirror imaging, and reverse imaging. Prices are \$26,200 (7222, 7224), \$35,900 (7424, 7422). **Versatec**, Santa Clara, CA **Write 274**



## NEW PRODUCTS

### HALF-HEIGHT 5¼" FLOPPY DRIVE

The Model 596-16 is a half-height 5¼" floppy drive with 1.6 Mbytes of unformatted memory. The drive is equipped with both ANSI and Apple-compatible interfaces and bezels that match most industry-standard configurations. Components of the drive include a ball bearing carriage, continuous band positioner and a servo-controlled direct drive brushless spindle motor. Track to track access time is 3ms. Price is approximately \$180. **Hi-Tech Peripherals Corp.**, Huntington Beach, CA **Write 167**

### EIGHT COLOR GRAPHICS TERMINAL

The QVT-51IGX color graphics terminal is compatible with Tektronix's 4105 graphics terminal and meets the ANSI X3.64 standard. Using a palette of 64 colors, graphics and text (alphanumeric) modes can each display up to eight colors at the same time, and 16 colors at once. The QVT-51IGX display resolution is 480 × 360 pixels with memory addressability of 4096 by 4096 points. A mouse is included. **Qume Corp.**, San Jose, CA **Write 179**

### GRAPHICS DISPLAY

The Miligraphic display combines high resolution raster-scan graphics with multiple MC68000 microprocessors in a unit designed for severe airborne, shipboard and ground mobile environments. The display features a VME industry standard bus architecture has a 19" diagonal display with 1280 by 1024 resolution and is capable of displaying up to 256 colors or shades of grey, available from a palette of 16 million colors. **Sanders Associates**, Nashua, NH **Write 242**

### STREAMING TAPE SUBSYSTEM

The CS-300M is a streaming magnetic tape subsystem which provides automatic two minute backup for the RD51 disk memory at the rate of five Mbyte/min. Maximum storage capacity is 60 Mbytes. The CS-300M consists of a streaming Q-Bus adapter card, a 5¼" wide by 1¾" high cartridge tape drive, power supply and cables. A software driver is included with the subsystem. Price in OEM quantities is \$2,900. **Computer Storage Technology**, Anaheim, CA **Write 243**

### FORTTRAN COMPILER

SuperSoft FORTRAN version 2.0 operates under MS-DOS and PC-DOS. Version 2.0 has removed the 64K code and data space limitation allowing the users to have as many 64K code and 64K data segments as desired. The compiler follows the Intel calling format so that its code can be linked with code from other microcomputer languages. This version is for users wishing to compile large FORTRAN programs on microcomputers. Price is \$425. **SuperSoft**, Champaign, IL **Write 244**

### 19V ANALOG COLOR MONITORS

The CDA-203 HA and the CDA-203 HLA are rasters-can units with precision in-line gun CRTs that are designed for high-resolution display applications and computer graphics. Both models have horizontal scan rates of 28 kHz to 36 kHz and video bandwidths exceeding 40 MHz. The PIL gun CRT has fine dot-trio pitch (0.31mm) and black matrix screen and both models incorporate a 73% transmissivity filter to enhance contrast and reduce glare. **Ikegami Electronics**, Maywood, NJ **Write 241**

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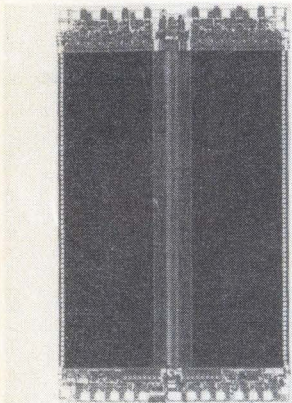
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## 512K EPROM FAMILY



The 27512 and 27513 are two 512-Kbit EPROMs. The 27513 features page addressing, a capability that allows the EPROM to be used with systems based on 8-bit microprocessors and 8- and 16-bit microcontrollers. The 27513 is partitioned into four 16-Kbit pages. The 27513 can be substituted for a 128K EPROM in 8-bit systems, quadrupling storage capacity with little modification. The 27512 and 27513 provide high-density firmware storage and save circuit-board space by allowing more storage to be accommodated by a standard 28-pin socket. Typical programming time for the 27512 and 27513 is less than six minutes. Each of the EPROMs comes in two speed versions, offering access times of 250 or 300 nsec. Price in quantities of 1,000 is \$140. **Intel Corp.**, Santa Clara, CA **Write 191**

## MULTIBUS 1/2" TAPE ADAPTOR

The Tapemaster A controls eight tape drives, is programmable for 8- or 16-bit systems, and is compatible with all industry standard formatted 1/2" tape drives. The adaptor has 24-bit addressing which accesses 16 Mbytes of memory and hardware byte swapping which allows integration into Motorola 68000 CPU based systems. The 8089 based Tapemaster A also uses parameter blocks in a ring buffer mode. Price in OEM quantities is \$943. **Ciprico**, Plymouth, MN **Write 212**

## 68000-BASED MULTIBUS BOARD

The 68000-based Multibus M68CPU board accesses 8 Mbytes on its companion memory boards at a speed of 10 MHz. M68MEMs come in 512 Kbyte and 2 Mbyte versions and four M68MEM boards can be connected for a total of 8 Mbytes of dynamic RAM. The M68CPU's memory management hardware contains 32 independent maps, which can support a task from 4K to 8 Mbytes in size. Two multi-protocol serial ports on the M68CPU interface with asynchronous, character-synchronous, or bit-synchronous RS-232C serial lines. Price is \$2,995. **SBE**, Emeryville, CA **Write 205**

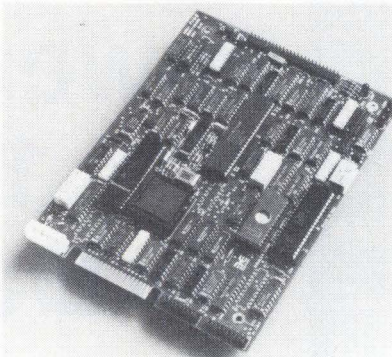
## NETWORK BOARD

The IEEE 696/S-100 bus compatible network board for CompuPro's System 816 multi-user microcomputers supports Datapoint's ARCnet protocol, and requires a passive hub and RG62 coaxial cable to network four System 816 multi-user systems. Running under CompuPro's Concurrent DOS 8-16 multi-user operating system as well as CP/M-86 and CP/M-80, the network board features 2.5 Mbit/sec data transfer rate using DMA, on-board timers and is interrupt driven. Price is \$395. **CompuPro**, Hayward, CA **Write 198**

## LSI-11 RAM BOARD

The Model 18MP-1024 22-bit high-density RAM module is designed to implement the block mode DMA protocols on the Q-Bus. Furnished with on-board timing, control logic, refresh circuitry, parity control and status register, the 18MP-1024 is DEC software and hardware compatible. **Adac Corp.**, Woburn, MA **Write 213**

## DISK CONTROLLER



The Medalist disk controller is designed for interfacing ST506, 5.25" Winchester disk drives to the SCSI. The controller employs an MOS microprocessor chip and CMOS custom VLSI buffer control and disk formatter chips designed by Emulex. The interface will support two independent ST506 5.25" drives, in uniform or mixed capacities, and will accommodate drives with up to 16 read/write heads. Price is \$395. **Emulex Corp.**, Costa Mesa, CA **Write 197**

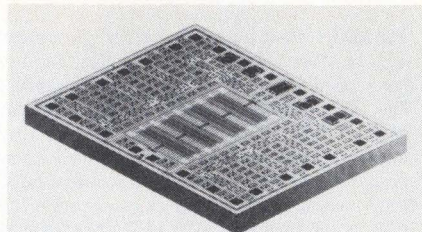
## DYNAMIC RAM CONTROLLER

The VL4500A Dynamic RAM (DRAM) Controller is a licensed alternate source product for Texas Instruments' TMS4500A DRAM Controller chip. The VL4500A operates at 150 nsec, directly drives 256 Kbytes of 64K dynamic RAM and provides address multiplexing, refresh control and time control. Price in production volumes is under \$100. **VLSI Technology**, San Jose, CA **Write 199**

## 68000-BASED CPU BOARD

The XPU processor board and XMM memory management board for computer systems have been incorporated into a new line of UNIX System V microcomputer systems. The XPU processor board employs a 68000-family microprocessor running at 10MHz. The board supports 128 fully vectored interrupts as well as three additional interrupt levels for responding to I/O, bus fault and power failure conditions. Prices are \$1,495 (XPU) and \$1,295 (XMM). **Cromemco, Inc.**, Mountain View, CA **Write 193**

## LINEAR/DIGITAL ARRAY



The Genesis II00 is a bipolar linear array to which has been added a cluster of 64 integrated-injection logic gates. The I<sup>2</sup>L gates are speed-power programmable over a range of 100mA to 200μA, with corresponding propagation delays of 7μsec to 50μsec. The linear components include 102 NPN and 41 PNP transistors; Schottky-clamped NPN transistors for high speed logic interfaces, power transistors with 400mA capability, a 10mA lateral PNP, and 347 resistors. **Cherry Semiconductor Corp.**, E. Greenwich, R.I. **Write 201**

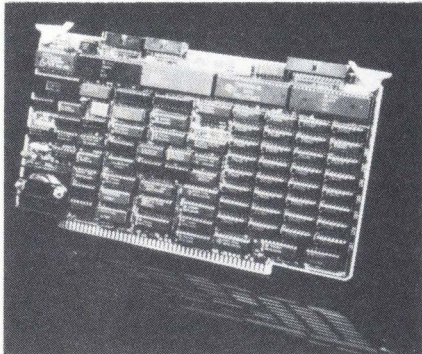
## COBALT SERVOMOTOR

The samarium cobalt (SmCo) DC motor is designed for applications such as robotics, computer peripherals, medical equipment, and instrumentation. The P/N AS-780D-007, has a high torque: inertia ratio and weighs 7.2 oz. It has a peak starting torque of 50 oz/in and measures 1.32" in diameter and 1.9" in length. **Clifton Precision**, Clifton Heights, PA **Write 209**

## SINGLE-CHIP MICROCOMPUTER

The Z8681 is a single-chip, 8-bit microcomputer which can be used to control a system addressing up to 128 Kbytes of off-chip memory. It provides 24 programmable I/O lines and uses a five volt power supply and comes in a 40-pin, TTL compatible plastic package. Price, in quantities of 100 is \$11.80. **SGS Semiconductor Corp.**, Phoenix, AZ **Write 194**

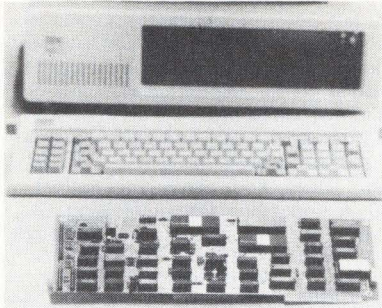
## 16-BIT SLAVES



The 16-bit S100 Bus slave board is based on the 8086-2 processor and has full compatibility with any 16-bit bus master with IEEE 696.2/D1 S100 spec compliance. The slave will run 8-bit Z80 as well as 16-bit, 8086 software. The slaves has memory mapped 8- or 16-bit data transfers and 256K and 1 Mbyte on-board RAM versions. Also included are two serial I/O ports, 2 1/2 parallel I/O ports, software selectable baud rates and vectored priority interrupt capability. Price is \$1,395. **Intercontinental Micro Systems**, Anaheim, CA **Write 189**



## HARD DISK CONTROLLER



The LTI-5150 controller interfaces with any IBM PC or compatible system and is used to upgrade the computer's data storage facilities. The controller includes ROM BIOS which is compatible with PC DOS 2.0 without the need for software drivers, thus allowing for automatic boot. The LTI-5150 can operate two ST412 compatible disk drives, has error correction and handles drives with up to eight heads. Price is \$395. **Logicom Technology**, South San Francisco, CA **Write 202**

## NUMERICAL CONTROL BOARDS

The Multibus-compatible control boards incorporate two proprietary CMOS LSI's that can be used to control servo or stepper motors. Linear and circular interpolations can be programmed. The boards have a 4MHz Z80A microprocessor and interfacing is accomplished via Multibus. Models include the NCB-102-2B Master Board for two axis control and its slave, the NCB-102-3B, which allows control of one or two additional axes. Prices are \$2,150 (NCB-102-2B) and \$3,160 (NCB-102-3B). **Toko America, Inc.**, Skokie, IL **Write 188**

## CUSTOM CMOS GATE ARRAYS

These custom CMOS gate arrays are designed to reduce component count on IBM PC compatible board level products. The FE 2000 is a CPU controller chip containing control logic designed to complement the 8088 processor on an IBM PC compatible CPU. The chip replaces an 8255 parallel I/O chip, clock generator, keyboard and printer ports and 16 other chips. The FE 2100 is a floppy disk controller chip designed to complement an NEC 765 or Intel 8272 to provide an IBM PC compatible floppy disk adapter. **Faraday Electronics**, Sunnyvale, CA **Write 208**

## LINEAR SEMICUSTOM ARRAYS

The FB900 Series consists of a family of six bipolar array chips that can be customized into application-specific LSI functions by means of metal interconnection patterns. The FB900 Series of linear semicustom arrays are supported by Micro Linear's CAD package, Linear CAD I, which performs schematic capture and SPICE circuit simulation on the IBM PC and compatibles. Micro Linear includes kit parts, design aids, characterization data, modeling information and optional macro cells of frequently used functional blocks. **Micro Linear Corp.**, San Jose, CA **Write 200**

## COLOR GRAPHICS PROCESSOR

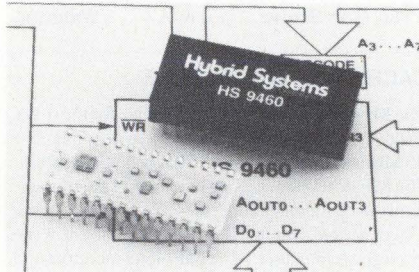
The VM-8851 Color Graphics Processor conforms to Multibus/IEEE-796 standards and offers DMA, Programmed I/O, and RS-232 interfaces. The VM-8851 utilizes a graphics engine with drawing speeds

of 25 million pixels/sec. Using 256K RAM devices, the 512K pixel image RAM expands to 2M pixels with multiple virtual image size options including up to eight buffers and a 1K x 1K image space. Price is \$3,500. **Vermont Microsystems Inc.**, Winooski, VT **Write 206**

## LINE PROCESSOR CARD

The TIL LPC458 is an intelligent communications controller that operates as a slave with 24 bit addressing, a 16 bit data bus, and generates eight non-vectored interrupts. Hardware features of the board are a 68B09 operating at 1.8432 MHz, 64 Kbytes of CMOS static RAM dual ported between the 6809 and the Multibus, a 6522 VIA for parallel communication and internal timers, and six Z8030 SCC's for multi-protocol serial communications. **TIL Systems Ltd.**, Toronto, Ontario **Write 186**

## HYBRID I/O SUBSYSTEM



The HS9460 is a Hybrid I/O Subsystem. The HS9460 contains four analog to digital input channels, timing and control circuitry for direct microprocessor interface and four digital to analog output channels. The input section consists of four single-ended inputs multiplexed to a 20µsec 8 bit ADC. The analog output section has four independent channels of 8 bit resolution. Price in quantities of 100 is \$89. **Hybrid Systems**, Billerica, MA **Write 207**

## CMOS STATIC RAMS

The Am9968 and Am99L68 are CMOS static RAMs organized as 4096 words by 4 bits which have a 45 nsec access time while drawing 80 mA when active. Users can select either the standard Am9968 or the lower power Am99L68. Both devices feature automatic power down when they are deselected. Samples of the Am9968/99L68 are available in 20-pin plastic and ceramic packages, with production quantities planned for December. Price in quantities of 100 is \$20.90. **Advanced Micro Devices**, Sunnyvale, CA **Write 190**

## HCMOS GATE ARRAYS

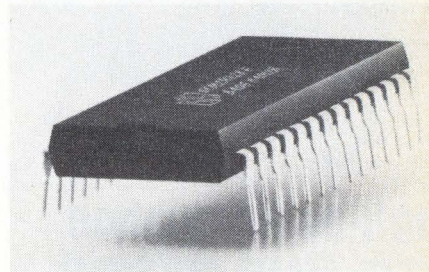
This series of HCMOS gate arrays feature flip-flop toggle rates of 75 MHz. The Quad Logic arrays utilize a basic four-gate equivalent cell arranged as two 2-input and two 3-input gates. The arrays range in complexity from 2,000 to 8,000 two-input and three-input gates. The Quad logic arrays are supported by Hughes design automation software tools, including a macro function library, logic and timing simulation, automatic placement and routing, and design verification. **Hughes Solid State Products**, Newport Beach, CA **Write 192**

## GRAPHICS PROCESSOR BOARD

The Matrox SX-900 is a Multibus color graphics processor which provides 640 x 480 resolution, 4

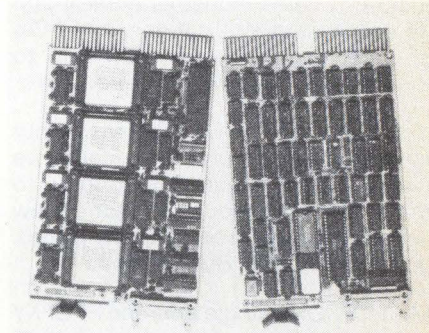
or 8 bit planes, a 4096 color lookup table and a 60Hz refresh rate. The SX-900 has a pipelined architecture, using a 80286 CPU front end display list processor and is supported by a 7220 graphics primitive processor and a high speed pixel processor for simultaneous eight plane drawing. Prices are \$2,995 (4 bits/pixel) and \$4,195 (8 bits/pixel). **Matrox Electronic Systems Ltd.**, Montreal, Quebec **Write 187**

## 128K CMOS ROMS



The 23C128 128K CMOS ROMs feature access times of 150, 120 and 100 nsec. Under worst case conditions they have a current of 25 mA maximum, a standby current of 100 µA, and LSTTL-compatible inputs and outputs. Because they are pin compatible with NMOS EPROMs, these 23C128 ROMs can also be substituted for existing EPROMs. **Solid-State Scientific**, Willow Grove, PA **Write 204**

## BUBBLE-MEMORY SYSTEM

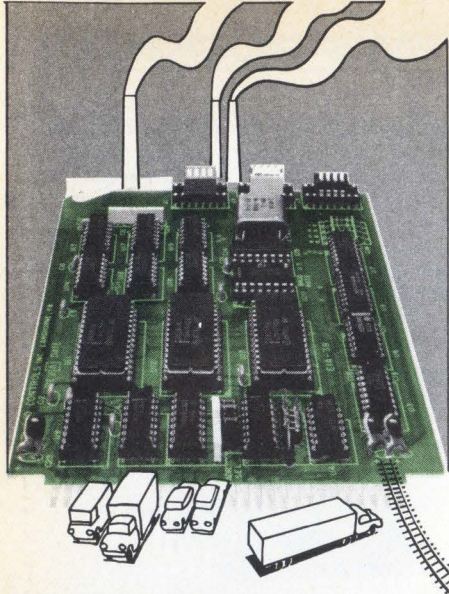


The QBL-II/02 is a RL02-compatible magnetic-bubble memory system for DEC LSI-II microcomputers. Storage capacity can be configured from 256 Kbytes, to 32 Mbytes. Bootstrap ROMs for both RT-II and RSX-II are included on the QBL-II/02 module. Access time to the first data byte averages 30 msec, and data is transferred to/from bubble storage at a rate approaching 1 Mbit/sec. Price is \$776. **Bubbl-Tec**, Dublin, CA **Write 203**

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Model PPCI-X (single axis) and PPCI-XY (dual axis) stepping motor control cards offload motion control routines from the host CPU. The 70128 card has memory capability to 128K PROM or 128K RAM or PROM/RAM combinations. The 33-232 card provides one RS-232 serial port, 3 eight-bit parallel ports, 8 level priority interrupt and 3 timers. The 16X16 card provides 16 each of opto-isolated inputs and outputs. The Model 2002 card has 256K non-volatile RAM.

Call or write for full details.



## I/O Controls Inc.

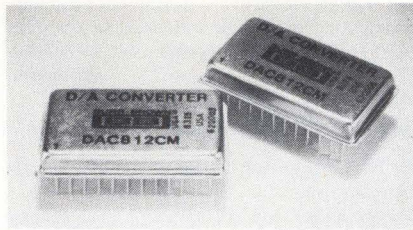
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Write 38 on Reader Inquiry Card

138

## NEW PRODUCTS

### 12-BIT TTL DAC



The DAC812 is a 12-bit TTL DAC which has a current output settling time of less than 65nsec to  $\pm 0.012\%$  of full-scale range. A bipolar process is applied in the switch array and in the stable thin-film-on-sapphire resistor network. Packaged in a 24-pin case the DAC is specified over  $-25^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ . An output compliance voltage range of  $\pm 4\text{V}$  allows generation of an output voltage without using an external output op amp. Price in quantities of 100 is \$86. **Burr-Brown**, Tucson, AZ **Write 195**

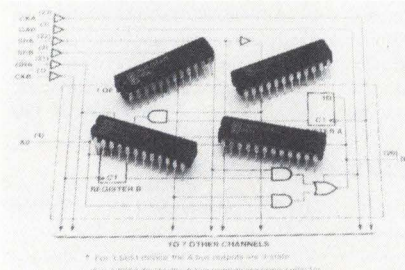
### CACHE MEMORY MODULE

The MF-4593 cache memory module for the iLBX bus on Multibus system images the system memory (16 Mbytes), using a two set LRU caching algorithm. The MF-4593 stores 2K 16 bit words of the most recently used memory addresses. Cache memory has a data access rate of 100 nsec, utilizing a write through architecture. The MF-4593 monitors and buffers into a FIFO all writes to the Multibus by other masters. Price is \$1,995. **Symbicon Associates, Inc.**, Amherst, NH **Write 196**

### 4 MBYTE Q-BUS MEMORY

The CI-1173 memory is for all Q-Bus compatible systems and is available in configurations ranging from 128 Kbyte to 4 Mbyte on a single card. Access and cycle times are 160nsec. Each module consumes one quad slot in any Q-bus backplane. The memory can be customer configured to start and stop addresses on any 16 Kbyte boundary in the 0 to 4 Mbyte address range. Price in OEM quantities is \$1,975 (1 Mbyte) and \$9,975 (4 Mbyte). **Chrislin Industries, Inc.**, Westlake Village, CA **Write 210**

### DOUBLE DENSITY INTERFACE SERIES

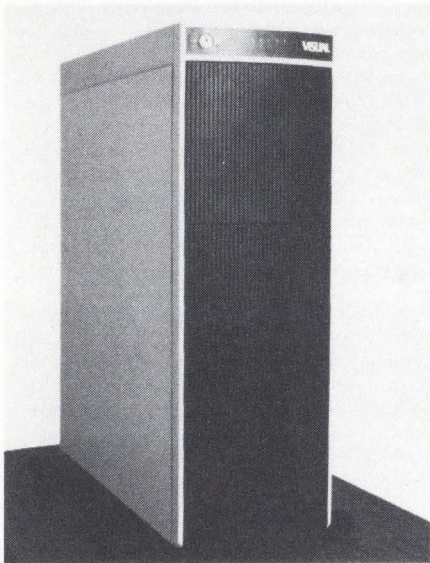


The 54/74LS651, 54/74LS652, 54/74LS653, and 54/74LS654 are double density interface devices, which combine two registers and two multiplexers into a single part for bidirectional data flow. Two front-loading latches are cross-coupled in each of the eight-bit positions, so that data can enter or exit from either side of the latch. All four parts share a pinout, with a one-byte-wide, bidirectional data bus on each side of the physical device. Price in quantities of 100 is \$6.78. **Monolithic Memories**, Santa Clara, CA **Write 211**

### CAD SOFTWARE SYSTEM

The Medusa System utilizes DEC VAX computers as its computer resource. Medusa is an integrated software system for two-dimensional design, drafting, and dimensioning, and three-dimensional solid modeling. Supporting Medusa is the MWS workstation 3400 which incorporates the Motorola 68010, 32-bit microprocessor technology and a UNIX operating system. Price ranges from \$10,000 to \$15,000 per workstation. **Computervision**, Bedford, MA **Write 128**

### MULTI-USER SYSTEM



The Visual 2000 is a multi-user system based on the Intel 286 microprocessor. The Visual 2000 is designed to support 16 terminals under the XENIX operating system. In a base-level configuration, the Visual 2000 includes 512 Kbyte of RAM, a 19 Mbyte Winchester disk, a 5.25" floppy, six RS-232 terminal ports and a parallel printer port. Options include a 1/4" streaming tape cartridge drive for disk backup and expansion capabilities. Price is \$8,990. **Visual Technology Inc.**, Tewksbury, MA **Write 142**

### DESIGN AUTOMATION SYSTEM

The Modular Integrated Design Automation System is an integrated set of application and design tools for engineers and logic designers. The software consists of logic simulation, fault simulation and layout. MIDAS has an integrated data base and engineering data library which allows compatibility between all data used in different applications. Midas operates on Control Data's Cyber computer series and the Cybernet data services network. Price is \$500,000. **Control Data**, Minneapolis, MN **Write 126**

### 32-BIT PROCESSOR

The Concept 32/27XX processor is designed around the SelBus and has a transfer rate of 26.67 Mbyte/sec. The system has eight general purpose registers to use in arithmetic, logical and shift operations. The processor can accommodate 96 priority interrupt levels used for I/O controllers and external signals. **Gould Inc.**, Ft. Lauderdale, FL **Write 127**





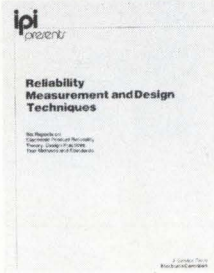
**Board Test Systems Brochure.** This brochure from Teradyne describes its L280 Board Test System and MultiMode testing for VLSI circuit boards. Included is an overview of the L280 architecture, a discussion of Automatic Bus Cycle Emulation, a summary of channel card features, and system specification highlights. Described is the MultiMode test strategy with charts and block diagrams illustrating implementation on the L280.

**Teradyne Write 257**



**VG/DIN Connectors Catalog.** This 32-page VG/DIN Design Guide & Catalog from Elco describes its line of two, three and four-row low insertion and withdrawal force connectors for single, double and multilayer boards. The Design Guide details connectors in I/O and board-to-board applications.

**Elco Write 259**



**Electronic Reports.** These six reports from ElektronikCentralen, a Danish research center, look at electronic product reliability, theory, design practices, test methods and standards. The reports consist of research, development and testing in the fields of systems engineering and circuit design; components, materials and process technology; and testing of electronic equipment and components.

**ElektronikCentralen 252**



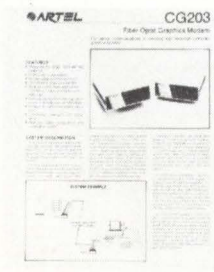
**Meter Catalog.** This catalog from International Instruments introduces the Verigraph meter line, a vacuum-fluorescent bargraph display. The bulletin includes an explanation of the vacuum fluorescence principle, information on special features of the Verigraph, mechanical data, and performance specifications.

**International Instruments Write 251**



**Interface Product Catalog.** This four-page catalog from Erbtec Engineering, Inc. describes tools for interfacing to the IEEE-488 bus. Product descriptions include photo, list of features, and price. A tear-sheet is provided for detailed information.

**Erbtec Engineering Write 262**



**Fiber Optic Bulletin.** This bulletin from Artel Communications Corp. describes its CG203 system. A diagram illustrates the system which consists of two self-powered transmitter and receiver modems (CG203T and CG203R). The modems allow communication of high resolution color video and duplex data between the graphics computer and the monitor/workstation.

**Artel Write 264**

## Monitoring and Control System Data Sheet.

This eight-page data sheet from Di-an Micro Systems Ltd. describes its DMS561 and DMS661 distributed monitoring and control systems. These microcomputer-based units support analog and digital input/out configurations, and will operate with any computer or terminal with an RS-422, RS-423, RS-232C or 20mA current loop serial port.

**Di-an Write 260**

## Data Communication Devices Catalog.

This mid-year 1984 issue from Black Box contains over 400 products of data communication devices and accessories. An expanded cable product line plus 30 new products are included. Each product is described and illustrated with photos and diagrams and the catalog includes price.

**Black Box Corp. Write 266**

## Encoder Application Note.

This eight-page application note from ILC Data Device Corp. discusses the selection of encoders for microprocessor-based systems. The note describes the major types of encoders and the dynamics of resolver-to-digital converters. Seven figures illustrate the points mentioned and five representative converters for motion control applications are also described.

**ILC DDC Write 253**

## Disk Controller Brochure.

The StorageTek 8890 Sybercache Intelligent Disk Controller is described in this four-page brochure from Storage Technology Corp. The brochure contains a performance improvement chart, which displays results obtained by users along with illustrations and information on reducing system response time.

**Storage Technology Write 250**

## Microcomputer Bulletin.

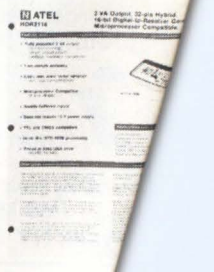
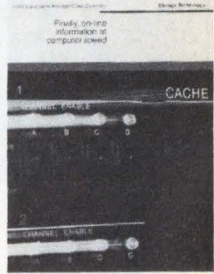
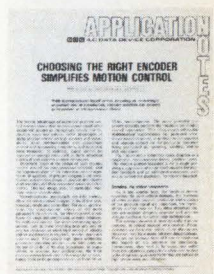
This three-page bulletin from Apollo Lasers Inc. describes its computer controlled FIR Laser Stabilization System. The system consists of a hardware interface and a microcomputer program. The bulletin details eight options that are available from the start-up menu.

**Apollo Lasers Write 265**

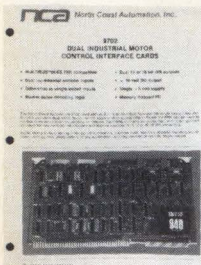
## D/R Converter Data Sheet.

This eight-page data sheet from Natel Engineering Co., Inc. describes a 16-bit Digital-to-Resolver Converter, with two VA output and microprocessor compatibility. The converter is packaged in a 32-pin hybrid DDIP, with one arc-minute accuracy and 0.03% vector accuracy. Included are applications information, specifications and product features.

**Natel Engineering Write 269**





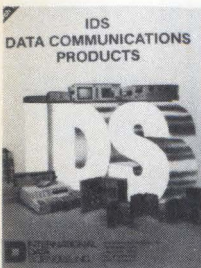


**Motor Control Interface Brochure.** This four-page brochure from North Coast Automation details features and applications for the 8- or 16-bit Multibus compatible card. Discussed is the operation with a standard incremental encoder, analog servo output signal, and microprocessor address system. Input and output specs are presented as well as dimensions, power supply requirements and ordering information.

North Coast Automation Write 218

**Data Communications Product Catalog.** This 32-page catalog from Racal-Milgo includes sections on network components, communications networks, and office products. The sections discuss modems, multiplexers, data service units, encryption products, network management systems, local area networks, protocol and code translators, terminals, printers and communications controllers.

Racal-Milgo Write 225



**Data Communication Catalog.** This 51-page catalog of data communication products profiles International Data Sciences' line of hand-held testers, data traps and data comm testers, data switches, modems, and cables. Products featured include the Model 67/60 Modem and Mux Tester, Models 4020 and 4030 Data Communications Analyzers, Model 1320 TDM-Modem Test Set, as well as its series 8500 Data Switches.

International Data Sciences Write 217

**Electronic Control Data Sheet.** This data sheet from Control Technology Corp. describes the 2000 series of programmable controllers and accessories. The data sheets discuss the use of programmable functions, including time delays, input monitoring, counters, flags and multi-tasking. Hardware and software features are also provided for the controllers, as well as connection diagrams and electrical specifications.

Control Technology Corp. Write 224

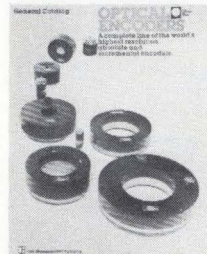


**Data Conversion Catalog.** This eight-page short form catalog from ILC Data Device Corp. (DDC) describes over 100 products. Specifications and technical data for bus products, A/D, D/A, S/D and D/S converters are noted. Other products listed include sample/hold and track/hold amplifiers, synchro instruments and MIL-STD-1553 components.

DDC Write 221

**Encoder Catalog.** This six-page catalog from Itek Measurement Systems provides specs, features, and data about optical encoders. The catalog lists performance ratings, features, and options for a range of solid shaft and thru-hole optical shaft angle encoders in absolute and incremental configurations.

Itek Write 220



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ON THE  
RIGHT BUS



VERSAbus



MULTIbus



VMEbus

Backpanel and bus connection systems from the factory through production.

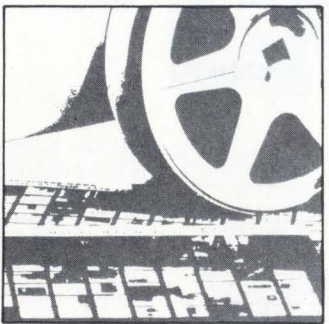
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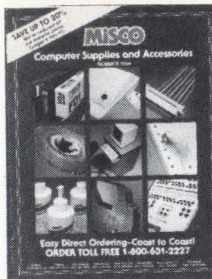
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Dept. P.R.  
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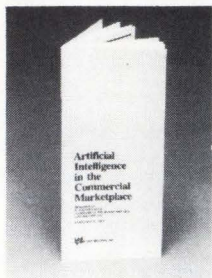
# NEW LITERATURE



**Personal Computer Products Catalog.** This 100-page full color catalog from Misco, Inc. offers supplies and accessories for computers and word processors. Described are new items such as the Support Platform which will accommodate any PC with a detached keyboard measuring up to 19 1/8" by 2 3/4" by 9 1/2" and weighs 11 lbs. and a Data Entry Station designed to conform to ergonomic standards.

**Misco Inc.**

**Write 255**



**AI Technology Brochure.** This 16-page illustrated brochure from LISP Machine Inc. (LMI) documents the nature of artificial intelligence, the developing applications of this technology, and its approach to the growing commercial market for AI hardware and software. The brochure emphasizes that for AI to succeed in the commercial world, it must be applied to situations and problems encountered in a wide range of industries.

**LISP Machines**

**Write 254**



**Disk Drive Data Sheet.** This data sheet from Advanced Storage Technology, Inc. describes its AST 96200 family of 61 and 103 Mbyte 5 1/4" half-height disk drives. A list of features is provided as well as specifications covering performance, functions, physical measurements and reliability parameters.

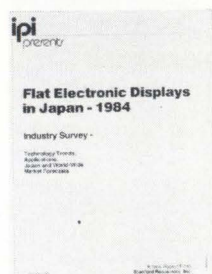
**Advanced Storage Technology Write 263**



**Integrated Circuit Book.** This 70-page shortform data book from Harris Semiconductor describes its analog, digital and custom integrated circuit line. Each section provides a product description including applicable specifications and pinout. Also included are analog and digital user cross references.

**Harris**

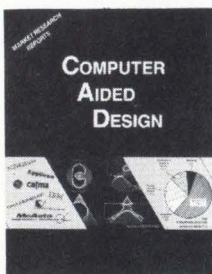
**Write 268**



**Industry Survey.** This study from Stanford Resources, Inc. presents an analysis of market and technology trends in Japan for flat electronic displays. Issues discussed are industry participants, Japanese and worldwide market forecasts, applications being addressed and what Japan's strategy is for the future.

**Stanford Resources, Inc.**

**256**



**CAD Report.** This 200-page report from Strategic Inc. offers an analysis of markets in mechanical CAD applications for central host systems, minicomputer systems, engineering workstations, and personal computer systems. It evaluates companies involved in mechanical design and vendor offerings including system hardware and system software. Also discussed are future trends in hardware, software, as well as applications, support and prices.

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**Write 267**



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**Ninth Conference on Local Computer Networks.** Minneapolis, MN. Contact: 9th Conference on Local Networks, c/o Harvey A. Freeman, General Chairman, Architectural Technology Corp., PO Box 24344, Minneapolis, MN 55424.

## October 9-11

**Electronics Manufacturing Technologies and**

**Systems Conference (EMTAS '84).** Raleigh, NC. Contact: Society of Manufacturing Engineers, PO Box 930, Dearborn, MI 48121.

## October 10

**1984/85 Invitational Computer Conference (ICC).** Cherry Hill, NJ. Contact: Suzanne Hubner, Conference Director - US, B.J. Johnson & Associates, 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

## October 11-14

**Computer Expo and PC Show.** Sacramento, CA. Contact: Cal Expo, Sacramento, PO Box 160288, Sacramento, CA 95816. (916) 924-9351.

## October 16-18

**UNIX Operating System Exposition and Conference.** New York, NY. Contact: Robert P. Birkfeld, National Expositions Co., Inc., 14 West 40th St., New York, NY 10018. (212) 391-9111.

## October 18-19

**Aluminum Metalization for VLSI.** Palo Alto, CA. Contact: Public Information Office, University Extension, University of California, Berkeley, 2223 Fulton St., Berkeley, CA 94720. (415) 642-3112.

## October 21-24

**Computer Graphics '85.** Atlanta, GA. Contact: National Computer Graphics Assoc., 8401 Arlington Blvd., Fairfax, VA 22031. (703) 698-9600.

## October 21

**Integrated Optical Circuit Engineering.** Cambridge, MA. Contact: SPIE, PO Box 10, Bellingham, WA 98227-0010. (206) 676-3290.

## October 22-26

**Iecon 84, International Conference on Industrial Electronics, Control, and Instrumentation (IEEE et al.).** Tokyo, Japan. Contact: F. Harashima, Institute of Industrial Science, University of Tokyo, Roppongi, Minato-ku, Tokyo, 106 Japan. Tel: 03-402-6231.

## October 23

**1984/85 Invitational Computer Conferences (ICC).** Englewood/Denver, CO. Contact: Suzanne Hubner, Conference Director - US, B.J. Johnson & Associates, 3151 Airway Ave., #C-2, Costa Mesa, CA 92626. (714) 957-0171.

## October 30-November 1

**ATE Central, CADCON Central '84.** Dallas TX. Contact: Morgan-Grampian Expositions Group, Two Park Ave., New York, NY 10016-5667. (212) 340-9780.

## November 13-17

**Electronica 84.** Munich, Germany. Contact: Munchener Messe- und Ausstellungs-, gesellschaft mbH, Messsegelände, Postfach 12 10 09, D-8000 Munchen 12. Tel: (089) 51 07-229.

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