

DIGITAL DESIGN

SYSTEMS ARCHITECTURE, INTEGRATION AND APPLICATIONS

OCTOBER 1985



**386-IT'S
HERE!**

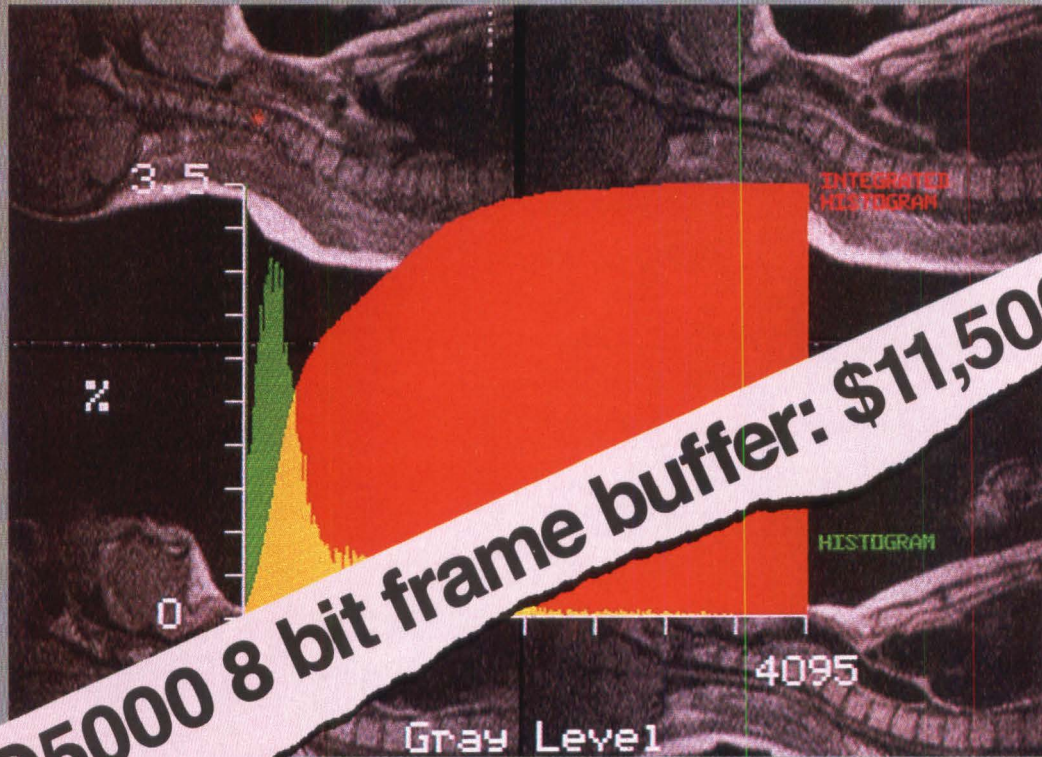
**PCs GET TOUGH —
CONTROLLERS GET SMART**

**VME BUILDING BLOCKS
MAKE IMAGE PROCESSING A SNAP**

EDIF BREAKS CAE COMPATIBILITY BARRIER

HIGH-PERFORMANCE ICs FUEL UP WITH GaAs

Gould...Innovation and Quality in Image Processing.



Histogram of 12 bit magnetic resonance medical image with four (4) bit color overlay. Courtesy of Mallinckrodt, Institute of Radiology.

Gould's FD5000 Image Processor Introduces a Whole New Idea:

Performance and Economy.

An image processor can be expensive. Unless it's the FD5000. For \$11,500, you can purchase an 8 bit frame buffer with driver software. And the system doesn't stop there. As your needs expand, so will the FD5000 to a full

32 bit image processing system for advanced applications.

Check these basic and optional features:

Flexible Architecture:

Two 12 bit deep images or three 8 bit images with 4 bits of color or monochrome overlay provide monochrome, pseudocolor, and true color.

60Hz Flicker-Free Display:

Bright, flicker-free image display at 60Hz; 30Hz for image processing and real time input.

Feedback Processor:

Five times faster than host-based operations for convolutions, digital filtering, interactive math, regions of interest, and recursive filtering.

1024² × 32 Bit Memory Arrays:

Optional memory configuration provides user choice of image size and processing precision to display through 512² viewport.

MINI-LIPS Image Processing Software:

Interactive keyboard control; prompts for filters, real-time math, Look-Up Tables, histograms, geometric operations, utilities, and image storage; demo programs include source code.

The Closer Look:

The FD5000 will minimize the load on your host CPU and your processing staff. Peripheral or stand alone configurations are available.

Give Us A Call:

We'll be happy to discuss your application needs and the FD5000 at your convenience.

Gould Inc., Imaging and Graphics Division
46360 Fremont Boulevard, Fremont, CA 94538 USA
Telephone (415) 498-3300 • TWX (910) 338-7656

European Headquarters
Tegernseer Landstrasse 161,
D-8000 Munchen 90, West Germany
Telephone (089) 6-92-79-06
Telex 5218078-GOUI D



GOULD
Electronics

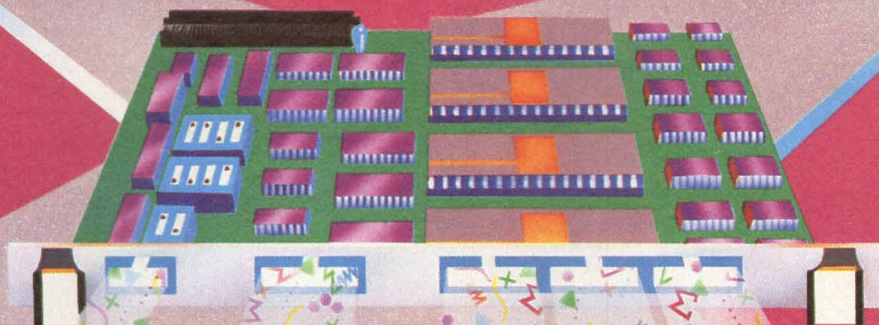
Datacube presents
MaxVideo™

The most powerful family of video image processors.

Choose modules that match your real-time image processing requirements.

MAXbus™, the video interconnect standard, gives you flexibility to expand your MaxVideo system.

Write or call today.



DATAcube

Datacube, Inc.
4 Dearborn Road, Peabody, MA 01960
(617) 535-6644

Circle 4

"NO WAIT STATE"



OF - THE - ART

by



Force's "NO WAIT STATE" - OF - THE - ART CPU-4 features the 68010 at 12.5MHz with 128KBytes of SRAM for your high speed applications.

Proven speed superior in benchmarks, the CPU-4 is ideal for high performance VMEbus applications. In fact, the "NO WAIT STATE" CPU-4 holds its own against 68020 CPU products operating with several wait states!

Addition of the CPU-4 to Force's distinguished product family, designed and manufactured with years of VMEbus board engineering and production experience, assures you of a reliable, available, high performance CPU. CPU products available include:

CPU-1 Series The World's most popular and universal VMEbus CPU featuring 8/10MHz 68000, 128/512KBytes DRAM, 3 serial ports, RTC, and more. Over 6000 sold worldwide.

CPU-2 Series A highly versatile CPU incorporating the 8/10MHz 68010 with true "Dual Ported RAM" from 128KBytes up to 1MByte, multi protocol communications controller, floppy disk controller, PIT, and RTC.

CPU-3 Series The World's first UNIX* VMEbus board incorporating the 68010 CPU, 68451 MMU, and 68450 DMAC, 4 level bus arbiter, and serial I/O on one double Euro-card, 32 or 128K Bytes, zero wait state, SRAM CACHE mode operation

CPU-4 Series Additional features to those already mentioned include, a 68450 DMAC, 1 serial port, 2 parallel ports, RTC, and a floppy disk controller option.

NEW PRODUCT ADDITIONS

DRAM-E3M1+E3S3

The 1MByte DRAM master operates stand-alone or with multiple 3MByte slaves offering optimum performance in 32 bit data/32 bit address, Byte parity check environments. Typical access time is 65ns (write) and 240ns (read) with parity generation.

CMC-1

As an intelligent monochrome or color controller for raster scan terminals, this

stand-alone VMEbus board offers interfaces for keyboard, lightpen, 2 serial ports and 1 Centronics parallel port.

ASCU-1/2

This new breed of high performance advanced system controller handles all exception signals on the VMEbus and contains powerful I/O devices such as a serial interface, Centronics parallel interface, 4 level bus arbiter, RTC, and GPIB interface (ASCU-2).

If the VMEbus boards you purchase aren't designed and manufactured by FORCE, chances are they aren't "NO WAIT STATE" - OF - THE - ART.

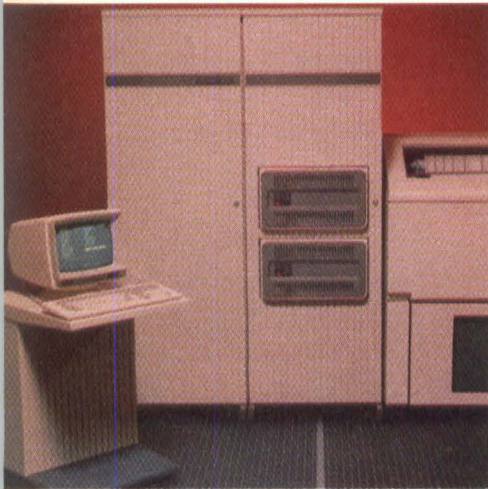
Call Force Computers today, the VMEbus specialist!

FORCE COMPUTERS INC.
727 University Ave.
Los Gatos, CA 95030
Phone (408) 354-3410 1
Tlx 172465
Telefax (408) 3957718

FORCE COMPUTERS GmbH
Daimlerstraße 9
D-8012 Ottobrunn
Telefon (0 89) 6 09 20 33 2
Telex 5 24 190 forc-d
Telefax (089) 6 09 77 93

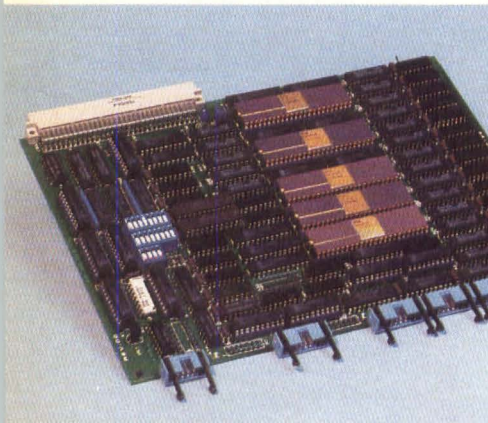
FORCE COMPUTERS FRANCE
11, Rue Casteja
F-92100 Boulogne
Tel. (1) 620 37 37 3
Telex 206 304 forc-f
Telefax (1) 621 35 19

*Unix is a registered trademark of AT&T



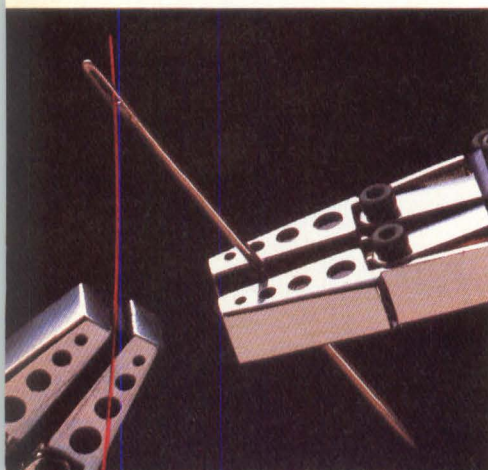
COURTESY PERKIN-ELMER

17 Multiprocessing Cruncher arrives



COURTESY DATACUBE

48 Image processing is a snap



COURTESY ALLEN-BRADLEY

60 PCs vs. programmable controllers

TECHNOLOGY TRENDS

- 17 **Systems** / Cruncher Enters Multiprocessing Arena
- 19 **ICs** / Systems On A Chip Via 20,000-Gate Array
 - Mainframe-Style Architecture Joins Microprocessor Fray
 - Language Specific ICs Debut At Wescon '85
- 27 **Design Tools** / Hardware And Software Development Linked To Shorten Product Cycle
- 29 **Imaging** / Color Image Framestore Uses Precision Converters For High-Quality Images • Imaging Functions Go On-Chip At GOMAC '85
- 13 **Editor's Comment**
- 15 **Hotline**
- 75 **Letters**
- 77 **New Product Focus**
- 78 **New Products**
- 81 **Reader Service**
- 99 **New Literature**
- 100 **Calendar**
- 100 **Advertiser Index**

ON THE COVER

Intel's 80386 32-bit microprocessor provides an upgrade path from the entire family of 8086 products. Not only can an installed base of 16-bit software gain immediate access to this new processor, but PC DOS and UNIX programs can exist side by side. Packaged in a 132-pin pin-grid array, the 386 is designed to operate at 12 MHz and 16 MHz and dissipate between 1.5 to 3 watts. Photo courtesy Intel Corp.

Published monthly thirteen times a year with two issues in November. Subscription rates for non-qualified subscribers (US and Canada) — \$40/yr; foreign — surface mail — \$50/yr; airmail — \$85/yr. Single copies — \$4. Copyright 1985 by Morgan-Grampian Publishing Company, 1050 Commonwealth Ave., Boston, MA 02215. Second class postage paid at Boston, MA and at additional mailing offices. POSTMASTER: Send address changes to Morgan-Grampian Publishing Company, Berkshire Common, Pittsfield, MA 01201 ISSN 0147-9245

32 80386
Intel's 32-bit 386
preserves software
investment from
the 16-bit world.

COURTESY INTEL

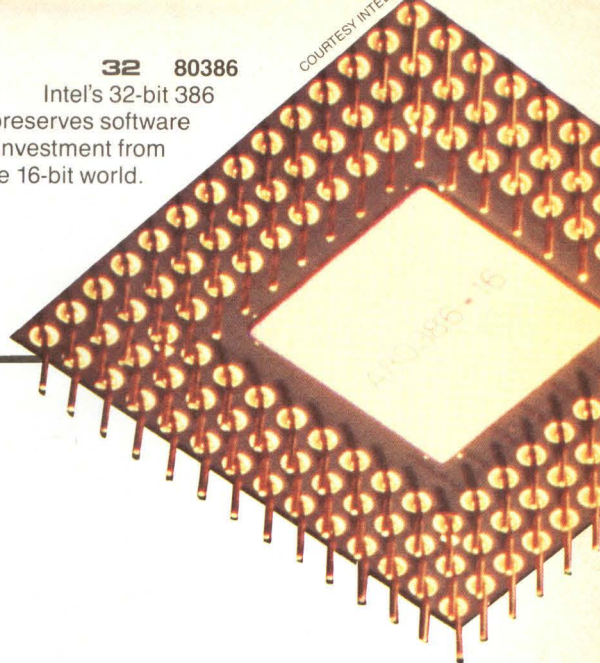


TABLE OF CONTENTS

FEATURES

SEMICONDUCTOR TECHNOLOGY

32 80386 Raises The Flag For Compatibility

by Paul Wells

The 80386 32-bit microprocessor is the latest microprocessor from Intel Corp. and provides access to the 32-bit world: 32-bit registers, 32-bit data bus, 32-bit address bus and 8-, and 16-, and 32-bit data types.

41 High-Performance ICs Fuel Up With GaAs

by Dave Wilson

Offering four to six times the speed of silicon-based ECL parts and as much as ten times the speed of silicon CMOS parts, gallium arsenide (GaAs) devices are carving an ever-widening market niche with each process improvement.

IMAGING AND GRAPHICS

48 VME Building Blocks Make Image Processing A Snap

by Shep Siegel

Users of board-level image processors have to meet a range of performance requirements and functional needs. By providing modules, the task of adding new functions and performance requirements can be reduced dramatically.

55 Video Filters Process Pictures Precisely

by Vince Emmerson

Electronic images in robotics, television broadcasting, computer graphics, diagnostic medical equipment, fiber optic transmission equipment and similar applications are nearly all subjected to some form of digital processing.

SYSTEMS ARCHITECTURE

60 Personal Computers Get Tough; Programmable Controllers Get Smart

by Brita Meng

The migration of the personal computer from the office to the factory floor raises new questions for system integrators designing industrial computer systems.

DESIGN TECHNOLOGY

69 EDIF Breaks CAE/CAD Compatibility Barrier

by Lisa Hampton

EDIF—Electronic Design Interchange Format—a new standard format for the transmission of design data allows designers to select from a wider variety of gate array and CAE vendors. Otherwise, designers must wait until the gate array vendor and the workstation vendor develop new libraries.

THE MOST SPECTACULAR BUS ANNOUNCEMENT SINCE MULTIBUS® II.



INTEL CORP.

- 2940 MEAD AVE., SANTA CLARA, CA 95051
- 5200 ELAM YOUNG PKWY., HILLSBORO, OR 97123
- 2420 WEST BEARDSLEY RD., PHOENIX, AZ 85027
- 5000 WEST WILLIAMS FIELD RD., CHANDLER, AZ 85224
- OTHER: _____

SHIP TO:

Advanced Systems Inc.
77 Industry Drive
San Francisco, CA 94108

Attention: Mark Dickerson
(415)445-3000

REF. NO. _____

RECEIVED

SHIPPING MEMO NO. _____

87121

VENDOR MUST
BE NOTIFIED
IN ADVANCE,
IN WRITING,
WHEN RETURNING

ITEM	QUANTITY	UNIT	INTEL PART NO.	DESCRIPTION
1	10	--		iSBC 286/100 8MHz MBII CPU board
2	2	--		iSBC MEM/312 512 Kbyte Mem board
3	4	--		iSBC MEM/310 1 Mbyte Mem board
4	2	--		iSBC MEM/320 2 Mbyte Mem board
5	2	--		iSBC MEM/340 4 Mbyte Mem board
6	10	--		iSBC CSM/001 Cent. Serv. Module
7	1	--		iRMX 86II R.0 RMX86 MBII R-t OS
8	5	--		iSBC PKG/609 9 slot cardcage & PSB backplane
9	5	--		iSBC PKG/903 3 slot iLBXII backplane
10	1	--		iSDM 286 R.0 286 System Debug Mo

You've heard the announcements about MULTIBUS II specs.

But now there's an even more spectacular announcement:

The first wave of MULTIBUS II products is here.

Take the 286/100 Single Board Computer. It's the first commercially available 286-based board that runs at 8

MHz. It also introduces the iLBX II™ interface and is iSBX™ compatible.

Then there's our family of cached-based memory boards, from ½ to 4 MB, which give zero wait state performance over the iLBX II bus. And because the boards are configured in software, there are no jumpers. Anywhere.

There's software support, too, with the iRMX™ 86 MULTIBUS II support package. It supports the same tools, languages and utilities as the iRMX 86 operating system.

And for software development support, the iSDM 286 System Debug Monitor is also available. So you'll be up and running in no time with products based on the advanced MULTIBUS II architecture.

We designed the 32-bit MULTIBUS II architecture to give you a quantum leap in performance where you need it: in a multiprocessing environment.

To get such radically improved performance we had to redefine bus architectures with radically advanced concepts.

Like distributed arbitration. It breaks the bus access bottleneck and helps maximize system level performance for multiprocessing environments.

And we're taking a unique approach to interprocessor communication. It's called message passing. It'll free up

the CPU from bus management tasks and put it back to work on your application.

And the MULTIBUS II architecture has the reliability to back up that performance — reliability that surpasses everything else commercially available.

How?

By being the first open systems bus to incorporate parity protection on address, data and control lines. By being the only bus that allows every board to perform self-test.

Even the 32-bit bus inter-

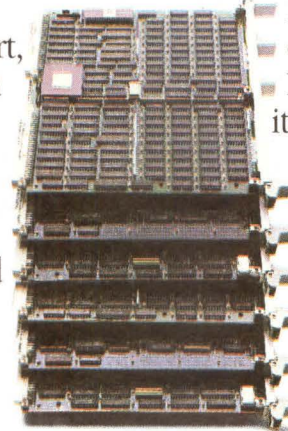
face is reliable. It not only fits onto one DIN connector, but it's been designed to be integrated onto one VLSI chip. And that's more reliable than two or three or more.

But the most important feature of MULTIBUS II is that Intel and other manufacturers are already working on dozens more MULTIBUS II products.

Just the kinds of products you need to meet the needs of your market.

For complete information, call us toll free at (800) 538-1876. Or write Intel Corporation, Lit. Dept. W225, 3065 Bowers Avenue, Santa Clara, CA 95051.

So don't miss this bus. Because you could have a short ride on any other.



SHIPPING MEMO

April 12, 1985

CODE 0404 / 348

DIVISION / DEPT.

REFERENCE THE
C. ON ALL CORRESPON-
S, PACKING LISTS, ETC.
SIG MATERIALS TO INTEL.

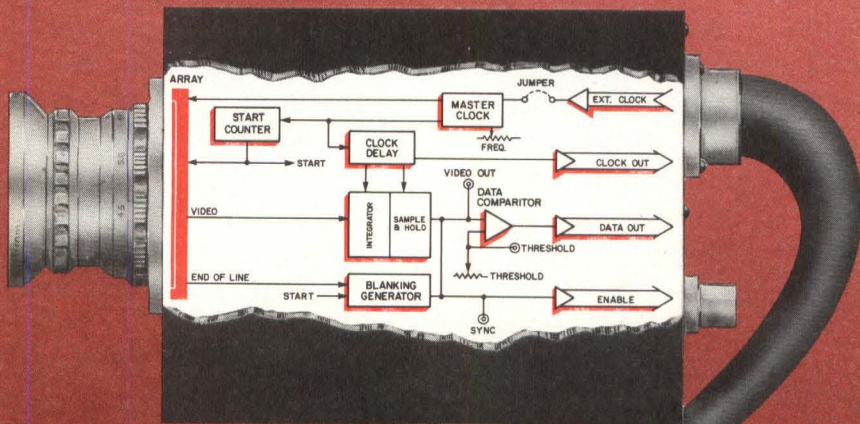


© 1985 Intel Corporation

intel®

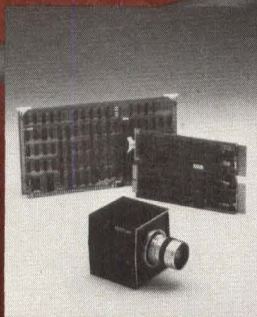
AS SIMPLE AS 1,2,3

1. Internal clock
2. Single video line output
3. From \$850 in single quantities



Reticon's LC310 Series cameras offer you an easy solution to industrial vision applications. These low-cost rugged modular cameras also feature binary output, wide dynamic range, differential line drivers, a sealed industrial case, and can be jumpered for internal/external clock and/or start.

More Reticon cameras have been used in industrial settings than any other. We also have a complete line of support products: controllers, light sources, computer interface boards and power supplies.



Using a Reticon interface board, the LC310 camera can plug into a Multibus™ or Q-Bus™.

For more information, contact:
EG&G RETICON
 345 Potrero Avenue,
 Sunnyvale, California
 94086-4197, (408) 738-
 4266, TWX 910-339-9343,
 or: Chicago (312) 640-7713;
 Boston (617) 745-7400; Japan
 03-343-4411; England (0734)
 788666; Germany (089) 92692-666.

Q-Bus™ is a trademark of Digital Equipment Corporation
 Multibus™ is a trademark of Intel Corporation

EG&G RETICON
 WHERE VISION AND TECHNOLOGY MEET

Circle 7

DIGITAL DESIGN

Editor in Chief	John Bond
Managing Editor	Debra A. Lambert
Features:	
Semiconductor Technology	Dave Wilson, Executive Editor
Electronic Imaging	Andrew Wilson, Senior Technical Editor
Design Technology	Ronald E. Collett, Senior Technical Editor
Systems Architecture	Brita Meng, Technical Editor
Technology Trends	Jack Vaughan News Editor
West Coast Technical Editors (408) 356-0405	Gregory MacNicol Joe Aseo
Copy Editor	Sherri Mack
Editorial Assistant	Tia Partin
Contributing Editor: Peripherals	Bob Hirshon
Senior Art Director	Tilly Berenson
Advertising Production Manager	Martha Watjen
Production Director	Paul Dadarria
Graphics: Supervisor Sr. Technician Sr. Technician	William Manning Jr. Don Schaaf Jan B. Seymour
Marketing Director	Charlotte King
Promotion Manager	Elaine Bull
Marketing Assistant	Sharon Lembo
Research	Carolyn Wulfsberg, Peter Micheli
Circulation Director	Hugh J. Dowling
Circulation Supervisor	Nancy McPherson
Circulation Staff	Miriam Hlister, Kelly Kudlate
Reader Service (413) 499-2550	Terri Giroux
Executive Administrator	Suzanne Levecque
Corp. Services Administrator	Janet R. Pitt
General Administration	Beth Giles, Tyrone Simpson, Mal Rankin, Debra James

President,
 Ronald W. Evans
Publisher,
 James R. DiFilippo
Associate Publisher
 Terry L. Willins

Advertising Sales

Northeast: Terry L. Willins (In MA) (617) 232-5470, (Outside MA) (800) 223-7126, 1050 Commonwealth Avenue, Boston, MA 02215

Middle Atlantic/Southeast: Richard V. Busch (609) 921-7763, 40 Stony Brook Lane, Princeton, NJ 08540

Central: Mike Prewitt (303) 696-6276, 11628 East Cornell Circle, Aurora, CO 80014

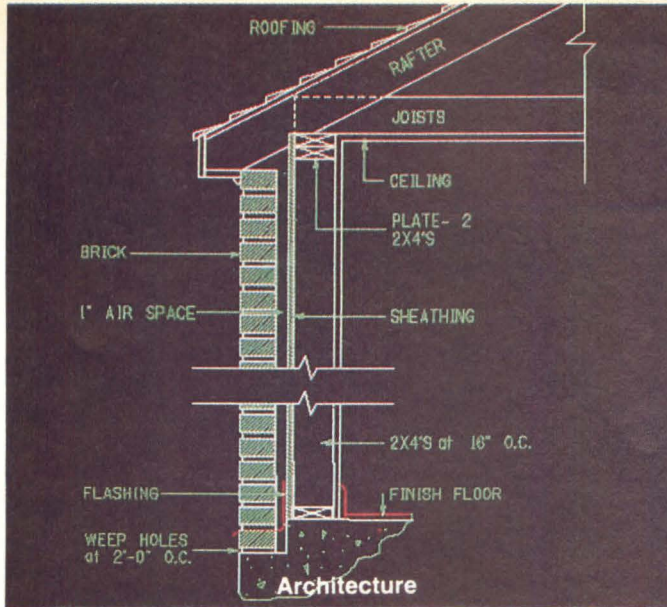
Northwest: Carole Sacino, Diane Ross (408) 356-0405, 15951 Los Gatos Blvd., Suite 7, Los Gatos, CA 95030

Southwest: Thomas A. Stillman (714) 851-8550, 2041 Business Center Dr., Suite 206, Irvine, CA 92715

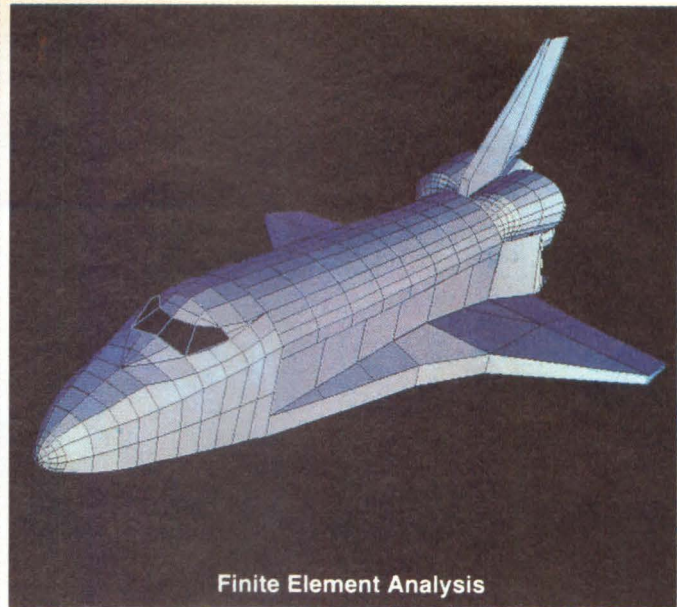
National Recruitment Sales: Brenda Stillman (714) 851-8550, 2041 Business Center Dr., Suite 206, Irvine, CA 92715

National Postcard Sales: Crickett Cunningham (In MA) (617) 232-5470, (Outside MA) (800) 223-7126, 1050 Commonwealth Avenue, Boston, MA 02215

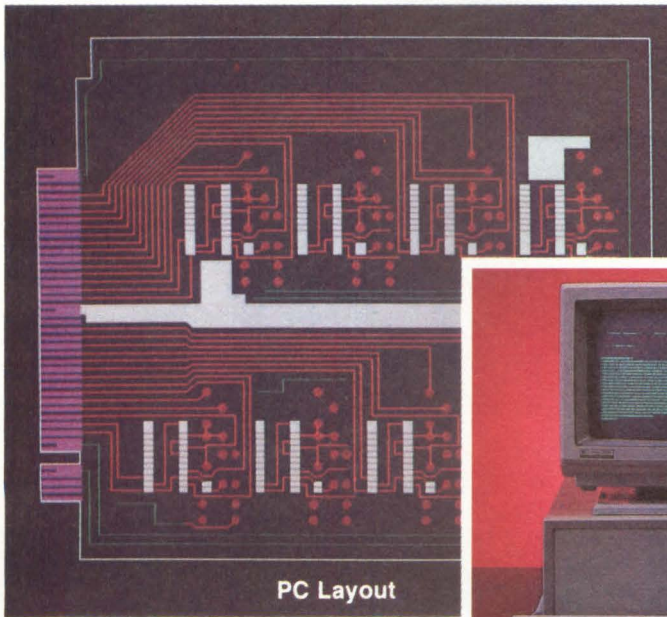
National List Rental Sales: Deb Goldstein (In MA) (617) 232-5470, (Outside MA) (800) 223-7126, 1050 Commonwealth Avenue, Boston, MA 02215



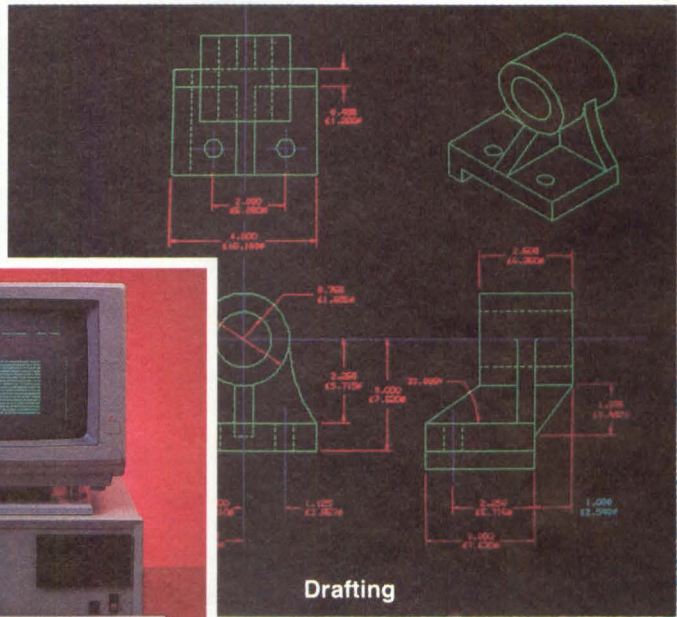
Architecture



Finite Element Analysis



PC Layout



Drafting



System Quality Graphics at a PC-Based Price. Introducing the Lundy 2000 Workstation.

Lundy 2000 is a powerful turnkey workstation that gives you sharp, high speed, high quality graphics for about what you'd pay for a fully configured pc-based system.

Turnkey Simplicity

Because it is a stand-alone workstation, you're spared from dealing with several manufacturers for different system components, as is common with most "put-together" systems. With the Lundy 2000, you're backed by a Company with a proven, solid reputation for providing fine quality graphics systems complete with service and support. The Lundy 2000 is

as dependable and easy to operate as it is effective. All of this power is packaged as a highly compact turnkey system.

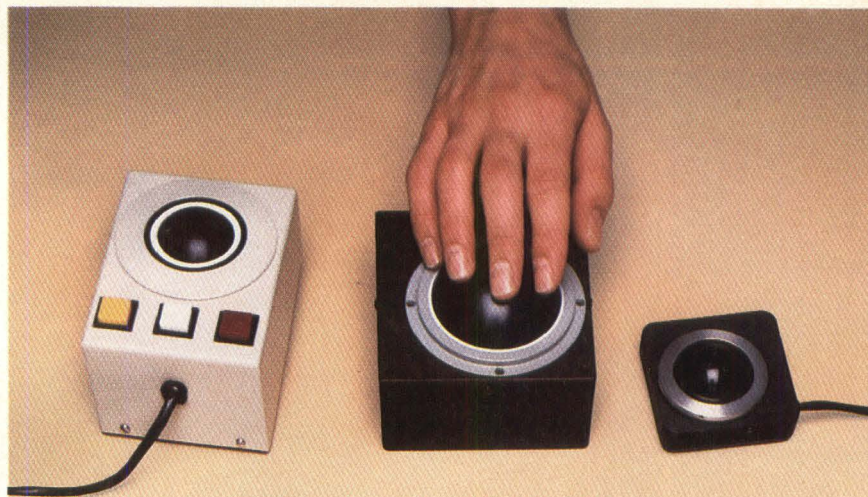
Application Flexibility

The Lundy 2000 workstation gives you fast, high quality design for finite element analysis, solids modeling, PC layout, mechanical design, and architectural applications, as well as business graphics and word processing. It displays up to 256 colors from a palette of 16.7 million and provides a 1536 x 1024 addressable map with 768 x 512 displayable resolution. Dual processor architecture

and a high speed vector generator combine to provide full pan, zoom, and preview capabilities. This gives you operational flexibility to handle special graphics processing needs not met by standard host-dependent terminals.

For more information, contact: Graphics Marketing, Lundy Electronics & Systems, Inc., One Robert Lane, Glen Head, N.Y. 11545. (516) 671-9000.





Trackballs. Flexibility at your fingertips.

When you need to get your hands on a top quality, high reliability, long life, smooth performing trackball, where can you turn for help?

Fortunately there is a solution right at your fingertips... trackballs from Measurement Systems.

You can achieve super-fast cursor movement on a CRT display and precise positioning too with a variety of ball sizes ranging from 1.5 to 3.5 inch diameter. We can offer two or three axes, a variable pulse rate output, digital outputs, low profile housing, a variety of interface options and much more.

Call or write for our new catalog illustrating our trackball products as well as our joystick and handgrip controls.

MS **Measurement Systems, Inc.**
121 Water Street, Norwalk, CT 06854, U.S.A.
(203) 838-5561

Circle 11

TELL US YOUR THOUGHTS

Digital Design is your forum—your inputs help keep the magazine interesting and vital to the

design community. So let us know how we're doing and how we can serve you better in the future. We want to know what you like or dislike about *Digital Design*, the subjects you'd like to see us address, how you feel about the problems you face every day as design professionals.

If you have thoughts your peers should know about, put them in a letter in *Digital Design*. Have your say in your magazine! Send letters and comments to: Editor, *Digital Design*, 1050 Commonwealth Ave., Boston, MA 02215.

EDITORIAL AND SALES OFFICES

DIGITAL DESIGN, 1050 Commonwealth Avenue,
Boston, MA 02215, Telephone: (617) 232-5470

ME MORGAN-GRAMPIAN

CORPORATE HEADQUARTERS

Morgan-Grampian Publishing Company, 1050
Commonwealth Avenue, Boston, MA 02215, (617)
232-5470. Brian Rowbotham, Chairman; Ronald W.
Evans, President; Charles Benz, Vice President.

EXPOSITIONS GROUP

Morgan-Grampian Expositions Group, 1050 Common-
wealth Avenue, Boston, MA 02215 (617) 232-EXPO.
The following is a list of conferences produced by the
Expositions Group:

ATE West	CADCON East
CADCON West	ATE Central
ATE Northwest	CADCON Central
ATE East	Electronic Imaging

In addition to DIGITAL DESIGN, Morgan-Grampian
publishes the following in the United States: Circuits
Manufacturing • Electronics Test

Morgan-Grampian also publishes the following in
the United Kingdom: Electronic Engineering • Control
& Instrumentation • Electronics Times • What's
New in Electronics • What's New in Computing •
Business Computing and Communications • Com-
munications Systems Worldwide.

DIGITAL DESIGN serves the manufacturers of com-
puter-related OEM products. This includes primary
computer and systems manufacturers, systems inte-
grators, components and peripheral manufacturers,
integrating OEM's and commercial end users. These
companies manufacture products used to control
machinery, equipment and information in manu-
facturing, material processing, machine tools,
packaging, health care, defense, data processing,
communications, instrumentation, and scientific
and business operations.

★ **ABP** ▽ **BPA**

SUBSCRIPTION POLICY

DIGITAL DESIGN is circulated only to qualified
research, development and design engineers and
engineering managers primarily responsible for
computer products and systems in OEM plants. To
obtain a complimentary subscription, request (on
company letterhead) a qualification card from Circu-
lation Director. For change of address, attach old
address label from recent issue to new company
letterhead or note. Send this plus request for new
qualification card to:

Circulation Department, **DIGITAL DESIGN**, Berkshire
Common, Pittsfield, MA 01201

Subscription rates: non-qualified subscribers (US
and Canada) — \$40/yr; foreign — surface mail —
\$50; air mail — \$85. Single copies — \$4.

Authorization to photocopy items for internal or per-
sonal use, or the internal or personal use of specific
clients, is granted by Morgan-Grampian Publishing
Co. for libraries and other users registered with the
Copyright Clearance Center (CCC) Transactional
Reporting Service, provided that the base fee of
\$2.00 per copy, plus \$.25 per page is paid directly to
CCC, 21 Congress St., Salem, MA 01970. 0147-
9245/84 \$2.00 + \$.25.

DIGITAL DESIGN solicits editorial material and
articles from engineers and scientists. Contributors
should submit duplicate manuscripts typed with two
spaces between lines. All illustrations should be
clear; components on all schematics and line draw-
ings should be labeled. The editors assume no re-
sponsibility for the safety or return of any unsolicited
manuscripts.

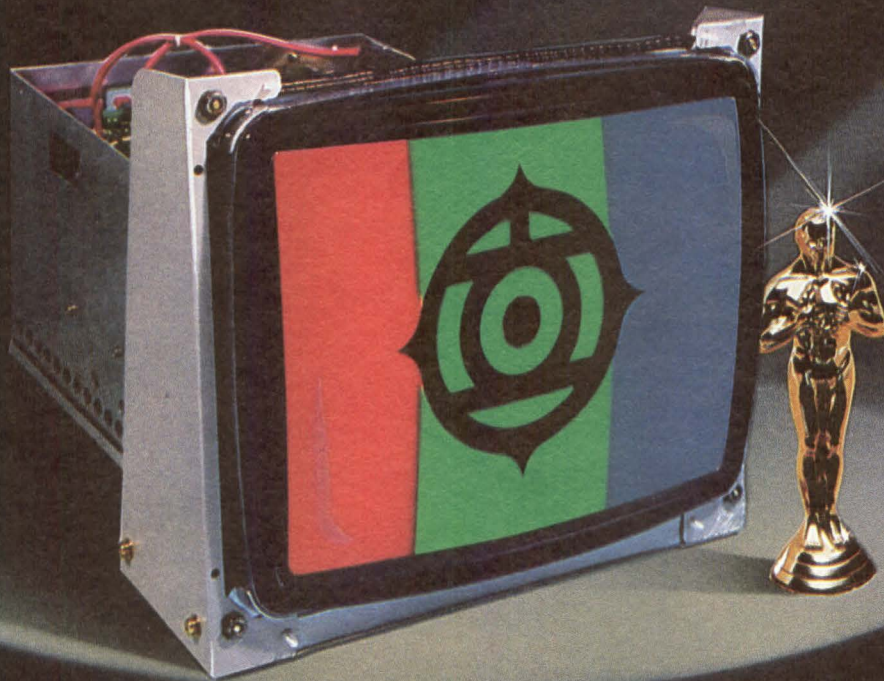
... and the winner is



for the newest technological advance
in RGB color monitor history ...

**Our square cornered, 15", compact and
affordable, hi-resolution
flicker-free desk top...**

Model HM 4615



HITACHI, the world leader in technology has done it again with the entirely new and innovative HM 4615 RGB Color Monitor.

New Hitachi gun and yoke technology brings a sharper focus and convergence to your picture; a new LSI for our Video Amplifier requires only one third the space of previous models making the HM 4615 extremely compact.

Square corners provide greater viewing area and 1024 x 800 hi-resolution is standard with 1280 x 1024 available as an option.

The Hitachi HM 4615 is economically priced, ideally suited for CAD-CAM and other desk top computer graphics systems. It carries worldwide approvals, including FCC, UL, CSA, and VDE.

For more information contact Hitachi America Ltd.

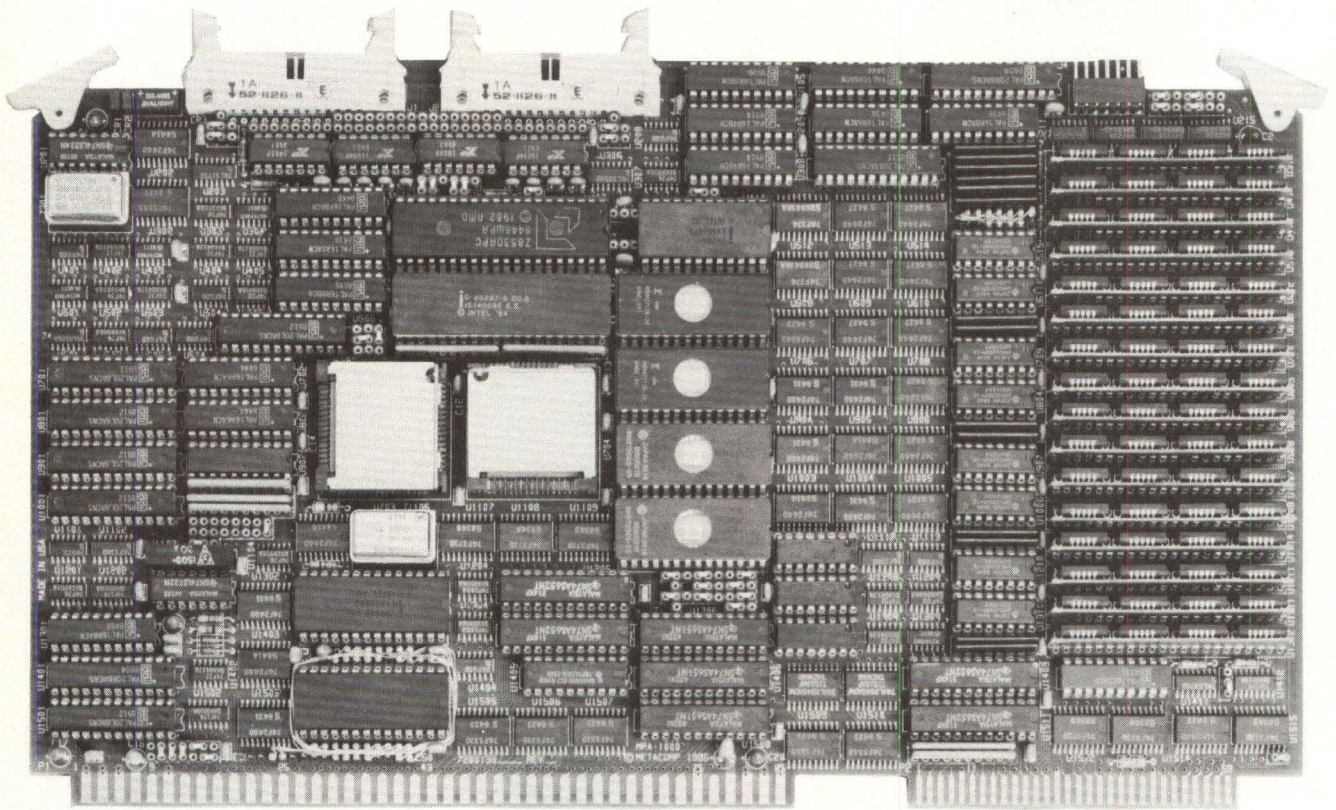
50 Prospect Avenue
Tarrytown, NY 10591-4698
(914) 332-5800

950 Elm Avenue
San Bruno, CA 94066
(415) 783-8400



The Image Speaks for Itself

HONEST ENGINE



An 80286 CPU Board Without Compromise.

The MPA-1000 is the only Multibus-compatible CPU that taps the full capabilities of the 80286 microprocessor. An honest engine, built to unleash the full potential of the 80286 in multi-user, multi-tasking or real-time applications. And it delivers the power and memory for these demanding applications all in a single card slot.

Up to 2 Mbytes of dual-ported zero wait state dynamic RAM. iLBX high speed memory bus interface. Two serial I/O ports, and programmable registers which allow flexible memory mapping and minimize option jumpers and possible configuration errors.

And for even greater performance, simply plug in the optional 80287 numeric coprocessor and the 82258 Advanced DMA Controller.

Don't compromise. Call or write METACOMP today. Discover what makes the MPA-1000 the honest 80286 engine.

METACOMP

THE MULTIBUS BREAKTHROUGH PEOPLE

METACOMP, Inc
9466 Black Mountain Road
San Diego, CA 92126
(619) 578-9840
TWX 910-335-1736 METACOMP SDG

MPA-1000 is a trademark of METACOMP, Inc.
Multibus is a registered trademark of Intel Corporation.

EDITOR'S COMMENT

More Ink On Japan Inc.

Recent cutting of 64K DRAM prices by the Japanese have led to charges of dumping. This is just another example of "dirty tricks" according to journalists, congressmen, business executives and almost everyone else. In this instance they may be right—and there are laws on the books to deal with that—if the government has the fortitude to apply the law quickly and forcefully.

We shouldn't get too righteous about it, however. Despite such occasional lapses into illegal or unfair competition, the Japanese have beaten us in the trade wars because they outperformed us in quality, manufacturing efficiency and marketing. We were once a world leader in all of those areas, and I am old enough to remember when "made in Japan" was synonymous with junk. What happened? An overpopulated island nation with very limited natural resources decided that it must trade to survive. To trade successfully, Japanese companies had to pay attention to basics and had to use technology to make themselves more efficient every step of the way. They had to gradually immerse themselves in foreign markets and make high quality, inexpensive products that customers wanted.

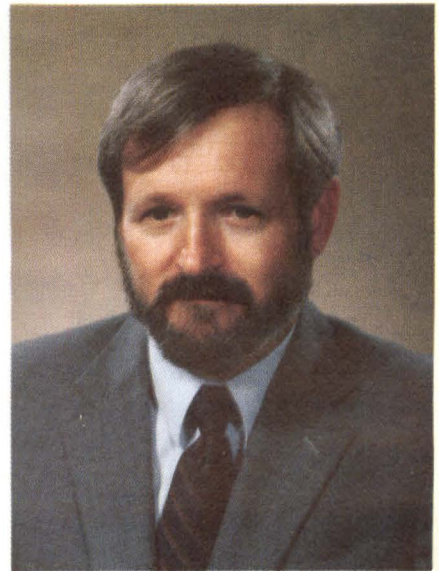
They didn't do it overnight. The 1968 Japanese car I owned, quite frankly, wasn't as good as most American cars. But it was a small car and it was cheap. It met a market need. Today, the quality problems have been resolved and it is American manufacturers who must catch up. Generally, this is the approach that Japanese companies follow: Find a market niche that is not well served. Establish a reputation based on quality and price. Expand into other segments of the market. There's nothing magic about it. It takes long-range vision and hard work.

While the Japanese were learning how to compete in international markets, the Americans were handing over their companies to managers with financial backgrounds. These managers, often adorned with MBA degrees, performed as might be expected—emphasizing short-term profits at the expense of the long-range good of the company. Since they had little experience with engineering, manufacturing and marketing, such vital functions got short shrift compared to financial considerations. That is beginning to change in our larger companies and indeed in small entrepreneurial companies we have always had engineers and marketers in charge. As a result, smaller companies have been more innovative than large companies although they may not have the clout to compete internationally.

Many large American companies do compete successfully in Japan. In computers and semiconductors, IBM and TI are notable for their strong positions within the Japanese market. Motorola and Tektronix are successfully challenging the Japanese on several fronts. And many other companies are gearing up to do battle.

The Japanese are not as invincible as they seem. Manufacturing is their strong point, but even so, they are competitive on the world market in only a handful of mass production industries that employ less than 15% of Japanese workers. The second tier of Japanese companies, uncompetitive by international standards, competes fiercely for domestic markets. Bankruptcies and layoffs are the price they often pay. Only the large, successful companies can afford lifetime employment. Out of that crucible have come those few Japanese companies that the US electronics industry must compete with internationally. They are tough, worthy competitors who can teach us something. They didn't do all that with company songs and trade barriers.

— John Bond, Editor in Chief

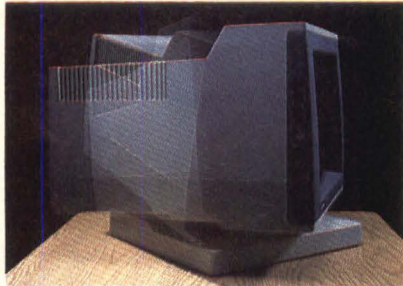


LEXIDATA. LOOKING GOOD.

HIGH-PERFORMANCE COLOR GRAPHICS SYSTEMS.

We're looking good for a lot of good reasons.

Our family of high-performance, raster graphics display processors



Lexidata's monitor enclosure design features a unique tilt and swivel movement with smooth and easy operation. All monitor connections and peripheral power supplies are located in the enclosure's base.

and subsystems are recognized worldwide for their ability to cost-effectively reduce the picture-processing workload of host computers.

They're being used to find oil, design motorcycles, treat hospital patients, compose magazines, and trace the movement of military troops. And as many applications as there are now, there are many more to come.

HIGH-PERFORMANCE COMPANY.

For over a decade, Lexidata™ has been advancing color graphics technology, especially in the area of computer-aided design, where our systems are being successfully integrated by OEMs and end-users.

We've set some very high stand-

ards for our systems. And we see to it that they're built cost-effectively so they can be priced the same way.

OUR RESOLUTION: INTELLIGENT SOLUTIONS.

We offer a variety of systems with a variety of resolutions.

LEX 90™ is Lexidata's newest family of raster display processors. There's a LEX 90 model that can support up to 24 planes of 1280x1024 display memory at 60Hz non-interlaced refresh.

There's SimulRes, which allows the simultaneous display of 640x512 and 1280x1024 images on the same screen.

There's GEOVIEW™, a three-dimensional geological interpretation package.

And for solid modelers, there's the extraordinary capability of SOLIDVIEW™. Lexidata's patented z-buffer technology for the display of solid models.

If you need

an intelligent low-cost color or monochrome 1280x1024 graphics terminal, with PLOT 10™ or VT100™ emulation, our Series 2000 is available featuring a powerful 16/32-bit 68000 microprocessor.

And, of course, all Lexidata systems are compatible with a variety of leading third party application

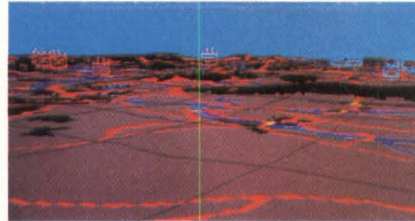
software packages for mechanical design/analysis, business graphics, mapping, and geological interpretation.

TAKE A CLOSER LOOK. Lexidata systems are hard at work around the world, helping companies realize their goals in all kinds

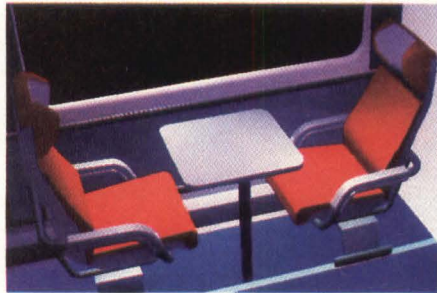
of applications. These companies have found powerful, cost-effective solutions that can do the job for them now, yet grow with them later.

If that sounds like your kind of company – or your kind of customer – then we should talk.

Call us at 1-800-472-4747. In Massachusetts, call 617-663-8550. Or write: Lexidata Corporation, 755 Middlesex Turnpike, Billerica, Massachusetts USA 01865. TWX: 710-347-1574. In UNITED KINGDOM call: Lexidata, Ltd., Hook (025672) 3411. In FRANCE call: Lexidata SARL, Rungis (1) 686-56-71. In JAPAN call: Lexidata Technical Center, Tokyo 486-0670.



Computer-driven command and control battle simulators are using Lexidata graphics systems to display 3-D terrain appreciation maps. (Courtesy of The Singer Company, Link Simulation Systems Division)



Students at the Royal College of Art in Kensington, England, use Lexidata's SOLIDVIEW to create designs such as these first-class passenger train seats.



LEXIDATA
LOOKING GOOD.

HOTLINE

PC-ON-A-CHIP AVAILABLE SOONER THAN LATER—NEC (Mountain View, CA) has beaten Intel in the race for the PC-on-a-chip (*Digital Design*, Sept., p. 29). Intel, slated to announce its 80886 by mid-1986 will now have to compete with NEC's CMOS μ PD70208 and 70216, which offer all functions of the Intel chip plus serial I/O, 8088 emulation and instructions for packed decimal strings.

GRAPHICS CONTROLLER ICs BOW AT WESCON—Next month's Wescon in San Francisco will mark the launch of four graphics chips from major semiconductor vendors. National Semiconductor (Santa Clara, CA) will describe a four-chip chip set comprising a raster graphics processor, a bit-block transfer engine, plus a video clock generator and shift register. Motorola (Austin, TX) will present the 68490, a RISC-type 68000 coprocessor with an on-board raster engine. NEC (Mountain View, CA) will announce the V40 MPU and a 256K video RAM. Finally, Intel (Santa Clara, CA) will announce two text and graphics processors, the 82716 and the high-end 82786.

STORING IMAGES ON FLOPPIES—This is the goal of a system under test by Eastman Kodak (Rochester, NY). The system will allow users to display photographic images on TV sets and to produce hard-copy from those images. The first component available commercially will be the Video Imager, a system that produces instant color prints from video images. The unit, which features both RGB and NTSC inputs, can be used to expose color prints from these inputs in one-tenth sec.

FACTORY LANS GET ON THE MAP—Industrial Networking Inc. (Santa Clara, CA), the joint venture of GE and Ungermann-Bass, has released the MAP/One local area network for the factory. This broadband token-bus LAN claims the first board-level interface capable of supporting the entire MAP specification backed by General Motors. The MAP/One boasts a 10-Mbit/sec modem board.

ACCELERATOR FOR CAE—Mentor Graphics (Beaverton, OR) has announced a hardware accelerator that speeds the entire range of compute-intensive CAE tasks. The new Compute Engine accelerator is a parallel processor system that uses RISC concepts and extensive pipelining to produce throughput as high as 10 MIPS.

DSP CHIPS FORM THE HEART OF AN IMAGING SYSTEM—From Sky Computer (Lowell, MA), the VME-based image processor, dubbed Challenger, will use two 32020 chips from TI (Dallas, TX) to process images. A PC/AT version is expected next year. Also, Sky plans to introduce a 64-bit processor, the Vortex, which will implement full IEEE 64-bit precision and cost less than \$10,000.

ALCHEMY LIVES—An alloy with the properties of gold could soon appear in electronic components. Developed by Allied Corp (Morristown, NJ), the material is called Altraloy. It contains no precious metals and can be electroplated directly on top of copper alloys without the need for a nickel underplate. Altraloy reportedly combines solderability and low contact resistance.

STANDARDS FOR UNIX AND CAD/CAM/CAE FILE SHARING—Sun Microsystems (Mountain View, CA) is working with AT&T to offer a common UNIX system merging System V with Sun's version of 4.2. At the same time, Sun's proposed file sharing standard has gained several recent adherents including Celerity Computing (San Diego, CA) and Sequent Computer Systems (Portland, OR). Dubbed the Network File System (NFS), the proposed standard will let diverse CAD systems communicate. Sun will license the NFS source code to manufacturers and software houses.



FOR VMEbus CPU MODULES, CALL MIZAR.

612-224-8941

We have the CPU module that fits. Our top-quality single- and double-height CPU modules support the 68000 family of microprocessors at speeds of 8, 10 and 12.5 Mhz; have on-board memory from 16K bytes to ½M of RAM; and have 32K bytes to 128K bytes of EPROM. Double-height modules have many additional features.

For full details, call Mizar...
the VMEbus authority.



MIZAR INC.

302 Chester Street
St. Paul, MN 55107
(612) 224-8941
Telex: 469542



FOR VMEbus I/O MODULES, CALL MIZAR.

612-224-8941

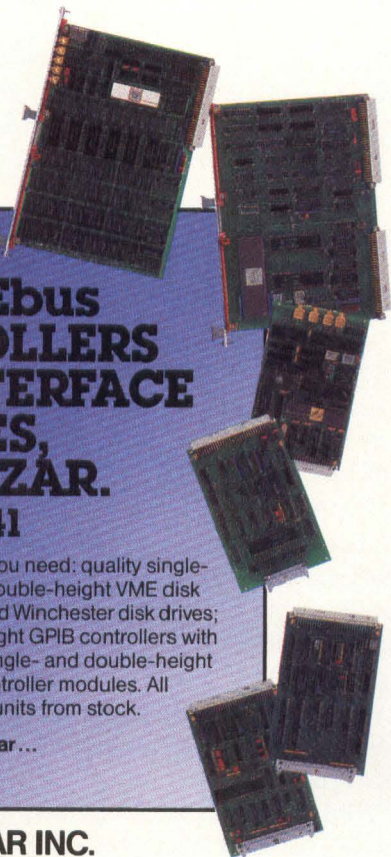
Our top-quality line of single-height I/O modules includes Quad Serial Port and Quad Parallel Port cards, Analog Input and Output cards, and Counter-Timer card. Our double-height 8-channel serial communications processor is an intelligent self-contained VMEbus serial communications center.

For full details, call Mizar...
the VMEbus authority.



MIZAR INC.

302 Chester Street
St. Paul, MN 55107
(612) 224-8941
Telex: 469542

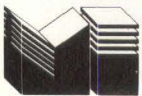


FOR VMEbus CONTROLLERS AND INTERFACE MODULES, CALL MIZAR.

612-224-8941

We have the modules you need: quality single-height and intelligent double-height VME disk controllers for floppy and Winchester disk drives; single- and double-height GPIB controllers with or without DMA; and single- and double-height video and graphics controller modules. All available in evaluation units from stock.

For full details, call Mizar...
the VMEbus authority.



MIZAR INC.

302 Chester Street
St. Paul, MN 55107
(612) 224-8941
Telex: 469542



CALL MIZAR. THE VMEbus AUTHORITY.

612-224-8941

You can't beat Mizar for top-quality VMEbus boards, systems, software... and service. We have a complete line of VMEbus products... single- and double-height CPUs, memory modules, controllers, and I/O modules; auxiliary hardware; and operating systems and software. Call us to discuss how we can help make VMEbus technology work for you. We're Mizar... the VMEbus authority.



MIZAR INC.

302 Chester Street
St. Paul, MN 55107
(612) 224-8941
Telex: 469542

TECHNOLOGY TRENDS

SYSTEMS

Cruncher Enters Multiprocessing Arena

As the industry sees a parade of computer systems claiming parallel processing capability, the near-religious question is often asked: how parallel are you? But, as the machines leave the labs and enter the marketplace, the distinctions between approaches will likely blur. Pipelining, multiprocessing, loosely and tightly coupled architectures, single instruction multiple data (SIMD) and multiple instruction multiple data (MIMD) paths — designers will opt for variations on these themes as their next-generation architectures meet the real world.

With the introduction of the 3280, or Cruncher, Perkin-Elmer (Oceanport, NJ) seeks to establish itself as a properly parallel contestant in this arena. The system, which is an extension of the 3200 computer series, perhaps fits more comfortably in the multiprocessor category. But, evolving 3200 series design shows how different parallel categories can merge to improve performance.

The 32-bit 3280 boasts 4-MIPS throughput in its uniprocessor configuration. In a multiprocessor set-up, the machine can be configured with up to five attached (or auxiliary) processor units (APUs) and achieve 22-MIPS performance. The APUs can be dedicated to computation or I/O functions. Each processor has equal access to a global memory, and high-speed set associative instruction and data caches are used. Using a Fortran compiler, an increasingly important tool in parallel and multiprocessor design, a fully configured 3280MPS can run 65 million whetstone instructions per second.

In the multiprocessor configuration, each attached processor assumes only

one role. Thus, the set-up strays from "true" parallelism. Perkin-Elmer chooses to define parallel processing as two or more interconnected processors simultaneously performing different portions of the same application. As an example they cite a financial services application in which the CPU handles system control and database management while the APUs handle trading activity or rating revision tasks. APUs can be array processors. In an automobile suspension modeling application, an APU is dedicated to simulate operation of each of the car's four wheels. In a field mostly noted for start-ups, Perkin-Elmer likes to trace its parallel processing lineage back through several years and several design iterations.

The 3280's performance ratings represent a marked increase over its 3230 and 3260 model predecessors. This seems more due to evolutionary design refinements than to dramatic architectural departures. Like most superminis, the 3280 implements pipelining — the most basic form of parallelism. In 400 nsec, a 3280MPS completes a single instruction and performs operations on the next three instructions in queue. This marks the first appearance of a four-stage instruction pipeline in the 3200 series. Interlock circuitry controls the pipeline process and the 3280's instruction set is tailored for pipeline utilization.

Each 3280 processor contains two 8-Kbyte caches with two-way associative organization. Cache memory is based on a 45-nsec NMOS implementation. Memory ranges from 2 Mbytes to 16 Mbytes. The system supports composite

memory modules (CMMs) which each have on-board controllers. Four-way interleaving among multiple CMMs allows fast, concurrent memory access. Main memory is composed of 120-nsec, 64-Kbit MOS dynamic RAMs. Serving as a pathway for processor-to-processor communications, a 64-Mbyte/sec system bus assures high throughput and provides control functions. This bus supports positional priority within three priority levels: high priority, round robin priority and simple priority.

Evolving throughout the 3200 series history, Perkin-Elmer's optimizing Fortran compiler has become an important factor in achieving high performance. It features universal optimization that is said to eliminate overhead in subroutine calls, allowing full exploitation of structured programming. Further, Perkin-Elmer offers a set of microcoded routines that, used with the writable control store, speed the Fortran compiler's operation by 30%. With the thought that compilers are notoriously "register hungry," the 3280 furnishes eight sets of sixteen general-purpose 32-bit registers, one set of eight single-precision floating point registers (32-bits each), one set of sixteen 32-bit scratch pad registers and one set of eight double-precision floating point registers. Stacked-up against the VAX 8600, which has itself become a benchmark of sorts for its competitors, Perkin-Elmer estimates that the 3280MPS costs \$30,000 per MIPS versus an estimated \$100,000 per MIPS for a VAX 8600 cluster.

—Vaughan

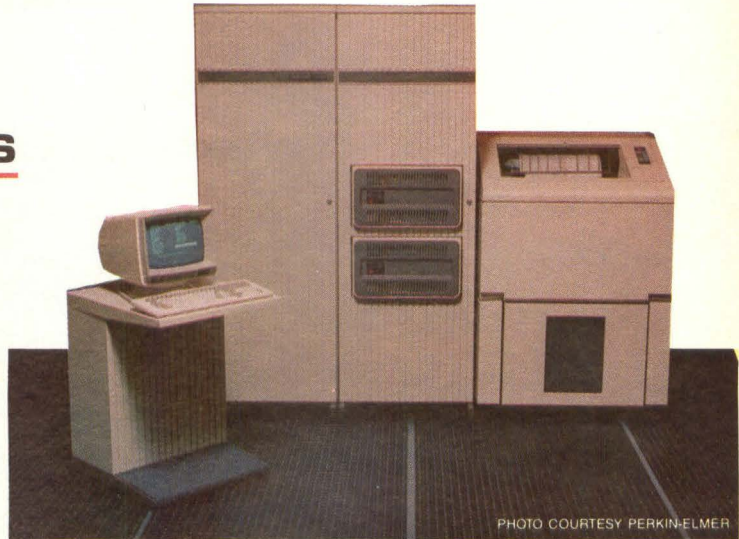


PHOTO COURTESY PERKIN-ELMER

We run with a great crowd.

Complete hardware/software compatibility.



Talk about easy interfacing. You can take a ZETA 824 or ZETA 836 plotter and plug it into virtually any computer made.

What's more, you'll be ready to run because our plotters understand a variety of computer protocols. Select the model for your application then just plug in and plot.

In fact, we're a plug compatible replacement for many plotters from HP, CalComp and Tektronix. Some models of our plotter can even run directly from your IBM cluster controller. Now that's easy interfacing.

When it comes to your favorite application packages, you'll be on safe ground too. Packages such as CADAM, TechniCAD, Euclid, P-CAD, AutoCAD and many more.

The most productive plotter for the money.

You'll be getting the highest output plotters for the money with our new ZETA 824CS and ZETA 836CS. More

finished plots. More productivity. Plus, these "D" and "E" format plotters let you run either single sheet or roll media.

Easy-to-use touch controls.

Your time is valuable. So we've made our touch controls simple – yet powerful. Set speed, pen pressure, liquid ink parameters, electronic limit sensing, windowing, scaling – all at the touch of a finger. Self-test and diagnostic plots too. Let us show you dozens of other time-saving operations in a brief demonstration.

Plotter specialists.

We've been designing hardware interfaces, plotting language emulators and high performance pen plotters for over 14 years. Nicolet also provides you with worldwide sales and service support.

Give us a call. See how easy it is to join the crowd.

Call (415) 372-7568.
Nicolet Computer Graphics
Division, 777 Arnold Drive,
Martinez, CA 94553
TWX 910-481-5951



Nicolet
Computer Graphics Division

CADAM is a trademark of CADAM, Inc.
TechniCAD is a trademark of Tektronix, Inc.
Euclid is a trademark of MATRA DATAVISION, Inc.
P-CAD is a trademark of Personal CAD Systems.
AutoCAD is a trademark of Autodesk, Inc.

Circle 18 on Reader Inquiry Card

ICS

Systems On A Chip Via 20,000-Gate Array

Fast high-density gate arrays provide the building blocks for placing entire systems on a chip. In fact, recently announced CMOS offerings boast 20,000 gates with typical propagation delays under 1 nsec. Users wishing even faster circuit speeds can choose from several bipolar arrays ranging from 3400 to 8000 gates with internal bandwidths exceeding 100 MHz. This wide range of sizes and speeds enables circuit designers to dispose of SSI/MSI devices in their applications, shrinking board size and power consumption while increasing overall system throughput.

To make this task easier, vendors provide a wide array of tools that help users design systems on a chip. Sophisticated timing analyzers identify critical paths that are then routed automatically. In addition, large macrocell libraries composed of such elements as 16-bit register files and multipliers move the level of design from individual gates to logical functions with users also able to select the most desirable speed and power.

Designers wishing to pack the largest amount of random logic on a single chip or build single-chip systems can consider CMOS gate arrays available from Fujitsu Microelectronics (Santa Clara, CA), Honeywell Digital Product Center (Colorado Springs, CO) and NEC Electronics (Mountain View, CA). With 20,000 gates available on a single chip, circuit designers can expect as much as a 2000:1 reduction in system component count when compared with similar systems built using conventional SSI/MSI CMOS or TTL logic functions. Power dissipation also shrinks dramatically with an entire array consuming around

2.5W under nominal voltage and temperature conditions.

Propagation delays also shrink as gate counts increase. Typical delays under conditions of room temperature and nominal voltage (5V) range from 0.63 nsec to 0.79 nsec, yielding an internal bandwidth exceeding 30 MHz. However, designers must be aware that increasing the number of gate-level fan-out limitations will present penalties. For example, moving from one fan-out to three could easily add another 0.3 nsec delay for the Honeywell gate array under the same temperature and voltage conditions.

Designers can overcome these limitations by taking advantage of functions like multipliers, multiplexers and register files contained in each vendor's macrocell library. These predefined LSI/VLSI functions are optimized for minimum propagation delays.

Fujitsu Microelectronics has taken the macrocell approach another step by organizing its array into four 5,000-gate quadrants. Using hierarchical design rules, designers first specify the architecture of the entire chip, then move in succession to specify the layout of individual quadrants in terms of 1000- and 2000-gate blocks and then individual macros and gates if desired. With this approach, designers can readily identify critical

paths for special routing. The company also provides arrays that mix random logic with static memory in 6-Kbit and 12-Kbit configurations.

With large gate counts and low power, CMOS arrays prove ideal for shrinking the size of many systems implemented in discrete logic. Yet, bipolar arrays provide internal bandwidth easily three to four times faster than possible in current CMOS processes. Mark Friedmann, strategic marketing manager with Applied Microcircuits (AMCC) (San Diego, CA) claims that the company's arrays can accommodate internal bandwidths of 100 to 300 MHz for telecommunications and data acquisition applications or bandwidths exceeding 50 MHz for computationally intensive tasks found with mainframe computers or array processors. Fujitsu, Honeywell and Raytheon Semiconductor (Mountain View, CA) have also announced bipolar arrays.

Users can easily be deceived when first comparing CMOS and bipolar arrays. Although touted as having gate-level propagation delays of 0.73 nsec to 1.7 nsec, CMOS arrays tend to be at least 40% slower than comparable bipolar gates when temperature, voltage and process derating factors are considered. In addition, bipolar arrays have fewer problems in driving large fan-outs (as many as eight



The C20000 CMOS gate array from Fujitsu Microelectronics mixes high-speed static RAM with random logic. Configuration shown consists of 15,000 uncommitted gates with 6 Kbits of RAM.

TECHNOLOGY TRENDS/ICs

loads) so users can design high-speed applications using small macrocells or individual gates.

On the other hand, bipolar arrays are susceptible to timing problems caused by interconnect wiring. Interconnect delays can easily equal or exceed a function's internal propagation delay. As a result, critical path analysis is a key factor in circuit optimization. Vendors provide extensive timing analysis in conjunction with logic simulation so race and hazard conditions are identified early, and critical sections are routed efficiently. Vendors also resimulate the array after routing to ensure that critical paths meet performance criteria.

AMCC and Raytheon allow users to

program the speed of selected portions of the array. By selecting from high- and low-speed versions in each vendor's macrocell libraries, users are assured that speed-critical portions of circuits have been optimized without dramatically increasing the array's power consumption. Friedmann notes that this approach can easily keep total power dissipation under 4W. However, increasing the array speed to that of critical paths could bump power dissipation to 8W. AMCC offers four different levels of gate delays (275, 350, 500 and 700 ps) for a 2-input NAND gate, while Raytheon limits its arrays to two: 0.9 nsec and 1.5 nsec for a 2-input NAND gate.

Designers must look at the quality of

the support tools to determine whether entire applications can be placed on a single chip. Macrocell libraries should be sufficiently large and varied so that designs need not be implemented using gate-level constructs. In addition, timing analysis should be an integral part of logical simulation so that critical paths can be easily identified and accommodated. Finally, place-and-route software should provide minimum interconnect lengths between logical functions as well as efficient distribution of I/O and control signals. Lapses in any of these areas will compromise the performance of the entire array.

—Aseo

UNPRECEDENTED MTBFS

If you're using Anritsu tape drives or sub-systems to back-up your disks, you already know there's extraordinary reliability behind them.

Like an average MTBF of 7400 hours on 1/2" streaming tape drives. And 10,000 hours on our 1/4" cartridge drives.

A VARIETY OF TAPE DRIVE OPTIONS

Our continually expanding line of rack-mountable tape drives meets your varied storage needs. For low-cost 1/2" start/stop digital magnetic tape drives consider the DMT 3000 Series. Simple to operate and maintain, their excellent tape interchangeability lets you use a variety of tapes while accommodating ISO, ANSI, ECMA and IBM standard interface (PERTEC) formatted tape drive is also available.

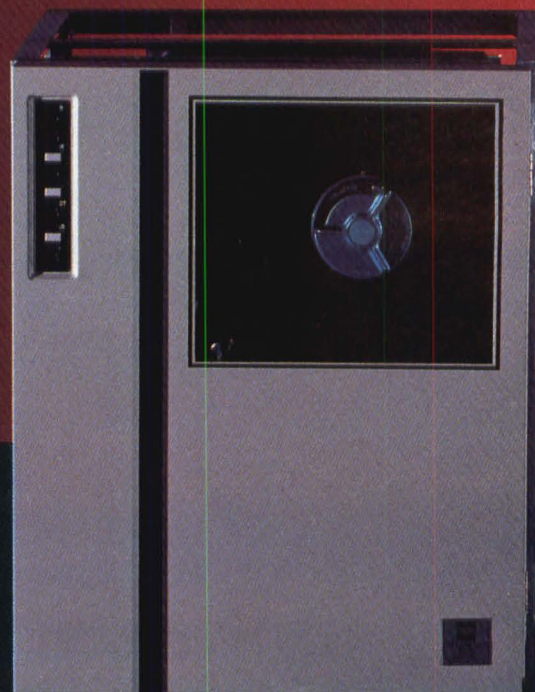
Our DMT 2500 Series 1/2" streaming tape drives, for example, deliver data capacity up to 138 Mbytes. Automatic loading and threading. Dual tape speeds of 100 and 25 ips. ANSI/IBM compatibility at either 1600 or 3200 BPI. And a model with cache memory for even more efficient data transfer.

DMT 2500 SERIES EXCLUSIVE

6000 Gate CMOS Chip Improves Reliability and Lowers Cost.

Anritsu Corp., Tokyo, Japan

ANRITSU TAPE DRIVES.



DMT 3000 SERIES

Mainframe-Style Architecture Joins Microprocessor Fray

Aiming its sights at multitasking applications, Fairchild Camera and Instrument (Palo Alto, CA) has announced a 32-bit microprocessor chip set called the Clipper. The Clipper consists of three chips: a single 32-bit microprocessor and two integrated cache/MMU chips. One cache (ICAMMU) handles instructions and the other (DCAMMU) is for data. Fabricated in a 2-micron CMOS process, the chip set runs on a 33-MHz single-phase clock and is projected to exceed a

5-MIPS average performance level.

As shown in **Figure 1**, the Clipper provides separate bus paths for instructions and data. Each bus is a full 32-bit multiplexed address/data bus, operating with a 30-nsec cycle time. An additional 32-bit multiplexed address/data bus is provided by each CAMMU to interface with main memory and I/O peripherals. Called the Clipper bus, this path operates at either one-half or one-quarter of the CPU clock frequency. By using multiple buses, Fairchild has overcome the limitations im-

posed by a single-bus microprocessor architecture.

Based on performance measurements of a 68020 requiring transfer of 8.6 bytes (3.3 instruction bytes and 5.3 data bytes) per instruction executed, Fairchild notes that a single-bus architecture would require a bandwidth of 43 Mbytes/sec. In terms of a single 32-bit bus, a word would need to be transferred at the unrealistic rate of once every 70 nsec.

By separating the instruction and data bus and by providing separate caches, the highest bandwidth is reduced to 26 Mbytes/sec, or an average of one word every 160 nsec. When references to 400 nsec main memory are factored in, aver-

EXTENDED LIFE BACK-UP FOR PEOPLE WHO THINK AHEAD.

Additionally, the Anritsu DMT 730 Series offers two cost-effective 1/4" cartridge tape drives. One even operates on a command set identical to 1/2" tape drives, so there's no need to modify your existing tape handlers. These drives also offer either serpentine or separate channel recording options in both streaming and start/stop modes.

ANRITSU QUALITY

We've earned an outstanding record for quality and performance that's helped sell thousands of our devices world-wide, as either a primary or a second source. That's because, like anyone who wants to stay ahead, we won't settle for less a quality product. And neither should you.

For all the information and back-up you need, contact: Computer Products Marketing, Anritsu America, Inc., 128 Bauer Drive, Oakland, NJ 07436. (201) 337-1111. 1-800-255-7234.



DMT 2500 SERIES



DMT 730 SERIES

Anritsu
ANRITSU AMERICA, INC.

TECHNOLOGY TRENDS/ICs

age access times only grow to 130 nsec — well within the data and instruction transfer rates needed to sustain the targeted 5-MIPS execution range.

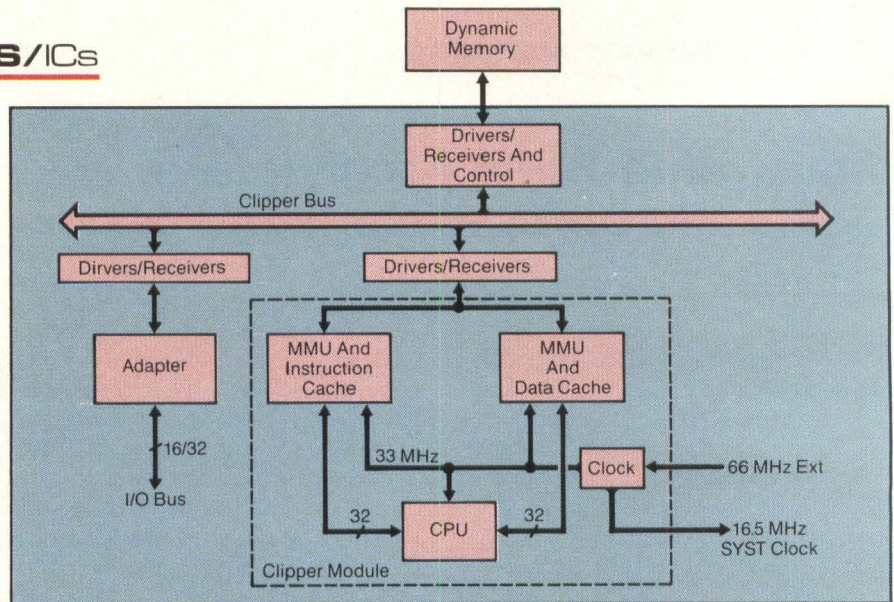
Combining both the cache and the MMU on the same chip reduces the bus loading and eliminates chip-to-chip delays. This results in faster access times. Each CAMMU supports a 4-Gbyte virtual address space and has an on-board 64 entry two-way set-associative TLB (translation look-aside buffer) containing the most recently used translations. Overlapping the cache access with the MMU provides a 33% access time improvement.

Using concepts developed under the UC Berkeley RISC and Stanford MIPS projects, the Clipper processor implements a register-to-register architecture with multiple register sets and a load/store interface to memory. Instructions are decoded and sequenced using hardwired logic instead of microcode and a pipelined execution unit performs all register operations. All nonmemory reference instructions operate only on register. All memory reference instructions pass data between one memory location and one register.

Four functional blocks make up the actual CPU: an integer pipeline, a register file, a 64-bit floating point unit and macrocode ROM. The integer pipe has three stages: fetch registers, ALU operations and register store of ALU results.

Each stage in the pipe is synchronous and a bypass path is provided to use the result of an ALU operation in the next sequential instruction. The ALU handles address computations as well as data manipulations, and nine addressing modes are supported. The register file supports three independent sets of 16 general-purpose registers, a supervisor set, user set and a special function set used with the macrocode ROM. In addition, the floating point unit has its own set of eight 64-bit registers.

Complete prefetch logic supports an 8-byte instruction buffer. Together with the program counter in the ICAMMU, this logic keeps the CPU full of instructions and immediate operands. The im-



The Clipper processor from Fairchild Camera and Instrument provides parallel processing in a uniprocessor configuration with separate floating point and integer units as well as an independent I/O bus.

mediate operands are routed directly to the integer pipe for use as data values or address offset. Instructions are sent to the issue, timing and branch control sections where they are decoded in hardwired logic, which transmits control signals to both the integer pipe and FPU logic.

A small (2000 instruction) macrocode ROM is used to execute strings of standard machine instructions. Thus, the basic architectural efficiency is maintained while additional complex instructions are provided.

An IEEE standard floating point unit resides on the chip. Clipper designers feel that this approach is superior to the common coprocessor scenario. A coprocessor attached to the CPU data cache interface, Fairchild designers indicate, would have slowed the CPU, adding a clock cycle to the access time of the cache. A load or store operation reportedly takes 4 to 6 clock cycles. This would cause a 16% to 25% slow down in operation, resulting in the CPU speed slowing by 8% to 16%.

The Fairchild announcement comes at a time when other processor manufacturers have also disclosed information about their CMOS product lines. For its part, Intel (Santa Clara, CA) has formerly announced its CMOS 386 proces-

sor this month (p. 32 this issue). By the first quarter next year, Intel will have both Multibus I and Multibus II boards to support systems integrators.

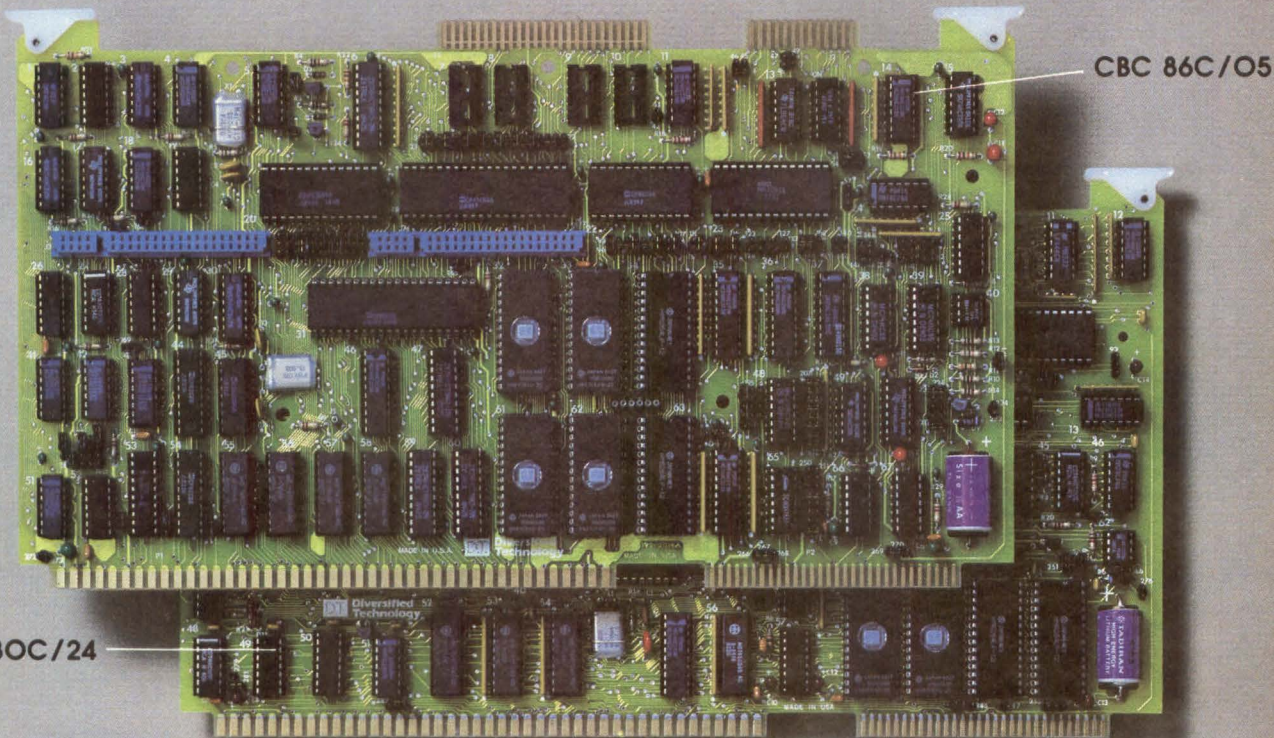
A recent disclosure by Motorola (Austin, TX) has revealed that the company will announce a 2 micron CMOS version of the 68000 in a similar time-frame. A co-development with Hitachi (San Jose, CA), the part will be followed by DMA, graphics and disk controller parts.

Finally, Inmos (Colorado Springs, CO) has announced the availability of its Transputer product, together with several development system environments. Three evaluation boards were announced this month — the B001, B002 and B004. The first product, the 001, includes a transputer, 64 KBytes of static RAM and two RS-232 ports. The 002 differs only in the fact that the user has the option of 1 to 2 Mbytes of DRAM instead of the static RAM on the 001. The third product, the 004, plugs directly into an IBM PC. Available in November, the board contains a Transputer and up to 2 Mbytes of memory. Three transputer development environments will be supported by Inmos, one for Stride computers, one for Digital Equipment's VAX line and one for the IBM PC.

—Aseo

Diversified Technology's CMOS MULTIBUS* CPU BOARDS

Give You MULTIBUS Specs In Cool CMOS Designs



Five CPU Boards Provide a Wide Range of Performance:

	CBC86C/14	CBC86C/O5	CBC88C/25	CBC85C/24	CBC80C/24
CPU	80C86	80C86	80C88	80C85	NSC800*
Speed	5 or 8 MHz	5 or 8 MHz	5 or 8 MHz	2.42 or 4.84 MHz	2.5 MHz
On-board RAM	32Kb	16Kb	16Kb	8Kb	8Kb
Parallel I/O Lines	24	24	24	48	48
RAM/ROM Sockets	4	4	4	4	3
5V Operating Current	<200mA	<200mA	<200mA	<150mA	<150mA
Availability	1Q, 1986	Now	3Q, 1985	3Q, 1985	Now

In addition, all of DTI's CMOS MULTIBUS* CPU boards have the following features:

- 0° to 70° C operating temperature ranges (-40° to 85° C available)
- Compatibility with other manufacturers non-CMOS boards
- Software compatibility with popular Intel boards

- Optional math hardware modules (80C88, 80C86 only)
- Fast CMOS static RAM
- Optional RAM/ROM piggyback expansion boards
- One RS-232 port; two ISBX* connectors
- Optional CMOS ISBX* modules available
- High-Rel versions available

So whether your application is an existing system upgrade or a low-power CMOS system design, DTI's CMOS MULTIBUS CPU boards will make your job easier.

For more information regarding these or any of our other all-CMOS MULTIBUS boards, contact Bill Long, CBC Product Manager at **(601) 856-4121**

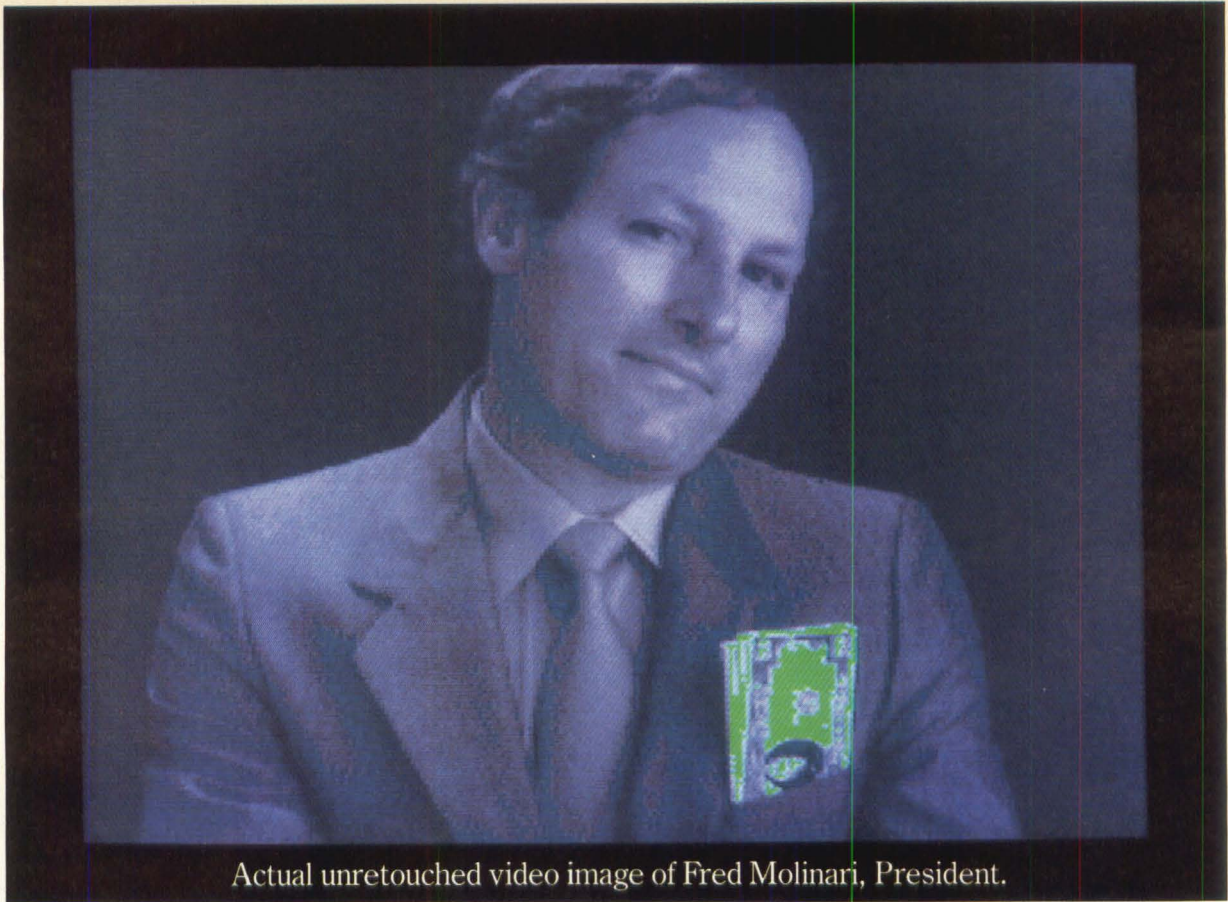
ASK ABOUT OUR NONVOLATILE CMOS RAM FOR THE MULTIBUS, Q-BUS, AND VME BUS TOO! CUSTOM BOARD AND CONTRACT MANUFACTURING INQUIRIES ARE ALSO WELCOME!

Diversified Technology
An Ergon Co.

P. O. Box 748, Ridgeland, MS 39158
Telex 585326

Circle 27

*MULTIBUS and ISBX are trademarks of Intel Corp./NSC800 is a trademark of National Semiconductor Corp.



Actual unretouched video image of Fred Molinari, President.

“It’s easy to spot the difference between our IBM PC™-based frame grabber and the others”

High performance and affordable cost, just \$1495 for a single plug-in board.



Laplacian Filter



False Color

Unlike other video I/O systems, the new DT2803 provides real-time image capture capabilities, digitizing a 6-bit video field every 1/30 second. An on-board, memory-mapped, dual-ported frame store memory (256 × 256 × 8) makes it ideal for the IBM PC’s 64K buffer size. And for real number crunching,

the DT2803’s external ports interface to high speed co-processors.

With our software package, VIDEOLAB™, the DT2803 is easy to use for image operations like averages, histograms, and convolutions.

So, if your application is manufacturing/automatic inspection, robotics, or medical research,

our new high performance video I/O board will really open your eyes – at an unbeatable price.



Call for our new 576 pg. catalog/handbook or see it in Gold Book 1985.

SPECIFICATIONS: DT2803	
A/D Input	RS-170 (CCIRR), 6-bits at 5MHz
Frame Grab	1/30 (1/25) second per field
LUT's	8, 64 × 8 input; 4, 256 × 12 output
D/A Output	64 colors × 64 intensities, R-G-B; 64 grey levels, monochrome
Frame Memory	256 × 256 × 8 (2-bits for graphic overlays)

Call (617) 481-3700

DATA TRANSLATION

World Headquarters: Data Translation, Inc., 100 Locke Dr., Marlboro, MA 01752 (617) 481-3700 Tlx 951 646.

European Headquarters: Data Translation, Ltd., 13 The Business Centre, Molly Millars Lane, Wokingham Berks, RG112QZ, England Tlx: 851849862 (#D)

In Canada: (416) 625-1907.

IBM PC is a registered trademark of IBM. VIDEOLAB is a registered trademark of Data Translation, Inc.

Circle 14 on Reader Inquiry Card

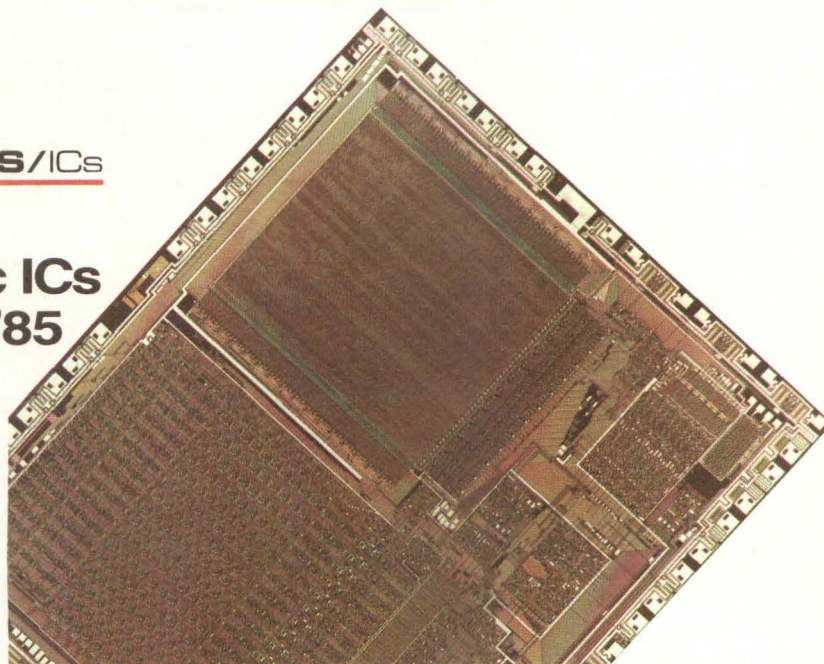
Language Specific ICs Debut At Wescon '85

Until recently, languages such as Forth, Prolog and Lisp have been available only in compiled or interpreted form on conventional processors or microprocessors. Now, AI software is beginning to get hardware support, and special purpose hardware is emerging to relieve the performance penalty usually associated with executing AI software on general-purpose machines.

At the upcoming Wescon '85 show in San Francisco, two sessions will focus on the problems of direct hardware execution of high-level language operations. The sessions will present both single-chip high-level language processors and large-scale building block designs. Douglas Fine and Chuck Hastings of Monolithic Memories (Santa Clara, CA) will describe a high-performance Forth engine using LSI building blocks. The implementation will be compared with an earlier one based on similar Forth hardware concepts performed at the University of Indiana before these LSI components were available.

The LSI component family includes a 16-bit ALU with four working registers and an integral long-word carry network, a 16×16 Cray multiplier with the entire 32-bit product simultaneously available at the outputs, a 16×16 shifter geared for cascadeability to long-words with one level of delay and an 18×2048 PROM which is used for microcode storage and address sequencing. Jim Flournoy, general manager of Proceadamus (Rosemead, CA) will describe how the capabilities of the machine are extended to LISP execution by an efficient implementation of LISP directly in Forth primitives.

In another session, Charles Moore and Bob Murphy from Novix (Cupertino, CA) will describe the Novix Forth Engine. This highly parallel machine



Prototype of Rockwell's Advanced Architecture microprocessor.

architecture directly executes Forth primitives in a single clock cycle. According to the company, the initial implementation of the device is based on a 4000-gate CMOS semicustom IC operating at an 8-MHz clock rate.

Under the premise that computer architecture should be directed by the programming language it is to support, David Best of Rockwell (Cedar Rapids, IO) will describe two VLSI implementations of a single-chip 16-bit CMOS Advanced Architecture Microprocessor (AAMP). AAMP is designed to support the execution of block-structured high-level languages such as Ada and PL-1 in embedded-computer applications. The processor architecture directly supports concurrent task execution and procedure reentrancy. Procedure parameter passage and context switching are performed automatically by the processor. The AAMP instruction set includes multiplication and division for 16- and 32-bit integer and fractional data, as well as 32- and 48-bit floating-point data. Best will conclude by describing a next generation architecture with full 32-bit data paths implemented in 1.25-micron CMOS technology.

A set of VME-based circuit boards rather than a single chip, the Xenologic (Berkeley, CA) Prolog Accelerator system is also geared to provide high-per-

formance execution of AI programs—this time in Prolog. Alvin Despain, president of Xenologic, will describe the co-processor system and the software it supports. One example he cites is in conjunction with the Sun 2/160 workstation. The Xenologic boards fit from two to five unused slots of the main processors cabinet and the UNIX 4.2 operating system provides the software interface. According to Mr. Despain, the processor achieves about 200,000 logical inferences per second on the Berkeley ProLog Benchmark Set.

Rounding out the technical sessions, Steven Krueger from Texas Instruments (Dallas, TX) will discuss the high-level language instruction set for a microprogrammed VLSI computer for LISP. An overview will be presented of the architecture of the machine as well as the computer system called the Compact LISP machine TI intends to build around it.

Advances in VLSI technology, as well as the increasing use of AI languages have for the first time provided competitive approaches to the practical implementation of high-level languages in dedicated designs. These special-purpose ICs will provide a closer fit to the software problem than is conventionally available using general-purpose machines.

—D. Wilson



Our Smart-Frame™ will put you in touch.

One of the easiest ways to interact with a computer is through a touch activated display. One that lets you merely point your finger at what you want your computer to do.

With touch, even the most complex application can become user friendly. And less susceptible to user error.

But the advantages of the highly reliable infrared touch input systems have been overshadowed by cost. Placing them out of the range of medium to low-cost turnkey systems manufacturers.

Which is the main reason Carroll Touch completely redesigned its line of touch input products.

We call it Smart-Frame™. Because it contains a powerful microprocessor built into the frame. And because it uses scanning infrared technology—a touch technology which is incredibly reliable, rugged, accurate, and fast. A technology Carroll Touch pioneered and refined.

As a result of the Smart-Frame design, Carroll Touch units contain 45 percent fewer components than before. Which means the cost to you is about 50 percent lower too.

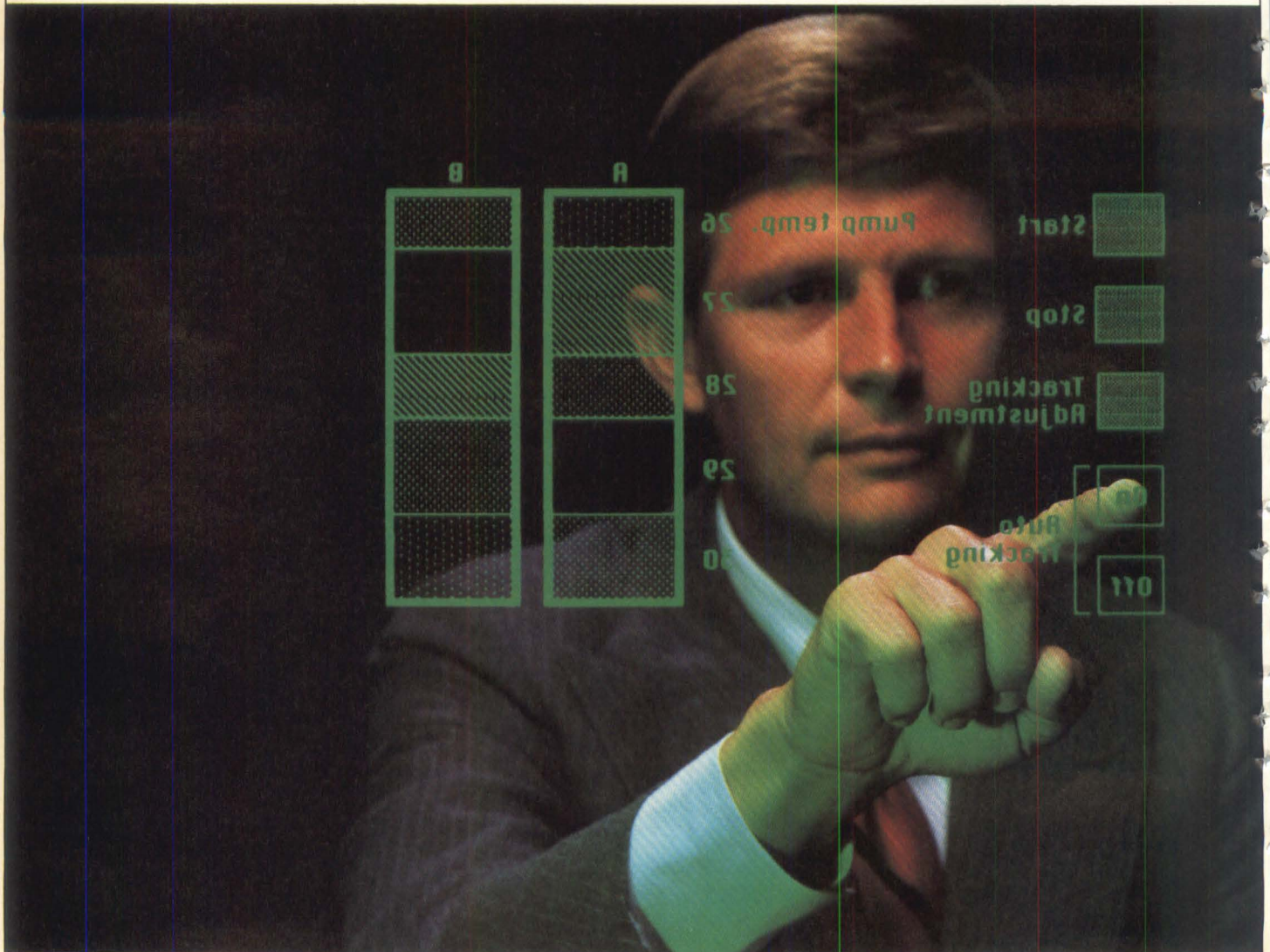
We think that's pretty smart. And Carroll Touch did it just so you could get in touch. Today.

Carroll Touch

a subsidiary of AMP Incorporated

In Touch with Technology

P.O. Box 1309
Round Rock, Texas 78680
512/244-3500, Telex 881906



Circle 5 on Reader Inquiry Card

TECHNOLOGY TRENDS

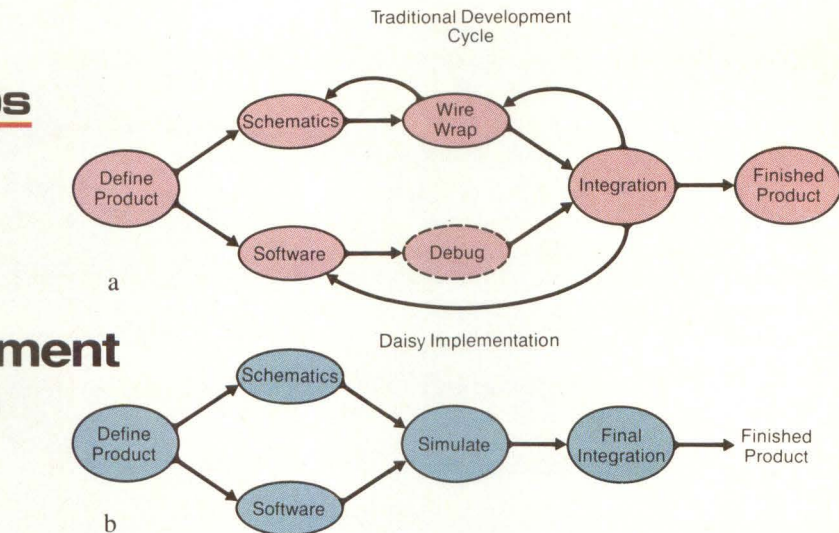
DESIGN TOOLS

Hardware And Software Development Linked To Shorten Product Cycle

Coupling microprocessor development systems with CAD systems promises to reduce the time needed for hardware/software integration. Both Tektronix/CAE Systems (Sunnyvale, CA) and Daisy Systems (Mountain View, CA) have announced the capability to download object code into the target system for extensive software simulation. At an early stage of the development cycle, designers can exercise a preliminary circuit as well as check out such hardware-dependent portions as interrupt routines and device drivers. With this, potential hardware/software integration problems can be readily identified, and the final hardware or software design changed before final prototypes are built.

To aid programmers in their efforts to develop object codes in high-level languages, microprocessor development system vendors have provided source-code symbolic debugging with the ability to single-step through source code statements as well as entire routines. Microlink from Tektronix/CAE Systems and Personal Logician-Microprocessor Design (PL-MD) from Daisy Systems act as debuggers for prototype hardware designs by using actual code rather than stimulus patterns for logic simulation.

The key to this close coupling of hardware and software development is the ability to translate object code into a format suitable for input into a logic simulator. For example, many compilers and assemblers from Daisy Systems for the 8086 family generate an output database called the Object Module Format (OMF). This database contains such



In traditional development cycles (A), designs undergo multiple wire-wrapped prototype versions and repetitive software debugging sessions using in-circuit emulators. Product cycles are shortened by downloading object code (B) for direct execution in a logic simulator.

information as variable names, data types and source code line numbers. This information is retained for symbolic debugging so that object module absolute addresses can reference the corresponding lines in the relocatable source code. A similar approach is used within Microlink and PL-MD as the object code is translated into the syntax used by a logic simulator. In addition, similar care is taken so that any software references to port addresses, control signals and address and data signals correctly correspond to the physical devices in the hardware design.

Hardware designers can execute object code modules under software simulation or through hardware modeling systems like TurboChip from Tektronix/CAE Systems or PMX (Physical Modeling Extension) from Daisy Systems. Both vendors recommend software simulation for running small routines and hardware modeling for executing larger modules on the actual chip. Execution speed is the primary consideration since it takes huge amounts of code to mimic the behavior of a microprocessor. Hardware extensions like PMX or TurboChip replace the software description of the microprocessor with the physical device although the remainder of the prototype system is still described in the device modeling language used by the simulator.

Both approaches allow hardware

designers to assess the behavior under actual conditions and make necessary changes before the design is sent for layout. Likewise, software designers have the opportunity to exercise hardware-dependent portions of their programs without waiting for a prototype to be built. Both companies claim the simulation runs will reduce the number of prototype systems that must be built.

To monitor program execution in real-time for final hardware/software integration, symbolic debuggers access the breakpoint and trace facilities of in-circuit emulators found with the Intel I²CICE or the Tektronix 8540 integration station. These facilities allow program execution to occur at full-speed in the prototype target system until the flagged instruction is reached. The emulator typically works in a background mode so that the target system is unaware of its operation.

From the disassembly of data and instruction accesses that occur on the bus, the internal CPU state can be inferred. With this information, software designers can garner execution times for individual routines, and monitor inter-module references and memory usage. If closer inspection of the CPU status is needed, intrusive measures (e.g., forcing a hardware interrupt) can be used to dump the internal control registers.

—Aseo

VICOM. The Power and Technology of our Workstation belongs in your PACS Network



VICOM, for the PACS architect who's building the best. When you learn about the VICOM family of modular image consoles, we're confident that you'll want VICOM as an integral part of your design. Please call us so we can tell you why.

Vicom Systems, Inc., 2520 Junction Avenue, San Jose, CA 95134.
Tel: (408) 946-5660 or (800) 538-3905. Telex 171603 VICOM SYS



For Immediate Interest Circle 36
For Information Only Circle 50

Color Image Framestore Uses Precision Converters For High-Quality Images

Systems integrators are faced with a number of problems when building or specifying systems for color image processing. At the low end, several frame grabbers exist which can be used to capture images up to $512 \times 512 \times 8$ -bits deep. Costing around \$3,000, these boards allow users to capture either NTSC or analog video data into RAM located on the boards for further processing. To implement color systems, three of these boards could be used with a host CPU, image processor boards and manufacturer-supplied imaging software. By opting for this route, systems integrators can implement systems for around \$20,000. However, other problems may arise. For example, if the image to be digitized is taken from a VCR, then a time base corrector may be needed to correct the artifacts placed on the video signal by the VCR operation. Timing of the video signals between the boards (for a color system) must be accurately controlled to reproduce the incoming images.

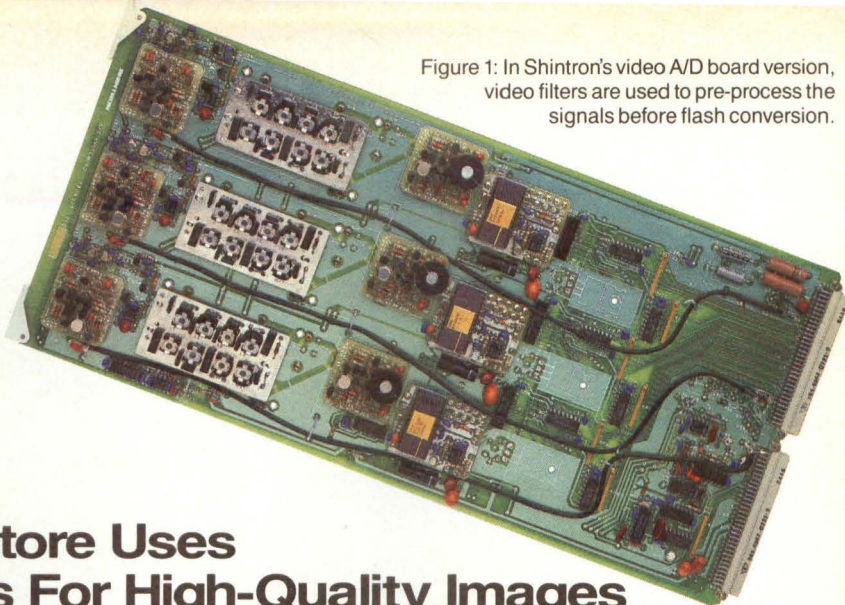
Having emerged from a computer-related background, many manufacturers have only partially addressed these problems in the design of their products. However, companies which have until now built products for the broadcast industry are entering the imaging market.

One company, Shintron (Cambridge, MA), has addressed the problems associated with color framestore design with a product called the Andromeda 3000. The 3000 uses a number of boards built by Shintron (Figure 2). Featuring full 13.5-MHz sampling on all three RGB channels, the subsequent picture information is written into a $768 \times 505 \times 8$ -bit memory per color plane. Using this 13.5-MHz clock, the system can also act

as a time base corrector. Currently, the Andromeda interfaces via Shintron's Orange Bus to its series of video switcher units. However, by the end of the year, a DMA interface will be offered for DEC's MicroVAX II. This will allow system integrators to use the MicroVAX as the control processor for the 3000.

One of the most novel features of the framestore's design is the attention which has been paid to both the A/D converter and the D/A converter boards. Accepting RS-170, RGB and YIQ signals, each of the three RGB channels has been built in a modular fashion on one board. Before each of the video channels are digitized, analog signal conditioning is applied to them. First, an operational amplifier increases the gain of the video signal for input into an MLY1350/15/2 video filter from Matthey (Stoke-on-Trent, UK). These are 75-Ohm phase-equalized filters used for pre- and antialiasing filtering. After filtering, the video signal is

Figure 1: In Shintron's video A/D board version, video filters are used to pre-process the signals before flash conversion.



sent to another discrete op amp to provide the low-output impedance needed by the flash converters.

In the Shintron design, three 14-MHz 1048 A/D converters from TRW (La Jolla, CA) are used. The outgoing TTL signals are then converted to ECL and transferred to the system memory. In operation, the read/write address controller regulates the DRAM memory array and multiplexes the data from the three video sources.

Digital boards in the system are manufactured on Unilayer boards supplied by Augat (Attleboro, MA). Schematics generated at Shintron were input into a PC running Dash from FutureNet (Canoga Park, CA). The resulting net list was transmitted to Augat for autorouting of the finished boards. According to company president, Shintaro Asano, this allows inexpensive, rapid upgrades.

—A. Wilson

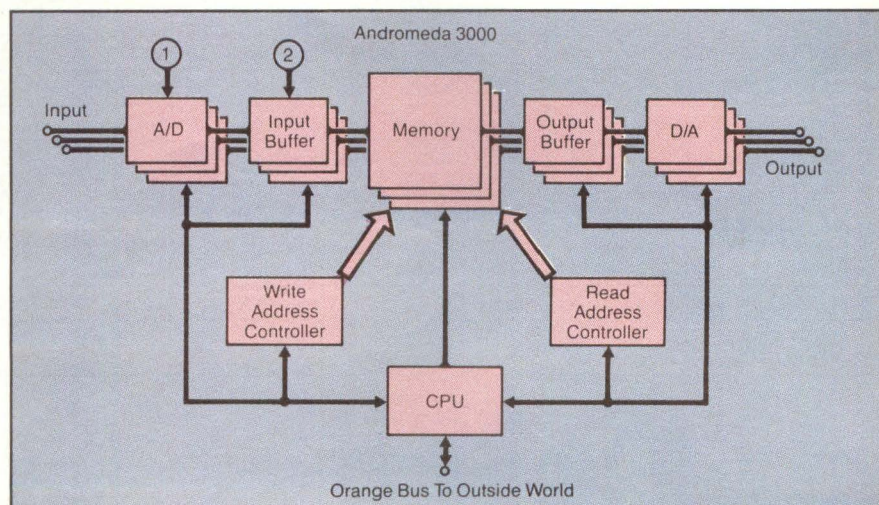
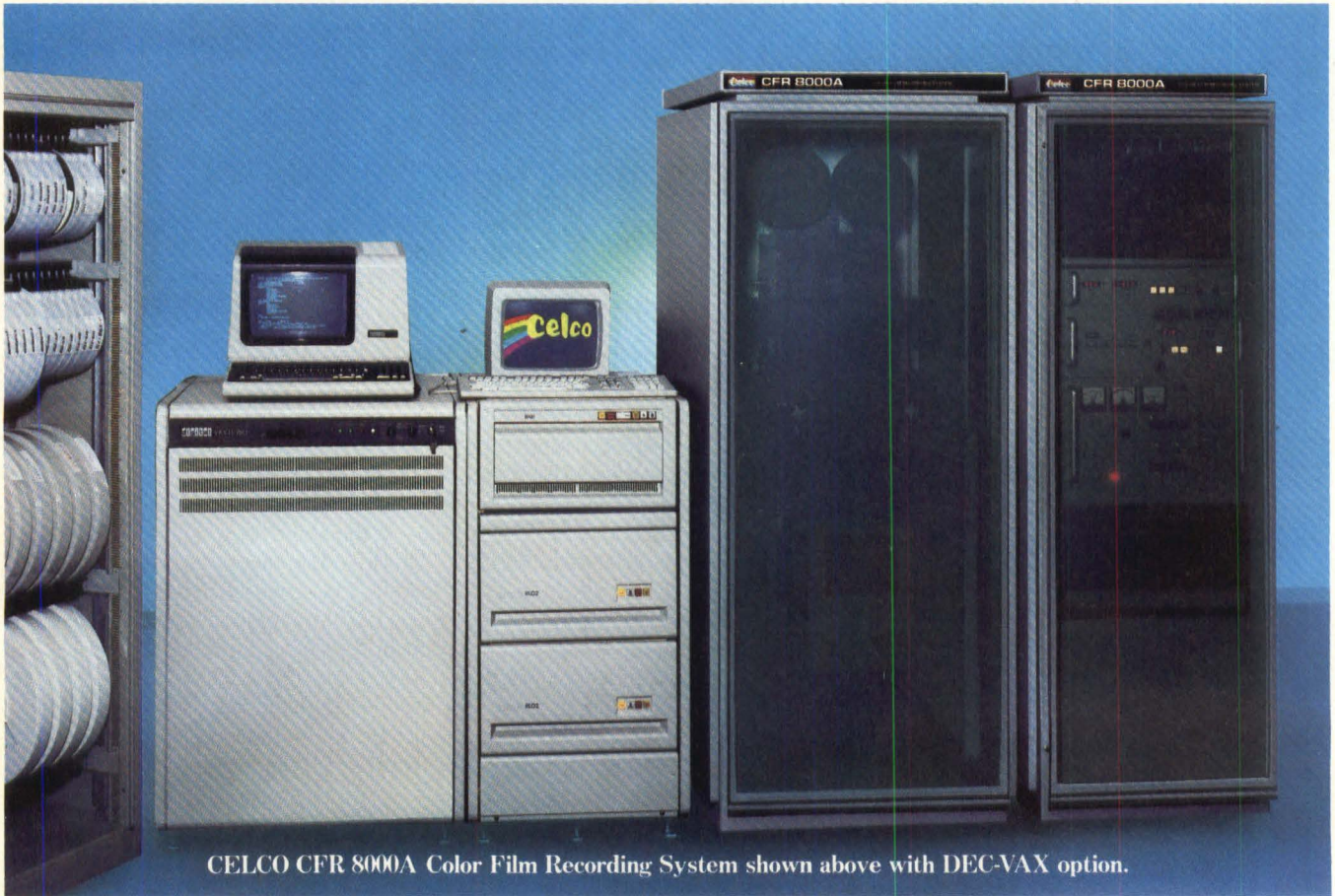


Figure 2: Shintron's Andromeda 3000 framestore is capable of digitizing three channels of video at a 13.5-MHz rate.

Ultra-High Speed and Resolution Color Film Recording Systems



CELCO CFR 8000A Color Film Recording System shown above with DEC-VAX option.

for LANDSAT, Animation and Presentation Business Graphics

SPECIFICATIONS	Celco 8000A	Celco 8000B	Celco 5000A	Celco 5000B
■ Resolution	7500 resolvable pixels		4200 resolvable pixels	
■ CRT Size	7" diameter CRT (0.0008" spot size)		5" diameter CRT (0.0008" spot size)	
■ Recording Speed	Less than 20 seconds for a complex 35mm graphics slide (run length encoded)			
■ Variable Pixel Rates	From 400ns/pixel to 6.2µs/pixel, in 400ns increments			
■ Addressability	4096 x 8192 (pixel x pixel), 8192 x 8192 (Run length encoded)			
■ Film Format Flexibility	Multi Format from 16mm to 8" x 10"	Fixed, selectable from 16mm to 8" x 10"	Multi Format from 16mm to 8" x 10"	Fixed, selectable from 16mm to 8" x 10"
■ Graphic Arts Workstations Interface Compatibility	Includes Autographix, Artronics, Executive Presentation Systems, MAGI, Management Graphics			
■ Mainframe Compatibility	DEC-LSI-11, PDP-11 and VAX; Perkin-Elmer 3200 series; IBM channel			
■ Device Independent Graphics Software Compatibility	ISSCO, UNIRAS			



For complete details circle reader service number or call CELCO today.
CONSTANTINE ENGINEERING LABORATORIES COMPANY
 70 Constantine Drive Mahwah, NJ 07430 TEL: 201-327-1123
 1150 E. Eighth Street Upland, CA 91786 TEL: 714-985-9868

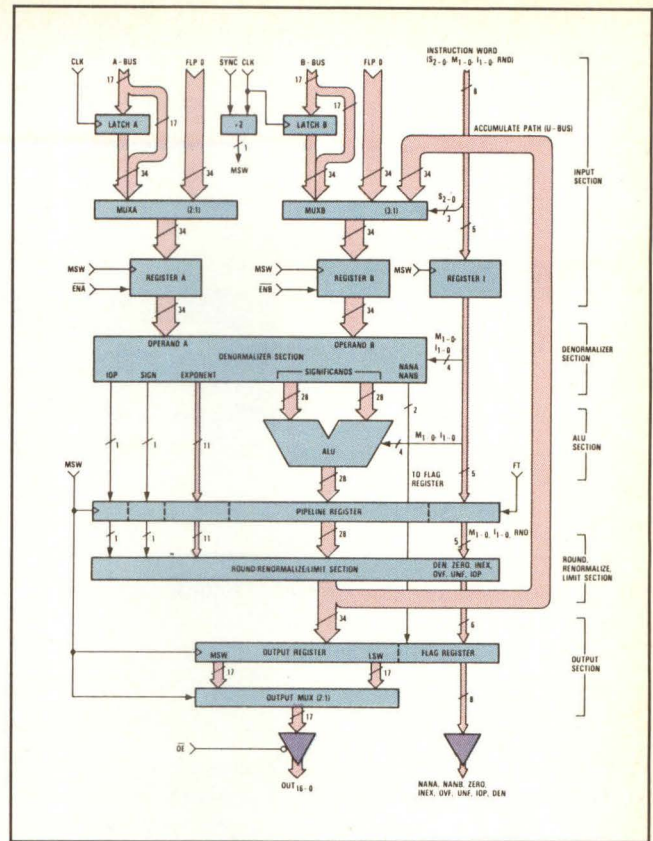
Imaging Functions Go On-Chip At GOMAC '85

One of the leading factors driving imaging functions into silicon is the money currently being spent by DARPA (Defense Advanced Research Projects Agency) and other military government agencies. Imaging functions, being so compute- and memory-intensive, should migrate to silicon in order to increase performance levels, especially in military applications.

At next month's Government Microcircuit Applications Conference (GOMAC) held in Orlando, FL, many companies will describe advanced processor architectures, optimized software-in-silicon functions and array processors for imaging applications. Although three of the conference sessions are classified, many of the abstracts already published give an important guide to the future of IC image processors.

In a session entitled Advanced System Concepts, LTV Aerospace (Dallas, TX) will describe a modular multiple processor architecture that supports both processing and memory elements. By designing the processor around a distributed crosspoint switching system, each switching element can connect one processor bus to one memory bus. Operating under control of the processor address bus, the switches form cycle-by-cycle connections based on each cycle's address. A different approach, adopted by the US Army Missile Command (Redstone Arsenal, AL) will describe the architecture of an image processor built around ten 68000 microprocessors. Because of the speed required, the theme of the paper will concentrate on techniques needed to allow real-time image processing. Ultimately, the architecture will be used as a preprocessor, postprocessor or both for analyzing FFT radar return signals.

Figure 1: TRW (La Jolla, CA) will announce the TMC3200 32/34-bit floating point unit at this year's GOMAC.



Many of the papers will describe how specific functions can be implemented as processors. Lockheed (Palo Alto, CA) will describe the Winograd Fourier Transform and a VLSI processor capable of performing a 120-point DFT in 1.6 msec. ESL (Sunnyvale, CA) will describe a systolic solution to the eigenvector subspace problem in signal processing and will announce a VLSI processor developed for such a purpose. And a paper from the Jet Propulsion Laboratory (Pasadena, CA) will describe techniques for computing the DFT using the residue Fermat number system and its VLSI implementation.

In a session on analog and digital signal processing, several companies will describe unique imaging products. The first paper, from Westinghouse (Baltimore, MD), will describe an ultra-high-speed monolithic operational amplifier fabricated in complementary bipolar technology. The op amp has a gain bandwidth product in excess of 600 MHz, a gain of 10, and slew rate of over 200 V/msec. Following this, MIT (Lexington, MA) will announce the development of a programmable SAW filter with a 1.5 msec impulse response and a programmable bandwidth of 50 MHz. The device is implemented using a piezoelectric SAW delay line coupled to a silicon IC. Sobel Edge Extraction, an important imaging function, will be described by TI (Dallas,

TX). The company's VLSI implementation of the function is capable of real-time operation on a 512- x 512-pixel image at 30 frames/sec. The device accepts 8-bit input data and produces a 9-bit edge magnitude output and a 3-bit direction output.

In the signal processing applications sessions, many types of specialized VLSI processors will be considered. Lockheed (Plainfield, NJ) will describe a floating point systolic array with 20 MFLOPS per processing element. The array is capable of DFTs, adaptive filtering, correlation and convolution. This will be followed by a discussion of a VLSI coordinate rotation computer from McDonnell Douglas (Huntington Beach, CA). The paper will detail the Cordic class of coordinate rotation algorithms and how a VLSI processor will be built to support them. In one of the final papers of the conference, TRW (La Jolla, CA) will announce a three-chip set designed for high-speed DSP. The TMC3200 is a 32/34-bit floating point processor (Figure 1), the TMC3201 is its companion multiplier, and the TMC3220 is a three-port register file.

While many of these products will never become available commercially, it is certain that they embody a trend in which many of the imaging functions currently performed in software will migrate to VLSI.

—A. Wilson

80386

The 80386 32-bit microprocessor is the latest microprocessor from Intel Corp. (Santa Clara, CA) designed for applications requiring high CPU performance, bus bandwidth and address space. The 80386 provides access to the 32-bit world: 32-bit registers, 32-bit data bus, 32-bit address bus and 8-, 16- and 32-bit data types.

The 386 addresses two other important issues. It gives system level support to systems designers by providing an integrated memory management capability which has virtual memory support, optional on-chip paging, four levels of protection and an integrated task switch. It also is object-code compatible with the entire family of 8086 microprocessors: 8086/88, 80186/188 and 80286. The flexibility provided by the 386 not only affords the installed base of 16-bit software immediate access to the latest processor technology, but also allows these object-code modules to run concurrently. For example, PC-DOS programs written for the 8088 can exist beside UNIX or XENIX code or can interact directly with 32-bit software written specifically for the 386.

Packaged in a 132-pin ceramic pin grid array, the 386 is fabricated in Intel's CHMOS III process. Using this technology, the 386 is designed to operate at 12 MHz and 16 MHz and dissipate between 1.5W and 3.0W. It has demultiplexed 32-bit data and address buses which allows a 32-bit access in only two clock cycles.

Processor Organization

Six functional units make up the 386 (**Figure 1**). These six units are arranged in a pipeline that enables them to operate in parallel on different instructions or on different parts of the same instruction. The bus unit performs bus transactions for the other units. When no other unit needs the bus, the prefetch unit reads the next word of the instruction stream from memory into the prefetch queue. Most code fetches are performed in parallel with execution using unneeded bus cycles. The decode unit cracks each opcode, converting it into a pointer to the microcode that implements the instructions. The execution unit executes the microinstructions and can add two 32-bit registers in two clock periods. Multiply and divide hardware performs 32-bit multiplications in 20 to 40 clocks, depending on the number of significant digits and 32-bit division in 40 clocks. Shift, rotate and the new bit field instructions are aided by a barrel shifter that can shift up to 64 bits in a single clock. The on-chip MMU consists of segment and page units.

The segment unit translates logical addresses to linear

addresses and checks each access for consistency with segment protection attributes. For the majority of instructions, the segment unit obtains the translation and protection data from the on-chip segment and descriptor registers. The page unit is enabled or disabled by operating system software. When paging is disabled, the linear addresses produced by the segment unit pass through the page unit unaltered. When paging is enabled, the page unit translates linear addresses into physical addresses and verifies that accesses are consistent with page attributes. The page unit includes a 32-entry Translation Look-



Raises The Flag For Compatibility

by Paul Wells, Technical Marketing Manager, Intel Corp.

aside Buffer (TLB) that caches the translation information for the most recently used pages. Using the TLB, the page unit can translate most page accesses (typically 97-99%) without consulting the memory-based page tables. When necessary, the page unit initiates the bus cycles required to return an older TLB entry to its page table and to load the vacated TLB slot with the page table entry referenced by the current instruction.

All 386 instructions operate on 0, 1, 2 or 3 operands; an

operand resides in a register, in the instruction or in memory. Most 0-operand instructions (e.g., CLI, STI) take only 1 byte. Generally, 1-operand instructions are 2 bytes long. The average instruction length for the processor is 3.2 bytes with an average instruction time of 4.4 clock periods. The use of 2 operands permits the following types of common instructions: Register to Register, Memory to Register, Immediate to Register, Memory to Memory, Register to Memory, and Immediate to Memory.

The operands can be either 8-, 16- or 32-bits long. As a rule, when the processor is executing 32-bit code, operands are 8 or 32 bits. When executing 16-bit code, operands are 8 or 16 bits. Instruction prefixes can be added to all instructions which over-

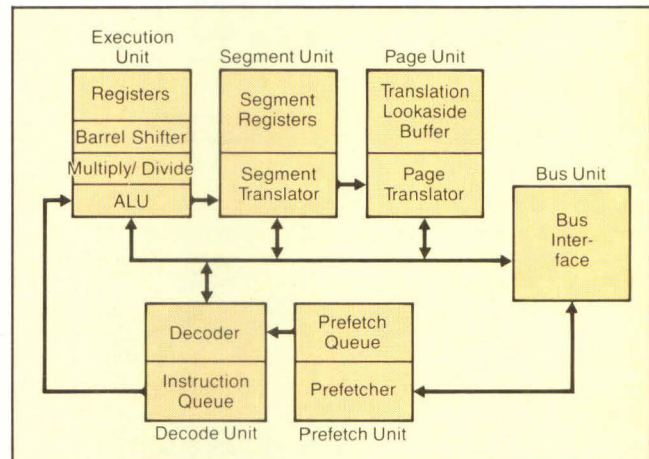


Figure 1: Six functional units make up the 32-bit 386. Arranged in a pipeline, they can operate in parallel on different instructions or on different parts of the same instruction.

ride the default length of the operands. Thus, it is possible to further optimize code with the selective use of 32-bit operands with 16-bit code or 16-bit operands with 32-bit code.

80386 Register Set

The 386 microprocessor has a total of 34 registers divided into the following categories: General-Purpose Registers, Segment Registers, Status and Control Registers, Systems Address Registers, Debug Registers and Test Registers (Figure 2). The General-Purpose Registers are a superset of the 8086 and 80286 registers. These eight registers (EAX, EBX, ECX, EDX, EBP, EDI, ESI and ESP) hold 32-bit quantities. The low-order word

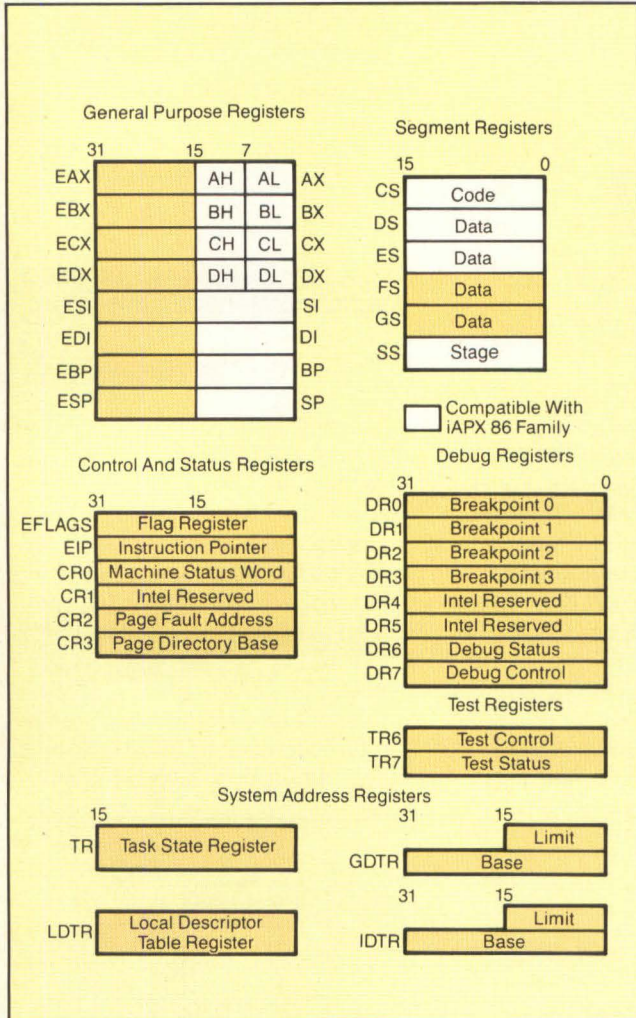


Figure 2: The 386 has a total of 34 registers divided into six categories: general purpose, control and status, segment, debug, test and system address.

of each register is used when performing 16-bit operations. Four of these low-order registers (AX, BX, CX and DX) are divided into pairs of 8-bit quantities to support 8-bit operations.

Six 16-bit segment registers (or selectors) select separate regions of memory. Three of the segment selectors (CS, DS and

SS) are used to address the current code, data and stack segments. The remaining registers (ES, FS and GS) are used to address user-defined data regions. The size of the segments addressed by the 386 range from 1 byte to 4 Gbytes.

The Control and Status Register block consists of the Flag Register (EFLAGS), the Instruction Pointer (EIP), and four Control Registers (CR0-CR3). The flag register, which stores information about the processor, is extended to 32 bits, with a few new bits defined in the upper two bytes (Figure 3). The lower 2 bytes are the same as the 286 flag register to ensure compatibility.

Flag bits 1, 3, 5, 15 and 18 through 31 are undefined, but when used with the SAHF or PUSHF instructions or when interrupt processing occurs, zeroes are stored in these bits except for bit 1. Bits 0, 2, 4, 6, 7 and 11 indicate the state of a computation such as parity, sign and overflow. Bits 8, 9 and 17 identify and control the operation of the processor within a given mode. Bit 8 (Trap Flag) enables the generation of single-step interrupts. Bit 9 (Interrupt Flag) is used to enable or disable certain classes of external interrupts. Bit 17 (virtual Mode Flag) is a new bit defined to indicate that the processor is operating in the virtual 86 environment. Bit 16, the Restart Flag (RF), is another new bit defined in the 386. The RF flag is reset at the successful completion of every instruction, except IRET, POPF and instructions which perform task switches, and is set in the flag register image as part of processing a fault.

The 386 defines a set of four 32-bit control registers, (CR0-CR3), to hold information on the global machine state. These registers, along with the System Address Registers described later, hold the machine state that affects all tasks in the system. CR0, the machine status and control register, is used to provide system information to the processor. The machine status word of the 286 maps directly into the low order half-word of CR0 and two new bits have been defined, bit 4 and bit 31. Bits 5 through 30 are reserved for future use by Intel. The new CR0 bits, except for bit 4, are upwards compatible from the 286 since they are in register bits not defined on the 286.

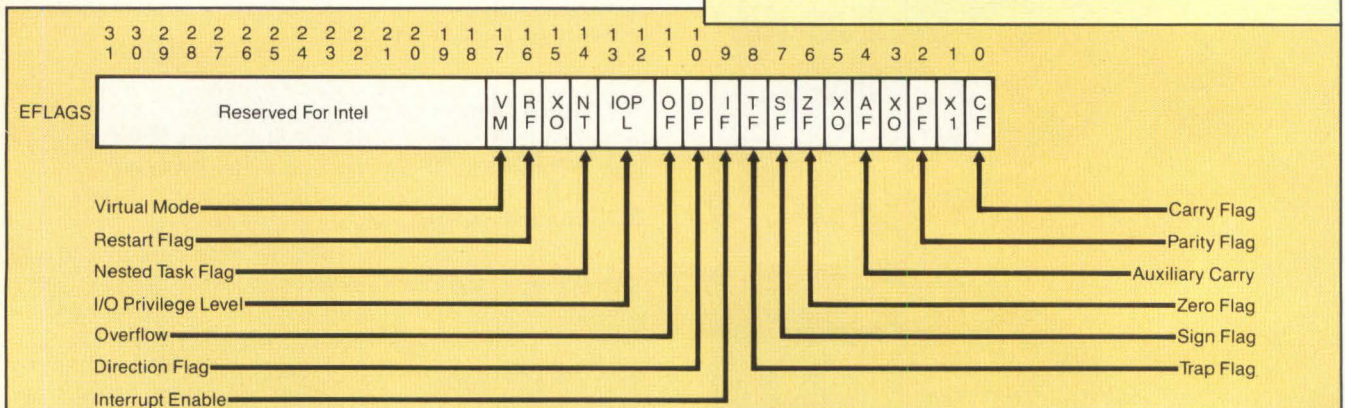


Figure 3: The control and status register block consist of the flag register, the instruction pointer and four control registers.

ONLY EIKONIX[®]

DOES SO MUCH IN HIGH PERFORMANCE DIGITAL IMAGING CAMERAS.

EIKONIX[®] high-performance digital imaging cameras offer unique capabilities that clearly distinguish them from all others.

CCD or Photodiode Technology

Only EIKONIX offers a choice of high-resolution cameras employing either linear CCD (charge-coupled device) or photodiode technology. In fact, EIKONIX offers the highest-resolution CCD camera available anywhere, with up to 20 million pixels per image (4096 x 5200).

You can choose the economy and low-light capabilities of a CCD camera, or the greater dynamic range of a photodiode camera, *without sacrificing high resolution.*

Color or Monochrome

Only EIKONIX has a family of high-resolution cameras available for either monochrome (256 gray-scale levels) or color (a palette of 16 million colors) applications.

More User Control

Only EIKONIX cameras use a precision stepping-motor/lead-screw/ball-slide stage mechanism, which provides precise positioning of the array and eliminates one-dimensional



smearing. In addition, this mechanism allows asynchronous operation, so the user can control both scan speed and data collection rate. This eliminates the need for a separate "frame grabber" or dedicated processor, and frees the host computer for multi-tasking.

Buy Just What You Need

Only EIKONIX' broad product line lets OEMs and end users match needs precisely. Configurations range from bare-bones digital camera heads through complete image acquisition subsystems, including cameras, light sources, control electronics, imaging

software, and interfaces for many widely used computers (including most DEC and Multibus-based systems).

More Applications

Only EIKONIX offers the performance and flexibility to handle the broadest range of the most demanding applications, including mapping, engineering drawing digitizing, graphic arts, CAD/CAM input, office automation, X-ray storage and analysis, textile pattern design, geological imaging, communications, animation and microscopy.

EIKONIX Know-How

Only EIKONIX digital imaging products are backed by our 17 years of experience in matching advanced electro-optical technology to a widening world of applications.

To find out what we can do to support your digital imaging applications, contact EIKONIX, 23 Crosby Drive, Bedford, MA 01730, (617) 275-5070.

EIKONIX[®]
A KODAK COMPANY

Circle 56 on Reader Inquiry Card

Bit 4 (ET) holds information on the processor extension type. A zero in this field indicates that a 287 floating point coprocessor is in the system. If this field contains a 1, a 387 floating point coprocessor is being used. Thus, designers are given a choice between the 287 16-bit protocol and the 387 32-bit protocol.

Bit 31, the Paging Enable (PE) bit, is used to indicate whether the on-board paging unit is enabled. The PG and PE (protection enabled) bits are paired to provide four combinations which select the operating environment for the 386. The operating modes defined by these bits are described in **Table 1**.

CR1 is currently undefined and is reserved for future use by Intel. CR2, the page fault linear address register, holds the full linear address which caused the last page fault. CR3 contains the starting address of the page directory.

The 80386 contains four system address registers which hold information about the protection and address translation tables needed by an operating system. These registers, Task Register (TR), Global Descriptor Table Register (GDTR), Local Descriptor Table Register (LDTR) and Interrupt Descriptor Table Register (IDTR), define the task environment, address space and interrupt vector space for a task currently under execution. The semantics and manipulation of these registers is upwardly compatible with the 286.

The 80386 also provides on-chip hardware support for debugging. Eight registers, DR0-DR7, give system program-

PG	PE	MODE
0	0	'Real Mode.' 8086 operation.
0	1	'Protected Mode.' Exact 286 semantics plus 32-bit extensions. (A sub-environment is also defined to support a virtual 8086 within the context of the extended 286/386 protection model.
1	0	UNDEFINED. If attempted, the condition will trigger a general protection fault.
1	1	'Paged Protected' environment. Enables all of the facilities of the Protected mode with paging enabled.

Table 1: Two bits are paired to provide four combinations which select the operating environments for the 386.

mers the ability to define up to four breakpoints. These can specify any combination of instruction execution and data reads or writes. Debug Registers DR0-DR3 hold four breakpoint addresses. DR6 is the Debug Status Register. The low-order bits are indicator bits set by the hardware at entry to the debug exception handler when an enabled debug exception is detected. The debug handler must clear these bits before exiting. DR7 is the Debug Control Register. The high-order half-word is divided into four fields which specify the length of the breakpoint field (1, 2 or 4 bytes) and the type of access that should cause the breakpoint. The bit-fields in the low-order half-word are used to enable the breakpoints and selected debug conditions.

Test Registers TR6 and TR7 are available for use to control the testing of the RAM/CAM (content addressable memory) in the Translation Lookaside Buffer portion of the paging unit. TR6 is the test command register, and TR7 is the data register which contains the data for the Translation Lookaside Buffer

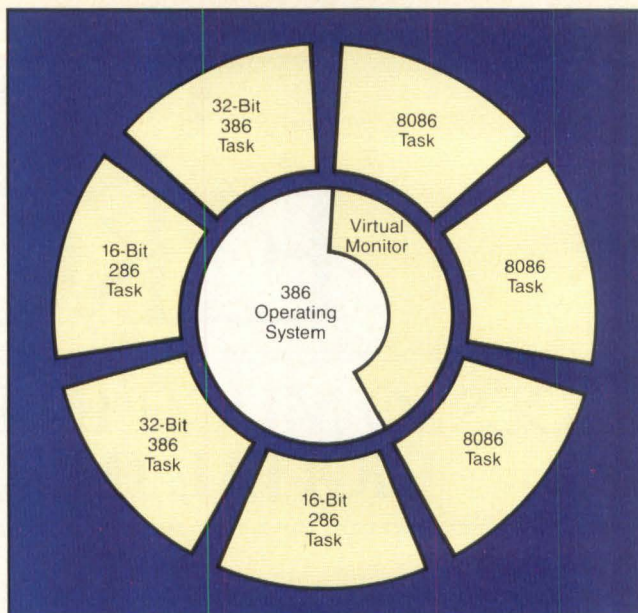


Figure 4: The 286 object code can coexist as tasks alongside 32-bit tasks.

test.

The 386 microprocessor can operate under one of two modes, real or protected, which are controlled by the PE bit in control register 0. The real mode causes the 386 to behave exactly like a very fast 8086. Although the real mode is intended primarily for use in booting up the system for operation in the protected mode, it is one way to execute 8086/88 code. The real mode is bit compatible with the 8086/88, and the addressing mechanism, interrupt structure and segment size are exactly the same. There is a superset of the 386 functionality available to code running in the real mode, such as new instructions to manipulate bit fields and access to 32-bit offsets and operands; however, these would not be available for use unless the code were recompiled. Further, care must be taken so that the real mode capabilities are not exceeded. For example, 32-bit offsets in the real mode may not violate the 64K offset maximum.

The full capabilities of the 386 are available when the processor is operating in the protected mode. The linear address and segment offset size are increased to 4 Gbytes and programs have a virtual memory space of 64 terabytes. In addition to the 32-bit capabilities of the processor, the protected mode provides the user with hardware-assisted support for a multilayered protection model, hardware-assisted multitasking support and the most sophisticated memory management capability available.

Supporting 8086 And 286 Software

The 386 protected environment is able to support a variety of software combinations. As shown in **Figure 4**, 286 object code can coexist as tasks alongside 32-bit tasks. The processor also provides a virtual 86 environment which allows the running of 8086 programs and operating systems encapsulated within a 386 task. Because 386 tasks can be protected and paged in virtual memory, paging is available to 286 programs; protection

Segment Base 15..0		Segment Limit 15..0		
Base 31..24	Size Control	Limit 19..16	Access Control	Base 23..16

Figure 5: Generalized segment descriptor format.

The lean, mean plotting machine from Houston Instrument

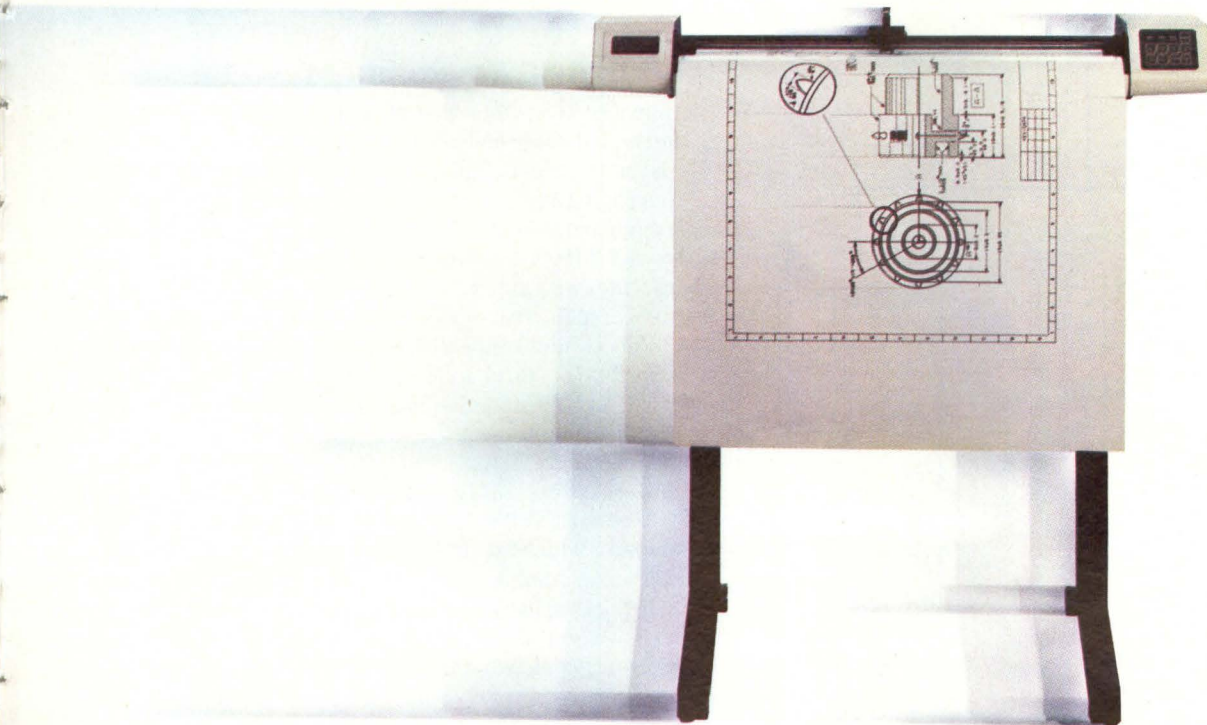
Houston Instrument's brand new servo driven DMP-51 is the fastest drum plotter we've designed to date. This superb plotter offers a pen speed of up to 22 inches/second; programmable accelerations, and a pen-on-paper resolution of 1/1000 of an inch! That means you'll turn out quality 17" x 22" and 22" x 34" drawings a lot faster, increasing your firm's productivity and profitability.

Now, for more good news. The DMP-51, priced at \$4,495*, is as fast as other plotters costing three times more. At that price, you can afford to put a DMP-51 at individual drafting work stations.

This is the professional plotter that meets the needs—and the budgets—of all companies, large or small.

The DMP-51 is intelligent, too. The DMP-51 can execute complex graphics operations from the simplest commands. A mechanical/architectural version, the DMP-52, with its 18" x 24" and 24" x 36" paper size, is available for the same price from Houston Instrument.

So, watch our new plotter in action . . . it won't take much time to realize it's the best buy for your money. For the name, address and phone number of your nearest dealer or distributor, write Houston Instrument, 8500 Cameron Rd., Austin, Texas, 78753. You can also call 1-800-531-5205 or 1-512-835-0900 (Texas residents). In Europe, contact Houston Instrument Belgium NV, Rochesterlaan 6, 8240 Gistel, Belgium. Tel: 059-27-74-45. Tlx: 846-81399.



*Suggested U.S. retail price

4P014

Circle 21

**houston
instrument**

plus paging is available to 8086 programs. All programs operating as virtual 86 tasks require a virtual machine monitor to be present. A virtual machine monitor is a program which maps resources from the virtual machine (8086) to the host operating system. The 386 provides hardware hooks within the chip which simplifies the implementation of a virtual machine monitor to emulate the virtual environment.

The 386 implements a descriptor-based segmented memory management system. Each task in the system may have up to 16,000 segments of code, data and stack which define the task's virtual address space. Each segment has a data structure, which is a descriptor that describes the properties of the segment (Figure 5). All of the descriptors which define a task are collected in one of two tables: a Global Descriptor Table (GDT) which contains descriptors common to the system and a Local Descriptor Table (LDT) which contains descriptors private to the individual task. A particular table and descriptor within that table is selected by a segment selector (Figure 6). This mechanism is common to both the 286 and 386 processors.

The descriptor types available within the 386 include all of the 286 descriptor types. The basic difference between 286 descriptors and 386 descriptors, aside from specific type numbers assigned to each, is their treatment of high-order 16 bits. The 286 descriptors treat the high-order 16 bits of the descriptor as reserved and contain zeros in these 2 bytes, whereas the 386 descriptors use these high-order 16 bits to define upper

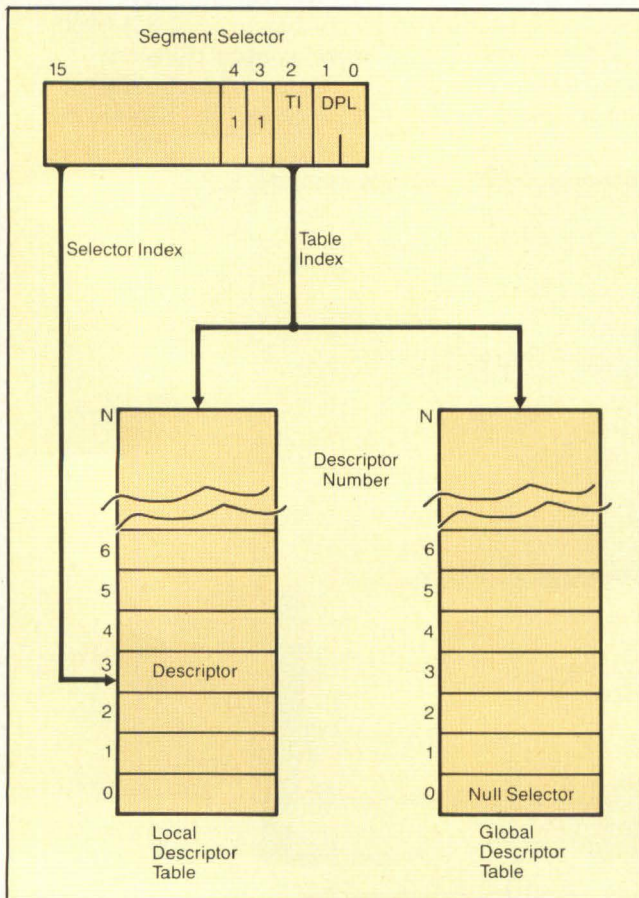


Figure 6: In 286/386 descriptor organization, a particular table and descriptor within that table is selected by a segment selector.

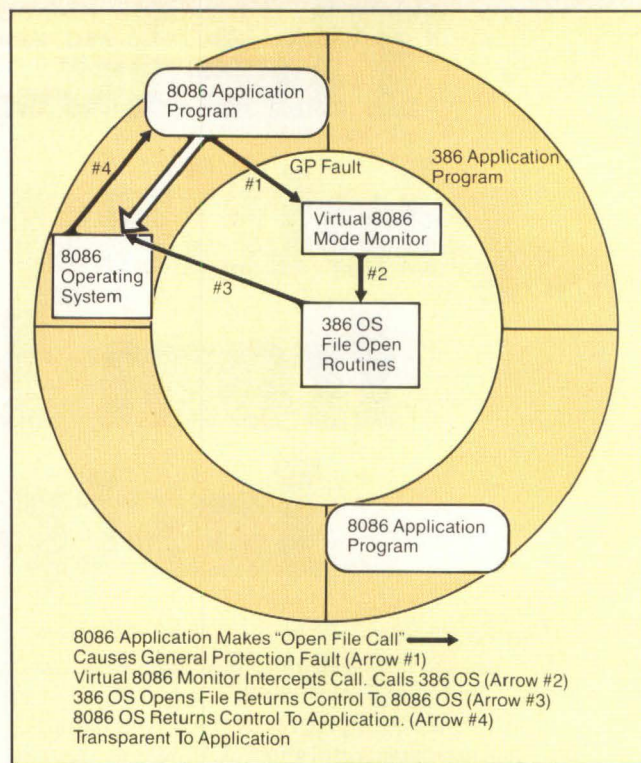


Figure 7: This example is one possible approach to handling system calls from a virtual 86 program.

order Base and Limit values and supply segment size information. Thus, in order for a 286 system to run on the 386, the reserved fields in the 286 descriptors must be zero and none of the unassigned type codes in the access control byte can be used (although the codes may now define 386 descriptor types). Following these simple rules will allow the 386 to determine on the fly whether the segment being accessed is 16-bit 286 code or 386 code.

Virtual 86 Environment

The virtual 86 environment of operation is a subset of the 386 protected mode and permits 8086 code to be executed within the protected and paged environment provided by the 386. Without paging enabled, one 8086 program can be supported; with paging, any number of virtual 8086 programs can run in their own 1 Mbyte address space. The virtual 86 environment executes with the PE bit of the machine status word (MSW) set to one; in the real mode, this bit is zero. The real mode of the 386 is similar to the virtual mode in that both execute 8086 object code, form addresses and treat segment registers the same. In both modes, segment relocation is performed by shifting the 16-bit value in the segment register 4 bits to the left and adding the 16-bit (or 32-bit) effective address to obtain a 32-bit linear address.

The virtual 86 environment relies on a virtual machine monitor which executes in the 386 protected environment and is used to emulate a few privileged and sensitive instructions which cause protection traps. The 8086 code running in a virtual machine state executes at protection level 3. An attempt to execute privileged instructions, which can only run at level 0, or sensitive instructions, which are normally I/O related instructions that must execute at a predefined I/O privilege level (IOPL), will cause a trap into the virtual machine monitor which must reside at privilege level 0.

Aside from the protection and paging capabilities available

to the virtual 86 environment, the primary difference between the real and virtual environment is the way in which interrupts are handled. In real mode, interrupts trap through a vector of procedure pointers in the 8086 interrupt vector table. The base address of this table is held in one of the System Address Registers, the Interrupt Descriptor Table Register (IDTR).

Each entry is 4 bytes long and gives the starting address of the interrupt handling procedure, just like the 8086. In the virtual 86 environment, interrupts are vectored through the protected Interrupt Descriptor Table (IDT) which contains descriptors pointing to the interrupt service routines. Vectoring through the IDT causes the processor to leave the virtual environment and enter the protected environment of the 386. The 386 trap handlers can either completely process the interrupt themselves and simply return to the virtual 86 environment with an IRET (interrupt return instruction) or reflect the interrupt to the virtual 86 program by manipulating the virtual 86 state saved at the trap.

The example in **Figure 7** illustrates one possible approach to handling system calls from a virtual 86 program. Many 8086 programs perform operating system calls by PUSHing parameters on the stack and executing an interrupt instruction (INT n). The application thinks it is making an Open File call in this manner. If the I/O Privilege Level (IOPL) is set to zero, that is, the system is preventing I/O operations by the 8086 code, the INT n instruction is intercepted by the virtual monitor. The 386 operating system could open the requested file and then return control to the virtual 86 environment.

The virtual 86 environment is entered by executing an IRET instruction from privilege level zero or by a task switch (from any privilege level) with the Flag Register image containing a one in the VM bit position. The POPF (pop flags) instruction does not affect the VM bit and so cannot be used to enter virtual 86 environment. The PUSHF (push flags) instruction always pushes a zero in the VM bit so that a program cannot tell if it is executing in the real or the virtual 86 environment.

The transition out of the virtual 86 environment into the 386 protected mode occurs only on receipt of an interrupt or exception. All interrupts or exceptions from the virtual 86 environment pass through the protected IDT and, as part of the process, the VM bit is cleared. All transitions from the virtual 86 environment must go to privilege level 0. Any other condition will raise a general protection fault. Transitions to and from the virtual 86 environment via task switches must have a 386 task as the source or destination since 286 tasks do not have access to the high-order 16 bits of the EFLAGS register where the VM bit resides.

Because of the cost of software development, the need to preserve software investments has become an important element in the choice of processor architectures. The 80386 microprocessor maintains a level of continuity to provide designers with a wide range of hosting options. The 386 allows the installed software base immediate access to the performance and system level capabilities of the 32-bit generation of microprocessors. **DD**

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful 601
 Useful 602
 Somewhat Useful 603

DEC Users

The waiting for disk response is over

- Finally there is a cost-effective way to speed up PDP-11 and VAX computers.
- Waiting time for disk access can be dramatically reduced.
- Caching and disk emulation techniques combined.

With the MegaDSC-11 high performance storage management system.



If your system is I/O bound because of disk intensive applications, the MegaDSC-11 can significantly increase your system's performance.

How?

The MegaDSC-11 intelligent disk caching system anticipates the data most likely to be needed by the CPU and holds that data in high-speed cache memory. Many read responses come directly from the cache memory, thereby eliminating mechanical motion as a factor in disk access time. Extra performance is gained by off-loading storage management functions from the CPU.

Features:

- 32MBytes of cache
- Solid-state disk emulation
- Transparent to existing system software
- Provides all UDA 50 functions
- Supports MSCP protocol
- Multiporting
- Automatic error detection and recovery
- User selectable caching algorithms
- Volume shadowing.



Imperial Technology, Inc.

831 S. Douglas Street • El Segundo, CA 90245
 Telephone: (213) 536-0018 • Telex: 664469

YOUR VAX IS MULTI-USER. YOUR ARRAY PROCESSOR SHOULD BE TOO.



Up to four VAX users can perform computationally-intensive scientific and engineering tasks simultaneously on Mini-MAP Plus4, CSPI's 32-bit floating point array processor. When you team your VAX with Mini-MAP Plus4, multi-user/multi-tasking applications are shifted off the VAX, freeing it for other tasks. No degradation of performance. No need to unload programs and data between jobs. And no "roll-in/roll out" overhead. These are three unique contributions that Mini-MAP Plus4 makes to array processing technology. And three reasons why Mini-MAP Plus4 is especially effective in systems where continuous AP production processing and AP program debugging must be simultaneously carried out.

High Throughput: To the VAX team, Mini-MAP Plus4 brings 28 MFLOPS and 13 MIPS of computational speed. That power, plus Mini-MAP Plus4's 64 MBytes of physical data memory, can speed your VAX-11/780 by a factor of 5 to 20 times.

FORTRAN Convenience: Mini-MAP Plus4's compiler lets you program directly in FORTRAN. And CSPI's Scientific Subroutine Library provides 300 highly optimized routines.

Compact and Energy-efficient: Mini-MAP Plus4 enters your work space easily. It requires a mere 10.5" (26.7 cm) in your DEC rack and is self-cooling. And if you need less capability now but want to upgrade later, CSPI offers a modular system that lets you build in increments.

So when user pressure is heavy and your computational tasks push against tight deadlines, you'll be glad to have Mini-MAP Plus4 on your VAX team. To find out how Mini-MAP Plus4 can work for you, call toll free 1 800 325-3110.



Circle 20 on Reader Inquiry Card

CSPI
THE ARRAY PROCESSORS

40 Linnell Circle, Billerica, Massachusetts 01821
617/272-6020 • TWX: 710-347-0176

DEC and VAX are trademarks of Digital Equipment Corporation.
Mini-MAP Plus4 is a trademark of CSPI.

High-Performance ICs Fuel Up With GaAs

by Dave Wilson, Executive Editor

Offering four to six times the speed of silicon-based ECL parts and as much as ten times the speed of silicon CMOS parts, gallium arsenide (GaAs) devices are carving an ever-widening market niche with each process improvement. However, unlike silicon's domination of germanium, GaAs is not expected to become a universal replacement for silicon. Often referred to as "gigahertz logic," GaAs ICs will become the preferred technology in the over 1 GHz range, with gate delays down to 30 ps and power consumption as low as 150 mW. Many ECL designs use GaAs circuits for cache memory and I/O. Other applications for which GaAs circuits are suited are direct broadcast communications systems, telecommunications, supercomputers, instrumentation and test.

A number of different transistor types have been built with gallium arsenide. The most commonly used and commercially successful is the Metal Semiconductor Field Effect Transistor (MESFET). The Depletion-mode MESFET (D-MESFET), which is normally on, has been in use for 10 years and is consequently the most widely used device. The Enhancement-mode MESFET (E-MESFET) is a normally off device that requires only one power supply and uses less power than D-MESFETs. D-MESFETs have larger current-drive capabilities and larger signal-voltage swings, which have made them popular for use in systems and easier to process.

Another GaAs device type that has shown potential for commercialization is the High Electron Mobility Transistor (HEMT). A variety of nomenclatures are used to describe this device; each is a description of a different aspect of the device. Fujitsu calls the device a HEMT. The University of Illinois and Rockwell International adopted the term MODFET for modulation-doped FET. Thomson-CSF uses TEGFET or two-

dimension electron gas FET. Bell Labs calls the device SDHT or selectively doped heterojunction transistor. These devices are superlattice heterojunctions, that is, layer by layer of GaAlAs are deposited on an undoped GaAs channel.

Electron mobility is higher in HEMTs than MESFETs because the charge carriers are not scattered by dopant ions in the channel. By raising gate voltages just above threshold, HEMTs quickly reach their full transconductance, giving them one of the fastest turn-on times. HEMTs do perform better than E-MESFETs and at about the same power dissipation, especially at lower temperatures around 77 Kelvin.

There are other GaAs device developments that show promise for commercial production. Heterojunction bipolar transistors (HBTs or HBJTs) have shown some feasibility. Their performance is higher than HEMTs with switching delays around 10 ps, even at high output current levels. Other devices are mixed E- and D-MESFETs that can provide fast low-power circuits.

Figure 1 shows a comparison of these transistor technologies based on conservative design. The diagonal lines represent a constant power-delay product. Only the Josephson junction offers comparable propagation delay and lower power dissipation than the nitrogen-cooled 77 Kelvin MODFET.

There are three main types of GaAs logic commonly used. The type first produced and most popular is Buffered FET Logic (BFL). It has relatively simple processing and is the most easily produced. A variation of BFL, called low-power BFL,

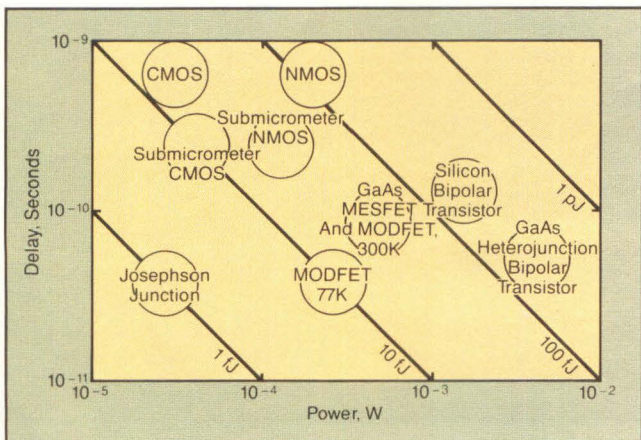
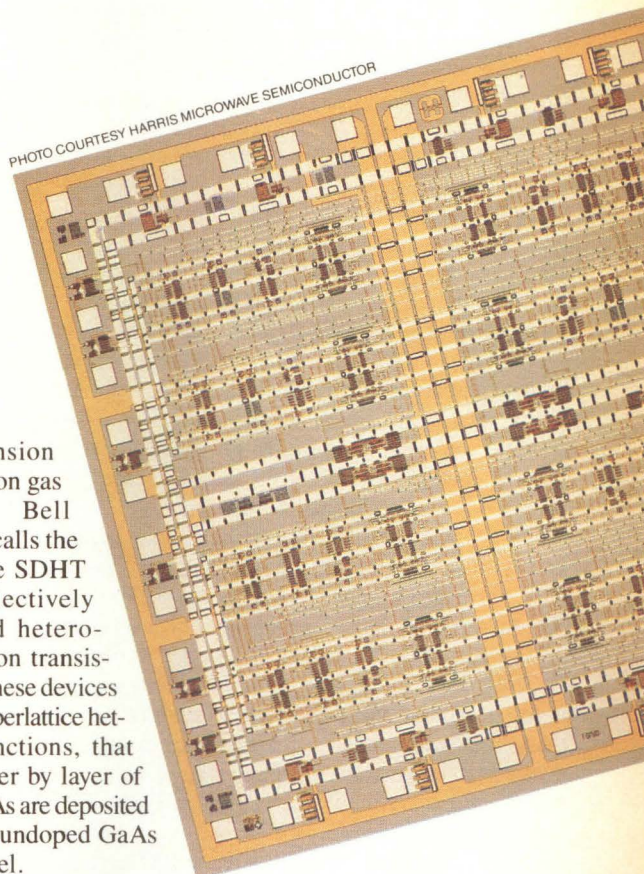


Figure 1: Power-delay continuums of transistor technologies indicated by circles based on conservative design. (Courtesy IEEE Spectrum)



has a lower power consumption and faster speed than its predecessor. The second type, Schottky Diode FET Logic design, is similar to BFL with operating speeds nearly as high and with lower power dissipation. However, the diodes are relatively small, which complicates wafer processing. The third type of GaAs logic, Direct Coupled FET Logic (DCFL), uses E-MESFETs for even lower power supply. It has the simplest structure and is popular for VLSI design efforts.

Table 1 compares not only these three types of logic but others currently under development. It is divided into two processing technologies, Depletion (D) and Enhancement-Depletion (E-D). The D technology is more producible, but as the technology matures, E-D will be the choice because of its potential for higher performance and larger scale integration.

Depletion-mode MESFET technology is relatively mature and is being manufactured in growing volumes in the US, Japan and Europe. This technology is well suited to monolithic microwave integrated circuits and MSI applications which require microwave bandwidths of 12 GHz or more and digital clock rates above 1 GHz. In particular, MSI digital devices appear to be ready for immediate development in high-speed interface circuit applications such as in new fiber-optic communication systems, instrumentation and high-speed computers. All of the companies who have recently announced commercial GaAs IC products are using Depletion-mode technology.

On the other hand, LSI components such as large RAMs and gate arrays use Enhancement-Depletion mode technology, which provides relatively high-speed clock rates ranging from 100 to 1000 MHz, but power dissipation levels much lower than available in silicon ECL devices. The speed/power performance of GaAs LSI devices will complement and interface well with high-speed CMOS LSI and VLSI currently in development. GaAs may ultimately reach higher gate complexity and lower cost per function than ECL because of its relatively simpler manufacturing technology. However, GaAs E-D LSI is still relatively new and more work remains to be done to guarantee the reliable, reasonable cost of these LSI devices. It will probably be another 12 months before GaAs LSI volumes become significant even though sampling of some LSI components is

expected in 1985.

Vitesse Electronics' (Camarillo, CA) plans include not only GaAs circuits, but also a high-speed computer family based on the technology. It will also implement GaAs products using both Depletion and Enhancement-Depletion mode devices. Dr. Lou Thomasetta, president of Vitesse, states that the company will introduce products with levels of integration larger than the 500 gates seen as the maximum for Depletion-mode MESFETs.

During the first quarter of 1986, Triquint Semiconductor (Beaverton, OR) also plans to move from Depletion-mode devices to Enhancement-Depletion mode gate arrays ranging in complexity from 500 to 2000 gates. The company notes that these arrays should have lower power dissipation levels than their ECL equivalents but higher operating speeds (at worst case 1 GHz toggle frequencies on flip-flops).

Both Vitesse and Gigabit Logic (Newbury Park, CA) plan to offer high-speed LSI-level standard parts such as multiplier/accumulators and multiplexers where they can increase performance over current bipolar offerings at a significant price premium. Dr. Thomasetta notes that parts currently marketed by TRW will be likely candidates.

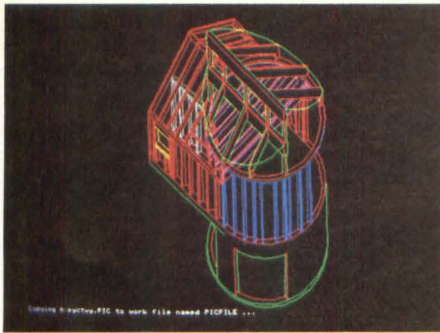
Although E-D mode devices may not be available for some time, medium-scale parts are offered by a number of manufacturers including Gigabit Logic and Harris Microwave Semiconductor (Milpitas, CA). Harris was one of the first companies to announce the commercial availability of two MSI parts last year. These devices were a 4-bit universal shift register and a divide by 2/4/8 binary counter. Both were originally designed for Cray computers. Over the past few months, Harris has added more parts including a master/slave D-type flip-flop, a divide by two/prescaler, a five-input NAND/AND gate and a digital phase comparator.

These devices currently have ECL-compatible inputs and outputs that allow them to be interfaced to high-speed silicon circuitry. However, providing ECL compatibility has its drawbacks. For example, 60% of the power consumption of the device could be saved by going to GaAs logic without the ECL interface. And since a large proportion of the die area is used solely for achieving ECL compatibility, pure GaAs devices could use much less real estate and be built cheaper.

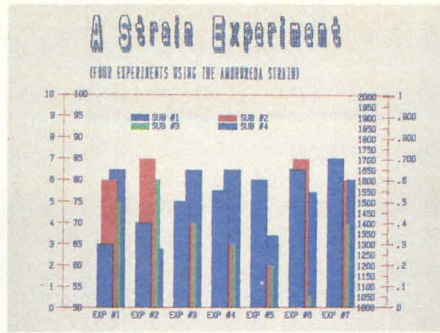
Gigabit Logic has also built a range of SSI and MSI GaAs logic devices based on its own capacitor diode FET process. It offers a number of parts including two- and seven-stage ripple counters, dual one to four fan-out buffers and a variable

Logic Gate Characteristic	DEPLETION MODE ONLY TECHNOLOGY				ENHANCEMENT-DEPLETION TECHNOLOGY		
	Buffered FET Logic (BFL)	Schottky Diode FET Logic (SDFL)	Capacitor Coupled Logic (CCL)	FET Diode FET Logic (FDFL)	Direct Coupled FET Logic (DCFL)	DCFL Push Pull (DCFL PP)	Diode FET Logic (DFL)
Noise Margin (1)	Med	Low-Med (2)	Med	High	Very Low	Low	Med (2)
Fan-Out Sens.	Low-Med	Med-High	High	Low	Med	Low-Med	Med-High
Fan-In Sens.	Med	Low	Med	Low	Med	Med	Low
Producibility	Med	Low-Med	Med	Med	Very Low	Very Low	Low
Speed (3)	Med	Med	Med (4)	High	Low-Med	Med	High
Power	High	Med	Med	Low-Med	Low-Med	Med	Low
Area Efficiency	Med	High	Low	Low-Med	High	Low	Low-Med
Supplies (5)	3	3	3	3	2	2	3

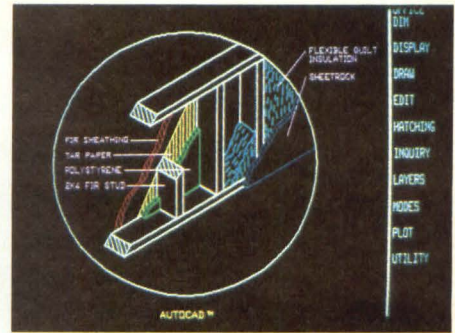
Table 1: This comparison of various GaAs logic types from Ford Microelectronics shows two proprietary Ford logic devices, FDFL and DCFL. Notes: 1) Only four input NOR gates were considered for gate array applications. 2) Depends on fan-out. 3) Fan-out of three (1500 μ of interconnect and three gate loads). 4) Severe area penalty as capacitive load increases to maintain speed. 5) Ground is considered as a supply.



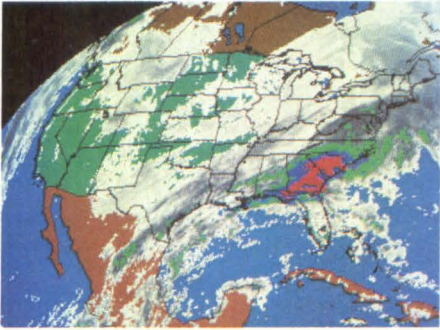
1. High Speed (MicroCAD Software)



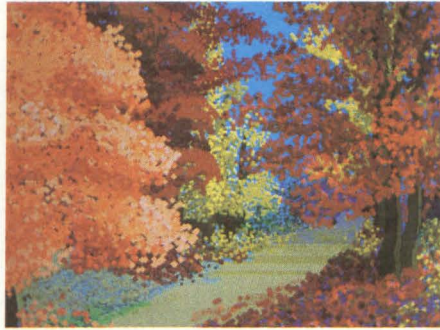
2. Dual Display Modes (Energraphics Software)



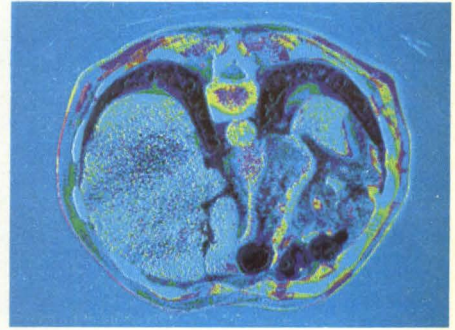
3. Simplified Processing (AutoCAD Software)



4. 9 Bit Planes (Courtesy WSI Inc., Bedford, MA)



5. 16.8M Color Shades (Courtesy Catherine Del Tito, Wave Graphics)



6. High Resolution (Courtesy University of North Carolina at Chapel Hill, Depts of Computer Science and Radiology)

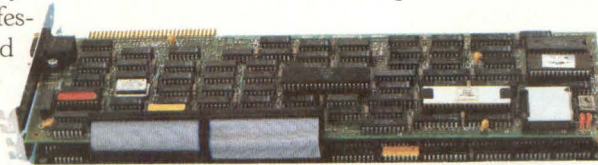
Six reasons why professionals continue to choose Vectrix for quality IBM XT/PC graphics.

Even though IBM offers a color graphics card, professionals still choose Vectrix. It's not surprising. Especially once they've seen us in action. Professionals know that our VX/PC Board Set delivers the quality and performance they need for serious color graphics.

The VX/PC Board Set provides advanced features that help simplify sophisticated graphics design. Besides displaying 512 simultaneous colors from a palette of 16.8 million, the VX/PC supports an extensive library of on-board graphics macros for ease of programming and fast design, as well as full emulation of the IBM color card. And, an on-board 16-bit micro-

processor frees your computer to concentrate on other tasks.

But that's not all. Our 9 bit planes



add an extra dimension of sharpness and clarity to your image that must really be seen to be appreciated. That's why it's not surprising to see Vectrix color cards in applications such as medical imaging, weather satellite data mapping, computer aided design and drafting, and graphics arts, to name a few.

What you will find most surprising, however, is the price. Our VX/PC Board Set was designed with the OEM in mind. So when comparing the performance of Vectrix with the competition, check the price too. You'll like what you see. For more information, contact Vectrix Corporation, 2606

Branchwood Drive, Greensboro, North Carolina 27408. Phone (919) 288-0520. Telex 574417.



Distributor inquiries welcome.

Inquire about our new Pepe Graphics Board Set

Seeking distributor(s) in Germany and Austria

IBM XT, IBM AT, and IBM PC are trademarks of International Business Machines Corporation, White Plains, NY. MicroCAD is a trademark of Imagimedia Technologies, Inc., San Francisco, CA. AutoCAD is a trademark of Autodesk, Inc., Sausalito, CA. EnerGraphics is a trademark of Enertronics Research, Inc., St. Louis, MO.

modulus divider.

Preserving the performance of E-D mode devices inevitably poses problems in packaging. Devices that operate with a bandwidth higher than 1 GHz and clock rates faster than 300 MHz need packages that provide 50Ω connection between the IC and the system circuit board. Although moderate cost microwave 50Ω packages have been in production for several years, there are no 50Ω packages with more than a few I/Os currently on the market. A number of innovative approaches are being offered by the GaAs IC manufacturers, such as the use of silicon chip carriers, the adoption of current multilayer packages to approximate coplanar I/O connections and the development of special coplanar chip carrier packages.

In addition to its SSI and MSI parts, Gigabit Logic has also disclosed information about its NanoRAM family of pipelined static RAMs. It is not the only entry in the field. As early as 1980, NTT (Kanogawa, Japan) produced a GaAs RAM. This part was only 16 bits and was followed in 1981 by a 256-bit device and in late 1982 by a 1K part with an access time of under 4 nsec. At the 1983 ISSCC, Fujitsu announced that it too had fabricated a 1K SRAM with a 4 nsec access time. By 1984, both

Fujitsu and NTT described 4K parts with under 3 nsec access times. Yet another Japanese company entered the fray in 1985 when NEC disclosed a current-mode logic compatible 4K GaAs static RAM with an access time of 0.97 nsec and a 2.3W power dissipation. To date, the largest chip described is a 16K device with a 4 nsec access time developed by NTT. Although none of these devices are available, it is evident from these disclosures that the Japanese have developed great expertise in this area.

In the gate array arena, a number of manufacturers currently offer less than 1000-gate gate arrays. To support the design environment, a wide range of CAD tools is available from vendors offering GaAs arrays. Logic simulation (in the form of detailed unit delay information at the gate or functional level) is the predominant form of timing analysis for arrays from Ford Microelectronics (Colorado Springs, CO), Harris Microwave Semiconductor and Triquint Semiconductor. SPICE device models are available on request but are not part of the normal design process. Cell libraries are available for the 100-gate equivalent arrays from Harris and Triquint, and are currently being developed for the Ford 500-gate gate array. Logic schematics will be the primary input for the Ford and Triquint arrays since they favor variable cell location. Harris recommends that designers lay out their own circuits since its arrays are at fixed locations.

COMPANY	DESCRIPTION	TECHNOLOGY	SPEED	POWER CONSUMPTION	COMMENTS
MULTIPLEXERS AND DEMULTIPLEXERS					
Honeywell	8:1 multiplexer	D-MESFET	2 gigahertz	4 watts	
Tektronix	8:1 multiplexer	D-MESFET	2 gigahertz	2 watts	
Ericsson	8:1 multiplexer	ECL	566 megahertz		
ANALOG/DIGITAL CONVERTERS					
TRW	3-bit quantizer	D-MESFET	1×10 ⁹ samples/sec.		
TRW/Honeywell	8-bit converter	E/D-MESFET	1×10 ⁹ samples/sec.		performance goal
TRW/Honeywell	4-bit converter	E/D-MESFET	3×10 ⁹ samples/sec.		performance goal
Sony	8-bit converter	bipolar	0.1×10 ⁹ samples/sec.	1.2 watts	
TRW	5-bit converter	bipolar	0.4×10 ⁹ samples/sec.		
MULTIPLIERS					
Fujitsu	16×16 bit	E/D-MESFET	10.5 nanoseconds	950 milliwatts	
OKI	8×8 bit	E/D-MESFET	8.6 nanoseconds	157 milliwatts	
Nippon Electric	16×16 bit	CMOS	45 nanoseconds	100 milliwatts	
Bell Laboratories	16×16 bit	NMOS	20 nanoseconds	1 watt	
GATE ARRAYS					
Honeywell	3,000 gates	D-MESFET	1.1 nanoseconds	100 microwatts/gate	
Honeywell	3,000 gates	E/D-MESFET	0.5 nanoseconds	100 microwatts/gate	
Tektronix	1,224 gates		100 picoseconds	250 microwatts/gate	
			50 picoseconds	550 microwatts/gate	
Honeywell	5,000 gates	CML	0.5 nanosecond	1 milliwatt/gate	
IBM	10,000 gates	TTL	1.4 nanosecond	0.57 milliwatt/gate	
MEMORY CHIPS (STATIC RANDOM-ACCESS MEMORY)					
Fujitsu	4 kilobits	E/D-MESFET	2.6 nanoseconds	0.7 watt	
Fujitsu	4 kilobits	E/D-MODFET	2 nanoseconds	1.6 watt	
			4.4 nanoseconds	1.86 watt	at 77 Kelvin
Nippon Telephone & Telegraph	16 kilobits	E/D-MESFET	4 nanoseconds	2.5 watts	at 300 Kelvin
Nippon Electric	4 kilobits	ECL	2.3 nanoseconds	1.6 watts	
IBM	64 kilobits	bipolar	2.3 nanoseconds	8 milliwatts	standby mode
			25 nanoseconds	270 milliwatts	cycle time
IBM	64 kilobits	NMOS	50 nanoseconds		
			20 nanoseconds		
MICROPROCESSORS					
	32-bit data path		200 megahertz		DARPA proposal
Motorola	32-bit data path	CMOS	16.6 megahertz	1.5 watts	
Bell Laboratories	32-bit data path	CMOS	11 megahertz	0.7 watt	
Hewlett-Packard	32-bit data path	NMOS	18 megahertz		

Table 2: Representative digital chips made with GaAs and high-performance silicon technologies. (Courtesy Scientific Honeywell)

Fingertip control

FLUKE 1722A INSTRUMENT CONTROLLER

Can make the difference
in your OEM system

Touch Here

The Fluke 1722A Instrument Controller

Of course, the biggest difference is 1722A touch-sensitivity. It will make your system truly user-friendly. And that sells systems!

But there's much more.

The 1722A Controller provides your customers with predictably controlled procedures. Even semi-skilled personnel can easily operate complex systems at the touch of a finger.

Designing the 1722A into your system is no problem. It's fully integrated and features a high-performance micro-computer, graphics display, 400K disk drive, complete software packages, plus RS-232-C and IEEE-488 I/O ports.

Most importantly, with the 1722A you



Panel or rack mountable, the 1722A fits right into your OEM system.

get Fluke support. You're working with a multinational corporation and worldwide service organization.

The 1722A Instrument Controller is available, on an OEM basis, in as few as

20-piece quantities for under \$6000. For further details, contact your local Fluke Sales Engineer or Representative. Or call us at **1-800-426-0361**.

Consider the 1722A in your next development. It will make your OEM system easier to build, to sell, to use, and to support. That's a big difference!

IN THE U.S. AND NON-
EUROPEAN COUNTRIES:

John Fluke Mfg. Co., Inc.
P.O. Box C9090, M/S 250C
Everett, WA 98206
206-356-5400, Tlx: 152662

IN EUROPE:

Fluke (Holland) B.V.
P.O. Box 5053, 5004 EB,
Tilburg, The Netherlands
(013) 673973, Tlx: 52237

FLUKE®

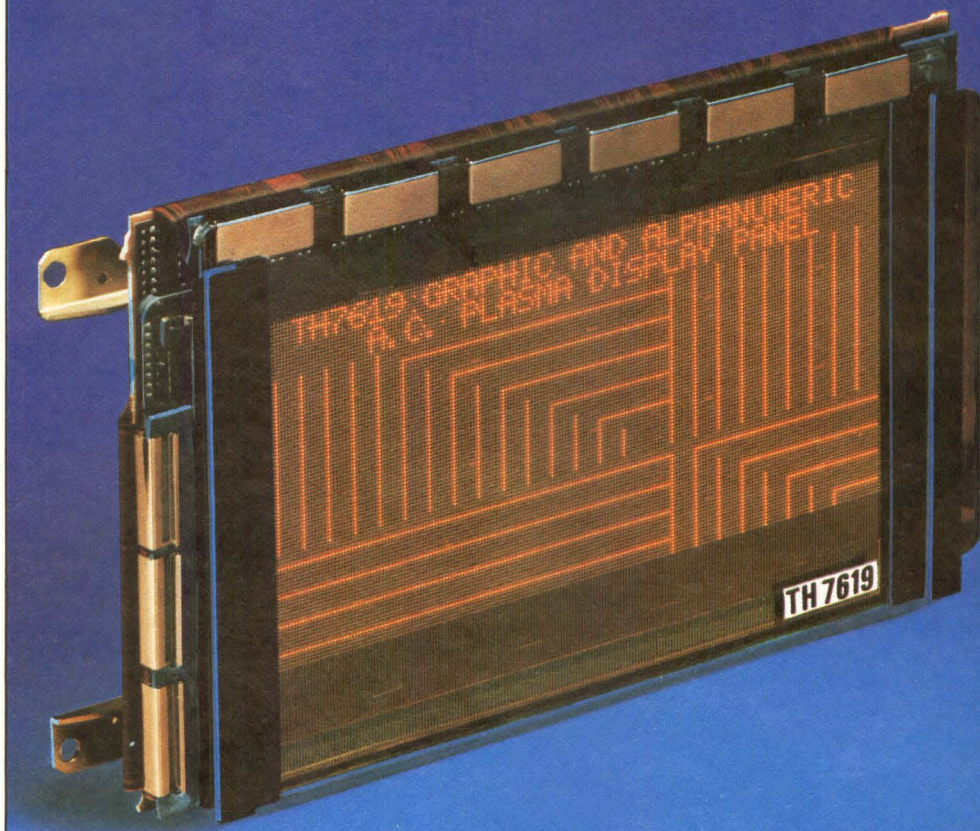
TODAY'S DISPLAYS

Thomson-CSF ac plasma panels: slim, low on power drain, and simple to connect. They're a perfect match for your terminal, anywhere: machine tools, bank terminals, mobile equipment...

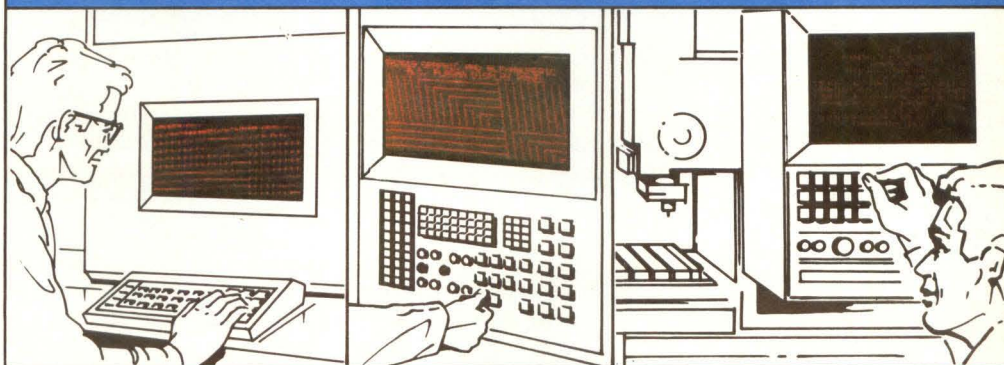
And they bring you more:

- ruggedness and unlimited lifetime (ac technology),
- unequalled viewability,
- competitive price.

Thomson-CSF's flat panels: now in the age of plasma.



THOMSON-CSF
COMPONENTS CORPORATION
Electron Tube Division
301 Route Seventeen North
RUTHERFORD, NEW JERSEY 07070
Tel. (201) 438.23.00.
TWX: 710989 7286.



Belgique BRUXELLES Tel. (32-2) 648 64 85 Tx: 23113 THBXL B	Brasil SAO PAULO Tel. (55-11) 542 47 22 Tx: (011) 24226 TCSF BR	Canada MONTREAL Tel. (1-514) 288 41 48 Tx: 5560248 TESAFI MTL	Deutschland MÜNCHEN Tel. (49-89) 78 79-0 Tx: 522 916 CSF D	España MADRID Tel. (34-1) 4051615 Tx: 46033 TCCE E	France BOULOGNE-BILLANCOURT Tel. (33-1) 46 04 81 75 Tx: THOMTUB 200 772 F
Italia ROMA Tel. (39-6) 639 02 48 Tx: 620 683 THOMTE I	Japan TOKYO Tel. (81-3) 264 63 46 Tx: 2324241 THCSF J	Sverige STOCKHOLM Tel. (46-8) 63 50 60 Tx: 12078 THCSF S	United-Kingdom BASINGSTOKE Tel. (44-256) 29155 Tx: 858865 TESAFI G	U.S.A. RUTHERFORD, NJ Tel. (1-201) 438 2300 TWX: 710989 7286	

VME Building Blocks Make Image Processing A Snap

by Shep Siegel, Senior Engineer, Datacube Inc.

Modular video signal processor architectures have evolved from machine vision and pattern recognition applications, which demand a specialized imaging function designed in hardware. Since each application uses a unique algorithm, different hardware is required for each task. With demands for easy algorithm modification, more complex operations and increased bandwidth, hardware modularity is a critical issue. Without it, products are restrained at fixed performance levels.

This trend is evident in MaxVideo, an architecture based on modularity and interconnection, not dynamic memory trends. And, although the initial MaxVideo family members are focused on common machine vision and pattern recognition algorithms (a combination of the algorithm and the architecture of a process), the MaxVideo family has a much broader scope.

Modularity

Users of board-level image processors have to meet a range of performance requirements and functional needs. By providing modules, the task of adding new functions and performance requirements can be reduced dramatically. Designing these modules to tier in a linear fashion allows the integrators to increase processing power by adding more processing hardware. The result of this tiering concept is that a broad price/performance range may be met by single module designs.

Modularity, however, must not impose a particular processor architecture. Conventional microprocessors function by sequential von Neumann processing which is also used by array processors but with generally faster cycle times. Image processing is, in many cases, better tackled through a data flow processor.

Parallelism

In image processing, parallelism is important. A sequential von Neumann computer, a 68000, an array processor or a Cray, simply cannot exploit the parallelism present in many image processing algorithms. Prevailing designs must exploit parallelism wherever possible and practical. The results are inexpensive modules that outperform supercomputers on key image processing benchmarks. There are at least four dimensions to parallelism in image processing: operator parallelism, image parallelism, neighborhood parallelism and pixel-bit

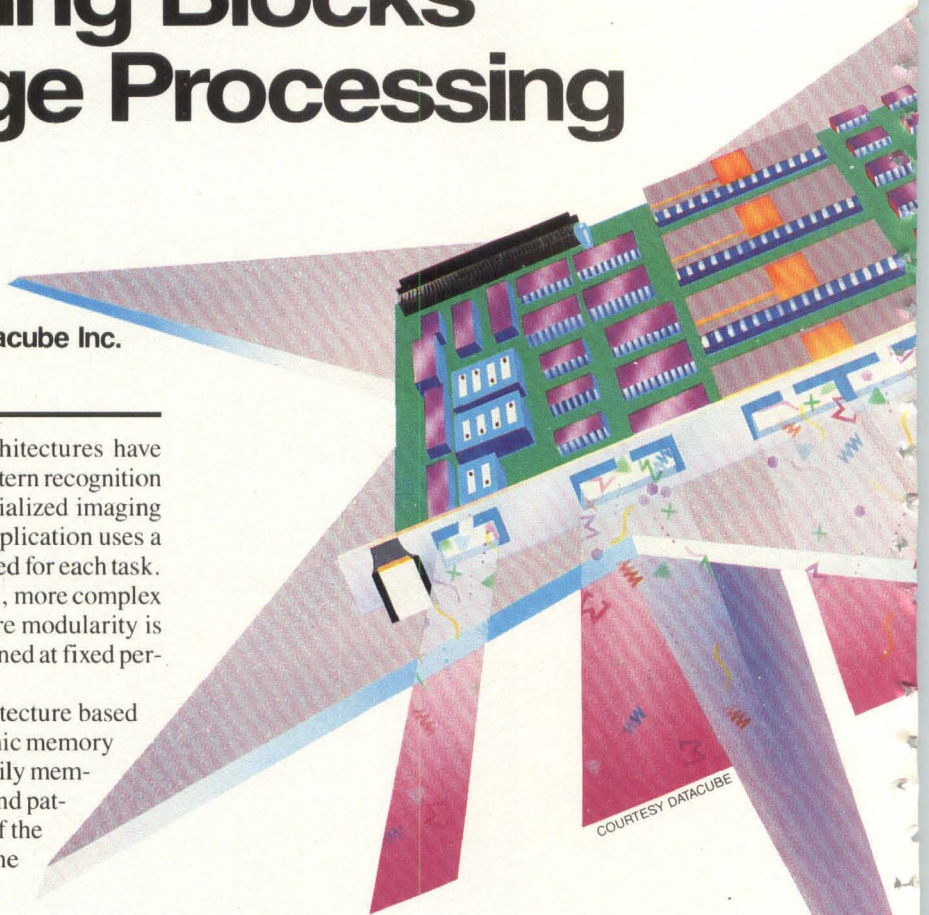
parallelism.

Operator parallelism is equivalent to pipelining and used throughout the MaxVideo family from Datacube (Peabody, MA). For example, in the real-time computation of the Sobel operator, one type of module would perform the x and y gradient operation and another would find the Euclidean distance between the two results (**Equation 1**).

$$S(m,n) = \sqrt{(dx)^2 + (dy)^2} \quad \text{Equation 1}$$

Image parallelism is used when separate processors synchronously process neighborhoods destined for different pixels in the same output image. An example would be the real-time conversion of a 512×512 image to a 1024×1024 image. Multiple MaxVideo Interpolators, each working on a quadrant of the target image, would be considered as operating in parallel. Single Instruction Multiple Data (SIMD) processors are often used as parallel image processors.

Neighborhood parallelism involves parallel access to a neighborhood. This parallelism is exhibited within all of MaxVideo's systolic processors. When Featuremax searches for neighborhood features by looking at all the neighbors at the same time, it uses neighborhood parallelism. Pixel-bit parallelism, used extensively in image processing, involves accessing all the bits of a single pixel. MaxVideo's MAXbus digital interconnect, in conjunction with its VME/VMXbus, allows a variable degree of parallelism across all of these dimensions.



Command And Control Bus

Users of image processing hardware often have the responsibilities of systems integrators. Image processors, I/O processors and control computers all need to communicate over a common bus. An established standard is needed. In the implementation of MaxVideo, the decision was made to base the family on double-height VME boards. Several factors influenced this decision. The small form factor of the double-height Euro-card best exploited VLSI components, high-speed CMOS memory and surface mount technology.

The VMEbus allows MaxVideo users to use their own proprietary boards and ones from other VMEbus vendors. By keeping to the double-Eurocard form factor, the MaxVideo boards remain mechanically and electrically compatible with other true VME boards. In the design, the secondary P2 connector was not "stolen" for transfer of digital video data. Instead, this was accomplished across the front of the boards by a MAXbus. The P2 connector was used for 32-bit VME and VMX data transfers in accordance with the VMEbus specification.

Image Bus

Although the VMEbus and its VMX subset provide adequate bandwidth for data transfer to and from von Neumann processors, they are poorly suited for high-speed synchronous transfers used by programmable pipelined processors. The MaxVideo family uses programmable pipelined processors, and the MAXbus provides a way of interchanging video data, in a synchronous pipelined manner, between arbitrary modules. The bandwidth of MAXbus can be extended by adding additional pipelines. Because many MaxVideo systems will be used in harsh EMI laden environments, the MAXbus interface was designed to be noise and skew tolerant.

MAXbus relies on four special differential ECL signals feeding every MaxVideo board. From these signals, a pixel clock and its multiples, as well as standard television synchronization signals, may be derived. The use of differential ECL allows the skew dependent TTL clocks to be well controlled. In this way, pixel rate pipelines may be sent between any arbitrary set of modules without flaw.

The fundamental basis of the MAXbus is the byte-wide video pipeline. On this 14-way ribbon cable, 8-bits of data from one of two sources may be transmitted to up to 10 receivers every 100 nsec. Thus, one MAXbus cable provides 10 Mbytes/sec data transfer. MAXbus, like the modules it interconnects, obeys the tiering dogma: Two cables provide twice the bandwidth, trans-

ferring 20 Mbytes/sec. If more interconnect bandwidth is needed, more interconnects are added. No limit of bus transfer capability exists as in fixed bus systems.

The result is much like a video patch panel. MaxVideo modules are interconnected together in many ways until a final architecture is settled upon. During development, an algorithmist may change interconnects several times as the many possible solutions to the problem are tried. Crosspoint switch modules extend the intrinsic multiplexing capacity when required. The data being transferred, although often scan-sequential pixel values, can represent almost anything. Instructions for processors and addresses for transformations may be passed between processors.

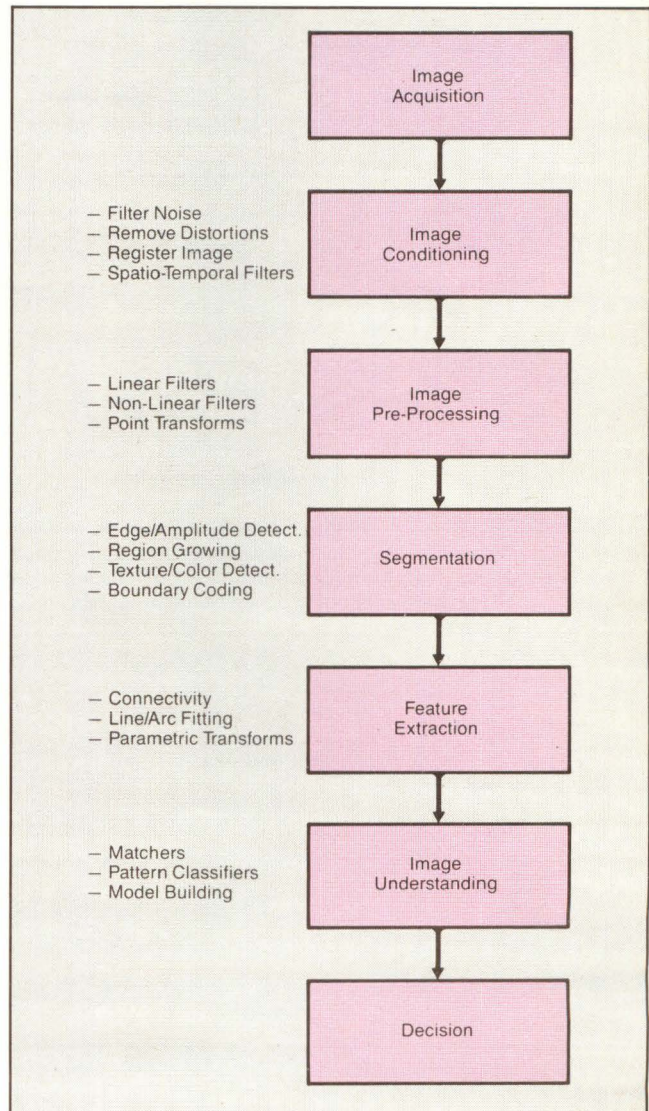


Figure 1: Typical sequence of events for image recognition processes.

MaxVideo users may design their own processors onto the MAXbus, using a MaxVideo Protomax board. This board is a wirewrap VMEbus slave with a MAXbus interface to allow new hardware designs to be placed into the MaxVideo family.

Performing Operations

A typical sequence of events for an image recognition process from acquisition to decision is shown in **Figure 1**. Historically, the operations require a great amount of computrons (arbitrary unit of computer resource) and time, despite their repetitiveness. This is where the MaxVideo design effort has been focused. MaxVideo boards such as VFIR, SNAP and MaxSP can perform most of the processing at these levels. The result is often a set of images requiring feature-list extraction which translates a set of image features into a table of x, y coordinate pairs. The MaxVideo Featuremax board performs this task in real time. Processing from extraction through decision requires far fewer, though more complex, decisions. If low-level processing could be performed by dedicated hardware, the supervising CPU would be

free for high-level decisions.

Relieved of the burden of image processing, a 68000 is all users need to perform many complex vision tasks. Even with the 32-bit 68020 and 68881 making their debut, image processors will still use dedicated hardware.

Imaging Configurations

By creating a modular imaging system, it is possible to realize many compute-intensive functions at high speed. Two examples of these types of functions include edge detection and real-time filtering. **Figure 2** shows two MaxVideo VFIR boards performing 3×3 convolutions in parallel. The convolution kernels are such that while one VFIR board is computing the gradient along the X-axis, the other is computing the gradient along the Y-axis. The resulting X and Y gradients can be used to evaluate many edge operators. A general-purpose look-up table is provided by an 8-Kbyte SRAM on the MaxSP board. The result of this computation is the edge magnitude and direction. This example is common in relaxation algorithms used in edge detection and perimeter binding.

An example of a real-time separable filter is shown in **Figure 3**. Separable transforms are a subset of the general class of two-dimensional transforms. For example, if a transform can be

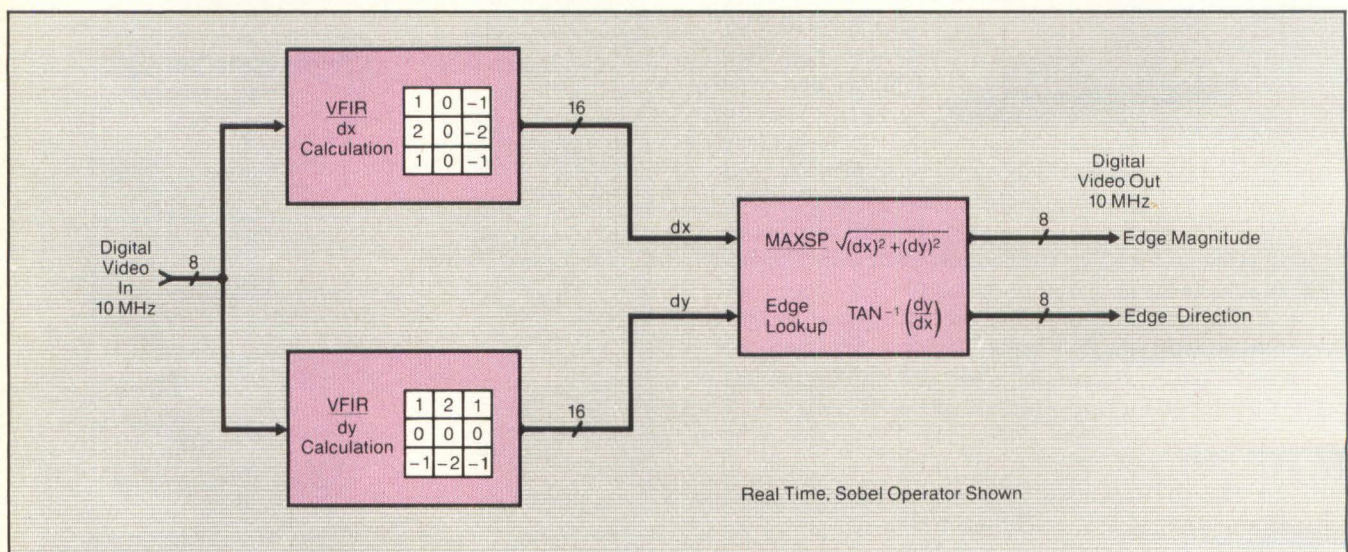


Figure 2: MaxVideo configuration for real-time edge detection. In operation, two parallel VFIR modules compute the orthogonal X and Y gradients. A MaxSP module then finds the edge magnitude and direction through a look-up table of $\sqrt{(dx)^2 + (dy)^2}$ and $\text{Tan}^{-1}(dy/dx)$. Other edge operators can then be implemented by changing the convolution kernels and look-up tables.

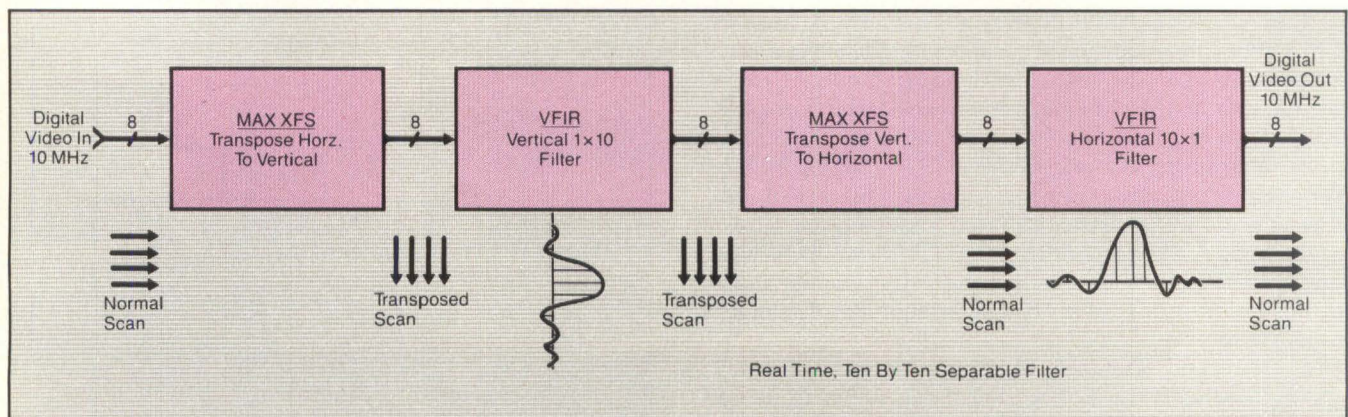
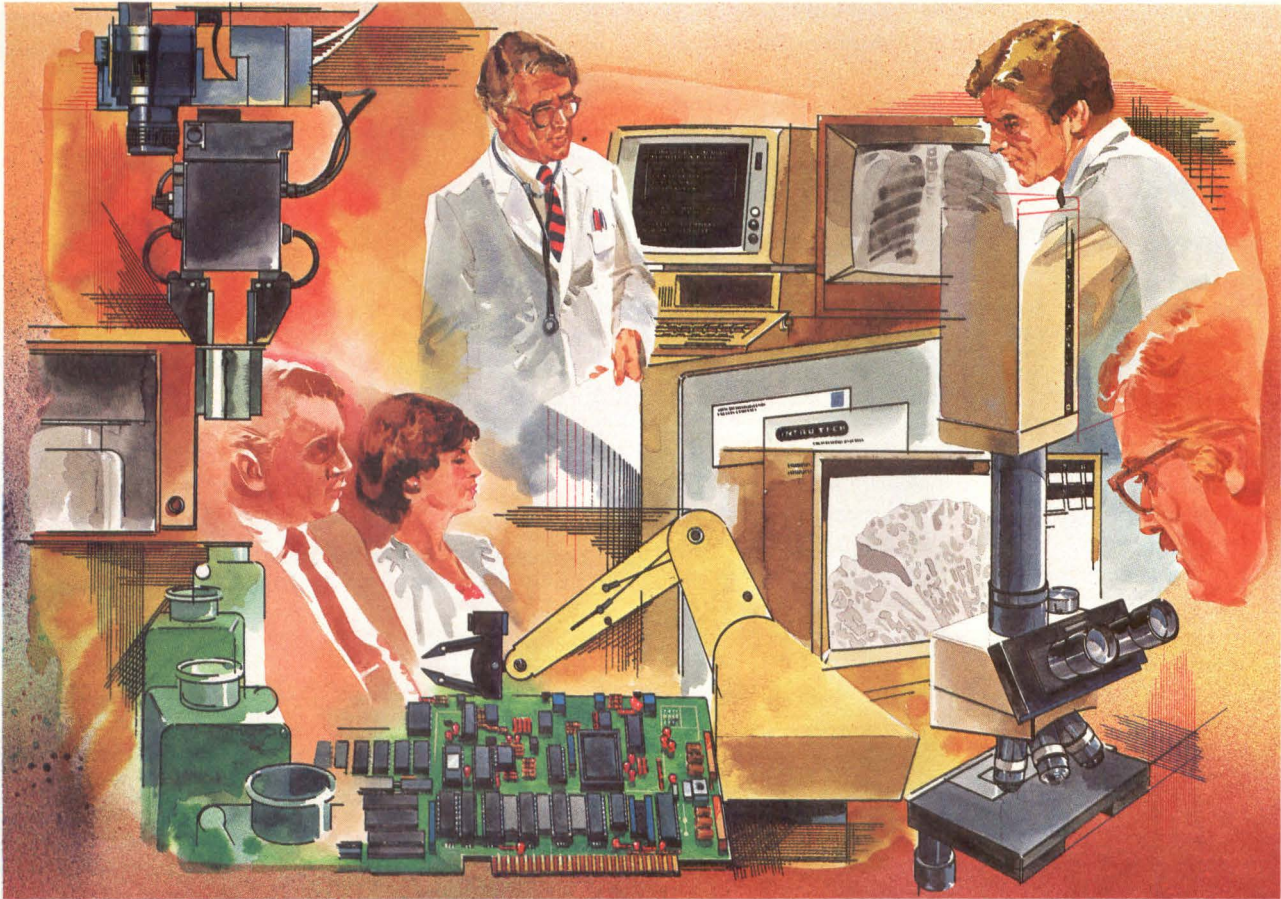


Figure 3: Separable filters in real time. First, the MAX XFS transposes the horizontal scan to a vertical scan. The VFIR then performs a 1×10 FIR filter and the second MAX XFS transposes the vertical scan back to a horizontal scan. The second VFIR board performs a 10×1 vertical filter to complete the process. In applications where less than real time is acceptable, the hardware requirement may be reduced to a single MAX XFS and VFIR board.

INTRODUCING PCVISION™'S BIG BROTHER



You already know the other members of our PCVISION family:
The PCVISION Frame Grabber . . . The *first* image processing hardware for the IBM PC. **ImageAction** . . . The *first* user-friendly image processing software for personal computers. Now we are pleased to introduce the newest addition to the family:

The FG-100-AT

The *first* image processing hardware module designed specifically for the IBM PC AT. The FG-100-AT is the only board on the market that takes full advantage of the speed and expanded capabilities of the IBM PC AT. It gives you all the power and flexibility of the PCVISION Frame Grabber, and includes:

- 12 bit-planes of frame memory
- Real-time arithmetic and logic processing (summation, subtraction, averaging, etc.)
- Extensive graphic overlay capabilities
- Hardware pan, scroll, and zoom
- Memory access to eight pixels simultaneously

To find out how the FG-100-AT can provide your personal computer with the high-performance image processing capabilities of systems costing much more, call our Sales

Department at any of the numbers listed or write. Dealer inquiries are invited.

Leaders by Design

IMAGING

Imaging Technology Incorporated
600 West Cummings Park, Woburn, MA 01801
(617) 938-8444 Telex 948263

Southern California Office
Northern California Office
Midwestern Office

(714) 960-7676
(408) 748-9313
(313) 855-2680

© 1985 IMAGING TECHNOLOGY INCORPORATED
PCVISION™ and ImageAction™ are trademarks of Imaging Technology Incorporated.
IBM is a registered trademark of International Business Machines Corporation.

parameterized independently along orthogonal axes, it is separable. Indeed, many transforms used in image processing are separable. A separated 10×10 filter requires only 20 multiply operations as opposed to the 100 operations required by the general class filter. In **Figure 3**, MaxFS, the transposing framestore, is used to transpose horizontal scan to vertical scan and then back again. This allows the VFIR's 10×1 multiplier array to be applied both vertically and horizontally. The result is a real-time 10×10 filter accomplished with minimal hardware.

Software

Control software complexity for MaxVideo boards varies between applications. At Datacube, software is written in C. MaxVideo boards are designed to minimize the CPU overhead. The VFIR board, a 10-point digital filter, has a few control registers and 10 coefficient registers. And software is needed only to load the coefficients over the VMEbus.

Software techniques may be used within MaxVideo to isolate levels of functionality. If a particular algorithm requires a 10×10 convolution, the high level description needs to know only that. Intermediate-level code may determine the hardware resources available to perform the operation. The more available resources, the faster the operation is performed.

MaxVideo represents a novel approach to image processing. Since there is a need for modular digital signal processing tools, MaxVideo provides the vehicle for the design of a modern, adaptive

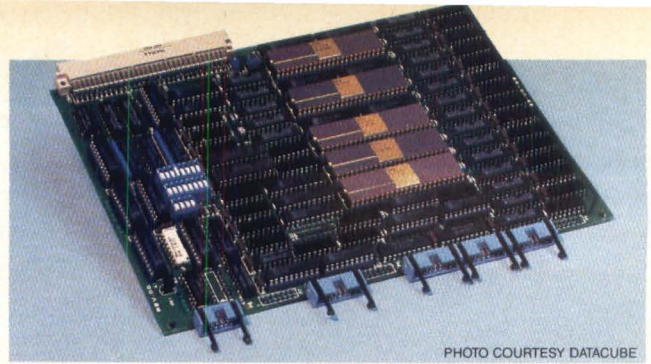


PHOTO COURTESY DATACUBE

vision system. The open architecture, in conjunction with MAX-bus, allows the family to address a broad price/performance range now and in the future.



REFERENCES

1. Danielson, P. and Leviaidi, S., "Computer Architectures for Pictorial Information Systems," *IEEE Computer Journal Society*, Piscataway, NJ. November 1981, pp. 53-66.
2. Hall, E., *Computer Image Processing and Recognition*, New York, NY. Academic Press, 1979.
3. Kittler, J. and Duff, M., *Image Processing System Architectures*, Letchworth, Hertfordshire, England. Research Studies Press Ltd., 1985.

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful	607
Useful	608
Somewhat Useful	609

The Compact, Low-Cost BLOB-1 Binary Image Pattern Recognition System Introduces Advanced Capabilities.

The new BLOB-1 Binary Image Pattern Recognition System is a unique design. BLOB-1 utilizes the SRI* pattern recognition algorithm.

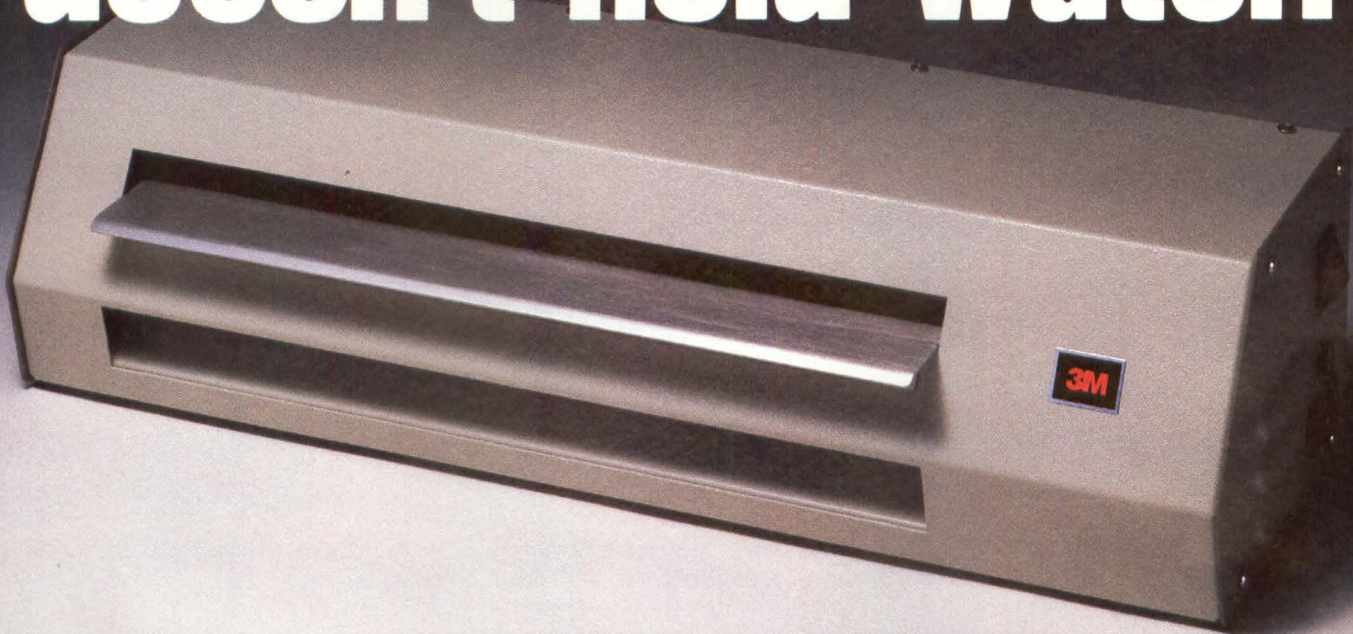
It's a small, low-cost system that excels as an image data processing unit in factory automation, as well as robot eyes. BLOB-1 converts visual images into 39 feature parameters and transmits the data through an RS232C interface to the host computer. Patterns are precisely measured and/or identified at high speed.

Contact Intertek today for complete details on the remarkable BLOB-1.

*Stanford Research Institute

Marketed by:
INTERTEK, INC.
7-4-6 NISHI-SHINJUKU, SHINJUKU-KU, TOKYO 160, JAPAN
TEL: (03) 363-6649 TELEX: J 28497 FETC FAX: (03) 365-5631

Quite frankly, this processor just doesn't hold water.



Or chemicals, or solvents, or anything else that makes a mess or wastes time

It's a totally dry processor for 3M Dry Silver Papers and Films. There's nothing in it that needs to be mixed or can spill or stain. Just heat. And it can process all kinds of electro-optical images in as little as four seconds.

But there's more than speed and dry instant processing to 3M's improved Dry Silver Papers and Films. Perfect for a wide range of imaging applications, 3M Dry Silver systems offer:

- Spectral sensitivity compatible with most commercially available electro-optical sources.
- Photographic quality and resolution similar to wet-process materials.
- Sufficient sensitivity to handle faster writing rates or low energy light sources.

3M Dry Silver Papers and Films hold nothing but opportunity for you

Faster access to high quality, permanent hardcopy images is an advantage anyone involved in optical recording can appreciate. And now you can have access to the time-saving proprietary technology of 3M Dry Silver processing for your own systems. We offer over 20 years of experience in dry silver media development and associated thermal processor hardware to our OEM partners. Together we can make your imaging future much brighter.

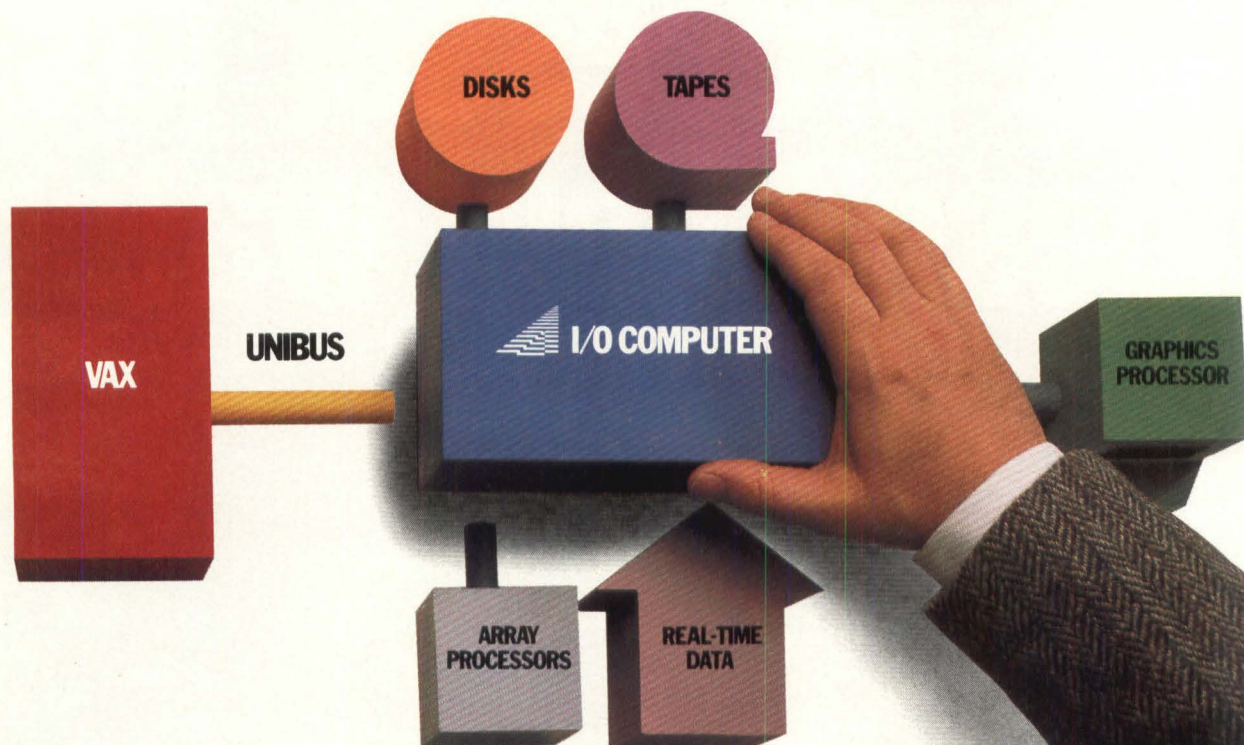
Contact us today and discover the opportunities 3M Dry Silver systems hold for you.



Imaging Systems Division/3M
223-2SW 3M Center
St. Paul, MN 55144-1000

3M hears you...

THE MOST SIGNIFICANT BREAKTHROUGH IN VAX SYSTEM PERFORMANCE SINCE THE ARRAY PROCESSOR.



Introducing the Aptec 2400 I/O Computer – a new class of computer that can increase the throughput of VAX-based systems as much as 40X. Simply. And economically.

By eliminating the I/O bottlenecks that limit performance, the Aptec I/O Computer makes your peripherals work faster and more efficiently. Including disks and tapes, APs, graphics/image processors, and special purpose devices.

It lets you achieve true super-computer performance with any VAX by allowing efficient integration of multiple array processors.

And, the Aptec I/O Computer permits dramatic new levels of performance in real-time data acquisition and analysis.

Not since the array processor has any development done so much to boost the performance of minicomputer systems.

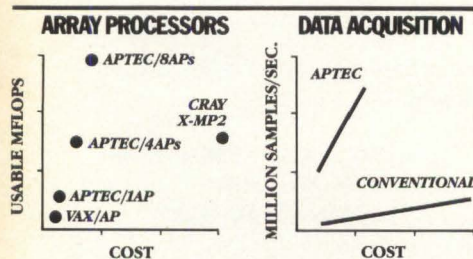
Here's how it works: The Aptec I/O Computer creates an independent, 24 MB/sec, FILES-11 I/O environment that allows VAX-shared peripherals to transfer data at full speed, free from VAX bandwidth limitations.

From 1 to 200 MB of high speed memory is directly accessible by your attached peripherals and VAX.

And, the Aptec I/O Computer provides the intelligence to control peripherals, data transfers and peripheral computations – with minimal involvement of the VAX CPU, the VMS operating system or the Unibus.

Peripheral operations become more efficient. Attached processors work at peak efficiency. And your VAX is free to provide better service to your on-line users.

Learn how the Aptec 2400 I/O Computer can unleash the performance potential of your VAX system. For the complete story on this exciting new class of computer, write or call Aptec today.



The Aptec I/O Computer will unleash the performance potential of your VAX.



Aptec Computer Systems, Inc.
10180 SW. Nimbus Ave.
Portland, OR 97223
(503) 620-9840
Telex 467167

VAX, Unibus and FILES-11 are registered trademarks of Digital Equipment Corp.
© Copyright 1985 Aptec Computer Systems, Inc.

Video Filters Process Pictures Precisely

by Vince Emmerson, Director, Matthey Electronics

Electronic images in robotics, television broadcasting, computer graphics, diagnostic medical equipment, fiber optic transmission equipment and similar applications are nearly all subjected to some form of digital processing. In imaging, analog information is digitized before processing and then converted back to analog form for display. In graphics, information is generated by computer, manipulated and then converted to analog form for display. In both these areas, analog low-pass filters can help the designer achieve the best picture quality.

An example of the quality improvements that can be gained on video signals using low-pass filters is shown in **Figure 1**. This figure shows a typical 5 MHz electronic image test signal degraded by out-of-band noise. By passing the video signal through a video filter, the signal can be substantially improved (**Figure 1b**). The Matthey MLW range of filters used in this example extends to a lowest cut-off frequency of 2.36 MHz. For cut-off frequencies below 2.36 MHz, the FLM range can be used.

Numerous types of imaging equipment are built following the filter guidelines in **Figure 2**. These guidelines are essential if the best performance is to be achieved. In other equipment, simpler filters or no filters at all can be used. Filters fall into two groups: prefilters (for antialiasing) and postfilters (for interpolating the D/A sampled data). In each group, the shape, cost and characteristics will vary according to the application.

Prefilters

The prefilter should present to the A/D converter a signal with a truncated spectrum to minimize the energy of frequency components which could alias during the digitizing process. In performing this function, the filter should be virtually transparent to the signal spectrum. **Figure 3** shows a 1T (10 MHz bandwidth) pulse after transition through an A/D, D/A converter, sampling at 13.5 MHz. The waveform in **Figure 3** results when only a postfilter is used. Antialiasing filters were omitted.

Aliasing components can be seen because of the presence of information above the half-sampling frequency in the input signal. The waveform in **Figure 4** shows how the aliasing components can be removed by the addition of an antialiasing filter prior to digitizing. The phase-equalized 75 Ω filters used in this

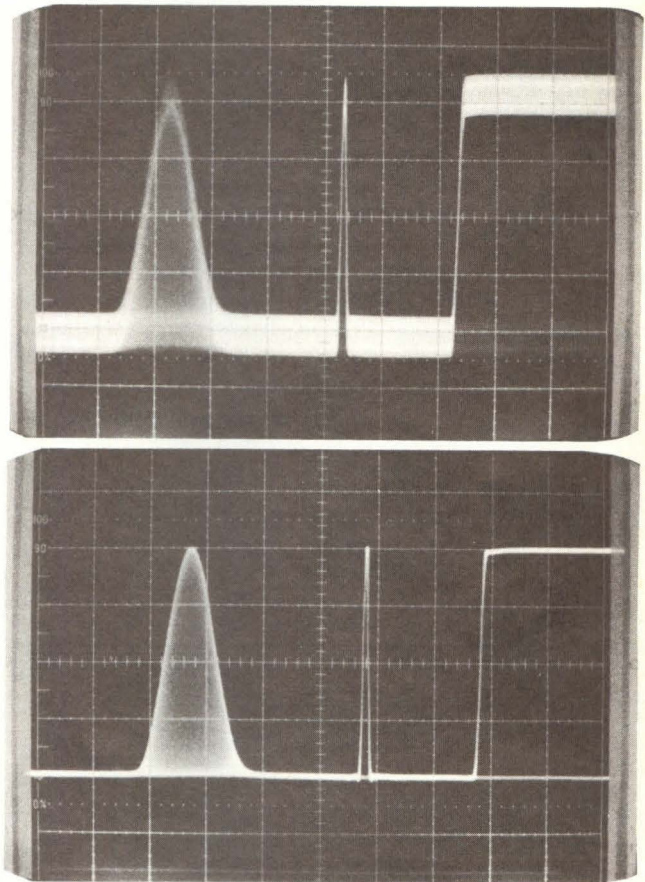


Figure 1: (a) Typical 5 MHz image test signal degraded by out-of-band noise. (b) Clear signal after passing through the Matthey MLW 532P video filter.

example are MLY 1350/15/2 for antialiasing and MLY 1350/15/2S (with passband shaped for $\text{Sin } x/x$ correction) for postfiltering.

The exact shape of the truncation, the attenuation at the Nyquist (or half sampling) frequency and the amount of stop-band attenuation must be determined by the designer. For example, prefilters which have sharp transition to maximize the pass bandwidth for a specific half-sampling frequency attenuation (HSFA) will exhibit slightly more ringing in the time domain (**Figure 5a**). This ringing is due to difficulties in main-

taining a small group delay ripple over the passband. Prefilters which have a softer transition will exhibit minimal ringing in the time domain, but will provide a reduced pass bandwidth if the same HSFA is involved (Figure 5b).

The HSFA is sometimes specified around 40 dB. Theoretical studies have shown that the HSFA for individual filters can be reduced to a value between 12 dB and 20 dB before unacceptable levels of aliasing distortion appear. The result of prefiltering is an increased bandwidth in the baseband signal region. No disadvantages occur with system stopband attenuation since the HSFA's on prefilters and postfilters are roughly additive. In many imaging systems, a stopband attenuation of >40 dB is usually satisfactory, but the increasing appearance of 12-bit converters in these systems will demand 60 dB attenuation.

In the design of the Matthey range of filters the stopband attenuation is maintained to approximately 100 MHz. This is important in minimizing crosstalk (at 50-60 MHz) arising from the high energy contained in modern IC switches.

Postfilters

Postfilters can have a dual role. They must accept the signal from the D/A converter interpolating the D/A sampled data to yield a good video signal. And if the D/A converter output spectrum is affected by the $\text{Sin } x/x$ function due to the sampling process, the filter passband response can be shaped to counteract it and yield a net flat video response. Since the $\text{Sin } x/x$ function is calculable and predictable for a given sampling frequency, the compensation shaping is designed to comply with the theoretical shape within 0.2 dB peak to peak.

Essentially, the parameters important in the prefilter are equally important in the postfilter. However, opinions differ and equipment manufacturers have to opt for a filter which meets their own needs. Two options exist in postfilter response design: a cut-off response that is identical to the prefilter response and one that is slower. If the cut-off response is identical, the signal

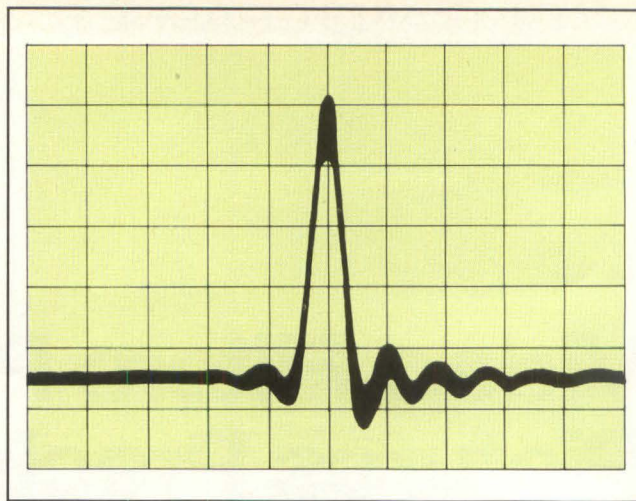


Figure 3: A 10-MHz bandwidth pulse after transition through an A/D converter and D/A converter, sampling at 13.5 MHz. This waveform results when only a postfilter is used.

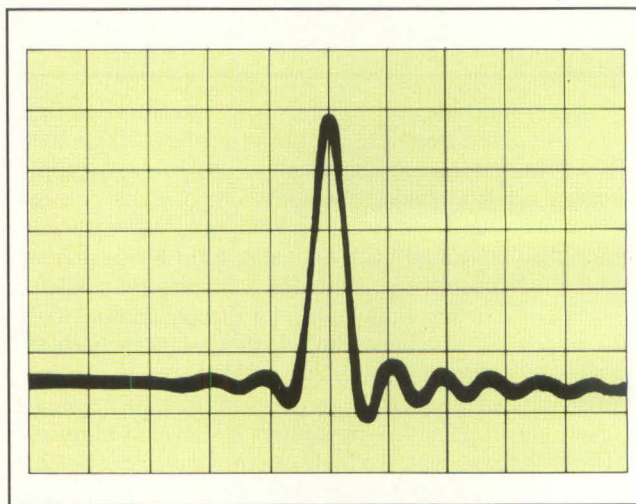


Figure 4: Aliasing components removed by the addition of an aliasing filter prior to digitization.

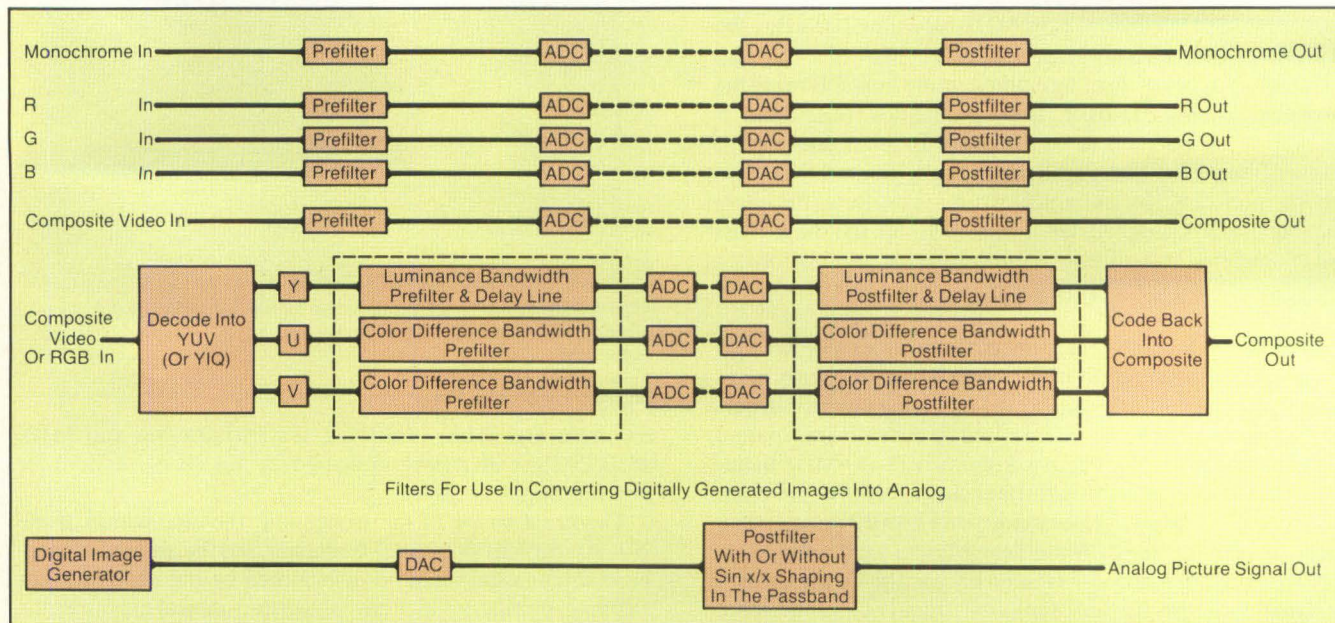
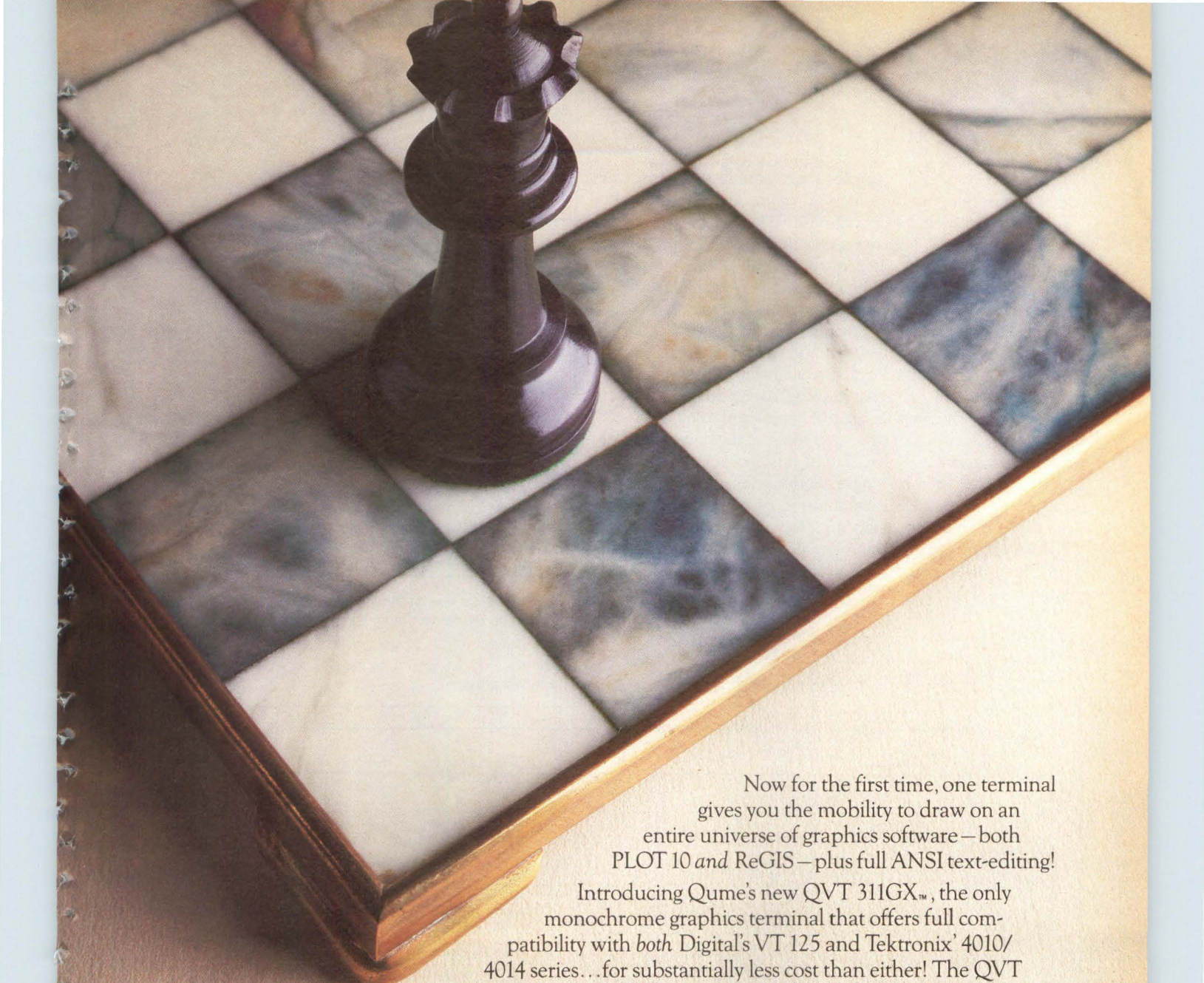


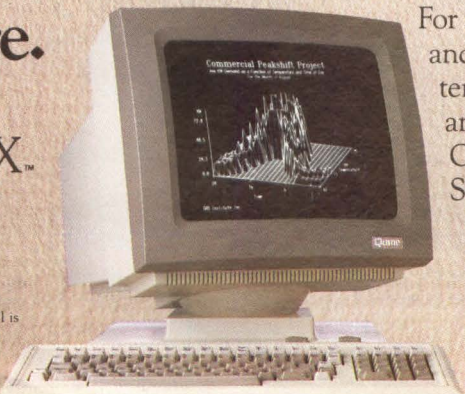
Figure 2: Filters for digital image enhancement or manipulation. Programmable DIP video delay lines enable the designer to compensate for the differences between Y and U/V channels. Additional delay is available so that other transmission path differences can be accommodated in the one delay line package. In the postfilter, the passband can be shaped to compensate for the $\text{Sin } x/x$ function.



When you want
a graphics terminal
that lets you move
in all directions,
we'll be there.

QVT-311GX™
MONOCHROME
TERMINAL

Tektronix 4010, 4014 and PLOT 10 are registered trademarks of Tektronix Inc. VT 125 and ReGIS are trademarks of Digital Equipment Corporation. ANSI is designed to American National Standards Institute, Inc. ANSI X3.64-1979 guidelines.
© 1984 Qume Corporation.



Now for the first time, one terminal gives you the mobility to draw on an entire universe of graphics software – both PLOT 10 and ReGIS – plus full ANSI text-editing!

Introducing Qume's new QVT 311GX™, the only monochrome graphics terminal that offers full compatibility with both Digital's VT 125 and Tektronix' 4010/4014 series...for substantially less cost than either! The QVT 311GX provides full bit-mapped graphics on a 14" non-glare white phosphor screen, with four shades of gray. There's an optional mouse device as well.

As with all Qume terminals, the QVT 311GX is engineered to the highest standards of performance and reliability, and backed by our experience and resources as an ITT company. So whatever moves you make in the years ahead, you know we'll be there with expert service and technical support.

For more information about the QVT 311GX and Qume's other graphics and alphanumeric terminals, or our full line of daisywheel printers and disk drives, call (800) 223-2479.

Or write Qume Corporation, 2350 Qume Drive, San Jose, CA 95131.

Qume®
A Subsidiary of ITT

Circle 35 on Reader Inquiry Card

bandwidth is maximized but may introduce ringing effects. If the cut-off response is slower, then some reduction in bandwidth occurs, but the effects of ringing are reduced.

In TV broadcasting, the options pose a dilemma for equipment manufacturers. The slower cut-off response results in pictures of seemingly excellent quality in standalone equipment. However, when used in TV multistage systems, the slight reduction in bandwidth accumulates and may cause an unacceptably reduced picture quality. The identical cut-off response can therefore be regarded as more desirable from a system standpoint. The extra bandwidth allows maximum signal fidelity to be passed along to the next processing system. The ringing which can be expected to result from the increased bandwidth can be removed at the end of the processing sequence. A gaussian or raised cosine filter is usually used to minimize ringing at this point.

In electronic picture manipulation or enhancement, however, equipment designers must look first at the slower response option. Part of the range of cut-off shapes now available for 8-bit systems is shown in Figure 6. From an equipment layout point of view, the filters can be mounted as single components on another printed circuit card and still not exceed 1/2" height.

Matthey products are distributed by TV Equipment Associates, Box 393, Boway Road, South Salem, NY 10590.

DD

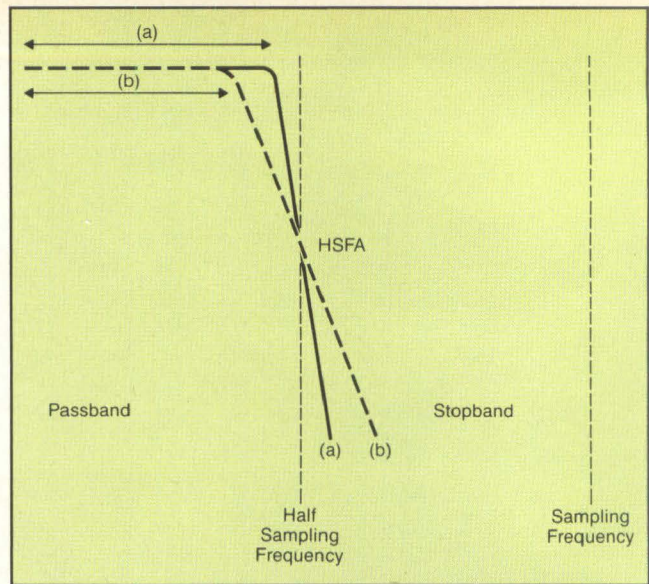


Figure 5: Effects of filter transition. (a) Prefilters with sharp transition will maximize pass bandwidth but will exhibit slight ringing in the time domain. (b) Prefilters having a softer transition will exhibit minimal ringing but will provide a reduced pass bandwidth.

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

- Very Useful 604
- Useful 605
- Somewhat Useful 606

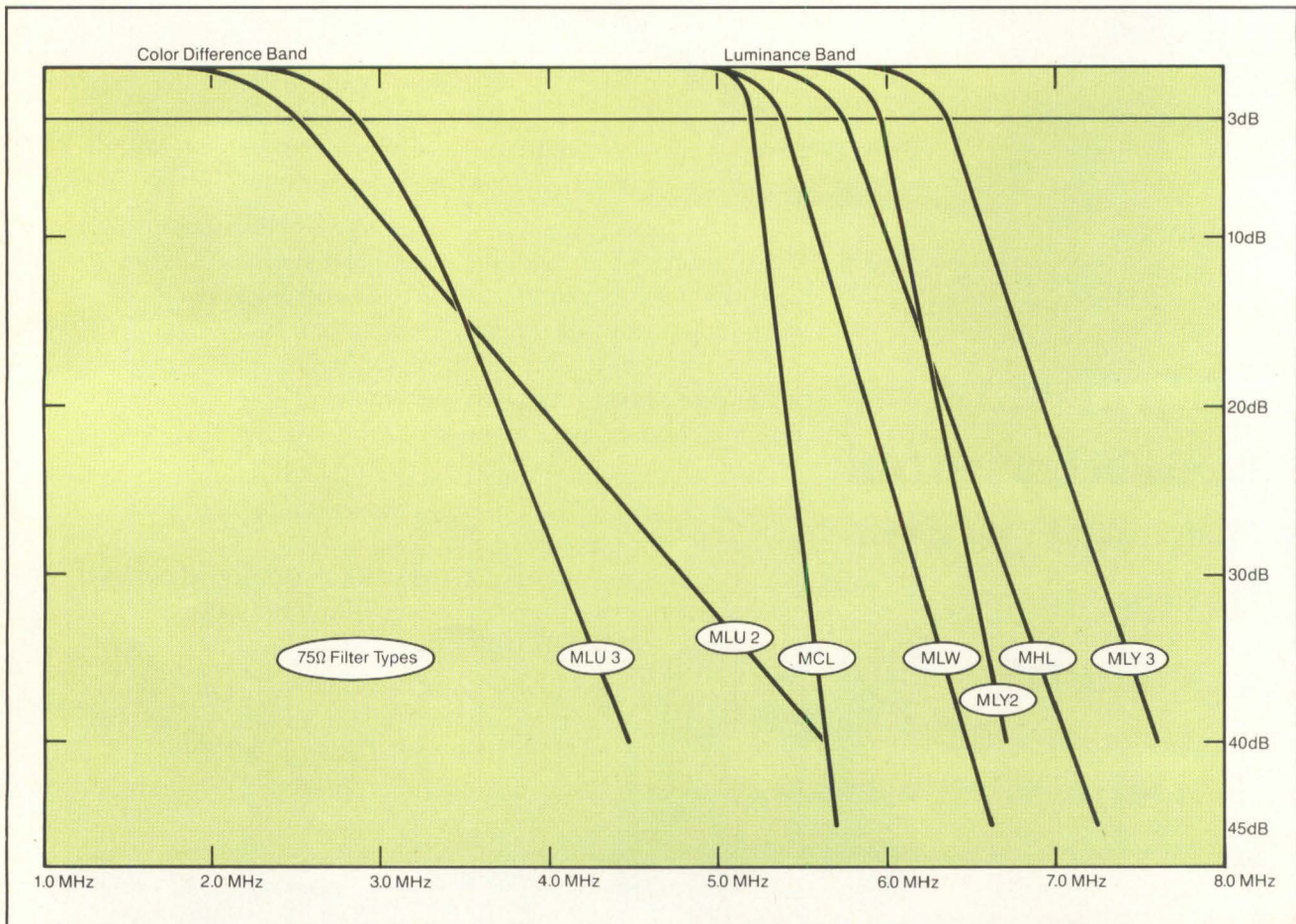


Figure 6: Video filter parameters in the color difference and luminance bands.

INTRODUCING WORKCELL SUPER-VISION.



THE S512: THE NEXT GENERATION WORKCELL / VISION ARCHITECTURE.

Now you can control; multiple high resolution machine vision systems, multiple robots and machines from a common database, or all of the above, simultaneously. The IRI S512 Supervision System makes it all possible.

The S512 is a flexible multi-processor workcell supervisor with architecture that opens up a totally new control performance range. Now multiple high resolution color machine vision systems (512 x 512 pixels) can be configured to our S512. It's our 20 megabyte-per-second multi-processor workcell supervision system that provides concurrent factory control, database management, multi-user access and coordination of robot vision, manipulators, machine tools, and other processes—in real-time.

See us at:

**Electronic Imaging in Boston,
October 8-10, booth 1528**

**Nepcon Northwest in San Mateo,
October 8-10, booth 211**

The S512 is a tightly-coupled multicomputer system, that acquires more than 250 million pixels per second and processes at a maximum rate of 1200 million arithmetic operations per second.

The master-system provides you with a real-time UNIX program development environment, performs data base management, and supervises the subsystems that function under their own specialized operating system. Both the master and subsystems are multiprocessor architectures designed to communicate through shared-memory via an ultra-fast 20 megabyte-per-second arbitrated memory bus.

The result? The S512 Supervision System is the world's fastest, most powerful, expandable, configurable, cost-effective workcell supervision system available today. And, it's ready to plug into your factory control world. For more information, call: Richard Carroll, V.P. Sales (619) 438-4424. International Robomation/Intelligence, 2281 Las Palmas Drive, Carlsbad, CA 92008.



THE BEST VISION INDUSTRY HAS EVER SEEN.

Circle 54 on Reader Inquiry Card

Personal Computers Programmable Controllers

by Brita Meng, Technical Editor

Factory automation is no longer debatable for manufacturing companies. Production efficiency and quality control depend upon it. The migration of the personal computer from the office to the factory floor raises new questions for systems integrators designing industrial computer systems.

In the past, the programmable controller was the control device of choice. But the recent industrial hardening of the personal computer allows it to be placed in a factory environment, giving each station the power of a small minicomputer. At the same time, the programmable controller has evolved from a fixed-scan computer replacing relays, timers and counters in digital logic control systems to a complex computing system. The scope of the two devices has broadened to the point that an overlap in features exists. This seeming convergence of capabilities makes the choice between the programmable controller and the personal computer for a control application difficult.

Some experts in factory automation predicted a quick demise for programmable controllers with the advent of personal computers in the factory. That scenario has not yet come to pass—and most industrial systems integrators believe it never will. The programmable controller still remains one of the major components of factory floor automation. According to Mike Issim, product manager at Hewlett-Packard's Data Systems Division (Cupertino, CA), the main reasons for this is that the programmable controller was designed by factory people for that environment and that it is a tried and proven piece of equipment.

A programmable controller is essentially a solid state control system consisting of a central processor, I/O interface modules (usually 120V ac type), some type of programming device and memory. The memory, which is user-programmable, stores instructions to implement specific functions such as I/O control logic, timing, counting and arithmetic and data manipulation.

The system architecture of programmable controllers is especially optimized for real-time and sequential control. As a result, most respond within milliseconds to any condition changes in their realm of control. Because controllers are programmed for bit decisions, as opposed to functioning on a word-by-word basis, they enable quick response time. On the factory line, where one machine can halt the entire manufacturing process, responsiveness in a control device is as essential as dependability and ruggedness.

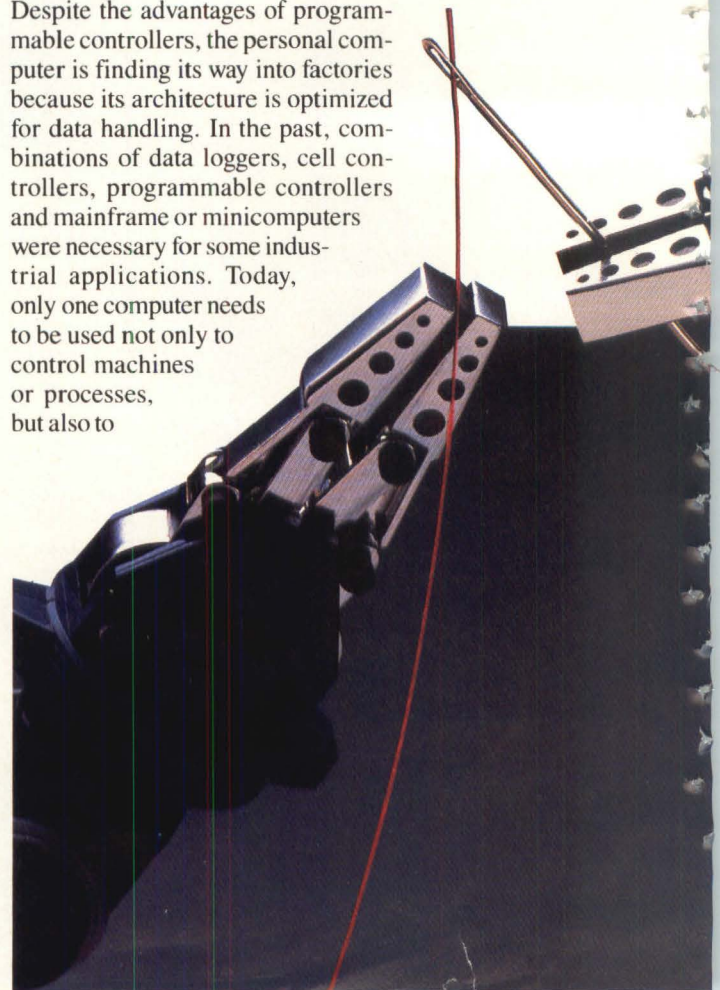
Programmable controllers are also designed to function re-

liably in harsh factory environments. They offer immunity to noise and electrical variations such as voltage spikes. In a proper NEMA enclosure, they can withstand oil mists, liquid spills, temperatures, humidity and mechanical vibrations. Furthermore, controllers retain data integrity despite the line noise caused by the sudden start and stop of controlled machines and processes.

Most importantly, plant and maintenance personnel are familiar with programmable controllers because they have been in use since the late 1960s. They are comfortable with the relay ladder logic programming language. And the modularity of a programmable controller allows it to be repaired on a card-by-card, or even a module-by-module, basis avoiding long-term mass shutdowns for maintenance or repair.

Personal Computers Move In

Despite the advantages of programmable controllers, the personal computer is finding its way into factories because its architecture is optimized for data handling. In the past, combinations of data loggers, cell controllers, programmable controllers and mainframe or minicomputers were necessary for some industrial applications. Today, only one computer needs to be used not only to control machines or processes, but also to



Get Tough; Get Smart

reduce and log data and to communicate with other parts of the factory. Combined with the available computing horsepower of personal computers, this may represent tremendous cost savings to industrial systems integrators.

For example, a personal computer may allow data acquisition and control functions to be executed on the factory floor. A variety of I/O cards are available from a number of companies, including Analog Devices (Norwood, MA), Metrabyte (Stoughton, MA) and Data Translation (Marlboro, MA). Interfacing directly to the system bus, these can accept in the range of 16 differential analog inputs to 32 single-ended analog inputs, 2 analog outputs, 8 digital inputs, 8 digital outputs and 2 channels to measure frequency.

High-level language programming helps in the development

of complex manufacturing supervision programs, obviating the need for specialized development stations. ScreenLink Development software from Industrial Data Terminals (Westerville, OH), which is written in C, allows plant personnel to develop and to dynamically link industrial control color graphics. Software such as ON-SPEC by Heuristics (Sacramento, CA) provides color graphics, alarm reports, word processing, spreadsheets and statistical process control. And as computer-integrated manufacturing (CIM) becomes a reality, the networking capabilities of a personal computer are increasingly important for tying together the computers in the factory and in the offices.

Moving a personal computer to the fac-

tory floor requires ruggedization to withstand the harsher environment. Several industrially hardened personal computers are available, and

other computers may also be adapted to the environment. For example, the MicroVAX II from Digital Equipment Corp. (DEC) (Maynard, MA) is making a transition to the factory floor. DEC manufactures a rack-mounted version; Monolithic Systems (Englewood, CO) recently announced its industrial Q-Bus-based enclosure for that computer. However, the most visible computers are those from IBM (Boca Raton, FL). Even programmable controller manufacturers such as Allen-Bradley (Highland Heights, OH) and General Electric (Charlottesville, VA) are now offering their own lines of IBM-manufactured industrial computers.

The IBM 5531 industrial computer is a software-compatible, industrialized version of the PC/XT. Specified to operate from 4°C to 46.1°C, it can endure humidity from 8% to 80%, non-condensing. It is protected against 2500V ac power line transients lasting as long as 16 msec and operates from 104V to 127V ac with a frequency range from 57 Hz to 63 Hz. In addition, the system includes a filter and cooling fan, thermal sensor and shutdown system and internal retainer bar to prevent dislocation of plug-in cards due to vibrations. The keyboard is protected by a mylar membrane, and there is a plastic cover over the CRT screen and a locking door for the disk drives. A floor-standing, industrialized version of the PC/AT, called the 7531, is also available from IBM. The 7532 is a rack-mounted version of the 7531.

Even though the 5531 and the 7531 are called industrial computers, most system integrators believe that they are simply not hardened enough and can only be placed in a semihostile environment. Reliability may still be a problem. For example, the rack enclosure for the 7532 is not a NEMA cabinet. It may take distributed intelligence or redundant units on the factory floor to guard against total system failure. Disk drives are a main source of concern because of their delicate nature, although few companies, if any, have as yet experienced disk failures on the factory floor. And floppy disk media do not take well to dust, grit and oil.

These concerns have led to other integration options for personal computers. According to Ron Mazza, vice president of marketing at Faraday Electronics (Sunnyvale, CA), the open architecture PC bus and the availability of IBM PC-compatible



Figure 1: The GENIUS I/O System from General Electric consists of an I/O block, bus controller module and hand-held monitor. Aimed at applications requiring 100 or more I/O points, it can be placed up to 2000 feet from the programmable controller.

Programmable controllers and personal computers will help sew together all elements of a computer integrated manufacturing system, such as robots. Photo courtesy Allen-Bradley.

single board computers have created new possibilities for industrial systems. An alternative to S-100 and STD buses, PC bus boards enable users to tailor their system to their functional needs and environmental qualifications, while taking advantage of the I/O cards, software and flexibility of a personal computer. The AT bus, in turn, now appears to be an alternative to the VMEbus, Q-Bus and Multibus I for applications needing higher throughput and calculation capability.

Advanced Systems Design (Cambridge, MA) uses the single board computer on the PC bus as a diagnostic and control processor within a Fourier Transform Infrared Analyzer for continuous monitoring and control. The processor hosts a supervisory program which performs data flow control, floating point processor control, user interface control, database management and systems diagnostics. A robotic controller product from Adaptive Intelligence (Milpitas, CA) embeds the single board computer in the company's enclosure and allows robot movement manipulation by either teach pendant or keyboard motion control parameters.

Other companies have taken to configuring industrial personal computers specifically with harsh environments and placement in mind. One example is Amdex Corp.'s (Andover, MA) RPC-50 industrial microcomputer, an IBM PC-compatible computer which can be used for machine control. Built on a ten-slot motherboard, the RPC-50 uses three slots for the CPU, RAM and mass memory, leaving seven for peripheral cards. Its temperature and humidity range is wider than the 5531 and its voltage and frequency range is also better. The RPC-50 has no moving parts, battery backup can be provided in case of power loss, and its memory can be either EPROM, DRAM or bubble.

The shortage of I/O expansion slots in the IBM personal computer is a problem. Eight expansion slots are contained in the 5531. Of those, three are required for standard equipment: one



Figure 2: The 7531 industrial computer from IBM is a factory hardened version of its PC/AT. Standard equipment includes 512 Kbytes of memory, a 1.2 Mbyte diskette drive and seven available I/O expansion slots.



Figure 3: The Allen-Bradley PLC-3 is one of the largest programmable controller systems available, controlling up to 8196 I/O points with up to 1.92 Mbytes of memory. Basic programming provides computer functions like floating point math and report generation.

for the fixed disk controller, one for the floppy disk controller and one for the serial I/O. A color monitor and printer controller uses another slot. Therefore, at most four expansion slots exist for other uses in a standard PC/XT configuration.

There are ways to solve this predicament. IBM's expansion unit for its personal computers comes with a 10 Mbyte fixed disk and eight expansion slots. After combining a personal computer with this unit, an IBM PC has six slots for other interface cards and an XT, nine slots for other interface cards. The drawback to using the expansion box is that its connecting signal cable can be only one meter long.

Converting the PC bus I/O signals to those compatible with the VME, STD or Multibus may allow more flexibility in the placement and more choices in the variety of interface cards. The availability of specialized function boards for the PC bus or AT bus, such as stepper motor controllers and isolated thermocouple input boards, is limited. However, many vendors offer industrialized cages or enclosures for cards based on STD, VME or Multibus. Datel (Mansfield, MA) recently introduced the ST-702, an intelligent, isolated, thermocouple processing A/D board for the Multibus. Front-end subsystems for larger applications can be connected to personal computers by an IEEE-488, RS-232 serial interface or other high-speed specialized links.

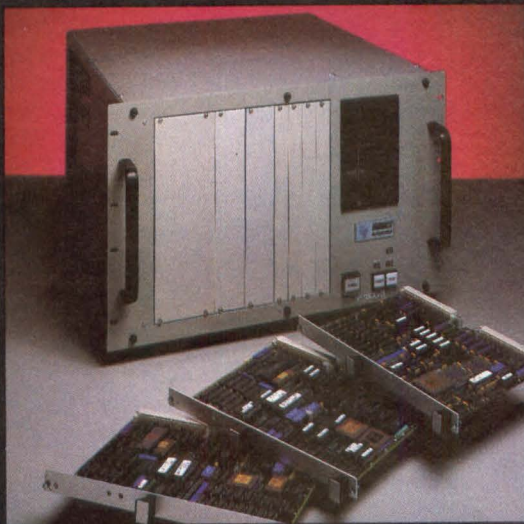
Operating systems for personal computers have also been a source of concern to industrial systems integrators. A multitasking environment can be crucial. Obtaining a process status printout on a personal computer may require that it stop running the process until the printer is finished, possibly resulting in an overlooked alarm condition. Although Digital Research Inc. (Monterey, CA) is now marketing packages of concurrent DOS and concurrent CP/M that allow up to four simultaneous tasks on a personal computer, these packages require an increase in computer memory. And monitoring more channels with a personal computer, coupled with user interface and graphics func-

THE ADVANCED MULTIPROCESSING MULTIPROCESSING MULTIPROCESSING MULTIPROCESSING ENVIRONMENT

Ironics, the high performance leader in VMEbus, announces the availability of the next generation of VMEbus CPU modules. Optimized for multiprocessing, these modules implement a standard set of hardware and software features that take full advantage of the VMEbus multimaster capabilities. For the first time, efficient interprocessor communication and synchronized data exchange make true high speed multiprocessing a reality. Features such as VMXbus interfaces, interrupters and interrupt handlers, fast dual-ported static and dynamic RAM arrays, and mailbox interrupts harness the raw power of 68010 and 68020 MPUs functioning in parallel. This power can be configured to match the most demanding applications.

The Ironics **Performer Series™ UNIX™ Systems** are especially well suited to multi-processor environments. Since all system functions reside on one VMEbus board, UNIX-related bus traffic is completely eliminated. As a debugging tool, UNIX may be used to initiate, monitor, and control the function of a target board set residing on the same backplane. It does this without impacting the target system's use of the bus. UNIX may also function as a front end for multiple processor boards running independent real-time tasks, all under the control and coordination of UNIX.

If you would like to know more about how the Ironics approach to multiprocessing can be used on your next project, write or call for the Ironics **Multiprocessing Technical Brief**. Ironics Incorporated, 798 Cascadilla Street, Ithaca, NY 14850, Telephone (607) 277-4060.



Performer Series is a trademark of Ironics Incorporated. UNIX is a trademark of AT&T Bell Laboratories.



tions, degrades its response time to seconds despite this facility.

Direct factory control may also need real-time response by a computer, in addition to multitasking capabilities. Aside from custom-developed software, operating systems available which meet these specifications are Intel's (Hillsboro, OR) iRMX-86 and iRMX-286, Hunter and Ready's (Palo Alto, CA) VRTX and Industrial Programming Inc.'s (Jericho, NY) MTOS.

One solution to these problems is adding extra capabilities to a personal computer. The MACSYM 120 workstation from Analog Devices is based on the 5531 and includes concurrent CP/M, an 8087 math coprocessor and a multitasking programming language. Another solution may be the addition of intelligent front-end subsystems which are able to preprocess collected data before sending it to a personal computer.

Intelligent Programmable Controllers

Although personal computers have become industrialized and capable of distributed control and multitasking, programmable controllers are now able to perform some of the control and data processing functions which, in the past, required a minicomputer. The primary reason is the addition of more memory in the main processor, as much as 200K in some cases. In addition to adding computing horsepower, larger memory systems allow more extensive machine diagnostics.

The availability of more specialized I/O cards for programmable controllers has also extended their use in industrial computer systems. General Electric recently introduced its GENIUS I/O system for its Series Six programmable controllers. The product, which has a built-in intelligent power switch and intelligent input modules to check sensors, is able to continuously monitor and identify faults in actuators, wiring circuits and hard-contact sensors.

A programmable controller from Siemens-Allis Automation (Peabody, MA) called the SIMATIC S5-115U allows a user to develop programs using any one of three languages: ladder diagram, statement list and control system flowchart. Translating the same program back and forth from one language to another is accomplished by hitting a function key. For factory



Figure 4: SIMATIC S5-150U programmable controllers from Siemens are installed in this continuous casting plant to control mold adjustment, the dummy bar and cutting length measurement.

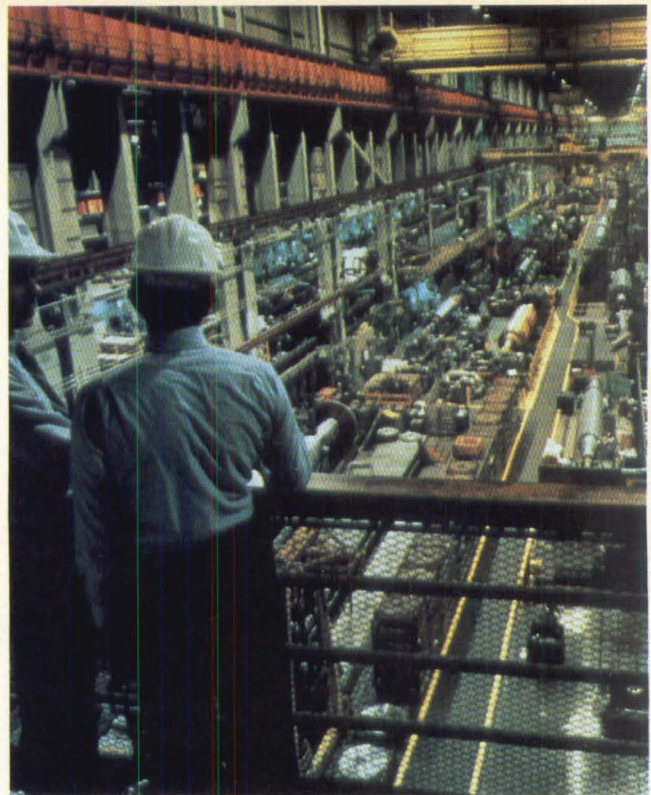


Figure 5: At General Electric's steam turbine generator facility in Schenectady, NY, 14 Data General computer systems are used for functions ranging from process planning to inventory control.

personnel not wanting to use those languages, programmable controllers can now be programmed in Basic or Fortran by simply inserting an intelligent language card into the controller module, such as the Programmable BASIC module from Texas Instruments (Johnson City, TN).

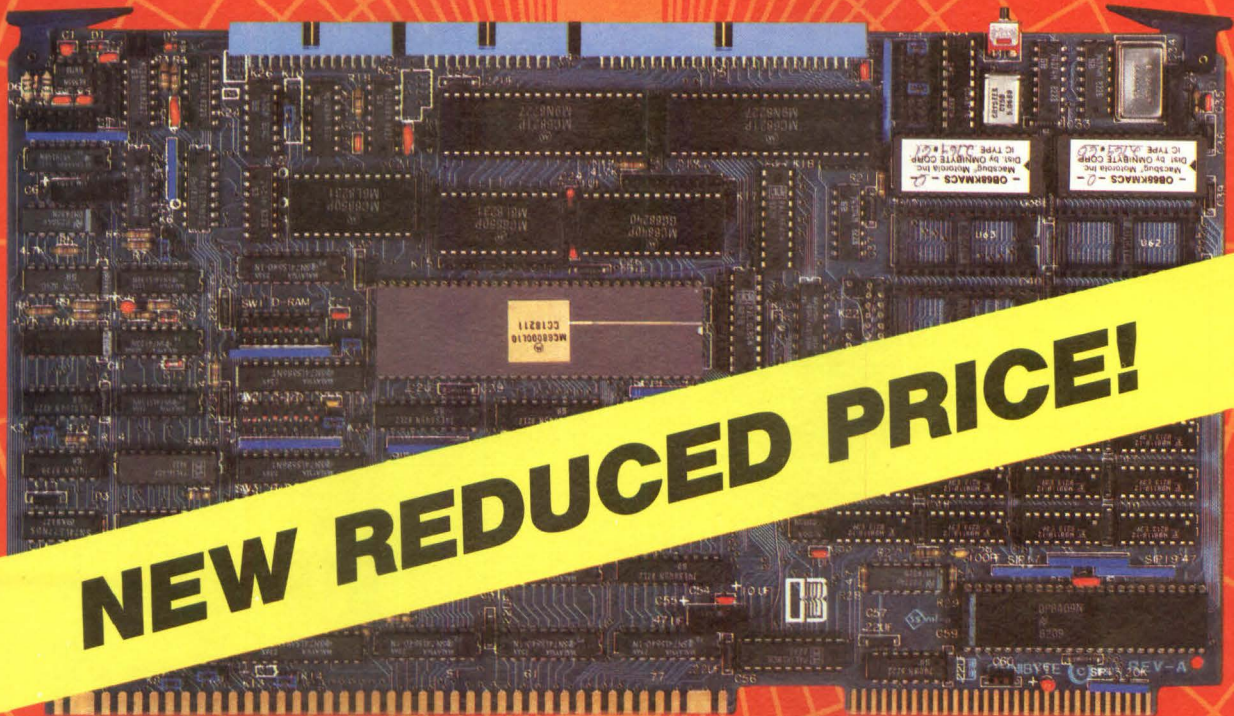
Other available cards enable process engineers to use such ASCII devices line printers, bar code readers and bar code printers with a programmable controller. Servo drives and systems from companies including Gould (Troy, MI), Ferguson Machine Co. (St. Louis, MO), Opcon (Everett, WA) and Allen-Bradley interface with programmable controllers to control robot movement on the floor. Color graphics monitors can also be connected to enable factory floor supervisors to see process statuses in a form similar to a personal computer.

Networking and communications possibilities have also expanded for programmable controllers. Previously, it was difficult for a programmable controller to talk to any device other than a controller from the same manufacturer. Now personal computer interfaces such as RS-232 links are built in to allow programmable controllers to communicate with personal computers.

The formulation and implementation of the General Motors MAP standard should allow all industrial system components to interface. MAP is a broadband token-bus local area network employing standardized communication protocols for each layer of the ISO-OSI model. It is not yet a finished specification, despite the fact many manufacturers already claim full compliance. Even when it is finished, there still may be problems implementing MAP—such as interfaces that are more expensive than some of the devices to be connected. Proprietary networks which number over 200, like Allen-Bradley's Data Highway, TI's TIWAY and Gould's Modway, must be merged to MAP as well.

OMNIBYTE™

Multibus* 68000 Single Board Computer



OB68K1A™

128KB 68000 Multibus SBC priced as low as \$777 each in OEM quantities of 250.

Thanks to the great success you've given our OB68K1A, we have obtained quantity discounts on its components. This, coupled with recent overall price reductions on RAM, peripheral, CPU and other chips allow us to pass these cost savings on to you.

We have been able to do this and still maintain our tough quality and reliability standards. These standards are so stringent that we give you a two year limited warranty—the same warranty you have become accustomed to with Omnibyte board level products. In all the years this board has been manufactured:

- Over 99% of boards manufactured, never return because of product failure!

- Of the less than 1% that have been returned for repair . . . 90% are checked, repaired, tested and sent back within 24-48 hours.

This is proof of Omnibyte's commitment to support you with quality and service! And just look at the advanced features you get with the OB68K1A:

- 10MHz 68000 16/32 BIT CPU
- 32K/128K/512K-bytes of dual-ported zero-wait-state on-board RAM
- Up to 192K-bytes of EPROM
- (2) RS232C serial ports
- (2) 16-BIT parallel ports
- (3) 16-BIT timer/counters
- (7) prioritized-vectored interrupts
- Directly address 16M-bytes.
- IEEE-796 (MULTIBUS)* compatible (MASTER D16 M24 I16 VOL/SLAVE D16 M24)

- Low noise multilayer design
- Omnibyte two year limited warranty
- And more!

SOFTWARE SUPPORT

A variety of software packages are available for the OB68K1A. They range from the option VERSABUG** or MACSBUG** monitor/debuggers to Realtime Executive and Target Operating Systems in silicon.

The OB68K1A has been used successfully in thousands of applications such as: process control, computer typesetting and data acquisition. To learn more about the features of this board—its new low pricing structure and to obtain a free data sheet, call our Marketing Manager, Peter Czuchra today. A detailed technical manual is also available for \$10.00

*A Look at Today . . .
A Vision of Tomorrow*

*Multibus is a trademark of Intel Corp.

**MACSBUG and VERSABUG are trademarks of Motorola, Inc.

©OMNIBYTE CORPORATION

Circle 30



OMNIBYTE CORPORATION
245 W. Roosevelt Road
West Chicago, IL 60185
312/231-6880

Solutions In Harmony

As programmable controllers' applications have expanded from Ford and General Motors factory lines, so too have their capabilities. And as personal computers' applications have grown from the office to the factory floor, their capabilities have done the same. Even though the two devices may be similar in appearance or features, more memory and a man-machine interface does not make a programmable controller a personal computer, nor does ruggedization and real-time operation make a personal computer a programmable controller. Their architectures and the tasks for which they are optimized are just too different for the two to ever be completely interchangeable on the factory floor.

For machine control, discrete manufacturing and batch processing involving either digital sequencing or few recipes, a programmable controller may still be the control device of choice. For testing, laboratory or pilot plants, executive or supervisory control and batch processing requiring either a great deal of manual control or many recipes, a personal computer is probably better.

Cost also plays a part. The dropping price of industrialized personal computers has allowed them to become almost disposable commodities for some customers, who either want a quick payback on the investment or will not use them for vital control functions on the factory floor. Conversely, the higher

price of programmable controllers reflects that device's hardened, proven design.

Most industrial computer system integrators feel that the optimal solution for a control system will probably be a hierarchical partnership which capitalizes on the strengths of both programmable controllers and personal computers. Dan Krause, sales manager at Autologic (Brighton, MI), sees the base level of this structure as including data collection and dedicated control performed within the distributed intelligence of programmable controllers. As a microhost or workstation, personal computers would provide gathering points for data from those programmable controllers, accomplishing scada-type functions, trending and performance optimization calculations. Other integrators foresee the development of systems which can be defined as personal computer-type programmable controllers—a merging of the two technologies.

The increased ruggedness of personal computers and the increased intelligence of programmable controllers allows more flexible industrial systems to be configured in the factory. Used in conjunction with evolving standards for communication networks and application software, integrators may finally be able to wire the factory for productivity and a secure manufacturing future. DD

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful	616
Useful	617
Somewhat Useful	618

Order Your Panel Wired
GUARANTEED
One-Week Delivery!

Augat's turnkey prototype service, QWIKTURN, provides ONE-WEEK turnaround on panels and wiring from a clean database. Just select your panel from our stock or yours and submit your netlist and placement data in electronic form. CAD or CAE WORKSTATION database is acceptable either VIA MODEM or on mag tape or floppy disc.

For other input formats, or additional services such as twisted pair, installation of solder clips and capacitors, engineering changes, etc., there will be a slightly longer turnaround.

Now on our shelf:
VME Bus
Multibus I and II
IBM PC
Plus other Augat standard panels

Call For Details:
Central (713) 495-3100
West (408) 249-8801
East (617) 222-2202



Write for AUGAT "Wiring Services Brochure"

OUR GUARANTEE: ONE-WEEK DELIVERY OR YOU PAY NO PREMIUM!

AUGAT

QWIKTURN
WIRING SERVICES

Multibus and IBM PC are registered trademarks of INTEL Corp. and International Business Machines Corp. respectively

Free catalog of 68000 Multibus* products.

Single-board computers. Unix*-compatible computer systems. Communications boards. Piggyback I/O modules. Software products and support.

Phone now 1-800-221-6458.

In California call (415) 680-7722 or 1-800-328-9900.

SBE, Inc., 2400 Bisso Lane, Concord, CA 94520.



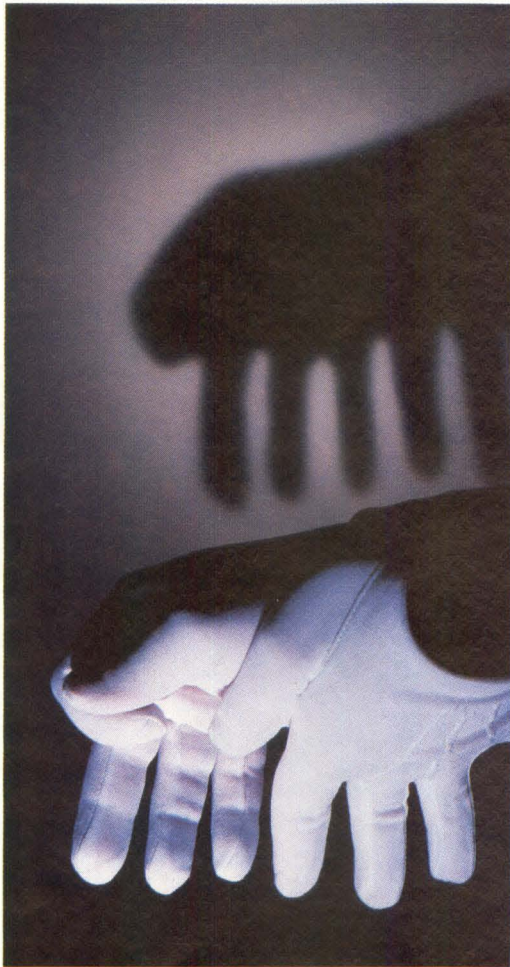
Your partner in computer boards and systems.

*Multibus is a trademark of Intel. Unix is a trademark of Bell Laboratories.

Circle 33

Circle 58

ME AND MY SHADOW.



The User-Configurable Shadow RAM from Mostek.

Take a moment to consider this. Mostek has a new low-cost answer to your low-density nonvolatile memory needs. It's the user-configurable MK4701 128 x 8 Shadow RAM.

Being user-configurable, it lets you decide which characteristics to give it. Like automatic storage. Or on-command storage. It even lets you adjust its Vcc trip point.

And being a single-chip solution, the MK4701 will fit a standard 24-pin byte-wide socket — even in an existing design. Which not only makes it easy to work with, but also does away with additional circuitry since it interfaces directly with your system's microprocessor.

What's more, its Vcc sensing detects power outages, and write protects the MK4701 to prevent data corruption from spurious cycles. Its automatic store option will then store all of its data in bulk — which avoids separate signaling to the nonvolatile store pin.

So, for more information on the Shadow RAM that puts others in the shade, contact Mostek Corp., 1215 W. Crosby Road, MS2218, Carrollton, TX 75006, (214) 466-7479. In Europe, (32) 02/673.99.60. In Japan, 03/496-4221. In the Far East (Hong Kong), 5.681.157-9.



We earned our reputation on the 6 o'clock news!



It took real innovation to earn our first Emmy for technical excellence in broadcast television. And a proven track record to record America's first manned space flight.

Which explains, perhaps, why Ikegami is rapidly becoming the first name in electronic imaging components.

Today, you'll find us wherever award-winning performance counts.

Providing original equipment manu-

facturers with the precision components demanded by a Space Age environment. With the same reliability that keeps the 6 o'clock news in focus night after night.

Outer space or inner space, you'll find us wherever products and their end users demand proven performers.

We're Ikegami. We can make a difference in how you do business. And what your business can do for you.

We'll stake our reputation on it.



A NAME TO WATCH
Ikegami[®]

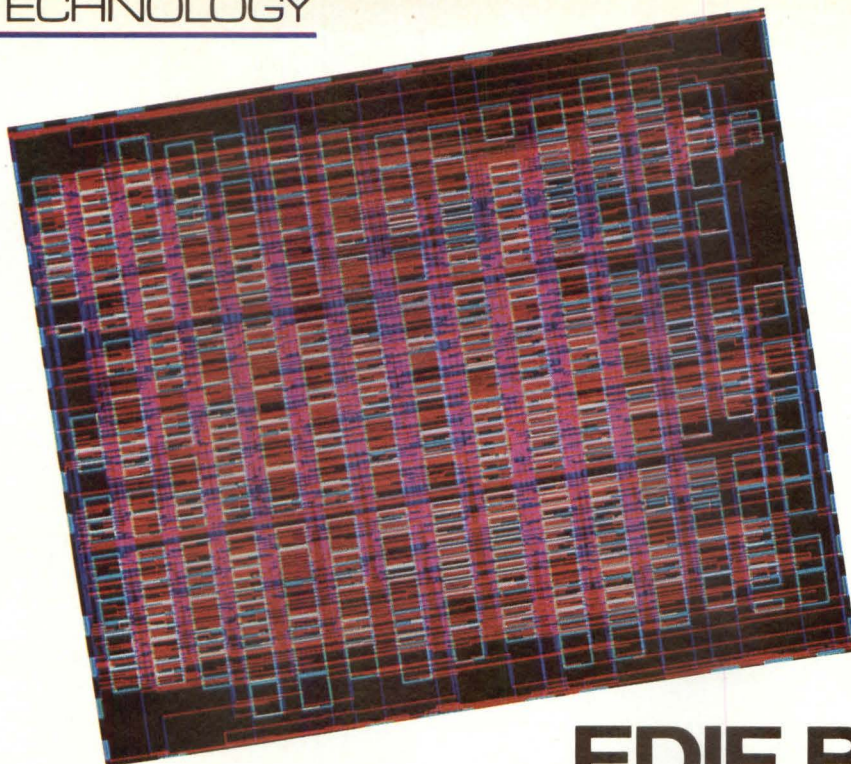
Ikegami Electronics (U.S.A.), Inc., 37 Brook Avenue, Maywood, NJ 07607 (201) 368-9171

West Coast: (213) 534-0050

Midwest: (312) 834-9774

Southwest: (214) 233-2844

Southeast: (813) 884-2046



EDIF Breaks CAE/CAD Compatibility Barrier

by Lisa Hampton, Semicustom Product Marketing Manager, Mentor Graphics

Workstations are becoming an ideal environment for semicustom IC design. What started as a tool to generate netlists for the IC vendor's mainframe CAD system has evolved into a powerful standalone design system. Workstations support almost the entire semicustom IC design cycle, including schematic entry, simulation, layout and back annotation of wire delay information for resimulation.

Workstation vendors would like to offer their customers as many different gate array libraries as possible. Similarly, gate array vendors would like to offer their libraries on as many

EDIF allows designers to select from a wider range of CAE/CAD tools and semiconductor vendors.

workstations as possible. For gate array vendors, maintaining several different databases of the same data at the same level is a difficult task. For the workstation vendors, writing specialized interfaces for each gate array vendor is not feasible. The solution is EDIF—Electronic Design Interchange Format—a new standard format for the transmission of design data.

An industry standard such as EDIF has several benefits. Semiconductor manufacturers need to maintain only one data-

base and one set of translation utilities to support all CAE/CAD vendors. This is a significant aid to these vendors because compatibility is maintained with many foundries and other design systems, with minimal investment in software development. CAE/CAD makers need to write only one set of translation utilities to support a wide range of semiconductor vendors. As a result, system designers can choose from a much wider range of semicustom libraries and CAE/CAD systems. Foundries can accept a customer's circuit regardless of the CAE/CAD system on which it is designed.

Most semiconductor companies have their own representation of design data. Some of the formats are nonproprietary, but none are considered an industry standard. Also, many of these formats are narrowly focused. They address a particular type of design data such as mask artwork, simulation models or netlist information.

What Is EDIF?

EDIF is the result of a cooperative development effort between several semiconductor and CAE/CAD companies. The steering committee consists of representatives from Daisy Systems, Mentor Graphics, Motorola, National Semiconductor, Tektronix, Texas Instruments and the University of California at Berkeley. Representatives from these organizations began meeting in 1983 to start development of a common interchange format. Several technical subcommittees, comprised of representatives from many companies, have been formed to address specific portions of design description. In January 1985, the first version of the EDIF specification was released. It supports both

IC and printed circuit board design and describes the full spectrum, from the symbol representing a macro to the physical layout.

EDIF, whose files are single data structures, is based on a LISP-like syntax in which data is represented as symbolic expressions. Numerous defined data constructs are available to facilitate the description of component libraries (Figure 1). As it becomes necessary to describe new features, the format can be equipped with additional data constructs, and this can be done without obsoleting the old format or databases. Other strong points of EDIF include ease of parsing, transportability to different machines and fabrication technology independence.

The building blocks of EDIF consist of primitive elements such as signals, ports, strings, numbers and identifiers. Complex structures are formed from parenthesized lists that are made up of primitive data or other lists. The first position of each list is devoted to a key word which gives meaning to the positioning of subsequent elements in the list. New key words can be added and lists may be lengthened or shortened without changing existing parsers. This makes the format easily extendable since the key words are the controlling elements, not the syntax.

Since humans and machines will be reading and writing EDIF, the format must be concise, yet comprehensible to engineers. EDIF's LISP-like syntax provides a balance between keeping the format compact and retaining legibility. If EDIF memory requirements become a problem in a particular design, the format can be compressed to reduce file size. EDIF descriptions are expressed hierarchically and at the highest level is an abstract representation. As it descends the hierarchy, it becomes more detailed.

EDIF On Workstations

In the past, putting a new set of gate array libraries on a workstation required tremendous effort. Whether done by gate array manufacturers or workstation vendors, the work required a great deal of time to ensure accuracy in the databases. Once gate array manufacturers had offered their databases on one workstation, it was almost as much effort to achieve support for a second workstation. Creating an EDIF database for design libraries requires an initial investment of resources, but once they are created, any workstation that accepts EDIF data can be supported. This gives designers greater flexibility in choosing a workstation.

Writing EDIF translation routines is a task that must be performed by the workstation vendors. This, too, demands an initial investment of resources, but once completed, any gate array library represented in EDIF can be supported on that workstation. As a result, designers can choose from a wider range of gate array technologies.

A more subtle advantage of using a standard interchange format is data integrity. Now that gate array manufacturers have to maintain only one database to support all workstations, the maintenance problem is much easier. Making sure that libraries are kept current also implies that all workstations supported by that database have the latest revision of data.

The Mentor-Motorola Connection

The workstation can be used for various portions of the design cycle. Figure 2 illustrates the gate array design stream and the

(Cell NAND2

```
(View Symbolic Logic
  (Interface
    (Define INPUT PORT (multiple ab))
    (Define OUTPUT PORT z)
    (Body (FigureGroup Schematic Symbol ... )))
  (Contents
    (Instance NAND2Primitive Logic N2)))

(View MaskLayout physical
  (Interface
    (Define INPUT PORT (multiple ab))
    (Define OUTPUT PORT z)
    (Define INOUT PORT (multiple VCC VDD))
    (Body (FigureGroup MetalBlockage ... )))
  (Contents
    (FigureGroup Metal (Polygon ...) ...)))

(View Document
  (Contents
    (section "NAND2—Its uses" "The NAND2 ...."))))
```

Figure 1: EDIF is a hierarchically based standard with a syntax similar to the LISP programming language. Shown is an example (found in the EDIF specification manual) of how EDIF might express a two-input NAND gate cell. The representation consists of the logic model, schematic symbol, detailed layout and layout abstraction for placement and routing.

various points of interface. EDIF was chosen as the interchange format between Mentor Graphics (Beaverton, OR) and Motorola (Phoenix, AZ) to implement the gate array design methodology.

The design stream has been divided into three possibilities: A, B and C. In stream A, the IC vendor supplies only a symbol library for the workstation. These symbols contain the information necessary to generate a netlist for the IC vendor. With this netlist, the IC vendor performs simulation and, subsequently, placement and routing.

In design stream B, the IC vendor supplies the simulation models and the symbol library. The designer enters the schematic and simulates the design. After the IC vendor completes the layout, actual wiring delays are extracted and back annotated into the simulation models. At this point, the circuit is resimulated and the test vectors are refined to reflect the more accurate simulation data.

In design stream C, the designer enters the schematic, simulates the design, performs placement and routing and returns the final layout to the IC vendor. Since the layout is done on the workstation, the post-layout delay data is extracted on the workstation and immediately back annotated to the simulation models. The test vectors are generated from the final simulation and submitted with the layout and netlist to the IC vendor.

Within Motorola's CAE/CAD system is the technology data that describes the firm's gate arrays. In addition, Motorola's translator programs convert its internal technology files to EDIF. To move this EDIF data onto Mentor's workstations, Mentor developed three translation programs that compile the data into its internal database format.

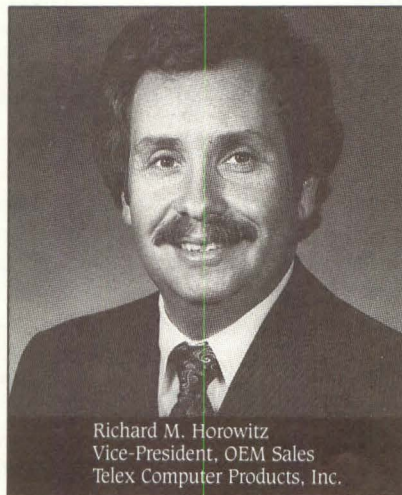
The first program, EDIF2SYM, translates Motorola's component information to Mentor's symbol library. Motorola maintains the EDIF file that contains the information necessary for generating the graphical symbols used on various workstations. In addition to the graphical data, this EDIF file contains component names and pin types for generating the design netlist from the schematic.

OEM Computer Product Buyers

“The Invitational Computer Conferences bring to you the latest high-tech information you need to hear, and the major OEM products you need to see. We’ll be there!”

And you’ll find other top OEM manufacturers, such as NCR, Fujitsu, Xebec, Lear Siegler, Siemens and IBM, to name but a few.

Celebrating its 15th year, the “OEM Only” ICCs bring you, the volume buying decision makers, together with the key suppliers of computer and peripheral products. The ICCs also bring you a full day of high-tech seminars, explaining the latest in computer product technologies and what they mean to you, the systems design engineer. As an invited guest, there is no charge to attend the seminars or product displays.



Richard M. Horowitz
Vice-President, OEM Sales
Telex Computer Products, Inc.

The ICCs, a series of eleven, one-day regional conferences are convenient to where you work. The small, exclusive setting makes it easy for you to meet potential suppliers one-on-one.

Hear what the OEM manufacturers have to say, learn about new technologies, and remember, you may attend “by invitation only.”

1985/86 U.S. ICC Locations

Sept. 5, 1985	Newton/Boston, MA
Sept. 23, 1985	Atlanta, GA
Oct. 8, 1985	Westlake Village, CA
Oct. 22, 1985	Minneapolis, MN
Nov. 7, 1985	Gaithersburg, MD (D.C. area)
Jan. 9, 1986	Irvine, CA
Jan. 28, 1986	Austin, TX
Jan. 30, 1986	Dallas, TX
Feb. 27, 1986	Ft. Lauderdale, FL
Mar. 18, 1986	San Jose, CA
Apr. 2, 1986	Nashua, NH

Call your local OEM supplier for your invitation or fill out the coupon and mail to:

B. J. Johnson & Associates, Inc.
3151 Airway Avenue, #C-2
Costa Mesa, CA 92626
Phone: (714) 957-0171
Telex: 5101002189 BJ JOHN



Yes, I need an invitation to your “OEM Only” ICC. The nearest ICC to me is: _____

I buy in volume:

- Computers
- Disk/Tape Drives
- Controllers/Interfaces
- Terminals/Graphic Displays
- Software
- Printers
- Memory Boards
- Modems/Multiplexers
- Power Supplies

Name _____

Title _____

Company/Division _____

Address _____

City _____ State _____ Zip _____

Mail To: B. J. Johnson & Associates, Inc., 3151 Airway Avenue, #C-2, Costa Mesa, CA 92626
Phone: (714) 957-0171 Telex: 5101002189 BJ JOHN

The second program, EDIF2SIM, translates Motorola's simulation model data into Mentor's format. Motorola maintains the EDIF file that contains simulator primitives and timing information to describe each macrocell. This information is used by the EDIF2SIM program to create Mentor Graphics Quickparts. The Quickparts library consists of component models that require up to 10 times less memory space than those in traditional libraries. This results in a fivefold increase in design throughput.

The third program, EDIF2PHY, converts Motorola's physical database to Mentor's physical database. Physical data describes the size, shape and location of such elements as silicon, metal and polysilicon. Motorola maintains the EDIF physical data file describing the uncommitted array and macrocells. Describing the uncommitted chip requires defining routing blockage information, the macro placement sites, and design rules for adding wiring and vias. Pin names, pin locations, pin swapping information and routing blockage data is needed to describe each macro.

Currently, the EDIF design kits and updates are distributed on floppy disks. In the future, engineers will be able to call the Motorola CAD system and receive all the design data as well as incremental updates via modem. To ensure that users always have the most current design data, it will be compiled on the workstation and the necessary files automatically updated. There will no longer be the time lag in receiving the new data that is inherent in creating and distributing the updates on floppy disks.

How Designers Use EDIF

Once all of the technology information has been transferred to the workstation, design work proceeds as normal. All of the schematic capture, simulation and layout programs function just as they would with any other technology resident on the workstation. It is not necessary to learn a new way to use familiar CAE/CAD programs.

One difference, however, is the way in which design data goes back to Motorola. EDIF is used as the interchange format between the two firms. Four programs are used to transfer data from the Mentor workstation to Motorola: EDIFNET, VEC2EDIF, ADD-DELAY and PHY2EDIF.

EDIFNET converts Mentor's design file to an EDIF netlist, which is a subset of EDIF describing the design's connectivity. Also in the netlist is any preplacement data for internal and I/O macros. Macro preplacement is particularly valuable if the design must conform to a predefined pinout. Pin assignment is handled by Mentor's PKG_DEF program which allows the designer to assign I/O signals directly to pins on the package before layout occurs.

VEC2EDIF translates Mentor's simulation output (Quicksim) to EDIF. In addition to converting the test vectors to EDIF, Motorola provides a program that configures Quicksim to generate Motorola's test vector output. An EDIF file containing all the test vector information is transferred to Motorola where it is converted into the necessary format to drive the automatic test equipment.

Before the test vectors are transferred to Motorola's CAE/CAD system, the post-layout delay data must be added to the simulation design file. Motorola supplies the EDIF file containing the actual capacitance values of each signal. The EDIF file

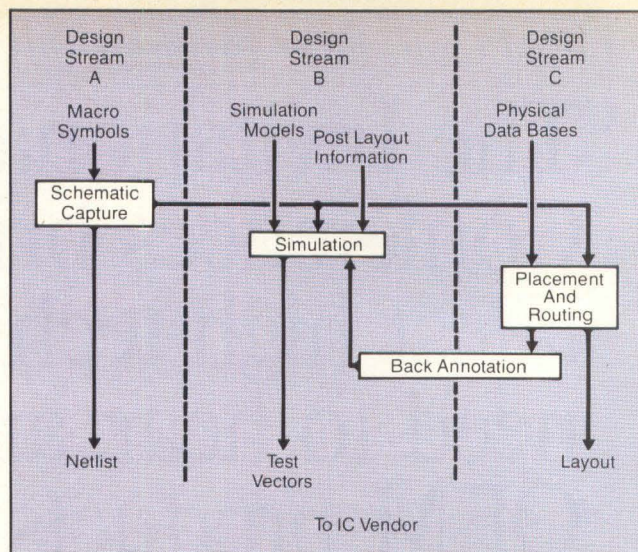


Figure 2: When designing a gate array on a workstation, engineers may choose to complete selected stages of the project on the workstation. Remaining tasks would be completed on the IC vendor's CAE/CAD system by the designer or the IC supplier. The diagram depicts the alternative points of interface between the designer and IC vendor. In the Design Stream C, the IC maker's only task is to fabricate the array.

is transferred to the workstation and the ADD_DELAY program is used to back annotate the delay values into the design file. This is the same program that adds predicted capacitance before layout. It is also used to model operating voltage and temperature delay, process delay and fan-out delay. All of the various conditions can be chosen independently or in conjunction with each other for modeling delay values. Delay values are modified by setting the desired condition at execution time.

When layout is performed on the workstation, the layout information is converted to EDIF using PHY2EDIF. The EDIF file contains the locations of all macros in the design and the paths describing the array's routing. And because the file does not include all of the internal macro or base array information, it does not consume large amounts of memory. To generate the masks for fabricating the device, this data is then merged on Motorola's CAE/CAD system with the macro's internal data and the base array.

EDIF's advantages are clear. Before the standard was developed, gate array vendors were forced to maintain different symbol, simulation and physical databases for each CAE/CAD system supported. Now, these vendors maintain one copy of symbol, simulation and physical databases.

Prior to EDIF's introduction, CAE vendor had to write different interface programs for each gate array vendor. But with a standard interchange format, CAE vendors maintain a single set of interface programs.

Finally, designers benefit from the EDIF standard since it allows them to select from a wider variety of gate array and CAE vendors. Without a common interface standard, designers must wait until the gate array vendor and the workstation vendor develop new libraries. And this is a lengthy process since each new library requires the same resource investment. **DD**

How useful did you find this article? Please circle the appropriate number on the Reader Inquiry Card.

Very Useful 613
Useful 614
Somewhat Useful 615