A CAHNERS PUBLICATION

AUGUST 6, 1987

EDN®

Micropower circuits

Engineering calculators

Digital signal processing

Sequential testing

Technical-article database index

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

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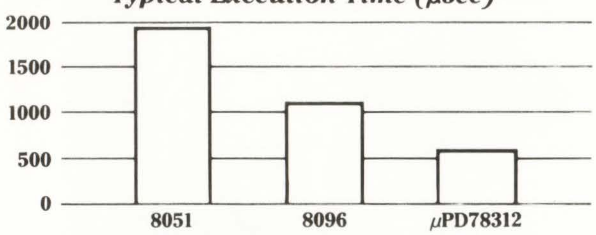

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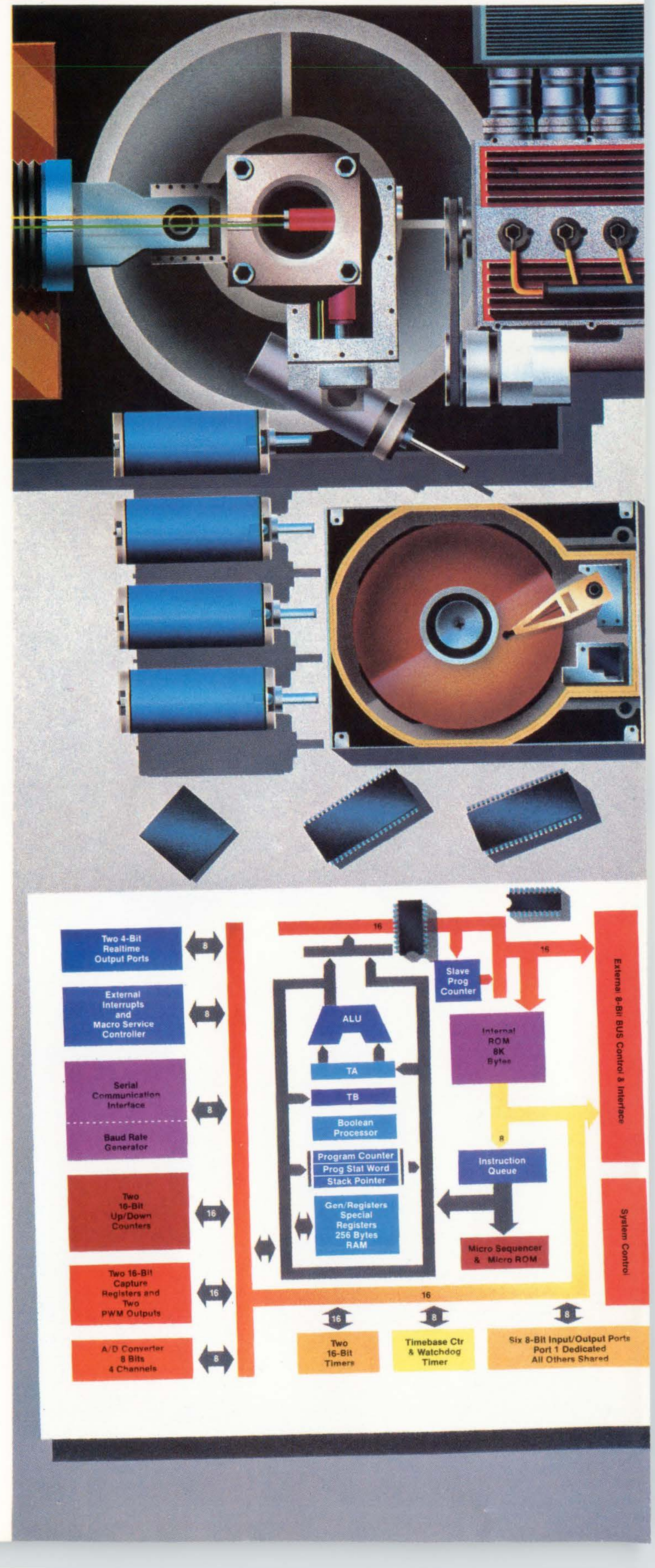

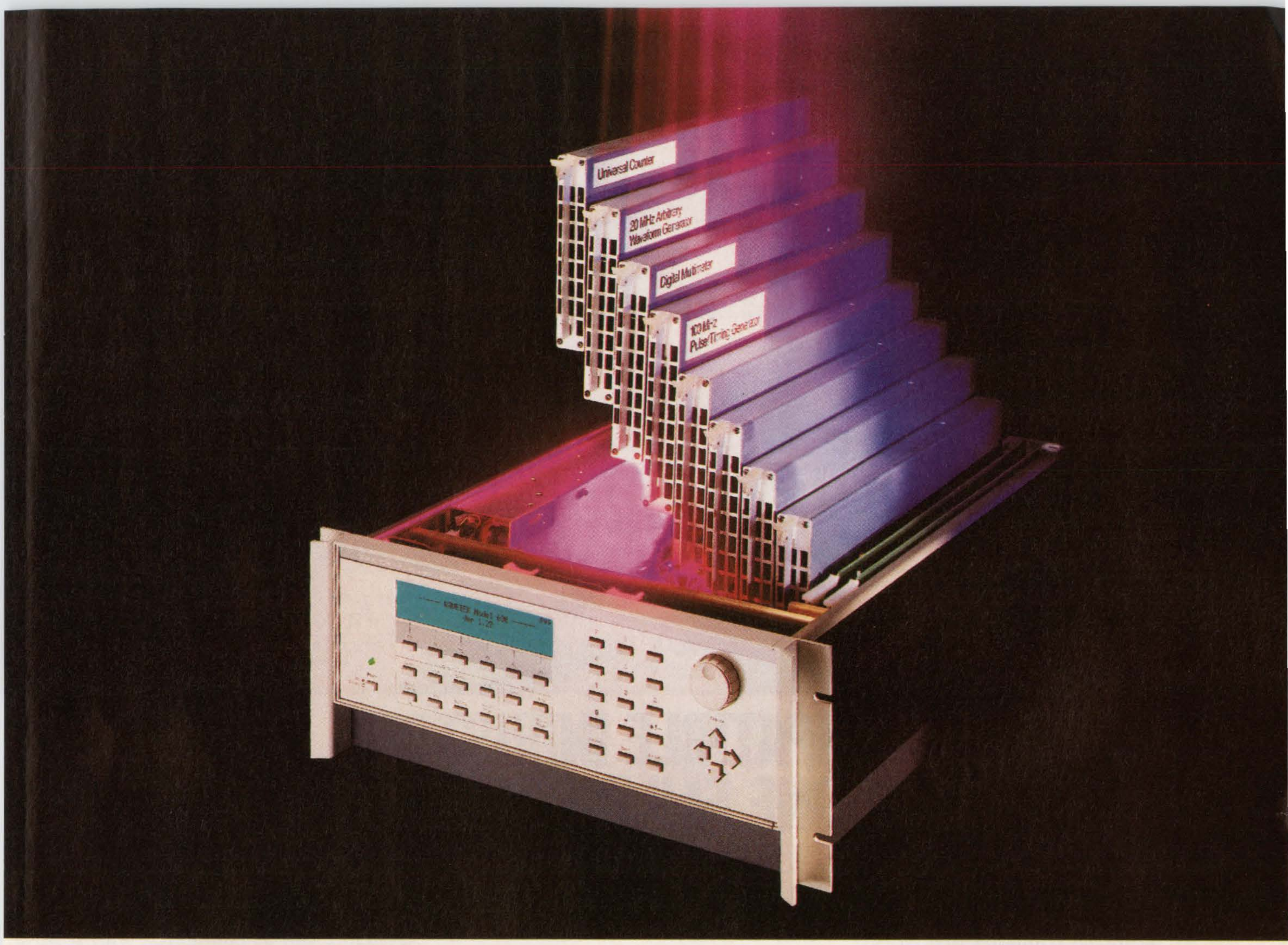

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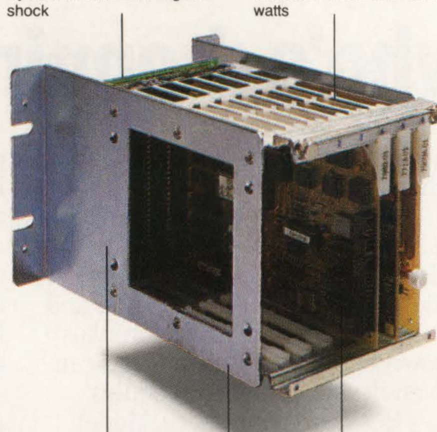

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INDUSTRIAL COMPUTERS PRO-LOG IN CONTROL QUALITY

Circle 28 for literature request only

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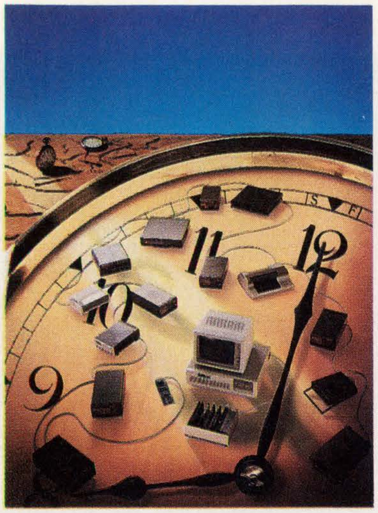
Volume 32, Number 16

EDN

August 6, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS



On the cover: *Sophisticated hardware and software tools are blurring the distinction between instrument control and data acquisition. See pg 94. (Photo courtesy Keithley Instruments)*

DESIGN FEATURES

Continued on page 7

BPA ABP

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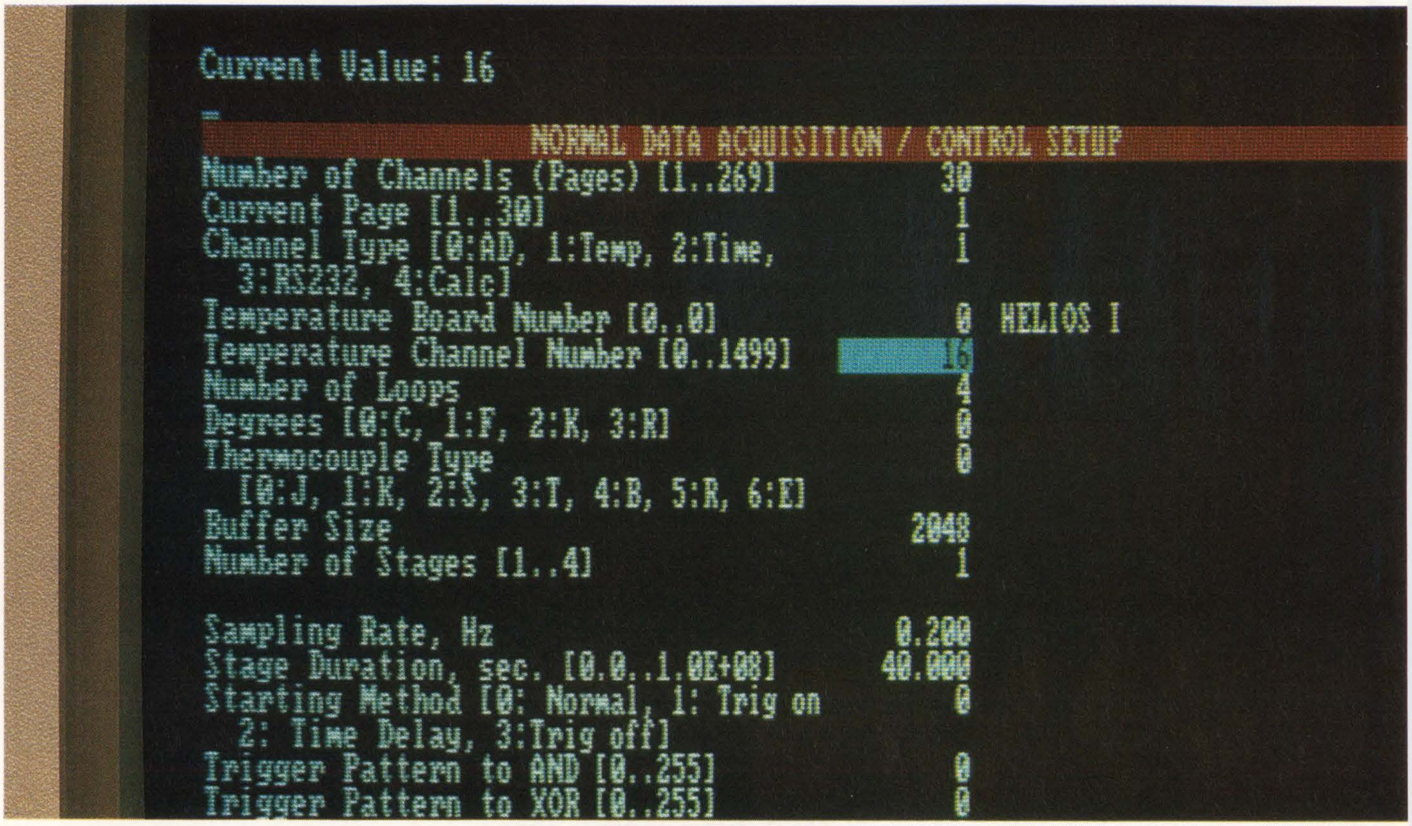

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CIRCLE NO 110

Continued from page 5

***Scientific calculators** are offering a host of intriguing new functions, features, and capabilities (pg 63).*

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

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	80186/188	LCC/PGA	○	
NEC	μPD70108/116 (V20/30)	DIP40P	○	
	μPD70208/216 (V40/50)	PGA	○	
MOTOROLA	MC68000	DIP64P,PGA68P		○

PROCESSOR (8bit)		PKG	SA2000
ZILOG	Z80CMOS (Z80, Z80A, Z80C)	DIP40P	○
	Z80H (Z80, Z80A, Z80B, Z80H)	DIP40P	○
	Z8 (Z8601/03/11/13-12R)	DIP40P	○
	SUPER-8 (Z8310-33)	DIP40/48P	○
INTEL	80C85, 8085AH-2	DIP40P	○
	8048 (8035/39/40/49/50AH)	DIP40P	○
	8051 (8031/51AH, 80C51)	DIP40P	○
MOTOROLA	MC6801 (6801/03-1)	DIP40P	○
	MC6809 (68A09, 68809)	DIP40P	○
	MC6809E (68A09E, 68B09E)	DIP40P	○
	MC68HC11	DIP48P	○
HITACHI	HD6301V/6303R, HD63701V	DIP40P	○
	HD6301X/6303X, HD63701X	SDIP64P	○
	HD6301Y/6303Y, HD63701Y	SDIP64P	○
	HD6305U/V, HD63705V	DIP40P	○
	HD6305X/Y	SDIP64P	○
	HD6305Z, HD63705Z	FLAT80P	○
	HD6309E	DIP40P	○
	HD61810B (HSP)	DIP40P	○
NEC	μPD7807/08/09	SDIP64P,QUIP64P	○
	μPD7810H/11/14/16	SDIP64P,QUIP64P	○
	μPD78C10/11	SDIP64P,QUIP64P	○
MITSUBISHI	M50734SP	SDIP64P	○
	M50745	SDIP64P	○
	M50747	SDIP64P	○
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EDITORIAL 55

You'll enjoy life more if you keep an eye open for the unexpected.

NEW PRODUCTS

PROFESSIONAL ISSUES 269

Users groups and their vendors: The ins and outs of a partnership.—*Deborah Asbrand, Associate Editor*

LOOKING AHEAD 279

Miniaturization move aids power-hybrid market. . . Delivery delays clog LVDT market.

DEPARTMENTS

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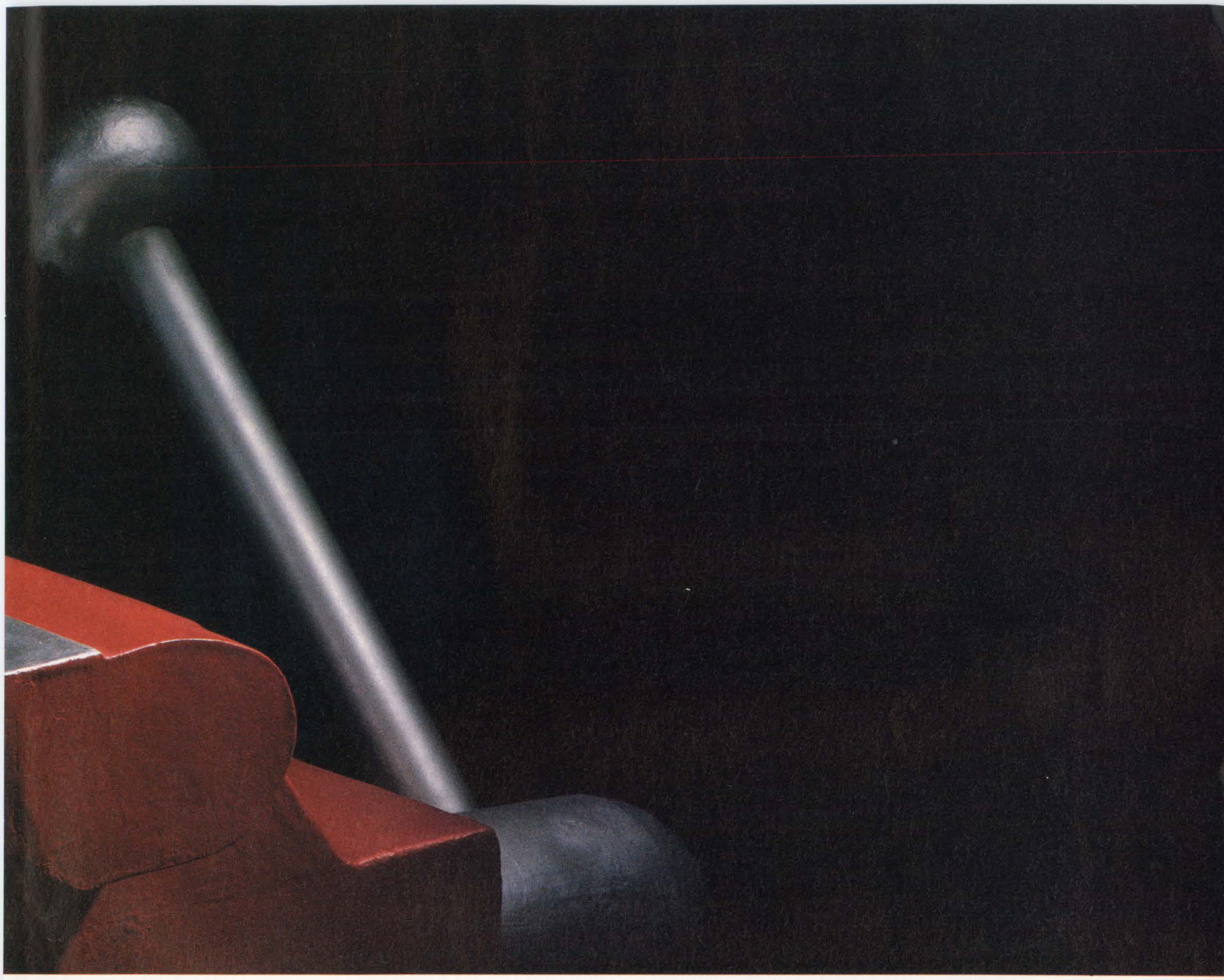

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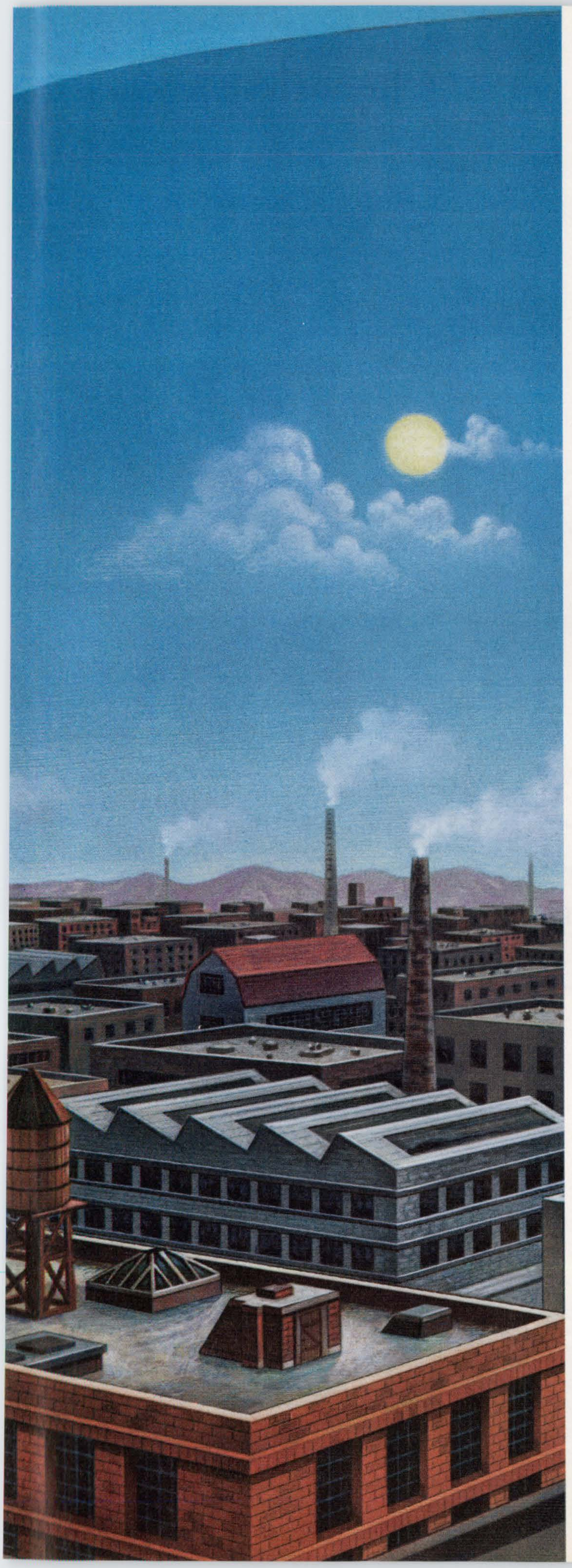

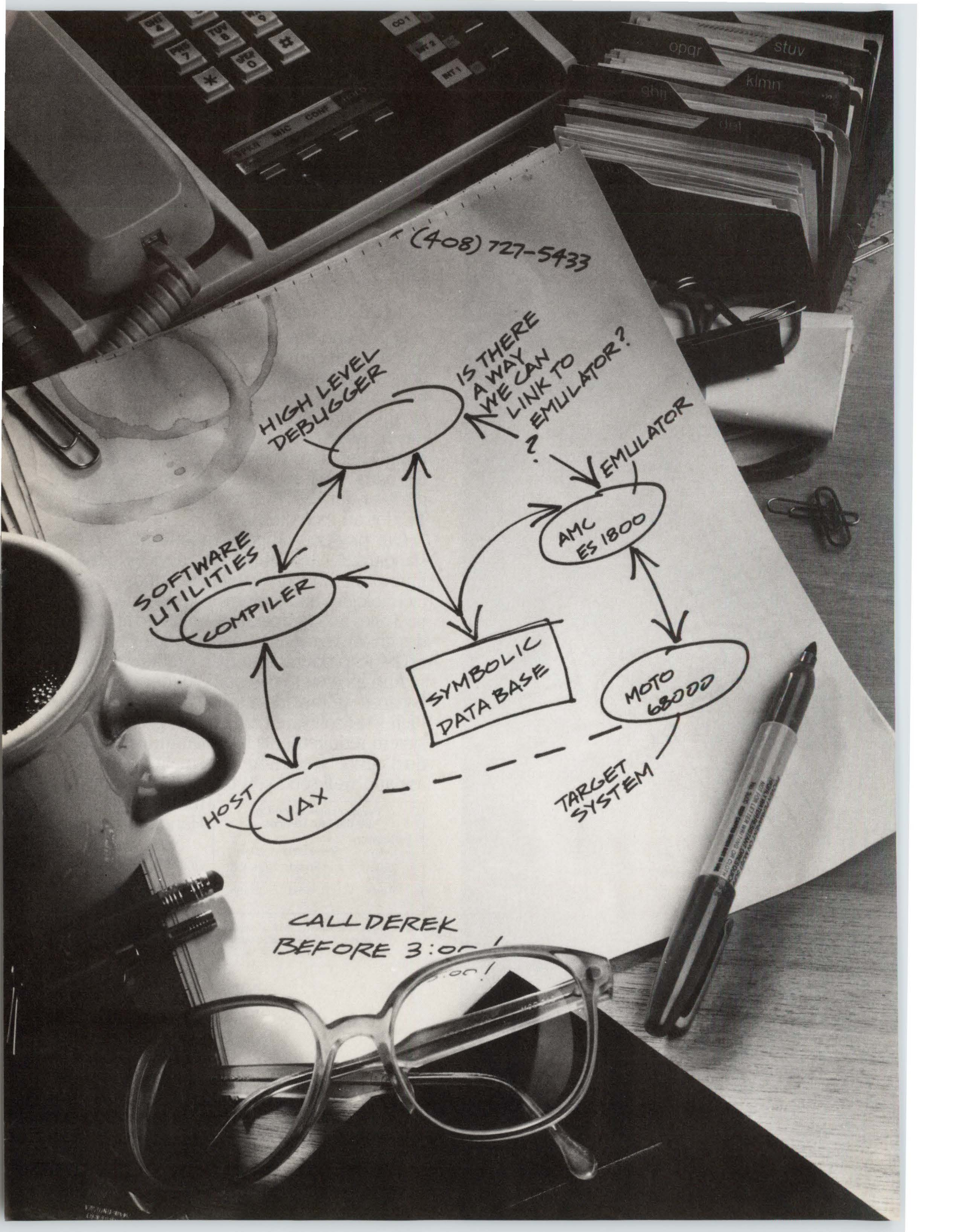
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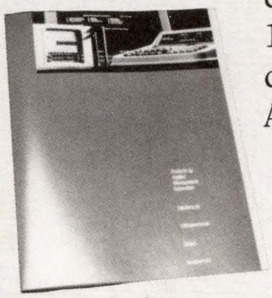

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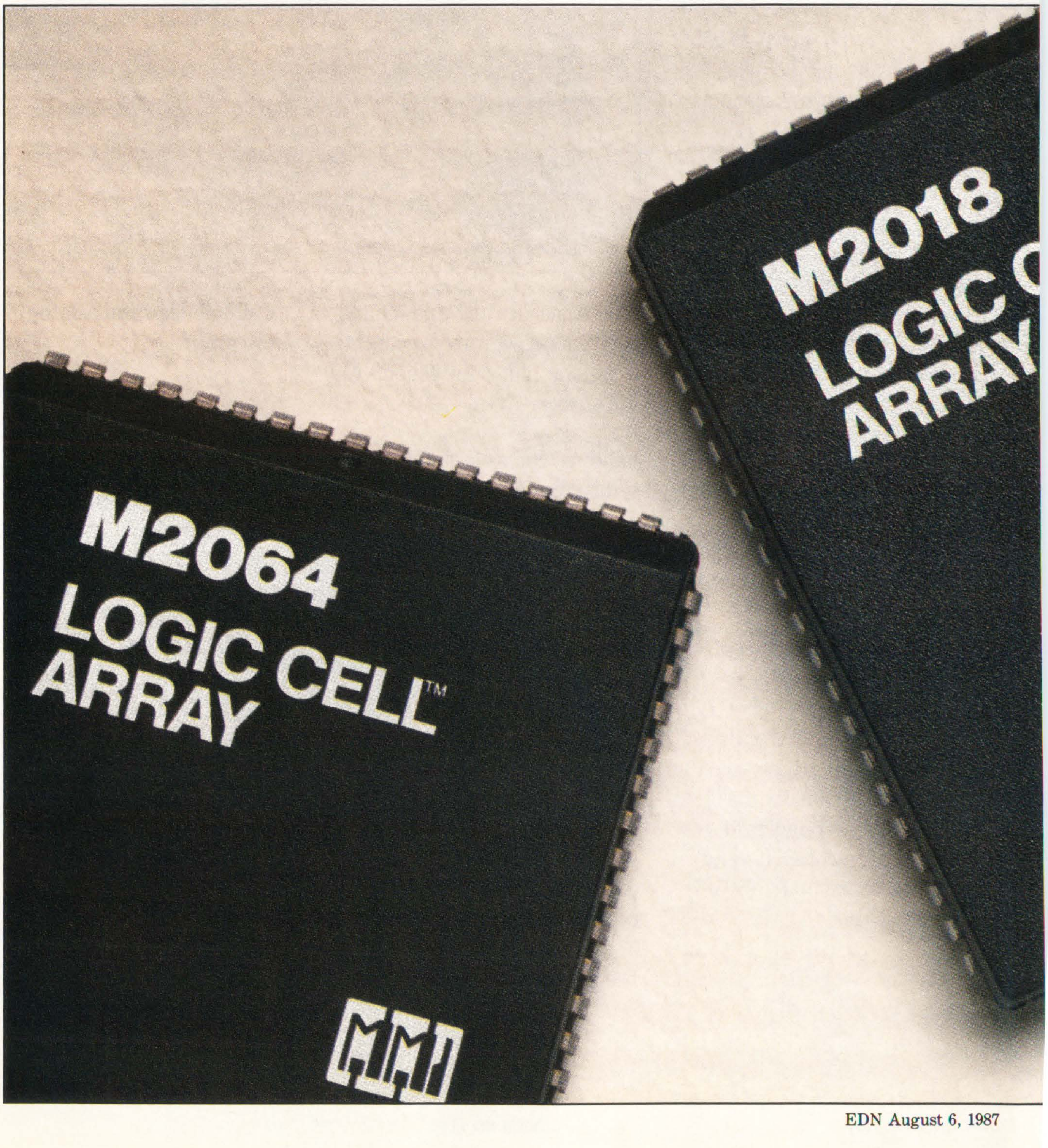

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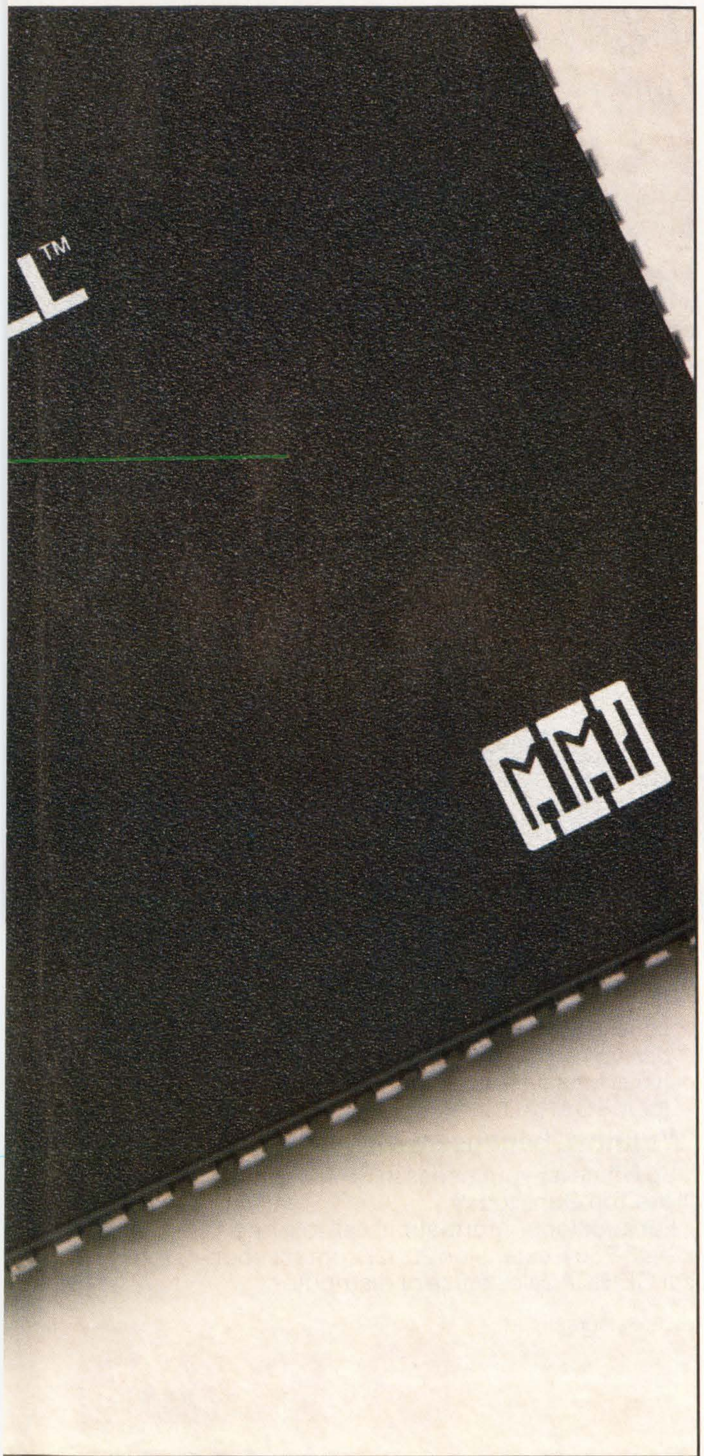

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*Rev. C, Paragraph 1.2.2

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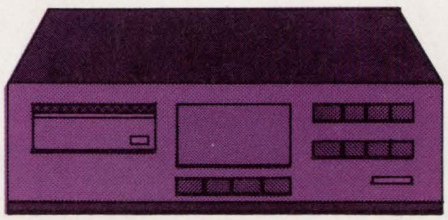

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4. Contest void where prohibited or taxed by law. Liability for any taxes on prizes is the sole responsibility of the winners.
5. Entries that most closely match the rank will be declared winners.
6. Entry cards must be postmarked before September 17, 1987
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8. In the event that a prize is not available, publisher may substitute an alternative prize of equal value without prior notice.

NEWS BREAKS

EDITED BY JOAN MORROW

80386-BASED ADD-IN BOARD TRIPLES SPEED OF MICROVAX

You can triple the processing speed of a MicroVAX system by running the system's CPU-bound programs on an 80386-based AP/20 Attached Processor add-in board. The AP/20, which costs $10,000, is made by Avalon Computer Systems (Glendale, CA, (818) 247-2216). It is compatible with any Q Bus VAX, runs at 3.5 to 4 MIPS, and features a floating-point multiply time of 437 nsec. It has its own memory and operating kernel; all user-mode instructions and many of the operating-system functions execute on the AP/20 with no transfers over the bus to the host VAX. The VAX interface only handles program loading, I/O, and system call processing.

The board comes with 4M bytes of memory. Options include high-speed floating-point capability and a choice of C, Fortran, or Pascal compilers.—Margery S Conner

FIVE TRACKBALL MODELS SUIT WORKSTATIONS AND PCs

The Mouse-Trak trackball from Itac Systems Inc (Richardson, TX, (214) 234-5366) lets you replace your mouse with a plug-in device that requires less desk space and less effort for cursor movement. For PCs, Models M4 and M5 plug into your RS-232C port, provide a cursor-speed regulator, and furnish two and three buttons, respectively, for menu selection or mouse emulation. Models Q1, MQ2, and MQ3 have quadrature interfaces for use with workstations such as the Sun, VAX, and Apollo. The Q1 and MQ2 have two buttons, and the MQ3 has three. The Q1 offers no cursor-speed control. OEM prices range from $80 (51) for the Q1 to $109 (51) for the M5.—J D Mosley

ENGINE USES THREE UNLIKE PROCESSORS TO SPEED PC-BOARD ROUTING

The combined might of a 68020 μP, a bit-slice processor, and a RISC μP in Cadnetix's (Boulder, CO, (303) 444-8075) $89,500 Route Engine III provide twice the pc-board routing performance of the company's previous offering. The standard version of the product includes 8M bytes of memory that you can expand to 48M bytes for very large jobs. Currently, the router employs a gridded, costed-maze routing algorithm, but the company plans to ship a free software upgrade, including a flexible-field routing algorithm, late this year. This flexible-field router shifts the routing grid over the span of the pc board as needed to avoid obstacles such as component pads, thus maximizing the board's routability. Owners of the company's older Route Engine Plus can upgrade their machines to Route Engine IIIs for $37,500.—Steven H Leibson

RUGGED WINCHESTERS FEATURE 129M- TO 389M-BYTE CAPACITIES

Hewlett-Packard Co (Palo Alto, CA, (800) 367-4772) has increased its offerings in the OEM hard-disk market by introducing a family of three rugged, hard-disk drives with unformatted capacities of 129M, 194M, and 389M bytes; 17-msec seek times; and an MTBF of 40,000 hours. The company offers these drives in both SCSI and ESDI versions as the HP97530S and HP97530E, respectively. The SCSI version supports the SCSI common command set, asynchronous transfer rates of 1.5M bytes/sec, and synchronous rates exceeding 2M bytes/sec. The ESDI version features a 10M-bps burst-transfer rate. In quantities of more than 1500, the 389M-byte versions of the SCSI and ESDI drives cost $2050 and $1900, respectively.—Steven H Leibson

KEYBOARD LETS YOU CHANGE LAYOUTS AND LEGENDS ON SITE

If you need a keypad that you can alter repeatedly, consider the reconfigurable keyboard from Preh Electronic Industries (Niles, IL, (312) 647-8338), which lets you easily change legends. According to the manufacturer, this "coffee and cola proof" keypad resists spills and moisture, thus making it suitable for factories and point-of-sale systems. But it's the polyvalent frame that lets you perform fast layout changes on site by popping off and repositioning single-, double-, triple-, and quad-size keys. You can even mix and interchange the various sizes on a single keypad. Changing legends on the keys is just as simple. OEM pricing for a typical keypad incorporating at least one multiposition key ranges from $20 to $100.—J D Mosley

SOFTWARE RELEASE QUADRUPLES MAP COMMUNICATIONS THROUGHPUT

Release 2 of the MicroMAP 2.1 software from Motorola Inc (Tempe, AZ, (800) 521-6274), running on the company's $2660 MVME372 MAP controller board, speeds task-to-task communications over the MAP network by a factor of four compared with the company's previous software. This latest software release increases the effective data rate between Unix tasks running on different network nodes from 35,000 to 140,000 bytes/sec. The company offers the new product for $600/copy and will sell source licenses to interested parties.—Steven H Leibson

8-BIT FLASH A/D CONVERTER DIGITIZES DATA AT 125M SAMPLES/SEC

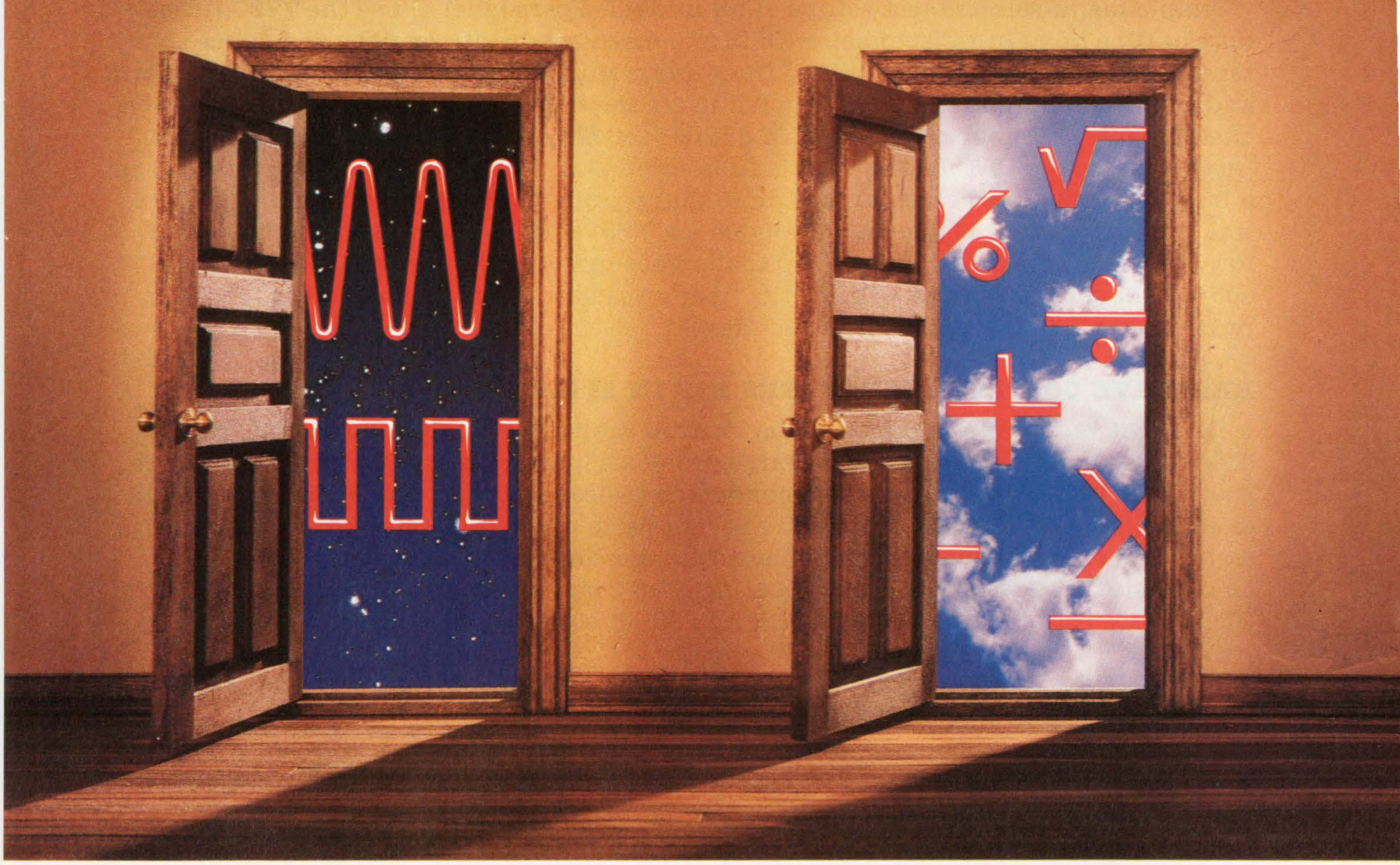
The HADC77200 flash A/D converter from Honeywell's Signal Processing Technologies (Colorado Springs, CO, (303) 577-1000) features a minimum sample rate of 125M samples/sec with a 5-nsec acquisition time. The IC includes an input preamplifier that minimizes the input noise often associated with flash converters. The converter, including the preamp, can follow signals with slew rates to 650V/μsec. Prices for the device are $115 (100) for a ±0.75-LSB version of the converter and $150 for a ±0.5-LSB version.—Steven H Leibson

IMAGE-PROCESSING ICs OPERATE ON VIDEO IMAGES IN REAL TIME

A family of five devices, which will be available in the 3rd qtr from LSI Logic Corp (Milpitas, CA, (408) 433-8000), will allow you to build real-time image-processing systems. Components in the 20-MHz family obtain their speed from highly parallel internal architectures. The $35 (500) L64210 and $60 (500) L64211 variable-length, video shift registers act as formatting devices for the other devices in the family by accepting four 1032-pixel or eight 516-pixel lines of 8-bit/pixel video data, respectively, and outputting the data in a parallel, multiline format. The $395 (500) L64220 rank-value filter operates on 12-bit data points in 1×64-, 2×32-, 4×16-, or 8×8-pixel arrays; determines pixel maxima or minima; finds pixels with a user-specified value; or masks pixels for windowing operations.

The $395 (500) L64230 binary filter and template matcher contains 1024 filter taps, each consisting of a 1-bit multiplier/comparator and associated adder, and will operate on 1- or 2-dimensional pixel arrays with window sizes to 32×32 pixels. Comprising the equivalent of 64 8×8-bit multiplier/accumulators, the $695 (500) L64240 multibit filter operates on 8- or 16-bit data presented in 1- or 2-dimensional arrays. All of the components are available as building blocks for incorporation into the company's ASICs.—Steven H Leibson

Bringing the Worlds of Data Acquisition and DSP Together



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NEWS BREAKS: INTERNATIONAL

OPTICAL TIME-DOMAIN REFLECTOMETER SIMPLIFIES FIBER TESTING

Simple menu-selected test setups allow unskilled personnel to use the 7720 Series optical time-domain reflectometer (OTDR) to make bandwidth or fiber and splice attenuation measurements on optical fiber links. More experienced personnel can obtain additional measurement data and zoom in on areas of special interest. From Solartron Instruments (Farnborough, UK, TLX 858245, or Elmsford, NY, (914) 592-9168), the instrument has a CRT display that is fully annotated with the fiber's losses, and it has a built-in printer and cassette tape drive that provide hard copy and storage/recall of link characteristics. Models are available for 0.85- and 1.3-μm multimode fibers and for 1.30-μm single-mode fibers. A special optocoupling device for the 0.85-μm fiber accepts all cable sizes and reduces the fiber's dead zone to zero. The OTDRs range in price from £12,000 to £16,500.—Peter Harold

RESISTIVE COATING ELIMINATES ESD IN ATE FIXTURES

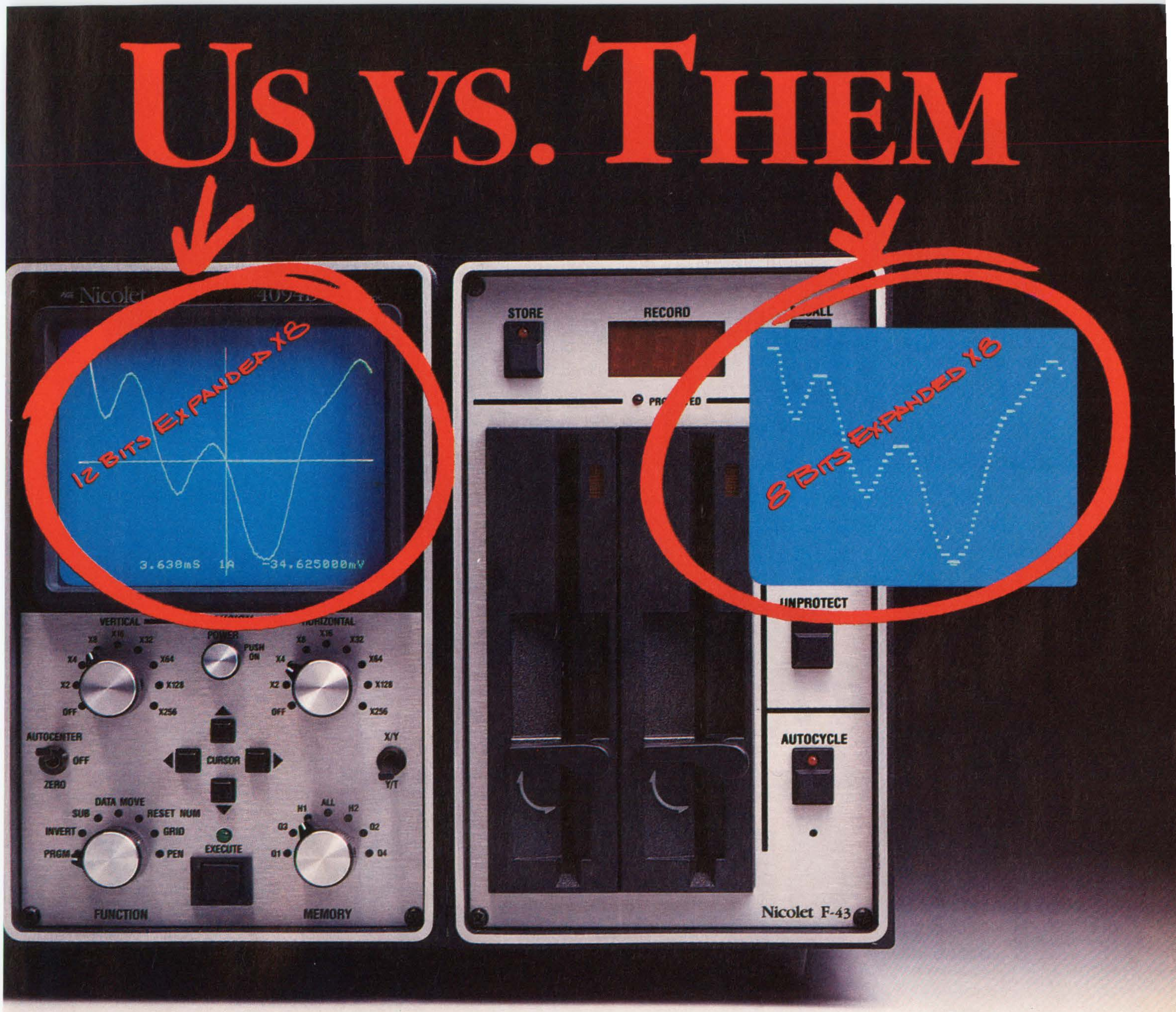
Diss-Stat vacuum test fixtures from Factron Schlumberger (Ferndown, UK, TLX 41436) eliminate electrostatic-discharge problems in board-test ATE, which can cause premature failure of sensitive semiconductor devices on the pc boards under test—for example, submicron VLSI chips. All relevant parts of the test fixture, including any internal and external surfaces that may accumulate an airflow-induced electrostatic charge, are coated with a resistive coating. This coating provides a discharge path for the electrostatic charge of between 10^9 and 10^{10} Ω/square.—Peter Harold

MITI GIVES APPROVAL TO US LAB FOR INSPECTION OF EXPORTS TO JAPAN

The Japanese Ministry of International Trade and Industry (MITI) has designated the United States Testing Co Inc (Hoboken NJ) as a Specific Foreign Inspection Organization in the "JIS" Mark program. This authorization by the MITI allows US Testing to perform inspection for export to Japan on a wide variety of industrial and consumer goods, including electronic equipment and electrical machinery. For more information, you can call the company at (201) 792-2400.—Joan Morrow

US CONCEPT, JAPANESE ENGINEERING LEAD TO NEW OFFICE PRODUCT

From a concept by Jef Raskin, originator of the Macintosh computer, Canon Inc (Tokyo) and Canon USA (Lake Success, NY, (516) 488-6700) have engineered and produced the Canon Cat, a "work processor" that includes a keyboard, 9-in. black-and-white display, software with spelling checker, a 3½-in. floppy-disk drive, a modem, and serial and parallel interfaces. An improvement in cursor control, called Leap keys, allows you to quickly locate and edit, move, or restyle information in 180k bytes of stored text in just a few keystrokes. The systems sells for $1495.—Joan Morrow



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SERIAL I/O	**ISIO-1** 68010 (10 MHz) 128 Kbyte SRAM dual ported, zero wait state access 8 serial I/O channels (RS232)	**ISIO-1** 68010 (10 MHz) 128 Kbyte SRAM dual ported, zero wait state access 8 serial I/O channels (RS232)
ADD. I/O CHANNELS	**ASCU-2** System controller, IEEE 488 interface, Centronics parallel printer port	**ASCU-2** System controller, IEEE 488 interface, Centronics parallel printer port
DISK DRIVES	170 Mbyte winchester, 1 Mbyte floppy 120 Mbyte streamer tape	170 Mbyte winchester, 1 Mbyte floppy 120 Mbyte streamer tape (optional)

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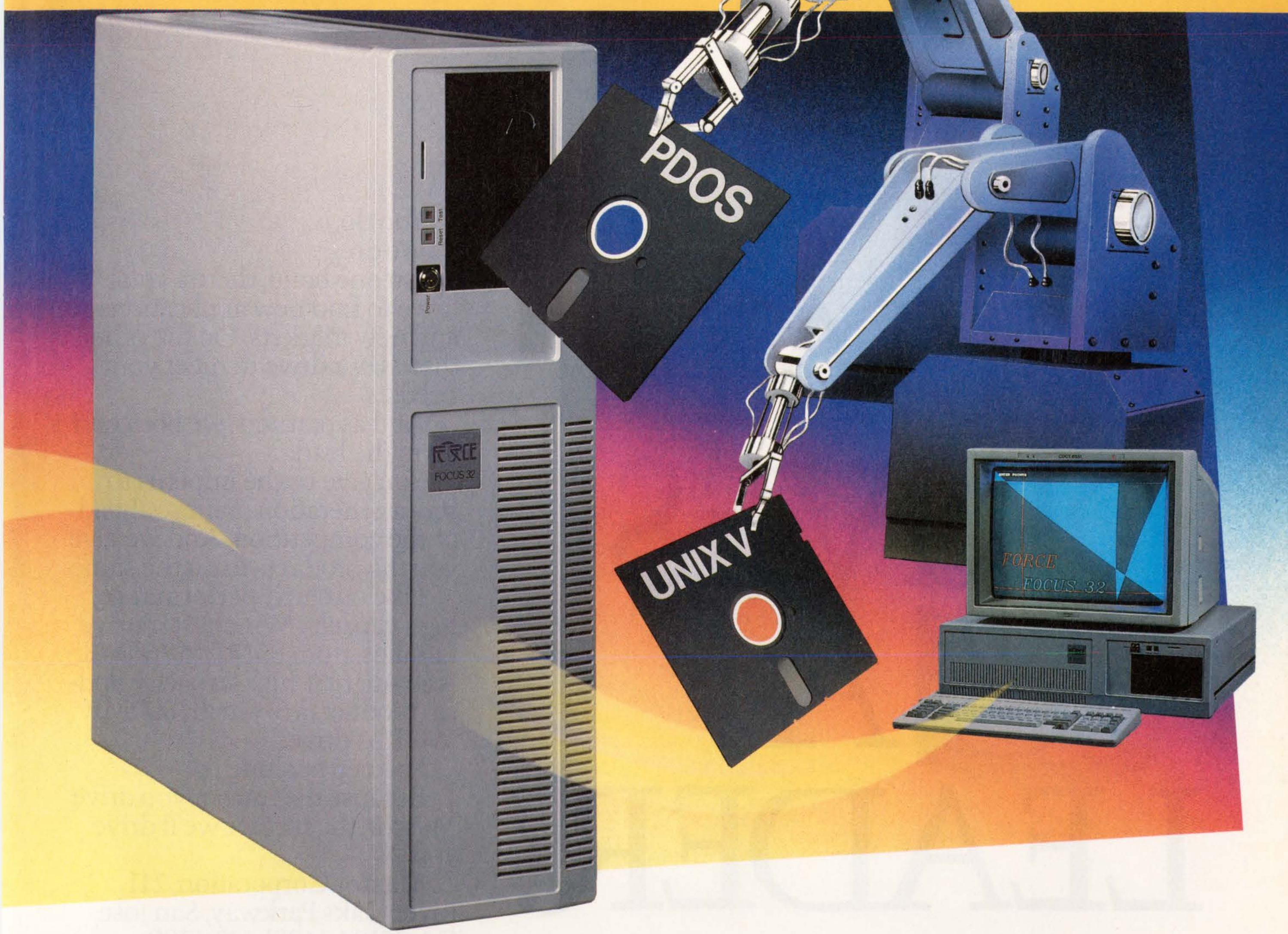

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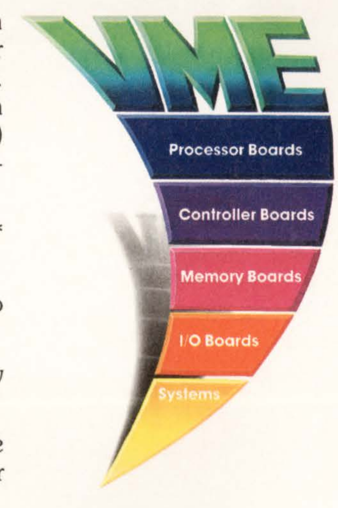

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SIGNALS & NOISE

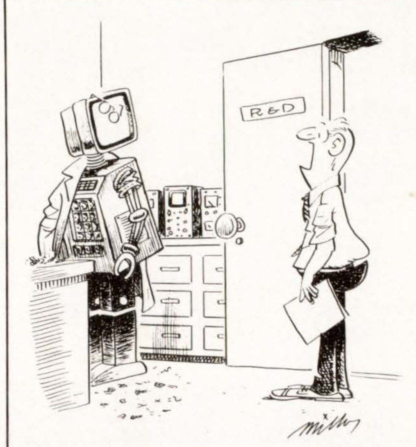
A clarification of telephone-noise specs

The excellent article by Brady Barnes in EDN's May 14 issue ("Check advanced features and noise specs when selecting codecs," pg 227) was interesting and informative in most respects, but Mr Barnes's attempts to clarify noise specifications (on pgs 229 to 234 of the article) may have added to any existing confusion about them. As an engineer with over 20 years' experience in testing international telephone circuits, perhaps I can offer some clarification.

Telephone-circuit weighing filters are based on the performance of telephone handsets, not on that of the human ear. While the Bell Telephone system held a monopoly position in the US, weighing filters were based on the telephone set currently in use. Bell system engineers thought that noise should be measured as a positive quantity; they introduced the concept of "reference noise." When the Western Electric Co (WECO) Model 144 handset was in use, the noise-measuring term was "dBRN" (144 line). The WECO Model F1A handset resulted in F1A weighing. C-Message-weighing filters are based on the WECO Model 500 handset, and the current US telephone noise-measuring term is dBrnC; −90 dBm is the current reference-noise level.

The CCITT, as an international standards group, produced a weighing filter based on the characteristics of most of the world's telephone handsets, and called it a "psophometric" filter after the Greek word "psophos," which means "noise." The CCITT's term for telephone-noise measurement is dBmp.

The CCITT did not adopt the Bell system's concept of reference noise, and no CCITT noise measurement implies reference noise. Unweighed noise is measured in dBm. Conversion to dBrn is simply a matter of adding 90. For example, a CCITT



"...A TALL GUY WITH GLASSES AND A MEDIUM HEIGHT FELLOW WEARING A SMOCK—THEY WORK HERE...WERE DEVELOPING A HUMAN-LIKE ROBOT."

measurement of −70 dBm is equal to 20 dBrn (that is, −70 dBm is 20 dB greater than the −90-dBm reference level). Similarly, you can easily convert 30 dBrn to a CCITT level of −60 dBm by subtracting 90. This conversion is exact for an unweighed measurement such as 3-kHz flat.

The psophometric and C-message filters are so nearly equivalent in terms of noise-power measurements that, even though the C-message filter is based on a reference tone of 1000 Hz and the psophometric filter is based on an 800-Hz tone, in a practical sense they are used interchangeably. In a telephone channel that has only white noise, both filters improve the noise reading by approximately 2 dB as compared with a 3-kHz flat measurement.

Consequently, you can convert dBmp to dBrnC simply by adding 90, and you can convert dBrnC to dBmp by subtracting 90. In other words, −65 dBmp is equal to 25 dBrnC. The conversion is accurate to within ±0.5 dB, which is better than the accuracy of most noise meters.

The term "dBp" means "dB referred to 1 pW," just as "dBm" means "dB referred to 1 mW." Since the Bell system has established 1 pW (−90 dBm) as reference noise, the terms dBrn and dBp are equiva-

Text continued on pg 34

TEK'S NEW EASY-TO-EXPERT LOGIC ANALYZER $3995.*

Introducing the Tek 1220 and 1225: the two newest members of the Tek 1200 Series of logic analyzers. Nothing else in their price range delivers so much and makes it all so easy to use. Consider:

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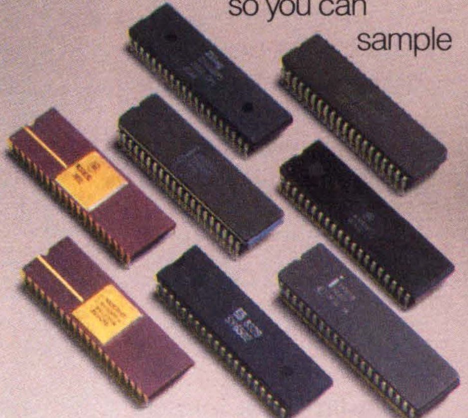

data from as many as three circuit sections at once.

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lent, and no weighing is implied.

Thus, −65 dBm0p (the level that CCITT recommends idle-channel noise not exceed) is equal to 25 dBrnC0 (−65+90) for telephone weighing. The equivalent 3-kHz flat values are −63 dBm0 and 27 dBrn0 (you add 2 to remove the weighing effect).

Most telecommunications handbooks have these conversion factors in chart form for easy use. One such handbook is Roger L Freeman's *Telecommunication Transmission Handbook*, 2nd ed, which is published by John Wiley & Sons.

G W Foreman
Contel Federal Systems
Applied Systems Div
Fairfax, VA

Transistor should be diode-connected

In my article "JFET-input amps are unrivaled for speed and accuracy" (EDN, May 14, pg 161), **Fig 4** (on pg 165) contains an error. The temperature-sensing transistor, Q_2, should be diode-connected; that is, its base and collector should be shorted together. Without this short, the circuit will have extreme difficulty working. I hope the error did not cause too many difficulties for those building the circuit.

Peter S Henry
Precision Monolithics Inc
Santa Clara, CA

What's in a name

"The promise of surface-mount technology," part 1 of EDN's Hands-On SMT Project (EDN, May 28, pg 164), used the word "onserter" in the photo caption on pg 172 as a generic name for automatic-insertion equipment for surface-mount devices (SMDs). Instead, we should have used the term "onsertion equipment," as we did elsewhere in the article. "Onserter" is a trademark of Universal Instruments Corp (Binghamton, NY) for its pick-and-place machine for SMDs. We apologize for inadvertently taking the name in vain.

Sorry, wrong number

The manufacturers' box accompanying EDN's μC Support-Chip Directory (EDN, June 11, pg 131) contained an incorrect phone number for AT&T Technologies Inc. The correct number is (800) 372-2447.

WRITE IN

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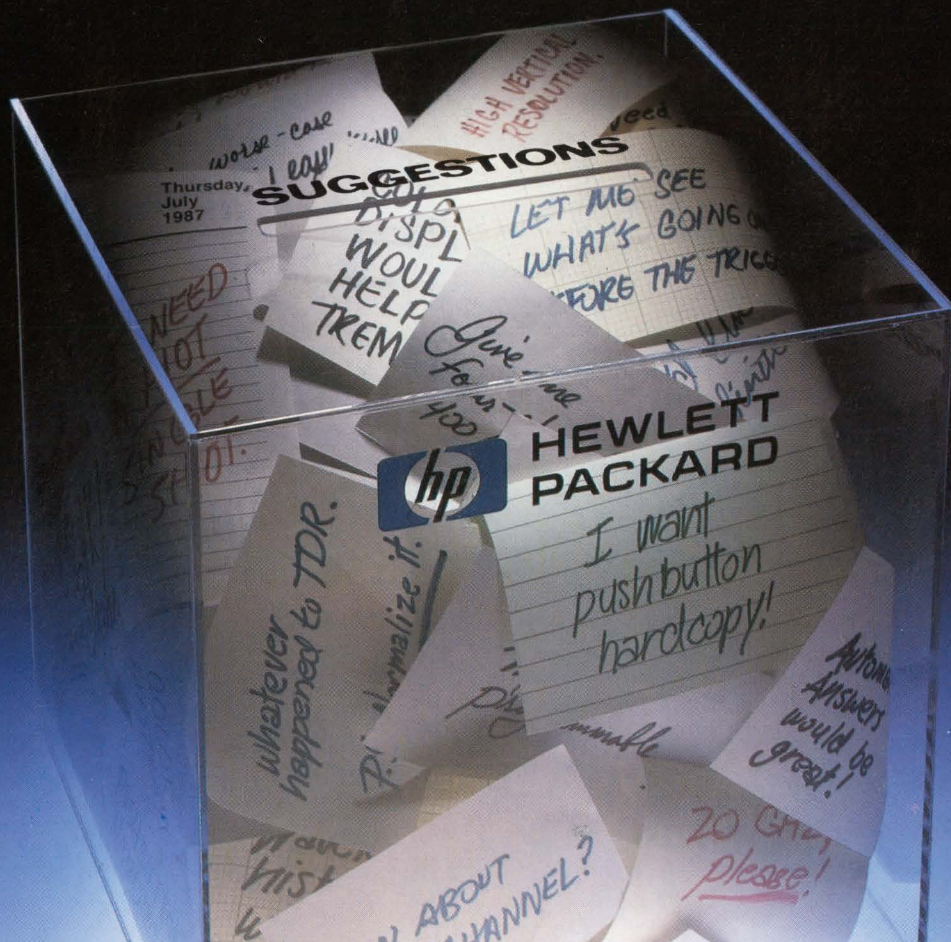

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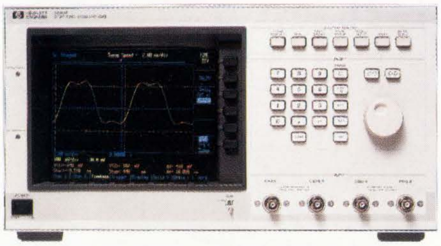

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Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	1 GSa/sec
Resolution	10 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	8k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups	10

HP 54112D $22,900.00*

VERTICAL:	
Rep. bandwidth	100 MHz
S.S. bandwidth	100 MHz
Inputs	4 chan & 1 trig
Resolution	6 bit to 100 MHz
Sensitivity	5 mV/div to 5 V/div
Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	400 MSa/sec
Resolution	40 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	64k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups:	10

HP 54120T $27,850.00**

VERTICAL:	
Rep. bandwidth	20 GHz
S.S. bandwidth	NO
Risetime	17.5 psec
Accuracy	0.4%
Inputs	4 chan & 1 trig
Resolution	12 bits
Sensitivity	1 mV/div to 80 mV/div
Coupling	50 Ohm
HORIZONTAL:	
Accuracy	10 psec
Resolution	0.25 psec
Pre-trigger viewing	NO
Range	10 psec/div-1 s/div
MEMORY:	
Acquisition/chan	0.5k
Waveform storage	2 pixel (volatile), 4 rep wfm (nonvolatile)
Nonvolatile instrument setups:	10
TDR	
Pulse source	
Amplitude	0-200 mV
Risetime	35 psec
Flatness	1%
Normalization	YES
Waveform histograms	YES

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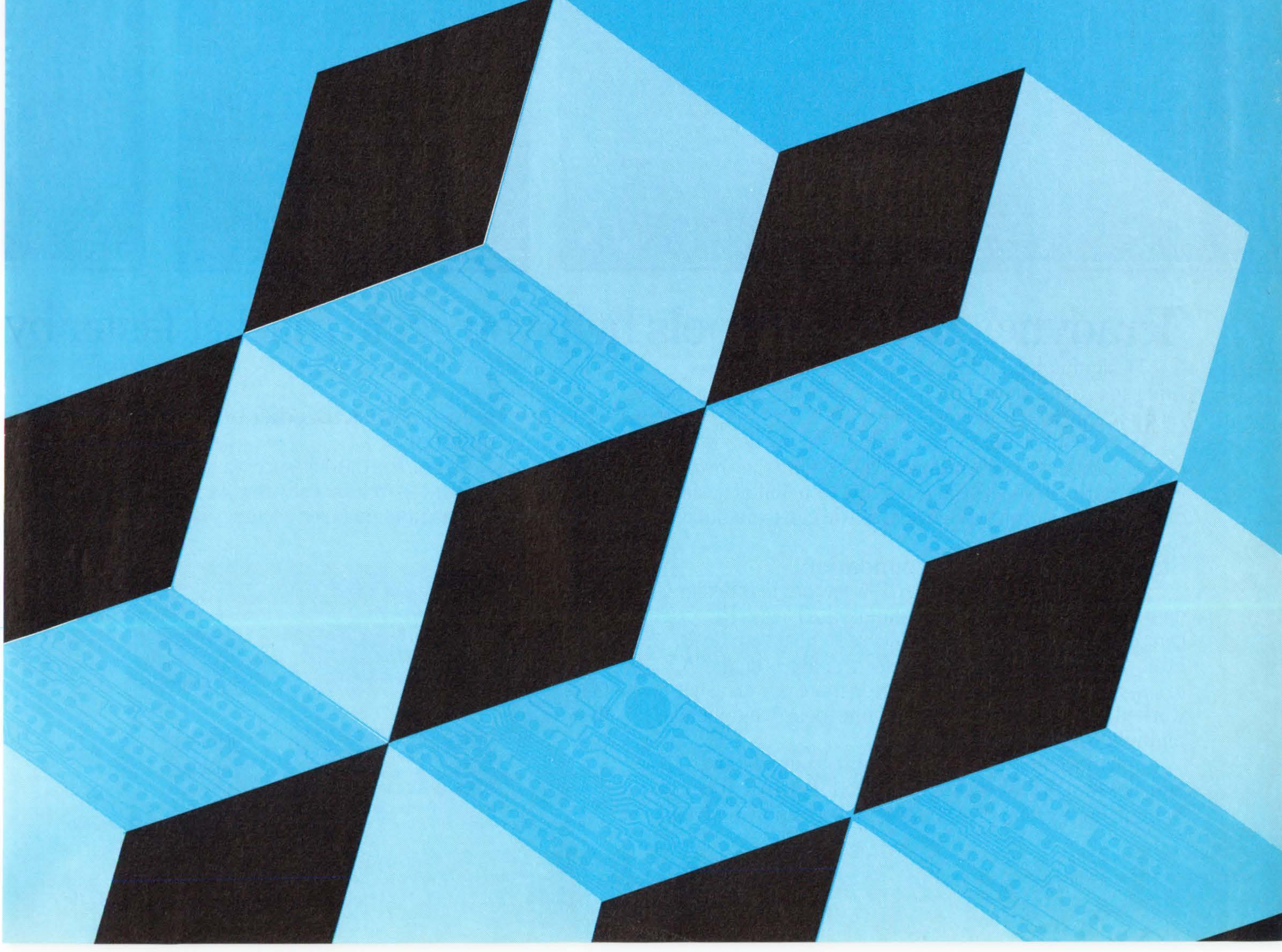
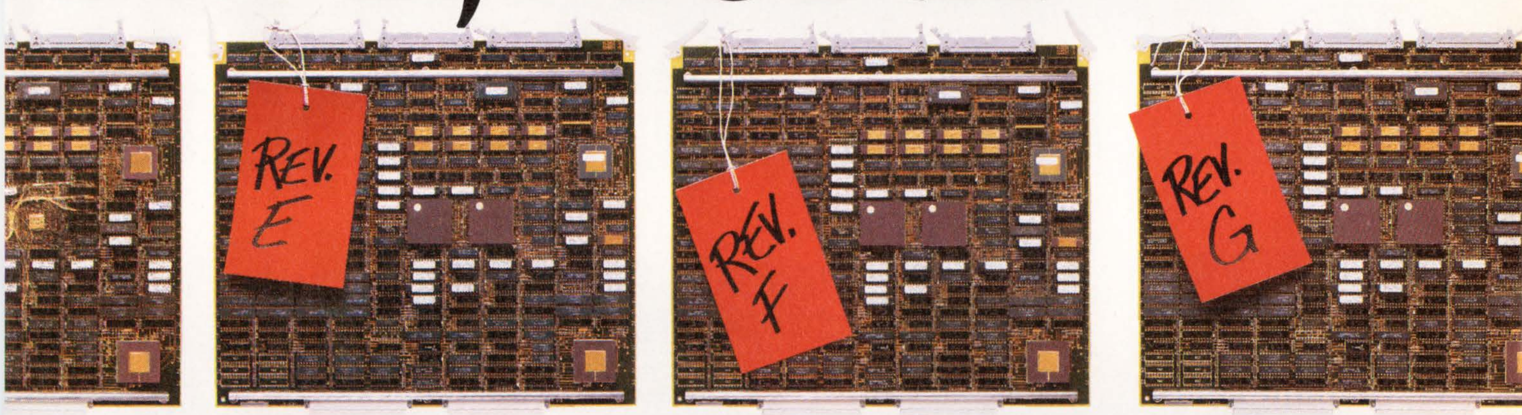


TWO PROTOTYPE, OTYPE FOUR. , SIX PROTOTYPE, OTYPE, MORE.



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CIRCLE NO 66

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Hitachi makes more devices in CMOS than anybody else. Our product lines include CMOS microprocessors and microcontrollers, as well as peripherals, gate arrays, and a broad range of memories. They're available in various industry-standard architectures, in a choice of speeds, temperature ranges, and packaging variations.

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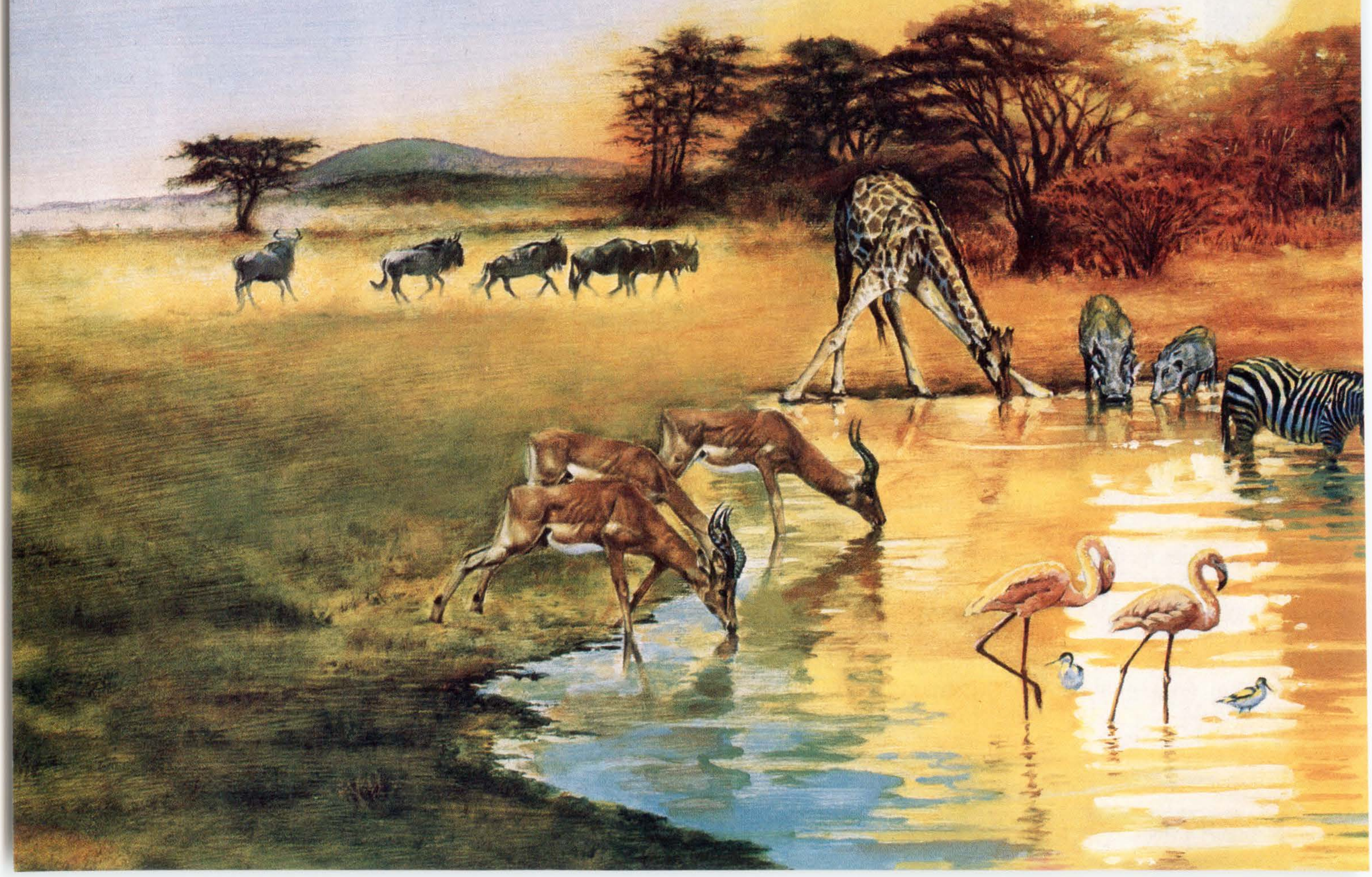

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- HD6303/6309 and HD64180 8-Bit Microprocessors
- HD68HC000 16-Bit Microprocessors
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International Computers in Engineering Conference and Exhibition, New York, NY. American Society of Mechanical Engineers, 345 E 47th St, New York, NY 10017. (212) 705-7795. August 9 to 13.

Modern Techniques in Digital Signal Processing and Analysis (short course), Santa Cruz, CA. University of California Extension, Santa Cruz, CA 95064. (408) 429-4535. August 10 to 12.

Intensive C Language Programming (short course), Santa Cruz, CA. University of California Extension, Santa Cruz, CA 95064. (408) 429-4535. August 10 to 13.

Advanced SMT Design Techniques (short course), San Jose, CA. Surface Mount Technology Plus, 2216 Lundy Ave, San Jose, CA 95134. (408) 943-0196. August 17 to 18.

Engineering and Manufacturing '87, Boston, MA. National Computer Graphics Association, 2722 Merrilee Dr, Suite 200, Fairfax, VA 22031. (703) 698-9600. August 17 to 20.

Designing Signal Processors with DSP and Bit-Slice Chips (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 1 to 4.

Effective Skills for Technical Managers (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 1 to 4.

Modern Electronic Packaging, Seattle, WA. Technology Seminars, Box 487, Lutherville, MD 21093. (301) 269-4102. September 9 to 11.

Invitational Computer Conference Computer Graphics Series, Fort Lauderdale, FL. BJ Johnson & As-

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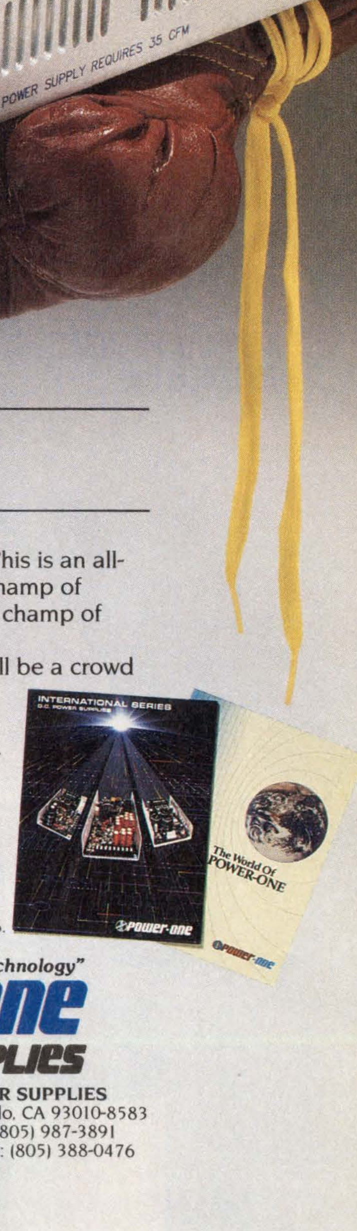
* Electronic Buyers' News, Annual Top 100 Component Suppliers Survey ... 1984, 1985, 1986.



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sociates, 3151 Airway Ave, #C-2, Costa Mesa, CA 92626. (714) 957-0171. September 10.

Integrated Manufacturing Solutions (IMS '87), Long Beach, CA. Intertec Communications, 2472 Eastman Ave, Bldg 33-34, Ventura, CA 93003. (805) 658-0933. September 14 to 18.

Hands-On Microprocessor Software, Hardware, and Interfacing (short course), Washington, DC. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 15 to 17.

PCB Expo, Minneapolis, MN. PMS Industries, 1790 Hembree Rd, Alpharetta, GA 30201. (404) 475-1818. September 15 to 17.

Effective Skills for Technical Managers (short course), Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 15 to 18.

Designing Signal Processors with DSP and Bit-Slice Chips (short course), Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 22 to 25.

Hands-On Microprocessor Software, Hardware, and Interfacing (short course), San Diego, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. September 22 to 25.

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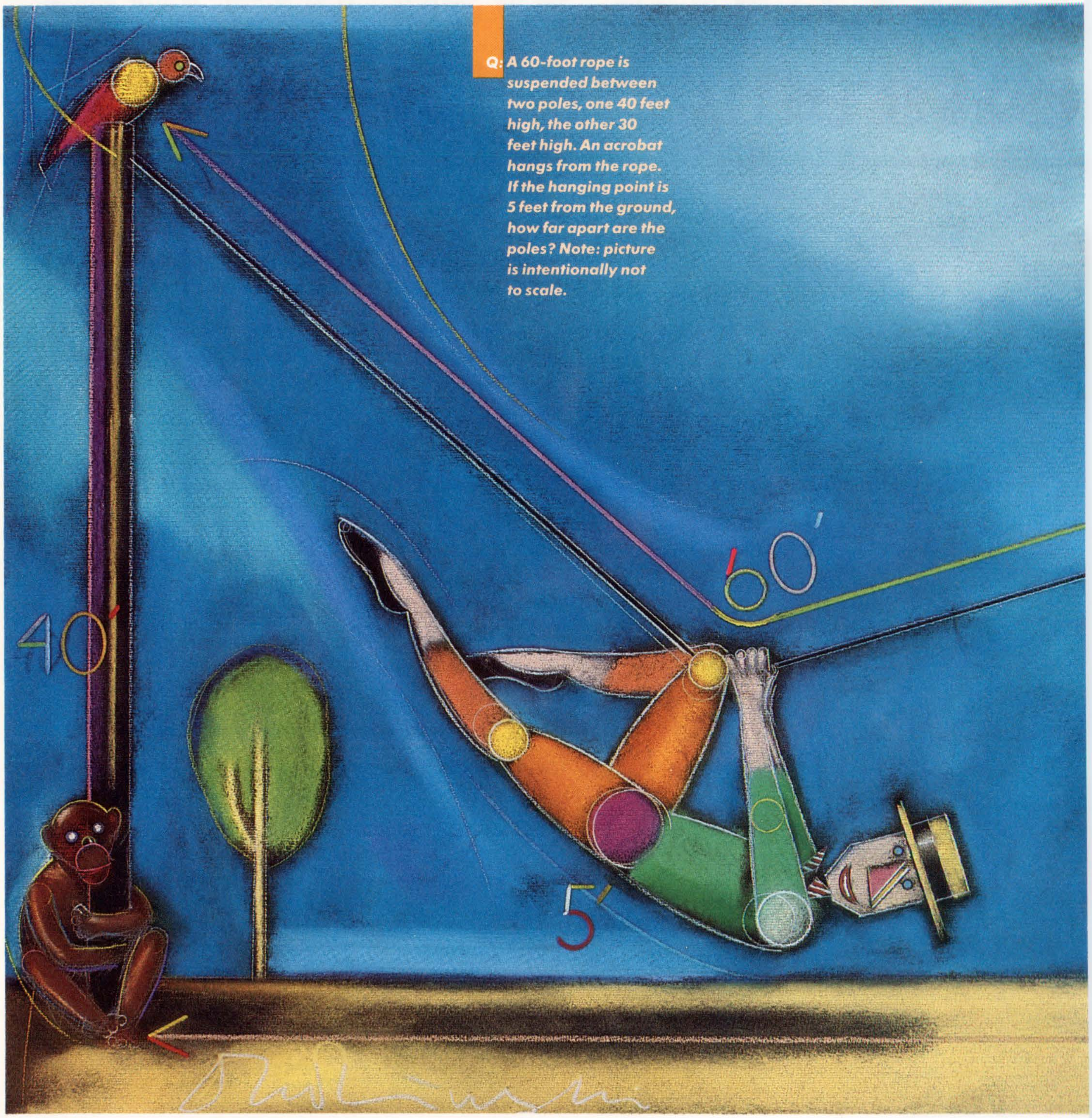
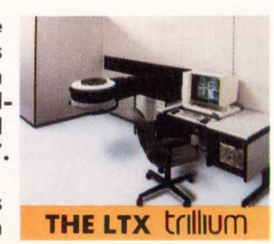
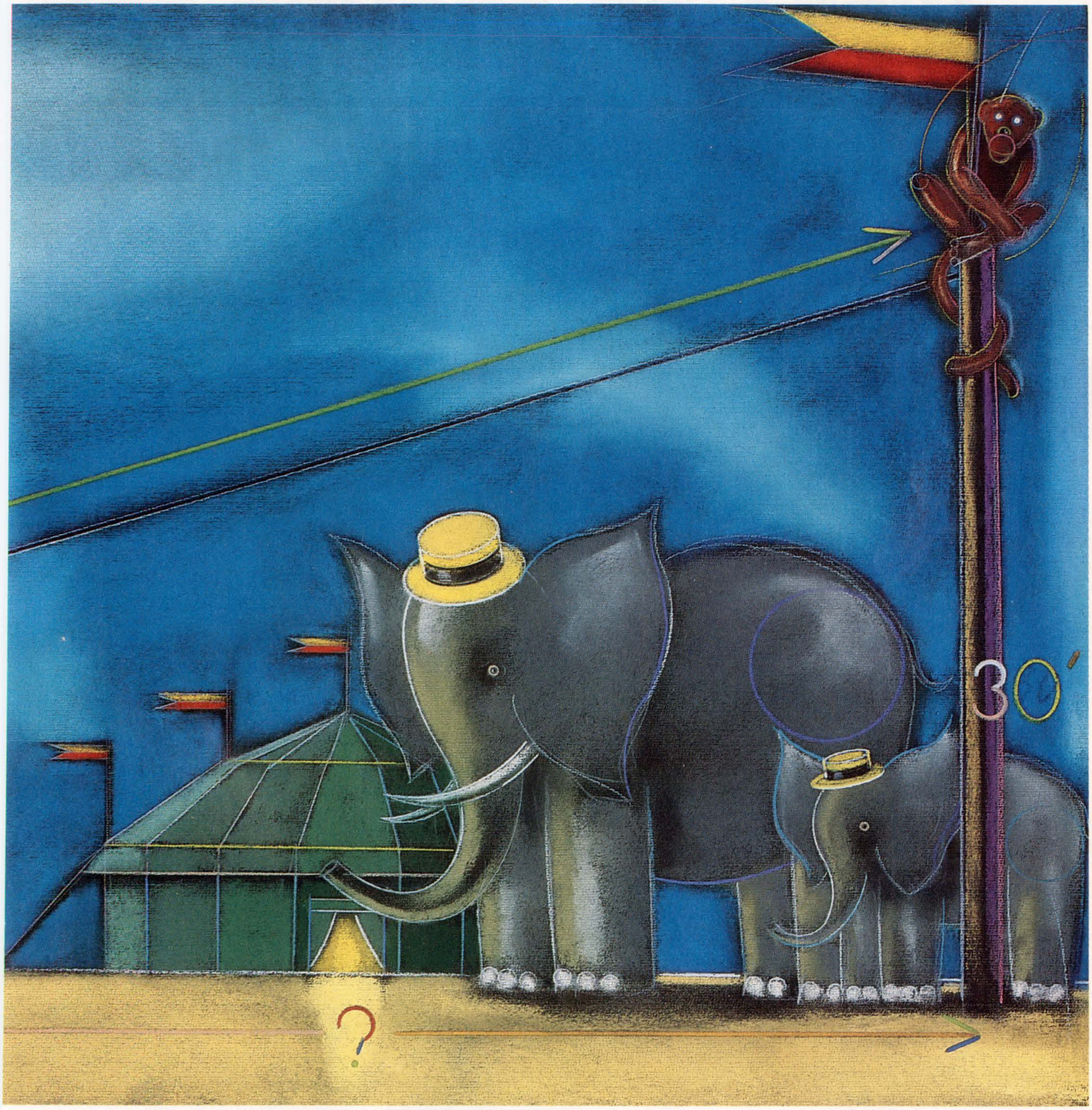
CIRCLE NO 65

A TOUGH ACT TO FOLLOW.







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CIRCLE NO 63

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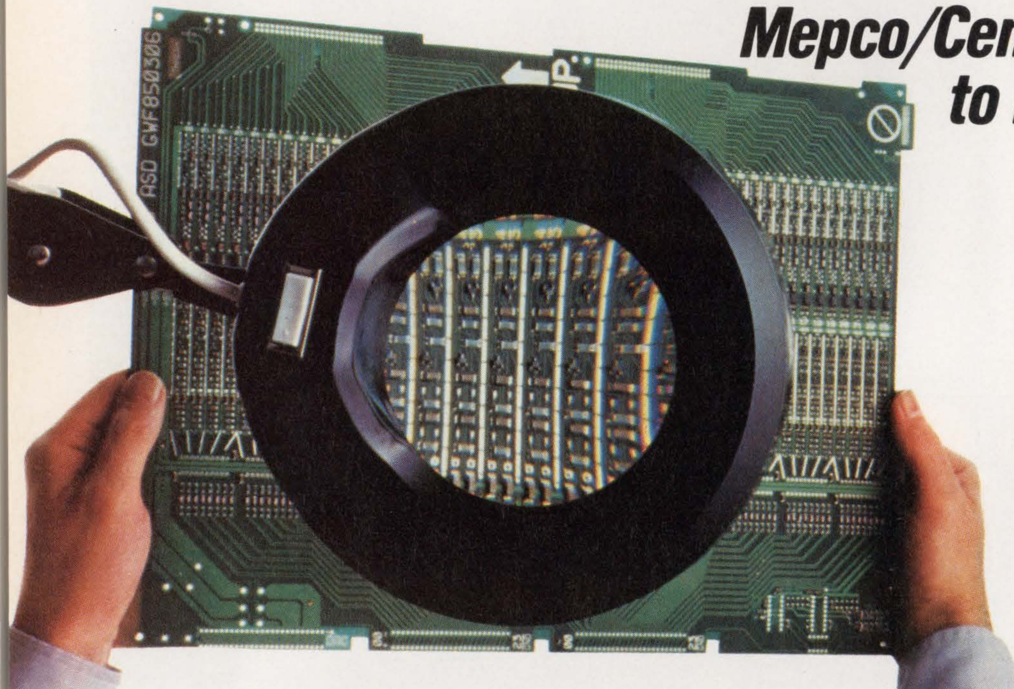

We know you face stiff competition with your next generation of products. We're actively working to help you stay in front.

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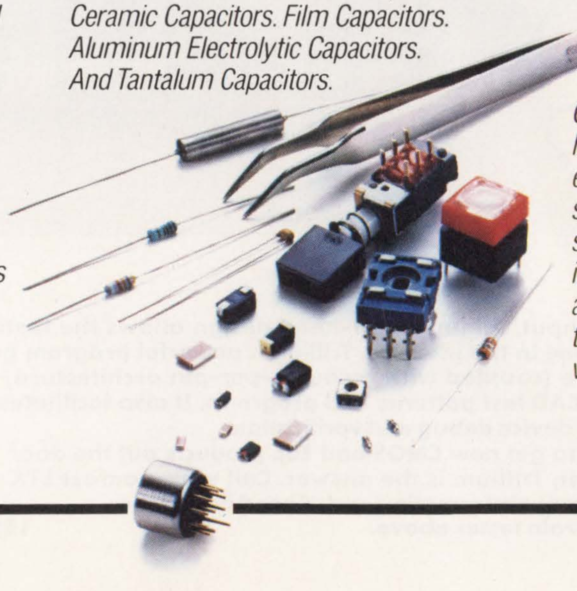
For example, we challenge you to find a supplier that can match Mepco/Centralab's wide selection of capacitors. Ceramic Capacitors. Film Capacitors. Aluminum Electrolytic Capacitors. And Tantalum Capacitors.



We also have a broad selection of resistors, including Thick Film Chip Resistors. Metal Film Resistors. Precision MELF Resistors. Nonlinear Resistors. And Trimming Potentiometers.

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EDITORIAL

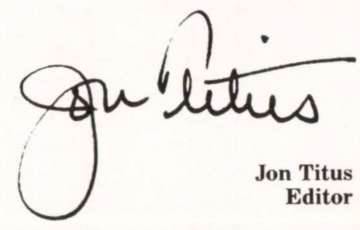
Expect the unexpected

Some time ago I noticed a slogan that someone had carefully painted on the sidewalk: "Expect a miracle." Well, it seems that miracles are few and far between. Although I hoped for one, no amount of expectation reduced my load of day-to-day work, nor did it lead to any great inspirations. The slogan reminds me of a cartoon I saw some time ago. Two researchers are looking at complex equations on a blackboard. Right in the middle there's the legend " . . . and then a miracle occurs."

Perhaps the phrases should have been "Expect the unexpected," and " . . . and then the unexpected occurs." For example, during the spring, my son's class was scheduled to take a field trip to one of Boston Harbor's many islands. Because other kids in his class were grumbling about the trip, he knew ahead of time that he'd hate the experience. So, at many dinners prior to the trip, we heard about how it was going to be "stupid" and "dumb." It turns out that he thoroughly enjoyed the visit and wants the whole family to go back with him during the summer.

I've wasted a lot of my own time worrying about how boring and "stupid" a meeting or trip was going to be only to find that, for the most part, it was interesting and informative. Even if the event turned out to be less useful than I had hoped, I usually found something positive that I hadn't expected. I tend to be a pessimist at heart, but I'm trying to change my attitude. My recent experiences confirm that optimists have more fun.

I'm not a complete optimist yet, because the unexpected has its negative side, too. For example, in early June, a bolt of lightning accidentally set off three rockets at NASA's Wallops Island, VA, facility. The rockets had their igniters in place and were awaiting launch. By a twist of fate, one of the rockets had been intended to help scientists study the effects of lightning on the ionosphere. Unfortunately, that rocket was set at a low angle, and it blasted into a body of water several hundred feet away. The other two rockets flew perfectly, but no one was set up to track them.



Jon Titus
Editor

THIS IS WHAT OUR NEW SRA

VLSI Part No.	Organization	Functions	Access Times
VT7C122	256 x 4	Separate I/O	15 ns
VT20C18	2K x 8	APD; 10 ns OE	20 ns
VT20C19	2K x 8	12 ns CE; 10 ns OE	20 ns
VT20C50	1K x 4	Separate I/O; FC	15 ns
VT20C68	4K x 4	APD	20 ns
VT20C69	4K x 4	12 ns CS	20 ns
VT20C71	4K x 4	Separate I/O; OT	20 ns
VT20C72	4K x 4	Separate I/O; HZ	20 ns
VT20C78	4K x 4	APD; 10 ns OE	20 ns
VT20C79	4K x 4	12 ns CS; 10 ns OE	20 ns
VT20C98*	8K x 8	APD	25 ns
VT20C99*	8K x 8	Fast CE	25 ns
VT62KS4*	16K x 4	15 ns CS	25 ns
VT63KS4*	16K x 4	15 ns CS; OE	25 ns
VT64KS4*	16K x 4	APD	25 ns
VT65KS4*	16K x 4	APD; OE	25 ns

APD=Auto Power Down; CE=Chip Enable; OE=Output Enable; CS=Chip Select; FC=Flash Clear; OT=Outputs Track Inputs During Write; HZ=High-Impedance Outputs During Write *Samples Available 4th Quarter, 1987.

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CIRCLE NO 62

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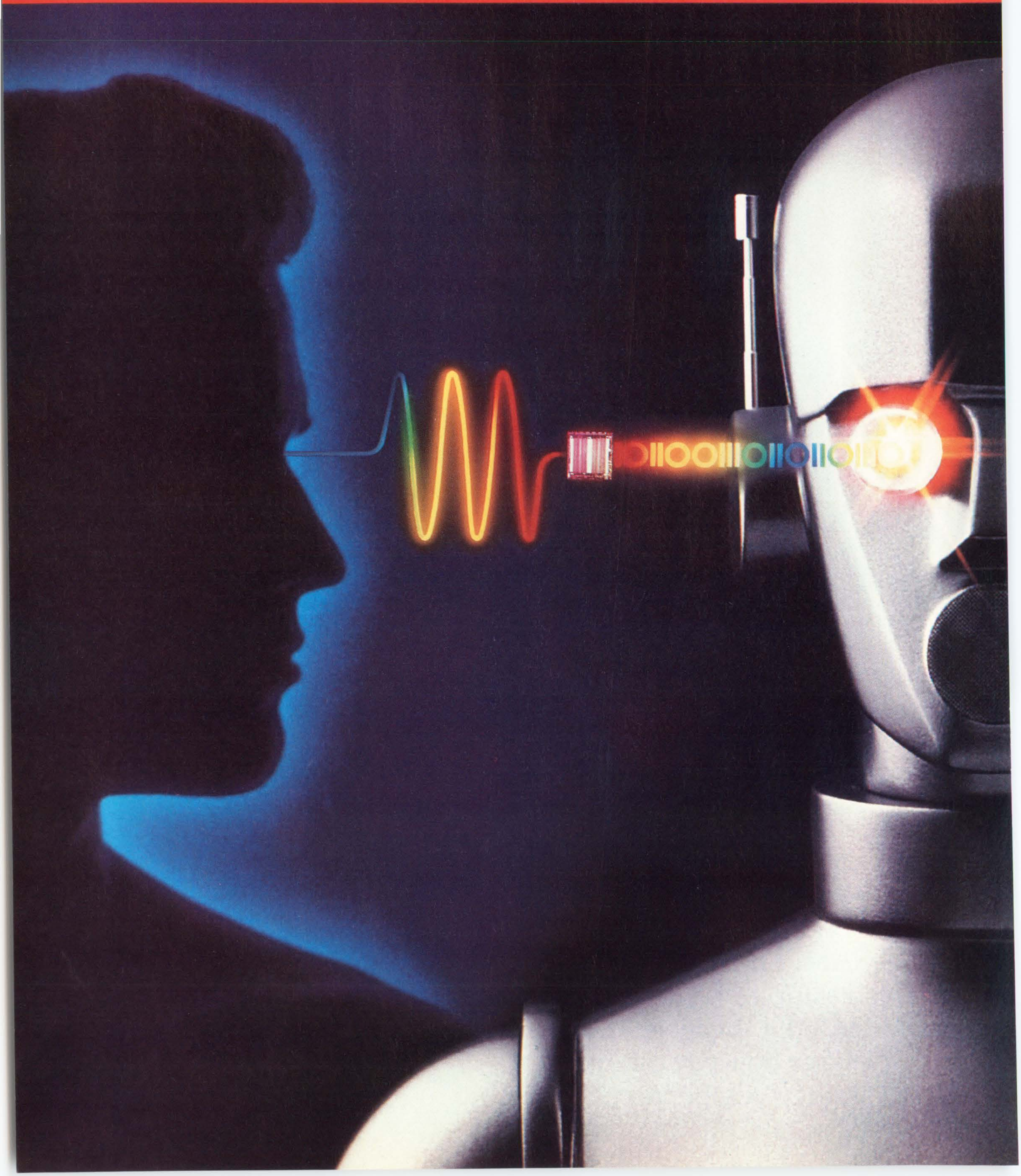

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ADC's	*Res. Bits*	*Conv. Rate Hz*	*Power Diss. (MW)*	*Pkg. Leads*	*1K Price*
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CA3306CE	6	10M	65	18	5.50
CA3306E/3306AE	6	15M	70	18	6.25/11.25
CA3318E/3318CE	8	15M	150	24	38.50/24.00
CA3310E/3310AE	10	150K	15	24	6.00/8.00
CDP68HC68A2E	10	10K	15	16	3.75
DAC's					
CA3338E/3338AE	8	50M	100	16	6.00/8.40
OP AMP	*UGBW Hz*	*Slew Rate (X10)*	*I_{OUT} MA*	*Pkg Leads*	*1K Price*
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*Typical propagation delay of 2-input NAND gate driving 1 internal load including 100μ interconnect.
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CIRCLE NO 61

Advanced engineering calculators perform sophisticated operations

Charles H Small,
Associate Editor

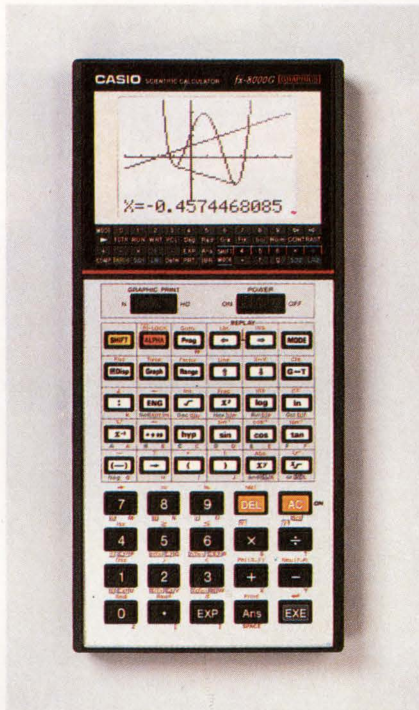
A recent survey by a calculator manufacturer revealed that design engineers have, on the average, five scientific calculators apiece. Even though the market for new calculators would seem to be more than saturated, all the major scientific-calculator makers are betting that engineers will add a sixth, top-of-the-line calculator to their flocks.

Casio, Hewlett-Packard, Sharp, and Texas Instruments have all recently introduced powerful scientific calculators with a host of intriguing new functions, features, and capabilities.

You can take for granted that these advanced, programmable calculators come with a full complement of scientific and engineering functions, including hyperbolic functions; single- and dual-variable statistical analysis; Boolean operations in binary, octal, and hexadecimal number bases; and conversion functions for both complex numbers and common English and metric units. These calculators have also benefited from general advancements in electronics—they now sport informative, eye-pleasing LCDs and low-power, CMOS circuitry.

You might well wonder, however, why you'd want to purchase one of these advanced models when you can get a perfectly serviceable, basic scientific calculator for less than $30, and when virtually every engineer has access to a personal or mainframe computer.

The answer is threefold. First, and quite simply, even though we are well into the computer age, the handheld calculator is still the engineer's primary, interactive, problem-solving tool. Second, the new advanced calculators provide important functions that basic calculators do not. Third, advanced calculators are becoming more and more computerlike in the way they operate and hence are not likely to be made obsolete by computers.



The $109.95 fx-8000G *from Casio has the largest LCD of any scientific calculator. The LCD can show long, complex command strings as well as graphs of functions.*

Computerlike calculators

The new, advanced calculators can perform sophisticated operations such as random-number generation, complex arithmetic, matrix mathematics, integration, and differentiation. The Hewlett-Packard HP-28C ($235) can even do symbolic math; it can rearrange, simplify, and solve equations for any variable and even do calculus.

Depending on the model, some advanced scientific calculators have the following computerlike features: high-level-language programmability, multiline displays, menus, typewriter-style (qwerty) keyboards, built-in subroutine libraries, graphics capability, off-line storage of programs, and printer and plotter interfaces.

One thing these calculators don't have that their less-complicated brethren do is shirt-pocket portability. With the exception of the 5⁵⁄₁₆-in.-tall Sharp Model EL-5200 ($109.95), none of the advanced scientific calculators in this article will fit into a typical shirt pocket without peeking over the top. Some, such as the Hewlett-Packard and Texas Instruments calculators, will not fit into a shirt pocket at all; perhaps they're best termed "suit-pocket portable."

Neither are these calculators in the same class as so-called handheld computers. Not long after the introduction of the scientific calculator, calculator makers also introduced calculator-size, handheld computers. These small computers differed from calculators in two ways: They lacked the calculators' built-in scientific functions, and you programmed them in an interpreted language such as Forth or Basic.

At first, the handheld computers were just a curiosity for the computer hobbyist and were not capable of much useful computing work. But one handheld, the Panasonic HHC, came with a Forth cross-development system. Armed with this system, OEM users wrote custom programs and hammered out a niche market for handheld computers as point-of-sale aids. For example, insurance and real-estate salesmen could use a handheld computer run-

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Handheld computers have evolved in parallel with scientific calculators. For example, Panasonic's latest model, the FH-2000, approaches the capabilities of a laptop computer and has a CMOS 8088 μP, 128k bytes of RAM and 512k bytes of ROM, and an 8-line×80-character LCD. With some changes to the source code, the unit can run programs written for the IBM PC. Despite their advancements, handheld computers remain devices that an engineer would design *in* rather than design *with.*

Basic-language programming

But advanced scientific calculators are incorporating one key feature of the handheld computers: Some now employ Basic-language programming rather than keystroke programming. The first programmable scientific calculators were keystroke programmable; that is, they had a memory that you could load with exactly the same series of keystrokes you'd use to evaluate a mathematical formula manually.

For a function that requires only one pass through the program—or series of keystrokes—keystroke programming is very straightforward because of its one-to-one correspondence with manual execution. But when a program requires decision-making branches and repeating loops, keystroke programming becomes less user friendly because of the quirky, arcane nature of the decision-making and looping constructs of the keystroke-programmable calculators.

Further, verifying a program after you had entered it into the older calculators was a tiresome, error-prone task because the machines' 7-segment numeric LED displays could not spell out the keys' mnemonics. Instead of mnemonics, the calculators would regurgitate encoded check digits.

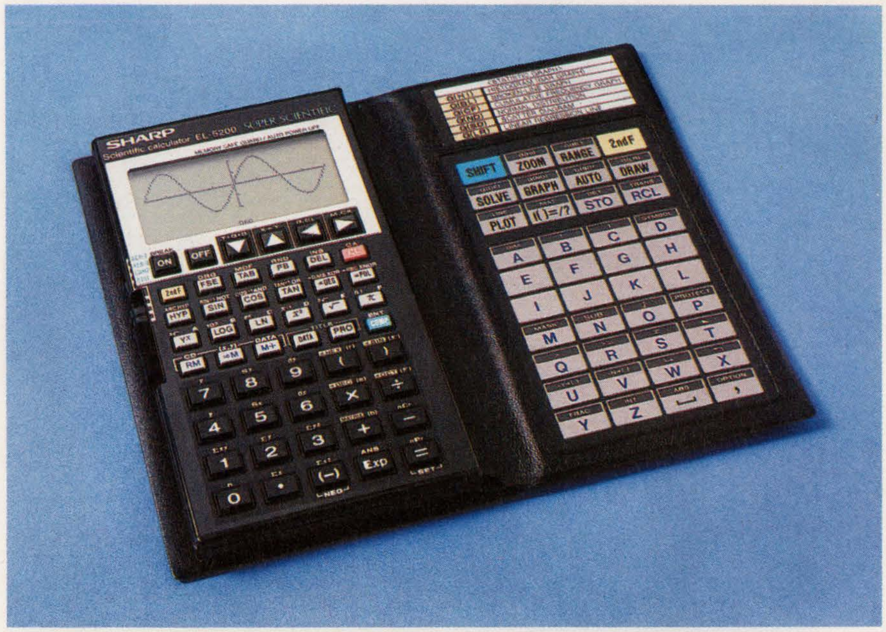
Now, one trend in advanced scientific calculators is to meld standard Basic programming constructs with the keystroke scientific functions. With these hybrid calculators, you can evaluate mathematical functions manually in the normal calculator fashion. Programming the calculators, however, doesn't mean you'll have to learn a new style of programming; you'll be able to use the Basic-programming skills you already have. As a plus, the flow of your programs will be somewhat easier for others to follow (and, for that matter, easier for you to follow when you try to regain understanding of a program you wrote in the past). Keystroke programming is hanging on in the US but has fallen into disfavor elsewhere in the world.

Whether they are keystroke or Basic programmable, virtually all new, advanced scientific calculators sport some form of alphabetic-character entry for naming programs and variables. Some have the alphabetic characters laid out in the standard qwerty format. Others have them in a less handy but more compact rectangular array in alphabetical order. Still others allow you to enter alphabetic characters as shifted, or second, functions. This last scheme results in the most compact keyboards but proves the least handy to use.

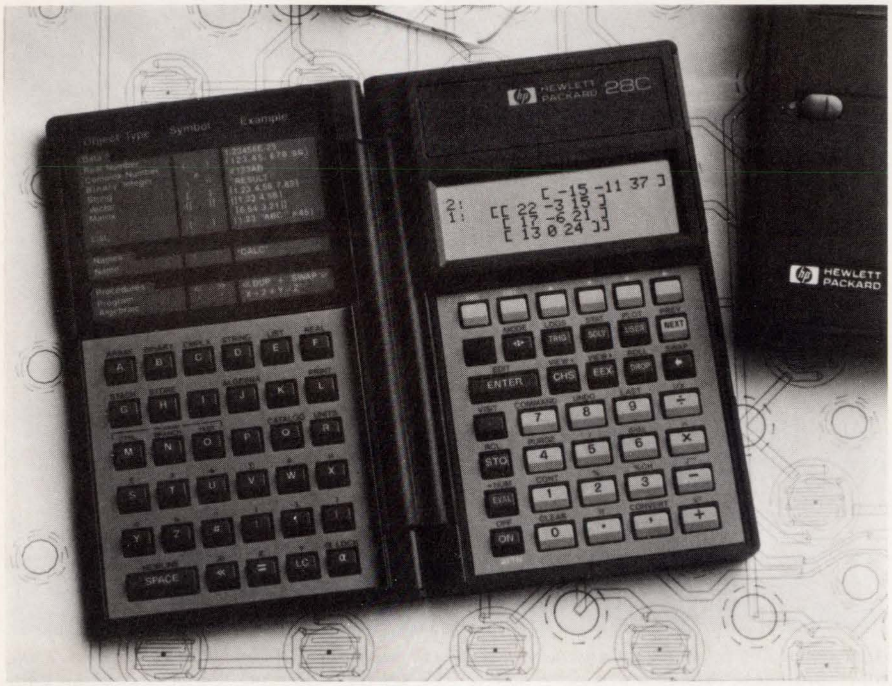
However, the issue of handiness is somewhat moot for punching text strings into a calculator. Although one model, the Casio fx-8000G ($109.95), can store text files, no one will ever be foolish enough to use a calculator for word processing. And, following a trend started by the Sinclair personal computer (which had a miserable, hard-to-use membrane keyboard), all programmable calculators provide one-stroke keys for common programming constructs and scientific-function calls. Therefore, you don't have to do as much typing to enter a program into a calculator as you would if you were entering your program into a file for compilation or interpretation on a computer.

The longest string of alphabetic characters you would typically enter would be a program's title. The next longest strings would be variable names. In either case, the ease of use of the various keyboards would probably not have a significant effect on the total time you would spend writing, entering, and debugging a program.

In addition to having alphabetic



A powerful Zoom key for manipulating graphs *is one feature of the $109.95 Sharp EL-5200. Other graphical calculators require you to call up and alter the Range menu for scale changes.*



To help you access its more than 250 built-in functions, *the $235 Hewlett-Packard HP-28C provides an extensive series of menus.*

keys, advanced scientific calculators are becoming more computerlike in other ways. Take, for example, the Casio Model fx-850P ($149.95). This calculator is laid out in a horizontal format with a numeric keypad and scientific keys occupying the rightmost third of the calculator. On the left is a miniature qwerty keyboard; the shifted functions of the qwerty keyboard include common Basic keywords. Thus, the fx-850P is indeed a hybrid of the scientific calculator and the handheld Basic computer.

Calculator has 1M-byte ROM

Basic programming isn't this calculator's only computerlike feature. Remarkably, the fx-850P comes with a huge (1M-byte) internal ROM that stores 116 scientific programs. You can use these programs just as you'd use the scientific-subroutine libraries of mainframe computers.

Similarly, the Texas Instruments Model TI-74 Basicalc ($135) has a qwerty keyboard and shifted functions for Basic keywords and scientific functions. However, when you press the Mode key, the alphabetical keys become scientific-calculator keys. Thus you have your choice, in one unit, of a handheld Basic computer with scientific functions or a conventional scientific calculator.

In addition to picking up the keyboards and programming languages of computers, calculators are also getting more computerlike displays. The Sharp Model EL-5150 ($79.95) is a new, low-cost entrant in the firm's line of programmable calculators. It sacrifices the qwerty layout and Basic keywords for a larger display than that of its cousins, Models EL-5500III and EL-5520. Just like a computer's graphics terminal, the calculator displays equations in algebraic form with true superscripts for powers and standard mathematical symbols (HP and TI calculators still use Fortran-like conventions for mathematical symbols). The Casio fx-8000G prints the characters A through F in one typeface when you use them in names and another typeface when they signify hex numbers.

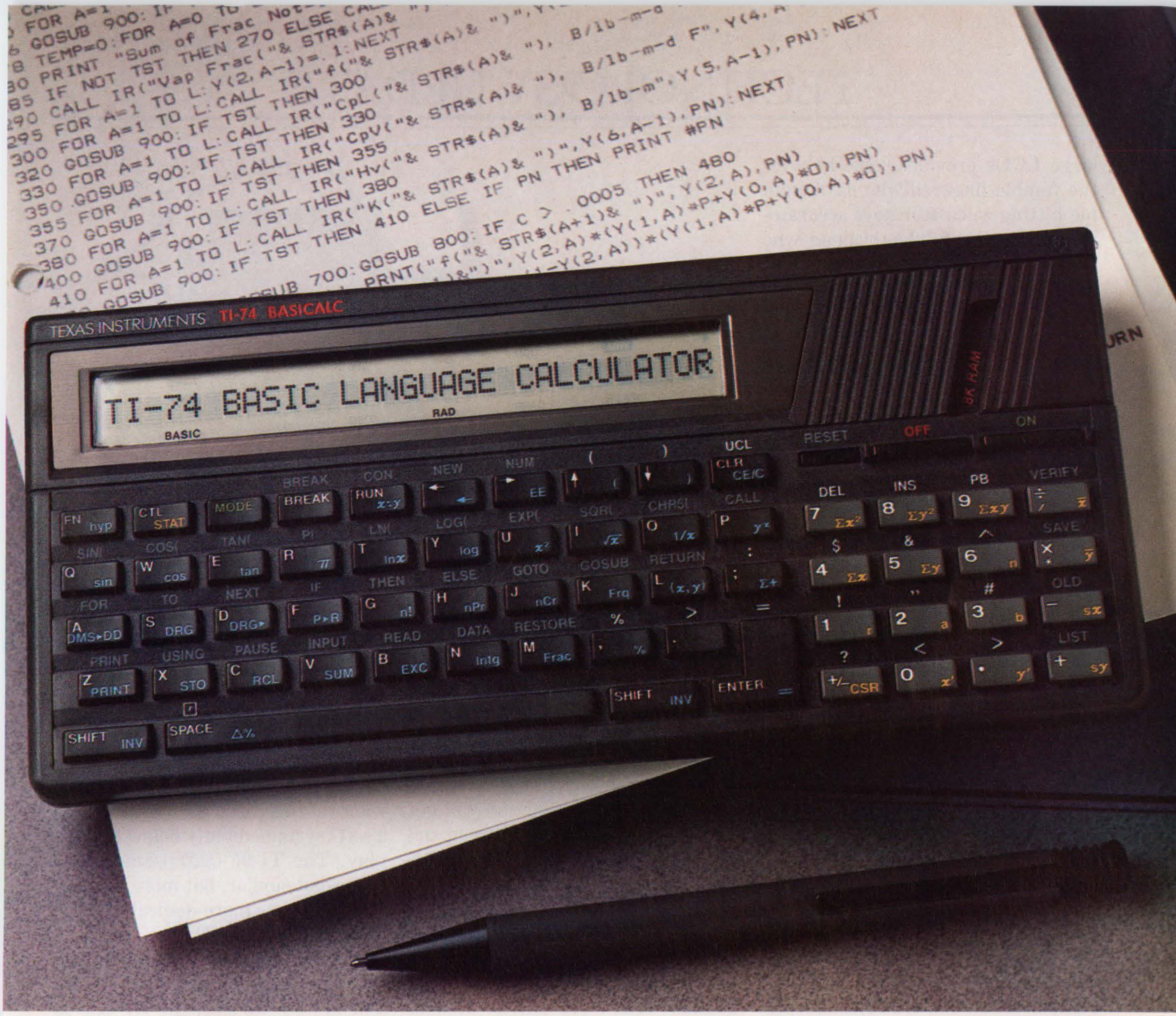
Advancements in calculator displays don't stop with mere mathematical symbols and Greek letters. Three new calculators, the Casio Model fx-8000G ($109.95), the Hewlett-Packard HP-28C ($235), and the Sharp Model EL-5200 ($109.95) feature large, multiline LCDs having graphics capabilities. The fx-8000G (like the company's earlier $79.95 fx-7000G) offers 16 characters×8 lines or 96×64 pixels. The HP-28C has 23 characters×4 lines or 137×32 pixels. The EL-5200 shows 16 digits×4 lines or 96×32 pixels.

These dot-addressable LCDs offer two capabilities that you formerly could get only from a computer. First, they let you draw a graph of any function you can key in. The calculators have functions for plotting points, for drawing straight lines, and for graphing several functions and determining their intersections. Further, the Sharp EL-5200 has dedicated keys for scrolling and zooming the display. You can invoke these keys manually or in a program. (To change the scale of Casio's and HP's displays, other than by a fixed multiplier or factors of two, you must call up and alter the Range menu and then rerun the graphing routine.)

Only time will tell whether or not the ability to quickly view a graph of a function is really a valuable tool for engineers or is just a gimmick. With the notable exception of software engineers, most engineers employ a wide variety of visual design aids such as pole-zero plots and Smith charts. These aids allow an engineer to go back and forth between the analytical realm and the real world. Perhaps engineers find such tools useful because, as brain research indicates, the creative half of the brain thinks in visual terms while the analytical half works syntactically.

Thus, perhaps the ability to jump from the inherently syntactical, analytical world of the calculator, with its precisely ordered strings of commands, into the visual domain of graphed functions will prove to be a surprisingly powerful aid to an engineer's creativity.

The other benefit conferred by



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large LCDs provides some help for the fumble-fingered who have trouble hitting calculator keys accurately and for the fumble-brained who can't get formulas or programs right on the first pass. Whereas most calculators display only the present results of the operation last invoked, the fx-8000G, HP-28C, and EL-5200 can retain and display an entire string of commands on their large, multiline displays. The calculators have editing keys for moving the cursor around in the command line, and they have inserting and deleting functions. Thus, you can go back and alter the string before you execute it. And, if you don't like the result of the calculation, you can recover the command string and data, alter them further, and rerun them. (The HP-28C can also operate in the immediate mode, as a conventional calculator does.)

This command-string mode of operation and these editing capabilities make entering complex functions and programs in this calculator much easier than it was in earlier calculators that did not capture your command line or support simple editing functions. The HP-28C has one further computerlike trait: a single-stepping command in its program-control menu for troubleshooting programs.

Menus and softkeys

An additional way in which scientific calculators are becoming more like computers is that many of them are now menu controlled, and many also provide some softkeys instead of having a dedicated key for each function. Very early in their development, scientific calculators acquired more functions than could possibly be handled by the maximum number of dedicated keys that could fit on a control panel of reasonable size. Soon each key had to do double duty—it had a primary function that you got with a single keystroke and a "shifted" function that you got by preceding the keystroke with the press of a shift or a second function key.

***The $200 TI-95** from Texas Instruments requires only a simple connecting cable to drive its companion printer ($115). The calculator also accepts preprogrammed ROM cartridges containing applications programs or constant-memory cartridges for storing user programs and data.*

The Casio fx-8000G provides an extreme example of this form of control. Some of its keys have five functions. Which function you get depends on the mode you are in and whether you precede a keystroke with a shift-key or alpha-key keystroke.

HP and TI have chosen to make their newest control interfaces more like menu-driven computer programs. The HP-28C's keypad doesn't have many of the math keys you'd expect to find on a scientific calculator. It has only eight math keys—four basic mathematical operations and four simple, shifted math functions. The keyboard has no keys for common scientific functions such as trigonometric or logarithmic operations. It does, however, have an equals sign (earlier scientific calculators from HP did not). The HP-28C gives you the option of entering functions algebraically as well as in the company's classical reverse Polish notation.

Before you can use most of the mathematical, graphical, or editing functions of the calculator, you must first summon the appropriate menu. For example, before taking the sine of an angle, you must first press the Trig button. After you've pressed the Trig key, a series of five choices appears across the bottom of the display. You invoke the function you want (in this case, sine) by pressing a softkey immediately below the display. The TI-95 ($200) employs a somewhat similar, but more limited, scheme; it has more dedicated function keys than the HP-28C does.

The HP-28C's designers had no choice but to employ this menu scheme. For its size, the HP-28C is probably the most complex object ever made by man. The calculator has far more functions than any other calculator—too many functions to employ dedicated keys for each one. Mechanically, the process of selecting a menu with one key and then using a softkey to get the function you want from the menu is identical—at least in the number of keystrokes—to pressing a shift key and a function key. Conceptually, though, the two schemes are significantly different.

To use the shifted-function approach, you need only learn your way around your calculator's keyboard. To use the HP-28C's menu approach, you must learn the hierarchy that the calculator's designers imposed on its collection of func-

The press of a button *switches the Texas Instruments $135 TI-74 from a handheld Basic computer with scientific functions to a scientific calculator.*

tions. Like many complex applications programs, the HP-28C has a Help menu with an entry for each of its functions and commands.

Optional printers

Just like real computers, most scientific calculators can give you a printout. But their optional printers have two drawbacks. First, they are generally noisy, slow, and somewhat troublesome to program. Second, some require extra interface boxes. The HP-28C has the simplest link to its printer. It uses an infrared LED to send a print file to its Model HP-82240A printer ($135) and requires no connecting cable.

The Sharp EL-5200 and the Texas Instruments TI-74 and TI-95 need only a single cable to link the calculator and printer. The Sharp Model CE-50P printer costs $124, and the TI Model PC 324 printer costs $115. The Casio calculators require an interface unit between calculator and printer. For example, the fx-8000G requires the $69.95 Model FA80 interface. The Casio Model FP40 printer costs $139.95. Casio's graphics calculators can also drive the $399.95 Model FP-100 plotter.

The latest scientific calculators offer nothing really new in the way of storage of programs and data. The cleanest solutions for storing user programs and data are the constant-memory cartridges that some Texas Instruments and Sharp calculators employ. (The TI cartridges cost $50; Sharp's are $45 to $125.) These calculators have a rudimentary file-management system that allows you to store and retrieve your programs from the cartridges. Continuing the long-standing tradition of ROM packs, the TI calculators also accept preprogrammed, $45 ROM cartridges that contain routines for various specific applications such as mathematics and chemical engineering.

With the aid of the appropriate interface units, you can also store programs for Casio, TI, and Sharp calculators on common cassette recorders. The Model FA80 cassette/printer interface for the Casio fx-8000G costs $69.95. The TI cassette interface costs $35. The Sharp CE-50P printer ($124) also incorporates a cassette interface. The Hewlett-Packard HP-28C has no provision for external storage.

These calculators vary widely in the amount of internal storage they offer. The Casio fx-8000G can store 10 programs (having a total of 1446 steps) internally. The Hewlett-Packard HP-28C has 1650 bytes of user memory and is not intended to replace the company's HP-41, which does offer off-line storage of large program libraries and data files.

The Sharp EL-5200 can store 99 formulas having a total of 5120 steps; the Model EL-5150 stores 99 formulas having 1454 total steps. Finally, the Texas Instruments Models TI 95 and TI 74 each have an 8k-byte memory that you can partition at will among file space, program steps, and data registers. You can expand the memory with an 8k-byte constant-memory cartridge. **EDN**

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For more information . . .

For more information on the calculators described in this article, circle the appropriate numbers on the Information Retrieval Service card or contact the following manufacturers directly.

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Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div	2 mV/div
Trigger Frequency	500 MHz	500 MHz	500 MHz	500 MHz	250 MHz
GPIB	Standard	Standard	Standard	Optional	Optional
Counter/Timer/Trigger/Word Recognizer	Standard	Standard	Standard	Optional	Optional
Digital Multimeter	Standard	Standard	Not Available	Optional	Optional
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Probes	4	4	4	2	2
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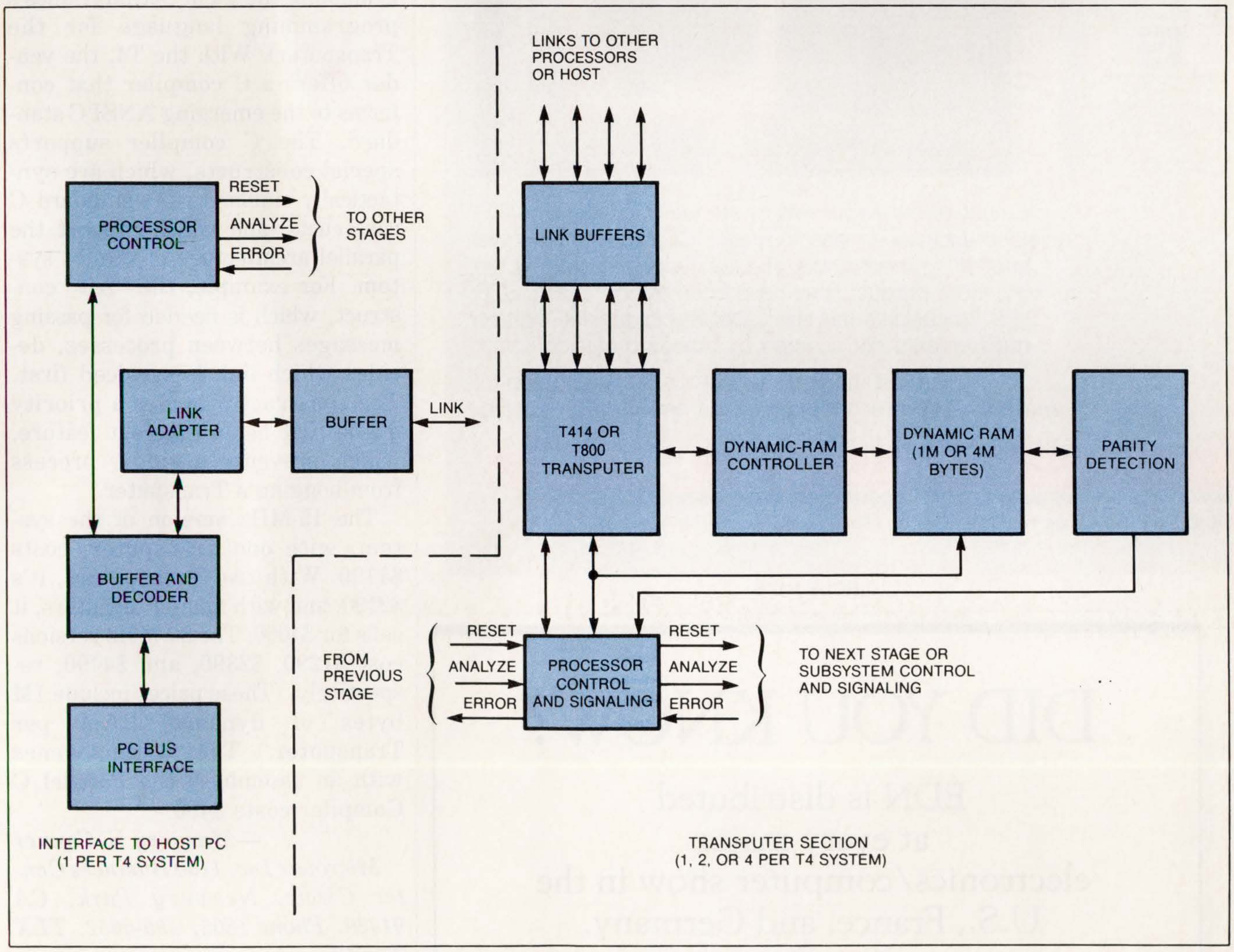
Transputer-based PC add-in board supports programming in C

With the T4 add-in board, you can develop parallel-processing applications on an IBM PC or compatible computer. The board comprises four processor sections, each containing an Inmos Transputer and 1M, 2M, or 4M bytes of dedicated dynamic RAM.

A program running on a parallel system typically comprises several processes, each operating on a separate processor, and is capable of interprocess communications. The Transputer performs these interprocess communications through four on-chip hardware links. The links perform high-speed (10M or 20M bps) serial data transfers between Transputers when necessary. The software can direct any process to send data to or receive it from any other process. Each Transputer has four links that connect to externally accessible pinouts, so you can connect the Transputers in a variety of parallel architectures, such as ring or hypercube configurations. In a system with multiple T4 boards, you can link Transputers between boards.

The initial version of the board uses a T414 Transputer that operates at 15 or 20 MHz and that's capable of an instruction throughput of 10 MIPS. The chip has a linear address space of 4G bytes, of



***The host-interface section of the Transputer-based T4 PC add-in board** receives data from the PC bus and passes it to the board's four Transputer sections over high-speed serial links. You can connect the links among the Transputers either on the same board or on multiple T4 boards, so you can configure parallel architectures, such as ring or hypercube configurations.*

which 2k bytes is 20-nsec internal memory. It's this fast workspace memory that lets the Transputer perform rapid context switching. Instead of having to store all of its register states when it switches tasks, the Transputer merely changes a pointer in the workspace; the pointer tracks the section of memory that holds a particular set of registers.

The vendor will offer to retrofit the T4 with the more powerful T800 version of the Transputer as soon as Inmos begins shipping it in production quantities. The T800 incorporates a floating-point unit and has 4k bytes of on-chip, 20-nsec dynamic RAM.

You have an alternative to programming the T4 in Occam (Inmos's programming language for the Transputer). With the T4, the vendor offers a C compiler that conforms to the emerging ANSI C standard. The C compiler supports special constructs, which are syntactically similar to the standard C constructs and which support the parallel architecture of the T4 system. For example, the "Alt" construct, which is needed for passing messages between processes, decides which link is serviced first. The construct provides a priority queue that has a time-out feature, which prevents a single process from hogging a Transputer.

The 15-MHz version of the system, with one Transputer, costs \$1190. With two Transputers, it's \$2190, and with four Transputers, it sells for \$4090. The 20-MHz versions cost \$1290, \$2390, and \$4490, respectively. (These prices include 1M bytes of dynamic RAM per Transputer.) The system comes with an assembler; the Parallel C Compiler costs \$495.

—Margery S Conner

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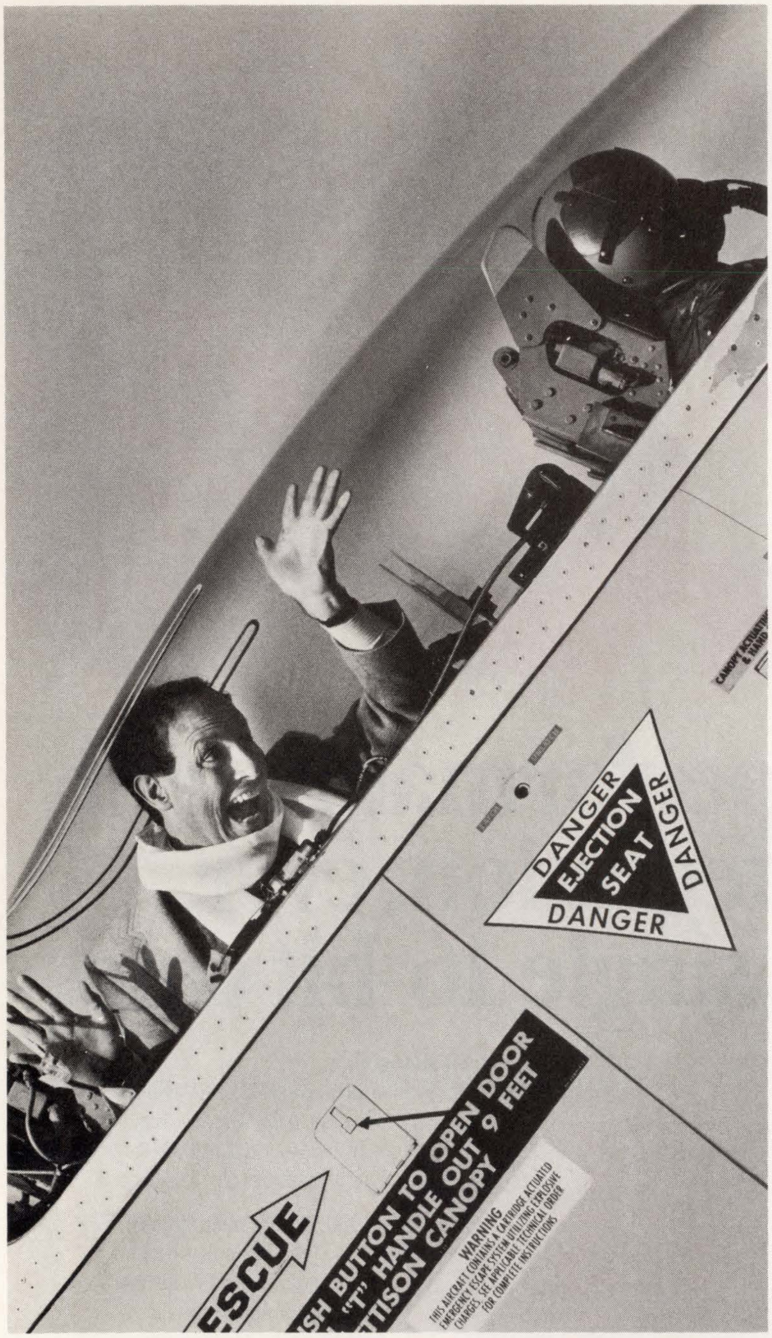

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*All execution speeds are real-world, not theoretical, and include overhead times.

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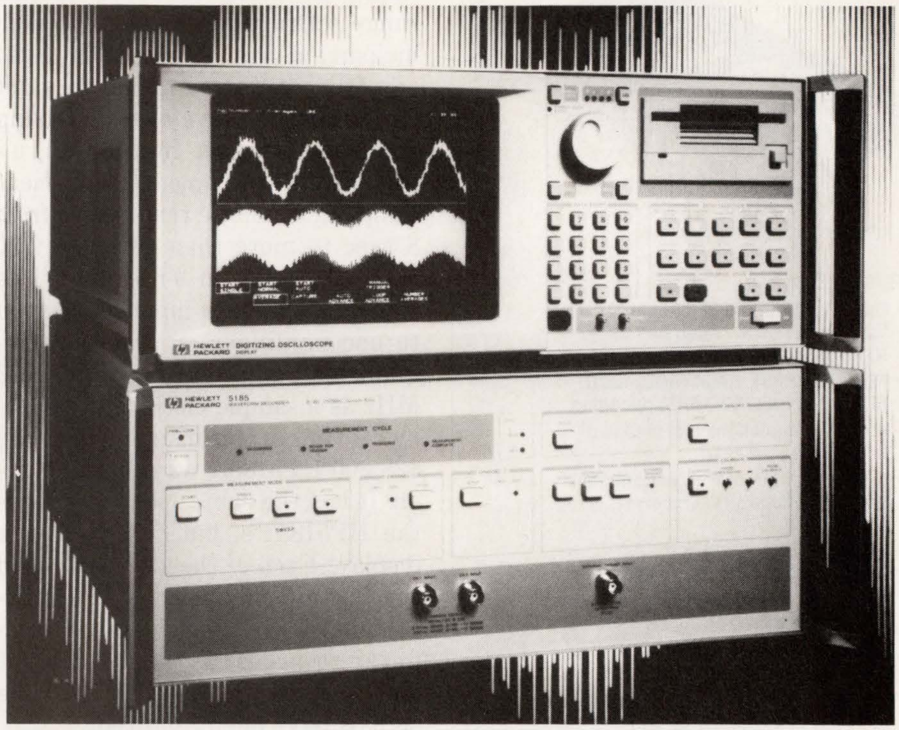
Trio of digitizing oscilloscopes features high bandwidth, deep memory

Three digitizing oscilloscopes—the HP5185T, HP54112D, and HP-54120T—can cater to almost all your high-bandwidth and deep-capture measurement needs. Each of the three instruments focuses on different measurement requirements (see **Table 1**). The HP5185T precision digitizing oscilloscope/waveform recorder provides the high resolution and variable digitizing rate you expect from a waveform recorder and also performs frequency-domain signal analysis. Although it has nearly the same input bandwidth, the HP54112D offers twice as many channels as the HP5185T does, but at a little more than half the price. For extremely high-frequency (to 20 GHz), repetitive measurements, the HP54120T offers high-resolution signal digitizing on four input channels.

With its high-resolution A/D converter, deep memory, and complex triggering capability, the HP5185T precision digitizing oscilloscope captures extensive information about a signal. The deep memory improves the instrument's ability to perform an FFT on the sampled waveform. In addition, the digital scope can compute and display a signal's power and phase spectra. Each input channel has two adjustable trigger levels for internal triggering.



One member of a family of three digitizing oscilloscopes, *the HP5185T features high-resolution digitizing on two input channels at rates to 250M samples/sec, and it captures 64k samples/channel.*

You can use these two levels to create a hysteresis window that prevents noise from accidentally triggering data capture, to create a "bi-trigger" window that triggers data capture when a signal deviates either above or below a set voltage, to create "posneg" trigger levels that start data capture only when a signal has crossed both trigger levels (regardless of the order of the crossings), or to create a dropout trigger that starts data capture when a signal is either above or below the trigger level for a specified length of time. A program-

TABLE 1—KEY SPECS FOR THREE DIGITIZING SCOPES

MODEL	REPETITIVE BANDWIDTH (MHz)	SINGLE-SHOT BANDWIDTH (MHz)	SAMPLE RATE (MHz)	RESOLUTION (BITS)	CHANNELS	SAMPLES/ CHANNEL	PRICE
HP5185T	110	110	250	8	2	64k	$40,000
HP54112D	100	100	400	6	4	64k	$22,900
HP54120T	2000	N/A	*	12	4	1k TO 10k	$27,850

NOTE: N/A=NOT APPLICABLE
*SEE TEXT

mable delay allows you to postpone the start of data capture by as many as 1M samples. The scope also has an external-trigger input.

Each channel of the HP5185T provides nine full-scale input ranges from ±50 mV to ±20V, and you can define as many as three custom range settings for frequently taken measurements. A gated timebase allows an external signal to start and stop the waveform digitizing after the trigger. In addition, although the instrument has a linear sampling timebase that ranges from 8 nsec to more than 490 μsec (250 MHz to 2 kHz) in 8-nsec steps, its external timebase input allows you to use nonlinear or precision frequencies ranging from dc to 250 MHz as a sample clock. The company also offers this instrument as the $28,200 HP5185A waveform digitizer: It has the same specifications as the HP5185T's, but doesn't have a display. Each of the two versions of the instrument includes an IEEE-488 interface that allows a host computer to program the instrument and to read the samples after the signals have been captured.

Although some of its specifications resemble those of the HP5185T, the HP54112D digitizing oscilloscope is quite a different instrument. It has two bits less vertical resolution, twice as many channels, and costs a little more than half the price. The HP54112D does not have the HP5185T's frequency-domain-calculation capability or its dual internal triggers for each channel, but it does share the HP5185T's ability to compute and display other signal attributes, including frequency, period, pulse duration, rise and fall times, and signal rms voltages.

The HP54112D digitizes signals at rates from a blazing 400 MHz to a snail-like 50 sec/sample. Its input-channel ranges span ±5 mV/div to ±5V/div. Each input has one trigger level, and the instrument accepts an external trigger applied to a rear-panel input connector. In addition, it has a pattern trigger that allows you to use the four analog input channels plus the external trigger input as a 5-bit logic trigger. A trigger delay allows you to hold off the start of data capture by as many as 16M trigger events. The scope's color display makes the multiple signal traces easy to identify: The scope ties numeric information on the display to the associated trace by displaying the numbers in a matching color.

For very-high-frequency analysis, the HP54120T digitizing oscilloscope features a 20-GHz repetitive-signal bandwidth on its four input channels. The company rates the scope's timebase as having 0.25-psec resolution and 10-psec accuracy. Because the instrument uses a sequential sampling technique that acquires only one sample per trigger, it does not perform single-shot measurements. In fact, the scope digitizes at a typical sample rate of 4500 Hz and has a maximum sample rate of 10 kHz. Its input channels have no trigger levels; you must use the instrument's 500-MHz external trigger input.

In addition, the 50Ω input channels have no input attenuators. The full-scale input range for all channels is ±320 mV. To reduce larger signals, you use fixed, external attenuators that you screw onto the channel's 3.5-mm input connectors. The company offers HP33340C Series fixed attenuators for $248 each; they offer attenuation of 0 to 40 dB. An external enclosure houses the input channels and trigger input, allowing you to place the input connectors close to the circuit you're testing so you can minimize the lengths of the test cables. At the very high frequencies the HP-54120T can capture, you need the shortest possible cable runs. The input head contains fast S/H circuits with filtering, so only low-frequency analog signals pass back to the instrument's mainframe, where the digitizing is performed.

Above 1 GHz, you'd normally pipe signals around a system by using

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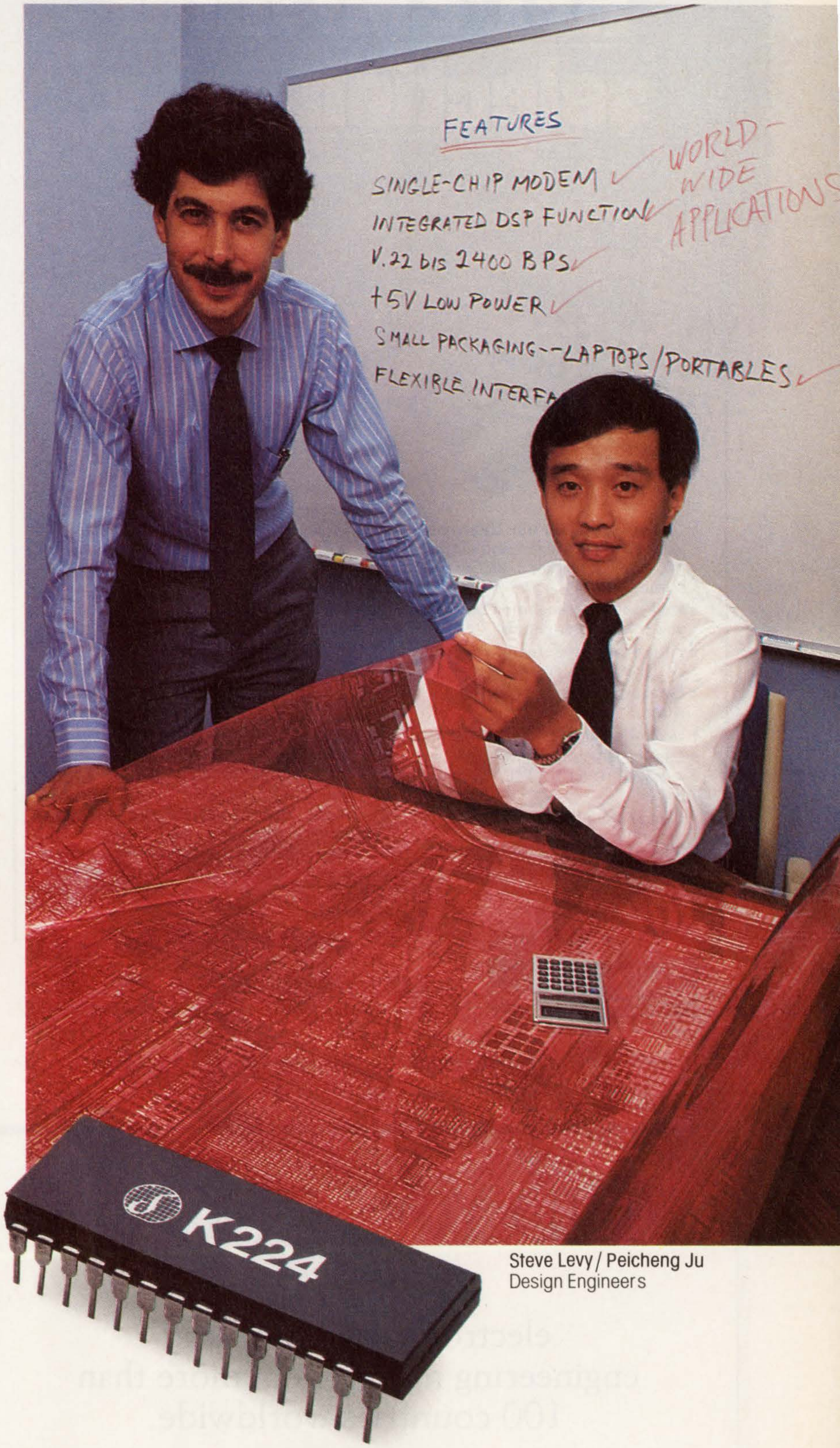
For more information on the SSI K224, or the complete K-Series family of compatible modem IC's, contact: **Silicon Systems**, 14351 Myford Road, Tustin, California 92680.



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coaxial cable and connectors. That procedure is often inconvenient for troubleshooting purposes, because the nodes you'd want to probe are generally not those that are conveniently attached to a connector. The company offers the Model HP-54006A, a passive, 6-GHz divider probe, for $895. The probe allows you to explore very-high-frequency circuits when a coaxial hookup isn't available. The probe operates the way a regular scope probe does, but at much higher frequencies. It has interchangeable resistors, which give it attenuation of either 10:1 or 20:1.

A time-domain reflectometer (TDR) built into channel 1's input allows you to perform reflectance and impedance tests on circuit traces and cables. The HP54120T's onboard μP allows you to null the effects of your test jig by pressing a button, so that only information pertaining to the circuit under test is displayed. With the TDR, you can explore the effects of stubs and impedance mismatches on ECL and GaAs pc-board traces.

The HP54120T features the color display and computation capabilities of the HP54112D and adds time and voltage statistics and histograms. You can use these histograms to determine jitter and noise on repetitive signals, a measurement traditionally made on analog scopes by subjectively judging the intensity of the shades in a smear of traces. At a single keystroke, the HP54120T calculates and displays the mean and standard deviation of time or voltage for several cycles of the digitized signal.—***Steven H Leibson***

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Circle No 649


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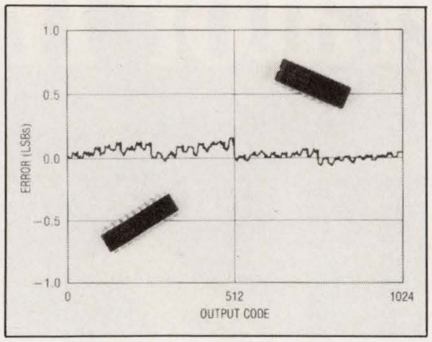
Data-acquisition chip contains 10-bit ADC, S/H circuit, and multiplexer

The LTC1090 data-acquisition system contains a 10-bit A/D converter, an S/H circuit with a 1-μsec acquisition time, and an analog input multiplexer, all on a single piece of silicon packaged in a 20-pin DIP. The secret of the low pin count is the device's full-duplex, serial μP interface. Selected versions of the part feature a total unadjusted error of ±0.5 LSB over the full operating temperature range.

You can configure the analog input multiplexer as eight single-ended inputs, four differential inputs, or a combination of single-ended and differential inputs by means of the chip's 8-bit input data word. This data word selects a multiplexer input channel, picks single-ended or differential operation for the selected analog input, sets the polarity of the input pins for a selected differential-input pair, selects unipolar or bipolar A/D operation, defines the output word width, and determines whether the LSB or the MSB of the conversion will emerge first from the serial output. The internal S/H circuit operates only for single-ended conversions.

An on-chip, 10-bit, switched-capacitor D/A converter; a comparator; and a successive-approximation register form the A/D converter. You can select either 10-bit unipolar or 9-bit-plus-sign bipolar conversions by means of the chip's serial input data word. A conversion requires 20 μsec. The total unadjusted error for either the unipolar or the bipolar conversion mode over the device's full temperature range is ±0.5 LSB for the LTC1090A and ±2 LSB for the LTC1090. The LTC1090CN, in a plastic package and rated for −40 to +85°C operation, costs $11.95 (100). A similarly



Each of these 20-pin DIPs houses a complete data-acquisition system *comprising an analog input multiplexer, an S/H circuit, a 10-bit A/D converter, and a serial I/O port. The manufacturer rates the part's total unadjusted error at ±0.5 LSB for selected devices.*

packaged LTC1090ACN costs $18.95 (100).

The A/D converter has ratiometric, differential reference inputs, so you can use any reference voltage and polarity that suits your application. When the reference voltages are low (around 0.5V), a charge-injection offset voltage becomes significant and can result in an error of about 0.5 LSB. However, this offset is proportional to the power-supply voltage and is not sensitive to temperature, so a software routine that runs an automatic calibration on a grounded input can null this error. For reference voltages around 5V, the offset voltage causes only about 0.1 LSB of error and therefore won't affect readings.

Because the device allows you to program unipolar or bipolar operation, you can achieve 11-bit resolution with this device by using a technique the company calls "Sneak-a-Bit." By performing two unipolar, 10-bit conversions and switching the polarity of the differential inputs between the two conversions, a software routine can assemble an 11-bit representation (composed of a 10-bit magnitude and a sign bit) of the analog signal.

To accommodate 4-, 8-, and 16-bit μPs, the manufacturer designed a variable word width into this device. You can select 8-, 10-, 12-, or 16-bit output data words, and you can decide whether the LSB or MSB of the data word will be shifted out of the serial port first. This latter feature allows the part to interface directly with Motorola's SPI and National Semiconductor's Microwire serial μC ports, which require data output to take place MSB first, or Hitachi's SCI and Texas Instruments' TMS7000 μC ports, which want the LSB first.

For applications for which the 8-channel multiplexer and 20-pin package are too large, the company offers the LTC1091CN8 and LTC1091ACN8, which are 2-channel versions of the data-acquisition system in an 8-pin DIP. You can use the analog channels as two single-ended or one differential input. The LTC1091ACN8 has a maximum unadjusted error of ±0.5 LSB, and it costs $15.80 (100). The LTC1091CN8, which has a relaxed specification for total unadjusted error, costs $10.95 (100).

—Steven H Leibson

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035. Phone (408) 942-0810. TLX 172110.

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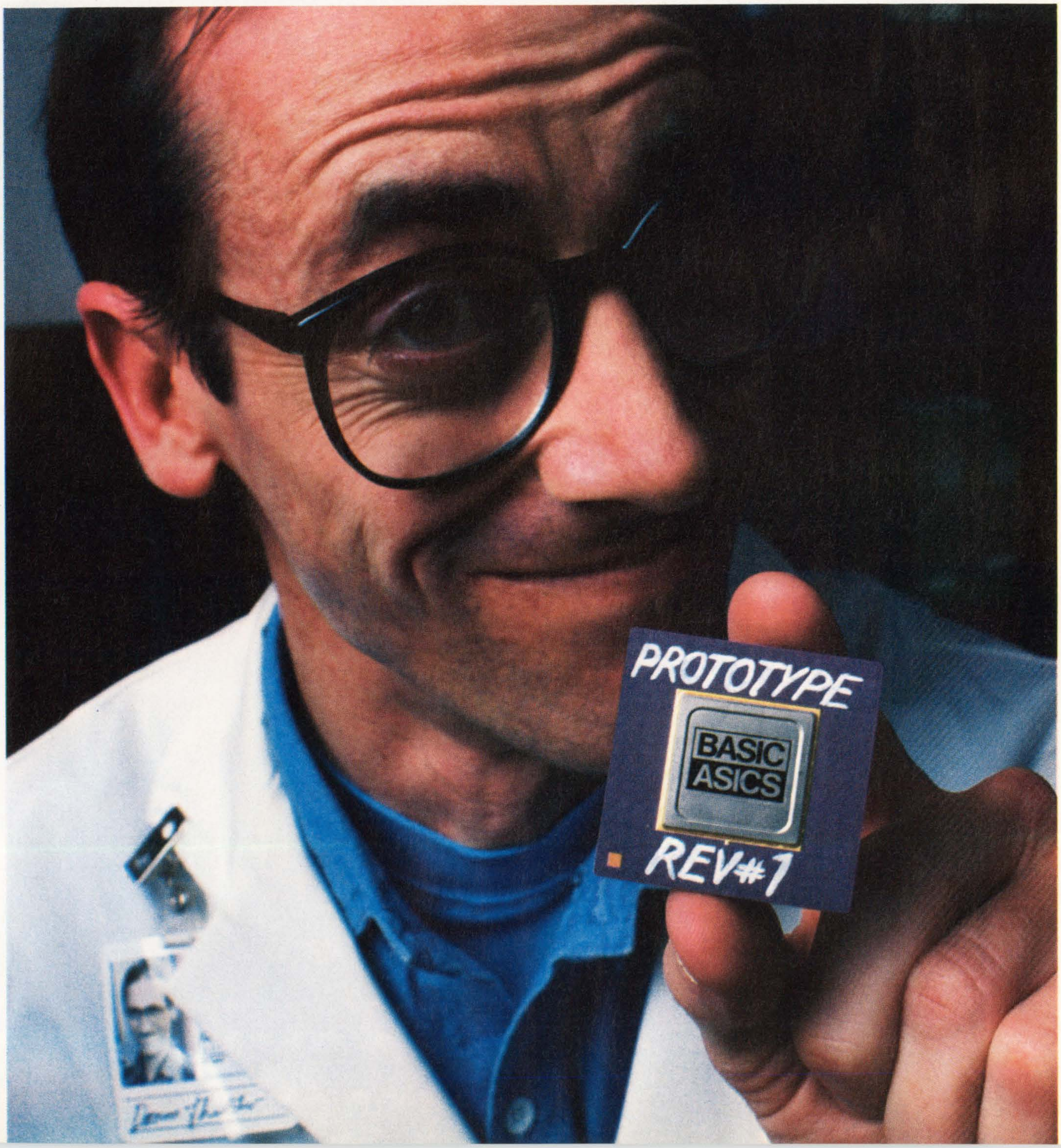

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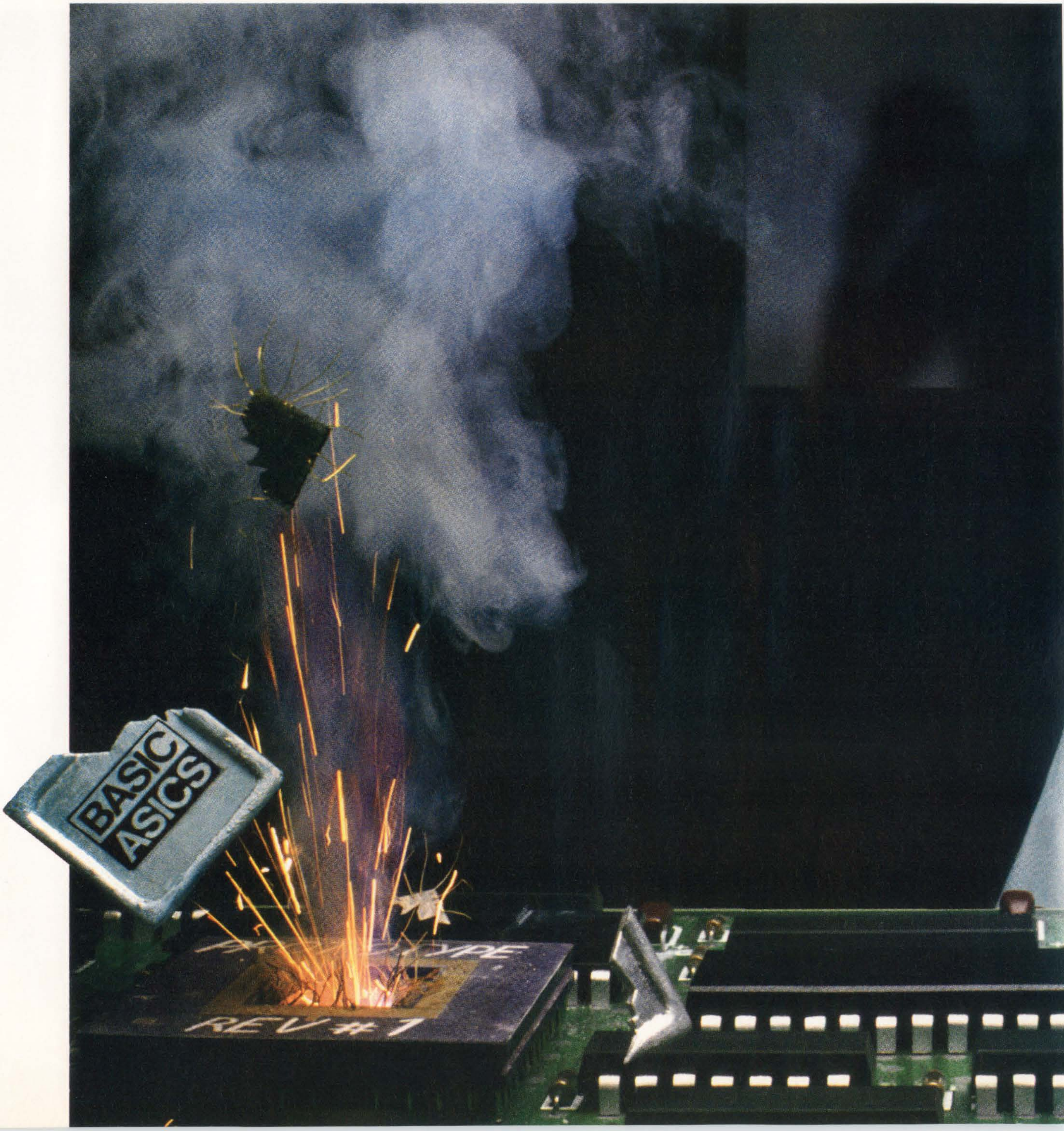

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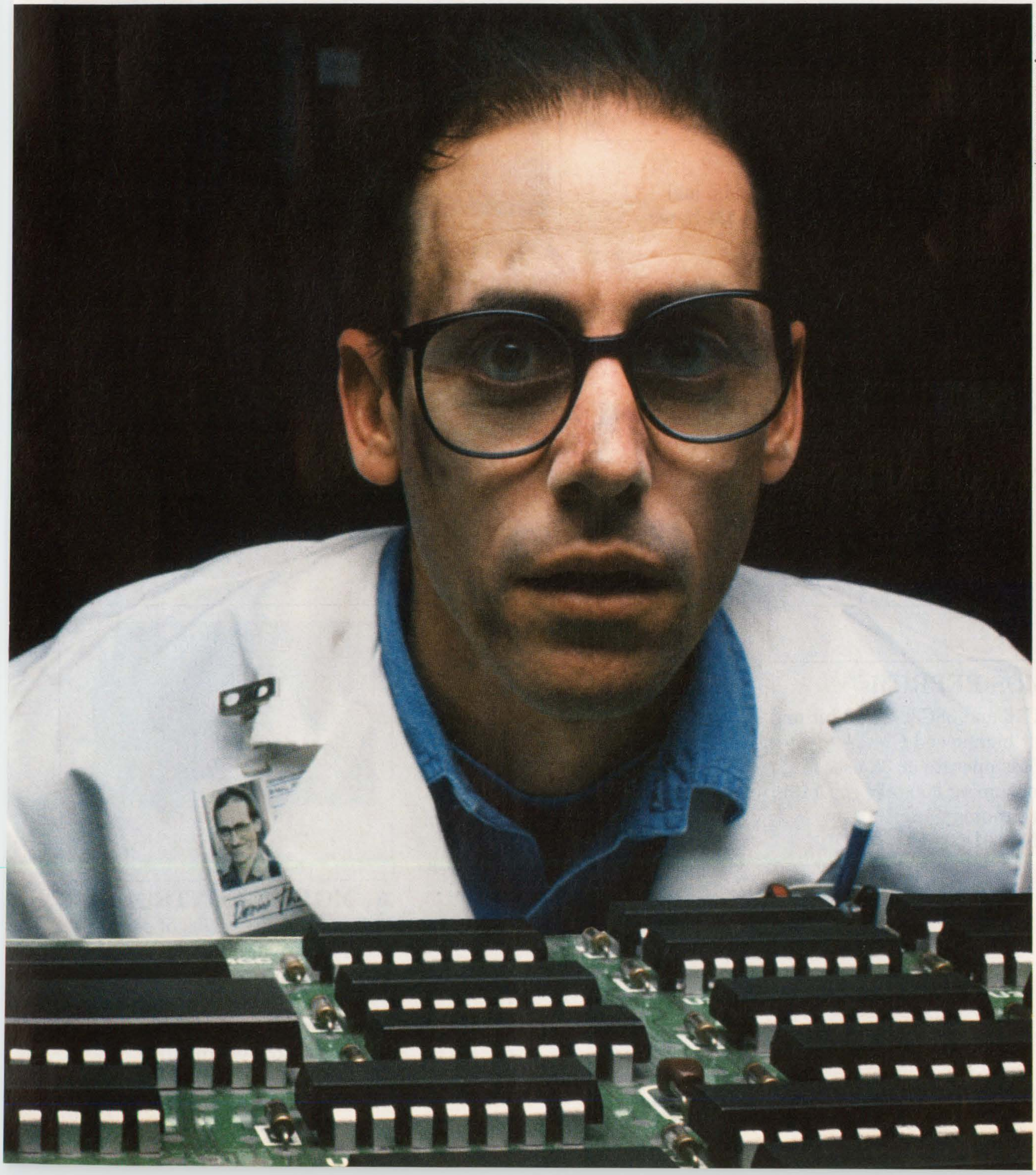
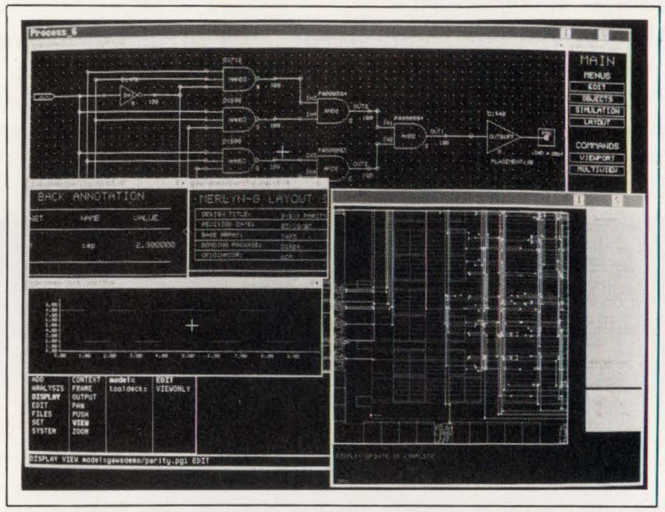


READERS' CHOICE

Of all the new products covered in EDN's **May 28, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **May 28, 1987,** issue.

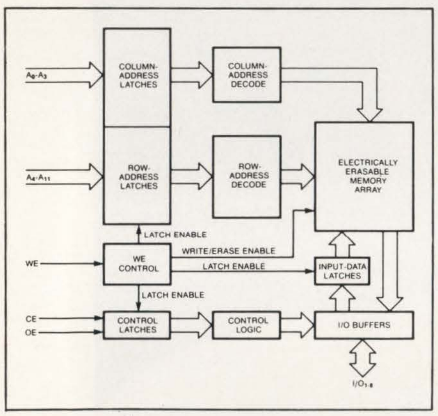
▲ PROM PROGRAMMER

The SE4944 programs PROMs, EPROMs, and EEPROMs having capacities of 16k to 1M bytes (pg 280).
Epotek Corp.
Circle No 605



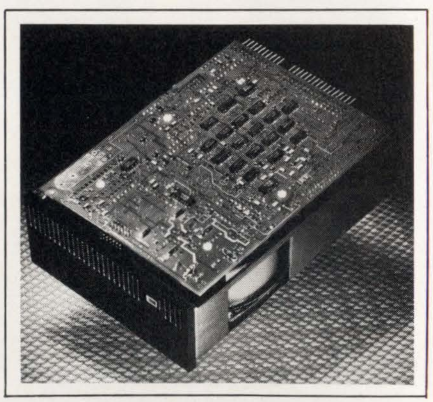
▲ INTEGRATED SOFTWARE

The Gate Array WorkSystem software integrates logic design, circuit simulation, and physical layout for creating and implementing circuit designs on gate arrays from specific foundries (pg 111).
Tektronix CAE Systems Div.
Circle No 603



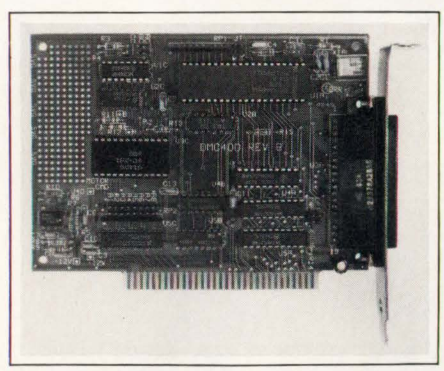
▲ CMOS EEPROMs

The 38C16 and 38C32 2k×8-bit and 4k×8-bit high-speed CMOS EEPROMs operate at 35 nsec while consuming 350 mW (pg 116).
Seeq Technology Inc.
Circle No 601



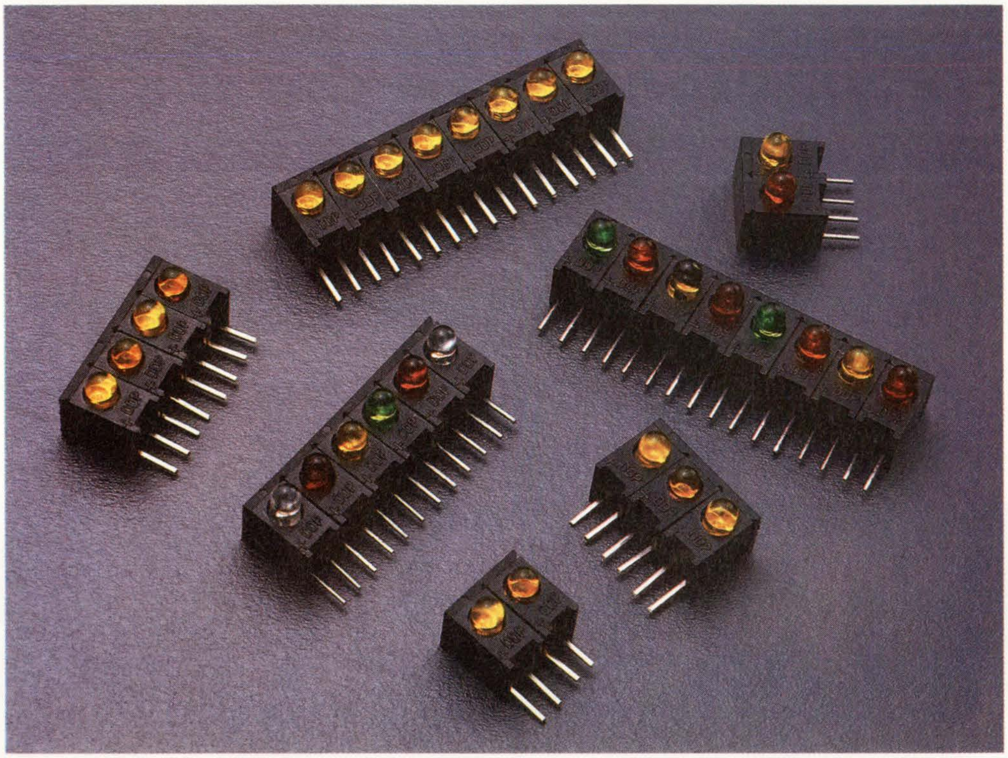
▲ WINCHESTER DRIVE

The LXT-170 stores 170M bytes of unformatted data in a standard 3½-in. package and offers a choice of SCSI- or ESDI-interface versions (pg 119).
Maxtor Corp.
Circle No 602



▲ MOTION CONTROLLER

Units in the -10 Series of servo motor controllers feature a digital integrator, programmable torque and error limits, a position latch, and diagnostics (pg 260).
Galil Motion Control Inc.
Circle No 604



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CIRCLE NO 96

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Like the 4501, the MK4503 is a first-in/first-out CMOS buffer memory. With its DIP packaging, the 4503 provides pin-for-pin replacement of our industry-standard 4501. And like its predecessor, the 4503 offers a CMOS RAM-based BiPORT architecture, allowing the two ports to operate at completely independent data rates and providing a simultaneous read/write capability.

What makes the MK4503 a true giant is its incredible 2K x 9 architecture – four times the density of the 4501. Making the MK4503 the new industry-standard CMOS FIFO.

And because the 4503 is memory-based, opposed to shift-register-based, you can implement very large FIFO arrays without experiencing ripple-through delay. Plus asynchronous read and write operations with no timing penalties.

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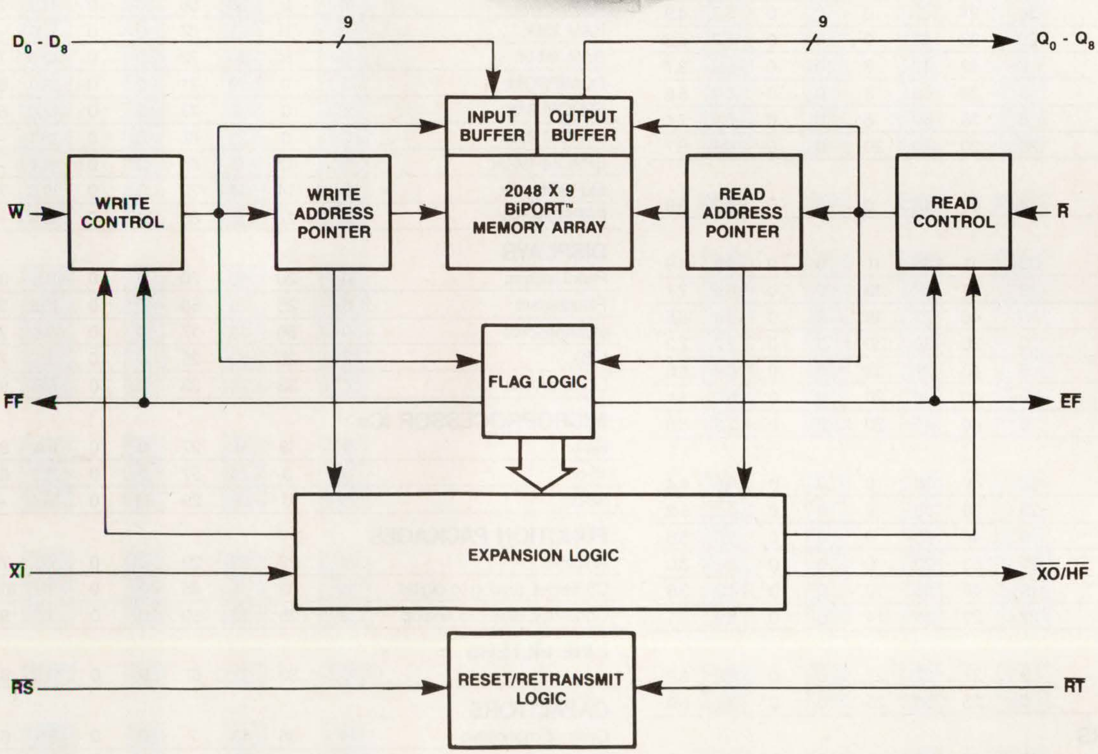
So if you thought the MK4501 was a small miracle, get ready for our latest giant step forward. The MK4503 BiPORT FIFO from Thomson-Mostek. The people who also bring you the world's fastest FIFO – the MK4505.

The MK4503 is available now. For sampling information, contact your distributor or write Thomson Components-Mostek Corporation, 1310 Electronics Drive, Carrollton, Texas 75006, MS2205. Or call (214) 466-6836.

BiPORT Family Features

	MK4501 (512 x 9)	**MK4503** (2K x 9)
First-in/First-out buffer	X	X
Independent data rates	X	X
Cycle rate	up to 12.5 MHz	up to 15.4 MHz
Access time range	65ns-200ns	50ns-200ns
Simultaneous read & write capability	X	X
Fully asynchronous	X	X
Fully expandable by word width & depth	X	X
Empty and full warning flags	X	X
Half-full status flag		X
Packaging available	28-pin DIP & 32-pin K PLCC	28-pin DIP & 32-pin** PLCC
Fully TTL compatible	X	X

**To be introduced.



MK4503 Block Diagram

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Integrated Electronics Corp.
ITAL Sales
Kieruiff Electronics
Lionex Corp.
Marshall Industries
Nu-Horizons Electronics
Pioneer Technologies Group
Pioneer-Standard
Quality Components (Q.C.-SW)
Quality Components (Q.C.-SE)
ITT Microcomponents
Schweber Electronics
Solid State, Inc.
Zentronics
Zeus Components, Inc.

THOMSON COMPONENTS MOSTEK

In addition to FIFOs, Thomson-Mostek manufactures a broad selection of MOS and bipolar devices for both commercial and military applications: microcomponents, ASIC, memories, telecom/datacom and linear circuits as well as Discrete, RF and microwave transistors and passive components.

 CIRCLE NO 17

LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	29	57	14	0	0	7.6	9.5
Pot-Core	0	50	33	17	0	0	6.8	8.8
Laminate (power)	0	25	33	34	8	0	10.7	7.1
CONNECTORS								
Military panel	0	20	40	0	0	40	16.2	10.7
Flat/Cable	25	38	37	0	0	0	4.1	5.7
Multipin circular	11	34	22	22	0	11	9.7	10.3
PC	11	34	22	22	0	11	9.7	5.8
RF/Coaxial	11	34	33	22	0	0	7.1	9.0
Socket	8	42	33	17	0	0	6.5	5.7
Terminal blocks	8	54	31	7	0	0	5.3	4.6
Edge card	11	33	45	11	0	0	6.3	6.6
Subminiature	0	42	33	17	8	0	8.6	8.2
Rack & panel	0	50	33	17	0	0	6.8	7.7
Power	0	33	34	33	0	0	8.8	8.4
PRINTED CIRCUIT BOARDS								
Single-sided	7	22	57	7	0	7	8.5	5.1
Double-sided	0	47	47	6	0	0	6.2	6.7
Multilayer	0	15	54	31	0	0	9.5	8.7
Prototype	0	83	17	0	0	0	3.8	3.8
RESISTORS								
Carbon film	31	25	38	6	0	0	4.7	3.6
Carbon composition	36	27	37	0	0	0	3.7	4.9
Metal film	20	33	47	0	0	0	4.7	4.3
Metal oxide	8	42	42	8	0	0	5.9	3.7
Wirewound	8	38	46	8	0	0	6.0	5.6
Potentiometers	6	38	50	6	0	0	6.1	7.4
Networks	20	20	40	20	0	0	6.9	5.7
FUSES	18	36	46	0	0	0	4.7	3.6
SWITCHES								
Pushbutton	33	11	45	11	0	0	5.6	4.9
Rotary	18	27	37	18	0	0	6.5	7.7
Rocker	9	46	27	18	0	0	6.4	6.5
Thumbwheel	20	20	30	30	0	0	7.7	7.2
Snap action	9	46	27	18	0	0	6.4	5.6
Momentary	10	40	30	20	0	0	6.7	5.1
Dual in-line	0	40	40	20	0	0	7.5	6.6
WIRE AND CABLE								
Coaxial	30	40	30	0	0	0	3.6	4.4
Flat ribbon	23	39	38	0	0	0	4.2	5.2
Multiconductor	9	46	45	0	0	0	5.0	5.8
Hookup	27	53	20	0	0	0	3.2	3.0
Wire wrap	18	46	36	0	0	0	4.3	3.8
Power cords	21	29	36	14	0	0	5.9	5.1
POWER SUPPLIES								
Switching	9	27	37	27	0	0	8.0	8.6
Linear	0	25	50	25	0	0	8.6	6.9
CIRCUIT BREAKERS	10	40	40	10	0	0	6.0	6.1
HEAT SINKS	17	58	17	8	0	0	4.4	5.8
RELAYS								
General purpose	0	54	23	23	0	0	7.0	6.8
PC board	0	33	9	58	0	0	10.7	8.6

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	0	38	25	37	0	0	8.9	8.5
Mercury	0	33	34	33	0	0	8.8	9.8
Solid state	11	33	22	34	0	0	7.9	10.1
DISCRETE SEMICONDUCTORS								
Diode	22	22	28	28	0	0	7.2	5.3
Zener	20	20	33	27	0	0	7.4	5.5
Thyristor	0	27	46	27	0	0	8.7	8.0
Small signal transistor	7	27	40	26	0	0	8.1	6.3
MOSFET	0	36	27	37	0	0	8.9	7.8
Power, bipolar	0	30	20	50	0	0	10.3	7.8
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	0	31	31	38	0	0	9.3	6.5
CMOS	6	24	23	47	0	0	9.9	6.5
TTL	0	25	44	31	0	0	9.1	6.3
LS	0	29	41	30	0	0	8.7	6.1
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	0	38	37	25	0	0	8.0	7.0
OP amplifier	0	36	29	35	0	0	8.9	7.7
Voltage regulator	0	38	31	31	0	0	8.4	5.9
MEMORY CIRCUITS								
RAM 16k	11	0	33	56	0	0	11.3	7.5
RAM 64k	11	0	33	56	0	0	11.3	7.9
RAM 256k	11	11	11	67	0	0	11.6	—
RAM 1M-bit	0	14	14	72	0	0	12.6	7.0
ROM/PROM	0	0	29	71	0	0	13.4	8.3
EPROM 64k	18	0	9	73	0	0	12.0	8.6
EPROM 256k	11	0	22	67	0	0	12.1	—
EPROM 1M-bit	0	17	0	66	17	0	15.1	—
EEPROM 16k	0	14	14	72	0	0	12.6	7.3
EEPROM 64k	0	17	0	83	0	0	13.4	—
DISPLAYS								
Panel meters	0	20	60	20	0	0	8.5	8.2
Fluorescent	0	25	25	50	0	0	10.5	9.1
Incandescent	0	50	33	17	0	0	6.8	7.9
LED	17	25	33	25	0	0	7.3	7.4
Liquid crystal	0	33	34	33	0	0	8.8	9.1
MICROPROCESSOR ICs								
8-bit	9	18	46	27	0	0	8.4	9.0
16-bit	14	0	29	57	0	0	11.1	6.8
32-bit	29	0	28	29	14	0	10.4	—
FUNCTION PACKAGES								
Amplifier	14	29	28	29	0	0	7.6	7.7
Converter, analog to digital	11	33	11	45	0	0	8.8	10.9
Converter, digital to analog	13	25	12	50	0	0	9.5	9.5
LINE FILTERS	0	33	0	67	0	0	11.3	8.3
CAPACITORS								
Ceramic monolithic	14	36	43	7	0	0	5.6	6.1
Ceramic disc	17	42	33	8	0	0	5.2	8.9
Film	15	31	39	15	0	0	6.4	6.8
Aluminum Electrolytic	7	36	29	28	0	0	7.8	7.8
Tantalum	0	50	25	25	0	0	7.4	7.1
INDUCTORS	0	38	37	25	0	0	8.0	6.4

Source: *Electronics Purchasing* magazine's survey of buyers

The HP 8175A is a great stimulus companion to logic analyzers used in response testing.

You spend a lot of time evaluating response instruments. What if you had a stimulus that measured up to your response?

Now you do.

The HP 8175A Signal Generator produces thousands of digital and analog signals, letting you emulate missing portions of your system . . . and test your design under many different operating conditions.

It's an advanced parallel and serial data generator that doubles as an analog dual arbitrary waveform generator.

You get 24 parallel channels at 50 Mbits/s. 2 serial channels at 100 Mbits/s. 2 analog channels at 50 Mbits/s. *Plus* an 8-bit input trigger and 8-bit output flags for easy interaction with your DUT. Prompts to guide you. Data editing capabilities to save you time. And more.

Just pair up the new HP 8175A Signal Generator with the HP 1630/31 Logic Analyzer or other response instrument. You'll have a powerful stimulus-response solution to make you more productive today and meet your test needs tomorrow as well.

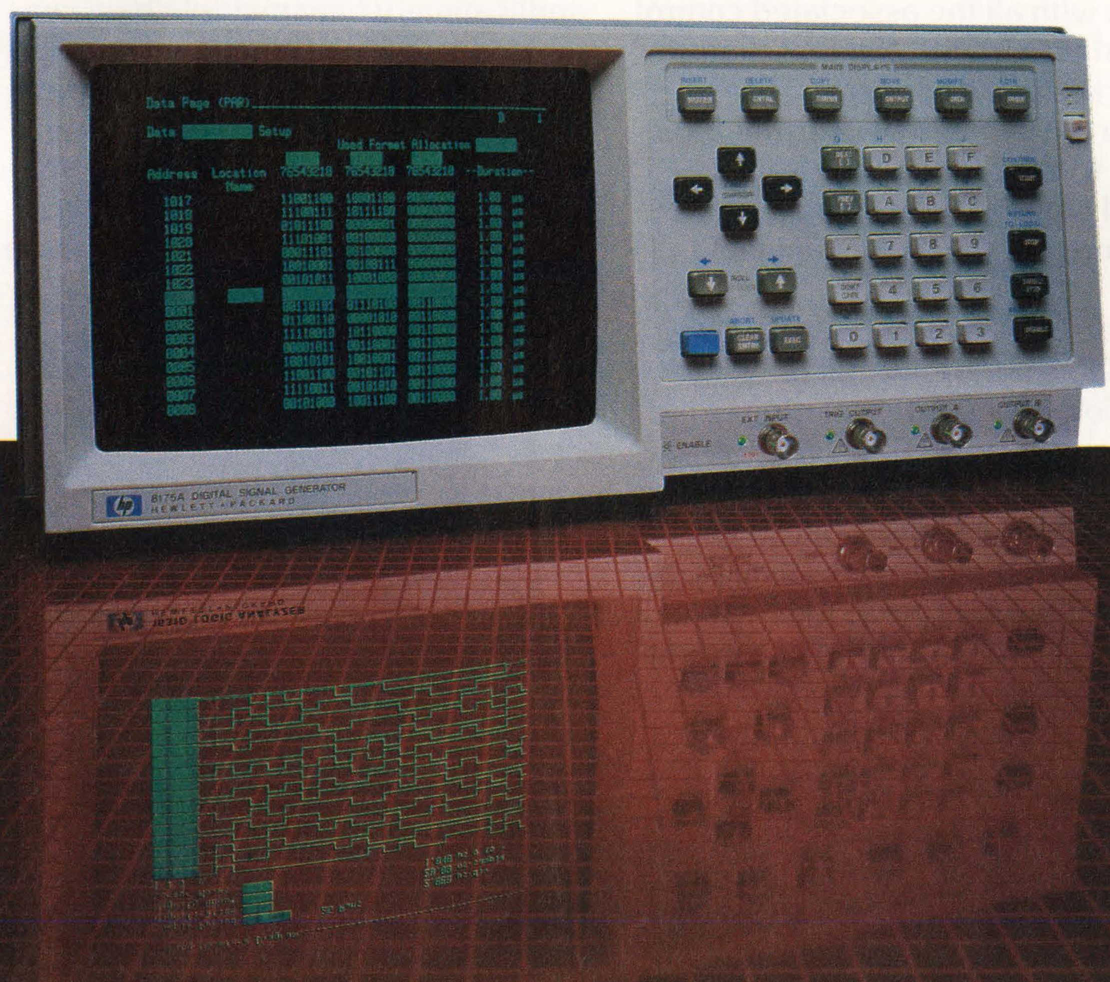
Call HP today!

Add a great stimulus to your test setup. For more information on the HP 8175A, contact your local HP sales office listed in the telephone directory white pages. Ask for the electronic instruments department.

HEWLETT PACKARD

CIRCLE NO 8

Now, a stimulus as good as your response!

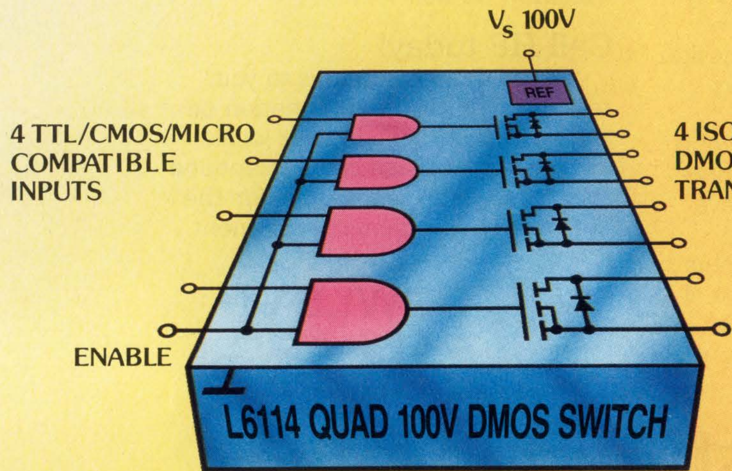


DESIGNED FOR HP-IB SYSTEMS

HP-IB: Not just IEEE-488, but the hardware, documentation and support that delivers the shortest path to a measurement system.

EI15704

WHO CAN INTEGRATE FOUR 100V DMOS SWITCHES IN A SINGLE SMART POWER CHIP?



Four fully isolated DMOS transistor switches with all the associated control and interface circuits. For less than $3 in quantities of 10K or more. That's what you get with the SGS L6114. Plus 70 watts total output power from a standard outline DIP package.

Can anyone else deliver anything like it?

The secret is SGS' Bipolar, CMOS, and DMOS smart power technology, which allows complete isolation of the output power DMOS transistors. And thanks to the high efficiency of the outputs, by using 6 of the package pins as a dedicated heat path, a small area of PCB copper dissipates the heat.

The L6114, with its 200kHz switching capability, is aimed at switch mode applications where multiple high current inductive loads are interfaced with low level logic. Unipolar stepper motor driving and needle solenoid driving in matrix printers are typical examples.

The L6114 is just one of a whole range of ICs based on SGS' Multipower-BCD™ technology. This unique smart power technology is bringing you a whole new generation of devices with improved performance levels and application potential.

Absolute Maximum Ratings

Vdss max	100V
Iout max	1.5A dc 5A peak
Ron	0.7ohms
Fswitch	200kHz
Package	Powerdip 14 + 3 + 3

PC-based GPIB control and data-acquisition

Powerful hardware and software tools make it easy for you to control a set of IEEE-488 instruments with a personal computer. (Photo courtesy National Instruments)

Sophisticated PC-based hardware and software tools are now blurring the distinctions between instrument control and data acquisition. You can use these tools to turn your IEEE-488 instruments into a data-acquisition system that you control from your PC.

IEEE-488 instruments and PC-based data-acquisition systems have traditionally provided very different services. The IEEE-488 or GPIB (general-purpose interface bus), which has long been recognized as the premier instrumentation bus, provides for the transfer of digital data among as many as 14 programmable instruments by using standardized sig-

products

J D Mosley, *Regional Editor*

With a well-planned combination of hardware and software tools for your personal computer, you can turn your set of IEEE-488 (GPIB) instruments into a PC-controlled data-acquisition system. To select the right PC-to-GPIB interface for your project, you'll need to consider such factors as controller intelligence, software sophistication, and system performance.

nals, techniques, and a single interface to the party-line GPIB. PC-based data-acquisition systems provide signal conditioning, A/D and D/A conversion, real-time data monitoring, and multiple inputs for as many as 32 channels on a standard IBM PC-compatible computer.

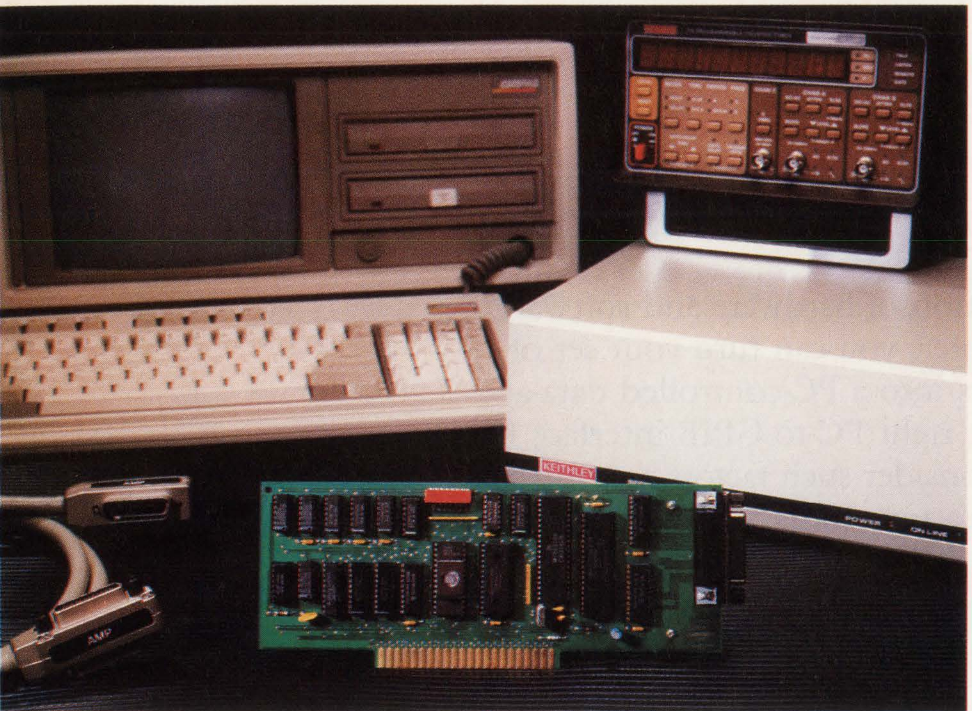
However, by adding a carefully selected suite of hardware and software tools to your PC, you can integrate GPIB instrumentation control with a PC-based data-acquisition system. Your system thus becomes a multiprogramming environment that lets you perform sophisticated test and measurement tasks. For instance, your laboratory-grade instruments will be able to provide precise measurements in the picoampere and microvolt range, as well as 24-bit A/D resolution and high-speed transient measurements that are accurate to eight bits at 1 MHz. Also, by using an IEEE-488 interface to control the instruments via a desktop PC, you'll obtain additional data-storage and -analysis capabilities that naturally complement any test and measurement task.

Further, the manufacturers of these hardware and software products have recently developed tools that allow you to use the IEEE-488 link for more than just controlling instruments. Some of these newly introduced products can provide you with more than rudimentary signal conditioning. Of course, for applications requiring 16-bit-wide DMA (direct-memory-access) transfers or 32 I/O lines, you'll still need to use dedicated data-acquisition boards. But some of the available software products are sophisticated enough that they can treat the input from multiple IEEE-488 boards as separate channels and can even provide different scale factors, sampling rates, and triggering conditions for each.

Windows simplify control

One such software product is LabWindows, which National Instruments expects to release in September. LabWindows lets you interactively control instruments, develop applications, and edit instrument-library modules. The product actually gives you several libraries: a graphics library, a digital-signal-processing (DSP) library, an instrument library, and a data-formatting library. LabWindows uses a proprietary internal format for command interpretation, but it displays the commands on your PC's CRT in the syntax of either C or Basic. LabWindows can also generate source code in C or Basic from your interactive session for incorporation in an application program.

You develop a program by entering the LabWindows program win-



Unlike IEEE-488 cards that plug directly into your PC, *Keithley Instruments' 500-IEEE card plugs into the System 570 data-acquisition unit. This configuration facilitates the integration of instrument control with data acquisition without monopolizing multiple expansion slots in your computer.*

dow, typing in program lines, and selectively executing them. You can also invoke pull-down menus and select library functions and parameters to generate a sequence of code that you can add to the program window. The instrument library lets you perform high-level programming of GPIB instruments. You can create and test an instrument-control program without knowing specific details of the instrument or of GPIB programming. A window can mimic a GPIB instrument's front panel with slide controls, binary controls, numeric-input boxes, and string-input boxes. By moving switches with the cursor keys or mouse, or by entering values in the numeric or string boxes, you can set up an instrument and manipulate its controls.

The LabWindows graphics library lets you produce a variety of graphs, plots, and charts. It allows you to zoom and pan and to superimpose graphs on one another. You can scale and rotate text generated with multiple fonts and create printouts without leaving your application program.

The DSP library includes such functions as array arithmetic, curve fitting, scaling, FFTs, and inverse FFTs. By using LabWindows' data-formatting library, you can transform data from one format to another, thus reducing the programming time for instruments that transfer data in peculiar formats. The software package also lets you call libraries from QuickBasic and Microsoft C. LabWindows starts at $395.

Another product that provides IEEE-488 control via software windows is Summation's TestWindows. Although the TestWindows software is a DOS-based ATE program, in order to use it you must also purchase the company's SigmaSeries TestStation and connect it to your PC. The TestStation is a $9950 chassis with an embedded 68000 μP for internal control, 512k bytes of RAM, 12 slots for instrumentation-function modules, an IEEE-488 interface with DMA, seven synchronization buses, 10 high-frequency buses, a power supply, DOS, and TestWindows. TestWindows alone costs $1950 and includes the TestBasic programming language, Microsoft Windows software, TestBasic Editor, an IEEE-488 window generator, debugging tools, documentation tools, and manuals.

A unique approach to GPIB control is to use a DOS-installable device driver that automatically loads your IEEE-488 control software each time you boot your PC. By using this technique, IOtech's Driver488 software functions as a utility. The technique also provides software compatibility with Basic, C, and Fortran, so when you use Driver488 you don't need separate device drivers for those languages. For applications written in Basic, Driver488 allows your program to vector to a subroutine upon a service request.

Driver488 uses a proprietary language that resembles the language used for HP Series 80 IEEE-488 controllers. Driver488 includes built-in error checking and time-out indications. The software works with the manufacturer's GPIB interface boards for IBM PC-compatible computers and for similar boards manufactured by National Instruments and Capital Equipment Corp. You can also order a version for use with the company's Personal488/2, a new board for the IBM Personal System/2. Driver488 starts at $195.

Ziatech Corp also offers DOS-installable driver software for its GPIB controller cards. The driver

Advancements in hardware and software products for the IEEE-488 bus are pushing GPIB control beyond the realm of mere instrumentation.

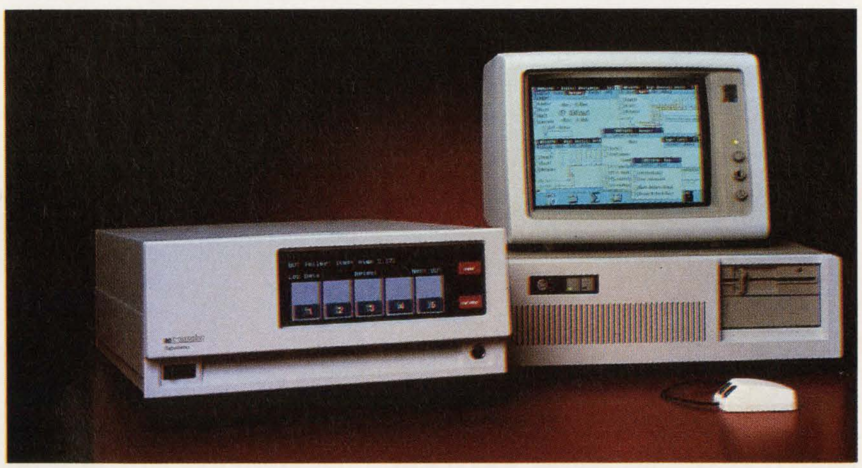
is called DOS.GPIB, and it gives your existing development tools and applications programs access to your IEEE-488 controllers without the need for additional programming. You can configure DOS.GPIB as a controller or as a talker/listener. DOS.GPIB costs \$250; the company requires no licensing fees for multiple-system users.

Database organizes input

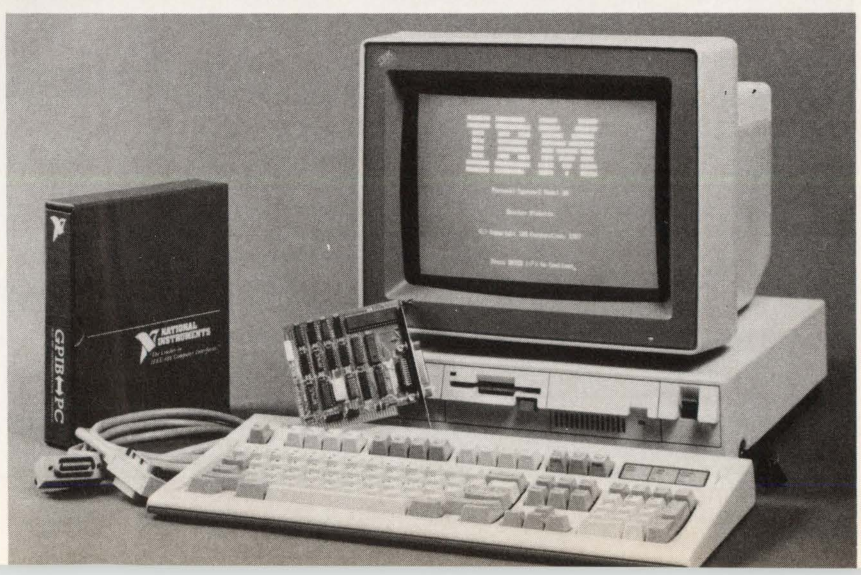
The latest software package from HP for IEEE-488 data management is especially suited to HP's hardware products, such as the HP Vectra PC, which comes with an IEEE-488 interface for instrument control. The \$1450 DACQ/PC program provides a vectorized database for data collected from IEEE-488 instruments, your computer's keyboard, and program results. DACQ/PC accommodates data-acquisition applications by including routines for thermocouple, RTD, and thermistor temperature linearizations. DACQ/PC also includes subroutines for calculating microstrain from strain-gauge cards.

Furthermore, the software facilitates process control by tuning and executing as many as 10 proportional-integral-derivative (PID) loops with one subroutine call. You can also use DACQ/PC to schedule as many as 99 prioritized tasks, to transfer data to other software programs (such as Lotus 1-2-3, WordStar, or dBaseIII), and to analyze your data via statistics, scaling, linearizations, and tabular conversions. You can plot your results on multiple-trace graphs or print them out as strip charts or formatted data.

Lotus Development Corp has introduced a program called Measure that links the GPIB and data-acquisition functions with spreadsheet analysis for technical applications. Although the spreadsheet was orignially developed for financial-analysis applications, its format is also suitable for use in technical data analysis. Measure runs under Lotus 1-2-3, and it provides device drivers that let you import data directly from your instruments to a spreadsheet. You can then analyze and graphically display your data by using Lotus 1-2-3's math and graphics functions.



Featuring a screen full of application windows, *the SigmaSeries TestStation from Summation provides an integrated multitasking environment that supplies IEEE-488 device windows, a TestBasic editor window, a debugging window, and output windows.*



The GPIB-PCII interface for the new IBM Personal System/2 Model 30 *(which is compatible with the IBM PC) specs data-transfer speeds exceeding 300k bytes/sec. The vendor, National Instruments, expects to offer versions for the PS/2 Models 50, 60, and 80 in September.*

Window-oriented software packages are simplifying test and measurement applications by letting engineers monitor several tasks at once.

The $495 menu-driven program uses the Lotus 1-2-3 macro language to capture keystrokes, automate repetitive tasks, and parse incoming data. If you are an experienced macro-language programmer, you can provide commands to make the system prompt the user for variables, perform file operations, facilitate decision making and branching, and provide screen and window control.

DSP Systems bills its DaDisp Worksheet program as "the first technical spreadsheet for digital signal analysis." Like Measure, DaDisp is a menu-driven program that lets you solve math problems, analyze data, perform "what-if" manipulations, generate graphs, and organize data. However, DaDisp has the sophistication to handle signal editing, waveform generation, FFT analysis, and peak finding. Furthermore, this package performs real and complex arithmetic and carries engineering

IEEE-488 CONTROLLER BOARDS FOR IBM PCs AND COMPATIBLE COMPUTERS

MANUFACTURER	MODEL	PRICE	SYSTEM BUS	DATA RATE (BYTES/SEC)	RAM CAPACITY
CAPITAL EQUIPMENT CORP	4×488	$795	PC	800k	4M BYTES (OPTIONAL)
	PC-488	$395	PC	800k	8k×8-BIT CACHE (OPTIONAL)
IOTECH INC	GP488A	$295	PC	300k	
	LPT488	$295	PC	N/A	
	PERSONAL488	$395	PC	300k	
	PERSONAL488/2	$500	MICRO-CHANNEL	250k	
KEITHLEY INSTRUMENTS	500-IEEE	$650	PC	N/A	
NATIONAL INSTRUMENTS	GPIB-PCII	$395	PC	300k	
	GPIB-PCIII	$795	PC	1M	
	MC-GPIB	$495	MICRO-CHANNEL	1M	
SCIENTIFIC SOLUTIONS	IEEE488	$395	PC	225k	
	IEEE488-LM	$355	PC	300k	
ZIATECH	ZT 2	$395	MICRO-CHANNEL		
	ZT 1444	$350	PC	450k	
	ZT 1488A	$449	PC	450k	

A=MICROSOFT'S BASICA
B=MICROSOFT'S GW BASIC
C=MICROSOFT'S COMPILED BASIC
D=MICROSOFT'S QUICK BASIC
E=MICROSOFT'S FORTRAN
F=MICROSOFT'S PASCAL
G=MICROSOFT C
H=BORLAND INTERNATIONAL'S TURBO PASCAL
I=MANX SOFTWARE SYSTEMS' AZTEC C
J=LOTUS'S MEASURE
K=MACMILLAN SOFTWARE'S ASYST
L=LABORATORY TECHNOLOGIES' LABTECH NOTEBOOK
M=TRANSERA'S TBASIC
N=TRUE BASIC'S TRUE BASIC
O=ASSEMBLY LANGUAGE
P=LATTICE C
Q=DESMET C

units through compound calculations.

DaDisp lets you create mutually dependent windows depicting graphic representations of signal-processing functions: When you load a new signal, each dependent window is automatically updated. The software's pipeline facility lets you run external programs, such as IEEE-488 drivers and data-acquisition software, from within DaDisp. The IBM PC-compatible version costs $795. You can order an interactive DaDisp demo disk for $20.

The IEEE-488 version of Labtech Notebook from Laboratory Technologies Corp also offers a spreadsheet format. This $1195 menu-driven program was originally developed to work exclusively with data-acquisition boards, but it's now compatible with National Instruments' IEEE-488 interface board as well. Its functions include process control, real-time graphics display, time stamping, mathematic calculations, and real-time data analysis.

Macmillan Software's Asyst is a 4-module software package that combines data-acquisition analysis and graphing with IEEE-488 support. To obtain GPIB control, you must purchase Modules 1, 2, and 4 for $1995. Module 1 provides the screen and array editor, graphics and windows, and statistical functions. Module 2 provides data analysis, including simultaneous equation solutions, FFTs, and least-squares approximations. Module 4 incorporates GPIB control and offers such complex bus functions as DMA transfers. You can add data-acquisition I/O (Module 3) for an additional $200, bringing the total cost of the four modules to $2195.

Boards vary in intelligence

The recent advancements in GPIB/data-acquisition products aren't limited to the realm of software. A number of hardware developments are also playing a major role in bridging the gap between data acquisition and GPIB instrumentation. Keithley Instruments' 500-IEEE card, for example, has an onboard 68000 μP. The manufacturer claims that this built-in intelligence makes the board easy to program: The μP converts high-level IEEE-488 commands from Keithley's simplified Soft500 programming language to GPIB protocol and handshaking.

Instead of requiring the cryptic programming codes used by most

ADDITIONAL I/O	SOFTWARE INCLUDED	SOFTWARE COMPATIBILITY	SPECIAL FEATURES
RS-232C; CENTRONICS	ROM-BASED; PROPRIETARY	A, B, C, D, E, F, G, H, O, P, Q	SHORT-SLOT CARD
	ROM-BASED; PROPRIETARY	A, B, C, D, E, F, G, H, O, P, Q	SHORT-SLOT CARD
		J, K, L, M, N	SHORT-SLOT CARD
			INTERFACES IBM PCs TO IEEE-488 PRINTERS AND PLOTTERS
	DRIVER488	A, B, C, D, E, F, G, H, I J, K, L, M, N	SHORT-SLOT CARD
			1M-BYTE/SEC VERSION AVAILABLE
		SOFT500	REQUIRES SERIES 500 OR SYSTEM 570 CHASSIS
	DOS HANDLER & BASICA	A, B, C, D, E, F, G, H, J, K, L, O	
	DOS HANDLER & BASICA	A, B, C, D, E, F, G, H, J, K, L, O	INCLUDES ONBOARD BUS ANALYZER
	DOS HANDLER	A, B, C, D, E, F, G, H, J, K, L, O	PROGRAMMABLE OPTION SELECT (POS)
	DRIVERS; BASIC	A	OPTIONAL SOFTWARE SUPPORT PACKAGE
	DRIVERS; BASIC	A, J, K, M	SHORT-SLOT BOARD
		DOS.GPIB	WATCHDOG TIMER; SECURITY OPTION
	DRIVERS; BASIC; COMPILED BASIC	C, F, G, H, P	SHORT-SLOT CARD
I/O EXPANSION SOCKET	DRIVERS; BASIC; COMPILED BASIC	C, F, G, H, P	SHORT-SLOT CARD

Many of the GPIB interface cards that fit into the short slot of an IBM PC's chassis offer as many or more features than do their full-size counterparts.

GPIB interfaces, the 500-IEEE card lets you use short, English-like commands similar to those used for HP Series 80 IEEE-488 controllers. For example, a 31-line program that polls a digital multimeter and displays the readings can be written in 13 brief lines of Soft500 text for the 500-IEEE. The card costs $650, but for PC-based control you must plug it into Keithley's System 570 data-acquisition unit—a chassis that attaches to your IBM PC or compatible computer. A complete system—including a System 570 chassis, a 500-IEEE card, analog I/O, digital I/O, 16 control relays, and Soft500—costs $2295.

Capital Equipment Corp provides its 4×488 multifunction board with the capacity for as much as 4M bytes of onboard RAM. Memory-management software comes with the board. The 4×488 card also has resident firmware that provides IEEE-488 extensions to Basic, Pascal, C, and Fortran, so you can program instruments without having to add software drivers for those languages. Besides providing an IEEE-488 interface, the board includes an RS-232C (serial) port and a parallel port, so it lets you test, store, and print results without monopolizing numerous expansion slots in your PC. With 1M bytes of RAM, the 4×488 costs $895.

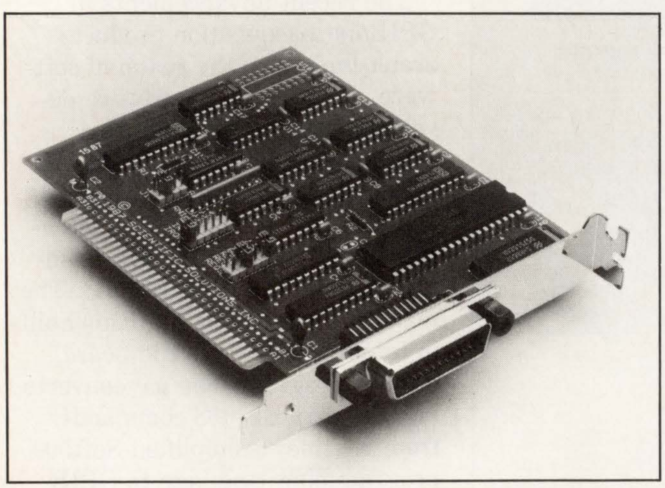
The 4×488 board works with third-party software packages and the company's $95 Co-Operator software. Co-Operator is a menu-driven program that writes IEEE-488 control programs. You can order free demo disks for Co-Operator and Lotus's Measure from Capital Equipment Corp.

National Instruments offers the $395 GPIB-PCII and the $795 GPIB-PCIII interface cards for PC-compatible computers. The PCII interface specs data-transfer speeds exceeding 300k bytes/sec. It also offers a choice of six interrupt lines and a choice of three DMA channels. It implements talker, listener, polling, service-request, and remote-programming functions. The GPIB-PCIII interface specs 1M-byte/sec data-transfer rates and includes an onboard IEEE-488 bus analyzer that monitors the status of your IEEE-488 bus command and data lines for debugging and loop-back testing.

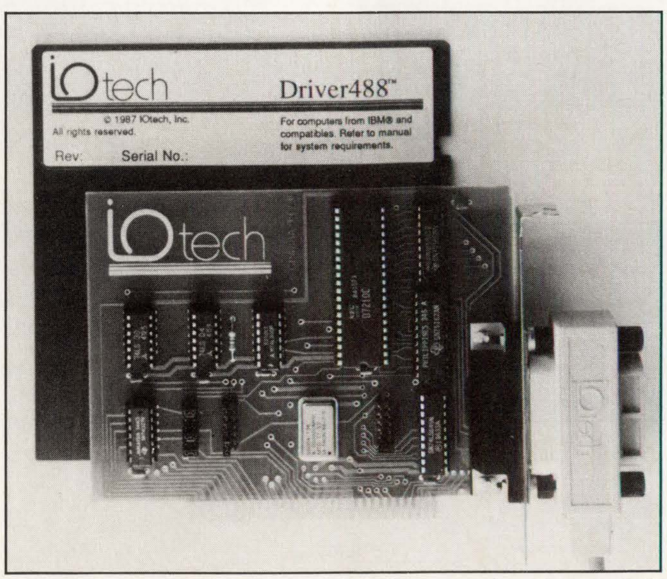
For continuous bus analysis, you can purchase the company's $995 GPIB-410 bus-analyzer/monitor card, which displays the bus status on the screen with simulated LEDs. The GPIB-410 includes a 256×16-bit buffer to capture bus data in real time, and it lets you store the data in your PC's memory for later review and analysis. You can also use the GPIB-410 to search for glitches or to find bus-timing problems.

Control on a short card

If you're running out of PC expansion slots, consider using the $355 IEEE-488LM card from Scientific Solutions. This half-slot board offers a full implementation of the IEEE-488 standard and includes a 2-meter IEEE-488 cable. It comes with menu-driven interface software (including the source code), a BIOS printer/plotter driver, a Basic subroutine library, and sample programs. The board's 3-state buffers facilitate data-transfer rates reaching 500k bytes/sec



Providing a full implementation of the IEEE-488 standard on a half-slot card, *the IEEE-488LM from Scientific Solutions includes menu-driven interface software and is compatible with such software packages as Measure and Asyst.*



Once you've installed the Driver488 software package in your PC, *you never have to load it from disk or reference it in ROM again. A DOS-installable device driver automatically loads IOtech's Driver488 each time you boot your PC.*

DMA-transfer rates reaching 1M byte/sec are not uncommon in some of today's sophisticated IEEE-488 controllers.

for devices with open-collector buffers and 2M bytes/sec for devices with 3-state buffers. An onboard oscillator provides the GPIB interface-timing parameters. You can run such third-party programs as Measure or Asyst on this board without making additional software or hardware modifications.

Another short-slot card, the PC-488 from Capital Equipment Corp, comes with resident firmware that adds IEEE-488 control statements to interpreted and compiled Basic, Pascal, C, and Fortran. This ROM-resident software makes your PC ready to run IEEE-488 applications as soon as you plug in the board. Your PC will also be ready to run word-processing and spreadsheet programs with IEEE-488 printers and plotters. The PC-488 runs AutoCAD in conjunction with HP plotters. It can transmit and receive byte arrays as large as 64k bytes each at speeds greater than 800k bytes/sec. You can select from single, demand, or burst DMA in either background or foreground modes. PC-488 costs $395, including software drivers and a programming and reference manual. The optional 8k×8-bit cache RAM costs $29.

Intelligent chassis automates lab

Containing an internal Z80A µP and a unique EPROM-resident operating system, the Taurus Lab from Taurus Computer Products Inc provides IEEE-488 control in conjunction with 64 analog and 64 digital channels for integrated data collection and control. This fixed-configuration system comes with 8k bytes of RAM and buffer storage, so you can adapt the unit for your particular process-control and data-acquisition tasks. Alternatively, you can use the Taurus Lab's preprogrammed features and commands for plug-and-go operation.

Providing a µP-controlled IEEE-488 interface to your PC and instruments, *this A/D-conversion system from Preston Scientific helps you integrate GPIB control with data-acquisition tasks.*

As many as 31 Taurus systems can communicate with a host computer over a single multidrop line. Taurus command messages include an embedded system address that lets you direct any command message to any of the linked systems. Taurus Lab sells for $5732.

Another chassis product comes from Preston Scientific. With the company's MPC, an IEEE-488 interface, you can transmit data to and from your PC-compatible computer, a rack-mountable A/D-converter chassis, and a variety of GPIB-compatible devices. Having a maximum DMA-transfer rate of 300k bytes/sec, a data-acquisition system using the MPC can provide continuous data throughput at speeds reaching 130 kHz and burst throughput at speeds reaching 1 MHz. The MPC software handler includes a language interface to interpretive Basic. You can purchase optional language interfaces for Fortran, Pascal, Compiled Basic, assembly language, and C. Depending on the configuration you choose, the MPC system costs from $7500 to $20,000.

GPIB boards for the IBM PS/2

Besides providing boards that are compatible with the IBM PC family and its clones, a number of hardware vendors offer GPIB boards that you can use with IBM's new Personal System/2 computers. IOtech, for example, recently introduced the Personal488/2 GPIB interface, which works with IBM PS/2 Models 50, 60, and 80. You can choose from two versions of the board: the 250k-byte/sec version, which starts at $500, and the 1M-byte/sec version (called the Personal488/2A), which costs $595. Both boards plug into the PS/2 Micro Channel and provide interrupt levels, DMA channels, and controller/peripheral mode selection. These boards use no DIP switches or jumpers—you can choose from seven interrupt levels, 15 DMA arbitration levels, and 256 I/O addresses by means of software control. Alternatively, you

Text continued on pg 104

Manufacturers of IEEE-488 data-acquisition products

For more information on IEEE-488 products such as those discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Analog Devices Inc
2 Technology Way
Norwood, MA 02062
(617) 329-4700
Circle No 650

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(617) 273-1818
Circle No 654

Computer Dynamics Inc
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Greer, SC 29651
(803) 877-7471
Circle No 655

Connecticut Microcomputer Inc
Box 186
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Suite 211
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(408) 727-1497
Circle No 657

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Newton, MA 02158
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Circle No 658

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Devtek Systems
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(617) 577-1133
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General Research Corp
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Circle No 664

Hewlett-Packard Co
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Palo Alto, CA 94303
Phone local office
Circle No 665

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Circle No 666

ICS Computer Products
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San Diego, CA 92123
(619) 279-0084
Circle No 667

Integrated Systems Products Inc
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Camarillo, CA 93010
(805) 987-5125
Circle No 668

Interactive Microware Inc
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State College, PA 16804
(814) 238-8294
Circle No 669

IOtech Inc
23400 Aurora Rd
Cleveland, OH 44146
(216) 439-4091
TWX 650-282-0864
Circle No 670

Keithley Instruments Inc
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Cleveland, OH 44139
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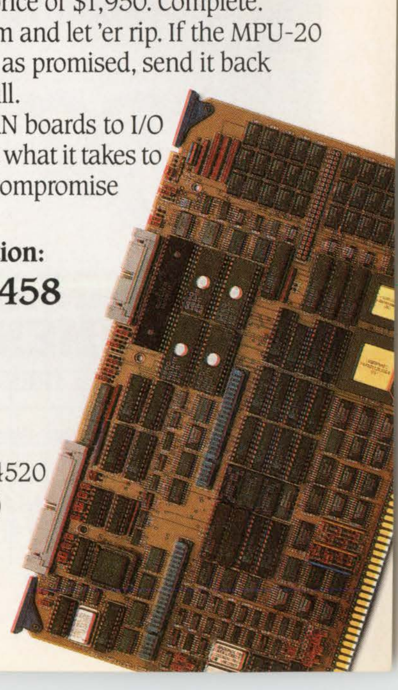

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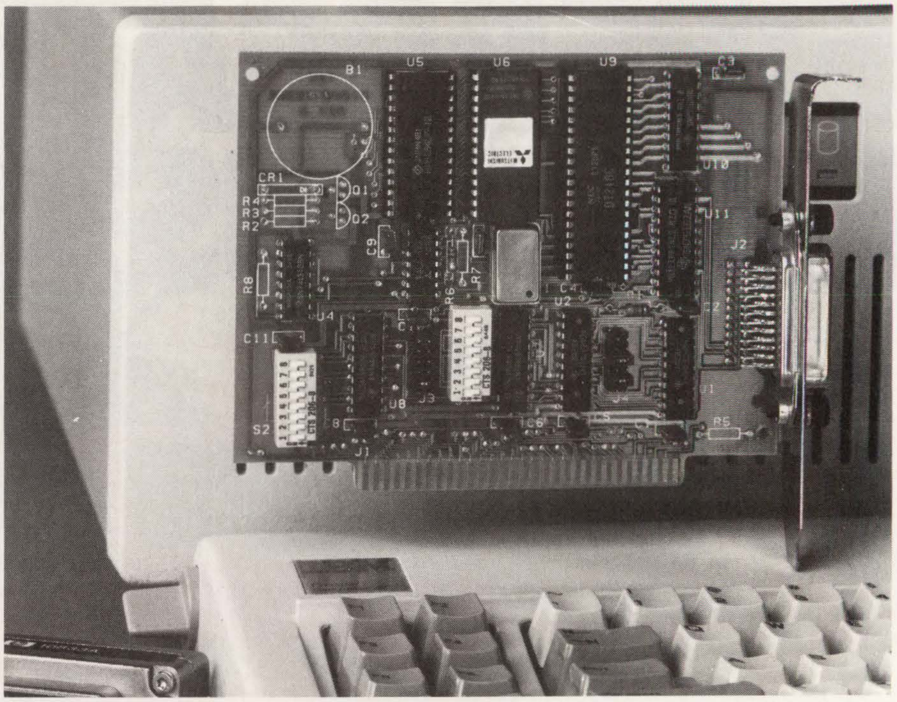

The ROM-based software and optional 8k×8-bit cache RAM of the PC-488 short-slot board from Capital Equipment Corp boosts DMA-transfer speed and facilitates advanced programming applications.

can use the company's $295 GP488A board to link your PC-compatible computer to IEEE-488 devices. The GP488A, bundled with the vendor's Driver488 software, costs $395.

National Instruments also offers a GPIB interface card for IBM's Micro Channel computers. The MC-GPIB board includes an NEC μPD7210 μP, which provides IEEE-488 talker, listener, and controller functions. The board also features a Turbo488 custom IC, which provides increased data-transfer rates and lower software overhead. The board specs programmed I/O data rates as high as 100k bytes/sec. Its FIFO buffers boost DMA transfers, allowing 1M-byte/sec GPIB reads, 700k-byte/sec GPIB writes, and 320k-byte/sec GPIB commands.

The board's Programmable Option Select feature lets you use IBM system-configuration utilities to select I/O addresses, interrupt levels, and DMA channels automatically, so you don't need any switches or jumpers from the board. The MC-GPIB also provides extra monitor and control ports for board- and bus-level diagnostics. For $495, you receive the MC-GPIB board and the MS/PC-DOS software handler. MS/PC-DOS is a device driver that can be installed as part of the operating system; it provides compatibility with most of the popular languages for the PC, including Fortran, Basic, C, Pascal, and assembly language.

A third company that offers an IEEE-488 controller for IBM's Micro Channel computers is Ziatech Corp. The firm's $395 ZT 2 board uses the same device driver (DOS.GPIB) that supports the company's PC-compatible IEEE-488 board, so it may be useful to engineers who intend to upgrade from a PC-based test and measurement system to one based on an IBM PS/2 machine. The ZT 2 features a watchdog timer that alerts your system whenever a GPIB device doesn't respond within a predefined interval, thus preventing instrument failure from suspending the system's operation. The ZT 2 also offers a security option: a hardware-based security lock for your software applications. **EDN**

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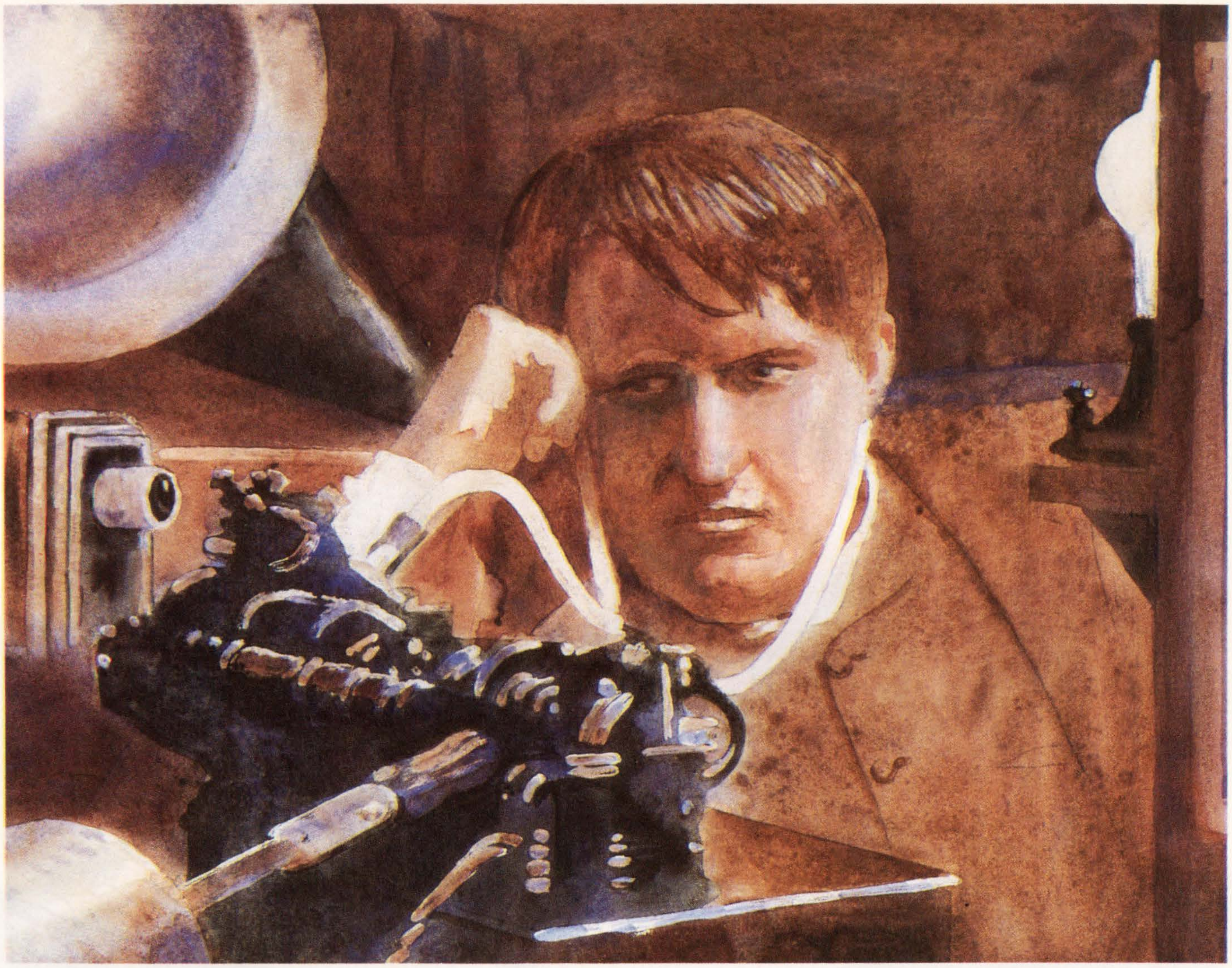

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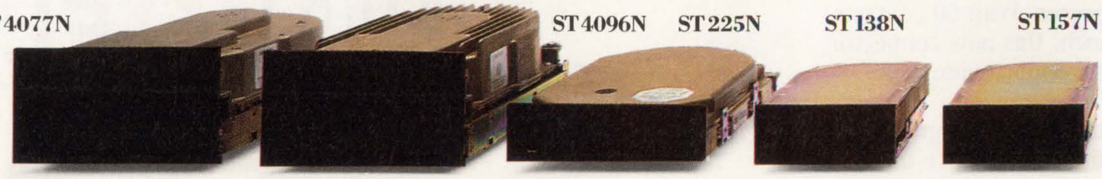

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EDN's DSP Project—Part 1

Digital signal processing enters the mainstream

Digital signal processing is finding use in products that don't involve such traditional applications as radar. And the chips in general are faster, cheaper, and even easier to use. DSP ICs are popping up in systems that address everything from the more conventional filtering applications to some less traditional ones like financial-modeling and servo-control applications. This first in a 4-part series reviews some basics and brings you up to date on digital-signal-processing products.

Jim Wiegand, *Associate Editor*

The strengths of the DSP approach to signal manipulation and analysis—extremely stable specs over temperature and time, and extreme flexibility—together with advances in operating speed, have made DSP a central player in areas where analog signal processing has long dominated. Although no one is willing to predict that DSP might replace analog signal processing the way digital computers have displaced analog computers, the quality and pervasiveness of digital products, such as compact disks, digital audio tape, and digital radio broadcast equipment, indicate that DSP is here to stay.

This, the first of a 4-part series EDN is devoting to DSP, briefly reviews the basics of DSP and gives you an update of the products available. David Shear's 2-part contribution will start with an article on the tools that can ease your implementation of a DSP design. David will follow that with a hands-on article, in which he will take you from conceptualization to finished product. Bob Cushman's directory of DSP products will conclude the series. Similar to EDN's μP directory, the DSP directory will provide you with a concise aid in the selection of DSP products.

DSP noise-reduction techniques provide audio/visual products with unmatched signal purity and dynamic range. And so it's unlikely that consumers will be trading in their CD players for a purely analog playback system. But other less traditional areas are beginning to use DSP techniques as well. DSP's promise now extends to the financial world, for example. Wall Street's traditional reliance on experience and intuition is giving way to increasing dependence on algorithms and computers, and this newfound trust seems to be creating a niche for DSP. The day when you can convert stock and commodity data into a financial model and then apply pattern-recognition techniques to predict market trends isn't too far away. This application is quite different from the siesmology, medical imaging, and radar applications that have been the mainstay of image processing.

Filling the gap between general-purpose μPs and bit-slice DSP products, the monolithic DSP chip provides you with the same flexibility afforded by a general-purpose μP along with an instruction set and archi-

DSP noise reduction techniques provide audio/visual products with unmatched signal purity and dynamic range.

tecture that are optimized for the multiply and accumulate operations that are characteristic of DSP applications. Basically, DSP products fall into three categories: special-purpose DSP ICs, general-purpose DSP chips, and building-block ICs. Typical of the special-purpose ICs is the DSP56200 finite-duration impulse-response filter (FIR) IC from Motorola. And the Texas Instruments TMS320C30 is a representative general-purpose DSP chip. The WS59510 multiplier accumulator (MAC) IC from Waferscale Integration (Fremont, CA) is a member of the building-block family **(Ref 1). Table 1** indicates some of the applications and corresponding hardware requirements for DSP designs.

The $32 (OEM qty) WEDSP16 from AT&T is a general-purpose DSP, but this programmable device offers above average rates, performing a 16×16-bit multiplication and 36-bit accumulation in 75 nsec. You can also test a standard set of ALU conditions for conditional ALU operations, including branches and subroutine calls. The condition tests, branching capability, and subroutine calls allow you to operate the processor as a 16- or 32-bit μP for logical and control operations in addition to the computationally intensive operations.

The WEDSP16 device contains a data arithmetic unit, which performs the signal-processing arithmetic; a ROM-address arithmetic unit; a RAM-address arithmetic unit; and a 2048×16-bit ROM that contains instructions and fixed data. For variable RAM data, it includes a 512×16-bit RAM. The device also has a serial I/O unit and a 16-bit parallel I/O unit. In addition, an on-chip cache is organized as 15×16 bits.

The chip includes a 2048×16-bit ROM. If you want to perform full-speed prototyping, you can replace the on-chip ROM with as much as 64k 16-bit words of off-chip ROM. The off-chip ROM must provide at least a 50-nsec access time, however. The clock input to the chip has a specified range of 37.5 to 1000 nsec for its cycle time. The access time for off-chip memory is given as twice the cycle time of the input clock minus 25 nsec.

TABLE 1—COMPONENTS REQUIRED FOR VARIOUS DSP APPLICATIONS

APPLICATION	REQUIRED COMPONENTS
LOW-FREQUENCY CONTROLLER	A GENERAL-PURPOSE μP
HIGH-SPEED MODEM	A GENERAL-PURPOSE DSP
ELECTRONIC ECHO CANCELER	A μP PLUS A SPECIAL-PURPOSE DSP
DIGITAL RADIO	A GENERAL-PURPOSE PLUS A SPECIAL-PURPOSE DSP
ACOUSTIC ECHO CANCELER	A GENERAL-PURPOSE DSP PLUS MULTIPLE SPECIAL-PURPOSE DSP
WORKSTATION	MULTIPLE GENERAL-PURPOSE DSPs
RADAR SYSTEM	MULTIPLE GENERAL-PURPOSE DSPs AND/OR BUILDING-BLOCK ICs

Use off-chip ROM to modify programs

You can also use the off-chip ROM to accommodate frequently modified programs. The additional circuitry required for an off-chip ROM implementation increases the per-piece price of your product, but the code, as with any μP-based design, often changes frequently enough to justify the added cost. So unless you are quite certain of your system specifications and the code you use to implement the system's functions, plan on using the off-chip ROM.

The $40 (OEM qty) TMS320C30 is a third-generation DSP chip from Texas Instruments. The part can achieve 33M flops when operated with a 60-nsec cycle time (the manufacturer claims that faster versions will be available). The processor incorporates two 1k×32-bit single-cycle, dual-access RAM blocks; one 4k×32-bit single-cycle dual-access ROM block; a 64×32-bit instruction cache; and an on-chip DMA controller.

The TMS320C30's multiplier operates in either floating-point or integer mode. In floating-point mode the inputs are 32-bit numbers, and the result is a 40-bit number that provides room for any growth that might occur after several calculations. The integer operands are 24-bit numbers, and the result is 32 bits long. You can use the part to build a 256-tap FIR filter that operates at a sampling rate of greater than 60 kHz or a 256-tap least-mean-square (lms) adaptive FIR filter with a sample rate of more than 20 kHz. The corresponding floating-point operation requires more time for these functions.

DSP's a natural for servo control

As with other DSPs, you needn't restrict your application of the TMS320C30 exclusively to DSP areas. Digital control systems are a natural extension of the application of these parts, and DSPs are already used as the servo controller in some disk drives. The stability over time and temperature is once again the crucial asset.

The high-speed processing that chips such as the $157 TS68930 from Thomson-Mostek offer also make them perfectly suitable for graphics engines. Graphics processors must create and manipulate images that typical-

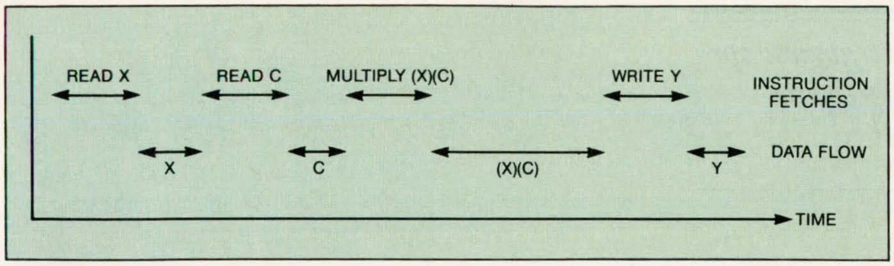

Fig 1—The traditional, Von Neumann architecture *of most μPs prevents parallel acquisition of data and instructions since both data and memory are contained in the same memory space. The sequential operation of acquiring, multiplying, and storing the results of the multiplication of two numbers is illustrated here.*

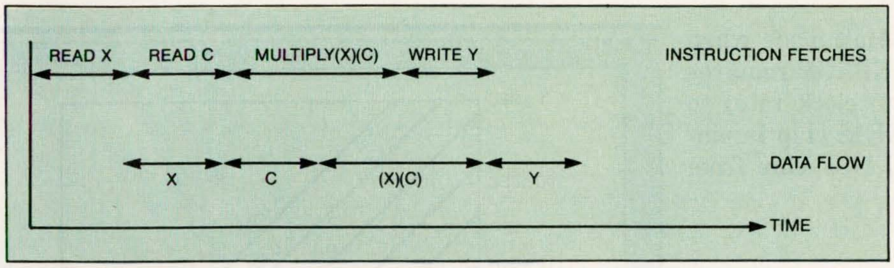

Fig 2—A Harvard-type architecture allows a μP to fetch data and instructions in parallel. *Beginning with the point where microinstruction READ C and data X are fetched in parallel, the multiplication operation of **Fig 1** is executed in parallel, using the Harvard architecture.*

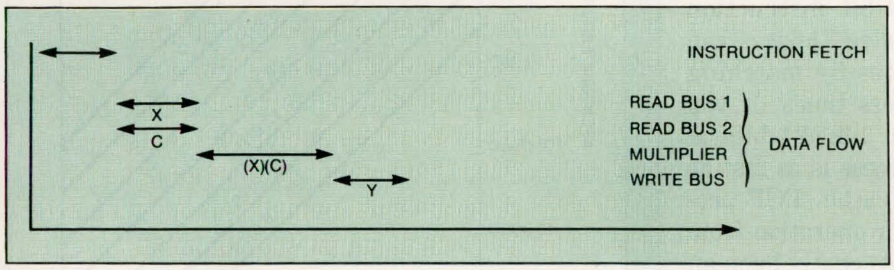

Fig 3—An enhancement to the Harvard architecture, *three parallel buses, allows a μP to fetch two operands simultaneously, but the μP's operation depends upon the execution speed of the multiplier.*

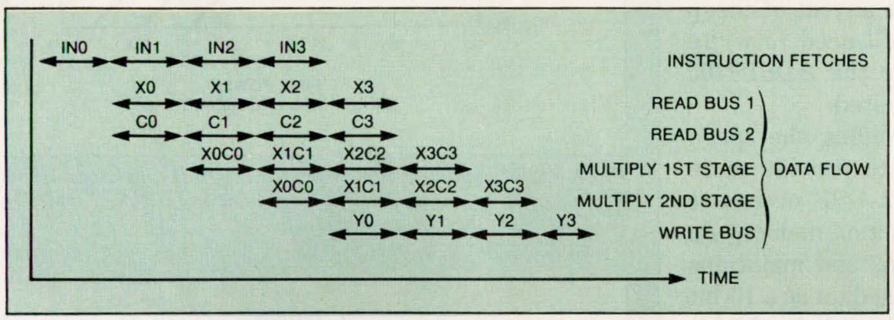

Fig 4—A parallel architecture can take advantage of pipeline techniques. *In this example, operands for the third multiplication in a series are fetched at the same time as the results of the first multiplication are stored.*

ly consist of 1k×1k×8 bits. And an image-rotation operation requires repeated multiplication and addition computations that must be performed on all one million bytes contained in such an image. Multiplications and additions are, of course, a forte of DSP chips.

The TS68930 incorporates the Harvard architecture, which is common to most DSP processors. By separating instruction and data memory, the Harvard architecture allows processors to fetch instructions and data simultaneously. All general-purpose μPs employ a Von Neumann architecture, in which instructions and data are located in the same memory space. During the first clock cycle of an instruction's execution, the μP fetches the instruction, and then it fetches the data. **Fig 1** illustrates the sequential nature of the instruction execution associated with the Von Neumann architecture. The Harvard processor, as illustrated in **Fig 2**, can fetch data and instructions simultaneously. By fetching instructions and data at the same time, the μP operates much faster than a Von Neumann μP.

One limitation of many Harvard processors, however, involves the bus structure. With two buses, simultaneous fetching is possible, but an extra bus cycle must be devoted to storing results. A processor that has three buses, one for each operand and one for results, benefits most from the Harvard architecture. **Fig 3** illustrates the advantages of a 3-bus Harvard architecture. By including pipelined operation, a μP can realize further improvements in throughput **(Fig 4).** To support the Harvard architecture, the TS68930 has three pipelined buses and 32-bit instructions. All these features combine to produce a performance level of 6.25 MIPS, which means the chip completes a 1024-point complex FFT in 9.65 msec.

The $100 DSP320EE12 from General Instrument Microelectronics adds a new twist to the DSP product line-up by incorporating 2.5k words of on-chip EEPROM. The EEPROM lets you design systems that monitor signals, interpret previously digitized inputs, and then adjust on-chip parameters to fine-tune your system's performance. The internal EEPROMs high-voltage programming supply is also included on the chip, so you don't need to include an external one. If you elect to reprogram the part during program execution, *DSP products fall into three categories: special-purpose DSP ICs, general-purpose DSP ICs, and building-block ICs.*

keep in mind that the μP remains in Halt mode when reprogramming is taking place. The EEPROM requires 1029 cycles (50 μsec at the maximum clock rate) to reprogram each word. The DSP320EE12 chip is pin-for-pin compatible with the TM32010 DSP chip from TI.

Tight code makes a comeback

Because it has an on-chip 16×24-bit instruction cache, the $337 ADSP2100 from Analog Devices can maintain maximum performance rates by matching instruction-fetch times with data-access times. If you can confine your code to the on-chip 16k×24 bits of program memory, then instruction access is as fast as data access, and you won't need the cache. DSP processors, because they are optimized for operation from on-chip memory, bring back what has recently been an outdated requirement: tight code. The advent of cheap memory obviated tight code, but you'll need to write tight code again if you use chips like the ADSP2100 because on-chip memory is strictly limited.

Of course, another approach to avoiding the speed penalty of using off-chip memory is to provide more memory on the chip. The $250 M6992 DSP processor from Oki includes 64k words of instruction memory on the chip. The part performs 20M flops and maintains 480 dB of dynamic range. It formats the data as a 16-bit mantissa and a 6-bit exponent. Although its 22-bit floating-point operations don't conform to 32-bit floating-point standards, the manufacturer claims that the extra resolution provided by 32-bit floating-point processors is wasted in 90% of all applications.

Adapt, adopt, improve

Adaptive filters form a distinct class of filters. Often used to provide echo cancellation in telecommunications applications, these filters have two inputs that are correlated to produce an error signal. The error signal is then used through feedback techniques to adapt the filter to signal conditions. The signal of one input passes through a filter that varies its parameters in order to estimate the ideal of the second input. An external processor or the filter itself varies the filter parameters until the parameters converge. At that point, the output, which is the error signal, is minimized.

The $100 DSP56200 from Motorola is a FIR-filter chip and, as is common in adaptive filters, it is based on the lms algorithm. The algorithm is implemented in silicon, so you don't have to write the software. You can

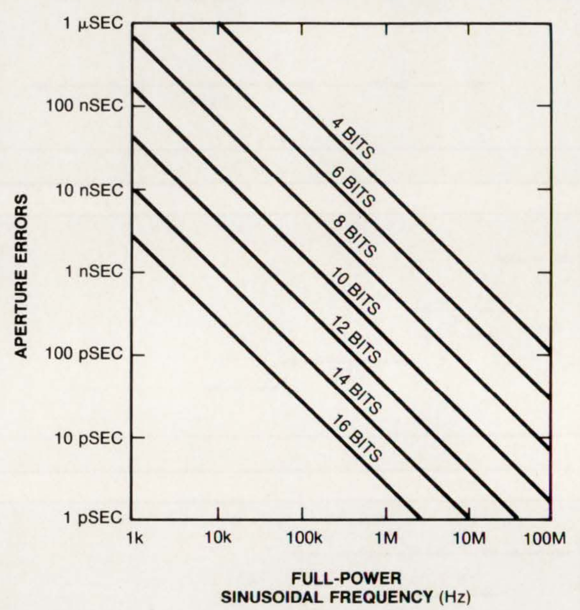

***Fig A—Allowable aperture errors** for a 1-LSB amplitude error are based on the frequency of a sinusoidal input signal and the required resolution for your system.*

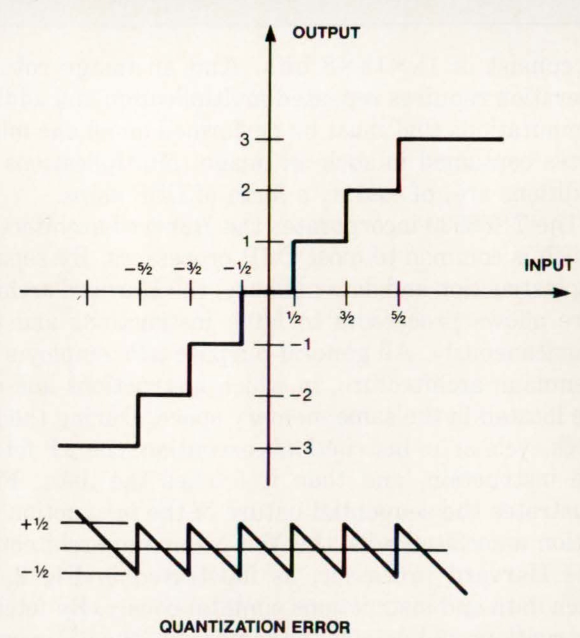

***Fig B—The quantization error varies between** ±½ LSB of the quantizer—in this case an A/D converter.*

A DSP primer

The function of any DSP system is pretty elementary: A DSP system generally acquires an analog signal and converts it to digital form. The system then processes the digitized data and, optionally, converts the results back into analog form.

The foundation of DSP is Shannon's sampling theorem, and it states that a signal must be sampled at a rate that is at least twice as high as the highest frequency in the signal's spectrum. In order to implement a DSP system, all you really need is an A/D converter for signal acquisition, a DSP to perform the digital processing, and a D/A converter to transform your processed signal to analog form.

But it's not quite that simple. The Shannon theorem applies to all frequency components and not just the ones you're trying to process. Thus, to avoid aliasing, you must prefilter those signals you intend to process. Any aliasing of the signal precludes the recovery of the original distortion-free signal. Further, the filter can't act like a brick wall. Therefore, in addition to prefiltering, you must sample the signal at a rate higher than the prefilter's cutoff frequency. If you adjust the sampling rate in this way, you avoid aliasing.

After filtering and oversampling the input signal, you also must take into account uncertainties associated with the sampling process. An error voltage associated with the variation in aperture time and uncertainties in the starting time of a sampling aperture can be expressed as

$$e=\Delta V/V \text{ full scale.}$$

In the case of a sinusoidal signal, the error-voltage equation can be written

$$e=2\pi f t_a,$$

where f is the frequency of the sinusoid and t_a is the aperture time of the digitizer. From the error-voltage equation, you can determine the maximum allowable aperture time for a given signal frequency and digitization resolution. **Fig A** illustrates this relationship for 1-LSB error.

Quantization error is also inherent in the digitization process because it's merely a measure of the limits of resolution of your digitizer. If you have a 2-bit ADC, then you can divide the full-scale signal you're sampling into four segments or steps, and the maximum error due to quantization is one-half step. **Fig B** illustrates quantization error as a function of input voltage for a 2-bit ADC.

When you select components for signal acquisition, it's important to consider not just the quantization error but also the aperture error associated with the A/D conversion process. A 12-bit ADC (244-ppm resolution) is wasted in a system where the signal frequency is 100 kHz and the aperture time is over 10 nsec. **Fig C** provides you with a good overview of the resolution and the conversion-rate requirements for a variety of applications.

Once you've digitized your signal, you'll need to determine what format you want the data to appear in. Fixed-point arithmetic provides greater resolution and speed. Floating-point operation, on the other hand, affords you greater dynamic range, but it does generally cost more.

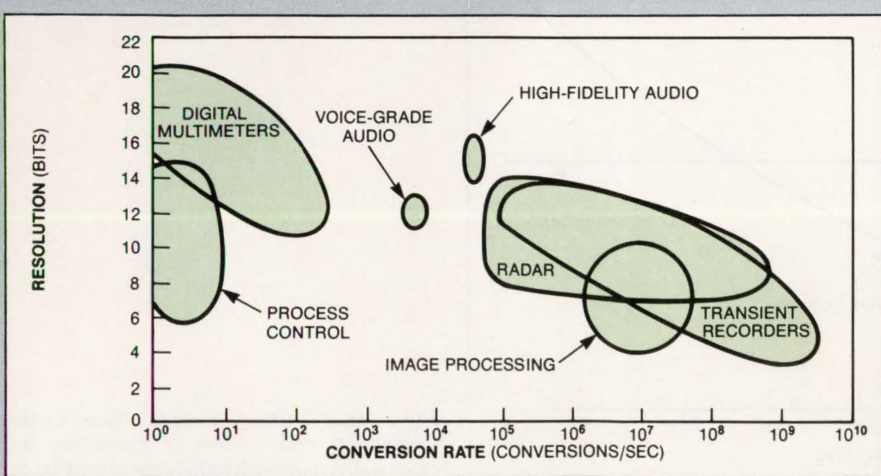

Fig C—The conversion rate and the resolution *determine the application ranges of ADCs. You must consider quantization error, too.*

The inherent stability and extreme flexibility of DSP, together with advances in IC technology, have made it an active player in the signal processing arena.

cascade these devices to increase the basic 256 taps or to increase the throughput of the filter. The chip provides a serial cascade interface that lets you cascade DSPs without using extra circuitry. For example, you can cascade 16 of these chips to fabricate a 4096-tap FIR filter that operates with a maximum sampling frequency of 37 kHz. The input frequency and the number of operations needed to implement the filter determine the maximum sampling frequency.

You can cascade four $110 (1000) ZR33881s from Zoran Corp and achieve a 40-MHz throughput. (These ICs are video-speed filter processors, which means they run at 10 MHz minimum.) The resultant cascading filter has only 16 taps, but it's sufficient for video applications. The ZR33481, ZR33881, and ZR33891 digital filter processors (DFP) from Zoran are all video-speed devices that you can use to implement 1-D and 2-D FIR filters, multibit correlators, and adaptive filters. Each of these devices comprises four (33481) or eight (33881 and 33891) filter cells and features 20-MHz sampling rate, 8- or 9-bit coefficients and data, and shift and add output stages for combining filter outputs. In quantities of 1000, the ZR33481 costs $100; the ZR33891, $150.

Zoran's $230 (1000) ZR34161 vector signal processor (VSP) is aimed at digital image-processing applications. The VSP is optimized for frequency-domain processing, which provides some advantages over spatial-domain processing. Image compression and coding algorithms, feature extraction, spectral analysis of images, and image restoration are some of the applications that benefit from frequency-domain treatment. You can restore an image, for example, by converting it to the frequency domain and de-convolving its spectrum with that of the noise or the blurring that degrades the image. **Fig 5** compares the efficiency achieved by frequency- and spacial-domain treatments and shows how those performances relate to the kernel size of filters and to the number of operations required to implement them.

Choose integer or floating-point operations

The VSP completes a 1024-point block-floating-point complex FFT in 3.3 msec; its 23 high-level instructions operate on complex vectors or arrays of data. The VSP features both integer and block-floating-point execution and 16-bit address and data buses. Block floating-point arithmetic is a method of dealing with overflow in the results of an arithmetic operation. This approach maintains the dynamic range of the processor by shifting results only when an overflow occurs rather than shifting results as a matter of course. The device performs all calculations with an internal accuracy of 17 bits. Its 25-bit accumulators operate with no overflow of the accumulation of 256 17-bit words, a requirement for 128 complex-point dot-product operations.

Video-speed filtering is also the object of the NC45CF8, an NCR FIR filter. The basic filter chip provides 14.5-MHz data-throughput rates on 9-bit data processed with 8-bit coefficients. You can cascade the $170 chip to lengths of either an even or odd number of taps. You can operate the chip in a linear phase mode, in which case it provides you with eight taps per chip, or

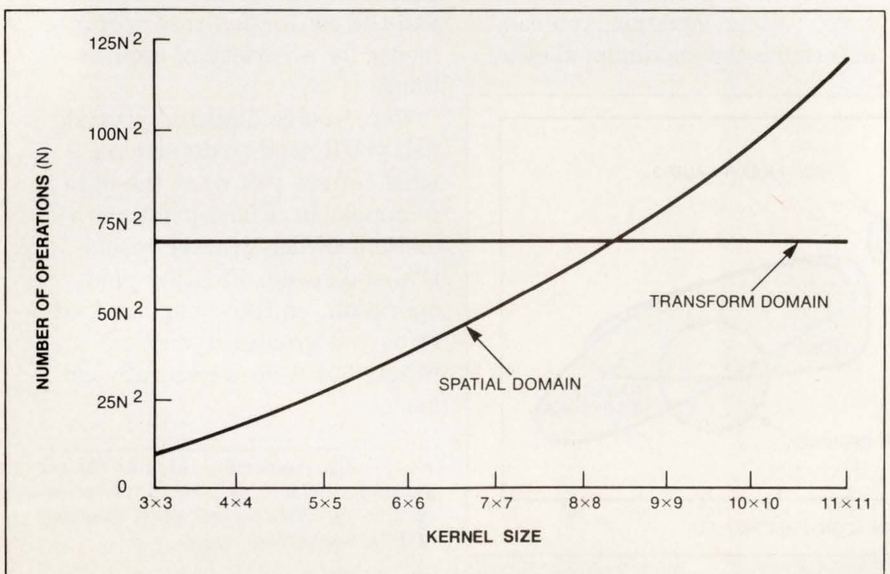

***Fig 5—In 2-D filtering applications,** as the kernel size and number of operations increase, it becomes advantageous to operate in the frequency domain.*

By fetching instructions and data at the same time, the Harvard processor operates much faster than the Von Neumann μP.

For more information . . .

For more information on the DSP products described in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Analog Devices Inc
Box 280
Norwood, MA 02066
(617) 329-4700
Circle No 702

AT&T Technology Systems
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Allentown, PA 18103
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Circle No 703

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Rte 202
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(214) 466-6000
Circle No 709

Zoran Corp
3450 Central Expressway
Santa Clara, CA 95051
(408) 720-0444
Circle No 710

you can operate in a nonlinear phase mode and obtain four taps per chip.

Another family of FIR filters also offers video-rate throughput. The CDSP family, which includes the CDSP100 programmable FIR digital filter, the CDSP110 LMS adaptive FIR filter, and the CDSP200 programmable-length FIFO represent GE/RCA's foray into the DSP arena. The $79 CDSP100 programmable FIR filter features a 20-MHz throughput rate. The chip is organized in a parallel fashion so you can cascade the devices and build higher-order filters without losing speed. The filter accepts 8-bit data and provides 11-bit 2's-complement output. The 11-bit data, however, is truncated to eight bits for output. The part limits truncation noise to less than −60 dB.

The $110 CDSP110 is a least-mean-square adaptive FIR filter that accepts 8-bit input data and produces 12-bit outputs. You can operate the part at 10 MHz and, because it adapts on every cycle, the convergence time (time required for the error signal to be reduced to an acceptable level) is minimized.

The $26 CDSP200 programmable-length FIFO device can write or recirculate from dc to 55 MHz and is programmable in single-delay steps from two to 1281 sample delays. The device comes in 9- or 10-bit dataword versions. You can use the FIFO in applications such as comb filter designs, horizontal delay-lines for high-resolution monitors, and image processing. **EDN**

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Designer's Guide
to Micropower
Circuits—Part 1

Micropower circuits assist low-current signal conditioning

Part 1 of this 2-part series focuses on micropower signal conditioning for the various sensors and transducers that have inherently low impedance or output voltage. Those characteristics can complicate the design of a circuit that must operate at low current and low power. Part 2, scheduled for the August 20 issue, will look at micropower design techniques for the signal conditioning of A/D and V/F converters, of an a S/H circuit, and of several low-power regulator circuits.

Jim Williams, *Linear Technology Corp*

Applications such as medical instrumentation, remote data acquisition, and power monitoring are all excellent candidates for battery operation, making low power consumption increasingly desirable in electronic apparatus. Micropower analog circuits for transducer-based signal conditioning present their own special problems. Although ICs that operate at low current are available, the interconnection of these devices to form a micropower circuit requires care (see **box**, "Designing micropower circuits: some guidelines"). In particular, tradeoffs between signal levels and power dissipation become painful when you want good performance in the 10- to 12-bit range. Also, many transducers intrinsically produce small outputs, complicating an already difficult situation when dealing with micropower requirements. Despite these problems, the design of micropower circuits is possible by using high-performance, low-current-drain ICs with the appropriate circuit techniques.

Fig 1 illustrates a simple circuit for signal conditioning a platinum RTD (resistance temperature detector); the circuit includes correction for the sensor's nonlinear response. The circuit accuracy is ±0.25°C over a sensed range of 2 to 400°C. To improve noise immunity, you should connect one side of the sensor to ground. Current consumption is 250 μA for a sensed temperature of 2°C and increases to 335 μA at 400°C. You connect the platinum sensor in a current-driven bridge with the 1-kΩ resistors.

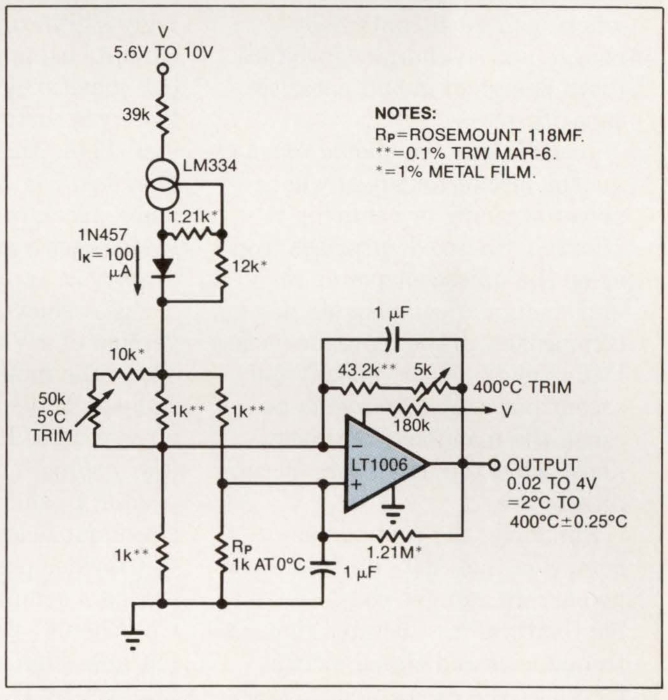


***Fig 1—This signal-conditioning circuit** for a platinum temperature sensor includes correction for the sensor's nonlinear response. Current drain is 250 μA at a 2°C sensed temperature, increasing to 335 μA at 400°C.*

Text continued on pg 126

Designing micropower circuits: some guidelines

The most obvious way to save power is to choose components that use little energy. Although they require more effort, some subtler procedures can give you additional savings. First, you should examine the circuit current flow in terms of all ac and dc paths. Check, for example, to see that dc base currents are going where they can do some useful work. Try to minimize ac signal swings, particularly where you must continually charge and discharge capacitors (both designed-in and parasitic capacitors).

In addition, you should examine the circuit for areas where power strobing or sampling is possible. To avoid surprises, consider the quiescent power requirements of components in comparison to the dynamic ones. Data sheets usually specify quiescent power requirements because the manufacturer doesn't know what the user's circuit conditions are.

Similarly, the common assumption that MOS devices draw no current can get you into trouble. Natural law dictates that, as frequencies and signal swings increase, the capacitances associated with MOS devices begin to require more power. So it's often a mistake to associate low-power operation with any particular process technology. Although it's likely that CMOS will provide lower power operation than a 12AX7 vacuum tube, a bipolar approach may be even better. In the end, you might opt for a combination of technologies—CMOS and bipolar ICs, for example, along with discrete transistors and diodes—for best results.

Obtaining low-power operation usually requires performance tradeoffs. Minimizing signal swings and current drain saves power, but it also moves circuit operation closer to the noise floor. As you constrict signal amplitudes to save power, you'll find that offsets, drift, bias currents, and noise become increasingly significant error factors. Circuits using power strobing can sometimes avoid this problem by resorting to low duty cycles. Using this technique, the circuit in **Fig 3** (pg 127), for example, achieves dramatic power savings with an on-state current drain that approaches 20 mA.

Fig A shows a rudimentary version of a V/F converter. When the input current-derived ramp at IC_{1A}'s negative input crosses zero, IC_{1A}'s output drops low, pulling a charge through capacitor C_1 and forcing the negative input below zero. Capacitor C_2 provides positive feedback, allowing a complete discharge for C_1. When C_2 decays, IC_{1A}'s output goes high and clamps at the level set by D_1, D_2, and V_{REF}. C_1 receives a charge, and recycling occurs when IC_{1A}'s negative input again reaches zero. The frequency of this action relates to the input voltage. Diodes D_3 and D_4 steer, while diodes D_1 and D_2 provide temperature compensation. The sink saturation voltage of IC_{1A} is small and uncompensated. IC_{1B} acts as a start-up loop.

Although the LT1017 and LT1034 have low operating currents, the circuit in **Fig A** draws almost 400 µA. The ac-current paths include C_1's charge-discharge cycle and C_2's branch circuit. The dc path through D_2 and V_{REF} is particularly costly. C_1's charging must occur quickly enough for 10-kHz operation—that is, the clamp seen by IC_{1A}'s output must have a low impedance at that frequency.

Capacitor C_3 helps, but you still need significant current to keep the impedance low. IC_{1A}'s current-limited output cannot do the job alone; it uses the supply's resistor to help in keeping the impedance low. Even if IC_{1A} could supply the necessary current, V_{REF}'s settling time would be an issue.

Dropping C_1's value reduces the impedance requirements proportionally and seems to solve the problem. Unfortunately, such a reduction magnifies the effects of stray capacitance

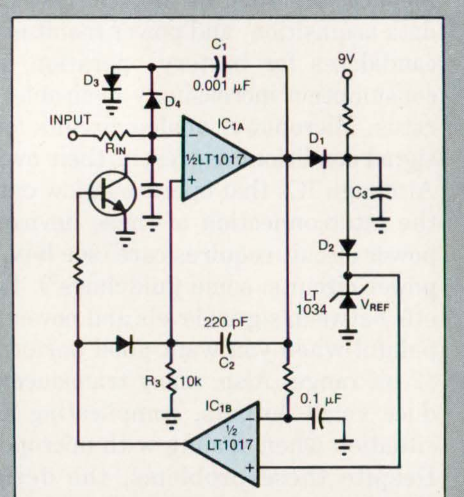


Fig A—This rudimentary version of a V/F converter *draws almost 400 µA. The dc path through D_2 and V_{REF} is particularly costly.*

at the D_3-D_4 junction. It also mandates an increase in the value of R_{IN} to keep the scale factor constant. This increase lowers the operating currents at IC_{1A}'s negative input and thus makes bias current and offset more significant sources of error.

Attacking the problems

Fig B shows an initial attempt at dealing with these issues. This scheme is similar to **Fig A**'s, except for the addition of Q_1 and Q_2. Instead of being on all the time, V_{REF} now receives switched bias via Q_1, and Q_2 provides the sink path for C_1. These transistors invert IC_{1A}'s output, requiring an exchange in its input-pin assignments. Resistor R_1 provides a small current from the supply, improving the reference settling time. This arrangement decreases supply current to about 300 μA.

Several problems remain, however. The switched operation of Q_1 is really only effective at higher frequencies. In the lower ranges, IC_{1A}'s output is low most of the time, biasing Q_1 on and wasting power. Also, when IC_{1A}'s output switches, Q_1 and Q_2 simultaneously conduct during the transition, effectively shunting R_2 across the supply. Finally, the base currents of both transistors flow to ground and are lost. The basic temperature compensation is thus the same as before, except that Q_2's saturation term replaces that of the comparator.

Fig C presents a better solution. Q_1 is gone, but Q_2 remains with the addition of Q_3, Q_4, and Q_5. V_{REF} and its associated diodes receive bias from R_1. Q_3 is an emitter follower and sources current to C_1. Q_4 provides temperature compensation for Q_3's V_{BE}, and Q_5 switches Q_3.

This method has some distinct advantages. The V_{REF} string can operate at greatly reduced current because of Q_3's current gain. Also, the simultaneous conduction problem in **Fig B** is largely alleviated because Q_2 and Q_5 are switched at the same voltage threshold from the output of IC_{1A}. Q_3 delivers its base and emitter currents to capacitor C_1. Q_5's currents are wasted, although they are much smaller than Q_3's. Q_2's small base current is also lost. The circuit design changes the values for C_2 and R_3. The time constant is the same, but some current reduction occurs because of the increase in the value of R_3.

If, for performance reasons, you cannot reduce the value of C_1, then you must accept its ac currents. The only significant wasted values are the Q_2 and Q_5 currents, along with the now smaller R_1 loss. Current drain for this circuit is about 200 μA max.

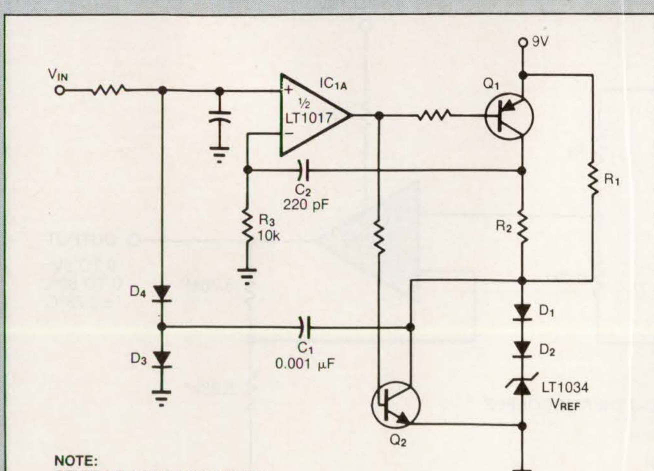


Fig B—This improved version of the Fig A circuit needs only 300 μA of current. Instead of being on continuously, V_{REF} now receives switched bias.

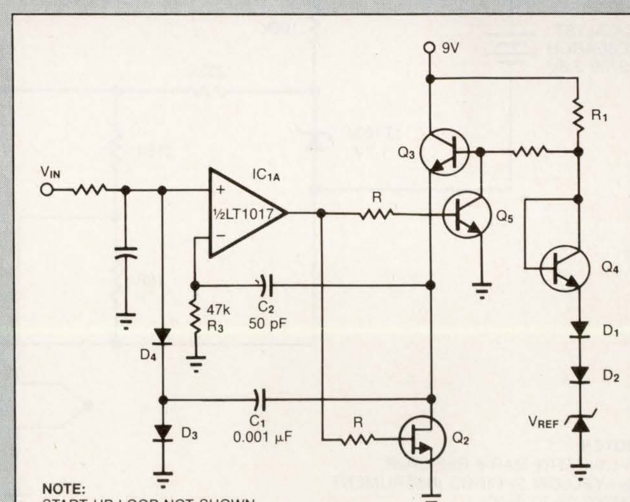


Fig C—Needing only 200 μA, this circuit operates the V_{REF} string at greatly reduced current.

ICs that operate at very low currents do not, by themselves, guarantee the successful design of micropower circuits. Techniques are of equal importance.

The LM334 current source drives the bridge at an operating current of 100 μA, determined by the bridge's equivalent resistance. The 1N457 diode in series with the bridge provides temperature compensation. By reducing the voltage across the LM334, the 39-kΩ resistor minimizes its temperature rise and ensures its closer temperature tracking with the diode. The low current of 100 μA, which is split by the bridge, restricts the platinum sensor's output to about 200 μV/°C.

To achieve a circuit accuracy of ±0.25°C and stable gain, you should use a low-power precision op amp like the LT1006. The LT1006 takes the signal differentially from the bridge to provide the circuit's output. The platinum sensor's slightly nonlinear response normally causes several degrees of error over the sensed temperature range, but the 1.21-MΩ resistor provides a slight positive feedback to correct for this error. The amplifier's negative feedback path dominates, and the circuit configuration is stable. The 1-μF capacitor rolls off the circuit's high-frequency response, and the 180-kΩ resistor programs the LT1006 for 80 μA of quiescent current.

Use decade box for calibrating

To calibrate this circuit, you can substitute a precision decade box (such as the General Radio #1432) for R_P. Set the box to the 5°C value (1019.9Ω) and adjust the 5°C trim for 0.05V at the output of the LT1006. Next, set the box for the 400°C value (2499.8Ω) and adjust the 400°C trim for 4.00V output. Repeat this sequence until both points remain fixed.

The resistance values set by the decade box are for a nominal 1000.0Ω (0°C) sensor. You can use sensors deviating from this nominal value by factoring in the deviation from 1000.0Ω. Because it is an offset value that arises from winding tolerances during the fabrication of the RTD, the manufacturer specifies this deviation for each individual sensor. The platinum's gain slope, which is primarily fixed by the purity of the material, is a very small error factor.

The temperature-sensing circuit in **Fig 2** uses a thermocouple as the transducer. It is accurate within 1.5°C over the sensed temperature range of 0 to 60°C. Current consumption is about 125 μA.

Not only are thermocouples inexpensive, they have low impedance and generate their own outputs. They do, on the other hand, produce low-level outputs and require cold-junction compensation, both of which complicate signal conditioning. The bridge network, composed of a thermistor and its associated resistors, provides cold-junction compensation with the LT1004 acting as a voltage reference. The lithium battery lets the bridge float and also lets the thermocouple have a ground reference, thereby eliminating the need for a multi-amplifier differential stage with its attendant

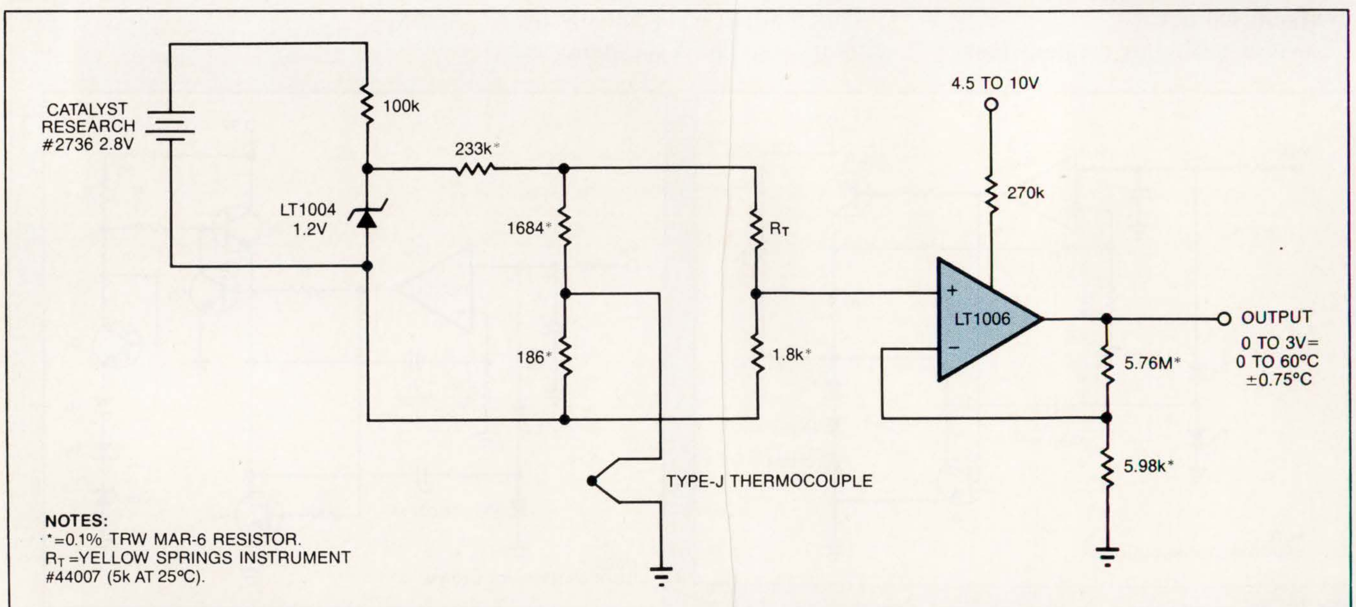


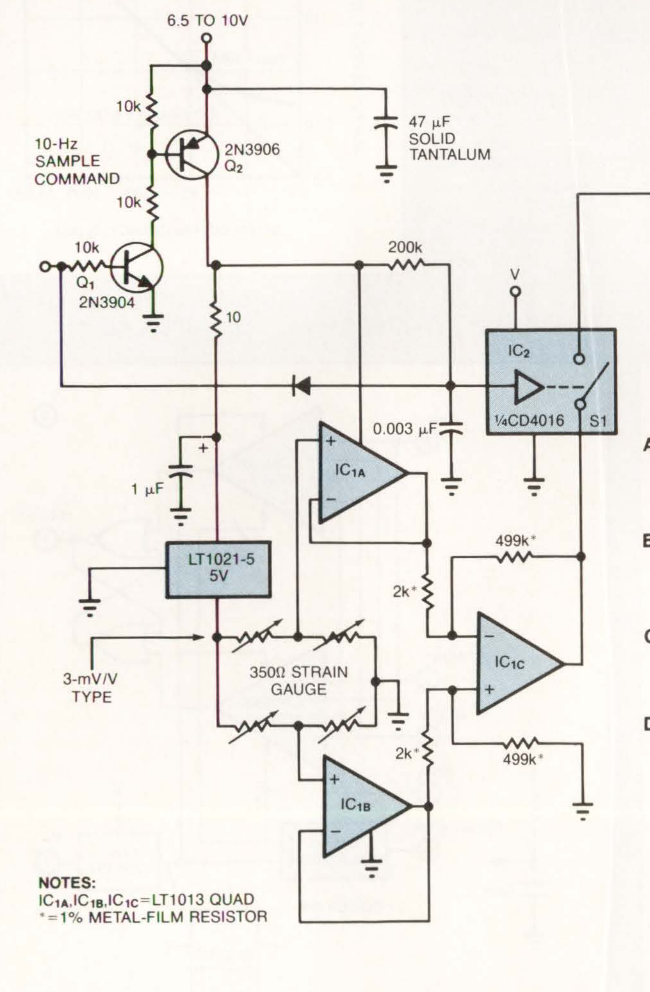
Fig 2—This thermocouple-type temperature-sensing circuit features cold-junction compensation *and is accurate within 1.5°C over a 60°C temperature range. Current-drain is about 125 μA.*

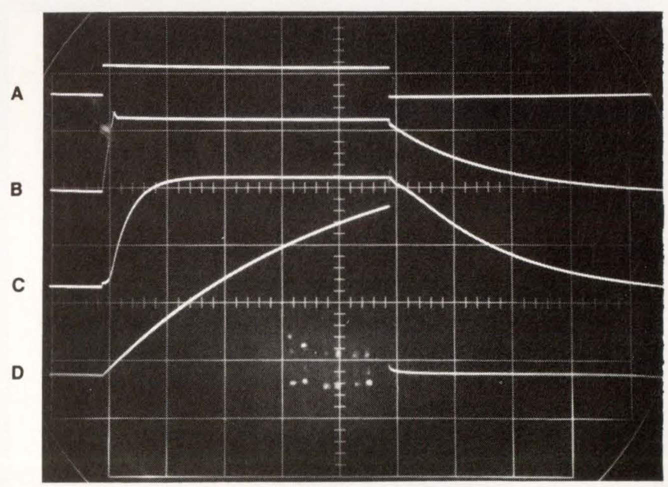
power drain. (The battery specified in the figure is supposed to last nearly 10 years.) The gain adjustment of the LT1006 provides the output shown, and the 270-kΩ resistor programs the IC for low current drain. Note that this circuit requires no trimming.

Bridge-based, strain-gauge transducers present a challenge for low-power designs. Some common values for the transducers are a 350Ω impedance and a low output signal (typically 1 to 3 mV per volt of drive), and these common values create problems for low-power designs. Even with only 1V of drive, the bridge current consumption approaches 3 mA. Reducing the drive to 100 mV drops the current to acceptable levels, but precludes any great accuracy because of the minuscule output available.

In many situations, continuous transducer information is unnecessary, and consequently a sampling operation is viable. Sampling at a low duty cycle permits a high-current bridge drive while keeping the average power consumption low (see **box,** "Sampling techniques reduce circuit current"). **Fig 3** uses such a scheme to achieve dramatic power savings in a strain-gauge bridge application.

In the circuit of **Fig 3,** Q_2 is off when the sample command is low. Under these conditions, only the LT1006 and the CD4016 receive power, and the current





TRACE	VERTICAL	HORIZONTAL
A	20V/DIV	200 µSEC/DIV
B	4V/DIV	200 µSEC/DIV
C	0.5V/DIV	200 µSEC/DIV
D	2V/DIV	200 µSEC/DIV

Fig 3—Strain-gauge bridge-type transducers present problems *in achieving low-current operation because of their low impedance and low output signals. The circuit shown in* ***a*** *uses a sampling approach to lower the average current. The operating waveforms shown in* ***b*** *are described in the text.*

Sampling or strobing techniques can drastically reduce the average current drain in many circuits while still providing full drive power when needed.

drain is less than 125 μA. When the sample-command pulse goes high, the collector of Q_2 (trace A, **Fig 3b**) goes high, providing power to all other circuit elements. The 10Ω resistor and the 1-μF capacitor at the input of the LT1021 prevent the strain bridge from having to handle a fast-rising pulse, which could cause long-term transducer degradation.

The LT1021-5 reference output (trace B) drives the strain bridge, and the output of the differential amplifier IC_{1A}, IC_{1B} appears at IC_{1C} (trace C). At the same time, S_1's switch-control input (trace D) ramps toward Q_2's collector. At about half of Q_2's collector voltage (in this case, just before midscreen), S_1 turns on, and the output of IC_{1C} charges capacitor C_1. When the sample command drops low, Q_2's collector falls, the bridge and its associated circuitry shuts down, and S_1 turns off.

Sampling techniques reduce circuit current

The best way to achieve low-power circuit characteristics is to turn off the power. Obviously, there are some problems with this approach, but in many applications, continuous circuit power is not necessary. If bandwidth requirements are low, sampling techniques offer a simple way to save power. With low duty cycles, instantaneous current can be relatively high, and average current drain remains low.

One of the issues you need to examine when considering a sampling approach is that the desired circuit bandwidth dictates the minimum sampling frequency in accordance with Nyquist criteria. The circuit's settling time (to the desired accuracy) determines the required duration of the sampling interval.

You should consider this settling time for all circuit elements (transducers, ICs, and discrete components) separately and together. You should also examine the effects of a sampled operation on component life and oper-

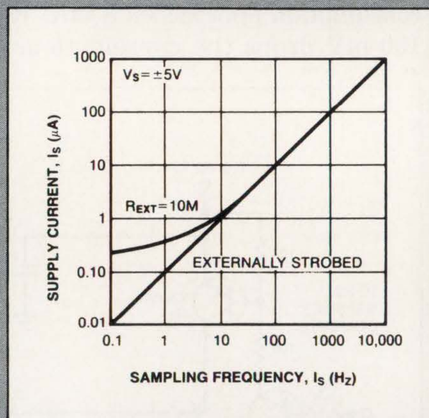


Fig B—This graph plots supply current vs frequency *for the circuit in* ***Fig A.***

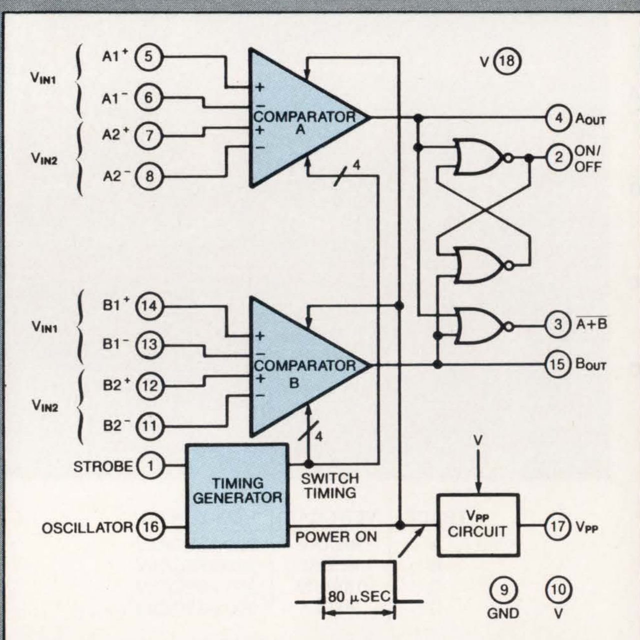


Fig A—The output of the LTC1040 dual comparator *supplies power only during the programmed sampling interval.*

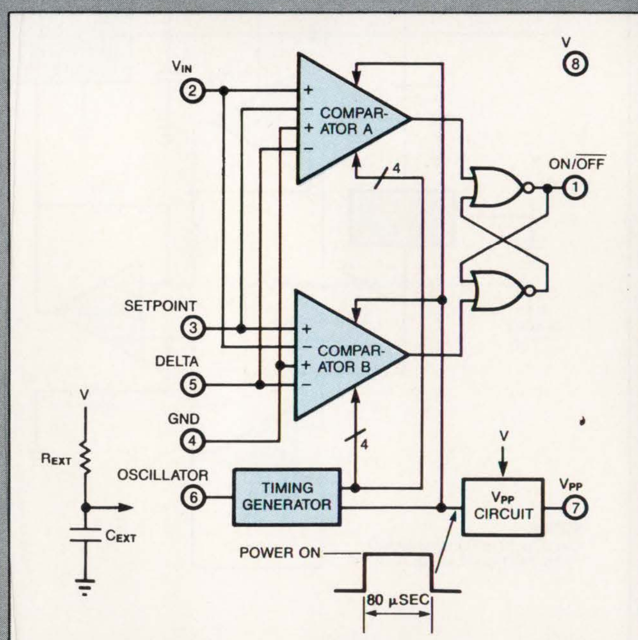


Fig C—The LTC1041 shown here *is dedicated to on-off servo operation.*

Capacitor C_1's stored value appears at the gain-scaled output of the LT1006 (IC_3).

By preventing the updating of C_1 until IC_{1C} settles, the RC delay at S_1's control input ensures glitch-free operation. During the 1-msec sampling phase, supply current approaches 20 mA, but the 10-Hz sampling rate cuts the effective current drain below 200 μA. Slower sampling rates will further reduce current drain, but C_1's droop rate (about 1 mV/100 msec) limits the accuracy. The 10-Hz rate provides adequate bandwidth for most transducers. The gain trimming shown allows calibration for 3-mV/V slope-factor transducers. You should rescale the trimming for other types. The current drain of this circuit is about 300 μA, and the output is accurate enough for 12-bit systems.

By switching most of the power into the circuit, the

ating characteristics. This latter issue is particularly important in the case of transducers, which are often designed and tested under dc operating conditions.

The LTC1040, 1041, and 1042 are specifically designed for sampled operation. **Fig A** details the LTC1040 dual micropower comparator. Its programmable internal oscillator sets a sampling rate with an interval lasting 80 μsec. The V_{PP} output supplies power during the sampling interval, thereby providing drive for the external circuitry or transducers. Note that the input common-mode range includes both rails. **Fig B** plots supply current vs sampling frequency.

The LTC1041 is shown in **Fig C**. Although similar to the 1040, it is specially dedicated to on-off servo loops. You can control the servo setpoint and delta at the inputs. The **Fig D** diagram graphically defines its operation. The operating current is similar to the 1040's.

The final example, the LTC1042, is also similar to the 1040, but it's laid out as a window comparator. Its internal construction is shown in **Fig E**, and its graphic operation, in **Fig F**. The operating current, input range, and sampling characteristics are similar to the LTC1040's and 1041's.

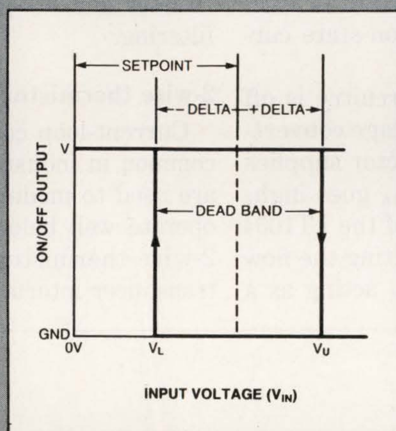


Fig D—This plot of the LTC1041's setpoint and delta graphically defines its operation.

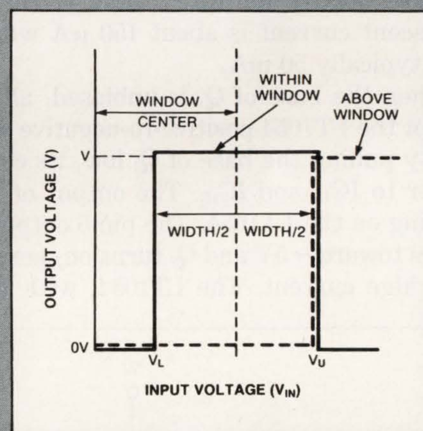


Fig F—This graph illustrates the window characteristics of the LTC1042 comparator.

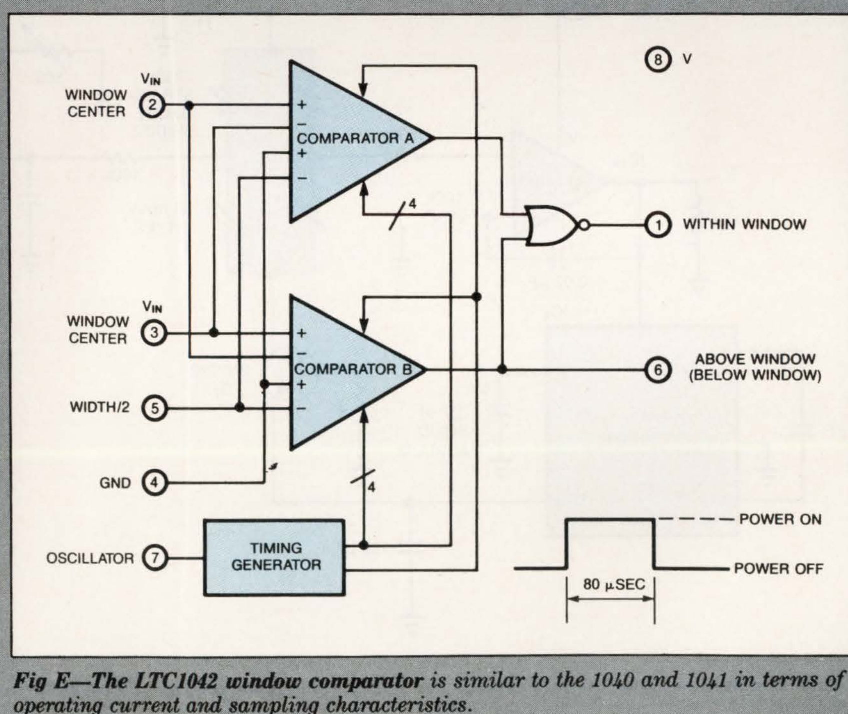


Fig E—The LTC1042 window comparator is similar to the 1040 and 1041 in terms of operating current and sampling characteristics.

The low impedance and low output-voltage of many transducers present special problems in the design of micropower circuits.

circuit in **Fig 4** helps to reduce losses caused by the strain-gauge bridge. Rather than operate in a continuously sampled mode, this circuit sits in a quiescent state for long periods, with relatively brief on times.

A typical application for this circuit is the remote measurement of the contents of a storage tank when weekly readings are sufficient. Despite the floating output of the strain-gauge bridge, the circuit has the advantage of not needing a differential amplifier. In addition, it improves measurement accuracy because it provides nearly full-rated drive to the strain bridge. Quiescent current is about 150 μA with on-state current typically 50 mA.

When the base of Q_1 is unbiased, all circuitry is off except the LT1054 positive-to-negative voltage converter. By pulling the base of Q_1 low, its collector supplies power to IC_{1A} and IC_{1B}. The output of IC_{1A} goes high, turning on the LT1054. The pin 5 output of the LT1054 heads toward −5V and Q_2 turns on, permitting the flow of bridge current. The LT1054, with IC_{1A} acting as a servo, balances the inputs to the bridge and drives the midpoint of the bridge to 0V. The bridge ends up with about 8V across it, and so requires the LT1054, which can handle 100 mA, to sink about 24 mA. The 0.02-μF capacitor then stabilizes the loop.

The negative output of the IC_{1A} and LT1054 loop sets the common-mode voltage of the bridge to zero, allowing IC_{1B} to make a simple single-ended measurement. The output trim adjustment scales the circuit for a 3-mV/V strain-gauge bridge transducer. The 100-kΩ resistor and 0.1-μF capacitor together provide noise filtering.

2-wire thermistor needs no external supply

Current-loop control in the range of 4 to 20 mA is common in industrial environments, and circuits that are used to modulate data into this type of loop must operate well below the 4-mA minimum current. The 2-wire thermistor used in a complete temperature-transducer interface (**Fig 5**) has an output in the 4- to

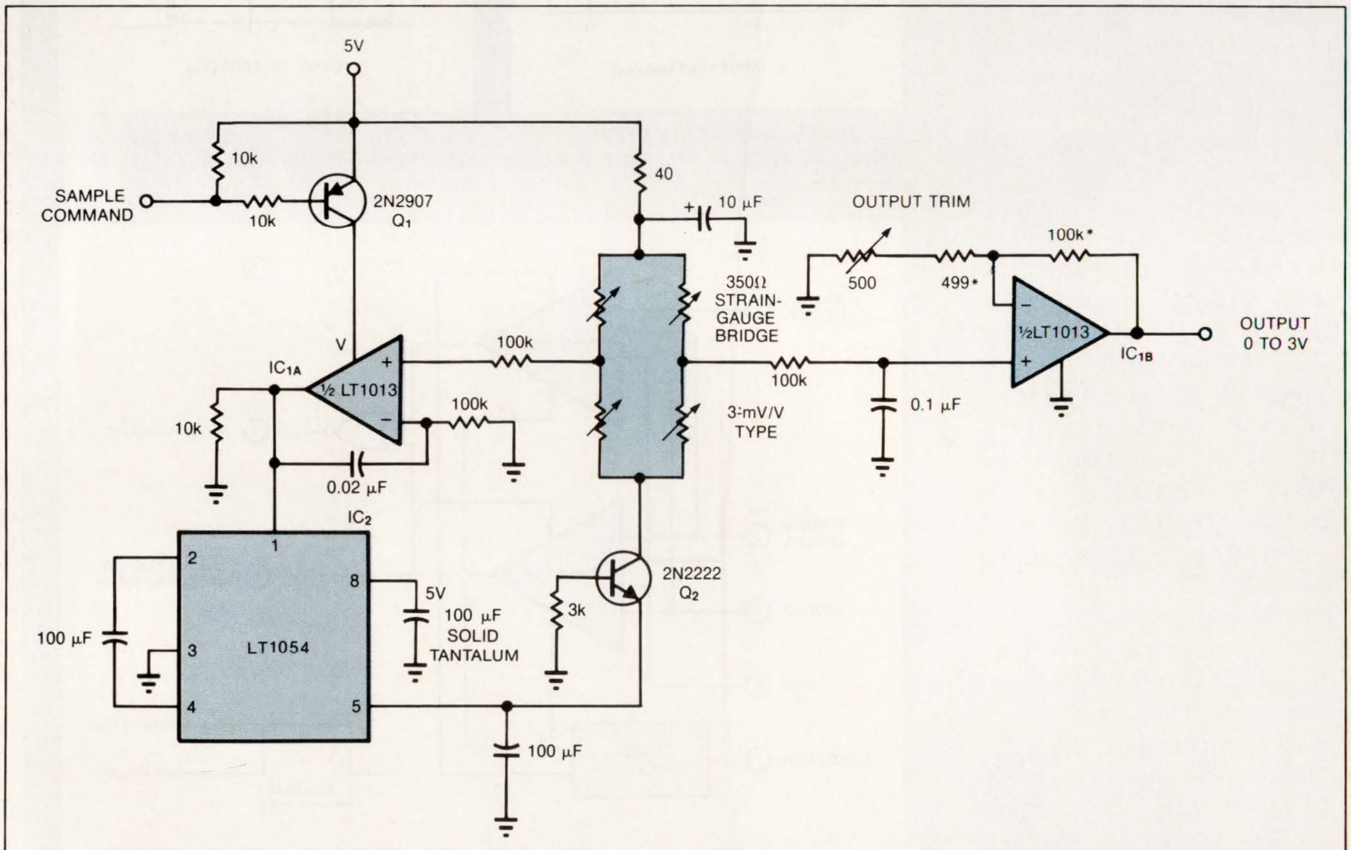


Fig 4—The strobed operation of this circuit uses only 150 μA of quiescent current. *Full-rated drive up to 50 mA occurs only on command.*

20-mA range. Accuracy for this current-loop circuit is ±0.3°C over a 0 to 100°C range. The circuit does not require an external supply.

By fixing the current well below the 4-mA minimum, the LM134 current source saves the LTC1040 from having to handle too high a supply voltage (see **box,** "Sampling techniques reduce circuit current"). The LTC1040 senses the thermistor-network output and forces this voltage across the output resistor to set the total circuit current. You can adjust the current by varying the gate voltage of the 2N6657 FET. The comparator output operates in a PWM mode, with the FET-gate voltage filtered by the 1-MΩ resistor and the 1-µF capacitor.

An important feature of the LTC1040 is that very little current—something on the order of nanoamperes—flows from the V− supply. The V− supply therefore connects to ground with negligible current error in the output-sensing resistor. The differential input of the LTC1040 can sense the current through the output resistor because its common-mode range includes the V− supply. You make the trimming adjustments for 0 and 100°C (full scale) by exposing the thermistor to those temperatures or by electrically simulating those conditions.

Fig 6 shows a circuit for a battery-powered thermostat using the LTC1041 and a bridge-connected thermistor to sense the temperature. A potentiometer at the output of the bridge provides a means of setting the temperature. The power for driving the bridge comes

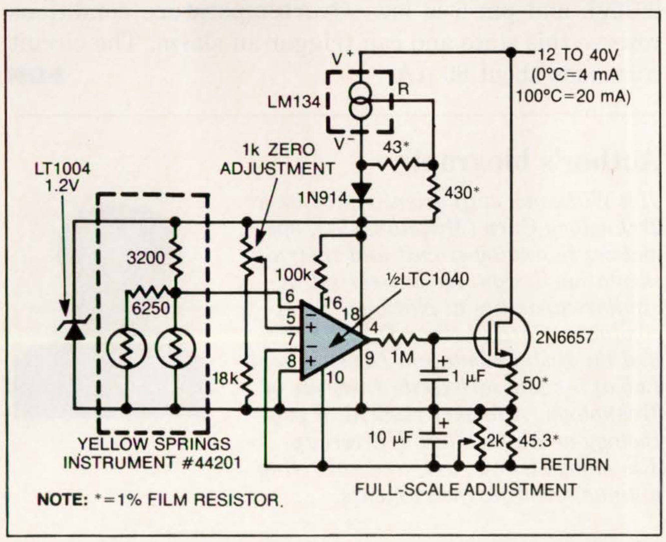


Fig 5—This 2-wire thermistor signal-conditioning circuit requires no external supply. *Powered by a current-loop, the circuit accuracy is ±0.3°C over a 100°C range.*

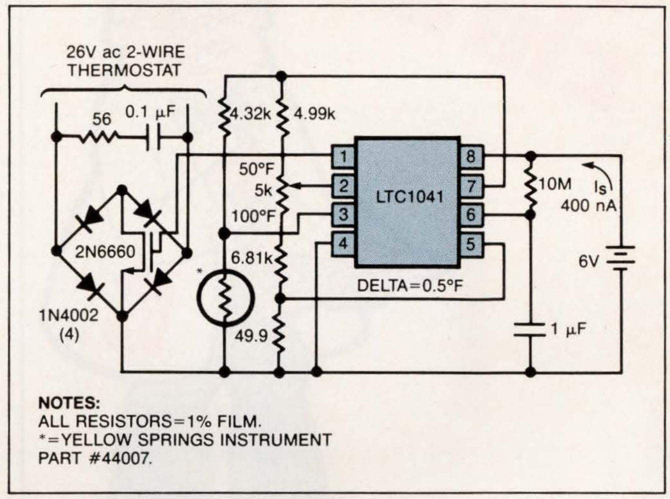


Fig 6—This thermistor-based temperature-sensing circuit uses pulse techniques to limit the current to 1 µA. *With a lithium battery, this circuit can operate for over 10 years.*

from pin 7 of the LTC1041, not from the battery. Pin 7 is the pulse-power (V_{PP}) output and only turns on when the LTC1041 samples the inputs. A system's average power consumption when this technique is used turns out to be quite small: In this application, total system current is less than 1 µA. This is far less than the self-discharge rate of the battery. A lithium battery can operate this circuit for over 10 years.

An external R-C network sets the sampling frequency. The initiation of an internal sampling cycle turns on power to the comparators and the V_{PP} output. The CMOS latches in the LTC1041 store the resulting outputs of the sampled analog inputs. After the sampling, the circuit switches off the power but keeps the outputs on. The unclocked CMOS logic consumes negligible current.

The sampling process takes approximately 80 µsec. During this interval, the LTC1041 draws about 1.7 mA of current from the 6V supply. Because the sampling rate is low, average power consumption is extremely small. The low sampling rate is adequate for a thermostat, however, because of the low rate of change associated with temperature.

A power MOSFET in the diode bridge switches 26V ac to the heater control circuitry. The MOSFET is a voltage-controlled device that requires no current from the battery. The voltage from pin 5 (DELTA) to pin 4 (GND) sets the dead band. The dead band, which is desirable to prevent excessive cycling in the heating unit under control, equals two times DELTA and is independent of both V_{IN} (pin 3) and setpoint (pin 2).

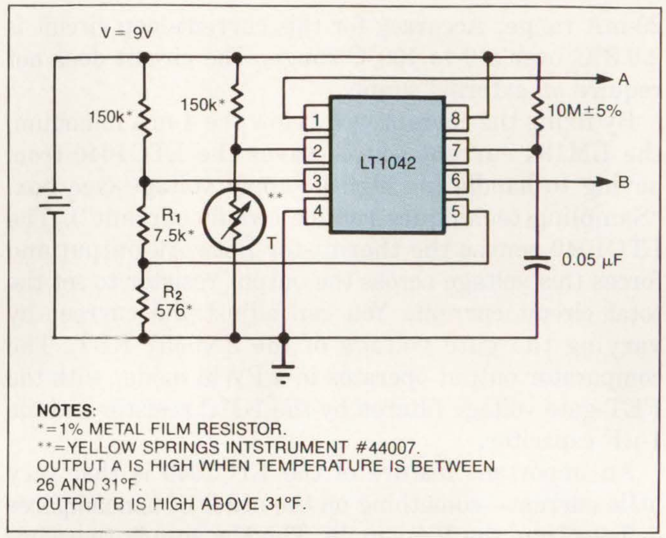
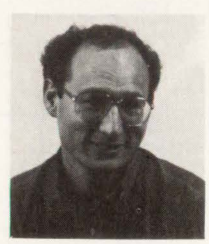


***Fig 7—This simple freezer-alarm circuit draws only 80 µA of current** and uses the LTC1042 as a sampling window-comparator.*

Thus as you vary the setpoint, the dead band remains fixed at two times DELTA. Conversely, as you vary the dead band, the setpoint stays the same.

Fig 7 is a very simple configuration for a freezer alarm. Circuits such as this one are useful in industrial and home freezers as well as in refrigerated trucks and rail cars. The LTC1042 acts as a sampling window comparator. The 10-MΩ resistor and 0.05-µF capacitor set a sampling rate of 1 Hz and the bridge-network values program the internal window comparator for the outputs shown. During normal freezer operation, pin 1 is high and pin 6 is low. Overtemperature conditions reverse this state and can trigger an alarm. The circuit consumes about 80 µA. **EDN**

Author's biography



Jim Williams, staff scientist at Linear Technology Corp (Milpitas, CA), specializes in analog-circuit and instrumentation design. He has served in similar capacities at National Semiconductor Corp, Arthur D Little Inc, and the Instrumentation Development Lab at the Massachusetts Institute of Technology. A former student of psychology at Wayne State University, Jim enjoys tennis, art, and collecting antique scientific instruments.

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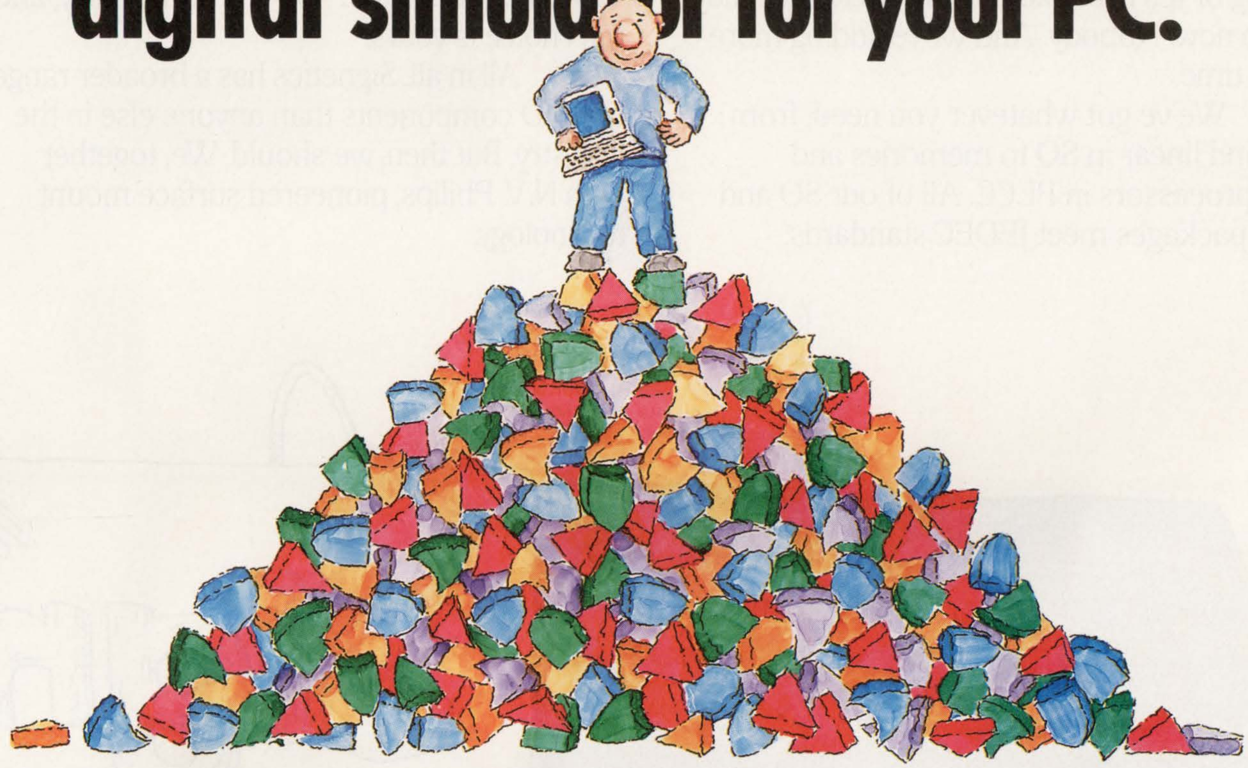

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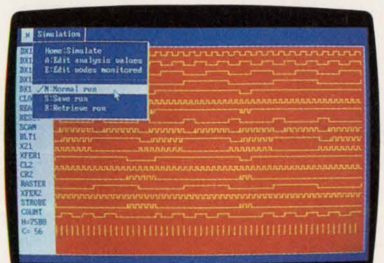

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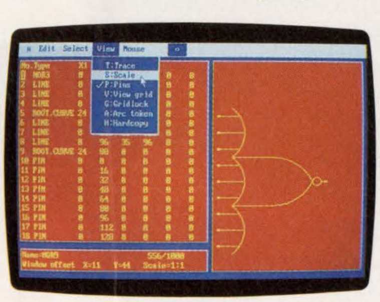

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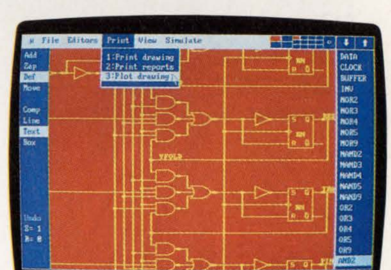

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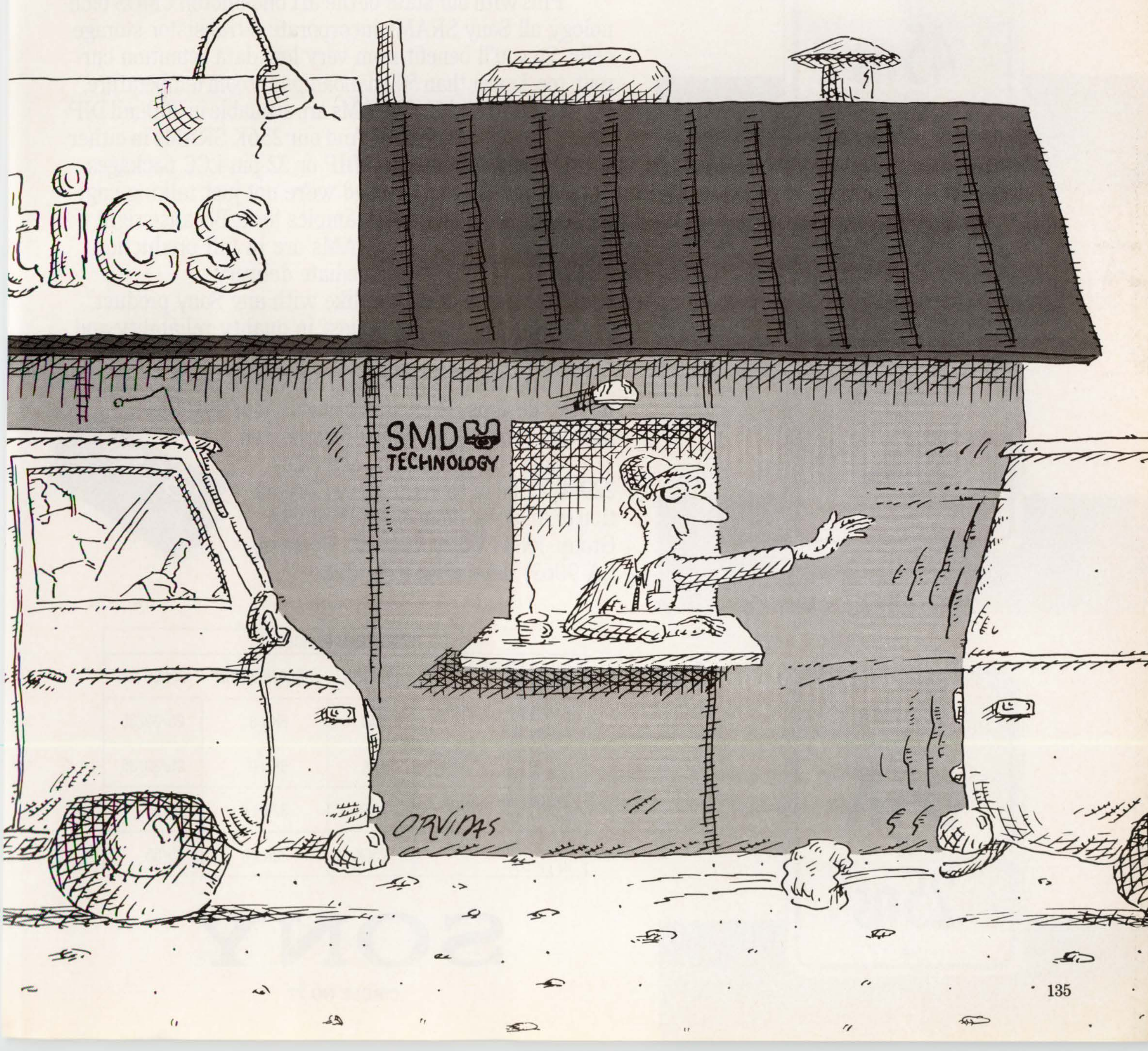

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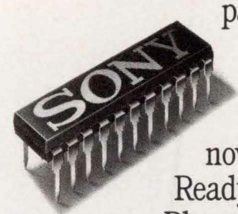

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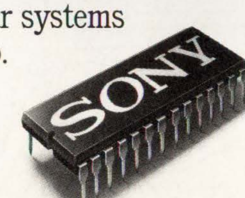

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CXK58255P—45/55 600 mil DIP	256K	32K x 8	45/55
CXK58255K—45/55 32 pin LCC	256K	32K x 8	45/55

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Sequential-test techniques maximize throughput in tests

You're wasting time if you test an obviously defective system as thoroughly as a system that comes close to meeting its specification. By performing a sequential test, which evaluates results after each trial, you can determine whether a system warrants further testing.

R F Cobb, *Harris Corp*

When you test a system that has statistical specifications, you can't measure the system's characteristics exactly. You have to measure the system repeatedly and determine the mean of the results. Clearly, this type of test takes a long time, but you can shorten the length of your test by measuring each system only long enough to determine whether the system meets its specifications.

Your test should be able to determine when the outcome is predictable enough to discontinue testing. You shouldn't need to test a unit that is far better or worse than its specification for as long as you test a system that is marginal. Once you know whether a unit passes or fails, further testing is unproductive.

You can determine the certainty of the result of your test by using the sequential test. To conduct such a test, you pose a null hypothesis (H_0) and calculate the minimum number of trials needed to dismiss or accept the hypothesis. **Ref 1** describes the hypothesis test.) The sequential test requires only a few trials if the equipment is far better or far worse than required. For equipment that comes close to its specifications, the test lasts longer.

The sequential test is an extension of the likelihood-ratio test, and thus both tests use the same basic equations. (For a review of these equations, see **box,** "Equations are key to sequential-test comprehension.") However, the likelihood-ratio test isn't intelligent, and the sequential test is. The number of trials (n) in a sequential test isn't a predetermined number: The sequential test assesses the need for more trials as a test progresses.

Suppose, for example, that you're testing a receiver for a bit-error rate of 10^{-5} and you've determined that, to obtain your desired probabilities of error α and β, you need $n=10^7$ trials and a mean (m) that is $\leq 2\times10^{-5}$. Thus, $n\times m$ must be less than or equal to 200—the unit fails if you record 201 errors.

Now assume that you measure 90 errors during the first 10^3 bits. The receiver will fail if you record 111 errors in the next 9.999×10^6 bits. Considering that you've recorded a bit-error probability of 9×10^{-2} already, you'll almost surely record a bit-error probability greater than 1.11×10^{-5} during the remainder of the test. The receiver is almost certain to fail, so further tests are a waste of time. In this example, the outcome is obvious. But when the outcome is less obvious, you can still use the sequential test to justify terminating a test.

Because the number of samples in a sequential test isn't fixed, you need more samples when θ_0 and θ_1 are nearly equal than when they differ by a great amount. You also need a large number of samples if you want to minimize the probability of error.

To calculate a likelihood ratio for a sequential test, start by choosing a pair of constants, A and B (**Ref 2**):

$$0<B<1 \qquad 1<A<\infty.$$

The likelihood ratio for the sequential test λ is the

The number of trials in a sequential test isn't a predetermined number—the sequential test assesses the need for more trials as the test progresses.

reciprocal of the general likelihood ratio λ_L,

$$\lambda = \frac{P(x_1|\theta_1)P(x_2|\theta_1)\ldots P(x_n|\theta_1)}{P(x_1|\theta_0)P(x_2|\theta_0)\ldots P(x_n|\theta_0)}. \qquad (1)$$

There's no mathematical reason for inverting the ratio —it's simply a matter of convention.

After i trials, compute the likelihood ratio $\lambda(i)$ and

if $\lambda(i) \le B$, accept H_0;
if $\lambda(i) \ge A$, reject H_0;
if $B < \lambda(i) < A$, take another sample.

The sequential test is like the general likelihood-ratio test in that, after a number of trials, you compare λ to a constant and decide whether to accept or reject H_0. But, in contrast to the likelihood-ratio test, the constants A and B replace the single constant k. Moreover, you compute λ after each trial. The two constants determine whether a test has reached the stage where you can make a decision.

Sequential test has potential drawbacks

Although you must continue testing until λ falls outside a certain range, all sequential tests end after a finite number of samples **(Ref 2)**. Nonetheless, the number of trials can be large, and therefore you should set a cap on the number of samples. This cap can distort test statistics, of course, but if you specify a cap large enough so that you conclude most tests before the cap is reached, the effect is negligible.

The sequential test has two disadvantages. First, because you must check your results after every trial, the test can't be left to run unattended. Second, it's hard to characterize the test's key performance parameters: its accuracy and efficiency.

Calculate the comparison thresholds

To analyze the probability that a sequential test will give an erroneous result, you must begin by calculating the values of the comparison thresholds A and B. Set A and B to produce your desired values of α and β. If you choose

$$A = \frac{1-\beta}{\alpha}$$

$$B = \frac{\beta}{1-\alpha}$$

the sensitivity of your test will be very close to what you want. The bounds on the actual performance parameters, α' and β', are

$$\alpha' \le \frac{\alpha}{1-\beta}$$

$$\beta' \le \frac{\beta}{1-\alpha}.$$

Because α and β are both small, the actual values of the error probabilities, α' and β', can't be much larger than the desired values of the error probability, α and β. In fact, because the definitions of α' and β' specify upper boundaries, the actual values of α' and β' are often lower than your planned values.

Try a Gaussian distribution of samples

Eq 1 indicates that solving for λ in a test with n trials requires 2n multiplications. However, it's often possible to implement a sequential test without multiplying. You can calculate the likelihood ratio for a continuous Gaussian random variable by taking the natural logarithm of **Eq 1.** For a Gaussian distribution having a known variance σ^2 and an unknown mean μ, the logarithm of the likelihood ratio reduces to a simple sum of the values taken at each sample. The likelihood ratio at the nth sample is

$$\lambda' = \sum_{i=1}^{n} x_i. \qquad (2)$$

Then, for $\mu_1 > \mu_0$,

if $\lambda' \le B'$, accept H_0;
if $\lambda' \ge A'$, reject H_0;
otherwise, take another sample.

The inequalities reverse if $\mu_0 > \mu_1$. The equations for A' and B' are

$$A' = \frac{\sigma^2 \ln(A)}{\mu_1 - \mu_0} + n\frac{\mu_0 + \mu_1}{2} \qquad (3)$$

$$B' = \frac{\sigma^2 \ln(B)}{\mu_1 - \mu_0} + n\frac{\mu_0 + \mu_1}{2}. \qquad (4)$$

Eq 2 shows that a sequential test of a Gaussian distribution doesn't require any multiplication or division; you simply add each new sample, x_i, to the running

Equations are key to sequential-test comprehension

In a hypothesis test **(Ref 1)**, you guess the value of a parameter, θ, and then perform tests until you collect sufficient evidence to see if the guess is right. The initial guess is the null hypothesis, H_0. The null hypothesis makes the statement that the value of θ is θ_0.

Part of the test process involves deciding how close to θ_0 your results must be to decide that H_0 is true. To make this decision, you must define an alternate hypothesis, H_1, against which to compare H_0. H_1 makes the statement that the value of θ is θ_1. After performing a test, you compare the test results with the two hypotheses and decide which hypothesis to accept.

Because you can't perform a perfect test, you can err in choosing one of the two hypotheses. If H_0 is true, but you decide that it's false, you commit a Type I error. The probability of producing a Type I error in a statistical test is α. If H_0 is false, but you decide it's true, you commit a Type II error. The probability of making a Type II error is β.

Deliberately bias results

Often you want to favor one type of error over the other type. For example, if you're testing an edible product for bacteria count, you want to make sure that you don't release tainted food—even though you may destroy some batches of good product. You can prevent the release of contaminated food by biasing your test to favor rejection.

To determine the value of a bias (the values of α and β), you may use risk analysis, game theory, or educated guessing. Once you set α and β, you must design your hypothesis test to obtain these values.

The likelihood-ratio test finds the acceptance criteria that will produce your desired values of α and β. To introduce a bias to a hypothesis test, you find a likelihood ratio λ_L that satisfies

$$\lambda_L = \frac{P(s|\theta_0)}{P(s|\theta_1)}, \tag{1}$$

where $P(s|\theta_0)$ is the conditional probability of measuring the data s if θ_0 is the true value of θ and $P(s|\theta_1)$ is the conditional probability of measuring s if θ_1 is true.

For each test,

$$\begin{gathered}\text{if } \lambda > k, \text{ accept } H_0;\\ \text{if } \lambda < k, \text{ reject } H_0;\\ \text{and if } \lambda = k, \text{ do either.}\end{gathered}$$

The value of k ($k>0$) determines the likelihood of choosing H_0. When you decrease k, you increase the likelihood of accepting H_0 (α decreases, β increases).

Once you set the bias of your test, you can tie the results of all trials into **Eq 1.** If the measured data consists of a set of independent results, x_1, x_2, . . . x_n, then $P(s|\theta_0)$ is $P(x_1 \text{ and } x_2 \text{ and } \ldots x_n|\theta_0)$ is the conditional probability of observing those n results if θ_0 is the true value of θ. If the results are independent,

$$\begin{aligned}P(s|\theta_0) &= P(x_1 \text{ and } x_2 \text{ and} \ldots x_n|\theta_0)\\ &= P(x_1|\theta_0)P(x_2|\theta_0)\ldots P(x_n|\theta_0).\end{aligned} \tag{2}$$

Substituting **Eq 2** into **Eq 1** gives

$$\lambda_L = \frac{P(x_1|\theta_0)P(x_2|\theta_0)\ldots P(x_n|\theta_0)}{P(x_1|\theta_1)P(x_2|\theta_1\ldots P(x_n|\theta_1)}. \tag{3}$$

Eq 3 is valid for discrete or continuous probability densities.

If a likelihood-ratio test includes hundreds of trials, it also has to include 2×hundreds of multiplication operations (to implement **Eq 3**). Although performing the multiplication is a time-consuming process, you can often simplify the likelihood ratio and avoid the multiplication by using the logarithm of the likelihood ratio as described in the main text.

Eq 3 is exact for a simple hypothesis such as $\theta=0.5$. For a composite hypothesis, such as $\theta_0<0.5$, you can't define the likelihood exactly.

Suppose you design a radar receiver for a bit-error probability P(e) that has a null hypothesis of $P(e)<10^{-5}$ and an alternate hypothesis of $P(e)>10^{-3}$. At every value of θ, α and β have different values. To find the likelihood ratio for this system, you simply choose values of θ_0 and θ_1. For example, you could choose $\theta_0=10^{-5}$ and $\theta_1=10^{-3}$.

At the chosen values of θ_0 and θ_1, you set α and β as if the hypotheses were simple. If the actual value of θ differs from either of the hypothesis values, it will have values of α and β that you can't control. You can compute the values and plot α and β over a wide range of θ, however. Even though you can control the test performance exactly only for simple hypotheses, you have the capability of knowing what the actual performance is at any point.

Reference

1. Cobb, R F, "Use statistics to test communications systems efficiently," *EDN*, January 8, 1987, pg 143.

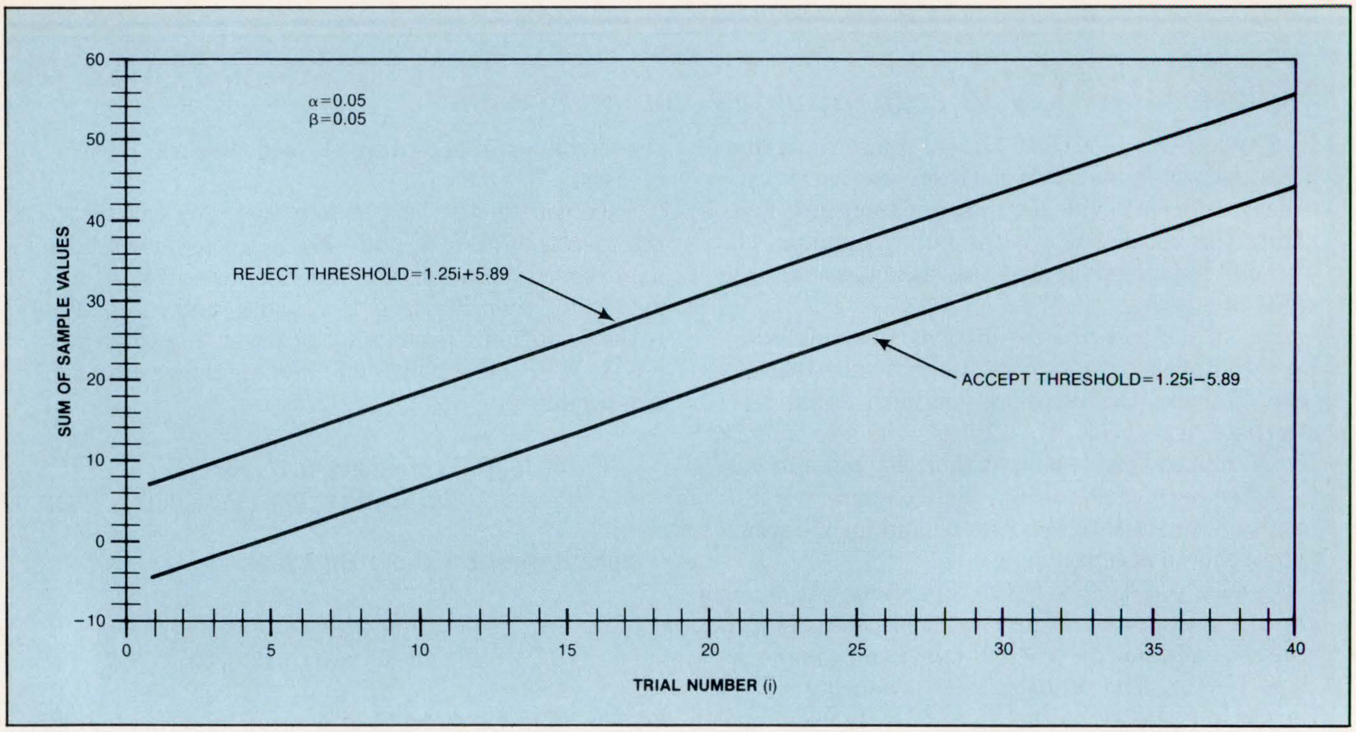

***Fig 1—The straight lines indicate the thresholds for testing** the null hypothesis, mean=1.0, vs the alternate hypothesis, mean=1.5, for a Gaussian random variable having a variance of 1.0. The unit under test passes by crossing the acceptance threshold at the 22nd trial.*

total. **Eqs 3** and **4** show that the thresholds (A′ and B′) aren't constants; they change linearly with the number of trials (n). Except for n, all the quantities in **Eqs 3** and **4** are fixed, so you can plot or tabulate A′ and B′ vs n before you begin your test. You can then compare λ' with the tabulated threshold values.

Eqs 3 and **4** show that the threshold values are parallel straight lines. Their slopes depend on the average value of the two hypothesized means. The distance between the parallel lines depends on the ratio of A to B (the difference between their logarithms) and the size of the difference in the hypothesized means.

Fig 1 plots the acceptance and rejection criteria as a function of the number of measurements for one set of parameters. As long as the running total remains between the lines, the test must continue. If the total rises above the upper line, you reject H_0; if it falls below the lower line, you accept H_0 (assuming $\mu_1>\mu_0$). You can confirm the plausibility of **Fig 1** by observing that if the difference between μ_1 and μ_0 is small, A′ and B′ are large. In this case, the threshold lines are far apart and you'll have to perform many measurements to reach a decision.

Try a binomial distribution of samples

The procedure for developing a sequential test for a binomial distribution is similar to the one for a Gaussian distribution. You can express the likelihood ratio as

$$\lambda' = \frac{{}_nC_xP_1{}^xq_1{}^{n-x}}{{}_nC_xP_0{}^xq_0{}^{n-x}},$$

where p_i is the probability of an event occurring during any one trial; $q_i=1-p_i$; x is the number of successes that have occurred; and ${}_nC_x=n!/[x!(n-x)!]$. **Ref 1** gives p_i for a binomial distribution.

After you cancel common factors and take the natural logarithm (to remove exponents), the equation becomes

$$\ln(A)\le x\ln(p_1)+(n-x)\ln(q_1)-x\ln(p_0)-(n-x)\ln q_0\le\ln(B), \quad \mathbf{(5)}$$

where ln(A) is the rejection threshold and ln(B) is the acceptance threshold. If you solve for the number of successes, x, as a function of the number of failures, w=n−x, you can express **Eq 5** as

$$\frac{\ln(A)-w\ln(q_1/q_0)}{\ln(p_1/p_0)}\le x\le\frac{\ln(B)-w\ln(q_1/q_0)}{\ln(p_1/p_0)},$$

when $p_1>p_0$. For a binomial distribution, the definition of the likelihood ratio becomes $\lambda'=x$. The rules of the sequential test are

if $\lambda'\le B'$, accept H_0;
if $\lambda'\ge A'$, reject H_0;

otherwise, take another sample.

This is true for

$$A'=\frac{\ln(A)-w\ln(q_1/q_0)}{\ln(p_1/p_0)} \quad \mathbf{(6)}$$

$$B'=\frac{\ln(B)-w\ln(q_1/q_0)}{\ln(p_1/p_0)}. \quad \mathbf{(7)}$$

If $p_1<p_0$, the inequalities reverse.

Although you must continue testing until the likelihood ratio falls outside of a certain range, all sequential tests end after a finite number of samples.

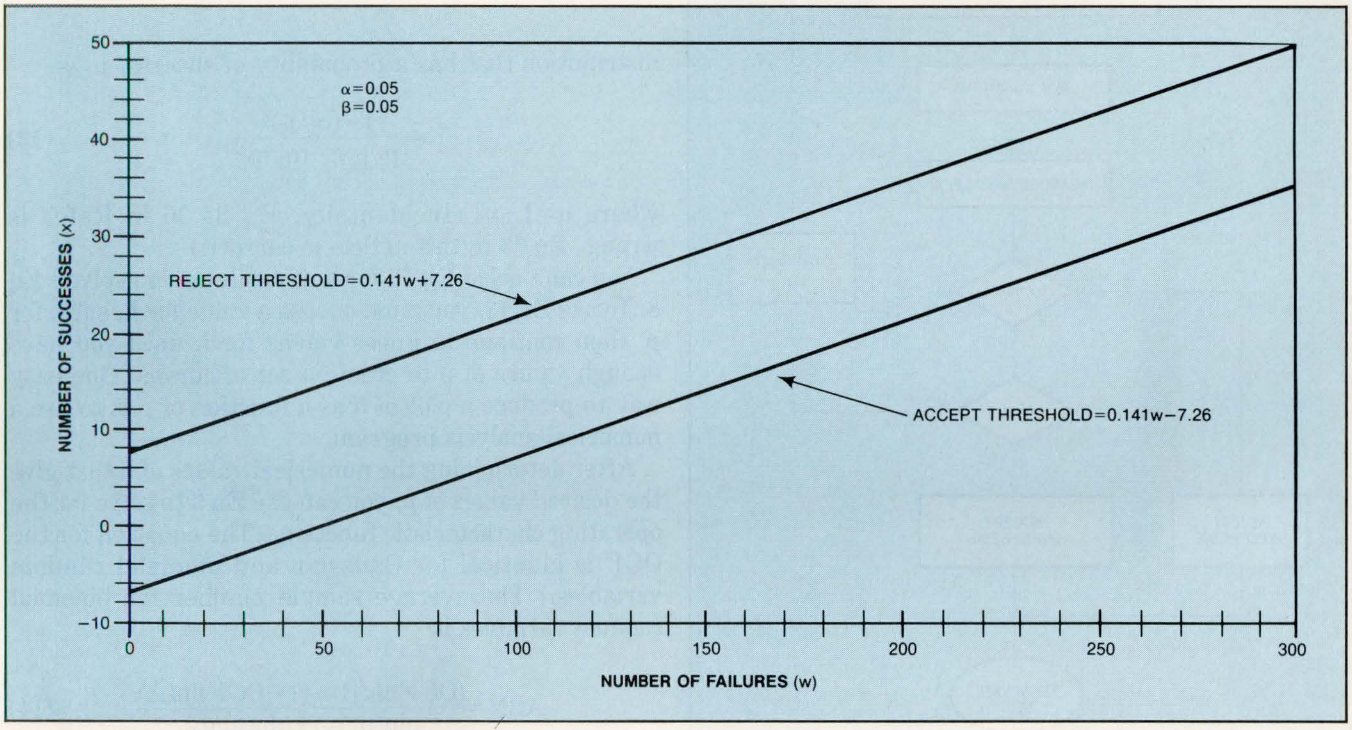

Fig 2—These parallel lines represent the thresholds for testing *a null hypothesis, $p_0=0.1$, vs an alternate hypothesis, $p_1=0.15$, for a binomial distribution. Because p is the probability of success, and $p_0<p_1$, units pass when the number of failures is large.*

Eqs 6 and **7** are of the form $c_i-(w\times k)$, where c_i and k are constants for any given set of test parameters. Therefore, just as for the Gaussian random variables, the sequential test for binomial random variables boils down to a simple set of operations.

To perform a sequential test on a binomial distribution, you plot (or tabulate) the number of successes, x, against the number of failures, w. Then you compare x against calculated values of A′ and B′ at each trial. **Fig 2** shows an example of this type of test.

Characterization may prove difficult

Although you may intuitively expect the sequential test to require fewer trials than a fixed-length test, you don't have to rely on your intuition. You can quantify the advantage of a sequential test over a fixed-length test by calculating the reliability of the sequential test.

The primary benchmarks that characterize a hypothesis test are its operating characteristic function (OCF) and its average sample number (ASN). The OCF is the probability of accepting H_0, plotted against values of the test quantity, θ. The ASN is the average number of samples that you must measure to reach a decision. Thus, the OCF gives the accuracy of the test; the ASN measures its efficiency. You can't calculate the ASN or the OCF exactly for a sequential test, but you can approximate these quantities **(Ref 3).**

To calculate the efficiency (ASN) of a sequential test for a Gaussian random variable, you start by defining a parameter h as

$$h=\frac{\mu_1+\mu_0-2\mu}{\mu_1-\mu_0}. \quad \textbf{(8)}$$

Then, express the OCF and the ASN as

$$OCF=\frac{A^h-1}{A^h-B^h} \quad \textbf{(9)}$$

$$ASN=\frac{(OCF)\ln(B)+(1-OCF)\ln(A)}{(\mu_1-\mu_0)\mu-(\mu_1^2-\mu_0^2)/2}. \quad \textbf{(10)}$$

When $\mu=\mu_0$, h=1; when $\mu=\mu_1$, h=−1. The ASN is close to its maximum value when h=0. Because usually you need to know how many trials you'll need in the worst case (of an average number of trials), you must determine the value of ASN when h=0. To solve **Eqs 9** and **10** for h=0, you use L'Hospital's rule:

$$\lim_{h\to 0}\frac{F(h)}{G(h)}=\frac{\frac{dF}{dh}}{\frac{dG}{dh}}.$$

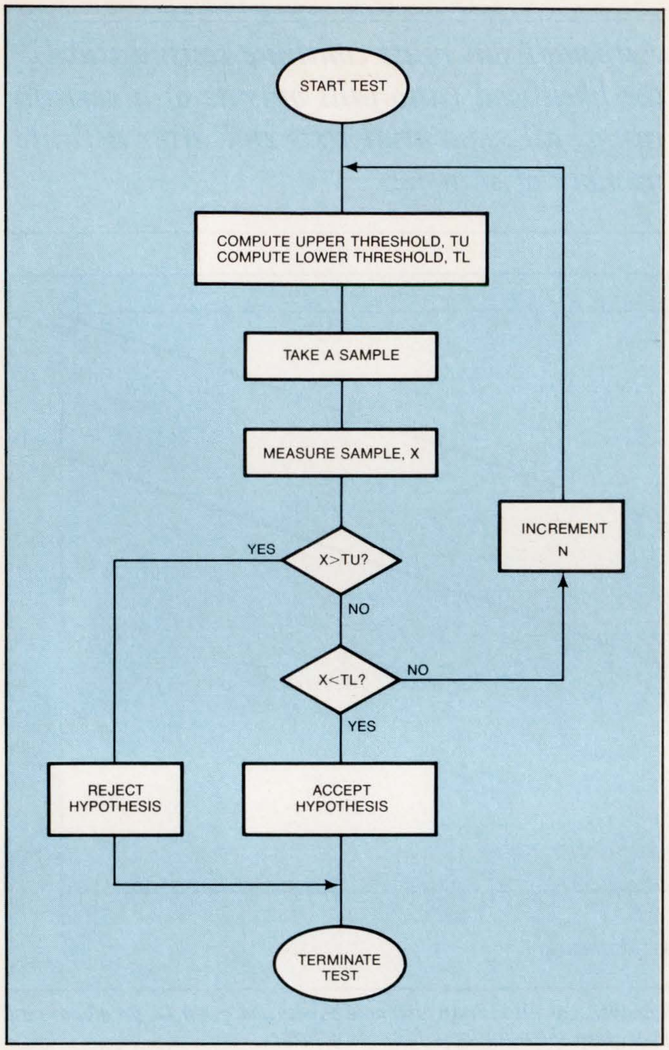

Fig 3—In this flow chart of a sequential hypothesis test, *a Monte-Carlo random-number generator produces the data. Depending on how you specify the acceptance criteria, you may need to interchange the acceptance and rejection blocks.*

To find the OCF when h=0, you use L'Hospital's rule once on **Eq 9**; to find the ASN, you must use the rule twice:

$$OCF(h=0)=\frac{\ln(A)}{\ln(A)-\ln(B)} \quad \textbf{(11)}$$

$$ASN(h=0)=\frac{\ln(A)\ln(B)}{(\mu_0-\mu_1)^2}. \quad \textbf{(12)}$$

Solving **Eq** 8 for μ when h=0 tells you the approximate value of μ that produces the largest value of ASN. It is the average value of the two hypothesis means, μ and μ_0. But note that the values given by these equations are approximate. Particularly when the ASN is small, a simulation can characterize a test better than an approximation.

To simulate a sequential test, you generate a set of random numbers and measure their OCF and ASN. You can implement a Monte-Carlo simulation of random numbers by using **Fig 3**'s flow chart.

The definition of the parameter, h, for a binomial distribution that has a probability of success, p, is

To analyze a sequential test's sensitivity to the probability of error, you must begin by calculating the values of the comparison thresholds.

$$p=\frac{1-(q_1/q_0)^h}{(p_1/p_0)^h-(q_1/q_0)^h}, \quad \textbf{(13)}$$

where q=1−p. (Incidentally, Eq 34.36 in **Ref** 3 is wrong. **Eq** 13 in this article is correct.)

You can't solve **Eq** 13 for h as easily as you solved **Eq** 8. To use **Eq** 13, you must choose a value for h, solve for p, then continue to guess values for h until you have enough values of p to create a set of curves. One easy way to produce a plot of h as a function of p is to use a numerical-analysis program.

After determining the numerical values of h that give the desired values of p, you can use **Eq 9** to solve for the operating characteristic function. (The equation for the OCF is identical for Gaussian and binomial random variables.) The average sample number for binomial random variables is

$$ASN=\frac{(OCF)\ln(B)+(1-OCF)\ln(A)}{p\ln(p_1/p_0)+q\ln(q_1/q_0)}. \quad \textbf{(14)}$$

To find the ASN when h=0, you must apply L'Hospital's rule three times:

$$ASN(h=0)=\frac{\ln(A)\ln(B)}{\ln(q_1/q_0)\ln(p_1/p_0)}. \quad \textbf{(15)}$$

An application for Gaussian variables

Now that you know how to design and characterize a sequential test, you can compare the sequential test to the fixed-length test (**Ref 1**). To perform a representative comparison, evaluate a sequential test of a Gaussian random variable that produces $\alpha=\beta=0.01$. Using **Eqs** 3 and 4,

$$\text{if } \lambda(i)<-2.298+1.5i, \text{ accept } H_0;$$
$$\text{if } \lambda(i)>2.298+1.5i, \text{ reject } H_0.$$

H_0 is the hypothesis that the mean is 1.4; H_1 is the hypothesis that the mean is 1.6; i is the sample number; and σ^2 is 1.0. Because $\alpha=\beta$, the thresholds at i=0 are symmetrical about zero.

Fig 4 shows this test's OCF. For this example, the approximation from **Eqs** 9 and 11 is quite good; the approximation agrees with the simulation. **Fig** 5 plots the ASN curve. The difference between the approximation and the simulation is greater than in **Fig** 4, but the percentage error is small.

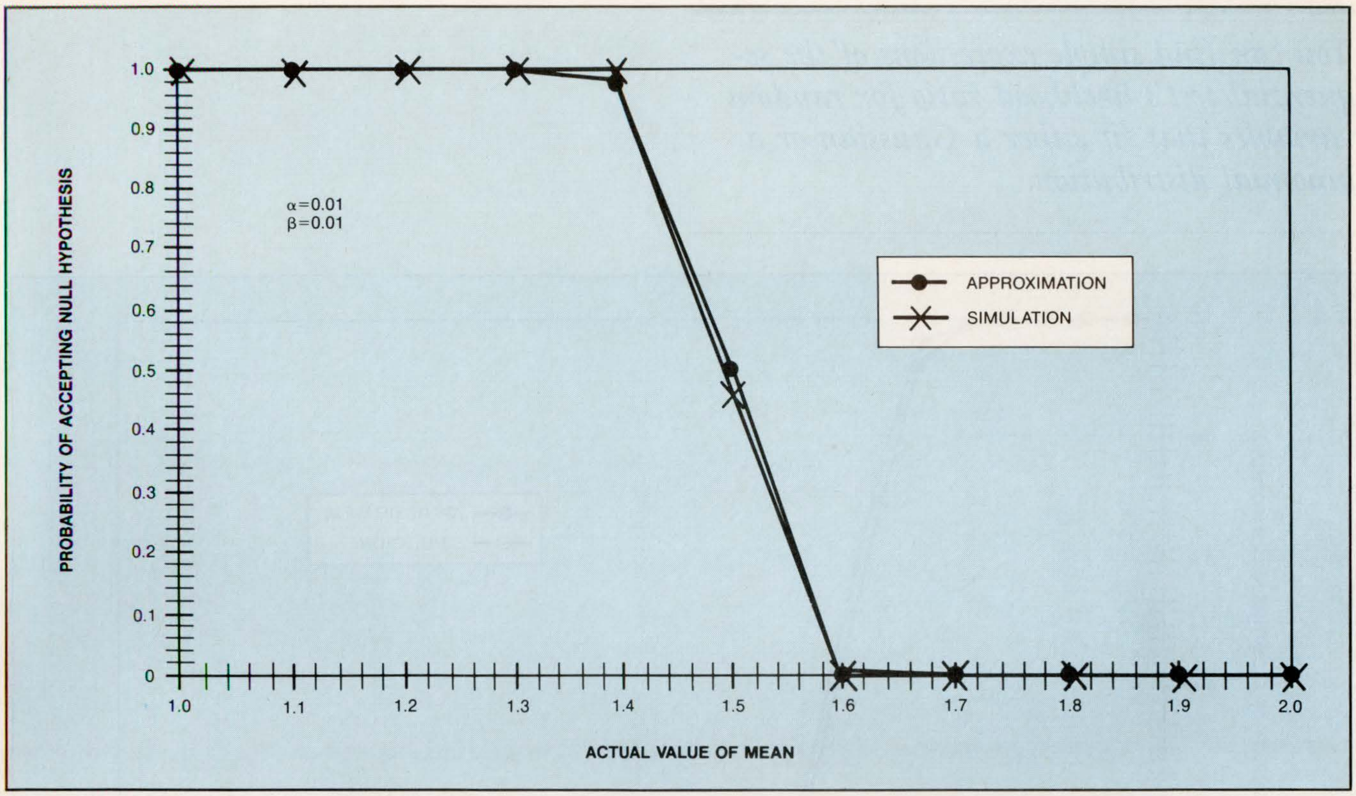

Fig 4—In this OCF plot of a sequential test *for a Gaussian random variable with a variance of 1.0, the test compares the null hypothesis, mean=1.4, and the alternate hypothesis, mean=1.6.*

As a general rule, the approximations become more accurate as the number of samples becomes larger. If you measure large numbers of samples when α and β are small, it appears that the approximations are more accurate for small values of α and β. The largest ASN in Fig 5 occurs midway between the two hypothesis values. The maximum point is at the exact midpoint because the two error values are equal, but the maximum ASN is always between H_0 and H_1.

For a fixed-length test that produces α=β=0.01, the

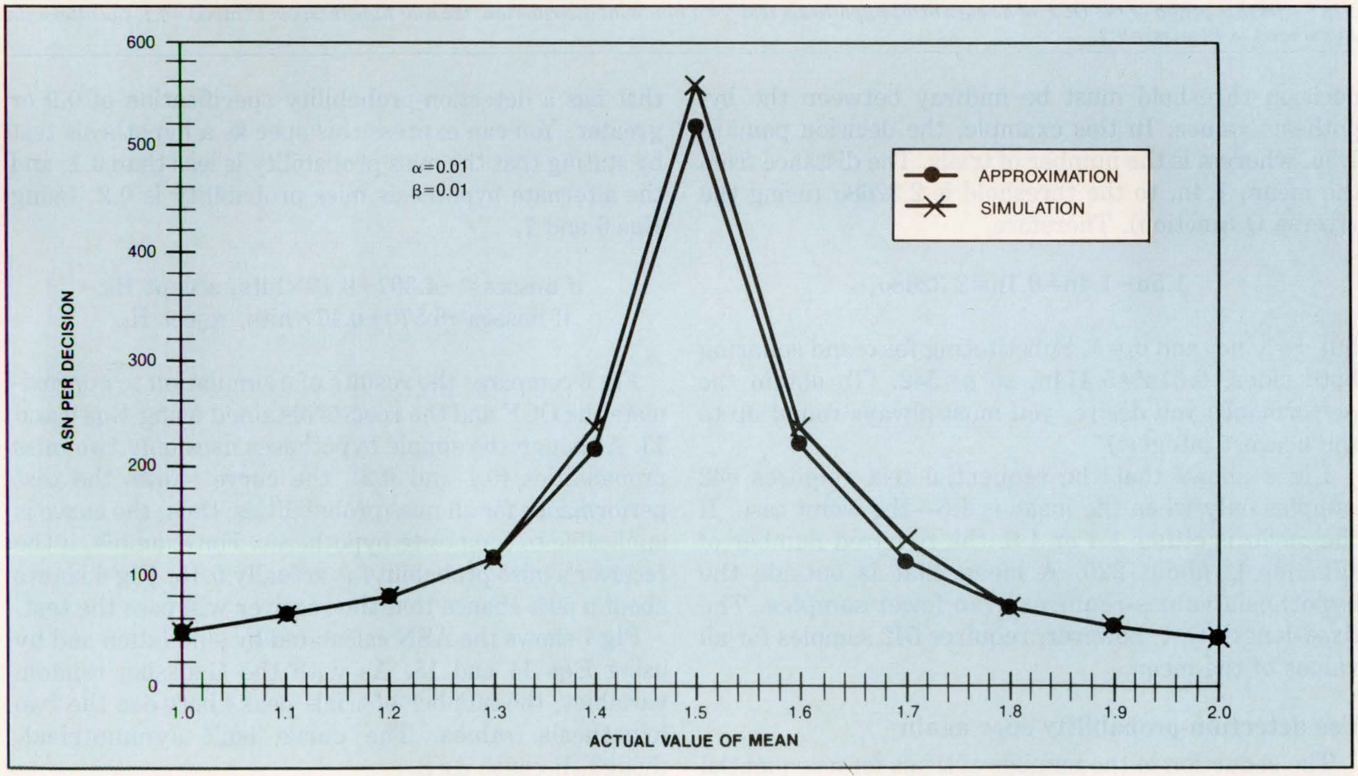

Fig 5—This figure plots the ASN curve *for the test performed in* ***Fig 4****. Because α=β, the curve is symmetric. The simulations always result in higher numbers of samples than the approximations.*

You can find simple expressions of the sequential test's likelihood ratio for random variables that fit either a Gaussian or a binomial distribution.

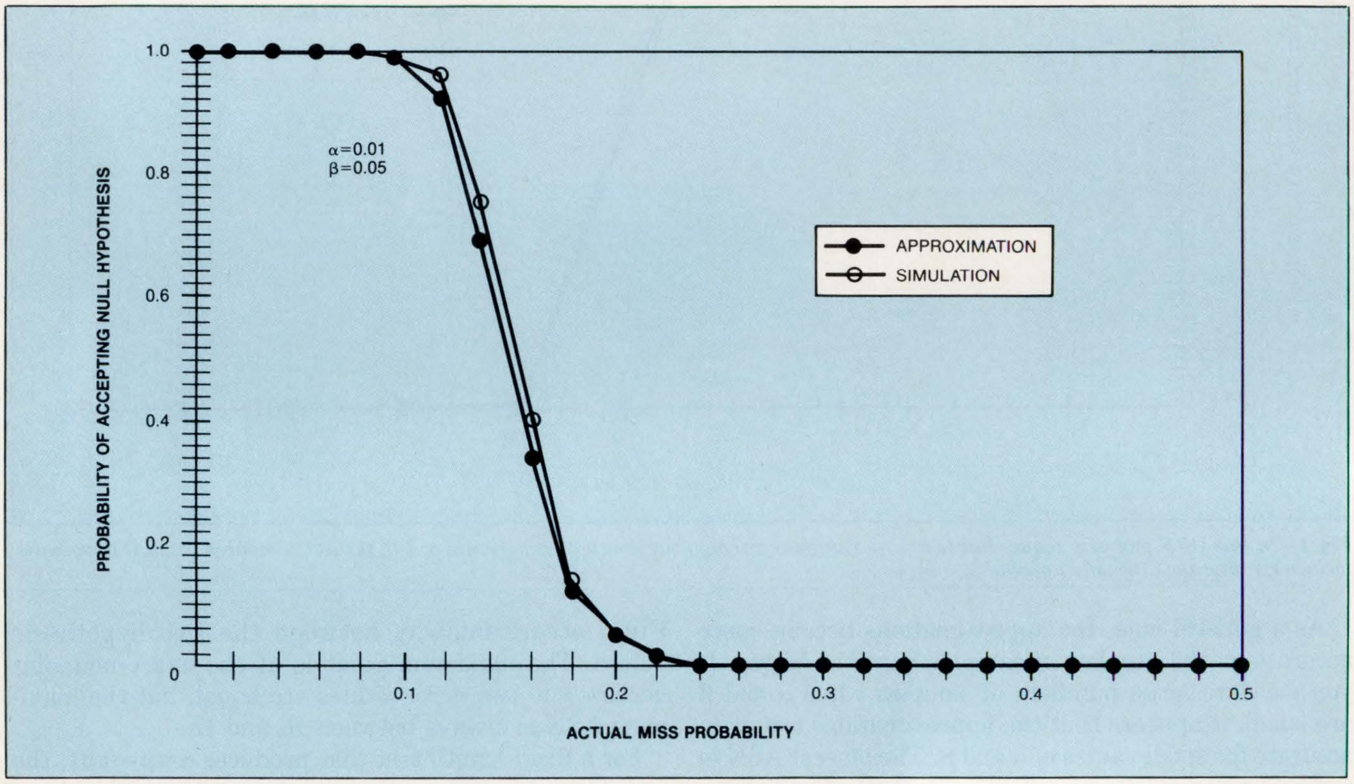

Fig 6—In this graph of the OCF of a sequential hypothesis test *for a binomial distribution, the null hypothesis is P(miss)=0.1; the alternate hypothesis is P(miss)=0.2.*

decision threshold must be midway between the hypothesis values. In this example, the decision point is 1.5n, where n is the number of trials. The distance from the mean, 1.4n, to the threshold is 2.3268σ (using the inverse Q function). Therefore,

$$1.5n-1.4n=0.1n=2.3268\sigma,$$

but $\sigma=\sqrt{n}\sigma_0$ and $\sigma_0=1$. Substituting for σ and squaring both sides, $0.01n^2=5.414n$, so n=542. (To obtain the performance you desire, you must always round up to the nearest integer.)

Fig 5 shows that the sequential test requires 542 samples only when the mean is 1.5—the worst case. If the mean is either 1.4 or 1.6, the required number of samples is about 220. A mean that is outside the hypothesis values requires even fewer samples. The fixed-length test, however, requires 542 samples for all values of the mean.

Use detection-probability spec again

The reduction in the number of trials for a sequential test of a binomial random variable is similar to that of a Gaussian variable. Consider the case of a radar receiver that has a detection-probability specification of 0.9 or greater. You can express this spec as a hypothesis test by stating that the miss probability is less than 0.1, and the alternate hypothesis miss probability is 0.2. Using **Eqs 6** and **7,**

$$\text{if misses} < -4.307+0.17\times\text{hits, accept } H_0;$$
$$\text{if misses} > 6.570+0.17\times\text{hits, reject } H_0.$$

Fig 6 compares the results of a simulation to approximate the OCF and the results obtained using **Eqs 9** and **13.** Although the simple hypotheses uses only two miss probabilities (0.1 and 0.2), the curve shows the test performance for all miss probabilities; thus, the curve is applicable to composite hypotheses. For example, if the receiver's miss probability is actually 0.15, **Fig 6** shows about a 50% chance that the receiver will pass the test.

Fig 7 shows the ASN calculated by simulation and by using **Eqs 14** and **15.** As with the Gaussian random variables, the number of trials peaks between the two hypothesis values. The curve isn't symmetrical, though, because $\alpha\neq\beta$.

To compare the sequential test to the fixed-length test with a large number of trials, you need the

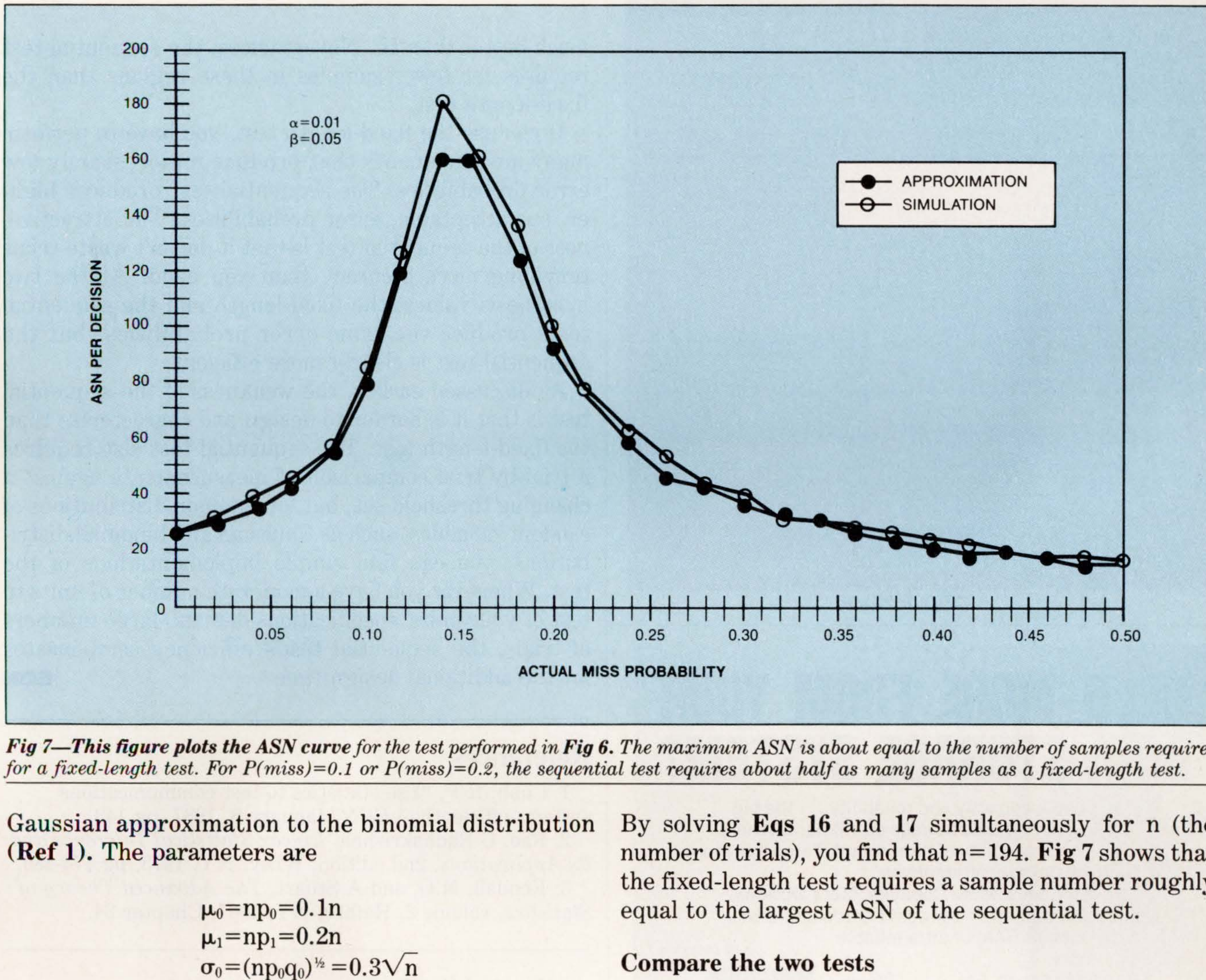

Fig 7—This figure plots the ASN curve *for the test performed in* ***Fig 6****. The maximum ASN is about equal to the number of samples required for a fixed-length test. For P(miss)=0.1 or P(miss)=0.2, the sequential test requires about half as many samples as a fixed-length test.*

Gaussian approximation to the binomial distribution **(Ref 1)**. The parameters are

$$\mu_0 = np_0 = 0.1n$$
$$\mu_1 = np_1 = 0.2n$$
$$\sigma_0 = (np_0q_0)^{1/2} = 0.3\sqrt{n}$$
$$\sigma_1 = (np_1q_1)^{1/2} = 0.4\sqrt{n}.$$

If the number of misses exceeds the threshold, t, the receiver fails the test. Using the Gaussian approximation, set

$$P(\text{exceeding the threshold}|p=0.1)=0.01$$
$$P(t \le x \le \infty) = Q\left(\frac{t-0.1n-0.5}{0.3\sqrt{n}}\right) = 0.01$$
$$t-0.1n-0.5 = 0.698\sqrt{n}, \qquad \textbf{(16)}$$

and

$$P(\text{falling below threshold}|p=0.2)=0.05$$
$$P(-\infty \le x \le t) = 1-Q\left(\frac{t-0.2n+0.5}{0.4\sqrt{n}}\right) = 0.05$$
$$t-0.2n+0.5 = -0.6224\sqrt{n}. \qquad \textbf{(17)}$$

By solving **Eqs 16** and **17** simultaneously for n (the number of trials), you find that n=194. **Fig 7** shows that the fixed-length test requires a sample number roughly equal to the largest ASN of the sequential test.

Compare the two tests

When your measurements aren't right at the peak in the ASN, the sequential test requires far fewer samples than the fixed-length test. For example, when the miss probability is 0.1, the sequential test requires less than half the number of trials of the fixed test. The maximum ASN equals the sample number for the fixed-length test simply because the sequential test knows when to quit. If testing involves a difficult decision, even the sequential test can require a large number of samples.

If you calculate the fixed-length test's OCF for true values other than the two hypothesis values, you'll see that the fixed-length test is more accurate than the sequential test over a large portion of the curve. The fixed-length test is more likely than the sequential test to fail a unit whose performance is much worse than H_0, and it is more likely to pass a unit whose performance is much better than H_0. Nevertheless, the sequential test requires far fewer samples in these regions than the fixed-length test.

If you use the fixed-length test, you have to perform many measurements that produce unnecessarily low error probabilities. The sequential test produces higher, but acceptable, error probabilities. The attractiveness of the sequential test is that it doesn't waste trials providing more accuracy than you need. At the two hypothesis values, the fixed-length and the sequential tests produce the same error probabilities, but the sequential test is clearly more efficient.

As discussed earlier, the weakness of the sequential test is that it is harder to design and characterize than the fixed-length test. The sequential test also requires a trial-by-trial comparison of measurements against a changing threshold set, but for common distributions of random variables, such as Gaussian and binomial distributions, you can find simple implementations of the test. Whenever you have a moderate number of units to test or your units' specifications demand large numbers of trials, the sequential test's efficiency compensates for the additional design time. **EDN**

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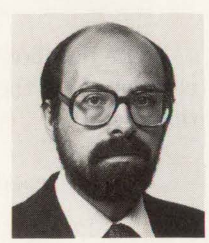
Author's biography



R F Cobb, a senior scientist at Harris Corp's Government Communications Systems Div (Melbourne, FL), specializes in the design of spread-spectrum modems for satellite communications. He received a BSEE from the University of Detroit and an MSEE from the Georgia Institute of Technology. Ray devotes his free time to teaching a neighborhood Bible study and to running.

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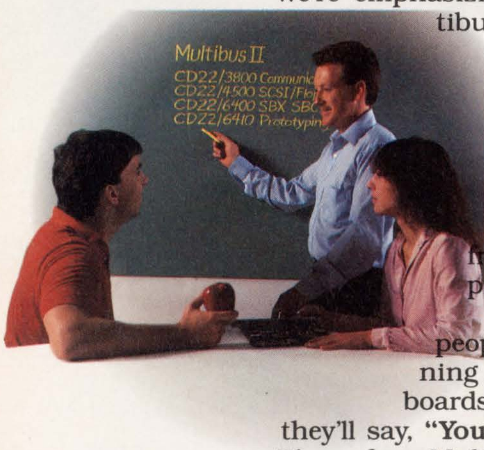

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Simplify FIR-filter design with a CMOS filter-control chip

Digital techniques let you define the phase and frequency characteristics of a high-speed filter more rigorously than you can with analog methods, but they require complex control circuitry. You can now implement this circuitry easily by using three CMOS chips to construct an FIR filter that has fully programmable characteristics.

Jeff D Haight, *Intersil Inc*

The design of digital filters used to be tedious, because it required either complex software or a great deal of hardware: multiple up/down counters, clock generators, data memory, and a μP or microprogrammed controller. By using VLSI components, however, you can now design a digital filter that uses only three CMOS chips and has fully programmable characteristics. Without enmeshing you in complexity, these chips let you design a medium- or high-speed filter that is stable, yields high performance, maintains linear phase response, and has zero drift over a wide temperature range.

Although designers have traditionally preferred analog techniques for designing filters that operate at audio or subaudio frequencies, all analog filters that use linear op amps suffer to some extent from drift caused by component aging, power-supply voltage changes, temperature changes, humidity changes, and component tolerances. These effects become more serious as you increase the filter's operating frequency or sharpen its roll-off characteristics. You can replace the linear amplifiers with charge-coupled or switched-capacitor devices, but the performance of filters using these devices can be limited by leakage of the charge on a capacitor (which can change the frequency response), by clock noise, and by the limited dynamic range of the devices.

Digital filters provide long-term stability

For demanding applications, therefore, the stability and programmability of digital filters makes them a better choice. The factors that determine the response of a digital filter are the coefficients, the clock or sample rate, and the number of taps, which determines the order of the filter. Digital filters provide long-term stability, because once you've programmed those parameters, only a hard failure (such as a change in one of the bits in a coefficient-storage PROM) can cause an undesired change in the filter's response.

You can choose from three basic types of digital filter for your design. Finite-impulse-response (FIR) filters are tolerant of reduced coefficient size and are always stable because they use only feedforward signal paths. They may require a large number of taps, however. Infinite-impulse-response (IIR) filters can yield the same response with fewer taps, because they include feedback paths as well as feedforward paths. However, because of the feedback, they may introduce more phase distortion and may be more difficult to stabilize than FIR filters. The third type, the lattice filter, can yield better results in some applications than either the FIR or the IIR types can, but it's much more difficult to design.

To choose a filter type, you can use a PC-based

The factors that determine a digital filter's response are the coefficients, the clock or sample rate, and the number of taps.

simulator that lets you tweak any filter parameters as a function of the various tradeoffs—S/N ratio, amplitude of passband ripple, stopband rejection, cost, and other factors. In digital-filter design, as in analog design, experience and rules of thumb will give you a good idea of what hardware you'll need in order to meet system requirements, but a simulator will let you see exactly how changes in filter type, filter length, coefficients, and other factors will affect filter performance.

You can design an FIR filter easily with two VLSI CMOS chips (from Intersil): the IM29C128 FIR filter controller (FFC), which contains all the required timing, addressing, data-history memory, and control circuitry, and the IM29C510 multiplier-accumulator (MAC), which performs the filtering. In addition, you'll need a RAM or PROM for coefficient storage. **Fig 1** shows the internal structure of the FFC; **Fig 2** shows how to interconnect the FFC, MAC, and PROM or RAM to construct a single-stage FIR filter with as many as 128 taps. **Fig 3** shows the timing requirements.

When you're performing your initial calculations, remember that typical filter operations require approximately 80 nsec per tap. Thus, when you take into account the setup and hold times of typical external circuitry, your coefficient storage will need to have an access time of 65 nsec or less. On the other hand, if the processing on each data point takes less than 80 nsec, you can slow the filter clock and use slower storage devices.

From the above figures you can easily calculate the

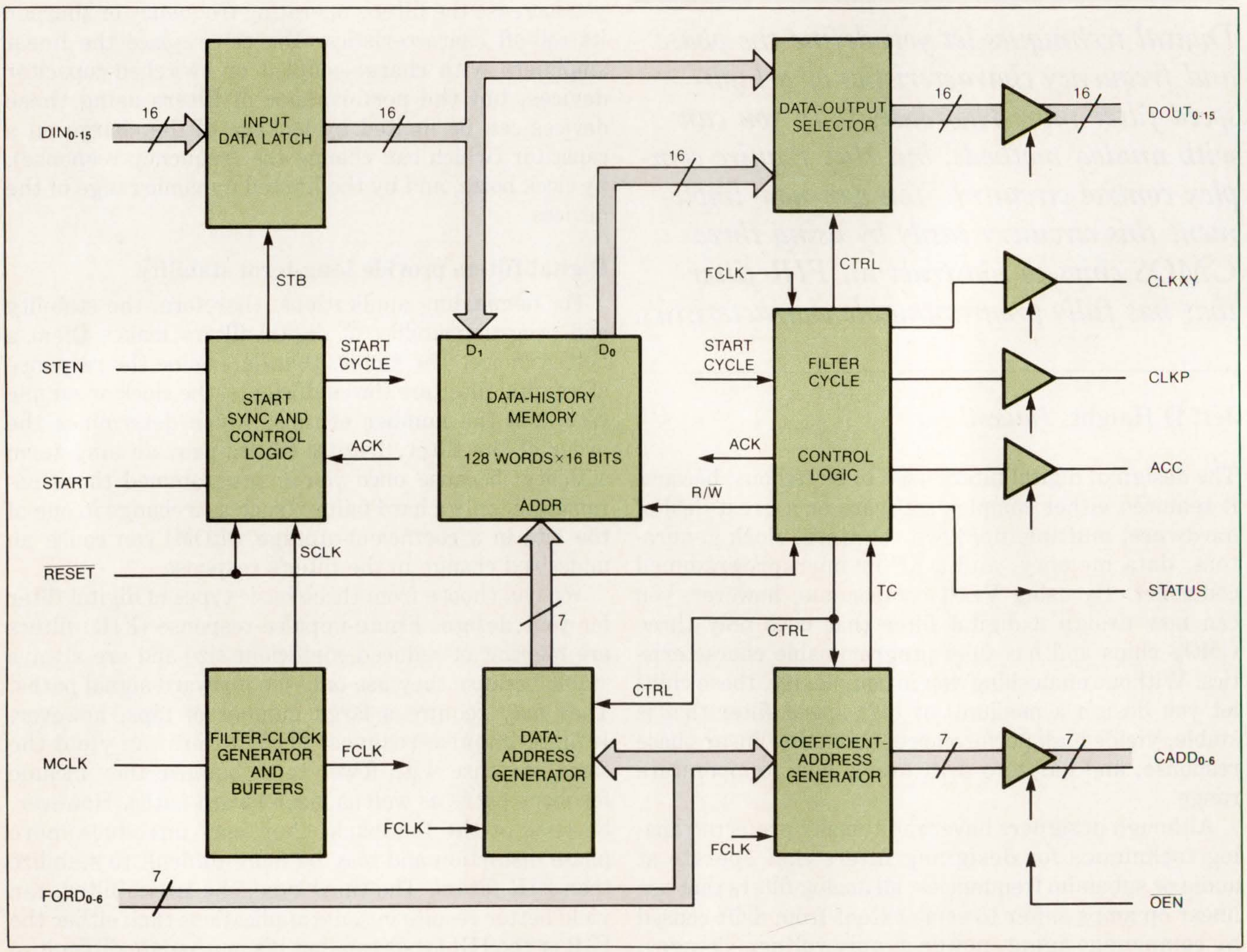


***Fig 1—This VLSI chip, the FFC, contains all the memory,** timing, and control circuits needed to control a multiplier-accumulator (MAC) and a coefficient-storage PROM. Using only these three chips, you can build a 128-tap FIR filter that has programmable characteristics.*

bandwidth that a single filter stage can handle. For example, if your simulations show that you'll need 100 taps to achieve the response you want, then each data point requires 100×80 nsec, or 8 μsec; that is, the filter can accept data at 1,000,000/8 data points per second, or 125 kHz. However, the Nyquist criterion states that, to avoid aliasing, sampling must take place at more than twice the maximum data frequency. Therefore, your filter will handle a bandwidth of 62.5 kHz.

You'll find that the number of taps you need in the filter depends entirely on the application. Some types of video processing (such as edge detection) may need as few as 10 taps. On the other hand, some types of notch filters may require several hundred taps, or, in extreme cases, several thousand.

If you need more than 128 taps, you'll have to cascade two or more stages. The total throughput depends on the number of multiplications and additions that the circuit must perform per second. If you double the number of stages, each of which contains its own MAC, you almost double the number of sum-of-products oper-

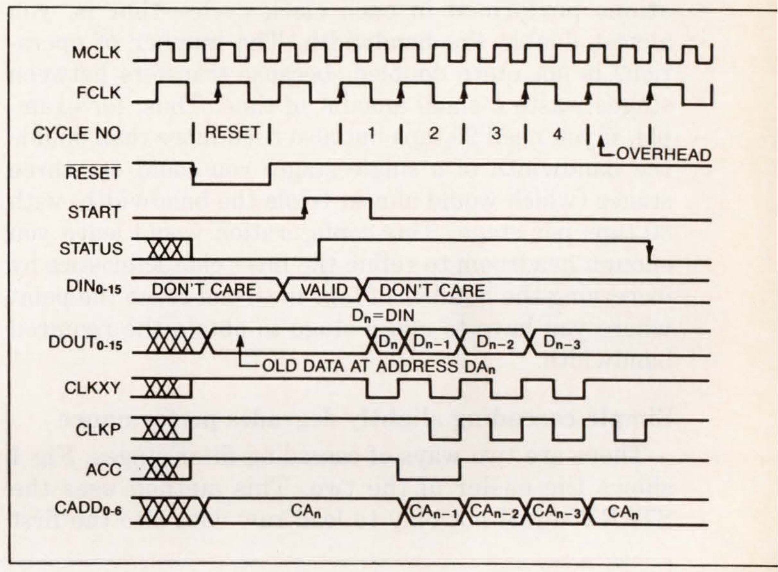


Fig 3—A filtering cycle starts on the rising edge of the START signal. *The FFC derives all timing and control signals from the externally supplied MCLK clock pulse, which must have twice the frequency of the internal CLKP filter clock.*

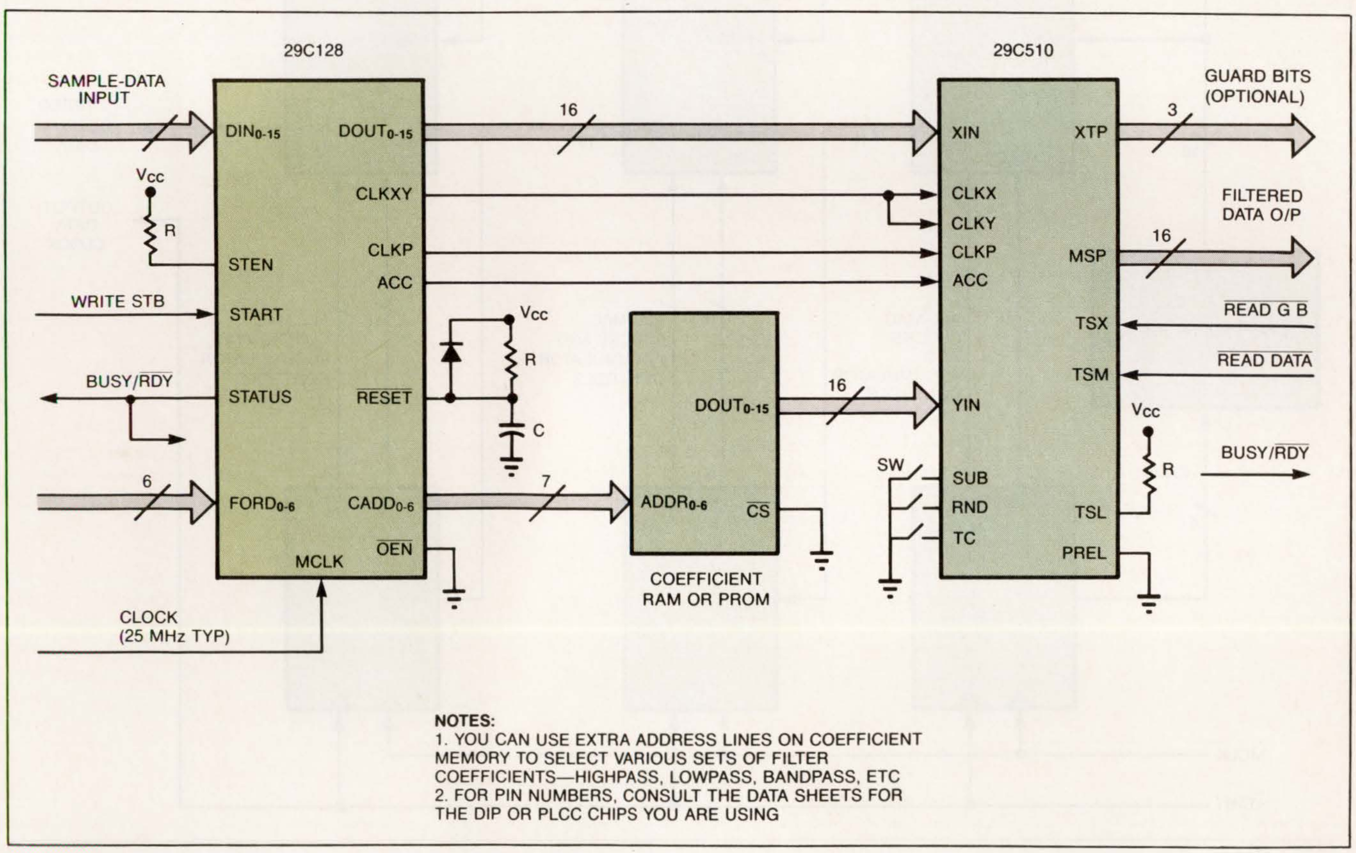


Fig 2—It's simple to connect the FFC to a 16-bit MAC. *The FFC also provides six address lines for accessing coefficients stored in PROM or RAM.*

Simple cascading may produce more ripple in the passband than an optimally designed filter would, but you can compensate for it by specifying less ripple initially.

ations performed in each clock cycle—that is, you almost double the bandwidth. The number of operations is not quite doubled, because transfers between stages waste a small amount of time. Thus, for example, if you need 90 taps but also need more than double the bandwidth of a single stage, you could use three stages (which would almost triple the bandwidth) with 30 taps per stage. This configuration would leave you enough headroom to refine the filter characteristics by increasing the number of taps until you reach the point where you have to add a stage to obtain the required bandwidth.

Simple cascading slightly degrades performance

There are two ways of cascading filter stages; **Fig 4** shows the easier of the two. This method uses the START signal not only to load raw data into the first FFC, but also to load partially filtered data present on the MSP and XTP output lines of that FFC into the following FFC. The method imposes a slight performance penalty, for the following reasons. Consider a filter that requires 205 taps configured as five stages with 41 taps each. At the output of any given stage, each data point has a history of 41 different points times 41 different coefficients, and these partially filtered and summed data points enter the next stage for further multiplication and summation. The result is not mathematically the same as that of an optimally designed 205-tap filter, in which each output would be the result of 205 different input data points multiplied by 205 different coefficients.

In practice, however, the difference may not be significant, because convolution is a linear operation: If you put a 20-dB notch in the signal in one stage, and

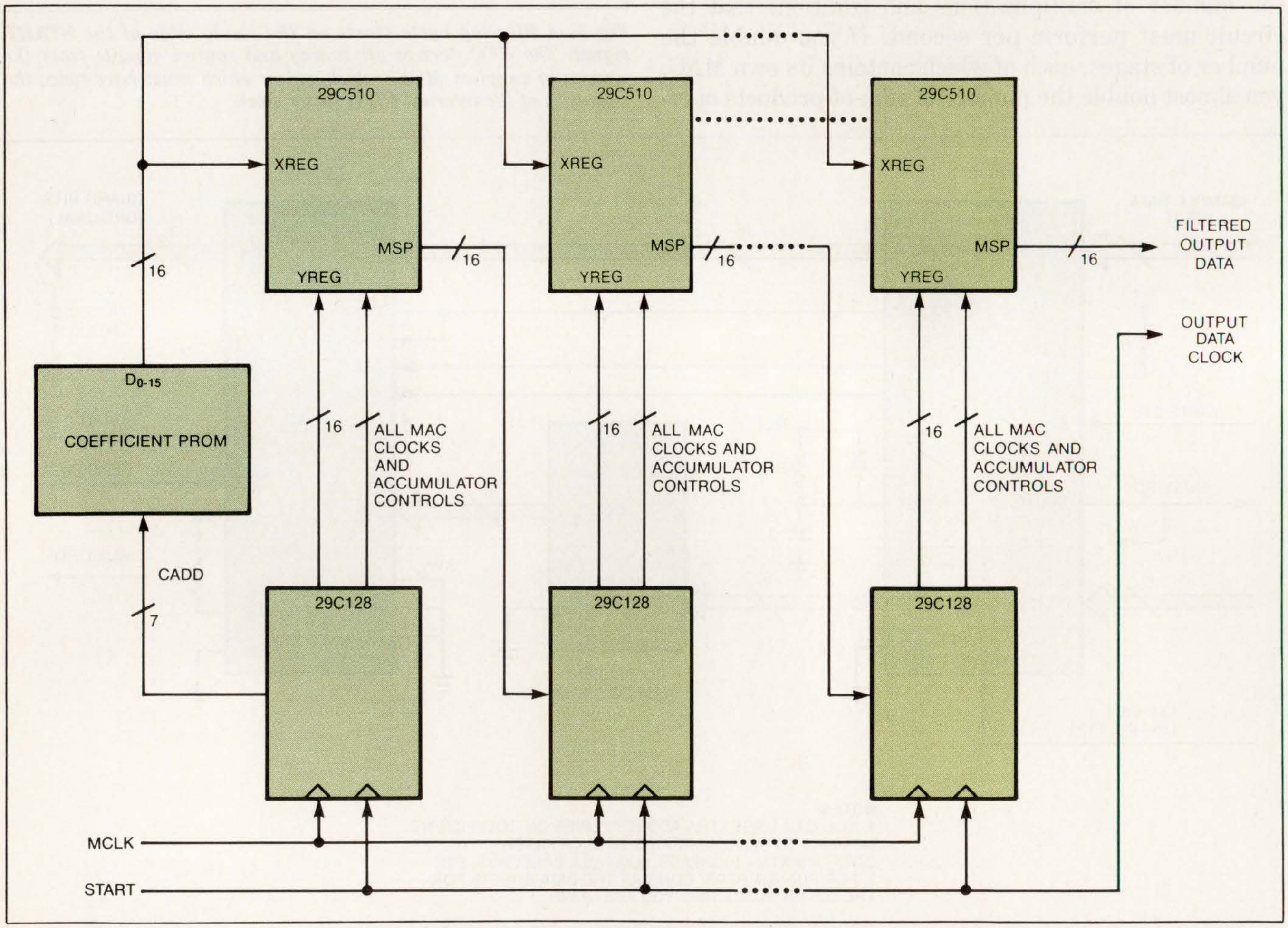


Fig 4—If you need more than 128 taps in your filter, *you can cascade several filter stages, each consisting of an FFC and a MAC. The coefficient-storage chips can be common to all stages.*

then feed the output of that stage into an identical second stage, the result will be a 40-dB notch. Additional stages will each deepen the notch by 20 dB. This characteristic makes it easy for you to design a filter by performing simple cascading. You simply divide the desired frequency characteristic (in dB) by the number of stages, calculate the coefficients and the number of taps needed for one stage, and cascade the required number of identical stages. Because you'll be using the same coefficients for each stage, you can simplify the hardware by using a single set of PROM or RAM coefficient-storage chips to serve all the MACs in the filter, regardless of the number of stages.

Other performance-degrading factors

You may have to consider some other factors that make the filter performance obtained from simple cascading less than optimal. For example, the Remez exchange algorithm (or any algorithm that uses Chebyshev or other polynomials in an iterative optimization technique) calculates the optimal set of coefficients for a given number of taps. Reducing the number of taps, or, more accurately, reducing the number of distinct coefficients, somewhat degrades filter performance. You can compensate for this degradation by specifying a tighter response and adding a few taps to obtain it.

Further, simple cascading may produce more ripple in the passband than an optimally designed filter would. However, you can compensate for the excess ripple by specifying less ripple in your initial calculations. Simple cascading may also cause a slight deterioration in the noise floor. In a single stage, arithmetic operations take place with full 16×16-bit-precision summing and 35-bit accumulation. When you employ simple cascading, however, the summed least-significant products in bits 15 through 0 of a 16-bit MAC are not passed to the next stage, so you'll observe truncation or round-off errors. These errors are relatively insignificant, except in very long filters that must satisfy very demanding requirements.

The second method of cascading filter stages **(Fig 5)** maintains full precision and full data history but re-

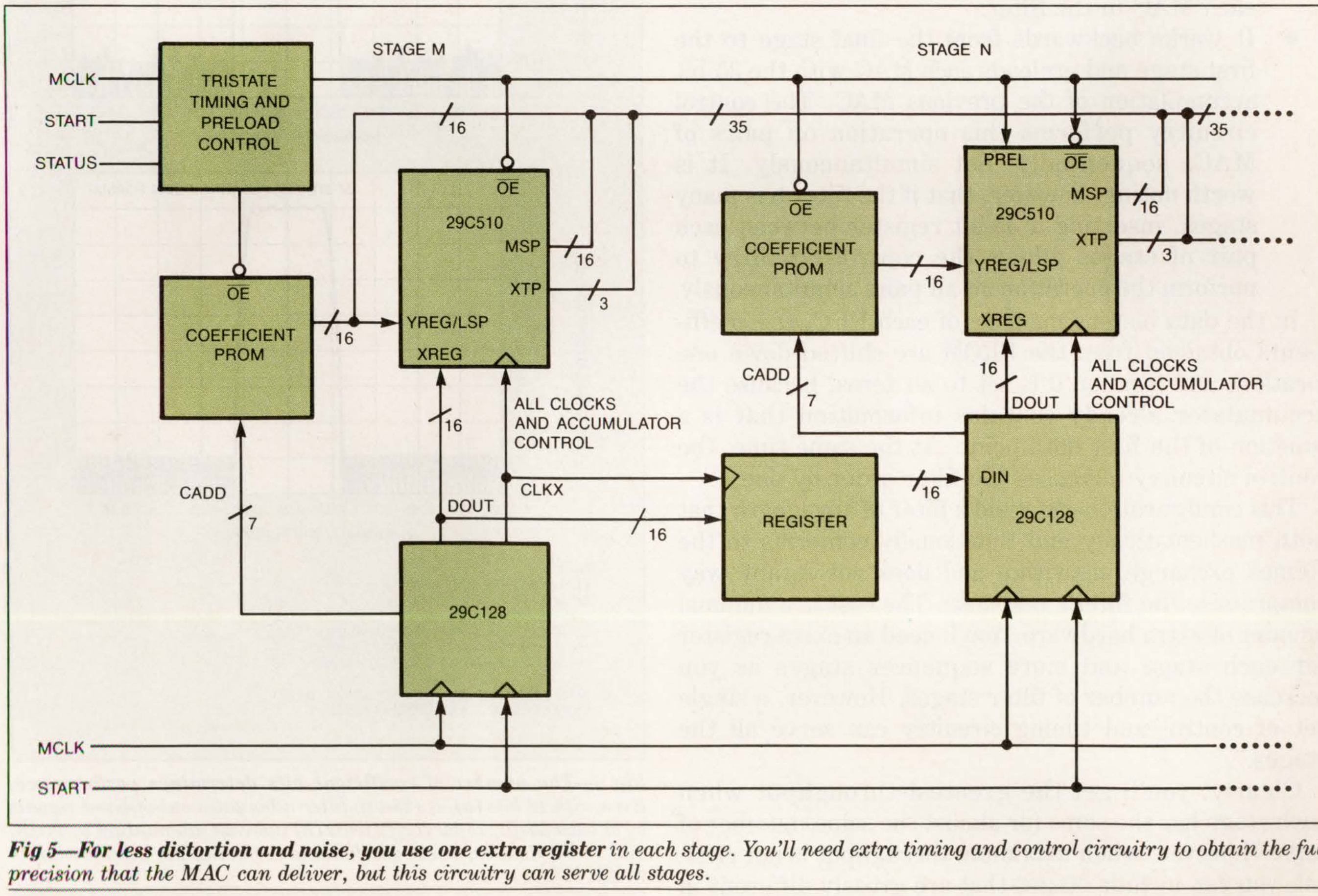


*Fig 5—**For less distortion and noise, you use one extra register** in each stage. You'll need extra timing and control circuitry to obtain the full precision that the MAC can deliver, but this circuitry can serve all stages.*

Cascading with extra registers maintains full precision and full data history, but requires some extra hardware for data storage and control-signal generation.

quires some extra hardware for data storage and control-signal generation. This method requires the addition of a register connected in parallel with the X register of each MAC. The rising edge of each CLKXY pulse loads the same data point into both the X register of the stage *M* MAC and the additional register; the output of the extra register is connected to the data-input port of the following stage-*N* FFC. At the beginning of each cycle (that is, for each new data point), the control circuitry clears the registers of the first-stage MAC.

The sequence of the filter's operations is as follows. When the START signal loads new data into the stage-*M* FFC, it also loads the previous data point into the initial position of the stage-*N* FFC's data memory. The falling edge of the FFC's status flag starts a control sequence that performs the following steps:

- It latches the output of the final filter stage into the next section of circuitry for display or other processing.
- It disables the MSP, LSP, and XTP outputs of each MAC in the filter.
- It works backwards from the final stage to the first stage and preloads each MAC with the 35-bit accumulation of the previous MAC. The control circuitry performs this operation on pairs of MACs sequentially, not simultaneously. It is worth noting, however, that if the filter has many stages, inserting a 35-bit register between each pair of stages allows the control circuitry to perform the operation on all pairs simultaneously.

In the data-history memory of each FFC, the coefficients obtained from the PROM are shifted down one location, and location 0 is set to all zeros, because the accumulator already contains information that is a function of the first data point. At the same time, the control circuitry increases the filter order by one.

This configuration can yield a filter of any length that both mathematically and functionally conforms to the Remez exchange algorithm and does not in any way compromise the filter's response. The cost is a minimal amount of extra hardware. You'll need an extra register for each stage and more sequencer stages as you increase the number of filter stages. However, a single set of control and timing circuitry can serve all the stages.

Clearly, you'll get the greatest throughput when each stage has the same (or almost the same) number of taps. However, when maximum throughput is not critical, you can include stages that are grossly different in

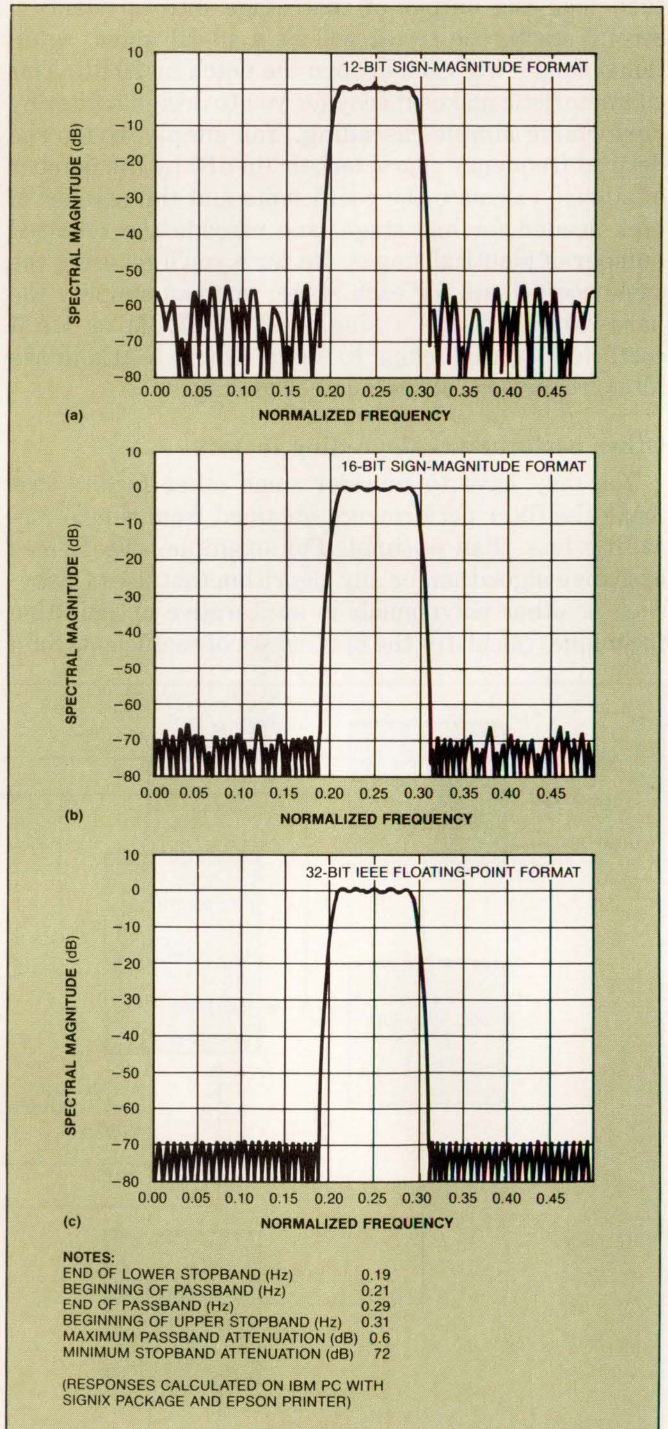


Fig 6—The number of coefficient bits determines performance. *Even with 12 bits **(a)**, a 128-tap filter attenuates out-of-band signals by at least 50 dB; 16-bit coefficients **(b)** increase attenuation to 65 dB; and 32-bit floating-point coefficients **(c)** bring the attenuation to 70 dB.*

length. You could, for instance, implement a lowpass filter in the first section and a bandpass filter in the second. This might simplify the implementation of adaptive algorithms, for example, in which only the bandpass portion varies.

MAC resolution affects performance

One advantage of the 29C128 FFC is that it can work with MACs of widely differing resolution. Although the price of MACs has dropped so much that 16-bit devices are economical for most applications, you may have to use MACs of a different size for filters with demanding requirements.

Further, you'll have noted from the discussion on cascading stages that simple cascading produces more ripple and noise than does the more complex cascading with registers. It's important to remember that the round-off and truncation noise are uniformly distributed, regardless of whether the source is data truncation, coefficient truncation, or truncation of the products that are summed. Further, a change in the coefficient size affects the filter response in exactly the same way, whether the data width is four bits or 400 bits. Thus, in very demanding applications, it may be desirable to use 16-bit, 24-bit, or floating-point MACs, even when the data width is only eight bits.

Fig 6 shows the different filter responses that you can achieve from a 127-tap bandpass filter according to whether you use the 12-bit fixed-point format **(Fig 6a)**; the 16-bit fixed-point format **(Fig 6b)**; or the 32-bit floating-point format **(Fig 6c)** for the coefficients. You can see from **Fig 6** that a filter of this length doesn't show much increase in performance when the coefficient word size goes from 16 to 32 bits. Even when you use 12-bit coefficients, out-of-band signals are reduced by more than 50 dB, which is adequate for most telecommunications applications.

For filters with very few taps, or for noncritical filters, you could use 8-bit MACs. Many image-processing operations consist of 1- or 2-dimensional FIR filtering that requires only a few taps and for which 8-bit resolution is sufficient. For many speech-processing operations, you'll need 12-bit resolution, however. The FFC lets you easily tailor the filter parameters to take advantage of the tradeoffs between resolution and number of taps.

You can change filter response dynamically

Other applications that benefit from the ability to vary filter parameters dynamically include adaptive filtering for modems, radar-signal processing, and multichannel applications such as ultrasound medical imaging and sonar systems. High-speed modems need to vary filter response dynamically to maximize, or at least improve, the S/N ratio as channels fade or multipath distortion varies. Most of the work requires the modem to vary the response of a fixed-length filter; however, the structure of the FFC makes it easy to vary filter length as well. In radar-signal processing, the same filter can encode biphase transmitted pulses and also compress the pulses of long, weak received sequences. For the processing of A/D radar outputs, 12-bit coefficients are usually adequate. For further processing, however, you'd need coefficients having 16 or more bits. In telecommunications applications, where very poor S/N ratio is the norm, you might

Filter board plugs into PC

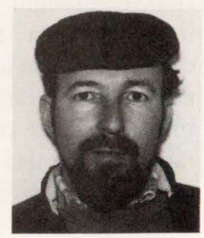
To simplify FIR-filter design and allow sophisticated data conversion without investing a lot of design time, you can use a plug-in filter board that occupies one slot in an IBM PC or compatible computer. The board, Intersil's EVK-128, provides an ICL7115 14-bit A/D converter, an ICL7121 16-bit D/A converter, an IM29C128 FFC, an IM29C510 16-bit CMOS MAC, and control and interface circuitry. It comes with a floppy disk containing programs for filter design. The programs include routines that let you calculate filter coefficients and plot filter response. Once you've calculated the coefficients, you can download them to RAM storage on the board so the filter system can use them.

The board also includes a digital uniform-noise generator that lets you perform further verification of your design. The documentation includes complete schematics, a parts list, and pc-board artwork, from which you can copy the items you need for your own filtering system. If you wish to use purely digital I/O, you can bypass either the A/D or the D/A converter or both: You can access the filter system directly, either via the PC bus or by means of edge-mounted connectors that are externally accessible. This arrangement allows you to process data off line, using floppy-disk storage for the intermediate results of repeated passes through the filter.

employ very long character codes that have very low cross-correlation values. In such applications, the coefficients wouldn't need to have more than eight bits.

If intermediate storage is available, you could achieve more than 128 taps in a single stage by storing the partially filtered data on disk and cycling it through the same filter stage several times. For example, you might have several hundred kilobytes of physiological data that you know has been contaminated by 60- or 120-Hz components radiated from fluorescent lighting. You could eliminate the noise by passing the data through a digital filter with 1000 taps, yielding extremely sharp notches at 60 and 120 Hz. Where software filtering is too slow, you could speed up the processing by three orders of magnitude by cycling the data through one 128-tap filter stage. To perform this and other types of filtering, you can use a special plug-in board for the IBM PC (see **box,** "Filter board plugs into PC"). **EDN**

Author's biography



Jeff Haight was product marketing manager for DSP products at GE Intersil (Cupertino, CA) when he wrote this article. He's now vice president of sales and marketing at Micro Integration Corp (San Jose, CA). Jeff holds a BA from the University of Washington; he also attended Caltech. He's a member of the Old Crows (an electronic warfare society) and SPIE, and his leisure pursuits include music, tennis, bicycling, reading, and skiing.

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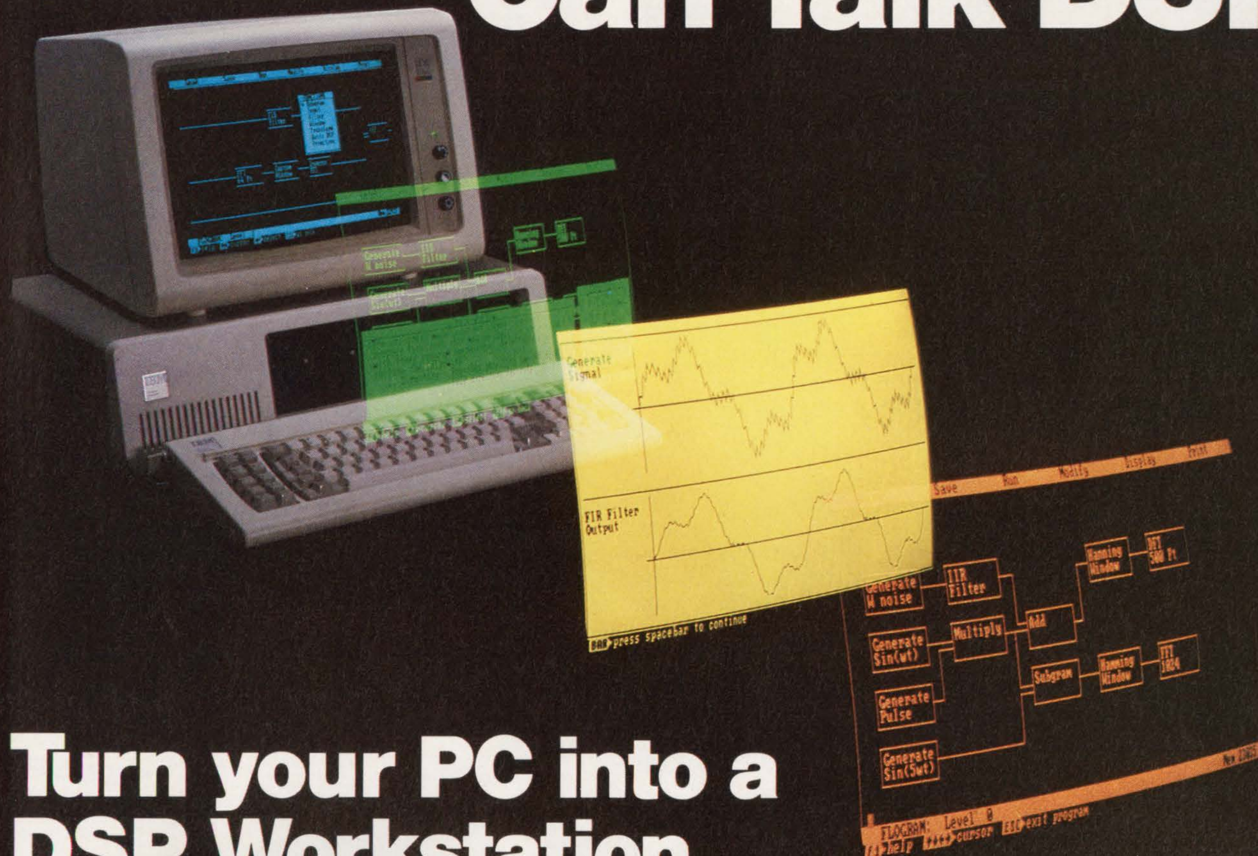

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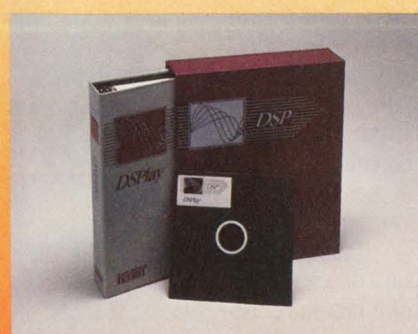

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Proper design tradeoffs translate to a precise position-control system

Microstepping technology offers a means of improving resolution in position-control applications. When it comes to a drive/control scheme, however, you must juggle a number of design tradeoffs if you hope to achieve an optimum design.

Yoram Hirsch, *IXYS Corp*

Designers of drive and control systems for microstepping motors in positioning applications have to take into account several considerations: matching and accuracy requirements for microstepping control; H-bridge power-stage operating modes; the impact of the PWM switching frequency on system operation; single-supply operation; sign/magnitude-vs-bipolar inputs; undervoltage, overcurrent, and overtemperature protection; and advanced adaptive-compensation schemes.

Although stepping motors have advantages when compared with servo motors, they aren't problem-free. A stepping motor's large pulse-drive waveforms create mechanical forces that excite and aggravate the mechanical resonances in the positioning system. These resonances are load dependent and difficult to control because stepping motors have very little inherent damping capability. At resonance, a stepping-motor system is likely to lose synchronization and skip or gain a step. In an open-loop system (typical in stepper-motor applications), this loss of synchronization implies loss of position information—obviously an unacceptable situation. Commonly, system designers circumvent this problem by avoiding the band of resonance frequencies, but this solution severely limits system performance.

Stepping motors also suffer from the disadvantage of limited resolution. Most steppers have resolutions of 200 steps/revolution (1.8° per step). The highest resolu-

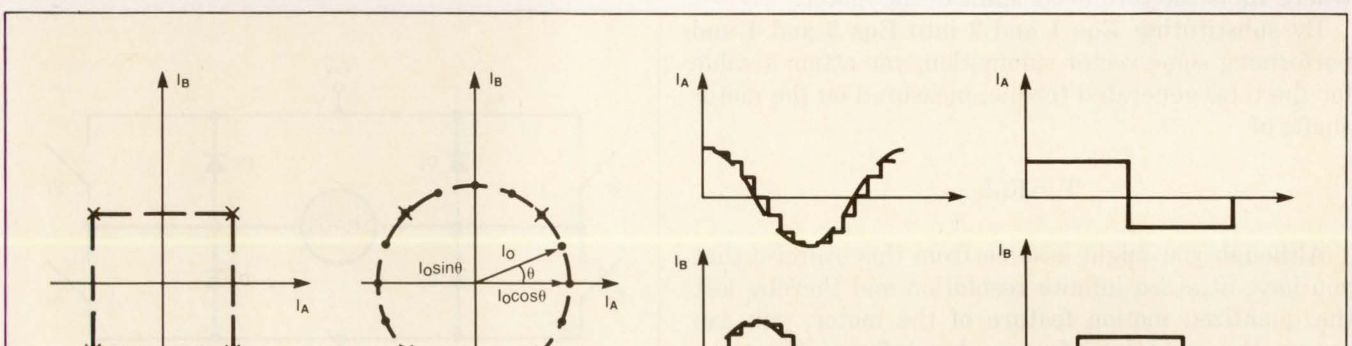


Fig 1—You can subdivide each full step into a number of microsteps *by driving a motor with the intermediate current levels at which the vector sum tracks the circle.*

tion motors spec 400 steps/revolution (0.9° per step).

Microstepping technology allows you to overcome these disadvantages while still retaining an open-loop system's advantages. Microstepping divides each normal step into smaller steps by applying currents to both phases of the motor, creating a torque phasor that's proportional to the vector sum of both currents. When this phasor completes one turn (360 electrical degrees), the motor moves exactly four full steps (one torque cycle). Similarly, when the phasor moves 22.5 electrical degrees, the motor will move (22.5/90)×100=25% of a full step. Thus, it is possible to position the motor to any arbitrary angle.

You can easily control the torque phasor's angle by applying two periodic waveforms to the motor, which are shifted by 90 electrical degrees. Let the phase current equations be

$$I_A=I_O\cos\theta_E \qquad (1)$$

and

$$I_B=I_O\sin\theta_E, \qquad (2)$$

where θ_E equals electrical position. The resulting torque generated by the corresponding phases is then

$$T_A=K_OI_A=K_OI_O\cos(\theta_E) \qquad (3)$$

and

$$T_B=K_OI_B=K_OI_O\sin(\theta_E) \qquad (4)$$

where K_O is the torque constant of the motor.

By substituting **Eqs** 1 and 2 into **Eqs** 3 and 4 and performing some vector summation, you attain a value for the total generated torque, measured on the motor shaft, of

$$T_G=K_OI_O.$$

Although you might assume from this exercise that you have attained infinite resolution and thereby lost the quantized motion feature of the motor, you can regain the quantized feature by defining the term microsteps per step. Subdivide each full step into a fixed number of microsteps by driving the motor with intermediate current levels. The current's vector sum will then track the circle in **Fig 1** and divide the full step (90 electrical degrees) into the required number of microsteps. **Fig 1** illustrates the phase currents required for full-step and four microstep/step operation. (Actually, you can implement this operation using look-up tables and two D/A converters.)

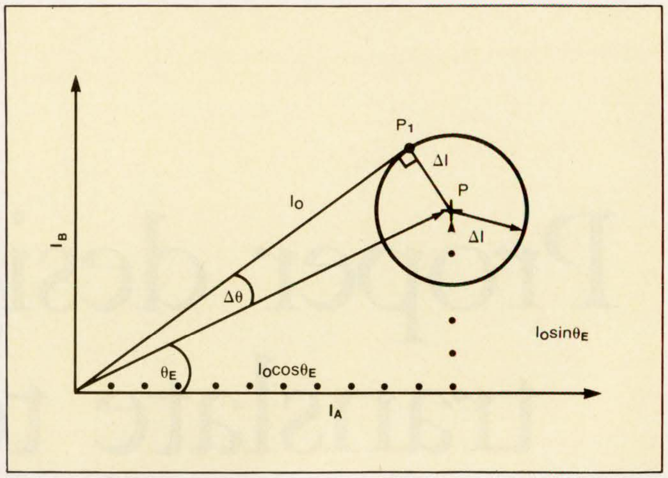


***Fig 2—Worst-case position errors occur** when the vector sum is tangent to the circle.*

Match phase currents for microstepping

To best utilize microstepping techniques to improve resolution, you must first select an appropriate motor based on torque requirements, the specified step accuracy, and the required resolution or number of microsteps/step. Secondly, you have to determine how closely you need to match the phase currents to avoid degrading the step accuracy.

Eqs 1, 2, 3, and **4** clearly indicate that errors in the magnitude or phase of the phase currents will have an impact on positioning accuracy. These equations also illustrate that if you keep the ratio of phase currents (I_A/I_B) constant, errors in their values will only result in torque-value errors, not positioning errors.

Referring to **Fig 2,** assume that the vector sum of currents I_A and I_B is located at point P. You must ascertain the upper boundary of the current errors that will keep the position error within some given angle $\Delta\theta$. Let the phase currents vary by a small amount such that their vector sum lies within the circle that has a

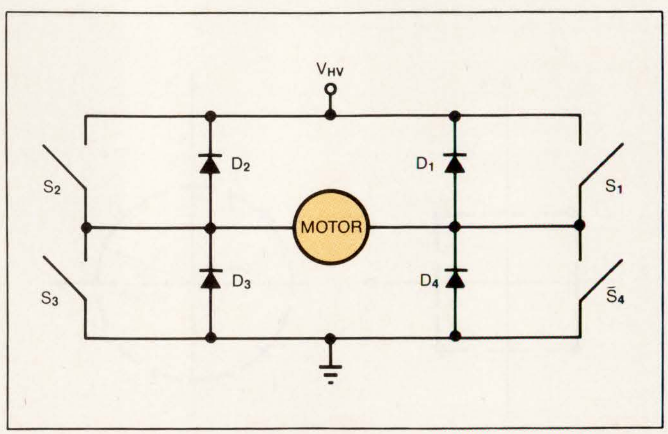


***Fig 3—In this H-bridge circuit operating in a noncirculating mode,** the closure of S_2 and S_4 generates the charging current. S_1 and S_3 then close to generate the discharging current.*

At resonance, a stepping-motor system is likely to lose synchronization and skip or gain a step.

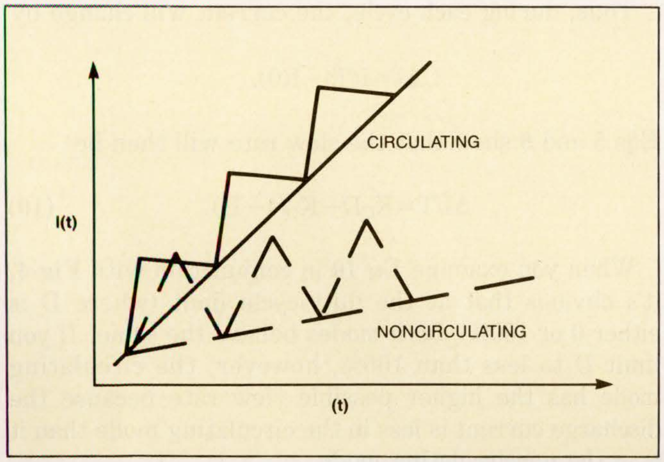


***Fig 4—The circulating and noncirculating modes behave the same** at the duty-cycle limit (0 or 100%).*

radius Δi and that is centered at point P. It follows that the worst-case position error occurs in the cases where the vector sum is tangent to the circle (such as point P_1). At this point,

$$\tan(\Delta\theta)=\Delta I/I_O$$

or

$$\Delta I/I_O=\tan(\Delta\theta).$$

To achieve a position error of less than 1% of a full step, for example, you must keep the total error current under 1.6% of full scale or peak current. This upper error boundary includes all sources such as zero-offset errors and full-scale matching errors. Looking at **Fig 2** again, you can see that in the vicinity of a full step, the phase with the smaller current has the biggest impact on position error.

Implement the H-bridge power stage

Your next design concern involves the implementation of H-bridge power stages for current-regulated PWM control. The stages can have two possible operating modes: circulating and noncirculating. In the noncirculating mode, the closure of S_2 and S_4 generates the phase charging current **(Fig 3)**. Current flows left to right through the motor's phase winding. At the appropriate moment, S_1 and S_3 close, generating a discharge current that flows through D_3 and D_1 back into the power-supply leads and typically charges the supply's output capacitor. In practice, you'll find that the charge and discharge slopes are about equal in the steady-state condition. For a low back-EMF, the forcing voltage for charge and discharge is about equal but opposite in sign.

In the circulating mode, the charging action mirrors that of the noncirculating mode. After the current reaches the appropriate level, however, only S_2 opens. The resulting discharge current then flows through D_3 and S_4 until the beginning of the next cycle. In general, the discharge slope is much smaller than the charge slope because there's no forcing voltage during the discharge phase—only initial current.

Next, define the duty cycle (D) and charge/discharge current slopes ($I_C(t)/I_D(t)$):

$$D=t_1/T$$

$$K_C=(B-A)/DT$$

$$K_D=(B-A)/(1-D)T;$$

therefore

$$I_C(t)=A+K_Ct \text{ for } 0\le t<DT \quad (5)$$

$$I_D(t)=A+(K_C+K_D)-K_Dt \text{ for } DT\le t<T. \quad (6)$$

After some mathematical manipulation, the result is

$$I_{AV}(t)=A+\tfrac{1}{2}(K_C+K_D)T[K_C/(K_C+K_D)-(D-1)^2].$$

In the steady-state (or static) case, $I_{AV}(t)$ is constant. Therefore,

$$I_C(0)=I_DT. \quad (7)$$

Combining **Eqs 5, 6,** and **7** for the steady-state duty cycle results in

$$D_{SS}=K_D/K_C+K_D. \quad (8)$$

According to **Eq 8,** and because both slopes are approximately equal in the noncirculating mode, D=50%. You can thus define the phase ripple current as

$$\Delta I_{PP}=I_D(DT)-I_D(T). \quad (9)$$

Combining **Eqs 6** and **9** results in

$$\Delta I_{PP}=T[(K_CK_D)/(K_C+K_D)].$$

Near a full step, the phase carrying the smallest current has the biggest impact on position error.

Maximum ripple current occurs when $K_C=K_D=K$. It has the value

$$\Delta I_{PP}=KT/2.$$

This mathematical exercise indicates that as far as ripple current is concerned, the noncirculating mode is never better than the circulating mode. In the noncirculating mode, D=50% (ripple is at its maximum), whereas in the circulating mode, D=0 (ripple is at its minimum).

Parameter affects slew-rate limiting

Ripple current notwithstanding, you also have to evaluate the maximum rate of change of $I_{AV}(t)$ in the two modes. This parameter sets an upper limit on the rate of change of the phase currents and on the maximum motor velocity in a microstepping application. When the positioning system reaches this velocity limit, it is in a slew-rate-limiting condition. This condition means that the product of the peak undistorted phase current and the frequency of the input command is a constant value.

To simplify things, assume that the ripple current stays approximately constant, which is a fair assumption because the motor's back-EMF voltage is the major contributor to changes in ripple current. This motor voltage changes relatively slowly compared to the modulator's chopping frequency.

Thus, during each cycle, the current will change by

$$\Delta I=I(T)-I(0).$$

Eqs 5 and **6** show that the slew rate will then be

$$\Delta I/T=K_C D-K_D(1-D). \qquad \textbf{(10)}$$

When you examine **Eq 10** in conjunction with **Fig 4**, it's obvious that at the duty-cycle limit (where D is either 0 or 100%), both modes behave the same. If you limit D to less than 100%, however, the circulating mode has the higher possible slew rate because the discharge current is less in the circulating mode than it is in the noncirculating mode.

Technically, it is much more difficult to build a circulating-mode PWM controller. This mode requires extremely fast circuit-design techniques, which aren't easy to implement. The circulating mode has another drawback: It doesn't return any energy to the power supply and thus is less efficient. A noncirculating-mode PWM controller, on the other hand, operates efficiently at duty cycles of approximately 50%.

Fig 5 shows the power-driver stage for a sample controller system and an IC that operates at a PWM switching frequency of 10 to 400 kHz **(Fig 6)**. To drive a 2-phase stepping motor, you need two of these stages. **Fig 5**'s circuit uses two n-channel and two p-channel

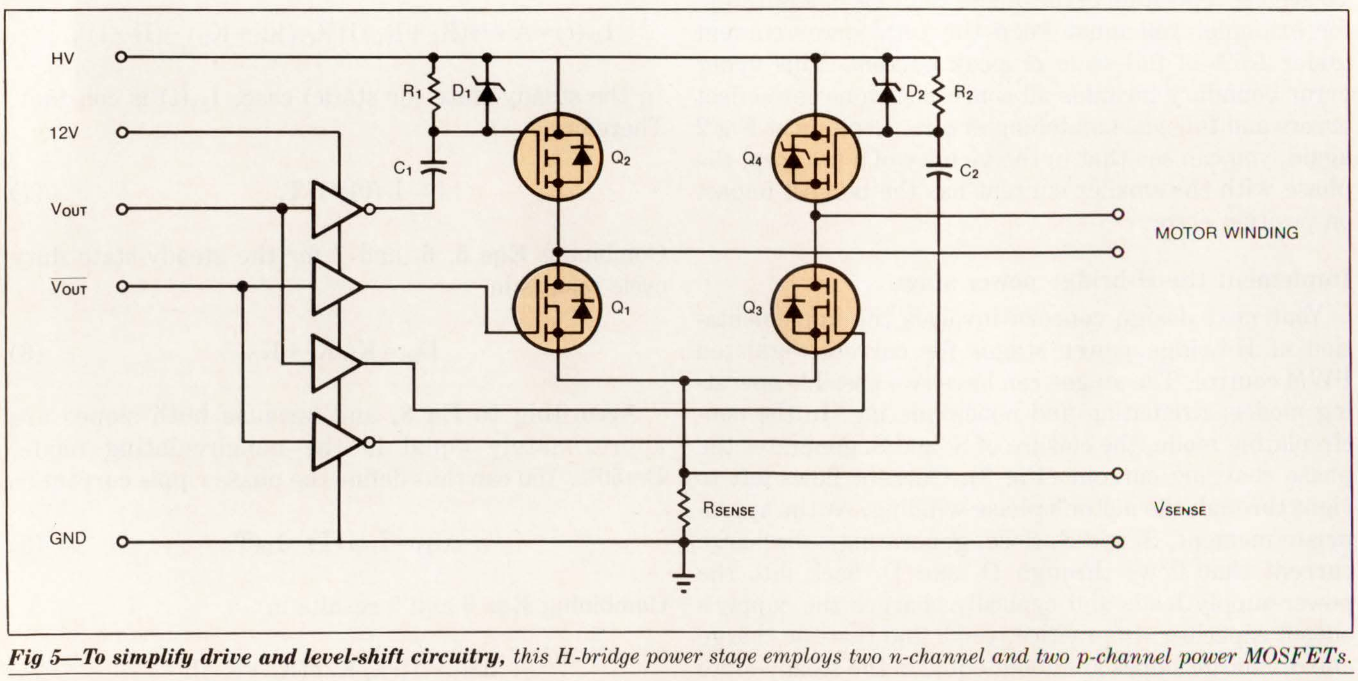


Fig 5—To simplify drive and level-shift circuitry, *this H-bridge power stage employs two n-channel and two p-channel power MOSFETs.*

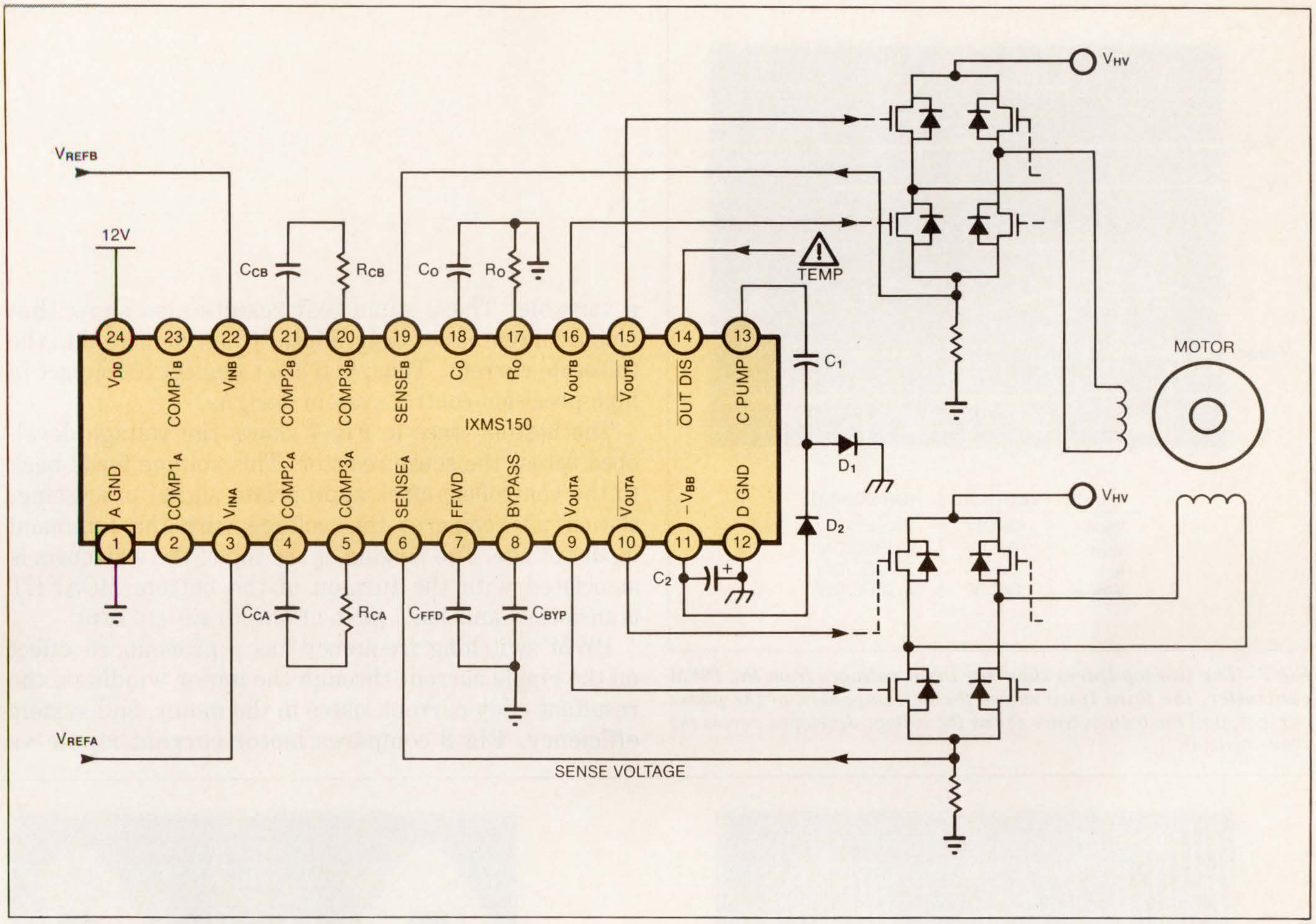


***Fig 6—This system's built-in undervoltage lockout feature** holds the outputs low until the negative-bias voltage is high enough to accept the negative sense voltages.*

power MOSFETs rather than an all n-channel architecture. P-channel transistors are larger and more expensive than similarly rated n-channel devices, but the use of p-channel units simplifies the drive and level-shift circuitry, which lowers component count and increases reliability. It also makes it easier to hybridize the circuit.

AC coupling enhances efficiency

This topology also offers other advantages. Using ac coupling in the level-shifting circuitry increases efficiency because there's no power dissipation with capacitors. Also, you can use the same circuit for motor applications where the supply voltage ranges from tens to hundreds of volts. Obviously, you have to change the transistors and capacitors to accommodate such voltage levels, but there's no need to change circuit topology.

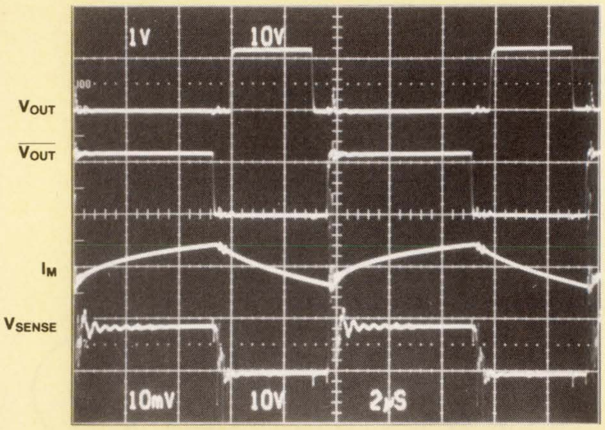
The circuit does have one limitation. It cannot accommodate operation at duty-cycle extremes (one input constantly low with the other constantly high). If an extreme duty-cycle condition persists, coupling capacitors C_1 and C_2 will charge to a voltage level that's high enough to turn off (and perhaps destroy) the two top transistors (Q_1 and Q_2). You can always remedy this problem by restricting the duty-cycle excursions.

In the control system of **Fig 6**, however, the IXMS150 solves this problem in another way. It places a minimum limit of 0.5 μsec on the output pulse width. Operating at 100 kHz, this translates to a 5 to 95% duty-cycle range. At 20 kHz, the duty-cycle range measures 1 to 99%. Limiting the duty cycle to D_{MAX} in the unrestricted case limits the maximum slew rate to $1-D_{MAX}^2$, which translates to 90% at 100-kHz operation.

Fig 7 shows the circuit waveforms for **Fig 5.** The two top traces illustrate the PWM controller's input voltages. Note that the input voltages aren't exactly complementary, but include a deadtime programmable by using the controller. This deadtime prevents Q_1 and Q_2 from conducting simultaneously. The third trace is the ac component of the phase current, and it indicates a ripple current of about 200 mA p-p. The supply voltage for these measurements is 40V, and the switching frequency is 100 kHz.

Select a phase-current sensing scheme

Most PWM controllers monitor and control the peak of the phase current by comparing the voltage across the sense resistor (or a somewhat filtered version of it) with a ramp voltage. The rationale is that the ripple current has a constant amplitude. Unfortunately, test results demonstrate that ripple current varies with frequency. Even in fixed-frequency systems, the ripple current is directly proportional to the motor supply voltage and to the motor's back-EMF voltage, which is



TRACE	VERTICAL	HORIZONTAL
V_{OUT}	10V/DIV	2 µSEC/DIV
$\overline{V_{OUT}}$	10V/DIV	2 µSEC/DIV
I_M	0.2A/DIV	2 µSEC/DIV
V_{SENSE}	1V/DIV	2 µSEC/DIV

Fig 7—The two top traces show the input voltages from the PWM controller, *the third trace shows the ac component of the phase current, and the bottom trace shows the voltage developed across the sense resistor.*

a variable. These same test results also show that ripple current is not insignificant when compared to the full-scale current. Thus, you can't neglect its impact in high-precision-control system designs.

The bottom trace in **Fig 7** shows the voltage developed across the sense resistor. This voltage feeds back to the controller; after appropriate signal processing, the circuit compares this voltage with the command input voltage. The ringing at the top of the waveform is associated with the turn-on of the bottom MOSFET transistors and isn't part of the drain current.

PWM switching frequency has a pronounced effect on the ripple current through the motor windings, the resultant eddy-current losses in the motor, and system efficiency. **Fig 8** compares motor current ripple vs

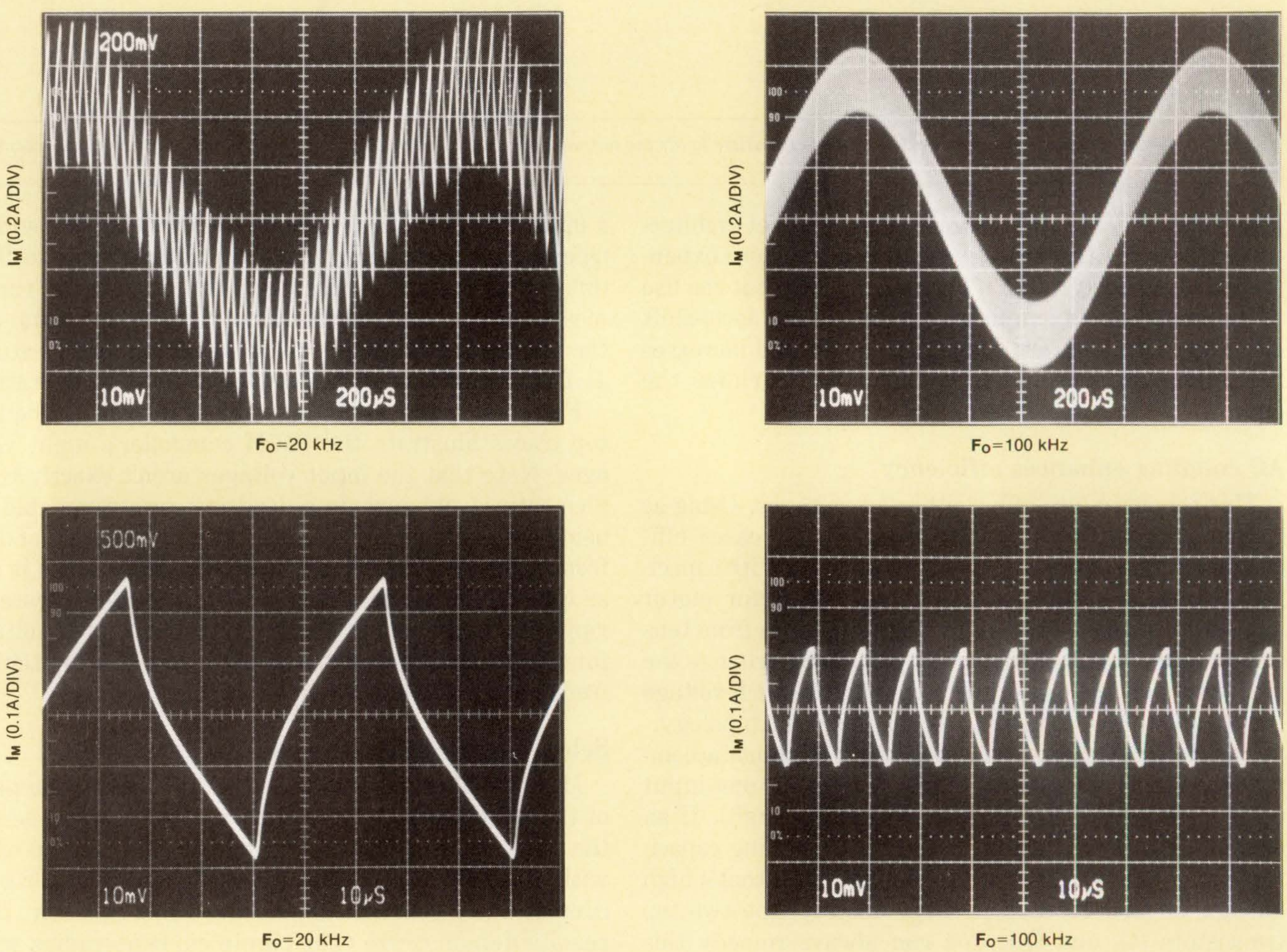


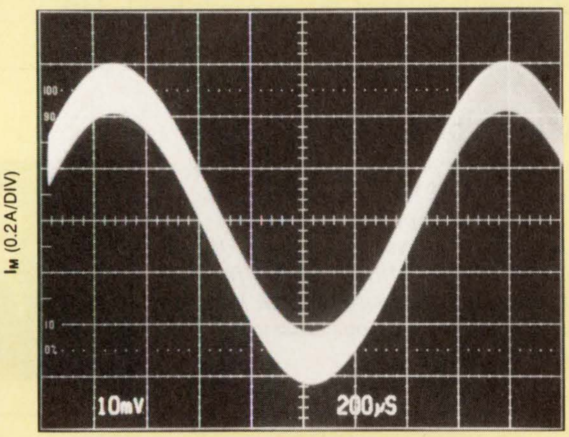
Fig 8—As these scope photos illustrate, current-ripple amplitude isn't exactly inversely proportional *to the frequency. In addition, the charge/discharge waveforms appear to have a double time constant.*

There are two possible operating modes for H-bridge power stages that use current-regulated PWM control: circulating and noncirculating.

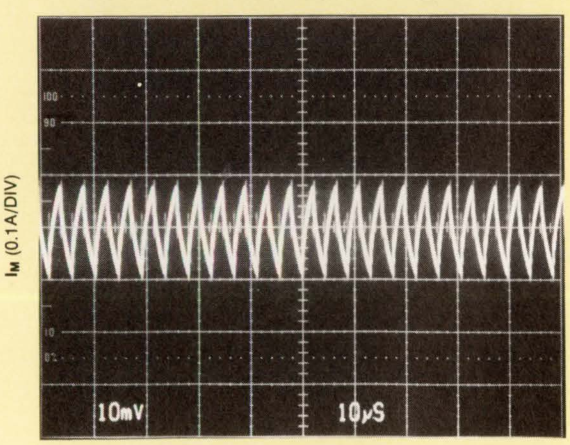
frequency in three ranges: 20, 100, and 250 kHz. As expected, ripple current goes down as frequency increases. Therefore, losses resulting from ripple current also decrease with increasing frequency.

Switching frequency also has an impact on losses in the power stage. These losses, a function of the energy required to turn the power MOSFETs on and off, are proportional to the switching frequency: the higher the frequency, the more on/off transitions per second.

Looking at **Fig 8** again, you can see that current-ripple amplitude is not exactly inversely proportional to the frequency. Secondly, charge/discharge waveforms seem to have a double time constant. The motor in the control-system test setup turns out to be the culprit here—its winding inductance actually decreases with increasing frequency. As unlikely as this might seem, measurement results indicate that, even though the winding inductance is about 3 mH at 1 kHz, it is only 0.8 mH at 100 kHz **(Fig 9)**.



F_O=250 kHz



F_O=250 kHz

Economic considerations take over

Today, many designers cut system costs by minimizing the number of power supplies; they strive to operate the control section from a single supply. Unfortunately, the current-feedback and reference-input signals are bipolar. In the past, designers used level shifting to solve the problem of the reference-input signal. Level shifting wasn't a good solution for the feedback signal, however, because it was very difficult to implement without degrading accuracy or efficiency.

Another solution to the reference-input level problem uses two inputs (sign and magnitude) instead of the usual bipolar input. Some chip vendors have tried this technique because in theory it requires only one supply. In practice, it's necessary to also use a negative power supply to generate a true zero voltage with a low-impedance drive; otherwise, you have to make a trade-off and sacrifice accuracy.

Sign and magnitude inputs also pose another problem. The input-voltage shape resembles a rectified sine wave, which means the system must have an extremely high-speed response at what would be the zero-crossing points for bipolar inputs.

To circumvent this problem and still accommodate single-supply operation, the controller IC in **Fig 6** incorporates an integral negative-bias generator. This circuitry consumes a significant amount of silicon and places stringent demands on noise decoupling. However, it does give the chip flexibility and has no impact on accuracy.

Protect against abnormal conditions

Reliability is a crucial requirement in any system and is especially critical for the high-voltage, high-current, and high-temperature environment of a motor-control system. It is very important to monitor and guard against abnormal conditions such as undervoltage (which would only partially turn on the power transistors and lead to excessive power dissipation in the power stage), overcurrent, and overtemperature (which would destroy the power devices).

The system in **Fig 6** incorporates a built-in undervoltage lockout feature. This lockout holds the outputs low (keeping the gates of the power MOSFETs at ground) until the supply exceeds approximately 9V, and the

The PWM switching frequency has a pronounced effect on ripple current through the motor windings.

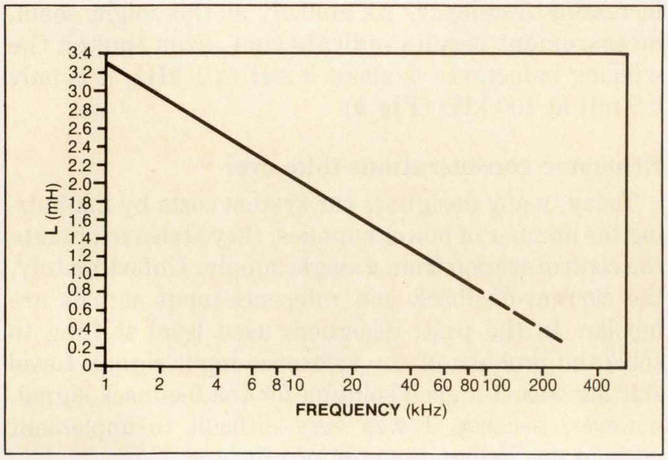


Fig 9—The motor's winding inductance clearly decreases *as the PWM switching frequency increases.*

internal negative-bias voltage is high enough to accept the negative sense voltages associated with normal operation.

The system also includes a 2-level current-limiting scheme. The first level, which is about 40% above full scale, is time dependent to prevent MOSFET turn-on spikes from tripping the system. The second trip point is at about 250% of full scale and is time independent. With this scheme, a true short will trip the system immediately. Finally, the system provides for overcurrent protection on a cycle-by-cycle basis, with automatic reset at the end of the overcurrent condition.

Because the IXMS150 IC doesn't include an integral power section, the power driver must provide the temperature-sensing function. The controller has a pin available that lets you develop overtemperature protection. Pulling this pin low disables the outputs.

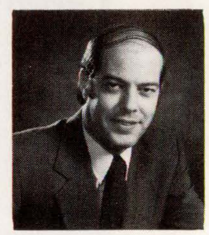
You can also use the output-disable pin as a status-output pin. When the internal circuitry pulls this pin low, it indicates an abnormal condition such as undervoltage, insufficient negative-supply voltage, or overcurrent conditions. You can use this low-output condition to gate or disable the input voltage until negative-supply levels are well enough established to prevent the possibility of latchup. You can also use this signal to poll the status of a smart system or to disable all channels in a multi-axis system.

Feedforward is best for loop compensation

Loop compensation is the final design tradeoff you have to consider. In all fixed-frequency PWM-control system applications, open-loop gain, motor-current slew rate, and motor-current ripple are proportional to the motor supply voltage. Feedforward, historically associated with switch-mode power supplies, is an open-loop technique that compensates for variations in the high-voltage level. In applications requiring high-current slew rates (such as high velocities), high supply voltage (with its associated high current ripple) is inevitable.

Using feedforward in a microstepping motor-control system offers some advantages. First, it allows you to use supplies that are not highly regulated. Second, feedforward lets you design sophisticated, high-performance systems that can take advantage of the adaptive motor-supply feature. These systems have to be stable under widely varying motor supply conditions. Without feedforward compensation, gain variations due to supply-voltage changes would complicate system design and severely restrict the system's bandwidth. **EDN**

Author's biography



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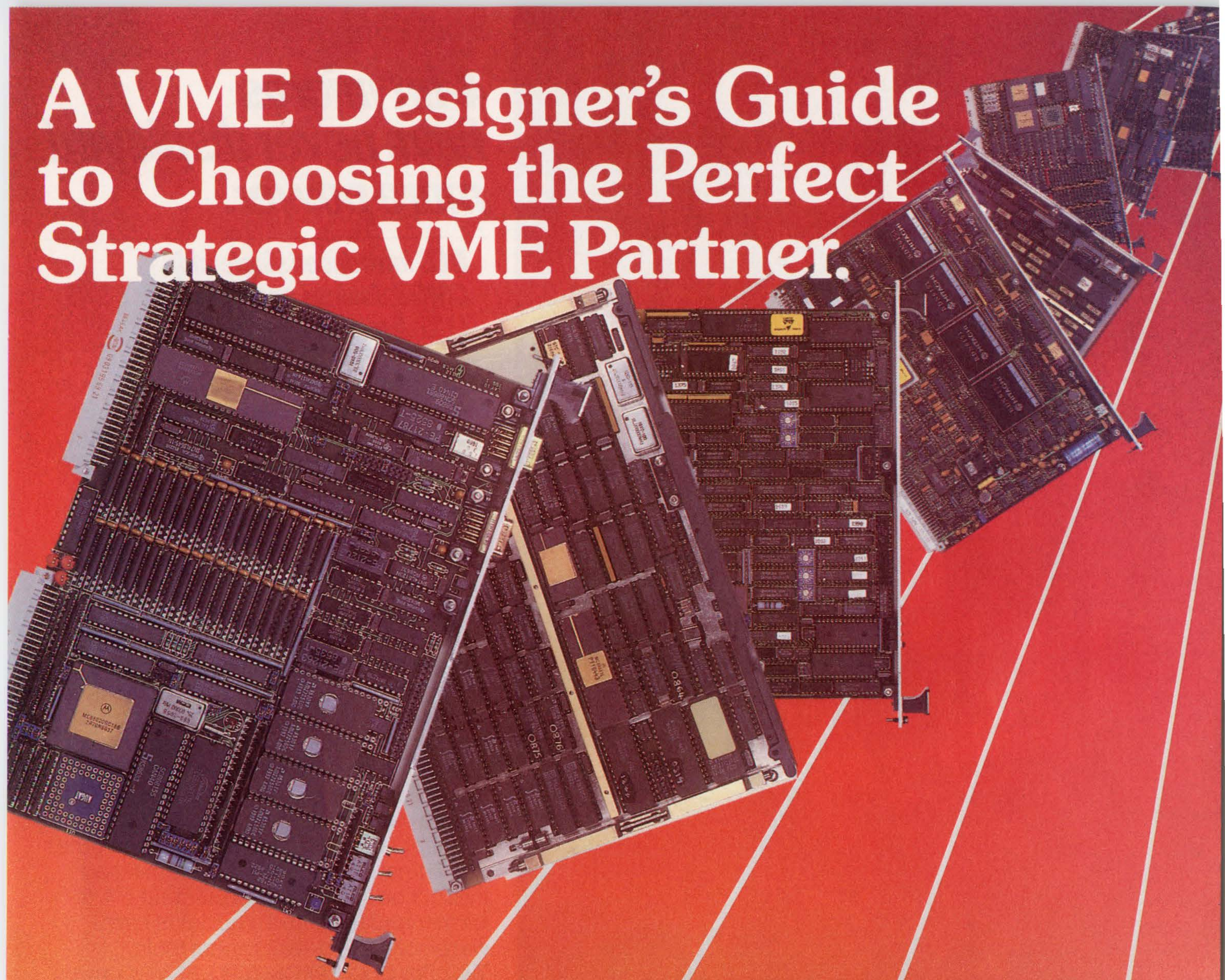

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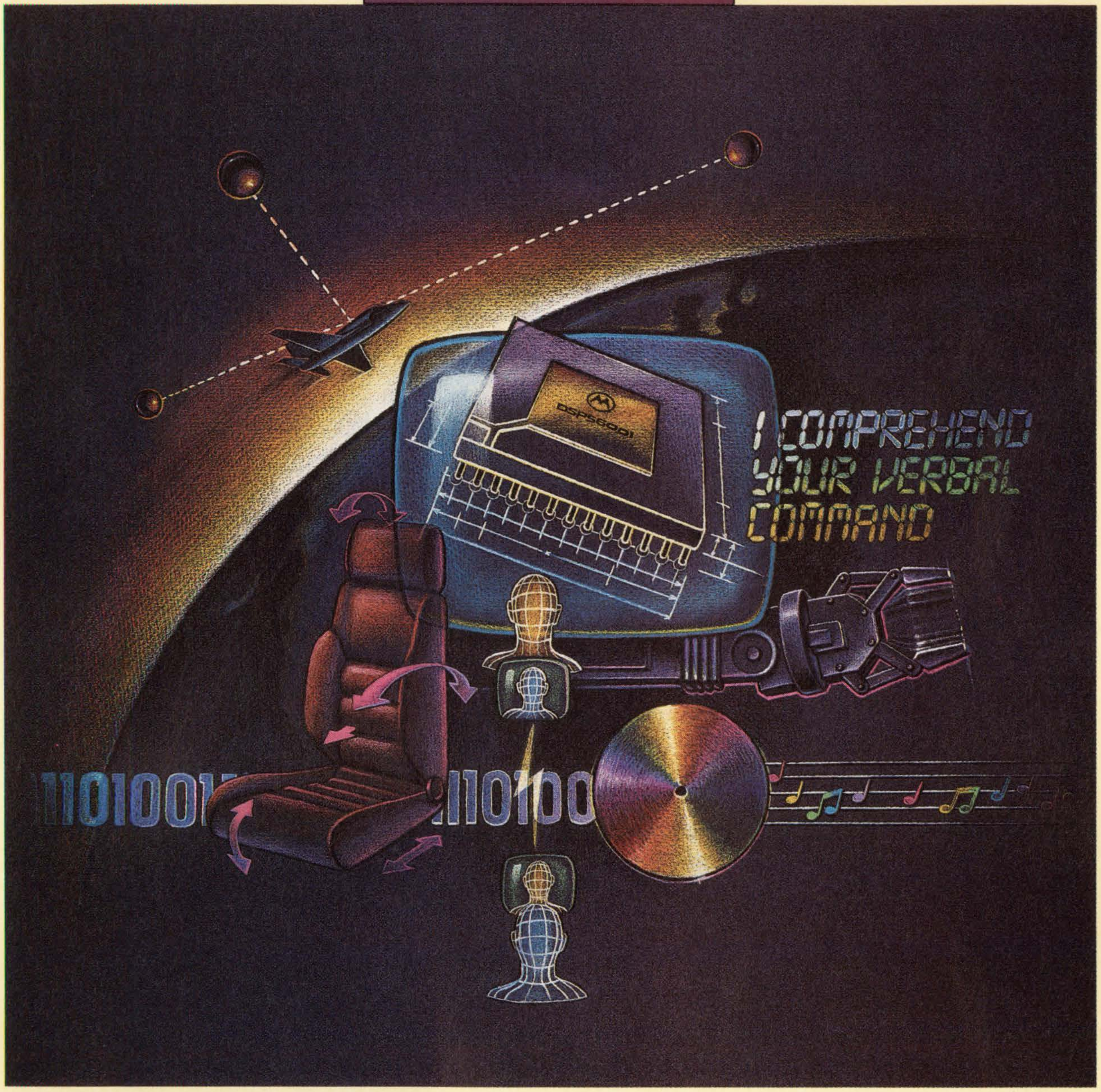

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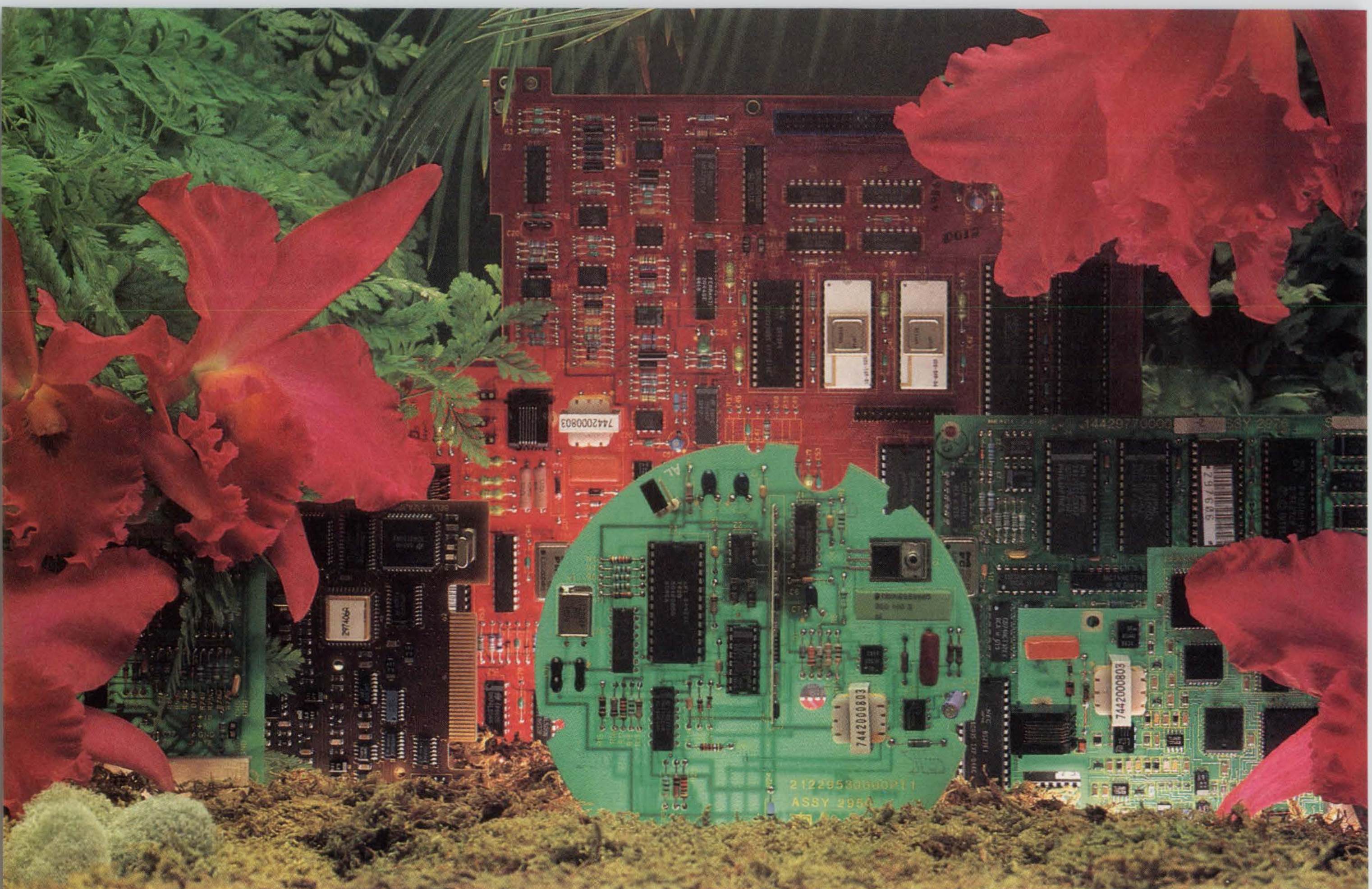

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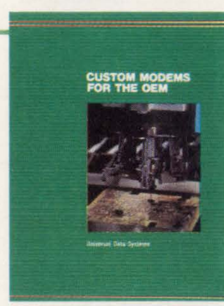

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At IEDM, new ways to boost chip speed and density. *Staff; Electronics, 11/27/86, pg 66, 3 pgs.*

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Manufacturers of fast CMOS logic families take sides in packaging controversy. *Mosley, J D, Regional Editor; EDN, 04/15/87, pg 69, 7.33 pgs.*

Mixed analog/digital technologies pack complete systems on-chip. *Martin, Steven L, Contributing Editor; Computer Design, 04/01/87, pg 39, 6 pgs.*

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Special report: AI boosts IQ of silicon compilers. *McLeod, Jonah, Staff Editor; Electronics, 04/30/87, pg 54, 4 pgs.*

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Wanted: Communications software for multiprocessing. *Boberg, Richard W, Microbar Systems; Digital Design, 03/87, pg 72, 4 pgs.*

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Debug system targets multiprocessor design. *Noelcke, Gus, Northwest Instrument Systems; Computer Design, 11/01/86, pg 105, 6.5 pgs.*

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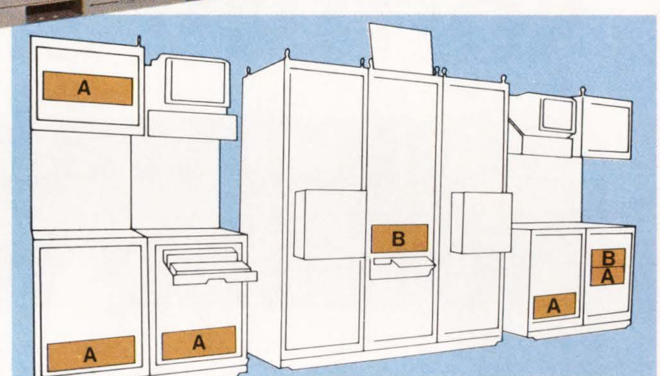

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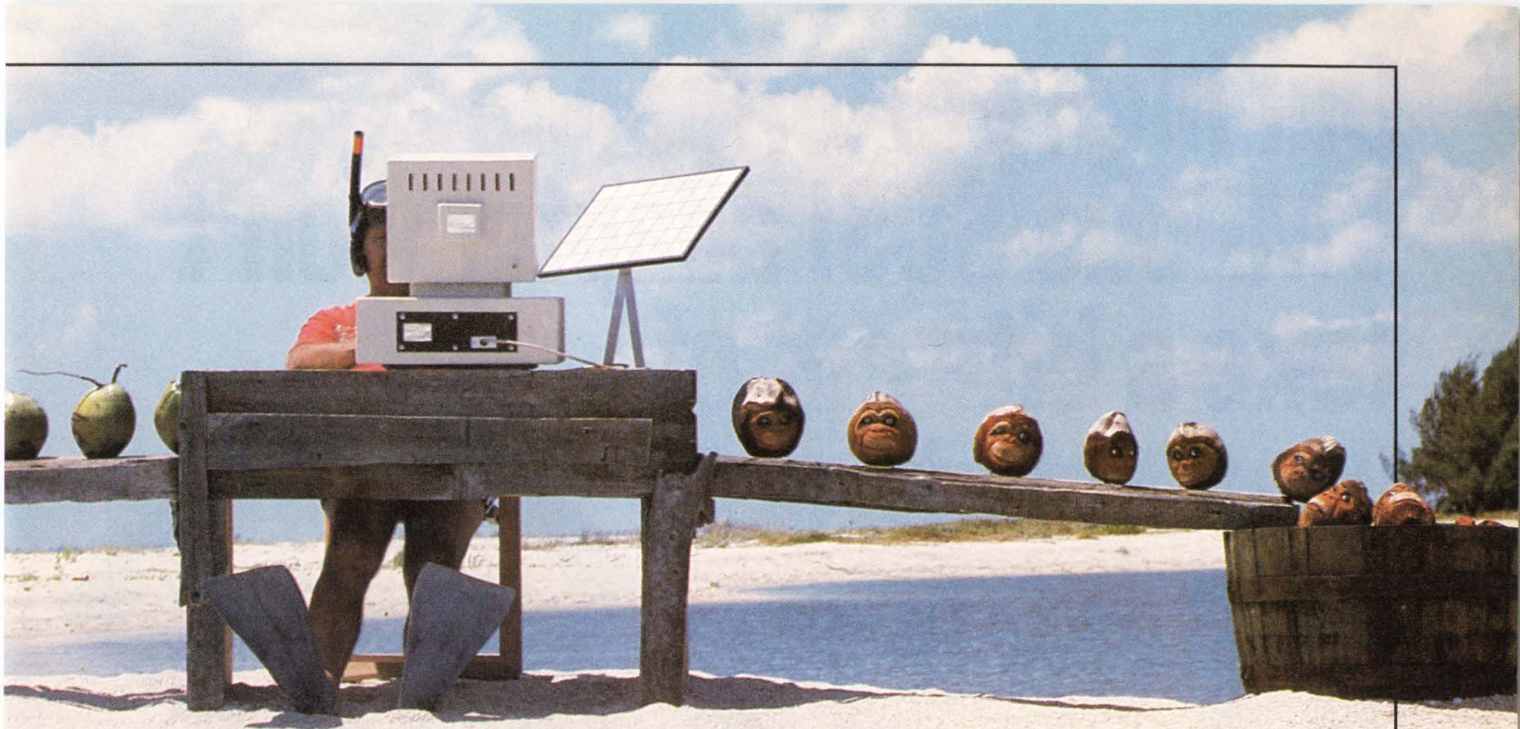

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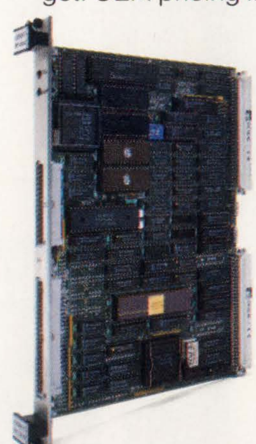

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William E, Contributing Editor; Computer Design, 11/15/86, pg 49, 5 pgs.

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Microprogram monitor helps develop bit-slice designs. *Richardson, Brian, Hewlett-Packard Co; EDN, 03/31/87, pg 191, 5 pgs.*

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Focus on conductive elastomers. *Bernhard, Robert, Electronic Design, 11/20/86, pg 149, 5 pgs.*

Higher pin densities, custom assemblies reshape insulation-displacement. *Bloom, Michael, Electronic Design, 11/13/86, pg 91, 4.5 pgs.*

Simple solution cures glitches on high-speed buses. *DeBock, Richard M, Matrix Corp; EDN, 04/30/87, pg 173, 6.5 pgs.*

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1987 U.S. market report: Consumer. *Staff; Electronics, 01/08/87, pg 64, 2 pgs.*

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A new wave rises on the Pacific Rim. *Berger, Michael, Staff Editor; Shapiro, Don, Staff Editor; Electronics, 04/02/87, pg 78, 2 pgs.*

A one-world industry is arriving fast. *Erikson, Arthur, Staff Editor; Electronics, 04/02/87, pg 69, 4 pgs.*

A streamlined AMD fights back, looks for strategic partners. *Barney, Clifford, Staff Editor; Electronics, 03/19/87, pg 64, 2 pgs.*

Convergent hustles to turn around. *Barney, Clifford, Staff Editor; Electronics, 11/13/86, pg 66, 2 pgs.*

Does Catalyst have the key to smart cards? *Staff; Electronics, 12/18/86, pg 59, 4 pgs.*

Europe pushes hard for global role. *Gosch, John, Staff Editor; Electronics, 04/02/87, pg 75, 1.5 pgs.*

Japan drives for strategic alliances. *Cohen, Charles L, Staff Editor; Electronics, 04/02/87, pg 76, 2 pgs.*

LSI Logic's big bag of ASIC design tools. *Staff; Electronics, 02/05/87, pg 59, 3 pgs.*

Recruiting engineers to the South Bronx is a task less difficult than it seems. *Asbrand, Deborah, Staff Editor; EDN, 12/11/86, pg 305, 3 pgs.*

Siemens joins the 1-Mb DRAM club. *Gosch, John, Staff Editor; Electronics, 11/13/86, pg 30, 0.5 pgs.*

The look of the industry in 2000. *Weber, Samuel, Staff Editor; Electronics, 04/02/87, pg 60, 2 pgs.*

Under Thomson's wing, Mostek is beginning to fly. *Lineback, J Robert, Staff Editor; Electronics, 04/16/87, pg 48, 1 pg.*

Winds of change sweep the industry. *Barney, Clifford, Staff Editor; Electronics, 04/02/87, pg 62, 6 pgs.*

Counters

Counter-timers beat the 60-GHz clock and break through 2-ns resolution. *Bloom, Michael, Electronic Design, 11/20/86, pg 78, 6.5 pgs.*

Electronic counters move ahead—slowly. *Yates, Warren, Staff Editor; Electronic Products, 12/01/86, pg 44, 4 pgs.*

Scopes wield counter-timer for automatic measurements. *Baker, Cliff, Tektronix; Electronic Design, 11/13/86, pg 113, 4 pgs.*

Crystals/crystal oscillators

The quickening (beat) of the quartz crystal. *Chin, Spencer, Staff Editor; Electronic Products, 11/03/86, pg 65, 4 pgs.*

D

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1987 U.S. market report: Communications. *Staff; Electronics, 01/08/87, pg 58, 3 pgs.*

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Use structured arrays for high-performance data processing. *Chang, Yen, LSI Logic Corp; EDN, 04/15/87, pg 177, 6 pgs.*

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Board-level systems set the trend in data acquisition. *Shapiro, Sydney F, Staff Editor; Computer Design, 04/01/87, pg 59, 12.5 pgs.*

Data-acquisition system fits on a smart peripheral chip. *Yager, Charles, Micro Linear; Electronic Design, 03/05/87, pg 85, 5 pgs.*

Design steps improve effective resolution of digitizing scopes, waveform digitizers. *Everett, Chris, Regional Editor; EDN, 01/08/87, pg 61, 5.5 pgs.*

Optical encoders are shrinking to satisfy position-sensing application requirements. *Ormond, Tom, Senior Editor; EDN, 11/27/86, pg 81, 4.33 pgs.*

Synchronous VFC enhances accuracy in analog-input systems. *DeVito, Larry, Analog Devices Semiconductor; EDN, 11/13/86, pg 269, 9.5 pgs.*

Tapping the analog world for serial 10-bit data. *Redfern, Thomas P; Rempfer, William, Linear Technology; Electronic Products, 04/01/87, pg 32, 7.5 pgs.*

Data-communications systems/techniques

Analyzers keep pace with communications protocol development. *Mayer, John H, Staff Editor; Computer Design, 03/01/87, pg 81, 3 pgs.*

Availability of cryptographic ICs augurs the increasing use of data encryption. *Terry, Chris, Associate Editor; EDN, 01/22/87, pg 63, 4 pgs.*

ISDN gains ground as needed ICs emerge. *Mokhoff, Nicolas, Staff Editor; Computer Design, 11/15/86, pg 43, 4.5 pgs.*

ISDN terminals simplify data transmissions. *O'Toole, Tony, Advanced Micro Devices; EDN, 01/22/87, pg 167, 8 pgs.*

Serial data races at parallel rates for the best of both worlds. *Connor, Gary, et al, Advanced Micro Devices; Electronic Design, 01/22/87, pg 79, 5 pgs.*

Synchronous-network circuit boosts network flexibility. *Vesuna, Sarosh N, Advanced Micro Devices; EDN, 11/13/86, pg 231, 6 pgs.*

Use statistics to test communications systems efficiently. *Cobb, R F, Harris Corp; EDN, 01/08/87, pg 143, 9 pgs.*

Use structured arrays for high-performance data processing.

Chang, Yen, LSI Logic Corp; EDN, 04/15/87, pg 177, 6 pgs.

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Comparing ADC architectures is a designer's best bet. *Koen, Mike, Burr-Brown; Electronic Design, 01/22/87, pg 119, 4 pgs.*

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Hardware methods improve 1-chip A/D converters. *Sidman, Steven, Harris; EDN, 02/05/87, pg 139, 13.5 pgs.*

Interface options enhance fast video converter. *Price, John; Morgan, Dennis, Motorola Semiconductors; Electronic Products, 12/15/86, pg 31, 4 pgs.*

New D-A converters boast higher performance and lower cost. *Mayer, John H, Staff Editor; Computer Design, 03/15/87, pg 90, 5 pgs.*

Resolver-to-digital IC makes move to monolithic. *Sylvan, John, Analog Devices; Electronic Design, 02/05/87, pg 84, 6 pgs.*

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Tapping the analog world for serial 10-bit data. *Redfern, Thomas P; Rempfer, William, Linear Technology; Electronic Products, 04/01/87, pg 32, 7.5 pgs.*

The standouts among fast converter ICs. *Spadaro, Joseph J, Staff Editor; Electronic Products, 02/15/87, pg 29, 4 pgs.*

Thermal-tracking IC converts rms to dc. *Williams, Jim, Linear Technology Corp; EDN, 02/19/87, pg 137, 15 pgs.*

Video hybrid digitizes images at RS-170 rates. *Hansford, Alan, Analog Devices; Digital Design, 03/87, pg 50, 3 pgs.*

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Availability of cryptographic ICs augurs the increasing use of data encryption. *Terry, Chris, Associate Editor; EDN, 01/22/87, pg 63, 4 pgs.*

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Design steps improve effective resolution of digitizing scopes, waveform digitizers. *Everett, Chris, Regional Editor; EDN, 01/08/87, pg 61, 5.5 pgs.*

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1987 U.S. market report: Data processing. *Staff; Electronics, 01/08/87, pg 54, 4 pgs.*

Add-in facsimile boards enable users of PCs to transfer CAE graphics in real time. *Terry, Chris, Associate Editor; EDN, 03/04/87, pg 53, 2.66 pgs.*

Fast-settling op amps aid in data conversion. *Kitchin, Charles, et al, Analog Devices Semiconductor; EDN, 03/18/87, pg 185, 5.5 pgs.*

Design services

Parameterizable cells strike middle ground between fixed and compiled cells. *Bloom, Michael, Contributing Editor; Computer Design, 11/01/86, pg 24, 5.5 pgs.*

Development systems

In-circuit emulators crowd eagerly onto the PC platform. *Leonard, Milt, Staff Editor; Electronic Products, 02/01/87, pg 19, 4 pgs.*

μP simulators let you debug software on an IBM PC. *Wright, Maury, Regional Editor; EDN, 12/11/86, pg 196, 6.5 pgs.*

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Hand-held DMMs exploit custom CMOS ICs to boost accuracy and add features. *Costlow, Terry, Staff Editor; Electronic Design, 11/27/86, pg 75, 5 pgs.*

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AT&T packs performance into its one-chip DSP. *Staff; Electronics, 02/19/87, pg 74, 2 pgs.*

CMOS DSP chip packs punch of a supercomputer. *Simar, Jr, Ray; Hames, Mike, Texas Instruments; Electronic Design, 03/19/87, pg 103, 5.5 pgs.*

DSP: A technology in search of applications. *Marrin, Ken, Staff Editor; Computer Design, 11/15/86, pg 59, 14 pgs.*

The multiple choices in DSP chips. *Myrvaagnes, Rodney, Staff Editor; Electronic Products, 04/15/87, pg 60, 8.5 pgs.*

The star of single-chip digital signal processing is rising. *Bader, Maryann L, Bader Associates; Electronic Products, 01/15/87, pg 41, 2 pgs.*

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Digitizing instruments: Making a fair comparison. *Manieri, Lawrence J, Sequence; Electronic Design, 11/20/86, pg 121, 3.5 pgs.*

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1987 U.S. market report: Components. *Staff; Electronics, 01/08/87, pg 72, 3 pgs.*

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Compiler allows Ada development on an IBM PC/AT. *Tetewsky, Avram, et al, Charles Stark Draper Laboratory Inc; EDN, 02/19/87, pg 157, 7.5 pgs.*

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LCDs lead the assault on CRT's dominance. *Williams, Tom, Staff Editor; Computer Design, 11/01/86, pg 53, 5 pgs.*

Next-generation LCDs abound with options. *Confrey, Jack, Epson America; Electronic Products, 11/03/86, pg 85, 3 pgs.*

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Former engineers parlay technical expertise into new careers. *Asbrand, Deborah, Staff Editor; EDN, 12/25/86, pg 169, 3.5 pgs.*

"Information revolution" may not make jobs. *Patton, Carole, Staff Editor; Electronic Design, 02/05/87, pg 16, 0.5 pgs.*

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Hierarchical-level CAE system features snap and simplicity. *Miadejovsky, Michael, Hewlett-Packard Salt Lake Cericor Operation; Electronic Design, 02/19/87, pg 113, 4 pgs.*

Pc-board workstation links production to design. *White, Lisa D; LeBrun, Jim, Cadnetix; Electronic Design, 03/19/87, pg 117, 5 pgs.*

Processor board recasts PC into 5-MIPS Unix workstation. *Lundell, Jon, et al, Opus Systems; Electronic Design, 03/05/87, pg 119, 4.5 pgs.*

Sony packs power into low-cost work stations. *Staff; Electronics, 03/19/87, pg 79, 3 pgs.*

Workstations leap ahead toward interactive CAE goal. *Lin, Patrick; Lauta, Andy, Daisy Systems; Electronic Design, 04/30/87, pg 113, 4 pgs.*

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Behavioral models and hardware modelers simulate pc boards containing VLSI devices. *Freeman, Eva, Associate Editor; EDN, 11/13/86, pg 65, 5.33 pgs.*

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Digital GaAs ICs make their move. *Tunick, Diane, Staff Editor; Electronic Design, 04/16/87, pg 35, 2 pgs.*

GaAs ICs add gain block to rf designer's arsenal. *Schappacher, Jerry, Harris Microwave Semiconductor; Electronic Design, 03/05/87, pg 109, 2.5 pgs.*

GaAs VLSI progresses toward commercial viability. *Bond, John, Contributing Editor; Computer Design, 01/15/87, pg 31, 4 pgs.*

GaAs bit-slice processors blaze past silicon equivalents. *Aseo, Joseph, Staff Editor; Digital Design, 12/86, pg 22, 1 pg.*

GaAs chips strive to mirror silicon functions. *Spadaro, Joseph J, Staff Editor; Electronic Products, 01/01/87, pg 41, 4 pgs.*

GaAs wedges deeper into digital LSI market. *Leonard, Milt, Staff Editor; Electronic Products, 04/15/87, pg 15, 2 pgs.*

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The first GaAs compiler is already producing chips. *McLeod, Jonah, Staff Editor; Electronics, 04/30/87, pg 58, 3 pgs.*

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Will Sematech fly? The next three months will tell. *Barney, Clifford, Staff Editor, et al; Electronics, 03/19/87, pg 31, 1.5 pgs.*

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A versatile architecture for imaging. *Casey, Patrick, Imaging Technology; Digital Design, 02/87, pg 81, 3.5 pgs.*

Convolution hardware accelerates imaging tasks. *MacRae, David, Matrox Electronic Systems; Digital Design, 01/87, pg 58, 3.5 pgs.*

Graphics chips, boards bring CAD to personal computers. *Gold, Martin, Staff Editor; Electronic Design, 02/19/87, pg 67, 5 pgs.*

Imaging boards put algorithms in hardware to up throughput. *Weir, Tony, Vision Systems; Digital Design, 03/87, pg 55, 3 pgs.*

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Graphics developments geared toward speed and capacity. *Williams, Tom, Staff Editor; Computer Design, 12/86, pg 127, 8 pgs.*

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Optimize your graphics system for 2-D and 3-D. *Khurana, Anoop S, et al, Advanced Micro Devices Inc; EDN, 03/18/87, pg 161, 12.5 pgs.*

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Overseas market report: Another tough year. *Staff; Electronics, 01/22/87, pg 65, 23 pgs.*

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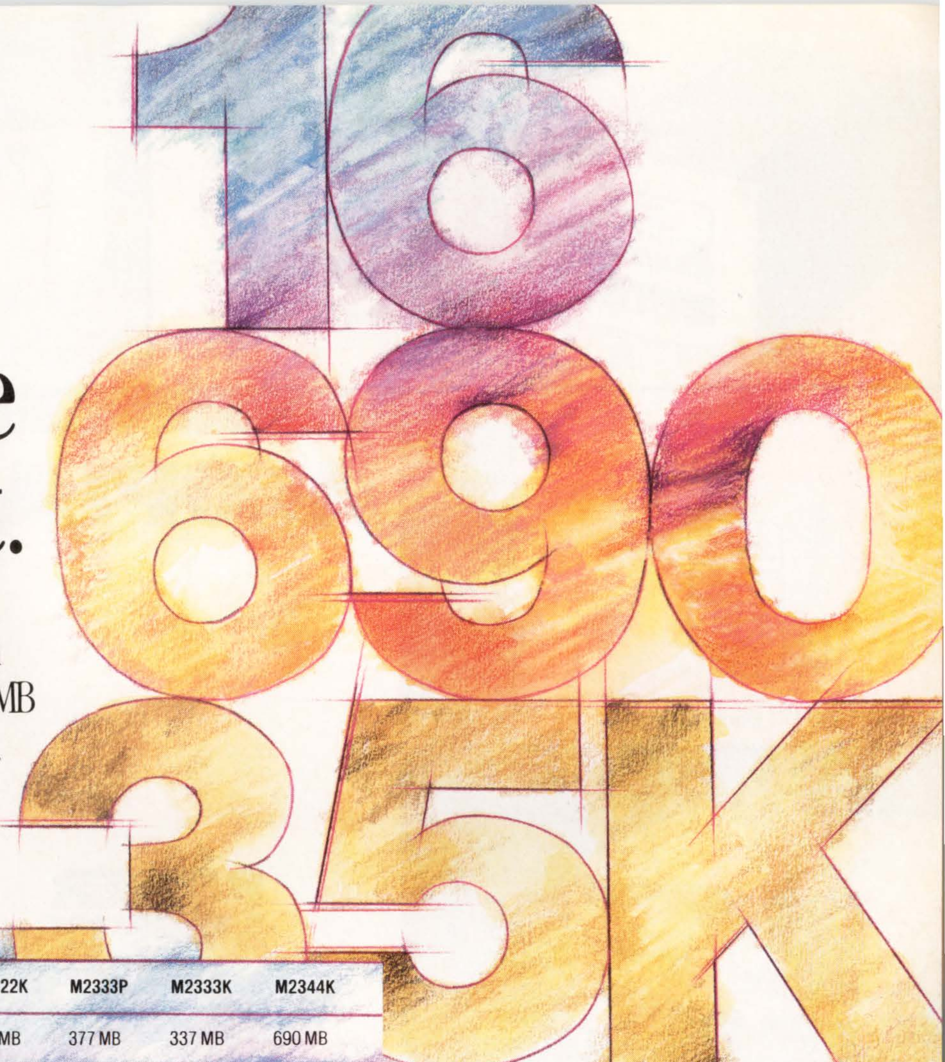

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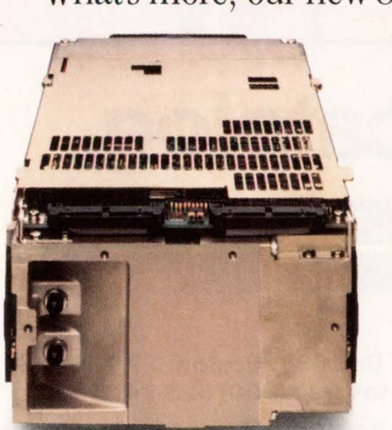

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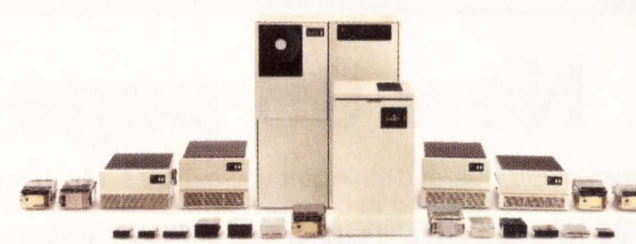

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SSH15N55	IRFP141	IRFP251	IRFP351	IRFP453	**N-Channel**	IRF522	IRF631	IRF740	IRF9511	IRF9620	SSM10N60	IRF131	IRF240	IRF343	IRF452	IRF9242
SSH10N55	IRFP142	IRFP252	IRFP352	**P-Channel**	**TO-220**	IRF523	IRF632	IRF741	IRF9512	IRF9621	SSM8N60	IRF132	IRF241	IRF350	IRF453	IRF9243
SSH8N55	IRFP143	IRFP253	IRFP353	**TO-3P**	SSP6N70	IRF530	IRF633	IRF742	IRF9513	IRF9622	SSM6N60	IRF133	IRF242	IRF351	**P-Channel**	**N-Channel**
SSH6N55	IRFP150	IRFP320	IRFP420	IRFP9130	SSP4N70	IRF531	IRF640	IRF743	IRF9520	IRF9623	SSM4N60	IRF140	IRF243	IRF352	**TO-3**	**TO-92L**
SSH4N55	IRFP151	IRFP321	IRFP421	IRFP9131	SSP3N70	IRF532	IRF641	IRF820	IRF9521	IRF9630	SSM15N55	IRF141	IRF250	IRF353	IRF9130	IRFL1Z0
			IRFP422	IRFP9132	SSP2N70	IRF533	IRF642	IRF821	IRF9522	IRF9631	SSM10N55	IRF142	IRF251	IRF420	IRF9131	IRFL1Z3
				IRFP9133	SSP6N60	IRF540	IRF643	IRF822	IRF9523	IRF9632	SSM8N55	IRF143	IRF252	IRF421		

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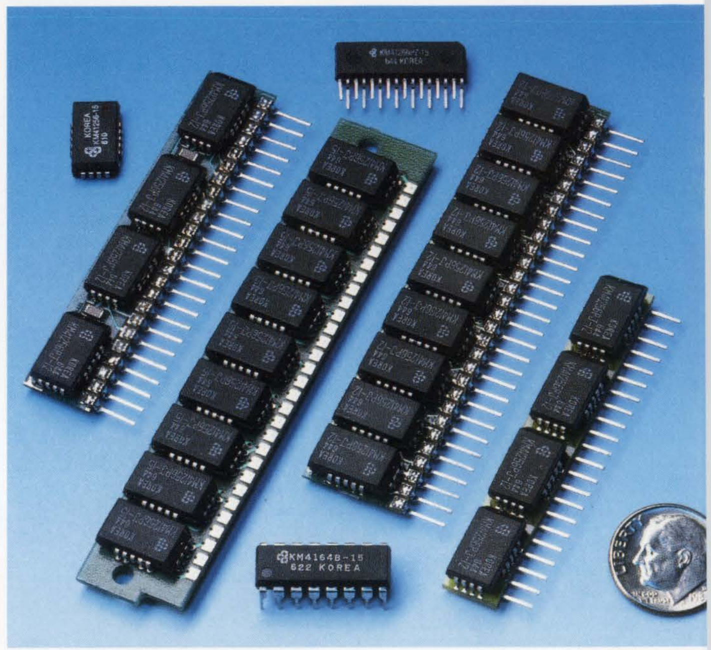
CIRCLE NO. **165**

Nobody is moving faster in memory technology development than Samsung.

Samsung now offers an extensive line of memories: DRAMs, EEPROMs and SRAMs. We are among the industry leaders, producing high quality, highly reliable memory products. Our industry-standard pin-for-pin compatible memories are all proprietary products of our own design, developed in our state-of-the-art R&D facility, utilizing our own technology and processing.

We are determined to be your long term memory supplier. Our production facilities are internationally recognized as being among the most advanced in the world. Samsung is one of the few semiconductor companies fabricating 6-inch wafers in production quantities. This advanced processing technology allows us to keep costs down and volume up.

Samsung's commitment to winning the memory game is underscored by the $600 million we're investing in memory product development and by our new 80,000 square foot headquarters in San Jose, staffed by our 160 person R&D team. This R&D facility has the ultimate in Class-1 clean room technology. A unique vertical laminar flow process helps us control every aspect of the fab environment to achieve the industry's most exacting quality standards. ■



DRAMs

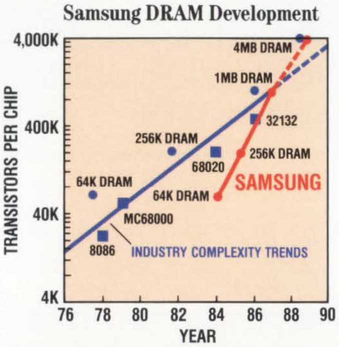
You can see how fast our DRAM technology is progressing in the graphs on the right.

Our 64K and 256K DRAMs are all available in production quantities now. You will be able to get engineering samples of our 1MB DRAM this quarter, qualification samples will be available in mid 1987 with production ramp starting in the third quarter.

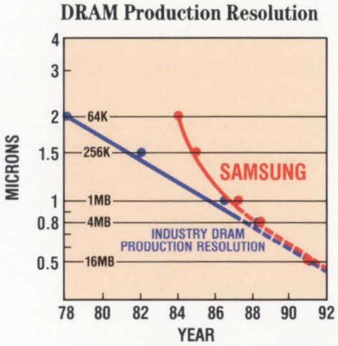
Samsung now offers every major DRAM part type.

We're not stopping at 1-million bits. Our 4MB DRAM development program is right on track. Engineering samples will be available early next year.

Samsung DRAM Development



DRAM Production Resolution



Samsung DRAMs are available in the most effective size, speed and organization combinations. Scan the chart below to find the right DRAMs for your applications.

You can see from the picture that we package our DRAMs the way you want them: DIP, PLCC, SIP/SIMM and ZIP.* If you're looking for state-of-the-art, check out our 256 x 8 (or x 9) SIP and SIMM memory modules.

We have the technology, we have an aggressive memory development program in place and we have the memory products to meet your requirements, available now. Samsung is committed to being your memory supplier. Call your nearest Samsung sales office for samples and data sheets, today. ■

*Q3

CIRCLE NO. **166**

DRAMs

Density	64K	256K	256K	1 Mb	1 Mb
Organization	64Kx1	256Kx1	64Kx4	1Mx1	256Kx4
Availability	Now	Now	Now	Q3'87	Q3'87
Technology	NMOS	NMOS	NMOS	CMOS	CMOS
Package	DIP	DIP, PLCC, SIP/SIMM, ZIP*	DIP, PLCC, SIP/SIMM, ZIP*	SOJ, SIP/SIMM, ZIP	SOJ, SIP/SIMM, ZIP
Speed	150 ns, 200 ns	120 ns, 150 ns	120 ns, 150 ns	80 ns, 100 ns, 120 ns	80 ns, 100 ns, 120 ns
Mode	Page	Page, Nibble	Page	Static Column Page, Nibble	Page

*Q3 '87

EEPROMs

Samsung 16K and 64K EEPROMs meet or exceed industry standards. Endurance is rated at 10,000 erase/write cycles. Data retention ratings are 10 years for our entire line. Moreover, our pin-out permits you to upgrade EEPROMs without re-designing your entire PCB. Most importantly, our EEPROMs are immediately available.

When it comes to EEPROMs, we deliver.

We offer industrial temperature operating range ($-40°$ to $+85°C$) and high performance 64K KM2864AH and KM2865AH EEPROMs. They feature write cycle times that are five times faster than standard parts.

Samsung is known for reliability, quality and performance. And nobody beats our EEPROM prices. See for yourself. Call your Samsung sales office to get our EEPROM reliability report, data sheets or samples. ■

CIRCLE NO. **167**

EEPROMs

Density	16K	16K	64K	64K	64K	64K
Part Number	KM2816A	KM2817A	KM2864A	KM2864AH	KM2865A	KM2865AH
Availability	Now	Now	Now	Now	Now	Now
Package	24 Pin Plastic DIP	28 Pin Plastic DIP	28 Pin Plastic DIP	28 Pin Plastic DIP	28 Pin Plastic DIP	28 Pin Plastic DIP
Speed	250 ns, 300 ns, 350 ns	250 ns, 300 ns, 350 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns	200 ns, 250 ns, 300 ns
Endurance	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles	10,000 Erase/Write Cycles
End of Write Scheme		RDY/$\overline{BSY}$	$\overline{\text{Data}}$ Polling	$\overline{\text{Data}}$ Polling	RDY/$\overline{BSY}$, Data Polling	RDY/$\overline{BSY}$, Data Polling
Byte Write Time	10 ms write/byte	10 ms write/byte	10 ms write/byte	2 ms write/byte	10 ms write/byte	2 ms write/byte

SRAMs

Samsung is making the same commitment to SRAMs that we make to all our memory products. Samsung is increasing Static RAM production rather than cutting back the way some other manufacturers are. And we are expanding our SRAM line as we develop the next generation 256K and fast 64K CMOS Static RAMs. Check our offerings in the chart below. Then call your Samsung sales office for samples and data sheets. Make Samsung your quality SRAM supplier. ■

CIRCLE NO. **168**

SRAMs

Density	64K	64K	64K	64K
Part Number	KM6264-12	KM6264-15	KM6264L-12	KM6264L-15
Organization	8Kx8	8Kx8	8Kx8	8Kx8
Availability	Q4	Now	Q4	Now
Technology	MIX-MOS	MIX-MOS	MIX-MOS	MIX-MOS
Package	28 Pin DIP	28 Pin DIP	28 Pin DIP	28 Pin DIP
Speed	120 ns	150 ns	120 ns	150 ns
Standby Current	1mA Max.	1mA Max.	100 μA Max.	100 μA Max.

Samsung's 54/74 AHCT and 54/74 HCTLS CMOS Logic gives you the most comprehensive selection of LS, ALS and FAST™ replacements. 61 parts now-86 more in Q3.

Replace LS, ALS and FAST with AHCT and HCTLS CMOS logic parts from Samsung—right now. Look at the advantages we can offer you. And at prices comparable to bipolar!

Comparison of Key Parameters for a 244 Octal Buffer

	74AHCT	74HCTLS	74ALS	74LS	74ACT*
Max Propagation Delay (C_L = 50pF)	10ns	18ns	10ns	18ns	13.5ns
Drive Current, I_{OL}	24mA	24mA	24mA	24mA	24mA
Power Dissipation (at 100KHz)	0.6mW	0.6mW	70mW	120mW	1mW

*Fairchild FACT™

You get low power, wide operating supply and temperature ranges, superior noise immunity, rail-to-rail output voltage swings and the low input currents of CMOS, combined with the high speed and drive capability of bipolar.

Unlike older performance-limited HC and HCT logic families, Samsung's high performance CMOS logic matches bipolar speed and drive. 24 mA is guaranteed. Moreover, our CMOS logic allows you to interface directly with all types of TTL, NMOS and CMOS circuitry.

Compare the power dissipation of Samsung's AHCT/HCTLS logic to bipolar LS/ALS/FAST. Our logic consumes 100,000 times less power at low frequencies and 10 times less power at 10 MHz. CMOS voltage swings also give you up to three times the noise immunity.

Ask us and we'll send you two free samples each of up to five part types. Just call your local Samsung sales office and specify AHCT or HCTLS with your part number. Use this list to order your samples and to see what's coming later this year. Take advantage of Samsung's cool running, highly reliable, high performance CMOS logic.

Order your free samples today.

(continued on next page)

CIRCLE NO. **169**

FAST is a trademark of Fairchild Semiconductor Corp.

For product information call your local Samsung sales office.

SAMSUNG SAYS SO.

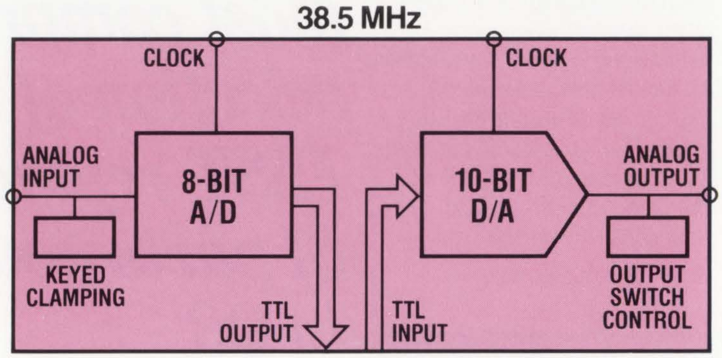
Flash Converter features independent 8-bit A to D and 10-bit D to A functions on a single chip.

The new KSV3100A flash converter is the latest and most impressive addition to Samsung's extensive line of linear products. The monolithic KSV3100A provides independent 8-bit flash A/D converter and 10-bit R-2R D/A converter functions over an operating range of DC to 38.5 MHz.

The single-chip architecture of the KSV3100A allows you to design-in with a single board rather than many. This saves real estate and gives you room to add more features to your system. Using fewer parts also raises the reliability of your system.

Samsung has designed a number of useful features into our new flash converter. You can choose between selectable peak level or keyed clamping. And the device's absolute non-linearity is rated at 1 per cent.

We also provide you with the support chips you need. Our KA2606 Sync Separate IC, KA2153 Chrominance Signal Processor for NTSC systems, and KA2154 Video Chroma Deflection System for NTSC and PAL systems make it easy to integrate the KSV3100A into your video applications.



Samsung's flash converter prices are unbeatable. The chart shows our 100 piece KSV3100A Flash Converter prices:

KSV3100 AN – 10	$48.90	KSV3100 AN – 8	$24.45
KSV3100 AN – 9	$32.60	KSV3100 AN – 7	$14.67

CIRCLE NO. **170**

SOT-23s

Samsung has the SOT-23s you're looking for: industry standard NPN and PNP epitaxial transistors implemented in the internationally standardized micro-package.

Samsung SOT-23s are ideal for both hybrid and surface mounting. Our SOT-23 micro-packaging saves real estate, slashes costs and boosts system reliability.

We also offer a broad range of TR products: industry standard TIP-series power transistors, high-speed high-voltage switching power transistors, power Darlington transistors and our TO-3P silicon mesa transistors—they're rated at 1500 Volts!

Call your Samsung sales office for our SOT-23s or New Transistor data book.

CIRCLE NO. **171**

LINEAR ICs

Samsung offers a full line of linear products, in addition to converters, including: amplifiers, timers, regulators, comparators, telephone ICs, power amplifiers and a number of other ICs.

Samsung's entire line of standard parts is now available in production quantities. A number of our key linear offerings are listed below:

Data Conversion

KS7126	3½ Digit CMOS A/D Converter
KS25C02	8 bit CMOS Successive Approx. Register
KS25C03	8 bit CMOS Successive Approx. Register
KS25C04	**12 bit CMOS Successive Approx. Register**

Voltage Regulators: MC78xx, MC78Mxx, MC78Lxx, MC79xx, MC79Mxx, LM317T, **μA78S40**

Op Amps: LM741, MC1458, MC4558, LM358/A, LM348, LM324/A, MC3403

Timers: **KS555 (CMOS)**, NE555, NE556, NE558

Comparators: LM311, LM393/A, LM339/A

Tone Decoder: LM567, LM567L (Micropower)

Interface: MC1488, MC1489/A

Telephone

KA2410	Tone Ringer
KA2411	Tone Ringer
KA2412A	Speech Network
KA2420	**Speaker Phone**
KA2413	DTMF
KS5808	DTMF
KS5805A/B	Pulse Dialer

Others

KS5803A/B	IR Transmitter
KA2181	IR Preamplifier
KA2182	IR Preamplifier
KA2183	IR Preamplifier
MC3361	FM IF Amplifier
KA2803	Ground Fault Detector
KA2084	Zero Voltage Switch
LM386	**Audio Power Amplifier**

Call your local Samsung sales representative for a Data Book that includes our Cross Reference Guide and samples.

CIRCLE NO. **172**

CMOS LOGIC *(Continued)*

KS/74AHCT & KS/74HCTLS Part Types

Gates & Inverters	00, 01, 02, 03, 04, 05, 08, 09, 10, 11, 12, 14*, 20*, 21*, 22*, 27*, 32, 51*, 58*, 86, 132*, 133*, 266
Buffers & Line Drivers	125*, 126*, 210, 240, 241, 244, 365, 366, 367, 368, 465*, 466*, 467*, 468*, 540, 541
Flip-Flops	73*, 74, 76*, 78*, 107, 109, 112, 173*, 174, 175, 273, 374, 377*, 399*, 534, 564, 574, 670*, 794*, 821*, 822*, 823*, 824*, 825*, 826*
Latches	259*, 373, 533, 563, 573, 793*, 841*, 842*, 843*, 844*
Transceivers/Registered Transceivers	242*, 243*, 245, 640, 643, 645, 646, 648, 651*, 652*, 658*, 659*, 664*, 665*
Counters	160, 161, 162, 163, 168*, 169*, 191*, 193*, 390*, 393, 590*, 591*, 592*, 593*
Decoders/Encoders	42*, 138, 139, 148*, 154*, 155*, 238, 239
Multivibrators	121*, 123*, 423*
Multiplexers	151*, 153*, 157, 158, 251*, 253*, 257, 258, 352*, 353*
Shift Registers	164, 165*, 166, 194*, 195*, 299*, 595*, 596*, 597*
Arithmetic Circuits	280*, 518*, 519*, 520*, 521*, 522*, 679*, 680*, 682*, 684*, 686*, 688*, 689*

*Part Types Available in Q3—All Other Part Types Available Now.

CIRCLE NO. **169**

SALES OFFICES

AL	EMA	(205) 536-3044
AZ	Haas & Associate, Inc.	(602) 994-3813
CA	Quest-Rep	(619) 546-1933
CA	Samsung Semiconductor	(408) 727-7433
CA	Samsung Semiconductor	(714) 662-3406
CA	SYNPAC	(408) 988-6988
CA	Westar	(714) 835-4711
CO	Electrodyne	(303) 695-8903
CT	Phoenix Sales	(203) 438-9644
FL	Lawrence Associates	(305) 368-7373
		(813) 584-8110
		(305) 339-3855
GA	EMA	(404) 448-1215
IL	IRI	(312) 967-8430
IL	Samsung Semiconductor	(312) 310-9780
IN	STB	(317) 844-9227
MA	Samsung Semiconductor	(617) 273-4888
MA	Tech Comp	(617) 449-7928
MD	ATS	(301) 789-9360
MI	C.B. Jensen	(313) 643-0506
MN	IEI	(612) 571-0000
NC	EMA	(919) 847-8800
NJ	NECCO	(201) 461-2789
NM	Nelco Electronix	(505) 292-3657
NY	Reagan-Compar	(518) 489-4777
		(716) 271-2230
		(607) 723-8743
		(315) 732-3775
OH	J.N. Bailey	(513) 687-1325
		(216) 273-3798
		(614) 262-7274
OR	Earl & Brown	(503) 245-2283
PA	RJI	(215) 631-1414
SC	EMA	(803) 233-4637
TX	Samsung Semiconductor	(214) 239-0754
TX	Vielock	(214) 881-1940
UT	Electrodyne	(801) 486-3801
WA	Earl & Brown	(206) 885-5064
WI	IRI	(414) 259-0965
CANADA	GNT	(604) 430-6677
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Semiconductor
3725 N. First Street
San Jose, CA 95134-1708
(800) 423-8624

EDN TECHNICAL-ARTICLE DATABASE

In-circuit emulators/emulation

ICE makers grapple with 32-bit microprocessors. *Goering, Richard, Staff Editor; Computer Design, 12/86, pg 46, 2 pgs.*

Inductors

Magnetic materials provide the final piece to the high-frequency switching-supply puzzle. *Small, Charles H, Associate Editor; EDN, 03/04/87, pg 79, 2.33 pgs.*

Industrial electronics

1987 U.S. market report: Industrial. *Staff; Electronics, 01/08/87, pg 66, 2 pgs.*

Personal computers march into the factory. *Dixon, Tom, Staff Editor; Electronic Products, 02/15/87, pg 36, 5.5 pgs.*

Inspection

Moving wafer inspection into the fast lane. *Lyman, Jerry, Staff Editor; Electronics, 03/05/87, pg 74, 3 pgs.*

Quality and reliability screens impact the cost of owning ICs. *Denton, Donald L, Texas Instruments; Electronic Design, 11/20/86, pg 105, 4.5 pgs.*

Instrument interface systems

Card-based ATE system could set a standard. *Sideris, George, Staff Editor; Electronics, 04/16/87, pg 60, 3 pgs.*

How DOD is creating a major new business. *Sideris, George, Staff Editor; Electronics, 04/16/87, pg 57, 3 pgs.*

Instrumentation amps

Instrumentation amp suits wide range of circuit designs. *Burt, Rod, Burr-Brown Corp; EDN, 01/08/87, pg 157, 7 pgs.*

Instrumentation/design aids & services/measurement, other

1987 U.S. market report: Test & measurement. *Staff; Electronics, 01/08/87, pg 61, 3 pgs.*

A bargain in board tester virtuosity. *Hall, John, Summation; Electronic Products, 03/15/87, pg 34, 6.5 pgs.*

A new tool dramatically cuts VLSI debugging time. *McLeod, Jonah, Staff Editor; Electronics, 04/30/87, pg 51, 3 pgs.*

ASIC-verification systems speed prototype testing, but system capabilities vary. *Everett, Chris, Regional Editor; EDN, 11/27/86, pg 51, 8 pgs.*

Affordable image scanners and software simplify the design of imaging systems. *Wright, Maury, Regional Editor; EDN, 03/31/87, pg 75, 6 pgs.*

Analog scopes automate bench test measurements. *Engholm Sunderman, Kathy, Tektronix; Electronic Design, 11/27/86, pg 119, 3 pgs.*

Built-in testability helps to clear some stubborn IC bottlenecks. *Seaton, John; Chu, Louis, Tangent Systems; Electronic Design, 11/27/86, pg 101, 4 pgs.*

Calibrators move to automation to cope with new demands. *Tunick, Diane, Staff Editor; Electronic Design, 03/87, pg 49, 6 pgs.*

Expert designers evaluate PC-based schematic editors. *Freeman, Eva, Associate Editor; EDN, 12/25/86, pg 82, 4.5 pgs.*

Fiber-optic testers determine faults in short-haul networks. *Conner, Margery S, Regional Editor; EDN, 12/25/86, pg 98, 6 pgs.*

IEEE 802.3 LAN testers and analyzers pinpoint network and equipment flaws. *Leibson, Steven H, Regional Editor; EDN, 04/30/87, pg 59, 6 pgs.*

Low-cost IC testers add features. *Yates, Warren, Staff Editor; Electronic Products, 02/01/87, pg 24, 5 pgs.*

Traditional products get squeezed by newer gear. *Sideris, George, Staff Editor; Electronics, 02/05/87, pg 89, 5 pgs.*

Use an interchange format to port component libraries. *Waters, Mike, et al, Motorola; EDN, 02/05/87, pg 175, 7 pgs.*

Integrated circuits/semiconductor devices/circuit design, other

1987 U.S. market report: Semiconductors. *Staff; Electronics, 01/08/87, pg 68, 4 pgs.*

A new wave rises on the Pacific Rim. *Berger, Michael, Staff Editor; Shapiro, Don, Staff Editor; Electronics, 04/02/87, pg 78, 2 pgs.*

A one-world industry is arriving fast. *Erikson, Arthur, Staff Editor; Electronics, 04/02/87, pg 69, 4 pgs.*

A swarm of RISC chips is chasing a fast-growing systems market. *Barney, Clifford, Staff Editor; Electronics, 03/19/87, pg 66, 1 pg.*

Accurate, high-speed analog multipliers promise greater use of analog techniques. *Fleming, Tarlton, Associate Editor; EDN, 02/19/87, pg 57, 5.33 pgs.*

Advances in CMOS and ECL process technology yield powerhouse ICs. *Marrin, Ken, Staff Editor; Computer Design, 12/86, pg 81, 9.5 pgs.*

Analog-IC arrays can field board-level circuitry. *Moore, Bruce D, Raytheon, Semiconductor Division; Electronic Products, 02/01/87, pg 43, 3 pgs.*

Bipolar and MOS beware: BMFET has speed, power edge. *Beedie, Mitch, Staff Editor; Electronic Design, 11/13/86, pg 35, 0.5 pgs.*

Chip-on-board technology chugs along. *Chin, Spencer, Staff Editor; Electronic Products, 03/01/87, pg 37, 3.5 pgs.*

Consider how TTL outputs work during power-downs. *Taylor, Mark A, Hewlett-Packard Co; EDN, 11/27/86, pg 221, 3 pgs.*

Cost, device speed, size, and reliability determine the best package for an ASIC. *Freeman, Eva, Associate Editor; EDN, 04/30/87, pg 77, 5 pgs.*

Design-for-test techniques suit diverse applications. *Hess, Robert D, et al, Caedent Corp; EDN, 04/15/87, pg 189, 4.5 pgs.*

Designing a state machine with a programmable sequencer. *Lee, Frank, Monolithic Memories; Electronic Products, 02/01/87, pg 29, 7 pgs.*

Don't write off wafer-scale work: It's still going strong. *Cole, Bernard C, Staff Editor; Electronics, 01/08/87, pg 94, 2 pgs.*

Europe pushes hard for global role. *Gosch, John, Staff Editor; Electronics, 04/02/87, pg 75, 1.5 pgs.*

Fuzzy logic allows creation of precise process controllers. *Guilamo, Pedro J, Bailey Controls Co; EDN, 04/15/87, pg 201, 3.5 pgs.*

Hardware methods improve 1-chip A/D converters. *Sidman, Steven, Harris; EDN, 02/05/87, pg 139, 13.5 pgs.*

Here comes the billion-transistor IC. *Cole, Bernard C, Staff Editor; Electronics, 04/02/87, pg 81, 5 pgs.*

How linear IC designers are building denser chips. *Cole, Bernard Conrad, Staff Editor; Electronics, 12/18/86, pg 67, 4 pgs.*

ISSCC: Analog. *Goodenough, Frank, Staff Editor; Electronic Design, 03/05/87, pg 71, 4 pgs.*

ISSCC: Digital. *Bursky, Dave, Staff Editor; Electronic Design, 03/05/87, pg 61, 4.5 pgs.*

ISSCC: Special purpose. *Allan, Roger, Staff Editor; Electronic Design, 03/05/87, pg 79, 3 pgs.*

Inova brings wafer-scale integration to market. *Cole, Bernard C, Staff Editor; Electronics, 01/08/87, pg 91, 3 pgs.*

Interface various IC technologies to CMOS arrays. *Stansberry, Mark, National Semiconductor Corp; EDN, 03/04/87, pg 153, 4 pgs.*

Japan drives for strategic alliances. *Cohen, Charles L, Staff Editor; Electronics, 04/02/87, pg 76, 2 pgs.*

LAN ICs for IEEE-802 networks. *Wiegand, Jim, Associate Editor; EDN, 04/30/87, pg 131, 8.5 pgs.*

Magnetic compensation gives new life to transformer-based SLICs. *Stacey, Chris, National Semiconductor Corp; EDN, 04/30/87, pg 149, 5 pgs.*

Micromachining shapes solid-state sensors and actuators for the digital era. *Allan, Roger, Staff Editor; Electronic Design, 11/13/86, pg 71, 9 pgs.*

Microprogrammable processing. *Leibson, Steven H, Regional Editor; EDN, 04/15/87, pg 143, 13 pgs.*

Mixed analog/digital technologies pack complete systems on-chip. *Martin, Steven L, Contributing Editor; Computer Design, 04/01/87, pg 39, 6 pgs.*

Power op amps solve deflection-yoke drive problems. *Scofield, Granger, Apex Microtechnology Corp; EDN, 02/19/87, pg 171, 6 pgs.*

Programmable-logic devices. *Small, Charles H, Associate Editor; EDN, 02/05/87, pg 112, 17 pgs.*

Record-setting CPUs, DRAMs, and SRAMs star at ISSCC. *Cole, Bernard C, Staff Editor; Electronics, 03/05/87, pg 58, 9 pgs.*

Reports from the PLD front. *Collett, Ron, Staff Editor; Digital Design, 02/87, pg 46, 5.5 pgs.*

Scan-path tools speed the conversion of your design into a testable chip. *Everett, Chris, Regional Editor; EDN, 03/04/87, pg 67, 5.33 pgs.*

Silicon-on-insulator gets easier. *Cole, Bernard C, Staff Editor; Electronics, 12/18/86, pg 32, 0.5 pgs.*

Synchronous VFC enhances accuracy in analog-input systems. *DeVito, Larry, Analog Devices Semiconductor; EDN, 11/13/86, pg 269, 9.5 pgs.*

Synchronous-network circuit boosts network flexibility. *Vesuna, Sarosh N, Advanced Micro Devices; EDN, 11/13/86, pg 231, 6 pgs.*

TI process boosts linear CMOS ICs to LSI densities. *Staff; Electronics, 12/18/86, pg 71, 3 pgs.*

The look of the industry in 2000. *Weber, Samuel, Staff Editor; Electronics, 04/02/87, pg 60, 2 pgs.*

EDN TECHNICAL-ARTICLE DATABASE

Thermal-tracking IC converts rms to dc. *Williams, Jim, Linear Technology Corp; EDN, 02/19/87, pg 137, 15 pgs.*
This bipolar process gives density and dynamic range. *Cole, Bernard C, Staff Editor; Electronics, 04/16/87, pg 69, 3 pgs.*
Use of check list prevents problems in TTL systems. *Sokal, Nathan O, Design Automation Inc; EDN, 11/13/86, pg 253, 8 pgs.*
Use structured arrays for high-performance data processing. *Chang, Yen, LSI Logic Corp; EDN, 04/15/87, pg 177, 6 pgs.*
VHSIC finally builds a head of steam. *Waller, Larry, Staff Editor; Electronics, 04/16/87, pg 84, 3 pgs.*
VHSIC moves headlong into the submicron stage. *Lyman, Jerry, Staff Editor; Electronics, 04/16/87, pg 91, 3 pgs.*
Winds of change sweep the industry. *Barney, Clifford, Staff Editor; Electronics, 04/02/87, pg 62, 6 pgs.*

Interconnection systems
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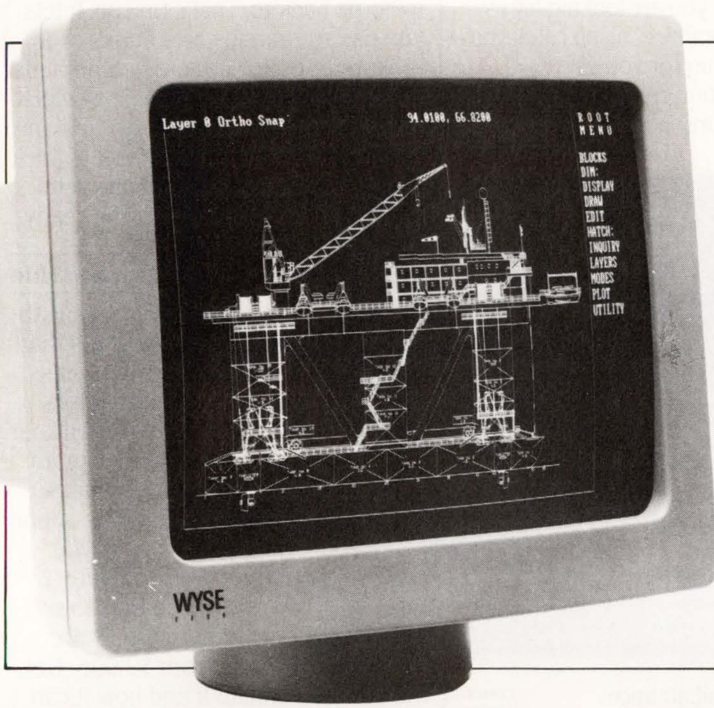

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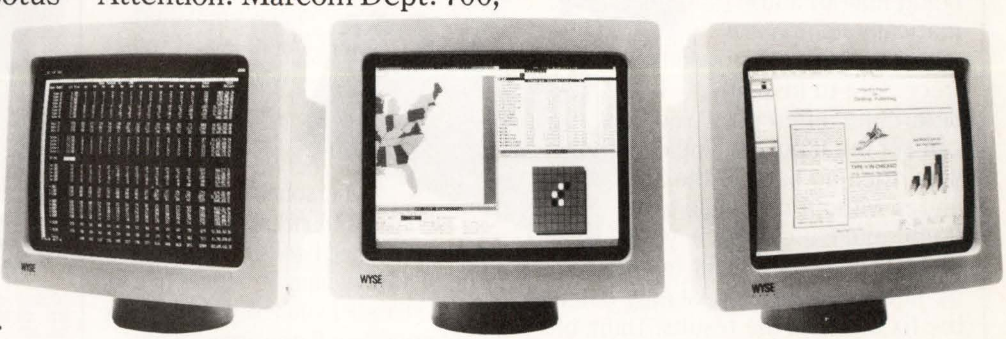

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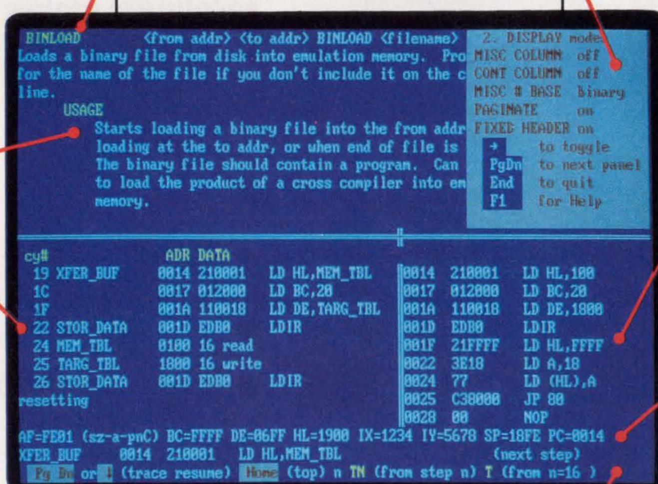

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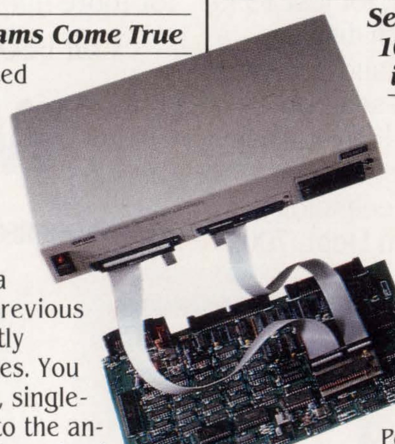

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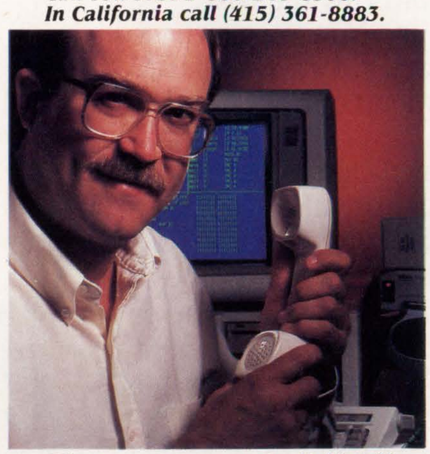

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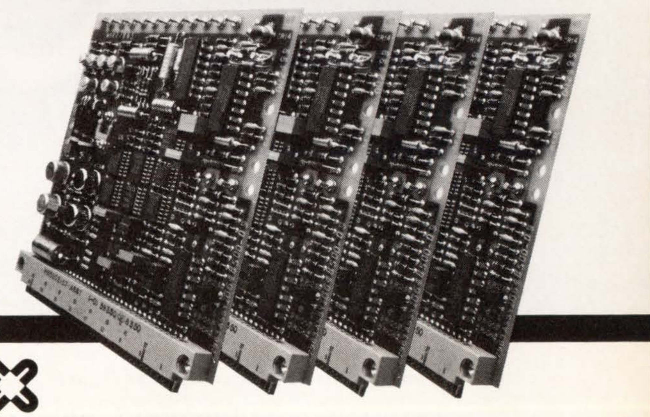

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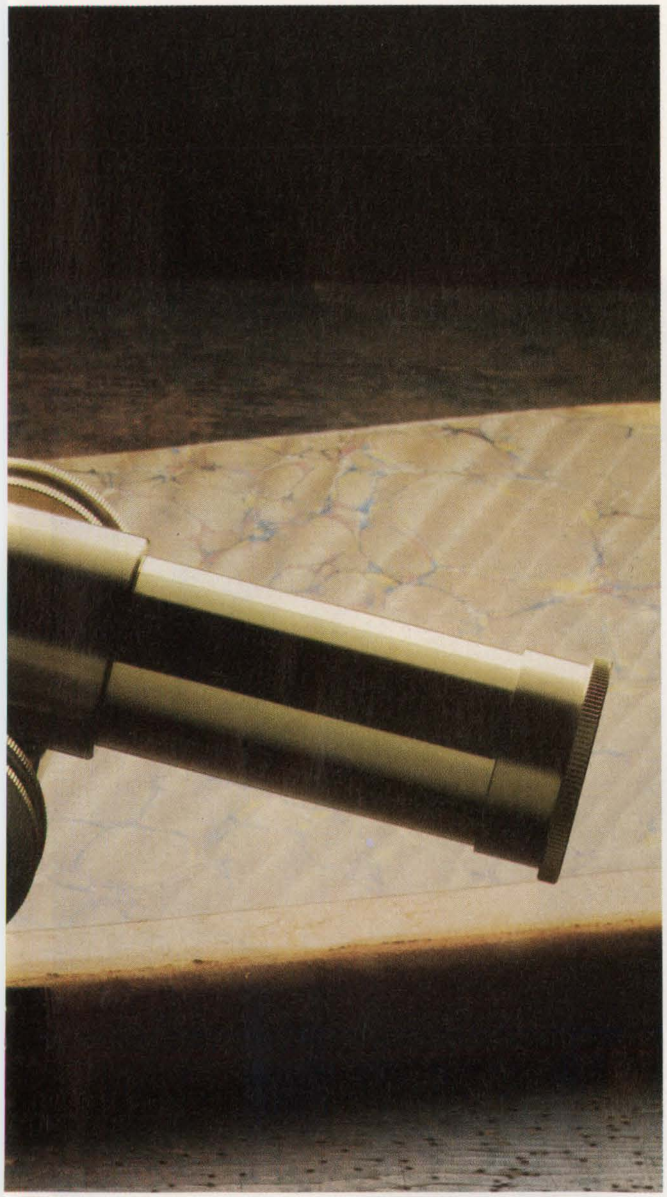

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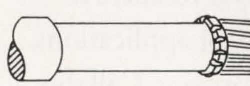

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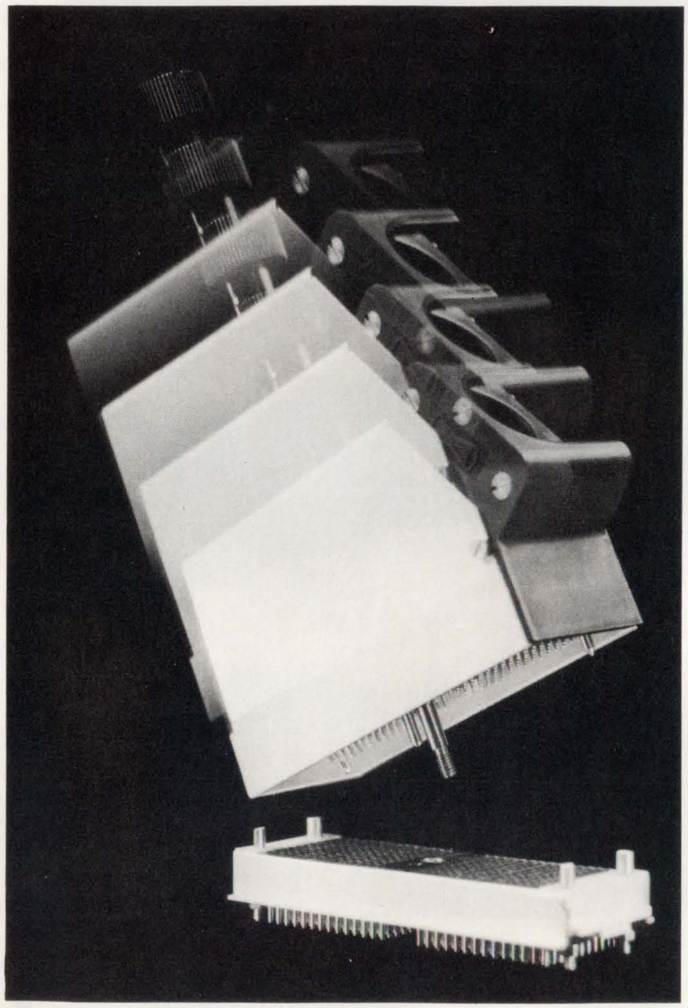

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Motorola grabs lead in ECL density, using Mosaic III. *Cole, Bernard C, Staff Editor; Electronics, 02/19/87, pg 71, 3 pgs.*

PLDs provide fast lane to semicustom designs. *Martin, Steven L, Contributing Editor; Computer Design, 03/01/87, pg 28, 6.5 pgs.*

Parameterizable cells strike middle ground between fixed and compiled cells. *Bloom, Michael, Contributing Editor; Computer Design, 11/01/86, pg 24, 5.5 pgs.*

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EDN DATABASE

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Applications determine architectures for imaging. *Wilson, Andrew C, Staff Editor; Digital Design, 04/87, pg 51, 3 pgs.*

High-powered desktop image processing gets closer. *Staff; Electronics, 02/19/87, pg 62, 3 pgs.*

How long will it take image processing to blast off? *Lineback, J Robert, Staff Editor; Electronics, 02/19/87, pg 65, 2 pgs.*

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Solid state sensors capture bigger images. *Wilson, Andrew C, Staff Editor; Digital Design, 12/86, pg 43, 2 pgs.*

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Power planes increase wire-wrapped circuit speeds. *Visco, P Anthony, Mupac Corp; EDN, 11/27/86, pg 225, 3 pgs.*

DESIGN NOTES

Number 1 in a series from Linear Technology Corporation August, 1987

New Data Acquisition Systems Communicate with Microprocessors Over 4 Wires

As board space and semiconductor package pins become more valuable, serial data transfer methods between microprocessors (MPUs) and their peripherals become more and more attractive. Not only does this save lines in the transmission medium, but, because of the savings in package pins, more function can be packed into both the MPU and the peripheral. Users are increasingly able to take advantage of these savings as more MPU manufacturers develop serial ports for their products[1–3]. However, peripherals which are able to communicate with these MPUs must be available in order for users to take full advantage. Also, MPU serial formats are not standardized so not all peripherals can talk to all MPUs.

The LTC1090 Family

A new family of 10-bit data acquisition circuits has been developed to communicate over just 4 wires to the recently developed MPU synchronous serial formats as well as to MPUs which do not have serial ports. These circuits feature software configurable analog circuitry including analog multiplexers, sample and holds, bipolar and unipolar conversion modes. They also have serial ports which can be software configured to communicate with virtually any MPU. Even the lowest grade device features guaranteed ±0.5LSB linearity over the full operating temperature range. Reduced span operation (down to 200mV), accuracy over a wide temperature range and low power single supply operation make it possible to locate these circuits near remote sensors and transmit digital data back through noisy media to the MPU. Figure 1 shows a typical hookup of the LTC1090 , the first member of this data acquisition family. For more detail, refer to the 24-page LTC1090 data sheet.

Included are eight analog inputs which can common-mode to both supply rails. Each can be configured for unipolar or bipolar conversions and for single-ended or differential inputs by sending a data input (D_{IN}) word from the MPU to the LTC1090 (Figure 1).

Both the power supplies are bypassed to analog ground. The V^- supply allows the device to operate with inputs which swing below ground. In single supply applications it can be tied to ground.

The span of the A/D converter is set by the reference inputs which, in this case, are driven by a 2.5V LT1009 which gives an LSB step size of 2.5mV. However, any reference voltage within the power supply range can be used.

The 4 wire serial interface consists of an active low chip select pin ($\overline{CS}$), a shift clock (SCLK) for synchronizing the data bits, a data input (D_{IN}) and a data output (D_{OUT}). Data is transmitted and received simultaneously (full duplex), minimizing the transfer time required.

The external ACLK input controls the conversion rate and can be tied to SCLK as in Figure 1. Alternatively, it can be derived from the MPU system clock (e.g., the 8051 ALE pin) or run asynchronously. When the ACLK pin is driven at 2MHz, the conversion time is 22μs.

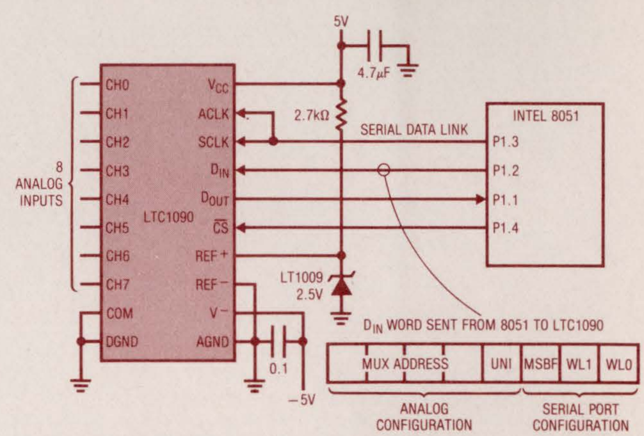

Figure 1. A Typical Hookup of the LTC1090

Advantages of Serial Communications

The LTC1090 can be located near the sensors and serial data can be transmitted back from remote locations through isolation barriers or through noisy media.

Several LTC1090s can share the serial interface and many channels of analog data can be digitized and sent over just a few digital lines (see Figure 2). This could, for example, be used to simplify the communications between an instrument and its front panel.

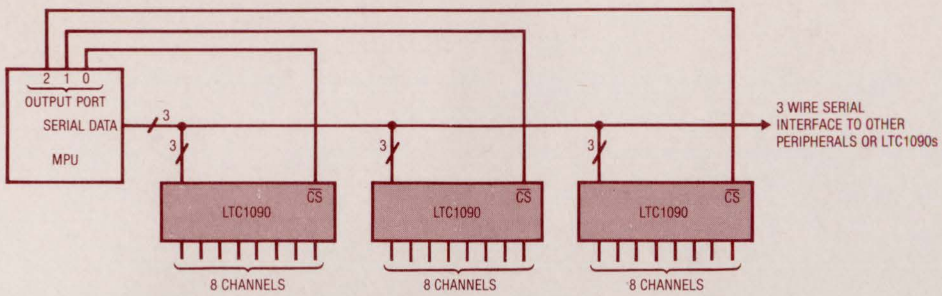

Figure 2. Several LTC1090s Sharing One 3 Wire Serial Interface

Using fewer pins for communication makes it possible to pack more function into a smaller package. LTC1090 family members are complete systems being offered in packages ranging from 20 pins to 8 pins (e.g., LTC1091).

Speed is Usually Limited by the MPU

A perceived disadvantage of the serial approach is speed. However, the LTC1090 can transfer a 10-bit A/D result in 10μs when clocked at its maximum rate of 1MHz. With the minimum conversion time of 22μs, throughput rates of 30kHz are possible. In practice, the serial transfer rate is usually limited by the MPU, not the LTC1090. Even so, throughput rates of 20kHz are not uncommon when serial port MPUs are used. For MPUs without serial ports, the transfer time is somewhat longer because the serial signals are generated with software. For example, with the Intel 8051 running at 12MHz, a complete transfer takes 80μs. This makes possible throughput rates of approximately 10kHz.

Talking to Serial Port MPUs

By accommodating a wide variety of transfer protocols, the LTC1090 is able to talk directly to almost all synchronous serial formats. The last 3 bits of the LTC1090 data input (D_{IN}) word define the serial format. The MSBF bit determines the sequence in which the A/D conversion result is sent to the processor (MSB or LSB first). The two bits WL1 and WL0 define the word length of the LTC1090 data output word. Figure 3 shows several popular serial formats and the appropriate D_{IN} word for each. Typically a complete data transfer cycle takes only about 15 lines of processor code.

Talking to MPUs without Serial Ports

The LTC1090 talks to serial port processors but works equally well with MPUs which do not have serial ports. In these cases, $\overline{CS}$, SCLK and D_{IN} are generated with software on 3 port lines. D_{OUT} is read on a fourth. Figure 3 shows the appropriate D_{IN} word for communicating with MPU parallel ports. Figure 1 shows a 4 wire interface to the popular Intel 8051. A complete transfer takes only 33 lines of code.

Sharing the Serial Interface

No matter what processor is used, the serial port can be shared by several LTC1090s or other peripherals (see Figure 2). A separate $\overline{CS}$ line for each peripheral determines which is being addressed.

Conclusions

The LTC1090 family provides data acquisition systems which communicate via a simple 4 wire serial interface to virtually any microprocessor. By eliminating the parallel data bus they are able to provide more function in smaller packages, right down to 8 pin DIPs. Because of the serial approach, remote location of the A/D circuitry is possible and digital transmission through noisy media or isolation boundaries is made easier without a great loss in speed.

Hardware and software is available from the factory to interface the LTC1090 to most popular MPUs. The LTC1090 data sheet contains source code for several microprocessors. Further applications assistance is available by calling the factory.

LTC1090 D_{IN} Word

Type of Interface	LTC1090 Data Format	Analog Configuration					MSBF	WL1	WL0
All Parallel Port MPUs	MSB First 10 Bits	X	X	X	X	X	1	0	1
National MICROWIRE*	MSB First 12 Bits	X	X	X	X	X	1	1	0
MICROWIRE/PLUS* Motorola SPI	MSB First 16 Bits	X	X	X	X	X	1	1	1
Hitachi Synchronous SCI TI TMS7000 Serial Port	LSB First 16 Bits	X	X	X	X	X	0	1	1

Figure 3. The LTC1090 Accommodates Both Parallel and Serial Ports

*MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corp.

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For LTC1090 literature call **800-637-5545.** For help with an application call (408) 432-1900, Ext. 361.

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EDITED BY TARLTON FLEMING

Add balanced signal to a variable voltage

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To provide pulse-width modulation of a control variable, some process-control circuits add a triangular waveform to the control-variable voltage. (The low signal frequencies of these circuits precludes the use of ac-coupling capacitors.) By first considering a conventional way of combining the sawtooth and control voltages **(Fig 1)**, you'll better appreciate the circuit of **Fig 2**, in which the oscillator's dc component continuously tracks the input voltage.

Output V_3 in this traditional circuit is

$$V_3=\left(\frac{R_2}{R_1+R_2}\right)V_1+\left(\frac{R_1}{R_1+R_2}\right)V_2,$$

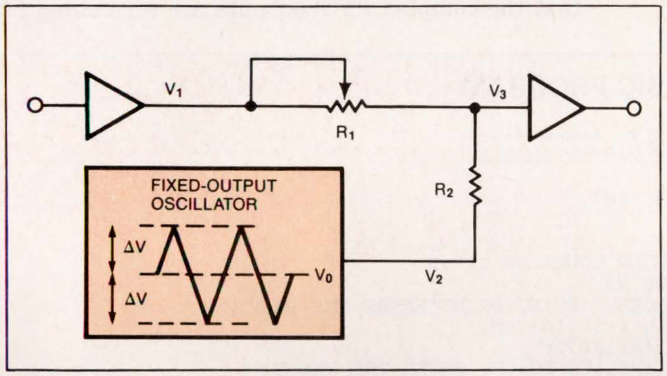

Fig 1—In this circuit, *which is similar to* ***Fig 2*** *except that the oscillator output is fixed, the sawtooth's dc component creates an offset error in V_3.*

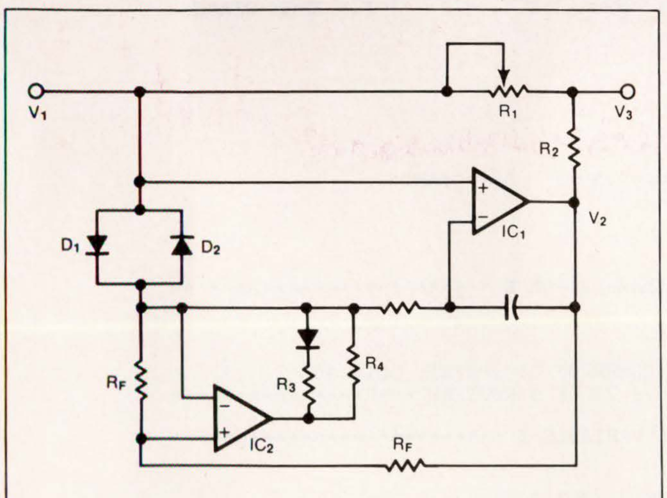

Fig 2—This circuit combines the input voltage V_1 *with a sawtooth waveform in which the sawtooth's dc component matches and tracks V_1.*

where V_1 is the control variable (a slowly varying dc signal), and V_2 is the sawtooth-oscillator output $V_0 \pm \Delta V$. The dc component of V_3 is

$$V_{3(DC)}=\left(\frac{R_2}{R_1+R_2}\right)V_1+\left(\frac{R_1}{R_1+R_2}\right)V_0.$$

You can see that the oscillator's fixed dc component, V_0, contributes an offset-error term that varies as you adjust R_1. Because this offset error affects V_3, it appears in the system as a change in the control variable V_1. This spurious change in V_3 can be significant: As R_1 varies from zero to full value, the shift is

$$V_{3(DC)}=\frac{R_1}{R_1+R_2}\left(V_1-V_0\right).$$

As an added drawback, you have to provide compensation for the signal attenuation of the resistors.

In **Fig 2,** the oscillator's dc component V_0 tracks the input V_1, thereby eliminating the offset error in V_3. Comparator IC_2 changes state each time V_2 differs from V_1 by more than one diode drop, creating a linear sawtooth waveform V_2 at the output of integrator IC_1:

$$V_2=V_1 \pm V_D+\frac{1}{2}\Delta V_D,$$

where V_D is the average forward-voltage drop for diodes D_1 and D_2 ($\frac{1}{2}(V_{D1}+V_{D2})$), and ΔV_D is the mismatch in diode drops.

Output V_3 still has an error component caused by ΔV_D:

$$V_3=V_1+\left(\frac{R_1}{R_1+R_2}\right)V_D+\frac{1}{2}\left(\frac{R_1}{R_1+R_2}\right)\Delta V_D.$$

To minimize this error, you must select diodes with a narrow spread of forward voltages. Rectifier diodes such as 1N4000s are well suited to this purpose; they have a typical spread of 20 mV at 1 mA. To further minimize error, you must select the resistor values of R_3 and R_4 to produce equal current in the diodes D_1 and D_2 over V_1's anticipated range; that is, the current in D_2 when the comparator output is high should equal the current in D_1 when the comparator is low. **EDN**

To Vote For This Design, Circle No 746

Program aids analysis of FFT algorithms

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When engineers use standard software routines or hardware devices to perform FFTs, they're mainly concerned with providing the proper inputs and correctly interpreting the outputs. When developing nonstandard FFTs for harmonic-analysis or DSP applications, however, you'll find it necessary to analyze and modify the internal "twiddle factors" inherent in the FFT.

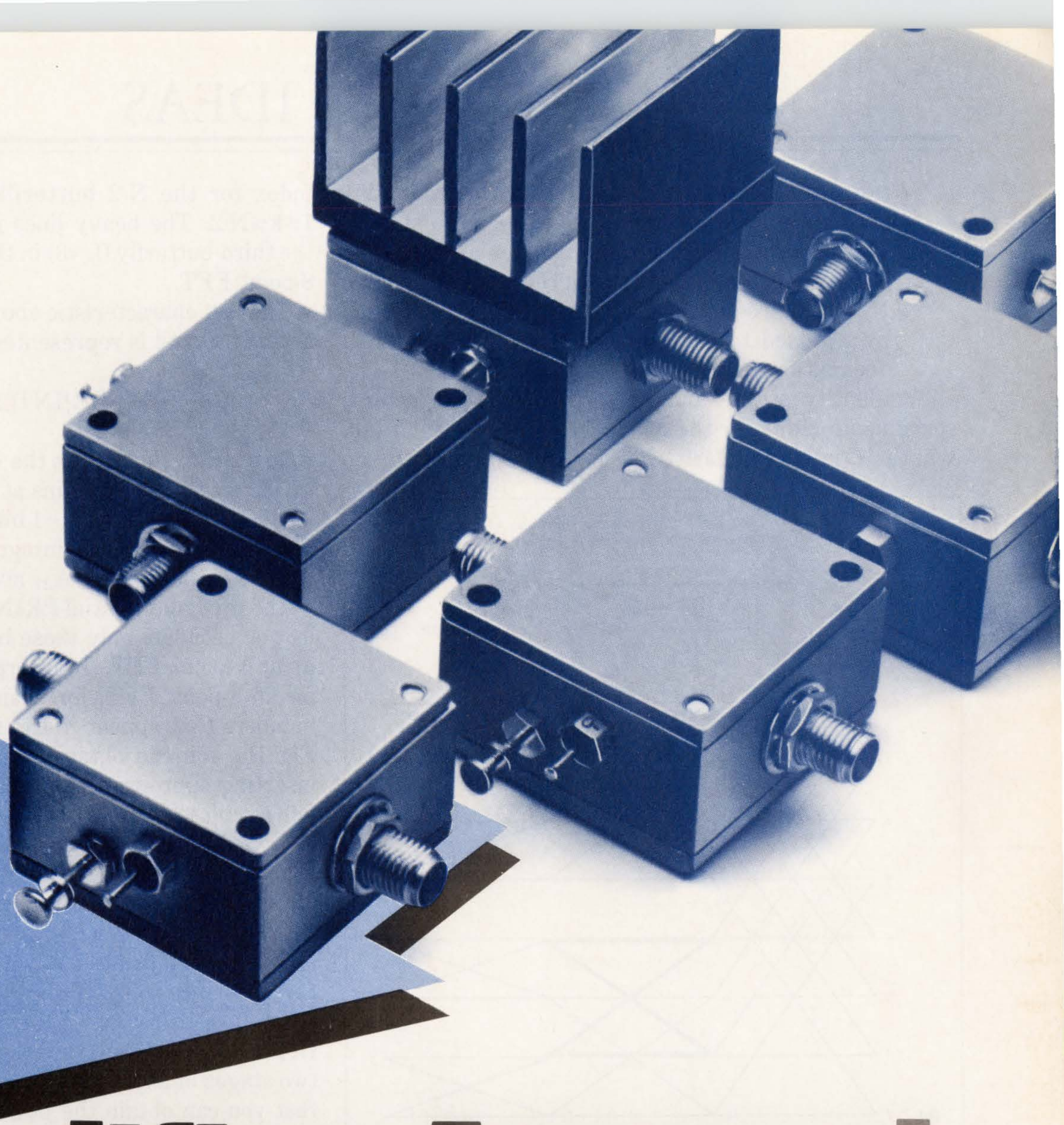
The Basic program of **Listing 1** contains an algorithm for analyzing the internal signal flows in an FFT by monitoring the angle associated with each of the complex twiddle factors. Often, you have to determine the twiddle factors for a specific subset of the butterflies in a given N-point FFT. (In the array of twiddle factors for smaller FFTs, the pattern is apparent, but the pattern becomes bewildering as you increase the FFT size.) The program returns the phase angles associated with twiddle factors of an arbitrary butterfly.

Further, the program directly obtains twiddle-factor angles for any or all butterflies in an arbitrary N-point FFT; you needn't re-evaluate the equations of the discrete Fourier transform each time you change the size of the FFT. The program's algorithm draws upon the following characteristics of the Decimation-In-Time (DIT) radix-2 FFT algorithm:

- An N-point FFT has M stages ($M=\log_2 N$), in which each stage is composed of N/2 butterflies.
- A single butterfly is defined as shown in **(Fig 1a)**.
- As defined in **Fig 1a,** a single butterfly ensures that the complex FFT outputs are scrambled (in

LISTING 1—BASIC PROGRAM

```
30 '     *********    PROGRAM: BUTTER.FLY  *********
40 '              CALCULATES FFT TWIDDLE FACTOR ANGLES
50 '
60 '                R.G. LYONS/SEDC (JUNE 1987)
70 '
80 CLS 'CLEAR SCREEN
90 INPUT "ENTER SIZE OF THE FFT (INTEGER POWER OF 2)";N
100 GOSUB 320:' FIND M [LOG(base 2) OF N]
110 PRINT:PRINT "THE FFT HAS";M;" STAGES.":PRINT:PRINT"ENTER THE RANGE";
120 PRINT " OF FFT STAGES OF INTEREST, ( 1 -to-";M;")"
130 INPUT "[SEPARATE BY A COMMA]";JSTART,JSTOP
140 PRINT:PRINT "THERE ARE";N/2;"BUTTERFLIES/STAGE. ENTER THE RANGE"
150 PRINT "OF BUTTERFLIES OF INTEREST, ( 1 -to-";(N/2);")"
160 INPUT "[SEPARATE BY A COMMA]";KSTART,KSTOP:PRINT:PRINT
170 LPRINT "TWIDDLE FACTORS FOR";N;"-POINT FFT"
180 LPRINT "J IS THE STAGE INDEX ( FROM 1 TO";M;") OF THE FFT,"
190 LPRINT "K IS THE BUTTERFLY INDEX ( FROM 1 TO";(N/2);") FOR EACH STAGE."
200 FOR J=JSTART TO JSTOP
210    LPRINT:LPRINT
220    FOR K=KSTART TO KSTOP
230       Z=INT(((2^J)*(K-1))/N)
240       GOSUB 390:' BIT REVERSE Z
250       AUP=ZBR
260       ART=ZBR+N/2
270       LPRINT "J=";J;"K=";K;"    Aup=";AUP;"  Art=";ART
280    NEXT K
290 NEXT J
300 END
310 '
320 '*********************** FIND LOG(base 2) OF N *************************
330 FOR M=2 TO 40
340    IF 2^M=N THEN RETURN
350 NEXT M
360 PRINT:PRINT "SELECTED N IS NOT A POWER OF 2!":PRINT: GOTO 90
370 '****************** END OF LOG(base 2) OF N ROUTINE ******************
380 '
390 '******************** BIT REVERSE VARIABLE Z *************************
400 ZBR=0
410 FOR KK=(M-2) TO 0 STEP -1
420    IF Z>=2^KK THEN ZBR=ZBR+2^(M-KK-2):Z=Z-2^KK
430 NEXT KK
440 RETURN
450 '********************** END OF BIT REVERSE ROUTINE ******************
```



the bit-reversed sense), provided that the FFT inputs are ordered samples.

- The twiddle-factor phase angle for an arbitrary butterfly is the bit-reversal of the integer (modulo N) of the product: The butterfly index, multiplied by 2 raised to the power of the FFT's order of decimation.

To identify stages and butterflies, let the letter j serve as an index for the M stages of an N-point FFT, where $1 \le j \le M$. Similarly, let the letter k serve as an index for the N/2 butterflies in each stage, where $1 \le k \le N/2$. The heavy lines in **Fig 1b,** then, illustrate the third butterfly (k=3) in the second stage (j=2) of an 8-point FFT.

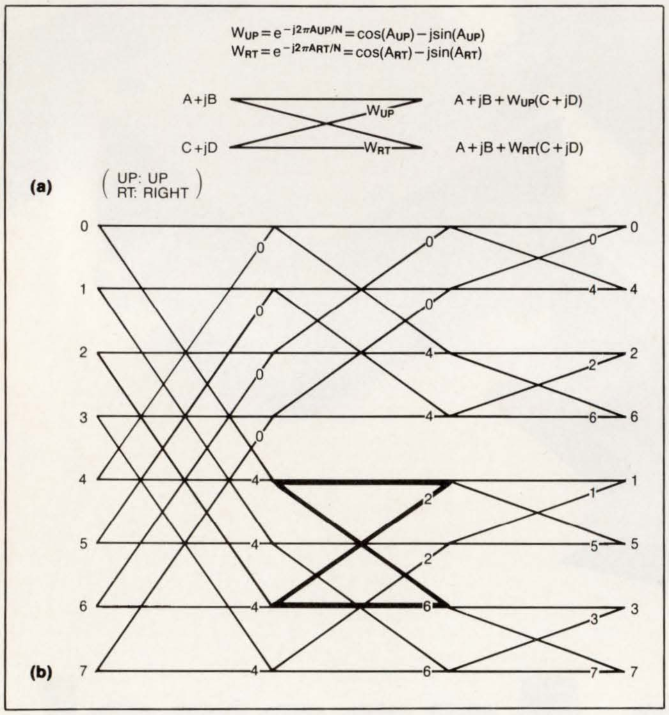


*Fig 1—**The standard butterfly operation (a)** accepts the inputs A+jB and C+jD on the left and returns the quantities on the right. The numbers on the 8-point-FFT figure **(b)** (right four columns only) represent the output from **Listing 1** when it is applied to the 8-point FFT.*

The last characteristic above appears in the program at line 230 and is represented mathematically as

$$A_{UP}=BR\{INT[2^j(k-1)/N]\},$$

where BR{z} represents the operation of the bit-reversal subroutine that begins at line 400 in **Listing 1.** The quantity z consists of M−1 bits, and INT[z] is a function that returns the lowest integer that is less than or equal to z. The phase angle A_{RT} always equals $A_{UP}+N/2$.

The program's initial PRINT and INPUT statements let you calculate only those butterfly angles of interest in an N-point FFT. To interpret the program's output for an 8-point FFT, for example, compare it with the numbers that appear in the rightmost four columns of **Fig 1b.** You can obtain the actual twiddle factors by inserting appropriate statements after line 260, which will calculate and print the sine and cosine of A_{UP}/N and A_{RT}/N.

You can also obtain the radix-2 FFT's bit-reversed output order by selecting only those butterflies contained in the last stage (j=M) of an arbitrary FFT. Note that the printed A_{UP} and A_{RT} values are exactly the indexing order of the bit-reversed FFT outputs. After further review of the twiddle-factor angles for a DIT FFT, you'll see that you can implement the first two stages of any DIT FFT without multiplication, and that you can obtain the power spectral-density results for an 8-point FFT without any sine or cosine multiplication. **EDN**

To Vote For This Design, Circle No 750

Receiver guards against current-loop shorts

R Mark Stitt
Burr-Brown, Tucson, AZ

The receiver circuit in **Fig 1** uses a current-protector device to guard against short circuits in the current-loop lines. Although such modern receiver circuits use a 50Ω sense resistor (R_1) that develops only 1V at 20 mA (compared with older designs that used a 250Ω resistor and developed 5V at 20 mA), this lower voltage exacts a penalty: More fault current flows in the event of a short circuit. In a circuit using ±18V supplies, for example, the 50Ω resistor dissipates 26W when a short circuit occurs, and the supply must deliver 1A.

In **Fig 1**, an IC difference amplifier senses the current signal and R_3 protects the circuit by providing foldback current limiting following a short circuit in the

CIRCLE NO 79

current loop. The loop current develops a signal across R_1; connecting this resistor to the negative rail makes full use of the current transmitter's dynamic range. The difference amplifier shifts the signal level to ground and also rejects any common-mode signals caused by fluctuations in the power supply.

Resistor R_2 preserves the amplifier's CMR by providing a source impedance at terminal 3 similar to the impedance at terminal 2. A 5% tolerance for R_2 maintains 86-dB CMR, but note that R_1's tolerance has a direct effect on the output's gain accuracy. V_{OUT}'s range is −0.2 to −1V for a 4- to 20-mA input. By interchanging the amplifier's inputs, you can obtain a positive 0.2 to 1V range. The circuit can also serve as a receiver for current loops connected to the negative rail; you simply swap connections to the positive and negative rails.

R_3 isn't actually a resistor but a protection circuit dubbed the PTC by its manufacturer; its only function is to protect R_1. When a short circuit in the current loop places a supply voltage across R_1 and the PTC, current through these components increases sharply. The higher current heats the PTC, triggering a change in resistance (from less than 2Ω to about 3 kΩ) that limits the R_1 current to about 10 mA. The response time depends on the supply voltages: about 0.6 sec for ±18V; about 1.4 sec for ±15V (**Fig 2**). When you remove the short circuit, the PTC resets to its low-resistance value.

The material in the PTC current protector is a homogeneous mixture of carbon granules in a polyolefin polymer base. During normal PTC operating currents, the granules are in contact with each other, forming a low-resistance path through the device. At the trip current (300 mA), the polyolefin expands and separates the granules, which raises the resistance. **EDN**

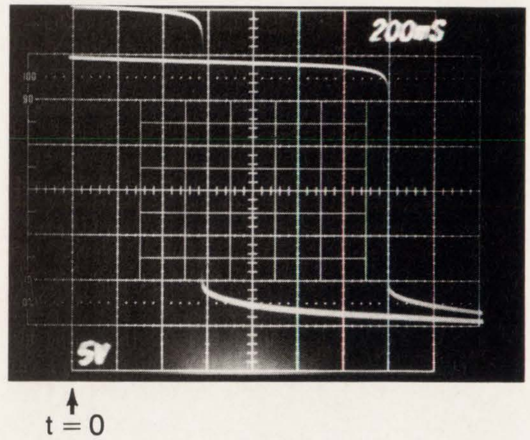


Fig 2—These waveforms from Fig 1 show how the PTC causes a change in the voltage across R_1 following a short in the current loop at t=0. This double-exposure photo illustrates the circuit's response to two operating conditions: ±18V supplies, 0.6-sec response; ±15V supplies, 1.4-sec response.

To Vote For This Design, Circle No 748

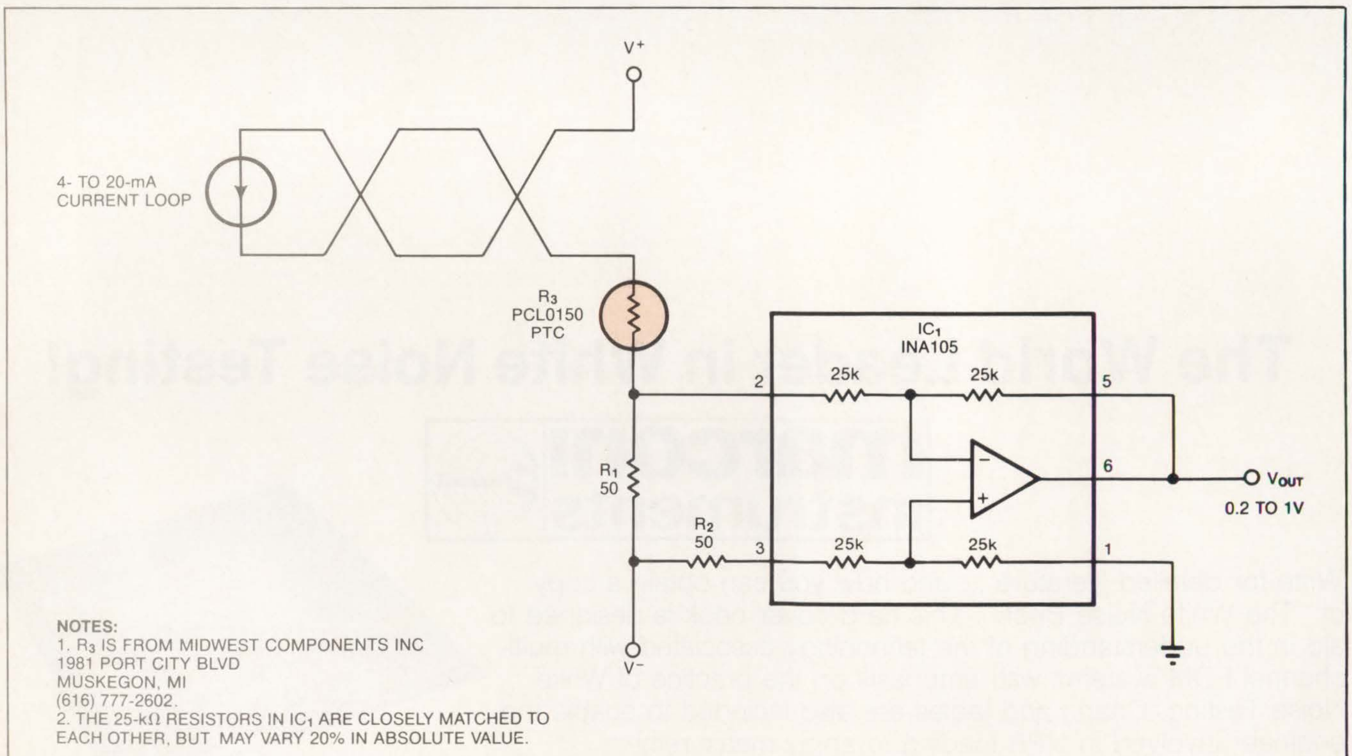


Fig 1—This 4- to 20-mA receiver circuit includes a current-protection device, R_3, whose resistance increases if a short circuit occurs in the current loop.

CIRCLE NO 13

PLD implements permutation addressing

James L Tolles
Tolles Engineering, Simi Valley, CA

To allow a system's mother board to select among circuit cards plugged into a backplane, you have a choice of several addressing techniques. You can connect a separate strobe line to each card, for example, but this technique complicates the backplane wiring and requires the main board to generate a separate strobe output for each card. Or, you can use the familiar technique of binary addressing, which requires a set of address lines connected to each card in parallel. Each card includes an address decoder and a device for manually setting the card's address assignment (such as a DIP switch). This approach provides each card with a unique address that stays with the card regardless of its slot position. However, if your application involves a moderate number of cards and a dedicated slot position for each, then the option of permutation addressing may be the most effective.

In permutation addressing, the system defines a valid address by setting a specified number of address lines low. In **Table 1**, for example, three lines low on an 8-line bus provides access to any one of 34 card slots. Different 3-line combinations define each address, and you hard-wire each group of three to the appropriate card connector. Because the address for all cards is the same (000), a 3-input NOR gate on each card serves as the address decoder, providing a high-strobe signal when the card's address is active. **Fig 1a** shows the lines you connect to the first six card connectors.

Fig 1b shows a PLD (IC_1) that generates permutation addresses in response to a 6-bit address. The address can originate from a counter or an address bus. In this example, a 6-bit counter drives the PLD, and the resulting output addresses provide sequential access to 34 cards at 500-nsec intervals. The Enable PA signal prevents change on the output (O) lines until all the input (I) lines have settled, thereby eliminating glitches on the O lines.

The PLD also saves board space. An alternative system, for example, required five 74LS138s to generate the separate strobes for each of the 34 cards. **EDN**

TABLE 1—PERMUTATION ADDRESSES

LOCATION	PERMUTATION ADDRESSES (THREE BITS LOW DEFINES A VALID ADDRESS)							
	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
0	0	0	0	1	1	1	1	1
1	0	0	1	0	1	1	1	1
2	0	0	1	1	0	1	1	1
3	0	0	1	1	1	0	1	1
4	0	0	1	1	1	1	0	1
5	0	0	1	1	1	1	1	0
6	0	1	0	0	1	1	1	1

To Vote For This Design, Circle No 747

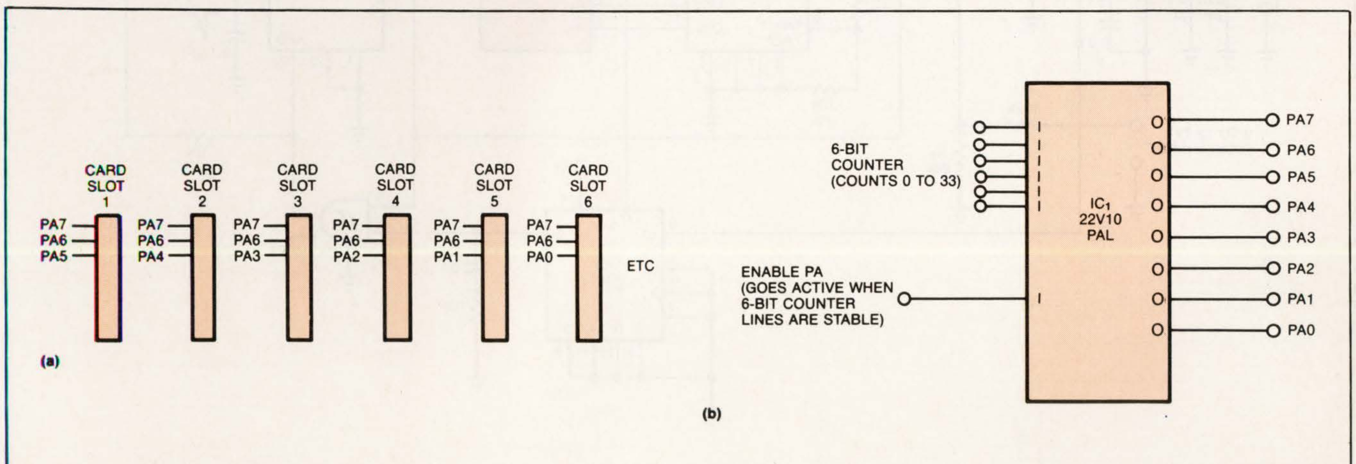


*Fig 1—**A space-saving PLD** generates permutation addresses in response to a 6-bit input address. Address lines connect to the backplane card slots as shown in **a**.*

Talking meter gives dc-voltage readings

Ricardo Jimenez-G
San Diego State University, Calexico, CA
and Francisco Meza and Jose J Lara
Mexicali Technological Institute, Mexicali, Baja California, Mexico

The Fig 1 circuit is a low-cost ($30) dc voltmeter that measures a positive 0 to 12.7V input and then voices the result in English. The meter can monitor a dc voltage automatically, thereby freeing a user for other tasks. Its resolution is ±0.1V.

Resistors R_1 and R_2 attenuate the input voltage, and an 8-bit A/D converter (IC_4) converts the result to a decimal equivalent at the outputs DB_0-DB_6. This 7-bit word drives the EPROM's upper address lines A_6-A_{12}, selecting a block of memory within the EPROM. Counter IC_3 then scans those memory locations in sequence by driving the lower address bits A_0-A_5. As a result, the EPROM delivers a preprogrammed sequence of instructions to the speech processor chip (IC_6).

Timer IC_2 is configured as a monostable monovibrator. When you depress the test switch, S_1, the monostable generates a 1.1-msec pulse that sets the Q output of flip-flop IC_7 high. The resulting negative transition at the speech processor chip's $\overline{ALD}$ input (pin 20) loads the current EPROM output and causes the

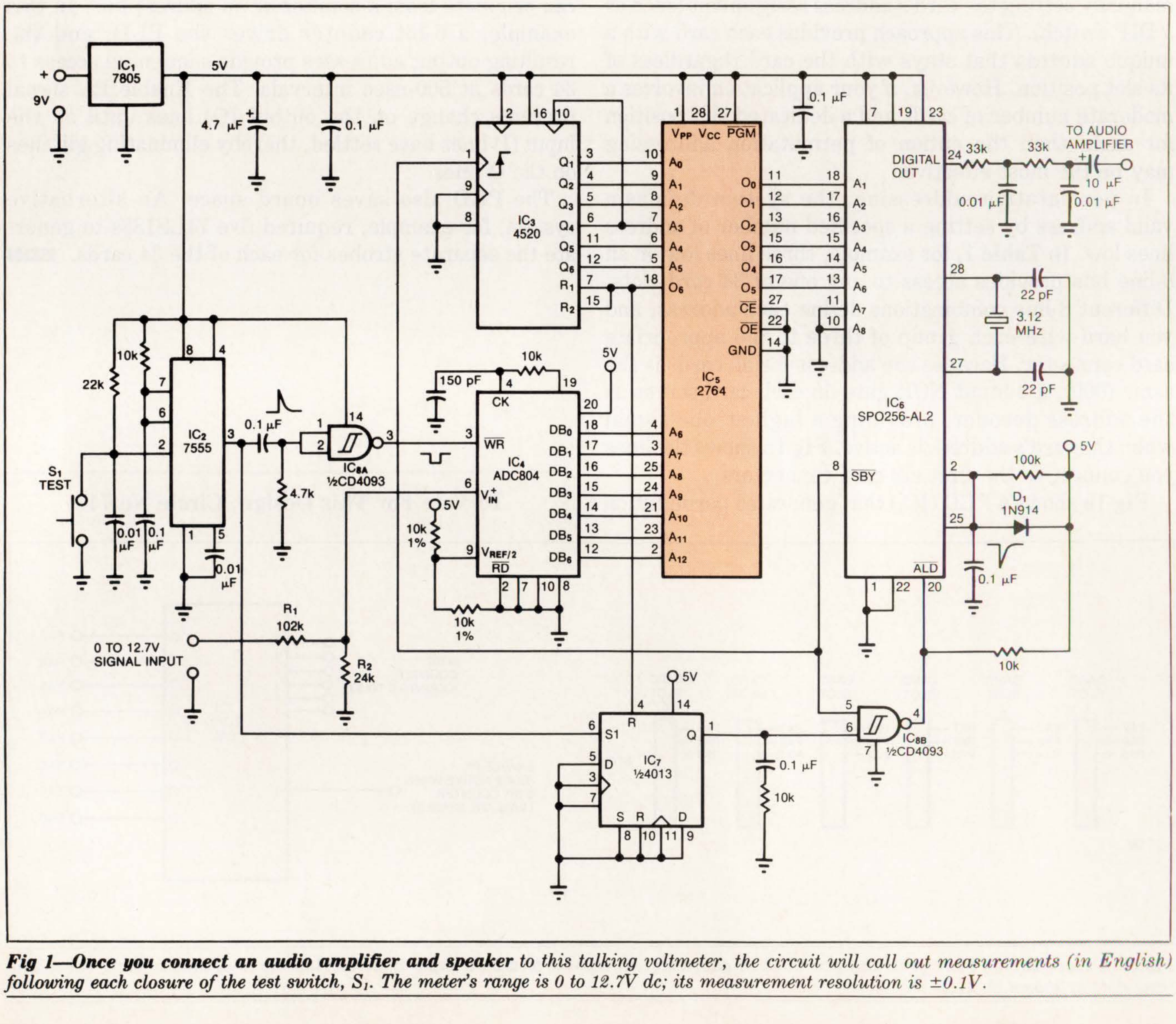


Fig 1—Once you connect an audio amplifier and speaker *to this talking voltmeter, the circuit will call out measurements (in English) following each closure of the test switch, S_1. The meter's range is 0 to 12.7V dc; its measurement resolution is ±0.1V.*

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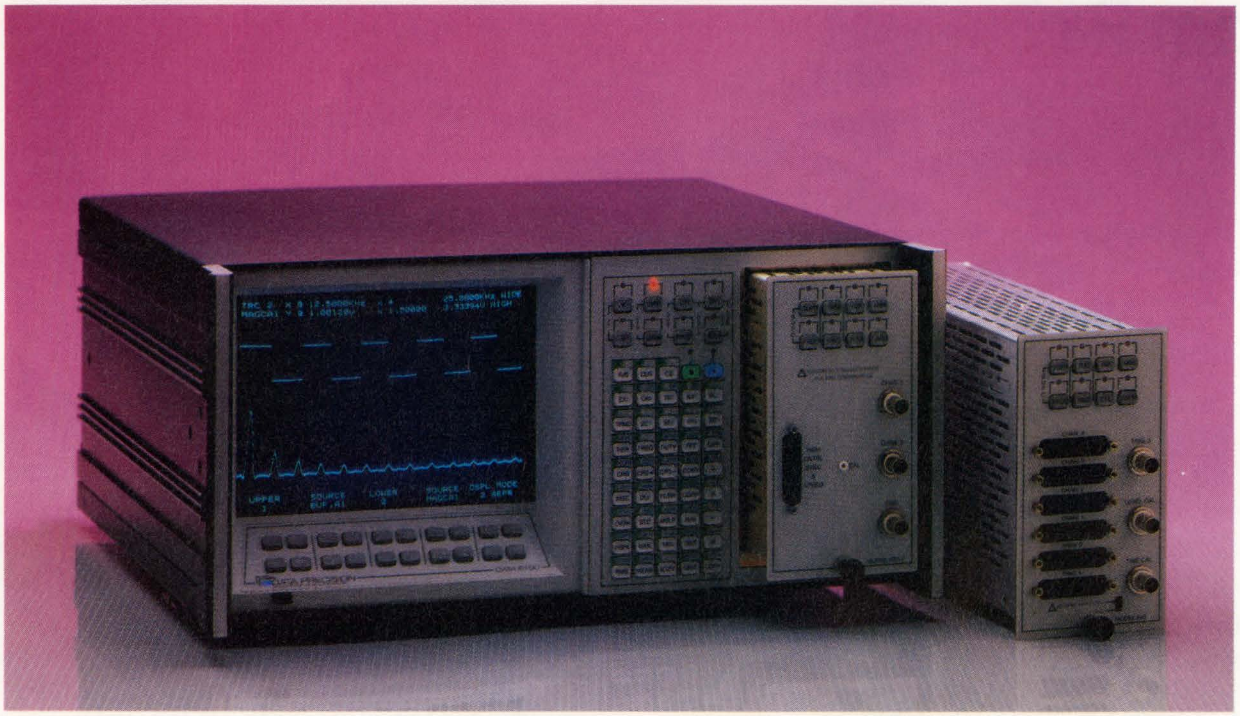

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TABLE 1—SAMPLE REPORT

DECIMAL ADDRESS	HEX ADDRESS	HEX DATA	ALLOPHONE	PHRASE
64	40	2F	ZZ	
65	41	3C	YR	"ZERO"
66	42	35	OW	
67	43	2	50-mSEC PAUSE	
68	44	9	PP	
68	45	5	OY	"POINT"
70	46	B	NN1	
71	47	11	TT1	
72	48	2	50-mSEC PAUSE	
73	49	39	HH2	
74	4A	F	AX	
75	4B	F	AX	"ONE"
76	4C	B	NN1	
77	4D	4	200-mSEC PAUSE; RESETS IC_6	
78	4E	44	200-mSEC PAUSE; RESETS IC_3 & IC_7	

processor to assert a low logic level at the $\overline{SBY}$ output (pin 8). This action changes the IC_{8B} output to a logic one, causing the processor to hold $\overline{SBY}$ low for an interval appropriate to that particular allophone. Note that you must connect an audio amplifier and speaker to the output as indicated.

The processor initiates the next allophone cycle by driving $\overline{SBY}$ high. Each audible report requires three to 20 allophones, which you can get from the dictionary that accompanies the speech-processor package (available at Radio Shack). In essence, you must program the EPROM in 200 blocks of 3 to 20 bytes each.

An input of A_6-A_{12}=1000000 (corresponding to a 0.1V input), for example, produces the words "zero point one" from the audio amplifier. You store the allophones representing these words in the EPROM as shown in **Table 1**. After each report, the hex-data instructions 4 and 44 internally reset the speech processor, and via the processor's 06 output they reset the counter and the flip-flop as well.

(Ed Note: Mr Jimenez-G has a 2764 EPROM that contains the data required for this circuit. If you send him a 2764 device and the necessary postage, he will return a programmed EPROM to you. Or, he'll be glad to send you a Xerox of the EPROM program if you send him a self-addressed envelope with two $0.22 stamps. His address is 96 Carmen Rivera Ave, Mexicali, Baja California, 21280 Mexico.) **EDN**

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ISSUE WINNER

The winning Design Idea for the May 14, 1987, issue is entitled "Nonlinear load extends PLL frequency range," submitted by Basel F Azzam and Christopher R Paul of Coherent Communications (Hauppauge, NY).

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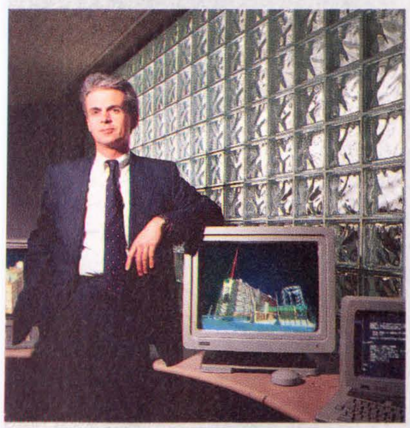

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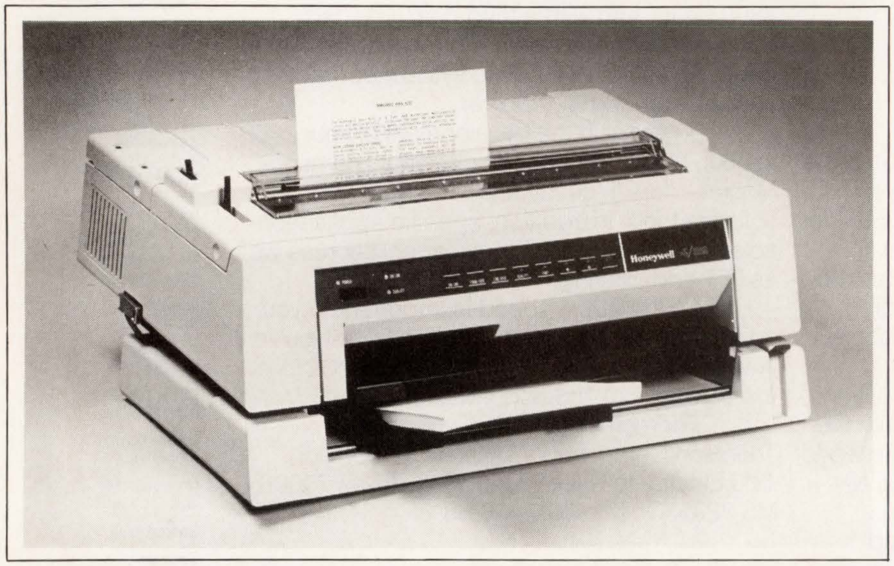


COLOR PRINTER

- *Provides letter-quality print at 120 cps*
- *Has resolution of 60×18 dots/character*

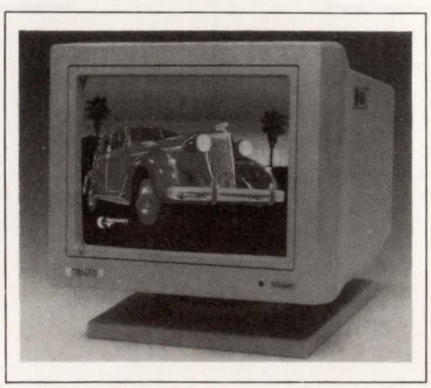
The 4/62 is a color dot-matrix printer designed for high-volume, letter-quality office output. Like the vendor's 4/66, it can switch automatically from cut sheets to fanfold paper, without your having to remove the paper from the tractors. An 18-wire staggered printhead permits the printer to produce letter-quality characters at 120 cps in a single pass. Its resolution is 60×18 dots/character; its noise level is below 55 dB. The device prints in seven colors, and you have the option of employing as many as six of the 20 available fonts on one page. The 15.4-in. printable width permits the processing of legal documents, spreadsheets, and B-size landscape paper. The printer is compatible with the IBM Graphics Printer and the Epson JX 80. $2160.

Honeywell Bull Italia, 120 Howard St, Suite 800, San Francisco, CA 94105. Phone (415) 974-4340.

Circle No 351

PS/2 COLOR MONITOR

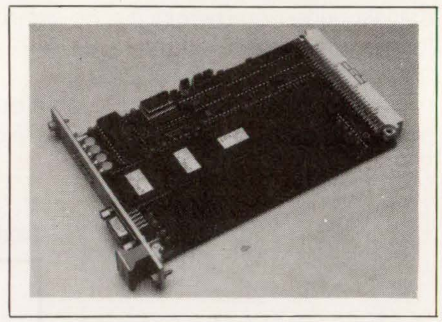
- *Has automatic scan frequency synchronization*
- *Features a 12-in., 0.28-mm dot-pitch CRT*



The Ultrasync is an RGB color monitor for the IBM Personal System/2 Series computers; the IBM PC, PC/XT, PC/AT, and compatibles; and Apple's Macintosh II. The monitor can automatically synchronize with any horizontal scan frequency from 15 to 35 kHz and, most notably, with any vertical scan frequency from 50 to 120 Hz. Measuring 12 in. diagonally, the monitor is compatible with the IBM MDA, EGA, CGA, and PGC; Hercules graphics card; and Persyst BOB. Its dot pitch is 0.28 mm; its resolution is 770×570 pixels max. The monitor offers eight, 16, or 64 colors for TTL inputs and has an infinite color palette for analog inputs. It features a 30-MHz video bandwidth and a built-in tilt-and-swivel base. $795.

Princeton Graphics Systems, 601 Ewing St, Bldg A, Princeton, NJ 08540. Phone (800) 221-1490; in NJ, (609) 683-1660. TLX 821402.

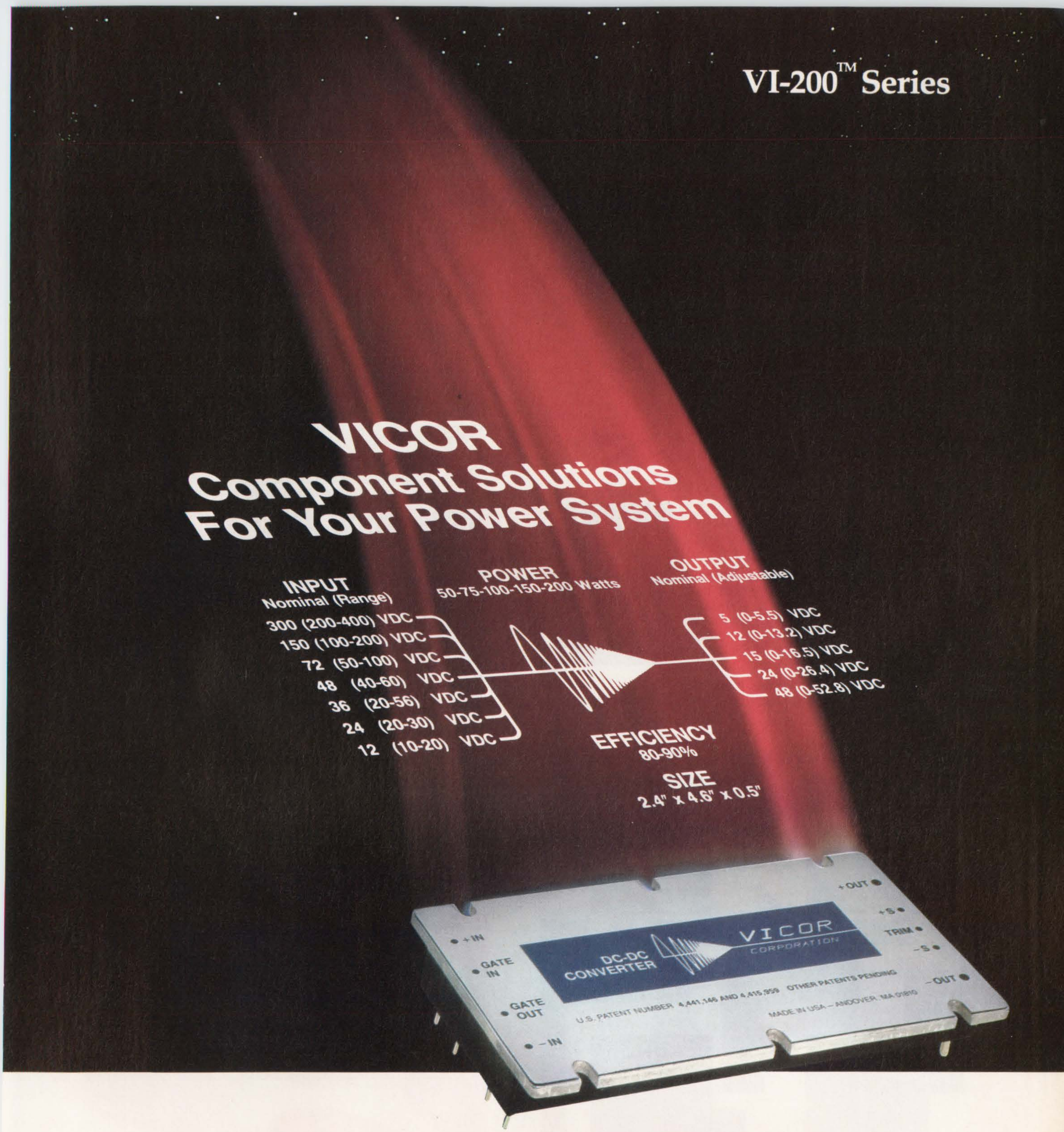
Circle No 352



GRAPHICS CONTROLLER

- *Prints graphics on a single-height VME Bus Eurocard*
- *Utilizes the Hitachi Advanced CRT Controller (ACRTC) 63484*

The VGPM is a graphics controller designed around the Hitachi ACRTC 63484 and integrated ASIC chips. The vendor claims that this single-height VME Bus Eurocard provides the performance of a dual-height board. The ACRTC 63484 runs at 8 MHz and provides typical drawing rates of 2 million pixels/sec. The 1M-byte dynamic RAM can be accessed in the 32-MHz dual mode or the 64-MHz single mode; the board is compatible with 20-in. flickerless-screen monitors. The board's horizontal and vertical frequencies are programmable via the ACRTC, and its graphics resolution is programmable to 1280×1024 pixels. The controller uses bit-block transfers to generate characters rapidly. The controller provides 16 colors with 4 bits/pixel; an optional



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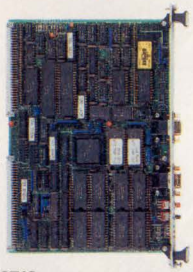
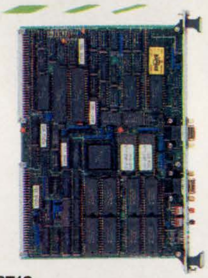
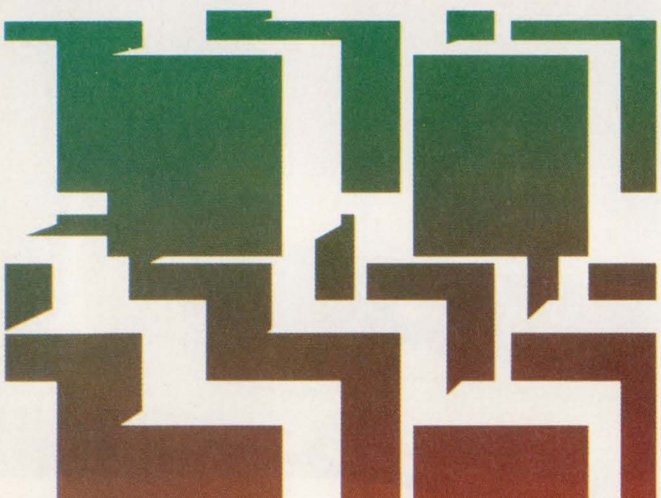
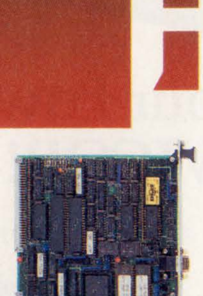
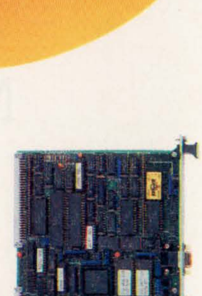






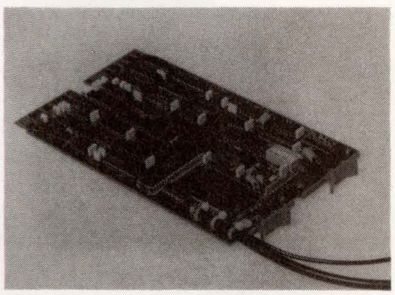




color look-up table lets you display 16 simultaneous colors from a palette of 4096. The board requires 5V dc at 0.9A typ and operates over 0 to 70°C. $1499 (OEM qty).

Pep Modular Computers Inc, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (800) 228-1737; in PA, (800) 255-1737. TLX 6711521.

Circle No 353



LAN INTERFACE

- *Interfaces Q Bus systems to Arcnet LANs*
- *Provides onboard data buffering*

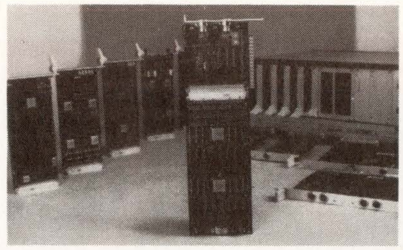
The Q Bus-compatible Q-ARC-01 interface card allows you to connect equipment based on Micro/Vax II, Micro/PDP, or LSI-11 architectures in an Arcnet LAN. You can use the card with the 16-, 18-, and 22-address-bit versions of the Q Bus. The interface is based on the SMC9026 network-controller IC, and it has 2k bytes of onboard dual-port RAM (four 512-byte packet buffers). Both the send and the receive data channels can use these packet buffers in any combination, and you can locate the base address of this buffer memory on any 2k-byte boundary within the Q Bus's memory-address range. You can position the SMC9026's control and status registers on any 4-byte boundary within the Q Bus I/O page. $1795.

Comendec Ltd, 6a School Lane, Hopwas, Tamworth, Staffs B78 3AD, UK. Phone (0827) 286180.

Circle No 354

C&C Marketing, Box 280, Batavia, IL 60510. Phone (312) 879-2074.

Circle No 355



TRANSPUTER INTERFACE

- *Allows you to install Transputer boards in IBM PCs*
- *Provides a bridge between the PC bus and other buses*

The Megaframe/IBM adapter card allows you to install any of the company's Megaframe Transputer-based parallel-processing industrial computer boards in a standard IBM PC slot. This facility allows you to use the PC as a Transputer-development system or to operate the Transputer board as an accelerator, improving the PC's processing power. Alternatively, you can plug only the adapter card into the PC and communicate with other equipment via a 20M-bps Transputer link operating at RS-422 levels. This link can be as long as 10m. The vendor offers interface boards that allow you to connect the link's far end into Transputer systems or into VME Bus and Siemens industrial-bus systems. DM 980.

Parsytec GmbH, Julicher Strasse 338, 5100 Aachen, West Germany. Phone (0241) 1822275. TLX 08329659.

Circle No 356

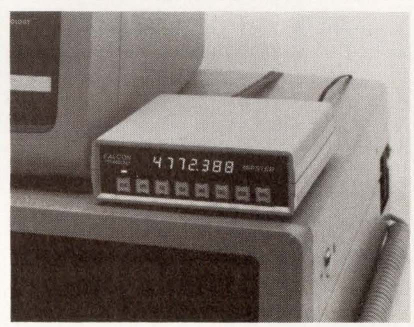
VISION SYSTEM

- *Provides image capture on IBM PC/XT and PC/AT*
- *Allows real-time or post-capture image processing*

The IDS512 and IDS542 add-in boards for IBM PC/XTs, PC/ATs, or compatible computers provide 512×512-pixel and 1024×1024-pixel imaging capabilities, respectively. The boards accept three CCIR or NTSC standard composite-video inputs, which are digitized to 8-bit/pixel resolution. The boards have internal or external gen-lock facilities, which synchronize the digitization to the video signal. The digitizer output is then fed through an 8-bit input look-up table before being stored in video RAM. The video RAM provides RGB outputs, which pass through separate 8-bit output look-up tables before being converted back to analog signals by three separate D/A converters. A monochrome output is also provided. Feedback from the output to the input allows real-time image processing. PC-bus access to the look-up tables and video RAM allows you to modify the look-up-table data and post-capture image processing. A floppy disk containing a library of image-processing routines —including linear and nonlinear convolutions—and menu-driven vision-system software are provided with the board. From Frfr 55,000.

i2S, BP 76, 33041 Bordeaux Cedex, France. Phone 56291003. TLX 540504.

Circle No 358



MEASURING INSTRUMENT

- *Measures machine speed in thousands of instructions/sec*
- *Shows results on a 7-segment LED display*

The Mipster is a modular measuring instrument for the IBM PC, PC/XT, or any 8086- or 8088-based system. It measures the following system parameters: machine speed (in thousands of instructions/sec), CPU clock frequency (within 0.03% accu-

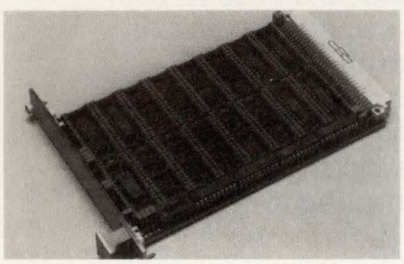
Text continued on pg 238

Now GE/RCA drives

racy), number of memory accesses, number of I/O port accesses, and number of times the CPU flushes the instruction-stream queue. A probe, which plugs into the system under test, intercepts and processes the appropriate signals either to or from the CPU. The results are sent to a 7-segment LED display. You can use front-panel keys to select the mode of operation (continuous or triggered), the counting period (1.0 or 0.1 sec), and the system parameter. When operating in the continuous mode, the device refreshes the selected parameter every 1.0 or 0.1 sec; in the triggered mode, it accumulates the parameter once and then displays it. $495.

Falcon Technology Inc, 664 W Hawthorne St, Glendale, CA 91204. Phone (818) 244-6460.

Circle No 359



RAM BOARD

- *Accommodates as much as 2M bytes of static RAM or ROM*
- *Provides two memory blocks with different access times*

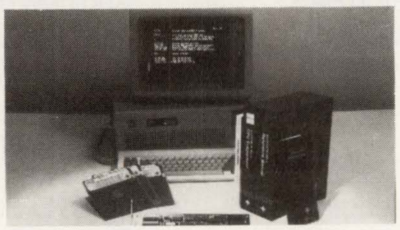
You can load the single-Eurocard VMEM-S1 VME Bus memory board with CMOS static RAM or ROM, or a mixture of static RAM and ROM, to a maximum capacity of 2M bytes. The board has sixteen 32-pin sockets that you can fill with 28- or 32-pin memory devices. The memory is divided into two separate memory blocks, so you can use different access-time devices for each block. The board accommodates devices having access times in the range of 100 to 250 nsec. It provides for the battery backup of static RAM. The board's VME Bus slave interface includes both address and address-modifier decoding. DM 990.

Pep Modular Computers GmbH, Am Klosterwald 4, 8950 Kaufbeuren, West Germany. Phone (08341) 8974. TLX 541233.

Circle No 360

Pep Modular Computers Inc, 600 N Bell Ave, Pittsburgh, PA 15106. Phone (412) 279-6661. TLX 6711521.

Circle No 361



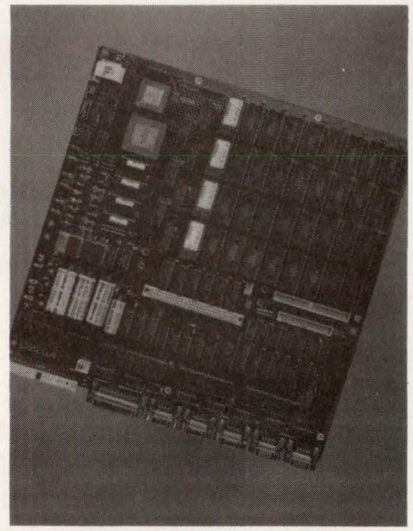
COPROCESSOR BOARD

- *For IBM PC-family- or BIOS-compatible systems*
- *Runs benchmark 2.6 times faster than a VAX 11/780 does*

The FB-4016 is a general-purpose coprocessor board that is compatible with IBM PC/AT-, PC/XT-, or BIOS-compatible systems. It combines the polyForth multitasking, multiuser operating system with the Novix NC-4016 high-speed microprocessor, yielding a high-speed coprocessor board for the IBM PC. Running polyForth at 5 MHz, it executes 10 Sieve of Eratosthenes benchmarks in 0.55 sec, which is 2.6 times faster than a VAX 11/780 or a 68020 running C at 16.7 MHz. The board has 128k bytes of RAM with 100k bytes available for applications. Applications needing faster I/O speed than is available through the PC bus can use the device's internal 40-pin high-speed I/O port directly. An extensive math library, database support, and a 1-msec clock for real-time applications are also included. $3450.

Forth Inc, 111 N Sepulveda Blvd, Manhattan Beach, CA 90266. Phone (213) 372-8493.

Circle No 362



1-BOARD COMPUTER

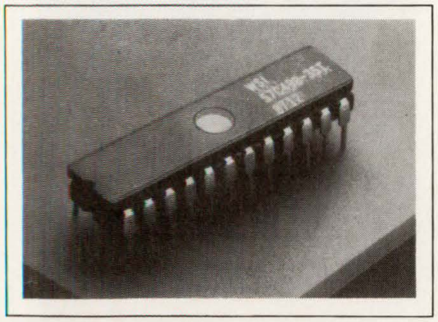
- *Runs a 12.5-MHz 68020 μP and a 68881 math coprocessor*
- *Includes serial ports, SCSI-bus and floppy-disk interfaces*

The Omega-OEM 32-bit single-board computer features a 12.5-MHz 68020 μP and a 68881 math coprocessor. It has 1M byte of zero-wait-state, nonvolatile static RAM, and it provides space for as much as 256k bytes of EPROM/ROM. You can expand the RAM to 5M bytes. Its communications ports include five RS-232C serial ports; a Centronics-compatible parallel port; and a 16-bit, bidirectional parallel printer port. The board also has a battery-backed real-time clock/calendar, a SCSI-bus initiator, and a Shugart-compatible floppy-disk controller. Its buffered, 16-bit expansion bus allows you to access 16M bytes of user memory. The board consumes 8W of power and has on-board rectification and power-supply regulators that allow you to power it directly from a transformer. Omega-OEM board, £1395 (100); OS-9/68K operating system, with a C compiler, £520.

Windrush Micro Systems Ltd, Worstead Laboratories, North Walsham, Norfolk NR28 9SA, UK. Phone (0692) 404086. TLX 975548.

Circle No 363

INTEGRATED CIRCUITS



CMOS EPROM

- *Offers 35-nsec access time*
- *Features 8k×8-bit organization*

The 35-nsec WS57C49B is the world's fastest 8k×8-bit CMOS EPROM, according to the manufacturer. As a pin-compatible, programmable alternative to bipolar PROMs, the device consumes a fraction of the power (400 mW). Available in a 35-nsec commercial version or a 45-nsec military version, the EPROM comes in a 300-mil-wide ceramic DIP, a 600-mil-wide DIP, or a 28-pin ceramic LCC. 35-nsec version in a 300-mil ceramic DIP, $29.50 (100).

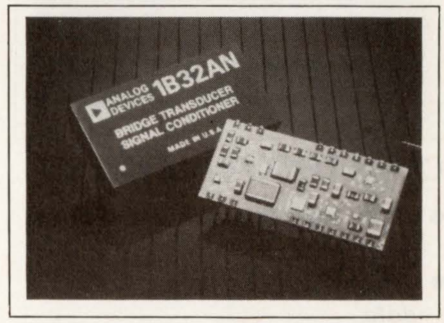
Waferscale Integration Inc, 47280 Kato Road, Fremont, CA 94528. Phone (415) 656-5400.

Circle No 368

BRIDGE TRANSDUCER

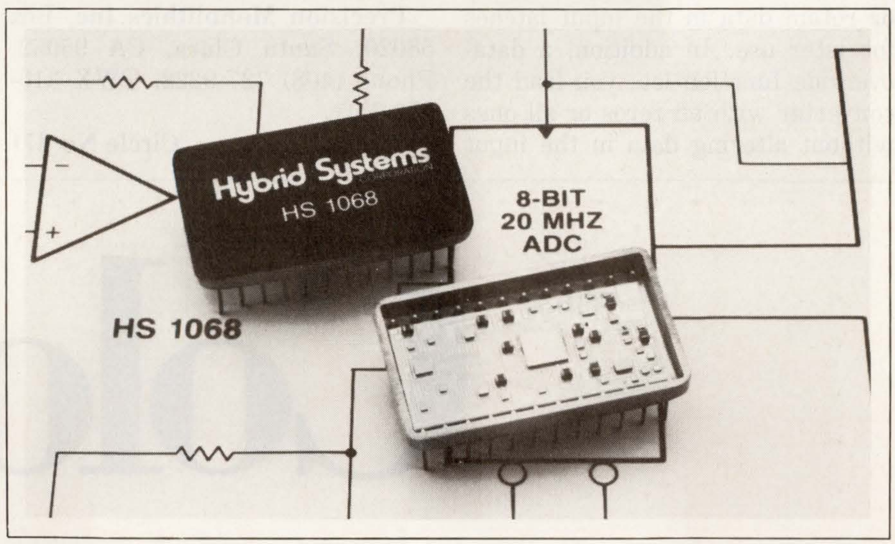
- *Maximum nonlinearity is ±0.005%*
- *Offset TC is ±0.07μV/°C*

The hybrid 1B32 is the most accurate strain-gauge signal conditioner available, claims the manufacturer. Providing amplification, filtering, and voltage excitation for load cells and other bridge-configuration transducers, the device includes a chopper amplifier, a low-pass filter, and an adjustable transducer-excitation source. The signal conditioner's ±0.005% max nonlinearity error and 140-dB CMR (at 60 Hz, for a gain of 1000) makes it compatible with requirements for 14- to 16-bit accuracy. Other specs include a ±0.07-μV/°C voltage-offset temperature coefficient (TC), a ±2-ppm/°C gain TC, and 1-μV p-p noise (0.1 to 10 Hz). The 1B32 provides an adjustable ±10V offset that lets you null a large load or do tare adjustments. Pin-programmable gains include 333.3 and 500 for 2-mV/V and 3-mV/V load cells, respectively. The device draws 4 mA/−1 mA from ±15V supplies and comes in a 28-pin DIP. $52 (100). Delivery, four to six weeks ARO.



Analog Devices Inc, Literature Center, 70 Shawmut Rd, Canton, MA 02021. Phone (617) 461-3643. TLX 174059. TWX 710-394-6577.

Circle No 369



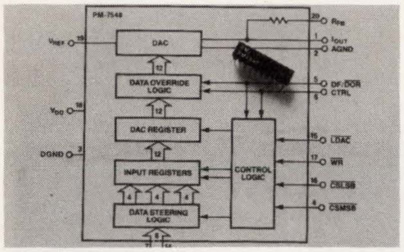
FLASH A/D CONVERTER

- *Has 8-bit resolution*
- *Provides 20M-sample/sec digitizing rate*

The HS1068 20M-sample/sec, flash A/D converter includes all necessary analog-support circuitry in the package: a wideband input amplifier, precision 1.2V voltage reference, and a 3-state output register. The 8-bit device comes in a 24-pin DIP that occupies less space than the original 28-pin-DIP TDC1048. You pin-program the converter to accept an input range of either 0 to 1V or ±0.5V, and you can select straight binary, inverted binary, 2's complement, or inverted 2's complement output code. Separate digital outputs flag input overranges at zero and full scale. Power supplies are 5V and −5.2V, drawing 101 and 207 mA, respectively. Power dissipation is 1.67W. Other key specs are ±½LSB integral and differential linearity errors, 60-psec aperture time, 2% differential gain, and 1° max differential phase. HS1068C, $295; HS1068B, $375 (100). Delivery, eight to 12 weeks ARO.

Hybrid Systems Corp, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821. Phone (617) 667-8700. TWX 710-347-1575.

Circle No 370



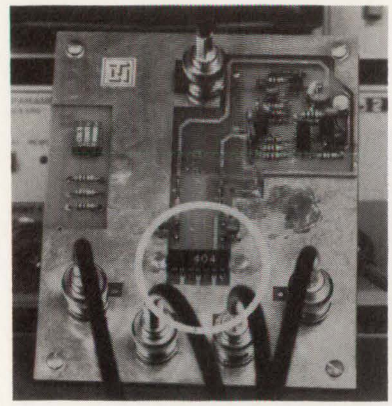
CMOS D/A CONVERTER

- *12-bit resolution; 8-bit-bus compatible*
- *Accepts left- or right-justified data*

The PM-7548 CMOS D/A converter combines 12-bit resolution with an 8-bit data-bus interface that accepts left- or right-justified data. The digital inputs are buffered; you can update the converter immediately or retain data in the input latches for later use. In addition, a data-override function lets you load the converter with all zeros or all ones without altering data in the input latches. It features ±½-LSB integral and differential linearity error over temperature, ±1-LSB gain error, and 0.03-LSB max zero-scale error. Compared with the original industry-standard equivalent, the converter offers a 30% reduction in glitch energy, a 30% reduction of input capacitance, and a 20-dB improvement in PSR. The internal voltage regulator ensures TTL compatibility while operating with supply voltages from 5 to 15V. The device comes in two electrical grades for each of the commercial, industrial, and military temperature ranges. From $7.58 to $30.92 (100). Delivery, eight to 10 weeks ARO for the commercial grade; stock for the industrial and military grades.

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 371



ANALOG SWITCH

- *Crosstalk is −77 dB at 10 MHz*
- *4×1 crosspoint switch*

The LR404 is a 4×1 crosspoint analog switch that comes in a 14-pin plastic DIP. The device is suitable for use in video signal-switching matrices; using multiple devices, you can switch many outputs to a common output. The chip provides differential phase and gain of 0.05° and 0.05%, respectively, at 3.58 MHz. Crosstalk is better than −77 dB at 10 MHz. $4, moderate quantities.

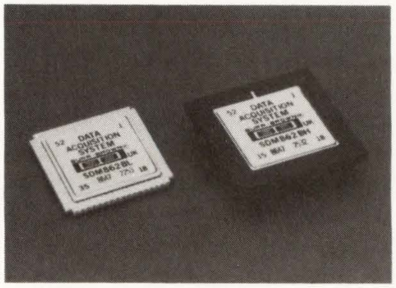
Linear Technology Inc, Box 489, Station A, Burlington, Ontario, Canada L7R 3Y3. Phone (416) 632-2996. TLX 0618525.

Circle No 372

DATA ACQUISITION

- *Complete, 12-bit data-acquisition systems*
- *45k-sample/sec at 8-bit resolution*

The SDM862 and SDM863 are miniature, complete data-acquisition systems, available either in a 68-lead LCC or a 68-lead pin-grid array. They both include an input multiplexer (the SDM862, 16-channel single-ended; the SDM863, 8-



channel differential); an instrumentation amplifier that is jumper-programmable for gains of 1, 10, and 100; an S/H amplifier; an A/D converter with a μP-compatible interface; and 3-state output buffers. The throughput rate for both devices is 22.22k-samples/sec in the serial mode or 33.33k-samples/sec in the overlap mode. It has input ranges of 0 to 10V, ±5V, and ±10V, and accuracy grades of 0.024% FSR and 0.012% FSR in the commercial-, industrial-, and military-temperature versions. Both models come in versions qualified for the requirements of BS9450/CECC63000. To evaluate the LCC versions, you can obtain a Eurocard pc board with an LCC socket from the company. From $103 (100). Delivery, stock to eight weeks ARO.

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 373

QUAD OP AMP

- *140-dB dynamic range with less than 0.0015% distortion*
- *Drives 600Ω loads*

Suitable for use in compact-disk players and other digital-audio systems, the LM837 quad op amp generates less than 0.0015% distortion over a 140-dB dynamic range. The output stage can drive a 600Ω load. The standard pinout (in a 14-pin DIP) lets you upgrade an existing

Text continued on pg 244

The Ultimate Math Machine.

Only from OKI:

The *Fastest* Floating Point DSP on the market today!

✓ **100ns Instruction Cycle Time** ✓ **40 MHz High-Speed Clock**

An outstanding achievement in Digital Signal Processing.

OKI presents the first real technology breakthrough in DSP with the CMOS 6992. A very high speed, very high performance Floating Point Processor which operates over a wide dynamic range—up to 480 dB. And provides pre- *and* post-normalization – in the first *true* CMOS Floating Point DSP.

The Ultimate Math Machine.

OKI's 6992 puts exceptional flexibility into your hands. A single chip, configurable for floating point format, fixed data format or a logical data format. Easy to interface with 8-bit, 16-bit and 32-bit MCUs.

Fastest development, too. Because OKI, of course, supports the DSP's sophistication with every sophisticated development and debugging tool you need—all PCDOS* compatible.

You're assured true DSP application ease, speed and cost-efficiency using OKI's special 6992 ICE optimized for realtime emulation. Supplied with a Macro Assembler and a special library of subroutines. Plus a PC add-on Evaluation Board you can order today—to get a *fast start* into advanced CMOS Floating Point DSP.

OKI: *the fast track in DSP*

for graphics, high-performance modems, image processing, speech processing and robotics applications.

SPECIAL OFFER: EDN 080687

OKI 6992 DSP Evaluation Board!

☐ Please rush _______ OKI 6992 DSP PC Add-on Evaluation Board(s)—125ns version with Assembler and technical data. Special introductory price per Board is $480.00, including shipping/handling/sales taxes.

Check or money order for $ ____________ enclosed.

(Sorry, no company purchase orders please.)

☐ Send only technical data package on OKI 6992 high-speed CMOS DSP.

Name/Title ______________________

Company ______________________

Address ______________________

City ______________ State ________ ZIP ________

Return to: Tel: (_______) ______________

DSP Marketing Manager, **OKI Semiconductor**, 650 N. Mary Avenue, Sunnyvale, CA 94086. (408) 720-1900. Offer limited to 3 Boards per customer and expires August 31, 1987. Available only for USA and Canada shipment.

DSP

OKI SEMICONDUCTOR

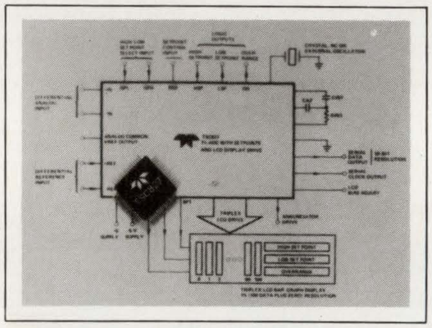
*PCDOS is a trademark of Microsoft Corporation.

CIRCLE NO 87

system with few or no design changes. The chip is also available in a molded small outline package. Unity-gain stable, the monolithic device specs an 8-V/μsec slew rate, a 140-kHz power bandwidth and a 15-MHz gain-bandwidth product. The input-noise voltage is 0.5 μV rms. $1.25 (25,000).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 721-5856. TLX 346353. TWX 910-339-9240.

Circle No 374



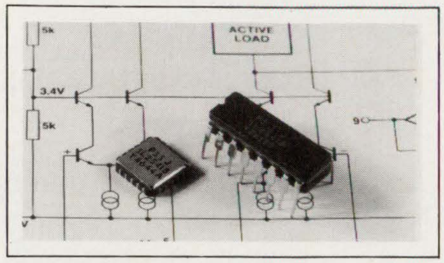
A/D CONVERTER

- *Bar-graph and 10-bit-serial outputs*
- *Two selectable set-points*

The TSC827 is a CMOS integrating-type A/D converter that includes on-chip drivers for a 101-segment LCD bar-graph display. The internal resolution is 1000 counts (±0.1%), and the result of each conversion is available as an additional serial digital output for use in driving numeric displays. The converter accepts positive inputs with full scale ranging from 0.1 to 2V, and the differential signal and reference inputs simplify the interface to a variety of signal sources. You can use switches or software programming to specify two setpoints; separate annunciators then flag under- and overrange inputs. The typical conversion rate is 7.5 samples/sec. The device consumes 15 mW and operates from a 9V battery. It comes in a 68-pin PLCC or a 60-pin flatpack. From $10.80 (100).

Teledyne Semiconductor, Box 7267, Mountain View, CA 94039. Phone (415) 968-9241. TWX 910-379-6494.

Circle No 375



OP AMP

- *Achieves a bandwidth of over 800 MHz into 50Ω loads*
- *Has several programmable parameters*

Featuring output rising- and falling-edge slew rates of 1400 and 900 V/μsec, respectively, the SL2541 op amp can directly drive 50Ω loads with a bandwidth in excess of 800 MHz. The output settling time to 0.5% of final value is 30 nsec, and various parameters, including open-loop gain, output current, supply-voltage range, and output dc offset, are externally programmable. The SL2541 is supplied in a 16-pin ceramic DIP or in a 20-pin leadless chip carrier; both packages operate over the military temperature range. £30.92 (100).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wiltshire SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 376

Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303. TLX 701464.

Circle No 377

COMPARATOR

- *Features sub-nsec propagation delay*
- *Contains eight comparators grouped as two sets of four*

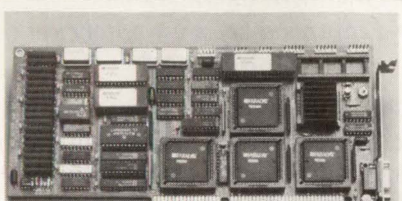
The SP93808 octal comparator features latched output data, adjustable input hysteresis, and glitch-capture circuitry. The eight comparators within the IC are divided into two groups of four, with each group controlled by a separate buffered clock input. The comparators spec a typical propagation delay of 950 psec, and individual comparator delays within the device are matched to within ±100 psec. They have a differential input voltage range of ±4V and a maximum input offset voltage of ±2.5 mV. The glitch-capture circuitry allows you to detect and latch glitches independently of the comparator strobe. Input hysteresis is adjustable between 0 and 10 mV, and the comparators can directly drive 50Ω loads. £40.37 (1000).

Plessey Semiconductors Ltd, Cheney Manor, Swindon, Wilts SN2 2QW, UK. Phone (0793) 36251. TLX 449637.

Circle No 378

Plessey Semiconductors, 9 Parker, Irvine, CA 92718. Phone (714) 472-0303.

Circle No 379



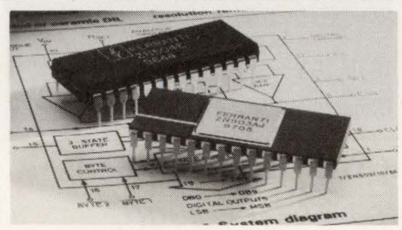
CHIP SET

- *PC/AT peripheral-control and CPU functions in four ICs*
- *6-, 8-, 10-, and 12-MHz operation*

The FE3400 chip set provides PC/AT peripheral-control and CPU functions with only four ICs. Implemented in 2-μm HCMOS technology, the four chips replace eight support ICs including the 8284 and 82284 clock generators, the 82288 bus controller, two 8237 DMA controllers, two 8259 interrupt controllers, an 8254 timer, and numerous SSI and MSI logic chips. Using the chip set reduces the area of a typical PC/AT mother board from 142 to 21.5 in^2 and reduces the typical chip count from 95 to 19. In addition, the chip set reduces the power requirement by 50% (16W). The FE3400 chips operate under the company's copyrighted BIOS to ensure IBM compatibility and are software-programmable for 6-, 8-, 10-, or 12-MHz operation. Starter kits and design-support tools are available. $118 (100). Delivery, 10 weeks ARO.

Faraday Electronics, 749 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 749-1900. TLX 706738.

Circle No 380



A/D CONVERTERS

- *Perform a 10-bit conversion in 15 μsec*
- *Feature parallel and serial I/O*

The ZN503 and ZN504 are 10-bit successive-approximation A/D converters that feature parallel and serial 3-state outputs. The ZN503 has a linearity specification of ½ LSB, while the ZN504 has a linearity specification of 1 LSB. You can configure the devices' TTL/CMOS-compatible parallel interface for 8- or 16-bit operation. The serial output suits the converters for remote sensing applications by reducing wiring requirements. Both devices have an on-chip 2.5V precision voltage reference, and are pin-programmable to have input ranges of 0 to 2.5V, 0 to 5V, or −2.5 to +2.5V. With the addition of two external components, the converters can perform a 10-bit conversion in 15 μsec. The ZN503 is available only as a military grade part in a 28-pin ceramic DIP and is priced at £22.27 (100). The ZN504 is available in a 28-pin ceramic or plastic DIP.

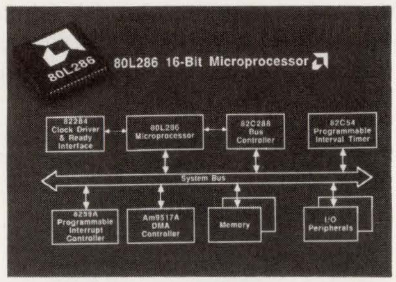
ZN503, £22.27; ZN504 ceramic, £14.18; ZN504 plastic, £9.45 (100).

Ferranti Electronics Ltd, Fields New Rd, Chadderton, Oldham, Lancashire OL9 8NP, UK. Phone 061-624 0515. TLX 668038.

Circle No 381

Ferranti Electric Inc, 87 Modular Ave, Commack, NY 11725. Phone (516) 543-0200. TLX 6852104.

Circle No 382



LOW-POWER 80286 μP

- *Operates at 12.5 MHz*
- *Dissipates 2.2W at 55°C*

The 80L286 is a low-power version of the standard 16-bit μP. It consumes 2.2W (30% less than the standard) and comes in 8-, 10-, and 12-MHz versions. Like the 80286, the 80L286 is compatible with software written for the 8086 and 8088 μPs. The company offers support peripherals for the 80L286, as well as the standard 80286. In 12.5-MHz, 68-pin plastic leaded-chip carrier, $100 (100).

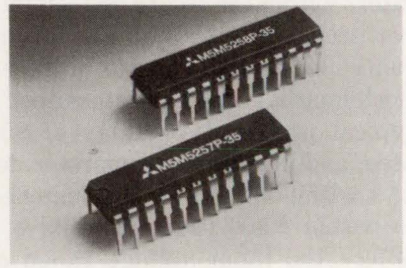
Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 383

CMOS STATIC RAMs

- *256k×1- or 64k×4-bit organizations*
- *Feature 35-nsec access time*

The 35-nsec M5M5257 (256k×1-bit) and M5M5258 (64k×4-bit) are the fastest 256k-bit static RAMs available, according to the manufacturer. Combining silicon-gate CMOS peripheral logic and a high-density



NMOS memory array, the devices are suitable for use in cache and main-memory applications. Both chips are also available in 45- and 55-nsec versions. They come in 300-mil, 24-pin plastic DIPs or plastic SOJ (small-outline J) packages for surface-mount applications. 35-nsec M5M5257P in DIP, $142; M5M5258P, $152 (100).

Mitsubishi Electronics America Inc, 1050 E Arques Ave, Sunnyvale, CA 94086. Phone (408) 730-5900.

Circle No 384

DUAL-PORT RAM

- *Organized as 512×9 bits*
- *Features a separate interrupt output for each port*

The MK4511 512×9-bit dual-port RAM features independent interrupt outputs for each port, which you can software control via two interrupt registers. Each port, which operates with multiplexed address/data, can simultaneously access RAM locations. The RAM is available with access times of 120, 150, or 200 nsec. The MK4511 is supplied in a 28-pin DIP or 28-pin plastic leaded chip carrier. From $9.56 to $12.65 (1000), depending on access-time rating.

Thomson Semiconducteurs, 45 Ave de l'Europe, 78140 Velizy, France. Phone (1) 39469719. TLX 204780.

Circle No 385

Thomson Components-Mostek Corp, 1310 Electronics Dr, Carrollton, TX 75006. Phone (214) 466-6000. TLX 730643.

Circle No 386

THE ANSWER IS IN TEK DIGITAL STORAGE:

$2995
$3995
$4995

Now! The new 60 MHz Tek 2221 joins the world's best-selling family of digital storage oscilloscopes. All featuring 20 MS/s *digitizing* along with familiar, full-bandwidth analog operation. It's the best of both worlds in an easy-to-use portable.

Discover the potential. With digital storage you can freeze waveforms. Capture events invisible to nonstorage scopes. Find signals buried in noise. And build a library of reference waveforms.

Digital storage display accuracy enhances your confidence in measurements. And all you have to do is push a button for *real-time* display analysis.

Compare the 2230, 2221 and 2220 to each other—and all others. The new 2221 offers such advanced features as CRT readout and measurement cursors. For even more performance and flexibility, there's the 100 MHz, dual time base 2230 with optional battery-backed memory for saving up to 26 waveform sets. And if it's economy you want, choose the 60 MHz 2220 with many of the same features at an even lower cost.

With each scope you can capture events as narrow as 100 ns at any sweep speed thanks to Tek's proprietary peak detect mode. View events prior to or following a trigger event with pre/post trigger. Store waveforms into 4K records. Automate measurements with optional GPIB and RS-232-C interfaces. And output direct to a printer or plotter.

Tek software is available to help you make the most of the 2230, 2221 and 2220 in system configurations.

Features	2230	● NEW! 2221	2220
Analog/Digital Storage BW	100 MHz	60 MHz	60 MHz
Maximum Sampling Speed	20 MS/s	20 MS/s	20 MS/s
Record Length	4K/1K (selectable)	4K	4K
Peak Detect	100 ns	100 ns	100 ns
Save Reference Memory	One, 4K Three, 1K	One, 4K	One, 4K
Vertical Resolution	8 bits 10 bits (AVG mode) 12 bits (AVG mode over the bus)	8 bits 10 bits (AVG mode)	8 bits
CRT Readout/Cursors	Yes	Yes	No
GPIB/RS-232-C Options	Yes ($750)	Yes ($500)	Yes ($500)
Battery-Backed Memory (save 26 waveform sets)	Yes (inc with GPIB/ RS-232-C)	No	No
Price	$4995	$3995	$2995

Call Tek for a free video brochure or to place an order.

Ask about free digital storage application notes and educational materials. Orders include complete documentation, manuals and 3-year warranty on labor, parts and CRT.

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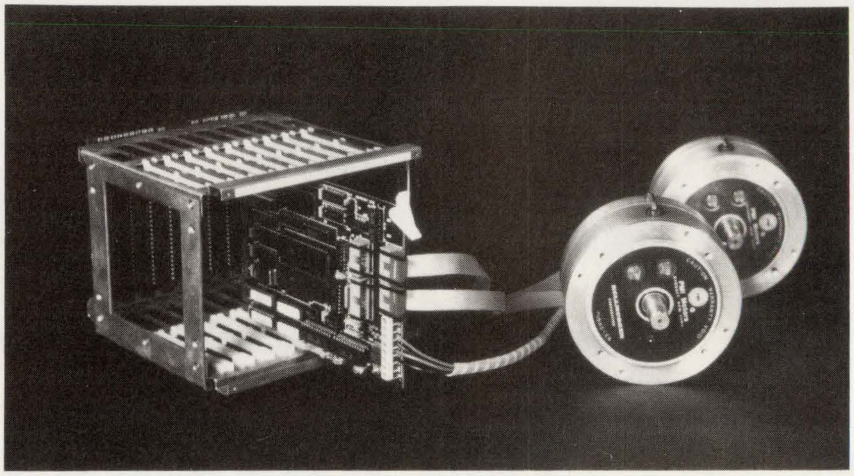
COMMITTED TO EXCELLENCE

NEW PRODUCTS

COMPONENTS & POWER SUPPLIES

MOTOR CONTROLLER

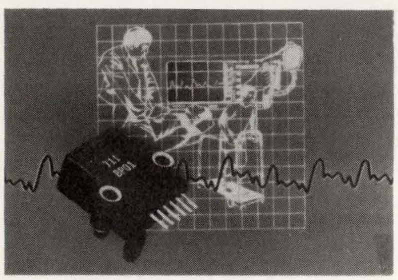
- *Controller is STD Bus compatible*
- *Offers four modes of position and velocity control*



The Model 4327 motor controller is STD Bus compatible. It intelligently controls two dc brush-type servo motors. It offers four modes of position and velocity control and provides programmable velocity and acceleration profiling. The controller features two channels for feedback from TTL-level incremental encoders for each axis of control, and a 24-bit counter keeps track of the motor position. The controller also provides inputs for two limit or stop signals per axis. Onboard amplifiers supply as much as 2A of pulse-width-modulated output. One axis, $435; two axes, $550.

Technology 80 Inc, 658 Mendelssohn Ave N, Minneapolis, MN 55427. Phone (800) 328-4827; in MN, (612) 542-9545.

Circle No 387



PRESSURE SENSOR

- *Calibrated for the normal blood-pressure range*
- *Maximum tolerance of ±1%*

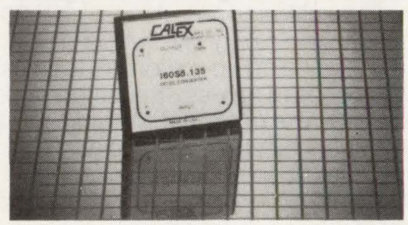
The BP01 noninvasive pressure sensor is fully temperature compensated and calibrated to operate over the normal blood-pressure range, 0 to 300 mm of mercury. It has a 6-mm max zero-pressure offset, a 0.2-mm/°C shift over temperature (from 10 to 50°C), a ±1% guaranteed tolerance, and a maximum 0.2% of FSO (full-scale output) linearity. The span change over temperature is ±0.02% FSO/°C max. In addition, the 4-kΩ impedance minimizes power dissipation, making the sensor compatible with portable or battery-backup medical equipment. The BP01 is housed in a glass-filled nylon case that is pc-board mountable; it features barbed pressure ports that can accommodate standard medical-grade tubing. $25 (OEM qty).

Sensym Inc, 1255 Reamwood Ave, Sunnyvale, CA 94089. Phone (408) 744-1500.

Circle No 388

I/V CONVERTER

- *Designed for the Bell 113T1 repeater current loop*
- *Six-sided shielded case eliminates RFI problems*



The Model I60S5.135 I/V converter is designed to operate with the Bell 113T1 repeater current loop and is completely compatible with paragraph 7 of those requirements. It operates from the Bell 60-mA current loop and generates 5V at 135 mA to operate logic circuits in telephone test systems or alarms. You can also use the isolated 5V output as a source of −5V for applications requiring multiple supply levels or isolated power for a meter. The unit has a 6-sided shielded case that eliminates RFI problems; an internal filter that minimizes current-noise feedback into the current loop; and a post-regulator stage and filter that provides a clean, low-noise output. $95.

Calex Mfg Co Inc, 3355 Vincent Rd, Pleasant Hill, CA 94523. Phone (415) 932-3911.

Circle No 389

TRANSISTORS

- *Suitable for use in off-line switch-mode power supplies*
- *Eliminate the need for snubber components in some uses*

The SGSF323 and SGSF463 bipolar

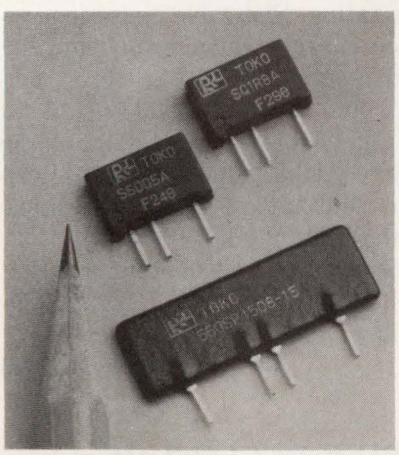
transistors have voltage ratings of 1000V and 1300V, respectively, so they eliminate the need for snubber components in many applications. The SGSF323 is suitable for use in power supplies switching between 50 and 75 kHz. In forward-converter circuits, it can produce output power as high as 180W with minimal power dissipation. In the normal base drive configuration, the SGSF463 has a fall time of 50 nsec and a storage time of 700 nsec. In flyback converter circuits, however, you can decrease the storage time to 300 nsec, without affecting the fall time, by performing switching in the emitter circuit with an SGSP362 power MOSFET. SGSF323, $0.60; SGSF463, $1.30 (10,000).

SGS Microelettronica SpA, Via C Olivetti 2, 20041 Agrate Brianza, Italy. Phone (039) 65551. TLX 330131.

Circle No 390

SGS Semiconductor Corp, 1000 E Bell Rd, Phoenix, AZ 85022. Phone (602) 867-6100. TLX 249976.

Circle No 391



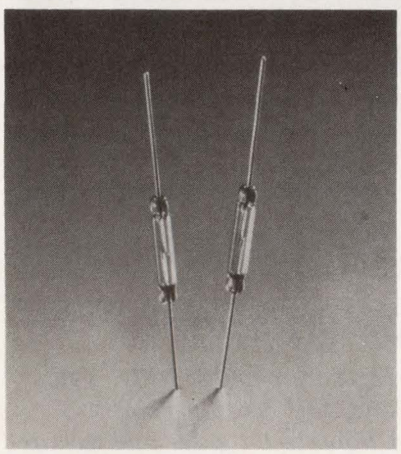
DELAY LINES

- *Offer delays to 0.1 nsec*
- *Suitable for ECL computer applications*

The SP, SQ, and SS Series delay lines offer delay capabilities ranging from 0.1 nsec and are suitable for ECL computer applications. The total delay times for SP units start at 0.1 nsec±0.05 nsec and step in 0.1-nsec increments to 1.7 nsec. The delay times for SQ units start at 0.2 nsec±0.1 nsec and increment by 0.2-nsec intervals to 2 nsec max. The total delay times for SS Series devices range from 1 to 5 nsec in 1-nsec increments. All the parts feature 55Ω impedance, 10% max waveform distortion, 1Ω max dc resistance, and 100-MΩ min insulation resistance. SP Series, from $1.73; SQ and SS Series, $4.68 (1000).

Toko America Inc, 1250 Feehanville Dr, Mount Prospect, IL 60056. Phone (312) 297-0070. TLX 724372.

Circle No 392



REED SWITCHES

- *Available with load power ratings as high as 25W*
- *Feature low contact resistance and long lifetime*

The RI-25 line of micro dry reed switches includes devices with maximum load-switching capabilities of 8, 15, and 25W. However, the switches can also handle load powers as low as 300 mW. They can withstand a voltage of 200V dc or 140V ac and can switch a maximum current of 1A into a resistive load. The reed switches have normally open spst contacts with operating magnetic fields of 8 to 16 At for the 8W switch and 46 to 70 At for the 25W switch. The corresponding release fields are 4 to 14 At and 16 to

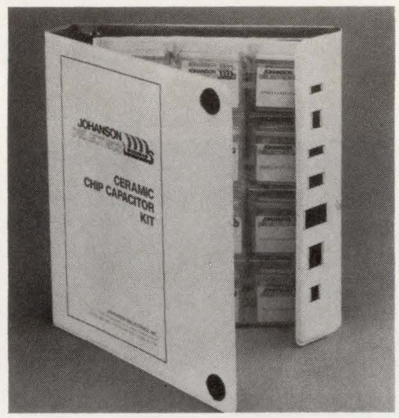
32 At. The initial contact resistance is 70 mΩ typ; it stays close to this value over 10^9 switching operations. The 8W version costs approximately gld 0.5 in volume quantities.

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 393

Amperex Electronic Corp, Box 560, Hicksville, NY 11802. Phone (516) 931-6200.

Circle No 394



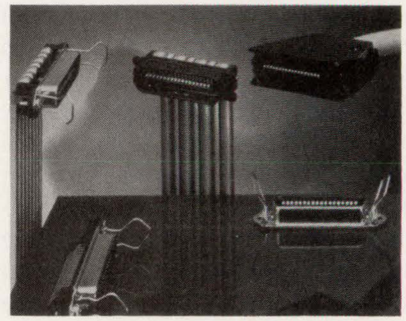
CAPACITOR KIT

- *Includes popular NPO, X7R, and Z5U ceramic chips*
- *Chip-selector guide and technical manual provided*

S-920 SMT prototype kits include the most popular values of NPO, X7R, and Z5U multilayer ceramic-chip capacitors. The kit, which is packaged in a special vinyl cover for shelf storage, includes 550 devices in the most popular capacitance values and in sizes 0805 and 1206. Each unit has nickel barrier terminations, and each is individually packed for easy access and immediate identification. The kit also includes a chip-selector guide and a 24-pg technical manual, which discusses the proper application of chip capacitors. $95.

Johanson Dielectrics Inc, 2220 Screenland Dr, Burbank, CA 91505. Phone (213) 848-4465. TWX 910-498-2735.

Circle No 395



CONNECTORS

- *Feature a 3A current rating*
- *Accept standard 28 AWG flat cable*

The DL 50 Series ribbon connectors utilize 0.085-in. centerline contacts on both the mating end and the pc-board interface. They accept standard 28 AWG flat cable, which is terminated by the insulation-displacement method. The connectors are available in 24-, 36-, and 50-position sizes. The series offers metal-shell straight and right-angle receptacles with ball locks, as well as mating plugs and receptacles for use with 0.050-in.-center cables. The connectors spec a 3A current rating; the receptacles have a 500V ac voltage rating. Flat-cable limitations reduce current ratings for the plug and receptacles to 1A. Three contact options are available (8, 15, or 30 μin. of gold over nickel) for all the devices. $3.23 (1000) for a 24-position right-angle pc-board receptacle with 8 μin. of gold.

Molex Inc, 2222 Wellington Ct, Lisle, IL 60532. Phone (312) 969-4550.

Circle No 396

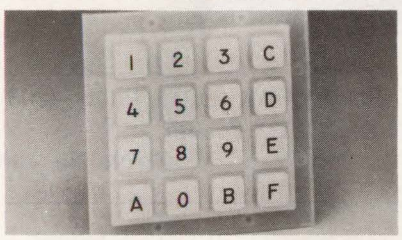
DRIVE ENCLOSURE

- *No tools needed for drive installation*
- *Includes a 100W power supply*

The SA-H163 enclosure is designed for applications that require removing, transporting, and storing dual 5¼-in. Winchester disk drives. It features pluggable drive capability along with a removable bracket (complete with power and data connectors) that you install on each drive. To remove a drive, you simply loosen two thumbscrews on the hinged cover, pull the handle on the bracket, and release the drive assembly from the docking connector. No tools are required for drive installation or removal. The enclosure also includes a 100W supply, exhaust fan, write-protect switches, and LED indicators for each drive. The front-panel connectors provide daisy-chaining capability for the controllers that support as many as four Winchester disk drives. $1431.

Sigma Information Systems, 3401 E LaPalma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

Circle No 397



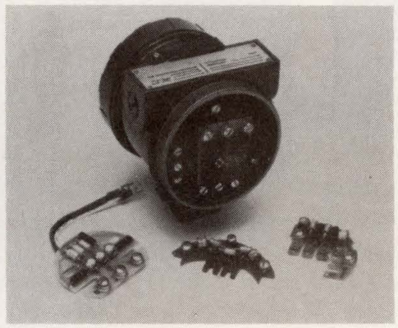
KEYPADS

- *Can stand up to severe environmental conditions*
- *Keypads have a life of 10 million operations*

These Sealedswitch keypads are designed to withstand severe environmental conditions and are available in industrial and military versions. The 3×4- and 4×4-in. models feature a 1-piece silicone rubber boot, which wraps around the pc board to form a complete seal when mounted. Switch legends, characters, or symbols are diffused into the key surface, making the entire front panel highly resistant to the effects of solvents, oils, most chemicals, heat, ultraviolet radiation, and scratching. The keypads' electrical specs include a 50-mA/28V dc contact rating, a 10-msec max bounce time, 1Ω max contact resistance, and 10-MΩ min insulation resistance. The mechanical specs include a life of 10^6 operations, a 400g actuation force, and 0.02-in. key travel. The military versions meet or exceed the requirements of MIL-STD-810. $40.75 and $50.15 (100) for industrial and military 4×4-in. units, respectively.

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 398



SUPPRESSORS

- *Designed to protect analog control-loop transmitters*
- *5-μA max standby current*

The 420T and 423T transient voltage suppressors are designed to protect temperature and pressure transmitters in analog control loops. These field-installable parts are capable of protecting almost all popular transmitters. Available in four standard models, they provide line-to-line and line-to-ground protection. All of them include devices with maximum operating line voltages of ±25, ±28, ±36, ±50, and ±60V; the respective maximum line-to-ground clamping voltages for these parts are 44, 46, 60, 80, and 95V. They also feature a short-circuit failure mode that provides maximum protection. All the parts have automatic reset. The maximum standby current is 5 μA, and the operating range spans −55 to +100°C. From $40 (100).

General Semiconductor Industries Inc, 2001 W Tenth Pl, Tempe, AZ 85281. Phone (602) 968-3101. TWX 910-950-1942.

Circle No 399

CAE & SOFTWARE DEVELOPMENT TOOLS

FORMAT CONVERTER

- *Converts waveform data to any of nine formats*
- *Runs on IBM PCs and compatibles*

The R900 Universal File Transfer software runs on IBM PCs, PC/XTs, PC/ATs, and compatible computers equipped with the vendor's data-acquisition or digital-oscilloscope interface boards. You load the R900 UFT software after acquiring a waveform or other real-time data (via one of the vendor's products) and storing the data on disk. The menu-driven UFT software can translate your data into a number of different formats for further processing and analysis. You can currently select the formats for Asyst, Asystant, DADiSP, dBASE III, ILS-PC1, ILS-PC2, Labtech Notebook, Lotus 1-2-3, or MathCAD. $199.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103. Phone (206) 547-8311. TLX 265017.

Circle No 400

μP SIMULATOR

- *Simulates Clipper μP bus cycles*
- *Lets you verify timing of system hardware designs*

The Clipper SmartModel is a software package that runs on workstations from Mentor Graphics (Beaverton, OR). The software provides a model of the CPU, FPU, and Cache/MMU logic contained in Fairchild's Clipper C100 32-bit μP. With the aid of simple commands that control the model, hardware designers can simulate bus cycles, timing sequences, interrupt processing, and reset processing at the full speed of the μP. Thus, you can repeatedly modify and verify your design without the expense of developing a wire-wrapped prototype board and assembly-language code to exercise it. This hardware-verification model costs $2500; a full-function version that will execute assembly-language instructions is under development.

Logic Automation Inc, 19545 NW Von Neumann Dr, Beaverton, OR 97006. Phone (503) 690-6900.

Circle No 401

MAP NETWORK TOOL

- *Monitors network performance and collects statistics*
- *Stores and displays message frames*

The token-bus frame analyzer (TBFA) is a software package that monitors token-bus-network performance in real time and lets you collect and store statistics relating to the traffic. You can select any type of ISO (International Organization for Standardization) message header or any segment of the medium-access-control layer as the trigger that initiates data collection. Because the TBFA is not part of the token-passing logical ring, it is transparent to all network operations and does not interfere with them in any way. The software resides in four PROMs located on the vendor's MVME372 MAP interface module board; in this application, the board operates as a stand-alone processor and requires no backplane bus. The only other items required are a DEC VT100 or equivalent terminal, a modem that matches the network, and a power supply. $2500.

Motorola Inc, Box 52073, Phoenix, AZ 85072. Phone (512) 440-2140.

Circle No 402

16M BYTES FOR PC/AT

- *C and assembly-language programs address 16M-byte RAM*
- *Allows programs to run in protected mode*

DOS/16M is a software package that lets C and assembly-language programs, running on an IBM PC/AT or compatible machine, address as many as 16M bytes of RAM. The package consists of a run-time library, which contains routines for managing extended memory and for starting and running programs in 80286 and 80386 protected mode under PC-DOS version 3. It also contains a symbolic debugger for protected-mode programs and source code for the run-time library and start-up code. When you use DOS/16M, it adjusts your program for protected-mode addressing, then switches the computer into protected mode before starting to execute the adjusted program. DOS/16M switches the computer back to real mode whenever it needs to service DOS or BIOS system calls or when it must service interrupt requests from devices that don't have protected-mode interrupt handlers. You don't need to rewrite or recompile your programs in order to use DOS/16M; you need only to relink them with the run-time library. You may also have to modify any arithmetic operations that your program performs on segment register values, and any parts of your program (such as interrupt handlers) that write into code segments of memory. $29,000.

Rational Systems Inc, Box 480, Natick, MA 01760. Phone (617) 653-6194.

Circle No 403

CASE TOOL

- *Creates modular, function, and structure charts from a database*
- *Supplements the information from the Modular Design tool*

ProMod/SC automatically creates graphics structure charts from software-design data developed with the aid of the vendor's ProMod/MD CASE tool. The tool can create three types of charts: modular network, function network, and function structure charts. Modular network charts show the connections between major system structures. Function network charts identify the import, internal, and export functions of the system. Function structure charts show conditional or repetitive calls of a function from the main program, multiple calls from one function to another, and recursive functions. Where appropriate, the graphics linkages show the data types of parameters that are passed over the linkages. You can display the charts on the screen and edit them, or you can send the charts to a pen plotter or laser printer. IBM PC version, $500; VAX system version, $1000.

Promod Inc, 23685 Birtcher Dr, Lake Forest, CA 92630. Phone (714) 855-3046.

Circle No 404

TEST & MEASUREMENT INSTRUMENTS

8051 EMULATOR

- *Emulator runs at 12 MHz*
- *Works with NMOS and CMOS versions*

The EC 7000/8051 works with all members of the 8051 family, including the 8051, 8052, 8031, 8751, and 8752. It handles NMOS and CMOS versions. The emulator runs at 12 MHz with no wait states. It features 64k bytes of emulation program memory and 64k bytes of emulation data memory; you can set a breakpoint on each program-memory location. The unit has a 4k×48-bit trace memory and a time stamp with 1-μsec resolution. For control, the emulator requires an IBM PC, PC/XT, PC/AT, or compatible computer. $5800.

Applied Microsystems Corp, 5020 148th Ave NE, Box 97002, Redmond, WA 98073. Phone (800) 426-3925; in WA, (206) 882-2000. TLX 185196.

Circle No 406

LEVEL TRANSLATOR

- *Programmable level translator accepts TTL input*
- *Output compatible with GaAs, ECL, TTL, and CMOS devices*

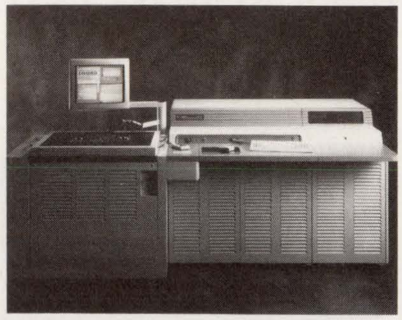
The PI-6800 programmable level translator accepts TTL-level input signals and translates them into output that is compatible with GaAs, TTL, CMOS, and ECL devices. The translator's output repetition rate is 100 MHz max and its rise times are 2.5 nsec min. The device accommodates as many as eight pc boards, and each board provides eight output channels. The output voltage range is −5V to +10V (−0.4 to +5V into 50Ω) with 10-mV resolution. The unit has a built-in CRT and is programmable over the IEEE-488 and RS-232C interfaces. $6000 to $13,500. Delivery, eight weeks ARO.

Pulse Instruments, 1234 Francisco St, Torrance, CA 90502. Phone (213) 515-5330.

Circle No 407

BOARD TESTER

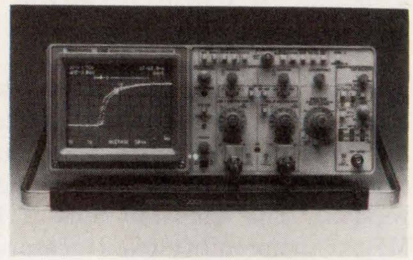
- *Performs short-circuit, in-circuit, and functional tests*
- *Software generates some tests automatically*



The GR2750 board-test system has a 32-bit CPU. Each pin of the tester can perform analog, digital, functional, or in-circuit tests. Pins provide digital test rates to 10 MHz (20 MHz multiplexed). Every pin possesses a 16k×4-bit memory (32k×4 bits max). The ATE can generate clock signals to 50 MHz and synchronize with external clock signals to 40 MHz. It can also scan eight analog channels at 10 MHz or four channels at 50 MHz max. The system's software automatically generates pc-board short-circuit tests and in-circuit tests for analog and digital components; the software includes the HILO simulator. $600,000 to $1,000,000. Delivery, 90 days ARO.

GenRad Inc, 300 Baker Ave, Concord, MA 01742. Phone (617) 369-4400.

Circle No 408



DIGITIZING SCOPE

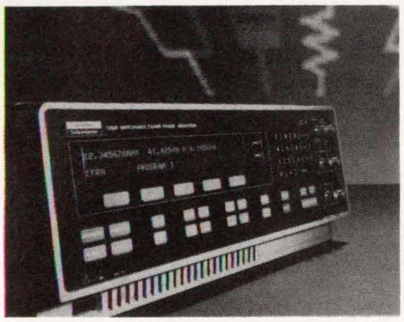
- *Combines digitizer with analog scope*
- *Drives X/Y plotter directly*

The 2221 oscilloscope combines a 60-MHz analog oscilloscope with a 20M-sample/sec digitizer. The digitizer can store 4096 8-bit samples in single-channel mode or two 2048-

sample records in dual-channel mode. The scope can record 100-nsec glitches. In the so-called envelope mode, it can also display the maximum and minimum excursions of a repeated waveform. The scope drives an X/Y plotter directly; IEEE-488 and RS-232C interfaces are optional. $3995.

Tektronix Inc, Box 500, Beaverton, OR 97077. Phone (800) 426-2220; in OR, (503) 627-9000.

Circle No 409



ANALYZER

- *Measures impedance and frequency response*
- *Interfaces to component handlers for batch sorting*

The Model 1260 impedance/gain-phase analyzer measures the impedance of components or electronic circuits and measures their frequency response over the range from 10 μHz to 32 MHz. The instrument digitizes input signals to 15-bit resolution on two independent voltage channels and one current channel. It employs a single-sine-correlation technique to provide fast and precise measurement of both amplitude and phase. Its overall frequency-response accuracy is 0.01 dB. You can perform frequency, amplitude, or bias sweeps by using the instrument's built-in voltage and current generators. Its post-measurement processing includes normalization of measured parameters or limit checking against simple or complex limit values. The unit comes with IEEE-488 and RS-232C interfaces, so you can control the unit remotely and obtain hard-copy printouts of the results. Battery-backed RAM provides nonvolatile storage for as many as nine test programs, and you can protect six more EEPROM-resident test programs with a key-switch. £11,500.

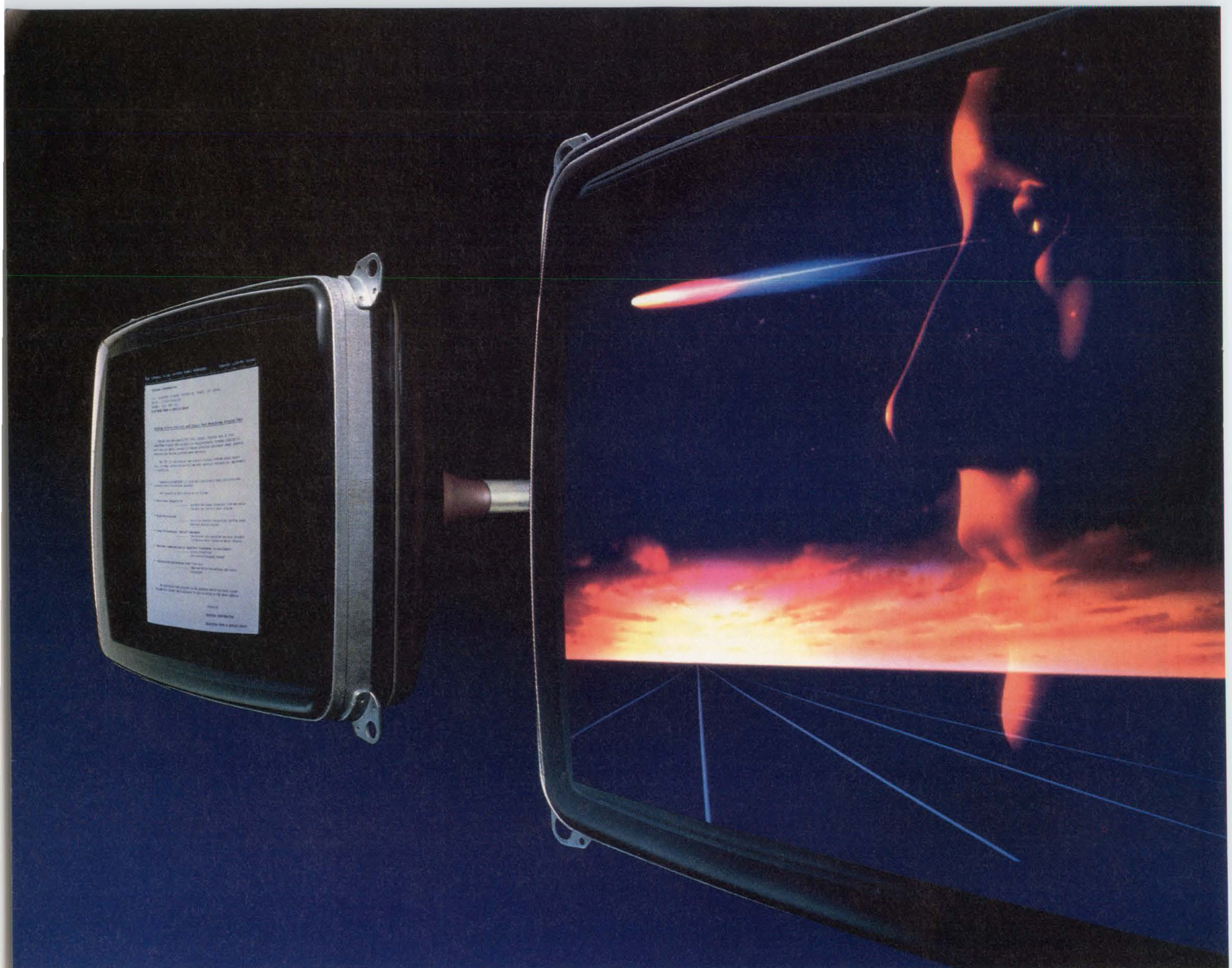
Solartron Instruments, Victoria Rd, Farnborough, Hampshire GU14 7PW, UK. Phone (0252) 544433. TLX 858245.

Circle No 410

Solartron Instruments Inc, 2 Westchester Plaza, Elmsford, NY 10523. Phone (914) 592-9168. TLX 145487.

Circle No 411

 CIRCLE NO 52



Ergonomic Engineering Reaches a New Height With a Flat Screen and Invar Mask Equipped Display Tube

Toshiba, always in pursuit of greater clarity in displays, has changed the concept of display tube technology. The FS tube was born of our quest for improved ergonomic engineering. It is not only Flat and Square, but it now has an Invar Mask. The results are clarity, brightness and reduced ambient light reflection for fatigue-free viewing. The Toshiba FS display tube also boasts high reliability and high quality and comes in a wide lineup to meet virtually any OA equipment need.

WIDE LINEUP

		Screen dot pitch (mm)	Display area (mm)	Display capability (pixels/line)	Faceplate radius (mm)
9″ (7.5V) FS	E8075**	0.28	140 × 105	460	900
10″ (9V) Conventional	E2957	0.28	170 × 130	580	495
13″ (12V) FS	E8046/E8077	0.36/0.28	230 × 170	590/760	1100
12″ (12V) Conventional	E8001/E8032	0.36/0.28	220 × 160	560/720	647
15″ (14V) FS	E2995/E2994	0.39/0.31	260 × 190	610/770	1200
14″ (13V) Conventional	E2971/E2894	0.39/0.31	250 × 180	590/740	575
17″ (16V) FS	E8162	0.26	300 × 220	1060	1370
16″ (15V) Conventional	E2864	0.31	290 × 210	820	653
21″ (20V) FS	E8142/E8170*	0.42/0.31	370 × 280	810/1100	1730
20″ (19V) Conventional	E2862	0.31	360 × 270	1000	820

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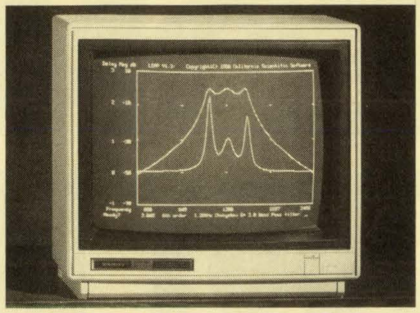
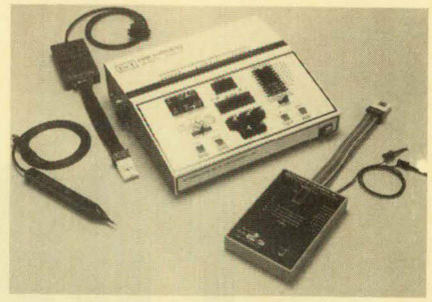


NEW ENGINEERING SOFTWARE

Filter designs active filters up to order 30. Bessel, Butterworth, Chebyshev, Allpass; High, Low Bandpass and Bandstop. Fully menu driven, Filter designs, plots, and selects component values for any filter in seconds. **LSAP analyzes linear systems** producing Bode, Nyquist, Impulse, Step Response and Root-Locus plots. **Micro-CSMP simulates control and servo systems** with full support for non-linear behavior. Filter is $750, LSAP is $450, Micro-CSMP is $900 for the IBM PC.

California Scientific Software
1159 North Catalina Ave, Pasadena, CA 91104
(818) 798-1201

CIRCLE NO 332



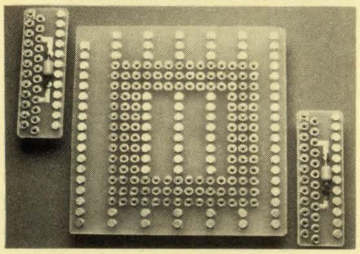
INSTRUMENT PAIR FOR IC IN-CIRCUIT TESTING

M-5700C Logic Scanmaster includes universal logic state indicator, logic pulser and clip, automatic bad level detector, auto-ranging DVM, pin to pin push-button interface of the signal to scope, counter, etc. M-150 Digital Comparator compares known good IC to DUT in-circuit. This instrument combination offers fast, accurate process to troubleshoot digital ICs to component level. Price $1,695.00

Information Scan Technology
487 Gianni Street, Santa Clara CA 95054
(408) 988-1908

CIRCLE NO 333

PGA & LCC PROTOTYPE



TEST ADAPTORS – VLSI

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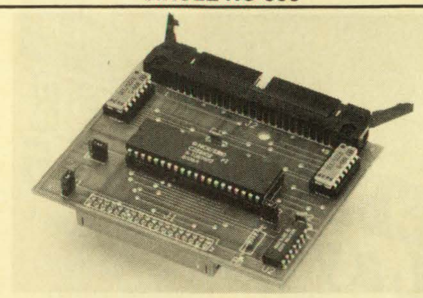

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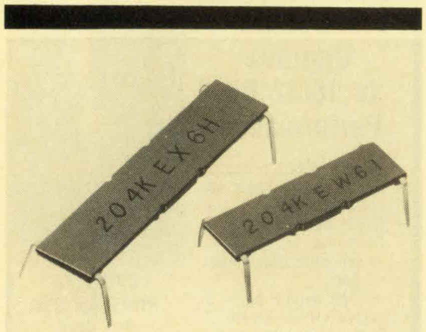

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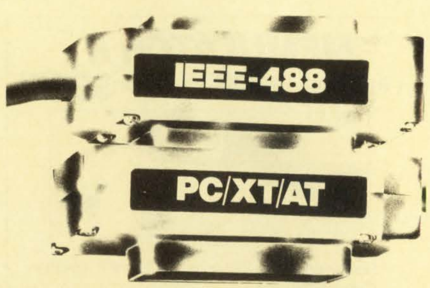

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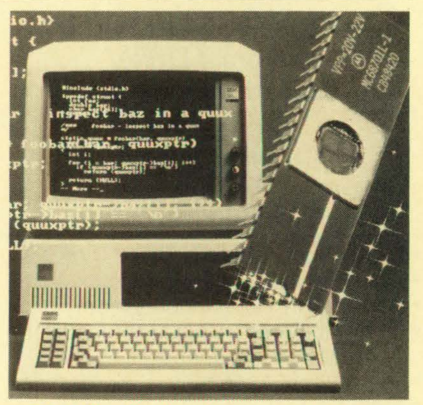

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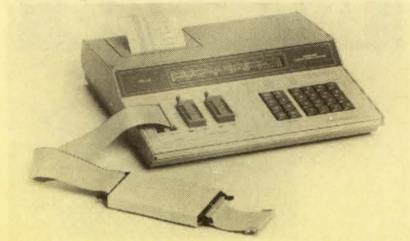

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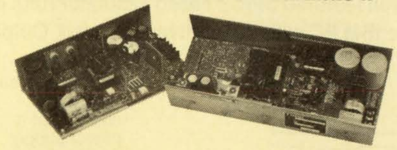

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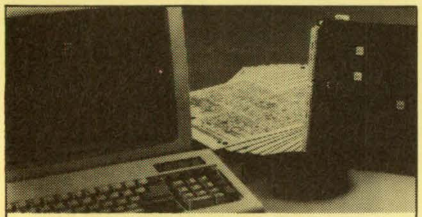

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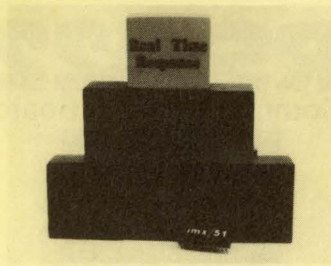

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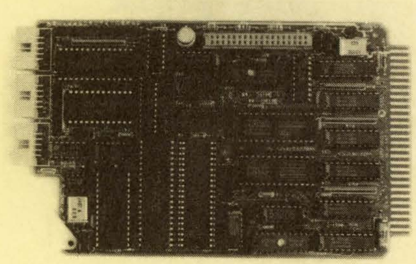

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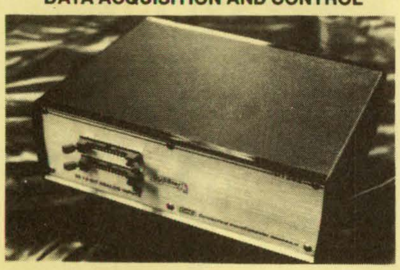

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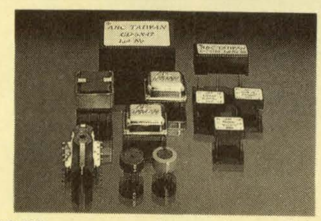

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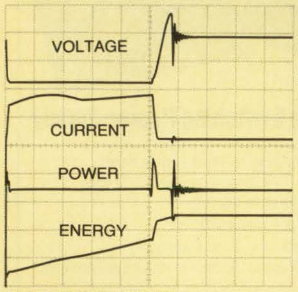

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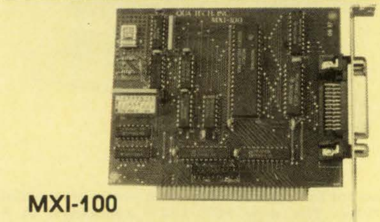

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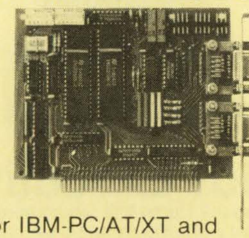

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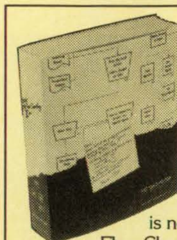

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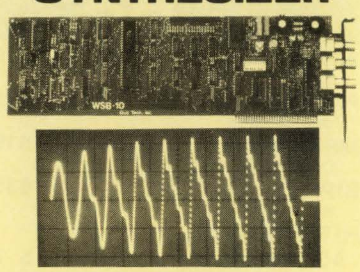

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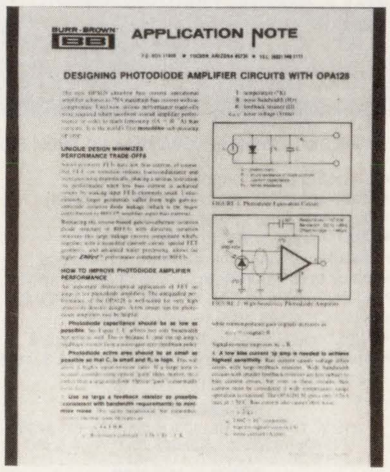

Note on amplifier circuit design

The 2-pg application note AN-151, *Designing Photodiode Amplifier Circuits with OPA128*, explains how to minimize the tradeoffs and improve the performance when designing photodiode amplifier circuits. Specific topics include photodiode capacitance, feedback and diode shunt resistance, photovoltaic vs photoconductive modes, shielding, and oscillation suppression.

Burr-Brown, Box 11400, Tucson, AZ 85734.

Circle No 414

IC solutions for communications

The 1987-1988 IC Product Handbook provides technical descriptions and application notes for more than 20 ASICs, including eight new products. It lists analog speech scramblers, delta modulation codecs, 1200-baud min shift-key modems, switched-capacitor filters, selective calling devices, and encoders/decoders. Illustrations, tables, figures, and schematics help to clarify the product descriptions.

MX-Com Inc, 4800 Bethania Station Rd, Winston-Salem, NC 27105.

Circle No 415

Fiber-optic measurements

The 25-pg booklet, *How to Make Accurate Fiber Optic Power Measurements*, contains six sections. The introduction presents the current status of fiber optics, the measurements of optical power, and the company's HP8152A power meter. The next two sections deal with accuracy limits due to the detector and amplifier and accuracy limits due to coupling methods. Sections on nonreproducibility caused by the fiber and the source, standards and calibrations, and literature complete the presentation. Also included are figures, tables, and 3-D examples.

Hewlett Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.

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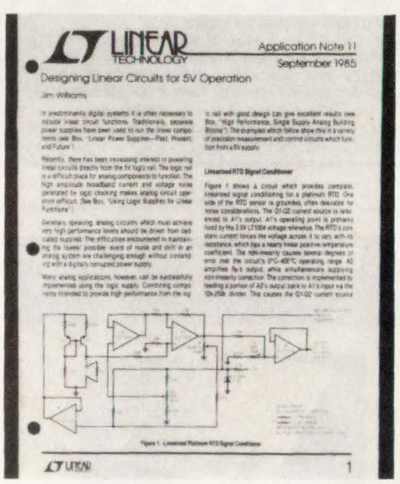

App note describes analog-circuit design

The 16-pg application note, *AN-11: Designing Linear Circuits for 5V Operation*, provides circuit schematics and descriptions of various linear functions that can be incorporated with digital functions on a pc board, using a common 5V supply. The applications discussed include a linearized-platinum signal conditioner; a linearized-output methane detector; a cold-junction, compensated thermocouple signal conditioner; an instrumentation amplifier; and a strain-gauge signal conditioner. Other applications described include a tachless motor-speed controller, a 4- to 20-mA current-loop transmitter (with a floating-point option), an isolated limit comparator with a gain of 100, and an isolated A/D converter.

Linear Technology Corp, 1630 McCarthy Blvd, Milpitas, CA 95035.

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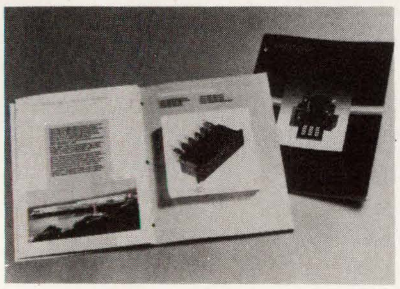

Listing of digital switches

This catalog describes a wide range of switches, including Digiswitch, Minilever, Digivider, and Digidecade switches, as well as Minikey keypad systems. Its easy-reference format guides you through military and commercial switch selection and includes a feature and options chart, truth tables listed by product series, engineering parameters, and layout drawings. It covers thumbwheel switches, lever/toggle switches, pushbutton switches, special-custom products, accessories, and switch-and-assembly ordering instructions.

Digitran, 3100 New York Dr, Pasadena, CA 91107.

Circle No 418

Report explains reliability testing

Product Reliability Report, RR-1C, describes the steps the vendor has taken to reach new reliability standards for analog and data-conversion products. The procedures and material presented in the 7-pg report are based on an audit by the accounting firm of Coopers & Lybrand. The two tutorials included in the report present the theory behind the computation of an acceleration factor and the determination of a failure-in-time rate.

Maxim Integrated Products, 510 N Pastoria Ave, Sunnyvale, CA 94086.

Circle No 419

How to create a mouse menu program

The *Microsoft Mouse Programmer's Reference Guide* explains how to write mouse menu programs and how to design a mouse interface for the applications you write. The guide has two main sections. The first section tells you how to create a mouse menu program that allows you to use the vendor's mouse with an application that doesn't have built-in mouse support. The second part explains how to build mouse support directly into one of your own applications. The guide also contains the tools and technical information you need to make direct calls to the driver. $25.

Microsoft Corp, Box 97017, Redmond, WA 98073.

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Coaxial products catalog

Catalog #587 is a 29-pg listing that features a full line of coaxial adapters, connectors, attenuators, terminations, and cable assemblies. The newly featured line of coaxial attenuators includes BNC, "N", SMA, and TNC. Both flexible and semirigid cable assemblies are available. It includes technical specifications and pricing for more than 1000 standard catalog items.

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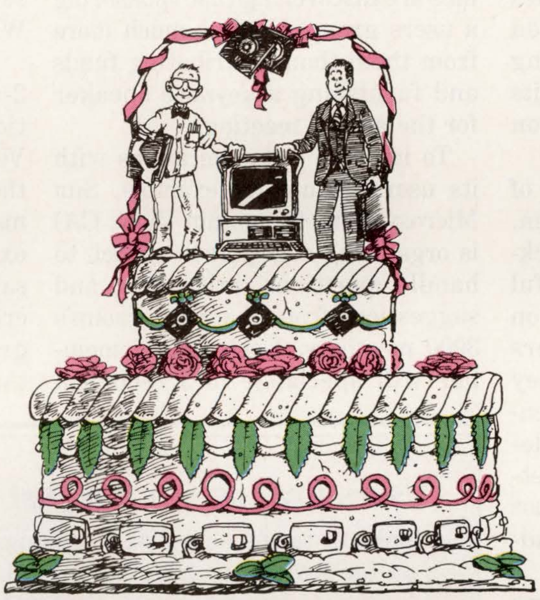
Users groups and their vendors:

The ins and outs of a partnership

Deborah Asbrand, *Associate Editor*



Jon McIntosh

Simon Favre, a modeling engineer for LSI Logic, cites three reasons for belonging to the Mentor Graphics Users Group, which is called MUG. First, he finds the exchange of information with other users of Mentor Graphics' workstations fruitful, and he also enjoys such membership benefits as the group's software exchange.

The third of Favre's reasons for belonging to MUG is perhaps the most important: MUG membership gives him the chance to influence the development of Mentor Graphics products—something he would not be able to do as an isolated, individual user. "If you get 200 people at a users-group meeting who say they don't like something, Mentor will sit up and take notice," says Favre, who runs Mentor's Idea Station software on the Apollo DN 3000.

Many members of other users groups agree on the relatively weak impact of the lone voice. "Requests from an individual user don't carry much weight," says David Austin, manager of computer-aided design at Integrated Technology Corp (ITC) in Tempe, AZ, and a member of an organization for users of Cadnetix Corp's CAE workstations. "As a result, the group is the only way that users can effectively communicate what they want in terms of new features."

Users of PC-level equipment are often attracted to general-purpose computing groups by their regular meetings and the chance to swap tips and software. But users of higher-level machines want much more. Engineers want users groups to open the door to discussions with the manufacturers' engineers about the current crop of products and the design decisions behind them as well as features planned for the next generation of products.

Nurturing a happy relationship between a manufacturer and the engineers who use its equipment, however, can be tricky. "It's a courtship and marriage type of situation," says Stan Nissen, MUG president. Indeed, after easily agreeing that some form of partnership is a good idea, a vendor and its users group must then tackle the more difficult tasks of managing two often differing sets of opinion, communicating regularly, and maintaining their independence.

Manufacturers and customers alike agree that users groups are beneficial. For manufacturers, sponsoring a users group provides a handy source of reference for design and marketing questions. It can also take the pressure off customer-support services. For users, the group

Nurturing a happy relationship between a manufacturer and the engineers who use its equipment can be tricky.

provides an educational and practical outlet for the exchange of ideas, tips, and materials.

Opinions on how a users group should operate, though, often diverge. Mentor Graphics users group appeared from the company's viewpoint to be a successful effort. In addition to regularly held regional and national meetings, MUG issues a monthly publication, called "Mugazine," that lists meeting dates and provides a forum for its members to exchange information and offer solutions to problems.

MUG filled most, but not all, of the customers' needs, says Nissen. "Mentor Graphics bent over backwards to make MUG a successful organization that was able to run on its own," he says. Yet the users found something lacking: They wanted to talk directly with Mentor's engineering staff. So MUG decided to hold its 1987 annual meeting in a Beaverton, OR, hotel—just a short drive from Mentor's headquarters.

More than 225 Mentor customers gathered for the 3-day meeting. Even more important, approximately 100 Mentor engineers spread themselves among the technical sessions and open forums to answer questions and talk with users. By all accounts, the meeting was easily the most successful to date: "There was overwhelming interaction between the users and Mentor Graphics' engineering staff," says Nissen, a digital engineer at Raytheon's Missile Systems Division in Bedford, MA. "Users gained a very strong insight into what's behind the scenes at Mentor, and the engineers gained great insight into what users' needs are."

"The users came with moans and gripes, but there's no question that we want and need a relationship with each other," says Peter Hoogerhuis, Mentor Graphics' manager of corporate field support.

Although most manufacturers readily recognize and appreciate the need for customers to communicate among themselves, Mentors' experience shows they can overlook the sophisticated user's need to communicate directly with the manufacturer's engineering staff. Other companies are discovering that sponsoring a users group requires much more from them than contributing funds and furnishing a keynote speaker for the annual meeting.

To improve communications with its users group, for example, Sun Microsystems (Mountain View, CA) is organizing a 12-person council to handle questions, criticisms, and suggestions from the users group's 3000 members. Each council member will specialize in a technical field, such as compiler development, network support, operating-system development, and window standards. Sun's workstation customers say the council's formation indicates the company's willingness to recognize the importance of their feedback. "It commits the company to the users group in a formal way," says Sun Users Group president William Toth.

A task of equal importance to 2-way communication is preservation of the users' independence. Vendors and customers both say they are sensitive to any attempts to manipulate the users group into an extension of the manufacturer's sales and marketing effort. Sun Microsystems' liaison to its users group, Sanford Meltzer, points out that although he has easy access to

Users groups are not just for novices

Contrary to the beliefs of many engineers that users groups are just for novices, members of users organizations say that they continue to benefit even as they become more skilled.

"Every CAD company has a customer support line, but the information users get from each other is of a much more practical nature," says David Austin, manager of computer-aided design at Integrated Technology Corp in Tempe, AZ. "There's a lot of information traded among users: application notes, bug reports, little pieces of custom software, new software, and lists of equipment to trade."

Users groups by definition should appeal to designers at all levels of advancement, says William Toth, president of the Sun Microsystems Users Group. "Users groups are more than just handholding groups. If anything, a users' group should become increasingly valuable as time goes by," says Toth. Leaders of the Mentor Graphics Users Group, for example, have taken deliberate steps to make membership in their organization as vital for seasoned users of Mentor equipment as for newcomers. They run technical papers in their newsletters and sponsor more advanced technical sessions at their annual meeting.

Tom Provost, a 13-year member of DECUS, the users organization for customers of Digital Equipment Corp, says that among the most important reasons for his long-standing membership are the contacts he makes with users who have similar applications. "I know who to call for help," Provost says.

"3000 of our best customers," Sun has always advocated the group's autonomy. "From the day I was hired, I was given no directions [from Sun] as to where the users group should go. My direction comes from the users group's board of directors."

Other company representatives agree that they should consider users groups as separate entities that complement the company. "It's not just a vendor-user relationship; it's a partnership," says Morris Paserchia, eastern regional technical support manager for Boulder, CO-based Cadnetix and liaison with its 700-member users group.

Seeing the fruits of labor

Once a manufacturer and its users group have established their responsibilities and jockeyed for position, users-group members say they are reasonably successful in influencing product design. "Cadnetix's response is not always immediate, but we do see it," says Ron EuDaly, head of Cadnetix's midwestern users group. EuDaly uses the Cadnetix CDX 50000S and 90100S workstations in his job as a supervisor for communications-equipment maker Xetron (Cincinnati, OH). He's pleased that the company has introduced both a floating-point operation and a drawing package in its latest software release—both enhancements that were recommended by attendees at a meeting of northeastern users that EuDaly attended last year.

Digital Equipment Corp's users group has acquired a reputation in users-group circles because of its substantial influence within the company. That influence stems in no small part from its size—55,000 members—and its considerable resources. Digital Equipment employs a staff of 35 to manage the activities of the group, called the Digital Equipment Corporation Users Society (DECUS), and its 21 special-interest groups.

Bill Brindley, a 12-year DECUS member and chairman of its special-interest group on networks, says the networks group has made many product recommendations to DEC, most of which have been implemented. "Going back over the years, users would say which capability they'd like to see in the product, and we'd write them up and pass them to DEC. More than 80 to 90% of those features got implemented in future network products."

Most recently, DECUS took Digital Equipment to task for a proposed software-licensing policy. After receiving a letter from DECUS's board of directors stating that the proposal was not in the best interests of the users, DEC abandoned its plans. DECUS is very effective in keeping DEC on track, says Tom Provost, a computer-group leader for MIT's William H Bates Linear Accelerator Center in Middleton, MA. "When DEC is not building the best product for the market, sometimes the users spot that more quickly than DEC."

Though their ability to affect product design may not always be all that they would like, users-group members say that without the backing of the group, they would have almost no chance to effect change. "Cadnetix has stated to us at Integrated Technology Corp as well as to other users that requests from individual users don't have much weight," says Austin. Observes DECUS member Provost, "Feedback has to be organized in order to carry weight." **EDN**

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Sept. 17	Aug. 27	Memory Technology; Communications Technology; Software	Closing: Aug. 20 Mailing: Sept. 10
Oct. 1	Sept. 10	Surface-Mount Technology; Computers & Peripherals; Industrial Product Showcase	Closing: Sept. 3 Mailing: Sept. 24
Oct. 15	Sept. 24	Test & Measurement Special Issue; Analog ICs; ASICs	Closing: Sept. 17 Mailing: Oct. 8
Oct. 29	Oct. 8	Computers & Peripherals; ICs & Semiconductors; Wescon '87 Product Preview	Closing: Oct. 1 Mailing: Oct. 22
Nov. 12	Oct. 22	Wescon '87 Show Issue; ICs; Computers & Peripherals	Closing: Oct. 15 Mailing: Nov. 5
Nov. 26	Nov. 5	Microprocessor Technology Report & Directory; Analog ICs; Sensors & Transducers	Closing: Oct. 29 Mailing: Nov. 19
Dec. 10	Nov. 19	Product Showcase-Volume I; ICs and Semiconductors; Software	Closing: Nov. 12 Mailing: Dec. 3
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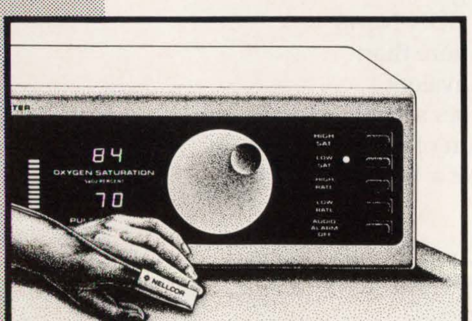

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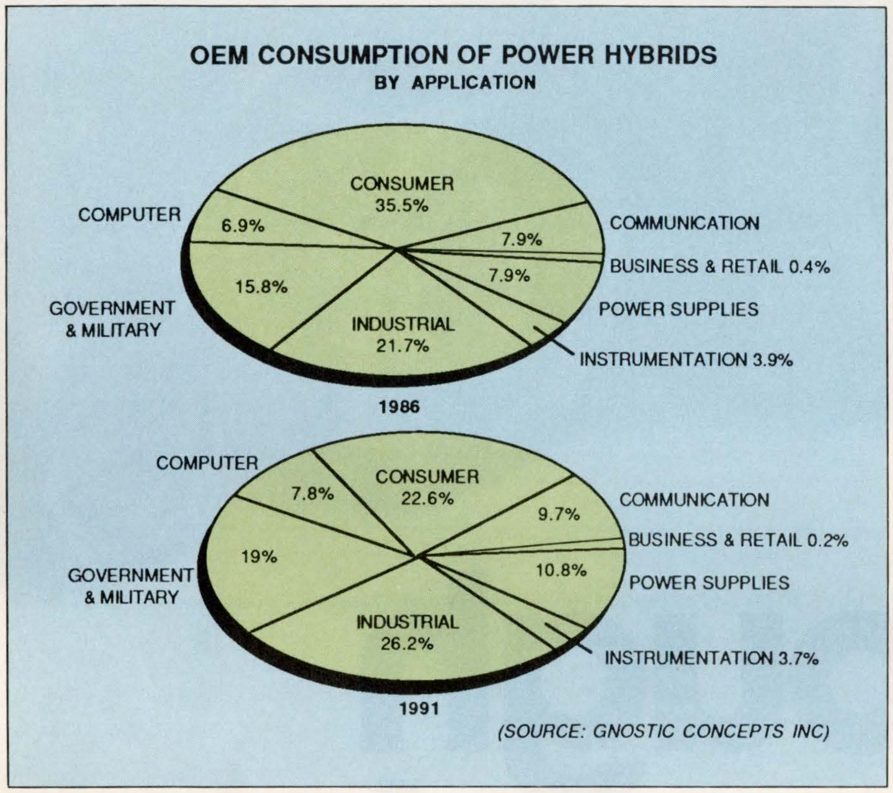

Miniaturization move aids power-hybrid market

The rush to miniaturize is causing hybrids to lose some ground to power ICs, but their use as replacements for discrete components will at least offset that loss, according to Gnostic Concepts Inc, a San Mateo, CA, market-research and consulting firm. Power hybrids provide denser configurations and require fewer discrete components than do discrete devices. They also have the advantage over power ICs of greater power dissipation. Furthermore, you can produce custom circuits in low volumes. Gnostic Concepts estimates power-hybrid sales will grow from $186.3 million in 1986 to $392.5 million in 1991—a 16.1% annual growth rate.

For its study, the market-research firm defined power hybrids as hybrid circuits that dissipate at least 5W per square inch. They further distinguished power hybrids from high-voltage hybrids, which can have a relatively low current flow.

Three application areas dominate the market for "smart" power hybrids: motor controllers, programmable voltage regulators, and automotive ignition systems. Because of their extensive use in robotics, motor controllers will be the preeminent application through the remainder of the decade. An increased interest in smart power supplies will boost the demand for programmable voltage regulators. Growing dependence on electronics in autombiles has contributed to power-hybrid use in automotive ignition systems, where they are employed to sense changes in various parameters and to thereby maximize engine performance.

Of the eight major end markets, Gnostic Concepts predicts the power-supply segment will grow the fastest, averaging 23.6% annually through 1991. The most dramatic change will involve the industrial- and consumer-electronic segments. Whereas the industrial-electronic segment claimed 21.7% of the market in 1986, it will have the largest share—26.2%—by 1991. On the other hand, the consumer-electronics share will drop from 35.5% in 1986 to 22.6% by 1991.

Delivery delays clog LVDT market

Users of displacement sensors are complaining of long lead times and back orders, especially in the delivery of LVDTs (least voltage coincidence detectors), and the inadequate production capacity will continue to face increasing demand over the next few years, according to Venture Development Corp (Natick, MA). Valued at $328 million last year, the total market for linear-proximity and displacement sensors should reach $691.6 million in 1991. Annual growth rate will average 16% over the period.

Availability problems are acute in the military and aerospace industries, which use large quantities of custom-made LVDTs. The ongoing conversion to fly-by-wire (tethered) technology, particularly in military aircraft, has substantially contributed to the growth in LVDT demand. The use of that technology necessitates more feedback about position of control surfaces, engine components, and landing gear. The tendency toward redundant systems—which increase reliability by using several LVDTs in single loops that previously would have employed only one—has stimulated growth as well.

Response to the delay crisis to date has been mixed. At least two OEMs now have in-house production facilities for LVDTs or, as a substitute, for precision potentiometers. And there's some chance that others will follow, by developing their own facilities, or perhaps, through acquisition. Two of the major manufacturers of the devices have already expanded their capacity in order to meet current and expected demands.

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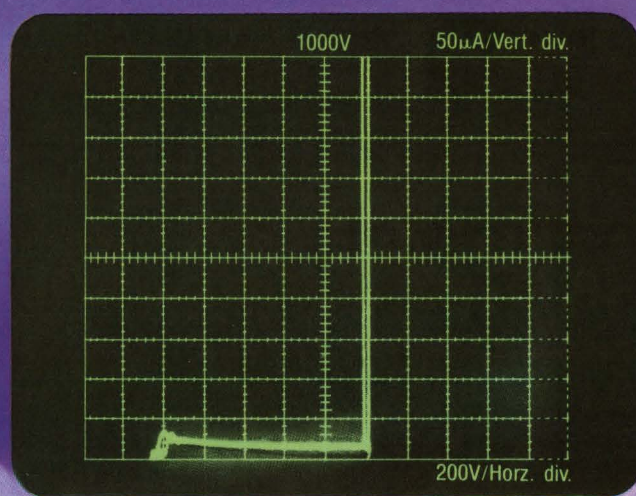

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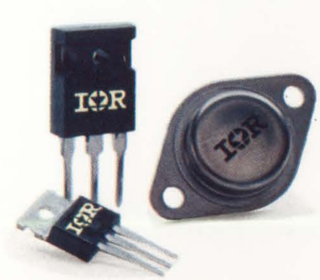

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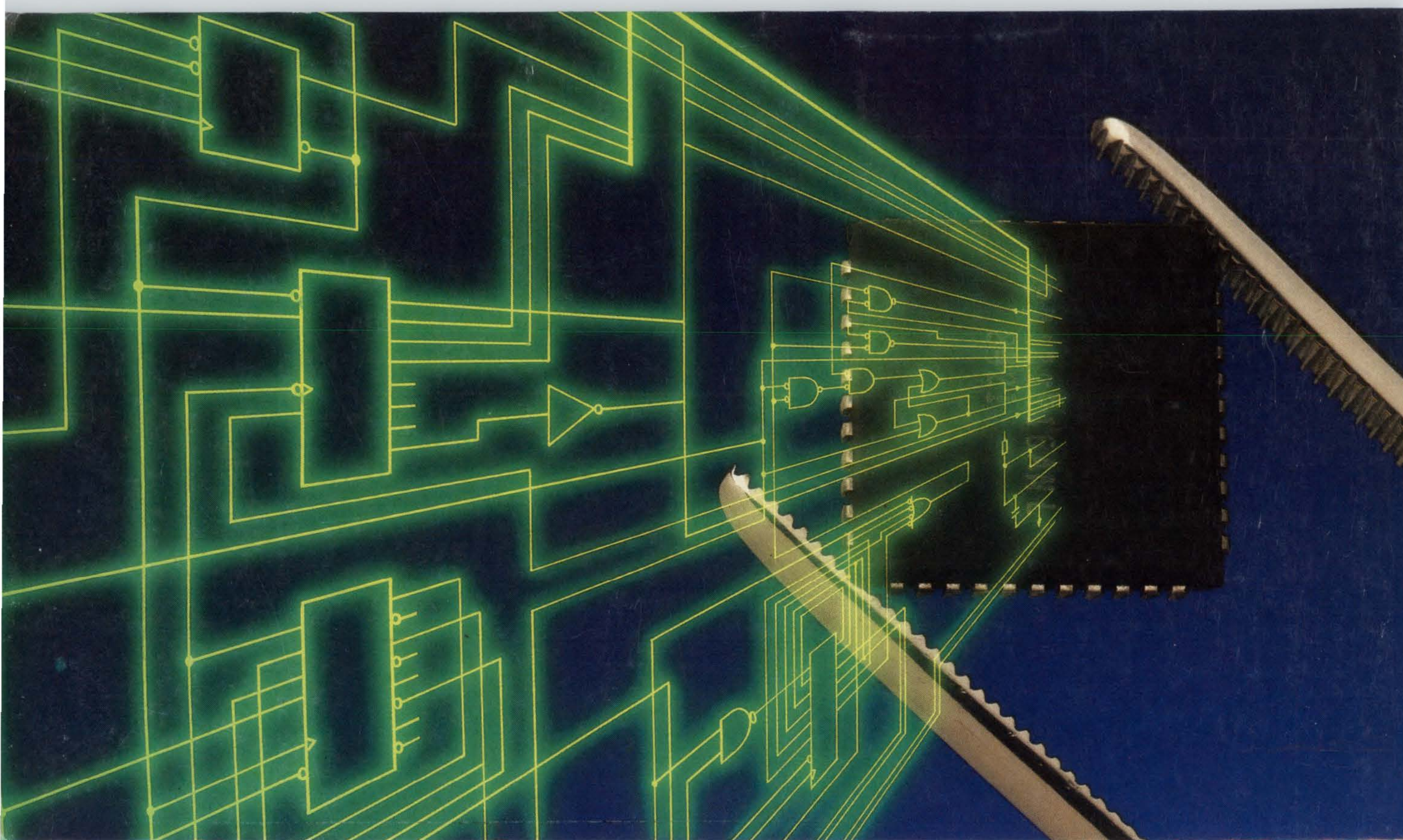

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