A CAHNERS PUBLICATION

OCTOBER 15, 1987

EDN®

SPECIAL ISSUE:
Test and measurement

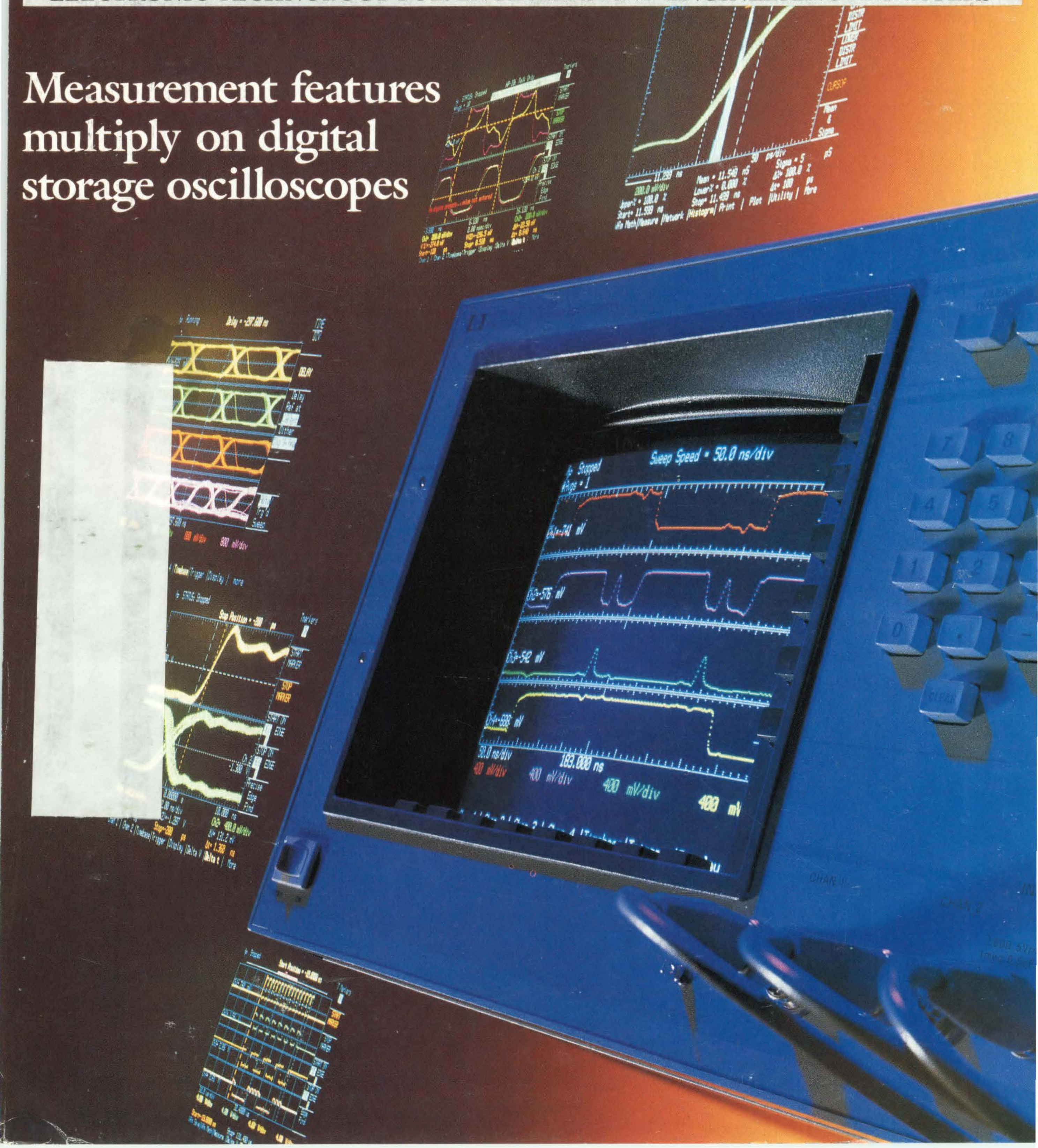
Reduce errors in digitizing instruments

Test A/D converters using DSP techniques

Semicustom linear arrays

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

Measurement features multiply on digital storage oscilloscopes



They're field programmable (even re-programmable). And they give you up to 1800 usable gates in an extremely flexible architecture.

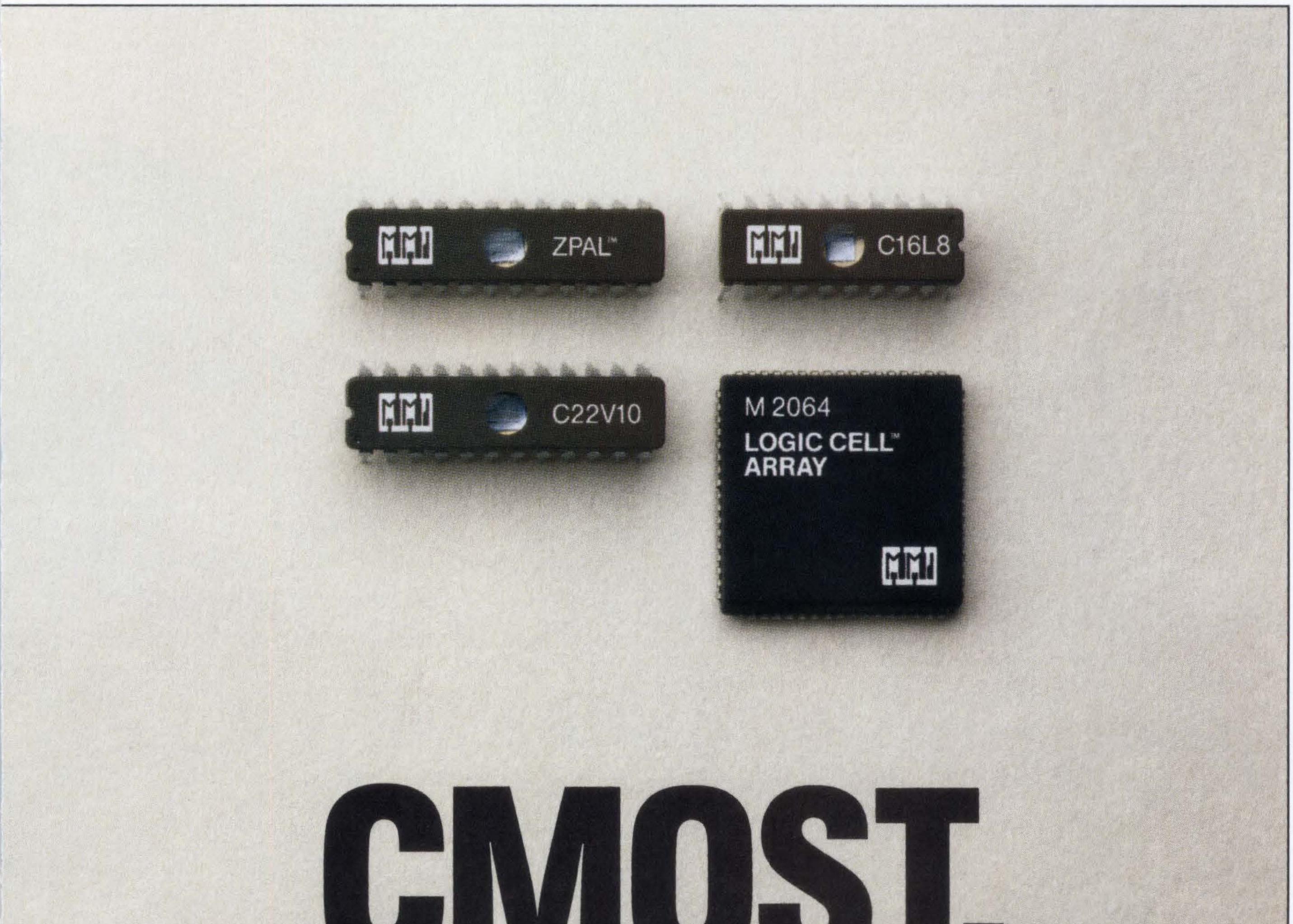
Naturally, we have all the programming tools you'll need to get your PLDs up and running in a hurry. The latest version of our PALASM® CAD software for your PAL designs. And XACT™ software for LCAs.

Best of all, we'll support you with a team of FAEs that's worked around programmable logic for years.

So call or write us for a CMOS sample kit and data sheets. Monolithic Memories, 2175 Mission College Blvd., M/S 09-14, Santa Clara, CA 95054-1592. (800) 222-9323.

And start getting the most out of CMOS.

Monolithic Memories



CIRCLE NO 172

There was nothing to it really.

Instead of making one CMOS PLD (like some competitors we could name), Monolithic Memories makes many.

So many, in fact, that our CMOS PLDs offer you more speed, power and architecture options than you can get from any of our competitors.

Take our ZPAL™ family, for example. It's a zero standby power (less than $100\mu A$) version of our popular PAL® C20R8 Series. And it comes in both 35ns and 45ns versions.

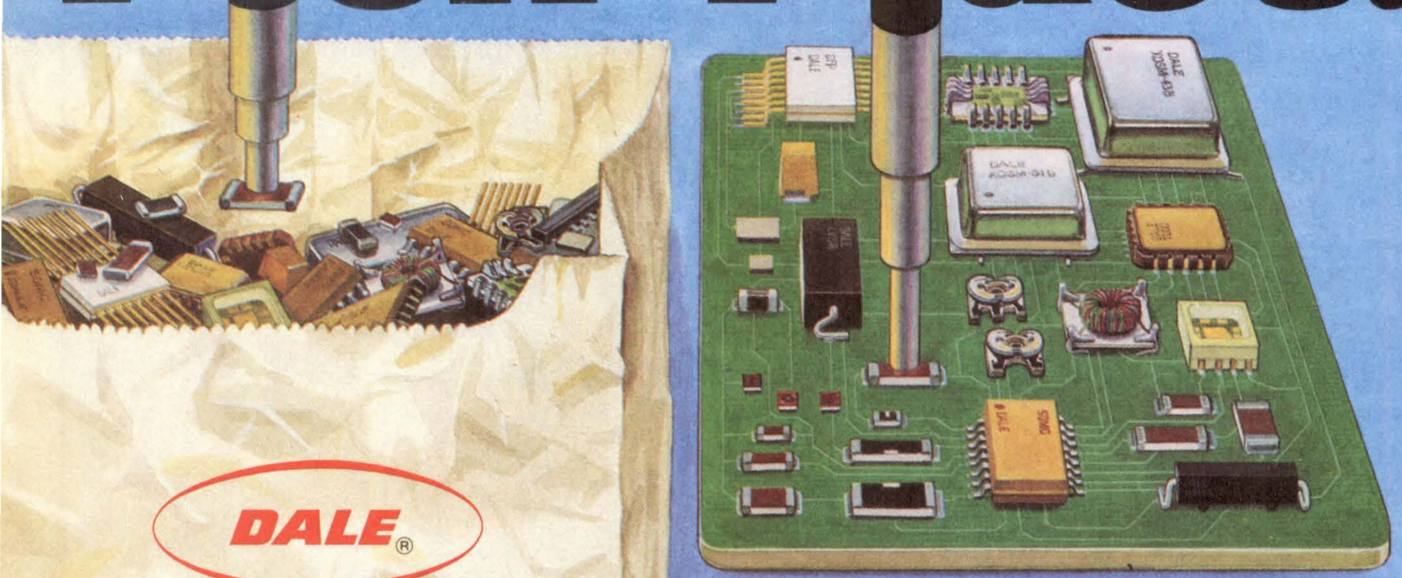
Or for universal applications, our PAL C22V10 combines a wide-open architecture with 25ns or 35ns speed. Yet it consumes a mere 90mA.

Better yet, our new quarter-power CMOS PAL C16R8 Series devices consume but 45mA. While their 25ns speed approaches the best of bipolar.

And should you need gate array density, but prefer PLD convenience, try our CMOS Logic Cell™ Arrays (LCA).

How we improved CMOS PLDs.

Pick&Place.



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You'll find the components at right already in use by major companies nationwide. These components are designed for automatic placement...compatible with standard soldering methods...and will help you shrink cost and board space.

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Dale makes your basics better.

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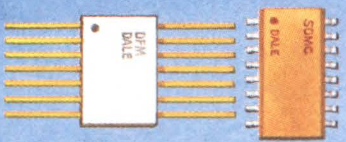
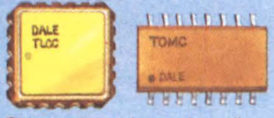
SOMC DFM DFP LCCC



Small outline molded dip package, ceramic chip carrier styles and flat pack (MIL-R-83401). All standard schematics. R/C styles available.

Thin Film Networks
TLCC *TOMC



Chip carrier styles and small outline molded dip package. All standard schematics.

Thick Film Chips
CRCW RCWP RCWPM

Commercial and MIL-R-55342 styles. 1%, 2% & 5% tolerance. Standard sizes available from stock.

Thin Film Chips
TNP
*TNPW

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Transformers

Custom designs available.

Chip Potentiometers
ST

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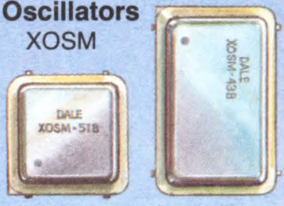
Thermistors
W H

NTC style. 5% & 10%, R_{25} tolerance.

Chip Inductors
*IMC

Molded style, 1 μH to 1000 μH. 10% & 20% tolerance.

Oscillators
XOSM



Metal packages in two styles (XOSM-43, XOSM-51*). Compatible with most logics. 240 Hz to 60 MHz.

Wirewound Resistors
LVSR
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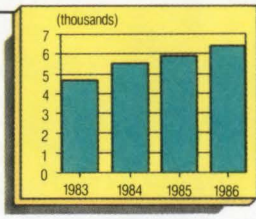
1, 2, 3, 5 watts including low value current sensing styles. "S" and Gull Wing leads.

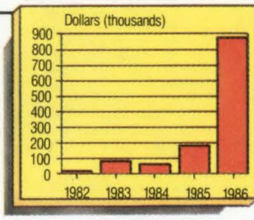
*Available soon.

Standards Update

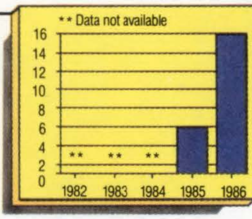
Uncle Sam Cracks Down on Computer Interference



The rising level of complaints to the FCC...



...caused it to issue more fines...



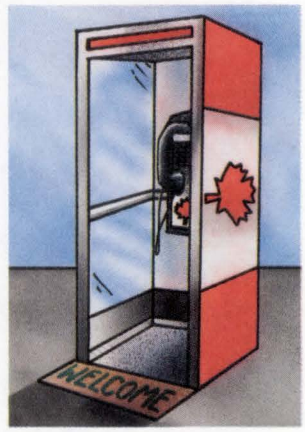
...and refer 15 cases for criminal prosecution.

Last Fall's COMDEX show in Las Vegas had a new kind of visitor. Federal marshals were there to seize equipment the FCC had tagged as non-compliant and to serve notice that arrests may follow. The computers were found to be in violation of Part 15 of the FCC rules, which bans sales of most electronic hardware unless tested for compliance.

The event did not surprise most computer executives, some of whom paid their share of more than $800,000 in fines issued by the FCC last year. Said one disgruntled manager, "These guys walk around here like Matt Dillon."

The need to comply has spawned a whole new kind of test business, companies specially skilled in designing and testing for compliance. One of these, the Boxborough, MA-based laboratory of Dash, Straus & Goodhue, combines testing, design and even legal services under one roof, permitting manufacturers to go to COMDEX with their minds on sales, not sanctions. The company even offers a "Guaranteed Rate/Guaranteed Date" plan under which equipment is tested, modified for compliance, and retested per FCC standards for a fixed price guaranteed in advance. The laboratory has been accredited by the National Bureau of Standards for telecommunications and emissions testing, and can be reached at 617-263-2662.

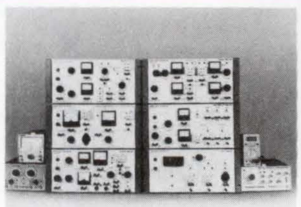
Canada Lays Out the Welcome Mat for Telecom Firms

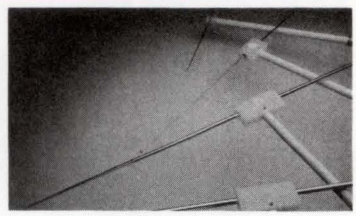


The Canadian government has swung its doors wide open for US telecom manufacturers. The open door policy is a welcome change for US manufacturers who have found most foreign markets closed to their goods. Canada's free trade telecom policy has allowed savvy manufacturers to increase their sales by up to 20%. But to sell north of the border, firms still need to follow a few simple steps. Most importantly, the equipment has to be registered under Canadian Standard CS-03, roughly equivalent to the FCC's interconnect regulations in Part 68. The government of Canada has already approved a number of firms in the United States to do the required telecom testing and submissions. One such firm, Dash, Straus & Goodhue of Boxborough, MA (617-263-2662), has seen a sharp rise in requests for Canadian approvals, especially among the industry's most successful firms. "There seems to be a correlation between economic success and willingness to enter foreign markets," says firm founder Glen Dash.

Elsewhere in the world, telecom markets are opening. Dash, Straus & Goodhue is currently performing submissions for telecom equipment in both the United Kingdom and Japan. New efforts within the Common Market (EC Directive 86/361/EEC) may make one unified approval scheme throughout Western Europe a reality within two to three years.

Fed's Own Instruments Help Manufacturers Comply





What kind of tools can best convince an agency that equipment complies? Why, their own, of course. Now the FCC's own designs are available through a company called Compliance Design. Key to emissions compliance is the use of the **Roberts Antenna®** developed for the FCC in the 1950's. Willmar Roberts, its inventor, is a former Assistant Chief Engineer of the FCC Laboratory in Laurel, MD.

The antennas are renowned for their near-lossless characteristics. Compliance Design, the exclusive vendor of the Roberts brand, also offers a complete laboratory assembly package. The firm will supply antennas, masts, turntables, site design; and will even perform the crucial "site attenuation" tests the FCC requires. The Boxborough, MA-firm can be reached at 617-264-4668.

For telecom manufacturers, Compliance Design also supplies a **Part 68 Workstation**™ containing everything that's needed to comply with FCC, CS-03 (Canada) and EIA standards. The Workstation makes setting up Part 68 laboratories practical for just about everyone.

Safety Violation Sends a CEO to Jail

On February 13, Kenneth Oden, prosecutor for Travis County, TX, won a landmark case that sent shivers down corporate backbones nationwide. For the first time, company executives were sentenced to jail terms for negligence that cost a worker his life. The case highlighted a nationwide trend in which prosecutors are holding executives criminally liable for the death of a customer or employee.

For makers of EDP, medical and telecom equipment, safety on the job generally means getting their products UL® listed. Listing is a recognition that the product meets UL's standards for fire, shock, energy and mechanical hazards; listing is a legal requirement of certain municipalities. In those places, a death caused by a non-compliant product could give rise to the same charge of gross negligence which caused Travis County executives to be sentenced to jail.

Overseas, marks such as Canada's CSA and West Germany's GS are required, and foreign courts have been even less tolerant of corporate negligence than have our own. With the profusion of worldwide standards, obtaining those marks has proven to be quite a chore. Fortunately, certain key test labs have set up liaison services which permit worldwide product approvals at one location. Dash, Straus & Goodhue is one such lab and is regularly visited by agents of UL, CSA and West German TüV. Required marks for fourteen countries can be initiated from DS&G's location. Since the Travis County case, according to execs, its business has been brisk. Dash, Straus & Goodhue, Inc. can be reached at 617-263-2662.

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EDN

Volume 32, Number 21

October 15, 1987

ELECTRONIC TECHNOLOGY FOR ENGINEERS AND ENGINEERING MANAGERS

On the cover: Digital storage oscilloscopes can no longer be considered niche-market instruments. DSOs now feature 1-GHz bandwidths and digitizing rates to 1G samples/sec; prices have also dropped during the last couple of years. See pg 90. (Photo by Reg Francklyn; art direction by John Aylor; photo courtesy Hewlett-Packard)

SPECIAL ISSUE: TEST & MEASUREMENT

DESIGN FEATURES

Continued on page 7

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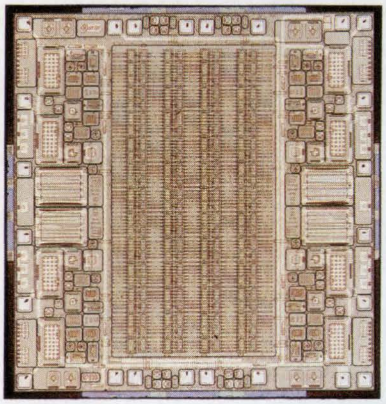
EDN

October 15, 1987



Linear and linear-digital semicustom ICs can operate at VHF and UHF frequencies and high voltages. Moreover, many of the linear devices include built-in gates that you can use to implement digital functions on the same chip (pg 57).

TECHNOLOGY UPDATE

PRODUCT UPDATE

DESIGN IDEAS

Continued on page 9

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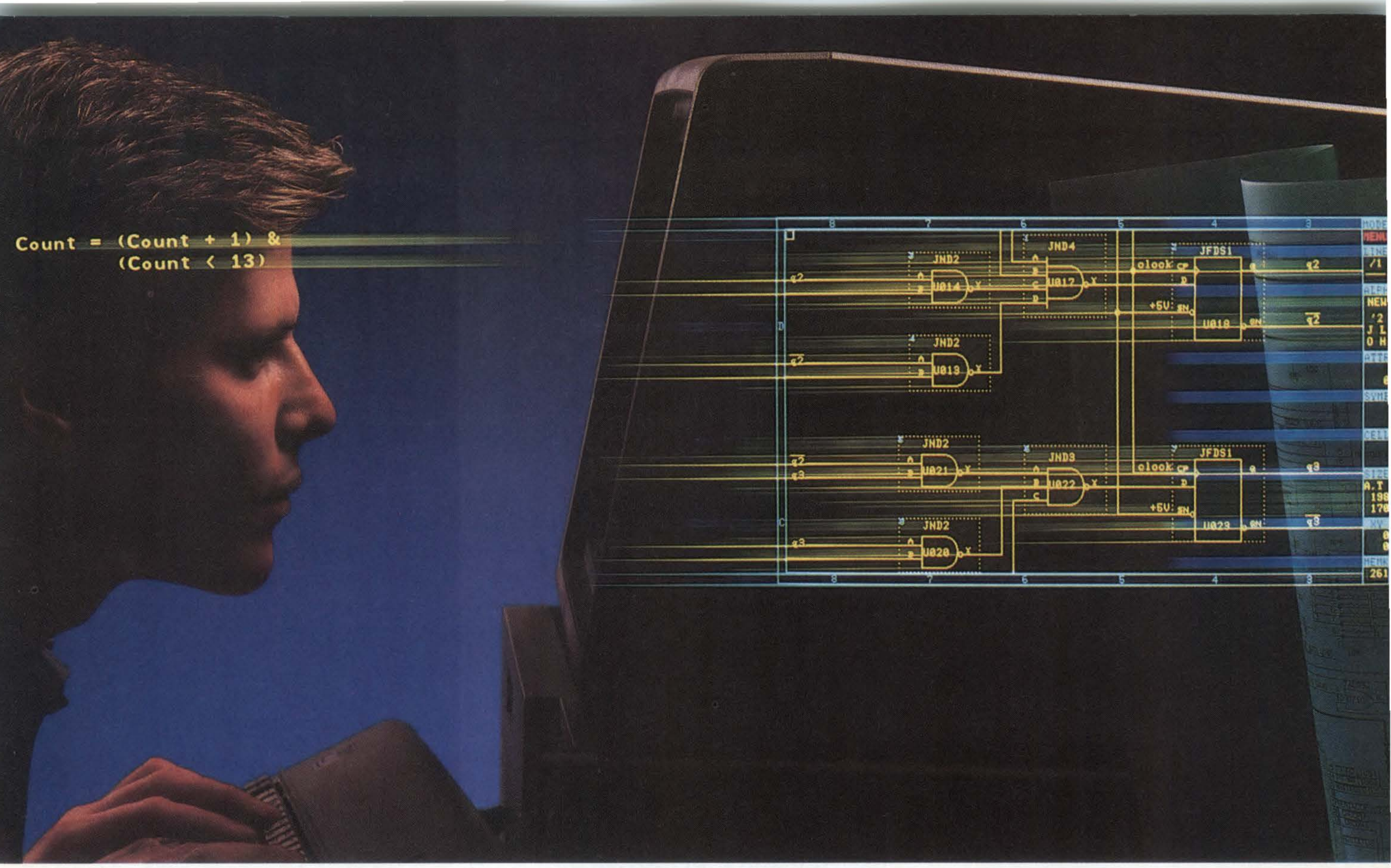

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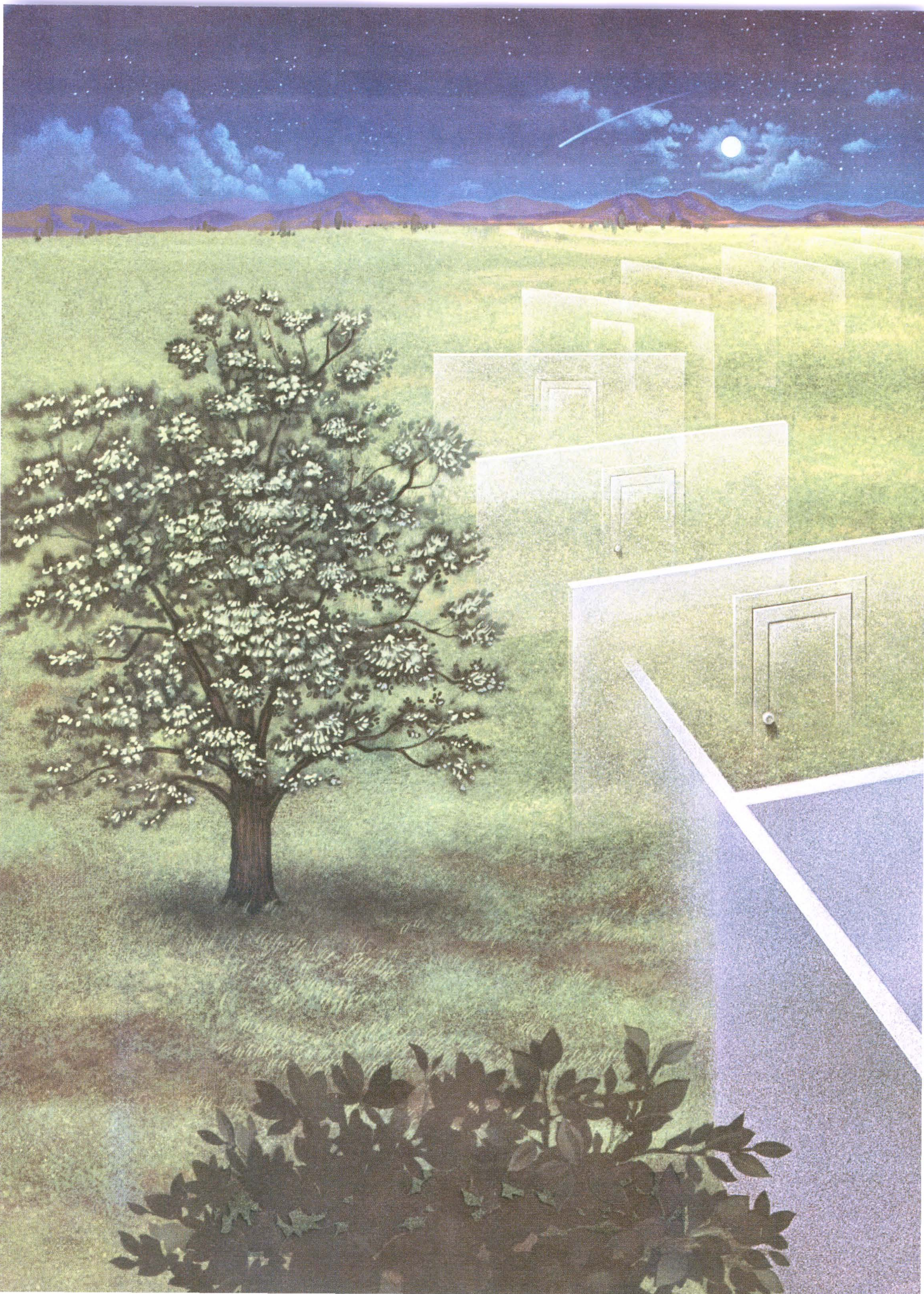

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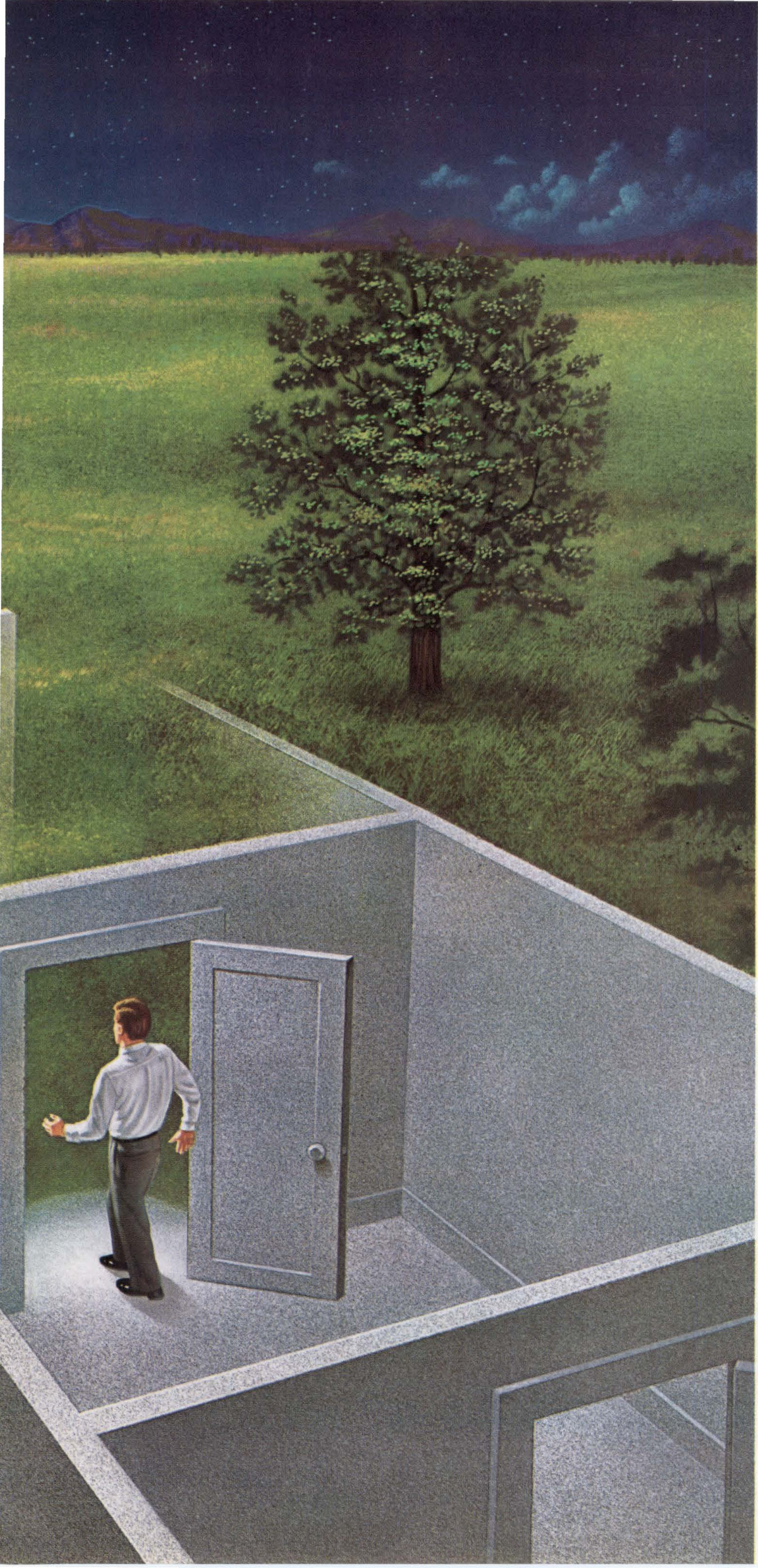

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Grab a pad and get to work on tomorrow.

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With a polyline draw speed of 110,000 vectors per second, a BITBLT transfer of 55ns per pixel, and a polygon fill of 20ns per pixel, QPDM can change a screen faster than the speed of thought. (It can redraw a 1K X 1K screen in 0.2 seconds.)

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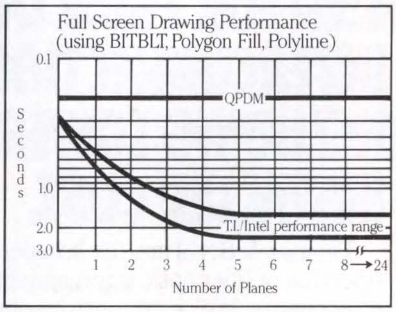

Each QPDM addresses four planes. It's cascadable, too. With no degradation in performance. And it can deliver all the color you need.

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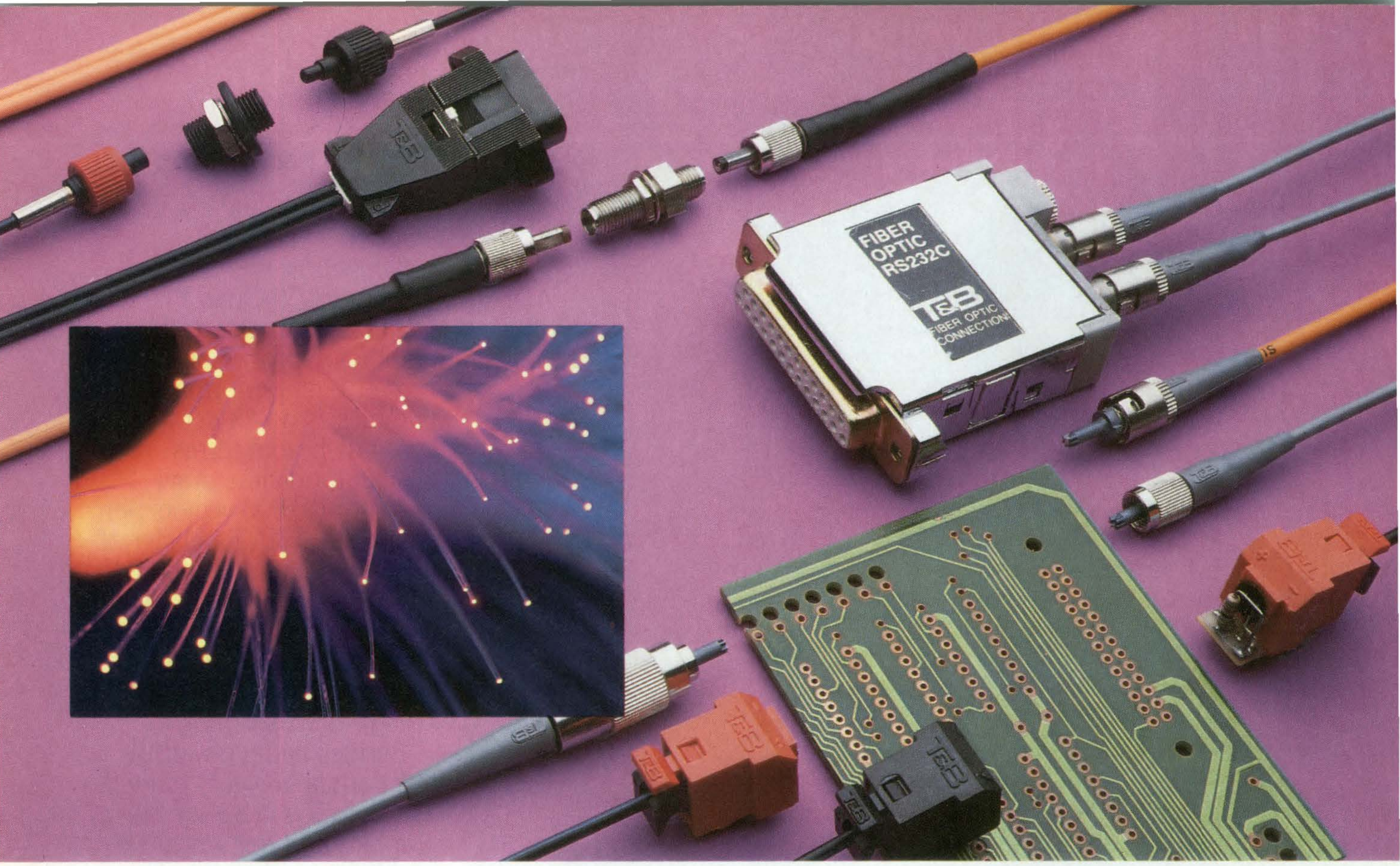

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Route any block and cell automatically.

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And you can document your design as you go along.

What's more, you can customize the EDS III interface to fit your needs. Whether you prefer the latest pull-down menus and windows in EDS III, the familiar GDS II menus or your own personal setup.

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Now everyone shines.

With design tracking that automatically reflects any change throughout the system, EDS III keeps everyone on your design team informed.

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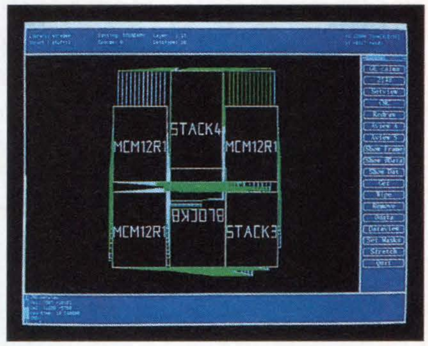

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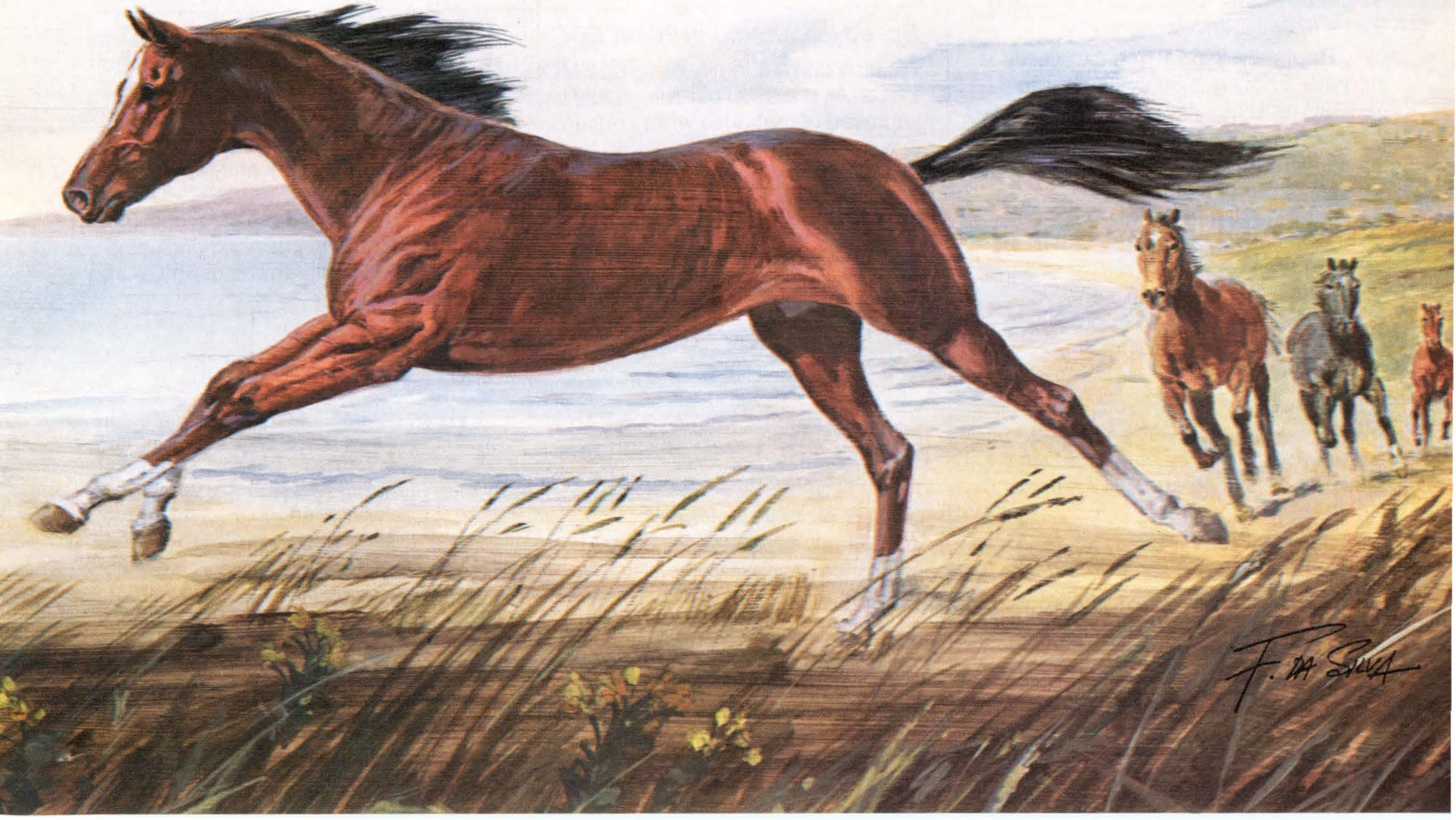

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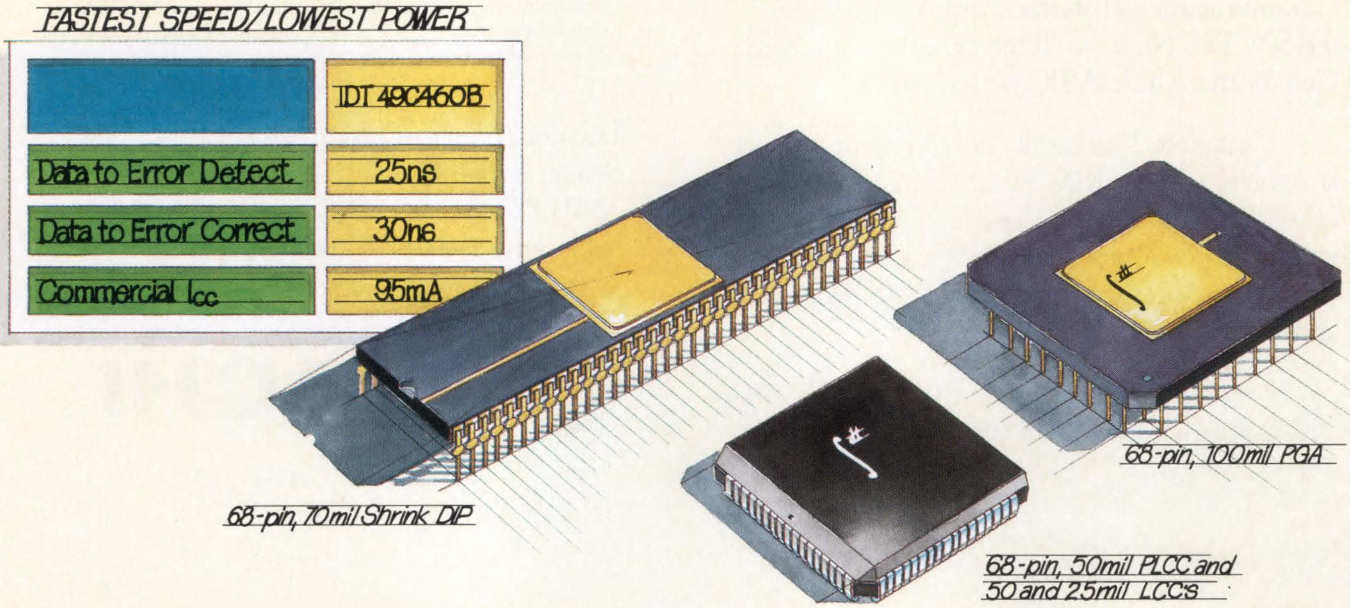
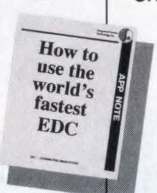


IDT49C460B: fastest speed, lowest power 32-bit EDC.

Your memories are getting bigger and with that comes higher error rates. Use the new, faster IDT49C460B to enhance data integrity. It corrects all single-bit errors, detects all double and some triple-bit errors.

Replaces 2960s. You can easily upgrade existing 2960 systems with the IDT49C460B because both devices use the same Hamming code. Your design benefits from faster speed, improved power consumption and a 3-to-1 reduction in chip count. Byte writes, byte operations and diagnostics are included.



Faster than bipolar. The IDT49C460B detects an error in 25ns and corrects in 30ns. Nothing is faster.

Lowest power. The only 32-bit EDC in CMOS consumes just 95mA commercial. Now you can get EDC faster than the fastest bipolar but with CMOS power.

Cascades to 64 bits. Only IDT offers you a simple, two chip solution for 64-bit EDC. (The TI632 cannot be cascaded to 64-bits; while the Am2960 approach requires 14 devices.)

16-Bit EDC

	IDT39C60A	IDT39C60-1	IDT39C60
Data to error detect	20ns	25ns	32ns
Data to error correct	30ns	52ns	65ns
Commercial I_{CC}	85mA	85mA	85mA

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Cascadable. Up to 64 bits.

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NEWS BREAKS

EDITED BY JOAN MORROW

THREE-TERMINAL 7.5A REGULATOR FEATURES 1.5V DROPOUT

The LT1083 3-terminal, positive, adjustable regulator from Linear Technology (Milpitas, CA, (408) 432-1900) features a guaranteed 1.5V dropout rating while carrying its maximum rated current of 7.5A. The device is suitable for applications that require high-efficiency linear regulation. In addition, the device dumps its quiescent current into the load, further improving the circuit's efficiency. Versions of the regulator are available in TO-3 and TO-247 packages. In the TO-247 package, the device costs $7.70 (100).—Steven H Leibson

WINCHESTER-DRIVE FAMILIES OFFER ESDI AND SCSI OPTIONS

Micropolis Corp (Chatsworth, CA, (818) 709-3300) has added the half-height 1600 and the full-height 1500 families of 5¼-in. Winchesters to its product line. The drives offer storage capacities of 180M and 765M bytes, respectively. You can choose from ESDI (Enhanced Small Device Interface) or embedded-SCSI (Small Computer System Interface) versions for both families. The 1650/1670 (ESDI/SCSI) half-height drives employ four platters to achieve the 180M-byte unformatted capacity. Eight platters fit within the full-height 1500 drives. The 1600 drives cost less than $4.50/megabyte; the 1500 Winchesters cost less than $3/megabyte (2500).—Maury Wright

LABWINDOWS NOW AVAILABLE FOR IBM MICROCOMPUTERS

In addition to running on the Macintosh, the LabWindows software development tool for applications involving data acquisition, GPIB instrument control, and data analysis now runs on IBM PC, PS/2, and compatible computers. This interactive program from National Instruments (Austin, TX, (512) 250-9119) lets you generate sequences of C and Basic code via pull-down menus that present an assortment of library functions and parameters; you don't need to know the specific details of GPIB programming or your instruments to use this program. This $495 program can simulate the front panel of an instrument, and it comes with routines for performing 2-dimensional data plots, statistical analysis, complex and array math, multiple curve plots, and data-format conversion.—J D Mosley

EIGHT-IN. DISK DRIVE STORES 1B BYTES OF DATA

Through the use of thin-film media and thin-film heads, Control Data Corp (Minneapolis, MN, (612) 853-7388) has manufactured the Sabre 1230, an 8-in. disk drive with an unformatted capacity of 1236M bytes. Featuring an average seek time of 16 msec, the Sabre 1230 provides a transfer rate of 24.19 MHz (3.02M bytes/sec). You can select from either an SMD, SMD-E, IPI-2, or SCSI interface. The manufacturer estimates a 30,000-hr MTBF and offers a 3-year warranty on head and disk assemblies. Priced at $6470 (OEM qty), customer-evaluation units of the Sabre 1230 are currently available. You can expect production deliveries during the second quarter of 1988.—J D Mosley

A/D-CONVERTER CARD ADDS ANALOG MEASUREMENT TO HP9000 SERIES

Infotek Systems' (Anaheim, CA) $1900 AD300 adds 32 single-ended or 16 differential channels of A/D conversion to the Hewlett-Packard HP9000 Series 200 and 300 workstations. The card performs 200,000 12-bit samples/sec and contains four S/H circuits to allow simultaneous measurements on as many as four signals. An onboard channel sequencer stores as many as 2048 sequencing steps; each step specifies a channel and gain. The AD300 includes level- and edge-sensitive trigger inputs and eight digital outputs for controlling external circuitry.—Steven H Leibson

VME BUS-BASED SYSTEM HOSTS UNIX SYSTEM V RELEASE 3.1

The Unicorn C multiuser/multitasking computer system runs Unix System V release 3.1. Microproject Corp (Marina del Rey, CA, (213) 306-8000) offers the VME Bus-based system, which is powered by a 30-MHz AT&T WE 32200 μP and support chips. You can buy system configurations that support as many as 200 users and a variety of peripheral configurations. The Unix implementation provides hooks that allow you to add device drivers without modifying the Unix source code. You can also specify the system with 68000-family VME Bus boards that act as a front end for real-time control applications. An 8-user, 85M-byte system costs $15,000.—Maury Wright

RISC-BASED UNIX SUPERMINI RUNS AT 14 VAX MIPS

Parallel instruction execution combined with 128k-byte caches for both code and data give the 5100 from Ridge Computers (Santa Clara, CA, (408) 986-8500) its 14 VAX MIPS rate. (Vendors are beginning to use the VAX 11/780's 1-MIPS rate as a standard measure.) The RISC-based computer can execute instructions in parallel by using three processing units for integer, floating-point, and memory-reference operations. The processing units execute instructions independently, yet share current data in general-purpose registers. A code-resequencing compiler automatically rearranges your code to make the best use of the parallel-processing units. Cache coherency hardware updates rather than flushes the cache when cache contents no longer match main memory. Prices start at $109,000 for a system with 16M bytes of main memory and a 300M-byte hard disk.—Doug Conner

TAPE-LENGTH INCREASE BOOSTS CARTRIDGE CAPACITY

Series II Gold Plus XL tape cartridges can now store as much as 500M bytes in the 5¼-in. form factor and 100M bytes in the 3½-in. form factor. The cartridges are compatible with industry-standard tape drives that use the QIC-24, -40, -100, -120, -150, and -300 formats. DEI (San Diego, CA) has engineered the series of ¼-in. tape cartridges to increase the tape area and has modified the tape coating and chemical formulation to result in thinner tape. The new design allows the company to put 750 to 1000 ft of tape into a package that typically holds 600 ft. The company also packs 300 ft into the minicartridge that previously held 205 ft. The 750-ft 750XL costs $55.50, the 1000-ft 1000XL is $59.00, and the Microtape 300XL costs $35.00.—Maury Wright

7200W MULTIPLE-OUTPUT POWER SUPPLY IS USER CONFIGURABLE

Westcor's (Los Gatos, CA, (408) 395-7050) PowerCage card cage and PowerCard cards allow you to configure a power supply in your factory. The PowerCage has slots for 18 PowerCards in a 19-in. rack-mount enclosure that measures 10½ in. high×11¼ in. deep. Each PowerCard supplies as much as 400W at one or two fixed voltages ranging from 2 to 75V; if you fill all 18 slots with 400W PowerCards, you can obtain 7200W max. You can connect in parallel as many as 18 single-output cards for high-current requirements, or use 18 dual-output cards for a total of 36 different output voltages, or use any combination in between. One-MHz switching converters allow the system to achieve typical efficiencies of 80%. The PowerCage is priced from $1000; the PowerCards start at $400.—Doug Conner

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μP-BUS INTERFACE CONTROLLER HAS SIX OPERATING MODES

The SAB82220 bus interface controller from Siemens AG (Munich, West Germany, TLX 5210025; in the US, Santa Clara, CA, (408) 980-4500) integrates into a 68-pin plastic leaded chip carrier several of the functions required to interface 8086/88, 80186/188, or 80286 μPs to microcomputer buses. The controller, which is expected to sell for around DM 27 (1000), includes byte-swapping logic, parity generation/check logic, bus-controller and bus-arbiter functions, an address decoder, and the 48-mA and 32-mA bidirectional bus transceivers required to drive multiplexed address/data buses.

By hardwiring mode-control inputs, you can operate the device in one of six different modes. These modes allow you to implement an 18-bit dual-port interface, 27- or 24-bit single-port interfaces, or 18- or 16-bit bus controllers. In addition, you can use the device to demultiplex addresses and data onto separate buses.—Peter Harold

GATE-ASSISTED TURN-OFF THYRISTORS BOOST CONVERTER FREQUENCY

Thomson Semiconducteurs' (Paris, France, TLX 204780) ZTO thyristors allow you to design high-power choppers and inverters that operate at frequencies higher than 20 kHz, and let you design resonant converters that operate at 50 kHz or higher. The ZTO (zero turn-off time) thyristor is a gate-assisted turn-off device that only requires small commutation components and simple gate-drive circuitry. Advantages over GTO (gate turn-off) thyristors include a maximum controllable current about 10 times greater than that of a similar-sized GTO and no minimum on-time or off-time requirement. In addition, because the anode current falls to zero before the anode voltage starts to increase, turn-off switching losses are small. As a result, you can use ZTO devices at higher frequencies than gate turn-off thyristors.

Initial offerings include 500 and 900A devices with blocking voltages as high as 1600V; they cost $200 and $300 (1000). In 1988 the company plans to add 2000A/2500V devices to the family.—Peter Harold

SEMICONDUCTOR COMPANIES WANT PRODUCTION LIMITS RAISED

Japanese semiconductor manufacturers, who have been observing a production curtailment under government supervision, will ask the Ministry of International Trade and Industry (MITI) to relax the limits for the last quarter of the year. Because of the semiconductor industry's recovery, the manufacturers are hoping for a 10% increase in the 256k-bit dynamic-RAM output and a 50% increase in 1M-bit dynamic-RAM production. The vendors would also like to see the ceilings rise on ASIC devices and microprocessors. MITI will study the market more closely before deciding on any action; it notes that although the market appears strong, there is a possibility that the current demand could be based on double ordering.—Joan Morrow

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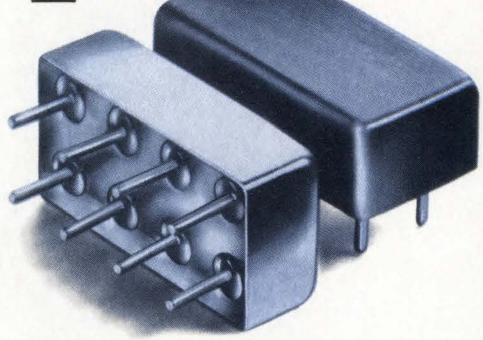

0.5 to 1000MHz from $13.95 (5 to 24 qty)

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MODEL	FREQ. RANGE (MHz) f_L to f_u	GAIN dB min	flatness††	MAX. OUT/PWR† dBm	NF dB (typ)	DC PWR 12V, mA	PRICE $ ea. (5-24)
MAN-1	0.5-500	28	1.0	8	4.5	60	13.95
MAN-2	0.5-1000	19	1.5	7	6.0	85	15.95
MAN-1LN	0.5-500	28	1.0	8	2.8	60	15.95

††Midband $10f_L$ to $f_{u/2}$, ± 0.5dB   † IdB Gain Compression

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CIRCLE NO 128

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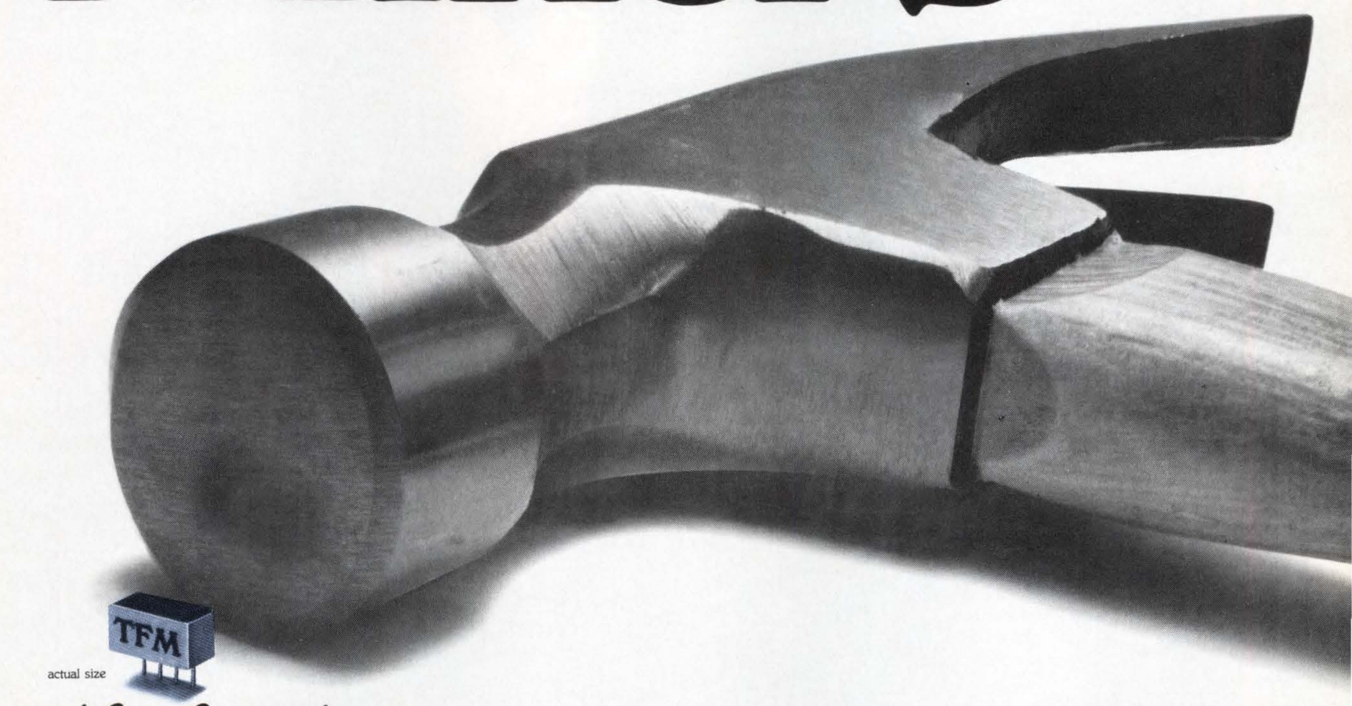

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We know our TFM mixers are tough ... they meet stringent MIL-M-28837 environmental requirements. But even we were surprised when our in-house weightlifter whacked a TFM-2 several times with a hammer ... and the unit still passed all electrical tests (we don't recommend you do the same).

Only 0.5 by 0.21 in. in pc board area, the TFM-series is the smallest hermetically-sealed mixer available anywhere. Although it has exceedingly wide bandwidth, it still takes up less space than flatpacks or TO-8 cases.

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*Units are not QPL-listed

Model	Freq. (MHz) LO/RF	Conv. Loss (dB), typ	L-R Isolation (dB), typ	Price $	Qty
TFM-2	1-1000	7.0	30	11.95	(1-49)
+ TFM-2P	1-1000	7.0	30	11.95	(1-49)
TFM-3	0.04-400	6.0	35	19.95	(5-49)
TFM-4	5-1250	7.5	30	21.95	(5-49)
TFM-5	5-1500	8.0	30	23.95	(5-49)
••• TFM-11	1-2000	7.5	25	39.95	(1-24)
••• TFM-12	800-1250	6.0	35	39.95	(1-24)
•• TFM-15	10-3000	6.3	35	49.95	(1-9)
•• TFM-150	10-2000	6.5	35	39.95	(1-9)

\+ phase detection, pos. polarity
••• IF port not DC coupled
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all other models +7dBm LO, +1dBm RF at 1dB compression

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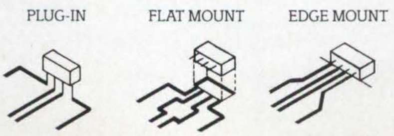

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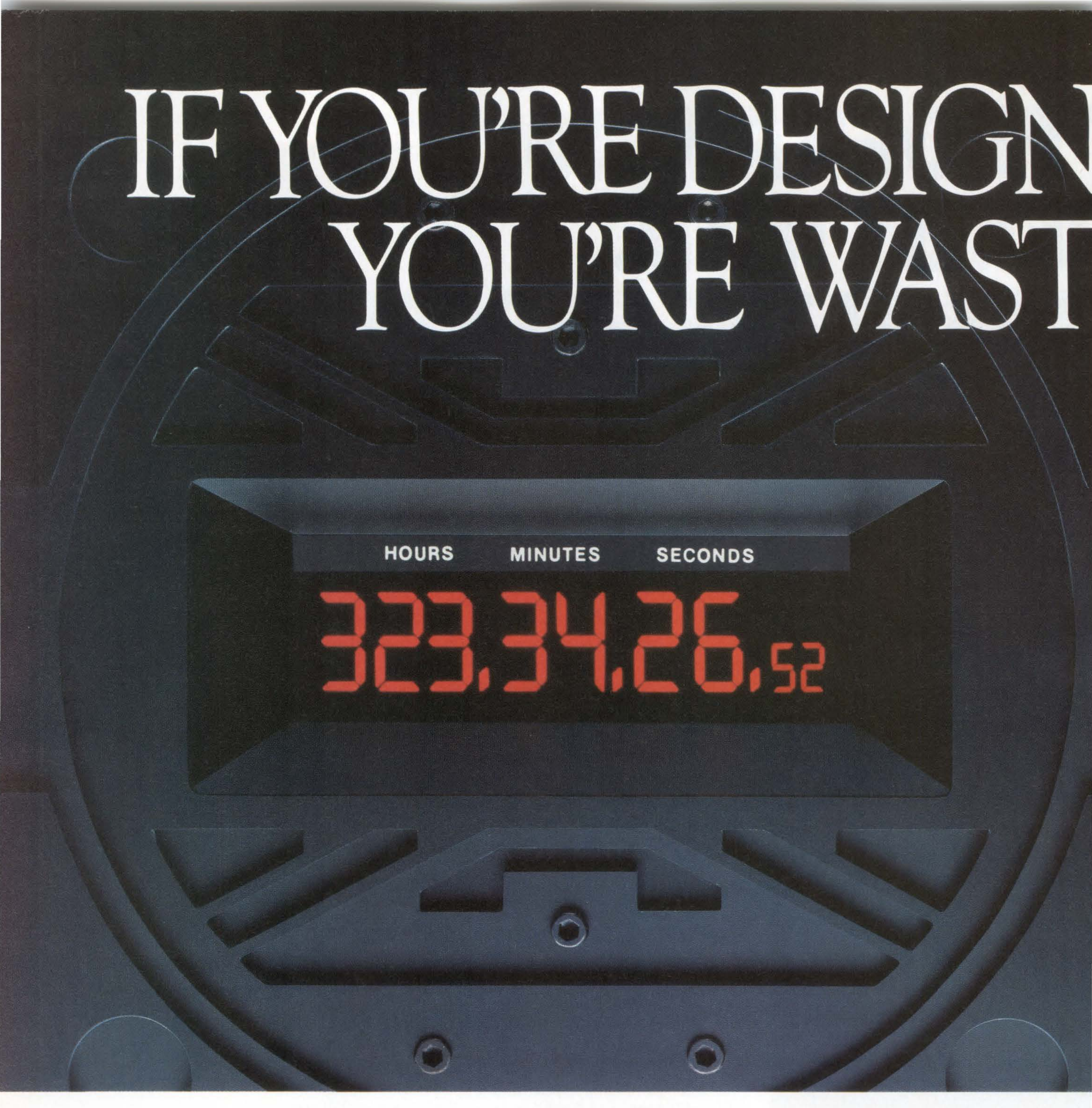

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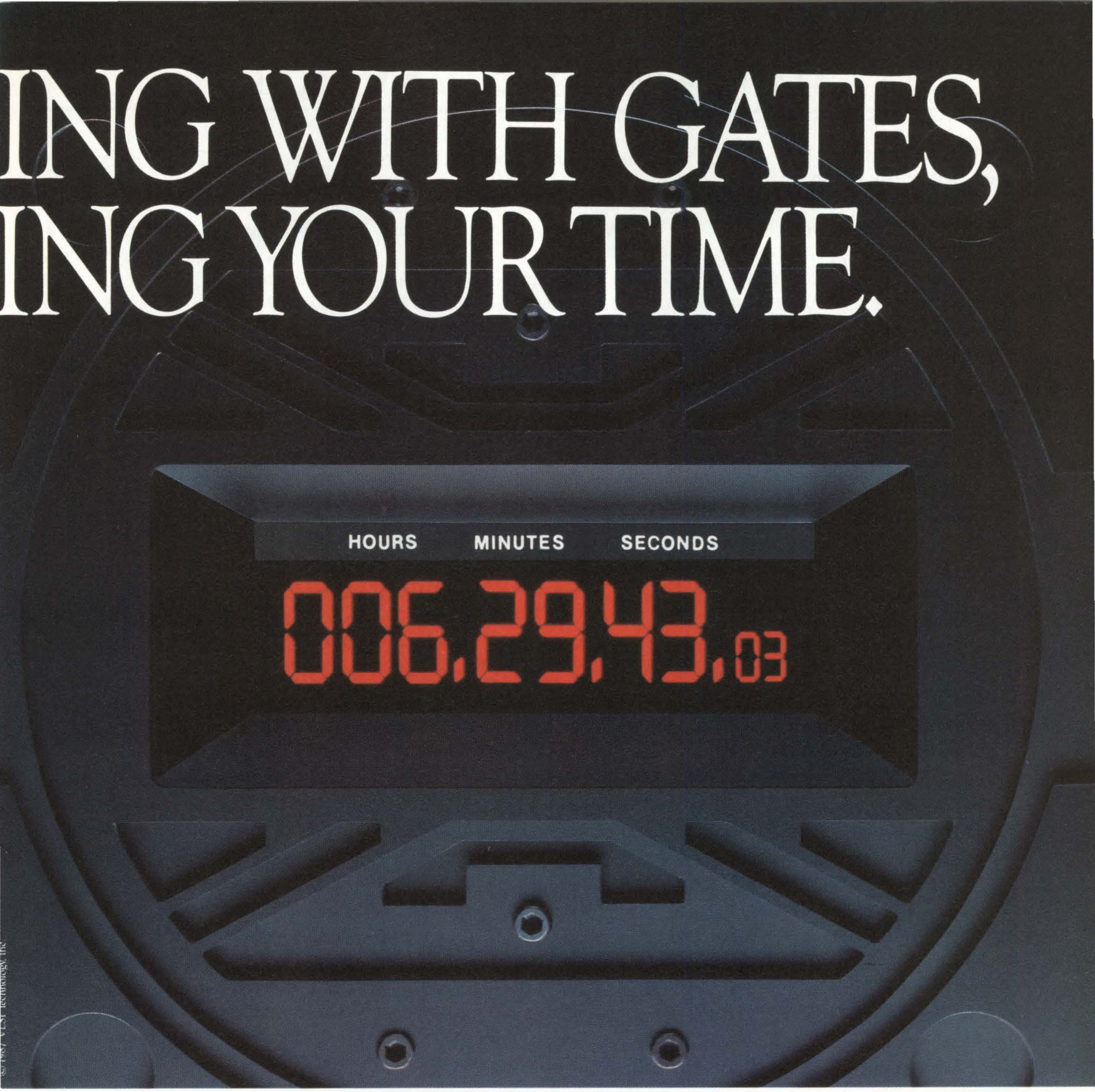

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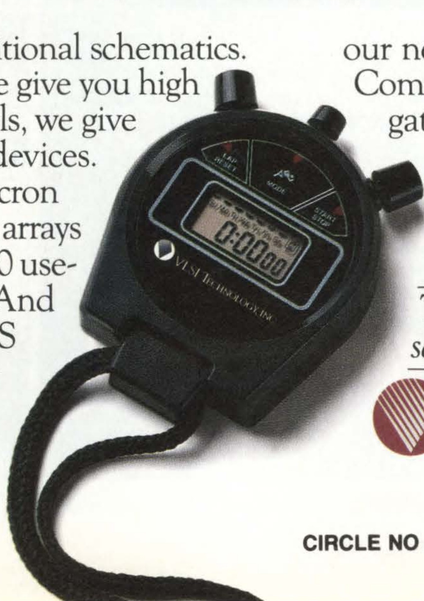

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CIRCLE NO 126

Don't reprogram space-program funds

With reference to the editorial "Nix the Mars trip" (EDN, June 11, pg 51): I understand Jon Titus's motivations for wanting to reprogram a hypothetical $10 billion Mars outlay toward improving high-school science programs. However, one must be very careful about leading charges to effect more prudent spending, especially when no one knows who is going to be in the position to decide what "more prudent" means.

If this hypothetical $10 billion emerged and got reprogrammed as Mr Titus suggests, I can just see the social scientists arguing: "Why spend this money on science labs only . . . why are you discriminating against psychology and sociology, or the study of pre-Columbian termite worship . . . ?" You see where this is going. Then come the "internationalists," who could certainly spend $10 billion on the world's hungry, thirsty, homeless, or whatever group is in vogue this year.

What I'm trying to convey, anecdotically, is the idea that once a $10 billion fund starts to be reprogrammed, for whatever reason, there's no telling what it will eventually be used for, or even if it will be so diluted that it won't be of help to anyone, from planetary scientist through the gamut of potential recipients. Upgrading high-school math and science curricula is certainly a laudable goal, and the good fight is to press for federal help in effecting it, not to take the money from some other laudable goal.

By the way, I disagree with Mr Titus's assessment of the technology fallout of the Apollo program. That effort was the agar in which computer technology was nurtured and from which it eventually flowered into its own market, for everyman.

Other than that, Mr Titus's views are generally insightful and useful.

Bill Kamenel
Ocean, NJ

PC-software report shouldn't ignore Macintosh

The focus on IBM personal computers in the Special Report entitled "PC-based GPIB control and data-acquisition products" (EDN, August 6, pg 94) is inappropriately narrow. The report mentions several products that are not yet available, while omitting available alternatives.

For instance, the report cites LabWindows as a powerful new software tool due this September from National Instruments. Yet no

mention is made of the company's equally powerful LabView software for the Apple Macintosh; this software has been available for almost a year. And although IBM's PS/2 machines are just coming on line, National Instruments has supported Apple's 32-bit, open-architecture Macintosh II since last fall. One can infer the company's commitment to this market by noting that the company's booth at Electro '87 showcased primarily Macintosh-based GPIB and DMA controllers.

Granted, every survey must draw the line somewhere. But a report purporting to summarize a technology area should draw it broadly enough to encompass the existing state of the art. EDN's report fails to do that.
Gordon H Benett
EMS Development Corp
Farmingdale, NY

Display module is available

The Design Idea entitled "Simple interface drives remote LED display" (EDN, June 11, pg 210) used the NSM4005A serial-data-input display module from National Semiconductor. Our company purchased National Semiconductor's Optoelectronics Div in December 1985. We continue to manufacture the display module, but now call it the TSM4005A.
Michael Bottini
Three-Five Semiconductor Inc
Tempe, AZ

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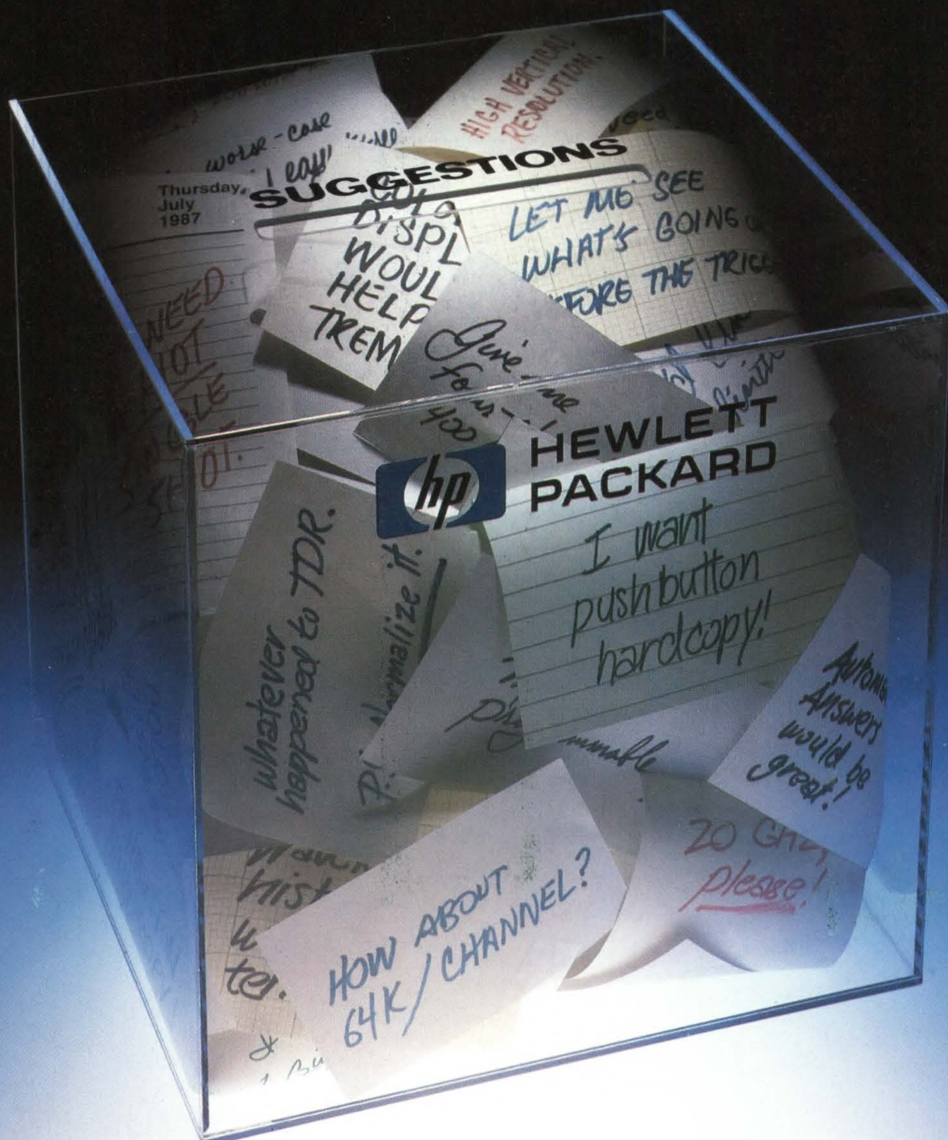
You told us what you wanted in digitizing oscilloscopes,



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And now, we bring you the new HP 54111D/54112D/54120T series.

These high-performance digitizing oscilloscopes let you measure what you've never measured before, with superb accuracy and ease of use.

You'll find innovations such as 20 GHz bandwidth, 4-channel simultaneous 400 MSa/sec with 64k memory per channel, time domain reflectometry (TDR) with normalization, 10 psec time interval accuracy, and more.

HP 54111D: the hot single shot.

The HP 54111D offers two simultaneous channels operating at up to 1 Gigasample per second...allowing you to capture high-speed single-shot phenomena such as high-speed pulses, plasma discharge, high voltage arcing, high frequency bursts, laser pulses and high energy events.

You get the single-shot performance of analog storage oscilloscopes with all of the performance advantages of digitizing oscilloscopes.

The HP 54111D also offers a 500 MHz bandwidth, so it will perform admirably in a wide variety of repetitive as well as non-repetitive applications.

HP 54112D: 64,000 bytes times 4.

The HP 54112D offers you simultaneous 4-channel capture at 400 Megasamples per second with 64k of memory per channel. Just right for the long data streams found in serial data communication applications.

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- ☐ 500 MHz repetitive bandwidth
- ☐ 250 MHz single-shot bandwidth
- ☐ 8k memory per channel
- ☐ 1 mV/div sensitivity

HP 54112D

- ☐ 400 Megasamples/sec digitizing rate
- ☐ 100 MHz repetitive or single-shot
- ☐ 4 simultaneous channels
- ☐ 64k memory per channel

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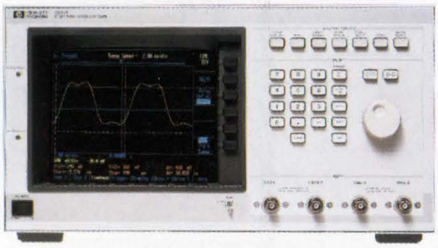

HP 54111D $23,900.00*

VERTICAL	
Rep. bandwidth	500 MHz
S.S. bandwidth	250 MHz
Inputs	2 chan & 2 trig
Resolution	8 bit to 25 MHz, 7 bit to 100 MHz, 6 bit to 250 MHz
Sensitivity	1 mV/div to 5 V/div
Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	1 GSa/sec
Resolution	10 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	8k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups	10

HP 54112D $22,900.00*

VERTICAL:	
Rep. bandwidth	100 MHz
S.S. bandwidth	100 MHz
Inputs	4 chan & 1 trig
Resolution	6 bit to 100 MHz
Sensitivity	5 mV/div to 5 V/div
Coupling	ac, dc; 50 Ohm & 1 MOhm
HORIZONTAL:	
Digitizing rate (max)	400 MSa/sec
Resolution	40 psec
Pre-trigger viewing	YES
MEMORY:	
Acquisition/chan	64k
Waveform storage	2 pixel, 4 rep wfm, 4 ss wfm
Nonvolatile instrument setups:	10

HP 54120T $27,850.00**

VERTICAL:	
Rep. bandwidth	20 GHz
S.S. bandwidth	NO
Risetime	17.5 psec
Accuracy	0.4%
Inputs	4 chan & 1 trig
Resolution	12 bits
Sensitivity	1 mV/div to 80 mV/div
Coupling	50 Ohm
HORIZONTAL:	
Accuracy	10 psec
Resolution	0.25 psec
Pre-trigger viewing	NO
Range	10 psec/div-1 s/div
MEMORY:	
Acquisition/chan	0.5k
Waveform storage	2 pixel (volatile), 4 rep wfm (nonvolatile)
Nonvolatile instrument setups:	10
TDR	
Pulse source	
Amplitude	0-200 mV
Risetime	35 psec
Flatness	1%
Normalization	YES
Waveform histograms	YES

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Varies according to options selected.

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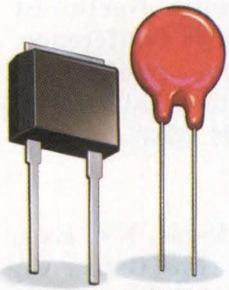

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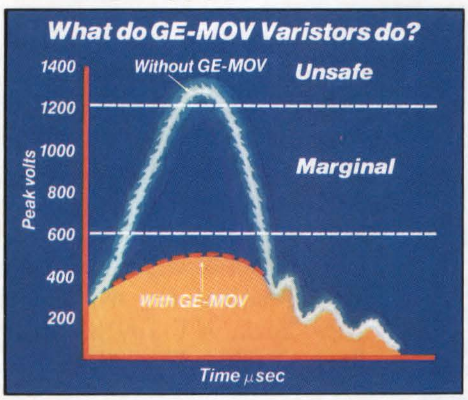

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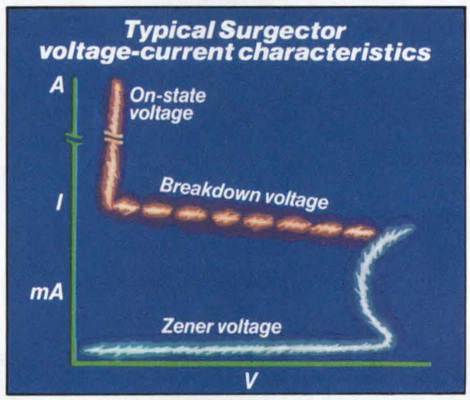

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6th Annual Pacific Northwest Computer Graphics Conference, Eugene, OR. University of Oregon Continuation Center, 1553 Moss St, Eugene, OR 97403. (503) 686-3537. October 25 to 27.

Expo SMT, Las Vegas, NV. Expo SMT, Box 1869, Los Gatos, CA 95031. (408) 354-0700. October 26 to 29.

International Fiber Optic Communications and Local Area Networks Exposition, Anaheim, CA. Information Gatekeepers, 214 Harvard Ave, Boston, MA 02134. (617) 232-3111. October 26 to 30.

Government Microcircuits Applications Conference (GOMAC '87), Orlando, FL. Palisades Institute for Research Services, 201 Varick St, New York, NY 10014. (212) 620-3371. October 27 to 29.

Unix Expo, New York, NY. National Expositions Co, 49 W 38th St, New York, NY 10018. (212) 391-9111. October 27 to 29.

Hands-On Expert Systems Design and Development (short course), Anaheim, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. October 27 to 30.

Hands-On Graphics Programming Using GKS/VDI Tools (short course), Boston, MA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. October 27 to 30.

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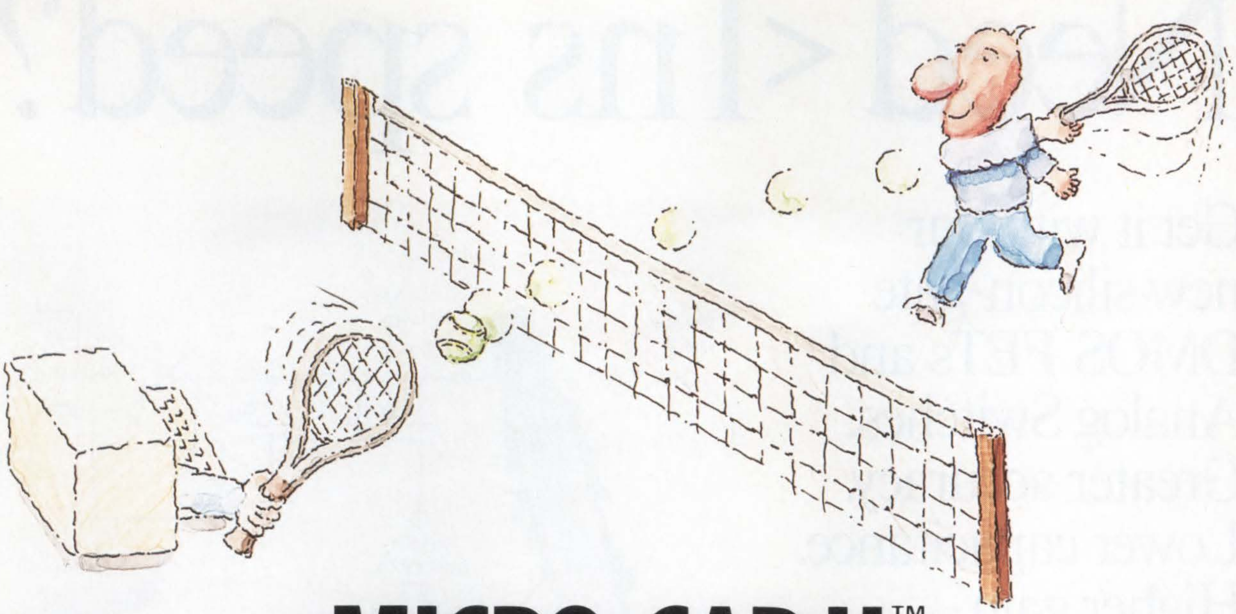

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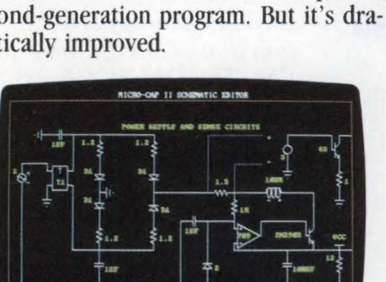

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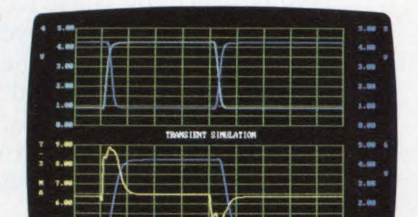

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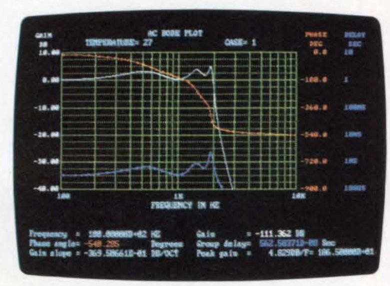

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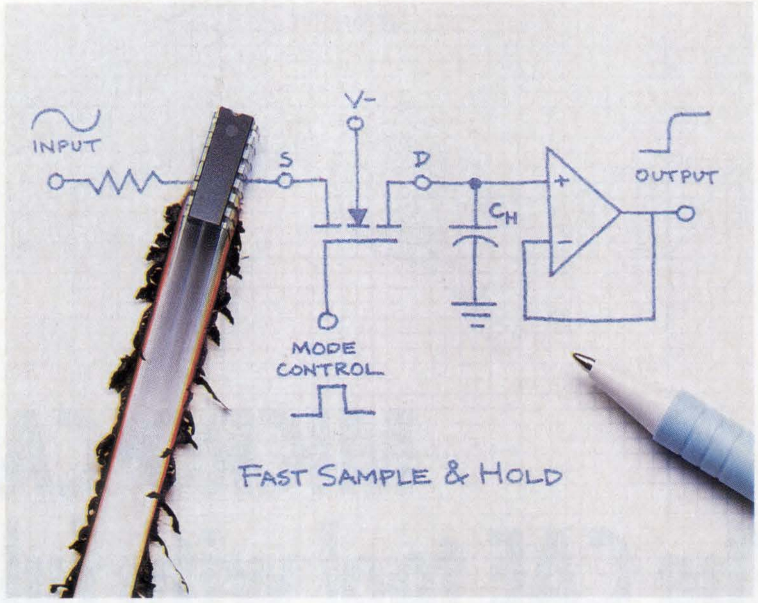

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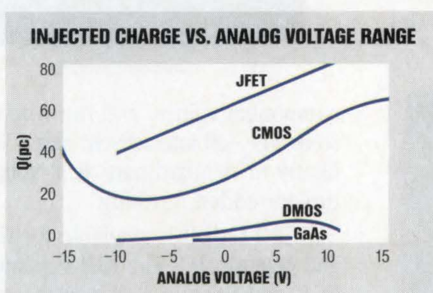

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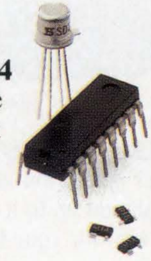

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Hands-On Microprocessor Software, Hardware, and Interfacing (short course), Los Angeles, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. November 3 to 6.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Atlanta, GA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. November 10 to 13.

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Designing Signal Processors with DSP and Bit-Slice Chips (short course), Anaheim, CA. Integrated Computer Systems, Box 3614, Culver City, CA 90231. (800) 421-8166; in CA, (213) 417-8888. November 17 to 20.

Troubleshooting Microprocessor-Based Equipment and Digital Devices, Norfolk, VA. Micro Systems Institute, 73 Institute Rd, Garnett, KS 66032. (800) 247-5239; in KS, (913) 898-4695. November 17 to 20.

9th Interservice/Industry Training Systems Conference, Washington, DC. Ralph Nelson, ADPA, Rosslyn Center, Suite 900, 1700 N Moore St, Arlington, VA 22209. (703) 522-1820. November 30 to December 2.

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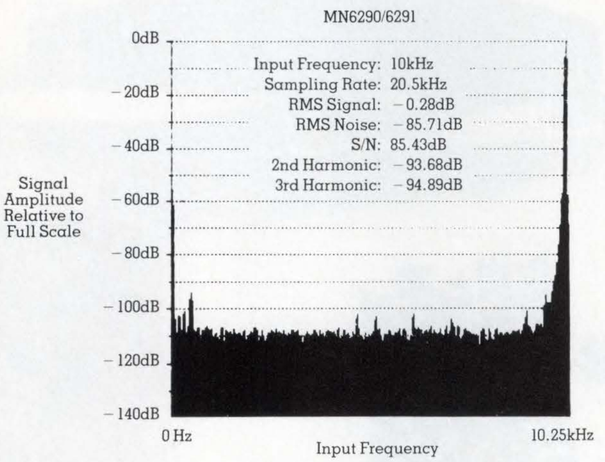

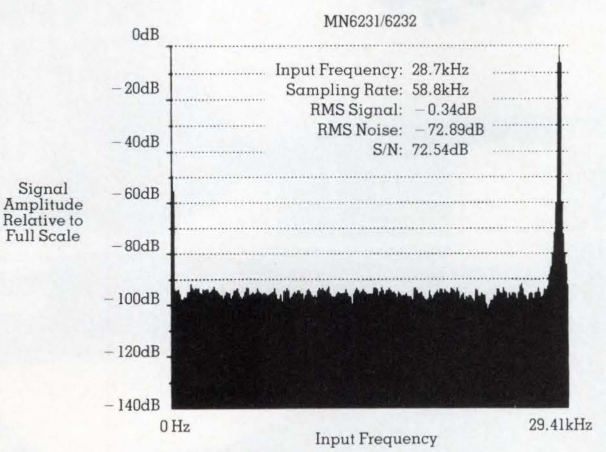

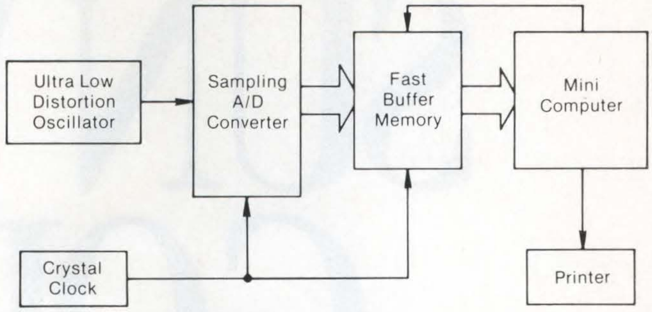

Frequency-Domain Testing of A/D Converters

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Part Number	Input Range	Minimum Sampling Rate	Minimum Input Bandwidth (Note 1)	SNR (Note 2)	Harmonics
12-Bit Resolution					
MN6227	10V	33kHz	16.5kHz	70dB	−80dB
MN6228	20V	33kHz	16.5kHz	70dB	−80dB
MN6231	10V	50kHz	25kHz	70dB	−80dB
MN6232	20V	50kHz	·25kHz	70dB	−80dB
16-Bit Resolution					
MN6290	10V	20kHz	10kHz	84dB	−88dB
MN6291	20V	20kHz	10kHz	84dB	−88dB

1. Input bandwidth for which SNR and harmonic specs are guaranteed when sampling at the minimum guaranteed rate.
2. Signal-to-noise ratio (r.m.s. to r.m.s.) with full-scale (0dB) input.

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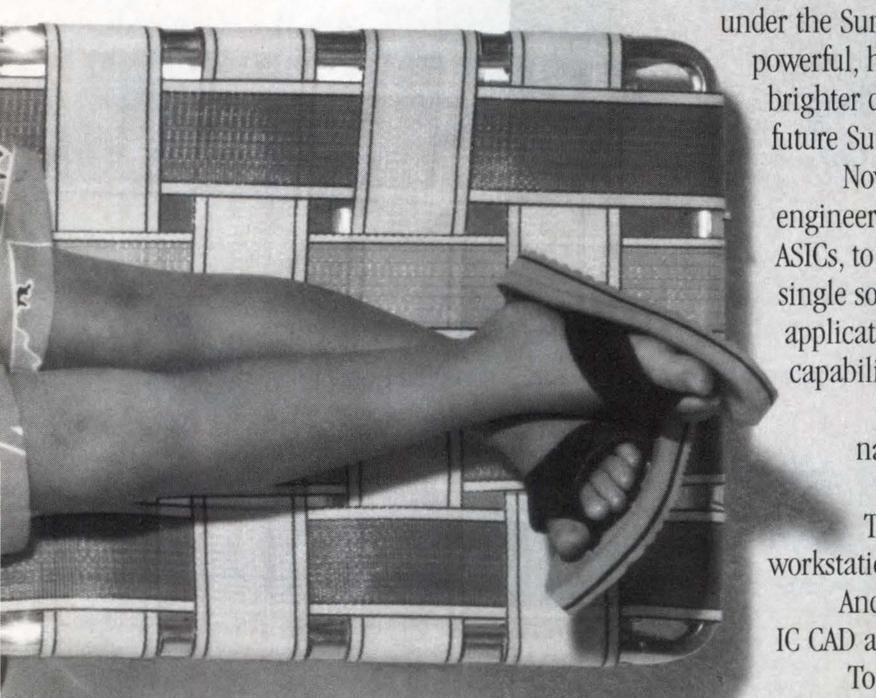

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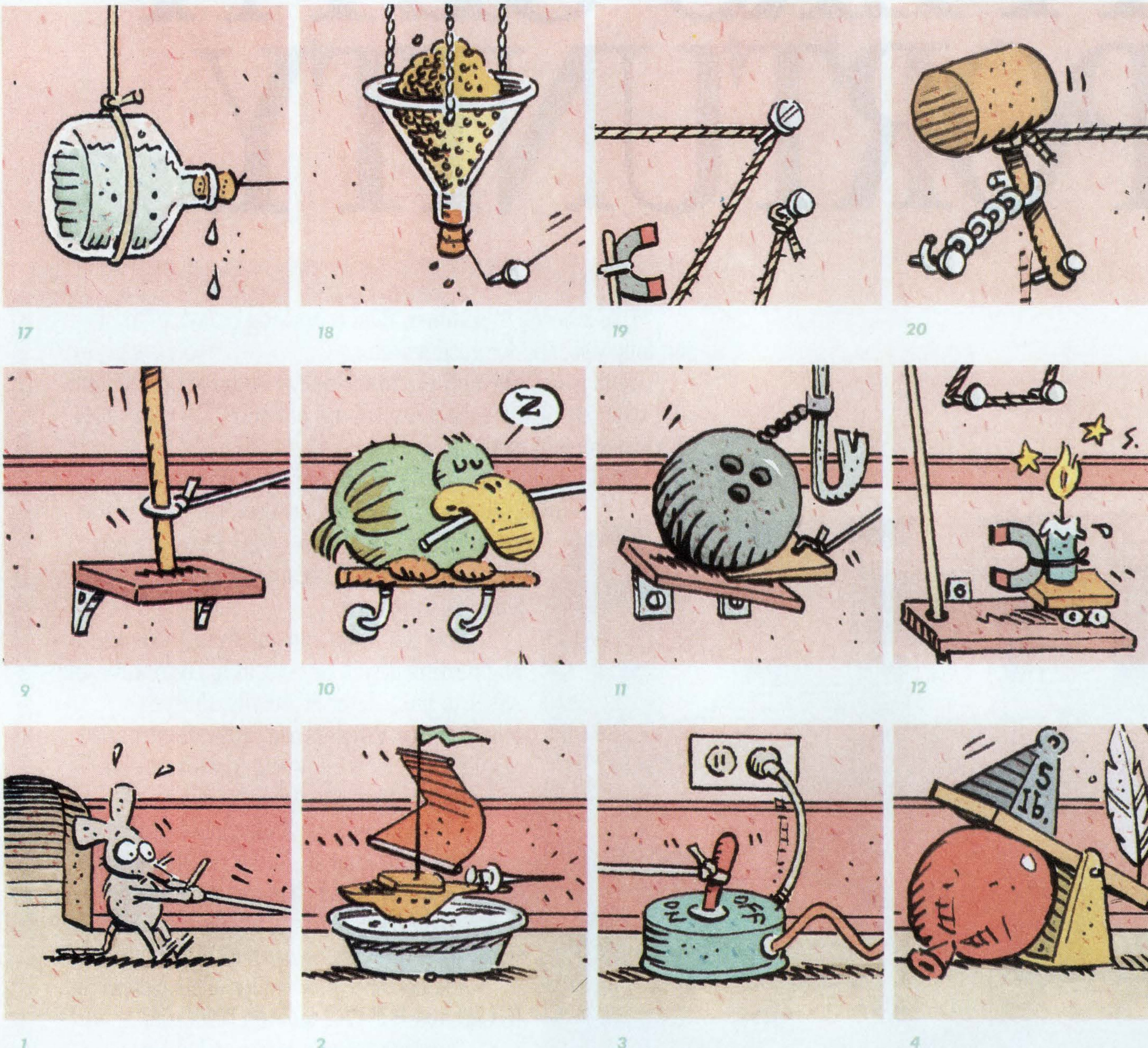

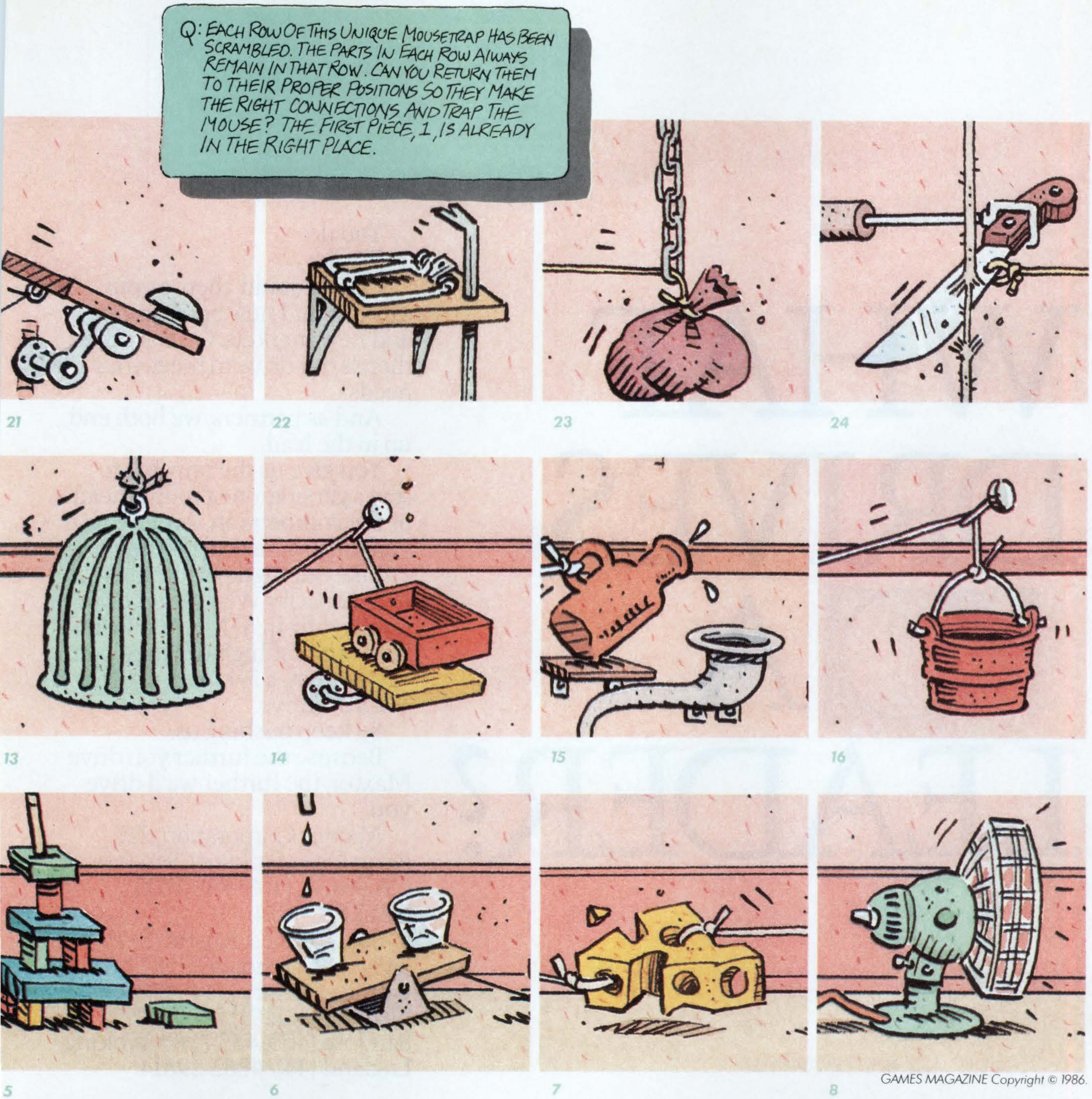

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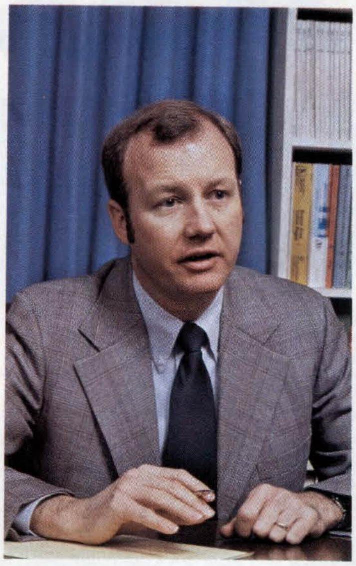
The details make a difference



Recently a friend of mine remarked that life would be great if it weren't for all the details. Another friend replied that life is 90 % details, so we're stuck with them. Both friends knew what they were talking about. The small details can easily consume most of our time. Frequently, though, the details fall through the cracks and receive scant attention—until something goes wrong.

Recall, for instance, the Delta Airlines' flight that ran into difficulty in June. Reacting to an engine-sensor light, the flight's captain inadvertently shut off both of his 767's engines, sending the plane into a downward glide that stopped just 500 ft short of the ground, at which point the crew was able to restart the engines. Apparently, because the plane's left- and right-engine fuel switches are close to each other, it's possible to inadvertently actuate both, cutting off fuel to both engines simultaneously. Since the incident, the FAA has called for the installation of a plastic guard between the switches. Such a guard may have been considered during the plane's design and deemed unnecessary—or perhaps it was one of those details that fell through the cracks.

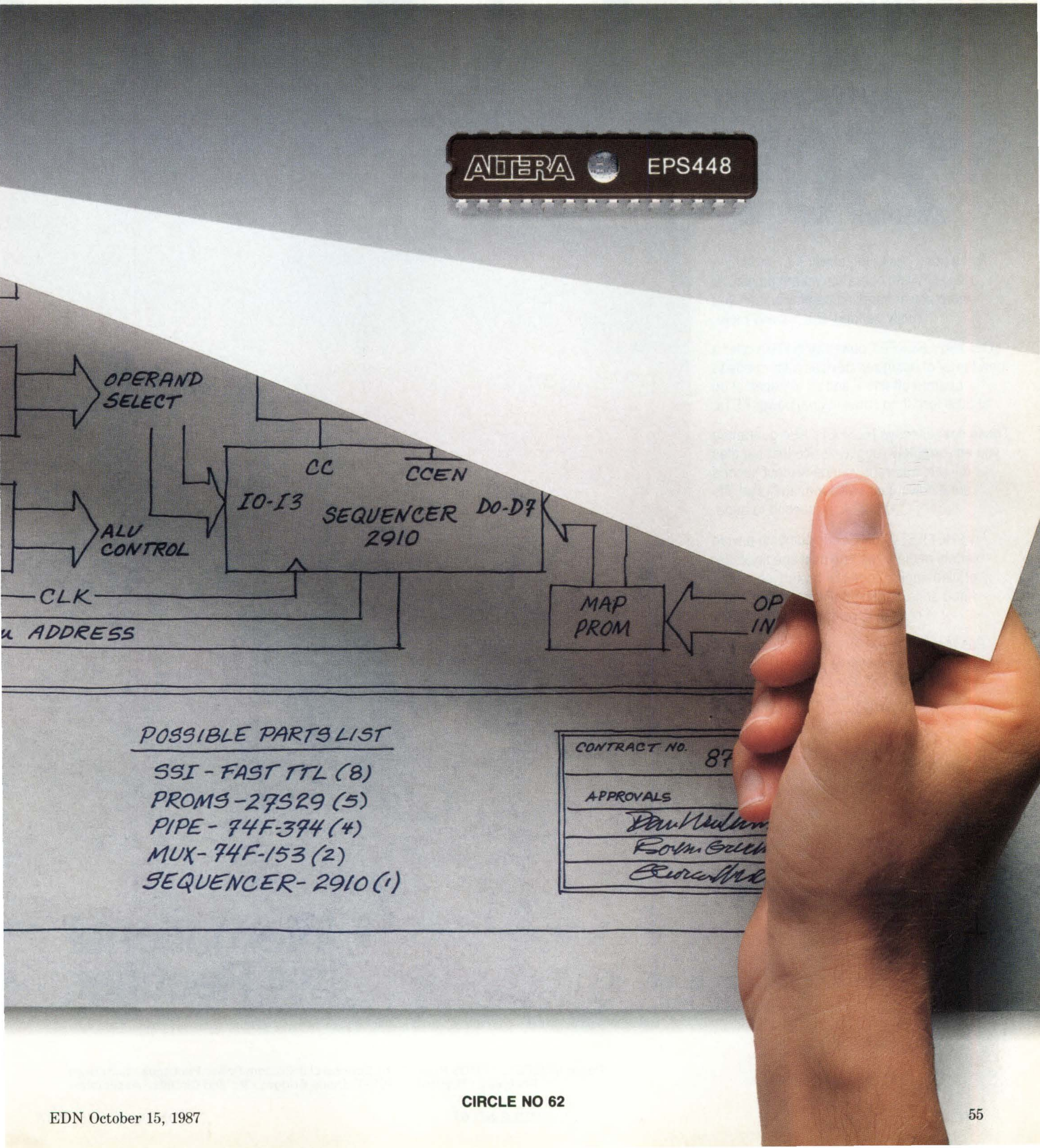
Forgotten details abound. A few months ago, the engine light on my car's dashboard went on. It took me some time to notice it, though, because, like the battery light, it's behind the steering wheel, hidden from view. The index in the owner's manual referred me to page 10; page 10, unfortunately, contained no reference to the engine light. However, the manual did mention oil and coolant-temperature lights, neither of which are illustrated in its pages or present in my car. So, as I sat in the breakdown lane along the Massachusetts Turnpike, miles from anywhere, the meaning of the glowing engine light was vague at best: either the catastrophe of an oil-pressure failure or the inconvenience of an overheated engine. Luckily, it turned out to be the latter.

Appliances provide the aspiring designer with a treasure trove of forgotten or ignored details. For example, power cords. It's amazing how many appliance designers forget to add a few plastic clips to their product so that wires can be stored neatly behind, underneath, or inside an appliance. I guess they figure you'll wrap the wire around the appliance, but that leaves it looking like a hostage trussed up with its own cord. Even worse are devices designed with removable cords or plug-in power modules, which are easily lost or misplaced. I have a box full of such cords and modules in my workshop, though I doubt that I can find it. My workshop is a mess and I should clean it up—but that's just a little detail.

Jon Titus

Jon Titus
Editor

State of Mind.



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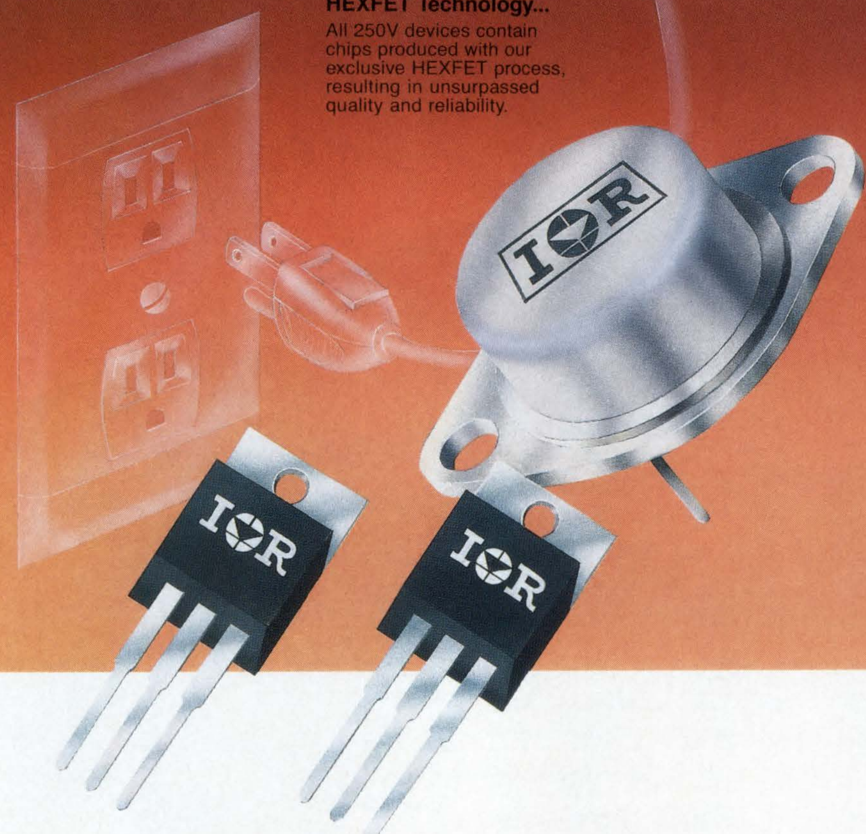

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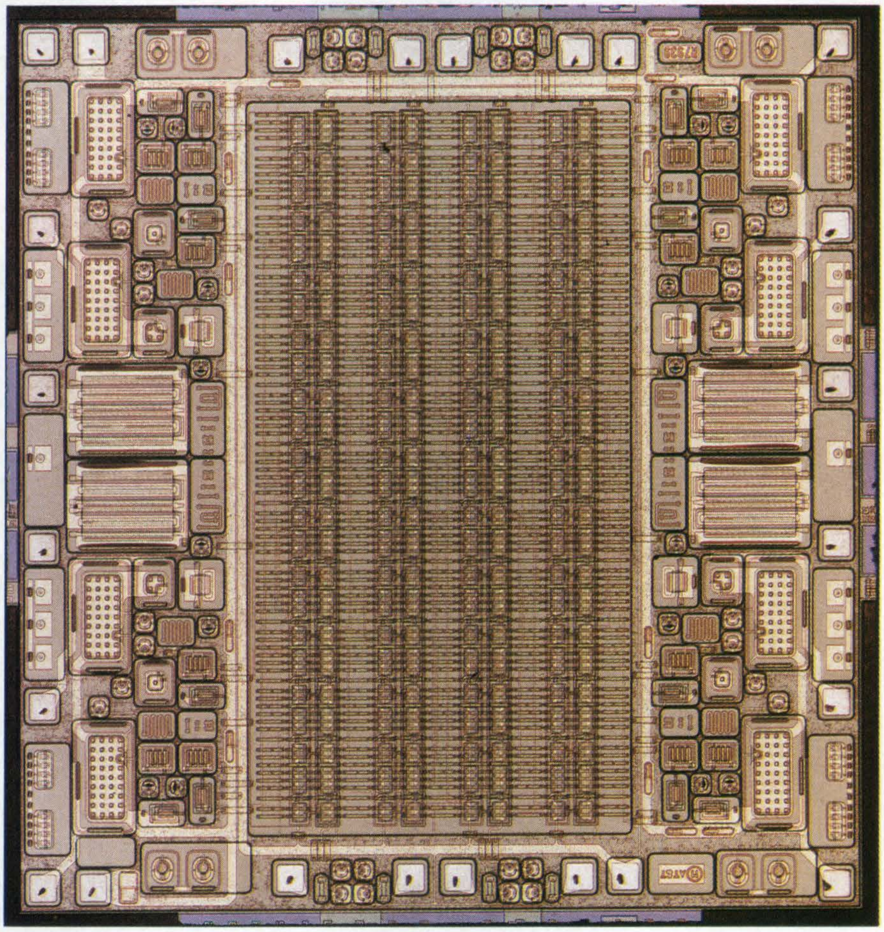
CIRCLE NO 61

Semicustom ICs' ratings and architectures aid analog- and digital-circuit designers

Dave Pryce, *Associate Editor*

The continuing introduction of new linear and linear-digital semicustom chips is providing an expanding choice of circuits to help you solve design problems. The trend to cell-type architectures is making it easier to design with linear semicustom circuits. Moreover, the availability of chips that can operate at VHF and UHF frequencies and at high voltages has extended the use of semicustom circuits to applications that semicustom technology heretofore couldn't serve. In addition, many of the new linear chips include built-in gates that you can use to implement digital functions on the same chip.



Standing above all others in the high-voltage hierarchy, *the ALA500 from AT&T has a rating of 250V. Fabricated in a BCDMOS technology with dielectric isolation, the chip includes 120 CMOS gates, 16 DMOS transistors, eight bipolar transistors, and 32 NMOS/PMOS transistors.*

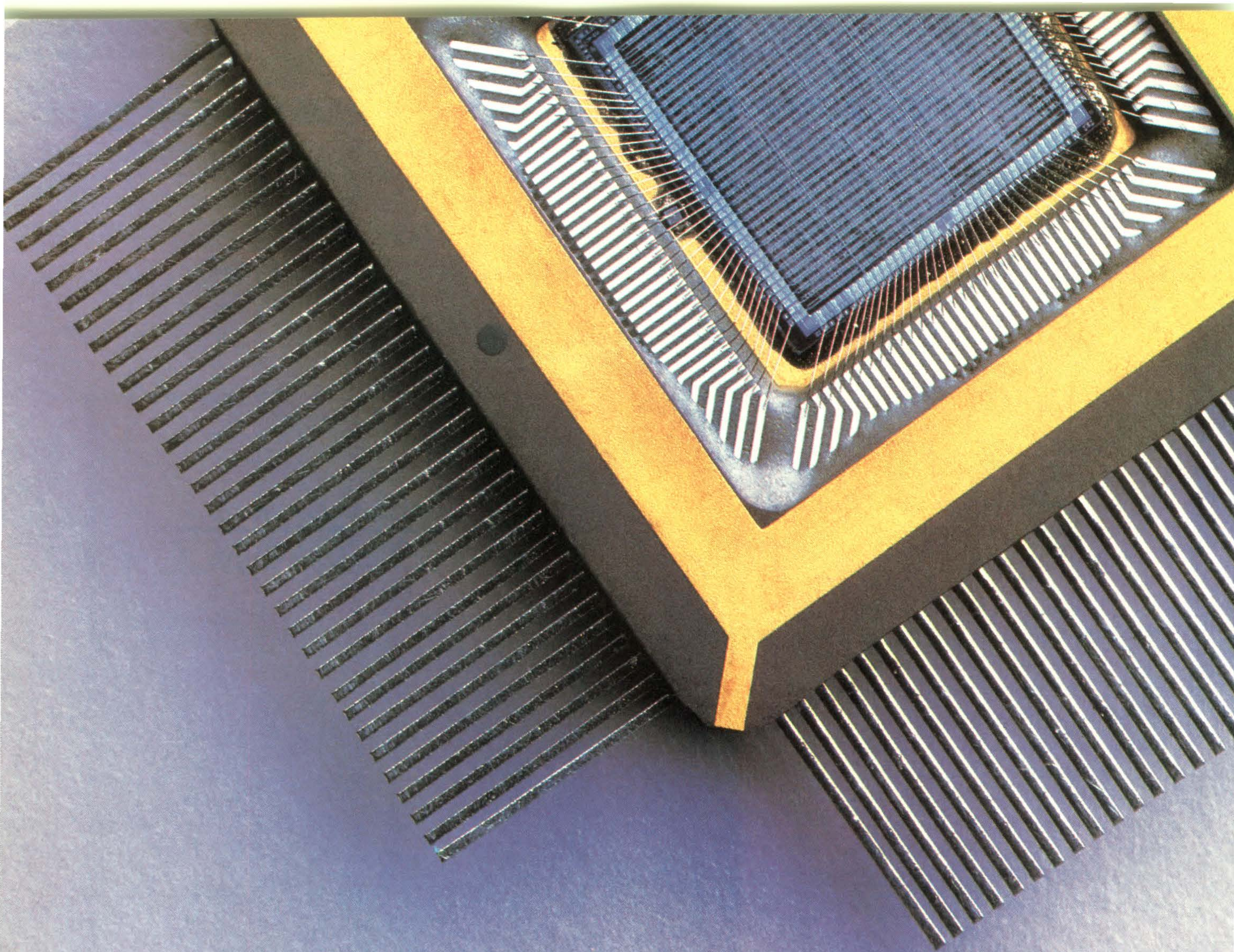
Breaking the gigahertz barrier

Typical of the UHF chips that follow the trend to cell-type layout are the ALA200 from AT&T, the QC-4 from Tektronix, and the VJ960 from VTC Inc. Each of these chips features npn transistors with gain-bandwidth products in the gigahertz range. The ALA200 and the VJ960 offer gigahertz-rated pnp transistors as well.

Fabricated in what AT&T calls a complementary bipolar integrated-circuit (CBIC) process, the ALA200 offers the advantages of similar npn and pnp transistor characteristics. The typical f_T is 4 GHz for the npn transistors and 2.5 GHz for the pnp transistors, thereby providing true complementary performance at VHF/UHF frequencies. In addition to the 133 npn and 85 pnp transistors, the array includes 984 ion-implanted resistors, whose resistance totals 1980 kΩ; 20 1- to 5-pF programmable capacitors; and two fixed 150-pF capacitors. The array is divided into 12 modules, consisting of eight standard, two power, one input, and one trim module.

KEEPING AMERICA COMPETITIVE

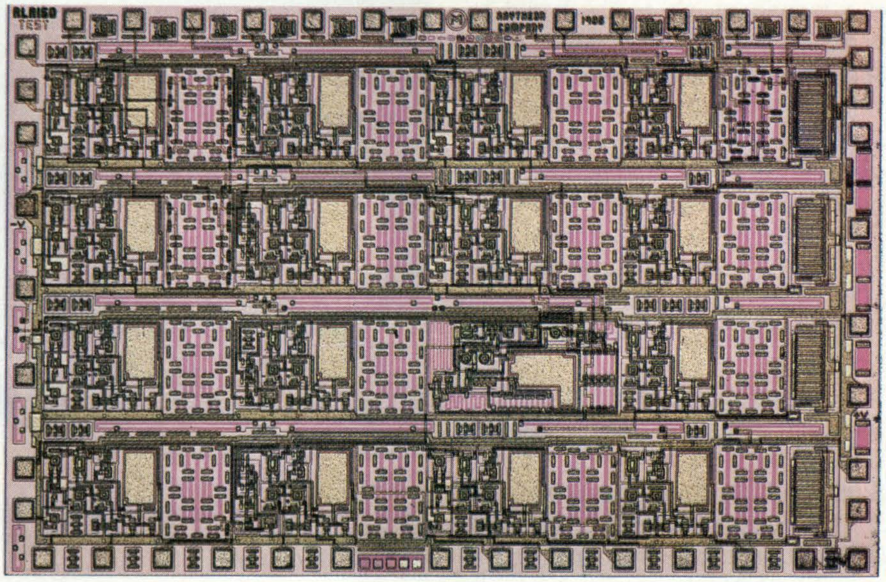
Tektronix is also addressing the demand for high-speed semicustom chips with its QC-4 Quickchip. Using the same process originally developed for the manufacturer's 1-GHz oscilloscope, the QC-4 chip combines digital and analog functions. The chip's ECL gate array has 300 equivalent gates with propogation delays under 400 psec. You can use these gates to implement multiplexers, decoders, latches, inverters, and TTL interfaces, for example.



Divided into tiles (or cells), the chip's analog portion includes 294 npn transistors with a typical f_T of 6.5 GHz. The chip's 174 pnp transistors are lateral and substrate types (see **box**, "A review of pnp and I²L basics") with a much lower cutoff frequency of 20 MHz. In addition to the gates and transistors, the large (196×196-mil) QC-4 chip contains 1290 resistors and 32 capacitors.

Tektronix has targeted the QC-4 for what it calls mixed-mode circuits that require a wide analog bandwidth along with fast, ECL-compatible outputs for digital control or data handling. Typical applications include interfaces to fiber-optic cables, high-speed modems, digital RF front ends, and test and measurement equipment.

The VJ960 from VTC is another cell-type linear chip that incorporates transistors with gigahertz cutoff frequencies. The f_T is 6 GHz for the npn transistors and 1 GHz for the true vertical (as opposed to substrate-type) pnp transistors. VTC refers to the cell-type structure as a block architecture. Whether one calls them cells, tiles, or blocks, their purpose is the same—the easy replication on the semicustom chip of library macrocell circuits such as op amps, comparators, references, S/H circuits, or logic elements. This approach eliminates the need for system designers to deal with the more complicated component-level design and layout of a semicustom chip. With a cell-type architecture, you need only concern yourself with standard (and familiar) IC functions.



A relative newcomer to the linear semicustom field, *Raytheon has recently introduced the RLA160 macrocell array. Among its other components are 15 user-configurable gain cells (each containing 10 transistors) and four large (200-mA) npn transistors. The thin-film resistors used in this array exhibit better tolerance and temperature-drift characteristics than do the diffused resistors used in most semicustom chips.*

The VJ960 is a relatively small chip designed primarily for high-frequency and -performance linear functions. It's divided into 12 blocks, each containing four vertical pnp transistors, six medium-size npn transistors, two low-noise npn transistors, two small Schottky diodes, and 10 resistors. Located around the periphery of the blocks are additional resistors and 26 capacitors.

Extending the voltage range

Although only a few manufacturers now offer semicustom chips capable of operating in the VHF/UHF range, the trend to higher frequen-

A review of pnp and I²L basics

For the edification of those designers unfamiliar with the characteristics of lateral and substrate pnp transistors and I²L gates, some explanation is worthwhile. The performance of the lateral pnp device is not nearly as good as that of the (vertical) npn transistor, particularly in terms of frequency response, gain, and maximum current. Current gain (beta) of a lateral pnp transistor generally falls off rapidly above 50 μA, and the gain-bandwidth product is typically in the 3- to 6-MHz range.

Although the substrate pnp transistor is a vertical device whose performance is somewhat superior to that of the lateral pnp device, it has two basic limitations: First, because its collector is connected to the substrate (ground), you can only use it as an emitter follower; second, it draws substrate current, generally requiring the use of an adjacent substrate contact to ground.

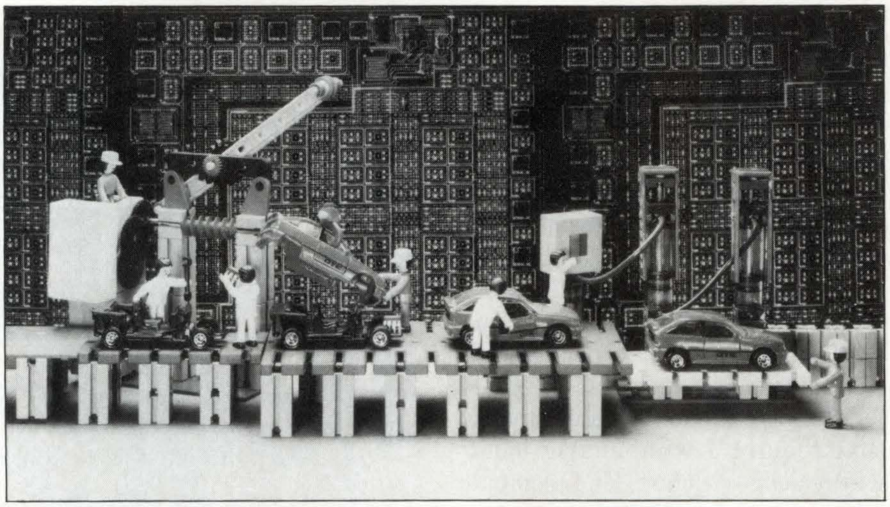
I²L (integrated injection logic) gates differ from most logic gates in that they are configured in a wired-AND technology having one input and numerous outputs instead of numerous inputs and one output. Design manuals from Motorola, Cherry, and Exar explain the construction and operation of I²L gates in detail. The main advantages of I²L gates are their low current consumption and the ease of incorporating them with linear bipolar elements on the same chip.

cies is evident. So is the trend toward higher voltages. Most semicustom chips operate at supply voltages in the 10 to 30V range, but several recently introduced types can operate at 50V and higher. Most notable are the Genesis 8000 (50V) from Cherry Semiconductor, the QC-3 (65V) from Tektronix, the MPD-8020 (100V) from Micrel, and the astonishing ALA-500 (250V) from AT&T.

Designed primarily for automotive and industrial-control applications, the CS-8000 from Cherry Semiconductor partitions 50V and 20V devices on the same chip. The 50V section contains a bandgap reference and 24 uncommitted transistors (six pnp, 16 low-power npn, and two high-power npn). The bandgap reference, which you can configure as a regulator, is capable of handling as much as 20 mA of current and is programmable from 1.25 to 20V. The two high-power npn transistors can drive 100-mA inductive loads. On-chip zener diodes provide protection.

The 20V section, which occupies about 60% of the total chip area, contains the remaining 70 transistors and most of the 427 resistors. In a typical application, you would operate the low-voltage transistors from the internal regulator and use the 50V transistors to provide the interface to the power source and to the output loads.

Partitioning the chip into two sections makes good sense: The division allows most of the circuitry to operate at low voltage and low current, thus permitting a significant reduction in total power consumption. Also, the more densely packed 20V components contribute to the effective utilization of the available chip area.

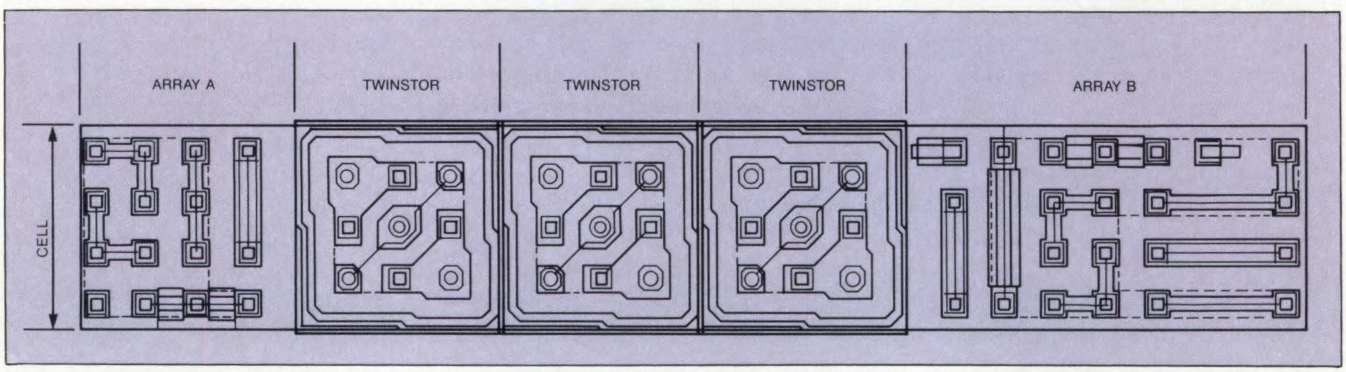


Designed primarily for automotive and industrial-control applications, *the Genesis 8000 chip from Cherry Semiconductor serves as a backdrop in this whimsical portrayal of its intended applications.*

The QC-3 Quickchip from Tektronix combines a 65V process with high-frequency capability in a partitioned cell-type architecture. The QC-3 has 198 npn transistors and 48 pnp transistors organized into six low-voltage (15V) cells and three high-voltage (65V) cells. The chip also includes 920 resistors and 28 programmable capacitors.

Both the high- and low-voltage npn transistors have a typical f_T of 2.5 GHz. The f_T of the pnp transistors is only 50 MHz, but that's a respectable rating considering that they are lateral- and substrate-type devices. Most lateral types, for example, are typically in the 3- to 5-MHz range. Resistors on the QC-3 are formed by implantation or thin-film nichrome deposition. The nichrome resistors have inherently tight tolerances and are laser trimmable. Typical applications for the QC-3 include high-output pulse generators, high-frequency analog multipliers, wideband amplifiers, and interface circuits.

Next up the ladder in the high-voltage hierarchy is the 100V MPD-8020 from Micrel. Fabricated in CMOS/DMOS, the MPD-8020 semicustom IC combines high-power capability and intelligence in a unique architecture. Micrel feels that it may well satisfy the frustrations of many design engineers who have heard of the promise and wonders of intelligent power but could not get



One of the most versatile linear arrays *is the Flexar Series from Exar. Shown here is a single cell containing three Twinstors and two resistor arrays. You can use the Twinstor as a pnp or npn transistor or as a resistor.*

their hands on any circuits suitable for their own applications.

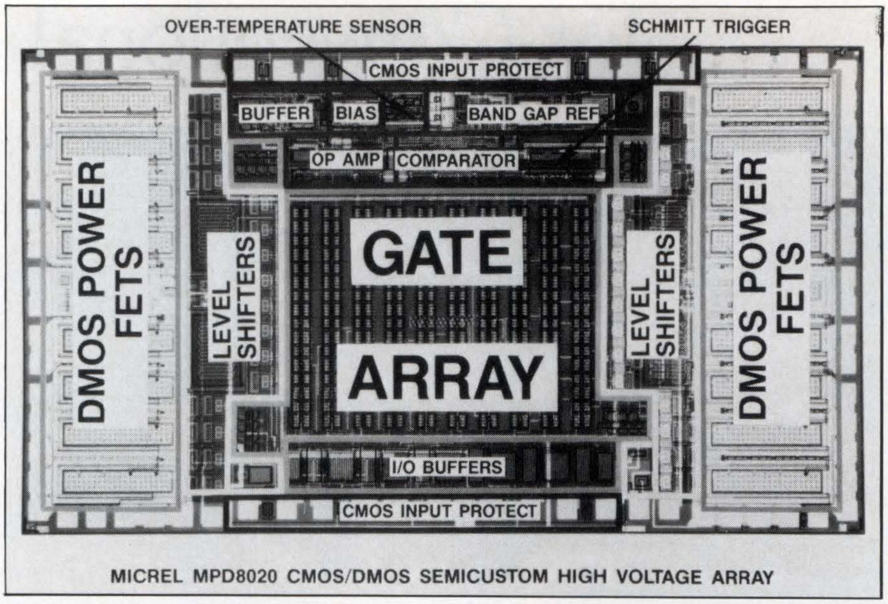
Although not strictly speaking a cell-type array, the MPD-8020 is modular in construction. It contains several basic sections, including 16 fully floating 100V/200-mA vertical DMOS transistors, 16 115V/20-mA level-shifters, 200 CMOS gates, 12 TTL/CMOS I/O buffers, three configurable op-amp/comparator/Schmitt-trigger cells, and a bandgap reference.

A single 5 to 15V supply powers the logic and analog circuitry while the high-voltage sections operate at voltages to 100V. The chip can also derive the 15V analog/digital supply from one 24, 48, or 100V supply. With the help of two external capacitors, an optional internal voltage pump can generate an extra voltage so that the high-side gates of the power n-channel DMOS FETs can be driven about 15V above the 100V supply. This feature provides rail-to-rail high-voltage switching for push-pull and H-bridge applications.

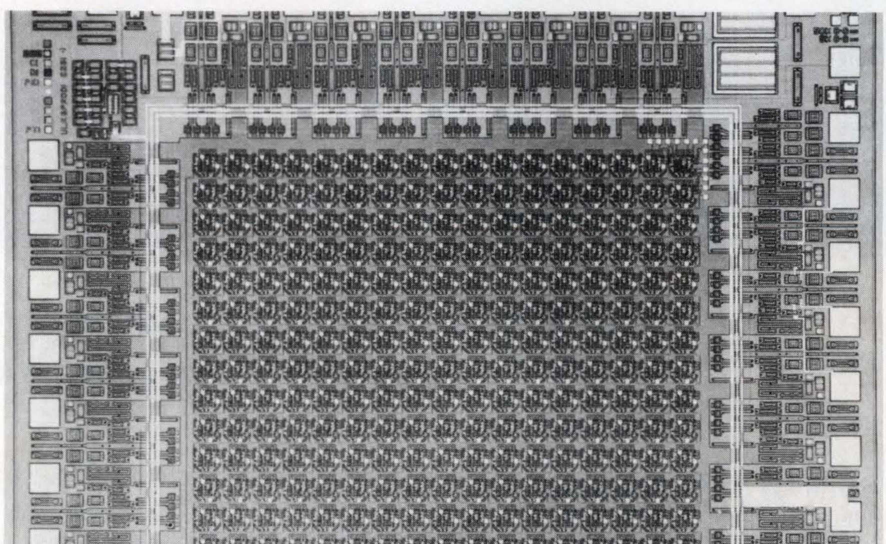
To assist the designer, Micrel can supply a number of kit parts containing discrete devices or the more popular analog and digital SSI and MSI circuits. The potential applications for this chip are numerous: They include switching-power-supply regulation; motor control; automotive switching; and relay, solenoid, lamp, and high-voltage-display driving.

Challenging Micrel for intelligent power semicustom-IC honors is the ALA-500 from AT&T. Although it differs considerably from the Micrel device in layout and component count, what really sets it apart is its 250V rating. The ALA-500 is fabricated in AT&T's high-voltage BCDMOS (Bipolar, CMOS, DMOS) technology with dielectric isolation. Implementation of the user's circuit is with single-level metal. The dielectric isolation eliminates parasitic effects caused by device interaction, making the chip essentially latch-up proof—an important requirement for high-voltage applications.

The breakdown voltage of the 24 high-voltage DMOS and PMOS transistors is 250V; that of the eight bipolar transistors is 150V. The other 24 NMOS and PMOS transistors and the 120 CMOS gates are rated at 20V. The chip's 44 polysili-



Employing a modular construction, *the MPD-8020 from Micrel includes 16 fully floating 100V/200-mA vertical DMOS transistors, 16 115V/20-mA level shifters, 200 CMOS gates, 12 TTL/CMOS I/O buffers, three op-amp/comparator cells, and a bandgap reference.*



Composed of matrix cells and peripheral cells, *the ULA-6P from Ferranti Interdesign includes 578 gates, 281 npn transistors, and 300 resistors with a combined value of more than 37 MΩ. Unlike Ferranti's G Series, the P Series emphasizes applications requiring more digital functions.*

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Rockwell's R144HD, a V.33 half-duplex modem for the public telephone network, offers 14.4 Kbps operation in facsimile and other imaging equipment, and also communicates at 12000, 9600, 7200, 4800, 2400 and 300 bps. It can transmit a page in less than 10 seconds, significantly lowering transmission costs.

It's optimized for use in Group 3 facsimile machines and is compatible with Group 2. It's small (13" square), low powered (2.5 W typical), and has a serial/parallel host interface and standard connector for a simple design in small spaces. It also has Automatic Adaptive Equalization algorithms, permitting virtually error-free transmission over poor phone lines.

Rockwell's R144DP, is a V.33 and V.29 compatible modem that permits high-speed transmission over all types of telephone lines by modems, multiplexers and network control equipment. Production quantities will be available in October.

It's VLSI-based design permits all necessary circuitry to be contained in less than 19 square inches, with automatic speed recognition and Automatic Adaptive Equalization.

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The R208/201 is two modems in one. During the synchronizing sequence, it automatically senses the mode of the other modem and switches to either Bell 208A/B or Bell 201C. This avoids costly upgrades and is ideally suited for expanding networks which use both types.

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VENDOR	TYPE NUMBER	V_{CC} MAX (V)	BOND PADS	GATES	DIODES	TRANSISTORS NPN (NMOS)	TRANSISTORS PNP (PMOS)	TRANSISTORS DMOS	RESISTORS QTY	RESISTORS TOTAL VALUE (kΩ)	NOTES
AT&T	ALA200	12	44			133	85		984	1980	UHF ARRAY
	ALA500	250	24	120	36	4 (12)	4 (20)	16	44	15,100	HIGH-VOLTAGE, DIGITAL-LINEAR
CHERRY	1500	12	30	98		126	72		464	814	DIGITAL-LINEAR
	8000	50	23		2	62	32		427	508	HAS 1.25 TO 20V BANDGAP REFERENCE
EXAR	BETA100	26	30			129*			594	1780	"FLEXAR" ARRAY
	BETA240	26	48			290*			1440	4280	"FLEXAR" ARRAY
FERRANTI	MV-G	40	28			140**			800	2839	12 CELLS
	ULA-6P	15	42	578		281			300	37,527	DIGITAL LINEAR, 36 LINEAR CELLS
HOLT	HI-5100	18	52	73		24 (87)	(88)		119	SEE DATA SHEET	DIGITAL-LINEAR
LINEAR TECHNOLOGY INC	LA252	20	32		6	116	34		SEE DATA SHEET	1790	"MODULA" ARRAY
MCE	A40AS	40	16			60	28		157	357	IMPROVED A40A
MICREL	MPD8020	100	78	200	SEE DATA SHEET			16	SEE DATA SHEET		HIGH-VOLTAGE INTELLIGENT MODULAR ARRAY
MICRO LINEAR	FB324	12	28	50		330	82		1068	3605	24-TILE ARRAY
MOTOROLA	MLA300	20	38	64		168	52		742	2678	MILL SCREENING AVAILABLE
RAYTHEON	RLA120	32	24			43	16		196	965	12 GAIN CELLS
TEKTRONIX	QC-3	65	28			198	48		920	1027	HIGH-VOLTAGE ARRAY, NINE CELLS
	QC-4	10	66	300		294	174		1290	1383	UHF CELL TYPE, LINEAR-DIGITAL
VTC	VJ960	12	28		74	108	56		120	468	UHF BLOCK-TYPE ARCHITECTURE

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con resistors provide a total resistance of more than 15 MΩ.

Although the availability of high-frequency and high-voltage semicustom circuits opens up many new application possibilities, the majority of circuit designs are satisfied with chips having considerably lower frequency and voltage ratings. Among the most versatile are the Flexar arrays (flexible linear array), which Exar introduced about 18 months ago.

The present Flexar line includes three types: the 100, 180, and 240—each varying in size and total number of components. All are cell-type arrays, but that's where any similarity to other semicustom chips ends. The key elements to the versatility of the Flexar arrays is what Exar calls Twinstors, Padstors, and Twinboosters. Each of these unique elements has a multiple personality.

The Twinstor—a programmable dual transistor whose polarity is set at the metallization step—is the work horse of the arrays. It can act as a dual npn device with a common collector, as a lateral dual-collector pnp device, or as a single or matched resistance element.

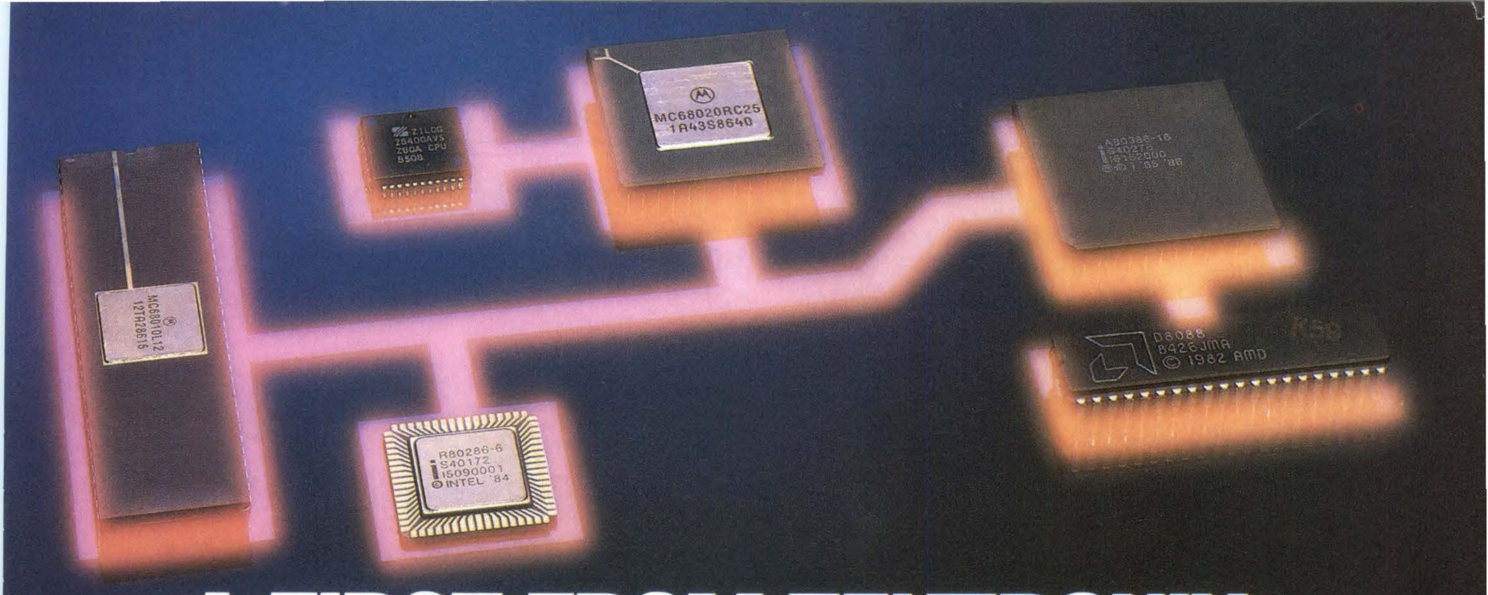
The Padstor can function as a standard bonding pad, a single or multi-emitter npn transistor, a pnp transistor, a clamp diode, a capacitor, or two resistors.

The Twinbooster is available only on the 240 chip, which includes two of them. The Twinbooster can function as a 500-mA npn transistor or as a 50-mA pnp transistor.

The architecture of the Flexar array is built around a flexible cell that needs only a single metal mask. The cell is replicated throughout the series to enable the duplication of a circuit layout anywhere within an array or on a different array. This replication shortens design, layout, and digitizing time. If you use the available soft-cell library, you can reduce the layout phase to a matter of hours or days instead of the weeks usually required.

Interdesign originated semicustom circuits some 15 years ago. Now doing business as Ferranti Interdesign, it has several series of semicustom chips in bipolar and MOS technology. Two of its newest series of semicustom chips are the ULA-P Series, a digital-linear combination that operates at 15V, and the MV Series, a linear series capable of operating at 40V. Both series employ a cell-type architecture.

An example of the trend to providing digital and analog functions



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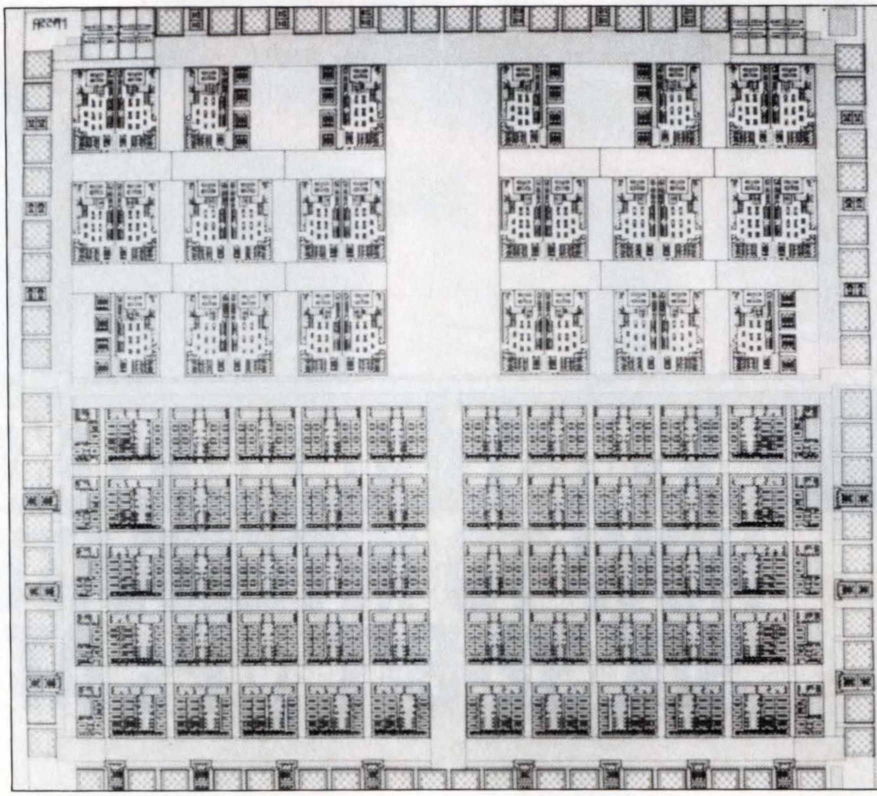
on the same chip is the ULA-6P. Contrary to Ferranti's G Series, the P Series emphasizes applications requiring more digital than analog functions. The ULA-6P has 578 gates in 289 matrix cells that take up about 57% of the total chip area. Each matrix cell contains components that, when connected in the simplest form, provide 2-input NOR gates. There are two speed-power options for each array in the series. Clock rates can vary from 400 kHz to 4.8 MHz, depending on the option chosen and the amount of gate current provided.

Component cells specifically designed for analog functions occupy the peripheral area of the chip, whose 32 standard peripheral cells contain a range of transistors and resistors for the implementation of a variety of linear functions and I/O interfaces. Special peripheral cells are located at each corner of the chip and include functions such as high-current drive transistors, low-offset transistors, a bandgap reference, and shaping capacitors.

The MV-G 40V chip is a linear-only array comprising 12 cells. Each cell contains 16 npn transistors, four pnp transistors, 36 diffused resistors with a total value of 44 kΩ, and 12 10-kΩ implanted resistors. Additional peripheral devices include 5-mA, 10-mA, and 50-mA npn transistors, substrate-type pnp transistors, and 5-pF capacitors. The mix of components and the cell-type structure provide high device utilization and ease of layout.

The MV family of devices is the product of a joint development between Ferranti Interdesign and Custom Arrays Corp. Each company has independent marketing and manufacturing rights and can act as a mask-transferable alternate source—a service that is not possible with most semicustom chips.

Reinforcing the trend to combination analog-digital chips are devices from Cherry, Holt, Micro Linear, and Motorola—a newcomer to the semicustom field.



To meet the demand for high-speed semicustom chips, *Tektronix introduced the QC-4. It contains 300 ECL gates with propogation delays of less than 400 nsec; its analog portion contains npn transistors that have a typical gain-bandwidth product of 6.5 GHz.*

The Genesis 1500 from Cherry Semiconductor is intended for single-chip integration of complete systems, and its fairly large size of approximately 17,000 mils^2 will accommodate moderately complex designs. Within the limitations of its 12V rating (a consequence of its 98 I^2L gates), it's a versatile device. A characteristic of I^2L gates is their good speed-power product, and at reasonable toggle rates they require little current. It's possible to operate the Genesis 1500 at currents as low as 0.1 μA per gate.

Apart from the gates, the chip is arranged in a quasi-tile layout that includes 122 small npn transistors, four large npn transistors, 72 pnp transistors, and 462 base resistors. The large npn transistors can handle currents as high as 150 mA.

The HI-5100 from Holt Integrated Circuits is a CMOS analog-digital array fabricated in 4-μm silicon-gate technology. Gate oxide between the chip's polysilicon layer and an implanted p-diffusion forms the chip's capacitors. The selection and location of the digital and analog components are suited for implementing switched-capacitor-filter circuits, among others.

The digital section contains standard gate-array elements such as TTL- and CMOS-compatible input/output cells, three 2-transistor arrays, and 14 dedicated set/reset D flip-flops. The analog section includes transistors, resistors, and capacitors. Although intended primarily to simulate analog or analog-digital circuits for use in custom circuits, the HI-5100 is useful in some applications as a stand-alone semicustom product.

The FB324 from Micro Linear combines a matrix of six general-purpose tiles and 16 high-performance tiles with a reference tile and a special-function tile. Each general-purpose tile can contain one or two op amps or comparators, or any of the other predefined macrocells from the FB300 family. The high-performance tiles support new,

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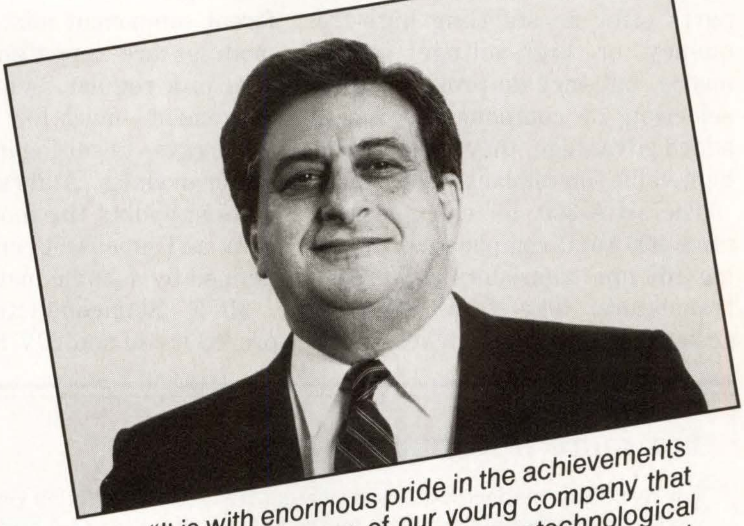

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higher-speed macrocells such as a 100-MHz cascode amplifier, an ECL-type D flip-flop, a high-speed comparator, or a 60-MHz wideband video amplifier. A total of 1643 components is available for analog design. It's possible to implement a total of 50 ECL gates by using 192 npn transistors from the high-performance tiles.

Motorola, a long-time supplier of custom circuits, has only recently entered the semicustom field with a series of three general purpose types: the MLA-150, -300, and -600. Basically similar to some of the first- and second-generation circuits still available from Interdesign, Exar, Cherry and others, the Motorola parts offer no startling high-frequency or high-voltage performance, but they do provide a good selection of components. As an added advantage, they include some high-value ion-implanted resistors.

The MLA-300, for example, contains 990 total components, including 168 npn transistors and 52 pnp transistors. The total diffusion resistance is 578 kΩ. The ion-implanted resistance is normally 2.10 MΩ and optionally 5.15 MΩ. The 164 small npn transistors have f_T specs in the 350- to 400-MHz range. The chip's four power npn transistors can handle up to 100 mA. The remaining active devices include 52 lateral- and substrate-type pnp transistors and 64 I^2L gates.

Linear Technology Inc of Burlington, Ontario, has a new series of semicustom linear arrays that are layed out in modular (tile, cell) form. Each of the three LA250 Series arrays has a highly regular core section surrounded by a variety of specialized peripheral components. The core is built of two types of building blocks, each having a different component mix. These basic modules are repeated across the core in a regular, symmetrical arrangement—much like other cell or tile arrays—resulting in a variety of larger modules. A library of subcircuits supports the modular structure, and subcircuit connections are defined by a single metal mask.

MCE Semiconductor has improved its 40 and 20V linear arrays (an S suffix denotes the improved versions) by adding a deep n+ "sinker" diffusion through the epilayer to the buried layer. The lowered collector-emitter resistance reduces the saturation voltage of the transistors and provides an increase in the maximum current capability—typically two times that obtainable without the extra diffusion. (Cherry Semiconductor offers a similar option on most of its 20V linear arrays.) Later this year, MCE expects to announce the availability of a new line of macrocell linear arrays ranging in size from 2 mm square to 15 mm square, with the largest array containing about 1600 components.

Raytheon, another relative newcomer to the linear semicustom field, offers the RLA80, RLA120, and RLA160 macrocell arrays. All can operate from 2 to 32V (±1 to ±16V). The newest chip, the RLA160, has 15 user-configurable gain cells, each containing 10 transistors. Other components include 43 small npn transistors, four large (200 mA) npn transistors, 10 small

For more information . . .

For more information on the semicustom ICs discussed in this article, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

AT&T Technologies
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2000 S County Trail
East Greenwich, RI 02818
(401) 885-3600
Circle No 702

Custom Arrays Corp
525 Del Ray Ave
Sunnyvale, CA 94086
(408) 749-1166
TWX 510-600-5119
Circle No 703

Exar Corp
750 Palomar Ave
Sunnyvale, CA 94086
(408) 732-7970
TWX 910-339-9233
Circle No 704

Ferranti Interdesign Inc
1500 Green Hills Rd
Scotts Valley, CA 95066
(408) 438-2900
Circle No 705

Holt Integrated Circuits Inc
9351 Jeronimo Rd
Irvine, CA 92718
(714) 859-8800
TLX 753307
Circle No 706

Linear Technology Inc
Box 489, Station A
Burlington, Ontario, Canada L7R-3Y3
(416) 632-2996
TLX 061-8525
Circle No 707

MCE Semiconductor Inc
1111 Fairfield Dr
West Palm Beach, FL 33407
(305) 845-2837
TLX 441405
Circle No 708

Micrel Inc
1235 Midas Way
Sunnyvale, CA 94086
(408) 245-2500
TWX 910-379-0007
Circle No 709

Micro Linear
2092 Concourse Dr
San Jose, CA 95131
(408) 262-5200
TLX 275906
Circle No 710

Motorola Inc
1300 N Alma School Rd
Chandler, AZ 85224
(602) 821-4426
Circle No 711

Raytheon Co
Semiconductor Div
Box 7016
Mountain View, CA 94039
(415) 968-9211
TWX 910-379-6484
Circle No 712

Tektronix Inc
Box 500, MS 59-420
Beaverton, OR 97077
(503) 627-7111
TWX 910-467-8708
TLX 151754
Circle No 713

VTC Inc
2401 E 86th St
Bloomington, MN 55420
(612) 851-5000
TLX 857113
Circle No 714

pnp transistors, and 240 resistors.

The RLA chips are primarily composed of op-amp/comparator cells and thin-film resistors. Unlike diffused resistors, the thin-film variety exhibits tolerance, temperature-drift, and matching characteristics comparable to those of many types of discrete film resistors. You can connect the cells and the chips' other components to form current sources, detector/amplifier circuits, voltage references, active filters, voltage-to-current converters, timers, data-conversion circuits, and many other types of analog functions.

A review of these new linear and digital-linear semicustom chips makes it clear that their manufacturers are extending the performance and application boundaries. High-frequency chips are penetrating the VHF/UHF range, and high-voltage chips are opening up applications that previously could be implemented only with standard ICs, hybrids, or discrete devices. Designers can now use cell-type arrays to implement system-level designs that include low-level analog and digital functions as well as high-power circuitry.

In addition to wider application possibilities, higher performance, and easier design, semicustom circuits continue to offer their traditional advantages. They offer lower NRE costs and faster turnaround than full-custom implementations would, yet they permit the realization of a proprietary circuit dedicated to a specific application. All of these advantages are combining to enhance the competitiveness of OEM purchasers of semicustom chips. **EDN**

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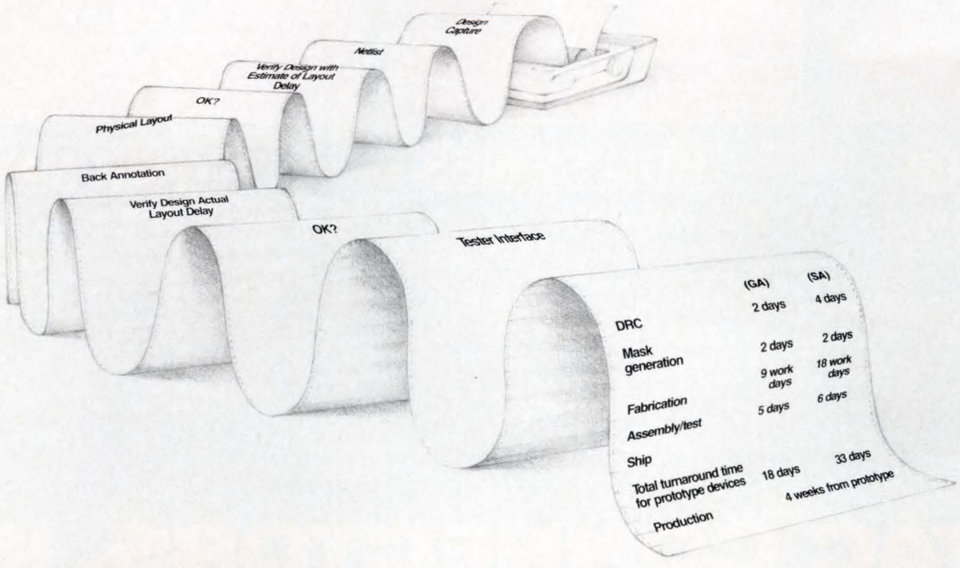

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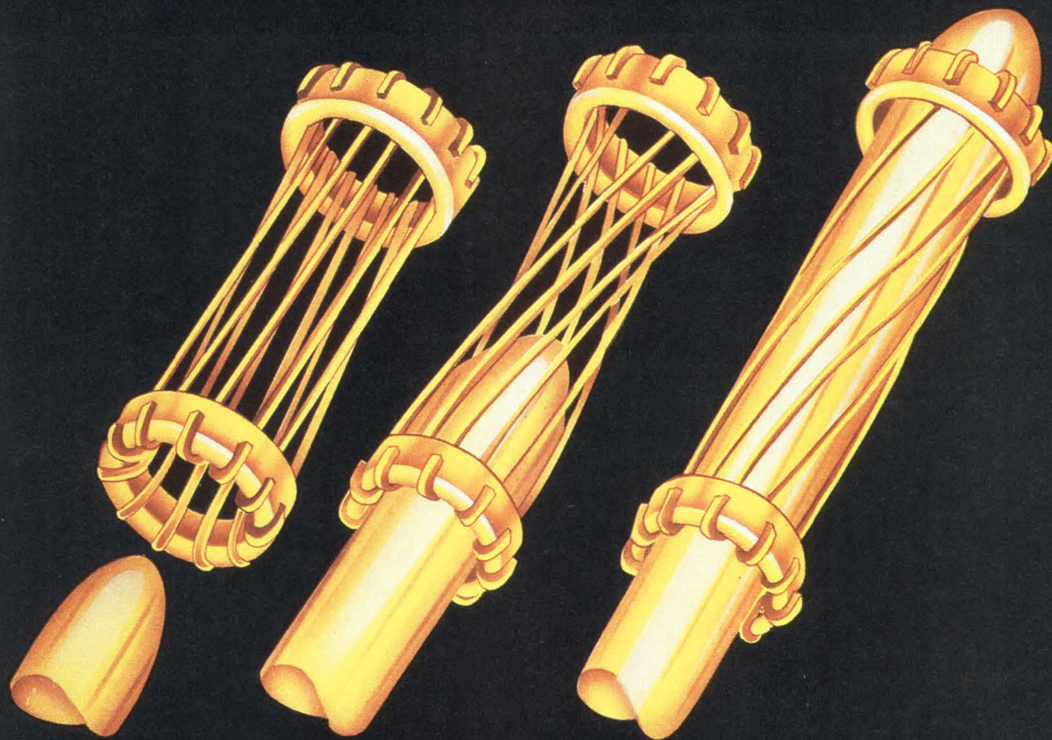

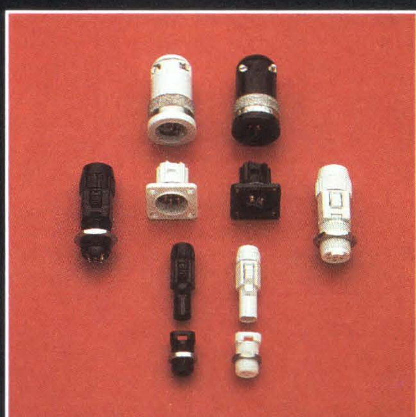

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Self-calibration and oversampling make room for more digital circuitry on monolithic ADCs

Jim Wiegand, *Associate Editor*

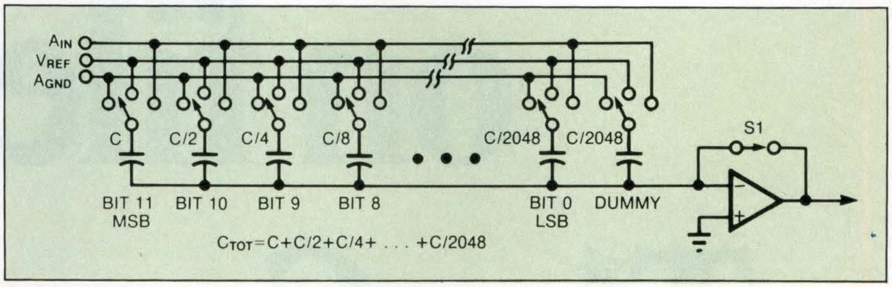

Fig 1—A charge-redistribution D/A converter *employs an array of binary-weighted capacitors rather than a resistor-ladder network to effect a D/A conversion. One advantage of the capacitor approach is that it eliminates the laser-trimming process step that the resistor-ladder method requires.*

Although proven A/D-converter designs migrated from hybrid to monolithic circuits in the early 1980s, their basic configuration hasn't really changed much since the 1960s, when ADCs were implemented in discrete components. Now, however, a different approach to A/D conversion is becoming increasingly popular. Manufacturers are using self-calibration and oversampling techniques to incorporate more digital circuitry than analog circuitry on these ADCs.

The new techniques provide some clear benefits. The self-calibration feature allows manufacturers to loosen the tolerances on the chips' analog circuitry by relaxing process sensitivities and complexities. Furthermore, it aids you in producing affordably manufacturable systems: Self-calibration lets you manufacture systems without potentiometers to autozero the ADCs, thus reducing manufacturing costs.

Also, because they can recalibrate themselves, these ADCs can adjust to changes over temperature and time. And because the chips use more digital circuitry, which takes up less space than analog circuitry, manufacturers are incorporating more functions—such as μP interfaces—on a single chip.

Some self-calibrating ADCs also use oversampling, a digitally intensive conversion method. Because of its complexity and its concomitant speed penalty, oversampling is most suitable for use in applications that involve audio-frequency and low-frequency signals.

In his keynote address at last February's International Solid-State Circuits Conference, Robert W Broderson, professor of electrical engineering at the University of California at Berkeley, noted that oversampling might allow manufacturers to eliminate the need for precision analog circuitry in A/D and D/A converters. In fact, Broderson stated, "it is likely that soon this approach will dominate the analog interface in most voiceband system applications, since the A/D conversion can be accomplished in standard digital technology, without added process steps" **(Ref 1).**

Self-calibrating ADC

A number of A/D converters that employ self-calibration and oversampling techniques are now available. Crystal Semiconductor, for example, offers the $59.34 (1000) CS5016, a 16-bit self-calibrating ADC that converts an input signal over the ±4.5V range in 16 μsec. The self-calibration technique allows the 16-bit converter to provide maximum nonlinearity of 0.0015% of full scale.

The CS5016 consists of a D/A converter (DAC), a track/hold amplifier, a conversion and calibration microcontroller, a comparator (a 1-bit ADC), μP-compatible 3-state I/O buffers, and calibration circuitry. The input track/hold amplifier acquires the analog input signal within 3.75 μsec after each conversion, allowing throughput rates as high as 50 kHz.

The CS5016 uses a successive-approximation technique to effect the A/D conversion. Like all successive-approximation converters, the CS5016 compares the analog input to the output of a DAC, which is controlled in accordance with the conversion algorithm. The DAC output is set to half the full-scale value (the most significant bit is on; all other bits are off). If the analog input is greater than or equal to the DAC output, then the corresponding bit in the ADC's output is set to one, and the next DAC output is tested against the analog input. In this way, each bit, from the most significant to the least significant, is successively tested against the analog input.

Unlike other successive-approximation converters, in which the internal DAC is based on a laser-trimmed resistor-ladder network, the CS5601 uses an array of binary-weighted capacitors to effect a charge-redistribution DAC **(Fig 1).** This DAC has an inherent track/hold

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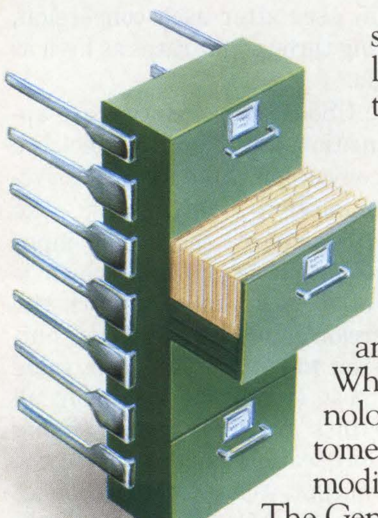

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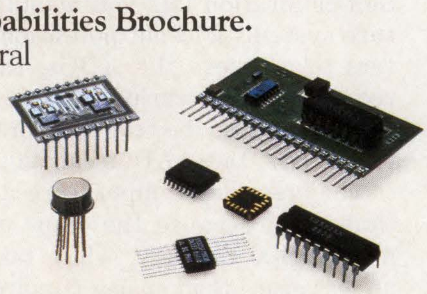

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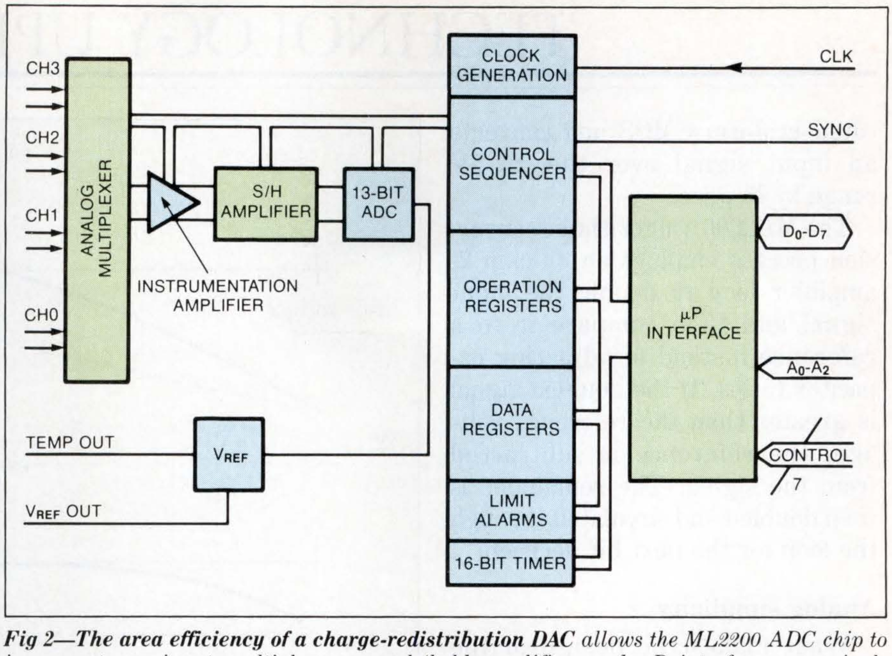

Fig 2—The area efficiency of a charge-redistribution DAC *allows the ML2200 ADC chip to incorporate an input multiplexer, sample/hold amplifier, and μP interface on a single chip.*

function, and it allows the chip to provide high-resolution conversion.

A charge-redistribution DAC stores, on a capacitor array, a charge that's proportional to the analog input signal. The floating side of each of the capacitors is connected to the input of a comparator. An on-chip controller then switches the other side of each capacitor either to analog ground or to a reference voltage, as the conversion algorithm specifies. As more capacitors are connected to ground, the common side of the capacitor array is forced to a more negative voltage.

Because the charge originally stored on the capacitors is constant, the charge at the floating node of the comparator remains constant. Therefore, the controller switches the capacitors between reference voltage and ground until the voltage at the floating input equals zero. At this point, the ratio of the capacitance connected to ground to the capacitance connected to the reference voltage represents the ratio of the input voltage to the reference voltage.

The charge-redistribution DAC technique lends itself to self-calibration. Because each of the binary-weighted capacitors can actually be a composite of several smaller capacitors, the capacitors in the array can be adjusted (that is, switched in and out of the array as needed) to provide a ratio of capacitances that provide the proper weighting between digital steps. During the calibration process, an on-chip microcontroller adjusts each of the bit capacitors: It switches the component capacitors of the bit capacitor into or out of the array until the value of the bit capacitor is equal to the sum of the capacitance of the lower-bit capacitors plus one LSB.

In addition to fulfilling the requirements for a highly accurate DAC, the CS5016 has an accurate comparator. The device uses an autozeroing technique to null errors introduced by the comparator. All offsets presented to the comparator are stored on the capacitor array while the ADC is in the track mode. The offset errors are then subtracted from the input signal when a conversion is initiated.

The CS5016 uses statistical noise-reduction techniques to calibrate the DAC to within ±¼ LSB at the time the device is first powered up. You can initiate subsequent calibrations to adjust for temperature drift and aging at any time.

Oversampling ADC

Besides simplifying the calibration process, the charge-redistribution architecture is naturally suited to the oversampling method of A/D conversion, primarily because it has an inherent sample/hold function. Crystal, for example, bills its $39.38 (1000) CS5014 as an oversampling converter as well as a self-calibrating device. This 14-bit ADC can convert an input signal over the ±4.5V range in as little as 14.25 μsec, allowing throughput rates as high as 56 kHz.

The basis for the oversampling technique is the fact that, by sampling a signal at a frequency much higher than twice the Nyquist frequency, one can spread the quantization noise of the ADC into a much broader frequency spectrum than that of the signal being converted. This action diminishes the power level of the quantization noise within the signal's frequency band and moves the noise energy to a higher frequency. After the noise energy has shifted, you can eliminate the noise with a digital-signal-processing technique called decimation.

As with the CS5016, you can recalibrate the CS5014 at any time and in a variety of modes. If you wish to calibrate the part in background mode, for instance, you can interleave the calibration process with the data-acquisition process. If, on the other hand, you need to recalibrate quickly—for example, when your system detects an abrupt change in its own temperature—you can use the "burst cal" mode. This quick recalibration overcomes the drifts introduced by rapid temperature change.

ADCs have size advantage

Another advantage of this self-calibrating, oversampling converter is its size. Because it uses more digital than analog circuitry, the chip can include more functions than a purely analog chip of the same size could contain. The size advantage that sampled-data A/D converters give you is evident in the ML2200 Data-Acquisition Peripheral, a 13-bit, 8-channel, self-calibrating analog-interface system from Micro-Linear (**Fig 2**). The device is fabricated in 3-μm CMOS and converts an input signal over the ±2.5V range in 25 μsec.

The ML2200's algorithmic conversion process employs an on-chip 2-amplifier loop to double the input signal and then compare it to a reference instead of adjusting capacitor ratios. If the doubled signal is greater than the reference voltage, the reference is subtracted from the signal. The remainder is then doubled and circulated through the loop for the next bit decision.

Analog simplicity

What makes the design of the ML2200 simple is that there's only one requirement for achieving ±0.5-LSB accuracy in the conversion process: The manufacturer must limit offsets within the conversion loop to less than 0.5 LSB. This requirement is the most basic limitation on the converter's accuracy, and the manufacturer satisfies it by using an offset-nulling, self-calibrating scheme. The offset-nulling scheme removes the op-amp offsets and cancels charge injection as well. The offset error is eliminated at the beginning of each conversion by the autozeroing circuits contained in the sample/hold amplifier and in the multiplying amplifier.

The ML2200 converter's linearity depends upon only two parameters, the gain and offset errors. The self-calibration circuitry limits the gain error by measuring the 2× gain of the loop and then adjusting the gain as necessary: The device measures gain by performing an A/D conversion on the internal voltage reference. In the ideal case, the result of the conversion would be all ones (that is, a full-scale value). If the loop gain is slightly less than 2, the resulting LSB of the conversion will be zero, and the on-chip controller will adjust the loop gain upward. On the other hand, if the result of the conversion is all ones, the loop gain may be too great; if so, the converter reduces the loop gain until the threshold value of the LSB is reached. The converter adjusts the loop gain by tuning binary-weighted input capacitors.

You can initiate the calibration process for the ML2200 by setting the CAL bit in the chip's control register. The self-calibration process requires 2 msec to execute; the chip generates a "calibration-complete" interrupt at the completion of the process. This interrupt output allows you to redirect the host processor to other tasks while the self-calibration is under way. The ML2200 costs $60 (1000).

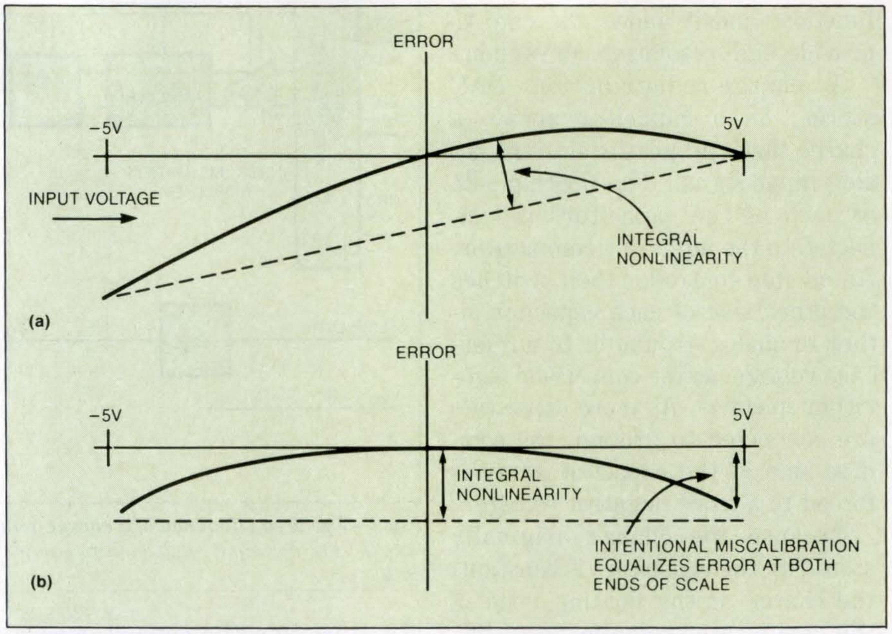

Fig 3—You can distribute the integral nonlinearity *of the AD1170 A/D converter in a way that minimizes the nonlinearity for positive voltages **(a)**, or you can distribute the nonlinearity over the entire operating range of the ADC **(b)**.*

Adjustable calibration

Another approach to self-calibrating converters—one which doesn't calibrate on a bit-by-bit basis—is represented by the AD1170 from Analog Devices. The AD1170's self-calibration process favors the positive-voltage-range conversion for applications such as temperature measurement. For other applications, however, you can adjust the self-calibration process to distribute the integral nonlinearity evenly over the positive and negative voltage ranges.

Specifically, the AD1170 normally performs self-calibration internally at 0 and 5V, not at −5 and +5V. This calibration process results in the error curve illustrated in **Fig 3a**. As the figure shows, this technique tends to exaggerate the relative error at the negative end of the scale and to reduce the error for input voltages between 0 and 5V. This calibration suits systems that measure or convert positive signals, such as those from thermocouples.

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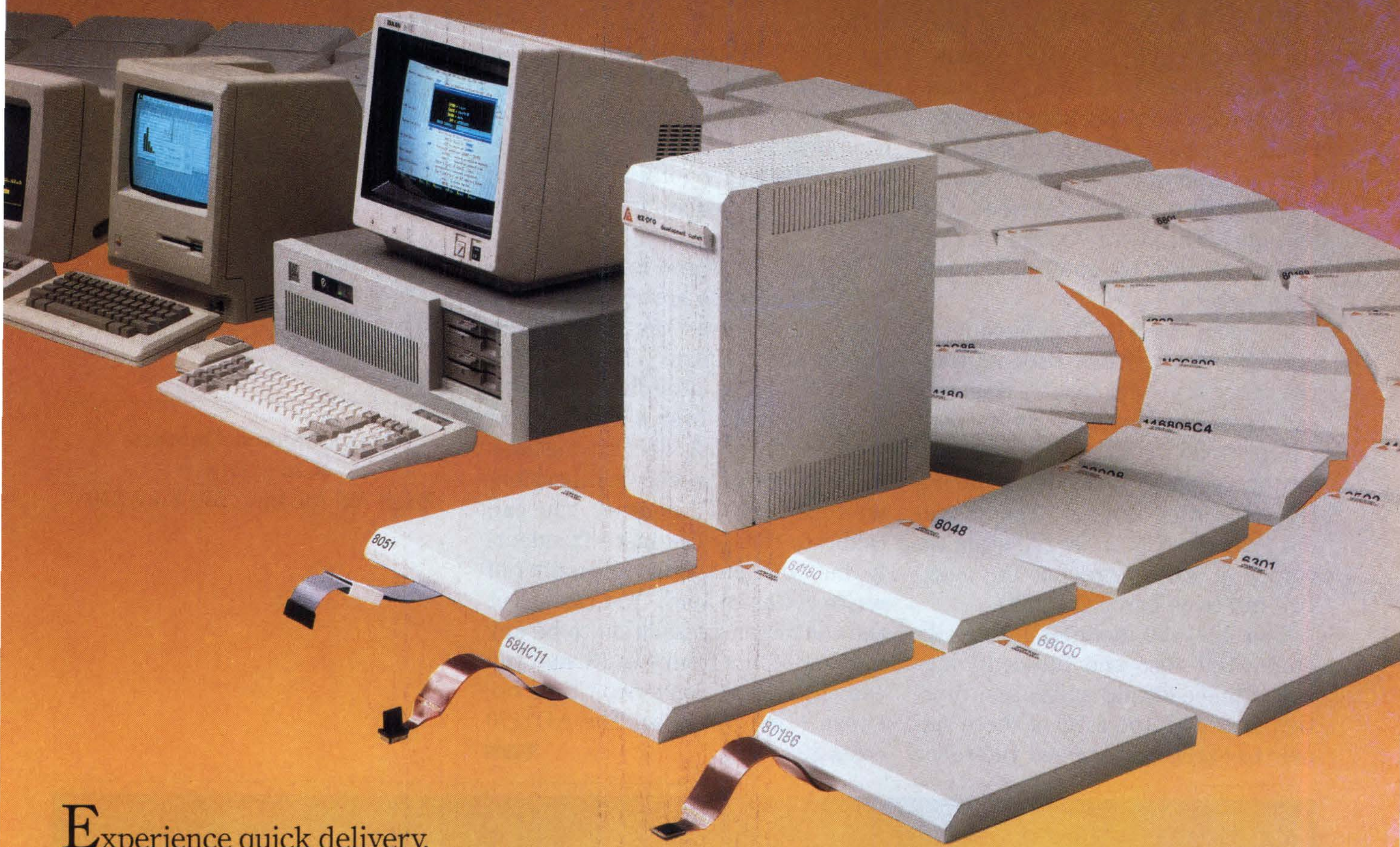

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The manufacturer claims the part has no more than ±0.001% nonlinearity; this spec is an endpoint measurement, and it excludes any gain or offset errors. (Endpoint nonlinearity is the typical deviation from a straight line drawn between the outputs of the charge-balancing converter at the +5 and −5V input extremes.)

To make the ADC's integral nonlinearity synonymous with its relative accuracy, you must externally calibrate the converter at its endpoints; to do so, you must intentionally introduce a span error during the calibration process. This procedure sacrifices positive full-scale accuracy in order to reduce the negative full-scale error (**Fig 3b**).

The AD1170 includes internally generated zero and full-scale signals. Its electronic-calibration function measures the ratio of these signals to externally applied reference voltages, in order to determine the ratio of the internal reference to the external reference. This ratio is applied to all the subsequent math computations in the conversion process, effectively compensating for errors in the device's internal reference.

The ratio is stored in RAM in the AD1170 until the host issues a command that stores the ratio in the chip's nonvolatile RAM. The AD1170's nonvolatile RAM is specified to operate over a minimum of 1000 write cycles, which translates to 19 years of weekly calibration/write cycles. Of course, you can calibrate the device more frequently, but you must limit the number of write cycles to 1000. You can select the converter's resolution to be any number of bits from 7 to 18, and you can choose any conversion time between 1 and 350 msec. The AD1170 costs $98 (100). **EDN**

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3. Adams, Robert W, "Design and implementation of an audio 18-bit A/D converter using oversampling techniques," 78th Convention of the Audio Engineering Society, New York, NY, 1985.

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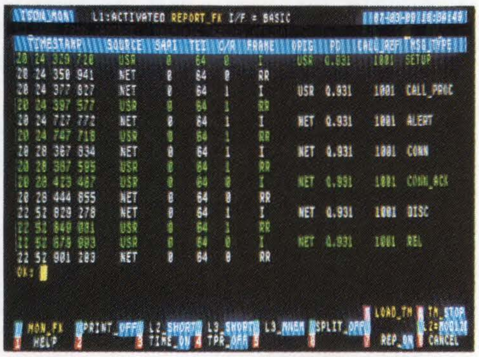

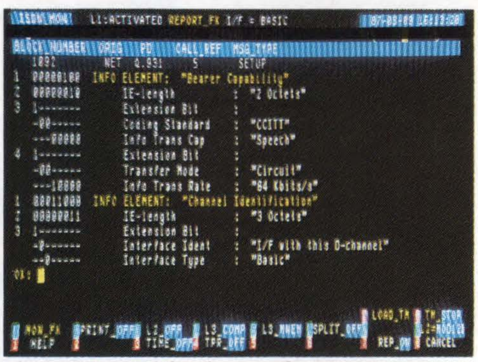

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Mountain View, CA (415) 964-5500
Norcross, GA (404) 925-9199

San Diego, CA (619) 571-7905
Wilmington, MA (617) 657-8400

Mississauga, Ontario (416) 624-6132

Nationwide (800) 423-2337
California Only (800) 232-2173

Electro Rent Corporation

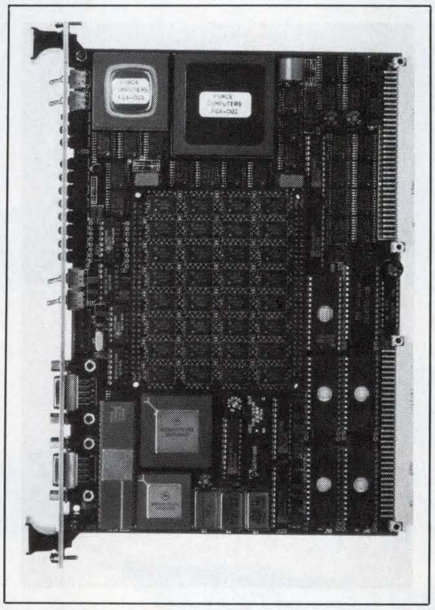
CIRCLE NO 49

68020-based CPU board expands VME Bus for message-passing operations

Although the 68020-based CPU-22/23 board for the VME Bus includes many useful features, its outstanding feature is the ability to support message-passing operations. Message passing lets any processor broadcast a message to other processors at any time. Such 8-bit messages might include information about a processor's status and its interrupts. The CPU-22/23 board includes two 8-byte, first-in/first-out (FIFO) memories that store incoming and outgoing messages.

The manufacturer claims that any 32-bit VME Bus CPU board can transmit a message to the CPU-22/23 board. Once the CPU-22/23 board receives a message, it initiates a quick response that has already been programmed. For example, servicing the interrupt that results from receiving a message might cause the computer to actuate controls, turn on an alarm, or perform other real-time tasks.

The board includes a 68020 μP chip and a 68882 floating-point math chip, both of which operate at clock rates of either 16.7 or 20 MHz. Its onboard memory includes either 256k bytes or 1M byte of dual-port static RAM and as many as 4M bytes of EPROM. The EPROM requires one wait state. The dual-port RAM allows the VME Bus and DMA devices, as well as the CPU, to share interleaved memory-access operations without degrading the μP's performance. The interleaved operations require no wait states or stop states. The presence of the high-speed dual-port RAM lets processors quickly exchange programs and data in a multiprocessing system. The manufacturer specifies that the CPU board facilitates multiprocessing applications that fall within the 3- to 15-MIPS range. Users will be able to upgrade the μP from a 68020 to a 68030 when the latter chip is available from Motorola.



***The CPU-22/23 board facilitates message passing on the VME Bus** and provides either 256k bytes or 1M byte of dual-port RAM. You can buy the board as well as license the manufacturer's technology.*

The heart of the CPU-22/23 board is the manufacturer's FGA-002 gate array, which controls message-passing operations, as well as DMA transfers and I/O functions. The CMOS gate-array chip also serves as the primary interface between the 68020 μP chip and the VME Bus. However, the board incorporates separate bus-driver/receiver ICs that actually connect the FGA-002 chip to the bus signal lines. The gate array also provides the signals that control an onboard real-time clock, two multiprotocol serial I/O ports, and five timers.

The manufacturer expects to patent its bus-management technology, which it calls VME/Plus. Licenses to use the technology embodied in the FGA-002 chip, however, will be available to manufacturers of competing VME Bus products. The licensing will take place through a consortium established by the VME Bus International Trade Association (VITA).

As part of the CPU-22/23 board, you also receive VMEPROM, a set of four EPROMs that contain a monitor/debugger program and a real-time operating-system kernel. The operating-system kernel provides a subset of PDOS operations as well as a PDOS file manager and BIOS modules. The PROM-based software also includes the manufacturer's Forcebug modules.

Although the CPU board provides a message-passing capability and many other onboard features, it still conforms to the IEEE-1014 VME Bus standard and its sub buses. For example, the CPU-22 board supports the VME memory-extension bus (VMX), and the CPU-23 supports the VME subsystem bus (VSB). The base price for either board, with a 68020 μP that runs at 16.7 MHz, is $6475. Each board also includes 256k bytes of dual-port RAM.—***Jon Titus***

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410.

Circle No 715

Force Computers GmbH, Daimlerstrasse 9, D-8012 Ottobrunn, West Germany. Phone (089) 600-910.

Circle No 716

WHEN YOU HAVE THE FACTS—YOU'LL KNOW THERE IS NO COMPETITION

Introducing the Venable 350—A New Generation Design Tool For Frequency Response Analysis, Synthesis, Modeling and Testing of Power Supply and Servo Control Loops.

The Venable 350. It's a highly flexible, computer-based 0.0001 Hz to 1.0 MHz frequency response analyzer. It allows you to quickly and precisely measure and document the frequency characteristics of any component or system. Competitively priced with other uncompromising analyzers, it truly offers a quantum leap forward in performance and design capability.

The Venable 350 is a new generation tool that—for the first time—fully integrates analysis, synthesis, modeling, and test functions. This means that you can now easily and quickly synthesize a circuit, plot the analysis results, specify design changes, test the frequency response of actual hardware, and then overlay the model with just a few key strokes on the same instrument.

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The 350 maximizes your engineering creativity. And it's a real workhorse in a test environment. But there's so much to the Venable 350 it can't be covered in one page. Why not contact Venable Industries today. After all, if you don't—how do you know your competition won't? **Venable Industries,** 3555 Lomita Blvd., Torrance, CA 90505. Outside CA **(800) 262-2522.** Inside CA **(213) 539-2522.** Fax: (213) 539-4139.

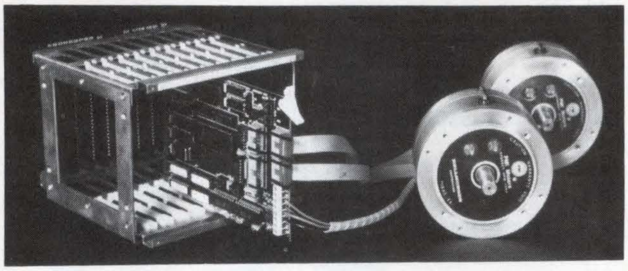
VENABLE INDUSTRIES,INC.

V E N A B L E

CIRCLE NO 48

READERS' CHOICE

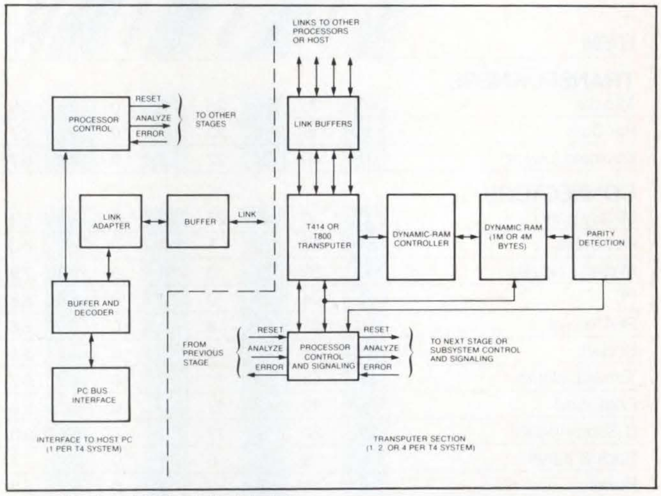
Of all the new products covered in EDN's **August 6, 1987,** issue, the ones reprinted here generated the most reader requests for additional information. If you missed them the first time, find out what makes them special: Just circle the appropriate numbers on the Information Retrieval Service card, or refer to the indicated pages in our **August 6, 1987,** issue.



▲ MOTOR CONTROLLER

The Model 4327 motor controller is STD Bus compatible. It intelligently controls two dc brush-type servo motors and offers four modes of position and velocity control (pg 250).

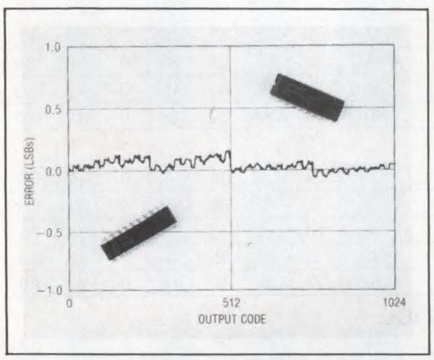
Technology 80 Inc.
Circle No 605



▲ ADD-IN BOARD

The T4 Transputer-based add-in board supports programming in C and allows you to develop parallel-processing applications on an IBM PC or compatible computer (pg 73).

Micropar Inc.
Circle No 601



◀ DATA-ACQUISITION CHIP

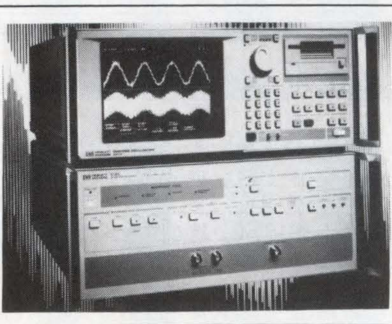
The LTC1090 data-acquisition system contains a 10-bit A/D converter, an S/H circuit with a 1-μsec acquisition time, and an analog input multiplexer, all on a single piece of silicon packaged in a 20-pin DIP (pg 82).

Linear Technology Corp.
Circle No 603

▲ FORMAT CONVERTER

The R900 Universal File Transfer software runs on IBM PCs, PC/XTs, PC/ATs, and compatible computers equipped with the vendor's data-acquisition or digital-oscilloscope interface boards (pg 254).

Rapid Systems Inc.
Circle No 604



◀ DIGITIZING OSCILLOSCOPES

The HP5185T, HP54112D, and HP54120T cater to almost all your high-bandwidth and deep-capture measurement needs (pg 77).

Hewlett-Packard Co.
Circle No 602

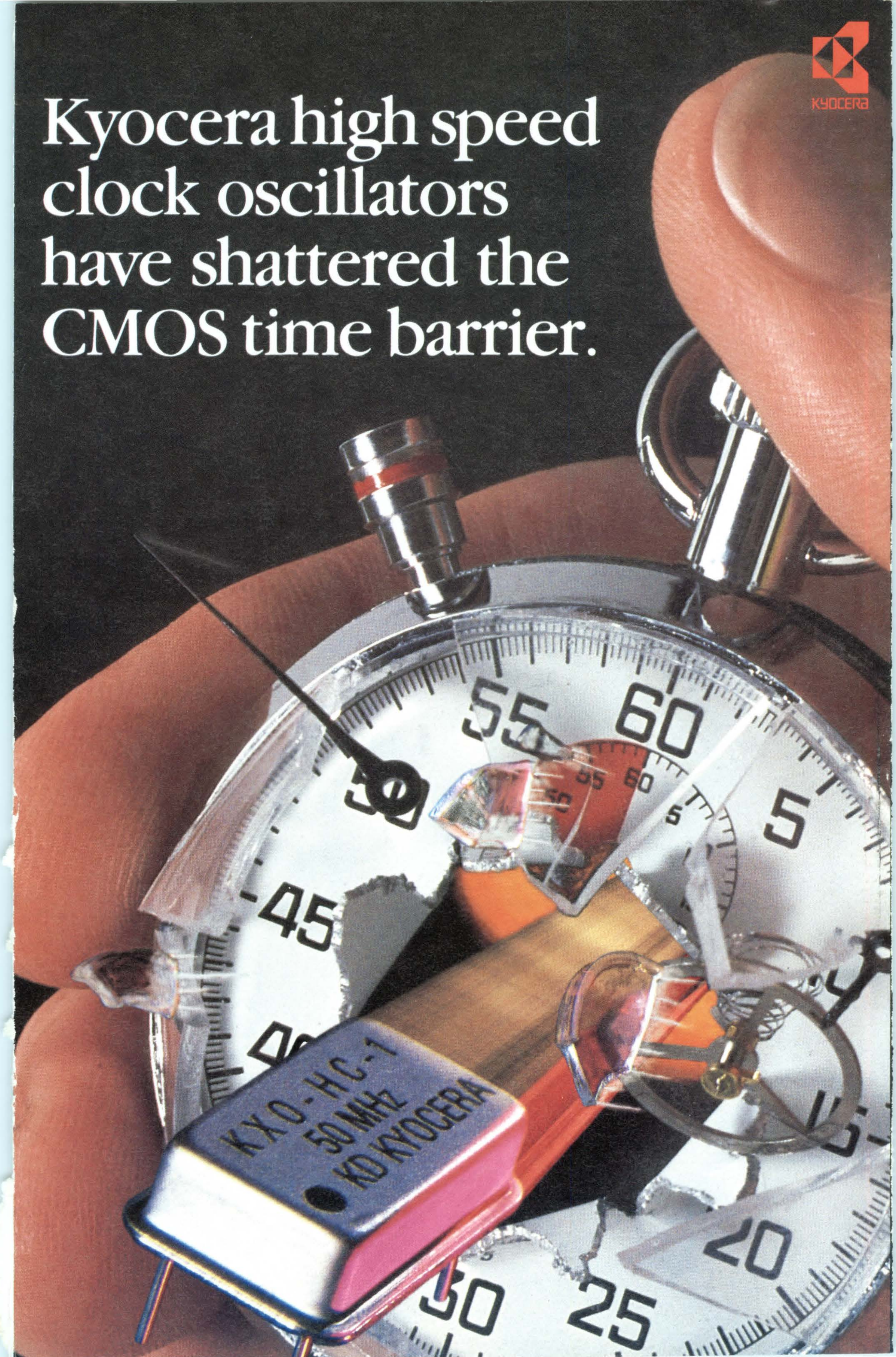
LEADTIME INDEX

Percentage of respondents

ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
TRANSFORMERS								
Toroidal	0	25	50	25	0	0	8.6	5.9
Pot-Core	8	15	46	23	8	0	9.7	7.7
Laminate (power)	0	40	27	27	6	0	9.2	6.7
CONNECTORS								
Military panel	0	0	75	25	0	0	9.9	5.3
Flat/Cable	27	27	40	6	0	0	5.0	4.3
Multi-pin circular	0	29	71	0	0	0	6.6	7.9
PC	0	44	56	0	0	0	5.8	5.6
RF/Coaxial	17	33	42	8	0	0	5.6	6.6
Socket	37	26	32	5	0	0	4.1	5.2
Terminal blocks	19	43	38	0	0	0	4.3	5.7
Edge card	19	19	43	19	0	0	7.0	5.8
D-Subminiature	20	20	47	13	0	0	6.4	6.3
Rack & panel	7	8	69	8	8	0	8.9	7.7
Power	9	46	36	9	0	0	5.7	6.9
PRINTED CIRCUIT BOARDS								
Single-sided	5	54	36	5	0	0	5.3	4.9
Double-sided	3	35	48	14	0	0	7.0	5.2
Multi-layer	0	12	63	25	0	0	9.3	8.1
Prototype	5	70	25	0	0	0	4.1	3.8
RESISTORS								
Carbon film	38	31	28	3	0	0	3.7	3.1
Carbon composition	38	33	29	0	0	0	3.3	3.2
Metal film	36	29	32	5	0	0	4.1	3.5
Metal oxide	18	29	41	12	0	0	6.0	2.8
Wirewound	14	24	48	9	5	0	7.2	6.6
Potentiometers	27	27	46	0	0	0	4.5	6.9
Networks	19	31	31	19	0	0	6.3	5.1
FUSES	35	35	20	10	0	0	4.2	2.6
SWITCHES								
Pushbutton	26	21	32	21	0	0	6.4	5.6
Rotary	15	35	35	15	0	0	6.2	6.7
Rocker	18	29	35	18	0	0	6.4	5.0
Thumbwheel	0	25	42	33	0	0	9.3	6.4
Snap action	15	31	31	23	0	0	7.0	5.5
Momentary	23	15	39	23	0	0	7.1	5.8
Dual in-line	30	20	20	30	0	0	6.9	5.9
WIRE AND CABLE								
Coaxial	33	20	47	0	0	0	4.3	2.8
Flat ribbon	33	22	34	11	0	0	5.1	4.1
Multiconductor	15	23	54	8	0	0	6.2	3.8
Hookup	48	28	24	0	0	0	2.8	1.6
Wire wrap	50	33	17	0	0	0	2.3	5.0
Power cords	36	18	27	14	5	0	6.0	4.4
POWER SUPPLIES								
Switcher	20	33	27	20	0	0	6.2	7.4
Linear	10	40	30	20	0	0	6.7	8.2
CIRCUIT BREAKERS	16	47	21	16	0	0	5.6	7.5
HEAT SINKS	11	56	28	5	0	0	4.8	4.8
RELAYS								
General purpose	32	37	21	10	0	0	4.4	6.1
PC board	10	37	21	32	0	0	7.7	7.4

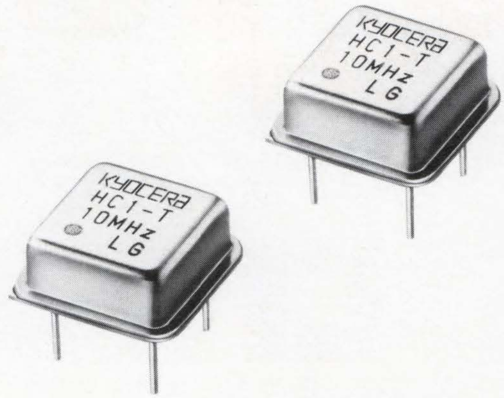
ITEM	Off the shelf	1-5 weeks	6-10 weeks	11-20 weeks	21-30 weeks	Over 30 weeks	Average (weeks)	Last month's average (weeks)
RELAYS								
Dry reed	0	50	17	33	0	0	8.0	7.9
Mercury	17	33	17	33	0	0	7.5	7.6
Solid state	8	50	17	17	8	0	7.5	6.0
DISCRETE SEMICONDUCTORS								
Diode	39	29	21	7	0	4	4.8	8.0
Zener	37	26	21	11	5	0	5.4	7.4
Thyristor	8	25	42	25	0	0	8.0	6.6
Small signal transistor	9	37	27	27	0	0	7.5	5.5
MOSFET	15	23	31	31	0	0	7.9	6.2
Power, bipolar	20	20	20	40	0	0	8.4	5.4
INTEGRATED CIRCUITS, DIGITAL								
Advanced CMOS	8	17	50	25	0	0	8.4	11.7
CMOS	26	21	32	21	0	0	6.4	8.9
TTL	27	27	26	20	0	0	6.0	6.5
LS	44	6	25	25	0	0	6.1	6.6
INTEGRATED CIRCUITS, LINEAR								
Communication/Circuit	11	11	56	22	0	0	8.2	6.3
OP amplifier	14	21	36	29	0	0	7.9	7.9
Voltage regulator	21	26	42	11	0	0	5.8	6.8
MEMORY CIRCUITS								
RAM 16k	20	20	30	30	0	0	7.7	7.9
RAM 64k	23	15	39	23	0	0	7.1	8.3
RAM 256k	37	0	27	27	9	0	8.7	7.8
RAM 1M-bit	17	17	33	17	16	0	10.0	8.8
ROM/PROM	30	0	50	20	0	0	7.1	9.0
EPROM 64k	21	14	36	29	0	0	7.7	9.4
EPROM 256k	17	8	42	33	0	0	8.8	8.8
EPROM 1M-bit	13	12	50	25	0	0	8.3	13.9
EEPROM 16k	10	20	40	30	0	0	8.5	12.3
EEPROM 64k	10	30	30	30	0	0	8.0	13.0
DISPLAYS								
Panel meters	7	29	21	36	7	0	9.9	6.6
Fluorescent	0	0	40	60	0	0	12.5	10.1
Incandescent	14	29	14	43	0	0	8.6	7.6
LED	30	15	20	35	0	0	7.5	6.0
Liquid crystal	0	27	33	40	0	0	9.7	9.9
MICROPROCESSOR ICs								
8-bit	14	33	33	20	0	0	6.8	8.9
16-bit	13	13	47	27	0	0	8.3	8.1
32-bit	0	9	36	46	9	0	12.5	8.5
FUNCTION PACKAGES								
Amplifier	0	22	45	33	0	0	9.4	7.5
Converter, analog to digital	0	20	50	30	0	0	9.3	8.3
Converter, digital to analog	0	25	50	25	0	0	8.6	8.3
LINE FILTERS	20	0	60	20	0	0	7.9	7.9
CAPACITORS								
Ceramic monolithic	28	32	32	8	0	0	4.8	5.9
Ceramic disc	38	19	33	10	0	0	4.7	6.0
Film	38	19	31	12	0	0	5.0	7.3
Aluminum electrolytic	18	41	27	14	0	0	5.5	8.2
Tantalum	35	15	35	15	0	0	5.6	7.3
INDUCTORS	21	22	43	14	0	0	6.3	5.8

Source: *Electronics Purchasing* magazine's survey of buyers


KYOCERA
Kyocera high speed clock oscillators have shattered the CMOS time barrier.
KXO-HC-1
50MHz
KD KYOCERA

KHO-HC SERIES

CRYSTAL CLOCK OSCILLATORS



FEATURES

Condensed into a half-inch size clock oscillator are the popular features and functions of the KXO-HC High Speed C-MOS clock oscillators. The output level is C-MOS compatible with its large noise margin and can also drive 10TTL (IOL=16 mA). So, it has drive capability of almost all devices such as TTL, LS-TTL, S-TTL, C-MOS, HC-MOS, N-MOS, etc. with a frequency range from 500 KHz to 50 MHz. The "E" (Enable) function is derived from a Tri-State output buffer controlled by logic levels on pin 1 (control). Output can be changed from normal oscillation to a high impedance state by the control pin, effectively de-coupling it from the oscillator bus. This function can provide a change of system timing as well as wired "OR" and easy system logic check by an alternate test oscillator.

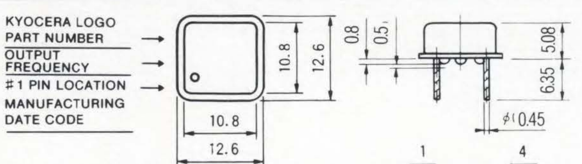
SPECIFICATIONS: KHO-HC/KXO-HC

FREQUENCY RANGE		0.5MHz to 50MHz
OPERATING TEMPERATURE RANGE		0 to 70°C
STORAGE TEMPERATURE RANGE		−55 to 125°C
INPUT VOLTAGE		5V ±10%
INPUT CURRENT		50mA MAX.
FREQUENCY STABILITY Vcc=4.5 to 5.5V Topr=0 to 70°C		±100ppm
AGING		±5 ppm/YEAR
OUTPUT	OUTPUT LEVEL	TTL LEVEL Fanout 10
	DUTY RATIO	40 to 60%
	DUTY RATIO (S)	45 to 55%
	Tr, Tf	5nS max.
INPUT (TRISTATE)	Iih	10μA max.
	Iil	−150μA max.
	Vih	2.2Vmin.
	Vil	0.8Vmax.

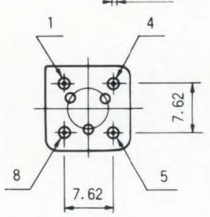
TRISTATE FUNCTION CHART

#1 PIN	#8 PIN
H OR OPEN	OSCILLATION
L	HIGH IMPEDANCE

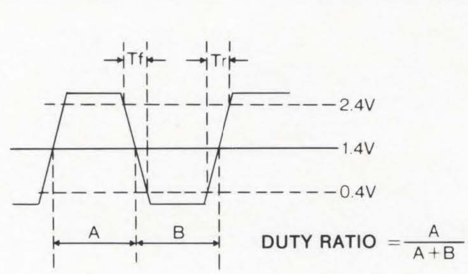
DIMENSIONS



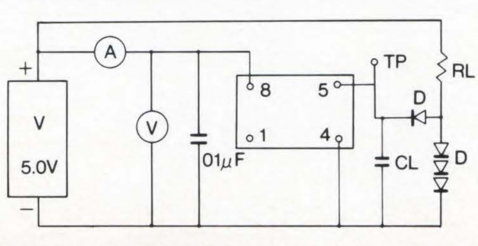
PIN CONN.	
1	NC
4	GND
5	OUTPUT
8	Vdd



OUTPUT WAVEFORM (TTL LOAD)

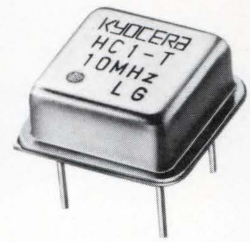


TEST CIRCUIT (TTL LOAD)



RL = 400Ω
D : Switching Diode
Trr ≦ 4nSec
CL = 15pF max.
Including Test Fixture and Probe Capacitance

KYOCERA DATA CLOCKS



A BROAD LINE OF CLOCKS FROM TTL TO HCMOS

Kyocera manufactures a complete line of clock oscillators to accommodate all your timing applications. No matter if the application requires driving high speed CMOS logic or fitting the low power needs of battery-operated equipment, Kyocera has the clock oscillator you need. Kyocera builds its high quality clock oscillators from the substrate up. They feature an all-metal welded package that has been hermetically sealed to protect them from humidity. And the number 7 pin is grounded to the case to help minimize RF radiation and meet FCC EMI specifications. These and other features combined with Kyocera's 25 years experience of manufacturing electronic ceramics, give you a quality clock oscillator you can rely on.

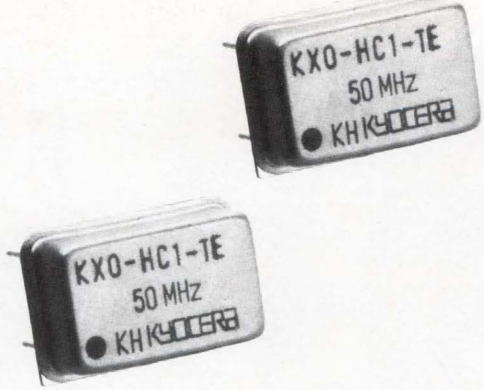
OSCILLATOR PRODUCTS

KXO SERIES, BASIC DATA
KXO-01 TTL COMPATIBLE CLOCK
KXO-CL CMOS COMPATIBLE CLOCK
KXO-CS 1-TTL OR CMOS, HCMOS COMPATIBLE CLOCK
KXO-HC 10-TTL OR CMOS, HCMOS COMPATIBLE CLOCK
LQV MULTI-OUTPUT CMOS COMPATIBLE CLOCK
KTXO, KTVXO TEMP. COMPENSATED AND VCO
QUARTZ, TUNING FORK LOW FREQUENCY

KYOCERA DATA CLOCK OSCILLATOR SELECTION CHART

MODEL	FREQUENCY RANGE (MHz)	FAN OUT	DRIVE LEVEL	DUTY RATIO	FEATURES
KXO-01	4.0–50.0	10 TTL IOH 0.4mA IOL 16mA	TTL VOH 2.4V VOL 0.4V	40/60	• TTL COMPATIBLE • TRANSISTOR CIRCUIT • EXCELLENT COST/PERFORMANCE
KXO-CL	50Hz–8.0 MHz	1 LSTTL IOH 0.08mA IOL 0.51mA	CMOS VOH 4.6V VOL 0.4V	40/60 50 Hz–4.0 MHz 45/55 (AVAILABLE)	• CMOS COMPATIBLE • LOW POWER CONSUMPTION • EXTREMELY LOW FREQUENCY OUTPUT AVAILABLE
KXO-CS	0.25–24.0	1 TTL IOH 0.1mA IOL.1.6mA	CMOS VOH 0.9 Vdd VOL 0.1 Vdd	40/60 0.25–12.0 MHz 45/55 (AVAILABLE)	• HCMOS COMPATIBLE • LOW POWER CONSUMPTION • STAND-BY FUNCTION • CMOS, TTL COMPATIBLE
KXO-HC	0.5–50.0	10 TTL IOH 1mA IOL 16mA	CMOS VOH Vdd-0.2V VOL. 0.4V	40/60 0.5–25.0 MHz 44/55 (AVAILABLE)	• HCMOS COMPATIBLE • HIGH SPEED, HIGH DRIVE CAPABILITY • TRI-STATE ENABLE/DISABLE FUNCTION • CMOS, TTL COMPATIBLE
LQV	12.0 Hz–8.0 MHz	1-CMOS		45/55 BELOW 4MHz	• MULTI-OUTPUT, BINARY RELATED FREQUENCIES • 4 OUTPUTS MAX. (3 WITH INHIBIT)
KTXO	4.0–50.0		1V P-P LOAD 1K/5PF	SINE OR SQUARE WAVE	• TCXO • 1PPM AGING • LOW POWER
KTVXO	10.0–20.0		1.5V P-P LOAD 1K		• VOLTAGE TRIMMABLE TCXO • 10PPM/VOLT SENSITIVITY

KXO-HC SERIES



500 KHZ-50.0 MHZ/10 TTL, CMOS, HCMOS, NMOS; TRI-STATE ENABLE OPTION

Kyocera announces a revolutionary breakthrough in clock oscillators for CMOS-based computers, peripherals and telecommunications applications. Now our clock oscillator family offers the dual advantages of the highest CMOS clock speeds and driving capability on the market and low power consumption as well.

World's fastest clocks for CMOS and TTL logic.

To meet the needs of today's and tomorrow's high speed gate arrays, Kyocera's KX0-HC clock oscillator spans a frequency range of 500 kHz to 50 MHz and can drive up to 100 pF loads, up to 10 TTL gates. Yet it consumes only 16mA at 24 MHz. This low power reduces heat in the circuit, which increases reliability. And, reduces power supply costs in the process.

Tri-state for easy circuit testing.

In addition, our KXO-HC model offers our tri-state capability which allows it to disable during testing and decouple from the oscillator bus when a control signal is applied. This lets circuit designers test the entire circuit board with an external synchronizing signal. Plus, it allows the circuit to be tested utilizing less expensive, lower power test equipment.

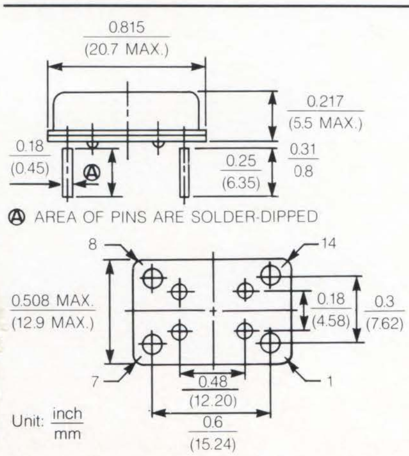
Pin 7 case ground for improved shielding.

The Kyocera KXO family of clock oscillators are hermetically sealed to protect them from humidity. And, are designed with the number 7 pin grounded to the case and an all-metal package which helps minimize RF radiation and meets FCC EMI specifications. If you need high speed, high driving capability with low power consumption, design Kyocera's advanced clock oscillators into your circuit design.

KYOCERA

Quality across the board.

DIMENSIONS



HOW TO ORDER

KHO-HC
KXO-HC [ ] [ ] [ ] [ ] [50.000 MHz]

KYOCERA KXO-HC CLOCK OSCILLATOR SERIES

FPEQUENCY STABILITY
S: ±25PPM
O: ±50PPM
1: ±100PPM
2: ±500PPM
3: ±0.1%
4: ±1.0%

MEASURING METHOD*
C: C-MOS LEVEL
T: TTL LEVEL

SYMMETRY
S: 55/45
NIL: 60/40

ENABLE/DISABLE FUNCTION
E: WITH FUNCTION
NIL: #1 PIN OPEN

OUTPUT FREQUENCY
NOTE: FREQUENCIES SHALL BE DESCRIBED WITH A MINIMUM OF THREE DECIMAL PLACES.

*NOTE: EITHER C-MOS OR TTL SHALL BE SELECTED BASED ON SPECIFICATIONS OF SYMMETRY AND RISE & FALL TIME.

PIN CONNECTION

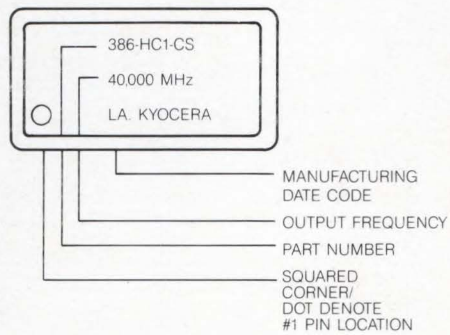
#1	N/C OR CONTROL
#7	GND
#8	OUTPUT
#14	+5Vcc

KYOCERA

SPECIFICATIONS

FREQUENCY RANGE		0.5MHz to 40MHz
OPERATING TEMPERATURE RANGE		0 to 70°C
STORAGE TEMPERATURE RANGE		−55 to 125°C
INPUT VOLTAGE		5V ± 5%
INPUT CURRENT		65mA max.
FREQUENCY STABILITY Vcc = 4.75 to 5.25V Topr = 0 to 70°C		±100ppm
AGING		±5ppm/YEAR
OUTPUT	LOAD	C-MOS (150PF LOAD)
	DUTY RATIO (S)	45 to 55% (Vcc/2)
	Tr, Tf	SEE CLOCK TIME
	V_{OH}	Vcc - 0.4V min.
	V_{OL}	0.4V max.
INPUT (TRISTATE)	I_{IH}	10μA max.
	I_{IL}	−150μA max.
	V_{IH}	2.2V min.
	V_{IL}	0.8V max.

386 MARKING



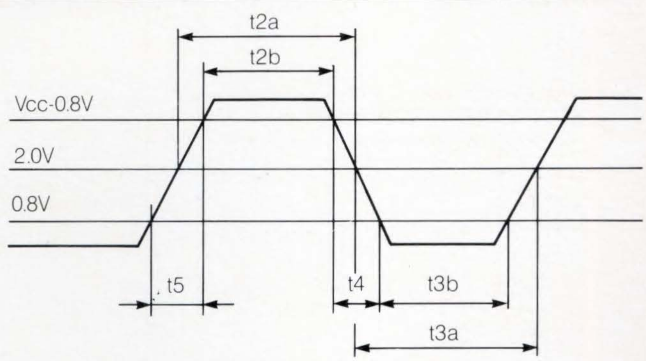
TRISTATE FUNCTION CHART (OPTION)

#1 PIN	#8 PIN
H or OPEN	OSCILLATION
L	HIGH IMPEDANCE

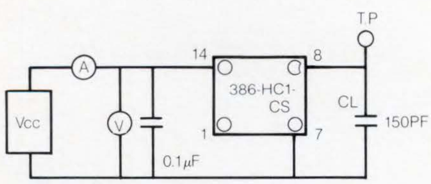
CLOCK TIME

FREQUENCY		32MHz		40 MHz	
CLOCK TIME (nS)		Min.	Max.	Min.	Max.
CLK HIGH TIME	t2a	9	—	8	—
CLK HIGH TIME	t2b	5	—	5	—
CLK LOW TIME	t3a	9	—	8	—
CLK LOW TIME	t3b	7	—	6	—
CLK FALL TIME	t4	—	7.5	—	8
CLK RISE TIME	t5	—	7.5	—	8

OUTPUT WAVEFORM



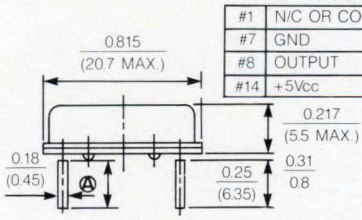
TEST CIRCUIT (CMOS LOAD)

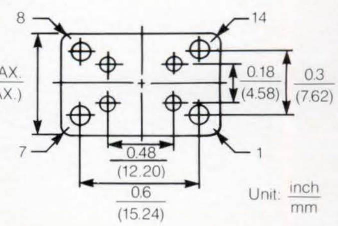


DIMENSIONS

PIN CONNECTION

#1	N/C OR CONTROL
#7	GND
#8	OUTPUT
#14	+5Vcc





Ⓐ AREA OF PINS ARE SOLDER-DIPPED

Unit: inch / mm

HOW TO ORDER

386-HC1-CS [ ] [32.000 MHz | 40.000 MHz]

ENABLE/DISABLE FUNCTION
E: WITH FUNCTION
NIL: #1 PIN OPEN

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386-HC1-CS SERIES

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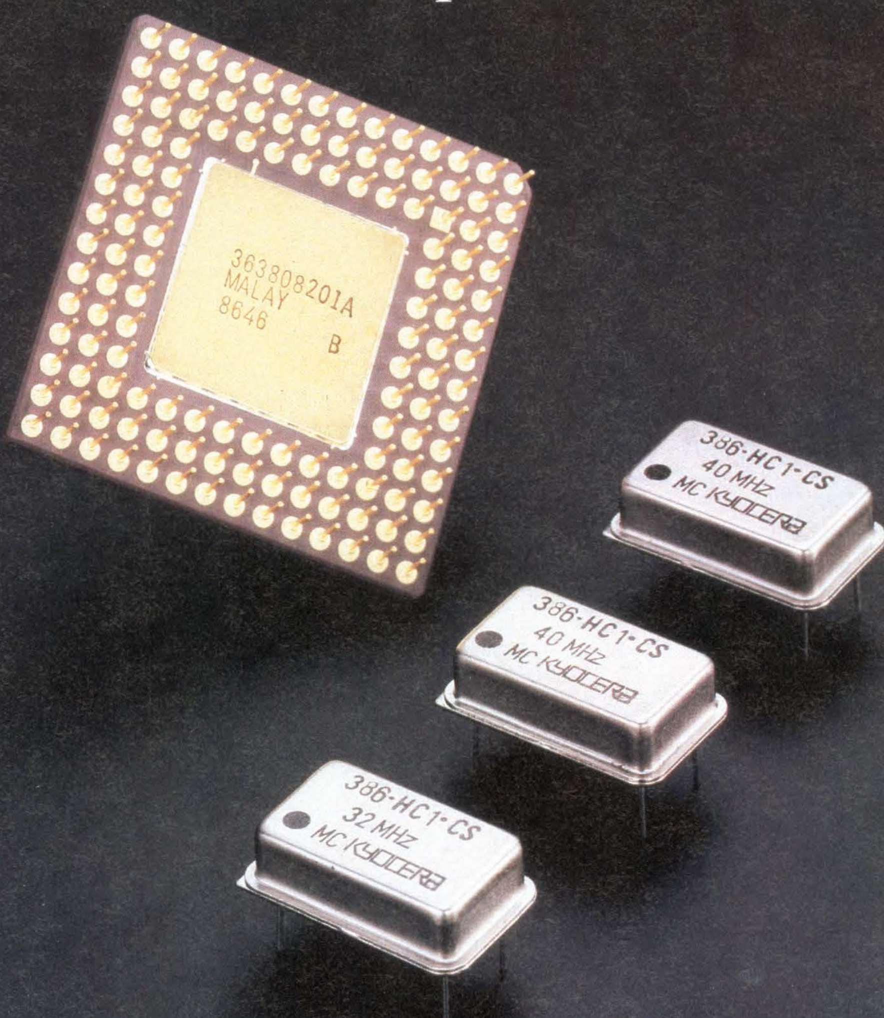

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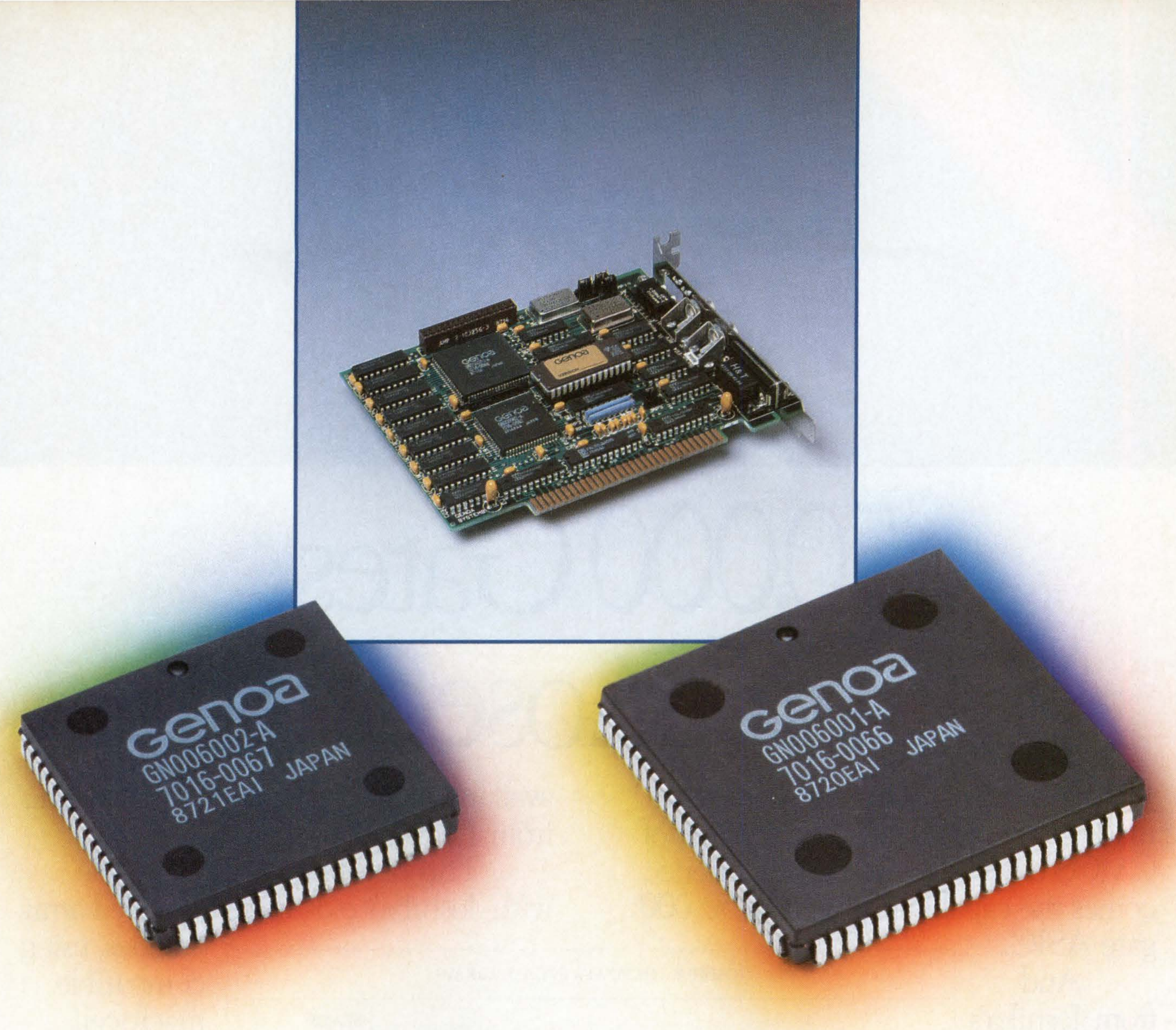

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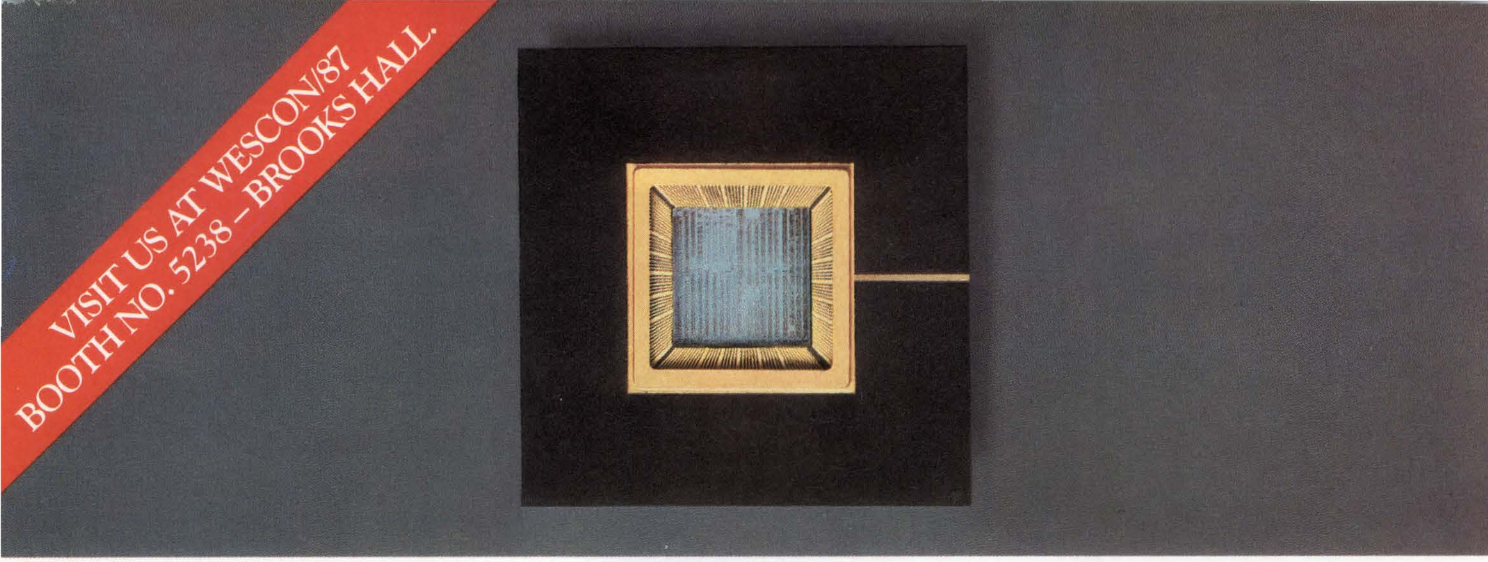

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DESIGN RULE	3μm	2μm	1.5μm	1.5μm
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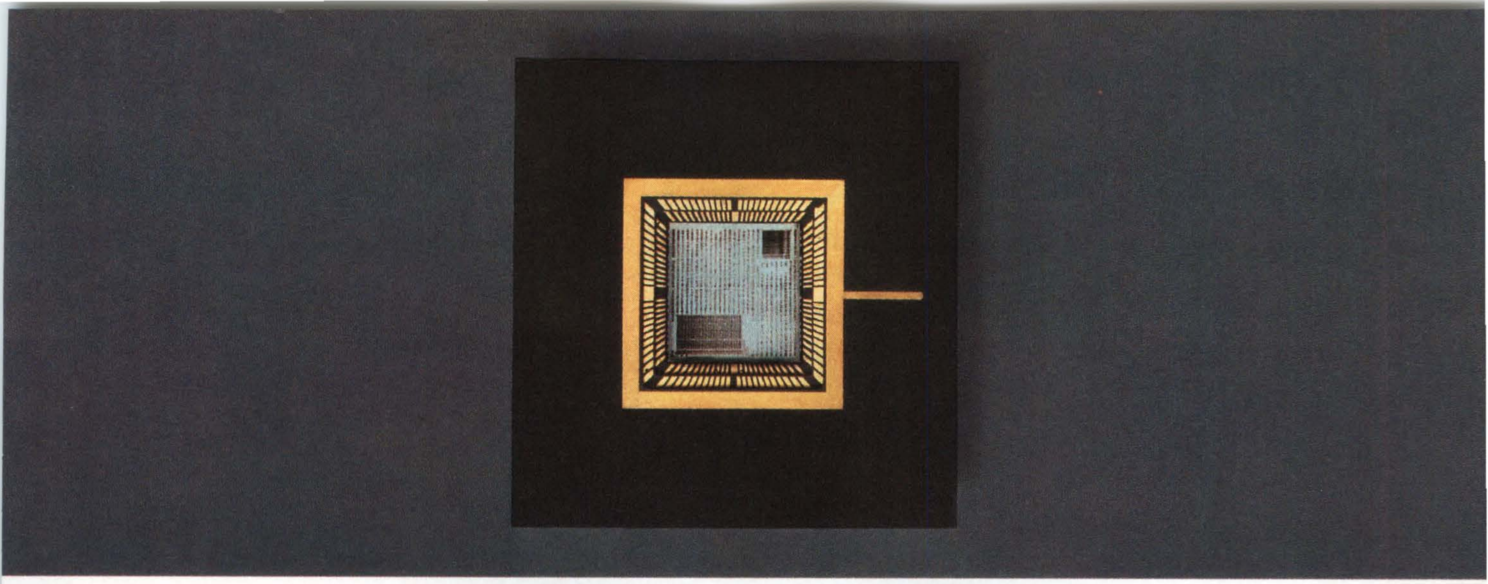

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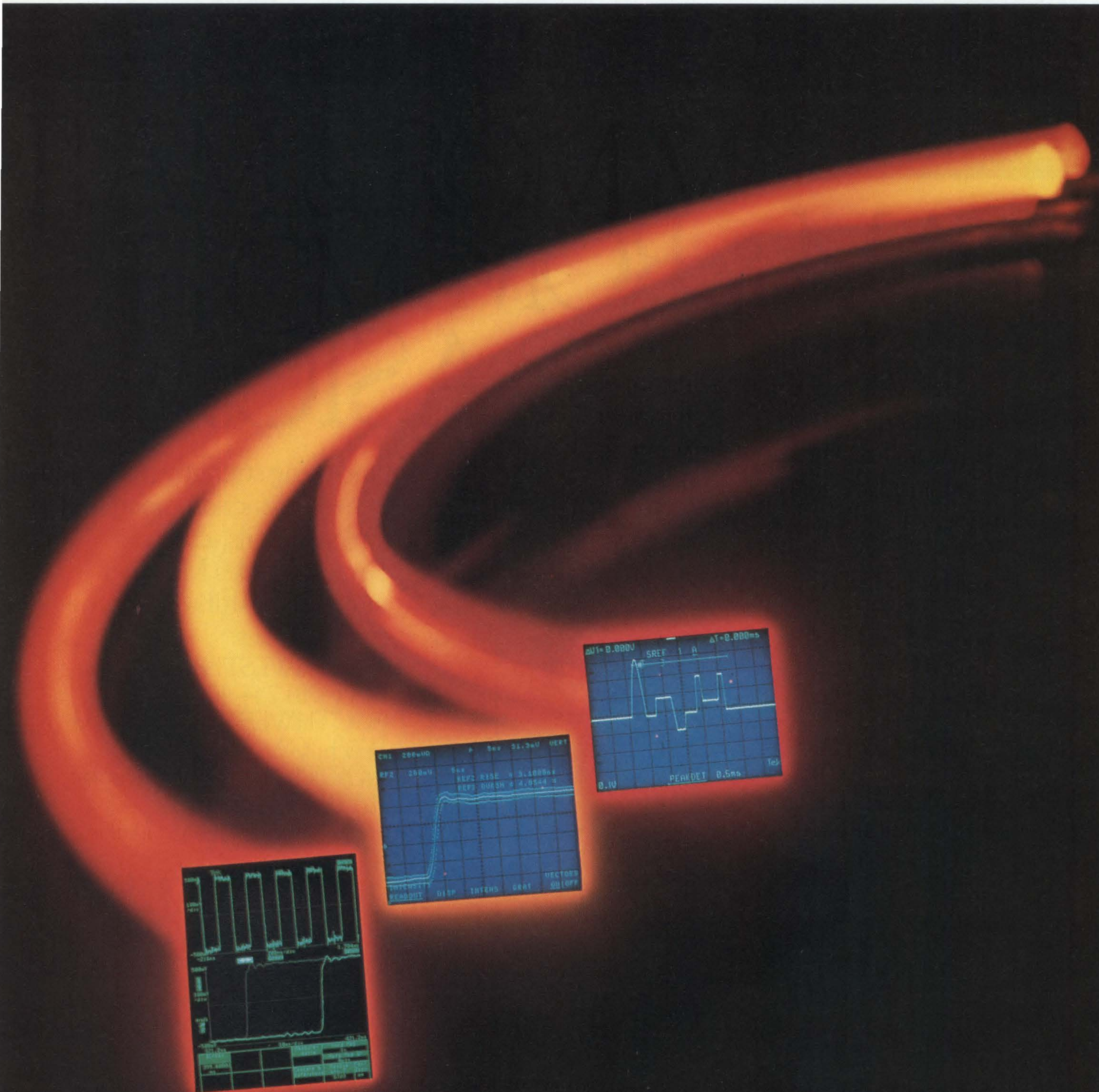
CIRCLE NO 47

Special Report

Digital storage



Offering a spectrum of measurement features, *such as manual or automatic cursor measurements, linear and curve interpolators, pretriggering and post-triggering, and equivalent time sampling, the latest digital storage oscilloscopes provide bandwidths to 1 GHz and digitizing rates as high as 1G samples/sec. (Photo courtesy Tektronix Inc)*

oscilloscopes

Whether you use them for single-shot storage, taking measurements, or troubleshooting, the latest digital storage oscilloscopes provide a number of measurement features that can help you work faster and more accurately. The available DSOs now include models with 1-GHz bandwidths and digitizing rates to 1G samples/sec.

Doug Conner, *Regional Editor*

Until a few years ago, digital storage oscilloscopes (DSOs) were just niche-market instruments: They didn't have high enough sample rates and bandwidths for general electronic engineering work, such as characterizing and troubleshooting circuits. Their bandwidths were lower than 100 MHz, and their sample rates were below 50M samples/sec. Now, however, you can find DSOs that offer bandwidths to 1 GHz and digitizing rates as high as 1G samples/sec. And you can choose from a wide variety of scopes: Virtually every analog scope manufacturer now sells a DSO as well.

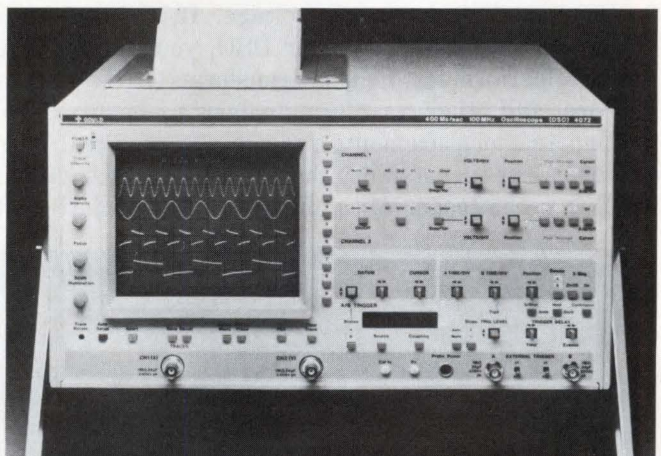
Digital storage oscilloscopes still can't compete with analog scopes on a bandwidth-for-dollars basis, however; analog scopes still give you more bandwidth for the money. Where digital scopes do compete is in engineering productivity. Their extensive measurement features help you get your work done more quickly and more accurately than you could with an analog scope. In addition, many DSOs can be connected to a computer for automated control and data analysis.

Many of the currently available DSOs were introduced in the past year. You'll find a wide selection of DSOs in the 50- to 100-MHz bandwidth range; as recently as two years ago, only one manufacturer offered DSOs in this range. Even if you're looking for bandwidths above 100 MHz, you can choose from several scopes from different manufacturers. And there's more good news: Competition between manufacturers at all levels is bringing DSO prices down while increasing the number of extra measurement features on the scopes.

Digital-storage-oscilloscope basics

When you use a digital storage oscilloscope instead of an analog scope, you have to take into account some of the differences between the two instruments. In DSOs, as in analog scopes, bandwidth is defined as the frequency at which a signal is attenuated by 3 dB. The bandwidth is limited by the front end of the scope, from the probes through the amplifier stage and into the input of the A/D converter. No matter how fast the instrument samples and converts the input signal, its analog bandwidth limit remains the same.

When you look at an analog signal with a DSO in single-shot storage mode, you get a series of data points. These points are separated in time by the digitizer's sample rate. A 50M-sample/sec digitizer will give you a data point every 20 nsec. Between these samples you have no idea what the waveform is doing.



Two channels at 400M samples/sec *allow Gould's 4072 to capture 100-MHz waveforms in real time and then plot them on an optional internal plotter.*

According to the Nyquist criterion, you need to sample at a frequency that is at least twice the frequency of the highest frequency signal component that interests you. This limit gives an inadequate representation of the signal for most scope work, however; a sampling limit of about 10 times the frequency of interest is a better rule of thumb (for instance, you'd sample a 10-MHz waveform at 100M samples/sec.)

On some DSOs you'll find curve interpolators that allow you to look at a reasonably good representation of

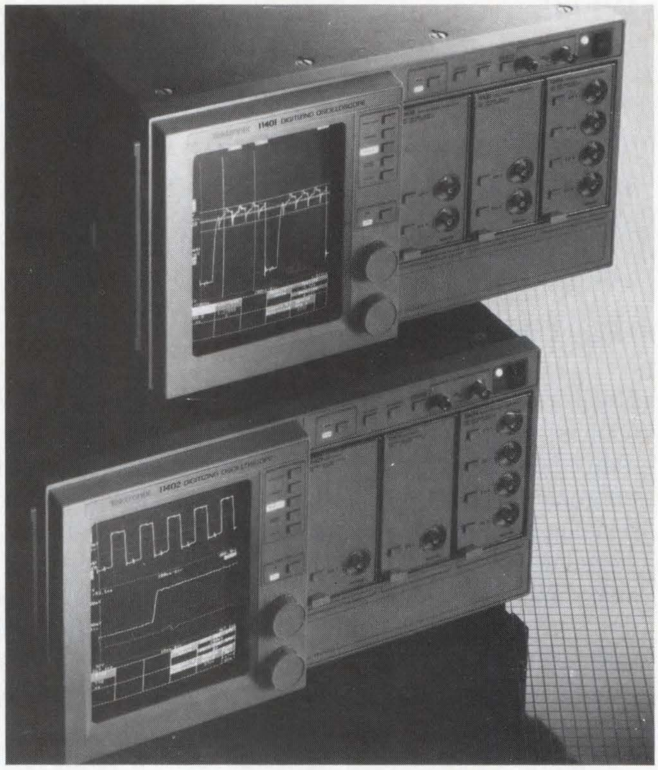
Analog scopes still give you more bandwidth for the money, but digital scopes help you get your work done more quickly and more accurately.

a waveform while sampling at four times the signal frequency. Remember, however, that the real information is still only in the data points. If you want to use a DSO to capture single-shot events at high signal frequencies, you must use a scope with a high sample rate. For extremely high single-shot bandwidths, it's best to choose a digital scan converter or an analog storage scope instead of a DSO.

You'll also want to know the record length, which is the number of data points that an oscilloscope can store for a waveform. A large record length lets you store long waveforms. Some DSOs allow you to magnify the record for examination after the waveform has been stored.

Automated measurements provide accuracy

Digital scopes can take a considerable variety of measurements. Some provide manual cursor-based measurements of voltage and time; others provide manual or automatic cursor-based measurements that can include rise/fall time, overshoot, undershoot, frequency, and peak-to-peak voltage. If you're using a computer interface with your DSO, you can use software to perform fast Fourier transforms (FFTs), convolutions, and other waveform-analysis procedures. The automated measurements provide accuracy and user-independent repeatability that is hard to match with an analog oscilloscope. Most digital scopes achieve high accuracy in timing because they use a crystal timebase instead of the ramp timing generator that analog scopes use.



The 1-GHz bandwidth *of Tektronix's 11402 and the 500-MHz bandwidth of the company's 11401 combine with the scopes' 10-bit vertical resolution and 10-psec horizontal resolution to give you precision measurement capability.*

A disk-drive plug-in *for Nicolet's 4094 allows you to store many waveforms and run extensive analysis programs on them.*

Many DSOs come with an equivalent-time-sampling feature, which is useful for examining waveforms that an analog scope could trigger on repetitively. Equivalent time sampling allows the scope, over a series of sweeps, to build an accurate representation of the waveform in memory. Usually, equivalent time sampling is limited only by the analog bandwidth of the scope. Because the digital scope displays from memory, the display remains bright even for low-repetition-rate triggers. It's a big advantage to have equivalent time sampling for repetitive waveforms, especially ones at high frequencies. The feature is not useful for single-shot waveforms.

Vertical resolution and signal averaging

Digital scopes' vertical resolution typically extends from 6 bits for higher sampling rates to 16 bits for some low-sample-rate applications. Eight bits is a typical value for DSOs' vertical resolution. If you're trying to

Packing a surprising amount of capability *into a 25-oz, handheld DSO, Dolch's SC01 gives you two 5-MHz channels that sample at 20M samples/sec simultaneously and provide cursors and readout.*

see small voltage differences, especially in combination with large offset voltages, you may need 10- or 12-bit resolution.

You can get the equivalent of higher resolution in some cases by using signal averaging, a feature available on many DSOs. If you're examining a repetitive waveform with a lot of noise or if you need to get vertical resolution greater than the bit resolution of the A/D converter, you'll find signal averaging very useful.

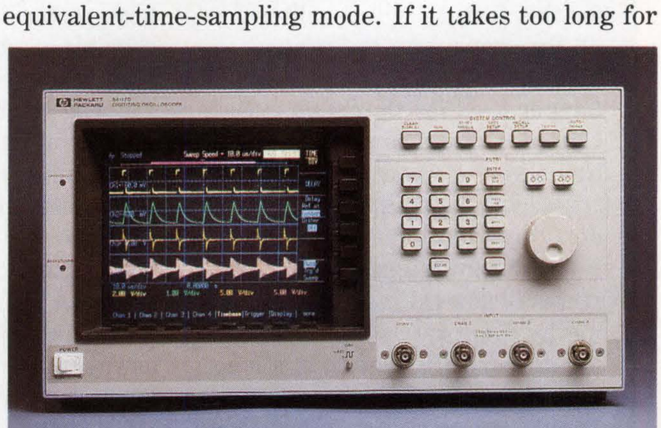
To find low-amplitude oscillations (as you must in troubleshooting), however, you'll need fairly high resolution before you can perform averaging: If the waveform you're looking at has a higher-frequency signal riding on top of it that is not in sync with your trigger, signal averaging will hide that signal. Even with an averaging feature, you'll have a difficult time identifying noise that falls below the basic digitizing noise of the system. In fact, when you first look at a signal, it's a good idea to leave the averaging function off, so that you don't miss any noise in the circuit you're examining.

DSOs can also provide some very useful trigger features. One trigger feature that isn't available on an analog scope is pretriggering, which allows you to start recording a waveform before the scope triggers on an event. By using pretriggering, you can follow a waveform back in time without having to look for another trigger source. Most digital scopes also provide post-triggering, which lets you look forward in time at a waveform in much the same way that you'd use delayed sweep, or a second timebase, on an analog scope. As long as it has sufficient time range, post-triggering can perform the same function as delayed sweep. In fact, post-triggering has replaced delayed sweep on many digital scopes. Some DSOs, however, still feature a second timebase, whether or not they have post-triggering.

Finally, one of the best features of a digital scope is that it spares you from having to take scope pictures: Virtually every DSO can connect to a computer, printer, or plotter.

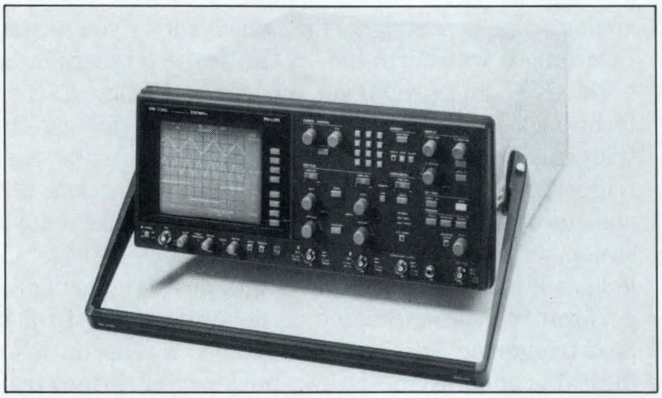
Examine the rearm dead time

One drawback of digital scopes that seldom appears in their specifications is the rearm dead time, which is the time it takes a scope to prepare for another trigger. The bottleneck here is that the data from the last sweep must be processed and placed in display memory before the scope is ready to trigger again. In some scopes, the processor is so busy with these tasks that it updates the display slowly, especially when performing operations, such as averaging, that require more computations. Faster digital processors tend to decrease the rearm dead time, but you still might want to examine it. To do so, you simply connect a function generator to the input at 30 kHz and vary the amplitude while the DSO is in an equivalent-time-sampling mode. If it takes too long for



Four channels operating at 400M samples/sec simultaneously *and a 64k-word memory on every channel allow Hewlett-Packard's 54112D to capture long, high-speed waveforms in real time.*

If you want to use a DSO to capture single-shot events at high signal frequencies, you must use a scope with a high sample rate.



Offering 3-nsec glitch capture and 10-bit resolution, Philips's 200-MHz PM 3320 also provides an autosetup feature.

the display to reflect the waveform change, you know that the rearm dead time is long.

Another problem is visual aliasing, which occurs when the number of points in a single-shot waveform is sufficient to define a waveform, but your eye has difficulty in perceiving the waveform. You can often solve this problem by using one of the various interpolation methods available on some scopes or by reducing the vertical amplitude.

100-MHz DSOs offer basic features

As you can see from **Table 1** on pg 96, manufacturers are incorporating a lot of different features in their scopes. You can find a few basic features on all 100-MHz

Digital-storage-oscilloscope features

Manufacturers are currently packing a lot of special features into digital storage oscilloscopes. This list covers some DSO features you may not be familiar with.

Analog capability—Some DSOs can function as analog scopes, totally bypassing the digital section. If you're not used to digital scopes, or if you want to compare a signal on both types of scope, you might like this feature.

Autosetup—Pressing the button for this feature will usually set up the scope with the proper vertical deflection, timebase, and trigger level for the input.

Complex triggering—This function covers a variety of different triggering capabilities. Some delay by events rather than by time. Others trigger from logic states of several inputs. Delaying by events is useful for looking at a specific section of a long pulse train.

Digitizing rate—All DSOs have at least one A/D converter. Some have one for each channel, allowing you to get the full sampling rate when using all channels. If the scope only has one A/D converter, the instrument's maximum digitizing rate will be divided by the number of channels you're using.

Envelope display—Scopes with this feature process the data taken every sweep and save a cumulative minimum and maximum voltage for every displayed time interval. You can use this feature to find out how a waveform responds to environmental changes, such as changes in temperature and voltage. You can also use this feature to look at the combined noise of the digital oscilloscope and the circuit you're examining. To obtain a measure of just the scope noise, you connect the scope input to ground.

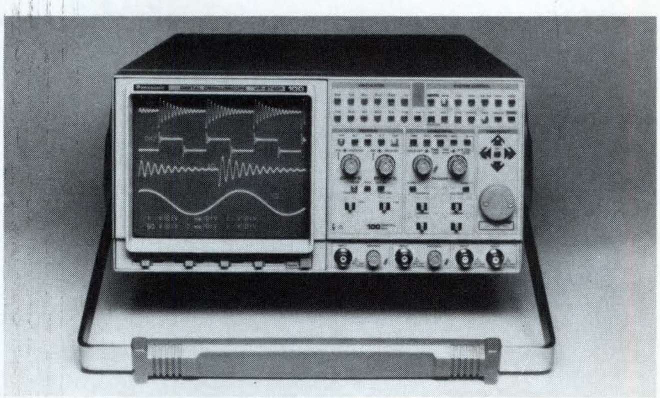
Envelope test limits—These limits can be loaded manually or through a computer interface; they let the scope automatically determine whether a waveform falls outside a prescribed time or voltage profile. If it does, the scope can save the waveform or perform some other prescribed action. Scope manufacturers often refer to this or a similar capability as go/no-go testing, save-on-delta, or babysit mode. This capability is useful in hunting for glitches and in performing automated or semiautomated testing.

External clock—This feature allows you to use an external clock to sample the input. It's useful when you want to run more slowly than the slowest timebase or when you want control of the timing interval.

Glitch/peak detect—This feature can provide data between stored sample points. The glitch/peak detect can take two forms: It can take the form of an analog peak detect that actually detects pulses of a certain width (to a specified minimum) between sample points, or it can be an A/D conversion that runs at full speed even on low-repetition-

DSOs, however. For example, they all offer pretriggering, post-triggering or delayed sweep, waveform memory, and voltage- and time-measurement capability. In addition, all 100-MHz DSOs offer either IEEE-488 or RS-232C interfaces (or both), although Tektronix's 2230 and Iwatsu's 6121/6121A offer the capability as an option.

For applications demanding single-shot storage of signals to 100 MHz, consider Hewlett-Packard's 54112D or Gould's 4074. Both these DSOs sample four inputs simultaneously at 400M samples/sec. The 4074 provides 8-bit vertical resolution with 1k-sample record lengths. It also has 5-nsec glitch capture at any timebase setting. Time and voltage cursors with display readouts



Internal program memory *for building automatic test routines is available on Panasonic's VP-5740P.*

rate signals where the actual stored sample rate is much lower than the maximum sample rate. (Some A/D converters slow the sample rate on low-repetition-rate signals.) In either case, this feature catches and displays any pulse of longer duration than the specified minimum.

Infinite persistence—This feature can be used in much the same way that you use the envelope mode to display cumulative data. Any point, once displayed, will remain on the display until you clear the screen. If you're looking at a repetitive signal, you can use the infinite-persistence feature to catch glitches.

Interfacing—Interfaces to computers, controllers, and plotters normally take one of three forms: IEEE-488 interfaces, RS-232C interfaces, and XY plotter data. In many DSOs, these interfaces not only allow you to use a computer to read the screen data, but also allow your computer to control the front-panel setup and write data to the scope.

Interpolators—Interpolators connect data points on the screen when the scope is operating in single-shot storage mode. Two different types of interpolators are available, both of which can solve the visual-aliasing problem (the difficulty of trying to see a continuous curve when you're only looking at the points). Linear interpolators merely join the points with straight lines, which is a satisfactory procedure as long as enough points are available. Curve interpolators, which come in a variety of different forms, attempt to connect the points with a curve that takes into account the bandwidth limitations of the scope. Curve interpolators can make some very nice-looking waveforms out of very sparse data. Remember, however, that it's only the data points that constitute the real data, so you must use interpolators with caution.

Roll mode—This mode displays data much as a strip-chart recorder does. The waveform display scrolls from right to left; the latest samples appear on the right. You can stop and save the data at any time. You can use the roll mode only at low sweep rates.

Setup memory—The setup memory allows you to store front-panel setups and call them up later. This feature can save you time if you frequently switch between two or more different setups.

Signal averaging—This feature takes data from sequential events and averages them to help filter out noise.

Waveform memory—This feature allows you to store a waveform from the screen and call it up later.

XY mode—The XY mode on a DSO is similar to the XY mode on an analog oscilloscope, except that a DSO's XY mode usually also gives you two full-bandwidth channels without delay lines or horizontal-sweep bandwidth limitations.

TABLE 1—DIGITAL STORAGE OSCILLOSCOPES

MANUFACTURER	MODEL	BANDWIDTH (MHz)	DIGITIZING RATE (M SAMPLES/SEC)	NUMBER OF ADCs	VERTICAL RESOLUTION (BITS)	RECORD LENGTH (WORDS)	INPUT CHANNELS + EXTERNAL TRIGGER	EQUIVALENT TIME SAMPLING	ANALOG OPERATION	GLITCH/PEAK DETECT (NSEC)	AVERAGE MODE	EXTERNAL CLOCK	ENVELOPE DISPLAY	INFINITE PERSISTENCE	ROLL MODE	XY MODE	LINEAR INTERPOLATION	CURVE INTERPOLATION	WAVEFORM MEMORY	SETUP MEMORY	AUTOSETUP	PRETRIGGERING	POST-TRIGGERING	COMPLEX TRIGGERING	DUAL TIMEBASE	IEEE-488 INTERFACE	RS-232C INTERFACE	ENVELOPE TESTING
ANALOGIC	6100-620-1	20	100	1	8	32k	2+1				●	●	●		●		●	●	●	●		●	●			O	O	
BBC-METRAWATT/GOERZ	SE571	15	25	2	8	1k	2+1				●	●			●		●	●	●	●	●	●	●	●		●		
B&K PRECISION	2520	20	2	1	8	1k	2+1	●	●						●	●	●					●						
	2521	20	2	1	8	1k	2+1	●	●		O				●	●	●		O			●					●	
DOLCH	SC01	5	20	2	7	256	2+1	●							●	●			●	●	●	●	●		●			
GOULD	1421	20	2	1	8	1k	2+1	●	●						●	●	●					●						
	1425	20	2	1	8	1k	2+1	●	●		O				●	●	●		O			●					●	
	1604	20	20	2	8	10k	4+1		●	50	O				●	●	●		●	●	●	●	●	●		O	O	
	4030	20	20	2	8	1k	2+1		●						●	●	●		●			●						
	4035	20	20	2	8	1k	2+1		●		O	●			●	●	●					●				●		
	4050	35	100	2	8	1k	2+1		●		O	●			●	●	●		●			●				●		●
	4072	100	400	2	8	1k	2+1	●		5	●				●	●	●	●	●	●	●	●	●	●	●	●	●	●
	4074	100	400	4	8	1k	4+1	●		5	●				●	●	●	●	●	●	●	●	●	●	●	●	●	●
HAMEG	HM205-2	20	5	2	8	1k	2+1		●							●	●									O		
	HM208	20	20	1	8	1k	2+1		●						●	●	●		●			●				O		
HEWLETT-PACKARD	54200D	50	200	2	6	1k	2+1				●	●	●	●			●		●	●	●	●	●	●		●		
	54201D	300	200	2	6	1k	2+1	●			●	●	●	●			●		●	●	●	●	●	●		●		
	54100A	1000	40	2	7	1k	2+1	●			●			●		●			●	●	●	●	●	●		●		
	54100D	1000	40	2	7	1k	2+2	●			●			●		●			●	●	●	●	●	●		●		
	54110D	1000	40	2	7	1k	2+2	●			●			●		●			●	●	●	●	●	●		●		
	54111D	500	1000	4	6-8	8k	2+2	●			●			●				●	●	●	●	●	●	●		●		
	54112D	100	400	4	6	64k	4+1	●			●			●				●	●	●	●	●	●	●		●		
HITACHI	VC-6020	20	1	2	8	1k	2+1	●	●		●				●	●						●				●		
	VC-6041	40	40	1	8	4k	2+1	●	●		●				●	●			●			●				●		
	VC-6050	60	40	1	8	4k	2+1	●	●		●				●	●			●			●	●			●		
	VC-6165	100	100	2	8	4k	2+1	●	●		●		●		●	●			●			●	●		●	●		
IWATSU	DS-6121	100	40	1	8	2k	2+1	●	●		●	●			●	●	●	●	●	●		●	●		●	O	O	●
	DS-6121A	100	40	1	8	2k	2+1	●	●	50	●	●	●		●	●	●	●	●	●		●	●		●	O	O	●
	DS-6411	40	10	2	8	16k	2+1		●	50			●		●	●	●	●	●			●	●		●	O	O	●
	DS-6612	60	20	2	8	16k	2+1	●	●	50			●		●	●	●	●	●			●	●		●	O	O	●
KIKUSUI	COM7061A	60	20	2	8	1k	4	●	●				●		●	●	●	●	●			●			●	●		
	COM7101A	100	50	1	8	1k	4	●	●				●		●	●	●	●	●			●			●	●		
	COM7201A	200	50	1	8	1k	4	●	●				●		●	●	●	●	●			●			●	●		
LEADER	LCD-100	0.2	3	1	6	256	1+1								●				●		●	●						
LECROY	9400	125	100	2	8	32k	2+1	●			O		●		●		●		●	●		●	●			●	●	
NICOLET	NIC-320	25	10	2	8	4k	2+1	●				●				●		●	●			●	●			●	●	
	2090-205A	25	50	2	8	4k	2+1					●				●			●			●				●	●	
	3091	0.3	1	2	12	4k	2+1					O			●	●			●			●				O	●	
	4094-4180	100	200	2	8	16k	2+1				●	●	●			●		●	●	O		●	●			●	●	
	4094-4175	75	50	2	8	16k	2+1	●			●	●	O			●			●	O		●	●			●	●	
PANASONIC	VP5730P	50	5	1	8	512	2+1	●	●	20	●		●		●	●	●		●			●	●		●	O		●
	VP5740P	100	·100	1	8	10k	2+1	●	●	10	●	●	●		●	●	●	●	●	●	●	●	●		●	●		●
PHILIPS	PM 3305	35	2	1	8	4k	4+1	●	●	10			●			●	●		●			●				O		
	PM 3315	60	125	1	8	256	2+1	●							●	●	●		●			●	●			●		
	PM 3320	200	250	2	10	4k	2+1	●		3	●	●	●		●	●	●	●	●	●	●	●	●	●		O	O	
TEKTRONIX	2220	60	20	1	8	4k	2+1	●	●	100					●	●	●		●			●	●			O	O	
	2221	60	20	1	8	4k	2+1	●	●	100	●		●		●	●	●		●			●	●			O	O	
	2230	100	20	1	8	4k	2+1	●	●	100	●		●		●	●	●		●			●	●		●	O	O	
	2430A	150	100	2	8	1k	2+2	●		2	●	●	●		●	●		●	●	●	●	●	●	●	●	●		●
	11401-11A52	500	20	1	10	10k	8	●			●		●	●		●	●		●	●	●	●	●		●	●	●	
	11402-11A71	1000	20	1	10	10k	8	●			●		●	●		●	●		●	●	●	●	●		●	●	●	

NOTE:
O = OPTIONAL FEATURE

TIME AND VOLTAGE MEASUREMENTS	FREQUENCY MEASUREMENT	EXTENSIVE MEASUREMENTS	WEIGHT (LBS)	PRICE ($)	COMMENTS
●	●	●	35	14,490	OPTIONAL DISK DRIVE
●	●		29	6500	8-CHANNEL LOGIC ANALYZER, PRINTER
			13	1990	
●	O		13	3050	
●	●	●	1.6	1995	HANDHELD MODEL, INCLUDES DVM
			13	1895	
●	O	O	17	2950	
●	O	O	18	5590	OPTIONAL INTERNAL PLOTTER
			24	2500	
●	O	O	26	4490	
●	O	O	38	6495	
●	O	O	25	7990	OPTIONAL INTERNAL PLOTTER
●	O	O	25	10,490	OPTIONAL INTERNAL PLOTTER
			18	888	
			20	2380	
●	●	●	25	10,100	
●	●	●	28	9950	
●	●	●	42	12,900	
●	●	●	42	17,600	
●	●	●	59	21,900	COLOR DISPLAY
●	●	●	59	23,400	COLOR DISPLAY
●	●	●	56	22,900	COLOR DISPLAY
			20	1950	
			33	3450	
●	●		33	4900	
●	●		29	7795	AUTOTRIGGERING
●	●		29	4975	
●	●		29	5475	
●	●		24	2570	
●	●		24	3795	
●	●		22	4195	
●	●		22	4995	
●	●		22	6495	100-MHz DIGITAL
			2.1	850	FULL DMM
●		O	30	9900	
●	●	●	23	7900	OPTIONAL BUBBLE-MEMORY PACK
●			46	13,720	DISK DRIVE INCLUDED
●			19	5300	OPTIONAL BUBBLE-MEMORY PACK
●	●	●	42	15,800	OPTIONAL DISK DRIVE
●	●	●	40	14,800	OPTIONAL DISK DRIVE
●			27	3800	
●	●	●	37	9900	INTERNAL PROGRAM MEMORY
			22	3315	
			26	5995	
●	●	●	39	9900	
			18	2995	
●	●		18	3995	
●	●		18	4995	OPTIONAL MEMORY EXPANSION
●	●	●	24	8900	INTERNAL PROGRAM MEMORY
●	●	●	44	15,405	PRICE INCLUDES TWO CHANNELS
●	●	●	46	20,900	PRICE INCLUDES TWO CHANNELS

are standard. You can add an optional waveform-processing keypad that provides such measurements as rise and fall time, overshoot, minimum, maximum, pulse width, period, and frequency. The keypad also allows you to perform envelope limit tests and post-storage filtering of signals.

You can use the 4074's optional, internal color plotter for hard-copy results, or you can send the data over an IEEE-488 or RS-232C interface to a plotter, printer, or computer. Both interfaces allow you to read and write most front-panel setups, as well as the contents of the display memory and the reference memories. When you're looking at a single-shot waveform on the display, you can select dots only, linear interpolation, or curve interpolation. Gould also offers the 4072, which has the same measurement features as the 4074's, but has two input channels.

Hewlett-Packard's 100-MHz 54112D has an exceptionally long (64k-sample/channel) record memory, which lets you store a 163-μsec event with a data point every 2.5 nsec on four channels simultaneously. The instrument's full-magnification mode lets you stretch one record over as many as 128 screens, which you can pan through.

The 54112D also has a color display. Don't underestimate the value of this feature. Multiple traces, different vertical-deflection factors, and cursors with readouts all on the same screen can be confusing. By grouping channels by color, a color display takes away the confusion. The color display is also helpful when you overlay two waveforms for comparison.

Earlier this year, Nicolet introduced the 4180 plug-in for its 4094 DSO. The plug-in lets the scope digitize 8 bits at 200M samples/sec. The scope accepts two plug-ins for a total of four input channels with a 100-MHz bandwidth. Each channel has a 16k-sample record length for 80 μsec of storage at the maximum sampling rate. The 4180 doesn't support equivalent time sampling; to obtain this feature, you can choose another plug-in, the 75-MHz 4175, which digitizes single-shot waveforms at 50M samples/sec and repetitive waveforms at 2-nsec intervals. The 4094 gives you extensive measurement and waveform-processing capabilities, including FFTs. Other plug-ins for the 4094 provide as many as 15 bits of vertical resolution at reduced sampling rates. The 4094 also has a plug-in with a disk-drive unit for storing waveforms and for additional processing.

If you want a DSO that can also function as a 100-MHz analog scope, you can choose from a number of

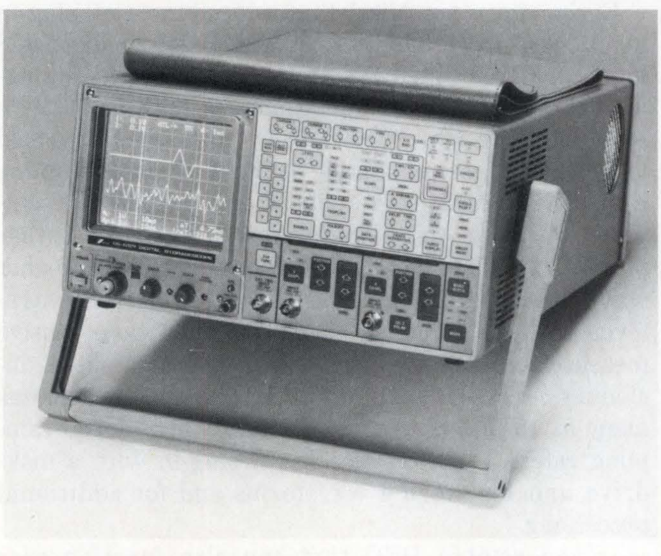
Many DSOs can be connected to a computer for automated control and data analysis.

analog-and-digital models offered by Hitachi, Iwatsu, Kikusui, Panasonic, and Tektronix. All these scopes have equivalent time sampling, XY display, roll mode, and envelope display mode to help you catch glitches even at low sweep rates.

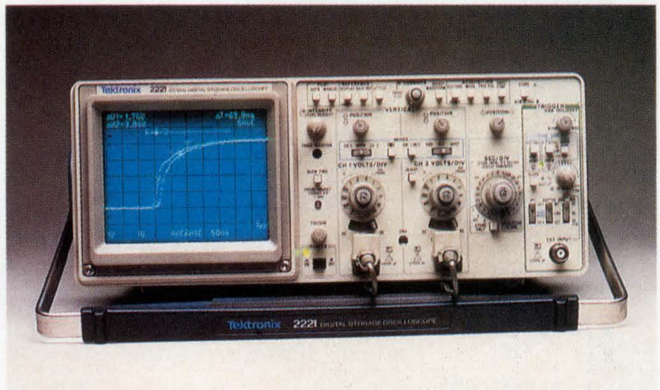
Hitachi's 100-MHz VC-6165 digitizes at 100M samples/sec on two channels simultaneously. It provides sweep-speed autoranging and trigger lock. The trigger-lock feature keeps the sum of sweep time and hold-off constant so that you can change sweep speed without losing the trigger on complex pulse trains. Iwatsu's 100-MHz DS6121A digitizes at 40M samples/sec on one channel and 20M samples/sec on two. Cursors with readouts are available for both the digital and the analog mode. The instrument's go/no-go envelope test mode lets you capture waveforms that fall inside a user-selected time and voltage envelope. Its setup memory allows you to store and recall front-panel settings.

The 100-MHz COM 7101A from Kikusui digitizes one channel at 50M samples/sec and as many as four channels at a reduced sample rate. Kikusui also offers the COM 7201A, which has a 200-MHz analog bandwidth, although the digital portion of the scope is still limited to 100 MHz.

Digitizing one channel at 100M samples/sec or two channels at 50M samples/sec, Panasonic's 100-MHz VP5740P lets you capture 10-nsec glitches even at low sweep speeds. The instrument's 10k-sample record length lets you store long waveforms. This scope not only provides setup memory, but also has an autosetup



Go/no-go testing of waveforms *allows Iwatsu's 6121A to capture glitches.*



Analog and digital functions are combined *on Tektronix's 60-MHz 2221; this feature is common in many DSOs that offer bandwidths of 100 MHz or less.*

feature. In addition, you can program the scope to run as many as 1000 steps in an automated measuring sequence.

Finally, Tektronix's 2230 analog-and-digital scope digitizes one channel at 20M samples/sec or two channels at 10M samples/sec. It has a 4k-sample record length. At 18 lbs, the 2230 is the lightest 100-MHz DSO available.

High-bandwidth DSOs

If you're looking for a digitizing scope with a bandwidth of 500 MHz to 1 GHz for repetitive events, you can choose from some impressive offerings from Tektronix and Hewlett-Packard. Tektronix's 11402, with a 11A71 plug-in, has a 1-GHz bandwidth and digitizes 10 bits at 20M samples/sec. When you use repetitive sampling, the instrument provides 10-psec time resolution. You can display eight of the 12 input channels at once on the 9-in. screen.

Operating mostly from the touchscreen menu, the 11402 has few knobs and buttons. One of the buttons it does have initiates what the company calls an "enhanced accuracy" feature, which calibrates the scope all the way out through the probe, giving it better than 1% vertical accuracy for scope measurements. Three microprocessors update the screen quickly when performing functions such as averaging, which tend to slow some scopes down.

The 11402's 10k-sample record lengths let you record relatively long waveforms in detail. Its dual timebases allow you to look at a magnified portion of one trace while the other trace remains on the screen. Tektronix's 11401 DSO is similar to the 11402 except that its bandwidth is limited to 500 MHz. The company offers a variety of plug-ins for both scopes; the same plug-ins

Competition between manufacturers at all levels is bringing DSO prices down while increasing the number of extra measurement features on the scopes.

Two analog channels and eight logic channels *are combined on the SE571 from BBC-Metrawatt/Goerz.*

also serve Tektronix's 11300 Series analog scopes. The 11400 Series scopes offer extensive measurement functions, such as rise- and fall-time measurement, and built-in IEEE-488 and RS-232C interfaces.

Also featuring a 1-GHz bandwidth are Hewlett-Packard's 54100 A/D and 54110D. These models digitize 7 bits at 40M samples/sec on two channels simultaneously with 10-psec resolution in equivalent-time-sampling mode. The 54110D has a color display. Like Tektronix's 11400 Series, HP's 54100 Series offers an extensive list of waveform measurements, triggering, and display features.

Hewlett-Packard added a faster digitizing scope to the 54100 family in the last year. This scope—the 54111D—has a maximum digitizing rate of 1G samples/sec on two channels simultaneously, so it's a good choice for fast single-shot applications. Its 8k-sample record length allows you to store waveforms in detail. The vertical resolution on this scope ranges from 8 bits at 25 MHz to 6 bits at 250 MHz. For repetitive operations, the scope has a 500-MHz bandwidth.

Another high-performance DSO is Philips's PM 3320, which has a 200-MHz bandwidth and offers 10-bit-resolution sampling at 250M samples/sec. Its record lengths vary from 512 words at the maximum sweep speed to 4k samples at lower sweep speeds. The DSO provides glitch capture on 3-nsec pulses even at the lowest timebase settings. For repetitive events, you can use equivalent time sampling to get 100-psec resolution. This scope also has an autosetup feature, and it lets you store 77 different front-panel settings.

All scope manufacturers are working hard to make their DSOs easy to operate for the new or infrequent user. A particularly user-friendly DSO is Tektronix's 2430A, which also offers both high performance and flexibility. The 2430A provides a button that lets you get on-screen help for all functions, so you don't have to look for the manual. The scope has a 150-MHz bandwidth, and it samples two channels simultaneously at 100M samples/sec. It features an analog glitch-capture circuit that captures 2-nsec glitches, so it can see glitches in the single-shot mode that would otherwise require a much higher sampling rate.

The 2430A's autostep feature lets you enter and

TABLE 2—DIGITAL-STORAGE-OSCILLOSCOPE SELECTION GUIDE

<50-MHz BANDWIDTH		50- TO 99-MHz BANDWIDTH		100- TO 200-MHz BANDWIDTH		>200-MHz BANDWIDTH	
<20M SAMPLES/SEC	≥20M SAMPLES/SEC	<100M SAMPLES/SEC	≥100M SAMPLES/SEC	<100M SAMPLES/SEC	≥100M SAMPLES/SEC	<200M SAMPLES/SEC	≥200M SAMPLES/SEC
GOULD	ANALOGIC	HITACHI	HEWLETT-	IWATSU	GOULD	HEWLETT-	HEWLETT-
1421	6100-620-1	VC-6050	PACKARD	DS-6121	4072	PACKARD	PACKARD
1425	BBC-METRA-	IWATSU	54200D	DS-6121A	4074	54100A	54201D
HAMEG	WATT/GOERZ	DS-6612	PHILIPS	KIKUSUI	HEWLETT-	54100D	54111D
HM205-2	SE571	KIKUSUI	PM 3315	COM7101A	PACKARD	54110D	
HITACHI	B&K PRECISION	COM7061A		COM7201A	54112D	TEKTRONIX	
VC-6020	2520	NICOLET		TEKTRONIX	HITACHI	11401	
IWATSU	2521	4094-4175		2230	VC-6165	11402	
DS-6411	DOLCH SC01	PANASONIC			LECROY		
LEADER	GOULD	VP-5730P			9400		
LCD-100	1604	TEKTRONIX			NICOLET		
NICOLET	4030	2220			4094-4180		
NIC-320	4035	2221			PANASONIC		
3091	4050				VP-5740P		
PHILIPS	HAMEG				PHILIPS		
PM 3305	HM208				PM 3320		
	HITACHI				TEKTRONIX		
	VC-6041				2430A		
	NICOLET						
	2090-205A						

Some DSOs offer curve interpolators that let you look at a fairly good representation of a waveform while sampling at four times the signal frequency.

Manufacturers of digital storage oscilloscopes

For more information on digital storage oscilloscopes, contact the following manufacturers directly or circle the appropriate numbers on the Information Retrieval Service card.

Analogic Corp
Data Precision Div
16 Electronics Ave
Danvers, MA 01923
(617) 246-1600
Circle No 650

BBC-Metrawatt/Goerz
2150 W 6th Ave
Broomfield, CO 80020
(303) 469-5231
Circle No 651

B&K Precision, Dynascan Corp
6460 W Cortland St
Chicago, IL 60635
(312) 889-8870
Circle No 652

Dolch American Instruments Inc
2029 O'Toole Ave
San Jose, CA 95131
(408) 435-1881
Circle No 653

Gould Inc
3631 Perkins Ave
Cleveland, OH 44114
(216) 361-3315
Circle No 654

Hameg Inc
88-90 Harbor Rd
Port Washington, NY 11050
(516) 883-3837
Circle No 655

Hewlett-Packard
Box 10301
Palo Alto, CA 94303
Phone local office
Circle No 656

Hitachi Denshi America Ltd
175 Crossways Park West
Woodbury, NY 11797
(516) 921-7200
Circle No 657

Iwatsu Instruments Inc
430 Commerce Blvd
Carlstadt, NJ 07072
(201) 935-5220
Circle No 658

Kikusui International Corp
19601 Mariner Ave
Torrance, CA 90503
(213) 371-4662
Circle No 659

Leader Instruments Corp
380 Oser Ave
Hauppauge, NY 11788
(516) 231-6900
Circle No 660

LeCroy Research Systems
700 S Main St
Spring Valley, NY 10977
(914) 425-2000
Circle No 661

Nicolet Test Instruments Div
5225 Verona Rd
Madison, WI 53711
(608) 273-5008
Circle No 662

Panasonic Industrial Co
2 Panasonic Way
Secaucus, NJ 07094
(201) 392-4050
Circle No 663

Philips Test & Measuring Instruments Inc
85 McKee Dr
Mahwah, NJ 07430
(201) 529-3800
Circle No 664

Tektronix Inc
Box 500
Beaverton, OR 97077
(503) 627-7111
Circle No 665

execute measurement routines right at the scope without using a separate computer for control. The instrument's waveform-parameter-extraction feature gives you a screen with 20 automatic waveform measurements, including rise and fall times, pulse width, overshoot, undershoot, peak-to-peak voltage, and frequency. An optional word-recognizer probe allows you to trigger from a 17-bit logic word.

DSOs provide logic-analyzer functions

Although further developments in DSOs will continue to come mainly in the form of higher bandwidths and sampling rates, some lower-bandwidth models are also providing improvements such as extra functions. For example, BBC-Metrawatt/Goerz recently came out with the SE571, a 15-MHz DSO that has two analog channels and eight logic-analyzer channels; it gives you 25M-sample/sec sampling on all channels simultaneously. The built-in printer can provide a hard copy of what you see on the screen in 10 seconds. The scope has cursor functions, as well as autoranging, setup memory, and autosetup.

Another noteworthy scope, the Scout SC01 from Dolch, packs a surprising amount of capability into a 25-oz, handheld DSO. It gives you two 5-MHz channels that sample at 20M samples/sec simultaneously. Each channel has its own timebase. The instrument also offers such features as equivalent time sampling, pretriggering, post-triggering, XY mode, and roll mode. Besides providing the functions of a DSO, the instrument also functions as a DMM that measures rms voltages to 1 MHz and frequency to 7 MHz. It has multiple microprocessors and custom VLSI chips on three surface-mount-technology circuit boards. The display is a 128×128-element LCD matrix.

As for future developments, you can expect to see all the high-end scopes coming out with color displays in the next two years. It's possible, too, that in the not-too-distant future, DSOs and logic analyzers may be combined in a single instrument. BBC-Metrawatt/Goerz's 15-MHz SE571 already provides logic-analyzer functions, and at least one company offers a logic analyzer that has DSO channels. **EDN**

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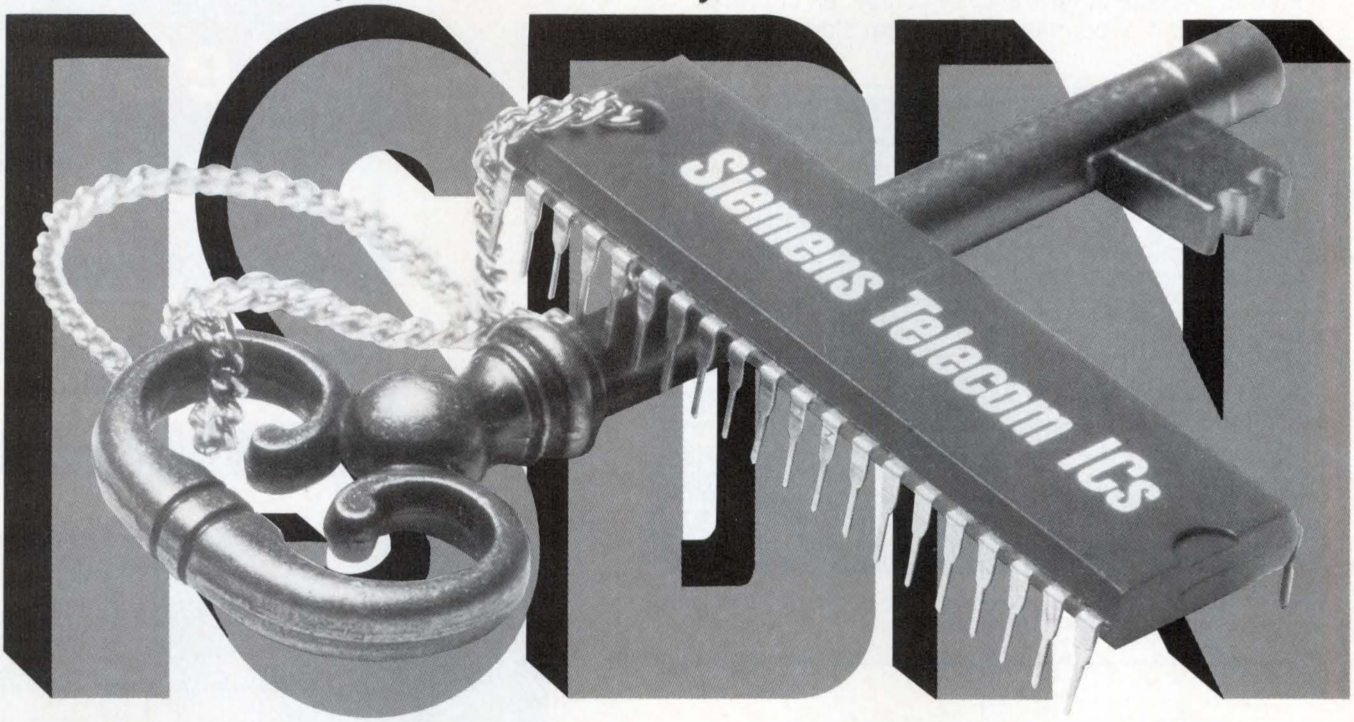

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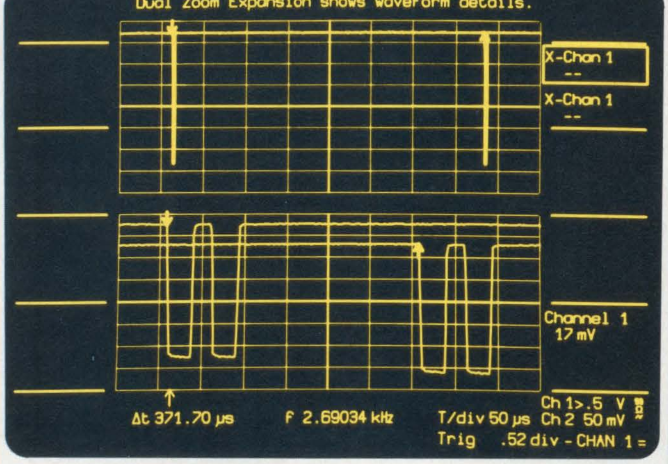

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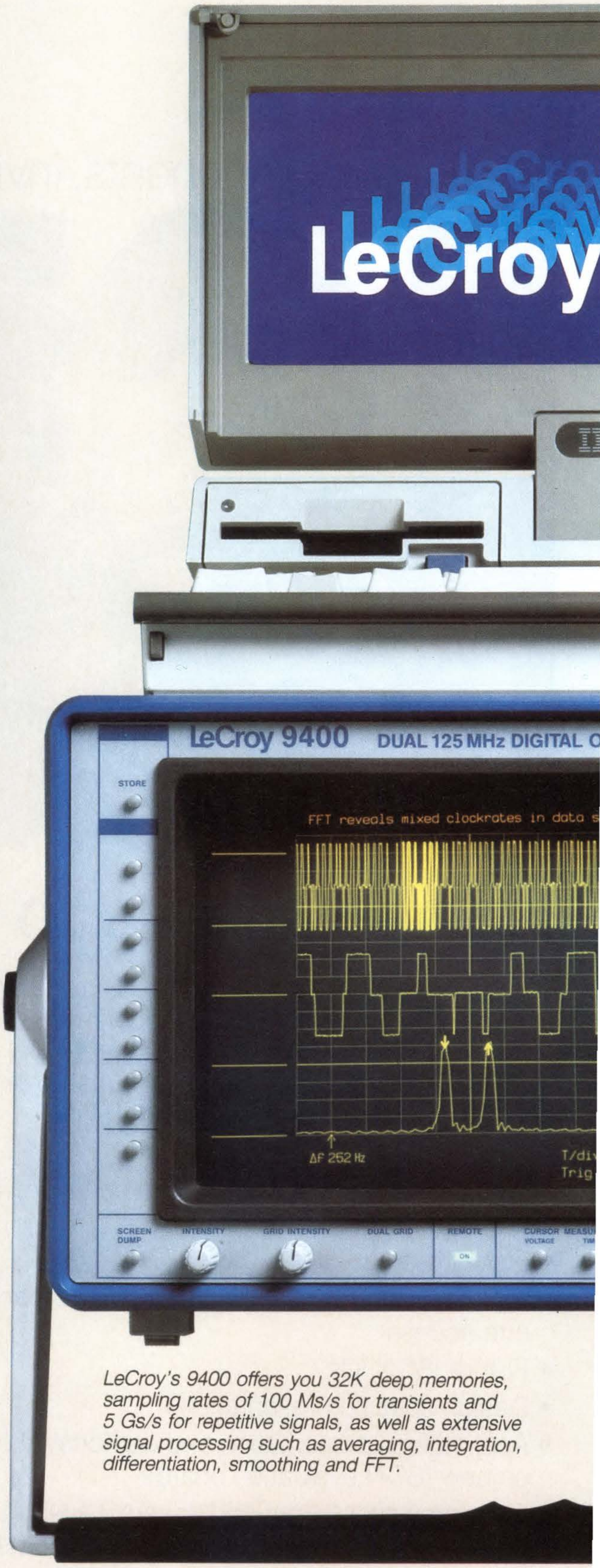

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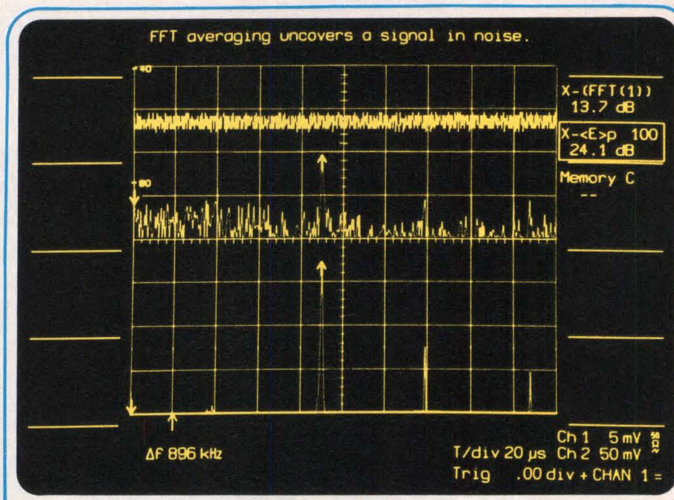

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Characterized analysis reduces error in digitizing instruments

Although digital signal processing enhances the usefulness of digitizing instruments, it also allows for instrumentation-induced errors that don't occur in conventional instruments. A technique called characterized analysis can define these errors.

David M George, *Hewlett-Packard*

A single digitizing instrument can emulate the capabilities of racks of conventional instruments, and many digitizing instruments provide measurements with high resolution. Not all the digits they produce are necessarily accurate, however. Instrument manufacturers typically specify their hardware's errors reasonably well, but they seldom specify their software's errors. In any case, you need to know more than just the hardware- or software-induced error—after all, it's the performance of the entire instrument system that is critical. You need hard numbers for the instrument's performance from its input connector to the final displayed result. Characterized analysis, which provides an overall, quantified characteristic for the entire hardware/software signal-processing chain, can eliminate uncertainty in digitizing instruments that use digital signal processing.

Errors in digitizing instruments that have built-in analysis functions fall into three basic groups: ac, dc, and algorithmic errors. An instrument's analog front end and its digitizing hardware together account for the ac and dc errors. Engineers familiar with A/D conversion understand these error sources well, and most digitizing-instrument makers do a good job of characterizing the dc and ac performance of their instruments. DC errors determine how accurately an instrument digitizes a dc level, and ac errors relate how accurately it digitizes a time-varying signal (see **box,** "Digitizers suffer from hardware errors").

Algorithmic errors determine how well the instrument's analysis package translates the raw digitized data into voltages, frequencies, timing intervals, and frequency spectrums, for example. Algorithmic errors are not as well understood by manufacturers and users as dc and ac errors are.

Algorithmic errors and their sources

Algorithmic errors can show up in several different ways: for example, data can be skewed in time, voltage, or frequency. Algorithmic errors can severely reduce the precision and dynamic range of the original digitized data. Poorly designed algorithms can even result in completely incorrect answers. Some of the errors that result from bad algorithms are round-off noise, interpolation error, and the failure to approach valid estimation limits.

Error may occur even when the algorithms aren't bad

Algorithmic errors can severely reduce the precision and dynamic range of the original digitized data.

ones: For example, an instrument's software designer may have used an incorrect application or nonstandard implementation of an otherwise valid algorithm. Also, the user could unwittingly select the wrong algorithm for a given application from a suite of algorithms supplied by the instrument.

Round-off noise

Mathematically processing the digitized data with finite numbers causes round-off noise. When the instrument simply displays its captured data as points, or reads them out as times and voltages, the original precision proves adequate; for instance, 8-bit data can remain in its 8-bit, fixed-point format. If the instrument performs further operations on the data—say, multiplying two waveforms together—the range of the arithmetic operations becomes a concern.

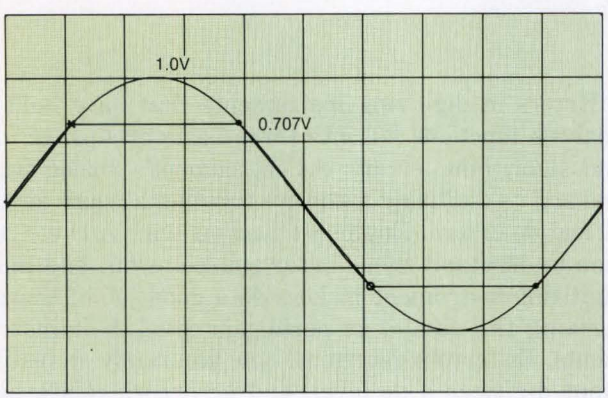


Fig 1—Different interpolation schemes *introduce different amounts of error when determining waveform characteristics that occur between sample points. For example, straight-line interpolation could result in an error of as much as 30% when the algorithm is estimating the peak of this waveform.*

For 8-bit data, its range before multiplication is 0 to 256; after multiplication, the range extends to 0 to 65,536 (or 16 bits) for a fixed format. Therefore, an 8-bit multiplication will probably overflow if the instrument doesn't increase the range of the result.

Typically, the algorithm's designer will use floating-point math to circumvent this trap. The designer will round off the result and retain only some of the less-significant bits (perhaps eight, perhaps more) of the result's mantissa. Repeated calculations involving rounded-off numbers can cause errors to accumulate.

The same effect of round-off noise comes from the uncertainty of the least significant digit in a discrete, digitized datum. Using floating-point math to determine the mean of a series of numbers, and varying the mantissa of the numbers from 8 to 12 bits **(Table 1)**, illustrates this effect. Averaging the numbers from 255 to 247 using an 8-bit mantissa yields 248, when the correct answer is 251. In this example, an error will occur in the mean unless the algorithm uses a 12-bit or larger mantissa, even though the data being averaged is only 8 bits long.

Interpolation errors

Interpolation errors arise because the digitized data is taken at discrete time intervals, but points of interest—the waveform's peaks, zero crossings, or its 10 and 90% points—don't necessarily occur during the sample intervals, and they can occur between two samples. Therefore, the analysis software must interpolate between samples to quantify the intersample events of interest.

The effectiveness of different interpolation schemes depends on the following parameters: the bandwidth of

TABLE 1—ROUND-OFF NOISE AS A FUNCTION OF SIGNIFICANT DIGITS FOR 8-BIT DATA

DATA POINTS TO BE AVERAGED	PRECISION OF MANTISSA	INTERIM SUMMATION	MANTISSA IN BINARY	EXPONENT IN BINARY	RESULTANT MEAN
255 254	8 BITS	140×2^4	1000.1100	100	248
253 252	9 BITS	281×2^3	1.0001.1001	11	249.5
251 ← MEAN 250	10 BITS	564×2^2	10.0011.0100	10	250.5
249 248	11 BITS	1411×2^1	101.1000.0011	1	250.875
247	12 BITS	2259×2^0	1000.1101.0011	0	251

the signal, the sample rate, and—for a given point in time—the preceding and succeeding number of samples used in the calculations. Because of this last condition, calculations at the boundaries (the beginning and end of the record) which obviously lack preceding and succeeding samples, respectively, therefore have the highest likelihood of inducing interpolation errors.

Several methods used to interpolate the points between digitized samples are the straight-line, sinc ([sin x]/x), parabolic, and Gaussian methods. **Fig 1** shows that when straight-line interpolation is used to find the peak amplitude of a waveform, it produces an error of as much as 30% for a signal that has four points/cycle. Parabolic interpolation produces an error of 12% under the same conditions. Sinc interpolation, on the other hand, furnishes an answer that has very little error, providing that the sample is properly bandlimited and the interpolation occurs away from the record's boundaries.

A different kind of error, associated with sinc interpolation, is called Gibbs's phenomenon. When sinc interpolation is used to perform waveform reconstruction with a sinc function on nonbandlimited data, Gibbs's phenomenon results in overshoot. **Fig 2** illustrates this phenomenon, which results in an error of 9% for nonbandlimited signals.

Quantization error leads to estimation limits

No matter how good an algorithm is, an absolute limit (referred to here as an estimation limit) to the algorithm's accuracy exists if you use it to process finite time records that have quantization error. Quantization error is present even in an ideal A/D converter. Round-off noise and interpolation error can also lead to estimation limits, but quantization error is typically the major contributor for ideal data; system noise and distortion may be the limiting factor for real data.

Estimation limits arise because the inevitable quantization error introduces a fixed error into each sample which ranges between zero and some computable maximum. As you analyze more data, that is, you process a longer time record. Effective signal processing will reduce some, but not all, of this fixed error. The amount of reduction is a function of the number of samples analyzed. As you analyze larger and larger records, the accuracy will approach the estimation limit asymptotically.

You can observe a classic example of this error reduction when you use the digitized data to determine the frequency in a zero-crossing estimation scheme. As **Fig 3** shows, the frequency estimation becomes more accurate in a linear fashion as the gate time increases (the sample rate is held constant, which increases the number of samples analyzed). This increase in accuracy will continue, assuming the data is digitized perfectly, until the algorithm reduces the error to the asymptotic error limit.

Incorrect application of an algorithm often results in errors. For example, the algorithm that determines the

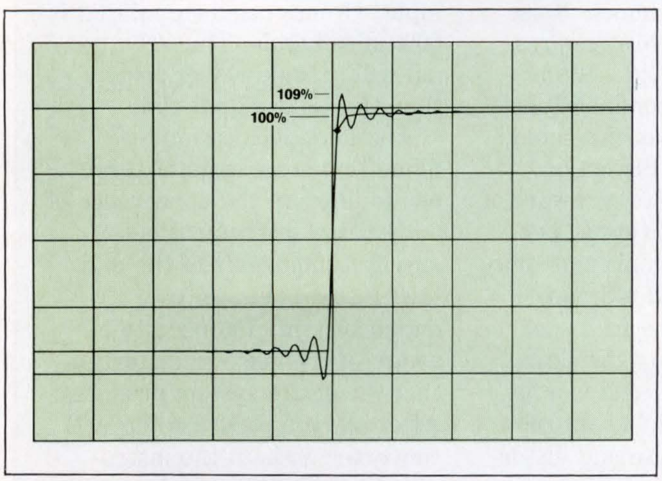


Fig 2—Gibbs's phenomenon results in overshoot *when the digitizing instrument performs waveform reconstruction with a sinc function on nonbandlimited data. In this example, Gibbs's phenomenon causes an error of 9% for a nonbandlimited signal.*

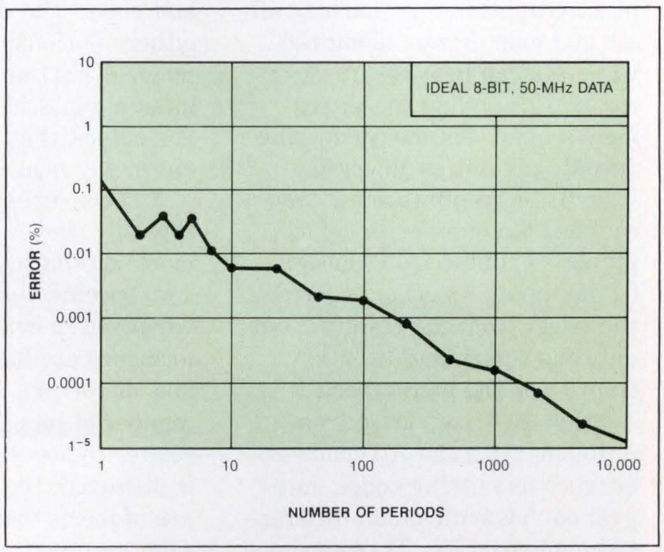


Fig 3—This plot of worst-case timing error *(arising from the quantization-error component of total estimation error) shows that frequency estimation becomes more accurate, in a linear fashion, as the gate time increases. The sample rate remains constant, thus increasing the number of samples analyzed.*

Mathematically processing digitized data with finite numbers causes round-off noise.

rms value of a digitized waveform can often yield errors simply by operating on the wrong portion of a set of digitized data. Typically, when digitizing-scope users (for example) want to perform an rms measurement on a signal, what they really need is a periodic rms measurement. That is, they need the rms value of one cycle of the captured waveform rather than the rms value of the entire data set.

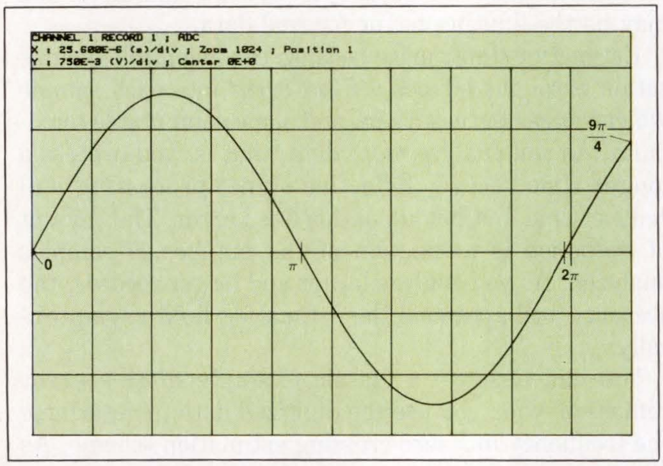


Fig 4—An rms-voltage calculation derived from this nonperiodic sine wave yields a 4% algorithmic error in comparison with the true-rms value of a periodic sine wave of the same frequency. Some digitizing instruments can perform both periodic and nonperiodic rms measurement.

Although the nonperiodic rms measurement is a useful analysis tool for transient phenomena, the lack of a periodic-rms function can severely limit the accuracy of the instrument in other cases. For example, a nonperiodic rms calculation over a set of captured data of a sine wave that has 1⅛ periods (rather than an integral number of periods) is limited to approximately 4% accuracy (**Fig 4**).

Nonstandard algorithm implementations

Some engineers might not see anything wrong with an algorithm designer's employing a nonstandard implementation that gets the job done and produces correct answers. One problem with nonstandard implementations, however, is that you can compare their results only against other results obtained with the same algorithm. The results might not be checked against any absolute standard or across the industry. If the manufacturer of your instrument decides to get out

Digitizers suffer from hardware errors

When a signal is digitized, it traverses the entire instrument, picking up dc errors, such as offset and gain errors, along the way. You can best see offset errors by grounding the instrument's input and measuring the output; any output deviation from 0V is an offset error. You can measure gain error by applying a calibrated 1V dc signal to the input. After you subtract the offset from the resulting output, any remaining deviation from 1V is the gain error.

Other dc errors arise from problems with the A/D converter, such as missing codes, integral nonlinearities, and differential nonlinearities. These are not only dc problems; they cause more havoc as the frequency of the input signal increases.

Two basic mechanisms degrade an ac signal: distortion and noise. The distortion can be either spurious distortion or harmonic distortion linked to the input signal's harmonics. Noise is a culprit that is always present in any measuring system.

A/D-converter nonlinearities typically show up as either harmonic or spurious distortion. Two specifications to be aware of when you're evaluating ac performance are harmonic and spurious distortion, and effective number of bits. The first spec relates to how badly the signal is distorted; the second is a figure of merit that takes into consideration both noise and distortion.

You should note that to compare digitizing instruments accurately, you must compare systems that have been tested under similar conditions. For instance, some manufacturers test their products using a full-scale input. Others use a signal that is 50% of full scale. The 50% signal will provide better specs than the 100% signal will.

Another specification technique that some manufacturers use to improve the appearance of a digitizing instrument is to specify components of the digitizer instead of specifying the entire system. You need to be aware of the noise or distortion that the entire system produces: After all, you can't use the A/D converter without the instrument's analog front end.

of the digitizing-instrument business, your historical files will be useless if the instrument fails or if you have to obtain additional instruments from another maker. The IEEE 194-1977 standard is an example of a standard used to characterize pulses (**Fig 5**).

When you use a digitizing instrument that provides multiple analysis techniques, you may have trouble deciding which algorithm to use. For instance, you can measure frequency by using a fast Fourier transform (FFT) or by using a zero-crossing estimation scheme. The best resolution an FFT can produce for a 50-MHz signal and 1024-sample record is 0.5% at a 4-nsec rate. The frequency-counting function of the HP 5185T digitizing oscilloscope, which uses a zero-crossing scheme, provides better than 0.008% relative accuracy for a record length of the same size (204 periods). Without some measure of the algorithms' accuracy, however, you wouldn't know which one to choose for a particular task.

Different FFT windows yield different results

When an instrument performs FFTs, it usually provides several different windowing functions. As **Fig 6** shows, different windows yield different results when applied to the same waveform. Flat-top windowing provides amplitude resolution of 0.01 dB, but its 3-dB resolution bandwidth is 3.8 times wider than the resolution bandwidth of uniform windowing. Hann windowing has a maximum error of 1.5 dB, but its resolution bandwidth is only 1.6 times wider than that of uniform

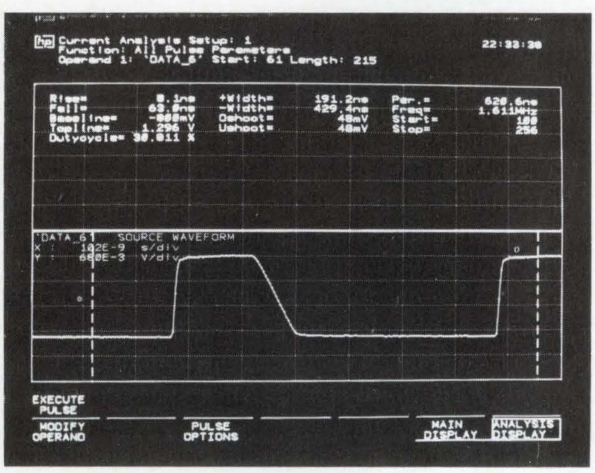
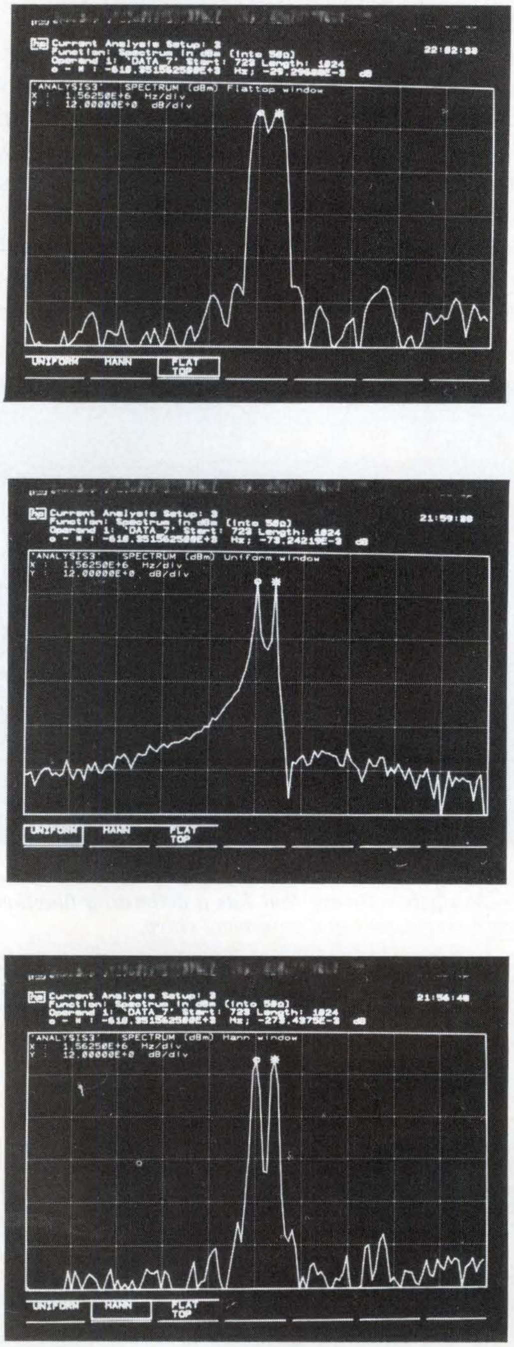


Fig 5—The IEEE 194-1977 standard is an example *of an industry standard that's used, in this case, to characterize pulses.*



(a)

(b)

(c)

Fig 6—The flat-top-window function (a) shows *frequency resolution that's 3.8 times wider than that obtained with uniform windowing* ***(b)****; the Hann window function* ***(c)*** *provides frequency resolution that's 1.6 times wider than that of uniform windowing. The benefit of flat-top windowing is its amplitude accuracy of 0.01 dB. In contrast, Hann windowing produces 1.5-dB amplitude accuracy, and uniform windowing produces 4-dB amplitude accuracy.*

windowing. Uniform windowing has the best frequency resolution for signals that are close in amplitude, but its amplitude error can reach 4 dB.

In order to get the most out of a particular instrument, you must understand the different windowing functions that digitizing instruments use. If amplitude resolution is of prime importance, the flat-top windowing function is what you should use. If frequency resolution of signals with similar amplitudes is the key issue, then you should choose uniform windowing. Hann windowing **(Fig 6c)** is a good compromise between amplitude accuracy and frequency resolution.

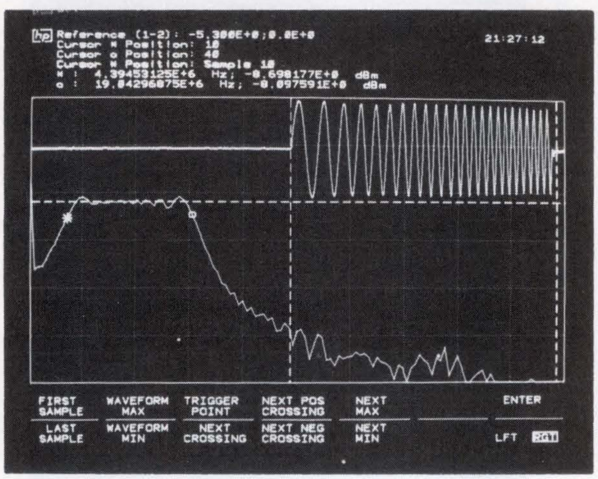


Fig 7—Analysis software that has a delimiting function *lets you analyze a single cycle of a sinusoidal chirp.*

For measuring the frequency of a single tone accurately, a zero-crossing estimation scheme is a better choice than any form of FFT.

Some digitizing instruments can start and end calculations at only the first and last sample of the recorded waveform. This characteristic severely limits the accuracy and resolution of some derived measurements. For example, performing a periodic-rms voltage measurement on a series of bursts that have a 50% duty cycle will result in a 50% error unless the instrument can process just the active portions of the waveform.

Limitations can result, for example, when you want to perform statistical measurements on a series of sine-wave chirps. If this statistical information is of interest, then you must be able to make a delimited measurement, analyzing just a single chirp **(Fig 7)**. Digitizing instruments that can start and end calculations at only the first and last sample of the waveform don't have sufficient flexibility to analyze smaller sections of the waveform, such as single bursts of the frequency chirp.

A solution to the uncertainty that signal-processing errors engender is a system of characterized analysis. Characterized analysis provides an overall (that is, for both hardware and software) accuracy characteristic for a digitizing instrument for each of its applications: voltmeter, frequency counter, and spectrum analyzer. **Fig 8** shows three characterized-analysis plots for the HP 5185T digitizing oscilloscope. Characterized analysis doesn't require you to know the ac, dc, or algorithmic errors, or how these errors interact with each

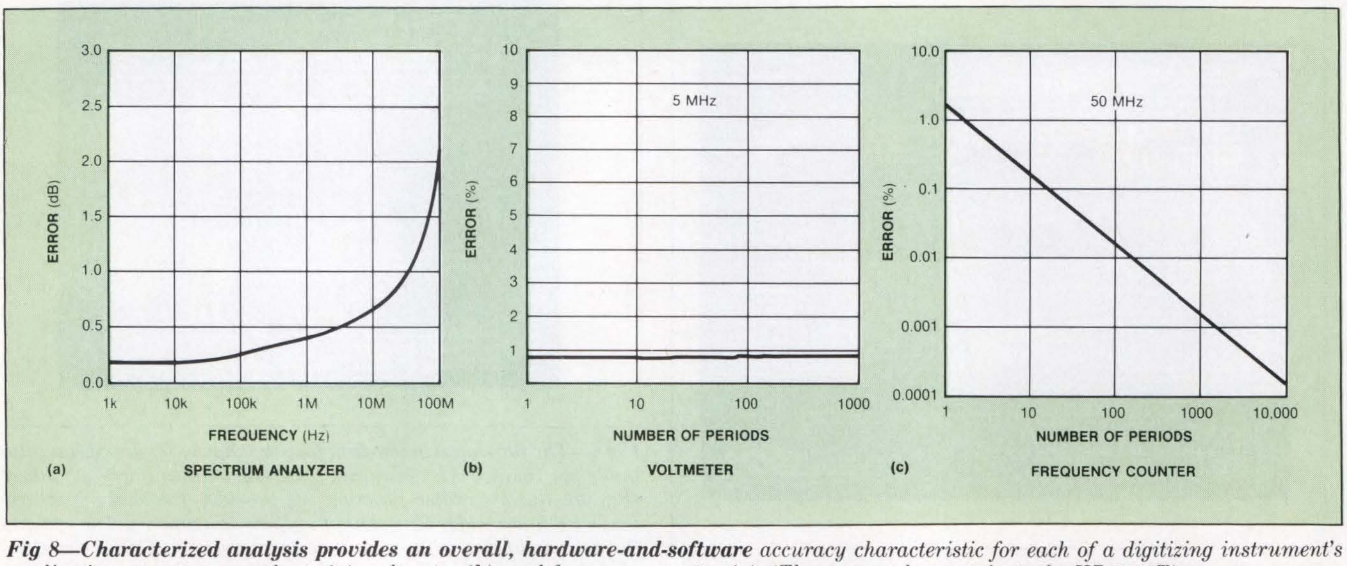
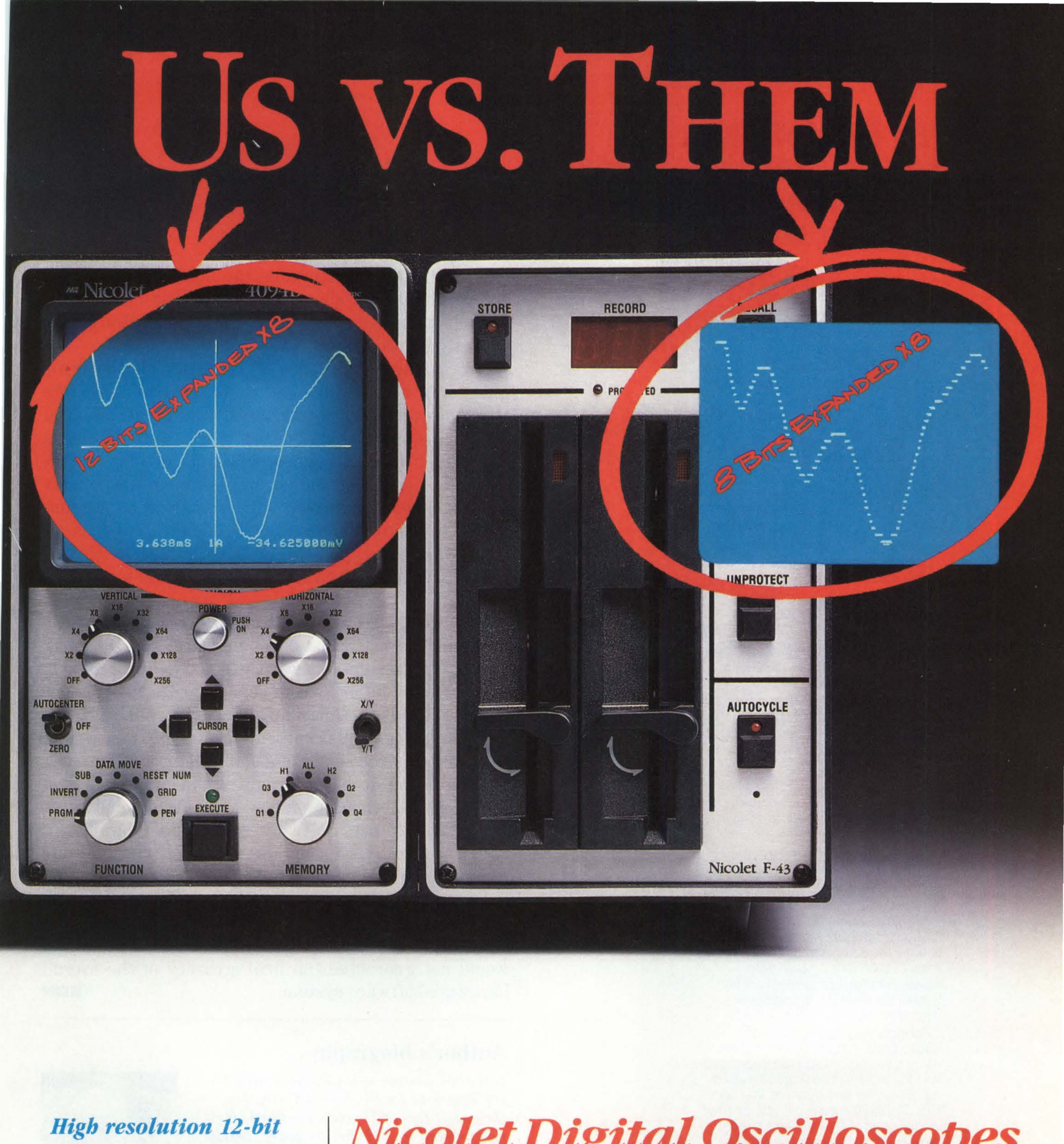


Fig 8—Characterized analysis provides an overall, hardware-and-software *accuracy characteristic for each of a digitizing instrument's applications: spectrum analyzer* ***(a)****, voltmeter* ***(b)****, and frequency counter* ***(c)****. (These examples pertain to the HP 5185T).*



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other, in order to determine the instrument's overall accuracy. Instead, characterized analysis provides an overall, quantified characteristic for the hardware/software signal-processing chain.

Not having quantified characteristics for the error introduced by software can cause even worse errors than those already enumerated. The worst case you could encounter would occur if you were to use a digitizing instrument simply as a front end for capturing data, doing your signal processing on a computer with untested third-party software having no warranty. In this situation, besides facing the problems already discussed, you might have to deal with bad algorithms, bugs in the implementation, and formatting errors.

Formatting errors result from incorrect assumptions about the format of data. For instance, your digitizer may output straight binary code or Gray code. Further, its data could be in 1's complement or 2's complement form. These issues may appear trivial, but they can keep an instrument from being useful or, even worse, they can require the aid of a software programmer.

Even if you do buy software with a warranty, you won't have information on how the software and hardware will interact. Software warranties typically ensure that the purchased software will run on your computer (or the manufacturer will make good on it), but say nothing about how much the analysis degrades the digitized data. Even if a warranty were to state how much error the software would add, this warranty still would not guarantee the final accuracy of the overall hardware/software system. **EDN**

Author's biography

David M George is a product-marketing engineer for the Santa Clara Instrument Div of Hewlett-Packard. He has worked for HP for 10 years. David obtained a BSEE from the University of Utah and an MSEE from Stanford University. He is a member of the IEEE and enjoys skiing, scuba diving, bicycling, running, dancing, and windsurfing in his spare time. David is interested in German culture and claims to be semifluent in German.

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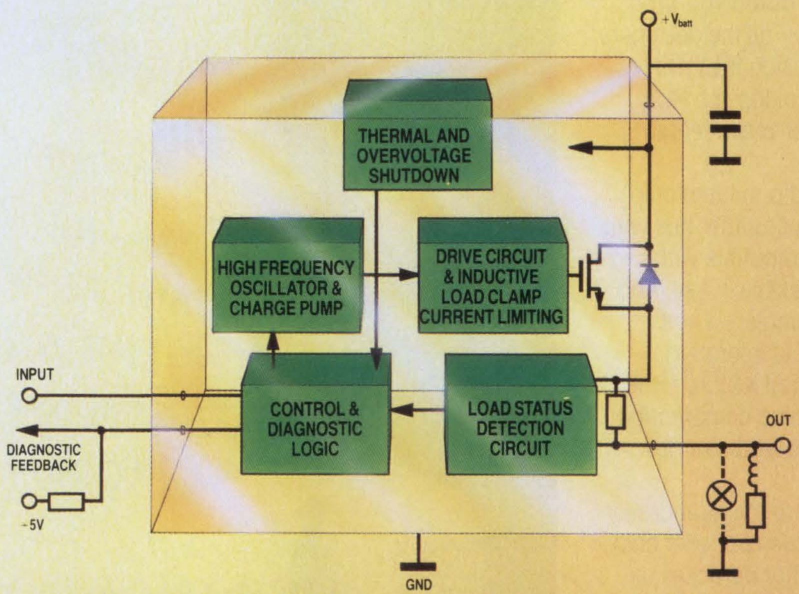

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Special circuit simplifies testing of voltage comparators

Voltage comparators generally have wide bandwidth and high gain—qualities that actually invite instability whether the device is operating in an application circuit or a test loop. You can modify the conventional op-amp test circuit to test the comparator, but a better solution is to build a comparator tester dedicated to the task.

Barry Harvey, *Elantec Inc*

Most analog engineers view the voltage comparator as a troublesome device because its wide bandwidth and high gain make it prone to oscillation. It's no surprise, then, that if you connect a comparator in a standard op-amp test circuit, it will most likely exhibit at least one of the following: input oscillation, output oscillation, or high-frequency, burst-mode oscillation involving the entire test circuit. Special requirements burden the measurement of a voltage comparator's ac and dc parameters. The test fixture must present a low-inductance connection to the comparator's ground pin, for example, and you may have to include a square-wave source on the fixture (commercial signal generators seldom produce the fast, clean step functions required).

If your application requirements necessitate the use of a voltage comparator, you'll find it helpful to understand why the op-amp test setup is generally unsuitable, how to build a dedicated circuit that is suitable, and how to modify and use the op-amp test circuit when building a dedicated tester isn't practical.

Fig 1 shows the basic loop for measuring an op amp's dc parameters. If, for instance, $V_{CM}=0V$ and you close S_1 and S_2, then the combined effect of the R_1/R_2 attenuator and feedback in the R_4, C_1, R_5, and IC_1 loop produces $V_{OUT}=1000V_{OS}$. (V_{CM} is the common-mode voltage, and V_{OS} is the op amp's input offset voltage.) By opening and closing S_1 and S_2, you can measure the op amp's input-bias and offset currents, and by varying V_{CM}, you can measure the op amp's sensitivity to common-mode voltage **(Ref 1)**.

Frequency roll-off stabilizes op amps

The op-amp device under test (DUT) behaves well in this test circuit because the DUT and the feedback integrator (IC_2) have open-loop gains that decrease

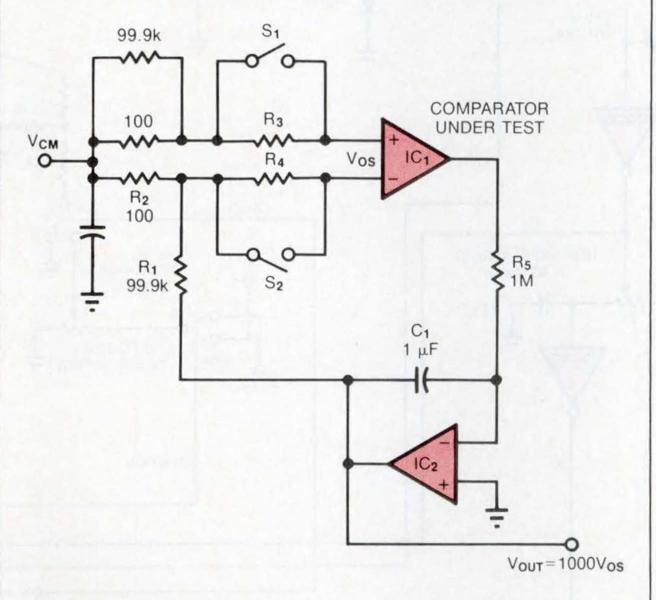


***Fig 1—The conventional op-amp test circuit** lets you measure V_{OS}, I_B, and I_{OS}. By varying V_{CM}, you can measure these parameters' sensitivity to common-mode voltage.*

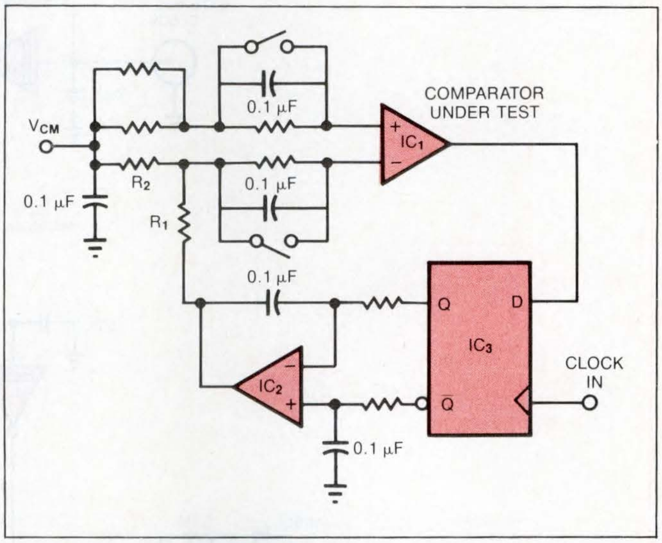


***Fig 2—To test a comparator, modify the Fig 1** op-amp test setup by adding a flip-flop (IC_3) and by substituting a differential integrator (IC_2) for the single-ended one.*

with increasing frequency. As a result, any oscillations in the circuit have amplitudes inversely proportional to their frequency, and the R_1/R_2 divider further attenuates these amplitudes below the level of concern.

When you install a comparator in the op-amp loop, however, the comparator's relatively large high-frequency gain sustains large-amplitude oscillations at the comparator's output. Internal rectification of this ac signal can shift the dc bias voltages within the comparator, and large dc shifts can momentarily bias the comparator off. The loop relaxes, then resumes oscillation, creating repetitive bursts of high-frequency oscillation called "squegging."

Another, more subtle problem involves IC_2. An integrator can attenuate high frequencies if its output impedance remains low, but the integrator op amp's output impedance increases with frequencies above approximately 50 kHz. Accordingly, the integrator's attenuation falls off for oscillations above that frequency level. Above 1 MHz in particular, most op amps have little gain—but comparators have plenty. The comparator is thus, unfortunately, able to amplify any oscillations present. Moreover, the comparator's high slew rate helps to ensure that its output signal will slam from rail to rail.

Comparators must switch but not oscillate

An adaptation of the classic delta-sigma modulator solves this oscillation problem **(Fig 2)**. The comparator's output feeds a D-type flip-flop (IC_3) that you drive with a clock signal in the 100-kHz to 1-MHz range. In turn, the flip-flop drives a differential integrator (IC_2), whose output voltage is attenuated by R_1/R_2 as in **Fig 1**. Equilibrium in this feedback loop demands that the comparator-output signal have a 50% duty cycle, which in turn produces a voltage at the R_1-R_2 junction equal to the comparator's V_{OS}. The flip-flop in this circuit provides excellent attenuation of high frequencies yet contributes little phase shift at moderate frequencies.

Some comparators will oscillate when tested in the **Fig 2** circuit, but the loop still forces the output to switch with a precise 50% duty cycle, which by definition implies that the input voltage equals V_{OS} (that is, the comparator's switching threshold). You measure the comparator's other dc parameters by controlling S_1, S_2, and V_{CM} as in **Fig 1**.

Fig 3 shows a practical comparator tester. Based on

Text continued on pg 129

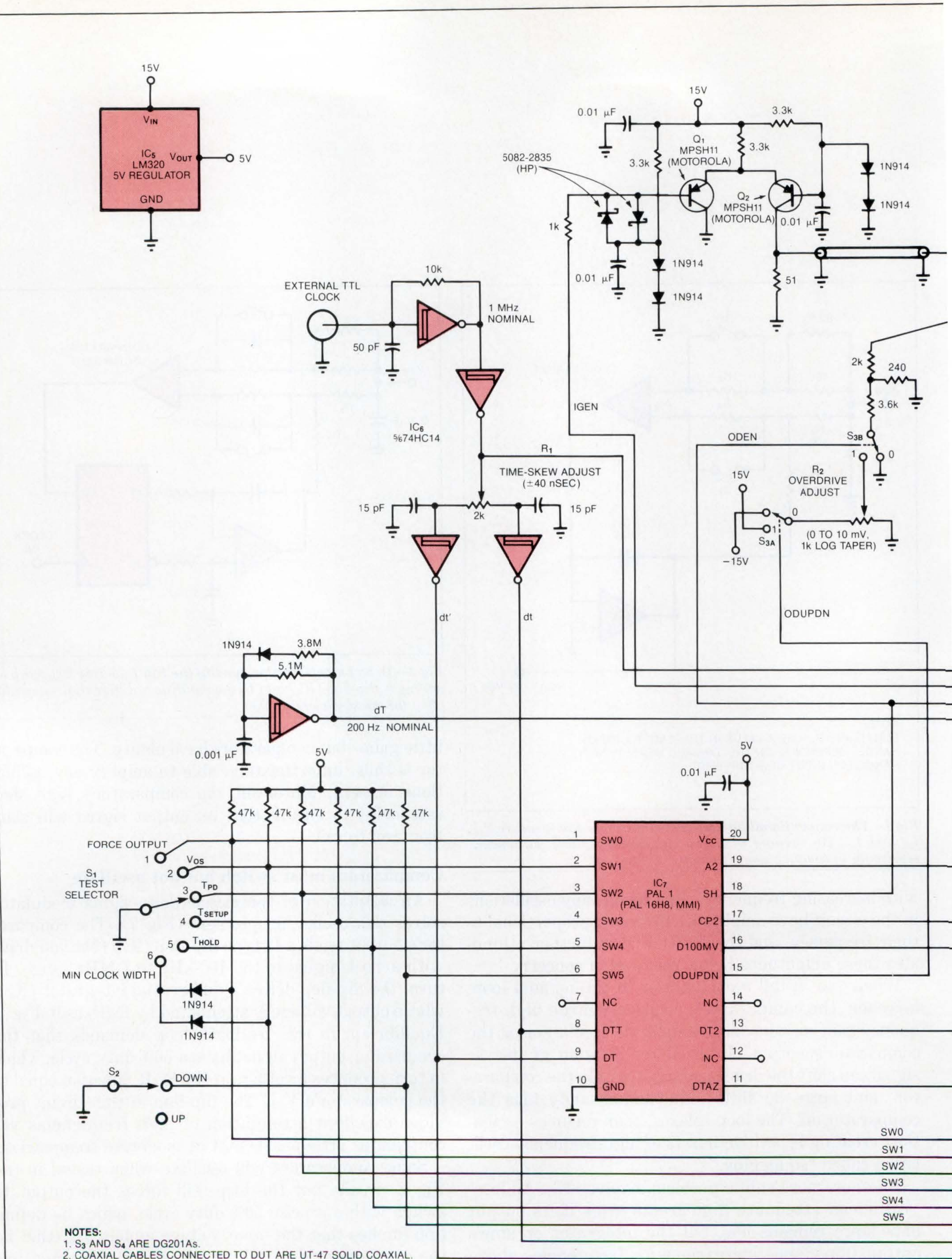
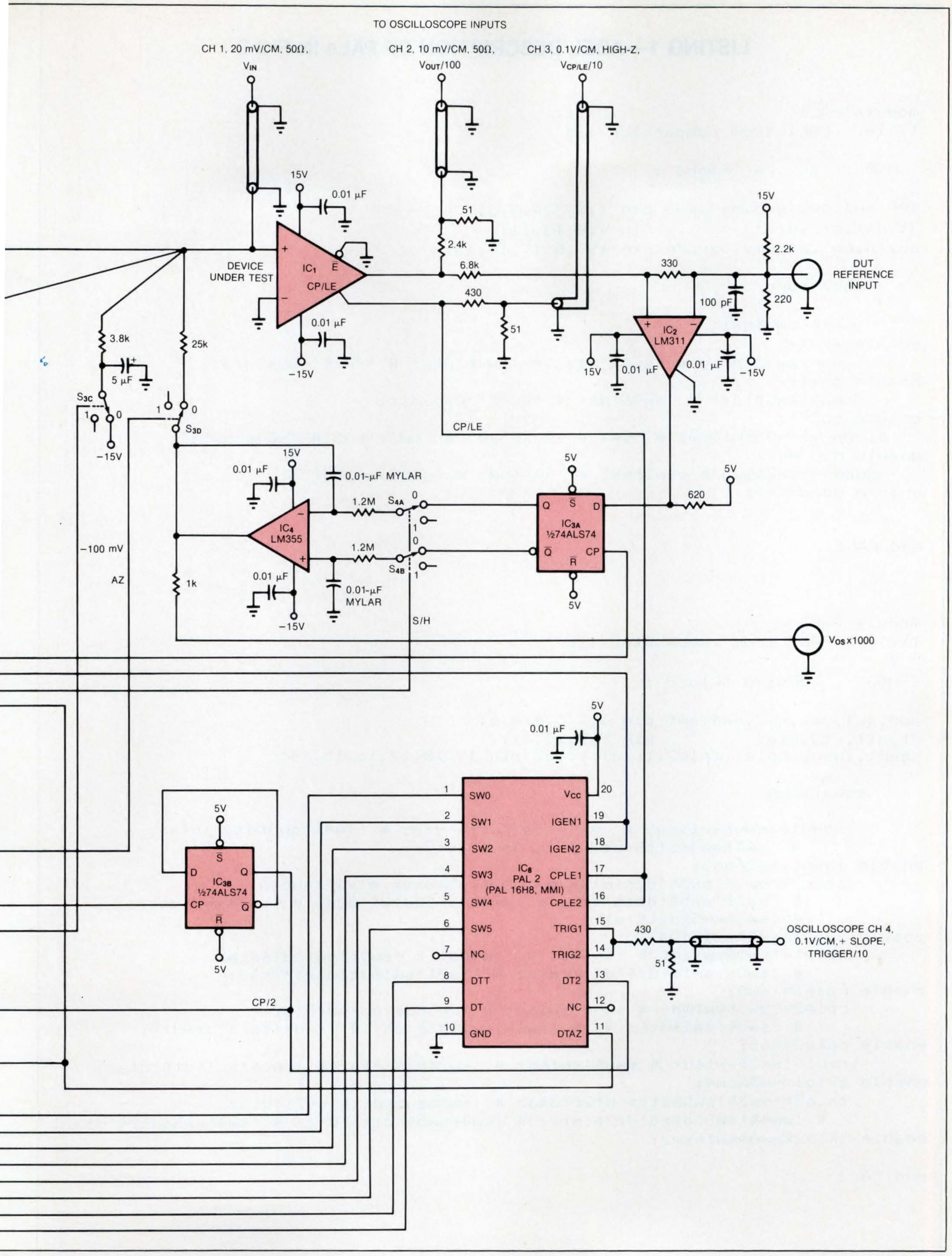


***Fig 3—This comparator-test circuit incorporates** the basic loop of **Fig 2**, but uses two programmable-array logic chips (IC_7 and IC_8) for sequencing the tests.*



TO OSCILLOSCOPE INPUTS
CH 1, 20 mV/CM, 50Ω,
CH 2, 10 mV/CM, 50Ω,
CH 3, 0.1V/CM, HIGH-Z,
VIN
VOUT/100
VCP/LE/10
15V
0.01 μF
51
2.4k
6.8k
430
330
2.2k
220
100 pF
DUT
REFERENCE
INPUT
DEVICE
UNDER TEST
IC1
CP/LE
IC2
LM311
3.8k
25k
5 μF
S3C
S3D
−15V
CP/LE
0.01-μF MYLAR
1.2M
S4A
S4B
IC4
LM355
IC3A
½74ALS74
620
5V
−100 mV
AZ
1k
S/H
VOS×1000
IC3B
½74ALS74
CP/2
IC8
PAL 2
(PAL 16H8, MMI)
SW0
SW1
SW2
SW3
SW4
SW5
NC
DTT
DT
GND
VCC
IGEN1
IGEN2
CPLE1
CPLE2
TRIG1
TRIG2
DT2
DTAZ
OSCILLOSCOPE CH 4,
0.1V/CM, + SLOPE,
TRIGGER/10

LISTING 1—ABEL DESCRIPTION OF PALs IN FIG 3

```
module PAL1
title    PAL1 from comparator jig'

   U08     device 'P16H8';

sw0,sw1,sw2,sw3,sw4,sw5 pin 1,2,3,4,5,6;
dt,dtt,dt2,dtaz         pin 9,8,13,11;
az,sh,cp2,d100mv,odupdn pin 19,18,17,16,15;

      equations

         az=!sw0&sw1;
enable az=1;
         sh=!sw2&!dtaz # !sw3&!dtaz # !sw4&!dtaz # !sw0&!sw1&!dtaz;
enable sh=1;
        cp2=!sw3&!dtt # !sw4&!dtt # !sw0&!sw1&!dtt;
enable cp2=1;
    d100mv=!sw0&sw1&sw5 # !sw1 # !sw2&!sw5 # !sw3&!sw5 # !sw4&!sw5;
enable d100mv=1;
    odupdn=!sw2&sw5 # !sw3&sw5 # !sw4&sw5 # !sw0&!sw1&dt2;
enable odupdn=1;


end PAL1



module PAL2
title   'PAL2 from comparator jig'

   H08      device 'P16H8';

sw0,sw1,sw2,sw3,sw4,sw5 pin 1,2,3,4,5,6;
dt,dtt,dt2,dtaz         pin 9,8,13,11;
igen1,igen2,cple1,cple2,trig1,trig2 pin 19,18,17,16,15,14;

      equations

         igen1=!sw0&sw1&sw5 # !sw4&!sw5&dtt&!dtaz # !sw4&!sw5&dt2&!dtaz
              # !sw4&sw5&dtt&!dt2 # !sw4&sw5&dtaz;
enable igen1=sw2&sw3;
         igen2=!sw2&!sw5&!dt&!dtaz # !sw2&sw5&dtaz #!sw2&sw5&dt
              # !sw3&!sw5&!dtt&!dtaz # !sw3&!sw5&dt2&!dtaz # !sw3&sw5&dtaz
              # !sw3&sw5&dtt&!dt2;
enable igen2=sw0&sw1&sw4;
         cple1=!sw0&sw1&dt # !sw3&dt # !sw4&dt # !sw0&!sw1&dt&dtaz
              # !sw0&!sw1&!dt&!dtt&!dtaz # !sw0&!sw1&dt&dtt&!dtaz;
enable cple1=!sw5;
         cple2=!sw0&sw1&dt # sw0&!sw1&dt # !sw3&dt # !sw4&!dt
              # !sw0&!sw1&dt&dtaz # !sw0&!sw1&dt&!dtt # !sw0&!sw1&!dt&dtt;
enable cple2=sw5;
       trig1=!sw0&sw1&dt # sw0&!sw1&dt # !sw2&dt&!dtaz # !sw0&!sw1&dt&!dtaz;
enable trig1=sw3&sw4;
         trig2=!sw3&!sw5&dtt&!dt2&!dtaz # !sw3&sw5&dtt&!dt2&!dtaz
           # !sw4&!sw5&dtt&!dt2&!dtaz # !sw4&sw5&!dtt&!dtaz # !sw4&sw5&dt2&!dtaz;
enable trig2=sw0&sw1&sw2;

end PAL2
```

IC_7 and IC_8 take the place of 10 or more MSI chips, and these PALs provide better-synchronized timing waveforms as well.

Fig 2's test setup, this circuit is capable of measuring the ac and dc parameters of most comparators. S_1 is the main control switch and selects among six positions. Position 1 forces the DUT output high or low according to the position of the up/down switch S_2. Position 2 causes the integrator's (IC_4's) output to assume a value 1000× that of the DUT's V_{OS}. Position 3 configures the tester for measurement of the DUT's propagation delay (after you set the desired input overdrive using potentiometer R_2). Positions 4, 5, and 6 set up the tester for measurements of setup time, hold time, and minimum pulse duration, respectively.

Tester includes square-wave generator

The transistors (Q_1 and Q_2) and associated components form a squaring circuit that presents the DUT input with a ±100-mV square-wave signal. This signal features the 300-MHz bandwidth and 3-nsec rise times necessary for satisfactory comparator testing. When the circuit measures propagation delay (S_1 in position 3), switch S_2 selects the desired signal polarity by shifting the square wave in the positive or negative direction.

You set the desired overdrive voltage by adjusting R_2. The test circuit's nulling mechanism ensures that the circuit will apply this overdrive with respect to a voltage level that includes the DUT's V_{OS} plus any offset error in the input-signal amplitude. **Fig 4** shows the resulting waveforms (from a measurement of propagation delay for Elantec's EL2018 comparator).

IC_7 and IC_8, programmable-array logic (PAL) chips, perform the test-sequencing and autozeroing functions for the DUT. They take the place of the otherwise required 10 or more MSI chips, and they provide better-synchronized timing waveforms as well. **Listing 1** describes the PALs' logic in terms of the Abel fuse-compiler inputs. When you test a strobed comparator, potentiometer R_1 lets you adjust the clock edge with respect to the input edge by manually introducing a controlled amount of time skew via the PALs.

This practical tester not only lets you measure a comparator's performance, but also helps plot a comparator's transfer function. By applying an external ramp voltage at the DUT Reference Input, you can sweep the voltage to which the DUT output is autozeroed (the autozero operation occurs 200 times/sec). You connect this ramp signal for display on the scope's vertical axis and the tester's $V_{OS}\times1000$ signal for display on the scope's horizontal axis. The resulting plots of input vs output **(Fig 5)** are the transfer functions for the EL2019 comparator (clocked mode) and the EL2018 comparator (unclocked mode).

Ground plane provides low impedance

Careful layout and construction are essential attributes of any useful tester board. The board should have a copper ground plane, for example, to provide low resistance and inductance at the comparator's ground pin. (A low-impedance ground helps sink the large pulses of supply current that occur when the compara-

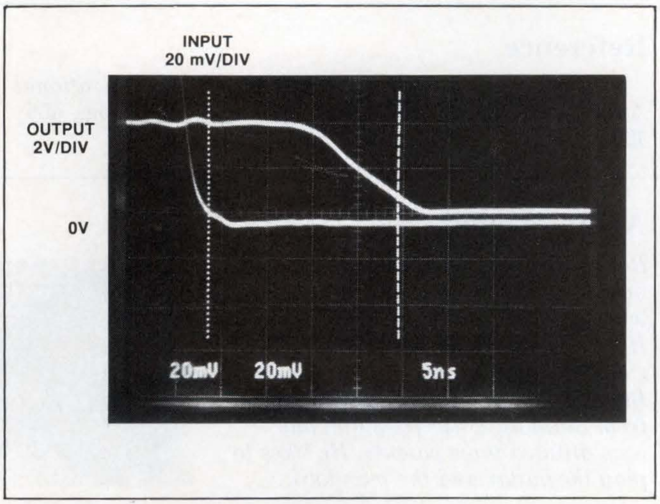


***Fig 4—This scope photo shows the propagation delay** for an EL2018 comparator by displaying the output waveforms (attenuated by a factor of 100) and the input waveforms. **Fig 3** shows the actual test setup.*

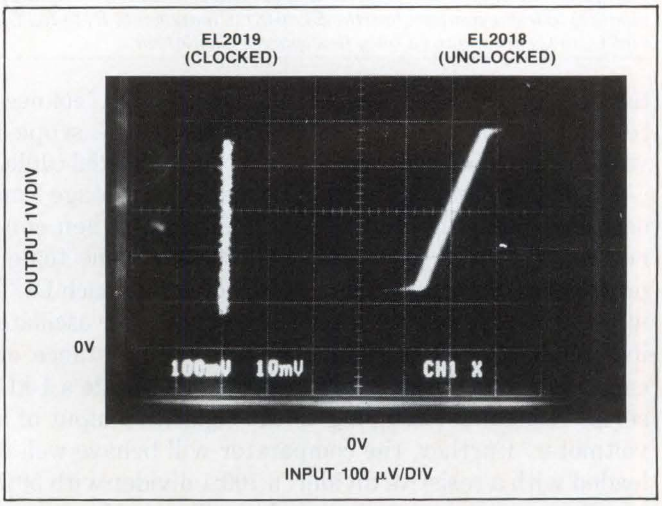


***Fig 5—This double-exposure photo shows the transfer functions** for the EL2019 comparator (while its internal master-slave flip-flop is being clocked) and the EL2018 comparator (while its internal latch is being held in the transparent, or unclocked position).*

A comparator's wideband input stage can oscillate by itself when connected to a large resistance or inductance (exclusive of feedback).

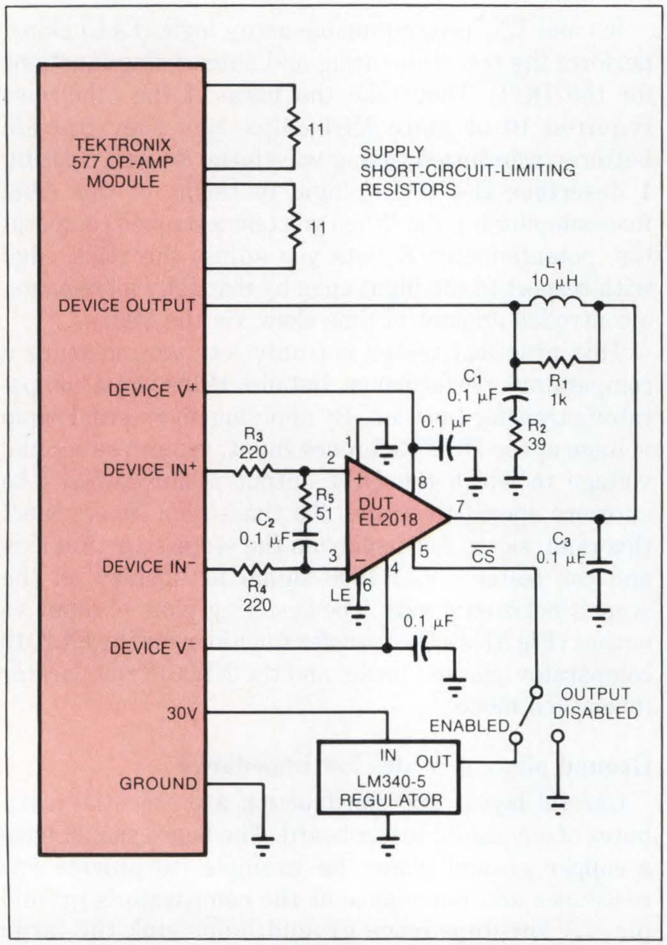


Fig 6—This test circuit shows the brute-force methods necessary to modify an op-amp tester (Tektronix's 577 curve tracer with op-amp module) to test a comparator (the EL2018). Components R_1 to R_5, L_1, and C_1 to C_3 are required only to suppress oscillation.

tor's output switches.) You should include BNC connectors on the board that mate directly to the scope's vertical amplifier without any intervening coaxial cable.

Because a comparator's wideband input stage can oscillate by itself (exclusive of feedback) when connected to a large resistance or inductance, the tester provides a source impedance of 50Ω or less at each DUT input. A comparator's output stage, too, can oscillate independently when connected to a low-resistance or capacitive load. Accordingly, you should provide a 1-kΩ series resistor for coupling to the capacitive input of a voltmeter. Further, the comparator will behave well if loaded with a resistive divider; a 100:1 divider with 50Ω junction resistance, for example, will provide a good interface to the oscilloscope.

If you have no choice but to test your comparator using an existing op-amp test setup, you'll have to add circuit components to prevent the oscillations from disrupting the tests. **Fig 6** is an example of the measures taken to test an EL2018 comparator using the op-amp adapter for Tektronix's Model 577 curve tracer. (The adapter employs the basic test circuit of **Fig 1**.)

First, you should minimize the oscillation caused by the magnetic coupling between wires by replacing the op-amp module's socket adapter with a simple multiple-insertion socket. Some oscillation may remain at various levels on the comparator's transfer curve (the EL2018 has a gain of 10^4 at 3 MHz), but the smaller socket minimizes this problem. The L_1/R_1 series network and the C_1/R_2 shunt network reduce the magnitude of the oscillations sent to the test system, and R_3, R_4, R_5, and C_2 reduce these amplitudes still further. Finally, capacitor C_3 eliminates any residual oscillation.

The resulting setup isn't elegant, but it works because it doesn't interfere with the test circuit's dc parameters. Some comparators, however, might have a problem driving the load capacitor C_3; comparators with asymmetrical output stages can induce an input offset by rectifying existing oscillation. To be sure this offset rectification doesn't happen, you must compare your results with those from a tester that can't sustain such oscillations (**Fig 3**). **EDN**

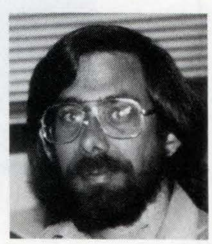
Acknowledgment

The author would like to thank Peter Ohlon for selecting the components for **Fig 6**.

Reference

1. Tobey, G E, J G Graeme, L O Huelsman, *Operational Amplifiers*, McGraw-Hill, New York, NY, 1971, pgs 456-460.

Author's biography



Barry Harvey is a senior design engineer for Elantec Inc in Milpitas, CA, where he designs integrated circuits. His previous employers include Precision Monolithics, AMD, and Siliconix. Barry holds BSEE and MSEE degrees from Stanford University and has been granted three patents. He likes to play the guitar and the mandolin.

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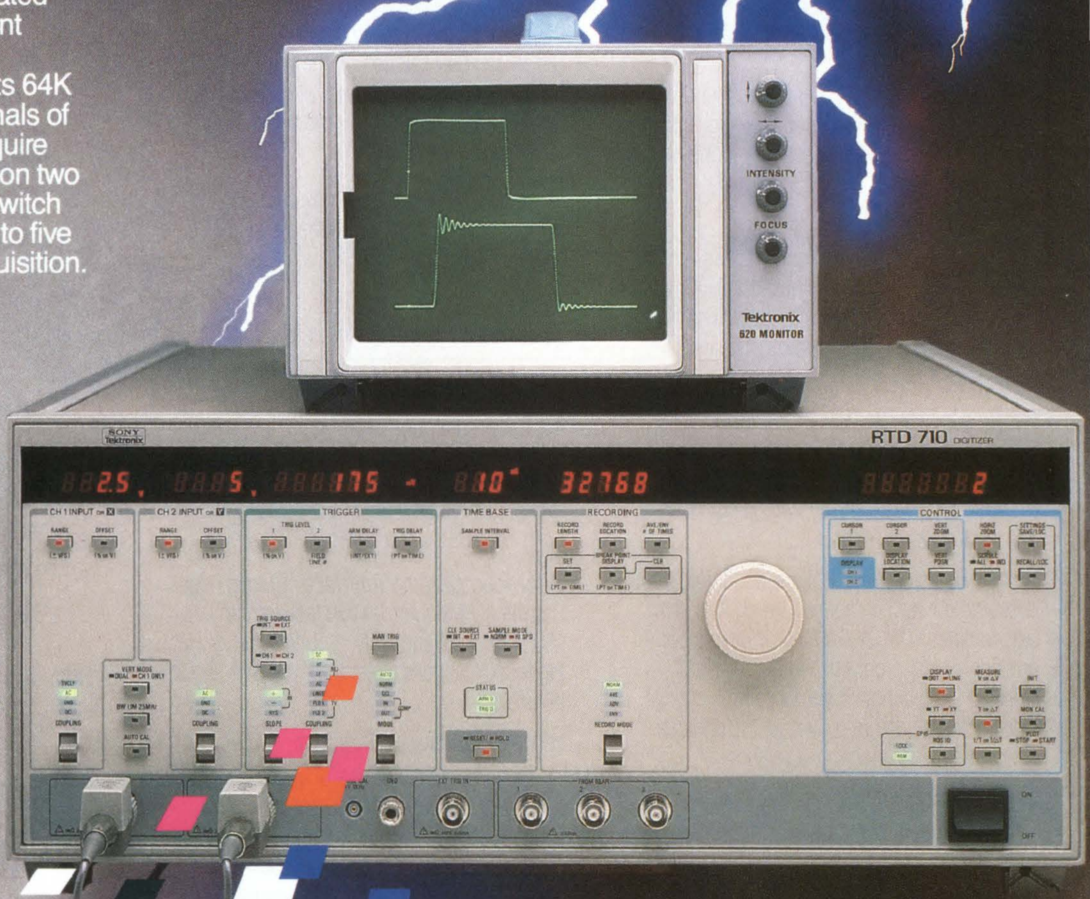

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Cluster testing overcomes many testability problems

Complete in-circuit testing of dense pc boards may not be possible, either because vital nodes are inaccessible, or because VLSI chips can be damaged by overdriving. You can both avoid these problems and gain some of the advantages of functional testing by testing several ICs as a group.

Stephen Caplow, *Teradyne Inc*

In the perfect world of the design engineer's dreams, designed-in testability carries every new VLSI circuit board smoothly and swiftly from design through test, and on to market. In the real world, however, test engineers still spend weeks and sometimes months trying to overcome the testability problems posed by many new board designs. These testability problems fall into three main categories: the difficulty of programming functional tests that will fully exercise a complex board; the inaccessibility of vital nodes; and the probability of causing damage to sensitive VLSI chips by overdriving them during in-circuit testing of neighboring ICs.

You can avoid these problems by using a relatively new technique called cluster testing, in which you test several ICs as a group. You can choose the group boundaries so that overdrive damage won't occur, and you can detect timing and other functional problems while incurring only a slight increase in programming complexity. Cluster testing, therefore, combines features of both in-circuit and functional testing.

Today's VLSI boards mix custom or semicustom ICs with off-the-shelf components, surface-mount devices with conventional through-hole devices, and high-power logic such as the advanced Schottky families with extremely low-power CMOS families. The same advanced device and packaging technologies that let you crowd more performance into less board space, however, also make it less likely that a purely in-circuit testing program will provide adequate fault coverage on a new board. At the same time, purely functional tests, which avoid many of the problems associated with in-circuit testing, require such a large programming effort that the costs are unacceptable (see **box**, "Functional vs in-circuit testing of pc boards.")

Gaining access to untestable components

The commonest barriers to in-circuit testing are devices that automatic test equipment (ATE) can't physically access, and devices that the ATE can't safely or reliably overdrive. Inaccessible ICs are themselves untestable by purely in-circuit techniques; devices that can't tolerate overdriving make their neighboring components untestable. In-circuit testing can't be fully effective if the ATE can't reach all of a board's internal nodes.

Surface-mount technology (SMT) accounts for many

In-circuit testing can't always probe all of a board's internal nodes. You can often reach inaccessible devices by making them part of a cluster.

accessibility problems. The narrow lead spacing of most SMT devices, and the practice of mounting these devices on both sides of a board to achieve greater densities, make it difficult (and sometimes impossible) for the ATE to probe internal nodes. Specialized, dual-sided test fixtures can help to some extent, but there are many boards to which even these fixtures can't provide sufficient nodal access for a complete test. Piggyback modules (sometimes called rider cards) that mount on a mother board can also create access problems.

When you find ICs that the ATE probes can't reach, you can group two or more of the ICs and test them functionally as a single entity or a cluster. The ATE must still overdrive other components in order to isolate the cluster, but it need not have direct contact with every IC in the cluster. For example, you might pair one component, whose narrowly spaced leads prohibit physical probing, with a neighboring component whose leads permit probing. You can then test the troublesome component indirectly through the leads of the accessible component. Similarly, in a logic chain consisting of components A, B, and C, if you can't safely overdrive component B in order to test component C, you could cluster B and C and test them as a unit (provided that A can safely be overdriven).

You'll find that many of the new device-fabrication technologies place severe restrictions on overdriving the devices. For example, many programmable-array-logic (PAL) devices oscillate if you overdrive the outputs from logical zero to logical one because of positive feedback in the output stages. Unless a PAL has built-in features that let you disable its outputs or preset them to logical one, the oscillation will propagate to all devices that fan out from the PAL and will interfere with the test signals that the ATE applies to these devices. Consequently, in-circuit testing can't achieve repeatable results from the ICs that fan out from the PAL.

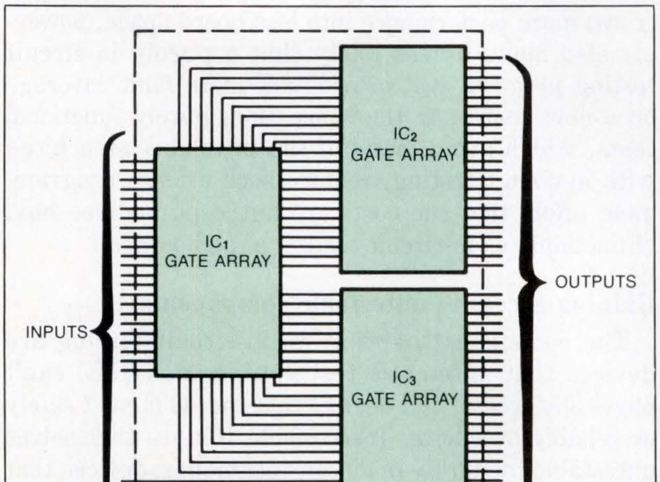


Fig 1—You can't perform in-circuit tests of either IC_2 or IC_3 in this circuit, *because overdriving so many outputs of IC_1 would overheat and damage IC_1.*

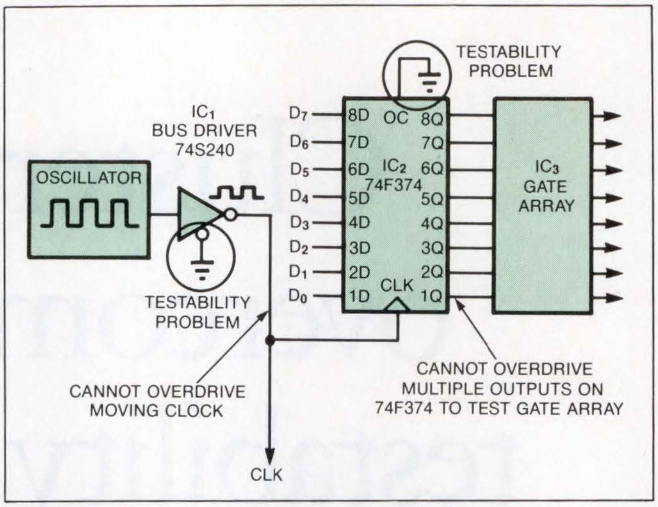


Fig 2—This circuit is untestable by in-circuit means. *You can't turn off the clock to test IC_2, nor can you turn off the outputs of IC_2 to test IC_3. Trying to overdrive a clock signal produces unrepeatable results; overdriving multiple outputs of IC_2 would damage it.*

You'll also have to take into account the possibility that overdriving many outputs of a device—or overdriving a few outputs for a long time—may damage the device. Large gate arrays that have a high pin count **(Fig 1)** are particularly susceptible to damage. Because so many of IC_1's output leads drive IC_2 and IC_3, the ATE can't safely overdrive either of the latter two; the cumulative overdrive current would almost certainly damage IC_1. Similarly, devices in high-power logic families, such as Fast and advanced Schottky, can't tolerate the overdriving of more than a few outputs; the overdrive currents applied to the various output pins all flow through the same ground-bonding wire, and an excessive total current can melt this wire.

Extremely long in-circuit tests can also make overdriving unsafe. For example, a large RAM chip might require thousands of test patterns for a full check of every cell. The industry-standard "6n march" test, applied to such a chip, might take hundreds of milliseconds, and subjecting the RAM's associated controller to overdrive currents for that length of time could damage the controller.

You'll often find that several different factors combine to make a device or group of devices virtually untestable by in-circuit methods. Consider the problems associated with testing the 74F374 8-bit latch (IC_2) and the gate array (IC_3) in **Fig 2**'s circuit. First, you need to isolate the clock input in order to apply single, carefully controlled clock pulses. You can't turn the clock off, however, because the output-enable terminal of bus driver IC_1 is wired directly to ground.

Second, it's not practical to overdrive the clock signal; wiring inductance gives rise to glitches whenever you try to overdrive moving signals such as those produced by clocks, delay lines, and unbreakable feedback loops. Furthermore, you need to apply very high currents (more than 700 mA) to overdrive the outputs of 74S240 and similar bus drivers; even if the driver escaped damage, your results would be unreliable. Thus, you have no safe or reliable means of isolating the clock input while testing IC_2.

Third, you can't isolate the gate array for an in-circuit test because the output-enable terminal of IC_2, OC, is also wired directly to ground. To test IC_3, you have to overdrive all eight of its output terminals while applying potentially thousands of patterns to test the gate array. Such a procedure is almost guaranteed to destroy the 74F374, either by melting common internal

Functional vs in-circuit testing of pc boards

The two most common methods of testing complete pc boards are functional testing and in-circuit testing. When it performs functional testing, automatic test equipment (ATE) emulates the system in which a board will be used, and accesses the board via the edge connectors. You program the ATE either to generate test patterns that will detect specific types of faults, or to exercise the board as it will operate in the system it's designed for.

Functional testing can detect timing problems and faults caused by interaction among board components, and it produces quick results with simple boards. The disadvantage of functional testing is that it can't isolate the fault to a particular component, so diagnosis requires time-consuming manual or computer-aided guided-probe signal-tracing techniques. Also, as board complexity increases, you'll find it becomes increasingly difficult and time consuming to create test programs that exercise all the board's functions.

ATE that uses the in-circuit approach accesses each digital IC individually by means of the probes in a bed-of-nails test fixture that's made specifically for testing a particular board. To test an IC, the ATE activates the probes that correspond to the IC's terminals, forcing the device inputs to particular logic states while observing the outputs. This forcing operation is called "overdriving" or "backdriving" because it overrides the outputs of any previous ICs in the logic path. To minimize the effects of stray capacitance, you can obtain a bilevel fixture, which has some taller, spring-loaded probes. At the first level, a partial vacuum pulls the board down only onto the taller probes; at the second level, a full vacuum pulls the board down onto all of the probes, compressing the springs of the taller ones.

The advantage of the in-circuit method is that it can make test-equipment programming a highly automated process—you merely extract from a library the standard test patterns for the devices on the board, and combine these patterns into a sequence that will test every IC on the board. The method is simple and inexpensive. Because the ATE produces a go/no-go report for each device, it's also easy to diagnose and replace a failing IC.

One disadvantage of the in-circuit method is that it depends on the accessibility of all significant nodes. In modern, high-density boards, and particularly in those having surface-mount components on both sides, all the significant nodes aren't always accessible.

Two potentially more serious disadvantages are that the in-circuit method can't easily detect timing errors, particularly in complex VLSI devices, and that some devices can be damaged by the large currents (>500 mA) needed to overdrive their outputs to test a neighboring device.

Inaccessibility isn't the only problem associated with in-circuit tests: The large currents needed to overdrive a device's output can damage the device.

ground leads or by the cumulative overheating. There are no easy solutions to this problem—this circuit is a conspicuous example of designing for untestability!

Constrained VLSI components, so called because they have pins that are tied to one another or tied directly to ground or V_{CC}, constitute yet another barrier to testability. You may be able to force an in-circuit test on a device of this kind by manually writing special test patterns, but many designs stubbornly resist the purely in-circuit approach.

The UART shown in **Fig 3** is an example of a constrained device: Two of its pins are tied together through an inverter. Although there is no hard connection between the pins, or between either of the pins and ground or V_{CC}, the connection through the inverter constitutes an unbreakable feedback loop that restricts the ATE's ability to perform a useful test. For example, if the test sequence includes patterns that drive both the input and the output of the inverter simultaneously, the result can be glitches that produce unrepeatable test results.

Some test nodes on a board may have sensitivities that don't allow in-circuit testing of the associated components. **Fig 4** shows an ECL gate (IC_1) that controls the clock line of an edge-sensitive ECL counter (IC_2). ECL counters require very fast signal transitions to avoid false clocking—in fact, no ATE could clock the counter fast enough through tester pin B to produce repeatable results, because the stray capacitance introduced by the gate and the probe lead would distort the waveform. However, by defining a small cluster that includes IC_1, IC_2, and the previous gate (not shown), you can apply your test clock signal through tester pin A to the ECL gate. The transition at the output of the gate is then undistorted, and it clocks the counter reliably to produce repeatable test results.

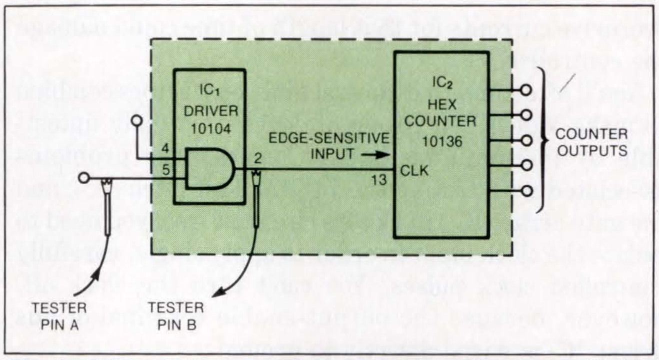


Fig 4—ECL counters must have very fast edges *to avoid false triggering. No tester could produce a fast enough edge by overdriving IC_1 (via test probe B) because of the stray capacitance added by the probe. You can test the two ICs as a cluster via test probe A, however.*

Certain analog nodes are also sensitive to stray capacitance. For example, if you apply a test probe to the summing junction of the op amp in **Fig 5,** the circuit will oscillate, thereby precluding any reliable in-circuit test of the D/A converter that feeds the summing junction. A bilevel fixture would allow you to perform an in-circuit test of the op amp alone, forcing it to behave as a simple comparator. To test the D/A converter, however, you'd have to withdraw the probe from the summing junction and perform a cluster test. Unless many other circuits on the board require the use of a bilevel fixture, which is expensive, this procedure would be uneconomical. It would be more practical to specify a functional cluster test of the D/A converter and the op amp together, right from the start.

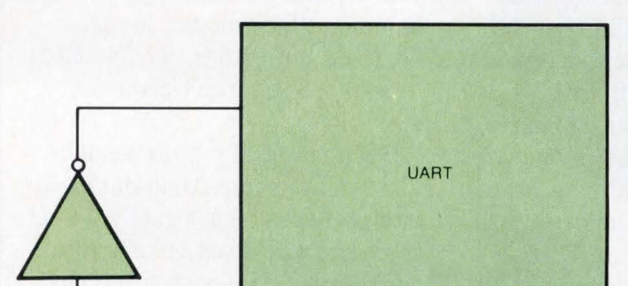


Fig 3—In this configuration, the inverter establishes an unbreakable feedback loop *between two pins of the UART. Test patterns that drive both these pins simultaneously would produce glitches and unrepeatable results.*

Some components are invisible to the tester

Analog circuits, such as disk interfaces, often contain small capacitors and inductors configured in a way that makes them invisible to the tester—no in-circuit test can detect the presence or absence of these invisible components. For example, in the tank circuit in **Fig 6,** the inductor's impedance, at 10 kHz, is 275,000 times lower than the capacitor's impedance. The capacitor, therefore, is invisible to the tester, and the only way to verify the presence or absence of the correct capacitance value is to measure the frequency response of the whole circuit.

Some board malfunctions are caused by complex interactions among several devices on the board, or by marginal drive and timing faults. Even very-high-performance ATE systems may be unable to detect such

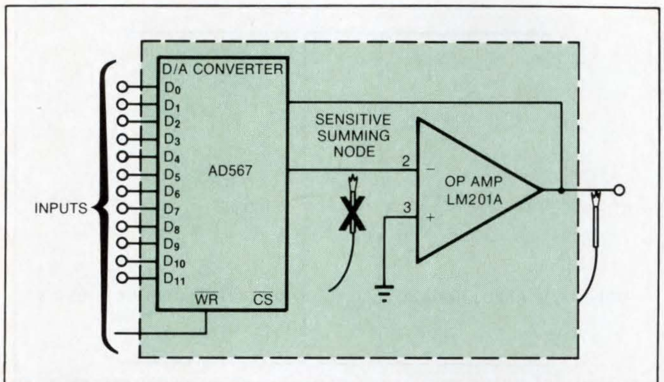


Fig 5—In this circuit, you can't test the op amp in its linear region *because capacitance added to the summing junction by the probe will make the op amp oscillate. You can test the D/A converter and the op amp as a cluster, though.*

faults, which can also be very difficult to diagnose at a later stage of testing. The most cost-effective way to detect such faults during production testing is to add some functional cluster tests to the in-circuit test program. These tests allow an in-circuit testing program to detect timing faults of 30 nsec or less.

The best way to define a cluster is to start with the components that are creating a testability problem, and work outward, adding neighboring components to the cluster until you've defined a functional block. This guideline may lead you to include more components than are strictly necessary for buffering the troublesome device, but it's usually easier to generate effective test patterns for a functional block than for a random collection of logic elements.

Another useful guideline is that, to obtain the best performance from the ATE, you should access the cluster at nodes that don't require overdriving, such as 3-state buses. You'll probably find it easy to implement cluster tests for bus-structured boards because the address and data buses form natural boundaries for most clusters.

Clusters can have as few as two components. Small clusters require little programming effort because they often allow you to use patterns from the in-circuit pattern library. Larger clusters demand more-traditional functional-test programming techniques. Nevertheless, even for a large number of clusters, the programming effort is still much smaller than that for a full functional test of a complete board.

A logic simulator can be a powerful aid in generating functional-test programs. A simulator models a circuit in software and predicts the circuit's responses, node by node, to a set of test stimuli. Today's advanced simulators provide an array of software tools that improve programming speed and program quality; their features include good-circuit simulation, current-strength analysis, worst-case timing analysis, fault simulation, and automatic-test-pattern-generation (ATPG) programs.

To simulate a cluster, you must first create a circuit description of it. You can extract the details pertaining to your cluster from the database previously created by your CAE/CAD system for the in-circuit test of the full board. The task will be easier and quicker if you have access to a model compiler that provides high-level editing tools. You'll have to extract details for each of the clusters that you define, so you'll end up with several circuit-description files for the board: one file for the complete board, and one file for each cluster that you define for testing purposes.

Once you've compiled your cluster circuit description into a simulation model, you'll need to generate the test patterns that the simulator will use to test the model. ATPG software can help you in this task, although its effectiveness decreases as the circuit's sequential depth increases. For this reason, you'll probably have to generate test patterns manually for very complex clusters—a time-consuming chore, but part of the price you must pay for getting an otherwise untestable board into production.

The simulator applies your functional-test patterns to the cluster model and predicts the model's responses both for a go/no-go test and for guided-probe diagnostics. This stimulus/response information provides the description of a "good cluster," against which your test system will later compare the responses of the corresponding physical cluster.

You'll probably follow good-cluster simulation with a fault-simulation run in which the simulator injects the logical equivalent of physical defects into the model and predicts their effect on circuit performance. The fault simulation grades the fault coverage provided by your set of test patterns, indicating which faults they detect and which faults they miss. You can also use fault-simulation data to generate a database to serve as the basis for fault-dictionary diagnostic routines. When the ATE detects a fault, but accessibility problems prevent detailed diagnosis of the components involved, the fault dictionary can lead you to routines that will help to isolate the faulty component.

Finally, postprocessing software converts the simulator's output files to the format required by the ATE; you can download the files to the ATE and merge them

Trying to overdrive moving signals, such as clock pulses, produces glitches that yield unrepeatable test results.

with the in-circuit test program for debugging. This transfer task is easier if the simulator and the ATE share a common language and operating environment. In addition, the simulator should be able to take into account the characteristics and limitations of the test system; this way, the simulator will provide only those test patterns that the ATE is able to execute.

Boards that form part of a μP-based system lend themselves to a programming process called bus-cycle emulation, which can be simpler than simulation. From the standpoint of programming and signal quality, these boards' address and data buses form ideal cluster boundaries.

In bus-cycle emulation, you put the μP on hold and use the test system's channels to emulate microprocessor cycles. The ATE can then use simple read and write cycles to test any board function independently. If the ATE has the specialized hardware needed for inserting the variable-length wait states that peripherals such as RAM-refresh controllers require, you need only enter the μP's specified timing characteristics to automatically generate the appropriate bus-cycle tests for each cluster.

By itself, bus-cycle emulation provides neither the stimulus/response data nor the test-pattern grading that you obtain from simulation. However, some test systems have tools that automatically learn the correct nodal responses for both go/no-go tests and guided-probe diagnostic routines. In addition, you can use the ATE's high-current drivers to physically inject stuck-at-one and stuck-at-zero faults into the board, and you can thereby measure a test program's fault coverage at the pin level.

Techniques for diagnosing cluster failures

You have several options for troubleshooting clusters that fail. For the very simplest cluster, consisting of two or three components, a rule-based expert system for in-circuit failure analysis may be sufficient. The expert system begins its analysis only after the ATE has completed all the in-circuit and simple cluster tests, and it's specifically designed to take into account the fact that a single fault may cause several different in-circuit device tests to fail. The expert system applies a series of rules to the failing-pin information to eliminate spurious failures that were merely products of the primary failure; thus, it isolates the faulty component.

For more complex and populous clusters, you'll need guided-probe analysis, a fault dictionary, or a combination of these two techniques. Integrating the fault-dictionary and guided-probe techniques provides the greatest diagnostic efficiency because it capitalizes on the respective strengths of each approach. The fault dictionary's fast initial identification of likely fault locations lets the guided probe proceed directly to those areas to verify the source of the failure, instead of painstakingly tracing backward from a failed cluster output.

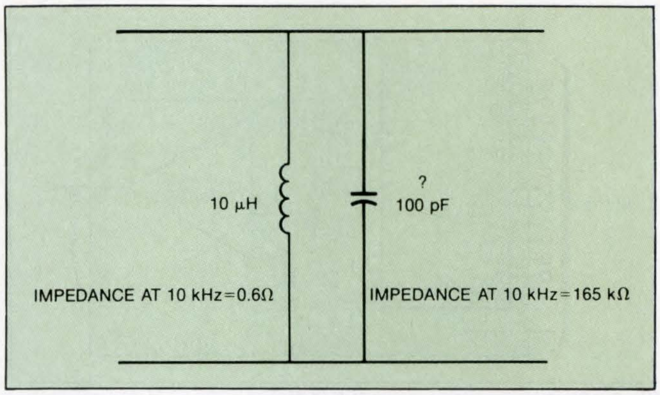


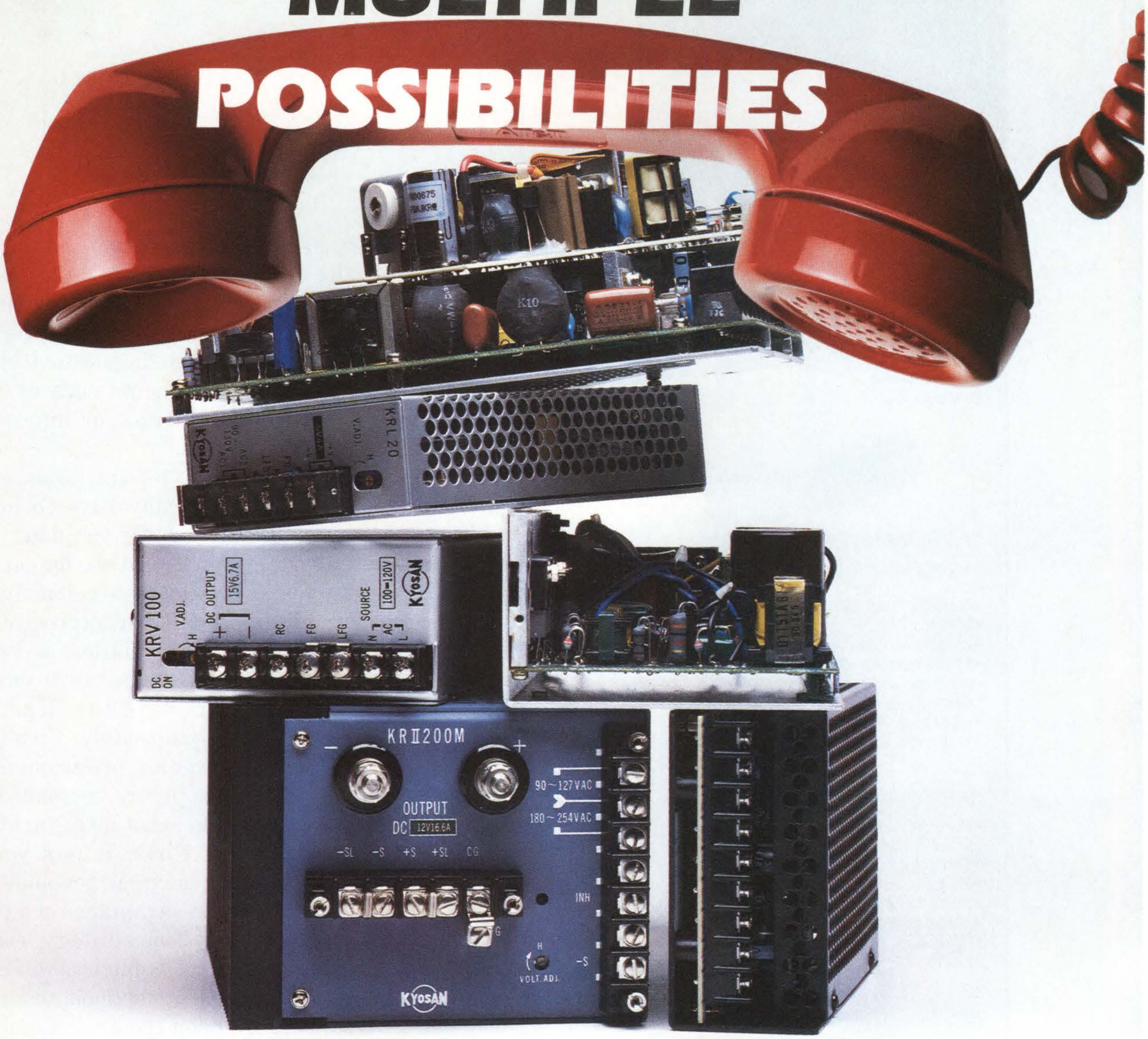
Fig 6—Some components are invisible to a tester. *At 10 kHz, the 165-kΩ impedance of the capacitor is shunted by the 0.6Ω impedance of the inductor—an impedance ratio of 275,000:1. An in-circuit test can't separate the two; only a frequency-response test will reveal whether the capacitor is present and has the right value.*

Guided-probe analysis uses simulator-provided or learned nodal responses to guide an operator with a handheld probe in tracing back from a failed output to the faulty node. The guided-probe algorithm must have access to the full-board circuit-description file, as well as to data about the I/O relationships of each device (that is, which outputs are affected by which inputs). When buses are involved, the algorithm must also have information about which devices are active on the bus for each test pattern, so that it can trace the direction of data flow on the bus. The chief drawback of guided probing is that it's very time consuming, so this bus-activity data is essential for minimizing the number of nodes you have to probe, as well as for ensuring diagnostic accuracy.

Fault-dictionary diagnostic routines use nodal-response data obtained from fault simulation to create a database describing the unique output responses of a cluster to various faults that you've injected into the simulation model. A look-up program then compares the actual responses of a failing cluster with the descriptions in the fault dictionary; close matches indicate likely fault locations.

Although typically it doesn't provide as high a diagnostic resolution as guided-probe analysis does, the

MULTIPLE POSSIBILITIES



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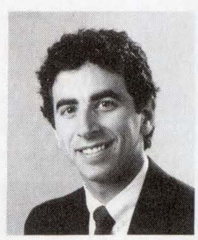
fault dictionary nevertheless has two critical advantages. First, the fault dictionary is fast, yielding a diagnosis in only a few seconds. Second, it's noninvasive—that is, it requires no physical probing of the board's internal nodes—so it's a boon to diagnostic technicians who have to cope with components such as surface-mount devices, which are difficult or impossible to access.

If you want to add cluster testing to an existing in-circuit test strategy, you may have to invest in additional hardware or software. If you don't already have a simulation system, you'll need one for generating functional cluster tests. Cluster tests certainly need a combinational test system—one that incorporates both in-circuit and functional test capabilities, and preferably one in which every test pin can operate in either test mode, so that programmers have the flexibility to define cluster boundaries appropriately. Finally, cluster testing entails more complex programming and diagnostic routines than does purely in-circuit testing.

Cluster testing repays this extra investment in two important ways, however. First, it lets you work around otherwise impossible in-circuit testability problems without taking away the advantages of a primarily in-circuit testing strategy. This strategy, even with the addition of cluster testing, is far less difficult and time consuming than full-board functional testing. Second, cluster tests improve upon the level of fault coverage yielded by in-circuit testing: They can detect faults that involve device interactions, marginal timing, and marginal drive performance. They therefore eliminate the time and expense of diagnosing and repairing such faults at the test bed or during system test and integration. **EDN**

Author's biography



Stephen Caplow was recently named product manager for test application at Teradyne's Design and Test Automation Group (Boston, MA). Prior to that he was applications-engineering manager for the company's L200 Series VLSI board-test systems. Steve holds a BSEE from Tufts University. In his spare time, he enjoys bicycling, squash, and skiing.

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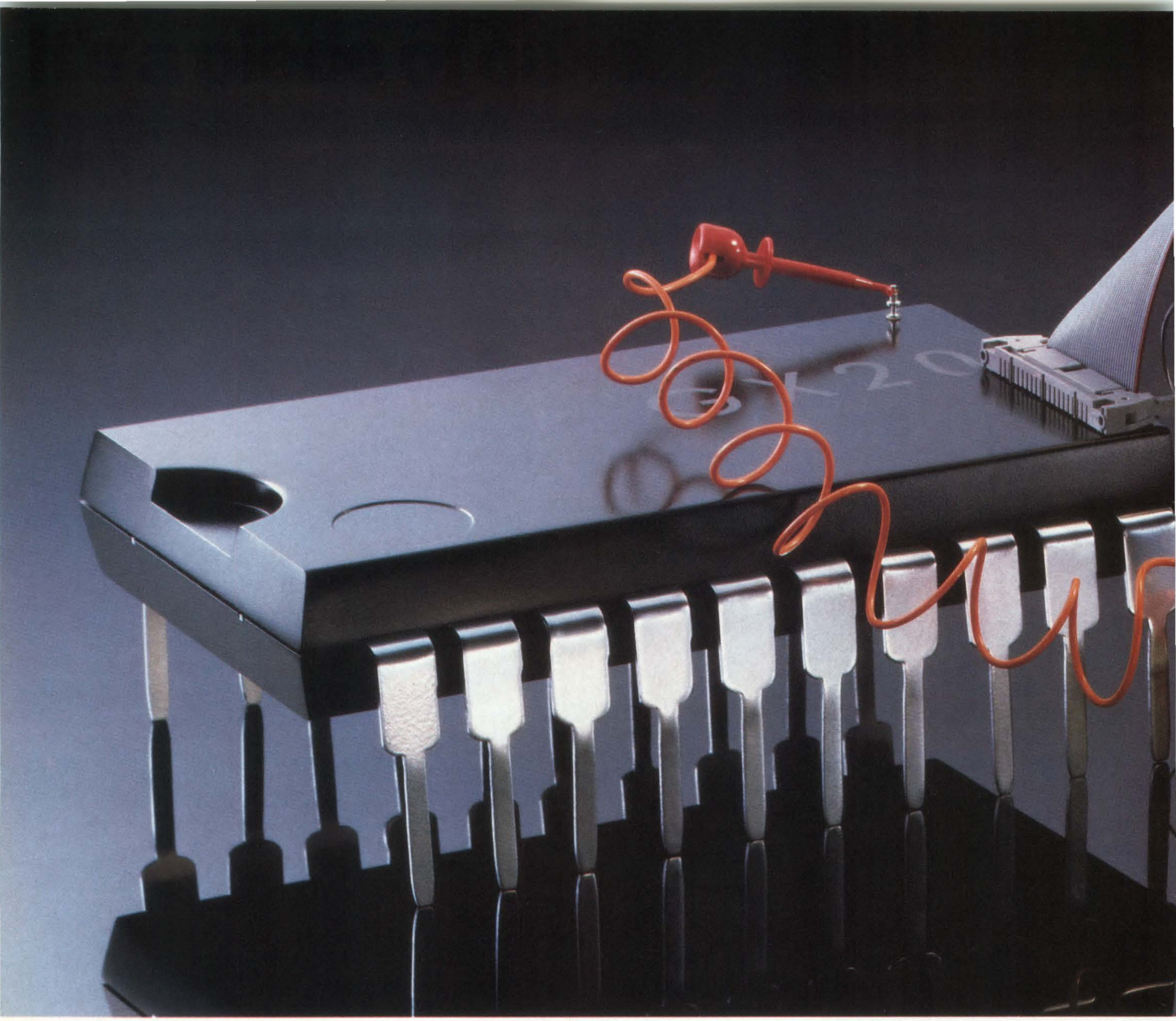

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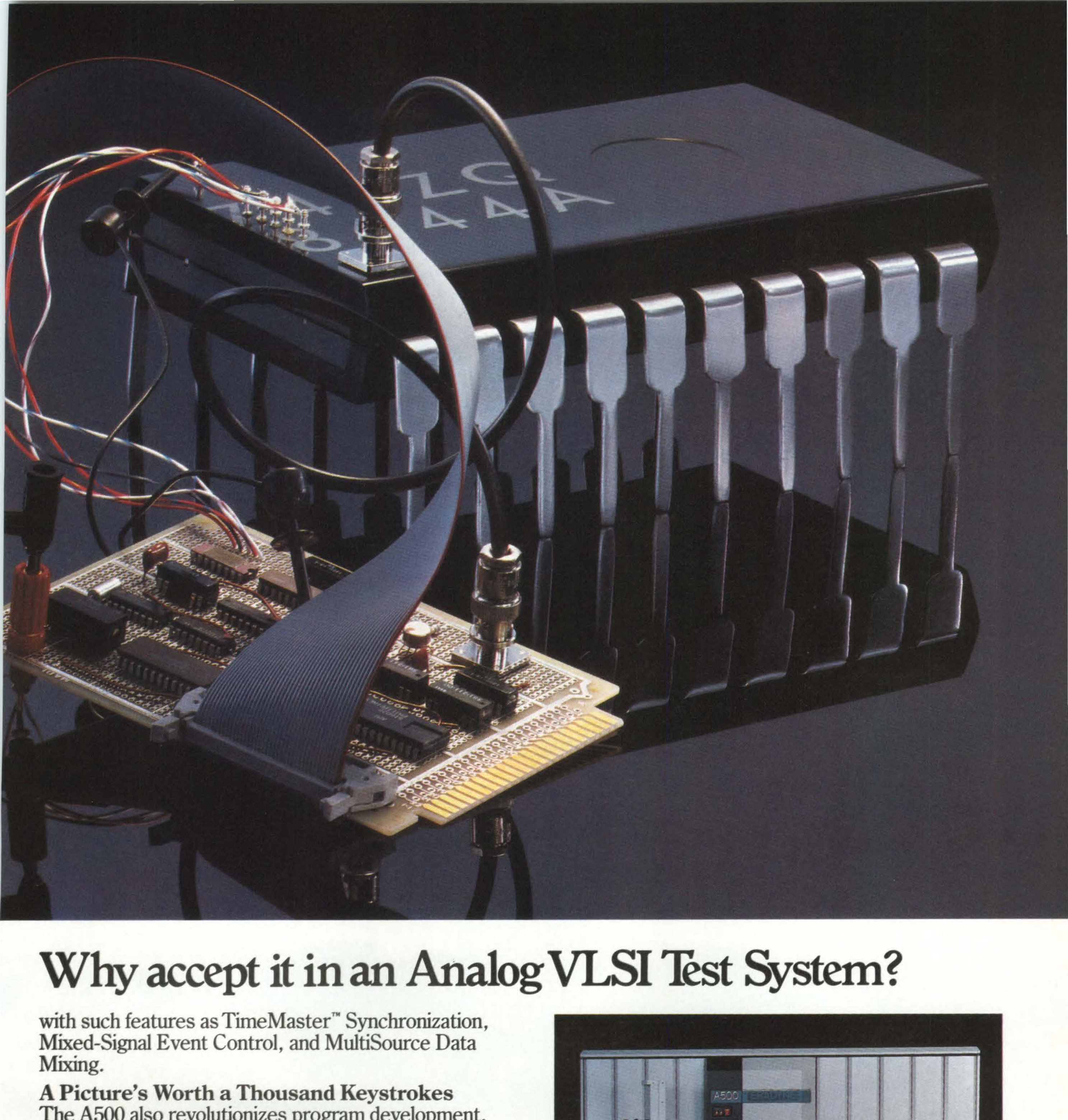

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CIRCLE NO 159

Coherent sampling helps when specifying DSP A/D converters

The use of A/D converters in signal-processing applications often requires knowledge of their dynamic capabilities as well as of their static specifications. You can use digital-signal-processing techniques to evaluate these dynamic parameters.

Brendan Coleman, Pat Meehan, John Reidy, and Pat Weeks, *Analog Devices BV*

In the past, A/D converters primarily found use in measuring static voltage levels. Traditional tests to characterize converters focused on parameters such as dc offset, gain, and integral nonlinearity. Today, sampling A/D converters are capable of digitizing ac waveforms in digital-signal-processing (DSP) systems. A sampling A/D converter includes a sample-and-hold (S/H) function on chip and therefore requires complete dynamic-parameter and dc characterization. As combinations of bipolar and CMOS processes find widespread application in building A/D converters, many ADCs will use a sampling architecture.

For signal-processing applications, you need to determine a converter's dynamic characteristics such as signal-to-noise ratio (SNR), total harmonic distortion (THD), intermodulation distortion (IMD), the effective number of bits (ENOB), and differential nonlinearity (DNL). (For a better understanding of these characteristics, see the **box**, "Dynamic parameters need to be defined.") You can use readily available benchtop instruments to determine these parameters.

To evaluate an ADC's dynamic capabilities, you can use either analog or digital methods. The analog method involves reconstructing the analog signal by feeding the output of the ADC to a D/A converter. You then monitor the reconstructed signal with a spectrum analyzer to determine its spectral content. To ensure reliable tests results, however, the DAC and the associated analog circuitry mustn't introduce appreciable measurement errors. Typically, you need DACs with accuracy specifications that are an order of magnitude better than the ADC, which usually mandates the use of elaborate deglitching and filtering circuits.

Using the digital method to evaluate an ADC's dynamic capabilities requires the digitization of a pure sine wave. A computer then analyzes the digitized samples by using Fourier-transform techniques to determine spectral purity. You can attribute any deviation from the spectral purity of the input sine wave to the ADC. With this method, the output of the ADC remains in its digital form prior to analysis, eliminating the errors introduced by the DAC using the analog method. Software routines evaluate the ADC's dynamic performance.

One of the most efficient methods for doing Fourier analysis on a computer is to implement a fast Fourier transform (FFT) on the data samples. Unless the number of samples you take for the FFT contains a

In signal-processing applications, you need to determine dynamic characteristics.

whole number of periods of the sampled waveform, however, a discontinuity will result at the boundary. These errors appear as side lobes to the main-lobe response and thereby smear the frequency response. One way to reduce the side lobes (or leakages) resulting from the discontinuity is to use a windowing technique.

The Hanning function is one of the most popular windowing techniques. It is mathematically defined as

$$WH(n) = \begin{bmatrix} 0.54+0.46\cos\left(\frac{2\pi n}{N}\right), & \frac{-(N-1)}{2}<n<\frac{(N-1)}{2} \\ 0, & \text{elsewhere} \end{bmatrix},$$

where WH(n) equals the Hanning weighted samples, and N equals the total number of samples.

The window function heavily weights the sample points in the middle of the sampling period and suppresses the data at the ends, thereby reducing any discontinuities. Although these windows attenuate the side-lobe errors, they also spread out the shape of the main-lobe response. The Hanning window spreads the main-lobe frequency response by a factor of 2. It also produces side lobes whose peak values are only −31 dB down from the peak of the main lobe.

A better approach to reducing leakage errors is coherent sampling. Coherent sampling requires a whole number of cycles of the input waveform in the sampled period; therefore, no discontinuity occurs, and window compensation is unnecessary. To maintain coherent sampling, you must observe the following relationship: $F_{IN}/F_S = m/N$. F_{IN} is the frequency of the input waveform, F_S is the sampling frequency, m is the number of cycles of the input waveform in a sampled period, and N is the number of samples during a sampled period.

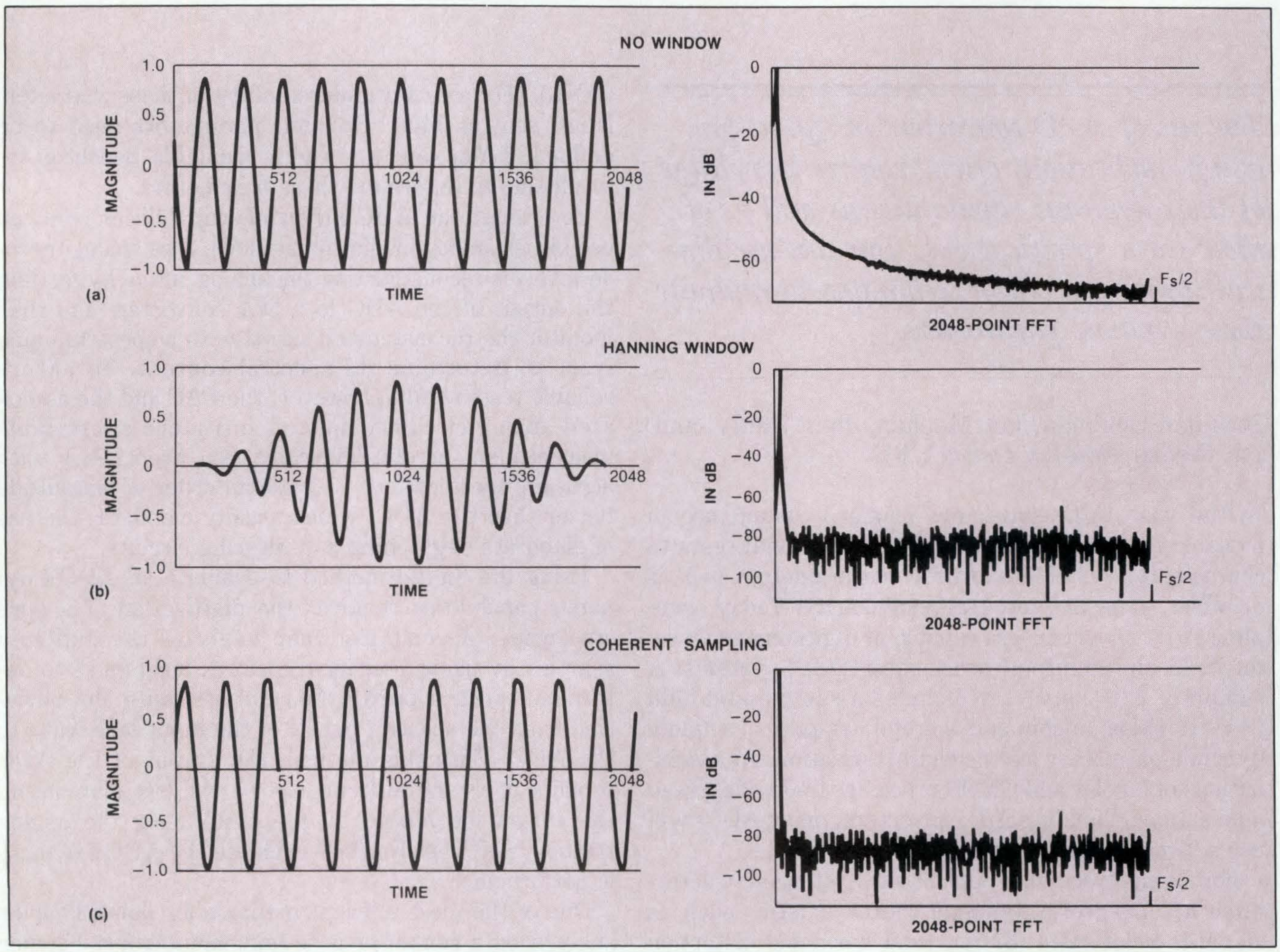


Fig 1—A 10-bit A/D converter took these samples. *Noncoherent sampling without window compensation is shown in* ***(a)****, noncoherent sampling with a Hanning window is shown in* ***(b)****, and coherent sampling is depicted in* ***(c)****.*

Dynamic parameters need to be defined

In the future, data sheets for A/D and D/A converters may routinely include dynamic-parameter specifications as well as static-dc specs. To successfully use converters in signal-processing applications, you need to understand how the following dynamic parameters are defined. You can determine the quantitative values of the parameters by performing spectral analysis.

Signal to noise ratio

In spectral analysis of a sampled data system, noise is measured in the frequency band extending from dc to half the sampling frequency ($F_S/2$). It includes all spectral components other than the signal and dc components. The SNR is defined as SNR=20 log Si/Ni. The SNR is the signal-to-noise ratio in dB, Si is the rms signal power, and Si is the total rms noise power in the frequency band.

Total harmonic distortion

When a sine wave is applied to a nonlinear device, harmonic frequencies occur at multiples of the fundamental frequency. You can measure the total harmonic distortion (THD) by taking the ratio of the square root of the sum of the mean-squared amplitudes of the harmonics to that of the fundamental component. Typically, only five harmonics are taken into account because higher-order harmonics have negligible effect on the calculated THD:

$$THD=20\log(V_2^2+V_3^2+V_4^2+V_5^2+V_6^2)^{1/2}/V_1,$$

where V_1 equals the rms amplitude of the fundamental component, and V_2, V_3, V_4, V_5, and V_6 equals the rms amplitudes of the respective individual harmonic components.

Intermodulation distortion

When two sine waves are present at the input to a device, any nonlinearities in the device create intermodulation distortion (IMD). This distortion is indicated by additional frequency components in the spectrum. If the input sine waves are at the frequencies F_1 and F_2, the frequency at which these intermodulation products occur is governed by $Fmn=m\times F_1\pm n\times F_2$, where m and n can take the values 1, 2, 3 . . . .

The second-order intermodulation frequencies occur when m and n are both equal to 1. These frequencies are F_1+F_2 and F_1-F_2. For other values of m and n, higher-order terms result. The formula for intermodulation distortion due to second-order terms is

$$IMD=20\log(V_{21}^2+V_{22}^2)^{1/2}/(V_{11}^2+V_{12}^2)^{1/2},$$

where V_{11} and V_{12} are the respective rms amplitudes of the two fundamental frequencies. V_{21} and V_{22} are the respective rms amplitudes of the second-order intermodulation frequencies.

Effective number of bits

SNR and the effective number of bits (ENOB) are directly related. Depending on your application, one of these representations may be more useful than the other. In an ideal A/D converter with a full-scale sine-wave input, the theoretical SNR is (6×b+1.8) dB, where b is the number of bits of accuracy. The relationship of SNR (in dB) to ENOB is ENOB=(SNR−1.8)/6.02.

Differential nonlinearity

Histogram testing is a means of evaluating any differential nonlinearity (DNL) that may be present in the ADC. In histogram testing, a sine wave applied to the ADC input covers the full dynamic range of the ADC. You select the frequency of the sine wave such that it is noncoherent with the sampling rate of the ADC, which ensures that all combinations of binary codes are exercised.

Once you've taken a large quantity of samples, plot a histogram of each code vs the frequency of its occurrence. Missing codes show up as gaps in the histogram. You can calculate the DNL for a given code by comparing its actual frequency of occurrence with its theoretical value. The DNL formula for a given code X is

$$DNL(X)=[(AF/TF)-1)]\times LSB,$$

where AF is the actual frequency of occurrence of code X, TF is the theoretical frequency of occurrence of code X, and LSB is the least significant bit.

An FFT plot for coherent sampling shows no spread in the frequency response due to discontinuities.

For a whole number of cycles, m must be an integer, and for nonrepetitive data, m must be odd and prime—eg, 1, 3, 5, 7, 11. When m is odd and prime, sampled data points during each test period will be unique so that you have no inefficiencies due to redundant data.

You can see the effect of coherent sampling in **Fig 1**, which shows the results of a 2048-point FFT taken on samples of a sine-wave waveform. An AD7580 10-bit sampling A/D converter took the samples. **Fig 1a** represents a sampling without any window compensation and with a noninteger number of waveform cycles in the sample period. Because of the severe spread in the frequency response due to side lobing, this circuit is unsuitable for frequency analyses. **Fig 1b** shows a case with window compensation. Even though the side lobes are considerably reduced, there is still some spread of the frequency response. **Fig 1c** shows the result of coherent sampling on exactly 11 cycles of the input waveform. The FFT plot shows no spread in the frequency response due to discontinuities, and thus coherent sampling provides the largest dynamic range for doing spectrum analysis.

Fig 2 shows a test setup for performing coherent sampling to measure an A/D converter's dynamic characteristics. Coherent sampling requires that the frequency of the input waveform to the ADC and to all control signals are frequency locked to a reference oscillator.

To avoid sampling uncertainty or jitter errors, the interval between samples must be constant, which means that the conversion-start command to the ADC must be synchronized with the sampling frequency. You can derive this command from the reference generator by using an external counter. You should use an external buffer memory to temporarily store the digitized samples. All read and write clocks should also be

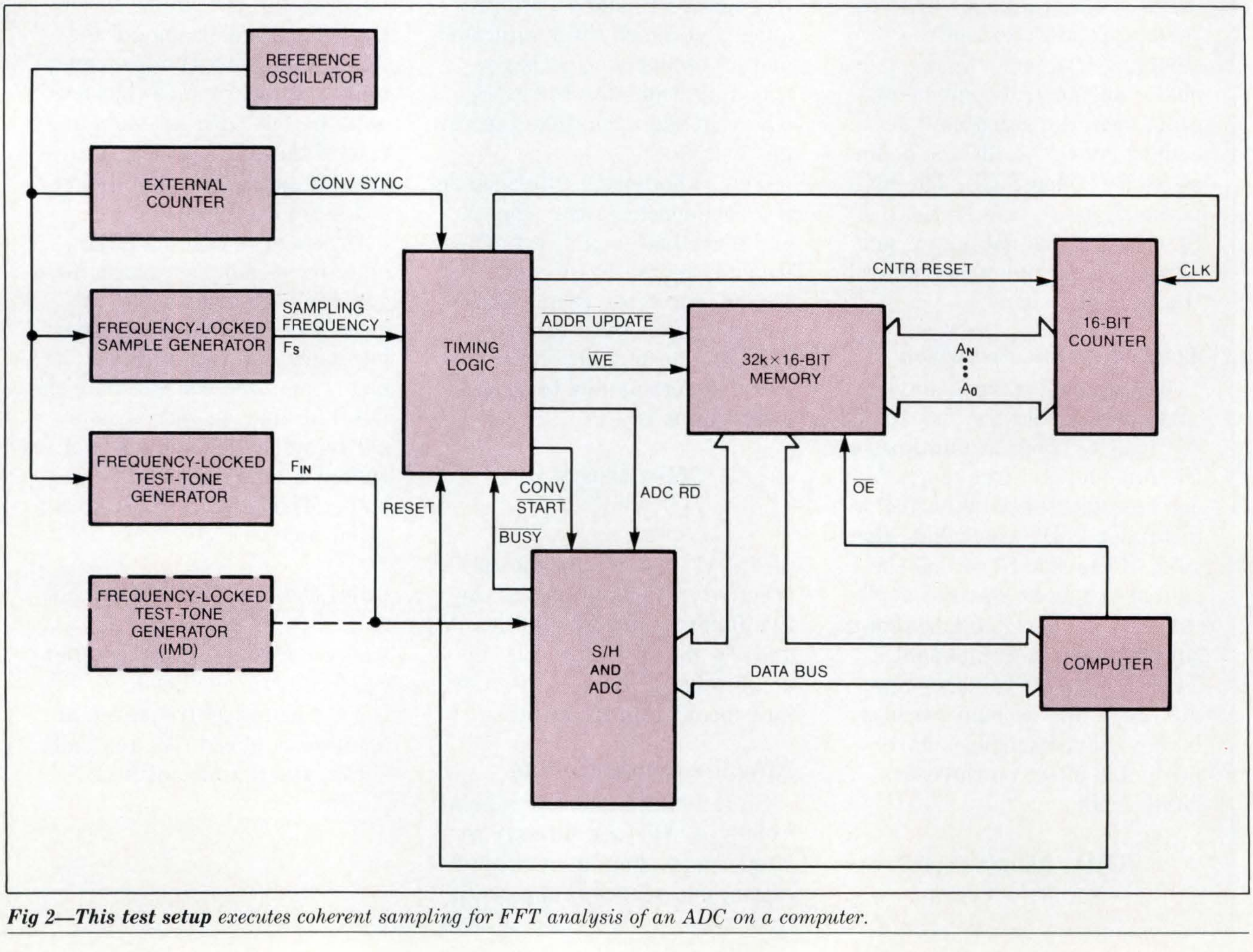


***Fig 2—This test setup** executes coherent sampling for FFT analysis of an ADC on a computer.*

synchronized to the sampling frequency to ensure jitter-free sampling. A memory buffer that uses 100-nsec, 32k×8-bit static RAMs in a 16-bit-wide configuration provides enough storage space for most applications. A 16-bit counter, which is reset at the start of the sampling sequence, supplies all the necessary memory addresses.

The expected quantization noise floor for an ADC determines both the SNR and the THD requirements for the test-tone generator. Usually, the test-tone generator that generates the sine-wave waveform must have a THD lower than −100 dB to test a 12-bit ADC. A 2048-point FFT performed on 12-bit accurate samples will yield a noise floor that is 100 dB below the fundamental component; therefore, no harmonic of the test-tone generator should be within 100 dB of the fundamental component. A Tektronix SG5010 programmable oscillator is a good choice for this task.

Another important requirement for the tone generator is that the test signal amplitude covers the entire dynamic range of the ADC, and that the amplitude remains constant over the frequency range of interest. You should also carefully match source and load impedances to minimize THD error.

To calculate the test-tone frequency (F_{IN}) for a given sampling frequency (F_S), use the equation $F_{IN}=m\times F_S/N$. N is the number of samples and should be equal to $2^{INTEGER}$ for FFT analysis. The variable m represents the number of cycles of the input frequency, and should be an odd and prime integer to prevent data redundancy. Quite often for a given sampling frequency, you find that the desired test-tone frequency is hard to generate. To make this generation easier, let F_S be an integer multiple of N, which will make F_{IN} an integer number.

A frequency synthesizer is a practical method for making the sampling frequency a known ratio of the test-tone frequency. **Fig 3**'s approach uses a 74HC4046 phase-locked loop with a frequency divider in the feedback path. This circuit establishes a sampling frequency that is an integer multiple of its input frequency. The input frequency to the synthesizer is derived from a stable reference generator. The reference generator produces the square wave to which the test-tone

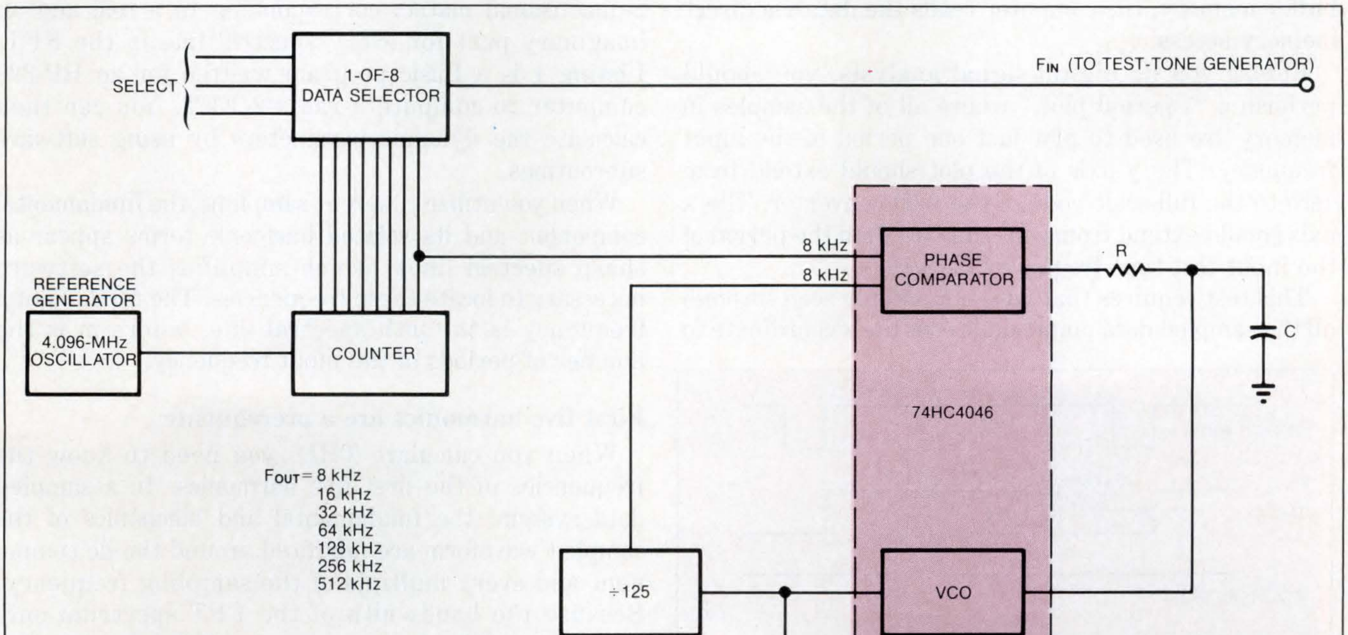


Fig 3—A frequency synthesizer generates *a sampling frequency that is an integer multiple of the test-tone frequency.*

A frequency synthesizer is a practical method for making the sampling frequency a known ratio of the test-tone frequency.

oscillator is locked. The reference generator's output frequency and amplitude must be within the locking range of the slave circuits (typically 1 MHz for TTL levels). According to this method, any frequency drifts are compensated for because all frequencies maintain the same ratios.

In a typical timing diagram of a single-conversion sequence **(Fig 4),** the timing logic issues a conversion-start (Conv $\overline{\text{Start}}$) command to the on-chip S/H converter, which initiates the digital conversion of the sampled analog input. The conversion-start command is derived from the external counter and is therefore synchronous with the test-tone frequency and the sampling frequency. The converter sends a busy command to the timing logic, indicating that the conversion is in progress.

When the conversion is complete, the timing logic issues an ADC $\overline{\text{RD}}$ command to access the ADC's 3-state output buffers, followed by a $\overline{\text{WE}}$ command to latch the data into memory. The memory address is then incremented via the $\overline{\text{Address Update}}$ command, which addresses a new space in memory to store the next sample. When N samples have been read into the buffer memory, the computer reads the data via direct memory access.

Before you do digital-signal analysis, you should perform a "1-period plot," where all of the samples in memory are used to plot just one period of the input frequency. The y axis of the plot should extend from zero to the full-scale code of the A/D converter. The x axis should extend from zero time (t=0) to the period of the input test-tone frequency ($t=1/F_{IN}$).

This test requires that you sequentially scan through all the sampled data points and reset the x coordinate to zero on each cycle of the test tone until all cycles are plotted. All samples should lie on the theoretical sine curve. Any deviation will indicate synchronization or frequency-locking problems (that is, the input test-tone frequency drifting with respect to the sampling frequency). The plot will also permit you to ascertain if the input of the sine wave is greater than the dynamic range of the converter.

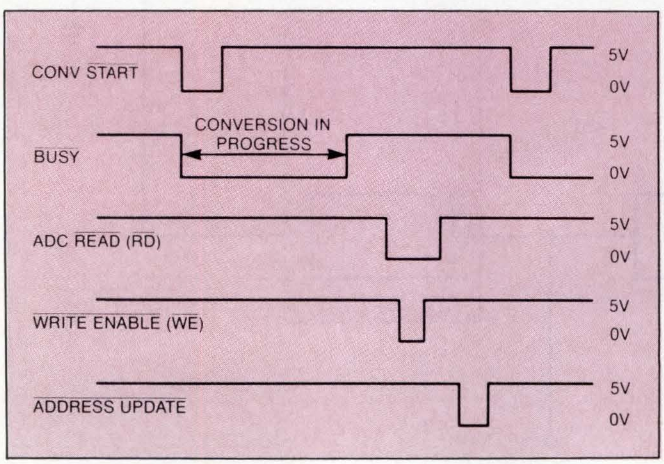


Fig 4—This timing diagram is typical *of the type required to digitize coherent samples and store them in a buffer memory.*

You can use almost any desktop engineering computer for digital signal analysis. Select a computer, however, with sufficient memory to accommodate all of the samples and large enough to execute the test algorithms. A computer with 250k bytes of memory is normally sufficient. Although speed may not be a major concern, some 16-bit processor-based systems may take as long as one minute to execute a 2048-point FFT. Because a complete analysis requires numerous FFTs to characterize an ADC over its frequency range, programming considerations can be important.

There are numerous implementations of the FFT, but a radix-2 decimation-in-time (DIT) implementation is the most popular. The radix-2 FFT produces a 2-dimensional matrix corresponding to a real and an imaginary part for every spectral line in the FFT. **Listing 1** is a Basic program written for an HP-320 computer to compute a radix-2 FFT. You can then calculate the dynamic parameters by using software subroutines.

When you utilize coherent sampling, the fundamental component and its related harmonic terms appear as sharp spectral lines, which simplifies the software necessary to locate these frequencies. The fundamental frequency is the mth spectral line, where m is the number of periods of the input frequency.

First five harmonics are a prerequisite

When you calculate THD, you need to know the frequencies of the first five harmonics. In a sampled data system, the fundamental and harmonics of the sampled waveform are mirrored around the dc component and every multiple of the sampling frequency. Because the bandwidth of the FFT spectrum only extends from the dc component to half of the sampling frequency, you need a formula to find the higher harmonics that exceed the FFT bandwidth. You can determine the frequency components that are aliased into the FFT bandwidth due to multiples of the sampling frequency according to the formula $FHi=ABS(k\times F_S-i\times F1)$, where F1 is the fundamental frequency of the waveform, i is the harmonic number,

LISTING 1—A RADIX-2 FFT COMPUTATION WRITTEN IN BASIC FOR AN HP-320

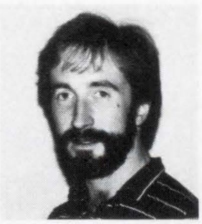
```
2152  sub Fft(Ar(*),Ac(*),M)
2153  !
2155  !
2156  INTEGER I,J,N,Nm1
2157  RAD
2158  N=2^M
2159  I=1
2160  J=1
2161  Nm1=N-1
2162  FOR I=1 TO Nm1 STEP 1
2163       IF I>=J THEN
2164          GOTO Lab2
2165                ELSE
2166          Tempr=Ar(J)
2167          Ar(J)=Ar(I)
2168          Ar(I)=Tempr
2169          Tempc=Ac(J)
2170          Ac(J)=Ac(I)
2171          Ac(I)=Tempc
2172       END IF
2173 Lab2: !
2174       K=N/2
2175 Lab3: !
2176       IF K>=J THEN GOTO Lab4
2177       J=J-K
2178       K=K/2
2179       GOTO Lab3
2180 Lab4: !
2181       J=J+K
2182  NEXT I
2183  FOR L=1 TO M                                        !INCREMENT STAGE
2184       Le=2^L
2185       Le1=Le/2
2186       Ur=1
2187       Uc=0
2188       Wr=COS(PI/Le1)
2189       Wc=-SIN(PI/Le1)
2190       FOR J=1 TO Le1
2191            FOR I1=J TO N STEP Le                  !PERFORM BUTTERFLY
2192                 I2=I1+Le1
2193                 Tr=Ar(I2)*Ur-Ac(I2)*Uc         !Tc =TEMP COMPLEX VARIABLE
2194                 Tc=Ar(I2)*Uc+Ac(I2)*Ur         !TR =TEMP REAL VARIABLE
2195                 Ar(I2)=Ar(I1)-Tr
2196                 Ac(I2)=Ac(I1)-Tc                 !I1=FIRST ELEMENT OF BUTTERFLY
2197                 Ar(I1)=Ar(I1)+Tr                 !I2=SECOND ELEMENT OF BUTTERFLY
2198                 Ac(I1)=Ac(I1)+Tc
2199            NEXT I1
2200            Ur1=(Ur*Wr)-(Wc*Uc)                           !INCREMENT COEFFICIENT
2201            Uc=(Wr*Uc)+(Wc*Ur)
2202            Ur=Ur1
2203       NEXT J
2204  NEXT L
2214  !
2224  SUBEND
```

F_S is the sampling frequency, k is the multiple of the sampling frequency, and FHi is the frequency of the aliased component.

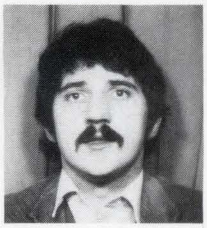
Be careful when analyzing the digitized samples. Random noise may not be noticeable in an FFT analysis because FFTs are designed for periodic signals. You may require correlation techniques to analyze random noise components. Other sources of concern are impedance matching, the quality of the input buffers, grounding considerations, and power-supply noise. Any of these factors can seriously degrade overall system specifications. **EDN**

Authors' biographies

Brendan Coleman has worked for Analog Devices in Limerick, Ireland, since 1982. He was educated at the College of Art, Commerce, and Technology, also in Limerick. He provides support for a design engineering team that evaluates devices for process development and circuit simulation. He has also worked in test engineering. His hobbies are tennis, music, and the theatre.



Pat Meehan is a senior engineer and head of the Design Evaluation Laboratory at Analog Devices BV. He received his Bachelor of Engineering degree in Electronics from the National Institute for Higher Education, Limerick. In addition to DSP, he is interested in radio.



John Reidy is an applications engineer at the same plant. In this capacity, he provides technical support to the sales force. He has an Electronic Bachelor of Engineering degree from the National Institute for Higher Education. In his spare time, John likes to play badminton, softball, and the guitar.

Pat Weeks is an Analog Devices' design engineer and has worked with the company since 1985. He holds a Bachelor of Engineering degree in Electronics from the National Institute for Higher Education. His hobbies include farming, music, and chess.

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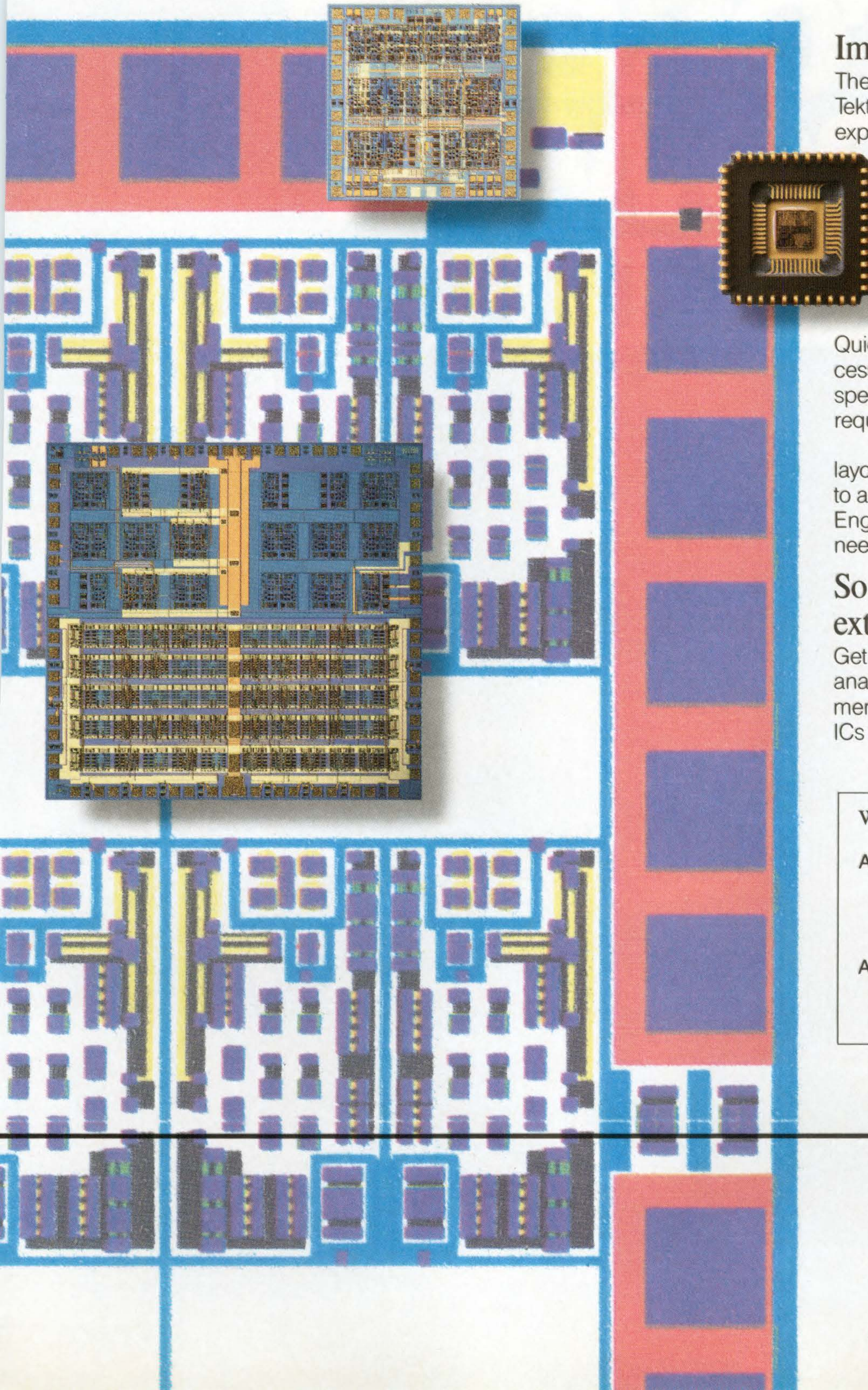

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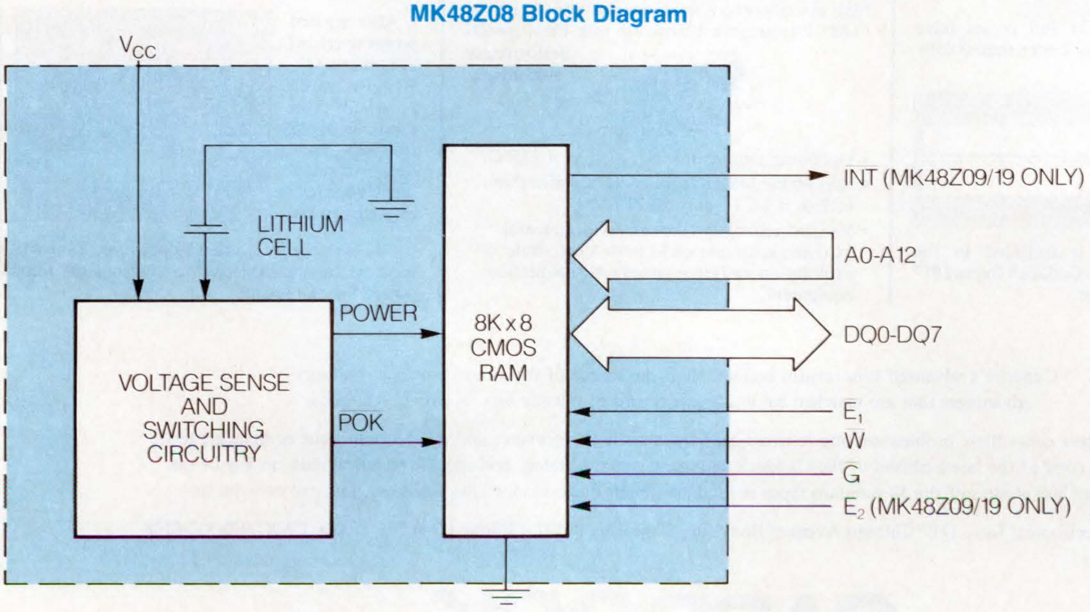
MK48Z12	0-70 C	4.5V	11 yrs.	Yes	120-250ns	2K x 8 SRAM unltd. write cycles
MKI48Z02	−40–85 C	4.75V	6 yrs.	Yes	120-250ns	2K x 8 SRAM indust. temp. range
MKI48Z12	−40–85 C	4.5V	6 yrs.	Yes	120-250ns	2K x 8 SRAM indust. temp. range
MK48T02	0-70 C	4.75V	11 yrs.	Yes	120-250ns	2K x 8 SRAM w/realtime clock
MK48T12	0-70 C	4.5V	11 yrs.*	Yes	120-250ns	2K x 8 SRAM w/realtime clock
MK48Z08/09	0-70 C	4.75V	11 yrs.	In Progress	120-250ns	8K x 8 SRAM w/additional CE and power fault flag (−09)
MK48Z18/19	0-70 C	4.5V	11 yrs.	In Progress	120-250ns	8K x 8 SRAM w/additional CE and power fault flag (−19)

*3.3 yrs. maximum, clock operating in battery backed mode.

MK48Z08 Block Diagram



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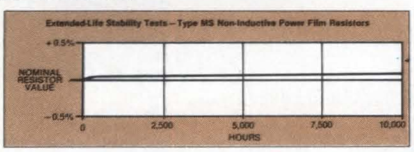

Detailed stability data is included in the "Reliability Test Summary – Caddock Report #1" which is available on request.

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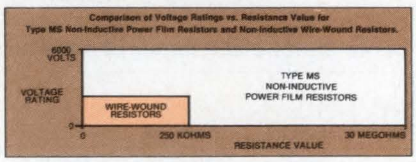

The higher voltage rating of Type MS resistors also overcomes the resistance value limits imposed on wire-wounds by the minimum wire size and spacing.

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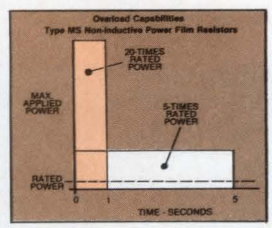

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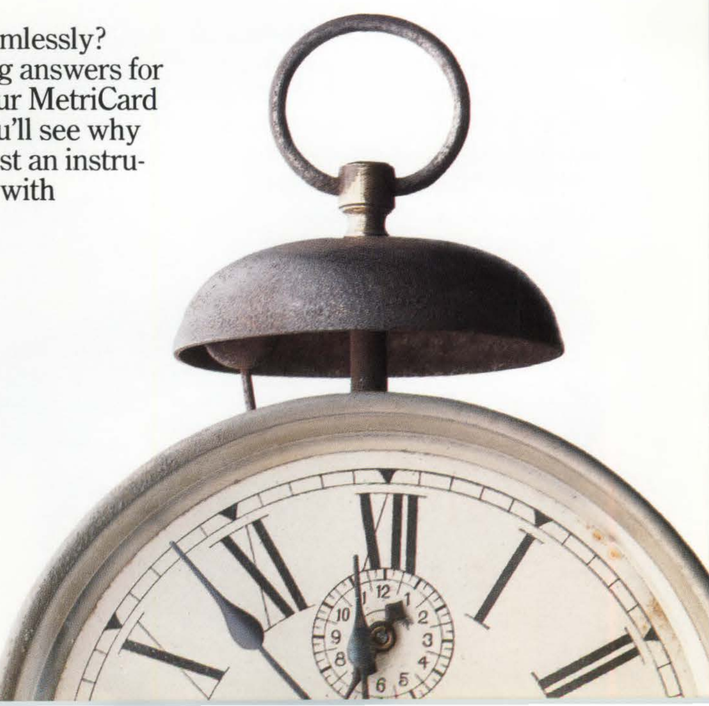

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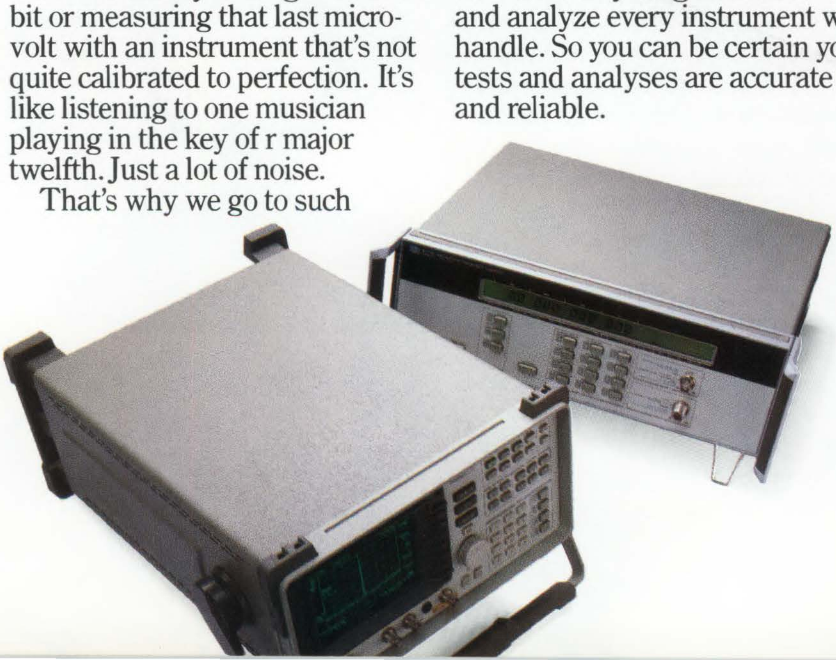

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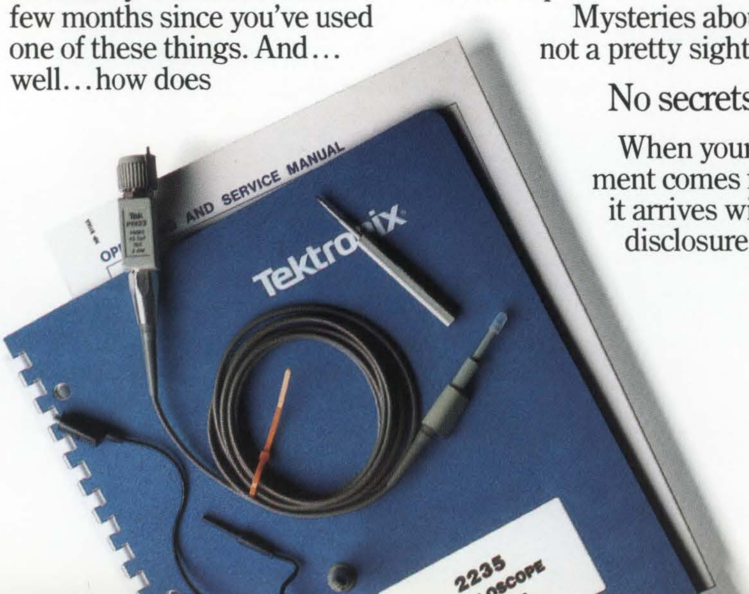

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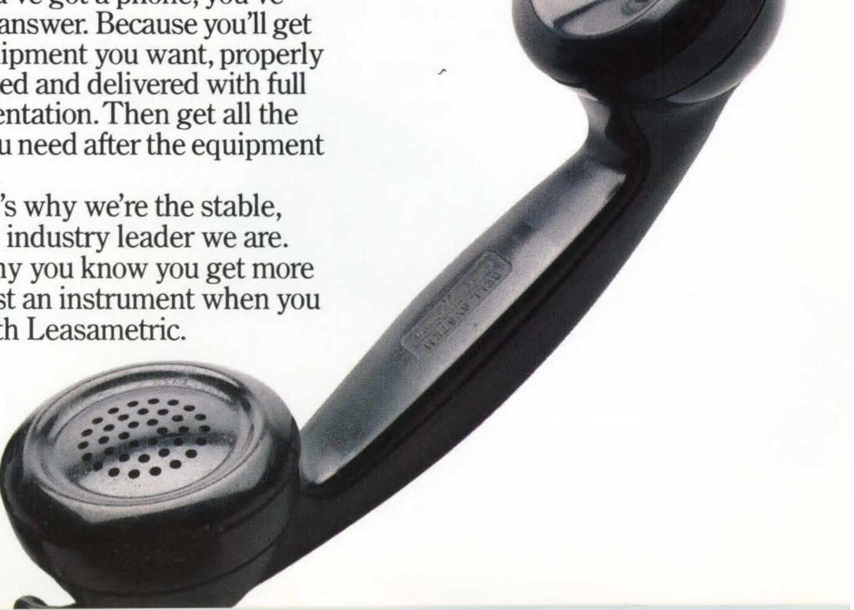

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Probing techniques become crucial above 500 MHz

As circuit and oscilloscope bandwidths increase, getting distortion-free signals to your scope is an increasing challenge. Probe effects that are bothersome at 100 MHz become devastating at 1 GHz. By understanding how probes interact with high-frequency circuits, you can improve your chances of making accurate measurements.

Eldon Walters and Stan Kaveckis, *Tektronix Inc*

Because the laws of physics become increasingly unforgiving as signal rise times shorten, oscilloscope probing techniques affect high-frequency signals more than most engineers realize. The failure to apply transmission-line concepts and proper grounding connections can alter your signals beyond recognition.

To view and measure high-frequency signals accurately, you need a probe equal to the task of working with today's circuits and oscilloscopes. Good-quality probes are essential for high-frequency jobs; it's equally important to use the probes correctly. Otherwise, you might waste time trying to eliminate what looks like ringing in your circuit but is only an artifact of your probing. Or you might fail to see a glitch that is really there. Only by understanding the physics of probing can you be sure that your oscilloscope displays useful information.

The three main considerations in probing are

- The reactive loading of a transmission line
- The physical-length limitations of a transmission line
- The limitations of the ground connections.

Each of these factors can become appallingly complex. For example, reactive loading includes capacitance and inductance from several sources, which exert different types of influence over signals. Reactive effects become increasingly profound as frequencies increase. Fortunately, the frequencies you're likely to be dealing with for the foreseeable future won't require that you delve into the mathematics of quantum effects. You do have to rigorously apply some transmission-line and grounding concepts, however.

Approaching the 500-MHz danger zone

The degree of rigor necessary depends on the signals you're working with. At 10 kHz, you can feel safe

You might waste time trying to eliminate what looks like ringing in your circuit but is only an artifact of your probing, or you might fail to see a glitch.

ignoring transmission-line concepts and make your ground wire about as long as you want. The situation becomes increasingly hazardous as the frequency rises. This article is primarily concerned with measurements on circuits where the highest frequency component of interest lies above 500 MHz or thereabouts. If a GaAs circuit is clocked at 1 GHz, for example, you must be able to see the significant harmonics of the clock, which extend the bandwidth requirements to 3 to 5 GHz. Above this 3- to 5-GHz frequency, probing in its generally accepted form becomes all but impossible.

You can also define the frequency area of concern in terms of the minimum rise time you want to be able to see on an oscilloscope. You should define this rise time such that it allows you to detect the fastest glitch that might affect your circuit. To translate rise time into bandwidth, you can use the following approximation, which assumes that the vertical amplifier in your scope has a Gaussian response (that is, the step response resembles half of a Gaussian bell curve):

bandwidth in megahertz=350/(rise time in nanoseconds).

GaAs-circuit rise times usually range from 50 to 200 psec, with frequencies of interest about 2 to 5 GHz and beyond. ECL-circuit rise times are as short as 400 psec, so frequency components are in the 1-GHz region. Even with TTL signals, you must sometimes deal with rise times as short as 0.5 nsec, which translates into the frequency area above 500 MHz.

In addition to considering the signal frequencies of the circuit under test, you must work within the limits of your test instruments. Today's sampling oscilloscopes can display waveforms containing frequencies higher than you're likely to encounter. Specialized samplers are available with 70-GHz bandwidths, for instance, which puts them far beyond the limits of currently available probes' capabilities. Don't forget, though, that there are weak links in the measurement chain, which can distort your display. As scope bandwidths have improved dramatically in recent years, many engineers have had the unsettling experience of seeing familiar circuits produce unfamiliar outputs—often the result of a new oscilloscope revealing probe deficiencies that weren't noticeable with a less-capable scope.

In fact, probe technology has been hard pressed to keep up with the generally available level of sampler, oscilloscope, and TDR (time-delay-reflectometer) capabilities. The latest general-purpose sampling scopes offer bandwidths higher than 14 GHz, allowing the display of rise times as short as 25 psec.

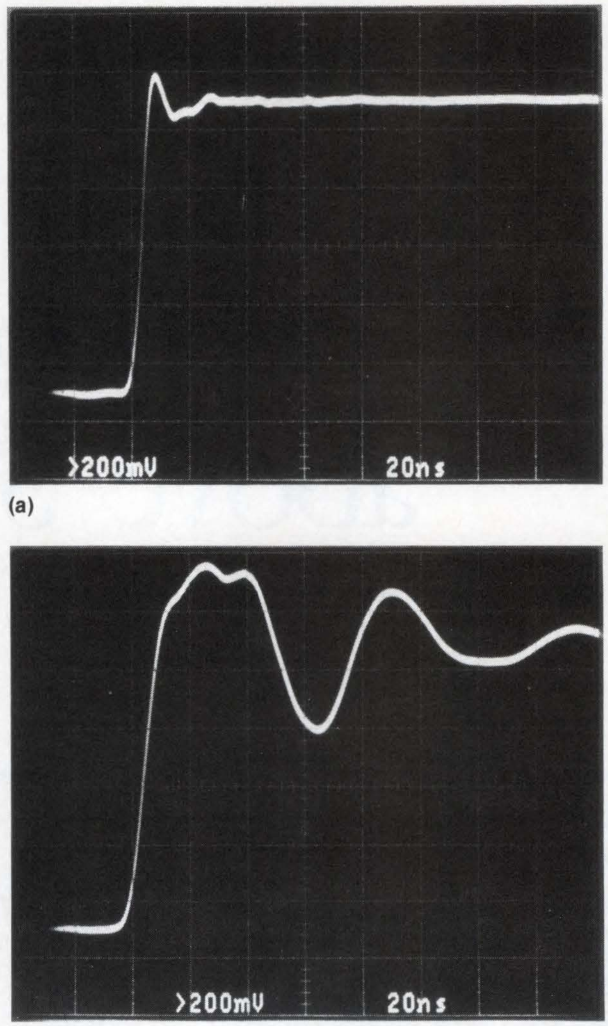


Fig 1—Loading a 500Ω impedance source with a 10-MΩ, 10-pF probe produces a 6-nsec rise time (a). Replacing the probe with two 2m lengths of hookup wire changes the loading to 1 MΩ and about 20 pF, and slows the rise time to about 10 nsec—in addition to ruining the transient response (b).

Get used to transmission lines

The single most important concept to remember in high-frequency probing is that every part of the measurement setup behaves like a transmission line. These elements include the probe and its ground connection as well as the conductors in the circuit under test; at low frequencies you could think of them as lumped for magnetic fields. The effects of the noise sources change any time you touch or rearrange the wire. **Fig 2** shows how interference can modify a signal.

Furthermore, with an unshielded wire, noise signals are not only routed into the scope along with the wanted signal, they can also be injected into the circuit under test. The source impedance of the circuit under test has a major influence on the amplitude of interference developed in the probe wire. A very low source impedance will tend to shunt capacitively coupled noise to ground, but high-frequency signals may still appear at the scope input and mask the wanted signal. A scope probe virtually eliminates the pickup of both electric and magnetic fields because its coaxial construction provides shielding.

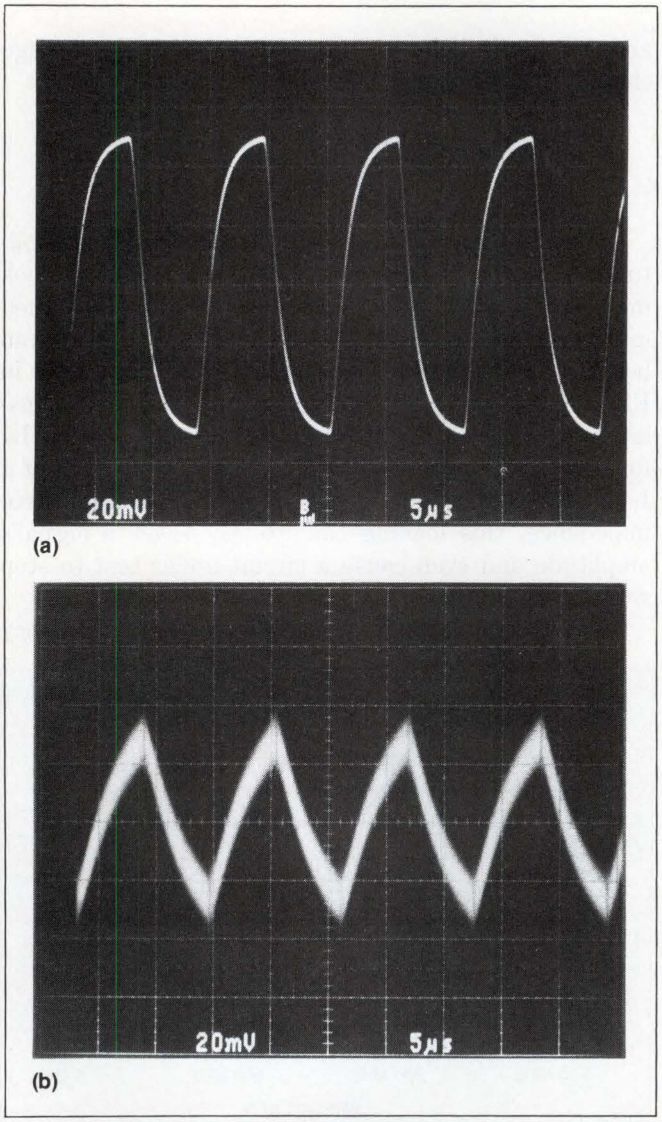


Fig 2—A true representation of a low-level signal *from a high-impedance source **(a)** changes drastically when hookup wire replaces the scope probe **(b)**. The amplitude decreases due to increased resistive and capacitive loading, and noise is added because the wire is unshielded.*

elements. **Fig 1** shows an extreme example of the signal degradation that can occur, even at low frequencies, when you use a piece of wire as a probe. The same loading principles apply to an ever-increasing extent as frequencies rise.

This example makes another factor painfully obvious. An unshielded wire acts as an antenna for capacitive coupling of ambient electric fields from ac power wiring, fluorescent lamps, radio transmissions, and nearby equipment; a loop of wire (eg, an unshielded scope lead and its associated ground) acts as an inductive pickup

According to transmission-line theory, a coaxial cable that's properly terminated (with respect to the circuit under test) introduces a minimum amount of degradation to a signal. The coaxial cable loads the circuit under test in the sense that it draws off as much as half of the signal energy, but the function of the higher value of resistance included in most passive probes is to minimize this effect. Moreover, this type of loading doesn't tend to degrade the signal quality if the signal source can drive the load.

In some cases, manufacturers of boards that use GaAs and high-speed ECL components use a piece of correctly terminated 50Ω coaxial cable to make measurements because of the circuits' inability to withstand capacitive loading. The only ac test the manufacturers perform on the boards is at the coaxial output connector: Probing the board using currently available probes would create unacceptable loading. If the signal at the output doesn't meet its specification, the hybrid or IC that produced it is discarded. Advances in probe technology will eventually make it possible to test these components at the wafer stage, but advances in semiconductor speeds will continue to result in some circuits that fall outside the capabilites of state-of-the-art probes.

Nevertheless, at frequencies above 500 MHz—yet low enough that probing is still practical—you must consider the effects of the circuit elements in **Fig 3**. The values of these loading effects depend on probe construction, the impedance of the signal source, and the quality of the ground connection. You can control the first variable (and account for the second) by selecting a probe that suits the job at hand. The ground quality also varies depending on the probe you select, as well as on the length of the ground path.

The biggest contribution to reactive loading comes

Fortunately, the frequencies you're likely to be dealing with for the foreseeable future won't require that you delve into the mathematics of quantum effects.

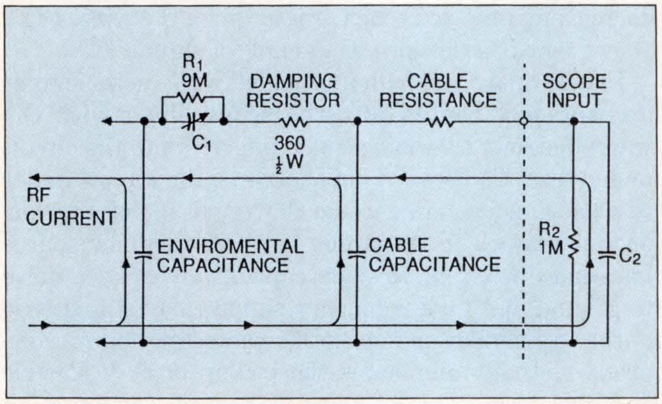


***Fig 3—The types of loading introduced by a probe** have different effects, but you can generally consider the loading sources as a combination of series resistance and parallel capacitance.*

from the capacitance created between the probe's tip and ground sleeve and the probe cable's center conductor and shield. An example will show how this loading affects a signal. In this case, the circuit under test generates a signal with a 0.5-nsec rise time. The signal's speed is influenced primarily by the circuit's resistance and capacitance, which limits the rise time to 2.2 RC, according to the universal time-constant curve for a capacitor (**Fig 4**).

If you use a probe to measure the signal, the loading diagrammed in **Fig 3** is added to that of the circuit under test. If the probe provides a typically high resistance, say 1 MΩ, you can ignore the resistive loading, but the probe's 2-pF capacitance must be added to that of the circuit. Applying the 2.2 RC formula again reveals that the rise time has lengthened to 0.7 nsec—a degradation of 40%.

Because capacitive loading effects depend almost entirely on the ratio between the values for the probe

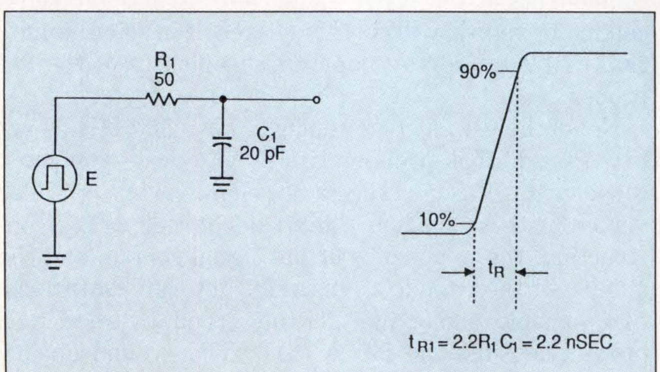


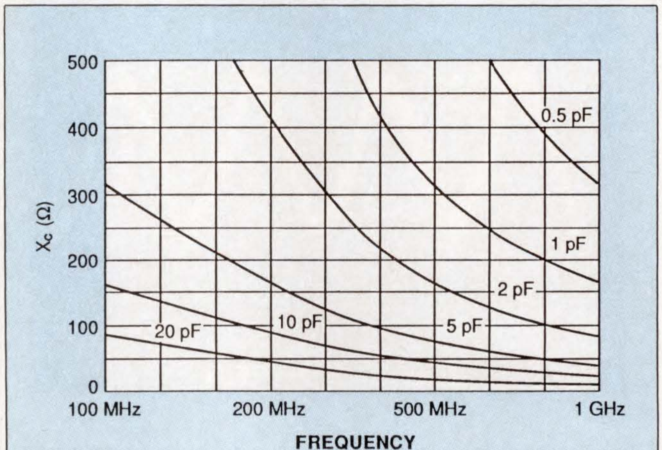
***Fig 4—Because of internal source resistance** and capacitance in the probe, at no time can the output rise time be faster than 2.2 RC.*

and the circuit under test, you can estimate percentage changes in rise time using

(C probe tip/C circuit)100=rise-time percentage change.

Capacitive loading can also affect a signal's amplitude: At higher frequencies, a capacitor begins to look increasingly like a short circuit. Inductance designed into most probes tends to offset this effect, but it can become troublesome at high frequencies. The curves in **Fig 5** show how a probe's capacitive reactance translates into impedance at different frequencies. At 1 GHz, for example, the total impedance seen at the tip of a 1-pF probe equals only 160Ω. Depending on the source impedance, this loading can greatly lower a signal's amplitude and even cause a circuit under test to stop working altogether.

Most probes come with an impedance-vs-frequency



CAPACITIVE REACTANCE (Ω) **VS FREQUENCY** (MHz)

C (pF) \ MHz	100	200	400	500	600	800	1000
0.2	7960	3980	1990	1592	1326	995	796
0.5	3184	1592	796	637	530	398	318
1	1592	796	398	318	265	199	159
2	796	398	199	159	133	100	80
5	318	159	80	64	53	40	32
10	159	80	40	32	27	20	16
20	80	40	20	16	13	10	8

***Fig 5—Impedance associated with capacitive reactance** varies with frequency. The lower the reactance, the higher the susceptance and the greater the loading of the circuit under test.*

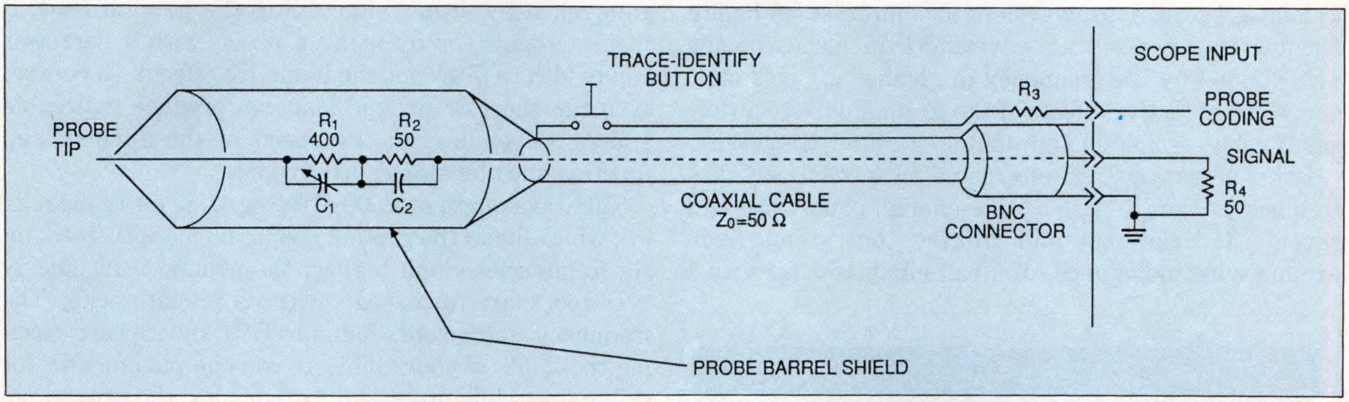


***Fig 6—The impedance sources in a low-Z probe** differ from those of a standard probe. Unlike the latter, a low-Z probe imposes near-zero susceptance loading on the circuit under test.*

graph, but if you can't lay your hands on the graph when you need it, you can get a good worst-case impedance value by using

$$X_C = 1/2\pi fC,$$

where X_C equals the capacitive reactance (in ohms), f equals the frequency of interest, and C equals the probe-tip capacitance (marked on the probe).

Alternative probes solve some problems

One way to obtain very low tip capacitance is to use a low-Z probe. You get this benefit at the expense of resistive loading, however. For instance, "50Ω" probes are available with 0.25-pF input capacitance, 500Ω resistance, and 10× attenuation. As long as the signal frequency stays below 1.25 GHz, the magnitude of the capacitive component of the input impedance remains larger than the resistive component. In **Fig 6,** because the cable acts as a transmission line, the probe's 450Ω tip resistor (the series element in the 10× voltage divider) sees only a pure 50Ω resistance; there is no capacitive or inductive component.

Note that this probe comes very close to being the simple piece of coaxial cable suggested earlier. The main difference is the 450Ω resistor used to improve resistive loading. The resistor reduces the scope's sensitivity at the probe tip by a factor of 10, but it also improves the loading by the same factor.

Low-Z probes are good for making high-speed rise time measurements, but the resistive loading can devastate a signal's amplitude (which also affects the 90% level at which you measure rise time and may thus affect the measured rise time). You're better off confining these probes to circuits having an impedance of 50Ω or less. (Impedances must be matched to the scope as well.)

It's possible to get both low resistive loading (10 MΩ) and low capacitive loading (1 pF) at the same time if you use an active probe, though this type of probe may be limited in bandwidth. These probes also have a FET input, which provides high sensitivity. The tradeoffs are that they have a limited dynamic range, and they can't handle very high power levels. Also, you should be aware that at most frequencies of interest capacitive reactance dominates the input impedance of a probe in which a 1-pF capacitance shunts a 10-MΩ input resistance.

Another option is sampling probes, which perform signal acquisition at the probe tip. Products such as the Model S3A from Tektronix (Beaverton, OR) and the Models 943 and 960 from EH International Inc (Fremont, CA) furnish high impedance and high bandwidth. These probes handle bandwidths in excess of 1 GHz with minimal loading.

Ground connections deserve respect

Just as critical as the probe itself is the probe's ground connection, which introduces inductance to the signal path. The ground-lead inductance and the probe capacitance form a series-resonant circuit that can produce overshoot or ringing when hit with a pulse. The inductance also limits the rate of change of current through the probe capacitance, thus limiting the displayed rise times. In addition, a long ground lead can add noise to the signal.

The longer the ground return path, the greater the inductance. You'll find it difficult to determine just how long is too long for any given case, but a rule of thumb does exist: The ground lead should be no more than 1/20

The single most important concept to remember in high-frequency probing is that every part of the measurement setup behaves like a transmission line.

as long as the shortest wavelength of interest. (A handy formula is expressed as wavelength in inches equals 11.8 divided by the frequency in gigahertz.) This limit keeps the inductive effects of the ground wire to a very small value—small enough to disregard in most cases.

Even when you are interested in a relatively low frequency, a scope with a wide-enough bandwidth will reveal the overshoot and ringing that stems from ground-wire inductance. You can eliminate this visual annoyance by either shortening the ground lead, if that's possible, or by using a probe with a narrower bandwidth to filter out the inductive effects. Of course, even the shortest ground lead can produce noticeable effects, depending on the speed of the applied step function and the scope's bandwidth.

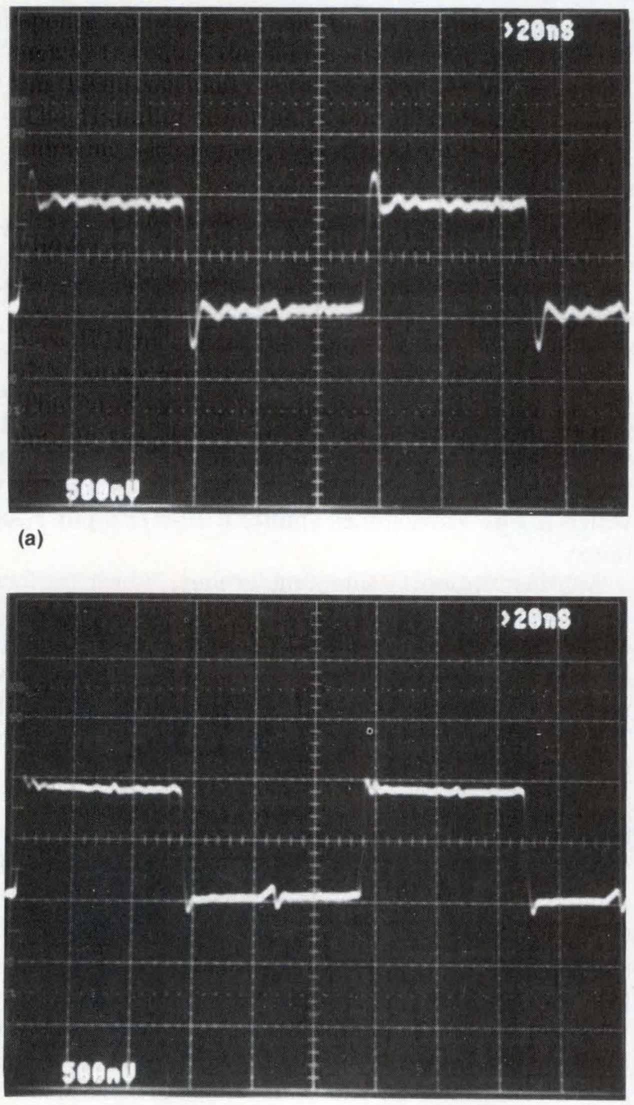


Fig 7—A 3-in. ground lead can degrade a signal from an ECL circuit (a). Shortening the ground lead to ¼ in. on the same probe cleans up the signal significantly (b).

The wavelength of a 500-MHz signal in air is about 24 in., which limits the ground lead to no more than 1.2 in. As frequencies climb higher, the ground lead quickly gets too short to manage with an alligator clip. The frequency components found in ECL devices are pushing the limits of your ability to use one pin of a DIP for grounding while probing the other pins; the ground pin is too far from some of the signal pins to maintain a short enough ground path.

Fig 7 compares the effects of a long-vs-short ground lead on an ECL-generated signal. To avoid the signal degradation illustrated in **Fig 7a,** design your pc boards with ground-plane feedthroughs next to every pin that you might want to probe. This approach might seem extreme, but if you don't use it, you won't get an accurate view of activity at frequencies much above 500 MHz.

Whatever type of probe you choose, don't forget that you have to combine it with an oscilloscope to furnish the required bandwidth. It's important to remember that the bandwidths of the probe, the scope, and the signal source (circuit under test) interact to produce a displayed bandwidth according to the following relationship:

$$\text{displayed BW} = \frac{1}{\sqrt{\left(\frac{1}{\text{scope BW}}\right)^2+\left(\frac{1}{\text{probe BW}}\right)^2+\left(\frac{1}{\text{source BW}}\right)^2}},$$

where BW stands for bandwidth.

Make clean contact

For both the ground connections and the probe tip, it is important at high frequencies to make stable, repeatable contact with the unit under test. Each time you attach a probe to a circuit, the probe's wiping action can cause a variation in the precise point of contact and in the contact resistance. Partially for this reason, you must sometimes use micromanipulators. At lower frequencies, this degree of care isn't required, but it's still important to apply constant pressure to handheld probes and to pay attention to the contact quality.

High-frequency probes designed mainly for wafer probing require special handling. For example, the Picoprobe from GGB Industries (Gilette, NJ) is an

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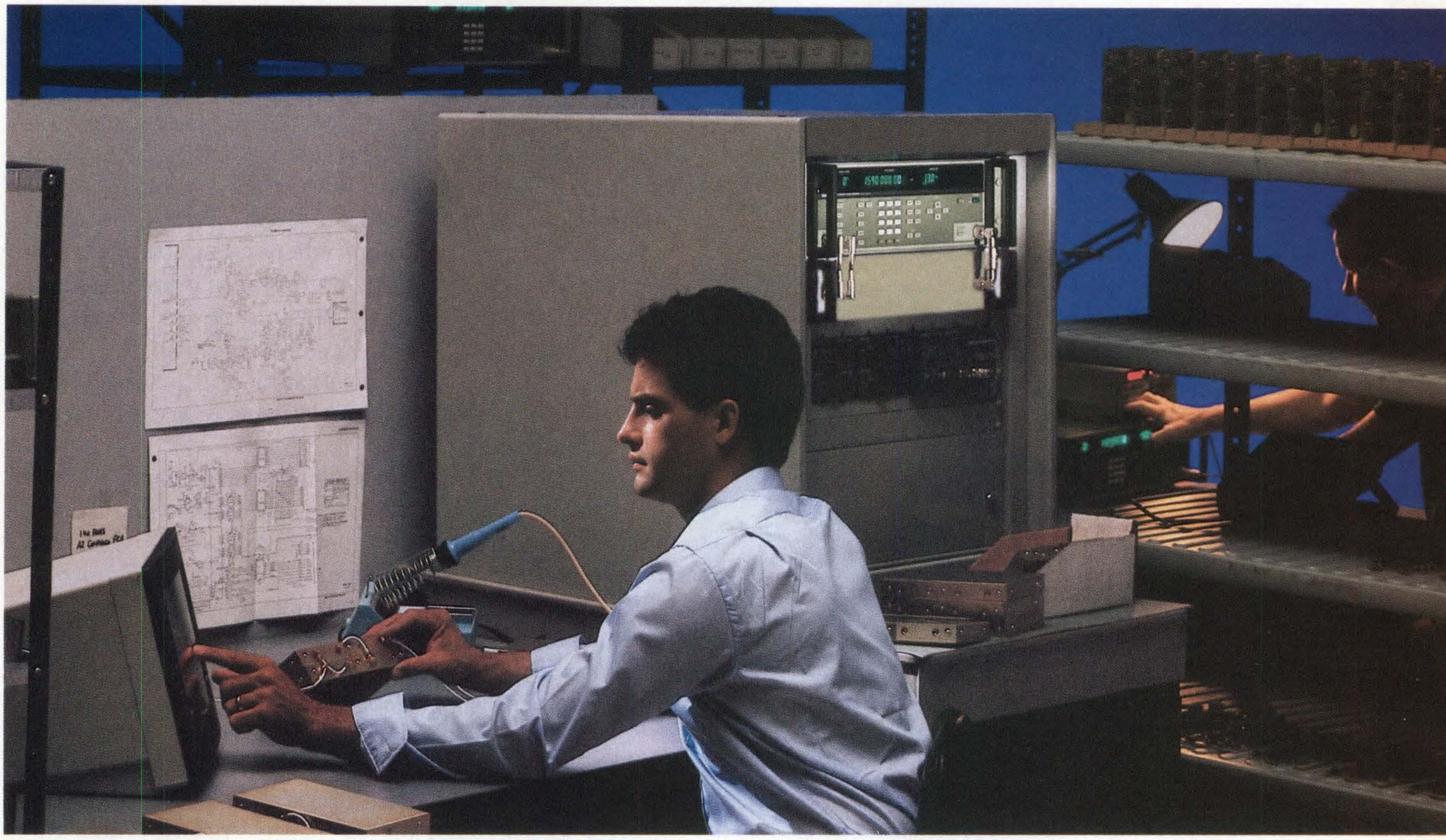

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The biggest contribution to reactive loading comes from the capacitance between the probe's tip and ground sleeve and the probe cable's center conductor and shield.

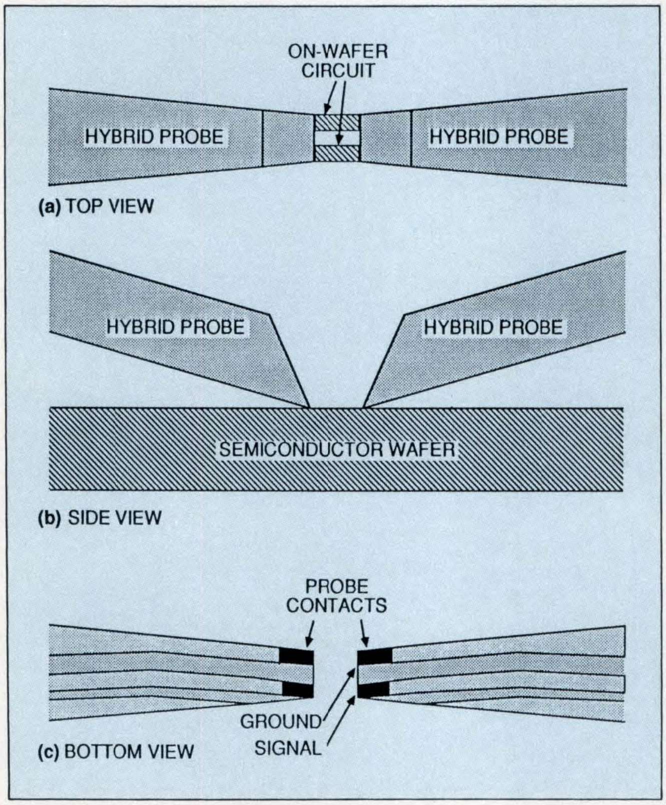


Fig 8—A new type of high-frequency probe *maintains good transmission-line qualities all the way to the probe tip by using tapered parallel strip lines on a ceramic base. The two outside strips are connected to ground.*

active probe that exhibits 0.1 pF at 1 MΩ and has a 500-MHz bandwidth. Micromanipulator Co (Carson City, NV) makes an active probe that exhibits 0.2 pF at 3 MΩ and provides a bandwidth that stretches to 1 GHz. As the company's name suggests, the device requires the use of a micromanipulator, which allows you to place the probe tip on a small contact area without causing damage to the circuit or the fairly delicate probe. In addition, the manipulator's consistent pressure is necessary because the probe's dielectric properties can change with flexing.

If you're interested in what the future might hold for probes suitable for ever-higher frequencies, a series of probes from Cascade Microtech (Beaverton, OR) may provide a clue. These probes allow you to make microwave wafer measurements at frequencies higher than 26 GHz. This phenomenal bandwidth results from the use of a structure that provides a coplanar 50Ω transmission line all the way out to the probe tip (**Fig 8**). It turns out that you can scale a strip-line transmission structure from wide strips to very narrow ones and still maintain a 50Ω line. The tiny amount of reactive loading in this structure is almost entirely inductive.

The Cascade probes aren't a universal solution to probing, of course. They force you to place signal and ground pads side by side at a designated spacing, and each signal source in your circuit must provide a 50Ω termination. Designers of microwave circuits are accustomed to meeting such requirements, but attempting to create a universal probing solution would impose high-frequency circuit layout constraints on low-frequency circuit designers. Nonetheless, at least in the high-frequency world, probe constraints will probably dictate circuit layouts. The alternative is to accept inaccurate measurements.

Instead of buying probes, you can make your own and tune them to some extent to work with your specific circuits. This method is especially effective when you solder several probes to various test points in a prototype circuit—an approach that doesn't suit manufacturing test but is good for research and development. Each probe has its own cable and adapter connector that plugs into the scope when needed. Such a probe can consist simply of a 450Ω film resistor with one end soldered to the board and the other soldered to a coaxial cable's center conductor; the coaxial shield is soldered directly to a ground on the board. You can vary the resistor's value depending on your circuit's impedance, and even insert filter elements for special purposes.

Whether you're constructing or attaching a probe, the crucial factor is still lead length. All unshielded wires must be as short as possible. Also, avoid the clever implementations that others have tried without success: Don't use pogo pins, for example, or other elements that allow lead length and pressure to vary. You won't be happy with the results.

A final important consideration when building a probe, or when connecting a scope cable directly to a connector on the unit under test, is the cable and connector: They may be a source of problems. A coaxial cable made for high-frequency work will have certain specifications—including bandwidth—that tell you how it will suit your application. With any unterminated coaxial cable, the longer the cable, the greater the capacitive loading, and so you should keep the cable as short as possible.

Further, the impedance of a coaxial cable is the result, in part, of the skin effect. High-frequency currents are crowded near the surface of the cable's shield. The skinnier the cable, the more severe the crowding and the greater the skin-effect losses. Thus,

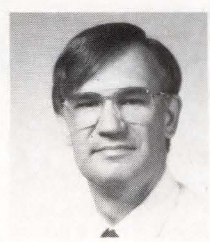
it's best to use coaxial cable with as large a diameter as possible at high frequencies even though it's less convenient to work with. Foam dielectric cables allow for smaller diameters with minimum skin-effect loss.

Some types of connectors can present problems at high frequencies. BNC connectors (as well as BNC cables), for example, tend to drastically degrade signal quality at high frequencies. A better choice is an SMA connector. With any connector, it is crucial that you keep it clean. Even the best connector will ruin your results if it's dirty. If you must disconnect connectors regularly, try to clean them with alcohol every day.

In all probing areas, the unforgiving nature of high frequencies cannot be overstated. To make use of the bandwidth improvements that today's oscilloscopes offer, you have to pay attention to every detail of the connection between the scope and the circuit under test. **EDN**

Authors' biographies

Eldon Walters is marketing product-line manager for sampling products at Tektronix's Laboratory Instruments Div in Beaverton, OR. He has worked for Tektronix for 14 years. He holds an AAET degree from American River College in Sacramento, CA, and a BS in marketing and economics from Portland State University. His leisure activities include photography and baseball.



Stan Kaveckis is a principal engineer at the same company. He holds a BSEE from the University of Washington and has worked at Tektronix for 11 years. Stan is a member of the International Society for Hybrid Microelectronics. When he isn't managing projects at Tektronix, he often works on his personal computer or takes his family on trips to the mountains and ocean.

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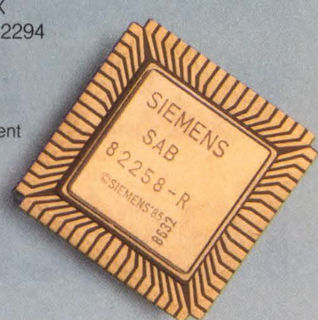

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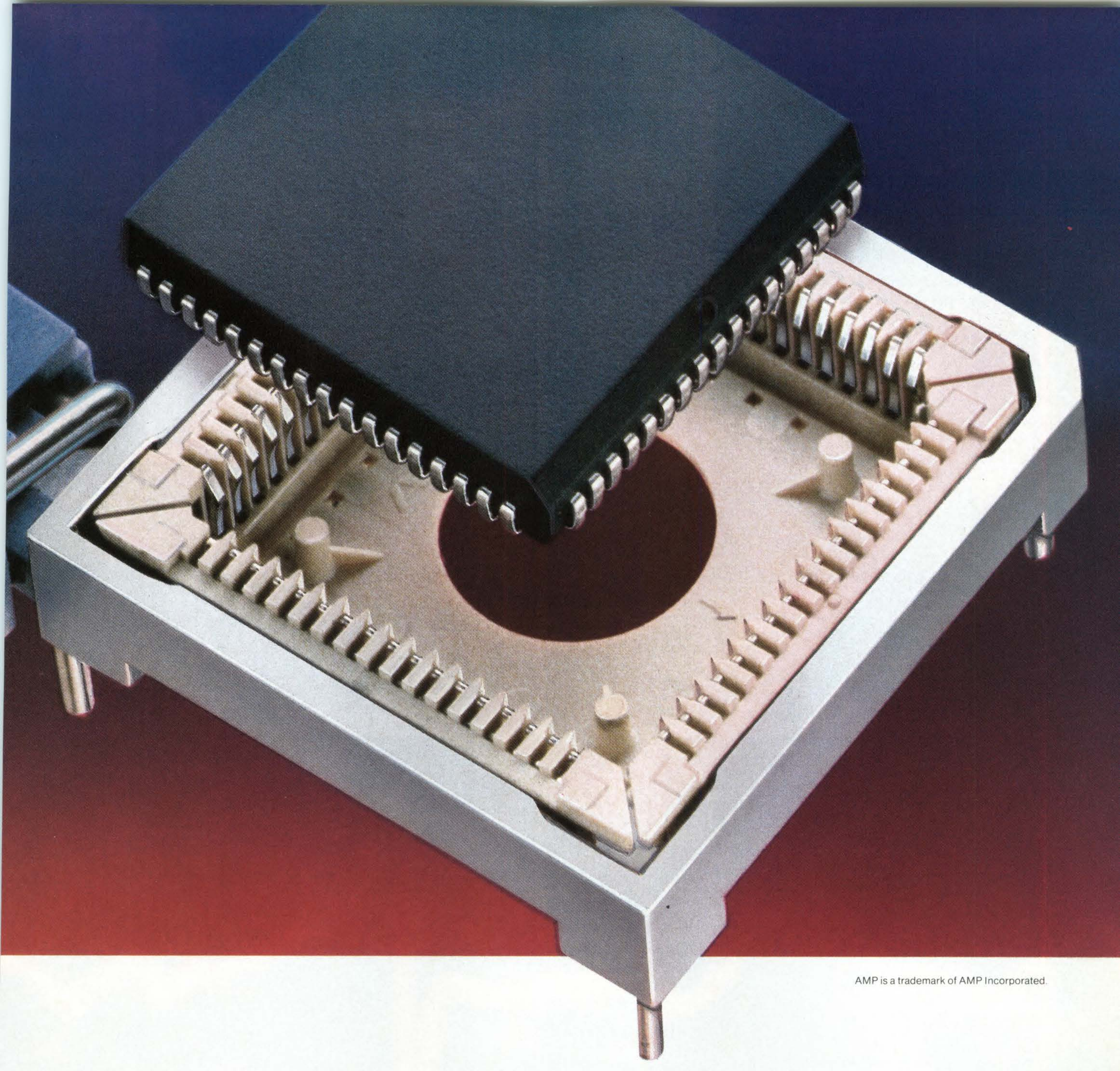

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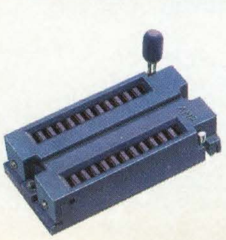

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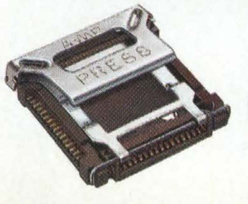

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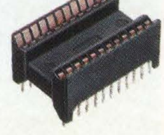

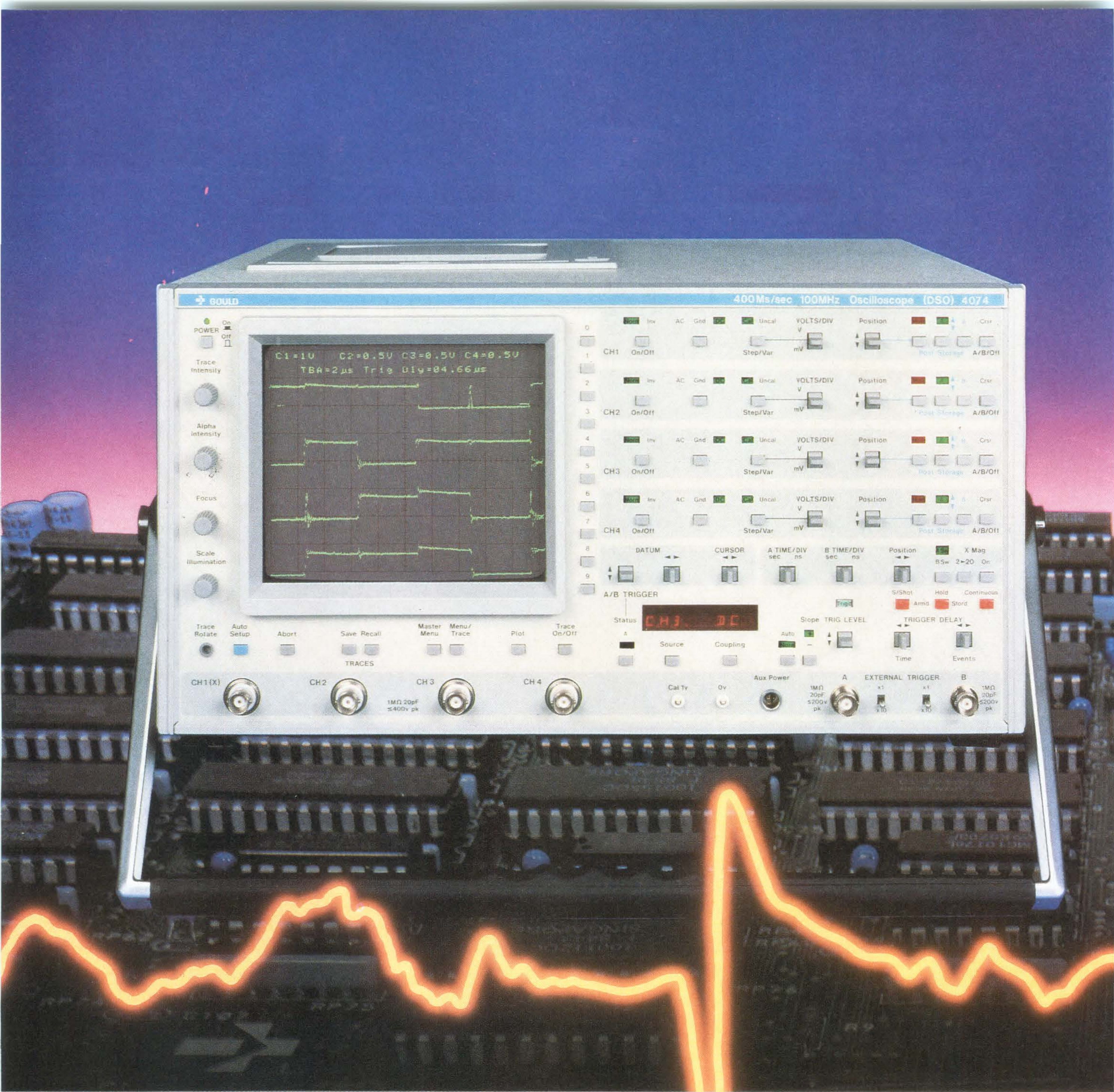
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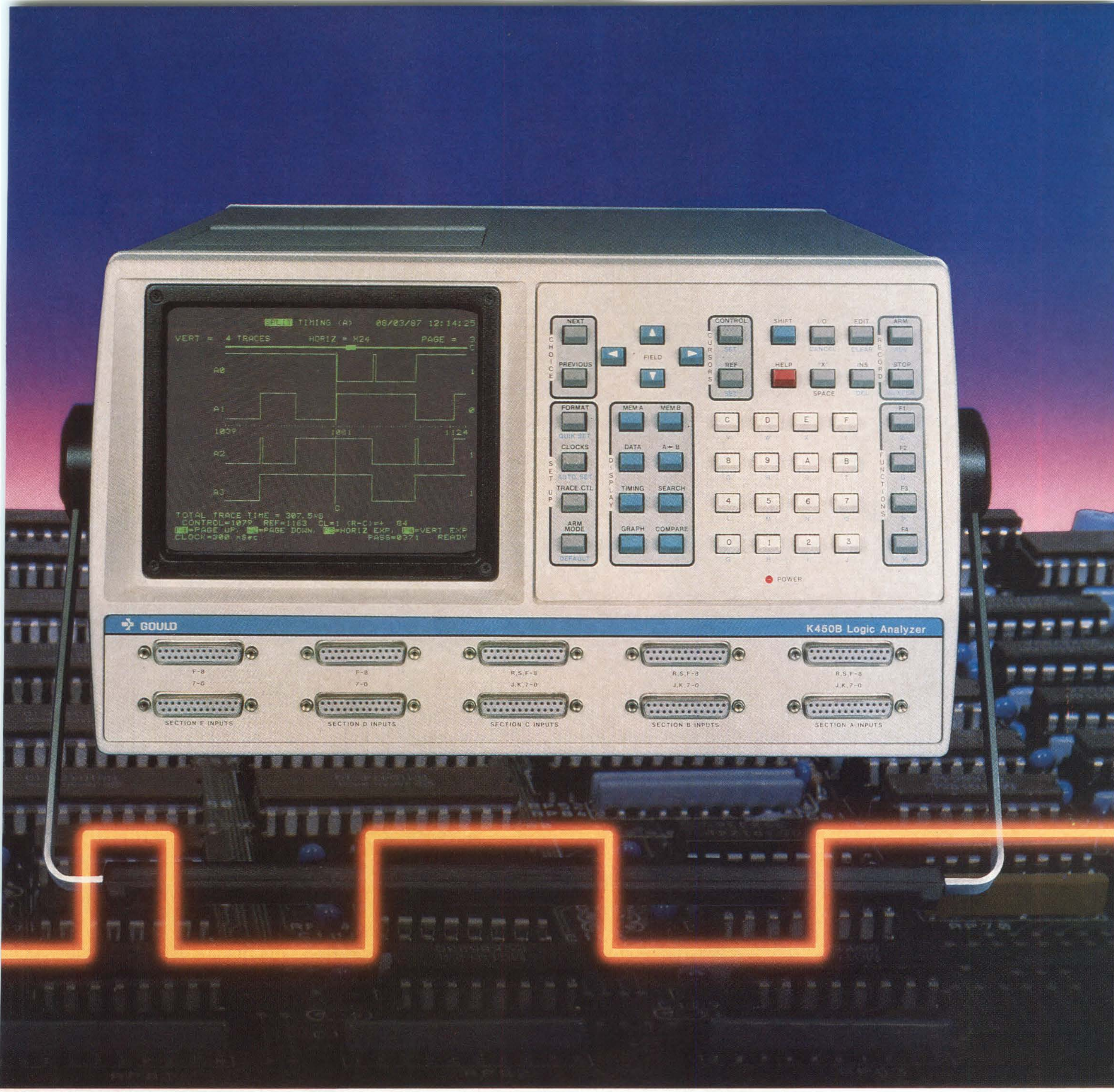

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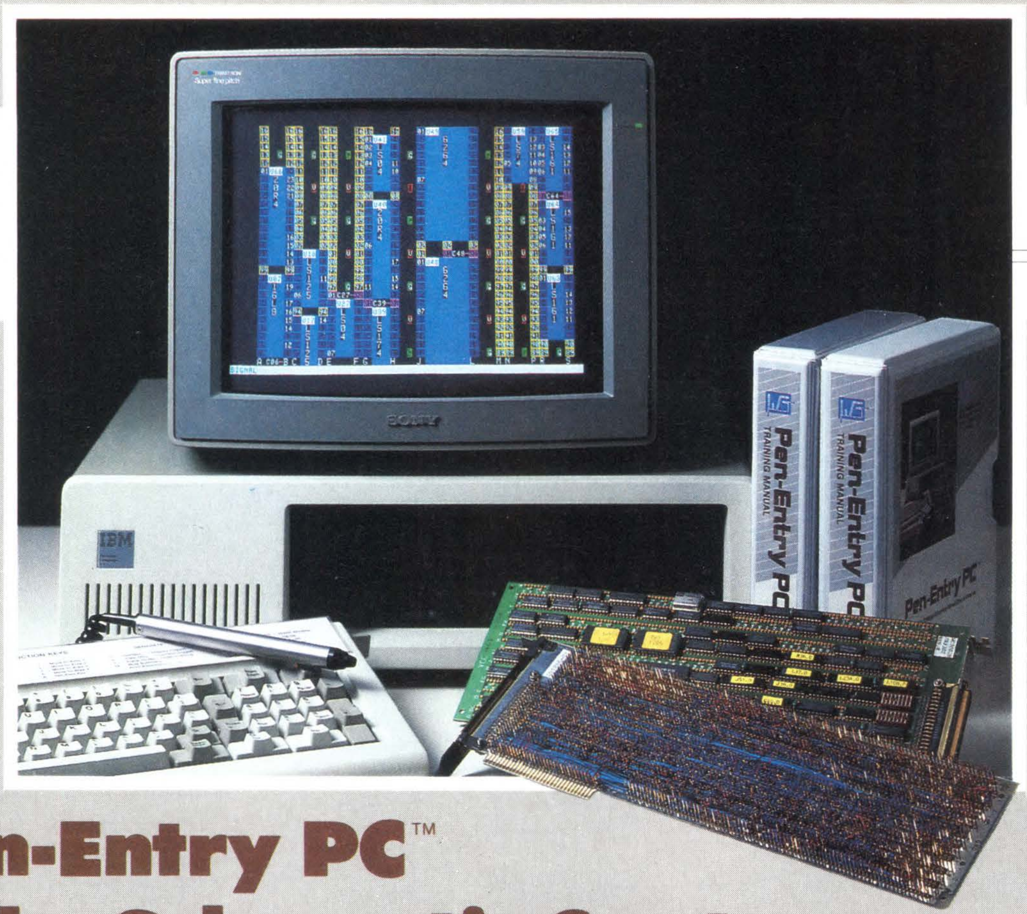
CIRCLE NO 145



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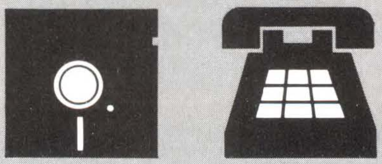

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CIRCLE NO 143

Design rules allow easy wire wrapping of ECL prototypes

When it comes to speed and throughput performance, no logic technology compares to ECL. Ironically, it is ECL's very advantages that have caused some designers to assume that wire wrapping and ECL are incompatible—an assumption that is definitely untrue.

Frank T Reid and Glenn Olsen, *Fairchild Semiconductor Corp*

Once they learn a few simple rules, most logic designers find ECL (emitter-coupled logic) surprisingly easy to handle. ECL takes well to wire-wrapping-type interconnections if you just remember to keep a set of rules in mind. Actually, these guidelines aren't ECL-specific —they apply to the transmission of any fast slewing signals. In fact, ECL is tailored to minimize the system-level problems typically encountered in systems involving high-speed switching.

The myths need to be dispelled

Many designers are put off by ECL because of the misconception that it presents many hard-to-understand and hard-to-implement circuit concepts not found in the world of TTL-compatible ICs. One prevailing myth about designing ECL circuitry is that you must understand transmission-line theory to calculate characteristic impedances and complex terminating load values to realize proper circuit interconnections. Without this understanding, supposedly, it's impossible to fabricate a prototype board that will work properly. Many designers believe that ECL interconnect requirements are so demanding that anyone who tries to wire wrap a prototype panel is asking for trouble.

There's no reason to be scared of transmission-line requirements. Design rules for ECL are no more demanding than those for any other high-speed digital-IC technology. In any high-speed system, you can't ignore the inductance, capacitance, and signal delay inherent in the interconnections. All this means, however, is that you must locate a terminating resistor at the very end of every signal wire to minimize the problems (reflections, ringing, crosstalk, and tight line-length limits) typically encountered in high-speed logic systems. Each resistor should match the characteristic impedance of that particular signal wire.

For a circuit on a board that has good voltage planes, for example, the characteristic impedance of each wire equals that of a wire over a ground plane **(Fig 1a)**. According to the formula in **Fig 1a,** for a 30-gauge wire on a typical wire-wrapped ECL board, the characteris-

Design requirements for ECL are no more demanding than those for any other high-speed digital-IC technology.

tic impedance is 140±50Ω. Many designers assume that they always have to calculate this tricky match, but they don't.

Your ECL vendor can supply recommended values. Over the years, vendors have ascertained the correct terminating-resistor values to achieve the best results —and these values don't have to be very precise. For a wire-wrapped board, the wire's height above the board generally varies between any two connecting points. Because the characteristic impedance of a wire depends on its height above the board, the wire has a varying range of characteristic impedances, and you can't precisely match the wire's impedance. This doesn't matter, though, because slight mismatches don't seem to affect circuit operation. (The most-often-mentioned characteristic impedance for a single-wire interconnection is 100 to 120Ω.)

By using twisted-pair interconnections for all signals, you'll maximize signal integrity, provide some transmission-line compatibility, and facilitate the wire-wrapping process **(Fig 1b)**. For particularly long wiring runs or when you're wiring interconnections from one board to another, it's especially desirable to use twisted-pair wiring. It's most important to use twisted-pair wiring when you have to distribute clock signals over long distances. One design solution, called quarantining, brings the clock signal to a differential receiver located in the middle of the board. You then fan out the receiver's outputs such that all paths to each final receiver are identical.

You'll also find it helpful to use differential circuitry when you're wire wrapping interconnections from board to board. Differential-type devices eliminate many sporadic and transient bugs. The 100K ECL family's outputs are virtually all differential types—and they can readily drive twisted-pair lines.

Quite often a board-to-board voltage differential exists, even when the system boards' voltage planes have been thoroughly bypassed. With a differential receiver, the boards in the system can have slightly different voltage-plane levels without causing problems; the differential receiver's common-mode rejection capability substantially reduces any sensitivity to such discrepancies. In addition, the characteristic impedance is usually more uniform for boards that are separated by lengthy distances, and the use of twisted-pair wiring tends to balance out noise picked up on the lines.

If you do decide to string single wires over shorter distances for less-critical signals, keep the wire at a uniform height above the board's ground plane. A wire that starts at a particular level on one wire-wrapped pin should go to the same level on the pin at the other end **(Fig 2)**.

This practice provides an additional bonus—it makes it easier to make wiring changes. If you have to remove a pin from a string, you'll only have to remove the two wires connected to that pin and then reconnect them with a new wrap. If you don't keep wires at the same level, you'll have to pull off every wire on the pins at both ends of the run and then rewrap them all.

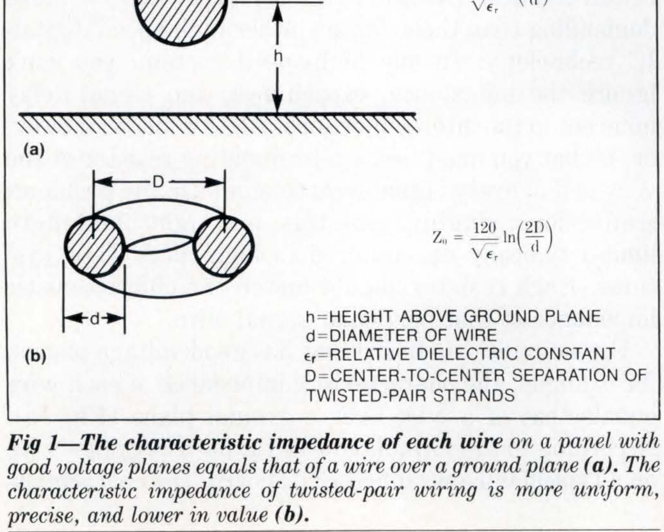


Fig 1—The characteristic impedance of each wire *on a panel with good voltage planes equals that of a wire over a ground plane* ***(a)***. *The characteristic impedance of twisted-pair wiring is more uniform, precise, and lower in value* ***(b)***.

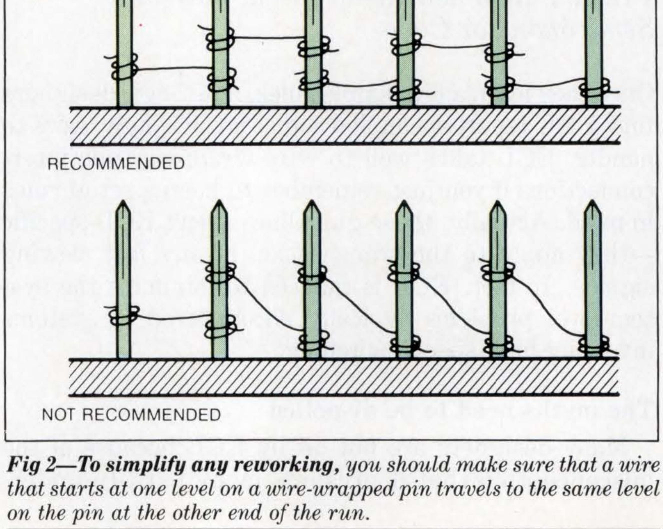


Fig 2—To simplify any reworking, *you should make sure that a wire that starts at one level on a wire-wrapped pin travels to the same level on the pin at the other end of the run.*

To minimize signal delays, you should also pay attention to your layout techniques. Wiring a driver output to various receivers in a daisy-chain sequence instead of a star-type configuration will prove effective, for instance. With a daisy chain, you only need a single terminating resistor at the far end; with a star, you need a resistor at the end of each spoke to make sure the spoke doesn't look like an open-ended stub, which could produce disruptive reflections and ringing. For a fanout of three, wrap driver to receiver to receiver to terminator. Fortunately, virtually any ECL output can drive a 50Ω line directly, so a driver can handle two properly terminated 100Ω lines going to different locations.

Special circuit boards are available

Selecting a wire-wrapping panel designed to accommodate ECL circuitry will enhance your prototyping efforts. A number of manufacturers offer wire-wrappable panels designed for ECL, including Augat, Garry, and Mupac. These special boards provide three power planes—one each for V_{EE}, V_{CC}, and V_{TT} **(Fig 3a)**. Each plane occupies more than 50% of the board area at its level; that figure can approach 80% in a well-laid-out board.

With ECL, the V_{CC} plane is actually 0V or ground. This plane provides the best coverage and shielding; ECL performance degrades badly when the power plane is inadequate. For this reason, some ECL boards (Augat's, for example) have a fourth plane that connects to V_{CC} **(Fig 3b)**. The V_{EE} plane goes to the −5.2V main power source, and the V_{TT} plane serves as the terminating resistor return (normally specified as −2V).

No matter which voltage level a plane supplies, it should be essentially at ground for ac. All ECL planes should have very low impedance between them to help decouple the circuits drawing power from the planes. The power planes' large area and close spacing, as well as their high-dielectric-constant substrate material, provide good capacitance paths between the planes, especially at high frequencies. By grounding the planes for ac signals, you'll help prevent cross coupling of noise and current spikes in the power sources.

Good practice dictates that you use a 0.1-μF disk capacitor (which has low internal inductance) to bypass V_{CC} and V_{EE} at every ECL device on the board. You should also mount larger tantalum electrolytic capacitors (25 μF, for instance) where these two voltages enter the board. It helps to mount large electrolytics at several other locations to decouple the lower frequencies. These precautions will help to prevent noise on the power planes from confusing the logic.

For the same reason, you should pay extra attention to the pins that connect to the power planes. These pins should be soldered rather than just wire wrapped. The power pins must have a very low resistance joint because they carry substantial current; good joints will keep any noise from current spikes low.

Ignore the rules at your own peril

It's paramount that you properly terminate the interconnecting wires in a high-speed ECL system. To illustrate what can happen if you don't, consider a step-voltage signal whose leading edge is very steep (100K ECL's is 0.7 nsec) and which is impressed on a transmission line that is relatively long for the signal rise time (the critical length is more than 3 in.).

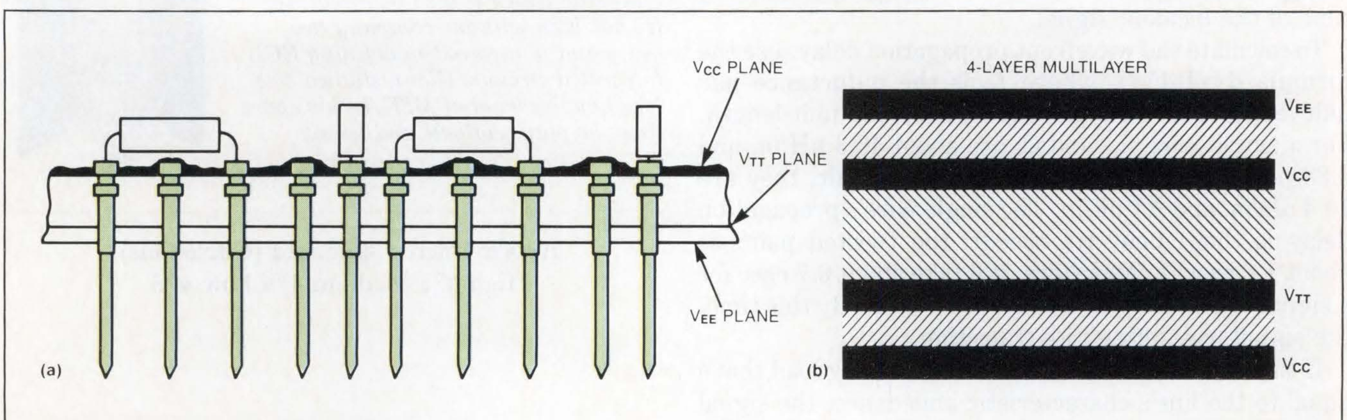


Fig 3—To accommodate the needs of ECL circuit designers, *some manufacturers offer panels that have three voltage planes—one each for V_{CC}, V_{TT}, and V_{EE}* ***(a)****. Some also offer boards that have a fourth voltage plane* ***(b)****, which you normally connect to V_{CC}.*

A wire that starts at a particular level on one wire-wrapped pin should travel to the same level on the pin at the other end of the run.

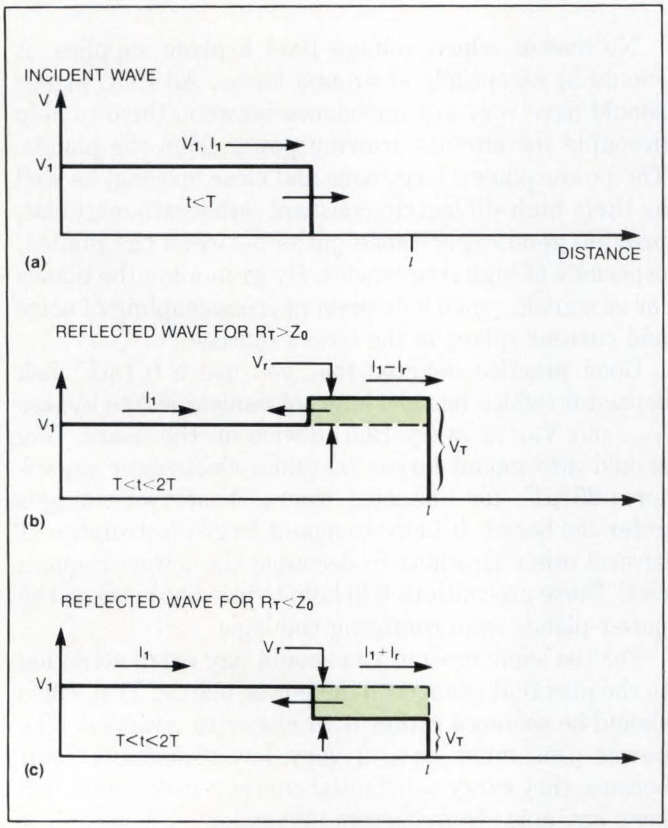


***Fig 4—Line terminations won't have any effect** on initial current flow impressed on a transmission line that is relatively long for the signal rise time **(a)**. For shorter lines that are improperly terminated, the reflected wave will either add **(b)** or subtract **(c)** from the incident wave, depending on whether the reflected wave is in phase or out of phase.*

Initially, the termination at the far end of the line has no effect on the current that flows into the line **(Fig 4a)**. Any signal reflections from the far end haven't had enough time to get there and back during the transition time of the incident signal.

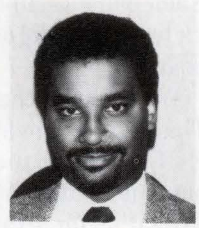
To calculate the wavefront propagation delay, use the formula $d=(L_0C_0)^{1/2}$, where L_0 is the inductance per unit-length and C_0 is the capacitance per unit-length. For a single wire, L_0 and C_0 are about 16.3 nH/in. and 0.83 pF/in., respectively. For a twisted pair, they are 10.4 nH/in. and 2.1 pF/in. The single wire's propagation delay is thus about 1.4 nsec/ft; the twisted pair's is about 1.8 nsec/ft. Therefore, it'll take about 0.7 nsec for a signal to travel down the wire and back. By this time, the signal has finished its transition.

If the far end of the line has a terminating load that's equal to the line's characteristic impedance, the signal is totally absorbed when it reaches the load, and there's no reflected energy. The signal thinks it is traveling forever on an infinitely long, uniform transmission line.

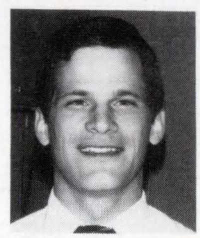
If the line isn't properly terminated, reflections will occur according to the formula $p=[(R_T-Z_0)/R_T+Z_0]\times 100\%$, where p is the percentage of signal reflection, R_T is the terminating resistance, and Z_0 is the line's characteristic impedance. When R_T is greater than Z_0, the reflected wave comes back in phase and adds to the incident wave **(Fig 4b)**. When R_T is less than Z_0, the reflected wave is out of phase and subtracts from the incident signal **(Fig 4c)**.

On long lines, end-of-line reflections come back after the initial signal transition is complete. A mismatch between the line driver and the line's input end will also reflect any signal returning from the far end of the line. Multiple reflections due to a mismatch at both ends of the line will generate ringing that lasts until the system's resistance damps it out. Large reflections and ringing can cause ambiguous logic-circuit behavior during periods when the signal should be stable or show no transition—which is obviously undesirable. **EDN**

Authors' biographies



Frank Reid is a senior product-planning engineer at the Custom and Microprocessor Div of Fairchild Semiconductor Corp in Puyallup, WA. In this position, Frank is responsible for ECL LSI product definition. He holds an ScB degree from Brown University and is a member of the IEEE and the Association for Computing Machinery. Besides engineering, Frank enjoys basketball, tennis, and bicycling.



Glenn Olsen is a product-planning engineer at Fairchild's Asia and Memory Unit Div, which is also in Puyallup. He has been with the company two years and is involved in defining ECL integrated circuits. Glenn studied electrical engineering at MIT. In his spare time, he plays softball and tennis.

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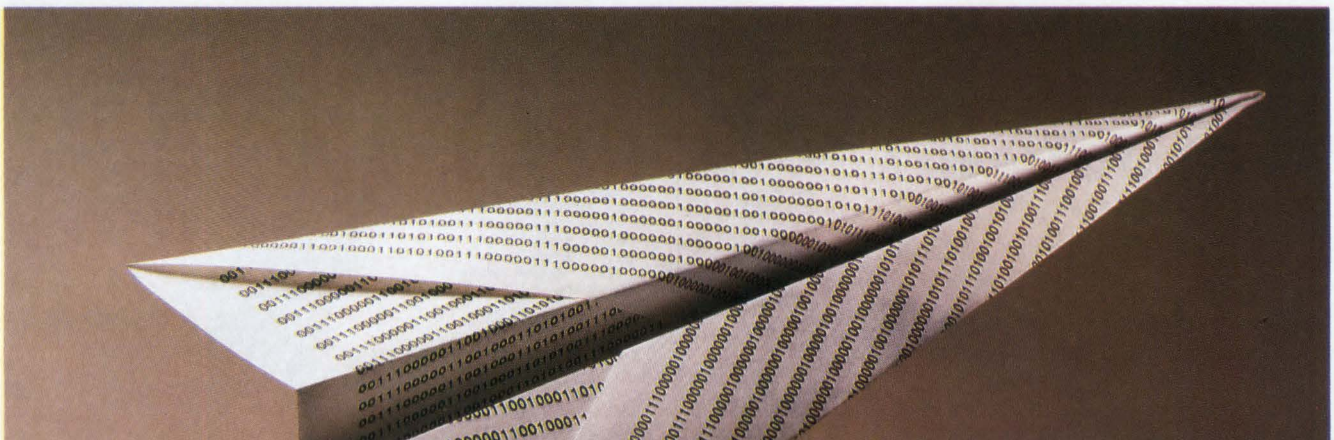

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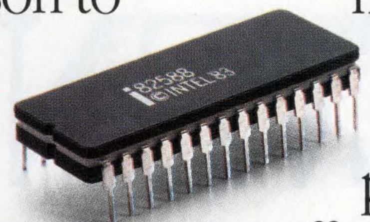

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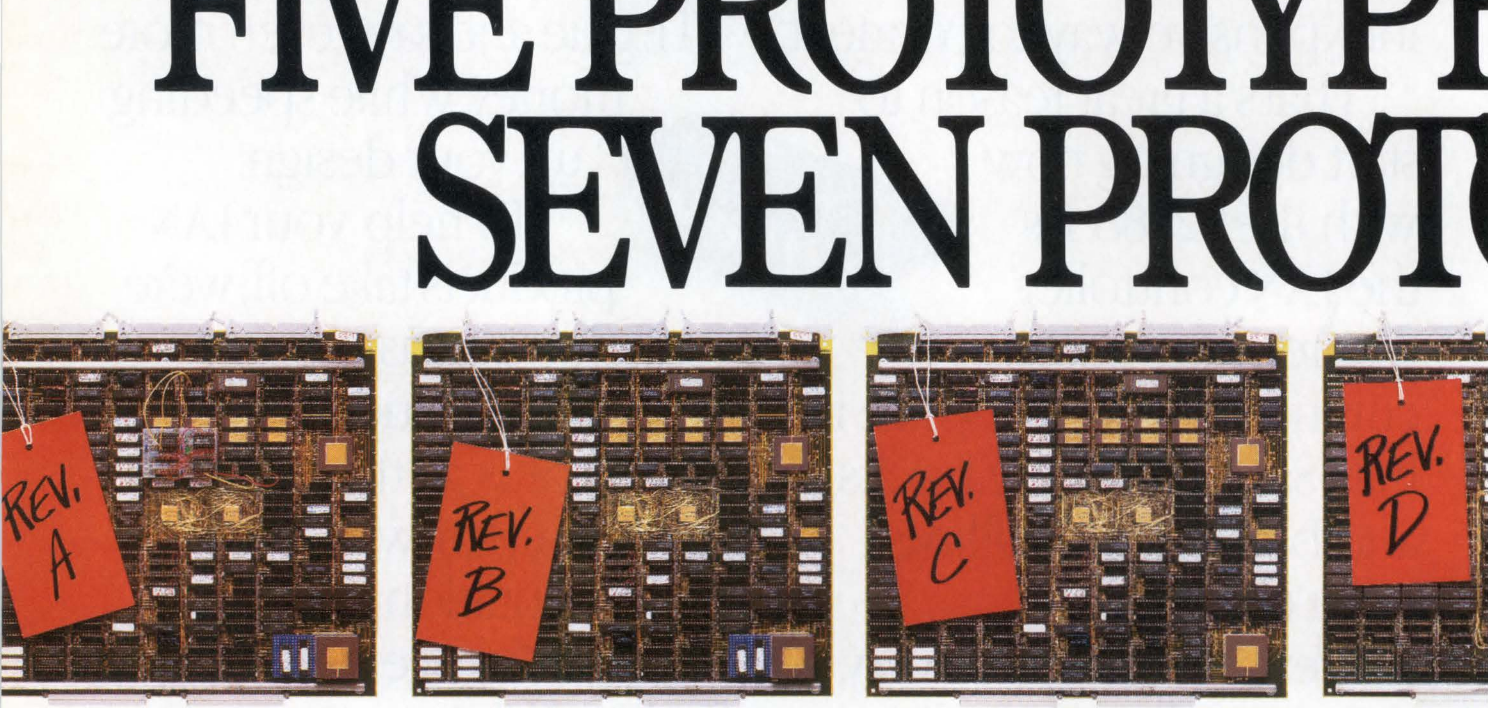

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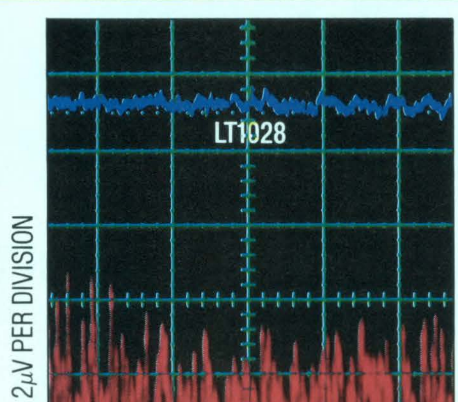

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Digital ICs form programmable divider

Steve Lubs
Dept of Defense, Washington, DC

The **Fig 1** circuit divides the input clock frequency by an integer between 2 and N (N=8 in this case). You select the integer by applying a 3-bit word at the divisor-control inputs.

IC_1 and IC_2 form an 8-bit shift register. These cascaded ICs either shift their output data to the right or load input data in parallel: When S1 (pin 10) is high, the chips load the A through D inputs (pins 3 through 6) on a positive transition of the input clock. When S1 is low, each positive clock transition causes the chips to shift their output data (which appears on Q_A through Q_D) to the right. Multiplexer IC_3 selects one of its eight inputs according to the 3-bit divisor-control input, and the multiplexer's output drives the S1 inputs of IC_1 and IC_2.

During operation, the circuit's output goes high for one clock cycle, causing the shift register to load the input word 10000000. Succeeding clock cycles shift the input word's single 1 to the right until it enters the selected IC_3 input. The resulting output pulse loads the shift register with another 10000000, which reinitiates the cycle. Coincident with each parallel-load operation, the circuit consisting of IC_4, IC_5, and IC_6 presents a 1 to the shift register's D_{SR} input, ensuring continued operation in the event that a malfunction clears the shift register.

The circuit can operate at 50 MHz if you use high-speed devices such as ones from Fairchild's Fast Series. You can obtain larger divisors by increasing the number of shift-register stages. Adding another multiplexer, however, lowers the system clock rate. **EDN**

To Vote For This Design, Circle No 746

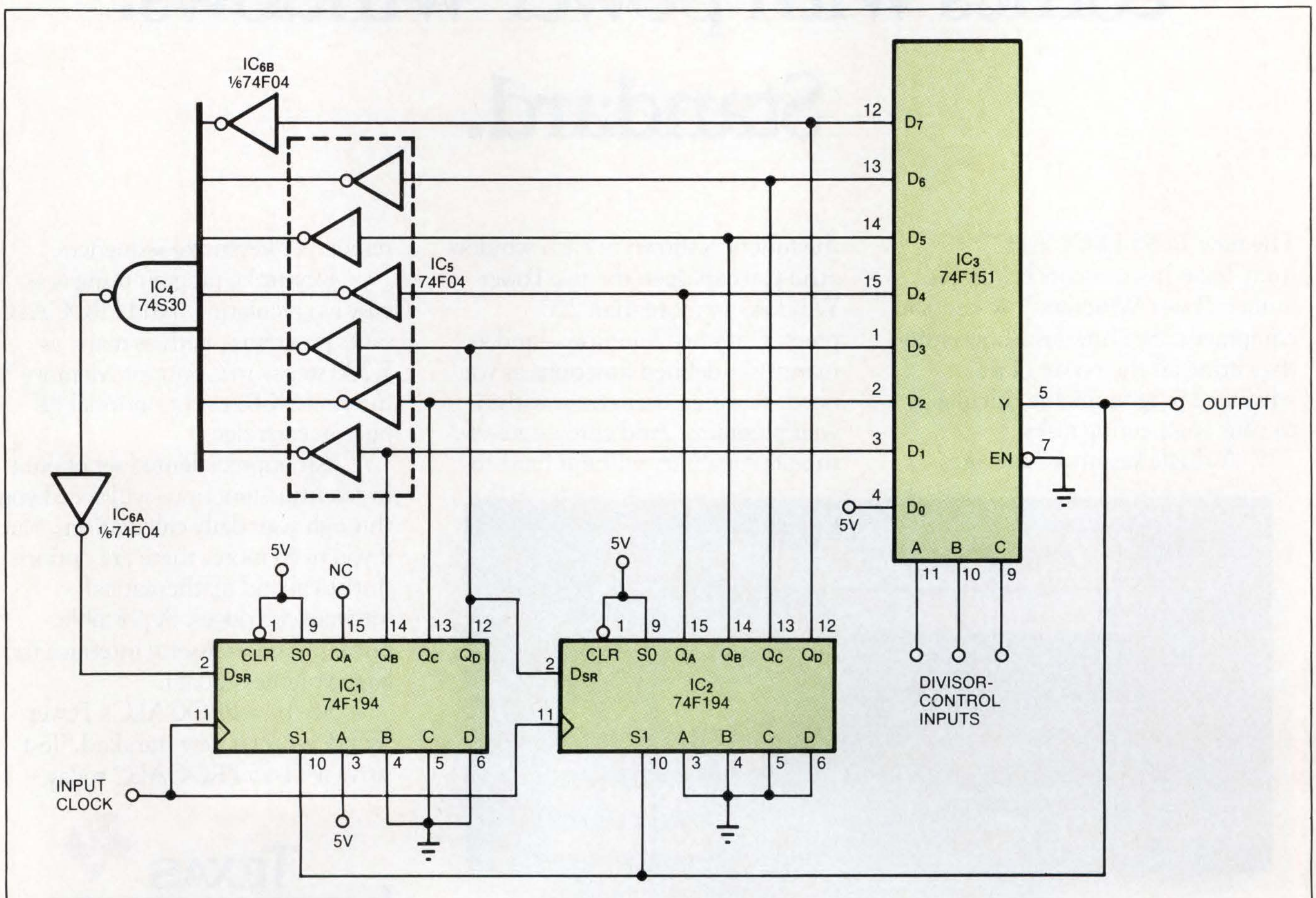

__Fig 1—Two universal shift registers__ (IC_1 and IC_2) and a 1-of-8 data selector (IC_3) form a programmable divider; IC_4, IC_5, and IC_6 provide a backup function for the divider's operation.

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TEXAS INSTRUMENTS

Run Z80 software on an 8085 system

Leo M Almazan
Naval Ocean Systems Center, San Diego, CA

The **Fig 1** circuit shows how to convert an 8085-based μP system to one that runs Z80 software. The scheme involves replacing the 8085 with an NSC800 μP. (The NSC800 is similar to the Z80 internally but has the same bus structure as the 8085). The resulting system is advantageous for those who would rather program for the Z80 than for the 8085.

The main external difference in the Z80 (NSC800) and 8085 μP is the latter's serial-I/O lines SID and SOD; no Z80 instructions can implement these functions. In addition, two discrepancies concern the programmer: The 8085 Trap (nonmaskable-interrupt) input causes a jump to location 24_{HEX1}; the NSC800 equivalent input NMI causes a jump to location 66_{HEX}. Finally, the NSC800 control register for internal interrupts is located at $0BB_{HEX}$, so that address must be free to service a mode-2 interrupt request. **EDN**

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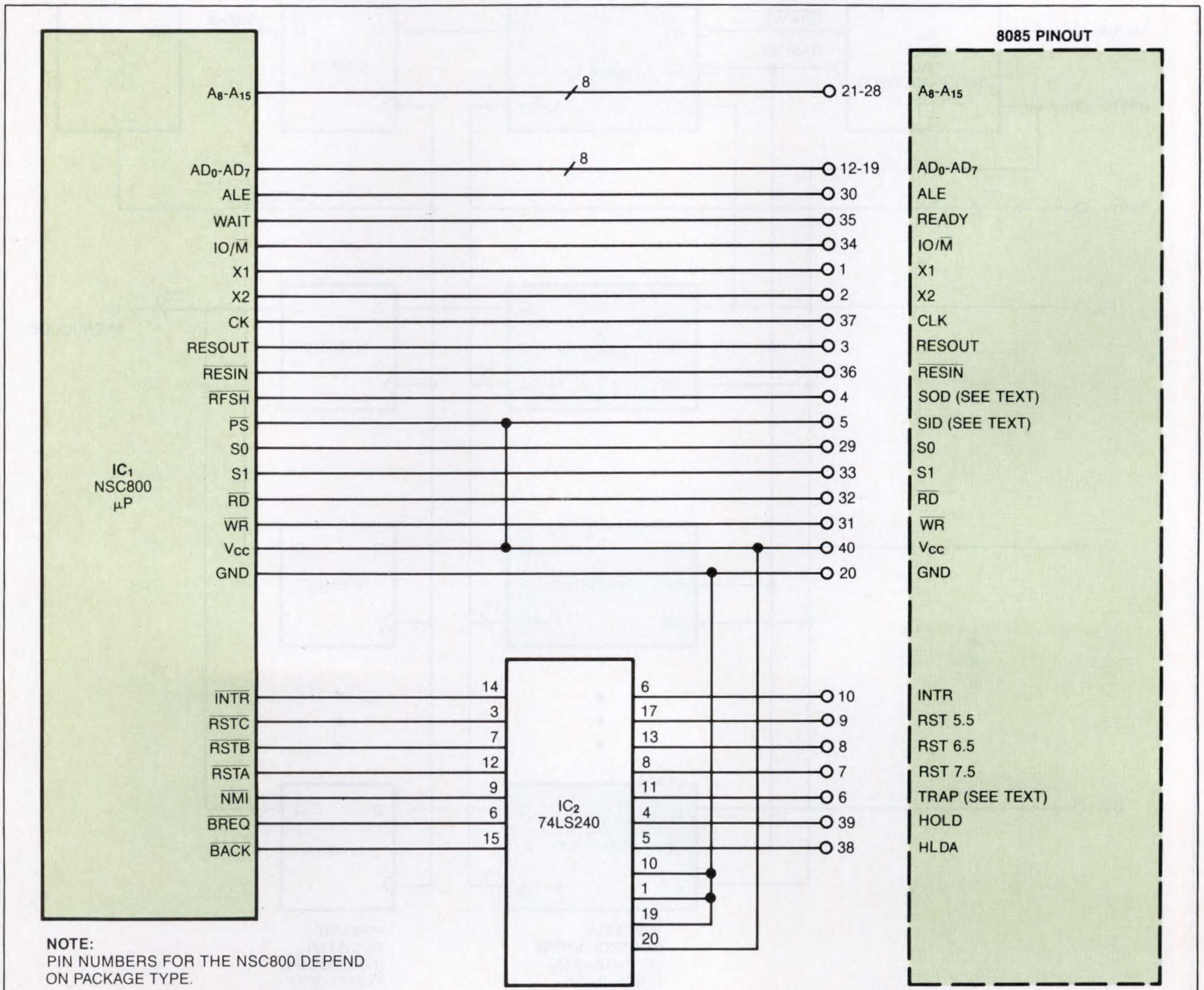

***Fig 1—This circuit lets you substitute** the Z80-like NSC800 for an 8085 μP and thereby obtain a system that can develop and run Z80 software.*

Shadow memory offers microcode breakpoints

Jo Gent
BBN Communications Corp, Billerica, MA

In **Fig 1**, a 16k×1-bit RAM chip (break RAM IC_2) lets you set an unlimited number of breakpoints for a 16k×32-bit writable control store. You write a 1 (bit D_0) to the break-RAM location corresponding to any control-store address for which you want a breakpoint. IC_1 provides IC_2 with a separate Write Enable ($\overline{BRKWE}$) signal that lets you write the breakpoint separately from the data bit D_0, which goes into IC_3.

The signal $\overline{RAMSEL}$ lets the system read all RAM chips in parallel, including the break RAM, and IC_4 samples the Break signal at each address. When IC_4 encounters a breakpoint, it stops the system by turning off SYSCLK. The system dedicates a 16k-byte address area to the break RAM. **EDN**

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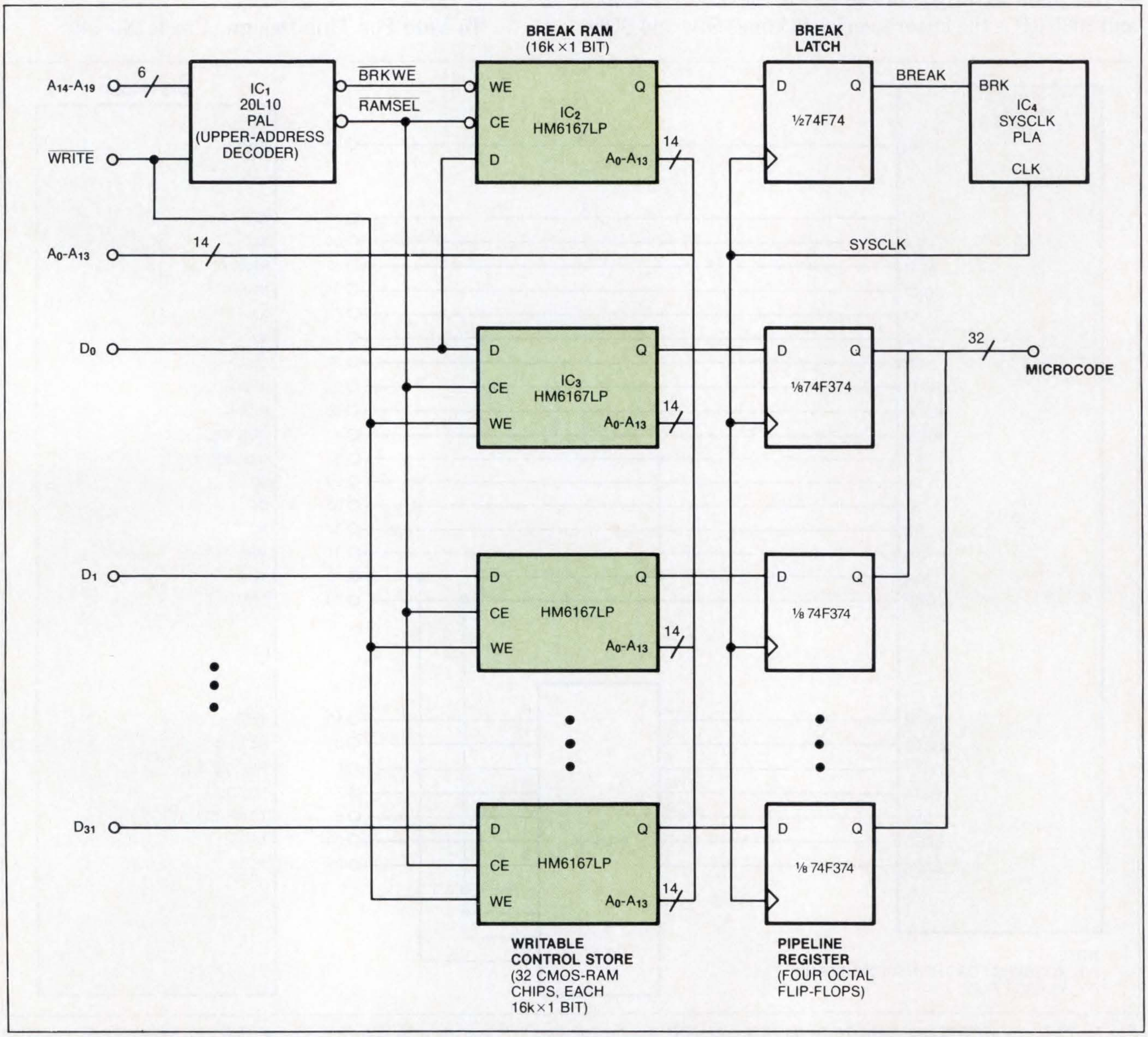

***Fig 1—The RAM chip (IC_2) stores breakpoints** for any number of addresses within the 16k×32-bit writable control store.*

Multiplex circuit adds peripheral options

Mike Ruhland
Motorola Microprocessor Products Group, Austin, TX

The 68000, 68HC000, and 68010 μPs include logic that allows a direct connection to M6800 peripherals that have a nonmultiplexed address and data bus. By creating a local multiplexed bus **(Fig 1a)**, you can also make use of multiplexed-bus peripherals such as the MCM68HC34 dual-port RAM, the MC146818 real-time clock, and the MC146823 parallel interface.

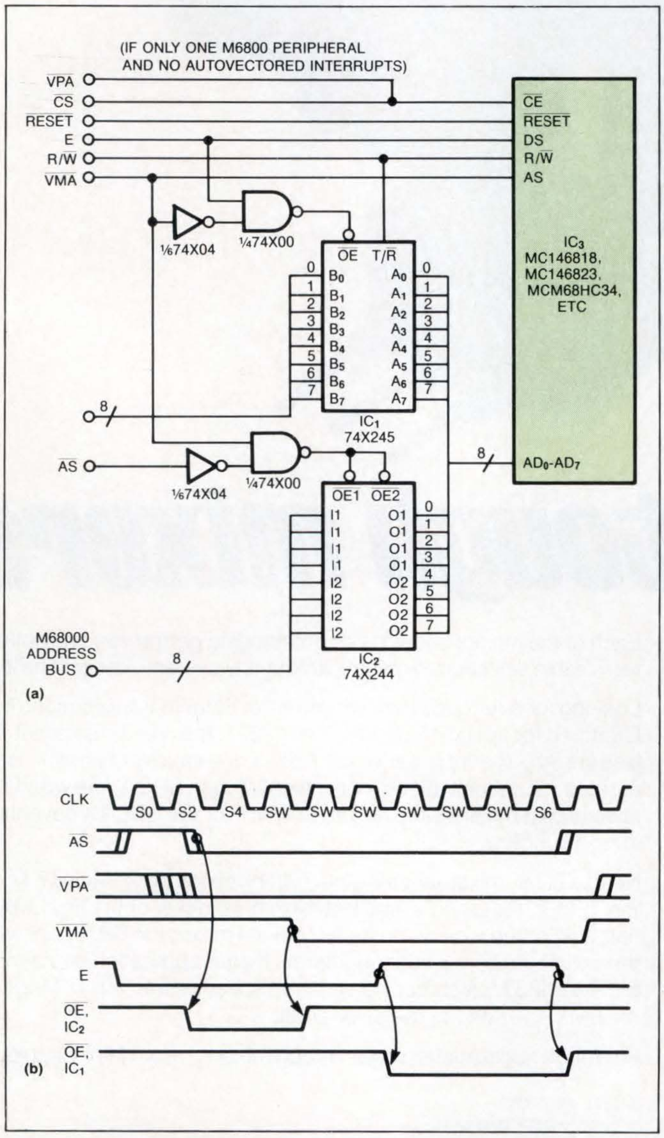

*Fig 1—**By demultiplexing the data/address bus** of a multiplexed-bus M6800 peripheral, you can provide an interface to the nonmultiplexed buses of a 68000-type μP.*

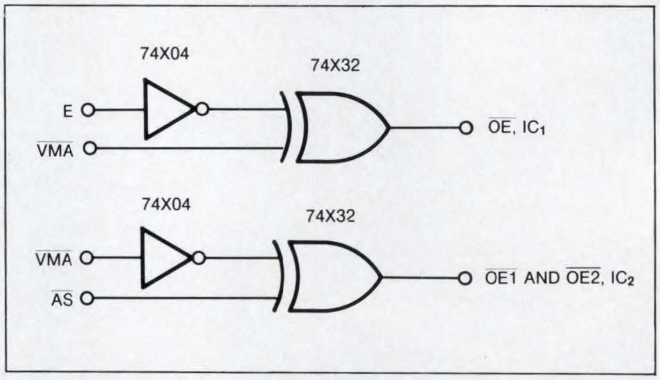

*Fig 2—**These circuits show an alternate way** to derive the output-enable (OE) signals required for buffers IC_1 and IC_2 in **Fig 1**.*

If spare gates are available, the multiplexed-bus interface requires only the additional buffer chips IC_1 and IC_2. You can derive control signals for the buffers by using NAND gates and inverters as shown in **Fig 1**, by using equivalent circuits based on OR gates **(Fig 2)**, or by using a mixture of the two as dictated by the types of spare gates available.

The μP signal $\overline{CS}$ is active low when the address bus points to one or more M6800 peripherals. If the system doesn't use autovectored interrupts and has no other M6800 peripherals, you can connect $\overline{CS}$ directly to the processor's $\overline{VPA}$ pin. Otherwise, you must combine the autovector signal and the $\overline{CS}$ signals from the other M6800 peripherals using additional logic (such as an AND gate). If the system has multiple, multiplexed-bus M6800 peripherals, you can use the same multiplexed bus and connect different $\overline{CS}$ signals to each device.

The resulting multiplexed-bus timing appears as in **Fig 1b** regardless of the control method. At the beginning of every bus cycle, signals from the M68000 address bus pass through buffer IC_2. If addressed, the peripheral asserts $\overline{VPA}$ and, in turn, the processor latches the peripheral's address by asserting $\overline{VMA}$. The control logic then turns off buffer IC_2.

After approximately two cycles of the CPU clock, the E signal goes high and turns on buffer IC_1. The E signal goes low after approximately four cycles of the CPU clock and, for a write operation, causes the peripheral to latch data. Finally, the control logic turns off IC_1. **EDN**

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	Z8002		X	X	X	
	Z8005		X			
	Z8030 Z-SCC		X	X		
	Z8530 SCC		X	X		
	Z8036 Z-CIO		X	X		
	Z8536 CIO		X	X		
	Z8581 CGC		X	X		
	Z8038 FIO		X			
8-BIT	Z280		△			C
	Z180		△			
	Z80		X	△	X	
	Z8420 PIO		X	X		
	Z8430 CTC		X	X		
	Z8440 SIO		X	△		
	Z8441 SIO		X	△		
	Z8442 SIO		X	X		
	Z8444 SIO		X	△		
	SUPER8		△			FORTH
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Software RAM refresh cuts parts count

John W Lydic Jr
Industrial Data Technologies, Westerville, OH

The advent of powerful and inexpensive μPs has allowed the use of software in place of hardware for the execution of various tasks. **Listing 1,** for example, is a software routine that provides an 8-bit dynamic-RAM refresh for systems based on μPs in the 68000 family. This software approach uses slightly more processor time but substantially fewer components than an equivalent hardware solution.

Listing 1 is based on the 68000-type processors' move-multiple instruction and their capability for manipulating the stack pointer. The routine presets the amount of dummy data to be moved by manipulating the stack pointer, and it uses the move-multiple instruction (four bytes from EPROM) to access as many as 128 dynamic-RAM addresses. For a 10-MHz processor and no-wait states, the routine consumes 134 μsec every 4.096 msec—a 3.27% overhead. By comparison, the hardware approach requires an overhead of 1.2 to 1.8%.

The routine first stacks the eight data registers and

LISTING 1—DYNAMIC-RAM REFRESH ROUTINE

```
*--*
*     This algorithm will refresh 64k or 256k drams on the 68000
*     It is invoked by the initialization software to fake an exception
*
*     Note: For 68010 or 68020 the exception stack frame is different
*           and must be accounted for in this code.
*
*--*
           SRefresh
0000 40e7                move.w   sr,-(a7)          stack the status register

*--*
*     This algorithm will refresh 64k or 256k drams on the 68000
*     It is invoked by the hardware every 4 ms
*--*
           Refresh
0002 48e7                movem.l  d0-d7/a0-a6,-(a7) plus exception does 32 of 256
     fffe
0006 9ffc                sub.l    #448,a7           index the stack for 224 words)
     000001c0
000c 4cdf                movem.l  (a7)+,d0-d7/a0-a6 062/256   ( 60 bytes)
     7fff
0010 4cdf                movem.l  (a7)+,d0-d7/a0-a6 092/256   (120 bytes)
     7fff
0014 4cdf                movem.l  (a7)+,d0-d7/a0-a6 122/256   (180 bytes)
     7fff
0018 4cdf                movem.l  (a7)+,d0-d7/a0-a6 152/256   (240 bytes)
     7fff
001c 4cdf                movem.l  (a7)+,d0-d7/a0-a6 182/256   (300 bytes)
     7fff
0020 4cdf                movem.l  (a7)+,d0-d7/a0-a6 212/256   (360 bytes)
     7fff
0024 4cdf                movem.l  (a7)+,d0-d7/a0-a6 242/256   (420 bytes)
     7fff
0028 4cdf                movem.l  (a7)+,d0-d6       256/256   (448 bytes)
     007f
002c 4cdf                movem.l  (a7)+,d0-d7/a0-a6 restore & return
     7fff
0030 4e73                rte
```

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NEC	μPD70108/116 (V20/30)	DIP40P	○	
	μPD70208/216 (V40/50)	PGA	○	
MOTOROLA	MC68000	DIP64P,PGA68P		○

PROCESSOR (8bit)		PKG	SA2000
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	Z80H (Z80, Z80A, Z80B, Z80H)	DIP40P	○
	Z8 (Z8601/03/11/13-12R)	DIP40P	○
	SUPER-8 (Z8310-33)	DIP40/48P	○
INTEL	80C85, 8085AH-2	DIP40P	○
	8048 (8035/39/40/49/50AH)	DIP40P	○
	8051 (8031/51AH, 80C51)	DIP40P	○
MOTOROLA	MC6801 (6801/03-1)	DIP40P	○
	MC6809 (68A09, 68809)	DIP40P	○
	MC6809E (68A09E, 68B09E)	DIP40P	○
	MC68HC11	DIP48P	○
HITACHI	HD6301V/6303R, HD63701V	DIP40P	○
	HD6301X/6303X, HD63701X	SDIP64P	○
	HD6301Y/6303Y, HD63701Y	SDIP64P	○
	HD6305U/V, HD63705V	DIP40P	○
	HD6305X/Y	SDIP64P	○
	HD6305Z, HD63705Z	FLAT80P	○
	HD6309E	DIP40P	○
	HD61810B (HSP)	DIP40P	○
NEC	μPD7807/08/09	SDIP64P,QUIP64P	○
	μPD7810H/11/14/16	SDIP64P,QUIP64P	○
	μPD78C10/11	SDIP64P,QUIP64P	○
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ISSUE WINNER

The winning Design Idea for the July 23, 1987, issue is entitled "Audio AGC circuit has 40-dB dynamic range," submitted by Norman M Hill of Zetron Inc (Bellevue, WA).

seven of the address registers. Next, it alters the stack pointer to point further into the stack, allowing the program to read 224 words in groups of 30 (60 bytes) at a time. These read operations destroy the contents of the 15 registers but not the contents of the stack. The final 32 read operations involve unstacking the registers, which restores the destroyed register data. The code that actually performs the refresh occupies about 96 bytes.

Your system startup code must install the Refresh routine's address in the exception vector for the system in use (normally the NMI). Then, for standard 8-bit dynamic RAMs, the system must invoke the routine at 4-msec (min) intervals. If the interrupting source is cyclic, it requires no attention from the software; otherwise, you must add acknowledgment code to the routine.

Further, your system startup code must call the routine's additional entry point, SRefresh, if execution of the startup code takes more than 4 msec. If the system has 9-bit (1M-byte) dynamic RAMs, you must adjust the stack offset and the number of move instructions accordingly. **EDN**

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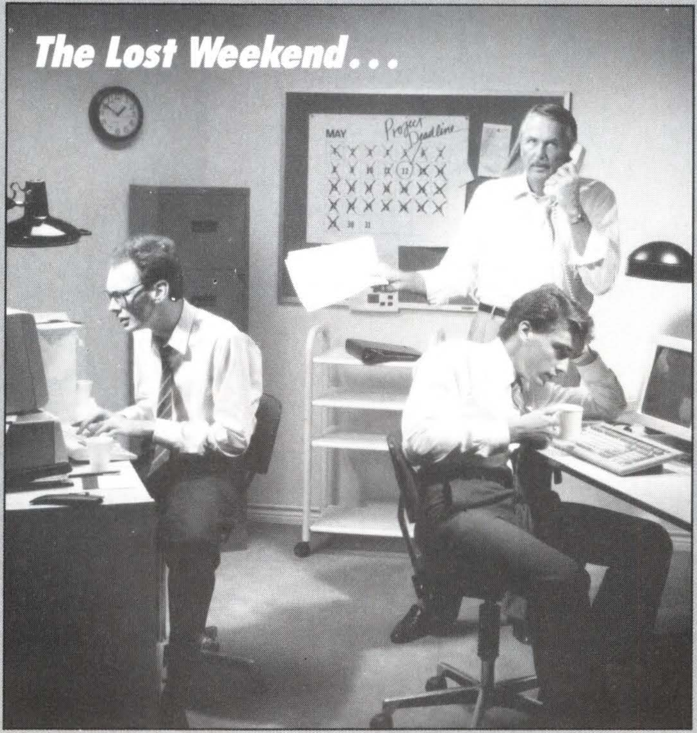

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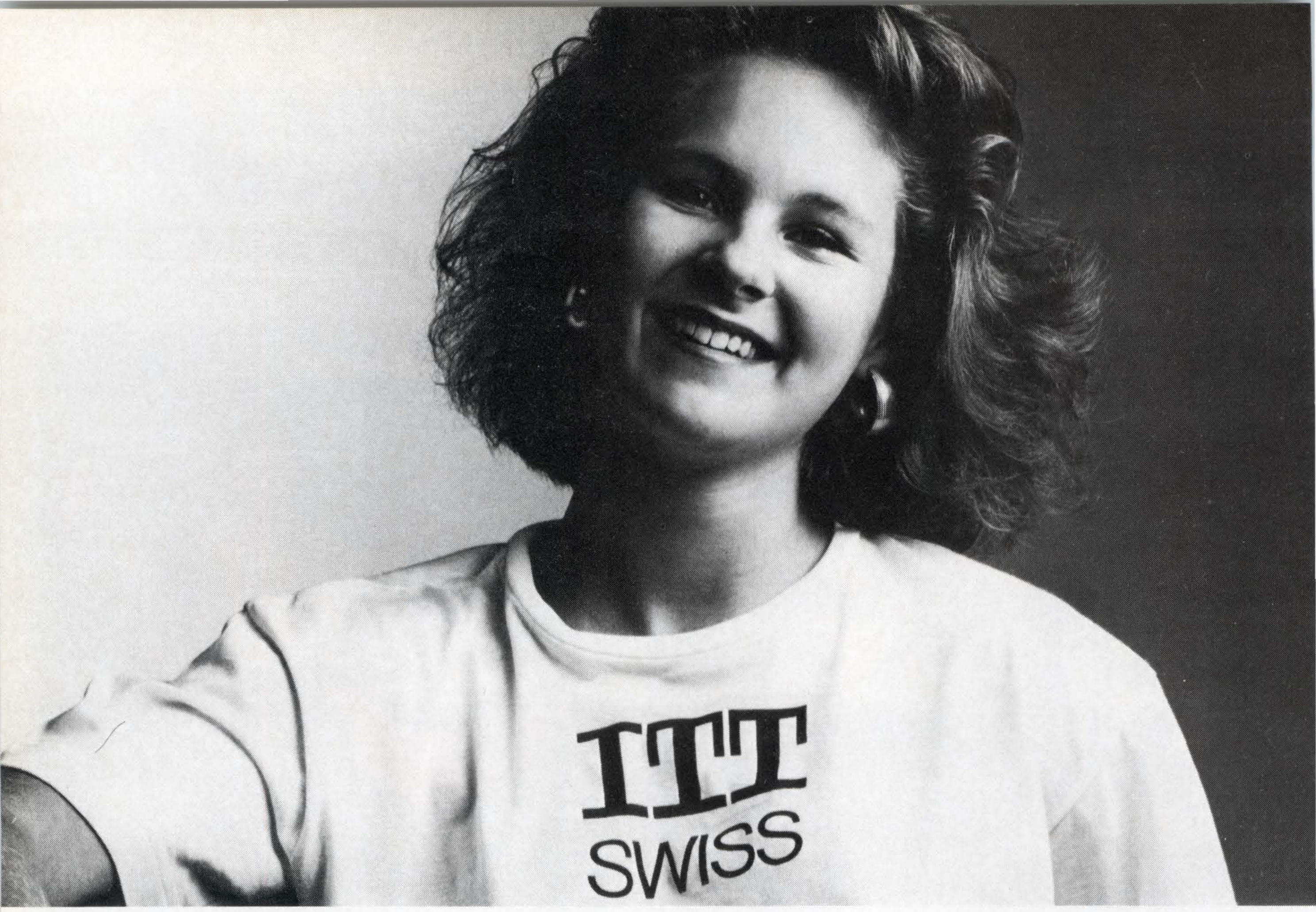

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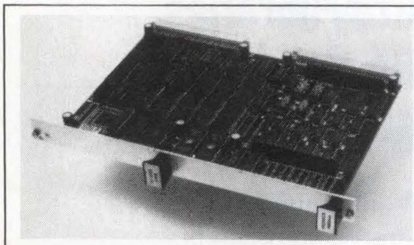

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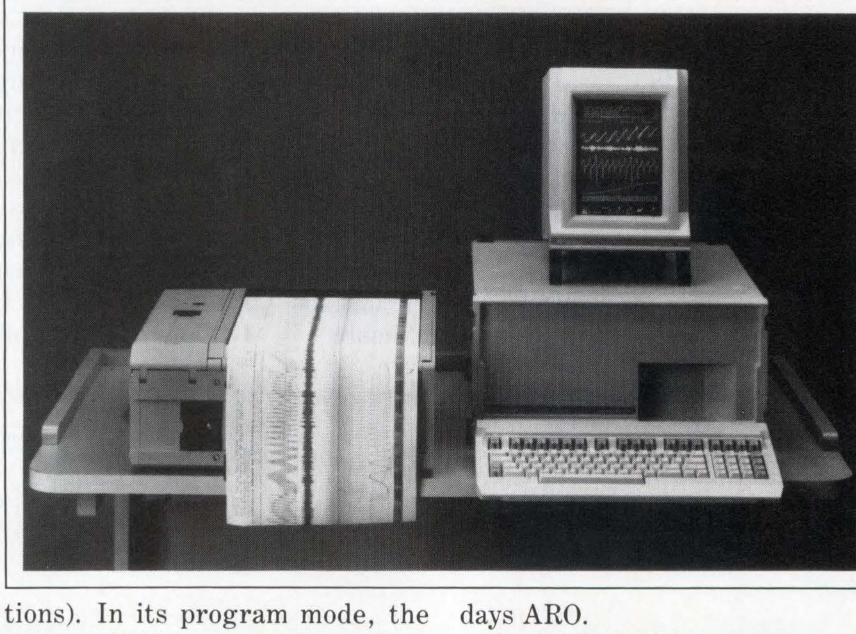

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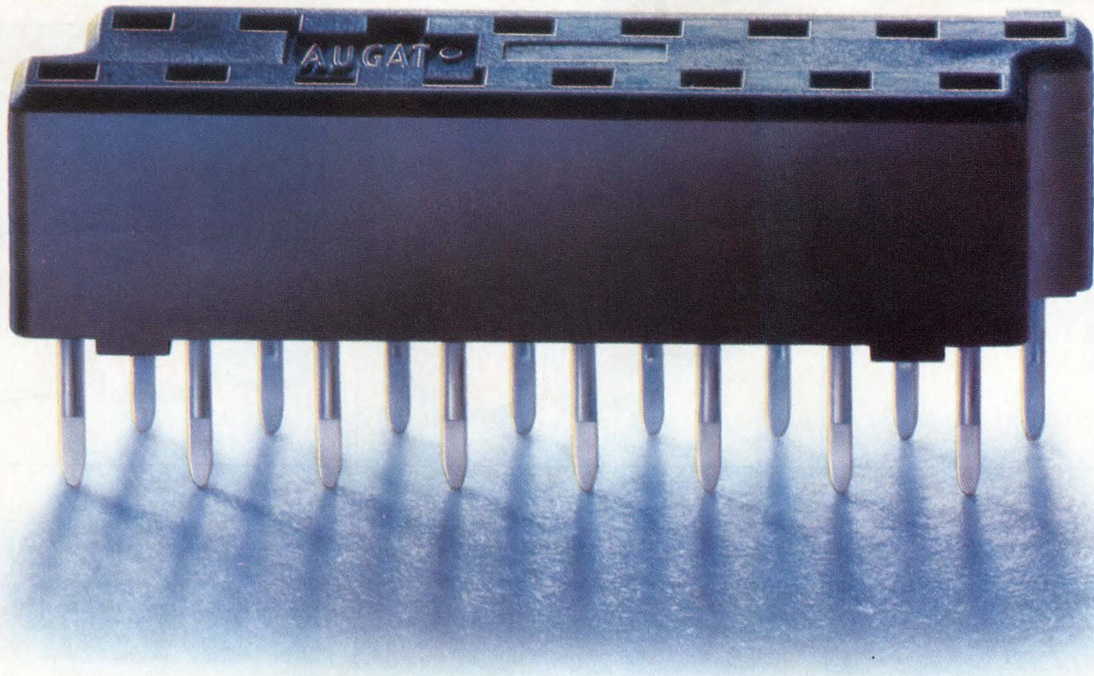

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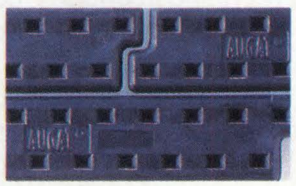

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- *Uses a bit-slice processor for graphics*
- *Provides a Unix operating system environment*

The Picture Processor is a high-resolution graphics and image-processing workstation incorporating a dedicated microcodable graphics/image processor and a Unix operating sytem environment. The graphics image processor is a 20-MIP bit-slice design that can handle logical pixel operations at rates as high as 110M pixels/sec. The single graphics/image processor supplied with the entry-level computer provides you with eight planes and has a double-buffered frame store for two 1280×1024-pixel resolution screens. With this single processor, the 8 bits per pixel allow you to simultaneously display as many as 256 colors from a palette of 16M colors. To extend image processing capabilities you can cascade as many as eight of the graphics/image processors within the machine for as many as 256 display planes. Video output modules are available for a single-user broadcast-quality display, and for a 6-user system. The Unix environment is provided by a CPU card that is based around Fairchild's Clipper RISC chip set, and that communicates with the graphics/image processor via the VME Bus. The computer is supplied with Unix System V.3, including support for full demand paging and virtual memory. A separate 80286 μP supervises I/O operations to speed up the Unix I/O handling. For communications purposes the computer supports TCP/IP protocol. From $30,000.

Benchmark Technologies Ltd, Benchmark House, 5 Penrhyn Rd, Kingston-upon-Thames, Surrey KT1 2BT, UK. Phone 01-541 1944. TLX 8952387.

Circle No 355

D/A BOARD

- *Features six 12-bit DACs*
- *Waveform sample rates to 380k samples/sec*

The NB-AO-6 is a NuBus analog output board for the Macintosh II. It features six 12-bit D/A converters that provide unipolar and bipolar voltage outputs. Each voltage output typically settles to within 1/2 LSB of full scale (10V) within 4 μsec. The offset and gain drifts are

New low price

Score a Whole In One

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Now you can score on your next round of systems designs *and* parlay your MS-DOS investment. Simply use our CMOS V25™ Whole in One™ — the new 16-bit microcomputer on a chip from NEC.

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Keeping score? In direct match play, *EDN* and *Byte* benchmark tests show the V25 clearly higher in performance.

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Check out the V25's real strengths. Full support, for one. It's here now with hardware and software tools including EPROM/OTP parts. And you're supported by regional design centers with an increasing number of application engineers.

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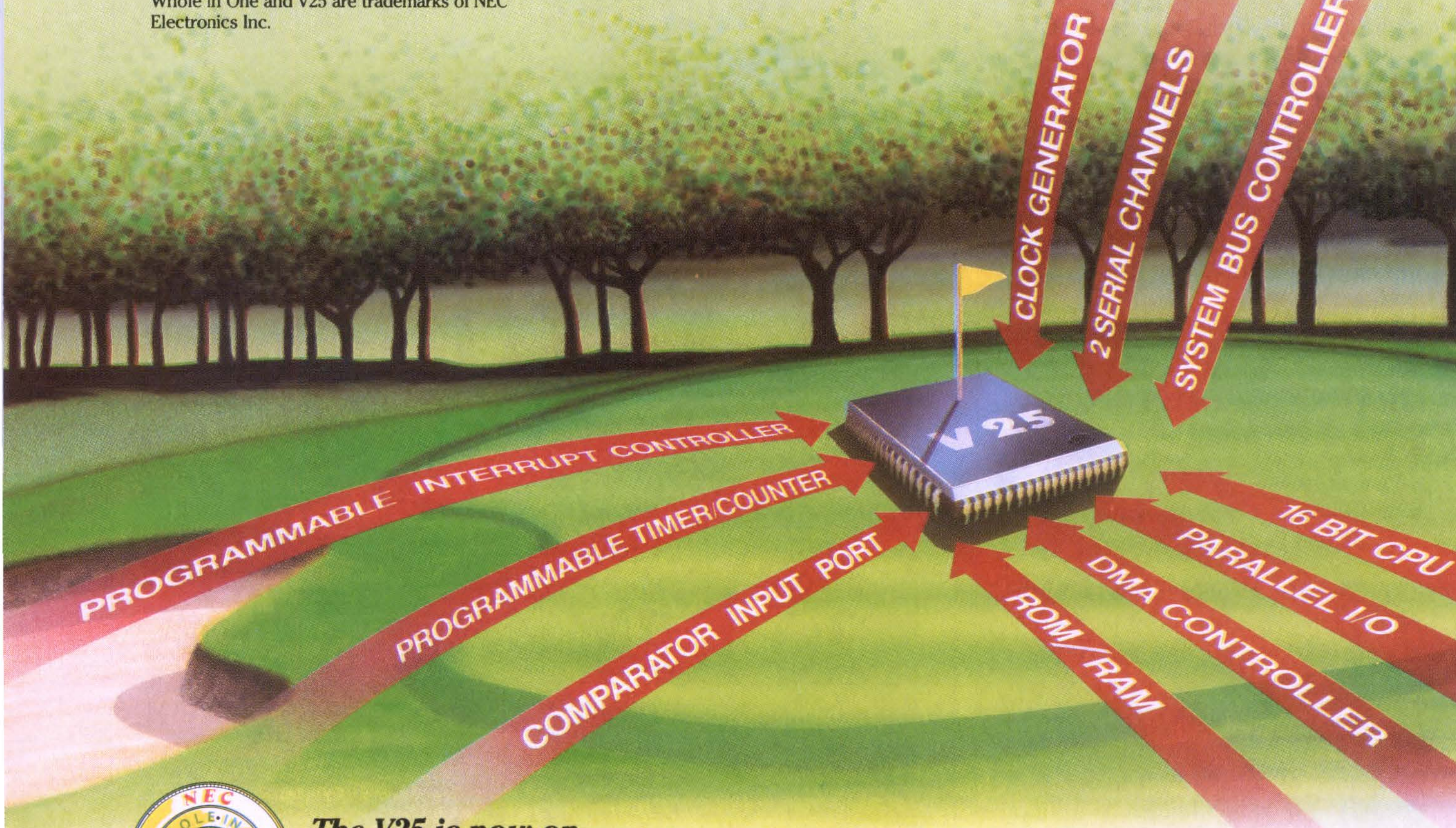
Production is another winning shot. The V25 is in full production in multiple fabs with high yields allowing very competitive pricing. Now add NEC's traditional high quality and leadership in CMOS manufacturing for a par-beating system on a chip.

For complete technical documentation and the number of your local Distributor Pro Shop, call 1-800-632-3531. In California, call 1-800-632-3532 and score your own Whole In One: the V25 from NEC.

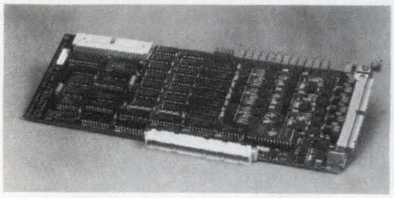
NEC Electronics Inc.
401 Ellis Street, P.O. Box 7241
Mountain View, CA 94039



The V25 is now on distributor shelves for immediate delivery

NEC

CIRCLE NO 95



typically 0.5 μV/°C and 10 ppm/°C, respectively. The board provides current outputs of 4 to 20 mA, which settle to a 0.1% accuracy within 5 μsec. Chopper-stabilization techniques minimize calibration requirements. The board features a real-time integration system (RTSI) bus that allows synchronization with other boards made by the company. The converter outputs can be updated by an RTSI bus signal, an external signal, or software control. The bus provides DMA capability, which allows the board to generate six different waveforms simultaneously. You can generate waveforms with sample rates as high as 380k samples/sec. In addition, you can write data to any combination of the DACs simultaneously with 16-bit write operations. $895.

National Instruments, 12109 Technology Blvd, Austin, TX 78727. Phone (800) 531-4742; in TX, (800) 433-3488. TLX 756737. FAX 512-250-0382.

Circle No 356

DISPLAY CONTROLLERS

- *Possess 13M-pixel/sec random vector-drawing rates*
- *Have 1280×1024- or 1024×768-pixel resolution*

The 1000VM Series consists of four display-controller models for the VME Bus, covering a pixel-resolution range of 1024×768 to 1280×1024 with 4 or 8 bits/pixel and an optional overlay of 4 bits. Two VLSI chips, a graphics processing unit (GPU) rated at 4 MIPS, and a memory control unit (MCU) can achieve drawing rates of 13M pixels/sec. The GPU controls the graphics subsystem and executes graphics commands from the host processor. The MCU controls raster memory, carrying out low-level graphics tasks such as vector drawing, polygon filling, and pixel block transfers. The combination of surface-mount technology and VLSI components results in each configuration occupying only one VME slot (6U). A standard palette has 4096 colors and 16 gray levels. An extended palette of 16 million colors and 256 levels of gray is available with two of the models. Power requirements range from 15 to 30W, depending on the model and configuration. The display controllers' memory consists of a 256k-bit video RAM chip, which you can configure to give 0.5M bytes to 2M bytes of onboard RAM by adding chips. $2495 to $3995.

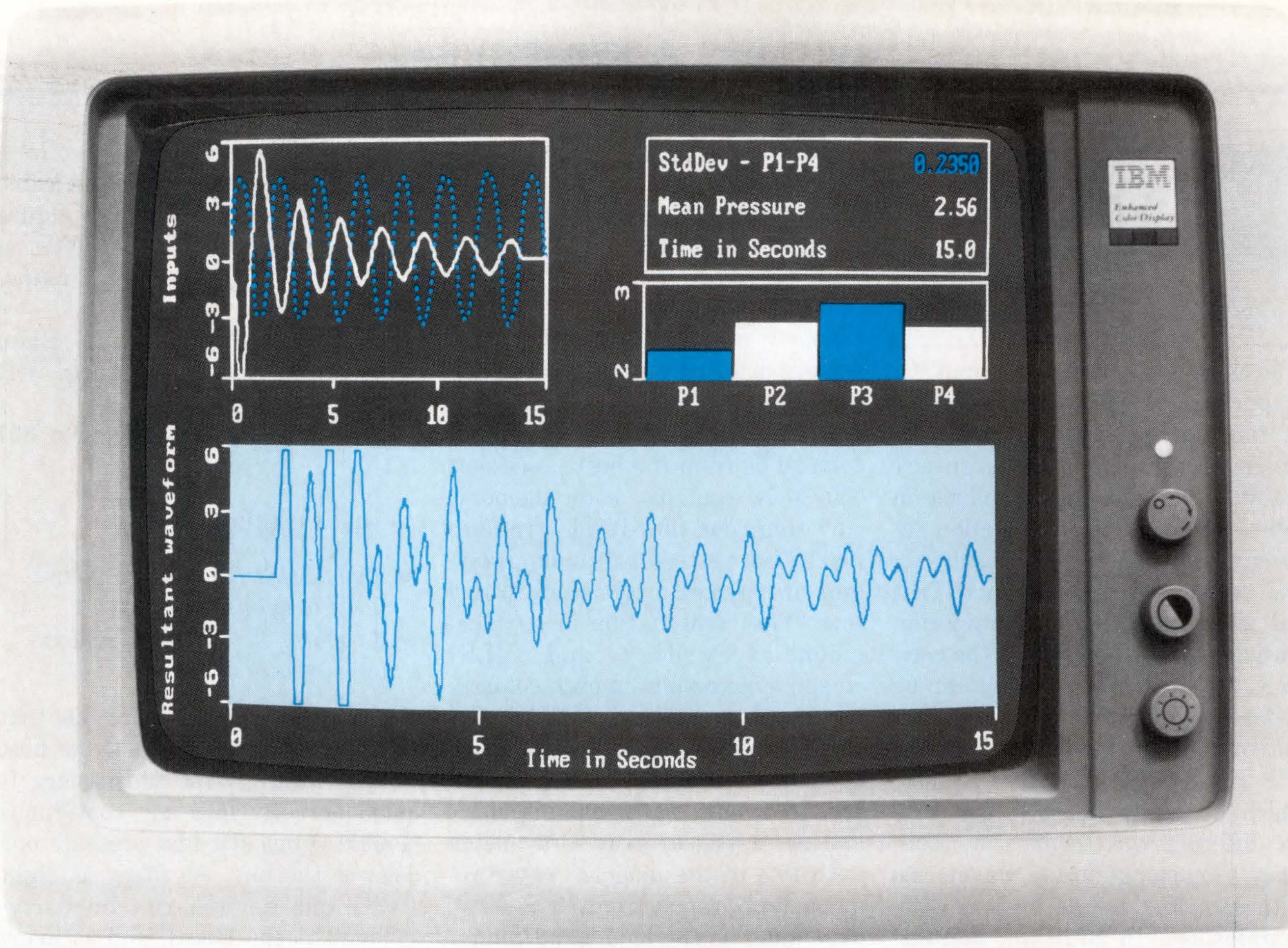
Metheus Corp, 5510 NE Elam Young Parkway, Hillsboro, OR 97124. Phone (503) 640-8000.

Circle No 357

SCSI ADAPTER

- *Eight SCSI devices are interfaces to Q-bus*
- *Supports slave, DMA, and interrupt modes*

The SDC-HA11 is a SCSI bus that provides an interface to a Q-bus host adapter with 22-bit addressing. It plugs directly into any contiguous double Q-bus slot and presents one load to the bus. As many as eight SCSI bus devices can be daisy-chained to the board, and as many


StdDev - P1-P4 0.2350
Mean Pressure 2.56
Time in Seconds 15.0
Inputs
Resultant waveform
P1 P2 P3 P4
Time in Seconds
IBM
Enhanced Color Display

as 10 command bytes can be requested by the SCSI bus device before a command from the host is executed. Upon completion of the command, the SCSI device stores the completion status in a register on the board. The board has three modes of operation: slave, DMA, and interrupt. It provides base-address selection by switch from 160000 to 177760 (octal) and interrupt vector selection from 000 to 374 (octal). Parity enable/disable and interrupt priority selection (4, 5, 6, or 7) are jumper selectable. $417.

Sigma Sales, 3401 E La Palma Ave, Anaheim, CA 92806. Phone (714) 630-6553. TLX 298607.

Circle No 358

WORKSTATION

- *68020 µP and 68881 coprocessor deliver 4 MIPS*
- *To 32M bytes of RAM*

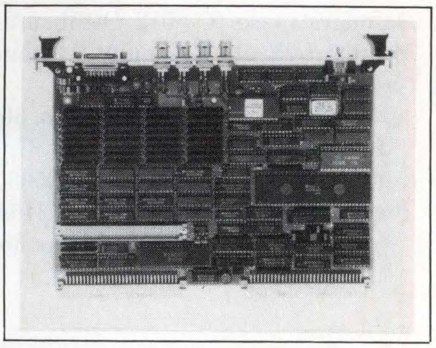
The Domain Series 4000 is a color workstation that features a 25-MHz 68020 µP and a 25-MHz 68881 floating-point coprocessor. Combined with an 8k-byte virtual cache memory, the system operates at 4 MIPS. It uses 1M-bit surface-mount dynamic RAM chips and can have as much as 32M bytes of main memory. You can choose from a 15- or 19-in., 60-Hz, noninterlaced color display, with a 1024×800-pixel resolution or a 19-in., 64-Hz noninterlaced monochrome display, with a 1280×1024 resolution. As many as 256 colors can be simultaneously displayed from a palette of 16 million. An IBM PC/AT-compatible expansion bus allows access to the third-party board market. The workstation has three RS-232C ports and either a 155M-byte or 348M-byte (formatted) ESDI Winchester drive. A 5¼-in., 1.2M-byte floppy disk and a ¼-in., 60M-byte cartridge tape are optional. The 4M-byte monochrome version without disks, $13,900; 4M-byte, 15-in. color version without disks, $18,900; 8M-byte, 19-in. color version with 155M-byte disk and cartridge tape, $33,900.

Apollo Computer Inc, 330 Billerica Rd, Chelmsford, MA 01824. Phone (617) 256-6600. TWX 710-343-C803.

Circle No 359

GRAPHICS CARD

- *1160×870 or 1024×800 pixel resolution*
- *Displays 16 colors from a palette of 64k colors*



The SYS68K/AGC-2 is a double-Eurocard VME Bus graphics card that uses the ACRTC-63484 advanced color-raster tube-controller chip. It provides a maximum screen resolution for a 50-Hz refresh rate of 1160×870 pixels, and 1024×800 pixels for a 60-Hz refresh rate. The board has 1M byte of onboard video RAM. Operating with 4 bits/pixel, the board is capable of simultaneously displaying 16 colors from a palette of 64k colors. Video output is via RGB and composite sync outputs. Graphics capabilities include hardware zoom, vertical and horizontal smooth scrolling, clipping, hitting, blinking, and conditional blinking. A light pen interface is also provided. A software package for GKS (Level 2b) support, operating under Unix or the PDOS real-time operating system, is currently being ported to the board. Around DM 3400.

Force Computers GmbH,

Daimlerstrasse 9, 8012 Ottobrunn/Munich, West Germany. Phone (089) 600910. TLX 524190.

Circle No 360

Force Computers Inc, 727 University Ave, Los Gatos, CA 95030. Phone (408) 354-3410. TLX 172465.

Circle No 361

CPU VERIFIER

- *Verifies the functions of 10 different μPs*
- *Demo program for in-circuit emulation*

The MJ700 is a single-board device tester and in-circuit-emulation board. The board can accept 10 different μPs at one time: The following devices are supported: Intel 8048, 8051, 8085, and 8088; Motorola 6801 and 6809; NEC V20; Rockwell 6502; and Zilog Z80. The board has an input port consisting of eight DIP switches that are read as 8 bits onto the data bus. Eight LEDs indicate the progress of μP operation. Each 1k-byte block of ROM is mapped into the appropriate memory space of each processor; a small demonstration program is included that highlights the features of in-circuit emulation. The software can be used to demonstrate features such as single stepping, breakpoint operation, and register modification during program execution. A 2k-byte RAM is available for program use. Board with power supply, $395.

MicroMark Engineering, 3337 Kifer Rd, Santa Clara, CA 95051. Phone (408) 733-1576.

Circle No 362

MEMORY MODULE

- *64-bit cache memory has a hit access time of 75 nsec*
- *Module selection is on 64k-byte boundaries*

The MM-6220D is a dynamic RAM memory module for the VME Bus. Its capacities range from 2M, 4M, 8M, and 16M bytes. It supports A32/A24, D32/D16, and D8 VME Bus interfaces. A combination of a 64-bit cache memory and block-mode transfers (BLTs) provides fast read times. The access time for cache hits is 75 nsec for both 16- and 32-bit transfers on read and write cycles. The average sequential read cycle for cache hits and 16-bit transfers is 135 nsec; for 32-bit transfers it's 170 nsec. Each byte is parity checked, with parity status stored and transmitted via the BERR signal. The module can be selected on 64k-byte boundaries whose upper and lower limits are switch-selectable. All boards are burned in, and memory diagnostics check the operation for 48 hours while being temperature-cycled from 0 to 60°C. MM-6220D/4M, $1485; MM-6220D/16M, $4995.

Micro Memory Inc, 9540 Vassar Ave, Chatsworth, CA 91311. Phone (818) 998-0070.

Circle No 363

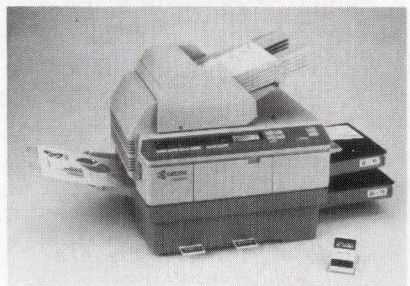
ETHERNET INTERFACE

- *Attaches via a VME Bus CPU card*
- *Supported under the OS9 operating system*

Piggybacked onto the company's IBAM 16-bit intelligent base module, or Eurocom-5 32-bit CPU card, the Ethernet-IPIN daughter board adds an intelligent Ethernet interface to a VME Bus system without increasing the number of card slots required. The interface is fully compatible with IEEE-802.3 LANs and features a standard media attachment interface. DMA support is provided to transfer data to and from the Ethernet LAN. Software support is provided in the OS9/68k real-time operating system, and software for the IBAM module, supporting the TCP/IP communication protocol and running under Unix 5.3 and OS9, is under development. The Ethernet-IPIN costs around $700.

Eltec Elektronik GmbH, Galileo-Galilei-Strasse 11, 6500 Mainz 42, West Germany. Phone (06131) 50630. TLX 4187273.

Circle No 364



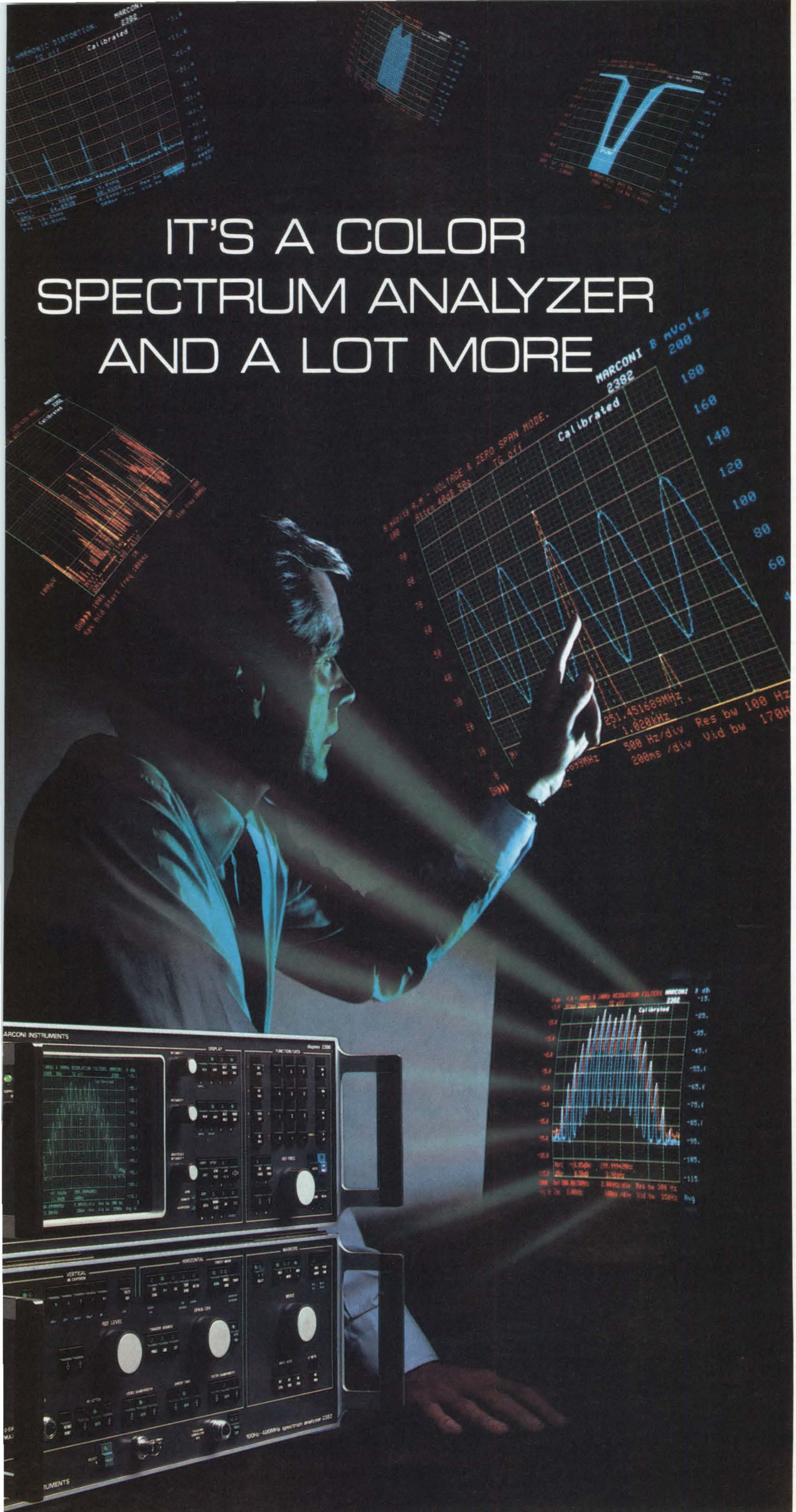
LASER PRINTER

- *Prints as many as 18 pages/min*
- *Produces 300×300-dots/in. raster graphics*

The F-3010 laser printer has a print speed of 18 pages/min. It has 78 resident fonts (including eight foreign-language character sets), 1.5M bytes of RAM (expandable to 3.5M bytes), two paper trays, a parallel port, and an RS-232C port. The printer comes with a page description language (Prescribe) and four fonts that let users create custom fonts from 3-point to 13-in. sizes. It can emulate seven popular printers; in addition, you can download fonts in the company's format or LaserJet Plus format. The printer can produce full-page (8½×11 in.) 300×300-dots/in. raster graphics, and line, circle, pie, arc, and fill-pattern vector graphics. It prints 39 bar-code styles. $8395.

Kyocera Unison Inc, Box 3056, Berkeley, CA 94703. Phone (415) 848-6680. TWX 650-306-1844.

Circle No 365



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Measures −150 dBm to +30 dBm with resolution 10 to 0.5 dB/div., Variety of log. and linear scales. Two independent display channels.

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Plus a host of features including standard GPIB, optional RGB output for color monitor, two markers, with 0.01 dB and 1 Hz resolution, selective level meter mode that eliminates the need to sweep when monitoring levels, display averaging on both channels for extracting signals from noise, limit masks that may be generated and stored, 9 storage locations for measurement set-ups, digital plotter output, max. hold for capturing transients, overload protection—we could go on.

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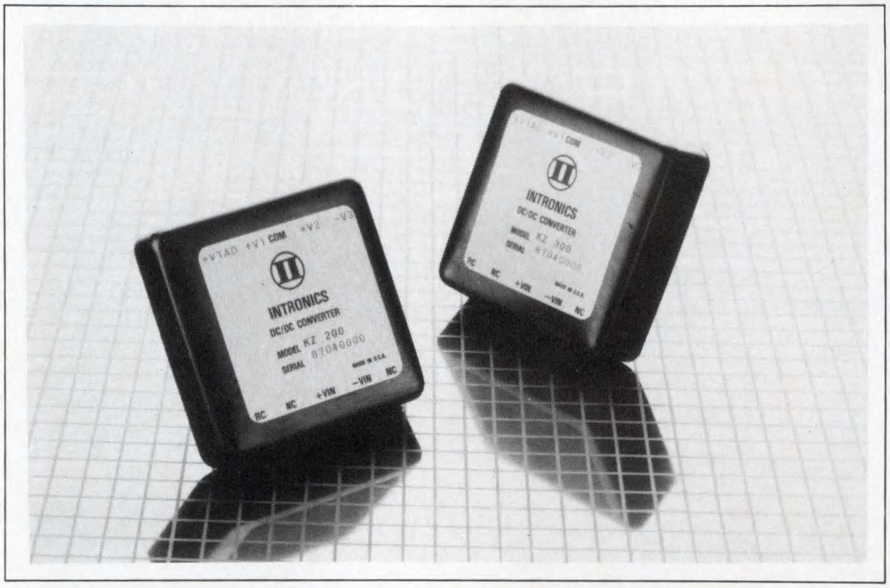
CIRCLE NO 84

COMPONENTS & POWER SUPPLIES

DC/DC CONVERTERS

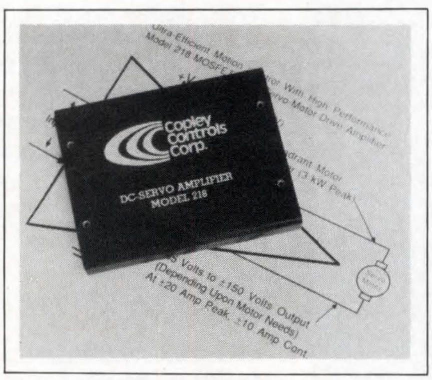
- *Offer 25 to 40W outputs*
- *PC-board mountable*

With power ratings of 25 and 40W, the KZ 200 and 300 Series converters offer a broad range of high-frequency/high-density devices. The units are pc-board mountable and are available as single- or triple-output modules. The nominal-input voltage ratings range from 20 to 72V. Both power ranges are available in single-output models with 5, 12, or 15V outputs, and in triple-output versions of 5, 12, and −12V or 5, 15, and −15V. The line/load regulation specs at 1% on the main channel, and efficiency equals 75% at full load. The operating range spans −40 to +85°C. Ripple and noise are 10 and 100 mV p-p, respectively. $74 to $104 (100).



Intronics Inc, 57 Chapel St, Newton, MA 02158. Phone (617) 964-4000. TWX 710-335-6835.

Circle No 366



SERVO AMPLIFIER

- *Outputs 1500W continuous*
- *Provides 3000W for motor acceleration and reversal*

Measuring only 5×4×0.8 in., the Model 218 servo amplifier readily mounts on a pc board or in a small NEMA enclosure. It provides a 1500W continuous output and can output 3000W for motor-acceleration and reversal operations. The module has an integral dc/dc converter that develops the voltages necessary to power the internal circuitry so it can operate from one 25 to 155V supply. The amplifier is protected against short circuits, overvoltage, undervoltage, and excessive temperature. It also responds to end-of-travel, beginning-of-travel, and emergency-stop inputs. The 22-kHz switching frequency allows the amplifier to drive servo motors with internal inductance as low as 250 μH without having to use series-smoothing chokes. $516. Delivery, four to six weeks ARO.

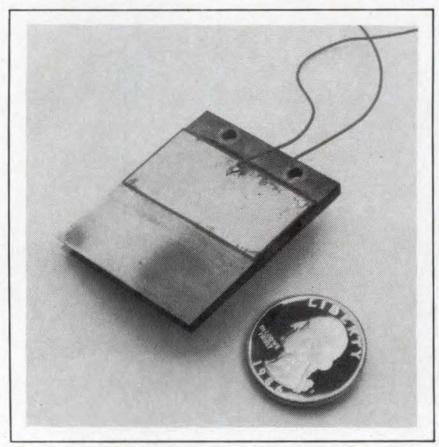
Copley Controls Corp, 375 Elliot St, Newton, MA 02164. Phone (617) 965-2410. TLX 285957.

Circle No 367

PIEZOELECTRIC FAN

- *Continuous high-temperature rating of 150°C*
- *Consumes only 170 mW of power*

The LP24HT, a dc-operated miniature piezoelectric fan, produces a planar airstream that emanates from the front tips of its resonating blades. It has a continuous high-

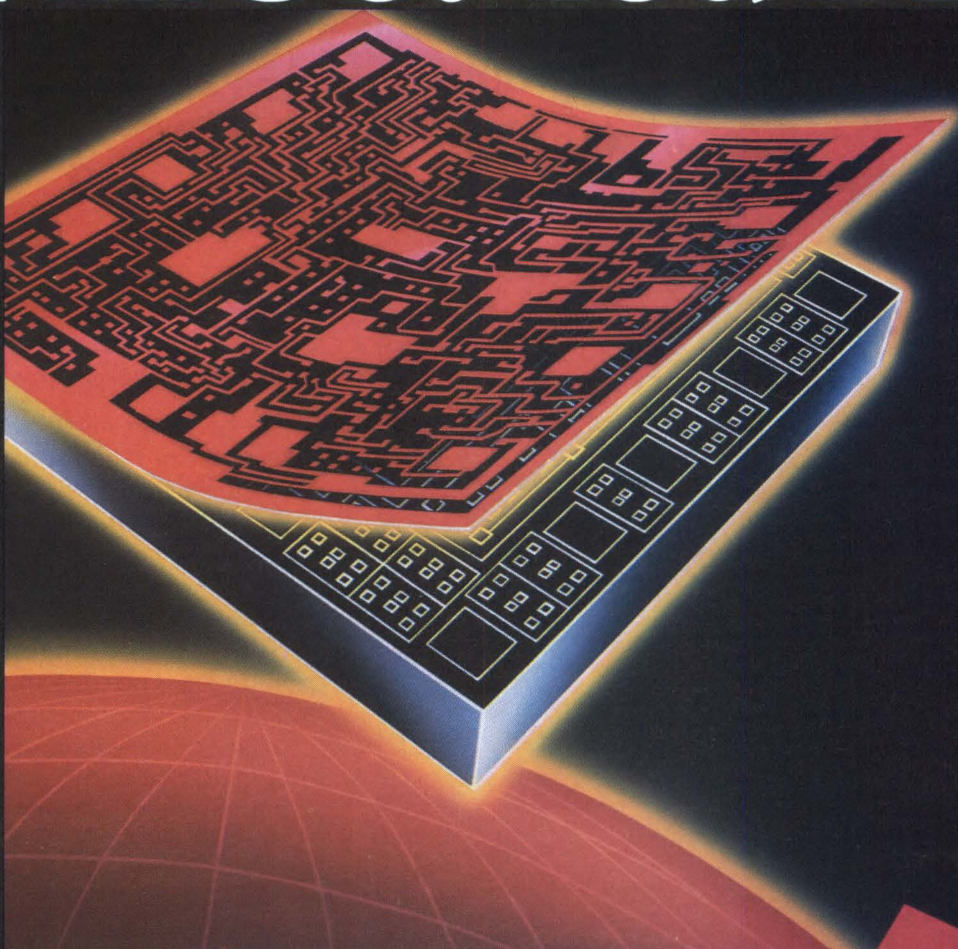


temperature rating of 150°C. Measuring 0.16×1.75×1.5 in. and weighing only 0.6 oz, the LP24HT delivers 1.5 cfm while consuming only 170 mW of power from a 24V dc supply. The fan comes with an inverter drive circuit that you can connect directly to the fan or mount remotely for high-temperature applications. Engineering evaluation kit, $300.

Piezo Electric Products Inc, 186 Massachusetts Ave, Cambridge, MA 02139. Phone (617) 547-1777.

Circle No 368

CSC Bipolar Arrays Will Set You Free.



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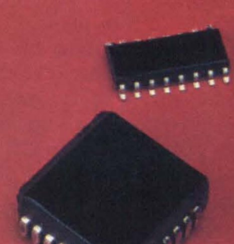
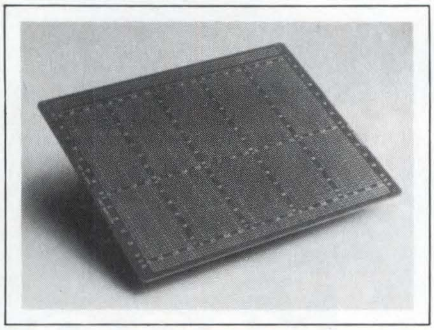
IC users worldwide have already benefited from CSC's expertise and quality control. As a result, CSC is now the 3rd largest U.S. producer of linear bipolar arrays. To make your design decisions easier, CSC offers over 275 pre-designed linear and digital cells. For solutions that will set you free, talk to CSC. With GENESIS Arrays, the possibilities are limitless.



CSC CHERRY SEMICONDUCTOR

CHERRY SEMICONDUCTOR CORP., 2000 South County Trail, East Greenwich, RI 02818
(401) 885-3600 FAX(401) 885-5786 Telex WUI 6817157

CIRCLE NO 83



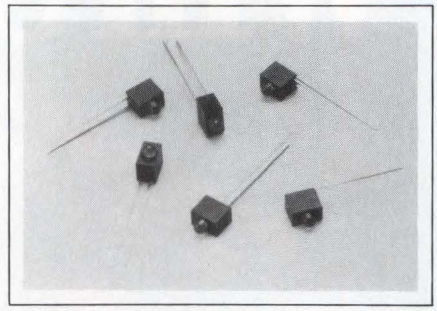
PROTOTYPE PANEL

- *Accommodates any combination of mixed-logic types*
- *72Ω characteristic impedance*

The Protoboard construction consists of six voltage and three ground planes. With a 72Ω characteristic impedance, it can accommodate any combination of mixed-logic families. The hole pattern can handle all types of components, including pin-grid arrays. The device is compatible with the Mupac high-speed series of wirewrap panels and is supplied 100% tested. $500.

Kollmorgen Corp, Multiwire Div, 250 Miller Pl, Hicksville, NY 11801. Phone (516) 933-8300.

Circle No 369



LED

- *60° viewing angle*
- *Features integral resistor*

The pc-board-mountable T-1 LED features an integral resistor and is designed for 5 and 12V operation. Available in models designed for vertical or horizontal viewing, it has a 60° viewing angle and a 4-mcd typical luminous intensity. The current draw is 13 mA typ, and the units are available in red, green, and amber. The package is designed to facilitate wave soldering; a polarity indication ensures correct mounting. From $0.42 (1000). Delivery, stock to six weeks ARO.

Data Display Products, Box 91072, Los Angeles, CA 90009. Phone (800) 421-6815; in CA, (213) 640-0442. TLX 664690.

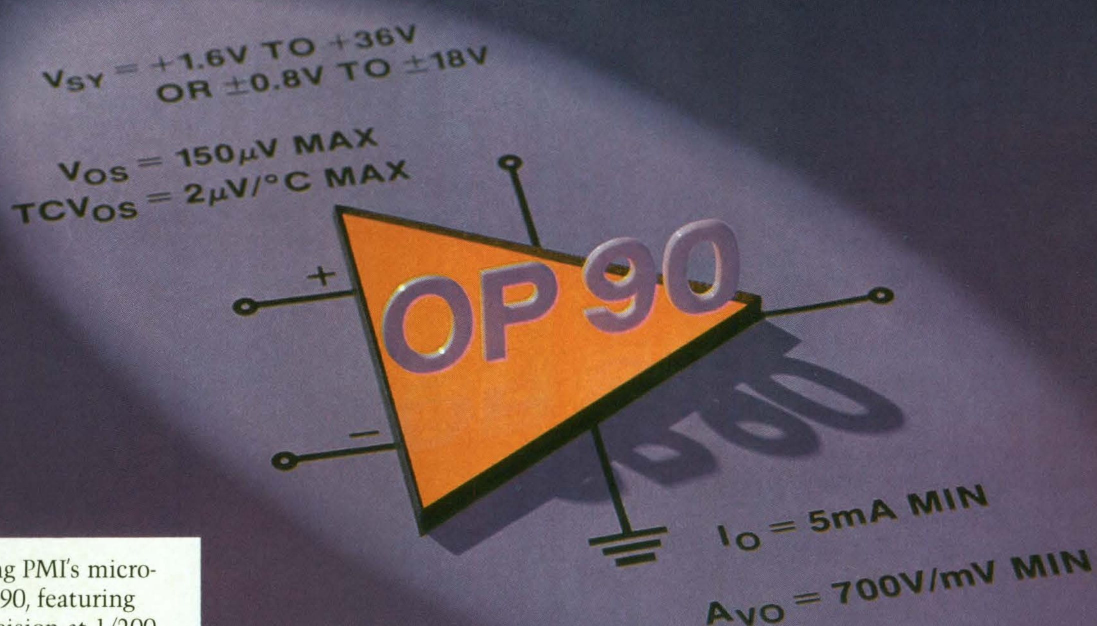
Circle No 370

NTC THERMISTORS

- *Have operating current ratings between 1.7 and 15A*
- *Protect sensitive equipment against surge currents*

Eight new additions to the 644 Series negative temeperature coefficient thermistors cover operating currents from 1.7 to 15A and offer

PMI PRESENTS: PRECISION PERFORMANCE AT 20μA MAX.



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OP-90E		
V_{SY}	+1.6 to +36	V Min/Max
V_{OUT}	0 to (V_{SY} − 0.8V)	V
I_{SY}	20	μA Max
I_{OUT}	5	mA Min
V_{OS}	150	μV Max
A_{VO}	700	V/mV Min

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CIRCLE NO 82

Analog CAE is More Than SPICE.

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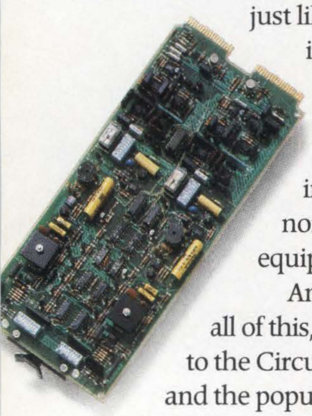

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CIRCLE NO 81

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Sunnyvale, CA 94086
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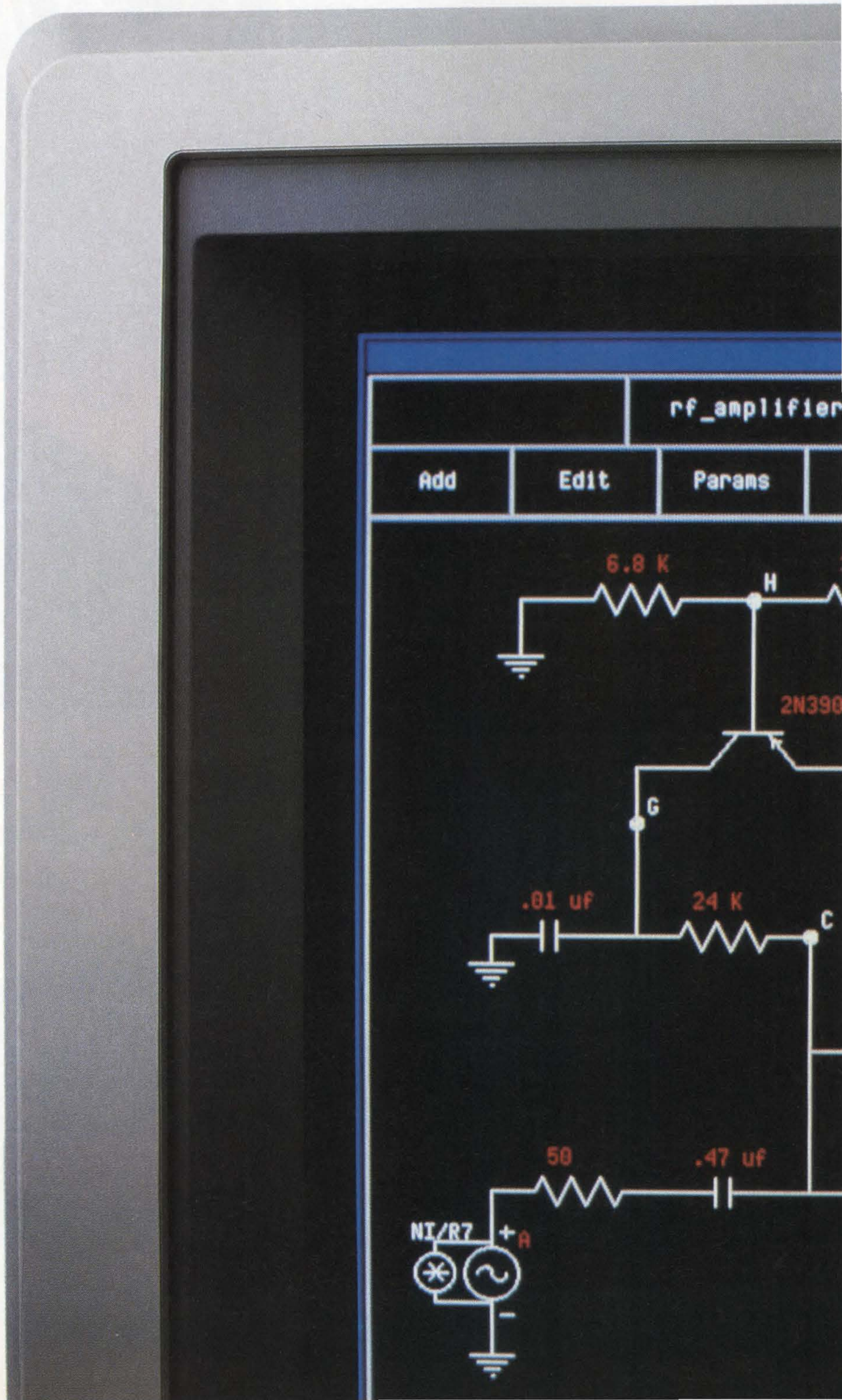


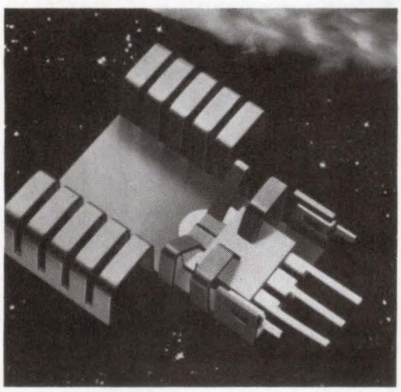
cold resistances of between 2 and 82Ω. You can use the devices, which are resistant to surge currents eight times their operating current, to limit the inrush current into sensitive equipment, such as switch-mode power supplies, or to prevent high starting torques in electric motors. The thermistors have a semiconductor disk construction with 38-mm radial leads. Customized versions, including devices with special cold resistances and leadless types for clamp mountings, are available to special order. Approximately DM 0.75 (1000).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 371

Mepco/Centralab Inc, 5900 Australian Ave, West Palm Beach, FL 33407. Phone (305) 842-3201.

Circle No 372



HEAT SINK

- *Spring-action design applies pressure in four places*
- *Vertical mounting minimizes pc-board space requirements*

Designed for TO-218-type semiconductors, the 5922 heat sink features a spring-action design that applies pressure in four places to maximize heat transfer. The dual-channel fins create additional surface area and air circulation for effective heat removal. With an input of 8W, the heat sink has a thermal resistance of 8.75°C/W under natural convection. Made of aluminum alloy, the unit is available in gold chromate and black, red, bronze, or blue anodize finish. Vertically mounted, the 1.97-in.-high unit takes minimum board space. $0.43 (1000).

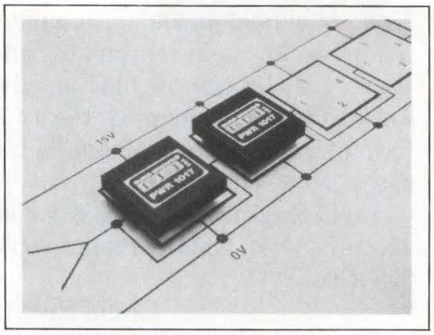
Aavid Engineering Inc, Box 400, Laconia, NH 03247. Phone (603) 528-3400.

Circle No 373

DC/DC CONVERTER

- *Eliminates unwanted beat-frequency noise*
- *1000V pk isolation*

The PWR1017 dc/dc converter eliminates unwanted beat-frequency noise generated by multiple power supplies in the same system. The 4-channel, dual-output unregulated converter operates over an input voltage range of 10 to 18V dc; each output channel outputs 25 mA at ±15V dc for a total output power of 3W. The continuous isolation voltage between each output channel and the input is 1000V pk. Other key features include 6-sided shielding to suppress EMI and input and output filtering to minimize the effects of electrical noise. Each converter is tested in compliance with UL544, VDE750, and CSA C22.2 dielectric withstanding specifications, in addition to 100% barrier-leakage current testing. $58.75 (100).



Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491. TWX 910-952-1111.

Circle No 374

TIMER MODULES

- *Versions record total run-time or elapsed time periods*
- *Have an internal lithium battery for 10-year operation*

The CUB3T and CUB3TR timer modules have 5½-digit LCD displays, allowing you to measure time periods as long as 199,999 hours with 1-hour resolution. Or you can measure periods as long as 19,999.9 hours with 0.1-hour resolution. The CUB3T is designed to monitor total run time, and therefore has no reset switch. The CUB3TR has a user-accessible pushbutton so that you can reset the timer. Both timers are powered by an internal lithium battery, which maintains operation for 10 years. Three versions of each timer are available: One version begins timing when an external switch is closed. Two other versions begin timing when a voltage of 10 to 30V or 60 to 260V, respectively, is applied to their inputs. All the timers have an operating range of −30 to +75°C. They snap-fit into standard 1×2-in. panel apertures. Approximately £24 (100).

Our 16-bit DACs & ADCs keep your precision designs on target.

Some customers say we're outstanding in our field because we offer the industry's widest selection of high resolution data converters—over 120 of them—and the deepest understanding of how to make them work best in your applications.

More Bits For Your Bucks

When you use our 16-bit converters, you'll get clearer images, cleaner sounds, more accurate representations of real-world signals and binary-world data streams.

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- Complete selection of A/D and D/A converters.
- Millions of units of design, manufacturing, and testing experience.
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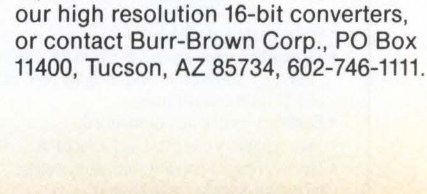
- ADC conversion speeds to 15μs, DACS to 1.5μs settling.
- Low drift, low power models.
- Wide variety of hermetic ceramic and low cost plastic package options.
- ADCs from \$66.15*, DACs from \$8.95*.



Ask your Burr-Brown sales representative for more information on our high resolution 16-bit converters, or contact Burr-Brown Corp., PO Box 11400, Tucson, AZ 85734, 602-746-1111.

BURR-BROWN®

*U.S. prices in 100s.

CIRCLE NO 79

Red Lion Controls Ltd, Cranford Lane, Heston, Hounslow, Middlesex TW5 9NQ, UK. Phone 01-759 0694. TLX 24178.

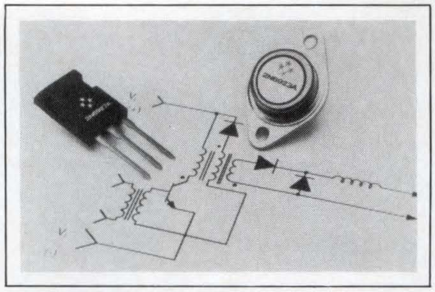
Circle No 375

Red Lion Controls Inc, Willow Springs Circle, Rd 5, York, PA 17402. Phone (717) 767-6511. TWX 510-657-4214.

Circle No 376

POWER TRANSISTORS

- *850V V_{CEO} with switching speeds of 35 nsec*
- $V_{CE(sat)}$ of just 1V at 25°C



The 2N6920A/27A and 2N6980A/81A Series bipolar power-switching transistors combine 850V V_{CEV} with a 35-nsec switching speed. They also offer V_{CEO}s of 400 and 450V, nominal collector current ratings of 10, 15, and 25A, and a maximum $V_{CE(sat)}$ of just 1V at 25°C. All models have the ability to switch peak-rated current (20 to 50A) at 500V. At 25°C, the units feature maximum voltage rise time and a current fall time of 30 nsec, and a maximum crossover time of 50 nsec. At 100°C, the maximum crossover time is only 70 nsec. For applications where 550V V_{CEV} is sufficient, you may order each model without the A suffix. $5.33 to $21.45 (100).

General Semiconductor Industries Inc, 2001 W Tenth Pl, Tempe, AZ 85281. Phone (602) 968-3101. TWX 910-950-1942.

Circle No 377

DISPLAY MODULE

- *Features swiveling mounting brackets*
- *Single-supply operation*

The 3601-88-016 is a 5×7 dot-matrix, 1-line×16-character, vacuum-fluorescent display module. It features 0.198-in.-high characters and swiveling mounting brackets that maximize front-panel design flexibility. An onboard µP controller handles all scan, refresh, and data I/O tasks, simplifying the interface to an 8-bit ASCII parallel data bus. It needs only one 5V supply for operation. The module displays the full 96-character ASCII font of upper-and lower-case letters, num-

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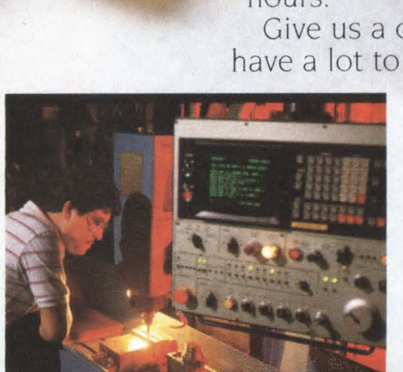

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bers, and symbols. The display characters are a blue-green color, but a wide variety of filters are available to fit almost any application. $61 (100). Delivery, four to six weeks ARO.

IEE Inc, 7740 Lemona Ave, Van Nuys, CA 91409. Phone (818) 787-0311. TLX 4720556.

Circle No 378

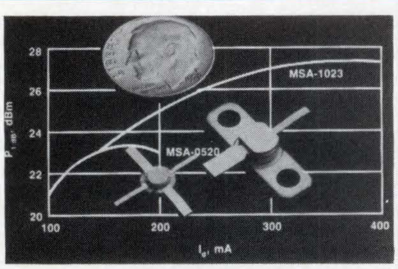
DC/DC CONVERTERS

- *50 to 72W output power*
- *Have 85% efficiency*

The DC60 Series dc/dc converters are fabricated on a single pc board. They have a switching frequency of 100 kHz. Twelve models offer nominal inputs of 12, 24, and 48V dc. Single outputs of 5, 12, 15, or 24V dc at 2.5 to 12A currents are offered with a total maximum output power of 50 to 72W. Efficiency ranges to 85%. Input/output isolation measures 2500V dc, and line/load regulation is ±0.2% typ. All models incorporate under/overvoltage shutdown and output short-circuit protection. The operating range spans 0 to 70°C. $159. Delivery, stock to eight weeks ARO.

Power General, Box 189, Canton, MA 02021. Phone (617) 828-6216.

Circle No 379



AMPLIFIERS

- *Feature 23-dBm power output*
- *Housed in BeO disk packages*

Featuring a 100-MHz to 2-GHz bandwidth, the MSA-0520 and MSA-1023 general-purpose, cascadable gain blocks are designed for use in narrow or broadband RF amplifier circuitry. At 1 GHz, the MSA-0520 features a 23-dBm power output at 1-dB compression, a 33-dBm third-order intercept point, and an 8.5-dB gain. It is housed in a BeO disk package for good thermal characteristics. At the same frequency, the MSA-1023 features a 27-dBm power output at 1-dB compression, a 37-dBm third-order intercept point, and an 8.5-dB gain. It is housed in a BeO flange package and is designed for use in push-pull configurations to achieve a 30-dBm power output. MSA-0520, $25.40; MSA-1023, $34.50 (100).

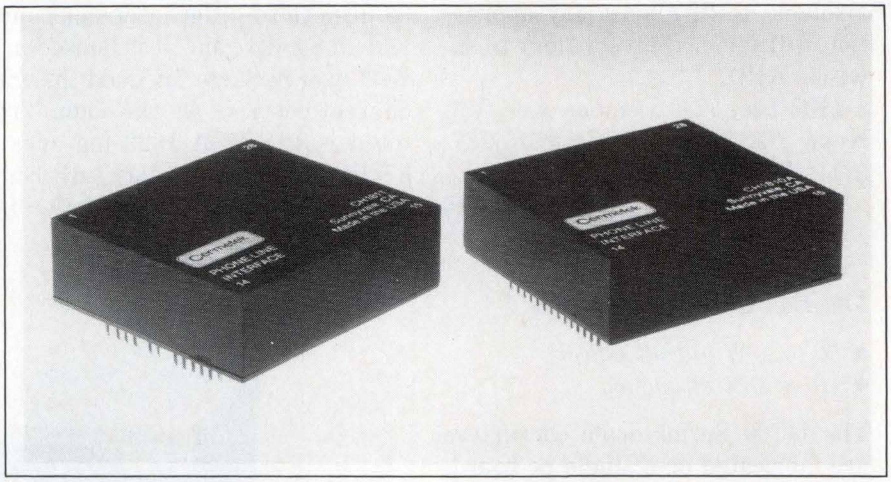
Avantek Inc, 3175 Bowers Ave, Santa Clara, CA 95054. Phone (408) 970-2659.

Circle No 380

INTEGRATED CIRCUITS

LINE-INTERFACE ICs

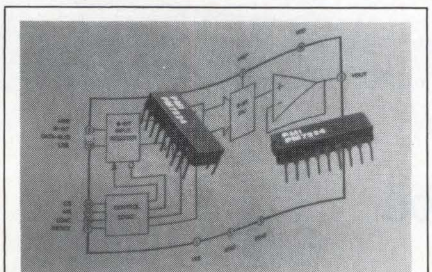
- *Suits voice and data applications*
- *FCC approved*



Suitable for voice and data applications, the CH1811 and CH1810A are modular circuits called telephone-line interfaces, or data-access arrangements (DAAs). These circuits provide an interface between the public switched-telephone network (PSTN) and a data-communications circuit such as a modem chip set. They are FCC approved. Common features of the two circuits include hook-switch control, a ring detector, pulse-dial capability, squelch control, 2- to 4-wire conversion, and billing delay. The CH1811 has a 5V supply that allows the use of a single DAA for both voice and data communications. You can adjust the device's power levels in the 1-dBm increments characteristic of leased-line operations. The CH1810A is a lower-profile version of the vendor's CH1810; it suits data applications only and requires a positive-voltage supply. CH1811, $54; CH1810A, $49 (1000).

Cermetek Microelectronics Inc, 1308 Borregas Ave, Sunnyvale, CA 94088. Phone (408) 752-5000. TWX 910-379-6931.

Circle No 381



CMOS DAC

- *Features 8-bit resolution*
- *Includes a voltage output*

The PM-7224 is an 8-bit, multiplying D/A converter. Its output amplifier can source 5 mA and drive a 3300-pF capacitive load. The double-buffered input latches reduce digital feedthrough and allow simultaneous updating in a multiple-converter system. In addition, the device has a zero-override reset input, which is useful during power-up and for periodic calibrations. It can operate from a 15V supply, a 5V supply, or a dual 15/−5V supply. The data bus and control inputs are TTL and 5V-CMOS compatible. The converter comes in a 0.3-in.-wide, 18-pin DIP. Commercial grade, $3.96; MIL-STD-883 version, $27.84 (100).

Precision Monolithics Inc, Box 58020, Santa Clara, CA 95052. Phone (408) 727-9222. TWX 310-371-9541.

Circle No 382

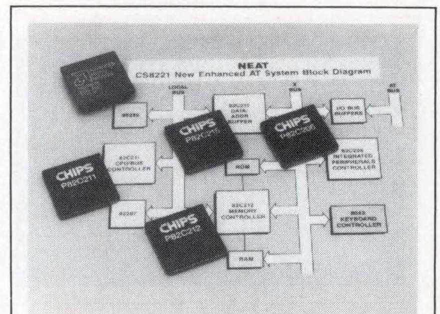
CLOCK GENERATOR

- *Has 125-MHz differential output*
- *Handles video data words from four to 32 bits*

The DP8530 video clock generator (VCG), suitable for use in lower-frequency graphics systems, is a less-expensive version of the vendor's DP8512 VCG. Fabricated in an oxide-isolated bipolar process, the DP8530 uses a crystal oscillator and a PLL to generate a graphics-processor clock, a raster-scan pixel clock, and the gated- and nongated-load clocks required to transfer data from a video RAM to video shift registers. The pixel clock has a 125-MHz max differential-ECL output. You can refer the ECL circuitry to a positive or negative power supply. The device accommodates video-data word widths from four to 32 bits in 4-bit increments. It is available in a 28-pin plastic chip carrier. $17 (1000).

National Semiconductor Corp, Box 58090, Santa Clara, CA 95052. Phone (408) 749-7431. TLX 346353.

Circle No 383



PC/AT CHIP SET

- *Chips for PC/AT-compatible design*
- *Provide 16-MHz performance*

The Neat chip set provides IBM PC/AT-compatible designs with 16-MHz capability. The chip set con-

Continued on pg 232

HARD-TO-FIND SIGNALS A SOURCE OF DELAY?

Look at the Tek 2465A with a 17-bit Word Recognizer. It's an easy, economical scope option that makes the critical difference when you need to trigger on data to monitor digital system performance. Parallel bus information **triggers** your display, so you can view up to four channels of real-time information. Add standard features such as 350 MHz bandwidth, on-screen cursors, 500 ps/div time base and trigger level readout, and you have a scope **made** for solving tough problems in digital design!

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You can tailor the 2465A for special needs. Or choose one of three multiple-option packages, the 2465A Special Editions. They are configured for specific application areas at a significant savings over the separately ordered options.

The 2465A CT with Counter/Timer/Trigger offers crystal-controlled timing accuracy plus the extra triggering power you need for digital systems.

Frequency and period can be measured with counter accuracy from any vertical channel directly. Or set up the scope to measure time intervals such as pulse width, rise time and propagation delay. Then store instrument setups in nonvolatile memory—for easy access and automatic execution.

Check Tek software development packages. They make it easy to generate automated and semi-automated test procedures, even without prior GPIB-programming experience. Use the simple, multi-level menus to develop sophisticated test programs.

Software is available to operate with the Tektronix 4041 controller, IBM PC, XT,™ AT® and compatibles.

Key Features	2465A DV	2465A DM	2465A CT	2465A	2445A
Probe Tip Bandwidth	350 MHz	350 MHz	350 MHz	350 MHz	150 MHz
No. of Channels	4	4	4	4	4
Horizontal Accuracy	2% (.001%*)	2% (.001%*)	2% (.001%*)	2% (.001%*)	2% (.001%*)
Max. Sweep Speed	500 psec	500 psec	500 psec	500 psec	1 nsec
Vertical Sensitivity	2 mV/div	2 mV/div	2 mV/div	2 mV/div	2 mV/div
Trigger Frequency	500 MHz	500 MHz	500 MHz	500 MHz	250 MHz
GPIB	Standard	Standard	Standard	Optional	Optional
Counter/Timer/Trigger/Word Recognizer	Standard	Standard	Standard	Optional	Optional
Digital Multimeter	Standard	Standard	Not Available	Optional	Optional
Video Trigger	Standard	Not Available	Not Available	Optional	Optional
Probes	4	4	4	2	2
Warranty	3 years on parts and labor, including CRT				

*with Counter/Timer/Trigger

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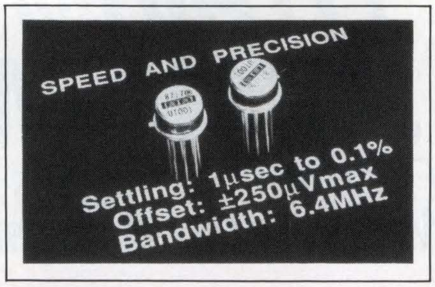
CIRCLE NO 77

sists of the 82C211 bus/clock controller, the 82C212 interleaved page-mode controller, the 82C206 integrated-peripherals controller, and the 82C215 address/data buffer. By adding 20 chips (mostly buffers), you can design a 16-MHz, PC/AT-compatible computer that's complete except for system memory. The chip set maintains IBM PC/XT and PC/AT compatibility during 16-MHz operation by using dynamic bus-clock switching and programmable wait states. The dynamic bus-clock feature lets you introduce an independent clock that operates asynchronously with the processor's 16-MHz clock, thereby allowing the system to use add-in cards designed for operation at 8 MHz, for example. CS8221-16 (16-MHz version), $136.80 (100).

Chips and Technologies Inc, 521 Cottonwood Dr, Milpitas, CA 95035. Phone (408) 434-0600.

Circle No 384



FET OP AMP

- *6.4-MHz bandwidth*
- *Settles to ±0.01% in 1 µsec typ*

The OPA602 FET-input op amp combines a 6.4-MHz bandwidth and 35V/µsec slew rate with a 0.25-mV V_{OS} max and a 0.01% settling time of 1 µsec typ. The noise-voltage density is 12 nV/$\sqrt{Hz}$ from 10 Hz to 10 kHz. The load-impedance condition for all ac and dc specs is 1 kΩ in parallel with 500 pF. The op amp can drive a 500-pF load while in the unity-gain configuration. The device comes in a TO-99 package specified for the industrial or military temperature range and has four performance grades. From $4.50 (100).

Burr-Brown Corp, Box 11400, Tucson, AZ 85734. Phone (602) 746-1111. TLX 666491.

Circle No 385

TRANSCEIVER

- *Provides OSI layer-1 functions for D^2B bus*
- *Operates at data rates as high as 1M bps*

The SAA1045 transceiver is capable of using low-cost twisted-pair cabling to transmit data over a distance of 150m; it suits office, home, industrial, and automotive applications. Intended for use with the company's 100k-bps serial D^2B bus (digital data bus), the transceiver provides the layer-1 (physical layer) functions of the OSI model. The vendor is developing a controller to implement layer-2 functions. The transceiver incorporates a digital filter that accepts only changes that are stable within two clock periods, thereby improving system noise rejection. By disabling the on-chip digital filter, you can increase the data rate of the transceiver to around 1M bps. The transceiver also has 20 mV of input hysteresis to help reject line noise. Irrespective of the data on the bus, the bus carries a common-mode voltage of 2.5V, with a high logic level represented by a differential voltage of <20 mV, and a low logic level represented by a differential voltage of >120 mV. You can wire AND data onto the bus. Connected devices require a common ground. The SAA1045 comes in an 8-pin DIP or small-outline surface-mount package, and its maximum active power dissipation is 300 mW. It uses a 5V supply and operates over −20 to +80°C. Approximately gld 3.70 (100).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 386

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-4571.

Circle No 387

CHIP SET

- *Five-chip IBM PC/AT equivalent*
- *Clock frequencies range from 6 to 12.5 MHz*

The 5-member FE3500 chip set provides the core logic and the memory and I/O control necessary to implement a 16-bit, 80286-based, IBM PC/AT-type of personal computer. In addition, the CMOS chip set allows the inclusion of Western Digital's standard peripheral-, communications-, and video-controller chips. The set consists of five devices: The FE3000A AT-CPU control-logic chip, which integrates all the control logic that supports the 80286 µP; the FE3010 AT peripheral-control logic chip, which contains 15 interrupt channels, three timer channels, and seven DMA channels and which supports 256k- and 1M-bit RAM chips; the FE3020 AT address-buffer chip (address buffers and memory read/write control buffers); the FE3030 data-buffer chip (AT system data buffers and control logic); and the FE3040 I/O-manager chip. The FE3040 includes multispeed control logic and decode/mapping logic, and provides a decoupled peripheral bus that supports programmable bus speeds and wait states. Using software, this chip can synchronously change the system clock frequency over the 8- to 12.5-MHz range. The FE3040 comes in a 68-pin, J-lead, surface-mount plastic chip carrier; the other chips come in the same package, but have 84 pins. $95 (1000-set qty).

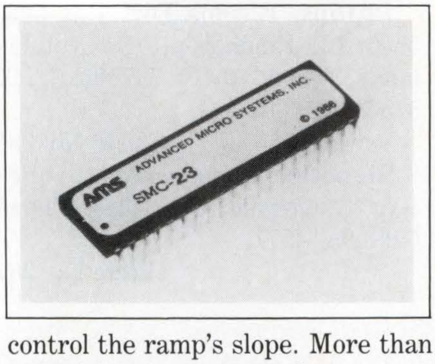
Faraday Electronics Inc, 749 N Mary Ave, Sunnyvale, CA 94086. Phone (408) 749-1900. TLX 706738.

Circle No 388

MOTOR CONTROLLER

- *RS-232C or parallel interface*
- *Serial control at rates to 9600 baud*

The SMC-23 stepper-motor controller lets you specify speed in steps per second. Initial and final motor velocities are independent variables. The monolithic IC can generate motor-phase, clock, direction, and status outputs. It accommodates an RS-232C or parallel interface to the external controller. The device comes in a 40-pin DIP, provides bidirectional ramping between motor speeds, and lets you control the ramp's slope. More than 30 high-level commands let you loop on port, count delays, set or clear ports, and implement limit- and home-sensor inputs. The device offers both serial daisy-chaining to 9600 baud and a simple bus interface. You can evaluate the controller by using the company's EVB-23 evaluation board, which includes RS-232C buffers, program memory, and motor drivers. $94.



Advanced Micro Systems Inc, 31 Flagstone Dr, Hudson, NH 03051. Phone (603) 882-1447, ext 23.

Circle No 389

SYNTHESIZER

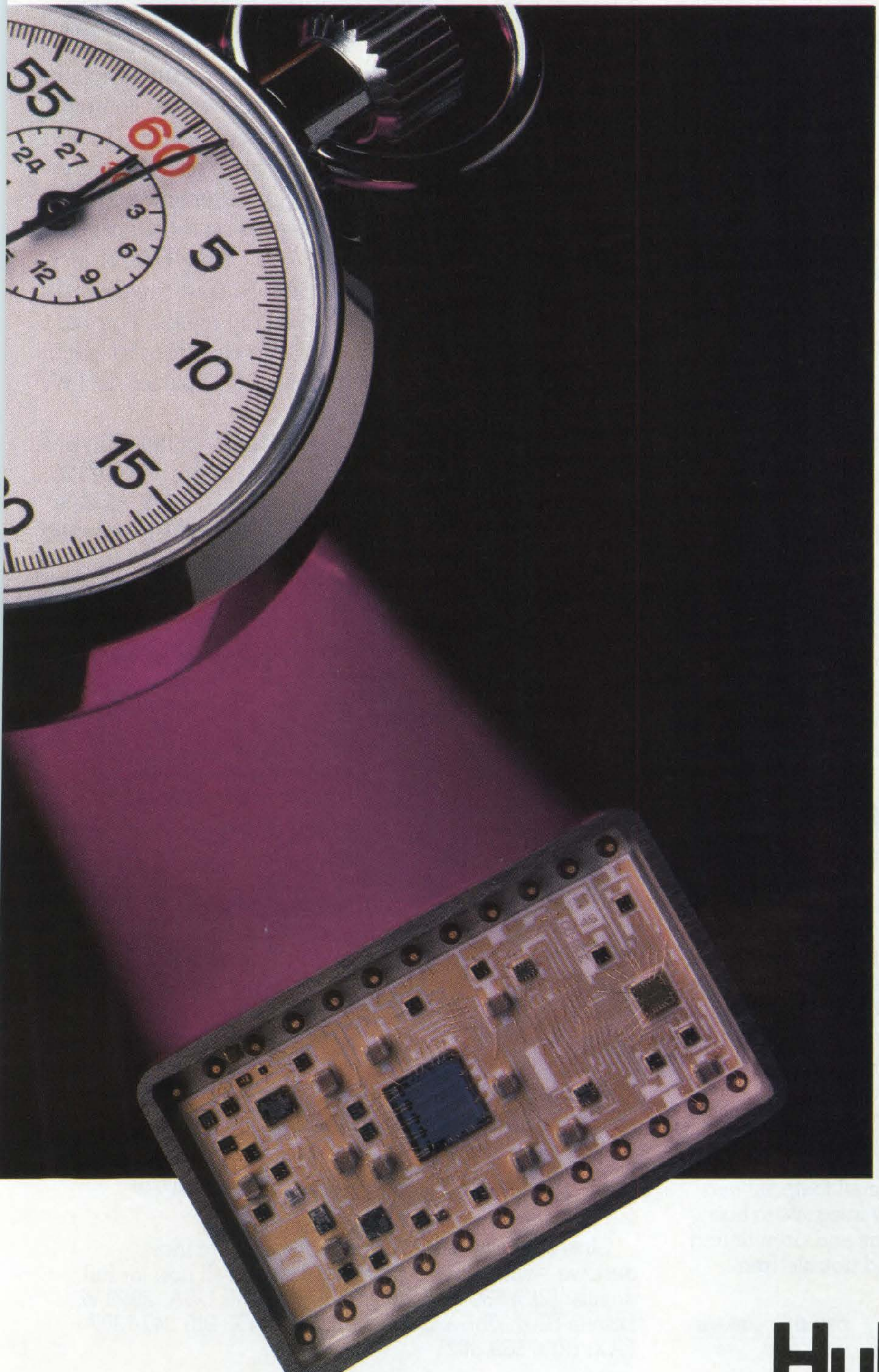
- *DC-to-8-MHz frequency range*
- *0.001-Hz resolution*

The Model 1080 frequency synthesizer can produce sine-wave signals from dc to 8 MHz with 0.001-Hz resolution. Its accuracy and stability depend either on an external source or on the internal, ±100-ppm, 20-MHz reference. The switching time between frequencies is phase continuous and requires less than 1 μsec. The output can drive a 50Ω load to 500 mV with less than −50 dBc of spurious and harmonic components. The case measures 4.0×5.5×0.5 in. Further, the device has TTL-compatible square-wave outputs, output phase-reset control, and provision for BCD programming of frequency. $990 (100).

Pentek Inc, 10 Volvo Dr, Rockleigh, NJ 07647. Phone (201) 767-7100.

Circle No 390

Real-Time In No Time.

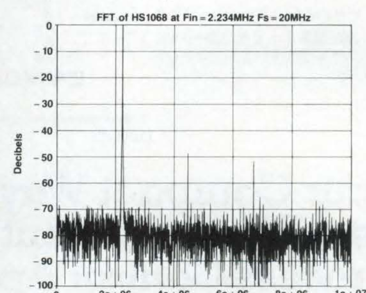


Our HS 1068 ADC combines a flash converter with all the necessary analog support circuitry into one unit so that you can access real-time capabilities instantly.

Flash converters broke through the time barrier in A/D conversion. Now, Hybrid Systems shatters the barriers to fast, convenient flash converter integration.

Our HS 1068 takes an industry-standard flash converter; adds a voltage reference, input buffer, and tri-state output; and places them all on one hybrid that's actually smaller than a package containing a flash converter alone. Yet the HS 1068 offers all these features:

- 20MHz minimum sampling rate
- No spurious codes—7MHz, 13MHz typ.
- No missing codes—to 10MHz typ.
- Aperture jitter of 60ps.
- Aperture error of 1LSB at 20MHz input—no sample/hold required for input frequencies lower than 10MHz.
- Signal-to-noise ratio of 46dB—true 8-bits
- Dynamic testing



Most important, you can integrate the HS 1068 into your applications in no time . . . no kidding.

With full MIL-STD-1772 Certification, Hybrid Systems can process the HS 1068 to the most stringent military and commercial specifications, including MIL-STD-883C.

The Hybrid Systems HS 1068: for video digitizing, radar, EW systems, high speed signal processing and all other applications that demand real-time A/D conversion, it's a component whose time has come.

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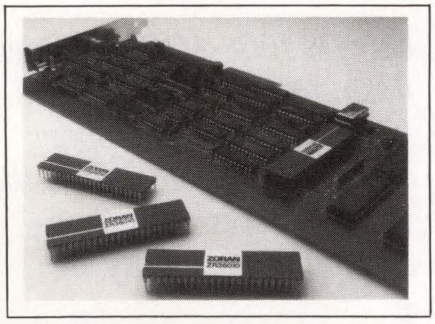


IMAGE PROCESSOR

- *Compresses video data at a ratio of 10:1*
- *Produces recognizable image using only 4% of data*

The ICP image-compression processor can reproduce compressed images 10 times faster than any digital signal processor currently available, according to the manufacturer. The device suits still-frame image compression in commercial and military applications such as electronic publishing, video conferencing, and military satellite reconnaissance. The processor reconstructs an image on the CRT in steps, progressively adding detail until the picture is complete. This approach allows you to look quickly through a database of images without waiting for a complete reconstruction of each one. $99 (OEM qty).

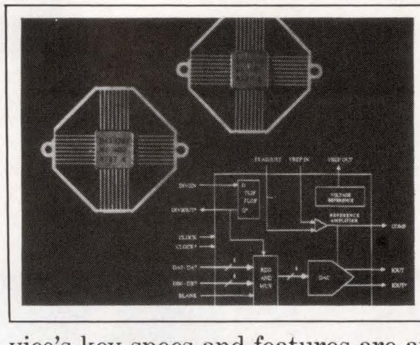
Zoran Corp, 3450 Central Expressway, Santa Clara, CA 95051. Phone (408) 720-0444.

Circle No 391

VIDEO DAC

- *Promises 400-MHz operation*
- *Onboard voltage reference included*

The Bt107 is a monolithic-bipolar video D/A converter. By multiplexing two input ports using a master flip-flop, the device achieves a guaranteed 400-MHz operating rate, wherein the data bandwidth is half the clock frequency. Among the de-



vice's key specs and features are an on-chip voltage reference, compatibility with 10KH or 100K ECL, a 0- or 7.5-IRE (Institute of Radio Engineers) blanking pedestal, and ±½ LSB max integral- and differential-linearity errors. The DAC's RS-343A-compatible output can directly drive a 75Ω coaxial cable. The part comes in a 32-pin ceramic flat pack; its typical power dissipation is 1W. $103 (100).

Brooktree Corp, 9950 Barnes Canyon Rd, San Diego, CA 92121. Phone (619) 452-7580. TLX 383596.

Circle No 392

CIRCLE NO 73

GRAPHICS CHIP

- *64-byte×8-bit organization*
- *200-MHz operation*

The Am8172 VDAF is a video-data-assembly FIFO-buffer IC that supports high-resolution windows without destroying the data currently displayed. Positioned in a graphics system between the display memory and the color palette or monitor, the VDAF allows nondestructive overlay of hardware windows. The device provides smooth, jitterless panning and supports hardware windows on pixel boundaries rather than on the conventional word boundaries, so it allows more flexibility in window sizes. Its 200-MHz operation provides high-resolution windows. The internal 64-byte×8-bit FIFO buffer provides a temporary buffer between the memory and display, allowing a continual flow of data to the display while you update or modify the memory contents. The ECL device comes in a 24-pin ceramic DIP. $31.43 (100).

Advanced Micro Devices Inc, Box 3453, Sunnyvale, CA 94088. Phone (408) 732-2400.

Circle No 393

ANALOG SWITCH

- *100-MHz −1-dB bandwidth*
- *70-dB off-isolation at 10 MHz*

The CDG201 quad analog switch is fabricated with a process that combines CMOS and DMOS (double-diffused CMOS) technology. Suitable for use in wideband-RF and low-noise-video switches, the device has a TTL-compatible control input and an industry-standard pinout. Its specs include a 100-MHz −1-dB bandwidth, off-isolation of 70 dB at 10 MHz and 40 dB at 100 MHz, a ±10V input range, and a max 600-nsec turn-on time for the switches. The switch's on-resistance is 45Ω typ. The device requires ±15V supplies and dissipates 45 mW typ under quiescent conditions. It comes in a 16-pin plastic or ceramic DIP and is specified for the commercial, industrial, and military temperature ranges. From $2 (100).

Topaz Semiconductor, 1971 N Capitol Ave, San Jose, CA 95132. Phone (408) 942-9100. TWX 910-338-0025.

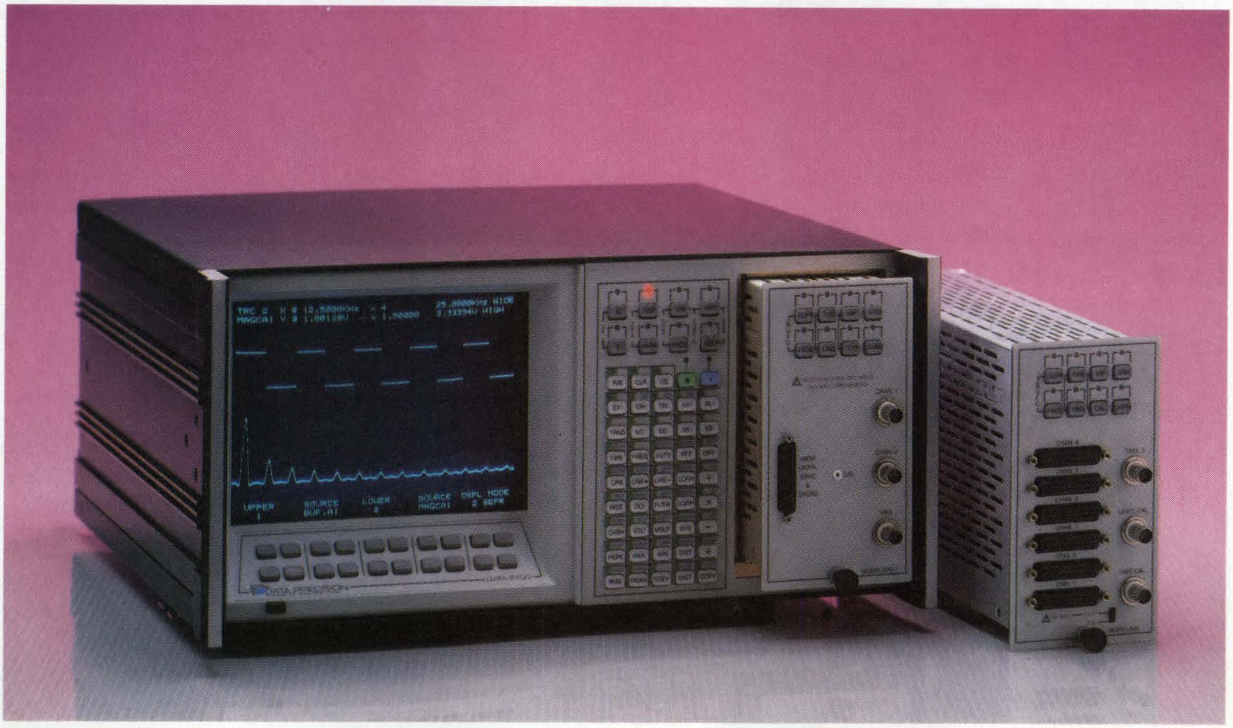
Circle No 394

TELETEXT IC

- *Compatible with all current Teletext standards*
- *Includes 8-bit μP and I²C interfaces*

The SAA5250 Teletext data-acquisition IC is compatible with all current Teletext standards including the French Didon Antiope system, the North American Broadcast Teletext System (NABTS), and the

The Most Powerful Instrument of its Kind in the World Today.



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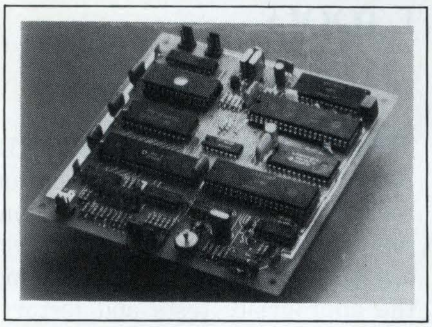
ANALOGIC GmbH, Daimlerring 2, 6200 Wiesbaden-Nordenstadt, W. Germany. Tel: 06122-70060, Telex: (17)6122969 ANA D.

CIRCLE NO 72



UK Ceefax system. It receives the standard Teletext and Datacast broadcasts that are transmitted during the vertical blanking interval of TV transmissions as well as full-channel packet-switched data transmissions. The device demultiplexes data from one of as many as 4000 packet-switched channels, correcting single-bit errors and detecting multiple-bit errors. It interfaces directly to 8-bit µPs and microcontrollers and, with the addition of a few TTL components, to 16-bit µPs. It can also communicate with other ICs via its on-chip I²C interface. It has a 7.5-MHz max conversion rate, and it evaluates the validation and color-burst blanking signals to synchronize the Teletext data to the TV picture. This CMOS device comes in a 40-pin plastic DIP or a 40-lead surface-mount package. Around Gld 35 (for quantities of less than 100).

Philips, Elcoma Div, Box 523, 5600 AM Eindhoven, The Netherlands. Phone (040) 757005. TLX 51573.

Circle No 395

Signetics Corp, 811 E Arques Ave, Sunnyvale, CA 94088. Phone (408) 991-4571.

Circle No 396

COMPARATORS

- *Features gain of 35,000*
- *Has propagation delay of 20 nsec*

The EL2018 and EL2019 comparators are fabricated with a dielectrically isolated process that provides nearly identical high-voltage pnp and npn transistors. The EL2018 is a conventional comparator with an industry-standard pinout. It has a typical gain of 35,000 and a typical propagation delay of 20 nsec. The EL2019 has an internal master-slave, edge-triggered flip-flop that virtually eliminates the problem of comparator oscillation. The speed for this device is expressed as 15 nsec from clock to output, with a 5-nsec setup time. Common features of the two comparators include a 60-nA bias current, a 40V (±20V) differential input range, a 2- to 4-mV input offset (typ), and 3-state outputs. EL2018 and EL2019, $4.50 (100) each.

Elantec Inc, 1996 Tarob Ct, Milpitas, CA 95035. Phone (408) 945-1323.

Circle No 397

CAE & SOFTWARE DEVELOPMENT TOOLS

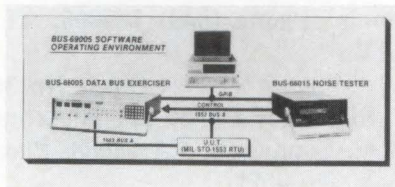
OPERATING SYSTEM

- *Provides enhanced Unix operating system for the 80386 μP*
- *Source-level compatible with Unix 4.3 bsd*

Uniplus+/386 is a version of the company's enhanced Unix operating system, which runs on Intel's 80386 μP. The enhancements include the Network File System (NFS), which allows you to share files across networks that link different machines with different operating systems and communications protocols; and Fast File System (FFS), which speeds up disk access as much as 10 times. In addition, Uniplus+/386 allows you to develop applications software in various national languages. It also has a special mode that provides source-level compatibility with Unix 4.3 bsd. Typical OEM licencing arrangements result in a cost per copy of around $200.

Root Technical Systems, Saunderson House, Hayne Street, London EC1A 9HH, UK. Phone 01-606 7799. TLX 885995.

Circle No 400



BUS-TEST SOFTWARE

- *Performs a full set of protocol tests for -1553 bus equipment*
- *Lets a PC drive a bus exerciser and noise generator*

The BUS-69005 protocol-test software package runs on an IBM PC or compatible. It uses the vendor's BUS-68005 data-bus exerciser and BUS-68015 noise generator to perform all protocol tests outlined in Section 5.2 of the SAE RTU Production Test Plan (PTP) for MIL-STD-1553 devices. The menu-driven software lets you perform the complete RTU protocol PTP, conduct any subgroup of tests by selecting the appropriate tests and factory-defined or user-definable fault parameters, and select control features such as halt on error, single execution, or continuous testing. For each type of unit to be tested, you construct a configuration file describing the unit's capabilities, the tests to be performed, and any other relevant data. You can store multiple configuration files on a single disk. An on-line Help feature lets you select a test title on a menu and review the corresponding SAE-document paragraph. You can print configuration files as well as test results. $995.

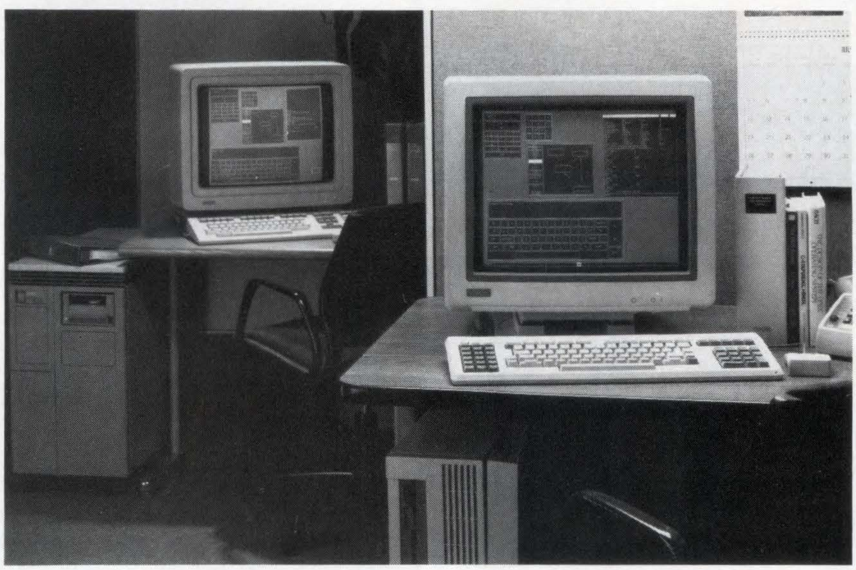
ILC Data Device Corp, 105 Wilbur Pl, Bohemia, NY 11716. Phone (516) 567-5600. TWX 510-228-7324.

Circle No 401

NETWORK INTERFACE

- *Based on X Window system for graphics*
- *Provides common interface for multimachine applications*

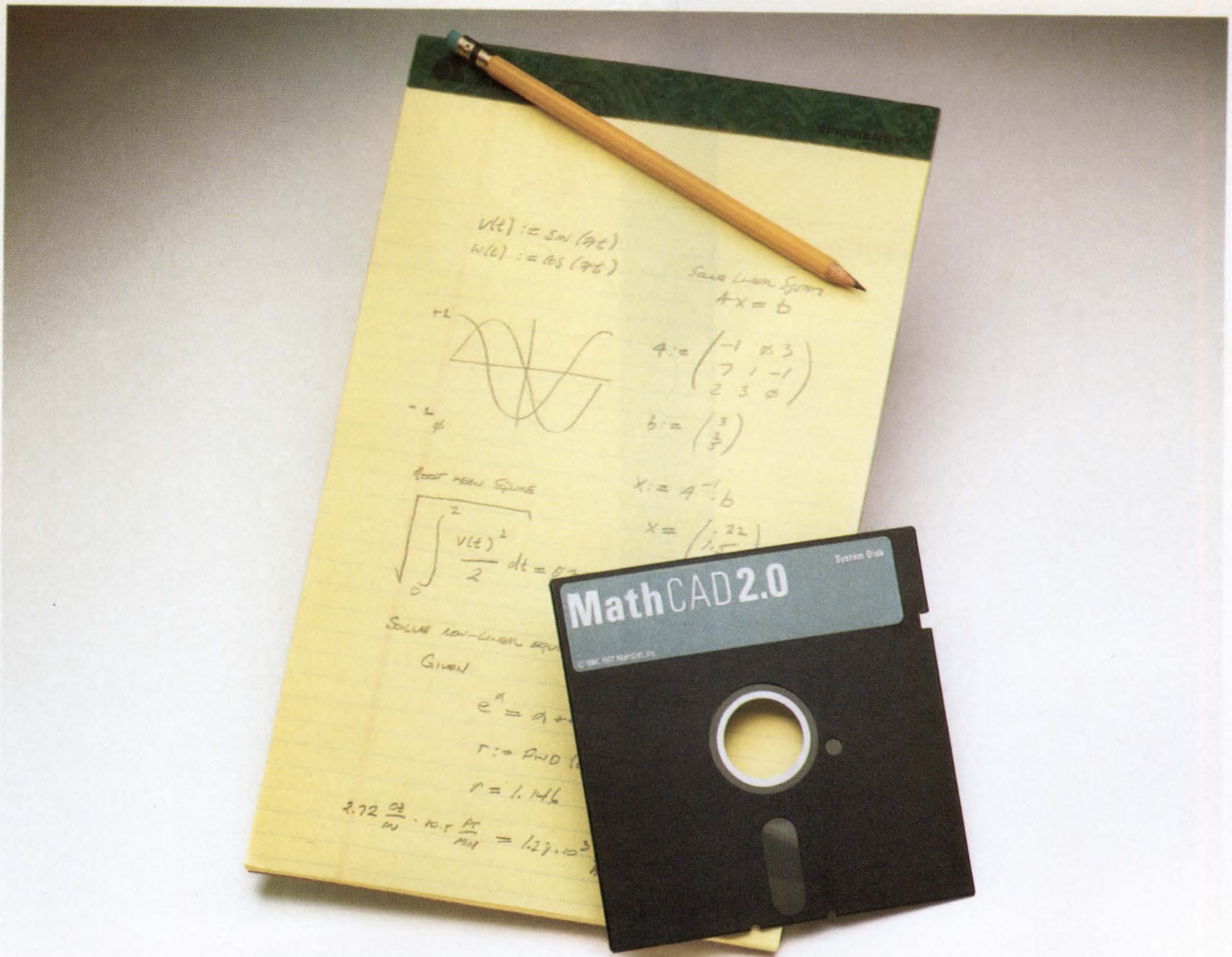
Open Dialogue is a software-development tool that lets you design graphical user interfaces that remain consistent regardless of the machine on which an application runs. Based on the X Window system developed at MIT, this tool unifies the user interface among different vendors' computers connected in a network, and makes it easier for users to run a given application from any of the machines. The package provides the high-level building blocks needed for management of the user-interface system; it lets you create customized interfaces with minimal coding and debugging. You can also create common user interfaces for different applications.



The package is available for Apollo workstations; a version for the DEC GPX workstation will be released in January 1988, followed by versions for the Sun and IBM RT PC workstations in March 1988. From $2000 for a single copy.

Apollo Computer Inc, 330 Billerica Rd, Chelmsford, MA 01824. Phone (617) 256-6600. TWX 710-343-C803.

Circle No 402



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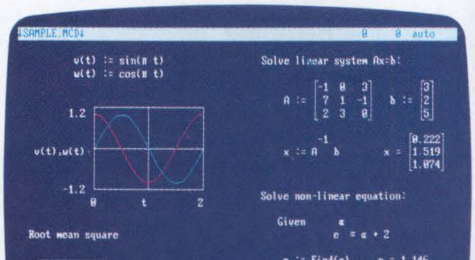

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LIBRARIAN

- *Provides pattern-recognition facilities*
- *Searches 1200 entries in one minute*

Fetch is a RAM-resident librarian that runs on the IBM PC/XT, PC/AT, and compatibles. When you create a new file from within an application program, Fetch prompts you for a description of the file. The description may consist of as many as 255 characters. At some later date, if you need to load the file but don't remember its exact name and don't want to go back to DOS, you can activate Fetch and search the file-description library for a key word or phrase; Fetch will find your file and display the description, file name and type, and the drive on which the file resides. According to the vendor, on an 8-MHz machine the program takes no more than one minute to search 1200 library entries for your key phrase. $79.95.

Thought Dynamics, 1142 Manhattan Ave, Suite CP-310, Manhattan Beach, CA 90266. Phone (213) 546-2958.

Circle No 403

FORTRAN VECTORIZER

- *Analyzes standard Fortran code to detect vector operations*
- *Constructs code that runs on a vector processor*

Vast-2 is an optimizing Fortran compiler for the vendor's iPSC-VX parallel computer. The compiler accepts source code written in Fortran-77 and 8x vector syntax and builds optimized code for execution on each of the iPSC-VX's nodes. It provides directives for controlling vectorization at the Fortran level, and diagnostic functions that help you optimize the code for vector execution. The compiler detects vector constructs in the application code and translates them into operations that can be performed by VecLib math-library subroutines. It vectorizes DO loops and IF loops and analyzes data dependencies to ensure safe translation of these loops; it also examines EQUIVALENCE statements to detect hidden recursion and, where possible, reorders array references to avoid such recursion. It translates scalar instructions into iPSC-VX scalar operations and takes advantage of the vector-processor's architecture to provide balanced vector/scalar performance. The compiler combines the vector and scalar operations to build execution modules that run as complete subroutines in a vector processor, thereby minimizing overhead and maximizing performance. Running the Livermore Loops, a benchmark of vectorizing efficiency, the vendor's compiler successfully vectorized 18 of 24 loops. $10,000.

Intel Scientific Computers, 15201 NW Greenbrier Parkway, Beaverton, OR 97006. Phone (503) 629-7629.

Circle No 404

PASCAL DEBUGGER

- *Monitors set conditional breakpoints*
- *Debugs programs that use CGA, EGA, or Hercules graphics*

T-Debugplus version 2.0 is a symbolic run-time debugger for Turbo Pascal. The original program displayed Turbo Pascal heap-management information, IORESULT values, and the contents of machine registers; it also debugged programs that use overlays and generated MAP files that are fully compatible with other debuggers. Version 2.0's principal enhancements are the ability to set conditional breakpoints that pass control to the program when a variable reaches a specified value or when a variable or a memory range is changed; the ability to create a window that displays a specified memory area and to browse through memory with the aid of the cursor keys;

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CIRCLE NO 67

and the ability to create a window that displays variable values at every breakpoint. This version also lets you examine the sequence of calls that led to a current breakpoint, and lets you use either a single monitor or dual monitors to debug programs that employ CGA, EGA, or Hercules graphics modes. Another new feature lets you search the symbol table for a partial identifier name and display the items that match it, as well as their types, sizes, addresses, and values. The package includes the source code and executable binary code. $60.

TurboPower Software, 3109 Scotts Valley Dr, Scotts Valley, CA 95066. Phone (800) 538-8157, ext 830; in CA, (800) 672-3470, ext 830.

Circle No 405

PC-TO-DEC LINK

- *Lets IBM PC users access a DEC host*
- *Provides VT220 emulation and dual-mode IBM/DEC keyboard*

The IBM PC Network-Integration Package allows IBM PC users to access multiple VAX/VMS hosts via a DECnet local-area network. The package includes the vendor's Ethernet controller, a dual-mode IBM/DEC keyboard, a mouse, MS-Windows, and VT220 terminal emulation, which lets you establish multiple VT220 terminal sessions to one or more VAX hosts under the control of MS-Windows. You can access all the network's files, data, and hardware resources. The IBM PC Network Services Package provides the same network facilities, but

does not include the mouse, the keyboard, MS-Windows, or VT220 terminal emulation—you have to employ the standard MS-DOS command-line interface to the operating system and the network. To use either package, you need an IBM PC/XT or PC/AT with 640k bytes of RAM, CGA or EGA graphics, PC-DOS 3.10 or higher, a system ROM BIOS dated 10/27/82 or later, a spare expansion slot, and a 130W power supply. Network Integration Package, $1195; Network Services Package, $895.

Digital Equipment Corp, 146 Main St, Maynard, MA 01754. Call local office.

Circle No 406

C COMPILER FOR DSP

- *Lets you write C programs for DSP processors*
- *Runs under VAX/VMS or PC-DOS*

The TMS320C25 C compiler accepts a digital signal processing program written in C and outputs TMS320 assembly-language source code; the TMS320C25 assembler then converts the assembly-language mnemonics to object code. The compiler provides all the C-language features specified by the Kernighan and Ritchie reference manual. TMS320C25: VAX/VMS version, $5000; PC- or MS-DOS version, $2500.

Texas Instruments, Semiconductor Group, Box 809066, Dallas, TX 75380. Phone (800) 232-3200, ext 700.

Circle No 407

WINDOWS FOR XENIX

- *X Windows runs under Xenix-386*
- *Provides XLIB functions, utilities, and display server*

GSS*X/386 is an implementation of the X Window System version 11 that runs under Xenix System

CAE & SOFTWARE

V-386 release 2.2 or higher. It allows microcomputers that run Xenix 386 to share applications with workstations, minicomputers, and mainframes that also run the X Window System. The graphical, network-transparent windows allow you to simultaneously view and operate applications on several hosts; in addition, you can run X Window-compatible applications on stand-alone microcomputers. To run this software, you need a computer that has an 80386 CPU, 2M bytes of RAM, a hard-disk drive, and (for network operation) a TCP/IP-compatible network interface board. GSS*X/386 development package, $595; application-environment runtime module, $195.

Graphic Software Systems Inc, Box 4900, Beaverton, OR 97005. Phone (503) 641-2200. TLX 4994839.
Circle No 408

RIP-UP ROUTER

- *Performs orthogonal or 45° routing*
- *Optimizes memory-array routing without using vias*

According to the vendor, the Strategic Automatic Router (STAR) routes most pc boards to 100% completion. The program runs on the IBM PC/AT and compatibles, and on the vendor's Personal Logician 386 and Boardmaster workstations. Single-user and multiuser versions are also available for VAX computers. The program uses a fast initial pass that performs either orthogonal or 45° routing and optimizes memory-array routing without vias. On designs with 45° connections, you can run a 45° pass and assign a diagonal-left or diagonal-right preference, providing high trace density and minimizing the length of connections between devices. The rip-up rerouting pass takes maximum advantage of the available space; you can run this pass in an optional 45° mode and allow or forbid vias. The manufacturing pass

not only smooths and chamfers end points and removes vias, it also sequentially rips up and reroutes individual traces to optimize trace spacing, connection length, and trace entry into pads. PC/AT version, $8000; Personal Logician version, $12,000; VAX versions from $18,000.

Daisy Systems Corp, 700 Middlefield Rd, Mountain View, CA 94039. Phone (415) 960-0123.

Circle No 409

GRAPHICS TOOLKIT

- *Operates with advance release of OS/2*
- *Compatible with DOS Graphics Development Toolkit*

An advanced release of the vendor's OS/2 Graphics Development Toolkit (GDT) lets you develop graphics applications to run under the OS/2 operating system. Because the OS/2 GDT is source-code compatible with the DOS GDT, you can use it to adapt existing DOS applications to run in the protected mode of an 80286-based computer, as well as to develop new applications that will run under OS/2. The advance release operates with the advance release of OS/2 from Microsoft (Redmond, WA), which is currently available for the PC/AT, PC/XT-286, and compatibles. The final version of the OS/2 GDT will operate with the final versions of Microsoft's OS/2 and IBM's Operating System/2, and on all IBM 80286- and 80386-based PS/2 microcomputers and compatibles. The advance release of OS/2 GDT includes device drivers for the video graphics array, enhanced graphics adapter, color graphics adapter, the Microsoft mouse, the IBM Proprinter, Graphics Printer, Color Graphics Printer, and Quietwriter III, as well as for plotters from IBM and Hewlett-Packard. $995.

Graphic Software Systems Inc, Box 4900, Beaverton, OR 97005. Phone (503) 641-2200. TLX 4994839.

Circle No 410

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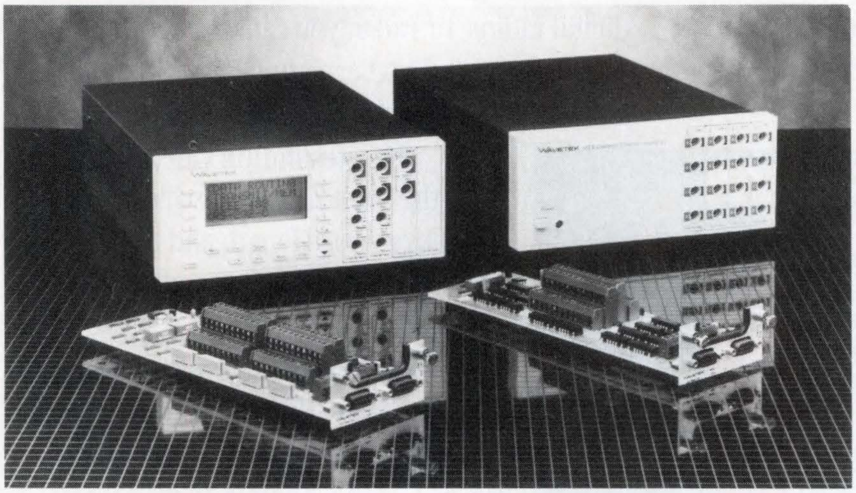


DATA LOGGER

- *Accommodates 260 channels in 5¼-in. rack space*
- *Built-in routines perform computations on captured data*

The Model 52/53 data logger accepts as many as 260 signals and can perform calculations on acquired data. The system, which has screw terminals for 256 channels, mounts in 5¼ in. of rack space and can be controlled from its panel, an RS-232C port, or an optional IEEE-488 interface. It accepts differential, single-ended, and 4-terminal inputs; its cold-junction compensation permits simultaneous connection of several types of thermocouples. The system's firmware includes routines to verify continuity and to calculate volt-amperes, frequency, period, time interval, pulse width, and decibels. Solid-state devices perform the multiplexing. From $3330; $10,380 for a system with 260 low-level channels and 768k bytes of battery-backed RAM.

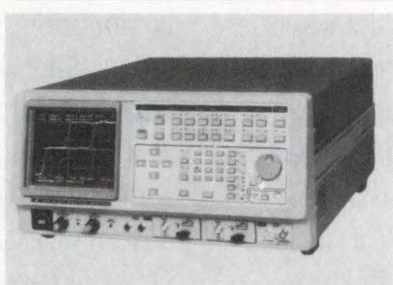
Wavetek San Diego, Box 85265, San Diego, CA 92138. Phone (619) 279-2200.

Circle No 411

WAVEFORM ANALYZER

- *Has time-measurement jitter of <20 psec*
- *Measures voltages with 10-bit resolution*

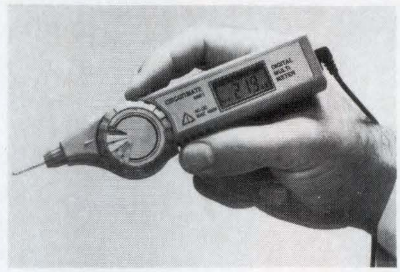
The SAS-8130 waveform analyzer is a 2-channel instrument that, when used with the manufacturer's SH-4B plug-in sampling head, can take measurements on dc to 12.4-GHz waveforms with rise times as short as 30 psec. Its internal memory can store 32 front-panel settings. The instrument comes with RS-232C and GPIB interfaces. You can add an external 3½-in. floppy-disk



drive for waveform storage and setup conditions. The analyzer has simple built-in waveform analysis routines such as signal averaging; averaging 4096 sweeps yields a 72-dB improvement in the S/N ratio. $22,000 with two 12.4-GHz heads; $19,500 with two 3.5-GHz heads. Delivery, 60 days ARO.

Iwatsu Instruments Inc, 430 Commerce Blvd, Carlstadt, NJ 07072. Phone (201) 935-5220.

Circle No 412



PEN-GRIP DMM

- *Probe and DMM are integrated*
- *Probe has sheath for ground lead*

The DM71 handheld, pen-type digital multimeter (DMM) features a 3½-digit LCD. The autoranging meter has 0.7% accuracy max and possesses a data-hold function. Unlike other pen-grip DMMs that have pushbutton function selection, this meter has a rotary dial. The unit operates for 90 hours from one battery. $49.95.

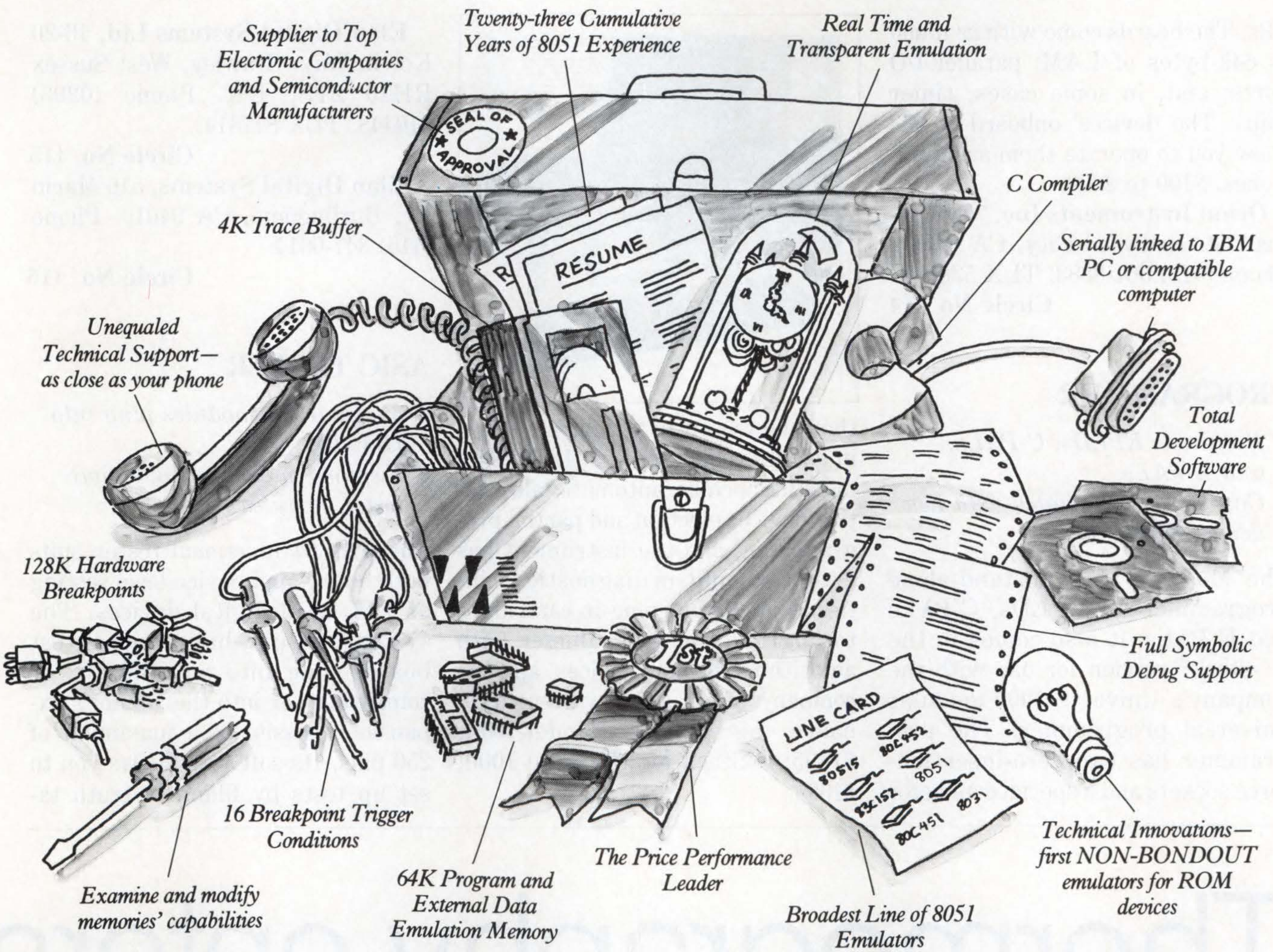
Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 565-3240.

Circle No 413

CODE EXECUTION

- *µP boards allow you to try out software*
- *Boards feature 12 different µPs*

The 14 MicroTarget boards allow you to try out your µP programs before your custom hardware is up and running. The boards emulate the 63P01, 64180, 6502, 68P05, 68000, 8031, 8051P, 8085, Z8, Z808086, or the maximum and minimum versions of the 8086 and 8088



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CIRCLE NO 137

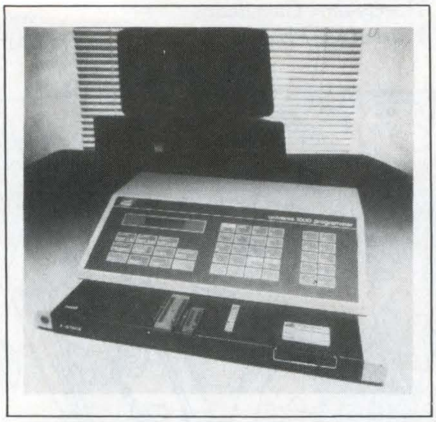
μPs. The boards come with as much as 64k-bytes of RAM; parallel I/O ports; and, in some cases, timer chips. The devices' onboard ROMs allow you to operate them as standalones. $100 to $300.

Orion Instruments Inc, 702 Marshall St, Redwood City, CA 94063. Phone (415) 361-8883. TLX 530942.

Circle No 414

PROGRAMMER

- *Programs EPLDs, C-PALs, and E-PALs*
- *Can be easily updated with new device algorithms*



The Model-1014 is a stand-alone programmer for EPLDs, C-PALs and E-PALs; it also comes in the "F-Stack" version for use with the company's Universe-1000 modular universal programmer. The programmer has two zero-insertion-force sockets and a special connector that allows you to program devices in leadless chip carriers. Its editing facilities include automatic alternative-device selection and partial programming, and the instrument has extensive built-in diagnostic facilities. You can use plug-in cartridges to upgrade the programmer with algorithms for new devices, and the company offers a software-maintenance agreement. Model-1014, £1895; F-Stack for Universe-1000, £1695.

Elan Digital Systems Ltd, 16-20 Kelvin Way, Crawley, West Sussex RH10 2TS, UK. Phone (0293) 510448. TLX 877314.

Circle No 415

Elan Digital Systems, 516 Marin Dr, Burlingame, CA 94010. Phone (415) 347-0614.

Circle No 416

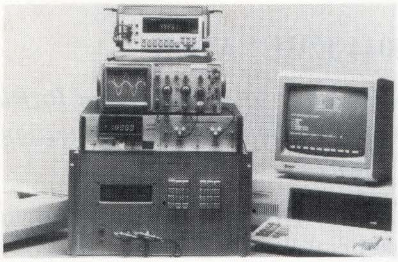
ASIC TESTER

- *64-pin tester modules plug into IBM PC*
- *Expansion chassis holds four tester modules*

The TS2064 functional tester suits both board- and device-level testing of TTL-level digital devices. The system's 64-pin, bidirectional test boards plug into an IBM PC or compatible, or into the vendor's expansion chassis, to a maximum of 256 pins. Its software allows you to set up tests by filling in truth tables. TS2064, $995 (64-pin version); additional 64-pin module, $695.

Modular Test Systems, 162 San Lazaro Ave, Sunnyvale, CA 94086. Phone (408) 732-0994.

Circle No 417



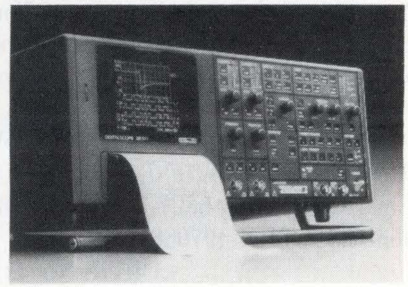
PHASE CALIBRATOR

- *IBM PC controls phase-meter calibration*
- *Calibrates as many as five phase meters simultaneously*

The GPIB Speedac phase-meter calibration package can simultaneously test and calibrate as many as five phase meters of the same model. The package includes IBM PC control software, the firm's phase standard, and an IBM PC interface board; an IBM PC clone is offered as an option. The software compiles uncertainty data for the tested meter and stores the data in ASCII files. The calibrator requires an IBM PC/XT for control and provides a pair of sine waves that you can adjust in phase to 0.001° resolution. GPIB Speedac version 1.0 software, including expansion card, $995; with PC clone, $2995. Version 5.0, for the Krohn-Hite 6620, Dranetz 3110, and North Atlantic 2250 phase meters, $2495; plus $1495 or $1995 for one or two meters, respectively, and $2000 for the clone. Phase standard, $10,350 to $12,950. Delivery, stock to 60 days.

Elpaz Instruments Inc, 160 N Craig St, Pittsburgh, PA 15213. Phone (412) 687-8700. TLX 382960.

Circle No 418



DIGITAL SCOPE

- *Has built-in printer*
- *Trace annotations include real-time clock*

The SE571 digital oscilloscope has a built-in printer. Its two channels have 25M-sample/sec, 8-bit digitizers; they also have 1k-sample memories. You can also store state samples from an 8-bit logic probe (50Ω and 1-MΩ versions are available). In addition to input waveforms, the screen and printouts from the scope's built-in printer can also show annotations such as the output from a built-in real-time clock. You can store 10 combined scope setups and waveforms in nonvolatile memory. $6500.

BBC-Metrawatt/Goerz, 2150 W 6th Ave, Broomfield, CO 80020. Phone (800) 821-6327; in CO, (303) 469-5231. TLX 4970869.

Circle No 419

FUNCTION GENERATOR

- *Synthesized function generator has 600-kHz bandwidth*
- *Combines signals from as many as four internal sources*

The HP 8094A synthesized function generator digitally combines signals from as many as four internal sources to produce complex waveforms. Its output level is 10V p-p max into 50Ω. The instrument's sources generate sine (0 to 600 kHz max), variable-duty-cycle square and triangle waves (0 to 20 kHz max), and noise by using a ROM-lookup technique. Three of the sources can modulate the fourth. The instrument performs all waveform generation and modulation digitally and thus has better signal-purity, phase-accuracy, and freguency-stability specs than do analog function generators. Noise is <−72 dB to 20 kHz typ, phase resolution is 0.1°, phase accuracy is ±0.18° channel-to-channel (< 20 kHz), and output flatness is ±0.007 dB from 0.1 to 100 kHz. An IEEE-488 interface is standard. HP 8904A, $2600; 2-channel option, $1200; four-channel option, $1500; fast-hop and digital modulation option, $500.

Hewlett-Packard Co, Inquiries Manager, 1820 Embarcadero Rd, Palo Alto, CA 94303. Phone local office.

Circle No 420

8044 EMULATOR

- *Handles 8044 family and BitBus*
- *Features 64k bytes of emulation memory*

The Ice-5100/044 handles the firm's proprietary BitBus and the 8044 family of specialized single-chip μPs. It emulates the 8344, 8044, and 8744 μPs. You need an IBM PC to control the emulator. The control software offers symbolic debugging if you use the vendor's assembler or compiler. The emulator features 64k bytes of emulation memory, a 254-sample trace memory, four breakpoints, and one range breakpoint. It

also has a built-in editor and disassembler. Ice-5100/044, $6995; without editor and assembler, $6495. 8044 upgrade for Ice-5100, $3495.

Intel Corp, Box 58065, Santa Clara, CA 95052. Phone local office.

Circle No 421

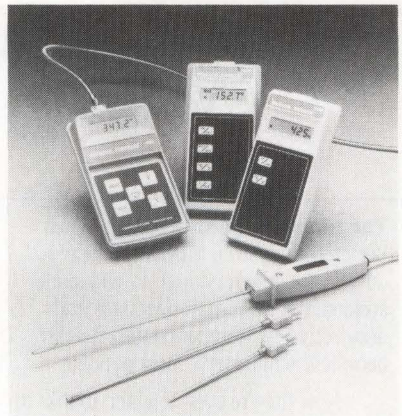
488 BUS EXPANDER

- *Allows controller to talk to 30 instruments instead of just 15*
- *Transfers data at 1M bytes/sec*

The Expander 488 links as many as 30 instruments to one IEEE-488 port. The device, which operates transparently to the 488's system controller, takes advantage of the IEEE-488's inherent ability to address 30 instruments and overcomes the electrical-loading limitations that force most 488 systems to handle only 15 addressed instruments. Maximum data-transfer rate is 1M bytes/sec. $795.

IOtech Inc, 23400 Aurora Rd, Cleveland, OH 44146. Phone (216) 439-4091. TWX 650-282-0864.

Circle No 422



DIGITAL THERMOMETERS

- *Three models offer various combinations of features*
- *Work with a variety of probe types*

The 440, 445, and 450 handheld digital thermometers possess LCDs, battery-conserving automatic shutoff features, switch-selectable °F or °C readings, and splash-proof membrane keyboards. The 440 uses type K thermocouples. The 445 has 0.1° max resolution, autoranging, and maximum/minimum hold features. The 450 has 0.1% accuracy, and touch-hold readings. It handles thermocouple, RTD, and termistor probes. 440, $99; 445, $169; 450, $295.

Beckman Industrial Corp, 3883 Ruffin Rd, San Diego, CA 92123. Phone (619) 565-4415.

Circle No 423

PORTABLE DIGITAL WAVEFORM RECORDER

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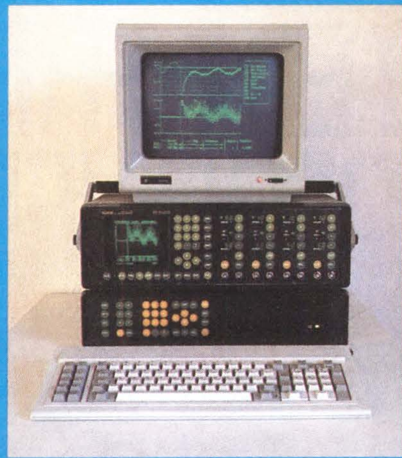

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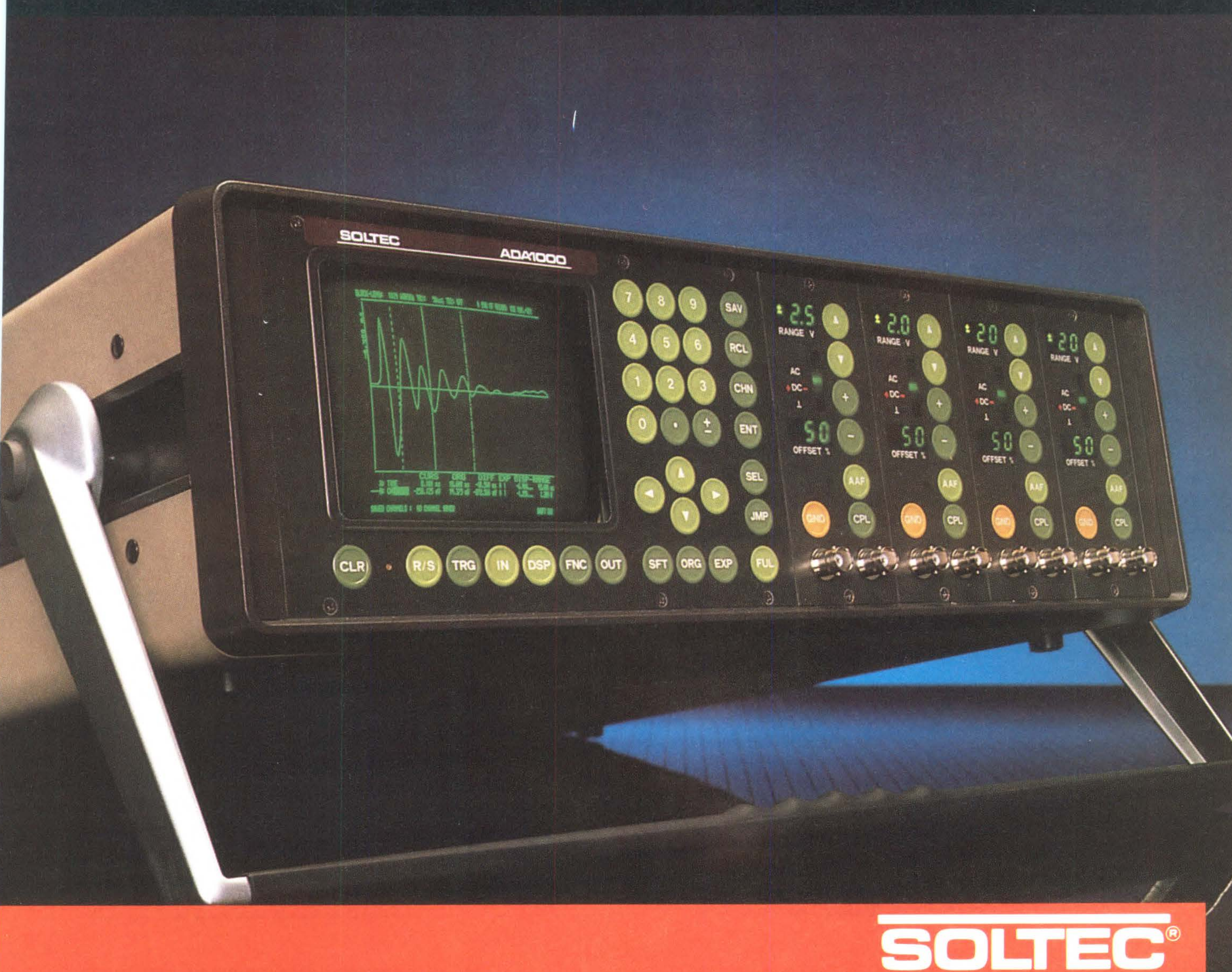

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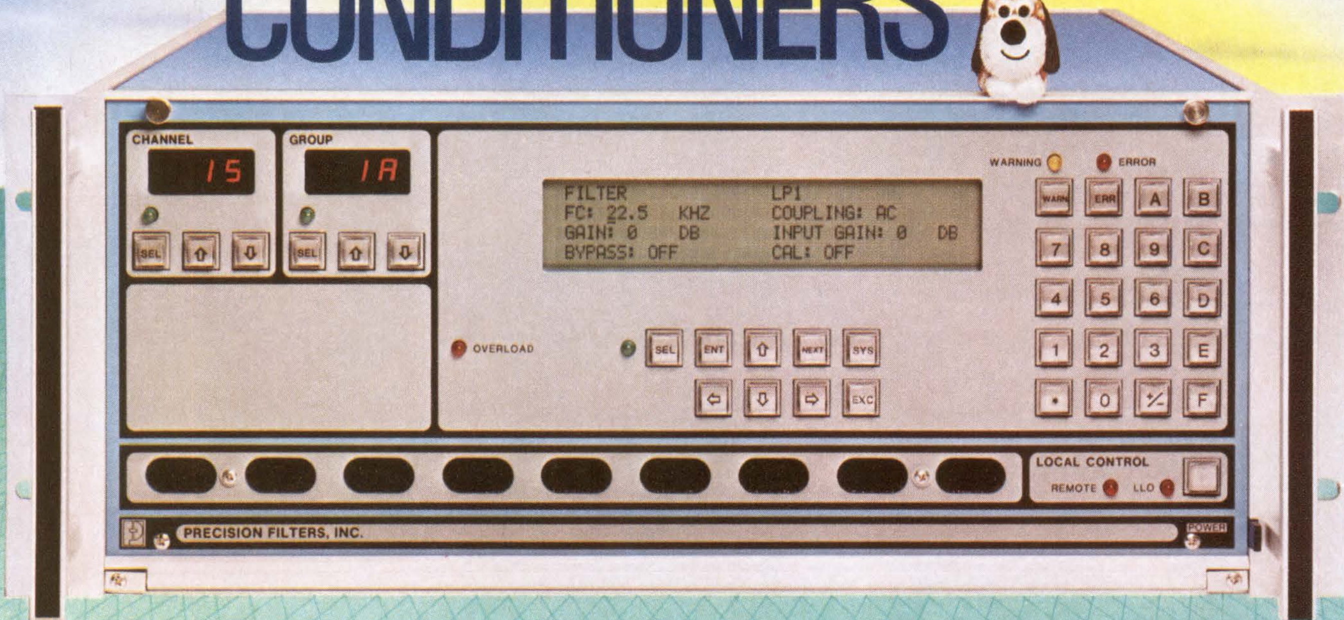

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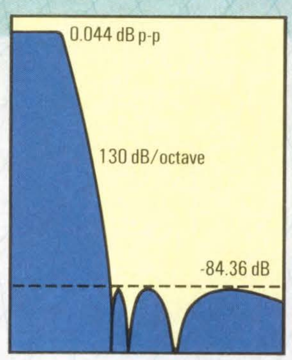

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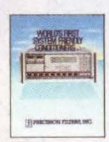

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CIRCLE NO 116.

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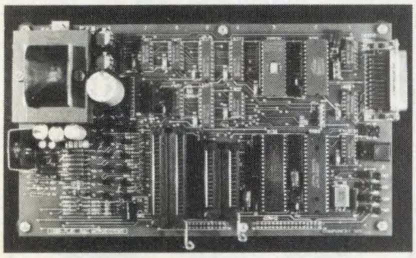

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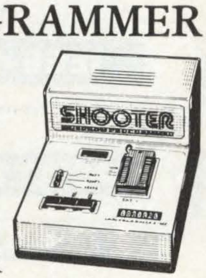

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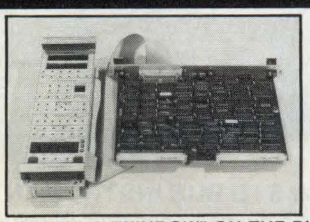

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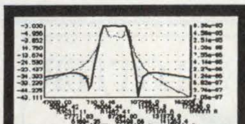

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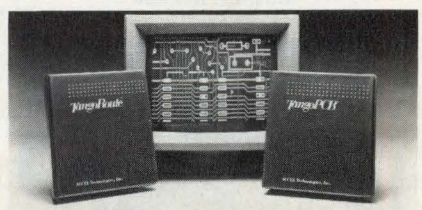

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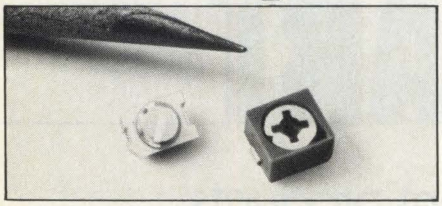

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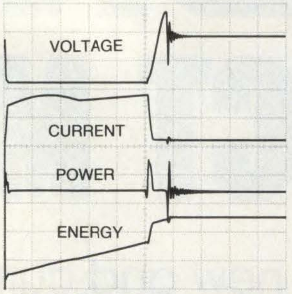

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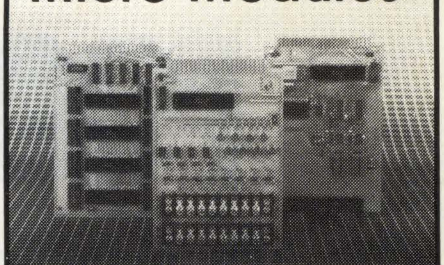

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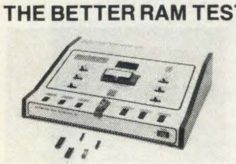

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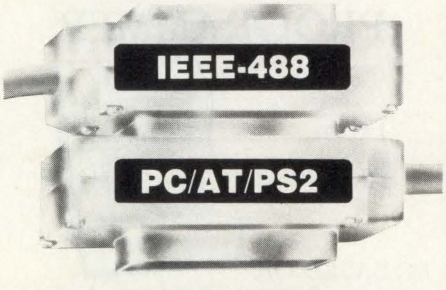

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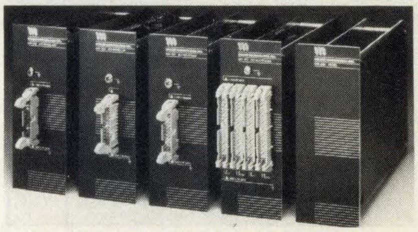

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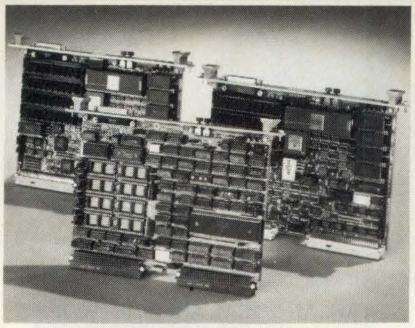

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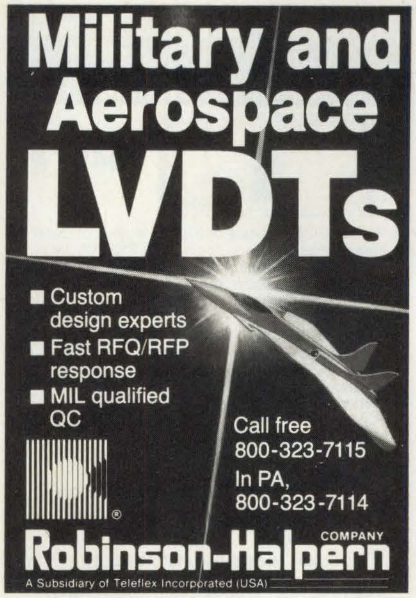

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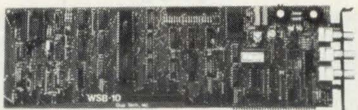

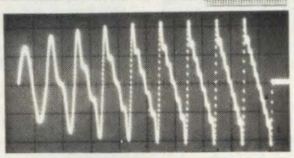

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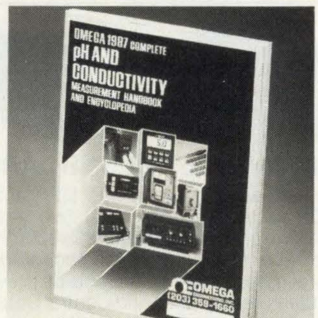

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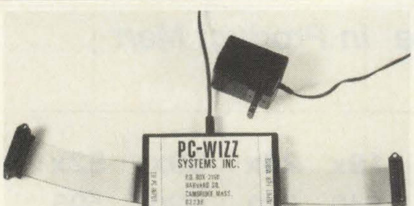

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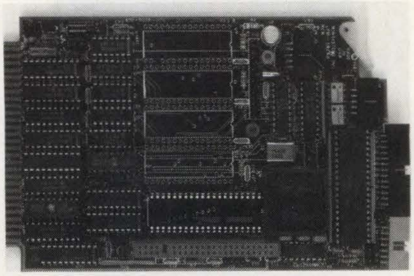

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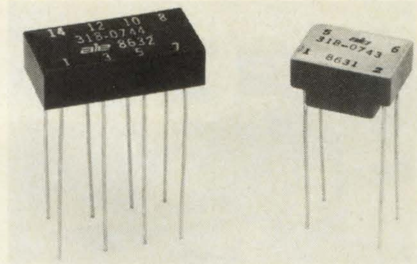

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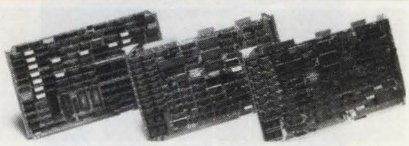

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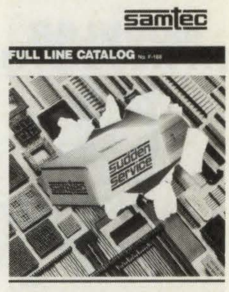

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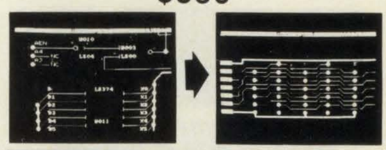

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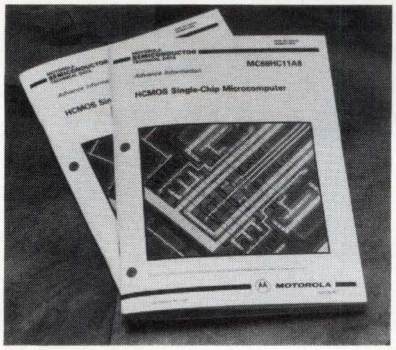

Brochure updates μC with EEPROM

The MC68HC11A8/D data sheet contains updated information on the MC68HC11A8 high-speed CMOS microcomputer with EEPROM. It has been entirely restructured to include new data on the bootstrap mode, updated parametrics, and examples of how to use the device.

Motorola, Literature Distribution Center, Box 20912, Phoenix, AZ 85036.

Circle No 424

Note discusses programming on simulator system

Product Note 8770S-2, *Effective Use of the HP 8770S Signal Simulator System*, offers programming help with the HP 1177A Waveform Generation Language. The 64-pg document presents principles of digital synthesis and provides product-specific information about the features and operation of the HP 8770S. It explains how to program six various waveforms from sine waves to frequency-hopped to multiple-tone carriers. Another section examines pulsed waveforms, pulsed carriers, and those with phase tagging, variable repetition rates and jitter, and pulse trains with AM and scan characteristics. Seven appendices complete the publication.

Hewlett-Packard Co, 1820 Embarcadero Rd, Palo Alto, CA 94303.

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Brochure and synopsis on PC-based T&M course

The R200 series of PC-based instrumentation laboratory courses contains a 500-pg course text with a variety of hardware packages. The applications include teaching labs, PC-based workstations, university courses, vocation technology for classrooms, and company training courses. Topics cover assembly and high-level programming languages, data acquisition, instruments, operating systems, and data links and buses. The text, with a selection of hardware packages, is priced from $999 to $2995.

Rapid Systems Inc, 433 N 34th St, Seattle, WA 98103.

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Hardcover book covers voice and data communications

The 325-pg *Telecommunications and Data Communications Factbook* provides information on communications technology, acronyms, numbering systems, formulas, and services. It also features a 75-pg glossary of terminology and abbreviations, directories of common carriers, major US exchange carriers, tariff references, state regulatory agencies, and interstate WATS areas. The World Numbering Plan, indexed both alphabetically and numerically, lists international and US/Canada area codes. This second edition also includes tutorials on traffic theory, as well as sections on local-area networks, artificial intelligence, fiber optics, and software. $39.95.

CCMI/McGraw-Hill, 50 S Franklin Turnpike, Ramsey, NJ 07446.

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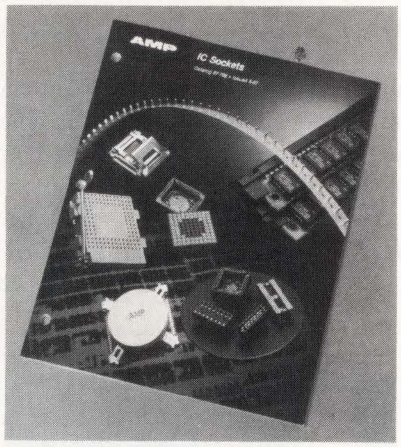

Catalog focuses on IC sockets

Catalog 87-798 lists IC sockets that remove the risk of soldering ICs directly onto pc boards. The 130-pg book divides IC sockets into two categories—production sockets and test and burn-in sockets. It provides photographs, drawings, and schematics, as well as detailed explanations of product features, performance characteristics, and materials. Its semiconductor-to-socket cross-reference chart matches common devices with complementing square and DIP sockets. The listings appear by manufacturer, part number, and description. Another special feature is a section on PGA (pin-grid array) patterns.

AMP Inc, Box 3608, Harrisburg, PA 17105.

Circle No 428

Video kit demonstrates building tool

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CIRCLE NO 115

plain the system's technology and its components, as well as interviews with customers who have developed commercial applications. $49.

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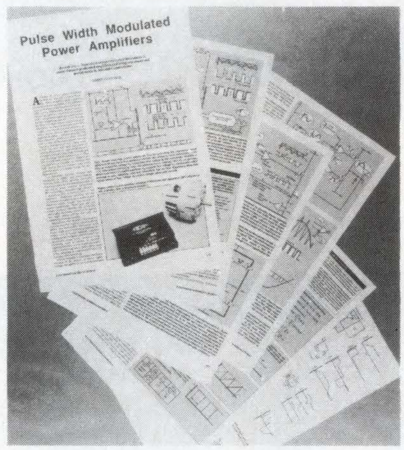

Paper discusses PWM amplifiers

The 6-pg reprint *Pulse Width Modulated Power Amplifiers* introduces PWM amplifiers starting with the basic principles. It discusses applications and compares PWM-amplifier technology with alternative linear amplifiers and SCR power systems. The article explains how applications fit into four broad categories of coil drivers, ac/dc power sources, motion control, and high-power function generators. Photographs and schematics highlight the text.

Copley Controls Corp, 375 Elliot St, Newton, MA 02164.

Circle No 430

Publication reports on software

The quarterly newsletter *Software Technology Report* details information about current software design and implementation, testing topics, and product reviews. Future reports will address such topics as how to design and implement machine-independent software modules and how to select programming languages. Annual subscription, $29. To obtain a free sample issue, send a self-addressed stamped envelope.

Software Technology Report, Microcomputer Applications, Box E, Suisun, CA 94585.

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Catalog lists IBM PC products

This 76-pg catalog describes data-acquisition hardware and data analysis/graphics software for the IBM PC, PC/XT, PC/AT, and PS/2 Model 30 μC and compatibles. It lists over 200 products. Items that are new to the booklet include general-purpose data-acquisition and -analysis software that requires no programming, as well as data-analysis software for gas and liquid chromatography. A special section on IBM industrial computers is also included.

Interactive Microware Inc, Box 139, State College, PA 16804.

Circle No 432

Software users' journal

Reference(Clipper): The Independent Guide to Clipper Expertise is designed to aid users of Clipper software. It provides programming tips, user-defined functions, database-management techniques, utility programs, and reviews and articles that deal with Clipper applications. Regular columns include features written by Clipper experts; reviews of Clipper-related products; Utility of the Month user-defined functions of the month; a column on networking solutions; an Expert's Log: Advanced Tutorial; Beginning User's Log; Advanced User's Log; and Procedure of the Month. The journal is published monthly. Annual subscription, $89; 2-year subscription, $160.

Pinnacle Publishing Inc, Box 1693, Tacoma, WA 98401.

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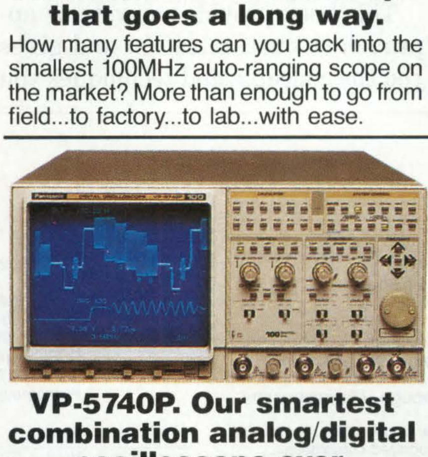

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CIRCLE NO 114

NEW BOOKS

Microprocessor-Based Design, by Michael Slater. 632 pgs; $39.95; Mayfield Publishing Co, Mountain View, CA, 1987. Phone (415) 960-0795.

This book guides you through designing efficient, cost-effective microprocessor-based hardware. It combines theory and practice, covering all commonly used microprocessors. It's illustrated with clear examples and includes a fully detailed design for a 68008-based controller system. Some advanced topics, including nonvolatile memory design, error-correcting codes, flat-panel display technology and interfacing, disk-drive interfacing, and multiple microprocessor systems, are also discussed.

dBASE III Plus For The Programmer, by Nelson T Dinerstein. 688 pgs; $22.95; Scott, Foresman and Co, Glenview, IL, 1987. Phone (312) 729-3000.

This book explains how to construct quality database systems using dBASE III Plus. It includes strategies for advanced system design; tips on programming for speed; debugging techniques and command tables; and numerous examples and illustrations. Besides covering such topics as local-area networks and C tools, it describes the differences between dBASE III and dBASE III Plus, and offers hints on how to take advantage of the changes.

Electronic Drafting and Design, 5th edition by Nicholas M Raskhodoff. 463 pgs; $37.95; Prentice-Hall Inc, Englewood Cliffs, NJ, 1987. Phone (201) 767-5937.

This edition covers the design and drafting techniques involved in the production of electronic equipment. It adds new dimensioning information based on the latest ANSI drawing standard and includes sections on surface-mount components and new interconnection systems. It also provides extensive coverage of VLSI and deals with modular equipment, racks and cabinets, chassis fabrication, and applicable military standards. All illustrations, drawings, and tables are updated.

Customizing AutoCAD, by Rusty Gesner and Joe Smith. 380 pgs; $34.95; New Riders Publishing, Thousand Oaks, CA, 1987. Phone (818) 991-5392.

This book provides a systems approach to customization and gives you the concepts and techniques you need to create your own application programs. You learn how to integrate AutoCAD with external programs, utilities, and DOS commands. Database topics include .DXF file processing, attribute extraction and importing database information, external manipulations, and reporting with Lotus 1-2-3 and dBASE. It discusses AutoLisp's theory and structure, showing you how to use AutoLisp to take control of the AutoCAD drawing editor, enhance it, and have your personal commands on line at all times. Included is a disk set that contains the AutoLisp library.

SMT—The Future of Electronics Assembly, by Charles-Henri Mangin and Stephen McClelland. 200 pgs; $159; CEERIS International Inc, Old Lyme, CT, 1987. Phone (203) 434-8740.

Incorporating state-of-the-art information on designing, deploying, and managing the introduction of surface-mount technology, this book details the design-for-producibility requirements and addresses the issues of component and delivery-format standardization. It analyzes the constraints associated with the management of an SMT assembly line, explains how to achieve the

highest practical first-pass yields, and reviews the performances of the available equipment for the entire board-populating process. It gives you a comprehensive view of the requirements of SMT assembly systems. It also includes case studies of such companies as I-Omega, Hewlett-Packard, Philips, Rank Xerox, and Texas Instruments.

Parallel Computing: Theory and Comparisons, by G Jack Lipovski and Miroslaw Malek. 384 pgs; $29.95; John Wiley & Sons Inc, New York, NY, 1987. Phone (201) 469-4400.

This book explores the basic principles used in the analysis and comparison of parallel computers. Its two main focuses are the extension of the space-time product used to measure the performance of systems and a graph-theoretical definition of interconnection networks. Other topics include elementary graphs and their relation to switches, computational energy and efficiency, inductive architecture and procedures, reliability, fault diagnosis, and fault tolerance.

Complete Handbook of Electronics Troubleshooting, by James W Jacox. 136 pgs; $27.95; Prentice-Hall Inc, Englewood Cliffs, NJ, 1987. Phone (201) 767-5937.

This handbook provides a logical approach to troubleshooting for any type of system. It describes the methods used by experienced technicians to isolate equipment malfunction rapidly and systematically and explains how to maintain equipment through inspection, testing, servicing, and repair. It emphasizes the need to know the equipment controls, specific equipment precautions, and the importance of recording observed data. It also introduces the use of an equipment functional block diagram, analyzes technical diagrams and testing procedures, and identifies a unique aspect of trouble isolation called bracketing.

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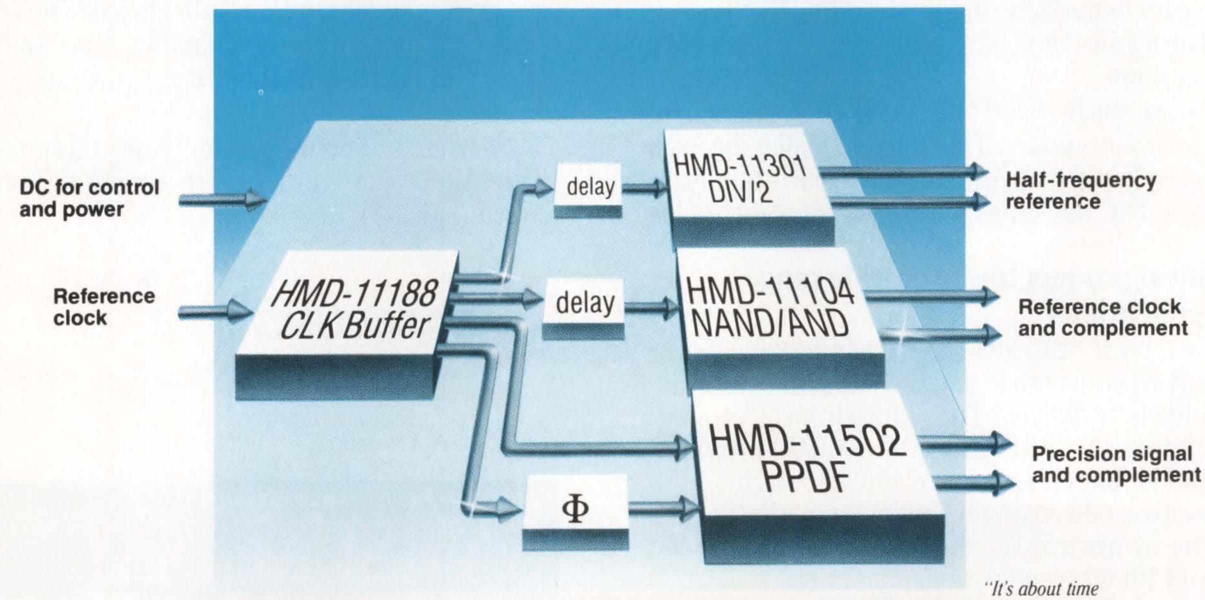

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CIRCLE NO 111

One design standard's unconventional making

Deborah Asbrand, *Associate Editor*

The evolution of a new design standard is usually anything but swift. In most cases, it takes years of meetings, reams of documents, and a virtually endless approval process before a new guideline receives a standards organization's seal of approval. The IEEE Standards Board, publisher of 500 standards to date, estimates that it studies a proposed standard an average of five years before endorsing it.

This past summer, however, five test-equipment manufacturers announced a proposed standard that they developed in just three months. The short period of time required for the creation of the suggested standard, the VME Bus Extension for Instrumentation, is testimony to the unusual cooperation among its five industry backers—Colorado Data Systems, Hewlett-Packard Co, Racal Dana Instruments, Tektronix, and Wavetek Corp. But, perhaps more importantly, it attests to the skill of the engineers who put aside their corporate affiliations and participated in a demanding joint venture to develop a criterion that other engineers could build to.

The proposed standard, also known as the VXIbus, is an open architecture for modular instruments based on the VME Bus and Eurocard standards. Its adoption will allow customers to plug different manufacturers' modules into the same card chassis. The largest market for so-called instruments-on-a-card is the military; the Army, Navy, and Air Force all sponsor their own modularization programs. Some companies, such as Colorado Data Systems, have been marketing modular instrumentation for use in the commercial sector since the mid-1970s. With the advent of a standard, though, some sources predict that commercial applications of the technology will account for 30% of the test and measurement market within five years.

Several factors influenced the timing of the five companies' move to develop a standard on their own. One factor was their unhappiness with the work being done by the user group of the Air Force's Modular Automated Test Equipment (MATE) program, which has had a subcommittee developing a standard since 1985. The subcommittee's pace was too slow for many participants. "Engineers from our company who went to the subcommittee meetings came back and said they weren't going to go to any more meetings," says Larry Desjardin, R&D section manager in Hewlett-Packard's Loveland, CO, Instrument Division.

Company loyalties

Even more frustrating for Desjardin, who is considered a principal contributor to the standard's development, were the partisan politics that blocked the subcommittee's discussion of the difficult technical issues, such as electromagnetic compatibility (EMC) between the modules and the configuration of the backplane. "A lot of the tough technical issues were brushed under the rug," says Desjardin. "People had their own private agenda and weren't interested in a standard. They wanted their own proprietary backplane to become the standard."

> *A watershed was reached when the companies consented to restrict participation in the standard's formulation to engineers.*

Meanwhile, it was growing clear that modular instrumentation's maturation as a profitable commercial and military market was near. It was also clear that test companies interested in breaking into the nascent market were extensively engaged in duplicative efforts. "There was a strong desire to get something happening because we were all in the middle of designs," says Fred Bode, manager of Wavetek Corp's Business Unit Systems Products and, by his own admission, a "shuttle diplomat" in efforts to organize the five-company cooperative.

When the larger test-equipment manufacturers such as Hewlett-Packard and Tektronix indicated interest, it seemed the time had come. The companies agreed that a standard would free them to do what they do best—design instrumentation.

Another factor also influenced the companies: They wanted to avoid having the military approve a standard that would most likely govern the commercial modular-instrumentation market as well. Not wanting to offend the military, however, the five companies agreed to develop a specification in time to present it at the MATE user group's July meeting.

Once the companies agreed to work collectively on the standard proposal, they adopted an egalitarian structure for the group, electing to rotate the chairmanship of the meetings among the five companies. They also agreed to rotate the meeting sites among the cities in which each was headquartered, taking turns as host and logistical director for the committee's lodging.

A watershed was reached, though, when the companies consented to restrict participation in the standard's formulation to engineers; no marketing representatives would sit in on the meetings. Ideally, standards are design decisions made by a group of engineers that represents the interests of the entire engineering community. In most cases, though, standards-committee members don't serve designers' interests so much as those of the companies they represent.

"We wanted to make sure we all had a common vision," says Dave Haworth, a program manager for Tektronix. "We didn't want things like marketing competitiveness wrapped up in what we were doing. Marketing [representatives] always want to sell the company, and we support that, but we wanted the VXIbus to represent the efforts of the whole group."

Putting their problem-solving training to work, the engineers set down strict ground rules. They agreed to give the effort three months of hard work. If little was accomplished in that time, they would abandon the project.

Open discussions

The group also decided that since its goal was to design an open architecture, all technical discussion would be open, unhindered by nondisclosure agreements of the sort that bind many joint industry efforts. "One way to guarantee that the focus would be on the standard and not on the products was to keep things totally open, with no legal agreements about what could and couldn't be disclosed," says Haworth.

The engineers set down strict ground rules: They agreed to abandon the project if little had been accomplished after three months.

Furthermore, it was agreed at the first meeting, hosted by Wavetek in San Diego, CA, that once the top-down architecture was established, no changes would be made except for alterations required by technical error. Members of the electrical, mechanical, power and EMC, and software and firmware groups had to work with the specifications set forth at the initial meeting.

At subsequent meetings, which lasted two to three days, an esprit de corps formed among the engineers. "It was a neat example of team building," says Desjardin. "Here were these people who were competitors, yet they developed real friendships." Group members usually worked together all day, ate dinner together, and then continued to work into the evening. They shared a sense of excitement over the technical issues under discussion. Desjardin recalls one meeting at which the computer terminals brought in for the engineers' use were set up in his suite. One morning, he awoke at 1:30 AM to find a crowd of engineers still gathered around the terminals.

The groups were not without problems, however. Devising a new set of specifications meant that the engineers had to swallow hard and at times accept decisions that they knew ran counter to their companies' plans. Each of the companies had to make concessions, but that was foreseen from the outset. "We knew from the start that we couldn't be protective of our own solutions," says Bode. "We understood that none of us was going to come out of this whole."

Meeting the three-month deadline also meant that there was no time for ego clashes. It was agreed that any decision that appeared to be leading to an outburst of temper would be tabled and raised for discussion again the next day. "If someone had a problem with something, we'd make it an issue and go back to it," says Wavetek project manager Allen Hollister, a member of the working group that studied the electrical system. Usually, says Hollister, when "someone who's argued violently for something comes back the next day, he'll say, 'You

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know, I think you guys were right.'"

The engineers were helped to meet their goals by their commitment not only to the standard but to other engineers. "It's a standard, but it's also a tutorial that helps other people so they can use it," says Haworth.

By early June, the subgroups were completing the documentation of their efforts, and in July, they presented the proposed standard to a meeting of the MATE user group. The user group is expected to comment on the standard at its November meeting. By then, the standard's architects hope to have ready a second draft that industry can begin using. A five-member committee is preparing the proposal for examination by the IEEE committee formed to study it.

The five companies are elated that the project has been such a success and proud that the cooperation that led to it is still possible in the ultra-competitive field of electronics. "It says something about our industry that this can still happen," says Brian Hull, vice president of sales and marketing for Racal Dana Instruments.

Lou Klahn, manager of advanced product planning for Colorado Data Systems, says he's pleased with the standard. Klahn is especially happy about it because he is chairman of the MATE subcommittee that has been working on an instrument-on-a-card standard since 1985. His subcommittee submitted its recommendations for a standard in 1986, but has yet to receive final approval because of the number of reviews the standard must undergo by military officials. Says Klahn of the industry effort, "I just wish they'd done it two years ago." **EDN**

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Nov. 26	Nov. 5	Microprocessor Technology Report & Directory; Analog ICs; Sensors & Transducers	
Dec. 10	Nov. 19	Product Showcase-Volume I; ICs and Semiconductors; Software	Closing: Nov. 12 Mailing: Dec.
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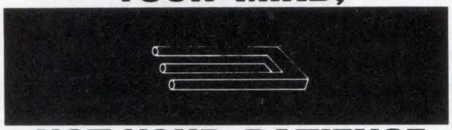

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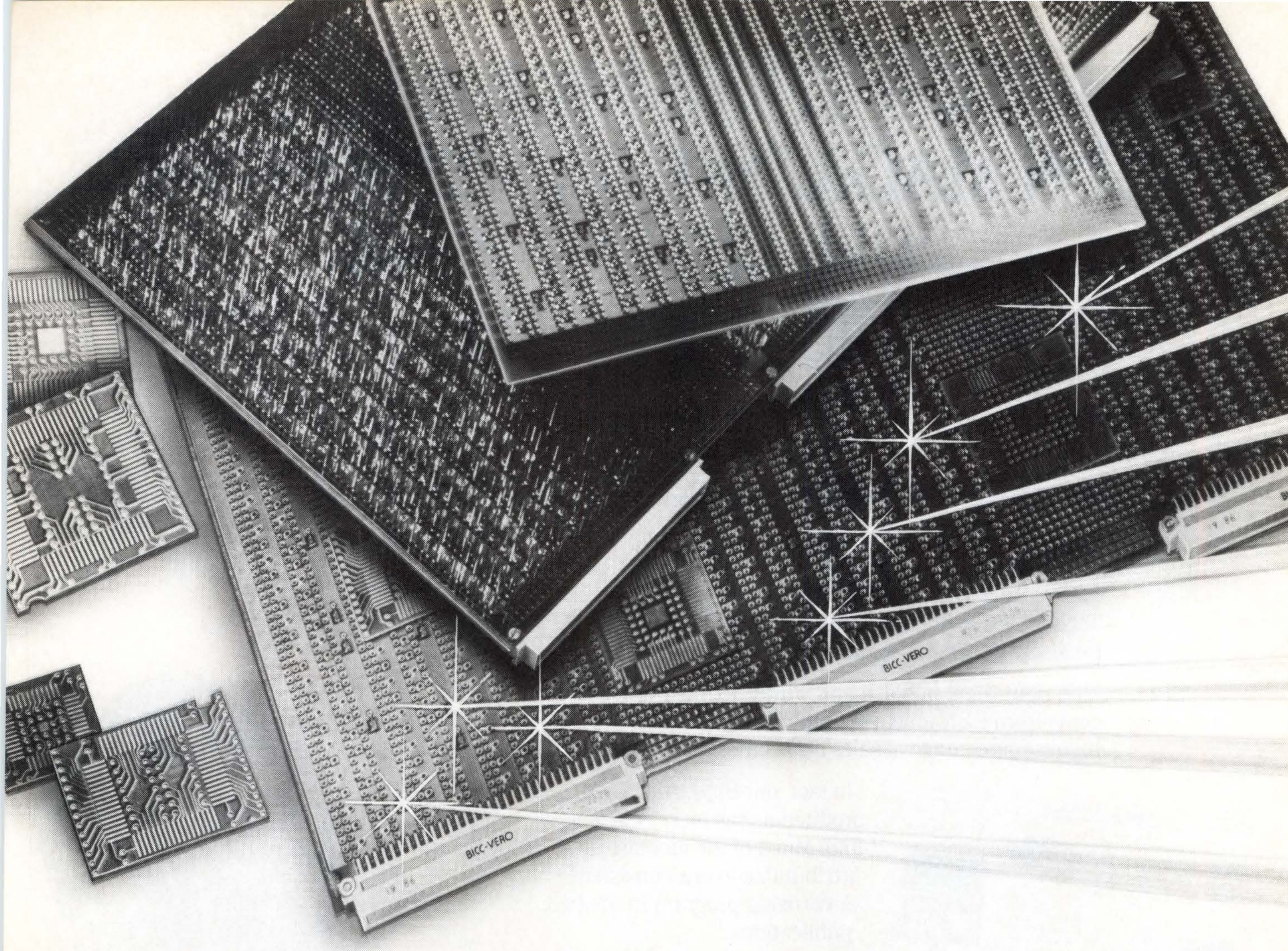

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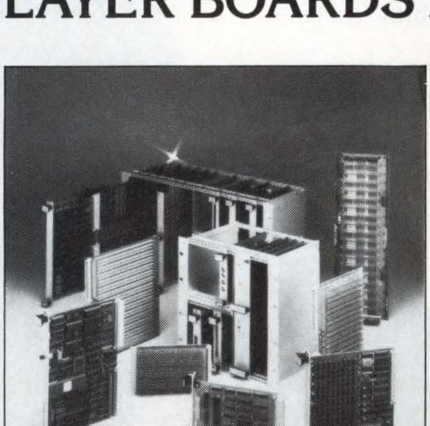

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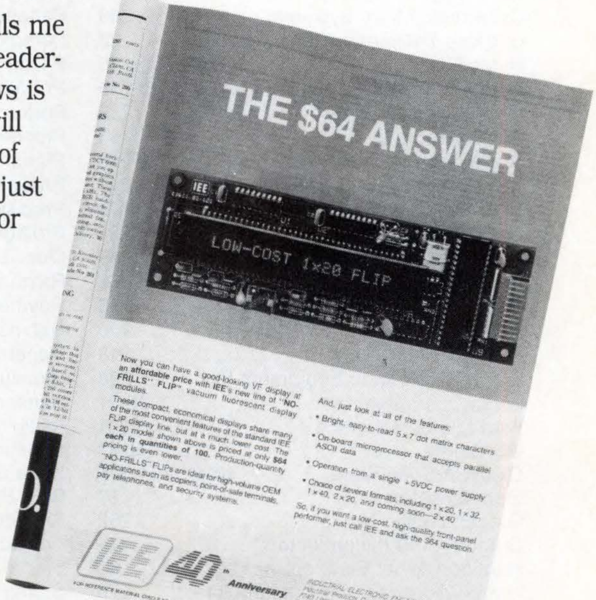

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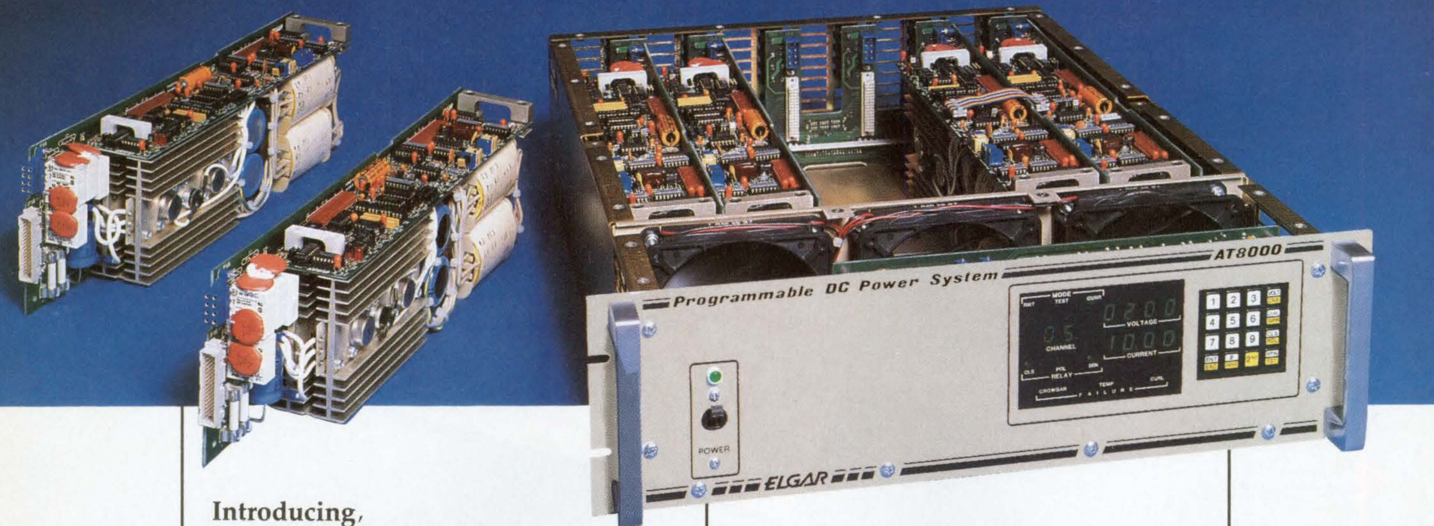

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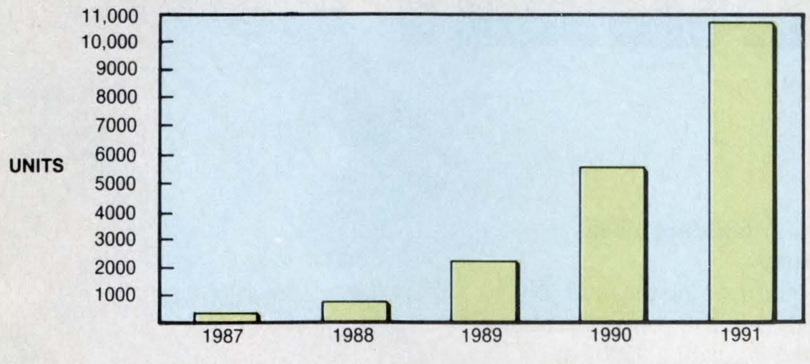

(SOURCE: VENTURE DEVELOPMENT CORP)

Availability of databases will define CD ROM sales

By the end of this year, the number of CD ROM drives sold could reach 30,000, forecasts Venture Development Corp (VDC) (Natick, MA), and sales of those drives should reach 1 million by 1991. The factory value of these sales will grow dramatically during this period, from \$20.7 million to \$168 million. Critical price reductions in hardware, averaging 35% per annum, as well as larger numbers of databases in CD ROMs, will be the major factors in market growth.

VDC points out that CD ROMs are frequently marketed incorrectly because of a perceived association with floppy- and hard-disk drives. Thus sellers try to market CD ROMs in much the same way as they do magnetic disk storage, and users approach them in a similar way. But CD ROMs can't replace floppy- and hard-disk drives. The fact that you can store large quantities of material on CD ROM for playback constitutes only their principal usefulness. Therefore sellers (and users) should approach these devices more as if they were offering (and purchasing) the contents of a particular database on ROM disk rather than a storage device per se.

Database publishers will, in the long run, decide the fate of the CD ROM industry. Good database titles will dictate how successful the sales of the drives themselves are. Fortunately, forecasts for the expansion of available CD ROM titles are very good. In 1986, the first year that CD ROMs were sold in significant numbers, 75 database titles were offered for sale. In 1987, the number has grown to 125. However, by 1991, VDC estimates that more than 10,000 titles will be on the market.

Application areas for CD ROMs are wide and varied; they include financial, educational-librarian, scientific-medical, legal-journalistic, and consumer areas. For most of these sectors, database publishers will control the sales and leases of CD ROMs. In the consumer segment, on the other hand, retailers will have to provide the primary means of sales.

Two other kinds of optical-disk drives, WORM (write once/read many) and erasable, will influence the CD ROM market significantly. Shipments of erasable optical-disk drives are not expected to have an impact until the end of 1988. But once that market is firmly established, it will seriously curb the growth of the CD ROM market because the erasable optical-disk techonolgy is interchangeable with magnetic media in some instances. WORM optical disks, on the other hand, should affect CD ROM markets less substantially. Security is the main advantage of the WORM disks and drives because internal databases can be created without any third parties.

Military will continue to dominate GaAs ICs

The market for gallium arsenide wafers will grow at an annual rate of 26.1% from this year through 1991, according to The Information Network of San Francisco, CA. The market-research company's evaluation of various device markets, including FETs, analog ICs, digital ICs, diode lasers, LEDs, photo voltaics, infrared photodetectors, optoelectronic ICs, and photonic ICs, indicates that the primary driving force behind the GaAs chip market is specialized miltary applications, along with some commercial R&D efforts. The market for military analog ICs remains dominant in spite of commercial product introductions. The commercial "MSI and pseudo-LSI devices," the study concludes, have been unimpressive.

Although growth has and will occur, the GaAs market has not met expectations of a few years ago. One problem stems from difficulties in achieving higher levels of integration. FET limits, such as back gating, are now overshadowing long anticipated problems like material, packaging, and testing. In addition, according to The Information Network, while Japanese semiconductor companies have shown strong commitments to GaAs devices in consumer products such as facsimile machines, compact-disk players, laser copiers and printers, and fiber-optic devices, US manufacturers have, by and large, maintained a wait-and-see attitude in the development of GaAs products for consumers.

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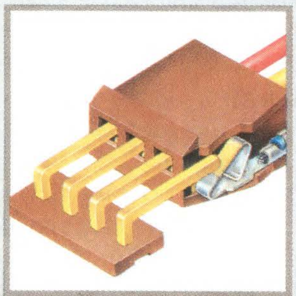
FLEXIBILITY & RELIABILITY

Eleven different components are your building blocks for thousands of interconnection solutions.

Molex's unique family of KK® connectors provide the flexibility you need to build interconnections precisely suited to your applications. Choose either tin or cost-effective selective gold plating, .100″ or .156″ center spacing. Crimp, solder, or insulation displacement termination…top, side, or bottom pin entry…break-to-size pin headers…they're all standard in thousands of demanding applications.



Gold plating placed selectively on terminal contact points means added economy.

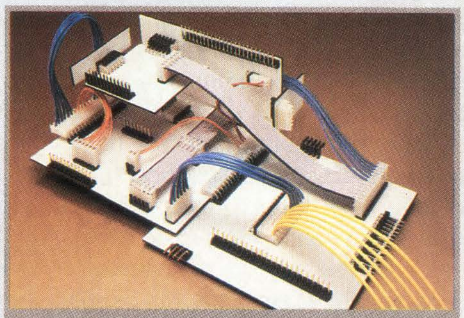
The KK® connector is just one example of how we take a total systems approach.

The KK® System includes a complete line of wire termination tooling from simple hand crimp tools to the latest automated insulation displacement technology. The System also features sophisticated pinsetting equipment. Molex goes beyond merely supplying connectors to help today's manufacturers achieve lower installed costs.

Intensive QC programs provide reliable connectors that stand up to tough environmental conditions in a wide range of electronic applications.

Dependable service worldwide.

Our multi-national organization offers you interconnection design, manufacturing, and technology from around the globe, with dependable supply and local service. Molex distributors stock the full line of flexible KK® connectors for your every need.



Unique break-away design allows you to order pin headers in bulk and break off the exact lengths you need to save on inventory and waste.

molex®

Service To The Customer…Worldwide

***Corporate Headquarters:** 2222 Wellington Ct., Lisle, IL 60532 USA, (312) 969-4550 • **European Headquarters:** Aldershot, England, (0252)318221*
***Northern Asia Headquarters:** Tokyo, Japan, 03-478-8777 • **Southeast Asia Headquarters:** Jurong Town, Singapore, 65-261-9733*

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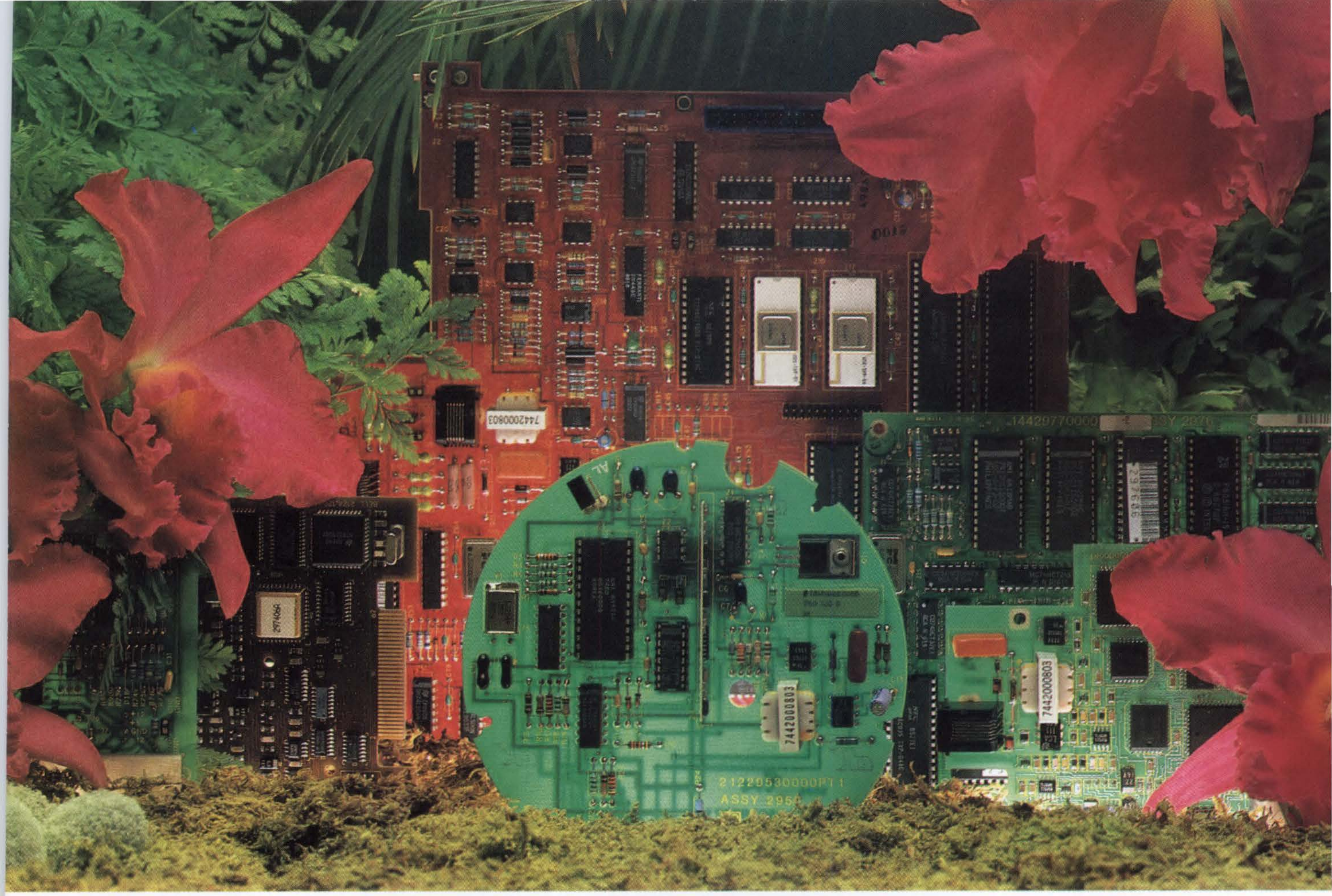


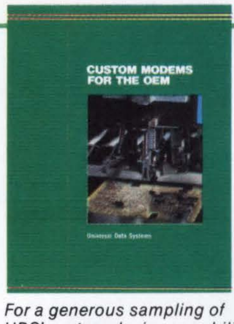
Exotic Customs at UDS

The special requirements of data communications OEMs have resulted in some pretty exotic custom modem cards from Universal Data Systems.

Funny form factors are routine fare for our custom designers. Nooks, crannies and odd card configurations are no problem, given sufficient square inches of real estate. UDS engineers have even designed a circular 212A modem that fits in the back of a residential electric meter.

Non-standard modem functions are another specialty of the house. For example, UDS engineers have already designed and delivered a hand-held RF modem operating at 4800 bps!

UDS has successfully handled more than 3,000 custom OEM modem design assignments — and we can handle yours. To begin an exotic custom, contact Universal Data Systems, 5000 Bradford Drive, Huntsville, AL 35805. Telephone 205/721-8000; Telex 752602 UDS HTV.



For a generous sampling of UDS' custom design capabilities, ask for the new, free OEM modem brochure.

Universal Data Systems

MOTOROLA INC.
Information Systems Group

UDS modems are offered nationally by leading distributors. Call the nearest UDS office for distributor listings in your area.
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